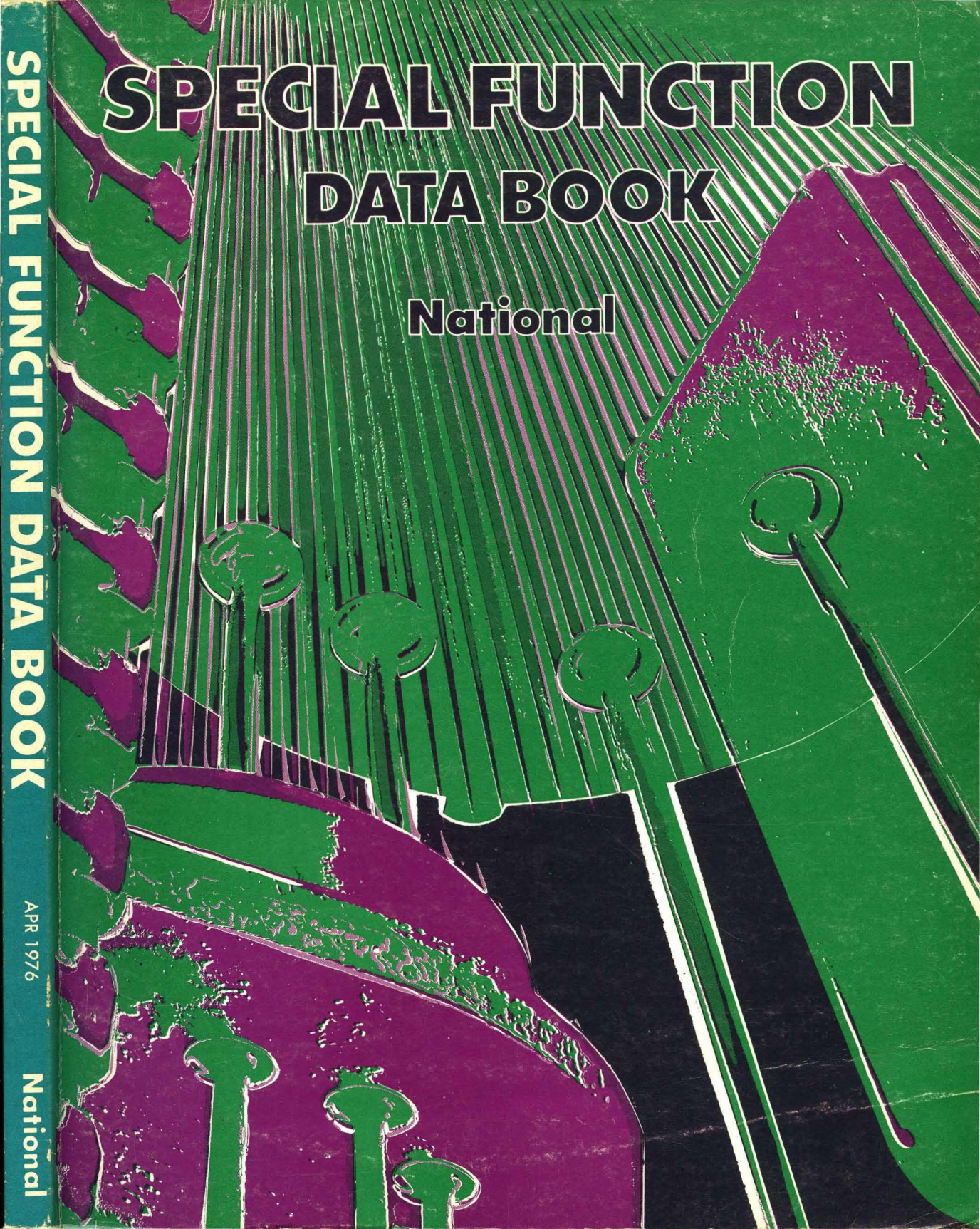
SPECIAL FUNCTION DATA BOOK

National



SPECIAL FUNCTION DATA BOOK

APR 1976

National

Edge Index by Function

Here is the new Special Function Analog and Digital Circuits data book. It contains detailed information for specifying and applying special amplifiers, buffers, clock drivers, analog switches, and D/A-A/D converter products.

For information regarding newer devices introduced since the printing of this handbook, or for further information on the listed parts, please contact our local representative, distributor or regional office.

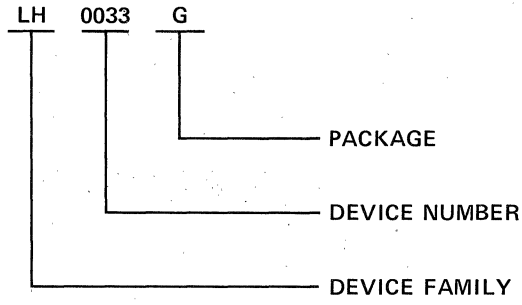
Printed in U.S.A.

Manufactured under one or more of the following U.S. patents: 3083262, 3189758, 3231797, 3303356, 3317671, 3323071, 3381071, 3408542, 3421025, 3426423, 3440498, 3518750, 3519897, 3557431, 3560765, 3566218, 3571630, 3575609, 3579059, 3593069, 3597640, 3607469, 3617859, 3631312, 3633052, 3638131, 3648071, 3651565, 3693248.

Ordering Information

For available packages, consult each data sheet. Then refer to the package drawings in the back of the book.

The ordering information for National devices covered in this catalog is as follows:



DEVICE FAMILY

AD – Hybrid Analog to Digital Converter
AF – Active Filter
AH – Hybrid Analog Switch
AM – Monolithic Analog Switch
DA – Hybrid Digital to Analog Converter
DH – Hybrid Digital Driver
DM – Monolithic Bipolar Digital Product
LF – Monolithic BI-FET Product
LH – Hybrid Linear Circuit
LM – Monolithic Linear Product
MH – Clock Driver
MM – Monolithic MOS Product
RA – Resistor Array

PACKAGE

D – Glass/Metal Dual-In-Line Package
F – Flat Package
G – TO-8 (12 lead) Metal Can
H – TO-5 (multi-lead) Metal Can
J – Glass/Glass Dual-In-Line Package
K – TO-3 (8 lead) Metal Can
N – Molded Dual-In-Line Package

DEVICE NUMBER

2 to 6 digit number.

Suffix Indicators are used to define specific electrical grades. Consult individual data sheet.

National Semiconductor Corp. • 2900 Semiconductor Drive • Santa Clara, California 95051 • (408) 732-5000, TWX: (910) 339-9240

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RESISTOR ARRAYS – SECTION 9

Alpha-Numerical Index

MILITARY TEMPERATURE RANGE: -55°C to +125°C

Device	Input Offset Voltage Max (mV)	Input Offset Voltage Drift Typ (μV/°C)	Input Offset Current Max (nA)	Input Bias Current Max (nA)	Voltage Gain Min (Volts/V)	Bandwidth A_V = 1 Typ (MHz)	Slew Rate A_V = 1 Typ (V/μs)	Output Current (mA)	Supply Voltage Min (V)	Supply Voltage Max (V)	Common Mode Range (V)	Differential Input Voltage (V)	Supply Current Max (mW)	Compensation Components	Package Types
LH0001	1	4	20	100	25,000	1	.25	±5	±5	±20	$\pm V_S$	±7	5	2	TO-5
LH0001A	2.5	3	20	100	25,000	1	.25	±5	±5	±20	$\pm V_S$	±7	5	2	TO-5 DIP F, P
LH0002	30	(Note 2)	10×10^3	10^4	.95	50	100	±100	±5	±22	$\pm V_S$	(Note 2)	100	0	TO-5 DIP
LH0003	3	4	200	2,000	15	30 (Note 1)	30 (Note 1)	±50	±5	±20	$\pm V_S$	±7	30	2	TO-5
LH0004	1	4	20	100	30	1	.25	±15	±5	±45	$\pm V_S$	±7	1.5	2	TO-5
LH0005	10	20	20	50	2	30 (Note 1)	20 (Note 1)	±50	±9	±20	$\pm V_S$	±15	90	3	TO-5
LH0020	2.5	10	50	250	100,000	1	.25	±40	±5	±22	$\pm V_S$	±30	50	2	TO-5
LH0021	3	3	100	300	100,000	1	3	±1,000	±5	±18	$\pm V_S$	±30	35	0	TO-3
LH0022	4	5	.002	.01	100,000	1	3	±10	±5	±22	$\pm V_S$	±30	35	0	TO-5 DIP F, P
LH0024	4	20	3×10^3	20×10^3	4,000	50	400	±100	±9	±18	$\pm V_S$	±5	252	1	TO-5
LH0032	5	25	.01	.02	1,000	50	500	±100	±5	±18	$\pm V_S$	±30	200	2	TO-8
LH0033	10	(Note 3)	(Note 3)	.1	.97 (Note 3)	100	1,500	±100	±5	±20	$\pm V_S$	(Note 3)	220	0	TO-8 8 PIN J
LH0041	3	3	100	300	100,000	1	3	±200	±5	±18	$\pm V_S$	±30	35	0	TO-8 8 PIN J
LH0042	20	5	.005	.025	50,000	1	3	±10	±5	±22	$\pm V_S$	±30	35	0	TO-5 DIP F, P
LH0044	.050	.2	5	30	500,000	.4	.06	±1.3	±3	±20	$\pm V_S$	±15	4	0	TO-5
LH0044A	.025	.1	2.5	15	1,000,000	.4	.06	±1.3	±3	±20	$\pm V_S$	±15	3	0	TO-5
LH0052	.5	2	.0001	.001	100,000	1	3	±10	±5	±22	$\pm V_S$	±30	25	0	TO-5 DIP
LH0061	4	5	100	300	50,000	15	70	±500	±5	±18	$\pm V_S$	(Note 4)	100	1	TO-3
LH0062	5	5	.001	.025	50,000	15	70	±6	±5	±20	$\pm V_S$	±30	80	0	TO-5 DIP
LH0063	25	(Note 1)	(Note 3)	.2	.96 (Note 3)	150	6,000	±400	±5	±18	$\pm V_S$	(Note 3)	500	0	TO-3
LH2101A	3	15	20	100	50,000	1	.5	7.5	±3	±22	±12	±30	3	1	DIP F, P
LH2108	3	15	.4	3	50,000	1	.3	1	±2	±20	±14	(Note 4)	.6	1	DIP F, P
LH2108A	1	5	.4	3	80,000	1	.3	1	±2	±20	±14	(Note 4)	6	1	DIP F, P
LH2110	6	12		10	.999	20	30	1	±5	±18	±10		5.5	0	DIP F, P
LH24250	4		5	15	100,000	.25	.16	.75	±1	±18	±12	±15	.03 set	0	DIP F, P

Note 1: Specified for A_V = -10.

Note 2: Current booster.

Note 3: Voltage follower.

Note 4: Inputs have shunt-diode protection; current must be limited.

Military Hybrid Op Amp Selection Guide

INDUSTRIAL TEMPERATURE RANGE: -25°C to +85°C

Device	Input Offset Voltage Max (mV)	Input Offset Voltage Drift Typ (μV/°C)	Input Offset Current Max (nA)	Input Bias Current Max (nA)	Voltage Gain Min (Volts/V)	Bandwidth A_V = 1 Typ (MHz)	Slew Rate A_V = 1 Typ (V/μs)	Output Current (mA)	Supply Voltage Min (V)	Supply Voltage Max (V)	Common Mode Range (V)	Differential Input Voltage (V)	Supply Current Max (mW)	Compensation Components	Package Types
LH0001AC	5	3	60	200	.25	1	.25	±5	±5	±20	$\pm V_S$	±7	1.3	2	TO-5 DIP F, P
LH0002C	30	(Note 2)	10×10^3	10^4	.95 (Note 2)	50	100	±100	±5	±22	$\pm V_S$	(Note 2)	100	0	TO-5 DIP
LH0003C	3	4	200	2,000	15,000	30 (Note 1)	30 (Note 1)	±50	±5	±20	$\pm V_S$	±7	30	2	TO-5
LH0004C	1.5	4	45	120	30,000	1	.25	±15	±5	±45	$\pm V_S$	±7	1.5	2	TO-5
LH0005C	10	25	25	100	2,000	30 (Note 1)	20 (Note 1)	±50	±9	±20	$\pm V_S$	±15	90	3	TO-5
LH0020C	6	10	200	500	50,000	1	.25	±100	±5	±18	$\pm V_S$	±30	50	2	TO-5
LH0021C	6	5	200	500	100,000	1	3	±1,000	±5	±18	$\pm V_S$	±30	40	0	TO-3
LH0022C	6	5	.005	.025	75,000	1	3	±10	±5	±22	$\pm V_S$	±30	24	0	TO-5 DIP F, P
LH0024C	8	25	5×10^3	22×10^3	3,500	50	400	±100	±9	±18	$\pm V_S$	±5	252	1	TO-5
LH032C	15	25	02	.5	700	50	500	±100	±5	±20	$\pm V_S$	±30	220	2	TO-8
LH0033C	20	(Note 3)	(Note 3)	.15	.96 (Note 3)	100	1,500	±100	±5	±20	$\pm V_S$	(Note 3)	240	0	TO-8 8 PIN J
LH0041C	6	5	200	500	100,000	1	3	±200	±5	±18	$\pm V_S$	±30	40	0	TO-8 8 PIN J
LH0042C	20	10	.01	.05	25,000	1	3	±10	±5	±22	$\pm V_S$	±30	28	0	TO-5 DIP F, P
LH0044AC	.025	.5	2.5	15	1,000,000	.4	.06	±1.3	±3	±20	$\pm V_S$	±15	3	0	TO-5
LH0044B	.050	.5	5	30	500,000	.4	.06	±1.3	±3	±20	$\pm V_S$	±15	4	0	TO-5
LH0044C	.150	1	5	30	500,000	.4	.06	±1.3	±3	±20	$\pm V_S$	±15	4	0	TO-5
LH0052C	1	5	0002	.005	75,000	1	3	±10	±5	±22	$\pm V_S$	±30	30	0	TO-5 DIP
LH0061C	10	5	200	200	25,000	15	70	±500	±5	±18	$\pm V_S$	(Note 4)	150	1	TO-3
LH0062C	15	10	.002	.065	25,000	15	70	±6	±5	±20	$\pm V_S$	±30	120	0	TO-5 DIP
LH0063C	50	(Note 3)	(Note 3)	.2	.96 (Note 3)	150	6,000	±400	±5	±18	$\pm V_S$	(Note 3)	500	0	TO-3
LH2201A	2	15	20	75	25,000	1	.5	5	±3	±22	±12	±30	3	1	DIP F, P
LH2208	2	15	.2	2	50,000	1	.3	1	±2	±20	±14	(Note 4)	.4	1	DIP F, P
LH2208A	.5	5	.2	2	80,000	1	.3	1	±2	±20	±14	(Note 4)	.4	1	DIP F, P
LH2210	4			3	.999	20	30	1	±5	±18	±10		5.5	0	DIP F, P

Note 1: Specified for A_V = -10. **Note 2:** Current booster. **Note 3:** Voltage follower. **Note 4:** Inputs have shunt-diode protection; current must be limited.

COMMERCIAL TEMPERATURE RANGE: 0°C to +70°C

LH2301A	7.5	30	50	250	25,000	1	.5	5	±3	±18	±12	±30	3	1	DIP F, P
LH2308	7.5	30	1	7	25,000	1	.3	1	±2	±18	±14	(Note 1)	.8	1	DIP F, P
LH2308A	.5	5	1	7	80,000	1	.3	1	±2	±20	±14	(Note 1)	.8	1	DIP F, P
LH2310	7.5	*	*	7	.999	20	30	1	±5	±18	±10	*	5.5	0	DIP F, P
LH24250C	6	*	10	30	75,000	.25	.16	.75	±1	±18	±12	±15	.03 set	0	DIP F, P

*Not specified. †Guaranteed at +25°C. **Note 1:** Inputs have shunt-diode protection; current must be limited.

Industrial and Commercial Hybrid Op Amp Selection Guide

Device No.	Package	National Pin for Pin Equivalent	Nearest National Equivalent
Analog Devices			
AD503J, K	TO-5	LH0042CH	
AD503S	TO-5	LH0042H	
AD506J, K, L	TO-5	LH0022CH	
AD506S	TO-5	LH0022H	
AD511	MOD		LH0042
AD513J, K	TO-5	LH0042CH	
AD513S	TO-5	LH0042H	
AD514J, K, L	TO-5		LH0042CH
AD514S	TO-5		LH0042H
AD516J, K	TO-5	LH0022CH	
AD516S	TO-5	LH0022H	
AD523J, K, L	TO-5		LH0052CH
AD528J, K	TO-5		LH0062CH
AD528S	TO-5		LH0062H
AD540J, K	TO-5		LH0042CH
AD540S	TO-5		LH0042H
ADP517	MOD		LH0042CH
M501A, B, C	TO-8		LH0022CH
40J, K	TO-8		LH0042CH
41J, K, L	MOD		LH0052CH
42J, K, L	MOD		LH0052CH
43J	MOD		LH0022CH
44J, K	MOD		LH0062CH
45J, K	MOD		LH0062CH
142A, B, C	MOD		LH0042CH
146J, K	MOD		LH0022CH
149J, K	MOD		LH0062CH
Bell and Howell			
20-008	MOD		LH0042CH
20-108	MOD		LH0042CH
20-208	TO-8		LH0022H
20-248	TO-8		LH0022CH
Burr-Brown			
3521L	TO-99		LH0022CH
3542J	TO-99	LH0042CH	
3542S	TO-99	LH0042H	
3542SQ	TO-99	LH0042H/883	
3506J	TO-99	LH0022CH	
3508J	TO-99	LH0062CH	
3348/03	DIL		LH0022CD
3349/03	DIL		LH0022CD
3350/03	DIL		LH0042CD
3503A	TO-99	LH0042CH	
3503B	TO-99	LH0042H	
3503C	TO-99	LH0022CH	
3503R	TO-99	LH0022H	
3503S	TO-99	LH0052CH	
3503T	TO-99	LH0052H	
Datel			
AM405-2	TO-99	LH0042CH	
AM406-2	TO-99	LH0042CH	
AM100A	MOD		LH0062H
AM100B	MOD		LH0062CH
AM102A	MOD		LH0062H
AM102B	MOD		LH0062CH
Fairchild			
U5B7740312 (μA740)	TO-5	LH740AH	
U5B7740393 (μA740C)	TO-5	LH740ACH	

Device No.	Package	National Pin for Pin Equivalent	Nearest National Equivalent
Helex			
XH0032	TO-8	LH0032CG	
Harris			
HA2050	TO-99	LH0042H	
HA2055	TO-99	LH0042CH	
HA2050A	TO-99	LH0022H	
HA2055A	TO-99	LH0042CH	
HA2060	TO-99	LH0062H	
HA2065	TO-99	LH0062CH	
HA2060A	TO-99	LH0062H	
HA2065A	TO-99	LH0062CH	
Intech			
A-100	MOD		LH0042
A-101	MOD		LH0042CH
A-102	MOD		LH0022CH
A-103	MOD		LH0022CH
A-122	MOD		LH0052CH
A-123	MOD		LH0052CH
A-125	MOD		LH0062CH
A-130	MOD		LH0062CH
A-131	MOD		LH0062CH
A-136	MOD		LH0062CH
A-137	MOD		LH0062CH
A-148A, B, C	MOD		LH0042CH
1-1026	MOD		LH0022CH
A-1027	MOD		LH0022CH
Intersil			
ICH8500	TO-5	LH0052H	
ICH8500A	TO-5	LH0052H	
ICH8500C	TO-5	LH0052CH	
ICH8007C	TO-5	LH0042CH	
ICH8007M	TO-5	LH0042H	
ICL8007AM	TO-5	LH0042H	
ICL8007AC	TO-5	LH0042CH	
Intronics			
FA530	MOD		LH0062CH
FA531	MOD		LH0062CH
FA540	MOD		LH0042CH
FA541	MOD		LH0042CH
Optical Electronics, Inc. (OEI)			
9712	MOD		LH0032CG
9725	MOD		LH0032CG
9731	MOD		LH0032G
9738	MOD		LH0032G
9718	MOD		LH0062CH
9726	MOD		LH0062CH
9727	MOD		LH0062CH
9715	MOD		LH0062CH
9721	MOD		LH0062CH
9723	MOD		LH0062CH
9733	MOD		LH0052CH
9720	MOD		LH0032CH
9729	MOD		LH0052CH
Signetics			
SU536T	TO-5	LH0042CH	
NE536T	TO-5	LH0042CH	
SU740T	TO-5	LH740ACH	
NE740T	TO-5	LH740ACH	

Device No.	Package	National Pin for Pin Equivalent	Nearest National Equivalent
Siliconix			
L120A	TO-5		LH0042H
L120C	TO-5		LH0042CH
L137AA	TO-5		LH0022H
L137CA	TO-5		LH0022CH
Teledyne Philbrick Nexus			
QFT	MOD		LH0042CH
QFT-2	MOD		LH0042CH
QFT-2A	MOD		LH0022CH
QFT-2B	MOD		LH0052CH
QFT-5	MOD		LH0042CH
Q25AH	TO-8		LH0042CH
PP25A	MOD		LH0042CH
1003	MOD		LH0052CH
100301	MOD		LH0052CH
1006	MOD		LH0042CH
1008	MOD		LH0042CH
1009	MOD		LH0042CH
100901	MOD		LH0042CH
100902	MOD		LH0042CH
1011	MOD		LH0062CH
101101	MOD		LH0062CH
101102	MOD		LH0062CH
1021	MOD		LH0022CH
1023	MOD		LH0052CH
102301	MOD		LH0052CH
1025	MOD		LH0032CG
1408	MOD		LH0052CH
140801	MOD		LH0052CH
140802	MOD		LH0052CH
140810	TO-8		LH0052CH
1402	TO-8		LH0042CH
140201	TO-8		LH0042CH
140202	TO-8		LH0042CH
1407	TO-8		LH0042CH
140701	TO-8		LH0042CH
1414	MOD		LH0062CH
141410	DIP		LH0062CH
1421	TO-5		LH0042CH
Zeltex			
ZA801/M1/M2/M3	MOD		LH0042CH
ZA801T1	TO-8		LH0042CH
ZA801D1	DIL		LH0042CH
ZA801E1	DIL		LH0042CH
ZA802M1, M2	MOD		LH0022CH
ZA803M1	MOD		LH0042CH
ZA804M1, M2	MOD		LH0042CH
ZA903M1, M2	MOD		LH0042CH
ZA910M	MOD		LH0062CH
133	MOD		LH0022CH
133-03	MOD		LH0052CH
133-04	MOD		LH0022CH
134	MOD		LH0042CH
134D	MOD		LH0042CH
135	MOD		LH0062CH

Fet OP Amp Cross Reference Guide

Device Number	Function	National Functional Equivalent
Dixon		
DAS2114	SPDT – 100 ohm	AH2114 (pin for pin)
DAS2126	SPDT – 50 ohm	AH0162
DAS2128	Quad SPST – 50 ohm	2-AH0152
DAS2132	Dual SPST – 50 ohm	AH0152
DAS2133	Dual SPST – 50 ohm	AH0152
DAS2136	Dual SPST – 50 ohm	AH0152
DAS2137	Dual SPST – 50 ohm	AH0152
Fairchild		
A3F3700 (xxx)	4CH MOS Switch	MM450 Series
A313701 (xxx)	6CH MOS MUX	AM2009
A6J3705 (xxx)	8CH MOS MUX	AM3705 (pin for pin)
A6J3708 (xxx)	8CH MOS MUX	AM3705 (pin for pin)
HAG3001 (1xx)	4PST (obsolete)	AH0015
HAG3002 (xxx)	SPDT – 400 ohm	AH0014, AH0019
General Instrument		
MEM2009	6CH MOS MUX	AM2009 (pin for pin)
MEM2017	6CH MOS MUX	AM2009 (pin for pin)
MEM3705	8CH MUX with Decode	AM3705 (pin for pin)
NC450	Dual SPST – 500 ohm	AH0152
NC451	Dual SPST – 100 ohm	AH0134
NC2114	SPDT – 100 ohm	AH2114 (pin for pin)
NC2126	SPDT – 50 ohm	AH0162
NC2137	SPDT – 20 ohm	AH0146
Intersil		
IH5001	SPST – 30 ohm	1/2 AH0133
IH5002	SPST – 50 ohm	1/2 AH0152
IH5003	Dual SPST – 30 ohm	AH0133
IH5004	Dual SPST – 50 ohm	AH0152
IH5009 thru IH5024 Series	TTL Compatible – JFET Analog Current Switches	AH5009 thru AH5024 Series (pin for pin)
DG126 thru DG162 Series	TTL Compatible – JFET Analog Voltage Switches	AH0126 thru AH0164 Series (pin for pin – see note 1)
G114 thru G124 Series	Multiple P-MOS Transistors	MM450 thru MM454 Series and AM2009
Siliconix		
DG110	Dual SPST – 400 ohm	1/2 AH0015
DGM111	Dual SPST – 400 ohm	1/2 AH0015
DG112	Dual SPST – 400 ohm	1/2 AH0015
DG116	Obsolete – see DG172	1/2 AH0015
DG118	Obsolete – see DG172	AH0015
DG120	Obsolete – see DG502	AH0015
DG121	Obsolete – see DG502	2-AH0015
DGM122	Dual 2CH MUX – 400 ohm	AH0015
DGM123	Obsolete – see DG501	AM3705
DG125	Obsolete – see DG501	AM3705
DG126 thru DG164 Series	TTL Compatible – JFET Analog Voltage Switches	AH0126 thru AH0164 Series (pin for pin – see note 1)
DG169	Obsolete – see DG173	AH0014
DG171	SPST – 100 ohm	AM1000
DG172	4CH MUX – 400 ohm	AH0015
DG173	DPDT – 400 ohm	AH0014
DG175	SPDT – 200 ohm	1/2 AH0015
DG181	Dual SPST – 30 ohm	AH0133
DG182	Dual SPST – 80 ohm	AH0134
DG184	Dual DPST – 30 ohm	AH0129
DG185	Dual DPST – 80 ohm	AH0126
DG187	SPDT – 30 ohm	AH0144
DG188	SPDT – 80 ohm	AH0143
DG190	Dual SPST – 30 ohm	2-AH0144
DG191	Dual SPDT – 80 ohm	2-AH0143
DG400 Series	Dual SPDT – 80 ohm	See note 2
DG501	8CH MUX – 200 ohm	2-AH0015
DG502	Dual 4CH MUX – 200 ohm	2-AH0015
DG503	8CH MUX – 400 ohm	AM3705
DG506	8CH MUX – 400 ohm	AM3705
DG507	8CH MUX – 400 ohm	AM3705
DG510	8CH MUX – 400 ohm	AM3705
DG511	Dual 4CH MUX – 400 ohm	2-AH0015
G114 thru G124 Series	Multiple P-MOS Transistors	MM450 thru MM454 Series and AM2009
G125 thru G135 Series	Multiple J-FET Transistors	AH5009 thru AH5024 Series
SI3001	DPST – 500 ohm	1/2 AH0019
SI3002	SPDT – 500 ohm	1/2 AH0015
SI3705	8CH MUX – 400 ohm	AM3705 (pin for pin)
Teledyne – Crystalonics		
CAG6	SPST – 100 ohm	1/2 AH0134
CAG7	SPDT – 100 ohm	AH0143
CAG10	SPST – 500 ohm	AM1000
CAG13	Dual SPST – 500 ohm	AH0134, 1/2 AH0015
CAG14	SPST – 500 ohm	AM1000
CAG20	Dual SPST – 500 ohm	AH0134, 1/2 AH0015
CAG21	Dual DPST – 50 ohm	AH0154
CAG22	Dual DPST – 300 ohm	AH0154, AH0019
CAG23	Dual DPST – 500 ohm	AH0019
CAG24	Dual SPST – 300 ohm	AH0134, 1/2 AH0015
CAG27	Dual SPST – 100 ohm	AH0134
CAG30	SPST – 600 ohm	1/4 AH0015
CAG513	Dual SPST – 500 ohm	1/2 AH0015
CDA1	SPST – 100 ohm	1/2 AH0134
CDA2	Dual SPST – 300 ohm	1/2 AH0015
CDA4	SPST – 100 ohm	1/2 AH0134
CDA5	SPST – 200 ohm	1/2 AH0134
CDA6	SPST – 100 ohm	1/2 AH0134
CDA11	SPST – 100 ohm	1/2 AH0134
CDA18	SPST – 50 ohm	AM1000
Teledyne Semiconductor (Amelco)		
2107BE	SPST – 100 ohm	1/2 AH0126
2110BE	SPST – 500 ohm	1/2 AH0126
2114BF	SPDT – 100 ohm	AH2114 (pin for pin)
2126BG	SPDT – 500 ohm	AH0162
2127BG	SPDT – 500 ohm	AH0162
2127BG	DPST – 500 ohm	AH0152
2128BG	Quad SPST – 500 ohm	2-AH0152
2130BG	Dual SPST – 50 ohm	AH0152
2137BF	SPDT – 200 ohm	AH0146
2138BE	Dual SPST – 500 ohm	NS8035 (pin for pin)
2139BE	Dual SPST – 500 ohm	AH0152
2141BF/BH	Dual SPST – 500 ohm	AH0152
2145BE	Dual SPST – 50 ohm	AH0152
2147BE	Dual SPST – 500 ohm	AH0152
Texas Instrument		
TMS6000	10CH MOS MUX	AM3705
TMS6002	6CH MOS MUX	AM2009
TMS6005	6CH MOS MUX	AM2009
TMS6009	6CH MOS MUX	AM2009 (pin for pin)

Note 1: These devices have additional letter designations after part numbers National's corresponding pkg and temp range codes are

Intersil & Siliconix Designations		National Designations
Letter "A"	= Military temperature range	= No letter
Letter "B"	= Industrial temperature range	= Letter "C"
Letter "L"	= Flatpack	= Letter "F"
Letter "P"	= Dual-In-Line	= Letter "D"

Examples:

DG129AL = AH0129F (pin for pin)
DG134BP = AH0134CD (pin for pin)

Note 2: "400" series used to denote industrial temperature range product. Coding was changed to use "100" series and letter "B."

Example: DG426 DG126B AH0126C.

Analog Switch Cross Reference Guide

Description	National	Allen-Bradley	Beckman	Bourns	CTS	Centralab	Dale	Mepco	Sprague
7 Independent Resistors, 14 Pins	RA07-XXXN	34B-XXX4	899-3-RXXX	4114R-001-XXXS	760-3-XXX	MEC-2-XXX	CDP1401-XXXG	D14G02-XXXX	914CXXXX5SR
8 Independent Resistors, 16 Pins	RA08-XXXN	36D-XXX4	898-3-RXXX	4116R-001-XXXS	761-3-XXX	MEC-3-XXX	CDP1601-XXXG	D16H12-XXXX	916CXXXX5SR
12 Resistors, Pins 7 and 14 Common, 14 Pins	RA12-XXXN								914CXXXX5PD
13 Resistors, Pin 14 Common, 14 Pins	RA13-XXXN	34A-XXX4	899-1-RXXX	4114R-002-XXXS	760-1-XXX	MEC-1-XXX	CDP1402-XXXG	D14M01-XXXX	914CXXXX5PE
14 Resistors, Pins 8 and 16 Common, 16 Pins	RA14-XXXN								916CXXXX5PE
15 Resistors, Pin 16 Common, 16 Pins	RA15-XXXN	36C-XXX4	898-1-RXXX	4116R-002-XXXS	761-1-XXX		CDP1602-XXXG	D16011-XXXX	916CXXXX5PE
24 Resistors, Line Terminator	RA24-ABCN	34E-XXXX	899-5-RXXX	4114R-003-XXXX	760-5-RXXXX				914CTRXXXXSTR
28 Resistors, Line Terminators	RA28-ABCN	36E-XXXX	898-5-RXXX	4116R-003-XXXX	761-5-RXXXX				916CTRXXXXSTR

Note: XXX represents resistor values; all resistors are the same value within a package. Tolerance is ±2% or ±2Ω, whichever is larger. Custom arrays are available. For terminator arrays, ABC represents resistor ratio values. Tolerance is ±5%.

All of these resistance values are available in each array configuration except terminators (all values in ohms):

22	47	100	220	470	1k	2.2k	4.7k	9.1k	20k
24	51	110	240	510	1.1k	2.4k	5.1k	10k	22k
27	56	120	270	560	1.2k	2.7k	5.6k	11k	33k
30	62	130	300	620	1.3k	3k	6k	12k	47k
33	68	150	330	680	1.5k	3.3k	6.2k	13k	68k
36	75	160	360	750	1.6k	3.6k	6.8k	15k	100k
39	82	180	390	820	1.8k	3.9k	7.5k	16k	
43	91	200	430	910	2k	4.3k	8.2k	18k	

TERMINATOR ARRAY VALUES

Part Number	R1	R2
RA24 – 220/270N	220	270
RA24 – 220/330N	220	330
RA24 – 390/500N	390	500
RA24 – 3k/6.2kN	3k	6.2k
RA28 – 220/270N	220	270
RA28 – 220/330N	220	330
RA28 – 390/500N	390	500
RA28 – 3k/6.2kN	3k	6.2k

Resistance tolerance is ±5%. Values are listed in ohms.

DIP Resistor Array Cross Reference Guide

Application Note Guide

Many of the products included within this catalog are described in one or more of the following application notes. Copies are available through your local National Sales Office.

AN-13	LH0002 Current Amplifier	9/68
AN-18	MOS Clock Driver	3/69
AN-28	High-Speed MOS Commutators	2/70
AN-33	Analog-Signal Commutation	2/70
AN-34	How to Bias the Monolithic JFET Dual	3/70
AN-38	MOS Analog Switches	4/70
AN-48	Applications for a New Ultra-High Speed Buffer	8/71
AN-49	Pin Diode Drivers	8/71
AN-53	High Speed Analog Switches	9/71
AN-63	New Design Techniques for FET Operational Amplifiers	3/72
AN-75	Applications for a High Speed FET Operational Amplifier	12/72
AN-76	Applying Modern Clock Drivers to MOS Memories	2/73
AN-155	Digital Voltmeters and the MM5330	11/75
MB-5	MOS Clock Savers	1971
MB-9	MOS Clock Drivers	1971

NATIONAL

Amplifiers

LH0001* low power operational amplifier

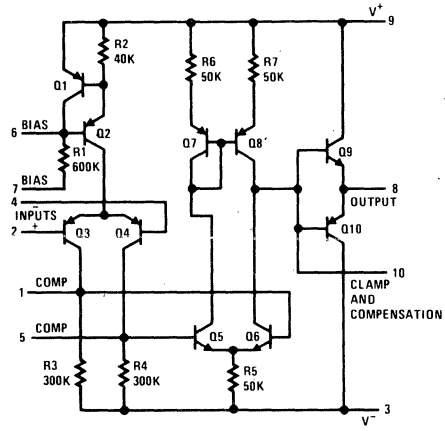
general description

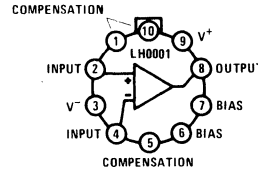
The LH0001 is a general purpose operational amplifier designed for extremely low quiescent power. Typical NO-load dissipation at 25°C is 2 milliwatts at V_S = ±15 volts, and 0.5 milliwatts at V_S = ±5 volts. Even with this low power dissipation, the LH0001 will deliver ±10 volts into a 2K load with ±15 volt supplies, and typical short circuit currents of 20 to 30 milliamps. Additional features are:

- Operation from ±5V to ±20V
- Very low offset voltage: typically 200 μV at 25°C, 600 μV at −55°C to 125°C
- Very low input offset current: typically 3 nA at 25°C, 6 nA at −55°C
- Low noise: typically 3 μV rms
- Frequency compensation with 2 small capacitors
- Output may be clamped at any desired level
- Output is continuously short circuit proof

The LH0001 is ideally suited for space borne applications or where battery operated equipment requires extremely low power dissipation.

schematic and connection diagrams





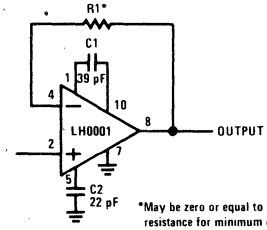
TOP VIEW

Note: Pin 7 must be grounded or connected to a voltage at least 5 volts more negative than the positive supply (Pin 9). Pin 7 may be connected to the negative supply however the standby current will be increased. A resistor may be inserted in series with Pin 7 up to a maximum of 100 kΩ per volt for the voltage difference between Pin 3 and Pin 9.

Order Number LH0001H
See Package 11

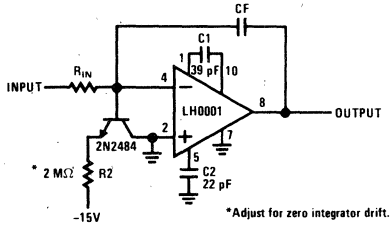
typical applications

Voltage Follower



*May be zero or equal to source resistance for minimum offset.

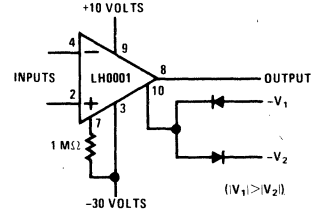
Integrator with Bias Current Compensation



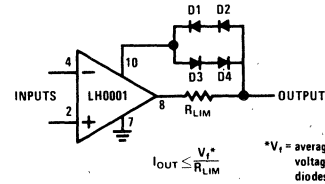
*Adjust for zero integrator drift.

*Previously called NH0001

Voltage Comparator for Driving MOS Circuits



External Current Limiting Method



*Vf = average forward voltage drop of diodes D1 to D4 at 20 to 50 μA.

absolute maximum ratings

Supply Voltage	±20V
Power Dissipation (see Curve)	400 mW
Differential Input Voltage	±7V
Input Voltage	Equal to supply
Short Circuit Duration (Note 1)	Continuous
Operating Temperature Range	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering 10 sec.)	300°C

electrical characteristics (Note 2)

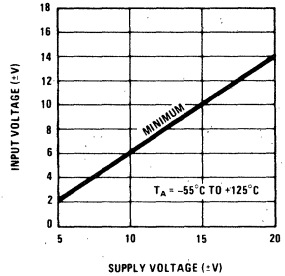
PARAMETER	TEMP (°C)	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	25	$R_S \leq 5K$		0.2	1.0	mV
	−55 to 125	$R_S \leq 5K$		0.6	2.0	mV
Input Offset Current	25 to 125				20	nA
	−55				100	nA
Input Bias Current	25 to 125				100	nA
	−55				300	nA
Supply Current (+)	25	$V_S = \pm 20V$		90	125	μA
	125	$V_S = \pm 20V$		70	100	μA
	−55	$V_S = \pm 20V$		100	150	μA
Supply Current (−)	25	$V_S = \pm 20V$		60	90	μA
	125	$V_S = \pm 20V$		45	75	μA
	−55	$V_S = \pm 20V$		75	125	μA
Voltage Gain	−55 to 25	$R_L = 100\ K\Omega$, $V_S = \pm 15V$, $V_{OUT} = \pm 10V$	25	60		V/mV
	125	$R_L = 100\ K\Omega$, $V_S = \pm 15V$, $V_{OUT} = \pm 10V$	10	30		V/mV
V_{OUT}	25	$V_S = \pm 15V$, $R_L = 2K$	10	11.5		V
	−55	$V_S = \pm 15V$, $R_L = 2K$	9	10.5		V
	125	$V_S = \pm 15V$, $R_L = 2K$	11	12.5		V
Common Mode Rejection Ratio	−55 to 125	$V_S = \pm 15V$, $V_{IN} = \pm 10V$, $R_S \leq 5K$	70	90		dB
Power Supply Rejection Ratio	−55 to 125	$V_S = \pm 15V$, $\Delta V = 5V$ to 20V, $R_S = \leq 5K$	70	90		dB
Input Resistance	25		0.5	1.5		MΩ
Average Temperature Coefficient of Offset Voltage	−55 to 125	$R_S \leq 5K$		4		μV/°C
Average Temperature Coefficient of Bias Current	−55 to 125			0.4		μA/°C
Equivalent Input Noise Voltage	25	$R_S = 1K$, f = 5 Hz to 1000 Hz, $V_S = \pm 15V$		3.0		μV rms

Note 1: Based on maximum short circuit current of 50 mA, device may be operated at any combination of supply voltages, and temperature to be within rated power dissipation (see Curve).

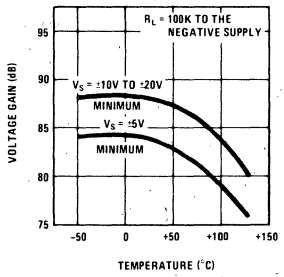
Note 2: These specifications apply for Pin 7 grounded, for $\pm 5V \leq V_S \leq \pm 20V$, with Capacitor C1 = 39 pF from Pin 1 to Pin 10, and C2 = 22 pF from Pin 5 to ground, unless otherwise specified.

guaranteed performance

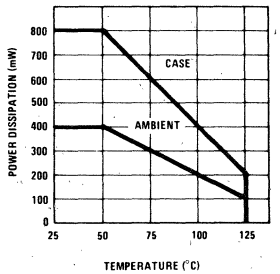
Input Voltage Range



Small Signal Voltage Gain

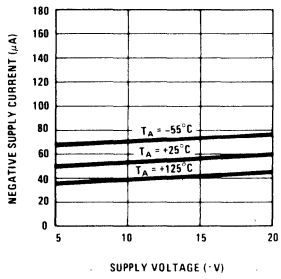


Maximum Power Dissipation

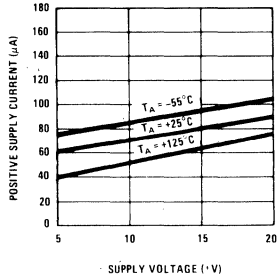


typical performance characteristics

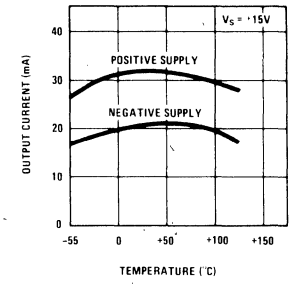
Negative Supply Current



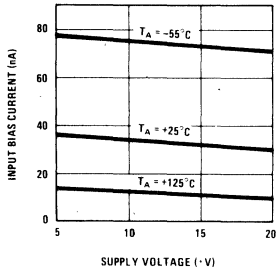
Positive Supply Currents



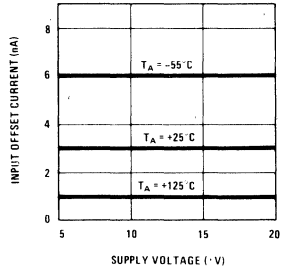
Short Circuit Output Current



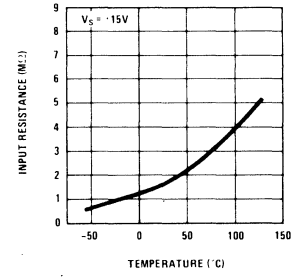
Input Bias Current



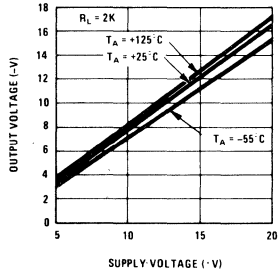
Input Offset Current



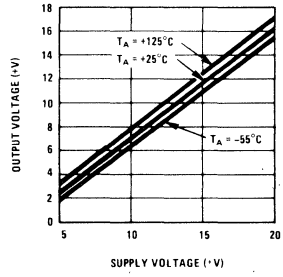
Input Resistance



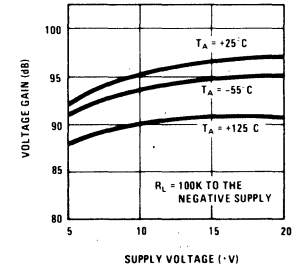
Negative Output Voltage Swing



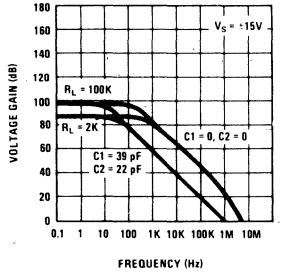
Positive Output Voltage Swing



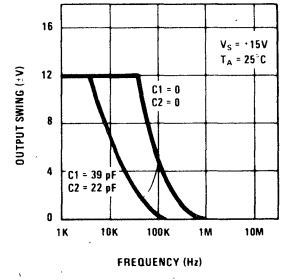
Voltage Gain



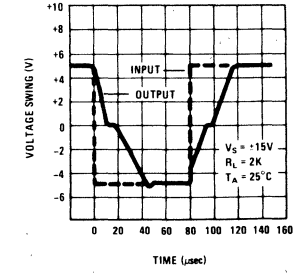
Open Loop Frequency Response



Large Signal Frequency Response



Voltage Follower Pulse Response



NATIONAL

LH0001A/LH0001AC micropower operational amplifier

general description

The LH0001A/LH0001AC is a micropower, high performance integrated circuit operational amplifier designed to have a no load power dissipation of less than 0.5 mW at $V_S = \pm 5V$ and less than 2 mW at $V_S = \pm 20V$. Open loop gain is greater than 50k and input bias current is typically 20 nA.

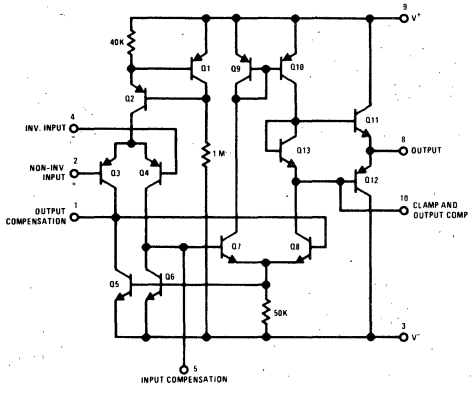
features

- 1.0 mV Typical low offset voltage
- 5 nA Typical low offset current
- 3 μVrms Typical low noise
- Simple frequency compensation
- Moderate bandwidth and slewrate
- Output short circuit proof

The LH0001A/LH0001AC may be substituted directly for the LH0001/LH0001C. Low power consumption, high open loop gain, and excellent input characteristics make the LH0001A an ideal amplifier for many low power applications such as battery powered instrument or transducer amplifiers.

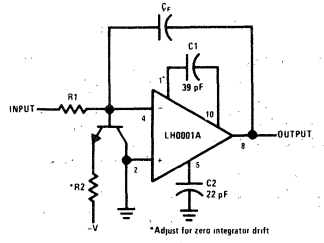
The LH0001A is specified for operation over the $-55^\circ C$ to $+125^\circ C$ military temperature range. The LH0001AC is specified for operation over the $0^\circ C$ to $+85^\circ C$ temperature range.

schematic diagram*



*Pin shown for TO-5 package

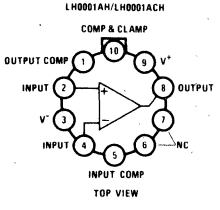
typical application*



Integrator with Bias Compensation

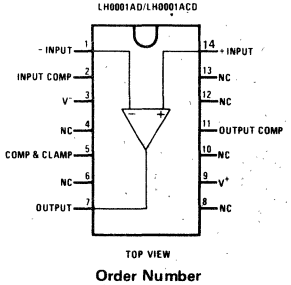
connection diagrams

Metal Can Package



Order Number
LH0001AH or LH0001ACH
See Package 11

Cavity Dual-In-Line Package



Order Number
LH0001AD or LH0001ACD
See Package 1

absolute maximum ratings

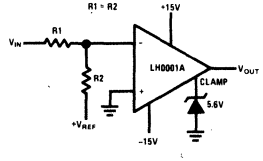
Supply Voltage		±20V
Power Dissipation (See curve)		400 mW
Differential Input Voltage		±7V
Input Voltage		$\pm V_S$
Short Circuit Duration		Continuous
Operating Temperature Range	LH0001A	-55°C to 125°C
	LH0001AC	-25°C to 85°C
Storage Temperature Range		-65°C to 150°C
Lead Temperature (Soldering, 10 sec)		300°C

electrical characteristics (Note 1)

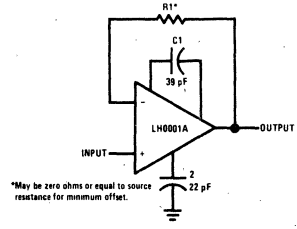
PARAMETERS	CONDITIONS	LH0001A			LH0001AC			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$R_S \leq 1k$, $T_A = 25°C$		1.0	2.5 4.0		2.0	5.0 7.0	mV mV
Input Bias Current	$T_A = 25°C$		20	100 300		20	200 300	nA nA
Input Offset Current	$T_A = 25°C$		5	20 100		20	60 100	nA nA
Supply Current	$V_S = \pm 20V$, $T_A = 25°C$ $V_S = \pm 20V$		80	125 150		80	125 150	μA μA
Voltage Gain	$V_S = \pm 15V$, $V_{OUT} = 10V$, $R_L = 100k$, $T_A = 25°C$ $V_S = \pm 15V$, $V_{OUT} = 10V$, $R_L = 100k$	25 25 10	60 60 30		25 25 10	60 60		V/mV V/mV
Output Voltage	$V_S = \pm 15V$, $R_L = 2k$, $T_A = 25°C$ $V_S = \pm 15V$, $R_L = 2k$	10 9	11.5		10 9	11.5		V V
Common Mode Rejection Ratio	$V_S = \pm 15V$, $V_{IN} = 10V$, $R_S = 1k$	70	90		70	90		db
Power Supply Rejection Ratio	$V_S = \pm 15V$, $R_S = 1k$, $V_S = \pm 5V$ to $\pm 20V$	70	90		70	90		db
Equivalent Input Noise Voltage	$V_S = \pm 15V$, $R_S = 1k$, $T_A = 25°C$ f = 500 Hz to 5 kHz		3.0			3.0		μVrms
Average Temperature Coefficient of Offset Voltage	$R_S \leq 1k$		3.0			3.0		μV/°C
Average Temperature Coefficient of Bias Current			0.3			0.3		nA/°C

Note 1: The specifications apply for $\pm 5V \leq V_S \leq 20V$, with output compensation capacitor, C_1 = 39 pF, input compensation capacitor, C_2 = 22 pF, -55°C to 125°C for the LH0001A and -25°C to +85°C for the LH0001AC unless otherwise specified.

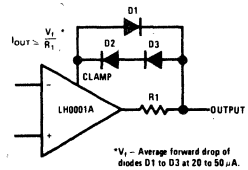
typical applications



TTL/DTL Compatible Comparator



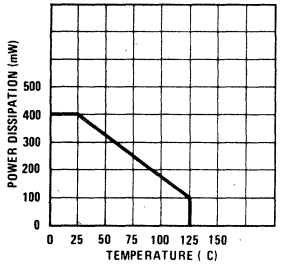
Voltage Follower



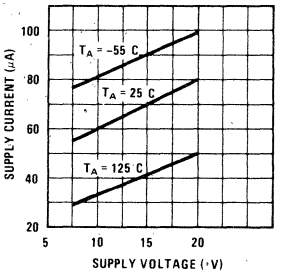
External Output Current Limiting

typical performance characteristics

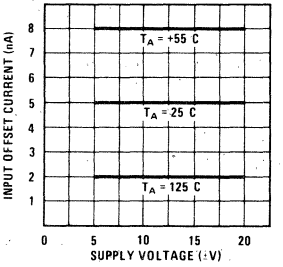
Maximum Power Dissipation



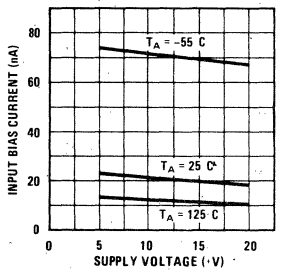
Supply Current



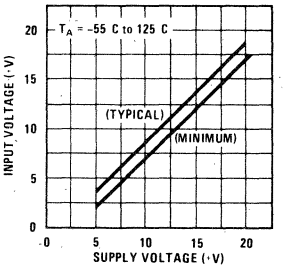
Input Offset Current



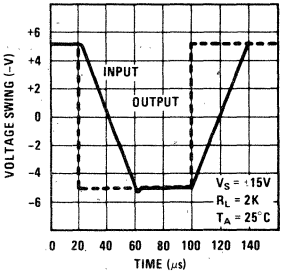
Input Bias Current



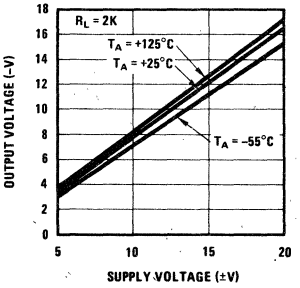
Input Voltage Range



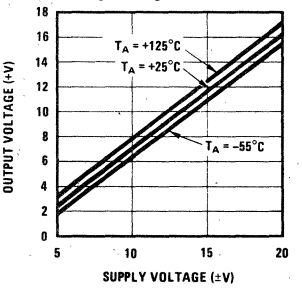
Voltage Follower Pulse Response



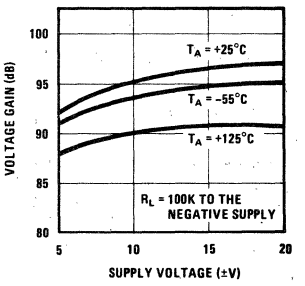
Negative Output Voltage Swing



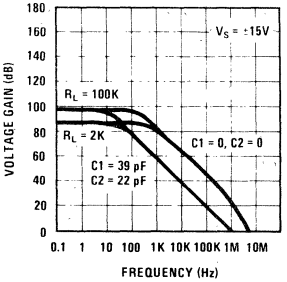
Positive Output Voltage Swing



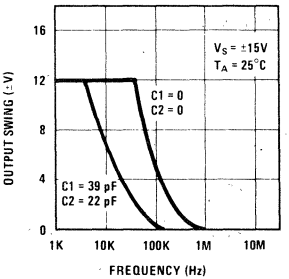
Voltage Gain



Open Loop Frequency Response



Large Signal Frequency Response



LH0003/LH0003C* wide bandwidth operational amplifier

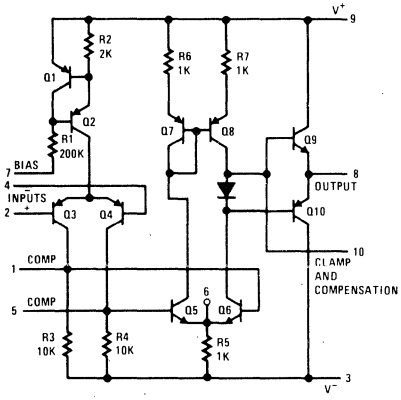
general description

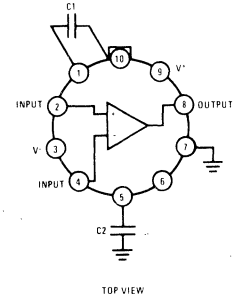
The LH0003/LH0003C is a general purpose operational amplifier which features: slewing rate up to 70 volts/μsec, a gain bandwidth of up to 30 MHz, and high output currents. Other features are:

- Very low offset voltage — Typically 0.4 mV
- Large output swing — $>\pm10$V into 100Ω load
- High CMRR — Typically >90 dB
- Good large signal frequency response — 50 kHz to 400 kHz depending on compensation

The LH0003 is specified for operation over the −55°C to +125°C military temperature range. The LH0003C is specified for operation over the 0°C to +85°C temperature range.

schematic and connection diagrams





TOP VIEW

Order Number LH0003H or LH0003CH
See Package 11

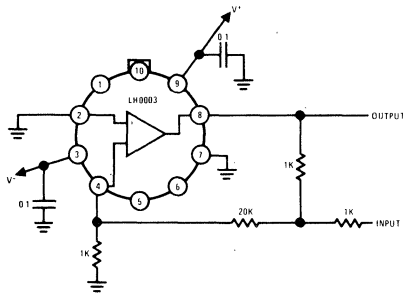
Circuit Gain	C_1 pF	C_2 pF	Slew Rate $R_L \geq 200\Omega$, V/μsec	Full Output Frequency $R_L \geq 200\Omega$, $V_{OUT} = 10$ V
≥ 40	0	0	70	400
≥ 10	5	30	30	350
≥ 5	15	30	15	250
≥ 2	50	50	5	100
≥ 1	90	90	2	50

kHz

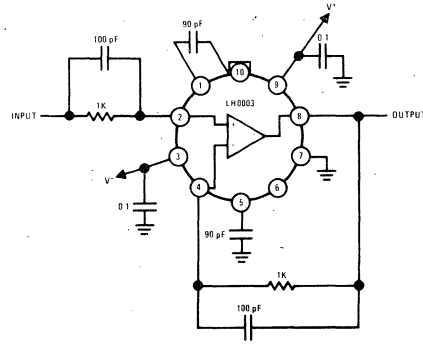
Typical Compensation

typical applications

High Slew Rate Unity Gain Inverting Amplifier



Unity Gain Follower



*Previously called NH0003/NH0003C

absolute maximum ratings

Supply Voltage		±20V
Power Dissipation		See curve
Differential Input Voltage		±7V
Input Voltage		Equal to supply
Load Current		120 mA
Operating Temperature Range	LH0003	−55°C to +125°C
	LH0003C	0°C to +85°C
Storage Temperature Range		−65°C to +150°C
Lead Temperature (Soldering, 10 sec)		300°C

electrical characteristics (Notes 1 & 2)

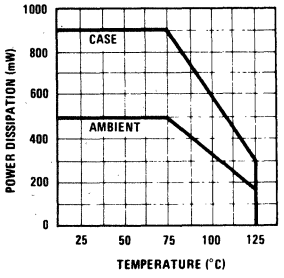
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	$R_S < 1k$		0.4	3.0	mV
Input Offset Current			0.02	0.2	μA
Input Bias Current			0.4	2.0	μA
Supply Current	V_S = ±20V		1.2	3	mA
Voltage Gain	R_L = 100k, V_S = ±15V, V_{OUT} = ±10V	20	70		V/mV
Voltage Gain	R_L = 2k, V_S = ±15V, V_{OUT} = ±10V	15	40		V/mV
Output Voltage Swing	V_S = ±15, R_L = 100Ω	±10	±12		V
Input Resistance			100		kΩ
Average Temperature Coefficient of Offset Voltage	$R_S < 5k$		4		μV/°C
Average Temperature Coefficient of Bias Current			8		nA/°C
CMRR	$R_S < 1k$, V_S = ±V, V_{IN} = ±10V	70	90		dB
PSRR	$R_S < 1k$, V_S = ±15V, ΔV = 5V to 20V	70	90		dB
Equivalent Input Noise Voltage	R_S = 1K, f = 10 kHz to 100 kHz, V_S = ±15V dc		1.8		μVrms

Note 1. These specifications apply for Pin 7 grounded, for $\pm 5V < V_S < \pm 20V$, with capacitor $C_1 = 90$ pF from Pin 1 to Pin 10 and $C_2 = 90$ pF from Pin 5 to ground, over the specified operating temperature range, unless otherwise specified.

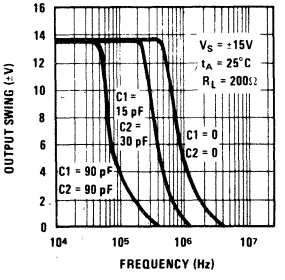
Note 2. Typical values are for $t_{AMBIENT} = 25°C$ unless otherwise specified.

typical performance

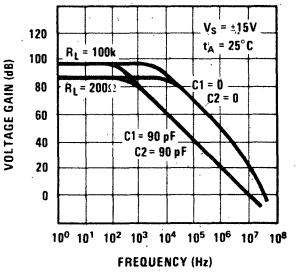
Maximum Power Dissipation



Large Signal Frequency Response



Open Loop Frequency Response



Amplifiers

LH0004/LH0004C* high voltage operational amplifier

general description

The LH0004/LH0004C is a general purpose operational amplifier designed to operate from supply voltages up to ±40V. The device dissipates extremely low quiescent power, typically 8 mW at 25°C and V_S = ±40V. Additional features include:

- Capable of operation over the range of ±5V to ±40V.
- Large output voltage typically ±35V for the LH0004 and ±33V for the LH0004C into a 5KΩ load with ±40V supplies
- Low input offset current typically 20 nA for the LH0004 and 45 nA for the LH0004C
- Low input offset voltage typically 0.3 mV
- Frequency compensation with two small capacitors.
- Low power consumption 8 mW at ±40V

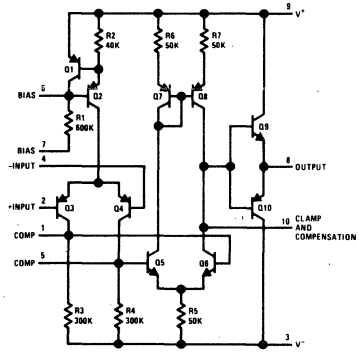
The LH0004's high gain and wide range of operating voltages make it ideal for applications requiring large output swing and low power dissipation.

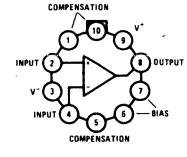
The LH0004 is specified for operation over the −55°C to +125°C military temperature range. The LH0004C is specified for operation over the 0°C to +85°C temperature range.

applications

- Precision high voltage power supply.
- Resolver excitation.
- Wideband high voltage amplifier.
- Transducer power supply.

schematic and connection diagrams





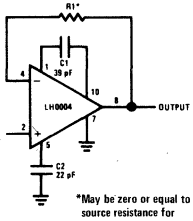
TOP VIEW

Note: Pin 7 must be grounded or connected to a voltage at least 5 volts more negative than the positive supply (Pin 9). Pin 7 may be connected to the negative supply, however, the standby current will be increased. A resistor may be inserted in series with Pin 7 to Pin 9. The value of the resistor should be a maximum of 100 KΩ per volt of potential between Pin 3 and Pin 9.

Order Number LH0004H or LH0004CH
See Package 11

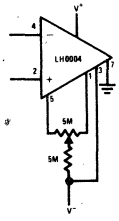
typical applications

Voltage Follower

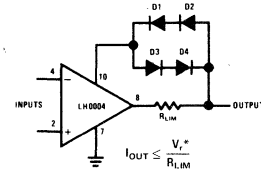


*May be zero or equal to source resistance for minimum offset.

Input Offset Voltage Adjust



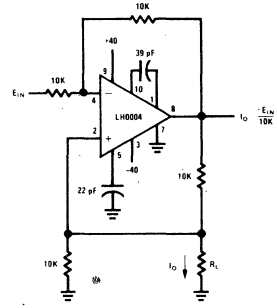
External Current Limiting Method



$$I_{OUT} \leq \frac{V_f^*}{R_{LIM}}$$

*V_f = average forward voltage drop of diodes D1 to D4 at 20 to 50 μA.

High Compliance Current Source



*Previously called NH0004/NH0004C

absolute maximum ratings

Supply Voltage, Continuous	±45V
Supply Voltage, Transient (≤0.1 sec, no load)	±60V
Power Dissipation (See curve)	400 mW
Differential Input Voltage	±7V
Input Voltage	Equal to supply
Short Circuit Duration	3 sec
Operating Temperature Range LH0004	−55°C to +125°C
LH0004C	0°C to 85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

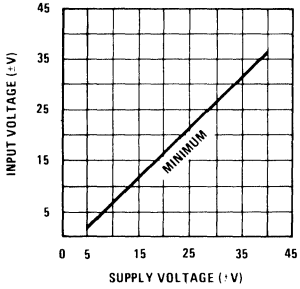
electrical characteristics (Note 1)

PARAMETER	CONDITIONS	LH0004			LH0004C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$R_S = 100\Omega$, $T_A = 25°C$, $V_S = \pm 40V$		0.3	1.0		0.3	1.5	mV
	$R_S = 100\Omega$, $V_S = \pm 40V$			2.0			3.0	mV
Input Bias Current	$T_A = 25°C$		20	100		30	120	nA
	$T_A = -55°C$			300			300	nA
Input Offset Current	$T_A = 25°C$		3	20		10	45	nA
	$T_A = -55°C$			100			150	nA
Positive Supply Current	$V_S = \pm 40V$, $T_A = 25°C$		110	150		110	150	μA
	$V_S = \pm 40V$			175			175	μA
Negative Supply Current	$V_S = \pm 40V$, $T_A = 25°C$		80	100		80	100	μA
	$V_S = \pm 40V$			135			135	μA
Voltage Gain	$V_S = \pm 40V$, $R_L = 100k\Omega$, $T_A = 25°C$, $V_{OUT} = \pm 30V$	30	60		30	60		V/mV
	$V_S = \pm 40V$, $R_L = 100k\Omega$, $V_{OUT} = \pm 30V$	10			10			V/mV
Output Voltage	$V_S = \pm 40V$, $R_L = 5k\Omega$	±30	±35		±30	±33		V
CMRR	$V_S = \pm 40V$, $R_S = 100\Omega$, $V_{IN} = \pm 33V$	70	90		70	90		dB
PSRR	$V_S = \pm 40V$, $R_S = 100\Omega$, $\Delta V = 20V$ to $40V$	70	90		70	90		dB
Average Temperature Coefficient Offset Voltage	$R_S \leq 5k\Omega$		4.0			4.0		μV/°C
Average Temperature Coefficient of Offset Current			0.4			0.4		μA/°C
Equivalent Input Noise Voltage	$R_S = 1k\Omega$, $V_S = \pm 40V$, f = 500Hz to 5kHz, $T_A = 25°C$		3.0			3.0		μVrms

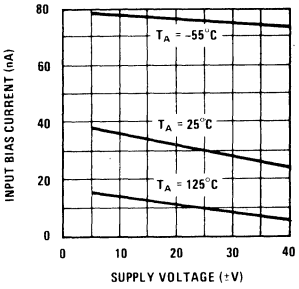
Note 1: These specifications apply for $\pm 5V \leq V_S \leq \pm 40V$, Pin 7 grounded, with capacitors C1 = 39 pF between Pin 1 and Pin 10, C2 = 22 pF between Pin 5 and ground, −55°C to 125°C for the LH0004, and 0°C to 85°C for the LH0004C unless otherwise specified.

typical performance

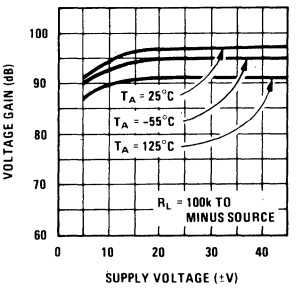
Input Voltage Range



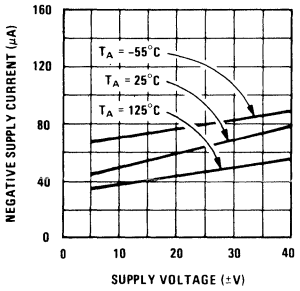
Input Bias Current



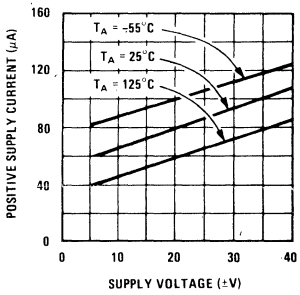
Voltage Gain



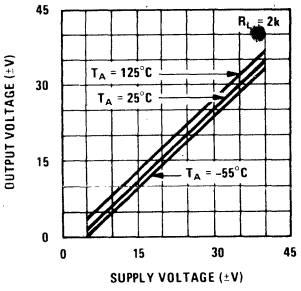
Negative Supply Current



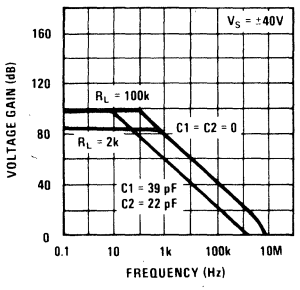
Positive Supply Current



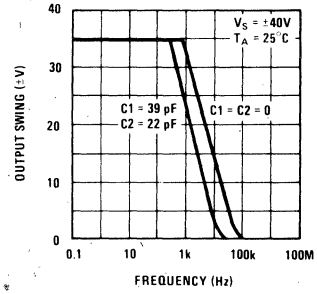
Output Voltage



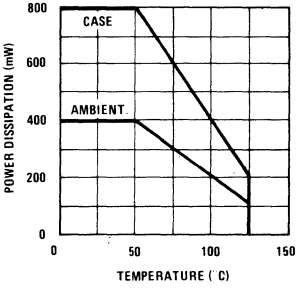
Open Loop Frequency Response



Large Signal Frequency Response



Package Power Dissipation



NATIONAL

Amplifiers

LH0005/LH0005A* operational amplifier

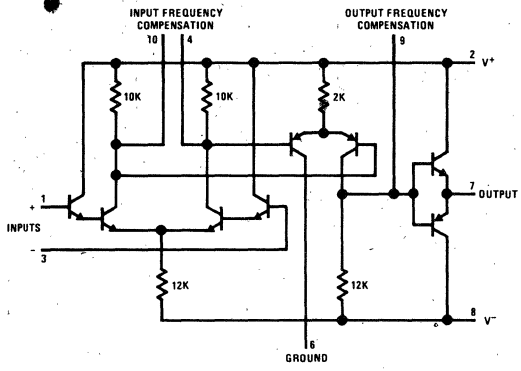
general description

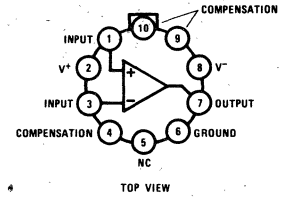
The LH0005/LH0005A is a hybrid integrated circuit operational amplifier employing thick film resistors and discrete silicon semiconductors in its design. The select matching of the input pairs of transistors results in low input bias currents and a very low input offset current, both of which exhibit excellent temperature tracking. In addition, the device features:

- Very high output current capability: ±50 mA into a 100 ohm load
- Low standby power dissipation: typically 60 mW at ±12V
- High input resistance: typically 2M at 25°C
- Full operating range: −55°C to +125°C
- Good high frequency response: unity gain at 30 MHz

With no external roll-off network, the amplifier is stable with a feedback ratio of 10 or greater. By adding a 200 pF capacitor between pins 9 and 10, and a 200 ohm resistor in series with a 75 pF capacitor from pin 4 to ground, the amplifier is stable to unity gain. The unity gain loop phase margin with the above compensation is typically 70 degrees. With a gain of 10 and no compensation the loop phase margin is typically 50 degrees.

schematic and connection diagrams



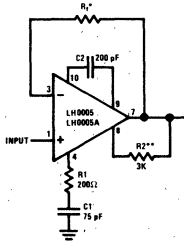


TOP VIEW

Order Number LH0005H or LH0005AH
See Package 11

typical applications

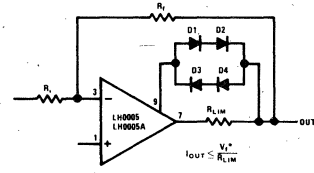
Voltage Follower



*May be zero or equal to the input resistance for minimum offset.

**To minimize crossover distortion at higher frequencies. May be omitted for low frequency application or selected to suit design requirements

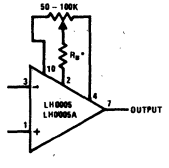
External Current Limiting



*V_I = Average forward voltage drop of diodes D_1 to D_4 at approx. 1 mA.

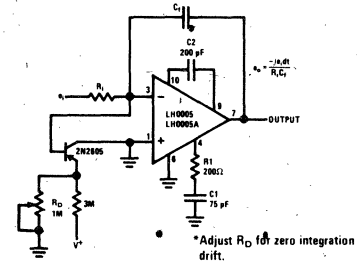
For continuous short circuit protection (V_S = ±12V, −55°C < T_A < +100°C) $R_{LIM} \geq 50\Omega$

Offset Balancing Circuit



*Typical value, R_B = 100K. R_B may be increased for greater sensitivity with reduction in range.

Integrator with Bias Current Compensation



*Adjust R_D for zero integration drift.

*Previously called NH0005/NH0005A

absolute maximum ratings

Supply Voltage	±20V
Power Dissipation (see Curve)	400 mW
Differential Input Voltage	±15V
Input Voltage	Equal to supply voltages
Peak Load Current	±100 mA
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−55°C to +125°C
Lead Temperature (Soldering, 10 sec)	300°C

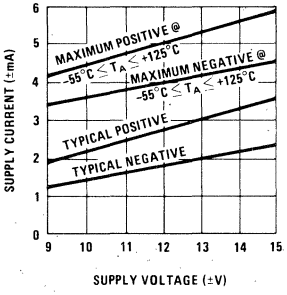
electrical characteristics (Note 1)

PARAMETER	CONDITIONS	LH0005			LH0005A			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage								
25°C	$R_S \leq 20\ k\Omega$		5	10		1	3	mV
−55°C, 125°C	$R_S \leq 20\ k\Omega$			10			4	mV
Input Offset Current								
25°C to 125°C			10	20		2	5	nA
−55°C			25	75		10	25	nA
Input Bias Current								
25°C to 125°C			15	50		8	25	nA
−55°C			100	250		60	125	nA
Large Signal Voltage Gain								
−55°C to 25°C	R_L = 10K, R2 = 3K, V_{OUT} = ±5V	2	4		4	5.5		V/mV
125°C		1.5	3		3	5		V/mV
Output Voltage Swing								
−55°C to 125°C	R_L = 10 kΩ	−10		+6	−10		+6	V
25°C to 125°C	R_L = 100Ω	−5		+5	−5		+5	V
−55°C	R_L = 100Ω	−4		+4	−4		+4	V
Input Resistance								
25°C		1	2		1	2		MΩ
Common Mode Rejection Ratio								
25°C	V_{IN} = ±4V, RS ≤ 20 kΩ	55	60		60	66		dB
Power Supply Rejection Ratio								
25°C		55	60		60	66		dB
Supply Current (+)								
−55°C to 125°C			3	5		3	5	mA
Supply Current (−)								
−55°C to 125°C			2	4		2	4	mA
Average Temperature Coefficient of Input Offset Voltage								
−55°C to 125°C	$R_S \leq 20\ k\Omega$		20			10		uV/°C
Output Resistance								
25°C			70			70		Ω

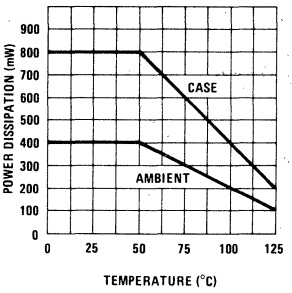
Note 1: These specifications apply for pin 6 grounded, V_S = ±12V, with Resistor R_1 = 200Ω in series with Capacitor C_1 = 75 pF from pin 4 to ground, and C_2 = 200 pF between pins 9 and 10 unless otherwise specified.

guaranteed performance characteristics

Supply Current

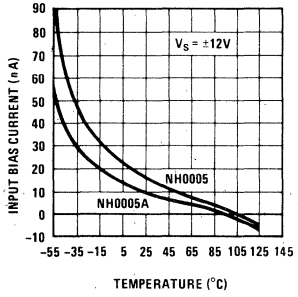


Maximum Power Dissipation

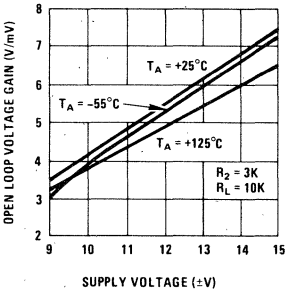


typical performance characteristics

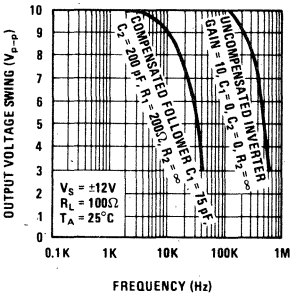
Input Bias Current



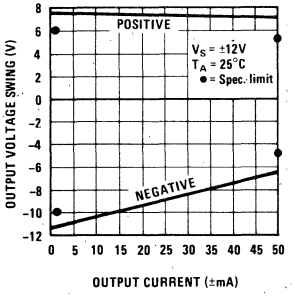
Voltage Gain



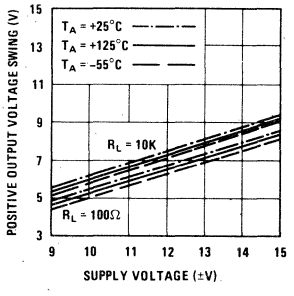
Loaded Output Voltage Swing



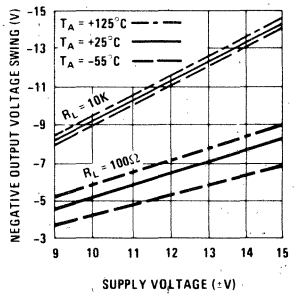
DC Output Voltage Swing



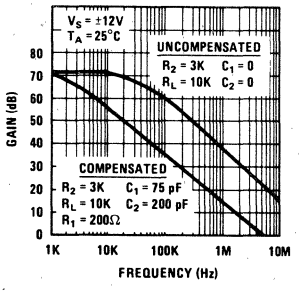
Positive Output Voltage Swing



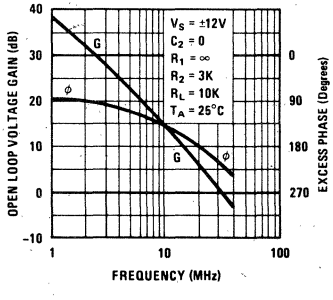
Negative Output Voltage Swing



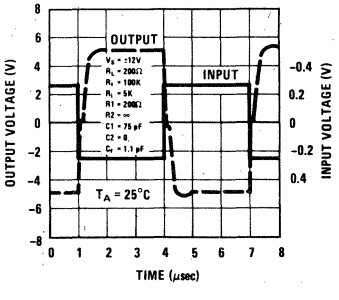
Frequency Response



Open Loop Gain vs Excess Phase



Inverting Pulse Response



Amplifiers

LH0005C* operational amplifier

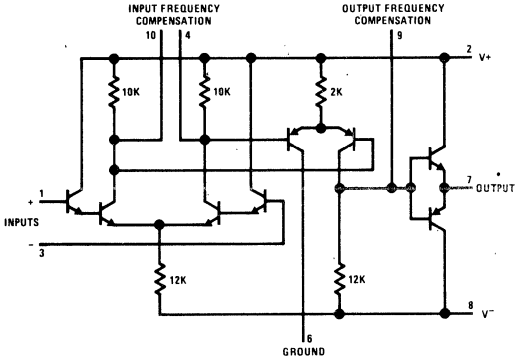
general description

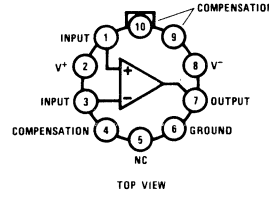
The LH0005C is a hybrid integrated circuit operational amplifier employing thick film resistors and discrete silicon semiconductors in its design. The select matching of the input pairs of transistors results in low input bias currents and a very low input offset current both of which exhibit excellent temperature tracking. In addition, the device features:

- Very high output current capability: ±40 mA into a 100 ohm load
- Low standby power dissipation: typically 60 mW at ±12V
- High input resistance: typically 2M at 25°C
- Operating range: 0° to 70°C
- Good high frequency response: unity gain at 30 MHz

With no external roll-off network, the amplifier is stable with a feedback ratio of 10 or greater. By adding a 200 pF capacitor between pins 9 and 10, and a 200 ohm resistor in series with a 75 pF capacitor from pin 4 to ground, the amplifier is stable to unity gain. The unity gain loop phase margin with the above compensation is typically 70 degrees. With a gain of 10 and no compensation the loop phase margin is typically 50 degrees.

schematic and connection diagrams



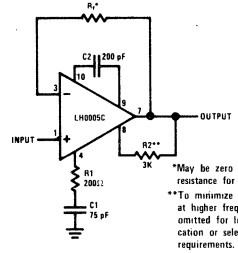


TOP VIEW

Order Number LH0005CH
See Package 11

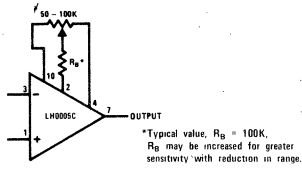
typical applications

Voltage Follower



*May be zero or equal to the input resistance for minimum offset.
**To minimize crossover distortion at higher frequencies. May be omitted for low frequency application or selected to suit design requirements.

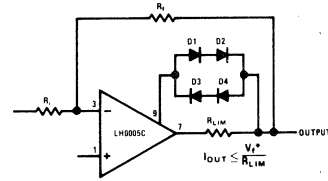
Offset Balancing Circuit



*Typical value, R_B = 100K. R_B may be increased for greater sensitivity with reduction in range.

*Previously called NH0005C

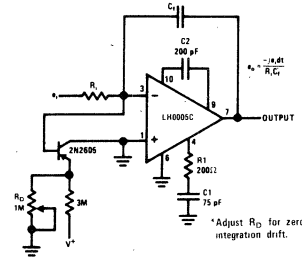
External Current Limiting



For continuous short circuit protection (V_S = ±12V, 0°C ≤ T_A ≤ 70°C, $R_{LIM} \geq 50\Omega$

*V_f = Average forward voltage drop of diodes D_1 to D_4 at approx. 1 mA

Integrator With Bias Current Compensation



*Adjust R_D for zero integration drift.

absolute maximum ratings

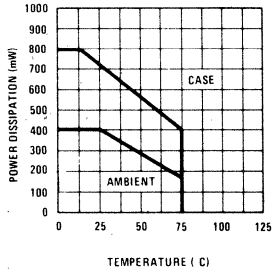
Supply Voltage	±20V
Power Dissipation (see Curve)	400 mW
Differential Input Voltage	±15V
Input Voltage	Equal to supply voltages
Peak Load Current	±100 mA
Storage Temperature Range	−55°C to +125°C
Operating Temperature Range	0°C to 85°C
Lead Temperature (soldering, 10 sec)	300°C

electrical characteristics

PARAMETER	CONDITIONS	LH0005C MIN	LH0005C TYP (Note 2)	LH0005C MAX	UNITS
Input Offset Voltage	$R_S \leq 20\ k\Omega$		3	10	mV
Input Offset Current			5	25	nA
Input Bias Current			20	100	nA
Large Signal Voltage Gain	R_L = 10K, R2 = 3K, V_{OUT} = ±5V	2	5		V/mV
Output Voltage Swing	R_L = 10 kΩ	−10		+6	V
	R_L = 100Ω	−4	±6	+4	V
Input Resistance	T_A = 25°C	0.5	2		MΩ
Common Mode Rejection Ratio	V_{IN} = ±4V, $R_S \leq 20\ k\Omega$, T_A = 25°C	50	60		dB
Power Supply Rejection Ratio	T_A = 25°C	50	60		dB
Supply Current (+)			3	5	mA
Supply Current (−)			2	4	mA

Note 1: These specifications apply for pin 6 grounded, V_S = ±12V, with Resistor R1 = 200Ω in series with Capacitor C1 = 75 pF from pin 4 to ground, and C2 = 200 pF between pins 9 and 10, over the temperature range of 0°C to +85°C unless otherwise specified.

Note 2: Typical values are for 25°C only.



Maximum Power Dissipation

LH0020/LH0020C* high gain instrumentation operational amplifier

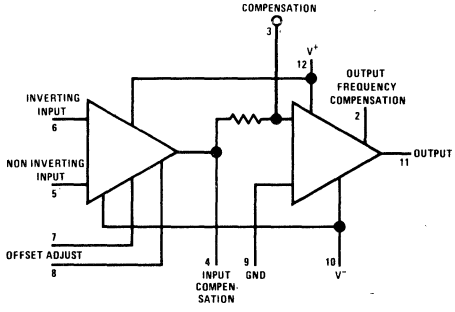
general description

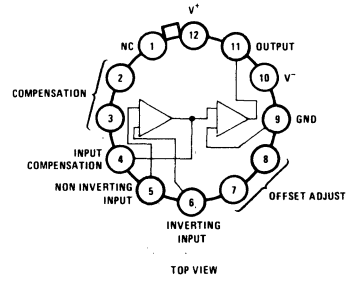
The LH0020/LH0020C is a general purpose operational amplifier designed to source and sink 50 mA output currents. In addition to its high output capability, the LH0020/LH0020C exhibits excellent open loop gain, typically in excess of 100 dB. The parameters of the LH0020 are guaranteed over the temperature range of −55°C to +125°C and $\pm 5V \leqslant V_S \leqslant \pm 22V$, while those of the LH0020C are guaranteed over the temperature range of 0°C to 85°C and $\leq \pm 5V \leq V_S \leq \pm 18V$. Additional features include:

- Low offset voltage typically 1.0 mV at 25°C over the entire common mode voltage range.
- Low offset current typically 10 nA at 25°C for the LH0020 and 30 nA for the LH0020C.
- Offset voltage is adjustable to zero with a single potentiometer.
- ±14V, 50 mA output capability.

Output current capability, excellent input characteristics, and large open loop gain make the LH0020/LH0020C suitable for application in a wide variety of applications from precision dc power supplies to precision medium power comparator.

schematic and connection diagrams

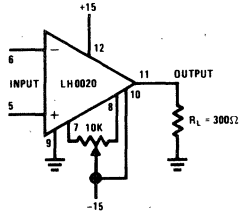




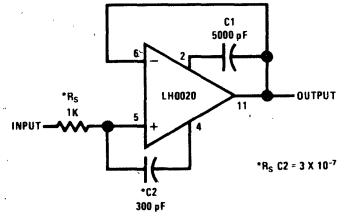
Order Number LH0020G or LH0020CG
See Package 6

typical applications

Offset Adjustment



Unity Gain Frequency Compensation



*Previously called NH0020/NH0020C

absolute maximum ratings

Supply Voltage		±22V
Power Dissipation		1.5W
Differential Input Voltage		±30V
Input Voltage (Note 1)		±15V
Output Short Circuit Duration		Continuous
Operating Temperature Range	LH0020	−55°C to +125°C
	LH0020C	0°C to 85°C
Storage Temperature		−65°C to +150°C
Lead Temperature (Soldering, 10 sec)		300°C

electrical characteristics

PARAMETER	CONDITIONS	LH0020				LH0020C				UNITS
		TEMP °C	MIN	TYP	MAX	TEMP °C	MIN	TYP	MAX	
Input Offset Voltage	$R_S \leq 10k$	25		1.0	2.5	25		1.0	6.0	mV
		−55 to +125		2.0	4.0	0 to 85		3.0	7.5	mV
Input Offset Current		25		10	50	25		30	200	nA
		−55 to +125			100	0 to 85			300	nA
Input Bias Current		25		60	250	25		200	500	nA
		−55 to +125			500	0 to 85			800	nA
Supply Current	$V_S = \pm 15V$	25		3.5	5.0	25		3.6	6.0	mA
Input Resistance		25	0.6	1.0		25	0.3	1.0		MΩ
Large Signal Voltage Gain	$V_S = \pm 15V$, $R_L = 300\Omega$, $V_O = \pm 10V$	25	100	300		25	50	150		V/mV
	$V_S = \pm 15V$, $R_L = 300\Omega$, $V_O = \pm 10V$	−55 to +125	50			0 to 85	30			V/mV
Output Voltage Swing	$V_S = \pm 15V$, $R_L = 300\Omega$	25	14.2	14.5		25	14.0	14.2		V
		−55 to +125	14.0			0 to 85	13.5			V
Output Short Circuit Current	$V_S = \pm 15V$, $R_L = 0\Omega$	25		100	130	25	25	120	140	mA
Input Voltage Range	$V_S = \pm 15V$	−55 to +125	±12			0 to 85	±12			V
										V
Common Mode Rejection Ratio	$R_S \leq 10k$	−55 to +125	90	96		0 to 85	90	96		dB
Power Supply Rejection Ratio	$R_S \leq 10k$	−55 to +125	90	96		0 to 85	90	96		dB

Note 1: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Note 2: These specifications apply for $\pm 5V \leq V_S \leq \pm 22V$ for the LH0020, $\pm 5V \leq V_S \leq \pm 18V$ for the LH0020C, pin 9 grounded, and a 5000 pF capacitor between pins 2 and 3, unless otherwise specified.

NATIONAL

LH0021/LH0021C 1.0 amp power operational amplifier
LH0041/LH0041C 0.2 amp power operational amplifier

general description

The LH0021/LH0021C and LH0041/LH0041C are general purpose operational amplifiers capable of delivering large output currents not usually associated with conventional IC Op Amps. The LH0021 will provide output currents in excess of one ampere at voltage levels of ±12V; the LH0041 delivers currents of 200 mA at voltage levels closely approaching the available power supplies. In addition, both the inputs and outputs are protected against overload. The devices are compensated with a single external capacitor and are free of any unusual oscillation or latch-up problems.

features

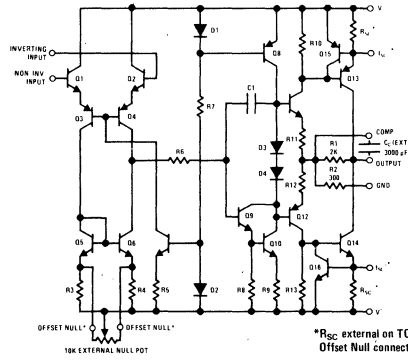
- Output current 1.0 Amp (LH0021)
  0.2 Amp (LH0041)
- Output voltage swing ±12V into 10Ω (LH0021)
  ±14V into 100Ω (LH0041)
- Wide full power bandwidth 15 kHz
- Low standby power 100 mW at ±15V
- Low input offset voltage and current 1 mV and 20 nA
- High slew rate 3.0V/μs
- High open loop gain 100 dB

The excellent input characteristics and high output capability of the LH0021 make it an ideal choice for power applications such as DC servos, capstan drivers, deflection yoke drivers, and programmable power supplies.

The LH0041 is particularly suited for applications such as torque driver for internal guidance systems, diddle yoke driver for alpha-numeric CRT displays, cable drivers, and programmable power supplies for automatic test equipment.

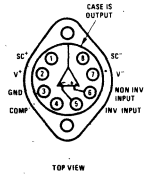
The LH0021 is supplied in a 8 pin TO-3 package rated at 20 watts with suitable heatsink. The LH0041 is supplied in both 12 pin TO-8 (2.5 watts with clip on heatsink) and a power 8 pin ceramic DIP (2 watts with suitable heatsink). The LH0021 and LH0041 are guaranteed over the temperature range of −55°C to +125°C while the LH0021C and LH0041C are guaranteed from −25°C to +85°C

schematic and connection diagrams



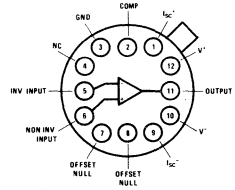
*R_{SC} external on TO-8 and TO-3 packages. R_{SC} internal on "J" package. Offset Null connections available only on TO-8 "G" package.

TO-3 Package



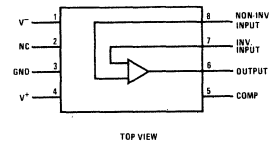
Order Number
LH0021K or LH0021CK
See Package 14

TO-8 Package



Order Number
LH0041G or LH0041CG
See Package 6

Ceramic DIP



Order Number
LH0041CJ
See Package 12

absolute maximum ratings

Supply Voltage		±18V
Power Dissipation		See curves
Differential Input Voltage		±30V
Input Voltage (Note 1)		±15V
Peak Output Current (Note 2)	LH0021/LH0021C	2.0 Amps
	LH0041/LH0041C	0.5 Amps
Output Short Circuit Duration (Note 3)		Continuous
Operating Temperature Range	LH0021/LH0041	−55°C to +125°C
	LH0021C/LH0041C	−25°C to +85°C
Storage Temperature Range		−65°C to +150°C
Lead Temperature (Soldering, 10 sec)		300°C

dc electrical characteristics for LH0021/LH0021C (Note 4)

PARAMETER	CONDITIONS	LIMITS						UNITS
		LH0021			LH0021C			
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$R_S \leq 10$ kΩ, $T_C = 25°C$		1.0	3.0		3.0	6.0	mV
	$R_S \leq 10$ kΩ			5.0			7.5	mV
Voltage Drift with Temperature	$R_S \leq 10$ kΩ		3	25		5	30	μV/°C
Offset Voltage Drift with Time			5			5		μV/week
Offset Voltage Change with Output Power			5	15		5	20	μV/watt
Input Offset Current	$T_C = 25°C$		30	100		50	200	nA
				300			500	nA
Offset Current Drift with Temperature			0.1	1.0		0.2	1.0	nA/°C
Offset Current Drift with Time			2			2		nA/week
Input Bias Current	$T_C = 25°C$		100	300		200	500	nA
				1.0			1.0	μA
Input Resistance	$T_C = 25°C$	0.3	1.0		0.3	1.0		MΩ
Input Capacitance			3			3		pF
Common Mode Rejection Ratio	$R_S \leq 10$ kΩ, $\Delta V_{CM} = \pm 10V$	70	90		70	90		dB
Input Voltage Range	$V_S = \pm 15V$	±12			±12			V
Power Supply Rejection Ratio	$R_S \leq 10$ kΩ, $\Delta V_S = \pm 10V$	80	96		70	90		dB
Voltage Gain	$V_S = \pm 15V$, $V_O = \pm 10V$							
	$R_L = 1$ kΩ, $T_C = 25°C$, $V_S = \pm 15V$, $V_O = \pm 10V$	100	200		100	200		V/mV
	$R_L = 100Ω$,	25			20			V/mV
Output Voltage Swing	$V_S = \pm 15V$, $R_L = 100Ω$	±13.5	14		±13	±14		V
	$V_S = \pm 15V$, $R_L = 10Ω$, $T_C = 25°C$	±11.0	±12		±10	±12		V
Output Short Circuit Current	$V_S = \pm 15V$, $T_C = 25°C$, $R_{SC} = 0.5Ω$	0.8	1.2	1.6	0.8	1.2	1.6	Amps
Power Supply Current	$V_S = \pm 15V$, $V_{OUT} = 0$		2.5	3.5		3.0	4.0	mA
Power Consumption	$V_S = \pm 15V$, $V_{OUT} = 0$		75	105		90	120	mW

ac electrical characteristics for LH0021/LH0021C ($T_A = 25°C$, $V_S = \pm 15V$, $C_C = 3000$ pF)

Slew Rate	$A_V = +1$, $R_L = 100Ω$	1.5	3.0		1.0	3.0		V/μs
Power Bandwidth	$R_L = 100Ω$		40			40		kHz
Small Signal Transient Response			0.3	1.0		0.3	1.5	μs
Small Signal Overshoot			5	20		10	30	%
Settling Time (0.1%)	$\Delta V_{IN} = 10V$, $A_V = +1$		4			4		μs
Overload Recovery Time			3			3		μs
Harmonic Distortion	$f = 1$ kHz, $P_O = 0.5W$		0.2			0.2		%
Input Noise Voltage	$R_S = 50Ω$, B.W. = 10 Hz to 10 kHz		5			5		μV/rms
Input Noise Current	B.W. = 10 Hz to 10 kHz		0.05			0.05		nA/rms

dc electrical characteristics for LH0041/LH0041C (Note 4)

PARAMETER	CONDITIONS	LIMITS						UNITS
		LH0041			LH0041C			
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$R_S \leq 10$ kΩ, $T_A = 25°C$		1.0	3.0		3.0	6.0	mV
	$R_S \leq 10$ kΩ			5.0			7.5	mV
Voltage Drift with Temperature	$R_S \leq 10$ kΩ		3			5		µV/°C
Offset Voltage Drift with Time			5			5		µV/week
Offset Voltage Change with Output Power			15			15		µV/watt
Offset Voltage Adjustment Range	(Note 5)		20			20		mV
Input Offset Current	$T_A = 25°C$		30	100		50	200	nA
				300			500	nA
Offset Current Drift with Temperature			0.1	1.0		0.2	1.0	nA/°C
Offset Current Drift with Time			2			2		nA/week
Input Bias Current	$T_A = 25°C$		100	300		200	500	nA
				1.0			1.0	µA
Input Resistance	$T_A = 25°C$	0.3	1.0		0.3	1.0		MΩ
Input Capacitance			3			3		pF
Common Mode Rejection Ratio	$R_S \leq 10$ kΩ, $\Delta V_{CM} = \pm 10V$	70	90		70	90		dB
Input Voltage Range	$V_S = \pm 15V$	±12			±12			V
Power Supply Rejection Ratio	$R_S \leq 10$ kΩ, $\Delta V_S = \pm 10V$	80	96		70	90		dB
Voltage Gain	$V_S = \pm 15V$, $V_O = \pm 10V$							
	$R_L = 1$ kΩ, $T_A = 25°C$	100	200		100	200		V/mV
	$V_S = \pm 15V$, $V_O = \pm 10V$							
	$R_L = 100Ω$	25			20			V/mV
Output Voltage Swing	$V_S = \pm 15V$, $R_L = 100Ω$	±13.0	14.0		±13.0	±14.0		V
Output Short Circuit Current	$V_S = \pm 15V$, $T_A = 25°C$ (Note 6)		200	300		200	300	mA
Power Supply Current	$V_S = \pm 15V$, $V_{OUT} = 0$		2.5	3.5		3.0	4.0	mA
Power Consumption	$V_S = \pm 15V$, $V_{OUT} = 0$		75	105		90	120	mW

ac electrical characteristics for LH0041/LH0041C ($T_A = 25°C$, $V_S = \pm 15V$, $C_C = 3000$ pF)

Slew Rate	$A_V = +1$, $R_L = 100Ω$	1.5	3.0		1.0	3.0		V/µs
Power Bandwidth	$R_L = 100Ω$		40			40		kHz
Small Signal Transient Response			0.3	1.0		0.3	1.5	µs
Small Signal Overshoot			5	20		10	30	%
Settling Time (0.1%)	$\Delta V_{IN} = 10V$, $A_V = +1$		4			4		µs
Overload Recovery Time			3			3		µs
Harmonic Distortion	f = 1 kHz, $P_O = 0.5W$		0.2			0.2		%
Input Noise Voltage	$R_S = 50Ω$, B.W. = 10 Hz to 10 kHz		5			5		µV/rms
Input Noise Current	B.W. = 10 Hz to 10 kHz		0.05			0.05		nA/rms

Note 1: Rating applies for supply voltages above ±15V. For supplies less than ±15V, rating is equal to supply voltage.

Note 2: Rating applies for LH0041G and LH0021K with $R_{SC} = 0Ω$.

Note 3: Rating applies as long as package power rating is not exceeded.

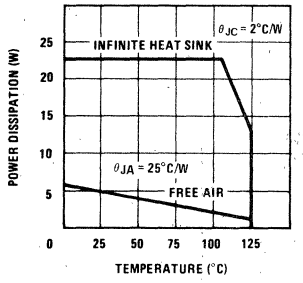
Note 4: Specifications apply for $\pm 5V \leq V_S \pm 18V$, and $-55°C \leq T_C = \leq 125°C$ for LH0021K and LH0041G, and $-25°C \leq T_C \leq +85°C$ for LH0021CK, LH0041CG and LH0041CJ unless otherwise specified. Typical values are for 25°C only.

Note 5: TO-8 "G" packages only.

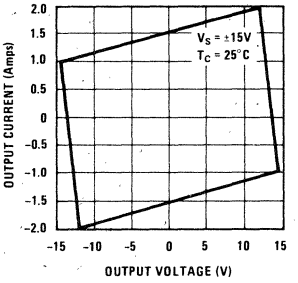
Note 6: Rating applies for "J" DIP package and for TO-8 "G" package with $R_{SC} = 3.3$ ohms.

typical performance characteristics

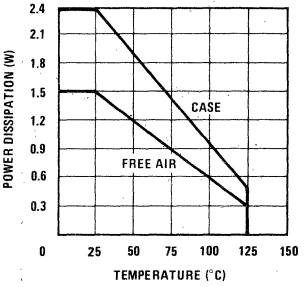
Power Derating-LH0021



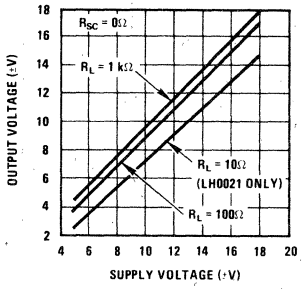
Safe Operating Area — LH0021



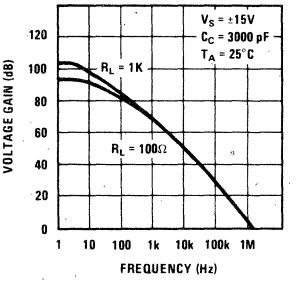
Package Power Dissipation
LH0041/LH0041C



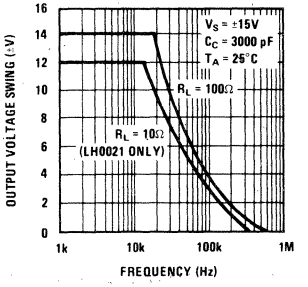
Output Voltage Swing



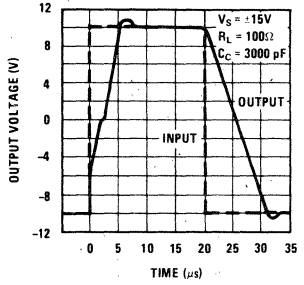
Open Loop Frequency
Response



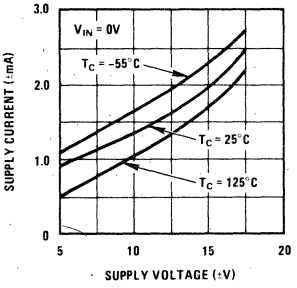
Large Signal Frequency
Response



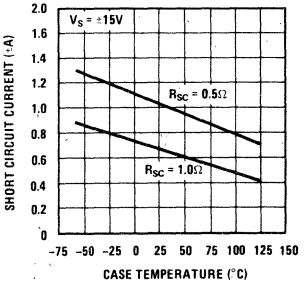
Voltage Follower Pulse
Response



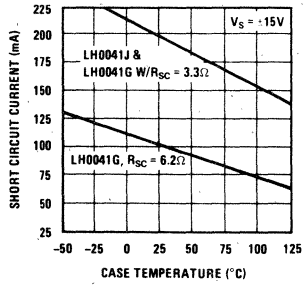
No Load Supply Current



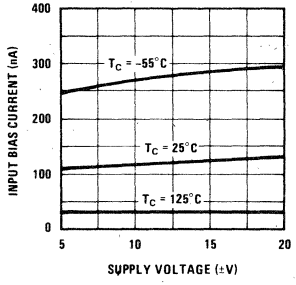
Short Circuit Current vs
Temperature LH0021/LH0021C



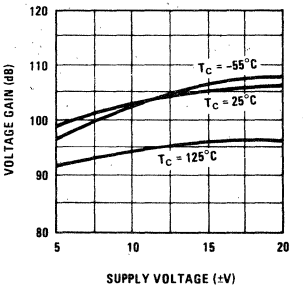
Short Circuit Current vs
Temperature LH0041/LH0041C



Input Bias Current

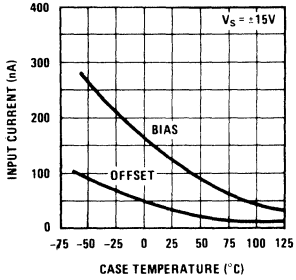


Voltage Gain

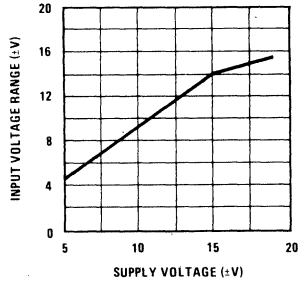


typical performance characteristics (con't)

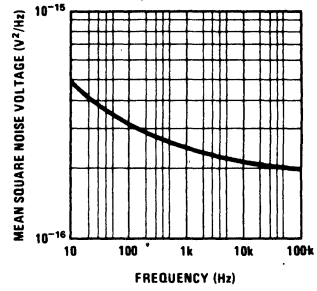
Input Current



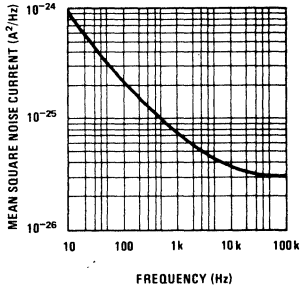
Input Voltage Range



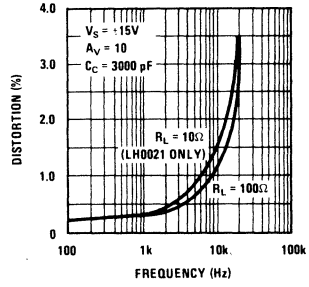
Input Noise Voltage



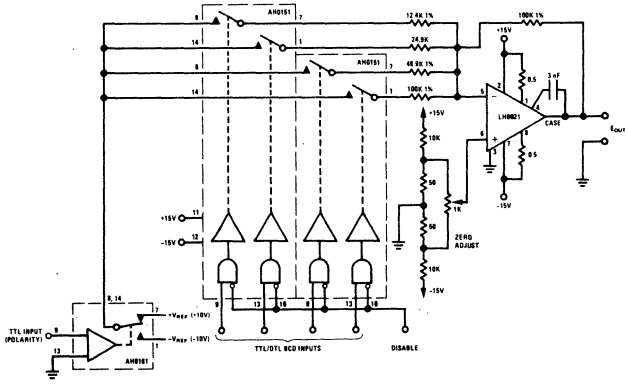
Input Noise Current



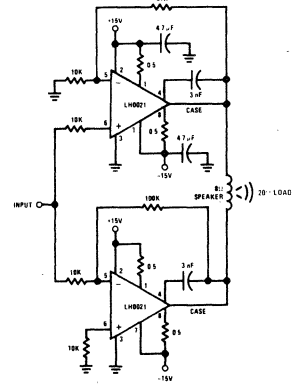
Distortion vs Frequency



typical applications

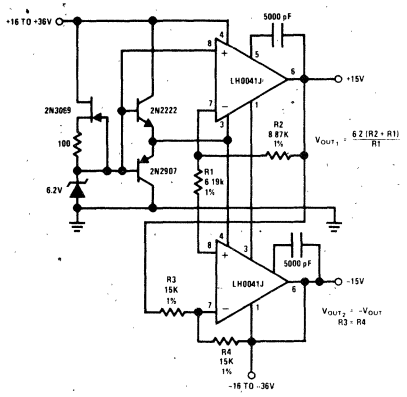


Programmable One Amp Power Supply

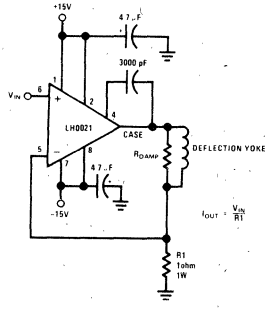


10 WATT (rms) Audio Amplifier

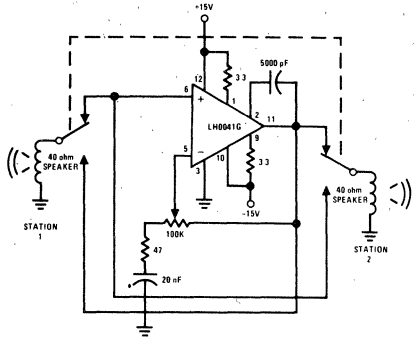
typical applications (con't)



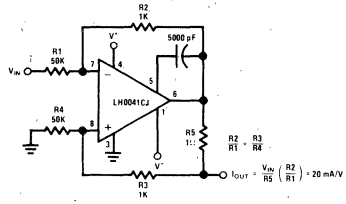
Dual Tracking One Amp Power Supply



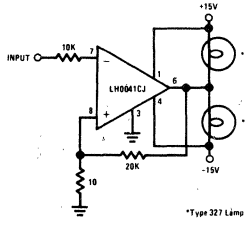
CRT Deflection Yoke Driver



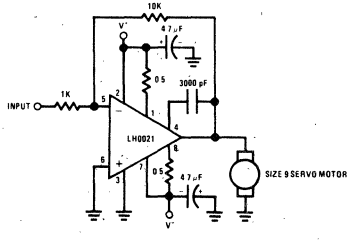
Two Way Intercom



Programmable High Current Source/Sink

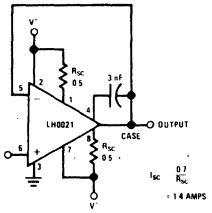


Power Comparator

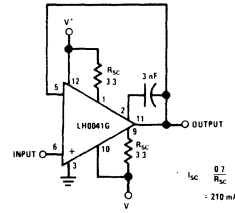


DC Servo Amplifier

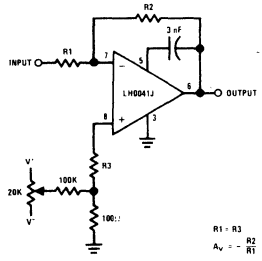
auxiliary circuits



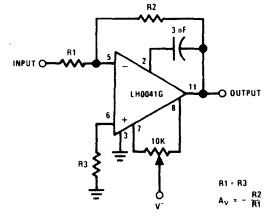
LH0021 Unity Gain Circuit with Short Circuit Limiting



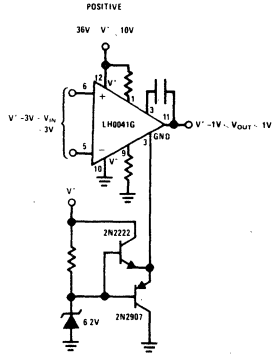
LH0041G Unity Gain with Short Circuit Limiting

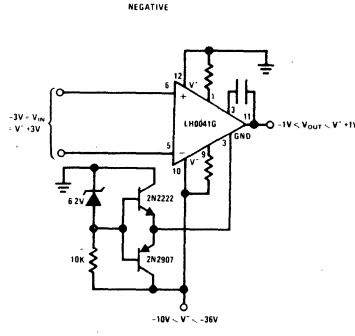


LH0041/LH0021 Offset Voltage Null Circuit (LH0041CJ Pin Connections Shown)*

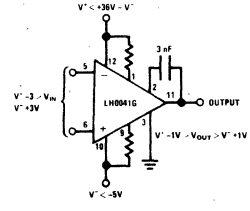


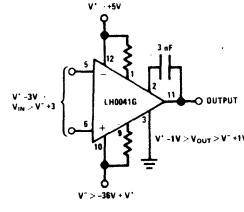
LH0041G Offset Voltage Null Circuit *





Operation from Single Supplies





Operation from Non-Symmetrical Supplies

*For additional offset null circuit techniques see National Linear Applications Handbook.

NATIONAL

Amplifiers

LH0022/LH0022C* high performance FET op amp
LH0042/LH0042C low cost FET op amp
LH0052/LH0052C precision FET op amp

general description

The LH0022/LH0042/LH0052 are a family of FET input operational amplifiers with very closely matched input characteristics, very high input impedance, and ultra-low input currents with no compromise in noise, common mode rejection ratio, open loop gain, or slew rate. The internally laser nulled LH0052 offers 200 microvolts maximum offset and 5 μV/°C offset drift. Input offset current is less than 500 femtoamps at room temperature and 100 pA maximum at 125°C. The LH0022 and LH0042 are not internally nulled but offer comparable matching characteristics. All devices in the family are internally compensated and are free of latch-up and unusual oscillation problems. The devices may be offset nulled with a single 10k trimpot with neglible effect in CMRR.

The LH0022, LH0042 and LH0052 are specified for operation over the -55°C to +125°C military temperature range. The LH0022C, LH0042C and LH0052C are specified for operation over the -25°C to +85°C temperature range.

features

- Low input offset current—500 femtoamps max. (LH0052)
- Low input offset drift—5 μV/°C max (LH0052)
- Low input offset voltage — 100 microvolts-typ.
- High open loop gain — 100 dB typ.
- Excellent slew rate — 3.0 V/μs typ.
- Internal 6 dB/octave frequency compensation
- Pin compatible with standard IC op amps (TO-5 package)

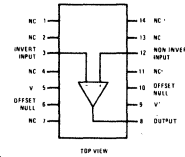
The LH0022/LH0042/LH0052 family of IC op amps are intended to fulfill a wide variety of applications for process control, medical instrumentation, and other systems requiring very low input currents and tightly matched input offsets. The LH0052 is particularly suited for long term high accuracy integrators and high accuracy sample and hold buffer amplifiers. The LH0022 and LH0042 provide low cost high performance for such applications as electrometer and photocell amplification, pico-ammeters, and high input impedance buffers.

Special electrical parameter selection and custom built circuits are available on special request.

For additional application information and information on other National operational amplifiers, see *Available Linear Applications Literature.*

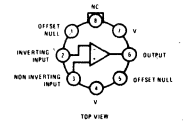
schematic and connection diagrams

Dual-In-Line Package

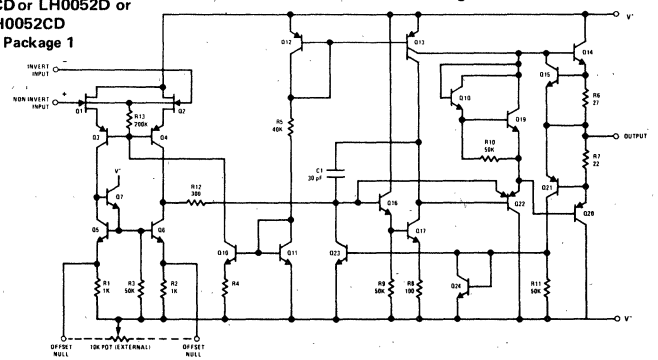


Order Number LH0022D or LH0022CD or LH0042D or LH0042CD or LH0052D or LH0052CD
See Package 1

Metal Can Package



Order Number LH0022H or LH0022CH or LH0042H or LH0042CH or LH0052H or LH0052CH
See Package 9



*Previously Called NH0022/NH0022C

absolute maximum ratings

Supply Voltage	±22V
Power Dissipation (see graph)	500 mW
Input Voltage (Note 1)	±15V
Differential Input Voltage (Note 2)	±30V
Voltage Between Offset Null and V^-	±0.5V
Short Circuit Duration	Continuous
Operating Temperature Range	
LH0022, LH0042, LH0052	−55°C to +125°C
LH0022C, LH0042C, LH0052C	−25°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

dc electrical characteristics For LH0022/LH0022C (Note 3)

PARAMETER	CONDITIONS	LIMITS						UNITS
		LH0022			LH0022C			
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$R_S \leq 100\ k\Omega$; $T_A = 25°C$, $V_S = \pm15V$		2.0	4.0		3.5	6.0	mV
	$R_S \leq 100\ k\Omega$, $V_S = \pm15V$			5.0			7.0	mV
Temperature Coefficient of Input Offset Voltage	$R_S \leq 100\ k\Omega$		5	10		5	15	µV/°C
Offset Voltage Drift with Time			3			4		µV/week
Input Offset Current	$T_A = 25°C$		0.2	2.0		1.0	5.0	pA
				2.0			0.5	nA
Temperature Coefficient of Input Offset Current		Doubles every 10°C			Doubles every 10°C			
Offset Current Drift with Time			0.1			0.1		pA/week
Input Bias Current	$T_A = 25°C$		5	10		10	25	pA
				10			2.5	nA
Temperature Coefficient of Input Bias Current		Doubles every 10°C			Doubles every 10°C			
Differential Input Resistance			10^{12}			10^{12}		Ω
Common Mode Input Resistance			10^{12}			10^{12}		Ω
Input Capacitance			4.0			4.0		pF
Input Voltage Range	$V_S = \pm15V$	±12	±13.5		±12	±13.5		V
Common Mode Rejection Ratio	$R_S \leq 10\ k\Omega$, $V_{IN} = \pm10V$	80	90		70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10\ k\Omega$, $\pm5V \leq V_S \leq \pm15V$	80	90		70	90		dB
Large Signal Voltage Gain	$R_L = 2\ k\Omega$, $V_{OUT} = \pm10V$, $T_A = 25°C$, $V_S = \pm15V$	100	200		75	160		V/mV
	$R_L = 2\ k\Omega$, $V_{OUT} = \pm10V$, $V_S = \pm15V$	50			50			V/mV
Output Voltage Swing	$R_L = 1\ k\Omega$, $T_A = 25°C$, $V_S = \pm15V$	±10	±12.5		±10	±12		V
	$R_L = 2\ k\Omega$, $V_S = \pm15V$	±10			±10			V
Output Current Swing	$V_{OUT} = \pm10V$, $T_A = 25°C$	±10	±15		±10	±15		mA
Output Resistance			75			75		Ω
Output Short Circuit Current			25			25		mA
Supply Current	$V_S = \pm15V$		2.0	2.5		2.4	2.8	mA
Power Consumption	$V_S = \pm15V$			75			85	mW

dc electrical characteristics for LH0042/LH0042C

(T_A = 25°C, V_S = ±15V; unless otherwise specified)

PARAMETER	CONDITIONS	LIMITS						UNITS
		LH0042			LH0042C			
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$R_S \leq 100\ k\Omega$		5.0	20		6.0	20	mV
Temperature Coefficient of Input Offset Voltage	$R_S \leq 100\ k\Omega$		5			10		µV/°C
Offset Voltage Drift with Time			7			10		µV/week
Input Offset Current			1	5		2	10	pA
Temperature Coefficient of Input Offset Current			Doubles every 10°C			Doubles every 10°C		
Offset Current Drift with Time			0.1			0.1		pA/week
Input Bias Current			10	25		15	50	pA
Temperature Coefficient of Input Bias Current			Doubles every 10°C			Doubles every 10°C		
Differential Input Resistance			10^{12}			10^{12}		Ω
Common Mode Input Resistance			10^{12}			10^{12}		Ω
Input Capacitance			4.0			4.0		pF
Input Voltage Range		±12	±13.5		±12	±13.5		V
Common Mode Rejection Ratio	$R_S \leq 10\ k\Omega$, V_{IN} = ±10V	70	86		70	80		dB
Supply Voltage Rejection Ratio	$R_S \leq 10\ k\Omega$, $\pm 5V \leq V_S \leq \pm 15V$	70	86		70	80		dB
Large Signal Voltage Gain	R_L = 1 kΩ, V_{OUT} = ±10V	50	150		25	100		V/mV
Output Voltage Swing	R_L = 1 kΩ	±10	±12.5		±10	±12		V
Output Current Swing	V_{OUT} = ±10V	±10	±15		±10	±15		mA
Output Resistance			75			75		Ω
Output Short Circuit Current			20			20		mA
Supply Current			2.5	3.5		2.8	4.0	mA
Power Consumption				105			120	mW

dc electrical characteristics For LH0052/LH0052C (Note 3)

PARAMETER	CONDITIONS	LIMITS						UNITS
		LH0052			LH0052C			
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$R_S < 100\ k\Omega$; V_S = ±15V, T_A = 25°C		0.1	0.5		0.2	1.0	mV
	$R_S < 100\ k\Omega$, V_S = ±15V			1.0			1.5	mV
Temperature Coefficient of Input Offset Voltage	$R_S \leq 100\ k\Omega$, V_S = ±15V		2	5		5	10	µV/°C
Offset Voltage Drift with Time			2			4		µV/week
Input Offset Current	T_A = 25°C		0.01	0.5		0.02	1.0	pA
				100			100	pA
Temperature Coefficient of Input Offset Current			Doubles every 10°C			Doubles every 10°C		
Offset Current Drift with Time			<0.1			<0.1		pA/week
Input Bias Current	T_A = 25°C		0.5	2.5		1.0	5.0	pA
				2.5			0.5	nA
Temperature Coefficient of Input Bias Current			Doubles every 10°C			Doubles every 10°C		
Differential Input Resistance			10^{12}			10^{12}		Ω
Common Mode Input Resistance			10^{12}			10^{12}		Ω
Input Capacitance			4.0			4.0		pF
Input Voltage Range	V_S = ±15V	±12	±13.5		±12	±13.5		V
Common Mode Rejection Ratio	$R_S \leq 10\ k\Omega$, V_{IN} = ±10V	80	90		76	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10\ k\Omega$, $\pm 5V < V_S \leq \pm 15V$	80	90		76	90		dB
Large Signal Voltage Gain	R_L = 2 kΩ, V_{OUT} = ±10V, V_S = ±15V, T_A = 25°C	100	200		75	160		V/mV
	R_L = 2 kΩ, V_{OUT} = ±10V, V_S = ±15V	50			50			V/mV
Output Voltage Swing	R_L = 1 kΩ, T_A = 25°C V_S = ±15V	±10	±12.5		±10	±12		V
	R_L = 2 kΩ, V_S = ±15V	±10			±10			V
Output Current Swing	V_{OUT} = ±10V, T_A = 25°C	±10	±15		±10	±15		mA
Output Resistance			75			75		Ω
Output Short Circuit Current			25			25		mA
Supply Current	V_S = ±15V		3.0	3.5		3.0	3.8	mA
Power Consumption	V_S = ±15V			105			114	mW

ac electrical characteristics For all amplifiers (T_A = 25°C, V_S = ±15V)

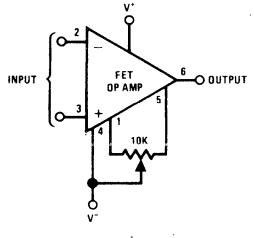
PARAMETER	CONDITIONS	LIMITS						UNITS
		LH0022/42/52			LH0022C/42C/52C			
		MIN	TYP	MAX	MIN	TYP	MAX	
Slew Rate	Voltage Follower	1.5	3.0		1.0	3.0		V/μs
Large Signal Bandwidth	Voltage Follower		40			40		kHz
Small Signal Bandwidth			1.0			1.0		MHz
Rise Time			0.3	1.5		0.3	1.5	μs
Overshoot			10	30		15	40	%
Settling Time (0.1 %)	ΔV_{IN} = 10V		4.5			4.5		μs
Overload Recovery			4.0			4.0		μs
Input Noise Voltage	R_S = 10 kΩ, f_o = 10 Hz		150			150		$nV/\sqrt{Hz}$
Input Noise Voltage	R_S = 10 kΩ, f_o = 100 Hz		55			55		$nV/\sqrt{Hz}$
Input Noise Voltage	R_S = 10 kΩ, f_o = 1 kHz		35			35		$nV/\sqrt{Hz}$
Input Noise Voltage	R_S = 10 kΩ, f_o = 10 kHz		30			30		$nV/\sqrt{Hz}$
Input Noise Voltage	BW = 10 Hz to 10 kHz, R_S = 10 kΩ		12			12		μVrms
Input Noise Current	BW = 10 Hz to 10 kHz		<.1			<.1		pArms

Note 1: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

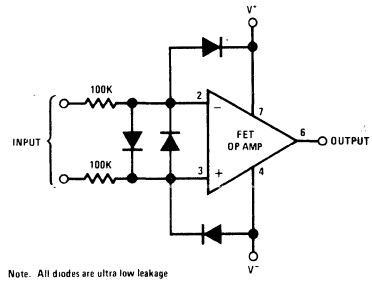
Note 2: Rating applies for minimum source resistance of 10 kΩ, for source resistances less than 10 kΩ, maximum differential input voltage is ±5V.

Note 3: Unless otherwise specified, these specifications apply for ±5V ≤ V_S ≤ ±20V and −55°C ≤ T_A ≤ ±125°C for the LH0022, LH0042 and LH0052 and −25°C ≤ T_A +85°C for the LH0022C, LH0042C and LH0052C. Typical values are given for T_A = 25°C.

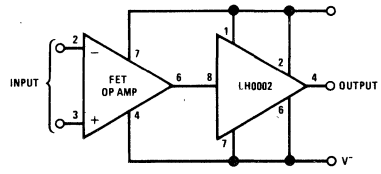
auxiliary circuits (shown for TO-5 pin out)



Offset Null

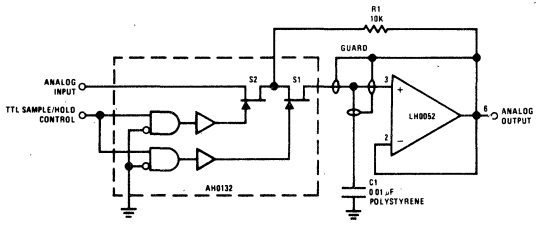


Protecting Inputs From ±150V Transients

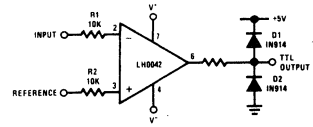


Boosting Output Drive to ±100 mA

typical applications

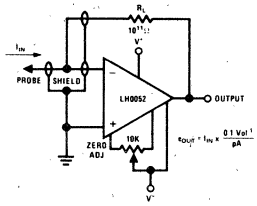


Alternate Low Drift Sample

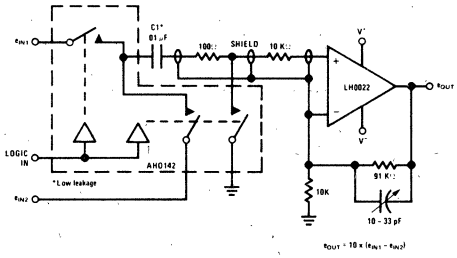


Precision Voltage Comparator

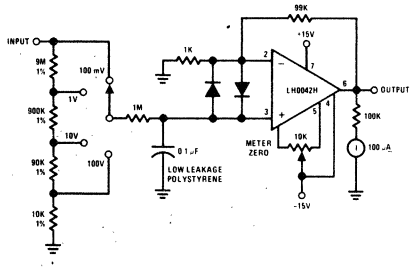
typical applications (con't)



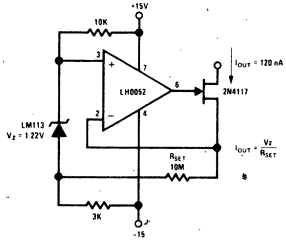
Picoamp Amplifier for pH Meters and Radiation Detectors



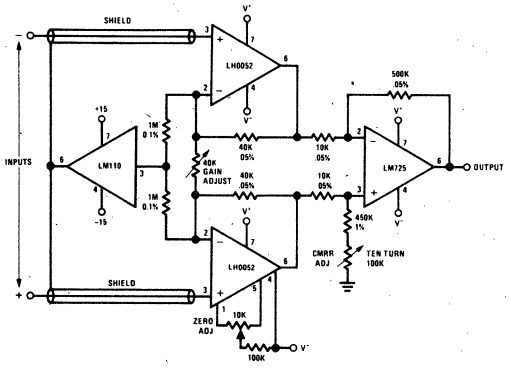
Precision Subtractor for Automatic Test Gear



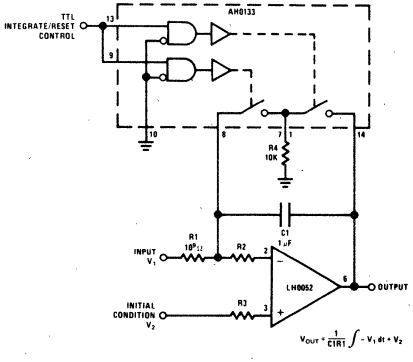
Sensitive Low Cost "VTVM"



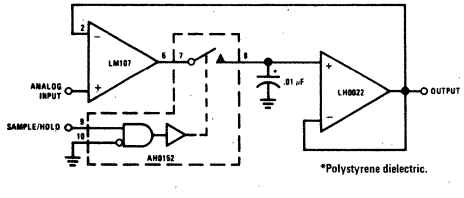
Ultra Low Level Current Source



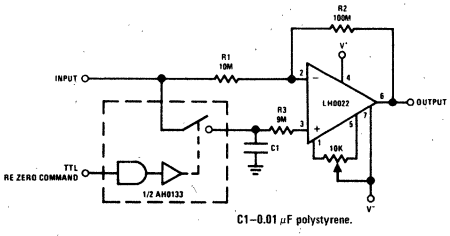
True Instrumentation Amplifier



Precision Integrator



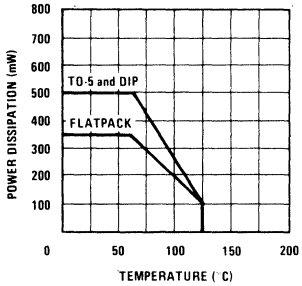
Precision Sample and Hold



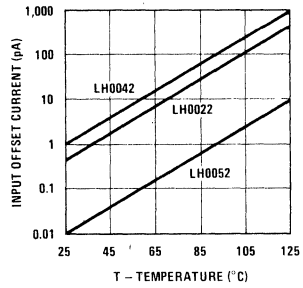
Re-Zeroing Amplifier

typical performance characteristics

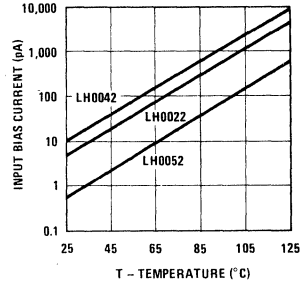
Maximum Power Dissipation



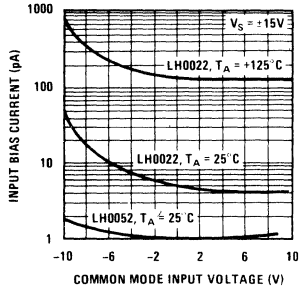
Input Offset Current vs Temperature



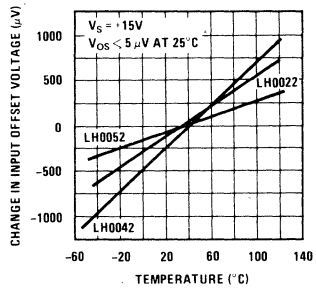
Input Bias Current vs Temperature



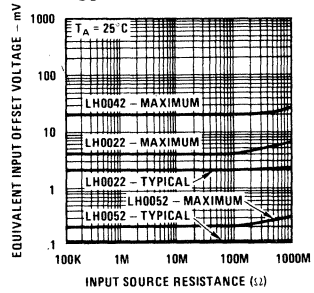
Input Bias Current vs Input Voltage



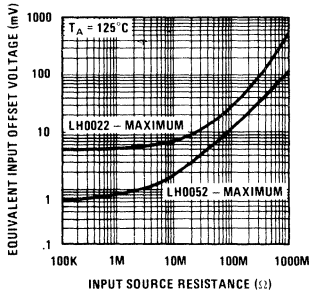
Input Offset Voltage vs Temperature



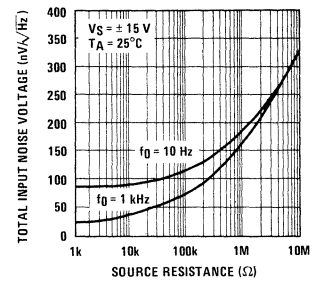
Offset Error (Without V_{OS} Null)



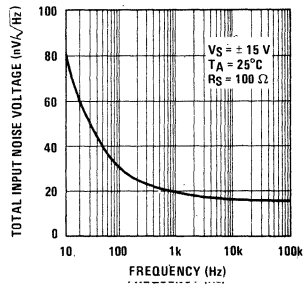
Offset Error (Without V_{OS} Null)



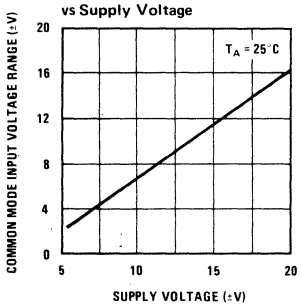
Total Input Noise Voltage* vs Source Resistance



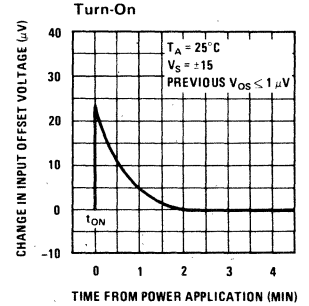
Total Input Noise Voltage* vs Frequency



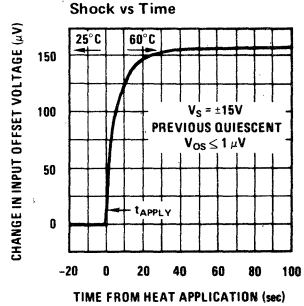
Common Mode Input Voltage vs Supply Voltage



Stabilization Time of Input Offset Voltage from Power Turn-On



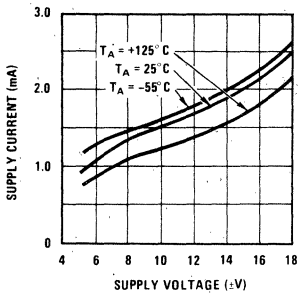
Change in Input Offset Voltage Due to Thermal Shock vs Time



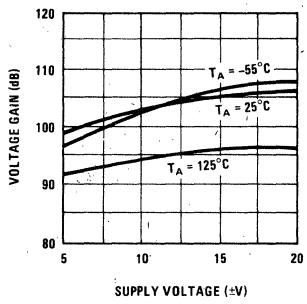
*Noise Voltage Includes Contribution from Source Resistance

typical performance characteristics (con't)

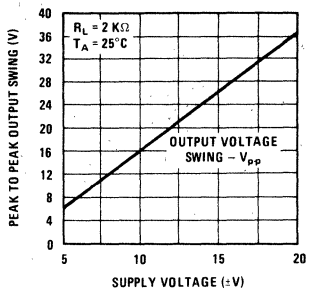
Supply Voltage vs Supply Current



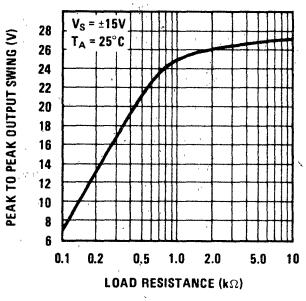
Voltage Gain



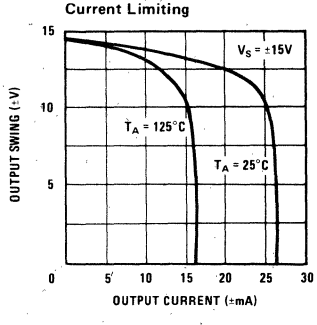
Output Swing vs Supply Voltage



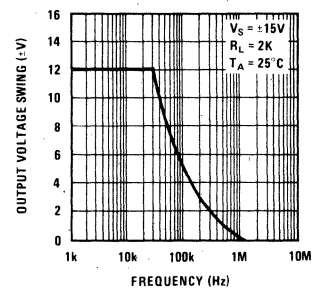
Output Voltage Swing vs Load Resistance



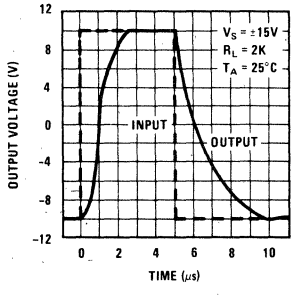
Current Limiting



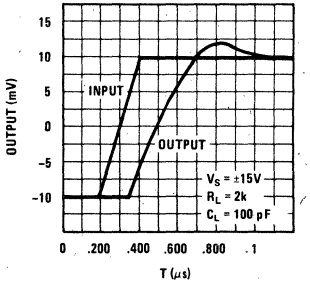
Output Voltage Swing vs Frequency



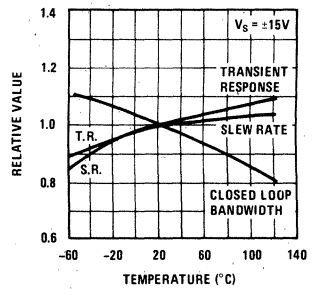
Voltage Follower Large Signal Response



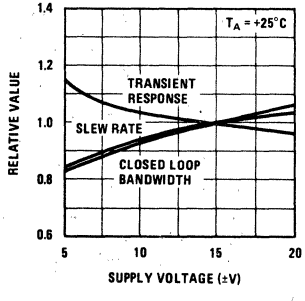
Transient Response



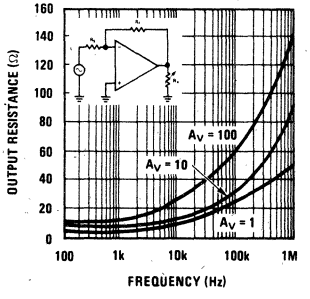
Frequency Characteristics vs Ambient Temperature



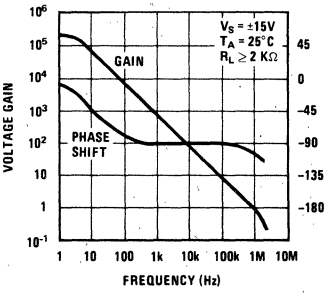
Frequency Characteristics vs Supply Voltage



Output Resistance vs Frequency



Open Loop Transfer Characteristics vs Frequency



NATIONAL

Amplifiers

LH0024/LH0024C high slew rate operational amplifier

general description

The LH0024/LH0024C is a very wide bandwidth, high slew rate operational amplifier intended to fulfill a wide variety of high speed applications such as buffers to A to D and D to A converters and high speed comparators. The device exhibits useful gain in excess of 50 MHz making it possible to use in video applications requiring higher gain accuracy than is usually associated with such amplifiers.

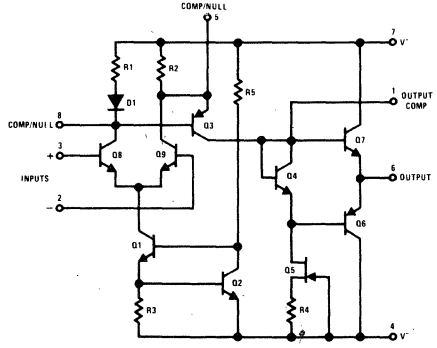
features

- Very high slew rate — 500 V/μs at Av = +1
- Wide small signal bandwidth — 70 MHz
- Wide large signal bandwidth — 15 MHz
- High output swing — ±12V into 1K
- Offset null with single pot
- Low input offset — 2 mV
- Pin compatible with standard IC op amps

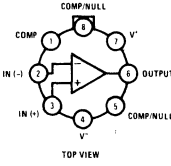
The LH0024/LH0024C's combination of wide bandwidth and high slew rate make it an ideal choice for a variety of high speed applications including active filters, oscillators, and comparators as well as many high speed general purpose applications.

The LH0024 is guaranteed over the temperature range −55°C to +125°C, whereas the LH0024C is guaranteed −25°C to +85°C.

schematic and connection diagrams



Metal Can Package



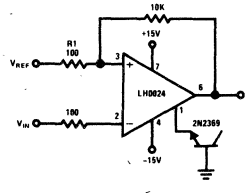
TOP VIEW

Note: For heat sink use Thermalloy 2230-5 series.

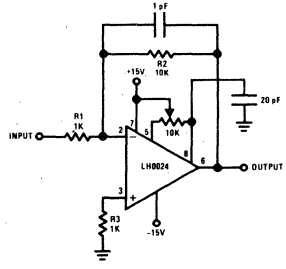
Order Number LH0024H or LH0024CH
See Package 9

typical applications

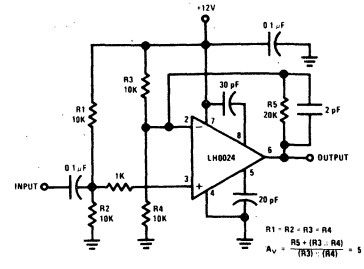
TTL Compatible Comparator



Offset Null



Video Amplifier



absolute maximum ratings

Supply Voltage		±18V
Input Voltage		Equal to Supply
Differential Input Voltage		±5V
Power Dissipation		600 mW
Operating Temperature Range	LH0024	−55°C to +125°C
	LH0024C	−25°C to +85°C
Storage Temperature Range		−65°C to +150°C
Lead Temperature (Soldering, 10 sec)		300°C

dc electrical characteristics (Note 1)

PARAMETER	CONDITIONS	LH0024			LH0024C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$R_S = 50\Omega$, $T_A = 25°C$		2.0	4.0		5.0	8.0	mV
	$R_S = 50\Omega$			6.0			10.0	mV
Average Temperature Coefficient of Input Offset Voltage	$V_S = \pm15V$, $R_S = 50\Omega$ −55°C to 125°C		−20			−25		µV/°C
Input Offset Current	$T_A = 25°C$		2.0	5.0		4.0	15.0	µA
				10.0			20.0	µA
Input Bias Current	$T_A = 25°C$		15	30		18	40	µA
				40			50	µA
Supply Current			12.5	13.5		12.5	13.5	mA
Large Signal Voltage Gain	$V_S = \pm15V$, $R_L = 1k$, $T_A = 25°C$	4	5		3	4		V/mV
	$V_S = \pm15V$, $R_L = 1k$	3			2.5			V/mV
Input Voltage Range	$V_S = \pm15V$	±12	±13		±12	±13		V
Output Voltage Swing	$V_S = \pm15V$, $R_L = 1k$, $T_A = 25°C$	±12	±13		±10	±13		V
	$V_S = \pm15V$, $R_L = 1k$	±10			±10			V
Slew Rate	$V_S = \pm15V$, $R_L = 1k$, $C_1 = C_2 = 30$ pF $A_V = +1$, $T_A = 25°C$	400	500		250	400		V/µs
Common Mode Rejection Ratio	$V_S = \pm15V$, $\Delta V_{IN} = \pm10V$ $R_S = 50\Omega$		60			60		dB
Power Supply Rejection Ratio	$\pm5V \leq V_S \leq \pm18V$ $R_S = 50\Omega$		60			60		dB

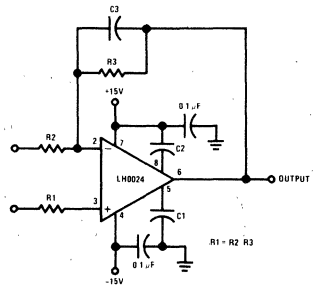
Note 1: These specifications apply for $V_S = \pm15V$ and −55°C to +125°C for the LH0024 and −25°C to +85°C for the LH0024C.

frequency compensation

TABLE I

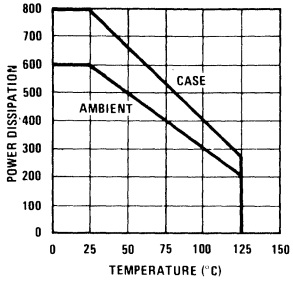
CLOSED LOOP GAIN	C_1	C_2	C_3
100	0	0	0
20	0	0	0
10	0	20 pF	1 pF
1	30 pF	30 pF	3 pF

Frequency Compensation Circuit

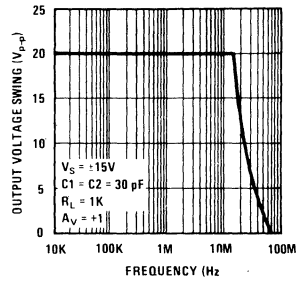


typical performance characteristics

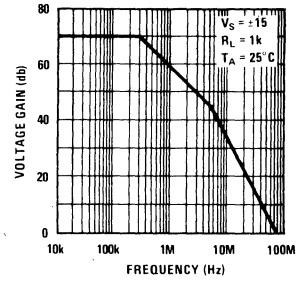
Maximum Power Dissipation



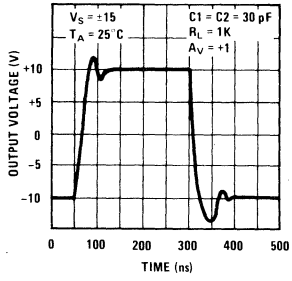
Large Signal Frequency Response



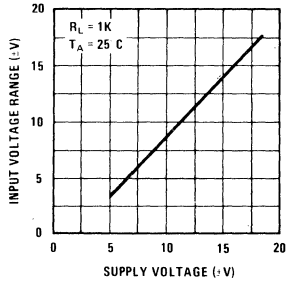
Open Loop Frequency Response



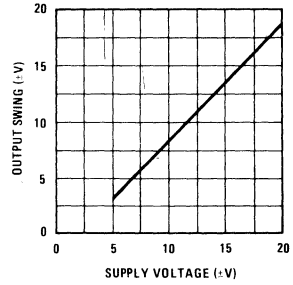
Voltage Follower Pulse Response



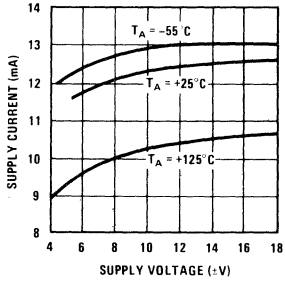
Input Voltage vs Supply Voltage



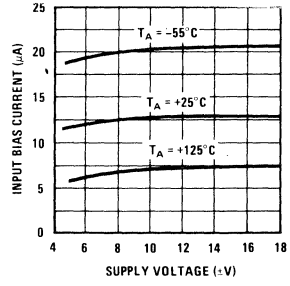
Output Voltage Swing



Supply Current vs Supply Voltage



Input Bias Current vs Voltage



applications information

1. Layout Considerations

The LH0024/LH0024C, like most high speed circuitry, is sensitive to layout and stray capacitance. Power supplies should be by-passed as near the device as is practicable with at least .01 μF disc type capacitors. Compensating capacitors should also be placed as close to device as possible.

2. Compensation Recommendations

Compensation schemes recommended in Table 1 work well under typical conditions. However, poor layout and long lead lengths can degrade the performance of the LH0024 or cause the device to oscillate. Slight adjustments in the values for C1, C2, and C3 may be necessary for a given layout. In particular, when operating at a gain of −1, C3 may require adjustment in order to perfectly cancel the input capacitance of the device.

When operating the LH0024/LH0024C at a gain of +1, the value of R1 should be at least 1K ohm.

The case of the LH0024 is electrically isolated from the circuit; hence, it may be advantageous to drive the case in order to minimize stray capacitances.

3. Heat Sinking

The LH0024/LH0024C is specified for operation without the use of an explicit heat sink. However, internal power dissipation does cause a significant temperature rise. Improved offset voltage drift can be obtained by limiting the temperature rise with a clip-on heat sink such as the Thermalloy 2228B or equivalent.

NATIONAL

Amplifiers

LH0032/LH0032C ultra fast FET operational amplifier

general description

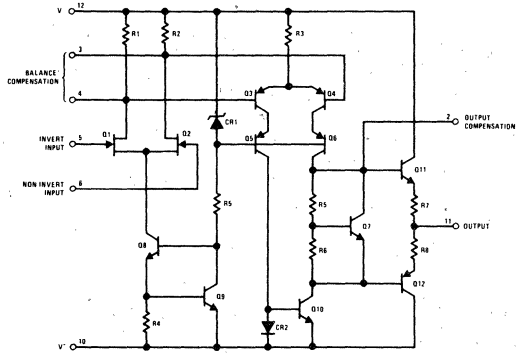
The LH0032/LH0032C is a high slew rate, high input impedance differential operational amplifier suitable for diverse application in fast signal handling. The high allowable differential input voltage, ease of output clamping, and high output drive capability particularly suit it for comparator applications. It may be used in applications normally reserved for video amplifiers allowing the use of operational gain setting and frequency response shaping into the megahertz region.

features

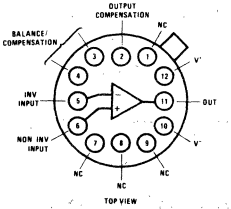
- High slew rate 500 V/μs
- High bandwidth 70 MHz
- High input impedance $10^{12}\Omega$
- Low input bias current 20 pA max
- Offset null with single pot
- Low input offset voltage 2 mV max
- No compensation for gains above 50

The LH0032's wide bandwidth, high input impedance and high output capacity make it an ideal choice for applications such as summing amplifiers in high speed D to A's, buffers in data acquisition systems, and sample and hold circuits. Additional applications include high speed integrators and video amplifiers. The LH0032 is guaranteed over the temperature range −55°C to +125°C and the LH0032C is guaranteed from −25°C to +85°C.

schematic and connection diagrams



Metal Can Package



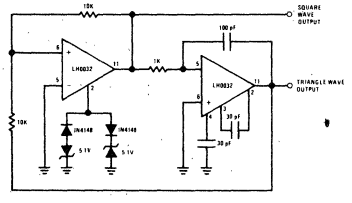
Note: For heat sink use thermalloy 2240 series or Wakefield 215-XX series.

Order Number LH0032G or LH0032CG

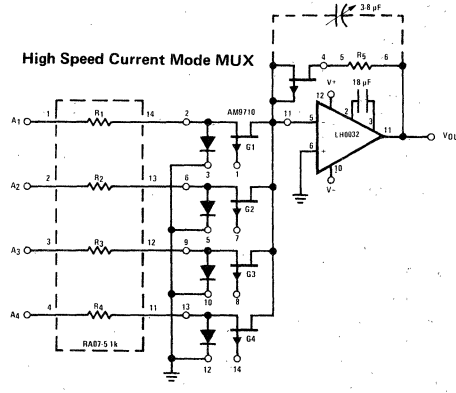
See Package 6

typical applications

1 MHz Function Generator



High Speed Current Mode MUX



absolute maximum ratings

Supply Voltage		±18V
Input Voltage		$\pm V_S$
Differential Input Voltage		±30V
Power Dissipation		See curve
Operating Temperature Range	LH0032	−55°C to +125°C
	LH0032C	−25°C to +85°C
Storage Temperature Range		−65°C to +150°C
Lead Temperature (Soldering, 10 sec)		300°C

dc electrical characteristics (Note 1)

PARAMETER	CONDITIONS	LH0032			LH0032C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	T_A = 25°C		2	5		5	15	mV
				10			20	mV
Average Offset Voltage Drift			25			25		µV/°C
Input Bias Current	T_A = 25°C		10	100		25	200	pA
				50			15.0	nA
Input Offset Current	T_A = 25°C		5	25		10	50	pA
				25			5	nA
Large Signal Voltage Gain	V_{OUT} = ±10V, f = 1 kHz, R_L = 1 kΩ, T_A = 25°C	60	70		60	70		dB
	V_{OUT} = ±10V, f = 1 kHz, R_L = 1 kΩ	57			57			dB
Input Voltage Range		±10	±12		±10	±12		V
Output Voltage Swing	R_L = 1 kΩ	±10	±13.5		+10	±13		V
Power Supply Rejection Ratio	ΔV_S = ±10V	50	60		50	60		dB
Common Mode Rejection Ratio	ΔV_{IN} = 10V	50	60		50	60		dB
Supply Current	T_A = 25°C		18	20		20	22	mA

ac electrical characteristics (Note 2)

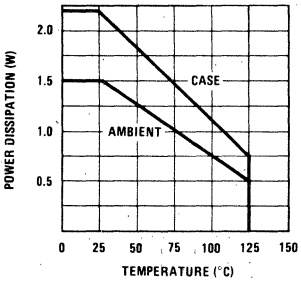
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Slew Rate	A_V = +1, ΔV_{IN} = 20V	350	500		V/µs
Settling Time to 1% of Final Value	A_V = −1, ΔV_{IN} = 20V		100		ns
Settling Time to 0.1% of Final Value	A_V = −1, ΔV_{IN} = 20V		300		ns
Small Signal Rise Time	A_V = +1, ΔV_{IN} = 1V		8	20	ns
Small Signal Delay Time	A_V = +1, ΔV_{IN} = 1V		10	25	ns

Note 1: These specifications apply at V_S = ±15V and over −55°C to +125°C for the LH0032 and −25°C to +85°C for the LH0032C, unless otherwise specified.

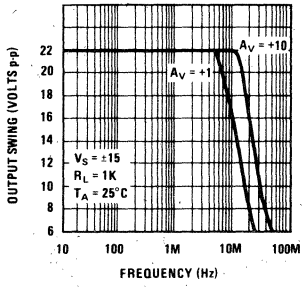
Note 2: These specifications apply for V_S = ±15V, R_L = 1 kΩ and T_A = 25°C.

typical performance characteristics

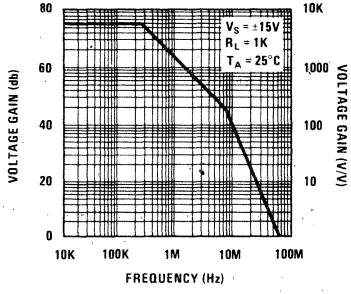
Maximum Power Dissipation



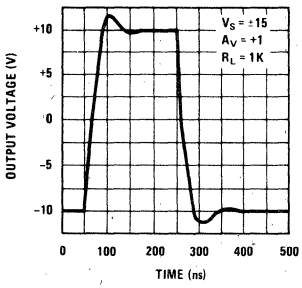
Large Signal Frequency Response



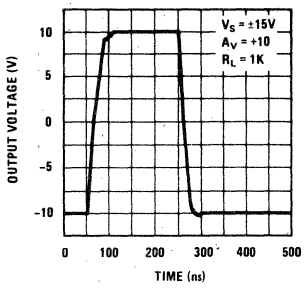
Open Loop Frequency Response



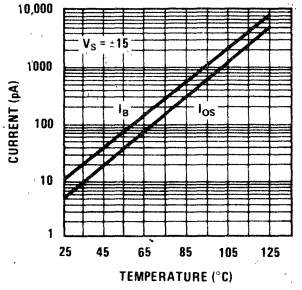
Large Signal Pulse Response



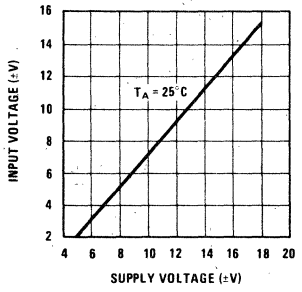
Large Signal Pulse Response



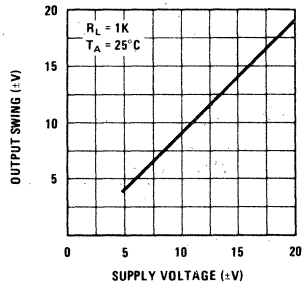
Input Bias and Offset Current vs Temperature



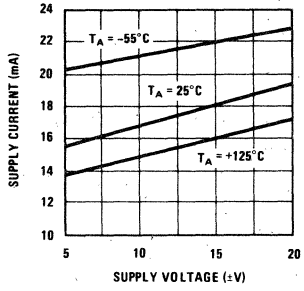
Input Voltage Range



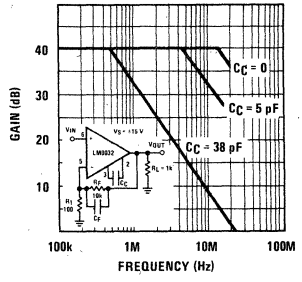
Output Swing



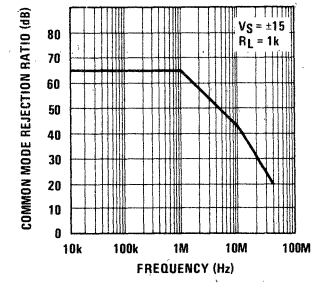
Supply Current vs Supply Voltage



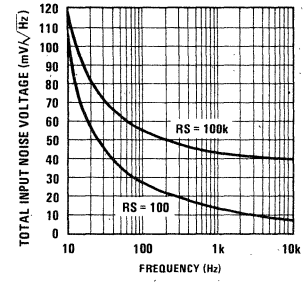
Closed Loop Frequency Response



Common Mode Rejection Ratio vs. Frequency



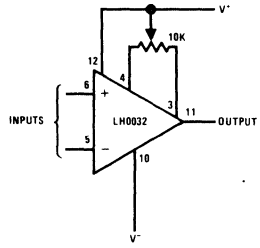
Total Input Noise Voltage vs. Frequency*



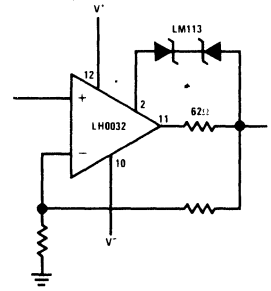
* Noise voltage includes contribution from source resistance.

auxiliary circuits

Offset Null

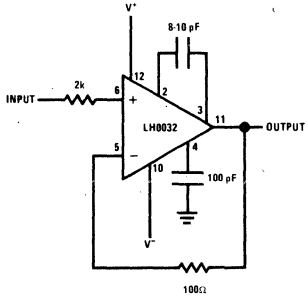


Output Short Circuit Protection

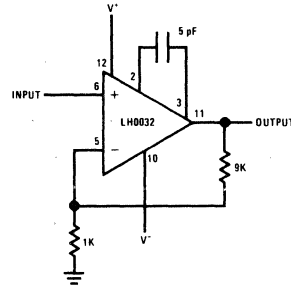


typical applications (con't)

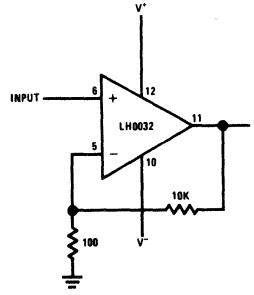
Unity Gain Amplifier



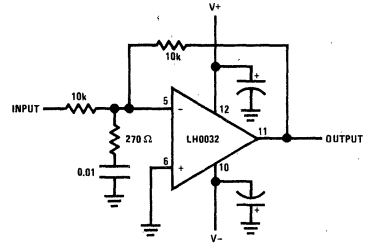
10X Buffer Amplifier



100X Buffer Amplifier

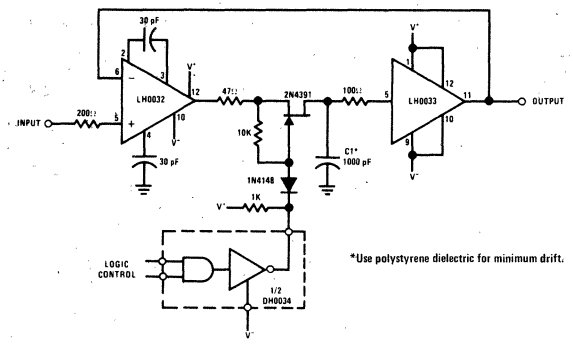


Non-Compensated Unity Gain Inverter

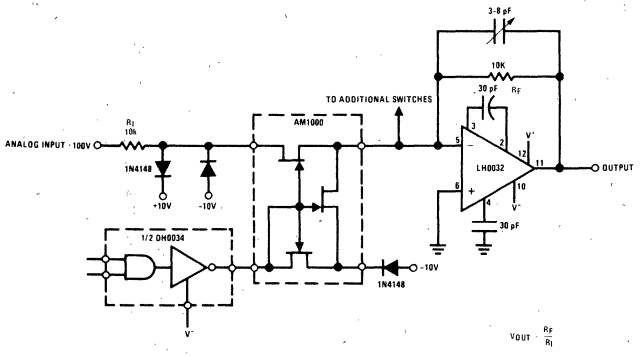


typical applications (con't)

High Speed Sample and Hold



Current Mode Multiplexer



applications information

Power Supply Decoupling

The LH0032/LH0032C like most high speed circuits is sensitive to layout and stray capacitance. Power supplies should be by-passed as near to Pins 10 and 12 as practicable with low inductance capacitors such as 0.01 μF disc ceramics. Compensation components should also be located close to the appropriate pins to minimize stray reactances.

Input Capacitance

The input capacitance to the LH0032/LH0032C is typically 5 pF and thus may form a significant time constant with high value resistors. For optimum performance, the input capacitance to the inverting input should be compensated by a small capacitor across the feedback resistor. The value is strongly dependent on layout and closed loop gain, but will typically be in the neighborhood of several picofarads.

In the non-inverting configuration, it may be advantageous to bootstrap the case and/or a guard conductor to the inverting input. This serves both to divert leakage currents away from the non-inverting input and to reduce the effective input capacitance. A unity gain follower so treated will have an input capacitance under a picofarad.

Heat Sinking

While the LH0032/LH0032C is specified for operation without any explicit head sink, internal power dissipation does cause a significant temperature rise. Improved bias current performance can thus be obtained by limiting this temperature rise with a small head sink such as the Thermalloy No. 2241 or equivalent. The case of the device has no internal connection, so it may be electrically connected to the sink if this is advantageous. Be aware, however, that this will affect the stray capacitances to all pins and may thus require adjustment of circuit compensation values.

NATIONAL

LH0036/LH0036C instrumentation amplifier

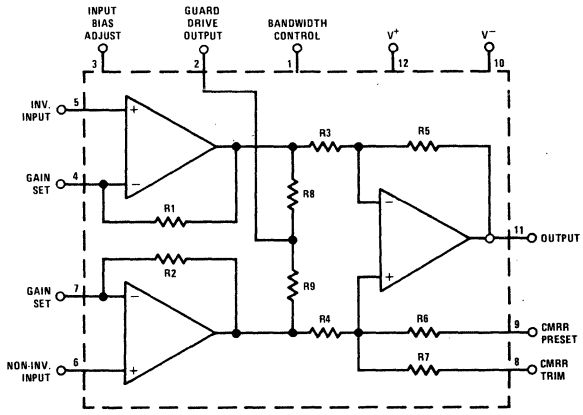
general description

The LH0036/LH0036C is a true micro power instrumentation amplifier designed for precision differential signal processing. Extremely high accuracy can be obtained due to the 300 MΩ input impedance and excellent 100 dB common mode rejection ratio. It is packaged in a hermetic TO-8 package. Gain is programmable with one external resistor from 1 to 1000. Power supply operating range is between ±1V and ±18V. Input bias current and output bandwidth are both externally adjustable or can be set by internally set values. The LH0036 is specified for operation over the −55°C to +125°C temperature range and the LH0036C is specified for operation over the −25°C to +85°C temperature range.

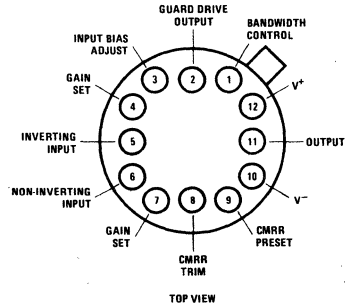
features

- High input impedance 300 MΩ
- High CMRR 100 dB
- Single resistor gain adjust 1 to 1000
- Low power 90μW
- Wide supply range ±1V to ±18V
- Adjustable input bias current
- Adjustable output bandwidth
- Guard drive output

equivalent circuit and connection diagrams



TO-8 Metal Can Package



TOP VIEW

Order Number LH0036 or LH0036C
See Package 6

absolute maximum ratings

Supply Voltage	±18V	Short Circuit Duration	Continuous
Differential Input Voltage	±30V	Operating Temperature Range	
Input Voltage Range	$\pm V_S$	LH0036	−55°C to +125°C
Shield Drive Voltage	$\pm V_S$	LH0036C	−25°C to +85°C
CMRR Preset Voltage	$\pm V_S$	Storage Temperature Range	−65°C to +150°C
CMRR Trim Voltage	$\pm V_S$	Lead Temperature, Soldering 10 seconds	300°C
Power Dissipation (Note 3)	1.5W		

electrical characteristics (Notes 1 and 2)

PARAMETER	CONDITIONS	LIMITS						UNITS
		LH0036			LH0036C			
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage (V_{IOS})	R_S = 1.0kΩ, T_A = 25°C		0.5	1.0		1.0	2.0	mV
	R_S = 1.0kΩ			2.0			3.0	mV
Output Offset Voltage (V_{OOS})	R_S = 1.0kΩ, T_A = 25°C		2.0	5.0		5.0	10	mV
	R_S = 1.0kΩ			6.0			12	mV
Input Offset Voltage Tempco ($\Delta V_{IOS}/\Delta T$)	$R_S \leq$ 1.0kΩ		10			10		µV/°C
Output Offset Voltage Tempco ($\Delta V_{OOS}/\Delta T$)			15			15		µV/°C
Overall Offset Referred to Input (V_{OS})	A_V = 1.0		2.5			6.0		mV
	A_V = 10		0.7			1.5		mV
	A_V = 100		0.52			1.05		mV
	A_V = 1000		0.502			1.005		mV
Input Bias Current (I_B)	T_A = 25°C		40	100		50	125	nA
				150			200	nA
Input Offset Current (I_{OS})	T_A = 25°C		10	40		20	50	nA
				80			100	nA
Small Signal Bandwidth	A_V = 1.0, R_L = 10kΩ		350			350		kHz
	A_V = 10, R_L = 10kΩ		35			35		kHz
	A_V = 100, R_L = 10kΩ		3.5			3.5		kHz
	A_V = 1000, R_L = 10kΩ		350			350		Hz
Full Power Bandwidth	V_{IN} = ±10V, R_L = 10k, A_V = 1		5.0			5.0		kHz
Input Voltage Range	Differential	±10	±12		±10	±12		V
	Common Mode	±10	±12		±10	±12		V
Gain Nonlinearity			0.03			0.03		%
Deviation From Gain Equation Formula	A_V = 1 to 1000		±0.3	±1.0		±1.0	±3.0	%
PSRR	±5.0V $\leq V_S \leq$ ±15V, A_V = 1.0		1.0	2.5		1.0	5.0	mV/V
	±5.0V $\leq V_S \leq$ ±15V, A_V = 100		0.05	0.25		0.10	0.50	mV/V
CMRR	A_V = 1.0 DC to		1.0	2.5		2.5	5.0	mV/V
	A_V = 10 100 Hz		0.1	0.25		0.25	0.50	mV/V
	A_V = 100 ΔR_S = 1.0k		50	100		50	100	µV/V
Output Voltage	V_S = ±15V, R_L = 10kΩ,	±10	±13.5		±10	±13.5		V
	V_S = ±1.5V, R_L = 100kΩ	±0.6	±0.8		±0.6	±0.8		V
Output Resistance			0.5			0.5		Ω
Supply Current			300	400		400	600	µA
Equivalent Input Noise Voltage			20			20		µV/p-p
Slew Rate	ΔV_{IN} = ±10V, R_L = 10kΩ, A_V = 1.0		0.3			0.3		V/µs
Settling Time	To ±10 mV, R_L = 10kΩ, ΔV_{OUT} = 1.0V							
	A_V = 1.0		3.8			3.8		µs
	A_V = 100		180			180		µs

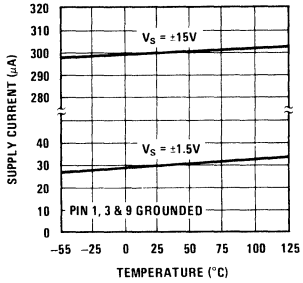
Note 1: Unless otherwise specified, all specifications apply for V_S = ±15V, Pins 1, 3, and 9 grounded, −25°C to +85°C for the LH0036C and −55°C to +125°C for the LH0036.

Note 2: All typical values are for T_A = 25°C.

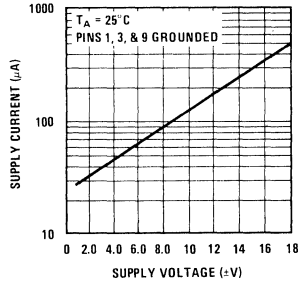
Note 3: The maximum junction temperature is 150°C. For operation at elevated temperature derate the G package on a thermal resistance of 90°C/W, above 25°C.

typical performance characteristics

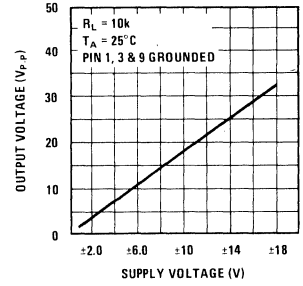
Supply Current vs Temperature



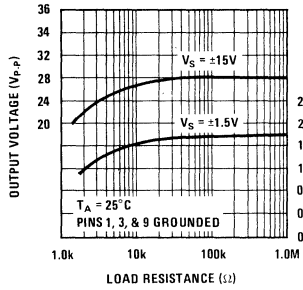
Supply Current vs Supply Voltage



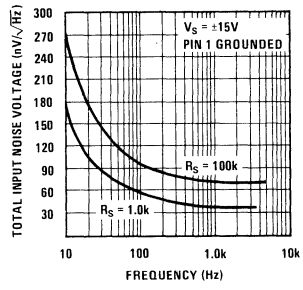
Output Voltage Swing vs Supply Voltage



Peak to Peak Output Voltage Swing vs R_L

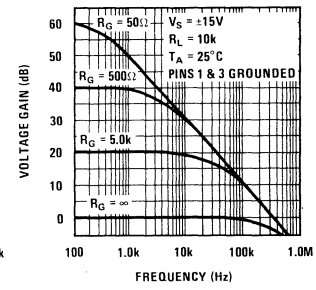


Total Input Noise Voltage* vs Frequency

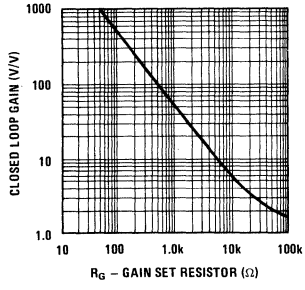


*Noise voltage includes contribution from source resistance

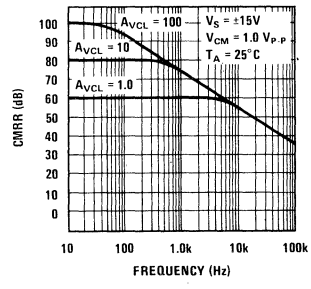
Closed Loop Voltage Gain vs Frequency



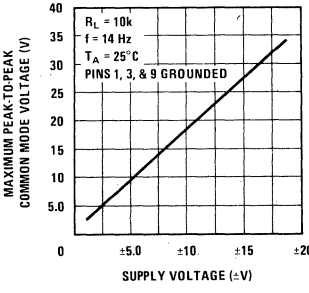
Closed Loop Voltage Gain



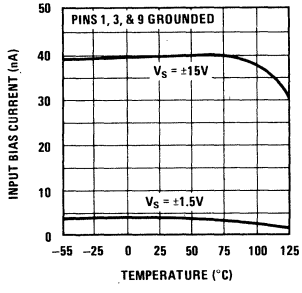
CMRR vs Frequency



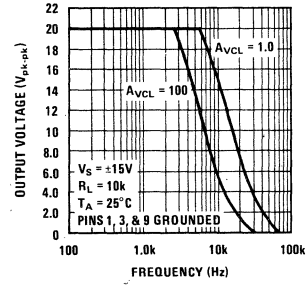
Common Mode Voltage vs Supply Voltage



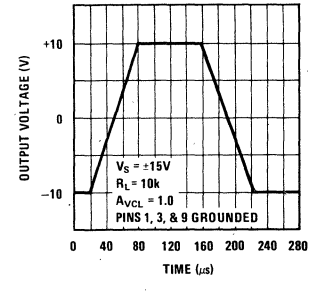
Input Bias Current



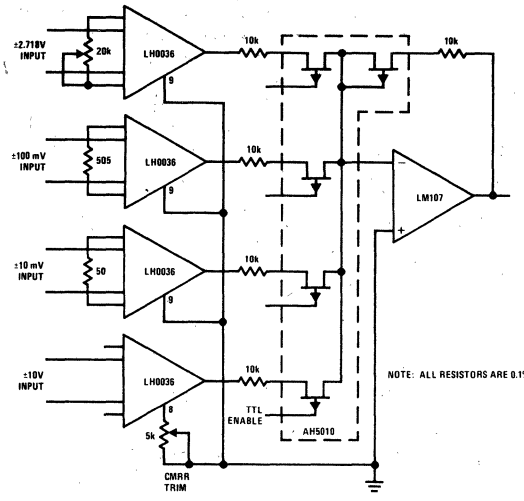
Output Voltage Swing vs Frequency



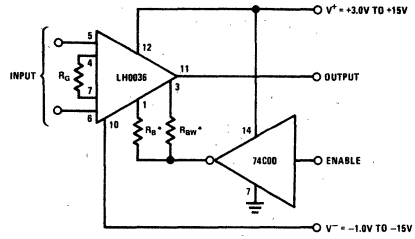
Large Signal Pulse Response



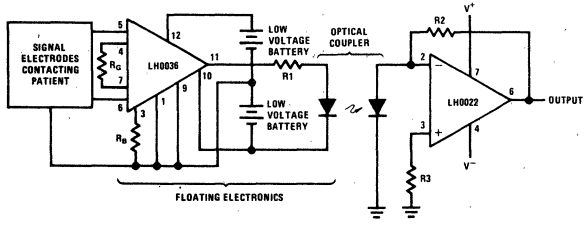
typical applications



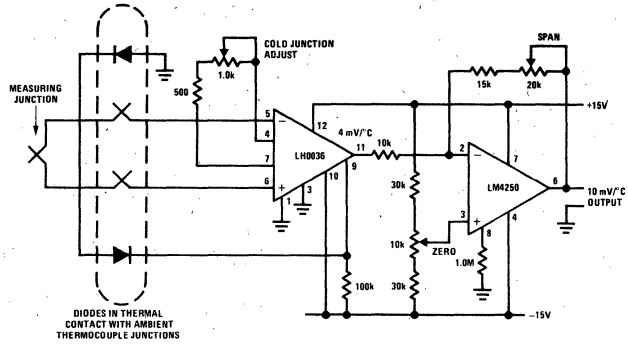
Pre MUX Signal Conditioning



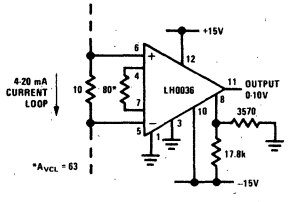
Instrumentation Amplifier with Logic Controlled Shut-Down



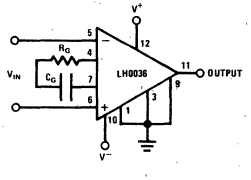
Isolation Amplifier for Medical Telemetry

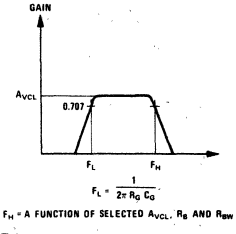


Thermocouple Amplifier with Cold Junction Compensation



Process Control Interface





High Pass Filter

applications information

THEORY OF OPERATION

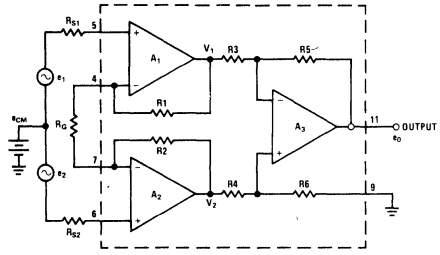


FIGURE 1. Simplified LH0036

The LH0036 is a 2 stage amplifier with a high input impedance gain stage comprised of A_1 and A_2 and a differential to single-ended unity gain stage, A_3. Operational amplifier, A_1, receives differential input signal, e_1, and amplifies it by a factor equal to $(R1 + R_G)/R_G$.

A_1 also receives input e_2 via A_2 and R2. e_2 is seen as an inverting signal with a gain of $R1/R_G$. A_1 also receives the common mode signal e_{CM} and processes it with a gain of +1.

Hence:

$$V_1 = \frac{R1 + R_G}{R_G} e_1 - \frac{R1}{R_G} e_2 + e_{CM} \quad (1)$$

By similar analysis V_2 is seen to be:

$$V_2 = \frac{R2 + R_G}{R_G} e_2 - \frac{R2}{R_G} e_1 + e_{CM} \quad (2)$$

For R1 = R2:

$$V_2 - V_1 = \left[\left(\frac{2R1}{R_G}\right) + 1\right](e_2 - e_1) \quad (3)$$

Also, for R3 = R5 = R4 = R6, the gain of $A_3 = 1$, and:

$$e_0 = (1)(V_2 - V_1) = (e_2 - e_1)\left[1 + \left(\frac{2R1}{R_G}\right)\right] \quad (4)$$

As can be seen for identically matched resistors, e_{CM} is cancelled out, and the differential gain is dictated by equation (4).

For the LH0036, equation (4) reduces to:

$$A_{VCL} = \frac{e_0}{e_2 - e_1} = 1 + \frac{50k}{R_G} \quad (5a)$$

The closed loop gain may be set to any value from 1 ($R_G = \infty$) to 1000 ($R_G \cong 50\Omega$). Equation (5a) re-arranged in more convenient form may be used to select R_G for a desired gain:

$$R_G = \frac{50k}{A_{VCL} - 1} \quad (5b)$$

USE OF BANDWIDTH CONTROL (pin 1)

In the standard configuration, pin 1 of the LH0036 is simply grounded. The amplifier's slew rate in this configuration is typically 0.3V/μs and small signal bandwidth 350 kHz for $A_{VCL} = 1$. In some applications, particularly at low frequency, it may be desirable to limit bandwidth in order to minimize the overall noise bandwidth of the device. A resistor R_{BW} may be placed between pin 1 and ground to accomplish this purpose. Figure 2 shows typical small signal bandwidth versus R_{BW}.

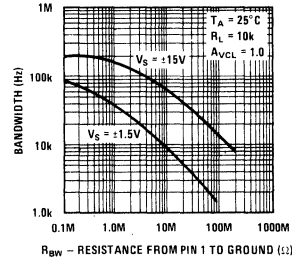


FIGURE 2. Bandwidth vs R_{BW}

It also should be noted that large signal bandwidth and slew rate may be adjusted down by use of R_{BW}. Figure 3 is plot of slew rate versus R_{BW}.

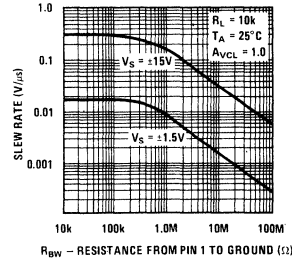


FIGURE 3. Output Slew Rate vs R_{BW}

CMRR CONSIDERATIONS

Use of Pin 9, CMRR Preset

Pin 9 should be grounded for nominal operation. An internal factory trimmed resistor, R6, will yield a CMRR in excess of 80 dB (for $A_{VCL} = 100$). Should a higher CMRR be desired, pin 9 should be left open and the procedure, in this section followed.

DC Off-set Voltage and Common Mode Rejection Adjustments

Off-set may be nulled using the circuit shown in Figure 4.

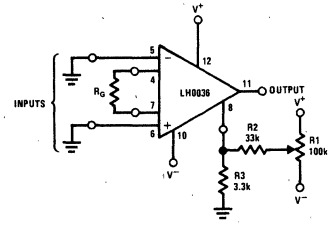


FIGURE 4. V_{OS} Adjustment Circuit

Pin 8 is also used to improve the common mode rejection ratio as shown in Figure 5. Null is

applications information (con't)

achieved by alternately applying ±10V (for V^+ & V^- = 15V) to the inputs and adjusting R1 for minimum change at the output.

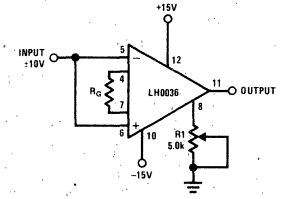


FIGURE 5. CMRR Adjustment Circuit

The circuits of Figure 4 and 5 may be combined as shown in Figure 6 to accomplish both V_{OS} and CMRR null. However, the V_{OS} and CMRR adjustment are interactive and several iterations are required. The procedure for null should start with the inputs grounded.

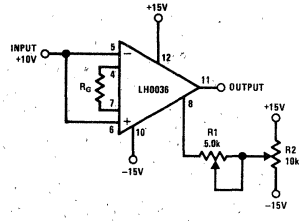
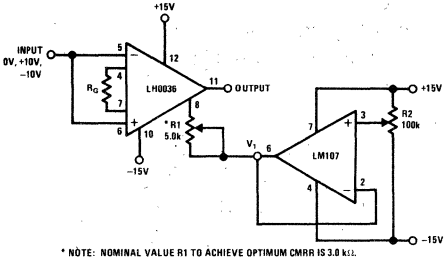


FIGURE 6. Combined CMRR, V_{OS} Adjustment Circuit

R2 is adjusted for V_{OS} null. An input of +10V is then applied and R1 is adjusted for CMRR null. The procedure is then repeated until the optimum is achieved.

A circuit which overcomes adjustment interaction is shown in Figure 7. In this case, R2 is adjusted first for output null of the LH0036. R1 is then adjusted for output null with +10V input. It is always a good idea to check CMRR null with a −10V input. The optimum null achievable will yield the highest CMRR over the amplifiers common mode range.



* NOTE: NOMINAL VALUE R1 TO ACHIEVE OPTIMUM CMRR IS 3.0 kΩ.

FIGURE 7. Improved V_{OS}, CMRR Nulling Circuit

AC CMRR Considerations

The ac CMRR may be improved using the circuit of Figure 8.

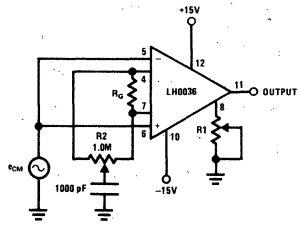


FIGURE 8. Improved AC CMRR Circuit

After adjusting R1 for best dc CMRR as before, R2 should be adjusted for minimum peak-to-peak voltage at the output while applying an ac common mode signal of the maximum amplitude and frequency of interest.

INPUT BIAS CURRENT CONTROL

Under nominal operating conditions (pin 3 grounded), the LH0036 requires input currents of 40 nA. The input current may be reduced by inserting a resistor (R_B) between 3 and ground or, alternatively, between 3 and V^-. For R_B returned to ground, the input bias current may be predicted by:

$$I_{BIAS} \cong \frac{V^+ - 0.5}{4 \times 10^8 + 800\ R_B} \qquad (6a)$$

or

$$R_B = \frac{V^+ - 0.5 - (4 \times 10^8)\ (I_{BIAS})}{800\ I_{BIAS}} \qquad (6b)$$

Where:

I_{BIAS} = Input Bias Current (nA)

R_B = External Resistor connected between pin 3 and ground (Ohms)

V^+ = Positive Supply Voltage (Volts)

Figure 9 is a plot of input bias current versus R_B.

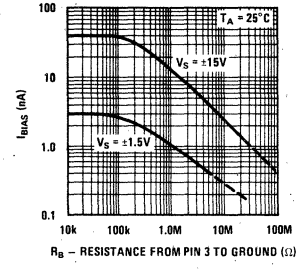


FIGURE 9. Input Bias Current as a Function of R_B

As indicated above, R_B may be returned to the negative supply voltage. Input bias current may then be predicted by:

$$I_{BIAS} \cong \frac{(V^+ - V^-) - 0.5}{4 \times 10^8 + 800\ R_B}$$

applications information (con't)

or

$$R_B \cong \frac{(V^+ - V^-) - 0.5 - (4 \times 10^8)(I_{BIAS})}{800\ I_{BIAS}} \quad (8)$$

Where:

I_{BIAS} = Input Bias Current (nA)

R_B = External resistor connected between pin 3 and V^- (Ohms)

V^+ = Positive Supply Voltage (Volts)

V^- = Negative Supply Voltage (Volts)

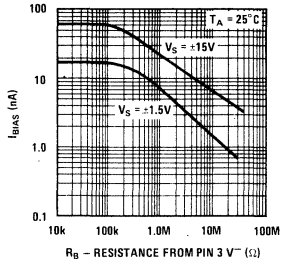


FIGURE 10. Input Bias Current as a Function of R_B

Figure 10 is a plot of input bias current versus R_B returned to V^- it should be noted that bandwidth is affected by changes in R_B. Figure 11 is a plot of bandwidth versus R_B.

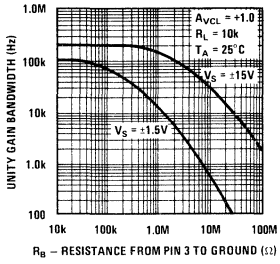


FIGURE 11. Unity Gain Bandwidth as a Function of R_B

BIAS CURRENT RETURN PATH CONSIDERATIONS

The LH0036 exhibits input bias currents typically in the 40 nA region in each input. This current must flow through R_{ISO} as shown in Figure 12.

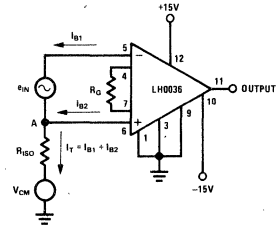


FIGURE 12. Bias Current Return Path

In a typical application, V_S = ±15V, $I_{B1} \cong I_{B2} \cong$ 40 nA, the total current, I_T, would flow through R_{ISO} causing a voltage rise at point A. For values of $R_{ISO} \geq 150$ MΩ, the voltage at point A exceeds the +12V common range of the device. Clearly, for $R_{ISO} = \infty$, the LH0036 would be driven to positive saturation.

The implication is that a finite impedance must be supplied between the input and power supply ground. The value of the resistor is dictated by the maximum input bias current, and the common mode voltage. Under worst case conditions:

$$R_{ISO} \leq \frac{V_{CMR} - V_{CM}}{I_T} \quad (9)$$

Where:

V_{CMR} = Common Mode Range (10V for the LH0036)

V_{CM} = Common Mode Voltage

$I_T = I_{B1} + I_{B2}$

In applications in which the signal source is floating, such as a thermocouple, one end of the source may be grounded directly or through a resistor.

GUARD OUTPUT

Pin 2 of the LH0036 is provided as a guard drive pin in those stringent applications which require very low leakage and minimum input capacitance. Pin 2 will always be biased at the input common mode voltage. The source impedance looking into pin 2 is approximately 15 kΩ. Proper use of the guard/shield pin is shown in Figure 13.

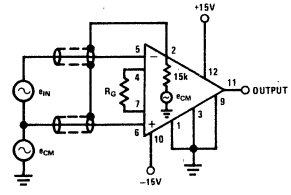


FIGURE 13. Use of Guard

For applications requiring a lower source impedance than 15 kΩ, a unity gain buffer, such as the LH0002 may be inserted between pin 2 and the input shields as shown in Figure 14.

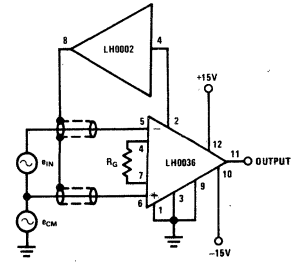


FIGURE 14. Guard Pin With Buffer

definition of terms

Bandwidth: The frequency at which the voltage gain is reduced to 0.707 of the low frequency (dc) value.

Closed Loop Gain, A_{VCL}: The ratio of the output voltage swing to the input voltage swing determined by $A_{VCL} = 1 + (50k/R_G)$. Where: R_G = Gain Set Resistor.

Common Mode Rejection Ratio: The ratio of input voltage range to the peak-to-peak change in offset voltage over this range.

Gain Equation Accuracy: The deviation of the actual closed loop gain from the predicted closed loop gain, $A_{VCL} = 1 + (50k/R_G)$ for the specified closed loop gain.

Input Bias Current: The current flowing at pin 5 and 6 under the specified operating conditions.

Input Offset Current: The difference between the input bias current at pins 5 and 6; i.e. $I_{OS} = |I_5 - I_6|$.

Input Stage Offset Voltage, V_{IOS}: The voltage which must be applied to the input pins to force the output to zero volts for $A_{VCL} = 100$.

Output Stage Offset Voltage, V_{OOS}: The voltage which must be applied to the input of the output stage to produce zero output voltage. It can be measured by measuring the overall offset at unity gain and subtracting V_{IOS}.

$$V_{OOS} = \left[V_{OS}\Big|_{A_{VCL}=1}\right] - \left[V_{OS}\Big|_{A_{VCL}=1000}\right]$$

Overall Offset Voltage:

$$V_{OS} = V_{IOS} + \frac{V_{OOS}}{A_{VCL}}$$

Power Supply Rejection Ratio: The ratio of the change in offset voltage, V_{OS}, to the change in supply voltage producing it.

Resistor, R_B: An optional resistor placed between pin 3 of the LH0036 and ground (or V^-) to reduce the input bias current.

Resistor, R_{BW}: An optional resistor placed between pin 1 of the LH0036 and ground (or V^-) to reduce the bandwidth of the output stage.

Resistor, R_G: A gain setting resistor connected between pins 4 and 7 of the LH0036 in order to program the gain from 1 to 1000.

Settling Time: The time between the initiation of an input step function and the time when the output voltage has settled to within a specified error band of the final output voltage.

NATIONAL

LH0037/LH0037C low cost instrumentation amplifier

general description

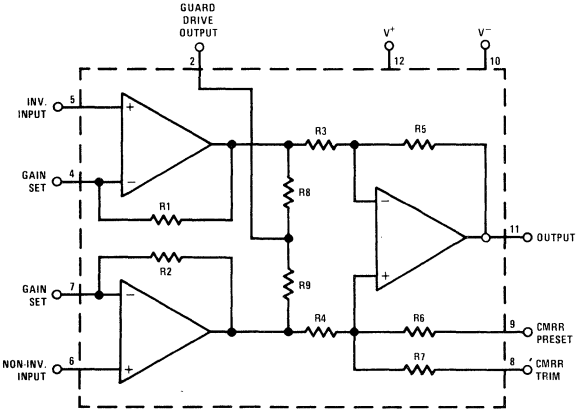
The LH0037/LH0037C is a true instrumentation amplifier designed for precision differential signal processing. Extremely high accuracy can be obtained due to the 300 MΩ input impedance and excellent 100 dB common-mode rejection ratio. It is packaged in a hermetic TO-8 package. Gain is programmable with one external resistor from 1 to 1000. Power supply operating range is between ±5V and ±22V.

The LH0037 is specified for operation over the −55°C to +125°C temperature range and the LH0037C is specified for operation over the −25°C to +85°C temperature range.

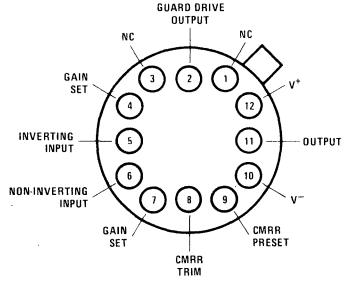
features

- High input impedance 300 MΩ
- High CMRR 100 dB
- Single resistor gain adjust 1 to 1000
- Low power 250 mW
- Wide supply range ±5V to ±22V
- Guard drive output

equivalent circuit and connection diagrams

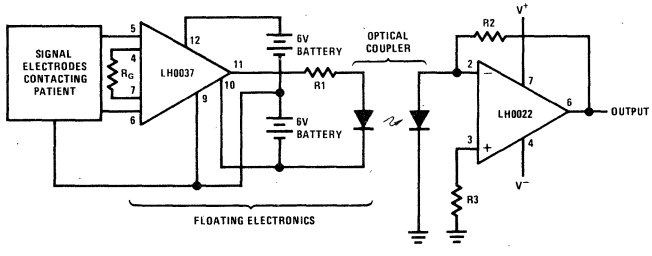


Metal Can Package



Order Number LH0037G or LH0037CG

typical applications



Isolation Amplifier for Medical Telemetry

absolute maximum ratings

Supply Voltage	±22V	Short Circuit Duration	Continuous
Differential Input Voltage	±30V	Operating Temperature Range	
Input Voltage Range	$\pm V_S$	LH0037	−55°C to +125°C
Shield Drive Voltage	$\pm V_S$	LH0037C	−25°C to +85°C
CMRR Preset Voltage	$\pm V_S$	Storage Temperature Range	−65°C to +150°C
CMRR Trim Voltage	$\pm V_S$	Lead Temperature (Soldering, 10 seconds)	300°C
Power Dissipation (Note 3)	1.5W		

electrical characteristics (Notes 1 and 2)

PARAMETER	CONDITIONS	LIMITS						UNITS
		LH0037			LH0037C			
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage (V_{IOS})	R_S = 1.0 kΩ, T_A = 25°C		0.5	1.0		1.0	2.0	mV
	R_S = 1.0 kΩ			2.0			3.0	mV
Output Offset Voltage (V_{OOS})	R_S = 1.0 kΩ, T_A = 25°C		2.0	5.0		5.0	10	mV
	R_S = 1.0 kΩ			6.0			12	mV
Input Offset Voltage Tempco ($\Delta V_{IOS}/\Delta T$)	$R_S \leq$ 1.0 kΩ		10			10		µV/°C
Output Offset Voltage Tempco ($\Delta V_{OOS}/\Delta T$)			15			15		µV/°C
Overall Offset Referred to Input (V_{OS})	A_V = 1.0		2.5			6.0		mV
	A_V = 10		0.7			1.5		mV
	A_V = 100		0.52			1.05		mV
	A_V = 1000		0.502			1.005		mV
Input Bias Current (I_B)	T_A = 25°C		200	500		200	500	nA
				1.5			0.8	µA
Input Offset Current (I_{OS})	T_A = 25°C			100			250	nA
Small Signal Bandwidth	A_V = 1.0, R_L = 2 kΩ		350			350		kHz
	A_V = 10, R_L = 2 kΩ		35			35		kHz
	A_V = 100, R_L = 2 kΩ		3.5			3.5		kHz
	A_V = 1000, R_L = 2 kΩ		350			350		Hz
Full Power Bandwidth	V_{IN} = ±10V, R_L = 2 kΩ A_V = 1		5.0			5.0		kHz
Input Voltage Range	Differential	±12			±12			V
	Common Mode	±12			±12			V
Gain Nonlinearity			0.03			0.03		%
Deviation From Gain Equation Formula	A_V = 1 to 1000		±0.3			±1.0		%
PSRR	±5.0V ≤ V_S ≤ ±15V, A_V = 1.0		1.0			1.0		mV/V
	±5.0V ≤ V_S ≤ ±15V, A_V = 100		0.05	0.25		0.10		mV/V
CMRR	A_V = 1.0 DC to		1.0	2.5		2.5	5.0	mV/V
	A_V = 10 100 Hz		0.1	0.25		0.25	1.0	mV/V
	A_V = 100 ΔR_S = 1.0k		25	100		25	100	µV/V
Output Voltage	R_L = 2 kΩ	12	14		12	14		V
	T_A = 25°C, R_L = 1 kΩ	10	13		10	13		V
Output Resistance			0.5			0.5		Ω
Supply Current			4.5	8.4		4.5	8.4	mA
Slew Rate	ΔV_{IN} = ±10V, R_L = 2 kΩ, A_V = 1.0		0.5			0.5		V/µs
Settling Time	To ±10 mV, R_L = 2 kΩ ΔV_{OUT} = 1.0V							
	A_V = 1.0		3.8			3.8		µs
	A_V = 100		180			180		µs

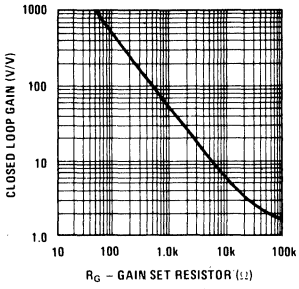
Note 1: Unless otherwise specified, all specifications apply for V_S = ±15V, pin 9 grounded, −25°C to +85°C for the LH0037C and −55°C to +125°C for the LH0037.

Note 2: All typical values are for T_A = 25°C.

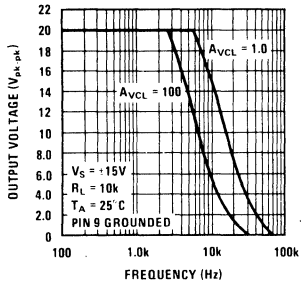
Note 3: The maximum junction temperature is 150°C. For operation at elevated temperature derate the G package on a thermal resistance of 90°C/W, above 25°C.

typical performance characteristics

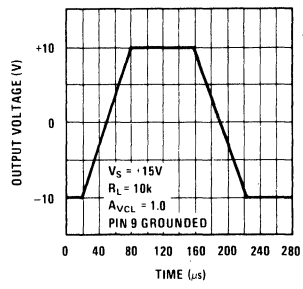
Closed Loop Voltage Gain



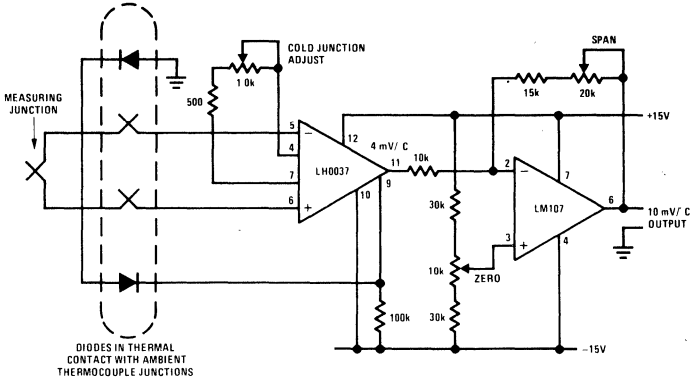
Output Voltage Swing vs Frequency



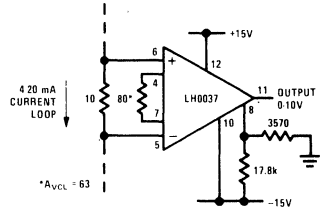
Large Signal Pulse Response



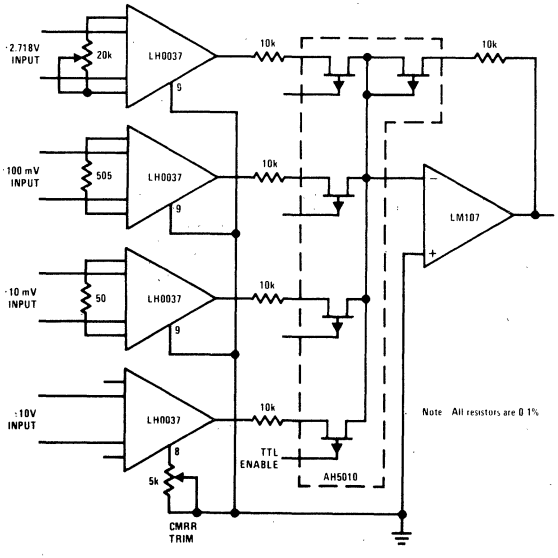
typical applications (con't)



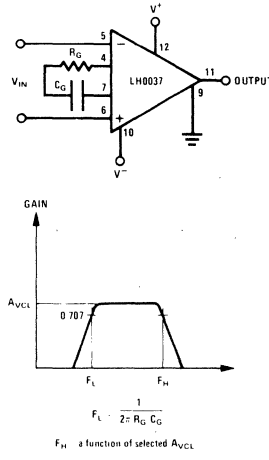
Thermocouple Amplifier with Cold Junction Compensation



Process Control Interface



Pre MUX Signal Conditioning



High Pass Filter

NATIONAL

LH0044 series precision low noise operational amplifiers

general description

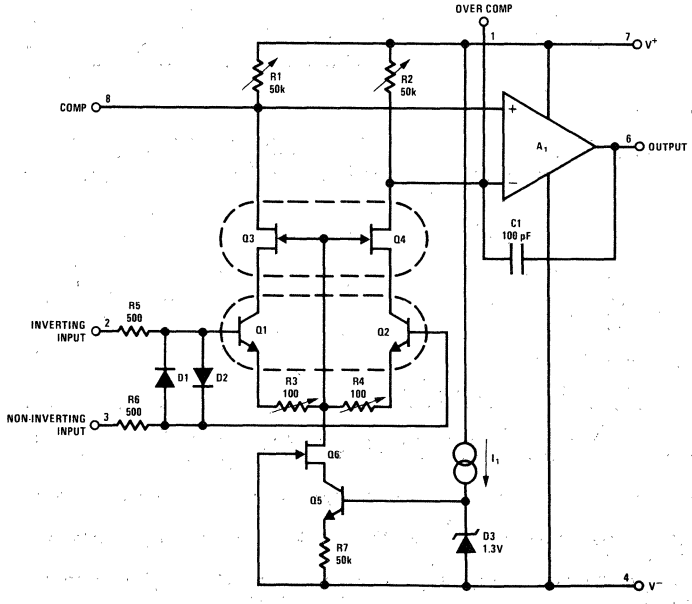
The LH0044 Series is a low noise, ultra-stable, high gain, precision operational amplifier family intended to replace either chopper-stabilized monolithic or modular amplifiers. The devices are particularly suited for differential mode, inverting, and non-inverting mode applications requiring very low initial offset, low offset drift, very high gain, high CMRR, and high PSRR. In addition, the LH0044 Series' low initial offset and offset drift eliminate costly and time consuming null adjustments at the systems level. The superior performance afforded by the LH0044 Series is made possible by advanced processing and testing techniques, as well as active laser trim of critical metal film resistors to minimize offset voltage and drift. Unique construction eliminates thermal feedback effects.

The LH0044 Series is an excellent choice for a wide range of precision applications including strain gauge bridges, thermocouple amplifiers, and ultrastable reference amplifiers. The LH0044 and LH0044A are guaranteed over the temperature range of −55°C to +125°C, and the LH0044AC, LH0044B, and LH0044C are guaranteed from −25°C to +85°C. The device is available in standard TO-5 op amp pin out and is compatible with LM108A, LM725, and LM741 type amplifiers.

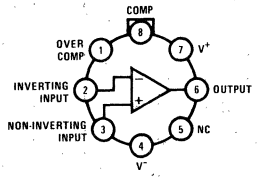
features

- Low input offset voltage 25μV max
- Excellent long-term stability ±1μV/month max
- Low offset drift 0.5μV/°C max
- Very low noise 0.7μVp-p max 0.1 Hz to 10 Hz
- High CMRR and PSRR 120 dB min
- High open loop gain 120 dB min
- Wide common-mode range ±13V min
- Wide supply voltage range ±2V to ±20V

equivalent circuit and connection diagram



Metal Can Package



TOP VIEW

Case is electrically isolated

Note: Compensation is not normally required. However, for maximum stability, a 0.01μF capacitor should be placed between pins 7 and 8 when device is used below closed loop gains of 10.

TO-5 Metal Can Package (H)

Order Number LH0044AH or LH0044H (-55°C to +125°C)

Order Number LH0044ACH, LH0044BH or LH0044CH (-25°C to +85°C)

See Package 9

absolute maximum ratings

Supply Voltage	±20V	Operating Temperature Range	
Power Dissipation	600 mW	LH0044, LH0044A	−55°C to +125°C
Differential Input Voltage (Note 4)	±15V	LH0044AC, LH0044B, LH0044C	−25°C to +85°C
Input Voltage (Note 5)	±15V	Storage Temperature Range	−65°C to +150°C
Output Short-Circuit Duration	Continuous	Lead Temperature (Soldering, 10 seconds)	300°C

dc electrical characteristics (Note 1)

PARAMETER	CONDITIONS	LIMITS						UNITS
		LH0044A/LH0044AC			LH0044/LH0044B/LH0044C			
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$T_A = 25°C$, $R_S = 50\Omega$, $V_{CM} = 0V$		8	25		12	50	μV
	LH0044C Only						100	μV
Input Offset Voltage	$R_S = 50\Omega$, $V_{CM} = 0V$			50			150	μV
	LH0044A and LH0044B Only			75			75	μV
Average Input Offset Voltage Drift	$T_{MIN} \leq T_A \leq T_{MAX}$		0.1	0.5		0.2	1.0	μV/°C
	LH0044B Only						0.5	μV/°C
Long-Term Stability	(Note 2)		0.2	1		0.3	2	μV/month
Input Noise Voltage (Note 3)	BW = 0.1 Hz to 10 Hz, $R_S = 50\Omega$		0.35	0.7		0.35	0.8	μVp-p
	R_S = 10 kΩ Imbalance		0.50	0.9		0.50	1.0	μVp-p
Thermal Feedback Coefficient			0.005			0.005		μV/mW
Open Loop Voltage Gain	R_L = 10 kΩ	120	145		114	140		dB
Common-Mode Rejection Ratio	$-10V \leq V_{CM} \leq +10V$	120	145		114	140		dB
Power Supply Rejection Ratio	$\pm 3V \leq V_S \leq \pm 18V$	120	145		114	140		dB
Input Voltage Range		±13	±13.8		±12	±13.5		V
Output Voltage Swing	R_L = 10 kΩ	±13	±13.7		±12	±13.5		V
Input Offset Current	$25°C \leq T_A \leq T_{MAX}$		1.0	2.5		1.5	5.0	nA
	$T_{MIN} \leq T_A < 25°C$			5.0			10.0	nA
Average Input Offset Current Drift			5	40		15	80	pA/°C
Input Bias Current	$25°C \leq T_A \leq T_{MAX}$		8.5	15		10	30	nA
	$T_{MIN} \leq T_A < 25°C$			50			100	nA
Average Input Bias Current Drift			50	300		100	600	pA/°C
Differential Input Impedance		5	10		2.5	8		MΩ
Common-Mode Input Impedance			2×10^{11}			2×10^{11}		Ω
Supply Current	$I_L = 0$		0.9	3.0		1.0	4.0	mA
Power Dissipation			27	90		30	120	mW

ac electrical characteristics $T_A = 25°C$, $V_S = \pm 15V$

PARAMETER	CONDITIONS	TYP	UNITS
Input Noise Voltage	R_S = 1 kΩ, f_O = 10 Hz	11	$nV/\sqrt{Hz}$
	R_S = 1 kΩ, f_O = 1 kHz	9	$nV/\sqrt{Hz}$
Slew Rate	$A_V = +1$, R_L = 10 kΩ, $V_{IN} = \pm 10V$	0.06	V/μs
Large Signal Bandwidth	$A_V = +1$, R_L = 10 kΩ, $V_{IN} = \pm 10V$	1	kHz
Overload Recovery Time	$A_V = +100$, $V_{IN} = -100$ mV, ΔV_{IN} = 200 mV	5	μs
Small Signal Bandwidth	$A_V = +1$, R_L = 10 kΩ	400	kHz
Small Signal Rise Time	$A_V = +1$, R_L = 10 kΩ, V_{IN} = 10 mV	2.5	μs
Overshoot	$A_V = +1$, R_L = 10 kΩ, V_{IN} = 10 mV, C_L = 100 pF	10	%

Note 1: All specifications apply for all device grades, at $V_S = \pm 15V$, and from T_{MIN} to T_{MAX} unless otherwise specified. T_{MIN} is −55°C and T_{MAX} is +125°C for the LH0044A and LH0044. T_{MIN} is −25°C and T_{MAX} is +85°C for the LH0044AC, LH0044B and LH0044C. Typicals are given for $T_A = 25°C$.

Note 2: This parameter is not 100% tested; however, 90% of the devices are guaranteed to meet this specification after one month of operation and after initial turn-on stabilization.

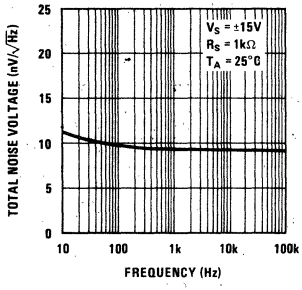
Note 3: Noise is 100% tested on the LH0044A, LH0044AC and LH0044B only. 90% of the LH0044 and LH0044C devices are guaranteed to meet this specification.

Note 4: The inputs are shunted by back-to-back diodes for over-voltage protection. Excessive current will flow for differential input voltages in excess of 1V. Input current should be limited to less than 1 mA.

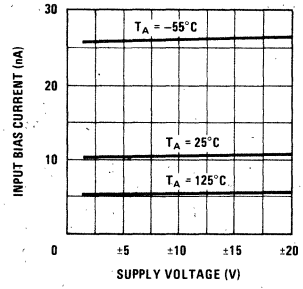
Note 5: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

typical performance characteristics

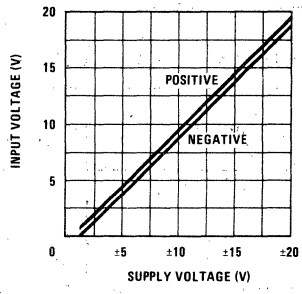
Total Input Noise Voltage vs Frequency



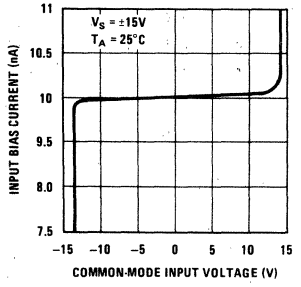
Input Bias Current



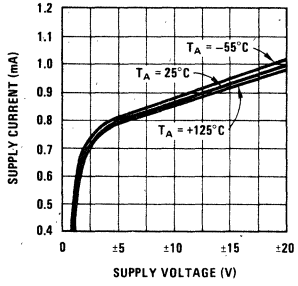
Input Voltage Range



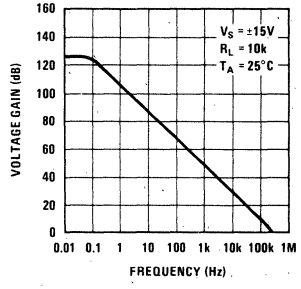
Input Bias Current vs Common-Mode Input Voltage



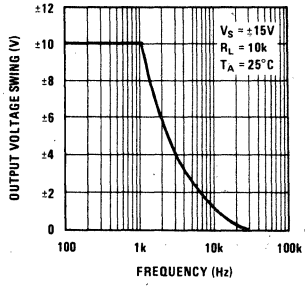
Supply Current vs Supply Voltage



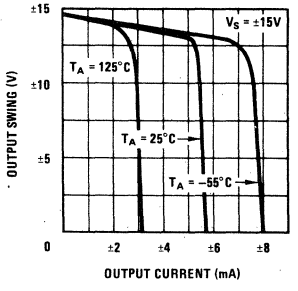
Open Loop Frequency Response



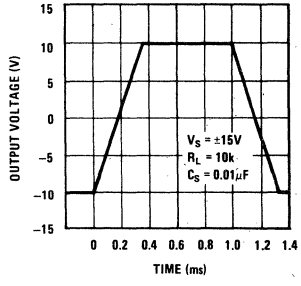
Large Signal Voltage Response



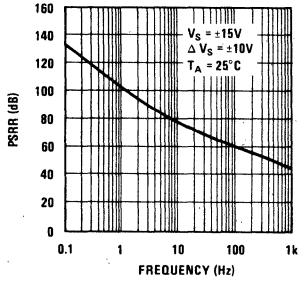
Output Swing



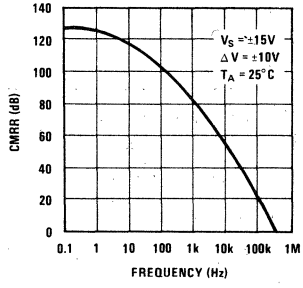
Large Signal Pulse Response



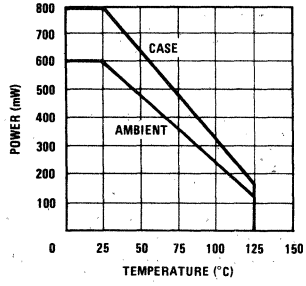
Power Supply Rejection Ratio vs Frequency



CMRR vs Frequency



Maximum Power Dissipation



applications information

LOW DRIFT CONSIDERATIONS

Achieving ultra-low drift in practical applications requires strict attention to board layout, thermocouple effects, and input guarding. For specific recommendations refer to AN-63 and AN-79.

A point worth stressing with regard to low drift specifications is testing of the LH0044. Simply stated—it is virtually impossible to test the device using a thermoprobe or other form of local heating. A one degree centigrade temperature gradient can account for tens of microvolts of virtual offset (or drift). The test circuit of *Figure 1* is recommended for use in a stabilized oven or continuously stirred oil bath with the entire circuit inside the oven or bath. Isothermal layout of the resistors is advised in order to minimize thermocouple induced EMF's.

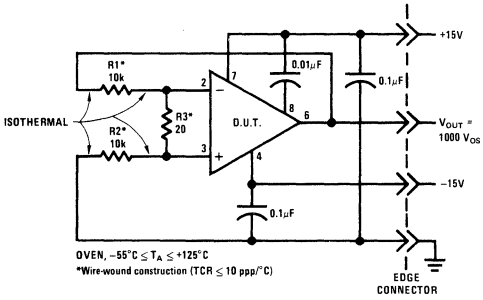


FIGURE 1. LH0044 Temperature Test Circuit

OVER COMPENSATION

The LH0044 may be overcompensated in order to minimize noise bandwidth by paralleling the internal 100 pF capacitor with an external capacitor connected between pins 1 and 6. Unity gain frequency may be predicted by:

$$f = \frac{4 \times 10^{-5}}{100\ pF + C_{ext}\ pF}\ (Hz)$$

COMPENSATION

For closed loop gains in excess of 10, no external components are required for frequency stability. However, for gains of 10 or less, a 0.01μF disc capacitor is recommended between pin 7 (V^+) and pin 8 (Comp). An improvement in ac PSRR will also be realized by use of the 0.01μF capacitor.

OFFSET NULL

In general, further nulling of LH0044 is neither necessary nor recommended. For most applications the specified initial offset is sufficient.

However, for those applications requiring additional null, an obvious temptation might be to place a pot between pins 1 and 8 with the wiper returned to V^+. This technique will usually result in reduced gain and increased offset drift due to mismatch in the TCR of the pot and R1 and R2. The technique is, therefore, not generally recommended.

The recommended technique for offset nulling the LH0044 is shown in *Figure 2.* Null is accomplished in A_2 and all errors are divided by the closed loop gain of the LH0044. Additional offset and drift incurred due to use of A_2 is less than 1μV/V for V^+ and V^- changes and 0.01μV/°C drift for the values shown in *Figure 2.*

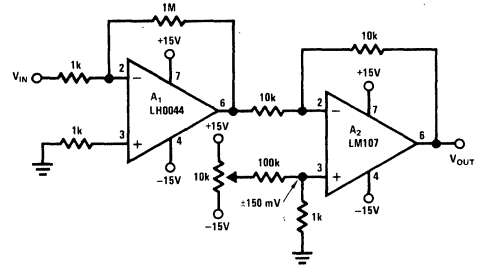
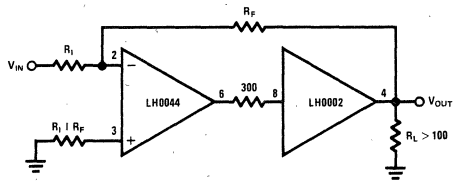
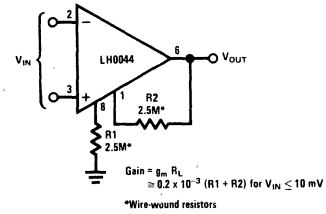


FIGURE 2. LH0044 Null Technique

typical applications

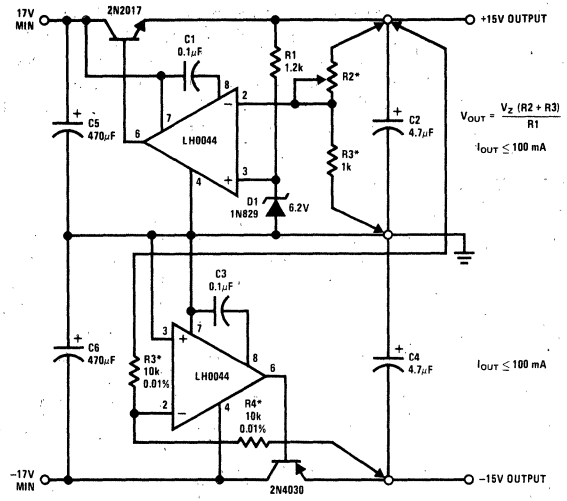


Buffered Output for Heavy Loads



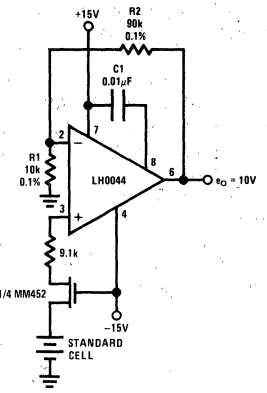
X1000 Instrumentation Amp

typical applications (con't)

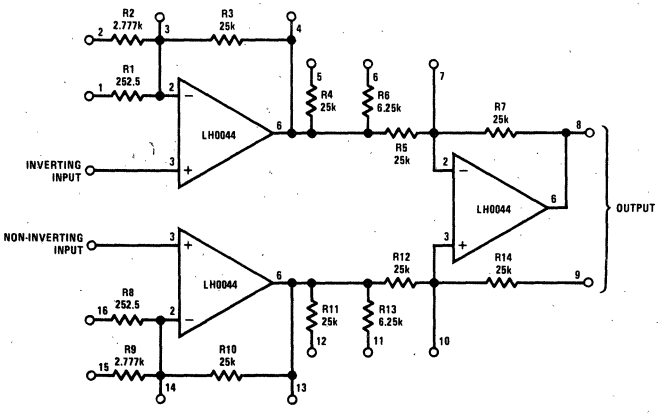


*Wire-wound for minimum drift.
Line and load regulation ≤ 0.005%

Precision Dual Tracking Regulator



10V Reference Supply

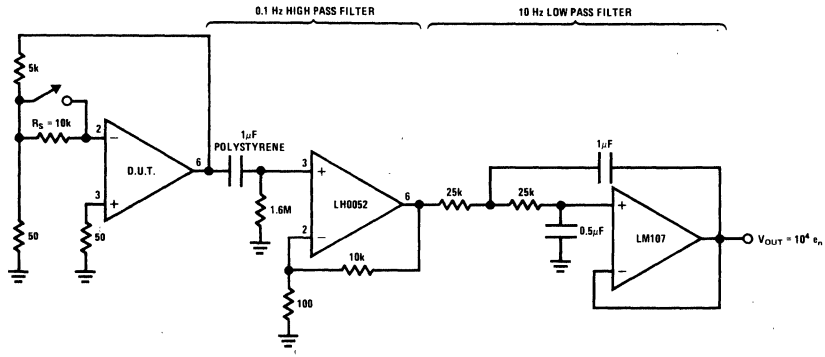


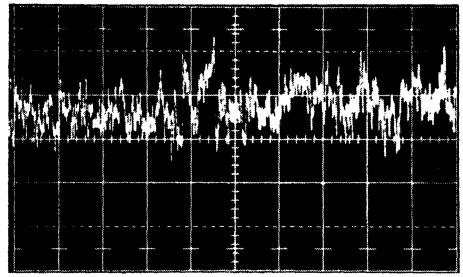
All resistors are part of National's RA201 resistor array.

OVERALL GAIN	INPUT STAGE GAIN	OUTPUT STAGE GAIN	JUMPER PINS ON RA201
X1	X1	X1	–
X2	X1	X2	5 to 7, 12 to 10
X5	X1	X5	6 to 7, 11 to 10
X10	X10	X1	2 to 15
X20	X10	X2	2 to 15, 5 to 7, 12 to 10
X50	X10	X5	2 to 15, 6 to 7, 11 to 10
X100	X100	X1	1 to 16
X200	X100	X2	1 to 16, 5 to 7, 12 to 10
X500	X100	X5	1 to 16, 6 to 7, 11 to 10
X995	X199	X5	1 to 14, 6 to 7, 11 to 10

Precision Instrumentation Amplifier

noise test circuit





VERT: 200 nV/DIV
HORIZ: 5 SEC/DIV

NATIONAL

LH0045/LH0045C two wire transmitter

general description

The LH0045/LH0045C Two Wire Transmitters are linear integrated circuits designed to convert the voltage from a sensor to a current, and send it through to a receiver, utilizing the same simple twisted pair as the supply voltage.

The LH0045 and LH0045C contain an internal reference designed to power the sensor bridge, a sensitive input amplifier, and an output current source. The output current scale can be adjusted to match the industry standards of 4.0 mA to 20 mA or 10 mA to 50 mA.

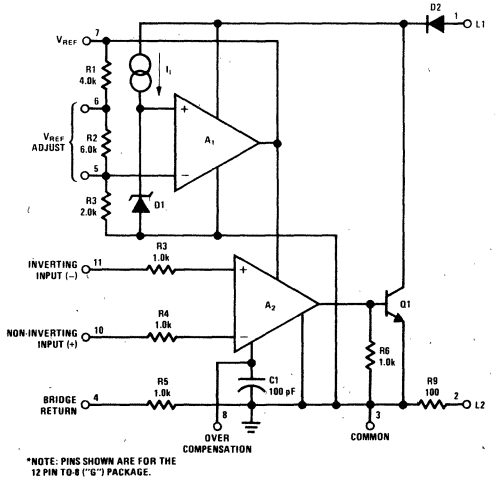
Designed for use with various sensors, the LH0045/LH0045C will interface with thermocouples, strain gauges, or thermistors. The use of the power supply leads as the signal output eliminates two or three extra wires in remote signal applications. Also, current output minimizes susceptibility to voltage noise spikes and eliminates line drop problems.

features

- High sensitivity — $> 10\ \mu A/\mu V$
- Low input offset voltage — 1.0 mV
- Low input bias current — 2.0 nA
- Single supply operation — 10V to 50V
- Programmable bridge reference (LH0045G) — 5.0V to 30V
- Non-interactive span and null adjust
- Over compensation capability
- Supply reversal protection

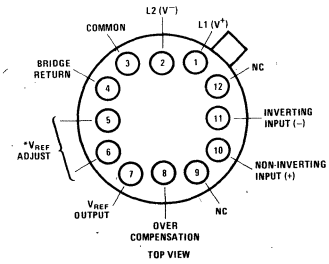
The LH0045/LH0045C is intended to fulfill a wide variety of process control, instrumentation, and data acquisition applications. The LH0045 is guaranteed over the temperature range of −55°C to +125°C; whereas the LH0045C is guaranteed from −25°C to +85°C.

equivalent schematic and connection diagrams



*NOTE: PINS SHOWN ARE FOR THE 12 PIN TO-8 ("G") PACKAGE.

TO-8

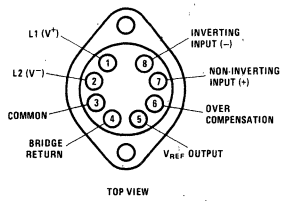


*NOTE: PIN 5 IS SHORTED TO PIN 6 TO OBTAIN A NOMINAL +5.1V, V_{REF}. LEFT OPEN V_{REF} = +10V.

THE CASE IS ISOLATED FROM THE CIRCUIT FOR BOTH TO-3 AND TO-8

Order Number LH0045G or LH0045CG
See Package 6

TO-3



Order Number LH0045K or LH0045CK
See Package 14

absolute maximum ratings

Supply Voltage (L1 to common)	+50V
Input Current	±20 mA
Input Voltage (Either Input to Common)	0V to V_{REF}
Differential Input Voltage	±20 V
Output Current (Either L1 or L2)	50 mA
Reference Output Current	5.0 mA
Power Dissipation	
LH0045G	1.5W
LH0045K	3.0W
Operating Temperature Range	
LH0045	−55°C to +125°C
LH0045C	−25°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

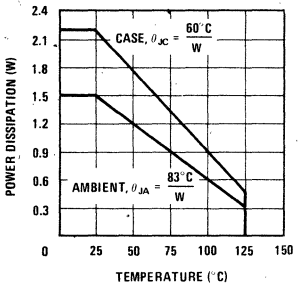
electrical characteristics (Note 1)

PARAMETER	CONDITIONS	LIMITS						UNITS
		LH0045			LH0045C			
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage (V_{OS})	I_S = 4.0 mA, T_A = 25°C		0.7	2.0		2.0	7.5	mV
	I_S = 4.0 mA			3.0			10	mV
Offset Voltage Temperature Coefficient ($\Delta V_{OS}/\Delta T$)	I_S = 4.0 mA		3.0			6.0		µV/°C
Input Bias Current (I_B)	T_A = 25°C		0.8	2.0		1.5	7.0	nA
				3.0			10	nA
Input Offset Current (I_{OS})	T_A = 25°C		0.05	0.2		0.2	1.0	nA
				0.4			1.5	nA
Open Loop Transconductance (g_{MOL})	ΔI_S = 4.0 mA to 20 mA	10^6	10^7		10^6	10^7		µ℧
	ΔI_S = 10 mA to 50 mA	$2x10^6$	$2x10^7$		$2x10^6$	$2x10^7$		µ℧
Supply Voltage Range (V_S)		9.0		50	9.0		50	V
	LH0045G pins 5 and 6 open	15		50	15		50	V
Input Voltage Range (V_{IN})		1.0		3.3	1.0		3.3	V
	LH0045G pins 5 and 6 open	1.0		7.6	1.0		7.6	V
Open Loop Output Impedance (R_{OUT})	V_S = 10V to 45V, I_S = 4.0 mA, T_A = 25°C		1.0			1.0		MΩ
Common Mode Rejection Ratio (CMRR)	ΔV_{IN} = 1.0V to 3.3V, I_S = 12 mA	0.1	0.05		0.1	0.05		mV/V
Power Supply Rejection Ratio (PSRR)	ΔV_S = 10V to 45V, I_S = 12 mA	0.1	0.01		0.1	0.01		mV/V
Open Loop Supply Current (I_{SOL})	V_S = 50V		2.0	3.0		2.0	3.0	mA
Reference Voltage Load Regulation ($\Delta V_{REF}/\Delta I_{REF}$)	ΔI_{REF} = 0 mA to 2.0 mA, T_A = 25°C		0.05	0.2		0.05	0.2	%
Reference Voltage Line Regulation ($\Delta V_{REF}/\Delta V_S$)	ΔV_S = 10V to 45V, T_A = 25°C		0.3	0.5		0.3	0.5	mV/V
Reference Voltage Temperature Coefficient ($\Delta V_{REF}/\Delta T$)	I_{REF} = 2.0 mA		0.004			0.004		%/°C
Reference Voltage (V_{REF})	I_{REF} = 2.0 mA, T_A = 25°C	4.3	5.1	5.9	4.3	5.1	5.9	V
	I_{REF} = 2.0 mA, T_A = 25°C, LH0045G pins 5 and 6 open	8.6	10.3	12	8.6	10.3	12	V
Resistor R9	I_S = 12 mA, T_A = 25°C	95	100	105	95	100	105	Ω
Average Temperature Coefficient of R9 (TCR_9)	I_S = 12 mA		50	300		50	300	PPM/°C
Resistor R5	I_S = 1.0 mA, T_A = 25°C	950	1000	1050	950	1000	1050	Ω
Average Temperature Coefficient of R5 (TCR_5)	I_S = 1.0 mA		50	300		50	300	PPM/°C
Input Resistance (R_{IN})	T_A = 25°C		50			50		MΩ

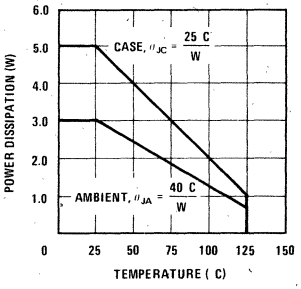
Note 1: Unless otherwise specified, these specifications apply for +10V ≤ V_S ≤ +50V, pin 5 shorted to pin 6 on the LH0045G, over the temperature range −55°C to +125°C for the LH0045 and −25°C to +85°C for the LH0045C.

typical performance characteristics

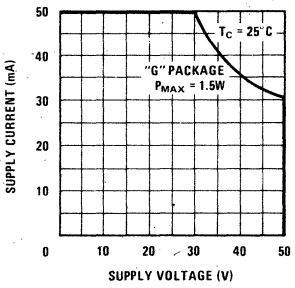
LH0045G Maximum Power Dissipation



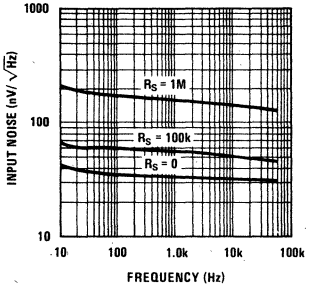
LH0045K Maximum Power Dissipation



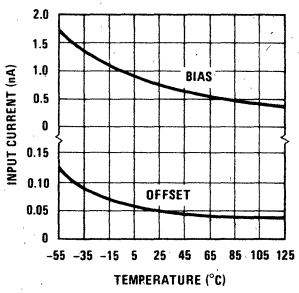
Safe Operating Area



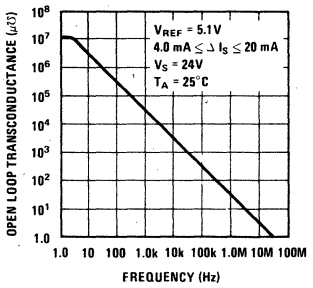
Input Noise Voltage



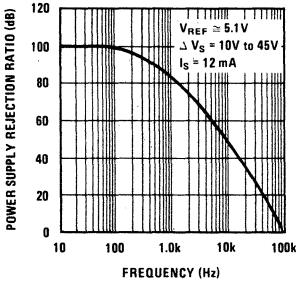
Input Currents



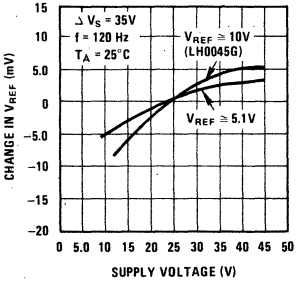
Open Loop Transconductance vs Frequency



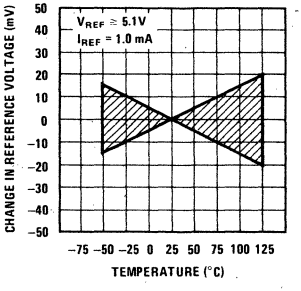
Power Supply Rejection Ratio vs Frequency



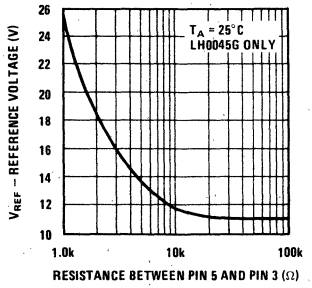
V_{REF} Line Regulation



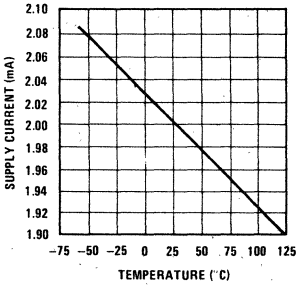
Variation of V_{REF} With Temperature Normalized to 25°C



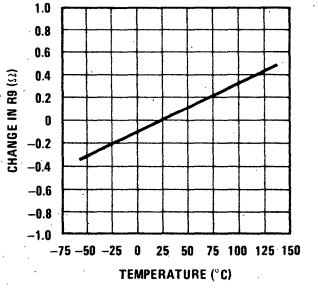
V_{REF} vs Resistance Between Pin 5 and Pin 3



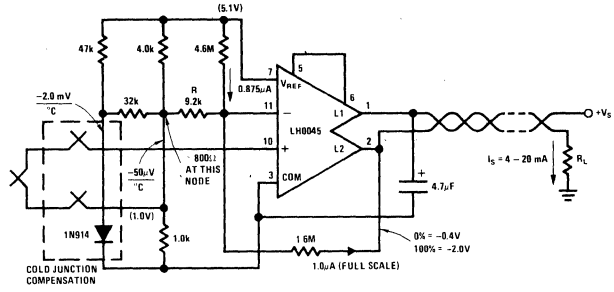
Open Loop Supply Current vs Temperature



Change in R9 With Temperature Normalized to 25°C

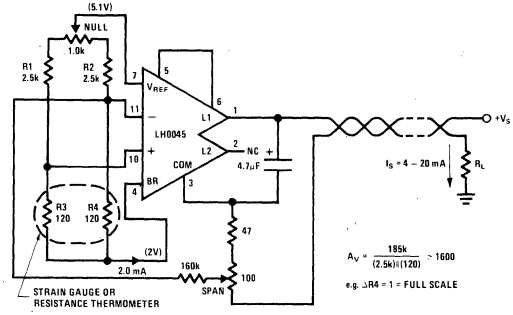


typical applications*

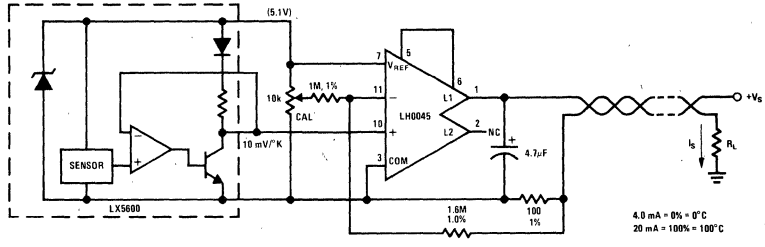


FOR 1μA FULL SCALE, $R_{IN} = V_{IN}/1\mu A$ = SOURCE IMPEDANCE @ PIN 11
e.g., V_{IN} (FULL SCALE) = 10 mV, R_{IN} = 10k
BRIDGE IMPEDANCE = 0.8k, R = 10k − 0.8k = 9.2k

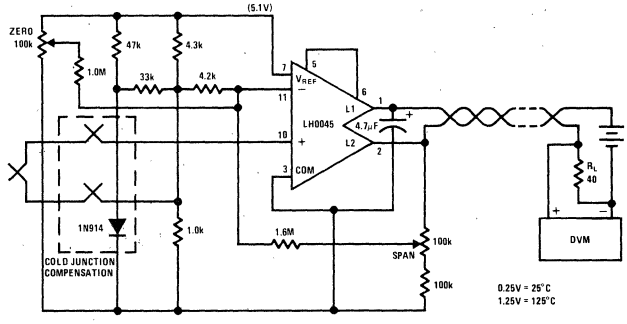
Thermocouple Input Transmitter



Resistance Bridge Input Transmitter

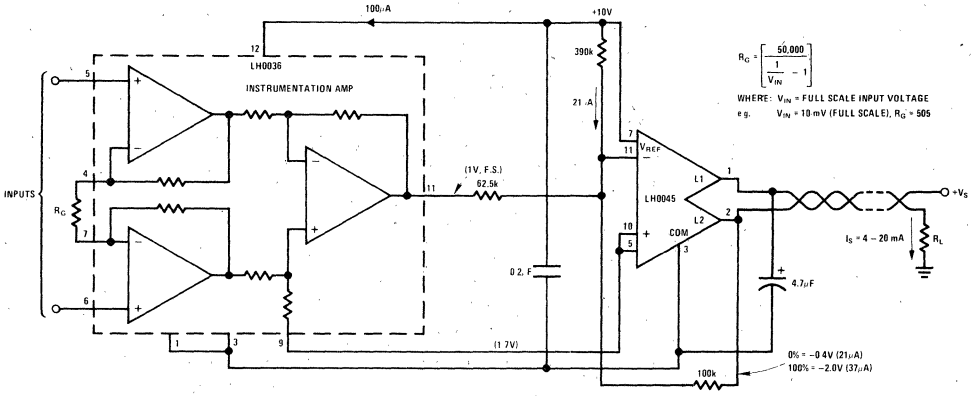


Electronic Temperature Sensor



*Pin numbers refer to 'G' package. All voltages indicated by ( ) are measured with respect to common, pin 3.

typical applications*(con't)



*Pin numbers refer to 'G' package. All voltages indicated by ( ) are measured with respect to common, pin 3.

Instrumentation Amplifier Transmitter

applications information

CIRCUIT DESCRIPTION AND OPERATION

A simplified schematic of the LH0045/LH0045C is shown in Figure 1. Differential amplifier, A_2 converts very low level signals to an output current via transistor Q1. Reference voltage diode D1 is used to supply voltage for operation of A_2 and to bias an external bridge. Current source I_1 minimizes fluctuation in the bridge reference voltage due to changes in V_S.

In normal operation, the LH0045/LH0045C is used in conjunction with an external bridge comprised of R_{B1} through R_{B4}. The bridge resistors in conjunction with bridge return resistor, R5, bias A_2 in its linear region and sense the input signal; e.g. R_{B4} might be a strain sensitive resistor in a strain gauge bridge. R_T is adjusted to purposely unbalance the bridge for 4.0 mA output (null) for zero signal input. This is accomplished by forcing 2.5μA more through R_{B3} than R_{B4}.

The 2.5μA imbalance causes a voltage rise of (2.5μA) x (100Ω) or 250μV at the top of R_{B3}. Terminal L2 may be viewed as the output of an op amp whose closed loop gain is approximately R_F/R_{B3} = 1600.

The 250μV rise at the top of R_{B3} causes a voltage drop of (1600) x (250μV) or −0.4V across R9. An output current, I_S, equal to 0.4V/R9 or 4.0 mA is thus established in Q1. If R_{B4} is now decreased by 1.0Ω (due to application of a strain force), a −1.0 mV change in input voltage will result. This causes L2 to drop to −2.0V. The output current would then be 2.0V/100Ω or 20 mA (Full Scale). If R_{B3} is a resistor of the same material as R_{B4} but not subjected to the strain, temperature drift effects will be equal in the two legs and will cancel.

In actual practice the loading effects of R_{B2} on the gain (span) and R_F on output current must be taken into account.

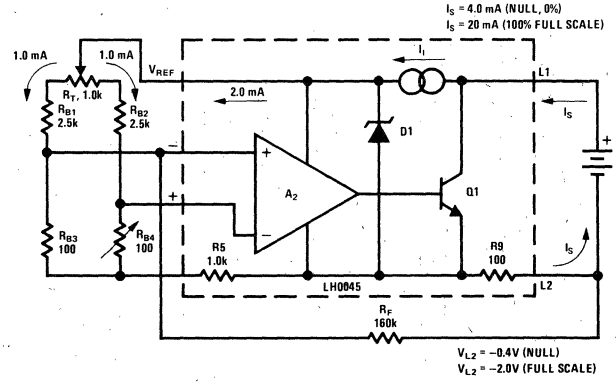


FIGURE 1. LH0045 Simplified Schematic

applications information (con't)

THERMAL CONSIDERATIONS

The power output transistor of the LH0045 is thermally isolated from the signal amplifier, A_2. Nevertheless, a change in the power dissipation will cause a change in the temperature of the package and thus may cause amplifier drift. These temperature excursions may be minimized by careful heat sinking to hold the case temperature equal to the ambient. With the TO-8 (G) package this is best accomplished by a clip-on heat sink such as the Thermalloy #2240A or the Wakefield #215-CB. The 8 lead TO-3 is particularly convenient for heat sinking, in that it may be bolted directly to many commercial aluminum heat sink extrusions, or to the chassis. In both packages the case is electrically isolated from the circuit.

In addition, the power change can be minimized by operating the device from relatively high supply voltages in series with a relatively high load resistance. When the signal forces the supply current higher, the voltage across the device will be reduced and the internal power dissipation kept nearly equal to the low current, high voltage condition.

For example, take the case of a 4.0 mA to 20 mA transmitter with a 24V supply and a 100Ω load resistance. The power at 4.0 mA is (23.6V) x (4.0 mA) = 94.4 mW while at full scale the power is (22V) x (20 mA) = 440 mW. The net change in power is 345 mW. This change in power will cause a change in temperature and thus a change in offset voltage of A_2.

If the optimum load resistance of 800Ω (from Figure 2) is used, the power at null is [24V − (4.0 mA) x (800Ω)] (4.0 mA) = 83 mW. The power at full scale is [24V − (20 mA) x (800Ω)] (20 mA) = 160 mW. The net change is 77 mW. This change is significantly less than without the resistor.

If the supply voltage is increased to 48V and the load resistance chosen to be the optimum value from Figure 2 (1.95k), then the power at null is [48V − (4.0 mA) x (1.95k)] (4.0 mA) = 160.8 mW and the power at full scale is [48 − (20) x (1.95k)] (20 mA) = 180 mW for a net change of 19.2 mW.

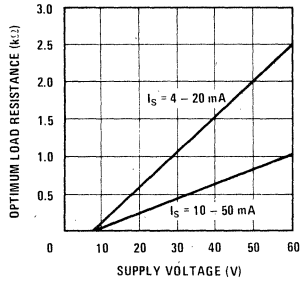


FIGURE 2. Optimum Load Resistance vs Supply Voltage

Note that the optimized load resistance is actually the sum of the line resistance, receiver resistances and added external load resistance. However, in many applications the line resistance and receiver resistances are negligible compared to the added external load resistance and thus may be omitted in calculations.

AUXILIARY PINS

The LH0045 has several auxiliary pins designed to provide the user with enhanced flexibility and performance. The following is a discussion of possible uses for these pins.

Programmable V_{REF} — Pins 5 and 6 (LH0045G Only)

The LH0045G provides pins 5 and 6 to allow the user to program the value of the reference voltage. The factory trimmed 10V value is obtained by leaving 5 and 6 open. A short between 5 and 6 will program the reference to a nominal 5.1V (equivalent to the fixed value used in the LH0045K).

A resistor or pot may be placed between pin 5 and common (pin 3) to obtain reference voltages between 10V and 30V or between pin 5 and pin 7 for reference voltages below 10V. Increased reference voltage might be useful to extend the positive common mode range or to accommodate transducers requiring higher supply voltage. A plot of resistance between pin 5 and pin 3 versus V_{REF} is given in the typical electrical characteristics section. V_{REF} may be adjusted about its nominal value by arranging a pot from V_{REF} to common and feeding a resistor from the wiper into pin 5 so that it may either inject or extract current. Lastly, pin 5 may be used as a nominal 1.7V reference point, if care is taken not to unduly load it with either dc current or capacitance. Obviously, higher supply voltages must be used to obtain the higher reference values. The minimum supply voltage to reference voltage differential is about 4.0V.

Bridge Return

An applications resistor is provided in the LH0045 with a nominal value of 1.0 kΩ. The primary application for the resistor is to maintain the minimum common mode input voltage (1.0V) required by the signal amplifier, A_2. A typical input application might utilize a strain gauge or thermistor bridge where the resistance of the sensor is 100Ω. Since only 1.0 mA may be drawn from V_{REF}, the 1.0 kΩ bridge return resistor is used to bias A_2 in its linear region as shown in Figure 3.

applications information (con't)

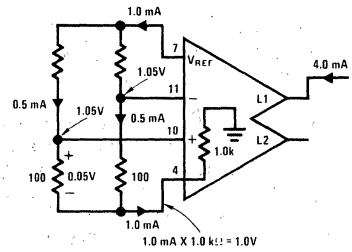


FIGURE 3. Use of Bridge Return

Over Compensation — Pin 8 (LH0045G), Pin 6 (LH0045K)

Over compensation of the signal amplifier, A_2 may be desirable in dc applications where the noise-bandwidth must be minimized. A capacitor should be placed between pin 8 (pin 6 on the LH0045K) and pin 3, common.

Typically,

$$f_{3db} = \frac{1}{2\pi R (C_1 + C_{EXT})}$$

where:

R = 400 MΩ

C1 = Internal Compensation Capacitor = 100 pF

C_{EXT} = External (over-compensation) Capacitor

Input Guard — Pins 9 and 12 (LH0045G)

Pins 9 and 12 have no internal connection whatever and thus need not be used. In some critical low current applications there may be an advantage to running a guard conductor between the inputs and the adjacent pins to intercept stray leakage currents. Pins 9 and 12 may be connected to this guard to simplify the PC board layout and allow the guard to continue under the device. (See AN-63 for further discussion of guarding techniques.)

NULL AND SPAN ADJUSTMENTS

Most applications of the LH0045 will require potentiometers to trim the initial tolerances of the sensor, the external resistors and the LH0045 itself. The preferred adjustment procedure is to stimulate the sensor, alternating between two known values, such as zero and full scale. The span and null are adjusted by monitoring the output current on a chart recorder, meter, or oscilloscope. A full scale stimulus is applied to the sensor and the span potentiometer adjusted for the desired full scale. Then, to adjust the null, apply a zero percent signal to the sensor and adjust the null potentiometer for the desired zero percent current indication.

If it is impractical to cycle the sensor during the calibration procedure, the signal may be simulated electrically with two cautions: 1) the calibration signal must be floating and 2) the calibration thus achieved does not account for sensor inaccuracies and/or errors in the signal generator.

SENSOR SELECTION

Generally it is easiest to use an insulated sensor. If it is necessary to use a grounded sensor, the power supply must be isolated from chassis ground to avoid extraneous circulating currents.

DESIGN EXAMPLE

There are numerous circuit configurations that may be utilized with the LH0045. The following is intended as a general design example which may be extended to specific cases.

Circuit Requirements

Output Characteristics

a. 0% = 4.0 mA (NULL)

b. 100% = 20 mA (SPAN = 16 mA)

c. Supply Voltage = 24V

Input (Sensor) Characteristics

a. V_{IN} = 100 mV (Full Scale)

b. V_{IN} = 0 mV (Zero Scale)

c. Source Impedance $\leq$ 1.0Ω

General Characteristics

a. 0°C $\leq T_A \leq$ +75°C

b. Overall Accuracy $\leq$ 0.5%

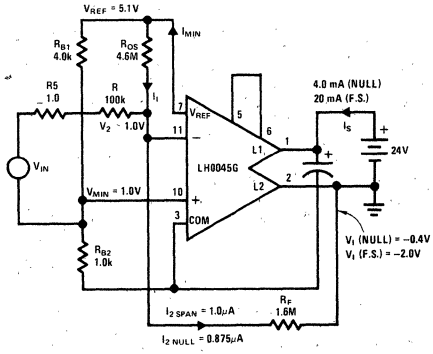


FIGURE 4. Design Example Circuit

Selection of R_F

Input bias current to the LH0045C is guaranteed less than 10 nA. Furthermore, the change in I_B over the temperature range of interest is typically under 1.0 nA. If $I_{2\ SPAN}$ is selected to be 1.0μA (1000 Δ I_B) errors due to Δ I_B/Δ T will be less than 0.1%. For SPAN = 16 mA.

$$V_{SPAN} = \Delta V_1 = -(16\,mA)(R9) = -1.6V$$

applications information (con't)

where R9 = Internal Current Set Resistor = 100Ω
For $I_{2\ SPAN}$ = 1.0μA,

$$R_F = \frac{V_{SPAN}}{I_{2\ SPAN}} = \frac{-1.6V}{1.0\mu A} = 1.6M$$

$$R_F = 1.6\ M\Omega$$

Selection of R_{B1} and R_{B2}

The minimum input common mode voltage, V_{MIN} required at the pin 10 input of A_2 is 1.0V. Furthermore, the maximum open loop supply current (I_{SOL}) drawn by the LH0045 is 3.0 mA. That leaves I_{MIN} = 4.0 mA − 3.0 mA = 1.0 mA left to bias the bridge at null. Hence:

$$R_{B2} \geqq \frac{V_{MIN}}{I_{MIN}} = \frac{1.0V}{1.0\ mA} = 1.0\ k\Omega$$

And,

$$\frac{V_{REF}\ R_{B2}}{R_{B1} + R_{B2}} = 1.0V$$

$$R_{B1} = R_{B2}\ \frac{V_{REF} - 1.0V}{1.0V}$$

$$= 1.0k\ (5.1 - 1.0)$$

$$R_{B1} \cong 4.0\ k\Omega$$

Alternatively, an LM113, 1.22V reference diode, or an op amp such as the LM108 may be used to bias the signal amplifier, A_2 as shown in Figure 5. These techniques have the advantage of lowering the impedance seen at pin 10.

Selection of R_{OS}

R_{OS} is selected to provide the null current of 4.0 mA, $V_{1\ NULL}$ = 4.0 mA x 100Ω = 0.4V. From previous calculations we know that V_{MIN} = 1.0V. The voltage pin 11, V_2 is:

$$V_2 = V_{MIN} + V_{OS} \cong V_{MIN}$$

for V_{IN} = 0V

Hence, the current required to generate the null voltage, $I_{2\ NULL}$ is:

$$I_{2\ NULL} = \frac{V_{MIN} - V_{1\ NULL}}{R_F}$$

$$= \frac{1.0V - (-0.4V)}{1.6\ M\Omega} = 0.875\mu A$$

This current must be provided by R_{OS} from V_{REF}; hence:

$$R_{OS} = \frac{V_{REF} - V_{MIN}}{I_{2\ NULL}}$$

The nominal value for V_{REF} is 5.1V, therefore the nominal value for R_{OS} is:

$$\frac{5.1V - 1.0V}{0.875\mu A} \quad \text{or}$$

$$R_{OS} = 4.6\ M\Omega$$

It should be noted however, that the variation of V_{REF} may be as high as 5.9V or as low as 4.3V. Furthermore, the tolerances of R9 (100Ω), R_{B1}. R_{B2}, and the input V_{OS} of A_2 would predict values for R_{OS} as low as 3.98M and as high as 5.43M. The implication is that in the specific case, R_{OS} should be implemented with a pot, of appropriate value, in order to accommodate the tolerances of V_{REF}, R9, V_{OS}, R_{B1}, R_{B2}, etc.

Selection of R

SPAN is required to be 16 mA. From feedback theory and the gain equation we know:

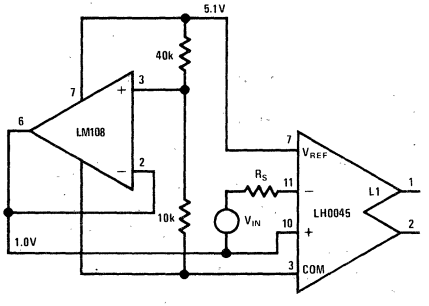
$$I_{SPAN} = V_{IN}\ \frac{R_F}{R}\ x\ \frac{1}{R9}$$

where:

R = total impedance in signal path between pin 10 and pin 11

R9 = Current setting resistor = 100Ω

V_{IN} = Full scale input voltage = 100 mV



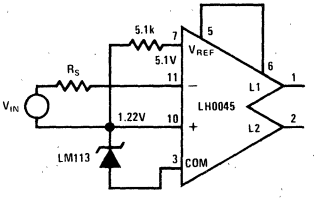


FIGURE 5. Alternate Biasing Techniques

applications information (con't)

$$\therefore R = \frac{(V_{IN})\,(R_F)}{(I_{SPAN})\,(R9)}$$

$$R = \frac{(100\ mV)\,(1.6\ M\Omega)}{(16\ mA)\,(100\Omega)}$$

$$R = 100\ k\Omega$$

As before, uncertainties in device parameters might dictate that R_F be made a pot of appropriate value.

Summary of the Steps to Determine External Resistor Values

1. Select $I_{FULL\ SCALE} = I_{NULL} + I_{SPAN}$ for the desired application. (I_{NULL} is frequently 4.0 mA and $I_{FULL\ SCALE}$ is frequently 20 mA.)

2. Select $I_{2\ SPAN}$ so that it is large compared to ΔI_B. 1000 ΔI_B is a good value.

3. Determine $V_{SPAN} = \Delta V_2 = (I_{SPAN})(R9)$.

4. Determine $R_F = (V_{SPAN}/I_{2\ SPAN})$

5. Select

$$R_{B2} \geq \frac{V_{MIN}}{I_{MIN}}$$

$$R_{B2} \geq \frac{1\ VOLT}{I_{NULL} - I_{SOL}}$$

Where:

V_{MIN} = minimum common mode input voltage

I_{MIN} = minimum available bridge current

I_{SOL} = maximum open loop supply current

6. Determine

$$R_{B1} = R_{B2}\,\frac{V_{REF} - V_{MIN}}{V_{MIN}}$$

7. Determine $V_{2\ NULL} = I_{NULL}\ R9$

8. Determine

$$I_{2\ NULL} = \frac{V_{MIN} - V_{2\ NULL}}{R_F}$$

9. Determine

$$R_{OS} = \frac{V_{REF} - V_{MIN}}{I_{2\,NULL}}$$

10. Determine

$$R = \frac{(V_{IN})\,(R_F)}{(I_{SPAN})\,(R9)}$$

Where:

V_{IN} = Sensor full scale output voltage

ERROR BUDGET ANALYSIS

Errors Due to Change in V_{REF} (ΔV_{REF})

There are several factors which could cause a change in V_{REF}. First, as the ambient temperature changes, a V_{REF} drift of ±0.2 mV/°C might be expected. Secondly, supply voltage variations could cause a 0.5 mV/V change in V_{REF}. Lastly, self-heating due to power dissipation variations can cause drift of the reference.

An overall expression for change in V_{REF} is:

$$\Delta V_{REF} = \underbrace{[(\theta)(\Delta P_{DISS}) + \Delta T_A]\,\frac{\Delta V_{REF}}{\Delta T}}_{\text{Thermal Effects}} + \underbrace{\frac{\Delta V_{REF}}{\Delta V_S}\,(\Delta V_S)}_{\text{Supply Voltage Effects}}$$

Where:

θ = Thermal resistance, either junction-to-ambient to junction to case

ΔP_{DISS} = Change in avg. power dissipation

ΔT_A = Change in ambient temperature

$\frac{\Delta V_{REF}}{\Delta T}$ = Reference voltage drift (in mV/°C)

$\frac{\Delta V_{REF}}{\Delta V_S}$ = Line regulation of V_{REF}

Several steps may be taken to minimize the bracketed terms in the equation above. For example, operating the LH0045G with a heat-sink reduces the thermal resistance from $\theta_{JA} = 83°C/W$ to $\theta_{JC} = 60°C/W$. For the LH0045K (TO-3) $\theta_{JA} = 40°C/W$ may be reduced to $\theta_{JC} = 25°C/W$ by using a heat sink. The ΔP_{DISS} term may be significantly reduced using the power minimization technique described under "Thermal Considerations." For the design example, ΔP_{DISS} is reduced from 384 mW to 77 mW ($R_L = 800\Omega$.) Evaluating the LH0045G with a heat-sink and $R_L = 800\Omega$ yields.

$$\Delta V_{REF} = \left(\frac{60°C}{W}\ (0.077W) + 75°C\right)\left(\frac{0.2\ mV}{°C}\right) + \frac{0.5\ mV}{V}\ (16V)$$

$$\Delta V_{REF} = 24\ mV$$

The LH0045K (TO-3) under the same operating conditions would exhibit a $\Delta V_{REF} \cong 23$ mV.

applications information (con't)

An expression for error in the output current due to ΔV_{REF} is:

$$\frac{\Delta I_S}{I_{SPAN}} (\%) = 100 \frac{(K)(R_{OS})(\Delta V_{REF}) - (1-K)(\Delta V_{REF})(R_F)}{(R9)(R_{OS})(I_{SPAN})}$$

Where:

ΔV_{REF} = Total change in V_{REF}

$$K = \frac{R_{B2}}{R_{B1} + R_{B2}}$$

R9 = Current set resistor

I_{SPAN} = Change in output current from 0% to 100%

For example, ΔV_{REF} = 24 mV, K = 0.2, R9 = 100Ω, I_{SPAN} = 16 mA. Hence, a 0.12% worst case error might be expected in output currents due to ΔV_{REF} effects.

Error Due to V_{OS} Drift

One of the primary causes of error in I_S is caused by V_{OS} drift. Drift may be induced either by self heating of the device or ambient temperature changes. The input offset voltage drift, $\Delta V_{OS}/\Delta T$, is nominally 3.3μV/°C per millivolt of initial offset. An expression for the total temperature dependent drift is:

$$\Delta V_{OS} = [(\theta)(\Delta P_{DISS}) + \Delta T_A] \frac{\Delta V_{OS}}{\Delta T}$$

Where:

θ = Thermal resistance either junction-to-ambient or junction-to-case

ΔP_{DISS} = Change in average power dissipation

ΔT_A = Change in ambient temperature

The bracketed term may be minimized by heat sinking and using the power minimization technique described under "Thermal Considerations." For the LH0045G design example, ΔV_{OS} = 0.352 mV under ambient conditions and 0.263 mV using a heat-sink and R_L = 800Ω. Comparable V_{OS} for the LH0045K would be 0.254 mV.

The error in output current due to ΔV_{OS} is:

$$\frac{\Delta I_S}{I_{SPAN}} (\text{in } \%) = 100 \times \frac{\Delta V_{OS}}{V_{IN\ (FULL\ SCALE)}}$$

$$= 100 \times \frac{R_F}{(R)(R9)(I_{SPAN})}$$

For the design example, ΔV_{OS} = 0.263 mV, V_{IN} (Full Scale) = 100 mV. Hence, 0.26 mV ÷ 100 mV or 0.26% worst case error could be expected in output current effects.

Errors Due to Changes in R9

The temperature coefficient of R9 (TCR) will produce errors in the output current. Changes in R9 may be caused by self-heating of the device or by ambient temperature changes.

$$\frac{\Delta I_S}{I_{SPAN}} (\text{in } \%) = 100 \frac{\Delta R9}{\Delta T} (\theta P_{DISS} + \Delta T_A)$$

Where:

θ = Thermal resistance either from junction-to-ambient or junction-to-case

ΔP_{DISS} = Change in average power dissipation

ΔT_A = Change in ambient temperature

$\frac{\Delta R9}{\Delta T}$ = TCR of R9

Using the LH0045G design example, $\Delta R9/\Delta T$ = 0.03%/°C, hence a 3.2% worst case error in output current might be expected for operation without a heat sink over the temperature range.

Heat sinking the device and using R_L = 800Ω, reduces $\Delta I_S/I_{SPAN}$ to 2.3%. Comparable error for the LH0045K would also be about 2.3%.

The error analysis indicates that the internal current set resistor, R9 is inadequate to satisfy high accuracy design criterion. In these instances, an external 100Ω resistor should be substituted for R9.

Obviously, the TCR of the resistor should be low. Metal film or wire-wound resistors are the best choice offering TCR's less than 10 ppm/°C versus 50 ppm/°C typical drift for R9.

External Causes of Error

The components external to the LH0045 are also critical in determining errors. Specifically, the composition of resistors R_{B1}, R_{OS}, R_F, R, etc. in the design example will influence both drift and long term stability.

In particular, resistors and potentiometers of wire wound construction are recommended. Also, metal-film resistors with low TCR (≤ 10 ppm/°C) may be used for fixed resistor applications.

applications information (con't)

Error Analysis Summary

The overall errors attributable to the LH0045 may be minimized using heat sinking, and utilization of an external load resistor. Although R_L reduces the compliance of the circuit, its use is generally advisable in precision applications. External components should be selected for low TCR and long-term stability.

The design example errors, using an external 100Ω wire wound resistor for R9 equal:

$$\frac{\Delta I_S}{I_{SPAN}} = \underbrace{0.12\%}_{\Delta V_{REF}} + \underbrace{0.26\%}_{\Delta V_{OS}} + \underbrace{0.08\%}_{\Delta R9} = 0.46\%$$

definition of terms

Input Offset Voltage, V_{OS}: The voltage which must be applied between the input terminals through equal resistances to obtain 4.0 mA of supply (output) current.

Input Bias Current, I_B: The average of the two input currents.

Input Offset Current, I_{OS}: The difference in the current into the two input terminals when the supply (output) current is 4.0 mA.

Input Resistance, R_{IN}: The ratio of the change in input voltage to the change in input current at either input with the other input connected to 1.0 Vdc.

Open Loop Transconductance, g_{MOL}: The ratio of the supply (output) current SPAN to the input voltage required to produce that SPAN.

Open Loop Output Resistance, R_{OUT}: The ratio of a specified supply (output) voltage change to the resulting change in supply (output) current at the specified current level.

Common Mode Rejection Ratio, CMRR: The ratio of the change in input offset voltage to the peak-to-peak input voltage range.

Power Supply Rejection Ratio, PSRR: The ratio of the change in input offset voltage to the change in supply (output) voltage producing it.

Input Voltage Range, V_{IN}: The range of voltages on the input terminals for which the device operates within specifications.

Open Loop Supply Current, I_S: The supply current required with the signal amplifier A_2 biased off (inverting input positive, non-inverting input negative) and no load on the V_{REF} terminal.

This represents a measure of the minimum low end signal current.

Reference Voltage Line Regulation, $\Delta V_{REF}/\Delta V_S$: The ratio of the change in V_{REF} to the peak-to-peak change in supply (output) voltage producing it.

Reference Voltage Load Regulation, $\Delta V_{REF}/\Delta I_{REF}$: The change in V_{REF} for a stipulated change in I_{REF}.

NATIONAL

LH0061/LH0061C 0.5 amp wide band operational amplifier

general description

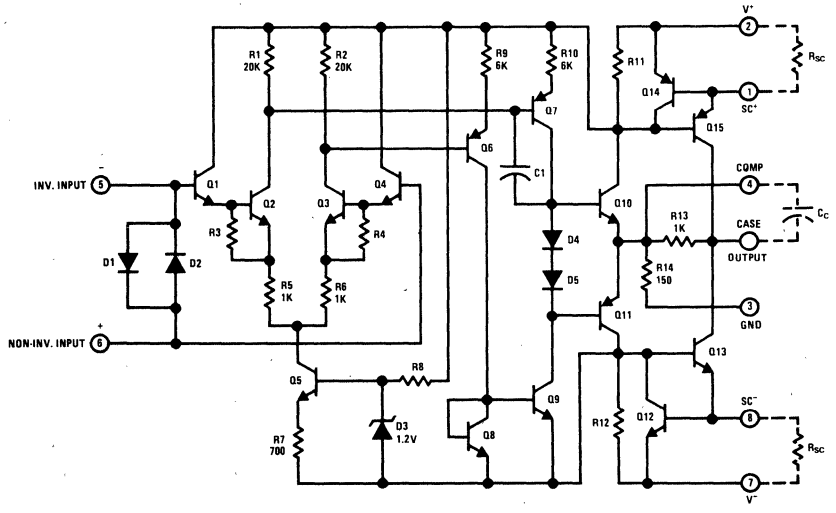
The LH0061/LH0061C is a wide band, high speed, operational amplifier capable of supplying currents in excess of 0.5 ampere at voltage levels of ±12V. Output short circuit protection is set by external resistors, and compensation is accomplished with a single external capacitor. With a suitable heat sink the device is rated at 20 Watts.

The wide bandwidth and high output power capabilities of the LH0061/LH0061C make it ideal for such applications as AC servos, deflection yoke drivers, capstan drivers, and audio amplifiers. The LH0061 is guaranteed over the temperature range −55°C to +125°C; whereas, the LH0061C is guaranteed from −25°C to +85°C.

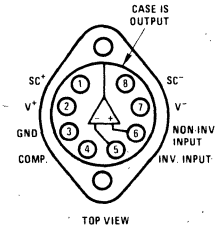
features

- Output current 0.5 Amp
- Wide large signal bandwidth 1 MHz
- High slew rate 70V/μs
- Low standby power 240 mW
- Low input current 300 nA Max

schematic and connection diagrams



TO-3 Package



Order Numbers:

LH0061K (−55°C to +125°C)
LH0061CK (−25°C to +85°C)
See Package 14

absolute maximum ratings

Supply Voltage	±18V
Power Dissipation	See Curve
Differential Input Current (Note 2)	±10 mA
Input Voltage (Note 3)	±15V
Peak Output Current	2A
Output Short Circuit Duration (Note 4)	Continuous
Operating Temperature Range LH0061	−55°C to +125°C
LH0061C	−25°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

dc electrical characteristics (Note 1)

PARAMETER	CONDITIONS	LIMITS						UNITS
		LH0061			LH0061C			
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$R_S \leq 10\ k\Omega$, $T_C = 25°C$, $V_S = \pm 15V$		1.0	4.0		3.0	10	mV
	$R_S \leq 10\ k\Omega$, $V_S = \pm 15V$			6.0			15	mV
Voltage Drift with Temperature	$R_S \leq 10\ k\Omega$		5			5		µV/°C
Offset Voltage Change with Output Power			5			5		µV/watt
Input Offset Current	$T_C = 25°C$		30	100		50	200	nA
				300			500	nA
Offset Current Drift with Temperature			1			1		nA/°C
Input Bias Current	$T_C = 25°C$		100	300		200	500	nA
				1.0			1.0	µA
Input Resistance	$T_C = 25°C$	0.3	1.0		0.3	1.0		MΩ
Input Capacitance			3			3		pF
Common Mode Rejection Ratio	$R_S \leq 10\ k\Omega$, $\Delta V_{CM} = \pm 10V$	70	90		60	80		dB
Input Voltage Range	$V_S = \pm 15V$	±11			±11			V
Power Supply Rejection Ratio	$R_S \leq 10\ k\Omega$, $\Delta V_S = \pm 10V$	70	80		50	70		dB
Voltage Gain	$V_S = \pm 15V$, $V_O = \pm 10V$							
	$R_L = 1\ k\Omega$, $T_C = 25°C$	50	100		25	50		V/mV
	$V_S = \pm 15V$, $V_O = \pm 10V$							
	$R_L = 20\Omega$	5			2.5			V/mV
Output Voltage Swing	$V_S = \pm 15V$, $R_L = 20\Omega$	±10	±12		±10	±12		V
Output Short Circuit Current	$V_S = \pm 15V$, $T_C = 25°C$, $R_{SC} = 1.0\Omega$		600			600		mA
Power Supply Current	$V_S = \pm 15V$, $V_{OUT} = 0$		7	10		10	15	mA
Power Consumption	$V_S = \pm 15V$, $V_{OUT} = 0$		210	300		300	450	mW

ac electrical characteristics ($T_C = 25°C$, $V_S = \pm 15V$, $C_C = 3000$ pF)

Slew Rate	$A_V = +1$, $R_L = 100\Omega$	25	70		25	70		V/µs
Power Bandwidth	$R_L = 100\Omega$		1			1		MHz
Small Signal Transient Response			30			30		ns
Small Signal Overshoot			5	20		10	30	%
Settling Time (0.1%)	$\Delta V_{IN} = 10V$, $A_V = +1$		0.8			0.8		µs
Overload Recovery Time			1			1		µs
Harmonic Distortion	f = 1 kHz, $P_O = 0.5W$		0.2			0.2		%

Note 1: Specifications apply for $\pm 5V \leq V_S \leq \pm 18V$, $C_C = 3000$ pF, and $-55°C \leq T_C \leq +125°C$ for the LH0061K and $-25°C \leq T_C \leq +85°C$ for the LH0061CK. Typical values are for $T_C = 25°C$.

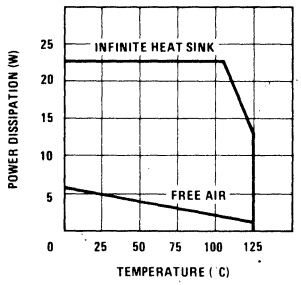
Note 2: The inputs are shunted with back-to-back diodes for overvoltage protection. Excessive current will flow if a differential voltage in excess of 1V is applied between the inputs without limiting resistors.

Note 3: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

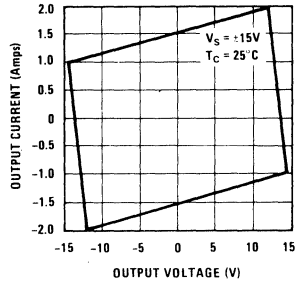
Note 4: Rating applies as long as package power rating is not exceeded.

typical performance characteristics

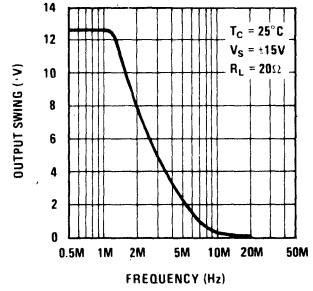
Power Derating



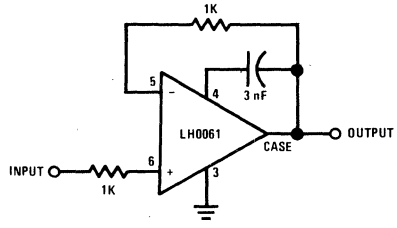
Safe Operating Area



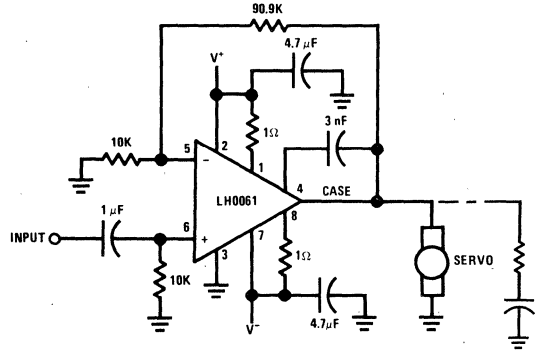
Large Signal Frequency Response



typical applications



Unity Gain Driver



AC Servo Amplifier

NATIONAL

LH0062/LH0062C high speed FET op amp

general description

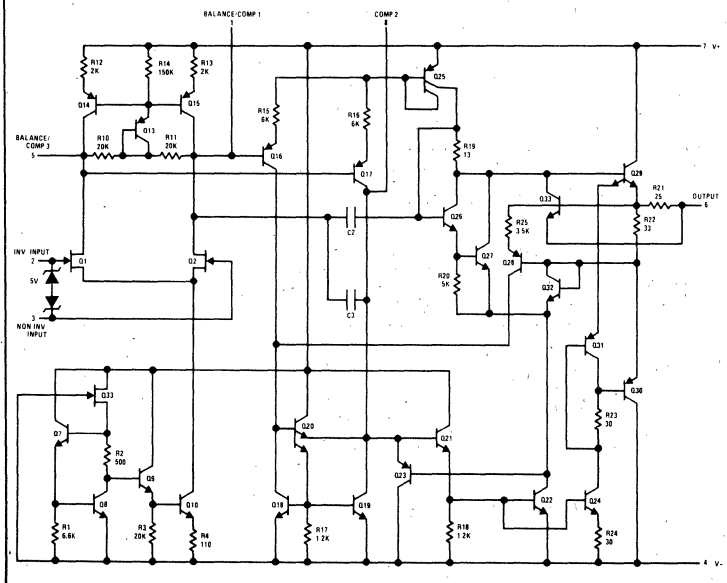
The LH0062/LH0062C is a precision, high speed FET input operational amplifier with more than an order of magnitude improvement in slew rate and bandwidth over conventional FET IC op amps. In addition it features very closely matched input characteristics, very high input impedance, and ultra low input currents with no compromise in noise, common mode rejection ratio or open loop gain. The device has internal unity gain frequency compensation, thus assuring stability in all normal applications. This considerably simplifies its application, since no external components are necessary for operation. However, unlike most internally compensated amplifiers, external frequency compensation may be added for optimum performance. For inverting applications, feed-forward compensation will boost the slew rate to over 120 V/μs and almost double the bandwidth. (See LB-2, LB-14, and LB-17 for discussions of the application of feed-forward techniques). Over-compensation can be used with the amplifier for greater stability when maximum bandwidth is not needed. Further, a single capacitor can be added to reduce the 0.1% settling time to under 1 μs. In addition it is free of latch-up and may be simply offset nulled with negligible effect on offset drift or CMRR.

The LH0062 is designed for applications requiring wide bandwidth, high slew rate and fast settling time while at the same time demanding the high input impedance and low input currents characteristic of FET inputs. Thus it is particularly suited for such applications as video amplifiers, sample/hold circuits, high speed integrators, and buffers for A/D conversion and multiplex system. The LH0062 is specified for the full military temperature range of −55°C to +125°C while the LH0062C is specified to operate over a −25°C to +85°C temperature range.

features

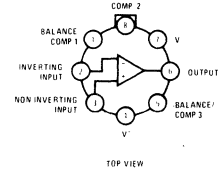
- High slew rate — 70 V/μs
- Wide bandwidth — 15 MHz
- Settling time (0.1%) — 1μs
- Low input offset voltage — 2 mV
- Low input offset current — 1 pA
- Wide supply range — ±5V to ±20V
- Internal 6 dB/octave frequency compensation
- Pin compatible with std IC op amps (TO-5 pkg)

schematic and connection diagrams*



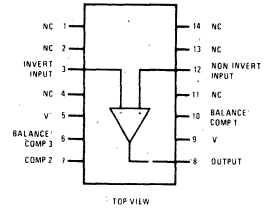
*Pin Numbers Shown for TO-5 Package

Metal Can Package



Order Number
LH0062H or LH0062CH
See Package 9

Dual-In-Line Package



Order Number
LH0062D or LH0062CD
See Package 1

absolute maximum ratings

Supply Voltage	±20V	Operating Temperature	
Power Dissipation (see graph)	500 mW	LH0062,	−55°C to +125°C
Input Voltage (Note 1)	±15V	LH0062C,	−25°C to +85°C
Differential Input Voltage (Note 2)	±30V	Storage Temperature Range	−65°C to +150°C
Short Circuit Duration	Continuous	Lead Temperature (Soldering, 10 sec)	300°C

dc electrical characteristics (Note 3)

PARAMETER	CONDITIONS	LIMITS						UNITS
		LH0062			LH0062C			
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$R_S \leq 100\ k\Omega$; $T_A = 25°C$		2	5		10	15	mV
	$R_S \leq 100\ k\Omega$			7			20	mV
Temperature Coefficient of Input Offset Voltage	$R_S \leq 100\ k\Omega$		5	25		10	35	µV/°C
Offset Voltage Drift with Time			4			5		µV/week
Input Offset Current	$T_A = 25°C$		0.2	2		1	5	pA
				2			0.2	nA
Temperature Coefficient of Input Offset Current		Doubles every 10°C			Doubles every 10°C			
Offset Current Drift with Time			0.1			0.1		pA/week
Input Bias Current	$T_A = 25°C$		5	10		10	65	pA
				10			2	nA
Temperature Coefficient of Input Bias Current		Doubles every 10°C			Doubles every 10°C			
Differential Input Resistance			10^{12}			10^{12}		Ω
Common Mode Input Resistance			10^{12}			10^{12}		Ω
Input Capacitance			4			4		pF
Input Voltage Range	$V_S = \pm15V$	±10	±12		±10	±12		V
Common Mode Rejection Ratio	$R_S \leq 10\ k\Omega$, $V_{IN} = \pm10V$	80	90		70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10\ k\Omega$, $\pm5V \leq V_S \leq \pm15V$	80	90		70	90		dB
Large Signal Voltage Gain	$R_L = 2\ k\Omega$, $V_{OUT} = \pm10V$, $T_A = 25°C$, $V_S = \pm15V$	50	200		25	160		V/mV
	$R_L = 2\ k\Omega$, $V_{OUT} = \pm10V$, $V_S = \pm15V$	25			25			V/mV
Output Voltage Swing	$R_L = 2\ k\Omega$, $T_A = 25°C$, $V_S = \pm15V$	±12	±13		±12	±13		V
	$R_L = 2\ k\Omega$, $V_S = \pm15V$	±10			±10			V
Output Current Swing	$V_{OUT} = \pm10V$, $T_A = 25°C$	±10	±15		±10	±15		mA
Output Resistance			75			75		Ω
Output Short Circuit Current	$T_A = 25°C$		25			25		mA
Supply Current	$V_S = \pm15V$		5	8		7	12	mA
Power Consumption	$V_S = \pm15V$			240			360	mW

ac electrical characteristics ($T_A = 25°C$, $V_S = \pm15V$)

PARAMETER	CONDITIONS	LIMITS						UNITS
		LH0062			LH0062C			
		MIN	TYP	MAX	MIN	TYP	MAX	
Slew Rate	Voltage Follower	50	70		50	70		V/µs
Large Signal Bandwidth	Voltage Follower		2			2		MHz
Small Signal Bandwidth			15			15		MHz
Rise Time			25			25		ns
Overshoot			10			15		%
Settling Time (0.1%)	$\Delta V_{IN} = 10V$		1			1		µs
Overload Recovery			0.9			0.9		µs
Input Noise Voltage	$R_S = 10\ k\Omega$, $f_o = 10$ Hz		150			150		$nV/\sqrt{Hz}$
Input Noise Voltage	$R_S = 10\ k\Omega$, $f_o = 100$ Hz		55			55		$nV/\sqrt{Hz}$
Input Noise Voltage	$R_S = 10\ k\Omega$, $f_o = 1$ kHz		35			35		$nV/\sqrt{Hz}$
Input Noise Voltage	$R_S = 10\ k\Omega$, $f_o = 10$ kHz		30			30		$nV/\sqrt{Hz}$
Input Noise Voltage	BW = 10 Hz to 10 kHz, $R_S = 10\ k\Omega$		12			12		µVrms
Input Noise Current	BW = 10 Hz to 10 kHz		<.1			<.1		pArms

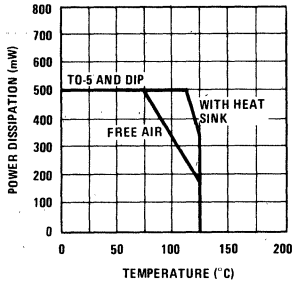
Note 1: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Note 2: Rating applies for minimum source resistance of 10 kΩ, for source resistances less than 10 kΩ, maximum differential input voltage is ±5V.

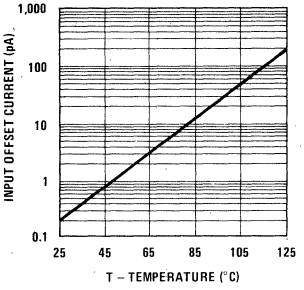
Note 3: Unless otherwise specified, these specifications apply for $\pm5V \leq V_S \leq \pm20V$ and $-55°C \leq T_A \leq +125°C$ for the LH0062 and $-25°C \leq T_A \leq +85°C$ for LH0062C. Typical values are given for $T_A = 25°C$. Power supplies should be bypassed with 0.1 µF ceramic capacitors.

typical performance characteristics

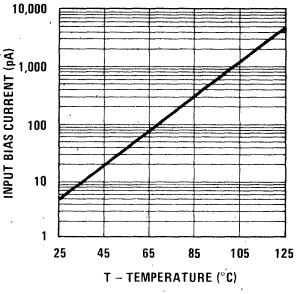
Maximum Power Dissipation



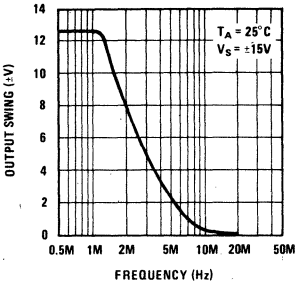
Input Offset Current vs Temperature



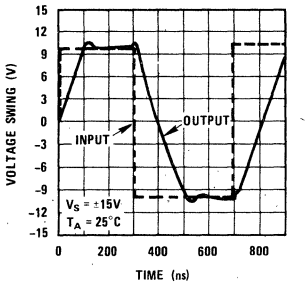
Input Bias Current vs Temperature



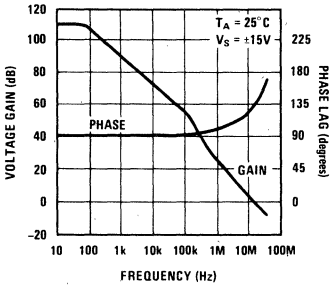
Large Signal Frequency Response



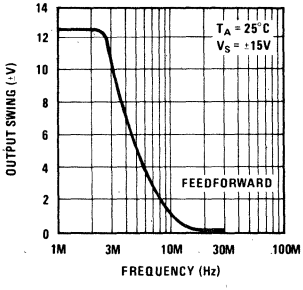
Voltage Follower Pulse Response



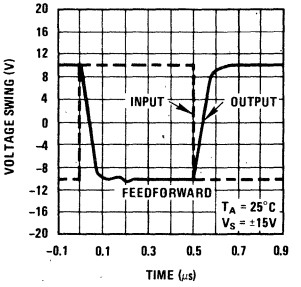
Open Loop Frequency Response



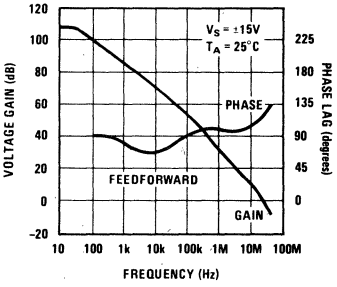
Large Signal Frequency Response



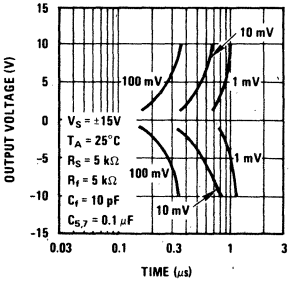
Inverter Pulse Response



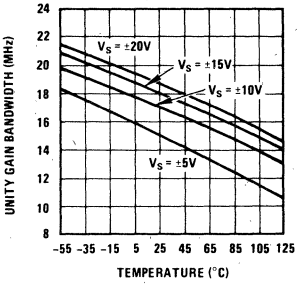
Open Loop Frequency Response



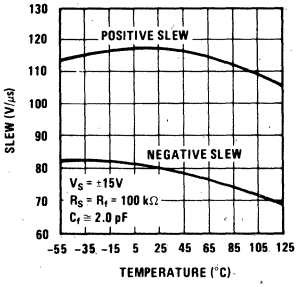
Inverter Settling Time



Unity Gain Bandwidth

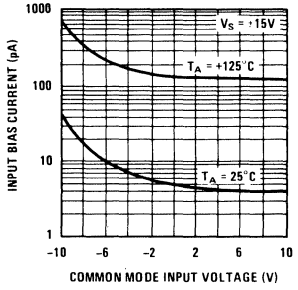


Voltage Follower Slew Rate

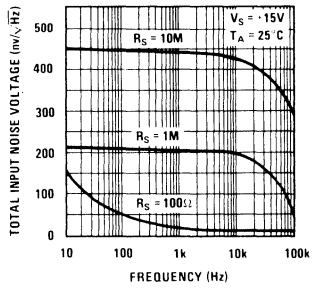


typical performance characteristics (con't)

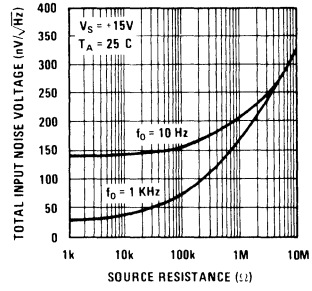
Input Bias Current vs Input Voltage



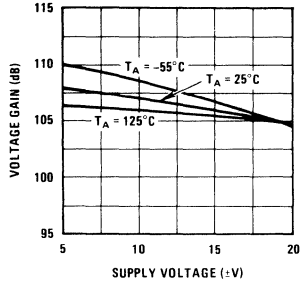
Total Input Noise Voltage* vs Frequency



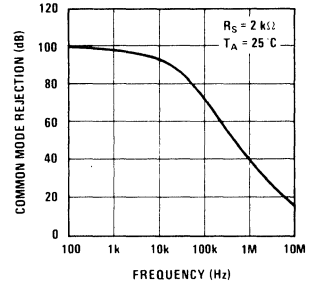
Total Input Noise Voltage* vs Source Resistance



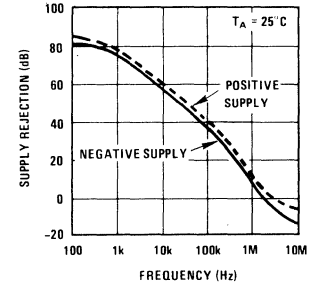
Voltage Gain



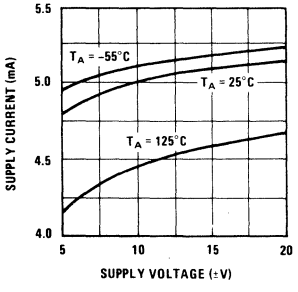
Common Mode Rejection



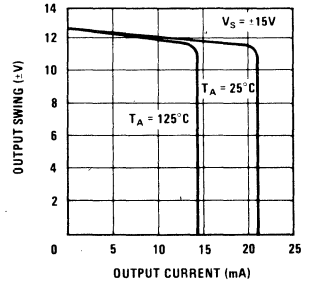
Power Supply Rejection



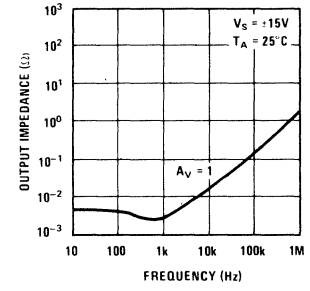
Supply Current



Current Limiting



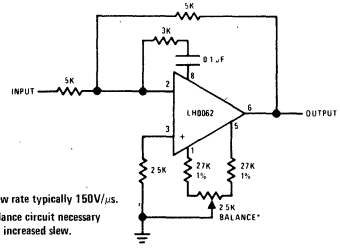
Closed Loop Output Impedance



*Noise Voltage Includes Contribution from Source Resistance

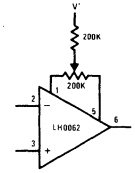
auxiliary circuits

Feedforward Compensation for Greater Inverting Slew Rate†

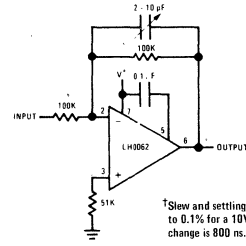


†Slew rate typically 150V/µs.
*Balance circuit necessary for increased slew.

Offset Balancing



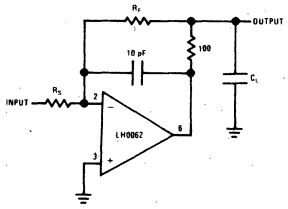
Compensation for Minimum Settling† Time



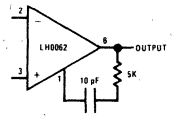
†Slew and settling time to 0.1% for a 10V step change is 800 ns.

auxiliary circuits (con't)

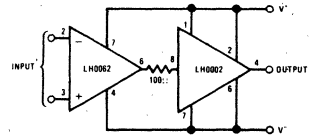
Isolating Large Capacitive Loads



Overcompensation

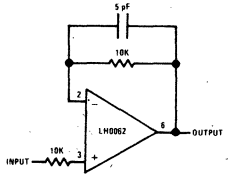


Boosting Output Drive to ± 100 mA

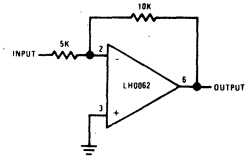


typical applications*

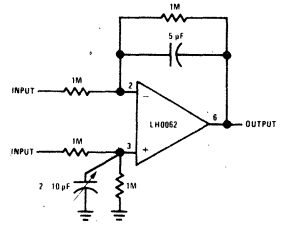
Fast Voltage Follower



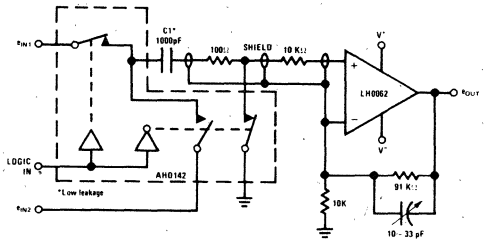
Fast Summing Amplifier



Differential Amplifier

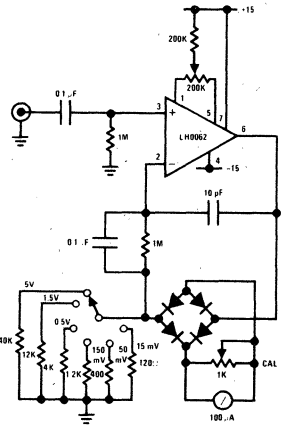


High Speed Subtractor

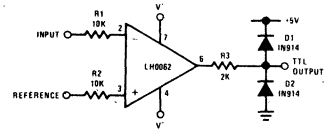


$e_{OUT} = 10 \times (e_{IN1} - e_{IN2})$

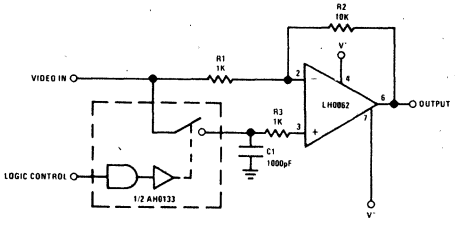
Wide Range AC Voltmeter



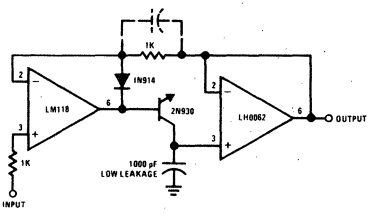
Fast Precision Voltage Comparator



Video DC Restoring Amplifier



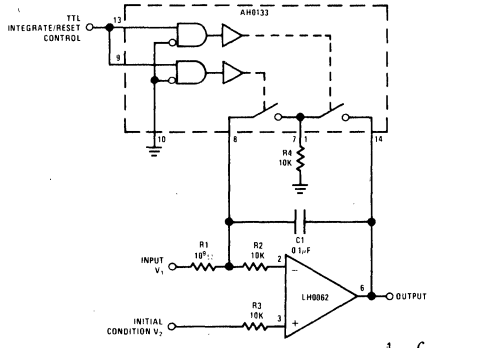
High Speed Positive Peak Detector



*Pin numbers shown for TO-5 package

typical applications* (con't)

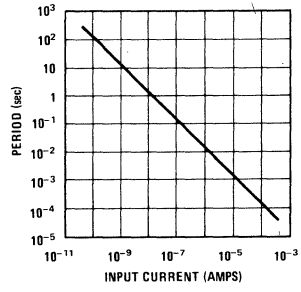
Precision Integrator

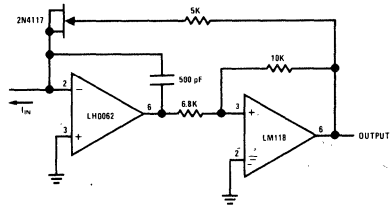


$$V_{OUT} = \frac{1}{C1R1} \int -V_1\,dt + V_2$$

*Pin numbers shown for TO-5 package

Precision Wide Range Current to Period Converter





NATIONAL

Amplifiers

LH740A/LH740AC FET input operational amplifier

general description

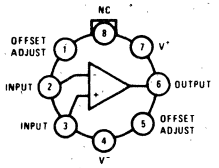
The LH740A/LH740AC is a FET input, general purpose operational amplifier with high input impedance, closely matched input characteristics, and good slew rates. Input offset voltage is typically 10.0 mV at 25°C, while input bias current is less than 100 pA at 25°C. Offset current is typically less than 40 pA at 25°C. Other important design features include:

- Internal 6 dB/octave frequency compensation
- Unity gain slew rate in excess of 6 V/μs
- Unity gain bandwidth of 1 MHz
- Input offset is adjustable with a single 10k pot
- Pin compatible with LM741, LM709, LM101A, and μA740
- Excellent offset current match over temperature, typically 100 pA
- Output is continuously short-circuit proof
- Excellent open loop gain, typically in excess of 100 dB
- Guaranteed over the full military temperature range

The LH740A/LH740AC is intended to fulfill a wide variety of applications requiring extremely low bias currents such as integrators, sample and hold amplifiers, and general purpose operational amplifier applications.

The LH740A is specified for operation over the −55°C to +125°C military temperature range. The LH740AC is specified for operation over the 0°C to +85°C temperature range.

connection diagram



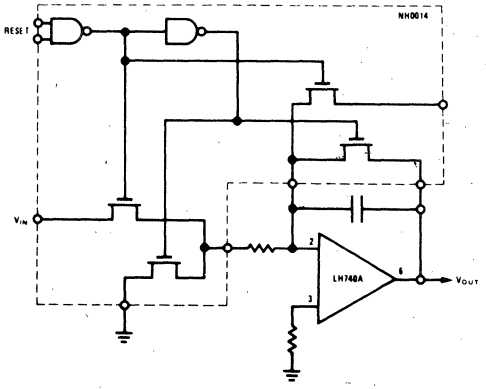
TOP VIEW

Order Number LH740AH or LH740ACH

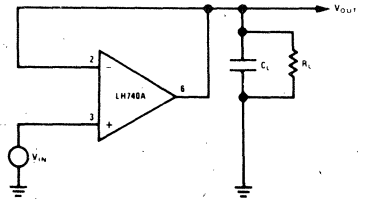
See Package 9

typical applications

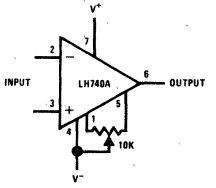
Integrator



Transient Response



Offset Null



absolute maximum ratings

Supply Voltage		±22V
Maximum Power Dissipation		500 mW
Differential Input Voltage		±5V
Input Voltage		±15V
Short Circuit Duration		Continuous
Operating Temperature Range	LH740A	−55°C to +125°C
	LH740AC	0°C to +85°C
Storage Temperature Range		−65°C to +150°C
Lead Temperature (soldering, 10 sec.)		300°C

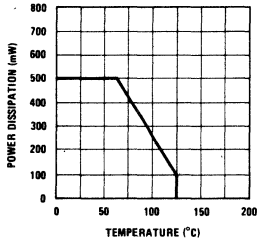
electrical characteristics (Note 1) (V_S = ±15V, T_A = 25°C unless otherwise noted)

PARAMETER	CONDITIONS	LH740A			LH740AC			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$R_S \leq 100$ kΩ		10	15		10	20	mV
Input Offset Current			40	100		60	150	pA
Input Current (either input)			100	200		100	500	pA
Input Resistance			1,000,000			1,000,000		MΩ
Large Signal Voltage Gain	$R_L \geq 2$ kΩ, V_{OUT} = ±10V	50,000	100,000		50,000	100,000		V/V
Output Resistance			75			75		Ω
Output Short-Circuit Current			20			20		mA
Common Mode Rejection Ratio		80			80			dB
Supply Voltage Rejection Ratio		80			80			dB
Supply Current			3.0	4.0		3.0	4.0	mA
Slew Rate			6.0			6.0		V/μs
Unity Gain Bandwidth			1.0			1.0		MHz
Transient Response (Unity Gain)	$C_L \leq 100$ pF, R_L = 2 kΩ, V_{IN} = 100 mV							
Risetime			110			300		ns
Overshoot			10	20		10		%
(These specifications apply for −55°C < T_A < 125°C for the LH740A and 0°C < T_A < 85°C for the LH740AC unless otherwise noted.)								
Input Voltage Range		±12			±12			V
Common Mode Rejection Ratio		80			80			dB
Supply Voltage Rejection Ratio		80			80			dB
Large Signal Voltage Gain		40,000			40,000			V/V
Output Voltage Swing	$R_L \geq 10$ kΩ	±12	±14		±12	±14		V
	$R_L \geq 2$ kΩ	±10	±13		±10	±13		V
Input Offset Voltage			15	20		30		mV
Input Offset Current			100	500		60	500	pA
Input Current (either input)			2.5	4.0		1.1	5.0	nA
Offset Voltage Drift	$R_S \leq 100$K		5.0			5.0		μV/°C

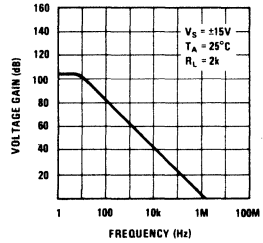
Note 1: For supply voltages less than ±10V, the absolute maximum input voltage is equal to the supply voltage.

typical performance characteristics

Maximum Power Dissipation



Open Loop Frequency Response



NATIONAL

LH2101A/LH2201A/LH2301A dual high performance op amp

general description

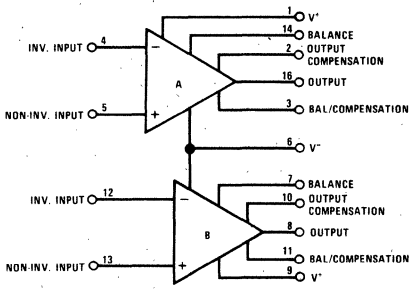
The LH2101A series of dual operational amplifiers are two LM101A type op amps in a single hermetic package. Featuring all the same performance characteristics of the single, these duals offer in addition closer thermal tracking, lower weight, reduced insertion cost, and smaller size than two singles. For additional information, see the LM101A data sheet and National's Linear Application Handbook.

The LH2101A is specified for operation over the −55°C to +125°C military temperature range. The LH2201A is specified for operation over the −25°C to +85°C temperature range. The LH2301A is specified for operation over the 0°C to +70°C temperature range.

features

- Low offset voltage
- Low offset current
- Guaranteed drift characteristics
- Offsets guaranteed over entire common mode and supply voltage ranges
- Slew rate of 10V/μs as a summing amplifier

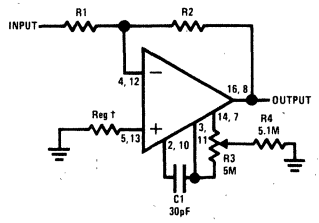
connection diagram



Order Number LH2101AD or LH2201AD or LH2301AD
See Package 2

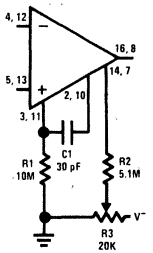
auxiliary circuits

Inverting Amplifier with Balancing Circuit

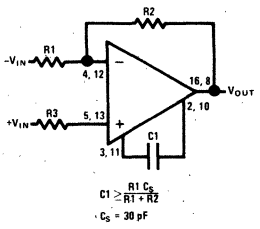


†May be zero or equal to parallel combination of R1 and R2 for minimum offset

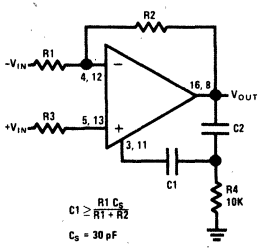
Alternate Balancing Circuit



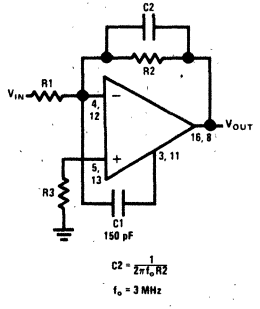
Single Pole Compensation



Two Pole Compensation



Feedforward Compensation



absolute maximum ratings

Supply Voltage	±22V	Operating Temperature Range	LH2101A	-55°C to 125°C
Power Dissipation (Note 1)	500 mW		LH2201A	-25°C to 85°C
Differential Input Voltage	±30V		LH2301A	0°C to 70°C
Input Voltage (Note 2)	±15V	Storage Temperature Range		-65°C to 150°C
Output Short-Circuit Duration	Continuous	Lead Temperature (Soldering, 10 sec)		300°C

electrical characteristics each side (Note 3)

PARAMETER	CONDITIONS	LIMITS			UNITS
		LH2101A	LH2201A	LH2301A	
Input Offset Voltage	$T_A = 25°C$, $R_S \leq 50\ k\Omega$	2.0	2.0	7.5	mV Max
Input Offset Current	$T_A = 25°C$	10	10	50	nA Max
Input Bias Current	$T_A = 25°C$	75	75	250	nA Max
Input Resistance	$T_A = 25°C$	1.5	1.5	0.5	MΩ Min
Supply Current	$T_A = 25°C$, $V_S = \pm 20V$	3.0	3.3	3.0	mA Max
Large Signal Voltage Gain	$T_A = 25°C$, $V_S = \pm 15V$ $V_{OUT} = \pm 10V$, $R_L \geq 2\ k\Omega$	50	50	25	V/mV Min
Input Offset Voltage	$R_S \leq 50\ k\Omega$	3.0	3.0	10	mV Max
Average Temperature Coefficient of Input Offset Voltage		15	15	30	µV/°C Max
Input Offset Current		20	20	70	nA Max
Average Temperature Coefficient of Input Offset Current	$25°C \leq T_A \leq 125°C$ $-55°C \leq T_A \leq 25°C$	0.1 0.2	0.1 0.2	0.3 0.6	nA/°C Max nA/°C Max
Input Bias Current		100	100	300	nA Max
Supply Current	$T_A = +125°C$, $V_S = \pm 20V$	2.5	2.5		mA Max
Large Signal Voltage Gain	$V_S = \pm 15V$, $V_{OUT} = \pm 10V$ $R_L \geq 2\ k\Omega$	25	25	15	V/mV Min
Output Voltage Swing	$V_S = \pm 15V$, $R_L = 10\ k\Omega$ $R_L = 2\ k\Omega$	±12 ±10	±12 ±10	±12 ±10	V Min V Min
Input Voltage Range	$V_S = \pm 20V$	±15	±15	±12	V Min
Common Mode Rejection Ratio	$R_S \leq 50\ k\Omega$	80	80	70	dB Min
Supply Voltage Rejection Ratio	$R_S \leq 50\ k\Omega$	80	80	70	dB Min

Note 1: The maximum junction temperature of the LH2101A is 150°C, while that of the LH2201A is 100°C. For operating temperatures, devices in the flat package, the derating is based on a thermal resistance of 185°C/W when mounted on a 1/16-inch-thick epoxy glass board with 0.03-inch-wide, 2-ounce copper conductors. The thermal resistance of the dual-in-line package is 100°C/W, junction to ambient.

Note 2: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Note 3: These specifications apply for $\pm 5V \leq V_S \leq \pm 20V$ and $-55°C \leq T_A \leq 125°C$, unless otherwise specified. With the LH2201A, however, all temperature specifications are limited to $-25°C \leq T_A \leq 85°C$. For the LH2301A these specifications apply for $0°C \leq T_A \leq 70°C$, ±5V and $\leq V_S \leq \pm 15V$. Supply current and input voltage range are specified as $V_S = \pm 15V$ for the LH2301A. $C_1 = 30$ pF unless otherwise specified.

LH2108/LH2208/LH2308, LH2108A/LH2208A/LH2308A
dual super beta op amp
general description

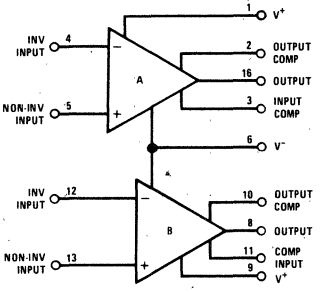
The LH2108A/LH2208A/LH2308A and LH2108/LH2208/LH2308 series of dual operational amplifiers are two LM108A or LM108 type op amps in a single hermetic package. Featuring all the same performance characteristics of the single device, these duals also offer closer thermal tracking, lower weight, reduced insertion cost, and smaller size than two single devices. For additional information see the LM108A or LM108 data sheet and National's Linear Application Handbook.

The LH2108A/LH2108 is specified for operation over the -55°C to +125°C military temperature range. The LH2208A/LH2208 is specified for operation over the -25°C to +85°C temperature range. The LH2308A/LH2308 is specified for operation over the 0°C to +70°C temperature range.

features

- Low offset current — 50 pA
- Low offset voltage — 0.7 mV
- Low offset voltage — LH2108A 0.3 mV; LH2108 0.7 mV
- Wide input voltage range — ±15V
- Wide operating supply range — ±3V to ±20V

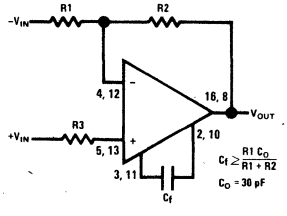
connection diagram



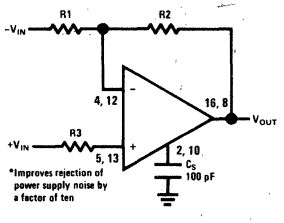
Order Number LH2108AD, LH2208AD LH2308AD, or LH2108D, LH2208D, or LH2308D
See Package 2

auxiliary circuits

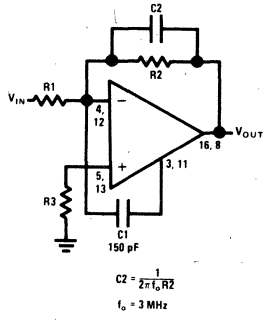
Standard Compensation Circuit



Alternate * Frequency Compensation



Feedforward Compensation



absolute maximum ratings

Supply Voltage	±20V	Operating Temperature Range	
Power Dissipation (Note 1)	500 mW	LH2108A/LH2108	−55°C to +125°C
Differential Input Current (Note 2)	±10 mA	LH2208A/LH2208	−25°C to +85°C
Input Voltage (Note 3)	±15V	LH2308A/LH2308	0°C to +70°C
Output Short Circuit Duration	Continuous	Storage Temperature Range	−65°C to +150°C
		Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics each side (Note 4)

PARAMETER	CONDITIONS	LIMITS			UNITS
		LH2108	LH2208	LH2308	
Input Offset Voltage	$T_A = 25°C$	2.0	2.0	7.5	mV Max
Input Offset Current	$T_A = 25°C$	0.2	0.2	1.0	nA Max
Input Bias Current	$T_A = 25°C$	2.0	2.0	7.0	nA Max
Input Resistance	$T_A = 25°C$	30	30	10	MΩ Min
Supply Current	$T_A = 25°C$	0.6	0.6	0.8	mA Max
Large Signal Voltage Gain	$T_A = 25°C$ $V_S = \pm 15V$ $V_{OUT} = \pm 10V$, $R_L > 10\ k\Omega$	50	50	25	V/mV Min
Input Offset Voltage		3.0	3.0	10	mV Max
Average Temperature Coefficient of Input Offset Voltage		15	15	30	μV/°C Max
Input Offset Current		0.4	0.4	1.5	nA Max
Average Temperature Coefficient of Input Offset Current		2.5	2.5	10	pA/°C Max
Input Bias Current		3.0	3.0	10	nA Max
Supply Current	$T_A = +125°C$	0.4	0.4	–	mA Max
Large Signal Voltage Gain	$V_S = \pm 15V$, $V_{OUT} = \pm 10V$ $R_L > 10\ k\Omega$	25	25	15	V/mV Min
Output Voltage Swing	$V_S = \pm 15V$, $R_L = 10\ k\Omega$	±13	±13	±13	V Min
Input Voltage Range	$V_S = \pm 15V$	±13.5	±13.5	±14	V Min
Common Mode Rejection Ratio		85	85	80	dB Min
Supply Voltage Rejection Ratio		80	80	80	dB Min

electrical characteristics each side (Note 4)

PARAMETER	CONDITIONS	LIMITS			UNITS
		LH2108A	LH2208A	LH2308A	
Input Offset Voltage	$T_A = 25°C$	0.5	0.5	0.5	mV Max
Input Offset Current	$T_A = 25°C$	0.2	0.2	1.0	nA Max
Input Bias Current	$T_A = 25°C$	2.0	2.0	7.0	nA Max
Input Resistance	$T_A = 25°C$	30	30	10	MΩ Min
Supply Current	$T_A = 25°C$	0.6	0.6	0.8	mA Max
Large Signal Voltage Gain	$T_A = 25°C$ $V_S = \pm 15V$ $V_{OUT} = \pm 10V$, $R_L > 10\ k\Omega$	80	80	80	V/mV Min
Input Offset Voltage		1.0	1.0	0.73	mV Max
Average Temperature Coefficient of Input Offset Voltage		5	5	5	μV/°C Max
Input Offset Current		0.4	0.4	1.5	nA Max
Average Temperature Coefficient of Input Offset Current		2.5	2.5	10	pA/°C Max
Input Bias Current		3.0	3.0	10	nA Max
Supply Current	$T_A = +125°C$	0.4	0.4	–	mA Max
Large Signal Voltage Gain	$V_S = \pm 15V$, $V_{OUT} = \pm 10V$ $R_L > 10\ k\Omega$	40	40	60	V/mV Min
Output Voltage Swing	$V_S = \pm 15V$, $R_L = 10\ k\Omega$	±13	±13	±13	V Min
Input Voltage Range	$V_S = \pm 15V$	±13.5	±13.5	±14	V Min
Common Mode Rejection Ratio		96	96	96	dB Min
Supply Voltage Rejection Ratio		96	96	96	dB Min

Note 1: The maximum junction temperature of the LH2108A/LH2108 is 150°C, while that of the LH2208A/LH2208 is 100°C and the LH2308A/LH2308 is 85°C. For operating at elevated temperatures, devices in the flat package, the derating is based on a thermal resistance of 185°C/W when mounted on a 1/16-inch-thick epoxy glass board with 0.03-inch-wide, 2-ounce cooper conductors. The thermal resistance of the dual-in-line package is 100°C/W, junction to ambient.

Note 2: The inputs are shunted with back-to-back diodes for overvoltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1V is applied between the inputs unless some limiting resistance is used.

Note 3: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Note 4: These specifications apply for $\pm 5V \leq V_S \leq \pm 20V$ and $-55°C \leq T_A \leq 125°C$, unless otherwise specified. With the LH2208A/LH2208, however, all temperature specifications are limited to $-25°C \leq T_A \leq 85°C$ and with the LH2308A/LH2308 for $\pm 5V \leq V_S \leq 15V$ and $0°C \leq T_A \leq 70°C$.

NATIONAL

Amplifiers

LH24250/LH24250C dual programmable micropower op amp

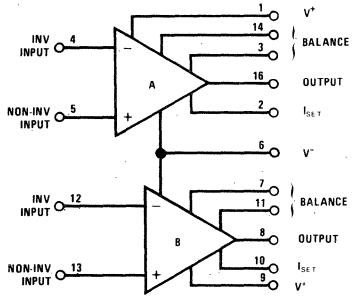
general description

The LH24250/LH24250C series of dual programmable micropower operational amplifiers are two LM4250 type op amps in a single hermetic package. Featuring all the same performance characteristics of the LM4250, the LH24250/LH24250C duals also offer closer thermal tracking, lower weight, reduced insertion cost and smaller size than two single devices. For additional information, see the LM4250 data sheet and National's Linear Application Handbook.

features

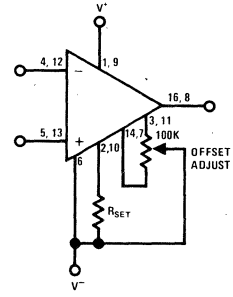
- ±1V to ±18V power supply operation
- Standby power consumption as low as 20 μW
- Offset current programmable from less than 0.5 nA to 30 nA
- Programmable slew rate
- May be shut-down using standard open collector TTL
- Internally compensated and short circuit proof

connection diagram and auxiliary circuit



Order Number LH24250D or LH24250CD
See Package 2

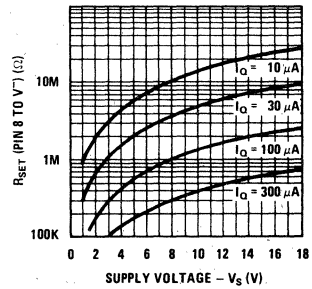
Offset Null Circuit



typical quiescent current setting resistor

(Pin 8 to V-)

V_S	10 μA	30 μA	100 μA	300 μA
±1.5	1.5 MΩ	470 kΩ	150 kΩ	
±3	3.3 MΩ	1.1 MΩ	330 kΩ	100 kΩ
±6	7.5 MΩ	2.7 MΩ	750 kΩ	220 kΩ
±9	13 MΩ	4 MΩ	1.3 MΩ	350 kΩ
±12	18 MΩ	5.6 MΩ	1.5 MΩ	510 kΩ
±15	22 MΩ	7.5 MΩ	2.2 MΩ	620 kΩ



absolute maximum ratings

Supply Voltage	±18V	Operating Temperature Range	
Power Dissipation (Note 1)	500 mW	LH24250	−55°C to +125°C
Differential Input Voltage (Note 2)	±15V	LH24250C	0°C to +70°C
Input Voltage (Note 3)	±15V	Storage Temperature Range	−65°C to +150°C
Output Short Circuit Duration	Continuous	Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics – each side (Note 4)

PARAMETER	CONDITIONS	LIMITS		UNITS
		LH24250	LH24250C	
Input Offset Voltage	$T_A = 25°C$, $R_S < 100\ k\Omega$	3.0	6.0	mV Max
Input Offset Current	$T_A = 25°C$	5	10	nA Max
Input Bias Current	$T_A = 25°C$	15	30	nA Max
Input Resistance	$T_A = 25°C$	3	3	MΩ Min
Power Consumption	$T_A = 25°C$, $V_O = 0$, $R_{SET} = 2.7\ M\Omega$	480	600	μW Max
Large Signal Voltage Gain	$T_A = 25°C$, $R_L > 10\ k\Omega$	100	75	V/mV Min
Input Offset Voltage	$R_S > 10\ k\Omega$	4.0	7.5	mV Max
Input Offset Current		5	15	nA Max
Input Bias Current		15	50	nA Max
Large Signal Voltage Gain	$R_L > 10\ k\Omega$	50	50	V/mV Min
Output Voltage Swing	$R_L > 10\ k\Omega$, $V_S = \pm 15V$	±10	±10	V Min
Input Voltage Range	$T_A = 25°C$, $V_S = \pm 15V$	±12	±12	V Min
Common Mode Rejection Ratio	$T_A = 25°C$, $R_S < 10\ k\Omega$	70	70	dB Min
Supply Voltage Rejection Ratio	$T_A = 25°C$, $R_S < 10\ k\Omega$	76	76	dB Min

Note 1: Derate linearly 2 mW/°C case temperature above 25°C.

Note 2: This rating applies to maximum voltage differential between input terminals. The maximum input voltage on either input terminal is limited to $\pm V_S$ up to ±15V.

Note 3: This rating limited to ± supply voltage to a maximum of ±15V.

Note 4: These specifications apply for $V_S = \pm 6V$, $I_Q = 30\ \mu A$, and $-55°C < T_A < +125°C$ unless otherwise specified. With the LH24250C, however, all temperature specifications are limited to $0°C < T_A < 70°C$.

NATIONAL

LH0002/LH0002C* current amplifier

general description

The LH0002/LH0002C is a general purpose thick film hybrid current amplifier that is built on a single substrate. The circuit features:

- High Input Impedance 400 kΩ
- Low Output Impedance 6Ω
- High Power Efficiency
- Low Harmonic Distortion
- DC to 30 MHz Bandwidth
- Output Voltage Swing that Approaches Supply Voltage
- 400 mA Pulsed Output Current
- Slew rate is typically 200V/μs
- Operation from ±5V to ±20V

These features make it ideal to integrate with an operational amplifier inside a closed loop configuration to increase current output. The symmetrical output portion of the circuit also provides a low output impedance for both the positive and negative slopes of output pulses.

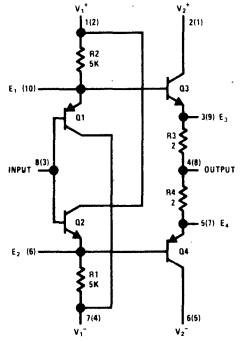
The LH0002 is available in an 8-lead low-profile TO-5 header; the LH0002C is also available in an 8-lead TO-5, and a 10-pin molded dual-in-line package.

The LH0002 is specified for operation over the −55°C to +125°C military temperature range. The LH0002C is specified for operation over the 0°C to +85°C temperature range.

applications

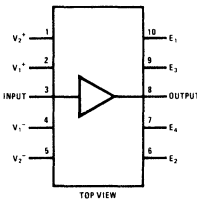
- Line driver
- 30 MHz buffer
- High speed D/A conversion
- Instrumentation buffer
- Precision current source

schematic and connection diagrams



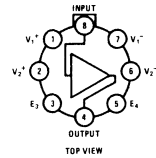
Pin numbers in parentheses denote pin connections for dual-in-line package.

Dual-In-Line Package



Order Number LH0002CN
See Package 16

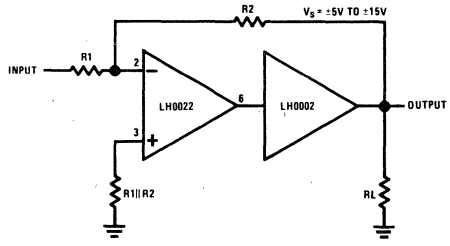
Metal Can Package



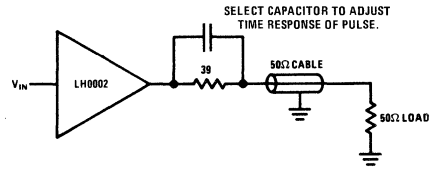
Order Number LH0002H or LH0002CH
See Package 9

typical applications

High Current Operational Amplifier



Line Driver



*Previously called NH0002/NH0002C

absolute maximum ratings

Supply Voltage		±22V
Power Dissipation Ambient		600 mW
Input Voltage (Equal to Power Supply Voltage)		
Storage Temperature Range		−65°C to +150°C
Operating Temperature Range	LH0002	−55°C to +125°C
	LH0002C	0°C to +85°C
Steady State Output Current		±100 mA
Pulsed Output Current (50 ms On/1 sec Off)		±400 mA

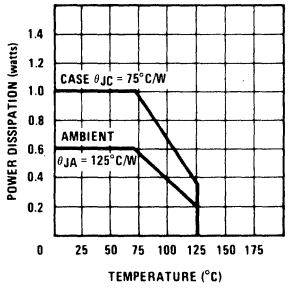
electrical characteristics (Note 1)

PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNITS
Voltage Gain	R_S = 10 kΩ, R_L = 1.0 kΩ V_{IN} = 3.0 V_{PP}, f = 1.0 kHz T_A = −55°C to 125°C	.95	.97		
AC Current Gain	V_{IN} = 1.0 V_{rms} f = 1.0 kHz		40		A/mA
Input Impedance	R_S = 200 kΩ, V_{IN} = 1.0 V_{rms}, f = 1.0 kHz, R_L = 1.0 kΩ	180	400	–	kΩ
Output Impedance	V_{IN} = 1.0 V_{rms}, f = 1.0 kHz R_L = 50Ω, R_S = 10 kΩ	–	6	10	Ω
Output Voltage Swing	R_L = 1.0 kΩ, f = 1.0 kHz	±10	±11	–	V
Output Voltage Swing	V_S = ±15V, V_{IN} = ±10V, R_L = 100Ω , T_A = 25°C	±9.5V			
DC Output Offset Voltage	R_S = 300Ω, R_L = 1.0 kΩ T_A = −55°C to 125°C	–	±10	±30	mV
DC Input Offset Current	R_S = 10 kΩ, R_L = 1.0 kΩ T_A = −55°C to 125°C	–	±6.0	±10	μA
Harmonic Distortion	V_{IN} = 5.0 V_{rms}, f = 1.0 kHz	–	0.1	–	%
Rise Time	R_L = 50Ω, ΔV_{IN} = 100mV		7	12	ns
Positive Supply Current	R_S = 10 kΩ, R_L = 1 kΩ	–	+6.0	+10.0	mA
Negative Supply Current	R_S = 10 kΩ, R_L = 1 kΩ	–	−6.0	−10.0	mA

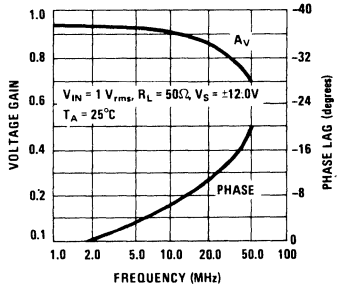
Note 1: Specification applies for T_A = 25°C with +12V on Pins 1 and 2; −12V on Pins 6 and 7 for the metal can package and +12V on Pins 1 and 2; −12V on Pins 4 and 5 for the dual-in-line package unless otherwise specified. The parameter guarantees for LH0002C apply over the temperature range of 0°C to +85°C, while parameters for the LH0002 are guaranteed over the temperature range −55°C to 125°C.

typical performance

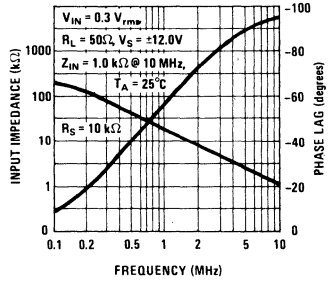
Maximum Power Dissipation



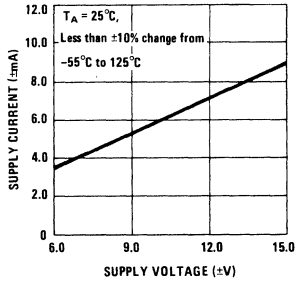
Frequency Response



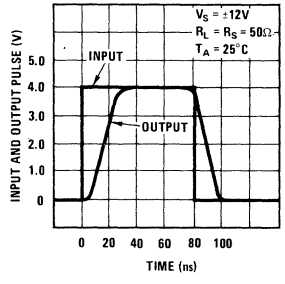
Input Impedance (Magnitude & Phase)



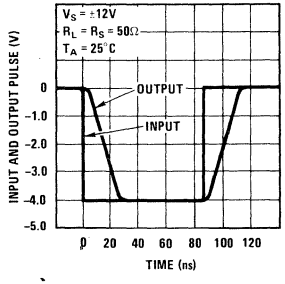
Supply Current



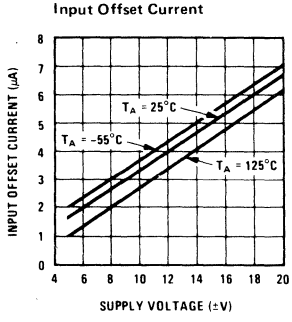
Positive Pulse



Negative Pulse



Input Offset Current



NATIONAL

Buffers

LH0033/LH0033C, LH0063/LH0063C
fast and damn fast buffer amplifiers

general description

The LH0033/LH0033C and LH0063/LH0063C are high speed, FET input, voltage follower/buffers designed to provide high current drive at frequencies from DC to over 100 MHz. The LH0033/LH0033C will provide ±10 mA into 1 kΩ loads (±100 mA peak) at slew rates of 1500V/μs. The LH0063/LH0063C will provide ±250 mA into 50Ω loads (±500 mA peak) at slew rates of up to 6000V/μs. In addition, both exhibit excellent phase linearity up to 20 MHz.

Both are intended to fulfill a wide range of buffer applications such as high speed line drivers, video impedance transformation, nuclear instrumentation amplifiers, op amp isolation buffer for driving reactive loads and high impedance input buffers for high speed A to D's and comparators. In addition, the LH0063/LH0063C can continuously drive 50Ω coaxial cables or be used as a diddle yoke driver for high resolution CRT displays. For additional applications information, see AN-48.

advantages

- Only +10V supply needed for 5 V_{P-P} video out
- Speed does not degrade system performance
- Wide data rate range for phase encoded systems
- Output drive adequate for most loads
- Single pre-calibrated package

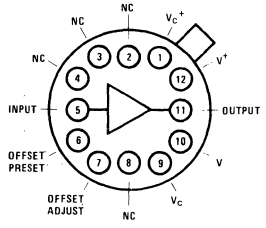
features

■ Damn fast (LH0063)	6000V/μs
■ Wide range single or dual supply operation	
■ Wide power bandwidth	DC to 100 MHz
■ High output drive	±10V with 50Ω load
■ Low phase non-linearity	2 degrees
■ Fast rise times	2 ns
■ High current gain	120 dB
■ High input resistance	10^{10} Ω

These devices are constructed using specially selected junction FET's and active laser trimming to achieve guaranteed performance specifications. The LH0033 and LH0063 are specified for operation from −55°C to +125°C; whereas, the LH0033C and LH0063C are specified from −25°C to +85°C. The LH0033/LH0033C is available in a 1.5W metal TO-8 package and a special 1/2 x 1 inch 8 pin ceramic dual-in-line package while the LH0063/LH0063C is available in a 5W 8-pin TO-3 package.

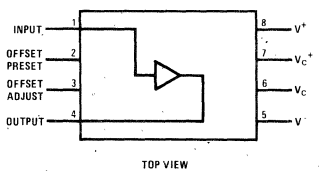
connection diagrams

LH0033/LH0033C
Metal Can Package



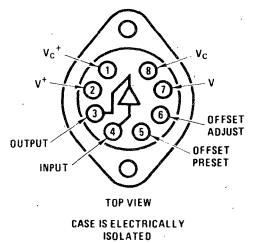
Order Number LH0033G or LH0033CG
See Package 6

LH0033/LH0033C
Dual-In-Line Package



Order Number LH0033J or LH0033CJ
See Package 12

LH0063/LH0063C
Metal Can Package



Order Number LH0063K or LH0063CK
See Package 14

absolute maximum ratings

Supply Voltage ($V^+ - V^-$)	40V
Maximum Power Dissipation (See Curves)	
LH0063/LH0063C	5W
LH0033/LH0033C	1.5W
Maximum Junction Temperature	175°C
Input Voltage	Equal to Supplies
Continuous Output Current	
LH0063/LH0063C	±250 mA
LH0033/LH0033C	±100 mA
Peak Output Current	
LH0063/LH0063C	±500 mA
LH0033/LH0033C	±250 mA
Operating Temperature Range	
LH0033 and LH0063	−55°C to +125°C
LH0033C and LH0063C	−25°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

dc electrical characteristics LH0033/LH0033C: (Note 1)

PARAMETER	CONDITIONS	LIMITS						UNITS
		LH0033			LH0033C			
		MIN	TYP	MAX	MIN	TYP	MAX	
Output Offset Voltage	R_S = 100 kΩ, T_C = 25°C		5	10		12	20	mV
	R_S = 100 kΩ			15			25	mV
Average Temperature Coefficient of Offset Voltage	R_S = 100 kΩ, $-55°C \leq T_C \leq 125°C$		50			50		µV/°C
Input Bias Current	T_C = 25°C		.05	.1		.05	.15	nA
				10			5	nA
Voltage Gain	V_{IN} = 1Vrms, f = 1 kHz, R_L = 1 kΩ, R_S = 100 kΩ	.97	.98	1	.96	.98	1	V/V
Input Impedance	R_L = 1 kΩ	10^{10}	10^{11}		10^{10}	10^{11}		Ω
Output Impedance	V_{IN} = 1Vrms, f = 1 kHz, R_S = 100 kΩ, R_L = 1 kΩ		6	10		6	10	Ω
Output Voltage Swing	R_L = 1 kΩ,	±12	±13		±12	±13		V
	R_L = 100Ω, T_C = 25°C	±9			±9			V
	V_S = ±5V, R_L = 1 kΩ		6			6		V_{P-P}
Supply Current	V_{IN} = 0V, V_S = ±15V		20	22		21	24	mA
	V_S = ±5V		18			18		mA
Power Consumption	V_{IN} = 0V, V_S = ±15V		600	660		630	720	mW
	V_S = ±5V		180			180		mW

ac electrical characteristics

LH0033/LH0033C (T_C = 25°C, V_S = ±15V, R_S = 50Ω, R_L = 1 kΩ)

PARAMETER	CONDITIONS	LIMITS						UNITS
		LH0033			LH0033C			
		MIN	TYP	MAX	MIN	TYP	MAX	
Slew Rate	V_{IN} = ±10V	1000	1500		1000	1400		V/µs
Bandwidth	V_{IN} = 1Vrms		100			100		MHz
Phase Non-Linearity	BW = 1 to 20 MHz		2			2		degrees
Rise Time	ΔV_{IN} = 0.5V		2.9			3.2		ns
Propagation Delay	ΔV_{IN} = 0.5V		1.2			1.5		ns
Harmonic Distortion			<0.1			<0.1		%

Note 1: Unless otherwise specified, these specifications apply for +15V applied to pins 1 and 12, −15V applied to pins 9 and 10, and pin 6 shorted to pin 7 for the LH0033/LH0033C. For the LH0063/LH0063C, specifications apply for ±15V applied to pins 1 and 2, −15V applied to pins 7 and 8, and pin 5 shorted to pin 6. Unless otherwise noted, specifications apply over a temperature range of $-55°C \leq T_C \leq +125°C$ for the LH0033 and LH0063; and $-25°C \leq T_C \leq +85°C$ for the LH0033C and LH0063C. Typical values shown are for T_C = 25°C.

dc electrical characteristics LH0063/LH0063C (Note 1)

PARAMETER	CONDITIONS	LIMITS						UNITS
		LH0063			LH0063C			
		MIN	TYP	MAX	MIN	TYP	MAX	
Output Offset Voltage	$R_S \leq 100\ k\Omega$, $T_C = 25°C$ $R_S \leq 100\ k\Omega$		10	25 100		10	50 100	mV mV
Average Temperature Coefficient of Output Offset Voltage	$R_S \leq 100\ k\Omega$		300			300		µV/°C
Input Bias Current	$T_C = 25°C$		.1	.2 10		.1	.2 5	nA nA
Voltage Gain	$V_{IN} = \pm 10V$, $R_S \leq 100\ k\Omega$, $R_L = 1\ k\Omega$	.96	.98	1	.96	.98	1	V/V
Voltage Gain	$V_{IN} = \pm 10V$, $R_S \leq 100\ k\Omega$, $R_L = 50\Omega$, $T_C = 25°C$	.94	.96	.98	.92	.96	.98	V/V
Input Resistance		10^{10}	10^{11}		10^{10}	10^{11}		Ω
Input Capacitance	Case Shorted to Output		8			8		pF
Output Impedance	$V_{OUT} = \pm 10V$, $R_S = 100\ k\Omega$		1	4		1	4	Ω
Output Current Swing	$V_{IN} = \pm 10V$, $R_S \leq 100\ k\Omega$	.2	.25		.2	.25		Amps
Output Voltage Swing	$R_L = 50\Omega$	±10	±13		±10	±13		V
Output Voltage Swing	$V_S = \pm 5V$, $R_L = 50\Omega$, $T_C = 25°C$	5	7		5	7		V_{P-P}
Supply Current	$T_C = 25°C$, $R_L = \infty$, $V_S = \pm 15V$		60	75		60	80	mA
Supply Current	$V_S = \pm 5V$		50			50		mA
Power Consumption	$T_C = 25°C$, $R_L = \infty$, $V_S = \pm 15V$		1.80	2.25		1.80	2.40	W
Power Consumption	$V_S = \pm 5V$		500			500		mW

ac electrical characteristics

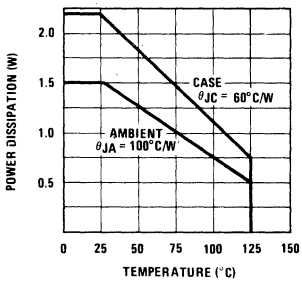
LH0063/LH0063C: ($T_C = 25°C$, $V_S = \pm 15V$, $R_S = 50\Omega$, $R_L = 50\Omega$)

PARAMETER	CONDITIONS	LIMITS						UNITS
		LH0063			LH0063C			
		MIN	TYP	MAX	MIN	TYP	MAX	
Slew Rate	$R_L = 1\ k\Omega$, $V_{IN} = \pm 10V$		6000			6000		V/µs
Slew Rate	$R_L = 50\Omega$, $V_{IN} = \pm 10V$ $T_C = 25°C$	2000	4000		2000	4000		V/µs
Bandwidth	$V_{IN} = 1$ Vrms		200			200		MHz
Phase Non-Linearity	BW = 1 to 20 MHz		2			2		degrees
Rise Time	$\Delta V_{IN} = .5V$		1.6			1.9		ns
Propagation Delay	$\Delta V_{IN} = .5V$		1.9			2.1		ns
Harmonic Distortion			<0.1			<0.1		%

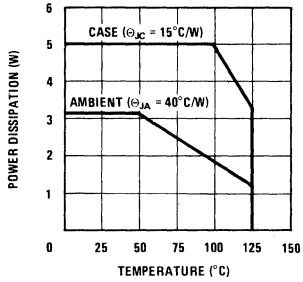
Note 1: Unless otherwise specified, these specifications apply for +15V applied to pins 1 and 12, −15V applied to pins 9 and 10, and pin 6 shorted to pin 7 for the LH0033/LH0033C. For the LH0063/LH0063C, specifications apply for +15V applied to pins 1 and 2, −15V applied to pins 7 and 8, and pin 5 shorted to pin 6. Unless otherwise noted, specifications apply over a temperature range of $-55°C \leq T_C \leq +125°C$ for the LH0033 and LH0063; and $-25°C \leq T_C \leq +85°C$ for the LH0033C and LH0063C. Typical values shown are for $T_C = 25°C$.

typical performance characteristics

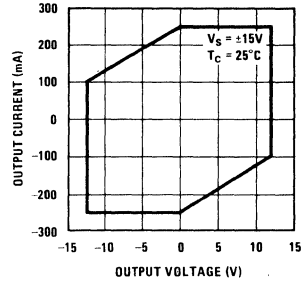
LH0033 Power Dissipation



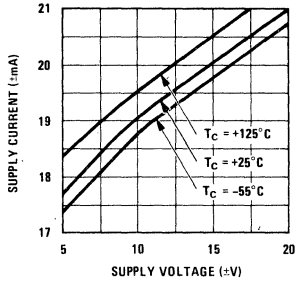
LH0063 Power Dissipation



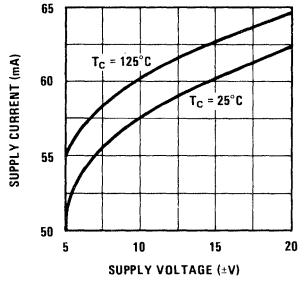
LH0063 DC Safe Operating Area



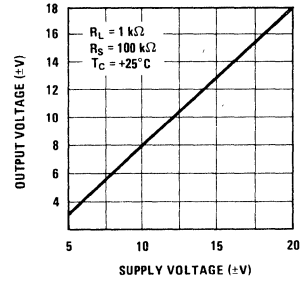
LH0033 Supply Current vs Supply Voltage



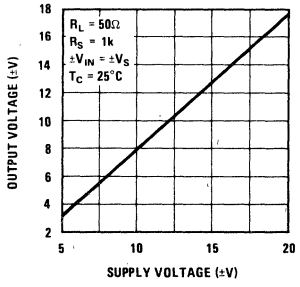
LH0063 Supply Current vs Supply Voltage



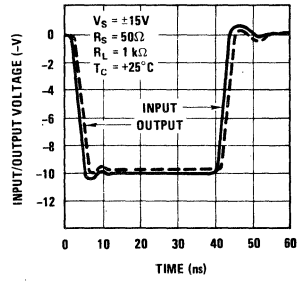
LH0033 Output Voltage vs Supply Voltage



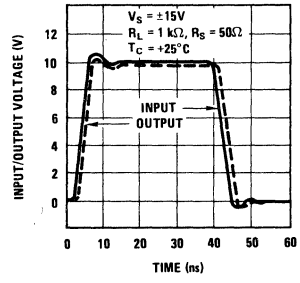
LH0063 Output Voltage vs Supply Voltage



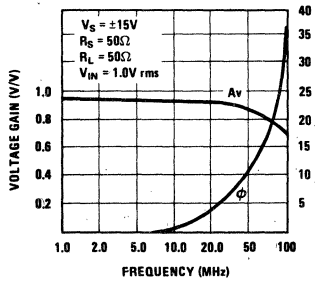
LH0033 Negative Pulse Response



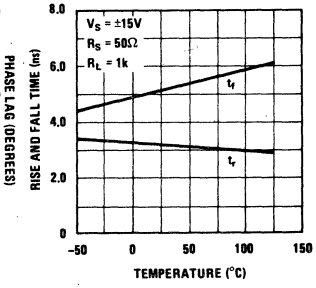
LH0033 Positive Pulse Response



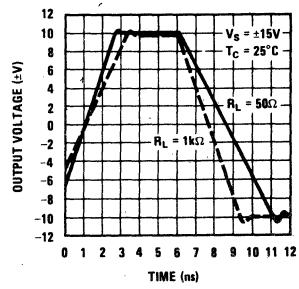
LH0033 Frequency Response



LH0033 Rise and Fall Time vs Temperature

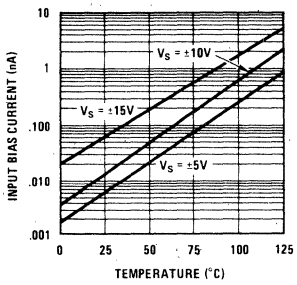


LH0063 Large Signal Pulse Response

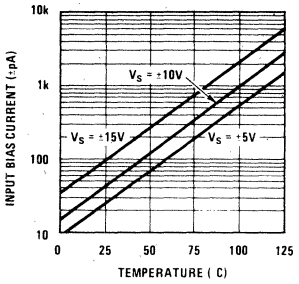


typical performance characteristics (con't)

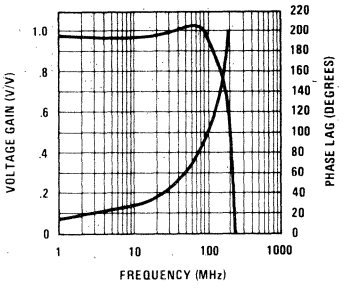
LH0033 Input Bias Current vs Temperature



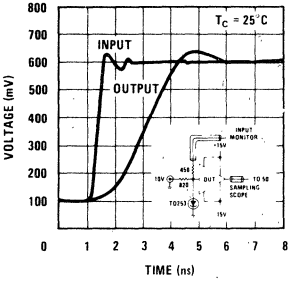
LH0063 Input Current



LH0063 Frequency Response



LH0063 Small Signal Rise Time



application hints

Recommended Layout Precautions: RF/video printed circuit board layout rules should be followed when using the LH0033 and LH0063 since they will provide power gain to frequencies over 100 MHz. Ground planes are recommended and power supplies should be decoupled at each device with low inductance capacitors. In addition, ground plane shielding may be extended to the metal case of the device since it is electrically isolated from internal circuitry. Alternatively the case should be connected to the output to minimize input capacitance.

Offset Voltage Adjustment: Both the LH0033's and LH0063's offset voltages have been actively trimmed by laser to meet guaranteed specifications when the offset preset pin is shorted to the offset adjust pin. This pre-calibration allows the devices to be used in most DC or AC applications without individually offset nulling each device. If offset null is desirable, it is simply obtained by leaving the offset preset pin open and connecting a trim pot of 100Ω for the LH0033 or 1 kΩ for the LH0063 between the offset adjust pin and V^- as illustrated in Figures 1 and 2.

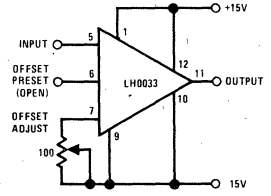


FIGURE 1. Offset Zero Adjust for LH0033 (Pin nos. shown for TO-8)

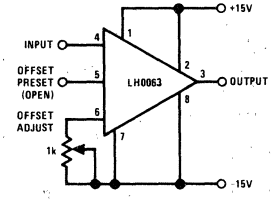


FIGURE 2. Offset Zero Adjust for LH0063

application hints (con't)

Operation from Single or Asymmetrical Power Supplies: Both device types may be readily used in applications where symmetrical supplies are unavailable or not desirable. A typical application might be an interface to a MOS shift register where $V^+ = +5V$ and $V^- = -12V$. In this case, an apparent output offset occurs due to the device's voltage gain of less than unity. This additional output offset error may be predicted by:

$$\Delta V_O \cong (1 - A_V) \frac{(V^+ - V^-)}{2} = .005\,(V^+ - V^-)$$

where:

A_V = No load voltage gain, typically .99

V^+ = Positive supply voltage

V^- = Negative supply voltage

For the above example, ΔV_O would be −35 mV. This may be adjusted to zero as described in Section 2. For AC coupled applications, no additional offset occurs if the DC input is properly biased as illustrated in the "typical applications" section.

Short Circuit Protection: In order to optimize transient response and output swing, output current limit has been omitted from the LH0033 and LH0063. Short circuit protection may be added by inserting appropriate value resistors between V^+ and V_C^+ pins and V^- and V_C^- pins as illustrated in Figures 3 and 4. Resistor values may be predicted by:

$$R_{LIM} \cong \frac{V^+}{I_{SC}} = \frac{V^-}{I_{SC}}$$

where: $I_{SC} \leq 100$ mA for LH0033

$I_{SC} \leq 250$ mA for LH0063

The inclusion of limiting resistors in the collectors of the output transistors reduces output voltage swing. Decoupling V_C^+ and V_C^- pins with capacitors to ground will retain full output swing for transient pulses. Alternate active current limit techniques that retain full DC output swing are shown in Figures 5, 6 and 7. In Figures 5 and 6, the current sources are saturated during normal operation thus apply full supply voltage to the V_C pins. Under fault conditions, the voltage decreases as required by the overload. For Figure 5:

$$R_{LIM} = \frac{V_{BE}}{I_{SC}} = \frac{.6V}{60\text{ mA}} = 10\Omega$$

In Figure 6, quad transistor arrays are used to minimize can count and:

$$R_{LIM} = \frac{V_{BE}}{1/3\ (I_{SC})} = \frac{.6V}{1/3\ (200\text{ mA})} = 8.2\Omega$$

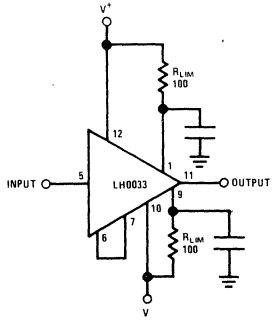


FIGURE 3. LH0033 Using Resistor Current Limiting

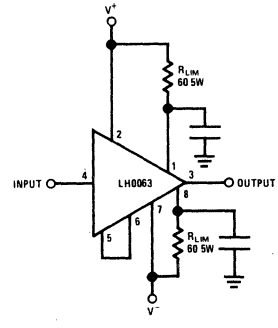


FIGURE 4. LH0063 Using Resistor Current Limiting

application hints (con't)

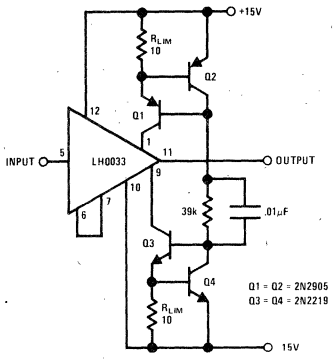


FIGURE 5. LH0033 Current Limiting Using Current Sources

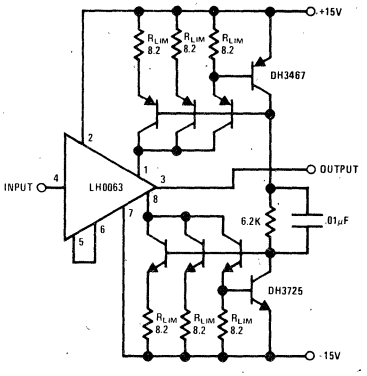


FIGURE 6. LH0063 Current Limiting Using Current Sources

Capacitive Loading: Both the LH0033 and LH0063 are designed to drive capacitive loads such as co-axial cables in excess of several thousand picofarads without susceptibility to oscillation. However, peak current resulting from $(C \times dv/dt)$ should be limited below absolute maximum peak current ratings for the devices.

Thus for the LH0033:

$$\left(\frac{\Delta V_{IN}}{\Delta t}\right) \times C_L \leq I_{OUT} \leq \pm 250\ mA$$

and for the LH0063:

$$\left(\frac{\Delta V_{IN}}{\Delta t}\right) \times C_L \leq I_{OUT} \leq \pm 500\ mA$$

application hints (con't)

In addition, power dissipation resulting from driving capacitative loads plus standby power should be kept below total package power rating:

$$P_{diss}_{pkg} \geq P_{DC} + P_{AC}$$

$$P_{diss}_{pkg} \geq (V^+ - V^-) \times I_S + P_{AC}$$

$$P_{AC} \cong (V_{P\text{-}P})^2 \times f \times C_L$$

where $V_{P\text{-}P}$ = Peak-to-peak output voltage swing

f = frequency

C_L = Load Capacitance

Operation Within an Op Amp Loop: Both devices may be used as a current booster or isolation buffer within a closed loop with op amps such as LH0032, LH0062, or LM118. An isolation resistor of 47Ω should be used between the op amp output and the input of LH0033. The wide bandwidths and high slew rates of the LH0033 and LH0063 assure that the loop has the characteristics of the op amp and that additional rolloff is not required.

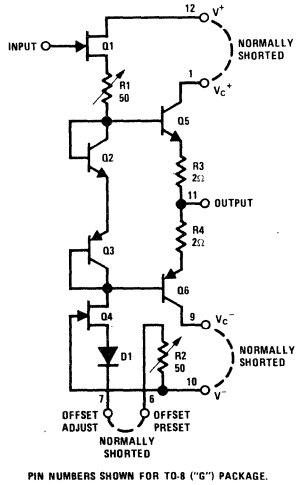
Hardware: In order to utilize the full drive capabilities of both devices, each should be mounted with a heat sink particularly for extended temperature operation. The cases of both are isolated from the circuit and may be connected to system chassis.

ACHTUNG!

Power supply bypassing is necessary to prevent oscillation with both the LH0033 and LH0063 in all circuits. Low inductance ceramic disc capacitors with the shortest practical lead lengths must be connected from each supply lead (within < ¼ to ½" of the device package) to a ground plane. Capacitors should be one or two 0.1μF in parallel for the LH0033; adding a 4.7μF solid tantalum capacitor will help in troubleosme instances. For the LH0063, two 0.1μF ceramic and one 4.7μF solid tantalum capacitors in parallel will be necessary on each supply lead.

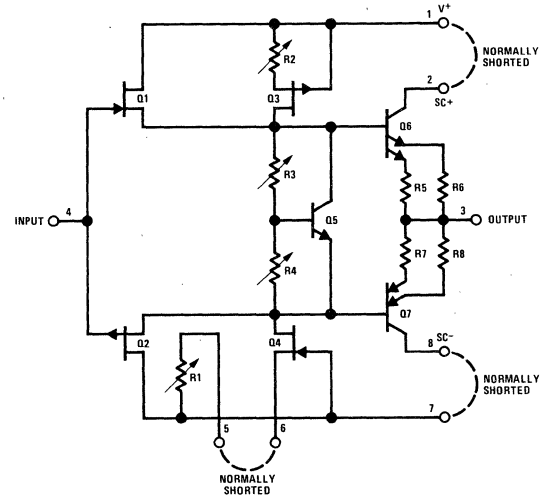
schematic diagrams

LH0033/LH0033C



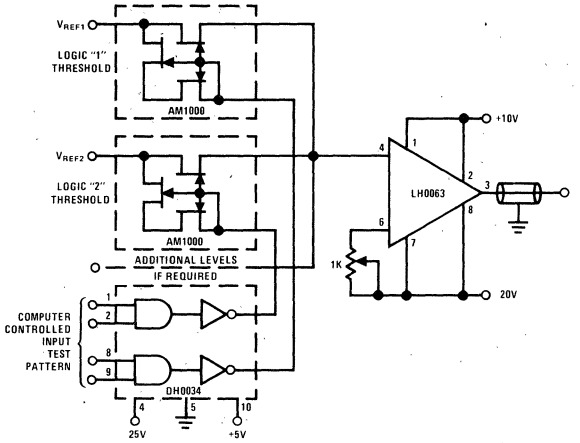
PIN NUMBERS SHOWN FOR TO-8 ("G") PACKAGE.

LH0063/LH0063C

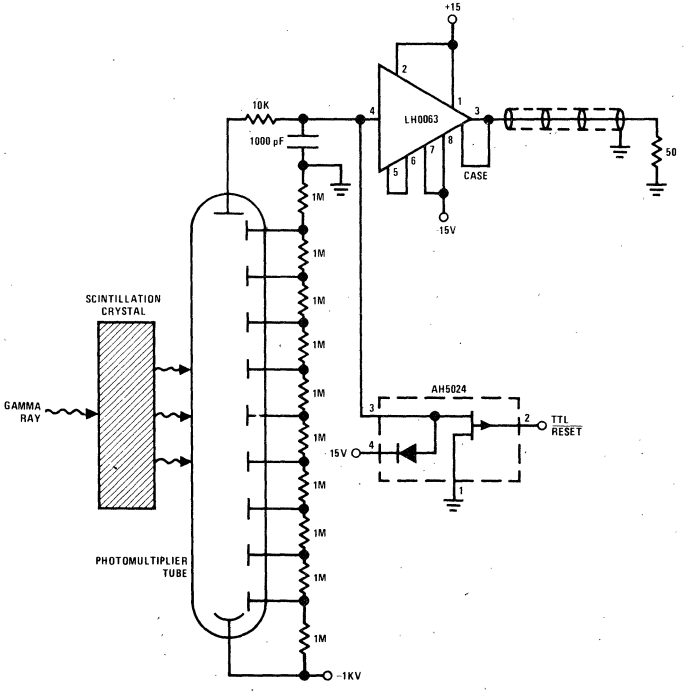


typical applications

High Speed Automatic Test Equipment
Forcing Function Generator

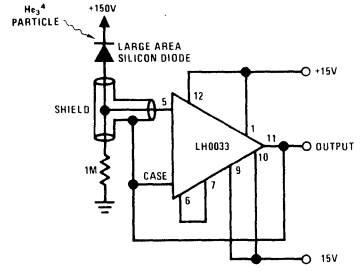


Gamma Ray Pulse Integrator

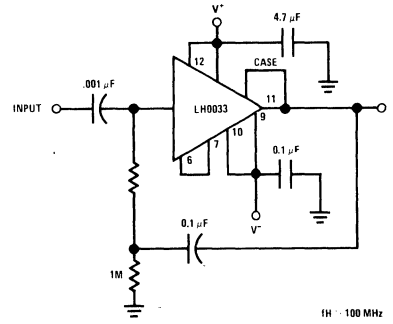


typical applications (con't)

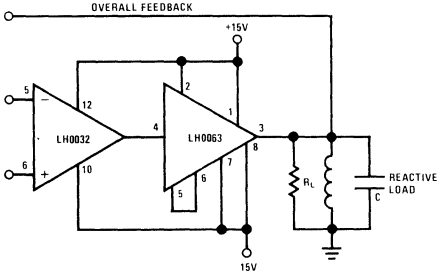
Nuclear Particle Detector



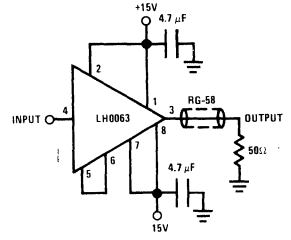
High Input Impedance AC Coupled Amplifier



Isolation Buffer



Coaxial Cable Driver



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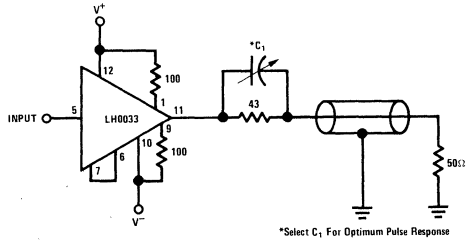
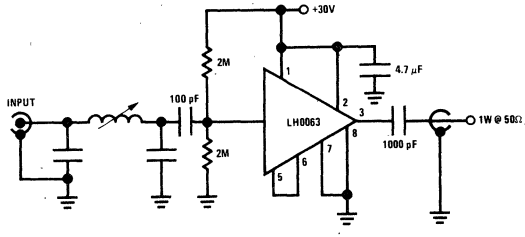


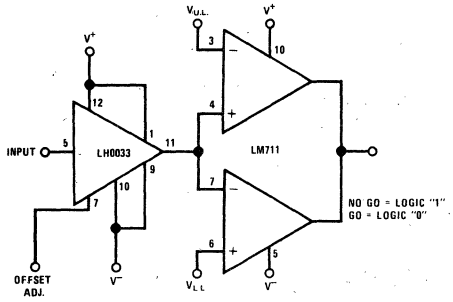
*Select C_1 For Optimum Pulse Response

1W CW Final Amplifier

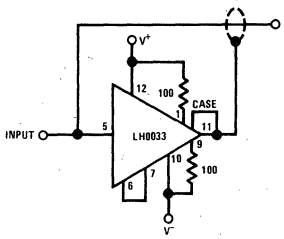


typical applications (con't)

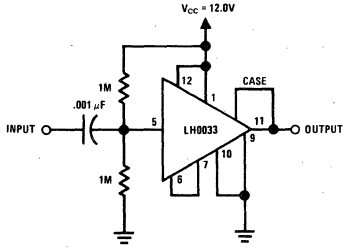
High Input Impedance Comparator With Offset Adjust



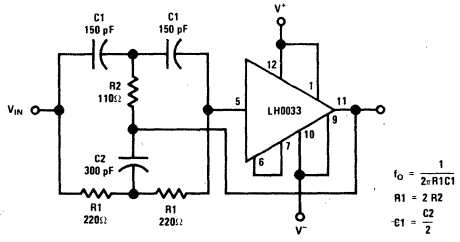
Instrumentation Shield/Line Driver



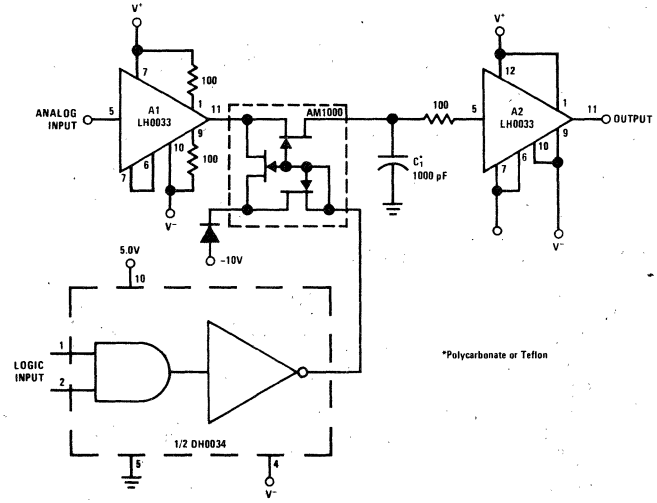
Single Supply AC Amplifier



4.5 MHz Notch Filter



High Speed Sample & Hold



NATIONAL

Buffers

LH2110/LH2210/LH2310 dual voltage follower

general description

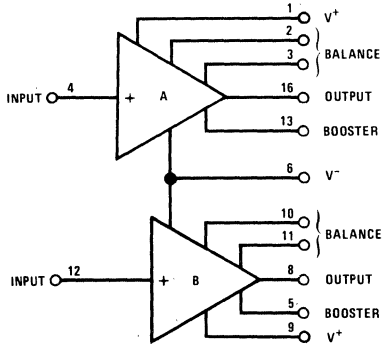
The LH2110 series of dual voltage followers are two LM110 type followers in a single hermetic package. Featuring all the same performance characteristics of the single, these duals offer in addition closer thermal tracking, lower weight, reduced insertion cost and smaller size than two singles. For additional information, see the LM110 data sheet and National's Linear Application Notebook.

The LH2110 is specified for operation over the −55°C to +125°C military temperature range. The LH2210 is specified for operation over the −25°C to +85°C temperature range. The LH2310 is specified for operation over the 0°C to +70°C temperature range.

features

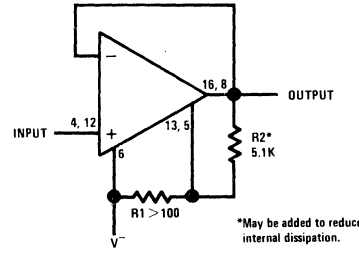
- Low input current 1 nA
- High input resistance 10^{10} ohms
- High slew rate 30V/μs
- Wide bandwidth 20 MHz
- Wide operating supply range ±5V to ±18V
- Output short circuit proof

connection diagram

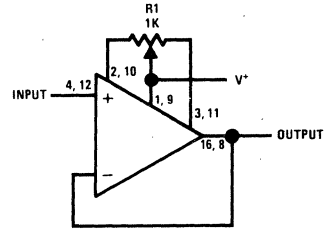


Order Number LH2111D or LH2211D or LH2311D
See Package 2

auxiliary circuits



Increasing Negative Swing Under Load



Offset Balancing Circuit

absolute maximum ratings

Supply Voltage	±18V	Operating Temperature Range LH2110	−55°C to 125°C
Power Dissipation (Note 1)	500 mW	LH2210	−25°C to 85°C
Input Voltage (Note 2)	±15V	LH2310	0°C to 70°C
Output Short Circuit Duration (Note 3)	Continuous	Storage Temperature Range	−65°C to 150°C
		Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics Each side (Note 4)

PARAMETER	CONDITIONS	LIMITS			UNITS
		LH2110	LH2210	LH2310	
Input Offset Voltage	$T_A = 25°C$	4.0	4.0	7.5	mV Max
Input Bias Current	$T_A = 25°C$	3.0	3.0	7.0	nA Max
Input Resistance	$T_A = 25°C$	10^{10}	10^{10}	10^{10}	Ω Min
Input Capacitance		1.5	1.5	1.5	pF Typ
Large Signal Voltage Gain	$T_A = 25°C$, $V_S = ±15V$ $V_{OUT} = ±10V$, $R_L = 8\ kΩ$	.999	.999	.999	V/V Min
Output Resistance	$T_A = 25°C$	2.5	2.5	2.5	Ω Max
Supply Current (Each Amplifier)	$T_A = 25°C$	5.5	5.5	5.5	mA Max
Input Offset Voltage		6.0	6.0	10	mV Max
Offset Voltage	$-55°C \leq T_A \leq 85°C$	6	6	10	μV/°C Typ
Temperature Drift	$T_A = 125°C$	12	12	–	μV/°C Typ
Input Bias Current		10	10	10	nA Max
Large Signal Voltage Gain	$V_S = ±15V$, $V_{OUT} = ±10V$ $R_L = 10\ kΩ$	.999	.999	.999	V/V Min
Output Voltage Swing (Note 5)	$V_S = ±15V$, $R_L = 10\ kΩ$	±10	±10	±10	V Min
Supply Current (Each Amplifier)	$T_A = 125°C$	4.0	4.0	–	mA Max
Supply Voltage Rejection Ratio	$±5V \leq V_S \leq ±18V$	70	70	70	dB Min

Note 1: The maximum junction temperature of the LH2110 is 150°C, while that of the LH2210 is 100°C and the LH2310 is 85°C. For operating at elevated temperatures, devices in the flat package, the derating is based on a thermal resistance of 185 C/W when mounted on a 1/16-inch-thick epoxy glass board with 0.03-inch-wide, 2-ounce copper conductors. The thermal resistance of the dual-in-line package is 100 C/W, junction to ambient

Note 2: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Note 3: Continuous short circuit is allowed for case temperatures to 125°C and ambient temperatures to 70°C. It is necessary to insert a resistor greater than 2 kΩ in series with the input when the amplifier is driven from low impedance sources to prevent damage when the output is shorted.

Note 4: These specifications apply for $±5V < V_S < ±18V$ and $-55°C < T_A < 125°C$, unless otherwise specified. With the LM210, however, all temperature specifications are limited to $-25°C < T_A < 85°C$ and for the LH2310, all temperature specifications are limited to $0°C < T_A < 70°C$.

Note 5: Increased output swing under load can be obtained by connecting an external resistor between the booster and V^- terminals.

NATIONAL

Sample and Hold Amplifiers

LH0023/LH0023C, LH0043/LH0043C sample and hold circuits

general description

The LH0023/LH0023C and LH0043/LH0043C are complete sample and hold circuits including input buffer amplifier, FET output amplifier, analog signal sampling gate, TTL compatible logic circuitry and level shifting. They are designed to operate from standard ±15V DC supplies, but provision is made on the LH0023/LH0023C for connection of a separate +5V logic supply in minimum noise applications. The principal difference between the LH0023/LH0023C and the LH0043/LH0043C is a 10:1 trade-off in performance on sample accuracy vs sample acquisition time. Devices are pin compatible except that TTL logic is inverted between the two types.

The LH0023/LH0023C and LH0043/LH0043C are ideally suited for a wide variety of sample and hold applications including data acquisition, analog to digital conversion, synchronous demodulation, and automatic test setup. They offer significant cost and size reduction over equivalent module or discrete designs. Each device is available in a hermetic TO-8 package and are completely specified over both full military and instrument temperature ranges.

The LH0023 and LH0043 are specified for operation over the −55°C to +125°C military temperature range. The LH0023C and LH0043C are specified for operation over the −25°C to +85°C temperature range.

For information on other National analog products, see *Available Linear Applications Literature.*

features

LH0023/LH0023C

- Sample accuracy—0.01% max
- Hold drift rate—0.5 mV/sec typ
- Sample acquisition time—100 μs max for 20V
- Aperture time—150 ns typ
- Wide analog range—±10V min
- Logic input—TTL/DTL
- Offset adjustable to zero with single 10k pot
- Output short circuit proof

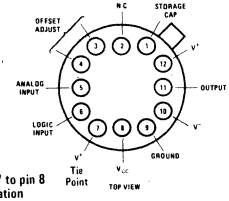
features

LH0043/LH0043C

- Sample acquisition time—15 μs max for 20V
  4 μs typ for 5V
- Aperture time—20 nS typ
- Hold drift rate—1 mV/sec typ
- Sample accuracy—0.1% max
- Wide analog range—±10V min
- Logic input—TTL/DTL
- Offset adjustable to zero with single 10k pot
- Output short circuit proof

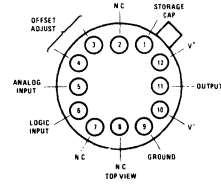
block and connection diagrams

LH0023/LH0023C

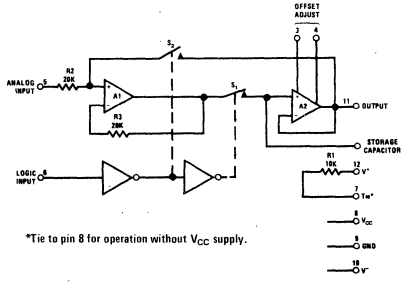


Tie pin 7 to pin 8 for operation without 5V supply.

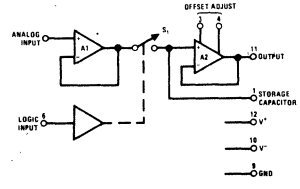
LH0043/LH0043C



Order Number LH0023G or LH0023CG or LH0043G or LH0043CG
See Package 6



*Tie to pin 8 for operation without V_{CC} supply.



absolute maximum ratings

Supply Voltage (V^+ and V^-)		±20V
Logic Supply Voltage (V_{CC})	LH0023, LH0023C	+7.0V
Logic Input Voltage (V_6)		+5.5V
Analog Input Voltage (V_5)		±15V
Power Dissipation		See graph
Output Short Circuit Duration		Continuous
Operating Temperature Range	LH0023, LH0043	−55°C to +125°C
	LH0023C, LH0043C	−25°C to +85°C
Storage Temperature Range		−65°C to +150°C
Lead Soldering (10 sec)		300°C

electrical characteristics LH0023/LH0023C (Note 1)

PARAMETER	CONDITIONS	LIMITS						UNITS
		LH0023			LH0023C			
		MIN	TYP	MAX	MIN	TYP	MAX	
Sample (Logic "1") Input Voltage	V_{CC} = 4.5V	2.0			2.0			V
Sample (Logic "1") Input Current	V_6 = 2.4V, V_{CC} = 5.5V			5.0			5.0	μA
Hold (Logic "0") Input Voltage	V_{CC} = 4.5V			0.8			0.8	V
Hold (Logic "0") Input Current	V_6 = 0.4V, V_{CC} = 5.5V			0.5			0.5	mA
Analog Input Voltage Range		±10	±11		±10	±11		V
Supply Current – I_{10}	V_5 = 0V, V_6 = 2V, V_{11} = 0V		4.5	6		4.5	6	mA
Supply Current – I_{12}	V_5 = 0V, V_6 = 0.4V, V_{11} = 0V		4.5	6		4.5	6	mA
Supply Current – I_8	V_8 = 5.0V, V_5 = 0		1.0	1.6		1.0	1.6	mA
Sample Accuracy	V_{OUT} = ±10V (Full Scale)		0.002	0.01		0.002	0.02	%
DC Input Resistance	Sample Mode	500	1000		300	1000		kΩ
	Hold Mode	20	25		20	25		kΩ
Input Current – I_5	Sample Mode		0.2	1.0		0.3	1.5	μA
Input Capacitance			3.0			3.0		pF
Leakage Current – pin 1	V_5 = ±10V; V_{11} = ±10V, T_A = 25°C		100	200		200	500	pA
	V_5 = ±10V; V_{11} = ±10V		0.6	1.0		1.0	2	nA
Drift Rate	V_{OUT} = ±5V, C_S = 0.01 μF, T_A = 25°C		0.5			0.5		mV/s
Drift Rate	V_{OUT} = ±10V, C_S = 0.01 μF, T_A = 25°C		10	20		20	50	mV/s
Drift Rate	V_{OUT} = ±10V, C_S = 0.01 μF			0.1			0.2	mV/ms
Aperture Time			150			150		ns
Sample Acquisition Time	ΔV_{OUT} = 20V, C_S = 0.01 μF		50	100		50	100	μs
Output Amplifier Slew Rate		1.5	3.0		1.5	3.0		V/μs
Output Offset Voltage (without null)	$R_S \leq$ 10k, V_5 = 0V, V_6 = 0V			±20			±20	mV
Analog Voltage Output Range	$R_L \geq$ 1k, T_A = 25°C	±10	±11		±10	±11		V
	$R_L \geq$ 2k	±10	±12		±10	±12		V

NOTE 1: Unless otherwise noted, these specifications apply for V^+ = +15V, V_{CC} = +5V, V^- = −15V, pin 9 grounded, a 0.01 μF capacitor connected between pin 1 and ground over the temperature range −55°C to +125°C for the LH0023, and −25°C to 85°C for the LH0023C. All typical values are for T_A = 25°C.

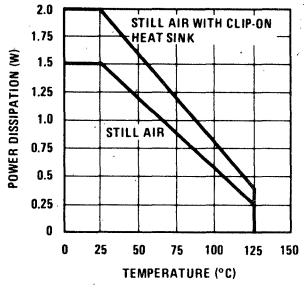
electrical characteristics LH0043/LH0043C: (Note 2)

PARAMETER	CONDITIONS	LIMITS						UNITS
		LH0043			LH0043C			
		MIN	TYP	MAX	MIN	TYP	MAX	
Hold (Logic "1") Input Voltage		2.0			2.0			V
Hold (Logic "1") Input Current	V_6 = 2.4V			5.0			5.0	μA
Sample (Logic "0") Input Voltage				0.8			0.8	V
Sample (Logic "0") Input Current	V_6 = 0.4V			1.5			1.5	mA
Analog Input Voltage Range		±10	±11		±10	±11		V
Supply Current	V_5 = 0V, V_6 = 2V, V_{11} = 0V V_5 = 0V, V_6 = 0.4V, V_{11} = 0V		20 14	22 18		20 14	22 18	mA mA
Sample Accuracy	V_{OUT} = ±10V (Full Scale)		0.02	0.1		0.02	0.3	%
DC Input Resistance	T_C = 25°C	10^{10}	10^{12}		10^{10}	10^{12}		Ω
Input Current – I_5			1.0	5.0		2.0	10.0	nA
Input Capacitance			1.5			1.5		pF
Leakage Current– pin 1	V_5 = ±10V; V_{11} = ±10, T_C = 25°C V_5 = ±10V; V_{11} = ±10V		10 10	25 25		20 2	50 5	pA nA
Drift Rate	V_{OUT} = ±10V, C_S = 0.001 μF, T_A = 25°C		10	25		20	50	mV/s
Drift Rate	V_{OUT} = ±10V, C_S = 0.001 μF		10	25		2	5	mV/ms
Drift Rate	V_{OUT} = ±10V, C_S = 0.01 μF, T_A = 25°C		1	2.5		2	5	mV/s
Drift Rate	V_{OUT} = ±10V, C_S = 0.01 μF		1	2.5		0.2	0.5	mV/ms
Aperture Time			20	60		20	60	ns
Sample Acquisition Time	ΔV_{OUT} = 20V, C_S = 0.001 μF ΔV_{OUT} = 20V, C_S = 0.01 μF ΔV_{OUT} = 5V, C_S = 0.001 μF		10 30 4	15 50		10 30 4	15 50	μs μs μs
Output Amplifier Slew Rate	V_{OUT} = 5V, C_S = 0.001 μF	1.5	3.0		1.5	3.0		V/μs
Output Offset Voltage (without null)	$R_S \leq$ 10k, V_5 = 0V, V_6 = 0V			±40			±40	mV
Analog Voltage Output Range	$R_L \geq$ 1k, T_A = 25°C $R_L \geq$ 2k	±10 ±10	±11 ±12		±10 ±10	±11 ±12		V V

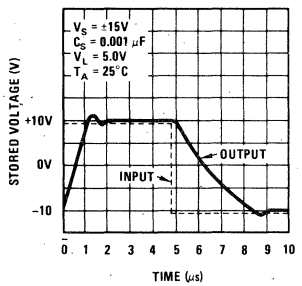
Note 2: Unless otherwise noted, these specifications apply for V^+ = +15V, V^- = –15V, pin 9 grounded, a 5000 pF capacitor connected between pin 1 and ground over the temperature range –55°C to +125°C for the LH0043, and –25°C to 85°C for the LH0043C. All typical values are for T_C = 25°C.

typical performance characteristics

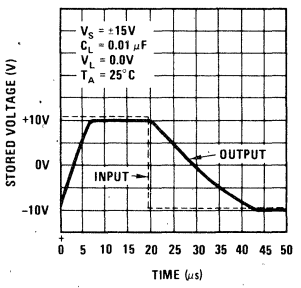
Power Dissipation



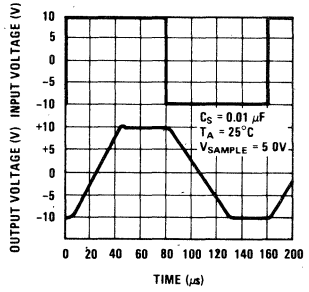
Sample Acquisition Time—LH0043



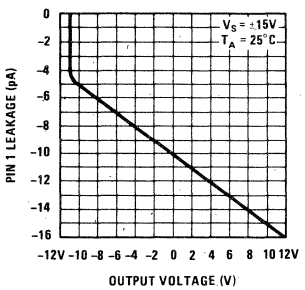
Sample Acquisition Time—LH0043



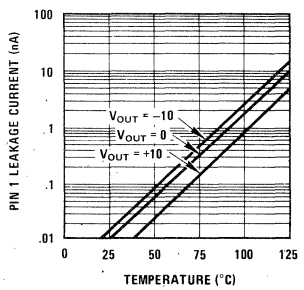
Sample Acquisition Time—LH0023



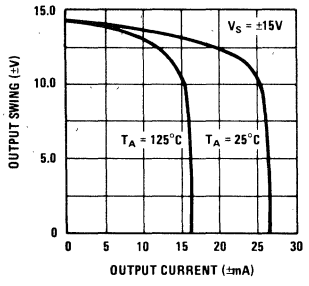
Pin 1 Leakage Current vs Output Voltage



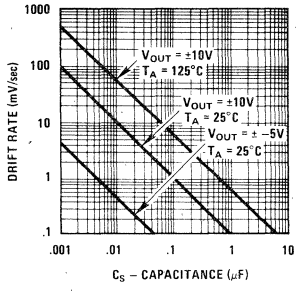
Pin 1 Leakage Current vs Temperature



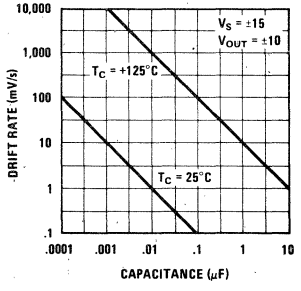
Output Current Limiting



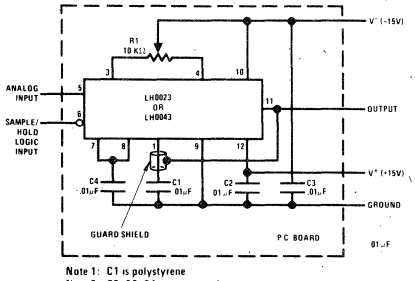
Drift Rate vs Capacitance



Drift vs Capacitance (LH0043)



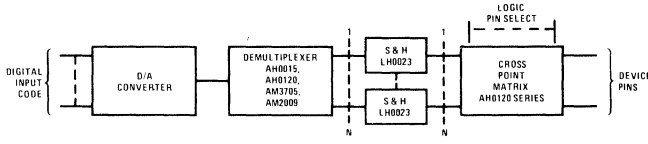
typical applications



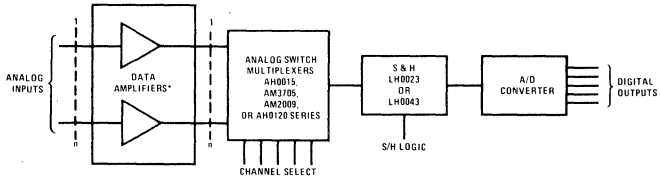
Note 1: C1 is polystyrene
Note 2: C2, C3, C4 are ceramic disc
Note 3: Jumper 7–8 and C4 not required for LH0043
Note 4: R1 optional if zero trim is required

How to Build a Sample and Hold Module

typical applications (con't)

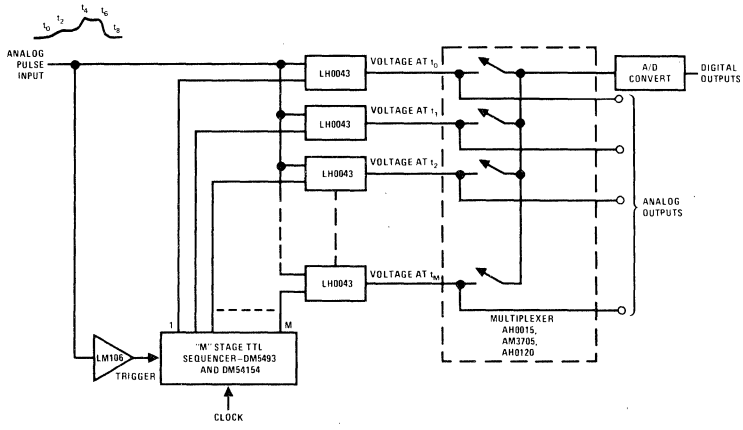


Forcing Function Setup for Automatic Test Gear

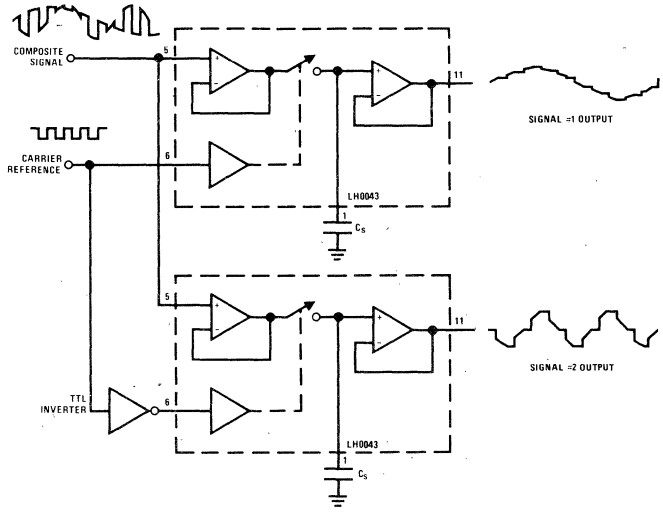


*See op amp selection guide for details. Most popular types include LH0052, LH1725, LM108, LM122 and LM116.

Data Acquisition System



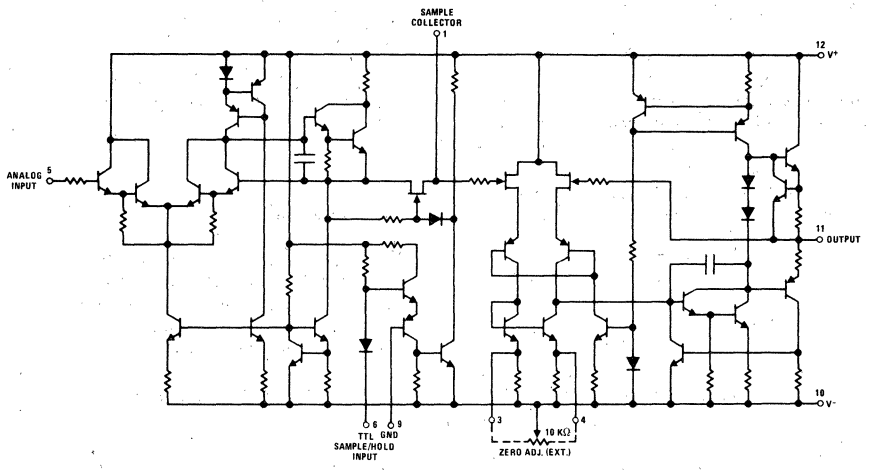
Single Pulse Sampler



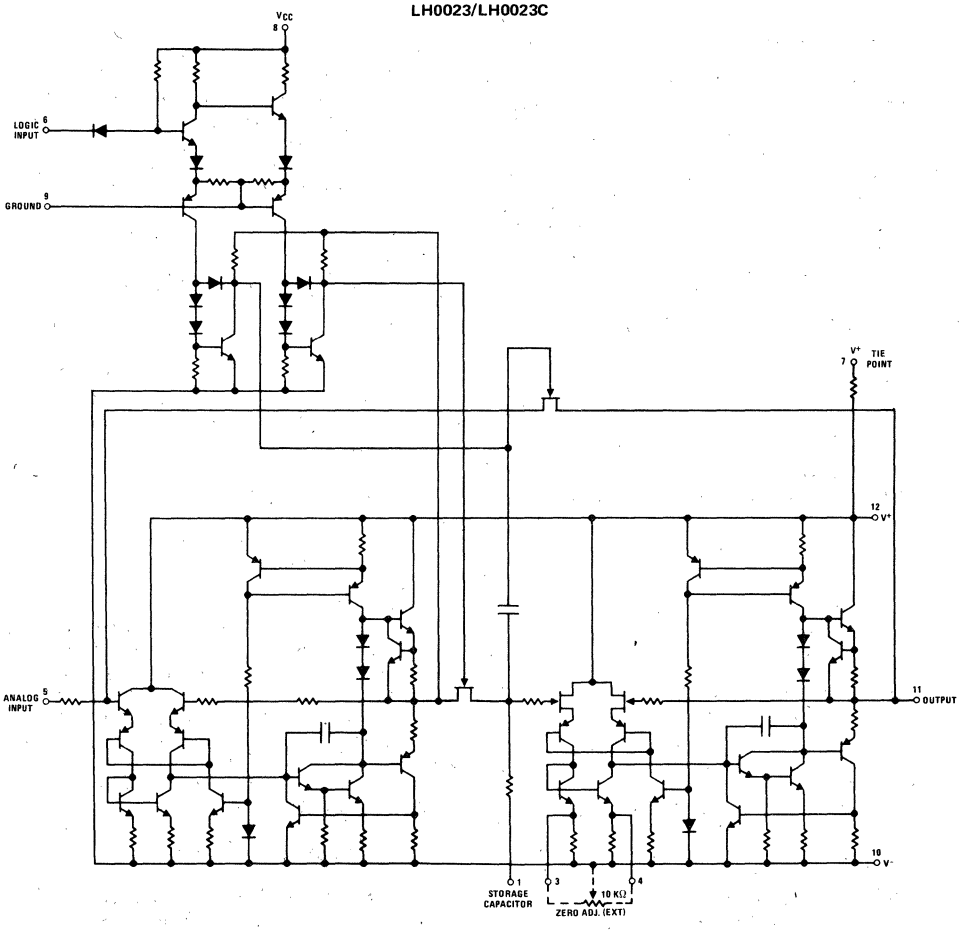
Two Channel Double Sideband Demodulator

schematic diagrams

LH0043/LH0043C



LH0023/LH0023C



applications information

1.0 Drift Error Minimization

In order to minimize drift error, care in selection of C_S and layout of the printed circuit board is required. The capacitor should be of high quality Teflon, polycarbonate, or polystyrene construction. Board cleanliness and layout are critical particularly at elevated temperatures. See AN-63 for detailed recommendations. A guard conductor connected to the output surrounding the storage node (pin 1) will be helpful in meeting severe environmental conditions which would otherwise cause leakage across the printed circuit board.

2.0 Capacitor Selection

The size of the capacitor is dictated by the required drift rate and acquisition time. The drift is determined by the leakage current at pin 1 and may be calculated by $\frac{dV}{dt} = \frac{I_L}{C_S}$, where I_L is the total leakage current at pin 1 of the device, and C_S is the value of the storage capacitor.

2.1 Capacitor Selection – LH0023

At room temperature leakage current for the LH0023 is approximately 100 pA. A drift rate of 10 mV/sec would require a 0.01 μF capacitor.

For values of C_S up to 0.01 μF the acquisition time is limited by the slew rate of the input buffer amplifier, A1, typically 0.5 V/μs. Beyond this point, current availability to charge C_S also enters the picture. The acquisition time is given by:

$$t_A \cong \sqrt{\frac{2\Delta e_O RC_S}{0.5 \times 10^6}} = 2 \times 10^{-3}\sqrt{\Delta e_O RC_S}$$

where: R = the internal resistance in series with C_S

Δe_O = change in voltage sampled

An average value for R is approximately 600 ohms. The expression for t_A reduces to:

$$t_A \cong \sqrt{\frac{\Delta e_O C_S}{20}}$$

For a –10V to +10V change and C_S = .05 μF, acquisition time is typically 50 μs.

2.2 Capacitor Selection—LH0043

At 25°C case temperature, the leakage current for the LH0043G is approximately 10 pA, so a drift rate of 5 mV/s would require a capacitor of $C_S = 10 \cdot 10^{-12}/5 \cdot 10^{-3} = 2000$ pF or larger.

For values of C_S below about 5000 pF, the acquisition time of the LH0043G will be limited by the slew rate of the output amplifier (the signal will be acquired, in the sense that the voltage will be stored on the capacitor, in much less time as dictated by the slew rate and current capacity of the input amplifier, but it will not be available at the output). For larger values of storage capacitance, the limitation is the current sinking capability of the input amplifier, typically 10 mA. With C_S = 0.01 μF, the slew rate can be estimated by $\frac{dV}{dt} = \frac{10 \cdot 10^{-3}}{0.01 \cdot 10^{-6}} = 1$V/$\mu$s or a slewing time for a 5 volt signal change of 5μs.

3.0 Offset Null

Provision is made to null both the LH0023 and LH0043 by use of a 10k pot between pins 3 and 4. Offset null should be accomplished in the sample mode at one half the input voltage range for minimum average error.

4.0 Switching Spike Minimization—LH0043

A capacitive divider is formed by the storage capacitor and the capacitance of the internal FET switch which causes a small error current to be injected into the storage capacitor at the termination of the sample interval. This can be considered a negative DC offset and nulled out as described in (3.0), or the transient may be nulled by coupling an equal but opposite signal to the storage capacitor. This may be accomplished by connecting a capacitor of about 30 pF (or a trimmer) between the logic input (pin 6) and the storage capacitor (pin 1). Note that this capacitor must be chosen as carefully as the storage capacitor itself with respect to leakage. The LH0023 has switch spike minimization circuitry built into the device.

5.0 Elimination of the 5V Logic Supply—LH0023

The 5V logic supply may be eliminated by shorting pin 7 to pin 8 which connects a 10k dropping resistor between the +15V and V_C. Decoupling pin 8 to ground through 0.1 μF disc capacitor is recommended in order to minimize transients in the output.

6.0 Heat Sinking

The LH0023 and LH0043G may be operated without damage throughout the military temperature range of –55 to +125°C (–25 to +85°C for the LH0023CG and LH0043CG) with no explicit heat sink, however power dissipation will cause the internal temperature to rise above ambient. A simple clip-on heat sink such as Wakefield #215–1.9 or equivalent will reduce the internal temperature about 20°C thereby cutting the leakage current and drift rate by one fourth at max. ambient. There is no internal electrical connection to the case, so it may be mounted directly to a grounded heat sink.

7.0 Theory of Operation—LH0023

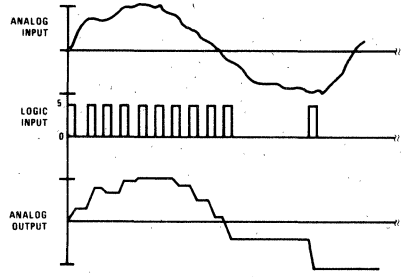
The LH0023/LH0023C is comprised of input buffer amplifier, A1, analog switches, S1 and S2, a

applications information (con't)

TTL to MOS level translator, and output buffer amplifier, A2. In the "sample" mode, the logic input is raised to logic "1" ($V_6 \geq 2.0V$) which closes S1 and opens S2. Storage capacitor, C_S, is charged to the input voltage through S1 and the output slews to the input voltage. In the "hold" mode, the logic input is lowered to logic "0" ($V_6 \leq 0.8V$) opening S1 and closing S2. C_S retains the sample voltage which is applied to the output via A2. Since S1 is open, the input signal is overridden, and leakage across the MOS switch is therefore minimized. With S1 open, drift is primarily determined by input bias current of A2, typically 100 pA at 25°C.

7.1 Theory of Operation—LH0043

The LH0043/LH0043C is comprised of input buffer amplifier A1, FET switch S1 operated by a TTL compatible level translator, and output buffer amplifier A2. To enter the "sample" mode, the logic input is taken to the TTL logic "0" state (V_6 = 0.8V) which commands the switch S1 closed and allows A1 to make the storage capacitor voltage equal to the analog input voltage. In the "hold" mode (V_6 = 2.0V), S1 is opened isolating the storage capacitor from the input and leaving it charged to a voltage equal to the last analog input voltage before entering the hold mode. The storage capacitor voltage is brought to the output by low leakage amplifier A2.



8.0 Definitions

V_5: The voltage at pin 5, e.g., the analog input voltage.

V_6: The voltage at pin 6, e.g., the logic control input signal.

V_{11}: The voltage at pin 11, e.g., the output signal.

T_A: The temperature of the ambient air.

T_C: The temperature of the device case at the center of the bottom of the header.

Acquisition Time:
The time required for the output (pin 11) to settle within the rated accuracy after a specified input change is applied to the input (pin 5) with the logic input (pin 6) in the low state.

Aperture Time:
The time indeterminacy when switching from sample mode to hold including the delay from the time the mode control signal (pin 6) passes through its threshold (1.4 volts) to the time the circuit actually enters the hold mode.

Output Offset Voltage:
The voltage at the output terminal (pin 11) with the analog input (pin 5) at ground and logic input (pin 6) in the "sample" mode. This will always be adjustable to zero using a 10k pot between pins 3 and 4 with the wiper arm returned to V^-.

Sample and Hold Amplifiers

LH0053/LH0053C high speed sample and hold amplifier

general description

The LH0053/LH0053C is a high speed sample and hold circuit capable of acquiring a 20V step signal in under 5.0μs.

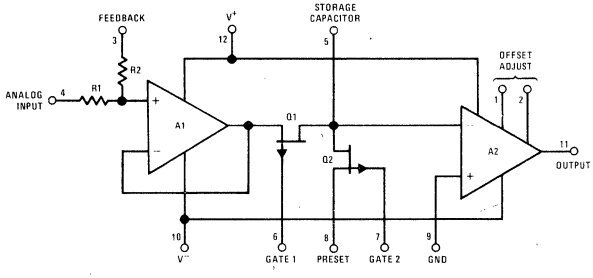
The device is ideally suited for a variety of high speed data acquisition applications including analog buffer memories for A to D conversion and synchronous demodulation.

An auxiliary switch within the device extends its usefulness in applications such as preset integrators.

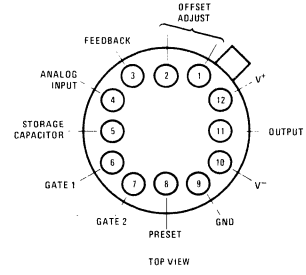
features

- Sample acquisition time 5.0μs max for 20V signal
- FET switch for preset or reset function
- Sample accuracy null
- Offset adjust to 0V
- DTL/TTL compatible FET gate
- Single storage capacitor

schematic and connection diagrams

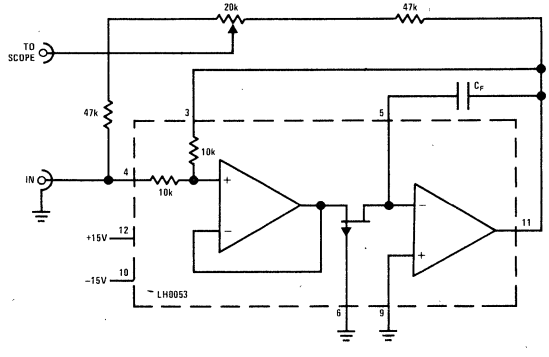


Metal Can Package



Order Number LH0053G or LH0053CG
See Package 6

ac test circuit



Acquisition Time Test Circuit

absolute maximum ratings

Supply Voltage (V^+ and V^-)	±18V
Gate Input Voltage (V_6 and V_7)	±20V
Analog Input Voltage (V_4)	±15V
Input Current (I_8 and I_5)	±10 mA
Power Dissipation	1.5W
Output Short Circuit Duration	Continuous
Operating Temperature Range	
LH0053	−55°C to +125°C
LH0053C	−25°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

electrical characteristics (Note 1)

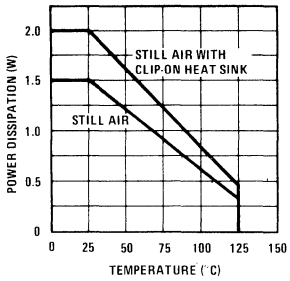
PARAMETER	CONDITIONS	LIMITS						UNITS
		LH0053			LH0053C			
		MIN	TYP	MAX	MIN	TYP	MAX	
Sample (Gate "0") Input Voltage				0.5			0.5	V
Sample (Gate "0") Input Current	V_6 = 0.5V, T_A = 25°C V_6 = 0.5			−5.0 −100			−5.0 −100	µA µA
Hold (Gate "1") Input Voltage		4.5			4.5			V
Hold (Gate "1") Input Current	V_6 = 4.5V, T_A = 25°C V_6 = 4.5V			1.0 1.0			1.0 1.0	nA µA
Analog Input Voltage Range		±10	±11		±10	±11		V
Supply Current	V_4 = 0V V_6 = 0.5V		13	18		13	18	mA
Input Bias Current (I_4)	V_4 = 0V, T_A = 25°C		120	250		150	500	nA
Input Resistance		9.0	10	11	9.0	10	11	kΩ
Analog Output Voltage Range	R_L = 2.0k	±10	±12		+10	±12		V
Output Offset Voltage	V_4 = 0V, V_6 = 0.5V, T_A = 25°C V_4 = 0V, V_6 = 0.5V		5.0	7.0 10		5.0	10 15	mV mV
Sample Accuracy (Note 2)	V_4 = ±10V, V_6 = 0.5V, T_A = 25°C		0.1	0.2		0.1	0.3	%
Aperture Time	ΔV_6 = 4.5V, T_A = 25°C		10	25		10	25	ns
Sample Acquisition Time	V_4 = ±10V, T_A = 25°C, C_F = 1000 pF		5.0	10		8.0	15	µs
Sample Acquisition Time	V_4 = ±10V, T_A = 25°C, C_F = 100 pF		4.0			4.0		µs
Output Slew Rate	ΔV_{IN} = ±10V, T_A = 25°C, C_F = 1000 pF		20			20		V/µs
Large Signal Bandwidth	V_4 = ±10V, T_A = 25°C, C_F = 1000 pF		200			200		kHz
Leakage Current (Pin 5)	V_4 = ±10V, T_A = 25°C, V_4 = ±10V		6.0	30 30		10	50 3.0	pA nA
Drift Rate	V_4 = ±10V, T_A = 25°C, C_F = 1000 pF		6.0	30		10	50	mV/s
Drift Rate	V_4 = ±10V, C_F = 1000 pF			30			3.0	V/s
Q2 Switch ON Resistance	V_7 = 0.5V, I_8 = 1.0 mA, T_A = 25°C		100	300		100	300	Ω

Note 1: Unless otherwise noted, these specifications apply for V_S = ±15V, pin 9 grounded, a 1000 pF capacitor between pin 5 and pin 11, pin 3 shorted to pin 11, over the temperature range −55°C to +125°C for the LH0053 and −25°C to +85°C for the LH0053C. All typical values are for T_A = 25°C.

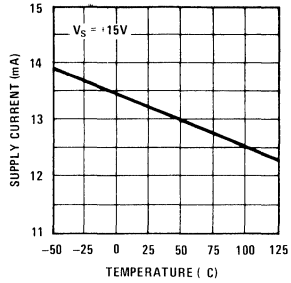
Note 2: Sample accuracy may be nulled by inserting a potentiometer in the feedback loop. This compensates for source impedance and feedback resistor tolerances.

typical performance characteristics

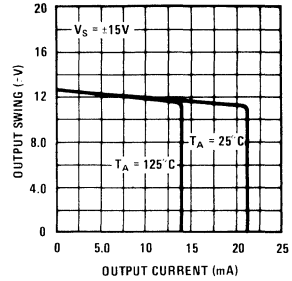
Power Dissipation



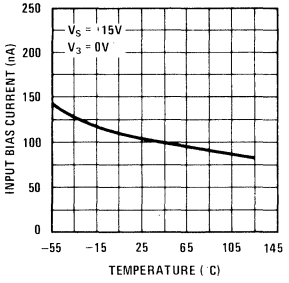
Supply Current vs Temperature



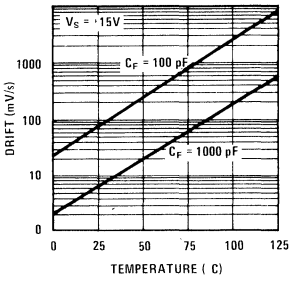
Output Current Limiting



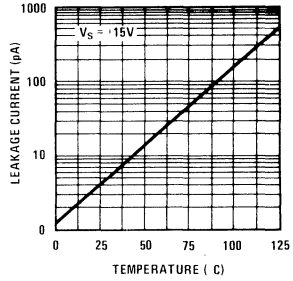
Input Bias Current



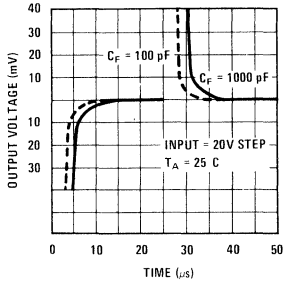
Drift



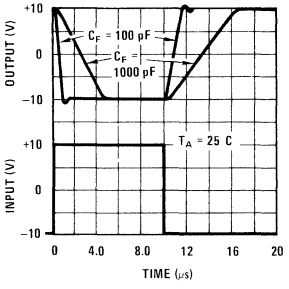
Leakage Current at Pin 5



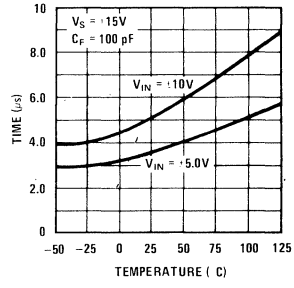
Sample Acquisition Time



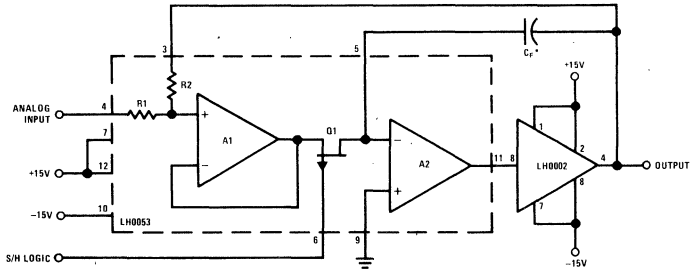
Output Slew Rate



Acquisition Time vs Temperature



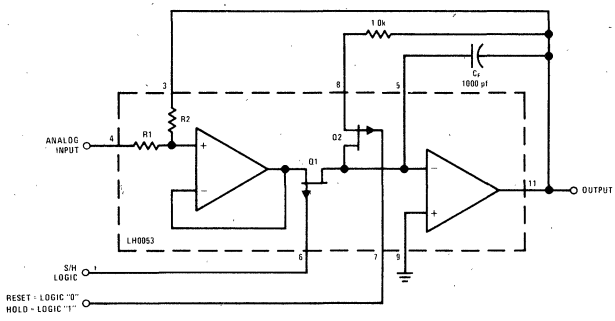
typical applications



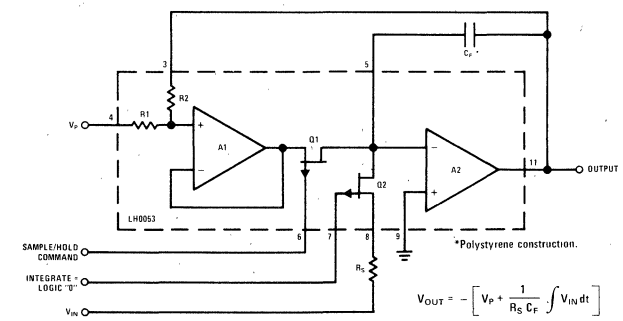
*Polystyrene construction.

Increasing Output Drive Capability

typical applications (con't)



Sample and Hold with Reset



Preset Integrator

applications information

SOURCE IMPEDANCE COMPENSATION

The gain accuracy (linearity) of the LH0053/LH0053C is set by two internal precision resistors. Circuit applications in which the source impedance is non-zero will result in a closed loop gain error, e.g. if R_S = 10Ω, a gain error of 0.1% results. Figure 1 and 2 show methods for accommodating non-zero source impedance.

DRIFT ERROR MINIMIZATION

In order to minimize drift error, care in selection C_F and layout of the printed circuit board is required. The capacitor should be of high quality teflon, polycarbonate or polystyrene construction. Board layout and clean lines are critical particularly at elevated temperature.

A ground guard (shield) surrounding pin 5 will minimize leakage currents to and from the summing junction, arising from extraneous signals. See AN-63 for detailed recommendations.

CAPACITOR SELECTION

The size of the capacitor is determined by the required drift rate usually at the expense of acquisition time.

The drift is dictated by leakage current at pin 5 and is given by:

$$\frac{dv}{dt} = \frac{I_L}{C_F}$$

Where I_L is the leakage current at pin 5 and C_F is the value of the capacitance. The room temperature leakage of the LH0053 is typical 6.0 pA, and a 1000 pF capacitor will yield a drift rate of 6.0 mV per second.

For values of C_F below 1000 pF acquisition for the LH0053 is primarily governed by the slew rate of the input amplifier (200V/μs) and the setting time of output amplifier (≅ 1.0μs). For values above C_F = 1000 pF, acquisition time is given by:

$$t_a = \frac{C_F\,\Delta V}{I_{DSS}} + t_{S2}$$

Where:

C_F = The value of the capacitor

ΔV = The magnitude of the input step; e. g. 20V

I_{DSS} = The ON current of switch Q1 ≅ 5.0 mA

t_{S2} = The setting time of output amplifier ≅ 1.0μs

applications information (con't)

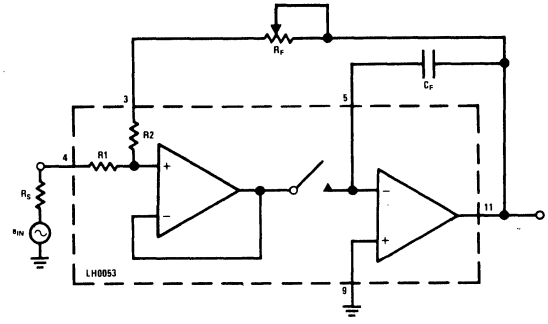


FIGURE 1. Non-Zero Source Impedance Compensation

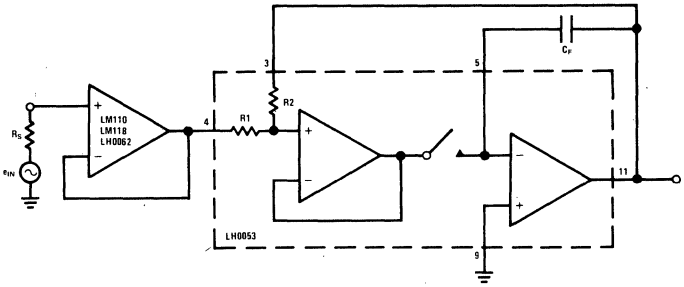


FIGURE 2. Non-Zero Source Impedance Buffering

GATE INPUT CONSIDERATIONS

5.0V TTL Applications

The LH0053 Gate inputs Gate 1 (pin 6) and Gate 2 (pin 7) will interface directly with 5.0V TTL. However, TTL gates typically pull up to 2.5V in the logic "1" state. It is therefore advisable to use a 10k pull-up resistor between the 5.0V, V_{CC}, and the output of the gate as shown in Figure 3.

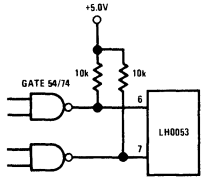


FIGURE 3. TTL Logic Compatibility

CMOS Applications

The LH0053 gate inputs may be interfaced directly with 74C, CMOS operating off of V_{CC}'s from 5.0V to 15V. However transient currents of several milliamps can flow on the rising and falling edges of the input signal. It is, therefore, advisable to parallel the outputs of two 54C/74C gates as shown in Figure 4.

It should be noted that leakage at pin 5 in the hold mode will be increased by a factor of 2 to 3 when operating into 15V logic levels.

Unused Switch, Q2

In applications when switch Q2 is not used the logic input (pin 7) should be returned to +5.0V (or +15V for HTL applications) through a 10kΩ resistor. Analog Input, preset (pin 8) should be grounded.

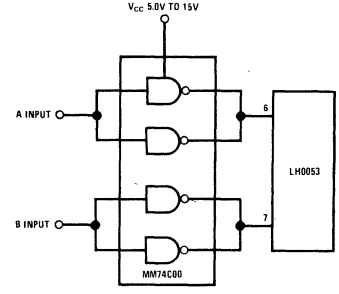


FIGURE 4. CMOS Logic Compatibility

HEAT SINKING

The LH0053 may be operated over the military temperature range, −55°C to +125°C, without incurring damage to the device. However, a clip on heat sink such as the Wakefield 215 Series or Thermolloy 2240 will reduce the internal temperature rise by about 20°C. The result is a two-fold improvement in drift rate at temperature.

applications information (con't)

Since the case of the device is electrically isolated from the circuit, the LH0053 may be mounted directly to a grounded heat sink.

POWER SUPPLY DECOUPLING

Amplifiers A1 and A2 within the LH0053 are very wide band devices and are sensitive to power supply inductance. It is advisable to by-pase V^+ (pin 12) and V^- (pin 10) to ground with 0.1μF disc capacitors in order to prevent oscillation. Should this procedure prove inadequate, the disc capacitors should be paralled with 4.7μF solid tantalum electrolytic capacitors.

DC OFFSET ADJUST

Output offset error may be adjusted to zero using the circuit shown in Figure 5. Offset null should be accomplished in the sample mode ($V_6 \leq 0.5V$) and analog input (pin 4) equal to zero volts.

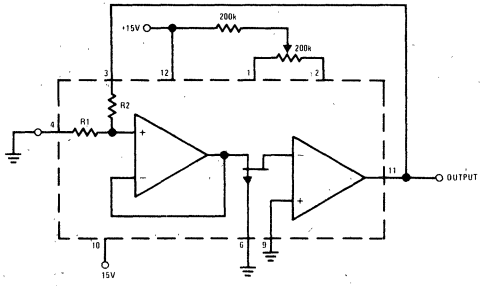


FIGURE 5. Offset Null Circuit

definition of terms

Voltage, V_4: The voltage at pin 4, i.e., the analog input voltage.

Voltage, V_6: The voltage at pin 6, i.e., the logic control signal. A logic "1" input, $V_6 \leq 4.5V$, places the LH0053 in the HOLD mode; a logic "0" input ($V_6 \leq 0.5V$) places the device in sample mode.

Acquisition Time: The time required for the output (pin 11) to settle within the rated accuracy after a specified input change is applied to Analog Input 1 (pin 4) with logic input, Gate 1, (pin 6) in the logic "0" state.

Aperture Time: The time indeterminacy when switching from the "sample" mode to the HOLD mode measured from time the logic input passes through it's threshold (2.0V) to the time the device actually enters the HOLD mode.

Sample Accuracy: Difference between input voltage and output voltage while in the sample mode, expressed as a percent of input voltage.

Comparators

LH2111/LH2211/LH2311 dual voltage comparator

general description

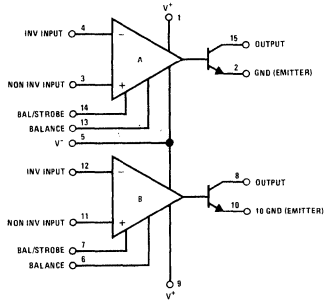
The LH2111 series of dual voltage comparators are two LM111 type comparators in a single hermetic package. Featuring all the same performance characteristics of the single, these duals offer in addition closer thermal tracking, lower weight, reduced insertion cost and smaller size than two singles. For additional information see the LM111 data sheet and National's Linear Application Handbook.

The LH2111 is specified for operation over the −55°C to +125°C military temperature range. The LH2211 is specified for operation over the −25°C to +85°C temperature range. The LH2311 is specified for operation over the 0°C to 70°C temperature range.

features

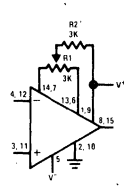
- Wide operating supply range — ±15V to a single +5V
- Low input currents — 6 nA
- High sensitivity — 10 μV
- Wide differential input range — ±30V
- High output drive — 50 mA, 50V

connection diagram

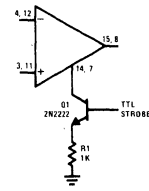


Order Number LH2110D or LH2210D or LH2310D
See Package 2

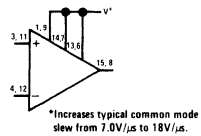
auxiliary circuits



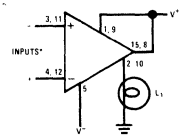
Offset Balancing



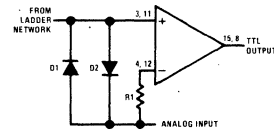
Strobing



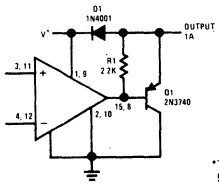
Increasing Input Stage Current*



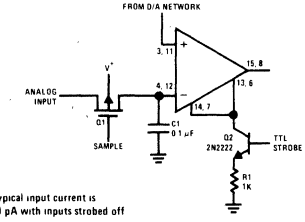
Driving Ground-Referred Load



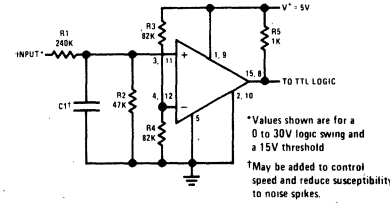
Using Clamp Diodes to Improve Responses



Comparator and Solenoid Driver



Strobing off Both Input* and Output Stages



TTL Interface with High Level Logic

absolute maximum ratings

Total Supply Voltage ($V^+ - V^-$)	36V	Output Short Circuit Duration	10 sec
Output to Negative Supply Voltage ($V_{OUT} - V^-$)	50V	Operating Temperature Range LH2111	−55°C to 125°C
Ground to Negative Supply Voltage (GND − V^-)	30V	LH2211	−25°C to 85°C
Differential Input Voltage	±30V	LH2311	0°C to 70°C
Input Voltage (Note 1)	±15V	Storage Temperature Range	−65°C to 150°C
Power Dissipation (Note 2)	500 mW	Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics — each side (Note 3)

PARAMETER	CONDITIONS	LIMITS			UNITS
		LH2111	LH2211	LH2311	
Input Offset Voltage (Note 4)	$T_A = 25°C$, $R_S \leq 50k$	3.0	3.0	7.5	mV Max
Input Offset Current (Note 4)	$T_A = 25°C$	10	10	50	nA Max
Input Bias Current	$T_A = 25°C$	100	100	250	nA Max
Voltage Gain	$T_A = 25°C$	200	200	200	V/mV Typ
Response Time (Note 5)	$T_A = 25°C$	200	200	200	ns Typ
Saturation Voltage	$V_{IN} \leq -5$ mV, $I_{OUT} = 50$ mA $T_A = 25°C$	1.5	1.5	1.5	V Max
Strobe On Current	$T_A = 25°C$	3.0	3.0	3.0	mA Typ
Output Leakage Current	$V_{IN} \geq 5$ mV, $V_{OUT} = 35V$ $T_A = 25°C$	10	10	50	nA Max
Input Offset Voltage (Note 4)	$R_S \leq 50k$	4.0	4.0	10	mV Max
Input Offset Current (Note 4)		20	20	70	nA Max
Input Bias Current		150	150	300	nA Max
Input Voltage Range		±14	±14	±14	V Typ
Saturation Voltage	$V^+ \geq 4.5V$, $V^- = 0$ $V_{IN} \leq -5$ mV, $I_{SINK} \leq 8$ mA	0.4	0.4	0.4	V Max
Positive Supply Current	$T_A = 25°C$	6.0	6.0	7.5	mA Max
Negative Supply Current	$T_A = 25°C$	5.0	5.0	5.0	mA Max

Note 1: This rating applies for ±15V supplies. The positive input voltage limit is 30V above the negative supply. The negative input voltage limit is equal to the negative supply voltage or 30V below the positive supply, whichever is less.

Note 2: The maximum junction temperature is 150°C. For operating at elevated temperatures, devices in the flat package, the derating is based on a thermal resistance of 185°C/W when mounted on a 1/16-inch-thick epoxy glass board with 0.03-inch-wide, 2 ounce copper conductor. The thermal resistance of the dual-in-line package is 100°C/W, junction to ambient.

Note 3: These specifications apply for $V_S = \pm 15V$ and $-55°C \leq T_A \leq 125°C$ for the LH2111, $-25°C \leq T_A \leq 85°C$ for the LH2211, and $0°C \leq T_A \leq 70°C$ for the LH2311, unless otherwise stated. The offset voltage, offset current and bias current specifications apply for any supply voltage from a single 5V supply up to ±15V supplies. For the LH2311, $V_{IN} = \pm 10$ mV.

Note 4: The offset voltages and offset currents given are the maximum values required to drive the output within a volt of either supply with a 1 mA load. Thus, these parameters define an error band and take into account the worst case effects of voltage gain and input impedance.

Note 5: The response time specified is for a 100 mV input step with 5 mV overdrive.

Analog Switches

AH0014/AH0014C* DPDT, AH0015/AH0015C quad SPST, AH0019/AH0019C* dual DPST-TTL/DTL compatible

MOS analog switches general description

This series of TTL/DTL compatible MOS analog switches feature high speed with internal level shifting and driving. The package contains two monolithic integrated circuit chips: the MOS analog chip is similar to the MM450 type which consists of four MOS analog switch transistors; the second chip is a bipolar I.C. gate and level shifter. The series is available in both hermetic dual-in-line package and flatpack.

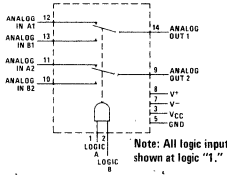
features

- Large analog voltage switching ±10V
- Fast switching speed 500 ns
- Operation over wide range of power supplies
- Low ON resistance 200Ω
- High OFF resistance $10^{11}\Omega$
- Fully compatible with DTL or TTL logic
- Includes gating and level shifting

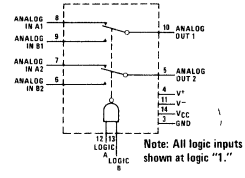
These switches are particularly suited for use in both military and industrial applications such as commutators in data acquisition systems, multiplexers, A/D and D/A converters, long time constant integrators, sample and hold circuits, modulators/demodulators, and other analog signal switching applications. For information on other National analog switches and analog interface elements, see listing on last page.

The AH0014, AH0015 and AH0019 are specified for operation over the −55°C to +125°C military temperature range. The AH0014C, AH0015C and AH0019C are specified for operation over the −25°C to +85°C temperature range.

block and connection diagrams

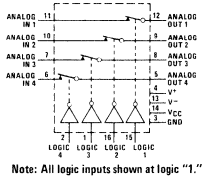


Order Number AH0014D or AH0014CD
See Package 1



Order Number AH0014D or AH0014CD
See Package 1
Order Number AH0014CN
See Package 17

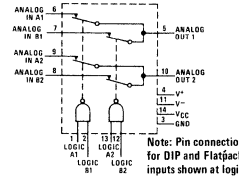
Quad SPST



Note: All logic inputs shown at logic "1."

Order Number AH0015D or AH0015CD
See Package 2
Order Number AH0015CN
See Package 18

Dual DPST

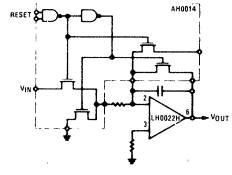


Note: Pin connections are identical for DIP and Flatpack. All logic inputs shown at logic "1."

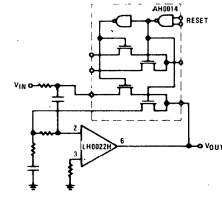
Order Number AH0019D or AH0019CD
See Package 1
Order Number AH0019CN
See Package 17

typical applications

Integrator



Reset Stabilized Amplifier



*Previously called NH0014/NH0014C and NH0019/NH0019C

absolute maximum ratings

V_{CC} Supply Voltage	7.0V
V^- Supply Voltage	−30V
V^+ Supply Voltage	+30V
V^+/V^- Voltage Differential	40V
Logic Input Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	
AH0014, AH0015, AH0019	−55°C to +125°C
AH0014C, AH0015C, AH0019C	−25°C to +85°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics (Notes 1 and 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	V_{CC} = 4.5V	2.0			V
Logical "0" Input Voltage	V_{CC} = 4.5V			0.8	V
Logical "1" Input Current	V_{CC} = 5.5V V_{IN} = 2.4V			5	μA
Logical "1" Input Current	V_{CC} = 5.5V V_{IN} = 5.5V			1	mA
Logical "0" Input Current	V_{CC} = 5.5V V_{IN} = 0.4V		0.2	0.4	mA
Power Supply Current Logical "1" Input – each gate (Note 3)	V_{CC} = 5.5V V_{IN} = 4.5V		0.85	1.6	mA
Power Supply Current Logical "0" Input – each gate (Note 3)	V_{CC} = 5.5V V_{IN} = 0V				
AH0014, AH0014C			1.5	3.0	mA
AH0015, AH0015C			0.22	0.41	mA
AH0019, AH0019C			0.22	0.41	mA
Analog Switch ON Resistance – each gate	V_{IN} (Analog) = +10V		75	200	Ω
	V_{IN} (Analog) = −10V		150	600	Ω
Analog Switch OFF Resistance			10^{11}		Ω
Analog Switch Input Leakage Current – each input (Note 4)	V_{IN} = −10V				
AH0014, AH0015, AH0019	T_A = 25°C		25	200	pA
	T_A = 125°C		25	200	nA
AH0014C, AH0015C, AH0019C	T_A = 25°C		0.1	10	nA
	T_A = 70°C		30	100	nA
Analog Switch Output Leakage Current – each output (Note 4)	V_{OUT} = −10V				
AH0014, AH0015, AH0019	T_A = 25°C		40	400	pA
	T_A = 125°C		40	400	nA
AH0014C, AH0015C, AH0019C	T_A = 25°C		0.05	10	nA
	T_A = 70°C		4	50	nA
Analog Input (Drain) Capacitance	1 MHz @ Zero Bias		8	10	pF
Output Source Capacitance	1 MHz @ Zero Bias		11	13	pF
Analog Turn-OFF Time – t_{OFF}	See test circuit; T_A = 25°C		400	500	ns
Analog Turn-ON Time – t_{ON}	See test circuit; T_A = 25°C				
AH0014, AH0014C			350	425	ns
AH0015, AH0015C			100	150	ns
AH0019, AH0019C			100	150	ns

Note 1: Min/max limits apply across the guaranteed temperature range of −55°C to +125°C for AH0014, AH0015, AH0019 and −25°C to +85°C for AH0014C, AH0015C, AH0019C. V^- = −20V. V^+ = +10V and an analog test current of 1 mA unless otherwise specified.

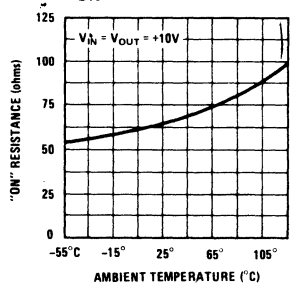
Note 2: All typical values are measured at T_A = 25°C with V_{CC} = 5.0V. V^+ = +10V, V^- = −22V.

Note 3: Current measured is drawn from V_{CC} supply.

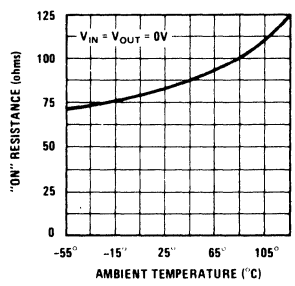
Note 4: All analog switch pins except measurement pin are tied to V^+.

analog switch characteristics (Note 2)

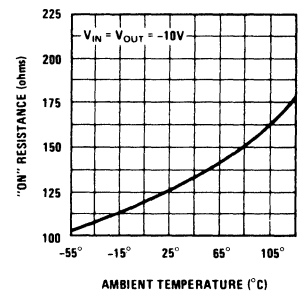
R_{ON} vs Temperature



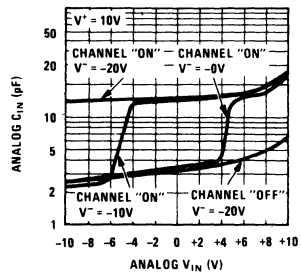
R_{ON} vs Temperature



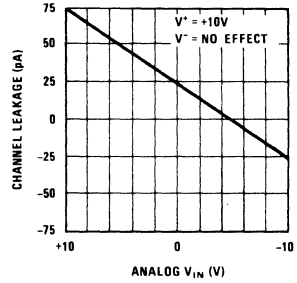
R_{ON} vs Temperature



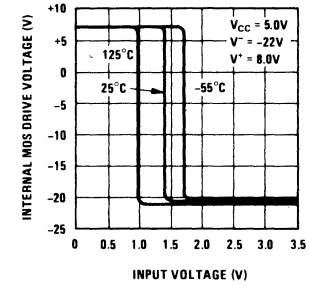
C_{IN} vs V_{IN}



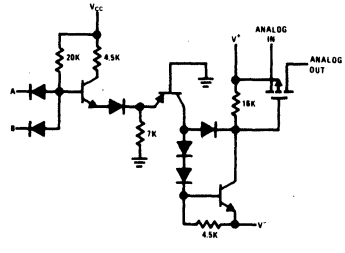
Leakage vs V_{IN} (Channel "OFF")



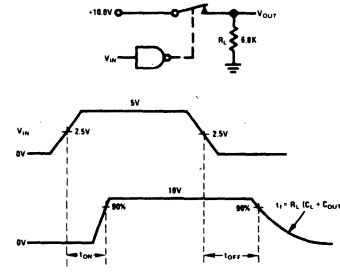
Driver Gate V_{IN} vs V_{OUT}



Schematic (Single Driver Gate and MOS Switch Shown)

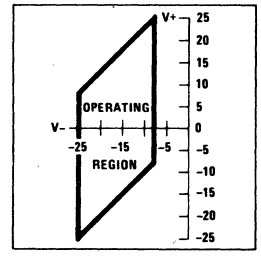


Analog Switching Time Test Circuit



selecting power supply voltage

The graph shows the boundary conditions which must be used for proper operation of the unit. The range of operation for power supply V^- is shown on the X axis. It must be between −25V and −8V. The allowable range for power supply V^+ is governed by supply V^-. With a value chosen for V^-, V^+ may be selected as any value along a vertical line passing through the V^- value and terminated by the boundaries of the operating region. A voltage difference between power supplies of at least 5V should be maintained for adequate signal swing.



Analog Switches

AH0120/AH0130/AH0140/AH0150/AH0160 series analog switches

general description

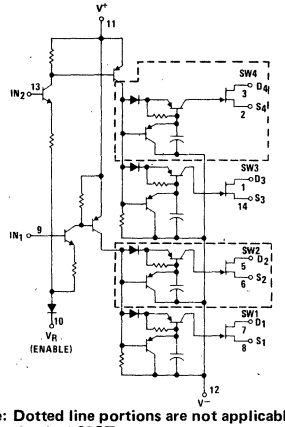
The AH0100 series represents a complete family of junction FET analog switches. The inherent flexibility of the family allows the designer to tailor the device selection to the particular application. Switch configurations available include dual DPST, dual SPST, DPDT, and SPDT. $r_{ds(ON)}$ ranges from 10 ohms through 100 ohms. The series is available in both 14 lead flat pack and 14 lead cavity DIP. Important design features include:

- TTL/DTL and RTL compatible logic inputs
- Up to 20V p-p analog input signal
- $r_{ds(ON)}$ less than 10Ω (AH0140, AH0141, AH0145, AH0146)
- Analog signals in excess of 1 MHz
- "OFF" power less than 1 mW
- Gate to drain bleed resistors eliminated
- Fast switching, t_{ON} is typically 0.4 μs, t_{OFF} is 1.0 μs
- Operation from standard op amp supply voltages, ±15V, available. (AH0150/AH0160 series)
- Pin compatible with the popular DG 100 series

The AH0100 series is designed to fulfill a wide variety of analog switching applications including commutators, multiplexers, D/A converters, sample and hold circuits, and modulators/demodulators. The AH0100 series is guaranteed over the temperature range -55°C to +125°C; whereas, the AH0100C series is guaranteed over the temperature range -25°C to +85°C

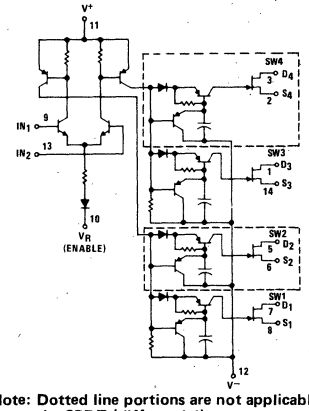
schematic diagrams

DUAL DPST and DUAL SPST



Note: Dotted line portions are not applicable to the dual SPST.

DPDT (diff.) and SPDT (diff.)

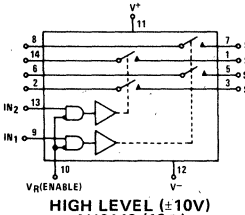


Note: Dotted line portions are not applicable to the SPDT (differential).

Order any of the devices below using the part number with a D suffix. See Package 1. AH0133C, AH0134C, AH0151C, AH0152C available in N Package also.

logic and connection diagrams

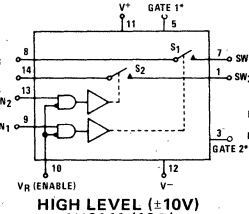
DUAL DPST



HIGH LEVEL (±10V)
AH0140 (10Ω)
AH0129 (30Ω)
AH0126 (80Ω)
MEDIUM LEVEL (±7.5V)
AH0153 (15Ω)
AH0154 (50Ω)

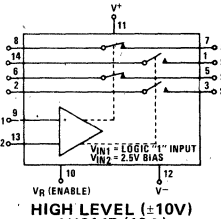
DUAL SPST

* Pinned out in N Package only.



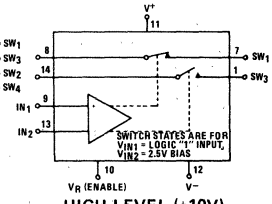
HIGH LEVEL (±10V)
AH0141 (10Ω)
AH0133 (30Ω)
AH0134 (80Ω)
MEDIUM LEVEL (±7.5V)
AH0151 (15Ω)
AH0152 (50Ω)

DPDT (diff.)



HIGH LEVEL (±10V)
AH0145 (10Ω)
AH0139 (30Ω)
AH0142 (80Ω)
MEDIUM LEVEL (±7.5V)
AH0163 (15Ω)
AH0164 (50Ω)

SPDT (diff.)



HIGH LEVEL (±10V)
AH0146 (10Ω)
AH0144 (30Ω)
AH0143 (80Ω)
MEDIUM LEVEL (±7.5V)
AH0161 (15Ω)
AH0162 (50Ω)

absolute maximum ratings

	High Level	Medium Level
Total Supply Voltage ($V^+ - V^-$)	36V	34V
Analog Signal Voltage ($V^+ - V_A$ or $V_A - V^-$)	30V	25V
Positive Supply Voltage to Reference ($V^+ - V_R$)	25V	25V
Negative Supply Voltage to Reference ($V_R - V^-$)	22V	22V
Positive Supply Voltage to Input ($V^+ - V_{IN}$)	25V	25V
Input Voltage to Reference ($V_{IN} - V_R$)	±6V	±6V
Differential Input Voltage ($V_{IN} - V_{IN2}$)	±6V	±6V
Input Current, Any Terminal	30 mA	30 mA
Power Dissipation		See Curve
Operating Temperature Range AH0100 Series		−55°C to +125°C
AH0100C Series		−25°C to +85°C
Storage Temperature Range		−65°C to +150°C
Lead Temperature (Soldering, 10 sec)		300°C

electrical characteristics for "HIGH LEVEL" Switches (Note 1)

PARAMETER	SYMBOL	DEVICE TYPE: DUAL DPST	DUAL SPST	DPDT (DIFF)	SPDT (DIFF)	CONDITIONS: $V^+ = 12.0V$, $V^- = -18.0V$, $V_R = 0.0V$		LIMITS: TYP	MAX	UNITS
Logic "1" Input Current	$I_{IN(ON)}$	All Circuits				Note 2	$T_A = 25°C$	2.0	60	μA
							Over Temp. Range		120	μA
Logic "0" Input Current	$I_{IN(OFF)}$	All Circuits				Note 2	$T_A = 25°C$	.01	.1	μA
							Over Temp. Range		2.0	μA
Positive Supply Current Switch ON	$I^+_{(ON)}$	All Circuits				One Driver ON Note 2	$T_A = 25°C$	2.2	3.0	mA
							Over Temp. Range		3.3	mA
Negative Supply Current Switch ON	$I^-_{(ON)}$	All Circuits				One Driver ON Note 2	$T_A = 25°C$	−1.0	−1.8	mA
							Over Temp. Range		−2.0	mA
Reference Input (Enable) ON Current	$I_{R(ON)}$	All Circuits				One Driver ON Note 2	$T_A = 25°C$	−1.0	−1.4	mA
							Over Temp. Range		−1.6	mA
Positive Supply Current Switch OFF	$I^+_{(OFF)}$	All Circuits				$V_{IN1} = V_{IN2} = 0.8V$	$T_A = 25°C$	1.0	10	μA
							Over Temp. Range		25	μA
Negative Supply Current Switch OFF	$I^-_{(OFF)}$	All Circuits				$V_{IN1} = V_{IN2} = 0.8V$	$T_A = 25°C$	−1.0	−10	μA
							Over Temp. Range		−25	μA
Reference Input (Enable) OFF Current	$I_{R(OFF)}$	All Circuits				$V_{IN1} = V_{IN2} = 0.8V$	$T_A = 25°C$	−1.0	−10	μA
							Over Temp. Range		−25	μA
Switch ON Resistance	$r_{ds(ON)}$	AH0126	AH0134	AH0142	AH0143	$V_D = 10V$, $I_D = 1$ mA	$T_A = 25°C$	45	80	Ω
							Over Temp. Range		150	Ω
Switch ON Resistance	$r_{ds(ON)}$	AH0129	AH0133	AH0139	AH0144	$V_D = 10V$, $I_D = 1$ mA	$T_A = 25°C$	25	30	Ω
							Over Temp. Range		60	Ω
Switch ON Resistance	$r_{ds(ON)}$	AH0140	AH0141	AH0145	AH0146	$V_D = 10V$, $I_F = 1$ mA	$T_A = 25°C$	8	10	Ω
							Over Temp. Range		20	Ω
Driver Leakage Current	$(I_D + I_S)_{ON}$	All Circuits				$V_D = V_S = -10V$	$T_A = 25°C$	.01	1	nA
							Over Temp. Range		100	nA
Switch Leakage Current	$I_{S(OFF)}$ OR $I_{D(OFF)}$	AH0126, AH0129	AH0134, AH0133	AH0142, AH0139	AH0143, AH0144	$V_{DS} = \pm 20V$	$T_A = 25°C$	0.8	1	nA
							Over Temp. Range		100	nA
Switch Leakage Current	$I_{S(OFF)}$ OR $I_{D(OFF)}$	AH0140	AH0141	AH0145	AH0146	$V_{DS} = \pm 20V$	$T_A = 25°C$	4	10	nA
							Over Temp. Range		1.0	μA
Switch Turn-ON Time	t_{ON}	AH0126, AH0129	AH0134, AH0133	AH0142, AH0139	AH0143, AH0144	See Test Circuit $V_A = \pm 10V$ $T_A = 25°C$		0.5	0.8	μs
Switch Turn-ON Time	t_{ON}	AH0140	AH0141	AH0145	AH0146	See Test Circuit $V_A = \pm 10V$ $T_A = 25°C$		0.8	1.0	μs
Switch Turn-OFF Time	t_{OFF}	AH0126, AH0129	AH0134, AH0133	AH0142, AH0139	AH0143, AH0144	See Test Circuit $V_A = \pm 10V$ $T_A = 25°C$		0.9	1.6	μs
Switch Turn-OFF Time	t_{OFF}	AH0140	AH0141	AH0145	AH0146	See Test Circuit $V_A = \pm 10V$ $T_A = 25°C$		1.1	2.5	μs

Note 1: Unless otherwise specified these limits apply for −55°C to +125°C for the AH0100 series and −25°C to +85°C for the AH0100C series. All typical values are for $T_A = 25°C$.

Note 2: For the DPST and Dual DPST, the ON condition is for $V_{IN} = 2.5V$; the OFF condition is for $V_{IN} = 0.8V$. For the differential switches and SW1 and 2 ON, $V_{IN2} = 2.5V$, $V_{IN1} = 3.0V$. For SW3 and 4 ON, $V_{IN2} = 2.5V$, $V_{IN1} = 2.0V$.

electrical characteristics for "MEDIUM LEVEL" Switches (Note 1)

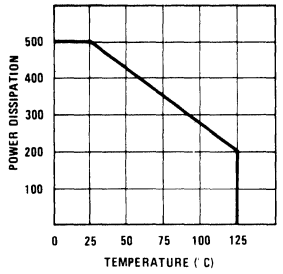
PARAMETER	SYMBOL	DEVICE TYPE: DUAL DPST	DUAL SPST	DUAL DPDT	SPDT (DIFF)	CONDITIONS: $V^+ = +15.0V$, $V^- = -15V$, $V_R = 0V$		LIMITS: TYP	MAX	UNITS
Logic "1" Input Current	$I_{IN(ON)}$	All Circuits				Note 2	$T_A = 25°C$	20	60	µA
							Over Temp. Range		120	µA
Logic "0" Input Current	$I_{IN(OFF)}$	All Circuits				Note 2	$T_A = 25°C$	.01	0.1	µA
							Over Temp. Range		2	µA
Positive Supply Current Switch ON	$I^+_{(ON)}$	All Circuits				One Driver ON Note 2	$T_A = 25°C$	2.2	3.0	mA
							Over Temp. Range		3.3	mA
Negative Supply Current Switch ON	$I^-_{(ON)}$	All Circuits				One Driver ON Note 2	$T_A = 25°C$	-1.0	-1.8	mA
							Over Temp. Range		-2.0	mA
Reference Input (Enable) ON Current	$I_{R(ON)}$	All Circuits				One Driver ON Note 2	$T_A = 25°C$	-1.0	-1.4	mA
							Over Temp. Range		-1.6	mA
Positive Supply Current Switch OFF	$I^+_{(OFF)}$	All Circuits				$V_{IN1} = V_{IN2} = 0.8V$	$T_A = 25°C$	1.0	10	µA
							Over Temp. Range		25	µA
Negative Supply Current Switch OFF	$I^-_{(OFF)}$	All Circuits				$V_{IN1} = V_{IN2} = 0.8V$	$T_A = 25°C$	-1.0	-10	µA
							Over Temp. Range		-25	µA
Reference Input (Enable) OFF Current	$I_{R(OFF)}$	All Circuits				V_{IN1} V_{IN2} 0.8V	$T_A = 25°C$	-1.0	-10	µA
							Over Temp. Range		-25	µA
Switch ON Resistance	$r_{ds(ON)}$	AH0153	AH0151	AH0163	AH0161	$V_D = 7.5V$, $I_D = 1$ mA	$T_A = 25°C$	10	15	Ω
							Over Temp. Range		30	Ω
Switch ON Resistance	$r_{ds(ON)}$	AH0154	AH0152	AH0164	AH0162	$V_D = 7.5V$, $I_D = 1$ mA	$T_A = 25°C$	45	50	Ω
							Over Temp. Range		100	Ω
Driver Leakage Current	$(I_D + I_S)_{ON}$	All Circuits				$V_D = V_S = 7.5V$	$T_A = 25°C$	.01	2	nA
							Over Temp. Range		500	nA
Switch Leakage Current	$I_{D(OFF)}$ OR $I_{S(OFF)}$	AH0153	AH0151	AH0163	AH0161	$V_{DS} = \pm 15V$	$T_A = 25°C$	5	10	nA
							Over Temp. Range		1.0	µA
Switch Leakage Current	$I_{D(OFF)}$ OR $I_{S(OFF)}$	AH0154	AH0152	AH0164	AH0162	$V_{DS} = \pm 15.0V$	$T_A = 25°C$	1.0	2.0	nA
							Over Temp. Range		200	nA
Switch Turn-ON Time	t_{ON}	AH0153	AH0151	AH0163	AH0161	See Test Circuit, $V_A = \pm 7.5V$, $T_A = 25°C$		0.8	1.0	µs
Switch Turn-ON Time	t_{ON}	AH0154	AH0152	AH0164	AH0162	See Test Circuit, $V_A = \pm 7.5V$, $T_A = 25°C$		0.5	0.8	µs
Switch Turn-OFF Time	t_{OFF}	AH0153	AH0151	AH0163	AH0161	See Test Circuit, $V_A = \pm 7.5V$, $T_A = 25°C$		1.1	2.5	µs
Switch Turn-OFF Time	t_{OFF}	AH0154	AH0152	AH0164	AH0162	See Test Circuit, $V_A = \pm 7.5V$, $T_A = 25°C$		0.9	1.5	µs

Note 1: Unless otherwise specified, these limits apply for –55°C to +125°C for the AH0100 series and –25°C to +85°C for the AH0100C series. All typical values are for $T_A = 25°C$.

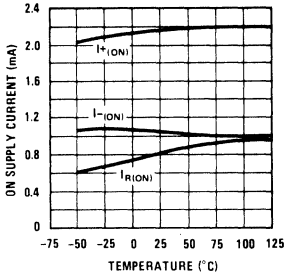
Note 2: For the DPST and Dual DPST, the ON condition is for $V_{IN} = 2.5V$; the OFF condition is for $V_{IN} = 0.8V$. For the differential switches and SW1 and 2 ON, $V_{IN2} = 2.5V$, $V_{IN1} = 3.0V$. For SW3 and 4 ON, $V_{IN2} = 2.5V$, $V_{IN1} = 2.0V$.

typical performance characteristics

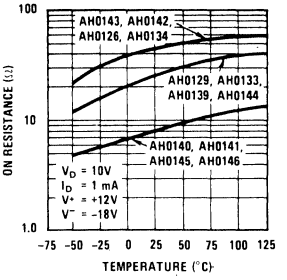
Power Dissipation vs Temperature



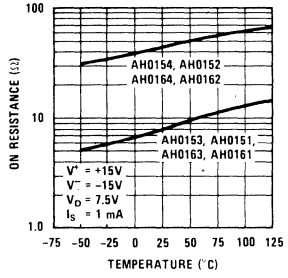
ON Supply Current vs Temperature



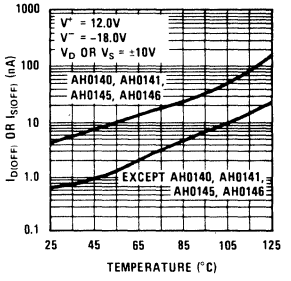
rds(ON) vs Temperature AH0120 thru AH0140 Series



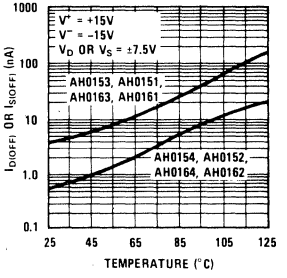
rds(ON) vs Temperature AH0150/AH0160 Series



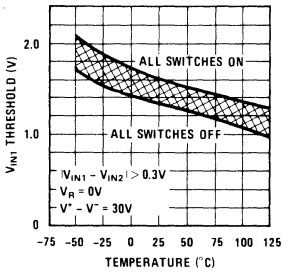
Leakage Current vs Temperature AH0120, AH0130, & AH0140



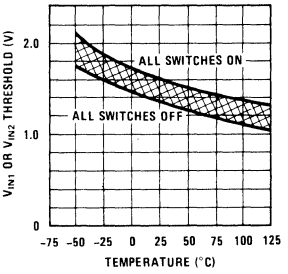
Leakage Current vs Temperature AH0150 & AH0160



Single Ended Switch Input Threshold vs Temperature

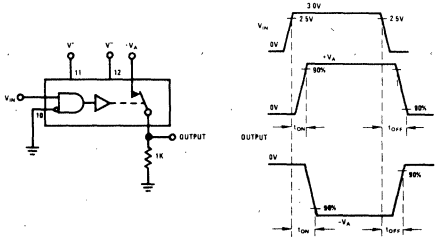


Differential Switch Input Threshold vs Temperature

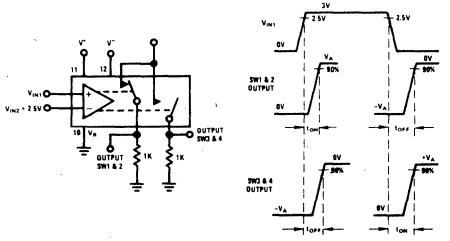


switching time test circuits

Single Ended Input



Differential Input



applications information

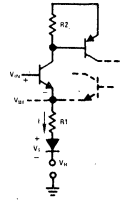
1. INPUT LOGIC COMPATIBILITY

A. Voltage Considerations

In general, the AH0100 series is compatible with most DTL, TTL, and RTL logic families. The ON-input threshold is determined by the V_{BE} of the input transistor plus the V_f of the diode in the emitter leg, plus I x R_1, plus V_R. At room temperature and V_R = 0V, the nominal ON threshold is: 0.7V + 0.7V + 0.2V, = 1.6V. Over temperature and manufacturing tolerances, the threshold may be as high as 2.5V and as low as 0.8V. The rules for proper operation are:

$V_{IN} - V_R \geq 2.5V$ All switches ON

$V_{IN} - V_R \leq 0.8V$ All switches OFF



B. Input Current Considerations

$I_{IN(ON)}$, the current drawn by the driver with V_{IN} = 2.5V is typically 20 μA at 25°C and is guaranteed less than 120 μA over temperature. DTL, such as the DM930 series can supply 180 μA at logic "1" voltages in excess of 2.5V. TTL output levels are comparable at 400 μA. The DTL and TTL can drive the AH0100 series directly. However, at low temperature, DC noise margin in the logic "1" state is eroded with DTL. A pull-up resistor of 10 kΩ is recommended when using DTL over military temperature range.

If more than one driver is to be driven by a DM930 series (6K) gate, an external pull-up resistor should be added. The value is given by:

$$R_P = \frac{11}{N-1} \text{ for } N > 2$$

where:

R_P = value of the pull-up resistor in kΩ

N = number of drivers.

C. Input Slew Rate

The slew rate of the logic input must be in excess of 0.3V/μs in order to assure proper operation of the analog switch. DTL, TTL, and RTL output rise times are far in excess of the minimum slew rate requirements. Discrete logic designs, however, should include consideration of input rise time.

2. ENABLE CONTROL

The application of a positive signal at the V_R terminal will open all switches. The V_R (ENABLE) signal must be capable of rising to within 0.8V of $V_{IN(ON)}$ in the OFF state and of sinking $I_{R(ON)}$ milliamps in the ON state (at $V_{IN(ON)} - V_R >$ 2.5V). The V_R terminal can be driven from most TTL and DTL gates.

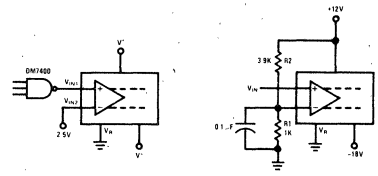
3. DIFFERENTIAL INPUT CONSIDERATIONS

The differential switch driver is essentially a differential amplifier. The input requirements for proper operation are:

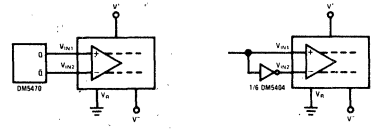
$|V_{IN1} - V_{IN2}| \geq 0.3V$

$2.5 \leq (V_{IN1} \text{ or } V_{IN2}) - V_R \leq 5V$

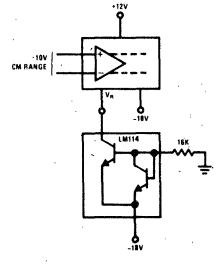
The differential driver may be furnished by a DC level as shown below. The level may be derived from a voltage divider to V^+ or the 5V V_{CC} of the DTL logic. In order to assure proper operation, the divider should be "stiff" with respect to I_{IN2}. Bypassing R1 with a 0.1 μF disc capacitor will prevent degradation of t_{ON} and t_{OFF}.



Alternatively, the differential driver may be driven from a TTL flip-flop or inverter.



Connection of a 1 mA current source between V_R and V^- will allow operation over a ±10V common mode range. Differential input voltage must be less than the 6V breakdown, and input threshold of 2.5V and 300mV differential overdrive still prevail.



4. ANALOG VOLTAGE CONSIDERATIONS

The rules for operating the AH0100 series at supply voltages other than those specified essentially breakdown into OFF and ON considerations. The OFF considerations are dictated by the maximum negative swing of the analog signal and the pinch off of the JFET switch. In the OFF state, the gate of the FET is at $V^- + V_{BE} + V_{SAT}$ or about 1.0V above the V^- potential. The maximum V_P of the FET switches is 7V. The most negative analog voltage, V_A, swing which can be accomodated for any given supply voltage is:

$$|V_A| \leq |V^-| - V_P - V_{BE} - V_{SAT} \text{ or}$$

$$|V_A| \leq |V^-| - 8.0 \text{ or } |V^-| \geq |V_A| + 8.0V$$

For the standard high level switches, $V_A \leq |-18| + 8 = -10V$. The value for V^+ is dictated by the maximum positive swing of the analog input voltage. Essentially the collector to base junction of the turn-on PNP must remain reversed biased for all positive value of analog input voltage. The base of the PNP is at $V^+ - V_{SAT} - V_{BE}$ or $V^+ - 1.0V$. The PNP's collector base junction should have at least 1.0V reverse bias. Hence, the most positive analog voltage swing which may be accommodated for a given value of V^+ is:

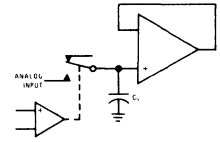
$$V_A \leq V^+ - V_{SAT} - V_{BE} - 1.0V \text{ or}$$

$$V_A \leq V^+ - 2.0V \text{ or } V^+ \geq V_A + 2.0V$$

For the standard high level switches, $V_A = 12 - 2.0V = +10V$.

5. SWITCHING TRANSIENTS

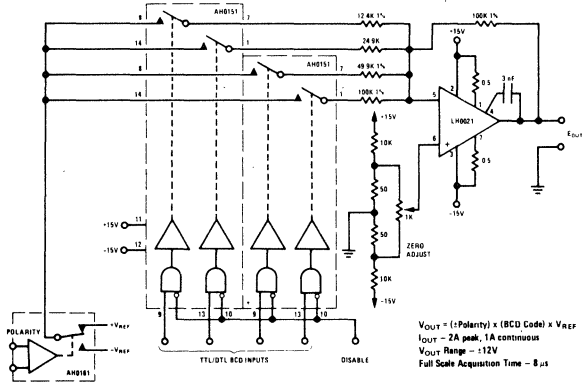
Due to charge stored in the gate-to-source and gate-to-drain capacitances of the FET switch, transients may appear in the output during switching. This is particularly true during the OFF to ON transition. The magnitude and duration of the transient may be minimized by making source and load impedance levels as small as practical.



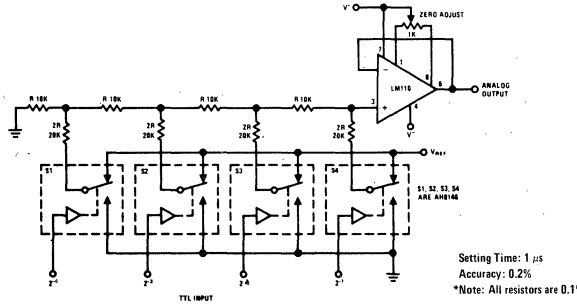
Furthermore, transients may be minimized by operating the switches in the differential mode; i.e., the charge delivered to the load during the ON to OFF transition is, to a large extent, cancelled by the OFF to ON transition.

typical applications

Programmable One Amp Power Supply

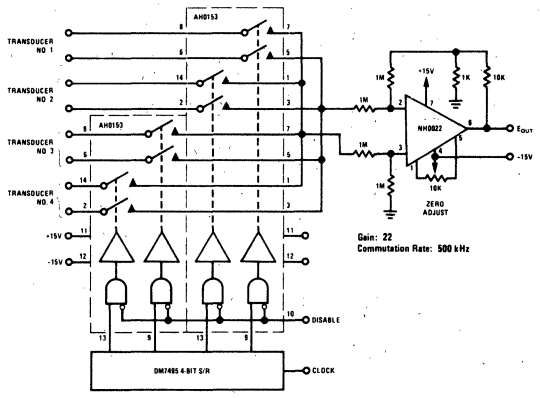


Four to Ten Bit D to A Converter (4 Bits Shown)



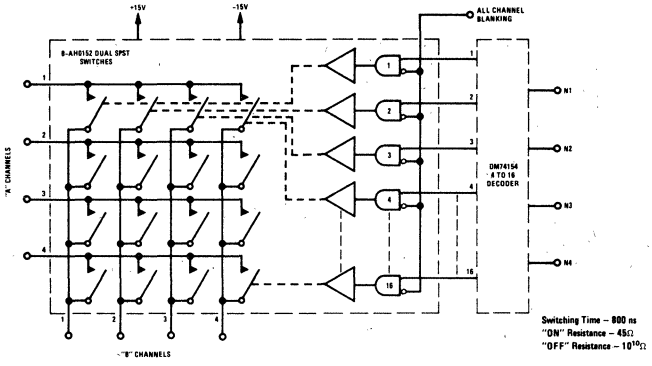
typical applications (con't)

Four Channel Differential Transducer Commutator



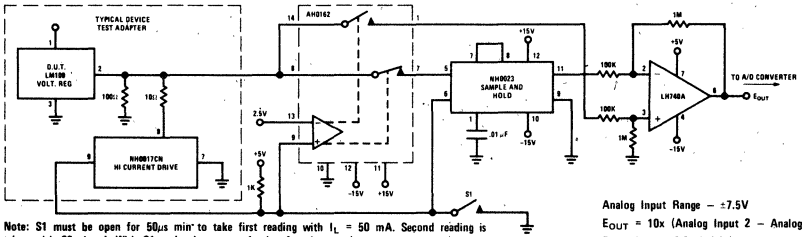
Gain: 22
Commutation Rate: 500 kHz

4 x 4 Cross Point Analog Switch



Switching Time – 800 ns
"ON" Resistance – 45Ω
"OFF" Resistance – 10^{10}Ω

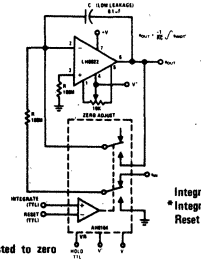
Delta Measurement System for Automatic Linear Circuit Tester



Note: S1 must be open for 50μs min to take first reading with I_L = 50 mA. Second reading is taken with S2 closed. With S1 and other set-up forcing functions under computer control, system will measure line and load regulation on voltage regulators, voltage gain, offset current, CMRR and PSRR on op amps as well as other circuits requiring measurement of the change of a parameter with the change of a forcing function.

Analog Input Range – ±7.5V
E_{OUT} = 10x (Analog Input 2 – Analog Input 1)
Error Rate – 0.01% F.S./sec

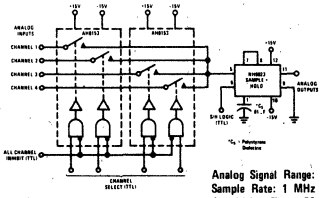
Precision Long Time Constant Integrator with Reset



Integration Internal = 10 sec
*Integration Error = 100μV
Reset Time: 30μs

*Note: V_{OS} adjusted to zero

Four Channel Commutator



Analog Signal Range: $15V_{P-P}$
Sample Rate: 1 MHz
Acquisition Time: 20μs
Drift Rate: 0.5 mV/sec

NATIONAL

Analog Switches

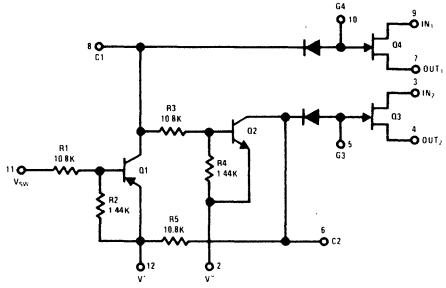
AH2114/AH2114C DPST analog switch general description

The AH2114 is a DPST analog switch circuit comprised of two junction FET switches and their associated driver. The AH2114 is designed to fulfill a wide variety of high level analog switching applications including multiplexers, A to D Converters, integrators, and choppers. Design features include:

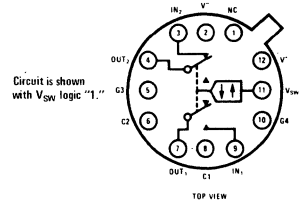
- Low ON resistance, typically 75Ω
- High OFF resistance, typically $10^{11}\Omega$
- Large output voltage swing, typically ±10V
- Powered from standard op-amp supply voltages of ±15V
- Input signals in excess of 1 MHz
- Turn-ON and turn-OFF times typically 1 μs

The AH2114 is guaranteed over the temperature range −55°C to +125°C whereas the AH2114C is guaranteed over the temperature range 0°C to +85°C.

schematic and connection diagrams

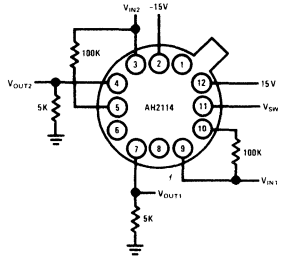


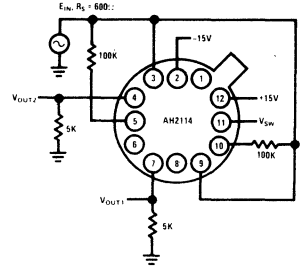
Metal Can Package

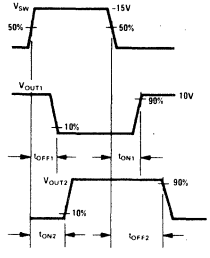


Order Number AH2114G or AH2114CG
See Package 7

ac test circuit and waveforms







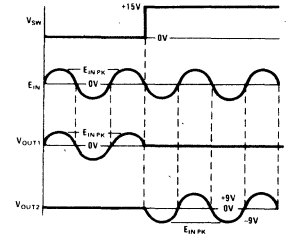


FIGURE 1.

FIGURE 2.

absolute maximum ratings

Vplus Supply Voltage	+25V
Vminus Supply Voltage	−25V
Vplus−Vminus Differential Voltage	40V
Logic Input Voltage	25V
Power Dissipation (Note 3)	1.36W
Operating Temperature Range	
AH2114	−55°C to +125°C
AH2114C	0°C to +85°C
Storage Temperature Range	−65°C to +125°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics (Notes 1 and 2)

PARAMETER	CONDITIONS	AH2114			AH2114C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Static Drain-Source "On" Resistance	I_D = 1.0 mA, V_{GS} = 0V, T_A = 25°C		75	100		75	125	Ω
	I_D = 1.0 mA, V_{GS} = 0V			150			160	Ω
Drain-Gate Leakage Current	V_{DS} = 20V, V_{GS} = −7V, T_A = 25°C		0.2	1.0		0.2	5.0	nA
				60			60	nA
FET Gate-Source Breakdown Voltage	I_G = 1.0 μA V_{DS} = 0V	35			35			V
Drain-Gate Capacitance	V_{DG} = 20V, I_S = 0 f = 1.0 MHz, T_A = 25°C		4.0	5.0		4.0	5.0	pF
Source-Gate Capacitance	V_{DG} = 20V, I_D = 0 f = 1.0 MHz, T_A = 25°C		4.0	5.0		4.0	5.0	pF
Input 1 Turn-ON Time	V_{IN1} = 10V, T_A = 25°C (See Figure 1)		35	60		35	60	ns
Input 2 Turn-ON Time	V_{IN2} = 10V, T_A = 25°C (See Figure 1)		1.2	1.5		1.2	1.2	μs
Input 1 Turn-OFF Time	V_{IN1} = 10V, T_A = 25°C (See Figure 1)		0.6	0.75		0.6	0.75	μs
Input 2 Turn-OFF Time	V_{IN2} = 10V, T_A = 25°C (See Figure 1)		50	80		50	80	ns
DC Voltage Range	T_A = 25°C (See Figure 2)	±9.0	±10.0		±9.0	±10.0		V
AC Voltage Range	T_A = 25°C (See Figure 2)	±9.0	±10.0		±9.0	±10.0		V

Note 1: Unless otherwise specified these specifications apply for pin 12 connected to +15V, pin 2 connected to −15V, −55°C to 125°C for the AH2114, and 0°C to 85°C for the AH2114C.

Note 2: All typical values are for T_A = 25°C.

Note 3: Derate linearly at 100°C/W above 25°C.

Analog Switches

AM9709/AM97C09/AH5009 series monolithic analog current switches

general description

A versatile family of monolithic JFET analog switches designed to economically fulfill a wide variety of multiplexing and analog switching applications.

Even numbered switches may be driven directly from standard 5V logic, whereas the odd numbered switches are intended for applications utilizing 10V or 15V logic. The monolithic construction guarantees tight resistance match and track.

The AM97C09 series is specifically intended to be driven from CMOS providing the best performance at lowest cost.

applications

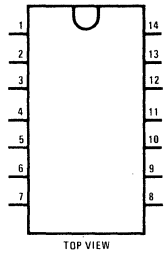
- AD/DA converters
- Micropower converters
- Industrial controllers
- Position controllers
- Data acquisition
- Active filters
- Signal multiplexers/demultiplexers
- Multiple channel AGC
- Quad compressors/expanders
- Choppers/demodulators
- Programmable gain amplifiers
- High impedance voltage buffer
- Sample and hold

features

- Interfaces with standard TTL and CMOS
- On-resistance match — 2 ohms
- Low "ON" resistance — 100 ohms
- Very low leakage — 50 pA
- Large analog signal range — ±10V peak
- High switching speed — 150 ns
- Excellent isolation between channels — 80 dB at 1 kHz

connection diagrams

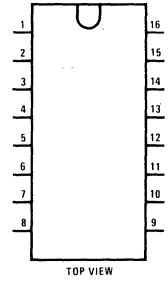
Dual-In-Line Package



TOP VIEW

Order Numbers
AM9709CN, AM97C09CN, AH5009CN, AH5013CN, AM9710CN, AM97C10CN, AH5010CN, AH5014CN
See Package 17

Dual-In-Line Package

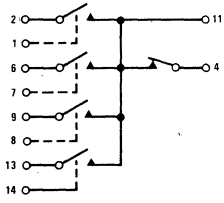


TOP VIEW

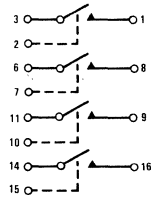
Order Numbers
AM9711CN, AM97C11CN, AH5011CN, AH5015CN, AM9712CN, AM97C12CN, AH5012CN, AH5016CN
See Package 18

functional and schematic diagrams (Additional type on other pages)

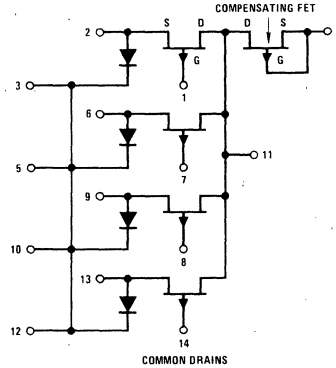
MUX Switches (4-Channel Version Shown)



SPST Switches (Quad Version Shown)

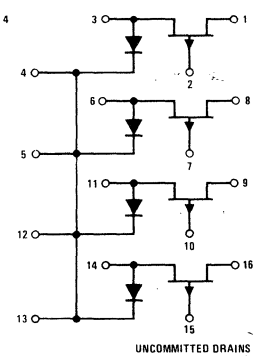


MUX Switches (4-Channel Version Shown)



COMMON DRAINS

SPST Switches (Quad Version Shown)



UNCOMMITTED DRAINS

absolute maximum ratings

Input Voltage	
AM9709–12CN, AH5009–24CN	30V
AM97C09–12CN	25V
Positive Analog Signal Voltage	30V
Negative Analog Signal Voltage	−15V
Diode Current	10 mA
Drain Current	30 mA
Power Dissipation	500 mW
Operating Temperature Range	−25°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

electrical characteristics

AM9709, AM97C09, AH5009 (Notes 1 and 2)

PARAMETER		CONDITIONS	5V TTL AM9710CN AM9712CN		5V TTL AH5010–16 (EVEN SERIES)		5V–10V CMOS AM97C10CN AM9712CN		UNITS
			TYP	MAX	TYP	MAX	TYP	MAX	
I_{GSX}	Input Current "OFF"	V_{GD} = 11V, V_{SD} = 0.7V	0.01	2	0.01	0.2			nA
		T_A = 85°C		100		10			nA
I_{GSX}	Input Current "OFF"	V_{GD} = 15V, V_{SD} = 0.7V					0.01	2	nA
		T_A = 85°C						100	nA
$I_{D(OFF)}$	Leakage Current "OFF"	V_{SD} = 0.7V, V_{GS} = 3.8V	0.01	0.2	0.01	0.2			nA
		T_A = 85°C		10		10			nA
$I_{D(OFF)}$	Leakage Current "OFF"	V_{SD} = 0.7V, V_{GS} = 4.3V					0.01	2	nA
		T_A = 85°C						100	nA
$I_{G(ON)}$	Leakage Current "ON"	V_{GD} = 0V, I_S = 1 mA	0.08	1	0.08	1	0.08	1	nA
		T_A = 85°C		200		200		200	nA
$I_{G(ON)}$	Leakage Current "ON"	V_{GD} = 0V, I_S = 2 mA	0.13	5		1000	0.13	5	nA
		T_A = 85°C		10		10		10	μA
$I_{G(ON)}$	Leakage Current "ON"	V_{GD} = 0V, I_S = −2 mA	0.1	10		100	0.10	10	nA
		T_A = 85°C		20		100		20	μA
$r_{DS(ON)}$	Drain-Source Resistance	V_{GS} = 0.35V, I_S = 2 mA	90	150	90	150			Ω
		T_A = +85°C		240		240			Ω
$r_{DS(ON)}$	Drain-Source Resistance	V_{GS} = 0V, I_S = 2 mA					90	150	Ω
		T_A = 85°C						240	Ω
V_{DIODE}	Forward Diode Drop	I_D = 0,5 mA		0.8				0.8	V
$r_{DS(ON)}$	Match	V_{GS} = 0, I_D = 1 mA	4	20		50	4	20	Ω
T_{ON}	Turn "ON" Time	See ac Test Circuit	150	500	150	500	150	500	ns
T_{OFF}	Turn "OFF" Time	See ac Test Circuit	300	500	300	500	300	500	ns
CT	Cross Talk	See ac Test Circuit	120		120		120		dB

Note 1: Test conditions 25°C unless otherwise noted.
Note 2: "OFF" and "ON" notation refers to the conduction state of the FET switch.

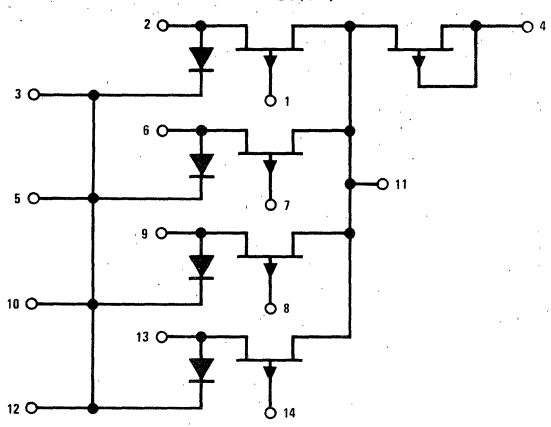
electrical characteristics (con't)

PARAMETER		CONDITIONS	15V TTL AM9709CN AM9711CN		15V TTL AH5009–15 (ODD SERIES)		10–15V CMOS AM97C09CN AM97C11CN		UNITS
			TYP	MAX	TYP	MAX	TYP	MAX	
I_{GSX}	Input Current "OFF"	V_{GD} = 11V, V_{SD} = 0.7V	0.01	2	0.01	0.2			nA
		T_A = 85°C		100		10			nA
I_{GSX}	Input Current "OFF"	V_{GD} = 15V, V_{SD} = 0.7V					0.01	2	nA
		T_A = 85°C						100	nA
$I_{D(OFF)}$	Leakage Current "OFF"	V_{SD} = 0.7V, V_{GS} = 9.3V					0.01	2	nA
		T_A = 85°C						100	nA
$I_{D(OFF)}$	Leakage Current "OFF"	V_{SD} = 0.7V, V_{GS} = 10.3V	0.01	2	0.01	0.2			nA
		T_A = 85°C		10		10			nA
$I_{G(ON)}$	Leakage Current "ON"	V_{GD} = 0V, I_S = 1 mA	0.04	0.5	0.04	0.5	0.04	0.5	nA
		T_A = 85°C		100		100		100	nA
$I_{G(ON)}$	Leakage Current "ON"	V_{GD} = 0V, I_S = 2 mA	0.07	2		2	0.07	2	nA
		T_A = 85°C		1		2		1	μA
$I_{G(ON)}$	Leakage Current "ON"	V_{GD} = 0V, I_S = −2 mA	0.05	5		100	0.05	5	nA
		T_A = 85°C		2		20		2	μA
$r_{DS(ON)}$	Drain-Source Resistance	V_{GS} = 0V, I_S = 2 mA					60	100	Ω
		T_A = 85°C						160	Ω
$r_{DS(ON)}$	Drain-Source Resistance	V_{GS} = 1.5V, I_S = 2 mA	60	100	60	100			Ω
		T_A = 85°C		160		160			Ω
V_{DIODE}	Forward Diode Drop	I_D = 0.5 mA		0.8				0.8	V
$r_{DS(ON)}$	Match	V_{GS} = 0, I_D = 1 mA	2	10		50	2	10	Ω
T_{ON}	Turn "ON" Time	See ac Test Circuit	150	500	150	500	150	500	ns
T_{OFF}	Turn "OFF" Time	See ac Test Circuit	300	500	300	500	300	500	ns
CT	Cross Talk	See ac Test Circuit	120		120		120		dB

schematic diagrams and pin connections

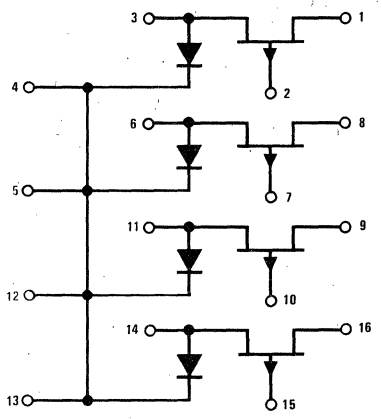
Four Channel

AM97C09CN ($R_{DS(ON)} \leq 100\Omega$, 10–15V CMOS)
AM97C10CN ($R_{DS(ON)} \leq 150\Omega$, 5–10V CMOS)
AM9709CN, AH5009CN ($R_{DS(ON)} \leq 100\Omega$, 15V TTL)
AM9710CN, AH5010CN ($R_{DS(ON)} \leq 150\Omega$, 5V TTL)



14-Pin DIP

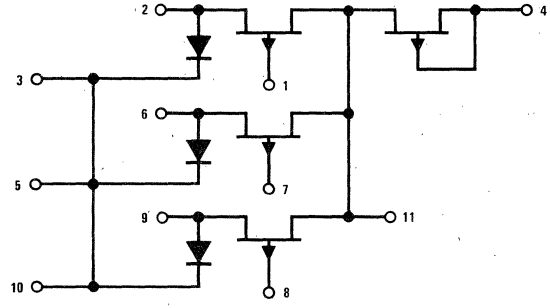
AM97C11CN ($R_{DS(ON)} \leq 100\Omega$, 10–15V CMOS)
AM97C12CN ($R_{DS(ON)} \leq 150\Omega$, 5–10V CMOS)
AM9711CN, AH5011CN ($R_{DS(ON)} \leq 100\Omega$, 15V TTL)
AM9712CN, AH5012CN ($R_{DS(ON)} \leq 150\Omega$, 5V TTL)



16-Pin DIP

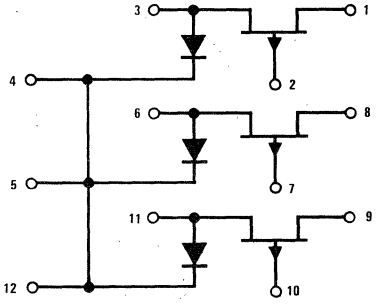
Three-Channel

AH5013CN ($R_{DS(ON)} \leq 100\Omega$, 15V TTL)
AH5014CN ($R_{DS(ON)} \leq 150\Omega$, 5V TTL)



14-Pin DIP

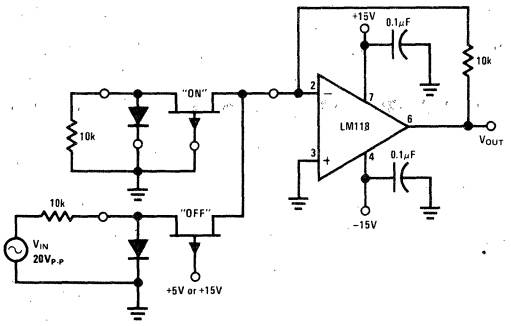
AH5015CN ($R_{DS(ON)} \leq 100\Omega$, 15V TTL)
AH5016CN ($R_{DS(ON)} \leq 150\Omega$, 5V TTL)



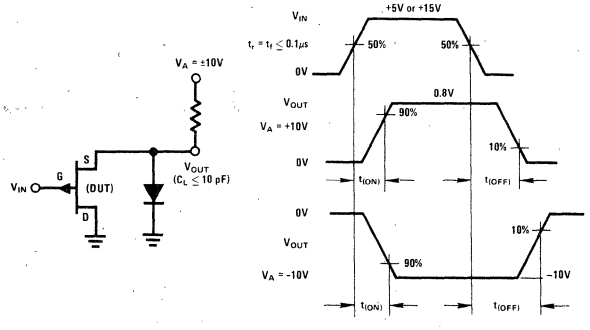
16-Pin DIP

test circuits and switching time waveforms

Cross Talk Test Circuit

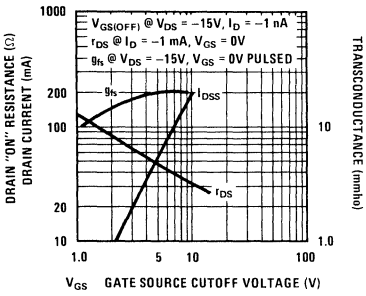


ac Test Circuit

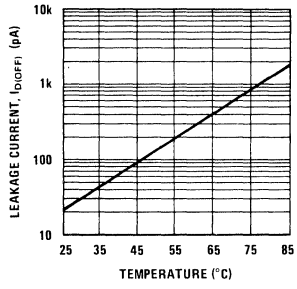


typical performance characteristics

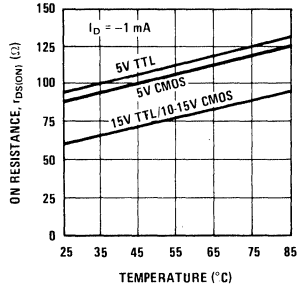
Parameter Interaction



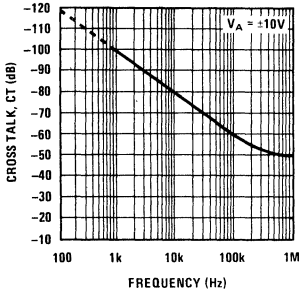
Leakage Current, $I_{D(OFF)}$ vs Temperature



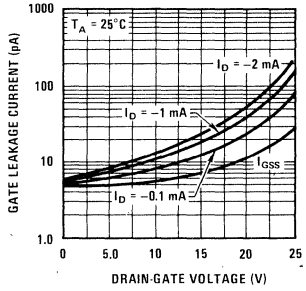
On Resistance, $r_{DS(ON)}$ vs Temperature



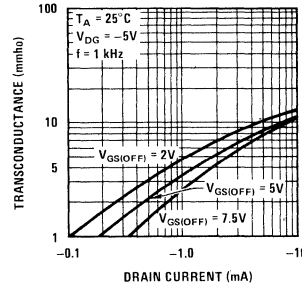
Cross Talk, CT vs Frequency



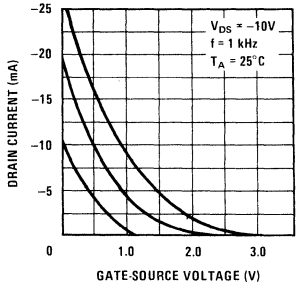
Leakage Current vs Drain-Gate Voltage



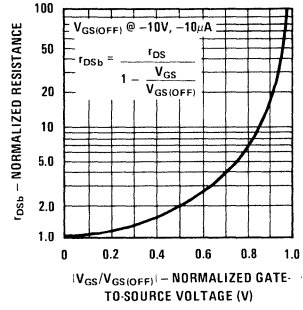
Transconductance vs Drain Current



Drain Current vs Bias Voltage



Normalized Drain Resistance vs Bias Voltage



applications information

Theory of Operation

The AM/AH series of analog switches are primarily intended for operation in current mode switch applications; i.e., the drains of the FET switch are held at or near ground by operating into the summing junction of an operational amplifier. Limiting the drain voltage to under a few hundred millivolts eliminates the need for a special gate driver, allowing the switches to be driven directly by standard TTL (AM9710), 5V–10V CMOS (AM97C10), open collector 15V TTL (AM9709), and 10–15V CMOS (AM97C09).

Two basic switch configurations are available: multiple independent switches (N by SPST) and multiple pole switches used for multiplexing (NPST-MUX). The MUX versions such as the AM9709 offer common drains and include a series FET operated at V_{GS} = 0V. The additional FET is placed in feedback path in order to compensate for the "ON" resistance of the switch FET as shown in *Figure 1.*

applications information (con't)

The closed-loop gain of *Figure 1* is:

$$A_{VCL} = \frac{R2 + r_{DS(ON)Q2}}{R1 + r_{DS(ON)Q1}}$$

For R1 = R2, gain accuracy is determined by the $r_{DS(ON)}$ match between Q1 and Q2. Typical match between Q1 and Q2 is 4 ohms resulting in a gain accuracy of 0.05% (for R1 = R2 = 10 kΩ).

Noise Immunity

The switches with the source diodes grounded exhibit improved noise immunity for positive analog signals in the "OFF" state. With V_{IN} = 15V and the V_A = 10V, the source of Q1 is clamped to about 0.7V by the diode (V_{GS} = 14.3V) ensuring that ac signals imposed on the 10V will not gate the FET "ON."

Selection of Gain Setting Resistors

Since the AM/AH series of analog switches are operated current mode, it is generally advisable to make the signal current as large as possible. However, current through the FET switch tends to forward bias the source to gate junction and the signal shunting diode resulting in leakage through these junctions. As shown in *Figure 2,* $I_{G(ON)}$ represents a finite error in the current reaching the summing junction of the op amp.

Secondly, the $r_{DS(ON)}$ of the FET begins to "round" as I_S approaches I_{DSS}. A practical rule of thumb is to maintain I_S at less than 1/10 of I_{DSS}.

Combining the criteria from the above discussion yields:

$$R1_{(MIN)} \geq \frac{V_{A(MAX)}\, A_D}{I_{G(ON)}} \qquad (2a)$$

or:

$$\geq \frac{V_{A(MAX)}}{I_{DSS}/10} \qquad (2b)$$

whichever is worse.

Where: $V_{A(MAX)}$ = Peak amplitude of the analog input signal

A_D = Desired accuracy

$I_{G(ON)}$ = Leakage at a given I_S

I_{DSS} = Saturation current of the FET switch

≅ 20 mA

In a typical application, V_A might = ±10V, A_D = 0.1%, 0°C ≤ T_A ≤ 85°C. The criterion of equation (2b) predicts:

$$R1_{(MIN)} \geq \frac{10V}{\frac{20\ mA}{10}} = 5\ k\Omega$$

For R1 = 5k, $I_S \cong$ 10V/5k or 2 mA. The electrical characteristics guarantee an $I_{G(ON)} \leq 1\mu A$ at 85°C for the AM9710. Per the criterion of equation (2a):

$$R1_{(MIN)} \geq \frac{(10V)(10^{-3})}{1 \times 10^{-6}} \geq 10\ k\Omega$$

Since equation (2a) predicts a higher value, the 10k resistor should be used.

The "OFF" condition of the FET also affects gain accuracy. As shown in *Figure 3,* the leakage across Q2, $I_{D(OFF)}$ represents a finite error in the current arriving at the summing junction of the op amp.

Accordingly:

$$R1_{(MAX)} \leq \frac{V_{A(MIN)}\, A_D}{(N)\, I_{D(OFF)}}$$

Where: $V_{A(MIN)}$ = Minimum value for the analog input signal

A_D = Desired accuracy

N = Number of channels

$I_{D(OFF)}$ = "OFF" leakage of a given FET switch

As an example, if N = 10, A_D = 0.1%, and $I_{D(OFF)}$ ≤ 10 nA at 85°C for the AM9709, $R1_{(MAX)}$ is:

$$R1_{(MAX)} \leq \frac{(1V)(10^{-3})}{(10)(10 \times 10^{-9})} = 10k$$

Selection of R2, of course, depends on the gain desired and for unity gain R1 = R2.

Lastly, the foregoing discussion has ignored resistor tolerances, input bias current and offset voltage of the op amp—all of which should be considered in setting the overall gain accuracy of the circuit.

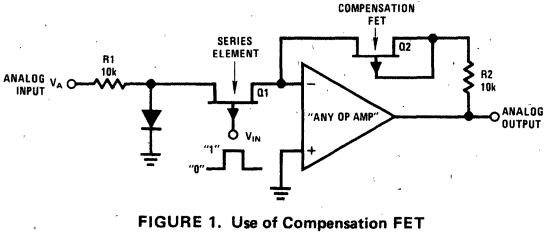


FIGURE 1. Use of Compensation FET

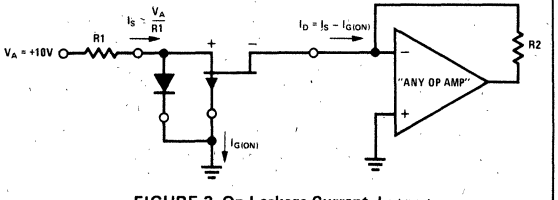


FIGURE 2. On Leakage Current, $I_{G(ON)}$

applications information (con't)

TTL Compatibility

Two input logic drive versions of AM/AH series are available: the even numbered part types are specified to be driven from standard 5V-TTL logic and the odd numbered types from 15V open collector TTL.

Standard TTL gates pull-up to about 3.5V (no load). In order to ensure turn-off of the even numbered switches such as AM9710, a pull-up resistor, R_{EXT}, of at least 10 kΩ should be placed between the 5V V_{CC} and the gate output as shown in *Figure 4.*

Likewise, the open-collector, high voltage TTL outputs should use a pull-up resistor as shown in *Figure 5.* In both cases, $t_{(OFF)}$ is improved for lower values of R_{EXT} and the expense of power dissipation in the low state.

CMOS Compatibility

The cost effective AM97C09 series of switches is optimized for CMOS drive without resistor pull-up. The AM97C10's and AM97C12's are specified for 5V–10V operation while the AM97C09's and AM97C11's are specified for 10V–15V operation.

Definition of Terms

The terms referred to in the electrical characteristics tables are as defined in *Figure 6.*

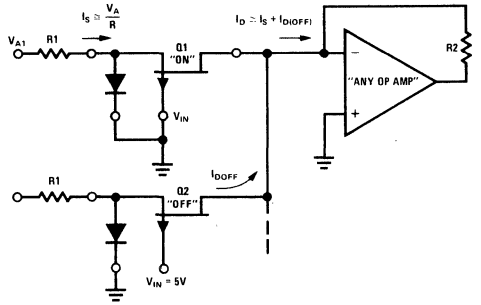


FIGURE 3.

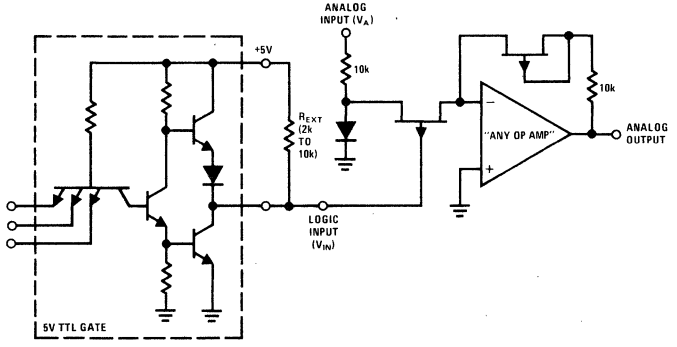


FIGURE 4. Interfacing with +5V TTL

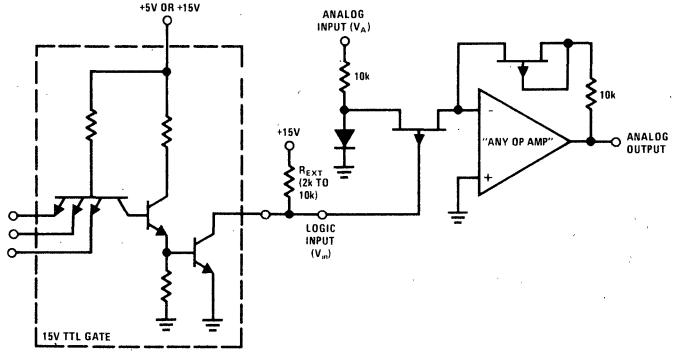


FIGURE 5. Interfacing with +15V Open Collector TTL

applications information (con't)

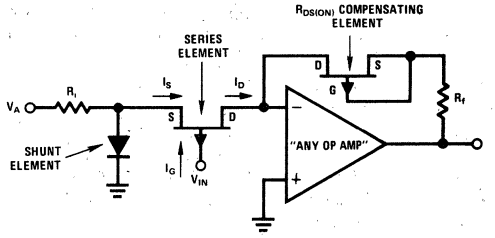
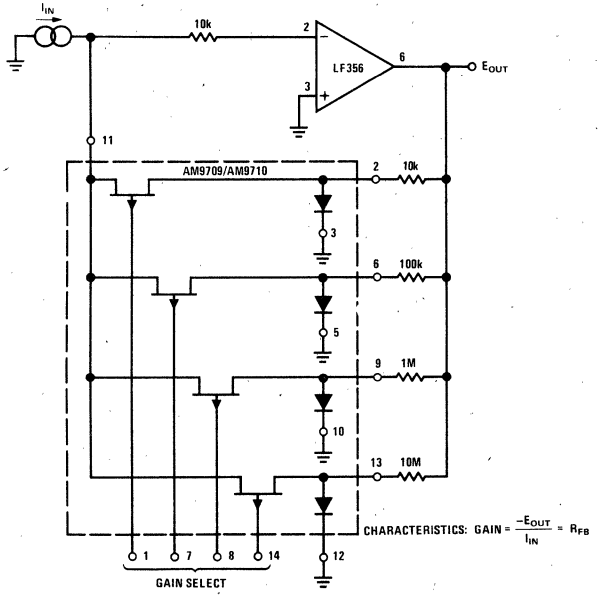


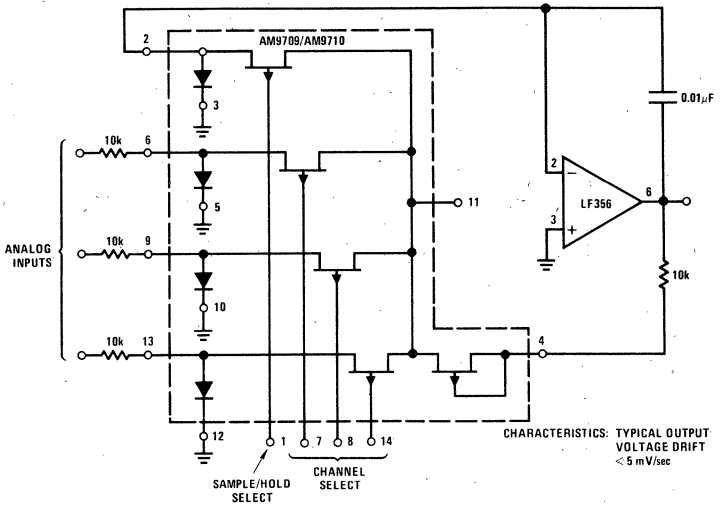
FIGURE 6. Definition of Terms

typical applications

Gain Programmable Amplifier

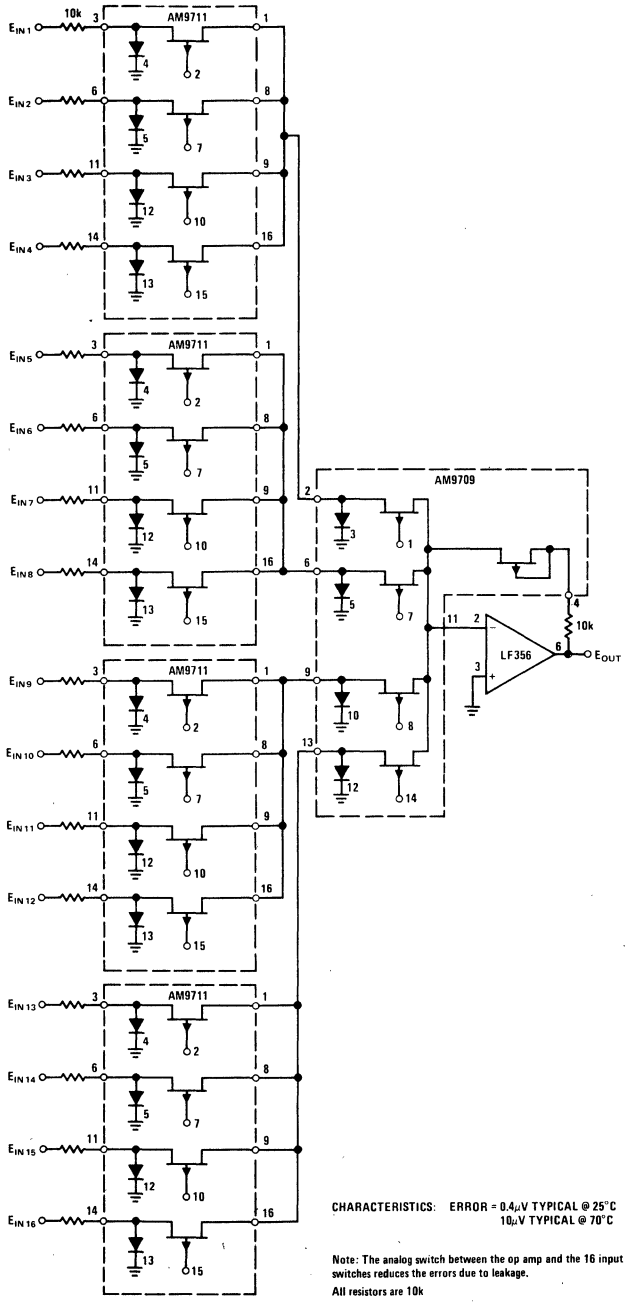


3-Channel Multiplexer with Sample and Hold



typical applications (con't)

16-Channel Multiplexer



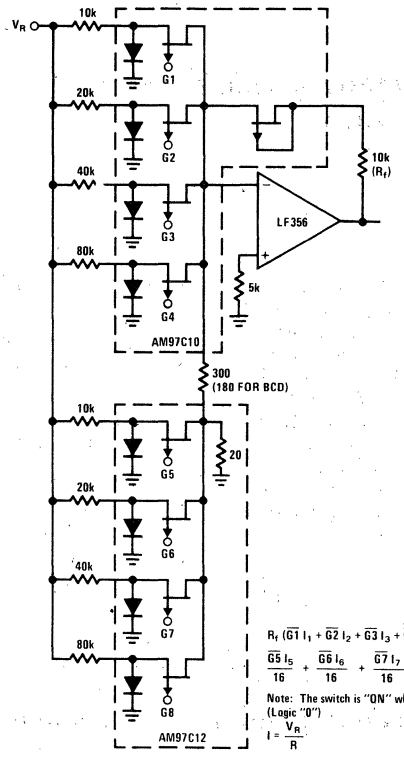
CHARACTERISTICS: ERROR = 0.4μV TYPICAL @ 25°C
10μV TYPICAL @ 70°C

Note: The analog switch between the op amp and the 16 input switches reduces the errors due to leakage.

All resistors are 10k

typical applications (con't)

8-Bit Binary (BCD) Multiplying D/A Converter



$$R_f\left(\overline{G1}\,I_1 + \overline{G2}\,I_2 + \overline{G3}\,I_3 + \overline{G4}\,I_4 + \frac{\overline{G5}\,I_5}{16} + \frac{\overline{G6}\,I_6}{16} + \frac{\overline{G7}\,I_7}{16} + \frac{\overline{G8}\,I_8}{16}\right)$$

Note: The switch is "ON" when G is at 0V (Logic "0")

$$I = \frac{V_R}{R}$$

Analog Switches

AM1000,AM1001,AM1002 silicon N-channel high speed analog switch

general description

The AM1000 series are junction FET integrated circuit analog switches. These devices commutate faster and with less voltage spiking than any other analog switch presently available. By comparison, discrete JFET switches require elaborate drive circuits to obtain reasonable performance for high toggle rates. Encapsulated in a four pin TO-72 package, these units require a minimum of circuit board area. Switching transients are greatly reduced by a monolithic integrated circuit process. The resulting analog switch device provides the following features:

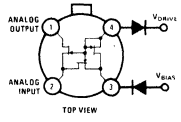
- Low ON Resistance 30Ω
- High Analog Signal Frequency 100 MHz
- High Toggle Rate 4 MHz
- Low Leakage Current 250 pA
- Large Analog Signal Swing ±15V
- Break Before Make Action

The AM1000 series of analog switches are particularly suitable for the following applications:

- High Speed Commutators
- Multiplexers
- Sample and Hold Circuits
- Reset Switching
- Video Switching

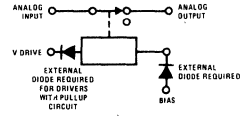
schematic and connection diagram

TO-72 Package



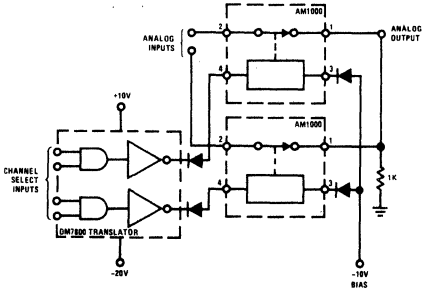
Order Number AM1000H or AM1001H or AM1002H
See Package 8

equivalent circuit

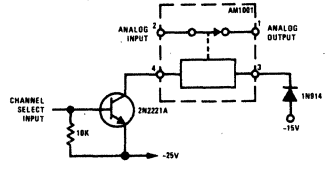


typical applications

±10 Volt Swing Analog Switch 0.5% Accuracy



±15 Volt Swing Analog Switch



absolute maximum ratings

	AM1001	AM1000 AM1002
V_{IN} (Note 1)	+50V	+40V
V_{OUT} (Note 1)	+50V	+40V
V_{DRIVE} (Note 1)	−50V	−40V
V_{BIAS} (Note 1)	+50V	+40V

Power Dissipation @ T_A = 25°C	300 mW
Linear Derating Factor	1.7 mW/°C
Power Dissipation @ T_C = 125°C	150 mW
Linear Derating Factor	6 mW/°C
Maximum Junction Operating Temperature	−55°C to +150°C
Storage Temperature	+200°C
Lead Temperature (Soldering, 10 sec)	+300°C

electrical characteristics

ON CHARACTERISTICS (Note 2)

PARAMETER	CONDITION		MIN	TYP	MAX	UNITS
R_{ON}	V_{DRIVE} = +15V, V_{BIAS} = −15V I_{IN} = 1 mA, V_{OUT} = 0V	AM1001	20	40	50	Ω
R_{ON}	V_{DRIVE} = +10V, V_{BIAS} = −10V I_{IN} = 1 mA, V_{OUT} = 0V	AM1000 AM1002	20 20	25 50	30 100	Ω Ω

OFF CHARACTERISTICS

PARAMETER	CONDITION	AM1000 AM1001			AM1002			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
$I_{OUT(OFF)}$	V_{DRIVE} = −20V, V_{BIAS} = −10V V_{IN} = −10V, V_{OUT} = +10V							
	T_A = +25°C		05	.25		0.5	1	nA
	T_A = +125°C		.025	.25		0.2	1	μA
$I_{OUT(OFF)}$	V_{DRIVE} = −20V, V_{BIAS} = −10V V_{IN} = +10V, V_{OUT} = −10V							
	T_A = +25°C		.05	.25		0.5	1	nA
	T_A = +125°C		.05	.25		0.2	1	μA

DRIVE CHARACTERISTICS (Note 3)

PARAMETER	CONDITION		MIN	TYP	MAX	UNITS
I_{DRIVE} (Switch OFF)	V_{DRIVE} = −20V, V_{BIAS} = −10V V_{IN} = ±10V, V_{OUT} = ±10V	AM1000, 1001, 1002		5	10	mA

SWITCHING CHARACTERISTICS

PARAMETER	CONDITION	AM1000 MAX	AM1001 MAX	AM1002 MAX	UNITS
t_{ON}	See Switching Time Test Circuit	100	150	200	ns
t_{OFF}		100	100	100	ns

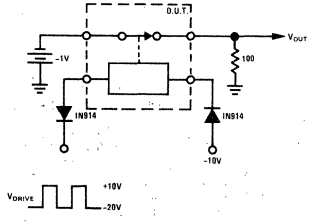
Note 1: The maximum voltage ratings may be applied between any pin or pins simultaneously. Power dissipation may be exceeded in some modes if the voltage pulse exceeds 10 ms. Normal operation will not cause excessive power dissipation even in a "D.C." switching application.

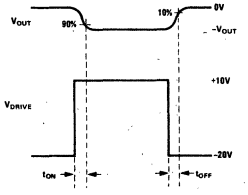
Note 2: All parameters are measured with external silicon diodes. See electrical connection diagram for proper diode placement.

Note 3: I_{BIAS} (Switch OFF) is equal to I_{DRIVE} (Switch OFF). $I_{(BIAS)}$ (Switch ON), is equal to external diode leakage.

Note 4: Rise and fall times of V_{DRIVE} shall be 15 ns maximum for switching time testing.

switching time test circuit and waveforms





NATIONAL

Analog Switches

AM2009/AM2009C/MM4504/MM5504
six channel MOS multiplex switches

general description

The AM2009/AM2009C/MM4504/MM5504 are six channel multiplex switches constructed on a single silicon chip using low threshold P-channel MOS process. The gate of each MOS device is protected by a diode circuit.

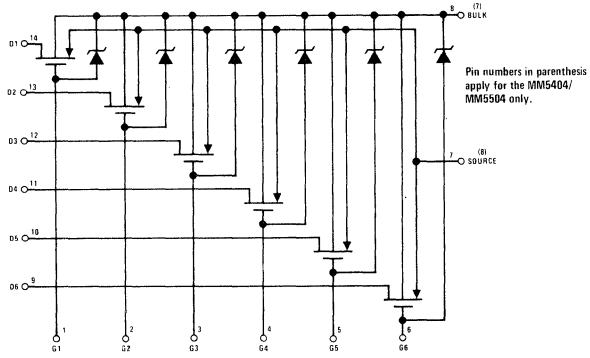
The AM2009/AM2009C/MM4504/MM5504 are designed for applications such as time division multiplexing of analog or digital signals. Switching speeds are primarly determined by conditions external to the device such as signal source impedance, capacitive loading and the total number of channels used in parallel.

The AM2009/MM4504 are specified for operation over the -55°C to +125°C military temperature range. The AM2009C/MM5504 are specified for operation over the -25°C to +85°C temperature range.

features

- Typical low "on" resistance 150Ω
- Typical low "off" leakage 100 pA
- Typical large analog voltage range ±10V
- Zero inherent offset voltage
- Normally off with zero gate voltage

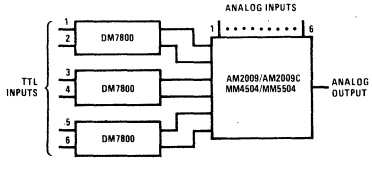
schematic diagram



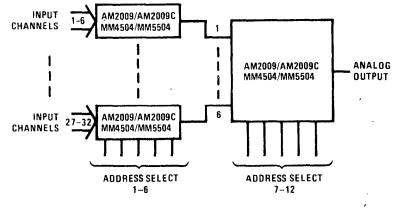
Order Number
AM2009F or AM2009CF
MM4504F or MM5504F
See Package 4

Order Number
AM2009D or AM2009CD
MM4504D or MM5504D
See Package 1

typical applications



TTL Compatible 6 Channel MUX



32 Channel MUX

absolute maximum ratings (V_{BULK} = 0V)

Voltage on Any Source or Drain	−30V	Total Power Dissipation (at T_A = 25°C)	900 mW
Voltage on Any Gate	−35V	Power Dissipation — each gate circuit	150 mW
Positive Voltage on Any Pin	+0.3V	Operating Temperature Range AM2009	−55°C to +125°C
Source or Drain Current	50 mA	AM2009C	−25°C to +85°C
Gate Current (forward direction of zener clamp)	0.1 mA	Storage Temperature Range	−65°C to +150°C
		Lead Temperature (Soldering, 10 sec)	300°C

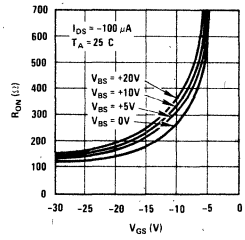
electrical characteristics (Note 1)

PARAMETER	CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Threshold Voltage	$V_{GS} = V_{DS}$, $I_{DS} = -1\ \mu A$	−1.0		−3.0	V
DC ON Resistance	$V_{GS} = -20V$, $I_{DS} = -100\ \mu A$, $T_A = 25°C$		150	250	Ω
DC ON Resistance	$V_{GS} = -10V$, $V_{SB} = -20V$, $I_{DS} = -100\ \mu A$, $T_A = 25°C$		500	1250	Ω
DC ON Resistance	$V_{GS} = -20V$, $I_{DS} = -100\ \mu A$			325	Ω
DC ON Resistance	$V_{GS} = -10V$, $V_{SB} = -20V$, $I_{DS} = -100\ \mu A$			1500	Ω
Gate Leakage	$V_{GS} = -20V$, Note 2			1.0	μA
	$V_{GS} = -20V$, Note 2, $T_A = 25°C$		100		pA
Input Leakage	$V_{DS} = -20V$, Note 2			1.0	μA
	$V_{DS} = -20V$, Note 2, $T_A = 25°C$		100		pA
Output Leakage	$V_{SD} = -20V$, Note 2			3.0	μA
	$V_{SD} = -20V$, Note 2, $T_A = 25°C$		500		pA
Gate-Bulk Breakdown Voltage	$I_{GB} = -10\ \mu A$, Note 2	−35			V
Source-Drain Breakdown Voltage	$I_{SD} = -10\ \mu A$, $V_{GD} = 0$, Note 2	−30			V
Drain-Source Breakdown Voltage	$I_{DS} = -10\ \mu A$, $V_{GS} = 0$, Note 2	−30			V
Transconductance			4000		mhos
Gate Capacitance	Note 3, f = 1 MHz		4.7	8	pF
Input Capacitance	Note 3, f = 1 MHz		4.6	8	pF
Output Capacitance	Note 3, f = 1 MHz		16	20	pF

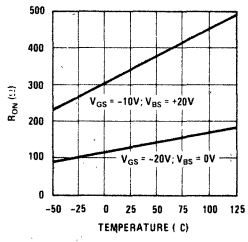
Note 1: Ratings apply over the specified temperature range and V_{BULK} = 0, unless otherwise specified.
Note 2: All other pins grounded
Note 3: Capacitance measured on dual-in-line package between pin under measurement to all other pins. Capacitances are guaranteed by design.

typical performance characteristics

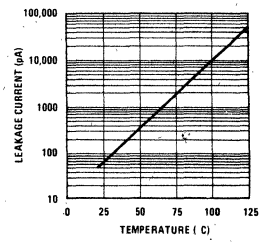
"ON" Resistance vs Gate-to-Source Voltage



"ON" Resistance vs T Temperature



Input Leakage Current vs Temperature



Analog Switches

AM3705/AM3705C 8-channel MOS analog multiplexer general description

The AM3705/AM3705C is an eight-channel MOS analog multiplex switch. TTL compatible logic inputs that require no level shifting or input pull-up resistors and operation over a wide range of supply voltages is obtained by constructing the device with low threshold P-channel enhancement MOS technology. To simplify external logic requirements, a one-of-eight decoder and an output enable are included in the device.

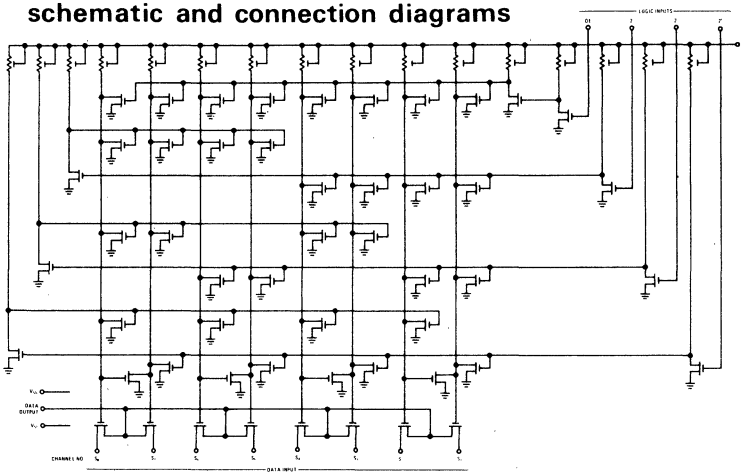
Important design features include:

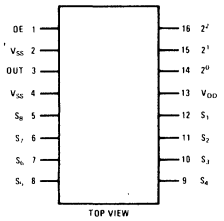
- TTL/DTL compatible input logic levels
- Operation from standard +5V and -15V supplies
- Wide analog voltage range — ±5V
- One-of-eight decoder on chip
- Output enable control
- Low ON resistance — 150Ω
- Input gate protection
- Low leakage currents — 0.5 nA

The AM3705/AM3705C is designed as a low cost analog multiplex switch to fulfill a wide variety of data acquisition and data distribution applications including cross-point switching, MUX front ends for A/D converters, process controllers, automatic test gear, programmable power supplies and other military or industrial instrumentation applications.

The AM3705 is specified for operation over the -55°C to +125°C military temperature range. The AM3705C is specified for operation over the -25°C to +85°C temperature range.

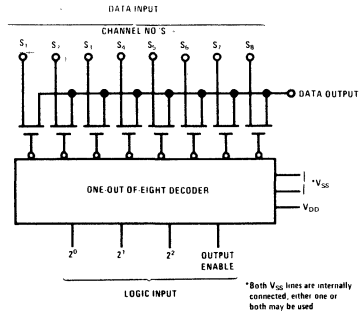
schematic and connection diagrams





Order Number
AM3705D or AM3705CD
See Package 2
AM3705F or AM3705CF
See Package 5
AM3705CN
See Package 18

block diagram (MIL-STD-806B)

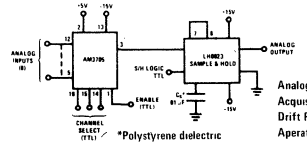


truth table

LOGIC INPUTS				CHANNEL
2^0	2^1	2^2	OE	ON
L	L	L	H	S_1
H	L	L	H	S_2
L	H	L	H	S_3
H	H	L	H	S_4
L	L	H	H	S_5
H	L	H	H	S_6
L	H	H	H	S_7
H	H	H	H	S_8
X	X	X	L	OFF

typical application

Buffered 8-Channel Multiplex, Sample and Hold



Analog Signal Range: +5V
Acquisition Time: 25 ns
Drift Rate: 0.5 mV/sec
Aperature Time: 250 ns

absolute maximum ratings

Positive Voltage on Any Pin (Note 1)		+0.3V
Negative Voltage on Any Pin (Note 1)		−35V
Source to Drain Current		±30 mA
Logic Input Current		±0.1 mA
Power Dissipation (Note 2)		500 mW
Operating Temperature Range	AM3705	−55°C to +125°C
	AM3705C	−25°C to +85°C
Storage Temperature Range		−65°C to +150°C
Lead Temperature (Soldering, 10 sec)		300°C

electrical characteristics (Note 3)

PARAMETER	SYMBOL	CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
ON Resistance	R_{ON}	$V_{IN} = V_{SS}$; $I_{OUT} = 100\ \mu A$		80	250	Ω
ON Resistance	R_{ON}	$V_{IN} = -5V$; $I_{OUT} = -100\ \mu A$		160	400	Ω
ON Resistance	R_{ON}	$V_{IN} = -5V$, $I_{OUT} = -100\ \mu A$				
AM3705		$T_A = +125°C$			400	Ω
AM3705C		$T_A = +70°C$			400	Ω
ON Resistance	R_{ON}	$V_{IN} = +5V$; $V_{DD} = -15V$, $I_{OUT} = 100\ \mu A$		100		Ω
ON Resistance	R_{ON}	$V_{IN} = 0V$, $V_{DD} = -15V$, $I_{OUT} = -100\ \mu A$		150		Ω
ON Resistance	R_{ON}	$V_{IN} = -5V$; $V_{DD} = -15V$; $I_{OUT} = -100\ \mu A$		250		Ω
OFF Resistance	R_{OFF}			10^{10}		Ω
Output Leakage Current	I_{LO}	$V_{SS} - V_{OUT} = 15V$		0.5	10	nA
AM3705	I_{LO}	$V_{SS} - V_{OUT} = 15V$; $T_A = 125°C$		150	500	nA
AM3705C	I_{LO}	$V_{SS} - V_{OUT} = 15V$; $T_A = 70°C$		35	500	nA
Data Input Leakage Current	I_{LDI}	$V_{SS} - V_{IN} = 15V$		0.1	3.0	nA
AM3705	I_{LDI}	$V_{SS} - V_{IN} = 15V$; $T_A = 125°C$		25	500	nA
AM3705C	I_{LDI}	$V_{SS} - V_{IN} = 15V$, $T_A = 70°C$		0.5	500	nA
Logic Input Leakage Current	I_{LI}	$V_{SS} - V_{Logic\ In} = 15V$		.001	1	μA
AM3705	I_{LI}	$V_{SS} - V_{Logic\ In} = 15V$; $T_A = 125°C$		.05	10	μA
AM3705C	I_{LI}	$V_{SS} - V_{Logic\ In} = 15V$; $T_A = 70°C$		.05	10	μA
Logic Input LOW Level	V_{IL}	$V_{SS} = +5.0V$		0.5	1.0	V
Logic Input LOW Level	V_{IL}		V_{DD}		$V_{SS} - 4.0$	V
Logic Input HIGH Level	V_{IH}	$V_{SS} = +5.0V$	3.0	3.5		V
Logic Input HIGH Level	V_{IH}		$V_{SS} - 2.0$		$V_{SS} + 0.3$	V
Channel Switching Time-Positive	t^+	Switching Time Test Circuit		300		ns
Channel Switching Time-Negative	t^-			600		ns
Channel Separation		f = 1 kHz		62		dB
Output Capacitance	C_{db}	$V_{SS} - V_{OUT} = 0$; f = 1 MHz		35		pF
Data Input Capacitance	C_{sb}	$V_{SS} - V_{DIP} = 0$; f = 1 MHz		6.0		pF
Logic Input Capacitance	C_{cg}	$V_{SS} - V_{Logic\ In} = 0$; f = 1 MHz		6.0		pF
Power Dissipation	P_D	$V_{DD} = -31V$, $V_{SS} = 0V$		125	175	mW

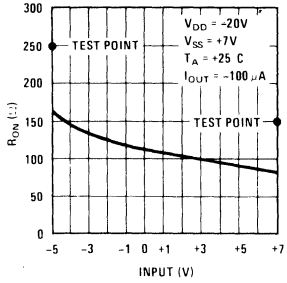
Note 1: All voltages referenced to V_{SS}.

Note 2: Rating applies for ambient temperatures to +25°C, derate linearly at 3 mW/°C for ambient temperatures above +25°C.

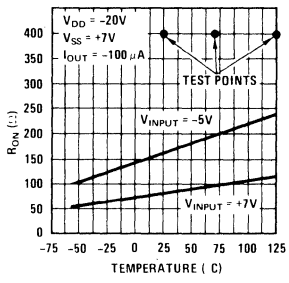
Note 3: Specifications apply for $T_A = 25°C$, $-24V \leq V_{DD} \leq -20V$, and $+5.0V \leq V_{SS} \leq +7.0V$; unless otherwise specified (all voltages are referenced to ground).

typical performance characteristics

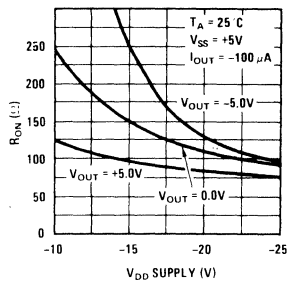
ON Resistance vs Analog Input Voltage



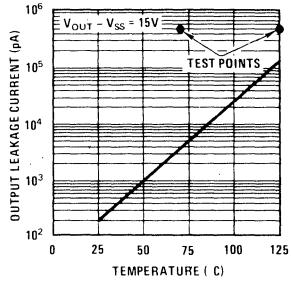
ON Resistance vs Ambient Temperature



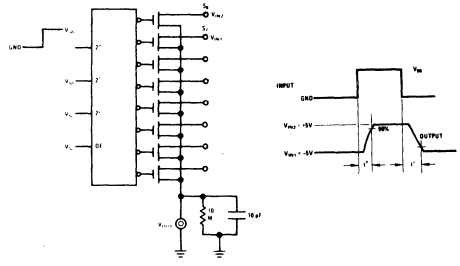
ON Resistance vs V_{DD} Supply Voltage



Output Leakage Current vs Ambient Temperature

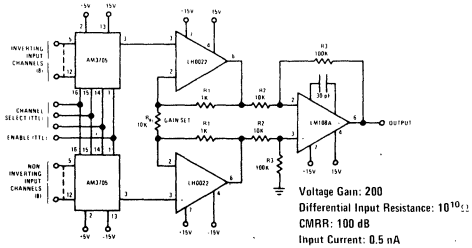


switching time test circuit



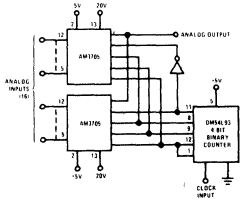
typical applications (con't.)

Differential Input MUX

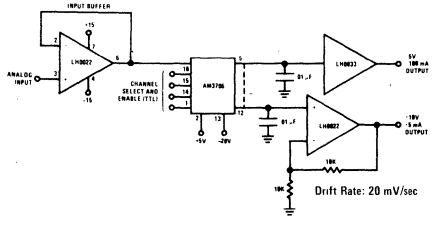


Voltage Gain: 200
Differential Input Resistance: $10^{10}\Omega$
CMRR: 100 dB
Input Current: 0.5 nA

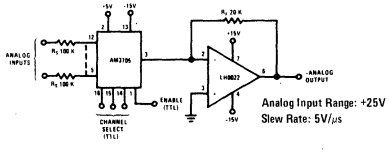
16-Channel Commutator



8-Channel Demultiplexer with Sample and Hold



Wide Input Range Analog Switch



Analog Input Range: +25V
Slew Rate: 5V/μs

NATIONAL

Analog Switches

MM450/MM550, MM451/MM551
MM452/MM552, MM455/MM555 MOS analog switches

general description

The MM450 and MM550 series each contain four p channel MOS enhancement mode transistors built on a single monolithic chip. The four transistors are arranged as follows:

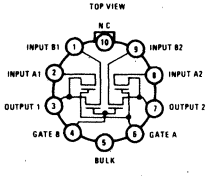
MM450, MM550	Dual Differential Switch
MM451, MM551	Four Channel Switch
MM452, MM552	Four MOS Transistor Package
MM455, MM555	Three MOS Transistor Package

These devices are useful in many airborne and ground support systems requiring multiplexing, analog transmission, and numerous signal routing applications. The use of low threshold transistors (V_{TH} = 2 volts) permits operations with large analog input swings (±10 volts) at low gate voltages (-20 volts). Significant features, then, include:

- Large Analog Input Swing ±10 Volts
- Low Supply Voltage V_{BULK} = +10 Volts
- Low ON Resistance V_{IN} = −10V, 150Ω; V_{IN} = +10V, 150Ω
- Low Leakage Current 200 pA @ 25°C
- Input Gate Protection
- Zero Offset Voltage

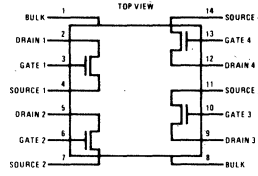
Each gate input is protected from static charge build-up by the incorporation of zener diode protective devices connected between the gate input and device bulk. The MM450, MM451, MM452 and MM455 are specified for operation over the -55°C to +125°C military temperature range. The MM550, MM551, MM552 and MM555 are specified for operation over the -25°C to +70°C temperature range.

schematic and connection diagrams



NOTE: Pin 5 connected to case and device bulk.
MM450, MM550

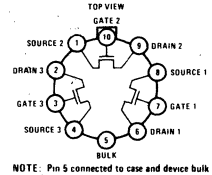
Order Number MM450H or MM550H
See Package 10



NOTE 1: Pins 1 and 8 connected to case and device bulk. Drain and Source may be interchanged. MM452F, MM552F.
NOTE 2: MM452D and MM552D (dual-in-line packages) have same pin connections as MM452F and MM552F shown above.

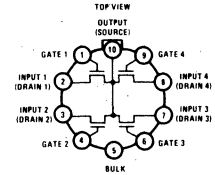
Order Number MM452F or MM552F
See Package 4

Order Number MM452D or MM552D
See Package 1



NOTE: Pin 5 connected to case and device bulk
Drain and Source may be interchanged.
MM455, MM555

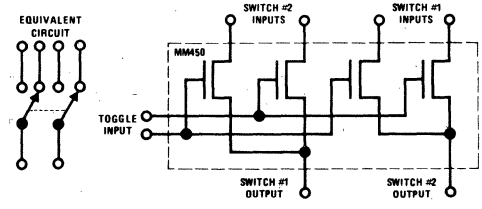
Order Number MM455H or MM555H
See Package 10



NOTE: Pin 5 connected to case and device bulk.
MM451, MM551

Order Number MM451H or MM551H
See Package 10

typical applications



DPDT Analog Switch

absolute maximum ratings

	MM450, MM451, MM452, MM455	MM550, MM551, MM552, MM555
Gate Voltage (V_{GG})	+10V to −30V	+10V to −30V
Bulk Voltage (V_{BULK})	+10V	+10V
Analog Input (V_{IN})	+10V to −20V	+10V to −20V
Power Dissipation	200 mW	200 mW
Operating Temperature	−55°C to +125°C	−25°C to 70°C
Storage Temperature	−65°C to +150°C	−65°C to +150°C

electrical characteristics

STATIC CHARACTERISTICS (Note 1)

PARAMETER	CONDITION	MIN	TYP	MAX	UNITS
Analog Input Voltage				±10	V
Threshold Voltage ($V_{GS(T)}$)	V_{DG} = 0, I_D = 1 μA	1.0	2.2	3.0	V
ON Resistance	V_{IN} = −10V		150	600	Ω
ON Resistance	V_{IN} = V_{SS}		75	200	Ω
OFF Resistance			10^{10}		Ω
Gate Leakage Current (I_{GSB})	V_{GS} = −25V, V_{BS} = 0, T_A = 25°C		20		pA
Input (Drain) Leakage Current					
MM450, MM451, MM452, MM455	T_A = 25°C		.025	100	nA
	T_A = 85°C		.002	1.0	μA
	T_A = 125°C		.025	1.0	μA
Input (Drain) Leakage Current					
MM550, MM551, MM552, MM555	T_A = 25°C		0.1	100	nA
	T_A = 70°C		.030	1.0	μA
Output (Source) Leakage Current					
MM450, MM451, MM452, MM455	T_A = 25°C		.040	100	nA
Output (Source) Leakage Current					
MM450	T_A = 85°C			1.0	μA
MM451	T_A = 85°C			1.0	μA
MM452, MM455	T_A = 85°C			1.0	μA
MM450, MM451, MM452, MM455	T_A = 125°C			1.0	μA
Output (Source) Leakage Current					
MM550	T_A = 70°C			1.0	μA
MM551	T_A = 70°C			1.0	μA
MM552, MM555	T_A = 70°C			1.0	μA
DYNAMIC CHARACTERISTICS					
Large Signal Transconductance	V_{DS} = −10V, I_D = 10 mA f = 1 kHz		4000		μmhos

CAPACITANCE CHARACTERISTICS (Note 2)

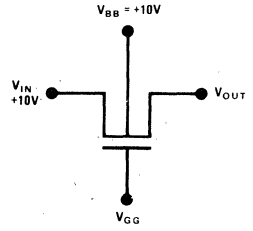
PARAMETER	DEVICE TYPE	MIN	TYP	MAX	UNITS
Analog Input (Drain) Capacitance (C_{DB})	ALL		8	10	pF
Output (Source) Capacitance (C_{SB})	MM450, MM550		11	14	pF
	MM451, MM551		20	24	pF
	MM452, MM552		7.5	11	pF
	MM455, MM555		7.5	11	pF
Gate Input Capacitance (C_{GB})	MM450, MM550		10	13	pF
	MM451, MM551		5.5	8	pF
	MM452, MM552		5.5	9	pF
	MM455, MM555		5.5	9	pF
Gate to Output Capacitance (C_{GS})	ALL		3.0	5	pF

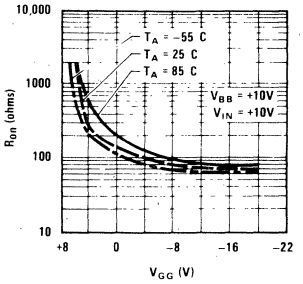
Note 1: The resistance specifications apply for $-55°C \leq T_A \leq +85°C$, V_{GG} = −20V, V_{BULK} = +10V, and a test current of 1 mA. Leakage current is measured with all pins held at ground except the pin being measured which is biased at −25V.

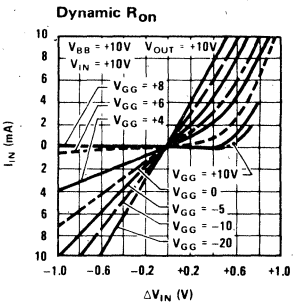
Note 2: All capacitance measurements are made at 0 volts bias at 1 MHz.

typical dynamic input characteristics (T_A = 25°C Unless Otherwise Noted)

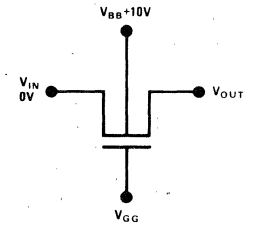
CONDITION 1:
ANALOG INPUT VOLTAGE
AT +10 VOLTS

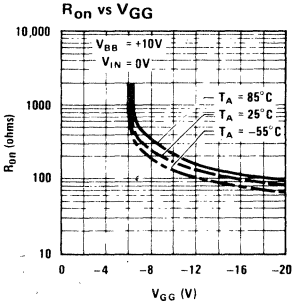


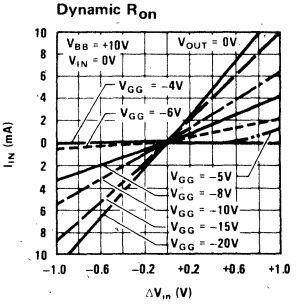




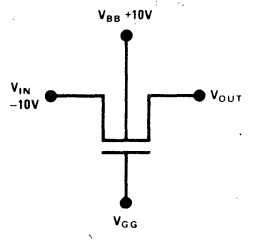
CONDITION 2:
ANALOG INPUT VOLTAGE
AT 0 VOLTS

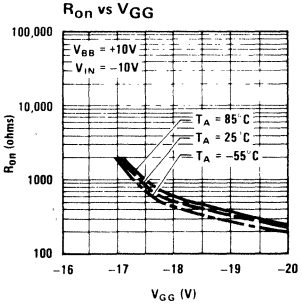


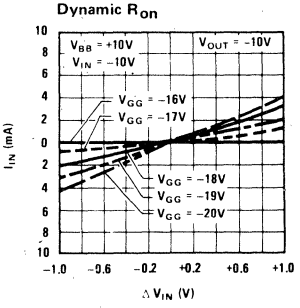


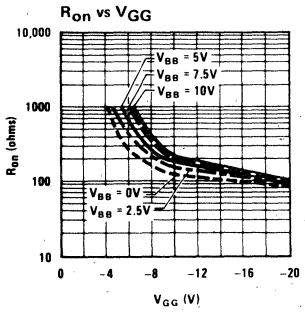


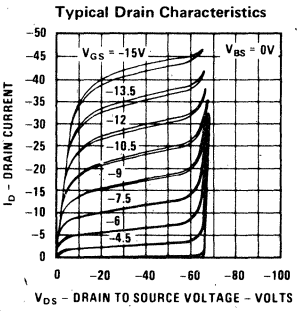
CONDITION 3:
ANALOG INPUT VOLTAGE
AT −10 VOLTS

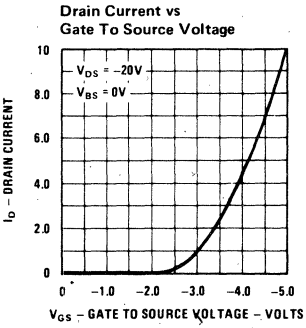






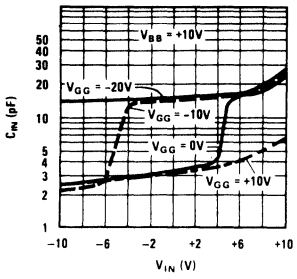




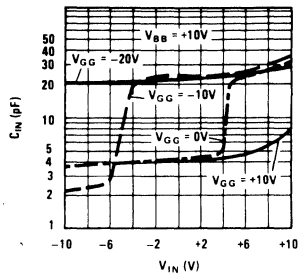


typical input capacitance characteristics

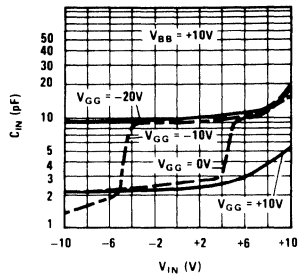
MM450, MM550
C_{IN} vs V_{IN}



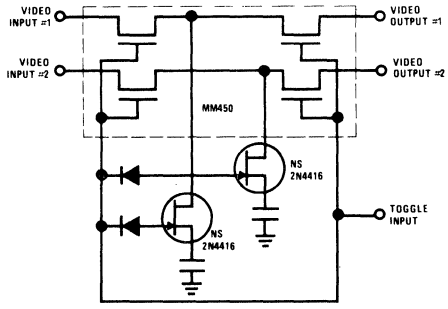
MM451, MM551
C_{IN} vs V_{IN}



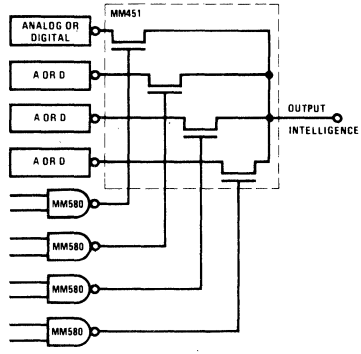
MM452, MM552, MM455, MM555
C_{IN} vs V_{IN}



typical applications (con't)



DPST High-Frequency Switch



4-Channel Multiplexer*

*Expansion in the number of data input lines is possible by using multiple level series switches allowing the same decode gates to be used for all lower rank decoding.

5

NATIONAL

Analog Switches

MM454/MM554 four-channel commutator

general description

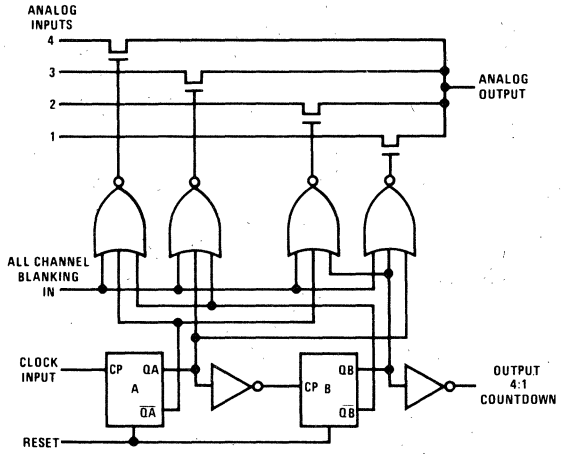
The MM454/MM554 is a four-channel analog commutator capable of switching four analog input channels sequentially onto an output line. The device is constructed on a single silicon chip using MOS P Channel enhancement transistors; it contains all the digital circuitry necessary to sequentially turn ON the four analog switch transistors permitting multiplexing of the analog input data. The device features:

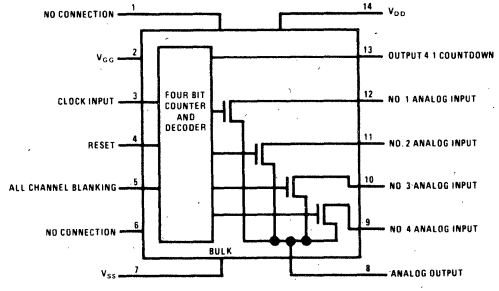
- High Analog Voltage Handling ±10V
- High Commutating Rate 500 kHz
- Low Leakage Current (T_A = 25°C) 200 pA
  (T_A = 85°C) 50 nA
- All Channel Blanking input provided
- Reset capability provided
- Low ON Resistance 200Ω

In addition, the MM454/MM554 can easily be applied where submultiplexing is required since a 4:1 clock countdown signal is provided which can drive the clock input of subsequent MM454/MM554 units.

The MM454 is specified for operation over the −55°C to +125°C military temperature range. The MM554 is specified for operation over the −25°C to +70°C temperature range.

schematic and connection diagrams





Note: Pin 7 connected to case and to device bulk. Nominal Operating Voltages: V_{GG} = −24V; V_{DD} = 0V; V_{SS} = +12V, RESET BIAS = +12V (0V for RESET), ALL CHANNEL BLANKING BIAS = +12V (0V for BLANKING)

Order Number MM454F or MM554F
See Package 4

absolute maximum ratings (Note 1)

Gate Voltage (V_{GG})	+10V to −30V
Bulk Voltage (V_{SS})	+10V
Analog Input (V_{IN})	+10V to −20V
Power Dissipation	200 mW
Operating Temperature MM454	−55°C to +125°C
MM554	−25°C to +70°C
Storage Temperature	−65°C to +150°C

static characteristics (Note 2)

PARAMETER		CONDITION	MIN	TYP	MAX	UNITS
Analog Input Voltage					±10	V
ON Resistance		V_{IN} = −10V		170	600	Ω
ON Resistance		V_{IN} = V_{SS}		90	200	Ω
OFF Resistance				10^{10}		Ω
Analog Input Leakage Current	MM454	T_A = 25°C		.050	100	nA
	MM454	T_A = 85°C		.006	1.0	μA
	MM554	T_A = 25°C		.0001	100	nA
	MM554	T_A = 70°C		.030	1.0	μA
Analog Output Leakage Current	MM454	T_A = 25°C		0.100	100	nA
	MM454	T_A = 85°C		30	1.0	μA
	MM554	T_A = 25°C		.0001	100	nA
	MM554	T_A = 70°C		.030	1.0	μA
V_{SS} Supply Current Drain		V_{SS} = +12V		3.8	5.5	mA
V_{GG} Supply Current Drain		V_{GG} = −24V		2.4	3.5	mA

capacitance characteristics

PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
Analog Input Capacitance Channel OFF	I_{IN} = 0		4	6	pF
Analog Input Capacitance Channel ON	I_{IN} = 0		20	24	pF
Analog Output Capacitance	I_{IN} = 0		20	24	pF
Clock Input	V_{CL} = +12V		2.0		pF
Reset Input	V_{RESET} = +12V		2.0		pF
Blanking Input	V_{BLANK} = +12V		2.0		pF

clock characteristics (Note 3)

PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
Clock Input (HIGH)[4]		V_{SS} − 2		V_{SS}	V
Clock Input (LOW)		−5	0	+5	V
Clock Input Rise Time (POS GOING)		No requirement			
Clock Input Fall Time (NEG GOING)				20	μsec
Countdown Output (POS) V_{OH}		V_{SS} −2		V_{SS}	V
Countdown Output (NEG) V_{OL}			0		V
Maximum Commutation Rate		0.5	2.0		MHz
V_{SS}		+10.0	+12	+14	V

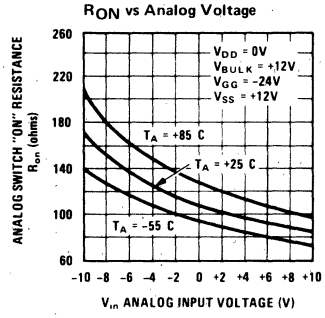
Note 1: Maximum ratings are limiting values above which the device may be damaged. All voltages referenced to V_{DD} = 0.

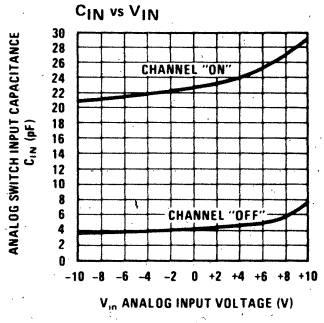
Note 2: These specifications apply over the indicated operating temperature range for V_{GG} = −24V, V_{DD} = 0V, V_{SS} = +12V, V_{RESET} = +12V, V_{BLANK} = +12V. ON resistance measured at 1 mA, OFF resistance and leakage measured with all analog inputs and output common. Capacitance measured at 1 MHz.

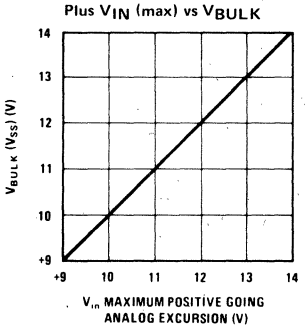
Note 3: Operating conditions in Note 2 apply. V_{SS} to V_{DD} (0V) voltage is applied to counting and gating circuits. V_{GG} is required only for analog switch biasing. All logic inputs are high resistance and are essentially capacitive.

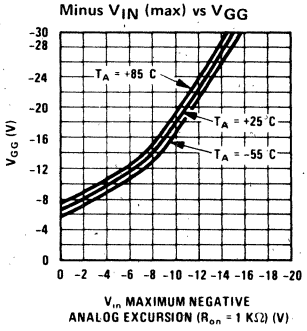
Note 4: Logic input voltage must not be more positive than V_{SS}.

typical performance characteristics

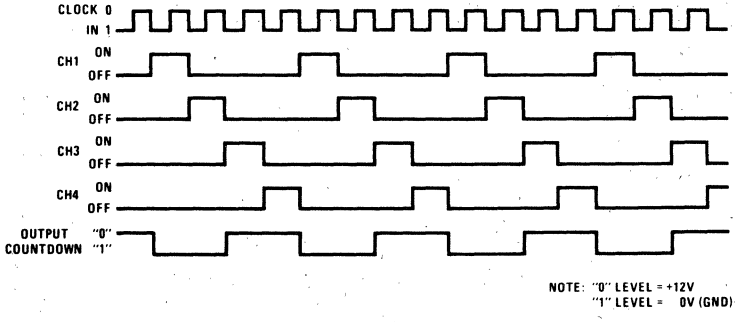








timing diagram



NOTE: "0" LEVEL = +12V
"1" LEVEL = 0V (GND)

Mos Clock Drivers

MH0007/MH0007C dc coupled MOS clock driver

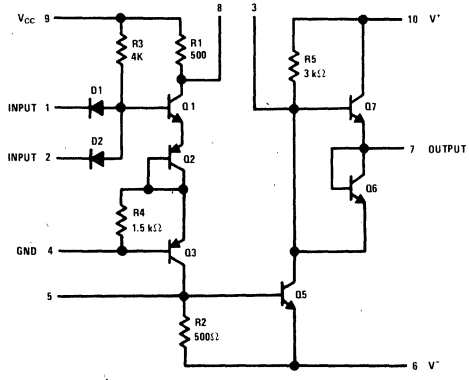
general description

The MH0007 is a voltage translator and power booster designed for interfacing between conventional TTL or DTL voltage levels and those levels associated with inputs or clocks of MOS FET type devices. The design allows the user a wide latitude in selection of supply voltages, and is especially useful in normally "off" applications, since power dissipation is typically only 5 milliwatts in the "off" state.

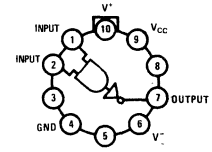
features

- 30 volts (max) output swing
- Standard 5V power supply
- Peak currents in excess of ±300 mA available
- Compatible with all MOS devices
- High speed: 5 MHz with nominal load
- External trimming possible for increased performance

schematic and connection diagram



10 Pin TO-100 Package

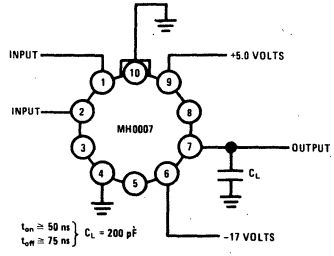


TOP VIEW

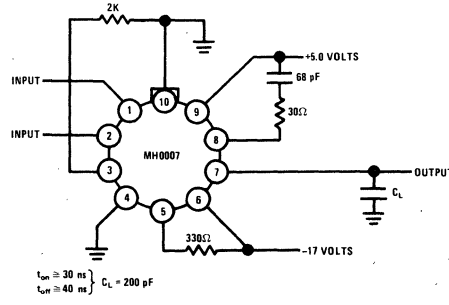
Order Number MH0007H
or MH0007CH
See Package 11

typical applications

Switching Time Test Configuration



High Speed Operation



absolute maximum ratings

V_{CC} Supply Voltage	8V
V^- Supply Voltage	−40V
V^+ Supply Voltage	+28V
$(V^+ - V^-)$ Voltage Differential	30V
Input Voltage	5.5V
Power Dissipation (T_A = 25°C)	800 mW
Peak Output Current	±500 mA
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range MH0007	−55°C to +125°C
MH0007C	0°C to +85°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics (Note 1)

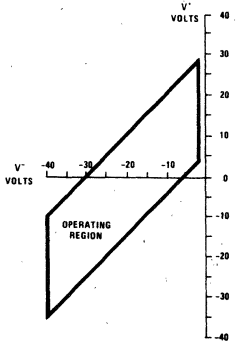
PARAMETER	CONDITIONS	MIN	TYP (Note 2)	MAX	UNITS
Logical "1" Input Voltage	V_{CC} = 4.5V	2.2			V
Logical "0" Input Voltage	V_{CC} = 4.5V			0.8	V
Logical "1" Input Current	V_{CC} = 5.5V, V_{IN} = 5.5V			100	μA
Logical "0" Input Current	V_{CC} = 5.5V, V_{IN} = 0.4V		1.0	1.5	mA
Logical "1" Output Voltage	V_{CC} = 5.5V, I_{OUT} = 30 mA, V_{IN} = 0.8V	V^+ − 4.0			V
	V_{CC} = 5.5V, I_{OUT} = 1 mA, V_{IN} = 0.8V	V^+ − 2.0			V
Logical "0" Output Voltage	V_{CC} = 4.5V, I_{OUT} = 30 mA, V_{IN} = 2.2V			V^- + 2.0	V
Transition Time to Logical "0" Output	C_L = 200 pF (Note 3)		50		ns
Transition Time to Logical "1" Output	C_L = 200 pF (Note 3)		75		ns

Note 1: Min/max limits apply across the guaranteed range of −55°C to +125°C for the MH0007, and from 0°C to +85°C for the MH0007C, for all allowable values of V^- and V^+.

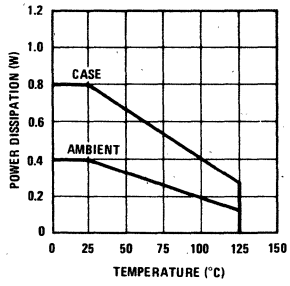
Note 2: All typical values measured at T_A = 25°C with V_{CC} = 5.0 volts, V^- = −25 volts, V^+ = 0 volts.

Note 3: Transition time measured from time V_{IN} = 50% value until V_{OUT} has reached 80% of final value.

Allowable Values for V^- and V^+



Maximum Power Dissipation



Mos Clock Drivers

MH0009/MH0009C dc coupled two phase MOS clock driver

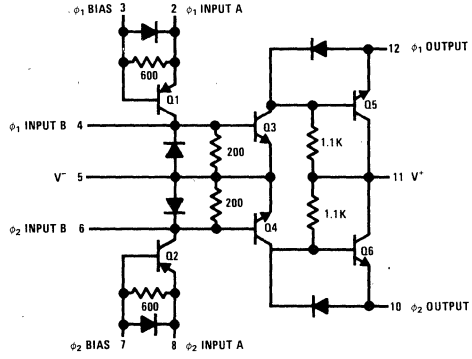
general description

The MH0009/MH0009C is high speed, DC coupled, dual MOS clock driver designed to operate in conjunction with high speed line drivers such as the DM8830, DM7440, or DM7093. The transition from TTL/DTL to MOS logic level is accomplished by PNP input transistors which also assure accurate control of the output pulse width.

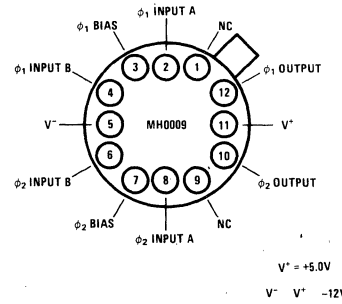
features

- DC logically controlled operation
- Output Swings – to 30V
- Output Currents – in excess of ±500 mA
- High rep rate – in excess of 2 MHz
- Low standby power

schematic and connection diagrams



12-Lead TO-8 Package



Order Number MH0009G
or MH0009CG
See Package 6

typical application

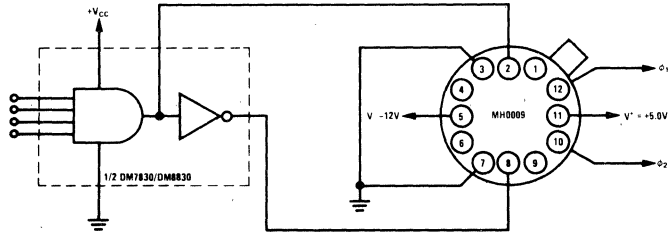


FIGURE 1

absolute maximum ratings

V^- Supply Voltage: Differential (Pin 5 to Pin 3) or (Pin 5 to Pin 7)	−40V
V^+ Supply Voltage: Differential (Pin 11 to Pin 5)	30V
Input Current: (Pin 2, 4, 6 or 8)	±75 mA
Peak Output Current	±500 mA
Power Dissipation (Note 2 and Figure 2)	1.5W
Storage Temperature	−65°C to +150°C
Operating Temperature: MH0009	−55°C to +125°C
MH0009C	0°C to 85°C
Lead Temperature (Soldering, 10 Sec.)	300°C

electrical characteristics (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{ON}	C_{IN} = .0022 μF C_L = .001 μF		10	35	ns
t_{rise}	C_{IN} = .0022 μF C_L = .001 μF		40	50	ns
Pulse Width (50% to 50%)	C_{IN} = .0022 μF C_L = .001 μF	340	400	440	ns
t_{fall}	C_{IN} = .0022 μF C_L = .001 μF		80	120	ns
t_{delay}	C_{IN} = 600 pF C_L = 200 pF		10		ns
t_{rise}	C_{IN} = 600 pF C_L = 200 pF		15		ns
Pulse Width (50% to 50%)	C_{IN} = 600 pF C_L = 200 pF	40	70	120	ns
t_{fall}	C_{IN} = 600 pF C_L = 200 pF		40		ns

Note 1: Characteristics apply for circuit of Figure 1. With V^- = −20 volts; V^+ = 0 volts; V_{CC} = 5.0 volts. Minimum and maximum limits apply from −55°C to +125°C for the MH0009 and from 0°C to +85°C for the MH0009C. Typical values are for T_A = 25°C.
Note 2: Transient power is given by $P = fC_L (V^+ - V^-)^2$ watts, where: f = repetition rate, C_L = load capacitance, and $(V^+ - V^-)$ = output swing.
Note 3: For typical performance data see the MH0013/MH0013C data sheet.

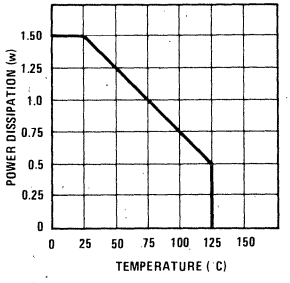


FIGURE 2. Maximum Power Dissipation

Mos Clock Drivers

MH0012/MH0012C high speed MOS clock driver

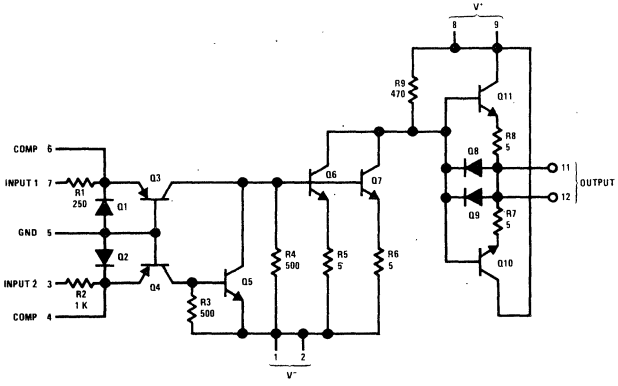
general description

The MH0012/MH0012C is a high performance clock driver that is designed to be driven by the DM7830/DM8830 or other line drivers or buffers with high output current capability. It will provide a fixed width pulse suitable for driving MOS shift registers and other clocked MOS devices.

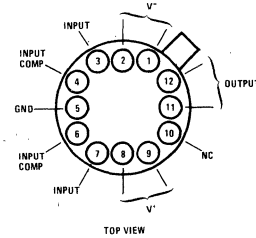
features

- High output voltage swings—12 to 30 volts
- High output current drive capability—1000 mA peak
- High repetition rate—10 MHz at 18 volts into 100 pF
- Low standby power—less than 30 mW

schematic and connection diagrams



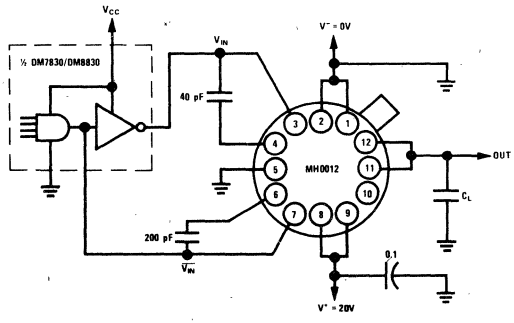
12-lead TO-8 Package



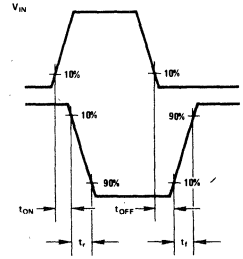
TOP VIEW

Order Number MH0012G or MH0012CG
See Package 6

typical application (ac test circuit)



timing diagram



6

absolute maximum ratings

V^- Supply Voltage: Differential (Pin 1 or 2 to Pin 5)	-40V
V^+ Supply Voltage: Differential (Pin 8 or 9 to Pin 1 or 2)	30V
Input Current: (Pin 3 or 7)	±75 mA
Peak Output Current	±1000 mA
Maximum Output Load–See Figure 2	
Power Dissipation–See Figure 1	1.5W
Storage Temperature	-65°C to +150°C
Operating Temperature: MH0012	-55°C to +125°C
MH0012C	0°C to +85°C
Lead Temperature (Soldering, 10 sec)	300°C

dc electrical characteristics (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Logic "1" Input Voltage (Pins 7 and 3)	$V^+ - V^- = 20V$, $V_{OUT} < V^- + 2V$		1.0	2.0	V
Logic "0" Input Voltage (Pins 7 and 3)	$V^+ - V^- = 20V$, $V_{OUT} > V^+ - 1.5V$	0.4	0.6		V
Logic "1" Output Voltage	$V^+ - V^- = 20V$, $I_{OUT} = 1mA$, $V_{IN} = 2.0V$		V^- + 1.0	V^- + 2.0	V
Logic "0" Output Voltage	$V^+ - V^- = 20V$, $I_{OUT} = -1mA$, $V_{IN} = 0.4V$	$V^+ - 1.5$	$V^+ - 0.7$		V
I_{DC} (V^- Supply)	$V^+ - V^- = 20V$, $V_{IN} = 2.0V$		34	60	mA

ac electrical characteristics

PARAMETER	CONDITIONS (Note 3)	MIN	TYP	MAX	UNITS
Turn-On Delay (t_{ON})	$V^+ - V^- = 20V$, $V_{CC} = 5.0V$ $C_L = 200$ pF, f = 1.0 MHz $T_A = 25°C$		10	15	ns
Rise Time (t_r)			5	10	ns
Turn-Off Delay (t_{OFF})			35	50	ns
Fall Time (t_f)			35	45	ns

Note 1: Characteristics apply for circuit of Figure 1. Min and max limits apply from -55°C to +125°C for the MH0012 and from 0°C to +85°C for the MH0012C. Typical values are for $T_A = 25°C$.

Note 2: Due to the very fast rise and fall times, and the high currents involved, extremely short connections and good by passing techniques are required.

Note 3: All conditions apply for each parameter.

Power Dissipation

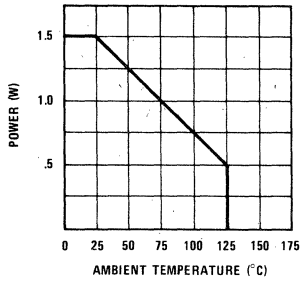


Figure 1.

Maximum Output Load vs Voltage Swing vs Rise Times

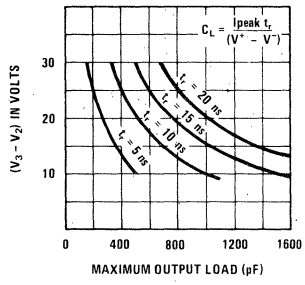
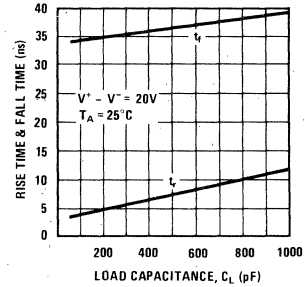


Figure 2.

Rise and Fall Times vs Load Capacitance



applications information

Power Dissipation Considerations

The power dissipated by the MH0012 may be divided into three areas of operation = ON, OFF and switching. The OFF power is approximately 30 mW and is dissipated by R_2 when Pin 3 is in the logic "1" state. The OFF power is neglible and will be ignored in the subsequent discussion. The ON power is dissipated primarily by Q_3 and R_9 and is given by:

$$P_{ON} \cong [V^-|I_{IN} + \frac{(V^+ - V^-)^2}{R_9}] \text{ DC} \quad (1)$$

Where:

$$\text{DC} = \text{Duty Cycle} = \frac{\text{ON Time}}{\text{ON Time \& OFF Time}}$$

I_{IN} is given by $\frac{V_{IN} - V_{BE3}}{R_1}$ and equation (1) becomes:

$$P_{ON} = \left[\frac{(V_{IN} - V_{BE3})|V^-|}{R_1} + \frac{(V^+ - V^-)^2}{R_9}\right] \text{DC} \quad (2)$$

For $V_{IN} = 2.5V$, $V_{BE3} = 0.7V$, $V^+ = 0V$, $V^- = -20V$, and DC = 20%, $P_{ON} \cong 200$ mW.

The transient power incurred during switching is given by:

$$P_{AC} = (V^+ - V^-)^2\, C_L f \quad (3)$$

For $V^+ = 0V$, $V^- = -20V$, $C_L = 200$ pF, and f = 5.0 MHz, $P_{AC} = 400$ mW.

The total power is given by:

$$P_T = P_{AC} + P_{ON} \quad (4)$$

$$P_T \leq P_{MAX}$$

For the above example, $P_T = 600$ mW.

NATIONAL

Mos Clock Drivers

MH0013/MH0013C two phase MOS clock driver

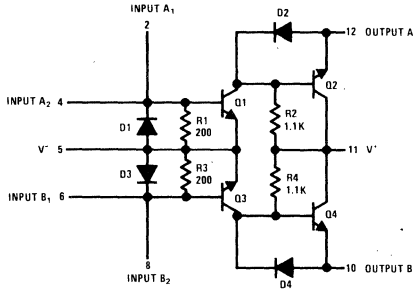
general description

The MH0013/MH0013C is a general purpose clock driver that is designed to be driven by DTL or TTL line drivers or buffers with high output current capability. It will provide fixed width clock pulses for both high threshold and low threshold MOS devices. Two external input coupling capacitors set the pulse width maximum, below which the output pulse width will closely follow the input pulse width or logic control of output pulse width may be obtained by using larger value input capacitors and no input resistors.

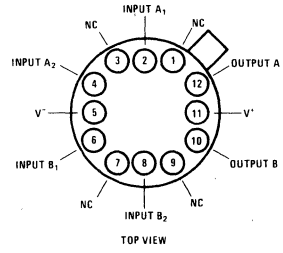
features

- High Output Voltage Swings—up to 30V
- High Output Current Drive Capability—up to 500 mA
- High Repetition Rate—up to 5.0 MHz
- Pin Compatible with the MH0009/MH0009C
- "Zero" Quiescent Power

schematic and connection diagrams

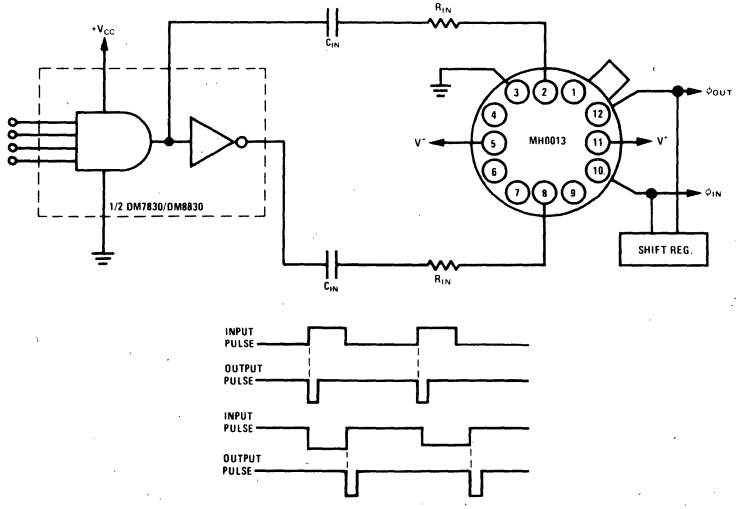


12-Lead TO-8 Package



Order Number MH0013G or MH0013CG
See Package 6

typical applications



absolute maximum ratings

$(V^+ - V^-)$ Voltage Differential	30V
Input Current (Pin 2, 4, 6 or 8)	±75 mA
Peak Output Current	±600 mA
Power Dissipation (Figure 7)	1.5W
Storage Temperature	−65°C to +150°C
Operating Temperature MH0013	−55°C to +125°C
MH0013C	0°C to +85°C
Lead Temperature (Soldering, 10 sec 1/16" from Case)	300°C

electrical characteristics (Note 1 and Figure 8)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Logical "0" Output Voltage	I_{OUT} = −50 mA I_{IN} = 1.0 mA	$V^+ - 3.0$	$V^+ - 1.0$		V
	I_{OUT} = −10 mA I_{IN} = 1.0 mA		$V^+ - 0.7$	$V^+ - 0.5$	V
Logical "1" Output Voltage	I_{OUT} = 50 mA I_{IN} = 10 mA		$V^- + 1.5$	$V^- + 2.0$	V
					V
Power Supply Leakage Current	$(V^+ - V^-)$ = 30V $I_{OUT} = I_{IN}$ = 0 mA		1.0	100	μA
Negative Input Voltage Clamp	I_{IN} = − 10 mA	$V^- - 1.2$	$V^- - 0.8$		V
$t_{d\,ON}$			20	35	ns
t_{rise}			35	50	ns
$t_{d\,OFF}$ (Note 2)	C_{IN} = 0.0022 μF		30	60	ns
t_{fall} (Note 2)	R_{IN} = 0Ω C_L = 0.001 μF	40	50	80	ns
t_{fall} (Note 3)		40	70	120	ns
Pulse Width (50% to 50%) (Note 3)		340	420	490	ns
t_{rise}	C_{IN} = 500 pF		15		ns
t_{fall}	R_{IN} = 0Ω		20		ns
Pulse Width (50% to 50%) (Note 3)	C_L = 200 pF		110		ns
Positive Output Voltage Swing			$V^+ - 0.7V$		V
Negative Output Voltage Swing			$V^- + 0.7V$		V

Note 1: Min/Max limits apply over guaranteed operating temperature range of −55°C to +125°C for MH0013 and 0°C to +85°C for MH0013C, with V^- = −20V and V^+ = 0V unless otherwise specified. Typical values are for 25°C.

Note 2: Parameter values apply for clock pulse width determined by input pulse width.

Note 3: Parameter values apply for input pulse width greater than output clock pulse width.

TABLE I. Typical Drive Capability of One Half MH0013 at 70°C Ambient

$(V_3 - V_2)$ VOLTS	FREQUENCY MHz	PULSE WIDTH ns	TYPICAL R_{IN} Ω	TYPICAL C_{IN} pF	OUTPUT DRIVE CAPABILITY IN pF[1]	RISE TIME LIMIT ns[2]
28					50	
20	4.0	100	0	750	200	7
16					350	10
28					100	5
20	2.0	200	10	1600	400	14.
16					700	19
28					400	19
20	1.0	200	0	2300	1000	34
16					1700	45
28					2800	130
20	0.5	500	10	4000	5500	183
16					9300	248

Note 1: Output load is the maximum load that can be driven at 70°C without exceeding the package rating under the given conditions.

Note 2: The rise time given is the minimum that can be used without exceeding the peak transient output current for the full rated output load.

circuit operation

Input current forced into the base of Q1 through the coupling capacitor C_{IN} causes Q1 to be driven into saturation, swinging the output to $V^- + V_{CE}(SAT) + V_{DIODE}$.

When the input current has decayed, or has been switched, such that Q1 turns off, Q2 receives base drive through R2, turning Q2 on. This supplies current to the load and the output swings positive to $V^+ - V_{BE}$.

It may be noted that Q1 always switches off before Q2 begins to supply current; hence, high internal transient currents from V^+ to V^- cannot occur.

typical performance characteristics

FIGURE 1. Output Load vs Voltage Swing

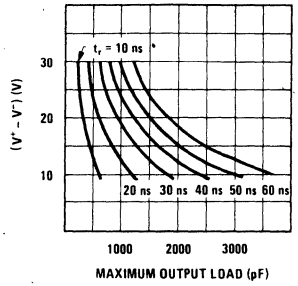


FIGURE 2. Transient Power vs Rep. Rate vs C_L

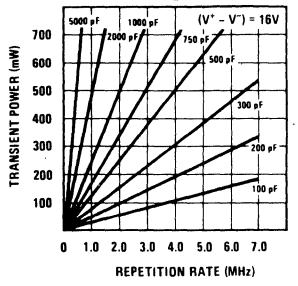


FIGURE 3. Transient Power vs Rep. Rate vs C_L

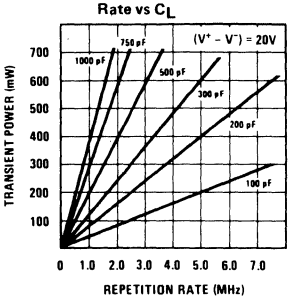


FIGURE 4. Average Internal Power vs Output Swing vs Duty Cycle

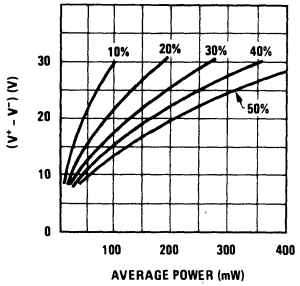


FIGURE 5. Typical Clock Pulse Variations vs Ambient Temperature

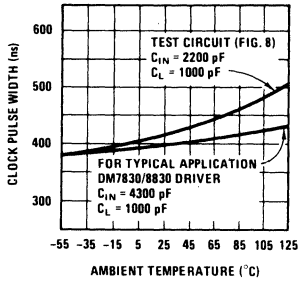


FIGURE 6. R_{IN} vs C_{IN} vs Pulse Width

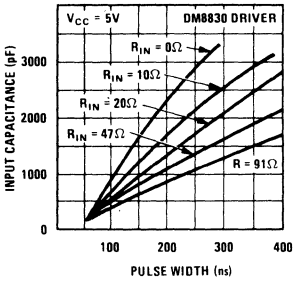
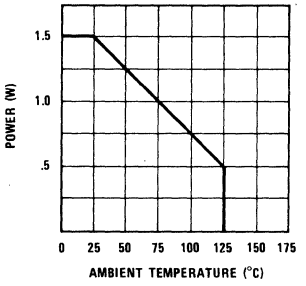


FIGURE 7. Package Power Derating



ac test circuit

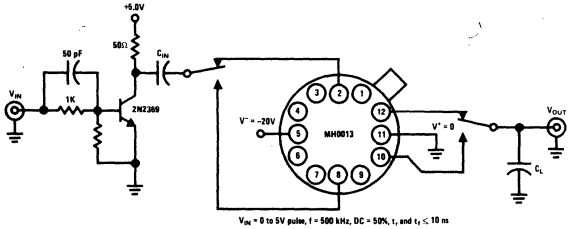
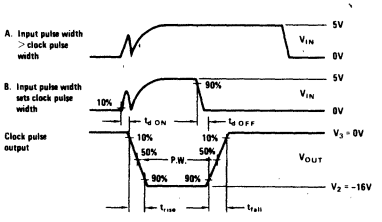


Figure 8

timing diagram



pulse width

Maximum output pulse width is a function of the input driver characteristics and the coupling capacitance and resistance. After being turned on, the input current must fall from its initial value I_{IN} peak to below the input threshold current I_{IN} min $\simeq V_{BE}/R1$ for the clock driver to turn off. For example, referring to the test circuit of Figure 8, the output pulse width, 50% to 50%, is given by

$$pw_{OUT} \cong \frac{1}{2}(t_{rise} + t_{fall}) + R_O C_{IN} \ln \frac{I_{IN}\ peak}{I_{IN}\ min} \cong 400\ ns.$$

For operation with the input pulse shorter than the above maximum pulse width, the output pulse width will be directly determined by the input pulse width.

$$pw_{OUT} = pw_{IN} + t_{d\,OFF} + t_{d\,ON} + \frac{1}{2}(t_{fall} + t_{rise})$$

Typical maximum pulse width for various C_{IN} and R_{IN} values are given in Figure 6.

fan-out calculation

The drive capability of the MH0013 is a function of system requirements, i.e., speed, ambient temperature, voltage swing, drive circuitry, and stray wiring capacity.

The following equations cover the necessary calculations to enable the fan-out to be calculated for any system condition. Some typical fan-outs for conditions are given in Table 1.

Transient Current

The maximum peak output current of the MH0013 is given as 600 mA. Average transient current required from the driver can be calculated from:

$$I = \frac{C_L (V^+ - V^-)}{T_R} \qquad (1)$$

This can give a maximum limit to the load.

Figure 1 shows maximum voltage swing and capacitive load for various rise times.

1. *Transient Output Power*

The average transient power (P_{AC}) dissipated is equal to the energy needed to charge and discharge the output capacitive load (C_L) multiplied by the frequency of operation (F).

$$P_{AC} = C_L \times (V^+ - V^-)^2 \times F \qquad (2)$$

Figures 2 and 3 show transient power for two different values of $(V^+ - V^-)$ versus output load and frequency.

2. *Internal Power*

"0" State

Negligible (<3 mW)

"1" State

$$P_{INT} = \frac{(V^+ - V^-)^2}{R_2} \times \text{Duty Cycle.} \qquad (3)$$

Figure 4 gives various values of internal power versus ouptut voltage and duty cycle.

3. *Input Power*

The average input power is a function of the input current and duty cycle. Due to input voltage clamping, this power contribution is small and can therefore be neglected. At maximum duty cycle of 50%, at 25° C, the average input power is less than 10 mW per phase for $R_{IN}C_{IN}$ controlled pulse widths. For pulse widths much shorter than $R_{IN}C_{IN}$, and maximum duty cycle of 50%, input power could be as high as 30 mW, since I_{IN} peak is maintained for the full duration of the pulse width.

4. *Package Power Dissipation*

Total Average Power = Transient Output Power + Internal Power + Input Power

Typical Example *Calculation for One Half MH0013C*

How many MM506 shift registers can be driven by an MH0013C driver at 1 MHz using a clock pulse width of 400 ns, rise time 30–50 ns and 16 volts amplitude over the temperature range 0–70°C?

Power Dissipation

From the graph of power dissipation versus temperature, Figure 7, it can be seen that an MH0013C at 70°C can dissipate 1W without a heat sink; therefore, each half can dissipate 500 mW.

Transient Peak Current Limitation

From Figure 1 (equation 1), it can be seen that at 16V and 30 ns, the maximum load that can be driven is limited to 1140 pF.

Average Internal Power

Figure 4 (equation 3) gives an average power of 102 mW at 16V 40% duty cycle.

Input power will be a maximum of 8 mW.

Transient Output Power

For one half of the MH0013C

500 mW = 102 mW + 8 mW
+ transient output power

390 mW = transient output power

Using Figure 2 (equation 2) at 16V, 1 MHz and 390 mW, each half of the MH0013C can drive a 1520 pF load. This is, however, in excess of the load derived from the transient current limitation (Figure 1, equation 1), and so a maximum load of 1140 pF would prevail.

From the data sheet for the MM506, the average clock pulse load is 80 pF. Therefore the number of devices driven is $\frac{1140}{80}$ or 14 registers.

For nonsymmetrical clock widths, drive capability is improved.

Digital Drivers

DH0006/DH0006C*current driver

general description

The DH0006/DH0006C is an integrated high voltage, high current driver designed to accept standard DTL or TTL logic levels and drive a load of up to 400 mA at 28 volts. AND inputs are provided along with an Expander connection, should additional gating be required. The addition of an external capacitor provides control of the rise and fall times of the output in order to decrease cold lamp surges or to minimize electromagnetic interference if long lines are driven.

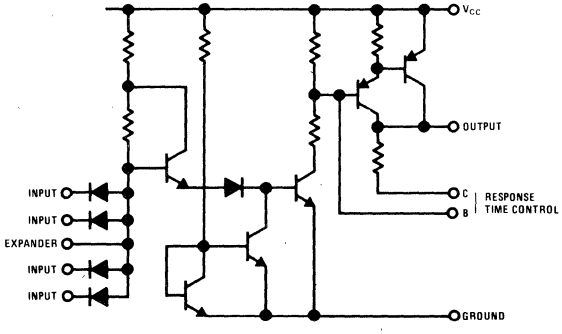
Since one side of the load is normally grounded, there is less likelihood of false turn-on due to an inadvertent short in the drive line.

*Previously called NH0006/NH0006C

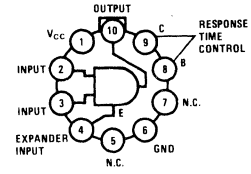
features

- Operation from a Single +10V to +45V Power Supply.
- Low Standby Power Dissipation of only 35 mW for 28V Power Supply.
- 1.5A, 50 ms, Pulse Current Capability.

schematic and connection diagrams

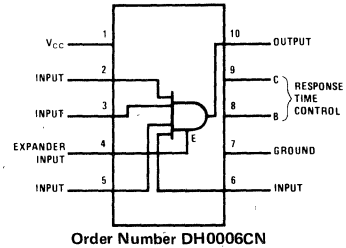


Metal Can Package



Order Number DH0006H
or DH0006CH
See Package 11

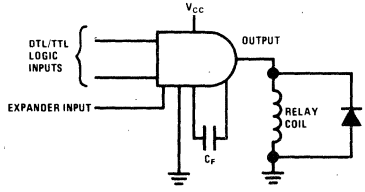
Dual-In-Line Package



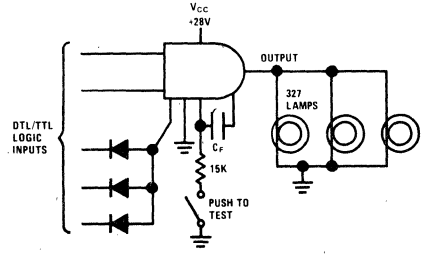
Order Number DH0006CN
See Package 16

typical applications

Relay Driver



Lamp Driver with Expanded Inputs



absolute maximum ratings

Peak Power Supply Voltage (for 0.1 sec)	60V
Continuous Supply Voltage	45V
Input Voltage	5.5V
Input Extender Current	5.0 mA
Peak Output Current (50 ms On/1 sec Off)	1.5A
Operating Temperature	
DH0006	−55°C to +125°C
DH0006C, DH0006CN	0°C to +70°C
Storage Temperature	−65°C to +150°C

electrical characteristics (Note 1)

PARAMETER	CONDITIONS	MIN	TYP (Note 2)	MAX	UNITS
Logical "1" Input Voltage	V_{CC} = 45V to 10V	2.0			V
Logical "0" Input Voltage	V_{CC} = 45V to 10V			0.8	V
Logical "1" Output Voltage	V_{CC} = 28V, V_{IN} = 2.0V, I_{OUT} = 400 mA	26.5	27.0		V
Logical "0" Output Voltage	V_{CC} = 45V, V_{IN} = 0.8V, R_L = 1K		.001	.01	V
Logical "1" Output Voltage	V_{CC} = 10V, V_{IN} = 2.0V, I_{OUT} = 150 mA	8.8	9.2		V
Logical "0" Input Current	V_{CC} = 45V, V_{IN} = .4V		−0.8	−1.0	mA
Logical "1" Input Current	V_{CC} = 45V, V_{IN} = 2.4V		0.5	5.0	μA
	V_{CC} = 45V, V_{IN} = 5.5V			100	μA
"Off" Power Supply Current	V_{CC} = 45V, V_{IN} = 0.8V		1.6	2.0	mA
"On" Power Supply Current	V_{CC} = 45V, V_{IN} = 2.0V, I_{OUT} = 0 mA			8	mA
Rise Time	V_{CC} = 28V, R_L = 82Ω		0.10		μs
Fall Time	V_{CC} = 28V, R_L = 82Ω		0.8		μs
T_{on}	V_{CC} = 28V, R_L = 82Ω		0.26		μs
T_{off}	V_{CC} = 28V, R_L = 82Ω		2.2		μs

Note 1: Unless otherwise specified, limits shown apply from −55°C to 125°C for DH0006 and 0°C to 70°C for DH0006C.

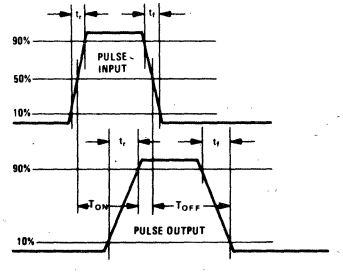
Note 2: Typical values are for 25°C ambient.

Note 3: Power ratings for the TO-5 based on a maximum junction temperature of +175°C and a ϕ_{JA} of 210°C/W.

Note 4: Power rating for the DH0006CN Molded DIP based on a maximum junction temperature of +150°C and a thermal resistance of 175°C/W when mounted in a standard DIP socket.

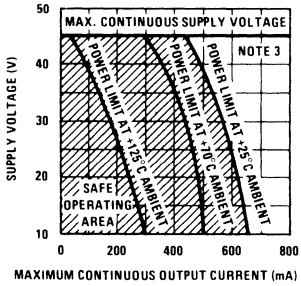
Note 5: Power rating for the DH0006CN Molded DIP based on a maximum junction temperature of +150°C and a thermal resistance of 150°C/W when mounted on a 1/16 inch thick, epoxy-glass board with ten 0.03 inch wide 2 ounce copper conductors.

switching time waveforms

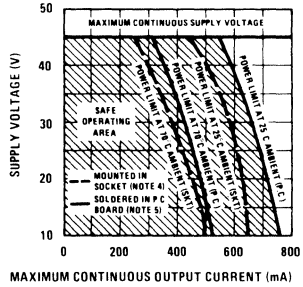


typical performance

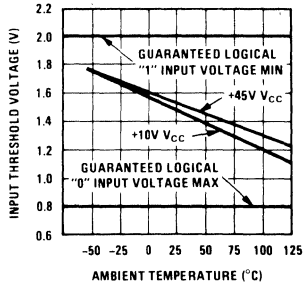
Maximum Continuous Output Current For TO-5



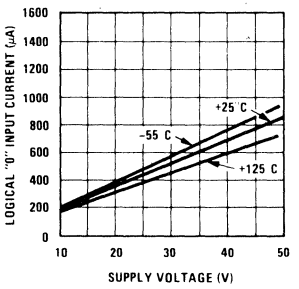
Maximum Continuous Output Current For Molded DIP



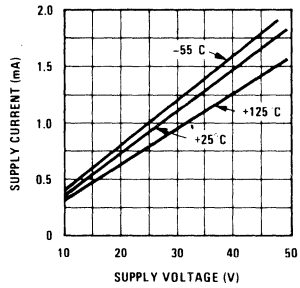
Input Threshold Voltage vs Temperature



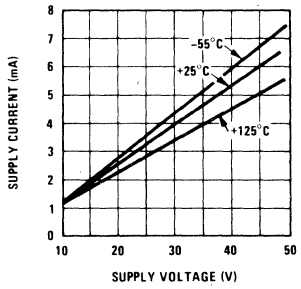
Logical "0" Input Current



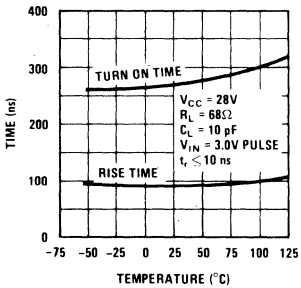
"OFF" Supply Current Drain



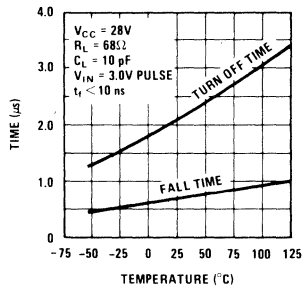
"ON" Supply Current Drain



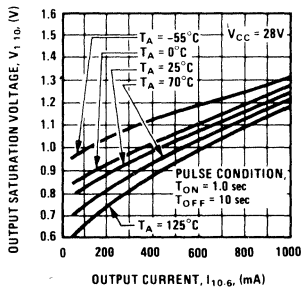
Turn On And Rise Time



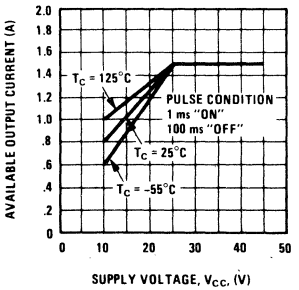
Turn Off and Fall Time



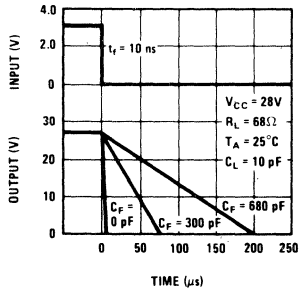
Output Saturation Voltage



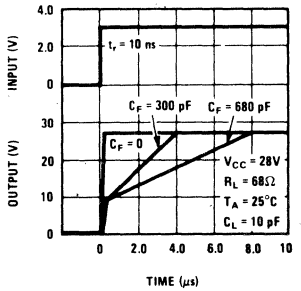
Available Output Current



Turn Off Control



Turn On Control



NATIONAL

Digital Drivers

DH0008/DH0008C*
high voltage, high current driver

general description

The DH0008/DH0008C is an integrated high voltage, high current driver, designed to accept standard DTL or TTL input levels and provide a pulsed load of up to 3A from a continuous supply voltage up to 45V. AND inputs are provided with an EXPANDER connection, should additional gating be required.

Since one side of the load is normally grounded, there is less likelihood of false turn-on due to an inadvertent short in the drive line.

The high pulse current capability makes the DH0008/DH0008C ideal for driving nonlinear resistive loads such as incandescent lamps. The

*Previously called NH0008/NH0008C

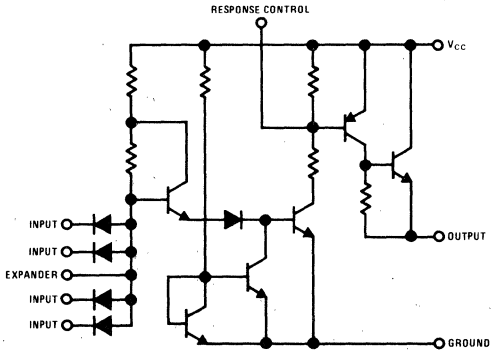
circuit also requires only one power supply for circuit functional operation.

The DH0008 is available in a 10-pin TO-5 package; the DH0008C is also available in a 10-pin TO-5, in addition to a 10-lead molded dual-in-line package.

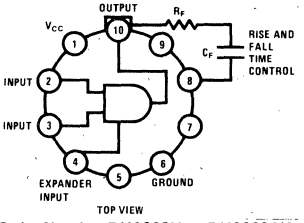
features

- Operation from a Single +10V to +45V Power Supply.
- Low Standby Power Dissipation of only 35 mW for 28V Power Supply.
- 3.0A, 50 ms, Pulse Current Capability.

schematic and connection diagrams

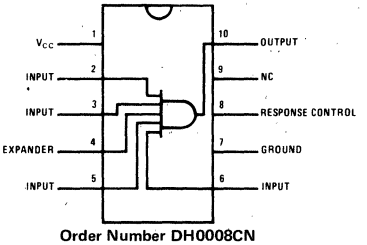


Metal Can Package



Order Number DH0008H or DH0008CH
See Package 11

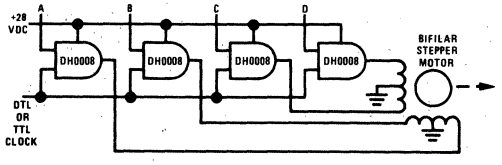
Dual-In-Line Package



Order Number DH0008CN
See Package 16

typical application

Controller for Closed Loop Stepper Motor



Switching Sequence

Step	A	B	C	D
1	1	0	1	0
2	1	0	0	1
3	0	1	0	1
4	0	1	1	0
1	1	0	1	0

To reverse the direction use a 4, 3, 2, 1 sequence

absolute maximum ratings

Peak Power Supply Voltage (for 0.1 sec)	60V
Continuous Supply Voltage	45V
Input Voltage	5.5V
Input Extender Current	5.0 mA
Peak Output Current	
(50 msec On/1 sec Off)	3.0 Amp
Continuous Output Current	
(See continuous operating curves.)	
Operating Temperature	
DH0008	−55°C to +125°C
DH0008C	0°C to +70°C
Storage Temperature	−65°C to +150°C

electrical characteristics (Note 1)

PARAMETER	CONDITIONS	MIN	TYP (Note 2)	MAX	UNITS
Logical "1" Input Voltage	V_{CC} = 45V to 10V	2.0			V
Logical "0" Input Voltage	V_{CC} = 45V to 10V			0.8	V
Logical "1" Output Voltage	V_{CC} = 45V, V_{IN} = 2.0V, I_{OUT} = 1.6A 50 ms On/1 sec Off	43	43.5		V
Logical "0" Output Voltage	V_{CC} = 45V, V_{IN} = 0.8V, R_L = 1K		0.02	0.1	V
Logical "1" Output Voltage	V_{CC} = 28V, V_{IN} = 2.0V, I_{OUT} = 0.8A 50 ms On/1 sec Off	26.5	27.1		V
Logical "0" Input Current	V_{CC} = 45V, V_{IN} = 0.4V		−0.8	−1.0	mA
Logical "1" Input Current	V_{CC} = 45V, V_{IN} = 2.4V		0.5	5.0	μA
	V_{CC} = 45V, V_{IN} = 5.5V			100	μA
"Off" Power Supply Current	V_{CC} = 45V, V_{IN} = 0V		1.6	2.0	mA
Rise Time	V_{CC} = 28V, R_L = 39Ω, V_{IN} = 5.0V		0.2		μs
Fall Time	V_{CC} = 28V, R_L = 39Ω, V_{IN} = 5.0V		3.0		μs
T_{ON}	V_{CC} = 28V, R_L = 39Ω, V_{IN} = 5.0V		0.4		μs
T_{OFF}	V_{CC} = 28V, R_L = 39Ω, V_{IN} = 5.0V		7.0		μs

Note 1: Unless otherwise specified limits shown apply from −55°C to 125°C for DH0008 and 0°C to 70°C for DH0008C.

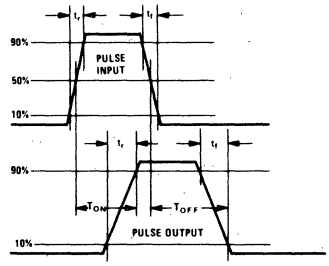
Note 2: Typical values are 25°C ambient.

Note 3: Power ratings for the TO-5 based on a maximum junction temperature of +175°C and a ϕ JA of 210°C/w.

Note 4: Power ratings for the DH0008CN Molded DIP based on a maximum junction temperature of 150°C and a thermal resistance of 150°C/w when mounted in a standard DIP socket.

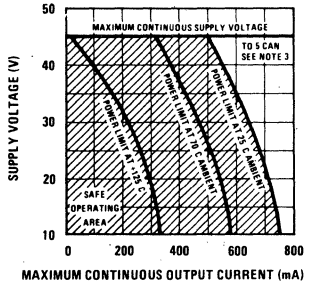
Note 5: Power ratings for the DH0008CN Molded DIP based on a maximum junction temperature of 150°C and a thermal resistance of 115°C/w when mounted on a 1/16 inch thick, epoxy-glass board with ten 0.03 inch wide 2 ounce copper conductors.

switching time waveforms

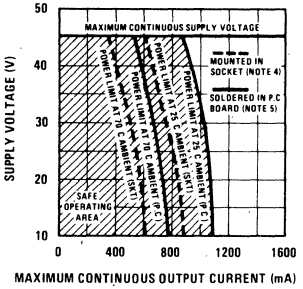


typical performance

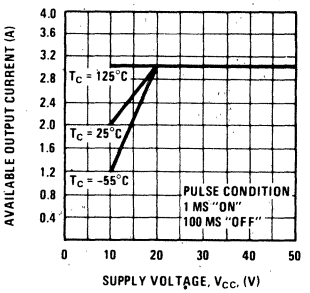
Maximum Continuous Output Current for TO-5 Package



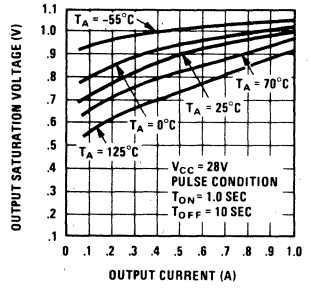
Maximum Continuous Output Current for Molded DIP



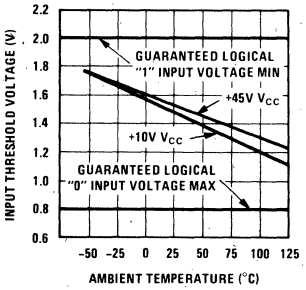
Available Output Current



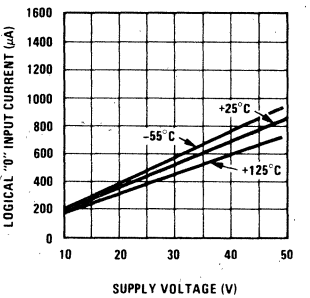
Output Saturation Voltage



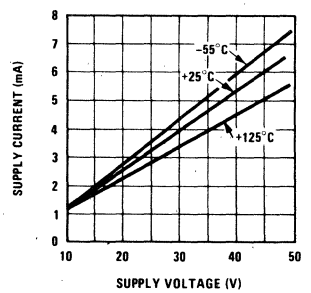
Input Threshold Voltage vs Temperature



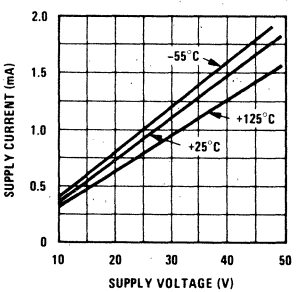
Logical "0" Input Current



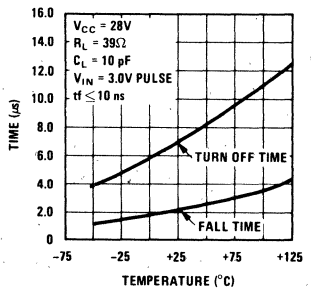
ON Supply Current Drain



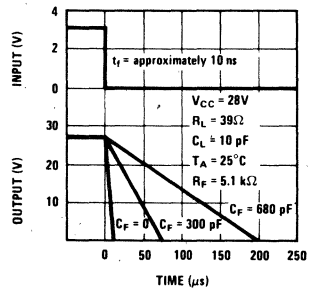
OFF Supply Current Drain



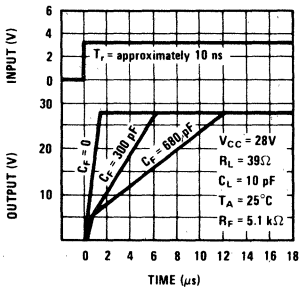
Turn OFF and Fall Times



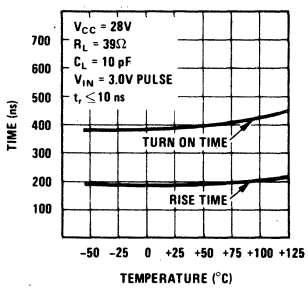
Turn ON Control



Turn OFF Control



Turn ON and Rise Time



Digital Drivers

DH0011*(SH2001)
DH0011C*(SH2002)
DH0011CN*(SH2002P)

high voltage high current drivers

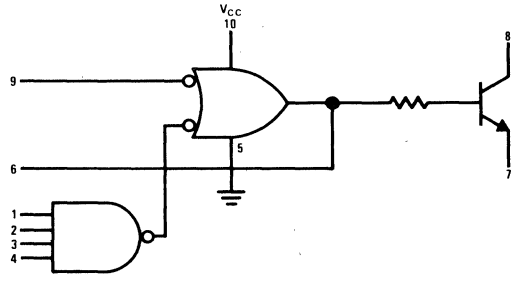
general description

The DH0011 high voltage, high current driver family consists of hybrid integrated circuits which provide a wide range of variations in temperature range, package, and output current drive capability. A summary of the variations is listed below.

Applications include driving lamps, relays, cores, and other devices requiring several hundred milliamp currents at voltages up to 40V. Logic flexibility is provided through a 4-input NAND gate, a NOR input and an input which bypasses the gating and connects the base of the output transistor.

*Previously called NH0011, NH0011C, NH0011CN

logic diagram



ordering information

NSC DESIGNATION	SH DESIGNATION	PACKAGE	TEMPERATURE RANGE	OUTPUT CURRENT CAPABILITY
DH0011H	SH2001	11	-55°C to +125°C	250 mA
DH0011CH	SH2002	11	0°C to +70°C	150 mA
DH0011CN	SH2002 P	16	0°C to +70°C	150 mA

absolute maximum ratings

V_{CC}		8V
Collector Voltage (Output)		40V
Input Reverse Current		1.0 mA
Power Dissipation		800 mW
Operating Temperature Range	DH0011	−55°C to +125°C
	DH0011C/DH0011CN	0°C to +70°C
Storage Temperature		−65°C to 150°C

electrical characteristics

TEST NO.	PIN 1	PIN 2	PIN 3	PIN 4	PIN 5	PIN 6	PIN 7	PIN 8	PIN 9	PIN 10	SENSE	MIN	MAX
1	V_{IH}	V_{IH}	V_{IH}	V_{IH}	GND		GND	I_{OL1}		V_{CCL}	V_8		V_{OL}
2	V_{IL}				GND		GND	I_{OL1}	V_{IL}	V_{CCL}	V_8		V_{OL}
3	V_{IL}				GND	I_{OL2}				V_{CCL}	V_6		V_{OL2}
4		V_{IL}			GND	I_{OL2}				V_{CCL}	V_6		V_{OL2}
5			V_{IL}		GND	I_{OL2}				V_{CCL}	V_6		V_{OL2}
6				V_{IL}	GND	I_{OL2}				V_{CCL}	V_6		V_{OL2}
7				GND	GND	I_{OL2}			V_{IH}	V_{CCL}	V_6		V_{OL2}
8	V_R	GND	GND	GND	GND					V_{CCH}	I_1		I_R
9	GND	V_R	GND	GND	GND					V_{CCH}	I_2		I_R
10	GND	GND	V_R	GND	GND					V_{CCH}	I_3		I_R
11	GND	GND	GND	V_R	GND					V_{CCH}	I_4		I_R
12					GND				V_R	V_{CCH}	I_9		I_R
13	V_F	V_R	V_R	V_R	GND					V_{CCH}	I_1		$-I_F$
14	V_R	V_F	V_R	V_R	GND					V_{CCH}	I_2		$-I_F$
15	V_R	V_R	V_F	V_R	GND					V_{CCH}	I_3		$-I_F$
16	V_R	V_R	V_R	V_F	GND					V_{CCH}	I_4		$-I_F$
17				GND	GND				V_F	V_{CCH}	I_9		$-I_F$
18					GND		GND			V_{CCL}	V_6	V_{OH}	
19	GND				GND		GND	V_{OX}		V_{CCL}	I_8		I_{OX}
20					GND		GND			V_{PD}	I_{10}		I_{PDH}
21	GND				GND					V_{MAX}	I_{10}		I_{MAX}
22*					GND					V_{PD}			t_{ON}
23*					GND					V_{PD}			t_{OFF}

*See Test Circuits and Waveforms on Page 4.

forcing functions (Note 1) DH0011

PARAMETER	−55°C	+25°C	+125°C	UNITS
V_{CCL}	4.5	4.5	4.5	V
V_{CCH}	5.5	5.5	5.5	V
V_{PD}		5.0		V
V_{MAX}		8.0		V
V_{IL}	1.4	1.1	0.8	V
V_{IH}	2.1	1.9	1.7	V
V_R	4.0	4.0	4.0	V
V_F	0.0	0.0	0.0	V
I_{OL1}	250	250	250	mA
I_{OL2}	8.0	8.0	7.5	mA
V_{OX}	40.0	40.0	40.0	V

Note 1: Temperature Range −55°C to +125°C

forcing functions (Note 2) DH0011C, DH0011CN

PARAMETER	0°C	+25°C	+70°C	UNITS
V_{CCL}	5.00	5.0	5.0	V
V_{CCH}	5.00	5.0	5.0	V
V_{PD}		5.0		V
V_{MAX}		8.0		V
V_{IL}	1.20	1.1	.95	V
V_{IH}	2.00	1.9	1.8	V
V_R	4.00	4.0	4.0	V
V_F	0.45	0.45	0.5	V
I_{OL1}	150	150	150	mA
I_{OL2}	8.0	8.0	7.5	mA
V_{OX}	40.00	40.0	40.0	V

test limits (Note 1) DH0011

PARAMETER	-55°C		+25°C		+125°C		UNITS
	MIN	MAX	MIN	MAX	MIN	MAX	
V_{OL1}		0.45		0.4		0.45	V
V_{OL2}		0.45		0.4		0.45	V
V_{OH}	2.20		2.00		1.80		V
I_R				2.0		5.0	μA
$-I_F$		1.60		1.6		1.5	mA
I_{OX}				5.0		200	μA
I_{PDH}				30.6			mA
I_{MAX}				29.6			mA
t_{ON}				160			ns
t_{OFF}				220			ns

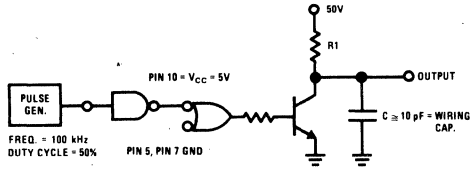
test limits (Note 2) DH0011C, DH0011CN

PARAMETER	0°C		+25°C		+70°C		UNITS
	MIN	MAX	MIN	MAX	MIN	MAX	
V_{OL1}		0.45		0.45		0.5	V
V_{OL2}		0.45		0.45		0.5	V
V_{OH}	2.05		1.95		1.85		V
I_R				5.0		10.0	μA
$-I_F$		1.40		1.4		1.35	mA
I_{OX}				5.0		200	μA
I_{PDH}				30.6			mA
I_{MAX}				34.0			mA

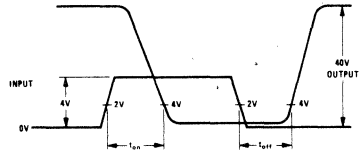
Note 1: Temperature Range −55°C to +125°C

Note 2: Temperature Range 0°C to +70°C

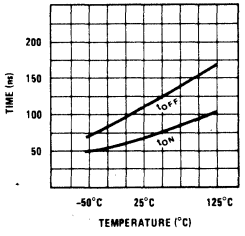
switching time test circuit



switching time waveforms



Typical Switching Times



7

NATIONAL

Digital Drivers

DH0016CN*
DH0017CN*(SH2200P)
DH0018CN*

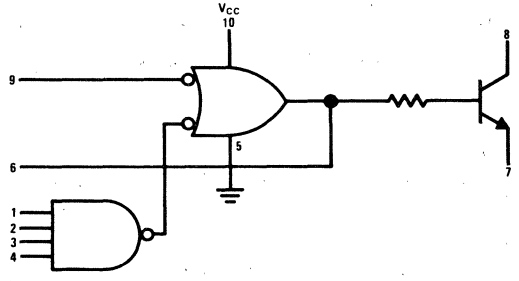
high voltage high current drivers

general description

This high-voltage, high-current driver family consists of hybrid integrated circuits which provide a wide range of output currents and output voltages. Applications include driving lamps, relays, cores, and other devices requiring up to 500 mA and withstanding voltages up to 100V. Logic flexibility is provided through a 4-input NAND gate, a NOR input and an input which bypasses the gating and connects to the base of the output transistor.

*Previously called NH0016CN, NH0017CN, NH0018CN

logic diagram



ordering information

NSC DESIGNATION	SH DESIGNATION	PACKAGE	OUTPUT CHARACTERISTICS	
			Maximum Standoff Voltage	Current
DH0016CN	N/A	16	70V	250 mA
DH0017CN	SH2200P	16	50V	500 mA
DH0018CN	N/A	16	100V	500 mA

absolute maximum ratings

V_{CC}		8V
Input Voltage		8V
Collector Voltage	DH0016CN	70V
	DH0017CN	50V
	DH0018CN	100V
Output Surge Current	DH0016CN	1.0A
	DH0017CN & DH0018CN	2.0A
Power Dissipation		455mW
Operating Temperature Range		0°C to +70°C
Storage Temperature		−65°C to +150°C

electrical characteristics

TEST NO.	PIN 1	PIN 2	PIN 3	PIN 4	PIN 5	PIN 6	PIN 7	PIN 8	PIN 9	PIN 10	SENSE	LIMITS MIN	LIMITS MAX
2	V_{IH}	V_{IH}	V_{IH}	V_{IH}	GND		GND	I_{OL1}		V_{CC}	V_8		V_{OL1}
3	V_{IL}				GND		GND	I_{OL1}	V_{IL}	V_{CC}	V_8		V_{OL1}
4		V_{IL}			GND		GND	I_{OL1}	V_{IL}	V_{CC}	V_8		V_{OL1}
5			V_{IL}		GND		GND	I_{OL1}	V_{IL}	V_{CC}	V_8		V_{OL1}
6				V_{IL}	GND		GND	I_{OL1}	V_{IL}	V_{CC}	V_8		V_{OL1}
7	V_{IL}				GND	I_{OL2}				V_{CC}	V_6		V_{OL2}
8		V_{IL}			GND	I_{OL2}				V_{CC}	V_6		V_{OL2}
9			V_{IL}		GND	I_{OL2}				V_{CC}	V_6		V_{OL2}
10				V_{IL}	GND	I_{OL2}				V_{CC}	V_6		V_{OL2}
11				GND	GND	I_{OL2}			V_{IH}	V_{CC}	V_6		V_{OL2}
12	V_R	GND	GND	GND	GND					V_{CC}	I_1		I_R
13	GND	V_R	GND	GND	GND					V_{CC}	I_2		I_R
14	GND	GND	V_R	GND	GND					V_{CC}	I_3		I_R
15	GND	GND	GND	V_R	GND					V_{CC}	I_4		I_R
16					GND				V_R	V_{CC}	I_9		I_R
17	V_F	V_R	V_R	V_R	GND					V_{CC}	I_1		$-I_F$
18	V_R	V_F	V_R	V_R	GND					V_{CC}	I_2		$-I_F$
19	V_R	V_R	V_F	V_R	GND					V_{CC}	I_3		$-I_F$
20	V_R	V_R	V_R	V_F	GND					V_{CC}	I_4		$-I_F$
21				GND	GND				V_F	V_{CC}	I_9		$-I_F$
22					GND		GND			V_{CC}	V_6	V_{OH1}	
23	GND				GND	I_{OL3}	GND	V_{OX}		V_{CC}	I_8		I_{OX}
24					GND					V_{PD}	I_{10}		I_{PD}
25	GND				GND				GND	V_{MAX}	I_{10}		I_{MAX}

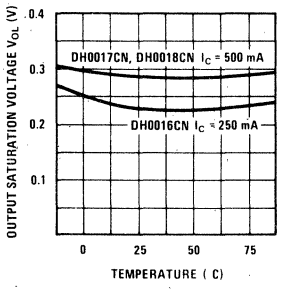
forcing functions

SYMBOL	0°C	+25°C	+70°C	UNITS
V_{CC}	5.0	5.0	5.0	V
V_{PD}		5.0		V
V_{MAX}		8.0		V
V_{IL}	0.85	0.85	0.85	V
V_{IH}	1.9	1.8	1.6	V
V_R	4.5	4.5	4.5	V
V_F	0.45	0.45	0.45	V
V_{OX} (DH0016CN)		70	70	V
V_{OX} (DH0017CN)		50	50	V
V_{OX} (DH0018CN)		100	100	V
I_{OL1} (DH0017CN, DH0018CN)	500	500	500	mA
I_{OL1} (DH0016CN)	250	250	250	mA
I_{OL2}	16	16	16	mA
I_{OL3}		8.0		mA

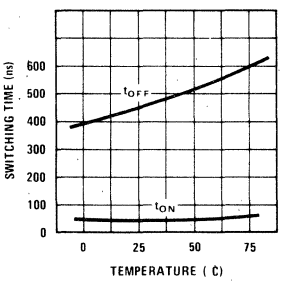
test limits

SYMBOL	0°C	+25°C	+70°C	UNITS
V_{OL1}	0.6	0.6	0.6	V
V_{OL2}	0.45	0.45	0.45	V
V_{OH1}	1.95	1.85	1.65	V
I_R		60	60	μA
$-I_F$	1.6	1.6	1.6	mA
I_{OX}		5.0	200	μA
I_{PD}		12.2		mA
I_{MAX}		10		mA

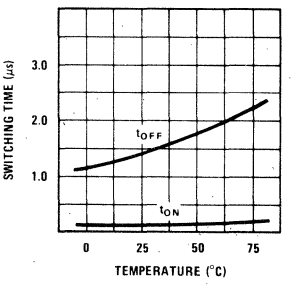
Typical Output Voltages vs Temperature



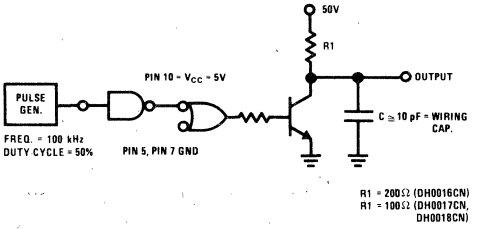
Typical Switching Times I_C = 250 mA
DH0016CN



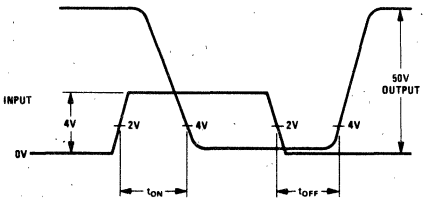
Typical Switching Times I_C = 500 mA
DH0017CN, DH0018CN



switching time test circuit



switching time waveform



Digital Drivers

DH0028C/DH0028CN* hammer driver

general description

The DH0028C/DH0028CN is a high current hammer driver designed for utilization in a wide variety of printer applications. The device is capable of driving 6 amp pulsed loads at duty cycles up to 10% (1 ms ON/10 ms OFF). The input is DTL/TTL compatible and requires only a single voltage supply in the range of 10V to 45V.

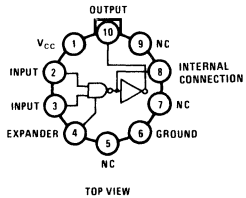
features

- Low standby power: 45 mW at V_{CC} = 36V, 35 mW at V_{CC} = 28V.
- AND input with expander affords logic flexibility.
- Fast turn-on, typically 200 ns.

*Previously called NH0028C/NH0028CN

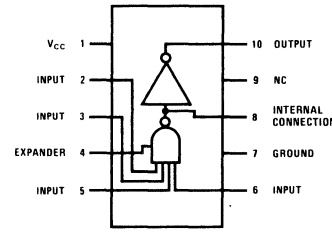
connection diagrams

Metal Can Package



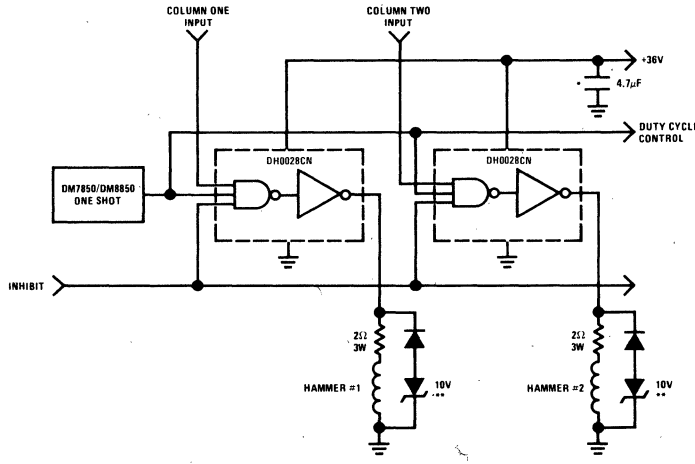
Order Number DH0028CH
See Package 11

Molded Dual-In-Line Package



Order Number DH0028CN
See Package 16

typical application



*Use one decoupling capacitor per six hammer drivers for improved AC noise immunity.
**Zener is used to control the dynamics of the hammer.

7

absolute maximum ratings

Continuous Supply Voltage	45V
Instantaneous Peak Supply Voltage (Pin 1 to Ground for 0.1 sec)	60V
Input Voltage	5.5V
Expander Input Current	5.0 mA
Peak Output Current (1 ms ON/10 ms OFF)	6.5A
Continuous Output Current DH0028C at 25°C	750 mA
DH0028CN at 25°C	1000 mA
Operating Temperature	0°C to 70°C
Storage Temperature	−65°C to +175°C
Lead Soldering Temperature (10 sec)	300°C

electrical characteristics (Note 1)

PARAMETER	CONDITIONS	MIN	TYP (Note 1)	MAX	UNITS
Logical "1" Input Voltage	V_{CC} = 10V to 45V	2.0			V
Logical "0" Input Voltage	V_{CC} = 10V to 45V			0.8	V
Logical "0" Input Current	V_{CC} = 45V, V_{IN} = 0.4V		0.8	1.0	mA
Logical "1" Input Current	V_{CC} = 45V, V_{IN} = 2.4V V_{CC} = 45V, V_{IN} = 5.5V		0.5	5.0 100.0	μA μA
Logical "1" Output Voltage	V_{CC} = 45V, V_{IN} = 2.0V, I_{OUT} = 1.6A V_{CC} = 36V, V_{IN} = 2.0V, I_{OUT} = 5A (Note 2)	43.0 33.5	43.5 34.0		V V
Logical "0" Output Voltage	V_{CC} = 45V, R_L = 1k, V_{IN} = 0.8V		.020	100	V
OFF Power Supply Current	V_{CC} = 45V, V_{IN} = 0.0V		1.6	2.0	mA
Rise Time (10% to 90%)	V_{CC} = 45V, R_L = 39Ω, V_{IN} = 5.0V peak, PRF = 1 kHz		0.2		μs
Fall Time (90% to 10%)	V_{CC} = 45V, R_L = 39Ω, V_{IN} = 5.0V peak, PRF = 1 kHz		3.0		μs
T_{ON}	V_{CC} = 45V, R_L = 39Ω, V_{IN} = 5.0V peak, PRF = 1 kHz		0.4		μs
T_{OFF}	V_{CC} = 45V, R_L = 39Ω, V_{IN} = 5.0V peak, PRF = 1 kHz		7.0		μs

Note 1: These specifications apply for ambient temperatures from 0°C to 70°C unless otherwise specified. All typical values are for 25°C ambient.

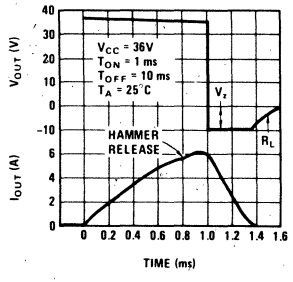
Note 2: Measurement made at 1 ms ON and 10 ms OFF.

Note 3: Power ratings for the DH0028C are based on a maximum junction temperature of 175°C and a thermal resistance of 210°C/W.

Note 4: Power ratings for the DH0028CN are based on a maximum junction temperature of 175°C and a thermal resistance of 150°C/W.

typical performance characteristics

Waveforms for Typical Drum Printer Hammer



NATIONAL

Digital Drivers

DH0034/DH0034C high speed dual level translator

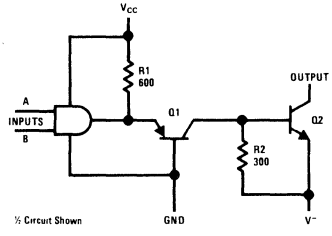
general description

The DH0034/DH0034C is a high speed level translator suitable for interfacing to MOS or junction FET analog switches. It may also be used as a universal logic level shifter capable of accepting TTL/DTL input levels and shifting to CML, MOS, or SLT levels.

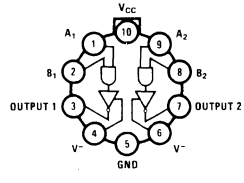
features

- Fast switching, t_{pd0}: typically 15 ns; t_{pd1}: typically 35 ns
- Large output voltage range: 25V
- Input is TTL/DTL compatible
- Low output leakage: typically 0.1 μA
- High output currents: up to ±100 mA

schematic and connection diagrams

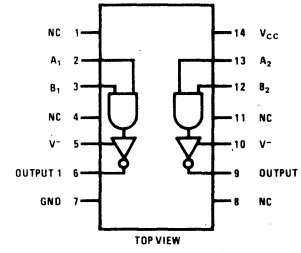


Metal Can Package



Order Number DH0034H
or DH0034CH
See Package 11

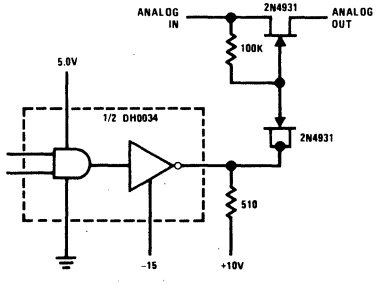
Dual-in-Line Package



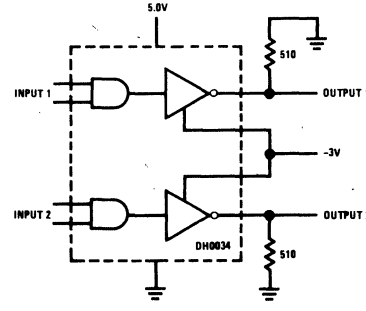
Order Number DH0034D
or DH0034CD
See Package 1

typical applications

5 MHz Analog Switch



TTL to IBM (SLT) Logic Levels



7

absolute maximum ratings

V_{CC} Supply Voltage		7.0V
Negative Supply Voltage		−30V
Positive Supply Voltage		+25V
Differential Supply Voltage		25V
Maximum Output Current		100 mA
Input Voltage		+5.5V
Operating Temperature Range:	DH0034	−55°C to +125°C
	DH0034C	0°C to +85°C
Storage Temperature Range		−65°C to +150°C
Lead Temperature (Soldering, 10 sec)		300°C

electrical characteristics (See Notes 1 & 2)

PARAMETER	CONDITIONS	DH0034			DH0034C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Logical "1" Input Voltage	V_{CC} = 4.5V V_{CC} = 4.75V	2.0			2.0			V
Logical "0" Input Voltage	V_{CC} = 5.5V V_{CC} = 4.75V			0.8			0.8	V
Logical "1" Input Current	V_{CC} = 5.5V, V_{IN} = 2.4V V_{CC} = 5.25V, V_{IN} = 2.4V			40			40	μA
Logical "1" Input Current	V_{CC} = 5.5V, V_{IN} = 5.5V V_{CC} = 5.25V, V_{IN} = 5.5V			1.0			1.0	mA
Logical "0" Input Current	V_{CC} = 5.5V, V_{IN} = 0.4V V_{CC} = 5.25V, V_{IN} = 0.4V			1.6			1.6	mA
Power Supply Current Logic "0"	(Note 3) V_{CC} = 5.5V, V_{IN} = 4.5V V_{CC} = 5.25V, V_{IN} = 4.5V		30	38		30	38	mA
Power Supply Current Logic "1"	(Note 3) V_{CC} = 5.5V, V_{IN} = 0V V_{CC} = 5.25V, V_{IN} = 0V		37	48		37	48	mA
Logical "0" Output Voltage	V_{CC} = 4.5V, I_{OUT} = 100 mA V_{CC} = 4.5V, I_{OUT} = 50 mA		V^- + .50 V^- + .3	V^- + .75 V^- + .50		V^- + .50 V^- + .3	V^- + .80 V^- + .65	V V
Output Leakage Current	V_{CC} = 5.5V, V_{IN} = 0.8V $V^+ - V^-$ = 25V		0.1	5		0.1	5	μA
Transition Time to Logical "0"	V_{CC} = 5.0V, V_3 = 0V, T_A = 25°C V^- = −25V, R_L = 510Ω		15	25		15	35	ns
Transition Time to Logical "1"	V_{CC} = 5.0V, T_A = 25°C V^- = −25V, R_L = 510Ω		35	60		35	75	ns

Note 1: These specifications apply over the temperature range −55°C to +125°C for the DH0034 and 0°C to +85°C for the DH0034C with a 510 ohm resistor connected between output and ground, and V^- connected to −25V, unless otherwise specified.

Note 2: All typical values are for T_A = 25°C.

Note 3: Current measured is total drawn from V_{CC} supply.

theory of operation

When both inputs of the DH0034 are raised to logic "1", the input AND gate is turned "on" allowing Q1's emitter to become forward biased. Q1 provides a level shift and constant output current. The collector current is essentially the same as the emitter which is given by $\frac{V_{CC} - V_{BE}}{R1}$ Approximately 7.0 mA flows out of Q1's collector.

About 2 mA of Q1's collector current is drawn off by pull down resistor, R2. The balance, 5 mA, is available as base drive to Q2 and to charge its associated Miller capacitance. The output is pulled to within a V_{SAT} of V^-. When either (or both) input to the DH0034 is lowered to logic "0," the AND gate output drops to 0.2V turning Q1 off. Deprived of base drive Q2 rapidly turns off causing the output to rise to the V_3 supply voltage. Since Q2's emitter operates between 0.6V and 0.2V, the speed of the DH0034 is greatly enhanced.

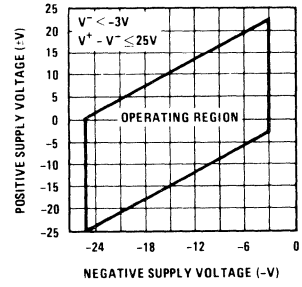
applications information

1. Paralleling the Outputs

The outputs of the DH0034 may be paralleled to increase output drive capability or to accomplish the "wire OR". In order to prevent current hogging by one output transistor or the other, resistors of 2 ohms/100 mA value should be inserted between the emitters of the output transistors and the minus supply.

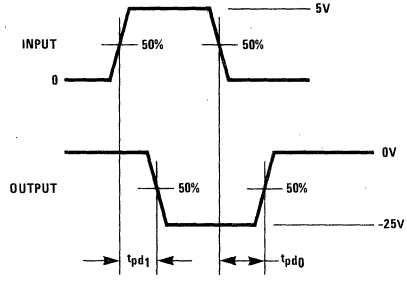
2. Recommended Output Voltage Swing

The graph shows boundary conditions which govern proper operation of the DH0034. The range of operation for the negative supply is shown on the X axis and must be between −3V and −25V. The allowable range for the positive supply is governed by the value chosen for V^-. V^+ may be selected by drawing a vertical line through the selected value for V^- and terminated by the boundaries of the operating region. For example, a value of V^- equal to −6V would dictate values of



V^+ between −5V and +19V. In general, it is desirable to maintain at least 5V difference between the supplies.

switching time waveforms



NATIONAL

Digital Drivers

DH0035/DH0035C PIN diode switch driver

general description

The DH0035/DH0035C is a high speed digital driver designed to drive PIN diodes in RF modulators and switches. The device is used in conjunction with an input buffer such as the DM7830/DM8830 or DM5440/DM7440.

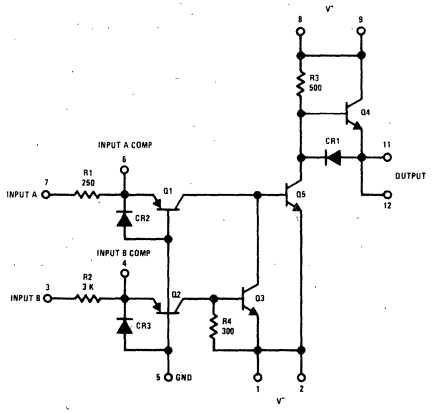
features

- Large output voltage swing – 30V
- Peak output current in excess of 1 Amp
- Inputs TTL/DTL compatible
- Short propogation delay – 10 ns
- High repetition rate – 5 MHz

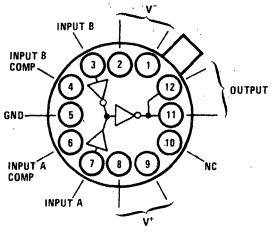
The DH0035/DH0035C is capable of driving a variety of PIN diode types including parallel, serial, anode grounded and cathode grounded. For additional information, see *AN-49 PIN Diode Drivers*.

The DH0035 is guaranteed over the temperature range −55°C to +125°C whereas the DH0035C is guaranteed from 0°C to 85°C.

schematic and connection diagrams



Metal Can Package

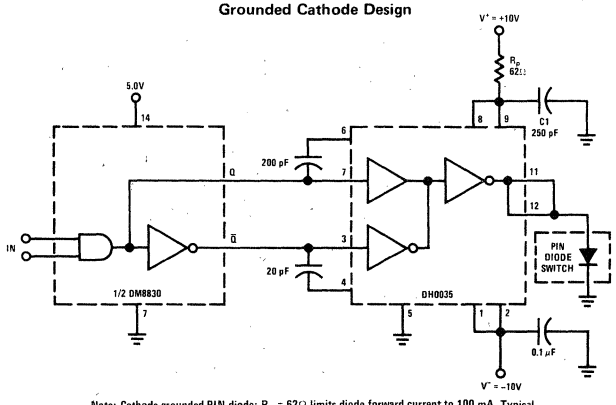


TOP VIEW

Order Number DH0035G
or DH0035CG
See Package 6

typical applications

Grounded Cathode Design



Note: Cathode grounded PIN diode: R_P = 62Ω limits diode forward current to 100 mA. Typical switching for HP33604A, RF turn-on 25 ns, turn-off 5 ns. C2 = 250 pF, R_P = 0Ω, C1 = 0.1F.

absolute maximum ratings

V^- Supply Voltage Differential (Pin 5 to Pin 1 or 2)	40V
V^+ Supply Voltage Differential (Pin 1 or 2 to Pin 8 or 9)	30V
Input Current (Pin 3 or 7)	±75 mA
Peak Output Current	±1.0 Amps
Power Dissipation (Note 3)	1.5W

Storage Temperature Range		−65°C to +150°C
Operating Temperature Range	DH0035	−55°C to +125°C
	DH0035C	0°C to +85°C
Lead Temperature (Soldering, 10 sec)		300°C

electrical characteristics (Notes 1, 2)

PARAMETER	CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Input Logic "1" Threshold	V_{OUT} = −8V, R_L = 100Ω	1.5			V
Input Logic "0" Threshold	V_{OUT} = +8V, R_L = 100Ω			0.4	V
Positive Output Swing	I_{OUT} = 100 mA	7.0	+8.0		V
Negative Output Swing	I_{OUT} = 100 mA		−8.0	−7.0	V
Positive Short Circuit Current	V_{IN} = 0V, R_L = 0Ω (Pulse Test; Duty Cycle ≤ 3%)	400	800		mA
Negative Short Circuit Current	V_{IN} = 1.5V, I_{IN} = 50 mA, R_L = 0Ω (Pulse Test, Duty Cycle ≤ 3%)	800	−1000		mA
Turn-On Delay	V_{IN} = 1.5V, V_{OUT} = −3V		10	15	ns
Turn-Off Delay	V_{IN} = 1.5V, V_{OUT} = +3V		15	30	ns
On Supply Current	V_{IN} = 1.5V		45	60	mA

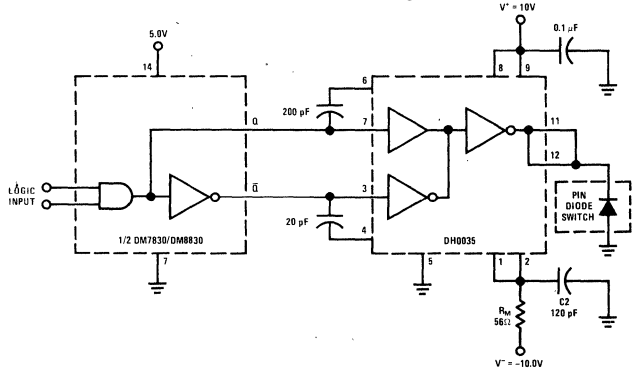
Note 1: Unless otherwise specified, these specifications apply for V^+ = 10.0V, V^- = −10.0V, pin 5 grounded, over the temperature range −55°C to +125°C for the DH0035, and 0°C to 85°C for the DH0035C.

Note 2: All typical values are for T_A = 25°C.

Note 3: Derate linearly at 10 mW/°C for ambient temperatures above 25°C.

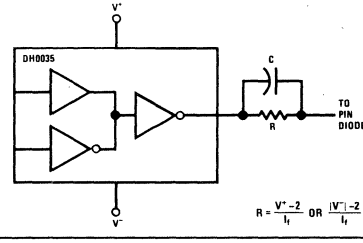
typical applications (cont.)

Grounded Anode Design



Note: Anode Grounded PIN diode: R_M = 56Ω limits diode forward current to 100 mA. Typical switching for HP33622A, RF turn-on 5 ns; turn-off 4 ns. C1 = 470 pF, C2 = 0.1 μF, R_M = 0Ω.

Alternate Current Limiting



$$R = \frac{V^+ - 2}{I_f} \text{ OR } \frac{|V^-| - 2}{I_f}$$

NATIONAL

Digital Drivers

DH3467C quad PNP core driver

general description

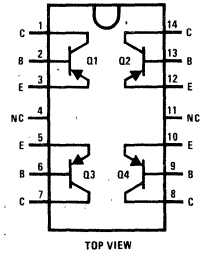
The DH3467C consists of four 2N3467 type PNP transistors mounted in a 14-pin molded dual-in-line package. The device is primarily intended for core memory application requiring operating currents in the ampere range, high stand-off voltage, and fast turn-on and turn-off times.

typical characteristics

Turn-ON Time	18 ns
Turn-OFF Time	45 ns
Collector Current	1A
Collector-Base Breakdown Voltage	120V typ.
Collector Saturation Voltage at I_C = 1A	0.55V
Collector Saturation Voltage at I_C = 0.5A	0.31V

connection diagram

Dual-In-Line Package



TOP VIEW

Order Number DH3467CN
See Package 17

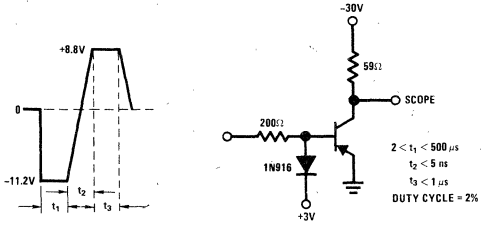


FIGURE 1. Turn-On Equivalent Test Circuit

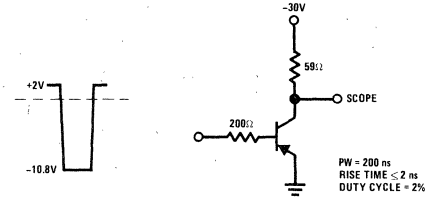


FIGURE 2. Turn-Off Equivalent Test Circuit

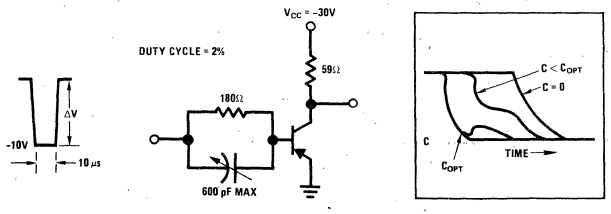


FIGURE 3. Q_T Test Circuit

absolute maximum ratings

Collector to Base Voltage	40V
Collector to Emitter Voltage	40V
Collector to Emitter Voltage (Note 1)	40V
Emitter to Base Voltage	5V
Collector Current – Continuous	1.0A
Power Dissipation (T_A = 25°C) (each device)	0.85W
Power Dissipation (T_A = 25°C) (total package)	2.5W
Operating Junction Temperature	150°C Max
Operating Temperature Range	0°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	300°C

electrical characteristics (T_A = 25°C, unless otherwise specified)

PARAMETER	CONDITIONS	LIMITS MIN	LIMITS MAX	UNITS
Collector to Base Breakdown Voltage (BV_{CBO})	I_C = 10 μA I_E = 0	−40		V
Emitter to Base Breakdown Voltage (BV_{EBO})	I_E = 10 μA I_C = 0	−5.0		V
Collector to Emitter Breakdown Voltage (Note 1) (BV_{CEO})	I_C = 10 mA I_B = 0	−40		V
DC Pulse Current Gain (Note 1) (h_{FE})	I_C = 150 mA V_{CE} = −1.0V	40		
DC Pulse Current Gain (Note 1) (h_{FE})	I_C = 500 mA V_{CE} = −1.0V	40	120	
DC Pulse Current Gain (Note 1) (h_{FE})	I_C = 1.0A V_{CE} = −5.0V	40		
Pulsed Collector Saturation Voltage (Note 1) ($V_{CE(sat)}$)	I_C = 150 mA I_B = 15 mA		−0.30	V
Pulsed Collector Saturation Voltage (Note 1) ($V_{CE(sat)}$)	I_C = 500 mA I_B = 50 mA		−0.50	V
Pulsed Collector Saturation Voltage (Note 1) ($V_{CE(sat)}$)	I_C = 1.0A I_B = 100 mA		−1.0	V
Pulsed Base Saturation Voltage (Note 1) ($V_{BE(sat)}$)	I_C = 150 mA I_B = 15 mA		−1.0	V
Pulsed Base Saturation Voltage (Note 1) ($V_{BE(sat)}$)	I_C = 500 mA I_B = 50 mA	−0.8	−1.2	V
Pulsed Base Saturation Voltage (Note 1) ($V_{BE(sat)}$)	I_C = 1.0A I_B = 100 mA		−1.6	V
Collector Cutoff Current (I_{CBO})	V_{CB} = −30V I_B = 0		100	nA
Collector Cutoff Current ($I_{CBO(100°C)}$)	V_{CB} = −30V I_B = 0		15	μA
Collector Cutoff Current (I_{CEX})	V_{CB} = −30V V_{EB} = −3.0V		100	nA
Base Cutoff Current (I_{BL})	V_{CB} = −30V V_{EB} = −3.0V		120	nA
Total Control Charge (Figure 3) (Q_T)	I_C = 500 mA I_B = 50 mA		6.0	nC
Turn On Delay Time (Figure 1) (t_d)	I_C = 500 mA I_{B1} = 50 mA		10	ns
Rise Time (Figure 1) (t_r)	I_C = 500 mA I_{B1} = 50 mA		30	ns
Storage Time (Figure 2) (t_s)	I_C = 500 mA I_{B1} = I_{B2} = 50 mA		60	ns
Fall Time (Figure 2) (t_f)	I_C = 500 mA I_{B1} = I_{B2} = 50 mA		30	ns
Output Capacitance (f = 100 kHz) (C_{ob})	I_E = 0 V_{CB} = −10V		25	pF
Input Capacitance (f = 100 kHz) (C_{ib})	I_C = 0 V_{CB} = −0.5V		100	pF
High Frequency Current Gain (f = 100 MHz) (h_{fe})	I_C = 50 mA V_{CE} = 10V	1.75		

Note 1: Pulsed test, PW = 300μs, duty cycle = 1%

NATIONAL

Digital Drivers

DH3725C quad NPN core driver

general description

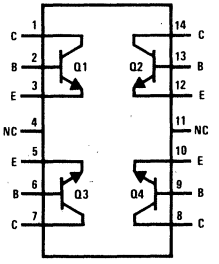
The DH3725C consists of four 2N3725 type NPN transistors mounted in a 14-pin molded dual-in-line package. The device is primarily intended for core memory application requiring operating currents in the ampere range, high stand-off voltage, and fast turn-on and turn-off times.

typical characteristics

Turn-ON Time	18 ns
Turn-OFF Time	45 ns
Collector Current	1A
Collector-Base Breakdown Voltage	120V typ.
Collector Saturation Voltage at I_C = 1A	0.55V
Collector Saturation Voltage at I_C = 0.5A	0.31V

connection diagram

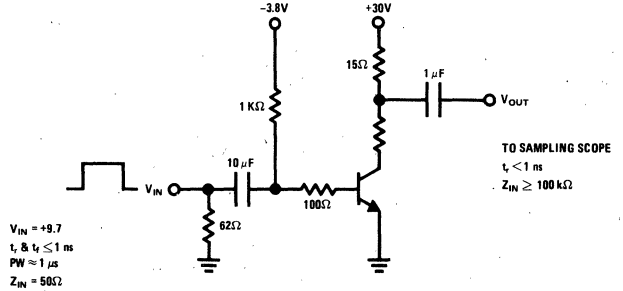
Dual-In-Line Package



TOP VIEW

Order Number DH3725CN
See Package 17

switching time test circuit



$I_C \approx 500$ mA, $I_{B1} \approx 50$ mA, $I_{B2} \approx -50$ mA

absolute maximum ratings

Collector to Base Voltage	80V
Collector to Emitter Voltage	80V
Collector to Emitter Voltage (Note 1)	50V
Emitter to Base Voltage	6V
Collector Current – Continuous	1.0A
Power Dissipation (T_A = 25°C)	0.6W
Power Dissipation (T_C = 25°C)	1.5W
Operating Junction Temperature	150°C Max
Operating Temperature Range	0°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	300°C

electrical characteristics – Each transistor (T_A = 25°C, unless otherwise specified)

PARAMETER	CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Collector to Emitter Sustaining Voltage (V_{CEO} (sust)	I_C = 10 mA, I_B = 0	50			V
Collector to Emitter Breakdown Voltage (BV_{CES})	I_C = 10 μA, V_{BE} = 0	80			V
Collector to Base Breakdown Voltage (BV_{CBO})	I_C = 10 μA, I_E = 0	80			V
Emitter to Base Breakdown Voltage (BV_{EBO})	I_C = 0, I_E = 10 μA	6.0			V
Collector Saturation Voltage ($V_{CE\ (Sat)}$) (Note 2)	I_C = 1A, I_B = 100 mA		0.55	0.95	V
	I_C = 0.5A, I_B = 50 mA		0.31	0.52	V
	I_C = 0.1A, I_B = 10 mA		0.19	0.26	V
DC Pulse Current Gain (h_{FE}) (Note 2)	I_C = 1A, V_{CE} = 5V	25	65		
	I_C = 0.5A, V_{CE} = 1V	35	45		
	I_C = 0.1A, V_{CE} = 1V	60	90	150	
Base Saturation Voltage (V_{BE} (Sat) (Note 2)	I_C = 1A, I_B = 100 mA		1.10	1.70	V
	I_C = 0.5A, I_B = 50 mA		0.95	1.20	V
	I_C = 0.1A, I_B = 10 mA		0.75	0.86	V
Collector Cutoff Current (I_{CBO})	I_E = 0, V_{CB} = 60V		0.33	1.70	μA
Turn-ON Time	I_C = 0.5A, I_{B1} = 50 mA (See test circuit)		18	30	ns
Turn-OFF Time	I_C = 0.5A, I_{B1} = 50 mA I_{B2} = 50 mA (See test circuit)		45	60	ns
High Frequency Current Gain	f = 100 MHz, I_C = 50 mA, V_{CE} = 10V	2.5	4.5		
Common Base, Open Circuit, Output Capacitance	I_E = 0, V_{CB} = 10V		4.8	10	pF
Common Base, Open Circuit, Input Capacitance	I_C = 0, V_{BE} = 0.5V		40	55	pF

Note 1: Ratings refer to a high-current point where collector-to-emitter voltage is lowest.
Note 2: Pulse conditions: Length = 300 μs, duty cycle = 1%.

NATIONAL

Digital Drivers

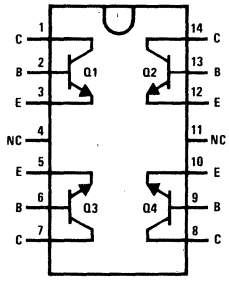
DH6376C quad NPN core driver

DESCRIPTION

The DH6376C consists of four 2N6376 type NPN transistors mounted in a 14-pin molded dual-in-line package. The device is primarily intended for core memory application requiring operating currents in the ampere range, and fast turn-on and turn-off times. Also available in ceramic dual-in-line as DH6376.

CONNECTION DIAGRAM

Dual-In-Line Package



TOP VIEW

Order Number DH6376CN
See Package 17

TYPICAL CHARACTERISTICS

Turn-On Time	12 ns
Turn-Off Time	28 ns
Collector Current	1A
Collector-Base Breakdown Voltage	110V typ.
Collector Saturation Voltage at I_C = 1A	0.48V
Collector Saturation Voltage at I_C = 0.5A	0.31V

ABSOLUTE MAXIMUM RATINGS

Collector to Base Voltage	75V
Collector to Emitter Voltage (Note)	40V
Emitter to Base Voltage	6V
Collector Current — Continuous	1.0A
Power Dissipation (T_A = 25°C) each device	0.85W
Power Dissipation (T_A = 25°C) total package	2.5W
Operating Junction Temperature	150°C Max
Operating Temperature Range	0°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Note: Ratings refer to a high-current point where collector-to-emitter voltage is lowest.

ELECTRICAL CHARACTERISTICS

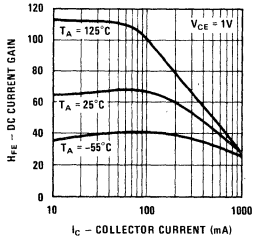
Each transistor (T_A = 25°C, unless otherwise specified)

PARAMETER	CONDITIONS	LIMITS			UNITS
		MIN	TYP	MAX	
Collector to Emitter Sustaining Voltage (V_{CEO} (sust))	I_C = 10 mA, I_B = 0	40			V
Collector to Base Breakdown Voltage (BV_{CBO})	I_C = 10 μA, I_E = 0	75			V
Emitter to Base Breakdown Voltage (BV_{EBO})	I_C = 0, I_E = 10 μA	6.0			V
Collector Saturation Voltage ($V_{CE(SAT)}$) (Note 1)	I_C = 1A, I_B = 100 mA		0.48	0.55	V
	I_C = 0.5A, I_B = 50 mA		0.31	0.4	V
	I_C = 0.1A, I_B = 10 mA		0.19	0.25	V
DC Pulse Current Gain (h_{FE}) (Note 1)	I_C = 1A, V_{CE} = 1V	20			
	I_C = 0.5A, V_{CE} = 1V	30		90	
	I_C = 0.1A, V_{CE} = 1V	60			
Base Saturation Voltage ($V_{BE(SAT)}$) (Note 1)	I_C = 1A, I_B = 100 mA		1.05	1.20	V
	I_C = 0.5A, I_B = 50 mA		0.93	1.00	V
	I_C = 0.1A, I_B = 10 mA		0.75	0.80	V
Collector Cutoff Current (I_{CBO})	I_E = 0, V_{CB} = 60V			0.5	μA
Turn-ON Time	I_C = 0.5A, I_{B1} = 50 mA (See test circuit)	10	12	20	ns
Turn-OFF Time	I_C = 0.5A, I_{B1} = 50 mA, I_{B2} = 50 mA (See test circuit)	20	28	35	ns
High Frequency Current Gain	f = 100 MHz, I_C = 50 mA, V_{CE} = 10 V	3.0			
Common Base, Open Circuit, Output Capacitance	I_E = 0, V_{CB} = 10V			9	pF
Common Base, Open Circuit, Input Capacitance	I_C = 0, V_{BE} = 0.5V			60	pF

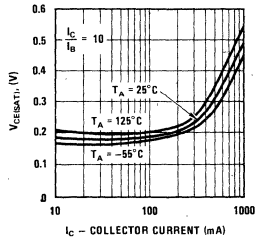
Note 1: Pulse conditions: Length = 300μs, duty cycle = 1%.

TYPICAL PERFORMANCE CURVES (each transistor)

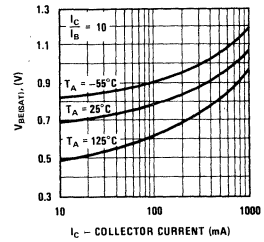
DC Current Gain vs Collector Current



$V_{CE(SAT)}$, Collector Saturation Voltage

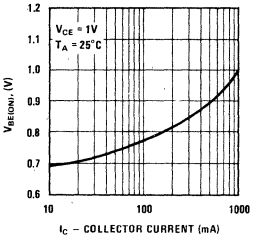


$V_{BE(SAT)}$, Base Saturation Voltage

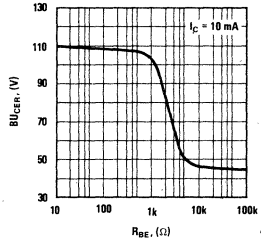


TYPICAL PERFORMANCE CURVES (Con't) (each transistor)

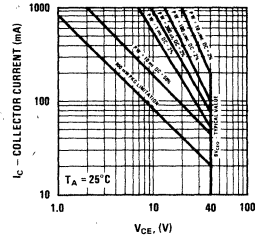
$V_{BE(ON)}$, Base Emitter On Voltage



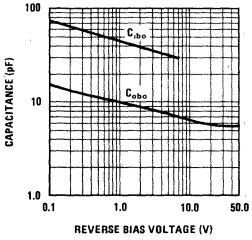
BV_{CER} vs R_{BE}



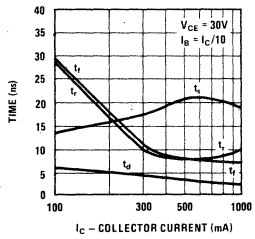
Safe Operating Area



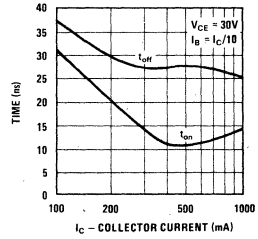
Capacitance vs Reverse Bias Voltage



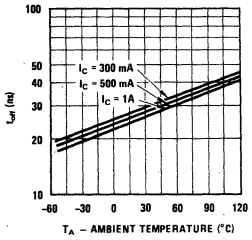
Switching Times vs Collector Current



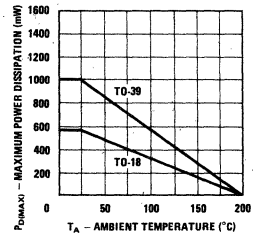
Turn On and Turn Off Times vs Collector Current



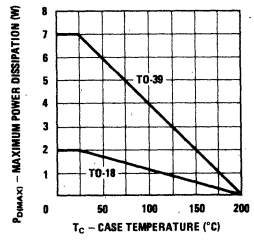
t_{off} vs Ambient Temperature



Maximum Power Dissipation vs Ambient Temperature



Maximum Power Dissipation vs Case Temperature



NATIONAL

D/A-A/D Products

LH0070 series precision BCD buffered reference
LH0071 series precision binary buffered reference

general description

The LH0070 and LH0071 are precision, three terminal, voltage references consisting of a temperature compensated zener diode driven by a current regulator and a buffer amplifier. The devices provide an accurate reference that is virtually independent of input voltage, load current, temperature and time. The LH0070 has a 10.000V nominal output to provide equal step sizes in BCD applications. The LH0071 has a 10.240V nominal output to provide equal step sizes in binary applications.

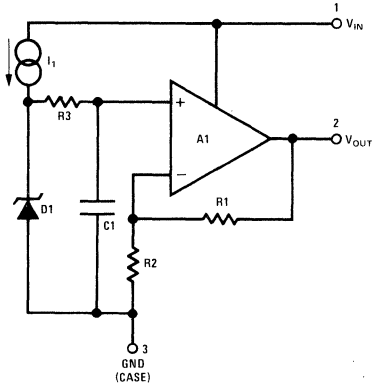
The output voltage is established by trimming ultra-stable, low temperature drift, thin film resistors under actual operating circuit conditions. The devices are short-circuit proof in both the current sourcing and sinking directions.

The LH0070 and LH0071 series combine excellent long term stability, ease of application, and low cost, making them ideal choices as reference voltages in precision D to A and A to D systems.

features

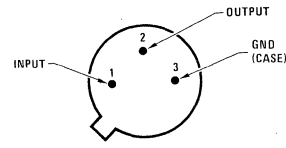
- Accurate output voltage
  - LH0070 — 10V ±0.02%
  - LH0071 — 10.24V ±0.02%
- Single supply operation — 12.5V to 40V
- Low output impedance — 0.1Ω
- Excellent line regulation — 0.1 mV/V
- Low zener noise — 100μVp-p
- 3-lead TO-5 (pin compatible with the LM109)
- Short circuit proof
- Low standby current — 3 mA

equivalent schematic



connection diagram

TO-5 Metal Can Package



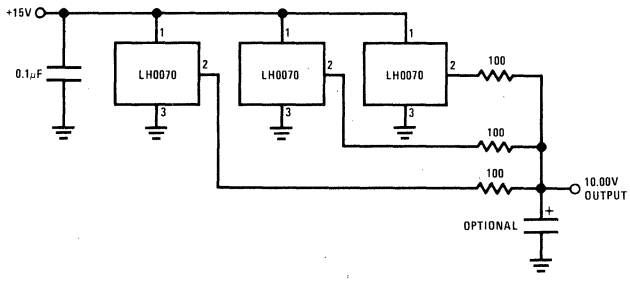
BOTTOM VIEW

See Package 19

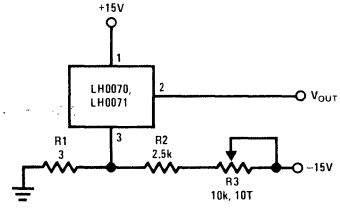
Order Numbers:

LH0070 – 1H LH0071 – 1H
LH0070 – 2H LH0071 – 2H

typical applications



Statistical Voltage Standard



*Note: The output of the LH0070 and LH0071 may be adjusted to a precise voltage by using the above circuit since the supply current of the devices is relatively small and constant with temperature and input voltage. For the circuit shown, supply sensitivities are degraded slightly to 0.01%/V change in V_{OUT} for changes in V_{IN} and V^-.

An additional temperature drift of 0.0001%/°C is added due to the variation of supply current with temperature of the LH0070 and LH0071. Sensitivity to the value of R1, R2 and R3 is less than 0.001%/%.

*Output Voltage Fine Adjustment

8

absolute maximum ratings

Supply Voltage	40V
Power Dissipation (See Curve)	600 mW
Short Circuit Duration	Continuous
Output Current	±20 mA
Operating Temperature Range	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

electrical characteristics (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage	$T_A = 25°C$				
LH0070			10.000		V
LH0071			10.240		V
Output Accuracy	$T_A = 25°C$				
−1			±0.03	±0.1	%
−2			±0.02	±0.05	%
Output Accuracy					
−1				±0.3	%
−2				±0.2	%
Output Voltage Change With Temperature	(Note 2)				
−1			±0.02	±0.1	%
−2			±0.01	±0.04	%
Line Regulation	$13V \leq V_{IN} \leq 33V$, $T_C = 25°C$				
−1			0.02	0.1	%
−2			0.01	0.03	%
Input Voltage Range		12.5		40	V
Load Regulation	$0\ mA \leq I_{OUT} \leq 5\ mA$		0.01	0.03	%
Quiescent Current	$13V \leq V_{IN} \leq 33V$, $I_{OUT} = 0\ mA$	2	3	5	mA
Change In Quiescent Current	$\Delta V_{IN} = 20V$ From 13V To 33V		0.75	1.5	mA
Output Noise Voltage	BW = 0.1 Hz to 10 Hz, $T_A = 25°C$		100		μVp-p
Ripple Rejection	f = 120 Hz		0.01		%/Vp-p
Output Resistance			0.2	1	Ω
Long Term Stability	$T_A = 25°C$ (Note 3)				
−1				±0.2	%/yr.
−2				±0.05	%/yr.

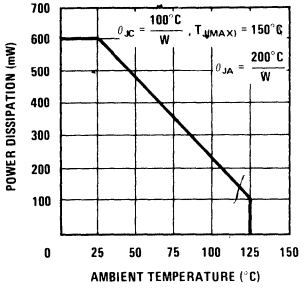
Note 1: Unless otherwise specified, these specifications apply for $V_{IN} = 15.0V$, $R_L = 10\ k\Omega$, and over the temperature range of $-55°C \leq T_A \leq +125°C$.

Note 2: This specification is the difference in output voltage measured at $T_A = +85°C$ and at $T_A = -25°C$ with readings taken after oven and device-under-test stabilization at temperature using a suitable precision voltmeter.

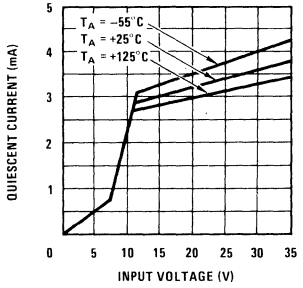
Note 3: This parameter is guaranteed by design and not tested.

typical performance characteristics

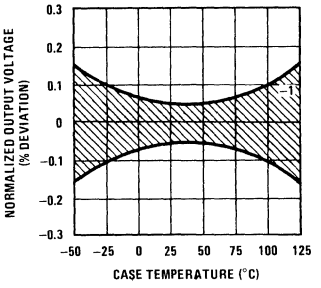
Maximum Power Dissipation



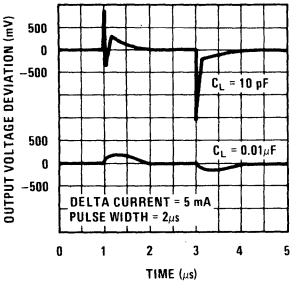
Quiescent Current vs Input Voltage



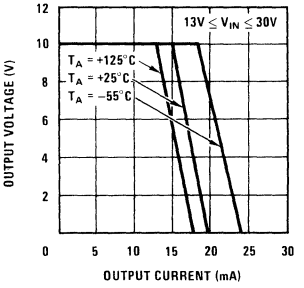
Normalized Output Voltage vs Temperature



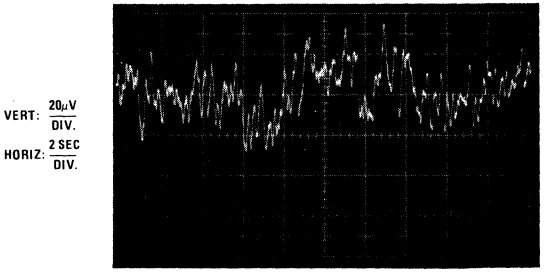
Step Load Response



Output Short Circuit Characteristics

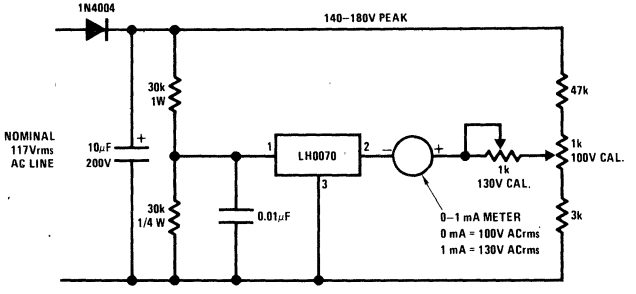


Noise Voltage



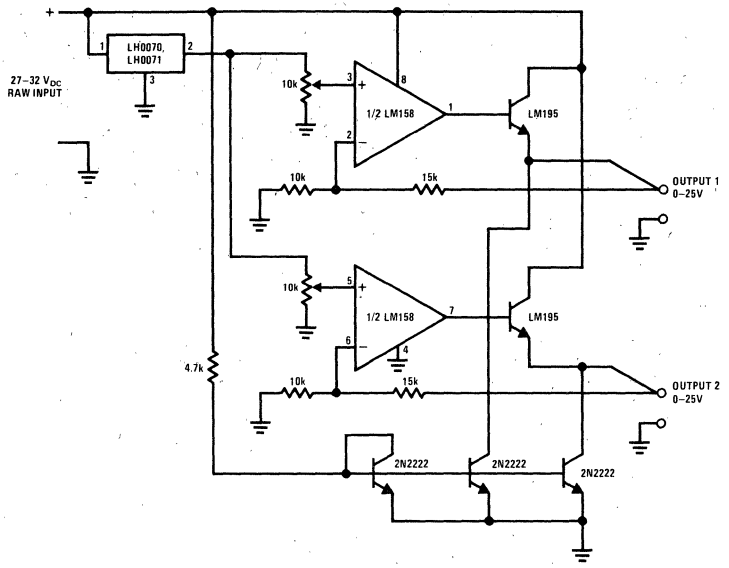
BW = 0.1 Hz TO 10 Hz

typical applications (con't)

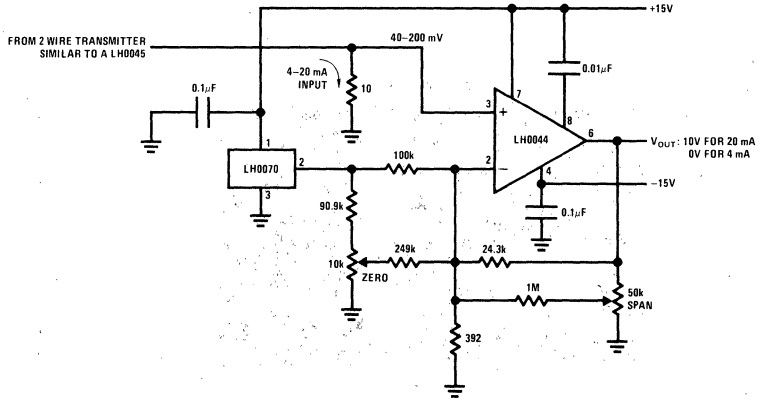


Expanded Scale ac Voltmeter

typical applications (con't)



Dual Output Bench Power Supply



Precision Process Control Interface

NATIONAL

LM199/LM299/LM399 precision reference

general description

The LM199/LM299/LM399 are precision, temperature-stabilized monolithic zeners offering temperature coefficients a factor of ten better than high quality reference zeners. Constructed on a single monolithic chip is a temperature stabilizer circuit and an active reference zener. The active circuitry reduces the dynamic impedance of the zener to about 0.5Ω and allows the zener to operate over 0.5 mA to 10 mA current range with essentially no change in voltage or temperature coefficient. Further, a new subsurface zener structure gives low noise and excellent long term stability compared to ordinary monolithic zeners. The package is supplied with a thermal shield to minimize heater power and improve temperature regulation.

The LM199 series references are exceptionally easy to use and free of the problems that are often experienced with ordinary zeners. There is virtually no hysteresis in reference voltage with temperature cycling. Also, the LM199 is free of voltage shifts due to stress on the leads. Finally, since the unit is temperature stabilized, warm up time is fast.

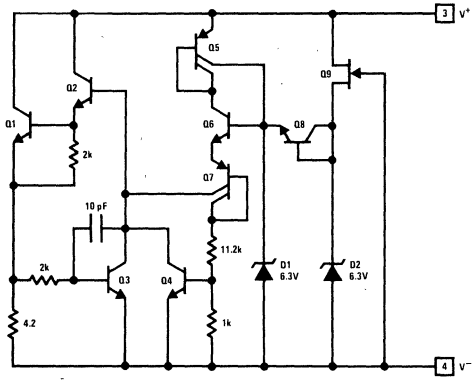
The LM199 can be used in almost any application in place of ordinary zeners with improved performance. Some ideal applications are analog to digital converters, calibration standards, precision voltage or current sources or precision power supplies. Further in many cases the LM199 can replace references in existing equipment with a minimum of wiring changes.

The LM199 series devices are packaged in a standard hermetic TO-46 package inside a thermal shield. The LM199 is rated for operation from −55°C to +125°C while the LM299 is rated for operation from −25°C to +85°C and the LM399 is rated from 0°C to +70°C.

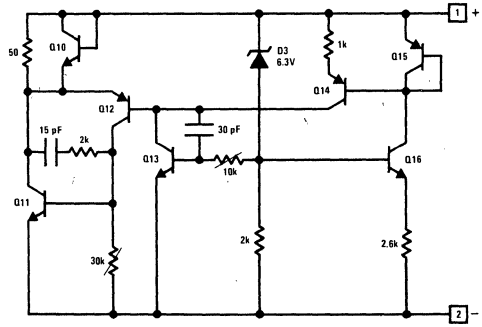
features

- Guaranteed 0.0001%/°C temperature coefficient
- Low dynamic impedance — 0.5Ω
- Initial tolerance on breakdown voltage — 2%
- Sharp breakdown at 400μA
- Wide operating current — 500μA to 10 mA
- Wide supply range for temperature stabilizer
- Guaranteed low noise
- Low power for stabilization — 300 mW at 25°C
- Long term stability — 20 ppm

schematic diagrams



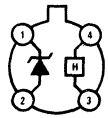
Temperature Stabilizer



Reference

connection diagram

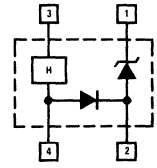
Metal Can Package



TOP VIEW

Order Number
LM199H
LM299H
LM399H
See Package 25

functional block diagram



8

absolute maximum ratings

Temperature Stabilizer Voltage	40V
Reverse Breakdown Current	20 mA
Forward Current	1 mA
Reference to Substrate Voltage $V_{(RS)}$ (Note 1)	+40V −0.1V
Operating Temperature Range	
LM199	−55°C to +125°C
LM299	−25°C to +85°C
LM399	0°C to +70°C
Storage Temperature Range	−55°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

electrical characteristics (Note 2)

PARAMETER	CONDITIONS		LM199/LM299			LM399			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Reverse Breakdown Voltage	$0.5\ mA \leq I_R \leq 10\ mA$		6.8	6.95	7.1	6.6	6.95	7.3	V
Reverse Breakdown Voltage Change With Current	$0.5\ mA \leq I \leq 10\ mA$			6	9		6	12	mV
Reverse Dynamic Impedance	$I_R = 1\ mA$			0.5	1		0.5	1.5	Ω
Reverse Breakdown Temperature Coefficient	$-55°C \leq T_A \leq 85°C$	LM199		0.00003	0.0001				%/°C
	$85°C \leq T_A \leq 125°C$	LM199		0.0005	0.0015				%/°C
	$-25°C \leq T_A \leq 85°C$	LM299		0.00003	0.0001				%/°C
	$0°C \leq T_A \leq 70°C$	LM399					0.00003	0.0002	%/°C
RMS Noise	$10\ Hz \leq f \leq 10\ kHz$			7	20		7	50	μV
Long Term Stability	Stabilized, $22°C \leq T_A \leq 28°C$, 1000 Hours, $I_R = 1\ mA \pm 0.1\%$			20			20		ppm
Temperature Stabilizer Supply Current	$T_A = 25°C$, Still Air, $V_S = 30V$			8.5	14		8.5	15	mA
	$T_A = -55°C$			22	28				
Temperature Stabilizer Supply Voltage (Note 3)			9		40	9		40	V
Warm-Up Time to 0.05%	$V_S = 30V$, $T_A = 25°C$			3			3		Seconds
Initial Turn-on Current	$9 \leq V_S \leq 40$, $T_A = 25°C$			140	200		140	200	mA

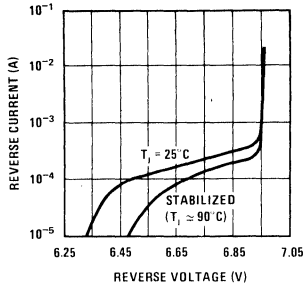
Note 1: The substrate is electrically connected to the negative terminal of the temperature stabilizer. The voltage that can be applied to either terminal of the reference is 40V more positive or 0.1V more negative than the substrate.

Note 2: These specifications apply for 30V applied to the temperature stabilizer and $-55°C \leq T_A \leq +125°C$ for the LM199; $-25°C \leq T_A \leq +85°C$ for the LM299 and $0°C \leq T_A \leq +70°C$ for the LM399.

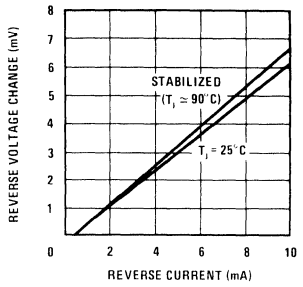
Note 3: CAUTION. If the device is operated for more than 60 seconds with heater supply voltage between 2V and 9V the heater temperature control circuitry is not properly biased and the device can rise to approximately +150°C.

typical performance characteristics

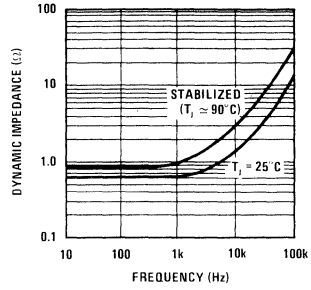
Reverse Characteristics



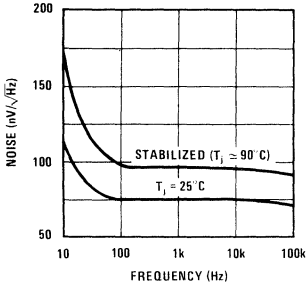
Reverse Voltage Change



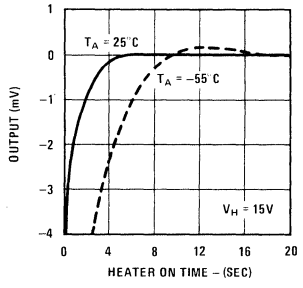
Dynamic Impedance



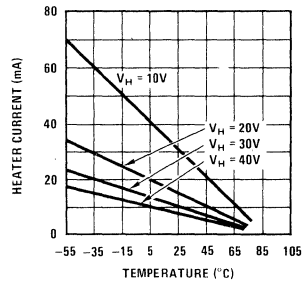
Zener Noise Voltage



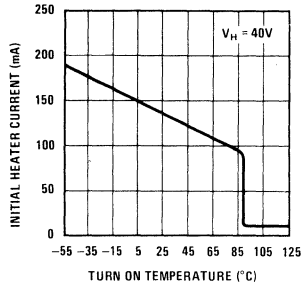
Stabilization Time



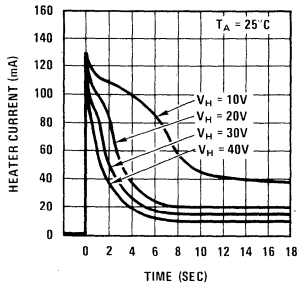
Heater Current



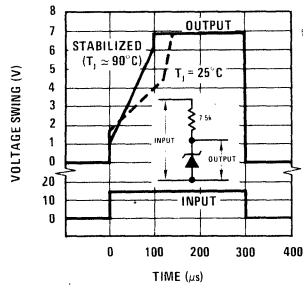
Initial Heater Current



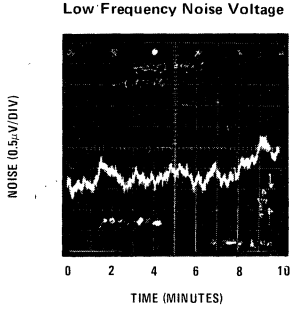
Heater Current



Response Time



Low Frequency Noise Voltage

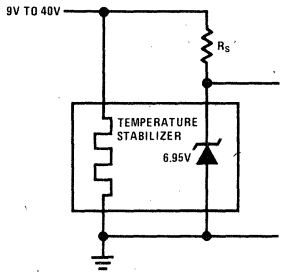


0.01 Hz ≤ f ≤ 1 Hz
STABILIZED
($T_j \sim 90°C$)

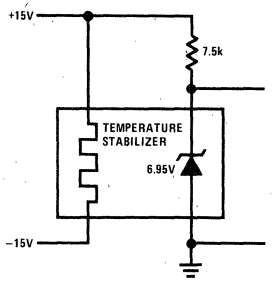
8

typical applications

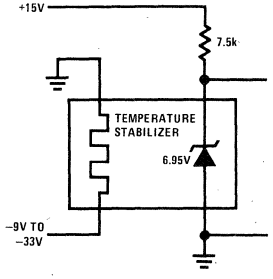
Single Supply Operation



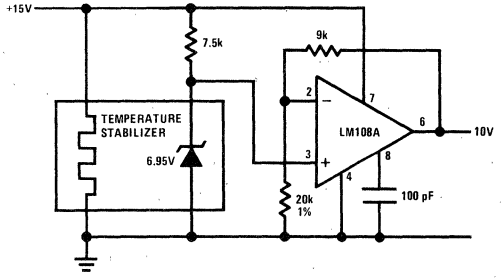
Split Supply Operation



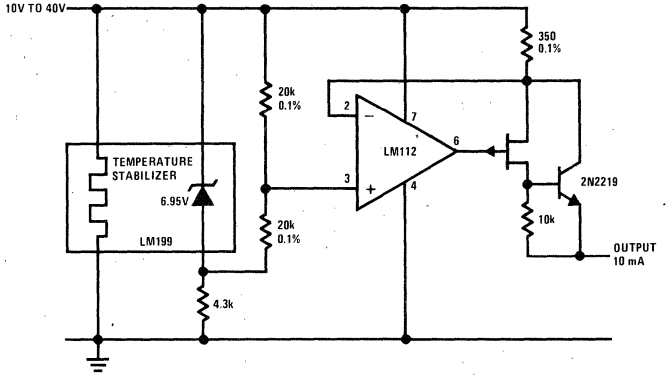
Negative Heater Supply with Positive Reference



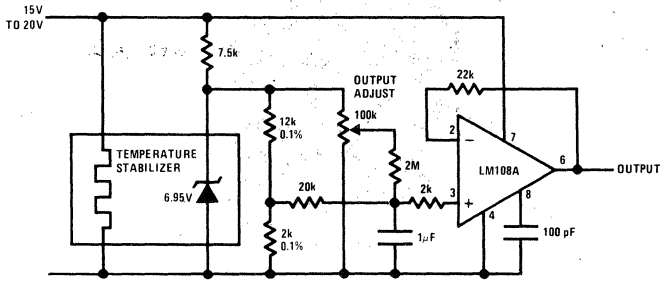
Buffered Reference With Single Supply



Positive Current Source

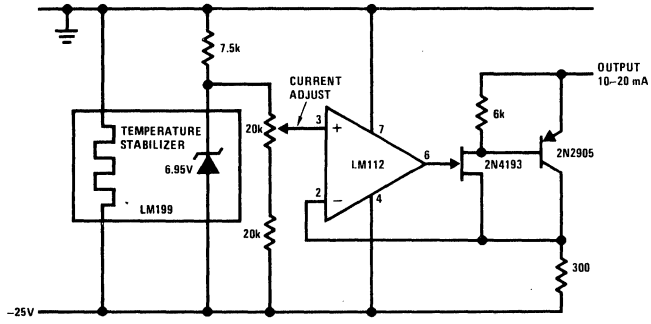


Standard Cell Replacement

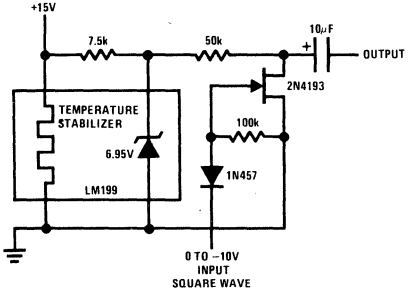


typical applications (con't)

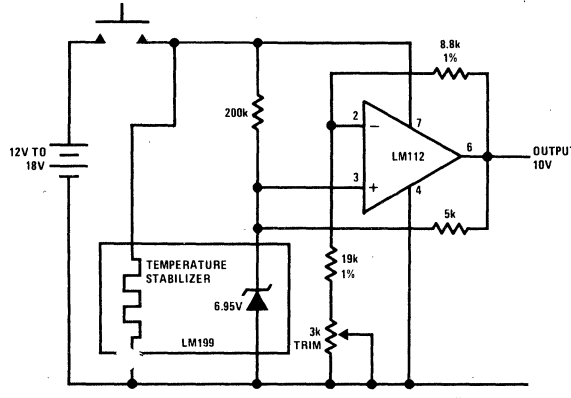
Negative Current Source



Square Wave Voltage Reference

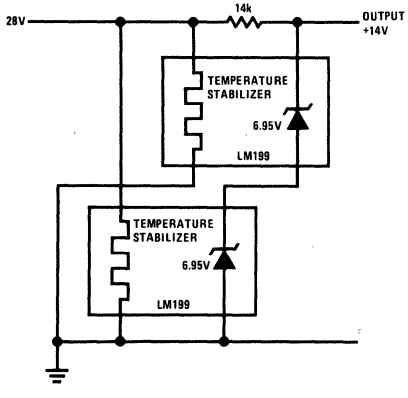


Portable Calibrator*

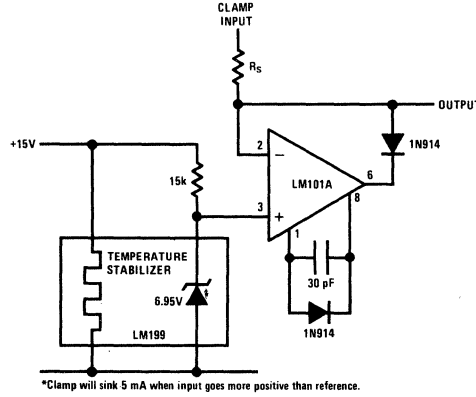


*Warm-up time 10 seconds; intermittant operation does not degrade long term stability.

14V Reference



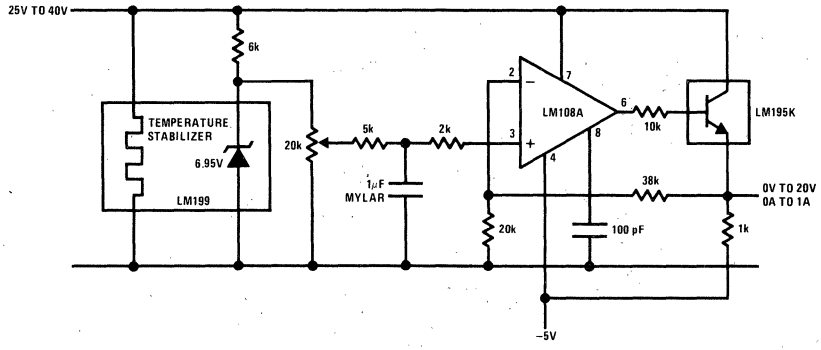
Precision Clamp*



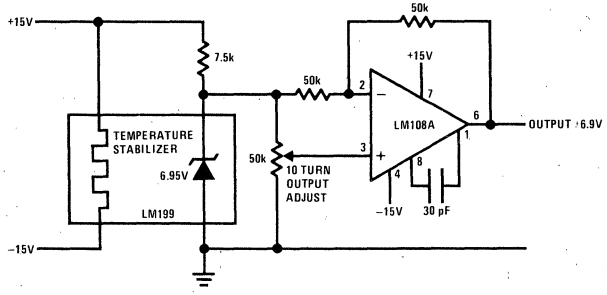
*Clamp will sink 5 mA when input goes more positive than reference.

typical applications (con't)

0V to 20V Power Reference



Bipolar Output Reference



NATIONAL

LM199A/LM299A/LM399A precision reference

general description

The LM199A/LM299A/LM399A are precision, temperature-stabilized monolithic zeners offering temperature coefficients a factor of ten better than high quality reference zeners. Constructed on a single monolithic chip is a temperature stabilizer circuit and an active reference zener. The active circuitry reduces the dynamic impedance of the zener to about 0.5Ω and allows the zener to operate over 0.5 mA to 10 mA current range with essentially no change in voltage or temperature coefficient. Further, a new subsurface zener structure gives low noise and excellent long term stability compared to ordinary monolithic zeners. The package is supplied with a thermal shield to minimize heater power and improve temperature regulation.

The LM199A series references are exceptionally easy to use and free of the problems that are often experienced with ordinary zeners. There is virtually no hysteresis in reference voltage with temperature cycling. Also, the LM199A is free of voltage shifts due to stress on the leads. Finally, since the unit is temperature stabilized, warm up time is fast.

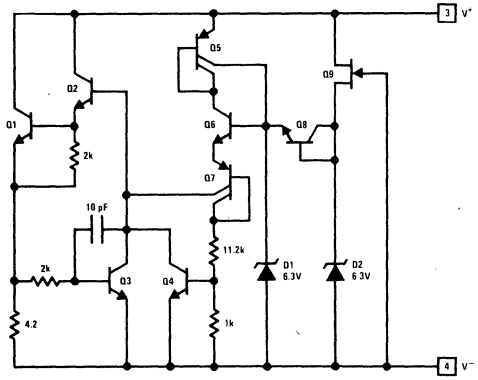
The LM199A can be used in almost any application in place of ordinary zeners with improved performance. Some ideal applications are analog to digital converters, calibration standards, precision voltage or current sources or precision power supplies. Further in many cases the LM199A can replace references in existing equipment with a minimum of wiring changes.

The LM199A series devices are packaged in a standard hermetic TO-46 package inside a thermal shield. The LM199 is rated for operation from −55°C to +125°C while the LM299A is rated for operation from −25°C to +85°C and the LM399A is rated from 0°C to +70°C.

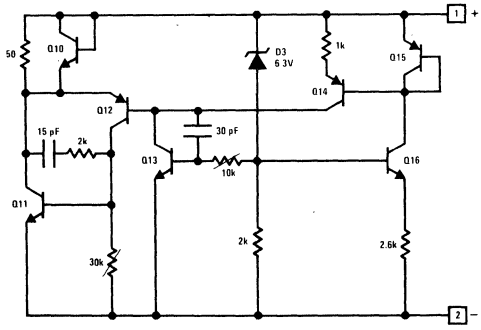
features

- Guaranteed 0.00005%/°C temperature coefficient
- Low dynamic impedance — 0.5Ω
- Initial tolerance on breakdown voltage — 2%
- Sharp breakdown at 400μA
- Wide operating current — 500μA to 10 mA
- Wide supply range for temperature stabilizer
- Guaranteed low noise
- Low power for stabilization — 300 mW at 25°C
- Long term stability — 20 ppm

schematic diagrams



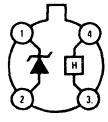
Temperature Stabilizer



Reference

connection diagram

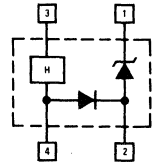
Metal Can Package



TOP VIEW

Order Number
LM199AH
LM299AH
LM399AH
See Package 25

functional block diagram



8

absolute maximum ratings

Temperature Stabilizer Voltage	40V
Reverse Breakdown Current	20 mA
Forward Current	1 mA
Reference to Substrate Voltage $V_{(RS)}$ (Note 1)	+40V
	−0.1V
Operating Temperature Range	
LM199A	−55°C to +125°C
LM299A	−25°C to +85°C
LM399A	0°C to +70°C
Storage Temperature Range	−55°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

electrical characteristics (Note 2)

PARAMETER	CONDITIONS		LM199A, LM299A			LM399A			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Reverse Breakdown Voltage	$0.5\ mA \leq I_R \leq 10\ mA$		6.8	6.95	7.1	6.6	6.95	7.3	V
Reverse Breakdown Voltage Change With Current	$0.5\ mA \leq I_R \leq 10\ mA$			6	9		6	12	mV
Reverse Dynamic Impedance	$I_R = 1\ mA$			0.5	1		0.5	1.5	Ω
Reverse Breakdown Temperature Coefficient	$-55°C \leq T_A \leq 85°C$	LM199A		0.00002	0.00005				%/°C
	$85°C \leq T_A \leq 125°C$	LM199A		0.0005	0.0010				%/°C
	$-25°C \leq T_A \leq 85°C$	LM299A		0.00002	0.00005				%/°C
	$0°C \leq T_A \leq 70°C$	LM399A					0.00003	0.0001	%/°C
RMS Noise	$10\ Hz \leq f \leq 10\ kHz$			7	20		7	50	μV
Long Term Stability	Stabilized, $22°C \leq T_A \leq 28°C$, 1000 Hours, $I_R = 1\ mA \pm 0.1\%$			20			20		ppm
Temperature Stabilizer Supply Current	$T_A = 25°C$, Still Air, $V_S = 30V$			8.5	14		8.5	15	mA
	$T_A = -55°C$			22	28				
Temperature Stabilizer Supply Voltage (Note 3)			9		40	9		40	V
Warm-Up Time to 0.05%	$V_S = 30V$, $T_A = 25°C$			3			3		Seconds
Initial Turn-on Current	$9 \leq V_S \leq 40$, $T_A = 25°C$			140	200		140	200	mA

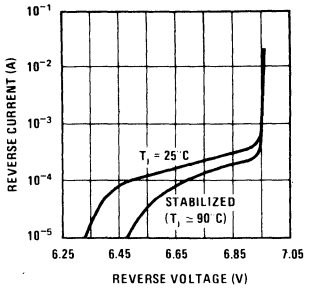
Note 1: The substrate is electrically connected to the negative terminal of the temperature stabilizer. The voltage that can be applied to either terminal of the reference is 40V more positive or 0.1V more negative than the substrate.

Note 2: These specifications apply for 30V applied to the temperature stabilizer and $-55°C \leq T_A \leq +125°C$ for the LM199A; $-25°C \leq T_A \leq +85°C$ for the LM299A and $0°C \leq T_A \leq +70°C$ for the LM399A.

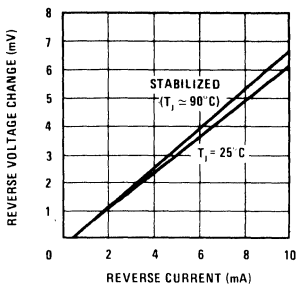
Note 3: CAUTION. If the device is operated for more than 60 seconds with heater supply voltage between 2V and 9V the heater temperature control circuitry is not properly biased and the device can rise to approximately +150°C.

typical performance characteristics

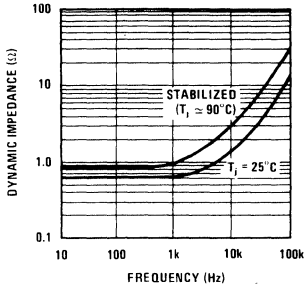
Reverse Characteristics



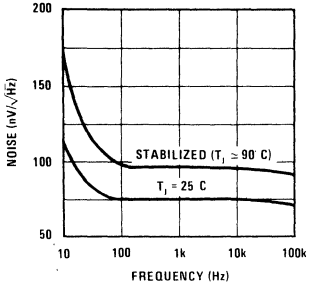
Reverse Voltage Change



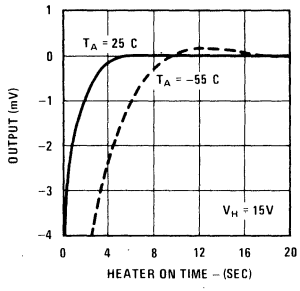
Dynamic Impedance



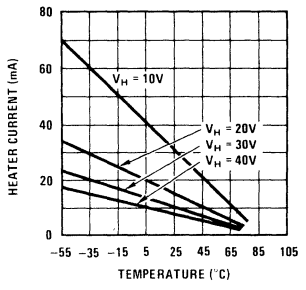
Zener Noise Voltage



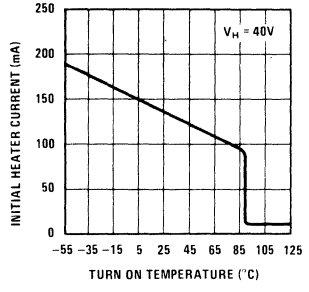
Stabilization Time



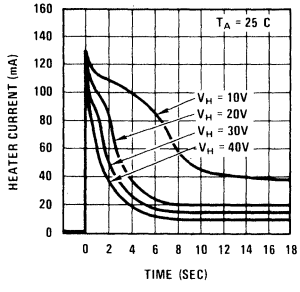
Heater Current



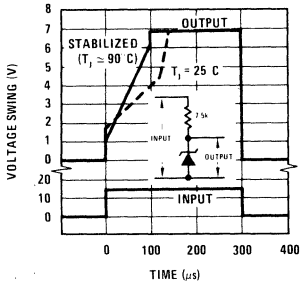
Initial Heater Current



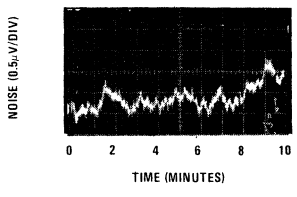
Heater Current



Response Time



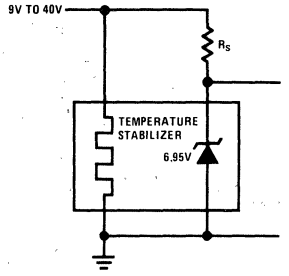
Low Frequency Noise Voltage



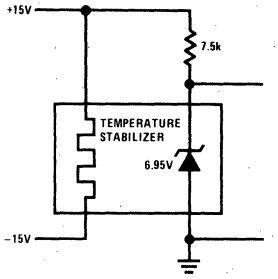
8

typical applications

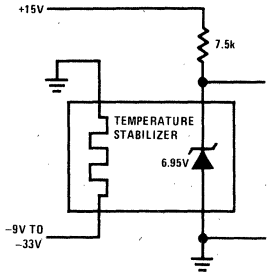
Single Supply Operation



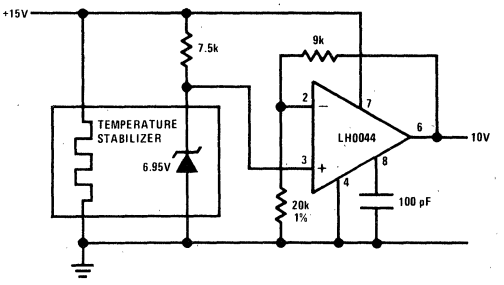
Split Supply Operation



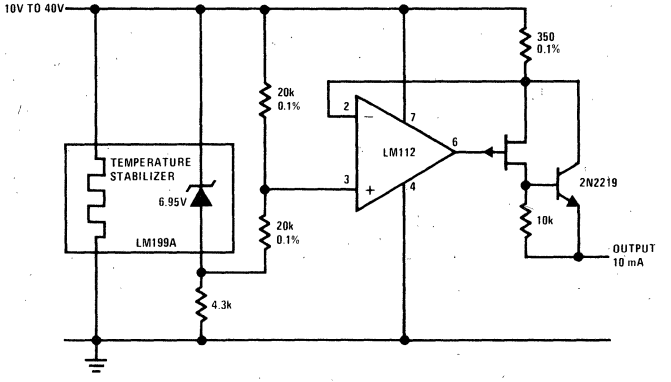
Negative Heater Supply with Positive Reference



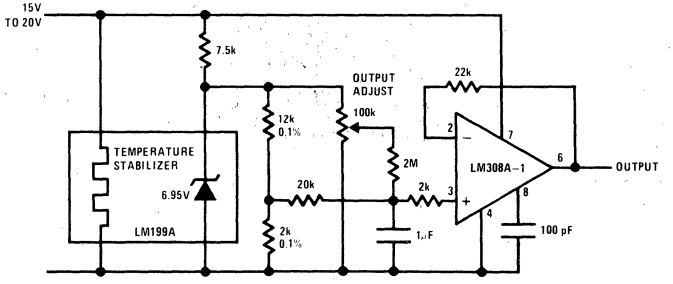
Buffered Reference With Single Supply



Positive Current Source

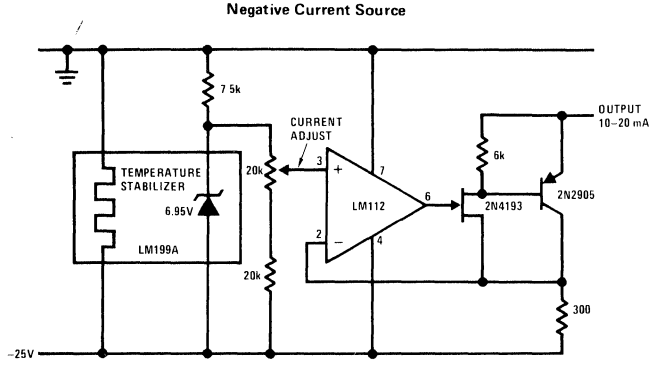


Standard Cell Replacement

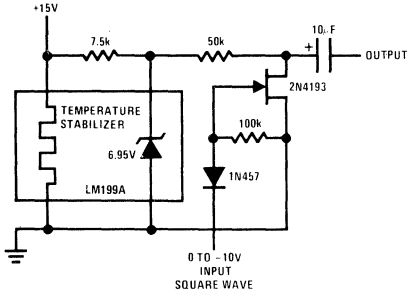


typical applications (con't)

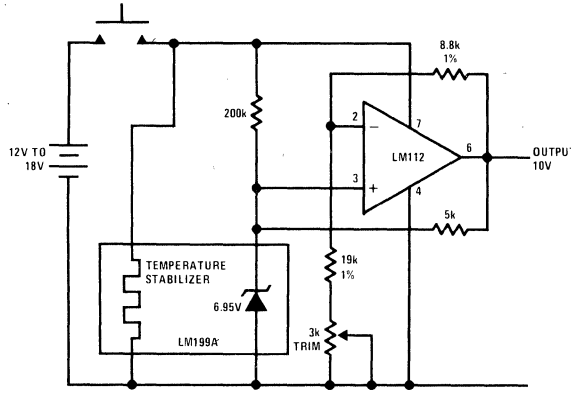
Negative Current Source



Square Wave Voltage Reference

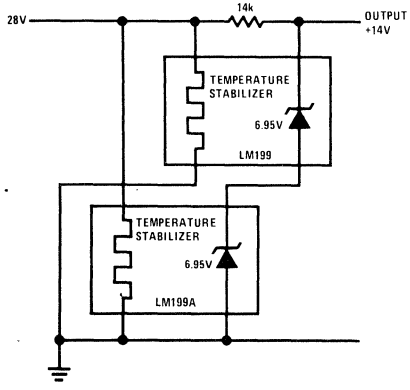


Portable Calibrator*

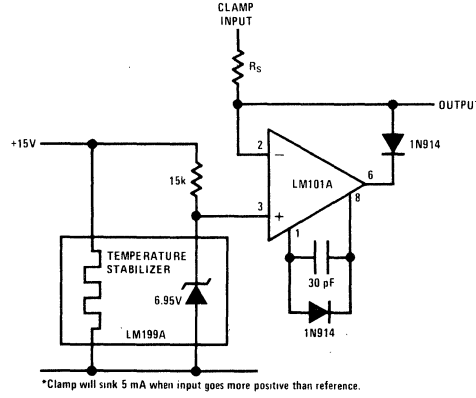


*Warm-up time 10 seconds; intermittant operation does not degrade long term stability.

14V Reference



Precision Clamp*

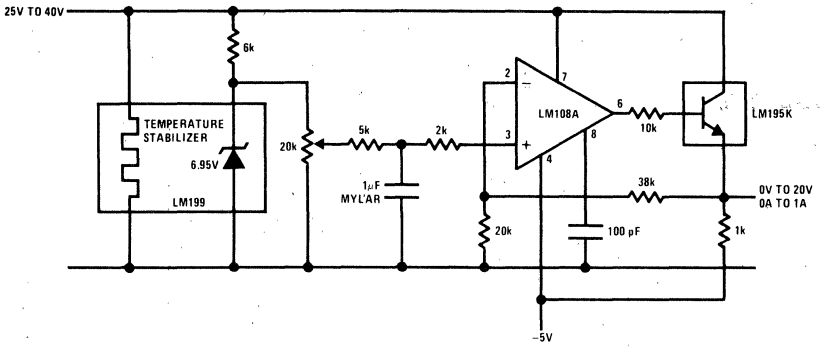


*Clamp will sink 5 mA when input goes more positive than reference.

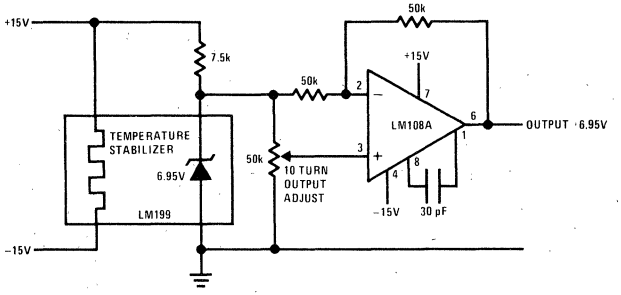
8

typical applications (con't)

0V to 20V Power Reference



Bipolar Output Reference



MM5330 4 1/2-digit panel meter logic block

general description

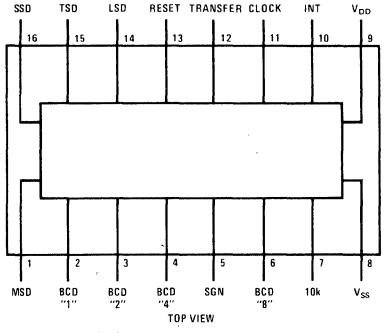
The MM5330 is a monolithic integrated circuit which provides the logic circuitry to implement a 4-1/2 digit panel meter. The MM5330 utilizes P-channel low threshold enhancement mode devices and ion-implanted depletion mode devices. All inputs and outputs are TTL compatible with BCD output for direct interface with various display drivers.

features

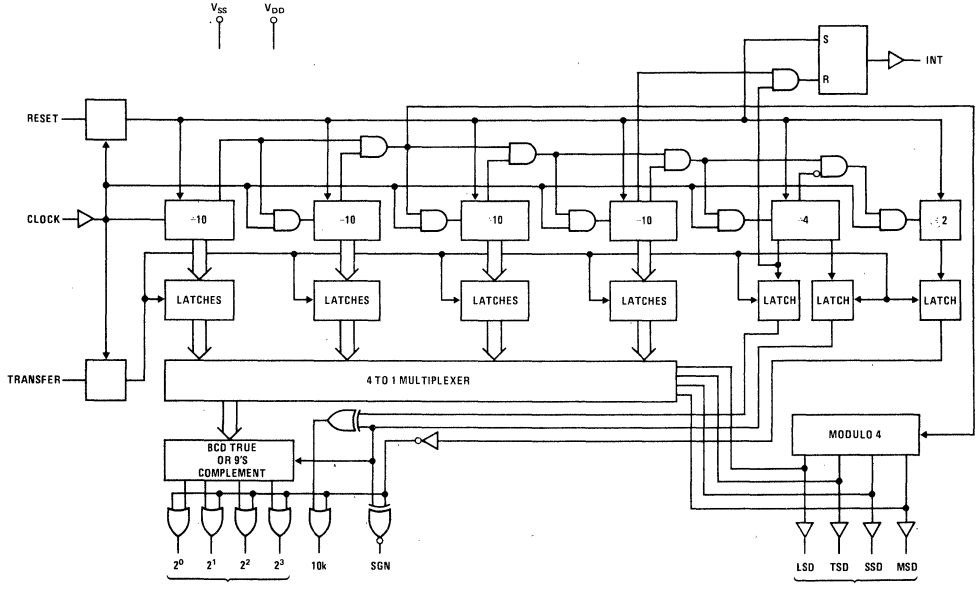
- dc to 400 kHz operation
- TTL compatible inputs and outputs
- BCD output code
- Overrange blanking
- Valid sign bit during overrange
- Standard supply voltages; +5, −15V

connection and block diagrams

Dual-In-Line Package



Order Number MM5330N
See Package 18



absolute maximum ratings

Voltage at Any Pin	V_{SS} + 0.3V to V_{SS} − 25V
Operating Temperature	0°C to +75°C
Storage Temperature	−40°C to +125°C
Lead Temperature (Soldering, 10 seconds)	300°C

electrical characteristics

T_A within operating range, V_{SS} = 4.75V to 5.25V, V_{DD} = −16.5V to −13.5V unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply Voltage (V_{SS})		4.75	5	5.25	V
Power Supply Voltage (V_{DD})		−16.5	−15	−13.5	V
Power Supply Current (I_{SS})	No Load			30	mA
Input Frequency		dc		400	kHz
Reset or Transfer Pulse Width		200			ns
Input Voltage Levels	V_{SS} = 5V, V_{DD} = −15V				
Logic "1"	Inputs Driven by TTL or Square Waves	3		5	V
Logic "0"	Inputs Driven by TTL or Square Waves	−15		0.8	V
Clock Input Voltage Levels					
Logic "1"	Driven by Sinewave	V_{SS}−0.5		V_{SS}+0.3	V
Logic "0"	Driven by Sinewave	V_{SS}−25		V_{SS}−4.5	V
Output Current Levels	V_{SS} = 5V, V_{DD} = −15V				
Digit Output State					
Logic "1"	V_O Forced To 4.75V	100			μA
Logic "0"	V_O Forced To 4.5V	−5		−20	mA
All Other Outputs					
Logic "1"	V_O Forced To 3V	100			μA
Logic "0"	V_O Forced To 0.4V	−2			mA
Delay From Digit Output to BCD Output		0.1		5	μs

FUNCTIONAL DESCRIPTION

Counters: The MM5330 has four ÷10 counters, one ÷4 counter, and one ÷2 for a count of 80,000 clock pulses. A ripple carry is provided and all counter flip-flops are synchronous with the negative transition of the input clock. The last flip-flop in the divider chain (÷2 in the block diagram) triggers with the "0" to "1" transition of the previous flip-flop. The count sequence is shown in the first column of the count diagram.

Reset: All counter stages are reset to "0" and the INT flip-flop (driving the INT output) is set to "1" on the first negative clock transition after a "0" is applied to the Reset input. The internal reset is removed on the first negative clock transition after the internal reset has occured and a "1" has been applied to the Reset input. This timing provides an on-chip reset at least one clock cycle wide and a one cycle delay to remove reset before counting begins.

Transfer: Data in the counters is transferred to the latches when the Transfer input is at "0." If the Transfer input is held low the state of the counters is continuously displayed (see count diagram). Data will cease to transfer to the latches on the first positive clock transition after the first negative clock transition after a "1" is applied to the Transfer input. This provides a transfer pulse at least one half clock cycle wide and a half clock cycle delay to remove the transfer signal before the counters change state.

INT: The integrate output is used to set the charge time on a dual slope integrator. INT is "1" from reset to the 18,000th clock pulse, then "0" until the next reset. The dual slope integrator is the voltage monitoring part of the external circuitry needed for a DPM. It charges a capacitor at a rate proportional to the measured voltage while INT is "1," then discharges at a rate proportional to a fixed reference as shown in the dual slope diagram. When the output of the integrator reaches 0V a pulse is generated and fed into the Transfer input of the chip. As the dual slope diagram indicates, the number in the latches is proportional to the measured voltage.

Multiplexing: The modulo 4 multiplex counter is triggered by the carry from the second decade counter, making the multiplex rate one hundredth the counting rate (4 kHz for a 400 kHz clock). The LSD, TSD, SSD and MSD (least significant, third significant, second significant and most significant digits) outputs indicate by a low level which decade latch is displayed at the BCD outputs.

FUNCTIONAL DESCRIPTION (Continued)

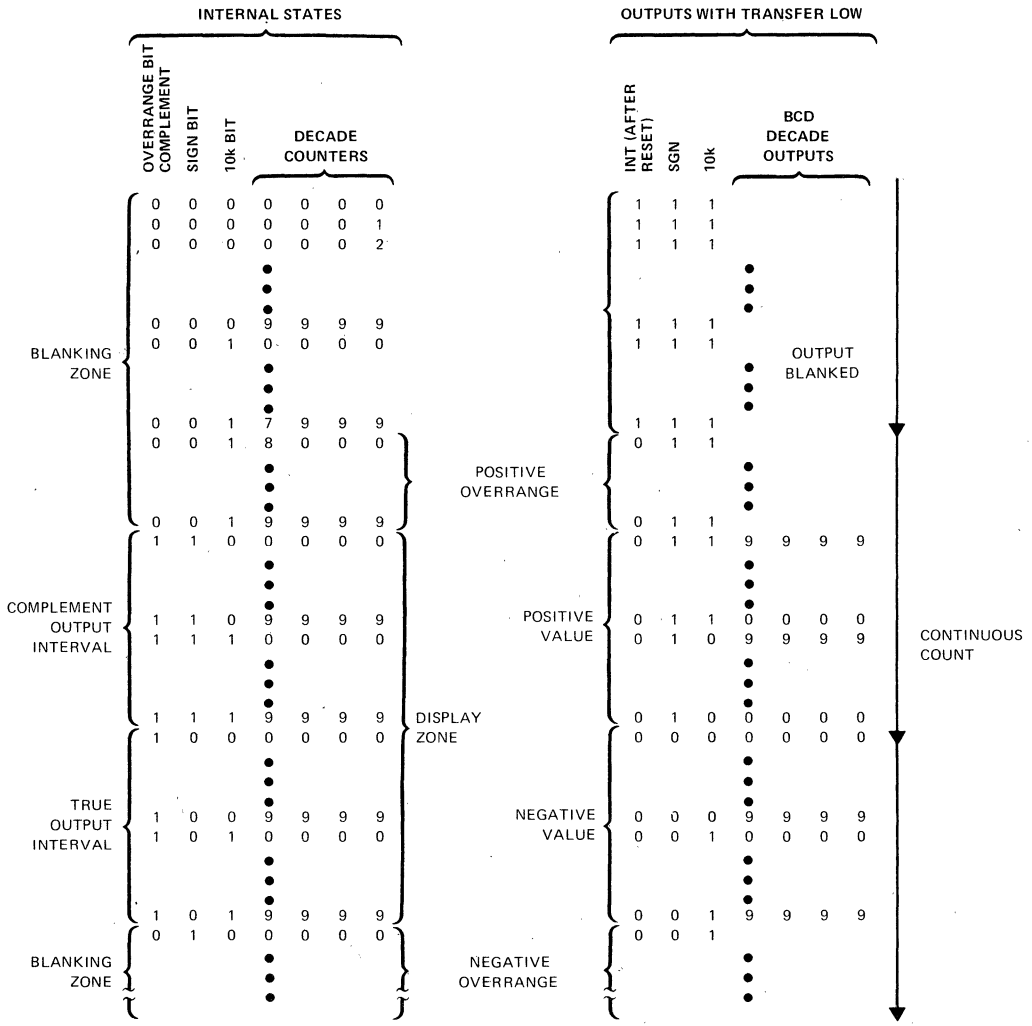
Overrange Blanking and Sign: The data in the latch for the ÷2 counter is used to detect an out-of-range voltage. If this latch is "0" the BCD and 10k outputs are forced to all "1's" and the SGN output is inverted. When the data in the overrange latch and the sign bit latch are "1" the sign bit generates the 9's complement of the decade latches and the complement of the 10k latch at the respective outputs. When the overrange bit is "1" and the sign bit is "0" true BCD of the decade latches and the uncomplemented 10k latch appear at the outputs.

APPLICATIONS INFORMATION

The MM5330 is the display and control for a modified dual slope system. It contains the counters and latches, together with a multiplexing system to provide 4 digits of display with one decoder driver. It also provides a sign digit, either plus or minus, and a ten-thousand counts digit for full display of ±19999. By eliminating the right-most digits it may also be used as a 2-1/2 or 3-1/2 digit DVM chip.

The basic modified dual slope system for which the MM5330 is designed, is shown in *Figure 1.* The integrator is now used in a non-inverting mode and is biased to integrate negatively for all voltages below V_{MAX}. Thus if the maximum positive voltage at V_{IN} is 1.9999V, then V_{MAX} would be set at 2.200V. In this way, all voltages measured are below V_{MAX}. This eliminates the need for reference switching and provides automatic polarity with no additional components. Also, it can be shown that the amplifier input bias currents which cause errors in conventional dual slope systems are eliminated by merely zeroing the display. Thus low bias current op amps are not necessarily required unless a high input impedance is desired at V_{IN}.

count diagram



APPLICATIONS INFORMATION (Continued)

Secondly, the use of a conventional op amp for a comparator allows zeroing of all voltage offsets in both the op amp and comparator. This is achieved by zeroing the voltage on the capacitor through the use of the comparator as part of a negative feedback loop. During the zeroing period, the non-inverting input of the integrator is at V_{REF}. As this voltage is within the active common-mode range of the integrator the loop will respond by placing the integrator and comparator in the active region. The voltage on the capacitor is no longer equal to zero, but rather to a voltage which is the sum of both the op amp and comparator offset voltages. Because of the intrinsic nature of an integrator, this constant voltage remains throughout the integrating cycle and serves to eliminate even large offset voltages.

The waveforms at the output of the integrator are as shown. The voltage at A is the comparator threshold just discussed. Simultaneously, with the opening of switch A, V_{IN} is connected to the input of the integrator via switch B. The output then slews to V_{IN}. Integration then begins for the reference period, after which time the reference voltage is again applied to the input. The output again slews the difference between V_{REF} and V_{IN} and integrates for the unknown period until the comparator threshold is crossed. At this point, the accumulated counts are transferred from the counters to the latches and zeroing begins until the next conversion interval.

It may be obvious, however, that while we have eliminated several of the basic dual slope circuits disadvantages, we have created another—the number of counts are no longer proportional to V_{IN} but rather to $(V_{MAX}-V_{IN})$. In fact, when we short V_{IN} to ground we are actually measuring our own 2.2000 V_{MAX}.

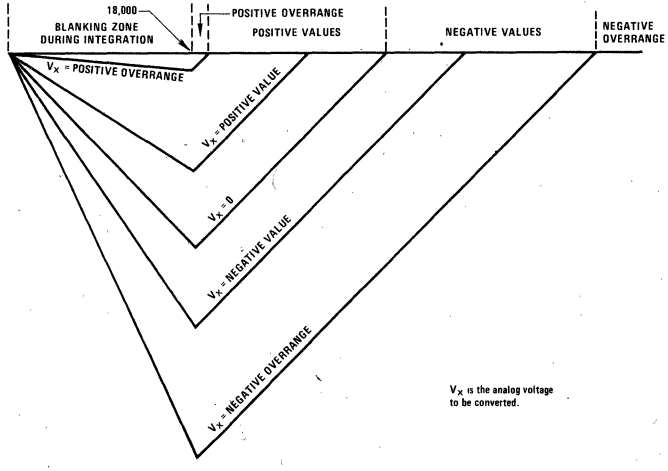
What is done in the MM5330 is to code convert the number of counts as shown in the count diagram. This chart shows a code conversion starting at the time of a reset. The first 18,000 counts are the reference period after which time the integrator changes slope. If a comparator crossing is detected within the next 2000 counts, a plus overrange condition will occur at the display. This condition results in a lit "+" sign, a lit "1" and four blanked rightmost digits. A transfer at 20,000 however, will create a reading of +1.9999, at 20,001 a reading of 19.998 and so on, until at 39,999 a reading of +0000 would be displayed. A transfer occuring at 40,000 would cause a −0000 display and so on until 60,000 counts were entered at which time a −1 with four blanked digits would be displayed indicating a minus overrange condition.

A typical circuit for a low cost 4 1/2 digit DPM is shown in *Figure 2*. The display interface used is a TTL, 7-segment decoder driver and four P-type transistors. The ±1 digit is driven directly by CMOS. The clock-synchronous reset and transfer functions prevent any cyclic digit variations and present a blink-free, flicker-free display. CMOS analog switches are used as reference, zero, and input switches and used also in the comparator slew rate circuit.

A problem with all dual slope systems occurs when short integrating times and high clock frequencies are used. Because of the very slow rise time of the ramp into the comparator, the output of the comparator will normally ramp at approximately 1/10 of its actual slew rate. Thus, a significant number of extra counts are displayed due to the slow rate of rise of the comparator. A technique to improve this consists of capacitor C_S and analog switch four. An unstable positive loop is created by this capacitor when the comparator comes out of saturation. This causes the output to rise at its slew rate to the comparator threshold. As soon as this threshold is reached the analog switch opens and zeroing is initiated as previously discussed.

A simplified approach to performing the modified dual slope function combines the MM5330 and the LF11300 dual slope analog block as in *Figure 3*. The LF11300 provides the front analog circuitry required. This includes a FET input amplifier, analog switches, integrator and comparator. The LF11300 provides auto zero, > 1000 MΩ input impedance, and a ±10V analog range.

dual slope diagram



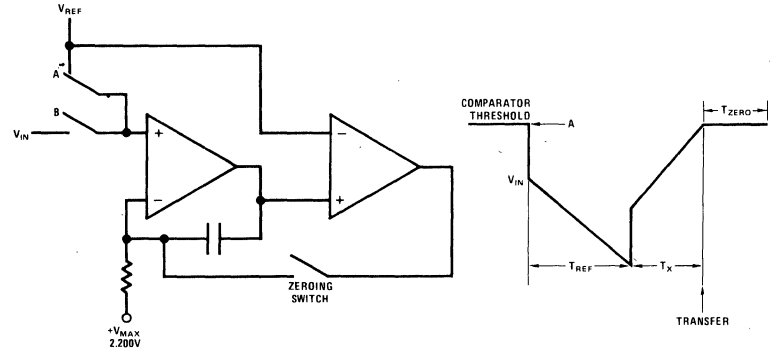


FIGURE 1. Modified Dual Slope

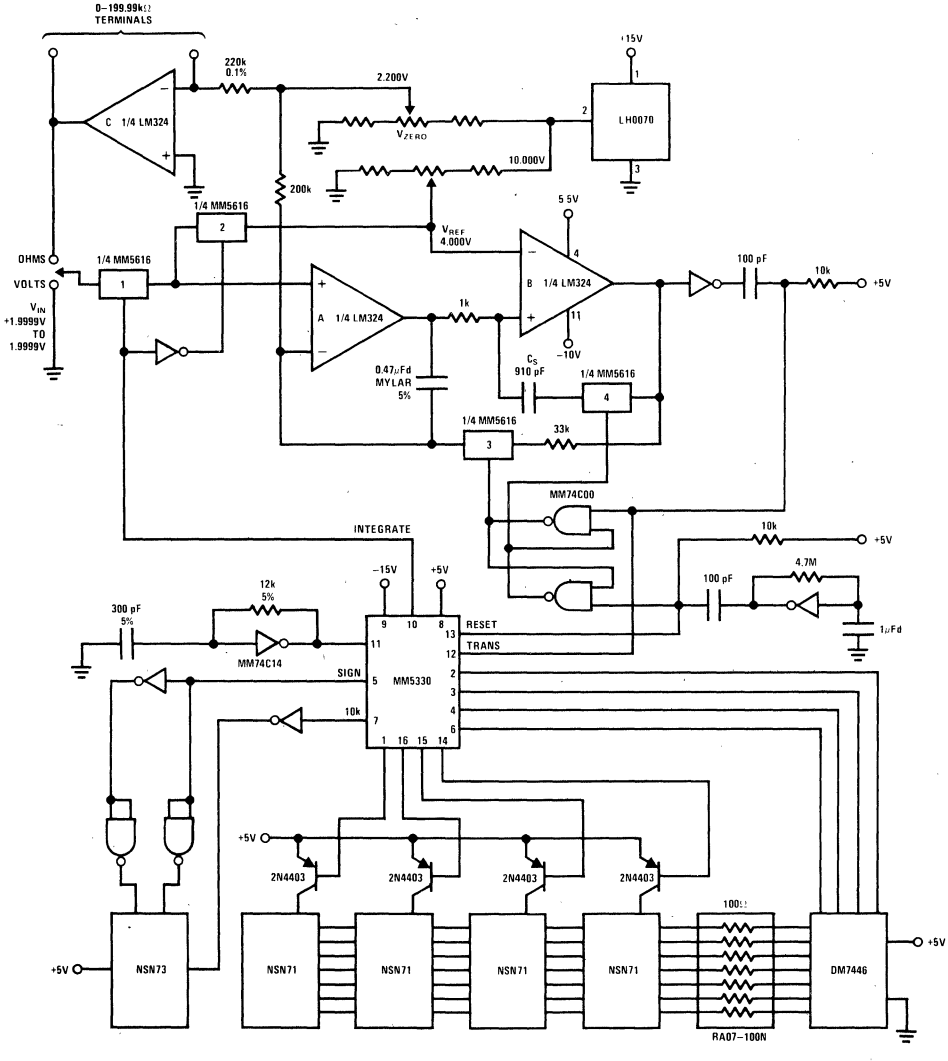


FIGURE 2. Typical Application Low Cost 4 1/2 Digit Volt-Ohm Meter

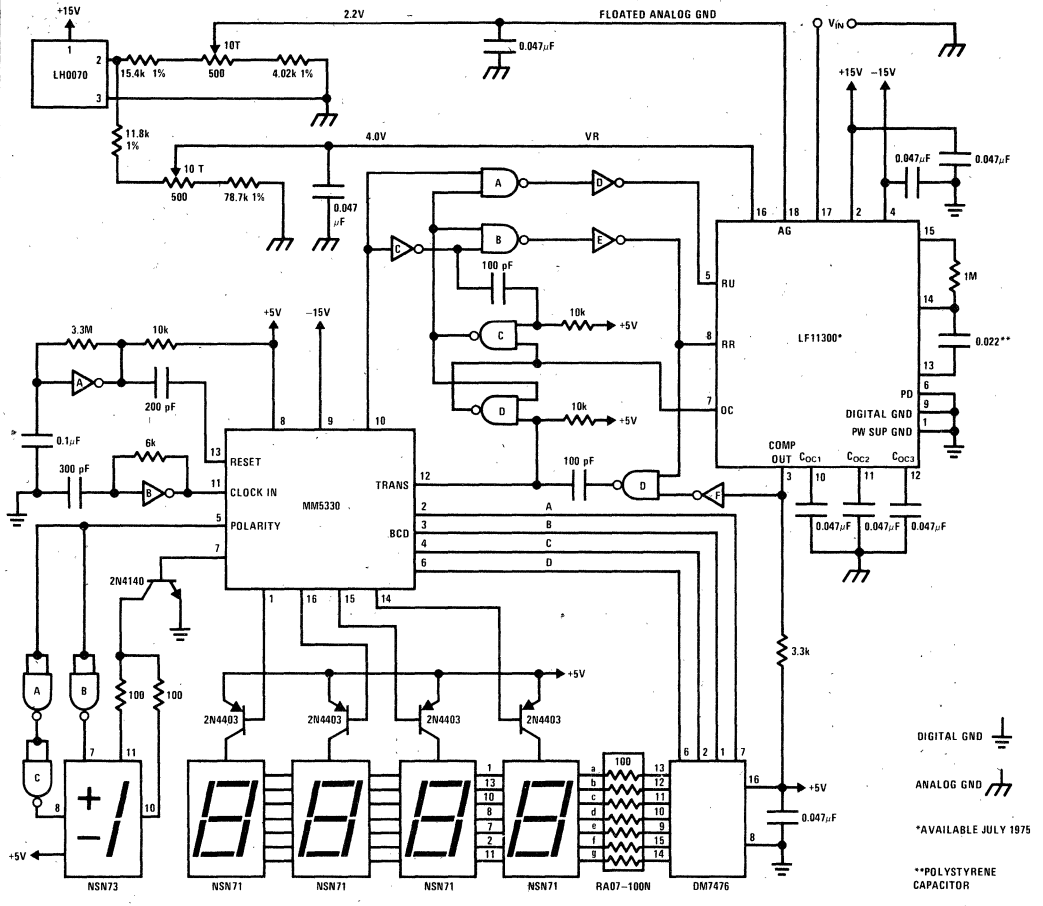


FIGURE 3. DPM Using MM5330 and LF11300

NATIONAL

DM2502, DM2503, DM2504 successive approximation registers

general description

The DM2502, DM2503 and DM2504 are 8-bit and 12-bit TTL registers designed for use in successive approximation A/D converters. These devices contain all the logic and control circuits necessary in combination with a D/A converter to perform successive approximation analog-to-digital conversions.

The DM2502 has 8 bits with serial capability and is not expandable.

The DM2503 has 8 bits and is expandable without serial capability.

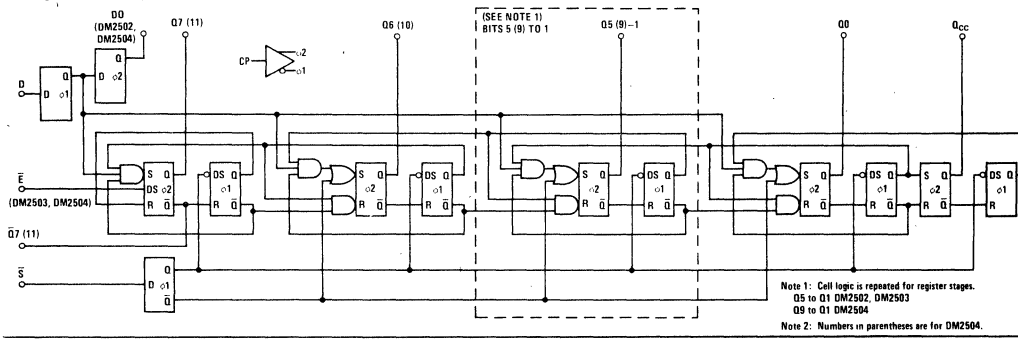
The DM2504 has 12 bits with serial capability and expandability.

All three devices are available in ceramic DIP, ceramic flatpak, and molded Epoxy-B DIPs. The DM2502, DM2503 and DM2504 operate over −55°C to +125°C; the DM2502C, DM2503C and DM2504C operate over 0°C to +70°C.

features

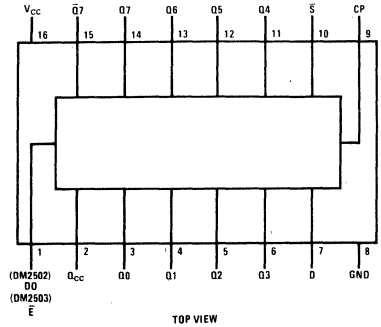
- Complete logic for successive approximation A/D converters
- 8-bit and 12-bit registers
- Capable of short cycle or expanded operation
- Continuous or start-stop operation
- Compatible with D/A converters using any logic code
- Active low or active high logic outputs
- Use as general purpose serial-to-parallel converter or ring counter

logic diagram



connection diagrams (Dual-In-Line and Flat Packages)

DM2502, DM2503



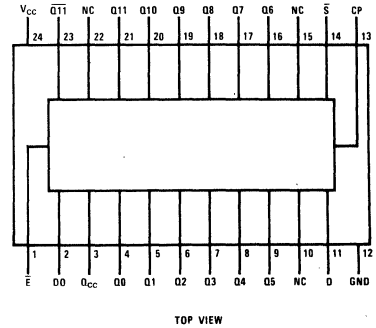
TOP VIEW

Order Numbers

DM2502J	DM2503J
DM2502CJ	DM2503CJ
DM2502CN	DM2503CN
DM2502W	DM2503W
DM2502CW	DM2503CW

See Packages 18 and 22

DM2504



TOP VIEW

Order Numbers

DM2504J
DM2504CJ
DM2504CN

See Packages 20 and 23

8

absolute maximum ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Output Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage, V_{CC}			
DM2502C, DM2503C, DM2504C	4.75	5.25	V
DM2502, DM2503, DM2504	4.5	5.5	V
Temperature, T_A			
DM2502C, DM2503C, DM2504C	0	+70	°C
DM2502, DM2503, DM2504	−55	+125	°C

electrical characteristics (Notes 2 and 3) V_{CC} = 5.0V, T_A = 25°C, C_L = 15 pF, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Logical "1" Input Voltage (V_{IH})	V_{CC} = Min	2.0			V
Logical "1" Input Current (I_{IH})	V_{CC} = Max				
CP Input	V_{IH} = 2.4V		6	40	μA
D, $\overline{E}$, $\overline{S}$ Inputs	V_{IH} = 2.4V		6	80	μA
All Inputs	V_{IH} = 5.5V			1.0	mA
Logical "0" Input Voltage (V_{IL})	V_{CC} = Min			0.8	V
Logical "0" Input Current (I_{IL})	V_{CC} = Max				
CP, $\overline{S}$ Inputs	V_{IL} = 0.4V		−1.0	−1.6	mA
D, $\overline{E}$ Inputs	V_{IL} = 0.4V		−1.0	−3.2	mA
Logical "1" Output Voltage (V_{OH})	V_{CC} = Min, I_{OH} = −0.48 mA	2.4	3.6		V
Output Short Circuit Current (Note 4) (I_{OS})	V_{CC} = Max; V_{OUT} = 0.0V; Output High; CP, D, $\overline{S}$, High; $\overline{E}$ Low	−10	−20	−45	mA
Logical "0" Output Voltage (V_{OL})	V_{CC} = Min, I_{OL} = 9.6 mA		0.2	0.4	V
Supply Current (I_{CC})	V_{CC} = Max, All Outputs Low				
DM2502C			65	95	mA
DM2502			65	85	mA
DM2503C			60	90	mA
DM2503			60	80	mA
DM2504C			90	124	mA
DM2504			90	110	mA
Propagation Delay to a Logical "0" From CP to Any Output (t_{pd0})		10	18	28	ns
Propagation Delay to a Logical "0" From $\overline{E}$ to Q7 (Q11) Output (t_{pd0})	CP High, $\overline{S}$ Low DM2503, DM2503C, DM2504, DM2504C Only		16	24	ns
Propagation Delay to a Logical "1" From CP to Any Output (t_{pd1})		10	26	38	ns
Propagation Delay to a Logical "1" From $\overline{E}$ to Q7 (Q11) Output (t_{pd1})	CP High, $\overline{S}$ Low DM2503, DM2503C, DM2504, DM2504C Only		13	19	ns
Set-Up Time Data Input ($t_{s(D)}$)		−10	4	8	ns
Set-Up Time Start Input ($t_{s(\overline{S})}$)		0	9	16	ns
Minimum Low CP Width (t_{PWL})			30	42	ns
Minimum High CP Width (t_{PWH})			17	24	ns
Maximum Clock Frequency (f_{MAX})		15	21		MHz

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DM2502, DM2503 and DM2504, and across the 0°C to +70°C range for the DM2502C, DM2503C and DM2504C. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Only one output at a time should be shorted.

application information

OPERATION

The registers consist of a set of master latches that act as the control elements in the device and change state on the input clock high-to-low transition and a set of slave latches that hold the register data and change on the input clock low-to-high transition. Externally the device acts as a special purpose serial-to-parallel converter that accepts data at the D input of the register and sends the data to the appropriate slave latch to appear at the register output and the DO output on the DM2502 and DM2504 when the clock goes from low-to-high. There are no restrictions on the data input; it can change state at any time except during a short interval centered about the clock low-to-high transition. At the same time that data enters the register bit the next less significant bit register is set to a low ready for the next iteration.

The register is reset by holding the $\overline{S}$ (Start) signal low during the clock low-to-high transition. The register synchronously resets to the state Q7 (11) low, and all the remaining register outputs high. The Q_{CC} (Conversion Complete) signal is also set high at this time. The $\overline{S}$ signal should not be brought back high until after the clock low-to-high transition in order to guarantee correct resetting. After the clock has gone high resetting the register, the $\overline{S}$ signal must be removed. On the next clock low-to-high transition the data on the D input is set into the Q7 (11) register bit and the Q6 (10) register bit is set to a low ready for the next clock cycle. On the next clock low-to-high transition data enters the Q6 (10) register bit and Q5 (9) is set to a low. This operation is repeated for each register bit in turn until the register has been filled. When the data goes into Q0, the Q_{CC} signal goes low, and the register is inhibited from further change until reset by a Start signal.

The DM2502, DM2503 and DM2504 have a specially tailored two-phase clock generator to provide non-overlapping two-phase clock pulses (i.e., the clock waveforms intersect below the thresholds of the gates they drive). Thus, even at very slow dV/dt rates at the clock input (such as from relatively weak comparator outputs), improper logic operation will not result.

LOGIC CODES

All three registers can be operated with various logic codes. Two's complement code is used by offsetting the comparator 1/2 full range + 1/2 LSB and using the complement of the MSB ($\overline{Q7}$ or $\overline{Q11}$) with a binary D/A converter. Offset binary is used in the same manner but with the MSB (Q7 or Q11). BCD D/A converters can be used with the addition of illegal code suppression logic.

ACTIVE HIGH OR ACTIVE LOW LOGIC

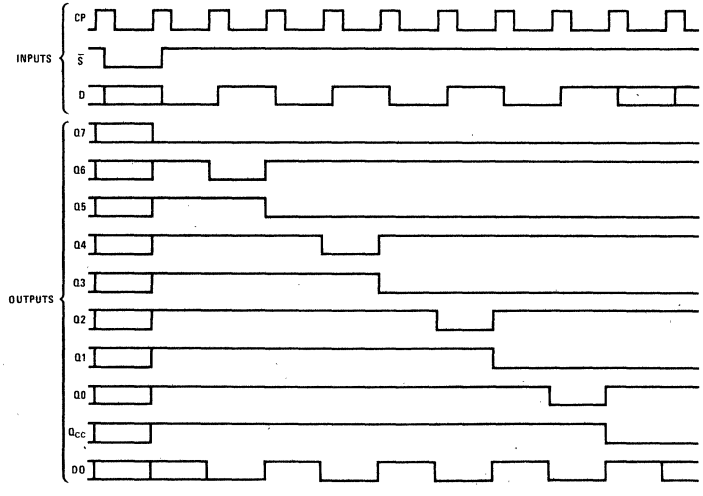
The register can be used with either D/A converters that require a low voltage level to turn on, or D/A converters that require a high voltage level to turn the switch on. If D/A converters are used which turn on with a low logic level, the resulting digital output from the register is active low. That is, a logic "1" is represented as a low voltage level. If D/A converters are used that turn on with a high logic level then the digital output is active high; a logic "1" is represented as a high voltage level.

EXPANDED OPERATION

An active low enable input, $\overline{E}$, on the DM2503 and DM2504 allows registers to be connected together to form a longer register by connecting the clock, D, and $\overline{S}$ inputs in parallel and connecting the Q_{CC} output of one register to the $\overline{E}$ input of the next less significant register. When the start signal resets the register, the $\overline{E}$ signal goes high, forcing the Q7 (11) bit high and inhibiting the register from accepting data until the previous register is full and its Q_{CC} goes low. If only one register is used the $\overline{E}$ input should be held at a low logic level.

timing diagram

DM2502, DM2503



application information (con't)

SHORT CYCLE

If all bits are not required, the register may be truncated and conversion time saved by using a register output going low rather than the Q_{CC} signal to indicate the end of conversion. If the register is truncated and operated in the continuous conversion mode, a lock-up condition may occur on power turn-on. This condition can be avoided by making the start input the OR function of Q_{CC} and the appropriate register output.

COMPARATOR BIAS

To minimize the digital error below ±1/2 LSB, the comparator must be biased. If a D/A converter is used which requires a low voltage level to turn on, the comparator should be biased +1/2 LSB. If the D/A converter requires a high logic level to turn on, the comparator must be biased −1/2 LSB.

definition of terms

CP: The clock input of the register.

D: The serial data input of the register.

DO: The serial data out. (The D input delayed one bit).

$\overline{E}$: The register enable. This input is used to expand the length of the register and when high forces the Q7 (11) register output high and inhibits conversion. When not used for expansion the enable is held at a low logic level (ground).

Q_i i = 7 (11) to 0: The outputs of the register.

Q_{CC}: The conversion complete output. This output remains high during a conversion and goes low when a conversion is complete.

Q7 (11): The true output of the MSB of the register.

$\overline{Q7}$ (11): The complement output of the MSB of the register.

$\overline{S}$: The start input. If the start input is held low for at least a clock period the register will be reset to Q7 (11) low and all the remaining outputs high. A start pulse that is low for a shorter period of time can be used if it meets the set-up time requirements of the $\overline{S}$ input.

truth table

DM2502, DM2503

TIME	INPUTS			OUTPUTS[1]									
t_n	D	$\overline{S}$	$\overline{E}$[2]	DO[3]	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0	Q_{CC}
0	X	L	L	X	X	X	X	X	X	X	X	X	X
1	D7	H	L	X	L	H	H	H	H	H	H	H	H
2	D6	H	L	D7	D7	L	H	H	H	H	H	H	H
3	D5	H	L	D6	D7	D6	L	H	H	H	H	H	H
4	D4	H	L	D5	D7	D6	D5	L	H	H	H	H	H
5	D3	H	L	D4	D7	D6	D5	D4	L	H	H	H	H
6	D2	H	L	D3	D7	D6	D5	D4	D3	L	H	H	H
7	D1	H	L	D2	D7	D6	D5	D4	D3	D2	L	H	H
8	D0	H	L	D1	D7	D6	D5	D4	D3	D2	D1	L	H
9	X	H	L	D0	D7	D6	D5	D4	D3	D2	D1	D0	L
10	X	X	L	X	D7	D6	D5	D4	D3	D2	D1	D0	L
	X	X	H	X	H	NC	NC	NC	NC	NC	NC	NC	NC

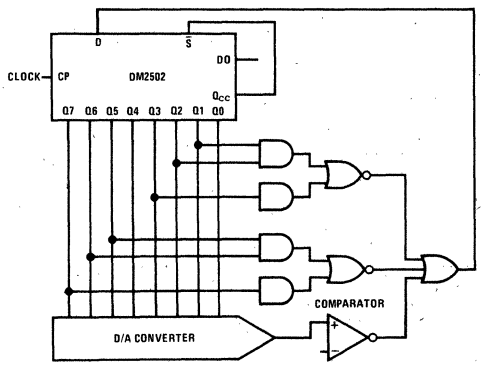
Note 1: Truth table for DM2504 is extended to include 12 outputs.

Note 2: Truth table for DM2502 does not include $\overline{E}$ column or last line in truth table shown.

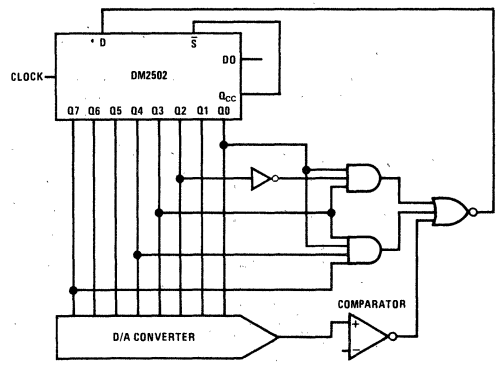
Note 3: Truth table for DM2503 does not include D0 column.

H = High Voltage Level
L = Low Voltage Level
X = Don't Care
NC = No Change

typical applications



Active High

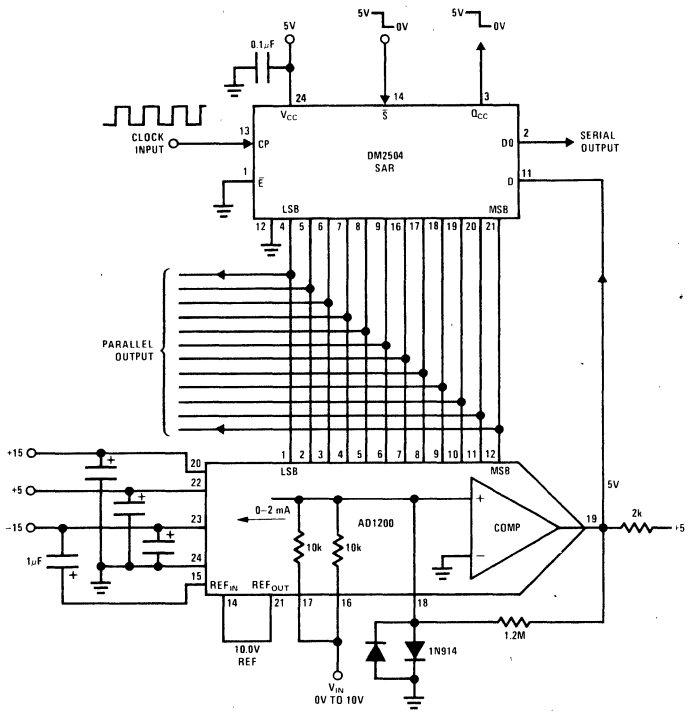


Active Low

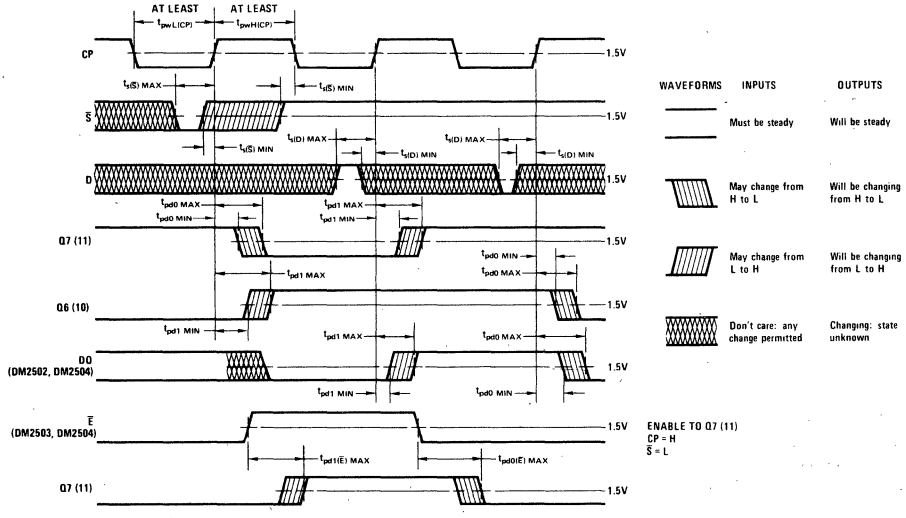
BCD Illegal Code Suppression

typical applications (con't)

High Speed 12-Bit A/D Converter



switching time waveforms



NATIONAL

MM54C905/MM74C905 12-bit successive approximation register

general description

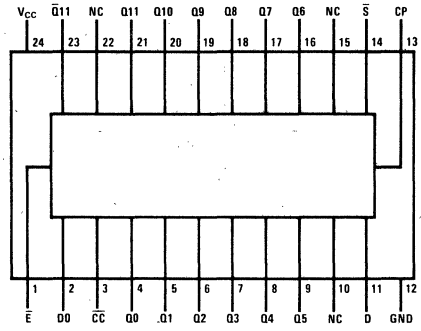
The MM54C905/MM74C905 CMOS 12-bit successive approximation register contains all the digit control and storage necessary for successive approximation analog-to-digital conversion. Because of the unique capability of CMOS to switch to each supply rail without any offset voltage, it can also be used in digital systems as the control and storage element in repetitive routines.

features

- Wide supply voltage range 3.0V to 15V
- Guaranteed noise margin 1.0V
- High noise immunity 0.45 V_{CC} typ
- Low power TTL compatibility fan out of 2 driving 74L
- Provision for register extension or truncation
- Operates in START/STOP or continuous conversion mode
- Drive ladder switches directly. For 10 bits or less with 50k/100k R/2R ladder network

connection diagram

Dual-In-Line Package



Order Numbers
MM54C905D
MM74C905D
MM74C905N
See Packages 20 and 21

truth table

TIME	INPUTS			OUTPUTS												
t_n	D	$\overline{S}$	$\overline{E}$	D0	Q11	Q10	Q9	Q8	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0	$\overline{CC}$
0	X	L	L	X	X	X	X	X	X	X	X	X	X	X	X	X	X
1	D11	H	L	X	L	H	H	H	H	H	H	H	H	H	H	H	H
2	D10	H	L	D11	D11	L	H	H	H	H	H	H	H	H	H	H	H
3	D9	H	L	D10	D11	D10	L	H	H	H	H	H	H	H	H	H	H
4	D8	H	L	D9	D11	D10	D9	L	H	H	H	H	H	H	H	H	H
5	D7	H	L	D8	D11	D10	D9	D8	L	H	H	H	H	H	H	H	H
6	D6	H	L	D7	D11	D10	D9	D8	D7	L	H	H	H	H	H	H	H
7	D5	H	L	D6	D11	D10	D9	D8	D7	D6	L	H	H	H	H	H	H
8	D4	H	L	D5	D11	D10	D9	D8	D7	D6	D5	L	H	H	H	H	H
9	D3	H	L	D4	D11	D10	D9	D8	D7	D6	D5	D4	L	H	H	H	H
10	D2	H	L	D3	D11	D10	D9	D8	D7	D6	D5	D4	D3	L	H	H	H
11	D1	H	L	D2	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	L	H	H
12	D0	H	L	D1	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	L	H
13	X	H	L	D0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	L
14	X	X	L	X	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	L
	X	X	H	X	H	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC

H = High level L = Low level X = Don't care NC = No change

absolute maximum ratings (Note 1)

Voltage at Any Pin	−0.3V to V_{CC} +0.3V
Operating Temperature Range	
MM54C905	−55°C to +125°C
MM74C905	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500 mW
Operating V_{CC} Range	3.0V to 15V
Absolute Maximum V_{CC}	16V
Lead Temperature (Soldering, 10 seconds)	300°C

dc electrical characteristics Min/max limits apply across temperature range, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CMOS TO CMOS					
Logical "1" Input Voltage ($V_{IN(1)}$)	V_{CC} = 5.0V	3.5			V
	V_{CC} = 10V	8.0			V
Logical "0" Input Voltage ($V_{IN(0)}$)	V_{CC} = 5.0V			1.5	V
	V_{CC} = 10V			2.0	V
Logical "1" Output Voltage ($V_{OUT(1)}$)	V_{CC} = 5.0V, I_O = −10μA	4.5			V
	V_{CC} = 10V, I_O = −10μA	9.0			V
Logical "0" Output Voltage ($V_{OUT(0)}$)	V_{CC} = 5.0V, I_O = 10μA			0.5	V
	V_{CC} = 10V, I_O = 10μA			1.0	V
Logical "1" Input Current ($I_{IN(1)}$)	V_{CC} = 15V, V_{IN} = 15V		0.005	1.0	μA
Logical "0" Input Current ($I_{IN(0)}$)	V_{CC} = 15V, V_{IN} = 0V	−1.0	−0.005		μA
Supply Current (I_{CC})	V_{CC} = 15V		0.05	300	μA
CMOS/LPTTL INTERFACE					
Logical "1" Input Voltage ($V_{IN(1)}$)					
MM54C905	V_{CC} = 4.5V	V_{CC}−1.5			V
MM74C905	V_{CC} = 4.75V	V_{CC}−1.5			V
Logical "0" Input Voltage ($V_{IN(0)}$)					
MM54C905	V_{CC} = 4.5V			0.8	V
MM74C905	V_{CC} = 4.75V			0.8	V
Logical "1" Output Voltage ($V_{OUT(1)}$)					
MM54C905	V_{CC} = 4.5V, I_O = −360μA	2.4			V
MM74C905	V_{CC} = 4.75V, I_O = −360μA	2.4			V
Logical "0" Output Voltage ($V_{OUT(0)}$)					
MM54C905	V_{CC} = 4.5V, I_O = 360μA			0.4	V
MM74C905	V_{CC} = 4.75V, I_O = 360μA			0.4	V
OUTPUT DRIVE (See 54C/74C Family Characteristics Data Sheet)					
Output Source Current (I_{SOURCE}) (P-Channel)	V_{CC} = 5.0V, V_{OUT} = 0V, T_A = 25°C	−1.75	−3.3		mA
Output Source Current (I_{SOURCE}) (P-Channel)	V_{CC} = 10V, V_{OUT} = 0V, T_A = 25°C	−8.0	−15		mA
Output Sink Current (I_{SINK}) (N-Channel)	V_{CC} = 5.0V, V_{OUT} = V_{CC}, T_A = 25°C	1.75	3.6		mA
Output Sink Current (I_{SINK}) (N-Channel)	V_{CC} = 10V, V_{OUT} = V_{CC}, T_A = 25°C	8.0	16		mA
Q11–Q0 Outputs	V_{CC} = 10V ±5%				
R_{SOURCE}	V_{OUT} = V_{CC} − 0.3V, T_A = 25°C	150		350	Ω
R_{SINK}	V_{CC} = 10V ±5%, V_{OUT} = 0.3V, T_A = 25°C	80		230	Ω

8

ac electrical characteristics $T_A = 25°C$, $C_L = 50$ pF, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Propagation Delay Time From Clock Input To Outputs (Q0–Q11) ($t_{pd(Q)}$)	$V_{CC} = 5.0V$		200	350	ns
	$V_{CC} = 10V$		80	150	ns
Propagation Delay Time From Clock Input To D_O ($t_{pd(D_O)}$)	$V_{CC} = 5.0V$		180	325	ns
	$V_{CC} = 10V$		70	125	ns
Propagation Delay Time From Register Enable ($\overline{E}$) To Output (Q11) ($t_{pd(\overline{E})}$)	$V_{CC} = 5.0V$		190	350	ns
	$V_{CC} = 10V$		75	150	ns
Propagation Delay Time From Clock To $\overline{CC}$ ($t_{pd(\overline{CC})}$)	$V_{CC} = 5.0V$		190	350	ns
	$V_{CC} = 10V$		75	0.50	ns
Data Input Set-Up Time (t_{DS})	$V_{CC} = 5.0V$	80			ns
	$V_{CC} = 10V$	30			ns
Start Input Set-Up Time (t_{SS})	$V_{CC} = 5.0V$	80			ns
	$V_{CC} = 10V$	30			ns
Minimum Clock Pulse Width (t_{PWL}, t_{PWH})	$V_{CC} = 5.0V$	250	125		ns
	$V_{CC} = 10V$	100	50		ns
Maximum Clock Rise and Fall Time (t_r, t_f)	$V_{CC} = 5.0V$			15	μs
	$V_{CC} = 10V$			5	μs
Maximum Clock Frequency (f_{MAX})	$V_{CC} = 5.0V$	2	4		MHz
	$V_{CC} = 10V$	5	10		MHz
Clock Input Capacitance (C_{CLK})	Clock Input (Note 2)		10		pF
Input Capacitance (C_{IN})	Any Other Input (Note 2)		5		pF
Power Dissipation Capacitance (C_{PD})	(Note 3)		100		pF

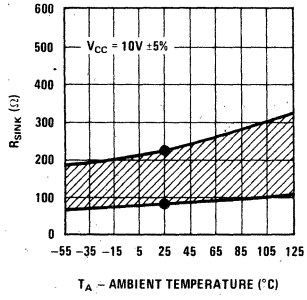
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note, AN-90.

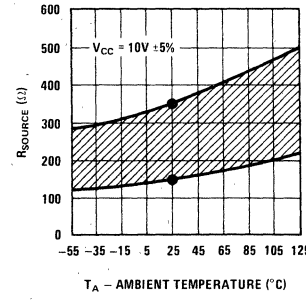
typical performance characteristics

R_{SINK} vs Temperature



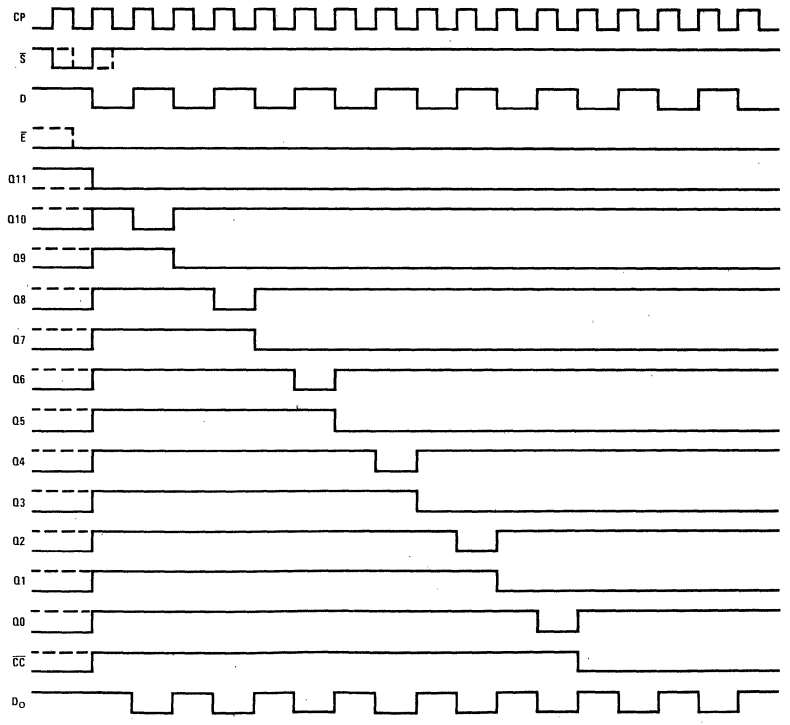
● These points are guaranteed by automatic testing.

R_{SOURCE} vs Temperature

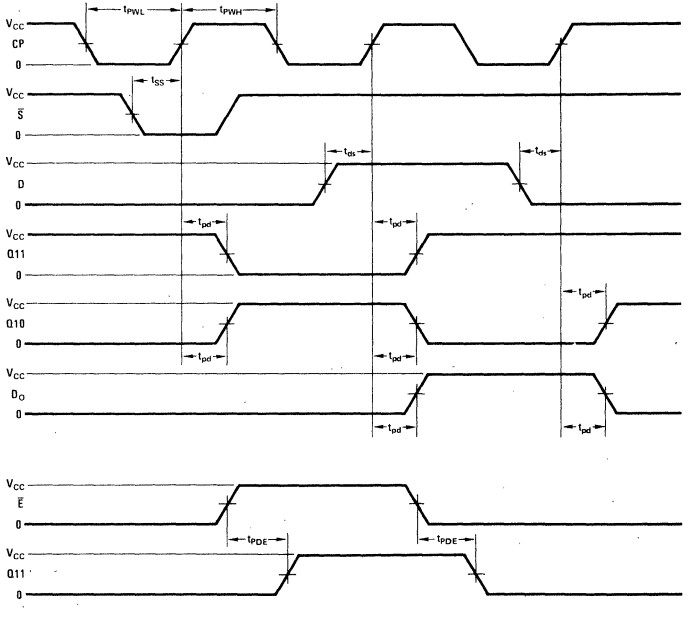


● These points are guaranteed by automatic testing.

timing diagram



switching time waveforms



USER NOTES FOR A/D CONVERSION

The register can be used with either current switches that require a low voltage level to turn the switch ON or current switches that require a high voltage level to turn the switch ON. If current switches are used which turn ON with a low logic level, the resulting digit output from the register is active low. That is, a logic "1" is represented as a low voltage level. If current switches are used which turn ON with a high logic level, the resulting digit output is active high. A logic "1" is represented as a high voltage level.

For a maximum error of ±1/2 LSB, the comparator must be biased. If current switches that require a high voltage level to turn ON are used, the comparator should be biased +1/2 LSB and if the current switches require a low logic level to turn ON, then the comparator must be biased −1/2 LSB.

The register can be used to perform 2's complement conversion by offsetting the comparator one half full range +1/2 LSB and using the complement of the MSB Q11 as the sign bit.

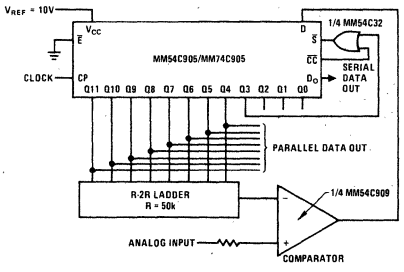
If the register is truncated and operated in the continuous conversion mode, a lock-up condition may occur on power-ON. This situation can be overcome by making the START input the "OR" function of $\overline{CC}$ and the appropriate register output.

The register, by suitable selection of register ladder network, can be used to perform either binary or BCD conversion.

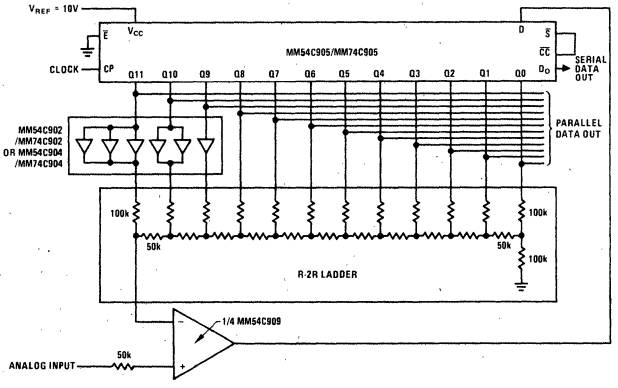
The register outputs can drive the 10 bits or less with 50k/100k R/2R ladder network directly for V_{CC} = 10V or higher. In order to drive the 12-bit 50k/100k ladder network and have the ±1/2 LSB resolution, the MM54C902/MM74C902 or MM54C904/MM74C904 is used as buffers, three buffers for MSB (Q11), two buffers for Q10, and one buffer for Q9.

typical applications

12-Bit Successive Approximation A-to-D Converter Operating in Continuous 8-Bit Truncated Mode



12-Bit Successive Approximation A-to-D Converter, Operating in Continuous Mode, Drives the 50k/100k Ladder Network Directly



definition of terms

CP: Register *clock* input.

$\overline{CC}$: *Conversion complete*—this output remains at $V_{OUT(1)}$ during a conversion and goes to $V_{OUT(0)}$ when conversion is complete.

D: Serial *data* input—connected to comparator output in A-to-D applications.

$\overline{E}$: *Register enable*—this input is used to expand the length of the register. When $\overline{E}$ is at $V_{IN(1)}$ Q11 is forced to $V_{OUT(1)}$ and inhibits conversion. When not used for expansion $\overline{E}$ must be connected to $V_{IN(0)}$ (GND).

Q11: True register MSB output.

$\overline{Q11}$: Complement of register MSB output.

Qi (i = 0 to 11): Register outputs.

$\overline{S}$: *Start input*—holding start input at $V_{IN(0)}$ for at least one clock period will initiate a conversion by setting MSB (Q11) at $V_{OUT(0)}$ and all other output (Q10–Q0) at $V_{OUT(1)}$. If set-up time requirements are met, a conversion may be initiated by holding start input at $V_{IN(0)}$ for less than one clock period.

DO: *Serial data output*—D input delayed by one clock period.

NATIONAL

D/A-A/D Products

PRELIMINARY DATA: MARCH 1976

MM4357/MM5357 8-bit A/D converter

general description

The MM4357/MM5357 is an 8-bit monolithic A/D converter using P-channel ion-implanted MOS technology. It contains a high input impedance comparator, 256 series resistors and analog switches, control logic and output latches. Conversion is performed using a successive approximation technique where the unknown analog voltage is compared to the resistor tie points using analog switches. When the appropriate tie point voltage matches the unknown voltage, conversion is complete and the digital outputs contain an 8-bit complementary binary word corresponding to the unknown. The binary output is TRI-STATE to permit bussing on common data lines.

The MM4357 is specified over −55°C to +125°C and the MM5357 is specified over 0°C to +70°C.

features

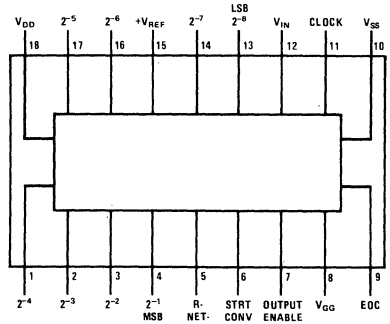
- Low cost
- ±5V, 10V input ranges
- No missing codes
- High input impedance
- Ratiometric conversion
- TRI-STATE outputs
- Fast
- Contains output latches
- TTL compatible

key specs

Resolution	8 bits
Linearity	±1/2 LSB
Conversion speed	40μs
Input impedance	>100 MΩ
Supply voltages	+5V, −12V, GND
Clock range	5.0 kHz to 2.0 MHz

connection diagram

Dual-In-Line Package



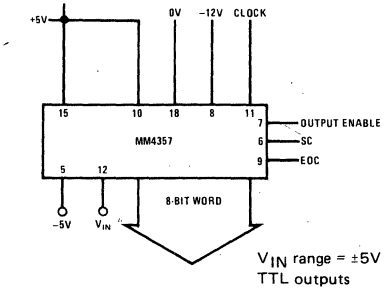
TOP VIEW

Order Part Numbers:

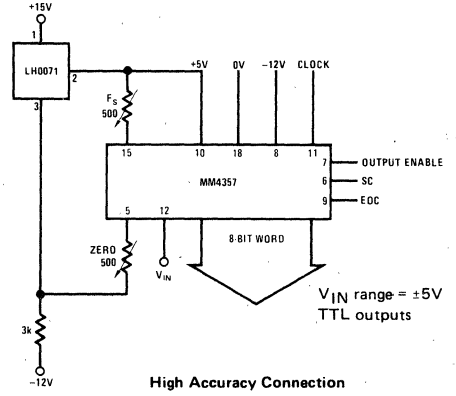
MM4357D
MM4357BD
MM5357D
MM5357BD
MM5357N
MM5357BN

See Packages 26 and 27

typical applications



General Connection



High Accuracy Connection

absolute maximum ratings

Supply Voltage (V_{DD})	V_{SS} − 22V
Supply Voltage (V_{GG})	V_{SS} − 22V
Voltage at Any Input	V_{SS} + 0.3V to V_{SS} − 22V
Operating Temperature	
MM4357/MM4357B	−55°C to +125°C
MM5357/MM5357B	0°C to +70°C
Storage Temperature	150°C
Lead Temperature (Soldering, 10 seconds)	300°C

electrical characteristics (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Nonlinearity (Note 2)	T_A = 25°C, MM4357/MM5357		±1/4	±1/2	LSB
	MM4357/MM5357		±1/2	±1	LSB
	T_A = 25°C, MM4357B/MM5357B		±1/2	±1	LSB
	MM4357B/MM5357B		±1	±2	LSB
Differential Nonlinearity	MM4357/MM5357		±1/8	±1/4	LSB
	MM4357B/MM5357B		±1/4	±1/2	LSB
Quantization Error				±1/2	LSB
Zero Error (Not Adjusted)	T_A = 25°C				
	MM4357/MM5357		±1/2	±1	LSB
	MM4357B/MM5357B		±1	±2	LSB
Zero Error Temperature Coefficient			0.0005	0.001	%/°C
Full Scale Error	T_A = 25°C				
	MM4357/MM5357		±1/2	±1	LSB
	MM4357B/MM5357B		±1	±2	LSB
Full Scale Error Temperature Coefficient			0.0005	0.001	%/°C
Input Impedance		100			MΩ
Power Supply Rejection	15.5V ≤ (V_{SS} − V_{GG}) ≤ 18.5V		0.005	0.01	%/V
Logical "1" Input Voltage	All Inputs	V_{SS}−1.5	V_{SS}−2.5	V_{SS}+0.3	V
Logical "0" Input Voltage	All Inputs	V_{GG}		V_{SS}−4.2	V
Logical Input Leakage	All Inputs, T_A = 25°C, V_{IL} = V_{SS}−10V		0.01	0.5	μA
Logical "1" Output Voltage	All Outputs, I_{OH} = 100μA	2.4	4.5		V
Logical "0" Output Voltage	All Outputs, I_{OL} = 1.6 mA			0.4	V
Disabled Output Leakage	All Outputs, T_A = 25°C, V_{OL} = V_{SS}−10V			2	μA
Minimum Clock Frequency	0°C ≤ T_A ≤ +70°C		5	50	kHz
	−55°C ≤ T_A ≤ +125°C		10	100	kHz
Maximum Clock Frequency	0°C ≤ T_A ≤ +70°C	1000	2000		kHz
	−55° ≤ T_A ≤ +125°C	500	1000		kHz
Clock Pulse Width		500	150		ns
TRI-STATE Enable/Disable Time			500	1000	ns
Conversion Time	T_A = 25°C		20	40	μs
				80	μs
Power Supply Current	T_A = 25°C		10	15	mA
				23	mA
Guaranteed Supply Range	(Note 3)	13		21	V

Note 1: These specifications apply for V_{SS} = +5V, V_{GG} = −12V, and V_{DD} = 0V; over −55°C to +125°C for the MM4357/MM4357B and over 0°C to +70°C for the MM5357/MM5357B unless otherwise specified.

Note 2: This specification is measured with 500Ω potentiometers connected to pins 5 and 15, V_{REF} = 10.00V, and with zero error and full scale error corrected to zero at T_A = 25°C. Temperature specifications apply with no readjustment made in the zero and full scale pots.

Note 3: This specification defines the range over which functional operation is guaranteed.

Note 4: Zero error and full scale error for the MM4357/MM5357 are guaranteed to be adjustable to zero.

OPERATION

The MM4357 contains a network with 256–300Ω resistors in series. Analog switch taps are made at the junction of each resistor and at each end of the network. In operation, a reference (10.00V) is applied across this network of 256 resistors. An analog input (V_{IN}) is first compared to the center point of the ladder via the appropriate switch. If V_{IN} is larger than $V_{REF}/2$, the internal logic changes the switch points and now compares V_{IN} and 3/4 V_{REF}. This process, known as successive approximation, continues until the best match of V_{IN} and V_{REF}/N is made. N now defines a specific tap on the resistor network. When the conversion is complete, the logic loads a binary word corresponding to this tap into the output latch and an end of conversion (EOC) logic level appears. The output latches hold this valid data until a new conversion is completed and new data is loaded into the latches. The data transfer occurs in about 200 ns so that valid data is present virtually all the time.

REFERENCE

The reference applied across the 256 resistor network determines the analog input range. V_{REF} = 10.00V with the top of the reference connected to +5V gives a ±5V range. The reference can be level shifted between V_{SS} and V_{GG}. However, the V_{REF} pin (pin 15) must not exceed V_{SS} and the R network pin (pin 5) must not go below V_{GG} + 5V.

Other reference voltages may be used (such as 10.24V). If a 5V reference is used, the analog range will be 5V and accuracy will be reduced by a factor of 2. Thus, for maximum accuracy it is desireable to operate with at least a 10V reference.

POWER SUPPLIES

Standard supplies are V_{SS} = +5V, V_{GG} = −12V and V_{DD} = 0V. Device accuracy is dependent on stability of the reference voltage and has slight sensitivity to $V_{SS} - V_{GG}$, typically 0.005%/V. V_{DD} has no effect on accuracy.

The output logic levels swing from V_{SS} to V_{DD}. Thus, TTL levels are generated with the standard supplies or CMOS levels occur with V_{SS} = 10V, V_{GG} = −7V and V_{DD} = 0V.

Maximum supply voltage, $V_{SS} - V_{GG}$, is 22V without damage to the device. The maximum operating voltage at which accuracy specs are measured is $V_{SS} - V_{GG}$ = 18.5V. Functional operation is guaranteed over 13V to 21V.

CLOCK

The MM4357 requires a TTL level (referenced to V_{SS}) clock with guaranteed minimum pulse width of 500 ns. Duty cycle is not critical. Conversion time is (1/f) x 40.

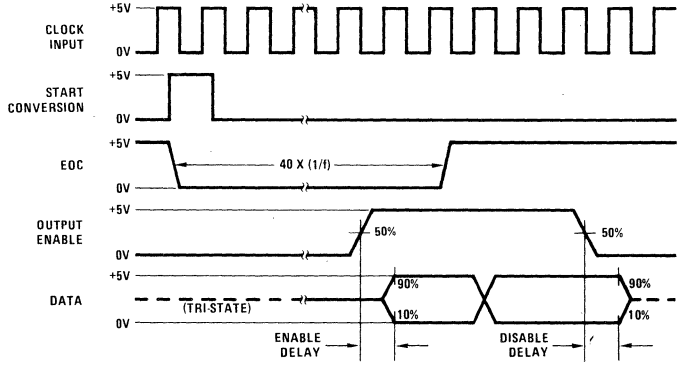
ZERO AND FULL SCALE ADJUSTMENT

In many applications, sufficient accuracy can be obtained by connecting pin 15 directly to the top of the reference. If maximum accuracy is desired, 500Ω pots should be used at both ends of the network and adjusted for zero and full scale.

The top and bottom resistors in the ladder are somewhat less than the nominal 300Ω used throughout the ladder. This permits zero and full scale adjust range with only one pot and no extra supplies. Common practice for zero adjust is to set the transition from 11111111 to 11111110 to occur at 1/2 LSB (20 mV for a 10.24V scale).

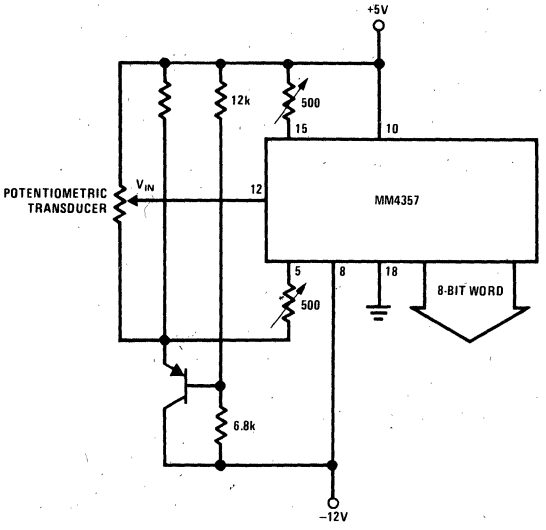
To set full scale, adjust the 500Ω pot on pin 15 until the 00000001 to 00000000 transition occurs 1 1/2 LSB from full scale (60 mV less than full scale for a 10.24V scale).

timing diagram

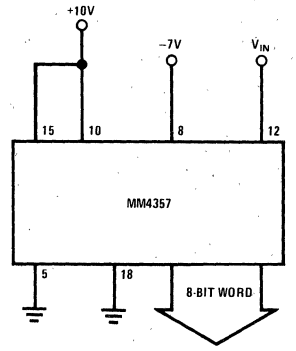


Data is complementary binary (full scale is all "0's" output).

typical applications (con't)

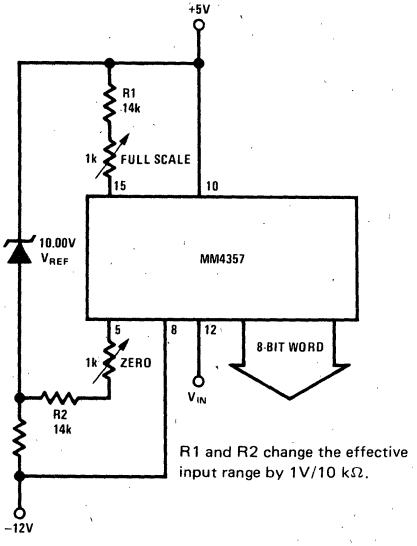


Ratiometric Input Signal with Tracking Reference



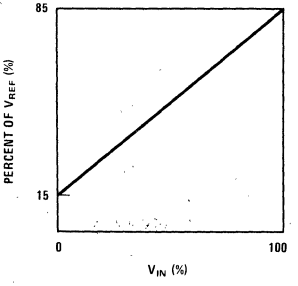
0V to 10V V_{IN} Range
0V to 10V Output Levels

Hi-Voltage CMOS Output Levels



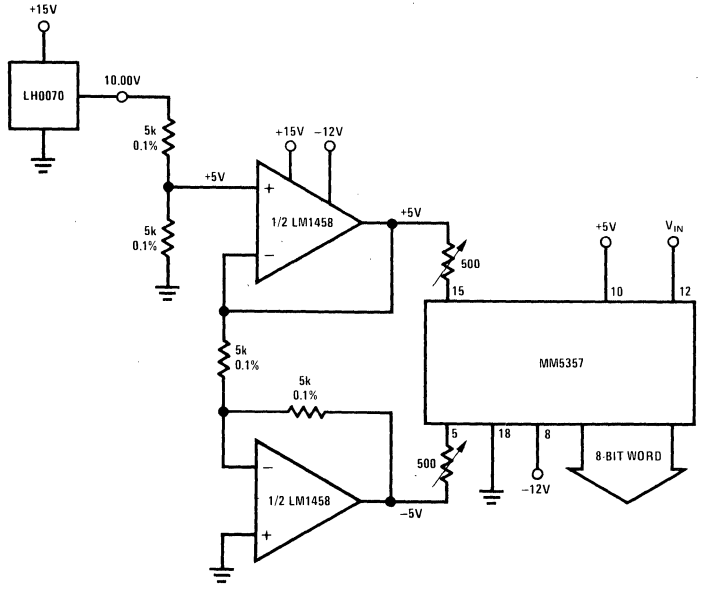
R1 and R2 change the effective input range by 1V/10 kΩ.

Level Shifted Input Signal Range



Level Shifted Zero and Full Scale for Transducers

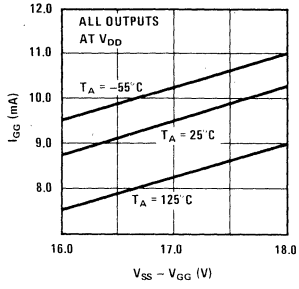
typical applications (con't)



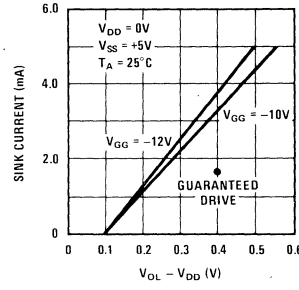
Ground Referenced Input Signal

typical performance characteristics

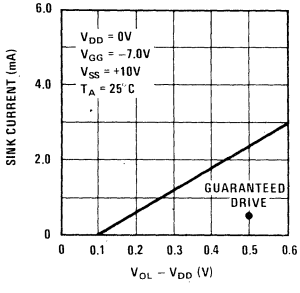
Power Supply Current



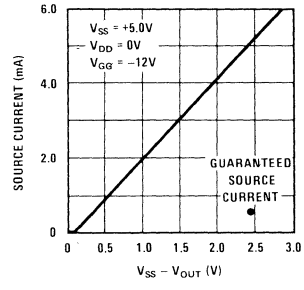
TTL Sink Current



CMOS Sink Current



Source Current



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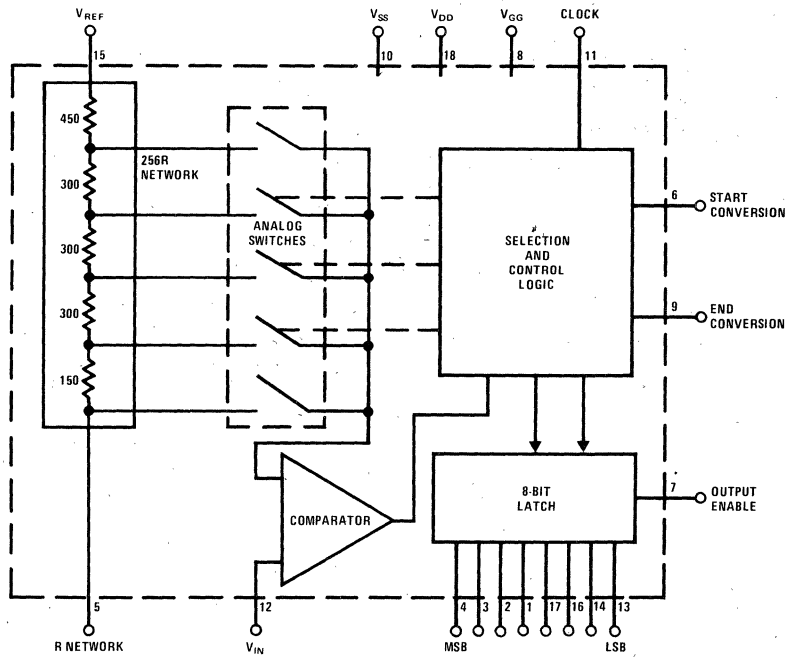
block diagram



NATIONAL

Resistor Arrays

RA07, RA08, RA12, RA13, RA14, RA15 resistor arrays

general description

The RA07, RA08, RA12, RA13, RA14 and RA15 are arrays of 7 to 15 equal value resistors packaged in high reliability Epoxy B dual-in-line packages.

Each array is manufactured using precision automatic laser trimming of high stability thin films. The thin film array is then mounted on a high power dissipation lead frame and molded in the same Epoxy B used for National's semiconductor products. Complete automatic testing and inexpensive Epoxy B packages provide low costs unprecedented in the resistor industry. The RA07, RA08, RA12 and RA14 are symmetrical for goof-proof insertions.

Custom resistor arrays are also available from National. Possible options include unequal values, different configurations and tight tolerances to 0.01%.

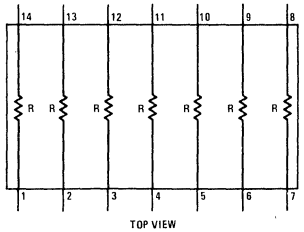
Resistor array applications range from pull-up and pull-down networks to line terminations and LED current limiting.

features

- Low cost
- Six configurations — 7 to 15 Resistors
- Wide resistance range — 22Ω to 100 kΩ
- Tight tolerance — ±2% or ±2Ω, max
- Excellent tracking — 2 ppm/°C
- Four symmetrical configurations

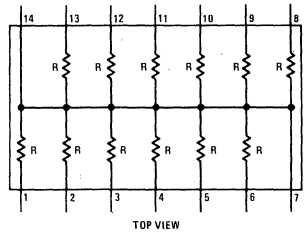
connection diagrams (Dual-In-Line Packages)

RA07



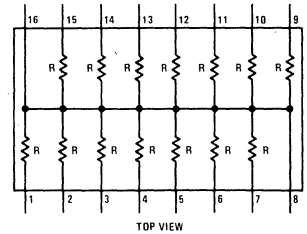
TOP VIEW

RA12



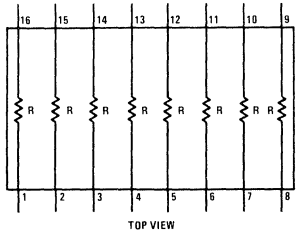
TOP VIEW

RA14



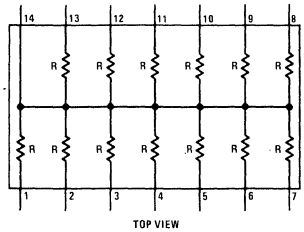
TOP VIEW

RA08



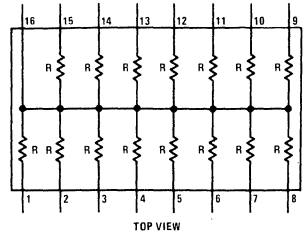
TOP VIEW

RA13



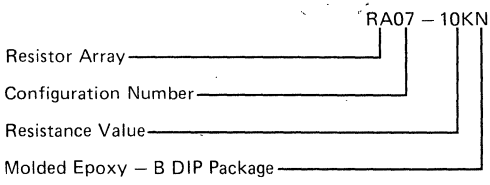
TOP VIEW

RA15



TOP VIEW

ordering information



See Packages 17 and 18

Value Listings

All of these resistance values are available in each array configuration. (All values in ohms):

22	47	100	220	470	1k	2.2k	4.7k	9.1k	20k
24	51	110	240	510	1.1k	2.4k	5.1k	10k	22k
27	56	120	270	560	1.2k	2.7k	5.6k	11k	33k
30	62	130	300	620	1.3k	3k	6k	12k	47k
33	68	150	330	680	1.5k	3.3k	6.2k	13k	68k
36	75	160	360	750	1.6k	3.6k	6.8k	15k	100k
39	82	180	390	820	1.8k	3.9k	7.5k	16k	
43	91	200	430	910	2k	4.3k	8.2k	18k	

Resistance values are ±2% or ±2Ω, whichever is larger.

absolute maximum ratings

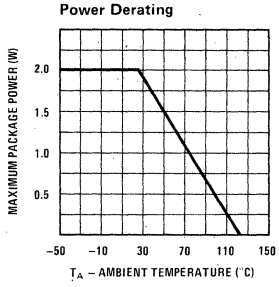
Rated Voltage	(Note 1)
Package Power at 25°C (See curve)	2.0 W
Operating Temperature Range	−55°C to +125°C
Storage Temperature Range	−55°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

electrical characteristics

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Resistor Tolerance	T_A = 25°C		±1	±2 or ±2	% Ω
Resistor Matching	T_A = 25°C		0.2		%
Absolute Tempco	−55°C to +125°C		80		ppm/°C
Matching Tempco	−55°C to +125°C		2		ppm/°C
Resistance Voltage Coefficient			Negligible		μV/V
Overload Resistance Shift	2.5 x rated voltage for 5 seconds, T_A = 25°C			0.5	%
Rise Time			5		ns

Note 1: Rated voltage is determined from maximum package power dissipation and resistance ($P_{MAX} \geq \Sigma \left(\frac{V_i^2}{R_i}\right)$). Maximum power per resistor is 1/4 watt.

typical performance characteristics



NATIONAL

Resistor Arrays

RA24, RA28 resistor termination networks

general description

The RA24 and RA28 are arrays of 24 or 28 resistors designed for use as digital transmission line terminators. The RA24–3k/6.2kN and RA28–3k/6.2kN are specifically tailored for programmable instrumentation terminations per IEEE specification 488-1975 for bus organized peripheral control.

Each array is manufactured using precision automatic laser trimming of high stability thin films. The thin film is then mounted on a high power dissipation lead frame and molded in the same Epoxy B used for National's semiconductor products. Complete automatic testing and inexpensive Epoxy B packages provide low costs unprecedented in the resistor industry.

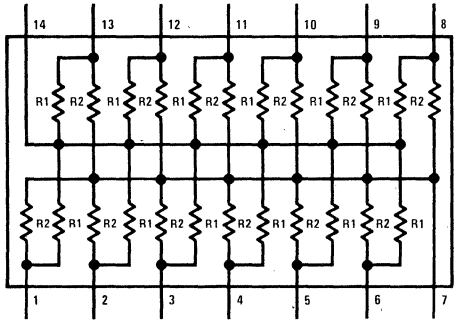
Custom resistor arrays are also available from National. Possible options include unequal values, different configurations and tight tolerances to 0.01%.

features

- Low Cost
- Excellent tracking 2 ppm/°C
- Low inductance

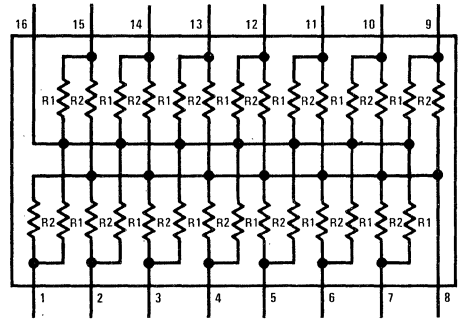
connection diagrams (Dual-In-Line Packages)

RA24



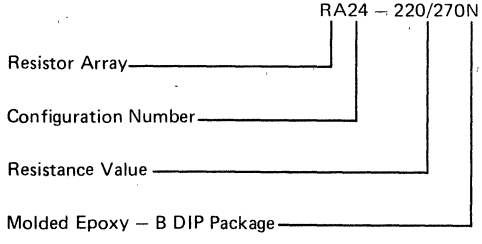
See Package 17

RA28



See Package 18

ordering information



Resistance Values

PART NUMBER	R1	R2
RA24 – 220/270N	220	270
RA24 – 220/330N	220	330
RA24 – 390/500N	390	500
RA24 – 3k/6.2kN	3k	6.2k
RA28 – 220/270N	220	270
RA28 – 220/330N	220	330
RA28 – 390/500N	390	500
RA28 – 3k/6.2kN	3k	6.2k

Resistance tolerance is ±5%.
Values are listed in ohms.

9

absolute maximum ratings

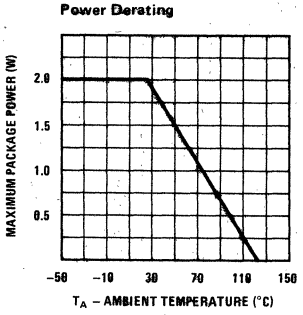
Rated Voltage	(Note 1)
Package Power at 25°C (See curve)	2.0 W
Operating Temperature Range	−55°C to +125°C
Storage Temperature Range	−55°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

electrical characteristics

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Resistor Tolerance	T_A = 25°C		±1	±5	%
Resistor Matching	T_A = 25°C		0.2		%
Absolute Tempco	−55°C to +125°C		80		ppm/°C
Matching Tempco	−55°C to +125°C		2		ppm/°C
Resistance Voltage Coefficient			Negligible		μV/V
Overload Resistance Shift	2.5 x rated voltage for 5 seconds, T_A = 25°C			0.5	%
Rise Time			5		ns

Note 1: Rated voltage is determined from maximum package power dissipation and resistance ($P_{MAX} \geq \Sigma \left(\frac{V_i^2}{R_i}\right)$). Maximum power per resistor is 1/4 watt.

typical performance characteristics



NATIONAL

Active Filters

AF100 universal active filter

general description

The AF100 state variable active filter is a general second order lumped RC network. Only four external resistors program the AF100 for specific second order functions. Lowpass, highpass, and bandpass functions are available simultaneously at separate outputs. Notch and allpass functions are available by summing the outputs in the uncommitted output summing amplifier. Higher order systems are realized by cascading AF100 active filters with appropriate programming resistors.

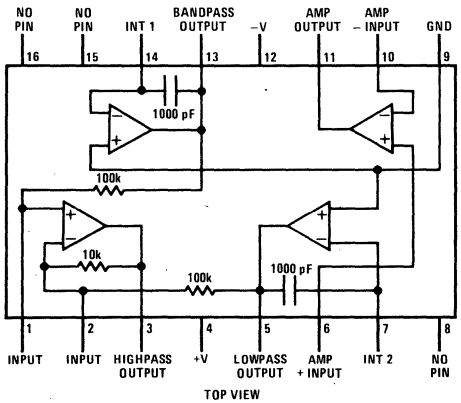
Any of the classical filter configurations, such as Butterworth, Bessel, Cauer, and Chebyshev can be formed.

features

- Military or commercial specifications
- Independent Q, frequency, gain adjustments
- Low sensitivity to external component variation
- Separate lowpass, highpass, bandpass outputs
- Inputs may be differential, inverting, or non-inverting
- Allpass and notch outputs may be formed using uncommitted amplifier
- Operates to 10 kHz
- Q range to 500
- Power supply range ±5V to ±18V
- Frequency accuracy ±1% unadjusted
- Q frequency product $\leq$ 50,000

connection diagrams

Dual-In-Line Package

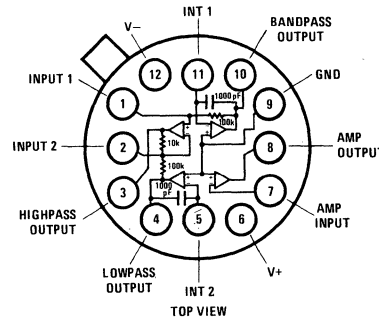


TOP VIEW

Package 24

Order Numbers
AF100-1CJ
AF100-2CJ

Metal Can Package



TOP VIEW

Package 6

Order Numbers
AF100-1CG
AF100-1G
AF100-2CG
AF100-2G

absolute maximum ratings

Supply Voltage	±18V
Power Dissipation	900 mW/Package (500 mW/Amp)
Differential Input Voltage	±36V
Output Short Circuit Duration (Note 1)	Infinite
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Temperature	
AF100-1CJ/AF100-2CJ/AF100-1CG/AF100-2CG	−25°C to +85°C
AF100-1G, AF100-2G	−55°C to +125°C
Storage Temperature	
AF100-1G, AF100-2G, AF100-1CG, AF100-2CG	−65°C to +125°C
AF100-1CJ, AF100-2CJ	−25°C to +100°C

electrical characteristics (Complete Active Filter) (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Frequency Range	$f_C \times Q \leq 50{,}000$			10k	Hz
Q Range	$f_C \times Q \leq 50{,}000$			500	Hz/Hz
f_O Accuracy					
AF100-1, AF100-1C	$f_C \times Q \leq 10{,}000$, $T_A = 25°C$			±2.5	%
AF100-2, AF100-2C	$f_C \times Q \leq 10{,}000$, $T_A = 25°C$			±1.0	%
f_O Temperature Coefficient			±50	±150	ppm/°C
Q Accuracy	$f_C \times Q \leq 10{,}000$, $T_A = 25°C$			±7.5	%
Q Temperature Coefficient			±300	±750	ppm/°C
Power Supply Current	$V_S = ±15V$		2.5	4.5	mA

electrical characteristics (Internal Op Amp) (Note 3)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	$R_S \leq 10\ k\Omega$		1.0	6.0	mV
Input Offset Current			4	50	nA
Input Bias Current			30	200	nA
Input Resistance			2.5		MΩ
Large Signal Voltage Gain	$R_L \geq 2k$ $V_{OUT} = ±10V$	25	160		V/mV
Output Voltage Swing	$R_L = 10\ k\Omega$	±12	±14		V
	$R_L = 2\ k\Omega$	±10	±13		V
Input Voltage Range		±12			V
Common Mode Rejection Ratio	$R_S \leq 10\ k\Omega$	70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10\ k\Omega$	77	96		dB
Output Short Circuit Current			25		mA
Slew Rate (Unity Gain)			0.6		V/μs
Small Signal Bandwidth			1		MHz
Phase Margin			60		Degrees

Note 1: Any of the amplifiers can be shorted to ground indefinitely, however more than one should not be simultaneously shorted as the maximum junction temperature will be exceeded.

Note 2: Specifications apply for $V_S = ±15V$, over −25°C to +85°C for the AF100-1C and AF100-2C and over −55°C to +125°C for the AF100-1 and AF100-2, unless otherwise specified.

Note 3: Specifications apply for $V_S = ±15V$, $T_A = 25°C$.

applications information

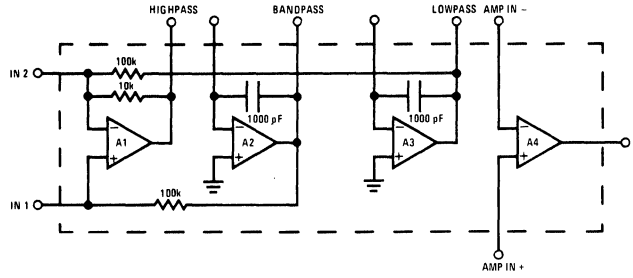


FIGURE 1. AF100 Schematic

CIRCUIT DESCRIPTION AND OPERATION

A schematic of the AF100 is shown in *Figure 1.* Amplifier A1 is a summing amplifier with inputs from integrator A2 to the non-inverting input and integrator A3 to the inverting input. Amplifier A4 is an uncommitted amplifier.

By adding external resistors the circuit can be used to generate the second order system

$$T(s) = \frac{a_3 s^2 + a_2 s + a_1}{s^2 + b_2 s + b_1}$$

The denominator coefficients determine the complex pole pair location and the quality of the poles where

$\omega_0 = \sqrt{b_1}$ = the radian center frequency

$Q = \frac{\omega_0}{b_2}$ = the quality of the complex pole pair

If the output is taken from the output of A1, numerator coefficients a_1 and a_2 equal zero, and the transfer function becomes:

$$T(s) = \frac{a_3 s^2}{s^2 + \frac{\omega_0}{Q} s + \omega_0^2} \qquad \text{(highpass)}$$

If the output is taken from the output of A2, numerator coefficients a_1 and a_3 equal zero and the transfer function becomes:

$$T(s) = \frac{a_2 s}{s^2 + \frac{\omega_0}{Q} s + \omega_0^2} \qquad \text{(bandpass)}$$

If the output is taken from the output of A3, numerator coefficients a_3 and a_2 equal zero and the transfer function becomes:

$$T(s) = \frac{a_1}{s^2 + \frac{\omega_0}{Q} s + \omega_0^2} \qquad \text{(lowpass)}$$

Using proper input and output connections the circuit can also be used to generate the transfer functions for a notch and allpass filter.

In the transfer function for a notch function a_2 becomes zero, a_1 equals 1, and a_3 equals ω_Z^2. The transfer function becomes:

$$T(s) = \frac{s^2 + \omega_Z^2}{s^2 + \frac{\omega_0}{Q} s + \omega_0^2} \qquad \text{(notch)}$$

In the allpass transfer function $a_1 = 1$, $a_2 = -\omega_0/Q$ and $a_3 = \omega_0^2$. The transfer function becomes:

$$T(s) = \frac{s^2 - \frac{\omega_0}{Q} s + \omega_0^2}{s^2 + \frac{\omega_0}{Q} s + \omega_0^2} \qquad \text{(allpass)}$$

COMMON CONFIGURATIONS

The specific transfer functions for some of the most useful circuit configurations using the AF100 are illustrated in *Figures 2 through 8.* Also included are the gain equations for each transfer function in the frequency band of interest, the Q equation, center frequency equation and the Q determining resistor equation.

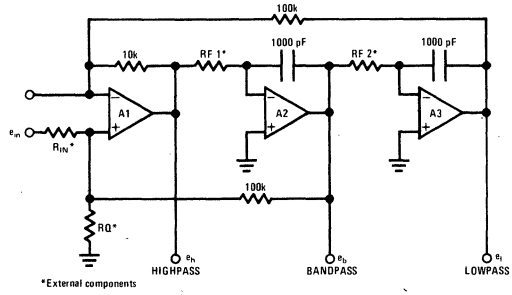


FIGURE 2. Non-inverting Input ($Q > Q_{MIN}$, See Q Tuning Section)

applications information (con't)

a) Non-inverting input *(Figure 2)* transfer equations are:

$$\frac{e_h}{e_{IN}} = \frac{s^2\left[\dfrac{1.1}{1+\dfrac{R_{IN}}{10^5}+\dfrac{R_{IN}}{RQ}}\right]}{\Delta} \quad \text{(highpass)}$$

$$\frac{e_b}{e_{IN}} = \frac{-s\,\omega_1\left[\dfrac{1.1}{1+\dfrac{R_{IN}}{10^5}+\dfrac{R_{IN}}{RQ}}\right]}{\Delta} \quad \text{(bandpass)}$$

$$\frac{e_\ell}{e_{IN}} = \omega_1\omega_2\left[\frac{1.1}{1+\dfrac{R_{IN}}{10^5}+\dfrac{R_{IN}}{RQ}}\right] \quad \text{(lowpass)}$$

$$\omega_1 = \frac{10^9}{R_{F1}} \qquad \omega_2 = \frac{10^9}{R_{F2}}$$

where

$$\Delta = s^2 + s\left[\frac{1.1}{1+\dfrac{10^5}{RQ}+\dfrac{10^5}{R_{IN}}}\right]\omega_1 + 0.1\,\omega_1\omega_2$$

$$\left.\frac{e_\ell}{e_{IN}}\right|_{s\to 0} = \frac{11}{\left(1+\dfrac{R_{IN}}{10^5}+\dfrac{R_{IN}}{RQ}\right)}$$

$$\left.\frac{e_h}{e_{IN}}\right|_{s\to\infty} = \frac{1.1}{\left(1+\dfrac{R_{IN}}{10^5}+\dfrac{R_{IN}}{RQ}\right)}$$

$$\left.\frac{e_b}{e_{IN}}\right|_{\omega=\omega_0} = -\frac{\left(1+\dfrac{10^5}{RQ}+\dfrac{10^5}{R_{IN}}\right)}{\left(1+\dfrac{R_{IN}}{10^5}+\dfrac{R_{IN}}{RQ}\right)}$$

$$\omega_0 = \sqrt{0.1\,\omega_1\omega_2}$$

$$Q = \left(\frac{1+\dfrac{10^5}{R_{IN}}+\dfrac{10^5}{RQ}}{1.1}\right)\sqrt{0.1\left(\frac{\omega_2}{\omega_1}\right)}$$

$$RQ = \frac{10^5}{\left(\dfrac{1.1Q}{\sqrt{0.1\dfrac{\omega_2}{\omega_1}}}\right) - 1 - \dfrac{10^5}{R_{IN}}}$$

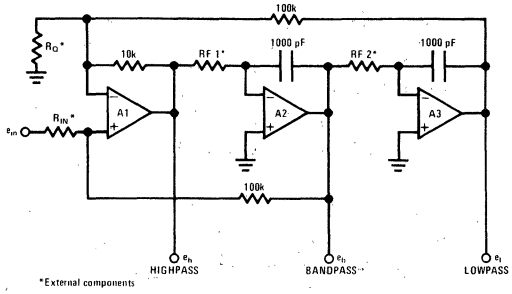


FIGURE 3. Non-Inverting Input (Q < Q_{MIN}, See Q Tuning Section)

b) Non-inverting input *(Figure 3)* transfer equations are:

$$\frac{e_h}{e_{IN}} = \frac{s^2\left[\dfrac{1.1+\dfrac{10^4}{RQ}}{1+\dfrac{R_{IN}}{10^5}}\right]}{\Delta} \quad \text{(highpass)}$$

$$\frac{e_b}{e_{IN}} = \frac{-s\,\omega_1\left[\dfrac{1.1+\dfrac{10^4}{RQ}}{1+\dfrac{R_{IN}}{10^5}}\right]}{\Delta} \quad \text{(bandpass)}$$

$$\frac{e_\ell}{e_{IN}} = \frac{\omega_1\omega_2\left[\dfrac{1.1+\dfrac{10^4}{RQ}}{1+\dfrac{R_{IN}}{10^5}}\right]}{\Delta} \quad \text{(lowpass)}$$

$$\omega_1 = \frac{10^9}{R_{F1}} \qquad \omega_2 = \frac{10^9}{R_{F2}}$$

where

$$\Delta = s^2 + s\,\omega_1\left[\frac{1.1+\dfrac{10^4}{RQ}}{1+\dfrac{10^5}{R_{IN}}}\right] + 0.1\,\omega_1\omega_2$$

$$\left.\frac{e_\ell}{e_{IN}}\right|_{s\to 0} = \frac{1.1+\dfrac{10^4}{RQ}}{0.1\left(1+\dfrac{R_{IN}}{10^5}\right)}$$

$$\left.\frac{e_h}{e_{IN}}\right|_{s\to\infty} = \frac{1.1+\dfrac{10^4}{RQ}}{1+\dfrac{R_{IN}}{10^5}}$$

$$\left.\frac{e_b}{e_{IN}}\right|_{\omega=\omega_0} = -\frac{1+\dfrac{10^5}{R_{IN}}}{1+\dfrac{R_{IN}}{10^5}}$$

$$\omega_0 = \sqrt{0.1\,\omega_1\omega_2}$$

$$Q = \left[\frac{1+\dfrac{10^5}{R_{IN}}}{1.1+\dfrac{10^4}{RQ}}\right]\sqrt{0.1\frac{\omega_2}{\omega_1}}$$

$$RQ = \frac{10^4}{\left(1+\dfrac{10^5}{R_{IN}}\right)\left(\dfrac{\sqrt{0.1\dfrac{\omega_2}{\omega_1}}}{Q}\right) - 1.1}$$

applications information (con't)

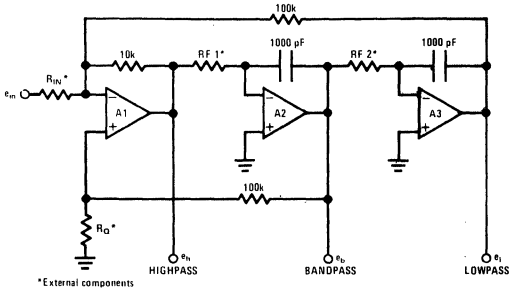


FIGURE 4. Inverting Input

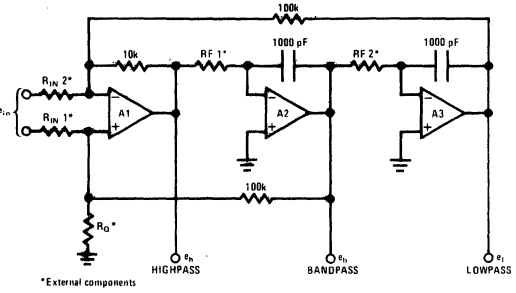


FIGURE 5. Differential Input

c) Inverting input *(Figure 4)* transfer function equations are:

$$\frac{e_h}{e_{IN}} = \frac{-s^2 \dfrac{10^4}{R_{IN}}}{\Delta} \qquad \text{(highpass)}$$

$$\frac{e_b}{e_{IN}} = \frac{s\,\omega_1 \dfrac{10^4}{R_{IN}}}{\Delta} \qquad \text{(bandpass)}$$

$$\frac{e_l}{e_{IN}} = \frac{-\omega_1\,\omega_2 \dfrac{10^4}{R_{IN}}}{\Delta} \qquad \text{(lowpass)}$$

$$\omega_1 = \frac{10^9}{R_{F1}} \qquad \omega_2 = \frac{10^9}{R_{F2}}$$

where

$$\Delta = s^2 + s\,\omega_1 \left[\frac{1.1 + \dfrac{10^4}{R_{IN}}}{1 + \dfrac{10^5}{R_Q}} \right] + 0.1\,\omega_1\omega_2$$

$$\left.\frac{e_l}{e_{IN}}\right|_{s \to 0} = -\frac{10^5}{R_{IN}} \qquad \text{(lowpass)}$$

$$\left.\frac{e_h}{e_{IN}}\right|_{s \to \infty} = -\frac{10^4}{R_{IN}} \qquad \text{(highpass)}$$

$$\left.\frac{e_b}{e_{IN}}\right|_{\omega = \omega_0} = \frac{\dfrac{10^4}{R_{IN}}\left(1 + \dfrac{10^5}{RQ}\right)}{1.1 + \dfrac{10^4}{R_{IN}}} \qquad \text{(bandpass)}$$

$$\omega_0 = \sqrt{0.1\,\omega_1\omega_2}$$

$$Q = \left[\frac{1 + \dfrac{10^5}{RQ}}{1.1 + \dfrac{10^4}{R_{IN}}} \right] \sqrt{0.1\,\frac{\omega_2}{\omega_1}}$$

$$RQ = \frac{10^5}{\dfrac{Q}{\sqrt{0.1\,\dfrac{\omega_2}{\omega_1}}}\left(1.1 + \dfrac{10^4}{R_{IN}}\right) - 1}$$

d) Differential input *(Figure 5)* transfer function equations are:

$$\frac{e_h}{e_{IN}} = \frac{s^2 \dfrac{10^4}{R_{IN2}}}{\Delta} \qquad \text{(highpass)}$$

$$\frac{e_b}{e_{IN}} = \frac{-s\,\omega_1 \dfrac{10^4}{R_{IN2}}}{\Delta} \qquad \text{(bandpass)}$$

$$\frac{e_l}{e_{IN}} = \frac{\omega_1\omega_2 \dfrac{10^4}{R_{IN2}}}{\Delta} \qquad \text{(lowpass)}$$

$$\omega_1 = \frac{10^9}{R_{F1}} \qquad \omega_2 = \frac{10^9}{R_{F2}}$$

where

$$\Delta = s^2 + s\,\omega_1 \left[\frac{1.1 + \dfrac{10^4}{R_{IN2}}}{1 + \dfrac{10^5}{RQ} + \dfrac{10^5}{R_{IN1}}} \right] + 0.1\,\omega_1\omega_2$$

$$\left.\frac{e_l}{e_{IN}}\right|_{s \to 0} = \frac{10^5}{R_{IN2}}$$

$$\left.\frac{e_h}{e_{IN}}\right|_{s \to \infty} = \frac{10^4}{R_{IN2}}$$

$$\left.\frac{e_b}{e_{IN}}\right|_{\omega = \omega_0} = \frac{0.1\left(1 + \dfrac{10^5}{R_{IN1}} + \dfrac{10^5}{RQ}\right)}{\left(1.1 + \dfrac{10^4}{R_{IN2}}\right)}$$

$$Q = \left[\frac{1 + \dfrac{10^5}{RQ} + \dfrac{10^5}{R_{IN1}}}{1.1 + \dfrac{10^4}{R_{IN2}}} \right] \sqrt{0.1\,\frac{\omega_2}{\omega_1}}$$

$$RQ = \frac{10^5}{\dfrac{Q}{\sqrt{0.1\,\dfrac{\omega_2}{\omega_1}}}\left(1.1 + \dfrac{10^4}{R_{IN2}}\right) - 1 - \dfrac{10^5}{R_{IN2}}}$$

applications information (con't)

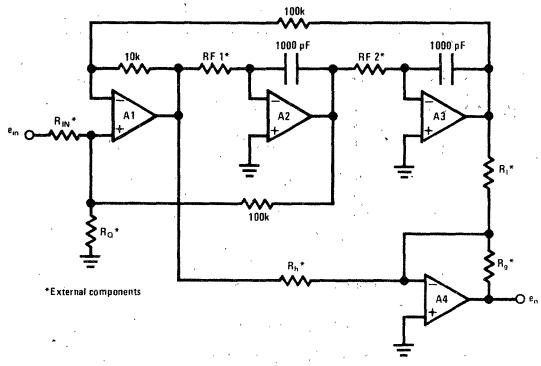


FIGURE 6. Output Notch Using All Four Amplifiers

e) Output notch *(Figure 6)* transfer function equations are:

$$\frac{e_n}{e_{IN}} = \frac{(s^2 + \omega_Z{}^2)\left[\dfrac{1.1}{1 + \dfrac{R_{IN}}{10^5} + \dfrac{R_{IN}}{RQ}}\right]\dfrac{R_g}{R_h}}{s^2 + s\,\omega_1\left[\dfrac{1.1}{1 + \dfrac{10^5}{RQ} + \dfrac{10^5}{R_{IN}}}\right] + 0.1\,\omega_1\omega_2}$$

$$\omega_1 = \frac{10^9}{R_{F1}} \qquad \omega_2 = \frac{10^9}{R_{F2}} \qquad \omega_0 = \sqrt{0.1\,\omega_1\omega_2}$$

$$\omega_Z = \omega_0\sqrt{\frac{10\,R_h}{R_\ell}}$$

$$\left.\frac{e_n}{e_{IN}}\right|_{s \to 0} = \frac{11}{\left(1 + \dfrac{R_{IN}}{10^5} + \dfrac{R_{IN}}{RQ}\right)}\frac{R_g}{R_\ell}$$

$$\left.\frac{e_n}{e_{IN}}\right|_{s \to \infty} = \frac{1.1}{\left(1 + \dfrac{R_{IN}}{10^5} + \dfrac{R_{IN}}{RQ}\right)}\frac{R_g}{R_h}$$

$$\left.\frac{e_n}{e_{IN}}\right|_{\omega = \omega_Z} = 0$$

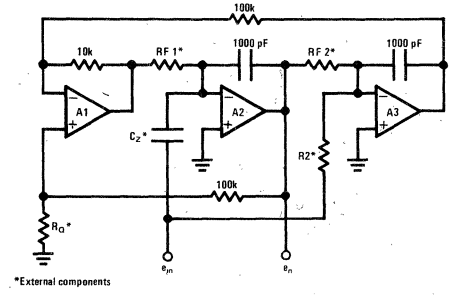


FIGURE 7. Input Notch Using Three Amplifiers

j) Input notch *(Figure 7)* transfer function equations are:

$$\frac{e_n}{e_{IN}} = \frac{\dfrac{10^{-9}}{C_Z}\left[s^2 + \omega_Z{}^2\right]}{s^2 + s\,\omega_1\left[\dfrac{1.1\,RQ}{10^5 + RQ}\right] + \omega_0{}^2}$$

$$\omega_1 = \frac{10^9}{R_{F1}} \qquad \omega_2 = \frac{10^9}{R_{F2}}$$

$$\omega_Z = \omega_0\sqrt{\frac{RF2 \times 10^{-9}}{R_Z\,C_Z}} \qquad \omega_0 = \sqrt{0.1\,\omega_1\omega_2}$$

$$\left.\frac{e_n}{e_{IN}}\right|_{\omega \to 0} = \left(\frac{10^{-9}}{C_Z}\right)^{1/2}\frac{R_Z\,C_Z}{RF2 \times 10^{-9}}$$

$$\left.\frac{e_n}{e_{IN}}\right|_{\omega \to \infty} = \left(\frac{10^{-9}}{C_Z}\right)^{1/2}$$

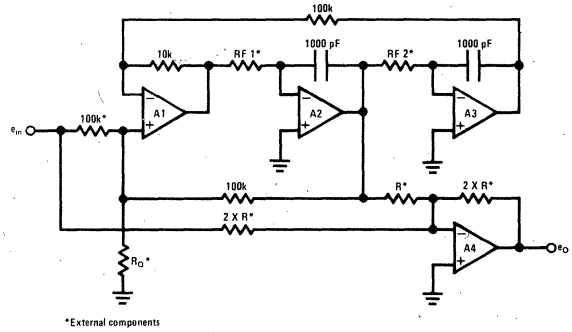


FIGURE 8. Allpass

g) Allpass *(Figure 8)* transfer function equations are:

$$\frac{e_o}{e_{IN}} = -\left[\frac{s^2 - s\,\omega_1\left[\dfrac{1.1}{2 + \dfrac{R_{IN}}{RQ}}\right] + \omega_0{}^2}{s^2 + s\,\omega_1\left[\dfrac{1.1}{2 + \dfrac{R_{IN}}{RQ}}\right] + \omega_0{}^2}\right]$$

$$Q = \frac{2 + \dfrac{10^5}{RQ}}{1.1}\sqrt{0.1\,\frac{\omega_2}{\omega_1}}$$

$$\omega_1 = \frac{10^9}{R_{F1}} \qquad \omega_2 = \frac{10^9}{R_{F2}}$$

$$\omega_0 = \sqrt{0.1\,\omega_1\omega_2}$$

Time delay at $\omega_0 = \dfrac{2Q}{\omega_0}$ seconds

FREQUENCY TUNING

To tune the AF100 two resistors are required for frequencies between 200 Hz and 10 kHz. For lower frequencies "T" tuning or addition of external capacitors

applications information (con't)

is required. Using external capacitors allows the user to go as low in frequency as he desires. "T" tuning and external capacitors can be used together.

Two resistor tuning for 200 Hz to 10 kHz

$$R_f = \frac{50.33 \times 10^6}{f_o}\ \Omega$$

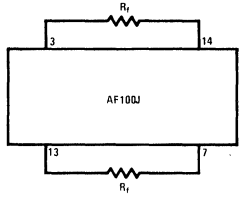
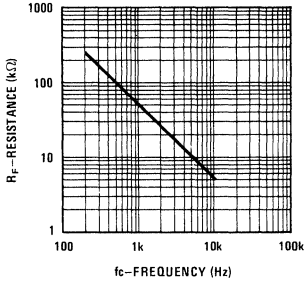


FIGURE 9. Resistive Tuning

GRAPH A. Resistive Tuning



"T" resistive tuning for $f_O < 200$ Hz

$$R_s = \frac{R_t^2}{R_f - 2R_t} \qquad R_t < \frac{R_F}{2}$$

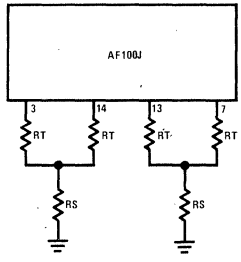
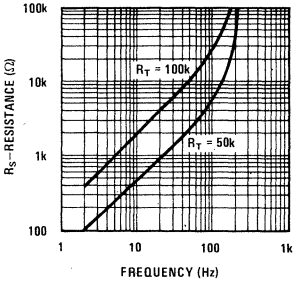


FIGURE 10. T Tuning

GRAPH B. "T" Tuning



RC tuning for $f_O < 200$ Hz

$$R_f = \frac{0.05033}{f_o\ (C + 1 \times 10^{-9})}$$

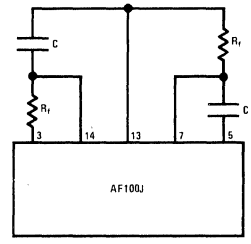
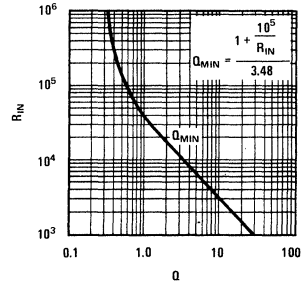


FIGURE 11. Low Frequency RC Tuning

Q TUNING

To tune the Q of an AF100 requires one resistor from pins 1 or 2 to ground. The value of the Q tuning resistor depends on the input connection and input resistance as well as the value of the Q. The Q of the unit is inversely proportional to resistance to ground at pin 1 and directly proportional to resistance to ground from pin 2.

GRAPH C. Q_{MIN}, Non-Inverting Input



For $Q > Q_{MIN}$ in non-inverting mode:

$$RQ = \frac{10^5}{3.48Q - 1 - \frac{10^5}{R_{IN}}}$$

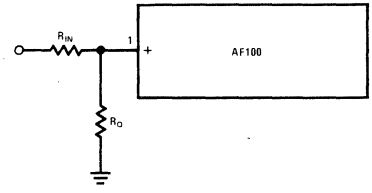
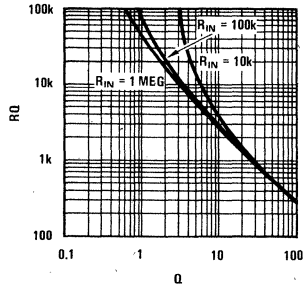


FIGURE 12. Q Tuning for $Q > Q_{MIN}$, Non-Inverting Input

applications information (con't)

GRAPH D. $Q > Q_{MIN}$, Non-Inverting Input



For $Q < Q_{MIN}$ in non-inverting mode:

$$RQ = \frac{10^4}{0.3162 \quad \frac{\left(1 + \frac{10^5}{R_{IN}}\right)}{Q} \quad - 1.1}$$

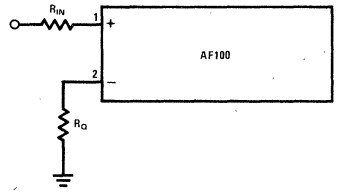
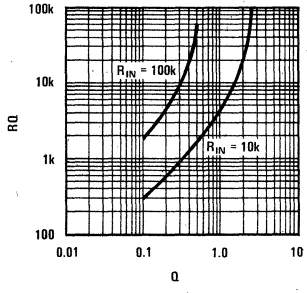


FIGURE 13. Q Tuning for $Q < Q_{MIN}$, Non-Inverting Input

GRAPH E. $Q < Q_{MIN}$, Non-Inverting Input



For any Q in inverting mode:

$$RQ = \frac{10^5}{3.16Q \quad \left(1.1 + \frac{10^4}{R_{IN}}\right) \quad - 1}$$

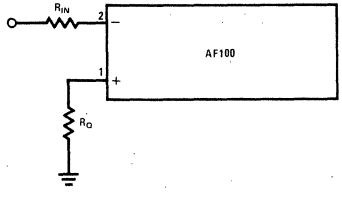
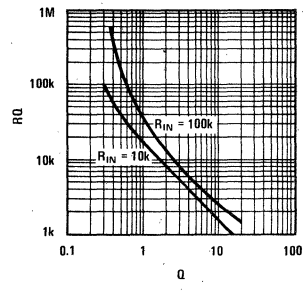


FIGURE 14. Q Tuning Inverting Input

GRAPH F. Q Tuning, Inverting Input



NOTCH TUNING

Two methods to generate notches are the RC input and lowpass/highpass summing. The RC input method requires adding a capacitor and resistor connected to the two integrator inputs. The capacitor connects to "Int 1" and the resistor connects to "Int 2." The output summing requires two resistors connected to the lowpass and highpass output.

For input RC notch tuning:

$$R_Z = C_Z \; R_F \times 10^9 \left(\frac{f_O}{f_Z}\right)^2$$

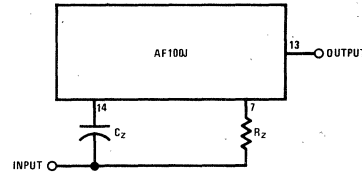
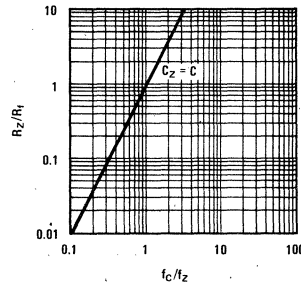


FIGURE 15. Input RC Notch

GRAPH G. Input RC Notch



For output notch tuning:

$$R_{HP} = \left(\frac{f_Z}{f_O}\right)^2 \frac{R_{LP}}{10}$$

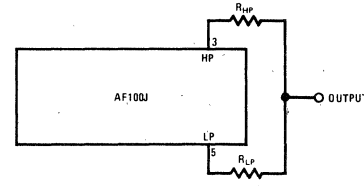


FIGURE 16. Output Notch

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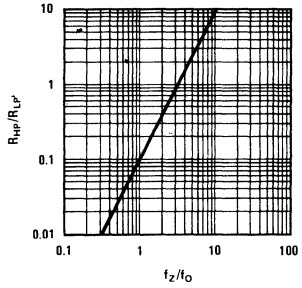
GRAPH H. Output Notch



TUNING TIPS

In applications where 2 to 3% accuracy is not sufficient to provide the required filter response, the AF100 stages can be tuned by adding trim pots or trim resistors in series or parallel with one of the frequency determining resistors and the Q determining resistor.

When tuning a filter section, no matter what output configuration is to be used in the circuit, measurements are made between the input and the bandpass (pin 13) output.

Before any tuning is attempted the lowpass (pin 7) output should be checked to see that the output is not clipping. At the center frequency of the section the lowpass output is 10 dB higher than the bandpass output and 20 dB higher than the highpass. This should be kept in mind because if clipping occurs the results obtained when tuning will be incorrect.

Frequency Tuning

By adjusting the resistance between pins 7 and 13 the center frequency of a section can be adjusted. If the input is through pin 1 the phase shift at center frequency will be 180° and if the input is through pin 2 the phase shift at center frequency will be 0°. Adjusting center frequency by phase is the most accurate but tuning for maximum gain is also correct.

"Q" Tuning

The "Q" is tuned by adjusting the resistance between pin 1 or 2 and ground. Low Q tuning resistors will be from pin 2 to ground ($Q < 0.6$). High Q tuning resistors will be from pin 1 to ground. To tune the Q correctly the signal source must have an output impedance very much lower than the input resistance of the filter since the input resistance affects the Q. The input must be driven through the same resistance the circuit will see to obtain precise adjustment.

The lower 3 dB (45°) frequency, f_L, and the upper 3 dB (45°) frequency, f_H, can be calculated by the following equations:

$$f_H = \left(\frac{1}{2Q} + \sqrt{\left(\frac{1}{2Q}\right)^2 + 1} \right) \times (f_O)$$

where f_O = center frequency

$$f_L = \left(\sqrt{\left(\frac{1}{2Q}\right)^2 + 1} - \frac{1}{2Q} \right) \times (f_O)$$

When adjusting the Q, set the signal source to either f_H or f_L and adjust for 45° phase change or a 3 dB gain change.

Notch Tuning

If a circuit has a jw axis zero pair the notch can be tuned by adjusting the ratio of the summing resistors (lowpass/highpass summing) or the input resistance (input RC).

In either case the signal is connected to the input and the proper resistor is adjusted for a null at the output.

Special Cases

When using the input RC notch the unit cannot be tuned through the normal input so an additional 100k resistor can be added at pin 1 and the unit can be tuned normally. Then the 100k input resistor should be grounded and the notch tuned through the normal RC input.

An alternative way of tuning is to tune using the Q resistor as the input. This requires the Q resistor be lifted from ground and connecting the signal source to the normally grounded end of the Q resistor. This has the problem that when the Q resistor is grounded after tuning, its value is decreased by the output impedance of the source. This technique has the advantage of not requiring an additional resistor.

TUNING PROCEDURE (See *Figure 17*)

Center Frequency Tuning

Set oscillator to center frequency desired for the filter section, adjust amplitude and check that clipping does not occur at the lowpass output pin 5 (AF100J).

Adjust the resistance between pins 13 and 7 until the phase shift between input and bandpass output is 180°.

Q Tuning

Set oscillator to upper or lower 45° frequency (see tuning tips) and tune the Q resistor until the phase shift is 135° (upper 45° frequency) or 225° (lower 45° frequency).

Zero Tuning

Set the oscillator output to the zero frequency and tune the zero resistor for a null at the output of the summing amplifier.

Gain Adjust

Set the oscillator to any desired frequency and the gain can be adjusted by measuring the output of the summing amplifier and adjusting the feedback resistance.

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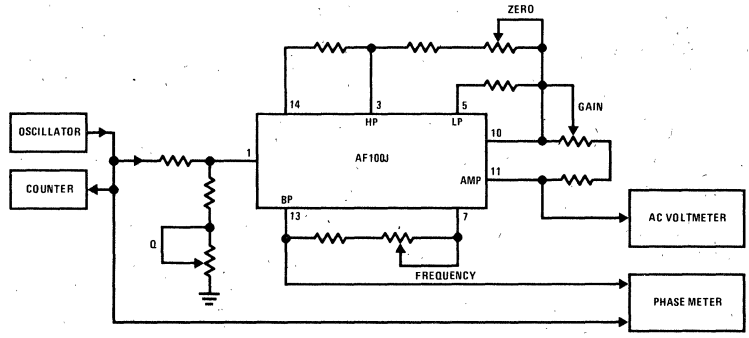


FIGURE 17. Filter Tuning Setup

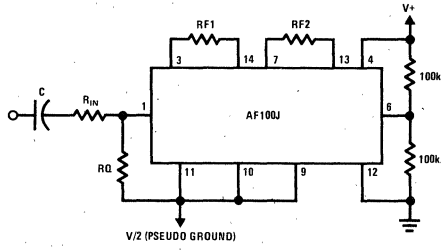


FIGURE 18. Single Power Supply Connection Using Uncommitted Amplifier to Split Supply

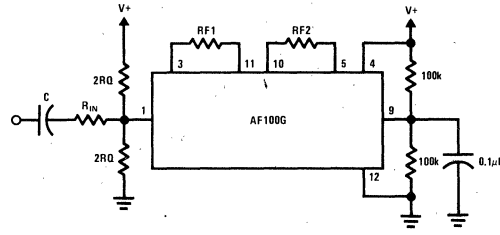
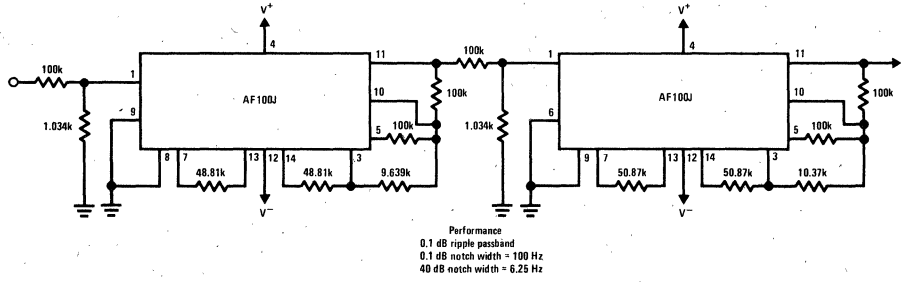


FIGURE 19. Single Power Supply Connection Using Resistive Dividers



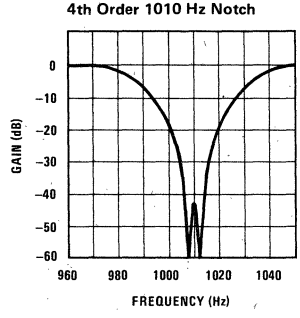


FIGURE 20. 1010 Hz Notch—Telephone Holding Tone Reject Filter

FILTER DESIGN

Since most filter tables are in terms of a normalized lowpass prototype, the filter to be designed is usually reduced to a lowpass prototype. After the lowpass transfer function is found, it is transformed to obtain the transfer function for the actual filter desired. *Graph I* shows the lowpass amplitude response which can be defined by four quantities.

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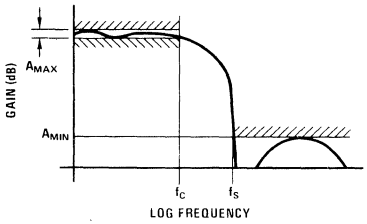
GRAPH I. Lowpass Prototype Response



A_{MAX} = the maximum peak to peak ripple in the passband.

A_{MIN} = the minimum attenuation in the stopband.

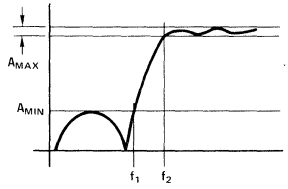
f_C = the passband cutoff frequency.

f_S = the stopband start frequency.

By defining these four quantities for the lowpass prototype the normalized pole and zero locations and the Q (quality) of the poles can be determined from tables or by computer programs.

To obtain the lowpass prototype for the highpass filter (*Graph J*) A_{MAX} and A_{MIN} are the same as for the lowpass case but $f_C = 1/f_2$ and $f_S = 1/f_1$.

GRAPH J. Highpass Response



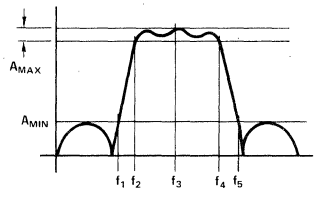
To obtain the lowpass prototype for a bandpass filter (*Graph K*) A_{MAX} and A_{MIN} are the same as for the lowpass case but

$$f_C = 1 \quad f_S = \frac{f_5 - f_1}{f_4 - f_2}$$

where $f_3 = \sqrt{f_1 f_5} = \sqrt{f_2 f_4}$ i.e. geometric symmetry

$f_5 - f_1$ = A_{MIN} bandwidth
$f_4 - f_2$ = Ripple bandwidth

GRAPH K. Bandpass Response

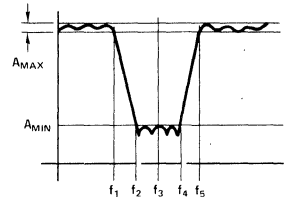


To obtain the lowpass prototype for the notch filter (*Graph L*) A_{MAX} and A_{MIN} are the same as for the lowpass case and

$$f_C = 1 \qquad f_S = \frac{f_5 - f_1}{f_4 - f_2}$$

where $f_3 = \sqrt{f_1 f_5} = \sqrt{f_2 f_4}$

GRAPH L. Notch Response



Normalized Lowpass Transformed To Un-Normalized Lowpass

The normalized lowpass filter has the passband edge normalized to unity. The un-normalized lowpass filter instead has the passband edge at f_C. The normalized and un-normalized lowpass filters are related by the transformation $s = s\omega_c$. This transforms the normalized passband edge $s = j$ to the un-normalized passband edge $s = j\omega_C$.

Normalized Lowpass Transformed To Un-Normalized Highpass

The transformation that can be used for lowpass to highpass is $S = \omega_C/s$. Since S is inversely proportional to s, the low frequency and high frequency responses are interchanged. The normalized lowpass $1/(S^2 + S/Q+1)$ transforms to the un-normalized highpass

$$\frac{s^2}{s^2 + \frac{\omega_C}{Q}s + \omega_C{}^2}$$

Normalized Lowpass Transformed To Un-Normalized Bandpass

The transformation that can be used for lowpass to bandpass is $S = s^2 + \omega_0{}^2/BWs$ where $\omega_0{}^2$ is the center frequency of the desired bandpass filter and BW is the ripple bandwidth.

Normalized Lowpass Transformed To Un-Normalized Bandstop (Or Notch)

The bandstop filter has a reciprocal response to a bandpass filter. Therefore a bandstop filter can be obtained by first transforming the lowpass prototype to a highpass and then performing the bandpass transformation.

SELECTION OF TRANSFER FUNCTION

The selection of a function which approximates the shape of the response desired is a complicated process. Except in the simplest cases it requires the use of tables or computer programs. The form of the transfer function desired is in terms of the pole and zero locations. The most common approximations found in tables are Butterworth, Tschebycheff, Elliptic, and Bessel. The decision as to which approximation to use is usually a function of the requirements and system objectives. Butterworth filters are the simplest but have the disadvantage of requiring high order transfer functions to obtain sharp roll-offs.

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The Tschebycheff function is a min/max approximation in the passband. This approximation has the property that it is equiripple which means that the error oscillates between maximums and minimums of equal amplitude in the passband. The Tschebycheff approximation, because of its equiripple nature, has a much steeper transition region than the Butterworth approximation.

The elliptic filter, also known as Cauer or Zolotarev filters, are equiripple in the passband and stopband and have a steeper transition region than the Butterworth or the Tschebycheff.

For a specific lowpass filter three quantities can be used to determine the degree of the transfer function: the maximum passband ripple, the minimum stopband attenuation, and the transition ratio ($tr = \omega_S/\omega_C$). Decreasing A_{MAX}, increasing A_{MIN}, or decreasing tr will increase the degree of the transfer function. But for the same requirements the elliptic filter will require the lowest order transfer function. Tables and graphs are available in reference books such as "Reference Data for Radio Engineers," Howard W. Sams & Co., Inc., 5th Edition, 1970 and Erich Christian and Egon Eisenmann, "Filter Design Tables and Graphs," John Wiley and Sons, 1966.

For specific transfer functions and their pole locations such text as Louis Weinberg, "Network Analysis and Synthesis," McGraw Hill Book Company, 1962 and Richard W. Daniels, "Approximation Methods for Electronic Filter Design," McGraw-Hill Book Company, 1974, are available.

DESIGN OF CASCADED MULTISECTION FILTERS

The first step in designing is to define the response required and define the performance specifications:

1. Type of filter:
   Lowpass, highpass, bandpass, notch, allpass
2. Attenuation and frequency response
3. Performance
   Center frequency/corner frequency plus tolerance and stability
   Insertion loss/gain plus tolerance and stability
   Source impedance
   Load impedance
   Maximum output noise
   Power consumption
   Power supply voltage
   Dynamic range
   Maximum output level

Second step is to find the pole and zero location for the transfer function which meet the above requirements. This can be done by using tables and graphs or network synthesis. The form of the transfer function which is easiest to convert to a cascaded filter is a product of first and second order terms in these forms:

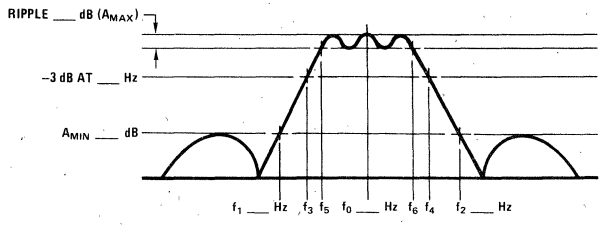
First Order	Second Order	
$\frac{K}{s^2 + \omega_R}$	$\frac{K}{s^2 + \frac{\omega_0}{Q}s + \omega_0{}^2}$	(low pass)
$\frac{Ks}{s + \omega_R}$	$\frac{Ks^2}{s^2 + \frac{\omega_0}{Q}s + \omega_0{}^2}$	(highpass)
	$\frac{Ks}{s^2 + \frac{\omega_0}{Q}s + \omega_0{}^2}$	(bandpass)
	$\frac{K(s^2 + \omega_Z{}^2)}{s^2 + \frac{\omega_0}{Q}s + \omega_0{}^2}$	(notch)
	$\frac{s^2 - \frac{\omega_0}{Q}s + \omega_0{}^2}{s^2 + \frac{\omega_0}{Q}s + \omega_0{}^2}$	(allpass)

Each of the second order functions is realizable by tuning an AF100 stage. By cascading these stages the desired transfer function is realized.

CASCADING SECOND ORDER STAGES

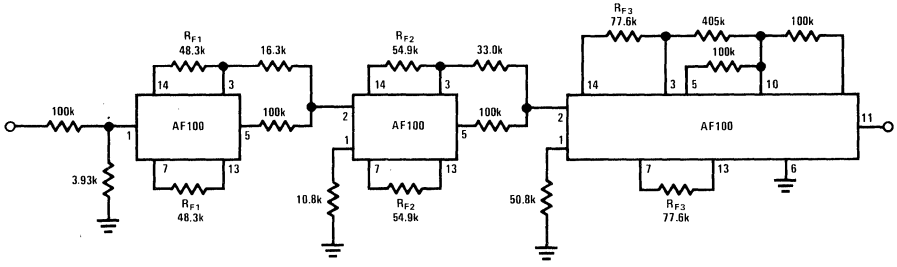
The primary concern in cascading second order stages is to minimize the maximum difference in amplitude from input to output over the frequencies of interest. A computer program is probably required in very complicated cases but some general rules that can be used that will usually give satisfactory results are:

GRAPH M. Generalized Model Response



applications information (con't)

1. The highest "Q" pole pair should be paired with the zero pair closest in frequency.
2. If highpass and lowpass stages are cascaded the lowpass sections should be the higher frequency and highpass sections the lower frequency.
3. In cascaded filters of more than two sections the first section should be the section with "Q" closest to 0.707 and then additional stages should be added in order of least difference between first stage Q and their Q.



Lowpass Elliptic Filter

$F_C = 1$

$F_S = 1.3$

$A_{MAX} = 0.1$ dB

$A_{MIN} = 40$ dB

$N = 6$

$f_{O1} = 1.0415 \quad Q_1 = 7.88 \quad f_{Z1} = 1.329 \quad f_Z/f_O = 1.28 \quad \left(\frac{f_z}{f_o}\right)^2 = 1.63$

$f_{O2} = 0.9165 \quad Q_2 = 1.79 \quad f_{Z2} = 1.664 \quad f_Z/f_O = 1.82 \quad \left(\frac{f_z}{f_o}\right)^2 = 3.30$

$f_{O3} = 0.649 \quad Q_3 = 0.625 \quad f_{Z3} = 4.1285 \quad f_Z/f_O = 6.36 \quad \left(\frac{f_z}{f_o}\right)^2 = 40.5$

$$R_{F1} = \frac{(503.3)}{f_{O1} \times f_C} \times 10^5 \qquad R_{F2} = \frac{(503.3)}{f_{O2} \times f_C} \times 10^5 \qquad R_{F3} = \frac{(503.3)}{f_{O3} \times f_C}$$

at 1000 Hz = f_C

$R_{F1} = 43.3k \qquad R_{F2} = 54.9k \qquad R_{F3} = 77.6k$

6th Order Elliptic Filter

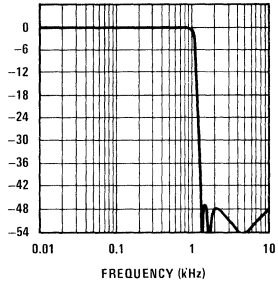
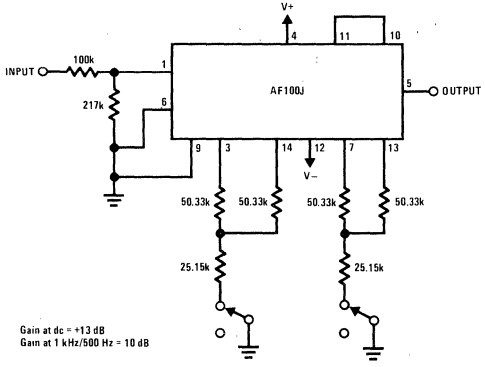


FIGURE 21. Lowpass Elliptic Filter Example



500/1000 Hz Switchable Butterworth Lowpass Filter

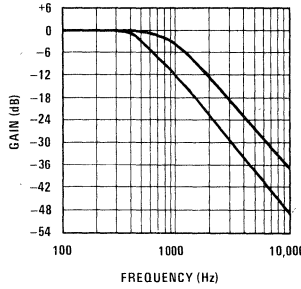
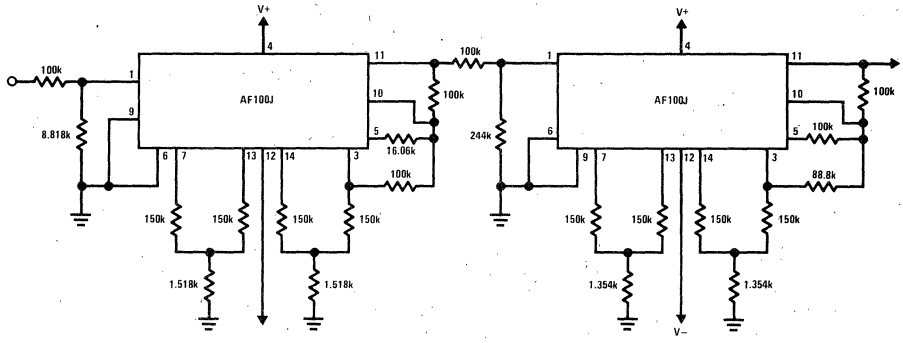


FIGURE 22. Switchable Filter Example: 500 Hz/1000 Hz Butterworth Lowpass

applications information (con't)



EEG Delta Filter

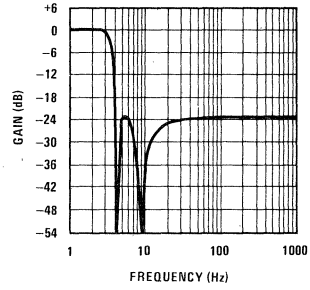


FIGURE 23. EEG Delta Filter–3 Hz Lowpass

Limits and Conditions for Use with Test Circuit

TEST	CONDITION	LIMIT	SWITCH POSITION
f_C	Phase Shift 180°	503.3 Hz ±1%	2
Q	$Q = \frac{f_C}{BW}$ $BW = f_{-45°} - f_{+45°}$	20 ±7.5%	2
A_{HP}	Measured at f_C 2k load	−10 dB ±0.15 dB	1
A_{BP}	Measured at f_C 2k load	0 ±0.15 dB	2
A_{LP}	Measured at f_C 2k load	+10 dB ±0.15 dB	3
A_{AMP}	Measured at f_C 2k load	0 ± 0.1 dB	4
DC Offset	Input Level 0V	±200 mV max	3
Power Supply Current	No Input Signal	4.5 mA max	–

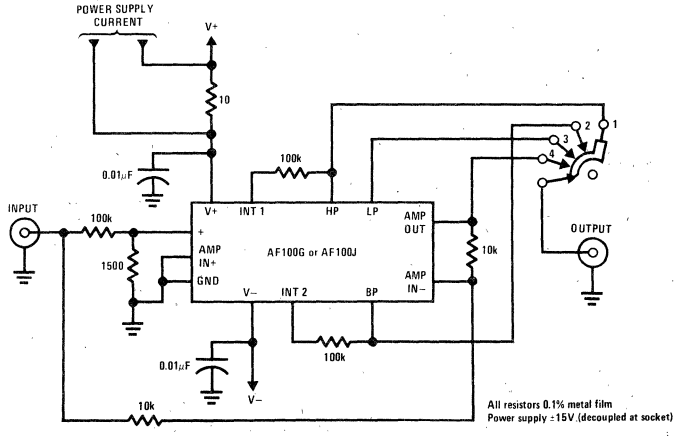


FIGURE 24. Device Test Fixture

applications information (con't)

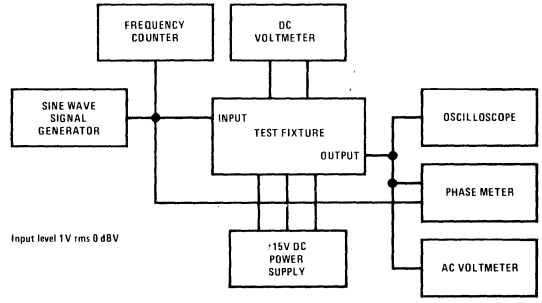


FIGURE 25. Test Circuit Block Diagram

COMPUTER AIDED DESIGN EXAMPLE*

This design is an example of a 60 Hz notch filter. The response is to have the following specifications:

Maximum passband ripple 0.1 dB

Minimum rejection 35 dB

0.1 dB bandwidth 15 Hz max

−35 dB bandwidth 1.5 Hz min

The steps in the design of this filter are:

1. Design a lowpass "prototype" for the filter.
2. Transformation of the lowpass prototype into a notch filter design.
3. Using the pole and zero locations found in step two calculate the value of the resistors required to build the filter.
4. Draw a schematic of filter using values obtained in step three.

*Computer programs shown are user interactive. Underlined copy is user input, non-underlined copy is computer response, and line indications in parenthesis are included for easy identification of data common to several programs.

PROGRAM NO. 1

```
RUN

THIS PROGRAM DESIGNS BUTTERWORTH CHEBYCHEFF OR ELLIPTIC NORMALIZED
LOWPASS FILTERS
WHAT TYPE OF FILTER ? B-C-E

ELLIPTIC
 DO YOU KNOW THE ORDER OF THE FILTER ? Y/N
? NO
INPUT FC,FS,AMAX,AMIN
? 1, 10, .1, 35
     FC                1.000
     FS               10.000
     AMAX               .100
     AMIN             35.000
     N                 2.000
     ATT AT FS       −35.671     (ATTENUATION IN dB)
IS THIS SATISFACTORY ? Y/N
? YES

   F                 Q
    1.823 (Line 1.1)      .775 (Line 1.2)
   Z
   14.124 (Line 1.3)
```

applications information (con't)

PROGRAM NO. 2
(DETERMINES UN-NORMALIZED POLE + ZERO LOCATIONS OF FIRST SECTION)
(DATA ENTERED FROM PROGRAM NO. 1)

```
RUN
WHAT TYPE FILTER BANDPASS OR NOTCH
? NOTCH
ENTER # OF POLE PAIRS? 1

ENTER # OF JW AXIS ZEROS? 1

  ENTER # OF REAL POLES? 0

  ENTER # OF ZEROS AT ZERO? 0

  ENTER # OF COMPLEX ZEROS? 0

ENTER # OF REAL ZEROS? 0

   ENTER F & Q OF EACH POLE PAIR
? 1.823, .775  (FROM LINE 1.1 AND LINE 1.2)

ENTER VALUES OF JW AXIS ZEROS
? 14.124  (FROM LINE 1.3)

ENTER FREQUENCY SCALING FACTOR
? 1
  ENTER THE # OF FILTERS TO BE DESIGNED
? 1
  ENTER THE C.F. AND BW OF EACH FILTER
? 60, 15
```

OUTPUT OF PROGRAM NO. 2
TRANSFORMED POLE/ZERO LOCATIONS
FIRST SECTION

```
                POLE LOCATIONS
  CENTER FREQ.                    Q

 56.93601  (From Line 2.3)     11.31813  (From Line 2.4)
 63.228877 (From Line 2.5)     11.31813  (From Line 2.6)
              JW AXIS ZEROS

 59.471339  (From Line 2.1)
 60.533361  (From Line 22
```

PROGRAM NO. 3
(CHECK OF FILTER RESPONSE USING PROGRAM NO. 2 DATA BASE)

```
RUN

NUMERATOR (ZEROS)
A(I)S^2+R(I)S+Z(I)^2
 1     0     59.471339     (From Line 2.1)
 1     0     60.533361     (From Line 2.2)

REAL POLE

COMPLEX POLE PAIRS

          F          Q
1      56.93601   11.31813   (From Lines 2.3 and 2.4)
2      63.228877  11.31813   (From Lines 2.5 and 2.6)
```

RUN

FREQUENCY	NOR. GAIN (DB)	PHASE	DELAY	NOR. DELAY	FREQUENCY	NOR. GAIN (DB)	PHASE	DELAY	NOR. DELAY
40.000	.032	347.69	.002275	5.847169	60.600	−47.102	169.17	.050801	108.232021
45.000	.060	342.20	.004107	8.749738	60.800	−33.650	165.48	.051677	110.096278
50.000	.100	330.70	.009983	21.268142	61.000	−27.577	161.72	.052809	112.508334
55.000	−.795	290.54	.046620	99.324027	61.200	−23.418	157.87	.054167	115.403169
56.000	−2.298	270.61	.063945	136.234562	61.400	−20.198	153.92	.055712	118.694436
57.000	−5.813	245.51	.072894	155.299278	61.600	−17.554	149.85	.057391	122.270086
58.000	−12.748	220.19	.065758	140.096912	61.800	−15.308	145.65	.059136	125.989157
58.200	−14.740	215.54	.063369	135.006390	62.000	−13.362	141.33	.060869	129.681062
58.400	−17.032	211.06	.060979	129.914831	63.000	−6.557	118.23	.065975	140.559984
58.600	−19.722	206.76	.058692	125.043324	64.000	−2.936	95.30	.059402	126.556312
58.800	−22.983	202.61	.056588	120.561087	65.000	−1.215	76.38	.045424	96.774832
59.000	−27.172	198.60	.054724	116.589928	66.000	−.463	62.43	.032614	69.484716
59.200	−33.235	194.72	.053139	113.212012	67.000	−.138	52.44	.023498	50.062947
59.400	−46.300	190.94	.051856	110.478482	70.000	.091	35.43	.010452	22.267368
59.600	−42.909	7.24	.050888	108.417405	75.000	.085	23.44	.004250	9.054574
59.800	−36.897	3.60	.050242	107.040235	80.000	.060	17.80	.002310	4.921727
60.00	−35.567	360.00	.049916	106.346516	85.000	.043	14.50	.001460	3.110493
60.200	−36.887	356.41	.049907	106.326777	90.000	.032	12.31	.001011	2.154297
60.400	−42.757	352.81	.050206	106.963750					

PROGRAM NO. 4

DESIGN OF FIRST SECTION

```
)RUN
WHICH FILTER AF100 -J OR G ?
? J
WHAT TYPE OF FILTER SECTION? HIGHPASS-BANDPASS-LOWPASS-NOTCH-ALLPASS
? NOTCH
INPUT FC AND Q VALUES
? 56.93601, 11.31813  (FROM LINES 2.3 AND 2.4)
INPUT REAL POLE AND CAPACITOR VALUES IF NONE ENTER 0
? 0
INPUT ZERO LOCATION
? 59.471339      (FROM LINE 2.1)
ARE TUNING INSTRUCTIONS REQUIRED ?
? YES
```

TUNING INSTRUCTION

PHASE SHIFT FROM INPUT TO PIN 13 SHOULD BE 180 DEG. AT 56.93601 HZ.
IF TUNING IS REQUIRED, RF2 FROM PINS 7 TO 13 SHOULD BE ADJUSTED.
PHASE SHIFT FROM INPUT TO PIN 13 SHOULD BE 135 DEG. AT 59.506798HZ.
OR 225 DEG. AT 54.476284 HZ.
IF TUNING IS REQUIRED RQ FROM 1 OR 2 TO GROUND SHOULD BE ADJUSTED
GAIN AT PIN 11 AT 59.471339 SHOULD BE 0 IF NOT
ADJUST RHP FROM PIN 3 TO 10 FOR NULL

FC= 56.93601 Q= 11.31813 F⟨L-3DB⟩ = 54.476284 F⟨H-3DB⟩ = 59.506798

GAIN AT F⟩⟩ FC= .00DB

FUNCTION	CONNECTION FROM	TO	VALUE OF EXTERNAL RESISTORS IN OHMS
R IN	INPUT	1	100000.000
RQ	1	GND	2675.931
RF1	3	14	883960.996
RF2	7	13	883960.996
RLP	5	10	100000.000
RHP	3	10	10910.418
RG	10	11	357910.697
+V		4	
-V		12	
GND		9	
GND		6	
OUTPUT	PIN 11		

applications information (con't)

PROGRAM NO. 4

DESIGN OF SECOND SECTION

WHAT TYPE OF FILTER SECTION? HIGHPASS-BANDPASS-LOWPASS-NOTCH-ALLPASS
? NOTCH
INPUT FC AND Q VALUES
? 63.228877, 11.31813 *(FROM LINES 2.5 AND 2.6)*
INPUT REAL POLE AND CAPACITOR VALUES IF NONE ENTER 0
? 0
INPUT ZERO LOCATION
? 60.533361 *(FROM LINE 2.2)*
ARE TUNING INSTRUCTIONS REQUIRED ?
? YES

TUNING INSTRUCTION

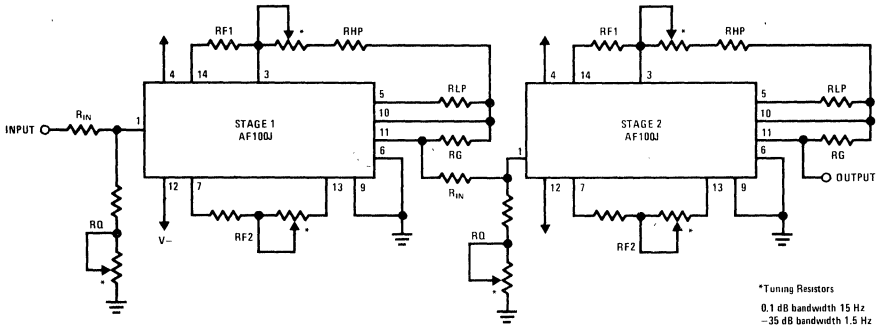
PHASE SHIFT FROM INPUT TO PIN 13 SHOULD BE 180 DEG. AT 63.228877 HZ.
IF TUNING IS REQUIRED RF2 FROM PINS 7 TO 13 SHOULD BE ADJUSTED
PHASE SHIFT FROM INPUT TO PIN 13 SHOULD BE 135 DEG. AT 66.083802 HZ.
OR 225 DEG. AT 60.497289 HZ.
IF TUNING IS REQUIRED RQ FROM 1 OR 2 TO GROUND SHOULD BE ADJUSTED
GAIN AT PIN 11 AT 60.533361 SHOULD BE 0 IF NOT
ADJUST RHP FROM PIN 3 TO 10 FOR NULL

FC= 63.228877 Q= 11.31813 F⟨L-3DB⟩= 60.497289 F⟨H-3DB⟩= 66.083802

GAIN AT F⟨⟨FC= .00DB

FUNCTION	CONNECTION FROM	TO	VALUE OF EXTERNAL RESISTORS IN OHMS
R IN	INPUT	1	100000.000
RQ	1	GND	2675.931
RF1	3	14	795984.596
RF2	7	13	795984.596
RLP	5	10	100000.000
RHP	3	10	9165.552
RG	10	11	328044.920
+V		4	
−V		12	
GND		9	
GND		6	
OUTPUT	PIN 11		

applications information (con't)



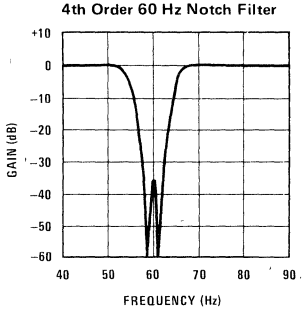


FIGURE 26. Implementation of a 60 Hz Notch From Computer Calculations

TEST PROCEDURE (Ref. *Figure 24*)

Center Frequency

The center frequency is measured by adjusted the signal generator for a 180° phase shift and then reading the input frequency on the counter.

Q

The Q is measured by measuring the bandwidth and dividing into the center frequency. To measure the bandwidth, increase the frequency of the signal generator until the phase shift reads 180°–45° (135°) and read the frequency on the frequency counter. This is $f_{-45°}$. Decrease the frequency of the signal generator until the phase meter reads 180° + 45 (225°) and read the frequency on the frequency counter. This is $f_{+45°}$.

To calculate the Q:

$$Q = \frac{f_O \text{ (center frequency)}}{f_{-45°} - f_{+45°} \text{ (BW)}}$$

Gain

To measure the gain, set the amplitude of the signal generator to 1V RMS (0 dBV) and set the frequency to the center frequency of the filter. Then read the output on the ac voltmeter. The output amplitude at highpass output is −10 dBV ±0.15 dB, which equals 0.316V ±0.006V RMS. The output amplitude at bandpass output is 0 dBV ±0.15 dB, which equals 1.000V ±0.017V RMS. The output amplitude at lowpass output is +10 dBV ±0.15 dB, which equals 3.16V ±0.06V RMS. The output at the amplifier output is 0 dBV ±0.1 dB, which equals 0V ±0.01V RMS.

DC Offset

The dc offset is measured with the DVM connected to the lowpass output by setting the input signal level to zero and reading the DVM.

PS Current

The power supply current is measured by connecting the DVM across a 10Ω resistor in the positive power supply lead with the input level set to zero. The DVM should read less than 45 mV.

applications information (con't)

DEFINITION OF TERMS

A_{MAX}	Maximum passband peak-to-peak ripple
A_{MIN}	Minimum stopband loss
f_Z	Frequency of jw axis pair
f_O	Frequency of complex pole pair
Q	Quality of pole
f_C	Passband edge
f_S	Stopband edge
A_{HP}	Gain from input to highpass output
A_{BP}	Gain from input to bandpass output
A_{LP}	Gain from input to lowpass output
A_{AMP}	Gain from input to output of amplifier
R_f	Pole frequency determining resistance
R_Z	Zero Frequency determining resistance
R_Q	Pole Quality determining resistance
f_H	Frequency above center frequency at which the gain decreases by 3 dB for a bandpass filter
f_L	Frequency below center frequency at which the gain decreases by 3 dB for a bandpass filter
BW	The bandwidth of a bandpass filter
N	Order of the denominator of a transfer function

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NATIONAL

Active Filters

AF120 generalized impedance converter, GIC

general description

The AF120 contains a pair of operational amplifiers and four precision thin film resistors connected as shown below. A gyrator may be formed by adding one external capacitor; or a frequency dependent negative resistance FDNR may be formed by adding two external capacitors. In the gyrator mode, $Z_{IN} \propto j\omega C$, which is equivalent to a grounded inductor. In the FDNR mode, $Z_{IN} \propto -1/\omega^2 C1C2$. The AF120 may also be used in pairs to form ungrounded inductors or inductor networks. Thus, with appropriate transformations, the GIC makes possible an active realization of any low-frequency ladder filter network. The advantage of ladder filters being, of course, that they exhibit lower sensitivity to component variations than any other type of filter realization. Temperature coefficient of the internal resistors is equal and opposite in sign to that of polystyrene capacitors, thus RC products exhibit approximately zero TC.

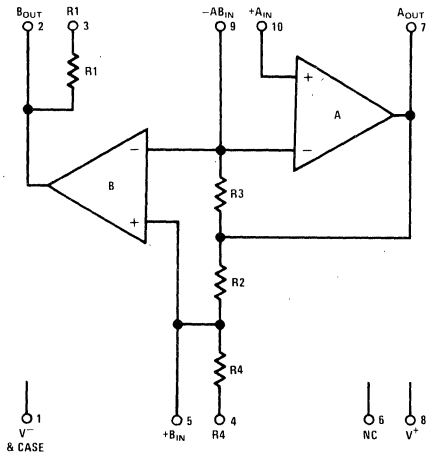
features

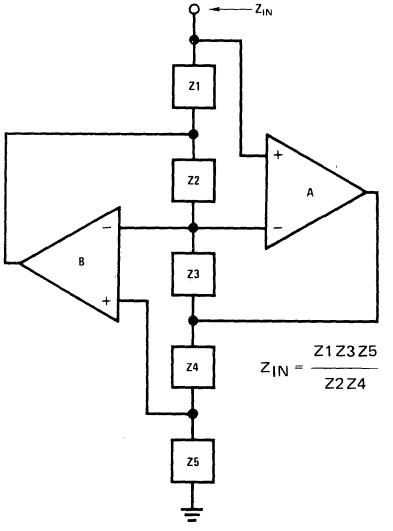
- Matched internal resistors 7500Ω ±0.1%
- Resistor TC = +110 ±30 ppm/°C
- Supply voltage ±5 to ±18V
- Input impedance 7500Ω

applications

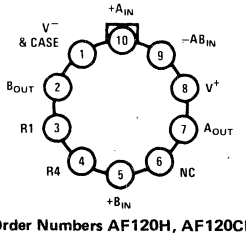
- Gyrator, $Z \propto s$
- Frequency dependent negative resistance, $Z \propto 1/s^2$
- Use in low-frequency active ladder filter networks

schematic and connection diagrams





TO-100
Metal Can Package



Order Numbers AF120H, AF120CH
See Package 10

absolute maximum ratings

Supply Voltage, V_S	±18V
Power Dissipation, T_A = 25°C	500 mW
Derate 18 mW/°C above 60°C	
Operating Temperature, T_A	
AF120	−55°C to +125°C
AF120C	−25°C to +85°C
Storage Temperature, T_{STG}	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

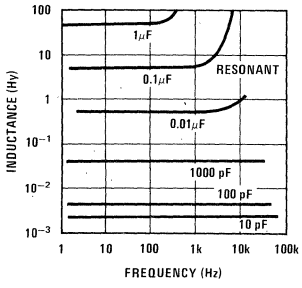
electrical characteristics T_A = 25°C, V_S = ±5 to ±15V, except as noted

PARAMETER		CONDITIONS	AF120			AF120C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
$\|Z_{IN}\|$	Input Impedance		7425	7500	7575	7350	7500	7650	Ω
θ	Phase (Note 1)	*(Figure 1)*	89.5	90	90.5	89	90	91	DEG.
V_{OS}	DC Voltage measured at Input Terminal			1	8		1	10	mV
	R1, R2, R3, R4		7485	7500	7515	7470	7500	7530	Ω
	R2/R3		0.999	1.000	1.001	0.998	1.000	1.002	
TC	Resistor Temp. Coeff.		80	110	140	50	110	170	ppm/°C
V_O	Op Amp Output Voltage	V_S = ±15V, R_L = 2k	±10	±13		±10	±13		V
I_{SC}	Op Amp Short-Circuit Output Current	V_S = ±15V		20			20		mA
I_S	Supply Current	V_S = ±15V		3	5.6		3	5.6	mA

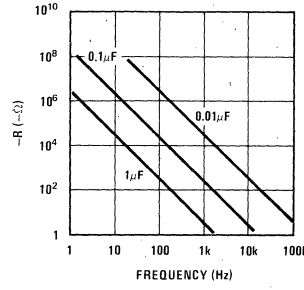
Note 1: 90° indicates that connection actually simulates a pure inductor.

typical performance characteristics

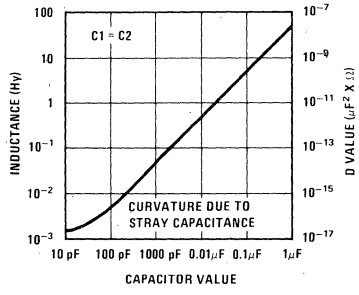
Equivalent Inductance vs Frequency



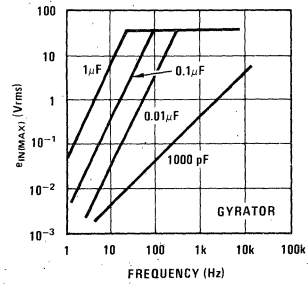
FDNR Value vs Frequency



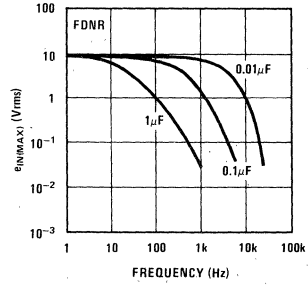
Equivalent L and D vs Capacitor Values



Maximum Terminal Voltage vs Frequency



Maximum Terminal Voltage vs Frequency



applications information

The generalized impedance converter GIC is a versatile tool for realization of inductive components in low-sensitivity filters. The driving point impedance is $Z_i(s) = k(s)\ Z_L(s)$. The input impedance of the AF120 is

$$Z_i = \frac{Z1\,Z3\,Z5}{Z2\,Z4} \quad \text{(Refer to } \textit{Figure 2}\text{)}$$

which reduces to

$$Z_i = \frac{Z1\,Z5}{Z2}$$

since Z3 = R3, Z4 = R2 and R2 = R3. No more than one or two of Z1, Z2 and Z5 may be external capacitors. Internal resistor R4 is available for use as Z5, and internal resistor R1 may be used as either Z1 or Z2. External resistors of other values may be substituted for R1 or R4 if proper attention is paid to temperature coefficients. The TC of internal resistors is +110 ±30 ppm/°C to compensate for the TC of polystyrene capacitors.

The AF120 may be used for the following impedance conversions:

Positive impedance converter (PIC) – k(s) is positive and real

$$Z2 = R1,\ Z5 = R4,\ k = R4/R1 = +1,$$

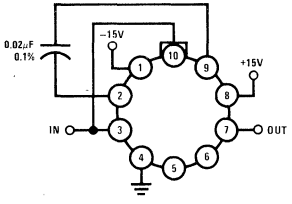
$$Z_i(\omega) = Z1(\omega) \quad \text{(trivial case)}$$

Positive impedance inverter (PII) – k(s) is positive and real

$$Z1 = R1,\ Z5 = R4,\ k = R1\,R4 = (7500)^2$$

$$Z_i(\omega) = R1\,R4/Z2(\omega)$$

If Z2 is an external capacitor, then $Z_i\ (\omega) = R1\,R2j\omega C$, and $Z_i(s) \propto (s)$



$V_{IN} \leq 1Vrms$ @ 1053 Hz

FIGURE 1. Test Circuit

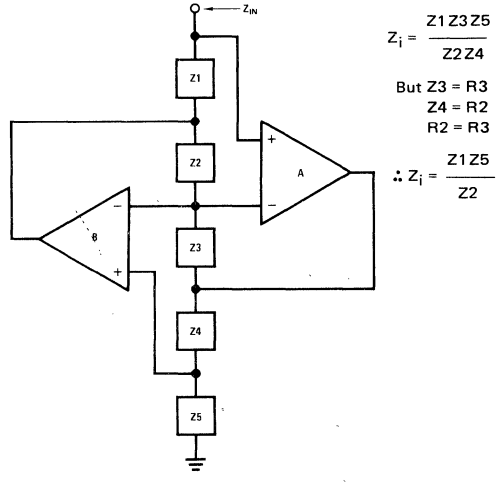


FIGURE 2. GIC Circuit

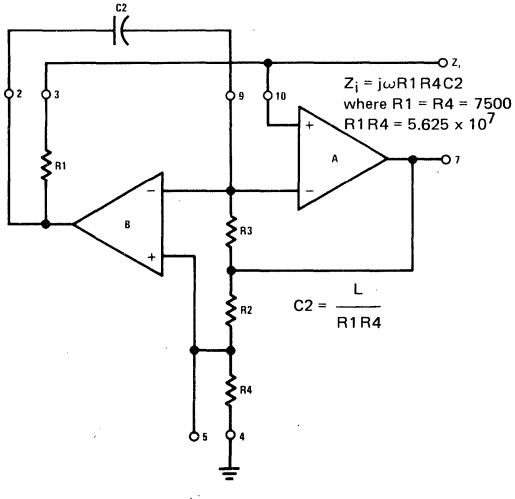


FIGURE 3. Gyrator (Inductive Element)

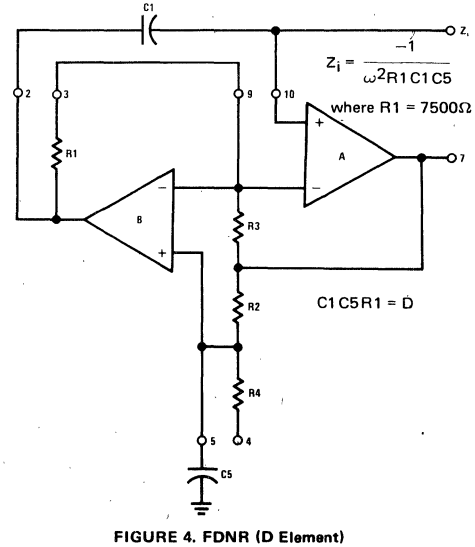
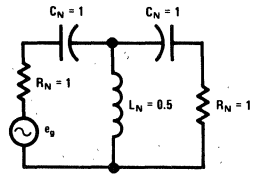
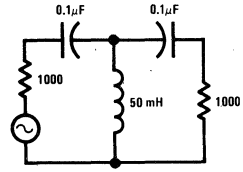


FIGURE 4. FDNR (D Element)

applications information (con't)

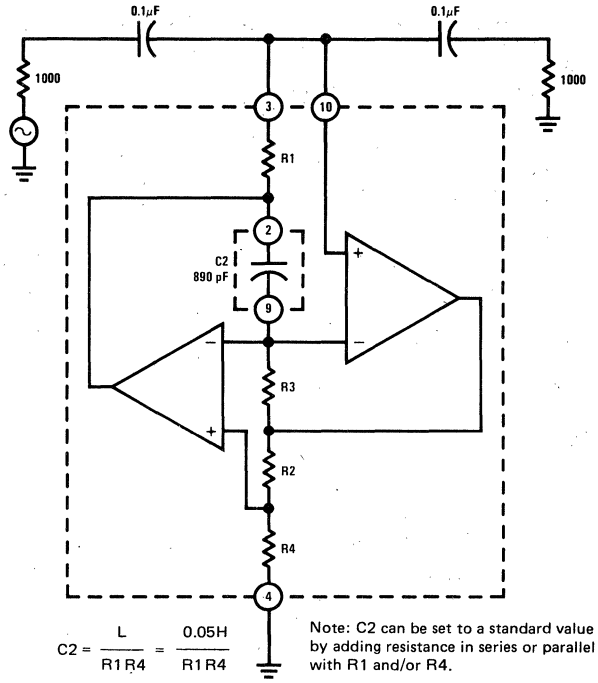


(a) Prototype



$R0 = 1\ k\Omega$
$f_c = 1590\ Hz$
$\omega_c = 10^4$

(b) Filter after Frequency and Impedance Transformation



$$C2 = \frac{L}{R1\,R4} = \frac{0.05H}{R1\,R4}$$

Note: C2 can be set to a standard value by adding resistance in series or parallel with R1 and/or R4.

(c) GIC Active Realization

FIGURE 5. Third-Order Butterworth Highpass Filter

Frequency dependent negative resistance (FDNR)

$$Z2 = R1,\ k = 1/R1$$
$$Z_i = Z1(\omega)Z5(\omega)/R1$$

If Z1 and Z5 are both external capacitors, then $Z_i = -1/R1\omega^2C1C5$, and $Z_i(s) \propto -1/s^2$

GIC elements are especially useful for active simulation of low-sensitivity passive ladder filters. Symmetrically terminated ladder filters exhibit an exceptionally low sensitivity to changes in network element value; in fact, they exhibit the lowest sensitivity of any filter type. This means that practical realization of multistage filter functions may be achieved with moderate tolerance components, and that component shifts due to temperature variations will have minimal effect on the filter transfer function. Additionally, a great deal of ladder filter design information exists in handbook form; hence the value of the GIC as a network element. Several examples are given on the following pages for the realization of filters with grounded inductors, with ungrounded inductors, and with both grounded and ungrounded inductors.

Highpass Filter (with Grounded Inductors)

Figure 5 shows the development of the GIC active realization of the prototype ladder filter of *Figure 5(a)*. The network is first designed with normalized values for all components. Next, the component values are transformed according to the desired characteristic impedance and cutoff frequency of the filter. To transform from prototype normalized values where R0 = 1 and $\omega_c = 1$,

$$\left.\begin{array}{l}\text{Multiply all R and L by R0}\\ \text{Divide all C by R0}\\ \text{Divide all L and C by } \omega_c\end{array}\right\} \text{ to obtain } \left\{\begin{array}{l}R = R0\,R_N\\ L = R0\,L_N/\omega_c\\ C = C_N/R0\omega_c\end{array}\right.$$

where N subscripts indicate original normalized values.

Lowpass Filter (with Ungrounded Inductors)

Since the simple GIC realization of an inductor results only in a grounded inductor, a network transformation is necessary in order to use the GIC in a lowpass filter. *Figure 6* shows the frequency and impedance transformation of the prototype lowpass filter, followed by a 1/s impedance transformation. When this 1/s transformation is made, the performance of the filter is unchanged, therefore the transformation is valid. The

applications information (con't)

resultant circuit shown in *Figure 6(c)* allows the realization of the prototype ungrounded inductor circuit with a grounded D element (FDNR). To make the 1/s transformation, each impedance is multiplied by 1/s so that

each R is replaced by a $C = 1/\omega_c R$,

each L is replaced by an $R = \omega_c L$, and

each C is replaced by a $D = C/\omega_c$.

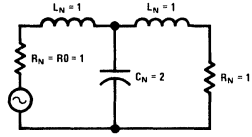
Examination of the GIC realization of an FDNR in *Figure 4* will reveal that a resistive path from FDNR terminal 10 must exist to ground in order to supply bias current to the internal amplifiers. The circuit of *Figure 6(c)* is, therefore, incomplete as no resistive path exists from D element to ground. If a large R were shunted across D, that R would appear in *Figure 6(b)* as an inductor across the C. The solution is to place large R's across the C's in *Figure 6(c)* which appear as large inductors across R0 of *Figure 6(b)*, and thus do not significantly affect the transfer function except near $\omega = 0$. The resultant network appears in *Figure 6(d)*. The transfer function at $\omega = 0$ is $T(0) = 0.5$, therefore resistors R_A and R_B must be chosen to affect this value. Then $T(0) = 0.5 = R_B/(R_A + R_B + 2R0)$.

The GIC realization of the lowpass filter, complete with low-frequency compensation appears in *Figure 6(e)*. Note again, that C1 and C5 can be varied or can be unequal just so long as C1C5R1 = D. Also note that in the final transformation of *Figure 6(c)*

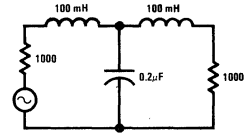
$D = C_N/\omega_c{}^2 R0$

$R = R0 L_N$

$C = 1/\omega_c R0 R_N$

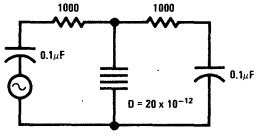


(a) Prototype

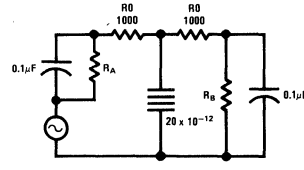


$R0 = 1\ k\Omega$
$f_c = 1590\ Hz$
$\omega_c = 10^4$

(b) Filter after Frequency and Impedance Transformation

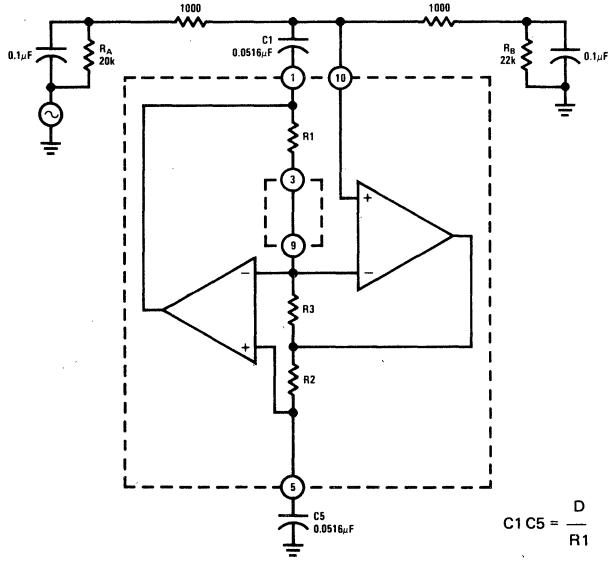


(c) Filter after 1/s Transformation



$R_A, R_B >> R0$
$R_B = R_A + 2R0$

(d) Final Circuit with Low-Frequency Compensation



$C1\,C5 = \frac{D}{R1}$

(e). Active Realization

FIGURE 6. Third-Order Butterworth Lowpass Filter

applications information (con't)

GIC Embedding

Ungrounded inductors may be simulated by embedding an ungrounded resistor between two GIC's as shown in *Figure 7(a)*. Actually, the embedded element may be any 2 or 3-terminal network and the GIC may be given any of its realizable impedance transformations Z(s), $Z(s^{-2})$, $Z(s^{-1})$ or $Z(s^2)$*.

Bandpass Filter (with Grounded and Ungrounded Inductors)

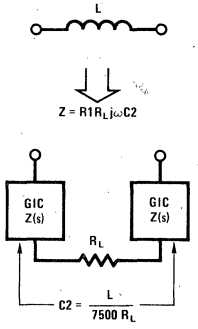
Direct RC active simulation of this filter requires the use of GIC embedding techniques (as described above) because there is no transformation which will eliminate all ungrounded L or D elements. *Figure 8* shows the step-by-step realization of a 6-pole Butterworth bandpass filter.

The filter circuit of *Figure 8(c)* constructed with AF120 and with R and C values shown performed as indicated in the plot of *Figure 9*. Note that the band center and cutoff frequencies occur at the design points as indicated by the phase measurements at 0°C and ±135°C.

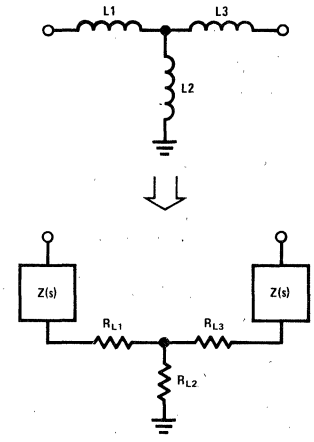
The circuit of *Figure 8(c)* is simplified with a shorthand notation for the GIC's. This shorthand circuit is equivalent to the GIC as shown in *Figure 10*.

The final circuit for the bandpass filter of *Figure 8* contains six capacitors, one for each pole of the 6-pole network. This circuit then contains a minimum number of reactive elements to satisfy the prototype design. A dc path to ground exists for all GIC elements in this design so no additional resistors are needed for dc compensation. Note also that even though one and two percent components have been used throughout the circuit and the $C_D C_C$ product is in error by 3%, performance is as designed. It should be clear from this exercise that ladder networks of virtually any complexity may be realized using the AF120 GIC circuit.

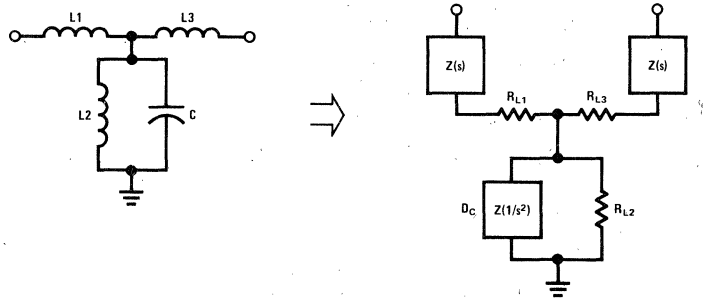
*$Z(s^2)$ is not realizable with the AF120.



(a) Ungrounded Inductor



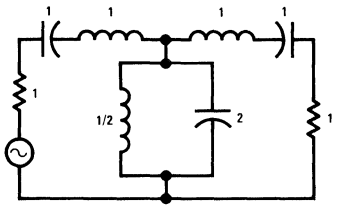
(b) Grounded T Network



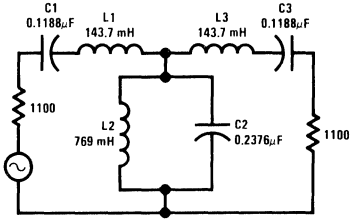
(c). GIC Realization of Complex T Network

FIGURE 7. GIC Realization of Ungrounded Inductors and T Networks

applications information (con't)

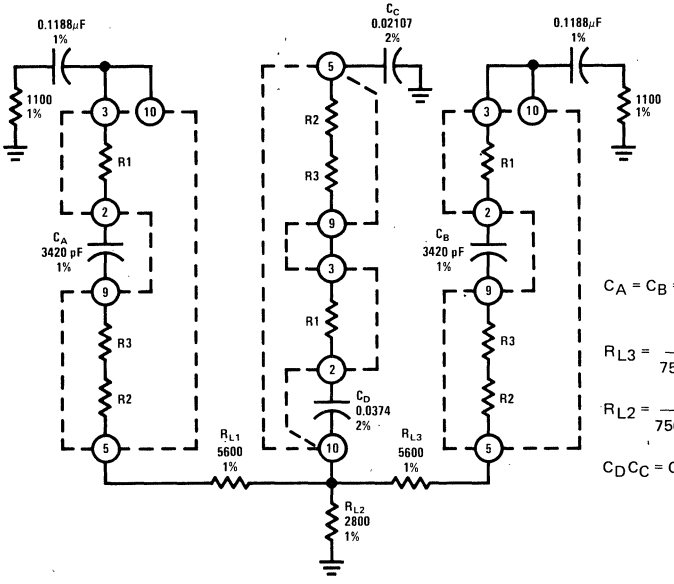


(a) Prototype



$R0 = 1100\Omega$
$f_O = 1218$ Hz
$f_L = 752.8$ Hz
$f_H = 1970.8$ Hz

(b) Filter after R0 and ω0 Transformations



$$C_A = C_B = \frac{L1}{7500\ R_{L1}} = 3420\ pF$$

$$R_{L3} = \frac{L3}{7500\ C_A} = 5600\Omega$$

$$R_{L2} = \frac{L2}{7500\ C_A} = 2800\Omega$$

$$C_D C_C = C_A C2 = 812 \times 10^{-6}\mu F^2$$

(c) GIC Realization

FIGURE 8. 6-Pole Butterworth Bandpass Filter

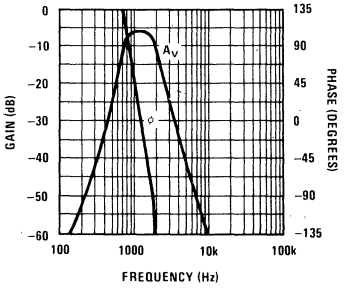
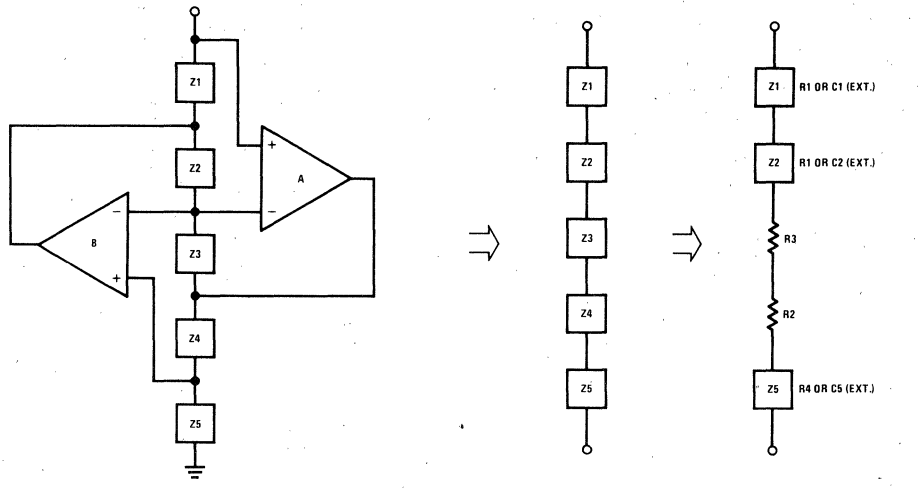


FIGURE 9. Gain and Phase Transfer Functions of the Filter of Figure 8(c).

applications information (con't)



(a) GIC (b) Shorthand Circuit (c) Short Circuit for AF120

FIGURE 10. Development of GIC Shorthand Circuit

NATIONAL

AD1200 low cost 12-bit A/D converter building block

general description

The AD1200 is a 12-bit binary analog building block designed for use with a successive approximation register to build a fast A/D converter. It includes 12 precision current sources and switches, precision laser-trimmed thin film ladder network, precision reference, and high speed FET comparator. The AD1200 is specifically tailored to match the DM2502/DM2503/DM2504 or MM54C905/MM74C905.

The AD1200 comes in a 24-pin plastic DIP and 24-pin metal DIP. The AD1200A and AD1200C have 0.01% ±1/2 LSB accuracy; the AD1200B and AD1200D have 0.05% ±1/2 LSB accuracy.

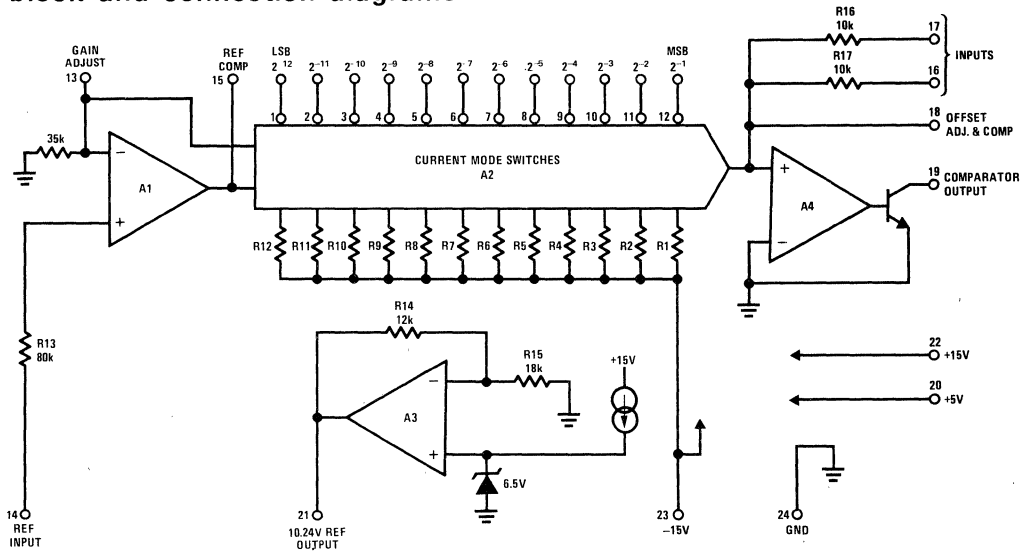
features

- Low cost
- Internal reference and FET comparator
- TTL, DTL, CMOS logic levels
- Standard power supplies ±15V, +5V

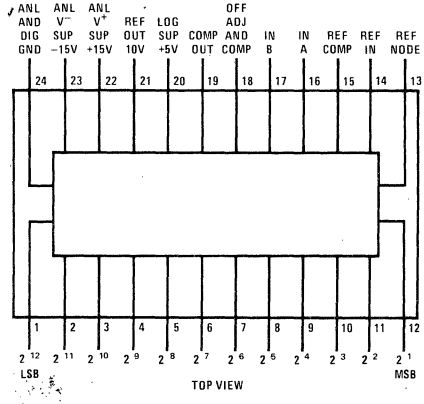
key specifications

- Resolution 12 bits
- Accuracy 0.01% ±1/2 LSB
- Conversion speed 15μs

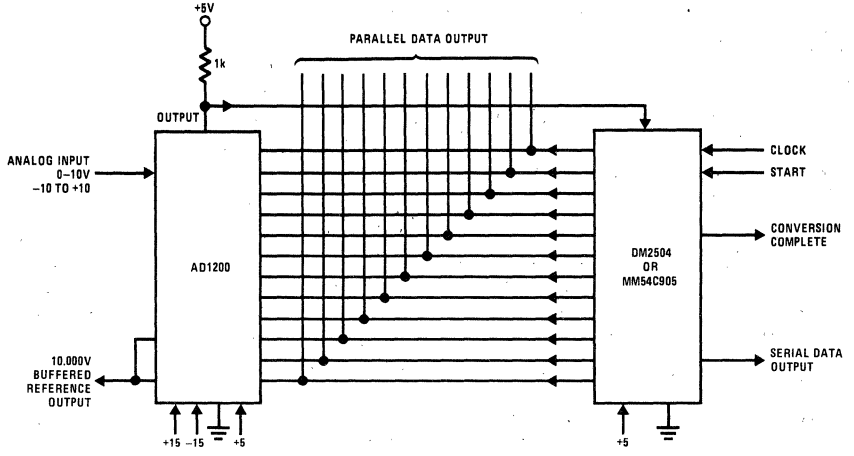
block and connection diagrams



Dual-In-Line Package

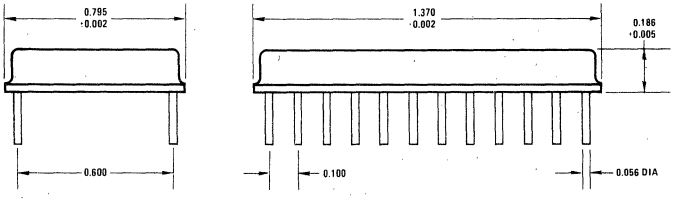


typical application

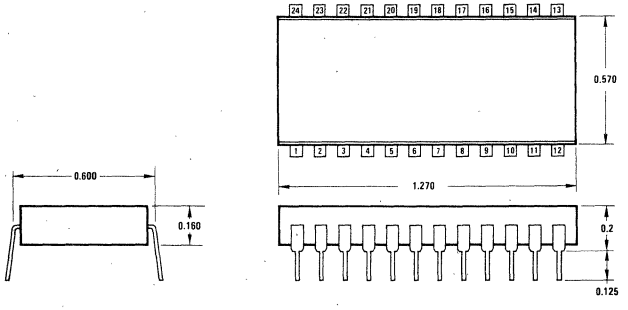


12-Bit Successive Approximation A to D

physical dimensions



Metal Dual-In-Line Package (D)



Cavity Plastic Dual-In-Line Package (N)

NATIONAL

PRELIMINARY DATA: JAN 1976

AD1210 12-bit CMOS A/D converter

general description

The AD1210 is a low power 12-bit successive approximation analog-to-digital converter. Included within the device are the successive approximation logic, analog switches, precision laser trimmed thin film R-2R ladder network and FET input comparator. The AD1210 will operate over a wide supply range, convert bipolar or unipolar signals, and operate in start-stop or continuous conversion modes. The binary outputs are directly compatible with CMOS logic levels. The only active external component required is the reference.

The AD1210 is available in 24-pin plastic DIP or 24-pin metal DIP.

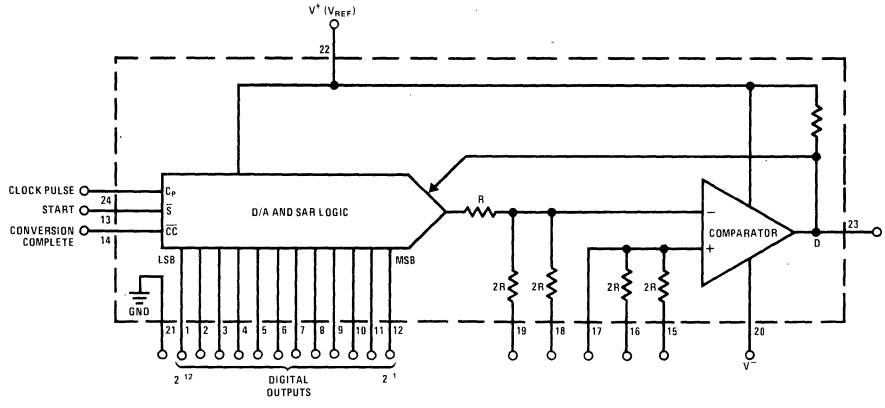
features

- Wide supply range 3V to 15V
- Single reference voltage
- CMOS compatible
- Low power consumption
- Single supply operation for single polarity voltages
- Internal comparator
- Provision for truncation
- Start/stop or continuous conversion
- High analog input impedance

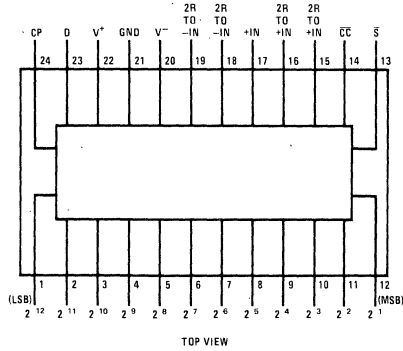
key specifications

- Resolution 12 bits
- Linearity ±1/2 LSB
- Clock rate up to 500 kHz
- Conversion rate 20 kHz
- Power consumption 75 mW @ +15V

block and connection diagrams

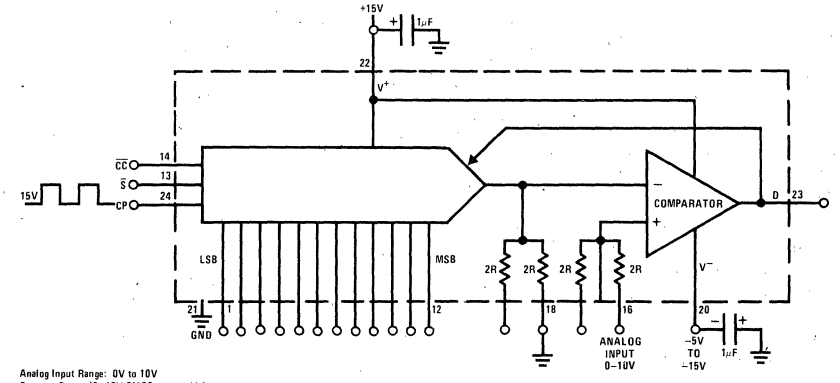


Dual-In-Line Package

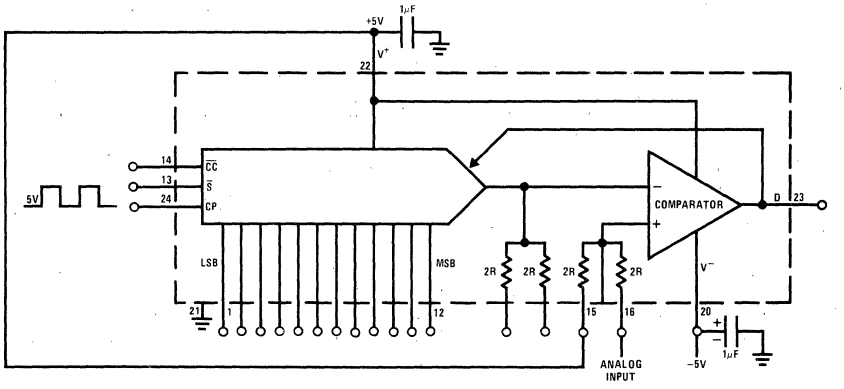


TOP VIEW

typical applications

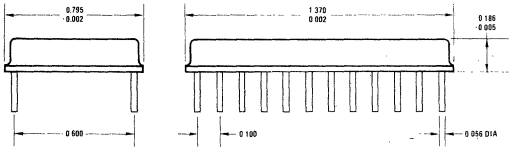


Analog Input Range: 0V to 10V
Output: Binary (0–15V CMOS compatible)

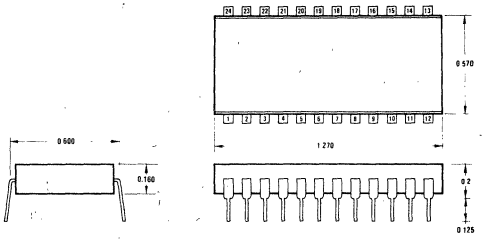


Analog Input Range: −5V to +5V
Output: Offset Binary (0–5V CMOS compatible)

physical dimensions



Metal Dual-In-Line Package (D)



Cavity Plastic Dual-In-Line Package (N)

PRELIMINARY DATA: JAN 1976

NATIONAL

DA1200 series digital to analog converter

general description

The DA1200 series of digital-to-analog converters are a family of precision, low cost, converter building blocks intended to fulfill a wide range of both industrial and military D to A applications. These devices are complete functional blocks and require only the application of power supply voltages for operation. The design combines precision weighted current switches with an ultra-stable, very low drift, thin film resistor network. A precision 10.240V buffered reference voltage is included in the package. Input coding options include binary and BCD formats. The output may be programmed for 0V to 10.2375V operation, −10.000V to +10.235V operation, or current mode 0 to 2 mA operation.

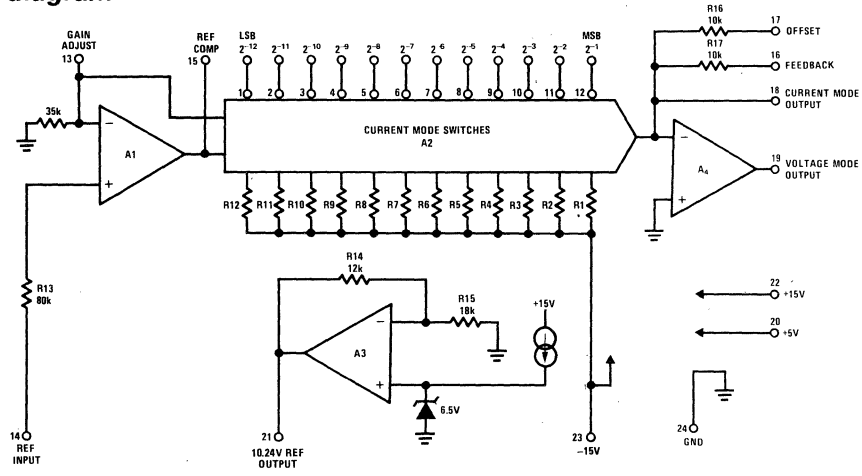
features

- Standard dual width 24 lead DIP (circuitry completely self-contained)
- Both current and voltage mode outputs
- Fast settling time — 5μs voltage mode
- Standard power supplies — ±15V, +5V
- TTL, DTL, CMOS compatible inputs
- Internal 10.240V precision reference
- Extendable to 14, 16 bits
- 1/2 LSB linerarity

applications

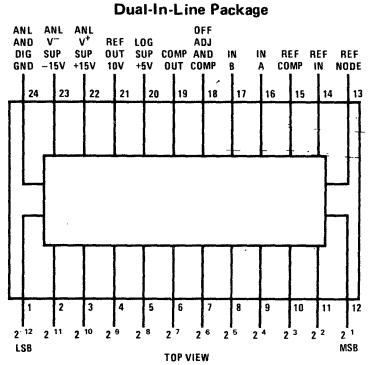
- CRT displays
- Programmable power supplies
- High speed data acquisition systems

block diagram



connection diagram

Dual-In-Line Package



PRELIMINARY DATA

DM7700/DM8700 one chip 2 1/2-digit panel meter

general description

The DM7700 contains the complete circuitry required to implement a 2-1/2 digit panel meter. Included are an input amplifier, temperature compensated reference, on-chip clock, counting and control logic, display multiplex circuitry and LED digit and current controlled segment plus decimal point drivers. The DM7700 employs a V-F conversion technique with counters and decode logic. Automatic polarity and overrange indication are provided.

The DM7700 is specified over −20°C to +95°C; the DM8700 is specified over 0°C to +50°C. The DM8700 is available in 24-pin Epoxy B and cavity DIPs; the DM7700 is available in 24-pin cavity DIP.

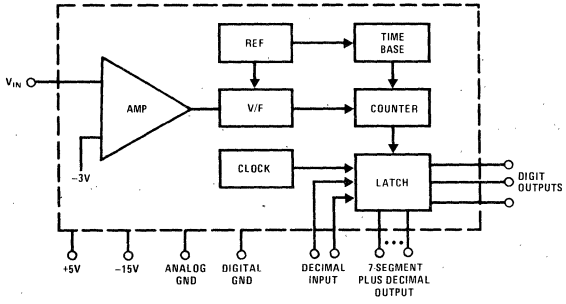
features

- Complete circuitry
- Internal reference
- Direct LED drive
- Auto polarity and overrange
- Standard supplies +5V, −15V, GND

key specifications

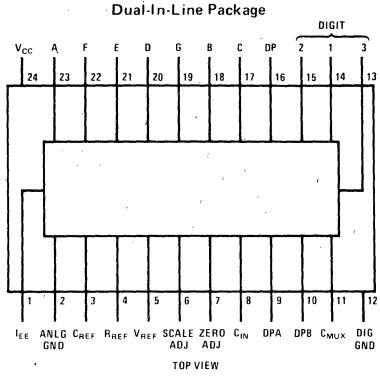
- Analog range ±1.99V
- Input impedance 500 kΩ
- Conversion time 1 second
- Accuracy ±1%

block diagram

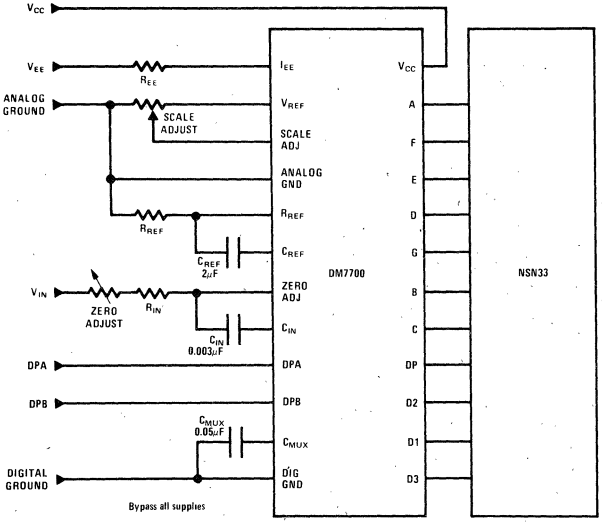


connection diagram

Dual-In-Line Package



typical application

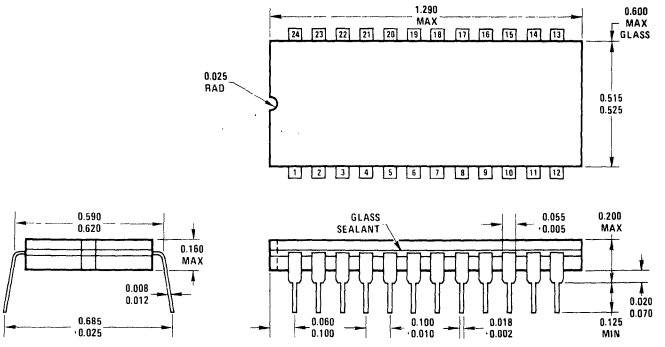


display patterns

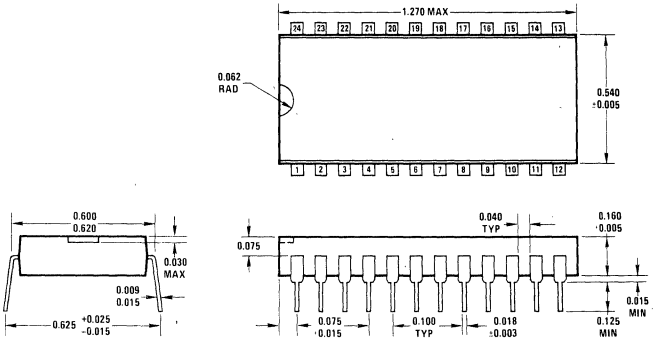
V_{IN}	DISPLAY
−3.00V	−. . .
−2.00V	−. . .
−1.99V	−1.99
−0.005V	−.005
0.005V	.005
1.99V	1.99
2.00V	. . .
2.99V	. . .

DECIMAL POINT LOCATION PROGRAMMED

physical dimensions



Cavity Dual-In-Line Package (J)
Order Number DM7700J or
DM8700J



Molded Dual-In-Line Package (N)

PRELIMINARY DATA: JAN 1976

NATIONAL

LF11300 dual slope A/D analog building block
MM5330 BCD dual slope A/D digital building block
MM5863 12-bit binary dual slope A/D digital building block

general description

LF11300

The LF11300 is the analog front end for a dual slope A/D converter. It is designed for use with either the MM5330 BCD digital building block or the MM5863 12-bit binary digital building block. The LF11300 provides a high impedance FET input, handles ±10V analog inputs with polarity indications and has automatic offset correction.

MM5330

The MM5330 provides multiplexed 4-1/2 digit BCD outputs, digit selects, polarity indicator, and overrange indication. It is used for 2-1/2, 3-1/2, or 4-1/2 digit panel meters. The LF11300 may be used as the analog front end or a discrete implementation may be used.

MM5863

The MM5863 provides a 12-bit parallel TRI-STATE® binary output or a 12-bit serial output. Overrange and polarity indication are also provided. A set of latches insures valid digital data at all times. Thus a practical low cost, accurate, 12-bit converter for use with microprocessors can be constructed, even though conversion speed is 20 ms.

features

LF11300

- Auto zero and auto polarity
- FET input — >100 MΩ impedance
- ±10V analog range
- Clock rate (f_C) — 1 kHz to 500 kHz
- Conversion rate — $10{,}000/f_C$
- Ratiometric inputs
- ±15V, +5V supplies
- 0.02% ±1 LSB accuracy
- No zero or full scale adjustments

MM5330

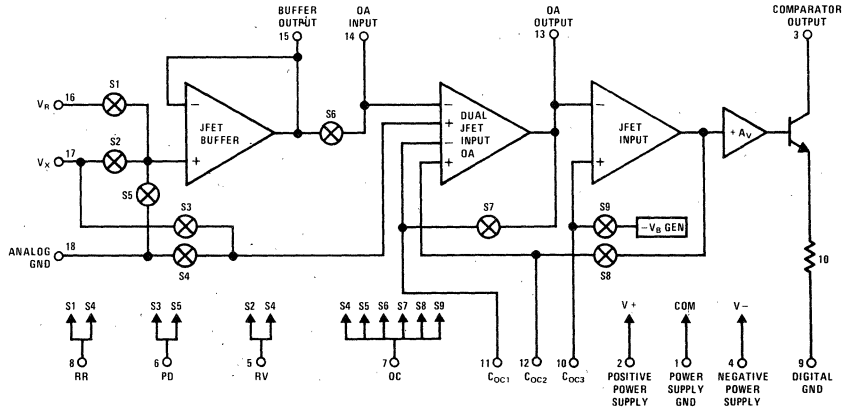
- 4-1/2 digit BCD output
- Overrange indicator
- Polarity indicator

MM5863

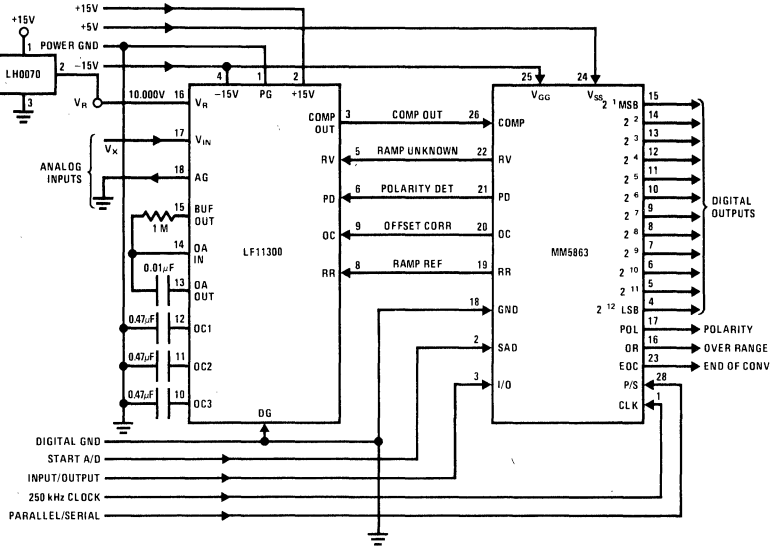
- 12-bit binary output
- Parallel or serial
- TRI-STATE® output
- Polarity indicator
- Overrange indicator

block diagram

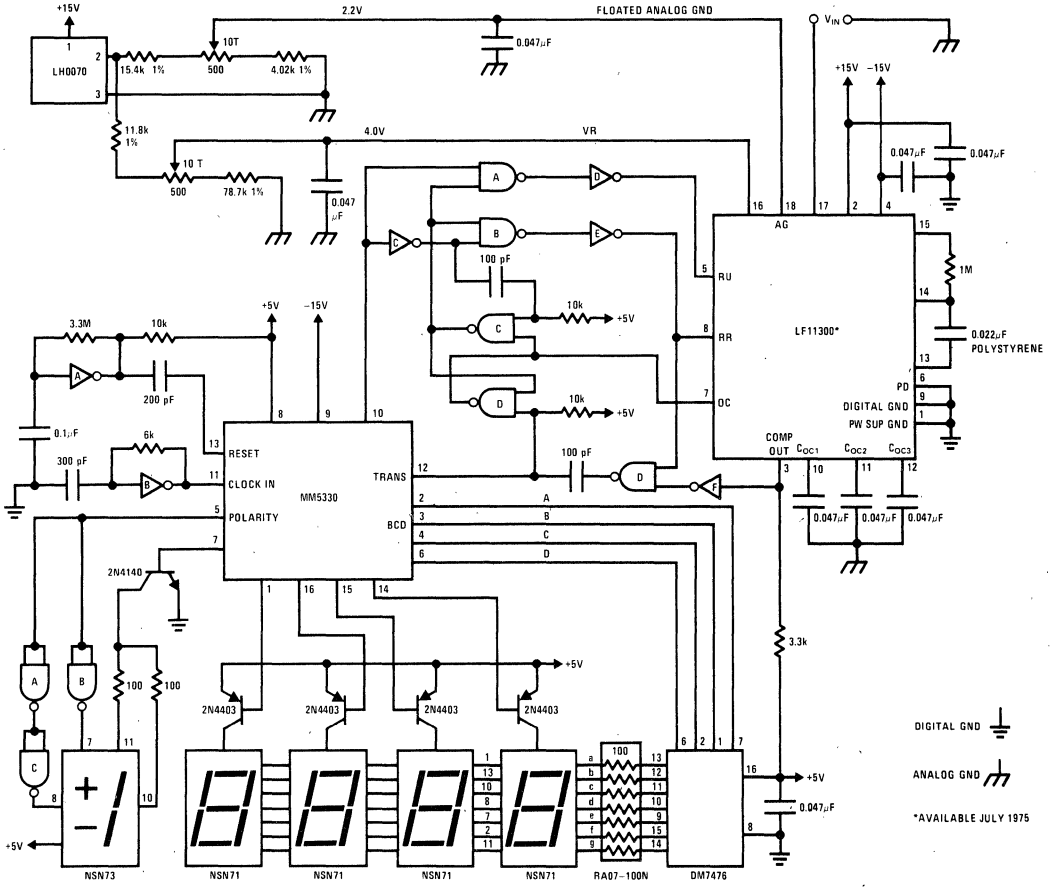
LF11300



typical applications

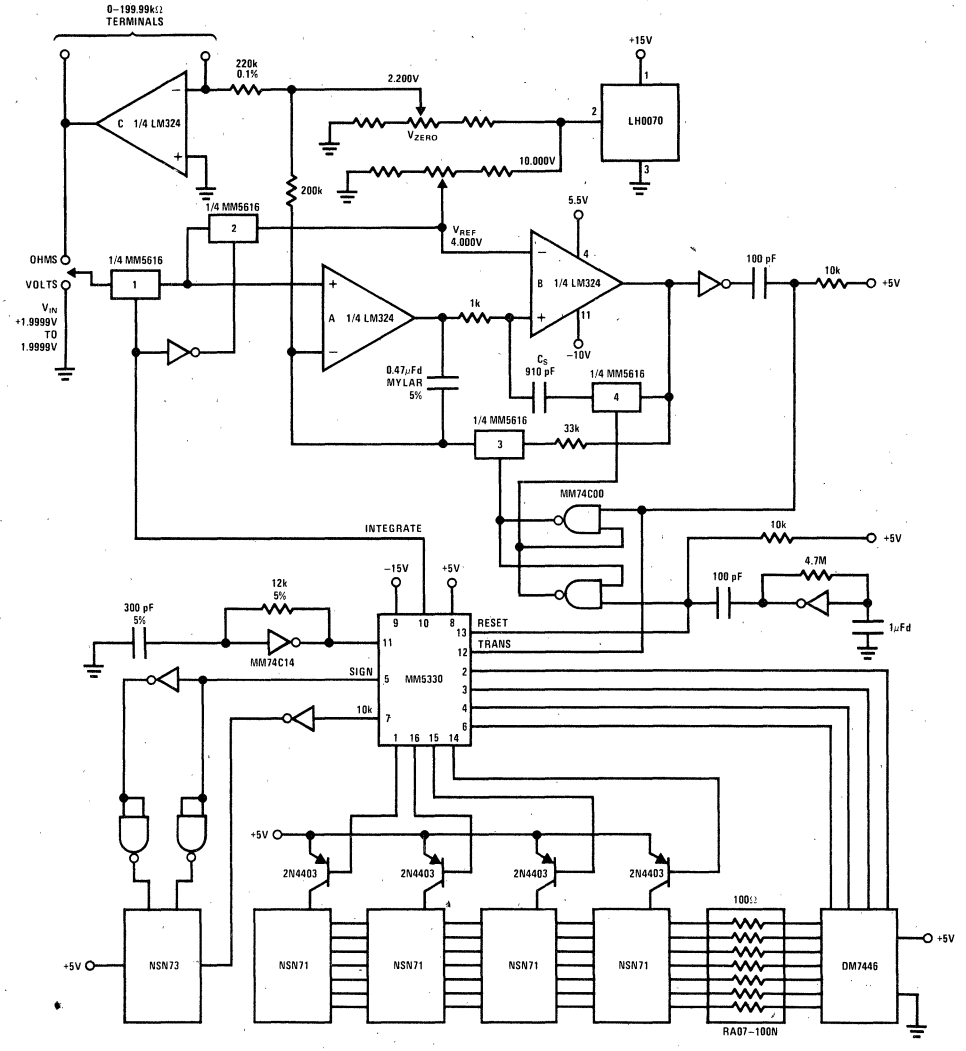


LF11300, MM5863 12-Bit Binary A/D Converter System



LF11300, MM5330 DPM Application

typical applications (con't)



MM5330 Discrete DPM Application

NATIONAL

LM11340 quad current switch

general description

The LM11340 is a high speed quad current switch for use in D/A conversion. It consists of four binary weighted current switches and an LSB reference transistor. The switch current magnitudes are set by an external voltage source and precision resistors. The four switch currents are summed to produce a single output proportional to the binary code at the switch inputs.

The reference transistor is used with external circuitry to compensate for Beta and V_{BE} variation due to temperature.

The LM11340 is TTL compatible. The LM11340 logic levels are referenced to ground and are independent of any baseline voltage changes.

The LM11340 also contains an extra baseline diode which prevents system latch-up when driving the baseline with an op amp.

The LM11340 comes in Epoxy B DIPs and cavity DIPs.

features

- TTL and CMOS compatible
- Wide power supply range
- Low logic input currents
- Power dissipation unaffected by bit patterns
- Isothermal layout
- No system latch-up

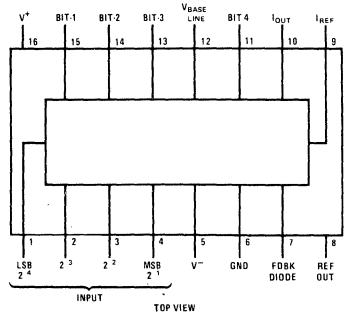
key specifications

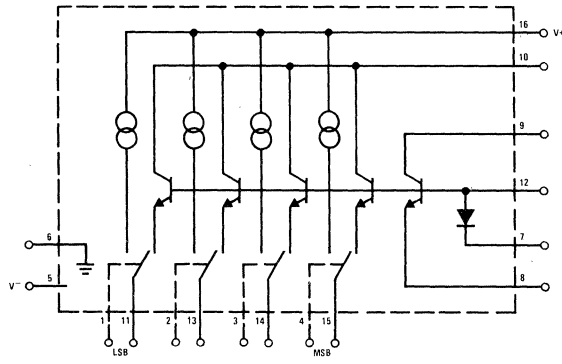
- 12-bit accuracy and linearity
- 100 ns settling time to 12-bit

connection and block diagrams

LM11340

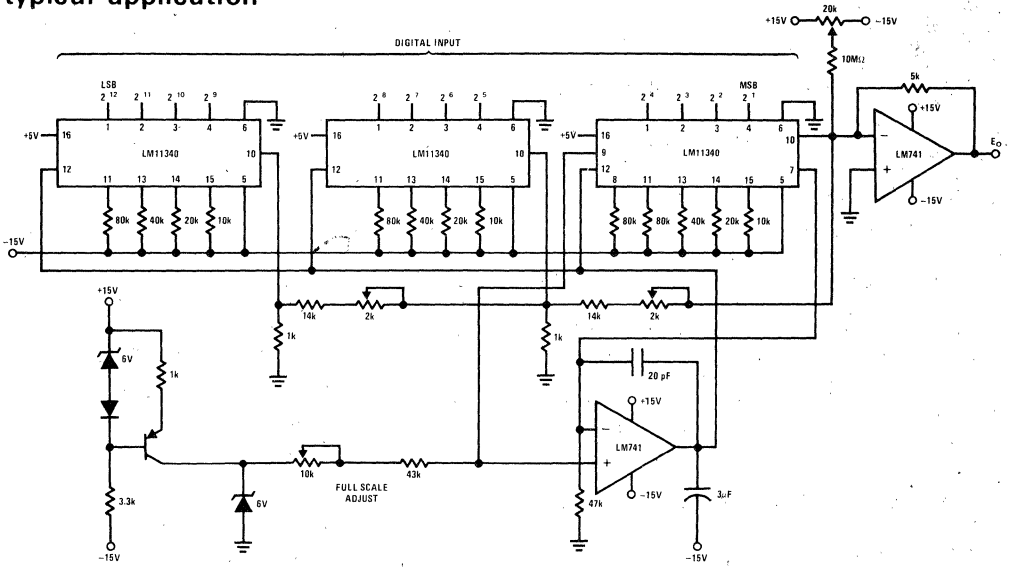
Dual-In-Line Package





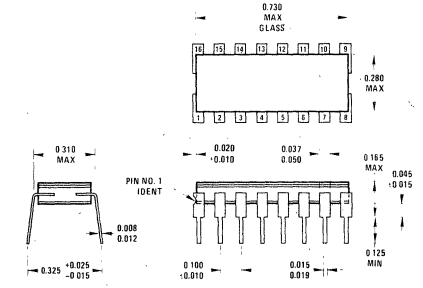
LM11340 Equivalent Circuit

typical application

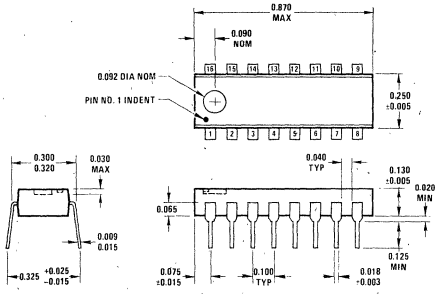


Temperature Compensated 12-Bit D/A Converter

physical dimensions



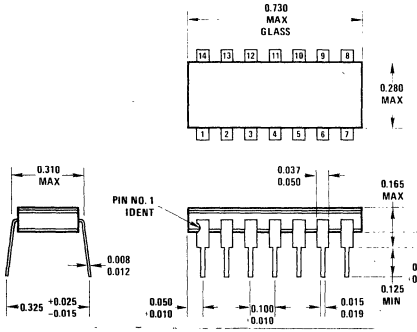
Cavity Dual-In-Line Package (D)



Molded Dual-In-Line Package (N)

Physical Dimensions

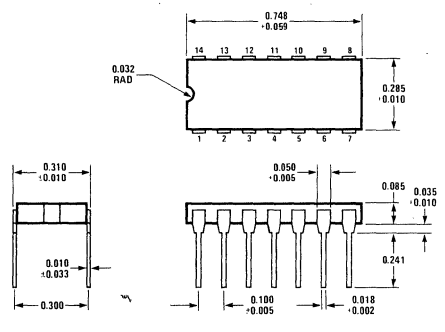
(All dimensions are in inches.)



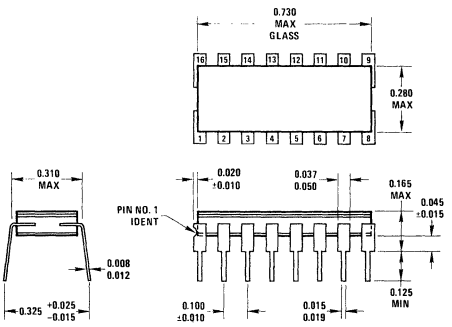
Note: Devices in this package may be supplied in Package 1A.

Package 1

14 Lead Cavity DIP (D)



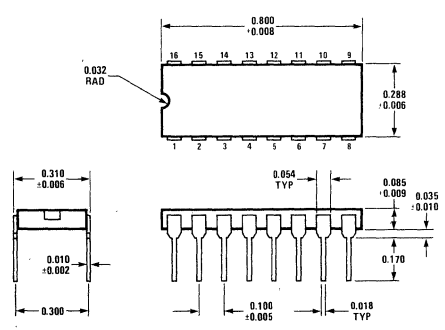
Package 1A



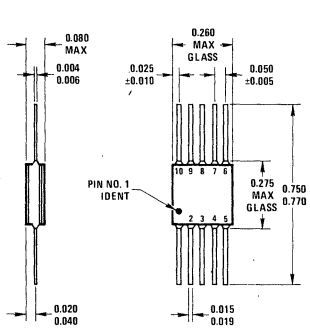
Note: Devices in this package may be supplied in Package 2A.

Package 2

16 Lead Cavity DIP (D)

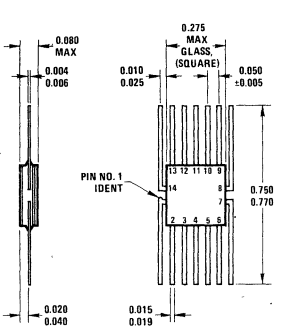


Package 2A



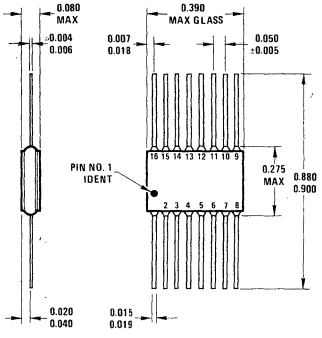
Package 3

10 Lead Flat Package (F)



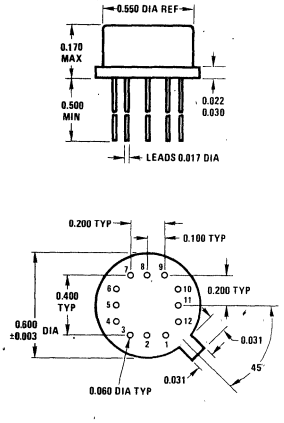
Package 4

14 Lead Flat Package (F)

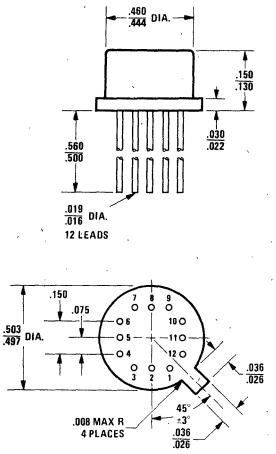


Package 5

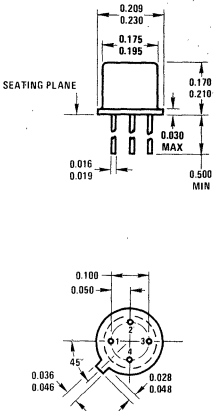
16 Lead Flat Package (F)



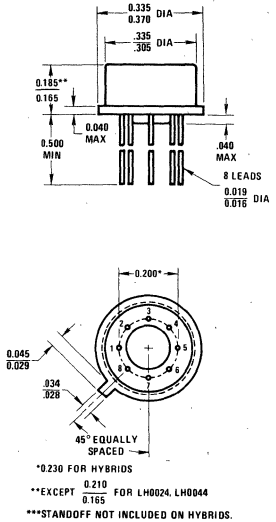
Package 6
12 Lead TO-8 Metal Can (G)



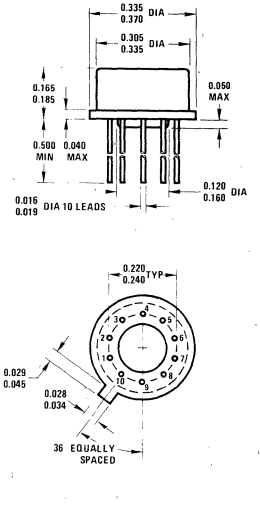
Package 7
12 Lead TO-8 Metal Can (G)
(AH2114/AH2114C only)



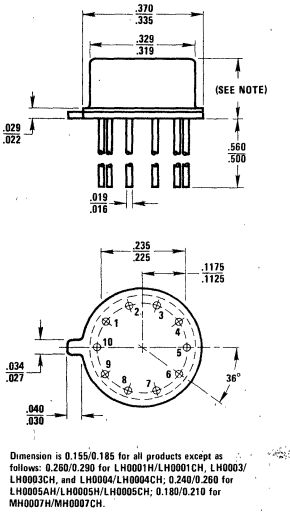
Package 8
4 Lead TO-72 Metal Can (H)



Package 9
8 Lead TO-5 Metal Can (H)

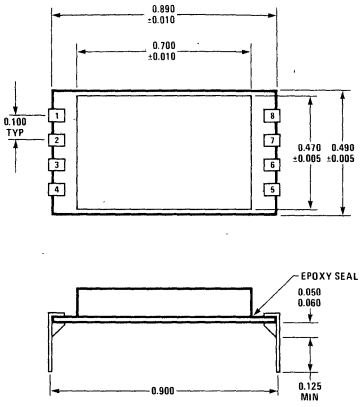


Package 10
10 Lead TO-5 Metal Can (H)
(Low Profile)

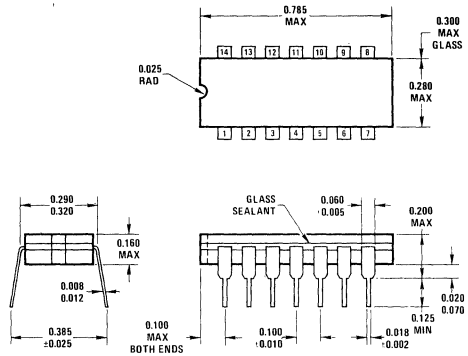


Dimension is 0.155/0.185 for all products except as follows: 0.260/0.290 for LH0001H/LH0001CH, LH0003/LH0003CH, and LH0004/LH0004CH; 0.240/0.260 for LH0005AH/LH0005H/LH0005CH; 0.180/0.210 for MH0007H/MH0007CH.

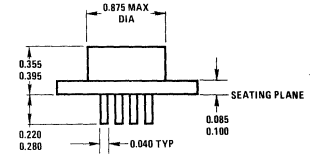
Package 11
10 Lead TO-5 Metal Can (H)

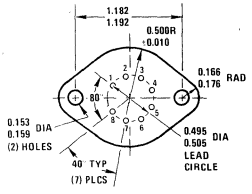


Package 12
8 Lead Cavity Package (J)

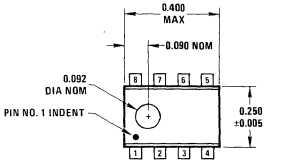


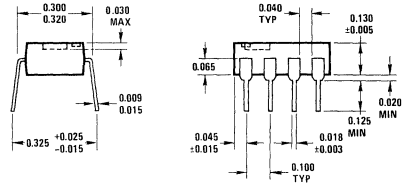
Package 13
14 Lead Cavity DIP (J)



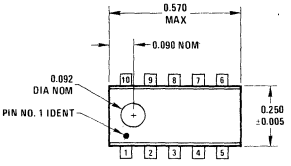


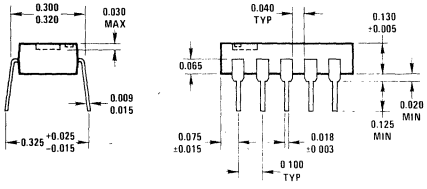
Package 14
8 Lead TO-3 Metal Can (K)



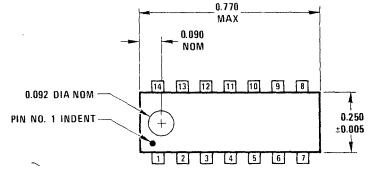


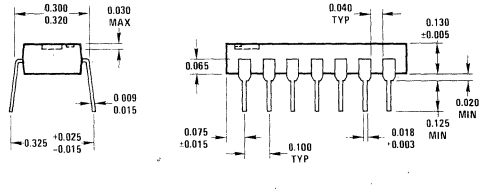
Package 15
8 Lead Molded Mini DIP (N)





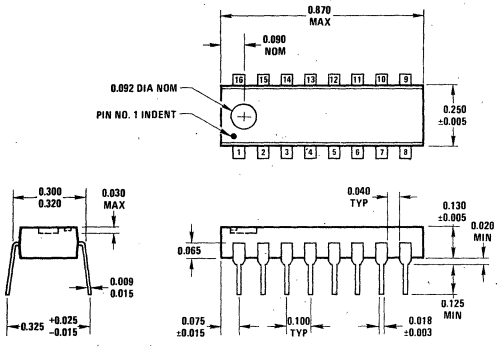
Package 16
10 Lead Molded DIP (N)



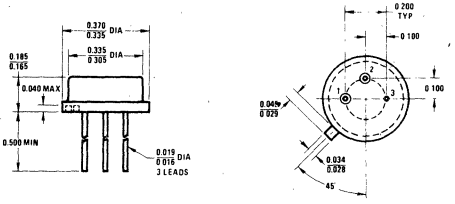


Package 17
14 Lead Molded DIP (N)

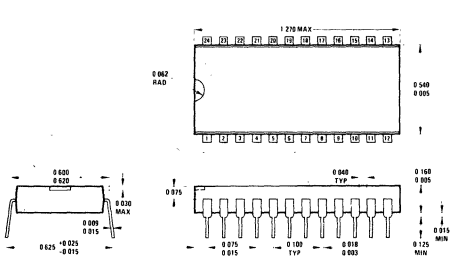
12



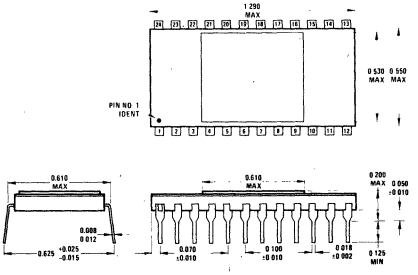
Package 18
16 Lead Molded DIP (N)



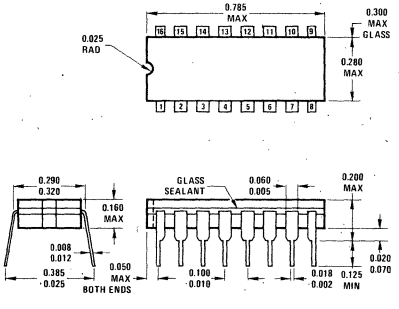
Package 19
Metal Can Package (H)



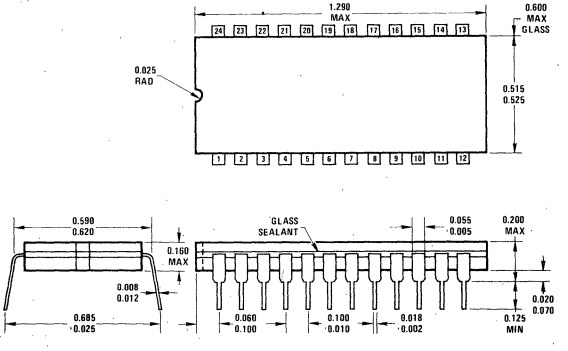
Package 20
Molded Dual-In-Line Package (N)



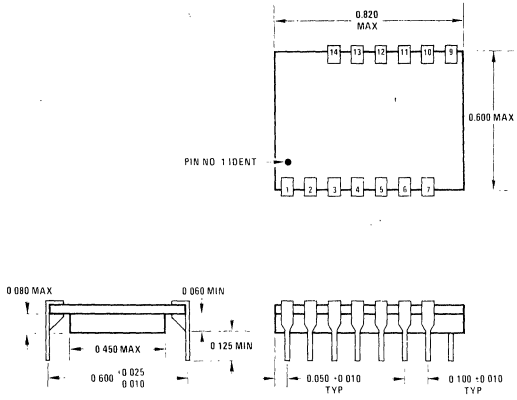
Package 21
24 Lead Cavity Dual-In-Line Package (D)



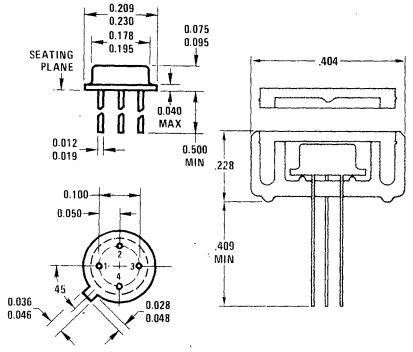
Package 22
16 Lead Cavity Dual-In-Line Package (J)



Package 23
24 Lead Cavity Dual-In-Line Package (J)



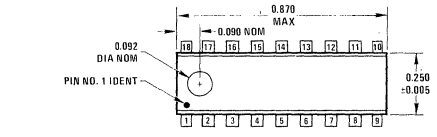
Package 24
Ceramic Dual-In-Line Package (J)

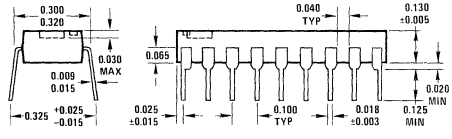


Package 25
TO-46 Metal Can Package (H)

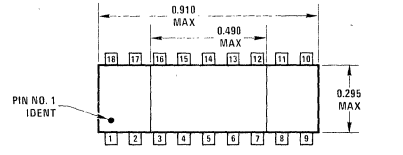
Thermal Shield
(TO-46 Package Inside)

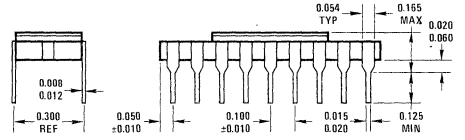
All units shipped with thermal shield.





Package 26
18-Lead Molded DIP (N)





Package 27
18-Lead Cavity DIP (D)

INCHES TO MILLIMETERS CONVERSION TABLE					
INCHES	MM	INCHES	MM	INCHES	MM
.001	.0254	.010	.254	.100	2.54
.002	.0508	.020	.508	.200	5.08
.003	.0762	.030	.762	.300	7.62
.004	.1016	.040	1.016	.400	10.16
.005	.1270	.050	1.270	.500	12.70
.006	.1524	.060	1.524	.600	15.24
.007	.1778	.070	1.778	.700	17.78
.008	.2032	.080	2.032	.800	20.32
.009	.2286	.090	2.286	.900	22.86

Miscellaneous Hardware

Following is a partial list of sockets and heat dissipators for use with various packages shown in this catalog. National assumes no responsibility for their quality or availability.

8-Lead TO-3 Hardware

SOCKETS
- Keystone 4626 or 4627
- Robinson Nugent 0002011
- Azimuth 6028 (test socket)

HEAT SINKS
- Thermalloy 2266B (35°C/W)
- IERC LAIC3B4CB
- IERC HP1-TO3-33CB (7°C/W)

MICA WASHERS
- Keystone 4658

24-Pin DIP

SOCKETS
- Amphenol/Barnes 821-40012-244
- Robinson Nugent IC 246-S1 or S2

12-Lead TO-8 Hardware

SOCKETS
- Amphenol/Barnes { 641-30031-121 / 641-01061-121 } (test socket)
- Robinson Nugent MP12100S or W
- Textool 212-100-323

HEAT SINKS
- Thermalloy 2240A (33°C/W)
- Wakefield 215CB (30°C/W)
- IERC UP-TO8-48CB (15°C/W)

Amphenol/Barnes
2875 S. 25th Ave.
Broadview, IL 60153

Azimuth Electronics
2377 S. El Camino Real
San Clemente, CA 92672

IERC
135 W. Magnolia Bl.
Burbank, CA 91502

Keystone Electronics Corp.
49 Bleecker St.
New York, NY 10012

Robinson Nugest Inc.
800 E. 8th St.
New Albany, IN 47150

Thermalloy
P.O. Box 34829
Dallas, TX 75234

Wakefield Engineering Inc.
Wakefield, MA 01880

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