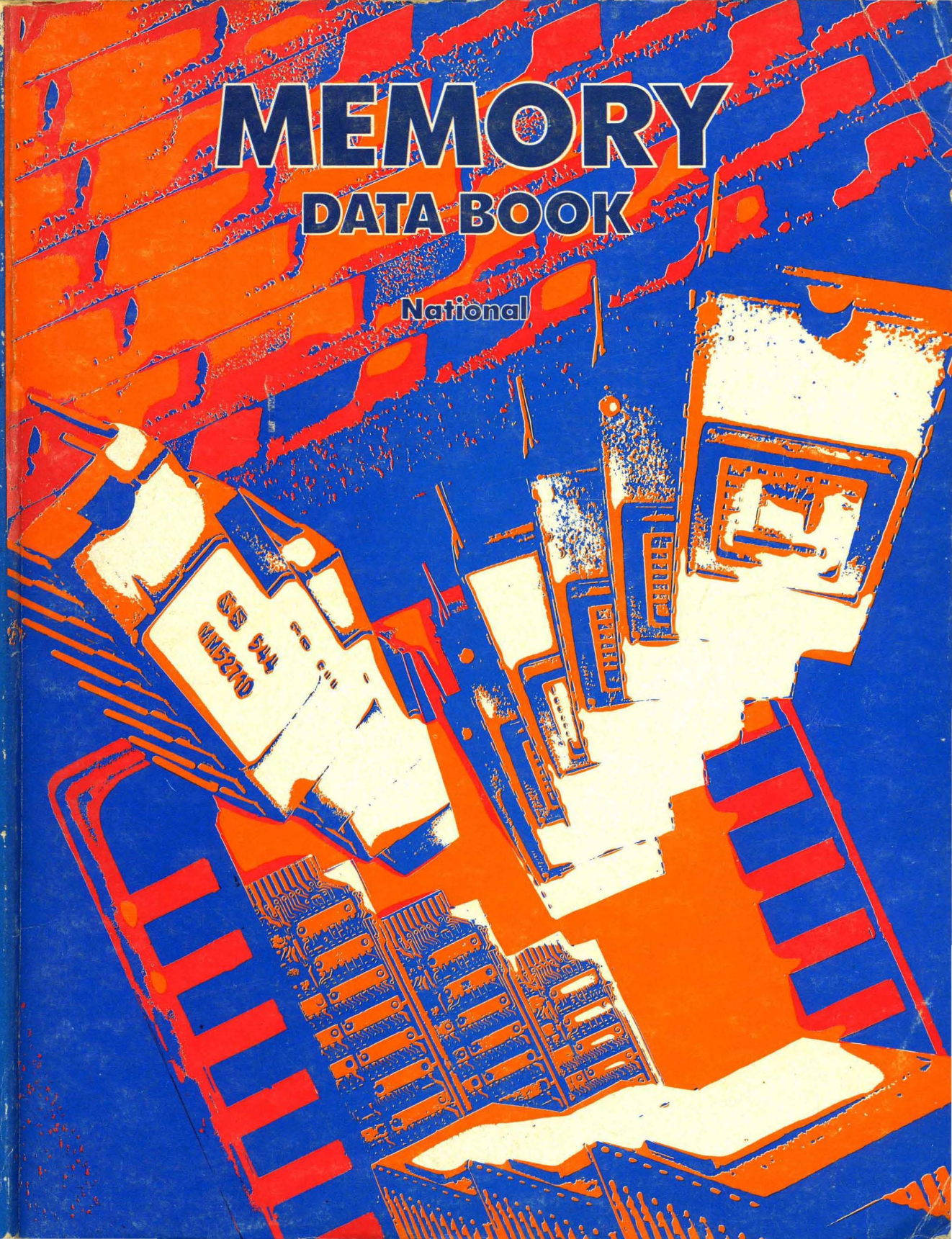
MEMORY DATA BOOK

National



MEMORY DATA BOOK

JAN 1976

National

Edge Index by Product Family

This is National's first Memory handbook containing information on MOS and Bipolar Memory Components, Systems, Application Notes and Support Circuits. For detailed information on Interface Circuits and other major product lines, contact a National sales office, representative, or distributor.

Manufactured under one or more of the following U.S. patents: 3083262, 3189758, 3231797, 3303356, 3317671, 3323071, 3381071, 3408542, 3421025, 3426423, 3440498, 3518750, 3519897, 3557431, 3560765, 3566218, 3571630, 3575609, 3579059, 3593069, 3597640, 3607469, 3617859, 3631312, 3633052, 3638131, 3648071, 3651565, 3693248.

COVER GRAPHICS BY TCHRAKIAN & ASSOC.

Future Products

In addition to the products contained in this catalog, the following products are planned for 1976:

DEVICE NUMBER	DESCRIPTION	AVAILABLE
MOS RAMs		
MM2101A	256 x 4 Static RAM—22 Pin	First Quarter, 1976
MM2102A	1k x 1 Static RAM	First Quarter, 1976
MM2111A	256 x 4 Static RAM—18 Pin	First Quarter, 1976
MM21112A	256 x 4 Static RAM—16 Pin	First Quarter, 1976
MM5255	1k x 4 Static RAM—18 Pin	Third Quarter, 1976
MM5256	1k x 4 Static RAM—22 Pin	Third Quarter, 1976
MM5257	4k x 1 Static RAM—18 Pin	Third Quarter, 1976
MM5275	1k x 4 Dynamic RAM	Second Quarter, 1976
Bipolar RAMs		
DM93415	1k x 1 TTL RAM	Fourth Quarter, 1976
CMOS RAMs		
MM74C921	256 x 4 Silicon Gate—18 Pin	First Quarter, 1976
MM74C929	1k x 1 Silicon Gate—16 Pin	Second Quarter, 1976
MM74C930	1k x 1 Silicon Gate—18 Pin	Second Quarter, 1976
Bipolar PROMs		
DM74S472	512 x 8—20 Pin	Third Quarter, 1976
DM74S473	512 x 8—20 Pin	Third Quarter, 1976
DM87S295	512 x 8—24 Pin	Third Quarter, 1976
DM87S296	512 x 8—24 Pin	Third Quarter, 1976
MOS ROMs		
MM5238	512 x 8 N-Channel ROM	Third Quarter, 1976
MM5245	2048 x 4 N-Channel ROM	Third Quarter, 1976
MM5247	4096 x 4 N-Channel ROM	Third Quarter, 1976
MM5249	1024 x 4 N-Channel ROM	Third Quarter, 1976
Shift Registers		
MM5062	P-Channel Quad 80-Bit Static	Second Quarter, 1976
MM5063	N-Channel Quad 256-Bit Static	Fourth Quarter, 1976
MM5064	N-Channel Dual 512-Bit Static	Fourth Quarter, 1976
MM5065	N-Channel Single 1024-Bit Static	Fourth Quarter, 1976

Table of Contents

BIPOLAR PROMS—SECTION 5

MOS ROMS—SECTION 6

MOS ROMS—SECTION 6 (Cont.)

BIPOLAR ROMS—SECTION 7

SHIFT REGISTERS—SECTION 8

SHIFT REGISTERS—SECTION 8 (Cont.)

MEMORY SYSTEMS—SECTION 9

INTERFACE—SECTION 10

INTERFACE–SECTION 10 (Cont.)

APP NOTES/BRIEFS–SECTION 11

Alpha-Numerical Index

MOS RAMs

MM1101, MM11011, MM1101A, MM1101A1, MM1101A2, MM4250
256-bit fully decoded static random access memory

general description

The MM1101 family of fully decoded 256 word x 1-bit random access memories are monolithic MOS integrated circuits using silicon gate low threshold technology to achieve bipolar compatibility. They are static, require no clocks, and hold information indefinitely, subject to the integrity of the power supply voltages.

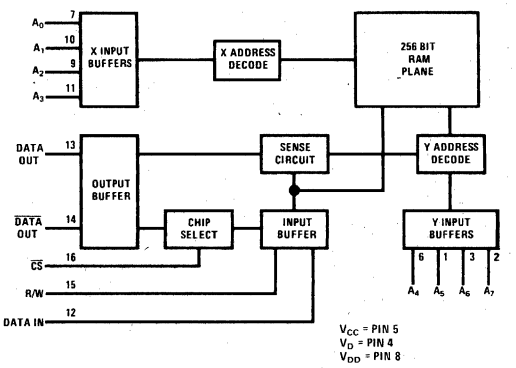
features

- Fast access times MM1101A2 500 ns max
  MM11011, MM1101A1 1.0 μs max
  MM1101, MM1101A 1.5 μs max
  MM4250 650 ns max
- Improved speed/power product MM1101A2 1/3 of 1101A
- Low power operation 1.5 mW/bit
- Fewer system components - bipolar compatible input and output
- Second source flexibility - MM1101, MM1101A MM11011, MM1101A1 second sources available
- TRI-STATE™ output - wired OR capability
- Specified ambient temperature 0°C to +70°C, for MM1101 family; −55°C to +125°C for MM4250

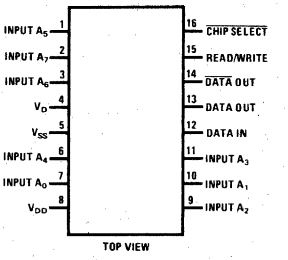
applications

- High speed buffer memories
- Local memory store

block and connection diagrams



Dual-In-Line Package



Order Number MM1101D, MM1101AD, MM1101A1D, MM1101A2D, MM11011D or MM4250D
See Package 3

Order Number MM1101N, MM1101AN, MM1101A1N, MM1101A2N or MM11011N
See Package 15

absolute maximum ratings

All Input or Output Voltages with Respect to the Most Positive Supply Voltage, V_{SS}	+0.3V to −20V
Supply Voltages V_{DD} and V_D with Respect to V_{SS}	−16V
Power Dissipation at Room Temperature	700 mW
Operating Temperature	
MM1101 Family	0°C to +70°C ambient
MM4250	−55°C to +125°C ambient
Storage Temperature	−66°C to +160°C
Lead Temperature (Soldering, 10 sec)	300°C

dc characteristics

T_A = 0°C to +70°C for MM1101 Family, T_A = −55°C to +125°C for MM4250;
V_{SS} = +5V ±5%, V_D = V_{DD} = −9V ±5% for MM4250, MM1101A, MM1101A1, MM1101A2;
V_{SS} = +5V ±5%, V_D = −10V ±5%, V_{DD} = −7V ±5%, for MM1101, MM11011 (unless otherwise specified).

SYMBOL	TEST	CONDITIONS	MM1101 FAMILY MIN	MM1101 FAMILY TYP	MM1101 FAMILY MAX	MM4250 MIN	MM4250 TYP	MM4250 MAX	UNITS
I_{LI}	Input Load Current (All Input Pins)	V_{IN} = 0.0		0.001	0.5			1.0	µA
I_{LO}	Output Leakage Current	V_{OUT} = 0.0V, CS = V_{SS} − 2.0V		0.001	0.5			1.0	µA
MM4250 MM1101A MM1101A1 MM1101A2 I_{DD}	Power Supply Current, V_{DD}	T_A = 25°C, Continuous Operation, I_{DL} = 0.0 mA		13.0	19.0		13.0	19.0	mA
MM4250 MM1101A MM1101A1 MM1101A2 I_{DD}	Power Supply Current, V_{DD}	T_A = 0°C, Continuous Operation, I_{DL} = 0.0 mA			25.0			25.0	mA
MM4250 MM1101A MM1101A1 MM1101A2 I_D	Power Supply Current, V_D	T_A = 25°C, Continuous Operation, I_{DL} = 0.0 mA		12.0	18.0		12.0	18.0	mA
MM4250 MM1101A MM1101A1 MM1101A2 I_D	Power Supply Current, V_D	T_A = 0°C, Continuous Operation, I_{DL} = 0.0 mA			24.0			24.0	mA
V_{IL}	Input LOW Voltage		V_{SS} − 10		V_{SS} − 4.2	V_{SS} − 10		V_{SS} − 4.2	V
V_{IH}	Input HIGH Voltage		V_{SS} − 2.0		V_{SS} + 0.3	V_{SS} − 2.0		V_{SS} + 0.3	V
I_{OL}	Output Sink Current	V_{OUT} = +0.45V, T_A = 25°C	3.0	8.0		3.0	8.0		mA
I_{OL}	Output Sink Current	V_{OUT} = +0.45V, T_A = 70°C	2.0			2.0			mA
I_{CF}	Output Clamp Current	V_{OUT} = −1.0V, T_A = 0°C		6.0	13.0		6.0	13.0	mA
I_{OH}	Output Source Current	V_{OUT} = 0.0V, T_A = +25°C	−3.0	−8.0		−3.0	−8.0		mA
I_{OH}	Output Source Current	V_{OUT} = 0.0V, T_A = +70°C	−2.0	−7.0		−2.0	−7.0		mA
V_{OH}	Output HIGH Voltage	I_{OH} = −100 µA	3.5	4.9		3.5	4.9		V
C_{IN}	Input Capacitance (Note 3) (All Input Pins)	V_{IN} = V_{SS}, f = 1 MHz		7.0	10.0		7.0	10.0	pF
C_{OUT}	Output Capacitance	V_{OUT} = V_{SS}, f = 1 MHz		7.0	10.0		7.0	10.0	pF
C_V	V_D Power Supply Capacitance	V_D = V_{SS}, f = 1 MHz		20.0	35.0		20.0	35.0	pF
MM1101 MM11011 I_{DD}	Power Supply Current, V_{DD}	T_A = 25°C, Continuous Operation, I_{DL} = 0.0 mA		14.0	18.0				mA
MM1101 MM11011 I_D	Power Supply Current, V_D	T_A = 25°C, Continuous Operation, I_{DL} = 0.0 mA		17.0	20.0				mA

ac characteristics

T_A = 0°C to +70°C for MM1101 Family, T_A = −55°C to +125°C for MM4250;
V_{SS} = +5V ±5%, V_D = V_{DD} = −9V ±5% for MM4250, MM1101A, MM1101A1, MM1101A2;
V_{SS} = +5V ±5%, V_D = −10V ±5%, V_{DD} = −7V ±5%, for MM1101, MM11011 (unless otherwise specified).

SYMBOL	TEST	MIN	TYP (Note 2)	MAX	UNITS
t_{rc}	Read Cycle MM1101, MM1101A	1.5			µs
	MM11011, MM1101A1	1.0			µs
	MM1101A2	500.0			ns
	MM4250	650.0			ns
t_{ac}	Address to Chip Select Delay				
	MM1101, MM1101A,			1.2 (Note 4)	µs
	MM11011, MM1101A1			0.7 (Note 4)	µs
	MM1101A			0.2 (Note 4)	µs
	MM4250			0.35 (Note 4)	µs
t_a	Access Time MM1101, MM1101A		0.85	1.5	µs
	MM11011, MM1101A1		0.65	1.0	µs
	MM1101A2		400.0	500.0	ns
	MM4250		400.0	650.0	ns
t_{oh}	Previous Read Data Valid	50.0			ns

Note 1: All voltage measurements are referenced to ground.
Note 2: Typical values are at T_A = +25°C and nominal supply voltages.
Note 3: Capacitances are measured periodically only.
Note 4: Maximum value for t_{ac} measured at minimum read cycle.

ac characteristics (con't)

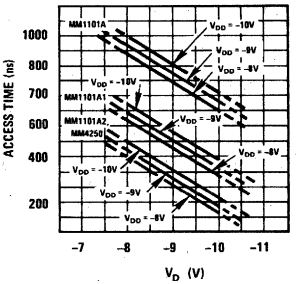
WRITE CYCLE (MM1101, MM11011, MM1101A, MM1101A1, MM1101A2)

SYMBOL	TEST	MIN	TYP (Note 2)	MAX	UNITS
t_{WC}	Write Cycle	0.8			μs
t_{WD}	Address to Write Pulse Delay	0.3			μs
t_{WP}	Write Pulse Width	0.4			μs
t_{DW}	Data Set up Time	0.3			μs
t_{DH}	Data Hold Time	0.1			μs
WRITE CYCLE (MM4250)					
t_{wc}	Write Cycle	1.0			μs
t_{wd}	Address to Write Pulse Delay	0.35			μs
t_{wp}	Write Pulse Width	0.50			μs
t_{dw}	Data Set-up Time	0.35			μs
t_{dh}	Data Hold Time	0.15			μs
CHIP SELECT AND DESELECT (MM1101, MM11011, MM1101A, MM1101A1, MM1101A2, MM4250)					
t_{CW}	Chip Select Pulse Width	0.4			μs
t_{CS}	Access Time Through Chip Select Input		0.2	0.3	μs
t_{CD}	Chip Deselect Time		0.1	0.3	μs

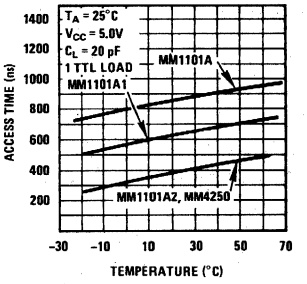
Note 1: All voltage measurements are referenced to ground.
Note 2: Typical values are at $T_A = +25°C$ and nominal supply voltages.
Note 3: Capacitances are measured periodically only.
Note 4: Maximum value for t_{ac} measured at minimum read cycle.

typical performance characteristics

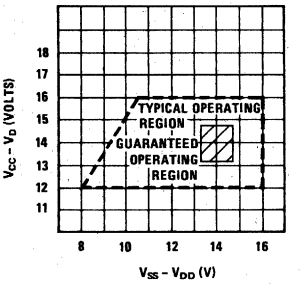
Typical Access Time vs Voltage



Typical Access Time vs Temperature

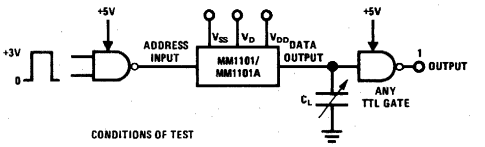


MM1101A, MM1101A1, MM1101A2, MM4250 Operating Region



ac test circuit

Test Setup for MM1101A and MM1101A Speed Measurement

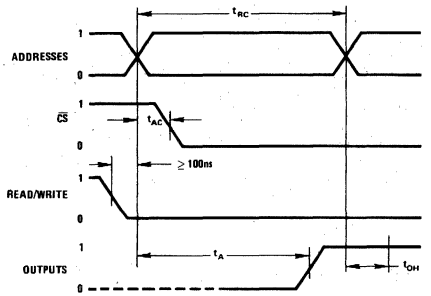


CONDITIONS OF TEST

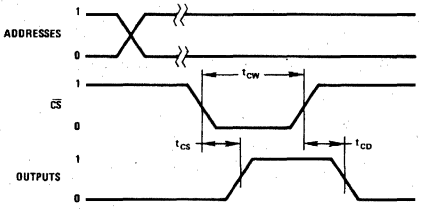
Input pulse amplitudes: 0V to +5.0V.
Input pulse rise and fall times ≤ 10 ns.
Speed measurements are referenced to the 1.5V level (unless otherwise noted); at the output of the TTL gate ($t_{pd} \leq 10$ ns) $C_L \leq 20$ pF.

switching time waveforms

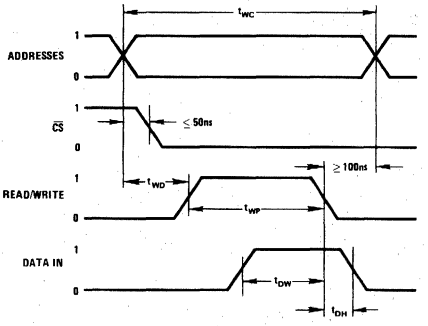
Read Cycle



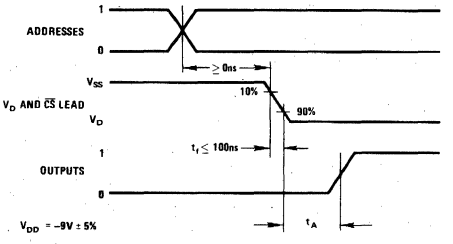
Chip Select and Deselect



Write Cycle



Power Switching For Reduced Power Applications



Note 1: All inputs of the MM1101A accept standard TTL outputs with V_{CC} = +5.0V ±5%.
Note 2: Maximum value for t_{AC} measured at minimum read cycle.

MOS RAMs

MM2101, MM2101-1, MM2101-2 1024-bit (256 × 4) static MOS RAM with separate I/O

general description

The National MM2101 is a 256 word by 4 bit static random access memory element fabricated using N-Channel enhancement mode Silicon Gate technology. Static storage cells eliminate the need for refresh and the additional peripheral circuitry associated with refresh. The data is read out nondestructively and has the same polarity as the input data.

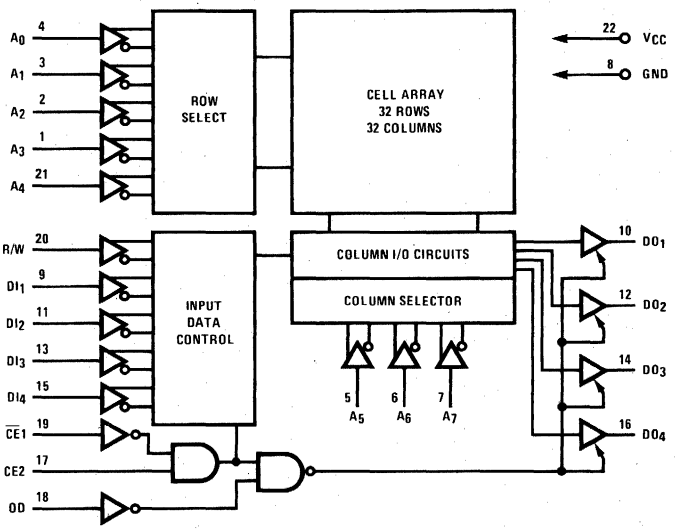
The 2101 is directly TTL compatible in all respects: inputs, outputs, and a single +5 V supply. Two chip-enables allow easy selection of an individual package when outputs are OR-tied. An output disable is provided so that data inputs and outputs can be tied for common I/O systems. The features of this memory device can be combined to make a low cost, high performance, and easy to manufacture memory system.

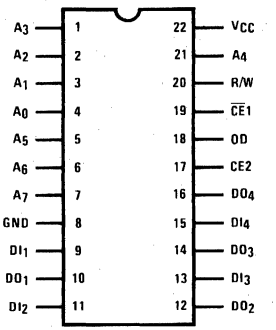
National's silicon gate technology also provides protection against contamination, and permits the use of low cost Epoxy B packaging.

features

- Organization 256 Words by 4 Bits
- Access Time – 0.5 to 1.0 μs Max.
- Single +5 V Supply Voltage
- Directly TTL Compatible – All Inputs and Outputs
- Static MOS – No Clocks or Refreshing Required
- Simple Memory Expansion – Chip Enable Input
- Low Cost Packaging – 22 Pin Epoxy B Dual-In-Line Configuration
- Low Power – Typically 150 mW
- Tri-State ® Output – OR-Tie Capability
- Output Disable Provided for Ease of Use in Common Data Bus Systems

block and connection diagrams





PIN NAMES

DI_1 - DI_4	DATA INPUT
A_0 - A_7	ADDRESS INPUTS
R/W	READ/WRITE INPUT
$\overline{CE}1$, CE2	CHIP ENABLE
OD	OUTPUT DISABLE
DO_1 - DO_4	DATA OUTPUT
V_{CC}	POWER (+5 V)

Order Number MM2101D, MM2101-1D or MM2101-2D
See Package 5

Order Number MM2101-N, MM2101-1N or MM2101-2N
See Package 17

absolute maximum ratings

Ambient Temperature Under Bias	0°C to +70°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin With Respect to Ground	-0.5 V to +7 V
Power Dissipation	1 Watt

dc electrical characteristics $T_A = 0°C$ to $+70°C$, $V_{CC} = 5\ V \pm 5\%$ unless otherwise specified.

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
I_{LI}	Input Current			10	μA	V_{IN} = 0 to 5.25 V
I_{LOH}	I/O Leakage Current[2]			15	μA	$\overline{CE1}$ = 2.2 V, V_{OUT} = 4.0 V
I_{LOL}	I/O Leakage Current[2]			-50	μA	$\overline{CE1}$ = 2.2 V, V_{OUT} = 0.45 V
I_{CC1}	Power Supply Current		30	60	mA	V_{IN} = 5.25 V, I_O = 0 mA, $T_A = 25°C$
I_{CC2}	Power Supply Current			70	mA	V_{IN} = 5.25 V, I_O = 0 mA, $T_A = 0°C$
V_{IL}	Input "Low" Voltage	-0.5		+0.65	V	
V_{IH}	Input "High" Voltage	2.2		V_{CC}	V	
V_{OL}	Output "Low" Voltage			+0.45	V	I_{OL} = 2.0 mA
V_{OH}	Output "High" Voltage	2.2			V	I_{OH} = -150 μA

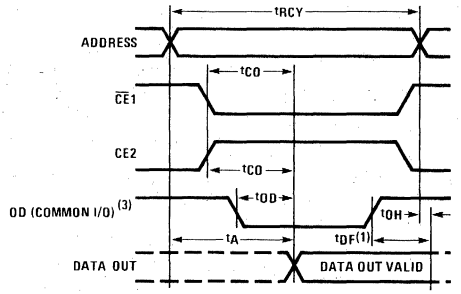
Note 1: Typical values are for $T_A = 25°C$ and nominal supply voltage.
Note 2: Input and Output tied together.

capacitance $T_A = 25°C$, f = 1 MHz

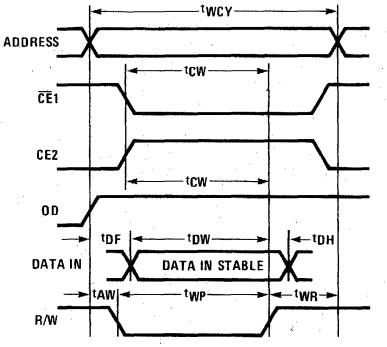
Symbol	Test	Limits (pF)	
		Typ.	Max.
C_{IN}	Input Capacitance (All Input Pins) V_{IN} = 0 V	4	8
C_{OUT}	Output Capacitance V_{OUT} = 0 V	8	12

switching time waveforms

READ CYCLE (R/W = "1")



WRITE CYCLE[2]



Note 1: t_{DF} is with respect to the trailing edge of $\overline{CE1}$, CE2, or OD, whichever occurs first.
Note 2: During the write cycle, OD is a logical 1 for common I/O and "don't care" for separate I/O operation.
Note 3: OD should be tied low for separate I/O operation.

ac electrical characteristics $T_A = 0°C$ to $+70°C$, $V_{CC} = 5\ V \pm 5\%$, unless otherwise specified.

MM2101

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
READ CYCLE						
t_{RCY}	Read Cycle	1,000			ns	Input Pulse Levels: +0.65 to +2.2 V
t_A	Access Time			1,000	ns	Input Pulse Rise and Fall Times:
t_{CO}	Chip Enable to Output			800	ns	20 ns
t_{OD}	Output Disable to Output			700	ns	Timing Measurement Reference
t_{DF}[1]	Data Output to High Z State	0		200	ns	Level: 1.5 V
t_{OH}	Previous Data Read Valid after change of Address	0			ns	Output Load: 1 TTL Gate and $C_L = 100\ pF$
WRITE CYCLE						
t_{WCY}	Write Cycle	1,000			ns	Input Pulse Levels: +0.65 to +2.2 V
t_{AW}	Write Delay	150			ns	Input Pulse Rise and Fall Times:
t_{CW}	Chip Enable to Write	900			ns	20 ns
t_{DW}	Data Setup	700			ns	Timing Measurement Reference
t_{DH}	Data Hold	100			ns	Level: 1.5 V
t_{WP}	Write Pulse	750			ns	Output Load: 1 TTL Gate and
t_{WR}	Write Recovery	50			ns	$C_L = 100\ pF$

MM2101-1 (500 ns Access Time)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
READ CYCLE						
t_{RCY}	Read Cycle	500			ns	Input Pulse Levels: +0.65 to +2.2 V
t_A	Access Time			500	ns	Input Pulse Rise and Fall Times:
t_{CO}	Chip Enable to Output			350	ns	20 ns
t_{OD}	Output Disable to Output			300	ns	Timing Measurement Reference
t_{DF}[1]	Data Output to High Z State	0		150	ns	Level: 1.5 V
t_{OH}	Previous Data Read Valid after change of Address	0			ns	Output Load: 1 TTL Gate and $C_L = 100\ pF$
WRITE CYCLE						
t_{WCY}	Write Cycle	500			ns	Input Pulse Levels: +0.65 to +2.2 V
t_{AW}	Write Delay	100			ns	Input Pulse Rise and Fall Times:
t_{CW}	Chip Enable to Write	400			ns	20 ns
t_{DW}	Data Setup	280			ns	Timing Measurement Reference
t_{DH}	Data Hold	100			ns	Level: 1.5 V
t_{WP}	Write Pulse	300			ns	Output Load: 1 TTL Gate and
t_{WR}	Write Recovery	50			ns	$C_L = 100\ pF$

MM2101-2 (650 ns Access Time)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
READ CYCLE						
t_{RCY}	Read Cycle	650			ns	Input Pulse Levels: +0.65 to +2.2 V
t_A	Access Time			650	ns	Input Pulse Rise and Fall Times:
t_{CO}	Chip Enable to Output			400	ns	20 ns
t_{OD}	Output Disable to Output			350	ns	Timing Measurement Reference
t_{DF}[1]	Data Output to High Z State	0		150	ns	Level: 1.5 V
t_{OH}	Previous Data Read Valid after change of Address	0			ns	Output Load: 1 TTL Gate and $C_L = 100\ pF$
WRITE CYCLE						
t_{WCY}	Write Cycle	650			ns	Input Pulse Levels: +0.65 to +2.2 V
t_{AW}	Write Delay	150			ns	Input Pulse Rise and Fall Times:
t_{CW}	Chip Enable to Write	550			ns	20 ns
t_{DW}	Data Setup	400			ns	Timing Measurement Reference
t_{DH}	Data Hold	100			ns	Level: 1.5 V
t_{WP}	Write Pulse	400			ns	Output Load: 1 TTL Gate and
t_{WR}	Write Recovery	50			ns	$C_L = 100\ pF$

Note 1: t_{DF} is with respect to the trailing edge of $\overline{CE1}$, CE2, or OD, whichever occurs first.

NATIONAL

MOS RAMs

MM2102, MM2102-1, MM2102-2
1024-bit fully decoded static random access memories

general description

The MM2102 family of 1024 word by one bit static random access read write memories are manufactured using N-channel enhancement mode silicon gate technology. Static storage cells eliminate the need for clocks and refresh. Data in and data out have the same polarity and the read operation is nondestructive.

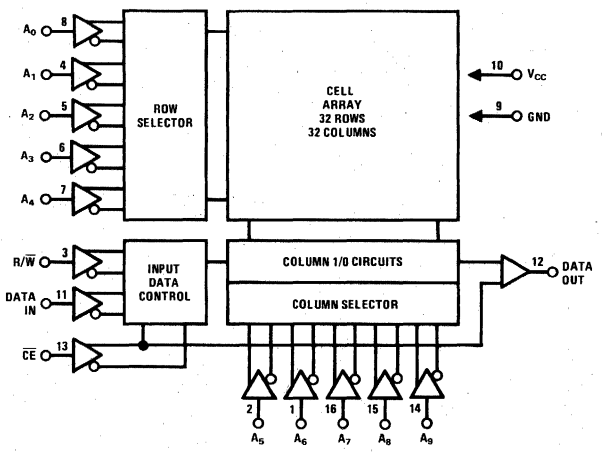
Low threshold silicon gate N-channel technology allows complete DTL/TTL compatibility of all inputs and outputs as well as a single +5V supply. The separate chip enable input ($\overline{CE}$) controlling the TRI-STATE® output allows easy memory expansion by OR-tying individual devices to a data bus.

The simple interface and high performance make the MM2102 family ideally suited for those applications, for large and small storage capacity, where cost is an important design consideration.

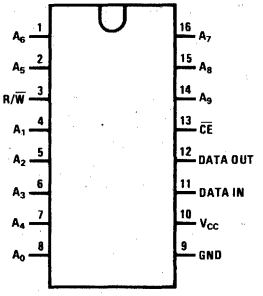
features

- Single +5V supply
- All inputs and output directly DTL/TTL compatible
- Static operation—no clocks or refreshing required
- Low power 150 mW typ
- Fast access
  - MM2102 1μs
  - MM2102-1 500 ns
  - MM2102-2 650 ns
- TRI-STATE output for bus interface
- Chip enable allows simple memory expansion
- On chip address decode
- All inputs protected against static discharge
- Low cost 16-pin Epoxy B package

block and connection diagrams



Dual-In-Line Package



TOP VIEW

Order Number MM2102D, MM2102-1D or MM2102-2D
See Package 3

Order Number MM2102N, MM2102-1N or MM2102-2N
See Package 15

absolute maximum ratings (Note 1)

Voltage at Any Pin	−0.5V to +7.0V
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Power Dissipation	1W
Lead Temperature (Soldering, 10 seconds)	300°C

dc electrical characteristics

(T_A within operating temperature range, V_{CC} = 5V ±5%, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Logical "1" Input Voltage (V_{IH})		2.2		V_{CC}	V
Logical "0" Input Voltage (V_{IL})		−0.5		0.65	V
Logical "1" Output Voltage (V_{OH})	I_{OH} = −100μA	2.2			V
Logical "0" Output Voltage (V_{OL})	I_{OL} = 1.9 mA			0.45	V
Input Load Current (I_{LI})	V_{IN} = 0 to 5.25V			10	μA
Output Leakage Current (I_{LOH})	$\overline{CE}$ = 2.2V, V_{OUT} = 4.0V			10	μA
Output Leakage Current (I_{LOL})	$\overline{CE}$ = 2.2V, V_{OUT} = 0.45V			−100	μA
Power Supply Current (I_{CC1})	All Inputs = 5.25V, Data Out Open, T_A = 25°C		30	60	mA
Power Supply Current (I_{CC2})	All Inputs = 5.25V, Data Out Open, T_A = 0°C			70	mA

ac electrical characteristics

(T_A within operating temperature range, V_{CC} = 5V ±5%, unless otherwise specified.)
See ac test circuit and switching time waveforms.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
READ CYCLE					
Read Cycle (t_{RC})					
MM2102	R/$\overline{W}$ = V_{IH}	1000			ns
MM2102-1	R/$\overline{W}$ = V_{IH}	500			ns
MM2102-2	R/$\overline{W}$ = V_{IH}	650			ns
Access Time (t_A)					
MM2102				1000	ns
MM2102-1				500	ns
MM2102-2				650	ns
Chip Enable to Output Time (t_{CO})					
MM2102				500	ns
MM2102-1				350	ns
MM2102-2				400	ns
Previous Read Data Valid with Respect to Address (t_{OH1})		50			ns
Previous Read Data Valid with Respect to Chip, Enable (t_{OH2})		0			ns

ac electrical characteristics (con't)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
WRITE CYCLE					
Write Cycle (t_{WC})					
MM2102		1000			ns
MM2102-1		500			ns
MM2102-2		650			ns
Address to Write Set-up Time (t_{AW})					
MM2102		200			ns
MM2102-1		150			ns
MM2102-2		200			ns
Write Pulse Width (t_{WP})					
MM2102		750			ns
MM2102-1		300			ns
MM2102-2		400			ns
Write Recovery Time (t_{WR})		50			ns
Data Set-up Time (t_{DW})					
MM2102		800			ns
MM2102-1		330			ns
MM2102-2		450			ns
Data Hold Time (t_{DH})		100			ns
Chip Enable to Write Set-up Time (t_{CW})					
MM2102		900			ns
MM2102-1		400			ns
MM2102-2		550			ns
CAPACITANCE					
Input Capacitance (All Inputs) (C_{IN}) (Note 4)	V_{IN} = 0V, T_A = 25°C, f = 1.0 MHz (Note 2)		3.0	5.0	pF
Output Capacitance (C_{OUT}) (Note 4)	V_{OUT} = 0V, T_A = 25°C, f = 1.0 MHz (Note 2)		7.0	10.0	pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

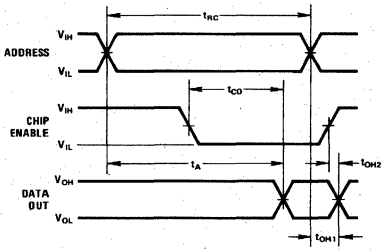
Note 2: Capacitance is guaranteed by periodic testing.

Note 3: Positive true logic notation is used: Logical "1" = most positive voltage level, Logical "0" = most negative voltage level.

Note 4: Typical values are for T_A = 25°C and nominal supply voltage.

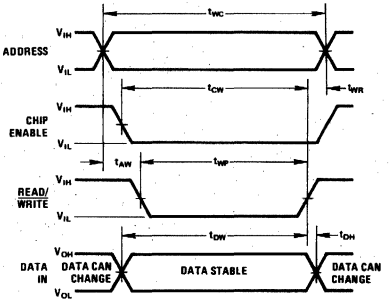
switching time waveforms

Read Cycle

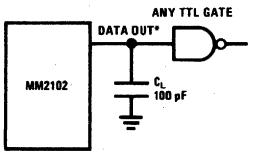


Note: All times measured with respect to 1.5V level with t_r and $t_f \leq 20$ ns.

Write Cycle



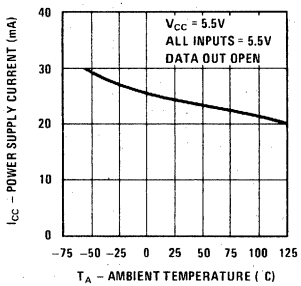
ac test circuit



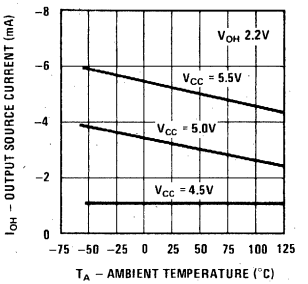
*Delay times measured at MM2102 output.

typical performance characteristics

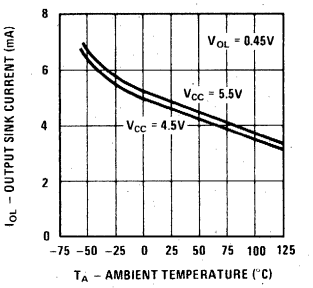
Power Supply Current vs Temperature



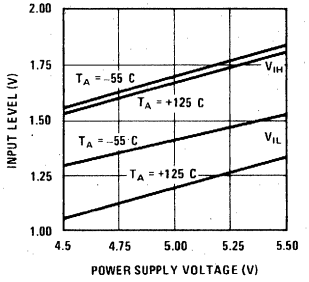
Output Source Current vs Temperature



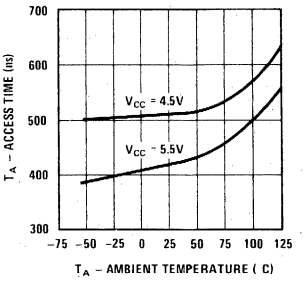
Output Sink Current vs Temperature



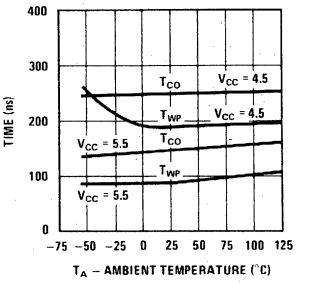
Input Levels vs Power Supply Voltage



Access Time vs Temperature



Write Pulse Width and Chip Enable—To Output Delay vs Temperature



NATIONAL

MOS RAMs

MM2102MD, MM2102-2MD military temperature range 1024-bit fully decoded static random access memories

general description

The MM2102 family of 1024 word by one bit static random access read write memories are manufactured using N-channel enhancement mode silicon gate technology. Static storage cells eliminate the need for clocks and refresh. Data in and data out have the same polarity and the read operation is nondestructive.

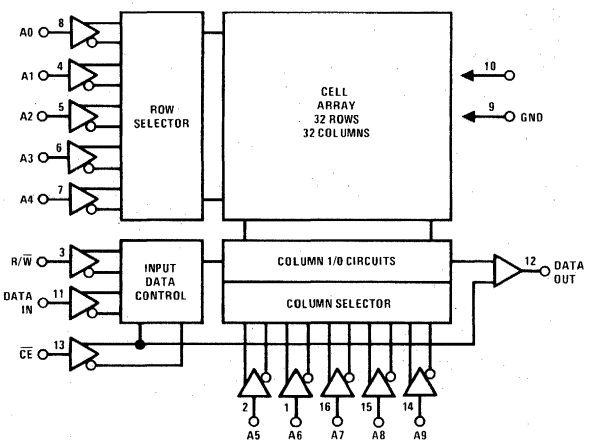
Low threshold silicon gate N-channel technology allows complete DTL/TTL compatibility of all inputs and outputs as well as a single +5V supply. The separate chip enable input ($\overline{CE}$) controlling the TRI-STATE® output allows easy memory expansion by OR-tying individual devices to a data bus.

The simple interface and high performance make the MM2102 family ideally suited for those applications, for large and small storage capacity, where cost is an important design consideration.

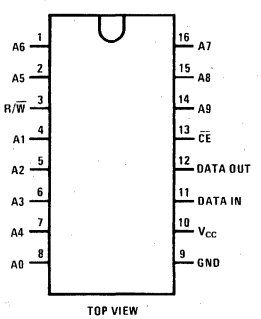
features

- Single +5V supply
- All inputs and output directly DTL/TTL compatible
- Static operation—no clocks or refreshing required
- Low power 150 mW typ
- Fast Access
  - MM2102 1μs
  - MM2102-2 650 ns
- TRI-STATE output for bus interface
- Chip enable allows simple memory expansion
- On chip address decode
- All inputs protected against static discharge
- −55°C to +125°C Operation

block and connection diagrams



Dual-In-Line Package



TOP VIEW

Order Number MM2102MD or MM2102-2MD
See Package 3

absolute maximum ratings (Note 1)

Voltage at Any Pin	−0.5V to +7.0V
Operating Temperature Range	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Power Dissipation	1W
Lead Temperature (Soldering, 10 seconds)	300°C

dc electrical characteristics

(T_A within operating temperature range, V_{CC} = 5V ±10%, unless otherwise noted.)

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{IH}	Logical "1" Input Voltage		2.2		V_{CC}	V
V_{IL}	Logical "0" Input Voltage		−0.5		0.65	V
V_{OH}	Logical "1" Output Voltage	I_{OH} = −100μA	2.2			V
V_{OL}	Logical "0" Output Voltage	I_{OL} = 2.1 mA			0.45	V
I_{LI}	Input Load Current	V_{IN} = 0 to 5.5V			10	μA
I_{LOH}	Output Leakage Current	$\overline{CE}$ = 2.2V, V_{OUT} = 4.0V			10	μA
I_{LOL}	Output Leakage Current	$\overline{CE}$ = 2.2V, V_{OUT} = 0.45V			−50	μA
I_{CC1}	Power Supply Current	All Inputs = 5.5V, Data Out Open, T_A = 25°C, (Note 4)		25	45	mA
I_{CC2}	Power Supply Current	All Inputs = 5.5V, Data Out Open, T_A = −55°C to +125°C			55	mA

ac electrical characteristics

(T_A within operating temperature range, V_{CC} = 5V ±10%, unless otherwise specified.)
See ac test circuit and switching time waveforms.

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
READ CYCLE						
t_{RC}	Read Cycle					
	MM2102	$R/\overline{W}$ = V_{IH}	1000			ns
	MM2102-2	$R/\overline{W}$ = V_{IH}	650			ns
t_A	Access Time					
	MM2102				1000	ns
	MM2102-2				650	ns
t_{CO}	Chip Enable to Output Time					
	MM2102				500	ns
	MM2102-2				400	ns
t_{OH1}	Previous Read Data Valid with Respect to Address		50			ns
t_{OH2}	Previous Read Data Valid with Respect to Chip, Enable		0			ns

ac electrical characteristics (con't)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
WRITE CYCLE						
t_{WC}	Write Cycle					
	MM2102		1000			ns
	MM2102-2		650			ns
t_{AW}	Address to Write Set-Up Time					
	MM2102		200			ns
	MM2102-2		200			ns
t_{WP}	Write Pulse Width					
	MM2102		750			ns
	MM2102-2		400			ns
t_{WR}	Write Recovery Time		50			ns
t_{DW}	Data Set-Up Time					
	MM2102		800			ns
	MM2102-2		450			ns
t_{DH}	Data Hold Time		100			ns
t_{CW}	Chip Enable to Write Set-Up Time					
	MM2102		900			ns
	MM2102-2		550			ns
CAPACITANCE						
C_{IN}	Input Capacitance (All Inputs)	V_{IN} = 0V, T_A = 25°C, f = 1.0 MHz (Notes 2 and 4)		3	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V, T_A = 25°C, f = 1.0 MHz (Notes 2 and 4)		7	10	pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

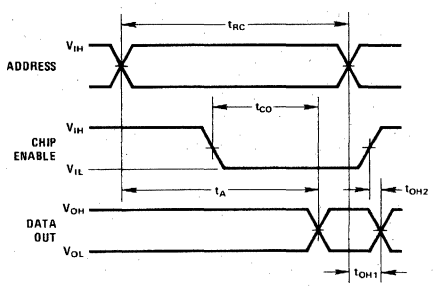
Note 2: Capacitance is guaranteed by periodic testing.

Note 3: Positive true logic notation is used: Logical "1" = most positive voltage level, Logical "0" = most negative voltage level.

Note 4: Typical values are for T_A = 25°C and nominal supply voltage.

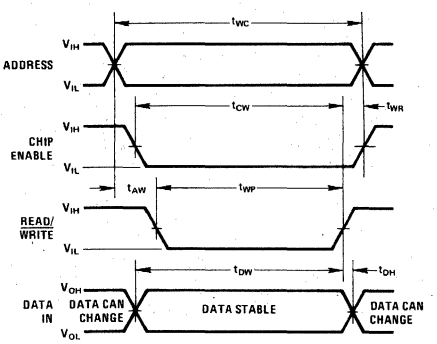
switching time waveforms

Read Cycle

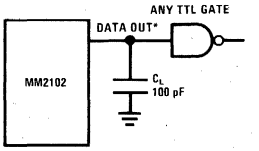


Note: All times measured with respect to 1.5V level with t_r and $t_f \leq 20$ ns.

Write Cycle



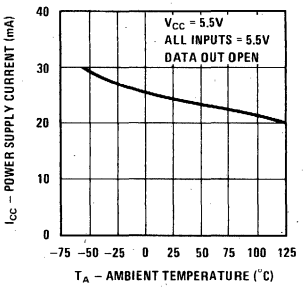
ac test circuit



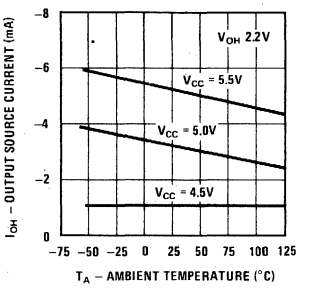
*Delay times measured at MM2102 output.

typical performance characteristics

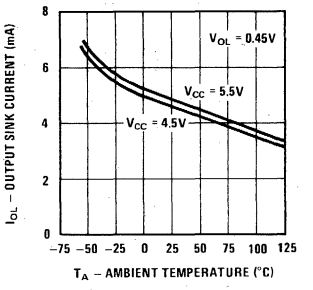
Power Supply Current vs Temperature



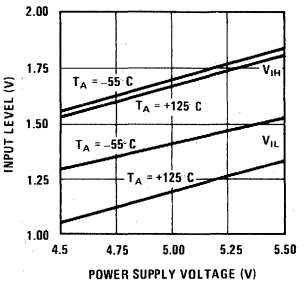
Output Source Current vs Temperature



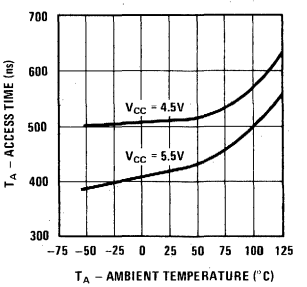
Output Sink Current vs Temperature



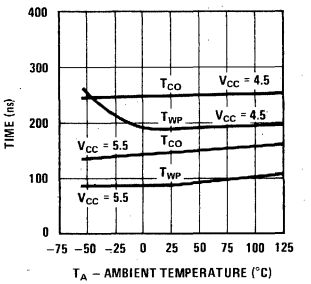
Input Levels vs Power Supply Voltage



Access Time vs Temperature



Write Pulse Width and Chip Enable–To Output Delay vs Temperature



NATIONAL

MOS RAMs

MM2111, MM2111-1, MM2111-2 1024-bit (256 × 4) static MOS RAM with common I/O and output disable

general description

The National MM2111 is a 256 by 4 static random access memory element fabricated using N-channel enhancement mode Silicon Gate technology. Static storage cells eliminate the need for refresh and the peripheral circuitry associated with refresh. The data is read out nondestructively and has the same polarity as the input data. Common Data Input/Output pins are provided.

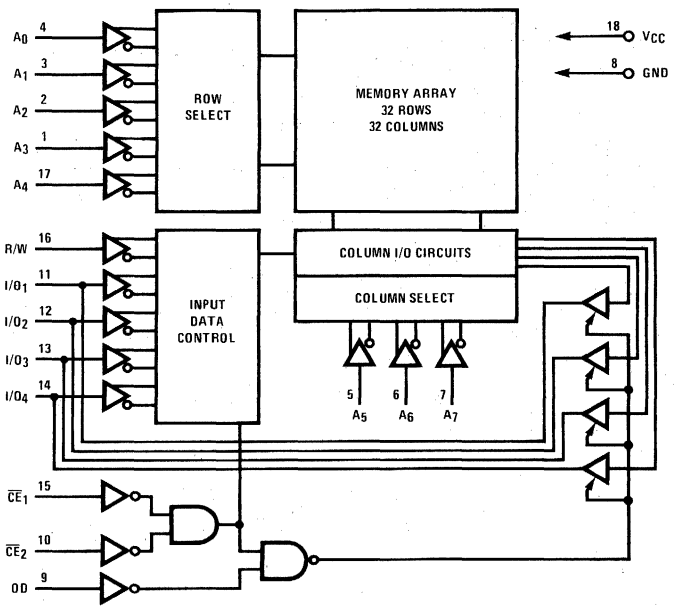
The 2111 is directly TTL in all respects: inputs, outputs and a single +5 V supply. The two Chip-enables allow easy selection of an individual package when outputs are OR-tied. The features of this memory device can be combined to make a low cost, high performance, and easy to manufacture memory system.

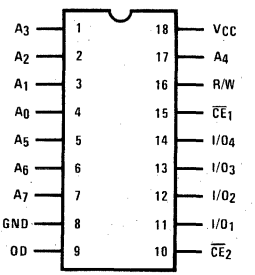
National's silicon gate technology provides excellent protection against contamination and permits the use of low cost Epoxy B packaging.

features

- Organization 256 Words by 4 Bits
- Common Data Input and Output
- Single +5 V Supply Voltage
- Directly TTL Compatible — All Inputs and Outputs
- Static MOS — No Clocks or Refreshing Required
- Access Time — 0.5 to 1.0 μs Max.
- Simple Memory Expansion — Chip Enable Input
- Low Cost Packaging — 18 Pin Epoxy B Dual-In-Line Configuration
- Low Power — Typically 150 mW
- Tri-State ® Output — OR-Tie Capability

block and connection diagrams





PIN NAMES

A_0-A_7	ADDRESS INPUTS
OD	OUTPUT DISABLE
R/W	READ/WRITE INPUT
$\overline{CE}1$	CHIP ENABLE 1
$\overline{CE}2$	CHIP ENABLE 2
I/O_1-I/O_4	DATA INPUT/OUTPUT

Order Number MM2111D, MM2111-1D or MM2111-2D
See Package 4

Order Number MM2111N, MM2111-1N or MM2111-2N
See Package 16

absolute maximum ratings

Ambient Temperature Under Bias	0°C to +70°C
Storage Temperature	-65°C to +150°C
Voltage On Any Pin With Respect to Ground	-0.5 V to +7 V
Power Dissipation	1 Watt

dc electrical characteristics $T_A = 0°C$ to $+70°C$, $V_{CC} = 5\ V \pm 5\%$, unless otherwise specified.

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
I_{LI}	Input Current			10	μA	$V_{IN} = 0$ to 5.25 V
I_{LOH}	I/O Leakage Current[2]			15	μA	$\overline{CE} = 2.2\ V$, $V_{I/O} = 4.0\ V$
I_{LOL}	I/O Leakage Current[2]			-50	μA	$\overline{CE} = 2.2\ V$, $V_{I/O} = 0.45\ V$
I_{CC1}	Power Supply Current		30	60	mA	$V_{IN} = 5.25\ V$, $I_{I/O} = 0\ mA$, $T_A = 25°C$
I_{CC2}	Power Supply Current			70	mA	$V_{IN} = 5.25\ V$, $I_{I/O} = 0\ mA$, $T_A = 0°C$
V_{IL}	Input "Low" Voltage	-0.5		+0.65	V	
V_{IH}	Input "High" Voltage	2.2		V_{CC}	V	
V_{OL}	Output "Low" Voltage			+0.45	V	$I_{OL} = 2.0\ mA$
V_{OH}	Output "High" Voltage	2.2			V	$I_{OH} = -150\ \mu A$

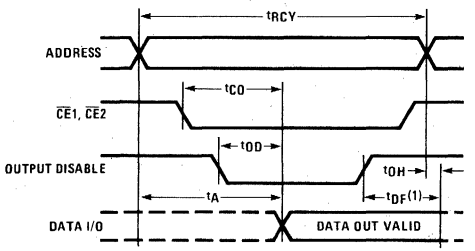
Note 1: Typical values are for $T_A = 25°C$ and nominal supply voltage.

capacitance $T_A = 25°C$, $f = 1\ MHz$

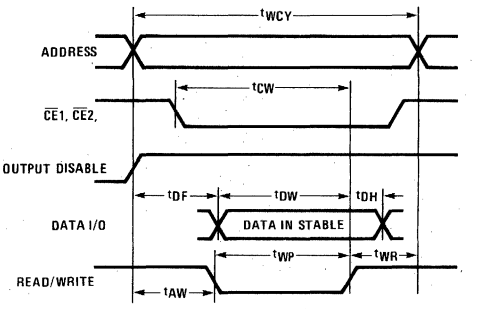
Symbol	Test	Limits (pF)	
		Typ.	Max.
C_{IN}	Input Capacitance (All Input Pins) $V_{IN} = 0\ V$	4	8
$C_{I/O}$	I/O Capacitance $V_{I/O} = 0\ V$	10	15

switching time waveforms

READ CYCLE (R/W = "1")



WRITE CYCLE



Note 1: t_{DF} is with respect to the trailing edge of $\overline{CE}1$, $\overline{CE}2$, or OD, whichever occurs first.

ac electrical characteristics

T_A = 0°C to +70°C, V_{CC} = 5 V ± 5%, unless otherwise specified.

MM2111

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
READ CYCLE						
t_{RCY}	Read Cycle	1,000			ns	Input Pulse Levels: +0.65 to +2.2 V
t_A	Access Time			1,000	ns	Input Pulse Rise and Fall Times:
t_{CO}	Chip Enable to Output			800	ns	20 ns
t_{OD}	Output Disable to Output			700	ns	Timing Measurement Reference
t_{DF}[1]	Data Output to High Z State	0		200	ns	Level: 1.5 V
t_{OH}	Previous Data Read Valid after change of Address	0			ns	Output Load: 1 TTL Gate and C_L = 100 pF
WRITE CYCLE						
t_{WCY}	Write Cycle	1,000			ns	Input Pulse Levels: +0.65 to +2.2 V
t_{AW}	Write Delay	150			ns	Input Pulse Rise and Fall Times:
t_{CW}	Chip Enable to Write	900			ns	20 ns
t_{DW}	Data Setup	700			ns	Timing Measurement Reference
t_{DH}	Data Hold	100			ns	Level: 1.5 V
t_{WP}	Write Pulse	750			ns	Output Load: 1 TTL Gate and
t_{WR}	Write Recovery	50			ns	C_L = 100 pF

MM2111-1 (500 ns Access Time)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
READ CYCLE						
t_{RCY}	Read Cycle	500			ns	Input Pulse Levels: +0.65 to +2.2 V
t_A	Access Time			500	ns	Input Pulse Rise and Fall Times:
t_{CO}	Chip Enable to Output			350	ns	20 ns
t_{OD}	Output Disable to Output			300	ns	Timing Measurement Reference
t_{DF}[1]	Data Output to High Z State	0		150	ns	Level: 1.5 V
t_{OH}	Previous Data Read Valid after change of Address	0			ns	Output Load: 1 TTL Gate and C_L = 100 pF
WRITE CYCLE						
t_{WCY}	Write Cycle	500			ns	Input Pulse Levels: +0.65 to +2.2 V
t_{AW}	Write Delay	100			ns	Input Pulse Rise and Fall Times:
t_{CW}	Chip Enable to Write	400			ns	20 ns
t_{DW}	Data Setup	280			ns	Timing Measurement Reference
t_{DH}	Data Hold	100			ns	Level: 1.5 V
t_{WP}	Write Pulse	300			ns	Output Load: 1 TTL Gate and
t_{WR}	Write Recovery	50			ns	C_L = 100 pF

MM2111-2 (650 ns Access Time)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
READ CYCLE						
t_{RCY}	Read Cycle	650			ns	Input Pulse Levels: +0.65 to +2.2 V
t_A	Access Time			650	ns	Input Pulse Rise and Fall Times:
t_{CO}	Chip Enable to Output			400	ns	20 ns
t_{OD}	Output Disable to Output			350	ns	Timing Measurement Reference
t_{DF}[1]	Data Output to High Z State	0		150	ns	Level: 1.5 V
t_{OH}	Previous Data Read Valid after change of Address	0			ns	Output Load: 1 TTL Gate and C_L = 100 pF
WRITE CYCLE						
t_{WCY}	Write Cycle	650			ns	Input Pulse Levels: +0.65 to +2.2 V
t_{AW}	Write Delay	150			ns	Input Pulse Rise and Fall Times:
t_{CW}	Chip Enable to Write	550			ns	20 ns
t_{DW}	Data Setup	400			ns	Timing Measurement Reference
t_{DH}	Data Hold	100			ns	Level: 1.5 V
t_{WP}	Write Pulse	400			ns	Output Load: 1 TTL Gate and
t_{WR}	Write Recovery	50			ns	C_L = 100 pF

MOS RAMs

MM2112, MM2112-2 1024-bit (256 × 4) static MOS RAM with common data I/O

general description

The National MM2112 is a 256 by 4 static random access memory element fabricated using N-Channel enhancement mode Silicon Gate technology. Static storage cells eliminate the need for refresh and the peripheral circuitry associated with refresh. The data is read out nondestructively and has the same polarity as the input data. Common Data Input/Output pins are provided.

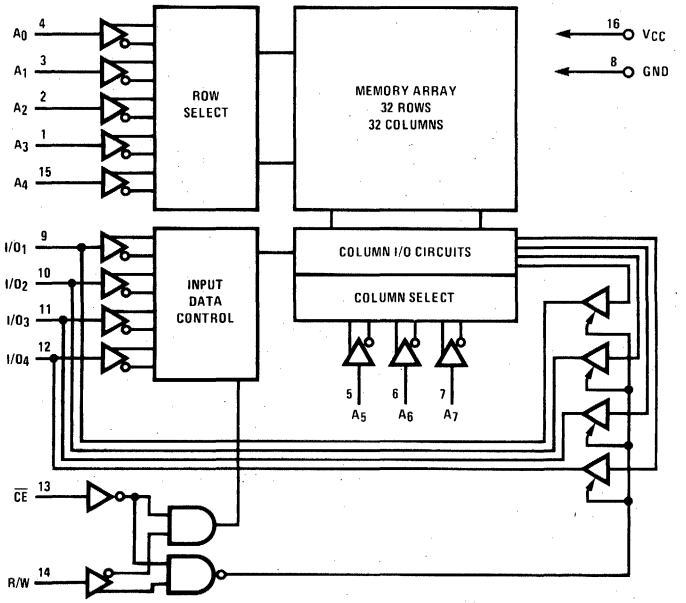
The MM2112 is directly TTL in all respects: inputs, outputs and a single +5 V supply. The Chip-enable allows easy selection of an individual package when outputs are OR-tied. The features of this memory device can be combined to make a low cost, high performance, and easy to manufacture memory system.

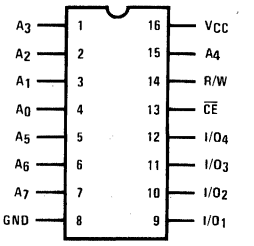
National's silicon gate technology provides excellent protection against contamination and permits the use of low cost Epoxy B packaging.

features

- Organization 256 Words by 4 Bits
- Common Data Input and Output
- Single +5 V Supply Voltage
- Directly TTL Compatible – All Inputs and Outputs
- Static MOS – No Clocks or Refreshing Required
- Access Time – 0.65 to 1 μs Max.
- Simple Memory Expansion – Chip Enable Input
- Low Cost Packaging – 16 Pin Epoxy B Dual-In-Line Configuration
- Low Power – Typically 150 mW
- Tri-State ® Output – OR-Tie Capability

block and connection diagrams





PIN NAMES

A_0-A_7	ADDRESS INPUTS
R/W	READ/WRITE INPUT
$\overline{CE}$	CHIP ENABLE INPUT
I/O_1-I/O_4	DATA INPUT/OUTPUT
V_{CC}	POWER (+5 V)

Order Number MM2112D or MM2112-2D
See Package 3

Order Number MM2112N or MM2112-2N
See Package 15

absolute maximum ratings

Ambient Temperature Under Bias	0°C to +70°C
Storage Temperature	-65°C to +150°C
Voltage On Any Pin With Respect to Ground	-0.5 V to +7 V
Power Dissipation	1 Watt

dc electrical characteristics

$T_A = 0°C$ to $+70°C$, $V_{CC} = 5\ V \pm 5\%$ unless otherwise specified.

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
I_{LI}	Input Current			10	μA	$V_{IN} = 0$ to 5.25 V
I_{LOH}	I/O Leakage Current			15	μA	$\overline{CE} = 2.2\ V$, $V_{I/O} = 4.0\ V$
I_{LOL}	I/O Leakage Current			-50	μA	$\overline{CE} = 2.2\ V$, $V_{I/O} = 0.45\ V$
I_{CC1}	Power Supply Current		30	60	mA	$V_{IN} = 5.25\ V$, $I_{I/O} = 0\ mA$, $T_A = 25°C$
I_{CC2}	Power Supply Current			70	mA	$V_{IN} = 5.25\ V$, $I_{I/O} = 0\ mA$, $T_A = 0°C$
V_{IL}	Input "Low" Voltage	-0.5		+0.65	V	
V_{IH}	Input "High" Voltage	2.2		V_{CC}	V	
V_{OL}	Output "Low" Voltage			+0.45	V	$I_{OL} = 2\ mA$
V_{OH}	Output "High" Voltage	2.2			V	$I_{OH} = -150\ \mu A$

Note 1: Typical values are for $T_A = 25°C$ and nominal supply voltage.

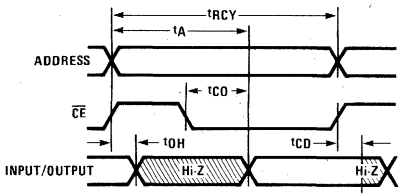
capacitance

$T_A = 25°C$, f = 1 MHz

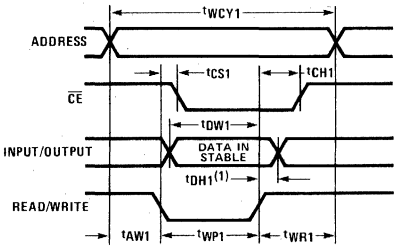
Symbol	Test	Limits (pF)	
		Typ.	Max.
C_{IN}	Input Capacitance (All Input Pins) $V_{IN} = 0\ V$	4	8
$C_{I/O}$	I/O Capacitance $V_{I/O} = 0\ V$	10	18

switching time waveforms

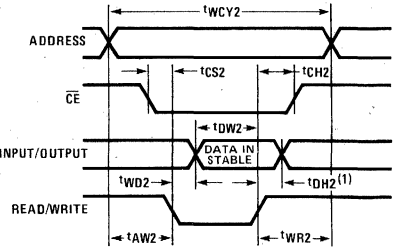
READ CYCLE (R/W = "1")



WRITE CYCLE #1



WRITE CYCLE #2



Note 1: Data Hold Time (T_{OH}) is referenced to the trailing edge of CHIP ENABLE ($\overline{CE}$) or READ/WRITE (R/W) whichever comes first.

ac electrical characteristics $T_A = 0°C$ to $+70°C$, $V_{CC} = 5\ V \pm 5\%$ unless otherwise specified.

MM2112

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
READ CYCLE						
t_{RCY}	Read Cycle	1,000			ns	Input Pulse Levels: +0.65 to +2.2 V
t_A	Access Time			1,000	ns	Input Pulse Rise and Fall Times: 20 ns
t_{CO}	Chip Enable to Output Time			800	ns	Timing Measurement Reference Level: 1.5 V
t_{CD}	Chip Enable to Output Disable Time	0		200	ns	Output Load: 1 TTL Gate and $C_L = 100\ pF$
t_{OH}	Previous Read Data Valid After Change of Address	50			ns	
WRITE CYCLE #1						
t_{WCY1}	Write Cycle	850			ns	
t_{AW1}	Address to Write Setup Time	150			ns	Input Pulse Levels: +0.65 to +2.2 V
t_{DW1}	Write Setup Time	650			ns	Input Pulse Rise and Fall Times: 20 ns
t_{WP1}	Write Pulse Width	650			ns	Timing Measurement Reference Level: 1.5 V
t_{CS1}	Chip Enable Setup Time	0		100	ns	Output Load: 1 TTL Gate and $C_L = 100\ pF$
t_{CH1}	Chip Enable Hold Time	0			ns	
t_{WR1}	Write Recovery Time	50			ns	
t_{DH1}	Data Hold Time	100			ns	
WRITE CYCLE #2						
t_{WCY2}	Write Cycle	1,050			ns	
t_{AW2}	Address to Write Setup Time	150			ns	Input Pulse Levels: +0.65 to +2.2 V
t_{DW2}	Write Setup Time	650			ns	Input Pulse Rise and Fall Times: 20 ns
t_{WD2}	Write to Output Disable Time	200			ns	Timing Measurement Reference Level: 1.5 V
t_{CS2}	Chip Enable Setup Time	0			ns	Output Load: 1 TTL Gate and $C_L = 100\ pF$
t_{CH2}	Chip Enable Hold Time	0			ns	
t_{WR2}	Write Recovery Time	50			ns	
t_{DH2}	Data Hold Time	100			ns	

MM2112-2 (650 ns Access Time)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
READ CYCLE						
t_{RCY}	Read Cycle	650			ns	Input Pulse Levels: +0.65 to +2.2 V
t_A	Access Time			650	ns	Input Pulse Rise and Fall Times: 20 ns
t_{CO}	Chip Enable to Output Time			500	ns	Timing Measurement Reference Level: 1.5 V
t_{CD}	Chip Enable to Output Disable Time	0		150	ns	Output Load: 1 TTL Gate and $C_L = 100\ pF$
t_{OH}	Previous Read Data Valid After Change of Address	50			ns	
WRITE CYCLE #1						
t_{WCY1}	Write Cycle	500			ns	
t_{AW1}	Address to Write Setup Time	100			ns	Input Pulse Levels: +0.65 to +2.2 V
t_{DW1}	Write Setup Time	350			ns	Input Pulse Rise and Fall Times: 20 ns
t_{WO1}	Write Pulse Width	350			ns	Timing Measurement Reference Level: 1.5 V
t_{CS1}	Chip Enable Setup Time	0		50	ns	Output Load: 1 TTL Gate and $C_L = 100\ pF$
t_{CH1}	Chip Enable Hold Time	0			ns	
t_{WR1}	Write Recovery Time	50			ns	
t_{DH1}	Data Hold Time	50			ns	
WRITE CYCLE #2						
t_{WCY2}	Write Cycle	700			ns	
t_{AW2}	Address to Write Setup Time	100			ns	Input Pulse Levels: +0.65 to +2.2 V
t_{DW2}	Write Setup Time	350			ns	Input Pulse Rise and Fall Times: 20 ns
t_{WD2}	Write to Output Disable Time	200			ns	Timing Measurement Reference Level: 1.5 V
t_{CS2}	Chip Enable Setup Time	0			ns	Output Load: 1 TTL Gate and $C_L = 100\ pF$
t_{CH2}	Chip Enable Hold Time	0			ns	
t_{WR2}	Write Recovery Time	50			ns	
t_{DH2}	Data Hold Time	50			ns	

NATIONAL

MOS RAMs

MM4261/MM5261 1024-bit fully decoded dynamic random access memory

general description

The MM4261/MM5261 fully decoded dynamic 1024 word x 1-bit word read/write Random Access Memory is a monolithic MOS integrated circuit using silicon gate low threshold technology to achieve bipolar compatibility on all I/O lines except the precharge and read/write lines. This provides an efficient approach to memory design using these systems oriented devices. The MM4261/MM5261 is used for main memory applications where large bit storage and improved operating performance are important. A TRI-STATE® output is utilized to allow wired "OR" capability and common I/O data busing in memory applications.

features

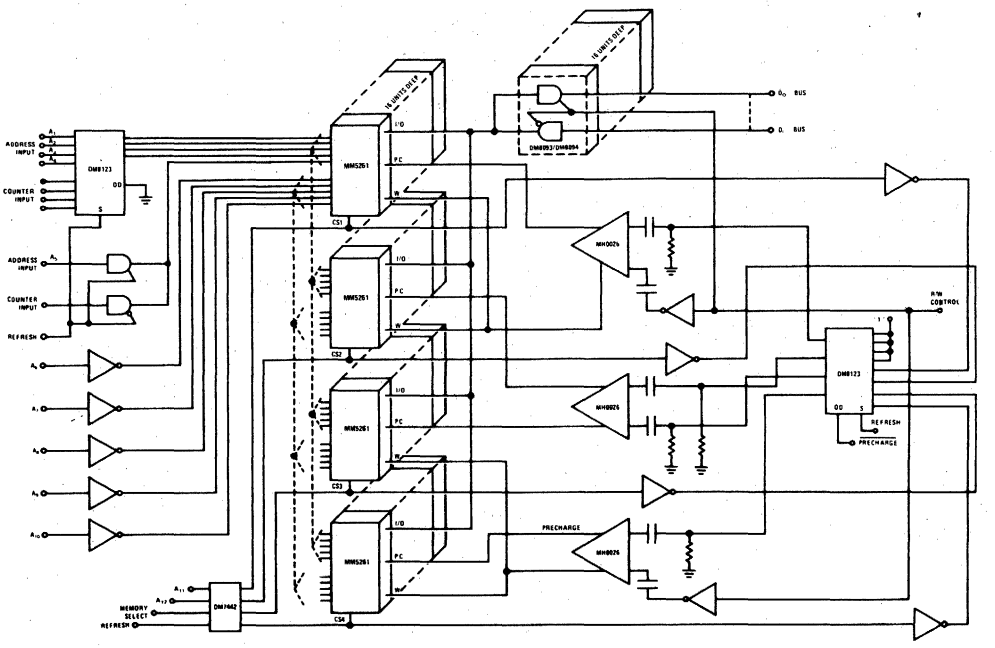
- Fast access time 300 typ
- Fast cycle time MM4261 600 ns read cycle min
  MM5261 500 ns read cycle min
  MM4261 750 ns write cycle min
  MM5261 625 ns write cycle min
- Low overhead circuit count Fully decoded
- Systems-oriented design
  Bipolar compatible (address lines, chip enable data I/O)
  Common data I/O line
  TRI-STATE output
- Refresh cycle 2.0 ms
- Easy memory expansion Chip enable
- Device protection All I/O lines have protection against static charge
- Low power dissipation 400 mW
- Small package size 18 pin dual-in-line package

applications

- High speed mainframe memory
- Mass memory storage

typical application

Main Memory Module Storing 4096 16-Bit Words



absolute maximum ratings (Note 3)

All Input or Output Voltages With Respect to Most Positive Supply Voltage V_{BB}	+0.3V to −22V
Power Dissipation	700 mW
Operating Temperature Range	
MM5261	0°C to +70°C
MM4261	−55°C to +125°C
Storage Temperature Range	−65°C to +160°C
Lead Temperature (Soldering, 10 seconds)	300°C

dc operating characteristics (MM4261) $T_A = -55°C$ to $+125°C$,

$V_{SS} = +5.0V \pm 5\%$, $V_{DD} = -12V \pm 5\%$, $(V_{BB} - V_{SS}) = 1.5V$ to $2.0V$ (Note 2), unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage (Address Input, Chip Enable and Data Input)					
Logic "1" (V_{IH})		$V_{SS} - 2.0$		$V_{SS} + 0.7$	V
Logic "0" (V_{IL})				$V_{SS} - 4.2$	V
Input Voltage (Precharge and Read/Write)					
Logic "1" (V_{IH})		$V_{SS} - 1.5$		$V_{SS} + 0.7$	V
Logic "0" (V_{IL})		$V_{SS} - 15$		$V_{SS} - 18$	V
Output Voltage Data Output					
Logic "1" (V_{OH})	$I_L = 200\mu A$ Source	2.4			V
Logic "0" (V_{OL})	$I_L = 1.6$ mA Sink			0.4	V
Standby Current (Note 1)	No Clocks, $\overline{CE} = V_{IH}$		6.0	12	mA
Average Supply Current (I_{SS}) (Note 1)	$t_{PW} = 300$, $t_{RC} = 600$ ns		20	34	mA
V_{BB} Supply Current				100	μA

ac operating characteristics (MM4261) $T_A = -55°C$ to $+125°C$,

$V_{SS} = +5.0V \pm 5\%$, $V_{DD} = -12V \pm 5\%$, $(V_{BB} - V_{SS}) = 1.5V$ to $2.0V$ (Note 2), unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Read Cycle (t_{RC})		600			ns
Write Cycle (t_{WC})		750			ns
Read/Write Cycle (t_{RWC})		$t_{ACC} + t_D + t_{WP} + t_{WRP} - t_{AP}$			
Address to $\overline{\text{Chip Enable}}$ (t_{AC})		0		50	ns
Address to Precharge (t_{AP})		0		50	ns
Precharge Width (t_{PW})		300		450	ns
Address Hold Time (t_{AH})		50			ns
Chip Enable Hold Time (t_{CH})		110			ns
Access Time (t_{ACC})			350	450	ns
Precharge Off Time (t_{PP})		300			ns
Precharge Leading Edge to R/$\overline{W}$ Leading Edge (t_{PWL})		225			ns
Read/$\overline{\text{Write}}$ Pulse Width (t_{WP})		300		450	ns
Read/$\overline{\text{Write}}$ Trailing Edge to Precharge Leading Edge (t_{WRP})		225			ns
Precharge Trailing to R/$\overline{W}$ Trailing (t_{PTW})		225			ns
Precharge to R/$\overline{W}$ Delay (t_{PWD})				500	ns
Refresh Interval (t_{REF})	(Note 6)			1.0	ms

capacitance characteristics (MM4261) (Note 4)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Address Capacitance (C_A)	$V_{IN} = V_{SS}$		5.0	7.0	pF
Chip Enable Capacitance (C_{CE})	$V_{IN} = V_{SS}$		5.0	9.0	pF
Precharge Capacitance (C_{PC})	$V_{IN} = V_{SS}$		25	45	pF
Read/Write Capacitance (C_{RW})	$V_{IN} = V_{SS}$		10	20	pF
Data Input/Output Capacitance ($C_{IN/OUT}$)	$V_{IN} = V_{SS}$		7.0	9.0	pF

f = 1 MHz, All Unused Inputs Are at AC Ground

dc operating characteristics (MM5261) $T_A = 0°C$ to $+70°C$,

$V_{SS} = +5.0V \pm 5\%$, $V_{DD} = -12V \pm 5\%$, $(V_{BB} - V_{SS}) = 1.5V$ to $2.0V$ (Note 2), unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage (Address Input, Chip Enable and Data Input)					
Logic "1" (V_{IH})		$V_{SS} - 2.0$		$V_{SS} + 0.7$	V
Logic "0" (V_{IL})				$V_{SS} - 4.2$	V
Input Voltage (Precharge and Read/Write)					
Logic "1" (V_{IH})		$V_{SS} - 1.5$		$V_{SS} + 0.7$	V
Logic "0" (V_{IL})		$V_{SS} - 15$		$V_{SS} - 18$	V
Output Voltage Data Output					
Logic "1" (V_{OH})	$I_L = 200\mu A$ Source	2.4			V
Logic "0" (V_{OL})	$I_L = 1.6$ mA Sink			0.4	V
Standby Current (Note 1)	No Clocks, $\overline{CE} = V_{IH}$		6.0	12	mA
Average Supply Current (I_{SS}) (Note 1)	$t_{PW} = 250$ ns, $t_{RC} = 500$ ns		20	34	mA
V_{BB} Supply Current				100	μA

ac operating characteristics (MM5261) $T_A = 0°C$ to $+70°C$,

$V_{SS} = +5.0V \pm 5\%$, $V_{DD} = -12V \pm 5\%$, $(V_{BB} - V_{SS}) = 1.5V$ to $2.0V$ (Note 2), unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Read Cycle (t_{RC})		500			ns
Write Cycle (t_{WC})		625			ns
Read/Write Cycle (t_{RWC})		$t_{ACC} + t_D + t_{WP} + t_{WRP} - t_{AP}$			
Address to $\overline{\text{Chip Enable}}$ (t_{AC})		0		50	ns
Address to Precharge (t_{AP})		0		50	ns
Precharge Width (t_{PW})		250		400	ns
Address Hold Time (t_{AH})		50			ns
Chip Enable Hold Time (t_{CH})		110			ns
Access Time (t_{ACC})			300	400	ns
Precharge Off Time (t_{PP})		250			ns
Precharge Leading Edge to R/$\overline{W}$ Leading Edge (t_{PWL})		175			ns
Read/$\overline{\text{Write}}$ Pulse Width (t_{WP})		250		400	ns
Read/$\overline{\text{Write}}$ Trailing Edge to Precharge Leading Edge (t_{WRP})		200			ns
Precharge Trailing to R/$\overline{W}$ Trailing (t_{PTW})		175			ns
Precharge to R/$\overline{W}$ Delay (t_{PWD})				500	ns
Refresh Interval (t_{REF})	(Note 6)			2.0	ms

capacitance characteristics (MM5261) (Note 4)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Address Capacitance (C_A)	$V_{IN} = V_{SS}$		5.0	7.0	pF
Chip Enable Capacitance (C_{CE})	$V_{IN} = V_{SS}$		5.0	9.0	pF
Precharge Capacitance (C_{PC})	$V_{IN} = V_{SS}$		25	45	pF
Read/Write Capacitance (C_{RW})	$V_{IN} = V_{SS}$		10	20	pF
Data Input/Output Capacitance ($C_{IN/OUT}$)	$V_{IN} = V_{SS}$		7.0	9.0	pF

f = 1 MHz, All Unused Inputs Are at AC Ground

Note 1: $V_{SS} = 5.0V$, $V_{DD} = -12V$, $T_A = 25°C$.

Note 2: Under power turn on conditions care must be taken to insure that V_{BB} is always the most positive potential in the system or large transient currents could result causing permanent damage.

Note 3: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

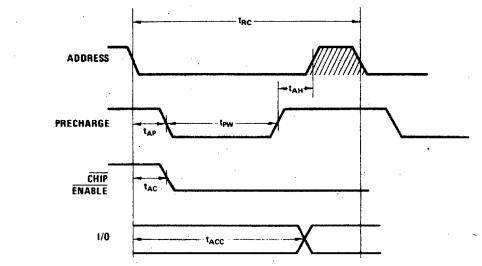
Note 4: Capacitance is guaranteed by periodic testing.

Note 5: Positive true logic notation is used:
Logic "1" = most positive voltage level
Logic "0" = most negative voltage level

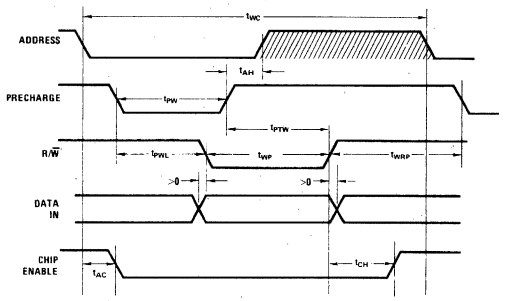
Note 6: Each of the 32 rows addressed by Address inputs A_0 through A_4 must be refreshed within the maximum interval, t_{REF}, by performing a write cycle. The row will be refreshed with $\overline{\text{Chip Enable}}$ ($\overline{CE}$) at V_{IH} or V_{IL}. Note, if $\overline{CE} = V_{IL}$ the memory cell defined by Address inputs A_0 through A_9 will be altered in accordance with information present on I/O line.

switching time waveforms

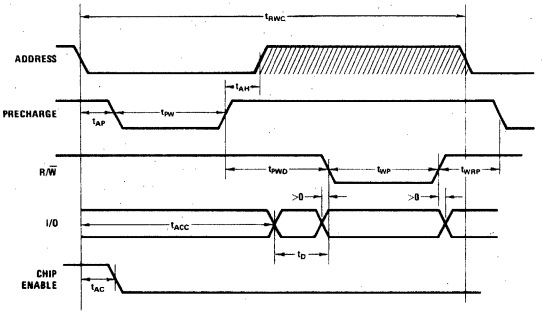
Read Cycle



Write Cycle



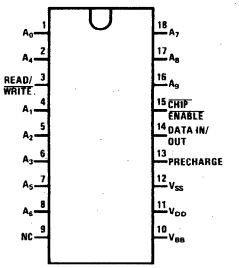
Read/Write Cycle



NOTE 1: ALL TIMING MEASUREMENTS MADE WITH 10% TO 90% t_R AND $t_F \leq 20$ ns FROM 50% POINTS.
NOTE 2: ACCESS TIME MEASURED WITH OUTPUT LOADED WITH DM8093 AND 15 pF.

connection diagram

Dual-In-Line Package



TOP VIEW

Order Number MM4261D
or MM5261D
See Package 4

Order Number MM5261N
See Package 16

NATIONAL

MOS RAMs

MM4262/MM5262 2048-bit fully decoded dynamic random access read/write memory

general description

The MM4262/MM5262 is a fully decoded 2048 word by 1 bit dynamic read/write random access memory fabricated using National Semiconductor's proprietary silicon gate low threshold technology. All inputs except the clocks are TTL compatible. The output provides a current pulse allowing a large number of devices to be bussed together without compromising system performance due to capacitive loading. The current pulse output is converted to TTL levels by means of a sense amplifier.

features

	MM4262	MM5262
■ Fast access time	470 ns (max)	365 ns (max)
■ Fast cycle time		
Short Read	565 ns (min)	475 ns (min)
Read/Write	750 ns (min)	635 ns (min)
Write	750 ns (min)	635 ns (min)
■ Refresh cycle	1.0 ms	2.0 ms

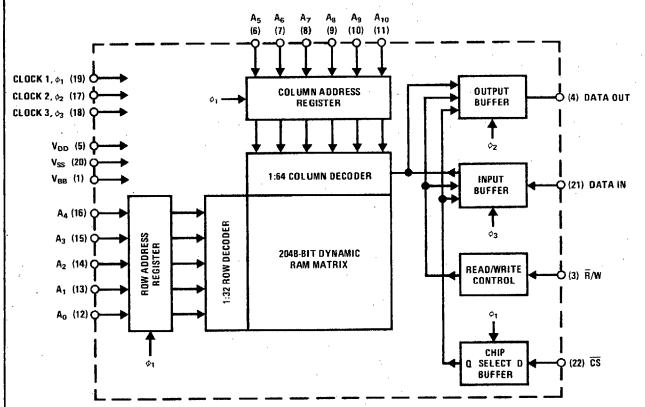
	MM4262	MM5262
■ Low power		
Operating	360 mW (max)	400 mW (max)
Standby	2.5 mW (max)	2.5 mW (max)

- Power supplies +5.0V, +8.5V, −15V
- Low overhead circuits: Fully decoded with internal memory address register
- System oriented design
  - Bipolar compatible except for clocks
  - Current sense output
  - Chip Select for easy memory expansion
- Package: 22 pin DIP (Cavity and Molded)
- Device protection: All inputs and outputs protected against static charge

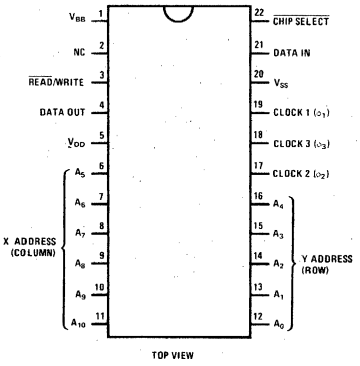
applications

- Core memory replacement
- Mainframe memory
- Buffer storage
- Non-volatile memory using battery back up

block and connection diagrams



Dual-In-Line Package



Order Number MM4262D or MM5262D
See Package 5
Order Number MM5262N
See Package 17

recommended interface circuits

CLOCK DRIVERS:	MH0026 MH8808
SENSE AMPLIFIERS:	LM167 LM168 DM7806/DM8806

absolute maximum ratings (Note 1)

Voltage at Any Pin	V_{BB} + 0.3V to V_{BB} − 27V (Note 16)
Power Dissipation	1.0W
Operating Temperature Range	
MM4262 (T_{CASE})	−55°C to +125°C
MM5262 ($T_{AMBIENT}$)	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

dc electrical characteristics MM4262 ($-55°C \leq T_{CASE} \leq +125°C$, V_{SS} = 5.0V ±0.25V, $V_{BB} - V_{SS}$ = 3.5V ±0.5V, V_{DD} = −15V ±1.0V, unless otherwise noted)

PARAMETER	CONDITIONS	MIN	TYP (Note 18)	MAX	UNITS
Inputs (Chip Select, Read/Write, Addresses, Data In)	(Notes 14, 15)				
Voltage					
Logical "1" (V_{IH})		V_{SS} 1.5		V_{SS} + 1.0	V
Logical "0" (V_{IL})		V_{SS} 10		V_{SS} 4.2	V
Current	$0 \leq V_{IN} \leq V_{SS}$			1.0	μA
Clock Inputs					
Voltage					
Logical "1" ($V_{\phi H}$)		V_{SS} 1.0		V_{SS} + 1.0	V
Logical "0" ($V_{\phi L}$)		V_{DD} 1.0		V_{DD} + 1.0	V
Current	V_{IN} = −16V			50	μA
Outputs	(Note 15)				
Current					
Logical "0" (I_{OL})	V_{OUT} = 0V			100	μA
Logical "1" (I_{OH})	V_{OUT} = 1.2V, $\overline{CS}$ = 0.4V			6.0	mA
	V_{OUT} = 1.8V, $\overline{CS}$ = 0.4V	500			μA
Leakage Current	V_{OUT} = 0V, $\overline{CS}$ = 3.5V			10	μA
Power Supply Current	(Note 17) T_A = 25°C, $V_{BB} - V_{SS}$ = 3.5V, V_{SS} = 5.0V, V_{DD} = −15V, V_{OUT} = 1.2V, Reading 1's at T_{CYCLE} = 750 ns				
(I_{DD})			12	18	mA
(I_{BB})	Operating			150	μA
	Standby (No Clocks)			100	μA

ac electrical characteristics MM4262 (All times measured from 50% points, t_r, $t_f \leq 20$ ns, see ac test circuit and timing diagram, conditions under dc electrical characteristics apply.)

PARAMETER	CONDITIONS	MIN	TYP (Note 18)	MAX	UNITS
ϕ_1 Clock Pulse Width (T_{1PW})	(Note 4)	115	70		ns
ϕ_2 Clock Pulse Width (T_{2PW})	(Note 6)	275	160	400	ns
ϕ_3 Clock Pulse Width (T_{3PW})	(Note 8)	110	60		ns
ϕ_1 Clock to ϕ_2 Clock Delay (T_{12})	(Note 5)	110	60		ns
ϕ_2 Clock to ϕ_3 Clock Delay (T_{23})	(Note 7)	65	10		ns
ϕ_3 Clock to ϕ_1 Clock Delay (T_{31})	(Note 9)	75	40		ns
Chip Select and Address Set Up Time (T_{AS})		100	60		ns
Chip Select and Address Hold Time (T_{AH})		110	50		ns
Read/Write Read Set Up Time (T_{RWS3})		85	30		ns
Read/Write Read Hold Time (T_{RWH3})		65	30		ns
Read/Write Write Set Up Time (T_{RWS1})		95	30		ns
Read/Write Write Hold Time (T_{RWD3})		25	0		ns
Logical "1" Data In Set Up Time (T_{DS1})	(Note 10)	180	60		ns
Logical "0" Data In Set Up Time (T_{DS2})	(Note 10)	75	30		ns
Data In Hold Time (T_{DH1})		70	20		ns
Read Access Time (T_{ACC2})			150	260	ns
Read Access Time (T_{ACC1})	$T_{ACC1} = T_{AS} + T_{12} + T_{ACC2}$		300	470	ns

ac electrical characteristics (con't) MM4262

PARAMETER	CONDITIONS	MIN	TYP (Note 18)	MAX	UNITS
Read Only Cycle ($T_{SHORT/READ}$)	(Note 11)	565			ns
Read, Write, Read Modify Write Cycle (T_{CYCLE})		750			ns
Refresh Time	(Note 12)			1.0	ms
Output Hold Time (T_{OH})	(Note 13)	1000			ns
$\overline{\text{Chip Select}}$, Address, $\overline{\text{Read}}$/Write, Data In, Data Out Capacitance (C_X)	(Note 2) $V_{BB} - V_{SS} = 3.5V$, $V_{SS} = 5.0V$ $V_{TEST} = 5.0\ V_{DC}$ With ≤ 15 mV RMS at f = 1 MHz			7.0	pF
ϕ_1 Clock Capacitance (C_1)				50	pF
ϕ_2 Clock Capacitance (C_2)				25	pF
ϕ_3 Clock Capacitance (C_3)				25	pF
Clock Rise/Fall Time				100	ns
Input Rise/Fall Time				50	ns

dc electrical characteristics MM5262 $0°C \leq T_A \leq +70°C$, $V_{SS} = 5.0V \pm 0.25V$, $V_{BB} - V_{SS} = 3.5V \pm 0.5V$, $V_{DD} = -15V \pm 1.0V$, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP (Note 18)	MAX	UNITS
Inputs ($\overline{\text{Chip Select}}$, $\overline{\text{Read}}$/Write, Addresses, Data In)	(Notes 14 and 15)				
Voltage					
Logical "1" (V_{IH})		$V_{SS} - 1.5$		$V_{SS} + 1.0$	V
Logical "0" (V_{IL})		$V_{SS} - 10$		$V_{SS} - 4.2$	V
Current	$0V \leq V_{IN} \leq V_{SS}$			1.0	μA
Clock Inputs					
Voltage					
Logical "1" ($V_{\phi H}$)		$V_{SS} - 1.0$		$V_{SS} + 1.0$	V
Logical "0" ($V_{\phi L}$)		$V_{DD} - 1.0$		$V_{DD} + 1.0$	V
Current	$V_{IN} = -16V$			50	μA
Output	(Note 15)				
Current					
Logical "0" (I_{OL})	$V_{OUT} = 0V$			100	μA
Logical "1" (I_{OH})	$V_{OUT} = 1.2V$, $\overline{CS} = 0.4V$			6.0	mA
	$V_{OUT} = 1.8V$, $\overline{CS} = 0.4V$	600			μA
Leakage Current	$V_{OUT} = 0V$, $\overline{CS} = 3.5V$			10	μA
Power Supply Current	(Note 17) $T_A = 25°C$, $V_{BB} - V_{SS} = 3.5V$, $V_{SS} = 5.0V$, $V_{DD} = -15V$, $V_{OUT} = 1.2V$, Reading 1's at $T_{CYCLE} = 635$ ns				
(I_{DD})	Operating		13	20	mA
(I_{BB})	Standby (No Clocks)			150	μA
				100	μA

ac electrical characteristics MM5262 (All times measured from 50% points, t_r, $t_f \leq 20$ ns, see ac test circuit and timing diagram, conditions under dc electrical characteristics apply.)

PARAMETER	CONDITIONS	MIN	TYP (Note 13)	MAX	UNITS
ϕ_1 Clock Pulse Width (T_{1PW})	(Note 4)	95	70		ns
ϕ_2 Clock Pulse Width (T_{2PW})	(Note 6)	240	160	400	ns
ϕ_3 Clock Pulse Width (T_{3PW})	(Note 8)	100	60		ns
ϕ_1 Clock to ϕ_2 Clock Delay (T_{12})	(Note 5)	90	60		ns
ϕ_2 Clock to ϕ_3 Clock Delay (T_{23})	(Note 7)	50	10		ns
ϕ_3 Clock to ϕ_1 Clock Delay (T_{31})	(Note 9)	60	40		ns
$\overline{\text{Chip Select}}$ and Address Set Up Time (T_{AS})		80	60		ns
$\overline{\text{Chip Select}}$ and Address Hold Time (T_{AH})		90	50		ns
$\overline{\text{Read}}$/Write Read Set Up Time (T_{RWS3})		70	30		ns
$\overline{\text{Read}}$/Write Read Hold Time (T_{RWH3})		65	30		ns
$\overline{\text{Read}}$/Write Write Set Up Time (T_{RWS1})		75	30		ns

ac electrical characteristics (con't) MM5262

PARAMETER	CONDITIONS	MIN	TYP (Note 18)	MAX	UNITS
$\overline{\text{Read}}$/Write Write Hold Time (T_{RWD3})		25	0		ns
Logical "1" Data In Set Up Time (T_{DS1})	(Note 10)	120	60		ns
Logical "0" Data In Set Up Time (T_{DS2})	(Note 10)	60	30		ns
Data In Hold Time (T_{DH1})		50	20		ns
Read Access Time (T_{ACC2})			150	195	ns
Read Access Time (T_{ACC1})	$T_{ACC1} = T_{AS} + T_{12} + T_{ACC2}$		300	365	ns
Read Only Cycle ($T_{SHORT/READ}$)	(Note 11)	475			ns
Read, Write, Read Modify Write Cycle (T_{CYCLE})		635			ns
Refresh Time	(Note 12)			2.0	ms
Output Hold Time (T_{OH})	(Note 13)	1000			ns
$\overline{\text{Chip Select}}$, Address, $\overline{\text{Read}}$/Write, Data In, Data Out Capacitance (C_X)	(Note 2) $V_{BB} - V_{SS} = 3.5V$, $V_{SS} = 5.0V$ $V_{TEST} = 5.0\ V_{DC}$ With ≤ 15 mV RMS at f = 1.0 MHz			7.0	pF
ϕ_1 Clock Capacitance (C_1)				50	pF
ϕ_2 Clock Capacitance (C_2)				25	pF
ϕ_3 Clock Capacitance (C_3)				25	pF
Clock Rise/Fall Time				100	ns
Input Rise/Fall Time				50	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: Positive true logic notation is used: Logic "1" = most positive voltage level
Logic "0" = most negative voltage level

Note 4: T_{1PW}, ϕ_1 clock — used to change input logic address and chip select.

Note 5: T_{12}, interval between clock 1 and 2 — for decode.

Note 6: T_{2PW}, ϕ_2 clock — cell access.

Note 7: T_{23}, interval between clock 2 and 3 — decision time.

Note 8: T_{3PW}, ϕ_3 clock — write or refresh clock.

Note 9: T_{31}, write recovery time.

Note 10: If a "1" is being written then data in must go high T_{DS1} before the end of ϕ_2 and remain in that state until T_{DH1} after ϕ_3 goes low. If a "0" is being written, data in must go low at least T_{DS2} before ϕ_3, and remain in that state until T_{DH1} after ϕ_3 goes low.

Note 11: For a short read cycle, ϕ_3 may be inhibited and the next cycle may begin T_{23} after ϕ_2.

Note 12: Addresses A_0 through A_4 are the row addresses. To accomplish a refresh, at least one location in each row must be accessed during any 2 ms period for the MM5262 and 1 ms for the MM4262. The row will refresh when reading or writing with the chip disabled or enabled as long as ϕ_3 is applied.

Note 13: During a read cycle the output will remain valid until the next ϕ_1 or T_{OH} whichever is less. During a read modify write or write cycle the output will remain valid until ϕ_3 time.

Note 14: The chip is enabled when $\overline{\text{chip select}}$ is at a logic "0."

Note 15: If a logic "1" (3.5V) is written, when it is read the output will source more than 600μA.

Note 16: Under power turn on conditions care must be taken to insure that V_{BB} is always the most positive potential in the system or large transient currents could result, causing permanent damage.

Note 17: An approximate relationship for I_{DD} is:

$$I_{DD\,max} = A\frac{T_{1PW}}{T_{CYC}} + B\frac{T_{2PW}}{T_{CYC}} + C\frac{1000\text{ ns}}{T_{CYC}}$$

where: A = 20 @ 25°C A = 23 @ 0°C A = 32 @ −55°C
B = 4.5 @ 25°C B = 5.2 @ 0°C B = 7.2 @ −55°C
C = 10 @ 25°C C = 10 @ 0°C C = 12 @ −55°C

Note 18: Typical values for $T_A = 25°C$, $V_{SS} = 5.0V$, $V_{BB} = 8.5V$, and $V_{DD} = -15V$.

timing and operation

The MM4262/MM5262 has four basic modes of operation: (1) read, (2) write, (3) read modify write and (4) refresh. Each, of these modes, is commonly used in memory systems. To make the timing and control considerations perfectly clear each mode will be discussed separately.

READ OPERATION

The read operation consists of reading previously stored data out of randomly selected address locations. The read operation may be performed in one of two ways.

The first method is by use of the $\overline{\text{Read}}/\overline{\text{Write}}$ control. As indicated in Figure 1, if the $\overline{\text{Read}}/\overline{\text{Write}}$ input goes low, for at least the time specified by $T_{RWS3} + T_{RWH3}$, the information will be read out of the selected memory location. The output will remain valid for $T_{OH(max)}$ or until the next ϕ_1 clock pulse, whichever is less.

The second method involves gating the ϕ_3 clock pulse. A write operation can only occur when the ϕ_3 clock is present. Thus by applying a logical "1" to the $\overline{\text{Read}}/\overline{\text{Write}}$ control (write mode) and not applying the ϕ_3 clock, the memory will read out information from the selected location. In other words the memory will be operating in the read mode. There are advantages in gating the ϕ_3 clock. First, since ϕ_3 clock is a high level signal, power will be reduced. Second, since in the read mode ϕ_3 has been eliminated, ϕ_1 may be applied after the T_{23} delay. This will shorten the read cycle by the $T_{3PW} + T_{31}$ interval. The short read cycle is then:

$$T_{SHORT\ READ} = T_{CYCLE} - (T_{3PW} + T_{31})$$
$$= (635 - 160)\ ns = 475\ ns \text{ for MM5262}$$
$$= (750 - 185)\ ns = 565\ ns \text{ for MM4262}$$

WRITE OPERATION

The write operation consists of storing new information into randomly selected address locations. Just as in the case of the read mode, write may be performed by using the $\overline{\text{Read}}/\overline{\text{Write}}$ control or by gating the ϕ_3 clock. The ϕ_3 clock is essential to the write operation and unless it is present, a write will not occur regardless of the state of the $\overline{\text{Read}}/\overline{\text{Write}}$ control.

READ MODIFY WRITE OPERATION

The read modify write operation consists of reading information out of a randomly selected memory location and then writing new information into this same location. The important point to remember in understanding this mode is that information is always read out of the selected address location regardless of the state of the $\overline{\text{Read}}/\overline{\text{Write}}$ control. In this sense, the $\overline{\text{Read}}/\overline{\text{Write}}$ control may be thought of as a write inhibit control.

Then, in the write mode, information will be output T_{ACC2} after the leading edge of the ϕ_2 clock and held until the start of the ϕ_3 clock. The write operation procedes in a normal manner and new information, present on the Data In line, will be written into the selected memory location.

If the Data In and Data Out lines are interfaced to a common data I/O bus, the T_{23} interval must be increased a sufficient amount to transfer the read data onto the common I/O bus and to change the I/O bus to the new information to be written. This, of course, will increase T_{CYC} by the same amount that T_{23} is increased.

REFRESH OPERATION

Because the storage mechanism of a dynamic RAM is charge retention on a capacitor, and leakage paths exist, these capacitors must be recharged or "refreshed" periodically. For the MM5262 the maximum time between refresh intervals must be less than or equal to 2.0 ms. For the MM4262 the maximum refresh interval is 1.0 ms.

The MM4262/MM5262 refreshes on a row basis. That is, when any location within a row is refreshed all locations in that row are refreshed. There are 32 rows in the RAM matrix, corresponding to addresses A_0 through A_4.

Refresh is accomplished within a row whenever the ϕ_3 clock is applied. It does not matter if the memory is in read mode, write mode, selected or not selected. The most common method of refreshing the memory is to place $\overline{CS}$ at V_{IH} and sequence the clocks through a normal read or write cycle with the ϕ_3 clock applied. Note that if, during normal system operation, each row is written into or read out of at an interval of 2.0 ms (1.0 ms for the MM4262) or less, refresh is not required as a separate operation.

Now that the four modes of operation have been defined a step by step description of a write cycle will serve to further clarify the operation of the MM4262/MM5262 RAM.

Any cycle is initiated by the leading edge of the ϕ_1 clock. For a device to be selected it must receive a ϕ_1 clock and $\overline{CS}$ must be at V_{IL} for the interval specified by T_{AS} and T_{AH}. Note that the ϕ_1 clock must be applied to deselect a device also (see block diagram). When a device is not selected, the output buffer assumes a high impedance state and the input buffer inhibits input data.

In addition to gating $\overline{CS}$ information into the device, the ϕ_1 clock also gates in address information (see block diagram). Address inputs, A_0 through A_{10}, must be stable for the interval specified by T_{AS} and T_{AH}.

timing and operation (con't)

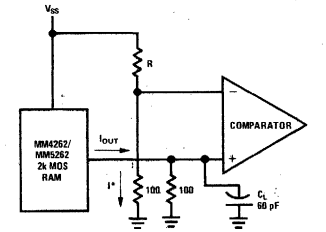
Assuming the read/write operation is to be controlled by the $\overline{\text{Read}}$/Write input, this input must be at V_{IH} for an interval of T_{RWS1} prior to the trailing edge of ϕ_1 clock, and remain at V_{IH} until T_{RWD3} after the trailing edge of the ϕ_3 clock. Note that if the $\overline{\text{Read}}$/Write input is low, during the T_{RWS3} plus T_{RWH3} interval the write operation is internally inhibited, allowing only a refresh to occur.

The ϕ_2 clock gates the information corresponding to the selected address through the output buffer (see block diagram) to the Data Out pin. The delay from leading edge of the ϕ_2 clock to valid data out is T_{ACC2}, Read Access Time. Note that even though the memory is in the write mode, data is being read out. Data out will remain valid only until the start of the ϕ_3 clock, because $\overline{\text{Read}}$/Write is at V_{IH}.

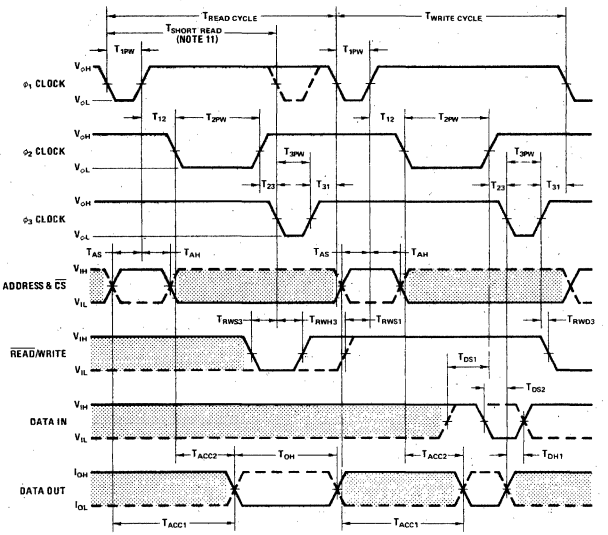
The actual write operation, as stated previously, is controlled by the ϕ_3 clock. The amount of time Data In must be stable is dependent on whether a logical "1" or a logical "0" is to be written. If a logical "1" is to be written, Data In must be stable T_{DS1} prior to the trailing edge of the ϕ_2 clock and remain stable until T_{DH1} after the leading edge of the ϕ_3 clock. If a logical "0" is to be written, Data In must be stable T_{DS2} prior to the leading edge of the ϕ_3 clock and remain stable until T_{DH1} after the leading edge of the ϕ_3 clock.

T_{31} after the trailing edge of the ϕ_3 clock another ϕ_1 clock may be applied to initiate the next cycle. Note that if the next address location is in another device the ϕ_1 clock must still be applied to deselect the current device. This becomes important when clock decoding is used to reduce power consumption in a memory system (see Application Note AN-86).

ac test circuit and switching time waveforms



*I = 500μA for MM4262
I = 600μA for MM5262



NOTE: Shaded areas are "don't care" conditions. All times measured with t_r, $t_f \leq 20$ ns.

FIGURE 1.

NATIONAL

MOS RAMs

MM5269 1024-bit (256 × 4) fully decoded static RAM with on chip registers

general description

The National MM5269 is a 256 word x 4 bit Static Random Access Memory device fabricated using N-Channel enhancement mode Silicon Gate technology. Static storage cells eliminate the need for refresh and the additional peripheral circuitry associated with refresh. Data in and data out have the same polarity.

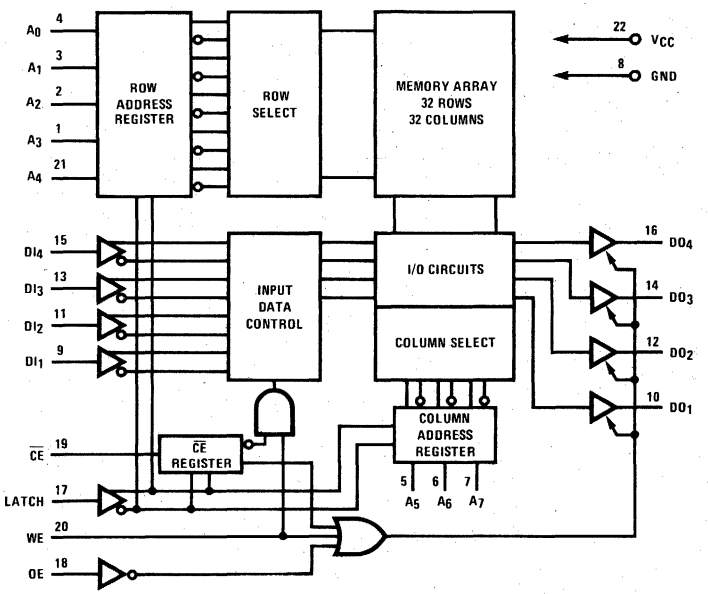
The MM5269 is fully TTL compatible including inputs, outputs and power supply. The chip enable input allows memory expansion and the address latch feature eliminates the need for external address registers. The output enable is provided for systems which use a common input/output data bus. All of the features of this memory device can be combined to make a low cost, high performance and easy to manufacture memory system. System design costs are also minimized because of the ease-of-use of the MM5269.

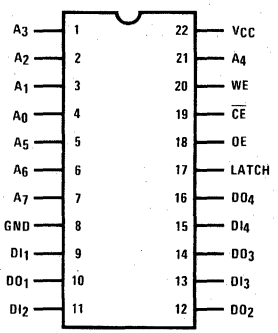
National's Silicon Gate process provides protection against contamination and permits the use of low cost Epoxy B packaging.

features

- Organization 256 Words by 4 Bits
- Access Time – 0.5 to 1.0 μs
- On Chip Address and Chip Enable Registers
- Directly TTL Compatible – All Inputs and Outputs
- Single +5 V Power Supply
- Tri-State ® Output – OR-Tie Capability
- Output Enable for Common Data Bus Systems
- Static Memory – No Refresh Required
- Packaged in a 22 Pin Epoxy B Dual-In-Line

block and connection diagrams





Order Number MM5269D
See Package 5
Order Number MM5269N
See Package 17

absolute maximum ratings

Voltage at Any Pin	-0.5 V to +7.0 V
Operating Temperature	0°C to +70°C
Storage Temperature	-65°C to +150°C
Power Dissipation	1 Watt
Lead Temperature (10 s)	300°C

dc electrical characteristics (V_{CC} = 5.0 V ± 5%, 0°C ≤ T_A ≤ +70°C)

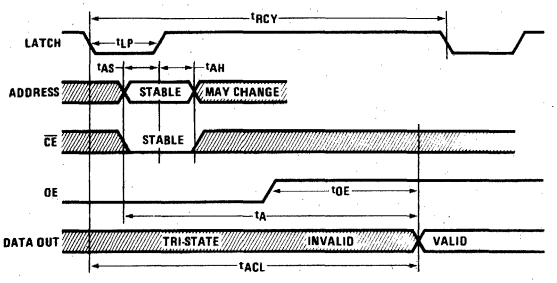
Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
V_{IH}	Logic "1" Input Voltage	2.2		V_{CC}	V	
V_{IL}	Logic "0" Input Voltage	-0.5		0.65	V	
V_{OH}	Logic "1" Output Voltage	2.2			V	I_{OH} = -150 μA
V_{OL}	Logic "0" Output Voltage			0.45	V	I_{OL} = 2.0 mA
I_{LI}	Input Load Current			10	μA	0 V ≤ V_{IN} ≤ 5.0 V
I_{LOH}	Output Leakage Current			15	μA	$\overline{CE}$ = 2.2 V, V_O = 4.0 V
I_{LOL}	Output Leakage Current			-50	μA	$\overline{CE}$ = 2.2 V, V_O = 0.45 V
I_{CC}	Power Supply Current			70	mA	V_{IN} = 5.25 V, I_O = 0 mA, T_A = 0°C

ac electrical characteristics (V_{CC} = 5.0 V ± 5%, 0°C ≤ T_A ≤ +70°C)

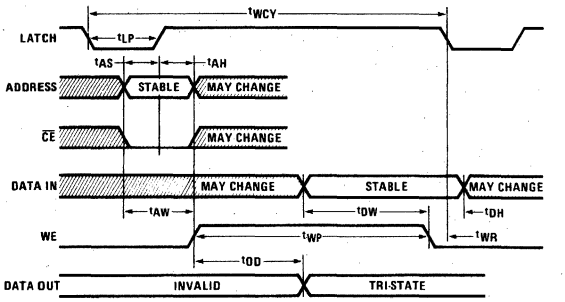
Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
READ CYCLE						
t_{RCY}	Read Cycle	1,000			ns	
t_A or t_{ACL}	Access Time			1,000	ns	Input Pulse Levels: +0.65 to +2.2 V Input Pulse Rise and Fall Times: 20 ns Timing Measurement Reference Level: 1.5 V Output Load: 1 TTL Gate and C_L = 100 pF
t_{OE}	Output Enable to Output Time			500	ns	
t_{LP}	Latch Pulse Width	200			ns	
t_{AS}	ADD & $\overline{CE}$ to Latch Setup Time	100			ns	
t_{AH}	ADD & $\overline{CE}$ to Latch Hold Time	100			ns	
WRITE CYCLE						
t_{WCY}	Write Cycle	1,000			ns	
t_{AW}	Address and CE to Write Setup Time	200			ns	
t_{WP}	Write Pulse Width	650			ns	Input Pulse Levels: +0.65 to +2.2 V Input Pulse Rise and Fall Times: 20 ns Timing Measurement Reference Level: 1.5 V Output Load: 1 TTL Gate and C_L = 100 pF
t_{WR}	Write Recovery Time	50			ns	
t_{OD}	Write to Output Disable Time			400	ns	
t_{DW}	Data Setup Time	350			ns	
t_{DH}	Data Hold Time	100			ns	
t_{CW}	Chip Enable to Write	750			ns	
t_{LP}	Latch Pulse Width	200			ns	
t_{AS}	Add & CE to Latch Setup Time	100			ns	
t_{AH}	Add & CE to Latch Hold Time	100			ns	

switching time waveforms

READ CYCLE (WE = "0")



WRITE CYCLE



NATIONAL

MM5270 TRI-SHARE™ 4096-bit fully decoded dynamic random access read/write memory

general description

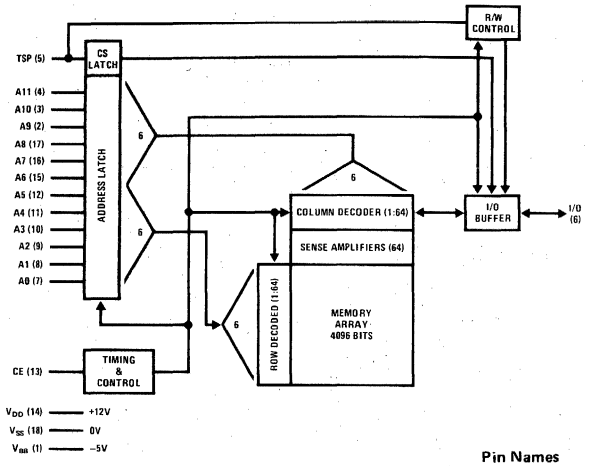
The MM5270 is a 4096-bit dynamic random access memory with TRI-SHARE. Because of this unique design feature, National is able to package a 4k device in an 18-pin dual-in-line package. The device is manufactured using N-channel silicon gate technology with a single transistor cell which provides higher density on a monolithic chip and thus lower cost.

The TRI-SHARE Port (TSP) is a multifunction input that, along with a common input/output, allows National to manufacture an 18-pin version of a 4k RAM. The functions controlled by the TSP are read/write, V_{CC}, and logical chip select. In order to understand how the TSP works, consider the timing diagrams. The state of the TSP at the leading edge of the chip enable clock determines whether the device is selected. If it is at a TTL high level, the chip is selected and the device goes into a read mode after chip enable goes high. This high level also performs a V_{CC} function in that it enables a reference voltage for a TTL high output. The supply for the output buffer is V_{DD}, not the TRI-SHARE Port; thus, no special driver is required. In order to perform a write, the TSP must be pulsed low after the minimum hold time and the appropriate data placed on the I/O. When the MM5270 goes into write, the output circuit is disabled. If the TSP is low at the start of the cycle, the memory is not selected but it will be refreshed if the chip enable clock is pulsed.

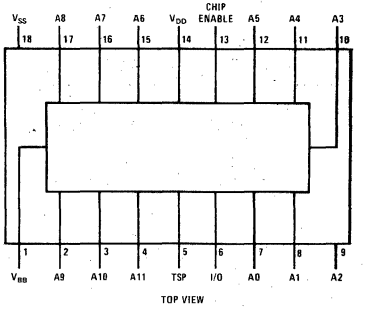
features

- 4096 x 1 bit organization
- Access time 200 ns maximum
- Cycle time 400 ns minimum
- TRI-SHARE port
- High memory density—18-pin package
- TTL compatible inputs (except chip enable)
- TRI-STATE® common input/output
- Registers on chip for addresses and chip select
- Two power supplies, +12V, −5V
- Simple read-modify-write operation

block and connection diagrams



Dual-In-Line Package



Order Number MM5270D
See Package 4

Pin Names

A0–A11	Address Inputs*	V_{BB}	Power (−5V)
CE	Chip Enable	V_{DD}	Power (+12V)
TSP	TRI-SHARE Port	V_{SS}	Ground
I/O	D_{IN}/D_{OUT}		

*Refresh Addess A0–A5

absolute maximum ratings (Note 1)

Operating Temperature Range	0°C to +70°C
Storage Temperature	−65°C to +150°C
All Input or Output Voltages with Respect to the Most Negative Supply Voltage, V_{BB}	−0.3V to +25V
Supply Voltages V_{DD} and V_{SS} with Respect to V_{BB}	−0.3V to +20V
Power Dissipation	1.0W

dc electrical characteristics

T_A = 0°C to +70°C, V_{DD} = +12V ±5%, V_{BB} (Note 2) = −5V ±5%, V_{SS} = 0V, unless otherwise noted

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP (3)	MAX	UNITS
I_{LI}	Input Load Current	V_{IN} = 0V to V_{IH} max, (All Inputs Except CE)		0.01	10	μA
I_{LC}	Input Load Current	V_{IN} = 0V to V_{IHC} max		0.01	10	μA
I_{LO}	Output Leakage Current Up For High Impedance State	CE = V_{ILC}, V_O = 0V to 5.25V		0.01	10	μA
I_{DD1}	V_{DD} Supply Current During CE "OFF"	CE = −1V to +0.6V, (Note 4)		110		μA
I_{DD2}	V_{DD} Supply Current During CE "ON"	CE = V_{IHC}, T_A = 25°C		20		mA
$I_{DD\ AV1}$	Average V_{DD} Current	T_A = 25°C, Cycle Time = 400 ns, t_{CE} = 230 ns		35		mA
$I_{DD\ AV2}$	Average V_{DD} Current	T_A = 25°C, Cycle Time = 1000 ns, t_{CE} = 230 ns		15		mA
I_{BB}	V_{BB} Supply Current Average			5	100	μA
V_{IL}	Input Low Voltage	t_T = 20 ns, (*Figure 4*)	−1.0		0.6	V
V_{IH}	Input High Voltage		2.4		V_{CC}+1	V
V_{ILC}	CE Input Low Voltage		−1.0		1.0	V
V_{IHC}	CE Input High Voltage		V_{DD}−1		V_{DD}+1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.0 mA	0.0		0.45	V
V_{OH}	Output High Voltage	I_{OH} = −2.0 mA	2.4			V

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: The only requirement for the sequence of applying voltage to the device is that V_{DD} or V_{SS} should never be 0.3V more negative than V_{BB}.

Note 3: Typical values are for T_A = 25°C and nominal power supply voltages.

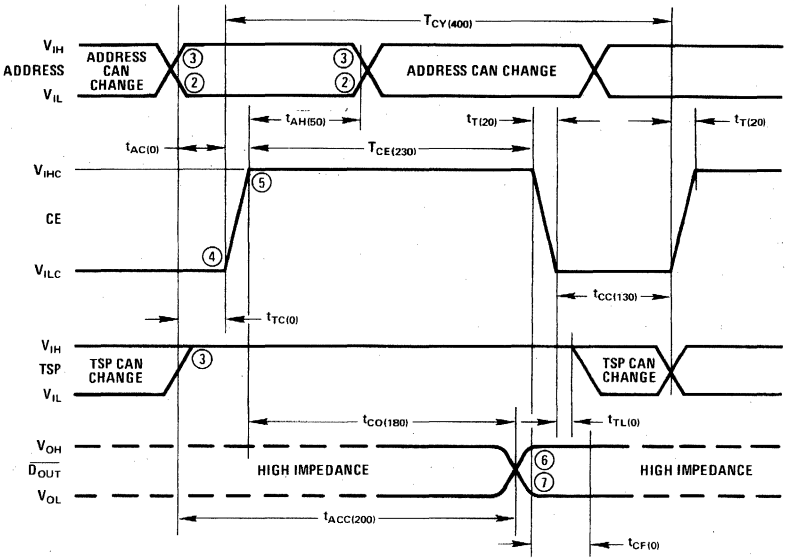
Note 4: The I_{DD} current is to V_{SS}. The I_{BB} current is the sum of all leakage currents.

ac electrical characteristics T_A = 0°C to +70°C, V_{DD} = 12V ±5%, V_{BB} = −5V ±5%

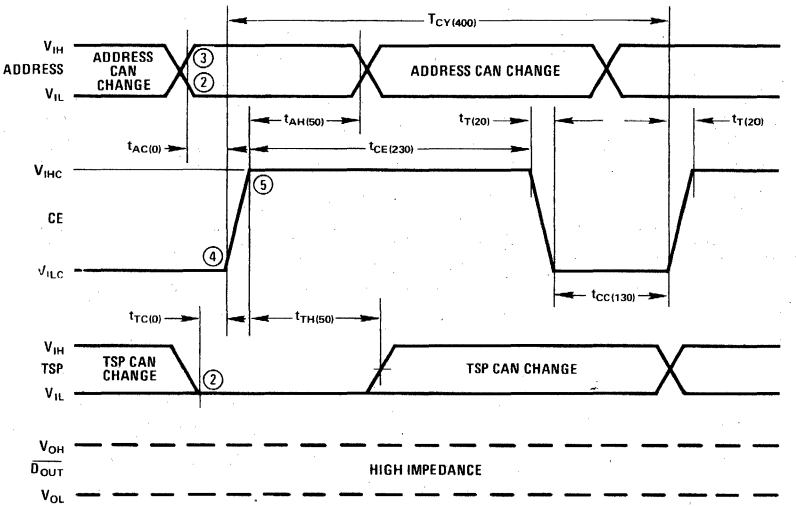
SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
READ, WRITE, READ/MODIFY/WRITE, AND REFRESH CYCLE						
t_{REF}	Time Between Refresh				2	ms
t_{AC}	Address to CE Set-Up Time	t_{AC} is Measured From End of Address Transition	0			ns
t_{AH}	Address Hold Time		50			ns
t_{CC}	CE "OFF" Time		130			ns
t_T	CE Transition Time		10		40	ns
t_{CF}	CE "OFF" to Output High Impedance State		0			ns
t_{TC}	TRI-SHARE Port to CE Set-Up Time		0			ns
t_{TH}	TRI-SHARE Port Hold Time		50			ns
READ CYCLE						
t_{CY}	Cycle Time	t_T = 20 ns C_{LOAD} = 50 pF, Load = One TTL Gate Ref 1 = 2.0V, Ref 0 = 0.8V $t_{ACC} = t_{AC} + t_{CO} + t_T$	400			ns
t_{CE}	CE "ON" Time		230		3000	ns
t_{CO}	CE Output Delay				180	ns
t_{ACC}	Address to Output Access				200	ns
t_{TL}	CE to TSP		0			ns

switching time waveforms

Read Cycle



Refresh Cycle ①



Note 1: For Refresh cycle, row and column addresses must be stable before t_{AC} and remain stable for entire t_{AH} period.

Note 2: $V_{IL\ MAX}$ is the reference level for measuring timing of the addresses, T_{SP} and D_{IN}.

Note 3: $V_{IH\ MIN}$ is the reference level for measuring timing of the addresses, T_{SP} and D_{IN}.

Note 4: V_{SS} + 2.0V is the reference level for measuring timing of CE.

Note 5: V_{DD} − 2V is the reference level for measuring timing of CE.

Note 6: V_{SS} + 2.0V is the reference level for measuring the timing of D_{OUT} for a high output.

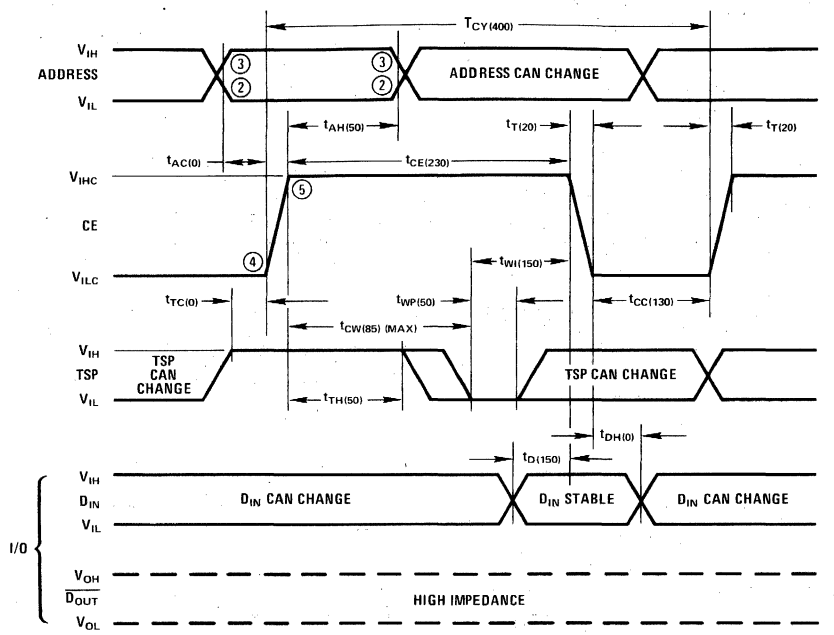
Note 7: V_{SS} + 0.8V is the reference level for measuring timing of D_{OUT} for a low output.

ac electrical characteristics (con't) $T_A = 0°C$ to $+70°C$, $V_{DD} = 12V \pm 5\%$, $V_{BB} = -5V \pm 5\%$

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
WRITE CYCLE						
t_{CY}	Cycle Time		400			ns
t_{CE}	CE "ON" Time		230		3000	ns
t_{WI}	TSP to CE "OFF"		150			ns
t_{CW}	CE to TSP	$t_T = 20$ ns			85	ns
t_D	D_{IN} to CE "OFF"		150			ns
t_{DH}	D_{IN} Hold Time		0			ns
t_{WP}	TSP Pulse Width		50			ns

switching time waveforms (con't)

Write Cycle



Note 1: For Refresh cycle, row and column addresses must be stable before t_{AC} and remain stable for entire t_{AH} period.

Note 2: $V_{IL\ MAX}$ is the reference level for measuring timing of the addresses, T_{SP} and D_{IN}.

Note 3: $V_{IH\ MIN}$ is the reference level for measuring timing of the addresses, T_{SP} and D_{IN}.

Note 4: $V_{SS} + 2.0V$ is the reference level for measuring timing of CE.

Note 5: $V_{DD} - 2V$ is the reference level for measuring timing of CE.

Note 6: $V_{SS} + 2.0V$ is the reference level for measuring the timing of D_{OUT} for a high output.

Note 7: $V_{SS} + 0.8V$ is the reference level for measuring timing of D_{OUT} for a low output.

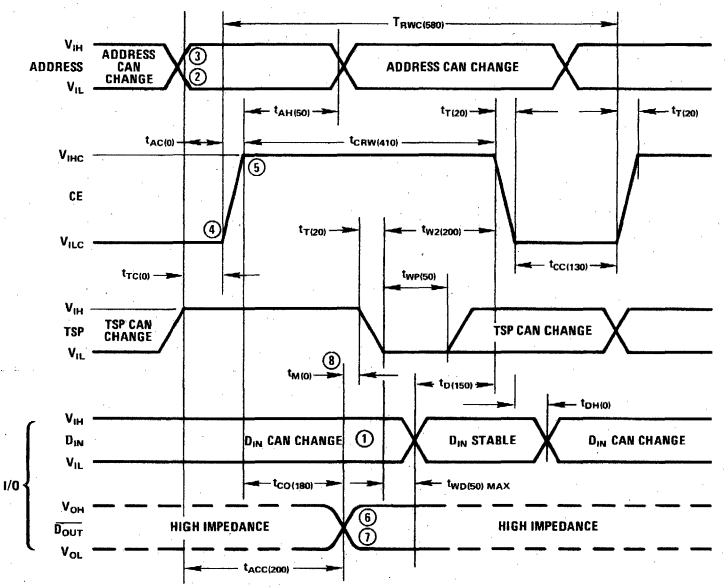
ac electrical characteristics (con't) $T_A = 0°C$ to $+70°C$, $V_{DD} = 12V \pm 5\%$, $V_{BB} = -5V \pm 5\%$

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
READ/MODIFY/WRITE CYCLE						
t_{RWC}	Read Modify Write (RMW) Cycle Time		580			ns
t_{CRW}	CE Width During RMW		410		3000	ns
t_{WC}	TSP to CE "ON"	t_T = 20 ns	0			ns
t_{W2}	TSP to CE "OFF"	C_{LOAD} = 50 pF, Load = One TTL Gate	200			ns
t_{WP}	TSP Pulse Width	Ref 1 - 2.0V, Ref 0 = 0.8V	50			ns
t_D	D_{IN} to CE "OFF"	$t_{ACC} = t_{AC} + t_{CO} + t_T$	150			ns
t_{DH}	D_{IN} Hold Time		0			ns
t_{CO}	CE to Output Delay				180	ns
t_{ACC}	Access Time				200	ns
t_{WD}	TSP to Output High Impedance				50	ns
t_M	Modify Time		0			ns
CAPACITANCE (Note 1)						
C_{AD}	Address Capacitance, $\overline{CS}$	$V_{IN} = V_{SS}$		2		pF
C_{CE}	CE Capacitance	$V_{IN} = V_{SS}$		15		pF
$C_{I/O}$	Data I/O Capacitance	$V_{OUT} = 0V$		8		pF
C_{IN}	TSP Capacitance	$V_{IN} = V_{SS}$		5		pF

Note 1: Capacitance measured with Boonton Meter or effective capacitance calculated from the equation $C = I\Delta t/\Delta V$ with the current equal to a constant 20 mA.

switching time waveforms (con't)

Read Modify Write Cycle



Note 1: If D_{IN} is forced prior to $\overline{D_{OUT}}$ becoming high impedance ($t_{WD(MAX)}$), then maximum ambient temperature should be derated by T_{0V}/T_{CYCLE} (35°C). Where T_{0V} is time between forcing D_{IN} and $\overline{D_{OUT}}$ becoming TRI-STATE.

Note 2: $V_{IL\ MAX}$ is the reference level for measuring timing of the addresses, T_{SP} and D_{IN}.

Note 3: $V_{IH\ MIN}$ is the reference level for measuring timing of the addresses, T_{SP} and D_{IN}.

Note 4: $V_{SS} + 2.0V$ is the reference level for measuring timing of CE.

Note 5: $V_{DD} - 2V$ is the reference level for measuring timing of CE.

Note 6: $V_{SS} + 2.0V$ is the reference level for measuring the timing of D_{OUT} for a high output.

Note 7: $V_{SS} + 0.8V$ is the reference level for measuring timing of D_{OUT} for a low output.

Note 8: For minimum cycle, $t_M = 0$, for test purposes $t_M = 10$ ns.

NATIONAL

MOS RAMs

MM5270-5 TRI-SHARE™ 4096-bit random access read/write memory

general description

The MM5270-5 is a slower speed version of National's MM5270 dynamic RAM. Please refer to the MM5270 specification for pin configuration, block diagram and switching time waveforms.

features

- Access time—270 ns
- Cycle time—470 ns

absolute maximum ratings (Note 1)

Operating Temperature Range	0°C to +70°C
Storage Temperature	−65°C to +150°C
All Input or Output Voltages with Respect to the Most Negative Supply Voltage, V_{BB}	−0.3V to +25V
Supply Voltages V_{DD} and V_{SS} with Respect to V_{BB}	−0.3V to +20V
Power Dissipation	1.0W

Order Number MM5270D-5
See Package 4

dc electrical characteristics

T_A = 0°C to +70°C, V_{DD} = +12V ±5%, V_{BB} (Note 2) = −5V ±5%, V_{SS} = 0V, unless otherwise noted

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP (3)	MAX	UNITS
I_{LI}	Input Load Current	V_{IN} = 0V to V_{IH} max, (All Inputs Except CE)		0.01	10	μA
I_{LC}	Input Load Current	V_{IN} = 0V to V_{IHC} max		0.01	10	μA
$\|I_{LO}\|$	Output Leakage Current Up For High Impedance State	CE = V_{ILC}, V_O = 0V to 5.25V		0.01	10	μA
I_{DD1}	V_{DD} Supply Current During CE "OFF"	CE = −1V to +0.6V, (Note 4)		110		μA
I_{DD2}	V_{DD} Supply Current During CE "ON"	CE = V_{IHC}, T_A = 25°C		20		mA
$I_{DD\ AV1}$	Average V_{DD} Current	T_A = 25°C, Cycle Time = 470 ns, t_{CE} = 300 ns		35		mA
$I_{DD\ AV2}$	Average V_{DD} Current	T_A = 25°C, Cycle Time = 1000 ns, t_{CE} = 300 ns		15		mA
I_{BB}	V_{BB} Supply Current Average			5	100	μA
V_{IL}	Input Low Voltage	t_T = 20 ns	−1.0		0.6	V
V_{IH}	Input High Voltage		2.4		V_{CC}+1	V
V_{ILC}	CE Input Low Voltage		−1.0		1.0	V
V_{IHC}	CE Input High Voltage		V_{DD}−1		V_{DD}+1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.0 mA	0.0		0.45	V
V_{OH}	Output High Voltage	I_{OH} = −2.0 mA	2.4			V

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: The only requirement for the sequence of applying voltage to the device is that V_{DD} or V_{SS} should never be 0.3V more negative than V_{BB}.

Note 3: Typical values are for T_A = 25°C and nominal power supply voltages.

Note 4: The I_{DD} current is to V_{SS}. The I_{BB} current is the sum of all leakage currents.

ac electrical characteristics

$T_A = 0°C$ to $+70°C$, $V_{DD} = 12V \pm 5\%$, $V_{BB} = -5V \pm 5\%$

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
READ, WRITE, READ/MODIFY/WRITE, AND REFRESH CYCLE						
t_{REF}	Time Between Refresh				2	ms
t_{AC}	Address to CE Set-Up Time	t_{AC} is Measured From End of Address Transition	0			ns
t_{AH}	Address Hold Time		50			ns
t_{CC}	CE "OFF" Time		130			ns
t_T	CE Transition Time		10		40	ns
t_{CF}	CE "OFF" to Output High Impedance State		0			ns
t_{TC}	TRI-SHARE Port to CE Set-Up Time		0			ns
t_{TH}	TRI-SHARE Port Hold Time		80			ns
READ CYCLE						
t_{CY}	Cycle Time	$t_T = 20$ ns	470			ns
t_{CE}	CE "ON" Time	$C_{LOAD} = 50$ pF, Load = One TTL Gate	300		3000	ns
t_{CO}	CE Output Delay	Ref 1 = 2.0V, Ref 0 = 0.8V			250	ns
t_{ACC}	Address to Output Access	$t_{ACC} = t_{AC} + t_{CO} + t_T$			270	ns
t_{TL}	CE to TSP		0			ns
WRITE CYCLE						
t_{CY}	Cycle Time		470			ns
t_{CE}	CE "ON" Time		300		3000	ns
t_{WI}	TSP to CE "OFF"		150			ns
t_{CW}	CE to TSP	$t_T = 20$ ns			115	ns
t_D	D_{IN} to CE "OFF"		150			ns
t_{DH}	D_{IN} Hold Time		0			ns
t_{WP}	TSP Pulse Width		50			ns
READ/MODIFY/WRITE CYCLE						
t_{RWC}	Read Modify Write (RMW) Cycle Time		650			ns
t_{CRW}	CE Width During RMW		480		3000	ns
t_{WC}	TSP to CE "ON"	$t_T = 20$ ns	0			ns
t_{W2}	TSP to CE "OFF"	$C_{LOAD} = 50$ pF, Load = One TTL Gate	200			ns
t_{WP}	TSP Pulse Width	Ref 1 - 2.0V, Ref 0 = 0.8V	50			ns
t_D	D_{IN} to CE "OFF"	$t_{ACC} = t_{AC} + t_{CO} + t_T$	150			ns
t_{DH}	D_{IN} Hold Time		0			ns
t_{CO}	CE to Output Delay				180	ns
t_{ACC}	Access Time				270	ns
t_{WD}	TSP to Output High Impedance				250	ns
t_M	Modify Time		0			ns
CAPACITANCE (Note 1)						
C_{AD}	Address Capacitance, $\overline{CS}$	$V_{IN} = V_{SS}$		2		pF
C_{CE}	CE Capacitance	$V_{IN} = V_{SS}$		15		pF
$C_{I/O}$	Data I/O Capacitance	$V_{OUT} = 0V$		8		pF
C_{IN}	TSP Capacitance	$V_{IN} = V_{SS}$		5		pF

Note 1: Capacitance measured with Boonton Meter or effective capacitance calculated from the equation $C = I\Delta t/\Delta V$ with the current equal to a constant 20 mA.

NATIONAL

MOS RAMs
Advance Information

MM5271 TRI-SHARE™ 4096-bit fully TTL compatible dynamic random access read/write memory

general description

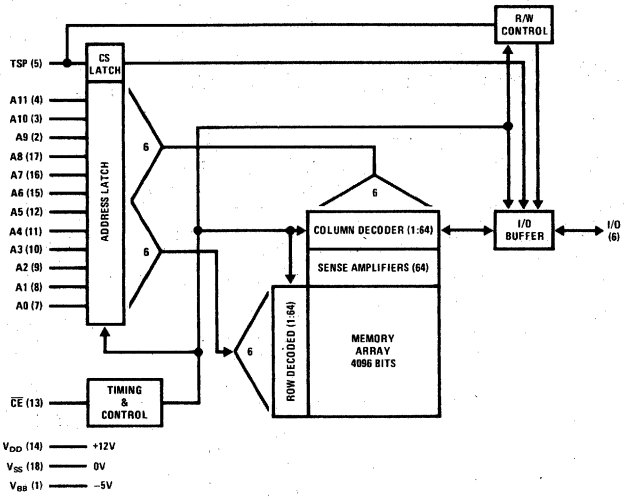
The MM5271 is a fully TTL compatible 4096-bit dynamic random access memory with TRI-SHARE. Because of this unique design feature, National is able to house a 4k device in an 18-pin dual-in-line package. The device is manufactured using N-channel silicon gate technology with a single transistor cell which provides higher density on a monolithic chip and thus lower cost.

The TRI-SHARE Port (TSP) is a multifunction input that, along with a common input/output, allows National to manufacture an 18-pin version of a 4k RAM. The functions controlled by the TSP are read/write, V_{CC}, and logical chip select. In order to understand how the TSP works, consider the timing diagrams. The state of the TSP at the leading edge of the chip enable clock determines whether the device is selected. If it is at a TTL high level, the chip is selected and the device goes into a read mode after chip enable goes high. This high level also controls the V_{CC} function in that it enables a reference voltage for a TTL high output. The supply for the output buffer is V_{DD}, not the TRI-SHARE Port; thus, no special driver is required. In order to perform a write, the TSP must be pulsed low after the minimum hold time and the appropriate data placed on the I/O. When the MM5271 goes into write, the output circuit is disabled. If the TSP is low at the start of the cycle, the memory is not selected but it will be refreshed when the chip enable clock is pulsed.

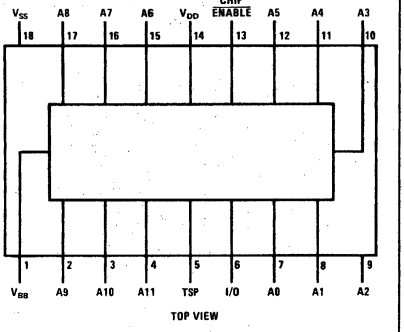
features

- 4096 x 1 bit organization
- Access time 250 ns maximum
- Cycle time 400 ns minimum
- TRI-SHARE port
- High memory density—18-pin package
- TTL compatible inputs
- TRI-STATE® common input/output
- Registers on chip for addresses and chip select
- Two power supplies, +12V, −5V
- Simple read-modify-write operation

block and connection diagrams



Dual-In-Line Package



Order Number MM5271D
See Package 4

Pin Names

A0–A11	Address Inputs*	V_{BB}	Power (−5V)
$\overline{CE}$	Chip Enable	V_{DD}	Power (+12V)
TSP	TRI-SHARE Port	V_{SS}	Ground
I/O	$D_{IN}/\overline{D_{OUT}}$		

*Refresh Addess A0–A5

absolute maximum ratings (Note 1)

Operating Temperature Range	0°C to +70°C
Storage Temperature	−65°C to +150°C
All Input or Output Voltages with Respect to the Most Negative Supply Voltage, V_{BB}	−0.3V to +25V
Supply Voltages V_{DD} and V_{SS} with Respect to V_{BB}	−0.3V to +20V
Power Dissipation	1.0W

dc electrical characteristics

T_A = 0°C to +70°C, V_{DD} = +12V ±5%, V_{BB} (Note 2) = −5V ±5%, V_{SS} = 0V, unless otherwise noted

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP (3)	MAX	UNITS
I_{LI}	Input Load Current	V_{IN} = 0V to V_{IH} max		0.01	10	μA
$\|I_{LO}\|$	Output Leakage Current Up For High Impedance State	$\overline{CE}$ = V_{IH}, V_O = 0V to 5.25V		0.01	10	μA
I_{DD1}	V_{DD} Supply Current During $\overline{CE}$ "OFF"	$\overline{CE}$ = V_{IH}, (Note 4)		1		mA
I_{DD2}	V_{DD} Supply Current During $\overline{CE}$ "ON"	CE = V_{IL}, T_A = 25°C		20		mA
$I_{DD\ AV1}$	Average V_{DD} Current	T_A = 25°C, Cycle Time = 400 ns, t_{CE} = 240 ns		35		mA
$I_{DD\ AV2}$	Average V_{DD} Current	T_A = 25°C, Cycle Time = 1000 ns, t_{CE} = 240 ns		15		mA
I_{BB}	V_{BB} Supply Current Average			5	100	μA
V_{IL}	Input Low Voltage	t_T = 10 ns, *(Figure 4)*	−1.0		0.6	V
V_{IH}	Input High Voltage		2.4		V_{CC}+1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.0 mA	0.0		0.45	V
V_{OH}	Output High Voltage	I_{OH} = −2.0 mA	2.4			V

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: The only requirement for the sequence of applying voltage to the device is that V_{DD} or V_{SS} should never be 0.3V more negative than V_{BB}.

Note 3: Typical values are for T_A = 25°C and nominal power supply voltages.

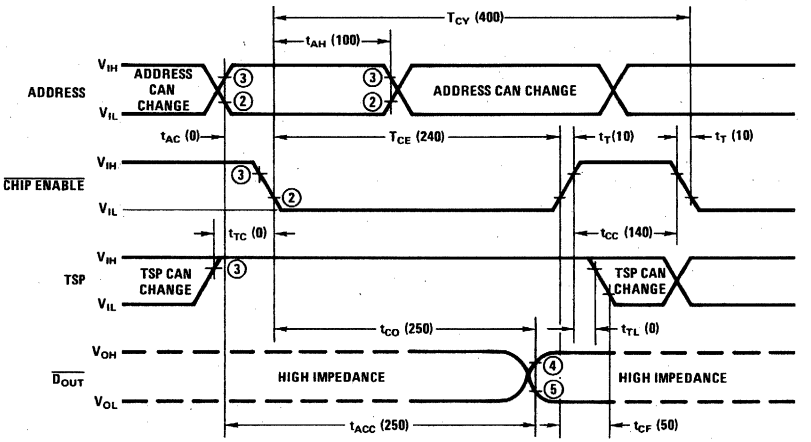
Note 4: The I_{DD} current is to V_{SS}. The I_{BB} current is the sum of all leakage currents.

ac electrical characteristics T_A = 0°C to +70°C, V_{DD} = 12V ±5%, V_{BB} = −5V ±5%

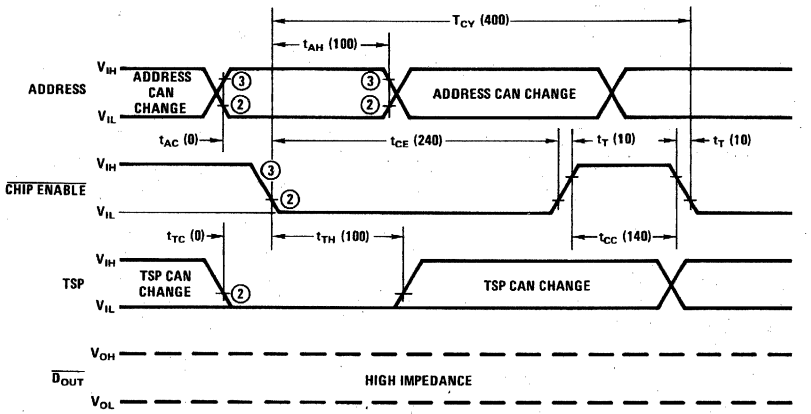
SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
READ, WRITE, READ/MODIFY/WRITE, AND REFRESH CYCLE						
t_{REF}	Time Between Refresh				2	ms
t_{AC}	Address to $\overline{CE}$ Set-Up Time	t_{AC} is MeasuredFrom End of Address Transition	0			ns
t_{AH}	Address Hold Time		100			ns
t_{CC}	$\overline{CE}$ "OFF" Time		140			ns
t_T	$\overline{CE}$ Transition Time				40	ns
t_{CF}	$\overline{CE}$ "OFF" to Output High Impedance State		50			ns
t_{TC}	TRI-SHARE Port to $\overline{CE}$ Set-Up Time		0			ns
t_{TH}	TRI-SHARE Port Hold Time		100			ns
READ CYCLE						
t_{CY}	Cycle Time	t_T = 10 ns	400			ns
t_{CE}	$\overline{CE}$ "ON" Time	C_{LOAD} = 50 pF, Load = One TTL Gate	240		3000	ns
t_{CO}	$\overline{CE}$ Output Delay	Ref 1 = 2.0V, Ref 0 = 0.8V			250	ns
t_{ACC}	Address to Output Access	t_{ACC} = t_{AC} + t_{CO}			250	ns
t_{TL}	$\overline{CE}$ to TSP		0			ns

switching time waveforms

Read Cycle



Refresh Cycle (See Note 1)



Note 1: For Refresh cycle, row and column addresses must be stable before t_{AC} and remain stable for entire t_{AH} period.

Note 2: $V_{IL\ MAX}$ is the reference level for measuring timing of the addresses, T_{SP} and D_{IN} and $\overline{CE}$.

Note 3: $V_{IH\ MIN}$ is the reference level for measuring timing of the addresses, T_{SP} and D_{IN} and $\overline{CE}$.

Note 4: V_{SS} + 2.0V is the reference level for measuring the timing of D_{OUT} for a high output.

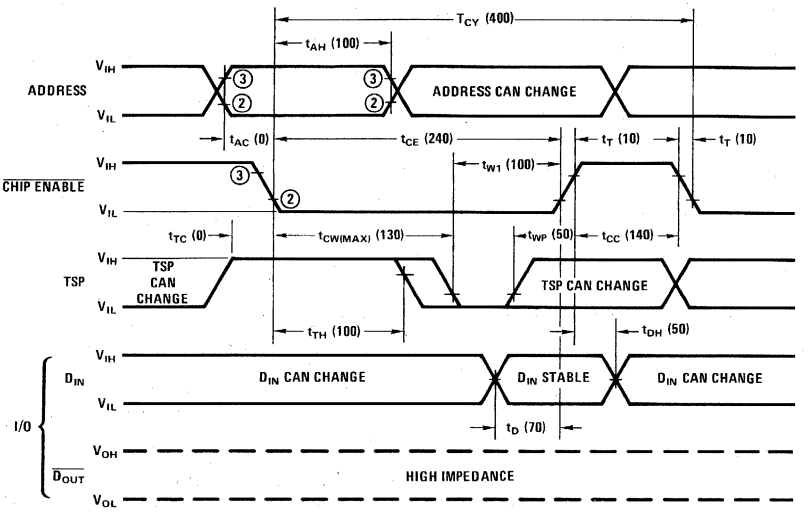
Note 5: V_{SS} + 0.8V is the reference level for measuring timing of D_{OUT} for a low output.

ac electrical characteristics (con't) $T_A = 0°C$ to $+70°C$, $V_{DD} = 12V \pm 5\%$, $V_{BB} = -5V \pm 5\%$

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
WRITE CYCLE						
t_{CY}	Cycle Time		400			ns
t_{CE}	$\overline{CE}$ "ON" Time		240		3000	ns
t_{WI}	TSP to CE "OFF"		100			ns
t_{CW}	$\overline{CE}$ to TSP	t_T = 10 ns, (Note 4)			130	ns
t_D	D_{IN} to $\overline{CE}$ "OFF"		70			ns
t_{DH}	D_{IN} Hold Time		50			ns
t_{WP}	TSP Pulse Width		50			ns

switching time waveforms (con't)

Write Cycle (See Note 4)



Note 1: For Refresh cycle, row and column addresses must be stable before t_{AC} and remain stable for entire t_{AH} period.

Note 2: $V_{IL\ MAX}$ is the reference level for measuring timing of the addresses, T_{SP} and D_{IN} and $\overline{CE}$.

Note 3: $V_{IH\ MIN}$ is the reference level for measuring timing of the addresses, T_{SP} and D_{IN} and $\overline{CE}$.

Note 4: If $t_{CW(MAX)}$ is greater than 130 ns then memory operation is like Read/Modify/Write cycle.

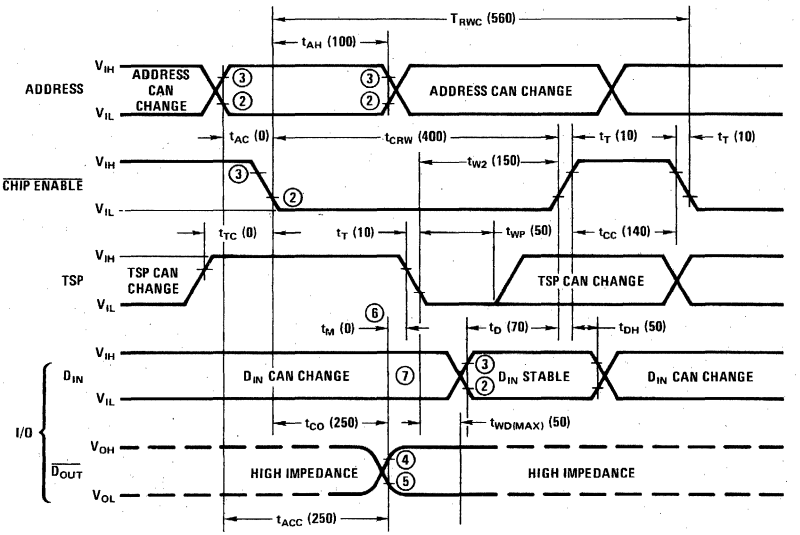
ac electrical characteristics (con't) $T_A = 0°C$ to $+70°C$, $V_{DD} = 12V \pm 5\%$, $V_{BB} = -5V \pm 5\%$

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
READ/MODIFY/WRITE CYCLE						
t_{RWC}	Read Modify Write (RMW) Cycle Time		560			ns
t_{CRW}	$\overline{CE}$ Width During RMW	$t_T = 10$ ns	400		3000	ns
t_{W2}	TSP to $\overline{CE}$ "OFF"	$C_{LOAD} = 50$ pF, Load = One TTL Gate	150			ns
t_{WP}	TSP Pulse Width	Ref 1 - 2.0V, Ref 0 = 0.8V	50			ns
t_D	D_{IN} to $\overline{CE}$ "OFF"	$t_{ACC} = t_{AC} + t_{CO}$	70			ns
t_{DH}	D_{IN} Hold Time		50			ns
t_{CO}	$\overline{CE}$ to Output Delay				250	ns
t_{ACC}	Access Time				250	ns
t_{WD}	TSP to Output High Impedance				50	ns
t_M	Modify Time		0			ns
CAPACITANCE (Note 1)						
C_{AD}	Address Capacitance, $\overline{CS}$	$V_{IN} = V_{SS}$		2		pF
C_{CE}	$\overline{CE}$ Capacitance	$V_{IN} = V_{SS}$		5		pF
$C_{I/O}$	Data I/O Capacitance	$V_{OUT} = 0V$		8		pF
C_{IN}	TSP Capacitance	$V_{IN} = V_{SS}$		5		pF

Note 1: Capacitance measured with Boonton Meter or effective capacitance calculated from the equation $C = I\Delta t/\Delta V$ with the current equal to a constant 20 mA.

switching time waveforms (con't)

Read Modify Write Cycle



Note 1: For Refresh cycle, row and column addresses must be stable before t_{AC} and remain stable for entire t_{AH} period.

Note 2: $V_{IL\ MAX}$ is the reference level for measuring timing of the addresses, T_{SP} and D_{IN} and $\overline{CE}$.

Note 3: $V_{IH\ MIN}$ is the reference level for measuring timing of the addresses, T_{SP} and D_{IN} and $\overline{CE}$.

Note 4: $V_{SS} + 2.0V$ is the reference level for measuring the timing of D_{OUT} for a high output.

Note 5: $V_{SS} + 0.8V$ is the reference level for measuring timing of D_{OUT} for a low output.

Note 6: For minimum cycle, $t_M = 0$, for test purposes $t_M = 10$ ns.

Note 7: If D_{IN} is forced prior to $\overline{D_{OUT}}$ becoming high impedance ($t_{WD(MAX)}$), then maximum ambient temperature should be derated by T_{0V}/T_{CYCLE} (35°C). Where T_{0V} is time between forcing D_{IN} and $\overline{D_{OUT}}$ becoming TRI-STATE.

NATIONAL

MOS RAMs

MM5280 4096-bit dynamic random access memory

general description

National's MM5280 is a 4096 word by 1 bit dynamic RAM. It incorporates the latest memory design features and can be used in a wide variety of applications, from those which require very high speed to ones where low cost and large bit capacity are the prime criteria.

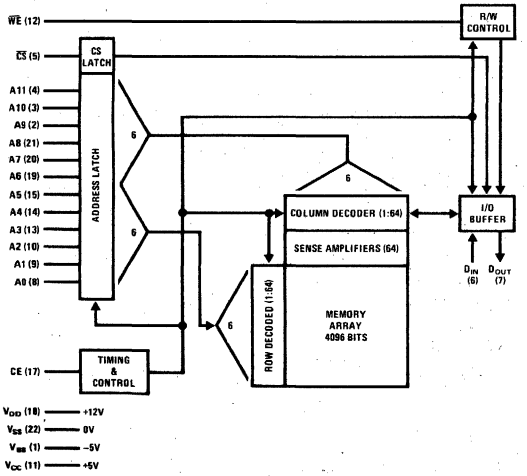
The MM5280 must be refreshed every 2 ms. This can be accomplished by performing a read cycle at each of the 64 row addresses (A0–A5). The chip select input can be either high or low for refresh.

The MM5280 has been designed with minimum production costs as a prime criterion. It is fabricated using N-channel silicon gate MOS technology, which is an ideal choice for high density integrated circuits. The MM5280 uses a single transistor cell to minimize the device area. The single device cell, along with unique design features in the on-chip peripheral circuits, yields a high performance memory device.

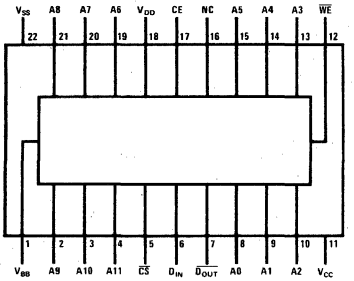
features

- Organization: 4096 x 1
- Access time 200 ns maximum
- Cycle time 400 ns minimum
- Easy system interface
  - One high voltage input—chip enable
  - TTL compatible—all other inputs and output
- Address registers on-chip
- TRI-STATE® output
- Simple read-modify-write operation
- Industry standard pin configuration

block and connection diagrams



Dual-In-Line Package



TOP VIEW

Order Number MM5280D
See Package 5

Pin Names

A0–A11	Address Inputs*	V_{BB}	Power (−5V)
CE	Chip Enable	V_{CC}	Power (+5V)
$\overline{CS}$	Chip Select	V_{DD}	Power (+12V)
D_{IN}	Data Input	V_{SS}	Ground
$\overline{D_{OUT}}$	Data Output	$\overline{WE}$	Write Enable
NC	Not Connected		

*Refresh Address A0–A5

absolute maximum ratings (Note 1)

Operating Temperature Range	0°C to +70°C	Supply Voltages V_{DD}, V_{CC} and V_{SS} with Respect to V_{BB}	−0.3V to +20V
Storage Temperature	−65°C to +150°C	Power Dissipation	1.25W
All Input or Output Voltages with Respect to the Most Negative Supply Voltage, V_{BB}	−0.3V to +25V		

dc electrical characteristics

$T_A = 0°C$ to $+70°C$ $V_{DD} = +12V \pm 5\%$, $V_{CC} = +5V \pm 5\%$, V_{BB} (Note 2) $= -5V \pm 5\%$, $V_{SS} = 0V$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I_{LI}	Input Load Current	$V_{IN} = 0V$ to V_{IH} max, (All Inputs Except CE)		0.01	10	μA
I_{LC}	Input Load Current	$V_{IN} = 0V$ to V_{IHC} max		0.01	10	μA
$\|I_{LO}\|$	Output Leakage Current Up For High Impedance State	CE = V_{ILC} or $\overline{CS}$ = V_{IH}, V_O = 0V to 5.25V		0.01	10	μA
I_{DD1}	V_{DD} Supply Current During CE "OFF"	CE = −1V to +6V, Note 4		110		μA
I_{DD2}	V_{DD} Supply Current During CE "ON"	CE = V_{IHC}, $T_A = 25°C$		20		mA
$I_{DD\ AV1}$	Average V_{DD} Current	$T_A = 25°C$ Cycle Time = 400 ns, t_{CE} = 230 ns		35		mA
$I_{DD\ AV2}$	Average V_{DD} Current	$T_A = 25°C$ Cycle Time = 1000 ns, t_{CE} = 230 ns		15		mA
I_{CC1}	V_{CC} Supply Current During CE "OFF"	CE = V_{ILC} or $\overline{CS}$ = V_{IH}, (Note 5)		0.01	10	μA
I_{BB}	V_{BB} Supply Current Average			5	100	μA
V_{IL}	Input Low Voltage	t_T = 20 ns *(Figure 4)*	−1.0		0.6	V
V_{IH}	Input High Voltage		2.4		V_{CC}+1	V
V_{ILC}	CE Input Low Voltage		−1.0		1.0	V
V_{IHC}	CE Input High Voltage		V_{DD}−1		V_{DD}+1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.0 mA	0.0		0.45	V
V_{OH}	Output High Voltage	I_{OH} = −2.0 mA	2.4		V_{CC}	V

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: The only requirement for the sequence of applying voltage to the device is that V_{DD}, V_{CC}, and V_{SS} should never be 0.3V more negative than V_{BB}.

Note 3: Typical values are for $T_A = 25°C$ and nominal power supply voltages.

Note 4: The I_{DD} and I_{CC} currents flow to V_{SS}. The I_{BB} current is the sum of all leakage currents.

Note 5: During CE "ON" V_{CC} supply current is dependent on output loading, V_{CC} is connected to output buffer only.

ac electrical characteristics $T_A = 0°C$ to $+70°C$, $V_{DD} = 12V \pm 5\%$, $V_{CC} = 5V \pm 5\%$, $V_{BB} = -5V \pm 5\%$

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
READ, WRITE, READ/MODIFY/WRITE, AND REFRESH CYCLE						
t_{REF}	Time Between Refresh				2	ms
t_{AC}	Address to CE Set-Up Time	t_{AC} is Measured From End of Address Transition	0			ns
t_{AH}	Address Hold Time		50			ns
t_{CC}	CE "OFF" Time		130			ns
t_T	CE Transition Time		10		40	ns
t_{CF}	CE "OFF" to Output High Impedance State		0			ns
READ CYCLE						
t_{CY}	Cycle Time		400			ns
t_{CE}	CE "ON" Time		230		3000	ns
t_{CO}	CE Output Delay	C_{LOAD} = 50 pF, Load = 1 TTL Gate, Ref = 2.0V, $t_{ACC} = t_{AC} + t_{CO} + 1\ t_T$			180	ns
t_{ACC}	Address to Output Access				200	ns
t_{WL}	CE to $\overline{WE}$		0			ns
t_{WC}	$\overline{WE}$ to CE "ON"		0			ns

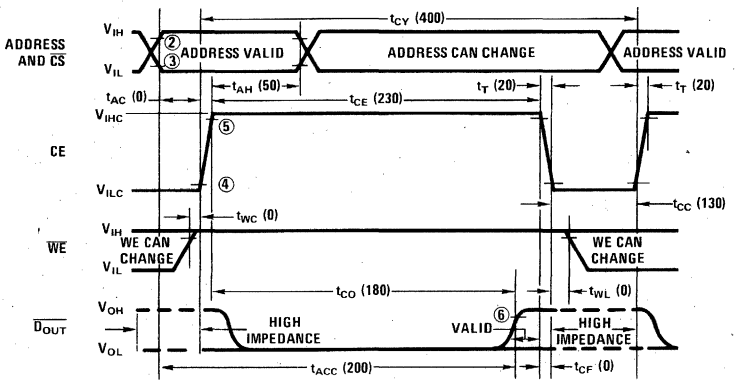
ac electrical characteristics (con't)

$T_A = 0°C$ to $+70°C$, $V_{DD} = 12V \pm 5\%$, $V_{CC} = 5V \pm 5\%$, $V_{BB} = -5\% \pm 5\%$

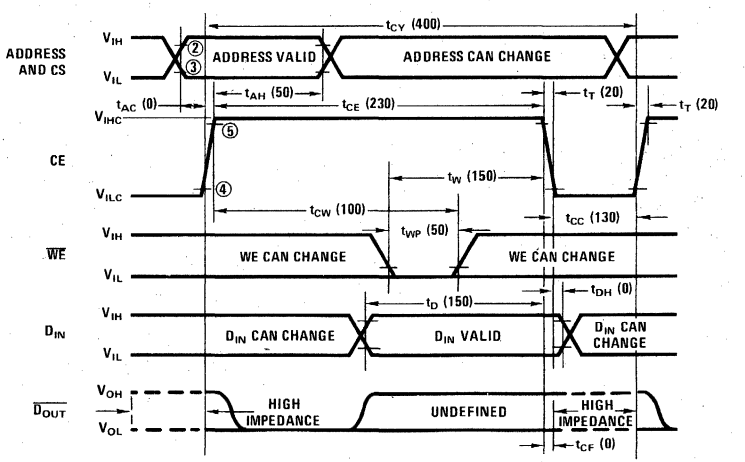
SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
WRITE CYCLE						
t_{CY}	Cycle Time		400			ns
t_{CE}	CE "ON" Time		230		3000	ns
t_W	$\overline{WE}$ to CE "OFF"		150			ns
t_{CW}	CE to $\overline{WE}$	$t_T = 20$ ns	100			ns
t_D	D_{IN} to CE Set-Up		150			ns
t_{DH}	D_{IN} Hold Time		0			ns
t_{WP}	$\overline{WE}$ Pulse Width		50			ns

switching time waveforms

Read and Refresh Cycle ①



Write Cycle



Note 1: For refresh cycle, row and column addresses must be stable before t_{AC} and remain stable for entire t_{AH} period.
Note 2: V_{IL} max is the reference level for measuring timing of the address, $\overline{CS}$ and D_{IN}.
Note 3: V_{IH} min is the reference level for measuring timing of the addresses, $\overline{CS}$ and D_{IN}.
Note 4: $V_{SS} + 2.0V$ is the reference level for measuring timing of CE.
Note 5: $V_{DD} - 2V$ is the reference level for measuring timing of CE.
Note 6: $V_{SS} + 2.0V$ is the reference level for measuring the timing of D_{OUT} for a high output.

ac electrical characteristics (con't)

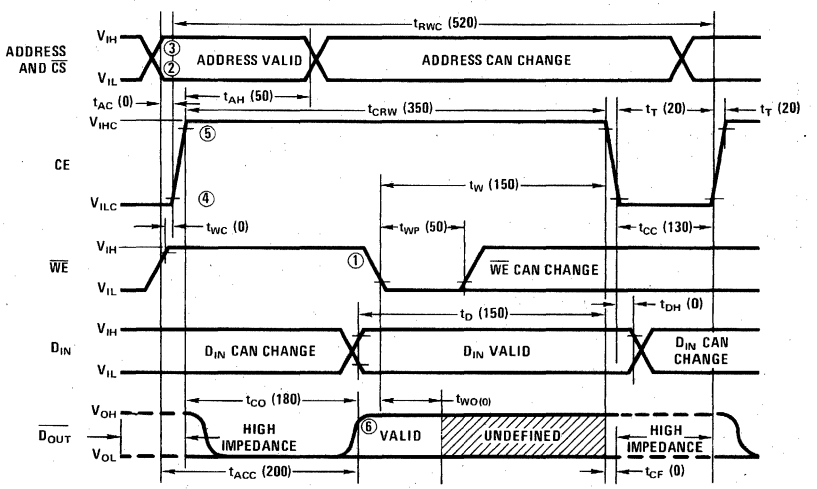
$T_A = 0°C$ to $+70°C$, $V_{DD} = 12V \pm 5\%$, $V_{CC} = 5V \pm 5\%$, $V_{BB} = -5\% \pm 5\%$

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
READ/MODIFY/WRITE CYCLE						
t_{RWC}	Read Modify Write (RMW) Cycle Time		520			ns
t_{CRW}	CE Width During RMW		350		3000	ns
t_{WC}	$\overline{WE}$ to CE "ON"		0			ns
t_W	$\overline{WE}$ to CE "OFF"		150			ns
t_{WP}	$\overline{WE}$ Pulse Width	$t_T = 20$ ns, $C_{LOAD} = 50$ pF, Load = 1 TTL Gate, Ref = 2.0V, $t_{ACC} = t_{AC} + t_{CO} + 1\ t_T$	50			ns
t_D	D_{IN} to CE Set-Up		150			ns
t_{DH}	D_{IN} Hold Time		0			ns
t_{CO}	CE to Output Delay				180	ns
t_{WO}	$\overline{WE}$ to $\overline{D_{OUT}}$ Invalid		0			
t_{ACC}	Access Time				200	ns
CAPACITANCE (Note 1)		$T_A = 25°C$				
C_{AD}	Address Capacitance, $\overline{CS}$	$V_{IN} = V_{SS}$		2		pF
C_{CE}	CE Capacitance	$V_{IN} = V_{SS}$		15		pF
C_{OUT}	Data Output Capacitance	$V_{OUT} = 0V$		5		pF
C_{IN}	D_{IN} and $\overline{WE}$ Capacitance	$V_{IN} = V_{SS}$		4		pF

Note 1: Capacitance measured with Boonton Meter or effective capacitance calculated from the equation $C = I\Delta t/\Delta V$ with the current equal to a constant 20 mA.

switching time waveforms (con't)

Read Modify Write Cycle



Note 1: $\overline{WE}$ must be high until end of t_{CO}.
Note 2: V_{IL} max is the reference level for measuring timing of the address, $\overline{CS}$, D_{IN} and $\overline{WE}$.
Note 3: V_{IH} min is the reference level for measuring timing of the address, $\overline{CS}$, D_{IN} and $\overline{WE}$.
Note 4: $V_{SS} + 2.0V$ is the reference level for measuring timing of CE.
Note 5: $V_{DD} - 2V$ is the reference level for measuring timing of CE.
Note 6: $V_{SS} + 2.0V$ is the reference level for measuring the timing of $\overline{D_{OUT}}$ for a high output.

NATIONAL

MOS RAMs

MM5280-5 4096-bit dynamic random access read/write memory

general description

The MM5280-5 is a slower speed version of National's MM5280. Please refer to the MM5280 specification for pin configuration, block diagram and switching time waveforms.

features

- Access time—270 ns
- Cycle time—470 ns

absolute maximum ratings (Note 1)

Operating Temperature Range	0°C to +70°C
Storage Temperature	−65°C to +150°C
All Input or Output Voltages with Respect to the Most Negative Supply Voltage, V_{BB}	−0.3V to +25V
Supply Voltages V_{DD}, V_{CC} and V_{SS} with Respect to V_{BB}	−0.3V to +20V
Power Dissipation	1.25W

Order Number MM5280D-5
See Package 5

dc electrical characteristics

T_A = 0°C to +70°C V_{DD} = +12V ±5%, V_{CC} = +5V ±5%, V_{BB} (Note 2) = −5V ±5%, V_{SS} = 0V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I_{LI}	Input Load Current	V_{IN} = 0V to V_{IH} max, (All Inputs Except CE)		0.01	10	μA
I_{LC}	Input Load Current	V_{IN} = 0V to V_{IHC} max		0.01	10	μA
$\|I_{LO}\|$	Output Leakage Current Up For High Impedance State	CE = V_{ILC} or $\overline{CS}$ = V_{IH}, V_O = 0V to 5.25V		0.01	10	μA
I_{DD1}	V_{DD} Supply Current During CE "OFF"	CE = −1V to +6V, Note 4		110		μA
I_{DD2}	V_{DD} Supply Current During CE "ON"	CE = V_{IHC}, T_A = 25°C		20		mA
$I_{DD\,AV1}$	Average V_{DD} Current	T_A = 25°C Cycle Time = 400 ns, t_{CE} = 230 ns		35		mA
$I_{DD\,AV2}$	Average V_{DD} Current	T_A = 25°C Cycle Time = 1000 ns, t_{CE} = 230 ns		15		mA
I_{CC1}	V_{CC} Supply Current During CE "OFF"	CE = V_{ILC} or $\overline{CS}$ = V_{IH}, (Note 5)		0.01	10	μA
I_{BB}	V_{BB} Supply Current Average			5	100	μA
V_{IL}	Input Low Voltage	t_T = 20 ns	−1.0		0.6	V
V_{IH}	Input High Voltage		2.4		V_{CC}+1	V
V_{ILC}	CE Input Low Voltage		−1.0		1.0	V
V_{IHC}	CE Input High Voltage		V_{DD}−1		V_{DD}+1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.0 mA	0.0		0.45	V
V_{OH}	Output High Voltage	I_{OH} = −2.0 mA	2.4		V_{CC}	V

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: The only requirement for the sequence of applying voltage to the device is that V_{DD}, V_{CC}, and V_{SS} should never be 0.3V more negative than V_{BB}.

Note 3: Typical values are for T_A = 25°C and nominal power supply voltages.

Note 4: The I_{DD} and I_{CC} currents flow to V_{SS}. The I_{BB} current is the sum of all leakage currents.

Note 5: During CE "ON" V_{CC} supply current is dependent on output loading, V_{CC} is connected to output buffer only.

ac electrical characteristics

$T_A = 0°C$ to $+70°C$, $V_{DD} = 12V \pm 5\%$, $V_{CC} = 5V \pm 5\%$, $V_{BB} = -5V \pm 5\%$

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
READ, WRITE, READ/MODIFY/WRITE, AND REFRESH CYCLE						
t_{REF}	Time Between Refresh				2	ms
t_{AC}	Address to CE Set-Up Time	t_{AC} is Measured From End of Address Transition	0			ns
t_{AH}	Address Hold Time		50			ns
t_{CC}	CE "OFF" Time		130			ns
t_T	CE Transition Time		10		40	ns
t_{CF}	CE "OFF" to Output High Impedance State		0			ns
READ CYCLE						
t_{CY}	Cycle Time		470			ns
t_{CE}	CE "ON" Time		300		3000	ns
t_{CO}	CE Output Delay	$C_{LOAD} = 50$ pF, Load = 1 TTL Gate, Ref = 2.0V, $t_{ACC} = t_{AC} + t_{CO} + 1\,t_T$			250	ns
t_{ACC}	Address to Output Access				270	ns
t_{WL}	CE to $\overline{WE}$		0			ns
t_{WC}	$\overline{WE}$ to CE "ON"		0			ns
WRITE CYCLE						
t_{CY}	Cycle Time		470			ns
t_{CE}	CE "ON" Time		300		3000	ns
t_W	$\overline{WE}$ to CE "OFF"		150			ns
t_{CW}	CE to $\overline{WE}$	$t_T = 20$ ns	130			ns
t_D	D_{IN} to CE Set-Up		150			ns
t_{DH}	D_{IN} Hold Time		0			ns
t_{WP}	$\overline{WE}$ Pulse Width		50			ns
READ/MODIFY/WRITE CYCLE						
t_{RWC}	Read Modify Write (RMW) Cycle Time		590			ns
t_{CRW}	CE Width During RMW		420		3000	ns
t_{WC}	$\overline{WE}$ to CE "ON"		0			ns
t_W	$\overline{WE}$ to CE "OFF"		150			ns
t_{WP}	$\overline{WE}$ Pulse Width	$t_T = 20$ ns, $C_{LOAD} = 50$ pF, Load = 1 TTL Gate, Ref = 2.0V, $t_{ACC} = t_{AC} + t_{CO} + 1\,t_T$	50			ns
t_D	D_{IN} to CE Set-Up		150			ns
t_{DH}	D_{IN} Hold Time		0			ns
t_{CO}	CE to Output Delay				250	ns
t_{WO}	$\overline{WE}$ to $\overline{D_{OUT}}$ Invalid		0			
t_{ACC}	Access Time				270	ns
CAPACITANCE (Note 1)		$T_A = 25°C$				
C_{AD}	Address Capacitance, $\overline{CS}$	$V_{IN} = V_{SS}$		2		pF
C_{CE}	CE Capacitance	$V_{IN} = V_{SS}$		15		pF
C_{OUT}	Data Output Capacitance	$V_{OUT} = 0V$		5		pF
C_{IN}	D_{IN} and $\overline{WE}$ Capacitance	$V_{IN} = V_{SS}$		4		pF

Note 1: Capacitance measured with Boonton Meter or effective capacitance calculated from the equation $C = I\Delta t/\Delta V$ with the current equal to a constant 20 mA.

NATIONAL

MOS RAMs
Advance Information

MM5281 4096-bit fully TTL compatible dynamic random access memory

general description

National's MM5281 is a 4096 word by 1 bit fully TTL compatible dynamic RAM. It incorporates the latest memory design features and can be used in a wide variety of applications, from those which require very high speed to ones where low cost and large bit capacity are the prime criteria.

The MM5281 must be refreshed every 2 ms. This can be accomplished by performing a read cycle at each of the 64 row addresses (A0–A5). The chip select input can be either high or low for refresh.

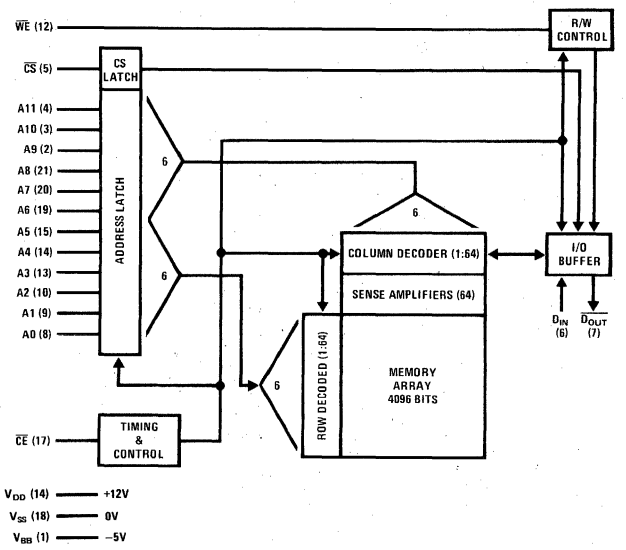
The MM5281 has been designed with minimum production costs as a prime criterion. It is fabricated using N-channel silicon gate MOS technology, which is an ideal choice for high density integrated circuits. The MM5281 uses a single transistor cell to minimize the device area.

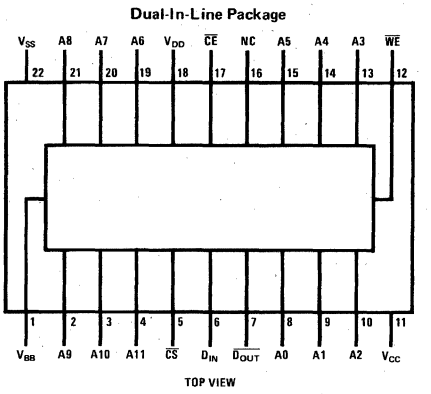
The single device cell, along with unique design features in the on-chip peripheral circuits, yields a high performance memory device.

features

- Organization: 4096 x 1
- Access time 250 ns maximum
- Cycle time 400 ns minimum
- TTL compatible
- Address registers on-chip
- TRI-STATE® output
- Simple read-modify-write operation
- Industry standard pin configuration

block and connection diagrams





Order Number MM5281D
See Package 5

Pin Names

A0–A11	Address Inputs*	V_{BB}	Power (−5V)
$\overline{CE}$	Chip Enable	V_{CC}	Power (+5V)
$\overline{CS}$	Chip Select	V_{DD}	Power (+12V)
D_{IN}	Data Input	V_{SS}	Ground
$\overline{D_{OUT}}$	Data Output	$\overline{WE}$	Write Enable
NC	Not Connected		

*Refresh Address A0–A5

absolute maximum ratings (Note 1)

Operating Temperature Range	0°C to +70°C	Supply Voltages V_{DD}, V_{CC} and V_{SS} with Respect to V_{BB}	−0.3V to +20V
Storage Temperature	−65°C to +150°C	Power Dissipation	1.25W
All Input or Output Voltages with Respect to the Most Negative Supply Voltage, V_{BB}	−0.3V to +25V		

dc electrical characteristics

T_A = 0°C to +70°C V_{DD} = +12V ±5%, V_{CC} = +5V ±5%, V_{BB} (Note 2) = −5V ±5%, V_{SS} = 0V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I_{LI}	Input Load Current	V_{IN} = 0V to V_{IH} max		0.01	10	μA
$\|I_{LO}\|$	Output Leakage Current Up For High Impedance State	$\overline{CE}$ = V_{IH} or $\overline{CS}$ = V_{IH}, V_O = 0V to 5.25V		0.01	10	μA
I_{DD1}	V_{DD} Supply Current During $\overline{CE}$ "OFF"	$\overline{CE}$ = V_{IH}		1		mA
I_{DD2}	V_{DD} Supply Current During $\overline{CE}$ "ON"	$\overline{CE}$ = V_{IL}, T_A = 25°C		20		mA
$I_{DD\,AV1}$	Average V_{DD} Current	T_A = 25°C Cycle Time = 400 ns, t_{CE} = 240 ns		35		mA
$I_{DD\,AV2}$	Average V_{DD} Current	Cycle Time = 1000 ns, t_{CE} = 240 ns		15		mA
I_{CC1}	V_{CC} Supply Current During CE "OFF"	$\overline{CE}$ = V_{IH} or $\overline{CS}$ = V_{IH}, (Note 5)		0.01	10	μA
I_{BB}	V_{BB} Supply Current Average			5	100	μA
V_{IL}	Input Low Voltage	t_T = 10 ns *(Figure 4)*	−1.0		0.6	V
V_{IH}	Input High Voltage		2.4		V_{CC}+1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.0 mA	0.0		0.45	V
V_{OH}	Output High Voltage	I_{OH} = −2.0 mA	2.4		V_{CC}	V

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: The only requirement for the sequence of applying voltage to the device is that V_{DD}, V_{CC}, and V_{SS} should never be 0.3V more negative than V_{BB}.

Note 3: Typical values are for T_A = 25°C and nominal power supply voltages.

Note 4: The I_{DD} and I_{CC} currents flow to V_{SS}. The I_{BB} current is the sum of all leakage currents.

Note 5: During $\overline{CE}$ "ON" V_{CC} supply current is dependent on output loading, V_{CC} is connected to output buffer only.

ac electrical characteristics T_A = 0°C to +70°C, V_{DD} = 12V ±5%, V_{CC} = 5V ±5%, V_{BB} = −5V ±5%

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
READ, WRITE, READ/MODIFY/WRITE, AND REFRESH CYCLE						
t_{REF}	Time Between Refresh				2	ms
t_{AC}	Address to $\overline{CE}$ Set-Up Time	t_{AC} is Measured From End of Address Transition	0			ns
t_{AH}	Address Hold Time		100			ns
t_{CC}	$\overline{CE}$ "OFF" Time		140			ns
t_T	$\overline{CE}$ Transition Time				40	ns
t_{CF}	$\overline{CE}$ "OFF" to Output High Impedance State		50			ns
READ CYCLE						
t_{CY}	Cycle Time		400			ns
t_{CE}	$\overline{CE}$ "ON" Time		240		3000	ns
t_{CO}	$\overline{CE}$ Output Delay	C_{LOAD} = 50 pF, Load = 1 TTL Gate, Ref = 2.0V, t_{ACC} = t_{AC} + t_{CO}			250	ns
t_{ACC}	Address to Output Access				250	ns
t_{WL}	$\overline{CE}$ to $\overline{WE}$		0			ns
t_{WC}	$\overline{WE}$ to $\overline{CE}$ "ON"		0			ns

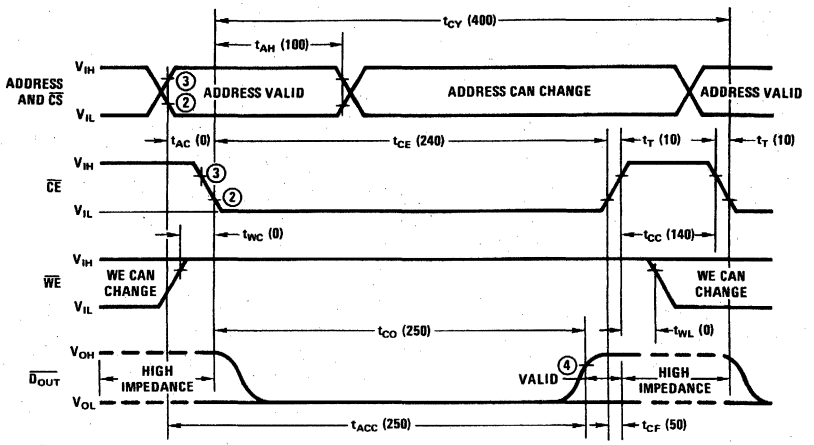
ac electrical characteristics (con't)

$T_A = 0°C$ to $+70°C$, $V_{DD} = 12V \pm 5\%$, $V_{CC} = 5V \pm 5\%$, $V_{BB} = -5\% \pm 5\%$

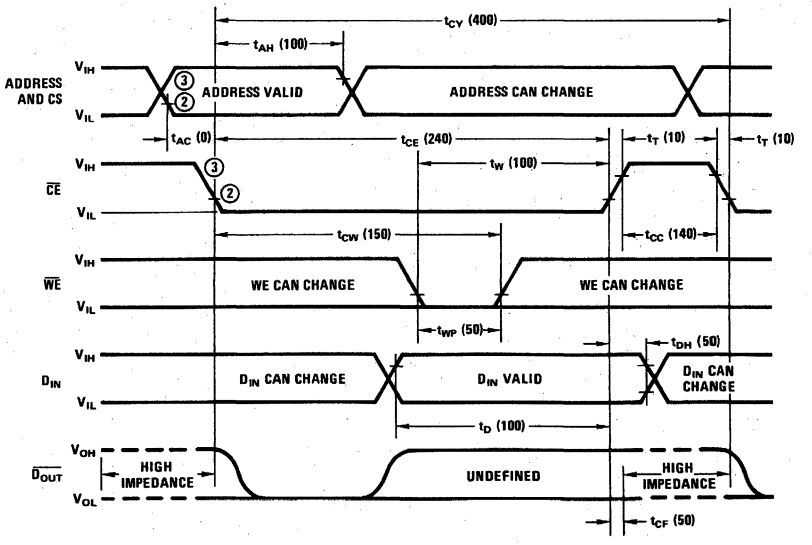
SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
WRITE CYCLE						
t_{CY}	Cycle Time		400			ns
t_{CE}	$\overline{CE}$ "ON" Time		240		3000	ns
t_W	$\overline{WE}$ to $\overline{CE}$ "OFF"		100			ns
t_{CW}	$\overline{CE}$ to $\overline{WE}$	$t_T = 10$ ns	150			ns
t_D	D_{IN} to $\overline{CE}$ Set-Up		100			ns
t_{DH}	D_{IN} Hold Time		50			ns
t_{WP}	$\overline{WE}$ Pulse Width		50			ns

switching time waveforms

Read and Refresh Cycle (See Note 1)



Write Cycle



Note 1: For refresh cycle, row and column addresses must be stable before t_{AC} and remain stable for entire t_{AH} period.
Note 2: V_{IL} max is the reference level for measuring timing of the address, $\overline{CS}$ and D_{IN}.
Note 3: V_{IH} min is the reference level for measuring timing of the addresses, $\overline{CS}$ and D_{IN}.
Note 4: $V_{SS} + 2.0V$ is the reference level for measuring the timing of D_{OUT} for a high output.

ac electrical characteristics (con't)

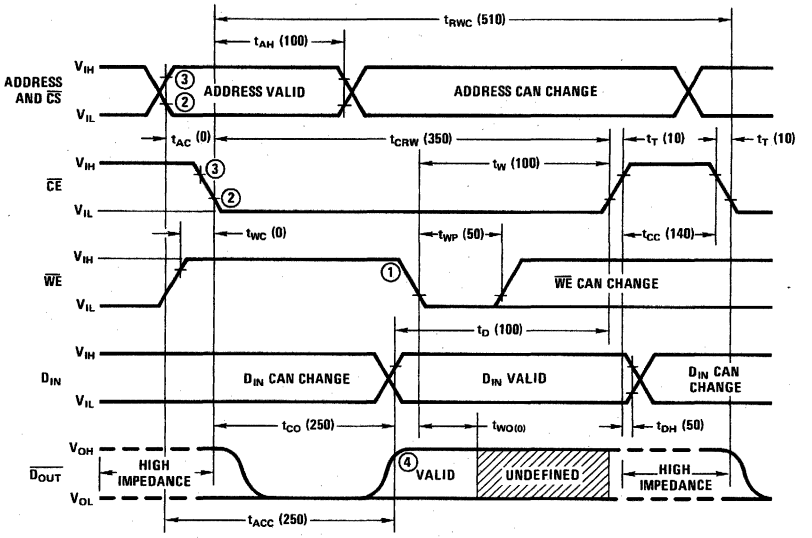
$T_A = 0°C$ to $+70°C$, $V_{DD} = 12V \pm 5\%$, $V_{CC} = 5V \pm 5\%$, $V_{BB} = -5\% \pm 5\%$

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
READ/MODIFY/WRITE CYCLE						
t_{RWC}	Read Modify Write (RMW) Cycle Time		510			ns
t_{CRW}	$\overline{CE}$ Width During RMW		350		3000	ns
t_{WC}	$\overline{WE}$ to $\overline{CE}$ "ON"		0			ns
t_W	$\overline{WE}$ to $\overline{CE}$ "OFF"		100			ns
t_{WP}	$\overline{WE}$ Pulse Width	$t_T = 10$ ns, $C_{LOAD} = 50$ pF, Load = 1 TTL Gate, Ref = 2.0V, $t_{ACC} = t_{AC} + t_{CO}$	50			ns
t_D	D_{IN} to $\overline{CE}$ Set-Up		100			ns
t_{DH}	D_{IN} Hold Time		50			ns
t_{CO}	$\overline{CE}$ to Output Delay				250	ns
t_{WO}	$\overline{WE}$ to $\overline{D_{OUT}}$ Invalid		0			
t_{ACC}	Access Time				250	ns
CAPACITANCE (Note 1)		$T_A = 25°C$				
C_{AD}	Address Capacitance, $\overline{CS}$	$V_{IN} = V_{SS}$		2		pF
C_{CE}	$\overline{CE}$ Capacitance	$V_{IN} = V_{SS}$		5		pF
C_{OUT}	Data Output Capacitance	$V_{OUT} = 0V$		5		pF
C_{IN}	D_{IN} and $\overline{WE}$ Capacitance	$V_{IN} = V_{SS}$		4		pF

Note 1: Capacitance measured with Boonton Meter or effective capacitance calculated from the equation $C = I\Delta t/\Delta V$ with the current equal to a constant 20 mA.

switching time waveforms (con't)

Read Modify Write Cycle



Note 1: $\overline{WE}$ must be high until end of t_{CO}.
Note 2: V_{IL} max is the reference level for measuring timing of the address, $\overline{CS}$, D_{IN} and $\overline{WE}$.
Note 3: V_{IH} min is the reference level for measuring timing of the address, $\overline{CS}$, D_{IN} and $\overline{WE}$.
Note 4: $V_{SS} + 2.0V$ is the reference level for measuring the timing of D_{OUT} for a high output.

Bipolar RAMs

DM5489/DM7489 (SN5489/SN7489)
64-bit random access read/write memory

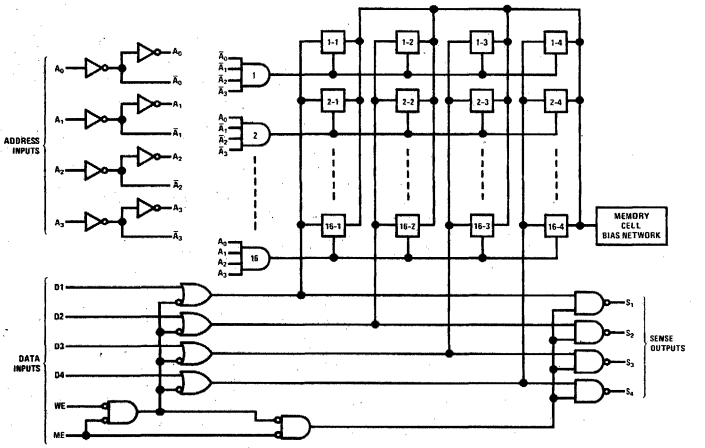
general description

The DM5489/DM7489 is a fully decoded 64-bit RAM organized as 16 4-bit words. The memory is addressed by applying a binary number to the four Address inputs. After addressing, information may be either written into or read from the memory. To write, both the Memory Enable and the Write Enable inputs must be in the logical "0" state. Information applied to the four Write inputs will then be written into the addressed location. To read information from the memory the Memory Enable input must be in the logical "0" state and the Write Enable input in the logical "1" state. Information will be read as the complement of what was written into the memory. When the Memory Enable input is in the logical "1" state, the outputs will go to the logical "1" state.

features

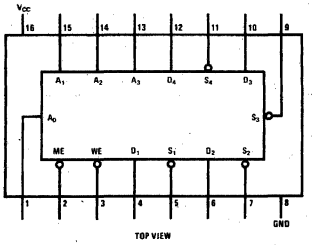
- Series 54/74 compatible
- Organized as 16 4-bit words
- Typical access from chip enable 23 ns
- Typical access 35 ns
- Typical power dissipation 400 mW
- Open collector outputs to permit "wire OR" capability

block diagram



connection diagram

Dual-In-Line Package



Order Number DM5489J or DM7489J
See Package 10
Order Number DM7489N
See Package 15

truth table

MEMORY ENABLE	WRITE ENABLE	OPERATION	OUTPUTS
0	0	Write	Logical "1" State
0	1	Read	Complement of Data Stored in Memory
1	X	Hold	Logical "1" State

absolute maximum ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Output Voltage	5.5V
Operating Temperature Range	
DM5489	−55°C to +125°C
DM7489	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics (Note 2)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	DM5489	V_{CC} = 4.5V		2.0			V
	DM7489	V_{CC} = 4.75V					
Logical "0" Input Voltage	DM5489	V_{CC} = 4.5V				0.8	V
	DM7489	V_{CC} = 4.75V					
Logical "1" Output Current	DM5489	V_{CC} = 5.5V	V_O = 5.25V			100	μA
	DM7489	V_{CC} = 5.25V				20	μA
Logical "0" Output Voltage	DM5489	V_{CC} = 4.5V	I_O = 12 mA			0.4	V
	DM7489	V_{CC} = 4.75V					
Logical "1" Input Current	DM5489	V_{CC} = 5.5V	V_{IN} = 2.4V			40	μA
	DM7489	V_{CC} = 5.25V					
	DM5489	V_{CC} = 5.5V	V_{IN} = 5.5V			1	mA
	DM7489	V_{CC} = 5.25V					
Logical "0" Input Current	DM5489	V_{CC} = 5.5V				−1.6	mA
	DM7489	V_{CC} = 5.25V					
Supply Current	DM5489	V_{CC} = 5.5V	All Inputs at GND		80	120	mA
	DM7489	V_{CC} = 5.25V					
Input Clamp Voltage	DM5489	V_{CC} = 4.5V	I_{IN} = −12 mA			V_{CC} −1.5	V
	DM7489	V_{CC} = 4.75V					

switching characteristics (Over recommended operating ranges of V_{CC} and T_A)

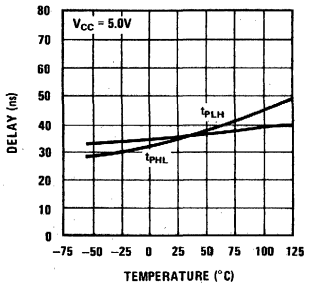
PARAMETER			CONDITIONS	DM5489			DM7489			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Access Time From Address		R_{L1} = 300Ω, R_{L2} = 600Ω, C_L = 30 pF		34	80		34	60	ns
t_{PHL}					35	80		35	60	ns
t_{PLH}	Disable Time From Memory Enable				23	55		23	40	ns
t_{PHL}	Enable Time From Memory Enable				23	55		23	40	ns
t_{SETUP}	Setup Time	Address to Write Enable		0	−14		0	−14		ns
		Data to Write Enable		0	−15		0	−15		ns
		Memory Enable To Write Enable		0	−10		0	−10		ns
t_{HOLD}	Hold Time	Address From Write Enable		5	−7		5	−7		ns
		Data From Write Enable		0	−14		0	−14		ns
		Memory Enable From Write Enable		0	−10		0	−10		ns
t_{WP}	Write Pulse Width			50	20		40	20		ns
t_{SR}	Sense Recovery Time				31	65		31	55	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

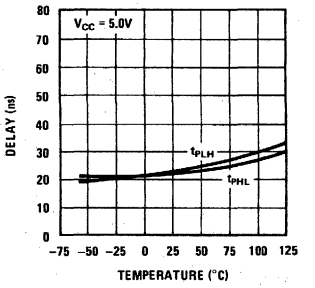
Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DM5489 and across the 0°C to 70°C range for the DM7489. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

typical performance characteristics

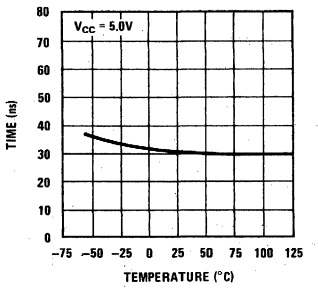
Delay from Address to Output



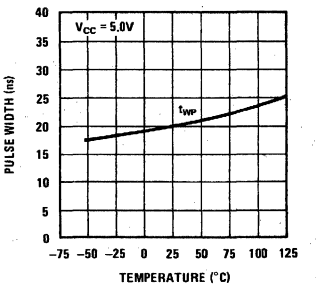
Delay from Memory Enable to Output



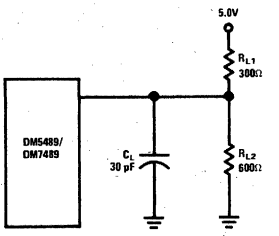
Sense Recovery Time



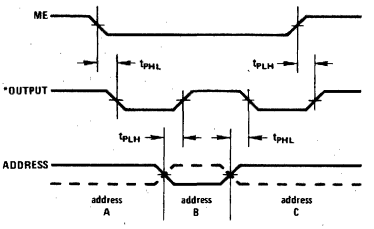
Minimum Write Pulse Width



ac test circuit and switching time waveforms

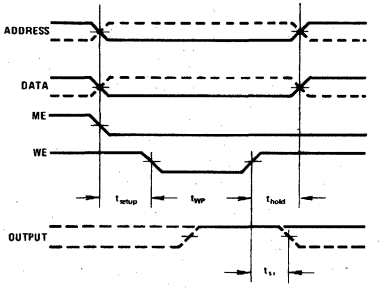


Read Cycle



*Output shown for stored data in address A = 1, in address B = 0.

Write Cycle



NATIONAL

Bipolar RAMs

DM74L89A(SN74L89A)
low power 64-bit random access memory

general description

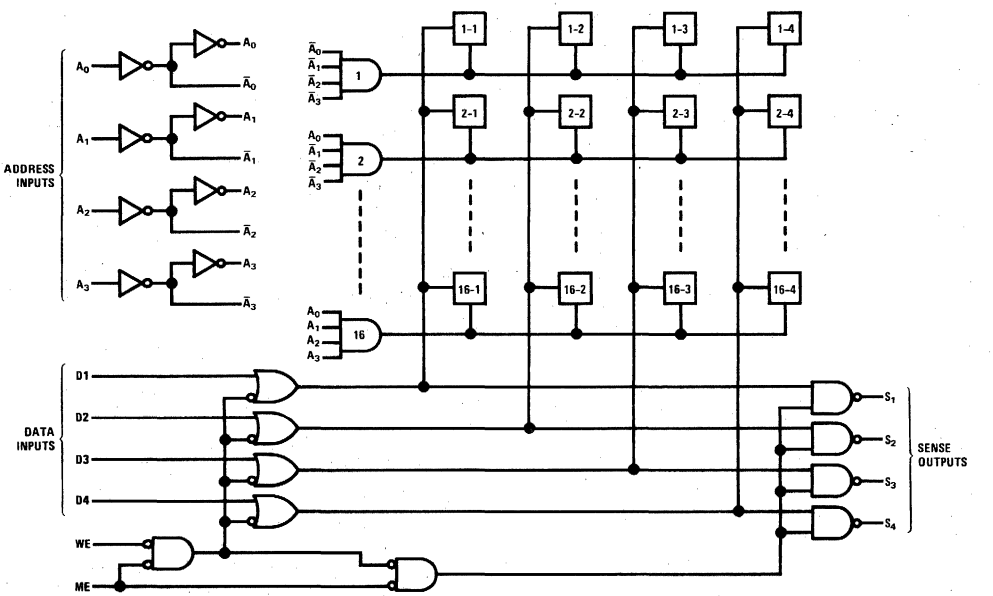
The DM74L89A is a fully decoded 64-bit RAM organized as 16 4-bit words. The memory is addressed by applying a binary number to the four Address inputs. After addressing, information may be either written into or read from the memory. To write, both the Memory Enable and the Write Enable inputs must be in the logical "0" state. Information applied to the four Write inputs will then be written into the addressed location. To read information from the memory the Memory Enable input must be in the logical "0" state and the Write Enable input in the logical "1" state. Information will be read as the complement of what was written into the memory. When the Memory Enable input is in the logical "1" state, the outputs will go to the logical "1" state.

The "A" suffix is used to denote that full "tenth-power" technology has been employed in building this RAM.

features

- Series 54L/74L compatible
- Organized as 16 4-bit words
- Typical access from chip enable 50 ns
- Typical power dissipation 75 mW
- Open collector outputs to permit "wire OR" capability
- Pin compatible with SN7489, 3101, MM5501

logic diagram



Order Number DM74L89AJ
See Package 10
Order Number DM74L89AN
See Package 15
Order Number DM74L89AW
See Package 28

absolute maximum ratings (Note 1)

Supply Voltage	7.0V
Input Voltage	5.5V
Output Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DM74L89A	4.75	5.25	V
Temperature (T_A)			
DM74L89A	0	+70	°C

electrical characteristics (Notes 2 and 3) V_{CC} = 5.0V, T_A = 25°C unless otherwise specified.

PARAMETER	CONDITIONS	LIMITS			UNITS
		MIN	TYP	MAX	
Logical "1" Input Voltage (V_{IH})	V_{CC} = Min	2.0			V
Logical "1" Input Current (I_{IH})	V_{CC} = Max, V_{IN} = 2.4V			10	μA
	V_{CC} = Max, V_{IN} = 5.5V			100	μA
Logical "0" Input Voltage (V_{IL})	V_{CC} = Min			0.7	V
Logical "0" Input Current (I_{IL})	V_{CC} = Max, V_{IN} = 0.3V			−180	μA
Input Clamp Voltage (V_{CD})	V_{CC} = Min, I_{IN} = −12 mA			−1.5	V
Logical "1" Output Current (I_{OH})	V_{CC} = Max, V_{OUT} = 5.5V			50	μA
Logical "0" Output Voltage (V_{OL})	V_{CC} = Min, I_{OUT} = 3.2 mA			0.4	V
Supply Current (I_{CC})	V_{CC} = Max		15	19	mA
Propagation Delay to a Logical "0" From Address to Output (t_{pd0})	V_{CC} = 5.0V, T_A = 25°C		78	150	ns
Propagation Delay to a Logical "1" From Address to Output (t_{pd1})	V_{CC} = 5.0V, T_A = 25°C		90	150	ns
Propagation Delay to a Logical "0" From Memory Enable to Output (t_{pd0})	V_{CC} = 5.0V, T_A = 25°C		33	60	ns
Propagation Delay to a Logical "1" From Memory Enable to Output (t_{pd1})	V_{CC} = 5.0V, T_A = 25°C		64	90	ns
Write Enable Pulse Width	V_{CC} = 5.0V, T_A = 25°C	50	30		ns
Setup Time, Data Input	V_{CC} = 5.0V, T_A = 25°C	0			ns
Hold Time, Data Input	V_{CC} = 5.0V, T_A = 25°C	0			ns
Setup Time, Address Input	V_{CC} = 5.0V, T_A = 25°C	0			ns
Hold Time, Address Input	V_{CC} = 5.0V, T_A = 25°C	0			ns
Setup Time, Memory Enable	V_{CC} = 5.0V, T_A = 25°C	0			ns
Hold Time, Memory Enable	V_{CC} = 5.0V, T_A = 25°C	0			ns
Sense Recovery Time From Write Enable (t_{SR})	V_{CC} = 5.0V, T_A = 25°C		110	165	ns
Disable Time From Write Enable ($t_{\overline{EN}}$)	V_{CC} = 5.0V, T_A = 25°C		47	71	ns

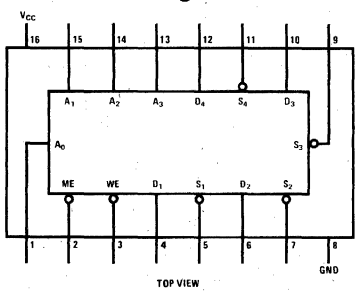
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C range for the DM74L89. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltage referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Only one output at a time should be shorted.

connection diagram (Dual-In-Line Package)



TOP VIEW

truth table

MEMORY ENABLE	WRITE ENABLE	OPERATION	OUTPUTS
0	0	Write	Logical "1" State
0	1	Read	Complement of Data Stored in Memory
1	X	Hold	Logical "1" State

NATIONAL

Bipolar RAMs

DM54S189/DM74S189 64-bit random access memories with TRI-STATE® outputs

general description

These 64-bit active-element memories are monolithic Schottky-clamped transistor-transistor logic (TTL) arrays organized as 16 words of four-bits each. They are fully decoded and feature a chip-enable input to simplify decoding required to achieve the desired system organization. The memories feature PNP input transistors that reduce the low level input current requirement to a maximum of −0.25 mA, only one-eighth that of a DM54S/DM74S standard load factor. The chip-enable circuitry is implemented with minimal delay times to compensate for added system decoding.

The TRI-STATE output combines the convenience of an open-collector with the speed of a totem-pole output; it can be bus-connected to other similar outputs, yet it retains the fast-rise-time characteristics of the TTL totem-pole output. Systems utilizing data-bus lines with a defined pull-up impedance can employ the open-collector DM54S289.

Write Cycle: The complement of the information at the data input is written into the selected location when both the chip-enable input and the read/write input are low. While the read/write input is low, the outputs are in the high-impedance state. When a number of the DM54S189 outputs are bus-connected, this high-impedance state will neither load nor drive the bus line, but it will allow the bus line to be driven by another active output or a passive pull-up if desired.

Read Cycle: The stored information (complement of information applied at the data inputs during the write cycle) is available at the outputs when the read/write input is high and the chip-enable is low. When the chip-enable input is high, the outputs will be in the high-impedance state.

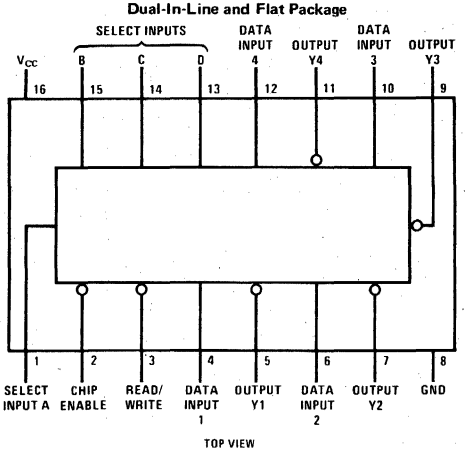
The fast access time of the DM54S189 makes it particularly attractive for implementing high-performance memory functions requiring access times on the order of 25 ns. The high capacitive-drive capability of the outputs permits expansion without additional output buffering. The unique functional capability of the DM54S189 outputs being at a high impedance during writing combined with the data inputs being inhibited during reading means that both data inputs and outputs can be connected to the data lines of a bus-organized system without the need for interface circuits.

features

- Schottky-clamped for high-speed applications:
  - access from chip-enable input 12 ns typ
  - access from address inputs 25 ns typ
- TRI-STATE outputs drive bus-organized systems and/or high capacitive loads
- DM54S289, DM74S289 are functionally equilvalent, have open-collector outputs, and are compatible with Intel 3101A in most applications
- DM54S189 is guaranteed for operation over the full military temperature range of −55°C to +125°C
- Compatible with most TTL and DTL logic circuits
- Chip-enable input simplifies system decoding

connection diagram

Dual-In-Line and Flat Package



TOP VIEW

truth table

FUNCTION	INPUTS		OUTPUT
	CHIP ENABLE	READ/ WRITE	
Write (Store Complement of Data)	L	L	High Impedance
Read	L	H	Stored Data
Inhibit	H	X	High Impedance

H = High Level
L = Low Level
X = Don't Care

Order Number DM54S189J or DM74S189J
See Package 10
Order Number DM74S189N
See Package 15

absolute maximum ratings (Note 1)

Supply Voltage, V_{CC}	7.0V
Input Voltage	5.5V
Output Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DM54S189	4.5	5.5	V
DM74S189	4.75	5.25	V
Temperature (T_A)			
DM54S189	−55	+125	°C
DM74S189	0	+70	°C

electrical characteristics

over recommended operating free-air temperature range (unless otherwise noted) (Notes 2 and 3)

PARAMETER		CONDITIONS		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
V_{IH}	High Level Input Voltage			2			V
V_{IL}	Low-Level Input Voltage					0.8	V
V_{OH}	High-Level Output Voltage	V_{CC} = Min	I_{OH} = −2.0 mA, DM54S189	2.4	3.4		V
			I_{OH} = −6.5 mA, DM74S189	2.4	3.2		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA	DM54S189			0.5	V
			DM74S189			0.45	
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7				25	μA
I_I	High Level Input Current at Maximum Voltage	V_{CC} = Max, V_I = 5.5V				1.0	mA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.45V				−250	μA
I_{OS}	Short Circuit Output Current (Note 4)	V_{CC} = Max, V_O = 0V		−30		−100	mA
I_{CC}	Supply Current (Note 5)	V_{CC} = Max			75	110	mA
V_{IC}	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
I_{OZH}	TRI-STATE Output Current, High Level Voltage Applied	V_{CC} = Max, V_O = 2.4V				50	μA
I_{OZL}	TRI-STATE Output Current, Low Level Voltage Applied	V_{CC} = Max, V_O = 0.45V				−50	μA

switching characteristics

over recommended operating ranges of T_A and V_{CC} (unless otherwise noted)

PARAMETER			CONDITIONS	LIMITS DM54S189 MIN	LIMITS DM54S189 TYP(1)	LIMITS DM54S189 MAX	LIMITS DM74S189 MIN	LIMITS DM74S189 TYP(1)	LIMITS DM74S189 MAX	UNITS
t_{AA}	Access Times From Address		C_L = 30 pF, R_L = 280Ω, *(Figure 1)*		25	50		25	35	ns
t_{CZH}	Output Enable Time to High Level	Access Times From Chip Enable			12	25		12	17	ns
t_{CZL}	Output Enable Time to Low Level				12	25		12	17	ns
t_{WZH}	Output Enable Time to High Level	Sense Recovery Times From Read/Write			22	40		22	35	ns
t_{WZL}	Output Enable Time to Low Level				22	40		22	35	ns

switching characteristics (con't)

PARAMETER			CONDITIONS	LIMITS						UNITS
				DM54S189			DM74S189			
				MIN	TYP(1)	MAX	MIN	TYP(1)	MAX	
t_{CHZ}	Output Disable Time From High Level	Disable Times From Chip Enable	C_L = 5 pF, R_L = 280Ω *(Figure 1)*		12	25		12	17	ns
t_{CLZ}	Output Disable Time From Low Level				12	25		12	17	ns
t_{WHZ}	Output Disable Time From High Level	Disable Times From Read/Write			12			12		ns
t_{WLZ}	Output Disable Time From Low Level				12			12		ns
t_{WP}	Width of Write-Enable Pulse (Read/Write Low)			25			25			ns
t_{ASW}	Set-Up Time *(Figure 1)*	Address to Read/Write		0			0			ns
t_{DSW}		Data to Read/Write		25			25			
t_{CSW}		Chip-Enable to Read/Write		0			0			
t_{AHW}	Hold Time *(Figure 1)*	Address From Read/Write		0			0			ns
t_{DHW}		Data From Read/Write		0			0			
t_{CHW}		Chip-Enable From Read/Write		0			0			

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

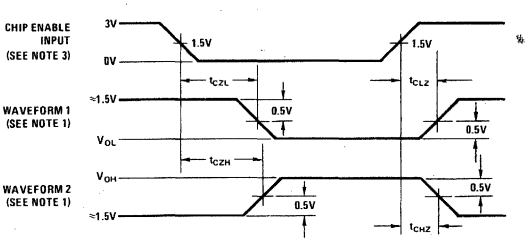
Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DM54S189 and across the 0°C to +70°C range for the DM74S189. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

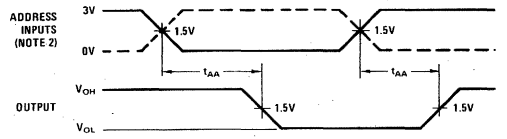
Note 4. Only one output at a time should be shorted.

Note 5: I_{CC} is measured with all inputs grounded, and the outputs open.

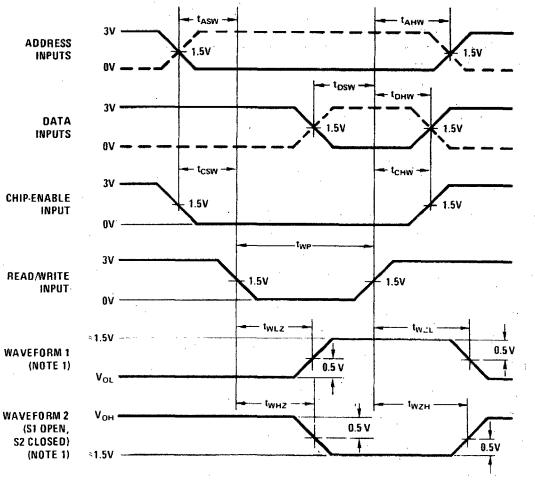
switching time waveforms



Enable and Disable Time From Chip Enable



Access Time From Address Inputs



Write Cycle

FIGURE 1

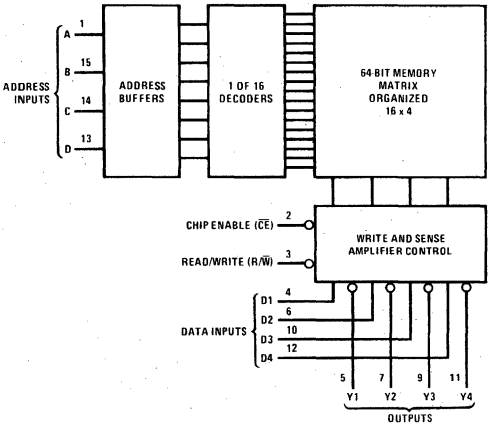
Note 1: Waveform 1 is for the output with internal conditions such that the output is low except when disabled. Waveform 2 is for the output with internal conditions such that the output is high except when disabled.

Note 2. When measuring delay times from address inputs, the chip enable input is low and the read/write input is high.

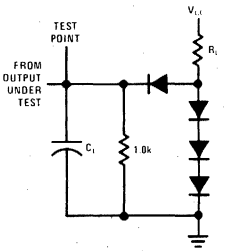
Note 3: When measuring delay times from chip enable input, the address inputs are steady-state and the read/write input is high.

Note 4: Input waveforms are supplied by pulse generators having the following characteristics: $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns, PRR ≤ 1 MHz, and $Z_{OUT} \approx 50\Omega$.

block diagram



ac test circuit



C_L includes probe and jig capacitance.
All diodes are 1N3064.

NATIONAL

Bipolar RAMs

DM54S200/DM74S200 256-bit read/write schottky memories with TRI-STATE® outputs

general description

The DM54S200/DM74S200 256-bit active-element memories are monolithic transistor-transistor logic (TTL) integrated circuits organized as 256 words of one bit each. They are fully decoded and have three gated memory-enable inputs to simplify decoding required to achieve the desired system organization. The memories feature PNP input transistors which reduce the low-level input current requirement to a maximum of −0.25 milliamperes, only one-eighth that of a normalized Series 54S/74S load factor. The memory-enable circuitry is implemented with minimal delay times to compensate for added system decoding.

The TRI-STATE output combines the convenience of an open-collector with the speed of a totem-pole output; it can be bus-connected to other similar outputs, yet it retains the fast-rise-time characteristics of the TTL totem-pole output.

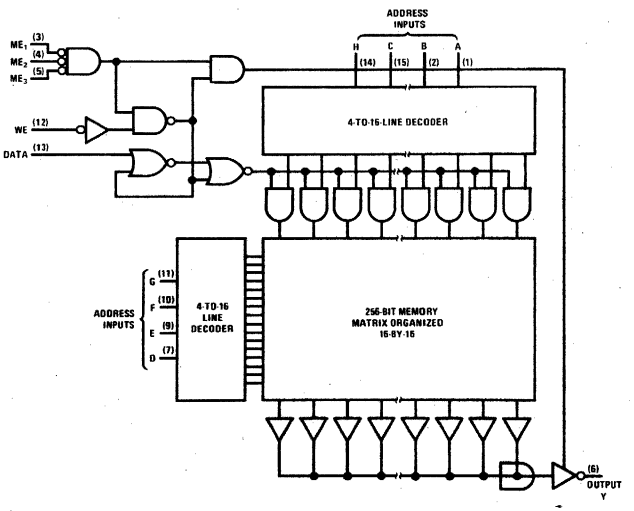
Write Cycle: The complement of the information at the data input is written into the selected location when all memory-enable inputs and write-enable input are low. While the write-enable input is low, the output is in the high-impedance state. When a number of outputs are bus-connected, this high-impedance output state will neither load nor drive the bus line, but it will allow the bus line to be driven by another active output or a passive pull-up if desired.

Read Cycle: The stored information (complement of information applied at the data input during the write cycle) is available at the output when the write-enable input is high and the three memory-enable inputs are low. When any one of the memory enable inputs is high, the output will be in the high-impedance state.

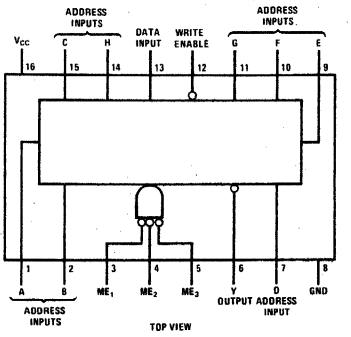
features

- Schottky-clamped for high-speed memory systems:
  - Access from memory-enable inputs 20 ns typ
  - Access from address inputs 31 ns typ
  - Power dissipation 1.7 mW/bit typ
- TRI-STATE output for driving bus-organized systems and/or highly capacitive loads
- Fully decoded, organized as 256 words of one bit each
- Compatible with most TTL and DTL logic circuits
- Multiple memory-enable inputs to minimize external decoding

block and connection diagrams



Dual-In-Line and Flat Package



Order Number DM54S200J or DM74S200J
See Package 10

Order Number DM74S200N
See Package 15

Order Number DM54S200W or DM74S200W
See Package 28

absolute maximum ratings (Note 1)

Supply Voltage, V_{CC}	7.0V
Input Voltage	5.5V
Output Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DM54S200	4.5	5.5	V
DM74S200	4.75	5.25	V
Temperature (T_A)			
DM54S200	−55	+125	°C
DM74S200	0	+70	°C

recommended operating conditions

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
High Level Output Current (I_{OH})					
DM54S200				−2.0	mA
DM74S200				−5.2	mA
Low Level Output Current (I_{OL})				16	mA
Width of Write Enable Pulse (t_W)					
DM54S200		50			ns
DM74S200		40			ns
Setup Time (t_{SETUP})					
Address to Write Enable		0			ns
Data to Write Enable		0			ns
Memory Enable to Write Enable		0			ns
Hold Time (t_{HOLD})					
Address from Write Enable		10			ns
Data from Write Enable		10			ns
Memory Enable from Write Enable		0			ns

electrical characteristics (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
High Level Input Voltage (V_{IH})			2.0			V
Low Level Input Voltage (V_{IL})					0.8	V
Input Clamp Voltage (V_I)	V_{CC} = Min, I_I = −18 mA				−1.2	V
High Level Output Voltage (V_{OH})	V_{CC} = Min, V_{IH} = 2.0V, V_{IL} = 0.8V, I_{OH} = Max		2.4			V
Low Level Output Voltage (V_{OL})	V_{CC} = Min, V_{IH} = 2.0V, V_{IL} = 0.8V, I_{OL} = Max	DM54S200			0.5	V
		DM74S200			0.45	
Off State (High Impedance State) Output Current ($I_{O(OFF)}$)	V_{CC} = Max, V_{IH} = 2.0V, V_O = 2.4V				50	μA
	V_{CC} = Max, V_{IH} = 2.0V, V_O = 0.5V				−50	μA
Input Current at Maximum Input Voltage (I_I)	V_{CC} = Max, V_I = 5.5V				1.0	mA
High Level Input Current (I_{IH})	V_{CC} = Max, V_I = 2.7V				25	μA
Low Level Input Current (I_{IL})	V_{CC} = Max, V_I = 0.5V				−250	μA
Short Circuit Output Current (I_{OS}) (Note 3)	V_{CC} = Max		−30		−100	mA
Supply Current (I_{CC})	V_{CC} = Max (Note 5)			87	130	mA

switching characteristics All Typical Values are at V_{CC} = 5.0V, T_A = 25°C. (Note 2)

SYMBOL	PARAMETER	PARAMETER CONDITIONS	TEST CONDITIONS	DM54S200			DM74S200			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Propagation Delay Time, Low to High Level Output	Access Time from Address	C_L = 30 pF, R_L = 300Ω		33	70		33	50	ns
t_{PHL}	Propagation Delay Time, High to Low Level Output	Access Time from Address			29	70		29	50	ns
t_{ZH}	Output Enable Time to High Level	Access Times from Memory Enable			21	45		21	35	ns
t_{ZL}	Output Enable Time to Low Level	Access Times from Memory Enable			10	30		10	20	ns
t_{ZH}	Output Enable Time to High Level	Sense Recovery Times from Write Enable			24	50		24	40	ns
t_{ZL}	Output Enable Time to Low Level	Sense Recovery Times from Write Enable			12	50		12	40	ns
t_{HZ}	Output Disable Time from High Level	Disable Times from Memory Enable	C_L = 5.0 pF, R_L = 300Ω		7.0	30		7.0	20	ns
t_{LZ}	Output Disable Time from Low Level	Disable Times from Memory Enable			20	45		20	35	ns
t_{HZ}	Output Disable Time from High Level	Disable Times from Write Enable			13	40		13	30	ns
t_{LZ}	Output Disable Time from Low Level	Disable Times from Write Enable			16	40		16	30	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for DM54S200 and across the 0°C to +70°C range for the DM74S200. All typicals are given for V_{CC} = 5.0V and T_A = +25°C.

Note 3: Duration of the short-circuit should not exceed one second.

Note 4: All voltage values are with respect to network ground terminal.

Note 5: I_{CC} is measured with the write enable and memory enable inputs grounded, all other inputs at 4.5V, and the output open.

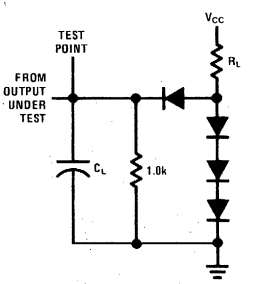
truth table

FUNCTION	INPUTS		OUTPUT
	MEMORY ENABLE†	WRITE ENABLE	
Write (Store Complement of Data)	L	L	High Impedance
Read	L	H	Stored Data
Inhibit	H	X	High Impedance

H = high level, L = low level, X = irrelevant

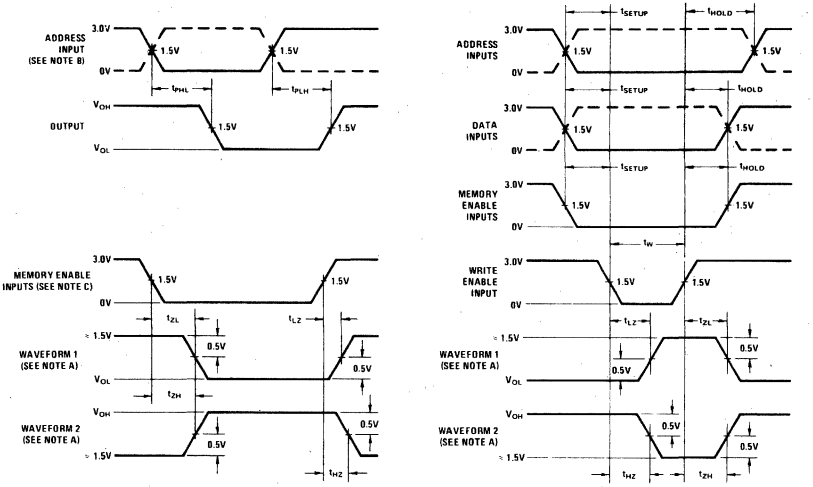
†For memory enable: L = all ME inputs low; H = one or more ME inputs high.

ac test circuit



C_L INCLUDES PROBE AND JIG CAPACITANCE.
ALL DIODES ARE 1N3064.

switching time waveforms



NOTE A: WAVEFORM 1 IS FOR THE OUTPUT WITH INTERNAL CONDITIONS SUCH THAT THE OUTPUT IS LOW EXCEPT WHEN DISABLED. WAVEFORM 2 IS FOR THE OUTPUT WITH INTERNAL CONDITIONS SUCH THAT THE OUTPUT IS HIGH EXCEPT WHEN DISABLED.

NOTE B: WHEN MEASURING DELAY TIMES FROM ADDRESS INPUTS, THE MEMORY ENABLE INPUTS ARE LOW AND THE WRITE ENABLE INPUT IS HIGH.

NOTE C: WHEN MEASURING DELAY TIMES FROM MEMORY ENABLE INPUTS, THE ADDRESS INPUTS ARE STEADY-STATE AND THE WRITE ENABLE INPUT IS HIGH.

NOTE D: INPUT WAVEFORMS ARE SUPPLIED BY PULSE GENERATORS HAVING THE FOLLOWING CHARACTERISTICS: $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns, PRR ≤ 1.0 MHz, AND $Z_{OUT} \approx 50\Omega$.

NATIONAL

Bipolar RAMs

DM54S206/DM74S206 256-bit read/write schottky memories with open-collector outputs

general description

The DM54S206/DM74S206 256-bit active-element memories are monolithic transistor-transistor logic (TTL) integrated circuits organized as 256 words of one bit each. They are fully decoded and have three gated memory-enable inputs to simplify decoding required to achieve the desired system organization. The memories feature PNP input transistors which reduce the low-level input current requirement to a maximum of −0.25 milliamperes, only one-eighth that of a normalized Series 54S/74S load factor. The memory-enable circuitry is implemented with minimal delay times to compensate for added system decoding.

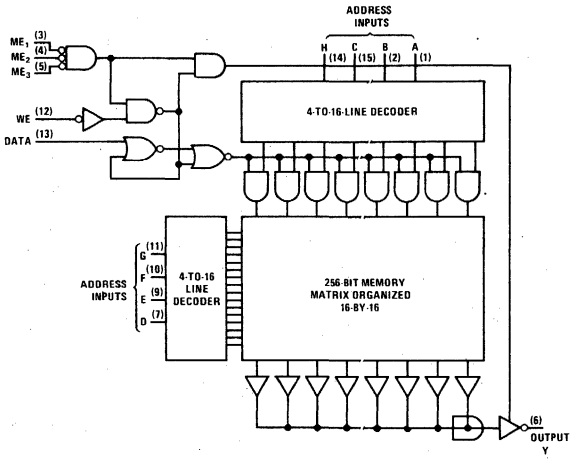
Write Cycle: The complement of the information at the data input is written into the selected location when all memory-enable inputs and write-enable input are low. While the write-enable input is low, the output is off.

Read Cycle: The stored information (complement of information applied at the data input during the write cycle) is available at the output when the write-enable input is high and the three memory-enable inputs are low. When any one of the memory enable inputs is high, the output will be off.

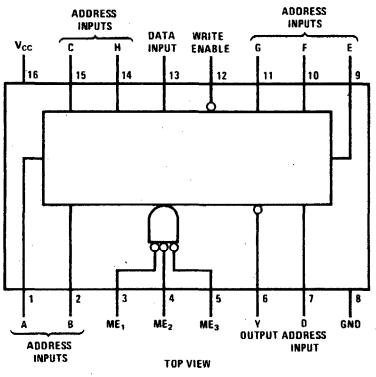
features

- Schottky-clamped for high-speed memory systems:
  - Access from memory-enable inputs 17 ns typ
  - Access from address inputs 35 ns typ
  - Power dissipation 1.4 mW/bit typ
- Open-collector output for word expansion
- Fully decoded, organized as 256 words of one bit each
- Compatible with most TTL and DTL logic circuits
- Multiple memory-enable inputs to minimize external decoding

block and connection diagrams



Dual-In-Line and Flat Package



Order Number DM54S206J or DM74S206J
See Package 10

Order Number DM74S206N
See Package 15

Order Number DM54S206W or DM74S206W
See Package 28

absolute maximum ratings (Note 1)

Supply Voltage, V_{CC}	7.0V
Input Voltage	5.5V
Output Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DM54S206	4.5	5.5	V
DM74S206	4.75	5.25	V
Temperature (T_A)			
DM54S206	−55	+125	°C
DM74S206	0	+70	°C

operating conditions

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Low Level Output Current (I_{OL})				16	mA
Width of Write Enable Pulse (t_W)					
DM54S206		50			ns
DM74S206		40			ns
Setup Time (t_{SETUP})					
Address to Write Enable		0			ns
Data to Write Enable		0			ns
Memory Enable to Write Enable		0			ns
Hold Time (t_{HOLD})					
Address from Write Enable		10			ns
Data from Write Enable		10			ns
Memory Enable from Write Enable		0			ns

electrical characteristics (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
High-Level Input Voltage (V_{IH})		2			V
Low-Level Input Voltage (V_{IL})				0.8	V
Input clamp voltage	V_{CC} = Min, I_I = −18 mA			−1.2	V
High-Level Output Current (I_{OH})	V_{CC} = Min, V_{IH} = 2V, V_{IL} = 0.8V				
	V_{OH} = 2.4V			40	μA
	V_{OH} = 5.5V			100	μA
Low-Level Output Voltage (V_{OL}) DM54S206 / DM74S206	V_{CC} = Min, V_{IH} = 2V, V_{IL} = 0.8V, I_{OL} = Max			0.5 / 0.45	V
Input Current at Maximum Input Voltage (I_I)	V_{CC} = Max, V_I = 5.5V			1	mA
High-Level Input Current (I_{IH})	V_{CC} = Max, V_I = 2.7V			25	μA
Low-Level Input Current (I_{IL})	V_{CC} = Max, V_I = 0.5V			−250	μA
Supply Current (I_{CC})	V_{CC} = Max, Note 2		70	130	mA

switching characteristics

All typical values are at V_{CC} = 5.0V, T_A = 25°C. (Note 2)

PARAMETER	CONDITIONS	LIMITS						UNITS
		DM54S206			DM74S206			
		MIN	TYP	MAX	MIN	TYP	MAX	
Access Times from Address (t_{PLH})	C_L = 30 pF, R_L = 300Ω		38	80		38	60	ns
Access Times from Address (t_{PHL})			32	80		32	60	ns
Disable Time from Memory Enable (t_{PLH})			21	45		21	35	ns
Enable Time from Memory Enable (t_{PHL})			13	35		13	25	ns
Disable Time from Write Enable (t_{PLH})			20	50		20	40	ns
Sense-Recovery Time (t_{SR})			14	50		14	40	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for DM54S206 and across the 0°C to +70°C range for the DM74S206. All typicals are given for V_{CC} = 5.0V and T_A = +25°C.

Note 3: All voltage values are with respect to network ground terminal.

Note 4: I_{CC} is measured with the write enable and memory enable inputs grounded, all other inputs at 4.5V, and the output open.

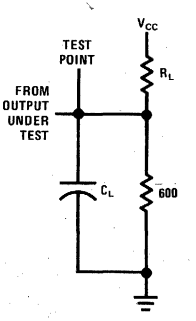
truth table

FUNCTION	INPUTS		OUTPUT
	MEMORY ENABLE†	WRITE ENABLE	
Write (Store Complement of Data)	L	L	H
Read	L	H	Stored Data
Inhibit	H	X	H

H = high level, L = low level, X = irrelevant

†For memory enable: L = all ME inputs low; H = one or more ME inputs high.

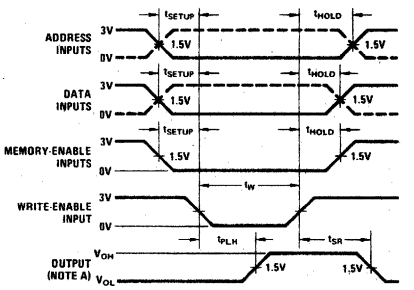
ac test circuit



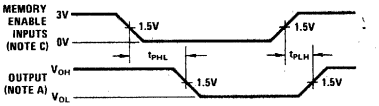
C_L includes probe and jig capacitance.

switching time waveforms

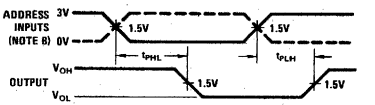
Write-Cycle



Access (Enable) Time and Disable Time from Memory Enable



Access Time from Address Inputs



Note A: Waveform shown is for the output with internal conditions such that the output is low except when disabled.
Note B: When measuring delay times from address inputs, the memory-enable inputs are low and the write-enable input is high.
Note C: When measuring delay times from memory-enable inputs, the address inputs are steady-state and the write-enable input is high.
Note D: Input waveforms are supplied by pulse generators having the following characteristics: $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns, PRR ≤ 1 MHz, and $Z_{OUT} \approx 50\Omega$.

NATIONAL

Bipolar RAMs

DM54S289/DM74S289 64-bit random access memories with open-collector outputs

general description

These 64-bit active-element memories are monolithic Schottky-clamped transistor-transistor logic (TTL) arrays organized as 16 words of four-bits each. They are fully decoded and feature a chip-enable input to simplify decoding required to achieve the desired system organization. The memories feature PNP input transistors that reduce the low level input current requirement to a maximum of −0.25 mA, only one-eighth that of a DM54S/DM74S standard load factor. The chip-enable circuitry is implemented with minimal delay times to compensate for added system decoding.

Write Cycle: The complement of the information at the data input is written into the selected location when both the chip-enable input and the read/write input are low. While the read/write input is low, the outputs are in the high-logic level ("OFF").

Read Cycle: The stored information (complement of information applied at the data inputs during the write cycle) is available at the outputs when the read/write input is high and the chip-enable is low. When the chip-enable input is high, the outputs are high ("OFF").

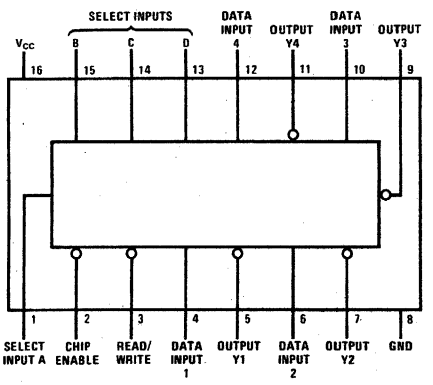
The fast access time of the DM54S289 makes it particularly attractive for implementing high-performance memory functions requiring access times on the order of 25 ns. The unique functional capability of the DM54S289 outputs being at a high during writing combined with the data inputs being inhibited during reading means that both data inputs and outputs can be connected to the data lines of a bus-organized system without the need for interface circuits.

features

- Schottky-clamped for high-speed applications:
  Access from chip-enable 12 ns typ
  Access from address inputs 25 ns typ
- Open collector outputs for controlled-impedance bus lines
- DM54S189/DM74S189 are functionally equivalent, but have TRI-STATE® outputs
- DM54S289 is guaranteed for operation over the full military temperature range of −55°C to +125°C
- Compatible with most TTL and DTL logic circuits
- Chip-enable input simplifies system decoding
- Compatible with Intel 3101A in most applications

connection diagram

Dual-In-Line Package



TOP VIEW

Order Number DM54S289J or DM74S289J
See Package 10

Order Number DM74S289N
See Package 15

truth table

FUNCTION	INPUTS		OUTPUT
	CHIP ENABLE	READ/ WRITE	
Write (Store Complement of Data)	L	L	H
Read	L	H	Stored Data
Inhibit	H	X	H

H = High Level
L = Low Level
X = Don't Care

absolute maximum ratings

Supply Voltage, V_{CC}	7.0V
Input Voltage	5.5V
Output Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DM54S289	4.5	5.5	V
DM74S289	4.75	5.25	V
Temperature (T_A)			
DM54S289	−55	+125	°C
DM74S289	0	+70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (Notes 2 and 3)

PARAMETER		CONDITIONS			MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage				2			V
V_{IL}	Low Level Input Voltage						0.8	V
I_{OH}	High Level Output Current	V_{CC} = Min	V_{OH} = 2.4V				40	μA
			V_{OH} = 5.5V				100	
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA		DM54S289			0.5	V
				DM74S289			0.45	
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7					25	μA
I_I	High Level Input Current at Maximum Voltage	V_{CC} = Max, V_I = 5.5V					1.0	mA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.45V					−250	μA
I_{CC}	Supply Current	V_{CC} = Max (Note 4)				75	105	mA
V_{IC}	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA					−1.2	V

switching characteristics over recommended operating ranges of T_A and V_{CC} (unless otherwise noted)

PARAMETER			CONDITIONS	DM54S289			DM74S289			UNITS
				MIN	TYP(1)	MAX	MIN	TYP(1)	MAX	
t_{AA}		Access Times From Address	C_L = 30 pF, R_{L1} = 300Ω, R_{L2} = 600Ω, *(Figure 1)*		25	50		25	35	ns
t_{CHL}	Enable Time From Chip Enable				12	25		12	17	ns
t_{WHL}	Enable Time From Read/Write	Sense Recovery Time From Read/Write			22	40		22	35	ns
t_{CLH}	Disable Time From Chip Enable				12	25		12	17	ns
t_{WP}	Width of Write Enable Pulse (Read/Write Low)			25			25			ns
t_{ASW}	Set-Up Time *(Figure 1)*	Address to Read/Write		0			0			ns
t_{DSW}		Data to Read/Write		25			25			
t_{CSW}		Chip-Enable to Read/Write		0			0			
t_{AHW}	Hold Time *(Figure 1)*	Address From Read/Write		0			0			ns
t_{DHW}		Data From Read/Write		0			0			
t_{CHW}		Chip-Enable From Read/Write		0			0			

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DM54S289 and across the 0°C to +70°C range for the DM74S289. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: I_{CC} is measured with all inputs grounded, and the outputs open.

switching time waveforms

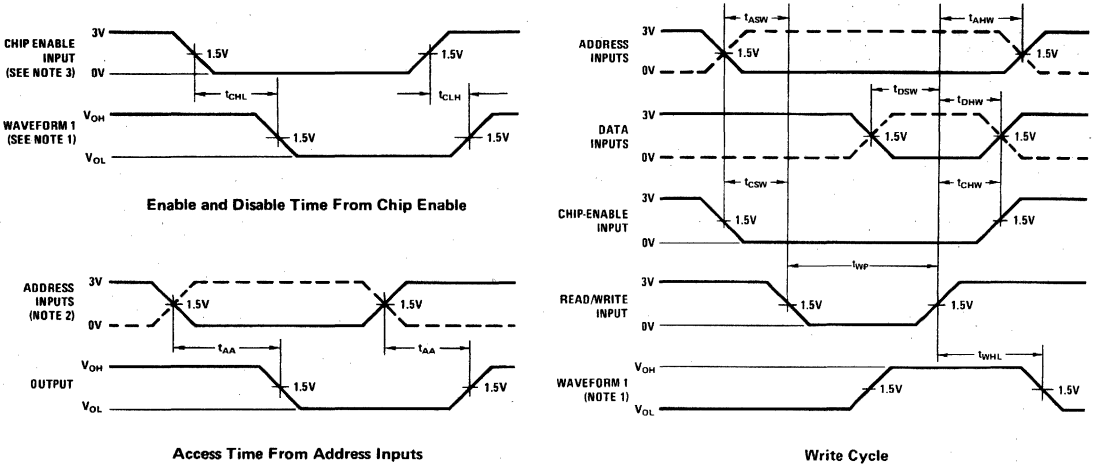


FIGURE 1

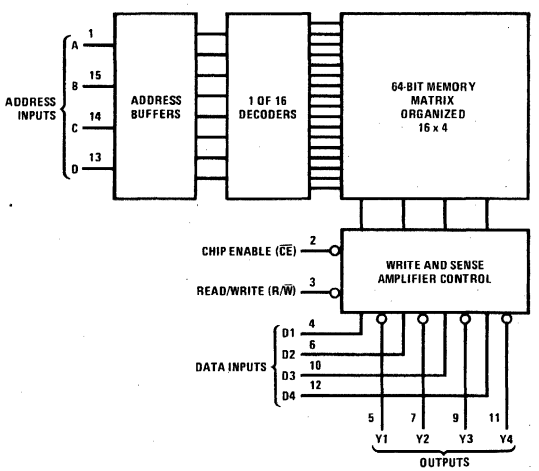
Note 1: Waveform 1 is for the output with internal conditions such that the output is low except when disabled.

Note 2: When measuring delay times from address inputs, the chip enable input is low and the read/write input is high.

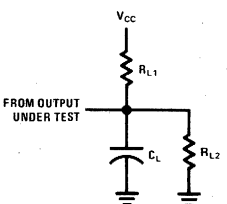
Note 3: When measuring delay times from chip enable input, the address inputs are steady state and the read/write input is high.

Note 4: Input waveforms are supplied by pulse generators having the following characteristics: $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns, PRR ≤ 1 MHz and $Z_{OUT} \approx 50\Omega$.

block diagram



ac test circuit



DM75S68/DM85S68 64-bit (16×4) edge triggered register

general description

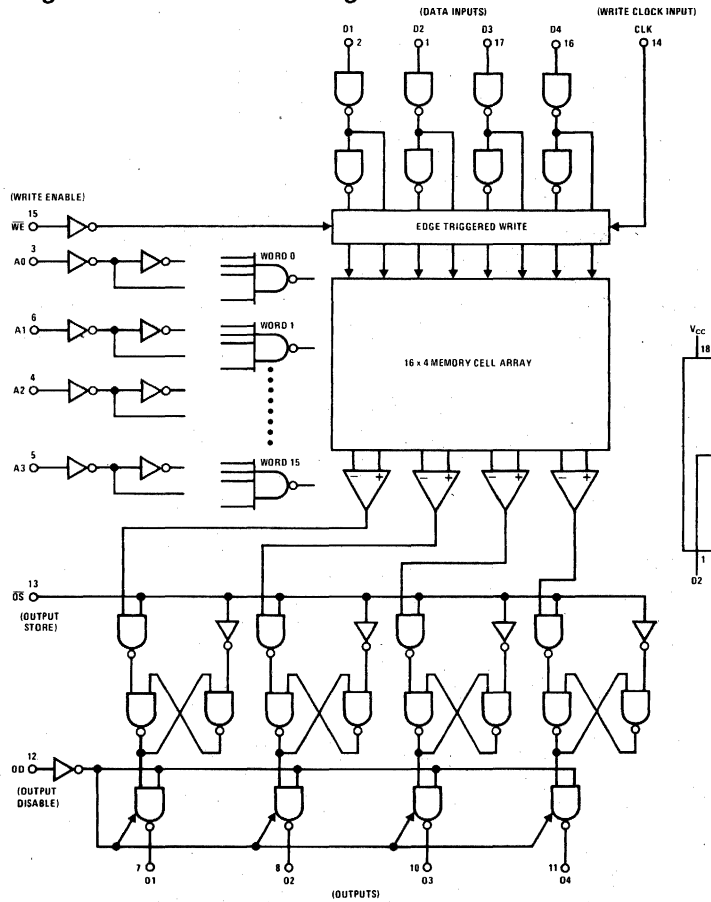
The DM75S68/DM85S68 is an addressable "D" register file. Any of its 16 four-bit words may be asynchronously read or may be written into on the next clock transition. An input terminal is provided to enable or disable the synchronous writing of the input data into the location specified by the address terminals. An output disable terminal operates only as a TRI-STATE® output control terminal. The addressable register data may be latched at the outputs and retained as long as the output store terminal is held in a low state. This memory storage condition is independent of the state of the output disable terminal.

All input terminals are high impedance at all times, and all outputs have low impedance active drive logic states and the high impedance TRI-STATE condition.

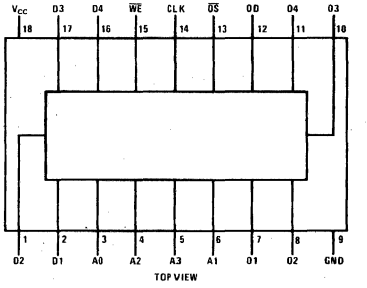
features

- On chip output register
- Edge triggered write
- High speed 30 ns typ
- TRI-STATE output
- Optimized for register stack applications
- Typical power dissipation 350 mW
- 18-pin package

logic and connection diagrams



Dual-In-Line Package



Order Number DM75S68D or DM85S68D
See Package 4

Order Number DM85S68N
See Package 16

absolute maximum ratings (Note 1)

Supply Voltage	7.0V
Input Voltage	5.5V
Output Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage, V_{CC}			
DM85S68	4.75	5.25	V
DM75S68	4.5	5.5	V
Temperature, T_A			
DM85S68	0	70	°C
DM75S68	−55	+125	°C

electrical characteristics

over recommended operating free-air temperature range (unless otherwise noted) (Notes 2 and 3)

PARAMETER		CONDITIONS		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
V_{IH}	High Level Input Voltage			2			V
V_{IL}	Low Level Input Voltage					0.8	V
V_{OH}	High Level Output Voltage	V_{CC} = Min	I_{OH} = −2.0 mA, DM75S68 I_{OH} = −5.2 mA, DM85S68	2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA	DM75S68			0.5	V
			DM85S68			0.45	
I_{IH}	High Level Input Current	V_{CC} = Max, V_{IH} = 2.4V	Clock Input			50	μA
			All Others			25	
I_I	High Level Input Current at Maximum Voltage	V_{CC} = Max, V_{IH} = 5.5V				1.0	mA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_{IL} = 0.5V	Clock Input			−500	μA
			All Others			−250	μA
I_{OS}	Short Circuit Output Current(4)	V_{CC} = Max, V_{OL} = 0V		−20		−55	mA
I_{CC}	Supply Current	V_{CC} = Max			70	100	mA
V_{IC}	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −18 mA				−1.2	V
I_{OZ}	TRI-STATE Output Current	V_{CC} = Max	V_O = 2.4V			+40	μA
			V_O = 0.5V			−40	

switching characteristics over recommended operating range of T_A and V_{CC} (unless otherwise noted)

PARAMETER			DM75S68 MIN	DM75S68 TYP	DM75S68 MAX	DM85S68 MIN	DM85S68 TYP	DM85S68 MAX	UNITS
t_{ZH}	Output Enable to High Level			20	40		20	35	ns
t_{ZL}	Output Enable to Low Level			14	30		14	24	ns
t_{HZ}	Output Disable Time From High Level			10	18		10	15	ns
t_{LZ}	Output Disable Time From Low Level			12	22		12	18	ns
t_{AA}	Access Time	Address to Output		30	55		30	40	
t_{OSA}		Output Store to Output		20	35		20	30	ns
t_{CA}		Clock to Output		25	50		25	40	
t_{ASC}	Set-Up Time	Address to Clock	25	5		15	5		ns
t_{DSC}		Data to Clock	15	5		5	0		
t_{ASOS}		Address to Output Store	40	15		30	15		
t_{WESC}		Write Enable Set-Up Time	10	5		5	0		
t_{OSSC}		Store Before Write	15	0		10	0		
t_{AHC}	Hold Time	Address From Clock	15	5		10	5		ns
t_{DHC}		Data From Clock	20	5		15	5		
t_{AHOS}		Address From Output Store	10	0		5	0		
t_{WEHC}		Write Enable Hold Time	20	5		15	5		

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DM75S68 and across the 0°C to +70°C range for the DM85S68. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Only one output at a time should be shorted.

typical applications

The DM85S68 can enhance the dynamic performance of a TTL processor, since it may safely operate using single phase clocking instead of the multiphase clocking systems being used currently. This simple feature not only enhances the system's dynamic performance, since multiple levels of registers need not be activated, but also reduces component count by elimination of one set of buffer registers. For example, note the simplicity of register file/ALU loop shown in *Figure 1*.

In a four-bit slice with zero delay within the arithmetic-logic unit, a level-triggered memory with buffering to prevent logic oscillation requires about 80 ns to make the loop whereas the DM75S68 does it in 35 ns. With a 30 ns delay in the ALU, the two compared system speeds are 110 ns and 65 ns, respectively.

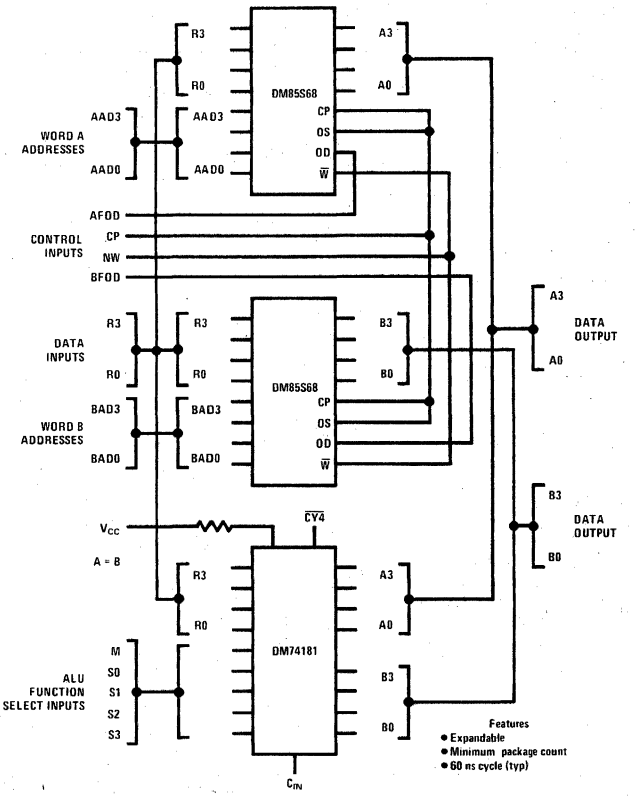
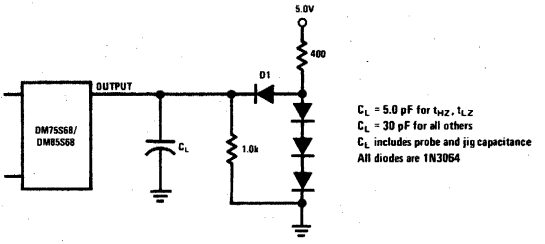


FIGURE 1. 4-Bit Register ALU

truth table

O_D	$\overline{W_E}$	CLK	$\overline{O_S}$	MODE	OUTPUTS
0	X	X	0	Output Store	Data From Last Addressed Location
X	0	⎍	X	Write Data	Dependent on State of OD and $\overline{OS}$
0	X	X	1	Read Data	Data Stored in Addressed Location
1	X	X	0	Output Store	High Impedance State
1	X	X	1	Output Disable	High Impedance State

ac test circuit and switching time waveforms



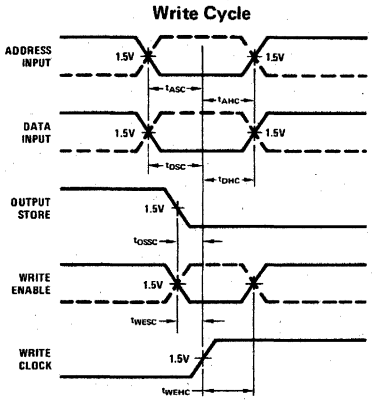


FIGURE 2. Clock Set-Up and Hold Time

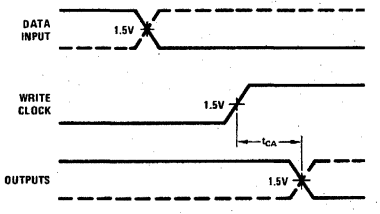


FIGURE 3. Clock to Output Access

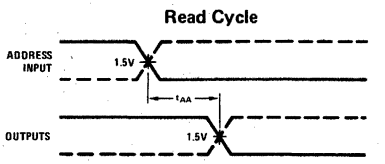


FIGURE 4. Address to Output Access Time

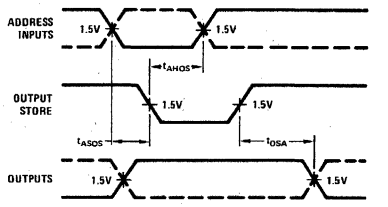


FIGURE 5. Output Store Access, Set-Up and Hold Time

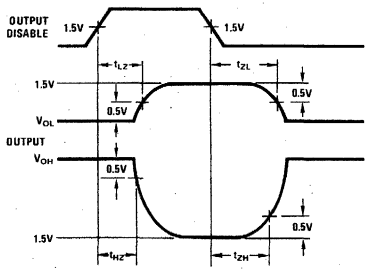


FIGURE 6. Output Disable and Enable Time

Note: Input waveforms supplied by pulse generator having the following characteristics: V = 3.0V, $t_R \leq 2.5$ ns, PRR $\leq$ 1.0 MHz and Z_{OUT} = 50M

NATIONAL

DM7599/DM8599 TRI-STATE™
64-bit random-access read/write memory

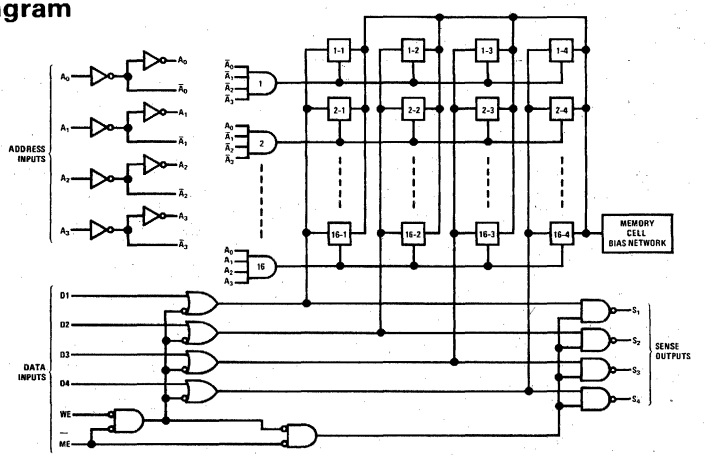
general description

The DM7599/DM8599 is a fully decoded 64-bit RAM organized as 16 4-bit words. The memory is addressed by applying a binary number to the four Address inputs. After addressing, information may be either written into or read from the memory. To write, both the Memory Enable and the Write Enable inputs must be in the logical "0" state. Information applied to the four Write inputs will then be written into the addressed location. To read information from the memory the Memory Enable input must be in the logical "0" state and the Write Enable input in the logical "1" state. Information will be read as the complement of what was written into the memory. When the Memory Enable input is in the logical "1" state, the outputs will go to the high-impedance state. This allows up to 128 memories to be connected to a common bus-line without the use of pull-up resistors. All memories except one are gated into the high-impedance while the one selected memory exhibits the normally totem-pole low impedance output characteristics of TTL.

features

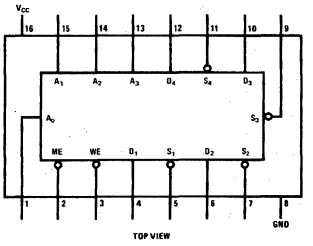
- Series 54/74 compatible
- Same pin-out as SN5489/SN7489
- Organized as 16 4-bit words
- Expandable to 2048 4-bit words without additional resistors (DM8599 only)
- Typical access from chip enable 20 ns
- Typical access time 28 ns
- Typical power dissipation 400 mW

block diagram



connection diagram

Dual-In-Line Package



Order Number DM7599J or DM8599J
See Package 10

Order Number DM8599N
See Package 15

truth table

MEMORY ENABLE	WRITE ENABLE	OPERATION	OUTPUTS
0	0	Write	Hi-Z State
0	1	Read	Complement of Data Stored in Memory
1	X	Hold	Hi-Z State

absolute maximum ratings (Note 1)

Supply Voltage	7V	Storage Temperature Range	−65°C to +150°C
Input Voltage	5.5V	Operating Temperature Range	
Output Voltage	5.5V	DM7599	−55°C to +125°C
Time that two bus-connected devices may be in opposite low impedance states simultaneously	Indefinite	DM8599	0°C to +70°C
		Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics (Note 2)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	DM7599	V_{CC} = 4.5V		2.0			V
	DM8599	V_{CC} = 4.75V					
Logical "0" Input Voltage	DM7599	V_{CC} = 4.5V				0.8	V
	DM8599	V_{CC} = 4.75V					
Logical "1" Output Voltage	DM7599	V_{CC} = 4.5V	I_O = −2 mA	2.4			V
	DM8599	V_{CC} = 4.75V	I_O = −5.2 mA	2.4			V
Logical "0" Output Voltage	DM7599	V_{CC} = 4.5V	I_O = 12 mA			0.4	V
	DM8599	V_{CC} = 4.75V					
Third State Output Current	DM7599	V_{CC} = 5.5V	V_O = 0.4V			±40	μA
	DM8599	V_{CC} = 5.25V	V_O = 2.4V			±40	
Logical "1" Input Current	DM7599	V_{CC} = 5.5V	V_{IN} = 2.4V			40	μA
	DM8599	V_{CC} = 5.25V					
	DM7599	V_{CC} = 5.5V	V_{IN} = 5.5V			1	mA
	DM8599	V_{CC} = 5.25V					
Logical "0" Input Current	DM7599	V_{CC} = 5.5V	V_{IN} = 0.4V			−1.6	mA
	DM8599	V_{CC} = 5.25V					
Output Short Circuit Current (Note 3)	DM7599	V_{CC} = 5.5V		−30		−70	mA
	DM8599	V_{CC} = 5.25V					
Supply Current	DM7599	V_{CC} = 5.5V	All Inputs at GND		80	120	mA
	DM8599	V_{CC} = 5.25V					
Input Clamp Voltage	DM7599	V_{CC} = 4.5V	I_{IN} = −12 mA			−1.5	V
	DM8599	V_{CC} = 4.75V					

switching characteristics (Over recommended operating ranges of V_{CC} and T_A)

PARAMETER			CONDITIONS	DM7599			DM8599			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Access Time From Address		R_{L1} = 400Ω, R_{L2} = 1.0 kΩ, C_L = 50 pF		27	70		27	50	ns
t_{PHL}					28	70		28	50	ns
t_{ZH}	Enable Time From Memory Enable				16	45		16	30	ns
t_{ZL}					20	40		20	35	ns
t_{ZH}	Sense Recovery Time From Write Enable				20	40		20	35	ns
t_{ZL}					35	65		35	55	ns
t_{HZ}	Disable Time From Memory Enable		R_{L1} = 400Ω, R_{L2} = 1.0k, C_L = 5.0 pF		10	30		10	25	ns
t_{LZ}					14	35		14	30	ns
t_{SETUP}	Setup Time	Address to Write Enable		0	−14		0	−14		ns
		Data to Write Enable		0	−15		0	−15		ns
		Memory Enable to Write Enable		0	−10		0	−10		ns
t_{HOLD}	Hold Time	Address From Write Enable		5	−7		5	−7		ns
		Data From Write Enable		0	−14		0	−14		ns
		Memory Enable From Write Enable		0	−10		0	−10		ns
t_{WP}	Write Pulse Width			50	20		40	20		ns

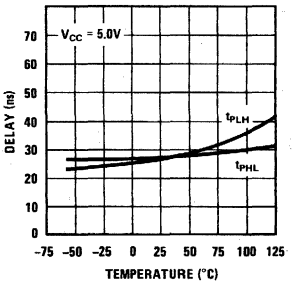
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DM7599 and across the 0°C to 70°C range for the DM8599. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

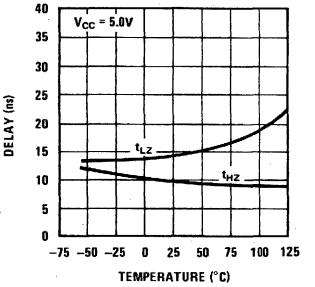
Note 3: Only one output at a time should be shorted.

typical performance curves

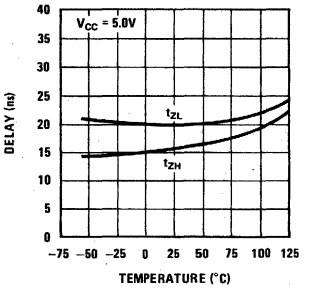
Delay from Address to Output



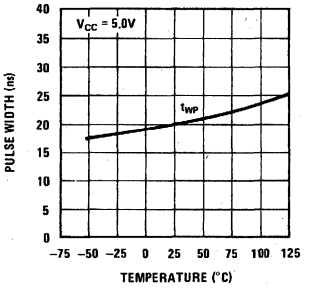
Delay from Memory Enable to High Impedance State



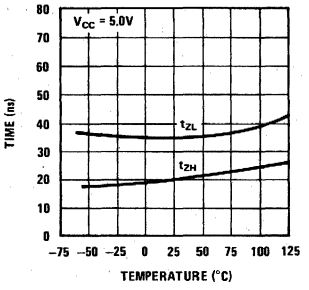
Delay from Memory Enable to Low Impedance State



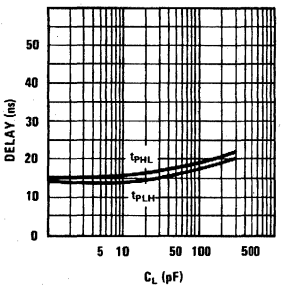
Minimum Write Pulse Width



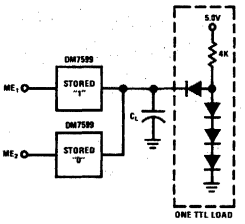
Sense Recovery Time



Delay from Enable to Output vs Load Capacitance



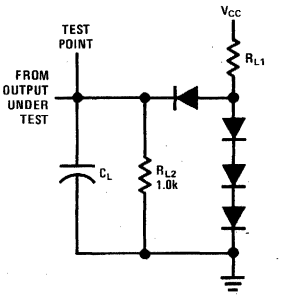
test circuit



Test Circuit for Delay vs Load Capacitance

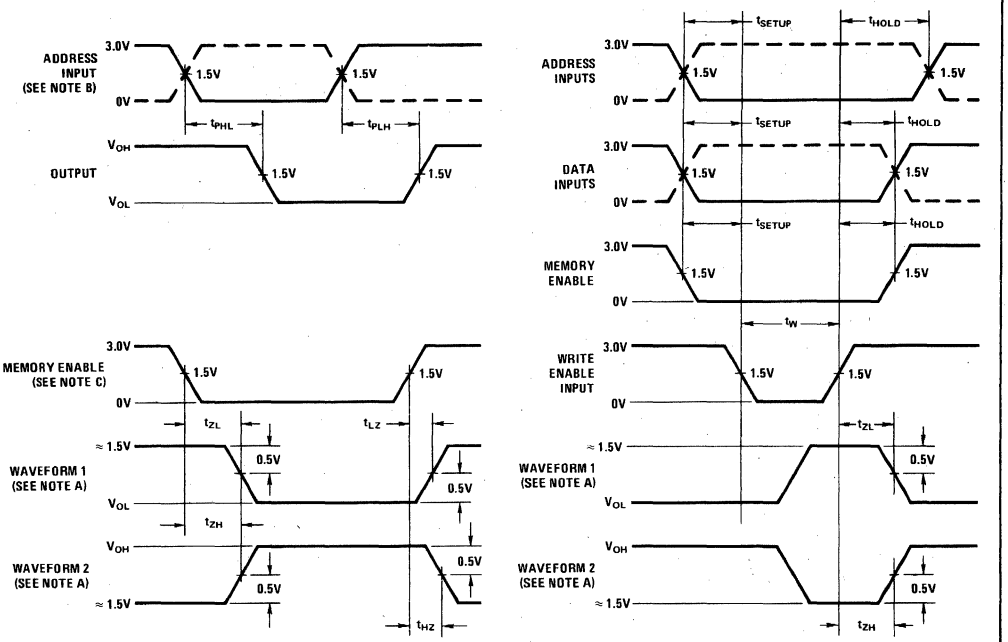
Note: In a typical application the output of the TRI-STATE memories might be wired together and one would be switching to the low impedance state at the same time the circuit previously selected would be switching back into the high impedance state. The measurements of delay versus load capacitance were made under conditions which simulate actual operating conditions in an application. (See test circuit.)

ac test circuit



C_L includes probe and jig capacitance.
All diodes are 1N3064.

switching time waveforms



Note A: Waveform 1 is for the output with internal conditions such that the output is low except when disabled. Waveform 2 is for the output with internal conditions such that the output is high except when disabled.

Note B: When measuring delay times from address inputs, the memory enable input is low and the write enable input is high.

Note C: When measuring delay times from memory enable input, the address inputs are steady-state and the write enable input is high.

Note D: Input waveforms are supplied by pulse generators having the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, PRR ≤ 1.0 MHz, and $Z_{OUT} \approx 50\Omega$.

Bipolar RAMs

DM86S21 64-bit bipolar high speed RAM (32 × 2 RAM)

general description

The DM86S21 is a TTL 64-bit Write-While-Read Random Access Memory organized in 32 words of 2 bits each. The DM86S21 is ideally suited for high speed buffers and as the memory element in high speed accumulators.

Words are selected through a 5 input decoder when the Read-Write enable input, CE is at logic "1." $\overline{W_0}$ and $\overline{W_1}$ are the write inputs for bit 0 and bit 1 of the word selected. $\overline{C}$ is the write control input. When $\overline{W_X}$ and $\overline{C}$ are both at logic "0" data on the I_0 and I_1 data lines are written into the addressed word. The read function is enabled when either $\overline{W_X}$ or $\overline{C}$ is at logic "1."

An internal latch is on the chip to provide the Write-While-Read capability. When the latch control line, $\overline{L}$, is logic "1" and data is being read from the DM86S21, the latch is effectively bypassed. The data at the output will be that of the addressed word. When $\overline{L}$ goes from a logic "1" to logic "0" the outputs are latched and will remain latched regardless of the state of any other address or control line. When $\overline{L}$ goes from "0" to "1" the outputs unlatch and the outputs will be that of the present address word.

features

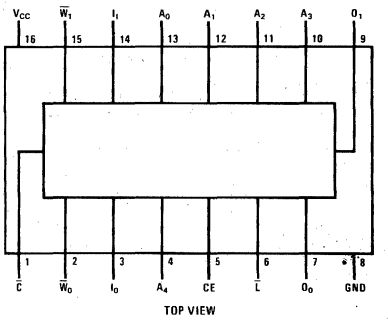
- Buffered address lines
- On chip latches
- On chip decoding
- Bit masking control lines
- Enable control line
- Open collector outputs with 40 mA capability
- Protected inputs
- Very high speeds 25 ns (typ)
- Second source to Signetics 82S21

applications

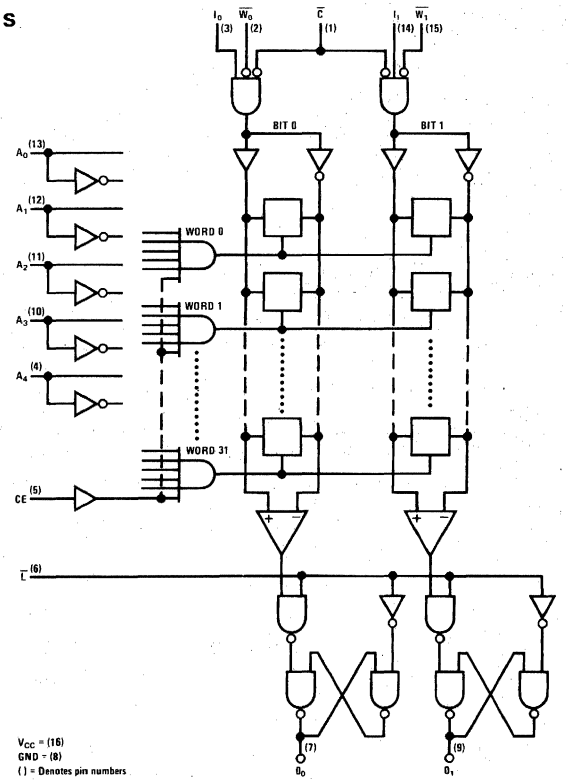
- Scratch pad memory
- Buffer memory
- Accumulator register
- Control store

logic and connection diagrams

Dual-In-Line Package



Order Number DM86S21J
See Package 10
Order Number DM86S21N
See Package 15



absolute maximum ratings (Note 1)

Supply Voltage	7.0V
Input Voltage	5.5V
Output Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage, V_{CC}	4.75	5.25	V
Temperature, T_A	0	+70	°C

electrical characteristics (Notes 2 and 3)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Logical "1" Input Voltage (V_{IH})		2.0			V
Logical "1" Input Current (I_{IH})	V_{CC} = Max, V_{IN} = 5.5V			25	μA
Logical "0" Input Voltage (V_{IL})				0.85	V
Logical "0" Input Current (I_{IL})	V_{CC} = Max, V_{IN} = 0.45V			−1.6	mA
Input Clamp Voltage (V_{CD})	V_{CC} = Min, I_{IN} = −18 mA			−1.2	V
Logical "1" Output Current (I_{OH})	V_{CC} = Max, V_{OUT} = 5.5V			40	μA
Logical "0" Output Voltage (V_{OL})	V_{CC} = Min, I_{OUT} = 40 mA			0.45	V
Supply Current (I_{CC})	V_{CC} = Max			130	mA
Read Access Time Address to Output (t_1)			25	50	ns
Address Set-up Time (t_2)			8		ns
Data Set-up Time (t_3)		20	15		ns
Address Hold Time (t_4)		0			ns
Control or Write Pulse Width (t_5)		20	15		ns
Write Access Time (t_6)			20		ns
Address to Latch Set-up Time (t_7)			25	50	ns
Latch Address to Address Hold Time (t_8)		10	7		ns
Delatch Access Time (t_9)			15	25	ns
Data Hold Time Earliest (t_{10})		5	0		ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

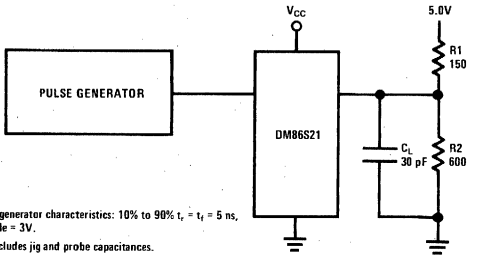
Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C range for the DM86S21. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

truth table

CE	$\overline{C}$	$\overline{W_0}$	$\overline{W_1}$	$\overline{L}$	MODE	OUTPUTS
X	X	X	X	0	Output Hold	Data from last addressed word when CE = "1"
0	X	X	X	1	Read & Write Disabled	Disabled logic "1"
1	1	X	X	X	Read	Data stored in addressed word
1	0	1	1	X	Read	Data stored in addressed word
1	0	0	0	0	Write Data	Data from last word address when L went from "1" to "0"
1	0	0	0	1	Write Data	Data being written into memory
1	0	0	1	X	Write Data into Bit 0 Only	If $\overline{L}$ = 0: Data from last word address when L went from "1" to "0"
1	0	1	0	X	Write Data into Bit 1 Only	If $\overline{L}$ = 1: Data being written into the selected bit location and stored in other addressed location

ac test circuit



Note 1: Pulse generator characteristics: 10% to 90% $t_r = t_f$ = 5 ns, pulse amplitude = 3V.

Note 2: C_L includes jig and probe capacitances.

switching time waveforms

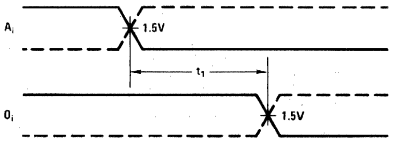


FIGURE 1. Read Access Time

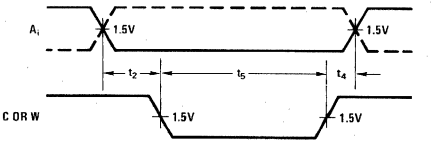


FIGURE 2. Address Set-up and Hold Time

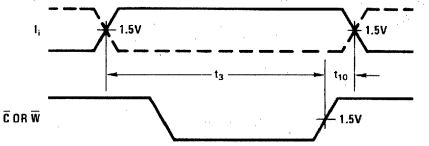


FIGURE 3. Data Set-up and Hold Time

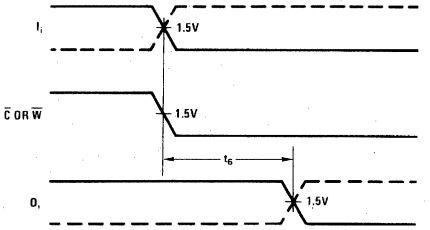


FIGURE 4. Write Access Time

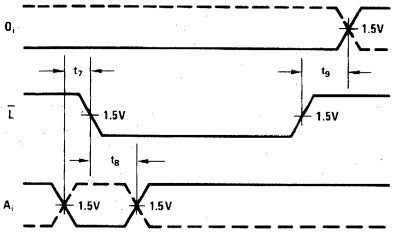


FIGURE 5. Latch Times

NATIONAL

Bipolar RAMs

DM86L99 TRI-STATE® low power 64-bit random access memory

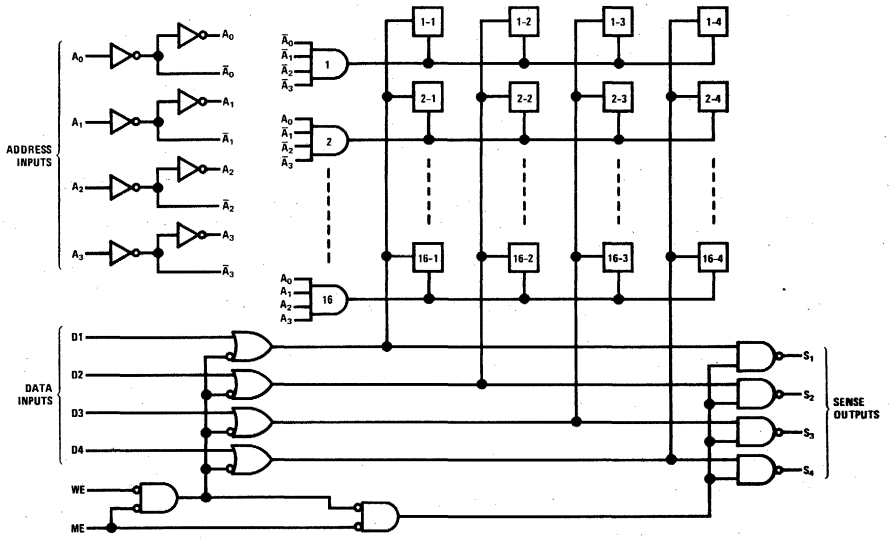
general description

The DM86L99 is a fully decoded 64-bit RAM organized as 16 4-bit words. The memory is addressed by applying a binary number to the four Address inputs. After addressing, information may be either written into or read from the memory. To write, both the Memory Enable and the Write Enable inputs must be in the logical "0" state. Information applied to the four Write inputs will then be written into the addressed location. To read information from the memory the Memory Enable input must be in the logical "0" state and the Write Enable input in the logical "1" state. Information will be read as the complement of what was written into the memory. When the Memory Enable input is in the logical "1" state, the outputs will go to the high-impedance state. This allows up to 75 memories to be connected to a common bus-line without the use of pull-up resistors. All memories except one are gated into the high-impedance while the one selected memory exhibits the normally totem-pole low impedance output characteristics of TTL.

features

- Series 54L/74L compatible
- Same pin-out as SN7489, 3101, MM5501
- Organized as 16 4-bit words
- Expandable to 1200 4-bit words without additional resistors
- Typical access from chip enable 50 ns
- Typical access time 80 ns
- Typical power dissipation 75 mW

logic diagram



absolute maximum ratings (Note 1)

Supply Voltage	7.0V
Input Voltage	5.5V
Output Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DM86L99	4.75	5.25	V
Temperature (T_A)			
DM86L99	0	+70	°C

electrical characteristics (Notes 2 and 3) V_{CC} = 5.0V, T_A = 25°C unless otherwise specified.

PARAMETER	CONDITIONS	LIMITS			UNITS
		MIN	TYP	MAX	
Logical "1" Input Voltage (V_{IH})	V_{CC} = Min	2.0			V
Logical "1" Input Current (I_{IH})	V_{CC} = Max, V_{IN} = 2.4V V_{CC} = Max, V_{IN} = 5.5V			10 100	μA μA
Logical "0" Input Voltage (V_{IL})	V_{CC} = Min			0.7	V
Logical "0" Input Current (I_{IL})	V_{CC} = Max, V_{IN} = 0.3V			−180	μA
Input Clamp Voltage (V_{CD})	V_{CC} = Min, I_{IN} = −12 mA			−1.5	V
Logical "1" Output Voltage (V_{OH})	V_{CC} = Min, I_{OUT} = −1.0 mA	2.4			V
Output Short Circuit Current (Note 4) (I_{OS})	V_{CC} = Max, V_{OUT} = 0V	−6.0		−30	mA
Logical "0" Output Voltage (V_{OL})	V_{CC} = Min, I_{OUT} = 3.2 mA			0.4	V
Supply Current (I_{CC})	V_{CC} = Max		15	19	mA
Third State Output Current	V_{CC} = Max, V_{OUT} = 2.4V V_{OUT} = 0.4V			±40	μA
Propagation Delay to a Logical "0" From Address to Output (t_{pd0})	V_{CC} = 5.0V, T_A = 25°C		77	150	ns
Propagation Delay to a Logical "1" From Address to Output (t_{pd1})	V_{CC} = 5.0V, T_A = 25°C		51	120	ns
Delay From Memory Enable to High Impedance State (From Logical "1" Level)(t_{1H})	V_{CC} = 5.0V, T_A = 25°C		18	27	ns
Delay From Memory Enable to High Impedance State (From Logical "0" Level)(t_{0H})	V_{CC} = 5.0V, T_A = 25°C		37	56	ns
Delay From Memory Enable to Logical "1" Level (From High Impedance State) (t_{H1})	V_{CC} = 5.0V, T_A = 25°C		50	30	ns
Delay From Memory Enable to Logical "0" Level (From High Impedance State)(t_{H0})	V_{CC} = 5.0V, T_A = 25°C		29	43	ns
Write Enable Pulse Width	V_{CC} = 5.0V, T_A = 25°C	50	30		ns
Setup Time, Data Input	V_{CC} = 5.0V, T_A = 25°C	0			ns
Hold Time, Data Input	V_{CC} = 5.0V, T_A = 25°C	0			ns
Setup Time, Address	V_{CC} = 5.0V, T_A = 25°C	0			ns
Hold Time, Address	V_{CC} = 5.0V, T_A = 25°C	0			ns
Setup Time, Memory Enable	V_{CC} = 5.0V, T_A = 25°C	0			ns
Hold Time, Memory Enable	V_{CC} = 5.0V, T_A = 25°C	0			ns
Sense Recovery Time From Write Enable (t_{SR})	V_{CC} = 5.0V, T_A = 25°C		110	165	ns
Disable Time From Write Enable ($t_{\overline{EN}}$)	V_{CC} = 5.0V, T_A = 25°C		73	110	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

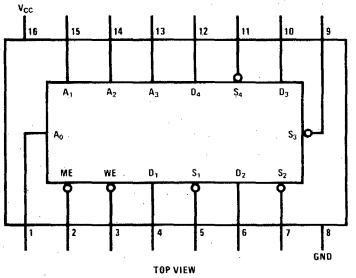
Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C range. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

Note 3: All currents into device pins shown as positive, out of device pins as negative. All voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Only one output at a time should be shorted.

connection diagram

Dual-In-Line Package



Order Number DM86L99J
See Package 10

Order Number DM86L99N
See Package 15

Order Number DM86L99W
See Package 28

truth table

MEMORY ENABLE	WRITE ENABLE	OPERATION	OUTPUTS
0	0	Write	Hi-Z State
0	1	Read	Complement of Data Stored in Memory
1	X	Hold	Hi-Z State

CMOS RAMs

MM54C89/MM74C89 64-bit TRI-STATE® random access read/write memory

general description

The MM54C89/MM74C89 is a 16-word by 4-bit random access read/write memory. Inputs to the memory consist of four address lines, four data input lines, a write enable line and a memory enable line. The four binary address inputs are decoded internally to select each of the 16 possible word locations. An internal address register, latches the address information on the positive to negative transition of the memory enable input. The four TRI-STATE® data output lines working in conjunction with the memory enable input provides for easy memory expansion.

Address Operation: Address inputs must be stable t_{SA} prior to the positive to negative transition of memory enable. It is thus not necessary to hold address information stable for more than t_{HA} after the memory is enabled (positive to negative transition of memory enable).

Note: The timing is different than the DM7489 in that a positive to negative transition of the memory enable must occur for the memory to be selected.

Write Operation: Information present at the data inputs is written into the memory at the selected address by bringing write enable and memory enable low.

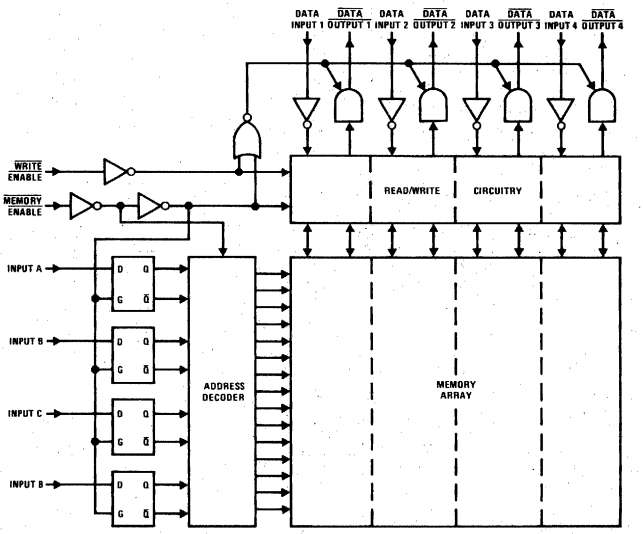
Read Operation: The complement of the information which was written into the memory is non-destructively read out at the four outputs. This is accomplished by selecting the desired address and bringing memory enable low and write enable high.

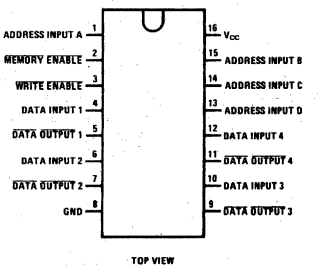
When the device is writing or disabled the output assumes a TRI-STATE (Hi-z) condition.

features

- Wide supply voltage range — 3.0V to 15V
- Guaranteed noise margin — 1.0V
- High noise immunity — 0.45 V_{CC} typ
- Low power TTL compatibility — fan out of 2 driving 74L
- Input address register
- Low power consumption — 100 nW/package typ @ V_{CC} = 5V
- Fast access time — 130 ns typ at V_{CC} = 10V
- TRI-STATE output

logic and connection diagrams





TOP VIEW

Order Number MM54C89D or MM74C89D
See Package 3
Order Number MM74C89N
See Package 15

absolute maximum ratings

Voltage at Any Pin	−0.3V to V_{CC} + 0.3V
Operating Temperature Range	
MM54C89	−55°C to +125°C
MM74C89	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500 mW
Operating V_{CC} Range	3.0V to 15V
Absolute Maximum V_{CC}	16V
Lead Temperature (Soldering, 10 seconds)	300°C

dc electrical characteristics

Min/max limits apply across temperature range, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CMOS TO CMOS					
Logical "1" Input Voltage ($V_{IN(1)}$)	V_{CC} = 5.0V	3.5			V
	V_{CC} = 10V	8.0			V
Logical "0" Input Voltage ($V_{IN(0)}$)	V_{CC} = 5.0V			1.5	V
	V_{CC} = 10V			2.0	V
Logical "1" Output Voltage ($V_{OUT(1)}$)	V_{CC} = 5.0V, I_O = −10μA	4.5			V
	V_{CC} = 10V, I_O = −10μA	9.0			V
Logical "0" Output Voltage ($V_{OUT(0)}$)	V_{CC} = 5.0V, I_O = +10μA			0.5	V
	V_{CC} = 10V, I_O = +10μA			1.0	V
Logical "1" Input Current ($I_{IN(1)}$)	V_{CC} = 15V, V_{IN} = 15V		0.005	1.0	μA
Logical "0" Input Current ($I_{IN(0)}$)	V_{CC} = 15V, V_{IN} = 0V	−1.0	−0.005		μA
Output Current in High Impedance State	V_{CC} = 15V, V_O = 15V		0.005	1.0	μA
	V_{CC} = 15V, V_O = 0V	−1.0	−0.005		μA
Supply Current (I_{CC})	V_{CC} = 15V		0.05	300	μA
CMOS/LPTTL INTERFACE					
Logical "1" Input Voltage ($V_{IN(1)}$)	54C, V_{CC} = 4.5V	V_{CC} − 1.5			V
	74C, V_{CC} = 4.75V	V_{CC} − 1.5			V
Logical "0" Input Voltage ($V_{IN(0)}$)	54C, V_{CC} = 4.5V			0.8	V
	74C, V_{CC} = 4.75V			0.8	V
Logical "1" Output Voltage ($V_{OUT(1)}$)	54C, V_{CC} = 4.5V, I_O = −360μA	2.4			V
	74C, V_{CC} = 4.75V, I_O = −360μA	2.4			V
Logical "0" Output Voltage ($V_{OUT(0)}$)	54C, V_{CC} = 4.5V, I_O = +360μA			0.4	V
	74C, V_{CC} = 4.75V, I_O = +360μA			0.4	V
OUTPUT DRIVE (See 54C/74C Family Characteristics Data Sheet)					
Output Source Current (I_{SOURCE}) (P-Channel)	V_{CC} = 5.0V, V_{OUT} = 0V, T_A = 25°C	−1.75	−3.3		mA
Output Source Current (I_{SOURCE}) (P-Channel)	V_{CC} = 10V, V_{OUT} = 0V, T_A = 25°C	−8.0	−15		mA
Output Sink Current (I_{SINK}) (N-Channel)	V_{CC} = 5.0V, V_{OUT} = V_{CC}, T_A = 25°C	1.75	3.6		mA
Output Sink Current (I_{SINK}) (N-Channel)	V_{CC} = 10V, V_{OUT} = V_{CC}, T_A = 25°C	8.0	16		mA

ac electrical characteristics (T_A = 25°C, C_L = 50 pF, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Propagation Delay from $\overline{\text{Memory Enable}}$ (t_{pd})	V_{CC} = 5.0V		270	500	ns
	V_{CC} = 10V		100	220	ns
Access Time from Address Input (t_{acc})	V_{CC} = 5.0V		350	650	ns
	V_{CC} = 10V		130	280	ns
Address Input Setup Time (t_{SA})	V_{CC} = 5.0V	150			ns
	V_{CC} = 10V	60			ns
Address Input Hold Time (t_{HA})	V_{CC} = 5.0V	60			ns
	V_{CC} = 10V	40			ns
$\overline{\text{Memory Enable}}$ Pulse Width (t_{ME})	V_{CC} = 5.0V	400	250		ns
	V_{CC} = 10V	150	90		ns
$\overline{\text{Memory Enable}}$ Pulse Width ($t_{\overline{ME}}$)	V_{CC} = 5.0V	400	200		ns
	V_{CC} = 10V	150	70		ns

ac electrical characteristics (con't)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{\text{Write}}$ $\overline{\text{Enable}}$ Setup Time for a Read (t_{SR})	V_{CC} = 5.0V V_{CC} = 10V	0 0			ns ns
$\overline{\text{Write}}$ $\overline{\text{Enable}}$ Setup Time for a Write (t_{WS})	V_{CC} = 5.0V V_{CC} = 10V			t_{ME} t_{ME}	ns ns
$\overline{\text{Write}}$ $\overline{\text{Enable}}$ Pulse Width ($t_{\overline{WE}}$)	V_{CC} = 5.0V, t_{WS} = 0 V_{CC} = 10V, t_{WS} = 0	300 100	160 60		ns ns
Data Input Hold Time (t_{HD})	V_{CC} = 5.0V V_{CC} = 10V	50 25			ns ns
Data Input Setup (t_{SD})	V_{CC} = 5.0V V_{CC} = 10V	50 25			ns ns
Propagation Delay from a Logical "1" or Logical "0" to the High Impedance State from $\overline{\text{Memory}}$ $\overline{\text{Enable}}$ (t_{1H}, t_{0H})	V_{CC} = 5.0V, C_L = 5.0 pF, R_L = 10k V_{CC} = 10V, C_L = 5.0 pF, R_L = 10k		180 85	300 120	ns ns
Propagation Delay from a Logical "1" or Logical "0" to the High Impedance State from $\overline{\text{Write}}$ $\overline{\text{Enable}}$ (t_{1H}, t_{0H})	V_{CC} = 5.0V, C_L = 5.0 pF, R_L = 10k V_{CC} = 10V, C_L = 5.0 pF, R_L = 10k		180 85	300 120	ns ns
Input Capacity (C_{IN})	Any Input (Note 2)		5.0		pF
Output Capacity (C_{OUT})	Any Output (Note 2)		6.5		pF
Power Dissipation Capacity (C_{pd})	(Note 3)		230		pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

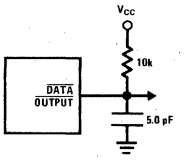
Note 3: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note, AN-90.

truth table

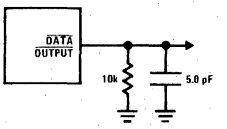
ME	WE	OPERATION	CONDITION OF OUTPUTS
L	L	Write	TRI-STATE
L	H	Read	Complement of Selected Word
H	L	Inhibit, Storage	TRI-STATE
H	H	Inhibit, Storage	TRI-STATE

ac test circuits

t_{0H}

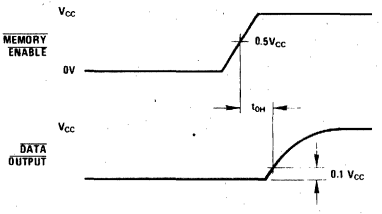


t_{1H}

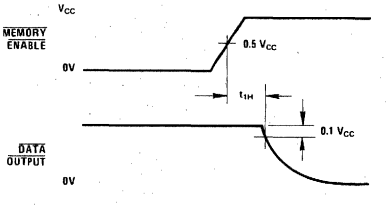


switching time waveforms

t_{0H}

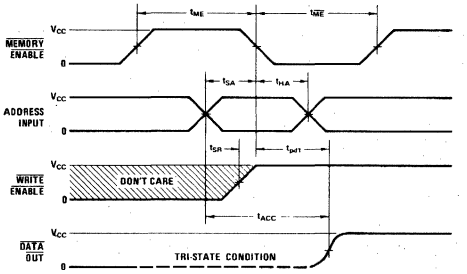


t_{1H}

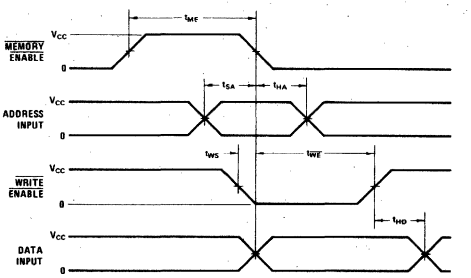


switching time waveforms (con't)

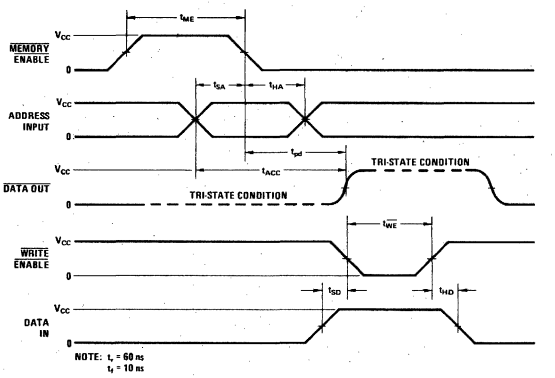
Read Cycle



Write Cycle



Read Modify Write Cycle



CMOS RAMs

MM54C200/MM74C200 256-bit TRI-STATE® random access read/write memory

general description

The MM54C200/MM74C200 is a 256-bit random access read/write memory. Inputs consist of eight address lines, a data input line, a write enable line, and three chip enables. The eight binary address inputs are decoded internally to select each of the 256 locations. An internal address register, latches and address information on the positive to negative edge of $\overline{CE}_3$. The TRI-STATE data output line working in conjunction with $\overline{CE}_1$ or $\overline{CE}_2$ inputs provides for easy memory expansion.

Address Operation: Address inputs must be stable t_{SA} prior to the positive to negative transition of $\overline{CE}_3$. It is thus not necessary to hold address information stable for more than t_{HA} after the memory is enabled (positive to negative transition).

Note: The timing is different than the DM74200 in that a positive to negative transition of the memory enable must occur for the memory to be selected.

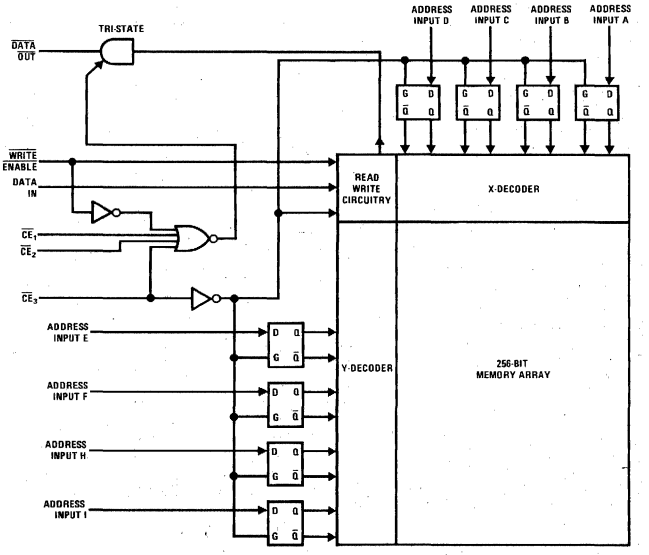
Read Operation: The data is read out by selecting the proper address and bringing $\overline{CE}_3$ low and write enable high. Holding $\overline{CE}_1$ or $\overline{CE}_2$ or $\overline{CE}_3$ at a high level forces the output into TRI-STATE. When used in bus organized systems, $\overline{CE}_1$, or $\overline{CE}_2$, a TRI-STATE control, provides for fast access times by not totally disabling the chip.

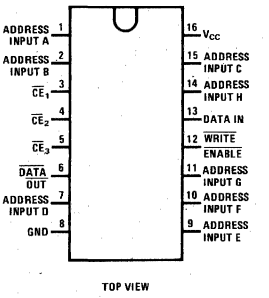
Write Operation: Data is written into the memory with $\overline{CE}_3$ low and write enable low. The state of $\overline{CE}_1$ or $\overline{CE}_2$ has no effect on the write cycle. The output assumes TRI-STATE with write enable low.

features

■ Wide supply voltage range	3.0V to 15V
■ Guaranteed noise margin	1.0V
■ High noise immunity	0.45 V_{CC} typ
■ TTL compatibility	fan out of 1 driving standard TTL
■ Low power	500 nW typ
■ Internal address register	

logic and connection diagrams





TOP VIEW

Order Number MM54C200D or MM74C200D
See Package 3
Order Number MM74C200N
See Package 15

absolute maximum ratings (Note 1)

Voltage at Any Pin	−0.3V to V_{CC} +0.3V
Operating Temperature Range	
MM54C200	−55°C to +125°C
MM74C200	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500 mW
Operating V_{CC} Range	3.0V to 15V
Absolute Maximum V_{CC}	16V
Lead Temperature (Soldering, 10 seconds)	300°C

dc electrical characteristics

Min/max limits apply across temperature range, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CMOS TO CMOS					
Logical "1" Input Voltage ($V_{IN(1)}$)	V_{CC} = 5.0V	3.5			V
	V_{CC} = 10V	8.0			V
Logical "0" Input Voltage ($V_{IN(0)}$)	V_{CC} = 5.0V			1.5	V
	V_{CC} = 10V			2.0	V
Logical "1" Output Voltage ($V_{OUT(1)}$)	V_{CC} = 5.0V, I_O = −10μA	4.5			V
	V_{CC} = 10V, I_O = −10μA	9.0			V
Logical "0" Output Voltage ($V_{OUT(0)}$)	V_{CC} = 5.0V, I_O = +10μA			0.5	V
	V_{CC} = 10V, I_O = +10μA			1.0	V
Logical "1" Input Current ($I_{IN(1)}$)	V_{CC} = 15V, V_{IN} = 15V		0.005	1.0	μA
Logical "0" Input Current ($I_{IN(0)}$)	V_{CC} = 15V V_{IN} = 0V	-1.0	-0.005		μA
Supply Current (I_{CC})	V_{CC} = 15V		0.10		μA
CMOS/LPTTL INTERFACE					
Logical "1" Input Voltage ($V_{IN(1)}$)	54C, V_{CC} = 4.5V	V_{CC} - 1.5			V
	74C, V_{CC} = 4.75V	V_{CC} - 1.5			V
Logical "0" Input Voltage ($V_{IN(0)}$)	54C, V_{CC} = 4.5V			0.8	V
	74C, V_{CC} = 4.75V			0.8	V
Logical "1" Output Voltage ($V_{OUT(1)}$)	54C, V_{CC} = 4.5V, I_O = −1.6 mA	2.4			V
	74C, V_{CC} = 4.75V, I_O = −1.6 mA	2.4			V
Logical "0" Output Voltage ($V_{OUT(0)}$)	54C, V_{CC} = 4.5V, I_O = 1.6 mA			0.4	V
	74C, V_{CC} = 4.75V, I_O = 1.6 mA			0.4	V
OUTPUT DRIVE (See 54C/74C Family Characteristics Data Sheet)					
Output Source Current (I_{SOURCE}) (P-Channel)	V_{CC} = 5.0V, V_{OUT} = 0V T_A = 25°C	-4.0	-6.0		mA
Output Source Current (I_{SOURCE}) (P-Channel)	V_{CC} = 10V, V_{OUT} = 0V T_A = 25°C	-16.0	-25		mA
Output Sink Current (I_{SINK}) (N-Channel)	V_{CC} = 5.0V, V_{OUT} = V_{CC} T_A = 25°C	5.0	8.0		mA
Output Sink Current (I_{SINK}) (N-Channel)	V_{CC} = 10V, V_{OUT} = V_{CC} T_A = 25°C	20.0	30		mA

ac electrical characteristics T_A = 25°C, C_L = 50 pF, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Access Time From Address (t_{ACC})	V_{CC} = 5.0V		450	900	ns
	V_{CC} = 10V		200	400	ns
Propagation Delay From $\overline{CE}_3$ (t_{pd})	V_{CC} = 5.0V		360	700	ns
	V_{CC} = 10V		120	300	ns
Propagation Delay From $\overline{CE}_1$ or $\overline{CE}_2$ ($t_{p\overline{CE}1}$)	V_{CC} = 5 0V		250	500	ns
	V_{CC} = 10V		85	200	ns
Address Setup Time (t_{SA})	V_{CC} = 5.0V	200	80		ns
	V_{CC} = 10V	100	30		ns
Address Hold Time (t_{HA})	V_{CC} = 5.0V	50	15		ns
	V_{CC} = 10V	25	5		ns

ac electrical characteristics (con't)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{\text{Write}}$ $\overline{\text{Enable}}$ Pulse Width ($t_{\overline{WE}}$)	V_{CC} = 5.0V V_{CC} = 10V	300 150	160 70		ns ns
$\overline{CE}_3$ Pulse Widths (t_{CE})	V_{CC} = 5.0V V_{CC} = 10V	400 160	200 80		ns ns
Input Capacity (C_{IN})	Any Input (Note 2)		5.0		pF
Output Capacity in TRI-STATE (C_{OUT})	(Note 2)		9.0		pF
Power Dissipation Capacity (C_{pd})	(Note 3)		400		pF

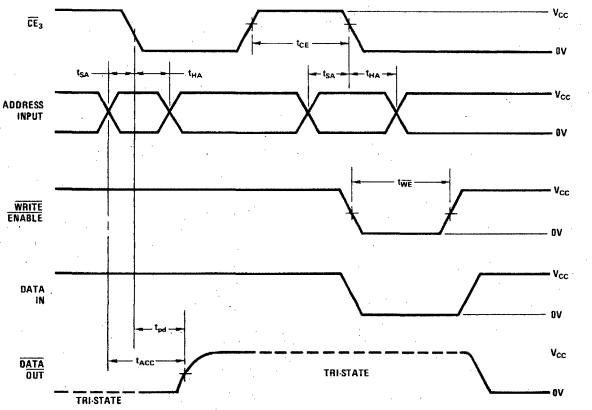
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

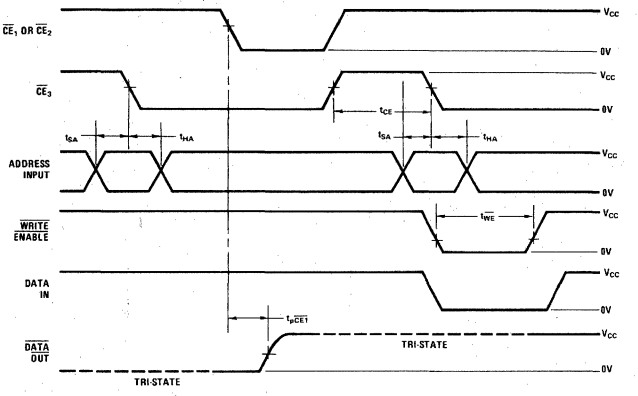
Note 3: C_{pd} determines the no load ac power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note, AN-90.

switching time waveforms

Read and Write Cycles Using $\overline{CE}_3$ ($\overline{CE}_1$ = $\overline{CE}_2$ = logic 0)



Read and Write Cycles Using $\overline{CE}_3$ and $\overline{CE}_1$ (or $\overline{CE}_2$)



Note: Used for fast access time in bused systems.

NATIONAL

CMOS RAMs

MM54C910/MM74C910 256-bit TRI-STATE® random access read/write memory

general description

The MM54C910/MM74C910 is a 64 word by 4 bit random access memory. Inputs consist of six address lines, four data input lines, a write enable, and a memory enable line. The six address lines are internally decoded to select one of 64 word locations. An internal address register, latches the address information on the positive to negative transition of memory enable. The TRI-STATE outputs allow for easy memory expansion.

Address Operation: Address inputs must be stable (t_{SA}) prior to the positive to negative transition of memory enable, and (t_{HA}) after the positive to negative transition of memory enable. The address register holds the information and stable address inputs are not needed at any other time.

Write Operation: Data is written into memory at the selected address if write enable goes low while memory enable is low. Write enable must be held low for $t_{\overline{WE}}$ and data must remain stable t_{HD} after write enable returns high.

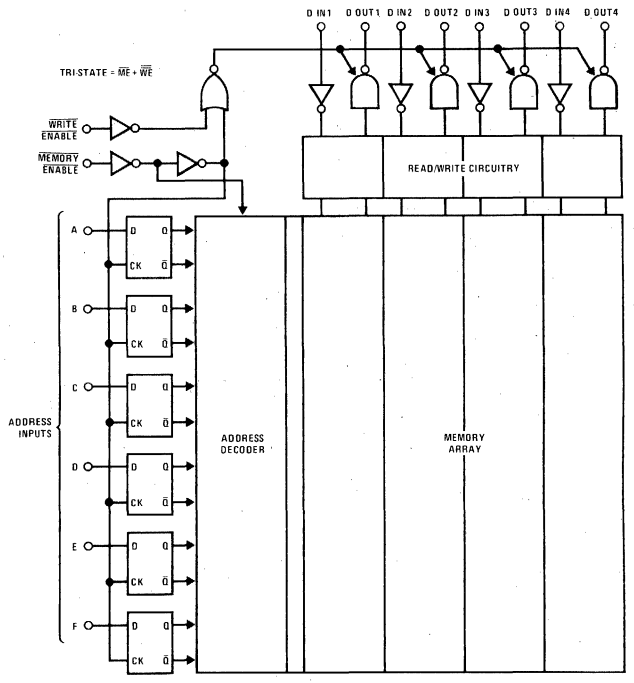
Read Operation: Data is nondestructively read from a memory location by an address operation with write enable held high.

Outputs are in the TRI-STATE (Hi-Z) condition when the device is writing or disabled.

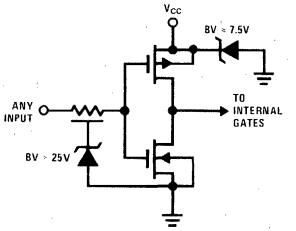
features

- Supply voltage range — 3V to 5.5V
- High noise immunity — 0.45 V_{CC} typ
- TTL compatible fan out — 1 TTL load
- Input address register
- Low power consumption — 250 nW/package typ (chip enabled or disabled)
- Fast access time — 250 ns typ at 5V
- TRI-STATE outputs
- High voltage inputs

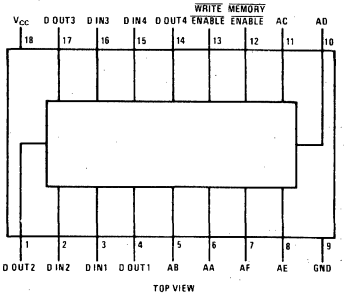
logic and connection diagrams



Input Protection



Dual-In-Line Package



Order Number MM54C910D
or MM74C910D
See Package 4

Order Number MM74C910N
See Package 16

absolute maximum ratings (Note 1)

Voltage At Any Output Pin	−0.3V to V_{CC} +0.3V
Voltage At Any Input Pin	−0.3V to +15V
Package Dissipation	500 mW
Operating V_{CC} Range	3.0V to 5.5V
Standby V_{CC} Range	1.5V to 5.5V
Absolute Maximum V_{CC}	6.0V
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
MM54C910	4.5	5.5	V
MM74C910	4.75	5.25	V
Temperature (T_A)			
MM54C910	−55	+125	°C
MM74C910	−40	+85	°C

dc electrical characteristics MM54C910/MM74C910

(Min/max limits apply across the temperature and power supply range indicated).

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$V_{IN(1)}$	Logical "1" Input Voltage	Full Range	V_{CC}−1.5			V
$V_{IN(0)}$	Logical "0" Input Voltage	Full Range			0.8	V
$I_{IN(1)}$	Logical "1" Input Current	V_{IN} = 15V		0.005	2	μA
		V_{IN} = 5V		0.005	1	μA
$I_{IN(0)}$	Logical "0" Input Current	V_{IN} = 0V	−1	−0.005		μA
$V_{OUT(1)}$	Logical "1" Output Voltage	I_O = −150μA	V_{CC}−0.5			V
		I_O = −400μA	2.4			V
$V_{OUT(0)}$	Logical "0" Output Voltage	I_O = 1.6 mA			0.4	V
	Output Current in High	V_O = 5V		0.005	1	μA
	Impedence State	V_O = 0V	−1	−0.005		μA
I_{CC}	Supply Current	V_{CC} = 5V		0.05	300	μA

ac electrical characteristics MM54C910/MM74C910

T_A = 25°C, V_{CC} = 5V, C_L = 50 pF

	PARAMETER	MIN	TYP	MAX	UNITS
t_{ACC}	Access Time from Address		250	500	ns
t_{PD}	Propagation Delay from $\overline{ME}$		180	360	ns
t_{SA}	Address Input Set-Up Time	140	70		ns
t_{HA}	Address Input Hold Time	20	10		ns
t_{ME}	Memory Enable Pulse Width	200	100		ns
$t_{\overline{ME}}$	Memory Enable Pulse Width	400	200		ns
t_{SD}	Data Input Set-Up Time	0			ns
t_{HD}	Data Input Hold Time	30	15		ns
$t_{\overline{WE}}$	Write Enable Pulse Width	140	70		ns
t_{1H}, t_{OH}	Delay to TRI-STATE (Note 4)		100	200	ns
CAPACITANCE					
C_{IN}	Input Capacity Any Input (Note 2)		5		pF
C_{OUT}	Output Capacity Any Output (Note 2)		9		pF
C_{PD}	Power Dissipation Capacity (Note 3)		350		pF

ac electrical characteristics (con't)

C_L = 50 pF

PARAMETER		MM54C910 T_A = −55°C to +125°C V_{CC} = 4.5V to 5.5V		MM74C910 T_A = −40°C to +85°C V_{CC} = 4.75V to 5.25V		UNITS
		MIN	MAX	MIN	MAX	
t_{ACC}	Access Time from Address		860		700	ns
t_{PD1}, t_{PD0}	Propagation Delay from $\overline{ME}$		660		540	ns
t_{SA}	Address Input Set-Up Time	200		160		ns
t_{HA}	Address Input Hold Time	20		20		ns
t_{ME}	$\overline{Memory\ Enable}$ Pulse Width	280		260		ns
$t_{\overline{ME}}$	$\overline{Memory\ Enable}$ Pulse Width	750		600		ns
t_{SD}	Data Input Set-Up Time	0		0		ns
t_{HD}	Data Input Hold Time	50		50		ns
$t_{\overline{WE}}$	$\overline{Write\ Enable}$ Pulse Width	200		180		ns
t_{1H}, t_{0H}	Delay to TRI-STATE (Note 4)		200		200	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

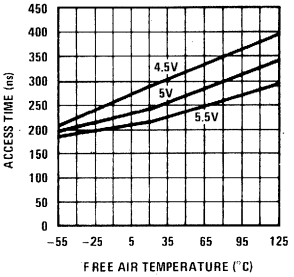
Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{pd} determines the no load ac power consumption for any CMOS device. For complete explanation see 54C/74C Family Characteristics application note, AN-90.

Note 4: See ac test circuit for t_{1H}, t_{0H}.

typical performance characteristics

Typical Access Time vs Ambient Temperature

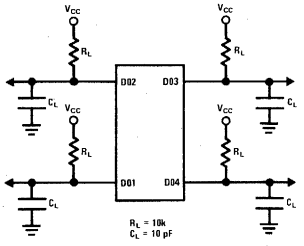


truth table

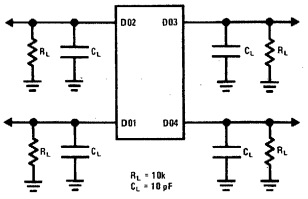
$\overline{ME}$	$\overline{WE}$	OPERATION	OUTPUTS
L	L	Write	TRI-STATE
L	H	Read	Data
H	L	Inhibit, Store	TRI-STATE
H	H	Inhibit, Store	TRI-STATE

ac test circuits

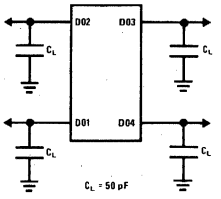
t_{0H}



t_{1H}

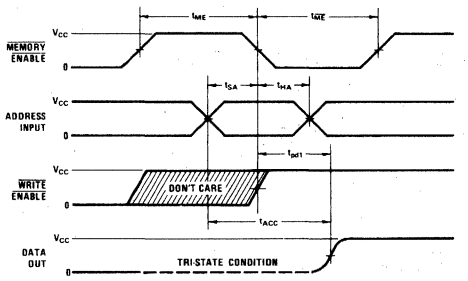


All Other AC Tests

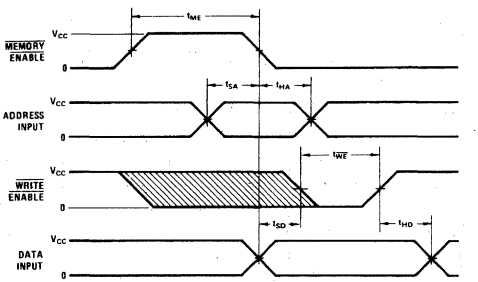


switching time waveforms

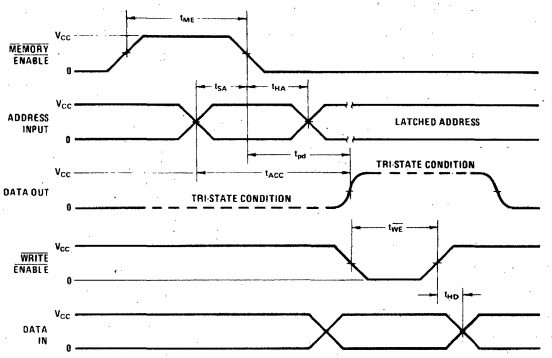
Read Cycle
(See Note 1)



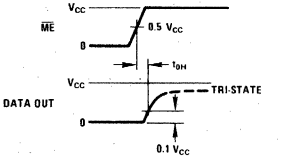
Write Cycle
(See Note 1)



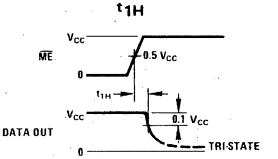
Read Modify Write Cycle
(See Note 1)



t_{0H}



t_{1H}



Note 1: MEMORY ENABLE must be brought high for t_{ME} nanoseconds between every address change.
Note 2: $t_r = t_f = 20$ ns for all inputs.

NATIONAL

CMOS RAMs
Advance Information

MM54C920/MM74C920 1024-bit static silicon gate CMOS RAM

general description

The MM54C920/MM74C920 256 x 4 random access read/write memory is manufactured using silicon gate CMOS technology. Data output is the same polarity as data input. Internal latches store address inputs, $\overline{CES}$ and data output. This RAM is specifically designed to operate from standard 54/74 TTL power supplies. All inputs and outputs are TTL compatible.

Complete address decoding as well as two chip select functions, $\overline{CEL}$ and $\overline{CES}$, and TRI-STATE® outputs allow easy expansion with a minimum of external components. Versatility plus high speed and low power make the MM54C920/MM74C920 an ideal element for use in microprocessor, minicomputer as well as main frame memory applications.

features

- Fast access—250 ns max
- TRI-STATE outputs
- Low power
- On-chip registers
- Single +5V supply
- Data retained with V_{CC} as low as 2V

functional description

The functional description will reference the logic diagram of the MM54C920/MM74C920 shown in *Figure 1.* Input addresses and $\overline{CES}$ are clocked into the input latches by the falling edge of $\overline{STROBE}$. Input setup and hold times must be observed on these signals (see timing diagrams). The true and complement address information is fed to the row and column decoders which access the selected 4-bit memory word.

logic and connection diagrams

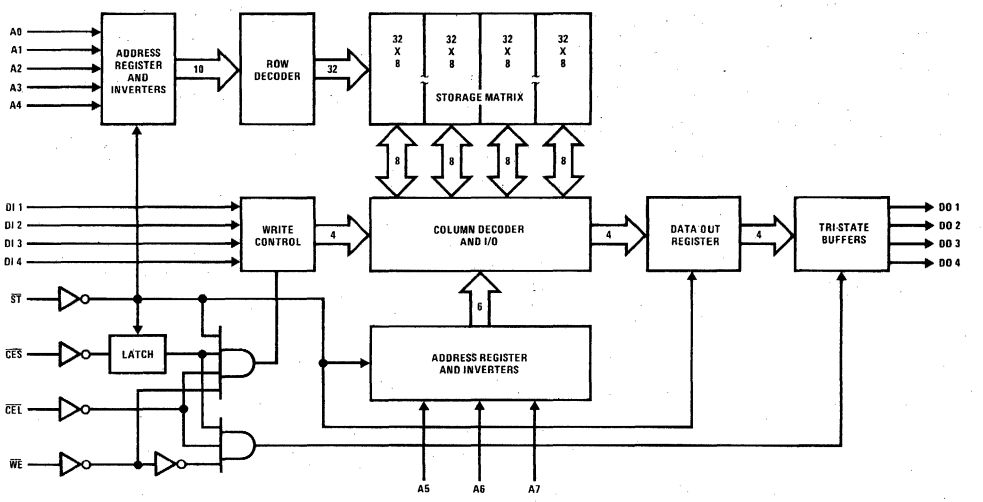
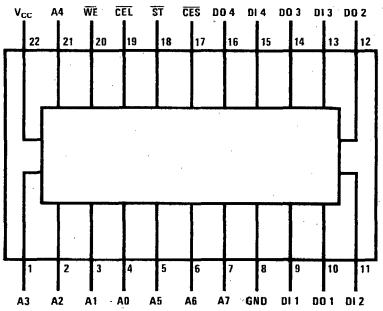


FIGURE 1. Logic Diagram

Dual-in-Line-Package



Order Number MM54C920D or MM74C920D
See Package 5
Order Number MM74C920N
See Package 17

functional description (con't)

The addressed word (4 bits) is fed to four sense amplifiers through the column decoders. The information from the sense amplifiers is retained in the output register when $\overline{\text{STROBE}}$ rises. The register drives the TRI-STATE output buffers.

Chip select inputs, $\overline{\text{CEL}}$ and $\overline{\text{CES}}$, have identical functions except that $\overline{\text{CES}}$ (Chip Enabled Stored) is clocked into a latch on the falling edge of $\overline{\text{STROBE}}$; $\overline{\text{CEL}}$ (Chip Enable Level) is not.

Note that setup and hold times must be observed on $\overline{\text{CES}}$. Because $\overline{\text{CEL}}$ is not clocked by $\overline{\text{STROBE}}$, it may fall after $\overline{\text{STROBE}}$ has fallen without affecting access time.

The outputs are in a high impedance state when the chip is not selected ($\overline{\text{CES}}$ or $\overline{\text{CEL}}$ high) or when writing ($\overline{\text{WE}}$ low). Note that the information stored in the output latches will be changed whenever $\overline{\text{STROBE}}$ falls, regardless of the logic states of $\overline{\text{WE}}$, $\overline{\text{CEL}}$ or $\overline{\text{CES}}$.

The timing diagrams in *Figures 2, 3, and 4* define the read, write, and output enable/disable parameters respectively. These timing diagrams and the logic diagram in *Figure 1* completely describe the operation of the RAM.

absolute maximum ratings

Supply Voltage, V_{CC}	7V
Voltage at Any Pin	$-0.3V$ to $V_{CC} + 0.3V$
Operating Temperature Range	
MM54C920	$-55°C$ to $+125°C$
MM74C920	$-40°C$ to $+85°C$
Storage Temperature Range	$-65°C$ to $+150°C$

dc electrical characteristics $V_{CC} = 5.0V \pm 10\%$, T_A = Operating Range

PARAMETER		CONDITIONS	MM54C920			MM74C920			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{IH}	Logical "1" Input Voltage		$V_{CC}-2.0$			$V_{CC}-2.0$			V
V_{IL}	Logical "0" Input Voltage				0.8			0.8	V
V_{OH1}	Logical "1" Output Voltage	$I_{OH} = -1.0$ mA	2.4			2.4			V
V_{OH2}	Logical "1" Output Voltage	$I_{OUT} = 0$	$V_{CC}-0.01$			$V_{CC}-0.01$			V
V_{OL1}	Logical "0" Output Voltage	$I_{OL} = 2.0$ mA			0.4			0.4	V
V_{OL2}	Logical "0" Output Voltage	$I_{OUT} = 0$			0.01			0.01	V
I_{IL}	Input Leakage	$0V \le V_{IN} \le V_{CC}$			1.0			1.0	μA
I_O	Output Leakage	$0V \le V_O \le V_{CC}$, $\overline{CEL} = V_{CC}$			1.0			1.0	μA
I_{CC}	Supply Current	$V_{IN} = V_{CC}$ or Gnd, $\overline{CEL} = V_{CC}$, DO = Open			100			100	μA
C_{IN}	Input Capacitance			5			5		pF
C_O	Output Capacitance			5			5		pF
V_{DR}	V_{CC} for Data Retention	$\overline{ST} = 0V$, $\overline{WE} = \overline{CEL} = V_{CC}$, DI = V_{CC} or Gnd	2.0			2.0			V

ac electrical characteristics $V_{CC} = 5.0V \pm 10\%$, T_A = Operating Range

PARAMETER		MM54C920			MM74C920			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
TTL Interface ($V_{IH} = V_{CC} - 2.0V$, $V_{IL} = 0.8V$, Input $t_{RISE} = t_{FALL} = 10$ ns, Load = 1 TTL Gate + 50 pF)								
t_C	Cycle Time	320	140		285	140		ns
t_{ACC}	Access Time From Address		120	275		120	250	ns
t_{AS}	Address Setup Time	25	10		25	10		ns
t_{AH}	Address Hold Time	25	15		25	15		ns
t_{OE}	Output Enable Time		60	120		60	110	ns
t_{OD}	Output Disable Time		60	120		60	110	ns
$t_{\overline{ST}}$	$\overline{ST}$ Pulse Width (Negative)	180	80		160	80		ns
t_{ST}	ST Pulse Width (Positive)	140	60		125	60		ns
t_{WP}	Write Pulse Width (Negative)	150	80		130	80		ns
t_{DS}	Data Setup Time	70	40		60	40		ns
t_{DH}	Data Hold Time	50	25		45	25		ns

switching time waveforms

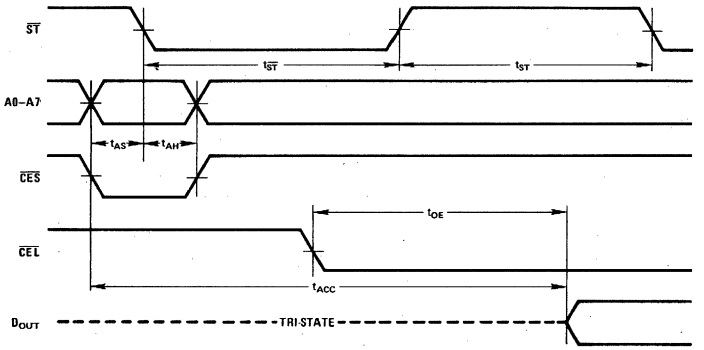


FIGURE 2. Read Cycle ($\overline{WE}$ = V_{IH})

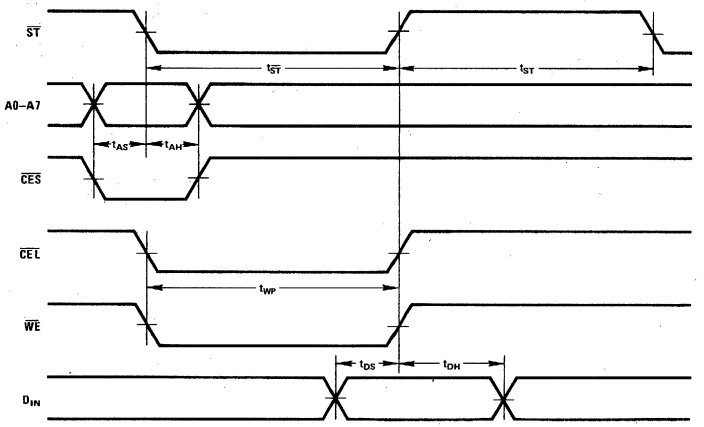


FIGURE 3.Write Cycle

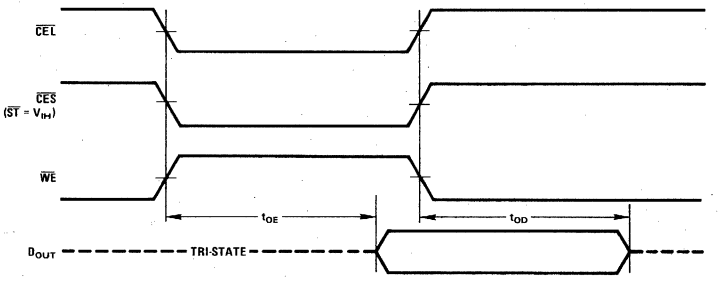


FIGURE 4. Output Enable/Disable

MOS EPROMs

MM1702A 2048-bit electrically programmable ROM

general description

The MM1702A is a 256 word by 8-bit electrically programmable ROM ideally suited for uses where fast turn-around and pattern experimentation are important. The MM1702A undergoes complete programming and functional testing on each bit position prior to shipment, thus insuring 100% programmability.

The MM1702AQ is packaged in a 24-pin dual-in-line package with a transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written into the device. The MM1702AD is packaged in a 24-pin dual-in-line package with a metal lid and is not erasable.

The circuitry of the MM1702A is entirely static; no clocks are required.

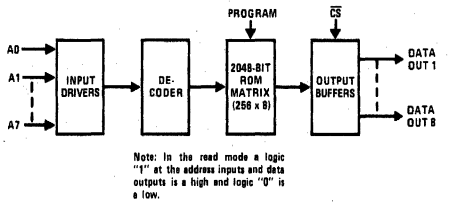
A pin-for-pin metal mask programmed ROM, the MM1302 is ideal for large volume production runs of systems initially using the MM1702A.

The MM1702A is fabricated with silicon gate technology. This low threshold technology allows the design and production of higher performance MOS circuits and provides a higher functional density on a monolithic chip than conventional MOS technologies.

features

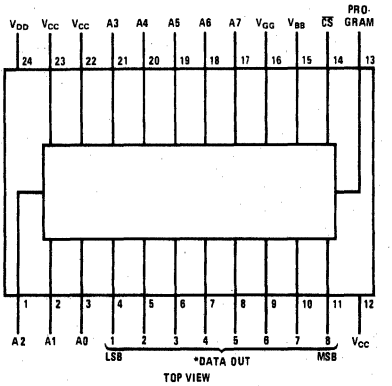
- Fast programming—30 seconds for all 2048 bits
- All 2048 bits guaranteed programmable—100% factory tested
- Fully decoded, 256 x 8 organization
- Static MOS—no clocks required
- Inputs and outputs DTL and TTL compatible
- TRI-STATE® output—OR-tie capability
- Simple memory expansion—chip select input lead
- Direct replacement for the Intel 1702A

block and connection diagrams



Note: In the read mode a logic "1" at the address inputs and data outputs is a high and logic "0" is a low.

Dual-In-Line Package



*This pin is the data input lead during programming.

Order Number MM1702AD
See Package 6
Order Number MM1702AQ
See Package 21

Pin Names

A0–A7	Address Inputs
$\overline{CS}$	Chip Select Input
$D_{OUT\,1} - D_{OUT\,8}$	Data Outputs

Pin Connections*

MODE/PIN	12 (V_{CC})	13 (PROGRAM)	14 ($\overline{CS}$)	15 (V_{BB})	16 (V_{GG})	22 (V_{CC})	23 (V_{CC})
Read	V_{CC}	V_{CC}	GND	V_{CC}	V_{GG}	V_{CC}	V_{CC}
Programming	GND	Program Pulse	GND	V_{BB}	Pulsed V_{GG} (V_{IL4P})	GND	GND

*The external lead connections to the MM1702A differ, depending on whether the device is being programmed or used in read mode. (See following table.) In the programming mode, the data inputs 1–8 are pins 4–11 respectively.

absolute maximum ratings (Note 1)

Ambient Temperature	0°C to +70°C
Storage Temperature	−65°C to +125°C
Power Dissipation	2W
Read Operation	
Input Voltages and Supply Voltages with Respect to V_{CC}	+0.5V to −20V
Program Operation	
Input Voltages and Supply Voltages with Respect to V_{CC}	−48V
Lead Temperature (Soldering, 10 seconds)	300°C

read operation dc characteristics

T_A = 0°C to +70°C, V_{CC} = +5V ±5%, V_{DD} = −9V ±5%, V_{GG} = −9V ±5%, unless otherwise noted. Typical values are at nominal voltages and T_A = 25°C. (Note 2)

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I_{LI}	Address and Chip Select Input Load Current	V_{IN} = 0.0V			1	μA
I_{LO}	Output Leakage Current	V_{OUT} = 0.0V, $\overline{CS}$ = V_{CC} −2			1	μA
I_{DDO}	Power Supply Current	V_{GG} = V_{CC}, $\overline{CS}$ = V_{CC} −2 I_{OL} = 0.0 mA, T_A = 25°C, (Note 2)		5	10	mA
I_{DD1}	Power Supply Current	$\overline{CS}$ = V_{CC} −2, I_{OL} = 0.0 mA, T_A = 25°C		35	50	mA
I_{DD2}	Power Supply Current	$\overline{CS}$ = 0.0, I_{OL} = 0.0 mA, T_A = 25°C		32	46	mA
I_{DD3}	Power Supply Current	$\overline{CS}$ = V_{CC} −2, I_{OL} = 0.0 mA, T_A = 0°C		38.5	60	mA
I_{CF1}	Output Clamp Current	V_{OUT} = −1.0V, T_A = 0°C		8	14	mA
I_{CF2}	Output Clamp Current	V_{OUT} = −1.0, T_A = 25°C			13	mA
I_{GG}	Gate Supply Current				1	μA
V_{IL1}	Input Low Voltage for TTL Interface		−1.0		V_{CC}−4.1	V
V_{IL2}	Input Low Voltage for MOS Interface		V_{DD}		V_{CC}−6	V
V_{IH}	Address and Chip Select Input High Voltage		V_{CC}−2		V_{CC}+0.3	V
I_{0L}	Output Sink Current	V_{OUT} = 0.45V	1.6	4		mA
I_{0H}	Output Source Current	V_{OUT} = 0.0V	−2.0			mA
V_{0L}	Output Low Voltage	I_{OL} = 1.6 mA		−0.7	0.45	V
V_{0H}	Output High Voltage	I_{OH} = −100μA	3.5	4.5		V

Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Note 2: Power-Down Option: V_{GG} may be clocked to reduce power dissipation. The average I_{DD} will vary between I_{DD0} and I_{DD1} depending on the V_{GG} duty cycle (see typical characteristics). For this option, please specify MM1702AL.

read operation ac characteristics

$T_A = 0°C$ to $+70°C$, $V_{CC} = +5V \pm 5\%$, $V_{DD} = -9V \pm 5\%$, $V_{GG} = -9V \pm 5\%$, unless otherwise noted.

PARAMETER		MIN	TYP	MAX	UNITS
Freq.	Repetition Rate			1	MHz
t_{0H}	Previous Read Data Valid			100	ns
t_{ACC}	Address to Output Delay		0.7	1	μs
t_{DVGG}	Clocked V_{GG} Set-Up (Note 1)	1			μs
t_{CS}	Chip Select Delay			100	ns
t_{CO}	Output Delay From $\overline{CS}$			900	ns
t_{0D}	Output Deselect			300	ns
t_{0HC}	Data Out Hold in Clocked V_{GG} Mode (Note 1)			5	μs

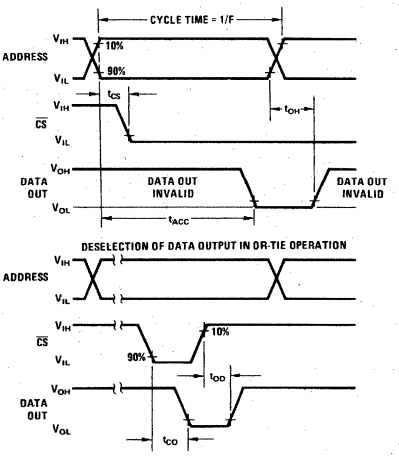
capacitance characteristics $T_A = 25°C$ (Note 3)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
C_{IN}	Input Capacitance	All Unused	$V_{IN} = V_{CC}$		8	15	pF
C_{OUT}	Output Capacitance	Pins Are	$\overline{CS} = V_{CC}$		10	15	pF
C_{VGG}	V_{GG} Capacitance (Note 1)	At ac Ground	$V_{OUT} = V_{CC}$ $V_{GG} = V_{CC}$			30	pF

Note 3: This parameter is periodically sampled and is not 100% tested.

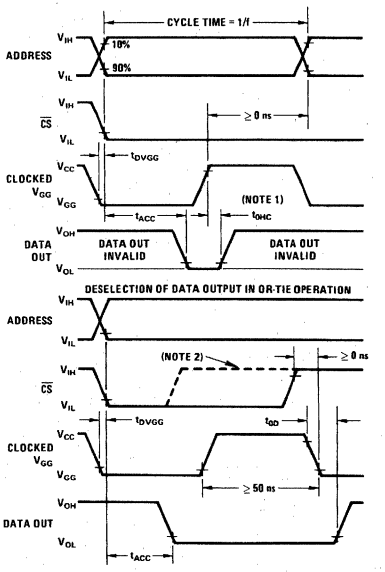
read operation switching time waveforms

(a) Constant V_{GG} Operation



Conditions of Test:
Input pulse amplitudes: 0–4V, t_r, $t_f \leq 50$ ns. Output load is 1 TTL gate; measurements made at output of TTL gate ($t_{PD} \leq 15$ ns), $C_L = 15$ pF.

(b) Power-Down Option (Note 1)



Note 1: The output will remain valid for t_{0HC} as long as clocked V_{GG} is at V_{CC}. An address change may occur as soon as the output is sensed (clocked V_{GG} may still be at V_{CC}). Data becomes invalid for the old address when clocked V_{GG} is returned to V_{GG}.

Note 2: If $\overline{CS}$ makes a transition from V_{IL} to V_{IH} while clocked V_{GG} is at V_{GG}, then deselection of output occurs at t_{OD} as shown in static operation with constant V_{GG}.

programming operation dc characteristics

$T_A = 25°C$, $V_{CC} = 0V$, $V_{BB} = 12V \pm 10\%$, $\overline{CS} = 0V$ unless otherwise noted.

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I_{LI1P}	Address and Data Input Load Current	$V_{IN} = -48V$			10	mA
I_{LI2P}	Program and V_{GG} Load Current	$V_{IN} = -48V$			10	mA
I_{BB}	V_{BB} Supply Load Current	(Note 5)		10	100	mA
I_{DDP}	Peak I_{DD} Supply Load Current	$V_{DD} = V_{PROG} = -48V$ $V_{GG} = -35V$ (Note 4)		200	300	mA
V_{IHP}	Input High Voltage				0.3	V
V_{IL1P}	Pulsed Data Input Low Voltage		−46		−48	V
V_{IL2P}	Address Input Low Voltage		−40		−48	V
V_{IL3P}	Pulsed Input Low V_{DD} and Program Voltage		−46		−48	V
V_{IL4P}	Pulsed Input Low V_{GG} Voltage		−35		−40	V

Note 4: I_{DDP} flows only during V_{DD}, V_{GG} on time. I_{DDP} should not be allowed to exceed 300 mA for greater than 100μs. Average power supply current I_{DDP} is typically 40 mA at 20% duty cycle.

Note 5: The V_{BB} supply must be limited to 100 mA max current to prevent damage to the device.

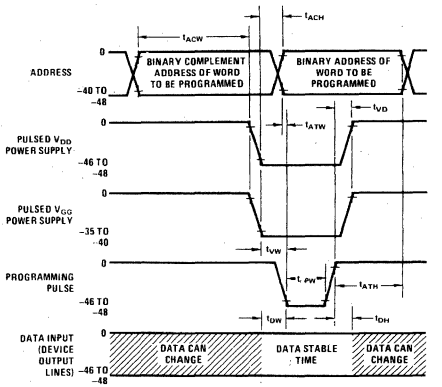
programming operation ac characteristics

$T_A = 25°C$, $V_{CC} = 0V$, $V_{BB} = 12V \pm 10\%$, $\overline{CS} = 0V$ unless otherwise noted.

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
	Duty Cycle (V_{DD}, V_{GG})				20	%
$t_{\phi PW}$	Program Pulse Width	$V_{GG} = -35V$, $V_{DD} = V_{PROG} = -48V$			3	ms
t_{DW}	Data Set-Up Time		25			μs
t_{DH}	Data Hold Time		10			μs
t_{VW}	V_{DD}, V_{GG} Set-Up		100			μs
t_{VD}	V_{DD}, V_{GG} Hold		10		100	μs
t_{ACW}	Address Complement Set-Up	(Note 6)	25			μs
t_{ACH}	Address Complement Hold	(Note 6)	25			μs
t_{ATW}	Address True Set-Up		10			μs
t_{ATH}	Address True Hold		10			μs

Note 6: All 8 address bits must be in the complement state when pulsed V_{DD} and V_{GG} move to their negative levels. The addresses (0–255) must be programmed as shown in the timing diagram until data reads true, then over-programmed 4 times that amount. (Symbolized by x + 4x.)

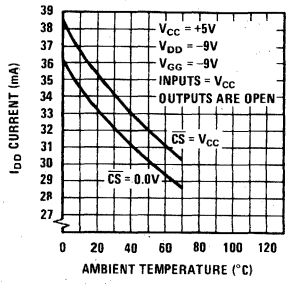
programming operation switching time waveforms



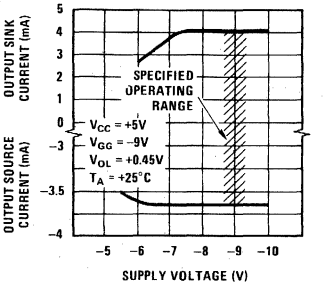
Conditions of Test:
Input pulse rise and fall times ≤ 1μs
$\overline{CS}$ = 0V

typical performance characteristics

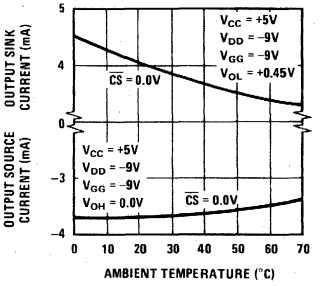
I_{DD} Current vs Temperature



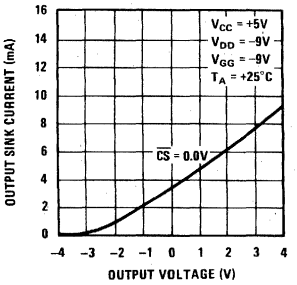
Output Current vs V_{DD} Supply Voltage



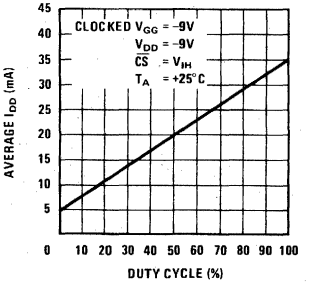
Program Waveforms



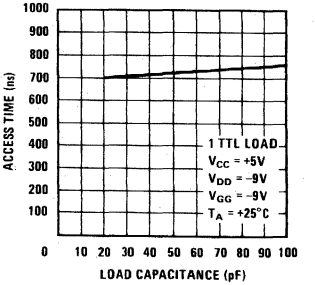
Output Sink Current vs Output Voltage



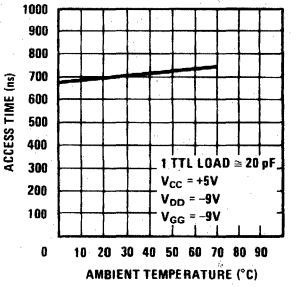
Average Current vs Duty Cycle for Clocked V_{GG} (Note 1)



Access Time vs Load Capacitance



Access Time vs Temperature



operation of the MM1702A in program mode

Initially, all 2048 bits of the ROM are in the "0" state (output low). Information is introduced by selectively programming "1's" (output high) in the proper bit locations.

Word address selection is done by the same decoding circuitry used in the READ mode (see table for logic levels). All 8 address bits must be in the binary complement state when pulsed V_{DD} and V_{GG} move to their negative levels. The addresses must be held in their binary complement state for a minimum of 25μs after V_{DD} and V_{GG} have moved to their negative levels. The addresses must then make the transition to their true state a minimum of 10μs before the program pulse is applied. The addresses should be programmed in the sequence 0—255 for a minimum of 32 times. The eight output terminals are used as data inputs to determine the information pattern in the eight bits of each word. A low data input level (−48V) will program a "1" and a high data input level (ground) will leave a "0" (see table on page 4-4). All eight bits of one word are programmed simultaneously be setting the desired bit information patterns on the data input terminals.

During the programming, V_{GG}, V_{DD} and the Program Pulse are pulsed signals.

MM1702A erasing procedure

The MM1702A may be erased by exposure to high intensity short-wave ultraviolet light at a wavelength of 2537Å. The recommended integrated dose (i.e., UV intensity x exposure time) is 6W sec/cm^2. Examples of ultraviolet sources which can erase the MM1702A in 10 to 20 minutes are the Model UVS-54 and Model S-52 short-wave ultraviolet lamps manufactured by Ultra-Violet Products, Inc. (5114 Walnut Grove Avenue, San Gabriel, California). The lamps should be used without short-wave filters, and the MM1702A to be erased should be placed about one inch away from the lamp tubes. There exists no absolute rule for erase time. Establish a worst case time required with the equipment. Then over-erase by a factor of 2, i.e., if the device appears erased after 8 minutes, continue exposure for an additional 16 minutes for a total of 24 minutes. (May be expressed as x + 2x.)

MOS EPROMs

MM4203/MM5203 electrically programmable 2048-bit read only memory (pROM)

general description

The MM4203/MM5203 is a 2048-bit static read-only memory which is electrically programmable and uses silicon gate technology to achieve bipolar compatibility. The device is a non-volatile memory organized as a 256-8-bit words or 512-4-bit words. Programming of the memory contents is accomplished by storing a charge in a cell location by programming that location with a 50 volt pulse. Separate output supply lead is provided to reduce internal power dissipation in the output stage (V_{LL}).

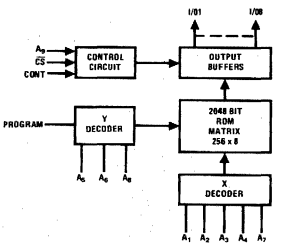
features

- Field programmable
- Bipolar compatibility +5V, −12V operation
- High speed operation 1μs max access time
- Pin compatible with MM5213, MM5231 mask programmable ROMs
- Static operation — no clocks required
- Common data busing (TRI-STATE® output)
- "Q" quartz lid version erasable with short wave ultra-violet light (i.e. 253.7 n.m.)
- Chip select output control
- 256 x 8 or 512 x 4 organization

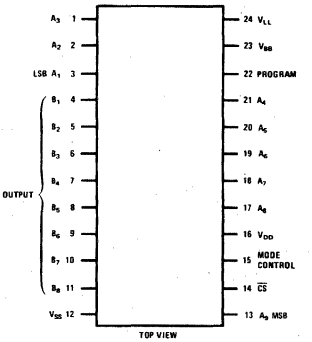
applications

- Code conversion
- Random logic synthesis
- Table look-up
- Character generator
- Micro-programming

block and connection diagrams



Dual-In-Line Package

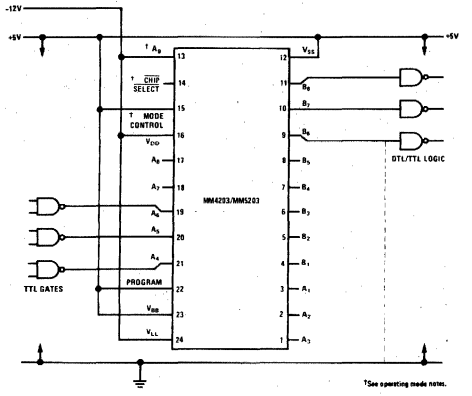


Order Number MM4203D or MM5203D
See Package 6

Order Number MM4203Q or MM5203Q
See Package 21

typical applications

256 x 8 PROM Showing TTL Interface



Note: For programming information see AN-100.

Operating Modes

256 x 8 ROM connection (shown)
Mode Control — HIGH (V_{SS})
A_9 — LOW

512 x 4 ROM connections
Mode Control — LOW (GND or V_{DD})
A_9 — Logic HIGH enables the odd (B_1, B_3..B_7) outputs
— Logic LOW enables the even (B_2, B_4..B_8) outputs

The outputs are enabled when a logic LOW is applied to the Chip Select line.

Programming is accomplished in 256 x 8 mode only.

absolute maximum ratings

All Input or Output Voltages with Respect to V_{BB} Except During Programming	+.3V to −20V	Storage Temperature Range	−65°C to 125°C
Power Dissipation	1W	Lead Temperature (Soldering, 10 sec)	300°C
Operating Temperature Range MM4203	−55°C to 85°C		
MM5203	0°C to 70°C		

electrical characteristics T_A within operating temperature range,

V_{SS} = +5V ±5%, V_{DD} = V_{LL} = −12V, ±5%, V_{BB} = PROGRAM = V_{SS} unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Current, I_{LI}	V_{IN} = 0V			1	μA
Output Leakage, I_{LO}	V_{OUT} = 0V $\overline{CS}$ = V_{SS} - 2.0			1	μA
Power Supply Current, I_{SS}	T_A = 25°C $\overline{CS}$ = V_{SS} - 2.0		35	55	mA
Input LOW Voltage, V_{IL}		V_{SS} - 10		V_{SS} - 4.0	V
Input HIGH Voltage, V_{IH}		V_{SS} - 2.0		V_{SS} + .3	V
Output LOW Voltage, V_{OL}	1.6 mA sink −12.6V < V_{LL} < −3V			.40	V
Output Clamp Current, I_{CF}	V_{LL} = −3.0V V_{OUT} = −1.0V (Note 8) T_A = 0°C		3.5	6.0	mA
	V_{LL} = −12.6V V_{OUT} = −1.0V (Note 8) T_A = 0°C		8.0	15.0	mA
Output HIGH Voltage, V_{OH}	0.8 mA source	2.4			V
Data Hold Time, T_{OH}	(Min Access Time) Figures 1 & 2			100	ns
Access Time, T_{ACC}	T_A = 25°C Figures 1 & 2 (Note 6)		.700	1	μs
Chip Select Time, T_{CO}	Figures 1 & 3			500	ns
Chip Deselect Time, T_{OD}	Figures 1 & 3			500	ns
Allowable Chip Select Delay, t_{CS}	Figures 1 & 2 Allowable delay in selecting chip after change of address without affecting access time.			100	ns
Input Capacitance, C_{IN}	V_{IN} = V_{SS} } f = 1.0 MHz (Note 2)		8	15	pF
Output Capacitance, C_{OUT}	V_{OUT} = V_{SS} } $\overline{CS}$ = V_{SS} - 2.0		8	15	pF

programming characteristics (see Figure 4)

T_A = 25°C, V_{SS} = 0V, V_{BB} = +12V ±10%, $\overline{CS}$ = 0V unless otherwise noted

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Address and Data Input Load Current, I_{LD}	V_{IN} = −50V		0	10	mA
Program Load Current, I_{LP}	V_{IN} = −50V		0	10	mA
V_{BB} Supply Load Current, I_{LB}			0	10	mA
Peak I_{DD} Supply Load Current I_{LDD} (Note 3)	V_{DD} = $V_{program}$ = −50V		650		mA
Input High Voltage, V_{IHP}		−2		+.3	V
Address and Data Input Low Voltage, V_{ILP}		−50		−40	V
Pulsed Input Low Voltage:					
V_{DD}, and Program, V_{DLP}		−50		−48	V
V_{LL}	(Note 5)	−50		0	V
V_{DD} Pulse Duty Cycle				2	%
Program Pulse Width, t_{PW} (Note 4)	V_{DD} = $V_{program}$ = −50V			20	ms
Data and Address Set Up Time, t_{DW}		1			μs
Data and Address Hold Time, t_{DH}		0			μs
Pulsed V_{DD} Supply Overlap, t_{SS}		1		100	μs
Pulsed V_{DD} Supply Overlap, t_{SH}		−.1		3	ms
V_{DD}, Program, Address, and Input Rise and Fall Times				1	μs

Note 1: During programming, data is always applied in the 256 x 8 mode, regardless of the logic state of A_9 and MODE CONTROL.

Note 2: Capacitances are not tested on a production basis but are periodically sampled.

Note 3: I_{DDP} flows only during program period t_{PWP}. Average power supply current I_{LDD} is typically 15 mA at 2% duty cycle.

Note 4: Maximum duty cycle of t_{PW} should not be greater than 2% of cycle time so that power dissipation is minimized. The program cycle should be repeated until the data reads true, then over-program three times that number of cycles (symbolized as X+3X programming.

Note 5: V_{LL} is not needed during programming but may be tied to V_{DD} for convenience.

Note 6: T_{ACC} = 1000 ns + 25(N−1) where N is the number of chips wired-OR together.

Note 7: Measured under continuous operation.

Note 8: I_{CF} flows out the V_{LL} pin, it does not flow out the V_{DD} pin.

access time diagrams

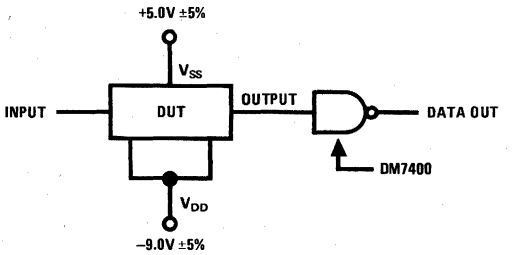


Figure 1

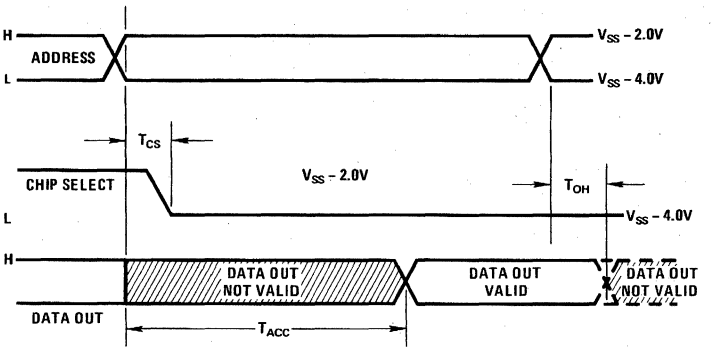


Figure 2

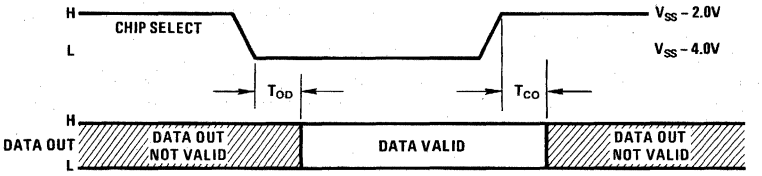


Figure 3

program waveforms

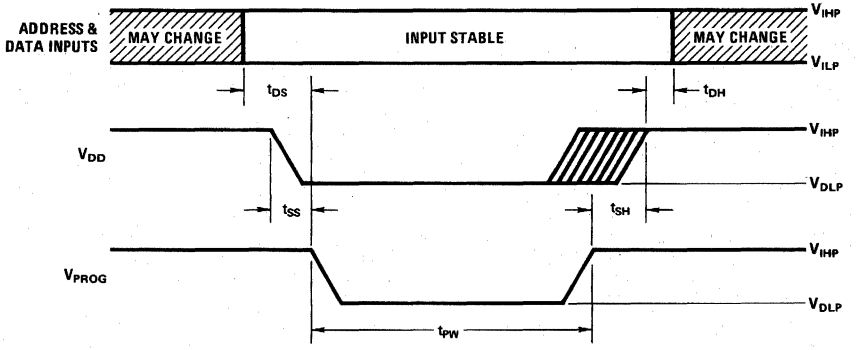


Figure 4

operation of the MM4203/MM5203 in program mode

Initially, all 2048 bits of the MM4203/MM5203 are in the HIGH state. Information is introduced by selectively programming LOWS in the proper bit locations. (Note 1)

Word address selection is done by the same decoding circuitry used in the Read mode. The eight output terminals are used as data inputs to determine the information pattern in the eight bits of each word. A LOW data input level (−50V) will leave a HIGH and a HIGH data input level will allow programming of a LOW. All eight bits of one word are programmed simultaneously by setting the desired bit information patterns on the data input terminals. The duty cycle of the V_{DD} pulse (amplitude and width as specified on page 4) should be limited to 2%. The address should be applied for at least 1 μs before application of the Program pulse. In programming mode, data inputs 1–8 are pins 4–11 respectively regardless of the logic state of A_9 and mode control. Chip select should be disabled (HIGH).

Positive logic is used during the read mode for addresses and data out. Address 0 corresponds to all address inputs at V_{IL} and address 255_{10} corresponds to all address inputs at V_{IH}. A "1" or a P at a data output corresponds to V_{OH}. A "0" or an N at a data output corresponds to V_{OL}. Positive logic is also used during the programming mode for addresses. Address 0 corresponds to all address inputs at V_{ILP} and address 255_{10} corresponds to all address inputs at V_{IHP}.

Negative logic is used during the programming mode for data in. A "1" or a P at a data input corresponds to V_{ILP}. A "0" or an N at a data input corresponds to V_{IHP}.

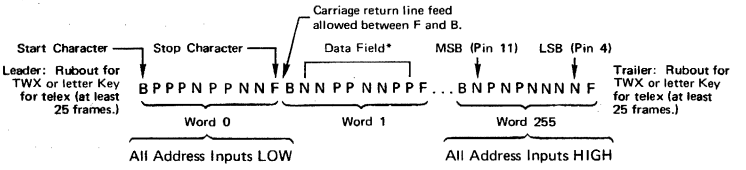
MODE	DATA AND ADDRESS LINES HIGH	DATA AND ADDRESS LINES LOW	V_{SS}	V_{BB}	V_{DD}	PROGRAM	$\overline{CS}$	V_{LL}
Read	V_{SS} −2.0	V_{SS} − 4.0	+5	V_{SS}	−12	V_{SS}	V_{SS} − 4V	−3V to −12V
Program	V_{SS} −2.0	V_{SS} − 40	GND	+12	−48 (Pulse)	−48 (Pulse)	GND	GND to −50V

erasing procedure

The MM4203Q/MM5203Q may be erased by exposure to short-wave ultraviolet light—253.7 nm. There exists no absolute rule for erasing time or distance from source. The erasing equipment output capability should be calibrated. Establish a worst-case time required with the equipment. Then over-erase by a factor of 2, i.e., if the device appears erased after 8 minutes, continue exposure for an additional 16 minutes for a total of 24 minutes. Examples of UV sources include the Model UVS-54 and Model S-2 manufactured by Ultra-Violet Products, Inc. (5114 Walnut Grove Avenue, San Gabriel, California). The lamps should be used without short-wave filters. The MM4203/MM5203 should be placed about one inch away from the lamp for about 20–30 minutes.

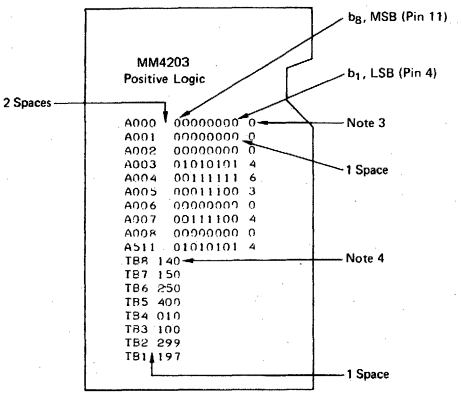
preferred tape format

The custom patterns may be sent in on a Telex or submitted as a paper tape in a 7 bit ASCII code from model 33 teletype or TWX. The paper tape should be as the following example:



*Data Field: Must have only P's or N's typed between B and F. No nulls or rubouts. Must have exactly eight P and N characters between B and F. Any characters except B and F may be typed between the F stop character and the B start character. If an error is made in preparing a tape the entire word including the B and F start and stop characters must be rubbed out. Data for exactly 256 words must be entered, beginning with word 0.

alternate format [Punched Tape (Note 1) or Cards]



Note 1: The code is a 7-bit ASCII code on 8 punch tape. The tape should begin and end with 25 or more "RUBOUT" punches.

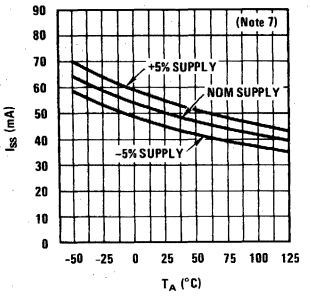
Note 2: The ROM input address is expressed in decimal form and is preceded by the letter A.

Note 3: The total number of "1" bits in the output word.

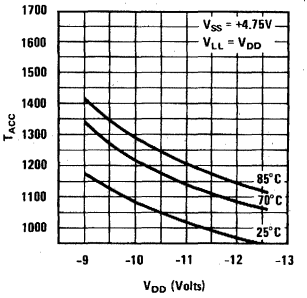
Note 4: The total number of "1" bits in each output column or bit position.

typical performance characteristics

Maximum Supply Current I_{SS} as a Function of Temperature



Maximum Access Time (T_{ACC}) as a Function of V_{DD} Supply Voltage



NATIONAL

MOS EPROMs

MM4204/MM5204
electrically programmable 4096-bit read only memory (EROM)

general description

The MM4204/MM5204 is a 4096-bit static Read Only Memory which is electrically programmable and uses silicon gate technology to achieve bipolar compatiblity. The device is a non-volatile memory organized as 512 words by 8 bits per word. Programming of the memory is accomplished by storing a charge in a cell location by applying a −50V pulse. A logic input, "Power Saver," is provided which gives a 5:1 decrease in power when the memory is not being accessed.

- Standard power supplies 5.0V, −12V
- Static operation—no clock required
- Easy memory expansion—TRI-STATE® output Chip Select input ($\overline{CS}$)
- "Q" quartz lid version erasable with short wave ultraviolet light (i.e., 253.7 nm)
- Low power dissipation
- "Power Saver" control for low power applications

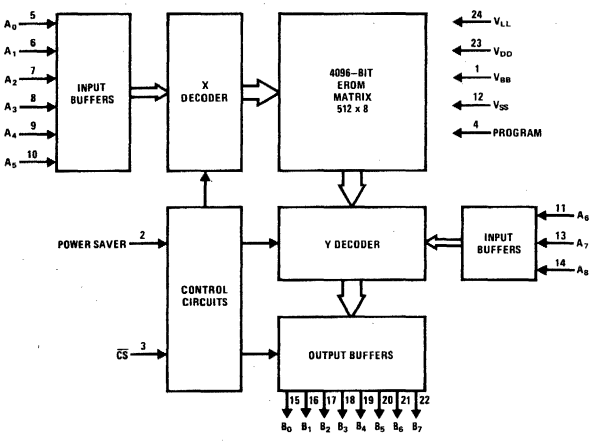
features

- Field programmable
- Fast program time: ten seconds typical for 4096-bits
- Fast access time
  - MM4204 1.25μs
  - MM5204 1μs
- DTL/TTL compatibility

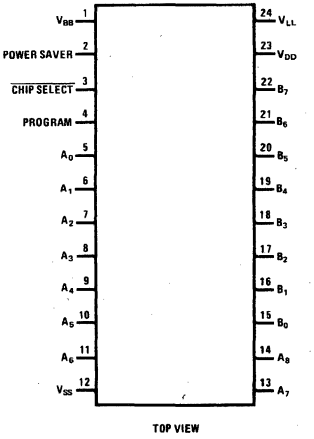
applications

- Code conversion
- Random logic synthesis
- Table look-up
- Character generator
- Microprogramming
- Electronic keyboards

block and connection diagrams



Dual-In-Line Package



TOP VIEW

Order Number MM4204D or MM5204D
See Package 6

Order Number MM4204Q or MM5204Q
See Package 21

absolute maximum ratings (Note 1)

All Input or Output Voltages with Respect to V_{BB} Except During Programming	+0.3V to −20V
Power Dissipation	750 mW
Operating Temperature Range	
MM5204	0°C to +70°C
MM4204	−55°C to +85°C
Storage Temperature Range	−65°C to +125°C
Lead Temperature (Soldering, 10 seconds)	300°C

dc electrical characteristics

T_A within operating temperature range, V_{LL} = 0V, V_{BB} = PROGRAM = V_{SS}, MM4204: V_{SS} = 5.0V ±10%, V_{DD} = −12V ±10%, MM5204: V_{SS} = 5.0V ±5%, V_{DD} = −12V ±5%, unless otherwise noted.

PARAMETER		CONDITIONS	MIN	TYP (Note 7)	MAX	UNITS
V_{IL}	Input Low Voltage		V_{SS}−14		V_{SS}−4.2	V
V_{IH}	Input High Voltage		V_{SS}−1.5		V_{SS}+0.3	V
I_{LI}	Input Current	V_{IN} = 0V			1.0	μA
V_{OL}	Output Low Voltage	I_{OL} = 1.6 mA	V_{LL}		0.4	V
V_{OH}	Output High Voltage	I_{OH} = −0.8 mA	2.4		V_{SS}	V
I_{LO}	Output Leakage Current	V_{OUT} = 0V, $\overline{CS}$ = V_{IH}			1.0	μA
I_{DD}	Power Supply Current	MM5204 T_A = 0°C, $\overline{CS}$ = V_{IH}, Power Saver = V_{IL}		28	40.0	mA
		MM4204 T_A = 0°C, $\overline{CS}$ = V_{IH}, Power Saver = V_{IL}			50.0	mA
		MM5204 T_A = 0°C, $\overline{CS}$ = V_{IH}, Power Saver = V_{IH}		6.0	8.0	mA
		MM4204 T_A = 0°C, $\overline{CS}$ = V_{IH}, Power Saver = V_{IH}			10.0	mA
I_{SS}		MM5204 T_A = 0°C, $\overline{CS}$ = V_{IH}, Power Saver = V_{IL}			42	mA
		MM4204 T_A = 0°C, $\overline{CS}$ = V_{IH}, Power Saver = V_{IL}			52	mA
		MM5204 T_A = 0°C, $\overline{CS}$ = V_{IH}, Power Saver = V_{IH}			10	mA
		MM4204 T_A = 0°C, $\overline{CS}$ = V_{IH}, Power Saver = V_{IH}			12	mA

ac electrical characteristics

T_A within operating temperature range, V_{LL} = 0V, V_{BB} = PROGRAM = V_{SS}, MM4204: V_{SS} = 5.0V ±10%, V_{DD} = −12V ±10%, MM5204: V_{SS} = 5.0V ±5%, V_{DD} = −12V ±5%, unless otherwise noted.

PARAMETER		CONDITIONS	MIN	TYP (Note 7)	MAX	UNITS
t_{ACC}	Access Time					
	MM5204	T_A = 70°C, *(Figure 1)*, (Note 4)		0.75	1.0	μs
	MM4204	T_A = 85°C, *(Figure 1)*, (Note 4)			1.25	μs
t_{PO}	Power Saver Set-Up Time					
	MM5204	*(Figure 1)*			1.8	μs
	MM4204	*(Figure 1)*			2.0	μs
t_{CO}	Chip Select Delay					
	MM5204	*(Figure 1)*			500	ns
	MM4204	*(Figure 1)*			600	ns
t_{OH}	Data Hold Time	*(Figure 1)*	30	50		ns
t_{ODC}	Chip Select Deselect Time					
	MM5204	*(Figure 1)*	30	300	500	ns
	MM4204	*(Figure 1)*	30	300	600	ns
t_{ODP}	Power Saver Deselect Time					
	MM5204	*(Figure 1)*	30	300	500	ns
	MM4204	*(Figure 1)*	30	300	600	ns
C_{IN}	Input Capacitance (All Inputs)	V_{IN} = V_{SS}, f = 1.0 MHz, (Note 2)		5.0	8.0	pF
C_{OUT}	Output Capacitance (All Outputs)	V_{OUT} = V_{SS}, $\overline{CS}$ = V_{IH}, f = 1.0 MHz, (Note 2)		8.0	15	pF

programmer electrical characteristics

$T_A = 25°C$, $V_{SS} = \overline{CS}$ = Power Saver = 0V, V_{LL} = 0V to −14V, unless otherwise specified, (see *Figure 2*), (Note 5).

PARAMETER		CONDITIONS	MIN	TYP (Note 7)	MAX	UNITS
I_{LD}	Data Input Load Current	V_{IN} = −18V			−10	mA
I_{ALD}	Address Input Load Current	V_{IN} = −50V			−10	mA
I_{LP}	Program Load Current	V_{IN} = −50V			−10	mA
I_{LBB}	V_{BB} Load Current				50	mA
I_{LDD}	V_{DD} Load Current	V_{DD} = PROGRAM = −50V			−200	mA
V_{IHP}	Address Data and Power Saver Input High Voltage		−2.0		0.3	V
V_{ILP}	Address Input Low Voltage		−50		−11	V
	Data Input Low Voltage		−18		−11	V
V_{DHP}	V_{DD} and Program High Voltage		−2.0		0.5	V
V_{DLP}	V_{DD} and Program Low Voltage		−50		−48	V
V_{BLP}	V_{BB} Low Voltage		0		0.4	V
V_{BHP}	V_{BB} High Voltage		11.4		12.6	V
V_{DD}	Pulse Duty Cycle				25	%
t_{PW}	Program Pulse Width		0.5		5.0	ms
t_{DS}	Data and Address Set-Up Time		40			μs
t_{DH}	Data and Address Hold Time		0			μs
t_{SS}	Pulsed V_{DD} Set-Up Time		40		100	μs
t_{SH}	Pulsed V_{DD} Hold Time		1.0			μs
t_{BS}	Pulsed V_{BB} Set-Up Time		1.0			μs
t_{BH}	Pulsed V_{BB} Hold Time		1.0			μs
t_{PSS}	Power Saver Set-Up Time		1.0			μs
t_{PSH}	Power Saver Hold Time		1.0			μs
t_R, t_F	V_{DD}, Program, Address and Data Rise and Fall Time				1.0	μs

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: Positive true logic notation is used except on data inputs during programming
Logic "1" = most positive voltage level
Logic "0" = most negative voltage level

Note 4: t_{ACC} = 1000 ns + 25 (N-1) where N is the number of devices wire—OR'd together.

Note 5: The program cycle should be repeated until the data reads true, then over-programmed 5 times that number of cycles. (Symbolized as X + 5X programming).

Note 6: The EROM is initially programmed with all "0's." A V_{IHP} on any data input B0—B7 will leave the stored "0's" undisturbed, and a V_{ILP} on any data input B0—B7 will write a logic "1" into that location.

Note 7: Typical values are for nominal voltages and $T_A = 25°C$, unless otherwise specified.

erase specification

The recommended dosage of ultraviolet light exposure is 6W sec/cm².

programming

The MM4204/MM5204 is normally shipped in the unprogrammed state. All 4096-bits are at logic "0" state. The table of electrical programming characteristics and *Figure 2* give the conditions for programming of the device. In the program mode the device effectively becomes a RAM with the 512 word locations selected by address inputs A0—A8. Data inputs are B0—B7 and write operation is controlled by pulsing the Program input. Since the EROM is initially shipped with all "0's," a V_{IHP} on any data input B0—B7 will leave the stored "0's" undisturbed and a V_{ILP} on any data input B0—B7 will write a logic "1" into that location.

programming (cont.)

National offers programmer options with both the IMP16-P and the PACE IPC-16P Microprocessor Development Systems.

Microprocessor System	Programmer Part Number
IMP16-P	IMP-16P/805
IPC-16P	IPC-16P/805

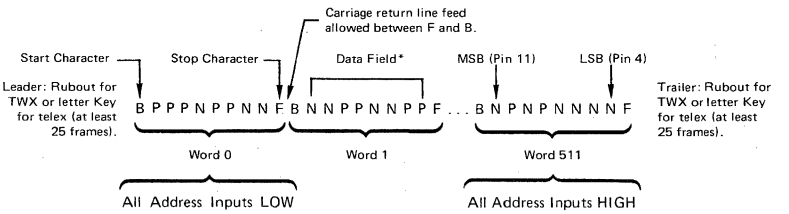
Contact the local sales office for further information. There are also several commercial programmers available such as the Data I/O Model V.

Most National distributors have programming capabilities available. Those distributors should be contacted directly to determine which data entry formats are available.

In addition, data may be submitted to National Semiconductor for factory programming. One of the following formats should be observed:

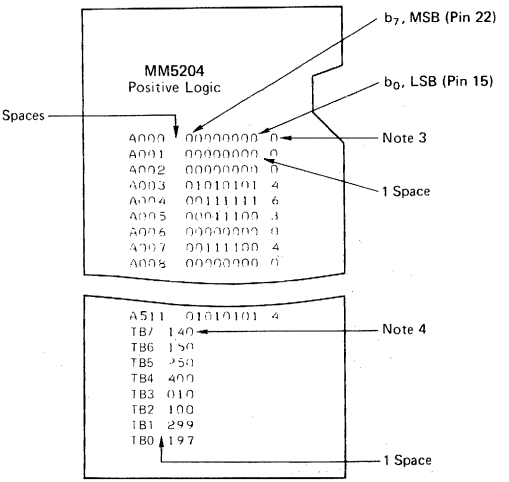
preferred format

The custom patterns may be sent in on a Telex or submitted as a paper tape in a 7-bit ASCII code from model 33 teletype or TWX. The paper tape should be as the following example:



*Data Field: Must have only P's or N's typed between B and F. No nulls or rubouts. Must have exactly eight P and N characters between B and F. Any characters except B and F may be typed between the F stop character and the B start character. If an error is made in preparing a tape the entire word including the B and F start and stop characters must be rubbed out. Data for exactly 512 words must be entered beginning with word 0.

alternate format [Punched Tape (Note 1) or Cards]



Note 1: The code is a 7-bit ASCII code on 8 punch tape. The tape should begin and end with 25 or more "RUBOUT" punches.

Note 2: The ROM input address is expressed in decimal form and is preceded by the latter A.

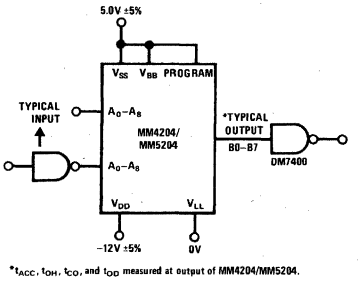
Note 3: The total number of "1" bits in the output word.

Note 4: The total number of "1" bits in each output column or bit position.

erasing procedure

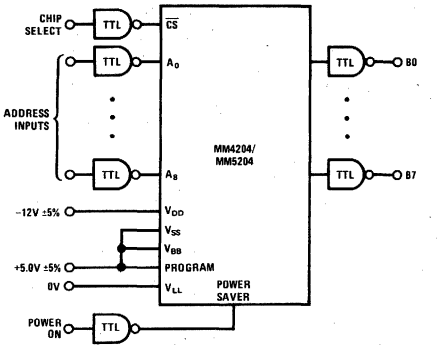
The MM4204Q/MM5204Q may be erased by exposure to short-wave ultraviolet light—253.7 nm. There exists no absolute rule for erasing time or distance from source. The erasing equipment output capability should be calibrated. Establish a worse case time required with the equipment. Then over-erase by a factor of 2,i.e., if the device appears erased after 8 minutes, continue exposure for an additional 16 minutes for a total of 24 minutes. Examples of UV sources include the Model UVS-54 and Model S-52 manufactured by Ultra-Violet Products, Inc. (5114 Walnut Grove Avenue, San Gabriel, California). The lamps should be used without short-wave filters. The MM4204/MM5204 should be placed about one inch away from the lamp for about 20—30 minutes.

ac test circuit

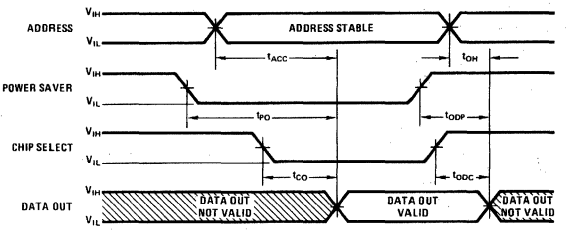


*t_{ACC}, t_{OH}, t_{CO}, and t_{OD} measured at output of MM4204/MM5204.

typical application



switching time waveforms



Note: All times measured with respect to 1.5V level with t_R and $t_F \leq 20$ ns.

FIGURE 1. Read Operation

programming waveforms

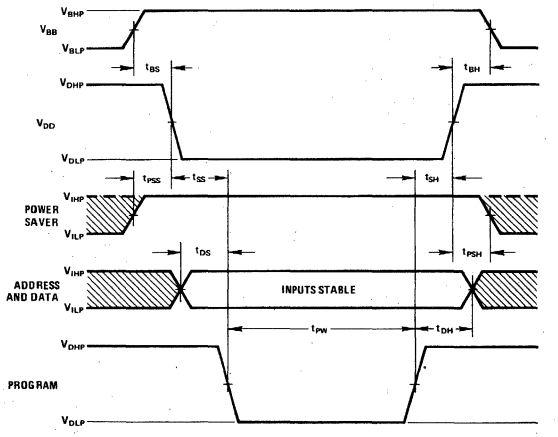


FIGURE 2. Programming Waveforms

NATIONAL

Bipolar PROMs
Advance Information

DM54S287/DM74S287 TRI-STATE® 1024-bit PROM
DM54S387/DM74S387 open-collector 1024-bit PROM

general description

These TTL compatible memories are organized in the popular 256 words by 4 bits configuration. Two memory enable inputs are provided to control the output states. When both enable inputs are in the logical "0" state, the outputs present the contents of the word selected by the address inputs.

If either or both of the enable inputs is raised to a logical "1" level, it causes all four outputs to go to the "OFF" or high impedance state. The memories are available in both open-collector and TRI-STATE versions and are available as ROMs as well as PROMs.

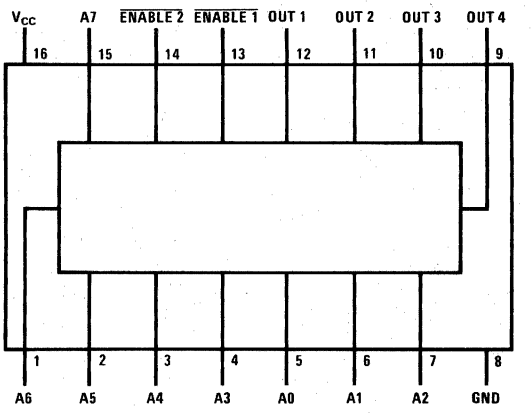
PROMs are shipped from the factory with a logical "0" in all locations. A logical "1" may be programmed into any selected locations by following the programming instructions. Once programmed, it is impossible to go back to a logical "0"; however, additional bits may be programmed to a logical "1."

features

- Schottky clamped for high speed systems
- High speed
  - Enable to output delay—typical 15 ns
  - Address to output delay—typical 30 ns
- PNP inputs reduce input loading
- All dc and switching characteristics may be measured prior to programming PROMs

connection diagram

Dual-In-Line Package



TOP VIEW

Order Number DM54S287D or DM54S387D
See Package 3
Order Number DM74S287N or DM74S387N
See Package 15

absolute maximum ratings (Note 1)

Supply Voltage (Note 2)	−0.5V to +7.0V
Input Voltage (Note 2)	−1.2V to +5.5V
Output Voltage (Note 2)	−0.5V to +5.5V
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DM54S287, DM54S387	4.5	5.5	V
DM74S287, DM74S387	4.75	5.25	V
Ambient Temperature (T_A)			
DM54S287, DM54S387	−55	+125	°C
DM74S287, DM74S387	0	+70	°C
Logical "0" Input Voltage	0	0.8	V
Logical "1" Input Voltage	2.0	5.5	V

dc electrical characteristics (Note 3)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
I_{IH}	Logical "1" Input Current	V_{IN} = 2.7V			25	μA
		V_{IN} = 5.5V			1.0	mA
I_{IL}	Logical "0" Input Current	V_{IN} = 0.45V			−250	μA
V_{CL}	Input Clamp Voltage	I_{IN} = −18 mA			−1.2	V
V_{OL}	Logical "0" Output Voltage	I_{OL} = 16 mA			0.50	V
I_{CC}	Maximum Supply Current			80	130	mA
DM54S387, DM74S387						
I_{OH}	Logical "1" Output Current	V_{OUT} = 2.4V			50	μA
		V_{OUT} = 5.5V			100	μA
DM54S287, DM74S287						
V_{OH}	Logical "1" Output Voltage					
	DM54S287	I_{OH} = −2.0 mA	2.4			V
	DM74S287	I_{OH} = −6.5 mA	2.4			V
I_{OS}	Output Short Circuit Current	V_{OUT} = 0V (Note 4) V_{CC} = Max	−30		−100	mA
I_{OZ}	TRI-STATE Output Current	$0.45V \leq V_{OUT} \leq 2.4V$	−50		50	μA

switching characteristics (Note 3)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{AA}	Address to Output Delay	R_L = 300Ω C_L = 30 pF		30		ns
t_{EA}	Time to Enable Output			15		ns
t_{ED}	Time to Disable Output			15		ns

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at these values.

Note 2: These limits do not apply to PROMs during programming. For the absolute maximum ratings, refer to the programming instructions.

Note 3: These limits apply over the entire operating range unless stated otherwise. All typical values are for V_{CC} = 5.0V and T_A = 25°C.

Note 4: During I_{OS} measurement, only one output at a time should be grounded. Permanent damage may otherwise result.

Bipolar PROMs
Advance Information

DM54S470/DM74S470 open-collector 2048-bit PROM
DM54S471/DM74S471 TRI-STATE® 2048-bit PROM

general description

These TTL compatible memories are organized in the versatile 256 words by 8 bits configuration. Two memory enable inputs are provided to further enhance their versatility. When both enable inputs are in the logical "0" state, the eight outputs present the contents of the word selected by the address inputs.

If either or both of the enable inputs is raised to a logical "1" level, it causes all eight outputs to go to the "OFF" or high impedance state. The memories are available in both open-collector and TRI-STATE versions and are available as ROMs as well as PROMs.

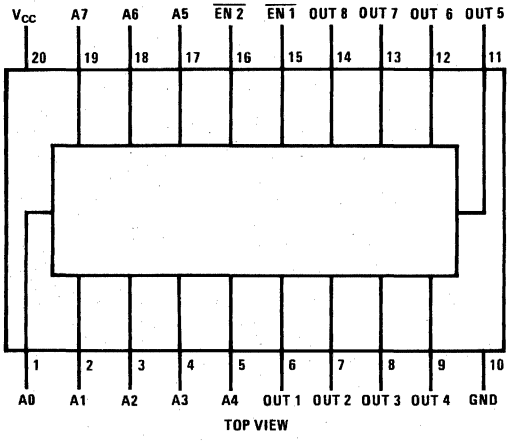
PROMs are shipped from the factory with a logical "0" in all locations. A logical "1" may be programmed into any selected locations by following the programming instructions. Once programmed, it is impossible to go back to a logical "0"; however, additional bits may be programmed to a logical "1."

features

- Schottky clamped for high-speed systems
- High speed
  - Address to output delay 35 ns
  - Enable to output delay 15 ns
- PNP inputs reduce input loading
- 20 pin, 300 mil package for high density
- All dc and switching characteristics may be measured prior to programming PROMs

connection diagram

Dual-In-Line Package



TOP VIEW

Order Number DM74S470N or DM74S471N
See Package 16A

absolute maximum ratings (Note 1)

Supply Voltage (Note 2)	−0.5V to +7.0V
Input Voltage (Note 2)	−1.2V to +5.5V
Output Voltage (Note 2)	−0.5V to +5.5V
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DM54S470, DM54S471	4.5	5.5	V
DM74S470, DM74S471	4.75	5.25	V
Ambient Temperature (T_A)			
DM54S470, DM54S471	−55	+125	°C
DM74S470, DM74S471	0	+70	°C
Logical "0" Input Voltage	0	0.8	V
Logical "1" Input Voltage	2.0	5.5	V

dc electrical characteristics (Note 3)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
I_{IH}	Logical "1" Input Current	V_{IN} = 2.7V			25	μA
		V_{IN} = 5.5V			1.0	mA
I_{IL}	Logical "0" Input Current	V_{IN} = 0.45V			−250	μA
V_{CL}	Input Clamp Voltage	I_{IN} = −18 mA			−1.2	V
V_{OL}	Logical "0" Output Voltage	I_{OL} = 16 mA			0.50	V
I_{CC}	Maximum Supply Current			100	150	mA
DM54S470, DM74S470						
I_{OH}	Logical "1" Output Current	V_{OUT} = 2.4V			50	μA
		V_{OUT} = 5.5V			100	μA
DM54S471, DM74S471						
V_{OH}	Logical "1" Output Voltage					
	DM54S471	I_{OH} = −2.0 mA	2.4			V
	DM74S471	I_{OH} = −6.5 mA	2.4			V
I_{OS}	Output Short Circuit Current	V_{OUT} = 0V (Note 4) V_{CC} = Max	−30		−100	mA
I_{OZ}	TRI-STATE Output Current	$0.45V \leq V_{OUT} \leq 2.4V$	−50		50	μA

switching characteristics (Note 3)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{AA}	Address to Output Delay			35		ns
t_{EA}	Time to Enable Output	R_L = 300Ω C_L = 30 pF		15		ns
t_{ED}	Time to Disable Output			15		ns

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at these values.

Note 2: These limits do not apply to PROMs during programming. For the absolute maximum ratings, refer to the programming instructions.

Note 3: These limits apply over the entire operating range unless stated otherwise. All typical values are for V_{CC} = 5.0V and T_A = 25°C.

Note 4: During I_{OS} measurement, only one output at a time should be grounded. Permanent damage may otherwise result.

NATIONAL

Bipolar PROMs
Advance Information

DM54S570/DM74S570 open-collector 2048-bit PROM
DM54S571/DM74S571 TRI-STATE® 2048-bit PROM

general description

These TTL compatible memories are organized as 512 words by 4 bits. These devices effectively double the capacity of the popular 1k ROMs on the market by utilizing one chip-enable input as an additional address. When the circuit is enabled, the 4 outputs present the contents of the word selected by the address inputs.

An overriding enable input is provided which, if in the logical "1" state, causes all outputs to go to the "OFF" state, or high impedance state. Available in both open-collector or TRI-STATE, both versions are also available as Programmable Read Only Memories.

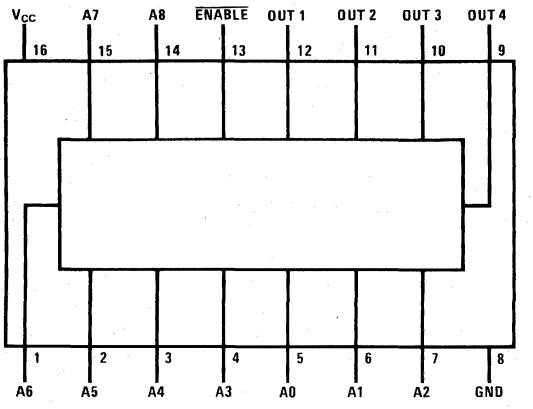
PROM's are shipped from the factory with a logical "0" in all locations. A logical "1" may be programmed into any selected locations by following the programming instructions. Once programmed, it is impossible to go back to a logical "0." Additional bits may be programmed to a logical "1," however.

features

- Schottky clamped for high speed systems
- High speed
  - Address to output delay—typical 35 ns
  - Enable to output delay—typical 15 ns
- PNP inputs reduce input loading
- All dc and switching characteristics may be measured prior to programming PROMs

connection diagram

Dual-In-Line Package



TOP VIEW

Order Number DM54S570D, DM54S571D, DM74S570D, DM74S571D
See Package 3
Order Number DM74S570N or DM74S571N
See Package 15

absolute maximum ratings (Note 1)

Supply Voltage (Note 2)	−0.5V to +7.0V
Input Voltage (Note 2)	−1.2V to +5.5V
Output Voltage (Note 2)	−0.5V to +5.5V
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DM54S570, DM54S571	4.5	5.5	V
DM74S570, DM74S571	4.75	5.25	V
Ambient Temperature (T_A)			
DM54S570, DM54S571	−55	+125	°C
DM74S570, DM74S571	0	+70	°C
Logical "0" Input Voltage	0	0.8	V
Logical "1" Input Voltage	2.0	5.5	V

dc electrical characteristics (Note 3)

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I_{IH}	Logical "1" Input Current	V_{IN} = 2.7V			25	μA
		V_{IN} = 5.5V			1.0	mA
I_{IL}	Logical "0" Input Current	V_{IN} = 0.45V			−250	μA
V_{CL}	Input Clamp Voltage	I_{IN} = −18 mA			−1.2	V
V_{OL}	Logical "0" Output Voltage	I_{OL} = 16 mA			0.50	V
I_{CC}	Maximum Supply Current			100	150	mA
DM54S570, DM74S570						
I_{OH}	Logical "1" Output Current	V_{OUT} = 2.4V			50	μA
		V_{OUT} = 5.5V			100	μA
DM54S571, DM74S571						
V_{OH}	Logical "1" Output Voltage					
	DM54S571	I_{OH} = −2.0 mA	2.4			V
	DM74S571	I_{OH} = −6.5 mA	2.4			V
I_{OS}	Output Short Circuit Current	V_{OUT} = 0V (Note 4) V_{CC} = Max	−30		−100	mA
I_{OZ}	TRI-STATE Output Current	$0.45V \leq V_{OUT} \leq 2.4V$	−50		50	μA

switching characteristics (Note 3)

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{AA}	Address to Output Delay	R_L = 300Ω C_L = 30 pF		35		ns
t_{EA}	Time to Enable Output			15		ns
t_{ED}	Time to Disable Output			15		ns

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at these values.

Note 2: These limits do not apply to PROMs during programming. For the absolute maximum ratings, refer to the programming instructions.

Note 3: These limits apply over the entire operating range unless stated otherwise. All typical values are for V_{CC} = 5.0V and T_A = 25°C.

Note 4: During I_{OS} measurement, only one output at a time should be grounded. Permanent damage may otherwise result.

NATIONAL

Bipolar PROMs
Advance Information

DM72S114/DM82S114 TRI-STATE® 2048-bit PROM with latches

general description

These TTL compatible memories are organized as 256 words by 8 bits. Two enable inputs are provided. When the strobe input is at a logical "1" level the memories function in the conventional manner with the enable inputs determining whether the outputs present the contents selected by the address inputs or are in the high impedance state. The outputs are in the high impedance state unless enable 1 is at a logical "0" and enable 2 is at a logical "1."

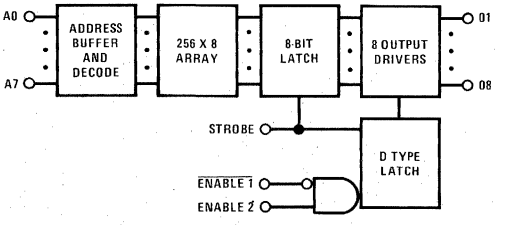
When the strobe is at a logical "0" the outputs are latched into the state they were in just prior to the strobe going low. The outputs remain in this condition until the strobe is again taken to the logical "1" state regardless of the state of the address or enable inputs.

PROMs are shipped from the factory with a logical "0" in all locations. A logical "1" may be programmed into any selected locations by following the programming instructions. Once programmed, it is impossible to go back to a logical "0"; however, additional bits may be programmed to a logical "1."

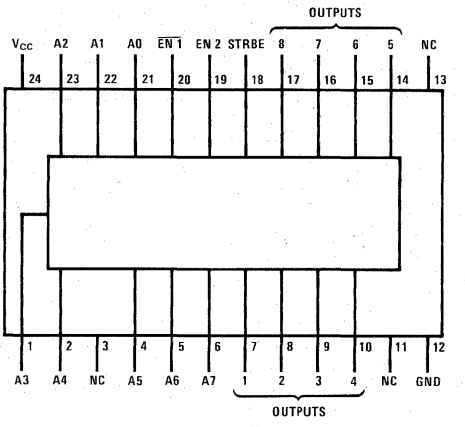
features

- Schottky clamped for high speed systems
- High speed
  - Enable to output delay 15 ns
  - Strobe to output delay 20 ns
  - Address to output delay 35 ns
- PNP inputs reduce input loading
- Output latches simplify system use
- All dc and switching characteristics may be measured prior to programming PROMs

logic and connection diagrams



Dual-In-Line Package



TOP VIEW

(NC = No Connection Internally)

Order Number DM72S114D or DM82S114D
See Package 6

Order Number DM82S114N
See Package 18

absolute maximum ratings (Note 1)

Supply Voltage (Note 2)	−0.5V to +7.0V
Input Voltage (Note 2)	−1.2V to +5.5V
Output Voltage (Note 2)	−0.5V to +5.5V
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DM72S114	4.5	5.5	V
DM82S114	4.75	5.25	V
Ambient Temperature (T_A)			
DM72S114	−55	+125	°C
DM82S114	0	+75	°C
Logical "0" Input Voltage	0	0.80	V
Logical "1" Input Voltage	2.0	5.5	V

dc electrical characteristics (Note 3)

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I_{IH}	Logical "1" Input Current	V_{IN} = 2.7V			25	μA
		V_{IN} = 5.5V			1	mA
I_{IL}	Logical "0" Input Current					
	DM72S114	V_{IN} = 0.45V			−250	μA
	DM82S114				−100	μA
V_{CL}	Input Clamp Voltage	I_{IN} = −18 mA			−1.2	V
V_{OL}	Logical "0" Output Voltage					
	DM72S114	I_{OUT} = 12 mA			0.50	V
	DM82S114				0.45	V
V_{OH}	Logical "1" Output Voltage					
	DM72S114	I_{OUT} = −2.0 mA	2.4			V
	DM82S114	I_{OUT} = −2.0 mA	2.7			V
	DM82S114	I_{OUT} = −6.5 mA	2.4			V
I_{OS}	Output Short Circuit Current	V_{OUT} = 0V (Note 4) V_{CC} = Max	−30		−100	mA
I_{OZ}	TRI-STATE Output Current					
	DM72S114	$0.45V \leq V_{OUT} \leq 2.4V$	−50		50	μA
	DM82S114	$0.45V \leq V_{OUT} \leq 5.5V$	−50		50	μA
I_{CC}	Maximum Supply Current			110	170	mA

switching characteristics (Note 3)

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{AA}	Address to Output Delay	Strobe = "1"		35		ns
t_{EA}	Time to Enable Output	Strobe = "1"		15		ns
t_{ED}	Time to Disable Output	Strobe = "1"		15		ns
t_{SA}	Strobe to Output Delay			20		ns
t_{SW}	Strobe Pulse Width			10		ns

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at these values.

Note 2: These limits do not apply to PROMs during programming. For the absolute maximum ratings, refer to the programming instructions.

Note 3: These limits apply over the entire operating range unless stated otherwise. All typical values are for V_{CC} = 5.0V and T_A = 25°C.

Note 4: During I_{OS} measurement, only one output at a time should be grounded. Permanent damage may otherwise result.

Bipolar PROMs

DM7573/DM8573 1024-bit field-programmable read only memory

general description

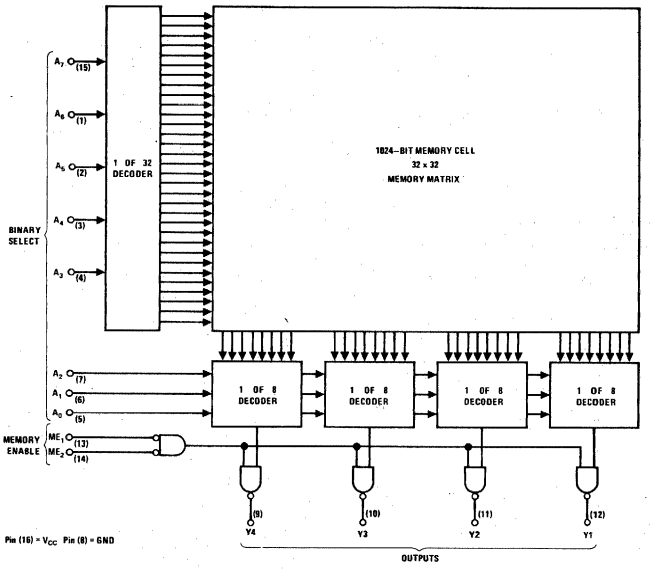
The DM7573/DM8573 is a field-programmable read-only memory organized as 256 four-bit words. Selection of the proper word is accomplished through the eight select inputs. Two overriding memory enable inputs are provided; when either or both of the enable inputs are taken to a high state, all the outputs will be turned off. A logical "1" has been built into each bit location. A logical "0" can be programmed into any bit by selecting the proper word, disabling the chip, and applying a programming pulse to the proper output.

An additional feature of the DM7573/DM8573 is that its outputs can be tested in the logical "0" state without permanently programming the memory. In order to place all outputs in the logical "0" state, a 9V level is applied to the most significant address input, Pin 15. This feature will allow a much more complete test to be made before a part is shipped, thus minimizing customer returns.

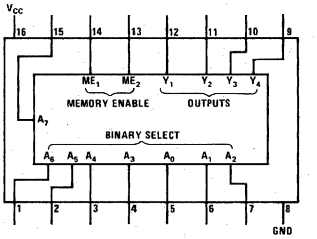
features

- Can be programmed in 1 sec (50% logical 1's; 50% logical 0's)
- Pin compatible with SN54187/SN74187
- Can be programmed after being connected in a system
- Outputs can be fully tested before programming
- Typical power dissipation 400 mW
- Propagation delay 60 ns

logic and connection diagrams



Dual-In-Line Package



TOP VIEW

Order Number DM7573D or DM8573D
See Package 3

Order Number DM8573N
See Package 15

absolute maximum ratings (Note 1)

Supply Voltage	7.0V
Input Voltage	5.5V (12V on Pins 13, 14)
Output Voltage	5.5V (25V for programming)
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DM7573	4.5	5.5	Volts
DM8573	4.75	5.25	Volts
Temperature (T_A)			
DM7573	−55	+125	°C
DM8573	0	70	°C

electrical characteristics (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	V_{CC} = Min	2.0			V
Logical "0" Input Voltage	V_{CC} = Min			0.8	V
Logical "1" Output Current	V_{CC} = Max, V_O = 4.0V			50	μA
Logical "0" Output Voltage	V_{CC} = Min, I_O = 16 mA			0.4	V
Logical "1" Input Current	V_{CC} = Max, V_{IN} = 2.4V V_{CC} = Max, V_{IN} = 5.5V			40 1	μA mA
Logical "0" Input Current	V_{CC} = Max, V_{IN} = 0.4V			−1	mA
Supply Current	V_{CC} = Max		82	110	mA
Input Clamp Voltage	V_{CC} = Min, I_{IN} = −12 mA			−1.5	V
Propagation Delay to a Logical "0" from Address to Output, t_{pd0}	V_{CC} = 5.0V T_A = 25°C		60		ns
Propagation Delay to a Logical "0" from Enable to Output, t_{pd0}	V_{CC} = 5.0V T_A = 25°C		28		ns
Propagation Delay to a Logical "1" from Address to Output, t_{pd1}	V_{CC} = 5.0V T_A = 2.5°C		60		ns
Propagation Delay to a Logical "1" from Enable to Output, t_{pd1}	V_{CC} = 5.0V T_A = 25°C		28		ns

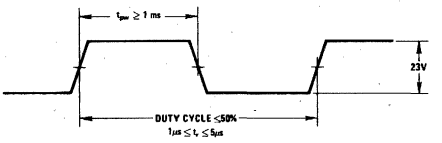
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55° to +125°C temperature range for the DM7573 and across the 0°C to 70°C range for the DM8573. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

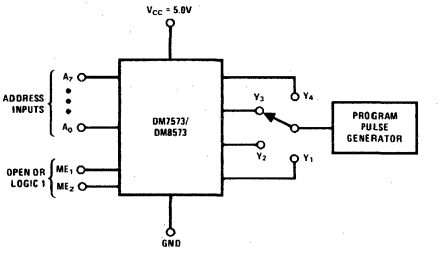
programming procedure

The DM7573/DM8573 is manufactured such that the outputs are high for all addresses. To program a logic zero (low output level), the following procedure should be followed:

1. Apply a V_{CC} voltage of 5.0V and select the word to be programmed using address inputs $A_7 - A_0$.
2. Apply a high level (logic 1) to either or both of the ENABLE inputs (Pins 13 and 14).
3. Apply a programming pulse to the output where a low level is desired. The voltage should be limited to 25V; the current should be limited to 70 mA. Apply the pulse as shown in the diagram. A reduction in current of approximately 15 mA indicates the bit is programmed.
4. To verify that the bit has been programmed, apply a logic zero to both of the enable inputs and check for a low level on the programmed output.
5. Advance to the next output and/or word, programming only one bit at a time.



Programming Pulse



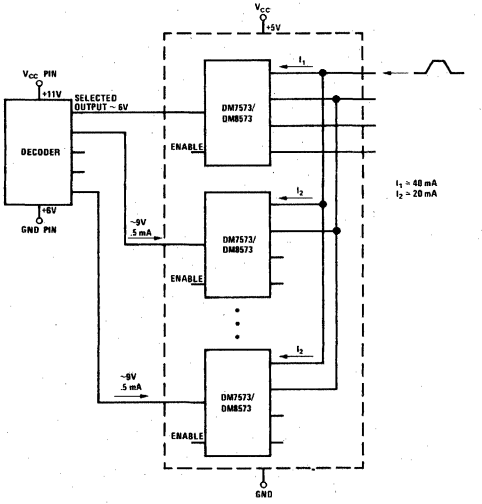
Programming Connections

board programming

The DM7573/DM8573 possesses added flexibility in that it can be programmed *after* it has already been connected in a system. Whether soldered to a printed circuit board or socketed, if the procedure described below is followed the units may be programmed even though their outputs are connected.

As shown in the diagram the decoder used to select the appropriate package must be operated at voltage levels which are 6 volts higher than normal. The outputs of the decoder therefore range between about 6V for a logical "0" and 9V for a logical "1". Because the decoder outputs are active-low, the ENABLE input of the device to be programmed is operated at 6V. The other ENABLE inputs reach 9V, normally a prohibited level, but in this case the circuit was designed to use the 9V to prevent the outputs from being programmed.

Although all common outputs receive the programming pulse, only the memory whose ENABLE input is at the 6V level is programmed.



NATIONAL

Bipolar PROMs

DM7574/DM8574 TRI-STATE® 1024-bit field-programmable read only memory

general description

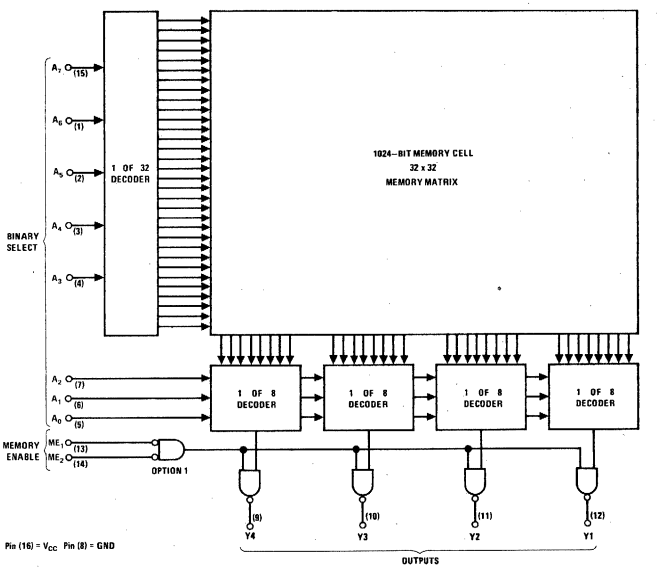
The DM7574/DM8574 is a field-programmable read-only memory organized as 256 four-bit words. Selection of the proper word is accomplished through the eight select inputs. Two overriding memory enable inputs are provided; when either or both of the enable inputs are taken to a high state, all the outputs go to the high impedance state. A logical "1" has been built into each bit location. A logical "0" can be programmed into any bit by selecting the proper word, disabling the chip, and applying a programming pulse to the proper output.

An additional feature of the DM7574/DM8574 is that its outputs can be tested in the logical "0" state without permanently programming the memory. In order to place all outputs in the logical "0" state, a 9V level is applied to the most significant address input, Pin 15. This feature will allow a much more complete test to be made before a part is shipped, thus minimizing customer returns.

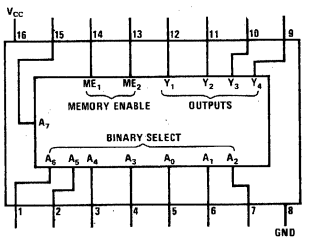
features

- Pin compatible with SN54187/SN74187
- Can be programmed after being connected in a system
- Outputs can be fully tested before programming
- Typical power dissipation 400 mW
- Propagation delay 60 ns

logic and connection diagrams



Dual-In-Line Package



Order Number DM7574D or DM8574D
See Package 3
Order Number DM8574N
See Package 15

absolute maximum ratings (Note 1)

Supply Voltage	7.0V
Input Voltage	5.5V (12V on Pins 13, 14)
Output Voltage	5.5V (25V for programming)
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DM7574	4.5	5.5	Volts
DM8574	4.75	5.25	Volts
Temperature (T_A)			
DM7574	−55	+125	°C
DM8574	0	70	°C

electrical characteristics (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	V_{CC} = Min	2.0			V
Logical "0" Input Voltage	V_{CC} = Min			0.8	V
Logical "1" Output Voltage	V_{CC} = Max, I_O = −2.0 mA	2.4			V
Logical "0" Output Voltage	V_{CC} = Min, I_O = 16 mA			0.4	V
High-Z Output Current	V_{CC} = Max, V_{OUT} = 2.4V, 0.4V			±40	μA
Logical "1" Input Current	V_{CC} = Max, V_{IN} = 2.4V V_{CC} = Max, V_{IN} = 5.5V			40 1	μA mA
Logical "0" Input Current	V_{CC} = Max, V_{IN} = 0.4V			−1	mA
Supply Current	V_{CC} = Max		82	110	mA
Input Clamp Voltage	V_{CC} = Min, I_{IN} = −12 mA			−1.5	V
Propagation Delay to a Logical "0" from Address to Output, t_{pd0}	V_{CC} = 5.0V T_A = 25°C		60	85	ns
Propagation Delay to a Logical "0" from Enable to Output, t_{pd0}	V_{CC} = 5.0V T_A = 25°C		28		ns
Propagation Delay to a Logical "1" from Address to Output, t_{pd1}	V_{CC} = 5.0V T_A = 2.5°C		60	85	ns
Propagation Delay to a Logical "1" from Enable to Output, t_{pd1}	V_{CC} = 5.0V T_A = 25°C		28		ns

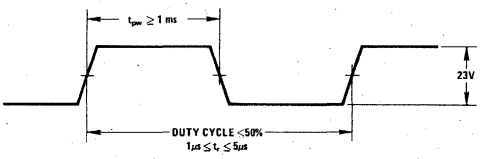
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55° to +125°C temperature range for the DM7574 and across the 0°C to 70°C range for the DM8574. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

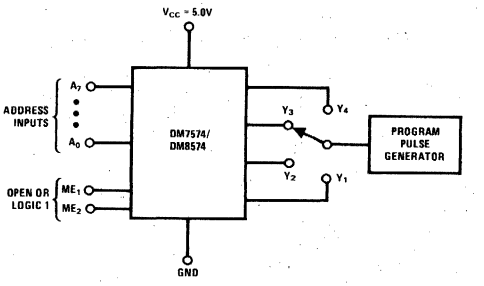
programming procedure

The DM7574/DM8574 is manufactured such that the outputs are high for all addresses. To program a logic zero (low output level), the following procedure should be followed:

1. Apply a V_{CC} voltage of 5.0V and select the word to be programmed using address inputs $A_7 - A_0$.
2. Apply a high level (logic 1) to either or both of the ENABLE inputs (Pins 13 and 14).
3. Apply a programming pulse to the output where a low level is desired. The voltage should be limited to 25V; the current should be limited to 70 mA. Apply the pulse as shown in the diagram. A reduction in current of approximately 15 mA indicates the bit is programmed.
4. To verify that the bit has been programmed, apply a logic zero to both of the enable inputs and check for a low level on the programmed output.
5. Advance to the next output and/or word, programming only one bit at a time.



Programming Pulse



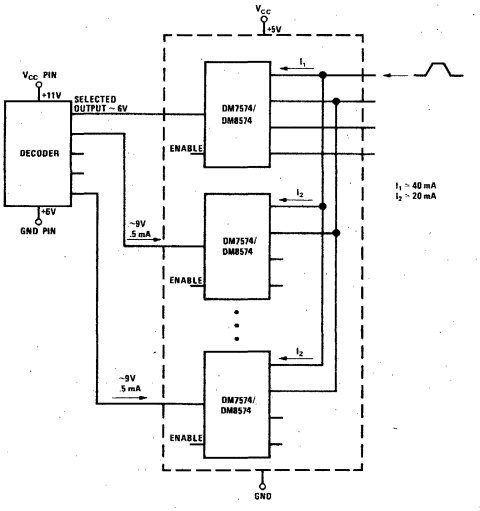
Programming Connections

board programming

The DM7574/DM8574 possesses added flexibility in that it can be programmed *after* it has already been connected in a system. Whether soldered to a printed circuit board or socketed, if the procedure described below is followed the units may be programmed even though their outputs are connected.

As shown in the diagram the decoder used to select the appropriate package must be operated at voltage levels which are 6 volts higher than normal. The outputs of the decoder therefore range between about 6V for a logical "0" and 9V for a logical "1". Because the decoder outputs are active-low, the ENABLE input of the device to be programmed is operated at 6V. The other ENABLE inputs reach 9V, normally a prohibited level, but in this case the circuit was designed to use the 9V to prevent the outputs from being programmed.

Although all common outputs receive the programming pulse, only the memory whose ENABLE input is at the 6V level is programmed.



Bipolar PROMs

DM7577/DM8577 256-bit programmable read only memory

general description

The DM7577/DM8577 is a field-programmable, 256-bit, read only memory organized as 32 words of 8 bits each. This monolithic, high-speed, transistor-transistor-logic (TTL) memory array is addressed in 5-bit binary with full on-chip decoding. An overriding memory-enable input is provided which, when taken high, will inhibit the function causing all eight outputs to remain high. The organization is expandable to 1,856 words of n-bits with no additional output buffering.

The address of an 8-bit word is accomplished through the buffered binary select inputs in coincidence with a low logic level at the enable input. Where multiple DM7577/DM8577 devices are used in a memory system, the enable input allows easy decoding of additional address bits.

Data can be electronically programmed, as desired, at any of the 256-bit locations of the DM7577/DM8577 in accordance with the programming procedure specified. Prior to programming, the memory contains a high-logic-level output condition at all 256 bit locations. The programming procedure open-circuits nichrome links which results in a low-logic-level output at selected locations. The procedure is irreversible and, once altered, the output for that bit is permanently programmed to provide a low logic level. Outputs never having been altered may later be programmed to supply a low-level output. Operation of the unit within the recommended operating conditions will not alter the memory content.

The mask-programmable DM5488/DM7488 can be used to replace the DM7577/DM8577 as they are functionally and mechanically identical.

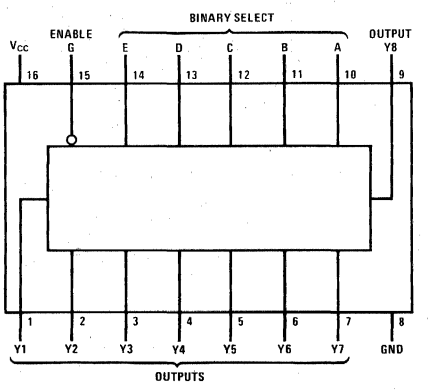
features

- Field programmable for custom or prototype memories
- Mask-programmable DM5488/DM7488 is a direct replacement for the DM7577/DM8577
- Typical access time 35 ns
- Organized as 32 words of 8-bits each
- Ideal for microprogramming and code converters
- Open-collector outputs are easily expanded
- Fully-decoded buffered inputs
- Fully compatible with most TTL and DTL circuits
- Pin compatible with SN74188A

5

connection diagram

Dual-In-Line Package



TOP VIEW

Order Number DM7577D
or DM8577D
See Package 3

Order Number DM8577N
See Package 15

absolute maximum ratings (Note 1)

Supply Voltage, V_{CC}	7.0V
Input Voltage	5.5V
Output Voltage	5.5V
Storage Temperature Range	−65°C to +150°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DM7577	4.5	5.5	V
DM8577	4.75	5.25	V
Temperature (T_A)			
DM7577	−55	+125	°C
DM8577	0	+70	°C
High-Level Output Voltage		5.5	V
Low-Level Output Current		12	mA

recommended conditions for programming

CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage, V_{CC}	5.0		5.5	V
Input Voltage				
Low Level	0		0.5	V
High Level	2.4		5.0	V
Programming Pulse Amplitude	20		22	V
Programming Pulse Rise Time	1.0	5.0	10	μs
Programming Pulse Current Limit	100		200	mA
Programming Pulse Width	10	20	50	ms
Case Temperature	25		75	°C

electrical characteristics V_{CC} = 5V, T_A = 25°C, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
High Level Input Voltage (V_{IH})		2			V
Low Level Input Voltage (V_{IL})				0.8	V
Input Clamp Voltage (V_I)	V_{CC} = Min, I_I = −12 mA			−1.5	V
High Level Output Current (I_{OH})	V_{CC} = Min, V_{IH} = 2V, V_{IL} = 0.8V, V_{OH} = 5.5V			100	μA
Low Level Output Voltage (V_{OL})	V_{CC} = Min, V_{IH} = 2V V_{IL} = 0.8V, I_{OL} = 12 mA			0.4	V
Input Current at Maximum Input Voltage (I_I)	V_{CC} = Max, V_I = 5.5V			1	mA
High Level Input Current (I_{IH})	V_{CC} = Max, V_I = 2.4V			40	μA
Low Level Input Current (I_{IL})	V_{CC} = Max, V_I = 0.4V			−1	mA
Supply Current, All Outputs High (I_{CCH})	V_{CC} = Max (Note 2)		50	80	mA
Supply Current, All Outputs Low (I_{CCL})	V_{CC} = Max (Note 3)		82	110	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: I_{CCH} is measured with all inputs at 4.5V, all outputs open.

Note 3: I_{CCL} is measured with enable input grounded, all other inputs at 4.5V, and all outputs open. The typical value shown is for the worst-case condition of all eight outputs low at one time. This condition may not be possible after the device has been programmed.

Note 4: For conditions shown as min or max, use the appropriate value specified under recommended operating conditions.

switching characteristics V_{CC} = 5V, T_A = 25°C

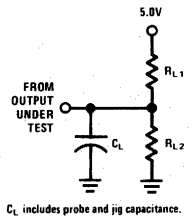
PARAMETER	FROM (INPUT)	TO (OUTPUT)	CONDITIONS	MIN	TYP	MAX	UNITS
Propagation Delay Time, Low to High Level Output (t_{PLH})	Enable	Any	C_L = 30 pF to GND, R_{L1} = 400Ω to V_{CC}, R_{L2} = 600Ω to GND		22	35	ns
Propagation Delay Time, High to Low Level Output (t_{PHL})	Enable	Any	C_L = 30 pF to GND, R_{L1} = 400Ω to V_{CC}, R_{L2} = 600Ω to GND		15	35	ns
Propagation Delay Time, Low to High Level Output (t_{PLH})	Select	Any	C_L = 30 pF to GND, R_{L1} = 400Ω to V_{CC}, R_{L2} = 600Ω to GND		35	50	ns
Propagation Delay Time, High to Low Level Output (t_{PHL})	Select	Any	C_L = 30 pF to GND, R_{L1} = 400Ω to V_{CC}, R_{L2} = 600Ω to GND		35	50	ns

programming procedure

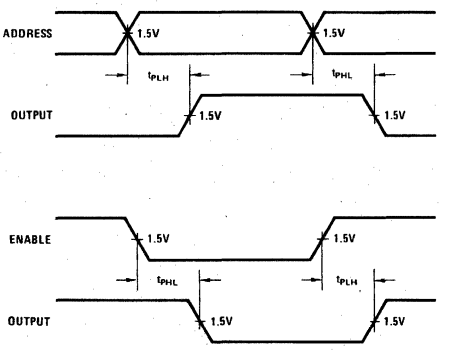
1. Apply steady-state supply voltage (V_{CC} = 5.0V, GND = 0V) and address the word to be programmed with specified input voltages.
2. Disable the outputs by applying a high logic level to the enable input.
3. Only one bit location is programmed at a time. Open circuit all outputs except the one to be programmed as a low logic level.
4. Apply the specified programming pulse to the output to be programmed. The recommended pulse width is 20 ms; however, 10 ms will program a high percentage of devices.

   The bit programmed may be verified by checking the output for a low logic level after the enable input reaches a low logic level.
5. Repeat steps 2 through 4 for each output of this address to be programmed as a low level.
6. Advance to next address location and repeat steps 2 through 5.

ac test circuit and switching time waveforms



C_L includes probe and jig capacitance.



Input waveforms are supplied by pulse generators having the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, PRR = 1 MHz, PDC = 50%, Amplitude = 3.0V, and Z_O = 50Ω.

NATIONAL

Bipolar PROMs

DM7578/DM8578 TRI-STATE® 256-bit programmable read only memory

general description

The DM7578/DM8578 is a field-programmable, 256-bit, read only memory organized as 32 words of 8 bits each. This monolithic, high-speed, transistor-transistor-logic (TTL) memory array is addressed in 5-bit binary with full on-chip decoding. An overriding memory-enable input is provided which, when taken high, will inhibit the function causing all eight outputs to remain in the high impedance (Z) state.

The address of an 8-bit word is accomplished through the buffered binary select inputs in coincidence with a low logic level at the enable input. Where multiple DM7578/DM8578 devices are used in a memory system, the enable input allows easy decoding of additional address bits. The TRI-STATE outputs eliminates the need for external pull-up resistors, and provides good capacitance drive capability.

Data can be electronically programmed, as desired, at any of the 256-bit locations of the DM7578/DM8578 in accordance with the programming procedure specified. Prior to programming, the memory contains a high-logic-level output condition at all 256 bit locations. The programming procedure open-circuits nichrome links which results in a low-logic-level output at selected locations.

The procedure is irreversible and, once altered, the output for that bit is permanently programmed to provide a low logic level. Outputs never having been altered may later be programmed to supply a low-level output. Operation of the unit within the recommended operating conditions will not alter the memory content.

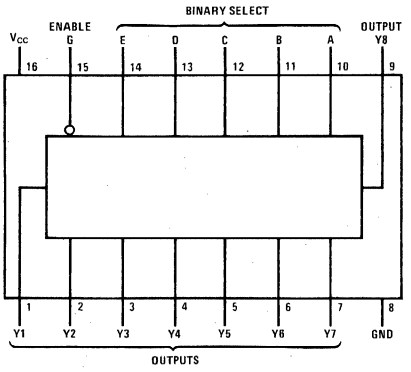
The mask-programmable DM7598/DM8598 can be used to replace the DM7578/DM8578 as they are functionally and mechanically identical.

features

- Field programmable for custom or prototype memories
- Mask-programmable DM7598/DM8598 is a direct replacement for the DM7578/DM8578.
- Typical access time 35 ns
- Organized as 32 words of 8-bits each
- Ideal for microprogramming and code converters
- TRI-STATE outputs are easily expanded
- Fully-decoded buffered inputs
- Fully compatible with most TTL and DTL circuits
- Pin compatible with SN74188A

connection diagram

Dual-In-Line Package



Order Number DM7578D or DM8578D
See Package 3
Order Number DM8578N
See Package 15

absolute maximum ratings (Note 1)

Supply Voltage, V_{CC}	7.0V
Input Voltage	5.5V
Output Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DM7578	4.5	5.5	V
DM8578	4.75	5.25	V
Temperature (T_A)			
DM7578	−55	+125	°C
DM8578	0	+70	°C
High-Level Output Voltage		5.5	V
Low-Level Output Current (I_{OL})		12	mA
High-Level Output Current (I_{OH})			
DM7578		−2.0	mA
DM8578		−5.2	mA

recommended conditions for programming

CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage (V_{CC})	5		5.5	V
Input Voltage				
Low Level	0		0.5	V
High Level	2.4		5	V
Programming Pulse Amplitude	20		22	V
Programming Pulse Rise Time	1	5	10	μs
Programming Pulse Current Limit	100		200	mA
Programming Pulse Width	10	20	50	ms
Case Temperature	25		75	°C

electrical characteristics (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
High Level Input Voltage (V_{IH})		2			V
Low Level Input Voltage (V_{IL})				0.8	V
Input Clamp Voltage (V_I)	V_{CC} = Min, I_I = −12 mA			−1.5	V
High Level Output Voltage (V_{OH})	V_{CC} = Min, V_{IH} = 2.0V, V_{IL} = 0.8V, I_{OH} = Max	2.4			V
Low Level Output Voltage (V_{OL})	V_{CC} = Min, V_{IH} = 2.0V, V_{IL} = 0.8V, I_{OL} = Max			0.4	V
Off State (High Impedance State) Output Current ($I_{O(OFF)}$)	V_{CC} = Max, V_{IH} = 2.0V, V_O = 2.4V			40	μA
	V_O = 0.5V			−40	μA
Input Current at Maximum Input Voltage (I_I)	V_{CC} = Max, V_I = 5.5V			1	mA
High Level Input Current (I_{IH})	V_{CC} = Max, V_I = 2.4V			40	μA
Low Level Input Current (I_{IL})	V_{CC} = Max, V_I = 0.4V			−1	mA
Short Circuit Output Current (I_{OS}) (Note 3)	V_{CC} = Max	−30		−70	mA
Supply Current (I_{CC})	V_{CC} = Max (Note 4)		82	110	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for DM7578 and across the 0°C to +70°C range for the DM8578. All typicals are given for V_{CC} = 5.0V and T_A = +25°C.

Note 3: Duration of the short-circuit should not exceed one second. Only one output at a time should be shorted.

Note 4: I_{CC} is measured with all inputs at 4.5V, all outputs open.

switching characteristics V_{CC} = 5V, T_A = 25°C

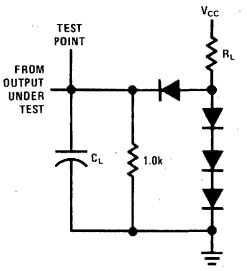
PARAMETER	FROM (INPUT)	TO (OUTPUT)	CONDITIONS	MIN	TYP	MAX	UNITS
Propagation Delay Time, Low to High Level Output (t_{PLH})	Select	Any	R_L = 400Ω, C_L = 50 pF		35	50	ns
Propagation Delay Time High to Low Level Output (t_{PHL})	Select	Any	R_L = 400Ω, C_L = 50 pF		35	50	ns
Output Enable Time to High Level (t_{ZH})	Enable	Any	R_L = 400Ω, C_L = 50 pF		19	35	ns
Output Enable Time to Low Level (t_{ZL})	Enable	Any	R_L = 400Ω, C_L = 50 pF		17	35	ns
Output Disable Time from High Level (t_{HZ})	Enable	Any	R_L = 400Ω, C_L = 5 pF		11	35	ns
Output Disable Time from Low Level (t_{LZ})	Enable	Any	R_L = 400Ω, C_L = 5 pF		21	35	ns

programming procedure

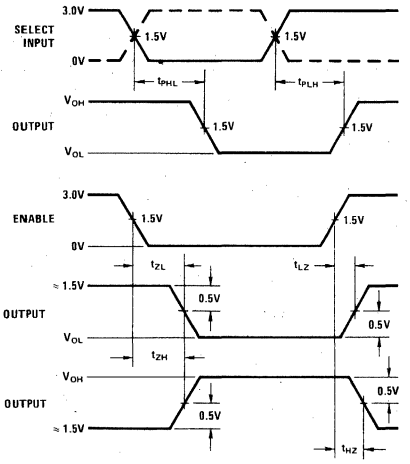
1. Apply steady-state supply voltage (V_{CC} = 5.0V, GND = 0V) and address the word to be programmed with specified input voltages.
2. Disable the outputs by applying a high logic level to the enable input.
3. Only one bit location is programmed at a time. Open circuit all outputs except the one to be programmed as a low logic level.
4. Apply the specified programming pulse to the output to be programmed. The recommended pulse width is 20 ms; however, 10 ms will program a high percentage of devices.

   The bit programmed may be verified by checking the output for a low logic level after the enable input reaches a low logic level.
5. Repeat steps 2 through 4 for each output of this address to be programmed as a low level.
6. Advance to next address location and repeat steps 2 through 5.

ac test circuit and switching time waveforms



C_L includes probe and jig capacitance.
All diodes are 1N3064.



Input waveforms are supplied by pulse generators having the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, PRR = 1 MHz, PDC = 50%, Amplitude = 3.0V, and Z_O = 50Ω.

NATIONAL

Bipolar PROMs
Advance Information

DM75S222/DM85S222 TRI-STATE® 2048-bit PROM with output latches

general description

These TTL compatible memories are organized as 256 words by 8 bits. When the strobe input is at a logical "1" level the memories function in the conventional manner with the enable input determining whether the outputs present the contents selected by the address inputs or are turned "OFF."

When the strobe input is at a logical "0" the outputs are latched into the state they were in just prior to the strobe going low. The outputs remain in this condition until the strobe is again taken to the logical "1" state regardless of the state of the address or enable inputs.

PROMs are shipped from the factory with a logical "0" in all locations. A logical "1" may be programmed into any selected locations by following the programming instructions. Once programmed, it is impossible to go back to a logical "0." Additional bits may be programmed to a logical "1," however.

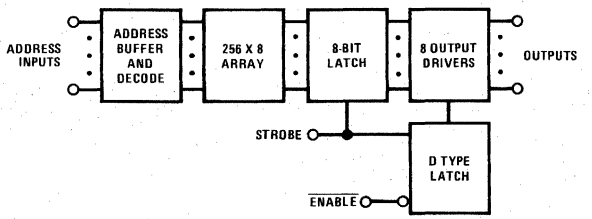
features

- Schottky clamped for high speed systems
- High speed

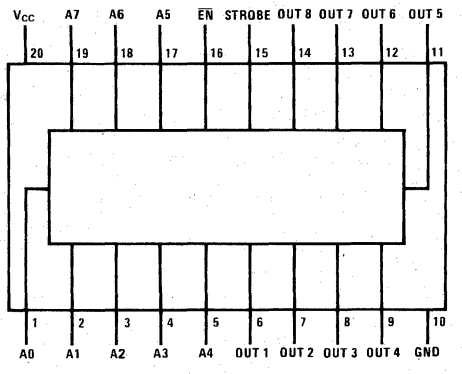
Address to output delay—typical	35 ns
Enable to output delay—typical	15 ns
Strobe to output delay—typical	20 ns

- PNP inputs reduce input loading
- Output latches simplify system use
- 20 pin, 300 mil package for high density
- All dc and switching characteristics may be measured prior to programming PROMs
- Pin compatible with DM54S271/DM54S371

logic and connection diagrams



Dual-In-Line Package



TOP VIEW

Order Number DM85S222N
See Package 16A

absolute maximum ratings (Note 1)

Supply Voltage (Note 2)	−0.5V to +7.0V
Input Voltage (Note 2)	−1.2V to +5.5V
Output Voltage (Note 2)	−0.5V to +5.5V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering,10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DM75S222	4.5	5.5	V
DM85S222	4.75	5.25	V
Ambient Temperature (T_A)			
DM75S222	−55	+125	°C
DM85S222	0	+70	°C
Logical "0" Input Voltage	0	0.8	V
Logical "1" Input Voltage	2.0	5.5	V

dc electrical characteristics (Note 3)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
I_{IH}	Logical "1" Input Current	V_{IN} = 2.7V			25	μA
		V_{IN} = 5.5V			1.0	mA
I_{IL}	Logical "0" Input Current	V_{IN} = 0.45V			−250	μA
V_{CL}	Input Clamp Voltage	I_{IN} = −18 mA			−1.2	V
V_{OL}	Logical "0" Output Voltage					
	DM75S222	I_{OL} = 12 mA			0.50	V
	DM85S222				0.45	V
V_{OH}	Logical "1" Output Voltage					
	DM75S222	I_{OH} = −2.0 mA	2.4			V
	DM85S222	I_{OH} = −6.5 mA	2.4			V
I_{OS}	Output Short Circuit Current	V_O = 0V (Note 4), V_{CC} = Max	−30		−100	mA
I_{OZ}	TRI-STATE Output Current	0.45V ≤ V_O ≤ 2.4V	−50		50	μA
I_{CC}	Maximum Supply Current			100	165	mA

switching characteristics (Note 3)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{AA}	Address to Output Delay	Strobe = "1"		35		ns
t_{EA}	Time to Enable Output	Strobe = "1"		15		ns
t_{ED}	Time to Disable Output	Strobe = "1"		15		ns
t_{SA}	Strobe to Output Delay			20		ns
t_{SW}	Strobe Pulse Width			10		ns

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at these limits.

Note 2: These limits do not apply to PROMs during programming. For the absolute maximum ratings, refer to the programming instructions.

Note 3: These limits apply over the entire operating range unless stated otherwise. All typical values are for V_{CC} = 5.0V and T_A = 25°C.

Note 4: During I_{OS} measurement, only one output at a time should be grounded. Permanent damage may otherwise result.

MOS ROMs

MM3501 1024-bit read-only memory

general description

The MM3501 is a 1024-bit read-only memory programmed in a 128 word by 8 bit format. It is an MOS monolithic integrated circuit utilizing P-channel enhancement mode technology. The fixed program memory is specified by the customer and customized by modifying one mask in the fabrication process. This results in a fast turn-around, low cost custom memory.

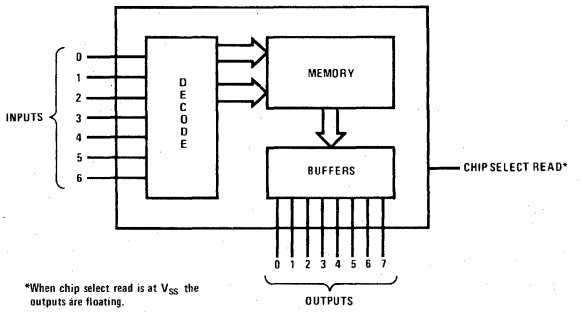
features

- Chip select
- 1.5 μs typical access time
- 115 mW typical static operation
- Low power consumption
- Bipolar compatible outputs

applications

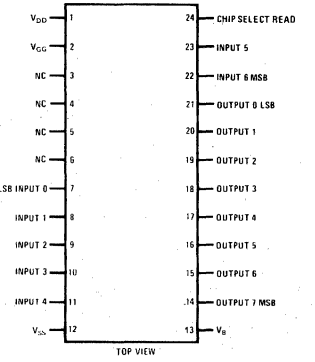
- Microprogramming
- Code conversion
- Table lookup
- Control logic

logic and connection diagrams



*When chip select read is at V_{SS} the outputs are floating.

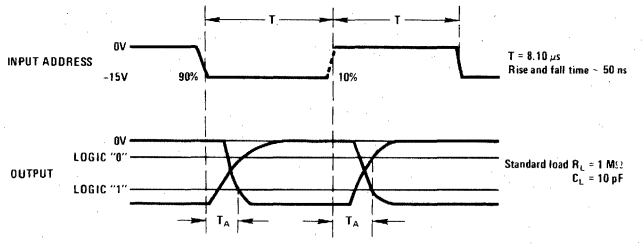
Dual-In-Line Package



Order Number MM3501J
See Package 11
Order Number MM3501N
See Package 18

switching time waveforms

Access and Chip Select Times



Note: The logic "0," "1" levels may be taken to be (−1.0V, −10V) or (−2.0V, −9.0V) respectively. Guaranteed limits are at −1.0V and −10V.

Note: For programming information see AN-100.

absolute maximum ratings

All Voltages and Data Input Lines with Respect to V_{SS}	−30V to +0.3V
Power Dissipation	250 mW
Storage Temperature Range	−65°C to +125°C
Operating Temperature Range	0°C to +70°C
Lead Temperature (soldering, 10 sec.)	300°C

electrical characteristics

T_A within operating temperature range $V_{DD} = -13V \pm 1.0V$, $V_{GG} = -27V \pm 2.0V$, $V_B = -27V \pm 2.0V$, $V_{SS} = 0V$ (GND), unless otherwise noted.

CHARACTERISTIC	CONDITIONS	MIN	TYP	MAX	UNITS
Input Logic Levels					
Logic "0"		$V_{SS}-2.0$		V_{SS}	V
Logic "1"				$V_{SS}-9.0$	V
Input Capacitance	(Note 4)		7.0	15	pF
Input Leakage	$V_{IN} = -15V$ (Note 5)			1.0	μA
Output Logic Levels					
Logic "0"	$I_L = -10\mu A$	$V_{SS}-1.0$		V_{SS}	V
Logic "1"	$I_L = +10\mu A$			$V_{SS}-10$	V
Access Time (T_A)	$R_L = 1.0\ M\Omega$, $C_L = 10$ pF (Notes 2 and 3, See Waveform)		1.5	4.0	μs
Output Current					
Logic "1"	$V_{OUT} = -4.6V$ (Forced) ($V_B = V_{DD}$)	1.6			mA
Logic "0"	$V_{OUT} = -1.0V$ (Forced) (Note 6)	−0.15	−0.24		mA
Logic "1"	$V_{OUT} = -10V$ (Forced) (Note 6)	0.30	0.85		mA
Supply Current Drain					
I_{DD}	$V_{DD} = -14V$, $V_{GG} = -29V$			6.5	mA
I_{GG}	(Note 2)			4.0	mA
Power Consumption	(Notes 1 and 2)		115	215	mW

Note 1: Exclusive of I_B (load current)
Note 2: $T_A = +25°C$.
Note 3: Sample tested.
Note 4: Guaranteed by design.
Note 5: Address and chip select inputs all pins grounded except the one under test
Note 6: $V_{DD} = -12V$, $V_{GG} = -25V$ (worst case condition of measurement)

MOS ROMs

MM4210/MM5210 1024-bit read only memory

general description

The MM4210/MM5210 is a 1024-bit static read only memory. It is a P-channel enhancement mode monolithic MOS integrated circuit utilizing low threshold technology. The device is a non-volatile memory organized as 256-4 bit words. Programming of the memory contents is accomplished by changing one mask during device fabrication. Customer programs may be supplied in a tape, card, or pattern selection format.

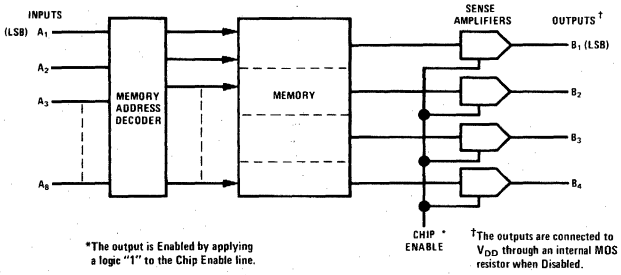
features

- Bipolar compatibility
- High speed operation — 500 ns typ
- Static operation — no clocks required
- Common data busing — output wire AND capability
- Chip enable output control.

applications

- Code conversion
- Random logic synthesis
- Table look-up
- Character generators
- Microprogramming.

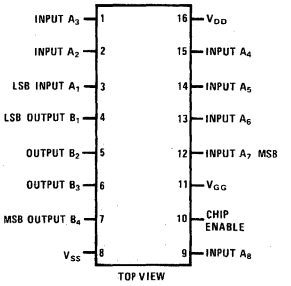
block and connection diagrams



*The output is Enabled by applying a logic "1" to the Chip Enable line.

†The outputs are connected to V_{DD} through an internal MOS resistor when Disabled.

Dual-In-Line Package

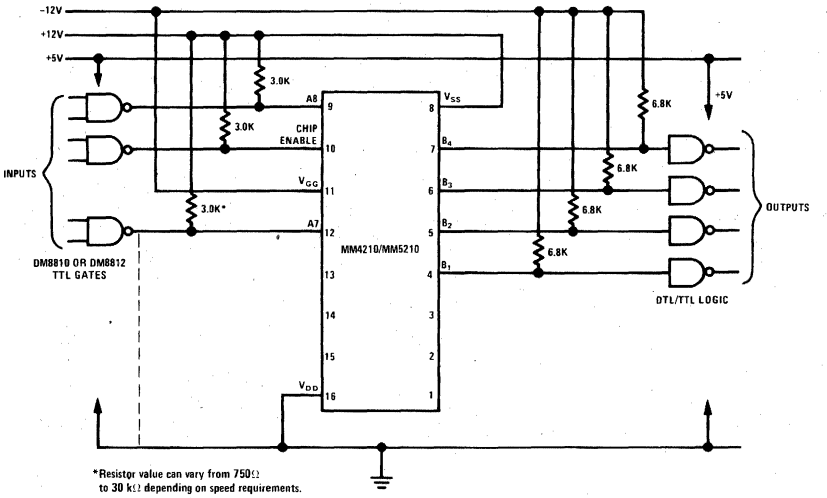


Order Number MM4210J or MM5210J
See Package 10

Order Number MM5210N
See Package 15

typical application

256 x 4 Bit ROM Showing TTL Interface



*Resistor value can vary from 750Ω to 30 kΩ depending on speed requirements.

Note: For programming information see AN-100.

6

absolute maximum ratings

V_{GG} Supply Voltage		$V_{SS}-30V$
V_{DD} Supply Voltage		$V_{SS}-15V$
Input Voltage		$(V_{SS}-20)V < V_{IN} < (V_{SS}+0.3)$
Storage Temperature		$-65°C$ to $+150°C$
Operating Temperature	MM4210	$-55°C$ to $+125°C$
	MM5210	$0°C$ to $+70°C$
Lead Temperature (Soldering, 10 sec)		$300°C$

electrical characteristics

T_A within operating temperature range, $V_{SS} = +12V \pm 5\%$ and $V_{GG} = -12V \pm 5\%$, unless otherwise specified.

PARAMETER	CONDITION	MIN	TYP	MAX	UNITS
Output Voltage Levels					
MOS to MOS					
Logical "1"	1 MΩ to GND Load			$V_{SS}-9.0$	V
Logical "0"		$V_{SS}-1.0$			V
MOS to TTL					
Logical "1"	6.8 kΩ to V_{GG} Plus One			+0.4	V
Logical "0"	Standard Series 54/74 Gate Input	+2.4			V
Input Voltage Levels					
Logical "1"				$V_{SS}-8.0$	V
Logical "0"		$V_{SS}-2.0$			V
Power Supply Current	$T_A = 25°C$				
V_{SS}			19	25	mA
V_{GG} (Note 1)				1	μA
Input Leakage	$V_{IN} = V_{SS}-12V$			1	μA
Input Capacitance	f = 1.0 MHz $V_{IN} = 0V$		5		pF
Access Time (Notes 2, 3)	$T_A = 25°C$				
T_{ACCESS}	(See Timing Diagram) $V_{SS} = +12V$ $V_{GG} = -12V$	150	500	650	ns
Output AND Connection	MOS Load			3	
	TTL Load			8	

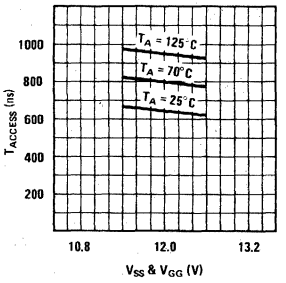
Note 1: The V_{GG} supply may be clocked to reduce device power without affecting access time.

Note 2: Address time is measured from the change of data on any input or Chip Enable line to the output of a TTL gate. See Timing Diagram.

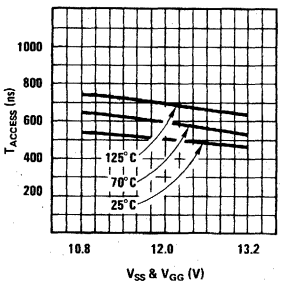
Note 3: The access time in the TTL load configuration follows the equation: T_{ACCESS} = the specified time + (N − 1) (50) ns where N = number of AND connections.

performance characteristics

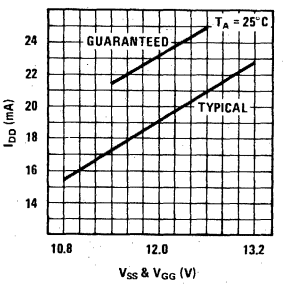
Guaranteed Access Time vs Supply Voltages



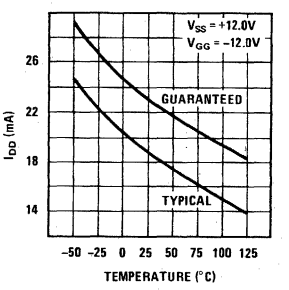
Typical Access Time vs Supply Voltages



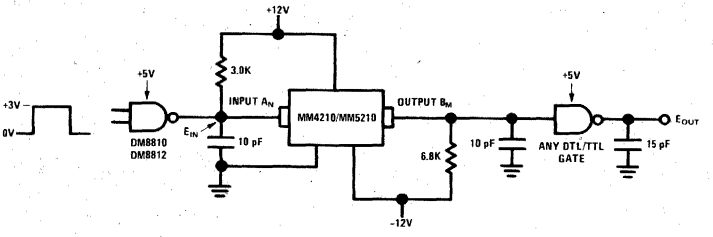
Power Supply Current vs Voltage

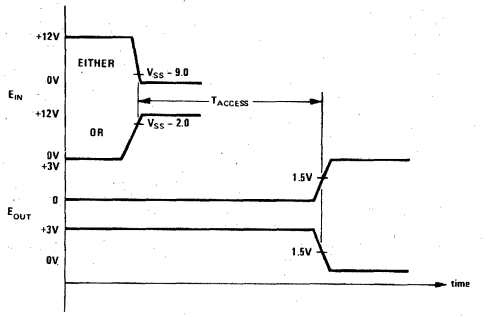


Power Supply Current vs Temperature



timing diagram/address time





NATIONAL

MOS ROMs

MM4211/MM5211 1024-bit read only memory

general description

The MM4211/MM5211 is a 1024-bit static read only memory. It is a P-channel enhancement mode monolithic MOS integrated circuit utilizing low threshold technology. The device is a non-volatile memory organized as 256-4 bit words. Programming of the memory contents is accomplished by changing one mask during device fabrication.

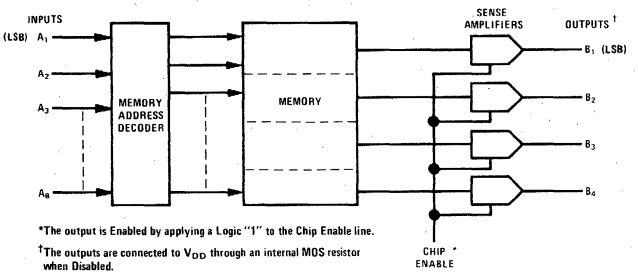
features

- Bipolar compatibility +5V, −12V operation
- High speed operation < 700 ns typ
- Static operation no clocks required
- Common data busing output wire AND capability
- Chip enable output control

applications

- Code conversion
- Random logic synthesis
- Table look-up
- Character generators
- Microprogramming

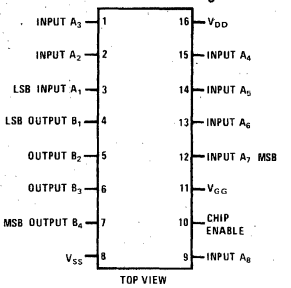
block and connection diagrams



*The output is Enabled by applying a Logic "1" to the Chip Enable line.

†The outputs are connected to V_{DD} through an internal MOS resistor when Disabled.

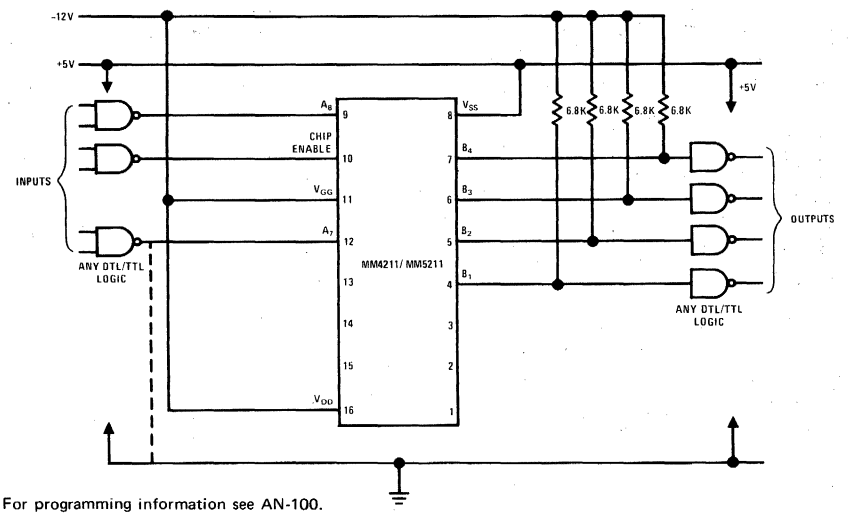
Dual-In-Line Package



Order Number MM4211J or MM5211J
See Package 10
Order Number MM5211N
See Package 15

typical application

256 x 4 Bit ROM Showing TTL Interface



Note: For programming information see AN-100.

absolute maximum ratings

V_{GG} Supply Voltage	V_{SS} – 20V
V_{DD} Supply Voltage	V_{SS} – 20V
Input Voltage	$(V_{SS} - 20)V < V_{IN} < (V_{SS} + 0.3)V$
Storage Temperature	–65°C to +150°C
Operating Temperature MM4211	–55°C to +125°C
MM5211	0°C to +70°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics

T_A within operating temperature range, V_{SS} = +5V ±5%, V_{GG} = V_{DD} = –12V ±5%, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage Levels					
MOS to TTL					
Logical "1"	6.8K ±5% to V_{GG} Plus One			+0.4	V
Logical "0"	Standard Series 54/74 Gate	+2.4			V
Output Current Capability					
Logical "0"	V_{OUT} = 2.4V	2.5			mA
Input Voltage Levels					
Logical "1"				V_{SS} – 4.2	V
Logical "0"		V_{SS} – 2.0			V
Power Supply Current	T_A = 25°C				
I_{DD}	V_{SS} = +5V		6.5	12.0	mA
I_{GG} (Note 1)	V_{GG} = V_{DD} = –12V			1	μA
Input Leakage	V_{IN} = V_{SS} – 12V			1	μA
Input Capacitance (Note 4)	f = 1.0 MHz, V_{IN} = 0V		5		pF
V_{GG} Capacitance (Note 4)	f = 1.0 MHz, V_{IN} = 0V		15	25	pF
Address Time (Note 2)	See Timing Diagram				
T_{ACCESS}	T_A = 25°C, V_{SS} = 5V, V_{GG} = V_{DD} = –12V		700	950	ns
Output AND Connection (Note 3)	6.8K ±5% to V_{GG} Plus One Standard Series 54/74 Gate			8	

Note 1: The V_{GG} supply may be clocked to reduce device power without affecting access time.

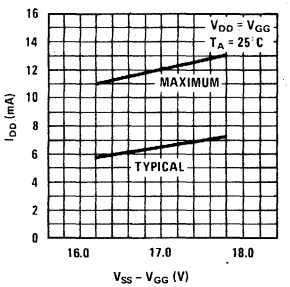
Note 2: Address time is measured from the change of data on any input or Chip Enable line to the output of a TTL gate. (See Timing Diagram.) See curves for guaranteed limit over temperature.

Note 3: The address time in the TTL load configuration follows the equation:
T_{ACCESS} = The specified limit + (N –1) (50) ns
Where N = Number of AND connections.

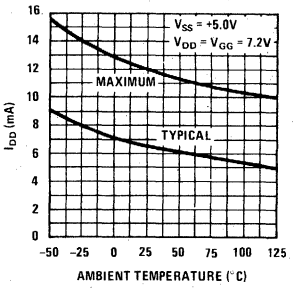
Note 4: Capacitance guaranteed by design.

performance characteristics

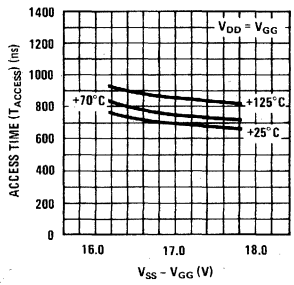
Power Supply Current vs
Power Supply Voltages



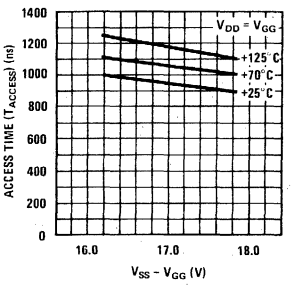
Power Supply Current vs
Ambient Temperature



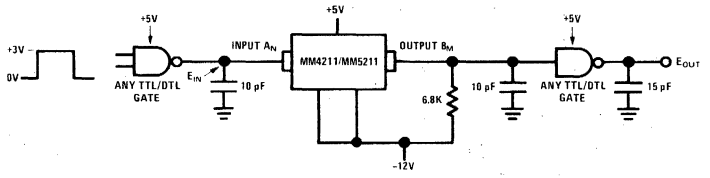
Typical Access Time vs
Power Supply Voltages

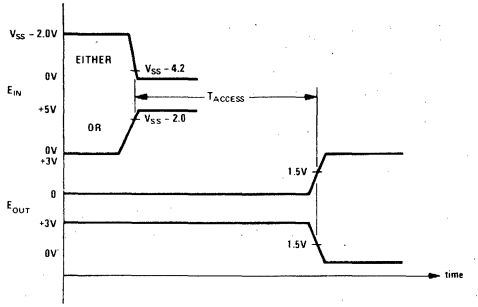


Guaranteed Access Time vs
Power Supply Voltages



timing diagram/address time





MOS ROMs

MM5212 12,288-bit read only memory

general description

The MM5212 12,288-bit read only memory is a P-channel enhancement mode monolithic MOS integrated circuit utilizing a low threshold voltage technology and ion-implanted resistors. Open drain outputs provide a TTL compatible wire OR capability with the addition of a 6.8 kΩ resistor. The ROM is organized in a 1024 word by 12-bit organization.

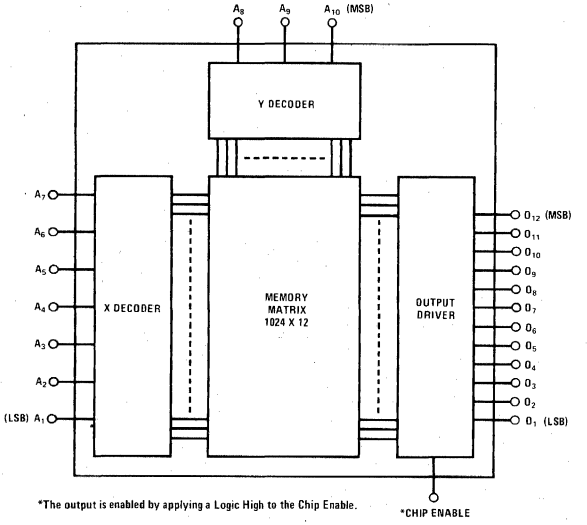
features

- Standard supplies +5.0V, −12V
- Open drain outputs Wire OR capability
- Static operation No clocks
- TTL compatible inputs and outputs

applications

- Character generator
- Random logic synthesis
- Microprogramming
- Table look-up

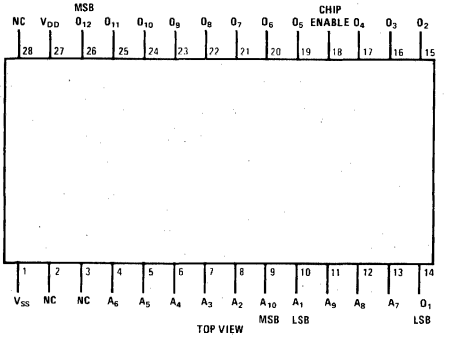
schematic diagram



*The output is enabled by applying a Logic High to the Chip Enable.

connection diagram

Dual-In-Line Package



Note: For programming information see AN-100.

Order Number MM5212AD
See Package 7

Order Number MM5212AN
See Package 19

absolute maximum ratings

Voltage at Any Pin	V_{SS} + 0.5V to V_{SS} − 22V
Power Dissipation at 25°C Ambient	800 mW
Operating Temperature	0°C to +70°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

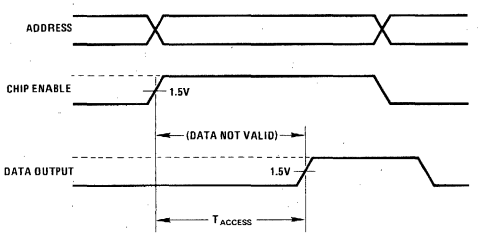
electrical characteristics

T_A within operating temperature range, V_{SS} = +5.0V ±5%, V_{DD} = −12V ±5%, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Data Input Levels (Note 1)					
Logical High Level (V_{IH})		+2.8			V
Logical Low Level (V_{IL})				+0.8	V
Data Output Levels (Note 1)					
Logical High Level (V_{OH})	6.8 kΩ ±5% to V_{DD} Plus One	+2.4			V
Logical Low Level (V_{OL})	Standard Series 54/74 Gate			+0.4	V
Output Current Capability					
Logical High Level (V_{IH})	V_{OUT} = 2.4V	2.5			mA
Power Supply Current	T_A = 25°C, V_{SS} = +5.0V				
I_{DD}	V_{DD} = −12V		6.0	10.0	mA
Standby Power Dissipation	V_{SS} = +5.0V, V_{DD} = −12V Chip Enable LOW			170.0	mW
Input Leakage	V_{IN} = V_{SS} −10V			1.0	μA
Address Time	See Timing Diagram				
T_{ACCESS}	T_A = 25°C, V_{SS} = +5.0V V_{DD} = −12V		3.5	5.0	μs

Note 1: Positive logic definition.

switching time waveforms



MOS ROMs

MM4213/MM5213 2048-bit read only memory

general description

The MM4213/MM5213 is a 2048-bit static read only memory. It is a P-channel enhancement mode monolithic MOS integrated circuit utilizing low threshold voltage technology. The device is a non-volatile memory organized as a 256-8 bit words or 512-4 bit words. Programming of the memory contents is accomplished by changing one mask during the device fabrication.

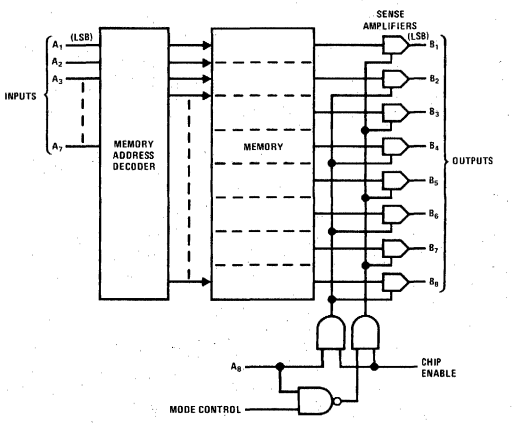
features

- Bipolar compatibility — +5V, −12V operation
- High speed operation — 600 ns typ
- Pin compatible with MM5203 pROM
- Static operation — No clocks required
- Common data busing — Output wire AND capability
- Chip enable output control
- TRI-STATE output

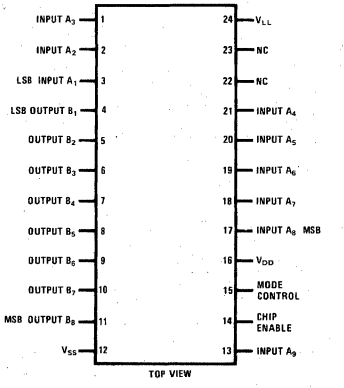
applications

- Code conversion
- Random logic synthesis
- Table look-up
- Character generator
- Microprogramming

block and connection diagrams



Dual-In-Line Package



Order Number MM4213J
or MM5213J
See Package 11

Order Number MM5213N
See Package 18

Note: For programming information see AN-100.

absolute maximum ratings

V_{LL} Supply Voltage	V_{SS} – 20V
V_{DD} Supply Voltage	V_{SS} – 20V
Input Voltage	$(V_{SS} - 20)\ V < V_{IN} < (V_{SS} + 0.3)\ V$
Storage Temperature	–65°C to +150°C
Operating Temperature MM4213	–55°C to +125°C
MM5213	0°C to +70°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output Current Capability					
Logical "1"	V_{OUT} = 2.4V	200			μA
Logical "0"	V_{OUT} = 0.4V	–1.6			mA
Input Voltage Levels					
Logical "0"				V_{SS} – 4.0	V
Logical "1"		V_{SS} – 2.0			V
Power Supply Current	T_A = 25°C				
I_{SS} (Note 2)	V_{SS} = +5V, V_{LL} = V_{DD} = –12V		20	35	mA
Input Leakage	V_{IN} = –12V			1	μA
Input Capacitance (Note 5)	f = 1.0 MHz, V_{IN} = 0V		5		pF
Address Time					
T_{ACCESS}	T_A = 25°C, V_{SS} = +5.0V, V_{GG} – V_{DD} = –12.0V		600	850	ns
Output AND Connections (Note 4)				10	

Note 1: These specifications apply for V_{SS} = +5.0V ±5%, V_{LL} = –12V, and T_A = –55°C to +125°C (MM4213), T_A = –25°C to +70°C (MM5213) unless otherwise specified.

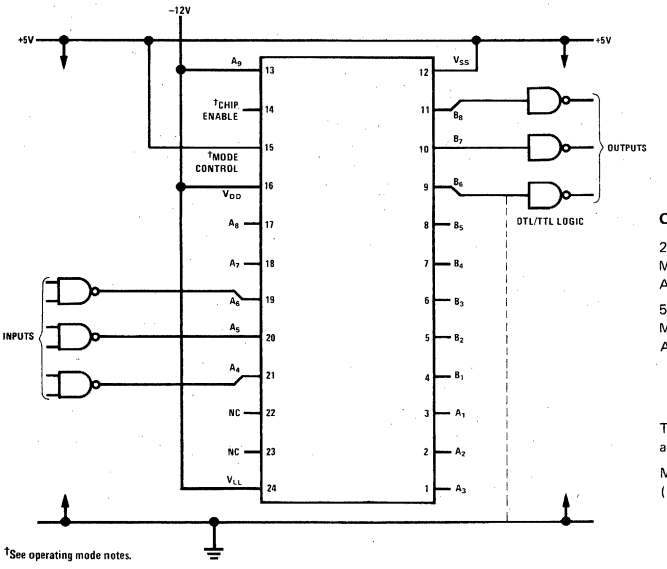
Note 2: Outputs open.

Note 3: Address time is measured from the change of data on any input or Chip Enable line to the output of a TTL gate.

Note 4: The address time in the TTL load configuration follows the equation: T_{ACCESS} = The specified limit + (N – 1) (25) ns. Where N = Number of AND connections.

Note 5: Capacitances are measured on a lot sample basis only.

typical applications (con't)



†See operating mode notes.

Operating Modes

256x8 ROM connection (shown)
Mode Control – Logic "1"
A_9 – Logic "0"

512x4 ROM connection
Mode Control – Logic "0"
A_9 – Logic "1" Enables the odd (B_1, B_3 . . . B_9) outputs
– Logic "0" Enables the even (B_2, B_4 . . . B_8) outputs.

The outputs are "Enabled" when a logic "0" is applied to the Chip Enable line.

Mode Control should be "hard wired" to V_{LL} (Logical "1") or V_{SS} (Logical "0").

NATIONAL

MOS ROMs

MM4214/MM5214 4096-bit static read only memory

general description

The MM4214/MM5214 4096-bit static read only memory is a P-channel enhancement mode monolithic MOS integrated circuit utilizing a low threshold voltage technology to achieve bipolar compatibility. TRI-STATE® outputs provide wire ORed capability without loading common data lines or reducing system access times. The ROM is organized in a 512 word x 8-bit memory organization.

Customer programs may be submitted for production in a paper tape or punched card format.

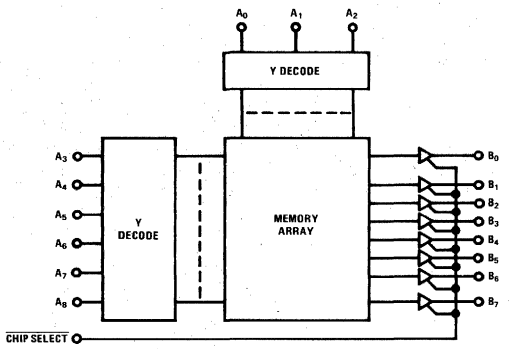
features

- Pin compatible with MM5204 PROM
- Bipolar compatibility — No external components required
- Standard supplies — +5.0V, −12V
- Bus ORable output — TRI-STATE outputs
- Static operation — No clocks required

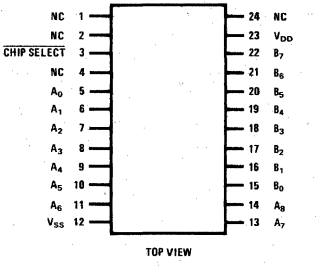
applications

- Character generator
- Random logic synthesis
- Microprogramming
- Table look-up

logic and connection diagrams



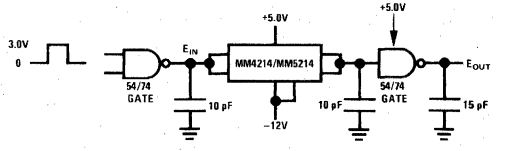
Dual-In-Line Package

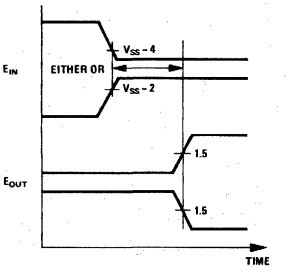


Order Number MM4214J or MM5214J
See Package 11

Order Number MM5214N
See Package 18

timing diagram/address time





Note: For programming information see AN-100.

absolute maximum ratings

V_{DD} Supply Voltage	V_{SS} − 20V	Operating Temperature Range	
Input Voltage	$(V_{SS} - 20)\ V < V_{IN} < (V_{SS} + 0.03)\ V$	MM4214	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C	MM5214	−25°C to +70°C
		Lead Temperature (Soldering, 10 seconds)	300°C

electrical characteristics

T_A within operating temperature range, V_{SS} = +5.0V ±5%, V_{DD} = −12V ±5%, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage Levels					
Logical Low Level (V_{IL})	I_L = 1.6 mA Sink			0.4	V
Logical High Level (V_{IH})	I_L = 100μA Source	2.4			V
Input Voltage Levels					
Logical Low Level (V_L)				V_{SS}−4.0	V
Logical High Level (V_H)		V_{SS}−2.0			V
Power Supply Current (I_{SS}) (Note 4)	V_{SS} = 5.0V, V_{DD} = −12V, T_A = 25°C		23	37	mA
Input Leakage	$V_{IN} = V_{SS} - 10V$			1.0	μA
Input Capacitance (Note 2)	f = 1.0 MHz, V_{IN} = 0V		5.0	10	pF
Output Capacitance (Note 2)	f = 1.0 MHz, V_{IN} = 0V		4.0	10	pF
Address Time (T_{ACCESS}) (Note 1)	V_{DD} = −12V, V_{SS} = 5.0V, T_A = 25°C	150		1000	ns
Output AND Connections (Note 3)				20	

Note 1: Capacitances are measured periodically only.

Note 2: Address is measured from the change of data on any input or chip enable line to the output of a TTL gate. (See Timing Diagram.)

Note 3: The address time follows the following equation: T_{ACCESS} = The specified limit + (N−1) x 25 ns where N = Number of AND connections.

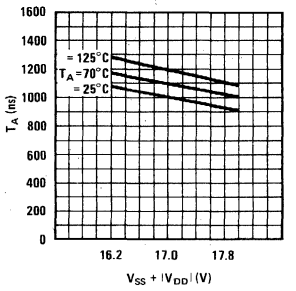
Note 4: Outputs open.

Note 5: Positive true logic notation is used. Logic "1" = most positive voltage level. Logic "0" = most negative voltage level.

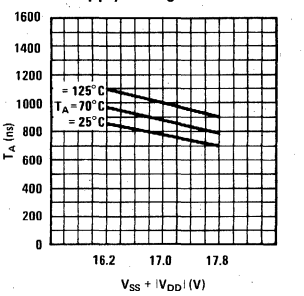
Note 6: Chip is enabled when Chip Select is low.

typical performance characteristics

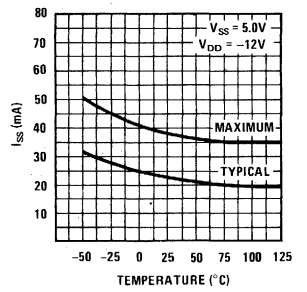
Guaranteed Access Time vs Supply Voltage



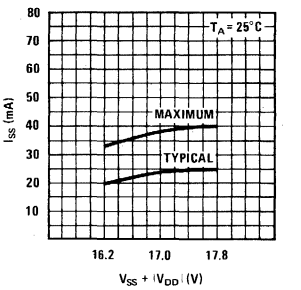
Typical Access Time vs Supply Voltage



Power Supply Current vs Temperature



Power Supply Current vs Voltage



MOS ROMs

MM5215 12,288-bit read only memory

general description

The MM5215 12,288-bit static read only memory is a P-channel enhancement mode monolithic MOS integrated circuit utilizing low threshold voltage technology and ion-implanted resistors. TRI-STATE® outputs provide wire-OR capability without loading common data lines or reducing system access times. The ROM is organized in a 1024 x 12 bit word configuration. The V_{GG} supply may be brought to 0V to reduce internal power dissipation in the non-enabled mode to 10μW/bit.

Customer programs may be submitted on Hollerith coded punched cards.

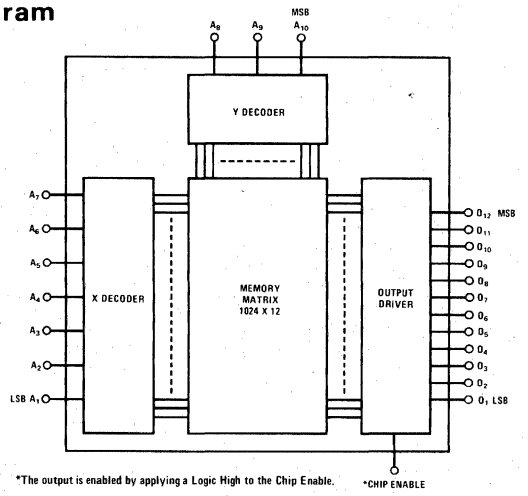
features

- Static operation
- TRI-STATE outputs
- No clocks required
- +12V and −12V supplies
- Pin compatible with E.A. 3800

applications

- Character generator
- Random logic synthesis
- Microprogramming
- Table look-up

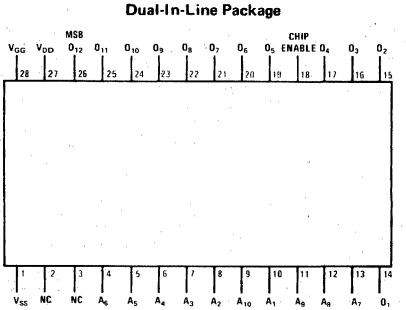
schematic diagram



*The output is enabled by applying a Logic High to the Chip Enable.

connection diagram

Dual-In-Line Package



Note: For programming information see AN-100.

Order Number MM5215AD
See Package 7

Order Number MM5215AN
See Package 19

absolute maximum ratings

V_{GG} Supply Voltage	V_{SS} +0.5V to V_{SS} −30V
Input Voltage	V_{SS} +0 5V to V_{SS} −30V
Power Dissipation at 25°C Ambient	800 mW
Operating Temperature	0°C to +70°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

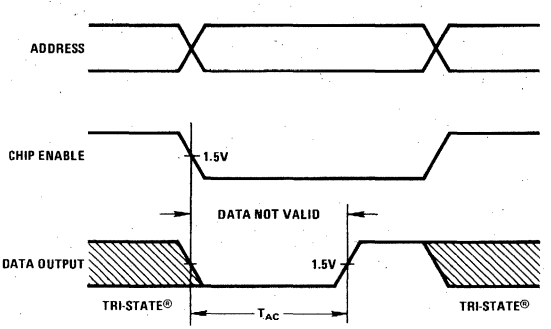
electrical characteristics

T_A within operating temperature range V_{SS} = +12V ±1.0V, V_{DD} = 0V, V_{GG} = −12V ±1.0V unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage Levels					
Logical "1"	(Note 1)			V_{SS} − 9.0	V
Logical "0"	(Note 1)	V_{SS} − 2.0			V
Output Voltage Levels					
Logical "1"	No Load			V_{DD}	V
Logical "0"	No Load	V_{SS}			V
Output Current					
Logical "1"	$V_O = V_{SS}$	2.5	15.0		mA
	$V_O = V_{SS}$ − 6.0V	0.7	7.0		mA
Logical "0"	$V_O = V_{SS}$ − 12V	−2.0	−6.5		mA
	$V_O = V_{SS}$ − 6.0V	−1.5	−5.0		mA
Power Supply Current					
I_{SS}	V_{SS} = +13V, V_{DD} = 0V, V_{GG} = −13V			30	mA
I_{GG}	V_{SS} = +13V, V_{DD} = 0V, V_{GG} = −13V			15	mA
Standby Power Dissipation	V_{SS} = +12V, V_{DD} = 0V V_{GG} = 0V, T_A = 25°C			150	mW
	V_{SS} = +12V, V_{DD} = 0V V_{GG} = −12V, T_A = 25°C			300	mW
Address Time					
T_{ACCESS}	T_A = 25°C		1.0	1.5	μs

Note 1: Negative logic definition.

switching time waveforms



MOS ROMs

MM4220/MM5220 1024-bit read only memory

general description

The MM4220/MM5220 is a 1024-bit static read only memory. It is a P-channel enhancement mode monolithic MOS integrated circuit utilizing low threshold voltage technology. The device is a non-volatile memory organized as 128-8-bit words or 256-4-bit words. Programming of the memory contents is accomplished by changing one mask during the device fabrication. Customer programs may be supplied in a tape, card, or pattern selection format.

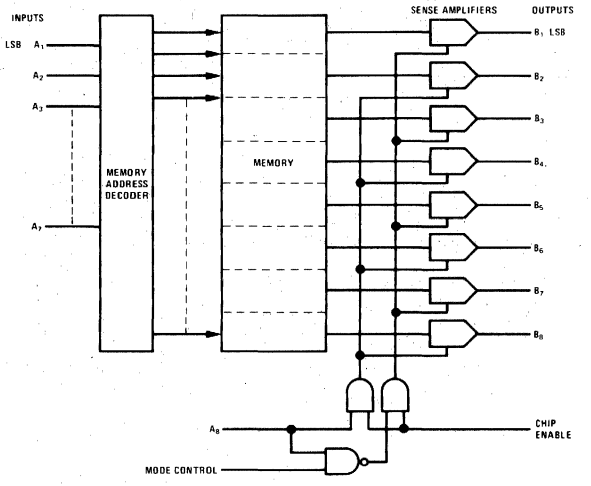
features

- Bipolar compatibility
- High speed operation — 500 ns typ
- Static operation — no clocks required
- Common data busing — output wire AND capability
- Chip enable output control.

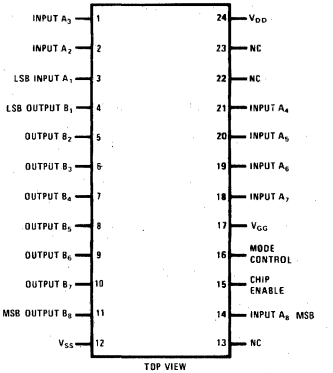
applications

- Code conversion
- Random logic synthesis
- Table look-up
- Character generators
- Microprogramming

block and connection diagrams



Dual-In-Line Package



Order Number MM4220J or MM5220J
See Package 11
Order Number MM5220N
See Package 18

Note: For programming information see AN-100.

absolute maximum ratings

V_{GG} Supply Voltage	$V_{SS}-30V$
V_{DD} Supply Voltage	$V_{SS}-15V$
Input Voltage	$(V_{SS}-20)V < V_{IN} < (V_{SS}+0.3)V$
Storage Temperature	$-65^{\circ}C$ to $+150^{\circ}C$
Operating Temperature MM4220	$-55^{\circ}C$ to $+125^{\circ}C$
MM5220	$0^{\circ}C$ to $+70^{\circ}C$
Lead Temperature (Soldering, 10 sec)	$300^{\circ}C$

electrical characteristics

T_A within operating temperature range, V_{SS} = +12V ±5% and V_{GG} = −12V ±5%, unless otherwise specified.

PARAMETER	CONDITION	MIN	TYP	MAX	UNITS
Output Voltage Levels					
MOS to MOS					
Logical "1"	1 MΩ to GND Load (Note 1)			V_{SS} −9.0	V
Logical "0"		V_{SS} −1.0			V
MOS to TTL					
Logical "1"	6.8 kΩ to V_{GG} Plus One			+0.4	V
Logical "0"	Standard Series 54/74 Gate Input	+2.4			V
Input Voltage Levels					
Logical "1"				V_{SS} −8.0	V
Logical "0"		V_{SS} −2.0			V
Power Supply Current	$T_A = 25^{\circ}C$				
V_{SS}			19	25	mA
V_{GG} (Note 1)				1	μA
Input Leakage	$V_{IN} = V_{SS}$ −12V			1	μA
Input Capacitance	f = 1.0 MHz V_{IN} = 0V		5		pF
Access Time (Notes 2, 3)	$T_A = 25^{\circ}C$				
T_{ACCESS}	(See Timing Diagram) V_{SS} = +12V V_{GG} = −12V	150	500	650	ns
Output AND Connection	MOS Load			3	
	TTL Load			8	

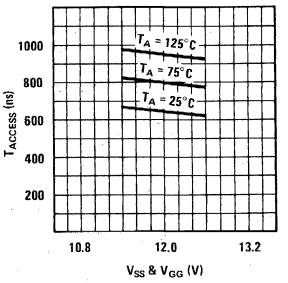
Note 1: The V_{GG} supply may be clocked to reduce device power without affecting access time.

Note 2: Address time is measured from the change of data on any input or Chip Enable line to the output of a TTL gate. See Timing Diagram.

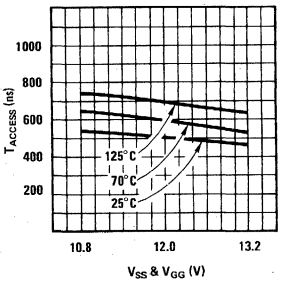
Note 3: The access time in the TTL load configuration follows the equation: T_{ACCESS} = the specified time + (N − 1) (50) ns where N = number of AND connections.

performance characteristics

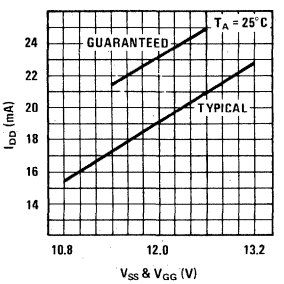
Guaranteed Access Time vs Supply Voltages



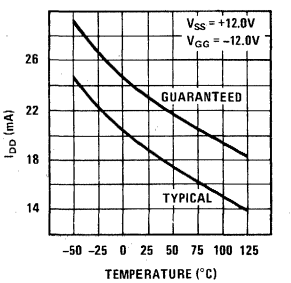
Typical Access Time vs Supply Voltages



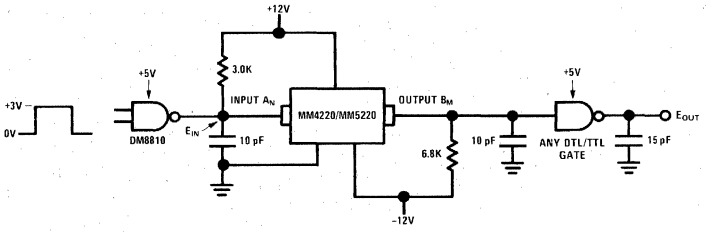
Power Supply Current vs Voltage

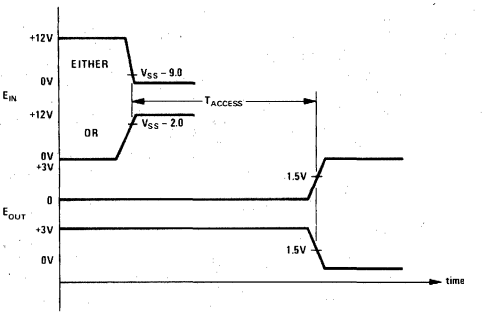


Power Supply Current vs Temperature



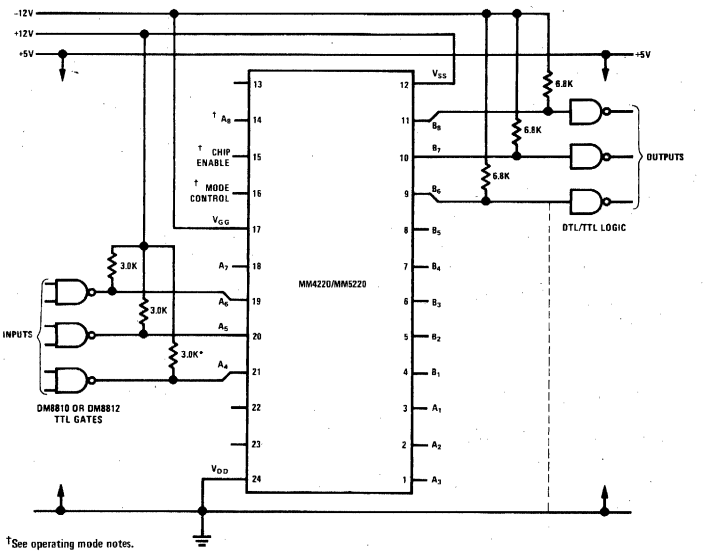
timing diagram/address time





typical application

128-8 Bit ROM Showing TTL Interface



†See operating mode notes.

*R values can vary from 740 to 30 kΩ depending on speed requirements.

OPERATING MODES

128x8 ROM connection
Mode Control – Logic "0"
A_8 – Logic "1"

256x4 ROM connection
Mode Control – Logic "1"
A_8 – Logic "0" Enables the odd ($B_1 \ldots B_7$) outputs
– Logic "1" Enables the even ($B_2 \ldots B_8$) outputs.

The outputs are "Enabled" when a logic "1" is applied to the Chip Enable line.

The outputs are connected to V_{DD} through an internal MOS resistor when "Disabled."

The logic levels are in negative voltage logic notation.

MOS ROMs

MM4220AE/MM5220AE ASCII-7 to hollerith code converter

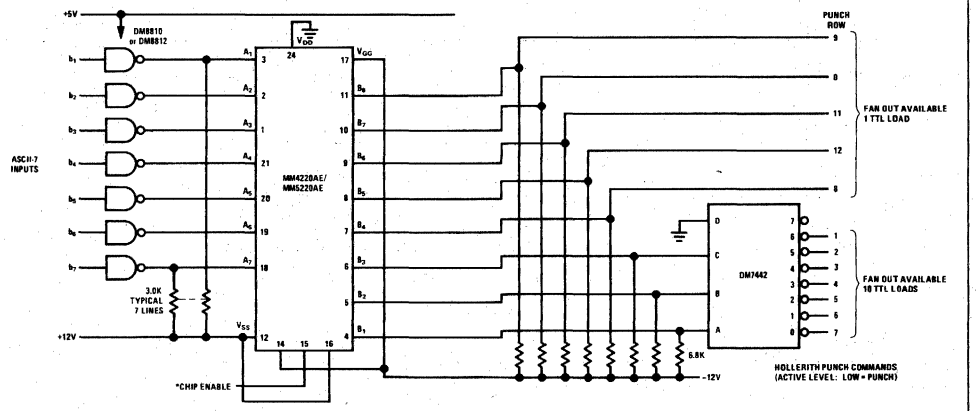
general description

The MM4220AE/MM5220AE 1024-bit read-only memory has been programmed to convert the 128 entries of the American Standard Code for Information Interchange in seven bits (ASCII-7) to Hollerith code (compressed to eight bits). The conversion performed follows the recommendation of American National Standard ANSI x 3.26–1970, Hollerith punched card code.

The typical application shows a recommended circuit for re-expansion of the Hollerith code to twelve lines.

For electrical, environmental and mechanical details, refer to the MM4220/MM5220 data sheet.

typical application



*Chip Enable = Logic "1" to obtain outputs.

Logic Levels:
DTL/TTL (except at MOS/ROM interface). Logic "1," +5.0V, NOM, Logic "0" ground, NOM.
MOS/ROM inputs and outputs. Logic "1," more negative, Logic "0," more positive.

Order Number MM4220AE/J or MM5220AE/J
See Package 11
Order Number MM5220AE/N
See Package 18

code conversion tables

$b_4\ b_3\ b_2\ b_1$	COL / ROW	b_7 0, b_6 0, b_5 0 — 0	b_7 0, b_6 0, b_5 1 — 1	b_7 0, b_6 1, b_5 0 — 2	b_7 0, b_6 1, b_5 1 — 3	b_7 1, b_6 0, b_5 0 — 4	b_7 1, b_6 0, b_5 1 — 5	b_7 1, b_6 1, b_5 0 — 6	b_7 1, b_6 1, b_5 1 — 7
0000	0	NUL 12-0-9-8-1	DLE 12-11-9-8-1	SP NO PCH	0 0	@ 8-4	P 11-7	` 8-1	p 12-11-7
0001	1	SCH 12-9-1	DC1 11-9-1	! ① 12-8-7	1 1	A 12-1	Q 11-8	a 12-0-1	q 12-11-8
0010	2	STX 12-9-2	DC2 11-9-2	" 8-7	2 2	B 12-2	R 11-9	b 12-0-2	r 12-11-9
0011	3	ETX 12-9-3	DC3 11-9-3	# 8-3	3 3	C 12-3	S 0-2	c 12-0-3	s 11-0-2
0100	4	ECT 9-7	DC4 9-8-4	$ 11-8-3	4 4	D 12-4	T 0-3	d 12-0-4	t 11-0-3
0101	5	ENQ 0-9-8-5	NAK 9-8-5	% 0-8-4	5 5	E 12-5	U 0-4	e 12-0-5	u 11-0-4
0110	6	ACK 0-9-8-6	SYN 9-2	& 12	6 6	F 12-6	V 0-5	f 12-0-6	v 11-0-5
0111	7	BEL 0-9-8-7	ETB 0-9-6	' 8-5	7 7	G 12-7	W 0-6	g 12-0-7	w 11-0-6
1000	8	BS 11-9-6	CAN 11-9-8	(12-8-5	8 8	H 12-8	X 0-7	h 12-0-8	x 11-0-7
1001	9	HT 12-9-5	EM 11-9-8-1	) 11-8-5	9 9	I 12-9	Y 0-8	i 12-0-9	y 11-0-8
1010	10	IF 0-9-5	SUB 9-8-7	* 11-8-4	: 8-2	J 11-1	Z 0-9	j 12-11-1	z 11-0-9
1011	11	VT 12-9-8-3	ESC 0-9-7	+ 12-8-6	; 11-8-6	K 11-2	[12-8-2	k 12-11-2	{ 12-0
1100	12	FF 12-9-8-4	FS 11-9-8-4	, 0-8-3	< 12-8-4	L 11-3	\ 0-8-2	l 12-11-3	¦ 12-11
1101	13	CR 12-9-8-5	GS 11-9-8-5	– 11	= 8-6	M 11-4	] 11-8-2	m 12-11-4	} 11-0
1110	14	SO 12-9-8-6	RS 11-9-8-6	. 12-8-3	> 0-8-6	N 11-5	∧ ② 11-8-7	n 12-11-5	~ 11-0-1
1111	15	SI 12-9-8-7	US 11-9-8-7	/ 0-1	? 0-8-7	O 11-6	– 0-8-5	o 12-11-6	DEL 12-9-7

① may be "|"

② may be "¬"

③ The top line in each entry to the table represents an assigned character (Columns 0 to 7).
The bottom line in each entry is the corresponding card hole-pattern.

code conversion tables(con't)

ADDRESS	OUTPUT CODE B8	B7	B6	B5	B4	B3	B2	B1
0	1	1	0	1	1	0	0	1
1	1	0	0	1	0	0	0	1
2	1	0	0	1	0	0	1	0
3	1	0	0	1	0	0	1	1
4	1	0	0	0	0	1	1	1
5	1	1	0	0	1	1	0	1
6	1	1	0	0	1	1	1	0
7	1	1	0	0	1	1	1	1
8	1	0	1	0	0	1	1	0
9	1	0	0	1	0	1	0	1
10	1	1	0	0	0	1	0	1
11	1	0	0	1	1	0	1	1
12	1	0	0	1	1	1	0	0
13	1	0	0	1	1	1	0	1
14	1	0	0	1	1	1	1	0
15	1	0	0	1	1	1	1	1
16	1	0	1	1	1	0	0	1
17	1	0	1	0	0	0	0	1
18	1	0	1	0	0	0	1	0
19	1	0	1	0	0	0	1	1
20	1	0	0	0	1	1	0	0
21	1	0	0	0	1	1	0	1
22	1	0	0	0	0	0	1	0
23	1	1	0	0	0	1	1	0
24	1	0	1	0	1	0	0	0
25	1	0	1	0	1	0	0	1
26	1	0	0	0	1	1	1	1
27	1	1	0	0	0	1	1	1
28	1	0	1	0	1	1	0	0
29	1	0	1	0	1	1	0	1
30	1	0	1	0	1	1	1	0
31	1	0	1	0	1	1	1	1
32	0	0	0	0	0	0	0	0
33	0	0	0	1	1	1	1	1
34	0	0	0	0	1	1	1	1
35	0	0	0	0	1	0	1	1
36	0	0	1	0	1	0	1	1
37	0	1	0	0	1	1	0	0
38	0	0	0	1	0	0	0	0
39	0	0	0	0	1	1	0	1
40	0	0	0	1	1	1	0	1
41	0	0	1	0	1	1	0	1
42	0	0	1	0	1	1	0	0
ROW	9	0	11	12	8	4	2	1

ADDRESS	OUTPUT CODE B8	B7	B6	B5	B4	B3	B2	B1
43	0	0	0	1	1	1	1	0
44	0	1	0	0	1	0	1	1
45	0	0	1	0	0	0	0	0
46	0	0	0	1	1	0	1	1
47	0	1	0	0	0	0	0	1
48	0	1	0	0	0	0	0	0
49	0	0	0	0	0	0	0	1
50	0	0	0	0	0	0	1	0
51	0	0	0	0	0	0	1	1
52	0	0	0	0	0	1	0	0
53	0	0	0	0	0	1	0	1
54	0	0	0	0	0	1	1	0
55	0	0	0	0	0	1	1	1
56	0	0	0	0	1	0	0	0
57	1	0	0	0	0	0	0	0
58	0	0	0	0	1	0	1	0
59	0	0	1	0	1	1	1	0
60	0	0	0	1	1	1	0	0
61	0	0	0	0	1	1	1	0
62	0	1	0	0	1	1	1	0
63	0	1	0	0	1	1	1	1
64	0	0	0	0	1	1	0	0
65	0	0	0	1	0	0	0	1
66	0	0	0	1	0	0	1	0
67	0	0	0	1	0	0	1	1
68	0	0	0	1	0	1	0	0
69	0	0	0	1	0	1	0	1
70	0	0	0	1	0	1	1	0
71	0	0	0	1	0	1	1	1
72	0	0	0	1	1	0	0	0
73	1	0	0	1	0	0	0	0
74	0	0	1	0	0	0	0	1
75	0	0	1	0	0	0	1	0
76	0	0	1	0	0	0	1	1
77	0	0	1	0	0	1	0	0
78	0	0	1	0	0	1	0	1
79	0	0	1	0	0	1	1	0
80	0	0	1	0	0	1	1	1
81	0	0	1	0	1	0	0	0
82	1	0	1	0	0	0	0	0
83	0	1	0	0	0	0	1	0
84	0	1	0	0	0	0	1	1
85	0	1	0	0	0	1	0	0
ROW	9	0	11	12	8	4	2	1

ADDRESS	OUTPUT CODE B8	B7	B6	B5	B4	B3	B2	B1
86	0	1	0	0	0	1	0	1
87	0	1	0	0	0	1	1	0
88	0	1	0	0	0	1	1	1
89	0	1	0	0	1	0	0	0
90	1	1	0	0	0	0	0	0
91	0	0	0	1	1	0	1	0
92	0	1	0	0	1	0	1	0
93	0	0	1	0	1	0	1	0
94	0	0	1	0	1	1	1	1
95	0	1	0	0	1	1	0	1
96	0	0	0	0	1	0	0	1
97	0	1	0	1	0	0	0	1
98	0	1	0	1	0	0	1	0
99	0	1	0	1	0	0	1	1
100	0	1	0	1	0	1	0	0
101	0	1	0	1	0	1	0	1
102	0	1	0	1	0	1	1	0
103	0	1	0	1	0	1	1	1
104	0	1	0	1	1	0	0	0
105	1	1	0	1	0	0	0	0
106	0	0	1	1	0	0	0	1
107	0	0	1	1	0	0	1	0
108	0	0	1	1	0	0	1	1
109	0	0	1	1	0	1	0	0
110	0	0	1	1	0	1	0	1
111	0	0	1	1	0	1	1	0
112	0	0	1	1	0	1	1	1
113	0	0	1	1	1	0	0	0
114	1	0	1	1	0	0	0	0
115	0	1	1	0	0	0	1	0
116	0	1	1	0	0	0	1	1
117	0	1	1	0	0	1	0	0
118	0	1	1	0	0	1	0	1
119	0	1	1	0	0	1	1	0
120	0	1	1	0	0	1	1	1
121	0	1	1	0	1	0	0	0
122	1	1	1	0	0	0	0	0
123	0	1	0	1	0	0	0	0
124	0	0	1	1	0	0	0	0
125	0	1	1	0	0	0	0	0
126	0	1	1	0	0	0	0	1
127	1	0	0	1	0	1	1	1
ROW	9	0	11	12	8	4	2	1

NATIONAL

MOS ROMs

MM4220AP/MM5220AP
BCDIC-to-ASCII code converter

general description

The MM4220AP/MM5220AP is used for the conversion of the Binary Coded Decimal Interchange Code(BCDIC) to the American Standard Code for Information Interchange (ASCII).

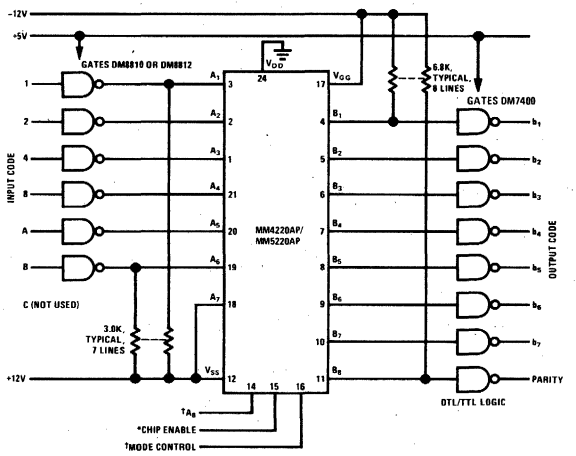
The input is a seven-bit BCDIC code with the exception of the parity (check) bit (pin 18) which is returned to +12V dc. The alternate set of input symbols is also shown in the Conversion Table for reference.

The output is a seven-bit ASCII code, with an eighth bit generated for even parity.

device characteristics

For full electrical, environmental, and mechanical details, refer to the MM4220/MM5220 1024-bit read only memory data sheet.

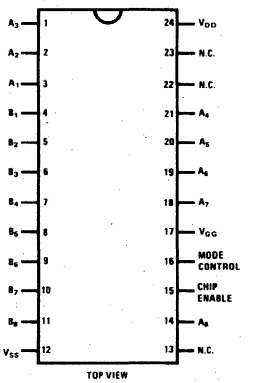
typical application



†Mode Control = Logic "0," A_8 = Logic "1."
*Chip Enable = Logic "1" to obtain outputs.
Logic Levels:
DTL/TTL (except at MOS/ROM interface). Logic "1," +5.0V, NOM. Logic "0," ground, NOM.
MOS/ROM inputs and outputs. Logic "1," more negative. Logic "0," more positive.

connection diagram

Dual-In-Line Package



Order Number MM4220AP/J or MM5220AP/J
See Package 11
Order Number MM5220AP/N
See Package 18

code conversion table

ROM ADDRESS	FUNCTION INPUT BCDIC SYMBOL	FUNCTION OUTPUT ASCII SYMBOL	CODE INPUT CODE	B	A	8	4	2	1	OUTPUT EP	b_7	b_6	b_5	b_4	b_3	b_2	b_1
0	Space	Space	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0
1	1	1	0	0	0	0	0	0	1	1	0	1	1	0	0	0	1
2	2	2	0	0	0	0	0	1	0	1	0	1	1	0	0	1	0
3	3	3	0	0	0	0	0	1	1	0	0	1	1	0	0	1	1
4	4	4	0	0	0	0	1	0	0	1	0	1	1	0	1	0	0
5	5	5	0	0	0	0	1	0	1	0	0	1	1	0	1	0	1
6	6	6	0	0	0	0	1	1	0	0	0	1	1	0	1	1	0
7	7	7	0	0	0	0	1	1	1	1	0	1	1	0	1	1	1
8	8	8	0	0	0	1	0	0	0	1	0	1	1	1	0	0	0
9	9	9	0	0	0	1	0	0	1	0	0	1	1	1	0	0	1
10	0	0	0	0	0	1	0	1	0	0	0	1	1	0	0	0	0
11	# or =	#	0	0	0	1	0	1	1	1	0	1	0	0	0	1	1
12	@ or '	@	0	0	0	1	1	0	0	1	1	0	0	0	0	0	0
13	:	:	0	0	0	1	1	0	1	0	0	1	1	1	0	1	0
14	>	>	0	0	0	1	1	1	0	1	0	1	1	1	1	1	0
15	√	?	0	0	0	1	1	1	1	0	0	1	1	1	1	1	1
16	Blank	!	0	0	1	0	0	0	0	1	1	0	1	1	0	1	1
17	/	/	0	0	1	0	0	0	1	1	0	1	0	1	1	1	1
18	S	S	0	0	1	0	0	1	0	0	1	0	1	0	0	1	1
19	T	T	0	0	1	0	0	1	1	1	1	0	1	0	1	0	0
20	U	U	0	0	1	0	1	0	0	0	1	0	1	0	1	0	1
21	V	V	0	0	1	0	1	0	1	0	1	0	1	0	1	1	0
22	W	W	0	0	1	0	1	1	0	1	1	0	1	0	1	1	1
23	X	X	0	0	1	0	1	1	1	1	1	0	1	1	0	0	0
24	Y	Y	0	0	1	1	0	0	0	0	1	0	1	1	0	0	1
25	Z	Z	0	0	1	1	0	0	1	0	1	0	1	1	0	1	0
26	‡	LF	0	0	1	1	0	1	0	0	0	0	0	1	0	1	0
27	,	,	0	0	1	1	0	1	1	1	0	1	0	1	1	0	0
28	% or (	%	0	0	1	1	1	0	0	1	0	1	0	0	1	0	1
29	∨	HT	0	0	1	1	1	0	1	0	0	0	0	1	0	0	1
30	\	'	0	0	1	1	1	1	0	0	0	1	0	0	1	1	1
31	≠	"	0	0	1	1	1	1	1	0	0	1	0	0	0	1	0
32	—	—	0	1	0	0	0	0	0	0	0	1	0	1	1	0	1
33	J	J	0	1	0	0	0	0	1	1	1	0	0	1	0	1	0
34	K	K	0	1	0	0	0	1	0	0	1	0	0	1	0	1	1
35	L	L	0	1	0	0	0	1	1	1	1	0	0	1	1	0	0
36	M	M	0	1	0	0	1	0	0	0	1	0	0	1	1	0	1
37	N	N	0	1	0	0	1	0	1	0	1	0	0	1	1	1	0
38	O	O	0	1	0	0	1	1	0	1	1	0	0	1	1	1	1
39	P	P	0	1	0	0	1	1	1	0	1	0	1	0	0	0	0
40	Q	Q	0	1	0	1	0	0	0	1	1	0	1	0	0	0	1
41	R	R	0	1	0	1	0	0	1	1	1	0	1	0	0	1	0
42	!	'	0	1	0	1	0	1	0	0	0	1	0	0	0	0	1
43	$	$	0	1	0	1	0	1	1	0	0	1	0	0	1	0	0
44	*	*	0	1	0	1	1	0	0	1	0	1	0	1	0	1	0
45	]	)	0	1	0	1	1	0	1	1	0	1	0	1	0	0	1
46	;	;	0	1	0	1	1	1	0	1	0	1	1	1	0	1	1
47	∧	[	0	1	0	1	1	1	1	1	1	0	1	1	1	0	1
48	& or ¬	&	0	1	1	0	0	0	0	1	0	1	0	0	1	1	0
49	A	A	0	1	1	0	0	0	1	0	1	0	0	0	0	0	1
50	B	B	0	1	1	0	0	1	0	0	1	0	0	0	0	1	0
51	C	C	0	1	1	0	0	1	1	1	1	0	0	0	0	1	1
52	D	D	0	1	1	0	1	0	0	0	1	0	0	0	1	0	0
53	E	E	0	1	1	0	1	0	1	1	1	0	0	0	1	0	1
54	F	F	0	1	1	0	1	1	0	1	1	0	0	0	1	1	0
55	G	G	0	1	1	0	1	1	1	0	1	0	0	0	1	1	1
56	H	H	0	1	1	1	0	0	0	0	1	0	0	1	0	0	0
57	I	I	0	1	1	1	0	0	1	1	1	0	0	1	0	0	1
58	?	(	0	1	1	1	0	1	0	0	0	1	0	1	0	1	1
59	.	.	0	1	1	1	0	1	1	0	0	1	0	1	1	1	0
60	¤ or)	⌒	0	1	1	1	1	0	0	1	1	0	1	1	1	1	0
61	[	(	0	1	1	1	1	0	1	0	0	1	0	1	0	0	0
62	<	<	0	1	1	1	1	1	0	0	0	1	1	1	1	0	0
63	‡	CR	0	1	1	1	1	1	1	1	0	0	0	1	1	0	1
			A_7	A_6	A_5	A_4	A_3	A_2	A_1	B_8	B_7	B_6	B_5	B_4	B_3	B_2	B_1

NATIONAL

MM4220BL/MM5220BL baudot-to-ASCII code converter

general description

The MM4220BL/MM5220BL is used for conversion of the Communications Set Baudot code to the American Standard Code for Information Interchange (ASCII).

The Baudot and ASCII codes have different formats. ASCII has a unique code combination for each alphabetic, numerical, or control character. The correct interpretation of a five bit Baudot is dependent upon knowing its previous history; whether upper or lower case was *last* selected. In effect a sixth-bit, which can be called the Case Bit, is required to uniquely identify the Baudot input. The latch circuit shown in the typical application can store this information and will generate the Case Bit. If the bit is externally supplied, the feedback and latch circuits can be deleted (as shown with the X's).

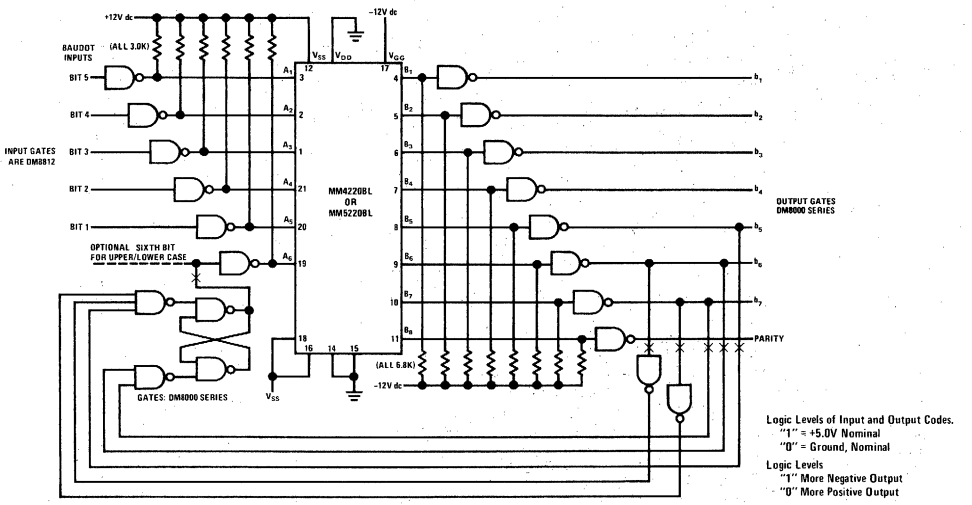
The accompanying table is applicable for the code conversion scheme as shown (or its alternate) rather than for the device itself. The input and output codes are defined at the TTL gates with the logic trues high (Logic "1" = +5 volts, nominal; Logic "0" = Ground, nominal).

device characteristics

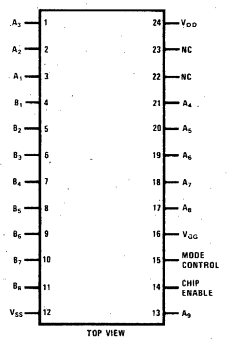
For full electrical, environmental, and mechanical details, refer to the MM4220/MM5220 1024-bit read only memory data sheet.

typical application and connection diagram

Baudot to ASCII



Dual-In-Line Package



Order Number MM4220BL/J or MM5220BL/J
See Package 11
Order Number MM5220BL/N
See Package 18

code conversion tables

ROM ADDRESS	FUNCTION INPUT BAUDOT SYMBOL	FUNCTION OUTPUT ASCII SYMBOL	CODE INPUT BAUDOT CASE	1	2	3	4	5	OUTPUT ASCII EP	b_7	b_6	b_5	b_4	b_3	b_2	b_1
0	Blank	NULL	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	T	T	0	0	0	0	0	1	1	1	0	1	0	1	0	0
2	CR	CR	0	0	0	0	1	0	1	0	0	0	1	1	0	1
3	O	O	0	0	0	0	1	1	1	1	0	0	1	1	1	1
4	Space	Space	0	0	0	1	0	0	1	0	1	0	0	0	0	0
5	H	H	0	0	0	1	0	1	0	1	0	0	1	0	0	0
6	N	N	0	0	0	1	1	0	0	1	0	0	1	1	1	0
7	M	M	0	0	0	1	1	1	0	1	0	0	1	1	0	1
8	LF	LF	0	0	1	0	0	0	0	0	0	0	1	0	1	0
9	L	L	0	0	1	0	0	1	1	1	0	0	1	1	0	0
10	R	R	0	0	1	0	1	0	1	1	0	1	0	0	1	0
11	G	G	0	0	1	0	1	1	0	1	0	0	0	1	1	1
12	I	I	0	0	1	1	0	0	1	1	0	0	1	0	0	1
13	P	P	0	0	1	1	0	1	0	1	0	1	0	0	0	0
14	C	C	0	0	1	1	1	0	1	1	0	0	0	0	1	1
15	V	V	0	0	1	1	1	1	0	1	0	1	0	1	1	0
16	E	E	0	1	0	0	0	0	1	1	0	0	0	1	0	1
17	Z	Z	0	1	0	0	0	1	0	1	0	1	1	0	1	0
18	D	D	0	1	0	0	1	0	0	1	0	0	0	1	0	0
19	B	B	0	1	0	0	1	1	0	1	0	0	0	0	1	0
20	S	S	0	1	0	1	0	0	0	1	0	1	0	0	1	1
21	Y	Y	0	1	0	1	0	1	0	1	0	1	1	0	0	1
22	F	F	0	1	0	1	1	0	1	1	0	0	0	1	1	0
23	X	X	0	1	0	1	1	1	1	1	0	1	1	0	0	0
24	A	A	0	1	1	0	0	0	0	1	0	0	0	0	0	1
25	W	W	0	1	1	0	0	1	1	1	0	1	0	1	1	1
26	J	J	0	1	1	0	1	0	1	1	0	0	1	0	1	0
27	Upper	IS1/Can	0	1	1	0	1	1	0	0	0	1	1	0	0	0
28	U	U	0	1	1	1	0	0	0	1	0	1	0	1	0	1
29	Q	Q	0	1	1	1	0	1	1	1	0	1	0	0	0	1
30	K	K	0	1	1	1	1	0	0	1	0	0	1	0	1	1
31	Lower	Delete	0	1	1	1	1	1	1	1	1	1	1	1	1	1
32	Blank	NULL	1	0	0	0	0	0	0	0	0	0	0	0	0	0
33	5	5	1	0	0	0	0	1	0	0	1	1	0	1	0	1
34	CR	CR	1	0	0	0	1	0	1	0	0	0	1	1	0	1
35	9	9	1	0	0	0	1	1	0	0	1	1	1	0	0	1
36	Space	Space	1	0	0	1	0	0	1	0	1	0	0	0	0	0
37	#/£ S/S	BS/FE	1	0	0	1	0	1	1	0	0	0	1	0	0	0
38	,	,	1	0	0	1	1	0	1	0	1	0	1	1	0	0
39	.	.	1	0	0	1	1	1	0	0	1	0	1	1	1	0
40	LF	LF	1	0	1	0	0	0	0	0	0	0	1	0	1	0
41	)	)	1	0	1	0	0	1	1	0	1	0	1	0	0	1
42	4	4	1	0	1	0	1	0	1	0	1	1	0	1	0	0
43	&	&	1	0	1	0	1	1	1	0	1	0	0	1	1	0
44	8	8	1	0	1	1	0	0	1	0	1	1	1	0	0	0
45	0	0	1	0	1	1	0	1	0	0	1	1	0	0	0	0
46	:	:	1	0	1	1	1	0	0	0	1	1	1	0	1	0
47	;	;	1	0	1	1	1	1	1	0	1	1	1	0	1	1
48	3	3	1	1	0	0	0	0	0	0	1	1	0	0	1	1
49	"	"	1	1	0	0	0	1	0	0	1	0	0	0	1	0
50	$	$	1	1	0	0	1	0	0	0	1	0	0	1	0	0
51	?	?	1	1	0	0	1	1	0	0	1	1	1	1	1	1
52	Bell	Bell	1	1	0	1	0	0	1	0	0	0	0	1	1	1
53	6	6	1	1	0	1	0	1	0	0	1	1	0	1	1	0
54	!	!	1	1	0	1	1	0	0	0	1	0	0	0	0	1
55	/	/	1	1	0	1	1	1	1	0	1	0	1	1	1	1
56	—	—	1	1	1	0	0	0	0	0	1	0	1	1	0	1
57	2	2	1	1	1	0	0	1	1	0	1	1	0	0	1	0
58	'	'	1	1	1	0	1	0	0	0	1	0	0	1	1	1
59	Upper	Can	1	1	1	0	1	1	0	0	0	1	1	0	0	0
60	7	7	1	1	1	1	0	0	1	0	1	1	0	1	1	1
61	1	1	1	1	1	1	0	1	1	0	1	1	0	0	0	1
62	(	(	1	1	1	1	1	0	0	0	1	0	1	0	0	0
63	Lower	Delete	1	1	1	1	1	1	1	1	1	1	1	1	1	1

LEGEND:
EP = Even Parity
LF = Line Feed
CR = Carriage Return
Can = Cancel
IS1 = Information Separator #1
S/S = Stop/Start
BS = Back Space

NATIONAL

MOS ROMs

MM4220BM/MM5220BM sine look-up table

general description

The MM4220BM/MM5220BM is a 1024-monolithic MOS read only memory that has been programmed to solve for the sine value x of a known angle θ; i.e., to obtain the solution of the equation $x = \sin \theta$.

Values of θ are defined in the look up table for $0^\circ \leq \theta < 90^\circ$ (quadrant I) which has corresponding solutions of $0 \leq x < 1$. For values of $90^\circ < \theta \leq 180^\circ$ (quadrant II), enter the complement $(180^\circ - \theta)$ to obtain the correct solution. Solutions for quadrants III and IV differ in sign with I and II. This is summarized in Table 1.

This input is divided into 128 parts for θ in each quadrant. Thus, the appropriate input address is $(\theta^1/90^\circ)(128)$ to the nearest whole integer. The actual input code to the ROM is the input address expressed in binary, with A_1 being the least significant bit.

The output is the value of X expressed in binary. The output lines $B_1, B_2, \ldots . B_8$ are binary place values 1/2, 1/4, ... 1/256. The sign for negative values of X is externally generated.

The 8 bit output code has been rounded off from a larger word code, i.e., where A_9 was a binary "1" it carried into the LSB of the eight bit code, where A_9 was a binary "0" it was simply dropped.

EXAMPLE

Find the sine of 45°.

The input address is (45/90) 128 = 64 or 1000000, as expressed in binary. The converter generates the output .10110101 whose decimal equivalent is 0.707131. Thus, sin 45° = 0.707.

Find the sine of 210°.

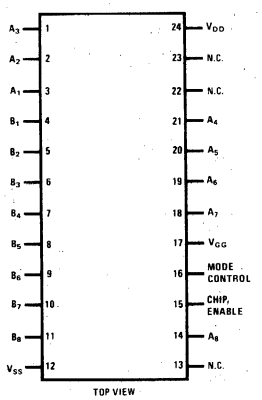
This value is in quadrant III; therefore $\theta^1 = 210^\circ - 180^\circ = 30^\circ$. The input address is then (30/90) $128 \cong 43$ to the nearest whole integer. The binary input to the ROM is then 0101011. The output value is .10000001 or 0.503906. Thus, sin 210° = −0.504, with the sign generated by the external logic. The solution is within 1%; note that address 43 is actually equal to 30.23°.

device characteristics

For full electrical, environmental and mechanical details refer to the MM4220/MM5220 1024-bit read only memory data sheet.

connection diagram

Dual-In-Line Package



Order Number MM4220BM/J or MM5220BM/J
See Package 11
Order Number MM5220BM/N
See Package 18

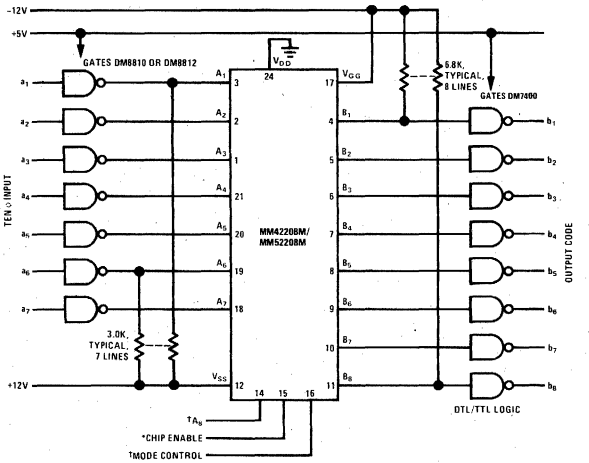
pattern selection form

ADDRESS REFERENCE	FUNCTION INPUT		CODE OUTPUT							
	DEGREES	RADIANS	B_8	B_7	B_6	B_5	B_4	B_3	B_2	B_1
0	.00	.000	0	0	0	0	0	0	0	0
1	.70	.012	1	1	0	0	0	0	0	0
2	1.41	.025	0	1	1	0	0	0	0	0
3	2.11	.037	1	0	0	1	0	0	0	0
4	2.81	.049	0	0	1	1	0	0	0	0
5	3.52	.061	1	1	1	1	0	0	0	0
6	4.22	.074	1	1	0	0	1	0	0	0
7	4.92	.086	0	1	1	0	1	0	0	0
8	5.63	.098	1	0	0	1	1	0	0	0
9	6.33	.110	0	0	1	1	1	0	0	0
10	7.03	.123	1	1	1	1	1	0	0	0
11	7.73	.135	0	1	0	0	0	1	0	0
12	8.44	.147	1	0	1	0	0	1	0	0
13	9.14	.160	0	0	0	1	0	1	0	0
14	9.84	.172	0	0	1	1	0	1	0	0
15	10.55	.184	1	1	1	1	0	1	0	0
16	11.25	.196	0	1	0	0	1	1	0	0
17	11.95	.209	1	0	1	0	1	1	0	0
18	12.66	.221	0	0	0	1	1	1	0	0
19	13.36	.233	1	1	0	1	1	1	0	0
20	14.06	.245	0	1	1	1	1	1	0	0
21	14.77	.258	1	0	0	0	0	0	1	0
22	15.47	.270	0	0	1	0	0	0	1	0
23	16.17	.282	1	1	1	0	0	0	1	0
24	16.88	.295	0	1	0	1	0	0	1	0
25	17.58	.307	1	0	1	1	0	0	1	0
26	18.28	.319	0	0	0	0	1	0	1	0
27	18.98	.331	1	1	0	0	1	0	1	0
28	19.69	.344	0	1	1	0	1	0	1	0
29	20.39	.356	1	0	0	1	1	0	1	0
30	21.09	.368	0	0	1	1	1	0	1	0
31	21.80	.380	1	1	1	1	1	0	1	0
32	22.50	.393	0	1	0	0	0	1	1	0
33	23.20	.405	1	1	1	0	0	1	1	0
34	23.91	.417	1	1	1	0	0	1	1	0
35	24.61	.430	0	1	0	1	0	1	1	0
36	25.31	.442	1	0	1	1	0	1	1	0
37	26.02	.454	0	0	0	0	1	1	1	0
38	26.72	.466	1	1	0	0	1	1	1	0
39	27.42	.479	0	1	1	0	1	1	1	0
40	28.13	.491	0	0	0	1	1	1	1	0
41	28.83	.503	1	1	0	1	1	1	1	0
42	29.53	.515	0	1	1	1	1	1	1	0
43	30.23	.528	0	0	0	0	0	0	0	1
44	30.94	.540	1	1	0	0	0	0	0	1
45	31.64	.552	0	1	1	0	0	0	0	1
46	32.34	.565	1	0	0	1	0	0	0	1
47	33.05	.577	1	1	0	1	0	0	0	1
48	33.75	.589	0	1	1	1	0	0	0	1
49	34.45	.601	1	0	0	0	1	0	0	1
50	35.16	.614	1	1	0	0	1	0	0	1
51	35.86	.626	0	1	1	0	1	0	0	1
52	36.56	.638	0	0	0	1	1	0	0	1
53	37.27	.650	1	1	0	1	1	0	0	1
54	37.97	.663	1	0	1	1	1	0	0	1
55	38.67	.675	0	0	0	0	0	1	0	1
56	39.37	.687	0	1	0	0	0	1	0	1
57	40.08	.699	1	0	1	0	0	1	0	1
58	40.78	.712	1	1	1	0	0	1	0	1
59	41.48	.724	1	0	0	1	0	1	0	1
60	42.19	.736	0	0	1	1	0	1	0	1
61	42.89	.749	0	1	1	1	0	1	0	1
62	43.59	.761	0	0	0	0	1	1	0	1
63	44.30	.773	1	1	0	0	1	1	0	1

pattern selection form(con't)

ADDRESS REFERENCE	FUNCTION INPUT		CODE OUTPUT							
	DEGREES	RADIANS	B_8	B_7	B_6	B_5	B_4	B_3	B_2	B_1
64	45.00	.785	1	0	1	0	1	1	0	1
65	45.70	.798	1	1	1	0	1	1	0	1
66	46.41	.810	1	0	0	1	1	1	0	1
67	47.11	.822	1	1	0	1	1	1	0	1
68	47.81	.834	1	0	1	1	1	1	0	1
69	48.52	.847	0	0	0	0	0	0	1	1
70	49.22	.859	0	1	0	0	0	0	1	1
71	49.92	.871	0	0	1	0	0	0	1	1
72	50.62	.884	0	1	1	0	0	0	1	1
73	51.33	.896	0	0	0	1	0	0	1	1
74	52.03	.908	0	1	0	1	0	0	1	1
75	52.73	.920	1	1	0	1	0	0	1	1
76	53.44	.933	1	0	1	1	0	0	1	1
77	54.14	.945	1	1	1	1	0	0	1	1
78	54.84	.957	1	0	0	0	1	0	1	1
79	55.55	.969	1	1	0	0	1	0	1	1
80	56.25	.982	1	0	1	0	1	0	1	1
81	56.95	.994	0	1	1	0	1	0	1	1
82	57.66	1.006	0	0	0	1	1	0	1	1
83	58.36	1.019	0	1	0	1	1	0	1	1
84	59.06	1.031	1	1	0	1	1	0	1	1
85	59.77	1.043	1	0	1	1	1	0	1	1
86	60.47	1.055	0	1	1	1	1	0	1	1
87	61.17	1.068	0	0	0	0	0	1	1	1
88	61.87	1.080	0	1	0	0	0	1	1	1
89	62.58	1.092	1	1	0	0	0	1	1	1
90	63.28	1.104	0	0	1	0	0	1	1	1
91	63.98	1.117	0	1	1	0	0	1	1	1
92	64.69	1.129	1	1	1	0	0	1	1	1
93	65.39	1.141	0	0	0	1	0	1	1	1
94	66.09	1.154	0	1	0	1	0	1	1	1
95	66.80	1.166	1	1	0	1	0	1	1	1
96	67.50	1.178	0	0	1	1	0	1	1	1
97	68.20	1.190	1	0	1	1	0	1	1	1
98	68.91	1.203	1	1	1	1	0	1	1	1
99	69.61	1.215	0	0	0	0	1	1	1	1
100	70.31	1.227	1	0	0	0	1	1	1	1
101	71.02	1.239	0	1	0	0	1	1	1	1
102	71.72	1.252	1	1	0	0	1	1	1	1
103	72.42	1.264	0	0	1	0	1	1	1	1
104	73.12	1.276	1	0	1	0	1	1	1	1
105	73.83	1.289	0	1	1	0	1	1	1	1
106	74.53	1.301	0	1	1	0	1	1	1	1
107	75.23	1.313	1	1	1	0	1	1	1	1
108	75.94	1.325	0	0	0	1	1	1	1	1
109	76.64	1.338	1	0	0	1	1	1	1	1
110	77.34	1.350	0	1	0	1	1	1	1	1
111	78.05	1.362	0	1	0	1	1	1	1	1
112	78.75	1.374	1	1	0	1	1	1	1	1
113	79.45	1.387	1	1	0	1	1	1	1	1
114	80.16	1.399	0	0	1	1	1	1	1	1
115	80.86	1.411	0	0	1	1	1	1	1	1
116	81.56	1.424	1	0	1	1	1	1	1	1
117	82.27	1.436	1	0	1	1	1	1	1	1
118	82.97	1.448	0	1	1	1	1	1	1	1
119	83.67	1.460	0	1	1	1	1	1	1	1
120	84.38	1.473	1	1	1	1	1	1	1	1
121	85.08	1.485	1	1	1	1	1	1	1	1
122	85.78	1.497	1	1	1	1	1	1	1	1
123	86.48	1.509	1	1	1	1	1	1	1	1
124	87.19	1.522	1	1	1	1	1	1	1	1
125	87.89	1.534	1	1	1	1	1	1	1	1
126	88.59	1.546	1	1	1	1	1	1	1	1
127	89.30	1.559	1	1	1	1	1	1	1	1

typical application



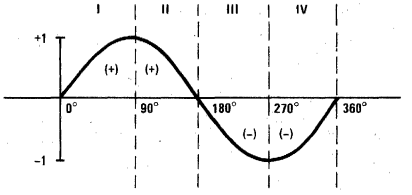
†Mode Control = Logic "0," A_8 = Logic "1."

*Chip Enable = Logic "1" to obtain outputs.

Logic Levels:
DTL/TTL (except at MOS/ROM interface). Logic "1," +5.0V, NOM. Logic "0," ground, NOM.
MOS/ROM inputs and outputs. Logic "1," more negative. Logic "0," more positive.

Table 1. SINE

	INPUT		OUTPUT	
Quadrant	**Range**	**Entry to ROM (θ^1)**	**Binary Value**	**Sign**
I	$\geq 0^\circ < 90^\circ$	Direct	Direct Reading	+
II	$> 90^\circ \leq 180^\circ$	$180^\circ - X$	Direct Reading	+
III	$\geq 180^\circ < 270^\circ$	$X - 180^\circ$	Direct Reading	-
IV	$> 270^\circ \leq 360^\circ$	$360^\circ - X$	Direct Reading	-



NATIONAL

MOS ROMs

MM4220BN/MM5220BN arctangent look-up table

general description

The MM4220BN/MM5220BN is a 1024-bit monolithic MOS read only memory that has been programmed to solve for the angle θ whose tangent value x is known; i.e., to obtain the solution to the equation: $\theta = \arctan x$.

Values of x are defined in the Look Up table for $0 \leq x < 1$ with angles corresponding from $0^\circ \leq \theta < 45^\circ$. For values $x \geq 1$, the reciprocal of x (i.e., 1/x) must be entered and the output angle must be complemented to obtain the actual value.

The input is divided into 128 equal parts for x. Thus, the appropriate input address is (128)(x) to the nearest whole integer for obtaining the appropriate ROM address. The input code is the ROM address expressed in binary with A_1 being the least significant bit. For input values greater than unity, the decimal reciprocal is to be taken prior to entry of the binary address.

The output has been normalized for 45°. To obtain the true angular reading, the output should be multiplied by 45°, i.e.: $\theta = (\theta_{output}) \times 45^\circ$ where θ_{output} is the decimal equivalent of the output. The output code is the normalized value of the angle θ expressed in binary. The output lines B_1, B_2, ... B_8 are binary place values 1/2, 1/4, ... 1/256. To obtain angles between 45° and 89.6° which occur when input values of x are equal to or greater than unity, either complement the output binary code and add a 1, or complement the resultant angular value (i.e., subtract from 90°).

The 8-bit output code has been rounded off. That is, if another bit of even lower significance had been computed for the given arctangent value was a binary "1", it would have carried over into the LSB of the eight bit code. If it was a binary "0", it would have been dropped.

EXAMPLE

Find the angle whose tangent is 0.258.

The input address is 128 x 0.258, or 33 to the nearest integer. Expressed in binary, this is 0100001, and is the actual input code to the converter. The converter will generate the binary value .01010010, whose decimal equivalent is 0.3203125.

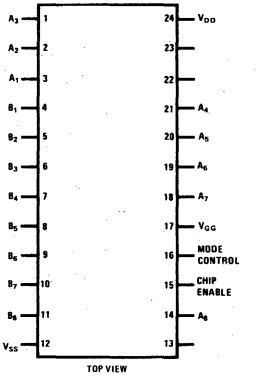
Thus, $\theta = 0.320 \times 45^\circ = 14.4^\circ$

device characteristics

For full electrical, environmental, and mechanical details, refer to the MM4220/MM5220 1024-bit read only memory data sheet.

connection diagram

Dual-In-Line Package



Order Number MM4220BN/J or MM5220BN/J
See Package 11

Order Number MM5220BN/N
See Package 18

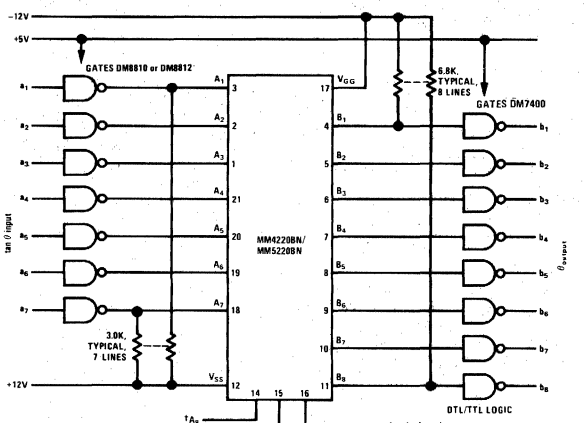
pattern selection form

ADDRESS 128 (x)	OUTPUT CODE (θ_{OUTPUT}) B8	B7	B6	B5	B4	B3	B2	B1
0	0	0	0	0	0	0	0	0
1	0	1	0	0	0	0	0	0
2	1	0	1	0	0	0	0	0
3	1	1	1	0	0	0	0	0
4	0	1	0	1	0	0	0	0
5	0	0	1	1	0	0	0	0
6	1	1	1	1	0	0	0	0
7	0	1	0	0	1	0	0	0
8	0	0	1	0	1	0	0	0
9	1	1	1	0	1	0	0	0
10	1	0	0	1	1	0	0	0
11	0	0	1	1	1	0	0	0
12	0	1	1	1	1	0	0	0
13	1	0	0	0	0	1	0	0
14	1	1	0	0	0	1	0	0
15	0	1	1	0	0	1	0	0
16	0	0	0	1	0	1	0	0
17	1	1	0	1	0	1	0	0
18	1	0	1	1	0	1	0	0
19	0	0	0	0	1	1	0	0
20	0	1	0	0	1	1	0	0
21	1	0	1	0	1	1	0	0
22	1	1	1	0	1	1	0	0
23	0	1	0	1	1	1	0	0
24	0	0	1	1	1	1	0	0
25	1	1	1	1	1	1	0	0
26	1	0	0	0	0	0	1	0
27	0	0	1	0	0	0	1	0
28	0	1	1	0	0	0	1	0
29	0	0	0	1	0	0	1	0
30	1	1	0	1	0	0	1	0
31	1	0	1	1	0	0	1	0
32	0	0	0	0	1	0	1	0
33	0	1	0	0	1	0	1	0
34	0	0	1	0	1	0	1	0
35	1	1	1	0	1	0	1	0
36	1	0	0	1	1	0	1	0
37	1	1	0	1	1	0	1	0
38	0	1	1	1	1	0	1	0
39	0	0	0	0	0	1	1	0
40	0	1	0	0	0	1	1	0
41	1	0	1	0	0	1	1	0
42	1	1	1	0	0	1	1	0
43	1	0	0	1	0	1	1	0
44	0	0	1	1	0	1	1	0
45	0	1	1	1	0	1	1	0
46	0	0	0	0	1	1	1	0
47	0	1	0	0	1	1	1	0
48	1	0	1	0	1	1	1	0
49	1	1	1	0	1	1	1	0
50	1	0	0	1	1	1	1	0
51	1	1	0	1	1	1	1	0
52	0	1	1	1	1	1	1	0
53	0	0	0	0	0	0	0	1
54	0	1	0	0	0	0	0	1
55	0	0	1	0	0	0	0	1
56	0	1	1	0	0	0	0	1
57	0	0	0	1	0	0	0	1
58	0	1	0	1	0	0	0	1
59	1	0	1	1	0	0	0	1
60	1	1	1	1	0	0	0	1
61	1	0	0	0	1	0	0	1
62	1	1	0	0	1	0	0	1
63	1	0	1	0	1	0	0	1
64	1	1	1	0	1	0	0	1
65	1	0	0	1	1	0	0	1
66	1	1	0	1	1	0	0	1
67	1	0	1	1	1	0	0	1
68	1	1	1	1	1	0	0	1
69	1	0	0	0	0	1	0	1
70	1	1	0	0	0	1	0	1
71	1	0	1	0	0	1	0	1
72	1	1	1	0	0	1	0	1
73	1	0	0	1	0	1	0	1
74	1	1	0	1	0	1	0	1
75	1	0	1	1	0	1	0	1
76	0	1	1	1	0	1	0	1
77	0	0	0	0	1	1	0	1
78	0	1	0	0	1	1	0	1
79	0	0	1	0	1	1	0	1
80	0	1	1	0	1	1	0	1
81	0	0	0	1	1	1	0	1
82	1	0	0	1	1	1	0	1
83	1	1	0	1	1	1	0	1
84	1	0	1	1	1	1	0	1
85	1	1	1	1	1	1	0	1
86	1	0	0	0	0	0	1	1
87	0	1	0	0	0	0	1	1
88	0	0	1	0	0	0	1	1
89	0	1	1	0	0	0	1	1
90	1	1	1	0	0	0	1	1
91	1	0	0	1	0	0	1	1
92	1	1	0	1	0	0	1	1
93	1	0	1	1	0	0	1	1
94	0	1	1	1	0	0	1	1
95	0	0	0	0	1	0	1	1
96	1	0	0	0	1	0	1	1
97	1	1	0	0	1	0	1	1
98	1	0	1	0	1	0	1	1
99	0	1	1	0	1	0	1	1
100	0	0	0	1	1	0	1	1
101	1	0	0	1	1	0	1	1
102	1	1	0	1	1	0	1	1
103	1	0	1	1	1	0	1	1
104	0	1	1	1	1	0	1	1
105	0	0	0	0	0	1	1	1
106	1	0	0	0	0	1	1	1
107	1	1	0	0	0	1	1	1
108	0	0	1	0	0	1	1	1
109	0	1	1	0	0	1	1	1
110	1	1	1	0	0	1	1	1
111	1	0	0	1	0	1	1	1
112	0	1	0	1	0	1	1	1
113	1	1	0	1	0	1	1	1
114	1	0	1	1	0	1	1	1
115	0	1	1	1	0	1	1	1
116	0	0	0	0	1	1	1	1
117	1	0	0	0	1	1	1	1
118	1	1	0	0	1	1	1	1
119	0	0	1	0	1	1	1	1
120	1	0	1	0	1	1	1	1
121	1	1	1	0	1	1	1	1
122	0	0	0	1	1	1	1	1
123	1	0	0	1	1	1	1	1
124	1	1	0	1	1	1	1	1
125	0	0	1	1	1	1	1	1
126	1	0	1	1	1	1	1	1
127	0	1	1	1	1	1	1	1

Note: 1 more negative output.
0 more positive output.

MM522BN

typical application



†Mode Control = Logic "0," A_8 = Logic "1."
*Chip Enable = Logic "1" to obtain outputs.

Logic Levels:
DTL/TTL (except at MOS/ROM interface). Logic "1," +5.0V, NOM. Logic "0," ground, NOM.
MOS/ROM inputs and outputs. Logic "1," more negative. Logic "0," more positive.

NATIONAL

MOS ROMs

MM4220DF/MM5220DF
"quick brown fox" generator

general description

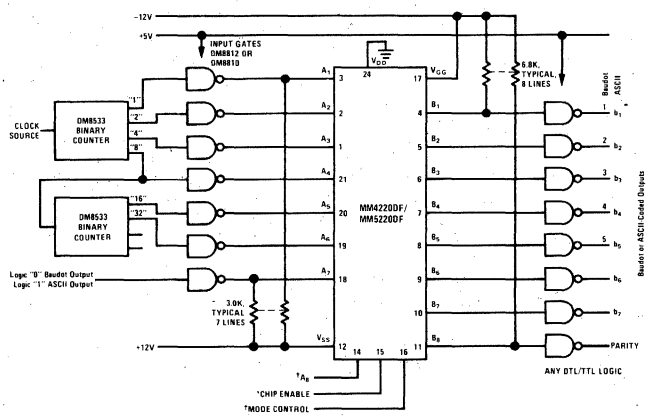
The MM4220DF/MM5220DF is designed for exercising and rapid testing of ASCII and Baudot-coded keyboards, typing mechanisms, and data communications links by generating the internationally accepted "Quick Brown Fox" message.

The input is a 7-bit binary sequential count. The output of a 6 stage up-counter can be used; a seventh bit selects the desired code. The message is generated in the 5-bit Baudot Communications Set code with a binary count input of 0 to 63. The message is generated in the 7-bit American Standard Code for Information Interchange (ASCII) along with an even parity bit for a binary count input of 64 to 127.

device characteristics

The message generator is fully contained on a monolithic MOS integrated circuit chip utilizing low threshold voltage technology for increased DTL/TTL compatibility. For complete electrical, environmental, and mechanical details, refer to the MM4220/MM5220 1024-bit read only memory data sheet.

typical applications



†Mode Control = Logic "0," A_8 = Logic "1."
*Chip Enable = Logic "1" to obtain outputs.
Logic Levels:
DTL/TTL (except at MOS/ROM interface). Logic "1," +5.0V, NOM. Logic "0," ground, NOM.
MOS/ROM inputs and outputs. Logic "1," more negative. Logic "0," more positive.

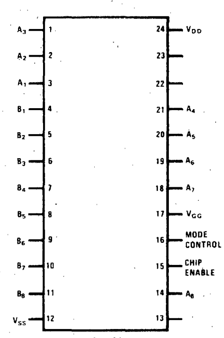
Outputs for circuit shown
Baudot: Logic "0" = "punch"
ASCII: Logic inversion

A typical application showing the ASCII-coded test message as received at a computer terminal.

```
THE QUICK BRØWN FØX JUMPS ØVER THE LAZY DØG 1234567890 DE
THE QUICK BRØWN FØX JUMPS ØVER THE LAZY DØG 1234567890 DE
THE QUICK BRØWN FØX JUMPS ØVER THE LAZY DØG 1234567890 DE
THE QUICK BRØWN FØX JUMPS ØVER THE LAZY DØG 1234567890 DE
THE QUICK BRØWN FØX JUMPS ØVER THE LAZY DØG 1234567890 DE
THE QUICK BKØWN FØX JUKPS ØVER THE LAZY DØG 1234567890 DE
THE QUICK BRØWN FØX JUMPS ØVER THE LAZY DØG 1234567890 DE
THE QUICK BRØWN FØX JUMPS ØVER THE LAZY DØG 1234567890 DE
THE QUICK BRØWN FØX JUMPS ØVER THE LAZY DØG 1234567890 DE
THE QUICK BRØWN FØX JUMPS ØVER THE LAZY DØG 1234567890 DE
THE QUICK BRØWN FØX JUMPS ØVER THE LAZY DØG 1234567890 DE
THE QUICK BRØWN FØX JUMPS ØVER THE LAZY DØG 1234567890 DE
```

connection diagram

Dual-In-Line Package



Order Number MM4220DF/J or MM5220DF/J
See Package 11
Order Number MM5220DF/N
See Package 18

code conversion table

ADDRESS	OUTPUT CHARACTER	OUTPUT CODE (Baudot) –	–	–	5	4	3	2	1	ADDRESS	OUTPUT CHARACTER	OUTPUT CODE (ASCII) PARITY	b_7	b_6	b_5	b_4	b_3	b_2	b_1
0	CR	1	1	1	1	0	1	1	1	64	NULL	0	0	0	0	0	0	0	0
1	CR	1	1	1	1	0	1	1	1	65	CR	0	1	1	1	0	0	1	0
2	LF	1	1	1	1	1	1	0	1	66	CR	0	1	1	1	0	0	1	0
3	Ltr.	1	1	1	0	0	0	0	0	67	LF	1	1	1	1	0	1	0	1
4	T	1	1	1	0	1	1	1	1	68	T	0	0	1	0	1	0	1	1
5	H	1	1	1	0	1	0	1	1	69	H	1	0	1	1	0	1	1	1
6	E	1	1	1	1	1	1	1	0	70	E	0	0	1	1	1	0	1	0
7	SP	1	1	1	1	1	0	1	1	71	SP	0	1	0	1	1	1	1	1
8	Q	1	1	1	0	1	0	0	0	72	Q	0	0	1	0	1	1	1	0
9	U	1	1	1	1	1	0	0	0	73	U	1	0	1	0	1	0	1	0
10	I	1	1	1	1	1	0	0	1	74	I	0	0	1	1	0	1	1	0
11	C	1	1	1	1	0	0	0	1	75	C	0	0	1	1	1	1	0	0
12	K	1	1	1	1	0	0	0	0	76	K	1	0	1	1	0	1	0	0
13	SP	1	1	1	1	1	0	1	1	77	SP	0	1	0	1	1	1	1	1
14	B	1	1	1	0	0	1	1	0	78	B	1	0	1	1	1	1	0	1
15	R	1	1	1	1	0	1	0	1	79	R	0	0	1	0	1	1	0	1
16	O	1	1	1	0	0	1	1	1	80	O	0	0	1	1	0	0	0	0
17	W	1	1	1	0	1	1	0	0	81	W	0	0	1	0	1	0	0	0
18	N	1	1	1	1	0	0	1	1	82	N	1	0	1	1	0	0	0	1
19	SP	1	1	1	1	1	0	1	1	83	SP	0	1	0	1	1	1	1	1
20	F	1	1	1	1	0	0	1	0	84	F	0	0	1	1	1	0	0	1
21	O	1	1	1	0	0	1	1	1	85	O	0	0	1	1	0	0	0	0
22	X	1	1	1	0	0	0	1	0	86	X	0	0	1	0	0	1	1	1
23	SP	1	1	1	1	1	0	1	1	87	SP	0	1	0	1	1	1	1	1
24	J	1	1	1	1	0	1	0	0	88	J	0	0	1	1	0	1	0	1
25	U	1	1	1	1	1	0	0	0	89	U	1	0	1	0	1	0	1	0
26	M	1	1	1	0	0	0	1	1	90	M	1	0	1	1	0	0	1	0
27	P	1	1	1	0	1	0	0	1	91	P	1	0	1	0	1	1	1	1
28	S	1	1	1	1	1	0	1	0	92	S	1	0	1	0	1	1	0	0
29	SP	1	1	1	1	1	0	1	1	93	SP	0	1	0	1	1	1	1	1
30	O	1	1	1	0	0	1	1	1	94	O	0	0	1	1	0	0	0	0
31	V	1	1	1	0	0	0	0	1	95	V	1	0	1	0	1	0	0	1
32	E	1	1	1	1	1	1	1	0	96	E	0	0	1	1	1	0	1	0
33	R	1	1	1	1	0	1	0	1	97	R	0	0	1	0	1	1	0	1
34	SP	1	1	1	1	1	0	1	1	98	SP	0	1	0	1	1	1	1	1
35	T	1	1	1	0	1	1	1	1	99	T	0	0	1	0	1	0	1	1
36	H	1	1	1	0	1	0	1	1	100	H	1	0	1	1	0	1	1	1
37	E	1	1	1	1	1	1	1	0	101	E	0	0	1	1	1	0	1	0
38	SP	1	1	1	1	1	0	1	1	102	SP	0	1	0	1	1	1	1	1
39	L	1	1	1	0	1	1	0	1	103	L	0	0	1	1	0	0	1	1
40	A	1	1	1	1	1	1	0	0	104	A	1	0	1	1	1	1	1	0
41	Z	1	1	1	0	1	1	1	0	105	Z	1	0	1	0	0	1	0	1
42	Y	1	1	1	0	1	0	1	0	106	Y	1	0	1	0	0	1	1	0
43	SP	1	1	1	1	1	0	1	1	107	SP	0	1	0	1	1	1	1	1
44	D	1	1	1	1	0	1	1	0	108	D	1	0	1	1	1	0	1	1
45	O	1	1	1	0	0	1	1	1	109	O	0	0	1	1	0	0	0	0
46	G	1	1	1	0	0	1	0	1	110	G	1	0	1	1	1	0	0	0
47	SP	1	1	1	1	1	0	1	1	111	SP	0	1	0	1	1	1	1	1
48	Fig.	1	1	1	0	0	1	0	0	112	1	0	1	0	0	1	1	1	0
49	1	1	1	1	0	1	0	0	0	113	2	0	1	0	0	1	1	0	1
50	2	1	1	1	0	1	1	0	0	114	3	1	1	0	0	1	1	0	0
51	3	1	1	1	1	1	1	1	0	115	4	0	1	0	0	1	0	1	1
52	4	1	1	1	1	0	1	0	1	116	5	1	1	0	0	1	0	1	0
53	5	1	1	1	0	1	1	1	1	117	6	1	1	0	0	1	0	0	1
54	6	1	1	1	0	1	0	1	0	118	7	0	1	0	0	1	0	0	0
55	7	1	1	1	1	1	0	0	0	119	8	0	1	0	0	0	1	1	1
56	8	1	1	1	1	1	0	0	1	120	9	1	1	0	0	0	1	1	0
57	9	1	1	1	0	0	1	1	1	121	0	1	1	0	0	1	1	1	1
58	0	1	1	1	0	1	0	0	1	122	SP	0	1	0	1	1	1	1	1
59	SP	1	1	1	1	1	0	1	1	123	D	1	0	1	1	1	0	1	1
60	Ltr.	1	1	1	0	0	0	0	0	124	E	0	0	1	1	1	0	1	0
61	D	1	1	1	1	0	1	1	0	125	SP	0	1	0	1	1	1	1	1
62	E	1	1	1	1	1	1	1	0	126	DEL	0	0	0	0	0	0	0	0
63	SP	1	1	1	1	1	0	1	1	127	DEL	0	0	0	0	0	0	0	0
		B8	B7	B6	B5	B4	B3	B2	B1			B8	B7	B6	B5	B4	B3	B2	B1
		Baudot: Logic "0" = "punch"										ASCII: Logic inversion							

SP = Space

Note: When chip enable input is at a logical 0, all outputs are at a logical 1.

NATIONAL

MOS ROMs

MM4220EK/MM5220EK
BCDIC-to-EBCDIC and ASCII-to-EBCDIC code converter

general description

The MM4220EK/MM5220EK is a 1024-bit read only memory that has been programmed to convert both Binary Coded Decimal Interchange Code (BCDIC) and the American Standard Code for Information Interchange (ASCII) to Extended Binary Coded Decimal Interchange Code (EBCDIC).

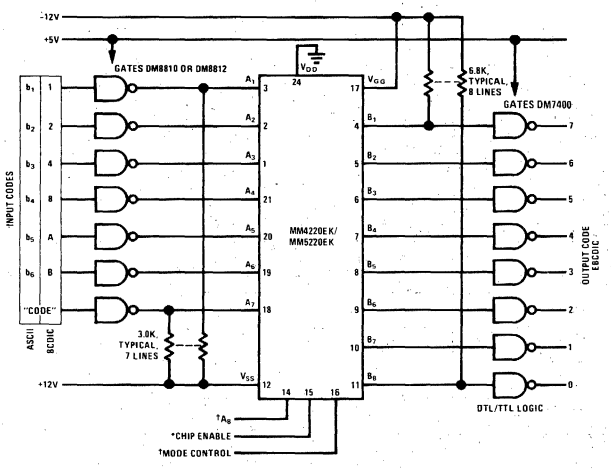
The BCDIC-to-EBCDIC converter is located in the first 64 8-bit bytes of the ROM. The unused parity check bit (the most significant input BCDIC bit) is always a "0".

The ASCII-to-EBCDIC converter is located in the second 64 8-bit bytes of the ROM. Thus, the input ASCII code in addresses 64 through 127 has a "1" in the most significant (A_7) bit which is used with the selection logic. The resulting 6-bit ASCII input is for display–only upper case and numerical codes, since it will not accept the control commands or the lower case characters.

device characteristics

For full electrical, environmental and mechanical details, refer to the MM4220/MM5220 1024-bit read only memory data sheet.

typical application



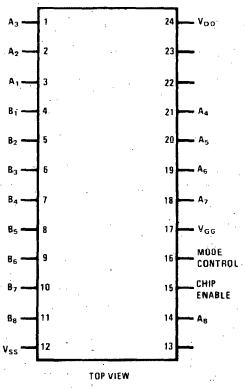
†Mode Control = Logic "0," A_8 = Logic "1."

*Chip Enable = Logic "1" to obtain outputs.

Logic Levels:
DTL/TTL (except at MOS/ROM interface). Logic "1," +5.0V, NOM. Logic "0," ground, NOM.
MOS/ROM inputs and outputs. Logic "1," more negative. Logic "0," more positive.

connection diagram

Dual-In-Line Package



Order Number MM4220EK/J or MM5220EK/J
See Package 11

Order Number MM5220EK/N
See Package 18

code conversion tables

ROM ADDRESS	FUNCTION		CODE															
	INPUT	OUTPUT	INPUT							OUTPUT								
	BCDIC SYMBOL	EBCDIC SYMBOL	CODE	BCDIC B	A	8	4	2	1	EBCDIC 0	1	2	3	4	5	6	7
0	Space	Space	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
1	1	1	0	0	0	0	0	0	1	1	1	1	1	0	0	0	1
2	2	2	0	0	0	0	0	1	0	1	1	1	1	0	0	1	0
3	3	3	0	0	0	0	0	1	1	1	1	1	1	0	0	1	1
4	4	4	0	0	0	0	1	0	0	1	1	1	1	0	1	0	0
5	5	5	0	0	0	0	1	0	1	1	1	1	1	0	1	0	1
6	6	6	0	0	0	0	1	1	0	1	1	1	1	0	1	1	0
7	7	7	0	0	0	0	1	1	1	1	1	1	1	0	1	1	1
8	8	8	0	0	0	1	0	0	0	1	1	1	1	1	0	0	0
9	9	9	0	0	0	1	0	0	1	1	1	1	1	1	0	0	1
10	0	0	0	0	0	1	0	1	0	1	1	1	1	0	0	0	0
11	# or =	#	0	0	0	1	0	1	1	0	1	1	1	1	0	1	1
12	@ or '	@	0	0	0	1	1	0	0	0	1	1	1	1	1	0	0
13	:	:	0	0	0	1	1	0	1	0	1	1	1	1	0	1	0
14	>	>	0	0	0	1	1	1	0	0	1	1	0	1	1	1	0
15	√(TM)	TM	0	0	0	1	1	1	1	0	0	0	1	0	0	1	1
16	Space	Space	0	0	1	0	0	0	0	0	1	0	0	0	0	0	0
17	/	/	0	0	1	0	0	0	1	0	1	1	0	0	0	0	1
18	S	S	0	0	1	0	0	1	0	1	1	1	0	0	0	1	0
19	T	T	0	0	1	0	0	1	1	1	1	1	0	0	0	1	1
20	U	U	0	0	1	0	1	0	0	1	1	1	0	0	1	0	0
21	V	V	0	0	1	0	1	0	1	1	1	1	0	0	1	0	1
22	W	W	0	0	1	0	1	1	0	1	1	1	0	0	1	1	0
23	X	X	0	0	1	0	1	1	1	1	1	1	0	0	1	1	1
24	Y	Y	0	0	1	1	0	0	0	1	1	1	0	1	0	0	0
25	Z	Z	0	0	1	1	0	0	1	1	1	1	0	1	0	0	1
26	‡(RM)	RM	0	0	1	1	0	1	0	1	1	1	0	0	0	0	0
27	,	,	0	0	1	1	0	1	1	0	1	1	0	1	0	1	1
28	% or (	%	0	0	1	1	1	0	0	0	1	1	0	1	1	0	0
29	∨	+	0	0	1	1	1	0	1	0	1	0	0	1	1	1	0
30	\	¢	0	0	1	1	1	1	0	0	1	0	0	1	0	1	0
31	≠	=	0	0	1	1	1	1	1	0	1	1	1	1	1	1	0
32	-	-	0	1	0	0	0	0	0	0	1	1	0	0	0	0	0
33	J	J	0	1	0	0	0	0	1	1	1	0	1	0	0	0	1
34	K	K	0	1	0	0	0	1	0	1	1	0	1	0	0	1	0
35	L	L	0	1	0	0	0	1	1	1	1	0	1	0	0	1	1
36	M	M	0	1	0	0	1	0	0	1	1	0	1	0	1	0	0
37	N	N	0	1	0	0	1	0	1	1	1	0	1	0	1	0	1
38	O	O	0	1	0	0	1	1	0	1	1	0	1	0	1	1	0
39	P	P	0	1	0	0	1	1	1	1	1	0	1	0	1	1	1
40	Q	Q	0	1	0	1	0	0	0	1	1	0	1	1	0	0	0
41	R	R	0	1	0	1	0	0	1	1	1	0	1	1	0	0	1
42	!	!	0	1	0	1	0	1	0	0	1	0	1	1	0	1	0
43	$	$	0	1	0	1	0	1	1	0	1	0	1	1	0	1	1
44	*	*	0	1	0	1	1	0	0	0	1	0	1	1	1	0	0
45	]	)	0	1	0	1	1	0	1	0	1	0	1	1	1	0	1
46	;	;	0	1	0	1	1	1	0	0	1	0	1	1	1	1	0
47	△	"	0	1	0	1	1	1	1	0	1	1	1	1	1	1	1
48	& or +	&	0	1	1	0	0	0	0	0	1	0	1	0	0	0	0
49	A	A	0	1	1	0	0	0	1	1	1	0	0	0	0	0	1
50	B	B	0	1	1	0	0	1	0	1	1	0	0	0	0	1	0
51	C	C	0	1	1	0	0	1	1	1	1	0	0	0	0	1	1
52	D	D	0	1	1	0	1	0	0	1	1	0	0	0	1	0	0
53	E	E	0	1	1	0	1	0	1	1	1	0	0	0	1	0	1
54	F	F	0	1	1	0	1	1	0	1	1	0	0	0	1	1	0
55	G	G	0	1	1	0	1	1	1	1	1	0	0	0	1	1	1
56	H	H	0	1	1	1	0	0	0	1	1	0	0	1	0	0	0
57	I	I	0	1	1	1	0	0	1	1	1	0	0	1	0	0	1
58	?	?	0	1	1	1	0	1	0	0	1	1	0	1	1	1	1
59	.	.	0	1	1	1	0	1	1	0	1	0	0	1	0	1	1
60	¤ or)	¤	0	1	1	1	1	0	0	0	1	1	0	1	0	1	0
61	[	(	0	1	1	1	1	0	1	0	1	0	0	1	1	0	1
62	<	<	0	1	1	1	1	1	0	0	1	0	0	1	1	0	0
63	‡	'	0	1	1	1	1	1	1	0	1	1	1	1	1	0	1

code conversion tables(con't)

ROM ADDRESS	FUNCTION INPUT ASCII SYMBOL	FUNCTION OUTPUT EBCDIC SYMBOL	CODE INPUT CODE	INPUT ASCII b_6	b_5	b_4	b_3	b_2	b_1	OUTPUT EBCDIC 0	1	2	3	4	5	6	7
64	@	@	1	0	0	0	0	0	0	0	1	1	1	1	1	0	0
65	A	A	1	0	0	0	0	0	1	1	1	0	0	0	0	0	1
66	B	B	1	0	0	0	0	1	0	1	1	0	0	0	0	1	0
67	C	C	1	0	0	0	0	1	1	1	1	0	0	0	0	1	1
68	D	D	1	0	0	0	1	0	0	1	1	0	0	0	1	0	0
69	E	E	1	0	0	0	1	0	1	1	1	0	0	0	1	0	1
70	F	F	1	0	0	0	1	1	0	1	1	0	0	0	1	1	0
71	G	G	1	0	0	0	1	1	1	1	1	0	0	0	1	1	1
72	H	H	1	0	0	1	0	0	0	1	1	0	0	1	0	0	0
73	I	I	1	0	0	1	0	0	1	1	1	0	0	1	0	0	1
74	J	J	1	0	0	1	0	1	0	1	1	0	1	0	0	0	1
75	K	K	1	0	0	1	0	1	1	1	1	0	1	0	0	1	0
76	L	L	1	0	0	1	1	0	0	1	1	0	1	0	0	1	1
77	M	M	1	0	0	1	1	0	1	1	1	0	1	0	1	0	0
78	N	N	1	0	0	1	1	1	0	1	1	0	1	0	1	0	1
79	O	O	1	0	0	1	1	1	1	1	1	0	1	0	1	1	0
80	P	P	1	0	1	0	0	0	0	1	1	0	1	0	1	1	1
81	Q	Q	1	0	1	0	0	0	1	1	1	0	1	1	0	0	0
82	R	R	1	0	1	0	0	1	0	1	1	0	1	1	0	0	1
83	S	S	1	0	1	0	0	1	1	1	1	1	0	0	0	1	0
84	T	T	1	0	1	0	1	0	0	1	1	1	0	0	0	1	1
85	U	U	1	0	1	0	1	0	1	1	1	1	0	0	1	0	0
86	V	V	1	0	1	0	1	1	0	1	1	1	0	0	1	0	1
87	W	W	1	0	1	0	1	1	1	1	1	1	0	0	1	1	0
88	X	X	1	0	1	1	0	0	0	1	1	1	0	0	1	1	1
89	Y	Y	1	0	1	1	0	0	1	1	1	1	0	1	0	0	0
90	Z	Z	1	0	1	1	0	1	0	1	1	1	0	1	0	0	1
91	[	(	1	0	1	1	0	1	1	0	1	0	0	1	1	0	1
92	\	\	1	0	1	1	1	0	0	0	1	0	0	0	0	0	0
93	]	)	1	0	1	1	1	0	1	0	1	0	1	1	1	0	1
94	⌒ or ^	¬	1	0	1	1	1	1	0	0	1	0	1	1	1	1	1
95	—	—	1	0	1	1	1	1	1	0	1	1	0	1	1	0	1
96	Space	Space	1	1	0	0	0	0	0	0	1	0	0	0	0	0	0
97	!	!	1	1	0	0	0	0	1	0	1	0	1	1	0	1	0
98	"	"	1	1	0	0	0	1	0	0	1	1	1	1	1	1	1
99	#	#	1	1	0	0	0	1	1	0	1	1	1	1	0	1	1
100	$	$	1	1	0	0	1	0	0	0	1	0	1	1	0	1	1
101	%	%	1	1	0	0	1	0	1	0	1	1	0	1	1	0	0
102	&	&	1	1	0	0	1	1	0	0	1	0	1	0	0	0	0
103	'	'	1	1	0	0	1	1	1	0	1	1	1	1	1	0	1
104	(	(	1	1	0	1	0	0	0	0	1	0	0	1	1	0	1
105	)	)	1	1	0	1	0	0	1	0	1	0	1	1	1	0	1
106	*	*	1	1	0	1	0	1	0	0	1	0	1	1	1	0	0
107	+	+	1	1	0	1	0	1	1	0	1	0	0	1	1	1	0
108	,	,	1	1	0	1	1	0	0	0	1	1	0	1	0	1	1
109	-	-	1	1	0	1	1	0	1	0	1	1	0	0	0	0	0
110	.	.	1	1	0	1	1	1	0	0	1	0	0	1	0	1	1
111	/	/	1	1	0	1	1	1	1	0	1	1	0	0	0	0	1
112	0	0	1	1	1	0	0	0	0	1	1	1	1	0	0	0	0
113	1	1	1	1	1	0	0	0	1	1	1	1	1	0	0	0	1
114	2	2	1	1	1	0	0	1	0	1	1	1	1	0	0	1	0
115	3	3	1	1	1	0	0	1	1	1	1	1	1	0	0	1	1
116	4	4	1	1	1	0	1	0	0	1	1	1	1	0	1	0	0
117	5	5	1	1	1	0	1	0	1	1	1	1	1	0	1	0	1
118	6	6	1	1	1	0	1	1	0	1	1	1	1	0	1	1	0
119	7	7	1	1	1	0	1	1	1	1	1	1	1	0	1	1	1
120	8	8	1	1	1	1	0	0	0	1	1	1	1	1	0	0	0
121	9	9	1	1	1	1	0	0	1	1	1	1	1	1	0	0	1
122	:	:	1	1	1	1	0	1	0	0	1	1	1	1	0	1	0
123	;	;	1	1	1	1	0	1	1	0	1	0	1	1	1	1	0
124	<	<	1	1	1	1	1	0	0	0	1	0	0	1	1	0	0
125	=	=	1	1	1	1	1	0	1	0	1	1	1	1	1	1	0
126	>	>	1	1	1	1	1	1	0	0	1	1	0	1	1	1	0
127	?	?	1	1	1	1	1	1	1	0	1	1	0	1	1	1	1

MOS ROMs

MM4220LR/MM5220LR BCDIC to ASCII-7/ ASCII-7 to BCDIC code converter

general description

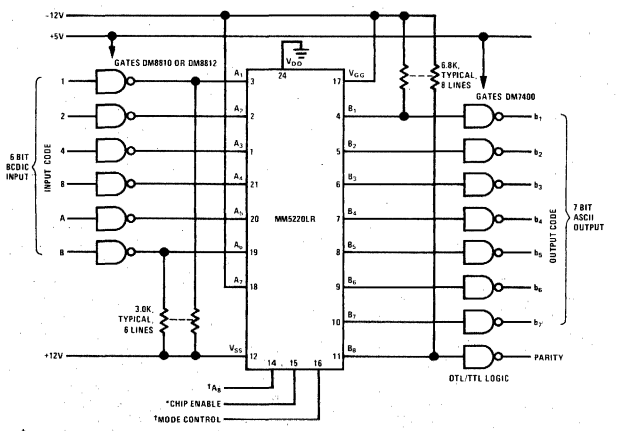
The MM4220LR/MM5220LR is a 128 x 8 read only memory which has been programmed to convert the 64 characters of the Binary Coded Decimal Interchange Code (BCDIC) to the American Standard code for Information Interchange in seven bits (ASCII-7).

The first half of the ROM, from address 0 to address 63, converts the 64 character ASCII graphic subset to BCDIC. The tables show the character assignments and their binary equivalents.

For electrical, environmental and mechanical details, refer to the MM4220/MM5220 data sheet.

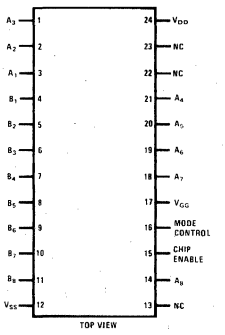
typical applications and connection diagram

BCDIC to ASCII



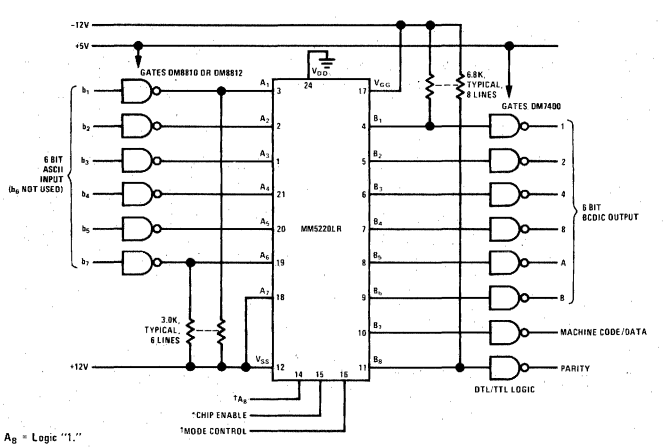
†Mode Control = Logic "0," A_8 = Logic "1."
*Chip Enable = Logic "1" to obtain outputs.
Logic Levels:
DTL/TTL (except at MOS/ROM interface). Logic "1," +5.0V, NOM. Logic "0," ground, NOM.
MOS/ROM inputs and outputs. Logic "1," more negative. Logic "0," more positive.

Dual-In-Line Package



Order Number MM4220LR/J or MM5220LR/J
See Package 11
Order Number MM5220LR/N
See Package 18

ASCII to BCDIC



†Mode Control = Logic "0," A_8 = Logic "1."
*Chip Enable = Logic "1" to obtain outputs.
Logic Levels:
DTL/TTL (except at MOS/ROM interface). Logic "1," +5.0V, NOM. Logic "0," ground, NOM.
MOS/ROM inputs and outputs. Logic "1," more negative. Logic "0," more positive.

code conversion tables

ASCII to BCDIC

ROM ADDRESS	FUNCTION INPUT ASCII SYMBOL	FUNCTION OUTPUT BCDIC SYMBOL	CODE																
				INPUT ASCII							OUTPUT BCDIC								
			CODE	b_7	b_5	b_4	b_3	b_2	b_1	MC/ DATA	EP	B	A	8	4	2	1
0	SP	SP	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
1	!	!	0	0	0	0	0	0	1	0	1	1	0	1	0	1	0		
2	"	+++	0	0	0	0	0	1	0	0	1	0	1	1	1	1	1		
3	#	#	0	0	0	0	0	1	1	0	1	0	0	1	0	1	1		
4	$	$	0	0	0	0	1	0	0	0	0	1	0	1	0	1	1		
5	%	%	0	0	0	0	1	0	1	0	1	0	1	1	1	0	0		
6	&	&	0	0	0	0	1	1	0	0	0	1	1	0	0	0	0		
7	'	V	0	0	0	0	1	1	1	0	0	0	1	1	1	0	1		
8	(	Blank	0	0	0	1	0	0	0	0	1	0	1	0	0	0	0		
9	)	Δ	0	0	0	1	0	0	1	0	1	1	0	1	1	1	1		
10	*	*	0	0	0	1	0	1	0	0	1	1	0	1	1	0	0		
11	VT	‡	0	0	0	1	0	1	1	1	0	0	1	1	0	1	0		
12	,	,	0	0	0	1	1	0	0	0	0	0	1	1	0	1	1		
13	CR	‡	0	0	0	1	1	0	1	1	1	1	1	1	1	1	1		
14	.	.	0	0	0	1	1	1	0	0	1	1	1	1	0	1	1		
15	/	/	0	0	0	1	1	1	1	0	0	0	1	0	0	0	1		
16	0	0	0	0	1	0	0	0	0	0	0	0	0	1	0	1	0		
17	1	1	0	0	1	0	0	0	1	0	1	0	0	0	0	0	1		
18	2	2	0	0	1	0	0	1	0	0	1	0	0	0	0	1	0		
19	3	3	0	0	1	0	0	1	1	0	0	0	0	0	0	1	1		
20	4	4	0	0	1	0	1	0	0	0	1	0	0	0	1	0	0		
21	5	5	0	0	1	0	1	0	1	0	0	0	0	0	1	0	1		
22	6	6	0	0	1	0	1	1	0	0	0	0	0	0	1	1	0		
23	7	7	0	0	1	0	1	1	1	0	1	0	0	0	1	1	1		
24	8	8	0	0	1	1	0	0	0	0	1	0	0	1	0	0	0		
25	9	9	0	0	1	1	0	0	1	0	0	0	0	1	0	0	1		
26	:	:	0	0	1	1	0	1	0	0	1	0	0	1	1	0	1		
27	;	;	0	0	1	1	0	1	1	0	0	1	0	1	1	1	0		
28	<	<	0	0	1	1	1	0	0	0	1	1	1	1	1	1	0		
29	=	√	0	0	1	1	1	0	1	0	0	0	0	1	1	1	1		
30	>	>	0	0	1	1	1	1	0	0	1	0	0	1	1	1	0		
31	?	?	0	0	1	1	1	1	1	0	0	1	1	1	0	1	0		
32	@	@	0	1	0	0	0	0	0	0	0	0	0	1	1	0	0		
33	A	A	0	1	0	0	0	0	1	0	1	1	1	0	0	0	1		
34	B	B	0	1	0	0	0	1	0	0	1	1	1	0	0	1	0		
35	C	C	0	1	0	0	0	1	1	0	0	1	1	0	0	1	1		
36	D	D	0	1	0	0	1	0	0	0	1	1	1	0	1	0	0		
37	E	E	0	1	0	0	1	0	1	0	0	1	1	0	1	0	1		
38	F	F	0	1	0	0	1	1	0	0	0	1	1	0	1	1	0		
39	G	G	0	1	0	0	1	1	1	0	1	1	1	0	1	1	1		
40	H	H	0	1	0	1	0	0	0	0	1	1	1	1	0	0	0		
41	I	I	0	1	0	1	0	0	1	0	0	1	1	1	0	0	1		
42	J	J	0	1	0	1	0	1	0	0	0	1	0	0	0	0	1		
43	K	K	0	1	0	1	0	1	1	0	0	1	0	0	0	1	0		
44	L	L	0	1	0	1	1	0	0	0	1	1	0	0	0	1	1		
45	M	M	0	1	0	1	1	0	1	0	0	1	0	0	1	0	0		
46	N	N	0	1	0	1	1	1	0	0	1	1	0	0	1	0	1		
47	O	O	0	1	0	1	1	1	1	0	1	1	0	0	1	1	0		
48	P	P	0	1	1	0	0	0	0	0	0	1	0	0	1	1	1		
49	Q	Q	0	1	1	0	0	0	1	0	0	1	0	1	0	0	0		
50	R	R	0	1	1	0	0	1	0	0	1	1	0	1	0	0	1		
51	S	S	0	1	1	0	0	1	1	0	0	0	1	0	0	1	0		
52	T	T	0	1	1	0	1	0	0	0	1	0	1	0	0	1	1		
53	U	U	0	1	1	0	1	0	1	0	0	0	1	0	1	0	0		
54	V	V	0	1	1	0	1	1	0	0	1	0	1	0	1	0	1		
55	W	W	0	1	1	0	1	1	1	0	1	0	1	0	1	1	0		
56	X	X	0	1	1	1	0	0	0	0	0	0	1	0	1	1	1		
57	Y	Y	0	1	1	1	0	0	1	0	0	0	1	1	0	0	0		
58	Z	Z	0	1	1	1	0	1	0	0	1	0	1	1	0	0	1		
59	[	[	0	1	1	1	0	1	1	0	1	1	1	1	0	1	1		
60	\	\	0	1	1	1	1	0	0	0	0	0	1	1	1	1	0		
61	]	]	0	1	1	1	1	0	1	0	0	1	0	1	1	0	1		
62	^	¤	0	1	1	1	1	1	0	0	0	0	1	1	1	0	0		
63	–	-	0	1	1	1	1	1	1	0	1	1	0	0	0	0	0		
			A_7	A_6	A_5	A_4	A_3	A_2	A_1	B_8	B_7	B_6	B_5	B_4	B_3	B_2	B_1		

code conversion tables(con't)

BCDIC to ASCII

ROM ADDRESS	FUNCTION INPUT BCDIC, SYMBOL	FUNCTION OUTPUT ASCII SYMBOL	CODE INPUT BCDIC CODE	B	A	8	4	2	1	PARITY	OUTPUT ASCII b_7	b_6	b_5	b_4	b_3	b_2	b_1
64	SP	SP	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0
65	1	1	1	0	0	0	0	0	1	1	0	1	1	0	0	0	1
66	2	2	1	0	0	0	0	1	0	1	0	1	1	0	0	1	0
67	3	3	1	0	0	0	0	1	1	0	0	1	1	0	0	1	1
68	4	4	1	0	0	0	1	0	0	1	0	1	1	0	1	0	0
69	5	5	1	0	0	0	1	0	1	0	0	1	1	0	1	0	1
70	6	6	1	0	0	0	1	1	0	0	0	1	1	0	1	1	0
71	7	7	1	0	0	0	1	1	1	1	0	1	1	0	1	1	1
72	8	8	1	0	0	1	0	0	0	1	0	1	1	1	0	0	0
73	9	9	1	0	0	1	0	0	1	0	0	1	1	1	0	0	1
74	0	0	1	0	0	1	0	1	0	0	0	1	1	0	0	0	0
75	#	#	1	0	0	1	0	1	1	1	0	1	0	0	0	1	1
76	@	@	1	0	0	1	1	0	0	1	1	0	0	0	0	0	0
77	:	:	1	0	0	1	1	0	1	0	0	1	1	1	0	1	0
78	>	>	1	0	0	1	1	1	0	1	0	1	1	1	1	1	0
79	√	=	1	0	0	1	1	1	1	1	0	1	1	1	1	0	1
80	Blank	(	1	0	1	0	0	0	0	0	0	1	0	1	0	0	0
81	/	/	1	0	1	0	0	0	1	1	0	1	0	1	1	1	1
82	S	S	1	0	1	0	0	1	0	0	1	0	1	0	0	1	1
83	T	T	1	0	1	0	0	1	1	1	1	0	1	0	1	0	0
84	U	U	1	0	1	0	1	0	0	0	1	0	1	0	1	0	1
85	V	V	1	0	1	0	1	0	1	0	1	0	1	0	1	1	0
86	W	W	1	0	1	0	1	1	0	1	1	0	1	0	1	1	1
87	X	X	1	0	1	0	1	1	1	1	1	0	1	1	0	0	0
88	Y	Y	1	0	1	1	0	0	0	0	1	0	1	1	0	0	1
89	Z	Z	1	0	1	1	0	0	1	0	1	0	1	1	0	1	0
90	‡	VT	1	0	1	1	0	1	0	1	0	0	0	1	0	1	1
91	,	,	1	0	1	1	0	1	1	1	0	1	0	1	1	0	0
92	%	%	1	0	1	1	1	0	0	1	0	1	0	0	1	0	1
93	V	'	1	0	1	1	1	0	1	0	0	1	0	0	1	1	1
94	\	\	1	0	1	1	1	1	0	0	1	0	1	1	1	0	0
95	+++	"	1	0	1	1	1	1	1	0	0	1	0	0	0	1	0
96	–	–	1	1	0	0	0	0	0	0	1	0	1	1	1	1	1
97	J	J	1	1	0	0	0	0	1	1	1	0	0	1	0	1	0
98	K	K	1	1	0	0	0	1	0	0	1	0	0	1	0	1	1
99	L	L	1	1	0	0	0	1	1	1	1	0	0	1	1	0	0
100	M	M	1	1	0	0	1	0	0	0	1	0	0	1	1	0	1
101	N	N	1	1	0	0	1	0	1	0	1	0	0	1	1	1	0
102	O	O	1	1	0	0	1	1	0	1	1	0	0	1	1	1	1
103	P	P	1	1	0	0	1	1	1	0	1	0	1	0	0	0	0
104	Q	Q	1	1	0	1	0	0	0	1	1	0	1	0	0	0	1
105	R	R	1	1	0	1	0	0	1	1	1	0	1	0	0	1	0
106	!	!	1	1	0	1	0	1	0	0	0	1	0	0	0	0	1
107	$	$	1	1	0	1	0	1	1	0	0	1	0	0	1	0	0
108	*	*	1	1	0	1	1	0	0	1	0	1	0	1	0	1	0
109	]	]	1	1	0	1	1	0	1	1	1	0	1	1	1	0	1
110	;	;	1	1	0	1	1	1	0	1	0	1	1	1	0	1	1
111	Δ	)	1	1	0	1	1	1	1	1	0	1	0	1	0	0	1
112	&	&	1	1	1	0	0	0	0	1	0	1	0	0	1	1	0
113	A	A	1	1	1	0	0	0	1	0	1	0	0	0	0	0	1
114	B	B	1	1	1	0	0	1	0	0	1	0	0	0	0	1	0
115	C	C	1	1	1	0	0	1	1	1	1	0	0	0	0	1	1
116	D	D	1	1	1	0	1	0	0	0	1	0	0	0	1	0	0
117	E	E	1	1	1	0	1	0	1	1	1	0	0	0	1	0	1
118	F	F	1	1	1	0	1	1	0	1	1	0	0	0	1	1	0
119	G	G	1	1	1	0	1	1	1	0	1	0	0	0	1	1	1
120	H	H	1	1	1	1	0	0	0	0	1	0	0	1	0	0	0
121	I	I	1	1	1	1	0	0	1	1	1	0	0	1	0	0	1
122	?	?	1	1	1	1	0	1	0	0	0	1	1	1	1	1	1
123	.	.	1	1	1	1	0	1	1	0	0	1	0	1	1	1	0
124	¤	∩	1	1	1	1	1	0	0	1	1	0	1	1	1	1	0
125	[	[	1	1	1	1	1	0	1	1	1	0	1	1	0	1	1
126	<	<	1	1	1	1	1	1	0	0	0	1	1	1	1	0	0
127	‡	CR	1	1	1	1	1	1	1	1	0	0	0	1	1	0	1
			A_7	A_6	A_5	A_4	A_3	A_2	A_1	B_8	B_7	B_6	B_5	B_4	B_3	B_2	B_1

NATIONAL

MM4220NP/MM5220NP, MM4230NN/MM5230NN, MM4230NO/MM5230NO, 7×9 horizontal scan display character generator

general description

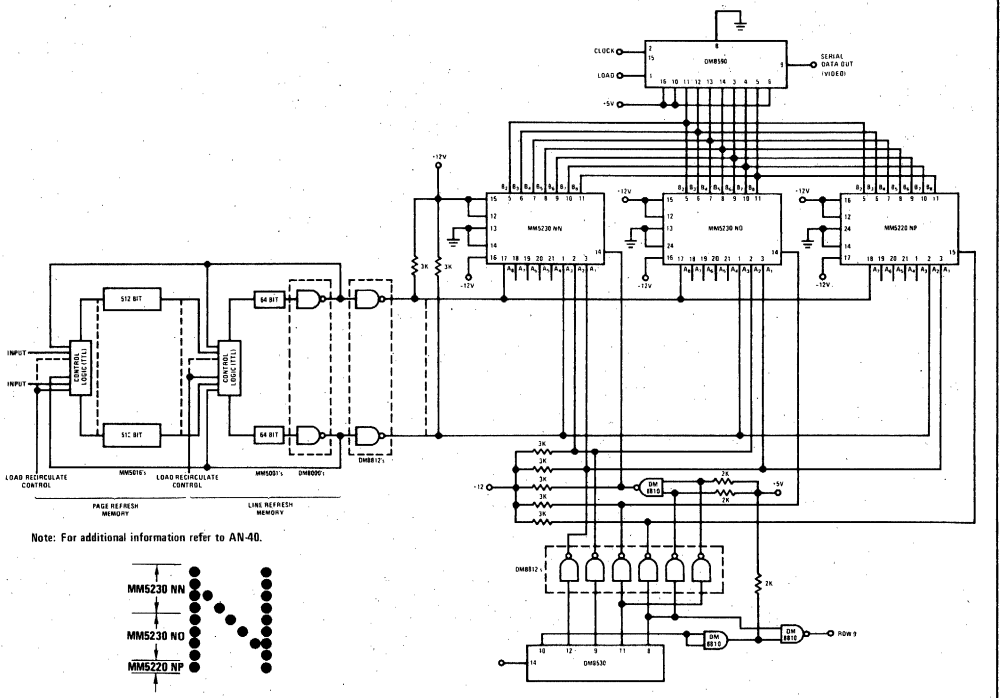
The MM4220NP/MM5220NP is a 1024-bit read-only memory and the MM4230NN/MM5230NN and MM4230NO/MM5230NO are 2048-bit read-only memories programmed to generate a font of 64 7x9 dot-type raster or horizontal-scan characters.

The typical application shows the ASCII-address system. The display refresh memory, built with MOS dynamic shift registers, and the TTL control techniques are similar to those described in *Application Note AN-40*. Designs for vertical-scan fonts, printer character generators, and designs for fonts larger than 7x9 are also outlined in *AN-40*.

For full electrical, environmental and mechanical details, refer to the MM4220/MM5220 and MM4230/MM5230 data sheets.

typical application

7x9 Character Generator System

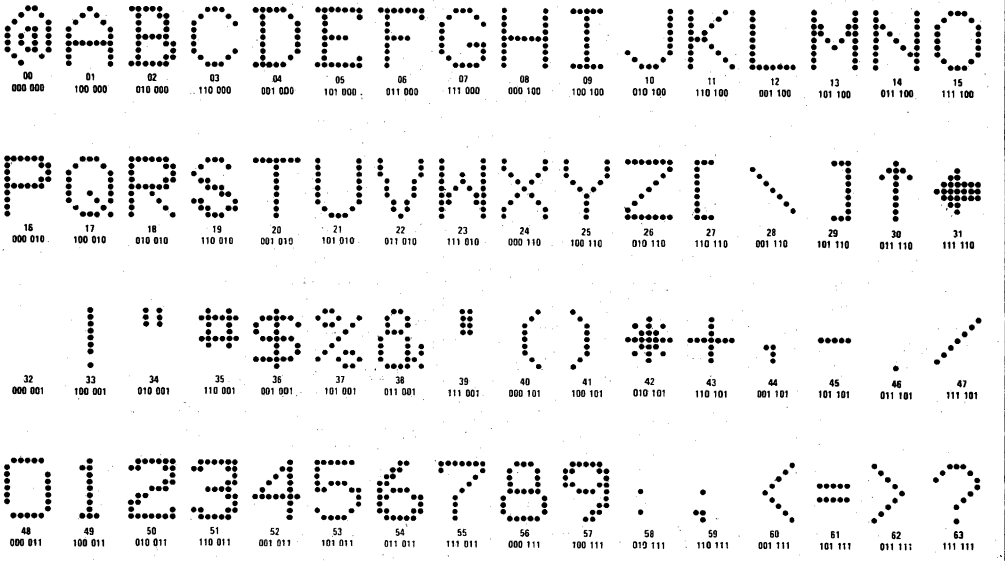


Note: For additional information refer to AN-40.

Order Number MM4220NP/J, MM5220NP/J, MM4230NN/J, MM5230NN/J, MM4230NO/J, or MM5230NO/J
See Package 11

Order Number MM5220NP/N, MM5230NN/N, or MM5230NO/N
See Package 18

character font



Note: Input addresses are in six bit ASCII code and are shown in the sequence $A_0, A_1 \ldots A_5$.

NATIONAL

MOS ROMs

MM4221/MM5221 1024-bit read only memory

general description

The MM4221/MM5221 is a 1024-bit static read only memory. It is a P-channel enhancement mode monolithic MOS integrated circuit utilizing low threshold voltage technology. The device is a non-volatile memory organized as 128-8-bit words or 256-4-bit words. Programming of the memory contents is accomplished by changing one mask during the device fabrication.

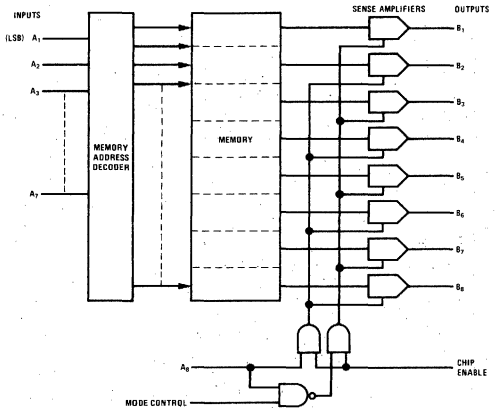
features

- Bipolar compatibility — +5V, −12V operation
- High speed operation — <700 ns typ
- Static operation — no clocks required
- Common data busing — output wire AND capability
- Chip enable output control

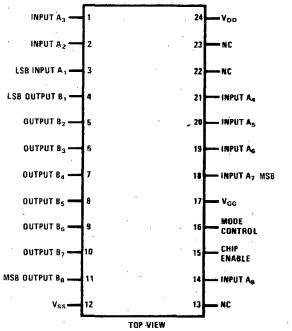
applications

- Code conversion
- Random logic synthesis
- Table look-up
- Character generators
- Microprogramming.

block and connection diagrams



Dual-In-Line Package



Order Number MM4221J or MM5221J
See Package 11
Order Number MM5221N
See Package 18

Note: For programming information see AN-100.

absolute maximum ratings

V_{GG} Supply Voltage	V_{SS} – 20V
V_{DD} Supply Voltage	V_{SS} – 20V
Input Voltage	$(V_{SS} - 20)V < V_{IN} < (V_{SS} + 0.3)V$
Storage Temperature	–65°C to +150°C
Operating Temperature MM4221	–55°C to +125°C
MM5221	0°C to +70°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics

T_A within operating temperature range, V_{SS} = +5V ±5%, V_{GG} = V_{DD} = –12V ±5%, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage Levels					
MOS to TTL					
Logical "1"	6.8 kΩ ±5% to V_{GG} Plus One			+0.4	V
Logical "0"	Standard Series 54/74 Gate	+2.4			V
Output Current Capability					
Logical "0"	V_{OUT} = 2.4V	2.5			mA
Input Voltage Levels					
Logical "1"				V_{SS} – 4.2	V
Logical "0"		V_{SS} – 2.0			V
Power Supply Current	T_A = 25°C				
I_{DD}	V_{SS} = +5V		6.5	12.0	mA
I_{GG} (Note 1)	V_{GG} = V_{DD} = –12V			1	μA
Input Leakage	V_{IN} = V_{SS} – 12V			1	μA
Input Capacitance	f = 1.0 MHz, V_{IN} = 0V		5		pF
V_{GG} Capacitance (Note 4)	f = 1.0 MHz, V_{IN} = 0V		15	25	pF
Address Time (Note 2)	See Timing Diagram				
T_{ACCESS}	T_A = 25°C, V_{SS} = 5V, V_{GG} = V_{DD} = –12V		700	950	ns
Output AND Connections (Note 3)	6.8 kΩ ±5% to V_{GG} Plus One Standard Series 54/74 Gate			8	

Note 1: The V_{GG} supply may be clocked to reduce device power without affecting access time.

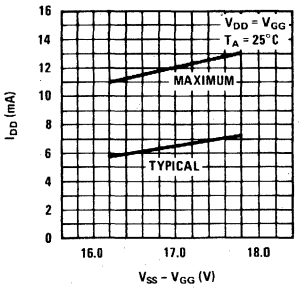
Note 2: Address time is measured from the change of data on any input except mode control or Chip Enable line to the output of a TTL gate. (See Timing Diagram). See curves for guaranteed limit over temperature.

Note 3: The address time in the TTL load configuration follows the equation:
T_{ACCESS} = The specified limit + (N – 1) (50) ns
Where N = Number of AND connections.

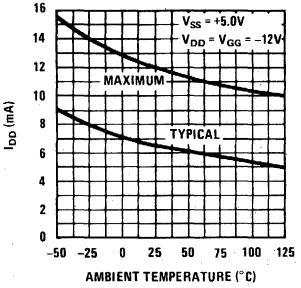
Note 4: Capacitance guaranteed by design.

performance characteristics

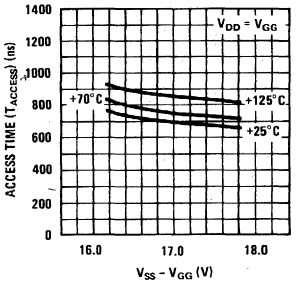
Power Supply Current vs
Power Supply Voltages



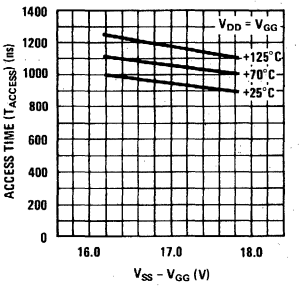
Power Supply Current vs
Ambient Temperature



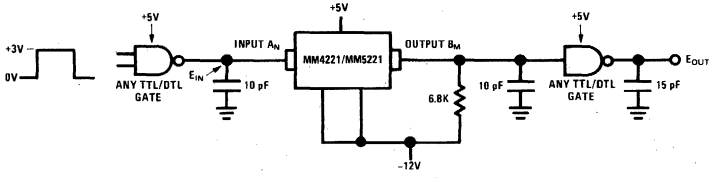
Typical Access Time vs
Power Supply Voltages

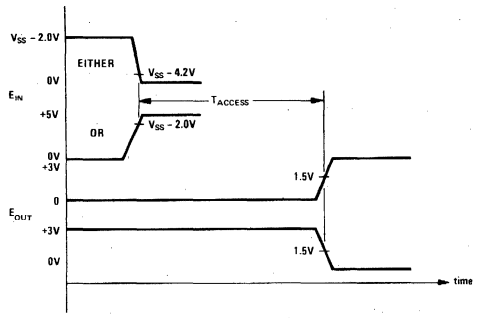


Guaranteed Access Time vs
Power Supply Voltages



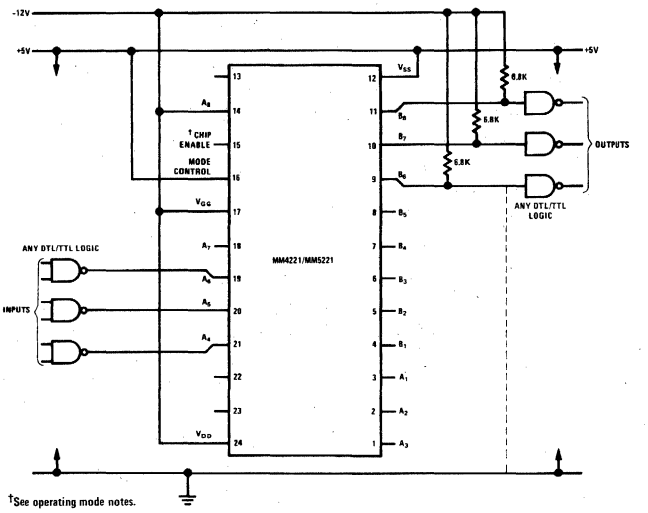
timing diagram/address time





typical application

128-8 Bit ROM Showing TTL Interface



OPERATING MODES

128x8 ROM connection
Control – Logic "0"
A_8 – Logic "1"

256x4 ROM connection
Control – Logic "1"
A_8 – Enables the odd ($B_1 \ldots B_7$) or even ($B_2 \ldots B_8$) outputs.

The outputs are "Enabled" when a logic "1" is applied to the Chip Enable line.

The outputs are connected to ground through an internal MOS resistor when "Disabled."

Logic levels are negative true MOS logic.

Mode control should be "hard wired" to either V_{DD} (logical "1") or V_{SS} (logical "0").

The logic levels are in negative voltage logic notation.

NATIONAL

MOS ROMs

MM4221RQ/MM5221RQ ASCII-7 to EIA RS244A/ EIA RS244A to ASCII-7

general description

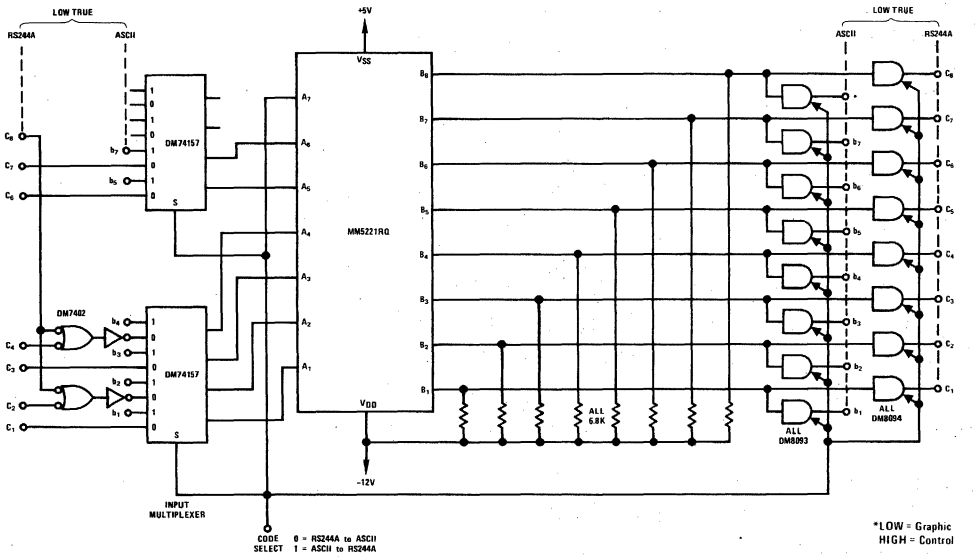
The MM4221RQ/MM5221RQ is a 1024-bit read only memory that has been programmed to convert between the American Standard Code for Information Interchange, compressed to six bits, and the Electronic Industries Association numerical control standard code, RS244A. The second group of addresses, from 64 to 127, effects the reverse conversion.

applications information

In the first 64 entries, compression of ASCII-7 to six bits has been accomplished by dropping bit b_6, and substituting the control codes listed for certain unused ASCII graphic symbols.

In the second 64 entries, the RS244A parity check bit, C_5 is ignored. The bit C_8, used only for the end of block code (EOB) is used externally to detect existence of this symbol, and to insert a redundant code, $C_4 \cdot C_2$ (ROM address 74). This code will be translated arbitrarily as an ASCII EXT.

typical application



Order Number MM4221RQ/J or MM5221RQ/J
See Package 11

Order Number MM5221RQ/N
See Package 18

code conversion tables

ASCII to RS244A

ROM ADDRESS	FUNCTION INPUT ASCII SYMBOL	FUNCTION OUTPUT EIA SYMBOL	CODE	CODE INPUT b_7	b_5	b_4	b_3	b_2	b_1	CODE OUTPUT c_8	c_7	c_6	c_5	c_4	c_3	c_2	c_1
0	SP	SP	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
1			0	0	0	0	0	0	1								
2			0	0	0	0	0	1	0								
3	ETX	EOB	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0
4	EOT	EOR	0	0	0	0	1	0	0	0	0	0	0	1	0	1	1
5	%	%	0							0	1	0	1	1	0	1	1
6	&	&	0							0	0	0	0	1	1	1	0
7			0														
8	BS	BS	0							0	0	1	0	1	0	1	0
9	HT	TAB	0							0	0	1	1	1	1	1	0
10			0							0	0	0	0	0	0	0	0
11	+	+	0							0	1	1	1	0	0	0	0
12	,	,	0							0	0	1	1	1	0	1	1
13	–	–	0							0	1	0	0	0	0	0	0
14	.	.	0							0	1	1	0	1	0	1	1
15	/	/	0							0	0	1	1	0	0	0	1
16	0	0	0							0	0	1	0	0	0	0	0
17	1	1	0							0	0	0	0	0	0	0	1
18	2	2	0							0	0	0	0	0	0	1	0
19	3	3	0							0	0	0	1	0	0	1	1
20	4	4	0							0	0	0	0	0	1	0	0
21	5	5	0							0	0	0	1	0	1	0	1
22	6	6	0							0	0	0	1	0	1	1	0
23	7	7	0							0	0	0	0	0	1	1	1
24	8	8	0							0	0	0	0	1	0	0	0
25	9	9	0							0	0	0	1	1	0	0	1
26			0														
27		UC	0														
28	FS	LC	0							0	1	1	1	1	0	1	0
29	GS		0							0	1	1	1	1	1	0	0
30			0														
31			0														
32			0														
33	a	a	0							0	1	1	0	0	0	0	1
34	b	b	0							0	1	1	0	0	0	1	0
35	c	c	0							0	1	1	1	0	0	1	1
36	d	d	0							0	1	1	0	0	1	0	0
37	e	e	0							0	1	1	0	0	1	0	0
38	f	f	0							0	1	1	1	0	1	1	0
39	g	g	0							0	1	1	0	0	1	1	1
40	h	h	0							0	1	1	0	1	0	0	0
41	i	i	0							0	1	1	1	1	0	0	1
42	j	j	0							0	1	0	1	0	0	0	1
43	k	k	0							0	1	0	1	0	0	1	0
44	l	l	0							0	1	0	0	0	0	1	1
45	m	m	0							0	1	0	1	0	1	0	0
46	n	n	0							0	1	0	0	0	1	0	1
47	o	o	0							0	1	0	0	0	1	1	0
48	p	p	0							0	1	0	1	0	1	1	1
49	q	q	0							0	1	0	1	1	0	0	0
50	r	r	0							0	1	0	0	1	0	0	1
51	s	s	0							0	0	1	1	0	0	1	0
52	t	t	0							0	0	1	0	0	0	1	1
53	u	u	0							0	0	1	1	0	1	0	0
54	v	v	0							0	0	1	0	0	1	0	1
55	w	w	0							0	0	1	0	0	1	1	0
56	x	x	0							0	0	1	1	0	1	1	1
57	y	y	0							0	0	1	1	1	0	0	0
58	z	z	0							0	0	1	0	1	0	0	1
59			0														
60			0														
61			0														
62			0														
63	DEL	DEL	0							0	1	1	1	1	1	1	1
			A_7	A_6	A_5	A_4	A_3	A_2	A_1	B_8	B_7	B_6	B_5	B_4	B_3	B_2	B_1

Increasing Binary Sequence

code conversion tables(con't)

RS244A to ASCII

ROM ADDRESS	FUNCTION INPUT EIA SYMBOL	FUNCTION OUTPUT ASCII SYMBOL	CODE	CODE INPUT c_7	c_6	c_4	c_3	c_2	c_1	CODE OUTPUT CC/G	b_7	b_6	b_5	b_4	b_3	b_2	b_1
64	Space	Space	1	0	0	0	0	0	0	1	0	1	0	0	0	0	0
65	1	1	1	0	0	0	0	0	1	1	0	1	1	0	0	0	1
66	2	2	1	0	0	0	0	1	0	1	0	1	1	0	0	1	0
67	3	3	1	0	0	0	0	1	1	1	0	1	1	0	0	1	1
68	4	4	1	0	0	0	1	0	0	1	0	1	1	0	1	0	0
69	5	5	1	0	0	0	1	0	1	1	0	1	1	0	1	0	1
70	6	6	1							1	0	1	1	0	1	1	0
71	7	7	1							1	0	1	1	0	1	1	1
72	8	8	1							1	0	1	1	1	0	0	0
73	9	9	1							1	0	1	1	1	0	0	1
74	EOB	ETX	1	0	0	1	0	1	0	0	0	0	0	0	0	1	1
75	EOR	EOT	1							0	0	0	0	0	1	0	0
76			1														
77			1														
78	&	&	1							1	0	1	0	0	1	1	0
79			1														
80	0	0	1							1	0	1	1	0	0	0	0
81	1	1	1							1	0	1	0	1	1	1	1
82	s	s	1							1	1	1	1	0	0	1	1
83	t	t	1							1	1	1	1	0	1	0	0
84	u	u	1							1	1	1	1	0	1	0	1
85	v	v	1							1	1	1	1	0	1	1	0
86	w	w	1							1	1	1	1	0	1	1	1
87	x	x	1							1	1	1	1	1	0	0	0
88	y	y	1							1	1	1	1	1	0	0	1
89	z	z	1							1	1	1	1	1	0	1	0
90	BS	BS	1							0	0	0	0	1	0	0	0
91	,	,	1							1	0	1	0	1	1	0	0
92			1														
93			1														
94	TAB	HT	1							0	0	0	0	1	0	0	1
95			1														
96	–	–	1	1	0	0	0	0	0	1	0	1	0	1	1	0	1
97	j	j	1	1	0	0	0	0	1	1	1	1	0	1	0	1	0
98	k	k	1							1	1	1	0	1	0	1	1
99	l	l	1							1	1	1	0	1	1	0	0
100	m	m	1							1	1	1	0	1	1	0	1
101	n	n	1							1	1	1	0	1	1	1	0
102	o	o	1							1	1	1	0	1	1	1	1
103	p	p	1							1	1	1	1	0	0	0	0
104	q	q	1							1	1	1	1	0	0	0	1
105	r	r	1							1	1	1	1	0	0	1	0
106			1														
107	%	%	1							1	0	1	0	0	1	0	1
108			1														
109			1														
110			1														
111			1														
112	+	+	1							1	0	1	0	1	0	1	1
113	a	a	1							1	1	1	0	0	0	0	1
114	b	b	1							1	1	1	0	0	0	1	0
115	c	c	1							1	1	1	0	0	0	1	1
116	d	d	1							1	1	1	0	0	1	0	0
117	e	e	1							1	1	1	0	0	1	0	1
118	f	f	1							1	1	1	0	0	1	1	0
119	g	g	1							1	1	1	0	0	1	1	1
120	h	h	1							1	1	1	0	1	0	0	0
121	i	i	1							1	1	1	0	1	0	0	1
122	LC	GS	1							0	0	0	1	1	1	0	1
123	.	.	1							1	0	1	0	1	1	1	0
124	UC	FS	1							0	0	0	1	1	1	0	0
125			1														
126			1														
127	DEL	DEL	1							0	1	1	1	1	1	1	1
			A_7	A_6	A_5	A_4	A_3	A_2	A_1	B_8	B_7	B_6	B_5	B_4	B_3	B_2	B_1

Increasing Binary Sequence

MOS ROMs

MM4221RR/MM5221RR ASCII-7 to EBCDIC code converter

general description

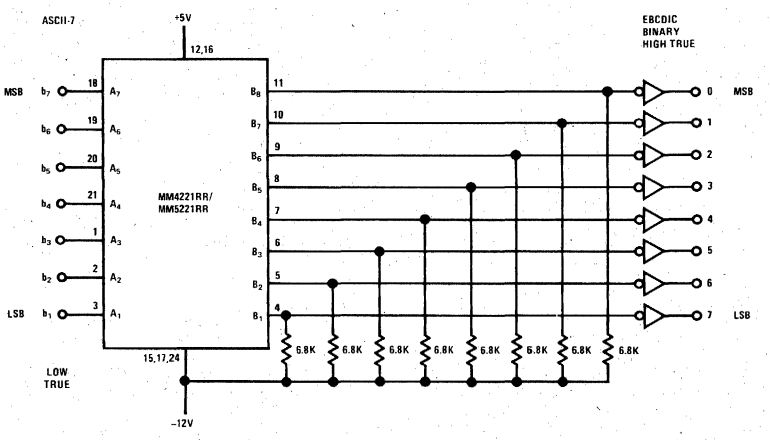
The MM4221RR/MM5221RR is a 1024-bit read-only memory that has been programmed to convert between the 128 characters of ASCII-7, the American Standard Code for Information Interchange in seven bits, and EBCDIC, an extended binary coded decimal interchange code. This conversion follows the EBCDIC character assignments used in the IBM 1130 computer.

Certain arbitrary assignments have also been made for maximum usefulness, and in these two areas the part differs from the MM4230QY/MM5230QY, which follows American National Standard ANSI X3.26 recommendations for character assignments.

For electrical, environmental and mechanical details, refer to the MM4221/MM5221 data sheet.

typical application

ASCII-7 to EBCDIC



Order Number MM4221RR/J or MM5221RR/J
See Package 11
Order Number MM5221RR/N
See Package 18

code conversion tables

ROM ADDRESS	FUNCTION INPUT ASCII SYMBOL	FUNCTION OUTPUT EBCDIC SYMBOL	CODE INPUT MSB						LSB	CODE OUTPUT MSB							LSB
0	NULL	NULL	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	SOH	SOH	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1
2	STX	STX	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0
3	ETX	ETX	0	0	0	0	0	1	1	0	0	0	0	0	0	1	1
4	EOT	EOT	0	0	0	0	1	0	0	0	0	1	1	0	1	1	1
5	ENQ	ENQ	0	0	0	0	1	0	1	0	0	1	0	1	1	0	1
6	ACK	ACK	0	0	0	0	1	1	0	0	0	1	0	1	1	1	0
7	BEL	BEL	0	0	0	0	1	1	1	0	0	1	0	1	1	1	1
8	BS	BS	0	0	0	1	0	0	0	0	0	0	1	0	1	1	0
9	HT	HT	0	0	0	1	0	0	1	0	0	0	0	0	1	0	1
10	LF	LF	0	0	0	1	0	1	0	0	0	1	0	0	1	0	1
11	VT	VT	0	0	0	1	0	1	1	0	0	0	0	1	0	1	1
12	FF	FF	0	0	0	1	1	0	0	0	0	0	0	1	1	0	0
13	CR	CR	0	0	0	1	1	0	1	0	0	0	0	1	1	0	1
14	S0	S0	0	0	0	1	1	1	0	0	0	0	0	1	1	1	0
15	S1	S1	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
16	DLE	DLE	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0
17	DC1	DC1	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1
18	DC2	DC2								0	0	0	1	0	0	1	0
19	DC3	DC3								0	0	0	1	0	0	1	1
20	DC4	RS								0	0	1	1	0	1	0	1
21	NAK	NAK								0	0	1	1	1	1	0	1
22	SYN	SYN								0	0	1	1	0	0	1	0
23	ETB	EOB								0	0	1	0	0	1	1	0
24	CAN	CAN								0	0	0	1	1	0	0	0
25	EM	EM								0	0	0	1	1	0	0	1
26	SUB	SUB								0	0	1	1	1	1	1	1
27	ESC	BYP								0	0	1	0	0	1	0	0
28	FS	FLS								0	0	0	1	1	1	0	0
29	GS	GS								0	0	0	1	1	1	0	1
30	RS	RDS								0	0	0	1	1	1	1	0
31	US	US								0	0	0	1	1	1	1	1
32	SP	SP	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0
33	!	!								0	1	0	1	1	0	1	0
34	"	"								0	1	1	1	1	1	1	1
35	#	#								0	1	1	1	1	0	1	1
36	$	$								0	1	0	1	1	0	1	1
37	%	%								0	1	1	0	1	1	0	0
38	&	&								0	1	0	1	0	0	0	0
39	'	'								0	1	1	1	1	1	0	1
40	(	(								0	1	0	0	1	1	0	1
41	)	)								0	1	0	1	1	1	0	1
42	*	*								0	1	0	1	1	1	0	0
43	+	+								0	1	0	0	1	1	1	0
44	,	,								0	1	1	0	1	0	1	1
45	–	–								0	1	1	0	0	0	0	0
46	.	.								0	1	0	0	1	0	1	1
47	/	/								0	1	1	0	0	0	0	1
48	0	0								1	1	1	1	0	0	0	0
49	1	1								1	1	1	1	0	0	0	1
50	2	2								1	1	1	1	0	0	1	0
51	3	3								1	1	1	1	0	0	1	1
52	4	4								1	1	1	1	0	1	0	0
53	5	5								1	1	1	1	0	1	0	1
54	6	6								1	1	1	1	0	1	1	0
55	7	7								1	1	1	1	0	1	1	1
56	8	8								1	1	1	1	1	0	0	0
57	9	9								1	1	1	1	1	0	0	1
58	:	:								0	1	1	1	1	0	1	0
59	;	;								0	1	0	1	1	1	1	0
60	<	<								0	1	0	0	1	1	0	0
61	=	=								0	1	1	1	1	1	1	0
62	>	>								0	1	1	0	1	1	1	0
63	?	?								0	1	1	0	1	1	1	1
			A_7	A_6	A_5	A_4	A_3	A_2	A_1	B_8	B_7	B_6	B_5	B_4	B_3	B_2	B_1

CONTINUING BINARY SEQUENCE

code conversion tables(con't)

ROM ADDRESS	FUNCTION INPUT ASCII SYMBOL	FUNCTION OUTPUT EBCDIC SYMBOL	CODE INPUT MSB						LSB	CODE OUTPUT MSB							LSB
64	@	@	1	0	0	0	0	0	0	0	1	1	1	1	1	0	0
65	A	A								1	1	0	0	0	0	0	1
66	B	B								1	1	0	0	0	0	1	0
67	C	C								1	1	0	0	0	0	1	1
68	D	D								1	1	0	0	0	1	0	0
69	E	E								1	1	0	0	0	1	0	1
70	F	F								1	1	0	0	0	1	1	0
71	G	G								1	1	0	0	0	1	1	1
72	H	H								1	1	0	0	1	0	0	0
73	I	I								1	1	0	0	1	0	0	1
74	J	J								1	1	0	1	0	0	0	1
75	K	K								1	1	0	1	0	0	1	0
76	L	L								1	1	0	1	0	0	1	1
77	M	M								1	1	0	1	0	1	0	0
78	N	N								1	1	0	1	0	1	0	1
79	O	O								1	1	0	1	0	1	1	0
80	P	P								1	1	0	1	0	1	1	1
81	Q	Q								1	1	0	1	1	0	0	0
82	R	R								1	1	0	1	1	0	0	1
83	S	S								1	1	1	0	0	0	1	0
84	T	T								1	1	1	0	0	0	1	1
85	U	U								1	1	1	0	0	1	0	0
86	V	V								1	1	1	0	0	1	0	1
87	W	W								1	1	1	0	0	1	1	0
88	X	X								1	1	1	0	0	1	1	1
89	Y	Y								1	1	1	0	1	0	0	0
90	Z	Z								1	1	1	0	1	0	0	1
91	[	[								1	0	1	0	1	1	0	1
92	\	NL								0	0	0	1	0	1	0	1
93	]	]								1	0	1	1	1	1	0	1
94	∧	¬								0	1	0	1	1	1	1	1
95	–	–								0	1	1	0	1	1	0	1
96	'	RES	1	1	0	0	0	0	0	0	0	0	1	0	1	0	0
97	a	a								1	0	0	0	0	0	0	1
98	b	b								1	0	0	0	0	0	1	0
99	c	c								1	0	0	0	0	0	1	1
100	d	d								1	0	0	0	0	1	0	0
101	e	e								1	0	0	0	0	1	0	1
102	f	f								1	0	0	0	0	1	1	0
103	g	g								1	0	0	0	0	1	1	1
104	h	h								1	0	0	0	1	0	0	0
105	i	i								1	0	0	0	1	0	0	1
106	j	j								1	0	0	1	0	0	0	1
107	k	k								1	0	0	1	0	0	1	0
108	l	l								1	0	0	1	0	0	1	1
109	m	m								1	0	0	1	0	1	0	0
110	n	n								1	0	0	1	0	1	0	1
111	o	o								1	0	0	1	0	1	1	0
112	p	p								1	0	0	1	0	1	1	1
113	q	q								1	0	0	1	1	0	0	0
114	r	r								1	0	0	1	1	0	0	1
115	s	s								1	0	1	0	0	0	1	0
116	t	t								1	0	1	0	0	0	1	1
117	u	u								1	0	1	0	0	1	0	0
118	v	v								1	0	1	0	0	1	0	1
119	w	w								1	0	1	0	0	1	1	0
120	x	x								1	0	1	0	0	1	1	1
121	y	y								1	0	1	0	1	0	0	0
122	z	z								1	0	1	0	1	0	0	1
123	¦	¦								1	0	0	0	1	0	1	1
124	¦	¦								0	1	0	0	1	1	1	1
125	}	}								1	0	0	1	1	0	1	1
126	~	¢								0	1	0	0	1	0	1	0
127	DEL	DEL								0	0	0	0	0	1	1	1
			A_7	A_6	A_5	A_4	A_3	A_2	A_1	B_8	B_7	B_6	B_5	B_4	B_3	B_2	B_1

CONTINUING BINARY SEQUENCE

NATIONAL

MOS ROMs

MM4229/MM5229 3072-bit read only memory (open drain)

general description

The MM4229/MM5229 is a 3072-bit static read only memory. It is a P-channel enhancement mode monolithic MOS integrated circuit utilizing low threshold technology. The device is a non-volatile memory organized in a 256 x 12 bit word configuration.

Customer programs may be supplied on Hollerith coded punched cards.

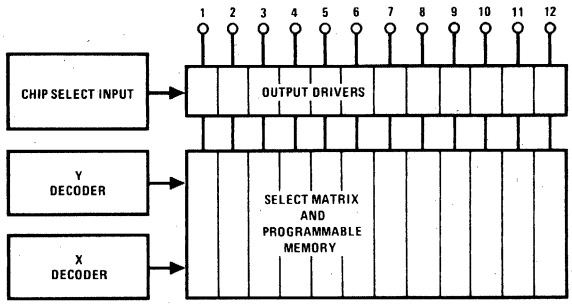
features

- TTL compatible
- Low standby power
- Programmable chip select inputs
- Typical 1.0μs access time
- Open drain outputs allow wire-OR of up to 8 devices

applications

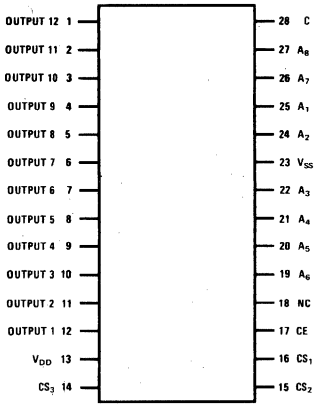
- Code conversion
- Random logic synthesis
- Table look-up
- Microprogramming

block diagram



connection diagram

Dual-In-Line Package



TOP VIEW

Note: For programming information see AN-100.

Order Number MM4229D or MM5229D
See Package 7

Order Number MM5229N
See Package 19

absolute maximum ratings

All Inputs or Outputs with Respect to the Most Positive Voltage V_{SS} (Substrate)	+0.3V to −20V
Supply Voltage V_{DD} and V_D with Respect to V_{SS} (Substrate)	+3.0V to −20V
Operating Temperature Range	
MM4229	−55°C to +125°C
MM5229	−25°C to +70°C
Storage Temperature Range	−65°C to +125°C
Lead Temperature (Soldering, 10 seconds)	300°C

electrical characteristics (Note 1)

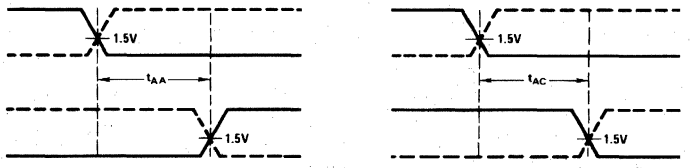
T_A within operating temperature range, V_{DD} = −12V ±10%, V_{SS} = +5V ±5%, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Data Input Levels					
Logical High Level (V_{IH})	V_{SS} = +4.75V	+2.4			V
Logical Low Level (V_{IL})	V_{SS} = +4.75V			+0.8	V
Data Output Levels					
Logical High Level (V_{OH})	6.8 kΩ ±5% to V_{DD} Plus One	+2.4			V
Logical Low Level (V_{OL})	Standard Series 54/74 Gate			+0.4	V
Output Current Capability					
Logical "0"	V_{OUT} = 2.4V	2.5			mA
Data Input Leakage (I_{RI})	$V_{IN} - V_{SS}$ = −5V			2.0	μA
Data Output Leakage (I_{RO})	$V_{OUT} - V_{SS}$ = −5V (Note 1)			2.0	μA
Data Input Capacitance (C_{IN})	$V_{IN} - V_{SS}$ = 0V			5.0	pF
Data Output Capacitance (C_{OUT})	$V_{OUT} - V_{SS}$ = 0V			8.0	pF
Access Time (T_A)					
Address Response (t_{AA})	C_L = 20 pF		1.0	1.4	μs
C Inhibit Response (t_{AC})	C_L = 20 pF		0.8	1.2	μs
Active Power Supply					
V_{DD} Supply (I_{DD})	V_{SS} = +5V, V_1 = 0V		25	32	mA
V_{SS} Supply (I_{SS})	V_{DD} = 12V, T_A = 25°C		25	32	mA
Data Input Currents					
Logical High Level (I_{IH})	$V_{IN} - V_{SS}$ = −2.4V			2.0	μA
Logical Low Level (I_{IL})	$V_{IN} - V_{SS}$ = 5V			2.0	μA
Standby Power Supply					
I_{DD}	V_{SS} = +5V, V_1 = 0V		12	18	mA
I_{SS}	V_{DD} = −12V, T_A = 25°C		12	18	mA

Note 1: Chip inhibited or de-selected.

Note 2: The above logic levels are indicated in negative logic notation.

switching time waveforms



Definitions:

Access Time: Represents the total propagation delay through input translation decode for memory selection and output sense amplification of the memory signal and is measured from the last input transition through 1.5V to the last output transition through 1.5V.

Chip Enable: The output source and sink transistors are turned off in the chip inhibit and chip de-select mode to allow OR-tieing of output for easy memory expansion.

Chip Select: The outputs are enabled and data from the selected memory location will appear at the outputs. The chip select and chip enable inputs are programmable for decoderless word expansion.

NATIONAL

MOS ROMs

MM4230/MM5230 2048-bit read only memory

general description

The MM4230/MM5230 is a 2048-bit static read only memory. It is a P-channel enhancement mode monolithic MOS integrated circuit utilizing low threshold voltage technology. The device is a non-volatile memory organized as 256-8 bit words or 512-4 bit words. Programming of the memory contents is accomplished by changing one mask during the device fabrication. Customer programs may be supplied in a tape, card, or pattern selection format.

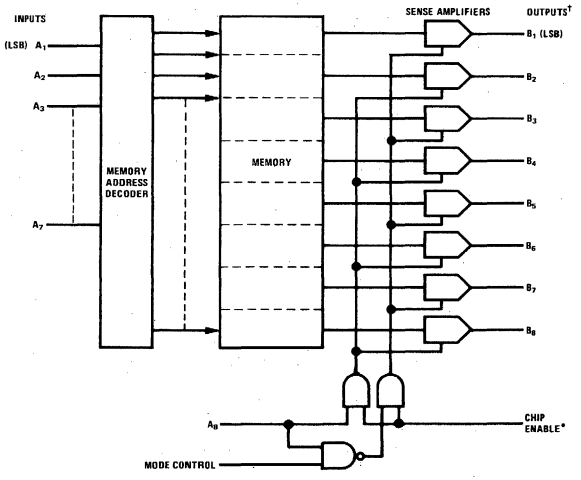
features

- Bipolar compatibility
- High speed operation — 500 ns typ
- Static operation — no clocks required
- Common data busing — output wire AND capability
- Chip enable output control.

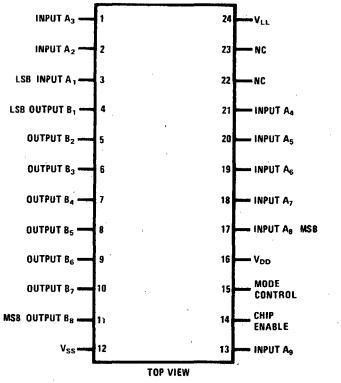
applications

- Code conversion
- Random logic synthesis
- Table look-up
- Character generators
- Microprogramming.

block and connection diagrams



Dual-In-Line Package



Order Number MM4230J
or MM5230J
See Package 11
Order Number MM5230N
See Package 18

Note: For programming information see AN-100.

absolute maximum ratings

V_{GG} Supply Voltage	$V_{SS}-30V$
V_{DD} Supply Voltage	$V_{SS}-15V$
Input Voltage	$(V_{SS}-20)V < V_{IN} < (V_{SS}+0.3)V$
Storage Temperature	$-65^{\circ}C$ to $+150^{\circ}C$
Operating Temperature MM4230	$-55^{\circ}C$ to $+125^{\circ}C$
MM5230	$0^{\circ}C$ to $+70^{\circ}C$
Lead Temperature (Soldering, 10 sec)	$300^{\circ}C$

electrical characteristics

T_A within operating temperature range, $V_{SS} = +12V \pm 5\%$ and $V_{GG} = -12V \pm 5\%$, unless otherwise specified.

PARAMETER	CONDITION	MIN	TYP	MAX	UNITS
Output Voltage Levels					
MOS to MOS					
Logical "1"	1 MΩ to GND Load (Note 1)			$V_{SS}-9.0$	V
Logical "0"		$V_{SS}-1.0$			V
MOS to TTL					
Logical "1"	6.8 kΩ to V_{GG} Plus One			+0.4	V
Logical "0"	Standard Series 54/74 Gate Input	+2.4			V
Input Voltage Levels					
Logical "1"				$V_{SS}-8.0$	V
Logical "0"		$V_{SS}-2.0$			V
Power Supply Current	$T_A = 25^{\circ}C$				
V_{SS}			24	40	mA
V_{GG} (Note 1)				1	μA
Input Leakage	$V_{IN} = V_{SS}-12V$			1	μA
Input Capacitance	f = 1.0 MHz $V_{IN} = 0V$		5		pF
Access Time (Notes 2, 3)	$T_A = 25^{\circ}C$				
T_{ACCESS}	(See Timing Diagram) $V_{SS} = +12V$ $V_{GG} = -12V$	150	500	725	ns
Output AND Connection	MOS Load			3	
	TTL Load			8	

Note 1: The V_{GG} supply may be clocked to reduce device power without affecting access time.

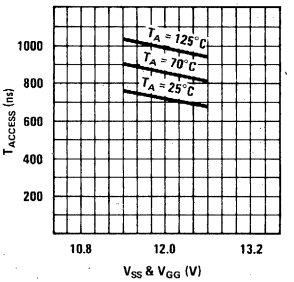
Note 2: Address time is measured from the change of data on any input or Chip Enable line to the output of a TTL gate. See Timing Diagram.

Note 3: The access time in the TTL load configuration follows the equation: T_{ACCESS} = the specified time + (N − 1) (50) ns where N = number of AND connections.

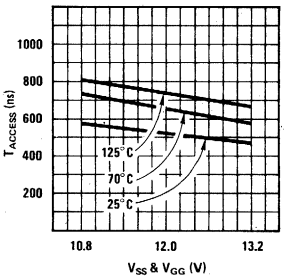
Note 4: The above logic levels are indicated in negative logic notation.

performance characteristics

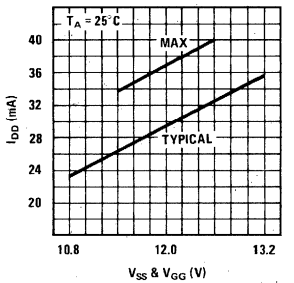
Guaranteed Access Time vs Supply Voltages



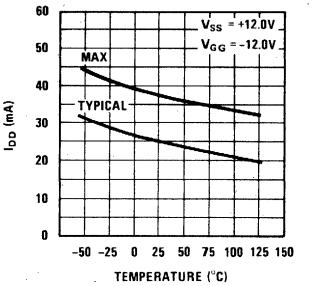
Typical Access Time vs Supply Voltages



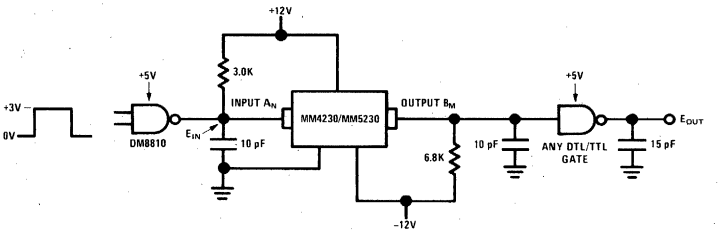
Power Supply Current vs Voltages

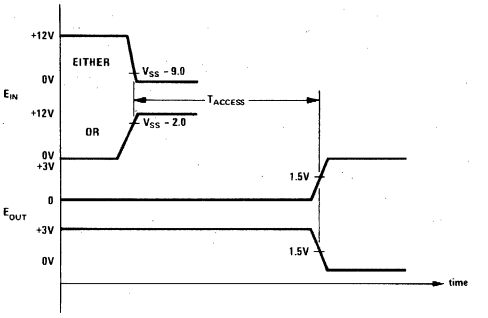


Power Supply Current vs Temperature



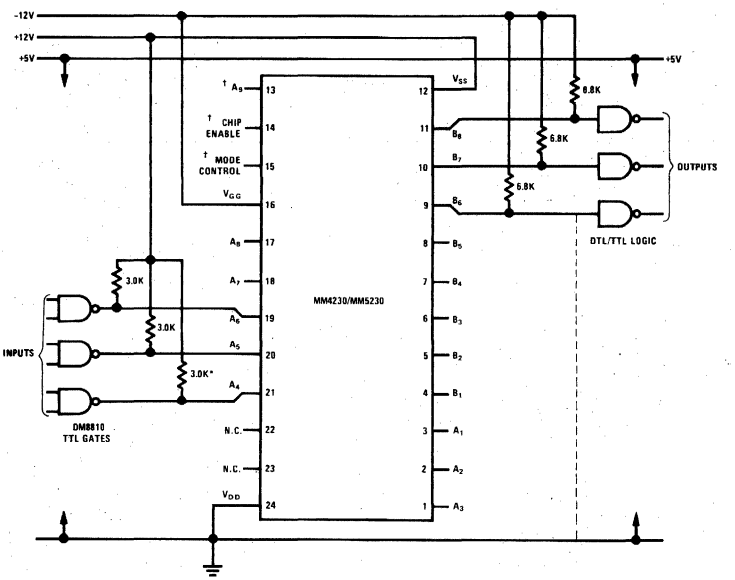
timing diagram/address time





typical application

256 x 8 Bit ROM Showing TTL Interface



†See operating mode notes.
*R values can vary from 740Ω to 30 kΩ.

OPERATING MODES

128x8 ROM connection
Mode Control – Logic "0"
A_9 – Logic "1"

256x4 ROM connection
Mode Control – Logic "1"
A_9 – Logic "0" Enables the odd ($B_1 \ldots B_7$) outputs
– Logic "1" Enables the even ($B_2 \ldots B_8$) outputs.

The outputs are "Enabled" when a logic "1" is applied to the Chip Enable line.

The outputs are connected to V_{DD} through an internal MOS resistor when "Disabled."

The logic levels are in negative voltage logic notation.

MOS ROMs

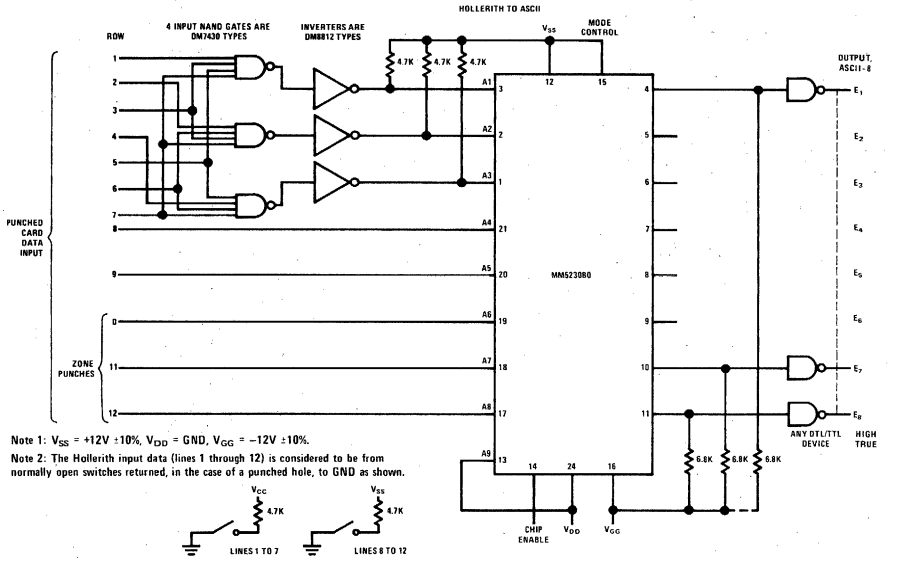
MM4230BO/MM5230BO, MM4231BUS/MM5231BUS hollerith to ASCII code converter

general description

The MM4230BO/MM5230BO 2048-bit MOS read-only memory has been programmed to convert the 12-line Hollerith punched card code to eight level ASCII. This conversion conforms to the American National Standard (ANSI x 3.26 – 1970). Three TTL 4-input NAND gates, and three inverters are used to compress the 12 Hollerith lines to eight-line binary encoded form suitable for use by the read-only memory. This application is shown below.

For electrical, environmental and mechanical details, refer to the MM4230/MM5230 or the MM4231/MM5231 data sheets.

typical application

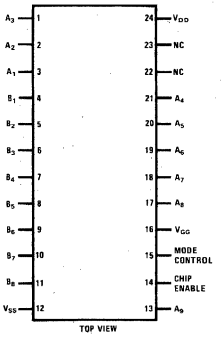


Note 1: V_{SS} = +12V ±10%, V_{DD} = GND, V_{GG} = −12V ±10%.

Note 2: The Hollerith input data (lines 1 through 12) is considered to be from normally open switches returned, in the case of a punched hole, to GND as shown.

connection diagram

Dual-In-Line Package



Order Number MM4230BO/J MM5230BO/J, MM4231BUS/J or MM5231BUS/J
See Package 11

Order Number MM5230BO/N or MM5231BUS/N
See Package 18

code conversion table

Hollerith to ASCII

	12	11	0		12 0	12 11	11 0	12 11 0	12	11	0		12 0	12 11	11 0	12 11 0	
	&	-	ϕ	SP	{	}	¦	11/10	10/8	11/1	11/9	`	12/3	12/10	13/1	13/8	8-1
1	A	J	/	1	a	j	~	13/9	SOH	DC1	8/1	9/1	10/0	10/9	9/15	11/11	9 -1
2	B	K	S	2	b	k	s	13/10	STX	DC2	8/2	SYN	10/1	10/10	11/2	11/12	9 -2
3	C	L	T	3	c	l	t	13/11	ETX	DC3	8/3	9/3	10/2	10/11	11/3	11/13	9 -3
4	D	M	U	4	d	m	u	13/12	9/12	9/13	8/4	9/4	10/3	10/12	11/4	11/14	9 -4
5	E	N	V	5	e	n	v	13/13	HT	8/5	LF	9/5	10/4	10/13	11/5	11/15	9 -5
6	F	O	W	6	f	o	w	13/14	8/6	BS	ETB	9/6	10/5	10/14	11/6	12/0	9 -6
7	G	P	X	7	g	p	x	13/15	DEL	8/7	ESC	EOT	10/6	10/15	11/7	12/1	9 -7
8	H	Q	Y	8	h	q	y	14/0	9/7	CAN	8/8	9/8	10/7	11/0	11/8	12/2	9 -8
9	I	R	Z	9	i	r	z	14/1	8/13	EM	8/9	9/9	NUL	DLE	8/0	9/0	9-8-1
8-2	[	]	\	:	12/4	12/11	13/2	14/2	8/14	9/2	8/10	9/10	14/8	14/14	15/4	15/10	9-8-2
8-3	.	$	,	#	12/5	12/12	13/3	14/3	VT	8/15	8/11	9/11	14/9	14/15	15/5	15/11	9-8-3
8-4	<	*	%	@	12/6	12/13	13/4	14/4	FF	FS	8/12	DC4	14/10	15/0	15/6	15/12	9-8-4
8-5	(	)	–	'	12/7	12/14	13/5	14/5	CR	GS	ENQ	NAK	14/11	15/1	15/7	15/13	9-8-5
8-6	+	;	>	=	12/8	12/15	13/6	14/6	SO	RS	ACK	9/14	14/12	15/2	15/8	15/14	9-8-6
8-7	! ①	^ ②	?	"	12/9	13/0	13/7	14/7	SI	US	BEL	SUB	14/13	15/3	15/9	15/15	9-8-7

① may be "|"
② may be "¬"

Note: The entries of Form A/B refer to the unassigned locations in the right hand side of the ASII table (bit $E_8 = 1$) designated for specialist use. (See National Bureau of Standards Technical Note No. 478.

Note: For the full ASCII-8 Code Table, see MM4230QY/MM5230QY data sheet.

NATIONAL

MOS ROMs

MM4230FE/MM5230FE selectric-to-EBCDIC/ EBCDIC-to-selectric code converter

general description

The MM4230FE/MM5230FE provides for the conversion of IBM Selectric Correspondence Code to Extended Binary Coded Decimal Interchange Code (EBCDIC) in both directions. These two decoders are contained on a monolithic MOS device.

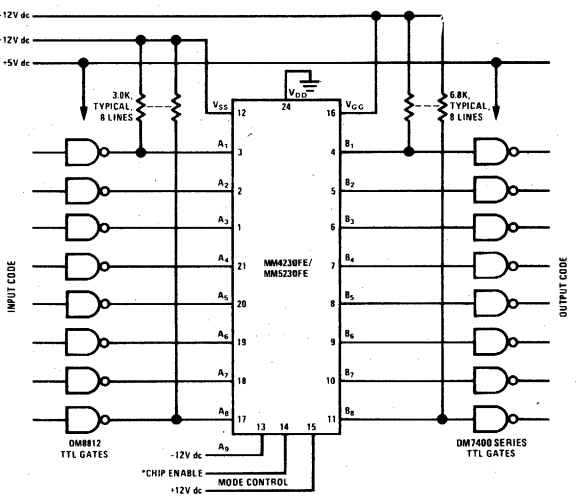
The Selectric-to-EBCDIC converter is located in binary addresses 0 through 127. Input bit A7 is used as a single line command to determine whether upper (denoted by a "1") or a lower (denoted by a "0") case has been selected.

The EBCDIC-to-Selectric converter is located in binary addresses 128 through 255. Since not all EBCDIC control commands have Selectric code counterparts, it is not necessary to encode bit position 0 (A8), which is used instead as the code converter selection bit. In addition to the Selectric Correspondence output code bits there is a bit to indicate upper or lower case. The odd parity bit generated does not account for the case bit.

device characteristics

For full electrical, environmental, and mechanical details refer to the MM4230/MM5230 2048-bit read only memory data sheet.

typical application

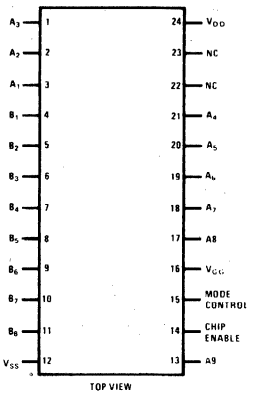


*Chip Enable = Logic "1" to obtain outputs.

Logic Levels:
DTL/TTL (except at MOS/ROM interface). Logic "1," +5.0V, NOM, Logic "0" ground, NOM.
MOS/ROM inputs and outputs. Logic "1," more negative, Logic "0," more positive.

connection diagram

Dual-In-Line Package



Order Number MM4230FE/J or MM5230FE/J
See Package 11

Order Number MM5230FE/N
See Package 18

code conversion table—selectric-to-EBCDIC

ROM ADDRESS	FUNCTION INPUT SELECTRIC SYMBOL	FUNCTION OUTPUT EBCDIC SYMBOL	CODE INPUT CODE	CASE	SELECTRIC R_5	R_2	R_1	R_{2A}	T_1	T_2	OUTPUT EBCDIC 0	1	2	3	4	5	6	7
0	–	–	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0
1	b	b	0	0	0	0	0	0	0	1	1	0	0	0	0	0	1	0
2	w	w	0	0	0	0	0	0	1	0	1	0	1	0	0	1	1	0
3	9	9	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	1
4	q	q	0	0	0	0	0	1	0	0	1	0	0	1	1	0	0	0
5	k	k	0	0	0	0	0	1	0	1	1	0	0	1	0	0	1	0
6	i	i	0	0	0	0	0	1	1	0	1	0	0	0	1	0	0	1
7	6	6	0	0	0	0	0	1	1	1	1	1	1	1	0	1	1	0
8	y	y	0	0	0	0	1	0	0	0	1	0	1	0	1	0	0	0
9	h	h	0	0	0	0	1	0	0	1	1	0	0	0	1	0	0	0
10	s	s	0	0	0	0	1	0	1	0	1	0	1	0	0	0	1	0
11	0	0	0	0	0	0	1	0	1	1	1	1	1	1	0	0	0	0
12	p	p	0	0	0	0	1	1	0	0	1	0	0	1	0	1	1	1
13	e	e	0	0	0	0	1	1	0	1	1	0	0	0	0	1	0	1
14	'	'	0	0	0	0	1	1	1	0	0	1	1	1	1	1	0	1
15	5	5	0	0	0	0	1	1	1	1	1	1	1	1	0	1	0	1
16		NULL	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
17		NULL	0	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0
18		NULL	0	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0
19		NULL	0	0	0	1	0	0	1	1	0	0	0	0	0	0	0	0
20	=	=	0	0	0	1	0	1	0	0	0	1	1	1	1	1	1	0
21	n	n	0	0	0	1	0	1	0	1	1	0	0	1	0	1	0	1
22	.	.	0	0	0	1	0	1	1	0	0	1	0	0	1	0	1	1
23	2	2	0	0	0	1	0	1	1	1	1	1	1	1	0	0	1	0
24		NULL	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0
25		NULL	0	0	0	1	1	0	0	1	0	0	0	0	0	0	0	0
26		NULL	0	0	0	1	1	0	1	0	0	0	0	0	0	0	0	0
27		NULL	0	0	0	1	1	0	1	1	0	0	0	0	0	0	0	0
28	j	j	0	0	0	1	1	1	0	0	1	0	0	1	0	0	0	1
29	t	t	0	0	0	1	1	1	0	1	1	0	1	0	0	0	1	1
30		NULL	0	0	0	1	1	1	1	0	0	0	0	0	0	0	0	0
31	z	z	0	0	0	1	1	1	1	1	1	0	1	0	1	0	0	1
32		NULL	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
33		NULL	0	0	1	0	0	0	0	1	0	0	0	0	0	0	0	0
34		NULL	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0
35		NULL	0	0	1	0	0	0	1	1	0	0	0	0	0	0	0	0
36	,	,	0	0	1	0	0	1	0	0	0	1	1	0	1	0	1	1
37	c	c	0	0	1	0	0	1	0	1	1	0	0	0	0	0	1	1
38	a	a	0	0	1	0	0	1	1	0	1	0	0	0	0	0	0	1
39	8	8	0	0	1	0	0	1	1	1	1	1	1	1	1	0	0	0
40	/	/	0	0	1	0	1	0	0	0	0	1	1	0	0	0	0	1
41	l	l	0	0	1	0	1	0	0	1	1	0	0	1	0	0	1	1
42	o	o	0	0	1	0	1	0	1	0	1	0	0	1	0	1	1	0
43	4	4	0	0	1	0	1	0	1	1	1	1	1	1	0	1	0	0
44	;	;	0	0	1	0	1	1	0	0	0	1	0	1	1	1	1	0
45	d	d	0	0	1	0	1	1	0	1	1	0	0	0	0	1	0	0
46	r	r	0	0	1	0	1	1	1	0	1	0	0	1	1	0	0	1
47	7	7	0	0	1	0	1	1	1	1	1	1	1	1	0	1	1	1
48		NULL	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0
49		NULL	0	0	1	1	0	0	0	1	0	0	0	0	0	0	0	0
50		NULL	0	0	1	1	0	0	1	0	0	0	0	0	0	0	0	0
51		NULL	0	0	1	1	0	0	1	1	0	0	0	0	0	0	0	0
52	f	f	0	0	1	1	0	1	0	0	1	0	0	0	0	1	1	0
53	u	u	0	0	1	1	0	1	0	1	1	0	1	0	0	1	0	0
54	v	v	0	0	1	1	0	1	1	0	1	0	1	0	0	1	0	1
55	3	3	0	0	1	1	0	1	1	1	1	1	1	1	0	0	1	1
56		NULL	0	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0
57		NULL	0	0	1	1	1	0	0	1	0	0	0	0	0	0	0	0
58		NULL	0	0	1	1	1	0	1	0	0	0	0	0	0	0	0	0
59		NULL	0	0	1	1	1	0	1	1	0	0	0	0	0	0	0	0
60	g	g	0	0	1	1	1	1	0	0	1	0	0	0	0	1	1	1
61	x	x	0	0	1	1	1	1	0	1	1	0	1	0	0	1	1	1
62	m	m	0	0	1	1	1	1	1	0	1	0	0	1	0	1	0	0
63	1	1	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	1
			128	64	32	16	8	4	2	1								
			(ROM ADDRESS IN BINARY)															
			(A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1)	(B_8	B_7	B_6	B_5	B_4	B_3	B_2	B_1)

code conversion table—selectric-to-EBCDIC(con't)

ROM ADDRESS	FUNCTION INPUT SELECTRIC SYMBOL	FUNCTION OUTPUT EBCDIC SYMBOL	CODE INPUT CODE	CASE	SELECTRIC R_5	R_2	R_1	R_{2A}	T_1	T_2	OUTPUT EBCDIC 0	1	2	3	4	5	6	7
64	–	–	0	1	0	0	0	0	0	0	0	1	1	0	1	1	0	1
65	B	B	0	1	0	0	0	0	0	1	1	1	0	0	0	0	1	0
66	W	W	0	1	0	0	0	0	1	0	1	1	1	0	0	1	1	0
67	(	(	0	1	0	0	0	0	1	1	0	1	0	0	1	1	0	1
68	Q	Q	0	1	0	0	0	1	0	0	1	1	0	1	1	0	0	0
69	K	K	0	1	0	0	0	1	0	1	1	1	0	1	0	0	1	0
70	I	I	0	1	0	0	0	1	1	0	1	1	0	0	1	0	0	1
71	¢	¢	0	1	0	0	0	1	1	1	0	1	0	0	1	0	1	0
72	Y	Y	0	1	0	0	1	0	0	0	1	1	1	0	1	0	0	0
73	H	H	0	1	0	0	1	0	0	1	1	1	0	0	1	0	0	0
74	S	S	0	1	0	0	1	0	1	0	1	1	1	0	0	0	1	0
75	)	)	0	1	0	0	1	0	1	1	0	1	0	0	1	1	0	1
76	P	P	0	1	0	0	1	1	0	0	1	1	0	1	0	1	1	1
77	E	E	0	1	0	0	1	1	0	1	1	1	0	0	0	1	0	1
78	"	"	0	1	0	0	1	1	1	0	0	1	1	1	1	1	1	1
79	%	%	0	1	0	0	1	1	1	1	0	1	1	0	1	1	0	0
80		NULL	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0
81		NULL	0	1	0	1	0	0	0	1	0	0	0	0	0	0	0	0
82		NULL	0	1	0	1	0	0	1	0	0	0	0	0	0	0	0	0
83		NULL	0	1	0	1	0	0	1	1	0	0	0	0	0	0	0	0
84	+	+	0	1	0	1	0	1	0	0	0	1	0	0	1	1	1	0
85	N	N	0	1	0	1	0	1	0	1	1	1	0	1	0	1	0	1
86	.	.	0	1	0	1	0	1	1	0	0	1	0	0	1	0	1	1
87	@	@	0	1	0	1	0	1	1	1	0	1	1	1	1	1	0	0
88		NULL	0	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0
89		NULL	0	1	0	1	1	0	0	1	0	0	0	0	0	0	0	0
90		NULL	0	1	0	1	1	0	1	0	0	0	0	0	0	0	0	0
91		NULL	0	1	0	1	1	0	1	1	0	0	0	0	0	0	0	0
92	J	J	0	1	0	1	1	1	0	0	1	1	0	1	0	0	0	1
93	T	T	0	1	0	1	1	1	0	1	1	1	1	0	0	0	1	1
94		NULL	0	1	0	1	1	1	1	0	0	0	0	0	0	0	0	0
95	Z	Z	0	1	0	1	1	1	1	1	1	1	1	0	1	0	0	1
96		NULL	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
97		NULL	0	1	1	0	0	0	0	1	0	0	0	0	0	0	0	0
98		NULL	0	1	1	0	0	0	1	0	0	0	0	0	0	0	0	0
99		NULL	0	1	1	0	0	0	1	1	0	0	0	0	0	0	0	0
100	,	,	0	1	1	0	0	1	0	0	0	1	1	0	1	0	1	1
101	C	C	0	1	1	0	0	1	0	1	1	1	0	0	0	0	1	1
102	A	A	0	1	1	0	0	1	1	0	1	1	0	0	0	0	0	1
103	*	*	0	1	1	0	0	1	1	1	0	1	0	1	1	1	0	0
104	?	?	0	1	1	0	1	0	0	0	0	1	1	0	1	1	1	1
105	L	L	0	1	1	0	1	0	0	1	1	1	0	1	0	0	1	1
106	O	O	0	1	1	0	1	0	1	0	1	1	0	1	0	1	1	0
107	$	$	0	1	1	0	1	0	1	1	0	1	0	1	1	0	1	1
108	:	:	0	1	1	0	1	1	0	0	0	1	1	1	1	0	1	0
109	D	D	0	1	1	0	1	1	0	1	1	1	0	0	0	1	0	0
110	R	R	0	1	1	0	1	1	1	0	1	1	0	1	1	0	0	1
111	&	&	0	1	1	0	1	1	1	1	0	1	0	1	0	0	0	0
112		NULL	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
113		NULL	0	1	1	1	0	0	0	1	0	0	0	0	0	0	0	0
114		NULL	0	1	1	1	0	0	1	0	0	0	0	0	0	0	0	0
115		NULL	0	1	1	1	0	0	1	1	0	0	0	0	0	0	0	0
116	F	F	0	1	1	1	0	1	0	0	1	1	0	0	0	1	1	0
117	U	U	0	1	1	1	0	1	0	1	1	1	1	0	0	1	0	0
118	V	V	0	1	1	1	0	1	1	0	1	1	1	0	0	1	0	1
119	#	#	0	1	1	1	0	1	1	1	0	1	1	1	1	0	1	1
120		NULL	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0
121		NULL	0	1	1	1	1	0	0	1	0	0	0	0	0	0	0	0
122		NULL	0	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0
123		NULL	0	1	1	1	1	0	1	1	0	0	0	0	0	0	0	0
124	G	G	0	1	1	1	1	1	0	0	1	1	0	0	0	1	1	1
125	X	X	0	1	1	1	1	1	0	1	1	1	1	0	0	1	1	1
126	M	M	0	1	1	1	1	1	1	0	1	1	0	1	0	1	0	0
127	±	NULL	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
			128	64	32	16	8	4	2	1								
			(ROM ADDRESS IN BINARY)															
			(A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1)	(B_8	B_7	B_6	B_5	B_4	B_3	B_2	B_1)

code conversion table—EBCDIC-to-selectric

ROM ADDRESS	FUNCTION INPUT: EBCDIC SYMBOL	FUNCTION OUTPUT: SELECTRIC SYMBOL	CODE INPUT: CODE	EBCDIC 1	EBCDIC 2	EBCDIC 3	EBCDIC 4	EBCDIC 5	EBCDIC 6	EBCDIC 7	OUTPUT: PARITY	CASE	SELECTRIC R_5	SELECTRIC R_2	SELECTRIC R_1	SELECTRIC R_{2A}	SELECTRIC T_1	SELECTRIC T_2
128	NUL	–	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
129	SOH a	a	1	0	0	0	0	0	0	1	0	0	1	0	0	1	1	0
130	STX b	b	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	1
131	ETX c	c	1	0	0	0	0	0	1	1	0	0	1	0	0	1	0	1
132	PF d	d	1	0	0	0	0	1	0	0	1	0	1	0	1	1	0	1
133	HT e	e	1	0	0	0	0	1	0	1	0	0	0	0	1	1	0	1
134	LC f	f	1	0	0	0	0	1	1	0	0	0	1	1	0	1	0	0
135	DEL g	g	1	0	0	0	0	1	1	1	1	0	1	1	1	1	0	0
136	h	h	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	1
137	i	i	1	0	0	0	1	0	0	1	1	0	0	0	0	1	1	0
138	SMM	–	1	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0
139	VT	–	1	0	0	0	1	0	1	1	0	0	0	0	0	0	0	0
140	FF	–	1	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0
141	CR	–	1	0	0	0	1	1	0	1	0	0	0	0	0	0	0	0
142	SO	–	1	0	0	0	1	1	1	0	0	0	0	0	0	0	0	0
143	SI	–	1	0	0	0	1	1	1	1	0	0	0	0	0	0	0	0
144	DLE	–	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
145	DC1 j	j	1	0	0	1	0	0	0	1	0	0	0	1	1	1	0	0
146	DC2 k	k	1	0	0	1	0	0	1	0	1	0	0	0	0	1	0	1
147	TM l	l	1	0	0	1	0	0	1	1	0	0	1	0	1	0	0	1
148	RES m	m	1	0	0	1	0	1	0	0	0	0	1	1	1	1	1	0
149	NL n	n	1	0	0	1	0	1	0	1	0	0	0	1	0	1	0	1
150	BS o	o	1	0	0	1	0	1	1	0	0	0	1	0	1	0	1	0
151	IL p	p	1	0	0	1	0	1	1	1	1	0	0	0	1	1	0	0
152	CAN q	q	1	0	0	1	1	0	0	0	0	0	0	0	0	1	0	0
153	EM r	r	1	0	0	1	1	0	0	1	1	0	1	0	1	1	1	0
154	CC	–	1	0	0	1	1	0	1	0	0	0	0	0	0	0	0	0
155	CU1	–	1	0	0	1	1	0	1	1	0	0	0	0	0	0	0	0
156	IFS	–	1	0	0	1	1	1	0	0	0	0	0	0	0	0	0	0
157	IGS	–	1	0	0	1	1	1	0	1	0	0	0	0	0	0	0	0
158	IRS	–	1	0	0	1	1	1	1	0	0	0	0	0	0	0	0	0
159	IUS	–	1	0	0	1	1	1	1	1	0	0	0	0	0	0	0	0
160	DS	–	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
161	SOS	–	1	0	1	0	0	0	0	1	0	0	0	0	0	0	0	0
162	FS s	s	1	0	1	0	0	0	1	0	1	0	0	0	1	0	1	0
163	t	t	1	0	1	0	0	0	1	1	1	0	0	1	1	1	0	1
164	BYP u	u	1	0	1	0	0	1	0	0	1	0	1	1	0	1	0	1
165	LF v	v	1	0	1	0	0	1	0	1	1	0	1	1	0	1	1	0
166	ETB w	w	1	0	1	0	0	1	1	0	0	0	0	0	0	0	1	0
167	ESC x	x	1	0	1	0	0	1	1	1	0	0	1	1	1	1	0	1
168	y	y	1	0	1	0	1	0	0	0	0	0	0	0	1	0	0	0
169	z	z	1	0	1	0	1	0	0	1	0	0	0	1	1	1	1	1
170	SM	–	1	0	1	0	1	0	1	0	0	0	0	0	0	0	0	0
171	CU2	–	1	0	1	0	1	0	1	1	0	0	0	0	0	0	0	0
172		–	1	0	1	0	1	1	0	0	0	0	0	0	0	0	0	0
173	ENQ	–	1	0	1	0	1	1	0	1	0	0	0	0	0	0	0	0
174	ACK	–	1	0	1	0	1	1	1	0	0	0	0	0	0	0	0	0
175	BEL	–	1	0	1	0	1	1	1	1	0	0	0	0	0	0	0	0
176		–	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0
177		–	1	0	1	1	0	0	0	1	0	0	0	0	0	0	0	0
178	SYN	–	1	0	1	1	0	0	1	0	0	0	0	0	0	0	0	0
179		–	1	0	1	1	0	0	1	1	0	0	0	0	0	0	0	0
180	PN	–	1	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0
181	RS	–	1	0	1	1	0	1	0	1	0	0	0	0	0	0	0	0
182	UC	–	1	0	1	1	0	1	1	0	0	0	0	0	0	0	0	0
183	EOT	–	1	0	1	1	0	1	1	1	0	0	0	0	0	0	0	0
184		–	1	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0
185		–	1	0	1	1	1	0	0	1	0	0	0	0	0	0	0	0
186		–	1	0	1	1	1	0	1	0	0	0	0	0	0	0	0	0
187	CU3	–	1	0	1	1	1	0	1	1	0	0	0	0	0	0	0	0
188	DC4	–	1	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0
189	NAK	–	1	0	1	1	1	1	0	1	0	0	0	0	0	0	0	0
190		–	1	0	1	1	1	1	1	0	0	0	0	0	0	0	0	0
191	SUB	–	1	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0
			128	64	32	16	8	4	2	1								
			(ROM ADDRESS IN BINARY)															
			(A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1)	(B_8	B_7	B_6	B_5	B_4	B_3	B_2	B_1)

code conversion table—EBCDIC-to-selectric(con't)

ROM ADDRESS	FUNCTION INPUT EBCDIC SYMBOL	FUNCTION OUTPUT SELECTRIC SYMBOL	CODE INPUT EBCDIC CODE	1	2	3	4	5	6	7	OUTPUT PARITY	CASE	SELECTRIC R_5	R_2	R_1	R_{2A}	T_1	T_2
192	Space	—	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
193	A	A	1	1	0	0	0	0	0	1	0	1	1	0	0	1	1	0
194	B	B	1	1	0	0	0	0	1	0	0	1	0	0	0	0	0	1
195	C	C	1	1	0	0	0	0	1	1	0	1	1	0	0	1	0	1
196	D	D	1	1	0	0	0	1	0	0	1	1	1	0	1	1	0	1
197	E	E	1	1	0	0	0	1	0	1	0	1	0	0	1	1	0	1
198	F	F	1	1	0	0	0	1	1	0	0	1	1	1	0	1	0	0
199	G	G	1	1	0	0	0	1	1	1	1	1	1	1	1	1	0	0
200	H	H	1	1	0	0	1	0	0	0	1	1	0	0	1	0	0	1
201	I	I	1	1	0	0	1	0	0	1	1	1	0	0	0	1	1	0
202	¢	¢	1	1	0	0	1	0	1	0	0	1	0	0	0	1	1	1
203	.	.	1	1	0	0	1	0	1	1	0	0	0	1	0	1	1	0
204	<	—	1	1	0	0	1	1	0	0	0	0	0	0	0	0	0	0
205	(	(	1	1	0	0	1	1	0	1	1	1	0	0	0	0	1	1
206	+	+	1	1	0	0	1	1	1	0	1	1	0	1	0	1	0	0
207	'	—	1	1	0	0	1	1	1	1	0	0	0	0	0	0	0	0
208	&	&	1	1	0	1	0	0	0	0	0	1	1	0	1	1	1	1
209	J	J	1	1	0	1	0	0	0	1	0	1	0	1	1	1	0	0
210	K	K	1	1	0	1	0	0	1	0	1	1	0	0	0	1	0	1
211	L	L	1	1	0	1	0	0	1	1	0	1	1	0	1	0	0	1
212	M	M	1	1	0	1	0	1	0	0	0	1	1	1	1	1	1	0
213	N	N	1	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
214	O	O	1	1	0	1	0	1	1	0	0	1	1	0	1	0	1	0
215	P	P	1	1	0	1	0	1	1	1	1	1	0	0	1	1	0	0
216	Q	Q	1	1	0	1	1	0	0	0	0	1	0	0	0	1	0	0
217	R	R	1	1	0	1	1	0	0	1	1	1	1	0	1	1	1	0
218	!	—	1	1	0	1	1	0	1	0	0	0	0	0	0	0	0	0
219	$	$	1	1	0	1	1	0	1	1	1	1	1	0	1	0	1	1
220	* or *	*	1	1	0	1	1	1	0	0	1	1	1	0	0	1	1	1
221	)	)	1	1	0	1	1	1	0	1	0	1	0	0	1	0	1	1
222	;	;	1	1	0	1	1	1	1	0	0	0	1	0	1	1	0	0
223	¬	—	1	1	0	1	1	1	1	1	0	0	0	0	0	0	0	0
224	—	—	1	1	1	0	0	0	0	0	1	0	0	0	0	0	0	0
225	/	/	1	1	1	0	0	0	0	1	1	0	1	0	1	0	0	0
226	S	S	1	1	1	0	0	0	1	0	1	1	0	0	1	0	1	0
227	T	T	1	1	1	0	0	0	1	1	1	1	0	1	1	1	0	1
228	U	U	1	1	1	0	0	1	0	0	1	1	1	1	0	1	0	1
229	V	V	1	1	1	0	0	1	0	1	1	1	1	1	0	1	1	0
230	W	W	1	1	1	0	0	1	1	0	0	1	0	0	0	0	1	0
231	X	X	1	1	1	0	0	1	1	1	0	1	1	1	1	1	0	1
232	Y	Y	1	1	1	0	1	0	0	0	0	1	0	0	1	0	0	0
233	Z	Z	1	1	1	0	1	0	0	1	0	1	0	1	1	1	1	1
234		—	1	1	1	0	1	0	1	0	0	0	0	0	0	0	0	0
235	,	,	1	1	1	0	1	0	1	1	1	0	1	0	0	1	0	0
236	%	%	1	1	1	0	1	1	0	0	1	1	0	0	1	1	1	1
237	– or —	–	1	1	1	0	1	1	0	1	1	1	0	0	0	0	0	0
238	>	—	1	1	1	0	1	1	1	0	0	0	0	0	0	0	0	0
239	?	?	1	1	1	0	1	1	1	1	1	1	1	0	1	0	0	0
240	0	0	1	1	1	1	0	0	0	0	0	0	0	0	0	1	1	1
241	1	1	1	1	1	1	0	0	0	1	1	0	1	1	1	1	1	1
242	2	2	1	1	1	1	0	0	1	0	1	0	0	1	0	1	1	1
243	3	3	1	1	1	1	0	0	1	1	0	0	1	1	0	1	1	1
244	4	4	1	1	1	1	0	1	0	0	1	0	1	0	1	0	1	1
245	5	5	1	1	1	1	0	1	0	1	1	0	0	0	1	1	1	1
246	6	6	1	1	1	1	0	1	1	0	0	0	0	0	0	1	1	1
247	7	7	1	1	1	1	0	1	1	1	0	0	1	0	1	1	1	1
248	8	8	1	1	1	1	1	0	0	0	1	0	1	0	0	1	1	1
249	9	9	1	1	1	1	1	0	0	1	1	0	0	0	0	0	1	1
250	:	:	1	1	1	1	1	0	1	0	0	1	1	0	1	1	0	0
251	#	#	1	1	1	1	1	0	1	1	0	1	1	1	0	1	1	1
252	@	@	1	1	1	1	1	1	0	0	1	1	0	1	0	1	1	1
253	'	'	1	1	1	1	1	1	0	1	0	0	0	0	1	1	1	0
254	=	=	1	1	1	1	1	1	1	0	1	0	0	1	0	1	0	0
255	"	"	1	1	1	1	1	1	1	1	0	1	0	0	1	1	1	0
			128	64	32	16	8	4	2	1								
			(ROM ADDRESS IN BINARY)															
			(A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1)	(B_8	B_7	B_6	B_5	B_4	B_3	B_2	B_1)

MOS ROMs

MM4230JT/MM5230JT BCDIC to EBCDIC/ EBCDIC to BCDIC code converter

general description

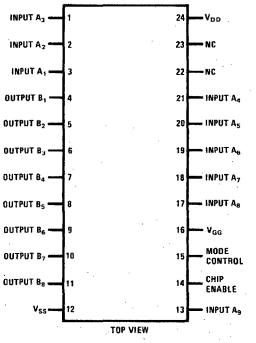
The MM4230JT/MM5230JT is a 2048-bit read-only memory that has been programmed to convert from the 64-entry, 6-bit Binary Coded Decimal Interchange Code (BCDIC) to the eight-bit extended BCD interchange code (EBCDIC) and back again. The tables show the two translations in binary.

Character assignments for the EBCDIC are given to IBM1130 specifications. All the non-alphanumeric assignments in BCDIC are subject to specialist usage, and care should be taken over them.

For electrical, environmental and mechanical details, refer to the MM4230/MM5230 data sheet.

connection diagram

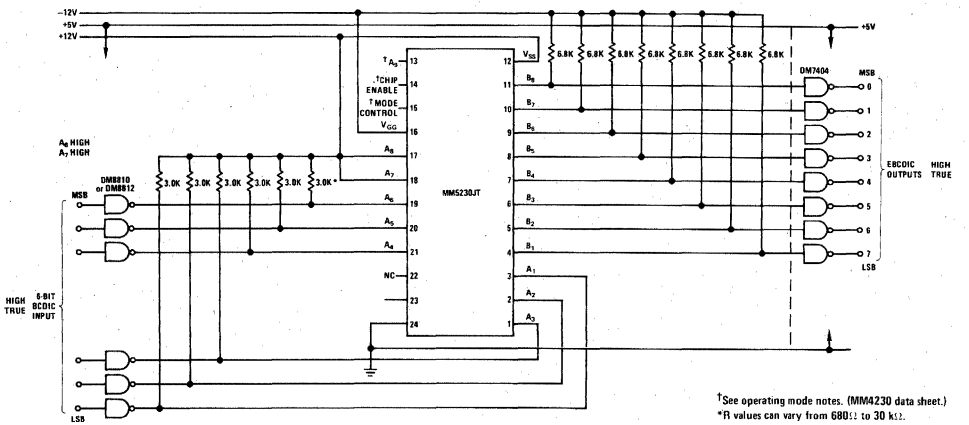
Dual-In-Line Package



Order Number MM4230JT/J or MM5230JT/J
See Package 11
Order Number MM5230JT/N
See Package 18

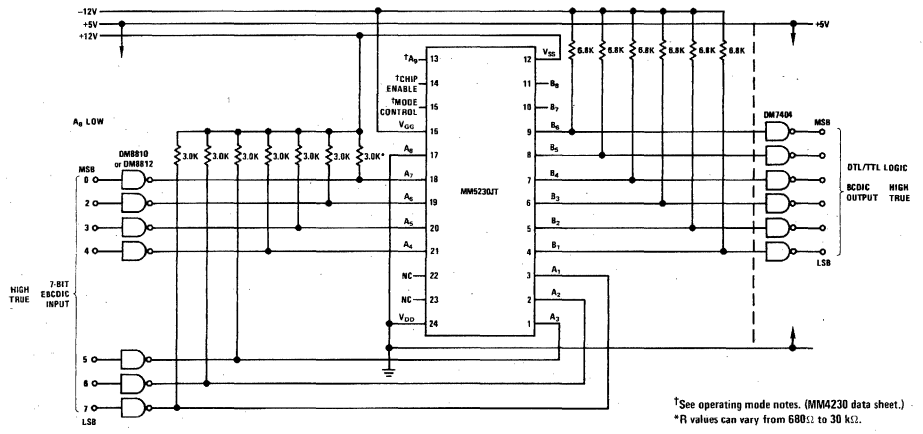
typical applications

BCDIC to EBCDIC



typical applications (con't)

EBCDIC to BCDIC



†See operating mode notes. (MM4230 data sheet.)
*R values can vary from 680Ω to 30 kΩ.

code conversion tables

BCDIC to EBCDIC

ROM ADDRESS	FUNCTION		CODE							
	INPUT	OUTPUT	OUTPUT							
	BCDIC	EBCDIC	EBCDIC							
	SYMBOL	SYMBOL	B_8	B_7	B_6	B_5	B_4	B_3	B_2	B_1
0	NULL	NULL	0	0	0	0	0	0	0	0
1	1	1	1	1	1	1	0	0	0	1
2	2	2	1	1	1	1	0	0	1	0
3	3	3	1	1	1	1	0	0	1	1
4	4	4	1	1	1	1	0	1	0	0
5	5	5	1	1	1	1	0	1	0	1
6	6	6	1	1	1	1	0	1	1	0
7	7	7	1	1	1	1	0	1	1	1
8	8	8	1	1	1	1	1	0	0	0
9	9	9	1	1	1	1	1	0	0	1
10	0	0	1	1	1	1	0	0	0	0
11	#	#	0	1	1	1	1	0	1	1
12	@	@	0	1	1	1	1	1	0	0
13	'	'	0	1	1	1	1	1	0	1
14	=	=	0	1	1	1	1	1	1	0
15	"	"	0	1	1	1	1	1	1	1
16	Space	Space	0	1	0	0	0	0	0	0
17	/	/	0	1	1	0	0	0	0	1
18	S	S	1	1	1	0	0	0	1	0
19	T	T	1	1	1	0	0	0	1	1
20	U	U	1	1	1	0	0	1	0	0
21	V	V	1	1	1	0	0	1	0	1
22	W	W	1	1	1	0	0	1	1	0
23	X	X	1	1	1	0	0	1	1	1
24	Y	Y	1	1	1	0	1	0	0	0
25	Z	Z	1	1	1	0	1	0	0	1
26	NULL	NULL	0	1	0	0	0	0	0	0
27	,	,	0	1	1	0	1	0	1	1
28	%	%	0	1	1	0	1	1	0	0
29	—	—	0	1	1	0	1	1	0	1
30	>	>	0	1	1	0	1	1	1	0
31	?	?	0	1	1	0	1	1	1	1
32	–	–	0	1	1	0	0	0	0	0
33	J	J	1	1	0	1	0	0	0	1
34	K	K	1	1	0	1	0	0	1	0
35	L	L	1	1	0	1	0	0	1	1
36	M	M	1	1	0	1	0	1	0	0
37	N	N	1	1	0	1	0	1	0	1
38	O	O	1	1	0	1	0	1	1	0
39	P	P	1	1	0	1	1	1	1	1
40	Q	Q	1	1	0	1	1	0	0	0
41	R	R	1	1	0	1	1	0	0	1
42	!	!	0	1	0	1	1	0	1	0
43	$	$	0	1	0	1	1	0	1	1
44	*	*	0	1	0	1	1	1	0	0
45	)	)	0	1	0	1	1	1	0	1
46	;	;	0	1	0	1	1	1	1	0
47	¬	¬	0	1	0	1	1	1	1	1
48	&	&	0	1	0	1	0	0	0	0
49	A	A	1	1	0	0	0	0	0	1
50	B	B	1	1	0	0	0	0	1	0
51	C	C	1	1	0	0	0	0	1	1
52	D	D	1	1	0	0	0	1	0	0
53	E	E	1	1	0	0	0	1	0	1
54	F	F	1	1	0	0	0	1	1	0
55	G	G	1	1	0	0	0	1	1	1
56	H	H	1	1	0	0	1	0	0	0
57	I	I	1	1	0	0	1	0	0	1
58	¢	¢	0	1	0	0	1	0	1	0
59	.	.	0	1	0	0	1	0	1	1
60	<	<	0	1	0	0	1	1	0	0
61	(	(	0	1	0	0	1	1	0	1
62	+	+	0	1	0	0	1	1	1	0
63	|	|	0	1	0	0	1	1	1	1

code conversion tables(con't)

BCDIC to EBCDIC (con't)

ROM ADDRESS	FUNCTION		CODE							
	INPUT	OUTPUT	OUTPUT							
	BCDIC SYMBOL	EBCDIC SYMBOL	EBCDIC							
			B_8	B_7	B_6	B_5	B_4	B_3	B_2	B_1
64	0	0	1	1	1	1	0	0	0	0
65	1	1	1	1	1	1	0	0	0	1
66	2	2	1	1	1	1	0	0	1	0
67	3	3	1	1	1	1	0	0	1	1
68	4	4	1	1	1	1	0	1	0	0
69	5	5	1	1	1	1	0	1	0	1
70	6	6	1	1	1	1	0	1	1	0
71	NULL	NULL	0	0	0	0	0	0	0	0
72	7	7	1	1	1	1	0	1	1	1
73	8	8	1	1	1	1	1	0	0	0
74	9	9	1	1	1	1	1	0	0	1
75	NULL	NULL	0	0	0	0	0	0	0	0
76	NULL	NULL	0	0	0	0	0	0	0	0
77	NULL	NULL	0	0	0	0	0	0	0	0
78	NULL	NULL	0	0	0	0	0	0	0	0
79	NULL	NULL	0	0	0	0	0	0	0	0
80	NULL	NULL	0	0	0	0	0	0	0	0
81	NULL	NULL	0	0	0	0	0	0	0	0
82	NULL	NULL	0	0	0	0	0	0	0	0
83	NULL	NULL	0	0	0	0	0	0	0	0
84	NULL	NULL	0	0	0	0	0	0	0	0
85	NULL	NULL	0	0	0	0	0	0	0	0
86	NULL	NULL	0	0	0	0	0	0	0	0
87	NULL	NULL	0	0	0	0	0	0	0	0
88	NULL	NULL	0	0	0	0	0	0	0	0
89	NULL	NULL	0	0	0	0	0	0	0	0
90	NULL	NULL	0	0	0	0	0	0	0	0
91	NULL	NULL	0	0	0	0	0	0	0	0
92	NULL	NULL	0	0	0	0	0	0	0	0
93	NULL	NULL	0	0	0	0	0	0	0	0
94	NULL	NULL	0	0	0	0	0	0	0	0
95	NULL	NULL	0	0	0	0	0	0	0	0
96	NULL	NULL	0	0	0	0	0	0	0	0
97	NULL	NULL	0	0	0	0	0	0	0	0
98	NULL	NULL	0	0	0	0	0	0	0	0
99	NULL	NULL	0	0	0	0	0	0	0	0
100	NULL	NULL	0	0	0	0	0	0	0	0
101	NULL	NULL	0	0	0	0	0	0	0	0
102	NULL	NULL	0	0	0	0	0	0	0	0
103	NULL	NULL	0	0	0	0	0	0	0	0
104	NULL	NULL	0	0	0	0	0	0	0	0
105	NULL	NULL	0	0	0	0	0	0	0	0
106	NULL	NULL	0	0	0	0	0	0	0	0
107	NULL	NULL	0	0	0	0	0	0	0	0
108	NULL	NULL	0	0	0	0	0	0	0	0
109	NULL	NULL	0	0	0	0	0	0	0	0
110	NULL	NULL	0	0	0	0	0	0	0	0
111	NULL	NULL	0	0	0	0	0	0	0	0
112	NULL	NULL	0	0	0	0	0	0	0	0
113	NULL	NULL	0	0	0	0	0	0	0	0
114	NULL	NULL	0	0	0	0	0	0	0	0
115	NULL	NULL	0	0	0	0	0	0	0	0
116	NULL	NULL	0	0	0	0	0	0	0	0
117	NULL	NULL	0	0	0	0	0	0	0	0
118	NULL	NULL	0	0	0	0	0	0	0	0
119	NULL	NULL	0	0	0	0	0	0	0	0
120	NULL	NULL	0	0	0	0	0	0	0	0
121	NULL	NULL	0	0	0	0	0	0	0	0
122	NULL	NULL	0	0	0	0	0	0	0	0
123	NULL	NULL	0	0	0	0	0	0	0	0
124	NULL	NULL	0	0	0	0	0	0	0	0
125	NULL	NULL	0	0	0	0	0	0	0	0
126	NULL	NULL	0	0	0	0	0	0	0	0
127	NULL	NULL	0	0	0	0	0	0	0	0

code conversion tables(con't)

EBCDIC to BCDIC

ROM ADDRESS	FUNCTION		CODE							
	INPUT	OUTPUT	OUTPUT							
	EBCDIC SYMBOL	BCDIC SYMBOL	BCDIC							
			B_8	B_7	B_6	B_5	B_4	B_3	B_2	B_1
128	NULL	NULL	0	0	0	0	0	0	0	0
129	NULL	NULL	0	0	0	0	0	0	0	0
130	NULL	NULL	0	0	0	0	0	0	0	0
131	NULL	NULL	0	0	0	0	0	0	0	0
132	NULL	NULL	0	0	0	0	0	0	0	0
133	–	.	0	0	0	1	0	0	0	0
134	–	–	0	0	0	1	0	0	0	0
135	NULL	NULL	0	0	0	0	0	0	0	0
136	NULL	NULL	0	0	0	0	0	0	0	0
137	–	–	0	0	0	1	0	0	0	0
138	¢	¢	0	0	1	1	1	0	1	0
139	.	.	0	0	1	1	1	0	1	1
140	<	<	0	0	1	1	1	1	0	0
141	(	(	0	0	1	1	1	1	0	1
142	+	+	0	0	1	1	1	1	1	0
143	|	|	0	0	1	1	1	1	1	1
144	&	&	0	0	1	1	0	0	0	0
145	NULL	NULL	0	0	0	0	0	0	0	0
146	NULL	NULL	0	0	0	0	0	0	0	0
147	NULL	NULL	0	0	0	0	0	0	0	0
148	NULL	NULL	0	0	0	0	0	0	0	0
149	–	–	0	0	0	1	0	0	0	0
150	–	–	0	0	0	1	0	0	0	0
151	NULL	NULL	0	0	0	0	0	0	0	0
152	NULL	NULL	0	0	0	0	0	0	0	0
153	!	!	0	0	0	0	0	0	0	0
154	$	$	0	0	1	0	1	0	1	0
155	*	*	0	0	1	0	1	0	1	1
156	)	)	0	0	1	0	1	1	0	0
157	;	;	0	0	1	0	1	1	0	1
158	¬	¬	0	0	1	0	1	1	1	0
159	-	-	0	0	1	0	1	1	1	1
160	/	/	0	0	1	0	0	0	0	0
161	⌟	⌟	0	0	0	1	0	0	0	1
162	NULL	NULL	0	0	0	0	0	0	0	0
163	NULL	NULL	0	0	0	0	0	0	0	0
164	NULL	NULL	0	0	0	0	0	0	0	0
165	NULL	NULL	0	0	0	0	0	0	0	0
166	NULL	NULL	0	0	0	0	0	0	0	0
167	NULL	NULL	0	0	0	0	0	0	0	0
168	NULL	NULL	0	0	0	0	0	0	0	0
169	NULL	NULL	0	0	0	0	0	0	0	0
170	NULL	NULL	0	0	0	0	0	0	0	0
171	,	,	0	0	0	1	1	0	1	1
172	%	%	0	0	0	1	1	1	0	0
173	–	–	0	0	0	1	1	1	0	1
174	>	>	0	0	0	1	1	1	1	0
175	?	?	0	0	0	1	1	1	1	1
176	NULL	NULL	0	0	0	0	0	0	0	0
177	NULL	NULL	0	0	0	0	0	0	0	0
178	NULL	NULL	0	0	0	0	0	0	0	0
179	NULL	NULL	0	0	0	0	0	0	0	0
180	NULL	NULL	0	0	0	0	0	0	0	0
181	–	–	0	0	0	1	0	0	0	0
182	–	–	0	0	0	1	0	0	0	0
183	NULL	NULL	0	0	0	0	0	0	0	0
184	NULL	NULL	0	0	0	0	0	0	0	0
185	NULL	NULL	0	0	0	0	0	0	0	0
186	:	:	0	0	0	0	0	0	0	0
187	#	#	0	0	0	0	1	0	1	1
188	@	@	0	0	0	0	1	1	0	0
189	'	'	0	0	0	0	1	1	0	1
190	=	=	0	0	0	0	1	1	1	0
191	"	"	0	0	0	0	1	1	1	1

code conversion tables(con't)

EBCDIC to BCDIC (con't)

ROM ADDRESS	FUNCTION INPUT EBCDIC SYMBOL	FUNCTION OUTPUT BCDIC SYMBOL	CODE OUTPUT BCDIC B_8	B_7	B_6	B_5	B_4	B_3	B_2	B_1
192	-	-	0	0	0	1	0	0	0	0
193	A	A	0	0	1	1	0	0	0	1
194	B	B	0	0	1	1	0	0	1	0
195	C	C	0	0	1	1	0	0	1	1
196	D	D	0	0	1	1	0	1	0	0
197	E	E	0	0	1	1	0	1	0	1
198	F	F	0	0	1	1	0	1	1	0
199	G	G	0	0	1	1	0	1	1	1
200	H	H	0	0	1	1	1	0	0	0
201	I	I	0	0	1	1	1	0	0	1
202	NULL	NULL	0	0	0	0	0	0	0	0
203	NULL	NULL	0	0	0	0	0	0	0	0
204	NULL	NULL	0	0	0	0	0	0	0	0
205	NULL	NULL	0	0	0	0	0	0	0	0
206	NULL	NULL	0	0	0	0	0	0	0	0
207	NULL	NULL	0	0	0	0	0	0	0	0
208	NULL	NULL	0	0	0	0	0	0	0	0
209	J	J	0	0	1	0	0	0	0	1
210	K	K	0	0	1	0	0	0	1	0
211	L	L	0	0	1	0	0	0	1	1
212	M	M	0	0	1	0	0	1	0	0
213	N	N	0	0	1	0	0	1	0	1
214	O	O	0	0	1	0	0	1	1	0
215	P	P	0	0	1	0	0	1	1	1
216	Q	Q	0	0	1	0	1	0	0	0
217	R	R	0	0	1	0	1	0	0	1
218	NULL	NULL	0	0	0	0	0	0	0	0
219	NULL	NULL	0	0	0	0	0	0	0	0
220	NULL	NULL	0	0	0	0	0	0	0	0
221	NULL	NULL	0	0	0	0	0	0	0	0
222	NULL	NULL	0	0	0	0	0	0	0	0
223	NULL	NULL	0	0	0	0	0	0	0	0
224	NULL	NULL	0	0	0	0	0	0	0	0
225	NULL	NULL	0	0	0	0	0	0	0	0
226	S	S	0	0	0	1	0	0	1	0
227	T	T	0	0	0	1	0	0	1	1
228	U	U	0	0	0	1	0	1	0	0
229	V	V	0	0	0	1	0	1	0	1
230	W	W	0	0	0	1	0	1	1	0
231	X	X	0	0	0	1	0	1	1	1
232	Y	Y	0	0	0	1	1	0	0	0
233	Z	Z	0	0	0	1	1	0	0	1
234	NULL	NULL	0	0	0	0	0	0	0	0
235	NULL	NULL	0	0	0	0	0	0	0	0
236	NULL	NULL	0	0	0	0	0	0	0	0
237	NULL	NULL	0	0	0	0	0	0	0	0
238	NULL	NULL	0	0	0	0	0	0	0	0
239	NULL	NULL	0	0	0	0	0	0	0	0
240	0	0	0	0	0	0	1	0	1	0
241	1	1	0	0	0	0	0	0	0	1
242	2	2	0	0	0	0	0	0	1	0
243	3	3	0	0	0	0	0	0	1	1
244	4	4	0	0	0	0	0	1	0	0
245	5	5	0	0	0	0	0	1	0	1
246	6	6	0	0	0	0	0	1	1	0
247	7	7	0	0	0	0	0	1	1	1
248	8	8	0	0	0	0	1	0	0	0
249	9	9	0	0	0	0	1	0	0	1
250	NULL	NULL	0	0	0	0	0	0	0	0
251	NULL	NULL	0	0	0	0	0	0	0	0
252	NULL	NULL	0	0	0	0	0	0	0	0
253	NULL	NULL	0	0	0	0	0	0	0	0
254	NULL	NULL	0	0	0	0	0	0	0	0
255	NULL	NULL	0	0	0	0	0	0	0	0

MOS ROMs

MM4230KP/MM5230KP ASCII-7 to selectric code converter

general description

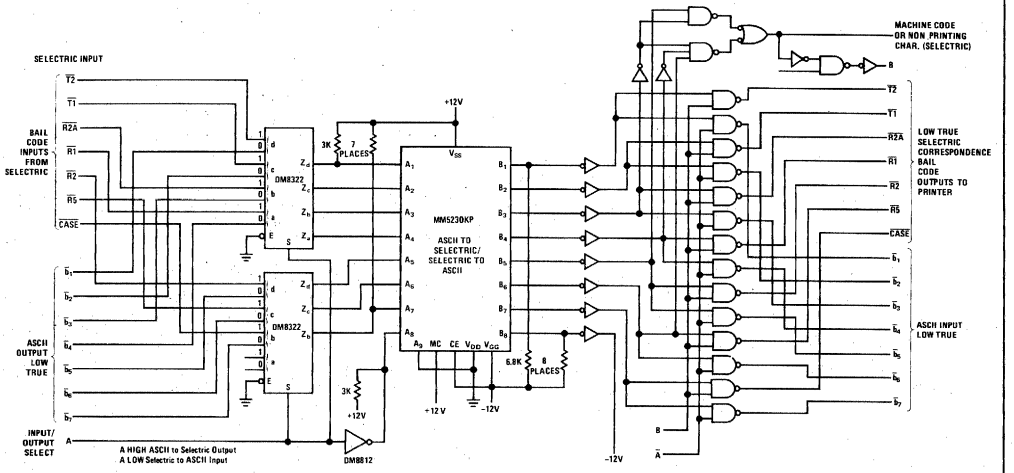
The MM4230KP/MM5230KP MOS read-only memory has been programmed to perform the conversion between the American Standard Code for Information Interchange in seven bits (ASCII) and the Selectric correspondence bail code transmitted and received by the IBM Series 7 input/output printers.

application hints

The ASCII field and Selectric bail code field as defined do not map exactly: for instance "space" is handled as a normal 7-bit code in ASCII, but is handled as a unique switch and solenoid pair in the Selectric printer. And even among the graphic characters, ± and ¢ exist only for Selectric, and > and < only for ASCII. The former problem is handled in the MM4230KP/MM5230KP by exploiting the inherent redundancy of the bail code (see Table 2). The latter inconsistency is resolved by making arbitrary equivalences between the unique characters. The two tables show the treatment of both the characters which have equivalents in both codes, and those characters, and the functions, which do not. Encoding and decoding the Selectric functions that the user requires is a matter of conventional Boolean logic. A typical example is shown below.

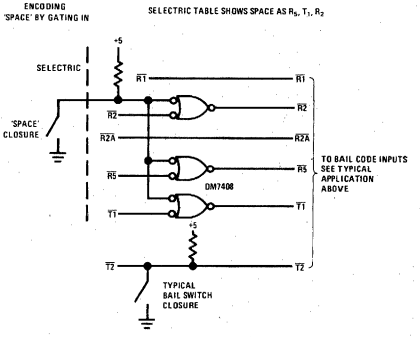
For electrical, environmental and mechanical details, refer to the MM4230/MM5230 data sheet.

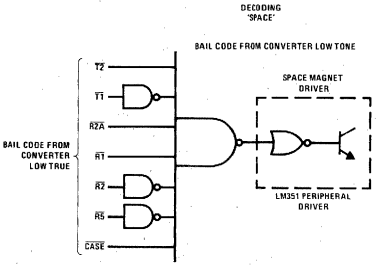
typical applications



Encoding 'Space' by Gating In on Input

Decoding 'Space' on Output





Order Number MM4230KP/J or MM5230KP/J
See Package 11

Order Number MM5230KP/N
See Package 18

code conversion tables

Table 1. ASCII-7 to Selectric

b_7 b_6 b_5 → / Bits					0 0 0	0 0 1	0 1 0	0 1 1	1 0 0	1 0 1	1 1 0	1 1 1
b_4	b_3	b_2	b_1	Row ↓ / Column →	0	1	2	3	4	5	6	7
0	0	0	0	0	NUL 02	DLE 0A	SP 62	0	@	P	` 25	p
0	0	0	1	1	SOH 12	DCI IA	!	1	A	Q	a	q
0	0	1	0	2	STX 22	DC2 2A	"	2	B	R	b	r
0	0	1	1	3	ETX 32	DC3 3A	#	3	C	S	c	s
0	1	0	0	4	EOT 03	DC4 0B	$	4	D	T	d	t
0	1	0	1	5	ENQ 13	NAK 1B	%	5	E	U	e	u
0	1	1	0	6	ACK 23	SYN 2B	&	6	F	V	f	v
0	1	1	1	7	BEL 33	ETB 3B	' 25	7	G	W	g	w
1	0	0	0	8	BS 42	CAN 4A	(	8	H	X	h	x
1	0	0	1	9	HT 52	EM 5A	)	9	I	Y	i	y
1	0	1	0	A	LF 53	SUB 6A	*	:	J	Z	j	z
1	0	1	1	B	VT 72	ESC 7A	+	;	K	[7F	k	{ 7F
1	1	0	0	C	FF 72	FS 4B	,	< 40	L	\ 60	l	¦ 48
1	1	0	1	D	CR 53	GS 5B	–	=	M	] 77	m	} 77
1	1	1	0	E	SO 63	RS 6B	.	> 50	N	^ 70	n	~ 58
1	1	1	1	F	SI 73	US 7B	/	?	O	_	o	DEL 00

code conversion tables (con't)

Table 2. Selectric to ASCII-7

R_5 → / T_1 → / T_2 →					0 0 0	0 0 1	0 1 0	0 1 1	1 0 0	1 0 1	1 1 0	1 1 1
S ↓	R_{2A} ↓	R_2 ↓	R_1 ↓	Row ↓ / Column →	0	1	2	3	4	5	6	7
0	0	0	0	0	¯ 2/D	b	w	9	< 3/C	> 3/E	\ 5/C	^ 5/E
0	0	0	1	1	y	h	s	0 3/0	/	l 6/C	° 6/F	4
0	0	1	0	2	NUL 0/0	SOH 0/1	STX 0/2	ETX 0/3	BS 0/8	TAB 0/9	SP 2/0	IND 0/A
0	0	1	1	3	EOT C/4	ENQ 0/5	ACK 0/6	BELL 0/7		CR 0/D	SO 0/E	SI 0/F
0	1	0	0	4	Q	k	i	6	' 2/C	c	a	8
0	1	0	1	5	P	e	, 2/7	5	; 3/B	d	r	7
0	1	1	0	6	= 3/D	n	. 2/E	2	f	u	v	3
0	1	1	1	7	J	t	½! 2/1	z	g	x	m	1
1	0	0	0	8	_	B	W	(	¦ 7/C	~ 7/E		
1	0	0	1	9	Y	H	S	)	?	L	o 4/F	$
1	0	1	0	A	DLE 1/0	DC1 1/1	DC2 1/2	DC3 1/3	CAN 1/8	EM 1/9	SUB 1/A	ESC 1/B
1	0	1	1	B	DC4 1/4	NAK 1/5	SYN 1/6	ETB 1/7	FS 1/C	GS 1/D	RS 1/E	US 1/F
1	1	0	0	C	Q	K	l 4/9	¢ 6/3	' 2/C	C	A	*
1	1	0	1	D	P	E	"	%	:	D	R	&
1	1	1	0	E	+	N	. 2/E	@	F	U	V	#
1	1	1	1	F	J	T	¼° F/F	Z	G	X	M	±[5/B

Entries Thus are Redundant Bail Codes

ASCII shown thus: Column No./Row No.

6

NATIONAL

MOS ROMs

MM4230QW/MM5230QW hollerith to EBCDIC code converter

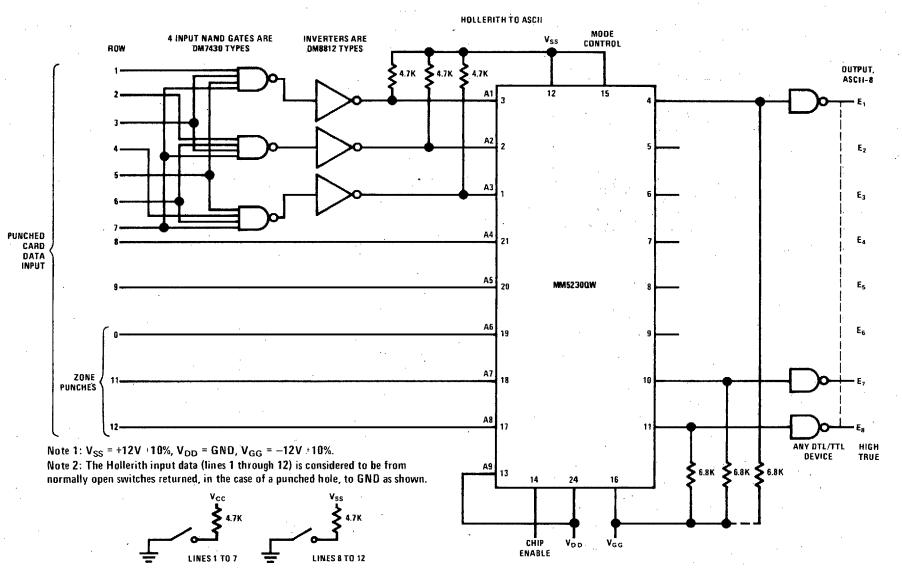
general description

The MM4230QW/MM5230QW 2048-bit MOS read only memory has been programmed to convert the 12 line Hollerith Code to the 8 line EBCDIC Code. Three TTL 4-input NAND gates and three TTL inverters are used to compress the 12 Hollerith lines to eight line binary encoded form suitable for use by the ROM.

For electrical, environmental and mechanical details, refer to the MM4230/MM5230 data sheet.

typical application

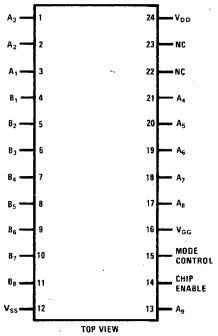
Hollerith to EBCDIC



Note 1: V_{SS} = +12V ±10%, V_{DD} = GND, V_{GG} = −12V ±10%.
Note 2: The Hollerith input data (lines 1 through 12) is considered to be from normally open switches returned, in the case of a punched hole, to GND as shown.

connection diagram

Dual-In-Line Package



Order Number MM4230QW/J or MM5230QW/J
See Package 11
Order Number MM5230QW/N
See Package 18

code conversion table

Hollerith to EBCDIC

	12	11	0		12 0	12 11	11 0	12 11 0	12	11	0		12 0	12 11	11 0	12 11 0	
	&	-	ϕ	SP	{	¦	}	70	49	59	69	`	80	90	A0	B0	8-1
1	A	J	/	1	a	j	~	B1	SOH	DC1	21	31	41	51	E1	71	9 -1
2	B	K	S	2	b	k	s	B2	STX	DC2	22	SYN	42	52	62	72	9 -2
3	C	L	T	3	c	l	t	B3	ETX	DC3	23	33	43	53	63	73	9 -3
4	D	M	U	4	d	m	u	B4	04	14	24	34	44	54	64	74	9 -4
5	E	N	V	5	e	n	v	B5	HT	15	LF	35	45	55	65	75	9 -5
6	F	O	W	6	f	o	w	B6	06	BS	ETB	36	46	56	66	76	9 -6
7	G	P	X	7	g	p	x	B7	DEL	17	ESC	EOT	47	57	67	77	9 -7
8	H	Q	Y	8	h	q	y	B8	08	CAN	28	38	48	58	68	78	9 -8
9	I	R	Z	9	i	r	z	B9	09	EM	29	39	NUL	DLE	20	30	9-8-1
8-2	[	]	\	:	8A	9A	AA	BA	0A	1A	2A	3A	CA	DA	EA	FA	9-8-2
8-3	.	$	,	#	8B	9B	AB	BB	VT	1B	2B	3B	CB	DB	EB	FB	9-8-3
8-4	<	*	%	@	8C	9C	AC	BC	FF	FS	2C	DC4	CC	DC	EC	FC	9-8-4
8-5	(	)	–	'	8D	9D	AD	BD	CR	GS	ENQ	NAK	CD	DD	ED	FD	9-8-5
8-6	+	;	>	=	8E	9E	AE	BE	SO	RS	ACK	3E	CE	DE	EE	FE	9-8-6
8-7	! ①	^ ②	?	"	8F	9F	AF	BF	SI	US	BEL	SUB	CF	DF	EF	FF	9-8-7

① may be "|"
② may be "¬"

Note: Unassigned entries e.g. AF refer to the EBCDIC code as a 16 x 16 table, column then row, in hexidecimal notation.

Note: The relationship between Hollerith as 256 valid punch combinations and EBCDIC as eight binary digits is well established. This converter conforms to this practice. The assignments shown in the table above are the recommendations of the American National Standards Institute. For details on alternate non-alphanumeric graphic and control codes, see ANSI x 3.26 – 1970.

NATIONAL

MOS ROMs

MM4230QX/MM5230QX
EBCDIC-8-to-ASCII-8 code converter

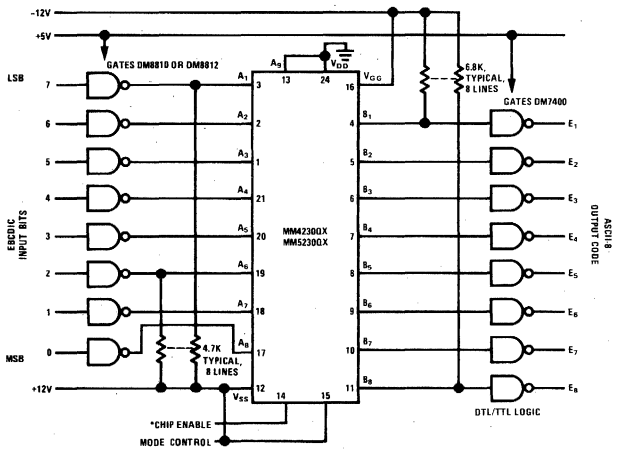
general description

The MM4230QX/MM5230QX is a 2048-bit read only memory that has been programmed to convert Extended Binary Coded Decimal Interchange Code (EBCDIC) to the American Standard Code for Information Interchange extended to eight bits (ASCII-8).

The conversion conforms to the practice established by the American National Standard ANSIx 3.26–1970. Exact details are shown in the code table.

For electrical, environmental and mechanical details, refer to the MM4230/MM5230 2048-bit read only memory data sheet.

typical application

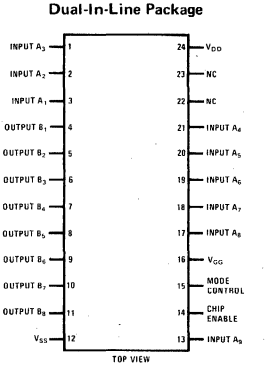


*Chip Enable = Logic "1" to obtain outputs.

Logic Levels:
DTL/TTL (except at MOS/ROM interface). Logic "1," +5.0V, NOM, Logic "0" ground, NOM.
MOS/ROM inputs and outputs. Logic "1," more negative, Logic "0," more positive.

connection diagram

Dual-In-Line Package

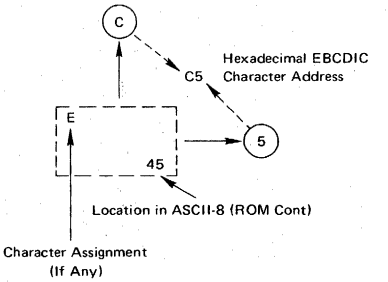


Order Number MM4230QX/J or MM5230QX/J
See Package 11

Order Number MM5230QX/N
See Package 18

code conversion table

4 5 6 7	Column → / Row ↓	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	
		0 0 0 0	0 0 0 1	0 0 1 0	0 0 1 1	0 1 0 0	0 1 0 1	0 1 1 0	0 1 1 1	1 0 0 0	1 0 0 1	1 0 1 0	1 0 1 1	1 1 0 0	1 1 0 1	1 1 1 0	1 1 1 1	
0 0 0 0	0	NUL 00	DLE 10	80	90	SP 20	& 26	– 2D	BA	C3	CA	D1	D8	¦ 7B	¦ 7D	\ 5C	0 30	0
0 0 0 1	1	SOH 01	DC1 11	81	91	A0	A9	/ 2F	BB	a 61	j 6A	~ 7E	D9	A 41	J 4A	9F	1 31	1
0 0 1 0	2	STX 02	DC2 12	82	SYN 16	A1	AA	B2	BC	b 62	k 6B	s 73	DA	B 42	K 4B	S 53	2 32	2
0 0 1 1	3	ETX 03	DC3 13	83	93	A2	AB	B3	BD	c 63	l 6C	t 74	DB	C 43	L 4C	T 54	3 33	3
0 1 0 0	4	9C	9D	84	94	A3	AC	B4	BE	d 64	m 6D	u 75	DC	D 44	M 4D	U 55	4 34	4
0 1 0 1	5	HT 09	85	LF 0A	95	A4	AD	B5	BF	e 65	n 6E	v 76	DD	E 45	N 4E	V 56	5 35	5
0 1 1 0	6	86	BS 08	ETB 17	96	A5	AE	B6	C0	f 66	o 6F	w 77	DE	F 46	O 4F	W 57	6 36	6
0 1 1 1	7	DEL 7F	87	ESC 1B	EOT 04	A6	AF	B7	C1	h 67	p 70	x 78	DF	G 47	:P 50	X 58	7 37	7
1 0 0 0	8	97	CAN 18	88	98	A7	B0	B8	C2	i 68	q 71	y 79	E0	H 48	Q 51	Y 59	8 38	8
1 0 0 1	9	8D	EM 19	89	99	A8	B1	B9	` 60	' 69	r 72	z 7A	E1	I 49	R 52	Z 5A	9 39	9
1 0 1 0	A	8E	92	8A	9A	[5B	] 5D	; 7C	: 3A	C4	CB	D2	E2	E8	EE	F4	FA	A
1 0 1 1	B	VT 0B	8F	8B	9B	. 2E	$ 24	. 2C	# 23	C5	CC	D3	E3	E9	EF	F5	FB	B
1 1 0 0	C	FF 0C	FS 1C	8C	DC4 14	< 3C	* 2A	% 25	@ 40	C6	CD	D4	E4	EA	F0	F6	FC	C
1 1 0 1	D	CR 0D	GS 1D	ENQ 05	NAK 15	(28	) 29	– 5F	' 27	C7	CE	D5	E5	EB	F1	F7	FD	D
1 1 1 0	E	SO 0E	RS 1E	ACK 06	9E	+ 2B	; 3B	> 3E	= 3D	C8	CF	D6	E6	EC	F2	F8	FE	E
1 1 1 1	F	SI 0F	US 1F	BEL 07	SUB 1A	! 21	^ 5E	? 3F	" 22	C9	DO	D7	E7	ED	F3	F9	EO FF	F



NATIONAL

MOS ROMs

MM4230QY/MM5230QY

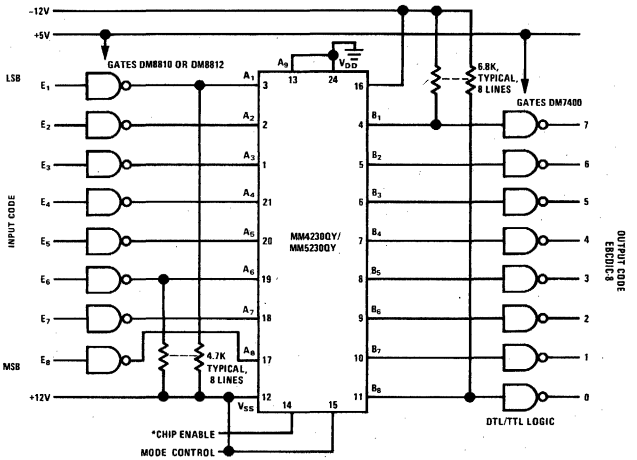
ASCII-8 -to- EBCDIC-8 code converter

general description

The MM4230QY/MM5230QY is a 2048-bit read only memory that has been programmed to convert the American Standard Code for Information Interchange extended to eight bits, (ASCII-8) to Extended Binary Coded Decimal Interchange Code (EBCDIC-8). The conversion conforms to the practice established by the American National Standard ANSIx3.26 1970. Exact details are shown in the code table.

For electrical, environmental and mechanical details, refer to the MM4230/MM5230 2048-bit read only memory data sheet.

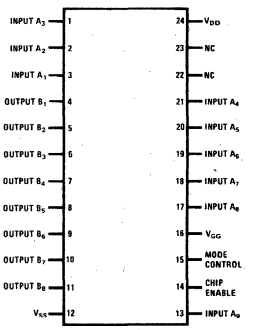
typical application



†Mode Control = Logic "0," A_8 = Logic "1."
*Chip Enable = Logic "1" to obtain outputs.
Logic Levels:
DTL/TTL (except at MOS/ROM interface). Logic "1," +5.0V, NOM. Logic "0," ground, NOM.
MOS/ROM inputs and outputs. Logic "1," more negative. Logic "0," more positive.

connection diagram

Dual-In-Line Package



Order Number MM4230QY/J or MM5230QY/J
See Package 11

Order Number MM5230QY/N
See Package 18

code conversion table

b_4 b_3 b_2 b_1	Row \ Column	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	Row \ Column
		b_8 0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	
		b_7 0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	
		b_6 0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	
		b_5 0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	
0 0 0 0	0	NUL 00	DLE 10	SP 40	0 0 F0	@ 7C	P D7	\ 79	p 97	20	30	41	58	76	9F	B8	DC	0
0 0 0 1	1	SOH 01	DC1 11	! ① 4F	1 F1	A C1	Q D8	a 81	q 98	21	31	42	59	77	AO	B9	DD	1
0 0 1 0	2	STX 02	DC2 12	" 7F	2 F2	B C2	R D9	b 82	r 99	22	1A	43	62	78	AA	BA	DE	2
0 0 1 1	3	ETX 03	DC3 13	# 7B	3 F3	C C3	S E2	c 83	s A2	23	33	44	63	80	AB	BB	DF	3
0 1 0 0	4	ECT 37	DC4 3C	$ 5B	4 F4	D C4	T E3	d 84	t A3	24	34	45	64	8A	AC	BC	EA	4
0 1 0 1	5	ENQ 2D	NAK 3D	% 6C	5 F5	E C5	U E4	e 85	u A4	15	35	46	65	8B	AD	BD	EB	5
0 1 1 0	6	ACK 2E	SYN 32	& 50	6 F6	F C6	V E5	f 86	v A5	06	36	47	66	8C	AE	BE	EC	6
0 1 1 1	7	BEL 2F	ETB 26	' 7D	7 F7	G C7	W E6	g 87	w A6	17	08	48	67	8D	AF	BF	ED	7
1 0 0 0	8	BS 16	CAN 18	(4D	8 F8	H C8	X E7	h 88	x A7	28	38	49	68	8E	B0	CA	EE	8
1 0 0 1	9	HT 05	EM 19	) 5D	9 F9	I C9	Y E8	i 89	y A8	29	39	51	69	8F	B1	CB	EF	9
1 0 1 0	A	IF 25	SUB 3F	* 5C	: 7A	J D1	Z E9	j 91	z A9	2A	3A	52	70	90	B2	CC	FA	10
1 0 1 1	B	VT OB	ESC 27	+ 4E	; 5E	K D2	[4A	k 92	{ CO	2B	3B	53	71	9A	B3	CD	FB	11
1 1 0 0	C	FF OC	FS 1C	, 6B	< 4C	L D3	\ E0	l 93	¦ 6A	2C	04	54	72	9B	B4	CE	FC	12
1 1 0 1	D	CR OD	GS 1D	- 60	= 7E	M D4	] 5A	m 94	} D0	09	14	55	73	9C	B5	CF	FD	13
1 1 1 0	E	SO OE	RS 1E	. 4B	> 6E	N D5	^ ② 5F	n 95	~ A1	0A	3E	56	74	9D	B6	DA	FE	14
1 1 1 1	F	SI OF	US 1F	/ 61	? 6F	O D6	_ 6D	o 96	DEL 07	1B	E1	57	75	9E	B7	DB	EO FF	15

1 may be "1"
2 may be "¬"
3 The top line in each entry to the table represents an assigned character (Columns 0 to 7). The bottom line in each entry is the corresponding EBCDIC Code, in hexadecimal notation.

The Hexadecimal EBCDIC entry is formed thus:

Eight EBCDIC bits

MSB 0 1 2 3 4 5 6 7 LSB

1st Digit 2nd Digit

Example: 0 1 0 1 1 1 0 0 or *

5 C

To convert ASCII-8 asterisk (*) to EBCDIC-8

E_8 E_1

* in ASCII is a 2A or binary 0010 1010

applying this as an address to the MM5230QY/MM4230QY

bit-0 bit-7

gives the output 0101 1100, which is an EBCDIC-8 asterisk.

NATIONAL

MOS ROMs

MM4230RS/MM5230RS binary to modulo-n divider code converter

general description

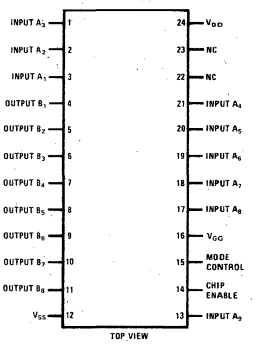
The MM4230RS/MM5230RS binary to modulo-n divider code converter is set up to generate the program input settings for a pair of DM7520/DM8520 modulo-n dividers, in order to divide by any binary number from one to 255. Detailed instructions for use of the DM7520/DM8520 are given in its data sheet.

Applying the required division ratio, in binary, to the inputs of the ROM as shown, generates two sets of four program inputs, one for each of the 2 DM7520/DM8520 dividers.

For electrical, environmental and mechanical details, refer to the MM4230/MM5230 data sheet.

connection diagram

Dual-In-Line Package

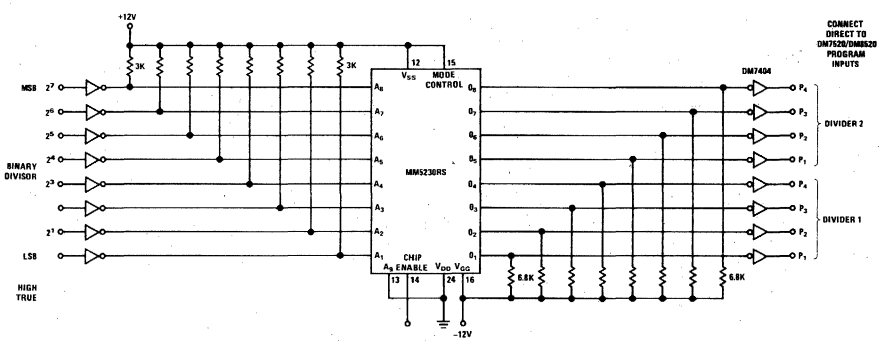


Order Number MM4230RS/J or MM5230RS/J
See Package 11

Order Number MM5230RS/N
See Package 18

typical application

Binary to Modulo-n Divider



code conversion table

SETTING								÷BY
DIVIDER 1				DIVIDER 2				
B_8	B_7	B_6	B_5	B_4	B_3	B_2	B_1	
0	1	1	1	1	1	1	1	255
1	0	1	1	1	1	1	1	254
0	1	0	1	1	1	1	1	253
0	0	1	0	1	1	1	1	252
1	0	0	1	0	1	1	1	251
0	1	0	0	1	0	1	1	250
0	0	1	0	0	1	0	1	249
0	0	0	1	0	0	1	0	248
0	0	0	0	1	0	0	1	247
0	0	0	0	0	1	0	0	246
0	0	0	0	0	0	1	0	245
0	0	0	0	0	0	0	1	244
1	0	0	0	0	0	0	0	243
1	1	0	0	0	0	0	0	242
1	1	1	0	0	0	0	0	241
0	1	1	1	0	0	0	0	240
1	0	1	1	1	0	0	0	239
1	1	0	1	1	1	0	0	238
0	1	1	0	1	1	1	0	237
0	0	1	1	0	1	1	1	236
0	0	0	1	1	0	1	1	235
0	0	0	0	1	1	0	1	234
0	0	0	0	0	1	1	0	233
0	0	0	0	0	0	1	1	232
1	0	0	0	0	0	0	1	231
0	1	0	0	0	0	0	0	230
0	0	1	0	0	0	0	0	229
1	0	0	1	0	0	0	0	228
1	1	0	0	1	0	0	0	227
0	1	1	0	0	1	0	0	226
1	0	1	1	0	0	1	0	225
0	1	0	1	1	0	0	1	224
0	0	1	0	1	1	0	0	223
0	0	0	1	0	1	1	0	222
0	0	0	0	1	0	1	1	221
0	0	0	0	0	1	0	1	220
1	0	0	0	0	0	1	0	219
1	1	0	0	0	0	0	1	218
0	1	1	0	0	0	0	0	217
1	0	1	1	0	0	0	0	216
0	1	0	1	1	0	0	0	215
1	0	1	0	1	1	0	0	214
1	1	0	1	0	1	1	0	213
1	1	1	0	1	0	1	1	212
0	1	1	1	0	1	0	1	211
0	0	1	1	1	0	1	0	210
0	0	0	1	1	1	0	1	209
0	0	0	0	1	1	1	0	208
1	0	0	0	0	1	1	1	207
0	1	0	0	0	0	1	1	206
1	0	1	0	0	0	0	1	205
1	1	0	1	0	0	0	0	204
1	1	1	0	1	0	0	0	203
1	1	1	1	0	1	0	0	202
0	1	1	1	1	0	1	0	201
0	0	1	1	1	1	0	1	200
1	0	0	1	1	1	1	0	199
0	1	0	0	1	1	1	1	198
0	0	1	0	0	1	1	1	197
0	0	0	1	0	0	1	1	196
1	0	0	0	1	0	0	1	195
1	1	0	0	0	1	0	0	194
1	1	1	0	0	0	1	0	193
0	1	1	1	0	0	0	1	192
0	0	1	1	1	0	0	0	191
0	0	0	1	1	1	0	0	190
1	0	0	0	1	1	1	0	189
0	1	0	0	0	1	1	1	188
1	0	1	0	0	0	1	1	187
1	1	0	1	0	0	0	1	186
0	1	1	0	1	0	0	0	185
0	0	1	1	0	1	0	0	184
1	0	0	1	1	0	1	0	183
0	1	0	0	1	1	0	1	182
0	0	1	0	0	1	1	0	181
1	0	0	1	0	0	1	1	180
0	1	0	0	1	0	0	1	179
0	0	1	0	0	1	0	0	178
1	0	0	1	0	0	1	0	177
1	1	0	0	1	0	0	1	176
1	1	1	0	0	1	0	0	175
0	1	1	1	0	0	1	0	174
1	0	1	1	1	0	0	1	173
0	1	0	1	1	1	0	0	172
1	0	1	0	1	1	1	0	171
1	1	0	1	0	1	1	1	170
0	1	1	0	1	0	1	1	169
1	0	1	1	0	1	0	1	168
1	1	0	1	1	0	1	0	167
0	1	1	0	1	1	0	1	166
1	0	1	1	0	1	1	0	165
1	1	0	1	1	0	1	1	164
1	1	1	0	1	1	0	1	163
0	1	1	1	0	1	1	0	162
0	0	1	1	1	1	1	0	161
0	0	0	1	1	1	1	1	160
0	0	0	0	1	1	1	1	159
0	0	0	0	0	1	1	1	158
1	0	0	0	0	0	1	1	157
0	1	0	0	0	0	0	1	156
1	0	1	0	0	0	0	0	155
0	1	0	1	0	0	0	0	154
0	0	1	0	1	0	0	0	153
0	0	0	1	0	1	0	0	152
0	0	0	0	1	0	1	0	151
1	0	0	0	0	1	0	1	150
0	1	0	0	0	0	1	0	149
0	0	1	0	0	0	0	1	148
0	0	0	1	0	0	0	0	147
0	0	0	0	1	0	0	0	146
1	0	0	0	0	1	0	0	145
1	1	0	0	0	0	1	0	144
1	1	1	0	0	0	0	1	143
1	1	1	1	0	0	0	0	142
0	1	1	1	1	0	0	0	141
0	0	1	1	1	1	0	0	140
0	0	0	1	1	1	1	0	139
1	0	0	0	1	1	1	1	138
1	1	0	0	0	1	1	1	137
0	1	1	0	0	0	1	1	136
0	0	1	1	0	0	0	1	135
0	0	0	1	1	0	0	0	134
1	0	0	0	1	1	0	0	133
0	1	0	0	0	1	1	0	132
0	0	1	0	0	0	1	1	131
0	0	0	1	0	0	0	1	130
1	0	0	0	1	0	0	0	129
0	1	0	0	0	1	0	0	128
0	0	1	0	0	0	1	0	127
1	0	0	1	0	0	0	1	126
0	1	0	1	1	0	1	1	125
1	0	0	1	1	0	1	0	124
0	1	0	1	1	0	0	1	123
0	0	1	0	1	1	0	0	122
1	0	0	1	0	1	1	0	121
1	1	0	0	1	0	1	1	120
0	1	1	0	0	1	0	1	119
0	0	1	1	0	0	1	0	118
1	0	0	1	1	0	0	1	117
1	1	0	0	1	1	0	0	116
0	1	1	0	0	1	1	0	115
1	0	1	1	0	0	1	1	114
1	1	0	1	1	0	0	1	113
1	1	1	0	1	1	0	0	112
1	1	1	1	0	1	1	0	111
0	1	1	1	1	0	1	1	110
1	0	1	1	1	1	0	1	109
0	1	0	1	1	1	1	0	108
1	0	1	0	1	1	1	1	107
0	1	0	1	0	1	1	0	106
1	0	1	0	1	0	1	1	105
0	1	0	1	0	1	1	0	104
1	0	1	0	1	0	1	0	103
1	1	0	1	0	1	0	1	102
0	1	1	0	1	0	1	0	101
0	0	1	1	0	1	0	1	100
0	0	0	1	1	0	1	0	99
1	0	0	0	1	1	0	1	98
1	1	0	0	0	1	1	0	97
1	1	1	0	0	0	1	1	96
1	1	1	1	0	0	0	0	95
1	1	1	1	1	0	0	0	94
1	1	1	1	1	1	0	0	93
1	1	1	1	1	1	1	0	92

NATIONAL

MOS ROMs

MM4231/MM5231 2048-bit read only memory

general description

The MM4231/MM5231 is a 2048-bit static read only memory. It is a P-channel enhancement mode monolithic MOS integrated circuit utilizing low threshold voltage technology. The device is a non-volatile memory organized as a 256-8 bit words or 512-4 bit words. Programming of the memory contents is accomplished by changing one mask during the device fabrication.

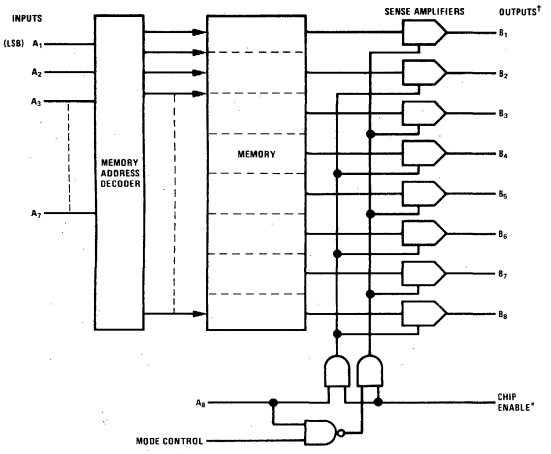
features

- Bipolar compatibility — +5V, −12V operation
- High speed operation — 640 ns typ.
- Static operation — No clocks required
- Common data busing — Output wire AND capability
- Chip enable output control

applications

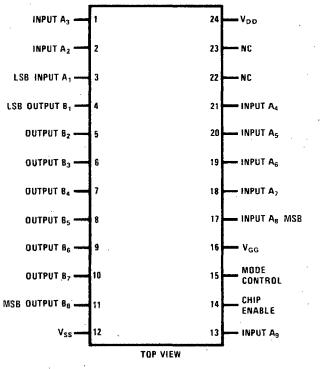
- Code conversion
- Random logic synthesis
- Table look-up
- Character generator
- Microprogramming

block and connection diagrams



† The outputs are open when Disabled.
* The output is enabled by applying a Logic "1" to the Chip Enable line.

Dual-In-Line Package



Order Number MM4231J
or MM5231J
See Package 11

Order Number MM5231N
See Package 18

Note: For programming information see AN-100.

absolute maximum ratings

V_{GG} Supply Voltage		V_{SS} – 20V
V_{DD} Supply Voltage		V_{SS} – 20V
Input Voltage		$(V_{SS} - 20)V < V_{IN} < (V_{SS} + 0.3)V$
Storage Temperature		−65°C to +150°C
Operating Temperature	MM4231	−55°C to +125°C
	MM5231	0°C to +70°C
Lead Temperature (Soldering, 10 sec)		300°C

electrical characteristics

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage Levels					
MOS to TTL					
Logical "1"	6.8 kΩ ±5% to V_{DD} Plus One			+0.4	V
Logical "0"	Standard Series 54/74 Gate	2.4			V
Output Current Capability					
Logical "0"	V_{OUT} = 2.4V	2.5			mA
Input Voltage Levels					
Logical "1"				V_{SS} – 4.2	V
Logical "0"		V_{SS} – 2.0			V
Power Supply Current	T_A = 25°C				
I_{DD}	V_{SS} = +5V		15	30	mA
I_{GG} (Note 1)	$V_{GG} = V_{DD}$ = −12V			1	μA
Input Leakage	V_{IN} = −12V			1	μA
Input Capacitance	f = 1.0 MHz, V_{IN} = 0V		5		pF
V_{GG} Capacitance	f = 1.0 MHz, V_{IN} = 0V		15		pF
Address Time (Note 2)	See Timing Diagram				
T_{ACCESS}	T_A = 25°C V_{SS} = +5.0V $V_{GG} = V_{DD}$ = −12.0V		640	950	ns
Output AND Connections (Note 3)	6.8 kΩ ±5% to V_{DD} Plus One Standard Series 54/74 Gate			8	

Note 1: These specifications apply for V_{SS} = +5V ±5%, $V_{GG} = V_{DD}$ = −12V, ±5%, and T_A = −55°C to +125°C (MM4231), T_A = −25°C to +70°C (MM5231) unless otherwise specified.

Note 2: The V_{GG} supply may be clocked to reduce device power without affecting access time.

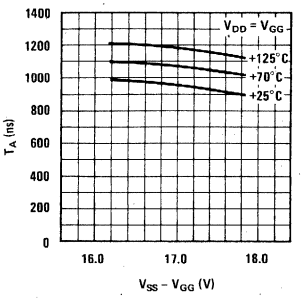
Note 3: Address time is measured from the change of data on any input or Chip Enable line to the output of a TTL gate. (See Timing Diagram.) See curves for guaranteed limit over temperature.

Note 4: The address time in the TTL load configuration follows the equation:
T_{ACCESS} = The specified limit + (N – 1) (50) ns.
Where N = Number of AND connections.

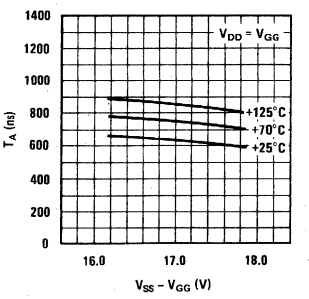
Note 5: Capacitances are measured on a lot sample basis only.

performance characteristics

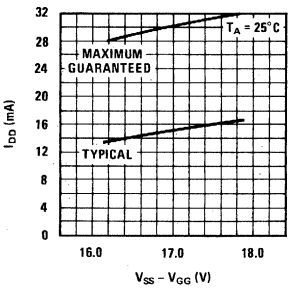
Guaranteed Access Time (T_A) vs Power Supply Voltage



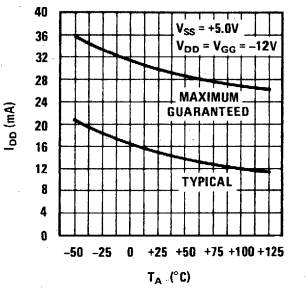
Typical Access Time (T_A) vs Power Supply Voltage



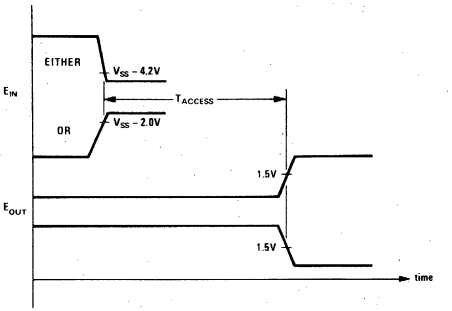
Power Supply Current vs Power Supply Voltage

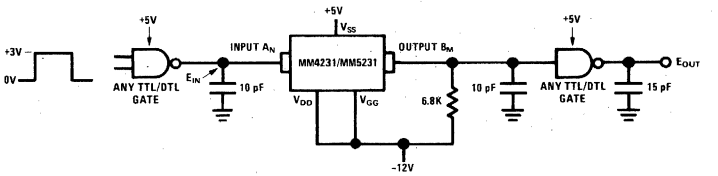


Power Supply Current vs Ambient Temperature



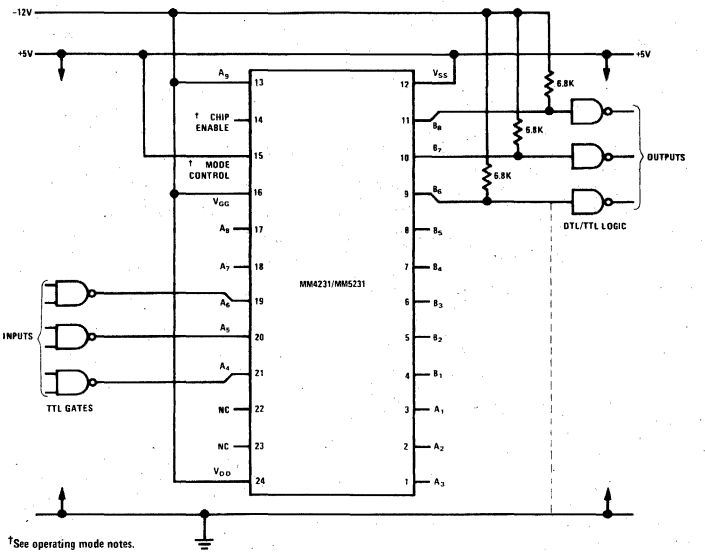
timing diagram/address time





typical application

256 x 8 Bit ROM Showing TTL Interface



Operating Modes

256 x 8 ROM connection (shown)
Mode Control – Logic "0"
A_9 – Logic "1"

512 x 4 ROM connection
Mode Control – Logic "1"
A_9 – Logic "0" Enables the odd (B_1, B_3 . . . B_9) outputs
– Logic "1" Enables the even (B_2, B_4 . . . B_8) outputs.

The outputs are "Enabled" when a logic "1" is applied to the Chip Enable line.

Logic levels are negative true MOS logic.

Mode Control should be "hard wired" to V_{DD} (Logical "1") or V_{SS} (Logical "0").

The logic levels are in negative voltage logic notation.

MM4231RP/MM5231RP EBCDIC to ASCII-7 code converter

general description

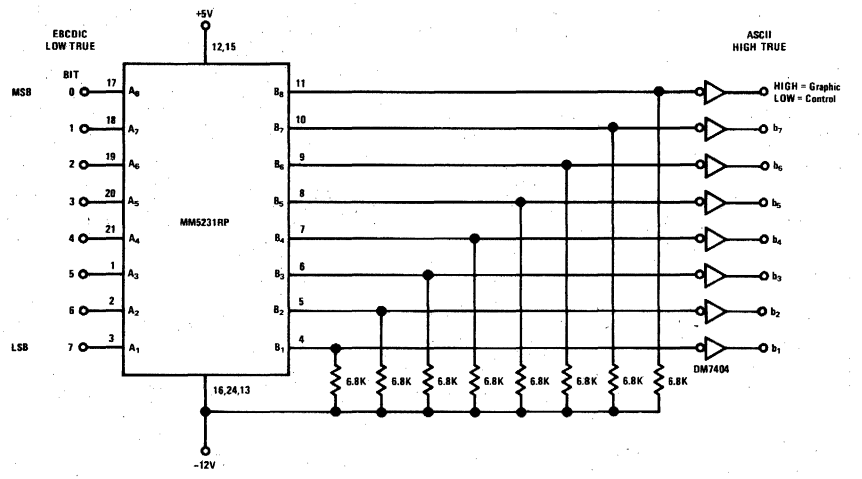
The MM4231RP/MM5231RP is a 2048-bit read-only memory that has been programmed to convert from EBCDIC, an extended binary coded decimal interchange code used in the IBM1130 computer, to ASCII-7, the American Standard Code for Information Interchange in seven bits.

This conversion differs from the ANSI x 3.26 conversion of the MM4230QX/MM5230QX in that it follows certain earlier IBM1130 character assignments. Also certain EBCDIC control codes are arbitrarily preserved and translated (see translation chart on truth table).

For electrical, environmental and mechanical details, refer to the MM4231/MM5231 data sheet.

typical application

EBCDIC TO ASCII-7



Order Number MM4231RP/J or MM5231RP/J
See Package 11

Order Number MM5231RP/N
See Package 18

code conversion tables

ROM ADDRESS	FUNCTION INPUT EBCDIC SYMBOL	FUNCTION OUTPUT ASCII SYMBOL	CODE INPUT MSB							LSB	CC/G	OUTPUT MSB						LSB
0	NULL	NUL	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	SOH	SOH	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1
2	STX	STX	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0
3	ETX	ETX	0	0	0	0	0	0	1	1	0	0	0	0	0	0	1	1
4	PF		0	0	0	0	0	1	0	0								
5	HT	HT									0	0	0	0	1	0	0	1
6	LC																	
7	DEL	DEL									0	1	1	1	1	1	1	1
8																		
9																		
10	SMM																	
11	VT	VT									0	0	0	0	1	0	1	1
12	FF	FF									0	0	0	0	1	1	0	0
13	CR	CR									0	0	0	0	1	1	0	1
14	SO	SO									0	0	0	0	1	1	1	0
15	S1	S1									0	0	0	0	1	1	1	1
16	DLE	DLE									0	0	0	1	0	0	0	0
17	DC1	DC1									0	0	0	1	0	0	0	1
18	DC2	DC2									0	0	0	1	0	0	1	0
19	DC3	DC3									0	0	0	1	0	0	1	1
20	RES										1	1	1	0	0	0	0	0
21	NL	\									1	1	0	1	1	1	0	0
22	BS	BS									0	0	0	0	1	0	0	0
23	IDL																	
24	CAN	CAN									0	0	0	1	1	0	0	0
25	EM	EM									0	0	0	1	1	0	0	1
26	CC																	
27	CUI																	
28	FLS	FS									0	0	0	1	1	1	0	0
29	GS	GS									0	0	0	1	1	1	0	1
30	RDS	RS									0	0	0	1	1	1	1	0
31	US	US									0	0	0	1	1	1	1	1
32	DS																	
33	SOS																	
34	FS		CONTINUING BINARY SEQUENCE															
35																		
36	BYP										0	0	0	0	0	0	0	0
37	LF	LF									0	0	0	0	1	0	1	0
38	EOB	ETB									0	0	0	1	0	1	1	1
39	PRE	ESC									0	0	0	1	1	0	1	1
40																		
41																		
42	SM																	
43	CU2																	
44																		
45	ENQ	ENQ									0	0	0	0	0	1	0	1
46	ACK	ACK									0	0	0	0	0	1	1	0
47	BEL	BEL									0	0	0	0	0	1	1	1
48																		
49																		
50	SYN	SYN									0	0	0	1	0	1	1	0
51																		
52	PN																	
53	RS	DC4									0	0	0	1	0	1	0	0
54	UC																	
55	EOT	EOT									0	0	0	0	0	1	0	0
56																		
57																		
58																		
59	CU3																	
60	DCA																	
61	NAK	NAK									0	0	0	0	1	0	1	0	1
62																		
63	SUB	SUB									0	0	0	0	1	1	0	1	0
			A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	B_8	B_7	B_6	B_5	B_4	B_3	B_2	B_1

code conversion tables(con't)

ROM ADDRESS	FUNCTION INPUT EBCDIC SYMBOL	FUNCTION OUTPUT ASCII SYMBOL	CODE INPUT MSB–LSB	CC/G	OUTPUT MSB						LSB
64	SP	SP		1	0	1	0	0	0	0	0
65											
66											
67											
68											
69											
70											
71											
72											
73											
74	¢	~		1	1	1	1	1	1	1	0
75	.	.		1	0	1	0	1	1	1	0
76	<	<		1	0	1	1	1	1	0	0
77	(	(		1	0	1	0	1	0	0	0
78	+	+		1	0	1	0	1	0	1	1
79	!	¦		1	1	1	1	1	1	0	0
80	&	&		1	0	1	0	0	1	1	0
81											
82											
83											
84											
85											
86											
87											
88											
89											
90	!	!		1	0	1	0	0	0	0	1
91	$	$		1	0	1	0	0	1	0	0
92	*	*		1	0	1	0	1	0	1	0
93	)	)		1	0	1	0	1	0	0	1
94	;	;	CONTINUING BINARY SEQUENCE	1	0	1	1	1	0	1	1
95	¬	^		1	1	0	1	1	1	1	0
96	-	-		1	0	1	0	1	1	0	1
97	/	/		1	0	1	0	1	1	1	1
98											
99											
100											
101											
102											
103											
104											
105											
106											
107	,	,		1	0	1	0	1	1	0	0
108	%	%		1	0	1	0	0	1	0	1
109	—	—		1	1	0	1	1	1	1	1
110	>	>		1	0	1	1	1	1	1	0
111	?	?		1	0	1	1	1	1	1	1
112											
113											
114											
115											
116											
117											
118											
119											
120											
121											
122	:	:		1	0	1	1	1	0	1	0
123	#	#		1	0	1	0	0	0	1	1
124	@	@		1	1	0	0	0	0	0	0
125	'	'		1	0	1	0	0	1	1	1
126	=	=		1	0	1	1	1	1	0	1
127	"	"		1	0	1	0	0	0	1	0
			A_8 A_7 A_6 A_5 A_4 A_3 A_2 A_1	B_8	B_7	B_6	B_5	B_4	B_3	B_2	B_1

code conversion tables(con't)

ROM ADDRESS	FUNCTION INPUT EBCDIC SYMBOL	FUNCTION OUTPUT ASCII SYMBOL	CODE INPUT MSB ... LSB	CODE OUTPUT CC/G	OUTPUT MSB						LSB
128											
129	a	a		1	1	1	0	0	0	0	1
130	b	b		1	1	1	0	0	0	1	0
131	c	c		1	1	1	0	0	0	1	1
132	d	d		1	1	1	0	0	1	0	0
133	e	e		1	1	1	0	0	1	0	1
134	f	f		1	1	1	0	0	1	1	0
135	g	g		1	1	1	0	0	1	1	1
136	h	h		1	1	1	0	1	0	0	0
137	i	i		1	1	1	0	1	0	0	1
138											
139	¦	¦		1	1	1	1	1	0	1	1
140											
141											
142											
143											
144											
145	j	j		1	1	1	0	1	0	1	0
146	k	k		1	1	1	0	1	0	1	1
147	l	l		1	1	1	0	1	1	0	0
148	m	m		1	1	1	0	1	1	0	1
149	n	n		1	1	1	0	1	1	1	0
150	o	o		1	1	1	0	1	1	1	1
151	p	p		1	1	1	1	0	0	0	0
152	q	q		1	1	1	1	0	0	0	1
153	r	r		1	1	1	1	0	0	1	0
154											
155	}	}		1	1	1	1	1	1	0	1
156											
157											
158			CONTINUING BINARY SEQUENCE								
159											
160											
161											
162	s	s		1	1	1	1	0	0	1	1
163	t	t		1	1	1	1	0	1	0	0
164	u	u		1	1	1	1	0	1	0	1
165	v	v		1	1	1	1	0	1	1	0
166	w	w		1	1	1	1	0	1	1	1
167	x	x		1	1	1	1	1	0	0	0
168	y	y		1	1	1	1	1	0	0	1
169	z	z		1	1	1	1	1	0	1	0
170											
171											
172											
173	[	[		1	1	1	0	1	1	0	1	1
174											
175											
176											
177											
178											
179											
180											
181											
182											
183											
184											
185											
186											
187											
188											
189	]	]		1	1	0	1	1	1	0	1
190											
191											
			A_8 A_7 A_6 A_5 A_4 A_3 A_2 A_1	B_8	B_7	B_6	B_5	B_4	B_3	B_2	B_1

code conversion tables(con't)

	FUNCTION		CODE															
	INPUT	OUTPUT	INPUT								OUTPUT							
ROM ADDRESS	EBCDIC SYMBOL	ASCII SYMBOL	MSB							LSB	CC/G	MSB						LSB
192	+ ZERO																	
193	A	A									1	1	0	0	0	0	0	1
194	B	B									1	1	0	0	0	0	1	0
195	C	C									1	1	0	0	0	0	1	1
196	D	D									1	1	0	0	0	1	0	0
197	E	E									1	1	0	0	0	1	0	1
198	F	F									1	1	0	0	0	1	1	0
199	G	G									1	1	0	0	0	1	1	1
200	H	H									1	1	0	0	1	0	0	0
201	I	I									1	1	0	0	1	0	0	1
202																		
203																		
204																		
205																		
206																		
207																		
208	–ZERO																	
209	J	J									1	1	0	0	1	0	1	0
210	K	K									1	1	0	0	1	0	1	1
211	L	L									1	1	0	0	1	1	0	0
212	M	M									1	1	0	0	1	1	0	1
213	N	N									1	1	0	0	1	1	1	0
214	O	O									1	1	0	0	1	1	1	1
215	P	P									1	1	0	1	0	0	0	0
216	Q	Q									1	1	0	1	0	0	0	1
217	R	R									1	1	0	1	0	0	1	0
218																		
219																		
220																		
221																		
222			CONTINUING BINARY SEQUENCE															
223																		
224																		
225																		
226	S	S									1	1	0	1	0	0	1	1
227	T	T									1	1	0	1	0	1	0	0
228	U	U									1	1	0	1	0	1	0	1
229	V	V									1	1	0	1	0	1	1	0
230	W	W									1	1	0	1	0	1	1	1
231	X	X									1	1	0	1	1	0	0	0
232	Y	Y									1	1	0	1	1	0	0	1
233	Z	Z									1	1	0	1	1	0	1	0
234																		
235																		
236																		
237																		
238																		
239																		
240	0	0									1	0	1	1	0	0	0	0
241	1	1									1	0	1	1	0	0	0	1
242	2	2									1	0	1	1	0	0	1	0
243	3	3									1	0	1	1	0	0	1	1
244	4	4									1	0	1	1	0	1	0	0
245	5	5									1	0	1	1	0	1	0	1
246	6	6									1	0	1	1	0	1	1	0
247	7	7									1	0	1	1	0	1	1	1
248	8	8									1	0	1	1	1	0	0	0
249	9	9									1	0	1	1	1	0	0	1
250																		
251			1	1	1	1	1	0	1	1								
252			1	1	1	1	1	1	0	0								
253			1	1	1	1	1	1	0	1								
254			1	1	1	1	1	1	1	0								
255			1	1	1	1	1	1	1	1								
			A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	B_8	B_7	B_6	B_5	B_4	B_3	B_2	B_1

MOS ROMs

MM4232/MM5232 4096-bit static read-only memory

general description

The MM4232/MM5232 4096-bit static read-only memory is a P-channel enhancement mode monolithic MOS integrated circuit utilizing a low threshold voltage technology to achieve bipolar compatibility. TRI-STATE™ outputs provide wire ORed capability without loading common data lines or reducing system access times. The ROM is organized in a 512 word x 8-bit or 1024 word x 4-bit memory organization that is controlled by the mode control input. Programmable Chip Enables (CE_1 and CE_2) provide logic control of up to 16K bits without external logic. A separate output supply lead is provided to reduce internal power dissipation in the output stages.

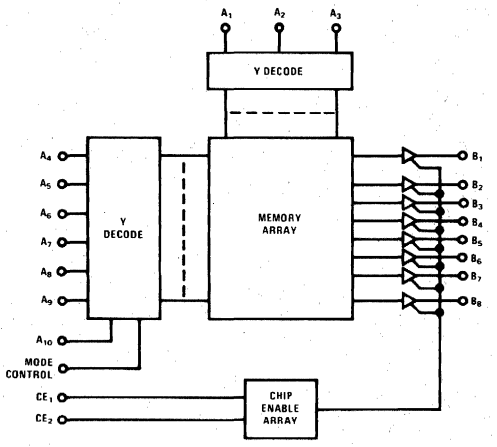
features

■ Bipolar compatibility	No external components required
■ Standard supplies	+5V, −12V
■ Bus ORable output	TRI-STATE outputs
■ Static operation	No clocks required
■ Multiple ROM control	Two-programmable Chip Enable lines

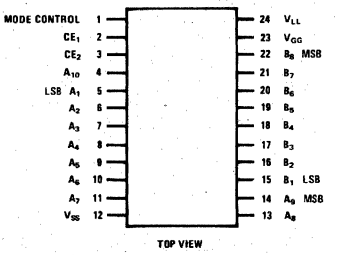
applications

- Character generator
- Random logic synthesis
- Microprogramming
- Table look-up

logic and connection diagrams



Dual-In-Line Package



Order Number MM4232J or MM5232J
See Package 11

Order Number MM5232N
See Package 18

Note: For programming information see AN-100.

absolute maximum ratings

V_{GG} Supply Voltage		V_{SS} – 20V
V_{LL} Supply Voltage		V_{SS} – 20V
Input Voltage		$(V_{SS} - 20)\ V < V_{IN} < (V_{SS} + .03)V$
Storage Temperature Range		−65°C to +150°C
Operating Temperature Range	MM4232	−55°C to +125°C
	MM5232	0°C to +70°C
Lead Temperature (Soldering, 10 sec)		300°C

electrical characteristics POSITIVE LOGIC

T_A within operating temperature range, V_{SS} = +5.0V ±5%, $V_{GG} = V_{DD}$ = −12V ±5%, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage Levels					
Logical "0", V_{OL}	I_L = 1.6 mA Sink			.4	V
Logical "1", V_{OH}	I_L = 100 μA Source	2.4			V
Input Voltage Levels					
Logical "0", V_{IL}		V_{GG}		V_{SS} – 4.0	V
Logical "1", V_{IH}		V_{SS} – 2.0		V_{SS} + 0.3	V
Power Supply Current					
I_{SS} (Note 4)	V_{SS} = 5, V_{GG} = −12, V_{LL} = −12, T_A = 25°C		23	37	mA
I_{SS} (Note 4)	V_{SS} = 5, V_{GG} = −12, V_{LL} = −3, T_A = 125°C		12	20	mA
Input Leakage	$V_{IN} = V_{SS}$ – 10V			1	μA
Input Capacitance (Note 1)	f = 1.0 MHz, V_{IN} = 0V		5	15	pF
Output Capacitance (Note 1)	f = 1.0 MHz, V_{IN} = 0V		4	10	pF
Address Time (Note 2)	T_A = 25°C, V_{SS} = 5	150		1000	ns
T_{ACCESS}	$V_{GG} = V_{LL}$ = −12V				
Output AND Connections (Note 3)				20	

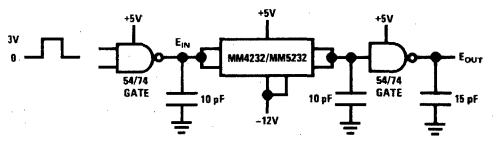
Note 1: Capacitances are measured periodically only.

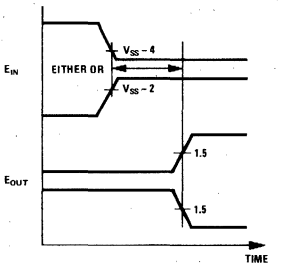
Note 2: Address time is measured from the change of data on any input or Chip Enable line to the output of a TTL gate. (See Timing Diagram.)

Note 3: The address time follows the following equation: T_{ACCESS} = the specified limit + (N − 1) x 25 ns where N = Number of AND connections.

Note 4: Outputs open.

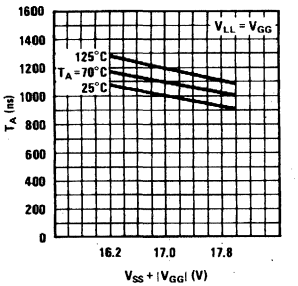
timing diagram/address time



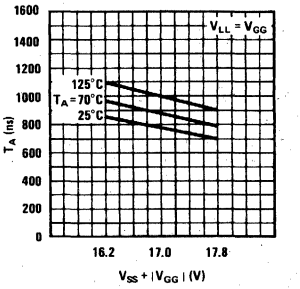


performance characteristics

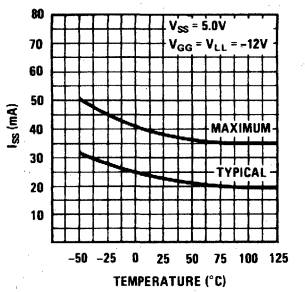
Guaranteed Access Time vs Supply Voltage



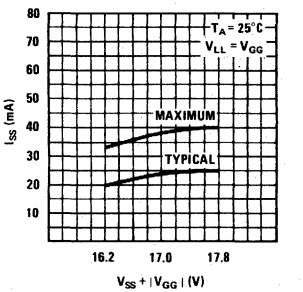
Typical Access Time vs Supply Voltage



Power Supply Current vs Temperature



Power Supply Current vs Voltage



typical applications

TTL/MOS Interface

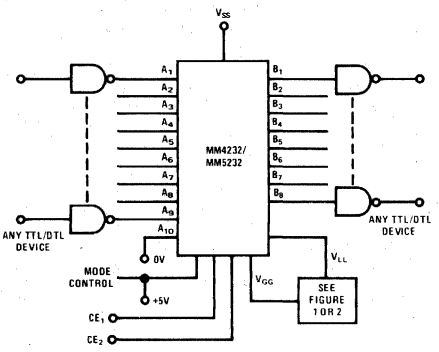
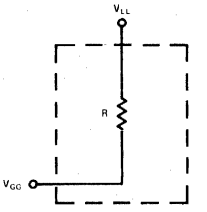
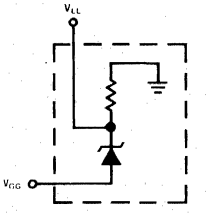


FIGURE 1. Power Saver for Small Memory Arrays



ASSUME $|V_{LL}|_{MIN} = |-3V|$
$V_{GG} - V_{LL}$ MIN = R (1.6 mA) (N) where N = 7 for 5 x 7 font.
N = 8 for 6 x 8 font.

FIGURE 2. Power Saver for Large Memory Arrays



Operating Modes

512 x 8 ROM connection
Mode Control = V_{IH}
$A_{10} = V_{IL}$

1024 x 4 ROM connection
Mode Control = V_{IL}
$A_{10} = V_{IL}$ enables the odd ($B_1 \ldots B_7$) outputs
V_{IH} enables the even ($B_2 \ldots B_8$) outputs

Note: Both chip enables may be programmed to provide any of four combinations. Example if $CE_1 = 1$ and $CE_2 = 1$ outputs (Positive Logic) would be enabled only when device pins 2 and 3 are Logic "1". The outputs will be in the third state when disabled.

NATIONAL

MOS ROMs

MM4232/MM5232 AEI, AEJ, AEK sine look up table

general description

The MM4232/MM5232 AEI, AEJ and AEK are all P-channel enhancement mode MOS read-only memories, each storing 4096 bits. They are programmed to generate the sine function of any angle expressed as a binary fraction of a right-angle. They may be combined and arranged to provide a look-up table of varying resolution and accuracy, to meet almost any system requirement for generation of the sine function.

application information

Figures 1 through 4 show the four ways that these parts may be combined. The table shows the performance of all combinations.

performance specifications

FIGURE	ROM NO. USED	RESOLUTION (= INPUT WORD LENGTH)	OUTPUT WORD LENGTH	ACCURACY	ADDER PACKAGES REQUIRED
1	AEI	9 bits	8 bits	+0 -1 bit in 8	0
2	AEI + AEJ	9 bits	16 bits	± 1/2 bit in 16	0
3	AEI + AEJ + AEK	12 bits	16 bits	± 3/4 bit in 14	4
4	AEI + AEJ + 2 AEK's	15 bits	16 bits	±1 bit in 14	6

SINE LOOK-UP TABLE WITH HIGH RESOLUTION AND ACCURACY

Theoretical Background

The table is based upon the equation:

$$\sin (M + L) = \sin M \cos L + \cos M \sin L \qquad (1)$$

By splitting M and L each into two parts MM, ML, and LM, LL, and (assuming $M \gg L$) the following equation is obtained.

$$\begin{aligned}\sin (M + L) &\approx \sin (MM + ML) \qquad (2)\\ &+ \cos (MM + 1/2 \text{ LSB of } MM) \sin LM\\ &+ \cos (MM + 1/2 \text{ LSB of } MM) \sin LL\\ &\approx \sin (MM + ML)\\ &+ \cos (MM + 1/2 \text{ LSB of } MM) (\sin LM + \sin LL)\end{aligned}$$

The following approximations have been used:

$$\cos (LM + LL) \approx 1$$
$$\sin (LM + LL) \approx \sin (LM) + \sin (LL)$$
$$\cos (MM + ML) \approx \cos (MM + 1/2 \text{ LSB of } MM)$$

By taking MM = 6 bits, ML = 3 bits, LM = 3 bits, and LL = 3 bits, 15 bits resolution is obtained. The accuracy has been computed by comparing the values of Equation 2 with the ideal value of the sine of an angle θ resolved into 2^{15} increments in the range $0 \leq \theta < \pi/2$.

This error, due to the mathematical approximation, is $\pm 3.2 \times 10^{-5}$ maximum, corresponding to ±1 bit in 15 bits. In addition to the mathematical error, an inevitable round-off error in the 16th bit is introduced. As there are 3 LSB outputs to be added (Figure 4), the maximum round-off error will be ±1-1/2 bit in 16 bits or $\pm 2.3 \times 10^{-5}$. The theoretical maximum total error will then be $\pm (3.2 + 2.3) \times 10^{-5} = \pm 5.5 \times 10^{-5}$, which is slightly less than ±1 bit in 14 bits.

A computer analysis shows that the actual errors in the table as implemented are as follows:

$+4.4 \times 10^{-5}$ (at 61.872°)

-4.7×10^{-5} (at 83.142°)

As the sine function is very linear in the LM-LL range, the third term of Equation 2 can be considered as being $1/(2)^3$ of the second term without significant error. Therefore, the same pattern can be used for the two lower ROMs in Figure 4, and a total of three different masks are needed. In addition, six 4-bit adders are used.

Order Number MM4232J or MM5232J
See Package 11

Order Number MM5232N
See Package 18

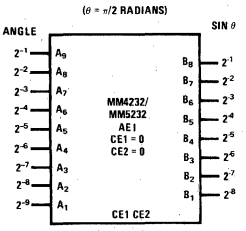


FIGURE 1

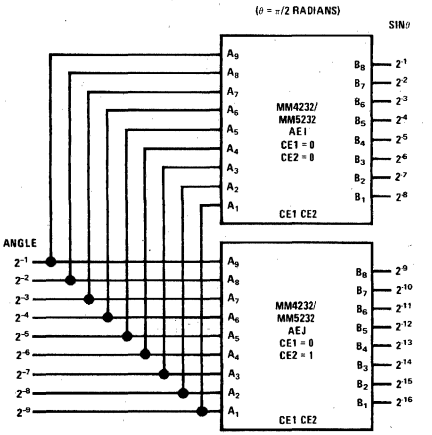


FIGURE 2

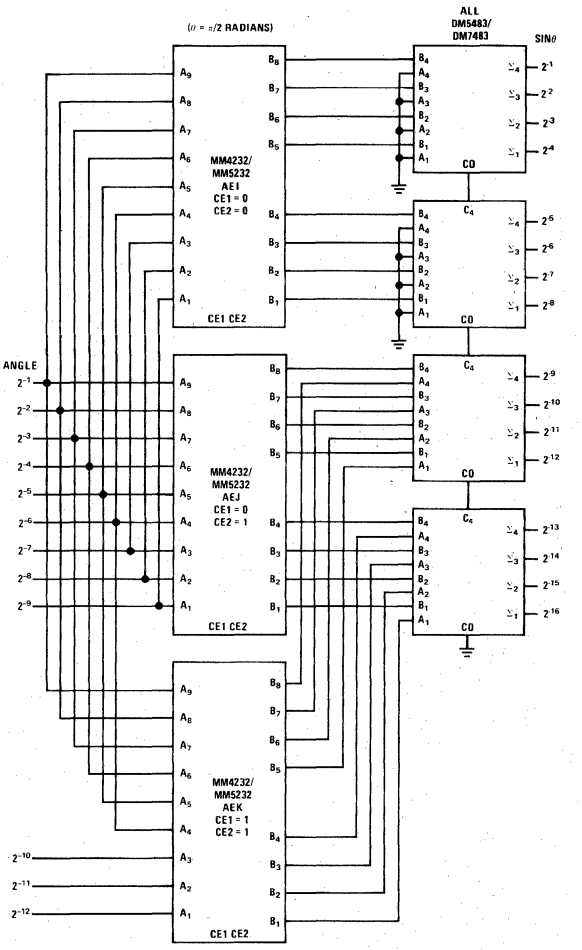


FIGURE 3.

Note: Angles are expressed as binary fractions of a right-angle.

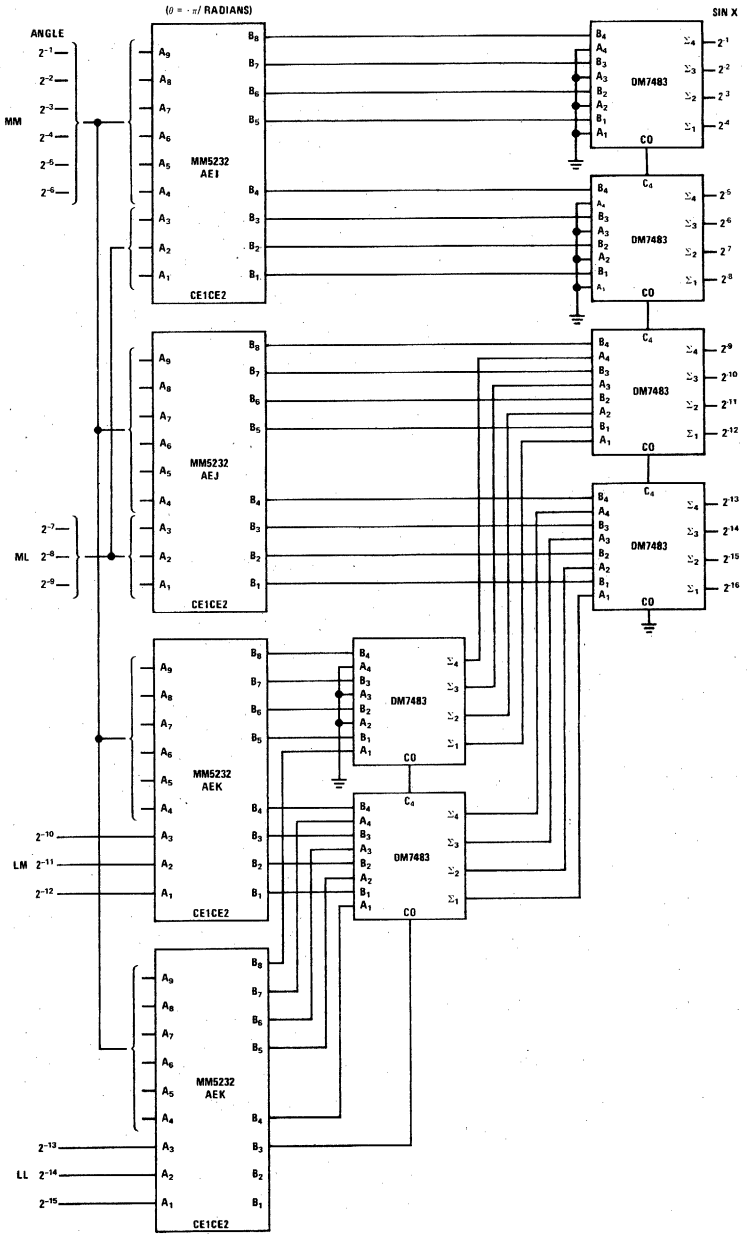


FIGURE 4

Note: Angles are expressed as binary fractions of a right angle.

MOS ROMs

MM4233/MM5233 4096-bit read only memory

general description

The MM4233/MM5233 4096-bit static read only memory is a monolithic MOS integrated circuit utilizing P-channel ion-implanted enhancement mode low threshold technology to achieve bipolar compatibility. The ROM is organized in a 512 word x 8-bit format.

Four programmable chip selects provide logic control of the TRI-STATE® outputs, allowing wire OR capability of up to 16 ROM's without loading common data lines or reducing systems access times. A separate output supply lead V_{DD} is provided to reduce internal power dissipation in the output stages.

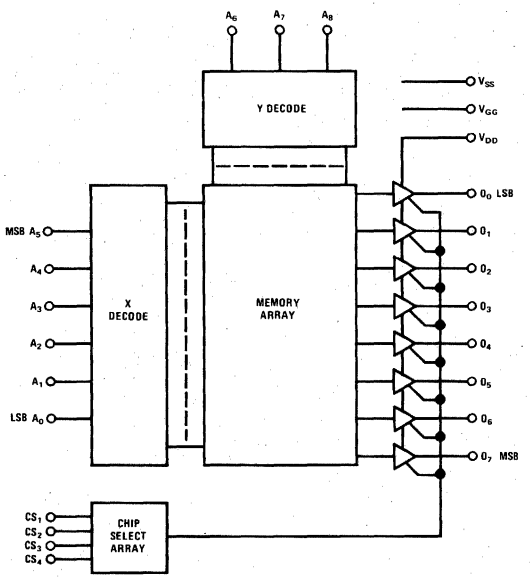
features

- Pin for pin compatible with the Fairchild 3514
- Bipolar compatible — No external components required
- Standard supplies — +5.0V, −12V
- TRI-STATE outputs — Bus ORable outputs
- Static operation — No clocks required
- Multiple ROM control — Four programmable chip select lines

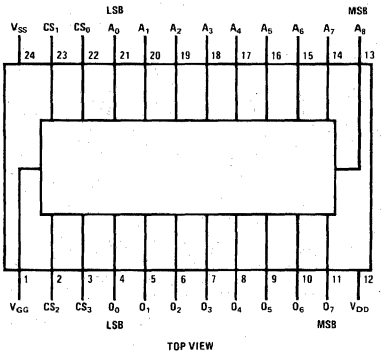
applications

- Code conversion
- Microprogramming
- Control logic
- Table look-up

logic and connection diagrams



Dual-In-Line Package



Order Number MM4233J or MM5233J
See Package 11

Order Number MM5233N
See Package 18

Note: For programming information see AN-100.

absolute maximum ratings

Voltage at Any Pin	V_{SS} + 0.5V to V_{SS} − 20 V
Power Dissipation at 25°C Ambient	0.8W
Operating Temperature	
MM4233	−55°C to +125°C
MM5233	0°C to +70°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

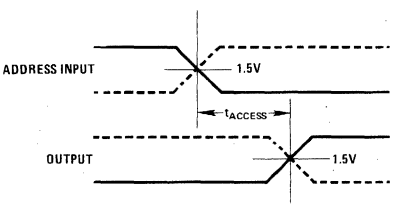
electrical characteristics

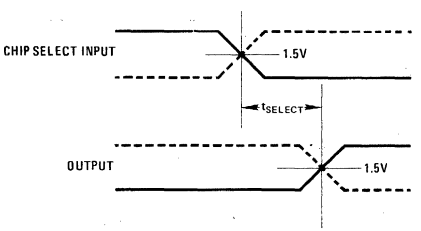
V_{SS} = +5.0V ±5%, V_{DD} = 0V, V_{GG} = −12V ±5%, T_A = −55°C to +125°C, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage Levels					
Logical Low	I_L = 2.4 mA Sink			0.4	V
Logical High	I_L = 0.5 mA Source	2.4			V
Input Voltage Levels					
Logical Low				V_{SS} − 4.0	V
Logical High		V_{SS} − 1.0			V
Power Supply Current	T_A = 25°C				
I_{SS}	(Note 1)		21	30	mA
I_{DD}				1.0	mA
I_{GG}			21	30	mA
Input Leakage	V_{IN} = V_{SS} −10V			1.0	μA
Input Capacitance (Note 2)	f = 1 MHz, V_{IN} = V_{SS}			5.0	pF
Output Capacitance (Note 2)	f = 1 MHz, V_{OUT} = V_{SS}			9.0	pF
Address Time	T_A = 25°C				
T_{ACCESS}	(Note 3 and Note 4)			1000	ns
Select Time	T_A = 25°C				
T_{SELECT}	(Note 3 and Note 4)			800	ns

Note 1: Outputs open.
Note 2: Capacitances are measured periodically only.
Note 3: See timing diagram.
Note 4: 1.5 TTL load, C_L = 20 pF.

switching time waveforms





MOS ROMs

MM4240/MM5240 2560-bit static character generator

general description

The MM4240/MM5240 2560-bit static character generator is a P-channel enhancement mode monolithic MOS integrated circuit utilizing a low threshold voltage technology. Six character address and three row address input lines provide access to 64–8 x 5 characters. Customer-generated single or multiple package character fonts are easily programmed by completing a pattern selection form. A standard 7 x 5 raster scan font is available by ordering the MM4240AA/MM5240AA.

The MM4240/MM5240 may be used as a 512 x 5-bit read only memory for applications other than character generation.

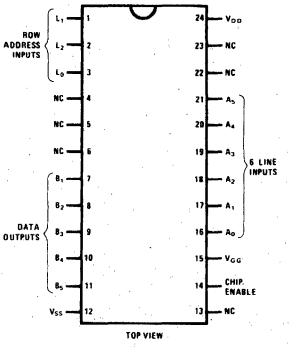
features

- Bipolar compatibility
- High speed operation—500 ns max
- ±12 volt power supplies
- Static operation—no clocks required
- Multiple ROM logic application—chip enable output control
- Standard fonts available—off-the-shelf delivery

applications

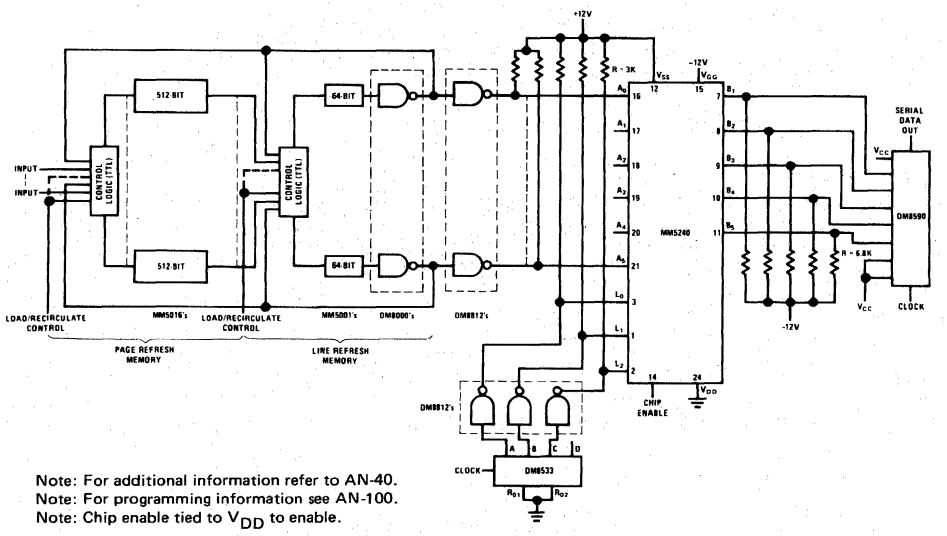
- Character generation
- Random logic synthesis
- Micro-programming
- Table look-up

connection diagram



Order Number MM4240J or MM5240J
See Package 11
Order Number MM5240N
See Package 18

typical application



Note: For additional information refer to AN-40.
Note: For programming information see AN-100.
Note: Chip enable tied to V_{DD} to enable.

absolute maximum ratings

V_{GG} Supply Voltage		V_{SS} – 30V
V_{DD} Supply Voltage		V_{SS} – 15V
Input Voltage		$(V_{SS} - 20)V < V_{IN} < (V_{SS} + 0.3)V$
Storage Temperature		–65°C to +150°C
Operating Temperature	MM4240	–55°C to +125°C
	MM5240	0°C to +70°C
Lead Temperature (Soldering, 10 sec)		300°C

electrical characteristics (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage Levels					
MOS to MOS					
Logical "1"	IMΩ to GND			V_{SS} – 9.0	V
Logical "0"		V_{SS} – 1.0			V
MOS to TTL					
Logical "1"	6.8 kΩ to V_{GG} Plus One			+0.4	V
Logical "0"	Standard Series 54/74 Gate	+2.5			V
Output Current Capability					
Logical "0"	$V_{OUT} = V_{SS} - 6.0V$	2.5			mA
Input Voltage Levels					
Logical "1"				V_{SS} – 8.0	V
Logical "0"		V_{SS} – 2.0			V
Power Supply Current	$T_A = 25°C$				
I_{DD}	MOS Load		25	40	mA
I_{GG} (Note 2)				1	μA
Input Leakage	$V_{IN} = V_{SS} - 12V$			1	μA
Input Capacitance (Note 5)	f = 1.0 MHz, $V_{IN} = 0V$		5	8	pF
V_{GG} Capacitance (Note 5)	f = 1.0 MHz, $V_{IN} = 0V$		25	40	pF
Address Time (Note 3)	See Timing Diagram				
T_{ACCESS}	$T_A = 25°C$	150	425	500	ns
Output AND Connection	MOS Load			4	
(Note 4)	TTL Load			10	

Note 1: These specifications apply for $V_{SS} = +12V$ ±5%, $V_{GG} = -12V$ ±5%, and $T_A = -55°C$ to +125°C (MM4240) $T_A = 0°C$ to +70°C (MM5240) unless otherwise specified.

Note 2: The V_{GG} supply may be clocked to reduce device power without affecting access time.

Note 3: Address time is measured from the change of data on any input or Chip Enable line to the output of a TTL gate. (See Timing Diagram). See curves for guaranteed limit over temperature.

Note 4: The address time in the TTL load configuration follows the equation:
T_{ACCESS} = The specified limit + (N – 1) (50) ns

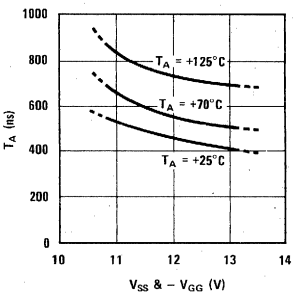
Where N = Number of AND connections.

The number of AND ties in the MOS load configuration can be increased at the expense of MOS "0" level.

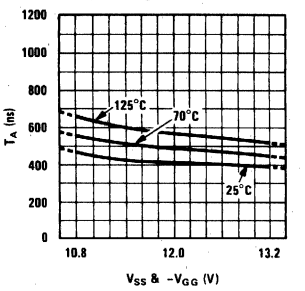
Note 5: Guaranteed by design.

performance characteristics

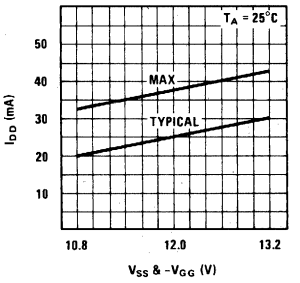
Guaranteed Access Time (T_A) vs Supply Voltage



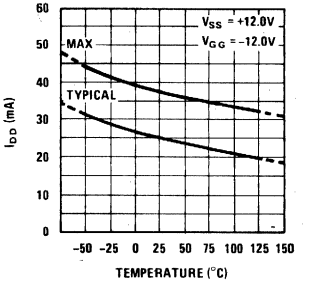
Typical Access Time (T_A) vs Supply Voltage



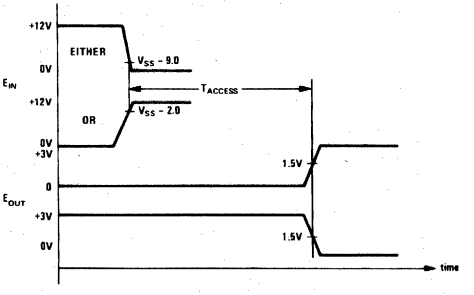
Power Supply Current vs Voltage

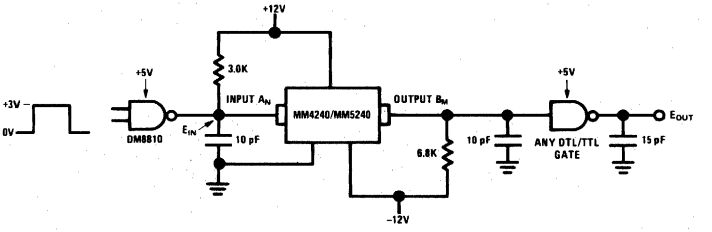


V_{DD} Power Supply Current vs Temperature

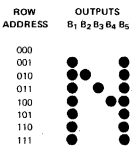


timing diagram/address time





MM4240AA/MM5240AA character font



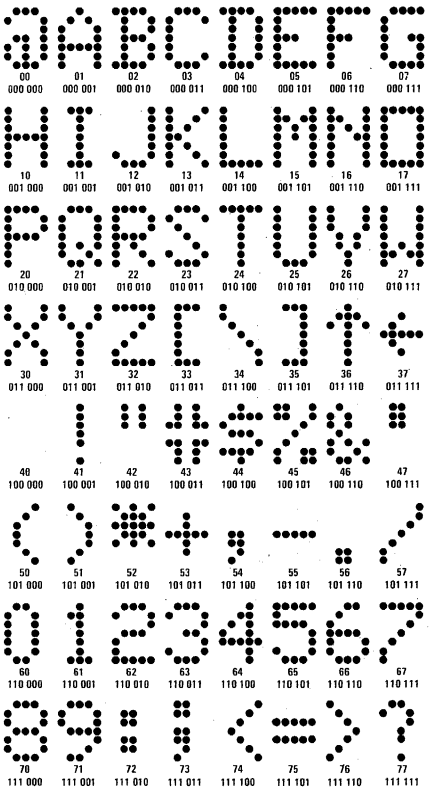


FIGURE 4

Note: Negative logic assumed.

NATIONAL

MOS ROMs

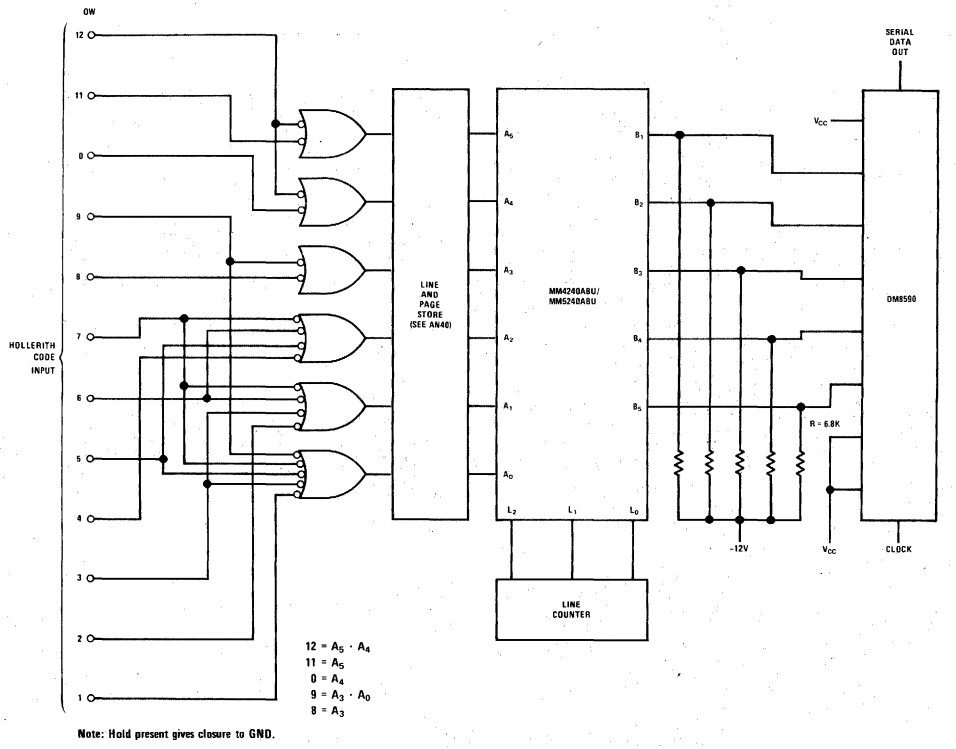
MM4240ABU/MM5240ABU hollerith character generator

general description

The MM4240ABU/MM5240ABU is a 64 x 8 x 5 read-only memory programmed to display a 64-character subset of the Hollerith 12-line code, normally used in punching 80 column cards. Compression from 12 lines to the six needed to make up a 64-character set may be accomplished as shown in the typical application.

For electrical, environmental and mechanical details, refer to the MM4240/MM5240 data sheet.

typical application



Note: Hold present gives closure to GND.

Order Number MM4240ABU/J or MM5240ABU/J
See Package 11
Order Number MM5240ABU/N
See Package 18

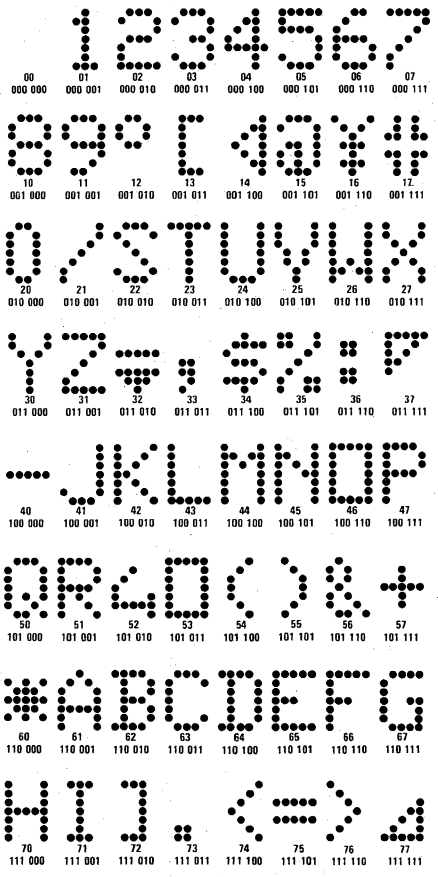
6

code table

HOLLERITH INPUT CODE (NON-COMPRESSED)	OCTAL SEQUENCE	GRAPHIC DISPLAY
	00	(space)
1	01	1
2	02	2
3	03	3
4	04	4
5	05	5
6	06	6
7	07	7
8	10	8
9	11	9
8 2	12	
8 3	13	
8 4	14	
8 5	15	
8 6	16	
8 7	17	
	20	
0	21	0
0 1	22	/
0 2	23	S
0 3	24	T
0 4	25	U
0 5	26	V
0 6	27	W
0 7	28	X
0 8	30	Y
0 9	31	Z
0 8 2	32	
0 8 3	33	
0 8 4	34	
0 8 5	35	
0 8 6	36	
0 8 7	37	
11	40	
11 1	41	J
11 2	42	K
11 3	43	L
11 4	44	M
11 5	45	N
11 6	46	O
11 7	47	P
11 8	50	Q
11 9	51	R
11 8 2	52	
11 8 3	53	
11 8 4	54	
11 8 5	55	
11 8 6	56	
11 8 7	57	
12	60	
12 1	61	A
12 2	62	B
12 3	63	C
12 4	64	D
12 5	65	E
12 6	66	F
12 7	67	G
12 8	70	H
12 9	71	I
12 8 2	72	
12 8 3	73	. (period)
12 8 4	74	
12 8 5	75	
12 8 6	76	
12 8 7	77	

character font

MM4240ABU/MM5240ABU



MOS ROMs

MM4240ABZ/MM5240ABZ EBCDIC-8 character generator

general description

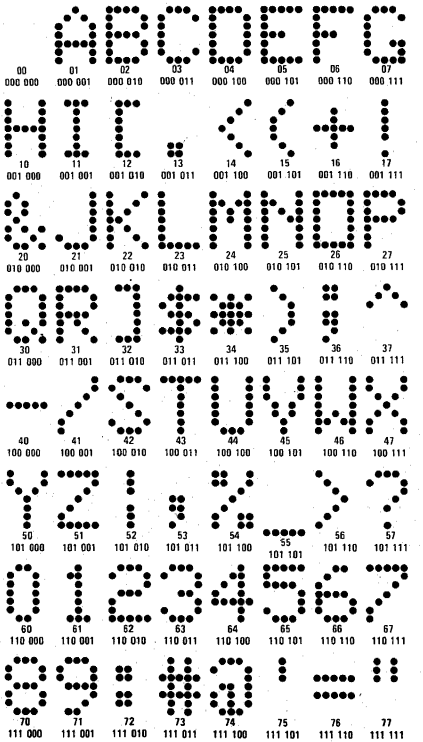
The MM4240ABZ/MM5240ABZ is a 64 x 8 x 5 read only memory that has been programmed to display the 64 character graphic subset of EBCDIC-8, an Extended Binary Coded Decimal Interchange Code with character assignments and locations conforming to the American Standard x 3.26-1970 (see MM5230QX data sheet for full EBCDIC-8 table).

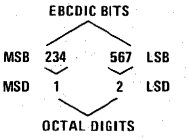
Compression of the eight bits of EBCDIC-8 to the six needed for a 64-character subset is accomplished by simply ignoring the two most significant EBCDIC bits, bit 0 and bit 1.

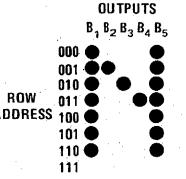
The octal character address digits are then formed as shown below.

For electrical, environmental and mechanical details, refer to the MM4240/MM5240 data sheet.

character font







Order Number MM4240ABZ/J or MM5240ABZ/J
See Package 11

Order Number MM5240ABZ/N
See Package 18

NATIONAL

MOS ROMs

MM4240ACA/MM5240ACA EBCDIC character generator

general description

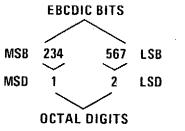
The MM4240ACA/MM5240ACA is a 64 x 8 x 5 read only memory that has been programmed to display the 64 character graphic subset of EBCDIC, an Extended Binary Coded Decimal Interchange code typically used in IBM systems.

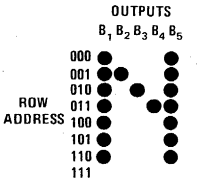
Compression of the eight bits of EBCDIC to the six needed for a 64-character subset is accomplished by simply ignoring the two most significant EBCDIC bits, bit zero and bit one.

The octal character address digits are then formed as shown below.

For electrical, environmental and mechanical details, refer to the MM4240/MM5240 data sheet.

character font





Order Number MM4240ACA/J or MM5240ACA/J
See Package 11

Order Number MM5240ACA/N
See Package 18

MOS ROMs

MM4241/MM5241 3072-bit static read-only memory

general description

The MM4241/MM5241 3072-bit static read-only memory is a P-channel enhancement mode monolithic MOS integrated circuit utilizing a low threshold-voltage technology to achieve bipolar compatibility. TRI-STATE™ outputs provide wire ORed capability without loading common data lines or reducing system access times. The ROM is organized in a 64 x 6 word by 8-bit memory organization. Programmable Chip Enables (CE_1 and CE_2) provide logic control of multiple packages without external logic. A separate output supply lead is provided to reduce internal power dissipation in the output stages.

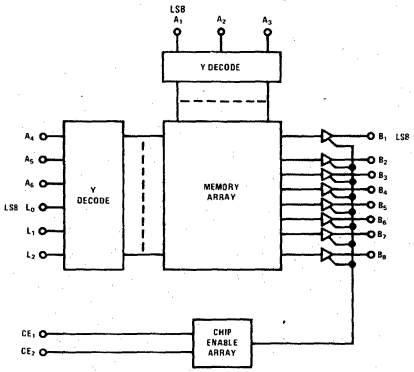
features

■ Bipolar compatibility	No external components required
■ Standard supplies	+5V, −12V
■ Bus ORable output	TRI-STATE outputs
■ Static operation	No clocks required
■ Multiple ROM control	Two programmable Chip Enable lines

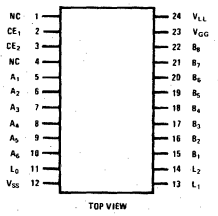
applications

- Character generator
- Random logic synthesis
- Microprogramming
- Table look-up

logic and connection diagrams



Dual-In-Line Package



Order Number MM4241J or MM5241J
See Package 11
Order Number MM5241N
See Package 18

typical applications

TTL/MOS Interface

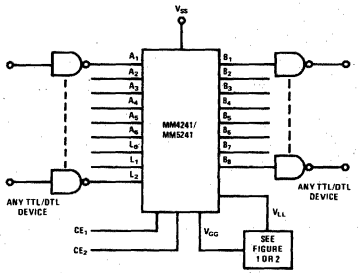


FIGURE 1. Power Saver for Small Memory Arrays

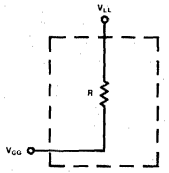
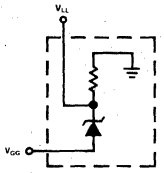


FIGURE 2. Power Saver for Large Memory Arrays



ASSUME $|V_{LL}|_{MIN} = |-3V|$
$V_{GG} - V_{LL}$ MIN = R (1.6 mA) (N) where N = 7 for 5 x 7 font.
N = 8 for 6 x 8 font.

Note: Both chip enables may be programmed to provide any of four combinations. Example: If $CE_1 = 1$ and $CE_2 = 1$ outputs (Negative Logic) would be enabled only when device pins 2 and 3 are negative (Logic "1"). The outputs will be in the third state when disabled. L_0, L_1 and L_2 (device pins 11, 13 and 14) are in positive logic (1 = most positive voltage levels = $V_S - 2V$; 0 = most negative voltage level = $V_{SS} - 4V$).

Note: For programming information see AN-100.

absolute maximum ratings

V_{GG} Supply Voltage		V_{SS} – 20V
V_{LL} Supply Voltage		V_{SS} – 20V
Input Voltage		$(V_{SS} - 20)\ V < V_{IN} < (V_{SS} + .03)V$
Storage Temperature Range		–65°C to +150°C
Operating Temperature Range	MM4241	–55°C to +125°C
	MM5241	–25°C to +70°C
Lead Temperature (Soldering, 10 sec)		300°C

electrical characteristics NEGATIVE LOGIC (Note 5)

T_A within operating temperature range, V_{SS} = +5.0V ±5%, $V_{GG} = V_{DD}$ = −12V ±5%, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage Levels					
Logical "1"	I_L = 1.6 mA sink			.4	V
Logical "0"	I_L = 100 μA source	2.4			V
Input Voltage Levels					
Logical "1"				V_{SS} – 4.0	V
Logical "0"		V_{SS} – 2.0			V
Power Supply Current					
I_{SS} (Note 4)	V_{SS} = 5, V_{GG} = −12, V_{LL} = −12, T_A = 25°C		23	37	mA
I_{SS} (Note 4)	V_{SS} = 5, V_{GG} = −12, V_{LL} = −3, T_A = 125°C			20	mA
Input Leakage	$V_{IN} = V_{SS}$ – 10V			1	μA
Input Capacitance (Note 1)	f = 1.0 MHz, V_{IN} = 0V		5	15	pF
Output Capacitance (Note 1)	f = 1.0 MHz, V_{IN} = 0V		4	10	pF
Address Time (Note 2) T_{ACCESS}	T_A = 25°C, V_{SS} = 5 $V_{GG} = V_{LL}$ = −12V	150	700	900	ns
Output AND Connections (Note 3)				20	

Note 1: Address time is measured from the change of data on any input or Chip Enable line to the output of a TTL gate. (See Timing Diagram.) See curves for guaranteed limit over temperature.

Note 2: Capacitances are measured periodically only.

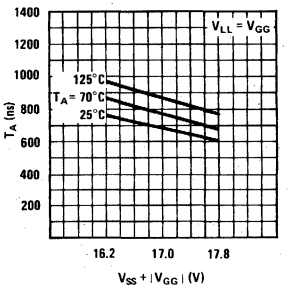
Note 3: The address time follows the following equation: T_{ACCESS} = the specified limit + (N − 1) x 25 ns where N = Number of AND connections.

Note 4: Outputs open.

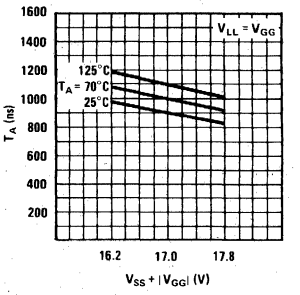
Note 5: All addresses and outputs are in negative true logic with the exception of L_0, L_1, and L_2 which are in positive logic.

performance characteristics

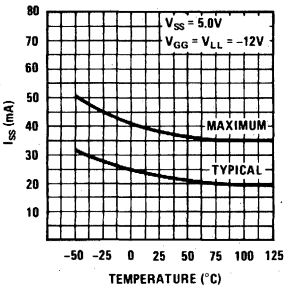
Typical Access Time vs Supply Voltage



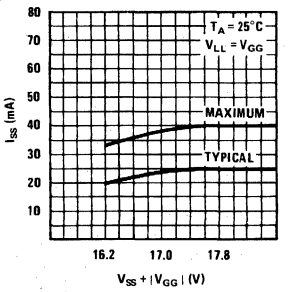
Guaranteed Access Time vs Supply Voltage



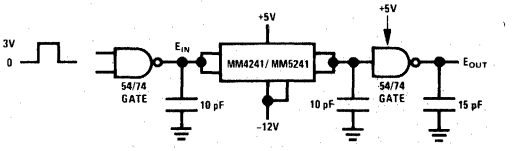
Power Supply Current vs Temperature

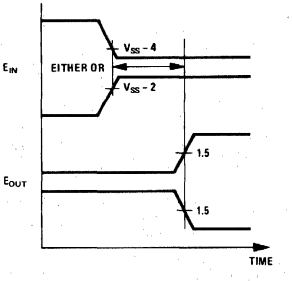


Power Supply Current vs Voltage



timing diagram/address time





NATIONAL

MOS ROMs
Advance Information

MM4242/MM5242 8192-bit read only memory

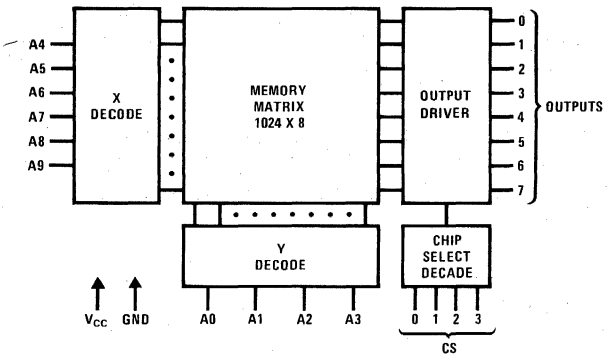
general description

The MM4242/MM5242 1024 x 8-bit read only memory is a monolithic MOS integrated circuit utilizing N-channel silicon-gate enhancement mode and ion-implanted depletion mode devices. Use of this technology allows operation from a single power supply and compatibility with TTL and DTL circuits. Programming of the memory contents and chip selects is accomplished by changing one mask during the device fabrication.

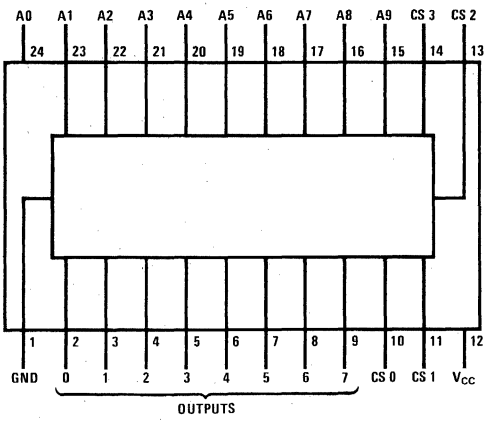
features

- Organized as 1024 bytes of 8 bits
- Static operation
- Four programmable chip select inputs
- Maximum access time—500 ns
- TTL compatible
- TRI-STATE outputs
- Single 5V power supply

block and connection diagrams



Dual-In-Line Package



TOP VIEW

Order Number MM4242D or MM5242D
See Package 6
Order Number MM5242N
See Package 18

NATIONAL

MOS ROMs
Advance Information

MM4246/MM5246 16,384-bit read only memory

general description

The MM4246/MM5246 is a static 16,384-bit read only memory organized in a 2048 word by 8-bit format. It is fabricated using N-channel enhancement and depletion mode silicon gate technology which provides complete DTL/TTL compatibility and single power supply operation.

Three chip select inputs controlling the TRI-STATE® outputs permit easy memory expansion. Programming of the memory and chip select active levels is accomplished by changing one mask during fabrication.

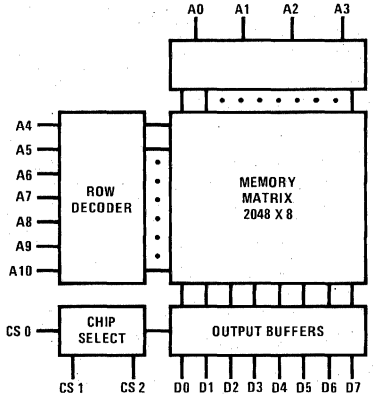
features

- Single 5.0V supply
- All inputs and outputs directly DTL/TTL compatible
- Static operation
- TRI-STATE outputs for bus interface
- Programmable chip selects
- 2048 word by 8-bit organization
- Maximum access time—500 ns

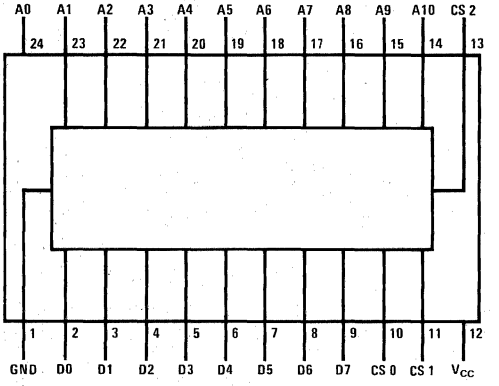
applications

- Microprogramming
- Control logic
- Table lookup

block and connection diagrams



Dual-In-Line Package



TOP VIEW

Order Number MM4246D or MM5246D
See Package 6
Order Number MM5246N
See Package 18

NATIONAL

MOS ROMs

SK0003 sine/cosine look-up table kit

general description

The SK0003 Sine/Cosine Look-Up Table Kit consists of four MOS ROMs: three MM4210/MM5210's and one MM4220/MM5220-1024 bit static read only memories. They are P-channel enhancement mode monolithic MOS integrated circuits utilizing a low threshold technology.

THE SINE FUNCTION

The SK0003 implements the equation $\sin\theta = \sin M \cos L + \cos M \sin L$. Cos L was assumed to be 1 in the equation. However, it is a variable between 1 and 0.99998 and is a function of round off error. Worst case error is 1-5/8 bits in LSB at address 1415 (62.25°). The error increases from zero to .002% every 8 bits, therefore, the MM4220/MM5220 provides the error correction factor $\cos(M - 2.81°)\sin L$ in the equation $\sin\theta = \sin M + \cos(M - 2.81°)\sin L$. The circuitry to perform this function is shown in Figure 1. Additional information is available in *MOS Brief 10*.

THE COSINE FUNCTION

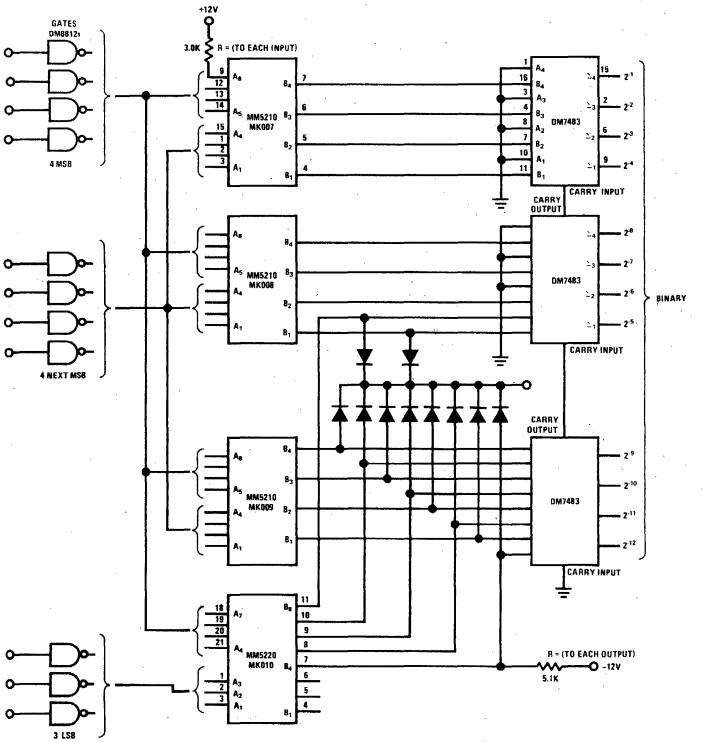
To generate the cosine function $\cos\theta = \sin(\theta - 90°)$, the input must be complemented and a logical "1" added. Figure 2A is a logic diagram of the circuitry used to provide the cosine function, as well as providing both sine and cosine functions in the same system. 11-bit resolution and 12-bit accuracy ±1-5/8-bits is achieved in this configuration.

A reduction in logic can be achieved as shown in Figure 2B if a loss in resolution of 1/2-bit in an 11-bit input or 1/4-bit in a 10-bit input is acceptable.

ELECTRICAL CHARACTERISTICS

Refer to the appropriate data sheet for each device shown in the figures. The devices noted are: MM4210/MM5210, MM4220/MM5220, DM5483/DM7483, DM7812/DM8812 and DM5486/DM7486.

logic diagram



Order Number SK0003C
or
Order Number SK0003M

FIGURE 1. SK0003 Logic Diagram (Kit Includes ROMs Only). This Circuit Provides 11-Bit Resolution and 12-Bit Accuracy in a θ to Sin θ Converter.

logic diagram

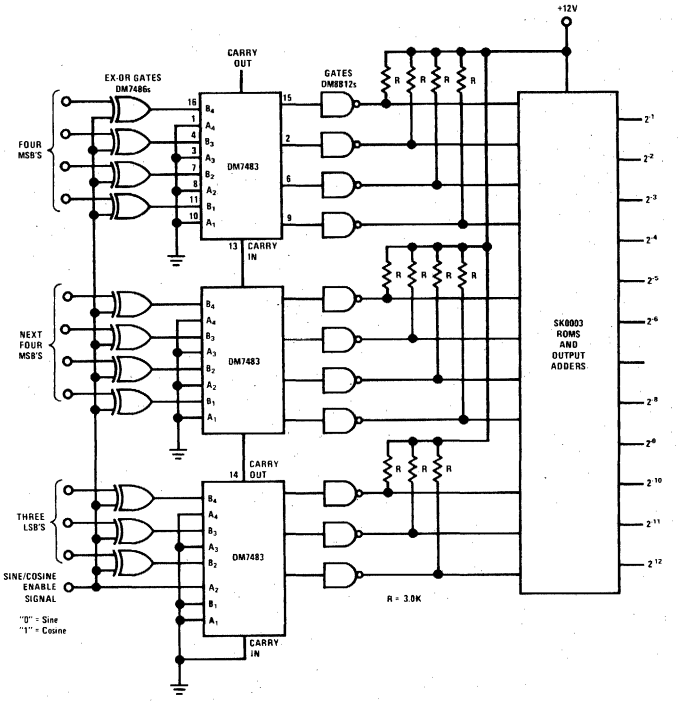


FIGURE 2A. Sine/Cosine Conversion Provides 11-Bit Resolution, 12-Bit ±1-5/8 Bit Accuracy.

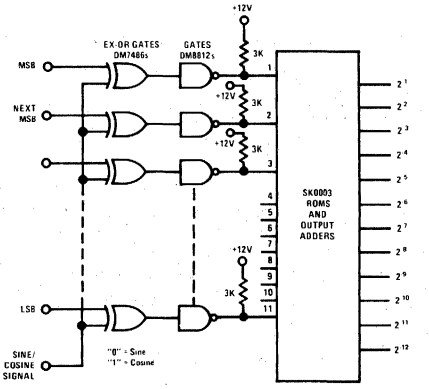


FIGURE 2B. Sine/Cosine Conversion with Cosine Approximated. (Cosine Conversion has 10-Bits Input Resolution and 12-Bit ±1-5/8-Bit Accuracy.)

NATIONAL

DM5488/DM7488 256-bit read only memories

general description

These custom-programmed, 256-bit, read only memories are organized as 32 words of 8 bits each. Each monolithic, high-speed, transistor-transistor logic (TTL), 32-word memory array is addressed in straight 5-bit binary with full on-chip decoding. An overriding memory-enable input is provided which, when taken high, will inhibit the 32 address gates and cause all 8 outputs to remain high (off). Data, as specified by the customer, are permanently programmed into the monolithic structure for the 256-bit locations. This organization is expandable to n-words to N-bit length.

The address of an 8-bit word is accomplished through the buffered, binary select inputs which are decoded by the 32 five-input address gates. When the memory-enable input is high, all 32 gate outputs are low, turning off the 8 output buffers.

Data are programmed into the memory at the emitters of 32 eight-emitter transistors. The programming process involves connecting or not connecting each of the 256 emitters. If an emitter is connected, a low-level voltage is read out of that bit location when its decoding gate is addressed. If the emitter is not connected, a high-level voltage is read when addressed. Those decoding-gate output emitters which are used are connected to their respective bit lines to drive the 8 output buffers. Since only one decoding gate is addressed at a time, only one of the 32 transistors can supply current to the output buffers at a time.

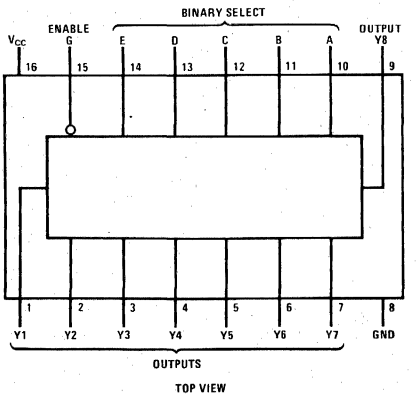
This memory is fully compatible for use with most TTL or DTL circuits. Input clamping diodes are provided to minimize transmission-line effects and simplify system design. Input buffers lower the fan-in requirement to only one normalized Series 54/74 load for all inputs including enable (G). The open-collector outputs are capable of sinking 12 mA of current and may be wire-AND connected to increase the number of words available. An external pull-up resistor from each output to the supply line (V_{CC}) is required to define the high-level output voltage. Where multiple DM5488/DM7488 devices are used in a memory system, the enable input allows easy decoding of additional address bits. Access propagation delay time is typically 20 ns and power dissipation is typically 240 mW.

features

- Applications in computer subroutines
- Useful in display systems and readouts
- Memory organized as 32 words of 8-bits each
- Input clamping diodes simplify system design
- Open-collector outputs permit wire-AND capability
- Typical access time: 20 ns
- Typical power dissipation: 240 mW
- Fully compatible with most TTL and DTL circuits

connection diagram

Dual-In-Line Package



TOP VIEW

Order Number DM5488J or DM7488J
See Package 10

Order Number DM7488N
See Package 15

absolute maximum ratings (Note 1)

Supply Voltage, V_{CC} (Note 3)	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DM5488	4.5	5.5	V
DM7488	4.75	5.25	V
Temperature (T_A)			
DM5488	−55	+125	°C
DM7488	0	+70	°C

electrical characteristics (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
High Level Input Voltage (V_{IH})		2			V
Low Level Input Voltage (V_{IL})				0.8	V
Input Clamp Voltage (V_I)	V_{CC} = Min, I_I = −12 mA			−1.5	V
High Level Output Current (I_{OH})	V_{CC} = Min, V_{IH} = 2V, V_{IL} = 0.8V, V_{OH} = 5.5V			40	μA
Low Level Output Current (I_{OL})				12	mA
Low Level Output Voltage (V_{OL}) (Note 2)	V_{CC} = Min, V_{IH} = 2V, V_{IL} = 0.8V, I_{OL} = 12 mA		0.2	0.4	V
Input Current at Maximum Input Voltage (I_I)	V_{CC} = Max, V_I = 5.5V			1	mA
High Level Input Current (I_{IH})	V_{CC} = Max, V_I = 2.4V			25	μA
Low Level Input Current (I_{IL})	V_{CC} = Max, V_I = 0.4V			−1	mA
Supply Current, all Outputs High (I_{CCH}) (Note 2)	V_{CC} = Max		37	65	mA
Supply Current, all Outputs Low (I_{CCL}) (Notes 2 and 4)	V_{CC} = Max		48	80	mA

switching characteristics V_{CC} = 5V, T_A = 25°C

PARAMETER	FROM INPUT	TO OUTPUT	CONDITIONS	MIN	TYP	MAX	UNITS
Propagation Delay Time, Low to High Level Output (t_{PLH})	Enable	Any	C_L = 30 pF, R_{L1} = 400Ω, R_{L2} = 600Ω		19	35	ns
Propagation Delay Time, High to Low Level Output (t_{PHL})	Enable	Any			18	35	ns
Propagation Delay Time, Low to High Level Output (t_{PLH})	Select	Any			21	35	ns
Propagation Delay Time, High to Low Level Output (t_{PHL})	Select	Any			17	35	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for DM5488 and across the 0°C to +70°C range for the DM7488. All typicals are given for V_{CC} = 5V and T_A = +25°C.

Note 3: All voltage values are with respect to network ground terminal.

Note 4: All 32 words are addressed separately to ensure that the supply current does not exceed the stated maximum. The typical value shown is for the worst-case condition of all eight outputs driven low at one time.

ordering instructions

Programming instructions for the DM5488 or DM7488 are solicited in the form of a sequenced deck of 32 standard 80-column data cards providing the information requested under "data card format," accompanied by a properly sequenced listing of these cards, and the supplementary ordering data. Upon receipt of these items, a computer run will be made from the deck of cards which will produce a complete function table of the requested part. This function table, showing output conditions for each of the 32 words, will be forwarded to the purchaser as verification of the input data as interpreted by the computer-automated design (CAD) program. This single run also generates mask and test program data; therefore, verification of the function table should be completed promptly.

Each card in the data deck prepared by the purchaser identifies the word specified and describes the levels at the eight outputs for that word. All addresses must have all outputs defined and columns designated as "blank" must not be punched. Cards should be punched according to the data card format shown.

SUPPLEMENTARY ORDERING DATA

Submit the following information with the data cards:

a. Customer's name and address
b. Customer's purchase order number
c. Customer's drawing number

DATA CARD FORMAT

Column

1–2 Punch a right-justified integer representing the positive-logic binary input address (00–31) for the word described on the card.

3–4 Blank

5 Punch "H," "L," or "X" for output Y8. H = high-voltage-level output, L = low-voltage-level output, X = output irrelevant.

6–9 Blank

10 Punch "H," "L," or "X" for output Y7.

11–14 Blank

15 Punch "H," "L," or "X" for output Y6.

16–19 Blank

20 Punch "H," "L," or "X" for output Y5.

21–24 Blank

25 Punch "H," "L," or "X" for output Y4.

26–29 Blank

30 Punch "H," "L," or "X" for ouput Y3.

31–34 Blank

35 Punch "H," "L," or "X" for output Y2.

36–39 Blank

40 Punch "H," "L," or "X" for output Y1.

41–49 Blank

50–51 Punch a right-justified integer representing the current calendar day of the month.

52 Blank

53–55 Punch an alphabetic abbreviation representing the current month.

56 Blank

57–58 Punch the last two digits of the current year

59 Blank

60–61 Punch "DM"

62–65 Punch the National Semiconductor part number 5488 or 7488.

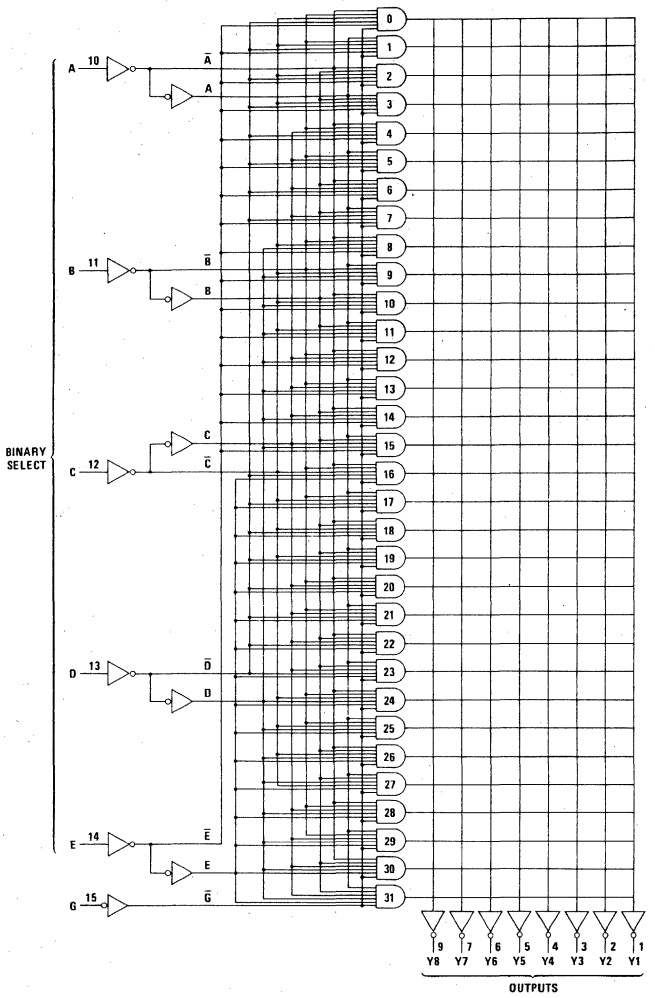
66–70 Blank

truth table

WORD	INPUTS				
	E	D	C	B	A
0	L	L	L	L	L
1	L	L	L	L	H
2	L	L	L	H	L
3	L	L	L	H	H
4	L	L	H	L	L
5	L	L	H	L	H
6	L	L	H	H	L
7	L	L	H	H	H
8	L	H	L	L	L
9	L	H	L	L	H
10	L	H	L	H	L
11	L	H	L	H	H
12	L	H	H	L	L
13	L	H	H	L	H
14	L	H	H	H	L
15	L	H	H	H	H
16	H	L	L	L	L
17	H	L	L	L	H
18	H	L	L	H	L
19	H	L	L	H	H
20	H	L	H	L	L
21	H	L	H	L	H
22	H	L	H	H	L
23	H	L	H	H	H
24	H	H	L	L	L
25	H	H	L	L	H
26	H	H	L	H	L
27	H	H	L	H	H
28	H	H	H	L	L
29	H	H	H	L	H
30	H	H	H	H	L
31	H	H	H	H	H

H = High level
L = Low level

functional block diagram



NATIONAL

Bipolar ROMs

DM54187/DM74187(SN54187/SN74187)
1024-bit read only memory

general description

The DM54187/DM74187 is a custom-programmed read-only memory organized as 256 four-bit words. Selection of the proper word is accomplished through the eight select inputs. Two overriding memory enable inputs are provided; and when one is taken to the logical "1" state, it will cause all four outputs to go to the logical "1" state.

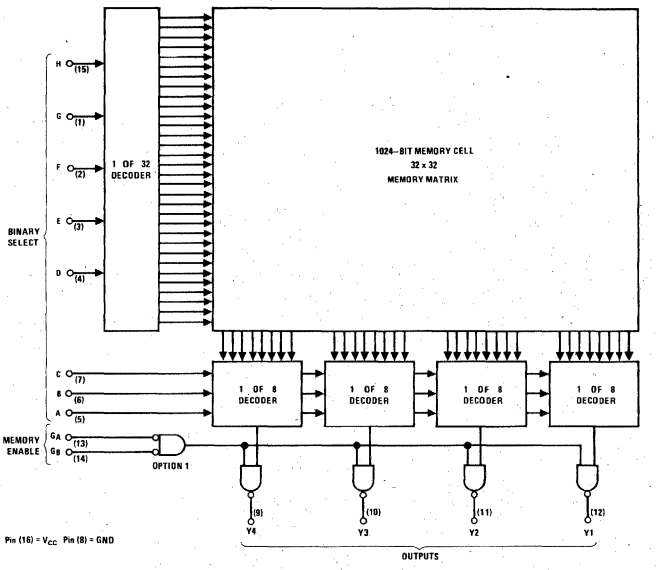
features

- 36 ns typical delay from address to output
- 20 ns typical delay from enable to output
- Open collector outputs for expansion

applications

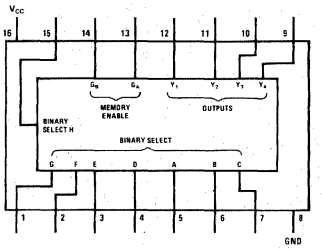
- Microprogramming
- Code conversions
- Look-up tables
- Use for any memory where content is fixed

logic diagram



connection diagram

Dual-In-Line Package



Order Number DM54187J
or DM74187J
See Package 10

Order Number DM74187N
See Package 15

7

absolute maximum ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Output Voltage	5.5V
Operating Temperature Range	
DM54187	−55°C to +125°C
DM74187	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics (Note 2)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	DM54187	V_{CC} = 4.5V		2.0			V
	DM74187	V_{CC} = 4.75V					
Logical "0" Input Voltage	DM54187	V_{CC} = 4.5V				0.8	V
	DM74187	V_{CC} = 4.75V					
Logical "1" Output Current	DM54187	V_{CC} = 5.5V	V_O = 5.5V			40	μA
	DM74187	V_{CC} = 5.25V					
Logical "0" Output Voltage	DM54187	V_{CC} = 4.5V	I_O = 16 mA			0.4	V
	DM74187	V_{CC} = 4.75V					
Logical "1" Input Current	DM54187	V_{CC} = 5.5V	V_{IN} = 2.4V			40	μA
	DM74187	V_{CC} = 5.25V					
Logical "0" Input Current	DM54187	V_{CC} = 5.5V	V_{IN} = 5.5V			1	mA
	DM74187	V_{CC} = 5.25V					
	DM54187	V_{CC} = 5.5V	V_{IN} = 0.4V			−1.0	mA
	DM74187	V_{CC} = 5.25V					
Supply Current	DM54187	V_{CC} = 5.5V	All Inputs at GND.		75	110	mA
	DM74187	V_{CC} = 5.25V					
Input Clamp Voltage	DM54187	V_{CC} = 4.5V	I_{IN} = −12 mA			−1.5	V
	DM74187	V_{CC} = 4.75V					
Propagation Delay to a Logical "0" from Enable to Output, t_{pd0}		V_{CC} = 5.0V, T_A = 25°C	C_L = 30 pF		20	30	ns
Propagation Delay to a Logical "0" from Address to Output, t_{pd0}		V_{CC} = 5.0V, T_A = 25°C	C_L = 30 pF		37	60	ns
Propagation Delay to a Logical "1" from Enable to Output, t_{pd1}		V_{CC} = 5.0V, T_A = 25°C	C_L = 30 pF		20	30	ns
Propagation Delay to a Logical "1" from Address to Output, t_{pd1}		V_{CC} = 5.0V, T_A = 25°C	C_L = 30 pF		36	60	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DM54187 and across the 0°C to 70°C range for the DM74187. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

ordering instructions

Programming instructions for the DM54187 or DM74187 are solicited in the form of a sequenced deck of 32 standard 80-column data cards providing the information requested under data card format, accompanied by a properly sequenced listing of these cards, and the supplementary ordering data. Upon receipt of these items, a computer run will be made from the deck of cards which will produce a complete truth table of the requested part. This truth table, showing output conditions for each of the 256 words, will be forwarded to the purchaser as verification of the input data as interpreted by the computer-automated design (CAD) program. This single run also generates mask and test program data; therefore, verification of the truth table should be completed promptly.

Each card in the data deck prepared by the purchaser identifies the eight words specified and describes the conditions at the four outputs for each of the eight words. All addresses must have all outputs defined and columns designated as "blank" must not be punched. Cards should be punched according to the data card format shown.

supplementary ordering data

Submit the following information with the data cards:

a) Customer's name and address
b) Customer's purchase order number
c) Customer's drawing number.

data card format

Column

1- 3	Punch a right-justified integer representing the binary input address (000-248) for the first set of outputs described on the card.
4	Punch a "–" (Minus sign)
5- 7	Punch a right-justified integer representing the binary input address (007-255) for the last set of outputs described on the card.
8- 9	Blank
10-13	Punch "H", "L", or "X" for bits four, three, two, and one (outputs Y4, Y3, Y2, and Y1 in that order) for the first set of outputs specified on the card. H = high-level output, L = low-level output, X = output irrelevant.
14	Blank
15-18	Punch "H", "L", or "X" for the second set of outputs.
19	Blank
20-23	Punch "H", "L", or "X" for the third set of outputs.
24	Blank
25-28	Punch "H", "L", or "X" for the fourth set of outputs.
29	Blank
30-33	Punch "H", "L", or "X" for the fifth set of outputs.
34	Blank
35-38	Punch "H", "L", or "X" for the sixth set of outputs.
39	Blank
40-43	Punch "H", "L", or "X" for the seventh set of outputs.
44	Blank
45-48	Punch "H", "L", or "X" for the eighth set of outputs.
49	Blank
50-51	Punch a right-justified integer representing the current calendar day of the month.
52	Blank
53-55	Punch an alphabetic abbreviation representing the current month.
56	Blank
57-58	Punch the last two digits of the current year.
59	Blank
60-61	Punch "DM"
62-66	Punch the National Semiconductor part number 54187 or 74187.
67-70	Blank

NATIONAL

Bipolar ROMs

DM54L187A/DM74L187A(SN54L187A/SN74L187A)
low power 1024-bit read only memory

general description

The DM54L187A/DM74L187A is a custom-programmed Read Only Memory organized as 256 4-bit words. Selection of the proper word is accomplished through the eight select inputs.

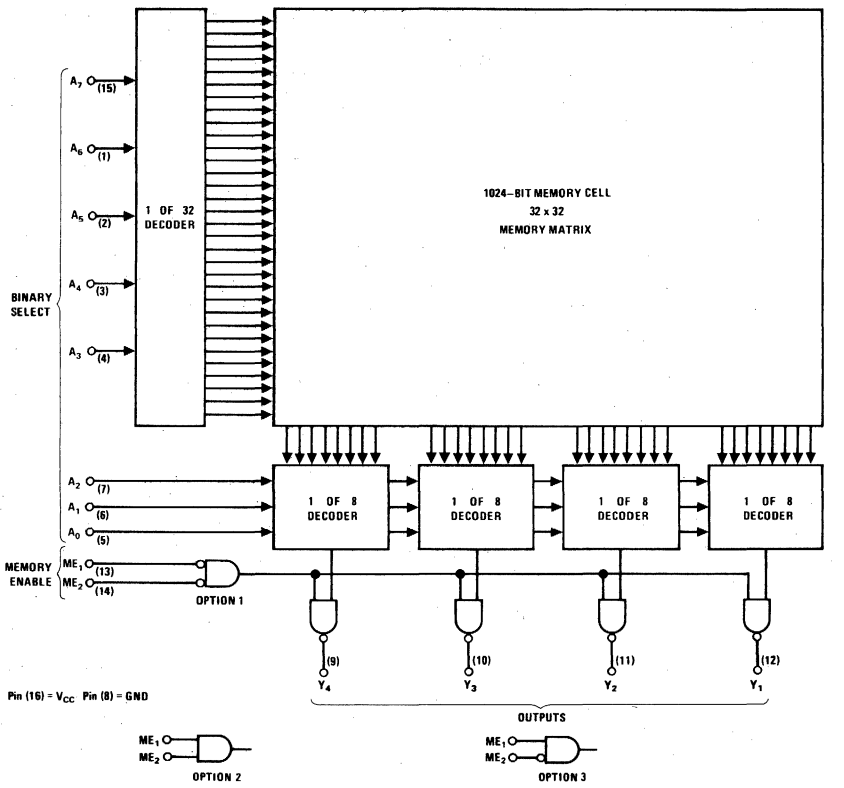
The "A" suffix is used to denote that full "tenth-power" technology has been employed in building this ROM.

Two overriding memory enable inputs are provided which when mask-programmed in one of the three options described will cause all four outputs to read either the normal memory contents or go to the logical "1" state.

features

- Full tenth-power technology
- Pin compatible with SN54187/SN74187
- Typical power dissipation 90 mW
- Typical access time 85 ns
- Custom-programmed memory enable inputs
- Open-collector outputs

logic diagram



absolute maximum ratings (Note 1)

Supply Voltage	7.0V
Input Voltage	5.5V
Output Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DM54L187	4.5	5.5	V
DM74L187	4.75	5.25	V
Temperature (T_A)			
DM54L187	−55	+125	°C
DM74L187	0	+70	°C

electrical characteristics (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	V_{CC} = Min	2.0			V
Logical "0" Input Voltage	V_{CC} = Min			0.7	V
Logical "1" Output Current	V_{CC} = Max, V_O = 5.5V (Memory Enable = Logical 1)			50	μA
Logical "0" Output Voltage					
DM54L187	V_{CC} = Min, I_O = 2.0 mA			0.3	V
DM74L187	V_{CC} = Min, I_O = 3.2 mA			0.4	V
Logical "1" Input Current	V_{CC} = Max, V_{IN} = 2.4V			10	μA
	V_{CC} = Max, V_{IN} = 5.5V			100	μA
Logical "0" Input Current	V_{CC} = Max, V_{IN} = 0.3V		−120	−180	μA
Supply Current (Each Device)	V_{CC} = Max, All Inputs at GND		18	25	mA
Input Clamp Voltage	V_{CC} = Min, I_{IN} = −12 mA			−1.5	V
Propagation Delay to a Logical "0" From Enable to Output (t_{pd0})	V_{CC} = 5.0V, C_L = 15 pF, T_A = 25°C, R_L = 2.0 kΩ		46	70	ns
Propagation Delay to a Logical "0" From Address to Output (t_{pd0})	V_{CC} = 5.0V, C_L = 15 pF, T_A = 25°C, R_L = 2.0 kΩ		65	98	ns
Propagation Delay to a Logical "1" From Enable to Output (t_{pd1})	V_{CC} = 5.0V, C_L = 15 pF, T_A = 25°C, R_L = 2.0 kΩ		85	130	ns
Propagation Delay to a Logical "1" From Address to Output (t_{pd1})	V_{CC} = 5.0V, C_L = 15 pF, T_A = 25°C, R_L = 2.0 kΩ		120	180	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DM54L187 and across the 0°C to +70°C range for the DM74L187. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

ordering instructions

Programming instructions for the DM54L187 or DM74L187 are solicited in the form of a sequenced deck of 32 standard 80-column data cards providing the information requested under data card format, accompanied by a properly sequenced listing of these cards, and the supplementary ordering data. Upon receipt of these items, a computer run will be made from the deck of cards which will produce a complete truth table of the requested part. This truth table, showing output conditions for each of the 256 words, will be forwarded to the purchaser as verification of the input data as interpreted by the computer-automated design (CAD) program. This single run also generates mask and test program data; therefore, verification of the truth table should be completed promptly.

Each card in the data deck prepared by the purchaser identifies the eight words specified and describes the conditions at the four outputs for each of the eight words. All addresses must have all outputs defined and columns designated as "blank" must not be punched. Cards should be punched according to the data card format shown.

supplementary ordering data

Submit the following information with the data cards:

a) Customer's name and address
b) Customer's purchase order number
c) Customer's drawing number.

data card format

Column

1- 3 Punch a right-justified integer representing the binary input address (000-248) for the first set of outputs described on the card.

4 Punch a "–" (Minus sign)

5- 7 Punch a right-justified integer representing the binary input address (007-255) for the last set of outputs described on the card.

8- 9 Blank

10-13 Punch "H", "L", or "X" for bits four, three, two, and one (outputs Y4, Y3, Y2, and Y1 in that order) for the first set of outputs specified on the card. H = high-level output, L = low-level output, X = output irrelevant.

14 Blank

15-18 Punch "H", "L", or "X" for the second set of outputs.

19 Blank

20-23 Punch "H", "L", or "X" for the third set of outputs.

24 Blank

25-28 Punch "H", "L", or "X" for the fourth set of outputs.

29 Blank

30-33 Punch "H", "L", or "X" for the fifth set of outputs.

34 Blank

35-38 Punch "H", "L", or "X" for the sixth set of outputs.

39 Blank

40-43 Punch "H", "L", or "X" for the seventh set of outputs.

44 Blank

45-48 Punch "H", "L", or "X" for the eighth set of outputs.

49 Blank

50-51 Punch a right-justified integer representing the current calendar day of the month.

52 Blank

53-55 Punch an alphabetic abbreviation representing the current month.

56 Blank

57-58 Punch the last two digits of the current year.

59 Blank

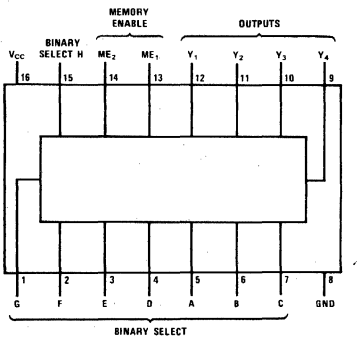
60-61 Punch "DM"

62-67 Punch the National Semiconductor part number 54L187 or 74L187

68-70 Blank

connection diagram

Dual-In-Line and Flat Package



TOP VIEW

Order Number DM54L187AJ
or DM74L187AJ
See Package 10

Order Number DM54L187AN
or DM74L187AN
See Package 15

Order Number DM54L187AW
or DM74L187AW
See Package 28

truth table

OPTION	ME_1	ME_2	OUTPUTS
1	0	0	Normal
	1	X	Logical 1
	X	1	Logical 1
2	1	1	Normal
	0	X	Logical 1
	X	0	Logical 1
3	1	0	Normal
	X	1	Logical 1
	0	X	Logical 1

X = Don't care

DM54S187/DM74S187 open-collector 1024-bit ROM
DM75S97/DM85S97 TRI-STATE® 1024-bit ROM

general description

These TTL compatible memories are organized in the popular 256 words by 4 bits configuration. Two memory enable inputs are provided to control the output states. When both enable inputs are in the logical "0" state, the outputs present the contents of the word selected by the address inputs.

If either or both of the enable inputs is raised to a logical "1" level, it causes all four outputs to go to the "OFF" or high impedance state. The memories are available in both open-collector and TRI-STATE versions and are available as PROMs as well as ROMs.

features

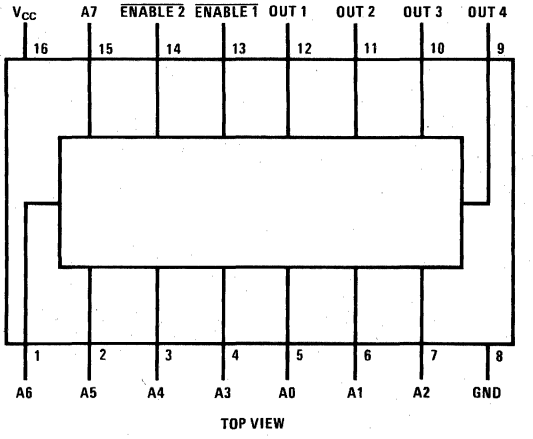
- Schottky clamped for high speed systems
- High speed

Enable to output delay—typical	15 ns
Address to output delay—typical	30 ns

- PNP inputs reduce input loading

connection diagram

Dual-In-Line Package



TOP VIEW

Order Number DM54S187J or DM74S187J, DM75S97J or DM85S97J
See Package 10
Order Number DM74S187N or DM85S97N
See Package 15

absolute maximum ratings (Note 1)

Supply Voltage (Note 2)	−0.5V to +7.0V
Input Voltage (Note 2)	−1.2V to +5.5V
Output Voltage (Note 2)	−0.5V to +5.5V
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DM54S187, DM75S97	4.5	5.5	V
DM74S187, DM85S97	4.75	5.25	V
Ambient Temperature (T_A)			
DM54S187, DM75S97	−55	+125	°C
DM74S187, DM85S97	0	+70	°C
Logical "0" Input Voltage	0	0.8	V
Logical "1" Input Voltage	2.0	5.5	V

dc electrical characteristics (Note 2)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
I_{IH}	Logical "1" Input Current	V_{IN} = 2.7V			25	μA
		V_{IN} = 5.5V			1.0	mA
I_{IL}	Logical "0" Input Current	V_{IN} = 0.45V			−250	μA
V_{CL}	Input Clamp Voltage	I_{IN} = −18 mA			−1.2	V
V_{OL}	Logical "0" Output Voltage					
	DM54S187, DM75S97	I_{OL} = 16 mA			0.50	V
	DM74S187, DM85S97				0.45	V
I_{CC}	Maximum Supply Current			80	130	mA
DM54S187, DM74S187						
I_{OH}	Logical "1" Output Current	V_{OUT} = 2.4V			50	μA
		V_{OUT} = 5.5V			100	μA
DM75S97, DM85S97						
V_{OH}	Logical "1" Output Voltage					
	DM75S97	I_{OH} = −2.0 mA	2.4			V
	DM85S97	I_{OH} = −6.5 mA	2.4			V
I_{OS}	Output Short Circuit Current	V_{OUT} = 0V (Note 3) V_{CC} = Max	−30		−100	mA
I_{OZ}	TRI-STATE Output Current	$0.45V \leq V_{OUT} \leq 2.4V$	−50		50	μA

switching characteristics (Note 2)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{AA}	Address to Output Delay			30		ns
t_{EA}	Time to Enable Output	R_L = 300Ω C_L = 30 pF		15		ns
t_{ED}	Time to Disable Output			15		ns

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at these values.

Note 2: These limits apply over the entire operating range unless stated otherwise. All typical values are for V_{CC} = 5.0V and T_A = 25°C.

Note 3: During I_{OS} measurement, only one output at a time should be grounded. Permanent damage may otherwise result.

Bipolar ROMs
Advance Information

DM54S270/DM74S270 open-collector 2048-bit ROM
DM54S370/DM74S370 TRI-STATE® 2048-bit ROM

general description

These TTL compatible memories are organized as 512 words by 4 bits. These devices effectively double the capacity of the popular 1k ROMs on the market by utilizing one chip-enable input as an additional address. When the circuit is enabled, the 4 outputs present the contents of the word selected by the address inputs.

An overriding enable input is provided which, if in the logical "1" state, causes all outputs to go to the "OFF" state, or high impedance state. Available in both open-collector or TRI-STATE, both versions are also available as Programmable Read Only Memories.

features

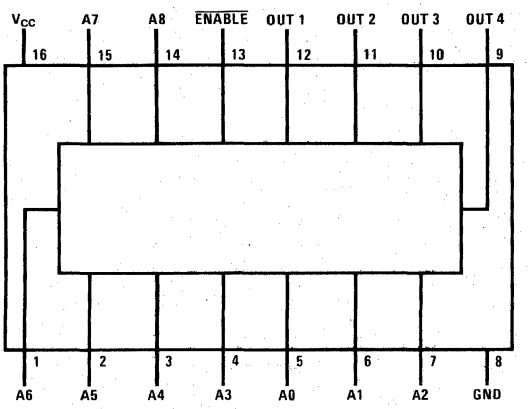
- Schottky clamped for high speed systems
- High speed

Address to output delay—typical	35 ns
Enable to output delay—typical	15 ns

- PNP inputs reduce input loading

connection diagram

Dual-In-Line Package



TOP VIEW

Order Number DM54S270J, DM54S370J, DM74S270J or DM74S370J
See Package 10

Order Number DM74S270N or DM74S370N
See Package 15

absolute maximum ratings (Note 1)

Supply Voltage (Note 2)	−0.5V to +7.0V
Input Voltage (Note 2)	−1.2V to +5.5V
Output Voltage (Note 2)	−0.5V to +5.5V
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DM54S270, DM54S370	4.5	5.5	V
DM74S270, DM74S370	4.75	5.25	V
Ambient Temperature (T_A)			
DM54S270, DM54S370	−55	+125	°C
DM74S270, DM74S370	0	+70	°C
Logical "0" Input Voltage	0	0.8	V
Logical "1" Input Voltage	2.0	5.5	V

dc electrical characteristics (Note 2)

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I_{IH}	Logical "1" Input Current	V_{IN} = 2.7V, V_{CC} = Max			25	μA
		V_{IN} = 5.5V, V_{CC} = Max			1.0	mA
I_{IL}	Logical "0" Input Current	V_{IN} = 0.45V, V_{CC} = Max			−250	μA
V_{CL}	Input Clamp Voltage	I_{IN} = −18 mA, V_{CC} = Min			−1.2	V
V_{OL}	Logical "0" Output Voltage					
	DM54S270, DM54S370	I_{OL} = 16 mA, V_{CC} = Min			0.50	V
	DM74S270, DM74S370				0.45	V
I_{CC}	Maximum Supply Current			100	150	mA
DM54S270, DM74S270						
I_{OH}	Logical "1" Output Current	V_{OUT} = 2.4V, V_{CC} = Max			50	μA
		V_{OUT} = 5.5V, V_{CC} = Max			100	μA
DM54S370, DM74S370						
V_{OH}	Logical "1" Output Voltage	V_{CC} = Min				
	DM54S370	I_{OH} = −2.0 mA	2.4			V
	DM74S370	I_{OH} = −6.5 mA	2.4			V
I_{OS}	Output Short Circuit Current	V_{OUT} = 0V (Note 3), V_{CC} = Max	−30		−100	mA
I_{OZ}	TRI-STATE Output Current	0.45V ≤ V_{OUT} ≤ 2.4V, V_{CC} = Max	−50		50	μA

switching characteristics (Note 2)

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{AA}	Address to Output Delay	R_L = 300Ω, C_L = 30 pF		35		ns
t_{EA}	Time to Enable Output			15		ns
t_{ED}	Time to Disable Output			15		ns

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at these values.

Note 2: These limits apply over the entire operating range unless stated otherwise. All typical values are for V_{CC} = 5.0V and T_A = 25°C.

Note 3: During I_{OS} measurement, only one output at a time should be grounded. Permanent damage may otherwise result.

Bipolar ROMs
Advance Information

DM54S271/DM74S271 open-collector 2048-bit ROM
DM54S371/DM74S371 TRI-STATE® 2048-bit ROM

general description

These TTL compatible memories are organized in the versatile 256 words by 8 bits configuration. Two memory enable inputs are provided to further enhance their versatility. When both enable inputs are in the logical "0" state, the eight outputs present the contents of the word selected by the address inputs.

If either or both of the enable inputs is raised to a logical "1" level, it causes all eight outputs to go to the "OFF" or high impedance state. The memories are available in both open-collector and TRI-STATE versions and are available as PROMs as well as ROMs.

features

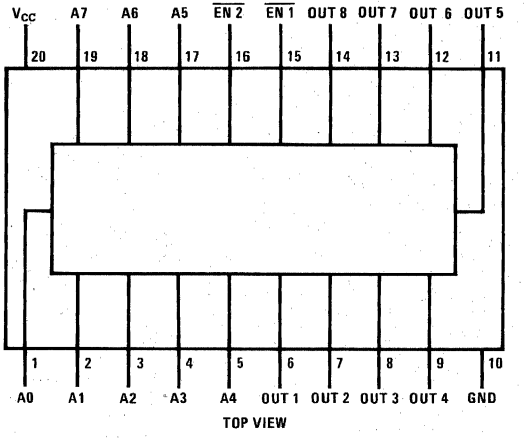
- Schottky clamped for high-speed systems
- High speed

Address to output delay—typical	35 ns
Enable to output delay—typical	15 ns

- PNP inputs reduce input loading
- 20 pin, 300 mil package for high density

connection diagram

Dual-In-Line Package



TOP VIEW

Order Number DM54S271N, DM54S371N,
DM74S271N or DM74S371N
See Package 16A

absolute maximum ratings (Note 1)

Supply Voltage (Note 2)	−0.5V to +7.0V
Input Voltage (Note 2)	−1.2V to +5.5V
Output Voltage (Note 2)	−0.5V to +5.5V
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DM54S271, DM54S371	4.5	5.5	V
DM74S271, DM74S371	4.75	5.25	V
Ambient Temperature (T_A)			
DM54S271, DM54S371	−55	+125	°C
DM74S271, DM74S371	0	+70	°C
Logical "0" Input Voltage	0	0.8	V
Logical "1" Input Voltage	2.0	5.5	V

dc electrical characteristics (Note 2)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
I_{IH}	Logical "1" Input Current	V_{IN} = 2.7V			25	μA
		V_{IN} = 5.5V			1.0	mA
I_{IL}	Logical "0" Input Current	V_{IN} = 0.45V			−250	μA
V_{CL}	Input Clamp Voltage	I_{IN} = −18 mA			−1.2	V
V_{OL}	Logical "0" Output Voltage	I_{OL} = 16 mA			0.50	V
I_{CC}	Maximum Supply Current			100	150	mA
DM54S271, DM74S271						
I_{OH}	Logical "1" Output Current	V_{OUT} = 2.4V			50	μA
		V_{OUT} = 5.5V			100	μA
DM54S371, DM74S371						
V_{OH}	Logical "1" Output Voltage					
	DM54S371	I_{OH} = −2.0 mA	2.4			V
	DM74S371	I_{OH} = −6.5 mA	2.4			V
I_{OS}	Output Short Circuit Current	V_{OUT} = 0V (Note 3) V_{CC} = Max	−30		−100	mA
I_{OZ}	TRI-STATE Output Current	0.45V ≤ V_{OUT} ≤ 2.4V	−50		50	μA

switching characteristics (Note 2)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{AA}	Address to Output Delay			35		ns
t_{EA}	Time to Enable Output	R_L = 300Ω C_L = 30 pF		15		ns
t_{ED}	Time to Disable Output			15		ns

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at these values.

Note 2: These limits apply over the entire operating range unless stated otherwise. All typical values are for V_{CC} = 5.0V and T_A = 25°C.

Note 3: During I_{OS} measurement, only one output at a time should be grounded. Permanent damage may otherwise result.

NATIONAL

Bipolar ROMs
Advance Information

DM72S04/DM82S04 TRI-STATE® 2048 bit ROM with latches

general description

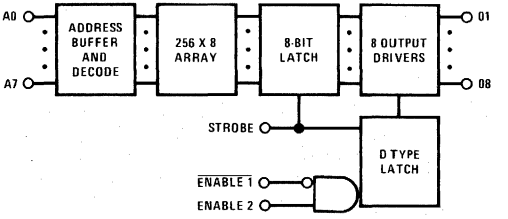
These TTL compatible memories are organized as 256 words by 8 bits. Two enable inputs are provided. When the strobe input is at a logical "1" level the memories function in the conventional manner with the enable inputs determining whether the outputs present the contents selected by the address inputs or are in the high impedance state. The outputs are in the high impedance state unless enable 1 is at a logical "0" and enable 2 is at a logical "1."

When the strobe is at a logical "0" the outputs are latched into the state they were in just prior to the strobe going low. The outputs remain in this condition until the strobe is again taken to the logical "1" state regardless of the state of the address or enable inputs.

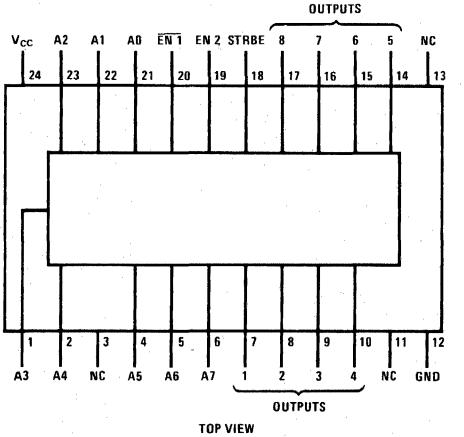
features

- Schottky clamped for high speed systems
- High speed
  - Enable to output delay—typical 15 ns
  - Strobe to output delay—typical 20 ns
  - Address to output delay—typical 35 ns
- PNP inputs reduce input loading
- Output latches simplify system use

logic and connection diagrams



Dual-In-Line Package



TOP VIEW

(NC = No Connection Internally)

Order Number DM72S04J or DM82S04J
See Package 11

Order Number DM82S04N
See Package 18

absolute maximum ratings (Note 1)

Supply Voltage (Note 2)	−0.5V to +7.0V
Input Voltage (Note 2)	−1.2V to +5.5V
Output Voltage (Note 2)	−0.5V to +5.5V
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DM72S04	4.5	5.5	V
DM82S04	4.75	5.25	V
Ambient Temperature (T_A)			
DM72S04	−55	+125	°C
DM82S04	0	+75	°C
Logical "0" Input Voltage	0	0.80	V
Logical "1" Input Voltage	2.0	5.5	V

dc electrical characteristics (Note 2)

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I_{IH}	Logical "1" Input Current	V_{IN} = 2.7V			25	μA
		V_{IN} = 5.5V			50	μA
I_{IL}	Logical "0" Input Current					
	DM72S04	V_{IN} = 0.45V			−250	μA
	DM82S04				−100	μA
V_{CL}	Input Clamp Voltage	I_{IN} = −18 mA			−1.2	V
V_{OL}	Logical "0" Output Voltage					
	DM72S04	I_{OUT} = 12 mA			0.50	V
	DM82S04				0.45	V
V_{OH}	Logical "1" Output Voltage					
	DM72S04	I_{OUT} = −2.0 mA	2.4			V
	DM82S04	I_{OUT} = −2.0 mA	2.7			V
	DM82S04	I_{OUT} = −6.5 mA	2.4			V
I_{OS}	Output Short Circuit Current	V_{OUT} = 0V (Note 3) V_{CC} = Max	−30		−100	mA
I_{OZ}	TRI-STATE Output Current					
	DM72S04	$0.45V \leq V_{OUT} \leq 2.4V$	−50		50	μA
	DM82S04	$0.45V \leq V_{OUT} \leq 5.5V$	−50		50	μA
I_{CC}	Maximum Supply Current			110	170	mA

switching characteristics (Note 2)

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{AA}	Address to Output Delay	Strobe = "1"		35		ns
t_{EA}	Time to Enable Output	Strobe = "1"		15		ns
t_{ED}	Time to Disable Output	Strobe = "1"		15		ns
t_{SA}	Strobe to Output Delay			20		ns
t_{SW}	Strobe Pulse Width			10		ns

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at these values.

Note 2: These limits apply over the entire operating range unless stated otherwise. All typical values are for V_{CC} = 5.0V and T_A = 25°C.

Note 3: During I_{OS} measurement, only one output at a time should be grounded. Permanent damage may otherwise result.

NATIONAL

Bipolar ROMs
Advance Information

DM75S28/DM85S28 TRI-STATE® 8192-bit ROM
DM75S29/DM85S29 open-collector 8192-bit ROM

general description

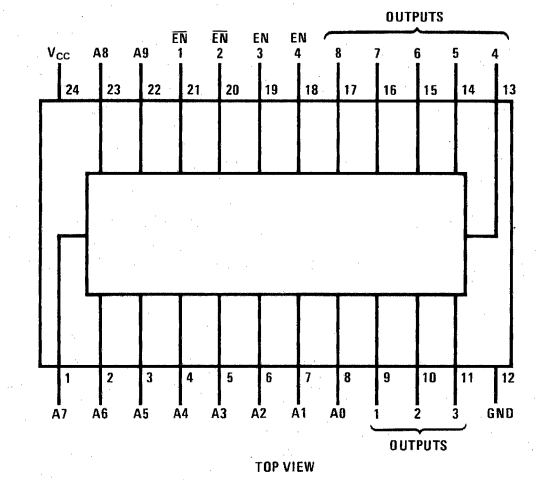
These TTL compatible memories are organized in a versatile 1024 words by 8 bits configuration. To add to the versatility, four memory enable inputs are provided, two of the enable inputs are complemented for further simplification in the system. The memory is enabled when Enable 1 and Enable 2 are both in the logical "1" state and simultaneously Enable 3 and Enable 4 are both in the logical "0" state. For all other conditions of the enable inputs, the memory is disabled and the outputs are in the "OFF" or high impedance state. When the memory is enabled, the 8 outputs present the contents of the word selected by the address inputs. The user may specify either TRI-STATE or open-collector outputs.

features

- Schottky-clamped for high speed systems
- High speed
  - Enable to output delay—typical 20 ns
  - Address to output delay—typical 50 ns
- PNP inputs reduce input loading
- Four enable inputs allow expansion to 16k words by 8 bits without additional decoding
- Pin compatible with A5280 and A5281

connection diagram

Dual-In-Line Package



TOP VIEW

Note: The chip is enabled when $\overline{E1}$ and $\overline{E2}$ are low and E3 and E4 are high.

Order Number DM75S28J, DM85S28J, DM75S29J or DM85S29J
See Package 11
Order Number DM85S28N or DM85S29N
See Package 18

7

absolute maximum ratings (Note 1)

Supply Voltage	−0.5V to +7.0V
Input Voltage	−1.2V to +5.5V
Output Voltage	−0.5V to +5.5V
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DM75S28, DM75S29	4.5	5.5	V
DM85S28, DM85S29	4.75	5.25	V
Ambient Temperature (T_A)			
DM75S28, DM75S29	−55	+125	°C
DM85S28, DM85S29	0	+70	°C
Logical "0" Input Voltage	0	0.8	V
Logical "1" Input Voltage	2.0	5.5	V

dc electrical characteristics (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I_{IH} Logical "1" Input Current	V_{IN} = 2.7V, V_{CC} = Max			25	μA
	V_{IN} = 5.5V			1.0	mA
I_{IL} Logical "0" Input Current	V_{IN} = 0.45V, V_{CC} = Max			−250	μA
V_{CL} Input Clamp Voltage	I_{IN} = −18 mA, V_{CC} = Min			−1.2	V
V_{OL} Logical "0" Output Voltage					
DM75S28, DM75S29	I_{OL} = 10 mA, V_{CC} = Min			0.5	V
DM85S28, DM85S29				0.45	V
I_{CC} Maximum Supply Current	V_{CC} = Max		130	190	mA
DM75S29, DM85S29					
I_{OH} Logical "1" Output Current	V_{OH} = 2.4V, V_{CC} = Max			50	μA
	V_{OH} = 5.5V			100	μA
DM75S28, DM85S28					
V_{OH} Logical "1" Output Voltage	V_{CC} = Min				
DM75S28	I_{OH} = −2.0 mA	2.4			V
DM85S28	I_{OH} = −6.5 mA	2.4			V
I_{OS} Output Short Circuit Current	V_{OUT} = 0V, (Note 3), V_{CC} = Max	−30		−100	mA
I_{OZ} TRI-STATE Output Current	0.45V ≤ V_{OUT} ≤ 2.4V, V_{CC} = Max	−50		50	μA

ac electrical characteristics (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{AA} Address to Output Delay	R_L = 400Ω, C_L = 30 pF		50		ns
t_{EA} Time to Enable Output			20		ns
t_{ED} Time to Disable Output			20		ns

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at these values.

Note 2: These limits apply over the entire operating range unless stated otherwise. All typical values are for V_{CC} = 5.0V and T_A = 25°C.

Note 3: During I_{OS} measurement only one output at a time should be grounded. Permanent damage may otherwise result.

NATIONAL

Bipolar ROMs
Advance Information

DM8531 16,384-bit ROM

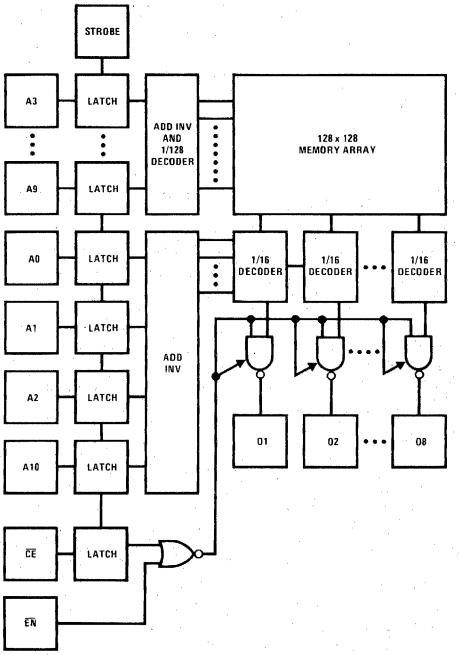
general description

The DM8531 is a 16,384-bit bipolar mask programmable ROM organized as 2048 x 8-bit words. Eleven address inputs select the desired 1-of-2048 words. All eleven address inputs and one of the two enable inputs have latch feature. The latch function is controlled by the strobe input. The two enable lines are used to either enable or disable the circuit. Truth table and logic diagram for this device are shown below. TRI-STATE® outputs allow for expansion to a greater number of words without sacrifice in speed as would be evidenced by open-collector outputs.

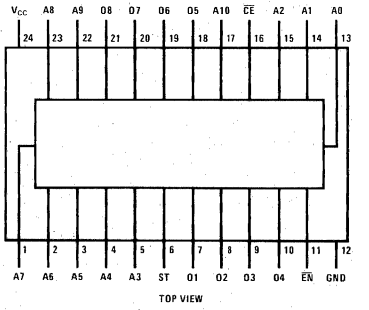
features

- 2k x 8 organization
- On-chip input latches
- TRI-STATE® outputs

logic and connection diagrams



Dual-In-Line Package



Order Number DM8531J
See Package 11
Order Number DM8531N
See Package 18

truth table

t			t + 1			
$\overline{CE}$	$\overline{EN}$	ST	$\overline{CE}$	$\overline{EN}$	ST	OUTPUTS
X	X	X	0	0	1	Read Stored Data
X	X	X	1	X	1	Hi-Z State
X	X	X	X	1	1	Hi-Z State
0	X	1	X	0	0	Read Stored Data for Address Inputs at t
1	X	1	X	X	0	Hi-Z State
X	X	X	X	1	0	Hi-Z State

absolute maximum ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Output Voltage	5.5V
Storage Temperature Range	−65°C to +160°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})	4.75	5.25	V
Temperature (T_A)	0	+70	°C

electrical characteristics (Notes 2 and 3)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	Logical "1" Input Voltage	V_{CC} = Min		2			V
I_{IH}	Logical "1" Input Current	V_{CC} = Max	V_{IN} = 2.4V			40	μA
			V_{IN} = 5.5V			1	mA
V_{IL}	Logical "0" Input Voltage	V_{CC} = Min				0.8	V
I_{IL}	Logical "0" Input Current	V_{CC} = Max, V_{IN} = 0.4V				−0.8	mA
V_{CD}	Input Clamp Voltage	V_{CC} = Min, V_{IN} = −12 mA		−1.5			V
V_{OH}	Logical "1" Output Voltage	V_{CC} = Min, I_{OUT} = −0.4 mA		2.4			V
I_{OS}	Output Short Circuit Current	V_{CC} = Max, V_{OUT} = 0V, (Note 4)		−15		−50	mA
V_{OL}	Logical "0" Output Voltage	V_{CC} = Min, I_{OUT} = 6 mA				0.45	V
I_{CC}	Supply Current	V_{CC} = Max			115	160	mA
I_{OZ}	TRI-STATE Output Current	V_{CC} = Max	V_{OUT} = 0.4V			−40	μA
			V_{OUT} = 2.4V			40	μA

switching characteristics

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{PHL}	Propagation Delay to a Logical "0" from Address Inputs to Outputs			200	450	ns
t_{PLH}	Propagation Delay to a Logical "1" from Address Inputs to Outputs			150	450	ns
t_{HZ}	Delay from Enable ($\overline{CE}$, $\overline{EN}$) to High Impedance State (from Logical "1" Level)			20	50	ns
t_{LZ}	Delay from Enable ($\overline{CE}$, $\overline{EN}$) to High Impedance State (from Logical "0" Level)			40	60	ns
t_{ZH}	Delay from Enable ($\overline{CE}$, $\overline{EN}$) to Logical "1" Level (from High Impedance State)			40	80	ns
t_{ZL}	Delay from Enable ($\overline{CE}$, $\overline{EN}$) to Logical "0" Level (from High Impedance State)			70	165	ns
t_{S1}	Address Set-Up Time		30	10		ns
t_{H1}	Address Hold Time		30	10		ns
t_{S2}	Enable Set-Up Time		30	10		ns
t_{H2}	Enable Hold Time		30	10		ns
t_W	Minimum Strobe Pulse Width		40	20		ns
t_{ST}	Strobe Access Time			250	450	ns

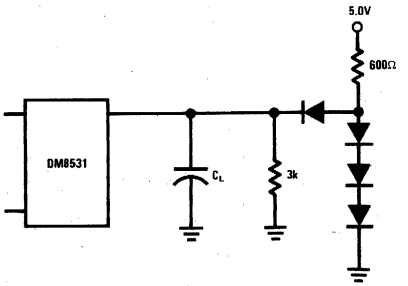
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C range for the DM8531. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4. Only one output at a time should be shorted.

ac test circuit

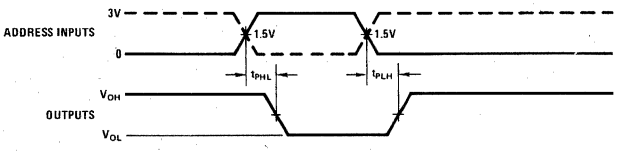


All Diodes are FD100

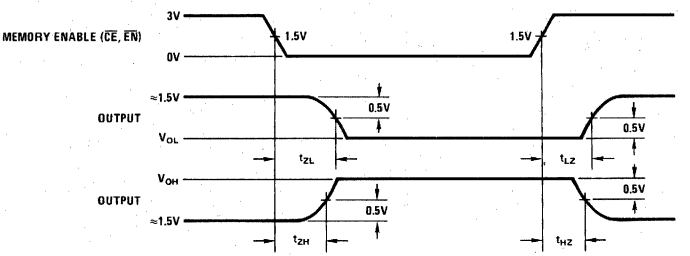
AC PARAMETERS	CL
t_{LZ}	5 pF
t_{HZ}	5 pF
All Others	50 pF

switching time waveforms

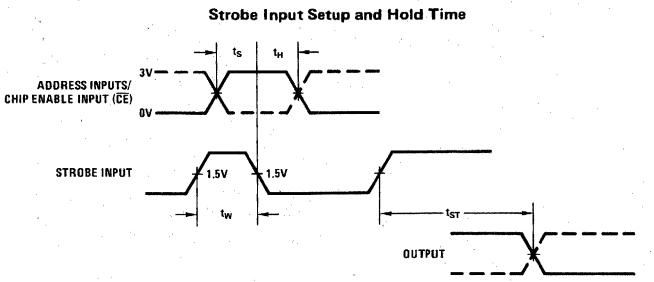
Address to Output Access Time



Memory Enable to Output Access Time



Strobe Input Setup and Hold Time



Notes: Input pulse waveform characteristics
f = 1 MHz, $t_r = t_f \leq 10$ ns (10% to 90%), duty cycle = 50%

Bipolar ROMs

DM7575/DM8575, DM7576/DM8576 programmable logic array (PLA)

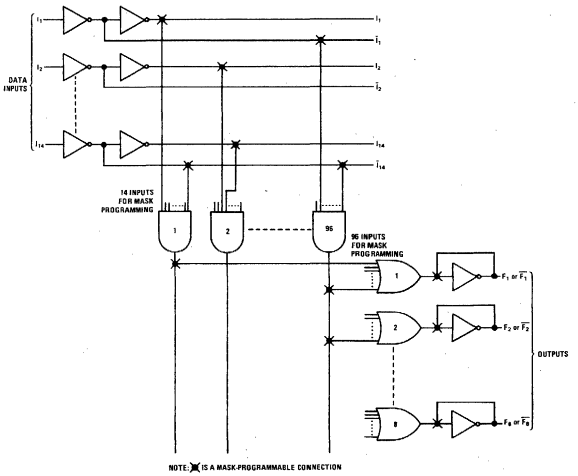
general description

The DM7575/DM8575 and DM7576/DM8576 are mask-programmable logic arrays designed for use in applications where random logic is required. The devices have fourteen data inputs and eight outputs. Each output provides a sum of product terms where each product term can contain any combination of 14 variables or their complements. The total number of product terms which can be provided is 96. Any product term which is repeated is counted only once. Since some functions are more easily represented in their inverted form, an option is provided to allow for either the true or complement of the function on each output. The products are particularly useful in providing control logic for digital systems. The DM7575/DM8575 has a conventional totem-pole output whereas the DM7576/DM8576 is provided with a passive pullup output. This latter configuration is useful in expanding functions by connection of outputs of different packages.

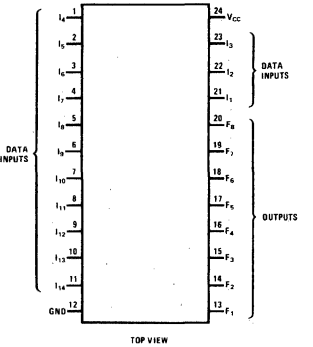
features

- A 2^{14}-by-8 (128k) bit memory would be needed to provide equivalent function
- Typical delay 90 ns
- Typical power dissipation 550 mW
- Series 54/74 compatible

logic and connection diagrams



Dual-In-Line Package



Order Number DM7575J, DM8575J, DM7576J or DM8576J
See Package 11
Order Number DM8575N or DM8576N
See Package 18

absolute maximum ratings (Note 1)

Supply Voltage	7.0V
Input Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DM7575, DM7576	4.5	5.5	V
DM8575, DM8576	4.75	5.25	V
Temperature (T_A)			
DM7575, DM7576	−55	+125	°C
DM8575, DM8576	0	70	°C

electrical characteristics (Note 2)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
Logical "1" Input Voltage		V_{CC} = Min	2			V
Logical "0" Input Voltage		V_{CC} = Min			0.8	V
Logical "1" Output Voltage (DM7575/DM8575 Only)		V_{CC} = Min, $V_{IN(1)}$ = 2V, $V_{IN(0)}$ = 0.8V, I_{OUT} = −800μA	2.4			V
Logical "1" Output Current (DM7576/DM8576 Only)		V_{CC} = Max, V_{OUT} = 5.5V			100	μA
Logical "0" Output Voltage		V_{CC} = Min, $V_{IN(1)}$ = 2V, $V_{IN(0)}$ = 0.8V, I_{OUT} = +12 mA			0.4	V
Logical "1" Input Current		V_{CC} = Max, V_{IN} = 2.4V			40	μA
		V_{CC} = Max, V_{IN} = 5.5V			1	mA
Logical "0" Input Current		V_{CC} = Max, V_{IN} = 0.4V			−1.0	mA
Output Short Circuit Current (Note 3)	DM7575/76	V_{CC} = Max, V_{OUT} = 0V	−20/−1.75		−55/−3.5	mA
	DM8575/76		−18/−1.65		−55/−3.3	
Supply Current		V_{CC} = Max		110	170	mA
Input Diode Clamp Voltage		V_{CC} = Min, T_A = 25°C, I_{IN} = −12 mA			−1.5	V
Propagation Delay to a Logical "0" from Data Inputs to Outputs, t_{pd0}		V_{CC} = 5.0V, T_A = 25°C, C_L = 50 pF, R_L = 400Ω		100	150	ns
Propagation Delay to a Logical "1" from Data Inputs to Outputs, t_{pd1}		V_{CC} = 5.0V, T_A = 25°C		80	150	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DM7575/76 and across the 0°C to 70°C range for the DM8575/76. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

Note 3: Only one output at a time should be shorted.

information needed to program the PLA

Information to program the PLA can be supplied in one of two formats:

1. Punched 80-column cards
2. The applicable section of this data sheet (manual entry of information).

punched cards

CARD 1: (Used to determine whether outputs are presented in their true or inverted form. If this card is not used it is assumed that all eight outputs are true.)

Col. 1-6: DM7575 or DM8575 or DM7576 or DM8576.

Col. 7-9: (Blank)

Col. 10-17: Output Data. Outputs are F_8 (most significant) to F_1 (least significant). All eight outputs must be specified.

A 'T' in an output location indicates that the output is true.

A 'C' in an output location indicates that the output is complemented (inverted).

Col. 18-39: (Blank)

Col. 40-75: This space is reserved for any unique letters/numbers desired by the customer (special part number, program number, etc.). However the exact combination of characters must appear on all cards, but only those cards, associated with that particular device.

Col. 76-78: (Blank)

Col. 79-80: 00

CARDS 2-97: Term Data Cards. Used to specify the input and output conditions.

Col. 1-6: DM7575 or DM8575 or DM7576 or DM8576.

Col. 7-9: (Blank)

Col. 10-17: Output Connections. Outputs are F_8 (most significant) to F_1 (least significant). This field describes the outputs on which the product term appears.

A '+' in one of the eight output locations indicates that the term described by the card is one of the "OR" terms in that output.

A '(blank)' in one of the eight output locations indicates that the term described by the card is not one of the "OR" terms in that output.

(Care should be exercised in punching this particular field; since in most cases, unless a product term is repeated, this field will appear as one '+' and seven blanks.)

Col. 18: (Blank)

Col. 19: = (equal sign)

Col. 20: (Blank)

Col. 21-34: Input Data. Inputs are I_{14} (most significant) to I_1 (least significant).

An 'H' in one of the fourteen locations indicates that input appears in the high state in the output term.

An 'L' in one of the fourteen input locations indicates that input appears in the low state in the output term.

An 'X' in one of the fourteen input locations indicates that input does not appear in the output term.

Col. 35-39: (Blank)

Col. 40-75: This space is reserved for any unique letter/number desired by the customer (special part number, program number, etc.) However the exact combination of characters must appear on all cards, but only those cards, associated with that particular device. The purpose of this section is to prevent mixing of cards.

Col. 76-78: (Blank)

Col. 79-80: Product Term Number 01 to 96. (All 96 cards need not be used.) Zero in column 79 may be suppressed.

manual entry

The matrix-blank shown in this data sheet can be used in lieu of punched cards to submit information for programming the PLA.

INSTRUCTIONS

1. Circle the appropriate part number. In the event a catalog part is not being purchased, circle the closest catalog part number. If an electrical screen is required between the military and commerical devices, the military designation should be circled.
2. Customer should write the name of his company.
3. Enter the total number of unique product terms found in all eight outputs. Repeated terms count only once.
4. Output Inverter Option. Under the appropriate output designation specify a 'T' when the high (true) level is desired on the output for the given input conditions. Specify a 'C' if the complement is needed.
5. Matrix
   a. Input data. This block is used to describe what comprises each of the 96 (maximum) product terms. In each row, opposite the appropriate Product Term number, information on the fourteen Input Data locations is entered. Information must be entered on all 14 inputs.
      1). Enter an "H" under the appropriate input designation if that particular input appears in the product term as a high (true) level.
      2). Enter an "L" under the appropriate input designation if that particular input appears in the product term as a low (complemented) level.
      3). Enter an "X" under the appropriate input designation if that particular input does not appear in the product term.

      If less than 96 product terms are used leave all spaces for the unused terms blank.

   b. Output Data. This block is used to describe the outputs on which the product terms appear.
      1). Enter a '+' under the appropriate output designation if the product term is contained in that output's expression.
      2). Leave a location blank if the product term is not contained in that output's expression.

truth table/order blank

1. PART NO. — (DM7575, DM8575, DM7576, DM8576)

2. CUSTOMER IDENTIFICATION –

3. TOTAL NO. OF UNIQUE PRODUCT TERMS USED –
(Repeated Terms Count Only Once)

4. OUTPUT INVERTER OPTION

F_8	F_7	F_6	F_5	F_4	F_3	F_2	F_1

5. MATRIX

PRODUCT TERM	INPUT DATA														OUTPUT DATA								
	I_{14}	I_{13}	I_{12}	I_{11}	I_{10}	I_9	I_8	I_7	I_6	I_5	I_4	I_3	I_2	I_1	F_8	F_7	F_6	F_5	F_4	F_3	F_2	F_1	
1																							
2																							
3																							
4																							
5																							
6																							
7																							
8																							
9																							
10																							
11																							
12																							
13																							
14																							
15																							
16																							
17																							
18																							
19																							
20																							
21																							
22																							
23																							
24																							
25																							
26																							
27																							
28																							
29																							
30																							
31																							
32																							
33																							
34																							
35																							
36																							
37																							
38																							
39																							
40																							
41																							
42																							

truth table/order blank (con't)

PRODUCT TERM	INPUT DATA															OUTPUT DATA								
	I_{14}	I_{13}	I_{12}	I_{11}	I_{10}	I_9	I_8	I_7	I_6	I_5	I_4	I_3	I_2	I_1		F_8	F_7	F_6	F_5	F_4	F_3	F_2	F_1	
43																								
44																								
45																								
46																								
47																								
48																								
49																								
50																								
51																								
52																								
53																								
54																								
55																								
56																								
57																								
58																								
59																								
60																								
61																								
62																								
63																								
64																								
65																								
66																								
67																								
68																								
69																								
70																								
71																								
72																								
73																								
74																								
75																								
76																								
77																								
78																								
79																								
80																								
81																								
82																								
83																								
84																								
85																								
86																								
87																								
88																								
89																								
90																								
91																								
92																								
93																								
94																								
95																								
96																								

truth table/order blank

1. PART NO. — (DM7575, DM8575, DM7576, DM8576)

DM7575AAA, DM8575AAA, DM7576AAA, DM8576AAA

2. CUSTOMER IDENTIFICATION —

STANDARD PATTERN — HOLLERITH 29 (IBM) TO ASCII

3. TOTAL NO. OF UNIQUE PRODUCT TERMS USED — (Repeated Terms Count Only Once) 96

4. OUTPUT INVERTER OPTION

F_8	F_7	F_6	F_5	F_4	F_3	F_2	F_1
T	T	T	T	T	T	T	T

5. MATRIX

PRODUCT TERM	INPUT DATA													OUTPUT DATA								Char. Assign.
	I_{14}	I_{13}	I_{12}	I_{11}	I_{10}	I_9	I_8	I_7	I_6	I_5	I_4	I_3	I_2	I_1	F_8	F_7	F_6	F_5	F_4	F_3	F_2	F_1	
1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	Space
2	0	0	0	1	1	0	0	0	0	0	0	0	0	1	1	0	1	0	0	0	0	1	!
3	0	0	0	1	1	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	1	0	"
4	0	0	0	1	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	1	1	#
5	0	0	0	1	0	0	0	0	1	0	0	0	1	0	1	0	1	0	0	1	0	0	$
6	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	0	1	0	0	1	0	1	%
7	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0	1	1	0	&
8	0	0	0	1	0	0	1	0	0	0	0	0	0	0	1	0	1	0	0	1	1	1	'
9	0	0	0	1	0	0	1	0	0	0	0	0	0	1	1	0	1	0	1	0	0	0	(
10	0	0	0	1	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	1	)
11	0	0	0	1	0	0	0	1	0	0	0	0	1	0	0	0	1	0	1	0	1	0	*
12	0	0	0	1	0	1	0	0	0	0	0	0	0	1	1	0	1	0	1	0	1	1	+
13	0	0	0	1	0	0	0	0	1	0	0	1	0	0	0	0	1	0	1	1	0	0	,
14	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0	1	1	0	1	-
15	0	0	0	1	0	0	0	0	1	0	0	0	0	1	1	0	1	0	1	1	1	0	.
16	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	1	0	1	1	1	1	/
17	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	1	1	0	0	0	0	0
18	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	1	0	0	0	1	1
19	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	1	0	0	1	0	2
20	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0	1	1	0	0	1	1	3
21	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	1	1	0	1	0	0	4
22	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	1	1	0	1	0	1	5
23	0	0	0	0	0	1	0	0	0	0	0	0	0	0	1	0	1	1	0	1	1	0	6
24	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	1	1	7
25	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	8
26	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	0	0	1	9
27	0	0	0	1	0	0	0	0	0	1	0	0	0	0	1	0	1	1	1	0	1	0	:
28	0	0	0	1	0	1	0	0	0	0	0	0	1	0	0	0	1	1	1	0	1	1	;
29	0	0	0	1	0	0	0	1	0	0	0	0	0	1	1	0	1	1	1	1	0	0	<
30	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	1	=
31	0	0	0	1	0	1	0	0	0	0	0	1	0	0	0	0	1	1	1	1	1	0	>
32	0	0	0	1	1	0	0	0	0	0	0	1	0	0	1	0	1	1	1	1	1	1	?
33	0	0	0	1	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	@
34	0	0	0	0	0	0	0	0	0	0	1	0	0	1	1	1	0	0	0	0	0	1	A
35	0	0	0	0	0	0	0	0	0	1	0	0	0	1	1	1	0	0	0	0	1	0	B
36	0	0	0	0	0	0	0	0	1	0	0	0	0	1	0	1	0	0	0	0	1	1	C
37	0	0	0	0	0	0	0	1	0	0	0	0	0	1	1	1	0	0	0	1	0	0	D
38	0	0	0	0	0	0	1	0	0	0	0	0	0	1	0	1	0	0	0	1	0	1	E
39	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	1	0	0	0	1	1	0	F
40	0	0	0	0	1	0	0	0	0	0	0	0	0	1	1	1	0	0	0	1	1	1	G
41	0	0	0	1	0	0	0	0	0	0	0	0	0	1	1	1	0	0	1	0	0	0	H
42	0	0	1	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	1	0	0	1	I
CARD ZONES			9	8	7	6	5	4	3	2	1	0	11	12	ODD PAR	b_7	b_6	b_5	b_4	b_3	b_2	b_1	ASCII BITS

truth table/order blank (con't)

PRODUCT TERM	INPUT DATA														OUTPUT DATA								
	I_{14}	I_{13}	I_{12}	I_{11}	I_{10}	I_9	I_8	I_7	I_6	I_5	I_4	I_3	I_2	I_1	F_8	F_7	F_6	F_5	F_4	F_3	F_2	F_1	CHAR. (ASCII)
43	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	1	0	0	1	0	1	0	J
44	0	0	0	0	0	0	0	0	0	1	0	0	1	0	1	1	0	0	1	0	1	1	K
45	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0	1	0	0	1	1	0	0	L
46	0	0	0	0	0	0	0	1	0	0	0	0	1	0	1	1	0	0	1	1	0	1	M
47	0	0	0	0	0	0	1	0	0	0	0	0	1	0	1	1	0	0	1	1	1	0	N
48	0	0	0	0	0	1	0	0	0	0	0	0	1	0	0	1	0	0	1	1	1	1	O
49	0	0	0	0	1	0	0	0	0	0	0	0	1	0	1	1	0	1	0	0	0	0	P
50	0	0	0	1	0	0	0	0	0	0	0	0	1	0	0	1	0	1	0	0	0	1	Q
51	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	1	0	1	0	0	1	0	R
52	0	0	0	0	0	0	0	0	0	1	0	1	0	0	1	1	0	1	0	0	1	1	S
53	0	0	0	0	0	0	0	0	1	0	0	1	0	0	0	1	0	1	0	1	0	0	T
54	0	0	0	0	0	0	0	1	0	0	0	1	0	0	1	1	0	1	0	1	0	1	U
55	0	0	0	0	0	0	1	0	0	0	0	1	0	0	1	1	0	1	0	1	1	0	V
56	0	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	1	1	1	W
57	0	0	0	0	1	0	0	0	0	0	0	1	0	0	0	1	0	1	1	0	0	0	X
58	0	0	0	1	0	0	0	0	0	0	0	1	0	0	1	1	0	1	1	0	0	1	Y
59	0	0	1	0	0	0	0	0	0	0	0	1	0	0	1	1	0	1	1	0	1	0	Z
60	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	1	1	0	1	1	[
61	0	0	0	1	0	0	0	0	0	1	0	1	0	0	1	1	0	1	1	1	0	0	\
62	0	0	0	1	0	0	0	0	0	1	0	0	1	0	0	1	0	1	1	1	0	1	]
63	0	0	0	1	1	0	0	0	0	0	0	0	1	0	0	1	0	1	1	1	1	0	^
64	0	0	0	1	0	0	1	0	0	0	0	1	0	0	1	1	0	1	1	1	1	1	_
65	0	0	0	1	0	0	0	0	0	0	1	0	0	0	1	1	1	0	0	0	0	0	`
66	0	0	0	0	0	0	0	0	0	0	1	1	0	1	0	1	1	0	0	0	0	1	a
67	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0	1	1	0	0	0	1	0	b
68	0	0	0	0	0	0	0	0	1	0	0	1	0	1	1	1	1	0	0	0	1	1	c
69	0	0	0	0	0	0	0	1	0	0	0	1	0	1	0	1	1	0	0	1	0	0	d
70	0	0	0	0	0	0	1	0	0	0	0	1	0	1	1	1	1	0	0	1	0	1	e
71	0	0	0	0	0	1	0	0	0	0	0	1	0	1	1	1	1	0	0	1	1	0	f
72	0	0	0	0	1	0	0	0	0	0	0	1	0	1	0	1	1	0	0	1	1	1	g
73	0	0	0	1	0	0	0	0	0	0	0	1	0	1	0	1	1	0	1	0	0	0	h
74	0	0	1	0	0	0	0	0	0	0	0	1	0	1	1	1	1	0	1	0	0	1	i
75	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	1	0	1	0	1	0	j
76	0	0	0	0	0	0	0	0	0	1	0	0	1	1	0	1	1	0	1	0	1	1	k
77	0	0	0	0	0	0	0	0	1	0	0	0	1	1	1	1	1	0	1	1	0	0	l
78	0	0	0	0	0	0	0	1	0	0	0	0	1	1	0	1	1	0	1	1	0	1	m
79	0	0	0	0	0	0	1	0	0	0	0	0	1	1	0	1	1	0	1	1	1	0	n
80	0	0	0	0	0	1	0	0	0	0	0	0	1	1	1	1	1	0	1	1	1	1	o
81	0	0	0	0	1	0	0	0	0	0	0	0	1	1	0	1	1	1	0	0	0	0	p
82	0	0	0	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	1	q
83	0	0	1	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	0	1	0	r
84	0	0	0	0	0	0	0	0	0	1	0	1	1	0	0	1	1	1	0	0	1	1	s
85	0	0	0	0	0	0	0	0	1	0	0	1	1	0	1	1	1	1	0	1	0	0	t
86	0	0	0	0	0	0	0	1	0	0	0	1	1	0	0	1	1	1	0	1	0	1	u
87	0	0	0	0	0	0	1	0	0	0	0	1	1	0	0	1	1	1	0	1	1	0	v
88	0	0	0	0	0	1	0	0	0	0	0	1	1	0	1	1	1	1	0	1	1	1	w
89	0	0	0	0	1	0	0	0	0	0	0	1	1	0	1	1	1	1	1	0	0	0	x
90	0	0	0	1	0	0	0	0	0	0	0	1	1	0	0	1	1	1	1	0	0	1	y
91	0	0	1	0	0	0	0	0	0	0	0	1	1	0	0	1	1	1	1	0	1	0	z
92	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	1	1	1	0	1	1	{
93	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	1	1	1	1	0	0	|
94	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	1	1	1	1	1	0	1	}
95	0	0	0	0	0	0	0	0	0	0	1	1	1	0	1	1	1	1	1	1	1	0	~
96	0	0	1	0	1	0	0	0	0	0	0	0	0	1	0	1	1	1	1	1	1	1	DEL
CARD ZONES			9	8	7	6	5	4	3	2	1	0	11	12	ODD PAR	b_7	b_6	b_5	b_4	b_3	b_2	b_1	ASCII BITS

NATIONAL

Bipolar ROMs

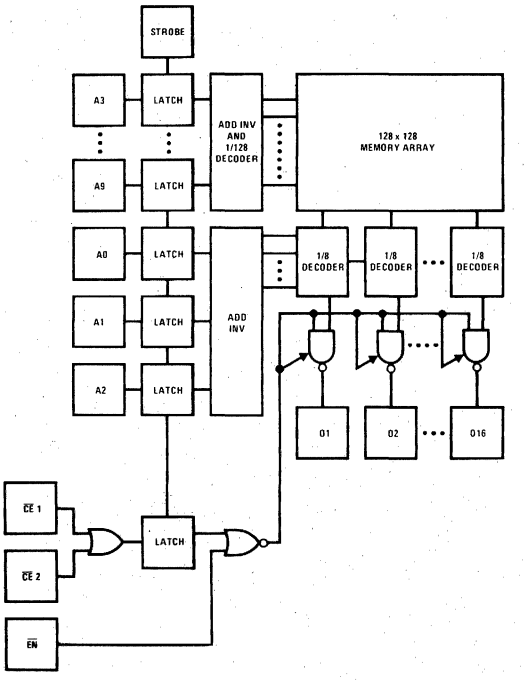
Advance Information

DM8581 1024×16 bit ROM (TSL)

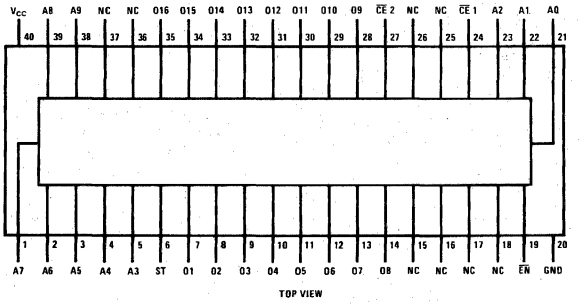
general description

The DM8581 is a 16,384-bit bipolar mask programmable ROM organized as 1024 16-bit words. Ten address inputs select the desired 1-of-1024 words. All ten address inputs and two of the three enable inputs have latch feature. The latch function is controlled by the strobe input. The three enable lines are used to either enable or disable the circuit. Truth table and logic diagram for this device are shown below. TRI-STATE® outputs allow for expansion to a greater number of words without sacrifice in speed as would be evidenced by open-collector outputs.

logic and connection diagrams



Dual-In-Line Package



TOP VIEW

Order Number DM8581D
See Package 8
Order Number DM8581N
See Package 20

absolute maximum ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Output Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})	4.75	5.25	V
Temperature (T_A)	0	+70	°C

electrical characteristics (Notes 2 and 3)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	Logical "1" Input Voltage	V_{CC} = Min		2			V
I_{IH}	Logical "1" Input Current	V_{CC} = Max	V_{IN} = 2.4V			40	μA
			V_{IN} = 5.5V			1	mA
V_{IL}	Logical "0" Input Voltage	V_{CC} = Min				0.8	V
I_{IL}	Logical "0" Input Current	V_{CC} = Max, V_{IN} = 0.4V				−0.8	mA
V_{CD}	Input Clamp Voltage	V_{CC} = Min, V_{IN} = −12 mA		−1.5			V
V_{OH}	Logical "1" Output Voltage	V_{CC} = Min, I_{OUT} = −800μA		2.4			V
I_{OS}	Output Short Circuit Current	V_{CC} = Max, V_{OUT} = 0V, (Note 4)		−20		−50	mA
V_{OL}	Logical "0" Output Voltage	V_{CC} = Min, I_{OUT} = 6 mA				0.4	V
I_{CC}	Supply Current	V_{CC} = Max			115		mA
	TRI-STATE Output Current	V_{CC} = Max	V_{OUT} = 0.4V			−40	μA
			V_{OUT} = 2.4V			40	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C range for the DM8581. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Only one output at a time should be shorted.

switching characteristics

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{PD0}	Propagation Delay to a Logical "0" From Address Inputs to Outputs	V_{CC} = 5.0V, T_A = 25°C		100		ns
t_{PD1}	Propagation Delay to a Logical "1" From Address Inputs to Outputs	V_{CC} = 5.0V, T_A = 25°C		300		ns
t_{1H}	Delay From Enable ($\overline{CE}$, $\overline{EN}$) to High Impedance State (From Logical "1" Level)	V_{CC} = 5.0V, T_A = 25°C		20		
t_{0H}	Delay From Enable ($\overline{CE}$, $\overline{EN}$) to High Impedance State (From Logical "0" Level)	V_{CC} = 5.0V, T_A = 25°C		40		ns
t_{H1}	Delay From Enable ($\overline{CE}$, $\overline{EN}$) to Logical "1" Level (From High Impedance State)	V_{CC} = 5.0V, T_A = 25°C		70		
t_{H0}	Delay From Enable ($\overline{CE}$, $\overline{EN}$) to Logical "0" Level (From High Impedance State)	V_{CC} = 5.0V, T_A = 25°C		60		
t_{S1}	With Respect to Strobe Address Setup Time	V_{CC} = 5.0V, T_A = 25°C				
t_{H1}	Address Hold Time	V_{CC} = 5.0V, T_A = 25°C				
t_{S2}	Enable Setup Time	V_{CC} = 5.0V, T_A = 25°C				
t_{H2}	Enable Hold Time	V_{CC} = 5.0V, T_A = 25°C				
t_W	Minimum Strobe Pulse Width	V_{CC} = 5.0V, T_A = 25°C		20		
t_{ST}	Strobe Access Time	V_{CC} = 5.0V, T_A = 25°C		300		

truth table

$\overline{CE1}$ t	$\overline{CE2}$ t	ST t	$\overline{CE1}$ t + 1	$\overline{CE2}$ t + 1	$\overline{EN}$ t + 1	ST t + 1	OUTPUT t + 1
X	X	X	0	0	0	1	Read stored data for add inputs at t + 1
X	X	X	1	X	X	1	Hi-Z
X	X	X	X	1	X	1	Hi-Z
X	X	X	X	X	1	1	Hi-Z
0	0	1	X	X	0	0	Read stored data for add inputs at t
1	X	1	X	X	X	0	Hi-Z
X	1	1	X	X	X	0	Hi-Z
X	X	X	X	X	1	0	Hi-Z

Bipolar ROMs

DM7595/DM8595 4096-bit bipolar ROM
DM7795/DM8795 4096-bit bipolar ROM

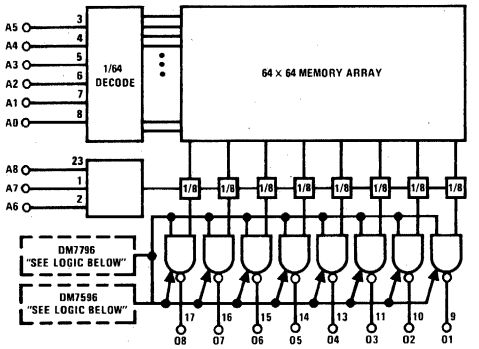
general description

The DM7595/DM8595 and DM7795/DM8795 are 4096-bit bipolar mask-programmable ROMs organized as 512 eight-bit words. Nine address inputs select the desired one-of-512 words. Four enable lines are used to either enable or disable the circuit. The two devices differ in the enable logic. Truth tables and logic diagrams for each device are shown below. Open collector outputs allow for expansion to greater number of words.

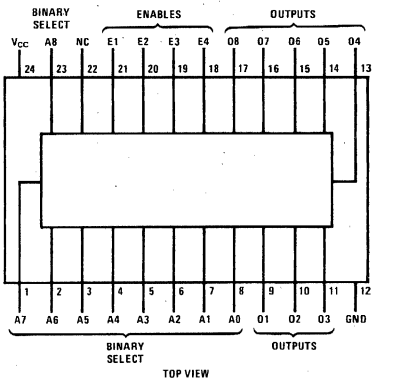
features

- Series 54/74 specification compatibility
- Pin compatible with monolithic memories 5240/6240
- Typical address time 80 ns
- Open collector output

logic and connection diagrams



Dual-In-Line Package

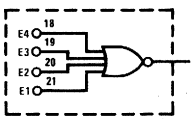


Order Number DM7595J, DM8595J, DM7795J or DM8795J
See Package 11

Order Number DM8595N or DM8795N
See Package 18

logic diagrams and truth tables for enable circuitry

DM7595/DM8595



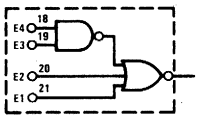
DM7595/DM8595

E1	E2	E3	E4	OUTPUT
0	0	0	0	Read Stored Data
1	X	X	X	Logical "1"
X	1	X	X	Logical "1"
X	X	1	X	Logical "1"
X	X	X	1	Logical "1"

X = Don't Care

ENABLE = E1 • E2 • E3 • E4

DM7795/DM8795



DM7795/DM8795

E1	E2	E3	E4	OUTPUT
0	0	1	1	Read Stored Data
1	X	X	X	Logical "1"
X	1	X	X	Logical "1"
X	X	0	X	Logical "1"
X	X	X	0	Logical "1"

X = Don't Care

ENABLE = E1 • E2 • E3 • E4

absolute maximum ratings (Note 1)

Supply Voltage	7.0V
Input Voltage	5.5V
Output Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DM7595, DM7795	4.5	5.5	V
DM8595, DM8795	4.75	5.25	V
Temperature (T_A)			
DM7595, DM7795	−55	+125	°C
DM8595, DM8795	0	+70	°C

electrical characteristics (Note 2)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	Logical "1" Input Voltage	V_{CC} = Min		2.0			V
V_{IL}	Logical "0" Input Voltage	V_{CC} = Min				0.8	V
I_{OH}	Logical "1" Output Current	V_{CC} = Max, V_O = 5.5V				100	μA
V_{OL}	Logical "0" Output Voltage	V_{CC} = Min, I_O = 12 mA				0.4	V
I_{IH}	Logical "1" Input Current	V_{CC} = Max	V_{IN} = 2.4V			40	μA
			V_{IN} = 5.5V			1	mA
I_{IL}	Logical "0" Input Current	V_{CC} = Max, V_{IN} = 0.4V				−1.0	mA
I_{CC}	Supply Current	V_{CC} = Max			103	158	mA
V_{IC}	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −12 mA				−1.5	V

switching characteristics (Note 2)

PARAMETER		PARAMETER CONDITIONS	TEST CONDITIONS	DM7595,DM7795			DM8595,DM8795			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Propagation Delay Time, Low to High Level Output	Access Time from Address	C_L = 30 pF, R_L = 400Ω		80	150		80	120	ns
t_{PHL}	Propagation Delay Time, High to Low Level Output	Access Time from Address			80	150		80	120	ns
t_{PLH}	Output Disable Time to High Level	Disable Time from Memory Enables			60	120		60	90	ns
t_{PHL}	Output Enable Time to Low Level	Access Times from Memory Enables			60	120		60	90	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DM7595 and DM7795 and across the 0°C to +70°C range for the DM8595 and DM8795. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

80-column card program data format

Col. 1-3: 3 Character ID code any 3 Alpha-Numeric characters. Must be the same on all cards associated with a particular pattern, but different for the ID code used on other patterns. The purpose of this code is to prevent mixing of cards.

Col. 4: (Blank)

Col. 5-12: Word Data. Order is 08 (most significant) to 01 (least significant). *Note 1.* Characters—For TTL high level are: H or 1. Characters—For TTL low are L or 0. "Don't Care" is X.

Col. 13: (Blank)

Col. 14-21: Word Data—same format as 5-12.

Col. 22: (Blank)

Col. 23-30: Word Data

Col. 31: (Blank)

Col. 32-39: Word Data

Col. 40: (Blank)

Col. 41-48: Word Data

Col. 49: (Blank)

Col. 50-57: Word Data

Col. 58: (Blank)

Col. 59-66: Word Data

Col. 67: (Blank)

Col. 68-75: Word Data

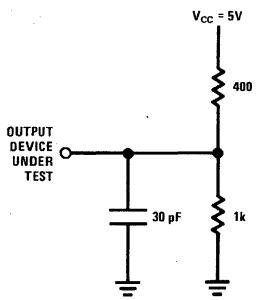
Col. 76-78: (Blank)

Col. 79-80: Card sequence number. 1 to 64. Leading zeros may be punched or suppressed. *(Note 2)*

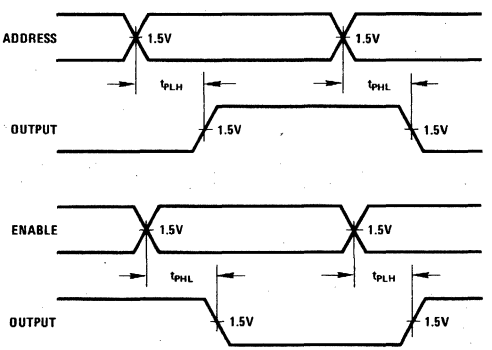
Note 1: The words are listed in sequence beginning on the first card with the word associated with address 0 and ending on the last card with the word associated with address 511. Address input A_8 is the most significant; A_0, the least significant.

Note 2: Card sequence numbers reference a specific group of 8 words, i.e.;
Card 01: Word address 0 to 7
Card 02: Word address 8 to 15
Card 03: Word address 16 to 23
. .
. .
. .
Card 64: Word address 504 to 511.

ac test circuit



switching time waveforms



Input waveforms are supplied by pulse generators having the following characteristics: $t \leq 10$ ns, $t_f \leq 10$ ns, PRR = 1 MHz, Amplitude = 3.0V, PDC = 50%, and $Z_O = 50\Omega$.

Bipolar ROMs

DM7596/DM8596 TRI-STATE® 4096-bit bipolar ROM
DM7796/DM8796 TRI-STATE 4096-bit bipolar ROM

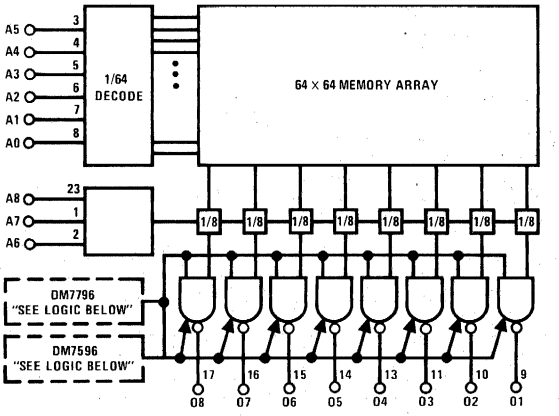
general description

The DM7596/DM8596 and DM7796/DM8796 are 4096-bit bipolar mask-programmable ROMs organized as 512 eight-bit words. Nine address inputs select the desired one-of-512 words. Four enable lines are used to either enable or disable the circuit. The two devices differ in the enable logic. Truth tables and logic diagrams for each device are shown below. TRI-STATE outputs allow for expansion to greater numbers of words without sacrifice in speed as would be evidenced by open-collector outputs.

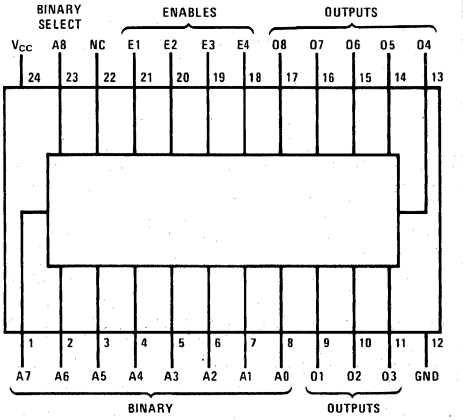
features

- Series 54/74 specification compatibility
- Pin compatible with Monolithic Memories MM5241/MM6241
- Typical address time 80 ns
- TRI-STATE outputs

logic and connection diagrams (Top View)



Dual-In-Line Package

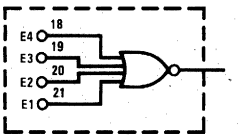


Order Number DM7596J, DM8596J, DM7796J or DM8796J
See Package 11

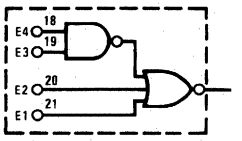
Order Number DM8596N or DM8796N
See Package 18

logic diagrams and truth tables for enable circuitry

DM7596/DM8596



DM7796/DM8796



DM7596/DM8596

E1	E2	E3	E4	OUTPUT
0	0	0	0	Read Stored Data
1	X	X	X	Hi - Z
X	1	X	X	Hi - Z
X	X	1	X	Hi - Z
X	X	X	1	Hi - Z

X = Don't Care ENABLE = $\overline{E}_1 \cdot \overline{E}_2 \cdot \overline{E}_3 \cdot \overline{E}_4$

DM7796/DM8796

E1	E2	E3	E4	OUTPUT
0	0	1	1	Read Stored Data
1	X	X	X	Hi - Z
X	1	X	X	Hi - Z
X	X	0	X	Hi - Z
X	X	X	0	Hi - Z

X = Don't Care ENABLE = $\overline{E}_1 \cdot \overline{E}_2 \cdot E_3 \cdot E_4$

absolute maximum ratings (Note 1)

Supply Voltage	7.0V
Input Voltage	5.5V
Output Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DM7596, DM7796	4.5	5.5	V
DM8596, DM8796	4.75	5.25	V
Temperature (T_A)			
DM7596, DM7796	−55	+125	°C
DM8596, DM8796	0	+70	°C

electrical characteristics (Note 2)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	Logical "1" Input Voltage	V_{CC} = Min		2.0			V
V_{IL}	Logical "0" Input Voltage	V_{CC} = Min				0.8	V
V_{OH}	Logical "1" Output Voltage	V_{CC} = Min, I_O = −2 mA		2.4			V
V_{OL}	Logical "0" Output Voltage	V_{CC} = Min, I_O = 12 mA				0.4	V
I_{OZ}	TRI-STATE Output Current	V_{CC} = Max	V_O = 2.4V			40	μA
			V_O = 0.4V			−40	
I_{IH}	Logical "1" Input Current	V_{CC} = Max	V_{IN} = 2.4V			40	μA
			V_{IN} = 5.5V			1	mA
I_{IL}	Logical "0" Input Current	V_{CC} = Max, V_{IN} = 0.4V				−1.0	mA
I_{OS}	Output Short Circuit Current	V_{CC} = Max, V_O = 0V, (Note 3)		−15		−70	mA
I_{CC}	Supply Current	V_{CC} = Max, Inputs Grounded			106	170	mA
V_{IC}	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −12 mA				−1.5	V

switching characteristics (Note 2)

PARAMETER		PARAMETER CONDITIONS	TEST CONDITIONS	DM7596,DM7796			DM8596,DM8796			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Propagation Delay Time, Low to High Level Output	Access Time from Address	C_L = 50 pF, R_L = 400Ω		80	150		80	120	ns
t_{PHL}	Propagation Delay Time, High to Low Level Output	Access Time from Address			80	150		80	120	ns
t_{ZH}	Output Enable Time to High Level	Access Times from Memory Enables			40	120		40	90	ns
t_{ZL}	Output Enable Time to Low Level	Access Times from Memory Enables			60	120		60	90	ns
t_{HZ}	Output Disable Time from High Level	Disable Times from Memory Enables	C_L = 5.0 pF, R_L = 400Ω		20	70		20	50	ns
t_{LZ}	Output Disable Time from Low Level	Disable Times from Memory Enables			25	70		25	50	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DM7596 and DM7796 and across the 0°C to 70°C range for the DM8596 and DM8796. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

Note 3: Only one output at a time should be shorted.

80-column card program data format

Col. 1-3: 3 Character ID code any 3 Alpha-Numeric characters. Must be the same on all cards associated with a particular pattern, but different for the ID code used on other patterns. The purpose of this code is to prevent mixing of cards.

Col. 4: (Blank)

Col. 5-12: Word Data. Order is 08 (most significant) to 01 (least significant). Note 1. Characters—For TTL high level are: H or 1. Characters—For TTL low are L or 0. "Don't Care" is X.

Col. 13: (Blank)

Col. 14-21: Word Data—same format as 5-12.

Col. 22: (Blank)

Col. 23–30: Word Data

Col. 31: (Blank)

Col. 32-39: Word Data

Col. 40: (Blank)

Col. 41-48: Word Data

Col. 49: (Blank)

Col. 50-57: Word Data

Col. 58: (Blank)

Col. 59-66: Word Data

Col. 67: (Blank)

Col. 68-75: Word Data

Col. 76-78: (Blank)

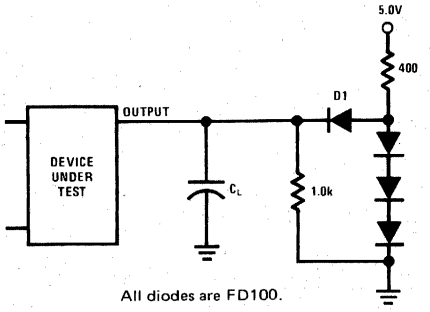
Col. 79-80: Card sequence number. 1 to 64. Leading zeros may be punched or suppressed. (Note 2)

Note 1: The words are listed in sequence beginning on the first card with the word associated with address 0 and ending on the last card with the word associated with address 511. Address input A_8 is the most significant; A_0, the least significant.

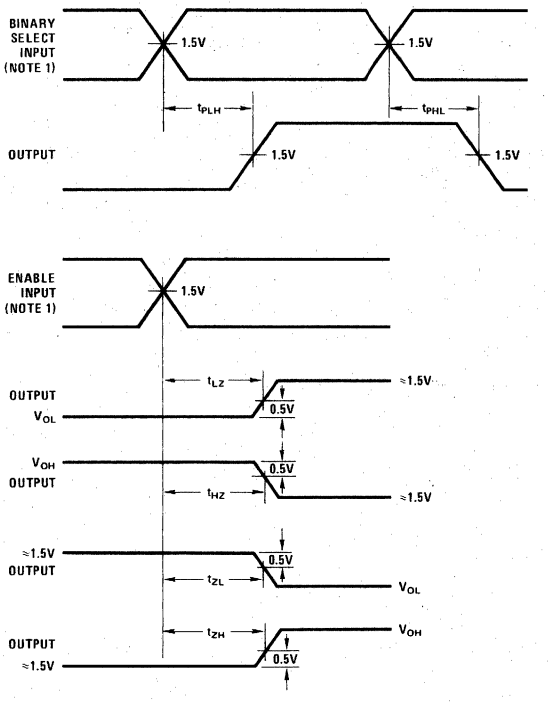
Note 2: Card sequence numbers reference a specific group of 8 words, i.e.;

Card 01: Word address 0 to 7
Card 02: Word address 8 to 15
Card 03: Word address 16 to 23
. .
. .
. .
Card 64: Word address 504 to 511

ac test circuit and switching time waveforms



All diodes are FD100.



Note 1: Input waveforms are supplied by pulse generators having the following characteristics:
$t_r \leq 10$ ns, $t_f \leq 10$ ns, PRR = 1 MHz, PDC = 50%, Amplitude = 3.0V, and $Z_O = 50\Omega$.

NATIONAL

Bipolar ROMs

DM7597/DM8597 TRI-STATE® 1024-bit read only memory

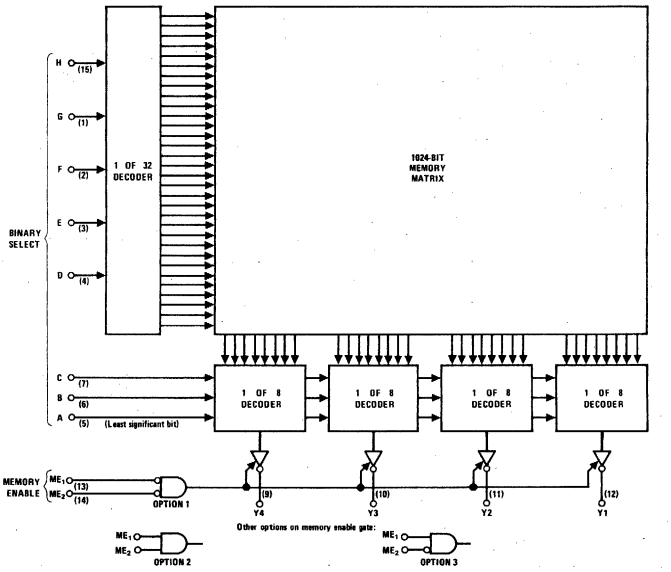
general description

The DM7597/DM8597 is a custom-programmed read-only memory organized as 256 four-bit words. Selection of the proper word is accomplished through the eight select inputs. Two overriding memory enable inputs are provided, which when mask-programmed in one of three options described will cause all four outputs to either read the normal memory contents or go to the "high impedance" state. In this state both the upper and lower output transistors are turned off. The outputs may therefore be paralleled to increase word capacity; since in the high-impedance state they present only a minimal load to the active output.

features

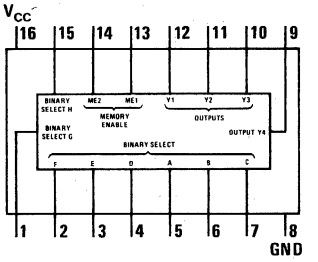
- Pin compatible with SN54187/SN74187
- 35 ns typical delay from address to output
- Can be expanded to 32,768 4-bit words by simple paralleling of outputs
- Programmable memory enable inputs

logic diagram



connection diagram

Dual-In-Line Package



TOP VIEW

Order Number DM7597J or DM8597J — **See Package 10**

Order Number DM8597N — **See Package 15**

truth table

TABLE of Programmable Memory Enable Options

OPTION	ME1	ME2	OUTPUTS
1	0	0	Normal
	1	X	HIGH Impedance
	X	1	HIGH Impedance
2	1	1	Normal
	0	X	HIGH Impedance
	X	0	HIGH Impedance
3	1	0	Normal
	X	1	HIGH Impedance
	0	X	HIGH Impedance

X = don't care

absolute maximum ratings (Note 1)

Supply Voltage		7V
Input Voltage		5.5V
Output Voltage		5.5V
Operating Temperature Range	DM7597	−55°C to +125°C
	DM8597	0°C to +70°C
Storage Temperature Range		−65°C to +150°C
Lead Temperature (Soldering, 10 sec)		300°C

electrical characteristics (Note 2)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	DM7597	V_{CC} = 4.5V		2.0			V
	DM8597	V_{CC} = 4.75V					
Logical "0" Input Voltage	DM7597	V_{CC} = 4.5V				0.8	V
	DM8597	V_{CC} = 4.75V					
Logical "1" Output Voltage	DM7597	V_{CC} = 4.5V	I_O = −2 mA	2.4			V
	DM8597	V_{CC} = 4.75V	I_O = −5.2 mA				
Logical "0" Output Voltage	DM7597	V_{CC} = 4.5V	I_O = 16 mA			0.4	V
	DM8597	V_{CC} = 4.75V					
Third State Output Current	DM7597	V_{CC} = 5.5V	V_O = 2.4V			40	μA
	DM8597	V_{CC} = 5.25V	V_O = 0.4V			−40	μA
Logical "1" Input Current	DM7597	V_{CC} = 5.5V	V_{IN} = 2.4V			40	μA
	DM8597	V_{CC} = 5.25V					
Logical "0" Input Current	DM7597	V_{CC} = 5.5V	V_{IN} = 5.5V			1.0	mA
	DM8597	V_{CC} = 5.25V					
	DM7597	V_{CC} = 5.5V	V_{IN} = 0.4V			−1.0	mA
	DM8597	V_{CC} = 5.25V					
Output Short Circuit Current (Note 3)	DM7597	V_{CC} = 5.5V	V_O = 0.0V	−20		−70	mA
	DM8597	V_{CC} = 5.25V					
Supply Current	DM7597	V_{CC} = 5.5V	All Inputs at GND		75	110	mA
	DM8597	V_{CC} = 5.25V					
Input Clamp Voltage	DM7597	V_{CC} = 4.5V	I_{IN} = −12 mA			−1.5	V
	DM8597	V_{CC} = 4.75V					
Propagation Delay to a Logical "0" from Address to Output, t_{pd0}		V_{CC} = 5.0V T_A = 25°C			39	60	ns
Propagation Delay to a Logical "1" from Address to Output, t_{pd1}		V_{CC} = 5.0V T_A = 25°C			31	60	ns
Delay from Enable to High Impedance State (from Logical "1" Level), t_{1H}		V_{CC} = 5.0V T_A = 25°C			13	30	ns
Delay from Enable to High Impedance State (from Logical "0" Level), t_{0H}		V_{CC} = 5.0V T_A = 25°C			16	30	ns
Delay from Enable to Logical "1" Level (from High Impedance State), t_{H1}		V_{CC} = 5.0V T_A = 25°C			18	30	ns
Delay from Enable to Logical "0" Level (from High Impedance State), t_{H0}		V_{CC} = 5.0V T_A = 25°C			20	30	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DM7597 and across the 0°C to 70°C range for the DM8597. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

Note 3: Only one output at a time should be shorted.

ordering instructions

Programming instructions for the DM7597 or DM8597 are solicited in the form of a sequenced deck of 32 standard 80-column data cards providing the information requested under data card format, accompanied by a properly sequenced listing of these cards, and the supplementary ordering data. Upon receipt of these items, a computer run will be made from the deck of cards which will produce a complete truth table of the requested part. This truth table, showing output conditions for each of the 256 words, will be forwarded to the purchaser as verification of the input data as interpreted by the computer-automated design (CAD) program. This single run also generates mask and test program data; therefore, verification of the truth table should be completed promptly.

Each card in the data deck prepared by the purchaser identifies the eight words specified and describes the conditions at the four outputs for each of the eight words. All addresses must have all outputs defined and columns designated as "blank" must not be punched. Cards should be punched according to the data card format shown.

supplementary ordering data

Submit the following information with the data cards:

a) Customer's name and address
b) Customer's purchase order number
c) Customer's drawing number.

data card format

Column

1- 3 Punch a right-justified integer representing the binary input address (000-248) for the first set of outputs described on the card.

4 Punch a "–" (Minus sign)

5- 7 Punch a right-justified integer representing the binary input address (007-255) for the last set of outputs described on the card.

8- 9 Blank

10-13 Punch "H", "L", or "X" for bits four, three, two, and one (outputs Y4, Y3, Y2, and Y1 in that order) for the first set of outputs specified on the card. H = high-level output, L = low-level output, X = output irrelevant.

14 Blank

15-18 Punch "H", "L", or "X" for the second set of outputs.

19 Blank

20-23 Punch "H", "L", or "X" for the third set of outputs.

24 Blank

25-28 Punch "H", "L", or "X" for the fourth set of outputs.

29 Blank

30-33 Punch "H", "L", or "X" for the fifth set of outputs.

34 Blank

35-38 Punch "H", "L", or "X" for the sixth set of outputs.

39 Blank

40-43 Punch "H", "L", or "X" for the seventh set of outputs.

44 Blank

45-48 Punch "H", "L", or "X" for the eighth set of outputs.

49 Blank

50-51 Punch a right-justified integer representing the current calendar day of the month.

52 Blank

53-55 Punch an alphabetic abbreviation representing the current month.

56 Blank

57-58 Punch the last two digits of the current year.

59 Blank

60-61 Punch "DM"

62-65 Punch 7597 or 8597

66-70 Blank

71 Punch 1, 2, or 3 for memory enable option desired (assumed 1 if not punched).

Bipolar ROMs

DM7598/DM8598 TRI-STATE® 256-bit read only memory

general description

The DM7598/DM8598 is a customer programmed 256-bit read only memory, organized as 32 8-bit words. A 5-bit input code selects the appropriate word which then appears on the eight outputs. An enable input overrides the select inputs and blanks all outputs.

Although the DM7598/DM8598 can have its outputs tied together for word-expansion, the outputs are not open-collector, but rather the familiar totem-pole output with the capability of being placed in a "third-state." This unique TRI-STATE concept allows outputs to be tied together and then connected to a common bus line. Normal TTL outputs cannot be connected due to the low-impedance logical "1" output current which one device would have to sink from the other. If, however, on all but one of the connected devices both the upper and lower output transistors are turned "OFF," then the one remaining device in the normal low impedance state will have to supply to or sink from the other devices only a small amount of leakage current. This is exactly what occurs on the DM7598/DM8598.

A typical system connection demonstrating expansion to greater numbers of words is shown in *Figure 1*. While it is true that in a TTL system open-collector gates could be used to perform the logic function of these three-state elements, neither waveform integrity nor optimum speed would be achieved. The low output impedance of the DM7598/DM8598 provides good capacitance drive capability and rapid transition from the logical "0" to logical "1" level thus assuring both speed and waveform integrity.

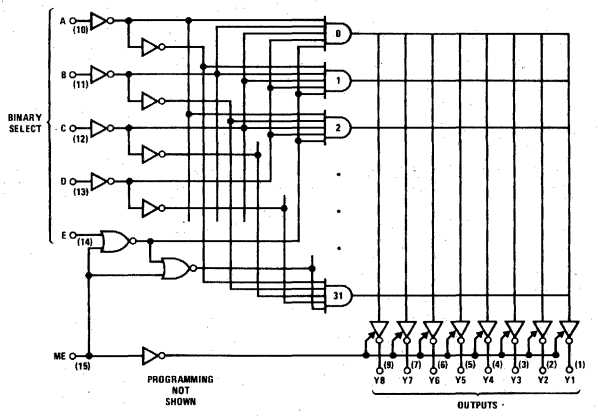
It is possible to connect as many as 128 DM8598s to a common bus line and still have adequate drive capability to allow fan-out from the bus. The example shown in *Figure 2* indicates how this guarantee can be made under worst-case conditions.

Figure 3 indicates how multiple packages can be used to increase word length.

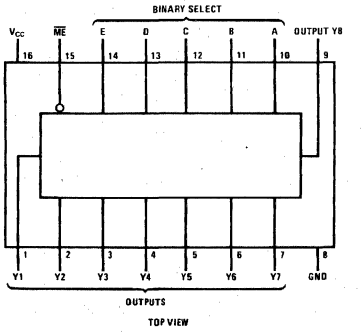
features

- Pin compatible with SN5488/SN7488
- Organized as 32 8-bit words
- Full internal decoding
- 26 ns typical access time
- 350 mW typical power dissipation
- Input clamp diodes
- Designed for bus-organized systems

logic and connection diagrams



Dual-In-Line Package



Order Number DM7598J or DM8598J
See Package 10
Order Number DM8598N
See Package 15

absolute maximum ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Output Voltage	5.5V
Operating Temperature Range	
DM7598	−55°C to +125°C
DM8598	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage, V_{CC}			
DM7598	4.5	5.5	V
DM8598	4.75	5.25	V
Temperature, T_A			
DM7598	−55	+125	°C
DM8598	0	+70	°C

electrical characteristics (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	Logical "1" Input Voltage	V_{CC} = Min		2.0			V
V_{IL}	Logical "0" Input Voltage	V_{CC} = Min				0.8	V
V_{OH}	Logical "1" Output Voltage	V_{CC} = Min	I_O = −2 mA, DM7598	2.4			V
			I_O = −5.2 mA, DM8598	2.4			
V_{OL}	Logical "0" Output Voltage	V_{CC} = Min, I_O = 12 mA				0.4	V
I_{OZ}	TRI-STATE Output Current	V_{CC} = Max	V_O = 2.4V			40	μA
			V_O = 0.4V			−40	
I_{IH}	Logical "1" Input Current	V_{CC} = Max	V_{IN} = 2.4V			25	μA
			V_{IN} = 5.5V			1	mA
I_{IL}	Logical "0" Input Current	V_{CC} = Max, V_{IN} = 0.4V				−1.0	mA
I_{OS}	Output Short Circuit Current	V_{CC} = Max, V_O = 0V, (Note 3)		−20		−70	mA
I_{CC}	Supply Current	V_{CC} = Max, Inputs Grounded			70	99	mA
V_{IC}	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −12 mA				−1.5	V

switching characteristics (Note 2)

SYMBOL	PARAMETER	PARAMETER CONDITIONS	TEST CONDITIONS	DM7598			DM8598			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Propagation Delay Time, Low to High Level Output	Access Time from Address			23	65		23	50	ns
t_{PHL}	Propagation Delay Time, High to Low Level Output	Access Time from Address	C_L = 50 pF, R_L = 400Ω		29	65		29	50	ns
t_{ZH}	Output Enable Time to High Level	Access Times from Memory Enable			16	40		16	30	ns
t_{ZL}	Output Enable Time to Low Level	Access Times from Memory Enable			20	40		20	30	ns
t_{HZ}	Output Disable Time from High Level	Disable Times from Memory Enable	C_L = 5.0 pF, R_L = 400Ω		10	30		10	20	ns
t_{LZ}	Output Disable Time from Low Level	Disable Times from Memory Enable			22	45		22	40	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DM7598 and across the 0°C to +70°C range for the DM8598. All typicals are given for V_{CC} = 5.0V, and T_A = 25°C.

Note 3: Only one output at a time should be shorted.

typical applications

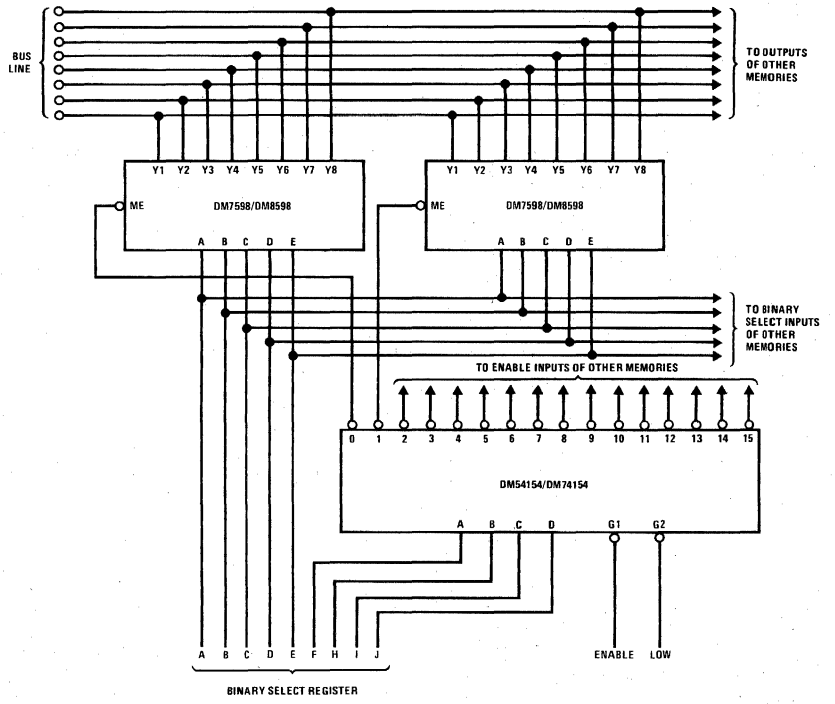


FIGURE 1. Expansion to Larger Word Capacity

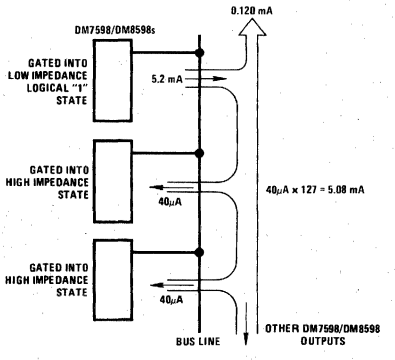


FIGURE 2.

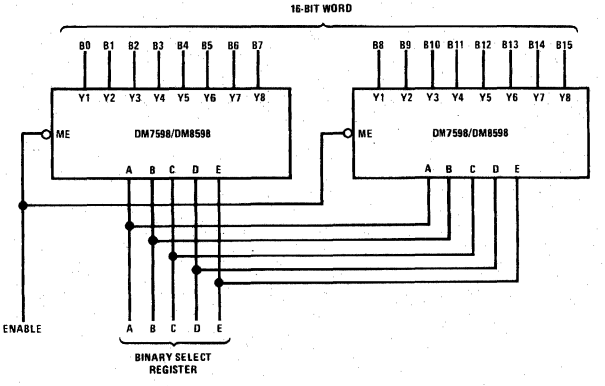


FIGURE 3.

truth table/order blank

A special pattern has been generated for the DM7598/DM8598. The AA pattern provides a sine table. The 5-bit input code linearly divides 90° into 32 equal segments. Each 8-bit output is therefore the sine of the angle applied.

EXAMPLE: Input 11010 means 26/32 of 90°, or about 73°. The corresponding output 1110100 indicates (1/2 + 1/4 + 1/8 + 1/16 + 1/64) or about 0.95, which is close to the sine of 73°. Rounding-off has not been employed, since without rounding-off it is possible to extend the accuracy with additional ROMs.

	INPUTS						OUTPUTS							
WORD	BINARY SELECT					ENABLE								
	E	D	C	B	A	ME	Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	1	0	0	0	0	0	1	1	0	0
2	0	0	0	1	0	0	0	0	0	1	1	0	0	1
3	0	0	0	1	1	0	0	0	1	0	0	1	0	1
4	0	0	1	0	0	0	0	0	1	1	0	0	0	1
5	0	0	1	0	1	0	0	0	1	1	1	1	1	0
6	0	0	1	1	0	0	0	1	0	0	1	0	1	0
7	0	0	1	1	1	0	0	1	0	1	0	1	1	0
8	0	1	0	0	0	0	0	1	1	0	0	0	0	1
9	0	1	0	0	1	0	0	1	1	0	1	1	0	1
10	0	1	0	1	0	0	0	1	1	1	1	0	0	0
11	0	1	0	1	1	0	1	0	0	0	0	0	1	1
12	0	1	1	0	0	0	1	0	0	0	1	1	1	0
13	0	1	1	0	1	0	1	0	0	1	1	0	0	0
14	0	1	1	1	0	0	1	0	1	0	0	0	1	0
15	0	1	1	1	1	0	1	0	1	0	1	0	1	1
16	1	0	0	0	0	0	1	0	1	1	0	1	0	1
17	1	0	0	0	1	0	1	0	1	1	1	1	0	1
18	1	0	0	1	0	0	1	1	0	0	0	1	0	1
19	1	0	0	1	1	0	1	1	0	0	1	1	0	1
20	1	0	1	0	0	0	1	1	0	1	0	1	0	0
21	1	0	1	0	1	0	1	1	0	1	1	0	1	1
22	1	0	1	1	0	0	1	1	1	0	0	0	0	1
23	1	0	1	1	1	0	1	1	1	0	0	1	1	1
24	1	1	0	0	0	0	1	1	1	0	1	1	0	0
25	1	1	0	0	1	0	1	1	1	1	0	0	0	1
26	1	1	0	1	0	0	1	1	1	1	0	1	0	0
27	1	1	0	1	1	0	1	1	1	1	1	0	0	0
28	1	1	1	0	0	0	1	1	1	1	1	0	1	1
29	1	1	1	0	1	0	1	1	1	1	1	1	0	1
30	1	1	1	1	0	0	1	1	1	1	1	1	1	0
31	1	1	1	1	1	0	1	1	1	1	1	1	1	1
All	X	X	X	X	X	1	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z

X = Don't Care

The output levels are not shown on the truth table since the customer specifies the output condition he desires at each of the eight outputs for each of the 32 words (256 bits). The customer does this by filling out the Truth Table on this data sheet, and sending it in with his purchase order.

	INPUTS						OUTPUTS							
WORD	BINARY SELECT					ENABLE								
	E	D	C	B	A	ME	Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1
0	0	0	0	0	0	0								
1	0	0	0	0	1	0								
2	0	0	0	1	0	0								
3	0	0	0	1	1	0								
4	0	0	1	0	0	0								
5	0	0	1	0	1	0								
6	0	0	1	1	0	0								
7	0	0	1	1	1	0								
8	0	1	0	0	0	0								
9	0	1	0	0	1	0								
10	0	1	0	1	0	0								
11	0	1	0	1	1	0								
12	0	1	1	0	0	0								
13	0	1	1	0	1	0								
14	0	1	1	1	0	0								
15	0	1	1	1	1	0								
16	1	0	0	0	0	0								
17	1	0	0	0	1	0								
18	1	0	0	1	0	0								
19	1	0	0	1	1	0								
20	1	0	1	0	0	0								
21	1	0	1	0	1	0								
22	1	0	1	1	0	0								
23	1	0	1	1	1	0								
24	1	1	0	0	0	0								
25	1	1	0	0	1	0								
26	1	1	0	1	0	0								
27	1	1	0	1	1	0								
28	1	1	1	0	0	0								
29	1	1	1	0	1	0								
30	1	1	1	1	0	0								
31	1	1	1	1	1	0								
All	X	X	X	X	X	1	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z

X = Don't Care

Notice: This sheet must be completed and signed by an authorized representative of the customer's company before an order can be entered.

To be used by National only

_____ Part Number

_____ S.O. Number

_____ Date Received

_____ _____

Authorized Representative Date

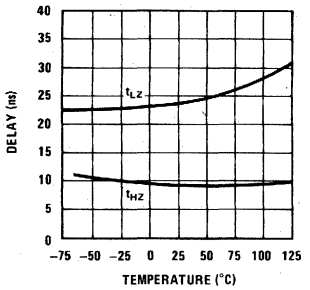
_____

Company

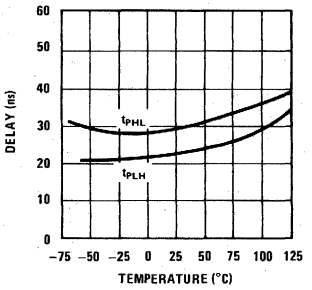
Desired Part ☐ DM7598 ☐ DM8598

typical performance characteristics

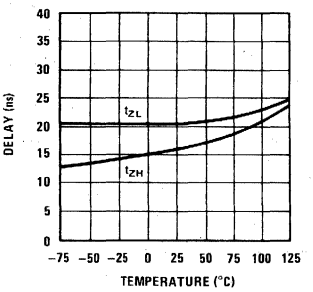
Delay from Enable to High Impedance State



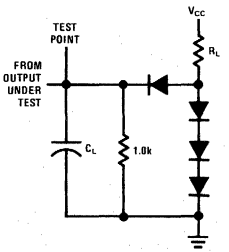
Delay from Address to Output



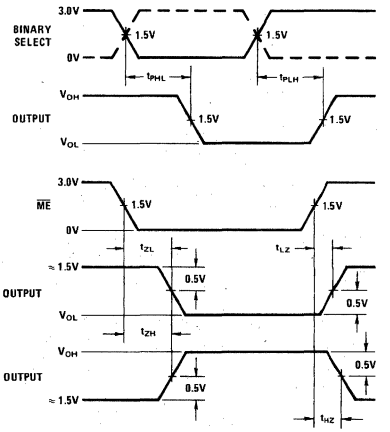
Delay from Enable to Low Impedance State



ac test circuit and switching time waveforms



C_L includes probe and jig capacitance.
All diodes are 1N3064.



Note: Input waveforms are supplied by pulse generators having the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, PRR ≤ 1.0 MHz and $Z_{OUT} \approx 50\Omega$.

ordering instructions

Programming instructions for the DM7598/DM8598 are solicited in the form of a sequenced deck of 32 standard 80-column data cards providing the information requested under "data card format," accompanied by a properly sequenced listing of these cards, and the supplementary ordering data. Upon receipt of these items, a computer run will be made from the deck of cards which will produce a complete function table of the requested part. This function table, showing output conditions for each of the 32 words, will be forwarded to the purchaser as verification of the input data as interpreted by the computer-automated design (CAD) program. This single run also generates mask and test program data; therefore, verification of the function table should be completed promptly.

Each card in the data deck prepared by the purchaser identifies the word specified and describes the levels at the eight outputs for that word. All addresses must have all outputs defined and columns designated as "blank" must not be punched. Cards should be punched according to the data card format shown.

ordering instructions (con't)

SUPPLEMENTARY ORDERING DATA

Submit the following information with the data cards:

a) Customer's name and address
b) Customer's purchase order number
c) Customer's drawing number

The following information will be furnished to the customer:
a) National's part number
b) National's sales order number
c) Date received

DATA CARD FORMAT

Col. 1–2: Punch a right-justified integer representing the positive-logic binary input address (00–31) for the word described on the card.

Col. 3–4: Blank

Col. 5: Punch "H" or "L" for output Y8. H = high-voltage level output, L = low-voltage level output.

Col. 6–9: Blank

Col. 10: Punch "H" or "L" for output Y7.

Col. 11–14: Blank

Col. 15: Punch "H" or "L" for output Y6.

Col. 16–19: Blank

Col. 20: Punch "H" or "L" for output Y5.

Col. 21–24: Blank

Col. 25: Punch "H" or "L" for output Y4.

Col. 26–29: Blank

Col. 30: Punch "H" or "L" for output Y3.

Col. 31–34: Blank

Col. 35: Punch "H" or "L" for output Y2.

Col. 36–39: Blank

Col. 40: Punch "H" or "L" for output Y1.

Col. 41–49: Blank

Col. 50–51: Punch a right-justified integer representing the current calendar day of the month.

Col. 52: Blank

Col. 53–55: Punch an alphabetic abbreviation representing the current month.

Col. 56: Blank

Col. 57–58: Punch the last two digits of the current year.

Col. 59: Blank

Col. 60–61: Punch "DM,"

Col. 62–66: Punch "7598" or "8598."

Col. 67–68: Blank

Col. 69–80: These columns may be used for any customer information or identification.

NATIONAL

Bipolar ROMs
Advance Information

DM75S202/DM85S202 TRI-STATE® 2048-bit ROM with output latches

general description

These TTL compatible memories are organized as 256 words by 8 bits. When the strobe input is at a logical "1" level the memories function in the conventional manner with the enable input determining whether the outputs present the contents selected by the address inputs or are turned "OFF."

When the strobe input is at a logical "0" the outputs are latched into the state they were in just prior to the strobe going low. The outputs remain in this condition until the strobe is again taken to the logical "1" state regardless of the state of the address or enable inputs.

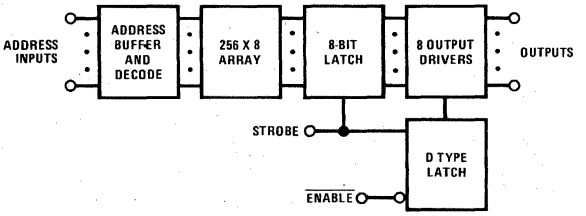
features

- Schottky clamped for high speed systems
- High speed

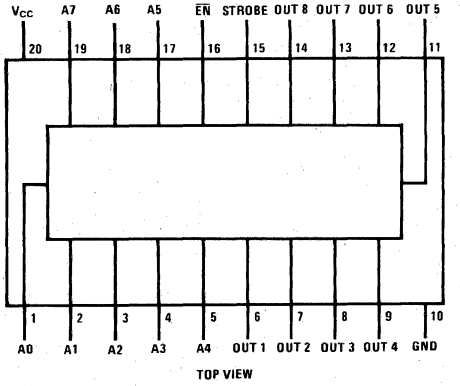
Address to output delay	35 ns
Enable to output delay	15 ns
Strobe to output delay	20 ns

- PNP inputs reduce input loading
- Output latches simplify system use
- 20 pin, 300 mil package for high density
- Pin compatible with DM54S271/DM54S371

logic and connection diagrams



Dual-In-Line Package



TOP VIEW

Order Number DM85S202N
See Package 16A

absolute maximum ratings (Note 1)

Supply Voltage (Note 2)	−0.5V to +7.0V
Input Voltage (Note 2)	−1.2V to +5.5V
Output Voltage (Note 2)	−0.5V to +5.5V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DM75S202	4.5	5.5	V
DM85S202	4.75	5.25	V
Ambient Temperature (T_A)			
DM75S202	−55	+125	°C
DM85S202	0	+70	°C
Logical "0" Input Voltage	0	0.8	V
Logical "1" Input Voltage	2.0	5.5	V

dc electrical characteristics (Note 2)

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I_{IH}	Logical "1" Input Current	V_{IN} = 2.7V			25	μA
		V_{IN} = 5.5V			1.0	mA
I_{IL}	Logical "0" Input Current	V_{IN} = 0.45V			−250	μA
V_{CL}	Input Clamp Voltage	I_{IN} = −18 mA			−1.2	V
V_{OL}	Logical "0" Output Voltage					
	DM75S202	I_{OL} = 12 mA			0.50	V
	DM85S202				0.45	V
V_{OH}	Logical "1" Output Voltage					
	DM75S202	I_{OH} = −2.0 mA	2.4			V
	DM85S202	I_{OH} = −6.5 mA	2.4			V
I_{OS}	Output Short Circuit Current	V_O = 0V (Note 3) V_{CC} = Max	−30		−100	mA
I_{OZ}	TRI-STATE Output Current	0.45V ≤ V_O ≤ 2.4V	−50		50	μA
I_{CC}	Maximum Supply Current			100	165	mA

switching characteristics (Note 2)

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{AA}	Address to Output Delay	Strobe = "1"		35		ns
t_{EA}	Time to Enable Output	Strobe = "1"		15		ns
t_{ED}	Time to Disable Output	Strobe = "1"		15		ns
t_{SA}	Strobe to Output Delay			20		ns
t_{SW}	Strobe Pulse Width			10		ns

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at these limits.

Note 2: These limits apply over the entire operating range unless stated otherwise. All typical values are for V_{CC} = 5.0V and T_A = 25°C.

Note 3: During I_{OS} measurement, only one output at a time should be grounded. Permanent damage may otherwise result.

NATIONAL

Bipolar ROMs

Advance Information

DM7678/DM8678, DM7679/DM8679 7×9 character generator

general description

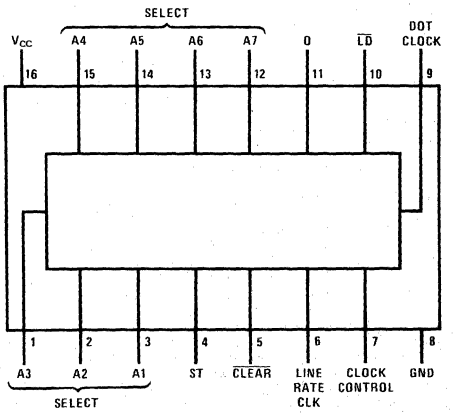
The DM7678/8678 and DM7679/DM8679 are bipolar character generators. A maximum of 64 characters can be displayed in a 7X9 dot matrix. Shifted characters can be generated by the on-chip subtractor. On-chip line counter and parallel-in-serial-out shift register reduce package pin-out.

The clear input and the load input are active low. $\overline{\text{Load}}$ is synchronous with the Dot Rate Clock. Both the line rate clock and the dot rate clock are positive triggered. When the strobe input receives a low signal, the character address will be held at the inputs.

features

- TRI-STATE output
- On-chip input latches
- On-chip line counter
- On-chip shift register
- Serial output
- 20 MHz typical clock rate
- Shifted characters

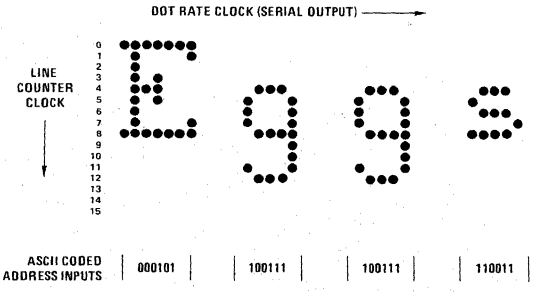
connection diagram



Order Number DM7678J, DM7679J, DM8678J or DM8679J
See Package 10

Order Number DM8678N or DM8679N
See Package 15

character display example



electrical characteristics

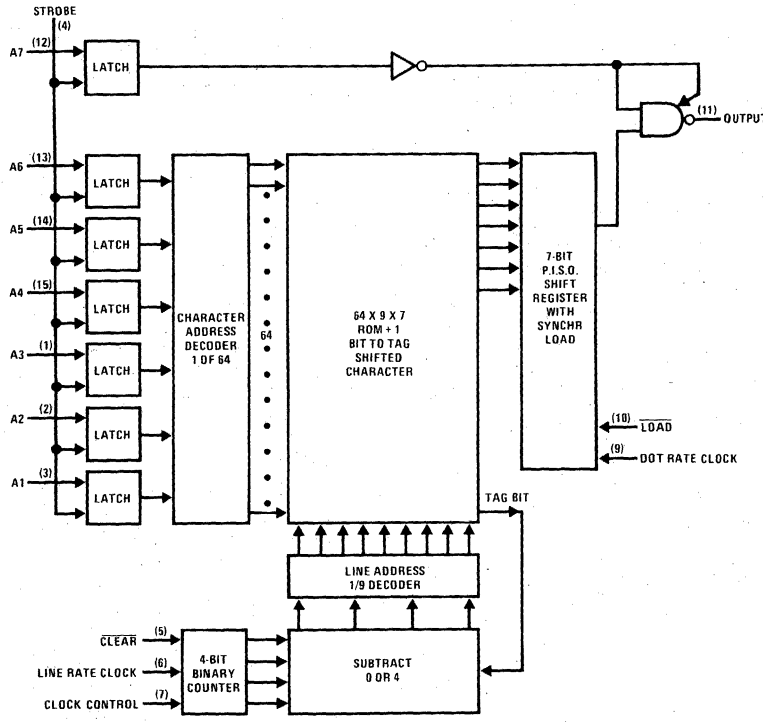
over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		CONDITIONS	DM76/86 78, 79 MIN	DM76/86 78, 79 TYP(1)	DM76/86 78, 79 MAX	UNITS
V_{OH}	High Level Output Voltage	I_{OH} = 2 mA, V_{CC} = Min	2.4			V
V_{OL}	Low Level Output Voltage	I_{OL} = 16 mA, V_{CC} = Min			0.4	V
I_{IH}	High Level Input Current	V_{CC} = Max, V_{IN} = 2.4V			40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_{IN} = 0.4V			−0.8	mA
I_{CC}	Supply Current	V_{CC} = Max		100		mA
f_{MAX}	Maximum Clock Frequency	V_{CC} = 5V, T_A = 25°C		20		MHz

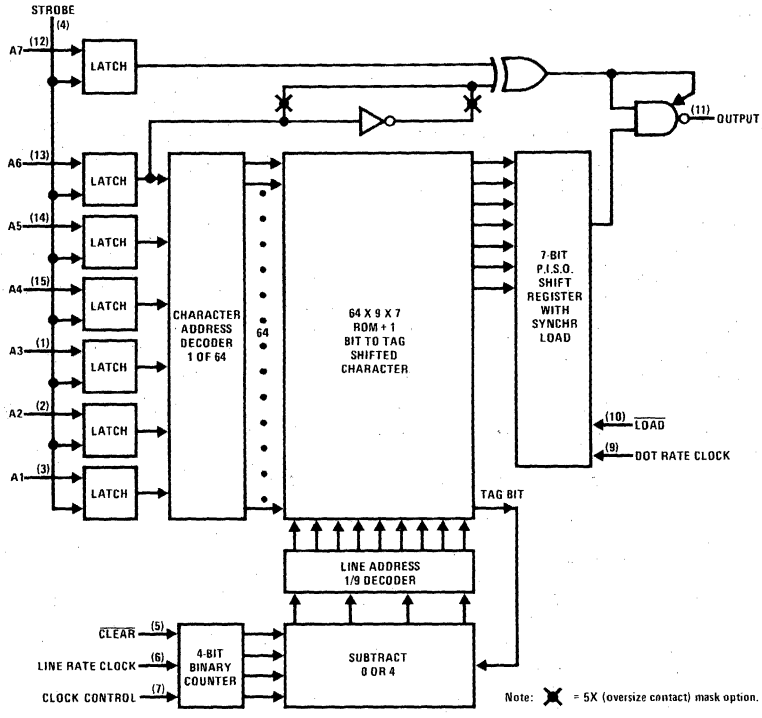
Notes:
(1) All typical values are at V_{CC} = 5V, T_A = 25°C

logic diagrams

DM7678/DM8678



DM7679/DM8679



Bipolar ROMs

DM76L97/DM86L97 TRI-STATE® low power 1024-bit read only memory

general description

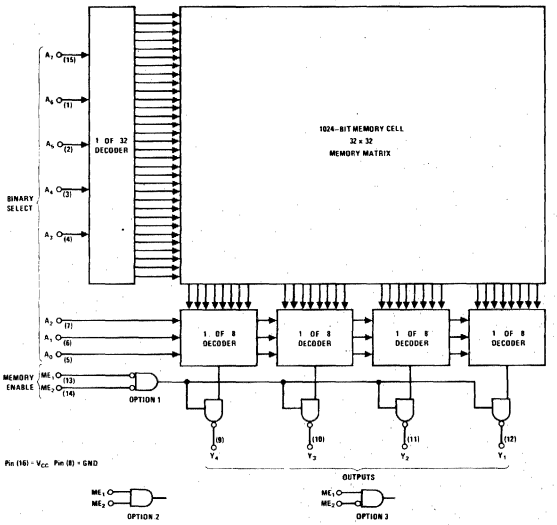
The DM76L97/DM86L97 is a custom-programmed Read Only Memory organized as 256 four-bit words. Selection of the proper word is accomplished through the eight select inputs.

Two overriding memory enable inputs are provided which when mask-programmed in one of the three options described will cause all four outputs to read either the normal memory contents or go to the high impedance state.

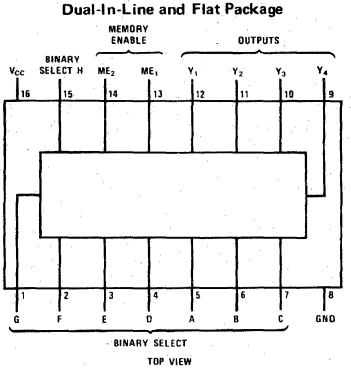
features

- Full tenth-power technology
- Pin compatible with SN54187/SN74187
- Typical power dissipation 75 mW
- Typical access time 70 ns
- Custom-programmed memory enable inputs
- TRI-STATE outputs

logic and connection diagrams



Dual-In-Line and Flat Package



Order Number DM76L97J or DM86L97J
See Package 10

Order Number DM76L97N or DM86L97N
See Package 15

Order Number DM76L97W or DM86L97W
See Package 28

absolute maximum ratings (Note 1)

Supply Voltage	7.0V
Input Voltage	5.5V
Output Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DM76L97	4.5	5.5	V
DM86L97	4.75	5.25	V
Temperature (T_A)			
DM76L97	−55	+125	°C
DM86L97	0	+70	°C

electrical characteristics (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	V_{CC} = Min	2.0			V
Logical "0" Input Voltage	V_{CC} = Min			0.7	V
Logical "1" Output Voltage	V_{CC} = Min, I_O = −1.0 mA	2.4			V
Logical "0" Output Voltage					
DM76L97	V_{CC} = Min, I_O = 2.0 mA			0.3	V
DM86L97	V_{CC} = Min, I_O = 3.2 mA			0.4	V
Third State Output Current					
DM76L97	V_{CC} = Max, V_O = 2.4V			±40	μA
DM86L97	V_{CC} = Max, V_O = 0.4V			±40	μA
Logical "1" Input Current	V_{CC} = Max, V_{IN} = 2.4V			10	μA
	V_{CC} = Max, V_{IN} = 5.5V			100	μA
Logical "0" Input Current	V_{CC} = Max, V_{IN} = 0.3V			−180	μA
Output Short Circuit Current (Note 3)	V_{CC} = Max, V_O = 0V	−6.0		−30	mA
Supply Current	V_{CC} = Max, All Inputs at GND		15	20	mA
Third State Output Current	V_{CC} = Max, V_{OUT} = 2.4V			+40	μA
	V_{CC} = Max, V_{OUT} = 0.4V			−40	μA
Input Clamp Voltage	V_{CC} = Min, I_{IN} = −12 mA			−1.5	V
Propagation Delay to a Logical "0" From Address to Output (t_{pd0})	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C		55	85	ns
Propagation Delay to a Logical "1" From Address to Output (t_{pd1})	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C		86	130	ns
Delay From Enable to High Impedance State (From Logical "1" Level) (t_{1H})	V_{CC} = 5.0V, C_L = 5.0 pF, T_A = 25°C		15	23	ns
Delay From Enable to High Impedance State (From Logical "0" Level) (t_{0H})	V_{CC} = 5.0V, C_L = 5.0 pF, T_A = 25°C		57	86	ns
Delay From Enable to Logical "1" Level (From High Impedance State) (t_{H1})	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C		34	51	ns
Delay From Enable to Logical "0" Level (From High Impedance State) (t_{H0})	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C		47	70	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DM76L97 and across the 0°C to +70°C range for the DM86L97. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

Note 3: Only one output at a time should be shorted.

ordering instructions

Programming instructions for the DM76L97 or DM86L97 are solicited in the form of a sequenced deck of 32 standard 80-column data cards providing the information requested under data card format, accompanied by a properly sequenced listing of these cards, and the supplementary ordering data. Upon receipt of these items, a computer run will be made from the deck of cards which will produce a complete truth table of the requested part. This truth table, showing output conditions for each of the 256 words, will be forwarded to the purchaser as verification of the input data as interpreted by the computer-automated design (CAD) program. This single run also generates mask and test program data; therefore, verification of the truth table should be completed promptly.

Each card in the data deck prepared by the purchaser identifies the eight words specified and describes the conditions at the four outputs for each of the eight words. All addresses must have all outputs defined and columns designated as "blank" must not be punched. Cards should be punched according to the data card format shown.

supplementary ordering data

Submit the following information with the data cards:

a) Customer's name and address
b) Customer's purchase order number
c) Customer's drawing number.

data card format

Column

1- 3 Punch a right-justified integer representing the binary input address (000-248) for the first set of outputs described on the card.

4 Punch a "–" (Minus sign)

5- 7 Punch a right-justified integer representing the binary input address (007-255) for the last set of outputs described on the card.

8- 9 Blank

10-13 Punch "H", "L", or "X" for bits four, three, two, and one (outputs Y4, Y3, Y2, and Y1 in that order) for the first set of outputs specified on the card. H = high-level output, L = low-level output, X = output irrelevant.

14 Blank

15-18 Punch "H", "L", or "X" for the second set of outputs.

19 Blank

20-23 Punch "H", "L", or "X" for the third set of outputs.

24 Blank

25-28 Punch "H", "L", or "X" for the fourth set of outputs.

29 Blank

30-33 Punch "H", "L", or "X" for the fifth set of outputs.

34 Blank

35-38 Punch "H", "L", or "X" for the sixth set of outputs.

39 Blank

40-43 Punch "H", "L", or "X" for the seventh set of outputs.

44 Blank

45-48 Punch "H", "L", or "X" for the eighth set of outputs.

49 Blank

50-51 Punch a right-justified integer representing the current calendar day of the month.

52 Blank

53-55 Punch an alphabetic abbreviation representing the current month.

56 Blank

57-58 Punch the last two digits of the current year.

59 Blank

60-61 Punch "DM"

62-67 Punch the National Semiconductor part number DM76L97 or DM86L97.

68-70 Blank

truth table

OPTION	ME_1	ME_2	OUTPUTS
1	0	0	Normal
	1	X	High Impedance
	X	1	High Impedance
2	1	1	Normal
	0	X	High Impedance
	X	0	High Impedance
3	1	0	Normal
	X	1	High Impedance
	0	X	High Impedance

X = Don't care

Shift Registers

MM400/MM500 series dynamic shift registers*

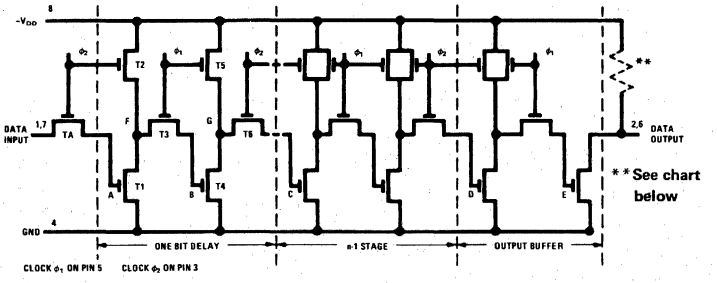
general description

The National Semiconductor line of dynamic shift registers are built on a single silicon chip utilizing MOS P channel enhancement mode transistors. Designed to operate over a wide frequency spectrum, these devices can be used in any sequential digital system that employs a two phase clocking system. The low threshold transistors used permit operation with a V_{DD} supply voltage of −10V and a −16V clock amplitude to obtain these device features:

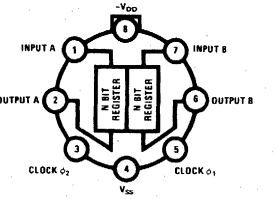
- Direct DTL or TTL compatibility
- High Frequency Operation — 1 MHz guaranteed
- Low Power Consumption — 0.8 mW/bit @ 1 MHz
- Minimum Operating Frequency Guarantee — 600Hz @ 25°C
- Military and Commercial Temperature Ranges
  - MM400 Series — −55°C to +125°C
  - MM500 Series — 0°C to +70°C
- Low Output Impedance (V_{OH}) — 500 ohms
- Clock inputs directly compatible with MH0009, two phase clock driver

The power dissipation of the device decreases as the operating frequency is decreased; at 10 kHz typical dissipation is 6 μW/bit. The minimum operating frequency is also reduced substantially at lower temperatures; typical minimum frequency of operation at 25°C is 100 Hz.

schematic and connection diagrams



Metal Can Package



Note: Pin 4 connected to case.

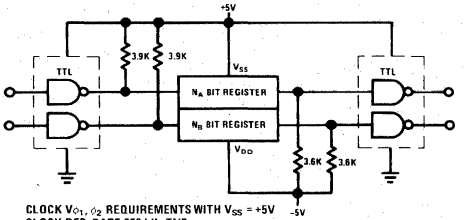
TOP VIEW

Order Number MM400H, MM500H, MM401H, MM501H, MM402H, MM502H, MM403H, MM503H, MM406H, MM506H, MM407H or MM507H

See Package 23

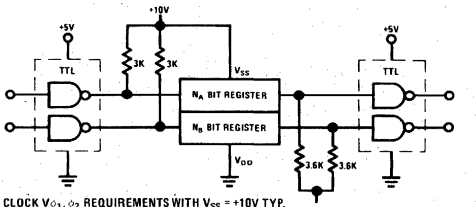
typical applications

FIGURE 1 – TTL/MOS Interface – Low Frequency
(see clock timing graph for detail)



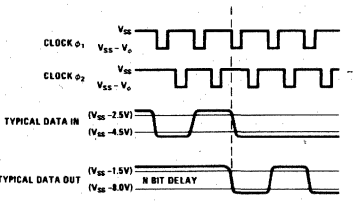
CLOCK V_{O1}, ϕ_2 REQUIREMENTS WITH V_{SS} = +5V
CLOCK REP. RATE 650 kHz TYP.
LOGIC "0" (V_{SS}) = +4.5V
LOGIC "1" ($V_{SS} - V_{OL}$) = −10V

FIGURE 2 – TTL/MOS Interfaces



CLOCK V_{O1}, ϕ_2 REQUIREMENTS WITH V_{SS} = +10V TYP.
LOGIC "0" (V_{SS}) = +9.5V
LOGIC "1" ($V_{SS} - V_{OL}$) = −6.0V

Waveforms for Applications



Standard Register Configurations †

CONFIGURATION	OPEN DRAIN OUTPUT		20 KΩ OUTPUT	
	−55°C to +125°C	−25°C to +70°C	−55°C to +125°C	−25°C to +70°C
Dual 25 bit	MM400	MM500	MM401	MM501
Dual 50 bit	MM402	MM502	MM403	MM503
*Dual 100 bit	MM406	MM506	MM407	MM507

†For other length registers consult your National representative.
*For New Designs, See MM4006A/MM5006A Data Sheet.

absolute maximum ratings

Drain Voltage ($-V_{DD}$)	+0.5V to −25V
Clock Inputs ($V\phi_1$, $V\phi_2$)	+0.5V to −25V
Data Inputs	+0.5V to −25V
Power Dissipation (Note 1)	500 mW
Operating Temperature	
MM400 Series	−55°C to +125°C
MM500 Series	−25°C to +70°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

electrical characteristics (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Clock Repetition Rate	See Fig. 2	See Note 5		1.0	MHz
	See Fig. 1	See Note 5		0.5	MHz
Clock Input Capacitance (Pins 3 & 5)	f = 1.0 MHz, 0V Bias				
	MM400, 401, 500, 501		22	40	pF
	MM402, 403, 502, 503		40	60	pF
	MM406, 407, 506, 507		85	100	pF
	−20V Bias				
	MM400, 401, 500, 501		18	25	pF
	MM402, 403, 502, 503		32	40	pF
	MM406, 407, 506, 507		55	65	pF
Data Output Voltage Levels					
MOS to MOS	V_{DD} = −10V, V_{SS} = GND				
Logic "0" (V_{OH})	freq = 1 MHz max. Input (d.c.)			V_{SS} −1.5	V
Logic "1" (V_{OL})		V_{SS} −8.0V			V
MOS to TTL (Fig. 1)	V_{DD} = GND, V_{SS} = +10V freq = 1 MHz max. Input (d.c.)				
Logic "0" (V_{OH})	I_L = 2.5 mA } See Note 6	2.5			V
Logic "1" (V_{OL})	I_L = −1.6 mA } See Note 6			0.4	V
MOS to TTL (Fig. 2)	V_{DD} = −5V, V_{SS} = +5V (V_{SS} = 4.75 min) freq = 0.5 MHz max.				
Logic "0" (V_{OH})	I_L = 2.5 mA } See Note 6	2.5			V
Logic "1" (V_{OL})	I_L = −1.6 mA } See Note 6			0.4	V
Breakdown Voltage	1.0 μA Test Current T_A = 25°C				
On Pin 1	GND on Pins 2, 3, 4, 5, 6, 7 −8V on Pin 8	−25			V
On Pin 2 (Note 3)	GND on Pins 1, 4, 6, 7, 8 −8V on Pins 3, 5	−25			V
On Pin 6 (Note 3)	GND on Pins 1, 2, 4, 7, 8 −8V on Pins 3, 5	−25			V
On Pin 7	GND on Pins 1, 2, 3, 4, 5, 6 −8V on Pin 8	−25			V
Leakage Current	T_A = 25°C				
Pin 1	V_1 = −18V, V_8 = −8V All Other Pins at GND			0.5	μA
Pin 2 (Note 4)	V_2 = −18V, V_3 = V_5 = −8V All Other Pins at GND			0.5	μA
Pin 6 (Note 4)	V_6 = −18V, V_3 = V_5 = −8V All Other Pins at GND			0.5	μA
Pin 7	V_7 = −18V, V_8 = −8V All Other Pins at GND			0.5	μA
Pin 8 (Note 4)	V_8 = −8V All Other Pins at GND			0.5	μA
Power Supply Current Drain	Outputs at Logic "1" 1 MHz Operations, T_A = 25°C (ϕ_1 = 0.4 μs, ϕ_2 = 0.2 μs)				
	MM400,401,500,501		4.5	9.0	mA
	MM402,403,502,503		9.0	14.0	(Average)
	MM406,407,506,507		18.0	30.0	

electrical drive requirements

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Clock Pulse Width	See Timing Diagram				
ϕ_1 Clock pw		0.4		10.0	μs
ϕ_2 Clock pw		0.2		10.0	μs
Clock Delay, ϕ_d	See Definition	0.1			μs
Clock Pulse Transition $t_{r\phi}$, $t_{f\phi}$	1 MHz, ϕ_{pw} = 0.2 μs			0.05	μs
	100 kHz, ϕ_{pw} = 0.2 μs			0.5	μs
	10 kHz, ϕ_{pw} = 10 μs			5.0	μs
Clock Input Level (V_ϕ)					
Logic "0" ($V_{\phi H}$)			V_{SS} −0.5	V_{SS} −1.5	V
Logic "1" ($V_{\phi L}$)		V_{SS} −14.5	V_{SS} −16.0	V_{SS} −18.0	V
Data Pulse Width t_{dw}		0.4			μs
Data Setup Time t_{ds}		0.1			μs
Data Input Voltage Levels					
MOS to MOS					
Logic "0" (V_{IH})	V_{DD} = −10V, V_{SS} = GND			2.0	V
Logic "1" (V_{IL})	freq = 1 MHz max.	−7.0			V
TTL to MOS (Fig. 1)					
Logic "0" (V_{IH})	V_{DD} = GND, V_{SS} = +10V			V_{SS} 2.0	V
Logic "1" (V_{IL})	freq = 1 MHz max.	V_{SS} −7.0			V
TTL to MOS (Fig. 2)					
Logic "0" (V_{IH})	V_{DD} = −5V, V_{SS} = +5V			V_{SS} 1.5	V
Logic "1" (V_{IL})	(V_{SS} = 4.75 min)				
	freq = 0.5 MHz max.	V_{SS} −4.2			V

Note 1: For operating at elevated temperatures, the device must be derated based on a +150°C maximum junction temperature and a thermal resistance of +150°C/W junction to ambient. The full rating applies for case temperatures to +125°C for MM400 Series and +70°C for MM500 Series units.

Note 2: These specifications apply over the indicated operating temperature ranges for V_{SS} = 0V and −11V < V_{DD} < −9.5V and 20 kΩ connected between pins 2 and 8 and between pins 6 and 8 without measurement load of less than 10 pF in parallel with 10 MΩ to ground unless otherwise specified. On the MM401/MM501, MM403/MM503, and MM407/MM507 optional versions which include 20 kΩ pull-up resistors internal to package, the external 20 kΩ resistors are not used in measurement circuits.

Note 3: For the odd number devices, MM401, MM403 and MM407, the output of pins 2 and 6 will exhibit a resistance when measured with the following bias conditions: pins 1, 6 and 8 = GND; pins 3 and 5 = −16V; pin 4 = open; measure pins 2 and 6 = 25k ≤ R_{OUT} ≤ 15 kΩ.

Note 4: Not for internal resistor devices.

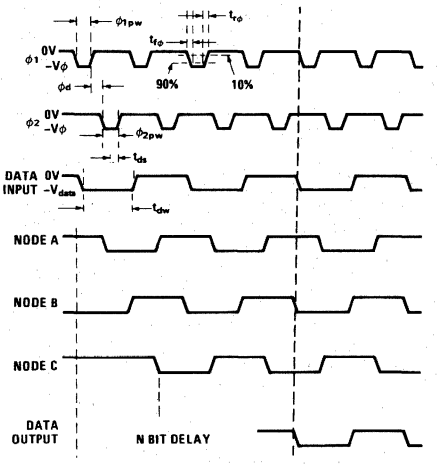
Note 5: See minimum operating frequency graph.

Note 6: In the logic "0" (V_{OH}) level the MOS register output will be sourcing 2.5 mA into the load combination of the pull-down resistors and the gate leakage current. In the logic "1" V_{OL} level I_L represents the current that the pull-down resistor and the internal 20k resistor combination will sink in order to insure current sinking capability for one gate.

operation

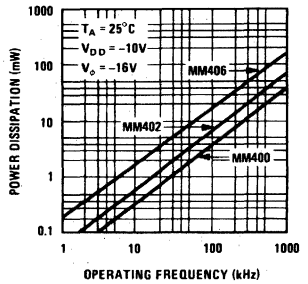
Each bit of delay shown in the circuit schematic consists of two inverters T1 and T4 accompanied by clocked load resistors T2 and T5 and two coupling devices T3 and T6. The circuit functions as follows: When ϕ_2 goes negative (one state) the coupling unit TA and the load resistor T2 are clocked ON allowing information at the input to be transferred to node A turning T1 ON or OFF depending on the state of the input. For example, if a negative potential (near $-V_{DD}$ level) is transferred from the input to the gate to source capacitance at node A, then T1 turns ON allowing node F to be at $\frac{-V_{DD}}{2}$. When ϕ_2 returns to its zero state (ground level) T2 turns OFF allowing node F to discharge to zero volts. When ϕ_1 goes negative (one state) the coupling unit T3 and the load resistor T5 are clocked ON allowing information at node F to be transferred to node B. T4 is held OFF if node F was at ground potential and is turned ON if node F had been at $-V_{DD}$ potential. Continuing the example above, T4 is held OFF and node G is at $-V_{DD}$ since T5 is ON during ϕ_1 clock pulse. When ϕ_1 returns to its zero state, node G maintains a $-V_{DD}$ voltage level. This voltage level is maintained at node G until the ϕ_2 clock appears. The bit delay demonstrated in this example is repeated through each half of the dual register.

timing diagram

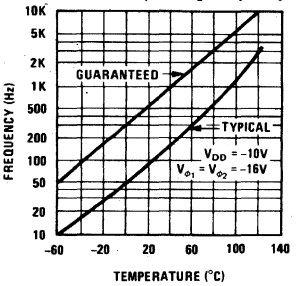


performance characteristics

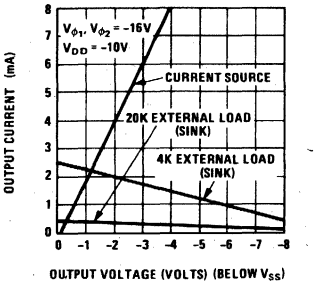
Power Dissipation vs Maximum Frequency



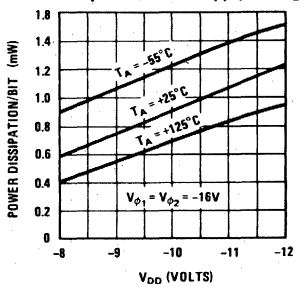
Minimum Operating Frequency



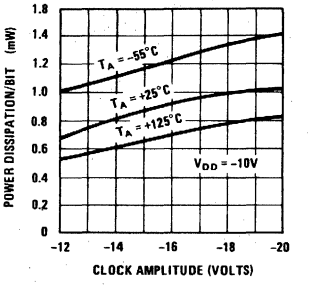
Output Sink/Source Current



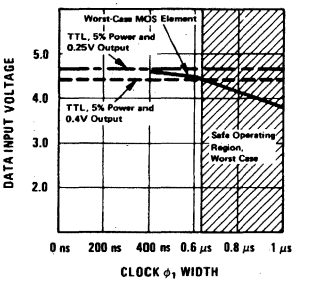
Power Dissipation/Bit vs. Supply Voltage



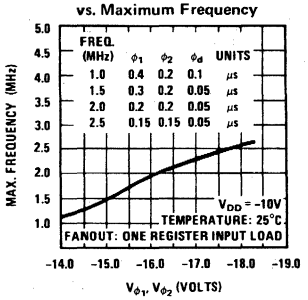
Power Dissipation/Bit vs. Clock Amplitude



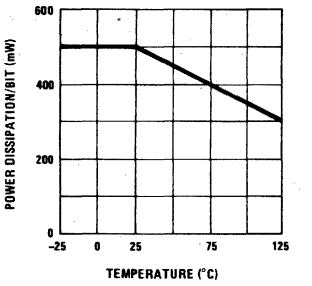
Clock Timing, Direct-Coupled TTL or DTL



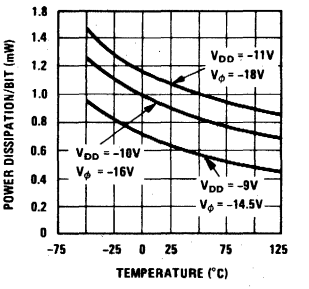
Clock Amplitude V_{ϕ_1}, V_{ϕ_2} vs. Maximum Frequency



Maximum Package Power Dissipation



Power Dissipation/Bit vs. Temperature



Note: All typical performance data is gathered with ϕ_{pw} = 0.4 µ; ϕ_{2pw} = 0.2 µs; ϕ_d = 0.1 µs; f = 1 MHz; except as otherwise noted.

Shift Registers

MM404/MM504 dual 16 bit static register*
MM405/MM505 dual 32 bit static register*

general description

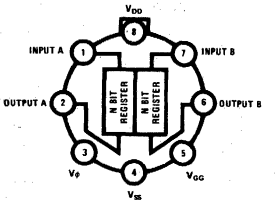
The National Semiconductor line of MOS static shift registers are monolithic integrated circuits utilizing P-channel enhancement mode transistors. The use of a low threshold technology permits operation with a V_{DD} supply voltage of −10 volts and a V_{GG} supply and clock amplitude voltage of less than −16 volts. These registers require only a single clock input to operate from DC to 1 MHz in either synchronous or asynchronous systems. Each register cell is designed specifically to avoid race conditions during latching, thus insuring operation under all conditions specified in the electrical characteristics.

Additional features include:

- Bipolar compatibility
- Single phase clock input
- High frequency operation 1.0 MHz
- Low power consumption 1.7 mW/bit typ
- Output impedance (V_{OH}) 500Ω typ
- Military and commercial temperature ranges
  - MM404, MM405 −55°C to +125°C
  - MM504, MM505 0°C to +70°C

connection diagram

Metal Can Package



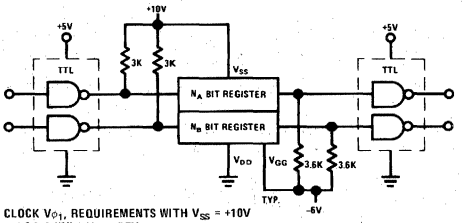
Note: Pin 4 connected to case.

TOP VIEW

Order Number MM404H, MM504H, MM405H or MM505H
See Package 23

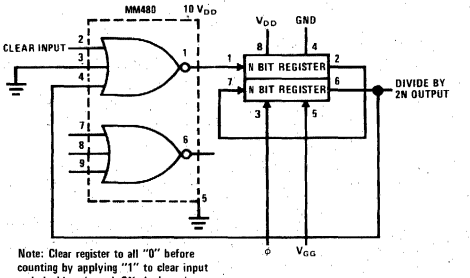
typical applications

TTL/MOS Interface



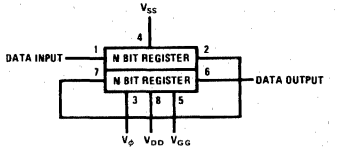
CLOCK V_{ϕ_1} REQUIREMENTS WITH V_{SS} = +10V
LOGIC "0" = V_{SS} −1.5V
LOGIC "1" = V_{SS} −16V

2N Bit Johnson Counter

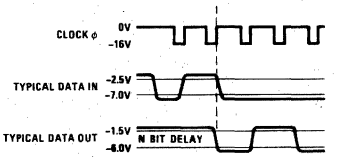


Note: Clear register to all "0" before counting by applying "1" to clear input and clocking through 2N clock cycles.

Single 2N Bit Register



Waveforms for Applications



*For New Designs, see MM4040/MM5040, MM4050A/MM5050A.

absolute maximum ratings

Drain Voltage (V_{DD})		+0.5V to −25V
Gate Voltage (V_{GG})		+0.5V to −25V
Clock Input ($V_{\phi 1}$)		+0.5V to −25V
Data Inputs		+0.5V to −25V
Power Dissipation (Note 1)		300 mW
Operating Temperature	MM404, MM405	−55°C to +125°C
	MM504, MM505	0°C to +70°C
Storage Temperature		−65°C to +150°C

electrical drive requirements (Note 1)

PARAMETER	CONDITION	MIN	TYP	MAX	UNITS
Clock pulse Width ϕ_1 Clock, ϕ_{1pw}		0.4		10	μs
Clock Pulse Risetime, $t_{r\phi}$	1 MHz with ϕ_{pw} = 0.4 μs			0.05	μs
Falltime, $t_{f\phi}$	100 kHz with ϕ_{pw} = 2 μs			0.6	μs
	10 kHz with ϕ_{pw} = 10 μs			2.0	μs
Clock Input Level					
Logic "$V_{\phi H}$"			V_{SS} −0.5	V_{SS} −1.5	V
Logic "$V_{\phi L}$"		V_{SS} −14.5	V_{SS} −16.0	V_{SS} −18.0	V
Data Input Voltage Levels					
Logic "V_{IH}"				V_{SS} −2.5	V
Logic "V_{IL}"		V_{SS} −7.0			V
Data Setup Time, t_{ds}		0.2			μs
Data Hold Time, t_{dh}		0.03			μs

electrical characteristics (Note 2)

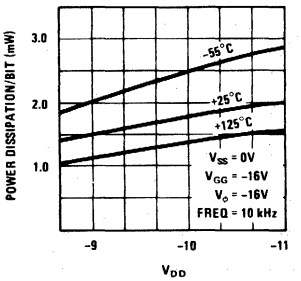
PARAMETER	CONDITION		MIN	TYP	MAX	UNITS
Clock Repetition Rate	Fan-Out "1"		dc		1.0	MHz
Data Output Voltage Levels						
Logic "V_{OH}"					V_{SS} −1.5	V
Logic "V_{OL}"			V_{SS} −8.0			V
Data Input Capacitance (Each Input)	f = 1 MHz V_{IN} = 0V			1.5	3.0	pF
Clock Line Capacitance	f = 1 MHz, −20V Bias	MM404, MM504		9.5	15	pF
		MM405, MM505		18	30	pF
	0V Bias	MM404, MM504		15.0	20	pF
		MM405, MM505		25	40	pF
Output Impedance	Outputs at Logic "0"			0.5	1.0	kΩ
Input Leakage Current Pin 1	T_A = 25°C V_{IN} = −18V All Other Pins at GND				0.5	μA
Power Supply Current Drain (V_{DD})	Outputs at Logic "0" 1 MHz Operation T_A = 25°C					
	MM404, MM504			5.5	10.0	mA
	MM405, MM505			10.0	15.0	mA

Note 1: For operating at elevated temperatures, the device must be derated based on a +150°C maximum junction temperature and a thermal resistance of +150°C/W junction to ambient. The full rating applies for case temperatures to +125°C.

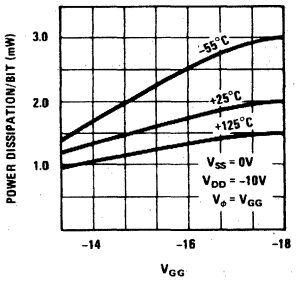
Note 2: These specifications apply over the specified temperature ranges for $-11V < V_{DD} < -9.5V$, and $-18V < V_{GG} < -14.5V$ and clock repetition rate of 10 kHz with output measurement load of less than 10 pF in parallel with 10 MΩ to ground unless otherwise specified.

performance characteristics

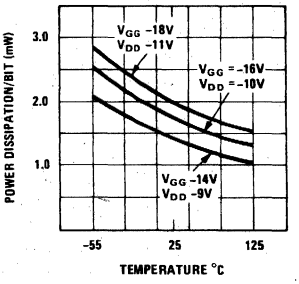
Power Dissipation vs V_{DD}



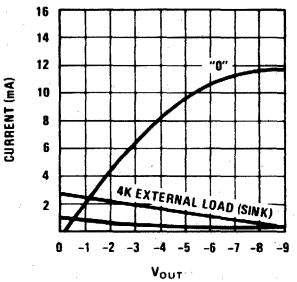
Power Dissipation vs V_{GG}



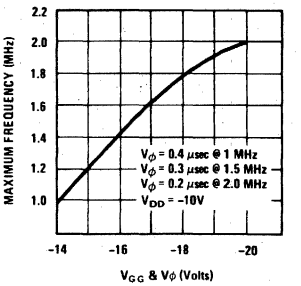
Power Dissipation vs Temp.



V_{OUT} vs Load Current



Max. Frequency vs Supply Voltages



operation

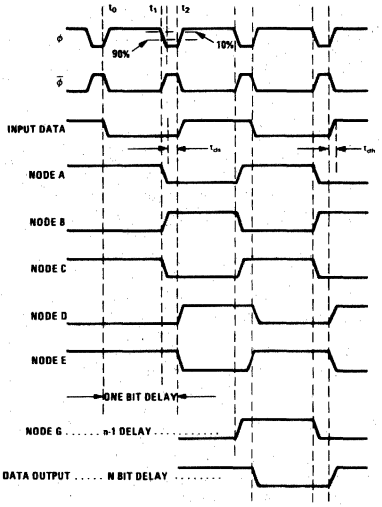
A diagram of a one-bit static register employing two clock phases (ϕ, $\bar{\phi}$) is shown in the schematic. The register requires only one external clock phase (ϕ) since the second clock ($\bar{\phi}$) is generated internally by T_{19} and 15K; this configuration simplifies the input drive requirements.

The basic cell functions as follows. Each bit of delay consists of three inverters T_2, T_4, and T_8 in conjunction with three MOS load resistors T_3, T_5, and T_9 followed by three coupling devices T_1, T_6, and T_7. The timing diagram shows the sequence of operation. Assume the input is at a logic "1" level during t_1 time. When the clock (ϕ) goes to a logic "1" level, two operations take place simultaneously. First, transistor T_1 turns "ON", transferring the input data (logic "1" level) to the gate to source capacitance (C_1) of T_2. The voltage stored on C_1 is sufficient to turn T_2 "ON" discharging node B. With the gate to source capacitance (C_2) of T_4 discharged, T_4 turns "OFF" placing a logic "1" level at node C. Concurrently ϕ turns T_{19} "ON" generating the complement of ϕ, that is ϕ and in turn $\bar{\phi}$ is used to turn T_6 and T_7 "OFF". This action allows the register's previous information to be temporarily stored on the gate to source capacitance C_3 of T_8. The output at node E during this timing sequence remains unchanged. However, during t_2 time, clock ϕ returns to ground; concurrently $\bar{\phi}$ goes to a logic "1" level turning T_1 "OFF" allowing T_6 and T_7 to turn "ON". The information which was previously stored on the gate of T_8 discharges to a logic "0" level causing the output at node E to switch to a logic "1" level thereby obtaining the required one-bit of delay.

Likewise the information at node C is fed back to node A latching T_2 in the "ON" state.

When a logic "0" level is presented at the register input, the sequence is once again repeated. The bit delay demonstrated in this example is repeated for each half of the dual static register.

timing diagram



8

NATIONAL

Shift Registers

MM1402A, MM1403A, MM1404A, MM5024A
1024-bit dynamic shift registers

general description

The MM1402A,MM1403A,MM1404A,MM5024A 1024-bit dynamic shift registers are MOS monolithic integrated circuits using silicon gate technology to achieve bipolar compatibility. 5 MHz data rates are achieved by on-chip multiplexing. The clock rate is one-half the data rate; i.e., one data bit is entered for each ϕ_1 and ϕ_2 clock pulse.

All devices in the family can operate from +5V, −5V, or +5V, −9V power supplies.

features

- Guaranteed 5 MHz operation
- Low power dissipation .1 mW/bit at 1 MHz
- DTL/TTL compatible
- Low clock capacitance 125 pF
- Low clock leakage $\leq 1\ \mu A$
- Inputs protected against static charge
- Operation from +5V, −5V or +5V, −9V power supplies
- Seven standard configurations

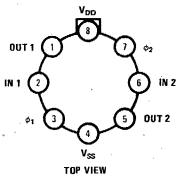
MM1402AD	Quad 256-bit
MM1402AN	Quad 256-bit
MM1403AH	Dual 512-bit
MM1403AN	Dual 512-bit
MM1404AH	Single 1024-bit
MM1404AN	Single 1024-bit
MM5024AH	Single 1024-bit with internal pull-down resistor

applications

- Radar and sonar processors
- CRT displays
- Terminals
- Desk top calculators
- Disk and drum replacement
- Computer peripherals
- Buffer memory
- Special purpose computers—signal processors, digital filtering and correlators, receivers, spectral compressors and digital differential analyzers
- Telephone equipment
- Medical equipment

connection diagrams

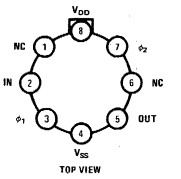
Metal Can Package



TOP VIEW

Order Number MM1403AH
See Package 23

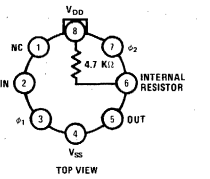
Metal Can Package



TOP VIEW

Order Number MM1404AH
See Package 23

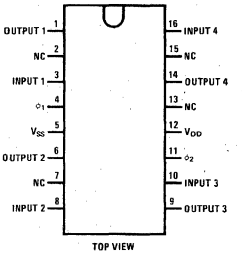
Metal Can Package



TOP VIEW

Order Number MM5024AH
See Package 23

Dual-In-Line Package

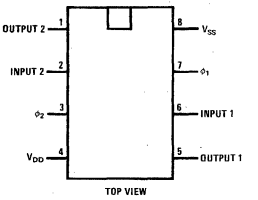


TOP VIEW

Order Number MM1402AD
See Package 3

Order Number MM1402AN
See Package 15

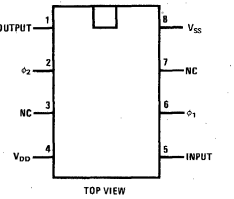
Dual-In-Line Package



TOP VIEW

Order Number MM1403AN
See Package 12

Dual-In-Line Package



TOP VIEW

Order Number MM1404AN
See Package 12

absolute maximum ratings

Data and Clock Input Voltages and Supply Voltages with Respect to V_{SS}	+0.3V to −20V
Power Dissipation	600 mW at T_A = 25°C
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +160°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics

T_A = −25°C to +70°C, V_{SS} = 5V ±5%, V_{DD} = −5V ±5% or −9V ±5%, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Data Input Levels					
Logical Low Level (V_{IL})		V_{SS} − 10.0		V_{SS} − 4.2	V
Logical High Level (V_{IH})		V_{SS} − 1.7		V_{SS} + 0.3	V
Data Input Leakage Current	V_{IN} = −15V, T_A = 25°C, All Other Pins GND		<10	500	nA
Input Capacitance	V_{IN} = V_{SS}		5	10	pF
Clock Input Levels	V_{DD} = −5V ± 5%				
Logical Low Level ($V_{\phi L}$)		V_{SS} − 17		V_{SS} − 15	V
Logical High Level ($V_{\phi H}$)		V_{SS} − 1		V_{SS} + 0.3	V
Logical Low Level ($V_{\phi L}$)	V_{DD} = −9V ± 5%	V_{SS} − 14.7		V_{SS} − 12.6	V
Logical High Level ($V_{\phi H}$)		V_{SS} − 1		V_{SS} + 0.3	V
Clock Leakage Current	Min $V_{\phi L}$, T_A = 25°C		10	1000	nA
Clock Capacitance	V_ϕ = V_{SS}		90	125	pF
Data Output Levels					
Logical Low Level (V_{OL})	R_{L1} = 3k to V_{DD}, I_{OL} = 1.6 mA, V_{DD} = −5V ± 5%		−0.3	0.5	V
Logical High Level (V_{OH})	R_{L1} = 3k to V_{DD}, I_{OH} = 100 μA	2.4	3.5		V
Logical Low Level (V_{OL})	R_{L1} = 4.7k to V_{DD}, I_{OL} = 1.6 mA, V_{DD} = −9V ± 5%		−0.3	0.5	V
Logical High Level (V_{OH})	R_{L1} = 4.7k to V_{DD}, I_{OH} = 100 μA	2.4	3.5		V
Logical High Level (V_{OH})	R_{L2} = 4.7k to V_{DD}, V_{DD} = −5V ± 5%	V_{SS} − 1.9	V_{SS} − 1		V
Logical High Level (V_{OH})	R_{L2} = 6.2k to V_{DD}, V_{DD} = −9V ± 5%, R_{L3} = 3.9k to V_{SS}	V_{SS} − 1.9	V_{SS} − 1		V
Power Supply Current (I_{DD})	T_A = 25°C, V_{DD} = −5V ± 5%, Output Logic "0", 5 MHz Data Rate, 33% Duty Cycle, Continuous Operation, $V_{\phi L}$ = V_{SS} − 17V		35	50	mA
	T_A = 0°C			56	mA
	T_A = 25°C, V_{DD} = −9V ± 5%, Output at Logic "0", 3 MHz Data Rate, 26% Duty Cycle, Continuous Operation, $V_{\phi L}$ = V_{SS} − 14.7V		30	40	mA
	T_A = 0°C			45	mA
Data Output Leakage Current	V_{OUT} = 0.0V, T_A = 25°C, $V_{\phi 1}$ = $V_{\phi 2}$ = V_{SS} − 10V, All Other Pins +5V		<10	1000	nA
Internal Resistor (MM5024A)	T_A = 25°C	3.7	4.7	5.2	kΩ
Output Capacitance	V_{OUT} = V_{SS}, f = 1 MHz		5	10	pF

ac characteristics T_A = −0°C to +70°C, V_{SS} = 5V ±5%

PARAMETER	V_{DD} = −5V ± 5%		V_{DD} = −9V ± 5%		UNITS
	MIN	MAX	MIN	MAX	
Clock Frequency (ϕ_f)	Note 1	2.5	Note 1	1.5	MHz
Data Frequency		5.0		3.0	MHz
Clock Pulse Width (ϕ_{PW})	0.130	10	0.170	10	μs
Clock Phase Delay Times (ϕ_d, $\bar{\phi}_d$)	10	Note 1	10	Note 1	ns
Clock Transition Times (ϕt_r, ϕt_f)		1000		1000	ns
Data Input Delay Time (t_{ds})	30		60		ns
Data Input Hold Time (t_{dH})	20		20		ns
Data Output Propagation Delay		90		110	ns

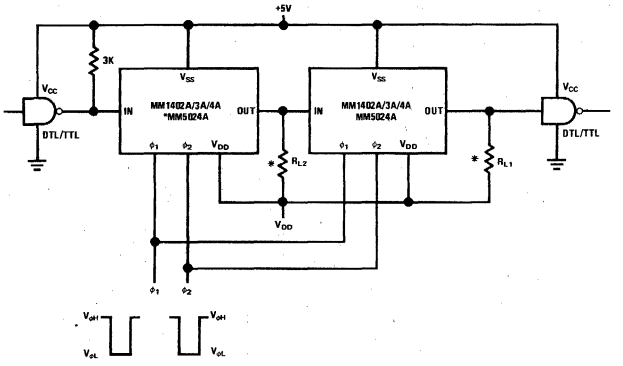
Note 1: Minimum clock frequency is a function of temperature and clock phase delay times, ϕ_d and $\bar{\phi}_d$ as shown by the ϕ_f versus temperature and ϕ_d, $\bar{\phi}_d$ versus temperature curves. The lowest guaranteed clock frequency can be attained by making ϕ_d equal to $\bar{\phi}_d$. The minimum guaranteed clock frequency is:

$\phi_f(\min) \cong 1/(\phi_d + \bar{\phi}_d)$ for the condition ($\phi t_r = \phi t_f << \phi_{PW} << \phi_d$ or $\bar{\phi}_d$), where the variables may not exceed the guaranteed maximums.

Note 2: Capacitance is guaranteed by periodic testing.

typical application

DTL/TTL to MOS Interface



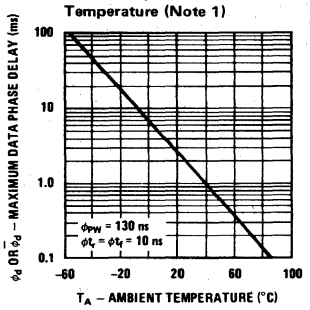
*A 4.7 kΩ resistors is included on the chip in the MM5024A and is connected between Pin 6 and V_{DD}.

R_L Load Resistor Value for Different V_{DD} Supplies

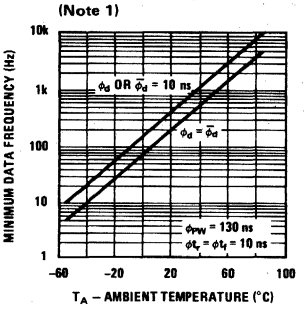
	V_{SS} = 5V V_{DD} = −5V	V_{SS} = 5V V_{DD} = −9V
R_{L1}	3.0k	4.7k
R_{L2}	4.7k	6.8k
R_{L3}	Not required	Not required

performance curves

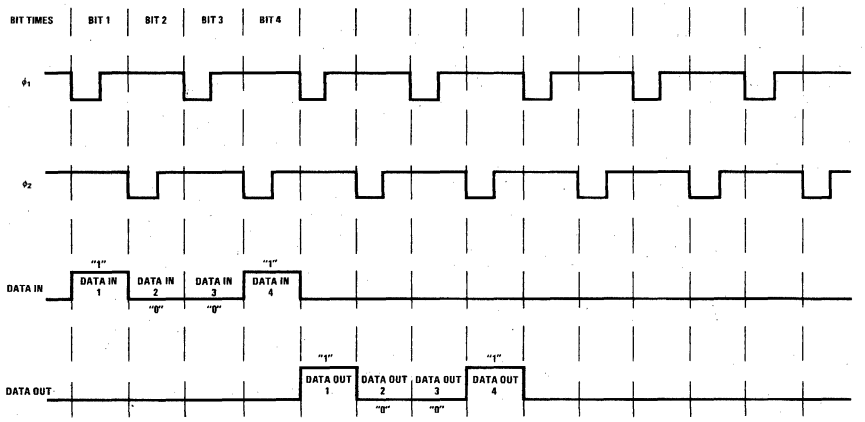
Guaranteed Maximum Data Phase Delay Times vs Temperature (Note 1)



Guaranteed Minimum Data Frequency vs Temperature (Note 1)

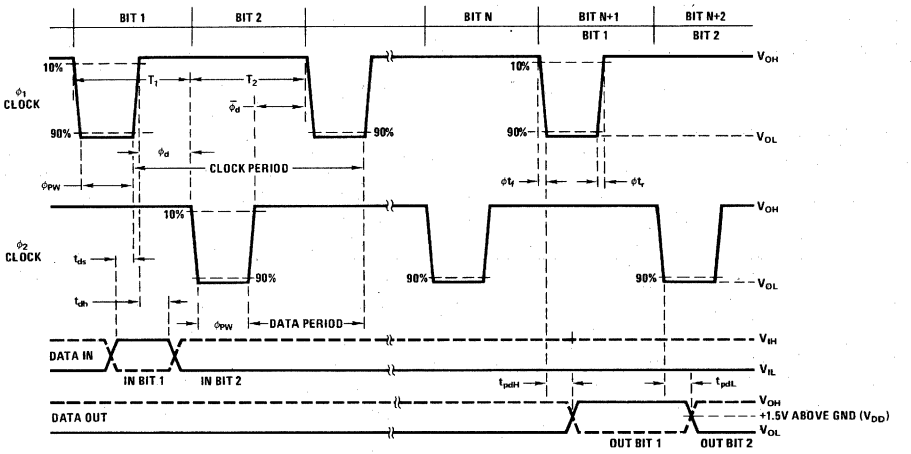


switching time waveforms



Shown is a simplified illustration of the timing of a 4-bit multiplexed register showing input output relationships with respect to the clock. If data enters the register at ϕ_1 time, it exists at ϕ_1 time. (Beginning on ϕ_1's negative going edge and ending on the succeeding ϕ_2's negative going edge.)

timing diagram



NATIONAL

Shift Registers

MM4001A/MM5001A dual 64-bit dynamic shift register
MM4010A/MM5010A dual 64-bit accumulator

general description

The MM4001A/MM5001A dual 64-bit dynamic shift register is a monolithic MOS integrated circuit utilizing P-channel enhancement mode low threshold technology. The device consists of two 64-bit registers with independent two phase clocks and is guaranteed to operate at a 2.5 MHz operating frequency for CRT display applications.

The MM4010A/MM5010A is a dual accumulator function capable of operating at very high frequency. The device is also constructed on a single silicon chip utilizing MOS P-channel enhancement transistors. With the recirculate control line at an MOS logic "0" state, the device functions as an accumulator. A logic "1" state at the recirculate control line allows external information to enter the register serially. It is important to note that recirculation of data is performed internally, independent of the output circuit thus making it insensitive to output loading.

features

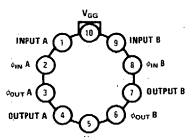
- High frequency operation — 3.3 MHz typ
- Low power consumption — 0.4 mW/bit at 1 MHz
- DTL/TTL compatibility — +5V, −12V power supplies, push-pull output stage
- Minimum operating frequency — guaranteed 250 Hz at 25°C
- Application versatility — "Split clock" operation, independent control of each register for MM4001A/MM5001A

applications

- Business machine
- CRT refresh memory
- Delay line memory
- Arithmetic operations

connection diagrams

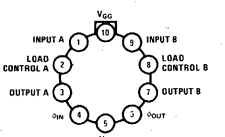
Metal Can Package



Note: Pin 5 connected to case.
TOP VIEW

Order Number MM4001AH or MM5001AH
See Package 24

Metal Can Package



Note: Pin 5 connected to case.
TOP VIEW

Order Number MM4010AH or MM5010AH
See Package 24

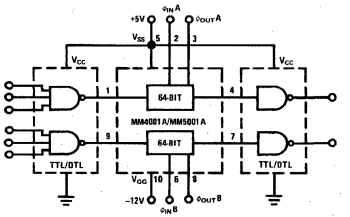
load control truth table

MM4010A/MM5010A

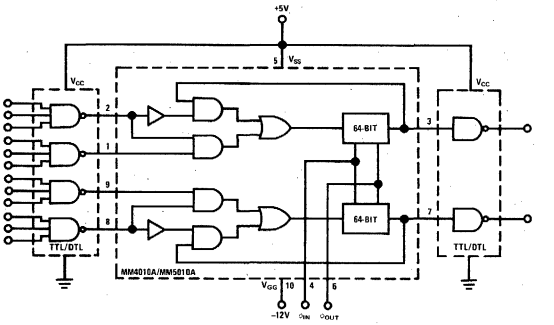
LOGICAL HIGH LEVEL (V_{LCH})	LOGICAL LOW LEVEL (V_{LCL})
Recirculates "old" data	Loads "new" data

typical applications

MM4001A/MM5001A TTL/MOS Interface



MM4010A/MM5010A TTL/MOS Interface



absolute maximum ratings

Voltage at Any Pin	V_{SS} + 0.3V to V_{SS} − 22V
Operating Temperature Range	
MM4010A/MM4001A	−55°C to +125°C
MM5010A/MM5001A	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics

T_A within operating temperature range, V_{SS} = +5.0V ±5%, V_{GG} = −12.0V ±10%, unless otherwise stated.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Data Input Levels					
Logical HIGH Level (V_{IH})		V_{SS} − 2.0		V_{SS} + 0.3	V
Logical LOW Level (V_{IL})		V_{SS} − 18.5		V_{SS} − 4.2	V
Data Input Leakage	V_{IN} = −20V, T_A = 25°C, All Other Pins GND		0.01	0.5	μA
Data Input Capacitance	V_{IN} = 0.0V, f = 1 MHz, All Other Pins GND, Note 2		3.0	5.0	pF
Load Control Input Levels					
Logical HIGH Level (V_{LCH})		V_{SS} − 2.0		V_{SS} + 0.3	V
Logical LOW Level (V_{LCL})		V_{SS} − 18.5		V_{SS} − 4.2	V
Load Control Input Leakage	V_{IN} = −20V, T_A = 25°C, All Other Pins GND		0.01	0.5	μA
Load Control Input Capacitance	V_{IN} = 0.0V, f = 1 MHz, All Other Pins GND, Note 2		3.0	5.0	pF
Clock Input Levels					
Logical HIGH Level ($V_{\phi H}$)		V_{SS} − 1.5		V_{SS} + 0.3	V
Logical LOW Level ($V_{\phi L}$)		V_{SS} − 18.5		V_{SS} − 14.5	V
Clock Input Leakage	V_ϕ = −20V, T_A = 25°C, All Other Pins GND		0.05	1.0	μA
Clock Input Capacitance	V_ϕ = 0.0V, f = 1 MHz, All Other Pins GND, Note 2				
	MM4001A/MM5001A		17	20	pF
	MM4010A/MM5010A		34	40	pF
Data Output Levels					
Logical HIGH Level (V_{OH})	I_{SOURCE} = −0.5 mA	2.4		V_{SS}	V
Logical LOW Level (V_{OL})	I_{SINK} = 1.6 mA			0.4	V
Power Supply Current					
I_{GG}	T_A = 25°C, V_{GG} = −12V, ϕ_{PW} = 150 ns, V_{SS} = 5.0V, $V_{\phi L}$ = −12V, Data = 0-1-0-1				
	0.01 MHz ≤ ϕ_f ≤ 0.1 MHz		2.0	3.0	mA
	ϕ_f = 1 MHz		3.0	4.5	mA
	ϕ_f = 2.5 MHz		5.0	7.0	mA
Clock Frequency (ϕ_f)	$\phi t_r = \phi t_f$ = 20 ns, Note 1	0.01	3.3	2.5	MHz
Clock Pulsewidth (ϕ_{PW})	$\phi t_f + \phi_{PW} + \phi t_r \leq 10.5\,\mu s$	0.15		10	μs
Clock Phase Delay Times ($\phi_d, \overline{\phi}_d$)	Note 1	10			ns
Clock Transition Times (ϕt_r, ϕt_f)	$\phi t_f + \phi_{PW} + \phi t_r \leq 10.5\,\mu s$			1	μs
Partial Bit Times (T)	Note 1				
Input Partial Bit Time (T_{IN})		0.20		100	μs
Output Partial Bit Time (T_{OUT})		0.20		100	μs
Data Input Setup Time (t_{ds})		80	30		ns
Data Input Hold Time (t_{dh})		20	0		ns
Load Control Input Setup Time (t_{LCs})		80	30		ns
Load Control Input Hold Time (t_{LCh})		20	0		ns
Data Output Propagation Delay From ϕ_{OUT}	See ac test circuit				
Delay to HIGH Level (t_{pdH})			150	200	ns
Delay to LOW Level (t_{pdL})			150	200	ns

Note 1: Minimum clock frequency is a function of temperature and partial bit times, T_{IN} and T_{OUT}, as shown by the ϕ_f versus temperature and T_{IN}, T_{OUT} versus temperature curves. The lowest guaranteed clock frequency for any temperature can be attained by making T_{IN} equal to T_{OUT}. The minimum guaranteed clock frequency is:

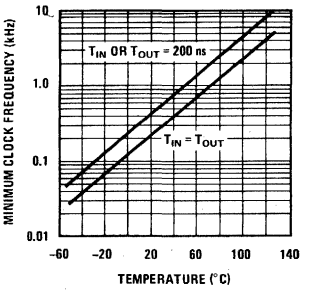
$$\phi_{f(min)} = \frac{1}{T_{IN} + T_{OUT}}$$

where T_{IN} and T_{OUT} may not exceed the guaranteed maximums.

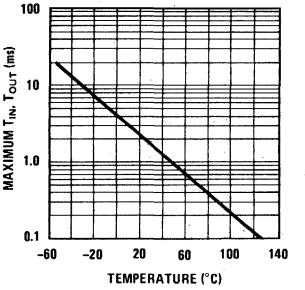
Note 2: Capacitance is guaranteed by lot sample testing.

performance characteristics

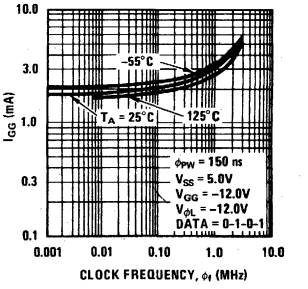
Guaranteed Minimum Clock Frequency vs Temperature (Note 1)



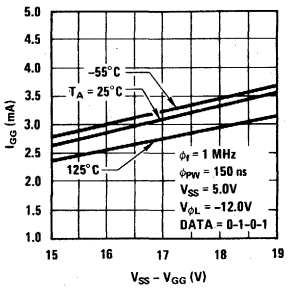
Guaranteed Maximum T_{IN} and T_{OUT} vs Temperature (Note 1)



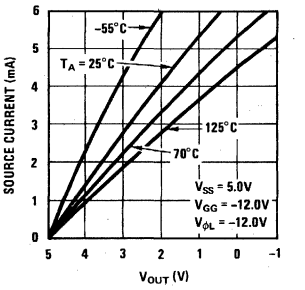
Typical Power Supply Current vs Clock Frequency



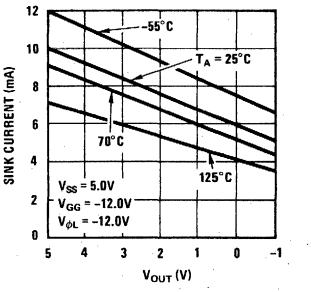
Typical Power Supply Current vs Voltage



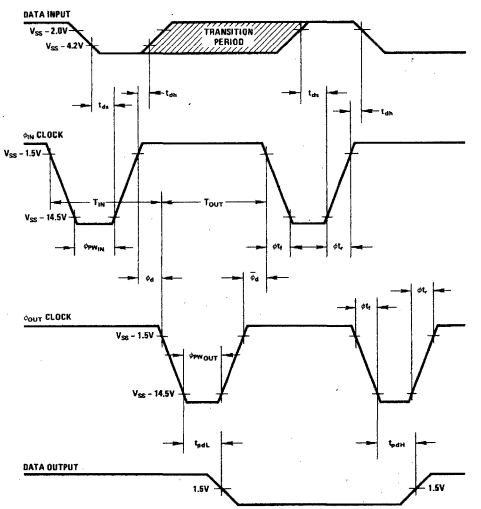
Typical Data Output Source Current vs Data Output Voltage



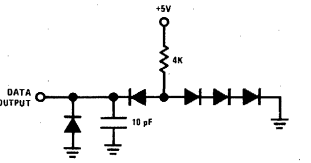
Typical Data Output Sink Current vs Data Output Voltage



switching time waveforms



ac test circuit



Shift Registers

NATIONAL

MM4006A/MM5006A dual 100-bit shift register
MM4007/MM5007 dual 100-bit mask programmable shift register
MM4019/MM5019 dual 256-bit mask programmable shift register

general description

The MM4007/MM5007 and MM4019/MM5019 are monolithic dual 100-bit and dual 256-bit dynamic shift registers utilizing P-channel enhancement mode technology to achieve bipolar compatibility. The length of the registers may be varied at manufacture by the altering of the metal mask providing custom length of both registers. Additional connection between registers may be accomplished at the metal mask to provide single shift register lengths of up to 200 or 512-bits, with or without an appropriate tap provided at the juncture. The MM5006A is an MM5007 programmed as a dual 100-bit shift register.

For the MM4007/MM5007 N = 20 to 100 bits
For the MM4019/MM5019 N = 40 to 256 bits

STANDARD LENGTHS:

MM4006A	Dual 100-bit
MM4007/AA	Dual 80-bit
MM4019	Dual 256-bit

CUSTOM LENGTHS:

The programmed shift registers are assigned a letter code for each option. These are designated by a pair of letters after the number code but before the package designation such as

MM5007/AA/H

which is a 0°C to +70°C dual 80-bit dynamic shift register in the TO-99 package. Pattern codes are assigned by National upon initial order entry. See MOS Brief 14 for a more detailed description of the custom mask.

features

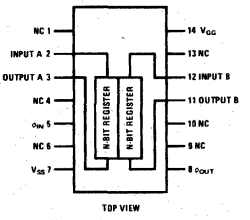
- Bipolar compatibility — Standard +5V, −12V power supplies
- Mask programmable length
  - MM4007/MM5007 — dual 20-100 bits
  - MM4019/MM5019 — dual 40-256 bits
- Low clock capacitance
  - MM4007/MM5007 — 65 pF max
  - MM4019/MM5019 — 125 pF max
- Standard clock frequency — 250 Hz min — typical at 25°C, 2.5 MHz max — guaranteed over temp
- Full temperature range
  - MM4007,MM4019 — −55°C to +125°C
  - MM5007,MM5019 — 0°C to +70°C

applications

- Custom shift registers
- CRT recirculate display

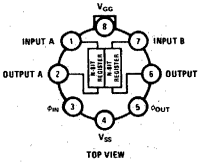
connection diagrams

Dual-In-Line Package



TOP VIEW

Note: Pin 7 connected to case.

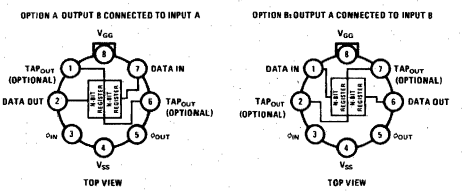


TOP VIEW

Note: Pin 4 connected to case.

Standard Connection

Metal Can Packages



TOP VIEW

Note: Pin 4 connected to case.

TOP VIEW

Note: Pin 4 connected to case.

Optional Connections

ordering information

DUAL 80-BIT	DUAL 100-BIT	DUAL 100-BIT	DUAL 256-BIT	PROGRAMMABLE 20 to 100 Bits	PROGRAMMABLE 40 to 256 Bits	SEE PACKAGE
MM4007AA/D	MM4006AD	MM4007D	MM4019D	MM4007XX/D	MM4019XX/D	2
MM4007AA/H	MM4006AH	MM4007H	MM4019H	MM4007XX/H	MM4019XX/H	23
MM5007AA/D	MM5006AD	MM5007D	MM5019D	MM5007XX/D	MM5019XX/D	2
MM5007AA/H	MM5006AH	MM5007H	MM5019H	MM5007XX/H	MM5019XX/H	23

absolute maximum ratings

Voltage at Any Pin	V_{SS} + 0.3V to V_{SS} − 22V
Operating Temperature Range	
MM4006A,MM4007,MM4019	−55°C to +125°C
MM5006A,MM5007,MM5019	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

electrical characteristics

T_A within operating temperature range, V_{SS} = 5.0V ±5%, V_{GG} = −12.0V ±10%, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Data Input Levels					
Logical HIGH Level (V_{IH})		V_{SS} − 2.0		V_{SS} + 0.3	V
Logical LOW Level (V_{IL})		V_{SS} − 18.5		V_{SS} − 4.2	V
Data Input Leakage	V_{IN} = −20V, T_A = 25°C, All Other Pins GND		0.01	0.5	μA
Data Input Capacitance	V_{IN} = 0.0V, f = 1 MHz, All Other Pins GND (Note 1)		3.0	5.0	pF
Clock Input Levels					
Logical HIGH Level ($V_{\phi H}$)		V_{SS} − 1.5		V_{SS} + 0.3	V
Logical LOW Level ($V_{\phi L}$)		V_{SS} − 18.5		V_{SS} − 14.5	V
Clock Input Leakage	V_ϕ = −2.0V, T_A = 25°C, All Other Pins GND		0.05	1.0	μA
Clock Input Capacitance	V_ϕ = 0.0V, f = 1 MHz, All Other Pins GND (Note 1)				
MM4006A/MM5006A & MM4007/MM5007			50	65	pF
MM4019/MM5019			95	125	pF
Data Output Levels					
Logical HIGH Level (V_{OH})	I_{SOURCE} = −0.5 mA	2.4		V_{SS}	V
Logical LOW Level (V_{OL})	I_{SINK} = 1.6 mA			0.4	V
Power Supply Current I_{GG}	T_A = 25°C, V_{GG} = −12V, ϕ_{PW} = 150 ns, V_{SS} = 5.0V, $V_{\phi L}$ = −12V, Data = 0-1-0-1				
MM4006A/MM5006A & MM4007/MM5007	0.01 MHz ≤ ϕ_f ≤ 0.1 MHz		2.0	3.0	mA
MM4019/MM5019			2.5	3.5	mA
MM4006A/MM5006A & MM4007/MM5007	ϕ_f = 1.0 MHz		4.0	6.0	mA
MM4019/MM5019			5.0	7.0	mA
MM4006A/MM5006A & MM4007/MM5007	ϕ_f = 2.5 MHz		6.0	9.0	mA
MM4019/MM5019			9.0	12.0	mA
Clock Frequency (ϕ_f)	$\phi t_r = \phi t_f$ = 20 ns	.01	3.3	2.5	MHz
Clock Pulsewidth (ϕ_{PW})	$\phi t_f + \phi_{PW} + \phi t_r \leq 10.5\ \mu s$	0.15		10	μs
Clock Phase Delay Times (ϕ_d, $\overline{\phi}_d$)	(Note 2)	10			ns
Clock Transition Times (ϕt_r, ϕt_f)	$\phi t_f + \phi_{PW} + \phi t_r \leq 10.5\ \mu s$			1.0	μs
Partial Bit Times (T)	(Note 2)				
Input Partial Bit Time (T_{IN})		0.20		100	μs
Output Partial Bit Time (T_{OUT})		0.20		100	μs
Data Input Setup Time (t_{ds})		80	30		ns
Data Input Hold Time (t_{dh})		20	0		ns
Data Output Propagation Delay from ϕ_{OUT}	(See ac test circuit)				
Delay to High Level (t_{pdH})			150	200	ns
Delay to Low Level (t_{pdL})			150	200	ns

Note 1: Capacitance is guaranteed by periodic testing.

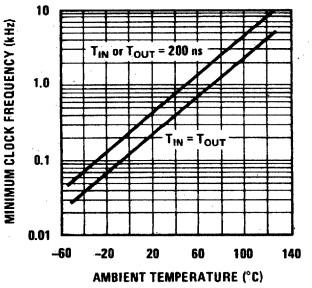
Note 2: Minimum clock frequency is a function of temperature and partial bit times (T_{IN} and T_{OUT}) as shown by the ϕ_f versus temperature and T_{IN}, T_{OUT} versus temperature curves. The lowest guaranteed clock frequency for any temperature can be attained by making T_{IN} equal to T_{OUT}. The minimum guaranteed clock frequency is:

$$\phi f(min) = \frac{1}{T_{IN} + T_{OUT}}$$, where T_{IN} and T_{OUT} do not exceed the guaranteed maximums.

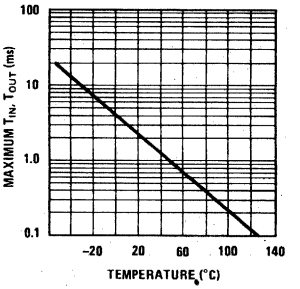
Note 3: Minimum clock frequency and partial bit time curves are guaranteed by testing at a high temperature point.

performance characteristics

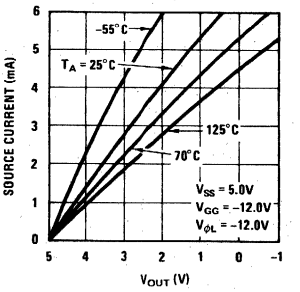
Guaranteed Minimum Clock Frequency vs Temperature (Note 2)



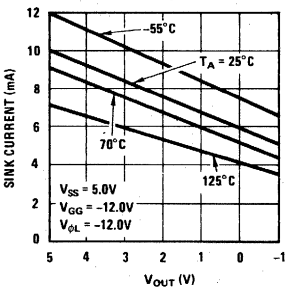
Guaranteed Maximum T_{IN} and T_{OUT} vs Temperature (Note 2)



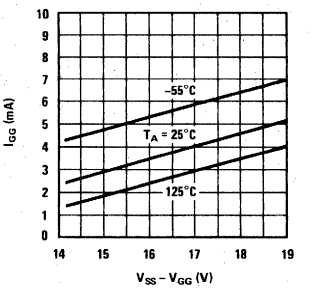
Typical Data Output Source Current vs Voltage



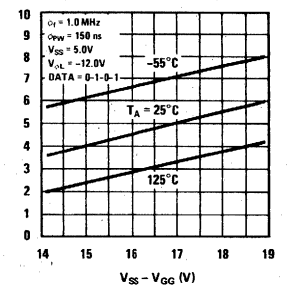
Typical Data Output Sink Current vs Voltage



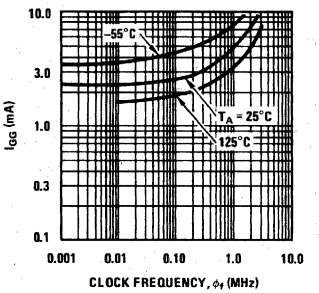
Typical Power Supply Current vs Voltage MM4006A/MM5006A MM4007/MM5007



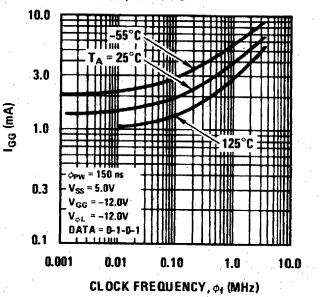
Typical Power Supply Current vs Voltage MM4019/MM5019



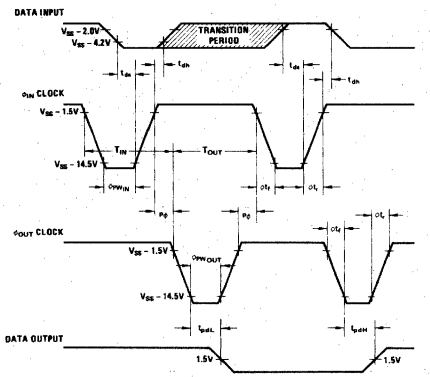
Typical Power Supply Current vs Clock Frequency MM4019/MM5019



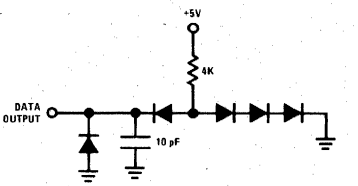
Typical Power Supply Current vs Clock Frequency MM4006A/MM5006A/ MM4007/MM5007



switching waveforms



ac test circuit



NATIONAL

Shift Registers

MM4013/MM5013 1024-bit dynamic shift register/accumulator

general description

The MM4013/MM5013 1024-bit dynamic shift register/accumulator is an MOS monolithic integrated circuit using P-channel enhancement mode low threshold technology to achieve direct bipolar compatibility. There is on-chip logic to load and recirculate data, and a read control for enabling the bus-ORable TRI-STATE™ push pull output stage.

features

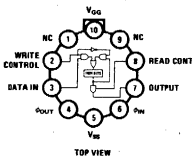
- Bipolar compatibility — Standard +5V, −12V power supplies; No pull down or pull up resistors required
- Package option — TO-99 or molded 8-pin mini-DIP
- Low clock capacitance — 160 pF max
- Wide frequency range — ϕ_f min = 400 Hz @ 25°C typ; ϕ_f max = 2.5 MHz over temp. guaranteed
- Built-in recirculate — Exclusive-OR and recirculate loop on-chip
- TRI-STATE output — Allows wire-OR bus structure on output
- Full temperature operation — MM4013 −55°C to +125°C; MM5013 0°C to +70°C

applications

- "Silicon Store" replacement for drum and disc memories
- File memories
- CRT refresh

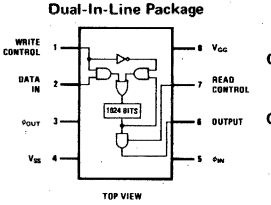
connection diagrams

Metal Can Package



Order Number MM4013H or MM5013H
See Package 24

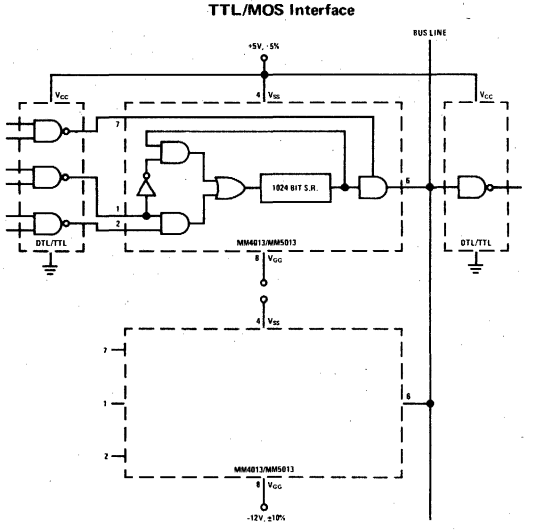
Dual-In-Line Package



Order Number MM4013D or MM5013D
See Package 1
Order Number MM5013N
See Package 12

typical applications

TTL/MOS Interface



truth table

(Positive Logic)
Logic "1" = V_{IH} = Logical HIGH Level
Logic "0" = V_{IL} = Logical LOW Level

WRITE	READ	FUNCTION
0	0	Recirculate Output Disabled
0	1	Recirculate Output Enabled
1	0	Write Mode Output Disabled
1	1	Write Mode Output Enabled

absolute maximum ratings

Voltage at Any Pin	$V_{SS}+0.3$ to $V_{SS}-22$
Operating Temperature Range MM4013	−55°C to +125°C
MM5013	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics

T_A within operating temperature range, V_{SS} = +5.0V ±5%, V_{GG} = −12.0V ±10%, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Data Input Levels					
Logical HIGH Level (V_{IH})		$V_{SS}-2.0$		$V_{SS}+0.3$	V
Logical LOW Level (V_{IL})		$V_{SS}-18.5$		$V_{SS}-4.2$	V
Data Input Leakage	V_{IN} = −20.0V, T_A = 25°C, All Other Pins GND		0.01	0.5	μA
Data Input Capacitance	V_{IN} = 0.0V, f = 1 MHz, All Other Pins GND (Note 1)		3.0	5.0	pF
Control Input Levels					
Logical HIGH Level (V_H)		$V_{SS}-2.0$		$V_{SS}+0.3$	V
Logical LOW Level (V_L)		$V_{SS}-18.5$		$V_{SS}-4.2$	V
Control Input Leakage	V_{IN} = −20.0V, T_A = 25°C, All Other Pins GND		0.01	0.5	μA
Control Input Capacitance	V_{IN} = 0.0V, f = 1 MHz, All Other Pins GND (Note 1)		3.0	5.0	pF
Clock Input Levels					
Logical HIGH Level ($V_{\phi H}$)		$V_{SS}-1.5$		$V_{SS}+0.3$	V
Logical LOW Level ($V_{\phi L}$)		$V_{SS}-18.5$		$V_{SS}-14.5$	V
Clock Input Leakage	V_ϕ = −20.0V, T_A = 25°C, All Other Pins GND		0.05	1.0	μA
Clock Input Capacitance	V_ϕ = 0.0V, f = 1 MHz All Other Pins GND (Note 1)		140	190	pF
Data Output Levels					
Logical HIGH Level (V_{OH})	I_{SOURCE} = −0.5 mA	2.4		V_{SS}	V
Logical LOW Level (V_{OL})	I_{SINK} = 1.6 mA			0.4	V
Data Output Leakage	V_{OUT} = −5.0V, T_A = 25°C Output in High Impedance State			10.0	μA
Power Supply Current I_{GG}	T_A = 25°C, V_{GG} = −12V, ϕ_{PW} = 150 ns, V_{SS} = 5.0V, $V_{\phi L}$ = −12V, Data = 0-1-0-1				
	0.01 MHz ≤ ϕ_f ≤ 0.1 MHz		1.60	3.0	mA
	ϕ_f = 1.0 MHz		5.3	8.0	mA
	ϕ_f = 2.5 MHz		10.3	15.0	mA
Clock Frequency (ϕ_f)	$\phi t_r = \phi t_f$ = 20 ns, (Note 2)	0.01	3.3	2.5	MHz
Clock Pulsewidth (ϕ_{PW})	$\phi t_f + \phi_{PW} + \phi t_r \leq 10.5\ \mu s$	0.15		10	μs
Clock Phase Delay Times (ϕ_d, $\bar{\phi}_d$)	(Note 2)	10.0			ns
Clock Transition Times (ϕt_r, ϕt_f)	$\phi t_f + \phi_{PW} + \phi t_r \leq 10.5\ \mu s$			1.0	μs
Partial Bit Times (T)	(Note 2)				
Input Partial Bit Time (T_{IN})		0.2		100	μs
Output Partial Bit Time (T_{OUT})		0.2		100	μs
Data Input Setup Time (t_{ds})		80	30		ns
Data Input Hold Time (t_{dh})		20	0		ns
Write Setup Time (t_{ds})		80	30		ns
Write Hold Time (t_{dh})		20	0		ns
Read Setup Time (t_{RS})		0			ns
Read Hold Time (t_{Rh})		0			ns
Data Output Propagation Delay from ϕ_{OUT}	(see ac test circuit)				
Delay to HIGH Level (t_{pd1})			150	200	ns
Delay to LOW Level (t_{pd0})			150	200	ns
Propagation Delay From Read Control Disable to HIGH Impedance State:					
Delay From HIGH Level (t_{1H})			150	200	ns
Delay From LOW Level (t_{0H})			150	200	ns
Propagation Delay From Read Control Enable to LOW Impedance State:					
Delay to HIGH Level (t_{H1})			150	200	ns
Delay to LOW Level (t_{H0})			150	200	ns

Note 1: Capacitance is guaranteed by periodic testing.

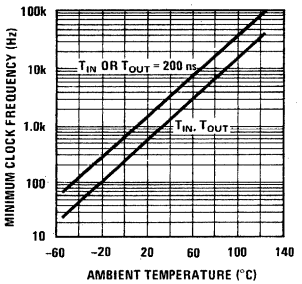
Note 2: Minimum clock frequency is a function of temperature and partial bit times (T_{IN} and T_{OUT}) as shown by the ϕ_f versus temperature and T_{IN}, T_{OUT} versus temperature curves. The lowest guaranteed clock frequency for any temperature can be attained by making T_{IN} equal to T_{OUT}. The minimum guaranteed clock frequency is:

$$\phi f(\text{min}) = \frac{1}{T_{IN} + T_{OUT}}$$, where T_{IN} and T_{OUT} do not exceed the guaranteed maximums.

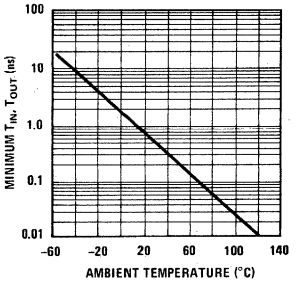
Note 3: Minimum clock frequency and partial bit time curves are guaranteed by testing at a high temperature point.

performance characteristics

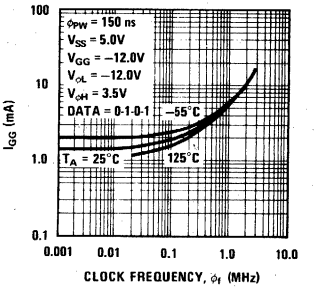
Guaranteed Minimum Clock Frequency vs Temperature (Note 2)



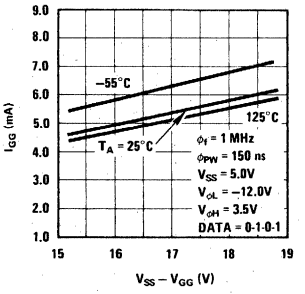
Guaranteed Maximum T_{IN} and T_{OUT} vs Temperature (Note 2)



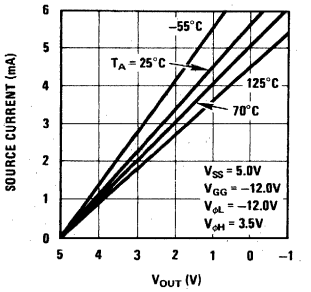
Typical Power Supply Current vs Clock Frequency



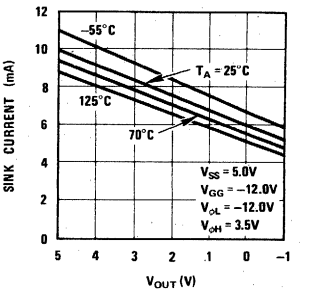
Typical Power Supply Current vs Voltage



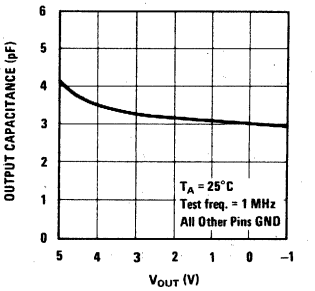
Typical Data Output Source Current vs Data Output Voltage



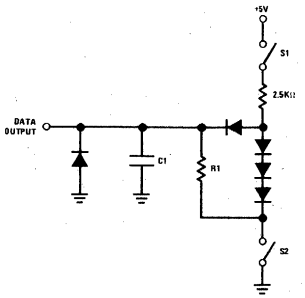
Typical Data Output Sink Current vs Data Output Voltage



Typical Tri-State Data Output Capacitance vs Voltage



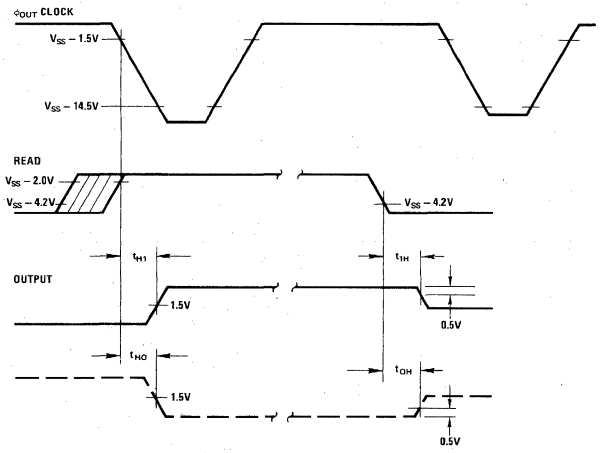
ac test circuit



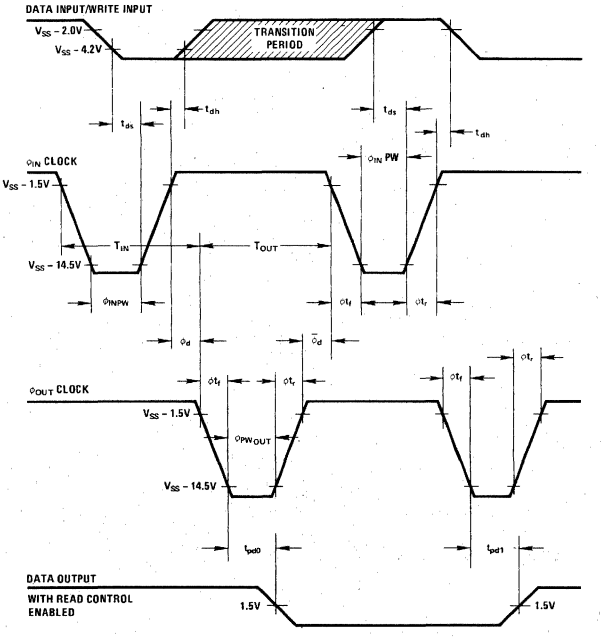
truth table

DELAY	S1	S2	R1	C1
t_{pd0}	Closed	Closed	35K	20 pF
t_{pd1}	Closed	Closed	35K	20 pF
t_{0H}	Closed	Closed	2.5K	5 pF
t_{1H}	Closed	Closed	2.5K	5 pF
t_{H0}	Closed	Open	35K	20 pF
t_{H1}	Open	Closed	35K	20 pF

switching time waveforms



The level of the output when it is in the high impedance state is determined by the external circuitry. The correct data will always appear, after some propagation delay, when the read control is enabled. The guaranteed delay from the high impedance state to the low impedance state requires that the read control is enabled on or before the leading edge of ϕ_{OUT}.



8

NATIONAL

Shift Registers

MM4015A/MM5015A triple 60+4 bit accumulator/register

general description

The MM4015A/MM5015A triple 60+4 bit dynamic accumulator is a monolithic MOS integrated circuit utilizing P-channel enhancement mode low threshold technology. The device consists of three independent shift registers with logic to control the entry of external data or to recirculate the data stored in that register. A common two phase clock is required to operate the device.

features

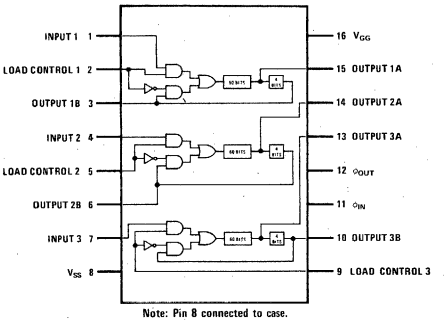
- Direct DTL and TTL compatibility — No pull-up or pull-down resistors required
- High frequency operation — 2.5 MHz guaranteed
- Low frequency operation — 250 Hz at 25°C, guaranteed
- Low power consumption — 0.4 mW/bit typically at 1 MHz
- Recirculate logic on-chip
- BCD correction look ahead tap

applications

- Data storage registers in BCD arithmetic applications
- Basic accumulator functions
- Business machine memory applications
- Recirculating delay line

connection diagram

Dual-In-Line Package



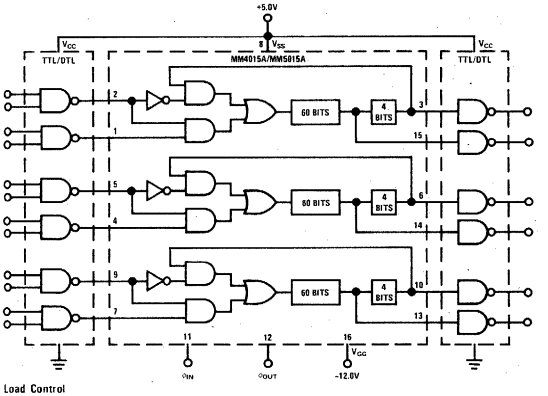
Note: Pin 8 connected to case.

TOP VIEW

Order Number MM4015AD or MM5015AD
See Package 3

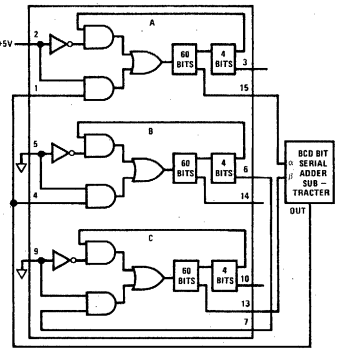
typical applications

TTL/MOS Interface



Load Control
Logical Low – Data is Loaded
Logical High – Data is Recirculated

Typical Arithmetic Configuration



The above circuit will generate the function:
A + C → B
B → C
A → A

absolute maximum ratings

Voltage at Any Pin		V_{SS} + 0.3V to V_{SS} − 22.0V
Operating Temperature Range	MM4015A	−55°C to +125°C
	MM5015A	0°C to +70°C
Storage Temperature Range		−65°C to +150°C

electrical characteristics

T_A within operating temperature range, V_{SS} = 5.0V ±5%, V_{GG} = −12.0V ±10%, unless otherwise stated

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Data Input Levels					
Logical HIGH Level (V_{IH})		V_{SS} − 2.0		V_{SS} + 0.3	V
Logical LOW Level (V_{IL})		V_{SS} − 18.5		V_{SS} − 4.2	V
Data Input Leakage	V_{IN} = −20.0V, T_A = 25°C, All Other Pins GND		0.01	0.5	μA
Data Input Capacitance	V_{IN} = 0.0V, f = 1 MHz, All Other Pins GND See Note 2		3.0	5.0	pF
Load Control Input Levels					
Logical HIGH Level (V_{IH})		V_{SS} − 2.0		V_{SS} + 0.3	V
Logical LOW Level (V_{IL})		V_{SS} − 18.5		V_{SS} − 4.2	V
Load Control Input Leakage	V_{IN} = −20.0V, T_A = 25°C, All Other Pins GND		0.01	0.5	μA
Load Control Input Capacitance	V_{IN} = 0.0V, f = 1 MHz, All Other Pins GND See Note 2		3.0	5.0	pF
Clock Input Levels					
Logical HIGH Level($V_{\phi H}$)		V_{SS} − 1.5		V_{SS} + 0.3	V
Logical LOW Level ($V_{\phi L}$)		V_{SS} − 18.5		V_{SS} − 14.5	V
Clock Input Leakage	V_ϕ = −20V, T_A = 25°C, All Other Pins GND		0.05	1.0	μA
Clock Input Capacitance	V_ϕ = 0.0V, f = 1 MHz, All Other Pins GND See Note 2		45.0	60.0	pF
Data Output Levels					
Logical HIGH Level (V_{OH})	I_{SOURCE} = −0.5 mA	2.4		V_{SS}	V
Logical LOW Level (V_{OL})	I_{SINK} = 1.6 mA			0.4	V
Power Supply Current I_{GG}	T_A = 25°C, V_{GG} = −12V, ϕ_{PW} = 150 ns, V_{SS} = +5.0V, $V_{\phi L}$ = −12V, Data = 0-1-0-1				
	0.01 MHz ≤ ϕ_f ≤ 0.1 MHz		2.2	3.0	mA
	ϕ_f = 1 MHz		4.5	5.5	mA
	ϕ_f = 2.5 MHz		7.0	8.5	mA
Clock Frequency (ϕ_f)	$\phi t_r = \phi t_f$ = 20 ns, Note 1	0.01	3.3	2.5	MHz
Clock Pulsewidth (ϕ_{PW})	$\phi t_f + \phi_{PW} + \phi t_r \leq 10.5\ \mu s$	0.15		10.0	μs
Clock Phase Delay Times (ϕ_d, $\overline{\phi}_d$)	Note 1	10			ns
Clock Transition Times (ϕt_r, ϕt_f)	$\phi t_f + \phi_{PW} + \phi t_r \leq 10.5\ \mu s$			1.0	μs
Partial Bit Times (T)	Note 1				
Input Partial Bit Time (T_{IN})		0.20		100	μs
Output Partial Bit Time (T_{OUT})		0.20		100	μs
Data Input Setup Time (t_{ds})		80	30		ns
Data Input Hold Time (t_{dh})		20	0		ns
Load Input Setup Time (t_{ls})		80	30		ns
Load Input Hold Time (t_{lh})		20	0		ns
Data Output Propagation Delay From ϕ_{OUT}					
Delay to HIGH Level (t_{pdH})			150	200	ns
Delay to LOW Level (t_{pdL})			150	200	ns

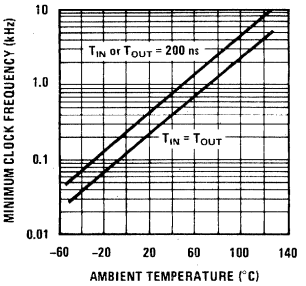
Note 1: Minimum clock frequency is a function of temperature and partial bit times (T_{IN} and T_{OUT}) as shown by the ϕ_f versus temperature and T_{IN}, T_{OUT} versus temperature curves. The lowest guaranteed clock frequency for any temperature can be attained by making T_{IN} equal to T_{OUT}. The minimum guaranteed clock frequency is:

$$\phi f(\text{min}) = \frac{1}{T_{IN} + T_{OUT}}$$, where T_{IN} and T_{OUT} do not exceed the guaranteed maximums.

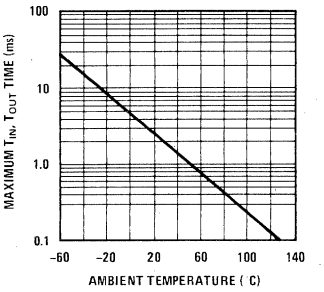
Note 2: Capacitance is guaranteed by periodic testing.

performance characteristics

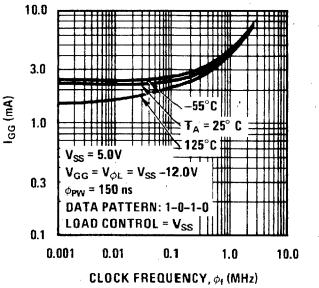
Typical Minimum Clock Frequency vs Temperature (Note 1)



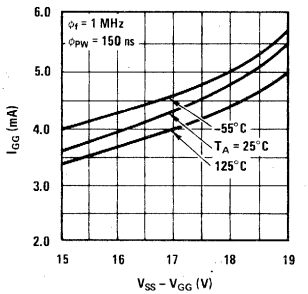
Typical Maximum Partial Bit Times vs Temperature (Note 1)



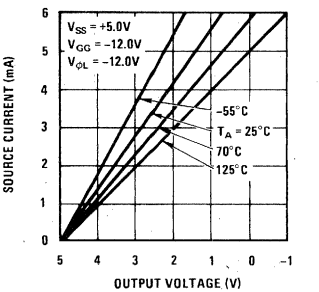
Power Supply Current vs Clock Frequency



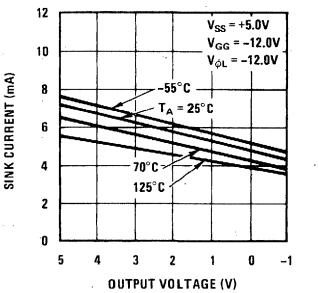
Power Supply Current vs Voltage



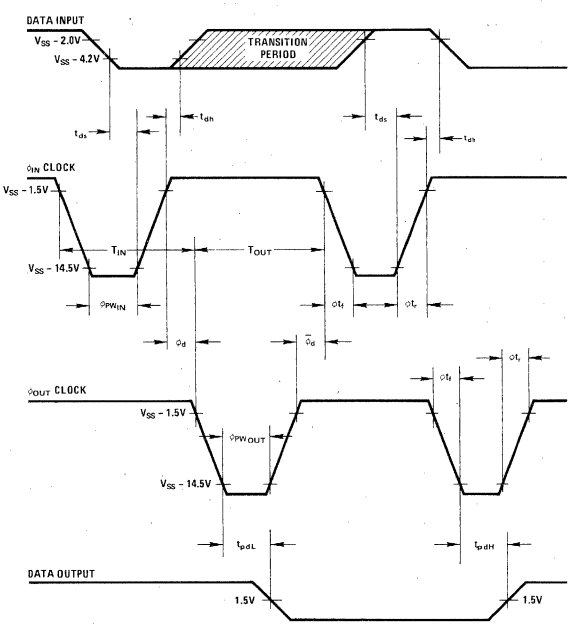
Data Output Source Current vs Voltage



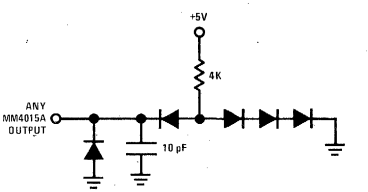
Data Output Sink Current vs Voltage



switching time waveforms



ac test circuit



Shift Registers

MM4016/MM5016 512-bit dynamic shift register

general description

The MM4016/MM5016 512-bit dynamic shift register is a monolithic MOS integrated circuit utilizing P channel enhancement mode low threshold technology to achieve bipolar compatibility. An input tap provides the option of using the device as either a 500 or 512-bit register.

features

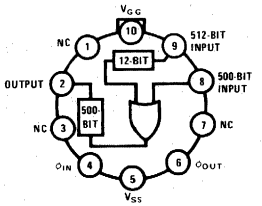
- Bipolar compatibility — +5V, −12V operation. No pull-up or pull-down resistors required.
- Package option — TO-100 or choice of two Dual-In-Line Packages
- Fewer clock drivers required — Clock line capacitance of 100 pF typ
- System flexibility — 300 Hz guaranteed min. operating frequency at 25°C. 500 or 512-bit register length.
- Military and Commercial Temperature Ranges
  MM4016 −55°C to +125°C
  MM5016 0°C to +70°C
- Low power dissipation — < 0.17 mW/bit at 1 MHz max. < 30 μW/bit at 100 kHz typ.

applications

- Glass and magnetostrictive delay line replacement.
- CRT refresh memory.
- Radar delay line.
- Drum memory storage (silicon store)
- Long serial memory.

connection diagrams

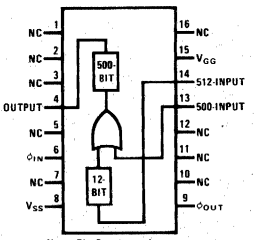
Metal Can Package



Note: Pin 5 connected to case.
TOP VIEW

Order Number MM4016H or MM5016H
See Package 24

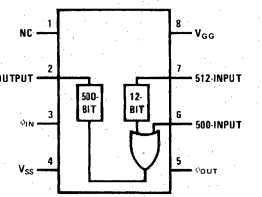
Dual-In-Line Package



Note: Pin 8 connected to case.
TOP VIEW

Order Number MM4016D or MM5016D
See Package 3

Dual-In-Line Package

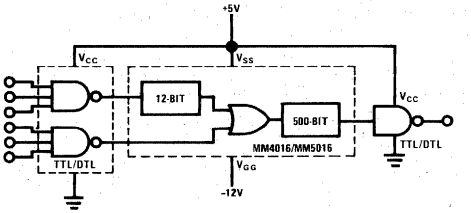


TOP VIEW

Order Number MM5016N
See Package 12

typical application

TTL/MOS Interface



Note: The unused input pin must be connected to V_{SS}.

absolute maximum ratings

Voltage at Any Pin		V_{SS} + 0.3V to V_{SS} −22V
Operating Temperature Range	MM4016	−55°C to +125°C
	MM5016	0°C to +70°C
Storage Temperature Range		−65°C to +150°C
Lead Temperature (Soldering, 10 sec)		300°C

electrical characteristics

T_A within operating temperature range, V_{SS} = +5.0V ±5%, V_{GG} = −12.0V ±10%, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Data Input Levels					
Logical HIGH Level (V_{IH})		V_{SS} − 2.0		V_{SS} + 0.3	V
Logical LOW Level (V_{IL})		V_{SS} − 18.5		V_{SS} − 4.2	V
Data Input Leakage	V_{IN} = − 20V, T_A = 25°C, All Other Pins GND		0.01	0.5	μA
Data Input Capacitance	V_{IN} = 0.0V, f = 1 MHz, All Other Pins GND, (Note 2)		3.0	5.0	pF
Clock Input Levels					
Logical HIGH Level ($V_{\phi H}$)		V_{SS} − 1.5		V_{SS} + 0.3	V
Logical LOW Level ($V_{\phi L}$)		V_{SS} − 18.5		V_{SS} − 14.5	V
Clock Input Leakage	V_ϕ = −20V, T_A = 25°C, All Other Pins GND		0.05	1.0	μA
Clock Input Capacitance	V_ϕ = 0.0V, f = 1 MHz, All Other Pins GND, (Note 2)		100	120	pF
Data Output Levels					
Logical HIGH Level (V_{OH})	I_{SOURCE} = −0.5 mA	2.4		V_{SS}	V
Logical LOW Level (V_{OL})	I_{SINK} = 1.6 mA			0.4	V
Power Supply Current					
I_{GG}	T_A = 25°C, V_{GG} = −12V, ϕ_{PW} = 150 ns, V_{SS} = 5.0V, $V_{\phi L}$ = −12V, Data = 0-1-0-1				
	0.01 MHz $\leq \phi_f \leq$ 0.1 MHz		1.0	2.0	mA
	ϕ_f = 1 MHz		3.5	5.0	mA
	ϕ_f = 2.5 MHz		7.0	10.0	mA
Clock Frequency (ϕ_f)	$\phi t_r = \phi t_f$ = 20 ns, (Note 1)	0.01	3.3	2.5	MHz
Clock Pulsewidth (ϕ_{PW})	$\phi t_f = \phi_{PW} + \phi t_r \leq$ 10.5 μs	0.15		10	μs
Clock Phase Delay Times (ϕ_d, $\bar{\phi}_d$)	(Note 1)	10			ns
Clock Transition Times (ϕt_r, ϕt_f)	$\phi t_f + \phi_{PW} + \phi t_r \leq$ 10.5 μs			1	μs
Partial Bit Times (T)	(Note 1)				
Input Partial Bit Time (T_{IN})		0.20		100	μs
Output Partial Bit Time (T_{OUT})		0.20		100	μs
Data Input Setup Time (t_{ds})		80	30		ns
Data Input Hold Time (t_{dh})		20	0		ns
Data Output Propagation Delay from ϕ_{OUT}	See ac test circuit.				
Delay to HIGH Level (t_{pdH})			150	200	ns
Delay to LOW Level (t_{pdL})			150	200	ns

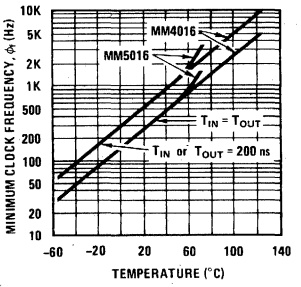
Note 1: Minimum clock frequency is a function of temperature and partial bit times (T_{IN} and T_{OUT}) as shown by the ϕ_f versus temperature and T_{IN}, T_{OUT} versus temperature curves. The lowest guaranteed clock frequency for any temperature can be attained by making T_{IN} equal to T_{OUT}. The minimum guaranteed clock frequency is:

$$\phi_{f(min)} = \frac{1}{T_{IN} + T_{OUT}}$$, where T_{IN} and T_{OUT} do not exceed the guaranteed maximums.

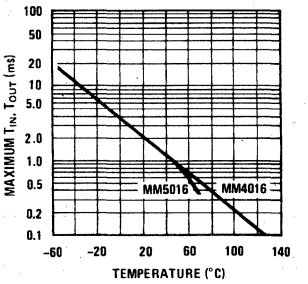
Note 2: Capacitance is guaranteed by periodic testing.

performance characteristics

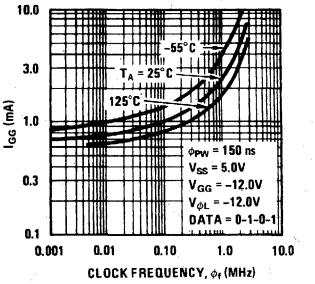
Typical Minimum Clock Frequency vs Temperature (Note 1)



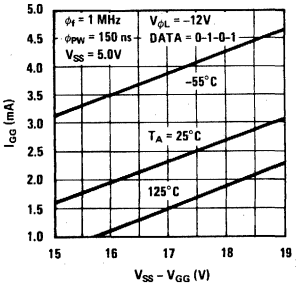
Typical Maximum T_{IN} and T_{OUT} vs Temperature (Note 1)



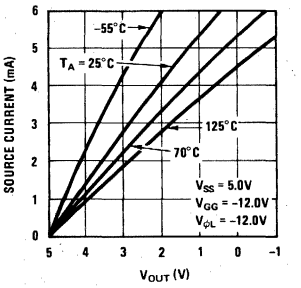
Typical Power Supply Current vs Clock Frequency



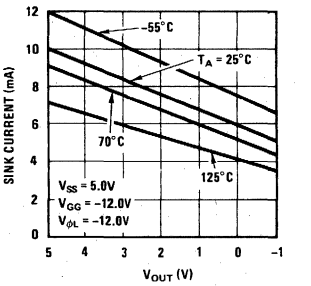
Typical Power Supply Current vs Voltage



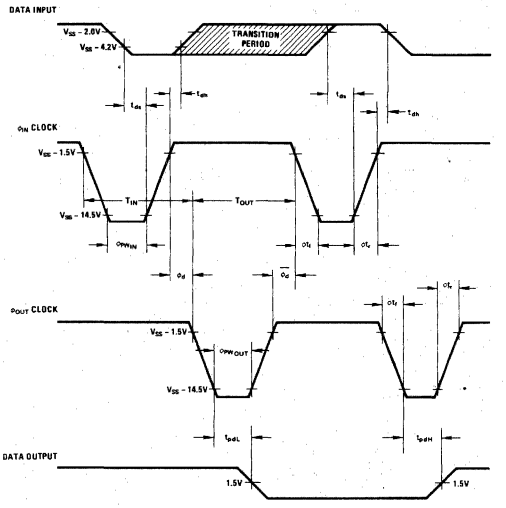
Typical Data Output Source Current vs Voltage



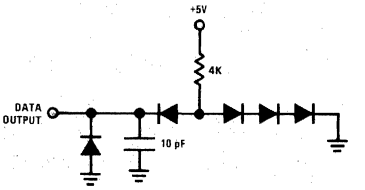
Typical Data Output Sink Current vs Voltage



switching time waveforms



ac test circuit



8

NATIONAL

Shift Registers

MM4017/MM5017 dual 512-bit dynamic shift register

general description

The MM4017/MM5017 dual 512-bit dynamic shift register is a monolithic MOS integrated circuit utilizing P channel enhancement mode low threshold technology to achieve bipolar compatibility. An input tap provides the option of using either register in a 500-bit or 512-bit configuration.

features

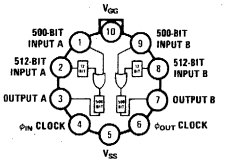
- Standard +5V, −12V supplies — Bipolar compatibility. No pull-up or pull-down resistors required.
- Package option TO-100 or Dual-In-Line Package.
- Fewer clock drivers required — Clock line capacitance of 140 pF typ.
- System flexibility — 400 Hz guaranteed min. operating frequency at 25°C. 500 or 512-bit register length.
- Military and Commercial Temperature Ranges
  MM4017 −55°C to +125°C
  MM5017 0°C to +70°C
- Low power dissipation — <0.17 mW/bit at 1 MHz max. < 30 μW/bit at 100 kHz typ.

applications

- Glass and magnetostrictive delay line replacement
- CRT refresh memory
- Radar delay line
- Drum memory storage (silicon store)
- Long serial memory

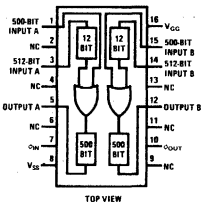
connection diagrams

Metal Can Package



Order Number MM4017H or MM5017H
See Package 24

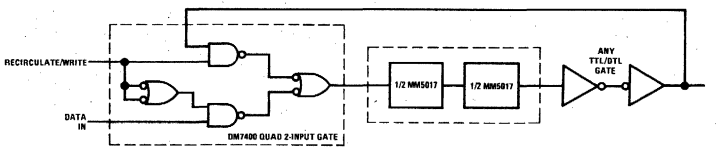
Dual-In-Line Package



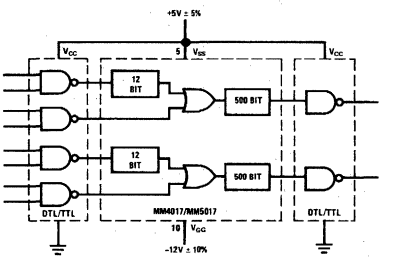
Order Number MM4017D or MM5017D
See Package 3
Order Number MM5017N
See Package 15

typical applications

1000 or 1024 Bit Accumulator



TTL/MOS Interface



Note: Unused input(s) should be tied to V_{SS}.

absolute maximum ratings

Voltage at Any Pin	V_{SS} + 0.3 to V_{SS} − 22
Operating Temperature MM4017	−55°C to +125°C
MM5017	0°C to +70°C
Storage Temperature	−65°C to 150°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics

T_A within operating temperature range, V_{SS} = +5.0V ±5%, V_{GG} = −12.0V ±10%, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Data Input Levels					
Logical HIGH Level (V_{IH})		V_{SS} − 2.0		V_{SS} + 0.3	V
Logical LOW Level (V_{IL})		V_{SS} −18.5		V_{SS} − 4.2	V
Data Input Leakage	V_{IN} = −20V, T_A = 25°C, All Other Pins GND		0.01	0.5	μA
Data Input Capacitance	V_{IN} = 0V, f = 1 MHz, All Other Pins GND		3.0	5.0	pF
Clock Input Levels					
Logical HIGH Level ($V_{\phi H}$)		V_{SS} − 1.5		V_{SS} + 0.3	V
Logical LOW Level ($V_{\phi L}$)		V_{SS} −18.5		V_{SS} − 14.5	V
Clock Input Leakage	V_ϕ = −20V, T_A = 25°C, All Other Pins GND		0.05	1.0	μA
Clock Input Capacitance	V_ϕ = 0V, f = 1 MHz, All Other Pins GND		140	160	pF
Data Output Levels					
Logical HIGH Level (V_{OH})	I_{SOURCE} = −0.5 mA	2.4		V_{SS}	V
Logical LOW Level (V_{OL})	I_{SINK} = 1.6 mA			0.4	V
Power Supply Current					
I_{GG}	T_A = 25°C, V_{GG} = −12V, ϕ_{PW} = 150 ns, V_{SS} = 5.0V, $V_{\phi L}$ = −12V, Data = 0-1-0-1				
	0.01 MHz ≤ ϕ_f ≤ 0.1 MHz		2.1	3.2	mA
	ϕ_f = 1 MHz		7.0	10.5	mA
	ϕ_f = 2.5 MHz		10.0	14.0	mA
Clock Frequency (ϕ_f)	$\phi t_r = \phi t_f$ = 20 ns, Note 1	0.01	3.3	2.5	MHz
Clock Pulsewidth (ϕ_{PW})	$\phi t_f + \phi_{PW} + \phi t_r \leq 10.5\ \mu s$	0.15		10	μs
Clock Phase Delay Times (ϕ_d, $\overline{\phi}_d$)	Note 1	10			ns
Clock Transition Times (ϕt_r, ϕt_f)	$\phi t_f + \phi_{PW} + \phi t_r \leq 10.5\ \mu s$			1.0	μs
Partial Bit Times (T)					
Input Partial Bit Time (T_{IN})		0.20		Note 1	μs
Output Partial Bit Time (T_{OUT})		0.20		Note 1	μs
Data Input Setup Time (t_{ds})		80	30		ns
Data Input Hold Time (t_{dh})		20	0		ns
Data Output Propagation Delay from ϕ_{OUT}	See ac test circuit				
Delay to HIGH Level (t_{pdH})			150	200	ns
Delay to LOW Level (t_{pdL})			150	200	ns

Note 1: Minimum clock frequency is a function of temperature and partial bit times (T_{IN} and T_{OUT}) as shown by the ϕ_f versus temperature and T_{IN}, T_{OUT} versus temperature curves. The lowest guaranteed clock frequency for any temperature can be attained by making T_{IN} equal to T_{OUT}. The minimum guaranteed clock frequency is:

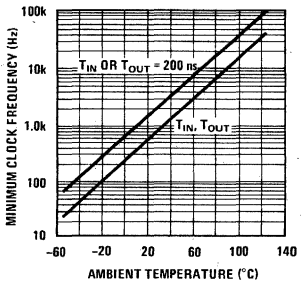
$$\phi f(min) = \frac{1}{T_{IN} + T_{OUT}}$$, where T_{IN} and T_{OUT} do not exceed the guaranteed maximums.

Note 2: The curves are guaranteed by testing at a high temperature point.

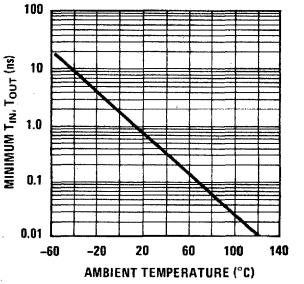
Note 3: Capacitance is guaranteed by periodic testing.

performance characteristics

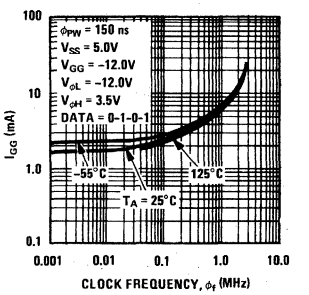
Guaranteed Minimum Clock Frequency vs Temperature (Notes 1 and 2)



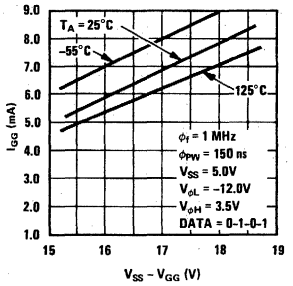
Guaranteed Maximum T_{IN} and T_{OUT} (Notes 1 and 2)



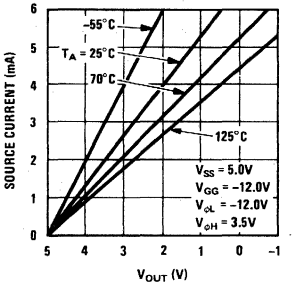
Typical Power Supply Current vs Clock Frequency



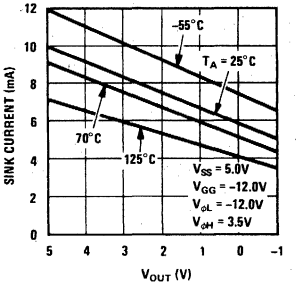
Typical Power Supply Current vs Voltage



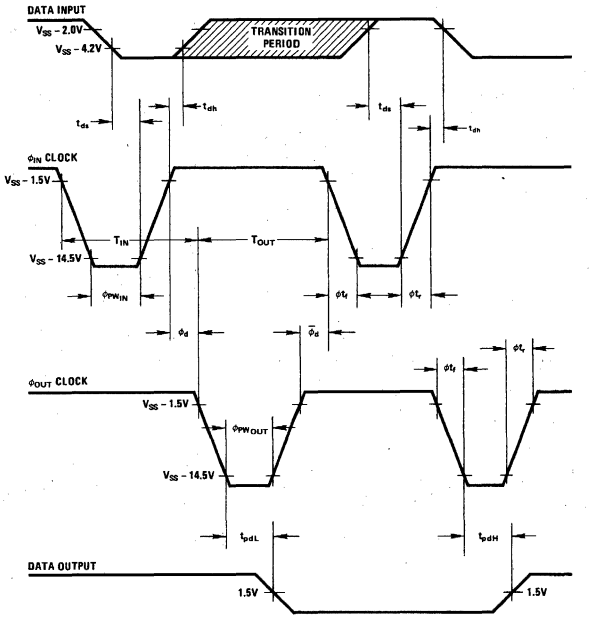
Typical Data Output Source Current vs Data Output Voltage



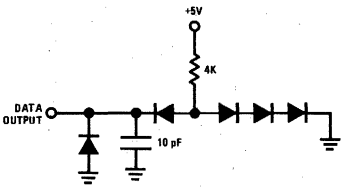
Typical Data Output Sink Current vs Data Output Voltage



switching time waveforms



ac test circuit



Shift Registers

Revised January 1976

MM4025/MM5025 dual 1024-bit dynamic shift register
MM4026/MM5026 dual 1024-bit dynamic shift register
MM4027/MM5027 2048-bit dynamic shift register

general description

These 2048-bit dynamic shift registers are MOS monolithic integrated circuits using P-channel silicon gate technology. They employ a push-pull output for bipolar compatability and on-chip multiplexing to achieve a 6 MHz data rate. The clock rate is one-half the data rate, i.e., one data bit is entered for each ϕ_1 and ϕ_2 clock pulse.

The MM4025/MM5025 and MM4027/MM5027 have on-chip logic to load and recirculate data.

The MM4026/MM5026 has an individual logic-select line to load one of the two inputs on each of the 1024-bit registers.

features

- Bipolar compatibility — Standard +5V, −12V power supplies
- High frequency of operation — 6 MHz guaranteed
- Low power dissipation — 120 μW/bit at 1 MHz ϕ rate 0°C, guaranteed
- Low clock capacitance — 190 pF max
- Wide operating temperature range
  MM4025,MM4026,MM4027 −55°C to +125°C
  MM5025,MM5026,MM5027 0°C to 70°C

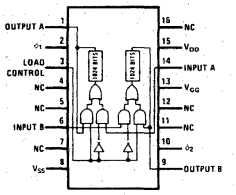
applications

- "Silicon store" replacement for drum and disc memories
- CRT displays
- Buffer memories

logic and connection diagrams

Military Temperature Range

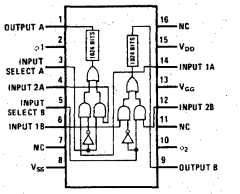
Dual-In-Line Package



TOP VIEW

Order Number MM4025D or MM5025D
See Package 3

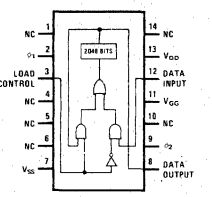
Dual-In-Line Package



TOP VIEW

Order Number MM4026D or MM5026D
See Package 3

Flat Package

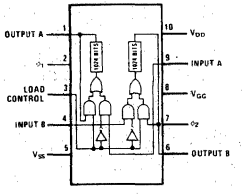


TOP VIEW

Order Number MM4027F or MM5027F
See Package 26

Commercial Temperature Range

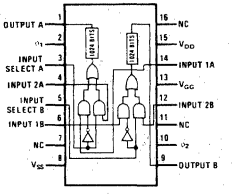
Dual-In-Line Package



TOP VIEW

Order Number MM5025N
See Package 13

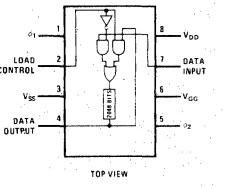
Dual-In-Line Package



TOP VIEW

Order Number MM5026N
See Package 15

Dual-In-Line Package



TOP VIEW

Order Number MM5027N
See Package 12

absolute maximum ratings

Voltage at Any Pin With Respect to V_{SS}	+0.3 to −20.0V
Operating Ambient Temperature Range	
MM4025,MM4026,MM4027	−55°C to +125°C
MM5025,MM5026,MM5027	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	300°C

electrical characteristics V_{SS} = +5.0V ± 5%, V_{DD} = GND, V_{GG} = −12.0V ±10%

T_A within operating temperature range unless otherwise stated.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Data Input Levels					
Logical High Level (V_{IH})		V_{SS}−1.5		V_{SS} + 0.3	V
Logical Low Level (V_{IL})		V_{SS}−10		V_{SS} − 4.2	V
Data Input Leakage	V_{IN} = −10V, T_A = 25°C, All other pins GND		0.01	1.0	μA
Data Input Capacitance	V_{IN} = 0V, f = 1 MHz, All other pins GND (Note 1)		2.5	5.0	pF
Load/Select Input Levels					
Logical High Level (V_{IH})		V_{SS}−1.5		V_{SS} + 0.3	V
Logical Low Level (V_{IL})		V_{SS} − 10		V_{SS} − 4.2	V
Load/Select Input Leakage	V_{IN} = −10V, T_A = 25°C, All other pins GND		0.01	1.0	μA
Load/Select Input Capacitance	V_{IN} = 0V, f = 1 MHz, All other pins GND (Note 1)		4.0	7.0	pF
Clock Input Levels					
Logical High Level ($V_{\phi H}$)		V_{SS} − 1.0		V_{SS} + 0.3	V
Logical Low Level ($V_{\phi L}$)		V_{SS} − 18.5		V_{SS} − 14.5	V
Clock Input Leakage	V_ϕ = −15V, T_A = 25°C, All other pins GND		.05	1.0	μA
Clock Input Capacitance	V_ϕ = 0V, f = 1 MHz, All other pins GND (Note 1)		165	190	pF
Data Output Levels					
Logical High Level (V_{OH})	I_{SOURCE} = −0.5 mA	2.4		V_{SS}	V
Logical Low Level (V_{OL})	I_{SINK} = 1.6 mA	0.0		0.4	V
Power Supply Current					
I_{GG}	T_A = 25°C, V_{GG} = −12.0V, ϕ_{PW} = 160 ns V_{SS} = 5.0V, $V_{\phi L}$ = −12.0V, DATA = Note 4 V_{DD} = 0.0V				
	0.01 MHz ≤ ϕ_f ≤ 0.1 MHz		2	3.5	mA
	ϕ_f = 1.0 MHz		2	3.5	mA
	ϕ_f = 3.0 MHz		2	3.5	mA
I_{DD}	0.01 MHz ϕ_f ≤ 0.1 MHz		8	15	mA
	ϕ_f = 1.0 MHz		22	32	mA
	ϕ_f = 3.0 MHz		48	70	mA
Clock Frequency (ϕ_f)					
MM4025,MM4026,MM4027	$\phi t_r = \phi t_f$ = 20 ns (Note 2, Note 3 & Note 5)	0.03	2.0	1.0	MHz
MM5025,MM5026,MM5027		0.003	4.0	1.25	MHz
Clock Pulsewidth (ϕ_{PW})					
MM4025,MM4026,MM4027	$\phi t_r = \phi t_f$ = 20 ns, Data Rate = 2 ϕ_f	0.240		8.0	μs
MM5025,MM5026,MM5027		0.240		10	μs
Clock Phase Delay Times (ϕ_d,$\overline{\phi}_d$)	See Curves	10			ns
Clock Transition Times (ϕt_r, ϕt_f)				0.5	μs
Partial Bit Times (T)	(Note 2, Note 3)				
T_1 Partial Bit Time					
MM4025,MM4026,MM4027		0.5		16.5	μs
MM5025,MM5026,MM5027		0.4		165	μs
T_2 Partial Bit Time					
MM4025,MM4026,MM4027		0.5		16.5	μs
MM5025,MM5026,MM5027		0.4		165	
Data & Load/Select Input Setup Time (t_{ds})		35			ns
Data & Load/Select Input Hold Time (t_{dh})		20			ns
Data Output Propogation Delay from ϕ					
Delay to High Level (t_{pdH})	15 pF Output Capacitance			160	ns
Delay to Low Level (t_{pdL})				160	ns

Note 1: Capacitance is guaranteed by periodic testing.

Note 2: Minimum clock frequency is a function of temperature and partial bit times (T_1 and T_2) as shown by ϕ_f versus temperature and T_1, T_2 versus temperature curves. The lowest guaranteed clock frequency for any temperature can be attained by making T_1 equal to T_2. The minimum guaranteed clock frequency: $\phi_{f\ (min)} = 1/(T_1 + T_2)$ where T_1 and T_2 do not exceed the guaranteed maximum.

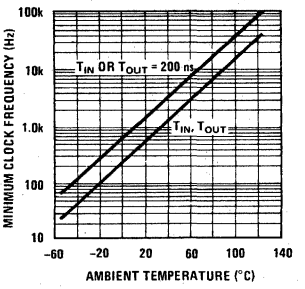
Note 3: Minimum clock frequency and partial bit time curves are guaranteed by testing at a high temperature point.

Note 4: For data pattern of 1111000011110000 etc.

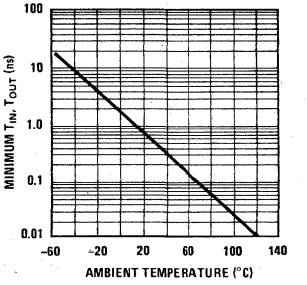
Note 5: Maximum frequency limited by maximum package power dissipation for MM4025, MM4026 and MM4027.

guaranteed performance characteristics

Typical Minimum Clock Frequency vs Temperature (Note 2)

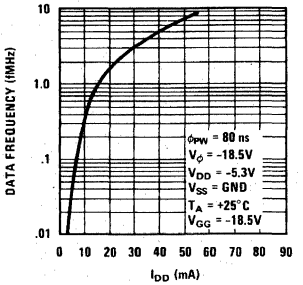


Typical Maximum T_1 and T_2 vs Temperature (Note 2)

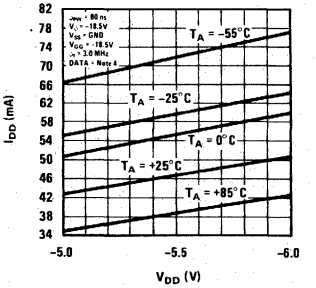


typical performance characteristics

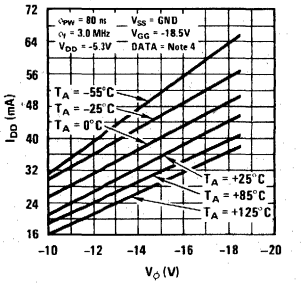
Power Supply Current vs Data Rate



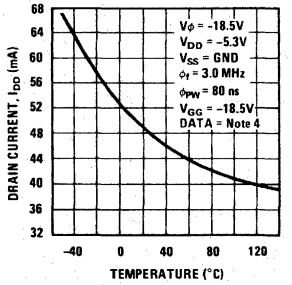
Power Supply Current vs V_{DD}



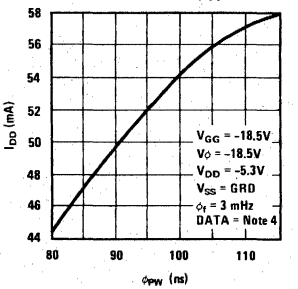
Power Supply Current vs Clock Voltage V_ϕ



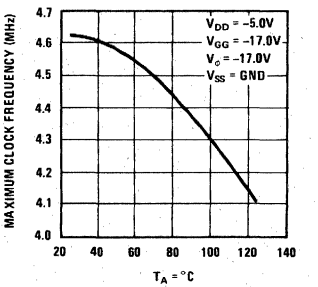
Power Supply Current vs Temperature



Power Supply Current vs Clock Pulse Width ϕ_{PW}



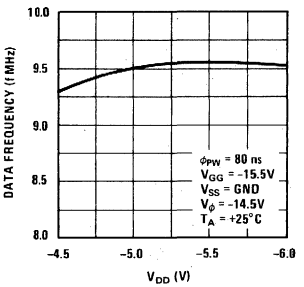
Maximum Clock Frequency vs Temperature



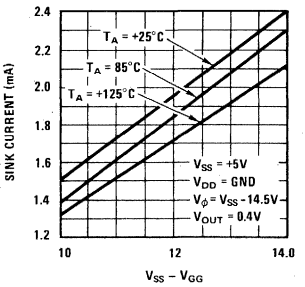
8

typical performance characteristics (con't)

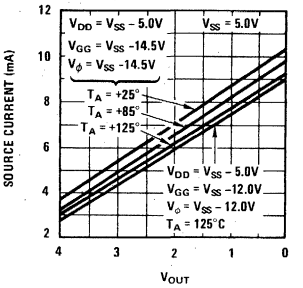
Maximum Data Rate vs V_{DD}



Typical Sink Current vs V_{GG}

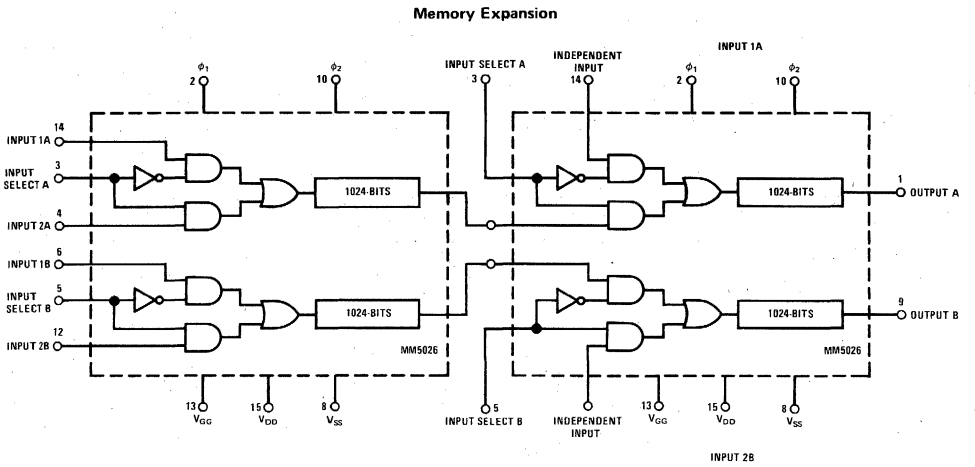


Typical Data Output Source Current vs Data Output Voltage

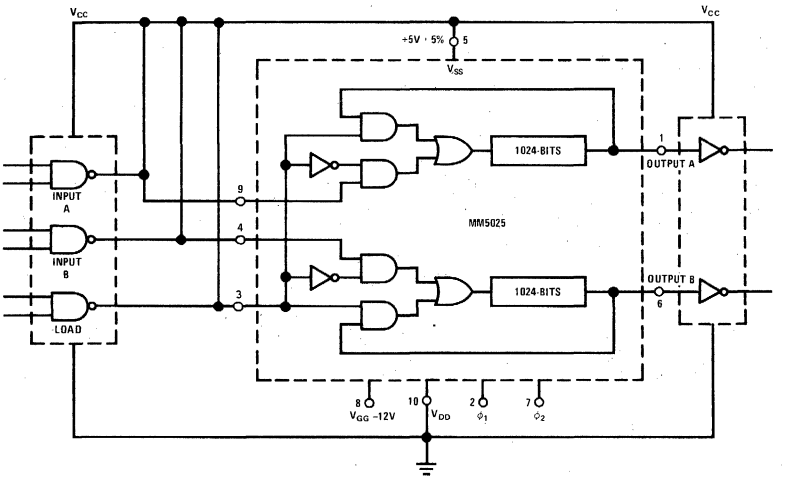


typical applications

Memory Expansion



TTL/MOS Interface



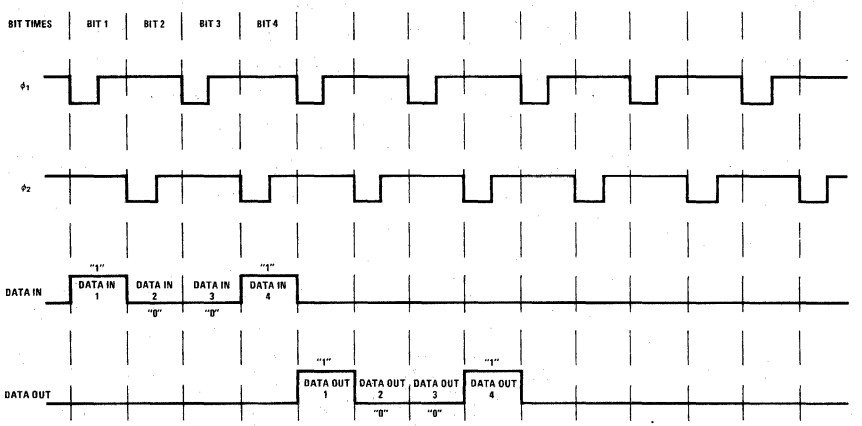
truth tables

Positive Logic
Logic "1" = V_{IH} = Logical High Level
Logic "0" = V_{IL} = Logical Low Level

Write/Recirculate	Function
1	Recirculate
0	Load Data

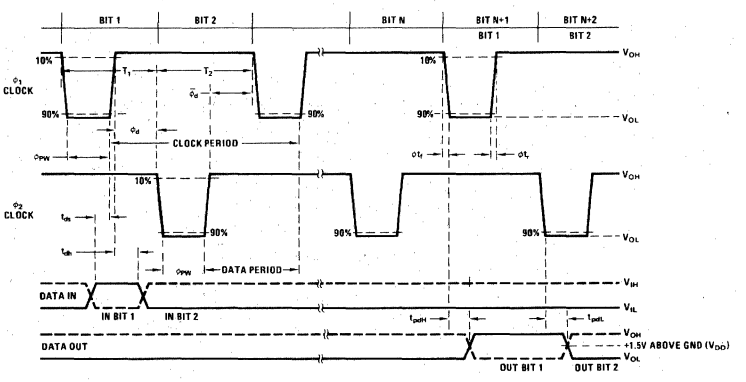
Input Select A	Function
1	Select Input 2A
0	Select Input 1A
Input Select B	**Function**
1	Select Input 2B
0	Select Input 1B

switching time waveforms



Shown is a simplified illustration of the timing of a 4-bit multiplexed register showing input output relationships with respect to the clock. If data enters the register at ϕ_1 time, it exits at ϕ_1 time, (beginning on $\phi_{1's}$ negative going edge and ending on the succeeding $\phi_{2's}$ negative going edge).

timing diagram



NATIONAL

Shift Registers

MM4040/MM5040 dual 16-bit static shift register

general description

The MM4040/MM5040 dual 16-bit static shift register is a monolithic integrated circuit utilizing P channel enhancement mode low threshold technology to achieve direct bipolar compatibility on the inputs and outputs. The device requires only a single phase clock.

features

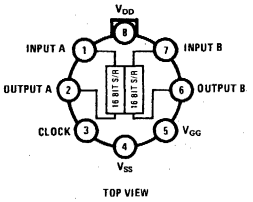
- Bipolar compatibility — +5, −12V operation; No pull-up or pull-down resistors needed
- High frequency operation — 2.2 MHz guaranteed
- Single phase clock

applications

- Static data buffer
- Serial memory storage
- Printer memory
- Telemetry systems and data sampling

connection diagram

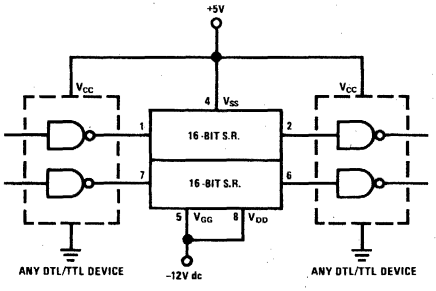
Metal Can Package



TOP VIEW

Order Number MM4040H or MM5040H
See Package 23

typical application



absolute maximum ratings

Voltage at Any Pin		V_{SS} + 0.3V to V_{SS} − 22
Operating Temperature Range	MM4040	−55°C to +125°C
	MM5040	0°C to +70°C
Storage Temperature Range		−65°C to +150°C
Lead Temperature (Soldering, 10 sec)		300°C

electrical characteristics

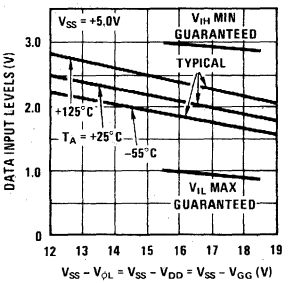
T_A within operating temperature range, V_{SS} = +5.0V ±5%, V_{SS} − V_{DD} = 9V to 18.5V, V_{GG} = −12V ±10%, unless otherwise specified

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Data Input Levels					
Logical High Level (V_{IH})		V_{SS} − 2.0		V_{SS} + 0.3	V
Logical Low Level (V_{IL})		V_{SS} − 18.5		V_{SS} − 4.2	V
Data Input Leakage	V_{IN} = −20V, T_A = 25°C, All Other Pins GND			0.5	μA
Data Input Capacitance	V_{IN} = 0.0V, f = 1 MHz, All Other Pins GND (Note 1)		2.5	5.0	pF
Clock Input Levels					
Logical High Level ($V_{\phi H}$)		V_{SS} − 1.5		V_{SS} + 0.3	V
Logical Low Level ($V_{\phi L}$)		V_{SS} − 18.5		V_{SS} − 14.5	V
Clock Input Leakage	V_ϕ = −20V, T_A = 25°C, All Other Pins GND			1.0	μA
Clock Input Capacitance	V_ϕ = 0.0V, f = 1 MHz, All Other Pins GND (Note 1)		19	22	pF
Data Output Levels					
Logical High Level (V_{OH})	I_{SOURCE} = −0.5 mA	2.4			V
Logical Low Level (V_{OL})	I_{SINK} = 1.6 mA			0.4	V
Power Supply Current	T_A = +25°C, V_{GG} = −12V, ϕ_{PW} = 200 ns, V_{SS} = 5V, V_{DD} = −12V, $V_{\phi L}$ = −12V, Data = 0–1–0–1				
I_{GG}	0.01 MHz ≤ ϕ_f ≤ 0.1 MHz		1.0	2.0	mA
	ϕ_f = 1.0 MHz		1.8	3.0	mA
	ϕ_f = 2.0 MHz		3.0	4.0	mA
I_{DD}	0.01 MHz ≤ ϕ_f ≤ 0.1 MHz		5.0	9.0	mA
	ϕ_f = 1.0 MHz		5.1	9.0	mA
	ϕ_f = 2.0 MHz		5.2	9.0	mA
Clock Frequency (ϕ_f)	$\phi t_r = \phi t_f$ = 20 ns	DC	3.0	2.2	MHz
Clock Pulsewidth (ϕ_{PW})	$\phi t_r + \phi t_f + \phi_{PW} \leq$ 10.5 ns	.200	.100	10.0	μs
Clock Transition Times ($\phi t_r + \phi t_f$)	$\phi t_r + \phi t_f + \phi_{PW} \leq$ 10.5 ns			1.0	μs
Data Input Setup Time (t_{ds})		120	60		ns
Data Input Hold Time (t_{dh})		20	0		ns
Data Output Propagation Delay from ϕ	See test circuit				
Delay to High Level (t_{pdH})			200	300	ns
Delay to Low Level (t_{pdL})			200	300	ns

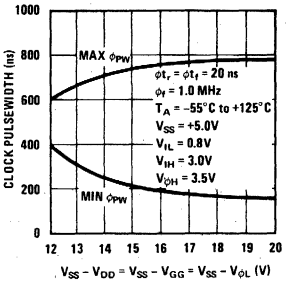
Note 1: Capacitance values are guaranteed by statistical lot sample testing.

guaranteed performance characteristics

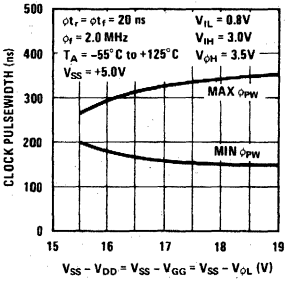
Data Input Levels vs Supply Voltage



1.0 MHz Operating Curve

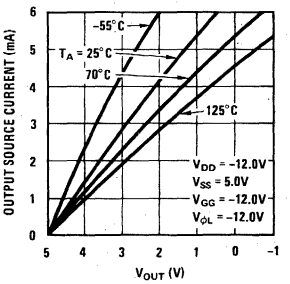


2.0 MHz Operating Curve

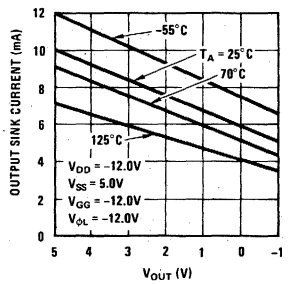


typical performance characteristics

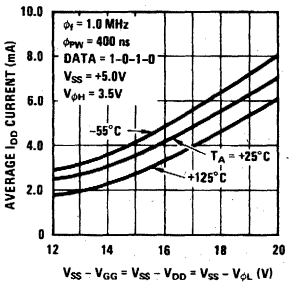
Data Output Source Current vs Voltage



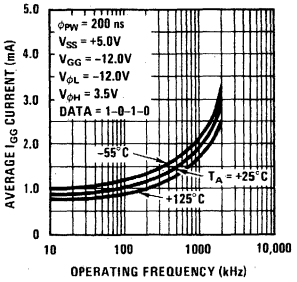
Data Output Sink Current vs Voltage



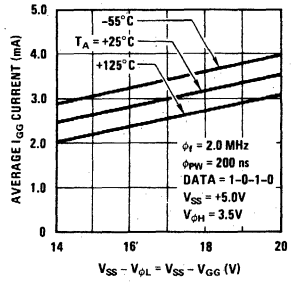
Power Supply Current vs Voltage



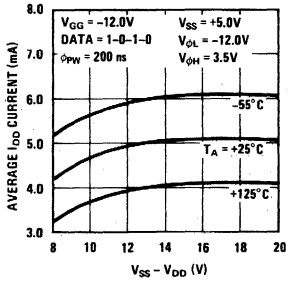
Power Supply Current vs Operating Frequency



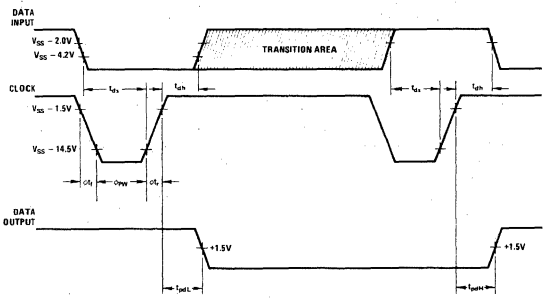
Power Supply Current



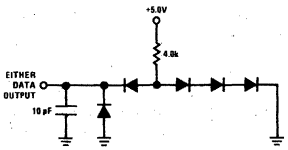
Power Supply Current



switching time waveforms



test circuit



Shift Registers

MM4050A/MM5050A dual 32-bit static shift register
MM4051A/MM5051A dual 32-bit static shift register—split clock

general description

The MM4050A/MM5050A and MM4051A/MM5051A dual 32-bit static shift registers are monolithic MOS integrated circuits utilizing P channel enhancement mode low threshold technology to achieve bipolar compatibility. Operation to 2.2 MHz is achieved with a single phase clock. The MM4051A/MM5051A is a bonding option of the MM4050A/MM5050A to provide independent clock control of each register.

features

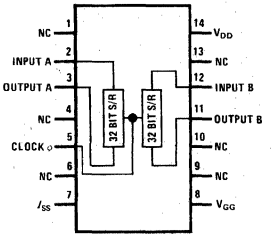
- Bipolar compatibility — +5V, −12V operation; No pull-up or pull-down resistors needed
- High frequency operation — dc to 2.2 MHz
- Single phase clock
- Improved drive capability — Push-pull outputs
- Military and commercial temperature ranges
  - MM4050A, MM4051A — −55°C to +125°C
  - MM5050A, MM5051A — 0°C to +70°C

applications

- Serial memory storage
- Printer memory
- Telemetry systems and data sampling

logic and connection diagrams

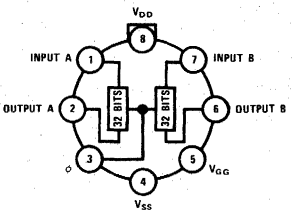
Dual-In-Line Package



TOP VIEW

Order Number MM4050AD or MM5050AD
See Package 2

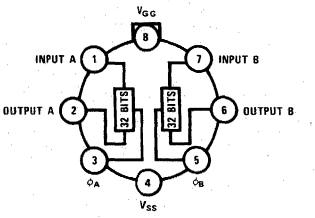
Metal Can Package



TOP VIEW

Order Number MM4050AH or MM5050AH
See Package 23

Metal Can Package

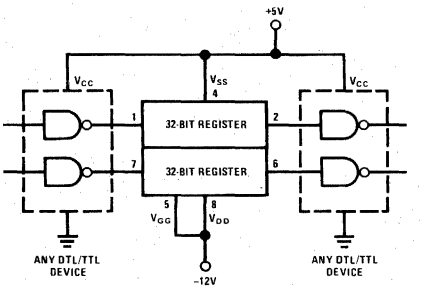


TOP VIEW

Order Number MM4051AH or MM5051AH
See Package 23

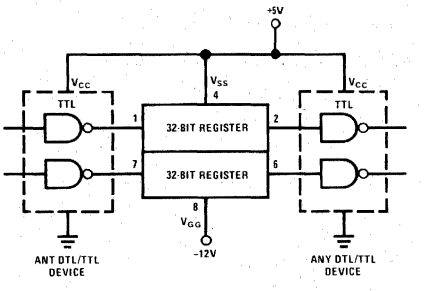
typical applications

TTL/MOS Interface



MM4050A/MM5050A

TTL/MOS Interface



MM4051A/MM5051A

absolute maximum ratings

Voltage at Any Pin	V_{SS} + 0.3V to V_{SS} − 22V
Operating Temperature Range MM4050A/MM4051A	−55°C to +125°C
MM5050A/MM5051A	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics

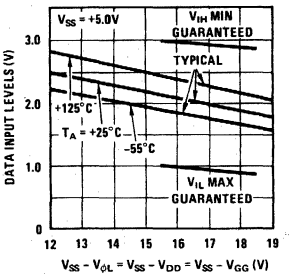
T_A within operating temperature range, V_{SS} = +5.0V ±5%, V_{SS} − V_{DD} = 9V to 18.5V, V_{GG} = −12V ±10%, unless otherwise stated.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Data Input Levels					
Logical HIGH Level (V_{IH})		V_{SS} − 2.0		V_{SS} + 0.3	V
Logical LOW Level (V_{IL})		V_{SS} − 18.5		V_{SS} − 4.2	V
Data Input Leakage	V_{IN} = −20V, T_A = 25°C, All Other Pins GND			0.5	μA
Data Input Capacitance	V_{IN} = 0.0V, f = 1 MHz, All Other Pins GND (Note 1)		2.5	5.0	pF
Clock Input Levels					
Logical HIGH Level ($V_{\phi H}$)		V_{SS} − 1.5		V_{SS} + 0.3	V
Logical LOW Level ($V_{\phi L}$)		V_{SS} − 18.5		V_{SS} −14.5	V
Clock Input Leakage	V_ϕ = −20V, T_A = 25°C, All Other Pins GND			1.0	μA
Clock Input Capacitance	V_ϕ = 0.0V, f = 1 MHz, All Other Pins GND (Note 1)		25	35	pF
Data Output Levels					
Logical HIGH Level (V_{OH})	I_{SOURCE} = −0.5 mA	2.4			V
Logical LOW Level (V_{OL})	I_{SINK} = 1.6 mA			0.4	V
Power Supply Current					
I_{GG}	T_A = +25°C, V_{GG} = −12.0V, ϕ_{PW} = 200 ns, V_{SS} = +5.0V, $V_{\phi L}$ = −12.0V, Data = 0-1-0-1, V_{DD} = −12.0V				
	0.01 MHz ≤ ϕ_f ≤ 0.1 MHz		1.6	3.5	mA
	ϕ_f = 1.0 MHz		3.8	8	mA
	ϕ_f = 2.0 MHz		4.6	11.0	mA
I_{DD}	0.01 MHz ≤ ϕ_f ≤ 0.1 MHz		2.7	5.0	mA
	ϕ_f ≤ 1.0 MHz		2.9	5.0	mA
	ϕ_f ≤ 2.0 MHz		3.1	5.0	mA
Clock Frequency (ϕ_f)	ϕt_r = ϕt_f = 20 ns	DC	3.0	2.2	MHz
Clock Pulsewidth (ϕ_{PW})	ϕt_r + ϕt_f + ϕ_{PW} ≤ 10.5 μs	0.2	0.100	10.0	μs
Clock Transition Times (ϕt_r, ϕt_f)	ϕt_r + ϕt_f + ϕ_{PW} ≤ 10.5 μs			1.0	μs
Data Input Setup Time (t_{ds})		80	50		ns
Data Input Hold Time (t_{dh})		20	0		ns
Data Output Propagation Delay From ϕ					
Delay to HIGH Level (t_{pdH})	See ac test circuit		150	300	ns
Delay to LOW Level (t_{pdL})			150	300	ns

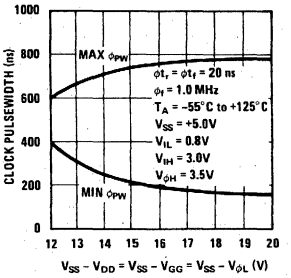
Note 1: Capacitance values are guaranteed by periodic testing.

guaranteed performance characteristics

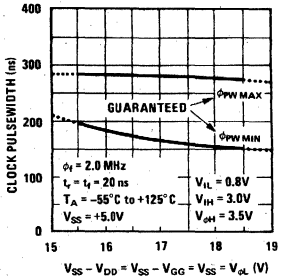
Data Input Voltage vs Supply



1.0 MHz Operating Curve

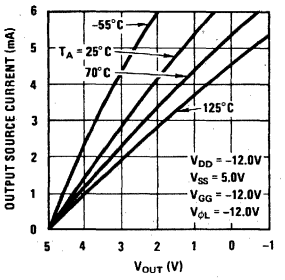


2.0 MHz Operating Curve

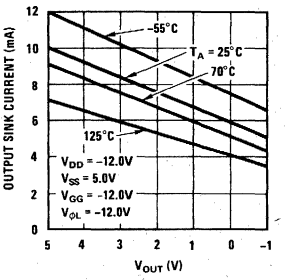


typical performance characteristics

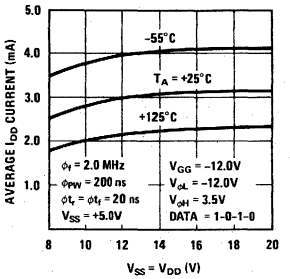
Data Output Source Current vs Voltage



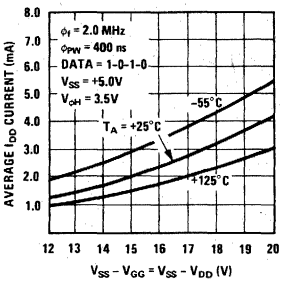
Output Sink Current vs Voltage



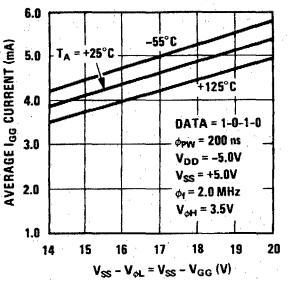
Power Supply Current



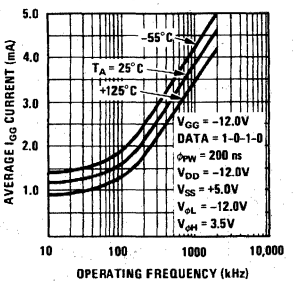
Power Supply Current vs Voltage



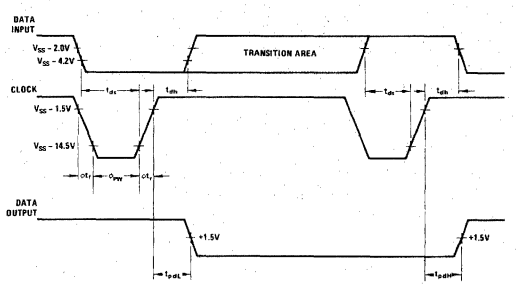
Power Supply Current



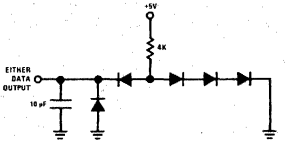
Power Supply Current vs Operating Frequency



switching time waveforms



ac test circuit



8

NATIONAL

Shift Registers

MM4052/MM5052 dual 80 bit static shift register
MM4053/MM5053 dual 100-bit static shift register

general description

The MM4052/MM5052 dual 80-bit and MM4053/MM5053 dual 100-bit static shift registers are monolithic integrated circuits utilizing P channel enhancement mode low threshold technology to achieve direct bipolar compatibility on the inputs and outputs. The devices require only a single phase clock.

features

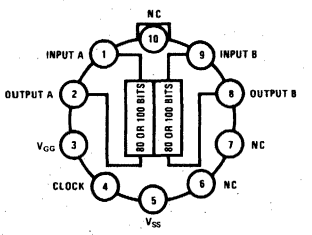
- Bipolar compatibility — +5, −12V operation; No pull-up or pull-down resistors needed
- High frequency operation — 1.6 MHz guarantee
- Single phase clock
- Improved drive capability — push-pull outputs

applications

- Static data buffer
- Serial memory storage
- Printer memory
- Telemetry systems and data sampling

connection diagram

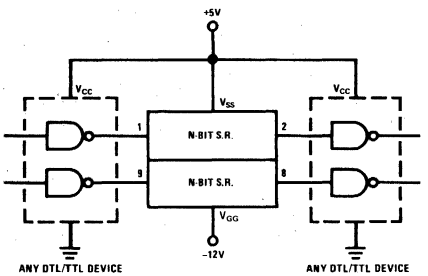
Metal Can Package



TOP VIEW

Order Number MM4052H, MM5052H, MM4053H or MM5053H
See Package 24

typical application



absolute maximum ratings

Voltage @ Any Pin	V_{SS} +0.3V to V_{SS} −22V
Operating Temperature Range	
MM4052/MM4053	−55°C to +85°C (Ambient) −55°C to +125°C (Case)
MM5052/MM5053	0°C to +70°C (Ambient)
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

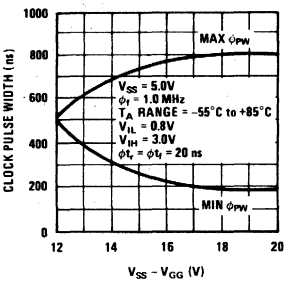
electrical characteristics

T_A within operating temperature range, V_{SS} = +5.0V ±5% and V_{GG} = −12V ±10%, unless otherwise specified.

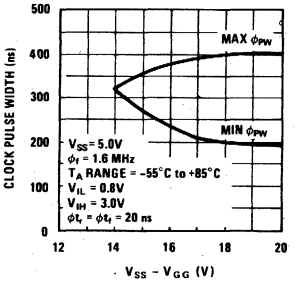
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Data Input Levels					
Logical High Level (V_{IH})		V_{SS} − 2.0			V
Logical Low Level (V_{IL})		V_{SS} − 18.5		V_{SS} − 4.2	V
Data Input Leakage	V_{IN} = −20V, T_A = 25°C All other pins GND		.01	0.5	μA
Data Input Capacitance	V_{IN} = 0.0V, f = 1.0 MHz All other pins GND		3.0	5.0	pF
Clock Input Levels					
Logical High Level ($V_{\phi H}$)		V_{SS} − 1.5		V_{SS}	V
Logical Low Level ($V_{\phi L}$)		V_{SS} − 18.5		V_{SS} − 14.5	V
Clock Input Leakage	V_{IN} = −20V, T_A = 25°C All other pins GND			1.0	μA
Clock Input Capacitance	V_{IN} = 0.0V, f = 1.0 MHz All other pins GND		22	28	pF
Data Output Levels					
Logical High Level (V_{OH})	I_{SOURCE} = −500 μA	2.4V	4.8	V_{SS}	V
Logical Low Level (V_{OL})	I_{SINK} = 1.6 mA		−3.0	0.4	V
Logical High Level (V_{OH})	I_{SOURCE} = −10 μA	V_{SS} − 1.0	V_{SS}	V_{SS}	V
Logical Low Level (V_{OL})	I_{SINK} = 10 μA		V_{SS} − 12.0	V_{SS} − 7.0	V
Power Supply Current	T_A = 25°C ϕ_f = 1.6 MHz				
(I_{GG}) MM4052/MM5052	V_{GG} = V_{SS} − 17V $V_{\phi L}$ = V_{SS} − 17V		9.5	12.5	mA
(I_{GG}) MM4053/MM5053			12.0	16.0	mA
Propagation Delays from Clock					
Propagation Delay to a High (t_{pdH})	See waveform		200	300	ns
Propagation Delay to a Low (t_{pdL})	See waveform		200	300	ns
Clock Frequency (ϕ_f)	See operating curves	0		1.6	MHz
Clock Pulse Width (ϕ_{PW})	See operating curves $\phi t_f + \phi_{PW} + \phi t_r \leq 10.5\ \mu s$	0.25		10	μs
Clock Transition Times					
Risetime (ϕt_r)	$\phi t_f + \phi_{PW} + \phi t_r \leq 10.5\ \mu s$			5	μs
Falltime (ϕt_f)	$\phi t_f + \phi_{PW} + \phi t_r \leq 10.5\ \mu s$			5	μs
Data Input Setup Time (t_{ds})		80	50		ns
Data Input Hold Time (t_{dh})		20	0		ns

guaranteed performance characteristics

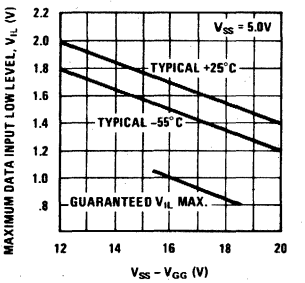
1.0 MHz Operating Curve



1.6 MHz Operating Curve

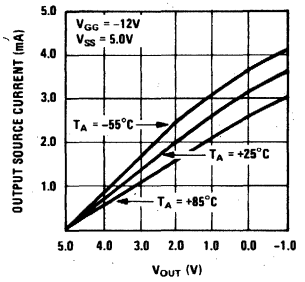


Maximum Data Input Low Level vs Supply Voltage

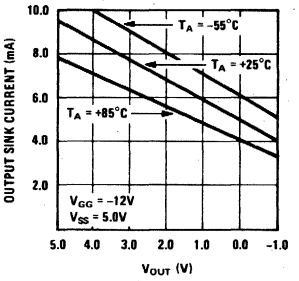


typical performance characteristics

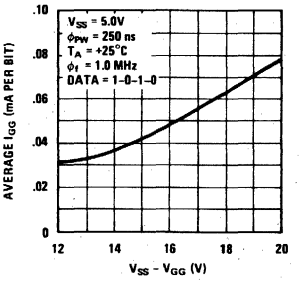
Data Output Source Current vs Data Output Voltage



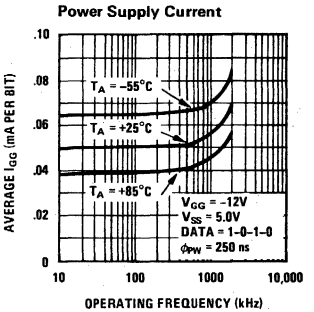
Data Output Sink Current vs Data Output Voltage



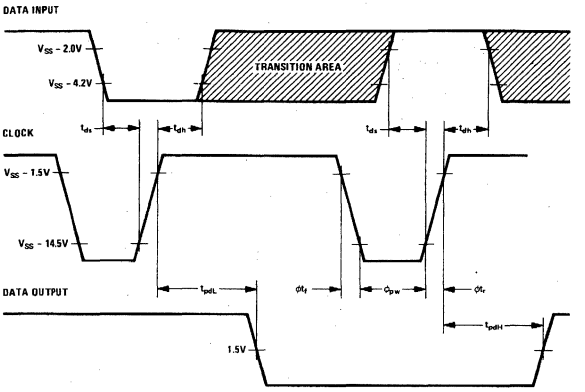
Power Supply Current



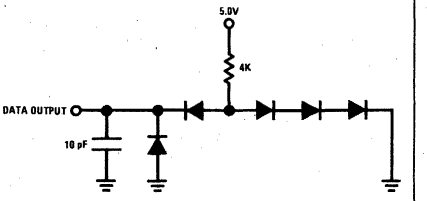
Power Supply Current



switching time waveforms



ac test circuit



Shift Registers

MM5054 dual 64/72/80-bit static shift register

general description

The MM5054 dual 80-bit static shift register is a monolithic MOS integrated circuit utilizing silicon gate low threshold technology to achieve complete bipolar compatibility. The device has input and output taps that also provide register lengths of 64 or 72 bits.

The single phase bipolar compatible clock lines may be driven by any conventional DTL or TTL circuit. The registers may be operated as a dual register by connecting the clock lines A and B together, or as two independent registers. Two clock control lines provide independent logical control of the shift register clock lines.

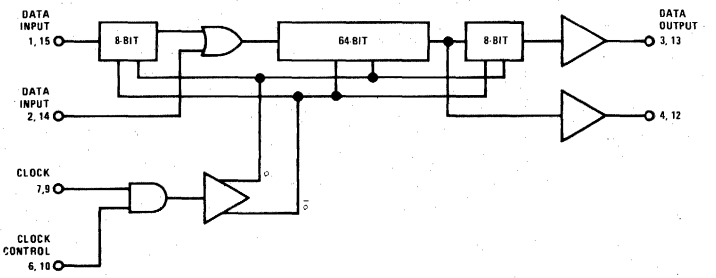
features

- Complete bipolar compatibility — DTL/TTL input/output and clock line compatibility without additional components
- Standard supplies — +5.0V, −12V
- High freq. operation — DC to 3.0 MHz typ
- Single phase clock — DTL/TTL compatible on-chip clock driver
- Low clock line capacitance — 8.0 pF max
- System flexibility — Split clock or common clock operation. Logical control of clock lines
- Low power dissipation — <600 μW/bit typ

applications

- Teletype data buffers
- Printer memory — 80, 128, 136, 144 bit lengths
- Telemetry and data sampling systems
- Serial memory storage

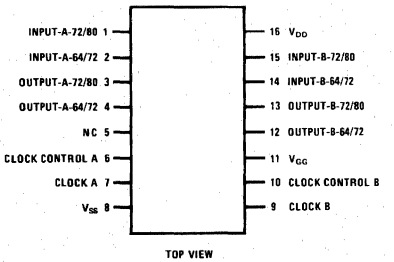
logic diagram



The unused data inputs and clock controls should be connected to V_{SS} to ensure proper operation.
Logic diagram shows 1/2 of the unit.

connection diagram

Dual-In-Line Package



TOP VIEW

Order Number MM5054D
See Package 3
Order Number MM5054N
See Package 15

truth table

Positive Logic

CLOCK CONTROL	CLOCK
Low	Inhibited
High	Active

absolute maximum ratings

Voltage at Any Pin	V_{SS} + 0.3V to V_{SS} − 20V
Operating Ambient Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C
Power Dissipation	600 mW @ 25°C

dc electrical characteristics

T_A within operating range, V_{GG} = −12V ±10%, V_{DD} = GND, V_{SS} = 5.0V ±5%, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Data, Clock Control, and Clock Levels					
Logical High Level (V_{IH})		V_{SS} − 1.5		V_{SS} + 0.3	V
Logical Low Level (V_{IL})				V_{SS} − 4.2	V
Input Leakages	V_{IN} = −10V, T_A = 25°C All Other Pins GND			0.5	μA
Data Input Capacitance	V_{IN} = 0V, f = 1.0 MHz All Other Pins GND (Note 1)		4.5	6.0	pF
Clock and Clock Control Capacitance	V_{IN} = 0V, f = 1.0 MHz (Note 1)		6.0	8.0	pF
Data Output Levels	(Figure 1)				
Logical High Level (V_{OH})	I_{SOURCE} = −0.5 mA	2.4		V_{SS}	V
Logical Low Level (V_{OL})	I_{SINK} = 1.6 mA		0.15	0.4	V
Power Supply Current	ϕ_f = 1.5 MHz, T_A = 25°C				
(I_{GG} + I_{DD} = I_{SS}) I_{GG}	V_{SS} = 5.0V, V_{DD} = GND		7.0	10	mA
I_{DD}	V_{GG} = −12V		5.0	8.0	mA

ac electrical characteristics

T_A within operating range, V_{GG} = −12V ±10%, V_{DD} = GND, V_{SS} = 5.0V ±5%, unless otherwise noted.

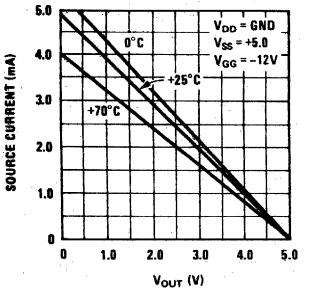
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Clock Frequency (ϕ_f)	ϕt_r, $\phi t_f \leq$ 10 ns (Note 2)	DC	3.0	1.5	MHz
Clock Pulsewidth (ϕ_{PW})					
ϕ_{PW}	$\phi t_r = \phi t_f \leq$ 10 ns	0.25	0.180	10	μs
$\overline{\phi_{PW}}$	$\phi t_r = \phi t_f \leq$ 10 ns	0.38			μs
Clock Transition Times					
Clock Risetime (ϕt_r)				500	ns
Clock Falltime (ϕt_f)				500	ns
Clock Control Setup Time (t_{CS})	(Figure 1) $\phi t_r = \phi t_f$ = 10 ns	0			ns
Clock Control Hold Time (t_{ch})	(Figure 1) $\phi t_r = \phi t_f$ = 10 ns	0			ns
Data Input Setup Time (t_{ds})	(Figure 1) $\phi t_r = \phi t_f$ = 10 ns	60	30		ns
Data Input Hold Time (t_{dh})	(Figure 1) $\phi t_r = \phi t_f$ = 10 ns	40	20		ns
Data Output Propagation Delay From Clock	(Figures 1 and 2) $\phi t_r = \phi t_f$ = 10 ns				
Delay to Output High Level (t_{pdH})			200	300	ns
Delay to Output Low Level (t_{pdL})			200	300	ns

Note 1: Capacitance is guaranteed by periodic testing.

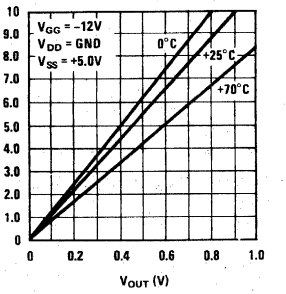
Note 2: For static operation clock must remain at V_{IL}.

typical performance characteristics

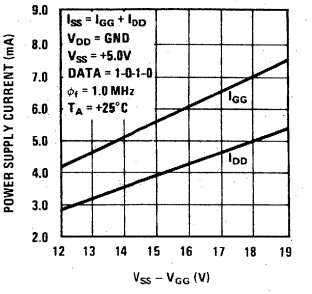
Typical Data Output Source Current vs Data Output Voltage



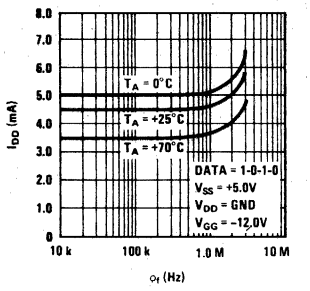
Typical Data Output Sink Current vs Data Output Voltage



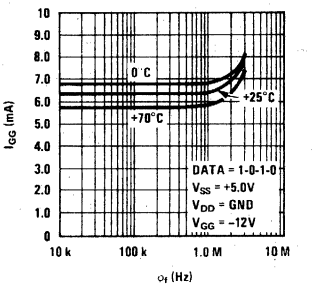
Typical Power Supply Current vs V_{GG}



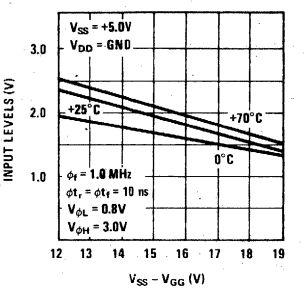
Typical I_{DD} vs Clock Frequency



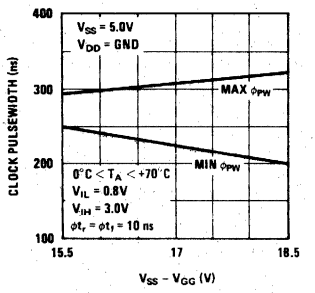
Typical I_{GG} vs Clock Frequency



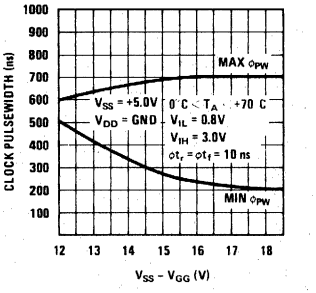
Typical Input Levels vs V_{GG}



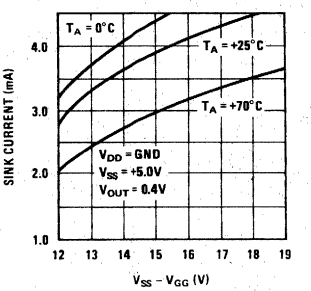
Typical 2.2 MHz Operating Curve



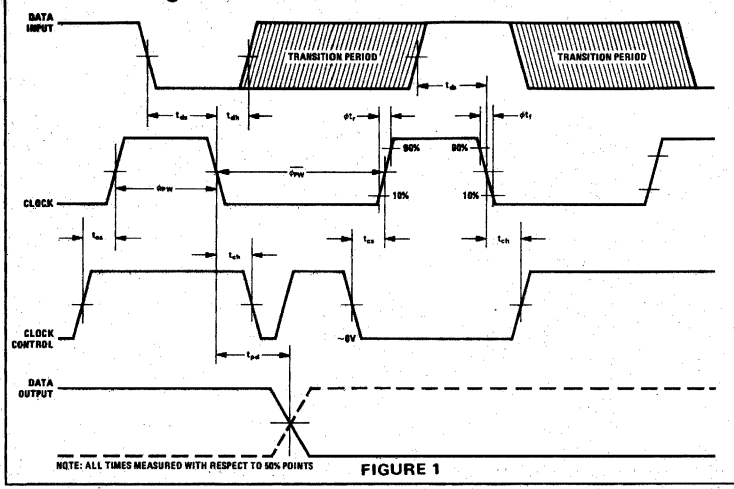
Typical 1.0 MHz Operating Curve



Typical Data Output Sink Current vs V_{GG}



switching time waveforms



NOTE: ALL TIMES MEASURED WITH RESPECT TO 50% POINTS

FIGURE 1

ac test circuit

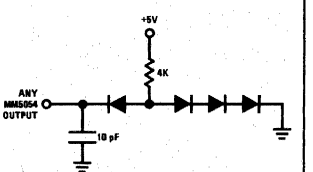


FIGURE 2

NATIONAL

Shift Registers

MM4055/MM5055 quad 128-bit static shift register
MM4056/MM5056 dual 256-bit static shift register
MM4057/MM5057 512-bit static shift register

general description

The MM4055/MM5055, MM4056/MM5056, MM4057/MM5057 512-bit static shift registers are MOS monolithic integrated circuits using silicon gate technology to achieve bipolar compatibility. They have a guaranteed operating frequency of 1.0 and 1.5 MHz respectively, and an on chip clock generator allows TTL level clock driver for complete TTL compatibility.

features

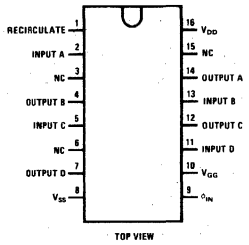
- Guaranteed operation
  - 1.5 MHz 0°C to +70°C
  - 1.0 MHz −55°C to +125°C
- Single TTL compatible clock, on chip clock generator
- Low clock capacitance 10 pF (typ)
- Operates from +5.0V, GND, and −12V
- Three configurations
  - MM4055/MM5055 Quad 128 bit
  - MM4056/MM5056 Dual 256 bit
  - MM4057/MM5057 Single 512 bit
- Internal recirculate

applications

- CRT displays
- Terminals
- Disk and drum replacements
- Buffer memory

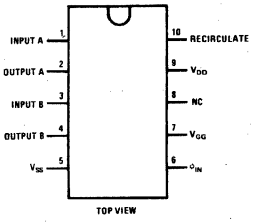
connection diagrams

Dual-In-Line Package



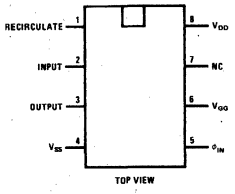
Order Number MM4055D or MM5055D
See Package 3
Order Number MM5055N
See Package 15

Dual-In-Line Package



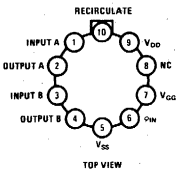
Order Number MM5056N
See Package 13

Dual-In-Line Package



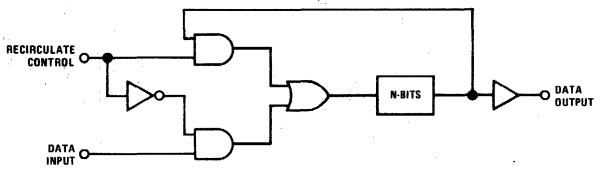
Order Number MM4057D or MM5057D
See Package 1
Order Number MM5057N
See Package 12

Metal Can Package



Order Number MM4056H or MM5056H
See Package 24

logic diagram



absolute maximum ratings (Note 1)

Data and Clock Input Voltages and Supply Voltages with Respect to V_{SS}	+0.3V to −20V
Power Dissipation	600 mW @ $T_A = 25°C$
Operating Temperature Range	
MM5055, MM5056, MM5057	0°C to 70°C
MM4055, MM4056, MM4057	−55°C to 125°C Case
Storage Temperature Range	−65°C to 160°C
Lead Temperature (Soldering, 10 seconds)	300°C

electrical characteristics (MM4055, MM4056, MM4057)

$T_A = -55°C$ to $+125°C$, $V_{SS} = 5.0V \pm 5\%$, $V_{GG} = -12V \pm 5\%$, $V_{DD} = 0V$, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Data, Recirculate and Clock Input Levels					
Logical High Level (V_{IH})		$V_{SS} - 1.0$		$V_{SS} + 0.3$	V
Logical Low Level (V_{IL})		$V_{SS} - 15$		$V_{SS} - 4.2$	V
Data, Recirculate and Clock Input Leakage	$V_{IN} = -10V$, $T_A = 25°C$ All Other Pins GND		0.01	0.5	μA
Data Input Capacitance	$V_{IN} = 0V$, f = 1 MHz All Other Pins GND (Note 2)		4.5	6.0	pF
Recirculate Input Capacitance	$V_{IN} = 0V$, f = 1 MHz All Other Pins GND (Note 2)		3.0	6.0	pF
Clock Capacitance	$V_{IN} = 0V$, f = 1 MHz All Other Pins GND (Note 2)		10	14	pF
Data Output Levels					
Logical High Level (V_{OH})	$I_{SOURCE} = -0.5$ mA	2.4		V_{SS}	V
Logical Low Level (V_{OL})	$I_{SINK} = 1.6$ mA	V_{DD}		0.4	V
Power Supply Current	$T_A = 25°C$, $V_{GG} = -12V$, $V_{SS} = 5.0V$ $V_{DD} = 0V$, $\phi_{PW} = 230$ ns Data = 0-1-0-1 · · ·				
I_{GG}	$\phi_f \leq 0.1$ MHz		6.5	9.0	mA
	$\phi_f \leq 1.6$ MHz		10.5	15.5	mA
I_{DD} (Note 4)	$\phi_f \leq 0.1$ MHz		13	18	mA
	$\phi_f \leq 1.6$ MHz		15	20	mA
Clock Frequency (ϕ_f)	$\phi_{tr}, \phi_{tf} \leq 10$ ns (Note 5)		2.2	1.0	MHz
Clock Pulse Width					
(ϕ_{PW})	$\phi_{tr}, \phi_{tf} \leq 10$ ns (See ac Test Circuit)	0.400	0.280	10	μs
$\overline{(\phi_{PW})}$	$\phi_{tr}, \phi_{tf} \leq 10$ ns (See ac Test Circuit)	0.400	0.160	dc	μs
Data Input Setup Time (t_{ds})	$t_r, t_f \leq 10$ ns For Load Conditions See ac Test Circuit	260			ns
Data Input Hold Time (t_{dH})		120			ns
Recirculate Setup Time (t_{ds})		260			ns
Recirculate Hold Time (t_{dH})		120			ns
Data Output Propagation Delay					
Delay to High Level (t_{pdH})			350	700	ns
Delay to Low Level (t_{pdL})			350	700	ns

electrical characteristics (con't) (MM5055, MM5056, MM5057)

$T_A = 0°C$ to $+70°C$, $V_{SS} = 5.0V \pm 5\%$, $V_{GG} = -12V \pm 5\%$, $V_{DD} = 0V$, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Data, Recirculate and Clock Input Levels					
Logical High Level (V_{IH})		$V_{SS} - 1.5$		$V_{SS} + 0.3$	V
Logical Low Level (V_{IL})		$V_{SS} - 15$		$V_{SS} - 4.2$	V
Data, Recirculate and Clock Input Leakage	$V_{IN} = -10V$, $T_A = 25°C$ All Other Pins GND		0.01	0.5	μA
Data Input Capacitance	$V_{IN} = 0V$, f = 1 MHz, All Other Pins GND (Note 2)		4.5	6.0	pF
Recirculate Input Capacitance	$V_{IN} = 0V$, f = 1 MHz, All Other Pins GND (Note 2)		3.0	6.0	pF
Clock Capacitance	$V_{IN} = 0V$, f = 1 MHz, All Other Pins GND (Note 2)		10	14	pF
Data Output Levels					
Logical High Level (V_{OH})	$I_{SOURCE} = -0.5$ mA	2.4		V_{SS}	V
Logical Low Level (V_{OL})	$I_{SINK} = 1.6$ mA	V_{DD}		0.4	V
Power Supply Current	$T_A = 25°C$, $V_{GG} = -12V$, $V_{SS} = 5.0V$ $V_{DD} = 0V$, $\phi_{PW} = 230$ ns Data = 0-1-0-1 · · ·				
I_{GG}	$\phi_f \leq 0.1$ MHz		6.5	9.0	mA
	$\phi_f \leq 2.2$ MHz		13	19	mA
I_{DD} (Note 4)	$\phi_f \leq 0.1$ MHz		13	18	mA
	$\phi_f \leq 2.2$ MHz		15	20	mA
Clock Frequency (ϕ_f)	ϕ_{tr}, $\phi_{tf} \leq 10$ ns (Note 5)		3.0	1.5	MHz
Clock Pulse Width					
(ϕ_{PW})	ϕ_{tr}, $\phi_{tf} \leq 10$ ns	0.230	0.100	100	μs
(ϕ_{PW})	ϕ_{tr}, $\phi_{tf} \leq 10$ ns	0.300	0.100	dc	μs
Data Input Setup Time (t_{ds})	t_r, $t_f \leq 10$ ns For Load Conditions See Test Circuit	110			ns
Data Input Hold Time (t_{dH})		40			ns
Recirculate Setup Time (t_{ds})		110			ns
Recirculate Hold Time (t_{dH})		40			ns
Data Output Propagation Delay					
Delay to High Level (t_{pdH})			250	345	ns
Delay to Low Level (t_{pdL})			250	345	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

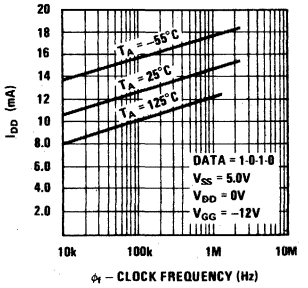
Note 3: Positive true logic notation is used:
Logic "1" = most positive voltage level
Logic "0" = most negative voltage level

Note 4: Outputs not loaded when measuring I_{DD}. Add 1.6 mA to I_{DD} for each TTL load to compute worst case power.

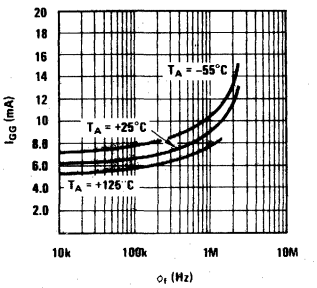
Note 5: For static operation clock must remain at V_{IL}.

typical performance characteristics

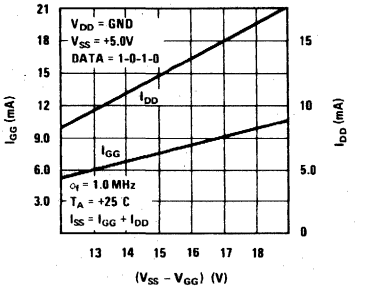
Typical I_{DD} vs Clock Frequency



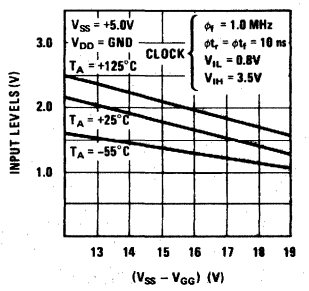
Typical I_{GG} vs Clock Frequency



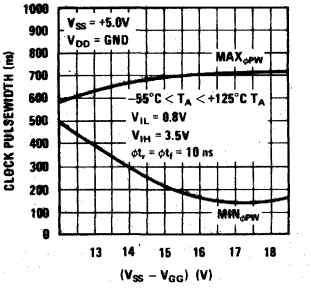
Typical Power Supply Current vs V_{GG}



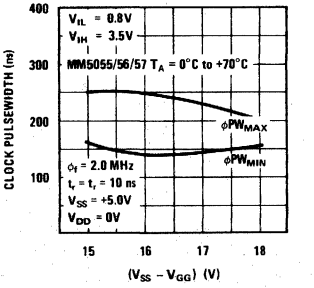
Typical Input Levels vs V_{GG}



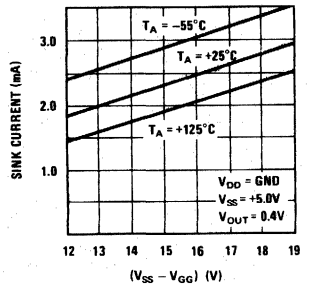
Typical 1.0 MHz Operating Curve



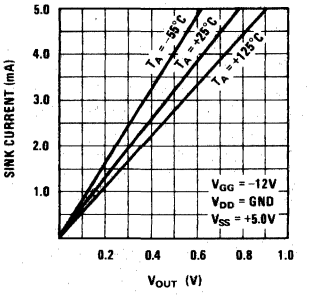
Typical 2.0 MHz Operating Curve



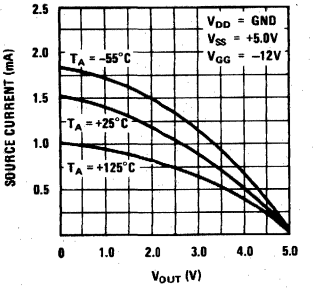
Typical Data Output Sink Current vs V_{GG}



Typical Output Sink Current vs Data Output Voltage

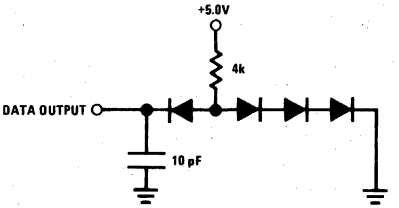


Typical Data Output Source Current vs Data Output Voltage

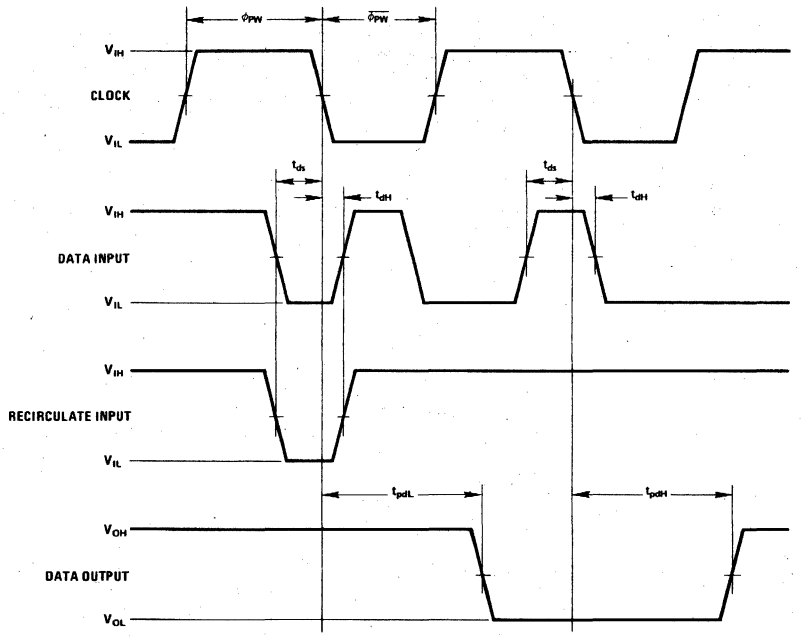


8

test circuit



switching time waveforms



$t_r, t_f \leq 10$ ns ALL TIMES MEASURED FROM 50% POINTS

Shift Registers

MM5058 1024-bit static shift register

general description

The MM5058 is a monolithic 1024-bit static shift register utilizing a low threshold P-channel silicon gate technology to achieve bipolar compatibility. "Stream select" logic on the chip chooses between two inputs, facilitating external recirculate operation. This in addition to an internal clock-driver, thus providing a single external TTL/DTL clock, makes this device flexible and convenient to integrate into existing TTL/DTL or MOS systems.

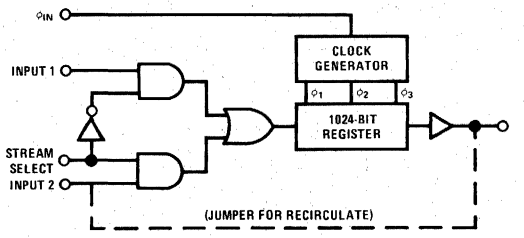
features

- Bipolar compatibility — All inputs, outputs, and clock interface directly with standard TTL/DTL circuits with no external components
- Single phase clock — On chip clock driver provides single TTL/DTL level clock with low input capacitance
- High frequency operation — DC to 1.5 MHz guaranteed
- Standard power supplies — +5.0V and −12V
- Small package — 8-pin mini DIP
- Low power consumption — 250μW/bit typ
- Stream select for easy external recirculate

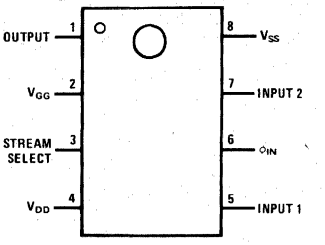
applications

- Sequential access memories
- Static buffer memories
- CRT refresh
- Delay lines
- Drum memory replacement

logic and connection diagrams



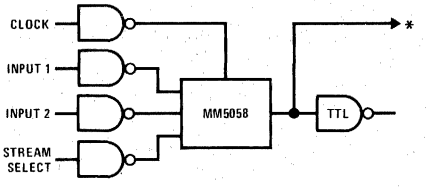
Dual-In-Line Package



TOP VIEW

Order Number MM5058D
See Package 1
Order Number MM5058N
See Package 12

ac test circuit



*PROPAGATION DELAYS MEASURED AT MM5058 OUTPUT.

truth table

STREAM SELECT	FUNCTION
LOGIC "0"	INPUT 1
LOGIC "1"	INPUT 2

absolute maximum ratings (Note 1)

Data and Clock Input Voltages and Supply Voltages with Respect to V_{SS}	+0.3V to -20V
Power Dissipation	535 mW @ T_A = 25°C
Operating Temperature Range	0°C to +70°C Ambient
Storage Temperature	-65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

dc electrical characteristics

T_A within specified operating temperature range, V_{SS} = +5.0V ±5%, V_{GG} = −12V ±5%, V_{DD} = 0V, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP (Note 4)	MAX	UNITS
Input Levels					
Logical High Level (V_{IH})		V_{SS} − 1.5		V_{SS} + 0.3	V
Logical Low Level (V_{IL})		V_{SS} − 10		V_{SS} − 4.2	V
Input Leakage (All Inputs)	V_{IN} = −10V, T_A = 25°C All Other Pins GND		0.05	0.5	μA
Input Capacitance (Note 2)	V_{IN} = 0V, f = 1.0 MHz (Note 1) All Other Pins (GND)		3.0	7.0	pF
Data Output Levels, TTL Load					
Logical High Level (V_{OH})	I_{SOURCE} = −0.5 mA	2.4	3.5		V
Logical Low Level (V_{OL})	I_{SINK} = 1.6 mA	V_{DD}		0.4	V
Power Supply Current	DATA = 0-1-0-1				
I_{GG}	ϕ_f = 1.5 MHz Continuous Operation		8.0	13	mA
I_{SS}	DATA = 0-1-0-1 ϕ_f = 1.5 MHz Continuous Operation		38	60	mA

ac electrical characteristics

T_A within specified operating temperature range, V_{SS} = +5.0V ±5%, V_{GG} = −12V ±5%, V_{DD} = 0V, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP (Note 4)	MAX	UNITS
Clock Frequency (ϕ_f)	$\phi t_r = \phi t_f$ = 10 ns		3.0	1.5	MHz
Clock Pulse Width					
ϕ_{PW}	$\phi t_r = \phi t_f$ = 10 ns	0.350	0.100	100	μs
$\overline{\phi_{PW}}$	$\phi t_r = \phi t_f$ = 10 ns	0.250		DC	μs
Clock Pulse Transition (t_r, t_f)				1.0	μs
Data Input Setup Time (t_{DS})	$t_r = t_f \leq$ 10 ns See AC Test Circuit for Load Conditions	100			ns
Data Input Hold Time (t_{DH})		30			ns
Stream Select Setup Time (t_{SS})		150			ns
Stream Select Hold Time (t_{SH})		30			ns
Data Output Propagation Delay From ϕ_{IN}					
Delay to High Level (t_{pdH})			200	300	ns
Delay to Low Level (t_{pdL})			200	300	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

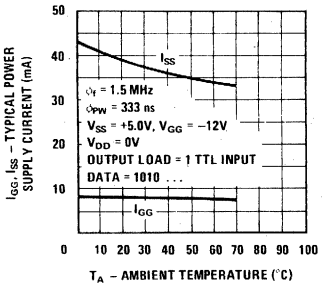
Note 2: Capacitance is guaranteed by periodic testing.

Note 3: Positive true logic notation is used: Logic "1" = most positive voltage level; Logic "0" = most negative voltage level.

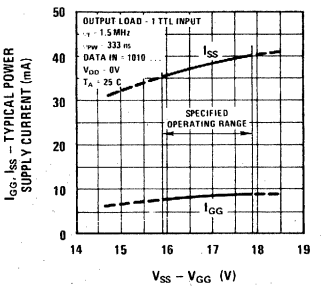
Note 4: Typical values apply for V_{SS} = 5.0V, V_{GG} = −12V, V_{DD} = 0V, and T_A = 25°C.

typical performance characteristics

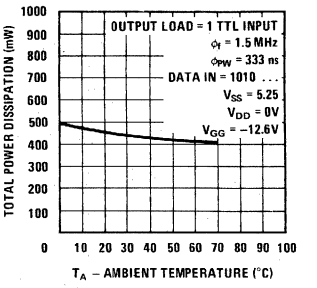
Typical Power Supply Current vs Temperature



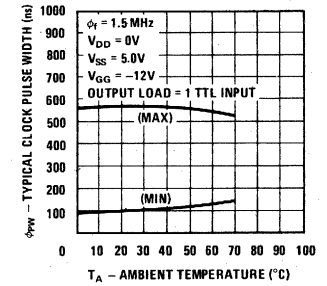
Typical Power Supply Current vs Supply Voltage



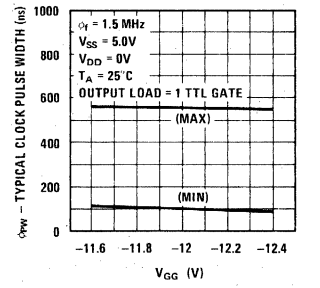
Guaranteed Power Consumption vs Temperature



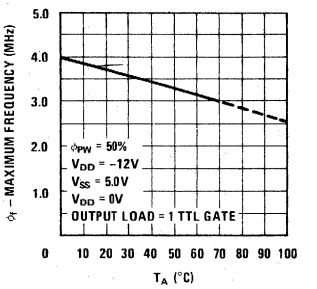
Typical Clock Pulse Width vs Ambient Temperature



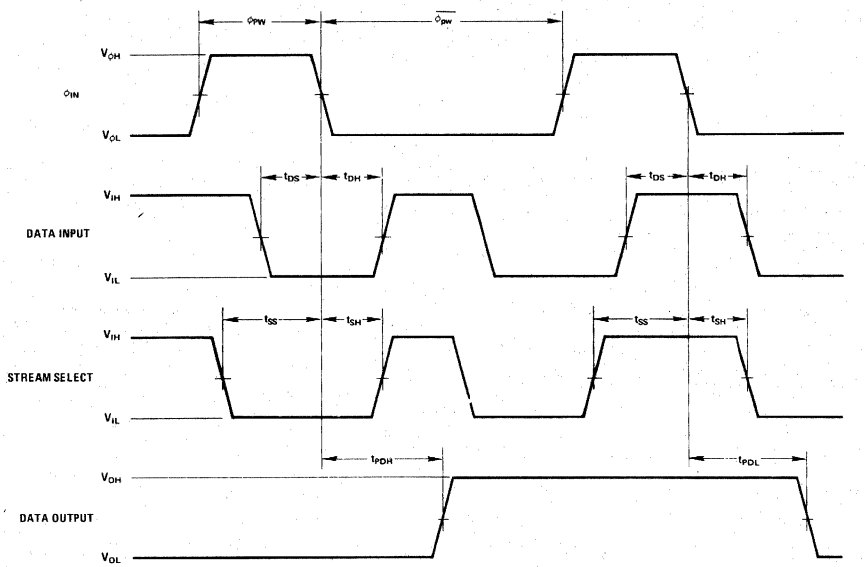
Typical Clock Pulse Width vs V_{GG}



Typical Maximum Frequency vs Ambient Temperature



switching time waveforms



NOTE 1: TIMES MEASURED AT 50% POINTS WITH t_r, $t_f \leq 10$ ns.
NOTE 2: FOR DC STORAGE CLOCK MUST REMAIN AT V_{OL}.

NATIONAL

Shift Registers

MM5060 dual 144-bit mask programmable static shift register

general description

The MM5060 is a monolithic dual 144-bit static shift register/accumulator utilizing a silicon gate low threshold P-channel enhancement mode technology to achieve complete bipolar compatibility. The device can be programmed by metal mask option to custom lengths from 125 to 144-bits in one bit increments.

Standard Lengths:

MM5060AA
Dual 128-Bit Shift Register/Accumulator
MM5060AB
Dual 132-Bit Shift Register/Accumulator
MM5060AC
Dual 133-Bit Shift Register/Accumulator
MM5060AD
Dual 144-Bit Shift Register/Accumulator

Custom Lengths:

The programmed shift registers are assigned a letter code for each option. These are designated by a pair of letters after the number code but before the package designation such as MM5060AD/D which is a 0°C to +70°C dual 144-bit shift register/accumulator in an 8-lead cavity dual-in-line package. Pattern codes are assigned by National upon entry of order.

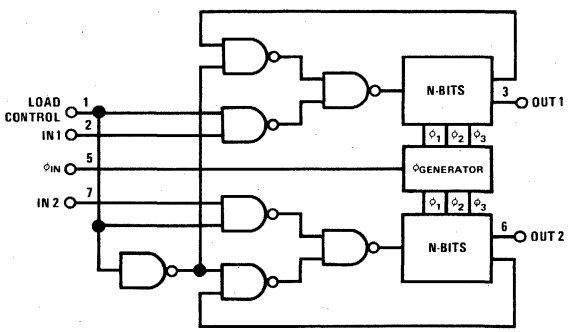
features

- Complete bipolar compatibility — input/output and clock input completely DTL/TTL compatible without additional components
- Standard Supplies +5V, −12V
- High frequency operation — DC to 3.0 MHz typical
- Single phase clock — DTL/TTL compatible on chip clock
- Low clock line capacitance 6.0 pF max.

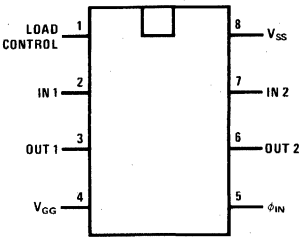
applications

- Printer memory — any length from 125 to 144-bits per line
- Telemetry systems and data sampling
- Serial memory storage

logic and connection diagrams



Dual-In-Line Package



TOP VIEW

Order Number MM5060AA/D, MM5060AB/D, MM5060AC/D, MM5060AD/D or MM5060XX/D
See Package 1

Order Number MM5060AA/N, MM5060AB/N, MM5060AC/N, MM5060AD/N or MM5060XX/N
See Package 12

truth table

LOAD CONTROL	INPUT	FUNCTION
0	0	Recirculate
0	1	Recirculate
1	0	"0" is written
1	1	"1" is written

absolute maximum ratings

Data and Clock Input Voltages and Supply Voltages with respect to V_{SS}	+0.3V to −20V
Power Dissipation	600 mW @ T_A = 25°C
Operating Temperature Range	
MM5060	0°C to +70°C (Ambient)
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics

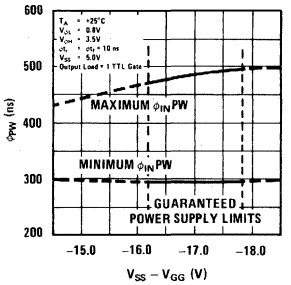
T_A within specified operating temperature range, V_{SS} = 5.0V ±5%, V_{GG} −12.0V ±5%, unless otherwise specified.

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Data Input Levels					
Logical High Level (V_{IH})		V_{SS} − 1.5		V_{SS} + 0.3	V
Logical Low Level (V_{IL})		V_{SS} − 10.0		V_{SS} − 4.2	
Data Input Leakage	V_{IN} = −10V, T_A = 25°C All Other Pins GND		0.01	0.5	μA
Data Input Capacitance	V_{IN} = 0.0V, f = 1 MHz All Other Pins GND (Note 1)		3.0	5.0	pF
Load Control Input Levels					
Logical High Level (V_H)		V_{SS} − 1.5		V_{SS} + 0.3	V
Logical Low Level (V_L)		V_{SS} − 10.0		V_{SS} − 4.2	V
Load Control Input Leakage	V_{IN} = −10V, T_A = 25°C All Other Pins GND		0.01	0.5	μA
Load Control Input Capacitance	V_{IN} = 0.0V, f = 1 MHz All Other Pins GND (Note 1)		3.0	5.0	pF
Clock Input Levels					
Logical High Level ($V_{\phi H}$)		V_{SS} − 1.5		V_{SS} + 0.3	V
Logical Low Level ($V_{\phi L}$)		V_{SS} − 10.0		V_{SS} − 4.2	V
Clock Input Leakage	V_ϕ = −10.0V, T_A = 25°C All Other Pins GND		0.01	0.5	μA
Clock Input Capacitance	V_ϕ = 0.0V, f = 1 MHz All Other Pins GND (Note 1)		3.5	6.0	pF
Data Output Levels TTL Load					
Logical High Level (V_{OH})	I_{SOURCE} = −0.5 mA	3.0	3.5		V
Logical High Level MOS Load (V_{OH})	I_{SOURCE} = −0.01 mA	4.0	4.5		V
Logical Low Level (V_{OL})	I_{SINK} = 1.6 mA			0.4	V
Power Supply Current (I_{GG})	T_A = 25°C, V_{GG} = −12V ϕ_{PW} = 300 ns, V_{SS} = +5.0V Data = 0-1-0-1				
	0.01 MHz ≤ ϕ_f ≤ 0.1 MHz		20.0	24.0	mA
	ϕ_f = 1.0 MHz		21.0	25.0	mA
	ϕ_f = 1.5 MHz		22.0	26.0	mA
Clock Frequency (ϕ_f)	$\phi t_r = \phi t_f$ = 10 ns, T_A = 25°C	DC	3.0	1.5	MHz
Clock Pulsewidth (ϕ_{PW})	$\phi t_r = \phi t_f$ = 10 ns, T_A = 25°C	0.300	0.100	100	μs
($\overline{\phi_{PW}}$)		0.200		DC	μs
Clock Pulse Transition (ϕt_r, ϕt_r)				1	μs
Data Input Setup Time (t_{ds})	T_A = 25°C, t_r, t_f = 10 ns	70			ns
Data Input Hold Time (t_{dh})	T_A = 25°C, t_r, t_f = 10 ns	50			ns
Load Control Setup (t_{ds})	T_A = 25°C, t_r, t_f = 10 ns	70			ns
Load Control Hold (t_{dh})	T_A = 25°C, t_r, t_f = 10 ns	50			ns
Data Output Propagation Delay from ϕ in	T_A = 25°C, t_r, t_f = 10 ns				
Delay to High Level (t_{pdH})			250	350	ns
Delay to Low Level (t_{pdL})			250	350	ns

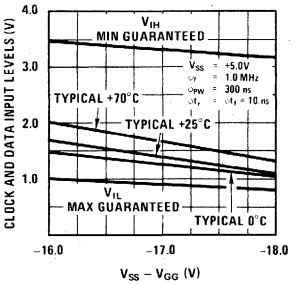
Note 1: Capacitance is guaranteed by periodic testing.

typical performance characteristics

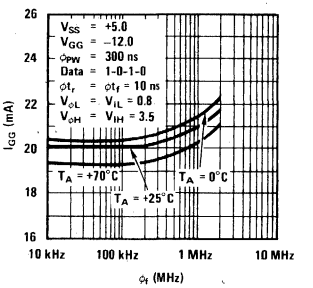
Guaranteed 1.5 MHz Operating Curve



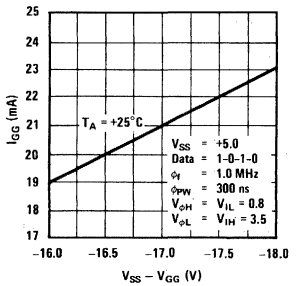
Guaranteed Input Voltage Levels vs Supply Voltage



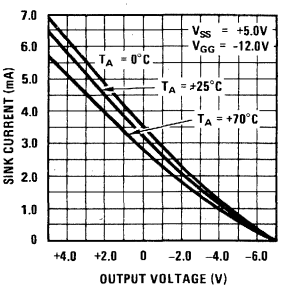
Typical I_{GG} vs Clock Frequency Under TTL Load



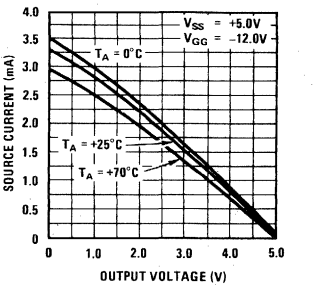
Typical Power Supply Current vs Voltage Under TTL Load



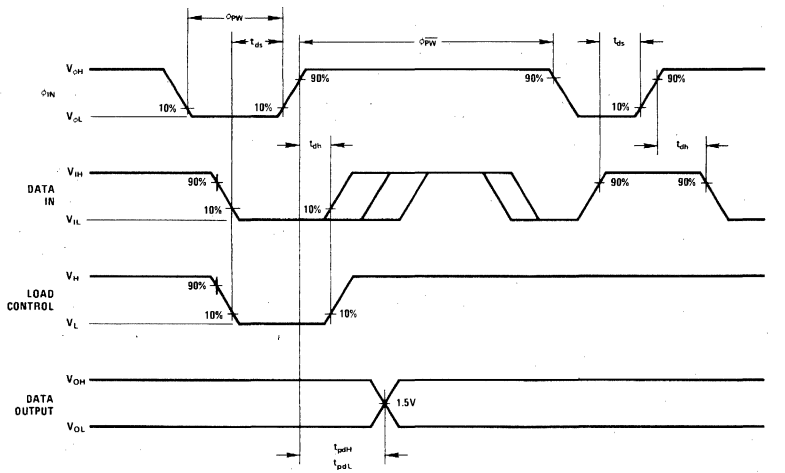
Typical Output Sink Current vs Output Voltage



Typical Output Source Current vs Output Voltage



switching time waveforms



Note: DC storage is accomplished during ϕ_{PW} time.

Shift Registers

MM5061 quad 100-bit static shift register

general description

The MM5061 quad 100-bit static shift register is a MOS monolithic integrated circuit using silicon gate technology to achieve bipolar compatibility. It has a guaranteed operating frequency of 1.5 MHz and an on-chip clock generator.

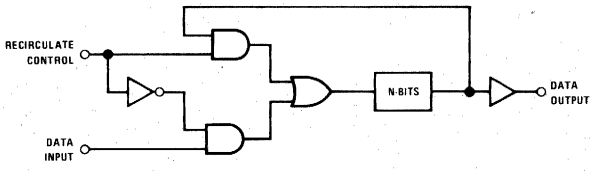
features

- Guaranteed 1.5 MHz operation
- Single TTL compatible clock on chip clock generator
- Low clock capacitance 10 typ, 14 max
- Operates from +5V, GND, and -12V
- Configuration Quad 100-bit
- Internal recirculate

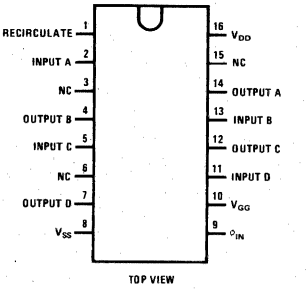
applications

- CRT displays
- Terminals
- Disk and drum replacements
- Buffer memory

logic and connection diagrams

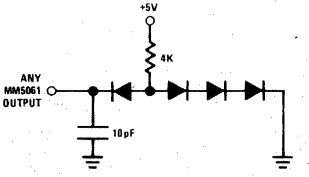


Dual-In-Line Package



Order Number MM5061D
See Package 3
Order Number MM5061N
See Package 15

test circuit



truth table

RECIRCULATE CONTROL	FUNCTION
1	Data Recirculates
0	Register Accepts Input Data

absolute maximum ratings (Note 1)

Data and Clock Input Voltages and Supply Voltages with Respect to V_{SS}	+0.3V to −20V
Power Dissipation	600 mW @ T_A = 25°C
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +160°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics

T_A within operating temperature range, V_{SS} = +5V ±5%, V_{GG} = −12V ±10%, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Data Input Level					
Logical High Level (V_{IH})		V_{SS} − 1.5		V_{SS} + 0.3	V
Logical Low Level (V_{IL})		V_{SS} − 10		V_{SS} − 4.2	V
Data Input Leakage	V_{IN} = −10.0V, T_A = 25°C, All Other Pins GND		0.01	0.5	μA
Data Input Capacitance (Note 2)	V_{IN} = 0.0V, f = 1 MHz, All Other Pins GND		4.5	6.0	pF
Recirculate Input Levels					
Logical High Level (V_H)		V_{SS} − 1.5		V_{SS} + 0.3	V
Logical Low Level (V_L)		V_{SS} − 10		V_{SS} − 4.2	V
Recirculate Input Leakage	V_{IN} = 10.0V, T_A = 25°C, All Other Pins GND		0.01	0.5	μA
Recirculate Input Capacitance	V_{IN} = 0.0V, f = 1 MHz, All Other Pins GND		3.0	6.0	pF
Clock Input Levels					
Logical High Level (V_{OH})		V_{SS} - 1.0		V_{SS} + 0.3	V
Logical Low Level (V_{OL})		V_{SS} - 10.0		V_{SS} − 4.2	V
Clock Input Leakage	V_ϕ = −10.0V, T_A = 25°C, All Other Pins GND		0.01	0.5	μA
Clock Capacitance (Note 2)			10.0	14.0	pF
Data Output Levels					
Logical High Level (V_{OH})	I_{SOURCE} = −3.0 mA	2.85		V_{SS}	V
Logical Low Level (V_{OL})	I_{SINK} = 1.6 mA			0.4	V
Power Supply Current (I_{GG})	T_A = 25°C, V_{GG} = −12.0V, ϕ_{PW} = 160 ns, V_{SS} = +5.0V, V_{OL} = 0.8V, Data = 0-1-0-1, V_{DD} = 0.0V				
	$\phi_f \leq$ 0.1 MHz		6.5	9.0	mA
	ϕ_f = 2.2 MHz		13.0	19.0	mA
(I_{DD})(Note 4)	$\phi_f \leq$ 0.1 MHz		13.0	18.0	mA
	$\phi_f \leq$ 2.2 MHz		15.0	20.0	mA
Clock Frequency ϕ_f	$\phi t_r = \phi t_f \leq$ 10 ns		3.0	1.5	MHz
Clock Pulse Width ϕ_{PW}	$\phi t_r = \phi t_f \leq$ 10 ns	0.230	0.100	10.0	μs
$\overline{\phi_{PW}}$	$\phi t_r = \phi t_f \leq$ 10 ns	0.200		DC	μs
Data Input Setup Time (t_{dS})	t_r, $t_f \leq$ 10 ns For Load Conditions see Test Circuit	100			ns
Data Input Hold Time (t_{dH})		40			ns
Recirculate Setup (t_{dS})		100			ns
Recirculate Hold (t_{dH})		40			ns
Data Output Propagation Delay from ϕ					
Delay to High Level (t_{pdH})			250	350	ns
Delay to Low Level (t_{pdL})			250	350	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

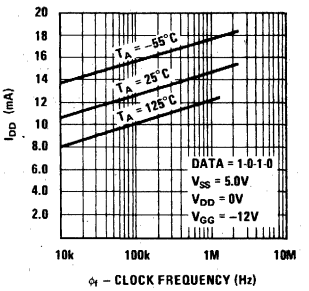
Note 2: Capacitance is guaranteed by periodic testing.

Note 3: Positive true logic notation is used: Logic "1" = most positive voltage level; Logic "0" = most negative voltage level.

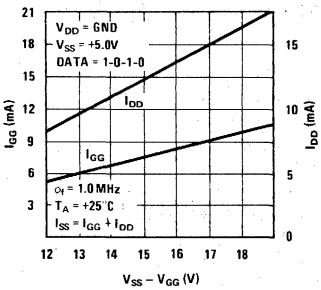
Note 4: Outputs not loaded when measuring I_{DD} therefore I_{DD} will increase by 1.6 mA for each TTL load (TTL "0" level output).

typical performance characteristics

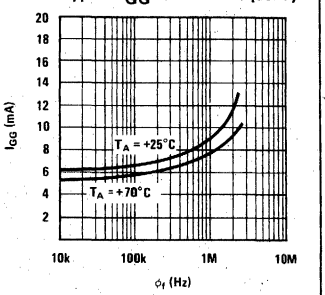
Typical I_{DD} vs Clock Frequency



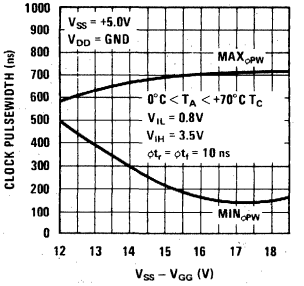
Typical Power Supply Current vs V_{GG}



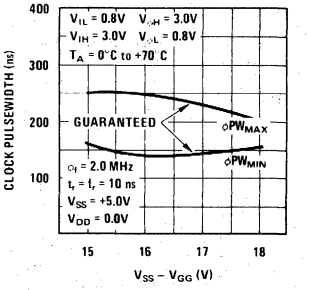
Typical I_{GG} vs Clock Frequency



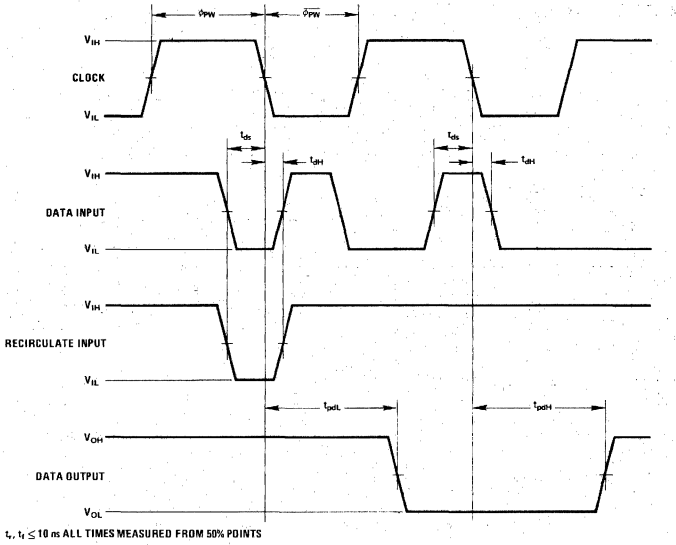
Guaranteed 1.0 MHz Operating Curve



Guaranteed 2.0 MHz Operating Curve



switching time waveforms



$t_r, t_f \leq 10$ ns ALL TIMES MEASURED FROM 50% POINTS

NATIONAL

Shift Registers

MM4104/MM5104 dynamic shift register

general description

The MM4104/MM5104 360/359, 228/287, 40/32 bit dynamic shift register is a monolithic MOS integrated circuit utilizing p-channel enhancement mode low threshold technology to achieve bipolar compatibility. The register lengths are lengthened or shortened by hard wiring the length select line to V_{GG} or V_{SS}. The lengths available are: 40, 288, 328, 360, 400, 560, 688; or 32, 287, 319, 359, 391, 446, 678.

- Multiple length registers — Electrically adjustable 360/359, 288/287, 40/32 bit registers
- Wide frequency range — 250 Hz min. guar. at 25°C; 2.5 MHz max. guar. over temp.

features

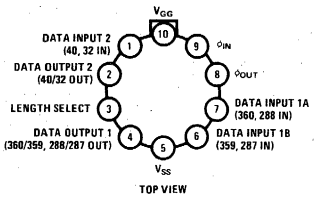
- DTL/TTL compatibility — +5V, −12V power supply. No pull-up or pull-down resistors required

applications

- Data store
- CRT displays
- Business machine

connection diagram

Metal Can Package

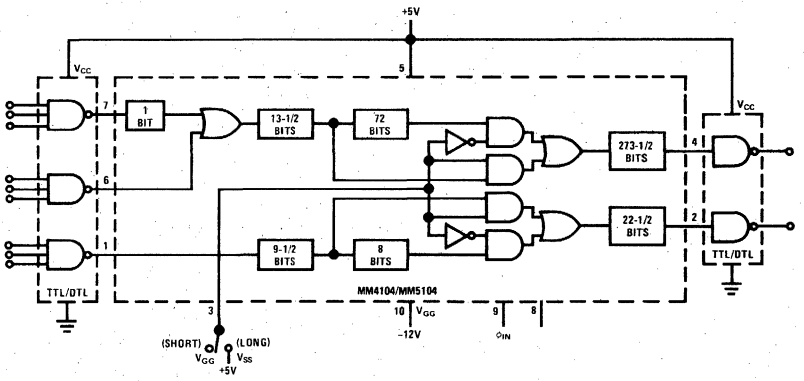


TOP VIEW

Order Number MM4104H or MM5104H
See Package 24

typical applications

TTL/MOS Interface



Note: V_{GG} on pin 3 results in a 288-bit register between pin 7 and pin 4 and a 287-bit register between pins 6 and 4. The unused input (6 or 7) must be returned to V_{SS}. Also, there is a 32-bit register between pins 1 and 2.

V_{SS} on pin 3 results in a 360 bit register between pin 7 and pin 4 and a 359-bit register between pins 6 and 4. The unused input (6 or 7) must be returned to V_{SS}. Also, there is a 40-bit register between pins 1 and 2.

absolute maximum ratings

Voltage at Any Pin	V_{SS} + 0.3V to V_{SS} − 22V
Operating Temperature Range MM4104	−55°C to 125°C
MM5104	−25°C to 70°C
Storage Temperature Range	−65°C to 150°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics

(T_A within operating temperature range, V_{SS} = +5.0V, ±5%, V_{GG} = −12.0V ±10%, unless otherwise specified.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Data Input Levels					
Logical HIGH Level (V_{IH})		V_{SS} − 2.0		V_{SS} + 0.3	V
Logical LOW Level (V_{IL})		V_{SS} − 18.5		V_{SS} −4.2	V
Data Input Leakage	V_{IN} = −20.0V, T_A = 25°C, All Other Pins GND		0.01	0.5	μA
Data Input Capacitance	V_{IN} = 0.0V, f = 1 MHz, All Other Pins GND, (Note 3)		3.0	5.0	pF
Length Select Input Levels					
Logical HIGH Level (V_{LSH})		V_{SS}		V_{SS} + 0.3	V
Logical LOW Level (V_{LSL})		V_{SS} − 18.5		V_{GG}	V
Length Select Input Leakage	V_{IN} = −20V, T_A = 25°C, All Other Pins GND		0.01	0.5	μA
Length Select Input Capacitance	V_{IN} = 0.0V, f = 1 MHz, All Other Pins GND, (Note 3)		6.0	9.0	pF
Clock Input Levels					
Logical HIGH Level ($V_{\phi H}$)		V_{SS} − 1.5		V_{SS} + 0.3	V
Logical LOW Level ($V_{\phi L}$)		V_{SS} −18.5		V_{SS} − 14.5	V
Clock Input Leakage	V_ϕ = −20V, T_A = 25°C, All Other Pins GND		0.05	1.0	μA
Clock Input Capacitance	V_ϕ = 0.0V, f = 1 MHz, All Other Pins GND, (Note 3)		85	100	pF
Data Output Levels					
Logical HIGH Level (V_{OH})	I_{SOURCE} = −0.5 mA	2.4		V_{SS}	V
Logical LOW Level (V_{OL})	I_{SINK} = 1.6 mA			0.4	V
Power Supply Current					
I_{GG}	T_A = 25°C, V_{GG} = −12V, ϕ_{PW} = 150 ns, V_{SS} = 5.0V, $V_{\phi L}$ = −12V, Data = 0-1-0-1				
	0.01 MHz ≤ ϕ_f ≤ 0.1 MHz		1.5	2.5	mA
	ϕ_f = 1 MHz		3.5	5.0	mA
	ϕ_f = 2.5 MHz		7.0	10.0	mA
Clock Frequency (ϕ_f)	$\phi t_r = \phi t_f$ = 20 ns, (Note 1)	0.01	3.3	2.5	MHz
Clock Pulsewidth (ϕ_{PW})	$\phi t_f + \phi_{PW} + \phi t_r \leq 10.5\ \mu s$	0.15		10	μs
Clock Phase Delay Times (ϕ_d, $\bar{\phi}_d$)	(Note 1)	10			ns
Clock Transition Time (ϕt_r, ϕt_f)	$\phi t_f + \phi_{PW} + \phi t_r \leq 10.5\ \mu s$			1	μs
Partial Bit Times (T)	(Note 1)				
Input Partial Bit Time (T_{IN})		0.20		100	μs
Output Partial Bit Time (T_{OUT})		0.20		100	μs
Data Input Setup Time (t_{ds})		80	30		ns
Data Input Hold Time (t_{dh})		20	0		ns
Data Output Propagation Delay from ϕ_{OUT}	See ac test circuit.				
Delay to HIGH Level (t_{pdH})			150	200	ns
Delay to LOW Level (t_{pdL})			150	200	ns

Note 1: Minimum clock frequency is a function of temperature and partial bit times (T_{IN} and T_{OUT}) as shown by the ϕ_f versus temperature and T_{IN}, T_{OUT} versus temperature curves. The lowest guaranteed clock frequency for any temperature can be attained by making T_{IN} equal to T_{OUT}. The minimum guaranteed clock frequency is:

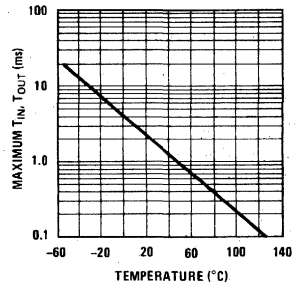
$$\phi_{f(min)} = \frac{1}{T_{IN} + T_{OUT}}$$, where T_{IN} and T_{OUT} do not exceed the guaranteed maximums.

Note 2: The curves are guaranteed by testing at a high temperature point.

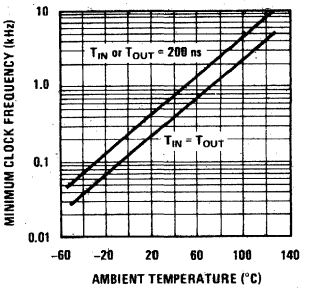
Note 3: Capacitance is guaranteed by periodic testing.

performance characteristics

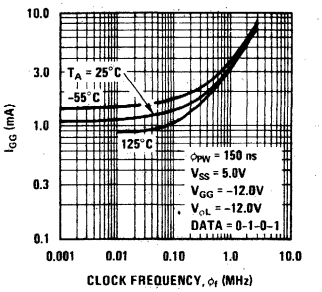
Guaranteed Maximum T_{IN} and T_{OUT} vs Temperature (Notes 1, 2)



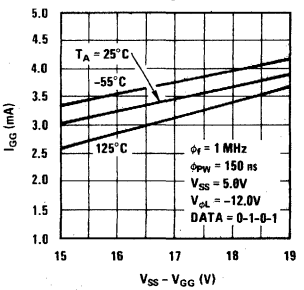
Guaranteed Minimum Clock Frequency vs Temperature (Notes 1, 2)



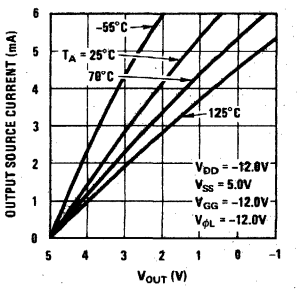
Typical Power Supply Current vs Clock Frequency



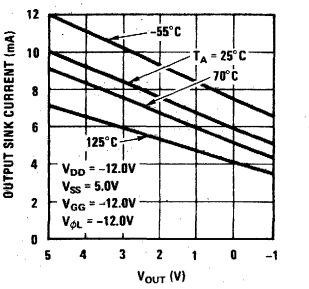
Typical Power Supply Current vs V_{GG}



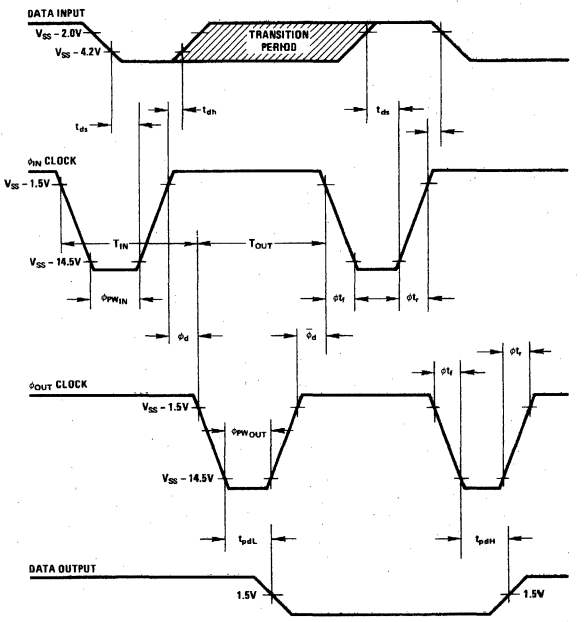
Typical Output Source Current vs Voltage



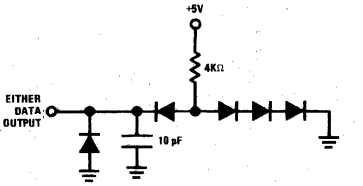
Typical Output Sink Current vs Voltage



switching time waveforms



ac test circuit



Memory Systems

INTRODUCTION

The Memory Systems Division was organized in January, 1974. A substantial financial commitment has been made to this division by National Semiconductor which has enabled the division to be fully staffed with the best engineering and manufacturing talent available in the industry. In addition, the division has purchased the latest in sophisticated design support computers and computer controlled testing equipment.

Since its founding, the division has rapidly grown. The major thrust of the division's effort to date has been in the development and production of memory cards and systems for the OEM market as well as the IBM Add-On Memory Systems market.

In the OEM market, the division has focused on standard/custom memory cards and systems currently being shipped to large OEM manufacturers for resale in CRT terminals, test equipment, phototypesetting equipment, airline reservation systems, large display systems, point of sale terminals, credit card embossing devices, CRT cluster controllers, editing terminals and other applications.

THE DESIGN OF MEMORY SYSTEMS

The three fundamentals essential in producing a cost effective and reliable semiconductor memory system are:

- Proper choice of memory component
- Design integrity of system
- Intensive production testing from components through entire system

National Memory Systems has focused on all three fundamentals and in doing so provides our customers with complete turn-key products. We specialize in assessing customer requirements, the writing of specifications for the customer when required, designing the system after choosing the most cost effective components and delivering fully-tested hardware—tested to an extent that most customers are unable to match.

"MAKE OR BUY" DECISION

One of the most difficult decisions to make under normal circumstances for the company that has a memory system requirement is whether the system should be designed and produced internal to their operations, or whether the decision should be to purchase memory systems from a company who specializes in providing systems, such as National Memory Systems.

Following are some of the reasons that our customers have chosen National Memory Systems (NMS) to solve their memory system requirements.

Design Expertise

NMS specializes in memory systems; by working with National, the customer's engineering staff is free to do what they do best.

Advances in Technology

NMS provides continual technology lead for customer (ask about our Guarantee Against Obsolescence).

Product Availability

Assurance of product during periods when component availability becomes difficult. (Assurance is due to our long lead procurement cycle and second sourcing policy).

NMS typically manufactures 90% of the components used in each memory module.

Inventory

Reduction of customer inventory. NMS works closely with our customers to establish production rates and NMS inventories consistent with customer objectives.

The purchase of a complete memory system from National reduces customer purchasing requirements.

Testing

This most critical element in the production of memory systems is a specialty at NMS.

Each memory system undergoes extensive testing in National's production test facility. Tests include component burn-in, aging and full system test under controlled temperature environment.

NMS has made a substantial investment in production test facilities. A customer typically is unable to make this huge investment in facilities, test methods and experienced personnel to ensure the level of product reliability achievable at National.

Quality Assurance

National maintains product integrity from design through all phases of manufacturing with two distinct quality groups—Quality Engineering and Quality Control.

No other memory system supplier provides the extensive testing and stringent quality assurance standards that is available at NMS.

Price/Performance

National Memory Systems provides the lowest cost, highest quality, highest performance memory products available.

CUSTOMER SUPPORT

National Memory Systems recognizes the need for a close customer relationship, since we are truly an extension of the customer's design and manufacturing staff. Each customer's support requirement varies; however, the following are common to all programs:

- A program manager is selected during early discussions to act as a single point contact at the factory for our customer
- Technical and Quality Control interfaces are established with the customer to assure proper communications on design, testing and realiability criteria
- Periodic status reports to customer including frequent design reviews during a custom development program
- Technical supervision on installation of prototypes
- Implementation of warranty repair procedures
- Correlation of test data to ensure accurate records and continual quality improvement
- Close cooperation to guarantee delivery of product on schedule as well as reaction to increased/decreased production requirements

CUSTOM PRODUCT DEVELOPMENT CAPABILITY

National Memory Systems maintains a complete product development staff and facility specializing in providing cost effect solutions to a customer's specific memory requirement.

Each custom development program consists of a design team with a project engineer, his staff of engineers and technicians, and services of design and drafting support group. The schedule for a typical custom development program may vary depending upon the complexity of the program and the manpower loading to satisfy a specific customer's requirement. Typical programs range from 8 weeks to 15 weeks for delivery of prototype units. Production quantities are available within 30 days after prototype acceptance.

The Memory Systems Engineering Department works closely with the National Memory Components Group to provide the latest cost-effective custom designs to our customers using state-of-the-art components.

The Memory Systems Division has an excellent track record of completing custom design programs on schedule with rapid customer acceptance.

PRODUCTION TEST FACILITY FOR MEMORY SYSTEM PRODUCTS

Component Burn-In Station

- Dynamic testing during burn-in includes automatic voltage margining and standard pattern tests at pre burn-in and post burn-in
- Manual test capability for voltage margining and selection of specific pattern tests
- Dedicated facility capable of throughput of 100,000 devices per month. Equipment includes:
  - Despatch Oven Co. burn-in chamber
  - Dedicated error loggers
  - Custom designed controller/sequencer
- Burn-in temperature and period vary with each memory component

Single Card Test Stations

- Dedicated Macrodata MD-100 (with "custom" personality card) and error logger.
  Note: Minimum of one test station is reserved for each customer
- Complete board functional test in ambient conditions. Tests include:
  - Mem Scan
  - March
  - Checkerboard March
  - Short Walk
  - Walk Pat
  - Gal Pat
  - Complete Voltage Margins
  - Special "customer required" tests and/or test parameters

Multicard Test Stations

- Equipment includes dedicated Macrodata MD-100 (with "custom" personality card), error logger, card cage assembly and temperature chamber.
  Note: Minimum of one test station is reserved for each customer.
- Testing is performed automatically under temperature conditions. Tests include:
  - Mem Scan
  - March
  - Checkerboard March
  - Short Walk
  - Walk Pat
  - Gal Pat
  - Complete voltage margins
  - Special "customer required" tests and/or test parameters
- Testing throughput of approximately 30 cards/week per test station. Capacity easily increased to accomodate multiples of 30 cards/week to satisfy customer needs.

Special Purpose Logic Test Station

- Used to test special "custom" memory cards which contain overhead circuitry not associated with memory operation
- Testing of this special circuitry is accomplished in a comparison mode (with a working sample) on a "Trendar 2000" digital logic test station
- Special personality cards and test fixtures are developed by Memory Systems Engineering for specific customer requirements

MEMORY SYSTEMS QUALITY ASSURANCE

Memory Systems Quality Assurance Department is subdivided into two basic groups: Quality Engineering and Quality Control.

Quality Engineering has the responsibility of ensuring that design parameters offer the utmost in reliability by devoting technical expertise to memory design engineering and production test techniques.

Quality Control maintains product integrity by practicing preferred commercial computer standards on incoming, in-process and final inspection of all material. Calibration of all test equipment is traceable to the National Bureau of Standards and is scheduled and performed on a regular basis. Memory Systems' vendors are qualified by their ability to meet preferred industry standards and scheduled delivery commitments. Vendors are periodically source and first article inspected to maintain overall integrity.

By maintaining a close working relationship, Quality Control and Quality Engineering provide state-of-the-art inspection and testing of all memory systems.

MEMORY SYSTEM PRODUCTS

In the pages which follow you will find data sheets on several of National Memory Systems' standard products and systems. If one of these products matches your memory requirement, our applications department will be pleased to provide detailed interface information. Pricing and delivery information are available from your local National Semiconductor regional office.

If none of the standard products satisfy your requirement, give our Marketing Department a call or contact your local National Semiconductor regional office listed in this catalog for details on how National Memory Systems specializes in satisfying your "custom" memory system requirements. We would be pleased to learn of your needs and will respond promptly with a complete technical and business proposal.

NATIONAL

Memory Systems

Advance Information

NS3-1 high density memory system

GENERAL DESCRIPTION

The NS3-1 is a self-contained semiconductor random access memory system with a maximum capacity of 128k x 22 bits or 256 bytes.

It is structured to provide a wide range of flexibility to satisfy individual systems applications.

The memory is configured in four modular cards. Each card has a maximum capacity of 32k x 22 bits (64 bytes). The memory can be modified to individual system requirements.

The basic storage element is a 4k dynamic RAM which provides speed, proven reliability and low cost. Memory Flexibility is achieved by board de-population. Optional features are provided. These include custom interfacing, error correction, and double word control (40 bits word structure).

A remote Self-Test unit is offered as an optional accessory which exercises the memory system.

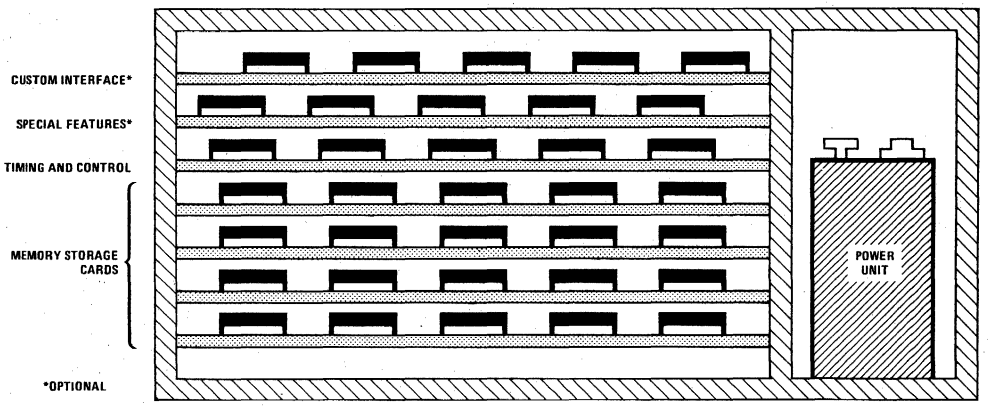
The NS3-1 system is housed in a 5 1/4" cabinet and contains its own power supply.

FEATURES

- Complete system
- Semiconductor memory
- High speed
- Low cost
- Compact
- Accessories
- Up to 128k x 22 bits (256 bytes)
- 32k x 22-bit modularity
- Byte control
- 5 1/4" cabinet
- Customized Interfacing
- Error check and correction
- TTL compatible

Optional Features

- Error check and correction
- Parity generation/parity check
- Double word control—40-bit word structure
- Late data strobe
- Custom logic interface
- Custom system interface cables



TECHNICAL SPECIFICATIONS

Modes of Operation

Write
Read
Read/Modify/Write

Performance

Access Time	280 ns
Read or Write Cycle	430 ns
Read/Modify/Write Cycle	*610 ns

*Plus user data modify time

Logic Levels

All levels are TTl compatible
Terminations are optional

Environment

Operating 0°C to +50°C
Non-operating −40°C to +80°C
Humidity 90% without condensation

Mechanical

Chassis 5 1/4" x 19" x 22 1/2"

Interfacing

Elco 90 pin (plug)
Elco 90 pin (receptacle)

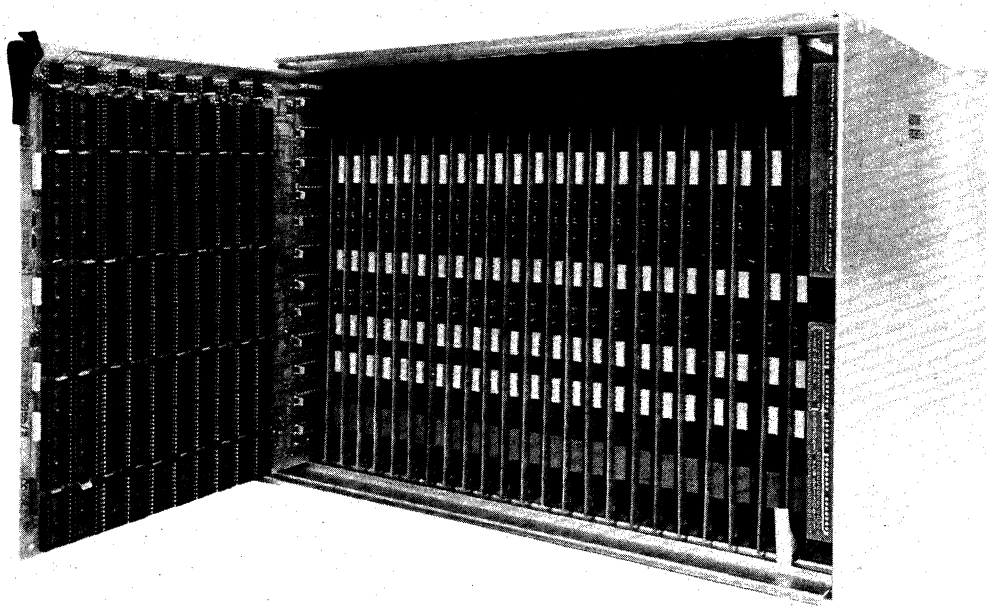
Memory Refresh

This can be implemented to individual customer applications either in a synchronous mode or in an asynchronous mode allowing handshaking with the CPU.

NATIONAL

Memory Systems

MOSRAM 310 bulk storage system
256k words X 24 bits, 128k words X 48 bits, 64k words X 96 bits



GENERAL DESCRIPTION

The MOSRAM 310 is a random access semiconductor memory system that requires only a timing and control card to be a complete memory system.

The memory is contained in a 19" rack mounted chassis that measures 12.0" H x 19.0" W x 11.5" D. The standard configuration is 256k x 24; however, the memory can be configured as either 128k x 48 or 64k x 96. Smaller capacities are available by depopulation, and larger capacities are obtained by utilizing multiple chassis.

The MOSRAM 310 is a semiconductor memory system that was designed to offer the user the highest performance and lowest bit cost available for bulk storage applications.

FEATURES

- Uses National 5280 4k RAM
- Low Cost
- High Speed
- Double Density Version Available Soon
- Separate Timing and Control Card
- Expandable
- Multiple Configurations:
  256k x 24 STD
  128k x 48 Optional
  64k x 96 Optional

TECHNICAL SPECIFICATIONS

Performance

Access Time	240 ns
Read Cycle Time	460 ns
Write Cycle Time	460 ns

Modes of Operation

Read
Write
Refresh

Power Requirements

	+5V	−5.2V
	+12V	−5.0V

Logic "1"	+2.4 V_{DC} to +5.5 V_{DC}
Logic "0"	
Input	0.0 V_{DC} to +0.6 V_{DC}
Output	0.0 V_{DC} to +0.4 V_{DC}

Environment

Operating	0°C to +50°C
Non-Operating	−40°C to +80°C
Humidity	To 90% Without Condensation

Mechanical (256k x 24)

Memory Chassis	19.0" W x 12.4" H x 11.5" D
Memory Module	10.5" x 11.0"

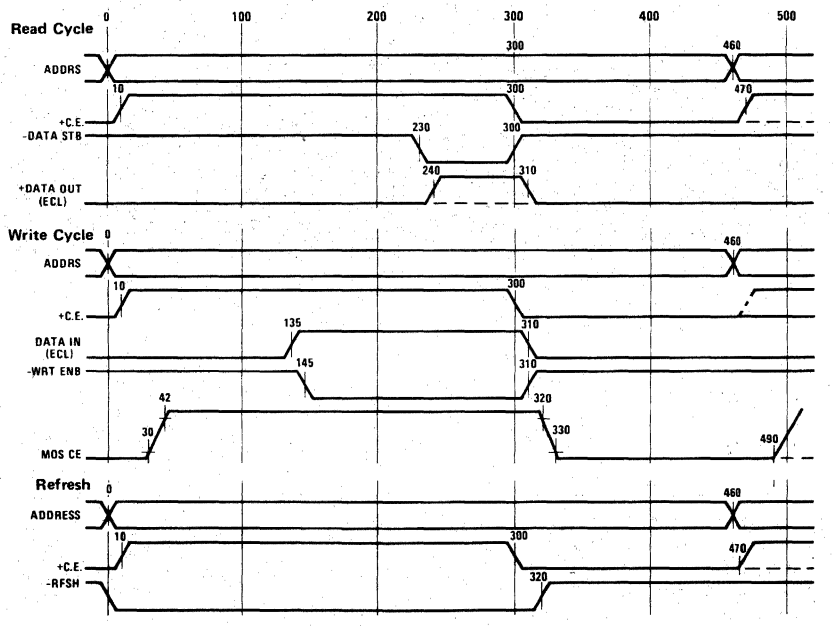
Input Signals (Storage Card)

Data 4 Bits (ECL B1–D1)	4 Lines
Address 16 Bits A0–A15	16 Lines
Read/Write Control	1 Line
MOS Timing CE	1 Line
Refresh	1 Line
Data Strobe	1 Line

Output Signals

Data 4 Bits	4 Lines

MOSRAM 310 BULK STORAGE CARD TIMING

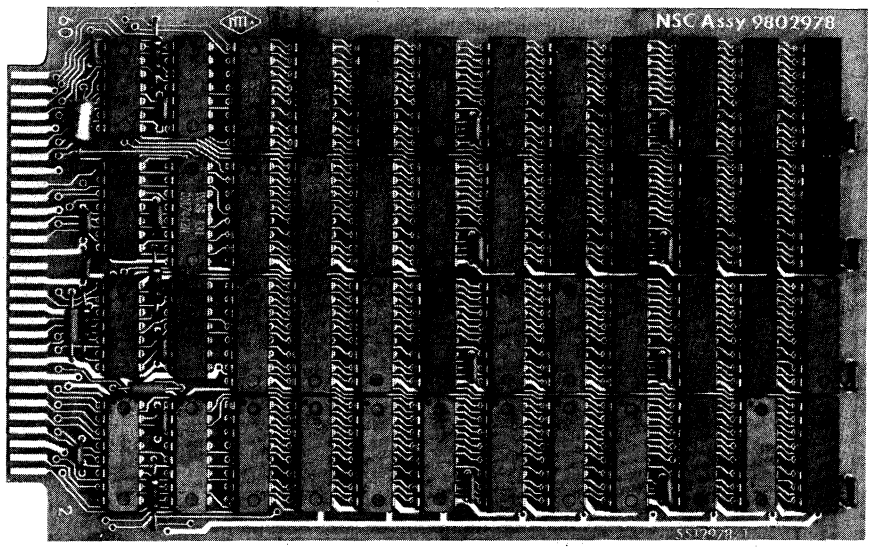


All National memory systems must meet stringent quality and test standards prior to shipment. Memory components are burned in, and systems undergo an extensive diagnostic test prior to shipment.

NATIONAL

Memory Systems

MOSRAM 410 memory system
4096 words X 10 bits



GENERAL DESCRIPTION

The MOSRAM 410 is designed to offer the systems engineer an alternative to the high cost design-prototype-test cycle. This memory system utilizes the MM2102 N-channel, 1k part as the storage medium. These static storage cells eliminate the need for clocks and refresh. Data in and data out have the same polarity and the read operation is nondestructive.

The simple interface and high performance make the MOSRAM 410 ideally suited for those memory applications, both large and small, where systems cost is an important consideration.

The only interface signals required are data in, data out, address, memory enable, and $\overline{R}/W$, all TTL compatible.

FEATURES

- Single +5.0V supply
- All inputs and outputs are DTL/TTL compatible
- Static operation—no clocks or refreshing required
- Low power 5W typ
- High speed 550 ns
- TRI-STATE® output for bus interface
- Programmable card select allows simple memory expansion to 32k x 10
- Small size 3.93 x 6.3 x 0.5 for 4k x 10
- Flexibility of speeds and capacities

TECHNICAL SPECIFICATIONS

Performance

Cycle/Access Time:	550 ns

Modes of Operation

Read
Write

Power Requirements

+5 V_{DC} at 1.0A

Interface

Logic "1"	+2.4 V_{DC} to +5.5 V_{DC}
Logic "0"	
Input	0.0 V_{DC} to +0.6 V_{DC}
Output	0.0 V_{DC} to +0.4 V_{DC}

Environment

Operating	0°C to +50°C
Non-Operating	−40°C to +80°C
Humidity	To 90% Without Condensation

Mechanical

Memory Module	3.93" x 6.3"*
Mounting	0.5" Centers
Connector	60 Pin Card Edge Type 0.100 Centers (ELCO 00-6307-060-309-001)

Input Signals

Data In, 10 Bits	10 Lines
Address 15 Bits A0–A14	15 Lines
$\overline{\text{Read}}$/Write Control	1 Line
External Output Enable	1 Line
Memory Enable	1 Line

Output Signals

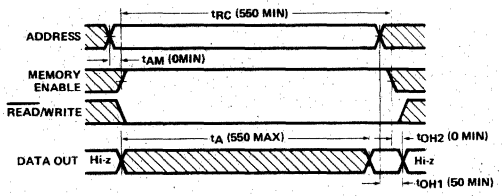
Data Out, 10 Bits	10 Lines

Memory Configurations
(Available as Follows:)

4k x 10	Model 410
4k x 9	Model 409
4k x 8	Model 408
2k x 10	Model 210
2k x 9	Model 209
2k x 8	Model 208

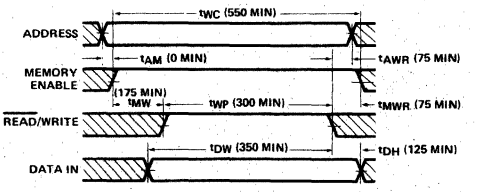
MOSRAM 410 TIMING

Read Cycle



t_{RC} (min)	550 ns
t_{AM} (min)	0
t_A (max)	550
t_{OH2} (min)	0
t_{OH1} (min)	50

Write Cycle



t_{WC} (min)	550 ns
t_{AM} (min)	0
t_{AWR} (min)	75
t_{MW} (min)	175
t_{WP} (min)	300
t_{MWR} (min)	75
t_{DW} (min)	350
t_{DH} (min)	125

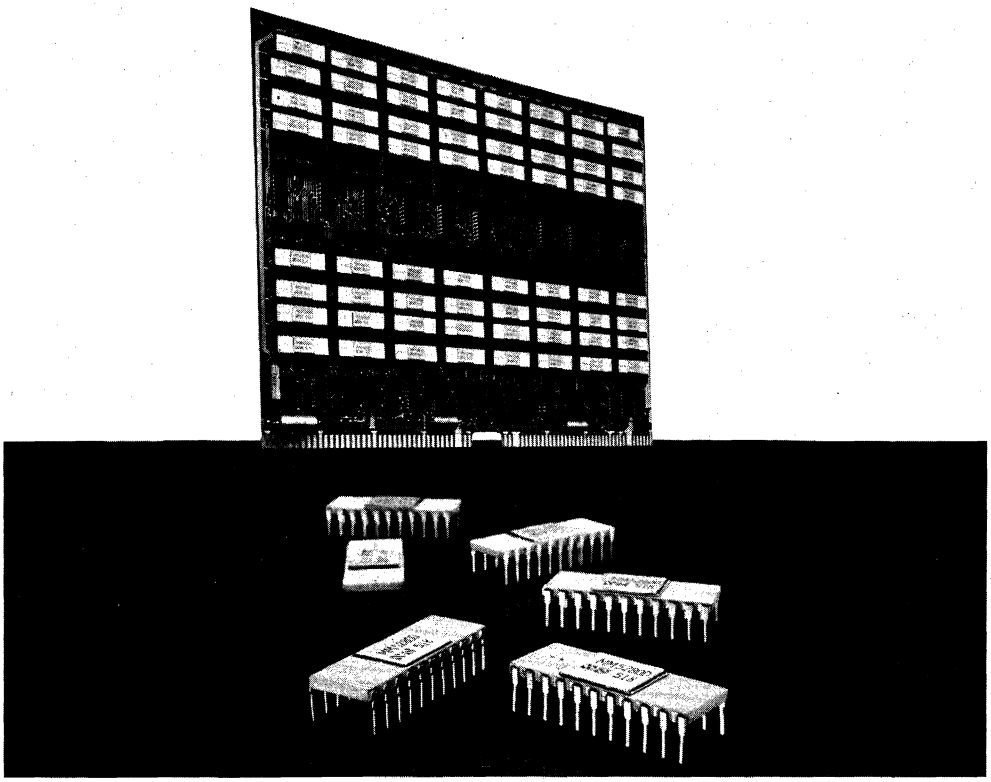
*Eurocard has 64 pin, on 0.100 centers connector.

All National memory systems must meet stringent quality and test standards prior to shipment. Memory components are burned in, and systems undergo an extensive diagnostic test prior to shipment.

NATIONAL

Memory Systems

MOSRAM 644 memory system
65536 words X 4 bits



GENERAL DESCRIPTION

The MOSRAM 644 is a high speed random access semiconductor memory that requires only a timing and control card to be a complete memory system.

The memory is contained on a printed circuit card that measures 10.0" x 11.0". The standard configuration is 64k x 4. Larger capacities are obtained by utilizing multiple storage cards.

The MOSRAM 644 is a compact planar semiconductor memory system that was designed to offer the user the highest performance and lowest bit cost available.

It is designed for a wide range of applications including large, high speed mainframe, minicomputer, and data communication systems.

FEATURES

- Low Cost
- High Speed
- Separate Timing and Control Card
- Card Select Input
- Easily Expandable
- Chassis

TECHNICAL SPECIFICATIONS

Performance

Access Time	240 ns
Read Cycle Time	460 ns
Write Cycle Time	460 ns

Modes of Operation

Read
Write
Refresh

Power Requirements

	+5 V	-5.2 V
	+12 V	-5.0 V

Interface

Logic "1"	+2.4 V_{DC} to +5.5 V_{DC}
Logic "0"	
Input	0.0 V_{DC} to +0.6 V_{DC}
Output	0.0 V_{DC} to +0.4 V_{DC}

Environment

Operating	0°C to +50°C
Non-Operating	-40°C to +80°C
Humidity	To 90% Without Condensation

Mechanical (64k x 4)

Memory Module	11.0" x 10.0"
Mounting	0.625" Centers
Connectors	Two (2) 80 Pin Card Edge Type

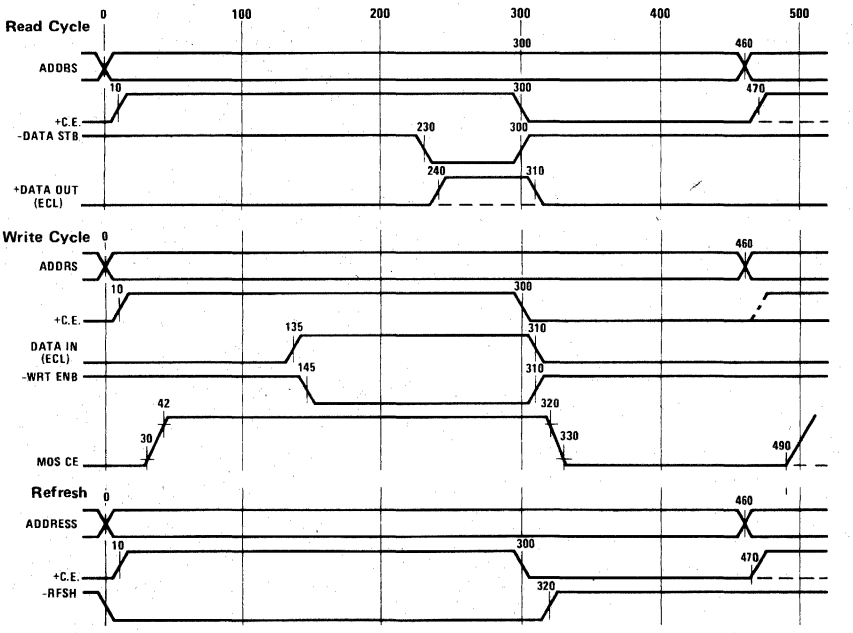
Input Signals

Data 4 Bits (ECL B1 - D1)	4 Lines
Address 16 Bits A0 - A15	16 Lines
Read/Write Control	1 Line
MOS Timing CE	1 Line
Refresh	1 Line
Data Strobe	1 Line

Output Signals

Data 4 Bits	4 Lines

MOSRAM 644 — 64 k x 4 TIMING

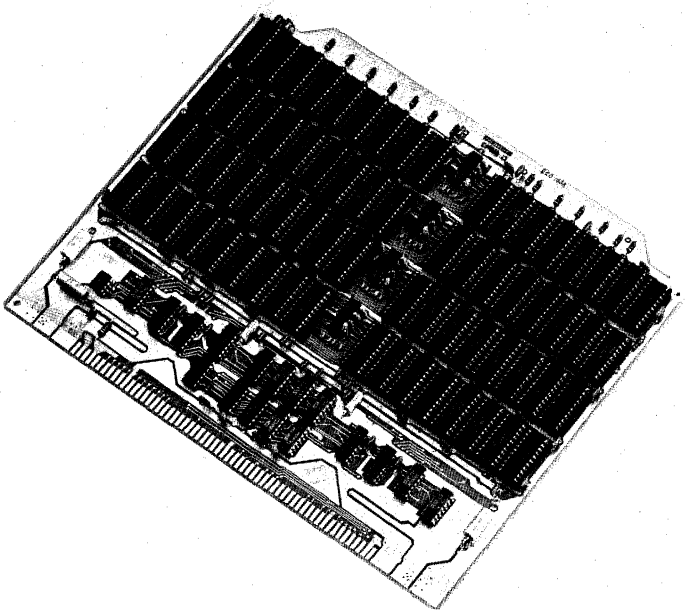


All National memory systems must meet stringent quality and test standards prior to shipment. Memory components are burned in, and systems undergo an extensive diagnostic test prior to shipment.

NATIONAL

Memory Systems

MOSRAM 817 memory system
8192 words X 17 bits



GENERAL DESCRIPTION

The MOSRAM 817 is a random access semiconductor memory that requires only a timing and control card to be a complete memory system.

The memory is contained on a printed circuit card that measures 9.0" x 11.0". The standard configuration is 8k x 17. Smaller capacities are available by depopulation, and larger capacities are obtained by utilizing multiple storage cards.

The MOSRAM 817 is a compact planar semiconductor memory system that was designed to offer the user high performance and low bit cost.

It is designed for a wide range of applications including mainframe, minicomputer intelligent terminals, data communication, data entry, and microprocessor extension memory. The card is compatible with National's IMP-16 microprocessor.

FEATURES

- Low Cost
- High Speed
- Output Data Registers
- Separate Timing and Control Card
- Card Select Input
- Expandability to Eight Cards (64k)

TECHNICAL SPECIFICATIONS

Performance

Access Time	500 ns
Read Cycle Time	505 ns
Write Cycle Time	690 ns
Read/Modify/Write	780 ns + Modify Time

Modes of Operation

Read
Write
Split Cycle (Read/Modify/Write)

Power Requirements

+5 V_{DC} at 1.5 A, -15 V_{DC} at 0.5 A, +15 V_{DC} at 0.1 A

Interface

Logic "1"	+2.4 V_{DC} to +5.5 V_{DC}
Logic "0"	
Input	0.0 V_{DC} to +0.6 V_{DC}
Output	0.0 V_{DC} to +0.4 V_{DC}

Environment

Operating	0°C to +60°C
Non-Operating	-40°C to +80°C
Humidity	To 90% Without Condensation

Mechanical (8k x 17)

Memory Module	9.0" x 11.0"
Mounting	0.625" Centers
Connector	1 Each 144 Pin

Input Signals

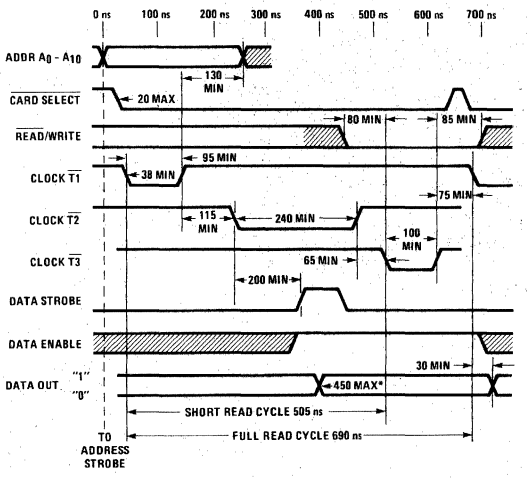
Data 17 Bits	17 Lines
Address 13 Bits A0 - A12	13 Lines
Read/Write Control	1 Line
MOS Timing T1 T2 T3	3 Lines
Refresh	1 Line
Data Out Enable	1 Line
Data Strobe	1 Line
Card Select	1 Line

Output Signals

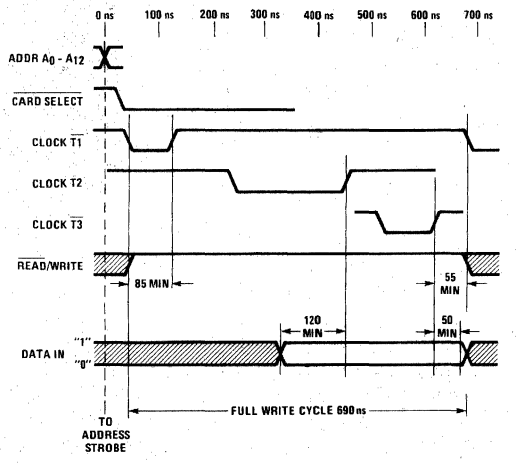
Data 17 Bits	17 Lines

MOSRAM 817 8k x 17 TIMING

Read Cycle



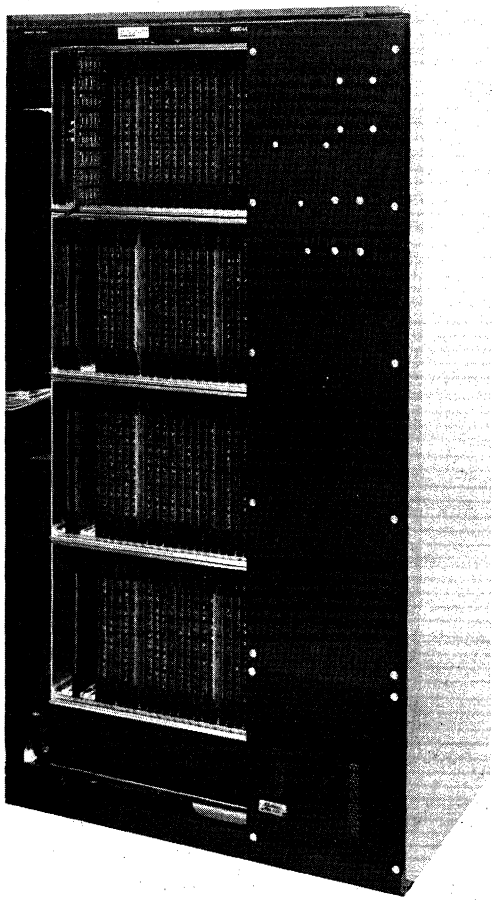
Write Cycle



NATIONAL

Memory Systems

BSM 1000 memory system
512k to 1 megaword



GENERAL DESCRIPTION

The National Memory Systems BSM 1000 add-on memory is a low cost, high performance bulk storage memory. The memory is designed for storage capability from 512k to a total of 1 megaword. The system is self-contained with power supply, cooling and other options in an attractive 31" x 18" x 60" enclosure.

The BSM 1000 uses high speed 4k RAMs which are utilized on the MOSRAM 644 storage card. The MOSRAM 644 (65,536 x 4) card is the basic building block for the system. In addition, timing/control and custom interface cards are supplied. The system design is readily adaptable to meet many custom applications. Applications include add-on memory to the IBM 370/158 Bulk Storage Module and other high speed systems.

FEATURES

- Field Proven
- Low Cost
- High Speed
- Low Power Consumption
- Compact Size
- Chassis, Rack, Power Supplies

TECHNICAL SPECIFICATIONS

Performance

Access Time	270 ns
Read Cycle Time	460 ns
Write Cycle Time	460 ns

Power Requirements

60 Hz	208-240 V_{AC}	30 A		3-Phase Delta
50 Hz	380-415 V_{AC}	30 A		3-Phase Wye
60 Hz	Plug	30 A	R&S	#FS3760
60 Hz	Connector	30 A	R&S	#FS3934
60 Hz	Receptacle	30 A	R&S	#FS3754

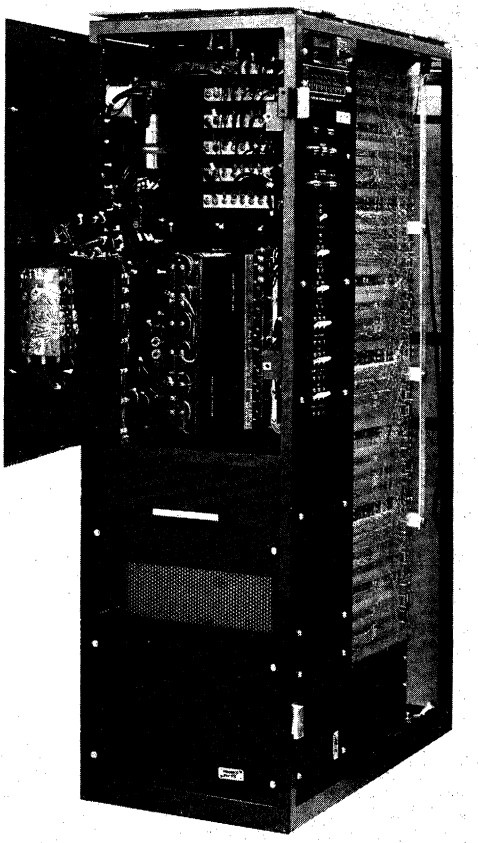
Environment

Operational:	
Temperature	+10°C to +40°C
Relative Humidity	20% to 90%
Maximum Wet Bulb	+26°C
Non-Operational	
Temperature	-46°C to +43°C
Relative Humidity	20% to 90%
Maximum Wet Bulb	+27°C

Mechanical

Specific Physical Planning Data for the National Memory System BSM 1000 is listed below:

Dimensions:	31" W (78.7 cm) 18" D (45.7 cm) 60" H (152.4 cm)
Weight	700 lbs (317.5 kg)
KVA Rating	2.9 KVA
KW Rating	2.4 KW
Heat Output	7,215 BTU/hr
Airflow	690 cf/min (19.54 cm/min)



BSM 1000 (rear view)

SPECIAL FEATURES

- Easy Maintenance
- Control Panels
- Power Supply Monitors
- Configuration Flexibility
- Easy Expandability

OPTIONS

- Custom Interfaces
- Error Correction & Control
- Configurations
  - Flexible Word Length (8 to 20 Bits)
  - Expandable Word Capacity (4k Increments) from 256k to 1 Megaword

All National memory systems must meet stringent quality and test standards prior to shipment. Memory components are burned in, and systems undergo an extensive diagnostic test prior to shipment.

NATIONAL

Memory Systems

Advance Information

NS3000-1 memory system
16k words X 20 bits

GENERAL DESCRIPTION

The NS3000-1 is a random access semiconductor memory contained on a single printed circuit card. Standard configurations are 16k x 16, 18 and 20 bits with individual 8, 9 or 10-bit byte structure as an option.

Design flexibility permits customized applications. Options include parity generation, parity check, late data input and data available reset.

The NS3000-1 is designed for a wide range of applications including mainframe computers, mini-computers, microprocessor-based systems, intelligent terminals and data entry.

FEATURES

- Low cost
- High speed
- Proven reliability
- Low power
- Special options
- Designed to incorporate special customer requirements
- Bi-directional data transmission if required
- TTL compatible

Standard Features

- Byte mode
- Late Data In—enables late presentation of data for write operation

Special Options

The following is available on a customized basis:
- Parity check
- Parity generation
- Data Available Reset—permits Data Available (DA) to be gated within the memory cycle. It can be used to release the data bus in a shared system.

TECHNICAL SPECIFICATIONS

Modes of Operation

Write Read
Read/Modify/Write

Performance

Access Time	280 ns
Read or Write Cycle	430 ns
Read/Modify/Write Cycle	*610 ns

*Plus user data modify time

Environment

Operating: 0°C to +50°C
Non-operating: −40°C to +80°C
Humidity: 90% without condensation

Mechanical

Card Size: 11.75" x 15.40"
Connectors: 2 each 80 pin edge connectors with pins space "125" center to center

Input Signals

- Initiate Pulse (RP)
- Byte Control Levels (BLC1, BLC2)
- Split Cycle (SC)
- Write Pulse (WP)
- Configuration Option (4 Lines)
- Address In (AI)
- Extended Address IN (XAI)
- Data In (DI)
- Memory Protect (MP)

Logic Levels

All levels are negative true TTL compatible. Terminations are optional.

Memory Organization

- Memory storage
- Timing and control
- Refresh circuitry
- Optional features

Note: The memory size may be reduced by board depopulation.

Output Signals

- Data Out (DO)
- Data Available (DA)
- Memory Busy (MB)

TECHNICAL SPECIFICATIONS (CON'T)

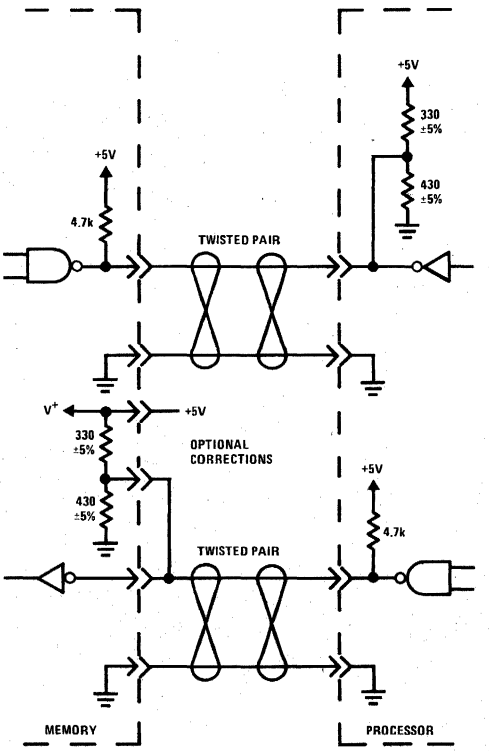
Power Requirements

Standard +15V, −15V, +5V
Option* +12V, −5V, +5V
*Lower cost

Memory Refresh

This can be implemented to individual customer applications either in a synchronous mode or in an asynchronous mode allowing hand shaking with the CPU.

Typical Memory Card Interface



NATIONAL

Memory Systems

Advance Information

NS3000-2 memory system 32k words X 18 bits

GENERAL DESCRIPTION

The NS3000-2 is a random access semiconductor memory contained on a single printed circuit card. Standard configuration is 32k x 16 or 18 bits which is alterable to 64k x 8, 9 using byte control.

Design flexibility permits customized applications. Special features include late data input and data available reset.

The NS3000-2 is designed for a wide range of high density memory applications including mainframe computers, mini-computers, microprocessor-based systems, intelligent terminals and data entry.

FEATURES

- Low cost
- High speed
- Proven reliability
- Low power
- Special options
- Designed to incorporate special customer requirements
- Bi-directional data transmission if required
- TTL compatible

Standard Features

- Byte mode
- Late Data In—enables late presentation of data for write operation
- Data Available Reset—permits Data Available (DA) to be gated within the memory cycle. It can be used to release the data bus in a shared system.

TECHNICAL SPECIFICATIONS

Modes of Operation

Write
Read

Environment

Operating: 0°C to +50°C
Non-operating: −40°C to +85°C
Humidity: 90% without condensation

Performance

Access Time	275 ns
Read or Write Cycle	430 ns

Input Signals

- Initiate Pulse (RP)
- Byte Control Levels (BLC1, BLC2)
- Address In (AI)
- Data In (DI)
- General Reset

Output Signals

- Data Out (DO)
- Data Available (DA)
- Memory Busy (MB)

Logic Levels

All levels are negative true TTL compatible. Terminations are optional.

Memory Organization

- Memory storage
- Timing and control
- Refresh circuitry
- Special features

Note: The memory size may be reduced by board depopulation.

Mechanical

Card size: 11.75" x 15.40"
Connectors: 2 each 80 pin edge connectors with pin spaced "125" center to center

Power Requirements

Standard: +15V, −15V, +5V
Option: +12V, −5V, +5V*

*Lower cost

Common Data Bus

Gating is provided on the Data Input and Data Output circuits to allow bi-directional data transmission if desired.

Memory Refresh

This can be implemented to individual customer applications either in a synchronous mode or in an asynchronous mode allowing hand shaking with the CPU.

DS0025/DS0025C two phase MOS clock driver

general description

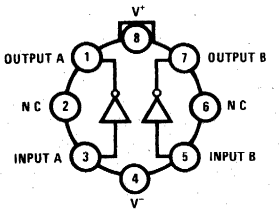
The DS0025/DS0025C is monolithic, low cost, two phase MOS clock driver that is designed to be driven by TTL/DTL line drivers or buffers such as the DM932, DS8830 or DM7440. Two input coupling capacitors are used to perform the level shift from TTL/DTL to MOS logic levels. Optimum performance in turn-off delay and fall time are obtained when the output pulse is logically controlled by the input. However, output pulse widths may be set by selection of the input capacitors eliminating the need for tight input pulse control.

features

- 8-lead TO-5 or 8-lead dual-in-line package
- High Output Voltage Swings—up to 30V
- High Output Current Drive Capability—up to 1.5A
- Rep. Rate: 1.0 MHz into > 1000 pF
- Driven by DM932, DS8830, DM7440 (SN7440)
- "Zero" Quiescent Power

connection diagrams

Metal Can Package

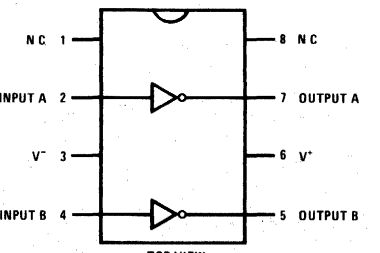


Note: Pin 4 connected to case.

TOP VIEW

Order Number DS0025H or DS0025CH
See Package 23

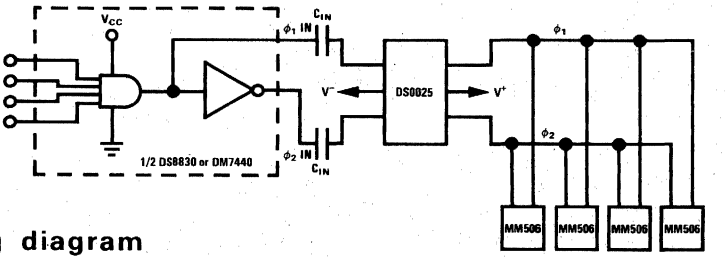
Dual-In-Line Package



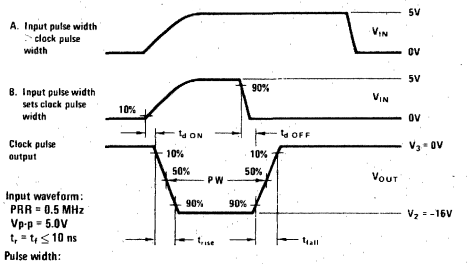
TOP VIEW

Order Number DS0025CN
See Package 12

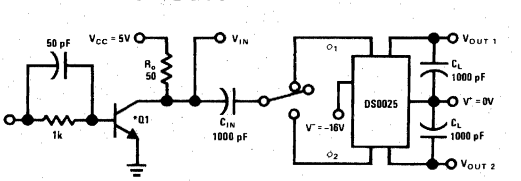
typical application



timing diagram



ac test circuit



*Q1 is selected high speed NPN switching transistor.

NATIONAL

DS0026, DS0056 5 MHz two phase MOS clock drivers

general description

DS0026/DS0056 are low cost monolithic high speed two phase MOS clock drivers and interface circuits. Unique circuit design provides both very high speed operation and the ability to drive large capacitive loads. The device accepts standard TTL/DTL outputs and converts them to MOS logic levels. They may be driven from standard 54/74 series and 54S/74S series gates and flip-flops or from drivers such as the DS8830 or DM7440. The DS0026 and DS0056 are intended for applications in which the output pulse width is logically controlled; i.e., the output pulse width is equal to the input pulse width.

The DS0026/DS0056 are designed to fulfill a wide variety of MOS interface requirements. As a MOS clock driver for long silicon-gate shift registers, a single device can drive over 10k bits at 5 MHz. Six devices provide input address and precharge drive for a 8k by 16-bit 1103 RAM memory system. Information on the correct usage of the DS0026 in these as well as other systems is included in the application note AN-76A.

The DS0026 and DS0056 are identical except each driver in the DS0056 is provided with a V_{BB} connection to supply a higher voltage to the output stage. This aids in pulling up the output when it is in the high state. An external resistor tied between these extra pins and a supply higher than V^+ will cause the output to pull up to ($V^+ - 0.1V$) in the off state.

For DS0056 applications, it is required that an external resistor be used to prevent damage to the device when the driver switches low. A typical V_{BB} connection is shown on the next page.

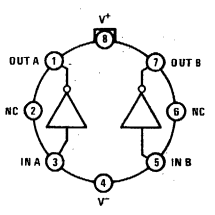
These devices are available in 8-lead TO-5, one watt copper lead frame 8-pin mini-DIP, and one and a half watt ceramic DIP, and TO-8 packages.

features

- Fast rise and fall times—20 ns with 1000 pF load
- High output swing—20V
- High output current drive—±1.5 amps
- TTL/DTL compatible inputs
- High rep rate—5 to 10 MHz depending on power dissipation
- Low power consumption in MOS "0" state—2 mW
- Drives to 0.4V of GND for RAM address drive

connection diagrams (Top Views)

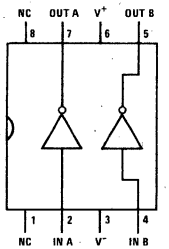
TO-5 Package



Note: Pin 4 connected to case.

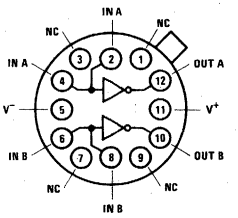
Order Number DS0026H or DS0026CH
See Package 23

Dual-In-Line Package



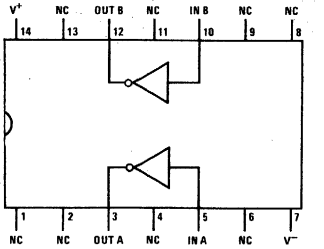
Order Number DS0026CN
See Package 12

TO-8 Package



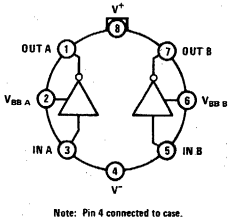
Order Number DS0026G or DS0026CG
See Package 25

Dual-In-Line Package



Order Number DS0026J, DS0026CJ or DS0026W
See Package 9 or 27

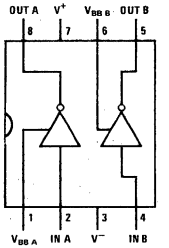
TO-5 Package



Note: Pin 4 connected to case.

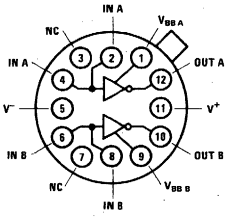
Order Number DS0056H or DS0056CH
See Package 23

Dual-In-Line Package



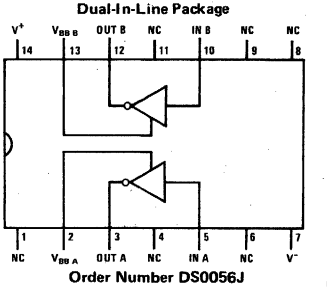
Order Number DS0056CN
See Package 12

TO-8 Package



Order Number DS0056G or DS0056CG
See Package 25

Dual-In-Line Package



Order Number DS0056J or DS0056CJ
See Package 9

NATIONAL

Interface

DS1603/DS3603, DS3604, DS55107/DS75107, DS55108/DS75108, DS75207, DS75208 dual line receivers

general description

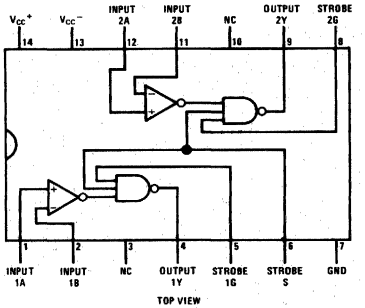
The nine products described herein are TTL compatible dual high speed circuits intended for sensing in a broad range of system applications. While the primary usage will be for line receivers or MOS sensing, any of the products may effectively be used as voltage comparators, level translators, window detectors, transducer preamplifiers, and in other sensing applications. As digital line receivers the products are applicable with the DS55109/DS75109 and DS55110/DS75110 companion drivers, or may be used in other balanced or unbalanced party-line data transmission systems. The improved input sensitivity and delay specifications of the DS75207, DS75208 and DS3604 make them ideal for sensing high performance MOS memories as well as high sensitivity line receivers and voltage comparators. TRI-STATE® products enhance bused organizations.

features

- Diode protected input stage for power "OFF" condition
- 17 ns typ high speed
- TTL compatible
- ±10 mV or ±25 mV input sensitivity
- ±3V input common-mode range
- High input impedance with normal V_{CC}, or V_{CC} = 0V
- Strobes for channel selection
- TRI-STATE outputs for high speed buses
- Dual circuits
- Sensitivity gntd. over full common-mode range
- Logic input clamp diodes—meets both "A" and "B" version specifications
- ±5V standard supply voltages

connection diagrams

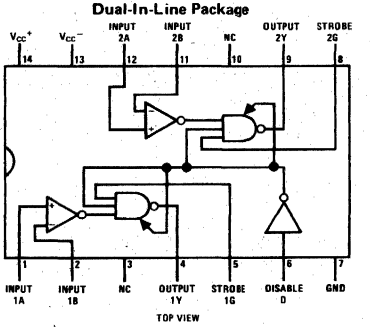
Dual-In-Line Package



TOP VIEW

Order Number DS55107J, DS75107J, DS55108J, DS75108J, DS75207J or DS75208J
See Package 9
Order Number DS75107N, DS75108N, DS75207N or DS75208N
See Package 14
Order Number DS55107W or DS55108W
See Package 27

Dual-In-Line Package



TOP VIEW

Order Number DS1603J, DS3603J DS3604J or DS1603W
See Package 9 or 27
Order Number DS3603N or DS3604N
See Package 14

product selection guide

TEMPERATURE→ / PACKAGE→	$-55°C \leq T_A \leq +125°C$ CAVITY DIP	$0°C \leq T_A \leq +70°C$ CAVITY OR MOLDED DIP	
INPUT SENSITIVITY→ / OUTPUT LOGIC↓	±25 mV	±25 mV	±10 mV
TTL Active Pull-up	DS55107	DS75107	DS75207
TTL Open Collector	DS55108	DS75108	DS75208
TTL TRI-STATE	DS1603	DS3603	DS3604

NATIONAL

DS1605/DS3605, DS1606/DS3606, DS1607/DS3607, DS1608/DS3608 hex MOS sense amplifiers (MOS to TTL converters)

general description

The DS3605 series is a new series of programmable hex MOS sense amplifiers featuring high speed direct MOS sense capability with high impedance states to allow use of a common bus line. The DS1605/DS3605 and the DS1606/DS3606 have TRI-STATE® outputs. The DS1607/DS3607 and DS1608/DS3608 have both TRI-STATE inputs and outputs. High impedance states are controlled by an enable input.

Input current threshold (the level at which the output changes state) is determined by the current at the programming pin. The current threshold is 100μA with the programming pin grounded and 250μA with the pin unconnected. The threshold can be set from 100μA to 300μA by connecting a resistor from the pin to ground, and set above 300μA by connecting a resistor from the pin to the positive supply.

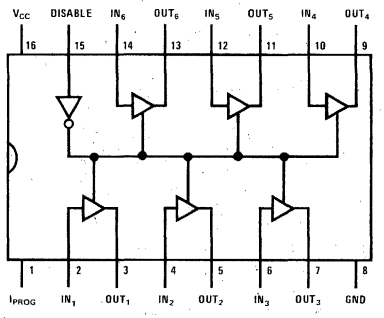
Outputs are high current drivers capable of sinking 50 mA in the low state and sourcing 5 mA in the high state.

features

- Non-inverting inputs (DS1605/DS3605, DS1607/DS3607)
- Inverting inputs (DS1606/DS3606, DS1608/DS3608)
- No external components required (direct MOS sensing)
- Programmable input thresholds
- Current sensing—100μA minimum
- 50 mA drive capability
- TRI-STATE control
- Single 5V supply
- 15 ns typical propagation delay (DS3605)

connection diagram

Dual-In-Line Package



TOP VIEW

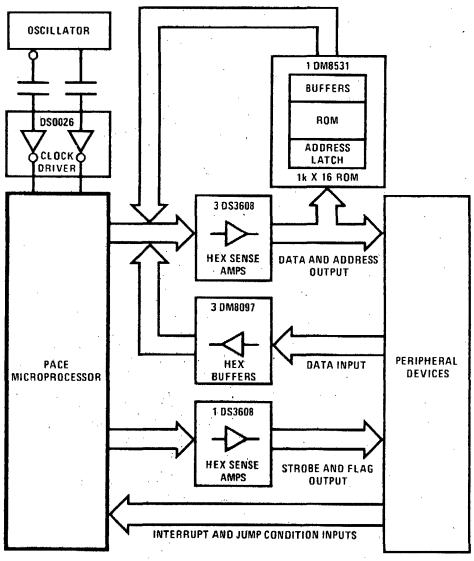
ordering information

ORDER NUMBERS	PACKAGE
DS1605J, DS1606J, DS1607J, DS1608J	Cavity DIP (J)
DS3605J, DS3606J, DS3607J, DS3608J	Cavity DIP (J)
DS3605N, DS3606N, DS3607N, DS3608N	Molded DIP (N)

See Package 10 or 15

typical application

PACE Interface



DS3608 shown as an interface between the PACE microprocessor and TTL data bus and I/O bus.

DS3625 dual high speed MOS sense amp

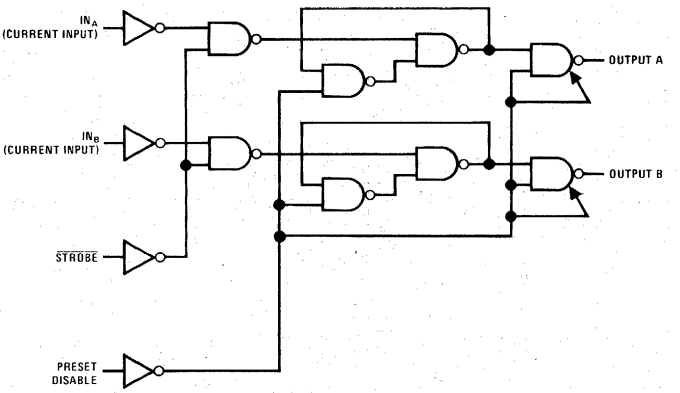
general description

The DS3625 is a dual high speed MOS to TTL level converter. It acts as an interface level converter between MOS and TTL logic devices. It consists of two 1-input converters with common strobe input to inhibit "0" entry when strobe is high. It allows parallel entry when strobe is low and the internal latch is preset by the common preset input. TRI-STATE® output logic is implemented in this circuit to facilitate high speed time sharing of decoder-drivers, fast random-access (or sequential) memory arrays, etc.

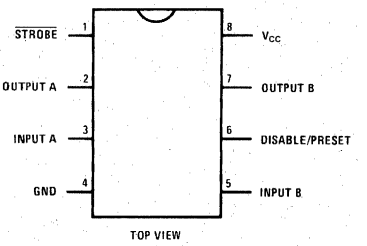
features

- Easily interfaces with most popular 1k and 2k dynamic MOS RAMs
- Pin-for-pin replacement for the 8T25
- Very low output impedance — high drive ability
- High impedance output state which allows many outputs to be connected to a common bus line
- Average power dissipation 110 mW per converter

logic and connection diagrams



Dual-In-Line Package



TOP VIEW

Order Number DS3625N
See Package 12

NATIONAL

Interface

DS3629 memory driver with decode inputs

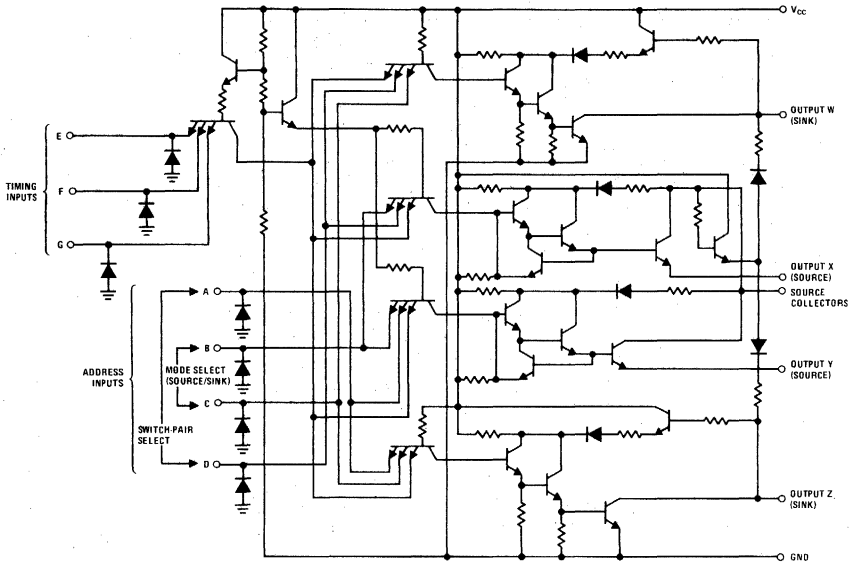
general description

The DS3629 is a monolithic memory driver which features two 400 mA (source/sink) switch pairs along with decoding capability from four address lines. Inputs B and C function as mode selection lines (source or sink) while lines A and D are used for switch-pair selection (output pair Y/Z or W/X). The DS3629 has the same pin-out and function as the DS75324 except that the source emitter voltage capability has been raised from 3V to 7V. This allows the DS3629 to drive larger memory systems at the same current levels of the DS75324.

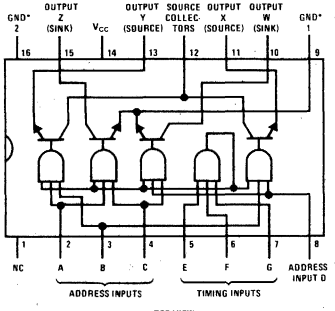
features

- Source emitter voltage of 7V (max) at 400 mA source
- Identical pin-out and function as DS75324
- 400 mA output capability
- High voltage outputs
- Dual sink/source outputs
- Internal decoding and timing circuitry
- Fast switching times
- DTL/TTL compatible
- Input clamping diodes

schematic and connection diagrams



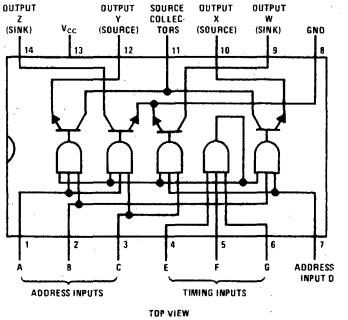
Dual-In-Line Package



*GND 1 and GND 2 are to be used in parallel.

Order Number DS3629J
See Package 10

Dual-In-Line Package



Order Number DS3629N
See Package 14

NATIONAL

Interface

Advance Information*

DS1640/DS3640, DS1670/DS3670 quad MOS TRI-SHARE™ port drivers

general description

The DS1640/DS3640 and DS1670/DS3670 are quad MOS TRI-SHARE port drivers with outputs designed to drive large capacitive loads up to 500 pF associated with MOS memory systems. PNP input transistors are employed to reduce input current, allowing the large fan-out to these drivers needed in memory systems. The circuit has Schottky-clamped transistor logic for minimum propagation delay.

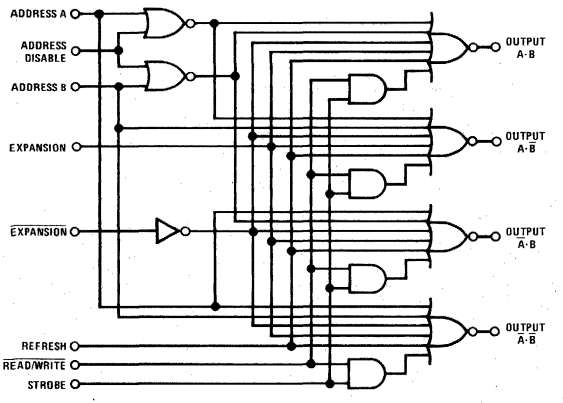
The DS1640/DS3640 has a 15 ohm resistor in series with the outputs to dampen transients caused by the fast switching output circuit. The DS1670/DS3670 has a direct, low impedance output source for use with or without an external resistor.

The DS1640/DS1670 has two address inputs which decode to one-of-four-high outputs. Provisions are made for address expansion. For example, two packages may be used to implement a three-input, eight-output decoder. Also included is a refresh control, read/write, and strobe input. These functions are required by the MM5270 4k TRI-SHARE MOS RAM.

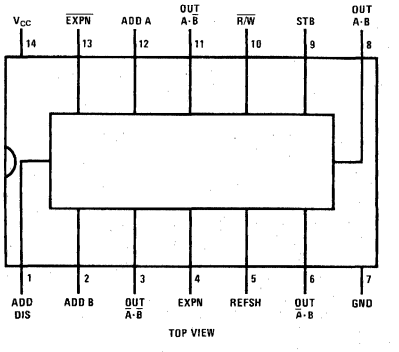
features

- TRI-SHARE port driver for MM5270 RAM
- TTL/DTL compatible inputs
- PNP inputs minimize loading
- Capacitance-driving outputs
- Built-in damping resistor (DS1640/DS3640)

logic and connection diagrams

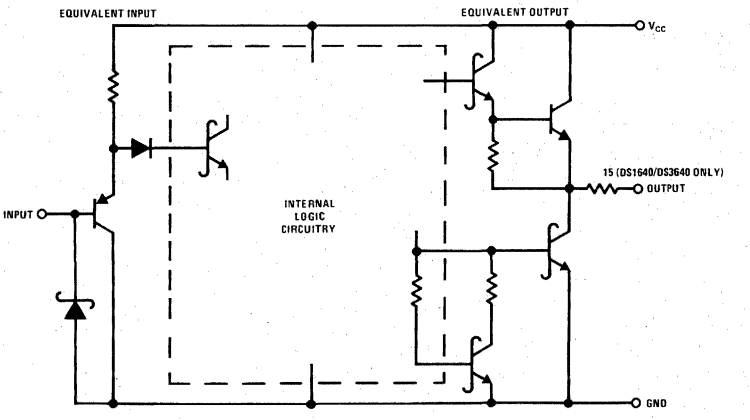


Dual-In-Line Package



Order Number DS1640J, DS1670J, DS3640J, DS3670J, DS3640N or DS3670N
See Package 9 or 14

schematic diagram



*Specifications may change.

NATIONAL

Interface

Advance Information*

DS1642/DS3642, DS1672/DS3672 dual bootstrapped MOS clock driver

general description

The DS1672 is a dual bipolar-to-MOS clock driver designed to provide high output current and voltage capabilities necessary for driving high capacitance (up to 500 pF) MOS memory systems. The circuit needs only one power supply, (12V typical). This feature greatly reduces high stand-by power levels and at the same time simplifies system design.

The circuit also features output bootstrapping capability. This feature eliminates the need for an additional high level supply to provide a higher voltage to the output stage. The function is accomplished by connecting a small value capacitor (typically 200 pF) from each output to each driver's bootstrap pin.

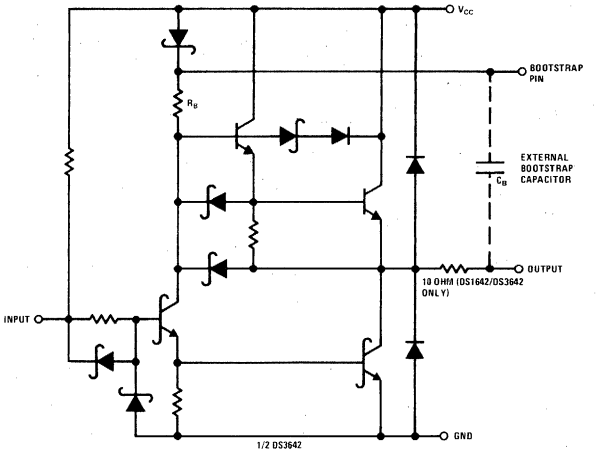
The circuit has Schottky-clamped transistor logic for minimum propagation delay. Typical stand-by power (output low) is 45 mW per driver. A fail-safe condition is provided for in the circuit, so if the input is opened the output assumes the logic "0" state.

The DS1642/DS3642 has a 10 ohm resistor in series with each output to dampen transients caused by the fast-switching output. The DS1672/DS3672 has a direct low impedance output for use with or without an external resistor.

features

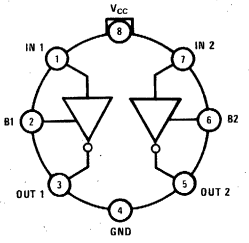
- 15V output voltage capability
- TTL/DTL compatible inputs
- High speed operation
- Bootstrapping eliminates extra supplies—reduces power
- 45 mW/driver stand-by power
- Built-in 10 ohm damping resistor (DS1642/DS3642)

schematic diagram



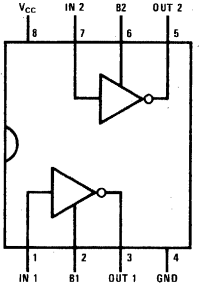
connection diagrams (Top Views)

Metal Can Package



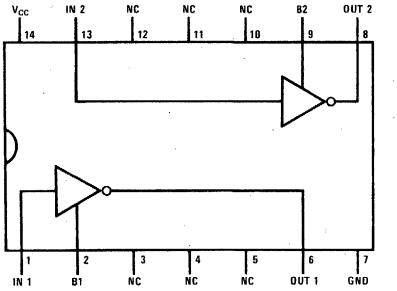
Order Number DS1642H, DS3642H, DS1672H or DS3672H
See Package 23

Dual-In-Line Package



Order Number DS3642N or DS3672N
See Package 12

Dual-In-Line Package



Order Number DS1642J, DS3642J, DS1672J or DS3672J
See Package 9

*Specifications may change.

NATIONAL

Interface
Advance Information*

DS3643, DS3673 decoded quad MOS clock drivers

general description

The DS3643 and DS3673 are quad bipolar-to-MOS decoder/clock drivers with TTL/DTL compatible inputs. They are designed to provide high output current and voltage capabilities necessary for optimum driving of high capacitance N-channel MOS memory systems.

The device features full decoding of input address lines from two inputs to one of four outputs. Also featured is the capability of expanding to three inputs to one of eight outputs with the use of the Expansion and $\overline{\text{Expansion}}$ inputs. Also included are clock and refresh inputs.

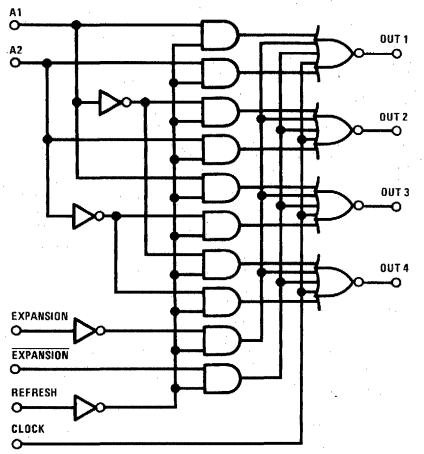
The circuit was designed for driving large capacitive loads at high speeds and uses Schottky-clamped transistors. PNP transistors are used on all inputs, thereby minimizing input loading.

The DS3643 has a 10 ohm damping resistor in series with each output to dampen transients caused by the fast switching output, while the DS3673 has a direct, low impedance output, for use with or without an external resistor.

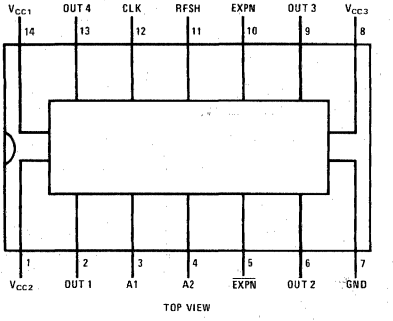
features

- TTL/DTL compatible inputs
- Operates from standard bipolar and MOS supplies
- PNP inputs minimize input loading
- Full logic decoding for either two inputs to one of four outputs or three inputs to one of eight outputs
- High voltage/current outputs
- Input and output clamping diodes
- Control logic optimized for use with MOS memory systems
- Built-in damping resistors (DS3643)

logic and connection diagrams



Dual-In-Line Package



TOP VIEW

Order Number DS3643J or DS3643N
Order Number DS3673J or DS3673N
See Package 9 or 14

truth table

INPUTS						OUTPUTS			
CLOCK	REFRESH	EXPANSION	$\overline{\text{EXPANSION}}$	A_2	A_1	OUT 1	OUT 2	OUT 3	OUT 4
1	X	X	X	X	X	0	0	0	0
0	1	X	X	X	X	1	1	1	1
0	0	1	0	0	0	1	0	0	0
0	0	1	0	0	1	0	1	0	0
0	0	1	0	1	0	0	0	1	0
0	0	1	0	1	1	0	0	0	1
0	0	1	1	X	X	0	0	0	0
0	0	0	1	X	X	0	0	0	0
0	0	0	0	X	X	0	0	0	0

X = Don't Care State.

*Specifications may change.

NATIONAL

Interface
Advance Information*

DS3644, DS3674 quad MOS clock drivers

general description

The DS3644 and DS3674 are quad bipolar-to-MOS clock drivers with TTL/DTL compatible inputs. They are designed to provide high output current and voltage capabilities necessary for optimum driving of high capacitance N-channel MOS memory systems.

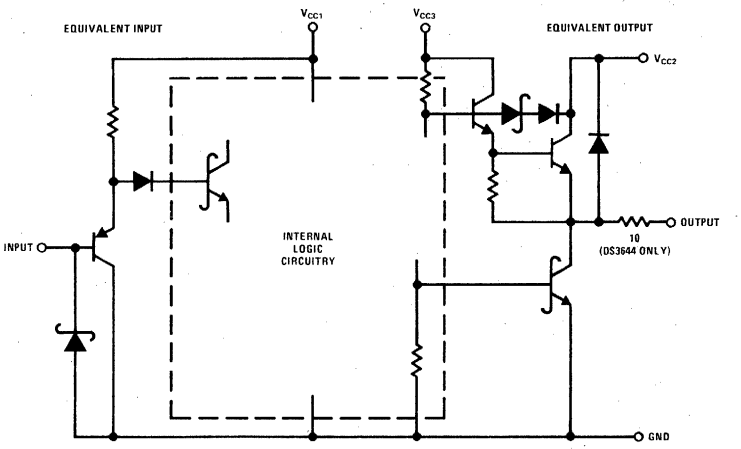
The device features two common enable inputs, a refresh input, and a clock control input for simplified system designs. The circuit was designed for driving highly capacitive loads at high speeds and uses Schottky-clamped transistors. PNP transistors are used on all inputs thereby minimizing input loading.

The DS3644 contains a 10 ohm resistor in series with each output to dampen the transients caused by the fast-switching output, while the DS3674 has a direct, low impedance output for use with or without an external damping resistor.

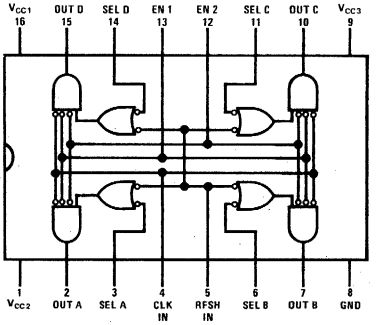
features

- TTL/DTL compatible inputs
- Operates from standard bipolar and MOS supplies
- PNP inputs minimize loading
- High voltage/current outputs
- Input and output clamping diodes
- Control logic optimized for use with MOS memory systems
- Pin and function compatible with MC3460 and 3235
- Built-in damping resistors (DS3644)

schematic and connection diagrams



Dual-In-Line Package



TOP VIEW

Order Number DS3644J, DS3674J, DS3644N or DS3674N
See Package 10 or 15

*Specifications may change.

NATIONAL

Interface
Advance Information*

DS1645/DS3645, DS1675/DS3675 hex TRI-STATE® MOS latch/drivers

general description

The DS1645/DS3645 and DS1675/DS3675 are hex MOS latch/drivers with outputs designed to drive large capacitive loads up to 500 pF associated with MOS memory systems. PNP input transistors are used to reduce input currents, allowing the large fan-out to these drivers needed in memory systems. The circuit has Schottky-clamped transistor logic for minimum propagation delay, and TRI-STATE® outputs which allow bus operation.

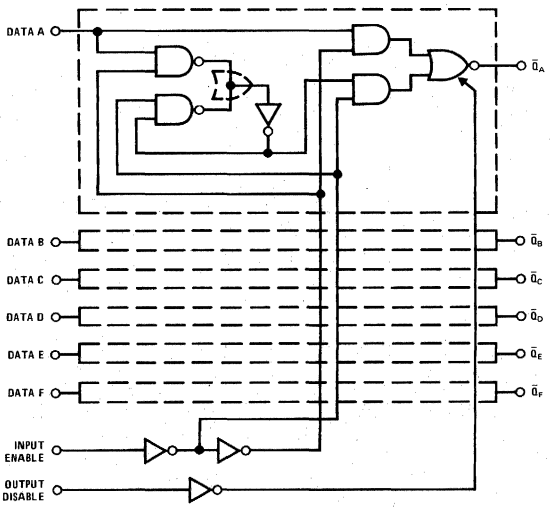
The DS1645/DS3645 has a 15 ohm resistor in series with the outputs to dampen transients caused by the fast switching output circuit. The DS1675/DS3675 has a direct, low impedance output for use with or without an external resistor.

The circuit employs a fall-through-latch which captures the data in parallel with the output, thereby eliminating the delay normally encountered in other latch circuits. The DS1645/DS3645 and DS1675/DS3675 may be used for input address lines or input/output data lines of a MOS memory system.

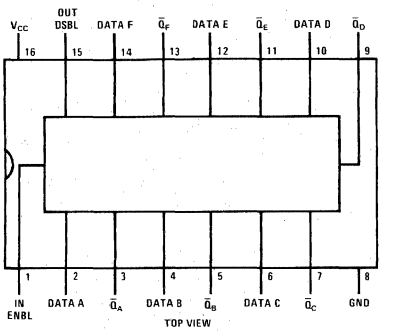
features

- TTL/DTL compatible inputs
- PNP inputs minimize loading
- Capacitance-driving outputs
- TRI-STATE outputs
- Built-in damping resistor (DS1645/DS3645)

logic and connection diagrams



Dual-In-Line Package



Order Number DS1645J, DS1675J, DS3645J, DS3675J, DS3645N or DS3675N
See Package 10 or 15

truth table

INPUT ENABLE	OUTPUT DISABLE	DATA	OUTPUT	OPERATION
1	0	1	0	Data Feed-Through
1	0	0	1	Data Feed-Through
0	0	X	Q	Latched to Data Present when Enable Went Low
X	1	X	Hi-z	High Impedance Output

X = Don't care.

*Specifications may change.

10

NATIONAL

DS1646/DS3646, DS1676/DS3676 6-bit TRI-STATE® MOS refresh counter/driver

general description

The DS1646/DS3646 and DS1676/DS3676 are 6-bit refresh counters with outputs designed to drive large capacitive loads up to 500 pF associated with MOS memory systems. PNP input transistors are employed to reduce input currents. The circuit has Schottky-clamped transistor logic for minimum propagation delay, and TRI-STATE® outputs allow it to be used on common data buses.

The DS1646/DS3646 has a 15 ohm resistor in series with the outputs to dampen transients caused by the fast switching output circuit. The DS1676/DS3676 has a direct, low impedance output, for use with or without an external resistor.

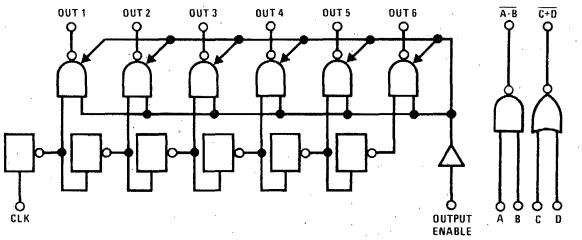
The counter uses as its input the RAM clock signal, and with each clock input, it advances the count by one, thus generating a new refresh address.

Extra pins in the package are used for a two input NAND gate and a two input NOR gate, both of which have capacitive drive outputs.

features

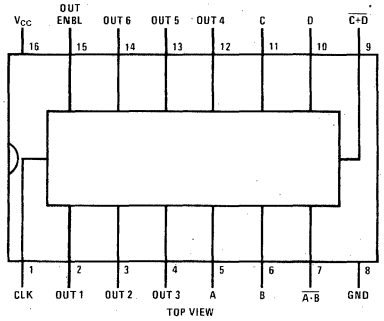
- Circuit counts when clock goes high
- TTL/DTL compatible inputs
- PNP inputs minimize loading
- Capacitance-driver outputs
- TRI-STATE outputs
- Extra gates on unused pins
- Built-in damping resistor (DS1646/DS3646)

logic diagram



connection diagram

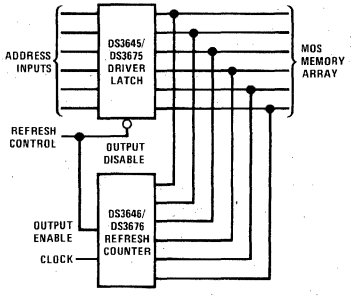
Dual-In-Line Package



Order Number DS1646J, DS1676J, DS3646J, DS3676J, DS3646N, or DS3676N
See Package 10 or 15

typical application

The DS1646/DS3646 and DS1676/DS3676 have TRI-STATE outputs which can be tied to the outputs of another TRI-STATE driver. The refresh counter can control the address lines into a memory array during a short refresh cycle, and then return to the high-impedance state to allow the primary driver to control the address lines.



*Specifications may change.

NATIONAL

Interface

Advance Information*

DS1647/DS3647, DS1677/DS3677, DS16147/DS36147, DS16177/DS36177 quad TRI-STATE® MOS memory I/O registers

general description

The DS1647/DS3647 series are 4-bit I/O buffer registers intended for use in MOS memory systems. The circuits employ a fall-through latch for data storage. This method of latching captures the data in parallel with the output, thus eliminating the delays encountered in other designs. The circuits use Schottky-clamped transistor logic for minimum propagation delay and employ PNP input transistors so that input currents are low, allowing large fan-out to these circuits needed in a memory system.

Two pins per bit are provided, and data transfer is bi-directional so that the register can handle both input and output data. The direction of data flow is controlled through the input enables. The latch control, when taken low, will cause the register to hold the data present at that time and display it at the outputs. Data can be latched into the register independent of the output disables or EXPANSION input. Either or both of the outputs may be taken to the high-impedance state with the output disables. The EXPANSION pin disables both outputs to facilitate multiplexing with other I/O registers on the same data lines.

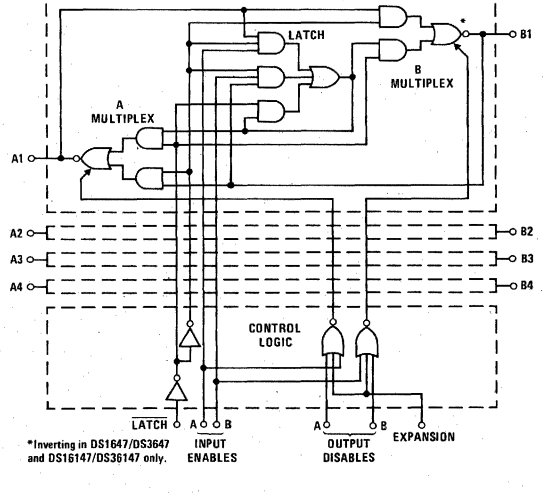
The "B" port outputs in the DS16147/DS36147 and DS16177/DS36177 are open collectors, and in the DS1647/DS3647 and DS1677/DS3677 they are TRI-STATE. The "B" port outputs are also designed for use in bus organized data transmission systems and can sink 80 mA and source −5.2 mA. The "A" port outputs in all four types are TRI-STATE.

Data going from port "A" to port "B" is inverted in the DS1647/DS3647 and DS16147/DS36147 and is not inverted in the DS1677/DS3677 and DS16177/DS36177. Data going from port "B" to port "A" is inverted in all four types.

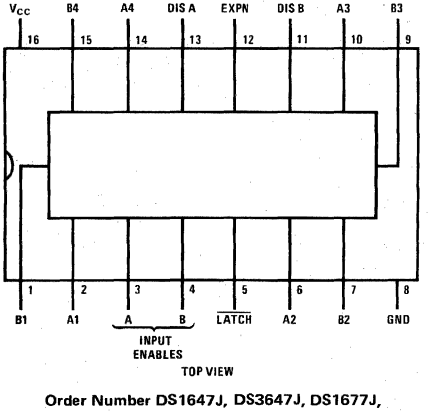
features

- PNP inputs minimize loading
- Fall-through latch design
- Propagation delay of only 15 ns
- TRI-STATE outputs
- EXPANSION control
- Bi-directional data flow
- TTL/DTL compatible
- Transmission line driver output

logic and connection diagrams



Dual-In-Line Package



Order Number DS1647J, DS3647J, DS1677J, DS3677J, DS16147J, DS36147J, DS16177J, DS36177J DS3647N, DS3677N, DS36147N or DS36177N

See Package 10 or 15

*Specifications may change.

10

NATIONAL

Interface
Advance Information*

DS1648/DS3648, DS1678/DS3678 TRI-STATE® MOS multiplexer/drivers

general description

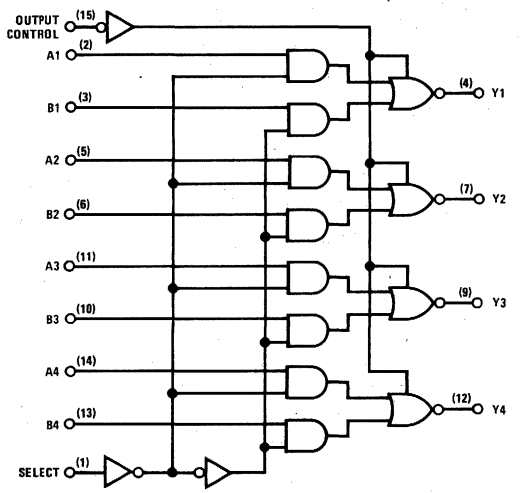
The DS1648/DS3648 and DS1678/DS3678 are quad 2-input multiplexers with TRI-STATE outputs designed to drive the large capacitive loads (up to 500 pF) associated with MOS memory systems. A PNP input structure is employed to minimize input currents so that driver loading in large memory systems is reduced. The circuit employs Schottky-clamped transistors for high speed and TRI-STATE outputs for bus operation.

The DS1648/DS3648 has a 15 ohm resistor in series with the outputs which dampens the transients caused by the fast-switching output circuit, while the DS1678/DS3678 has a direct, low impedance output for use with or without an external resistor.

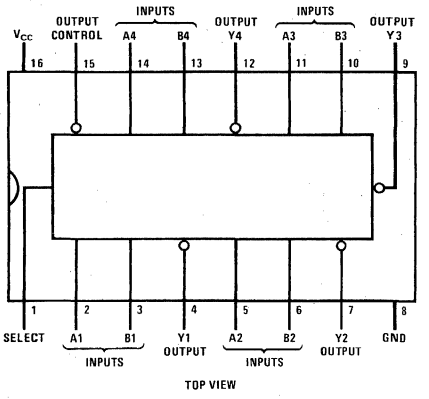
features

- TRI-STATE outputs interface directly with system bus
- Schottky-clamped for better ac performance
- PNP inputs to minimize input loading
- DTL and TTL compatible
- High-speed capacitive load drivers
- Built-in damping resistor (DS1648/DS3648 only)

logic and connection diagrams



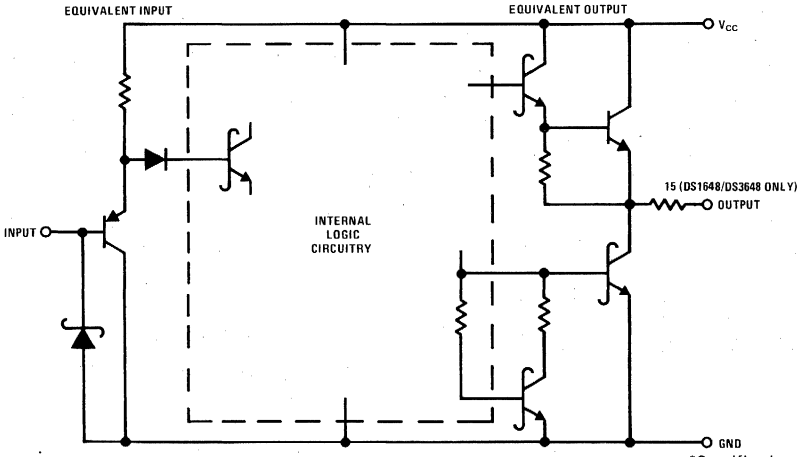
Dual-In-Line Package



TOP VIEW

Order Number DS1648J, DS1678J, DS3648J, DS3678J, DS3648N or DS3678N
See Package 10 or 15

schematic diagram



*Specifications may change.

NATIONAL

Interface
Advance Information*

DS1649/DS3649, DS1679/DS3679 hex TRI-STATE® MOS drivers

general description

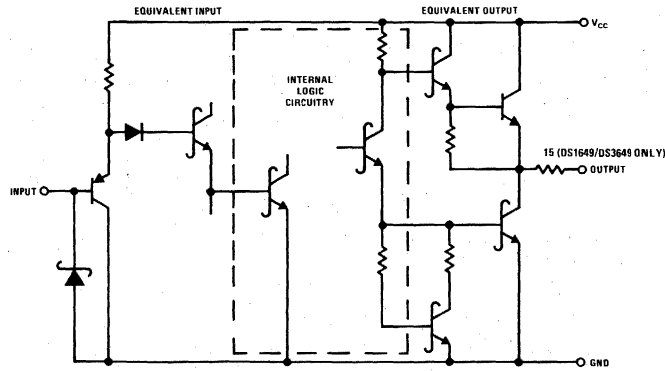
The DS1649/DS3649 and DS1679/DS3679 are Hex TRI-STATE MOS drivers with outputs designed to drive large capacitive loads up to 500 pF associated with MOS memory systems. PNP input transistors are employed to reduce input currents allowing the large fan-out to these drivers needed in memory systems. The circuit has Schottky-clamped transistor logic for minimum propagation delay, and TRI-STATE outputs for bus operation.

The DS1649/DS3649 has a 15 ohm resistor in series with the outputs to dampen transients caused by the fast-switching output. The DS1679/DS3679 has a direct low impedance output for use with or without an external resistor.

features

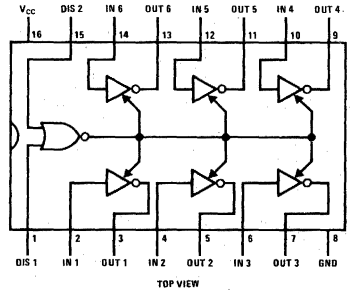
- High speed capabilities
  - Typ 7 ns driving 50 pF
  - Typ 25 ns driving 500 pF
- TRI-STATE outputs for data bussing
- Built-in 15 ohm damping resistor (DS1649/DS3649)
- Same pin-out as DS8096 and DS74366

schematic diagram



connection diagram

Dual-In-Line Package



TOP VIEW

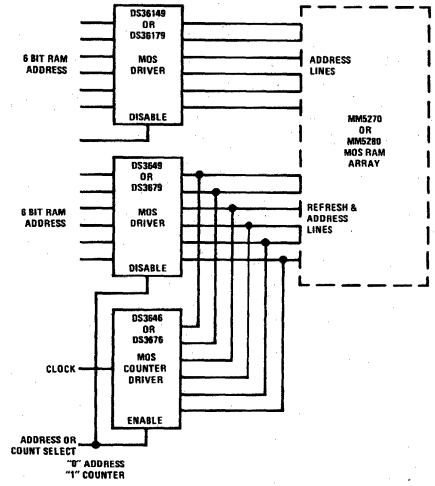
Order Number DS1649J, DS1679J, DS3649J, DS3679J, DS3649N or DS3679N
See Package 10 or 15

truth table

DISABLE INPUT		INPUT	OUTPUT
DIS 1	DIS 2		
0	0	0	1
0	0	1	0
0	1	X	Hi-Z
1	0	X	Hi-Z
1	1	X	Hi-Z

X = Don't care
Hi-Z = TRI-STATE mode

typical application



*Specifications may change.

NATIONAL

Interface
Advance Information*

DS3651, DS3653 quad high speed MOS sense amplifiers

general description

The DS3651 and DS3653 are TTL compatible high speed circuits intended for sensing in a broad range of MOS memory system applications. Switching speeds have been enhanced over conventional sense amplifiers by application of Schottky technology, and TRI-STATE® strobing is incorporated offering a high impedance output state for bused organization.

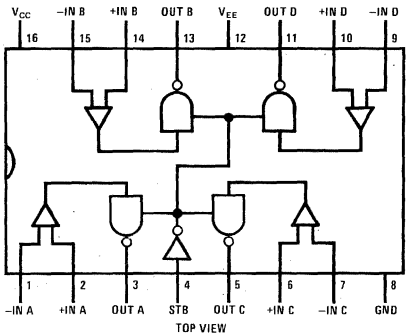
The DS3651 has active pull-up outputs, and the DS3653 offers open collector outputs providing implied "AND" operations.

features

- High speed — 15 ns (typ)
- TTL compatible
- Input sensitivity — ±7 mV
- TRI-STATE outputs for high speed buses
- Standard supply voltages — ±5V
- Pin and function compatible with MC3430 and MC3432

connection diagram

Dual-In-Line Package



Order Number DS3651J, DS3653J, DS3651N or DS3653N
See Package 10 or 15

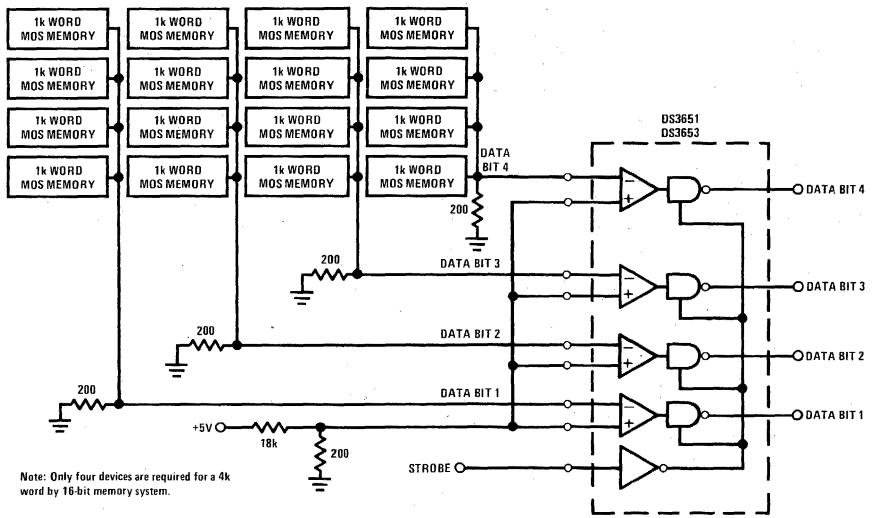
truth table

INPUT	STROBE	OUTPUT	
		DS3651	DS3653
$V_{ID} \geq +7.0$ mV $T_A = 0°C$ to $+70°C$	L	H	Open
	H	Open	Open
-7.0 mV $\leq V_{ID} \leq +7.0$ mV $T_A = 0°C$ to $+70°C$	L	X	X
	H	Open	Open
$V_{ID} \leq -7.0$ mV $T_A = 0°C$ to $+70°C$	L	L	L
	H	Open	Open

L = Low logic state
H = High logic state
Open = TRI-STATE
X = Indeterminate State

typical applications

A Typical MOS Memory Sensing Application for a 4k word by 4-bit memory arrangement employing 1103 type memory devices



Note: Only four devices are required for a 4k word by 16-bit memory system.

*Specifications may change

NATIONAL

Interface
Advance Information*

DS1671/DS3671 bootstrapped two phase MOS clock driver

general description

The DS1671/DS3671 is a high speed dual MOS clock driver and interface circuit. Unique circuit design provides both very high speed operation and the ability to drive large capacitive loads. The device accepts standard TTL/DTL outputs and converts them to MOS logic levels. It may be driven from standard 54/74 and 54S/74S series gates and flip-flops or from drivers such as the DS8830 or DM7440. The circuit can be used in both P-channel and N-channel MOS memory system drive applications.

The DS1671/DS3671 is intended to fulfill a wide variety of MOS interface requirements. As a MOS clock driver for long silicon gate shift registers, a single device can drive over 10k bits at 5 MHz. Six devices provide input address and precharge drive for an 8k by 16-bit 1103 RAM memory system.

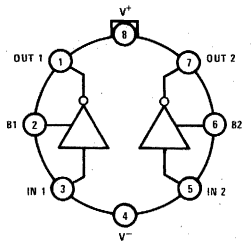
Each driver uses output bootstrapping to provide a higher voltage to the output stage, thus eliminating the need for an additional V_{DD} supply. The bootstrapping function is accomplished by connecting a small value capacitor (typically 200 pF) from each output to each drivers bootstrap node.

features

- Fast rise and fall times—20 ns with 1000 pF load
- High output swing—20V
- High output current drive—±1.5A
- TTL/DTL compatible inputs
- High rep rate—5 to 10 MHz depending on power dissipation
- Low power consumption in MOS "0" state—2 mW
- Swings to 0.4V of GND for RAM address drive

connection diagrams

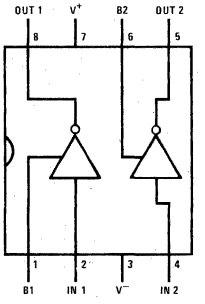
Metal Can Package



TOP VIEW

Order Number DS1671H
or DS3671H
See Package 23

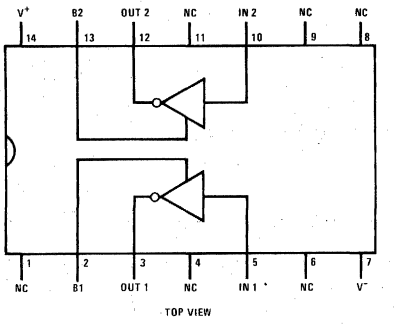
Dual-In-Line Package



TOP VIEW

Order Number DS3671N
See Package 12

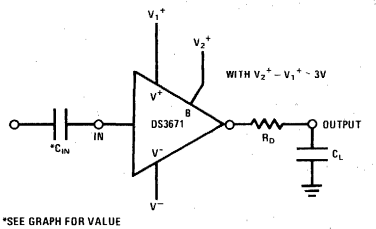
Dual-In-Line Package



TOP VIEW

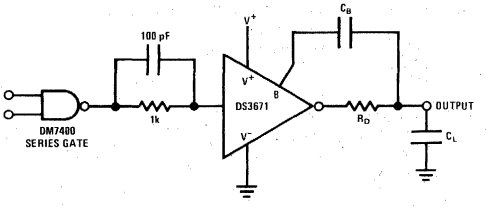
Order Number DS1671J or DS3671J
See Package 9

typical applications



*SEE GRAPH FOR VALUE

DS3671 Operating with Extra Supply
to Inhance Output Voltage Level



Bootstrap Clock Driver Driven from a TTL Gate

*Specifications may change.

NATIONAL

Interface

Advance Information*

DS16149/DS36149, DS16179/DS36179 hex MOS drivers

general description

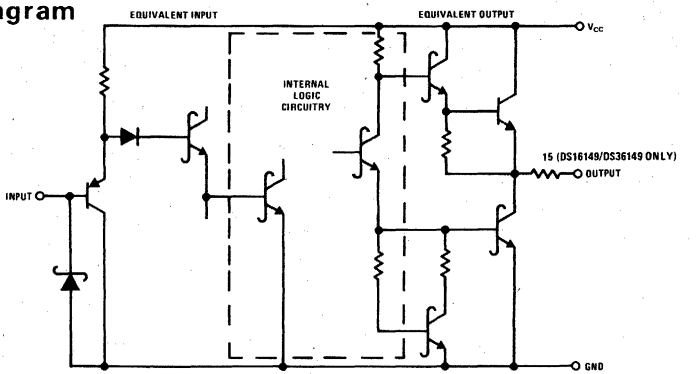
The DS16149/DS36149 and DS16179/DS36179 are Hex MOS drivers with outputs designed to drive large capacitive loads up to 500 pF associated with MOS memory systems. PNP input transistors are employed to reduce input currents allowing the large fan-out to these drivers needed in memory systems. The circuit has Schottky-clamped transistor logic for minimum propagation delay, and a disable control that places the outputs in the logical "1" state (see truth table). This is especially useful in MOS RAM applications where a set of address lines has to be in the logical "1" state during refresh.

The DS16149/DS36149 has a 15 ohm resistor in series with the outputs to dampen transients caused by the fast-switching output. The DS16179/DS36179 has a direct low impedance output for use with or without an external resistor.

features

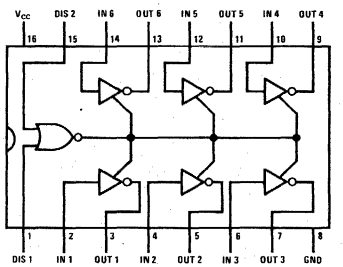
- High speed capabilities
  - Typ 7 ns driving 50 pF
  - Typ 25 ns driving 500 pF
- Built-in 15 ohm damping resistor (DS16149/DS36149)
- Same pin-out as DS8096 and DS74366

schematic diagram



connection diagram

Dual-In-Line Package



TOP VIEW

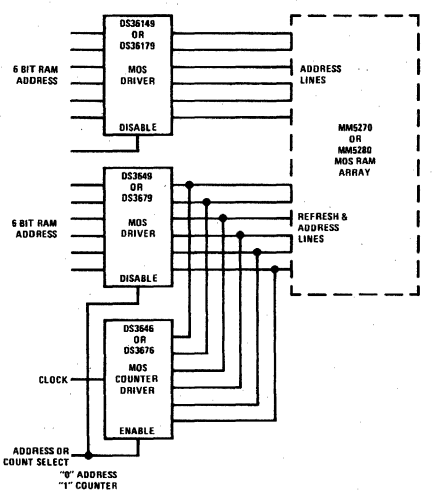
Order Number DS16149J, DS16179J, DS36149J, DS36179J, DS36149N or DS36179N
See Package 10 or 15

truth table

DISABLE INPUT		INPUT	OUTPUT
DIS 1	DIS 2		
0	0	0	1
0	0	1	0
0	1	X	1
1	0	X	1
1	1	X	1

X = Don't care

typical application



*Specifications may change.

NATIONAL

Interface
Advance Information*

DS55109/DS75109, DS55110/DS75110 dual line drivers

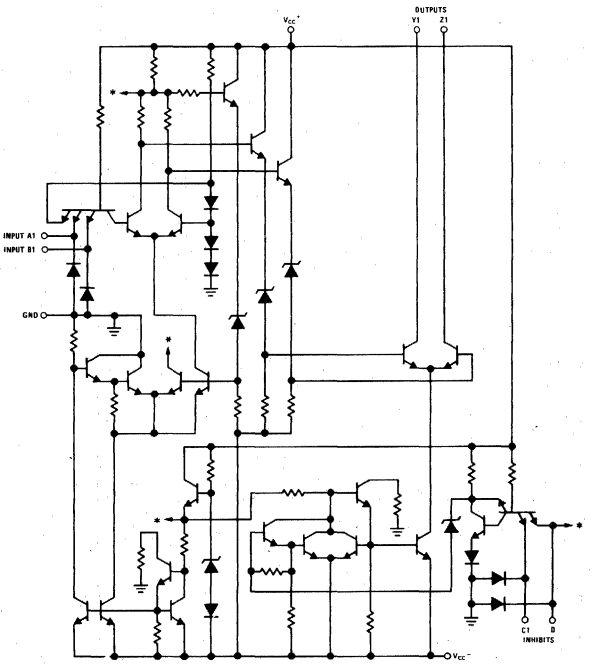
general description

These products are TTL compatible high speed differential line drivers intended for use in terminated twisted-pair party-line data transmission systems. They may also be used for level shifting since output common-mode range is −3V to +10V. An internal current sink is switched to either output dependent on input logic conditions. The current sink may be turned off by appropriate inhibit input conditions.

features

- Tightly controlled output currents over temperature, V_{CC}, and common-mode variations
- High speed — 15 ns max
- Wide output common-mode range
- High output impedance
- Inhibits for party-line applications
- Current sink outputs — 6 or 12 mA
- Dual circuits
- Standard supply voltages — ±5V
- Input clamp diodes
- 14 pin cavity or molded DIP

schematic diagram

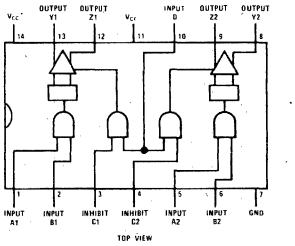


Note 1: 1/2 of the dual circuit shown.

Note 2: *Indicates connections common to second half of circuit.

connection diagram

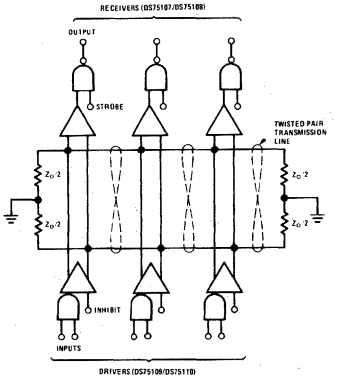
Dual-In-Line Package



Order Number DS55109J, DS55110J, DS75109J or DS75110J
See Package 9
Order Number DS75109N or DS75110N
See Package 14

typical application

Party-Line Data Transmission System



*Specifications may change

NATIONAL

Interface

DS55121/DS75121 dual line drivers

general description

The DS55121/DS75121 are monolithic dual line drivers designed to drive long lengths of coaxial cable, strip line, or twisted pair transmission lines having impedances from 50 to 500 ohms. Both are compatible with standard TTL logic and supply voltage levels.

The DS55121/DS75121 will drive terminated low impedance lines due to the low-impedance emitter-follower outputs. In addition the outputs are uncommitted allowing two or more drivers to drive the same line.

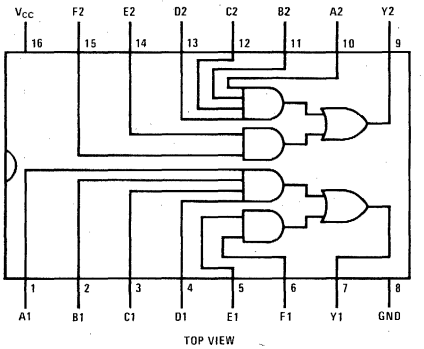
Output short-circuit protection is incorporated to turn off the output when the output voltage drops below approximately 1.5V.

features

- Designed for digital data transmission over 50 to 500 ohms coaxial cable, strip line, or twisted pair transmission lines
- TTL compatible
- Open emitter-follower output structure for party-line operation
- Short-circuit protection
- AND-OR logic configuration
- High speed (max propagation delay time 20 ns)
- Plug-in replacement for the SN55121/SN75121 and the 8T13

connection diagram

Dual-In-Line Package

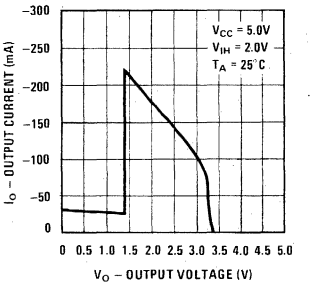


TOP VIEW

Order Number DS55121J, DS75121J, DS75121N or DS55121W
See Package 10, 15 or 28

typical performance characteristics

Output Current vs Output Voltage

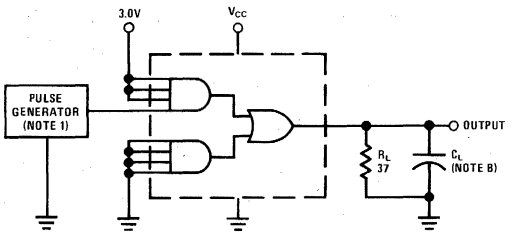


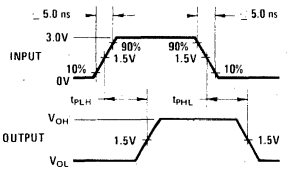
truth table

INPUTS						OUTPUT
A	B	C	D	E	F	Y
H	H	H	H	X	X	H
X	X	X	X	H	H	H
All Other Input Combinations						L

H = high level, L = low level, X = irrelevant

ac test circuit and switching time waveforms





Note 1: The pulse generators have the following characteristics: $Z_{OUT} \approx 50\Omega$, $t_W = 200$ ns, duty cycle = 50%, $t_r = t_f = 5.0$ ns.
Note 2: C_L includes probe and jig capacitance.

Interface

DS55122/DS75122 triple line receivers

general description

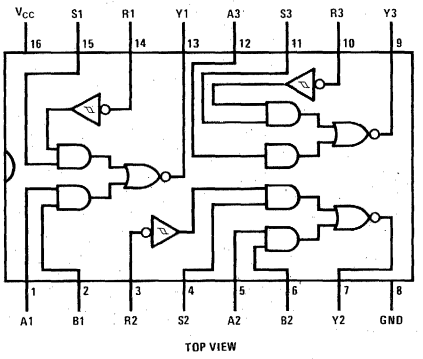
The DS55122/DS75122 are triple line receivers designed for digital data transmission with line impedances from 50Ω to 500Ω. Each receiver has one input with built-in hysteresis which provides a large noise margin. The other inputs on each receiver are in a standard TTL configuration. The DS55122/DS75122 are compatible with standard TTL logic and supply voltage levels.

features

- Built-in input threshold hysteresis
- High speed ... typical propagation delay time 20 ns
- Independent channel strobes
- Input gating increases application flexibility
- Single 5.0V supply operation
- Fanout to 10 series 54/74 standard loads
- Plug-in replacement for the SN55122/SN75122 and the 8T14

connection diagram

Dual-In-Line Package



TOP VIEW

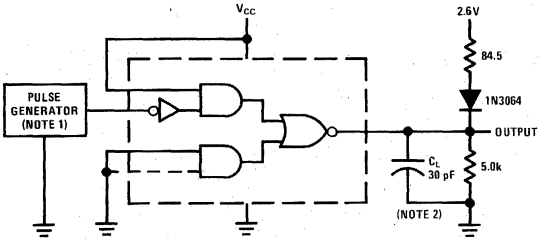
Order Number DS55122J, DS75122J, DS75122N or DS55122W
See Package 10, 15 or 28

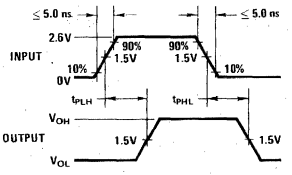
truth table

INPUTS A	INPUTS B†	INPUTS R	INPUTS S	OUTPUT Y
H	H	X	X	L
X	X	L	H	L
L	X	H	X	H
L	X	X	L	H
X	L	H	X	H
X	L	X	L	H

H = high level, L = low level, X = irrelevant
†B input and last two lines of the truth table are applicable to receivers 1 and 2 only.

ac test circuit and switching time waveforms





Note 1: The pulse generator has the following characteristics: $Z_{OUT} \approx 50\Omega$, t_W = 200 ns, duty cycle = 50%, $t_r = t_f$ = 5.0 ns.
Note 2: C_L includes probe and jig capacitance.

NATIONAL

Interface

DS75123 dual line driver

general description

The DS75123 is a monolithic dual line driver designed specifically to meet the I/O interface specifications for IBM System 360. It is compatible with standard TTL logic and supply voltage levels.

The low-impedance emitter-follower outputs of the DS75123 enable driving terminated low impedance lines. In addition the outputs are uncommited allowing two or more drivers to drive the same line.

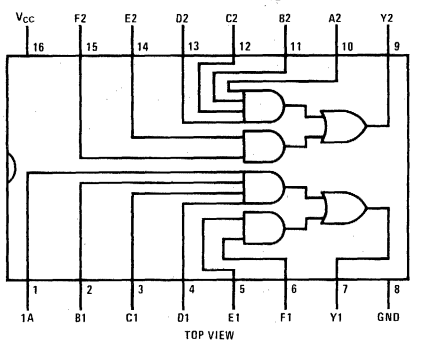
Output short-circuit protection is incorporated to turn off the output when the output voltage drops below approximately 1.5V.

features

- Meet IBM System 360 I/O interface specifications for digital data transmission over 50Ω to 500Ω coaxial cable, strip line, or terminated pair transmission lines
- TTL compatible with single 5.0V supply
- 3.11V output at I_{OH} = −59.3 mA
- Open emitter-follower output structure for party-line operation
- Short circuit protection
- AND-OR logic configuration
- Plug-in replacement for the SN75123 and the 8T23

connection diagram

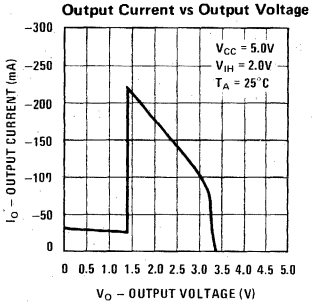
Dual-In-Line Package



Order Number DS75123J
See Package 10
Order Number DS75123N
See Package 15

typical performance characteristics

Output Current vs Output Voltage

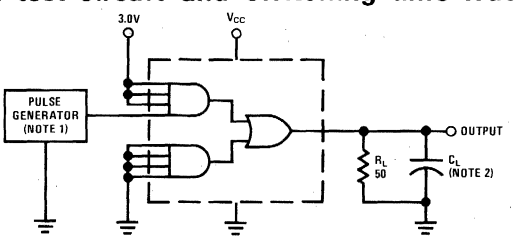


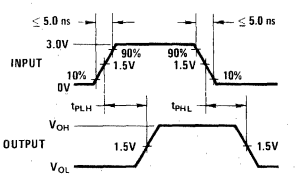
truth table

INPUTS						OUTPUT
A	B	C	D	E	F	Y
H	H	H	H	X	X	H
X	X	X	X	H	H	H
All Other Input Combinations						L

H = high level, L = low level, X = irrelevant

ac test circuit and switching time waveforms





Note 1: THE PULSE GENERATORS HAVE THE FOLLOWING CHARACTERISTICS: $Z_{OUT} \approx 50\Omega$, t_W = 200 ns, DUTY CYCLE = 50%.

Note 2: C_L INCLUDES PROBE AND JIG CAPACITANCE.

NATIONAL

DS75124 triple line receivers

general description

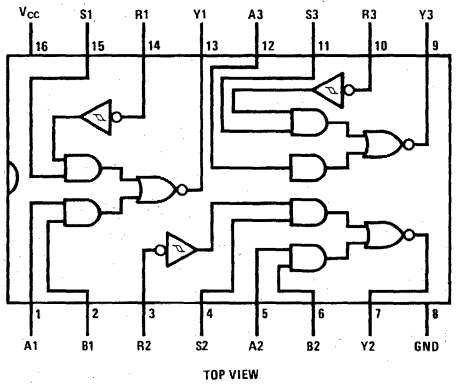
The DS75124 is designed to meet the input/output interface specifications for IBM System 360. It has built-in hysteresis on one input on each of the three receivers to provide large noise margin. The other inputs on each receiver are in a standard TTL configuration. The DS75124 is compatible with standard TTL logic and supply voltage levels.

features

- Built-in input threshold hysteresis
- High speed . . typ propagation delay time 20 ns
- Independent channel strobes
- Input gating increases application flexibility
- Single 5.0V supply operation
- Plug-in replacement for the SN75124 and the 8T24

connection diagram and truth table

Dual-In-Line Package



TOP VIEW

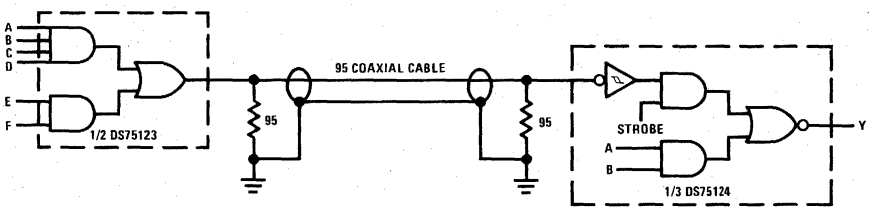
Order Number DS75124J
See Package 10

Order Number DS75124N
See Package 15

INPUTS				OUTPUT
A	B†	R	S	Y
H	H	X	X	L
X	X	L	H	L
L	X	H	X	H
L	X	X	L	H
X	L	H	X	H
X	L	X	L	H

H = high level, L = low level, X = irrelevant
†B input and last two lines of the truth table are applicable to receivers 1 and 2 only.

typical application



NATIONAL

Interface

DS75150 dual line driver

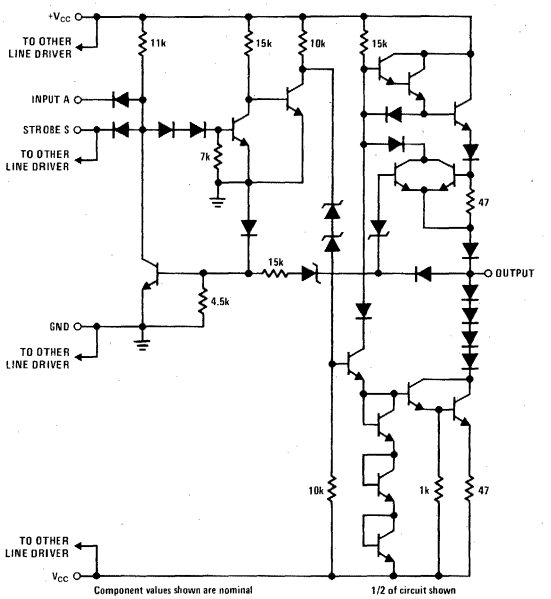
general description

The DS75150 is a dual monolithic line driver designed to satisfy the requirements of the standard interface between data terminal equipment and data communication equipment as defined by EIA Standard RS-232-C. A rate of 20,000 bits per second can be transmitted with a full 2500 pF load. Other applications are in data-transmission systems using relatively short single lines, in level translators, and for driving MOS devices. The logic input is compatible with most TTL and DTL families. Operation is from −12V and +12V power supplies.

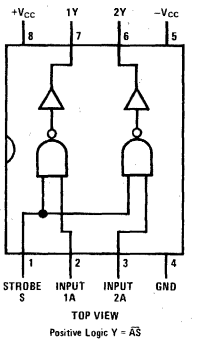
features

- Withstands sustained output short-circuit to any low impedance voltage between −25V and +25V
- 2μs max transition time through the −3V to +3V transition region under full 2500 pF load
- Inputs compatible with most TTL and DTL families
- Common strobe input
- Inverting output
- Slew rate can be controlled with an external capacitor at the output
- Standard supply voltages ±12V

schematic and connection diagrams

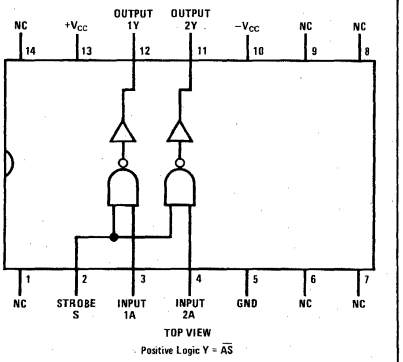


Dual-In-Line Package



Order Number DS75150N
See Package 12

Dual-In-Line Package



Order Number DS75150J
See Package 9

DS75154 quadruple line receiver

general description

The DS75154 is a quad monolithic line receiver designed to satisfy the requirements of the standard interface between data terminal equipment and data communication equipment as defined by EIA Standard RS-232C. Other applications are in relatively short, single-line, point-to-point data transmission systems and for level translators. Operation is normally from a single 5V supply; however, a built-in option allows operation from a 12V supply without the use of additional components. The output is compatible with most TTL and DTL circuits when either supply voltage is used.

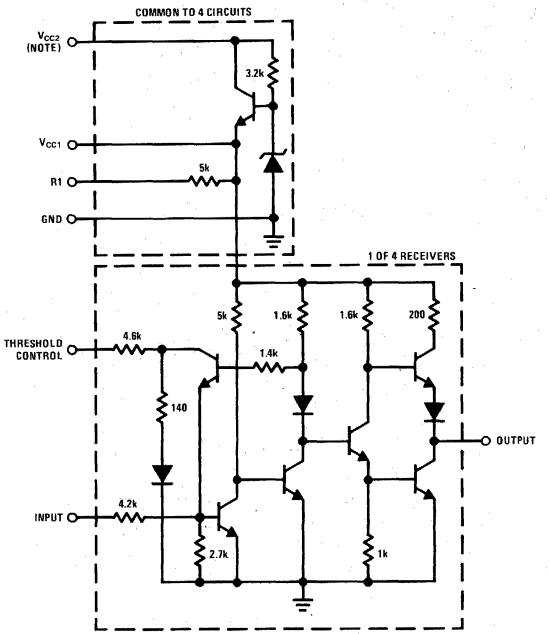
In normal operation, the threshold-control terminals are connected to the V_{CC1} terminal, pin 15, even if power is being supplied via the alternate V_{CC2} terminal, pin 16. This provides a wide hysteresis loop which is the difference between the positive-going and negative-going threshold voltages. In this mode, if the input voltage goes to zero, the output voltage will remain at the low or high level as determined by the previous input.

For fail-safe operation, the threshold-control terminals are open. This reduces the hysteresis loop by causing the negative-going threshold voltage to be above zero. The positive-going threshold voltage remains above zero as it is unaffected by the disposition of the threshold terminals. In the fail-safe mode, if the input voltage goes to zero or an open-circuit condition, the output will go to the high level regardless of the previous input condition.

features

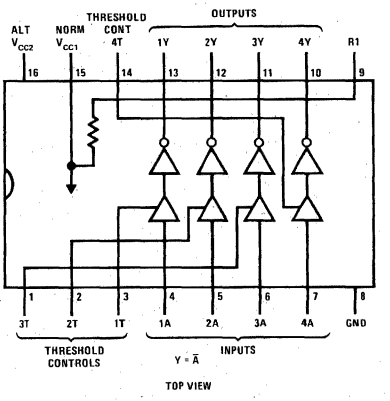
- Input resistance, 3 kΩ to 7 kΩ over full RS-232C voltage range
- Input threshold adjustable to meet "fail-safe" requirements without using external components
- Inverting output compatible with DTL or TTL
- Built-in hysteresis for increased noise immunity
- Output with active pull-up for symmetrical switching speeds
- Standard supply voltage—5V or 12V

schematic and connection diagrams



Note: When using V_{CC1} (pin 15), V_{CC2} (pin 16) may be left open or shorted to V_{CC1}. When using V_{CC2}, V_{CC1} must be left open or connected to the threshold control pins.

Dual-In-Line Package



Order Number DS75154J or DS75154N
See Package 10 or 15

NATIONAL

Interface

DS75324 memory driver with decode inputs

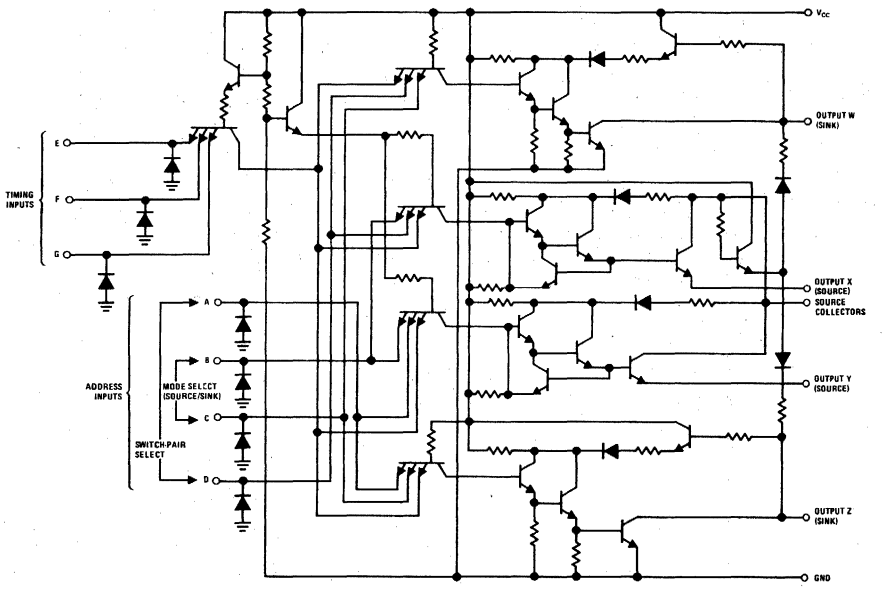
general description

The DS75324 is a monolithic memory driver which features two 400 mA (source/sink) switch pairs along with decoding capability from four address lines. Inputs B and C function as mode selection lines (source or sink) while lines A and D are used for switch-pair selection (output pair Y/Z or W/X).

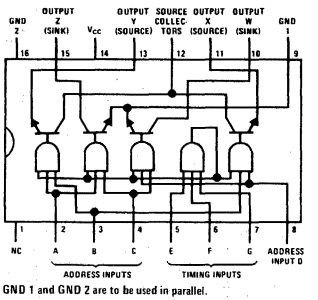
features

- High voltage outputs
- Dual sink/source outputs
- Internal decoding and timing circuitry
- 400 mA output capability
- DTL/TTL compatible
- Input clamping diodes

schematic and connection diagrams



Dual-In-Line Package

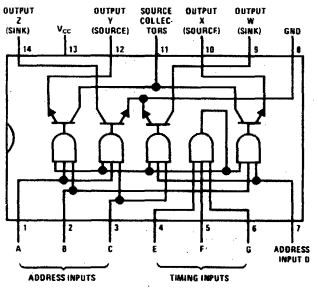


GND 1 and GND 2 are to be used in parallel.

TOP VIEW

Order Number DS75324J
See Package 10

Dual-In-Line Package



TOP VIEW

Order Number DS75324N
See Package 14

NATIONAL

DS55325/DS75325 memory drivers general description

The DS55325 and DS75325 are monolithic memory drivers which feature high current outputs as well as internal decoding of logic inputs. These circuits are designed for use with magnetic memories.

The circuit contains two 600 mA sink-switch pairs and two 600 mA source-switch pairs. Inputs A and B determine source selection while the source strobe (S_1) allows the selected source turn on. In the same manner, inputs C and D determine sink selection while the sink strobe (S_2) allows the selected sink turn on.

Sink-output collectors feature an internal pull-up resistor in parallel with a clamping diode connected to V_{CC2}. This protects the outputs from voltage surges associated with switching inductive loads.

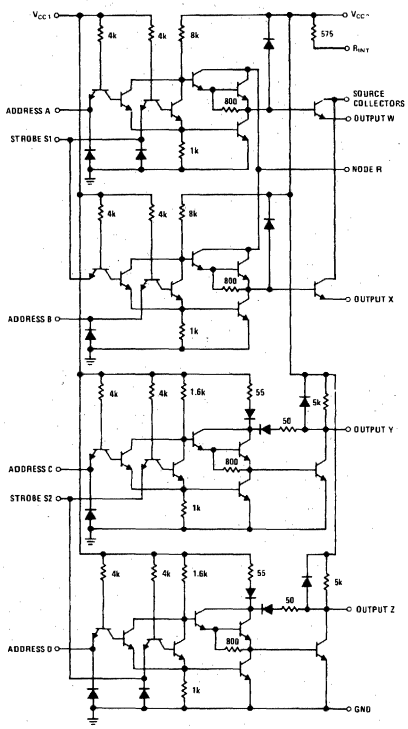
The source stage features Node R which allows extreme flexibility in source current selection by controlling the amount of base drive to each source transistor. This method of setting the base drive brings the power associated with the resistor outside the package thereby allowing the circuit to operate at higher source currents for a given junction temperature. If this method of source current setting is not desired, then Nodes R and R_{INT} can be shorted externally activating an internal resistor connected from V_{CC2} to Node R. This provides adequate base drive for source currents up to 375 mA with V_{CC2} = 15V or 600 mA with V_{CC2} = 24V.

The DS55325 operates over the fully military temperature range of −55°C to +125°C, while the DS5325 operates from 0°C to +70°C.

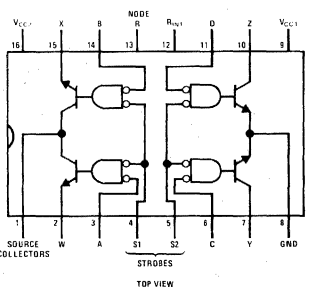
features

- 600 mA output capability
- 24V output capability
- Dual sink and dual source outputs
- Fast switching times
- Source base drive externally adjustable
- Input clamping diodes
- DTL/TTL compatible

schematic and connection diagrams



Dual-In-Line Package



Order Number DS55325J, DS75325J, DS75325N or DS55325W
See Package 10, 15 or 28

truth table

ADDRESS INPUTS				STROBE INPUTS		OUTPUTS			
SOURCE		SINK		SOURCE	SINK	SOURCE		SINK	
A	B	C	D	S1	S2	W	X	Y	Z
L	H	X	X	L	H	ON	OFF	OFF	OFF
H	L	X	X	L	H	OFF	ON	OFF	OFF
X	X	L	H	H	L	OFF	OFF	ON	OFF
X	X	H	L	H	L	OFF	OFF	OFF	ON
X	X	X	X	H	H	OFF	OFF	OFF	OFF
H	H	H	H	X	X	OFF	OFF	OFF	OFF

H = high level, L = low level, X = irrelevant

NOTE: Not more than one output is to be on at any one time.

NATIONAL

DS75361 dual TTL-to-MOS driver

general description

The DS75361 is a monolithic integrated dual TTL-to-MOS driver interface circuit. The device accepts standard TTL and DTL input signals and provides high-current and high-voltage output levels for driving MOS circuits. It is used to drive address, control, and timing inputs for several types of MOS RAMs including the 1103 and MM5270 and MM5280.

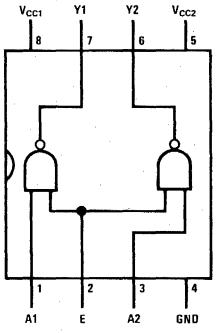
The DS75361 operates from standard TTL 5V supplies and the MOS V_{SS} supply in many applications. The device has been optimized for operation with V_{CC2} supply voltage from 16V to 20V; however, it is designed for use over a much wider range of V_{CC2}.

features

- Capable of driving high-capacitance loads
- Compatible with many popular MOS RAMs
- V_{CC2} supply voltage variable over wide range to 24V
- Diode-clamped inputs
- TTL and DTL compatible
- Operates from standard bipolar and MOS supplies
- High-speed switching
- Transient overdrive minimizes power dissipation
- Low standby power dissipation

connection diagrams

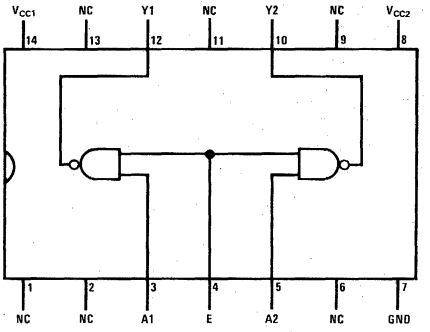
Dual-In-Line Package



TOP VIEW

Order Number DS75361N
See Package 12

Dual-In-Line Package



TOP VIEW

Order Number DS75361J
See Package 9

NATIONAL

DS75362 dual TTL-to-MOS driver

general description

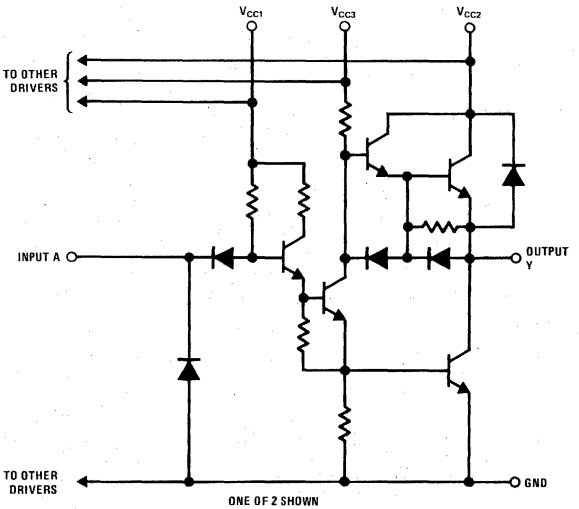
The DS75362 is a dual monolithic integrated TTL-to-MOS driver and interface circuit that accepts standard TTL and DTL input signals and provides high-current and high-voltage output levels suitable for driving MOS circuits. It is used to drive address, control, and timing inputs for several types of MOS RAMs including the 1103.

The DS75362 operates from the TTL 5V supply and the MOS V_{SS} and V_{BB} supplies in many applications. This device has been optimized for operation with V_{CC2} supply voltage from 16V to 20V, and with nominal V_{CC3} supply voltage from 3V to 4V higher than V_{CC2}. However, it is designed so as to be usable over a much wider range of V_{CC2} and V_{CC3}. In some applications the V_{CC3} power supply can be eliminated by connecting the V_{CC3} pin to the V_{CC2} pin.

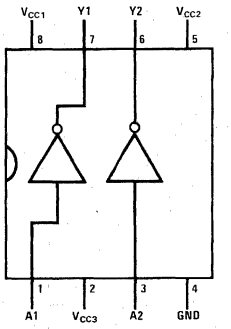
features

- Dual positive-logic NAND TTL-to-MOS driver
- Versatile interface circuit for use between TTL and high-current, high-voltage systems
- Capable of driving high-capacitance loads
- Compatible with many popular MOS RAMs
- V_{CC2} supply voltage variable over wide range to 24V maximum
- V_{CC3} supply voltage pin available
- V_{CC3} pin can be connected to V_{CC2} pin in some applications
- TTL and DTL compatible diode-clamped inputs
- Operates from standard bipolar and MOS supply voltages
- High-speed switching
- Transient overdrive minimizes power dissipation
- Low standby power dissipation

schematic and connection diagrams

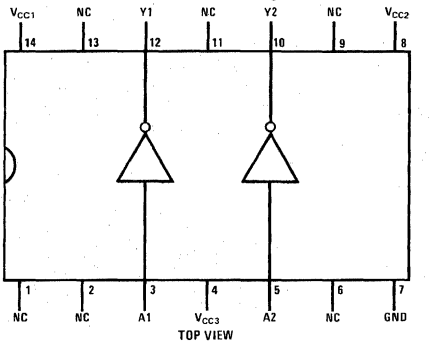


Dual-In-Line Package



Order Number DS75362N
See Package 12

Dual-In-Line Package



Order Number DS75362J
See Package 9

NATIONAL

DS75364 dual MOS clock driver

general description

The DS75364 is a dual MOS driver and interface circuit that operates with either current source or voltage source input signals. The device accepts signals from TTL levels or other logic systems and provides high current and high voltage output levels suitable for driving MOS circuits. It may be used to drive address, control and/or timing inputs for several types of MOS RAMs and MOS shift registers.

The DS75364 operates from standard MOS and bipolar supplies, and has been optimized for operation with V_{CC1} supply voltage from 12–20V positive with respect to V_{EE}, and with nominal V_{CC2} supply voltage from 3–4V more positive than V_{CC1}. However, it is designed so as to be useable over a much wider range of V_{CC1} and V_{CC2}. In some applications the V_{CC2} power supply can be eliminated by connecting the V_{CC2} pin to the V_{CC1} pin.

Inputs of the DS75364 are referenced to the V_{EE} terminal and contain a series current limiting resistor. The device will operate with either positive input current signals or input voltage signals which are positive with respect to V_{EE}. In many applications the V_{EE} terminal is connected to the MOS V_{DD} supply of −12V to −15V with the inputs to be driven from TTL levels or other positive voltage levels. The required negative level shifting may be done with an external PNP transistor current source or by use of capacitive coupling and appropriate input voltage pulse characteristics.

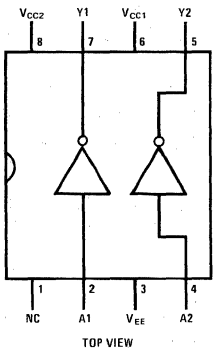
The DS75364 is characterized for operation over the 0°C to +70°C temperature range.

features

- Versatile interface circuit for use between TTL levels and level shifted high current, high voltage systems
- Inputs may be level shifted by use of a current source or capacitive coupling or driven directly by a voltage source
- Capable of driving high capacitance loads
- Compatible with many popular MOS RAMs and MOS shift registers
- V_{CC1} supply voltage variable over wide range to 22V maximum with respect to V_{EE}
- V_{CC2} pull-up supply voltage pin available
- Operates from standard bipolar and/or MOS supply voltages
- High-speed switching
- Transient overdrive minimizes power dissipation
- Low standby power dissipation

connection diagrams

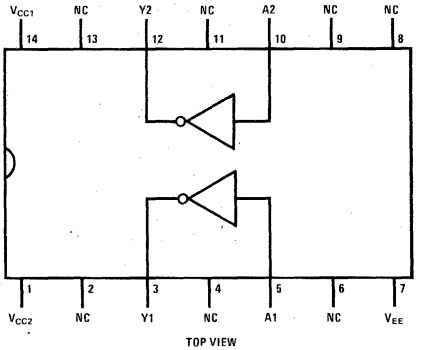
Dual-In-Line Package



TOP VIEW

Order Number DS75364N
See Package 12

Dual-In-Line Package



TOP VIEW

Order Number DS75364J
See Package 9

NATIONAL

Interface

DS75365 quad TTL-to-MOS driver

general description

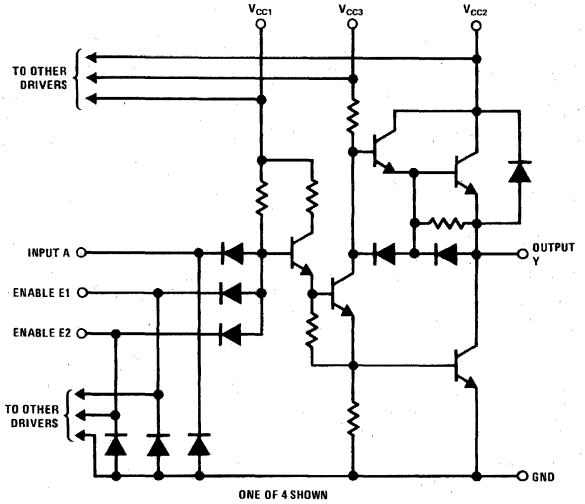
The DS75365 is a quad monolithic integrated TTL-to-MOS driver and interface circuit that accepts standard TTL and DTL input signals and provides high-current and high-voltage output levels suitable for driving MOS circuits. It is used to drive address, control, and timing inputs for several types of MOS RAMs including the 1103.

The DS75365 operates from the TTL 5V supply and the MOS V_{SS} and V_{BB} supplies in many applications. This device has been optimized for operation with V_{CC2} supply voltage from 16V to 20V, and with nominal V_{CC3} supply voltage from 3V to 4V higher than V_{CC2}. However, it is designed so as to be usable over a much wider range of V_{CC2} and V_{CC3}. In some applications the V_{CC3} power supply can be eliminated by connecting the V_{CC3} pin to the V_{CC2} pin.

features

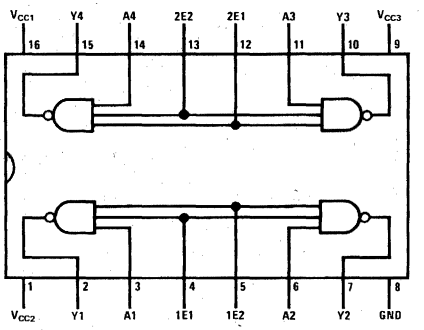
- Quad positive-logic NAND TTL-to-MOS driver
- Versatile interface circuit for use between TTL and high-current, high-voltage systems
- Capable of driving high-capacitance loads
- Compatible with many popular MOS RAMs
- Interchangeable with Intel 3207
- V_{CC2} supply voltage variable over wide range to 24V maximum
- V_{CC3} supply voltage pin available
- V_{CC3} pin can be connected to V_{CC2} pin in some applications
- TTL and DTL compatible diode-clamped inputs
- Operates from standard bipolar and MOS supply voltages
- Two common enable inputs per gate-pair
- High-speed switching
- Transient overdrive minimizes power dissipation
- Low standby power dissipation

schematic and connection diagrams



ONE OF 4 SHOWN

Dual-In-Line Package



TOP VIEW

Positive Logic: $Y = \overline{A \cdot E1 \cdot E2}$

Order Number DS75365J or DS75365N
See Package 10 or 15

DS7803/DS8803, DS8813 two phase oscillator/clock driver

general description

The DS7803 is a self contained two phase oscillator/clock driver. It requires no external components to generate one of three primary oscillator frequencies and pulse widths. Other frequencies can easily be obtained by programming input voltages. Three sets of outputs are provided: damped and undamped MOS outputs and TTL monitor outputs. The MOS outputs easily drive 500 pF loads with less than 150 ns rise and fall times. In addition the outputs have current limiting to protect against momentary shorts to the supplies.

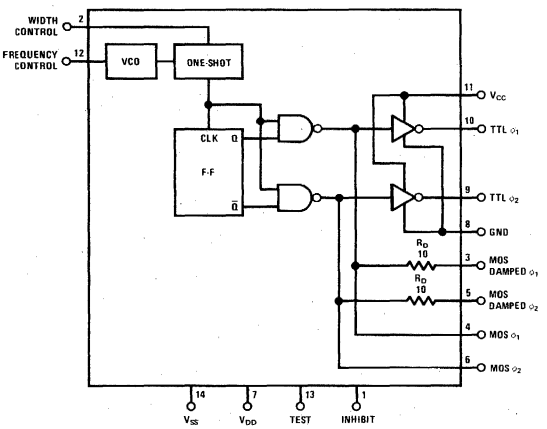
The DS7803 and DS8803 are available in a 14-lead cavity DIP. The DS8803 is also available in a 14-pin molded DIP. The DS8813 comes in an 8-pin molded DIP, providing damped MOS outputs only.

features

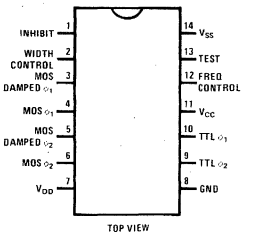
- Two phase non-overlapping outputs
- No external timing components required
- Frequency adjustable from 100 kHz to 500 kHz
- Pulse width adjustable from 260 ns to 1.4μs
- Damped and undamped MOS outputs
- TTL monitor outputs

block and connection diagrams

DS7803/DS8803

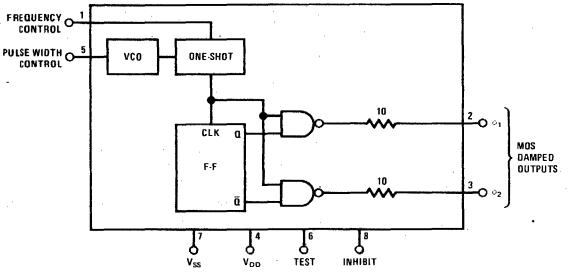


Dual-In-Line Package

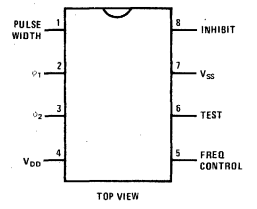


Order Number DS7803J, DS8803J or DS8803N
See Package 9 or 14

DS8813



Dual-In-Line Package



Order Number DS8813N
See Package 12

DS7807/DS8807, DS8817 two phase oscillator/clock driver

general description

The DS7807 is a self contained two phase oscillator/clock driver. It requires no external components to generate one of three primary oscillator frequencies and pulse widths. Other frequencies can easily be obtained by programming input voltages. Three sets of outputs are provided: damped and un-damped MOS outputs and TTL monitor outputs. The MOS outputs easily drive 500 pF loads with less than 75 ns rise and fall times. In addition the outputs have current limiting to protect against momentary shorts to the supplies.

The DS7807 and DS8807 are available in a 14-lead cavity DIP. The DS8807 is also available in a 14-pin molded DIP.

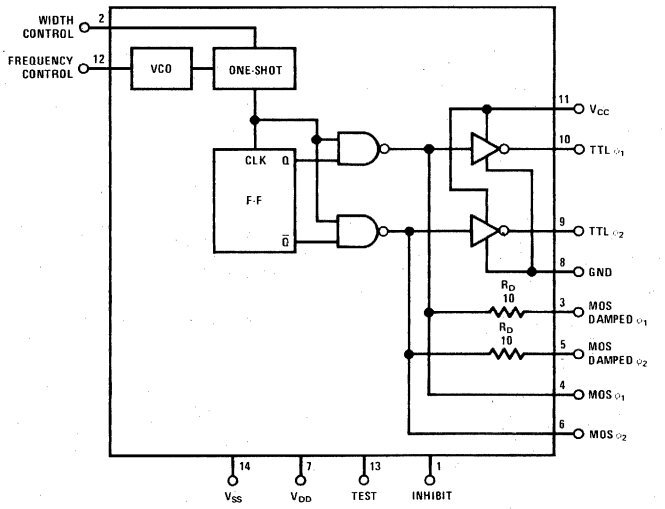
The DS8817 comes in an 8-pin molded DIP, providing damped MOS outputs only.

features

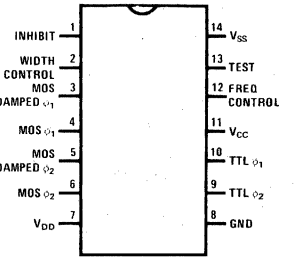
- Two phase non-overlapping outputs
- No external timing components required
- Frequency adjustable from 400 kHz to 2 MHz
- Pulse width adjustable from 130 ns to 700 ns
- Damped and un-damped MOS outputs
- TTL monitor outputs

block and connection diagrams

DS7807/DS8807



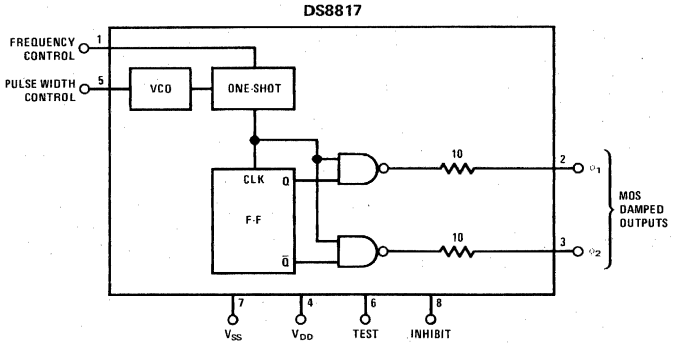
Dual-In-Line Package



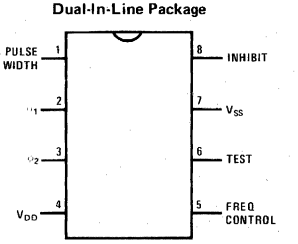
TOP VIEW

Order Number DS7807J, DS8807J or DS8807N
See Package 9 or 14

DS8817



Dual-In-Line Package



TOP VIEW

Order Number DS8817N
See Package 12

THE SYSTEMS APPROACH TO CHARACTER GENERATORS

A huge new market for man/machine interfaces is being created by the increasing availability of low cost data processing through computer time sharing, LSI calculators, minicomputers and digital business and control systems. In turn, the pressure is on to design CRT terminals, displays and teleprinters that are at least as compact and inexpensive as the new data processors.

MOS integrated circuit producers are in the thick of this competition. They have begun making read only memories and shift registers with enough storage capacity to put an appreciable dent in terminal and printer costs. Entire alphanumeric character fonts and CRT refresh channels now can be fabricated as single-chip arrays. Low threshold MOS processes and designs have been refined to make the storage arrays more compatible with bipolar logic and standard power supplies.

These developments have won MOS a place on the alphanumeric side of the readout family tree in Figure 1 (and some inroads are being made on the other side—see Appendix in this App. Note. In fact, MOS has pushed beyond the state of the art. MOS/TTL assemblies can generate characters faster than they can be handled by moderately priced CRT video circuitry or printer mechanisms. However, the increased storage capacity and speed also make higher performance systems feasible. For example, designers are considering larger fonts that make characters more legible. Large fonts have generally been economically impractical in the past because even a small increase in font size can double the memory size needed.

MOS ROMS AND REGISTERS

Large capacity, high speed, and bipolar compatibility strike directly at the problems involved in lowering data terminal costs. To generate and update readouts with many characters and symbols takes thousands of bits of storage and fast manipulation of data and control signals. If this capability is supplied in a central processor, it must be paid for in the form of central system overhead and communications costs. Using pre-LSI memory techniques in the terminals, however, can easily double the cost of each console.[1]

Storage capacities per MOS chip have increased at least tenfold in the past few years, with comparable reductions in assembly costs. By the close of 1969, MOS/TTL character generators cost about half as much as those built with bipolar devices. The newest ROMs (read only memories) for character generation represent the integration of some 3,000 diodes and 50 packages of IC gates. One terminal manufacturer who made the changeover late in 1969 replaced six large printed circuit boards with one plug-in card.

The largest MOS ROMs mass produced last year stored 1024 and 2048 bits—general purpose sizes used for table lookup, microprogramming and random-logic functions as well as character generation. A typical generator contained three 1024-bit ROMs, such as National Semiconductor's SK0001 and SK0002 kits (see Table 1 and Figures 2 and 3). Generating the standard 64 ASCII-selected characters in a 5 x 7 font requires a storage capac-

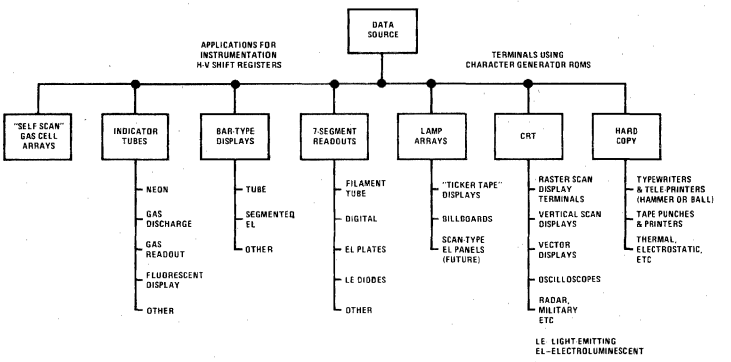


Figure 1. Display Family Tree

ity of at least 5 x 7 x 64. Each logical "1" bit stored in the ROM produces a black dot on a printout or a bright spot on a CRT screen, and each "0" bit a blank space.

Table 1. ROM Combinations for Various Fonts

FONT	CHARACTERISTICS	PARTS REQUIRED
5 x 7	Raster Scan	SK0001 or MM5240
7 x 5	Vertical Scan static ROM required	SK0002 or MM5241
7 x 9	Raster Scan	MM5241 (2 required)
9 x 7	Vertical Scan static ROM required	MM5240 (2 required)
8 x 10	Raster Scan	MM5241 (2 required)
10 x 8	Vertical Scan static ROM required	MM5240 (2 required)
9 x 11	Raster Scan	MM5240 (3 required)
11 x 9	Vertical Scan static ROM required	MM5241 (3 required)
12 x 16	Raster Scan	MM523 (6 required)
16 x 12	Vertical Scan static ROM required	MM5241 (4 required)

Two new soon-to-be-announced ROMs are the MM5240, storing 64 x 8 x 5 bits, and the MM5241 storing 64 x 6 x 8 bits. Each chip also contains decoding logic and sense amplifiers (as do the 1024 and 2048-bit chips). Thus, one ROM is ample for a standard 5 x 7 or 7 x 5 font. The added capacity can implement special needs, such as dropping comma tails below the other characters and symbols. But its main purpose is in providing the logic and programming flexibility that enables ROMs to be operated in tandem to generate the larger font sizes indicated in Table 1. The additional capacity costs little in terms of silicon real estate because these devices are made by low-threshold processes with p-channel-enhancement mode MOSFETs as the storage elements—the most LSI-able type of MOS.

In the past, when diode matrixes were used as character generators, the 5 x 7 or 7 x 5 fonts gave the best cost/legibility tradeoff. Because the new ROMs lower the cost per function, the 8 x 10 font will probably become the most attractive.

The input-output configurations of the MM5240 and MM5241 are outlined in Figure 4 for a standard ASCII-addressed font. The 6-bit ASCII code words will address any of 64 characters (2^6). The control logic generates the three additional address

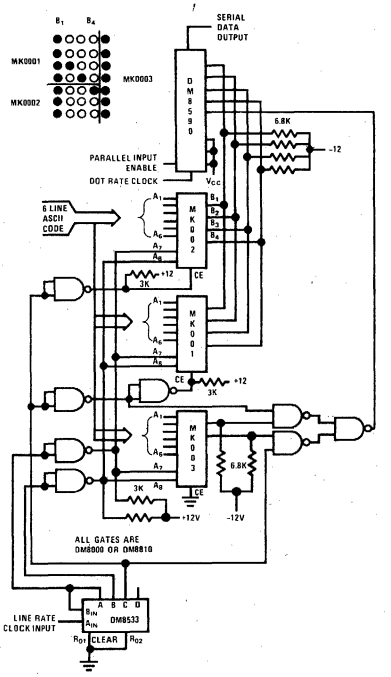


Figure 2a. Three-ROM Raster Scan Character Generators

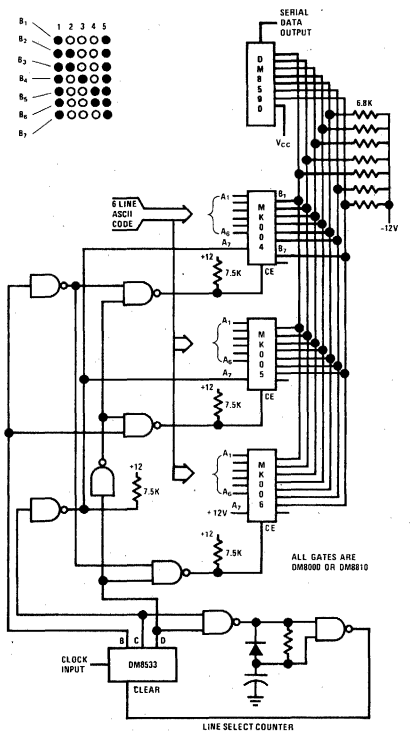


Figure 2b. Character Generator For Tape Printers and Other Vertical Scan Applications

CHARACTER SELECT

I_1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
I_2	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
I_3	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
I_4	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
CHAR.	0	8	4	12	2	10	6	14	1	9	5	13	3	11	7	15

ROW
I_5 I_6

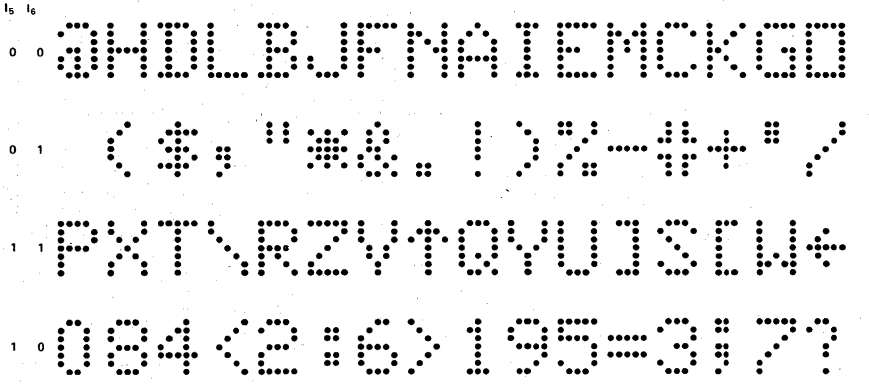


Figure 3a. Raster Scan Character Font

CHARACTER SELECT

I_6	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
I_5	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
I_4	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
I_3	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
CHAR.	0	8	4	12	2	10	6	14	1	9	5	13	3	11	7	15

ROW
I_2 I_1

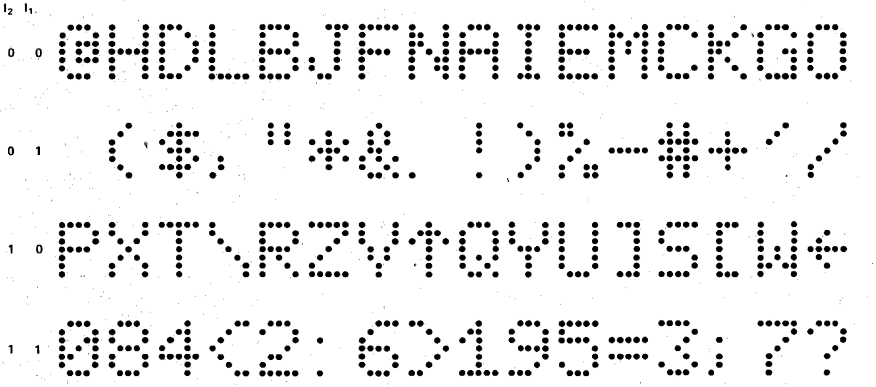


Figure 3b. Vertical Scan Character Font

bits needed to select the individual lines or columns of dots that form the characters in the

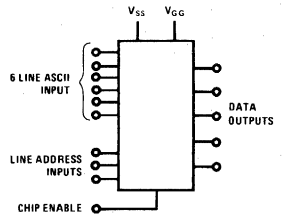


Figure 4a. MM5240 Raster Scan Character Generator Element

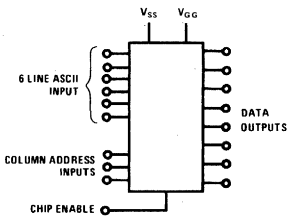


Figure 4b. MM5241 Vertical Scan Character Generator Element

5 x 7 x 64 dot matrix. The output bits forming each dot line or column are presented in parallel. The parallel outputs are serialized by a TTL register and used to control the CRT beam or the printer mechanism. To simplify the selection process, the ROMs are programmed to generate the lines or columns in the correct sequence when addressed by the sequential outputs of a TTL counter.

As for registers, they became quite popular during 1969 because a CRT refresh memory of up to about 5,000 bits—enough for a display of more than 800 characters—could be built less expensively with MOS dynamic registers than with delay lines.[2] This was achieved with registers containing 200 storage stages per chip. During 1970, dynamic registers up to 512 bits long will go into mass production, giving rise to predictions of significant savings in refresh memory costs. Whether savings that large can actually be realized will depend upon how quickly the new devices catch on and go into volume production.

Aside from cost per function, other pertinent consideration are temperature sensitivity and functional flexibility. In a refresh memory, register outputs are fed back to the inputs. On each recirculation, the data readdresses the ROM, regenerating (refreshing) the display (Figure 5). The recirculation times must correspond to the CRT scanning time to keep the display legible. MOS register delay times are relatively insensitive to temperature variations because they are established by system clock rates rather than physical parameters.

Also, special requirements of data entry and output for display formatting and editing can be implemented much more easily with registers than with physical delay lines. Data bit positions in the recirculation loops are maintained in alignment and can be monitored and modulated precisely by the control logic (one recirculation loop is needed for each data bit—six loops, for example, in an ASCII-addressed system). Data entry and output for display or transmission thus becomes a straightforward exercise in logic design.

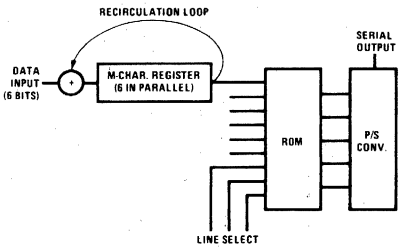


Figure 5. Basic Digital Character Generator and CRT Refresh Memory

BIPOLAR COMPATIBILITY

A dynamic register is one that must be clocked at some minimum frequency. Data is retained in the form of charge storage and the charges would eventually leak out of the storage nodes if not re-established. In contrast, the ROMs being discussed are static devices, generating an output only when addressed. Specifically, they are designed and programmed to be sequenced by TTL ICs. Furthermore, the new generations of ROMs and registers accept and put out bipolar level signals and operate off +5 volt and −12 volt power supplies.

These features eliminate any need for special level-translating circuits between the MOS and bipolar devices. Also, special power supplies are not generally required because ±12V as well as ±5V supplies are usually provided in terminals for other parts of the system. Such compatibility is a convenience and a cost saver in any digital system containing MOS storage subsystems and bipolar logic, since it minimizes the interface and drive complexity. In terminals, though, compatibility is practically essential for efficient operation and lowest cost per function.

First, as the detailed system diagrams show, many of the interconnections have a MOS device at one end and a TTL device at the other, so that a large number of level translators would be needed if they were not compatible.

Second, several control logic operations must occur between memory outputs, and the output-serializing device must operate at least six or eight times as fast as the word (dot line or column) output rate of the ROM. Obviously, if high speed

control logic—preferably TTL MSI devices such as single-chip binary counters and 8-bit parallel-input/serial-output shift registers—were not used, the character generating process would be slowed excessively. This would limit the number of characters that could be displayed in a CRT refresh cycle or printed out in a given time. The new generation of MOS ROMs can deliver up to eight bits in parallel in about 700 nanoseconds, compared with a microsecond or more for last year's models. Logic speeds around 10 MHz are therefore desirable (several times higher than the speed that can be achieved by MOS gates.) Likewise, dynamic registers can now easily be run at rates above 2 MHz—double the speed of early mass produced registers—so the logic controlling refresh storages must also be faster.

The improved compatibility and higher speed are largely due to better design and processing of the input and output stages of the registers and the sense amplifiers of the ROMs. They don't increase the complexity of the MOS circuitry, unlike other techniques for increasing MOS speed, and therefore they have permitted the capacity increases cited.

The net benefit to the system designer of this approach to MOS design is that it enables the system designer to capitalize on the best features of each technology—MOS storage for high density and low cost, and TTL for high speed processing of data and control signals. This is what produces lowest cost per function in most digital systems.

CRT RASTER SCAN DISPLAYS

The basic refresh mode in Figure 5 limits the number of characters that can be displayed. A better way of generating and refreshing raster scan displays, particularly those with many rows or lines of characters, is outlined in Figure 6. Figure 7 illustrates the timing and logical implementation for a multiple row system.

As before, coded data from a communications link or the console keyboard passes through the registers and addresses the character generator. In these examples, the 6-bit ASCII input and the 3-bit control logic input generate raster scan character formats that allow a conventional TV monitor to be used as a display. Communications codes other than ASCII can be used.

If the ROM contains a 5 x 7 font, each 5-bit character line output will form five horizontal bright spots on the CRT. That is, each ROM output generates one-seventh of each character in a row of displayed characters. The output is serialized by the TTL register and used to intensity modulate the CRT beam as it sweeps across the screen.

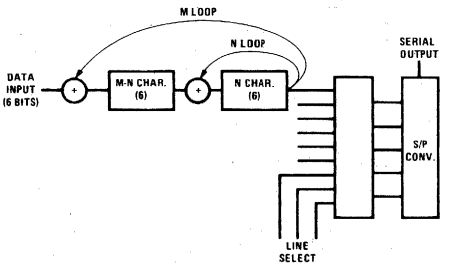


Figure 6. (M-N)+N Technique for Large Page Displays

The refresh memory registers are divided into M-N and N sections to facilitate page displays. M is the total number of characters displayed in several rows (lines of the page) and N is the number of characters in each row. To form such a display with single-loop registers, as in Figure 5, would take seven recirculations of all M data words during each refresh cycle of the CRT. The technique in Figures 6 and 7 only requires high speed recirculation of N bits at a time, with advantages that will be discussed shortly.

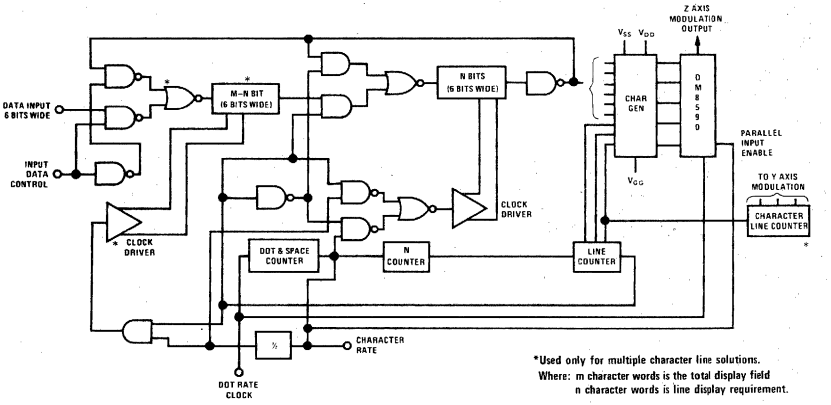


Figure 7. Multiple Row Raster Scan Display System

Assume that on the first sweep of the CRT beam, the ROM is being addressed by the six register outputs representing characters N_1, N_2, N_3, etc. The first horizontal, 5-dot line of each character in the display row are displayed in sequence. Then the line address inputs to the ROM from the control logic change to their second state at the time that N_1 has completed its recirculation to the N register's outputs. Thus, on the second CRT sweep, the second series of 5-dot lines are displayed horizontally for all N characters. At the end of seven recirculations, the complete row of N characters is on the display.

Now, the contents of the N register are not returned to the input of the N register. Instead, they are fed back to the input of the M-N register and this register is clocked to load the N register with the second group of N characters. The M-N register is then held still while the N register recirculates seven times to generate the second row of characters on the display. After all M characters are on the display, the first group of N characters is reloaded into the N register and the entire process is repeated to refresh the display.

Human factors—chiefly the eye's response time—dictate that the display be refreshed at least 30 to 35 times a second for good legibility. Most designers prefer to refresh at 60 Hz power line frequency because it is generally the most convenient frequency.

Besides generating the line address inputs (that is, the number of recirculations of the N register), the control logic keeps track of the number of dots and spaces in he output bit stream. The spaces between characters in a display row are inserted as "0" bits when the ROM outputs are serialized by the TTL register. The counters also control the loading and recirculations of the MOS registers in the refresh memory subsystem.

A multiple row raster scan display could be generated with the M-loop technique in Figure 5 but, the implementation is difficult and impractical. This technique is more appropriate for single row displays. Using this method of display, all M characters to be displayed must recirculate seven times to generate a 5 x 7 horizontal scan, so all stages of the registers must operate at the full character rate. To form several rows with a single-loop memory requires an interlaced scan rather than an ordinary raster scan. The first series of 5-dot lines are generated by the first N character outputs as before, but the next set of N inputs to the ROM will generate the first group of 5-dot lines in the second row of characters on the display. Therefore, the beam must jump to the new line position. To display four rows of 5 x 7 characters, for instance, would require a staircase generator that would step the beam by the height of nine scan lines (seven dot lines, plus two blank spacing lines between rows) three times after the initial scan. Then, as the second of the seven recirculations begins, the beam would have to be shifted an additional line to start the second series of line scans—and so forth.

The M-N-N technique does not require any more register stages than the M-loop technique and significantly reduces control and drive circuit requirements—again producing a lower cost per function.

REFRESH MEMORY MODULATION

The technique employed in the M-N-N refresh memory is called "clock modulation". In other applications, it has already been found to significantly reduce total storage costs.[3] It helps minimize power dissipation—in most terminals, the amount of power consumed is unimportant in itself since line power is used, but registers are powered by clock drivers and the cost and complexity of the drive network is certainly important. Furthermore, the technique allows long, very high-density MOS circuits, produced by relatively inexpensive low threshold (bipolar compatible) processes to operate at very high effective character rates.

As shown in Figure 7, the raster scan system uses nine clock intervals to generate a row of characters on the display. Seven are for the high-speed recirculations. During the other two intervals, the first N characters are fed back from the output of the N register to the input of the M-N register while the N register is loaded from the M-N register with a new row's worth of characters. Since two intervals are used for this operation, the registers operate at only half the character rate. The rest of the time, the M-N register is charge-quiescent. Its average clock frequency is only about 11% of the character rate.

In other words, most of the refresh memory (perhaps 90% in a large display system) operates at only half the character rate (say 1 MHz instead of 2 MHz) only two-ninths of the time. The savings in the drive network alone can be judged from the power-frequency plot for a typical MOS dynamic register (Figure 8)[3]. In addition, the designer can

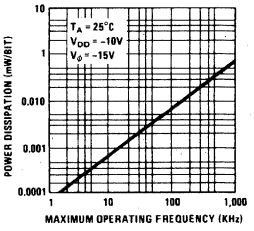


Figure 8. Power vs Frequency Plot of Typical MOS Dynamic Register

increase the number of characters generated per refresh cycle, for a larger display, or increase the number of dot lines, for a larger font, or both.

Remember, though, that dynamic registers must be clocked to retain data. How long can the M-N register be turned off? Long enough for practical applications. The guaranteed minimum frequency is temperature dependent, since temperature affects charge-storage time. The minimum for National Semiconductor's MM-series registers is 500 Hz at 25°C, rising to 3 kHz at 70°C (maximum operating temperature is 125°C, but that is not a display environment). At room temperature, the registers can safely be quiescent for as long as 2 msec. (The typical MM register will actually hold data for 10 msec.) Suppose the N register stores 40 characters and operates at 2 MHz. The quiescent period can be as short as 40 x 7 x 0.5 = 140 μs. If standard TV raster timing is maintained then the quiescent period will be 7 x 63 μs = 441 μs. Obviously, the designer has great leeway in character rates, operating temperatures, and register capacities.

Other applications in displays for clock modulation include input-output buffering of data during data reception and transmission,[2] or during display editing and formatting through the console keyboard. The register rates can be adjusted via control logic to accommodate differences between I/O and recirculation rates. Note that the gating in Figure 7 permits data entry under TTL control into either register section.

CHARACTER GENERATION

The first generally available MOS character generators were kits such as those in Figure 2, using three 1024-bit ROMs (MM521). Although single-chip generators were being developed in 1969, they were in very short supply. The kits cost about half as much as diode generators and thus allowed terminal manufacturers to start the changeover to MOS.

The kits are also a good place to begin describing character generator operation in this application note, because they provide an "exploded view" of multi-ROM generator operation. Similar techniques will be needed to build larger fonts with the new devices. The external gating functions shown in Figure 2 are not needed for these fonts when the MM5240 and MM5241 are used. The "assembly" of the dot patterns is taken care of in the programming of the ROMs. However, to generate a large font, such as 8 x 10 or 12 x 16, with the new ROMs will require operation of two to four ROMs.

Each MM521 in the SK0001 raster scan kit can store 256 4-bit dot patterns. As the inset letter "N" in Figure 2a indicates, the MK001 ROM stores the first four 4-dot line segments of each of the 5 x 7 characters, the MK002 stores 4-bit segments of the other three-dot lines, and MK003 supplies the fifth bit of each of the seven-dot lines. All ROMs are addressed simultaneously.

The 6-bit ASCII code was devised to select 64 (2^6) characters. However, an 8-bit address is used to select the dot lines and the 6-bit ASCII code from the 256 (2^8) word locations in each ROM. These two additional bits are supplied by the A and B outputs of a TTL binary counter DM8533 (SN7493) and the counter's C output is used to commutate the MK001 and MK002. The ROMs are enabled by an output at the TTL logical "0" level. Thus, with the gating shown, the MK001 is enabled during the first four of seven line-rate clock inputs and the MK002 during the remaining three inputs.

The MK003 is continuously enabled by grounding the chip-enabled pin, CE. It must generate a 1-bit output for each of the 7 x 64 dot lines in the 64-character set, which implies a 9-bit address. Rather than produce a special ROM just for this function—which would make it expensive—the MM521 was programmed to generate 256 2-bit outputs from the 8-bit address. The counter's C output simply gates out the unwanted bit.

For a 5 x 7 font, the new single-chip character generators are simply programmed to generate all 5 bits in each dot line, from a 9-bit address. Standard programming provides the 64-character ASCII set, but special characters can be substituted by changing the stored dot patterns. The reprogramming process consists of altering an etching mask that controls gate insultation thickness in the MOS field effect transistors of the storage array. If the oxide is left thick, the transistor will not switch when selected by the decoding logic, generating a "0" output from that location.

Figure 9 indicates why the storage capacity of the MM5240 is 5 x 8 x 64 rather than 5 x 7 x 64—each ROM can generate half of the 8 x 10 x 64 character set. The ROMs can be addressed simultaneously, as before, and be commutated by the

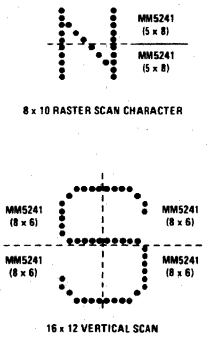


Figure 9. Multiple ROM Character Fonts

control logic to put out the 8-dot horizontal lines in the correct sequence. For very high speed character generation, the addressing of the ROMs can be skewed or overlapped so that the outputs from one are generated while the inputs to the other are being decoded. The only real limitations to the

character generation rates achievable with such techniques are the speed of the bit serializing logic and the bandwidth of the video circuitry.

CONTROL LOGIC

Starting with the dot/character or dot and space counter in Figure 7, the counter moduli are set to accomplish the following functions:

- The dot and space counter determines the number of horizontal spacing bits between characters in the character row on the display. Its output is loaded into the parallel inputs of the DM8590 serial-in/parallel-out shift register. For a 5 x 7 font, for example, a modulus of six inserts one spacing bit (logical "0" bit) between each 5-dot group in the serialized stream. During line recirculation periods, this counter also drives the N counter at the character shift rate of the N register.
- The N counter causes the line select counter to change state at the end of every recirculation of the row data in the N register. It generates a pulse at intervals of 6N dot clock periods (assuming one spacing bit).
- The line select counter generates seven sets of the three address bits that sequence dot-line selection from the ROM.
- A character line counter is needed in some raster-scan displays to keep track of which page line has just been generated. This time is signified by the C or D output of the line select counter.

Outputs of the first three counters actuate the register clock drivers, keeping the line select bits in synch with the data code. If the line select counter is a 4-bit binary device, eight states are available on the ABC outputs (000 through 111). The D output can be used to provide a ninth state and the reset function. Only seven states are needed for line select, so the eighth and ninth states provide the interval needed for loading the N register from the M-N register, as previously described.

VERTICAL SCANNERS AND PRINTERS

Vertical scan character generators are generally used in hard copy applications. Also, a vertical scan type of character generator can sometimes be more suitable for CRT displays than raster scan.

Displays or printouts of calculators and small business machines often show only numerals and a limited variety of symbols—not enough for a full alphanumeric generator. Such fonts are easily programmed into a small ROM such as the 1024-bit MM522, which stores 128 8-bit words. There's room for 16-5 x 7 dot characters on the chip.

These ROMs are also used in the SK0002 kit for a 64-character ASCII-addressed font (Figures 2b and 3b), which requires the storage of 320 7-dot columns and a 7-bit address. Connected as shown, the DM8533 TTL binary counter will reset on the count of 16. And with the gating and interconnections shown, the column select cycle is:

Counter Outputs DCB	ROMs Enabled
DCB	
000	MK004
001	MK005
010	MK004
011	MK005
100	MK006
101	reset (instantaneous)

A CRT beam can be intensity modulated by the serialized output, as in the raster scan technique. However, the electron beam traces either a sawtooth or pedestal-type scan pattern on the screen (Figure 10). Every column of each character in the display line is scanned in sequence, starting at the left-hand side of the screen.

The sawtooth scan is straightforward, but the pedestal scan requires that the bit order be reversed in the second and fourth columns. To do this, the outputs of the MK005 ROM are simply connected to the output buses in the reverse order (i.e., output 1 to bus 7, output 2 to bus 6, etc.).

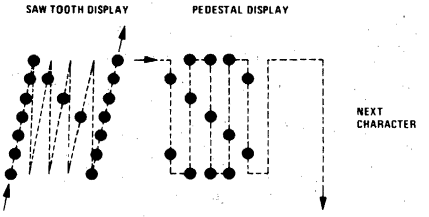


Figure 10a. Two Techniques for Vertical Scan

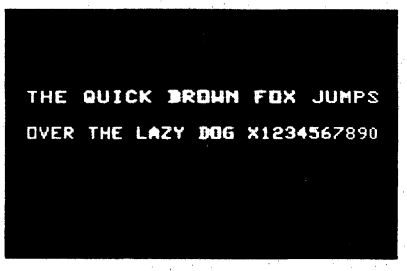


Figure 10b. Example of Character Generation Using Pedestal-type Scan.

Long shift registers, operating at relatively slow rates can be used. The character rate—the register shift rate—is no more than 1/6 of the column-select rate for a 5 x 7 font, since the beam traces one complete character before going on the next one. A dot counter loads spacing bits between characters via the TTL shift register, a character counter triggers the sawtooth or pedestal scanning patterns, and a row counter would control positioning of the beam in a page display system.

In the new single ROM (MM5241) version of this system, (Figure 11), a 9-bit address is needed, 6 bits for the ASCII code and 3 bits for dot column select, Since the ROM stores five dot columns for each of 64 characters in a 5 x 7 font, 3 decode line are necessary. Also, the ROMs are programmed differently for sawtooth or pedestal scanning. Because the output pins are committed for all columns, external connections cannot simply be used to reverse output bit order.

Hard-copy printers can use the same fonts as vertical scan CRT displays. MOS registers may be used for data input buffering, but of course refresh registers are not generally required. The character generator output may be used to select some combination of 35 hammers, needles or electrodes that print the 5 x 7 dot patterns on the paper. One technique for handling the character generator output is shown in Figure 12.

In Figure 12, a TTL counter connected to divide by six (five columns and the blank column space between characters) generates the column select address. The ROM's outputs are accumulated in TTL latches (or held in TTL serial-in/parallel-out shift registers). When all dots for a character are ready, they are printed. In tape printing applications in which a 7-transducer array sequentially prints or punches a column at a time as the paper moves under the transducers, the ROM outputs can be used as they are generated unless storage is required for some other purpose.

Character generators are not needed for conventional electromechanical typewriters. But MOS ROMs do have a role here—one version of the MM521, for example, is programmed to convert the ASCII communications code into the Selectric code used to control ball-type printers.

PRINTING APPLICATIONS

The application of character generators in a printing application is normally quite different from that of the display system. Most printers require that a total character font be available before the print is executed. An example of a practical method of accomplishing this (Figure 12) is to sequence the character generator element through the font sequence. Each of the character columns or rows is addressed. The character generator output data at each of these address intervals is transferred into bipolar memory. This

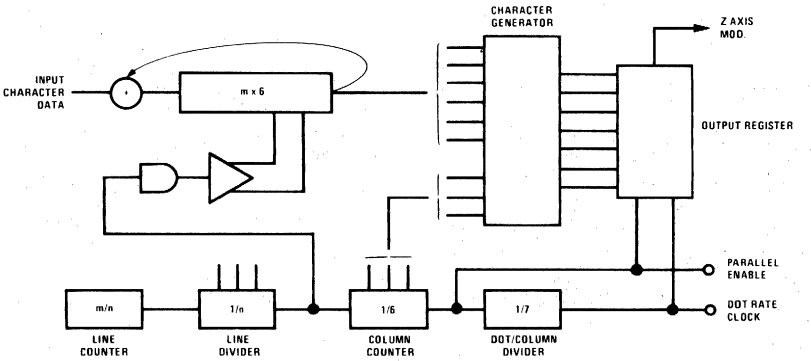


Figure 11. Vertical Scan Display System

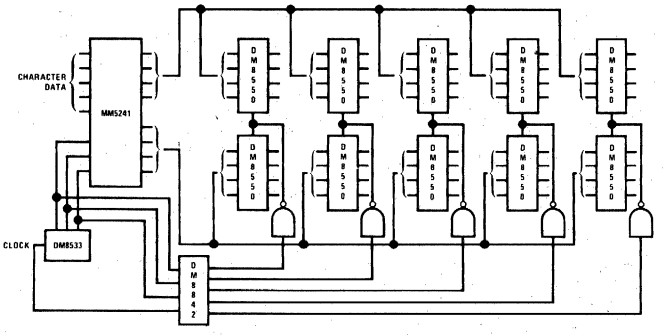


Figure 12. Printer Application Block Diagram

memory not only satisfies the memory storage but also the general power buffer which is required between the MOS character generator and the electromechanical on thermo electric printer. In the printer application there may be a requirement to buffer the input data with data storage because of the relative differences in data and printer rates but generally there is no need to retain the printed character intelligence.

The data transfer from the character generator to the bipolar memory in Figure 12 is accomplished by sequencing the column address lines and enabling the appropriate memory simultaneously. Each pair of DM8550s (SN7475s) then contains the data for one of the five columns in a character. The DM8842 (SN7442)—one in 10 decoder provides the decoding functions which are connected to the enable line on the quad latches.

LARGER, FASTER SYSTEMS

Most low cost terminal designs have been based on the 5 x 7 font because of the high cost of diode matrixes and wideband video circuits. But it is by no means the most legible font. A 5 x 7 font is acceptable for applications in which the display changes slowly, but human engineering studies indicate that it causes severe eyestrain when an operator reads rapidly changing data.

The greatest portion of the discussion has dealt with a 5 x 7 font. A full 64 character display can be coded into a single MOS package. Now that LSI has entered the scene, we see a different trend towards larger, more stylized font. The economy of MOS ROMs will provide the customer with a more legible character font at the present cost of "discrete" character generators. An analysis of the most practical solutions to various fonts are tabulated in Table 2. The part types which have been used to generate a 64 x 7 x 5 raster scan font are the SK0001-3 ROM kit or the MM5240 which is under development. The vertical scan font is satisfied by the SK0002-3 ROM bit or the MM5241 which is under development. If we examine the other possible fonts, these same two monolithic elements will satisfy the requirements if they were 64 x 8 x 5 and 64 x 6 x 8 respectively. Therefore, the added memory storage is being incorporated into the MM5240 and MM5241. In some of these cases the font is scanned in the horizontal dimension while in others the font is scanned in the vertical dimension. You find both the 8 x 5 and 6 x 8 elements capable of satisfying the font matrix requirement. Since all the ROMs listed are static by design, there are no special clocking hardships induced with the solution of any of these larger fonts. This is not true for all dynamic ROM solutions.

As mentioned before and shown in the table, the same ROM element is used in both raster scan or vertical scan applications. If we recall the design solutions showing the refresh memory and character generator for a 5 x 7 display, the first thing which is apparent is that the sequencing of the character generator is different in each of the two basic techniques. In one case the character generator is sequenced at the character rate (raster scan) while in the other case the generator element is sequenced at the column rate (vertical scan) of the font.

Since a display utilizing the vertical scan techniques has input address changes at some multiple of the display character rate, a clocking system for a dynamic ROM character generator must be supplied. This requires the addition of a frequency divider and clock generator which results in a higher system cost when dynamic ROMs are used.

A second consideration which should not be overlooked in systems cost is the compatibility of ROMs in multi-package character fonts. Optimum ROM usage and organization will result in lower systems cost. ROMs will also find applications in micro-programming and code conversion where synchronous operation is preferred.

The 8 x 10 font is much better and 12 x 16 is almost optimum for legibility. Small, lower case characters can be sharply defined, too, and they almost appear to be drawn with continuous strokes.

System designers considering these fonts for low-cost displays run, at present, into CRT cost problems. The least expensive displays are television-type CRTs with limited video bandwidth. Bandwidth also limits the number of characters that can be displayed simultaneously. Not counting the times required for beam retrace and functions other than character generation, which reduce the time available in a refresh cycle for dot handling, the necessary bandwidth is roughly:

BW = (dots and spacing bits per character)
X (characters per display row or page)
X (refresh rate)

TV-type CRTs have a maximum bandwidth of about 4 MHz, of which only about 2.5 MHz is generally useful. If one uses a 5 x 7 font with one spacing bit (6 x 7 total) at a 60-Hz refresh rate, each displayed character needs 2.52 kHz of bandwidth, so the limit is about 1,000 characters. In contrast, the new ROMs take as little as 700 nanoseconds to generate a dot line, or about 5 μs per character. That's fast enough to generate 200,000 characters a second, or a display of more than 3,000 characters at the 60-Hz refresh rate. The actual dot rate in the serial bit stream to the CRT can approach 10 MHz. And if larger fonts are generated in some multiplexed addressing mode, the required bandwidth can be much higher.

Luckily, these problems are not insurmountable and there are alternatives to using oscilloscope-quality CRTs or storage tubes, which are fine for high performance applications but too rich for low cost terminals.

Obviously, the designer can drop the refresh rates. New CRTs with longer persistence phosphors facilitate this. Also, CRT manufacturers have been responding to the new terminal market by working on bandwidth improvements, and they are apparently going to reach 10 MHz in moderately priced video systems soon.

Finally, the designer is not obliged to display his characters digitally just because he uses a MOS ROM. Don't forget that the ROM is really working as a code converter, generating a 35-bit machine language code from a communications code. The language translation can be whatever the situation requires.

All that need be done is update methods used in analog displays, which form characters with strokes rather than dot lines or columns. The ROMs can be programmed such that the bit outputs, when integrated, control X and Y ramp generators. The slopes of the ramp functions are determined by the number of bits in a sequence and the lengths are determined by the locations chosen for turn-off bits. As in the vertical scan technique, the ROM is addressed at the character rate.

Even though some characters can be formed with one or two strokes (I, L, etc.), equal time should be given to all characters in a page display to keep the character rows aligned. A standard sized area of the MOSFET array, such as 6 x 8 or 5 x 8 should be used for each character. Most patterns would thus be a combination of stroke and no-stroke outputs. The single-chip fonts have an 8-stroke capacity for each of 64 characters which is more legible than the standard segmented type of instrument readout, since slant lines could be generated wherever needed.

APPENDIX

WHAT ABOUT INSTRUMENTS AND CONTROLS?

While it is safe to predict that 1970 will be "the year of the MOS" in alphanumeric terminals, MOS applications in numeric readouts are just beginning to emerge.

A new device with considerable promise in this field is a high voltage, MOS static shift register, the MM5081. Developed by National, it has a TTL-compatible serial input, 10 parallel outputs that can stand off −55V, 10 latching-type storage stages, and a serial output.

This novel combination of functions means that the MM5081 can drive lamps, numeric indicator tubes, filament tubes in segmented number and symbols displays, electroluminescent panels, and the new gas-cell arrays. In short, it provides MOS with a good foothold on the numeric side of the readout family tree in Figure 1.

The register stages can either shift the bits to the serial output for recirculation or store the data indefinitely. Hence, displayed characters can be swept along a line of indicators, "frozen" on a stationary display, or made to reappear periodically at any desired repetition rate.

A code-converting/character-generating ROM can be placed at the register input, to display numbers and symbols or alphanumerics. A designer can get almost as much flexibility from a lamp or panel display as from a CRT display. In fact, the first application of the MM5081 is controlling a matrix of neon lamps in a moving billboard display.

Some applications for character generators in instruments are also cropping up. Displaying range scales on an oscilloscope is a good idea that can be improved upon with the new ROMs. The display frees the operator of the chores of mentally calculating scale factors and manually writing these on scope photos. With an alphanumeric font, the camera can also record information such as test conditions, date and time of test, identification numbers, etc. Photo sequences and the data needed to analyze the curves can be coordinated automatically.

Similarly, a ROM can be programmed to display standard curves for go-no-go equipment checkout operations. For example, if a radar's pulse amplifier should have certain output characteristics, the ROM generates the correct output curves through a digital-to-analog converter and stroke generator. When an actual operating characteristic and the reference curve are displayed simultaneously, the operator can tell at a glance whether the radar is functioning properly. Many curves or general purpose curve segments can be programmed into a ROM and picked out as needed with selector switches or a ROM microprogrammer.

ROMs can be programmed as lookup tables, random-logic synthesizers,[4] encoders, decoders, and microprogrammers as well as character generators. A single ROM can perform limited combinations of these functions, virtually qualifying it as a microcomputer. It has been suggested that this capability be used in control panels to perform functions like actuating an alarm when a transducer level goes out of range and initiating corrective action. ROM addresses can be derived from digital meter circuitry. In multi-point measuring systems, this would provide the solid state equivalent of a rack of meter relays.

DEFINITIONS OF DISPLAY TERMS

Font: A set of printing or display characters of a particular style and size. A typical dot-character font is 5 x 7, referring to the number of dot locations per character.

Dot Character: A character formed by a pattern of bright dots on a CRT screen or dark spots on hard copy, rather than by continuous strokes. The dot

pattern corresponds to bit-storage patterns in a digital memory.

Column: In a dot character matrix for vertical scanning, a column is a vertical series of dots. On a page display, a column contains several vertically aligned characters. In this article, a column refers to a dot column.

Row: A horizontally aligned group of characters on a display.

Line: In this report, line refers to the number of dots displayed in a single scan when a raster scan character is generated. In a 5 x 7 dot character, there are seven lines of 5 dots each.

Page: A display consisting of several rows of characters, corresponding to lines on a printed page.

Raster Scan: See Figure 9.

Vertical Scan: Two types of CRT vertical scans are shown in Figure 10. In hard copy applications, the dots in a column or character may be printed simultaneously by the printing transducers rather than being scanned.

Sawtooth Scan: See Figure 10.

Pedestal Scan: See Figure 10.

Dynamic Element: A digital device that must be clocked. A dynamic shift register must be clocked to retain data. A dynamic ROM is clocked to decode the address and generate an output.

Static Element: A device that does not have to be clocked to retain data. A static ROM uses direct coupled decoding for bit selection and static output buffers.

REFERENCES

1. A.D. Hughes, *Desired Characteristics of Automated Display Consoles, Proc. Society for Information Display,* Vol. 10, No. 1, Winter, 1969.

2. Dale Mrazek, *MOS Delay Lines,* Application Note AN-25, National Semiconductor, April, 1969.

3. Dale Mrazek, *Low Power MOS Clock-Modulated Memory Systems,* Application Note AN-19, National Semiconductor, April, 1969.

4. Floyd Kvamme, *Standard Read Only Memories Simplify Complex Logic Design,* Electronics, January 5, 1970.

HIGH VOLTAGE SHIFT REGISTERS MOVE DISPLAYS

There was a time when one had to go to Times Square or Picadilly Circus to see a moving lamp display. But now they're going into stadium scoreboards, stock brokers' offices, waiting rooms and many other places where an attention-getting man-machine interface is wanted.

Naturally, display designers would like to make the control and drive circuitry more compact and less expensive. What's needed to replace the banks of discrete switching devices is storage and switching high-voltage circuits in monolithic form. That's exactly why National developed the MM5081 high-voltage MOS shift register.

This unusual IC is the first MOS device capable of driving gas-discharge tubes and other high-voltage display elements without going through a bipolar buffer such as a transistor or SCR. Moreover, it can "walk" the message around and around the display when operated in a recirculating mode. The latter feature provides a clear-cut division between system functions – the MM5081's take on the responsibility of display operation per se, while the system logic need only format messages and control updating by invading the registers. In other words, the main system logic need pay only intermittent attention to display operation. If the main system is a data-processing computer, for instance, it can handle the display like any other peripheral. Relieved of responsibilities for moving and refreshing the display, the main system can do more data processing between display updates.

REGISTER PLUS SWITCHES

Figure 1 shows in simplified form how one MM5081 would be connected to drive a bank of 10 neon lamps. A data bit stream is entered into the serial input and shifted at the clock rate to the serial output. Then, it can be routed back to the input and recirculated to repeat the display motion.

The states of the data bits circulating through the register control the switching of the MOS output transistors. When a bit in the true state (MOS logical "1") is being stepped down the 10 register stages, the lamps will turn on and off in sequence at the register clock rate. In this mode, the clock rate is the display rate. A typical display rate will move the light along by no more than two or three lamps per second, making any message displayed on parallel rows of lamps easy to follow and read. A latch-type register cell that can shift at frequencies to DC and a single-phase clock input are used in the MM5081 to achieve this effect. However, the logic formatting the data for display will have to run at some higher rate. If the control system has other functions as well, it may be desirable to load the register at a clock rate in the hundreds of kilohertz. At such a high rate, the bit stream flashes by the 10 parallel output switches too rapidly to see the lamps being turned on. After loading, when the main system logic is freed, the clock rate is dropped to the display rate and the message is seen. The message simply recirculates at the display rate until new data is ready for loading.

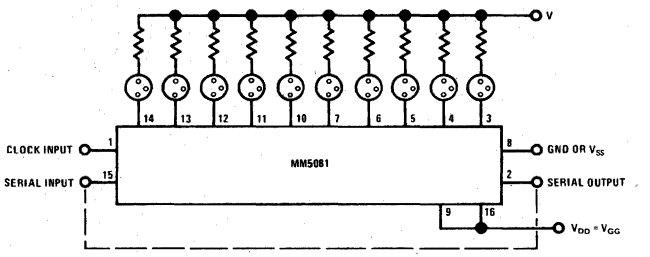


FIGURE 1. Block Diagram

The use of high-speed logic for control is facilitated by making the MM5081 with low-threshold, p-channel, enhancement-mode MOS transistors. As a rule, a low threshold device allows data to be entered at bipolar logic levels.

The output transistors do not need a large gate-voltage change to turn on and off. They are also low-threshold devices in this sense. But they have to withstand transients up to 100 volts and stand off steady state voltages up to 55V to operate lamp-type displays reliably. Adequate gate logic voltages for the output transistors must be ensured to make the lamps glow brightly when they should be on or to make them free of any residual glow due to switch leakage when the switching transistors are turned off. That is, a low R_{ON} and high R_{OFF} must be ensured despite very high voltage on the MOSFET drains. Because a pullup resistor is used, the input gate should be a TTL or DTL device with an uncommitted-collector output able to withstand at least 10V. Among such devices are the DM8810, DM8811 or DM7426 (SN7426) quad NOR-gates, or the DM8812 hex inverter. All these TTL devices will stand off to 14V.

The other two gates used in the input switch can be any TTL or DTL types. The arrangement shown brings the serial output back to the serial input through the top gate when the "new data enable" line is low (DTL/TTL logical "0") or permits the registers to be reloaded with new data when the enable line is high. A pull-down resistor is placed on the register output to handle 1.6 mA the current sinking required for operation of the TTL or DTL recirculation control gate.

TICKER-TAPE DISPLAY

A straightforward type of moving lamp display is illustrated in Figures 2 and 3. Simple messages such as CALLING DR. CASEY . . . CALLING DR. CASEY . . . DR. CASEY, PLEASE REPORT TO SURGERY . . . or stock quotes, or a series of instrument readings would be displayed as 7X5 characters by this system. That is, each character would be a lighted lamp pattern selected from a moving matrix seven lamps high by five lamps with a moving column of lamps turned off between characters. The off column is a space bit in each lamp row.

Assume that the display is long enough for 33 characters. Each row requires 33X6 lamps and 198 register stages. Each row is a cascade of 20 MM5081's. The input of the first register and the

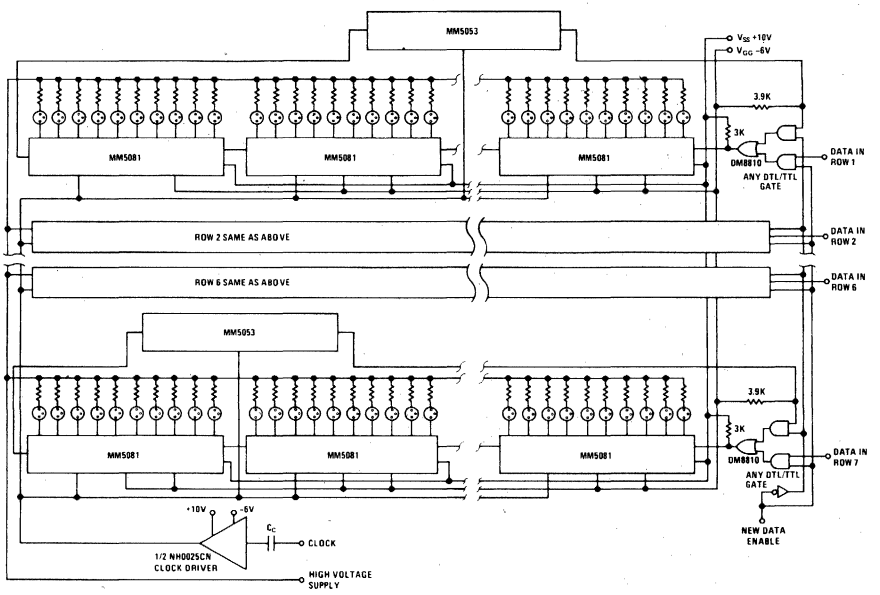


FIGURE 2. 7XN Bit Shift Register and Display

output of the last register are connected as in Figure 1, and the registers in between are simply daisy-chained by connecting each serial output to the next serial input. All seven rows would use 140 register packages.

The character data for this type of system can be formatted by a standard character generator. For instance, the standard ASCII code can address a bipolar compatible read-only memory such as National's MM5241AA, which is programmed to generate 5X7 dot-type characters for CRT display. However, in the lamp display system, the display refresh function is handled without an additional memory. The column bits are entered in each register chain, as before, through the input gating at a rate determined by the clock rate supplied the MH0025C clock driver. The MH0025C is a two-phase driver. However, since the MM5081 takes a single-phase clock input (converted to a two-phase clock inside the register package), only one of the dual drivers in the MH0025C package is shown (the other half can be used to share the clock-drive load).

After the registers are loaded, the clock into the driver is dropped to a frequency of 2 Hz, if the register was loaded at a higher frequency. This rate is stabilized by the coupling capacitor C_C. The coupling capacitor on this type of driver determines the maximum pulse width, but the minimum pulse width is established by the clock signal. So, at the lower frequency, the characters sweep smoothly from right to left across the display lamps. They repeat the message every 100 seconds because 200 register stages are in each of the seven parallel rows.

Both the clock driver and the registers operate off the 10V and –6V power supplied.

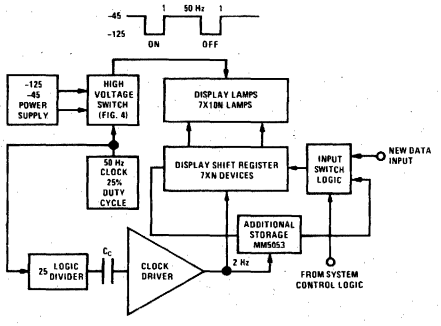


FIGURE 3. System Block Diagram

DISPLAY DRIVE

The high voltage supply (shown in the block diagram in Figure 3) is generated from a high voltage switch. The purpose is to limit the current and voltage across the lamps and the MOS output transistors to ensure that they operate reliably and have long lives. Also, the method reduces power consumption and allows lower power, inexpensive high-voltage power supplies to be used.

The high-voltage switch seen in Figure 3 and detailed in Figure 4 switches at a rate of 50 Hz and a duty cycle of 25%. Thus, when any of the MOS output transistors is on, the lamp that is "on" during that 250 msec display-rate interval (100% duty cycle at 2 Hz) is actually on for only 5 msec at a time. Then it turns off for 15 msec. This refresh rate was chosen because it provides a good lamp intensity with no apparent flicker.

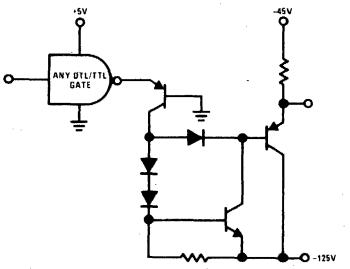


FIGURE 4. High Voltage Switch

The –125V supply turns on the lamps, and the –45V supply turns them off. But what is actually being used is the voltage difference, or bias. Most glow-discharge lamps require a 65V starting voltage and a 60V holding voltage. The switch keeps the lamps alternating between these levels while the MOS transistors are on, but imposes a maximum voltage of only –65V on the MOS transistors (that is, 125–60V) for the 5 msec "on" time. The MM5081 can easily take this – the spec allows –100V at 60 Hz (or 16.66 msec) and they are stress-tested to this level.

INDUSTRIAL DISPLAYS

The characters displayed can be any kind of symbol within the resolution of the lamp array – from letters to cartoon characters – and within the flexibility of the controls. Getting patterns to move back and forth while changing shape is technically feasible, but would require complex clocking techniques to put the bits in the desired location. Static pictorial displays would be fairly simple to implement, merely requiring loading of the registers at a high rate followed by storage at a DC display rate for the desired time. Although the characters would appear static, the high-voltage switch would keep the actual duty rate low.

There are many potential new applications for moving-lamp displays in industrial control systems. Functions such as process flow rates through several feeder pipelines or subassembly line rate in an assembly plant, cannot easily be set up on a CRT display. Complex computer graphic techniques or very expensive multi-gun displays may be needed.

The clock rates and lengths of a number of rows of lamps can readily be adjusted by hand-operated controls, such as voltage-controlled oscillators and gating between registers chosen by selector switches. Any feeder-line display rate that can be represented by the display rate could therefore be varied at a compressed scale of time and distance until the display operator arrived at the optimum balance of rates. This is a visual approach to a problem that generally requires complex mathematics and analog computers to solve.

Nor do the rows of lamps have to be aligned. Individual rows might represent route sections in a transportation network between junctions. By driving each section at a display rate simulating the speed of a particular train, and switching the "train" of moving lights from row to row via switches at the junctions (serial output to serial input register connections), control personnel could simulate system operation. Problems such as tie-ups – or worse – at junctions could be worked out by varying display rates for the trains whose schedules conflicted.

LOW FREQUENCY OPERATION WITH DYNAMIC SHIFT REGISTERS

In many dynamic shift register applications, it is advantageous to operate the circuit at low clock frequencies or in clock burst modes where high frequency clock rate periods are followed by long intervals in which the clocks are absent. To insure that his system will operate correctly under these conditions, the designer should be aware of the limitations of the type of shift register he is using.

There are two basic forms of dynamic shift register cells: the ratioless and the ratio. The ratioless circuit of Figure 1a is based on a capacitor precharge concept. During ϕ_{IN} clock time, node B is precharged by transistor Q_3; i.e., Q_3 is turned on by ϕ_{IN}, creating a low impedance path from node B to V_{GG} which charges the node capacitor C_2 to a negative voltage. Data is coupled at the same time through transfer transistor Q_1 to node A, the gate of Q_2. If the incoming data is a positive or "0" level, Q_2 will be in a high impedance off state, and node B will charge to a negative voltage one threshold more positive than the ϕ_{IN} clock amplitude.

When ϕ_{IN} returns to a positive level. Q_3 is shut off, isolating the precharged voltage of node B. The stored charge of node B, coupled with an additional increment contributed by C_4, redistributes between nodes B and C when the ϕ_{OUT} clock turns on transistor Q_4. The redistributed charge develops a negative voltage "1" level across C_3 which becomes isolated when ϕ_{OUT} returns to a "0" level. The "1" level turns on Q_5, resulting in a low impedance path between the output of the cell and V_{SS}, establishing a "0" level at the output.

In the ratioless cell, there are two nodes which become isolated from any charge replenishing source during normal operation of the circuit: nodes B and C. These are the nodes which establish the low frequency limitations of the cell. In most designs node C, the gate of the logic transistor Q_5, is the limiting node because total capacitance is less. If we had assumed the initial data coupled by Q_1 during ϕ_{IN} to be a "1" level, then node A would of course be the limiting node of the cell.

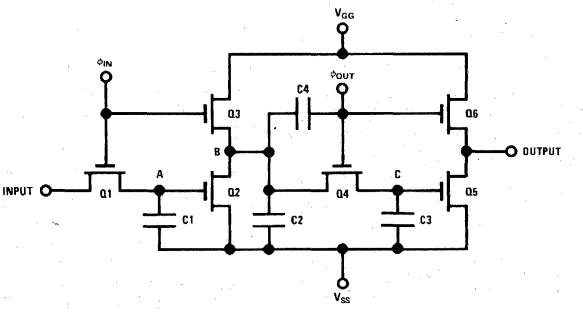


FIGURE 1a. Ratioless Dynamic Shift Register Cell

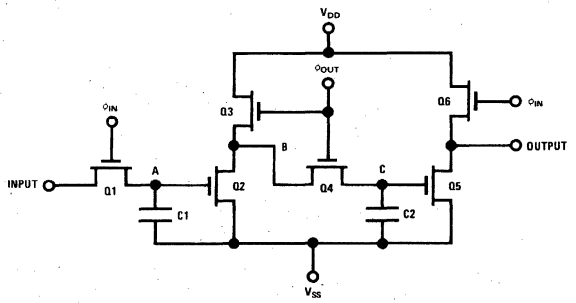


FIGURE 1b. Ratio Type Dynamic Shift Register Cell

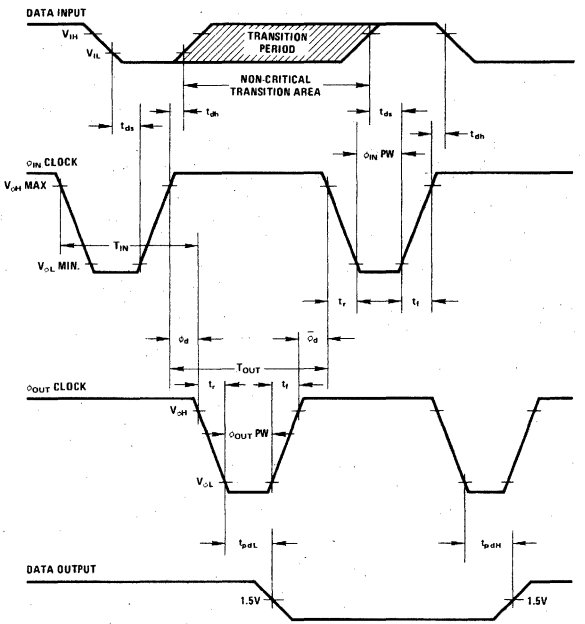


FIGURE 2. Timing Diagram For Two Phase Dynamic Shift Registers

The ratio dynamic shift register cell of Figure 1b has only one isolated node which limits minimum frequency operation. It, like the ratioless cell, is the gate node of the logic transistor. The ratio cell does not rely on stored precharge to establish a "1" level on a succeeding logic gate mode. If a "0" level had been transferred to node A of the ratio cell by Q_1 during ϕ_{IN} time, Q_2 would be off. A ϕ_{OUT} "1" level would turn on Q_3 and Q_4 creating a charging path between node C and V_{DD}, resulting in a "1" level at node C. The node would be isolated by Q_4, just as in the ratioless cell, when ϕ_{OUT} returns to a "0" level.

If the data coupled by Q_1 had been a "1", both Q_2 and Q_3 would be on during ϕ_{OUT} time. To establish a "0" at node B in that case, an electrical ratio between the on impedance of Q_2 and Q_3 must be considered by the cell designer.

Charge must be stored at the logic transistor gate node of the ratioless cell for the period of time between leading edges of the two phase clocks. This is because no charge enters the node B and C network after the leading edge of the transfer clock (ϕ_{OUT}) and there is no way for charge which leaks off the nodes to be replaced. This portion of the clock period is defined as a Partial Bit Time. The Partial Bit Time between the leading edge of ϕ_{IN} and the leading edge of ϕ_{OUT} is the T_{IN} period, and the time between the leading edge of ϕ_{OUT} and the leading edge of ϕ_{IN} is T_{OUT} (Figure 2).

The period of the minimum operating frequency is the sum of the two, or

$$\phi_f\,(\text{MIN}) = \frac{1}{T_{IN} + T_{OUT}} \qquad (1)$$

Obviously the lowest operating frequency can be attained when T_{IN} and T_{OUT} are each at their maximum limit and therefore equal. This says that for minimum frequency, 50% clock phasing should be used, i.e., the clocks should be equally spaced within the bit time.

The ratio cell has a similar storage requirement, but with one difference. During the time the transfer clock (ϕ_{OUT} in Figure 1b) is on, a source of charge is available to node C through the ON transistors Q_3 and Q_4, assuming Q_2 is OFF. Therefore, charge must be stored on the critical capacitor C_2 only after the transfer clock has returned to a "0" level, and isolated the node. This required storage time is usually referred to as Clock Phase Delay Time (ϕ_d). The phase delay time between the trailing edge of ϕ_{IN} and the leading edge of ϕ_{OUT} is ϕ_d; the time between the trailing edge of ϕ_{OUT} and the leading edge of ϕ_{IN} is $\overline{\phi}_d$ (Figure 2). Minimum clock operating frequency is:

$$\phi_f\,(\text{MIN}) = \frac{1}{\phi_{IN}\,PW + \phi_d + \phi_{OUT}\,PW + \overline{\phi}_d} \qquad (2)$$

assuming clock rise and fall time $\ll \phi_{PW}$.

Optimum low frequency operation can be obtained when the clock pulsewidths and phase delays are maximized and made equal. In most cases this would mean 10 μs clock pulsewidths and 50% clock phasing. For power or system application reasons it is usually not convenient to use such wide pulsewidths, and the minimum clock frequency is simplified to

$$\phi_f\,(\text{MIN}) \cong \frac{1}{\phi_d + \overline{\phi}_d} \qquad (3)$$

assuming $\phi_{PW} \ll \phi_d$ or $\overline{\phi}_d$.

Maximum Partial Bit Times and Clock Phase Delays for a given circuit are a measure of the ability of the critical nodes within the cell to store a minimum voltage level. Charge is usually lost due to leakage currents associated with the semiconductor junctions of the nodes. The total reverse leakage current for a p-n junction is the sum of three components; the bulk diffusion current, charge generation current and surface leakage current. Within the normal operating junction temperature range of MOS shift registers (–55°C to 150°C), the charge generation current is the primary component of leakage. Charge generation is usually attributed to recombination centers within the depletion layer of the junction. Leakage current generated in this manner is usually approximated by the expression

$$I_L = KT^{3/2}\,\epsilon\,-7020/T \qquad (4)$$

Where T = Junction temperature, °K

K = Proportionality constant

I_L = Leakage current of P-N junction

Therefore Partial Bit Times and Clock Phase Delays will be a definite function of temperature. Figure 3 shows a curve for Partial Bit Times as a function of temperature for a typical shift register using a ratio-less cell. Figure 4 gives the corresponding minimum operating frequency versus temperature for two cases: when $T_{IN} = T_{OUT}$ (50% clock phasing), and when one of the Partial Bit Times is minimized, the other maximized. Minimum Partial Bit Time is:

$$T_{(MIN)} = \phi\,PW_{(MIN)} + \phi_{tr} + \phi_{tf} + \phi_{d(MIN)} \qquad (5)$$

Any Partial Bit Time between minimum and maximum at a given temperature can be used. The minimum clock rate would be calculated using Equation 1.

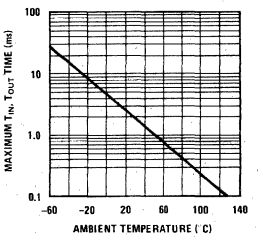


FIGURE 3. Maximum Partial Bit Time vs Ambient Temperature

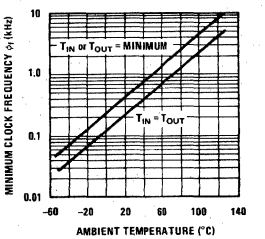


FIGURE 4. Minimum Clock Frequency vs Ambient Temperature

If the shift register utilizes a ratio cell, a curve identical to Figure 3 could be used to obtain maximum Clock Phase Delays for any required temperature. Equation 2 or Equation 3 could then be used to calculate minimum clock frequency at that temperature.

The shift register user can often increase his margin of safety when operating at low frequency, or for long periods of time with the clocks stopped, by designing the system with that operation in mind. The ambient operating temperature of the registers should always be minimized. The cell requires a minimum voltage at the critical node to operate, and the time to discharge the node to that value is dependent upon the initial voltage, as well as capacitance and leakage:

$$t_d \approx \frac{C_{NODE}\,(V_{INITIAL} - V_{MIN})}{I_L} \qquad (6)$$

t_d = T_{IN} or T_{OUT} for ratioless cells;

= ϕ_d or $\bar{\phi}_d$ for ratio cells

C_{NODE} = Total capacitance at critical node

$V_{INITIAL}$ = Voltage at critical node immediately after isolation of that node by transfer clock.

V_{MIN} = Minimum voltage required at critical node for operation.

I_L = Total leakage current at critical node.

The initial voltage can be optimized in two ways: by using the highest clock amplitude possible and by allowing something greater than minimum clock pulsewidth to insure that the maximum amount of charge is coupled to the node (and in the case of the ratioless cell, that the maximum precharge voltage is obtained before transfer). A high value of V_{GG} or V_{DD}, the negative supply voltage, increases on-chip power and therefore junction temperature, as well as increasing the minimum required node voltage. It is a good idea, therefore, to stay away from very high supply voltages. When both the clock driver reference voltage and V_{GG} or V_{DD} are the same supply, the best tradeoff is toward the higher end of the specified range, however. One other consideration which applies during operation at any frequency, but particularly at low frequency, is excursions of the clock line more positive than V_{SS}. This forward biases internal junctions which results in parasitic PNP transistors. If the collector of the parasitic PNP happens to be a critical node, the circuit will fail. Because critical nodes are often closer to the minimum required voltage during low frequency operation, registers are usually more sensitive to positive clock spikes.

When calculating temperature effects of a system operating in the clock burst mode, the designer must remember that power dissipation in the shift register is approximately double at 2.5 MHz what it is at 100 kHz. High frequency bursts will heat the chip, causing high junction temperatures which reduce the time the clocks can be off.

SUMMARY

Dynamic shift registers can be operated at very low clock rates if manufacturers data sheets are consulted and the proper clock phasing is used. Added margin can be designed into systems by keeping clock amplitudes high, the clock pulsewidths 10 to 20% wider than specified minimums, power supplies low and temperatures as low as possible. Beware of circuit board hot spots which increase the temperature of individual packages, or extensive interlead coupling or ringing which could result in positive clock spikes.

AMERICAN AND EUROPEAN FONTS IN STANDARD CHARACTER GENERATORS

Ten popular American and European 64-character subsets for displays and printers are now available from National as single-chip, standard character generators. These parts, listed in Table 1, are sold off-the-shelf without a ROM masking charge.

The ROMs are static, bipolar-compatible types, operating without clocks on standard power supplies. Row and column access times are typically 450 and 700 ns respectively. An MM4240/MM5240 2560-bit ROM is used for the 5 x 7 horizontal-scan fonts and an MM4241/MM5241 3072-bit ROM for the 7 x 5 vertical-scan fonts. The MM4240 and MM4241 operate at −55°C to +125°C and the MM5240 and MM5241 at −25°C to +70°C.

Input-output configurations and character formats for the ROMs are shown in Figures 1 and 2. Application Note *AN-40 The Systems Approach to Character Generators* gives examples of line and column address-control logic, and CRT and printer operating techniques.

TYPE NUMBER	CODE	64-CHARACTER SUBSET	FIGURE
Horizontal Scan (5 x 7)			
MM4240AA/MM5240AA	ASCII	Upper-case alphanumeric	3
MM4240AE/MM5240AE	ASCII	Lower-case alpha and symbols	4
MM4240ABU/MM5240ABU	Hollerith	Upper-case alphanumeric	5
MM4240ABZ/MM5240ABZ	EBCDIC-8	Upper-case alphanumeric	6
MM4240ACA/MM5240ACA	EBCDIC	Upper-case alphanumeric (IBM)	7
Vertical Scan (7 x 5)			
MM4241ABL/MM5241ABL	ASCII	Upper-case alphanumeric	8
MM4241ABV/MM5241ABV	ECMA	Upper-case A/N, Scandinavian	9
MM4241ABW/MM5241ABW	ECMA	Upper-case A/N, German	10
MM4241ABX/MM5241ABX	ECMA	Upper-case A/N, general European (French, British, Italian)	11
MM4241ABY/MM5241ABY	ECMA	Upper-case A/N, Spanish	12

TABLE 1. Single-Chip, Standard Horizontal-Scan and Vertical-Scan Character Generators

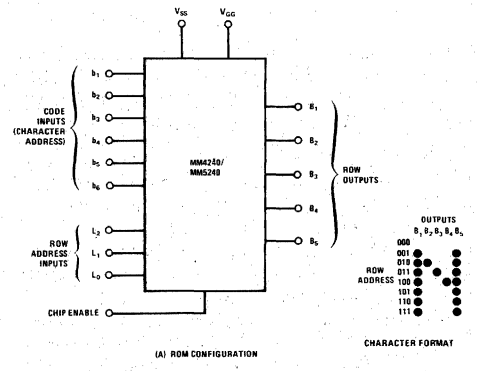


FIGURE 1. Horizontal-Scan Character Generator ROM

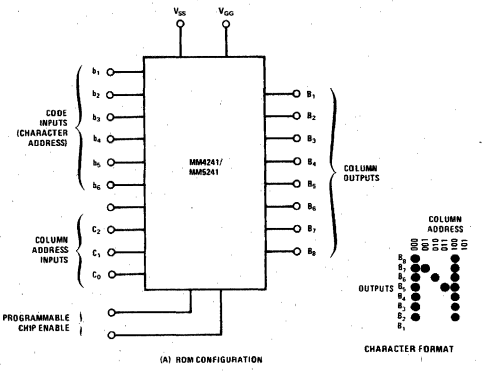


FIGURE 2. Vertical-Scan Character Generator ROM

Note that each ROM has a chip-enable input to permit multi-ROM operation with common control logic. For instance, two horizontal-scan ASCII character generators may be operated in tandem to obtain upper and lower-case characters. In this case, chip-enable would be controlled with bit b_6 of the normal 7-bit ASCII code, and its complement, $\overline{b_6}$.

HORIZONTAL SCAN FONTS

The subsets of 64 5 x 7 characters in the horizontal-scan fonts are the ones most commonly used in low-cost TV and CRT raster-scan displays and dot-matrix line printers.

MM4240AA/MM5240AA contains the ASCII-6 preferred graphic subset, formed from ASCII-7 by ignoring bit b_6. The remaining six bits form two octal address characters. One is formed by the three more significant bits, b_7, b_5 and b_4, and the second by b_3, b_2 and b_1.

Also, characters 36 and 37 in ASCII (x3.4 1968)* are respectively a carat (or circumflex), and an underscore. These are awkward in a video display, so they are replaced by the more useful arrows. (The arrows are related to characters in an older teletypewriter set.) This font, shown in Figure 3, is also described on the MM4240/MM5240 data sheet (which should be referred to for operating characteristics of all the horizontal-scan character generators).

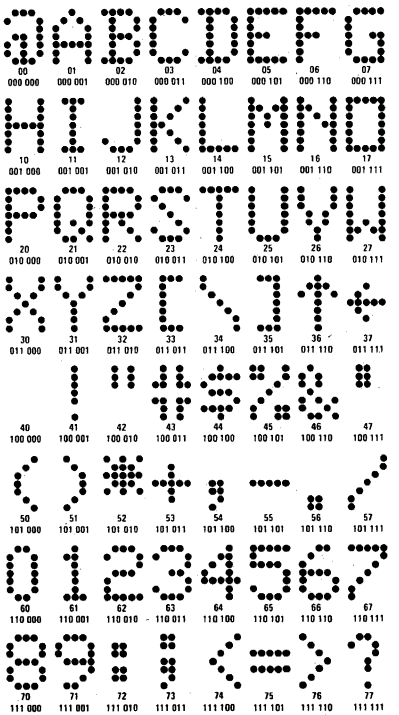


FIGURE 3. MM4240AA/MM5240AA Horizontal-Scan ASCII-7 Graphic Subset

MM4240AE/MM5240AE generates unique symbols describing the ASCII-7 control codes, as well as lower-case letters (Figure 4). The designer may not wish to display or dot-print the symbols. Since the symbols are generated only when the most significant address bit is logic "0", this bit line may be used to disable the chip, and blank the screen when control signals are transmitted. If not, the system designer can use the symbols as he likes.

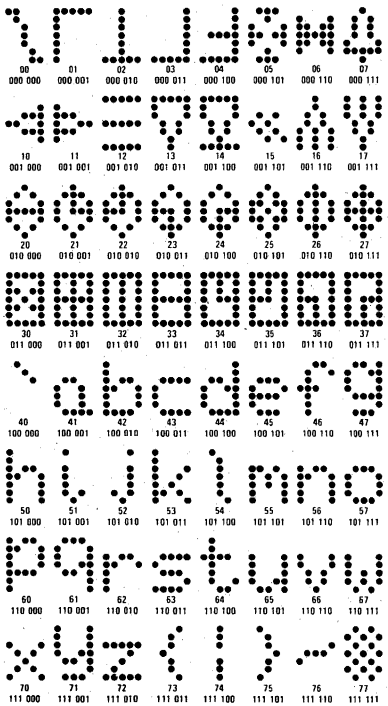


FIGURE 4. MM4240AE/MM5240AE Horizontal-Scan ASCII-7 Lower-Case Graphic and Control Symbol Subset

The Hollerith character subset in Figure 5b is formed by using six gates to compress the 12-line Hollerith code to the 6-bit address for 64 characters, as shown in Figure 5a

As shown in Figure 6, an ASCII-compatible subset is provided by the EBCDIC-8 character generator (MM4240ABZ/MM5240ABZ) by simply ignoring the two most significant bits, b_0 and b_1, in the EBCDIC-8 code. The ABZ version follows the ANSI standard, while the ACA version follows the IBM style. A cent sign, and IBM's logical OR and logic NOT signs are given by the ACA subset (characters 12, 17, and 37). And a plus or minus sign is provided, as character 52. (See Figure 7.)

*American National Standards Institute (ANSI)

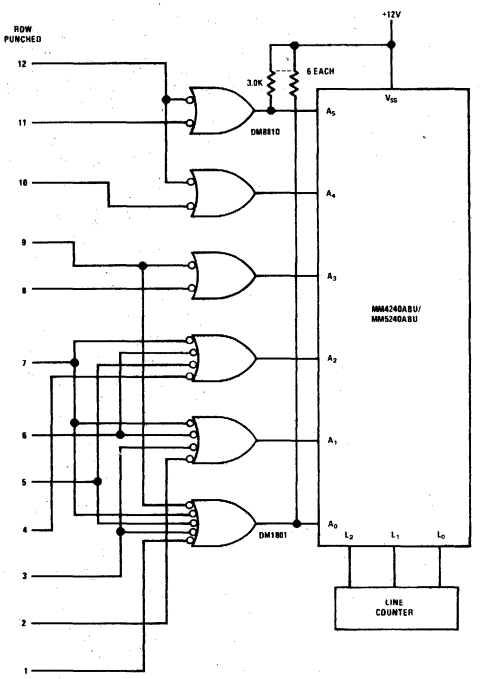


FIGURE 5a. MM4240ABU/MM5240ABU Typical Address Inputs

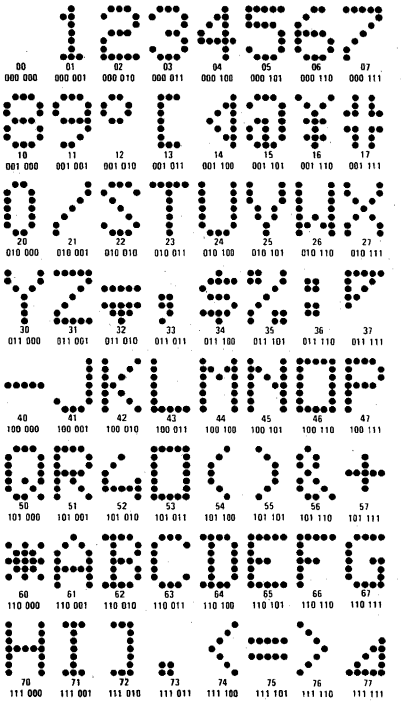


FIGURE 5b. MM4240ABU/MM5240ABU Horizontal Scan Hollerith Graphics Subset

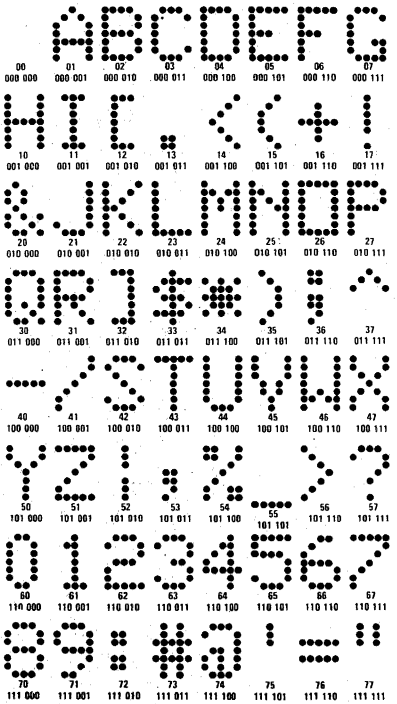


FIGURE 6. MM4240BABZ/MM5240BABZ Horizontal-Scan EBCDIC-8 Graphic Subset

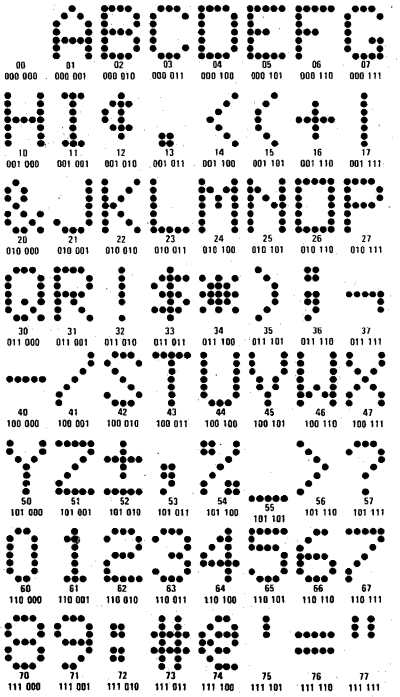


FIGURE 7. MM4240ACA/MM5240ACA Horizontal-Scan IBM EBCDIC Graphic Subset

VERTICAL SCAN FONTS

All five of the standard vertical-scan subsets in Figures 8 through 12 are generated with 6-bit codes derived from code recommendations R646 of the International Organization for Standardization. These recommendations cover ASCII-7, European ECMA-7 and CCITT alphabet number 5.

The ASCII subset for American use, in Figure 8, is practically identical to the horizontal-scan subset. Those in Figures 9 through 12 follow preferred character styles in the countries indicated. The underscore (character 37) is dropped below the line so that it may be used as a cursor.

Vertical-scan character generators are generally used in dot-matrix tape printers, ink-dot spray printers and high-definition sawtooth or pedestal-scan CRT displays. They may also be used to control raster-scan TV tubes or CRTs if the tube is turned on its side so that the raster scan is made vertically to provide a page-like format.

With standard programming, the bits in the column outputs are sequenced for a sawtooth scan with dot columns running in the same direction, as illustrated in Figure 13a. For a pedestal scan, Figure 13b, alternate columns can be reversed by putting an 8-bit shift left/shift right TTL shift register (DM74198) on the output as illustrated in Figure 14.

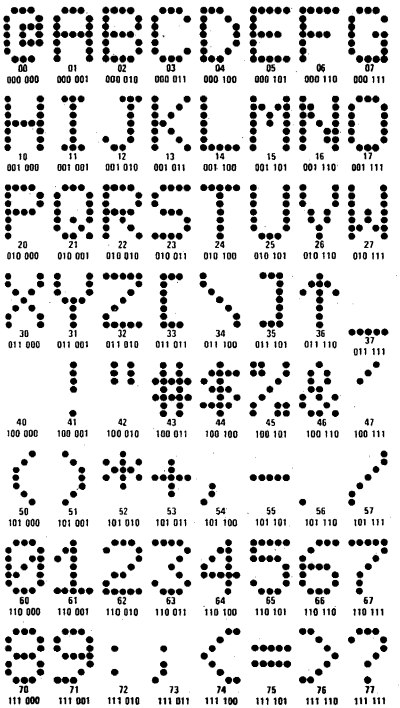


FIGURE 8. MM4241ABL/MM5241ABL Vertical-Scan ASCII-7 Graphic Subset

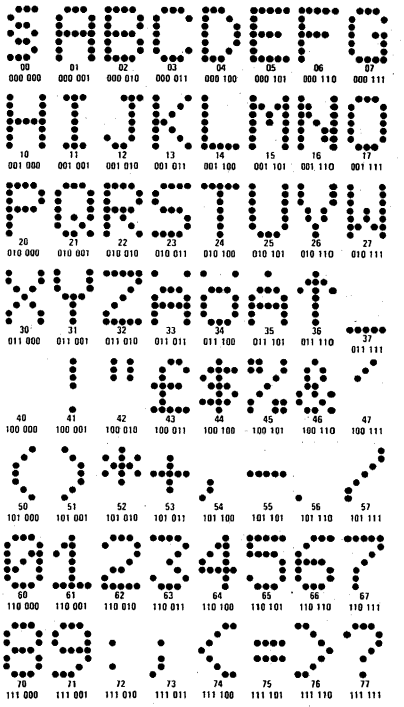


FIGURE 9. MM4241ABV/MM5241ABV Vertical Scan ECMA-7 Font for Scandinavian Use

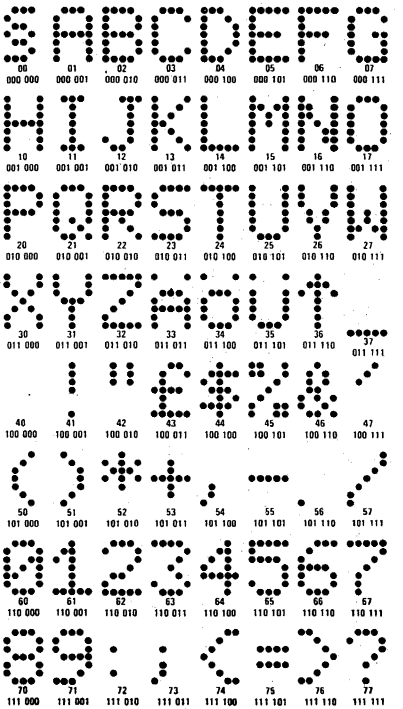


FIGURE 10. MM4241ABW/MM5241ABW Vertical-Scan ECMA-7 Font for German Use

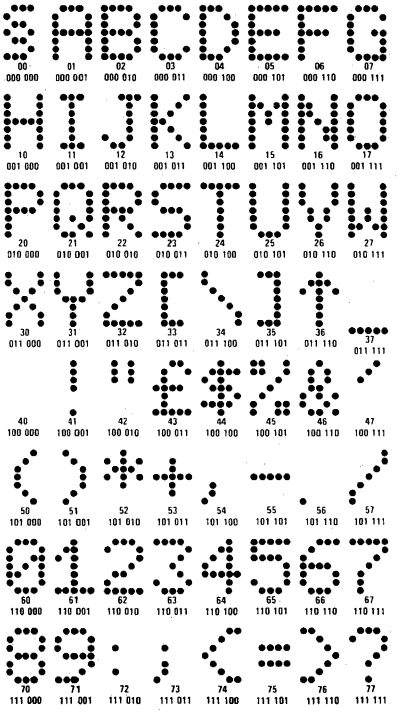


FIGURE 11. MM4241ABX/MM5241ABX Vertical-Scan ECMA-7 Font for General European Use (French, British, Italian)

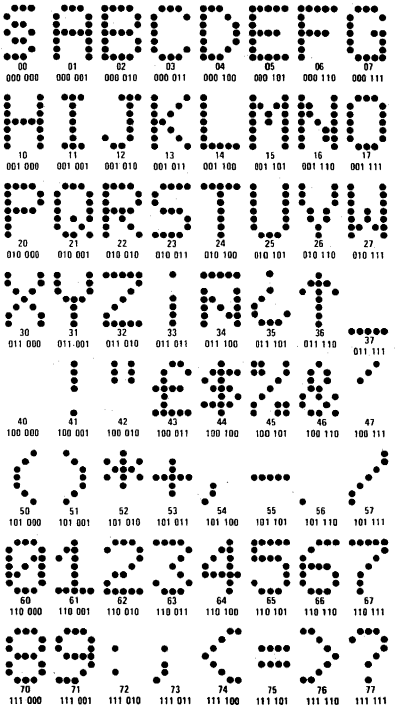


FIGURE 12. MM4241ABY/MM5241ABY Vertical-Scan ECMA-7 Font for Spanish Use

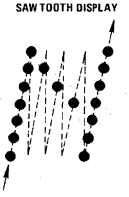


FIGURE 13a. Sawtooth Vertical Scan

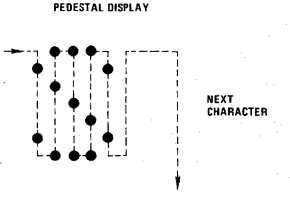


FIGURE 13b. Pedestal Vertical Scan

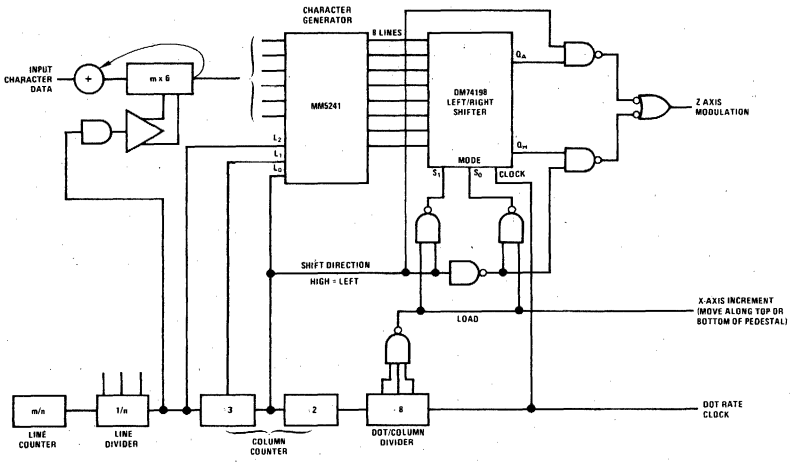


FIGURE 14. Conversion of Sawtooth Output to Pedestal Scan

CUSTOM FONTS

The two ROMs can also be custom-programmed to provide special characters, or fonts larger than 5 x 7. The MM4240/MM5240 actually stores 64 5 x 8 characters or character segments and the MM4241/MM5241 stores 64 8 x 6 characters or segments. They are not limited to 5 x 7 and 7 x 5. For example, the extra height may be used in an otherwise 5 x 7 font to drop the tails of commas, semicolons and lower-case letters below the bottom line of the capital letters. Fonts as large as 16 x 12 are entirely practical without additional control logic, using the chip-enable feature of four MM5241s. Large-font organizations are discussed in AN-40.

NATIONAL

APPLYING MODERN CLOCK DRIVERS TO MOS MEMORIES

INTRODUCTION

MOS memories present unique system and circuit challenges to the engineer since they require precise timing of input wave forms. Since these inputs present large capacitive loads to drive circuits, it is often that timing problems are not discovered until an entire system is constructed. This paper covers the practical aspects of using modern clock drivers in MOS memory systems. Information includes selection of packages and heat sinks, power dissipation, rise and fall time considerations, power supply decoupling, system clock line ringing and crosstalk, input coupling techniques, and example calculations. Applications covered include driving various types shift registers and RAM's (Random Access Memories) using logical control as well as other techniques to assure correct non-overlap of timing waveforms.

Although the information given is generally applicable to any type of driver, monolithic integrated circuit drivers, the DS0025, DS0026 and DS0056 are selected as examples because of their low cost.

The DS0025 was the first monolithic clock driver. It is intended for applications up to one megacycle where low cost is of prime concern. Table I illustrates its performance while Appendix I describes its circuit operation. Its monolithic, rather than hybrid or module construction, was made possible by a new high voltage-gold doped process utilizing a collector sinker to minimize $V_{CE\,SAT}$.

The DS0026 is a high speed, low cost, monolithic clock driver intended for applications above one megacycle. Table II illustrates its performance characteristics while its unique circuit design is presented in Appendix II. The DS0056 is a variation of the DS0026 circuit which allows the system designer to modify the output performance of the circuit. The DS0056 can be connected (using a second power supply) to increase the positive output voltage level and reduce the effect of cross coupling capacitance between the clock lines in the system. Of course the above are just examples of the many different types that are commercially available. Other National Semiconductor MOS interface circuits are listed in Appendix III.

The following section will hopefully allow the design engineer to select and apply the best circuit to his particular application while avoiding common system problems.

PRACTICAL ASPECTS OF USING MOS CLOCK DRIVERS

Package and Heat Sink Selection

Package type should be selected on power handling capability, standard size, ease of handling, availability of sockets, ease or type of heat sinking required, reliability and cost. Power handling capability for various packages is illustrated in Table III. The following guidelines are recommended:

TABLE I. DS0025 Characteristics

PARAMETER	CONDITIONS ($V^+ - V^-$) = 17V	VALUE	UNITS
t_{ON}		15	ns
t_{OFF}	C_{IN} = 0.0022μF, R_{IN} = 0Ω	30	ns
t_r	C_L = 0.0001μF, RO = 50Ω	25	ns
t_f		150	ns
Positive Output Voltage Swing	$V_{IN} - V^-$ = 0V, I_{OUT} = -1mA	$V^+ - 0.7$	V
Negative Output Voltage Swing	I_{IN} = 10mA, I_{OUT} = 1mA	$V^- + 1.0$	V
On Supply Current (V^+)	I_{IN} = 10 mA	17	mA

TABLE II. DS0026 Characteristics

PARAMETER	CONDITIONS ($V^+ - V^-$) = 17V	VALUE	UNITS
t_{ON}		7.5	ns
t_{OFF}	C_{IN} = 0.001μF, R_{IN} = 0Ω	7.5	ns
t_r	RO = 50Ω, C_L = 1000 pF	25	ns
t_f		25	ns
Positive Output Voltage Swing	$V_{IN} - V^-$ = 0V, I_{OUT} = -1mA	$V^+ - 0.7$	V
Negative Output Voltage Swing	I_{IN} = 10mA, I_{OUT} = 1mA	$V^- + 0.5$	V
On Supply Current (V^+)	I_{IN} = 10 mA	28	mA

The TO-5 ("H") package is rated at 750 mW still air (derate at 200°C/W above 25°C) soldered to PC board. This popular cavity package is recommended for small systems. Low cost (about 10 cents) clip-on heat sink increases driving capability by 50%.

The 8-pin ("N") molded mini-DIP is rated at 600 mW still air (derate at 90°C/W above 25°C) soldered to PC board (derate at 1.39W). Constructed with a special copper lead frame, this package is recommended for medium size commercial systems particularly where automatic insertion is used. (Please note for prototype work, that this package is only rated at 600 mW when mounted in a socket and not one watt until it is soldered down.)

To TO-8 ("G") package is rated at 1.5W still air (derate at 100°C/W above 25°C) and 2.3W with clip-on heat sink (Wakefield type 215-1.9 or equivalent-derate at 15 mW/°C). Selected for its power handling capability and moderate cost, this hermetic package will drive very large systems at the lowest cost per bit.

Additional information is given in the section of this data book on Maximum Power Dissipation (page 2).

Power Dissipation Considerations

The amount of registers that can be driven by a given clock driver is usually limited first by internal power dissipation. There are four factors:

1. Package and heat sink selection
2. Average dc power, P_{DC}
3. Average ac power, P_{AC}
4. Numbers of drivers per package, n

From the package heat sink, and maximum ambient temperature one can determine P_{MAX}, which is the maximum internal power a device can handle and still operate reliably. The total average power dissipated in a driver is the sum of dc power and ac power in each driver times the number of drivers. The total of which must be less than the package power rating.

$$P_{DISS} = n \times (P_{AC} + P_{DC}) \leq P_{MAX} \qquad (1)$$

Average dc power has three components: input power, power in the "OFF" state (MOS logic "0") and power in the "ON" state (MOS logic "1").

$$P_{DC} = P_{IN} + P_{OFF} + P_{ON} \qquad (2)$$

For most types of clock drivers, the first two terms are negligible (less than 10 mW) and may be ignored.

Thus:

$$P_{DC} \cong P_{ON} = \frac{(V^+ - V^-)^2}{Req} \times (DC)$$

where:

$V^+ - V^-$ = Total voltage across the driver

Req = Equivalent device resistance in the "ON" state

$$= V^+ - V^-/I_{S(ON)} \qquad (3)$$

DC = Duty Cycle

$$= \frac{\text{"ON" Time}}{\text{"ON" Time + "OFF" Time}}$$

For the DS0025, Req is typically 1 kΩ while Req is typically 600Ω for the DS0026. Graphical solutions for P_{DC} appear in *Figure 1.* For example if V^+ = +5V, V^- = −12V, Req = 500 Ω, and DC = 25%, then P_{DC} = 145 mW. However, if the duty cycle was only 5%, P_{DC} = 29 mW. Thus to maximize the number of registers that can be driven by a given clock driver as well as minimizing average system power, the minimum allowable clock pulse width should be used for the particular type of MOS register.

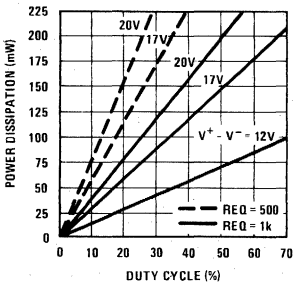


FIGURE 1. P_{DC} vs Duty Cycle

In addition to P_{DC}, the power driving a capacitive load is given approximately by:

$$P_{AC} = (V^+ - V^-)^2 \times f \times C_L \qquad (4)$$

where:

f = Operating frequency

C_L = Load capacitance

Graphical solutions for P_{AC} are illustrated in *Figure 2.* Thus, any type of clock driver will dissipate internally 290 mW per MHz per thousand pF of load. At 5 MHz, this would be 1.5W for a 1000 pF load. For long shift register applications, the driver with the highest package power rating will drive the largest number of bits.

Combining equations (1), (2), (3) and (4) yields a criterion for the maximum load capacitance which can be driven by a given driver:

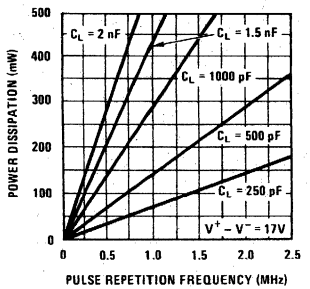


FIGURE 2. P_{AC} vs PRF

$$C_L \leq \frac{1}{f}\left[\frac{P_{MAX}}{n\,(V^+ - V^-)^2} - \frac{(DC)}{Req}\right] \qquad (5)$$

As an example, the DS0025CN can dissipate 890 mW at T_A = 70°C when soldered to a printed circuit board. Req is approximately equal to 1k. For V^+ = 5V, V^- = −12V, f = 1 MHz, and dc = 20%, C_L is:

$$C_L \leq \frac{1}{10^6}\left[\frac{(890 \times 10^{-3})}{(2)\,(17)^2} - \frac{0.2}{1 \times 10^3}\right]$$

$$C_L \leq 1340\ \text{pF (each driver)}$$

A typical application might involve driving an MM5013 triple 64-bit shift register with the DS0025. Using the conditions above and the clock line capacitance of the MM5013 of 60 pF, a single DS0025 can drive 1340 pF/60 pF, or 00 MM5013's.

In summary, the maximum capacitive load that any clock driver can drive is determined by package type and rating, heat sink technique, maximum system ambient temperature, ac power (which depends on frequency, voltage across the device, and capacitive load) and dc power (which is principally determined by duty cycle).

Rise and Fall Time Considerations

In general rise and fall times are determined by (a) clock driver design, (b) reflected effects of heavy external load, and (C) peak transient current available. Details of these are included in Appendixes I and II. *Figures AI-3, AI-4, AII-2 and AIII-3* illustrate performance under various operating conditions. Under light loads, performance is determined by internal design of the driver; for moderate loads, by load C_L being reflected (usually as $C_{L/\beta}$) into the driver, and for large loads by peak output current where:

$$\frac{\Delta V}{\Delta T} = \frac{I_{OUT\ PEAK}}{C_L}$$

Logic rise and fall times must be known in order to assure non-overlap of system timing.

Note the definition of rise and fall times in this application note follow the convention that rise time is the transition from logic "0" to logic "1" levels and vice versa for fall times. Since MOS logic is inverted from normal TTL, "rise time" as used in this note is "voltage fall" and "fall time" is "voltage rise."

Power Supply Decoupling

Although power supply decoupling is a wide spread and accepted practice, the question often arises as to how much and how often. Our own experience indicates that each clock driver should have at least 0.1μF decoupling to ground at the V^+ and V^- supply leads. Capacitors should be located as close as is physically possible to each driver. Capacitors should be non-inductive ceramic discs. This decoupling is necessary because currents in the order of 0.5 to 1.5 amperes flow during logic transitions.

There is a high current transient (as high as 1.5A) during the output transition from high to low through the V^- lead. If the external interconnecting wire from the driving circuit to the V^- lead is electrically long, or has significant dc resistance the current transient will appear as negative feedback and subtract from the switching response. To minimize this effect, short interconnecting wires are necessary and high frequency power supply decoupling capacitors are required if V^- is different from the ground of the driving circuit.

Clock Line Overshoot and Cross Talk

Overshoot: The output waveform of a clock driver can, and often does, overshoot. It is particularly evident on faster drivers. The overshoot is due to the finite inductance of the clock lines. Since most MOS registers require that clock signals not exceed V_{SS}, some method must be found in large systems to eliminate overshoot. A straightforward approach is shown in *Figure 3.* In this instance,

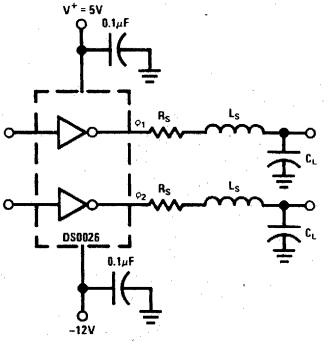


FIGURE 3. Use of Damping Resistor to Eliminate Clock Overshoot

a small damping resistor is inserted between the output of the clock driver and the load. The critical value for R_S is given by:

$$R_S = 2\sqrt{\frac{L_S}{C_L}} \qquad (6)$$

In practice, analytical determination of the value for R_S is rather difficult. However, R_S is readily determined empirically, and typical values range in value between 10 and 50Ω.

Use of the damping resistor has the added benefit of essentially unloading the clock driver; hence a greater number of loads may often be driven by a given driver. In the limit, however, the maximum value that may be used for R_S will be determined by the maximum allowable rise and fall time needed to assure proper operation of the MOS register. In short:

$$t_{r(MAX)} = t_{f(MAX)} \leq 2.2\ R_S\ C_L \qquad (7)$$

One last word of caution with regard to use of a damping resistor should be mentioned. The power dissipated in R_S can approach $(V^+ - V^-)^2 f C_L$ and accordingly the resistor wattage rating may be in excess of 1W. There are, obviously, applications where degradation of t_r and t_f by use of damping resistors cannot be tolerated. *Figure 4* shows a practical circuit which will limit overshoot to a diode drop. The clamp network should physically be located in the center of the distributed load in order to minimize inductance between the clamp and registers.

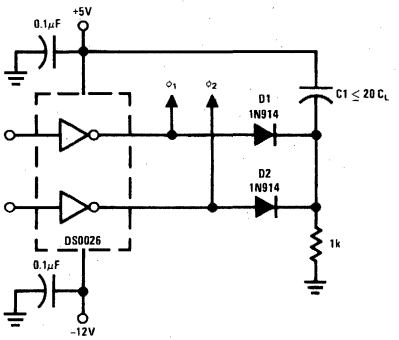


FIGURE 4. Use of High Speed Clamp to Limit Clock Overshoot

Cross Talk: Voltage spikes from ϕ_1 may be transmitted to ϕ_2 (and vice versa) during the transition of ϕ_1 to MOS logic "1." The spike is due to mutual capacitance between clock lines and is, in general, aggravated by long clock lines when numerous registers are being driven. *Figure 5* illustrates the problem.

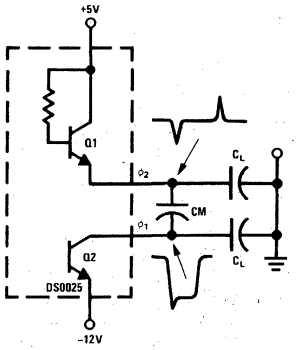


FIGURE 5. Clock Line Cross Talk

The negative going transition of ϕ_1 (to MOS logic "1") is capacitively coupled via C_M to ϕ_2. Obviously, the larger C_M is, the larger the spike. Prior to ϕ_1's transition, Q1 is "OFF" since only μA are drawn from the device.

The DS0056 connected as shown in *Figure 6* will minimize the effect of cross talk. The external resistors to the higher power supply pull the base of a Q1 up to a higher level and forward bias the collector base junction of Q1. In this bias condition the output impedance of the DS0056 is very low and will reduce the amplitude of the spikes.

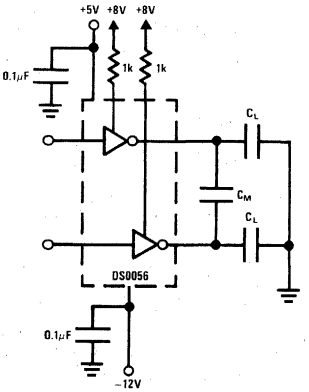


FIGURE 6. Use of DS0056 to Minimize Clock Line Cross Talk

Input Capacitive Coupling

Generally, MOS shift registers are powered from +5V and −12V supplies. A level shift from the TTL levels (+5V) to MOS levels (−12V) is therefore required. The level shift could be made utilizing a PNP transistor or zener diode. The disadvantage to dc level shifting is the increased power dissipation and propagation delay in the level shifting device. Both the DS0025, DS0026 and DS0056 utilize input capacitors when level shifting from

TTL to negative MOS capacitors. Not only do the capacitors perform the level shift function without inherent delay and power dissipation, but as will be shown later, the capacitors also enhance the performance of these circuits.

CONCLUSION

The practical aspects of driving MOS memories with low cost clock drivers has been discussed in detail. When the design guide lines set forth in this paper are followed and reasonable care is taken in circuit layout, the DS0025, DS0026 and DS0056 provide superior performance for most MOS input interface applications.

REFERENCES

1. Bert Mitchell, *"New MOS Clock Driver for MOS Shift Registers,"* National Semiconductor, AN-18, March 1969.
2. John Vennard, *"MOS Clock Drivers,"* National Semiconductor, MB-9, December 1969.
3. Dale Mrazek, *"MOS Delay Lines,"* National Semiconductor, AN-25, April 1969.
4. Dale Mrazek, *"MOS Clock Savers,"* National Semiconductor, MB-5.
5. Dale Mrazek, *"Silicon Disc's Challenge Magnetic Disc Memories,"* EDN/EEE Magazine, Sept. 1971.
6. Richard Percival, *"Dynamic MOS Shift Registers Can Also Simulate Stack and Silo Memories,"* Electronics Magazine, November 8, 1971.
7. Bapat and Mrazek, *"Dynamic MOS Random Access Memory System Considerations,"* National Semiconductor, AN-50, August 1971.
8. Don Femling, *"Using the MM5704 Keyboard Interface in Keyboard Systems,"* National Semiconductor, AN-52.

APPENDIX I

DS0025 Circuit Operation

The schematic diagram of the DS0025 is shown in *Figure AI-1.* With the TTL driver in the logic "0" state Q1 is "OFF" and Q2 is "ON" and the output is at approximately one V_{BE} below the V^+ supply.

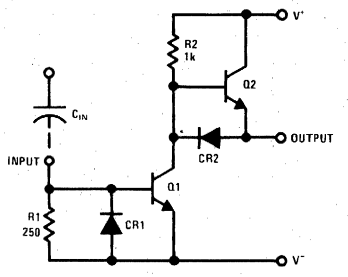


FIGURE AI-1. DS0026 Schematic (One-Half Circuit)

When the output of the TTL driver goes high, current is supplied to the base of Q1, through C_{IN}, turning it "ON." As the collector of Q1 goes negative, Q2 turns "OFF." Diode CR2 assures turn-on of Q1 prior to Q2's turn-off minimizing current spiking on the V^+ line, as well as providing a low impedance path around Q2's base emitter junction.

The negative voltage transition (to MOS logic "1") will be quite linear since the capacitive load will force Q1 into its linear region until the load is discharged and Q1 saturates. Turn-off begins when the input current decays to zero or the output of the TTL driver goes low. Q1 turns "OFF" and Q2 turns "ON" charging the load to within a V_{BE} of the V^+ supply.

Rise Time Considerations

The logic rise time (voltage fall) of the DS0025 is primarily a function of the ac load, C_L, the available input current and total voltage swing. As shown in *Figure AI-2,*

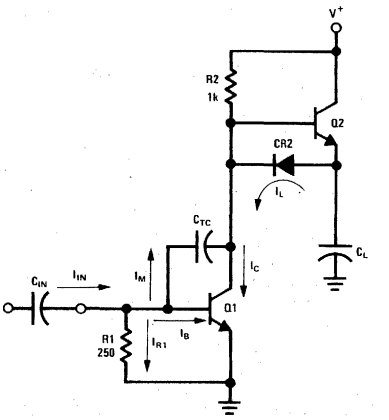


FIGURE AI-2. Rise Time Model for the DS0025

the input current must charge the Miller capacitance of Q1, C_{TC}, as well as supply sufficient base drive to Q1 to discharge C_L rapidly. By inspection:

$$I_{IN} = I_M + I_B + I_{R1} \qquad \text{(AI-1)}$$

$$I_{IN} \cong I_M + I_B, \text{ for } I_M >> I_{R1} \text{ \& } I_B >> I_{R1}$$

$$I_B = I_{IN} - C_{TC}\frac{\Delta V}{\Delta t} \qquad \text{(AI-2)}$$

If the current through R2 is ignored,

$$I_C = I_B h_{FEQ1} = I_L + I_M \qquad \text{(AI-3)}$$

where:

$$I_L = C_L\frac{\Delta V}{\Delta t}$$

Combining equations AI-1, AI-2, AI-3 yields:

$$\frac{\Delta V}{\Delta t}[C_L + C_{TC}(h_{FEQ1} + 1)] = h_{FEQ1} I_{IN} \qquad \text{(AI-4)}$$

or

$$t_r \cong \frac{[C_L + (h_{FEQ1} + 1)C_{TC}]\,\Delta V}{h_{FEQ1} I_{IN}} \qquad \text{(AI-5)}$$

Equation (AI-5) may be used to predict t_r as a function of C_L and ΔV. Values for C_{TC} and h_{FE} are 10 pF and 25 respectively. For example, if a DM7440 with peak output current of 50 mA were used to drive a DS0025 loaded with 1000 pF, rise times of:

$$\frac{(1000\text{ pF} + 250\text{ pF})\,(17\text{V})}{(50\text{ mA})\,(20)}$$

or 21 ns may be expected for $V^+ = 5.0$V, $V^- = -12$V, *Figure AI-3* gives rise time for various values of C_L.

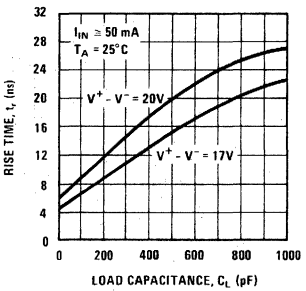


FIGURE AI-3. Rise Time vs C_L for the DS0025

Fall Time Considerations

The MOS logic fall time (voltage rise) of the DS0025 is dictated by the load, C_L, and the output capacitance of Q1. The fall time equivalent circuit of DS0025 may be approximated with the circuit of *Figure AI-4.* In actual

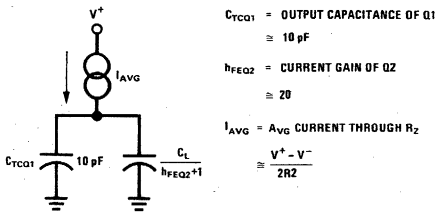


FIGURE AI-4. Fall Time Equivalent Circuit

practice, the base drive to Q2 drops as the output voltage rises toward V^+. A rounding of the waveform occurs as the output voltage reaches to within a volt of V^+. The result is that equation (AI-7) predicts conservative values of t_f for the output voltage at the beginning of the voltage rise and optimistic values at the end. *Figure AI-5* shows t_f as function of C_L.

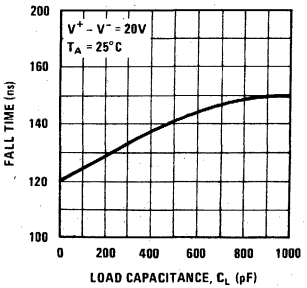


FIGURE AI-5. DS0025 Fall Time vs C_L

Assuming h_{FE2} is a constant of the total transition:

$$\frac{\Delta V}{\Delta t} = \frac{\left(\frac{V^+ - V^-}{2R2}\right)}{C_{TCQ1} + C_L/h_{FEQ1+1}} \qquad \text{(AI-6)}$$

or

$$t_f \cong 2R2\left(C_{TCQ1} + \frac{C_L}{h_{FEQ+1}}\right) \qquad \text{(AI-7)}$$

DS0025 Input Drive Requirements

Since the DS0025 is generally capacitively coupled at the input, the device is sensitive to current not input voltage. The current required by the input is in the 50–60 mA region. It is therefore a good idea to drive the DS0025 from TTL line drivers, such as the DM7440 or DM8830. It is possible to drive the DS0025 from standard 54/74 series gates or flip-flops but t_{ON} and t_r will be somewhat degraded.

Input Capacitor Selection

The DS0025 may be operated in either the logically controlled mode (pulse width out ≅ pulse width in) or C_{IN} may be used to set the output pulse width. In the latter mode a long pulse is supplied to the DS0025.

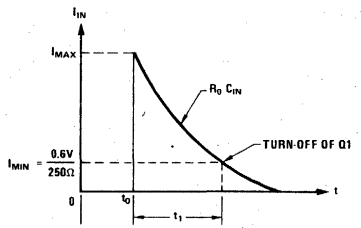


FIGURE AI-6. DS0025 Input Current Waveform

The input current is of the general shape as shown in *Figure AI-6*. I_{MAX} is the peak current delivered by the TTL driver into a short circuit (typically 50–60 mA). Q1 will begin to turn-off when I_{IN} decays below V_{BE}/R1 or about 2.5 mA. In general:

$$I_{IN} = I_{MAX}\, e^{-t/R0}\, C_{IN} \qquad \text{(AI-8)}$$

where:

R0 = Output impedance of the TTL driver

C_{IN} = Input coupling capacitor

Substituting $I_{IN} = I_{MIN} = \dfrac{V_{BE}}{R1}$ and solving for t_1 yields:

$$t_1 = R0C_{IN}\ \ln \frac{I_{MAX}}{I_{MIN}} \qquad \text{(AI-9)}$$

The total pulse width must include rise and fall time considerations. Therefore, the total expression for pulse width becomes:

$$t_{PW} \cong \frac{t_r + t_f}{2} + t_1$$

$$= \frac{t_r + t_f}{2} + R0C_{IN}\ \ln \frac{I_{MAX}}{I_{MIN}} \qquad \text{(AI-10)}$$

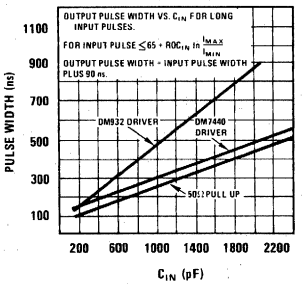


FIGURE AI-7. Output PW Controlled by C_{IN}

The logic "1" output impedance of the DM7440 is approximately 65Ω and the peak current (I_{MAX}) is about 50 mA. The pulse width for C_{IN} = 2,200 pF is:

$$t_{PW} \cong \frac{25\text{ ns} + 150\text{ ns}}{2} + (65\Omega)(2200\text{ pF})\ \ln$$

$$\frac{50\text{ mA}}{2.5\text{ mA}} = 517\text{ ns}$$

A plot of pulse width for various types of drivers is shown in *Figure AI-7*. For applications in which the output pulse width is logically controlled, C_{IN} should be chosen 2 to 3 times larger than the maximum pulse width dictated by equation (AI-10).

DC Coupled Operation

The DS0025 may be direct-coupled in applications when level shifting to a positive value only. For example, the MM1103 RAM typically operates between ground and +20V. The DS0025 is shown in *Figure AI-8* driving the addres or precharge line in the logically controlled mode.

If DC operation to a negative level is desired, a level translator such as the DS7800 or DS0034 may be employed as shown in *Figure AI-9*. Finally, the level shift may be accomplished using PNP transistors are shown in *Figure AI-10*.

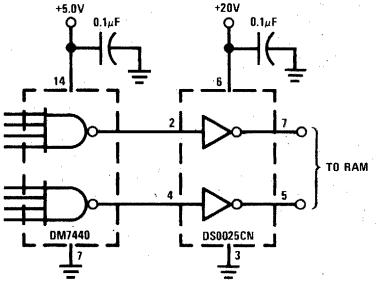


FIGURE AI-8. DC Coupled DS0025 Driving 1103 RAM

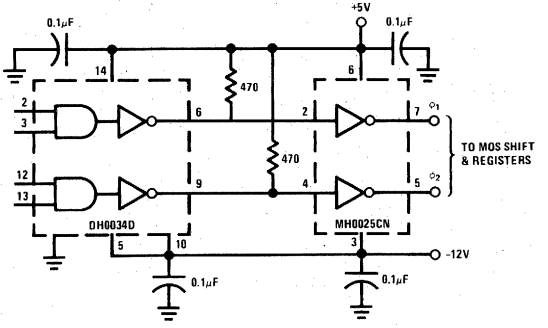


FIGURE AI-9. DC Coupled Clock Driver Using DS0034

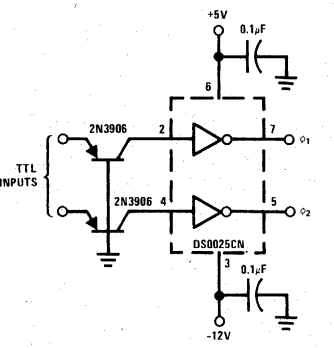


FIGURE AI-10. Transistor Coupled DS0025 Clock Driver

APPENDIX II

DS0026 Circuit Operation

The schematic of the DS0026 is shown in *Figure AII-1*. The device is typically ac coupled on the input and responds to input current as does the DS0025. Internal current gain allows the device to be driven by standard TTL gates and flip-flops.

With the TTL input in the low state Q1, Q2, Q5, Q6 and Q7 are "OFF" allowing Q3 and Q4 to come "ON." R6 assures that the output will pull up to within a V_{BE} of V^+ volts. When the TTL input starts toward logic "1," current is supplied via C_{IN} to the bases of Q1 and Q2 turning them "ON." Simultaneously, Q3 and Q4 are snapped "OFF." As the input voltage rises (to about 1.2V), Q5 and Q6 turn-on. Multiple emitter transistor Q5 provides additional base drive to Q1 and Q2 assuring their complete and rapid turn-on. Since Q3 and Q4 were rapidly turned "OFF" minimal power supply current spiking will occur when Q7 comes "ON."

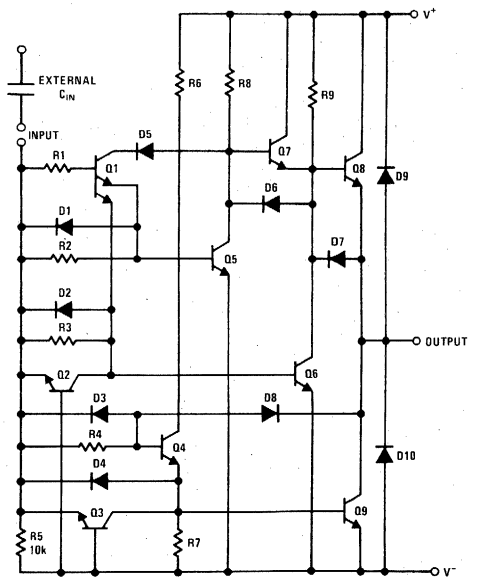


FIGURE AII-1. DS0025 Schematic (One-Half Circuit)

Q6 now provides sufficient base drive to Q7 to turn it "ON." The load capacitance is then rapidly discharged toward V^-. Diode D4 affords a low impedance path to Q6's collector which provides additional drive to the load through current gain of Q7. Diodes D1 and D2 prevent avalanching Q3's and Q4's base-emitter junction as the collectors of Q1 and Q2 go negative. The output of the DS0026 continues negative stopping about 0.5V more positive than V^-.

When the TTL input returns to logic "0," the input voltage to the DS0026 goes negative by an amount proportional to the charge on C_{IN}. Transistors Q8 and Q9 turn-on, pulling stored base charge out of Q7 and Q2 assuring their rapid turn-off. With Q1, Q2, Q6 and Q7 "OFF," Darlington connected Q3 and Q4 turn-on and rapidly charge the load to within a V_{BE} of V^+.

Rise Time Considerations

Predicting the MOS logic rise time (voltage fall) of the DS0026 is considerably involved, but a reasonable approximation may be made by utilizing equation (AI-5), which reduces to:

$$t_r \cong [C_L + 250 \times 10^{-12}]\ \Delta V \qquad \text{(AII-1)}$$

For C_L = 1000 pF, V^+ = 5.0V, V^- = −12V, $t_r \cong$ 21 ns. *Figure AII-2* shows DS0026 rise times vs C_L.

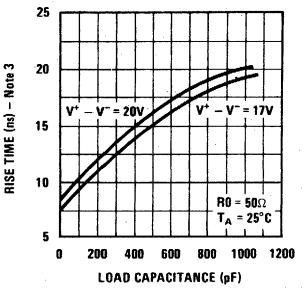


FIGURE AII-2. Rise Time vs Load Capacitance

Fall Time Considerations

The MOS logic fall time of the DS0026 is determined primarily by the capacitance Miller capacitance of Q5 and Q1 and R5. The fall time may be predicted by:

$$t_f \cong (2.2)(R5)\left(C_S + \frac{C_L}{h_{FE}{}^2}\right)$$

$$\cong (4.4 \times 10^3)\left(C_S + \frac{C_L}{h_{FE}{}^2}\right) \qquad \text{(AII-2)}$$

where:

C_S = Capacitance to ground seen at the base of Q3

= 2 pF

$h_{FE}{}^2 = (h_{FEQ3} + 1)(h_{FEQ4} + 1)$

$\cong$ 500

For the values given and C_L = 1000 pF, $t_f \cong$ 17.5 ns. *Figure AII-3* gives t_f for various values of C_L.

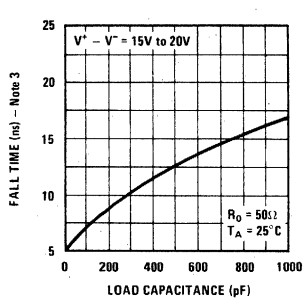


FIGURE AII-3. Fall Time vs Load Capacitance

DS0026 Input Drive Requirements

The DS0026 was designed to be driven by standard 54/74 elements. The device's input characteristics are shown in *Figure AII-4*. There is breakpoint at $V_{IN} \cong 0.6V$ which corresponds to turn-on of Q1 and Q2. The input current then rises with a slope of about 600Ω (R2 || R3) until a second breakpoint at approximately 1.2V is encountered, corresponding to the turn-on of Q5 and Q6. The slope at this point is about 150Ω (R1 || R2 || R3 || R4).

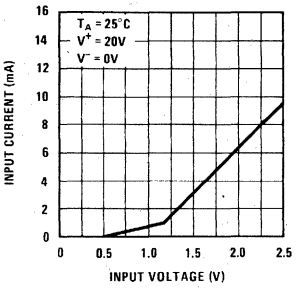


FIGURE AII-4. Input Current vs Input Voltage

The current demanded by the input is in the 5–10 mA region. A standard 54/74 gate can source currents in excess of 20 mA into 1.2V. Obviously, the minimum "1" output voltage of 2.5V under these conditions cannot be maintained. This means that a 54/74 element must be dedicated to driving 1/2 of a DS0026. As far as the DS0026 is concerned, the current is the determining turn-on mechanism not the voltage output level of the 54/74 gate.

Input Capacitor Selection

A major difference between the DS0025 and DS0026 is that the DS0026 requires that the output pulse width be logically controlled. In short, the input pulse width ≅ output pulse width. Selection of C_{IN} boils down to choosing a capacitor small enough to assure the capacitor takes on nearly full charge, but large enough so that the input current does not drop below a minimum level to keep the DS0026 "ON." As before:

$$t_1 = R0C_{IN} \ln \frac{I_{MAX}}{I_{MIN}} \qquad \text{(AII-3)}$$

or

$$C_{IN} = \frac{t_1}{R0 \ln \frac{I_{MAX}}{I_{MIN}}} \qquad \text{(AII-4)}$$

In this case R0 equals the sum of the TTL gate output impedance plus the input impedance of the DS0026 (about 150Ω). I_{MIN} from *Figure AII-5* is about 1 mA. A standard 54/74 series gate has a high state output impedance of about 150Ω in the logic "1" state and an output (short circuit) current of about 20 mA into 1.2V. For an output pulse width of 500 ns,

$$C_{IN} = \frac{500 \times 10^{-9}}{(150\Omega + 150\Omega) \ln \frac{20\text{ mA}}{1\text{ mA}}} = 560\text{ pF}$$

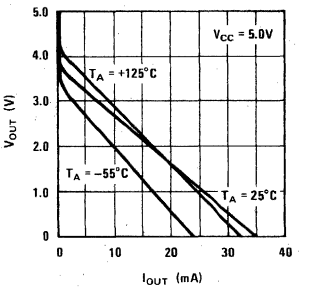


FIGURE AII-5. Logical "1" Output Voltage vs Source Current

In actual practice it's a good idea to use values of about twice those predicted by equation (AII-4) in order to account for manufacturing tolerances in the gate, DS0026 and temperature variations.

A plot of optimum value for C_{IN} vs desired output pulse width is shown in *Figure AII-6*.

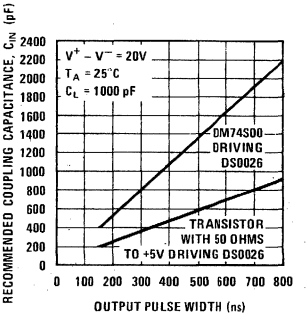


FIGURE AII-6. Suggested Input Capacitance vs Output Pulse Width

DC Coupled Applications

The DS0026 may be applied in direct coupled applications. *Figure AII-7* shows the device driving address or pre-charge lines on an MM1103 RAM.

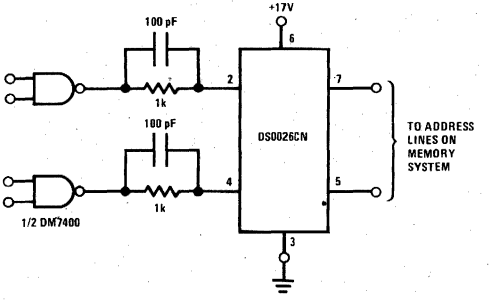


FIGURE AII-7. DC Coupled RAM Memory Address or Precharge Driver (Positive Supply Only)

For applications requiring a dc level shift, the circuit of *Figure AII-8 or AII-9* are recommended.

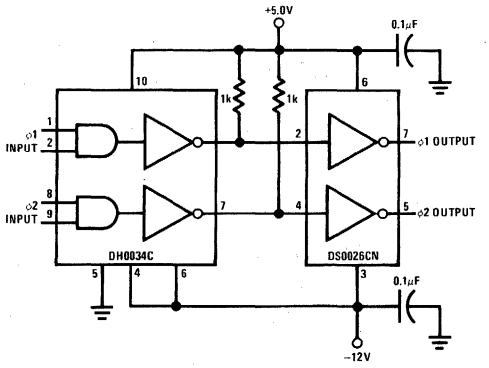


FIGURE AII-8. Transistor Coupled MOS Clock Driver

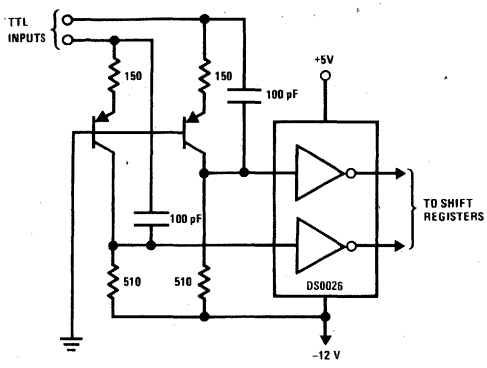


FIGURE AII-9. DC Coupled MOS Clock Driver

APPENDIX III

MOS Interface Circuits

MOS Clock Drivers

MH0007	Direct coupled, single phase, TTL compatible clock driver.
MH0009	Two phase, direct or ac coupled clock driver.
MH0012	10 MHz, single phase direct coupled clock driver.
MH0013	Two phase, ac coupled clock driver.
DS0025	Low cost, two phase clock driver.
DS0026	Low cost, two phase, high speed clock driver.
DS1671	Dual bootstrapped MOS driver.
DS1672	Dual TTL bootstrapped MOS driver.
DS1673	Quad decoded MOS clock driver.
DS1674	Quad MOS clock driver.
DS75361	Dual TTL-to-MOS driver.
DS75365	Quad TTL-to-MOS driver.

MOS Oscillator/Clock Drivers

DS7803/DS7807, DS7813/DS7817	Complete two phase clock system for MOS microprocessors and calculators.

MOS RAM Memory Address and Precharge Drivers

DS0025	Dual address and precharge driver.
DS0026	Dual high speed address and precharge driver.

TTL to MOS Interface

DH0034	Dual high speed TTL to negative level converter.
DS7800	Dual TTL to negative level converter.
DM7810/DM7812/ DM7819	Open collector TTL to positive high level MOS converter gates.
DM78L12	Active pull-up TTL to positive high level MOS converter gates.
DS1640/DS1670	Quad MOS TRI-SHARE™ driver.
DS1645/DS1675	Hex TRI-STATE® MOS driver.
DS1646/DS1676	6-bit TRI-STATE MOS driver refresh counter.
DS1647/DS1677	Quad TRI-STATE MOS driver I/O register.
DS1648/DS1678	TRI-STATE MOS driver multiplexer.
DS1649/DS1679	Hex TRI-STATE MOS driver.
DS16149/DS16179	Hex TRI-STATE MOS driver.

MOS to TTL Converters and Sense Amps

DS7802, DS7806*	Dual sense amp for MM5262 2k MOS RAM memory.
DS165 Series*	Hex sense amp MOS to TTL.
DS163, DS75107, DS75207*	Dual sense amp for MM1103 1k MOS RAM memory.

Voltage Regulators for MOS Systems

LM109, LM140 Series	Positive regulators.
LM120 Series	Negative regulators.
LM125 Series*	Dual +/− regulators.

*To be announced

SAVING ROMs IN HIGH-RESOLUTION DOT-MATRIX DISPLAYS AND PRINTERS

INTRODUCTION

Conventionally, the number of bits in a digital character generator's read only memory is proportional to the number of dots in the character matrix. That is, the ROM array ordinarily doubles and redoubles in size as one scales up the resolution or changes from an upper-case to an upper-case/lower-case font.

Fortunately, such progressions may not be required. Reorganizing the ROMs to suit the specific application often save thousands of bits and allows the designer to use smaller, faster, more economical monolithic ROMs. As a simple example, expanding the array in 32-character subsets rather than the more conventional 64-character subsets will enhance performance and save up to 25% of ROM capacity in typical UC/LC applications.

Savings much greater than 25% are possible when the matrix size reaches a point where several monolithic ROMs are needed to store the font. We have found a two-stage, column-generation approach called "intermediate coding" to be much more efficient than straightforward dot-matrix generation. It exploits the fact that column patterns tend to become highly redundant as the matrix size increases.

One version of this new technique automatically proportions character widths as in letterpress printing. This gives each character a more natural shape and eliminates the irregular spacings usually seen around "I" and other narrow characters. Yet the control logic is simple and the ROM savings approach 40% at typical font sizes.

Such advantages are available immediately, without development of special ROMs. The designs can be implemented with standard MOS or bipolar ROMs currently in production. In fact, intermediate coding broadens the cost/performance options by allowing a combination of MOS and bipolar ROMs to be used.

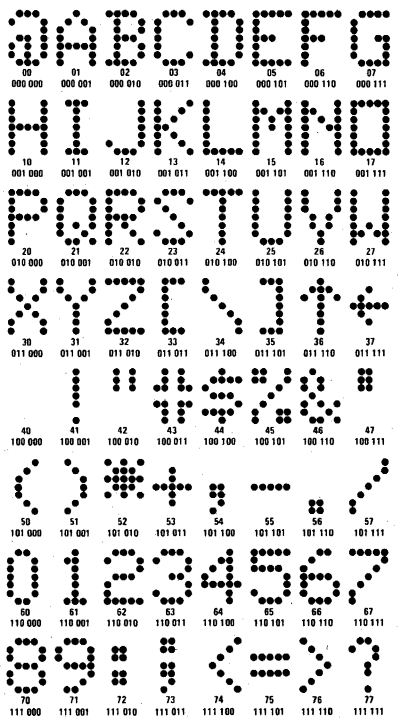
DOT-CHARACTER FONTS

Dot-character styles ranging in complexity from 5 x 7 to 12 x 24 or more dots per character have been developed to meet the human-engineering standard of various industries using digital displays and printers. The more popular sizes are listed in Table I.

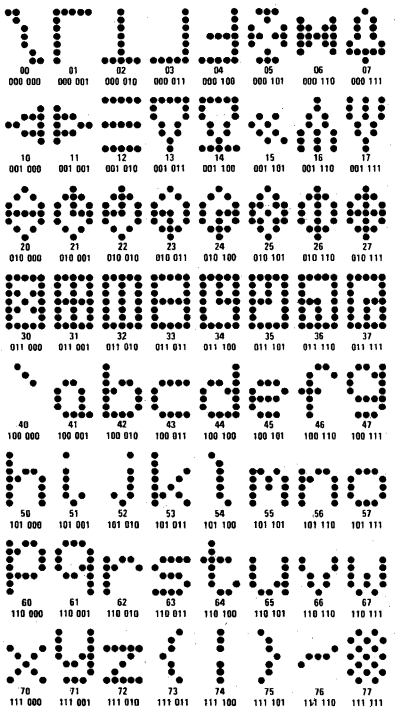
The 5 x 7 fonts, such as Figure 1, lead in applications volume due to their use in low-cost data

TABLE I. Typical Dot-Matrix Character Fonts

SIZE AND SCANNING	DOTS PER CHARACTER	THEORETICAL CHARACTER ROM	DESIGN EFFECTIVENESS	PRACTICAL DESIGNS
5 x 7				
Horizontal	35	64 x 7 x 5 = 2 – 1/2k	1.00	Fig. 3
7 x 5				
Vertical	35	64 x 5 x 7 = 2,560	1.00	Fig. 3
7 x 9				
Horizontal	63	64 x 9 x 7 = 4,032	0.67	Fig. 6
9 x 7				
Vertical	63	64 x 7 x 9 = 4,032	1.00	Figs. 5 & 8
7 x 12 & 8 x 12				
Horizontal	96	64 x 12 x 8 = 6,144 and 96 x 12 x 8 = 8,216	1.00 1.00	Figs. 6 & 7
12 x 7 & 12 x 8				
64 Character Vertical	96	64 x 8 x 12 = 6,144	1.00	Fig. 8C
96 Character Vertical	96	96 x 8 x 12 = 9,216	1.00	Fig. 8B
12 x 16				
64 Character Horizontal	192	64 x 16 x 12 = 12,288	1.50 for Fig. 9A	Fig. 9A
96 Character Horizontal	192	96 x 16 x 12 = 18,432	1.50 Fig. 9	Fig. 9B
16 x 12				
64 Character Vertical	192	64 x 12 x 16 = 12,288	1.50 for Fig. 9A	Figs. 6, 7, & 9
96 Character Vertical	192	96 x 12 x 16 = 18,432	1.50 for Fig. 9B	
24 x 12				
64 Character Vertical	288	64 x 12 x 24 = 18,432	2.00 for Fig. 9B	Figs. 6, 7, & 9
64 x 13 x 10 to 64 x 13 x 16				
64 Character Variable Font Width	208	64 x 13 x 16 = 13,312	3.06 for Fig. 10	Fig. 10



(A) Upper-Case Font



(B) Lower-Case Font

FIGURE 1. ASCII Full Set Font of 128 5 x 7 Characters

interface terminals (although some terminal manufacturers are going to larger sizes in response to complaints that 5 x 7 presentations cause eyestrain). In other applications, a standard is often set by older printing techniques. To cite a few examples: business-machine users are accustomed to typewriting; advertisers want characters with "sales appeal" on their billboard displays; scoreboards and traffic-control signs must be read easily at a distance; and electronic printing systems may have to simulate several metal type fonts.

The matrix size is frequently enlarged to improve lower-case character definition in UC/LC applications. A 5 x 7 font typically grows to 7 x 9 for UC and 7 x 12 for LC, as in Figure 2. Likewise, 7 x 9 is expanded to 8 x 12 and 12 x 16 to 12 x 24 for lower-cases.

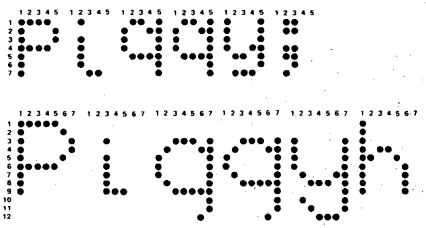


FIGURE 2. UC/LC Characters at 5 x 7 and 7 x 12 Matrix Sizes

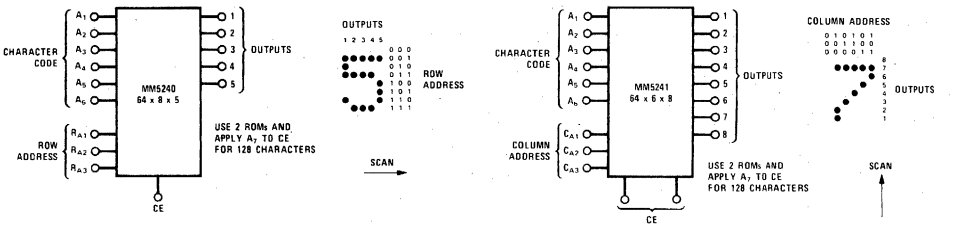
At 5 x 7, it is most economical, as a rule, to program a "full set" of 128 UC/LC characters in standard character-generator ROMs. The full set in Figure 1 is stored in two 64-character MOS ROMs. This provides a mass-production base and equalizes access times. If the 32 special symbols generated with the ASCII control codes are not usable, they are simply blanked by disenabling the lower-case ROM when the seventh ASCII bit is "0." But if the font is scaled up to simulate typewriting, for example, this practice becomes wasteful since 96 characters would suffice.

Another complication is that many specialized font sizes, such as 11 x 9, do not fit neatly into standard ROMs made in building block sizes. In other words, one cannot store the font in a minimum-sized ROM array without paying the extra costs of custom ROM development or specialized low-volumn ROMs.

CHARACTER-GENERATOR ROMs

Consequently, character-generator ROMs have been developed that adapt to a variety of font sizes. They may not exactly fit the theoretical matrix array at odd sizes. but that is easily offset by the economy of parts standardization.

Two such MOS ROMs are outlined in Figure 3 with their addressing for 5 x 7 horizontal scanning and 7 x 5 vertical scanning. The vertical-scan subsystem in Figure 4 shows the amount of support logic typically required in a display.



(A) 5 x 7 Horizontal-Scan, 64-Characters

(B) 7 x 5 Vertical-Scan, 64-Characters

FIGURE 3. MM5240 and MM5241 Standard Character-Generator ROMs

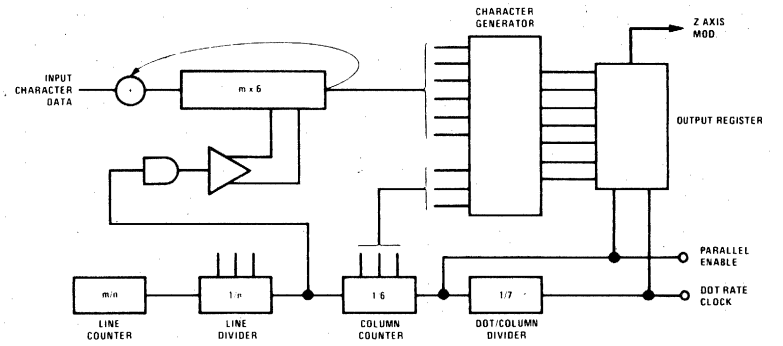


FIGURE 4. Typical 7 x 5 Vertical-Scan Display Generator Subsystem

The MM5240 expands straightforwardly in 64-character increments to larger fonts, such as the 9 x 7 or 10 x 8 arrays in Figure 5A. An expansion such as Figure 5B would be used to provide a full set UC/LC font. These expansions keep the character rate the same as at 5 x 7, whereas doubling the size of each monolithic ROM would not.

32-CHARACTER BLOCKS

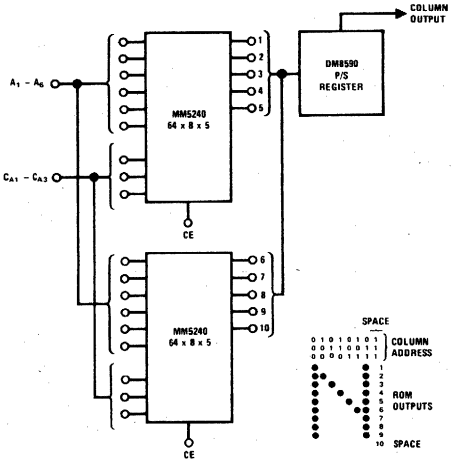
A similar expansion of the MM5241, as in Figure 6A, would provide 7 x 9 to 8 x 12 horizontal-scan fonts. However, the direct 64-character expansion places a ROM-enabling operation in the middle of the character. Such operations are common in large-font generator designs.

A simple solution to this problem is to "steal" a character-address input, use it as a row-address input, and then use a chip-enable input as a character input (Figure 6B). This provides a 32-character or 64-character block enabled during the between-characters spacing interval. A 32-character block would be the only ROM required in a system using only numbers and symbols.

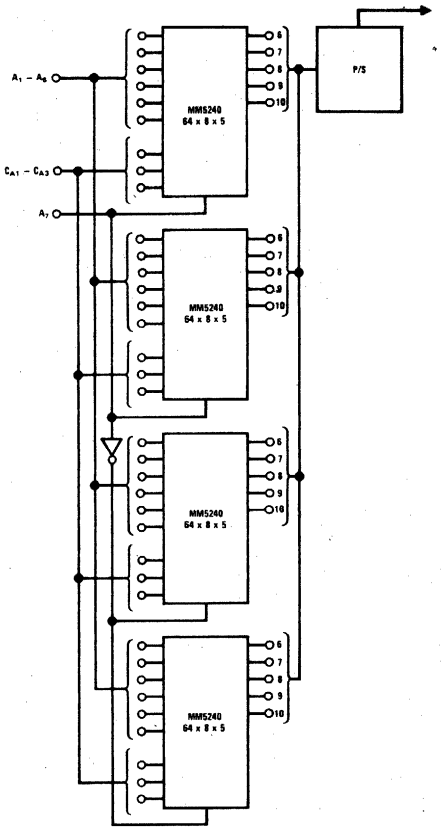
However, the chief attraction of this conversion is in UC/LC applications. Figure 7 shows how to use three ROMs to generate 96 7 x 9 to 8 x 12 horizontal-scan characters—a 25% savings compared with a "full set" expansion. The chip-enable inputs are programmed to sense the sixth and seventh character-address bits. External decoders aren't needed.

If each ROM in Figure 7 is replaced with a parallel assembly of three ROMs (24 outputs), the result is a 24 x 12, 96-character vertical-scan generator with the same character rate as at 8 x 12. In other words, the 32-character approach maintains the benefits of parts standardization and performance up to a very high resolution.

Other ROMs can be used in this fashion. In Figure 8, the MM5227 TRI-STATE® and MM5288 256 x 12 ROMs are shown in expansions that complement those of the MM5241. These ROMs provide access times well under a microsecond. For rates in the nanosecond range, general-purpose bipolar ROMs with four or eight outputs, such as the DM8597 256 x 4 and DM8596 512 x 8 can be worked into similar organizations.

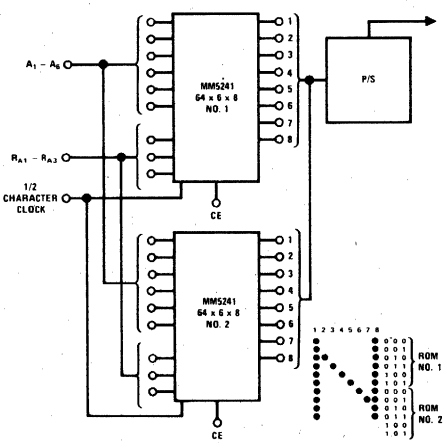


(A) 9 x 7 or 10 x 8 Vertical-Scan, 64-Characters

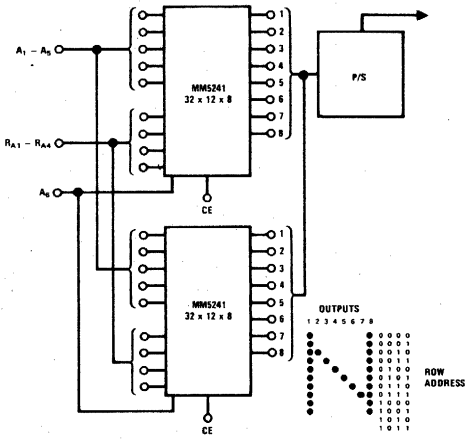


(B) 9 x 7 or 10 x 8 Vertical-Scan, 128-Characters

FIGURE 5. Expansion of MM5240 to Larger Fonts



(A) 7 x 9 to 8 x 12 Horizontal-Scan, 64-Characters



(B) 7 x 9 to 8 x 12 Horizontal-Scan, 64-Characters

FIGURE 6. Conventional and Improved MM5241 Expansions to 8 x 12

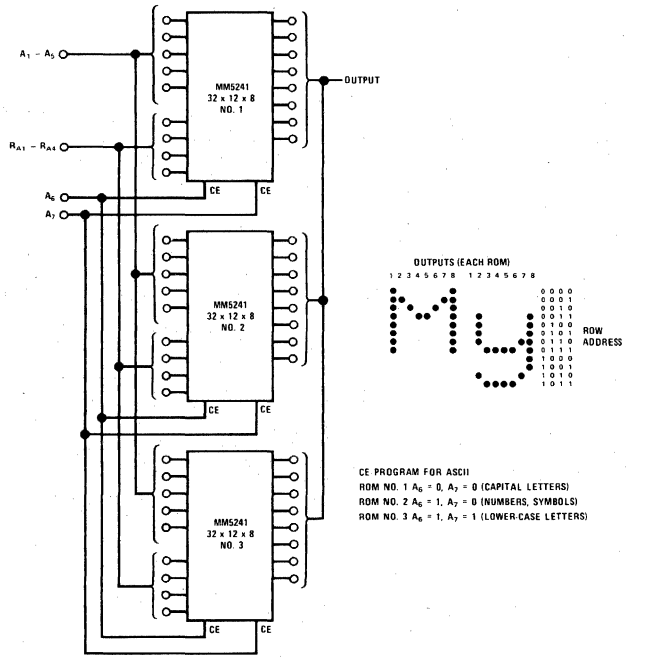
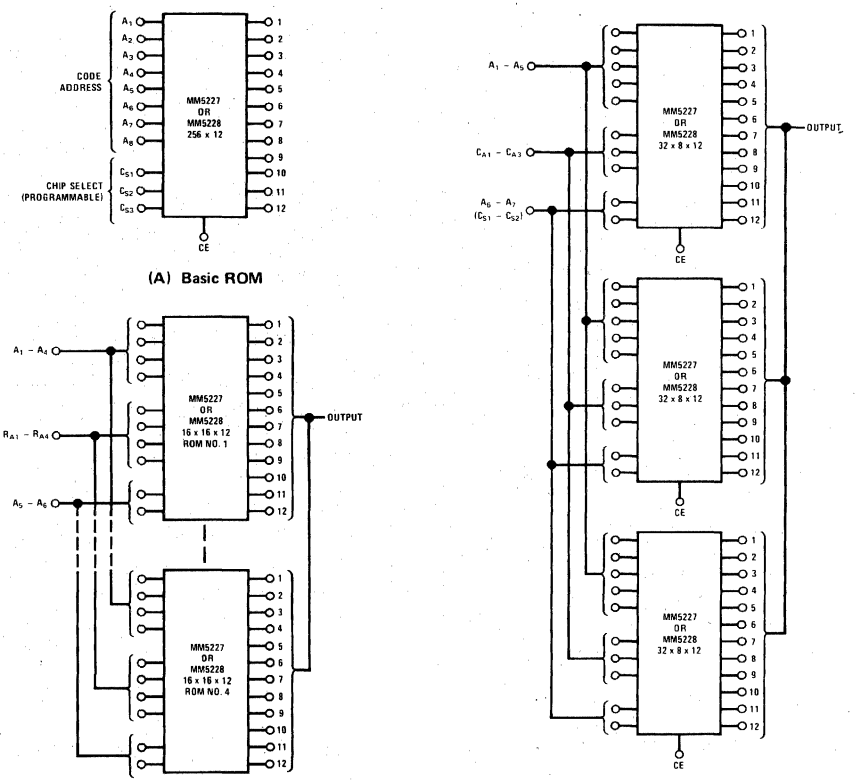


FIGURE 7. Using 32-Character Expansions for 7 x 12 or 8 x 12, 96-Character Generator



(A) Basic ROM

(C) 12 x 16 Horizontal-Scan, 64-Characters

(B) 9 x 7 to 12 x 8 Vertical-Scan, 96-Characters

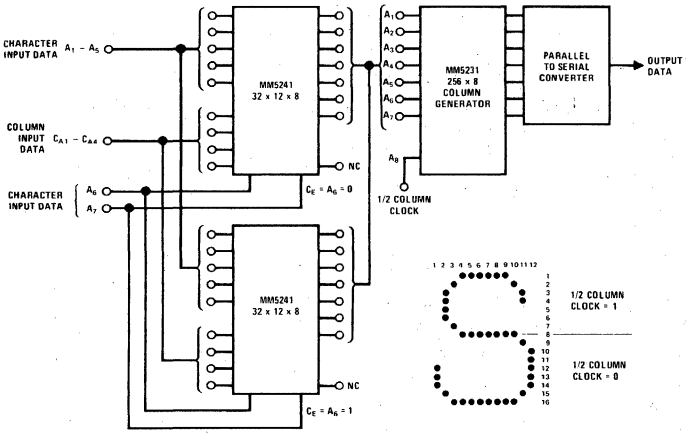
FIGURE 8. Addressing General-Purpose ROMs as Character Generators

INTERMEDIATE CODING

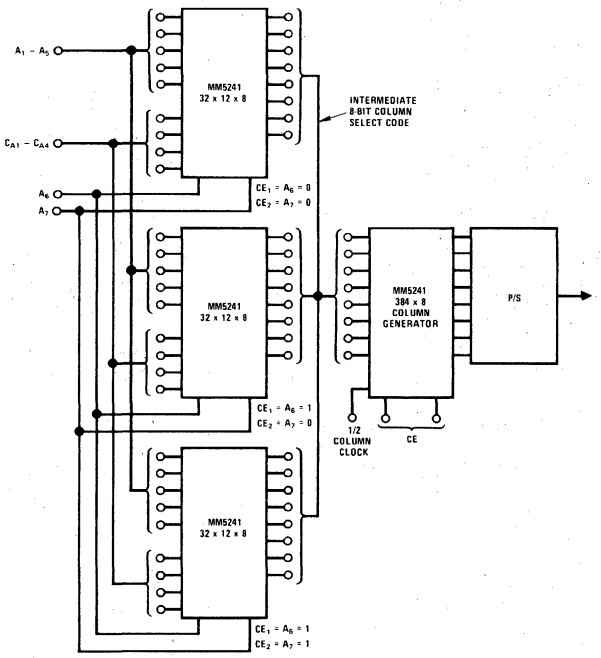
Designs proportioned to the matrix size are not the most efficient at the larger font sizes. It pays to analyze the actual character patterns to determine whether other organizations can be used.

For example, the full-dot columns in such vertical-scan characters as b, B, d, D, H, T, etc., are usually identical. An upper-case font typically contains only 60 unique column patterns at 7 x 5, 110 at 9 x 7, 120 at 11 x 9, and 122 at 16 x 12. Theoretically, they could all have been unique, since there is a possible pattern variation ranging from 128 to 65,536 (2^7 to 2^{16}). UC/LC and horizontal-scan fonts are more variable than upper-case vertical-scan fonts, but they are still far from worst-case.

This analysis led to the organization in Figure 9A. Instead of doubling the 64 x 12 x 8 organization to produce fonts up to 16 x 12, it adds only a 2k



(A) 12 x 16 Vertical Scan (UC)



(B) 16 x 12, 96-Character Generator (UC/LC)

FIGURE 9. Intermediate Coding Designs (MOS ROM Organizations)

ROM. Up to 128 unique column patterns are stored in 8-bit, half-column segments in the MM5231 256 x 8 ROM. These are accessed with 7-bit intermediate codes selected with the input array and a half-column clock at a submultiple of the dot rate. The intermediate codes necessary to form each character are simply listed in character-generator fashion in the input code converters. At 16 x 12, the savings for an upper-case font are 12k − 8k or 4 kilobits—33%.

Since the 8-bit outputs of the MM5241 ROMs actually allow 128 unique columns to be selected, the savings could grow rapidly through several expansion levels even without further rearranging. If more than 128 unique column codes are required the second ROM in the storing can be changed to possibly a 512 x 8 ROM (MM5232) therefore giving 256 unique columns which can be generated for the larger fonts and character group sets (96 characters or 128 characters).

Assume a 16 x 12, 96-character requirement. MM5241 ROMs added as in Figure 9B would provide 192 unique column patterns and the savings would be at least 18k − 12k = 6k.

It might be necessary at the 24 x 12 UC/LC size to use two MM5227 256 x 12 ROMs in parallel, but this would still save 27k − 15k = 12k (or perhaps 36k − 18k in a 128-character application, using four input and two output ROMs). The efficiency grows with font size because the column patterns become more redundant.

At first glance, the organization appears to double the access time because there are two stages to be accessed in sequence. But since there is no feedback, the stages can operate in a ripple mode. Thus, an 8-bit bipolar register can be inserted between the stages to temporarily store each intermediate code. This restores the overall access time to that of the slowest ROM in the series (e.g., less than a microsecond for MOS ROMs) and the character rate is essentially the same as that achieved with conventional ROM techniques.

Alternatively, the output ROM, input ROM, or both may be bipolar to increase the rate. The DM8596 512 x 8 ROM fits most large-font geometries quite well and costs less than sub-assemblies of 1k bipolar ROMs. Again, an intermediate register will maximize the rate.

REPEAT-PATTERN CODING

Some character styles have bold "double dot" or similar patterns that result in a high probability of the same column pattern repeating sequentially in the same character. This characteristic is common in "ticker tape" systems, large-panel and billboard displays, news bulletins broadcast to appear as a running line across a television picture, and so forth. Typical fonts exhibit less than 256 actual changes of column patterns through a 64-character sequence, not the worst-case of 320 at 7 x 5, 640 at 10 x 8, and so forth. Therefore, an organization that holds the column output static until it has to change would be highly efficient.

Figure 10 is a practical design for upper-case fonts with 10 x 10 to 13 x 10 matrices. It saves nearly 40% of ROM capacity. Moreover, the matrix width varies with the character shape as can be seen in the example word LIMB. The characters look more natural and are evenly spaced. Column height is changed by programming the outputs to be used.

Proportional spacing makes this organization an excellent choice for ink-dot spray printers and other "line of type" printing applications, as well as vertical-scan displays.

This technique does not lend itself directly to raster-scan displays since characters are scanned sequentially on one raster line at a time rather than completing a character before starting a new character. To use this technique on raster-scan an intermediate storage memory would be necessary for as a line memories.

PROGRAMMING AND OPERATION

Assume a nominal matrix size of 13 x 10. This takes a 256 x 16 ROM array. Each 16-bit output word contains a 13-dot column pattern, a 2-bit repeat code and, in the last word of a character, an EOC bit (end of character "1" bit). Address location 0000 0000 is reserved for an all-zero spacing column.

The first address of each character is listed in the small input ROM at locations where they will be accessed by the standard code. The intermediate code will then be the starting address and the next column-select codes for each character will be generated sequentially by the logic.

Suppose characters @ through K occupy locations 0000 0001 through 0010 1111 in the main ROM. Then, L's three words occupy locations 0011 0000 through 0011 0010, M starts at 0011 0011, and so forth. L takes three words at the 13 x 10 size since the 2-dot bar pattern can be repeated only four times with a 2-bit repeat code. If the columns were programmed 12 or less dots high, a 3-bit repeat code could be used. L would be generated with two words and single-pattern characters like "dash" with one word. This solution uses only 2 x 16 bits of storage for the character L and compared with its present technique of 10 x 12 = 120 bits.

Now, let's generate LIMB. First, the standard code for L (e.g. 001 100) is converted to 0011 0000, which sets the address counter. The address counter access that word in the main ROM, and the repeat code in the output sets the master counter to time out in two column scanning intervals.

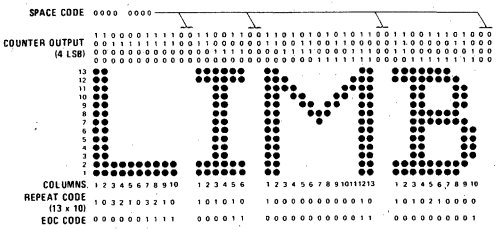
L's first two columns are thus formed. At the master counter's terminal state, the address counter advances to 0011 0001, the master counter is reset

to time out in four column intervals, the address counter advances again, and word 0011 0010 is accessed during four intervals.

This last word includes an EOC bit. When EOC and the time-out state of the master counter coincide, gate 1 clears the address counter. Now address 0000 0000 generates the space pattern in two spacing columns. When the master counter reaches its second state, gate 2 enables the address counter's parallel preset inputs. Finally, the input ROM sets the counter to the starting address for I and the process continues through I, M and B.

Proportional spacing is inherent. So is high-speed since the input ROM is a small bipolar array. The main ROM can be either MOS or bipolar general-purpose ROMs. This organization should also expand efficiently since the repeat probability tends to rise with matrix width.

In printing applications involving more complex characters, the operational advantages might be of more interest than ROM savings. For example, two 64 x 6 x 8 or 512 x 8 ROMs might be used as an UC/LC generator with the ninth address input a direct shift control.



(Repeat Pattern Character Quality and Coding Example)

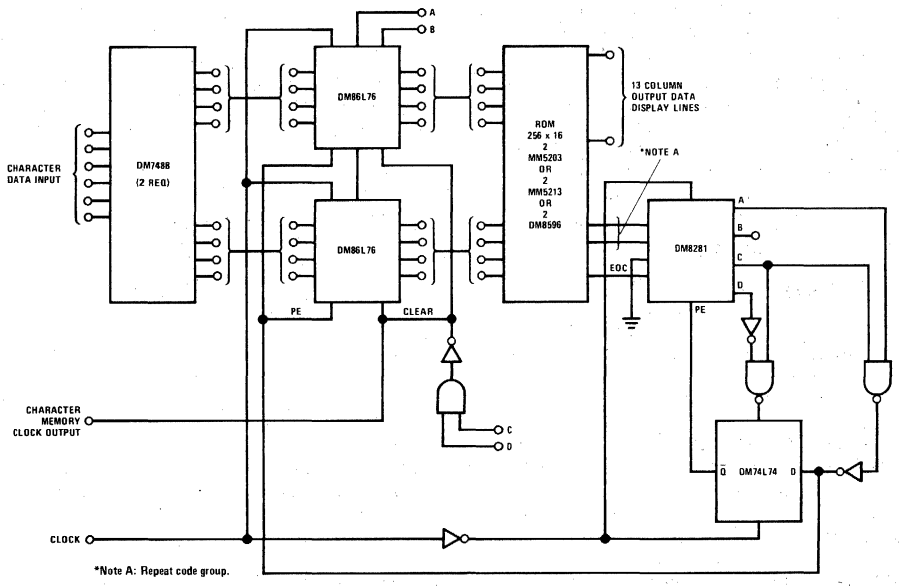


FIGURE 10. Repeat-Pattern Vertical-Scan Generator

NATIONAL

A SIMPLE POWER SAVING TECHNIQUE FOR THE MM5262 2k RAM

INTRODUCTION

The MM5262 is a state of the art RAM designed to operate efficiently in modern bus organized systems. Most bused systems present the address information to the data bus only during the early portion of the machine cycle and then transfer data during the remainder of the cycle. The MM5262, unlike many other RAMs, does not need a memory address register to hold the address stable on its inputs during the complete cycle because the address is clocked into the MM5262 on-chip address register by Phase 1. The address and chip select signals need only be applied during Phase 1 and the Phase 1 to Phase 2 gap.

SAVING POWER

Because of the very low power dissipation of the MM5262 when the clocks are turned off (< 2.0 mW), a method for decoding the clocks of unselected chips in the memory array would result in a sizable decrease in power consumption. A problem arises because to deselect a chip, a Phase 1 pulse must be applied to clock the disable signal into the chip. There would be little advantage in allowing Phase 1 to free run and decoding only Phase 2 and Phase 3 because approximately 75% of the power dissipation is associated with Phase 1. The best solution is a decoding arrangement where the disabling of Phase 1 is delayed by one cycle and the enabling of Phase 1 is not delayed. The chip will receive one extra Phase 1 pulse to disable it and will no longer draw power until it is again enabled. The power then becomes worst case when alternately accessing two chips. Both chips will draw power continuously while all other deselected chips draw 0.1 mA each. Table I shows expected power supply currents for various size memories per bit of word width: column II – average power supply current with only one chip selected; column III – average power supply current under worst case conditions of alternately selecting two chips; and column V – worst case average current including refresh (assuming a 635 ns cycle time). The peak current during refresh, assuming all chips are refreshed at the same time, is equal to the total number of chips multiplied by 20 mA maximum per chip. During an interval of 2.0 ms, the memory will cycle almost 3,000 times, of which only 32 cycles must be devoted to refresh; therefore, the average refresh power will be one percent of the peak power or 0.2 mA per chip. Comparable savings in clock driver power dissipation are also realized.

Using the data from Table I for a common application, such as an 8k-by-16 memory for a minicomputer, the power is cut to half that required without decoding. In a large memory, such as 64k words, the power is cut by a factor

TABLE I.

NUMBER OF WORDS	CHIPS PER BIT OF WORD WIDTH	MAXIMUM POWER SUPPLY CURRENT (mA)/PER BIT OF WORD WIDTH					
		I NO CLOCK DECODING	II CLOCK DECODING ONE CHIP SELECTED	III CLOCK DECODING TWO CHIPS ALTERNATELY SELECTED	IV ADDITIONAL AVERAGE REFRESH CURRENT	V NS TOTAL WORST CASE	6003 (4 mA STANDBY CURRENT)
2,048	1.0	20				20	10
4,096	2.0	40	20.1	40	0	40	20
8,192	4.0	80	20.3	40.2	0.4	40.6	28.2
16,384	8.0	160	20.7	40.6	1.2	41.8	44.6
32,768	16	320	21.5	41.4	2.8	44.2	77.4
65,536	32	640	23.1	43	6.0	49	143
131,072	64	1,280	26.3	46.2	12.4	58.6	274

N = Number of words in 2048 increments N $\geq$ 4096

B = Number of bits/words

t_{CYCLE} = Memory cycle time

$$\underbrace{I_{DD}\,(AVG)_{MAX}}_{V} = B\Bigg\{\underbrace{2 \times 20 + \left(\frac{N}{2048} - 2\right) \times 0.1}_{III} + \underbrace{\left(\frac{N}{2048} - 2\right) \times \frac{32\,t_{CYCLE}}{2\text{ ms}} \times 20}_{IV}\Bigg\}$$

of 13. Figure 1 shows a plot of memory current as a function of memory size with a comparison of the nearest equivalent 2k RAM.

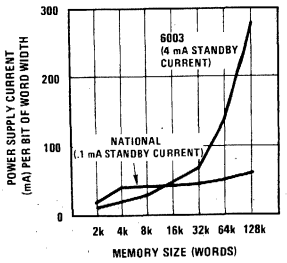


FIGURE 1. Memory Size vs 2k RAM Power Supply Current

A memory system configured as 8k words by 16-bits per word, for example, would draw 80 mA times 16-bits (1.28 Amps) if undecoded. If the same memory is decoded, the current drops to 40.6 mA times 16-bits (650 mA) which is half the current of the undecoded memory. In a large system, such as 64k words by 32-bits per word the savings is even greater. Undecoded the supply current is 640 mA times 32-bits (20.5 Amps) while the same memory when the clocks are decoded draws 49 mA times 32-bits (1.6 Amps). The power for the decoded memory then is one-thirteenth of that required for the undecoded memory.

LOGIC IMPLEMENTATION

Figure 2 shows the logic required to implement the power saving technique, Figure 3 is a timing diagram for the logic, and Figure 4 is a block diagram of an 8k word by 16-bit/word module.

In operation the clock decoder in Figure 2 will supply clock pulses during any cycle in which the chip is selected (Figure 3 — cycle 1 and cycle 6) or when the memory is being refreshed (Figure 3 — cycle 4) and will supply an extra Phase 1 pulse on the first cycle after deselecting the chip (Figure 3 — cycle 2). During all remaining cycles the chip is deselected and no clock pulses are supplied to the chips.

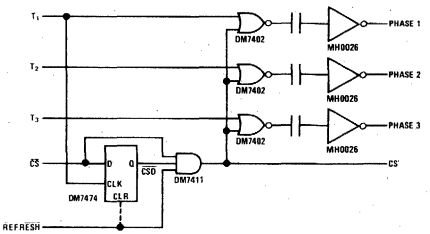


FIGURE 2. MM5262 Clock Decoding Logic

There are three practical considerations to be aware of when using this circuit. First is that, although the power supplies need only be large enough to supply the average current to the memory and its clock drivers, the capacitance bypassing the power supplies should be large enough to supply the peak current during refresh without excessive power supply droop. The second consideration is that if T1 goes to the low state prior to CS or $\overline{\text{REFRESH}}$ going low, the leading edge of Phase 1 will be delayed according to the delay in chip select and T1 pulse width may have to be increased to ensure that the minimum Phase 1 pulse width is supplied to the chip. The third is that if $\overline{\text{REFRESH}}$ goes high after T1 goes low a glitch will be produced on Phase 1. If $\overline{\text{REFRESH}}$ is connected to the clear input of

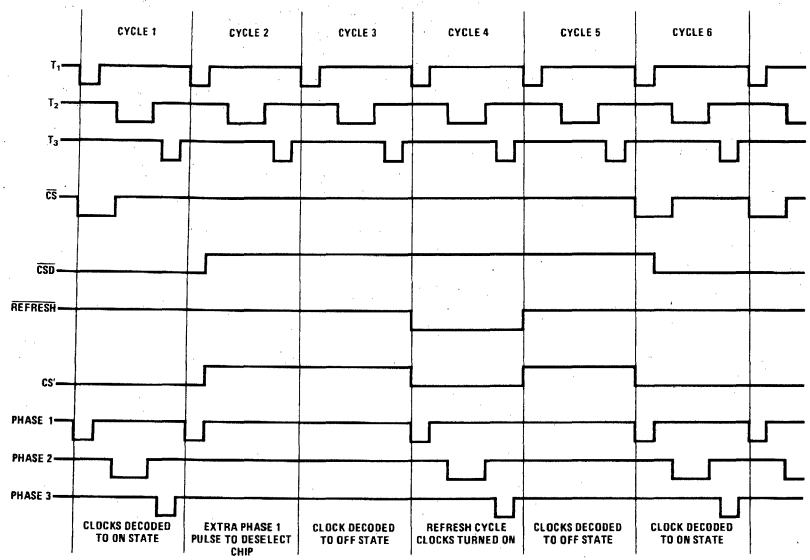


FIGURE 3. MM5262 Clock Decoding Timing Diagram

the DM7474, as shown by the dotted line in Figure 2, the glitch will be extended into a full Phase 1 pulse.

The extra Phase 1 pulse after a refresh cycle will not cause any problems but it will change the value of the refresh current. If refresh is implemented by doing one refresh cycle every 62.4μs, the refresh power will be doubled over what it would be if 32 refresh cycles are done consecutively every 2.0 ms. This is due to the fact that with 32 consecutive refresh cycles the memory receives 33 Phase 1 clocks and with a refresh cycle every 62.4μs the memory receives 64 Phase 1 clocks.

One advantage of connecting $\overline{\text{REFRESH}}$ to the clear input of the DM7474 is that $\overline{\text{REFRESH}}$ is no longer required to be applied for the entire cycle and may return to a one after the positive edge of T1.

It is perhaps of more interest to examine an actual system to determine the effects of clock decoding. As an example a complete 8k-by-16-bit memory has been designed and is shown in Figure 4. This system is not optimized but will serve as a good comparative example. Table II shows power consumption for operating and standby modes with clock decoding and Table III gives power consumption without clock decoding. A comparison between these tables shows a 42% decrease in power consumption by employing clock decoding. Table IV shows various memories mechanized using the basic 8k-by-16 module. Power consumption is given with and without clock decoding for cycle times of 635 ns and 1,000 ns. It is clear from these tables that as memory size increases clock decoding becomes essential. Saying this another way, the ratio of a memory components operating power to standby power is an important parameter for the designer.

TABLE II. Power Consumption of 8k x 16 Module (With t_{CYCLE} = 635 ns and Clock Decoding)

	I_{CC} (mA) @ 5.25V		I_{DD} (mA) @ −16V		I_{BB} (mA) @ 8.75V	
	OPERATING	STANDBY	OPERATING	STANDBY	OPERATING	STANDBY
TTL	1,180	1,180	0	0	0	0
MH0026	124	1.2	111	1.1	0	0
MM5262	699	12.8	650	19.2	8.0	6.5
Total Current	2,003	1,194	761	20.3	8.0	6.5
Total Power (Watts)	10.5	6.3	12.2	0.33	0.07	0.057

Total Operating Power = 10.5 + 12.2 + 0.07 ≅ 22.8 Watts
Total Standby Power = 6.3 + 0.33 + 0.057 = 6.7 Watts

TABLE III. Power Consumption of 8k x 16 Module (With t_{CYCLE} = 635 ns and No Clock Decoding)

	I_{CC} (mA) @ 5.25V	I_{DD} (mA) @ −16V	I_{BB} (mA) @ 8.75V
	OPERATING	OPERATING	OPERATING
TTL	1,180	0	0
MH0026	241	231	0
MM5262	1,333	1,290	9.6
Total Current	2,754	1,521	9.6
Total Power (Watts)	14.4	24.4	0.875

Total Operating Power = 14.4 + 24.4 + 0.875 ≅ 39.3 Watts

TABLE IV. Power Consumption of Larger Memory Systems Using Multiple 8k x 16 Modules

MEMORY SIZE	NUMBER OF CARDS	TOTAL POWER (Watts) t_{CYCLE} = 635 ns		TOTAL POWER (Watts) t_{CYCLE} = 1,000 ns	
		CLOCK DECODING	NO CLOCK DECODING	CLOCK DECODING	NO CLOCK DECODING
8k x 16	1	22.8	39.3	16.9	25.8
8k x 32	2	45.6	78.6	33.8	51.6
16k x 16	2	29.5	78.6	23.5	51.6
16k x 32	4	59	157.2	47	103.2
32k x 16	4	42.9	157.2	36.7	103.2
32k x 32	8	85.8	314.4	73.4	206.4

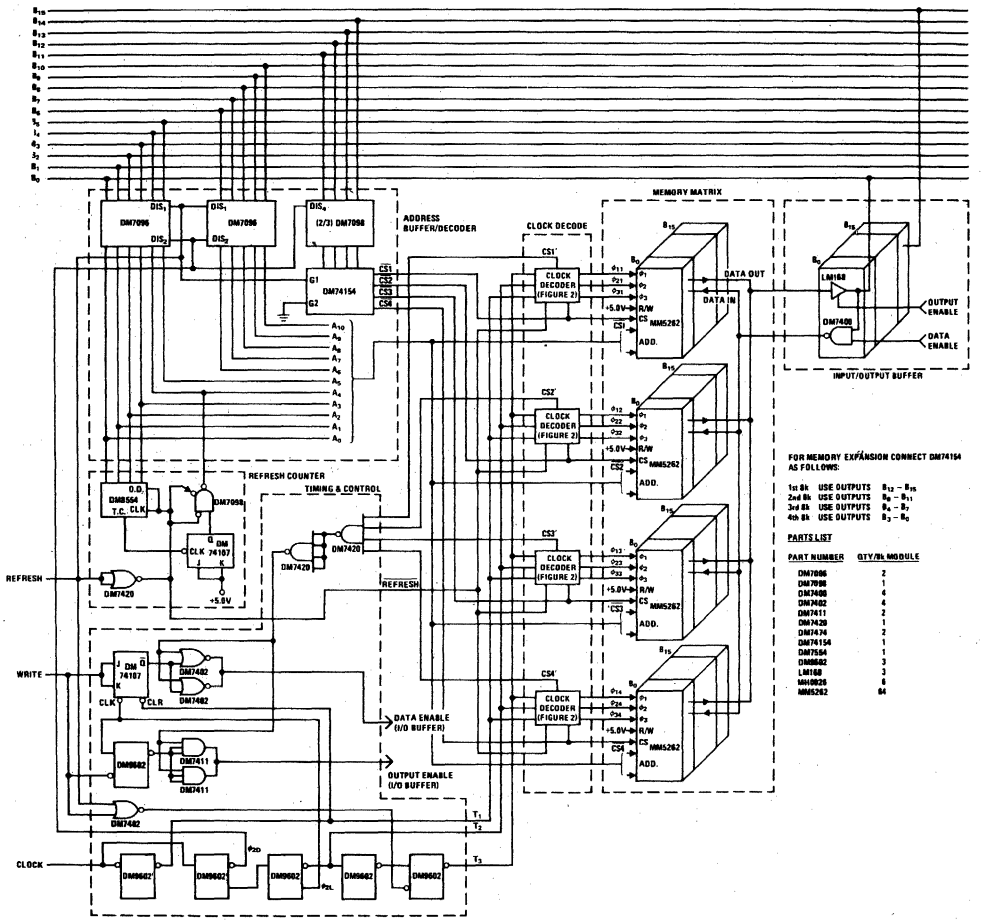


FIGURE 4. 8k x 16 Memory Module

HOW TO DESIGN WITH PROGRAMMABLE LOGIC ARRAYS

INTRODUCTION

A new and exciting IC device, the PLA (Programmable Logic Array), is heralding a new era of circuit compression comparable to the introduction of medium scale integration devices in the days when gates and flops were the only digital building blocks available.

As the name suggests, a PLA is an array of logic elements such that a given input function produces a known output function. In this sense, the device could be as simple as a gate or as complex as a Read Only Memory (ROM). Applications range from the slowest and smallest systems, such as traffic light controllers, to fast, high performance and complex large digital processors. In the following sections, the PLA will be described and its advantages over alternate logic forms demonstrated.

WHAT IS A PLA?

Since there is a difference between a Programmable Logic Array (PLA) and a rectangularly structured Read Only Memory (ROM), the PLA should be described. Even though any input code can be decoded to any output code in the PLA, not all possible input combinations are possible within the same package. The numbers of inputs to a PLA are much more than would be available with ROMs (Figure 1). In the case of the DM8575/DM8576 there are 14 inputs and 8 outputs. This would relate to ROM with 2^{14} or 16,384 words. This PLA (DM8575/DM8576) has 96 equivalent words. These terms are called partial product terms. Each product term can be described as a logical AND function which relates to a protion of the total output terminal solution. Each product term can be programmed to any complexity up to the input limit of the PLA. The DM8575/DM8576 PLA may have 14 variables in its product term or it may only have one input which establishes the product term. The PLA logically can be described as a collection of "ANDs" which may be "ORed" at any of its outputs. Figure 2 shows the logical data flow from the 14 address input terminals through the "AND" gate to the "OR" gate and to the output terminal.

The large variation in the partial product terms possibilities of the 14 input variables are shown below:

$$P_1 = I_1\ I_6\ I_7\ \overline{I_{10}}\ I_{14}$$

$$P_2 = I_4\ I_5\ I_7\ I_{12}\ \overline{I_{13}}\ I_{14}$$

$$P_3 = I_6\ I_{12}$$

$$P_4 = I_8\ I_9\ I_{10}\ I_{11}$$

$$\vdots$$

$$P_{96} = I_1\ I_2\ I_3\ I_{13}\ I_{14}$$

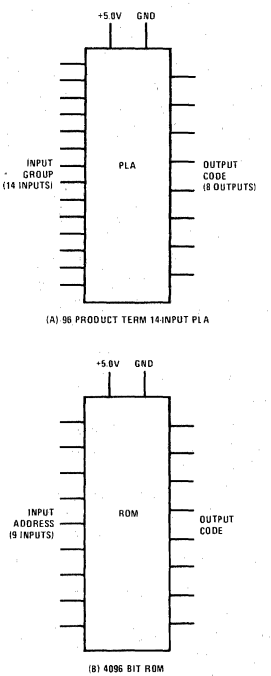


FIGURE 1.

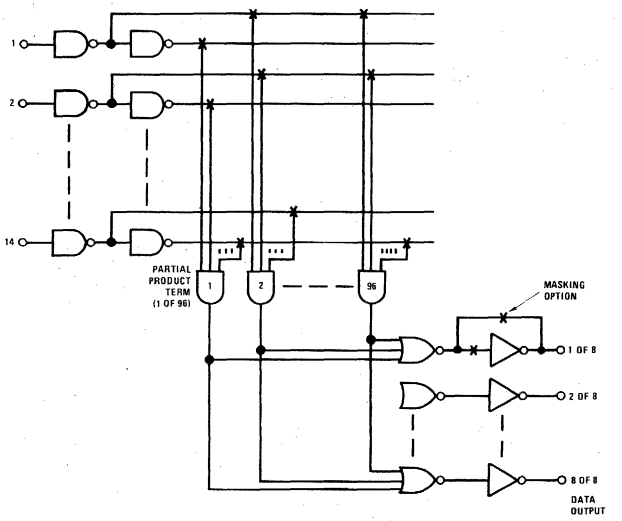


FIGURE 2.

It is possible to combine or collect by mask option any of the product terms for any of the several outputs to establish the output code combinations desired. Logically any or all of the partial product terms (AND terms) can be combined (ORed) at each output.

The equations for the output group have the following form:

$$O_1 = P_1 + P_{16} = P_{20} + P_{42} + \ldots P_{92}$$

$$O_2 = P_6 + P_{16} + P_{17} + P_{42} + \ldots P_{52}$$

$$O_3 = P_1 + P_{20} + P_{36} + \ldots P_{96}$$

Each of the partial product terms labeled P_1 through P_{96} are shown as they appear at each output. Note that the same product term may be used in as many output equation groups as required. It can be seen that P_1, the first product term, is used in both outputs one and three and P_{16} and P_{42} are used in outputs one and two.

A PLA need not have more than one output but it is generally more efficient to build the PLA or ROM with more than one output. The PLA in this discussion has eight output terminals which reflect the silicon efficiencies of today's technology. This product has the ability to be masked with outputs in either a positive true state or a negative true state. (Figure 2) These capabilities enhance the elements value when applied to the system solution since the inverter at the output terminal is not required.

To use this memory storage device, the memory storage equations must be written or tabulated so they can be stored within the mask programmed element. A large number of possible choices exist when the equations or product terms are collected at the outputs. The system designer must test the possible choices to be used within the PLA. He should combine all mutual terms within the same package. Commonly grouped product term adds to the efficiency of the PLA or PLA array as indicated in the previously mentioned equations.

WHY A PLA?

The application of the PLA in a digital solution is a natural evolution in system design. Several years ago digital systems were designed with gates and dual D memory elements. The system at that time, was conceived and implemented in its best possible way. A later development in system design utilized ROM's to provide the complex decoding for the control necessary to satisfy the same system design objective. Now we are in a new era. The design of the same system control function can be achieved by utilizing the desirable characteristics of the PLA (Programmable Logic Array). The reason for this evolution of design is based upon one or more of three possibilities. First, the new design will yield a higher performance solution. This generally relates to an improvement in system dynamic performance because fewer levels of logic are required to provide the same control function. Second, the design will result in a lower parts cost. This is due to the more efficient use of the memory array as compared with the normal rectangular array ROM. The third possible advantage comes from the reduction in system manufacturing cost brought about because of the reduction in component assembly cost, the reduction in printed circuit board cost or possibly connector cost within the system. Each time a system's physical size can be reduced by the use of more complex elements such as a PLA (Programmable Logic Array) the cost of that system decreases also because fewer cards and connectors are required.

THE PLA AS A CODE CONVERTER

Being a device, which from its input terminals produces outputs in accordance with a predefined set of rules, a PLA can be viewed as a memory storage device (i.e., a limited capability ROM). Hence, if all the partial product terms for a particular code conversion can be limited to the 96 available, then the PLA could be used in this application.

Recall that a product term consists of a combination of input variables which can represent a characters code, then the code conversion is possible for a 96 character set. Take the case of 12-line Hollerith to 8-line ASCII conversion as an example. Theoretically, 12-line input represents the possibility of 4k words. Actually, seven of the 12 Hollerith lines are not binary coded lines, they are ordinary decimally coded lines. So that a ROM structure with 12 input lines are not used, these seven lines must first be encoded to 3 binary lines using additional logic elements prior to being presented into a common 8-input ROM (Figure 3A). In addition, the 12-input ROM would have to decode all the non-existent input possibilities into don't care (or error) output states.

The PLA solves this problem efficiently. All 12 inputs are presented to the PLA. Since selective decoding is a feature of the PLA no provision need be made for pre-encoding of the inputs (Figure 3B).

An invalid input is designed to produce an all-high output state by virtue of the fact that it is not a recognizable product term.

THE PLA AS A DECODE ELEMENT IN A DIGITAL PROCESSOR

Why does it naturally follow that the PLA lends itself to the control function of a digital processor or other simularly organized system? Many processor oriented systems have control instruction codes which are much wider (a large number of inputs bits) than that which can be easily satisfied with ROM's.

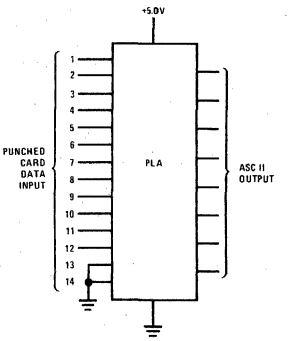


FIGURE 3B.

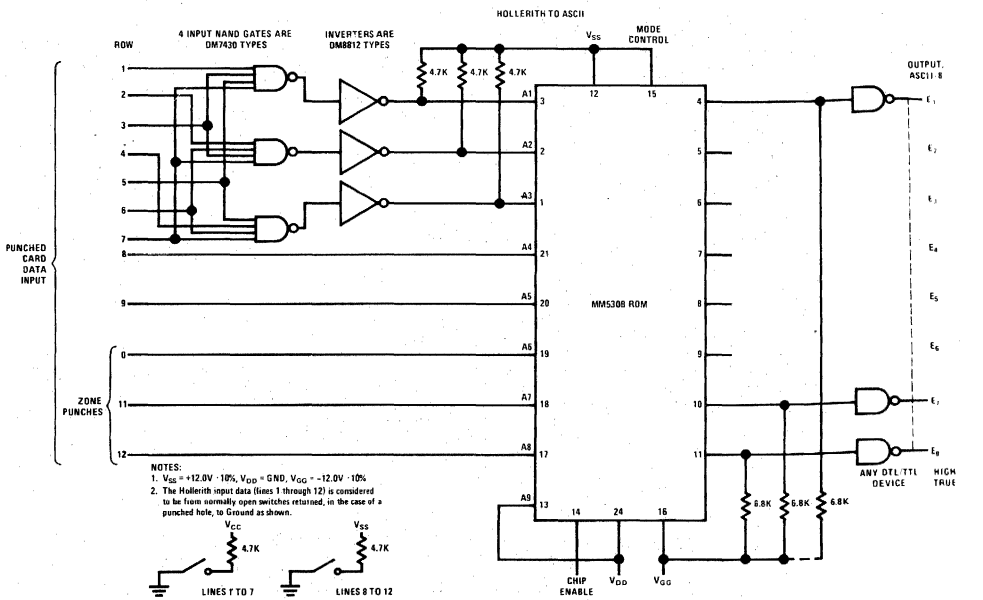


FIGURE 3A.

These types of applications have nine to eleven logical control code inputs. The timing code is also significant since the input instruction code must be logically "ANDed" with timing to form the output control signals. This results in a total input control group of eleven to thirteen bits to effect output control. Standard ROM's can be used to solve the the design problem. They have been used in the past but at the expense of system in component expense and generally in dynamic performance. If a complete input to output decode is solved, the cost of the complete ROM array is quite expensive. Two levels of logic are required to decode the proper ROM element group and enable the input data word to propagate to the output terminals (Figure 4). The technique is generally quite expensive since the quantity of ROM elements can be large.

In actual system use, not all combinations of codes of instruction data and timing data are used therefore, it is possible at times to use data compression techniques to reduce the number of ROM's necessary to store the output data. The technique normally used is to multiplex the required codes into the ROM elements as required by timing or a particular section of the input code group.

An example of such a multiplexer data decoder solution using ROM's is shown in Figure 5. Note that this solution technique uses two levels of multiplexers (DM74153's) to route the proper data to the ROM group. The use of these multiplexers significantly reduces the number of ROM's required but adds to the delay time to achieve the proper output levels. This technique also requires many engineering hours to first achieve a solution and even more to effect a change.

All five multiplexers and a ROM element are used to precode the inputs V of A PDP-8 system control ROM set.

A PLA solution would simply involve generating the logic equations for the outputs, isolating the common product terms, and implementing it in a masked PLA. Figure 6 illustrated how a PLA solution might look for the same 20-bit output word structure. The advantages of this approach are obvious.

First, the PLA design yields a higher performance solution. System dynamic performance will improve due to the reduction of signal paths interconnections and signal skewing. Secondly, a ROM solution is inefficient, requiring more silicon than is necessary to do the job and hence higher cost. Lastly, a reduction is effected in manufacturing costs due to the reduction in component assembly cost, P.C. Board cost, and interconnection cost.

THE PLA AS A SEQUENTIAL CONTROLLER

Another system application of the PLA is in sequential controllers. A sequential controller usually requires that a random set of input variables occur simultaneously to satisfy the condition of a particular state. This condition then allows advancing to the next controller state of the sequencer. An illustration of the use of the PLA in a sequencer application is that of a traffic controller. Referring to Figure 7, it is assumed that traffic can flow at high rates in any of four directions. It is also assumed that each direction has a left turn internal and that there is also provision for manual inputs to the system. It is also required to modify the timing interval depending upon the detected flow rate in any direction. The PLA is used as the controller for this adaptive sequence timer.

It would be possible to start the sequence within any of its possible status. While in each state, the other possible states are scanned to determine if the present state should be shortened or made longer in the example case, states B, C and D are checked as to the traffic status while the sequencer is in state A.

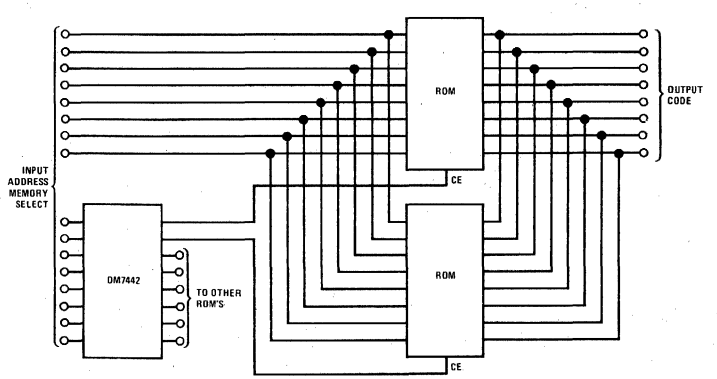


FIGURE 4.

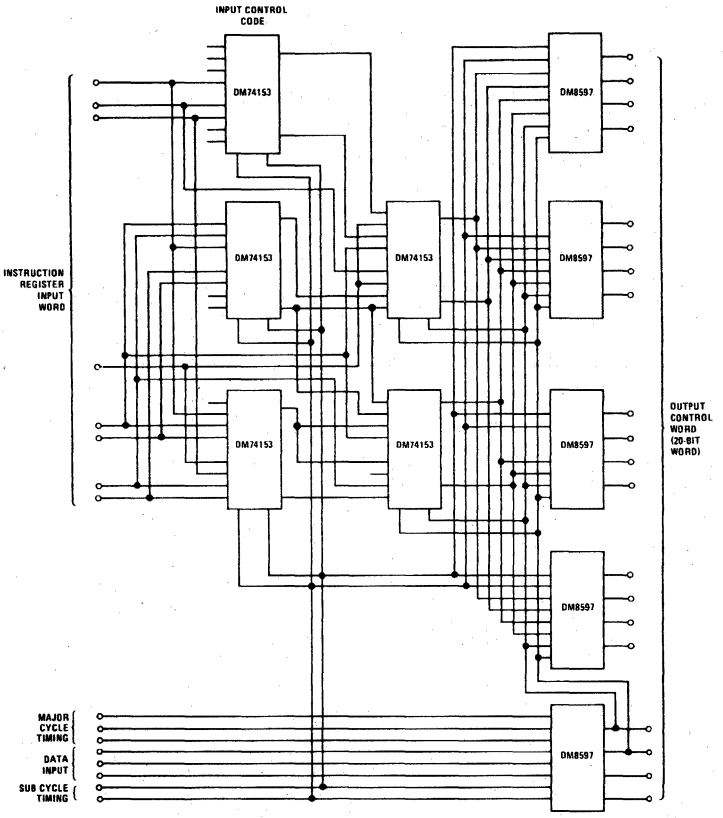


FIGURE 5.

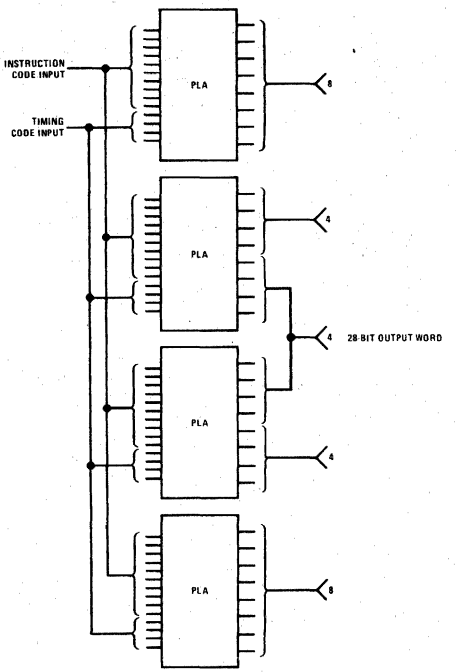


FIGURE 6.

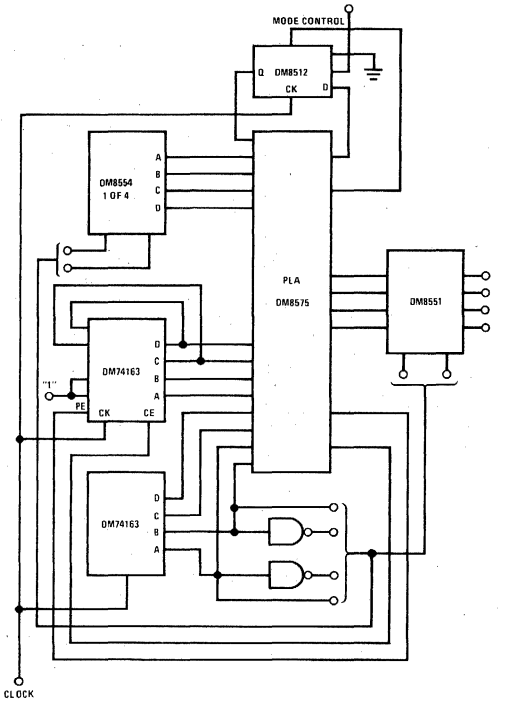


FIGURE 7.

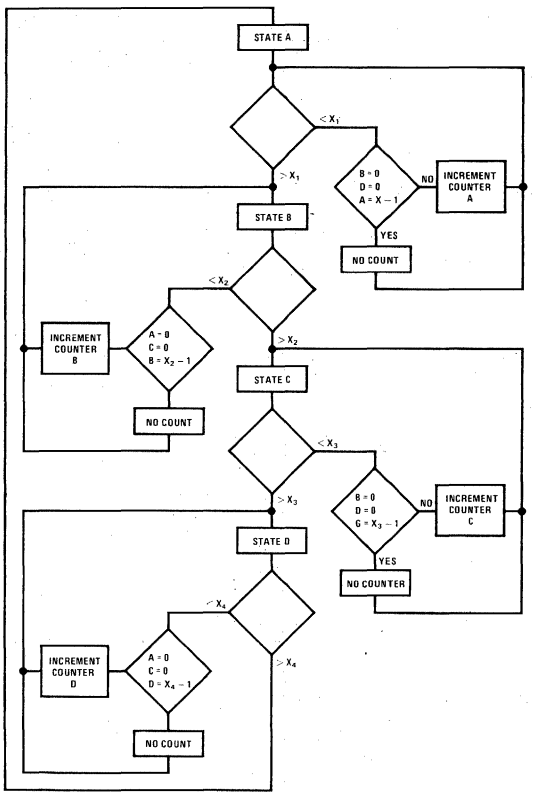


FIGURE 8.

Note that the state diagram Figure 8 shows that the maximum time interval X is checked to be greater than the present value of the A elapsed time counter. If this is true, the state counter indexes to the next machine state (state B). The output data transmitted to the holding memory (DM8551's in Figure 7) will be changed with every state step in the system. The four packages of holding memories are used to store the control information for the traffic indicators. The memories (DM8551's) are sequentially updated by using the same scan decoder which is used as a multiplex decode of remote traffic counters (DM85L54's).

The control coding developed allows a state interval to be shortened because one of the cross streets has detected on coming traffic. Also, the state interval can be lengthened if no cross or left turn traffic is detected. As the sequencer steps from state to state the other state conditions are tested. In other words, while in state B state conditions for A, C and D are tested for the necessary conditions which might modify the timing of state B. The four traffic counters which are shown in Figure 7 as DM8554 elements are multiplexed sequentially into the PLA sequencer controller where they are logically "ANDed" with present state timing. Using this information the sequencer period is modulated per the equations defined by the state equations.

It should be noted that the sequence order need not be orderly. The sequence of states through a complete cycle may have repeat intervals or jump commands in any step within the vastly variable complete sequence loop. There is no special requirement that the sequencer be designed with order in mind if some sort of disorder will yield an improvement in performance. The performance advantage may relate to a dynamic performance improvement or it may relate to a cost performance improvement. Generally a cost improvement results when fewer parts are required in the overall solution.

DESIGNING WITH A PLA

How should a PLA solution be developed? An orderly approach to the solution is necessary when the control word is wide and complex in form. The following techniques may be of some help in determining the decode combinations when using a PLA solution.

1. List all input control codes which are required for each output.
2. Reduce this list logically to minimize the number of partial product terms.
3. Combine similar terms which may be used on more than one output terminals.
4. Group outputs which can share the largest percentage of the same partial product terms.

There are some additional considerations with the general solution. Let's assume the following problem. The input control code is 14-bits wide and the output control word is 28-bits wide, Figure 9. This means that we would use four PLA's to generate the decoder solution if none of the packages required more than 96 partial product terms. In our example assume that there are four output codes which have 90 partial product solutions without considering the terms required by the four other output terminals of the PLA under question.

The initial thought about solving this problem, would suggest the use of an additional PLA with inputs and outputs connected together to obtain the extra product terms. Since the four PLA's have a total of 32 outputs and only 28 are required, the 4 unused additional outputs may be coupled from a second PLA to the PLA which first contained the 4 high usage partial product groups of terms (Figure 9).

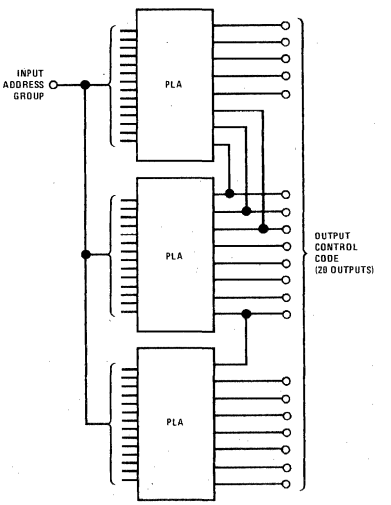


FIGURE 9.

Doing this allows half of the partial product terms to be placed in each of two separate PLA's. PLA's can be connected with common inputs and common outputs. It should be noted that the output code for the common terms must be programmed using a negative true logic for, since this permits "wire-OR'ing" the outputs. This very significant design possibility would not be allowed if standard ROM techniques are used.

This interesting observation shows that memory expansion for this product (PLA) is different than other memory elements. The normal Read Only Memory (ROM) or Random Access Memory (RAM) elements have chip select inputs which must be decoded and selected before the package is activated. When these types of memories are expanded, additional decoder logic elements are required to select the proper memory array Figure 4. In case where there are more than one output terminal,

it is necessary to activate the entire package group and therefore an entire memory word must be used for the address.

Neither of these conditions are necessary for the PLA. If the partial product does not exist as a decoder or programmed condition, the outputs do not change but if that product term does exist the outputs respond to the solution. In the PLA case it is possible for any one or combination of outputs to be selected from different but mutually connected packages (Figure 9). This element technique of grouping common control codes can simplify the solution. The technique may be used with multiple outputs to any degree which can prove economically efficient to the system design.

This last technique is a variation of items 3 and 4 in the design suggestions listed earlier. Utilization of this technique can result in significant improvements in memory storage efficiencies when compared different PLA solutions.

CONCLUSION

The two example applications, that of the control decoder within the digital processor and the traffic light sequencer, show the economic advantages of using the PLA because a reduction in circuit complexity and quantity results. The processor example application results also in an improvement in dynamic performance. Additionally both of these examples have a convenience of design which allows the system's work function to be modified without changing the overall system. Only a change of PLA programming need be accomplished to change the function of the decoder or controller system.

There are many more design ideas which will become apparent within your system when the PLA is applied to the system design. More design flexibility than that available with the ROM or random logic design can be achieved with the application of PLA elements to the system. The overall result will be more logic function per system dollar.

CUSTOM ROM PROGRAMMING

INTRODUCTION

Custom ROM programs are submitted to National in three formats: paper tape, punched cards or truth table with punched cards being the preferred. These programs are converted into machine language and outputted on a magnetic tape. This magnetic tape is used to make the programmable gate mask and the test tape. Wafers are held in inventory at gate mask. The wafers are then completed using the custom gate mask and tested at the wafer level. The wafer is then scribed and the good dice assembled. After assembly the units are tested using the custom test tape to assure the correct output pattern for every address.

When MOS was in its infancy the design engineers called a logic ONE a low voltage because a P-channel MOS transistor is turned on with a negative bias applied. This became known as NEGATIVE logic and was the opposite of TTL's POSITIVE logic. As the MOS technology evolved and TTL compatibility became a reality it became desirous to use the same logic in MOS as in TTL. Therefore the first ROMs to come out were specified in NEGATIVE logic and the new ROMs are specified in POSITIVE logic. Extra care must be taken in entering ROM codes that it is clear which logic level is used. National has programs to convert NEGATIVE logic to POSITIVE or POSITIVE to NEGATIVE so ROMs can be entered in either logic but the customer must specify which logic it is.

DEFINITIONS

Logic Definitions

NEGATIVE Logic: "0" = V_H = the more positive voltage. "1" = V_L = the more negative voltage.

POSITIVE Logic: "0" = V_L = the more negative voltage. "1" = V_H = the more positive voltage.

Input Output Definitions

Address: A_1 is the least significant input address on ROMs. L_0 is the least significant input address on character generators.

Outputs: B_1 is the least significant output.

INFORMATION NEEDED

So that National can better serve its customers the following information *must* be submitted with each ROM code.

National Semiconductor Corporation
2900 Semiconductor Dr., Santa Clara, CA 95051
Phone (408) 732-5000 TWX 910-339-9240

			NATIONAL PART NUMBER
			ROM LETTER CODE (NATIONAL USE ONLY)
NAME			DATE
ADDRESS			CUSTOMER PRINT OR I.D. NO.
CITY		STATE ZIP	PURCHASE ORDER NO.
TELEPHONE	NAME OF PERSON NATIONAL CAN CONTACT (PRINT)	AUTHORIZED SIGNATURE	DATE

TRUTH TABLE FORMS

Use the appropriate form for submitting truth tables.

Form I

MM3501	MM5204	MM4214/MM5214	MM4231/MM5231
MM5201	MM4210/MM5210	MM4220/MM5220	MM4232/MM5232
MM5202	MM4211/MM5211	MM4221/MM5221	MM4233/MM5233
MM4203/MM5203	MM4213/MM5213	MM4230/MM5230	

ADD-RESS	OUTPUT CODE NOTE: 1 B8	B7	B6	B5	B4	B3	B2	LSB B1	SUM
__ __0									
__ __1									
__ __2									
__ __3									
__ __4									
__ __5									
__ __6									
__ __7									
__ __8									
__ __9									
__ 10									
__ 11									
__ 12									
__ 13									
__ 14									
__ 15									
__ 16									
__ 17									
__ 18									
__ 19									
__ 20									
__ 21									
__ 22									
__ 23									
__ 24									
__ 25									
__ 26									
__ 27									
__ 28									
__ 29									
__ 30									
__ 31									
__ 32									
__ 33									
__ 34									
__ 35									
__ 36									
__ 37									
__ 38									
__ 39									
__ 40									
__ 41									
__ 42									
__ 43									
__ 44									
__ 45									
__ 46									
__ 47									
__ 48									
__ 49									
TB									

ADD-RESS	OUTPUT CODE B8	B7	B6	B5	B4	B3	B2	LSB B1	SUM
__ 50									
__ 51									
__ 52									
__ 53									
__ 54									
__ 55									
__ 56									
__ 57									
__ 58									
__ 59									
__ 60									
__ 61									
__ 62									
__ 63									
__ 64									
__ 65									
__ 66									
__ 67									
__ 68									
__ 69									
__ 70									
__ 71									
__ 72									
__ 73									
__ 74									
__ 75									
__ 76									
__ 77									
__ 78									
__ 79									
__ 80									
__ 81									
__ 82									
__ 83									
__ 84									
__ 85									
__ 86									
__ 87									
__ 88									
__ 89									
__ 90									
__ 91									
__ 92									
__ 93									
__ 94									
__ 95									
__ 96									
__ 97									
__ 98									
__ 99									
TB									

Note 1: The Appropriate Logic Level box must be checked or order will *not* be accepted.
- ☐ POSITIVE Logic on Addresses and Outputs
- ☐ NEGATIVE Logic on Addresses and Outputs

Note 2: The MM4232/MM5232 and MM4233/MM5233 have programmable chip selects and the logic level to enable the chip must be specified. CS 1 __ CS 2 __ CS 3 __ CS 4__

Note 3: TB is the total "1" bits in a column expressed in Decimal.

Note 4: SUM is the total "1" bits in a row expressed in Decimal.

Form II

MM5212
MM5215
MM4229/MM5229 (Positive logic only)

ADDRESS	OUTPUT CODE NOTE: 1 B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	LSB B1	SUM
__ __ 0													
__ __ 1													
__ __ 2													
__ __ 3													
__ __ 4													
__ __ 5													
__ __ 6													
__ __ 7													
__ __ 8													
__ __ 9													
__ 10													
__ 11													
__ 12													
__ 13													
__ 14													
__ 15													
__ 16													
__ 17													
__ 18													
__ 19													
__ 20													
__ 21													
__ 22													
__ 23													
__ 24													
__ 25													
__ 26													
__ 27													
__ 28													
__ 29													
__ 30													
__ 31													
__ 32													
__ 33													
__ 34													
__ 35													
__ 36													
__ 37													
__ 38													
__ 39													
__ 40													
__ 41													
__ 42													
__ 43													
__ 44													
__ 45													
__ 46													
__ 47													
__ 48													
__ 49													
TB													

ADDRESS	OUTPUT CODE NOTE: 1 B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	LSB B1	SUM
__ 50													
__ 51													
__ 52													
__ 53													
__ 54													
__ 55													
__ 56													
__ 57													
__ 58													
__ 59													
__ 60													
__ 61													
__ 62													
__ 63													
__ 64													
__ 65													
__ 66													
__ 67													
__ 68													
__ 69													
__ 70													
__ 71													
__ 72													
__ 73													
__ 74													
__ 75													
__ 76													
__ 77													
__ 78													
__ 79													
__ 80													
__ 81													
__ 82													
__ 83													
__ 84													
__ 85													
__ 86													
__ 87													
__ 88													
__ 89													
__ 90													
__ 91													
__ 92													
__ 93													
__ 94													
__ 95													
__ 96													
__ 97													
__ 98													
__ 99													
TB													

Note 1: The Appropriate Logic Level box must be checked or order will *not* be accepted.
- ☐ POSITIVE Logic on Address and Outputs
- ☐ NEGATIVE Logic on Address and Outputs

Note 2: The MM4229/MM5229 has programmable chip selects. Specify the Logic Level to enable the Chip (Positive Logic)
CS 1 ___ CS 2 ___ CS 3 ___

Note 3: TB is the total "1" bits in a column expressed in Decimal.

Note 4: SUM is the total "1" bits in a row expressed in Decimal.

Form III

MM4240/MM5240

CHARACTER ADDRESS (DECIMAL)	LINE ADDRESS (DECIMAL)	OUTPUT WORD B_1 B_2 B_3 B_4 B_5	SUM
_0	0 (000)		
	1 (001)		
	2 (010)		
	3 (011)		
	4 (100)		
	5 (110)		
	6 (110)		
	7 (111)		
_1	0 (000)		
	1 (001)		
	2 (010)		
	3 (011)		
	4 (100)		
	5 (110)		
	6 (110)		
	7 (111)		
_2	0 (000)		
	1 (001)		
	2 (010)		
	3 (011)		
	4 (100)		
	5 (110)		
	6 (110)		
	7 (111)		
_3	0 (000)		
	1 (001)		
	2 (010)		
	3 (011)		
	4 (100)		
	5 (110)		
	6 (110)		
	7 (111)		
	TB		

CHARACTER ADDRESS (DECIMAL)	LINE ADDRESS (DECIMAL)	OUTPUT WORD B_1 B_2 B_3 B_4 B_5	SUM
_4	0		
	1		
	2		
	3		
	4		
	5		
	6		
	7		
_5	0		
	1		
	2		
	3		
	4		
	5		
	6		
	7		
_6	0		
	1		
	2		
	3		
	4		
	5		
	6		
	7		
_7	0		
	1		
	2		
	3		
	4		
	5		
	6		
	7		
	TB		

CHARACTER ADDRESS (DECIMAL)	LINE ADDRESS (DECIMAL)	OUTPUT WORD B_1 B_2 B_3 B_4 B_5	SUM
_8	0		
	1		
	2		
	3		
	4		
	5		
	6		
	7		
_9	0		
	1		
	2		
	3		
	4		
	5		
	6		
	7		
	TB		

Note 1: A logic "1" = most negative voltage. A logic "0" = most positive voltage.

Note 2: Line address (L_0, L_1, L_2) are the row or column select lines in a character generator application. In a read only memory application, A_5 shall be considered the MSB and L_0 the LSB.

Note 3: TB is the total "1" bits in a column expressed in Decimal.

Note 4: SUM is the total "1" bits in a row expressed in Decimal.

The TO-5 ("H") package is rated at 750 mW still air (derate at 200°C/W above 25°C) soldered to PC board. This popular cavity package is recommended for small systems. Low cost (about 10 cents) clip-on heat sink increases driving capability by 50%.

The 8-pin ("N") molded mini-DIP is rated at 600 mW still air (derate at 90°C/W above 25°C) soldered to PC board (derate at 1.39W). Constructed with a special copper lead frame, this package is recommended for medium size commercial systems particularly where automatic insertion is used. (Please note for prototype work, that this package is only rated at 600 mW when mounted in a socket and not one watt until it is soldered down.)

To TO-8 ("G") package is rated at 1.5W still air (derate at 100°C/W above 25°C) and 2.3W with clip-on heat sink (Wakefield type 215-1.9 or equivalent-derate at 15 mW/°C). Selected for its power handling capability and moderate cost, this hermetic package will drive very large systems at the lowest cost per bit.

Additional information is given in the section of this data book on Maximum Power Dissipation (page 2).

Power Dissipation Considerations

The amount of registers that can be driven by a given clock driver is usually limited first by internal power dissipation. There are four factors:

1. Package and heat sink selection
2. Average dc power, P_{DC}
3. Average ac power, P_{AC}
4. Numbers of drivers per package, n

From the package heat sink, and maximum ambient temperature one can determine P_{MAX}, which is the maximum internal power a device can handle and still operate reliably. The total average power dissipated in a driver is the sum of dc power and ac power in each driver times the number of drivers. The total of which must be less than the package power rating.

$$P_{DISS} = n \times (P_{AC} + P_{DC}) \leq P_{MAX} \qquad (1)$$

Average dc power has three components: input power, power in the "OFF" state (MOS logic "0") and power in the "ON" state (MOS logic "1").

$$P_{DC} = P_{IN} + P_{OFF} + P_{ON} \qquad (2)$$

For most types of clock drivers, the first two terms are negligible (less than 10 mW) and may be ignored.

Thus:

$$P_{DC} \cong P_{ON} = \frac{(V^+ - V^-)^2}{Req} \times (DC)$$

where:

$V^+ - V^-$ = Total voltage across the driver

Req = Equivalent device resistance in the "ON" state

$$= V^+ - V^-/I_{S(ON)} \qquad (3)$$

DC = Duty Cycle

$$= \frac{\text{"ON" Time}}{\text{"ON" Time + "OFF" Time}}$$

For the DS0025, Req is typically 1 kΩ while Req is typically 600Ω for the DS0026. Graphical solutions for P_{DC} appear in *Figure 1.* For example if V^+ = +5V, V^- = −12V, Req = 500 Ω, and DC = 25%, then P_{DC} = 145 mW. However, if the duty cycle was only 5%, P_{DC} = 29 mW. Thus to maximize the number of registers that can be driven by a given clock driver as well as minimizing average system power, the minimum allowable clock pulse width should be used for the particular type of MOS register.

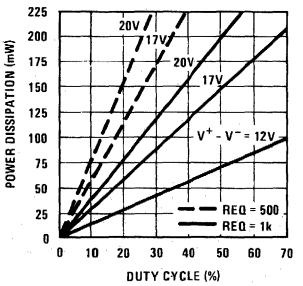


FIGURE 1. P_{DC} vs Duty Cycle

In addition to P_{DC}, the power driving a capacitive load is given approximately by:

$$P_{AC} = (V^+ - V^-)^2 \times f \times C_L \qquad (4)$$

where:

f = Operating frequency

C_L = Load capacitance

Graphical solutions for P_{AC} are illustrated in *Figure 2.* Thus, any type of clock driver will dissipate internally 290 mW per MHz per thousand pF of load. At 5 MHz, this would be 1.5W for a 1000 pF load. For long shift register applications, the driver with the highest package power rating will drive the largest number of bits.

NATIONAL

APPLYING MODERN CLOCK DRIVERS TO MOS MEMORIES

INTRODUCTION

MOS memories present unique system and circuit challenges to the engineer since they require precise timing of input wave forms. Since these inputs present large capacitive loads to drive circuits, it is often that timing problems are not discovered until an entire system is constructed. This paper covers the practical aspects of using modern clock drivers in MOS memory systems. Information includes selection of packages and heat sinks, power dissipation, rise and fall time considerations, power supply decoupling, system clock line ringing and crosstalk, input coupling techniques, and example calculations. Applications covered include driving various types shift registers and RAM's (Random Access Memories) using logical control as well as other techniques to assure correct non-overlap of timing waveforms.

Although the information given is generally applicable to any type of driver, monolithic integrated circuit drivers, the DS0025, DS0026 and DS0056 are selected as examples because of their low cost.

The DS0025 was the first monolithic clock driver. It is intended for applications up to one megacycle where low cost is of prime concern. Table I illustrates its performance while Appendix I describes its circuit operation. Its monolithic, rather than hybrid or module construction, was made possible by a new high voltage-gold doped process utilizing a collector sinker to minimize $V_{CE\,SAT}$.

The DS0026 is a high speed, low cost, monolithic clock driver intended for applications above one megacycle. Table II illustrates its performance characteristics while its unique circuit design is presented in Appendix II. The DS0056 is a variation of the DS0026 circuit which allows the system designer to modify the output performance of the circuit. The DS0056 can be connected (using a second power supply) to increase the positive output voltage level and reduce the effect of cross coupling capacitance between the clock lines in the system. Of course the above are just examples of the many different types that are commercially available. Other National Semiconductor MOS interface circuits are listed in Appendix III.

The following section will hopefully allow the design engineer to select and apply the best circuit to his particular application while avoiding common system problems.

PRACTICAL ASPECTS OF USING MOS CLOCK DRIVERS

Package and Heat Sink Selection

Package type should be selected on power handling capability, standard size, ease of handling, availability of sockets, ease or type of heat sinking required, reliability and cost. Power handling capability for various packages is illustrated in Table III. The following guidelines are recommended:

TABLE I. DS0025 Characteristics

PARAMETER	CONDITIONS ($V^+ - V^-$) = 17V	VALUE	UNITS
t_{ON}		15	ns
t_{OFF}	C_{IN} = 0.0022μF, R_{IN} = 0Ω	30	ns
t_r	C_L = 0.0001μF, R0 = 50Ω	25	ns
t_f		150	ns
Positive Output Voltage Swing	$V_{IN} - V^-$ = 0V, I_{OUT} = −1mA	$V^+ - 0.7$	V
Negative Output Voltage Swing	I_{IN} = 10mA, I_{OUT} = 1mA	$V^- + 1.0$	V
On Supply Current (V^+)	I_{IN} = 10 mA	17	mA

TABLE II. DS0026 Characteristics

PARAMETER	CONDITIONS ($V^+ - V^-$) = 17V	VALUE	UNITS
t_{ON}		7.5	ns
t_{OFF}	C_{IN} = 0.001μF, R_{IN} = 0Ω	7.5	ns
t_r	R0 = 50Ω, C_L = 1000 pF	25	ns
t_f		25	ns
Positive Output Voltage Swing	$V_{IN} - V^-$ = 0V, I_{OUT} = −1mA	$V^+ - 0.7$	V
Negative Output Voltage Swing	I_{IN} = 10mA, I_{OUT} = 1mA	$V^- + 0.5$	V
On Supply Current (V^+)	I_{IN} = 10 mA	28	mA

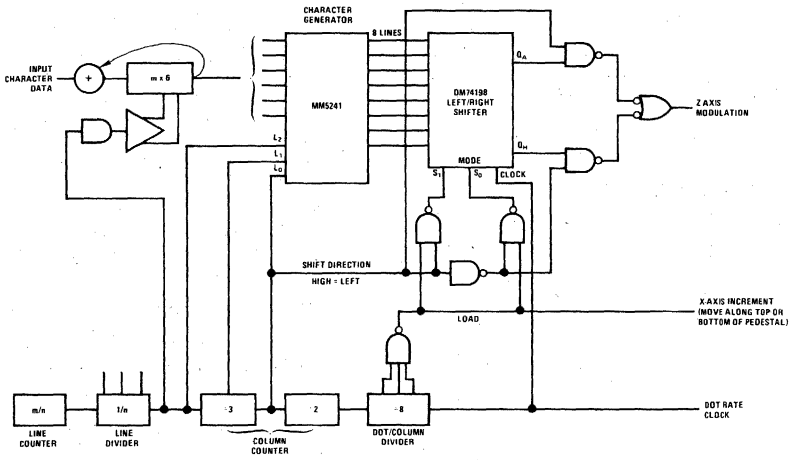


FIGURE 14. Conversion of Sawtooth Output to Pedestal Scan

CUSTOM FONTS

The two ROMs can also be custom-programmed to provide special characters, or fonts larger than 5 x 7. The MM4240/MM5240 actually stores 64 5 x 8 characters or character segments and the MM4241/MM5241 stores 64 8 x 6 characters or segments. They are not limited to 5 x 7 and 7 x 5. For example, the extra height may be used in an otherwise 5 x 7 font to drop the tails of commas, semicolons and lower-case letters below the bottom line of the capital letters. Fonts as large as 16 x 12 are entirely practical without additional control logic, using the chip-enable feature of four MM5241s. Large-font organizations are discussed in AN-40.

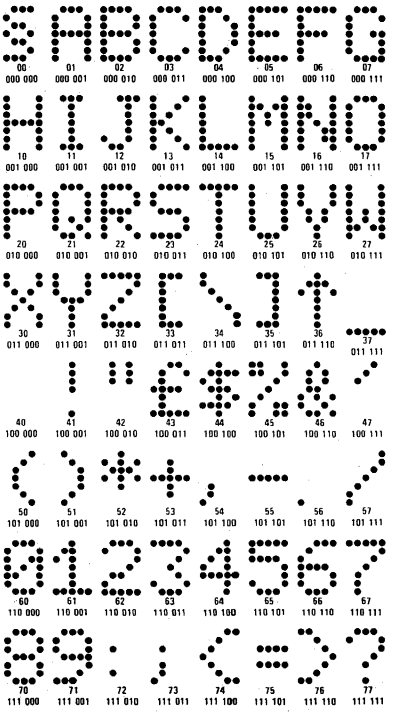


FIGURE 11. MM4241ABX/MM5241ABX Vertical-Scan ECMA-7 Font for General European Use (French, British, Italian)

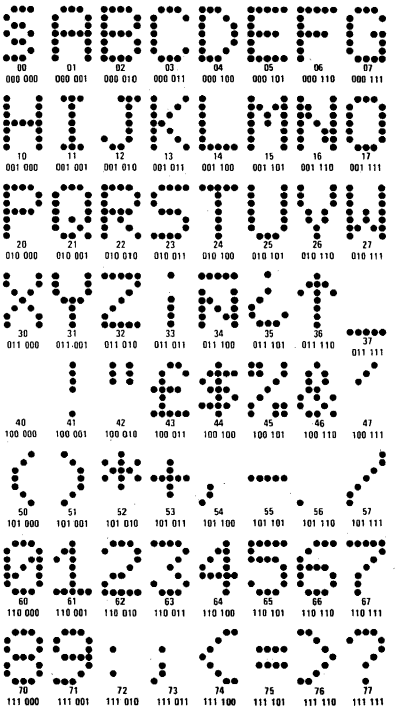


FIGURE 12. MM4241ABY/MM5241ABY Vertical-Scan ECMA-7 Font for Spanish Use

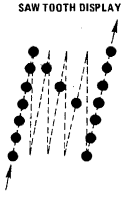


FIGURE 13a. Sawtooth Vertical Scan

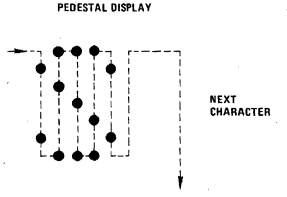


FIGURE 13b. Pedestal Vertical Scan

Form IV

MM4241/MM5241

CE_1

CHARACTER ADDRESS (DECIMAL)	LINE ADDRESS DECIMAL	LSB B1	B2	B3	B4	B5	B6	B7	B8	SUM
_0	0 ($L_2 L_1 L_0$ 0 0 0)									
	1 (0 0 1)									
	2 (0 1 0)									
	3 (0 1 1)									
	4 (1 0 0)									
	5 (1 1 0)									
_1	0 (0 0 0)									
	1 (0 0 1)									
	2 (0 1 0)									
	3 (0 1 1)									
	4 (1 0 0)									
	5 (1 1 0)									
_2	0 (0 0 0)									
	1 (0 0 1)									
	2 (0 1 0)									
	3 (0 1 1)									
	4 (1 0 0)									
	5 (1 1 0)									
_3	0 (0 0 0)									
	1 (0 0 1)									
	2 (0 1 0)									
	3 (0 1 1)									
	4 (1 0 0)									
	5 (1 0 1)									
_4	0									
	1									
	2									
	3									
	4									
	5									
	TB									

CE_2

CHARACTER ADDRESS (DECIMAL)	LINE ADDRESS DECIMAL	LSB B1	B2	B3	B4	B5	B6	B7	B8	SUM
_5	0									
	1									
	2									
	3									
	4									
	5									
_6	0									
	1									
	2									
	3									
	4									
	5									
_7	0									
	1									
	2									
	3									
	4									
	5									
_8	0									
	1									
	2									
	3									
	4									
	5									
_9	0									
	1									
	2									
	3									
	4									
	5									
	TB									

Note 1: On the character address and output word negative logic is used:
A logic "1" most negative voltage
A logic "0" most positive voltage
on the line address positive logic is used:
A logic "0" most negative voltage
A logic "1" most positive voltage

Note 2: Line address (L_0, L_1, L_2) are the column select lines in a character generator application. In a read only memory application A_6 shall be considered the MSB and L_0 the LSB.

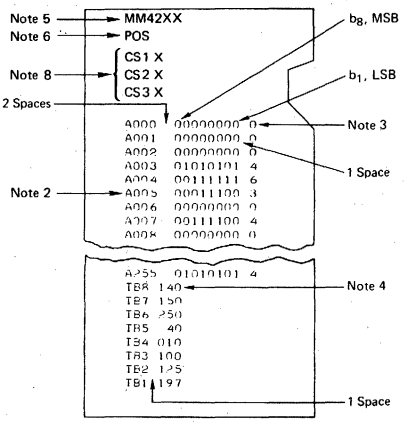
Note 3: TB is the total "1" bits in a column expressed in Decimal.

Note 4: SUM is the total "1" bits in a row expressed in Decimal.

TAPE ENTRY FORMAT

Tape format for the following ROMs.

MM3501	MM4214/MM5214	MM4231/MM5231
MM4210/MM5210	MM4220/MM5220	MM4232/MM5232
MM4211/MM5211	MM4221/MM5221	MM4233/MM5233
MM4213/MM5213	MM4230/MM5230	



8-BIT TAPE FORMAT

Note 1: The code is a 7-bit ASCII code on 8 punch tape.

Note 2: The ROM input address is expressed in decimal form and is preceded by the letter A.

Note 3: The total number of "1" bits in the output word.

Note 4: The total number if "1" bits in each output column or bit position.

Note 5: Specify product type.

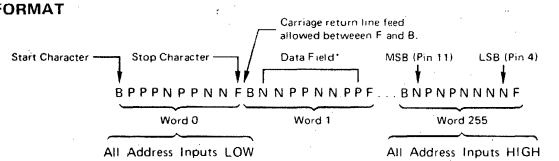
Note 6: Must type POS logic, or NEG logic depending on which is used.

Note 7: LOGIC ON ADDRESS AND OUTPUTS must be the same (either POS or NEG).

Note 8: Specify the pattern necessary to enable the ROM on the ROMS that need chip selects.

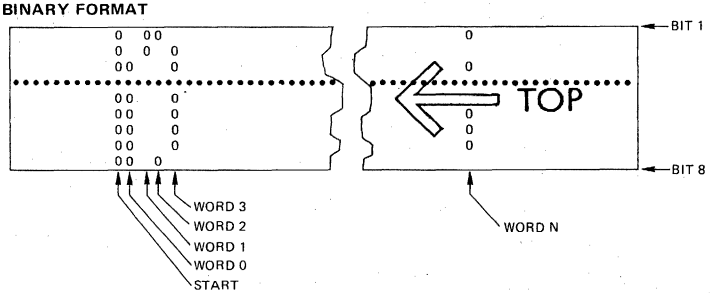
Tape format for the MM5202, MM4203/MM5203 and MM4204/MM5204.

PROM TAPE P AND N FORMAT



*Data Field: Must have only P's or N's typed between B and F. No nulls or rubouts. Must have exactly eight P and N characters between B and F. Any characters except B and F may be typed between the F stop character and the B start be rubbed out. Data for exactly 256 words must be entered, beginning with word 0. P = "1" or the more positive voltage. N = "0" or most negative voltage. When the MM4204/MM5204 is used the word length is 512.

PROM TAPE BINARY FORMAT



Note 1: Tape must be all blank except for the 513 words punched.

Note 2: Tape must start with a START punch.

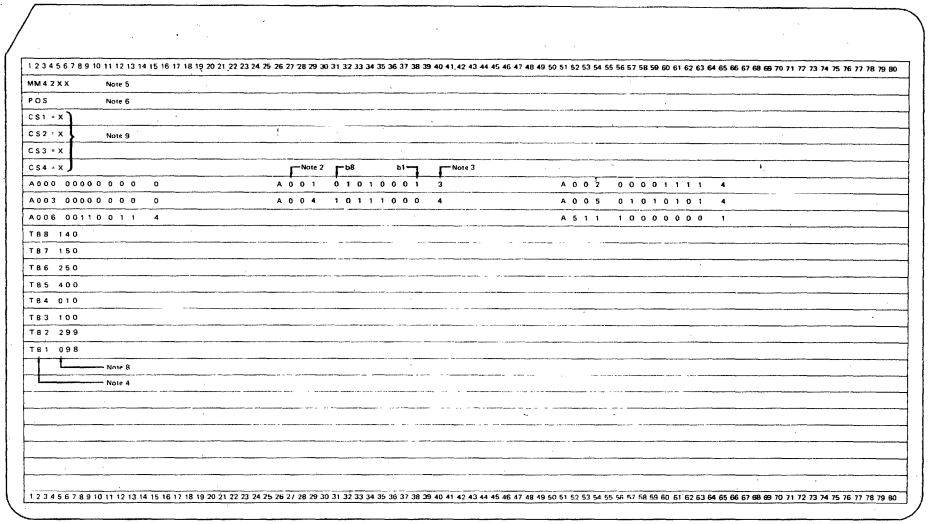
Note 3: Data is comprised of two words the first being the actual Data the second being the complement of the data.

Note 4: A punch is equal to a "1" or most positive voltage and the omission of a punch is a "0" or the more negative voltage.

When programming the MM5202 or MM4203/MM5203 it should be remembered that the opposite logic from what is programmed will appear on the output of the PROM. In otherwords a P on the tape will program a Logic "0" or V_L in the PROM.

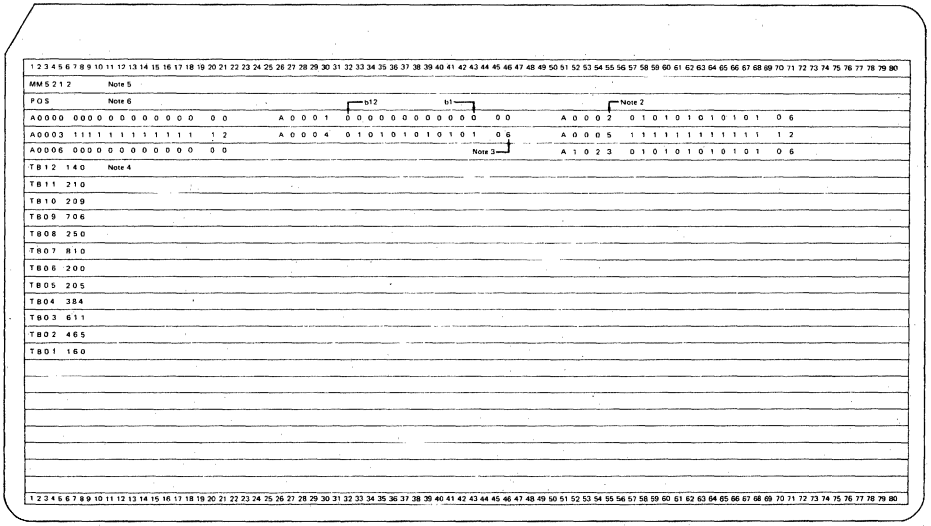
CARD ENTRY FORMAT

Card format for the: MM3501, MM4210/MM5210, MM4211/MM5211, MM4213/MM5213, MM4214/MM5214, MM4220/MM5220, MM4221/MM5221, MM4230/MM5230, MM4231/MM5231, MM4232/MM5232, MM4233/MM5233



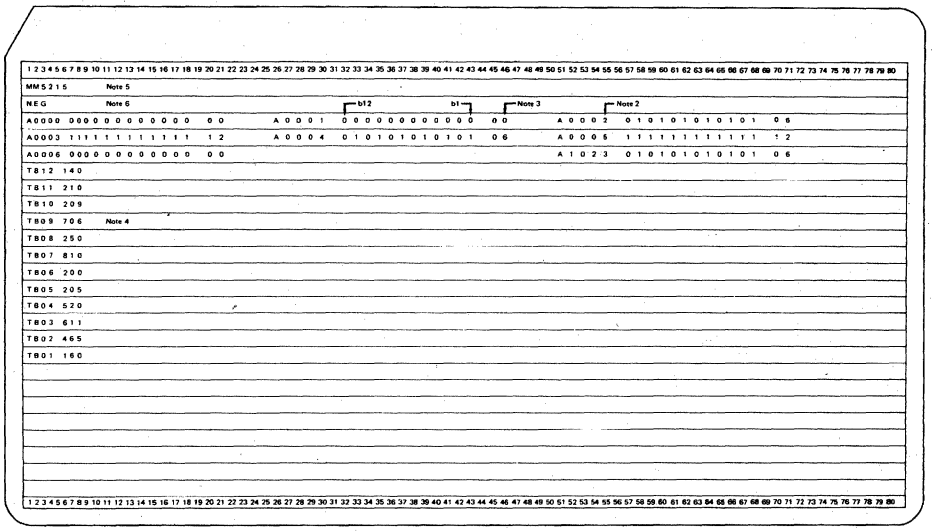
Note 1: Punch three input addresses per card with the first address in columns 1–25, the second in columns 26–50 and the third in columns 51–80.
Note 2: The ROM input address is expressed in decimal form and is preceded by the letter A.
Note 3: The total number of "1" bits in the output word.
Note 4: The total number if "1" bits in each output column or bit position.
Note 5: Specify product type.
Note 6: Must type POS logic or NEG logic depending on which is used.
Note 7: LOGIC ON ADDRESS, OUTPUTS AND CHIP ENABLE must be the same (either POS or NEG).
Note 8: Leading zeros must be punched.
Note 9: Specify the Chip Select Logic Levels that will enable the ROM where necessary.

Card format for the MM5212.



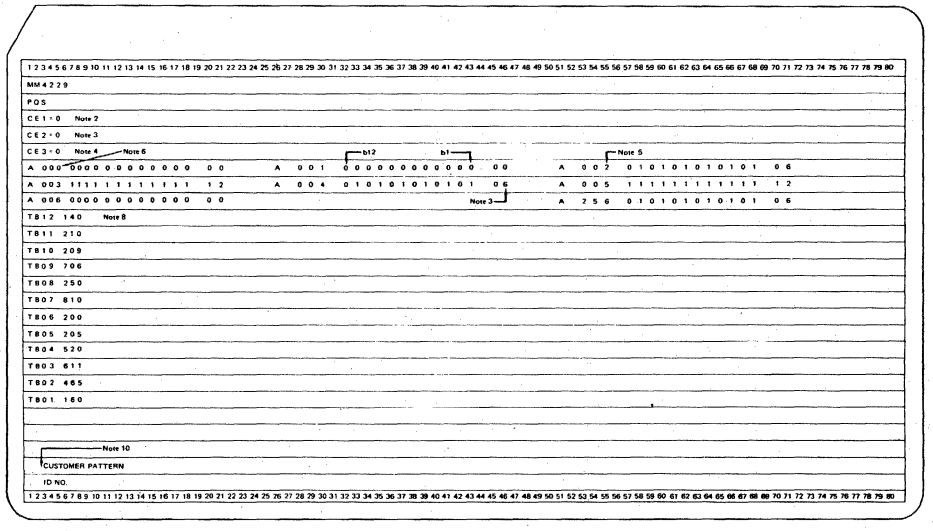
Note 1: Punch three input addresses per card with the first address in columns 1–25, the second in columns 26–50 and the third in columns 51–80.
Note 2: The ROM input address is expressed in decimal form and is preceded by the letter A.
Note 3: The total number of "1" bits in the output word.
Note 4: The total number if "1" bits in each output column or bit position.
Note 5: Specify product type.
Note 6: Must type POS logic.
Note 7: POSITIVE LOGIC ON ADDRESS AND OUTPUTS.
Note 8: "1" more positive output, "0" more negative output.
Note 9: Leading zeroes must be punched.

Card format for the MM5215.



Note 1: Punch three input addresses per card with the first in columns 1–25, the second in columns 26–50, and the third in columns 51–80.
Note 2: The ROM input address is expressed in decimal form and is preceded by the letter A.
Note 3: The total number of "1" bits in the output word.
Note 4: The total number if "1" bits in each output column or bit position.
Note 5: Specify product type.
Note 6: Must type negative logic.
Note 7: NEGATIVE LOGIC ON ADDRESS AND OUTPUTS.
Note 8: "1" more negative output. "0" more positive output.
Note 9: Leading zeroes must be punched.

Card format for the MM4229/MM5229.



Note 1: The code is Hollerith as punched on IBM Model 029.
Note 2: Corresponds to Pin 16
Note 3: Corresponds to Pin 15
Note 4: Corresponds to Pin 14
Note 5: The ROM input address is expressed in decimal form and is preceded by the letter A.
Note 6: All 256 address (0-255) must be coded.
Note 7: The total number of "1's" in each input word.
Note 8: The total number of "1's" in each output column.
Note 9: Leading zeros must be punched.
Note 10: The customer may use his own ID designation if he does not punch the first column.
Note 11: Positive logic on address and outputs "1" more positive voltage "0" more negative voltage.

NATIONAL

DESIGNING MEMORY SYSTEMS USING THE MM5262

INTRODUCTION

The objective of this application note is to describe, in detail, the operation of the MM4262/MM5262 Dynamic 2K P-channel silicon gate RAM and how to apply this RAM in designing memory systems. Specifically the topics to be covered are:

I. Detail description of operation of MM4262/MM5262

II. Memory Systems Application of MM4262/MM5262

- A. Interface
- B. System Timing
- C. Refresh Requirements
- D. Power Considerations
- E. Printed Circuit Layout Considerations

III. A 16K x 10 Memory Application Example

Although the MM4262/MM5262 device is being used as the primary example, many of the topics discussed are of general application to the design of memory systems.

I. Detail Description of Operation of MM4262/MM5262

The MM4262/MM5262 is a 2048 x 1 random access read/write dynamic MOS memory. "2048 x 1" says the device is organized as 2048 words with each word containing one bit. "Random access" says that words may be accessed in any sequence. "Read/write" says that information can be read from the memory or written into the memory. "Dynamic" says the information is stored in the form of voltages on capacitors. Lastly "MOS" says the device is manufactured using Metal-Oxide-Semiconductor technology.

Inputs consist of eleven address inputs ($2^{11} = 2048$), Chip Select, Read/Write Control, Data In, three clocks and three power supplies. All inputs except clocks and power supplies can be driven by standard TTL circuits. The power supplies are nominally $V_{DD} = -15V$, $V_{SS} = +5V$ and $V_{BB} = +8.5V$. The clocks swing from V_{DD} to V_{SS} nominally. There is one output which sources current.

A logic diagram for the MM4262/MM5262 is shown in *Figure 1*. Because dynamic logic is difficult to represent in standard logic symbols it is necessary to show actual transistors in some cases. Further, the internal logic is shown in negative logic notation. In this notation a logic "1" is the most negative voltage level and a logic "0" is the most positive voltage level. This is opposite to the normal TTL logic convention. It may seem, at first, that this change in logic convention introduces unneccessary confussion, particularly since all inputs and outputs to the MM4262/MM5262 are specified using standard TTL logic convention. However, once the negative logic convention is accepted and inputs are translated to this convention it will be much easier to understand the internal operation of the MM4262/MM5262.

To aid in this translation *Table 1* shows inputs and outputs in TTL positive logic format and in the negative logic format used in *Figure 1*. See page 11.

	TTL Positive Logic Notation ($V_{DD} = -15V$, $V_{SS} = +5V$)		Negative Logic Notation Used In Figure 1 ($V_{DD} = -15V$, $V_{SS} = +5V$)	
	Voltage Level	Logic Level	Voltage Level	Logic Level
Inputs	3.5V to 6V	1	3.5V to 6V	0
	−5V to 0.8V	0	−5V to 0.8V	1
Outputs	$\geqslant 500\mu A$ @ 1.8V	1	$\geqslant 500\mu A$ @ 1.8V	0
	$\leqslant 100\mu A$ @ 0V	0	$\leqslant 100\mu A$ @ 0V	1
Clocks	4V to 6V	1	4V to 6V	0
	−16V to −14V	0	−16V to −14V	1
Internal Levels	5V	1	+5V	0
	−15V	0	−15V	1

Table 1

Using the negative logic notation described in *Table 1* a logic "1" (−15V) applied to gate of an MOS transistor will cause that transistor to turn on giving a low impedance between the drain and source terminals, while a logic "0" will cause that transistor to turn off giving a high impedance between the drain and source terminals.

Detail A, shown in *Figure 1*, shows the basic memory cell used in the MM4262/MM5262. Information is written into the cell and read out of the cell via the column line X_N. The Write and Read operation are controlled by the two row lines, Y_{MW} and Y_{MR} respectively. Information is stored in the cell as a voltage level on capacitor C_A.

At ϕ_1 time, ϕ_1 clock at logic "1", all X lines are precharged to a "1" level by the transistors labeled Q1. This "1" level is maintained by the capacitance of the X lines until it is conditionally discharged by the cells of the selected row.

The conditional discharge of the X lines takes place when Y read line, Y_{MR}, goes to a logic "1" turning on Q_{A2}. If a logic "1" is stored on capacitor C_A, Q_{A3} is conducting, allowing the X_N line to discharge to V_{SS} (+5V). If, on the other hand, a logic "0" is stored on capacitor C_A, Q_{A3} is not conducting and the X_N line will maintain the logic "1" level established during $\phi 1$ time. Note that information being read out of the selected cells on the X lines is of the opposite level as that stored on capacitor C_A.

Although the information from only one cell will be output from the RAM, when the Y_{MR} line of a particular row is taken to a logic "1", all 64 X lines will assume the complement of the data stored in the 64 memory cells of that row. This characteristic is fundamental to the refresh operation of the MM4262/MM5262 and will be discussed in the following text.

The Write operation is controlled by the Y write line, Y_{MW}. When Y_{MW} of a particular row goes to a logic "1" level Q_{A1} conducts charging the storage capacitance, C_A, to the same logic state that existed on the X_N line prior to Y_{MW} going to a logic "1". Note that when the Y_{MW} line of a particular row goes to a logic "1" the information on the 64 X lines will be transferred to the 64 cells of the selected row.

Since the information is stored as a voltage on a capacitor this voltage must be restored or "refreshed" periodically or leakage currents will cause its loss. As described above information can be read out of a cell on to its corresponding X line and also can be read from the X line back to the storage capacitor, C_A. Referring to *Figure 1*, the row lines Y_{MR} and Y_{MW} (M = 1 through 32) are driven by transistors Q_3 and Q_4 respectively. Address inputs A_0 through A_4 select which row is to be driven by taking the gates of Q_3 and Q_4 to a logic "1". As can be seen from the logic diagram the Y Read line of the selected row will go to a logic "1" when ϕ_2 is a logic "1" and the Y Write line will go to a logic "1" when ϕ_3 is a logic "1".

In order for the MM4262/MM5262 to operate properly the clocks ϕ_1, ϕ_2, and ϕ_3 must be applied in sequence. Also, as can be seen from the above description of its operation, the clocks must not overlap one another. For instance, if ϕ_1 and ϕ_2 were both on simultaneously, the X_N lines could not be discharged properly by the memory cell transistors, Q_{A2} and Q_{A3}. If ϕ_2 and ϕ_3 were on together, the memory cell would quickly lose the information stored there.

The refresh of a row will then be accomplished when the clocks ϕ_1, ϕ_2 and ϕ_3 are applied in sequence. The sequence of events would occur as follows:

(1) All X lines are precharged to a logic "1" at ϕ_1 time.

(2) The complement of the data stored on the cell capacitors of the selected row, is stored on the X lines at ϕ_2 time.

(3) The information stored on the X lines is written back into the cells of the selected row at ϕ_3 time.

There is then only one remaining question to resolve. The above refresh cycle restores not the original voltage stored on capacitor C_A, but its complement. When the information is eventually read out of the cell, how can we tell if the cell contains a logic "1" or "0", since the voltage alternates with each application of the ϕ_3 clock? The answer is the Dummy Cell shown in detail B of *Figure 1*.

There are 32 Dummy Cells, one for each row. The output, DC, of the Dummy Cell corresponds to the X_N line of the memory cell. Like X_N of a memory cell, DC is precharged to a "1" level at ϕ_1 time (through Q_5). Since the Y_{MR} and Y_{MW} lines are the same for the Dummy Cell and its corresponding row, the output, DC, of the Dummy Cell will alternate between a logic "1" and a logic "0" each time the ϕ_1, ϕ_2, and ϕ_3 clocks are applied. As will be discussed, the output, DC, is used to complement or not complement the input and output information. The Dummy Cell is equivalent to a one bit counter and determines if the row has been complemented an even or an odd number of times. Since DC is changing in synchronism with all memory cells in its corresponding row, the voltage out of any cell will be properly interpreted logically to the outside world.

The description of the basic memory storage mechanism is now complete. All that remains is a description of the circuitry required to transfer information into and out of a particular cell. In order to understand the input/output circuitry, it is necessary to specify the timing

requirements of the MM4262/MM5262. *Figure 2* shows these timing requirements. The necessity of non-overlapping clocks has already been discussed. The timing diagram quantitatively shows this with the timing intervals T_{12}, T_{23} and T_{31}. In general, it requires a certain amount of time for information to propagate through the internal logic elements. This propagation time limits the minimum allowable clock pulse widths (T_{1PW}, T_{2PW} and T_{3PW}) and the minimum allowable time between clocks (T_{12}, T_{23} and T_{31}). Input signals in general must be in a stable logic state prior to a clock edge, input set up time, and after a clock edge, input hold time. These signals are subscripted "S" (set up) and "H" (hold) respectively on the timing diagram. Set up and hold times are also determined by internal propagation delays.

All timing conditions, as specified in the MM4262/MM5262 data sheet, must be adherred to for the proper operation of this device. This seems like an obvious statement, but in cases of malfunction it is often found that incorrect timing and/or voltage levels are the cause.

Up to this point, the description of the MM4262/MM5262 has proceeded from the inside out, so to speak. Changing our perspective at this time will make the description of the input/output circuitry more easily understood. To do this, let us consider the basic functional blocks of this, and almost any other RAM for that matter.

The basic functional blocks are: (1) Input Address Buffer, (2) Input Data Buffer, (3) Write Circuit, (4) Row Decoder, (5) Column Decoder, (6) Memory Storage Array, (7) Sense Circuit and (8) Output Data Buffer.

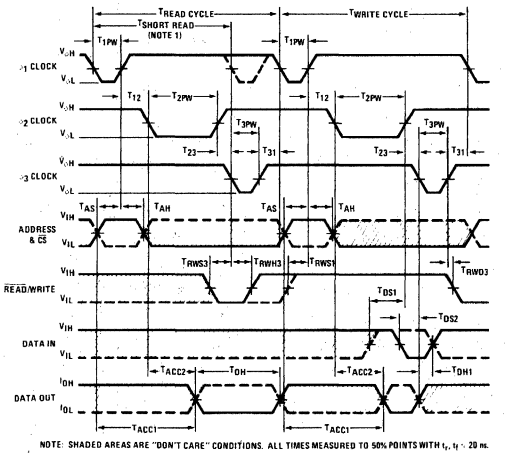


FIGURE 2. Timing Diagram for MM4262/MM5262

Any of the basic functional blocks is simple taken by itself. When considered in total, they only seem complex. Let us examine each, for the MM4262/MM5262, in turn:

(1) **Input Address Buffer**

Addresses A_0 through A_{10} and $\overline{CS}$ are strobed into latches by the ϕ_1 clock. The latches hold the address and chip select information fixed until the next ϕ_1 clock updates them. The true and complement of address and chip select inputs are available at the latch outputs. The Input Address Buffer also converts from TTL voltage levels to MOS voltage levels required by the internal circuitry.

(2) **Input Data Buffer**

The Input Data Buffer converts TTL input voltage levels to MOS voltage levels and gates the input data to the Write Circuit. The gating of input data is controlled by the $\overline{CS}$, $\overline{R}/W$ and ϕ_3 inputs and the output of the Dummy Cell, DC. When DC is a logic "0", the complement of the input data is written into the selected cell. When DC is a logic "1", the input data is written into the selected cell in the same logic sense in which it appears on the input pin.

(3) **Write Circuit**

The Write Circuit is driven by the Input Data Buffer and in turn drives the DS lines. The Memory is divided into four quadrants. Each quadrant contains 512 bits of storage capacity. There is a separate Write Circuit for each quadrant. The inputs of the four Write Circuits are tied together.

(4) **Row Decoder**

The Row Decoder decodes address inputs A_0 through A_4 into one of the 32 rows. The output of the five input NOR gate, of the selected row, goes to a logic "1", gating on transistors labeled Q_3 and Q_4. Information is then read from or written into the cells of that row, at ϕ_2 and ϕ_3 time, as previously described.

(5) **Column Decoder**

The Column Decoder decodes address inputs A_5 through A_{10} into one of 64 columns. The output of the six input NOR gate, of the selected column, goes to a logic "1" at ϕ_1 time turning on the transistor labeled Q_2. Turning on Q_2 will connect the selected X line to its appropriate DS line. As discussed previously, the X lines are precharged to a logic "1" at ϕ_1 time and, as will be seen, the sense amplifier also charges the DS line to a logic "1" at ϕ_1 time. At ϕ_2 time, information from the selected cell is input to the sense circuit via the selected X line through Q_2 and the DS line. At ϕ_3

time data is written into the selected cell from the Write Circuit via the DS line, Q_2 and the appropriate X line.

(6) **Memory Storage Array**

The Memory Storage Array contains 2048 memory cells (detail A) and is arranged in 32 rows and 64 columns. This array is subdivided into four quadrants of 16 rows and 32 columns (512 memory cells) each. The subdivision is necessary only to facilitate circuit layout and improve performance due to parasitic elements. It has no functional significance. The operation of the storage array has been discussed previously.

(7) **Sense Circuit**

The Sense Circuit is designed such that the DS lines are forced to a logic "1" and $\overline{DS}$ lines to a logic "0" at ϕ_1 time. Information from the DS lines is strobed and latched by the Sense Circuit at ϕ_2 time. The DS outputs of the Sense Circuits drive the Output Data Buffer.

(8) **Output Data Buffer**

The Output Data Buffer converts the output data from MOS levels to the output current levels specified on the data sheet. Three of the DS lines, from the three quadrants not selected, will be at a logic "0" level. The fourth DS line, from the selected quadrant, will be gated to the output in the same logic sense when DC is a logic "1", and complemented when DC is a logic "0".

The three clocks are obviously fundamental to the operation of the MM4262/MM5262. It is helpful to think of them in terms of the functions they control. These functions are:

ϕ_1 — Latches input addresses and precharges internal nodes.

ϕ_2 — Reads information from selected cells.

ϕ_3 — Writes information into selected cells.

II. Memory System Application of the MM4262/MM5262

A. Interface

In applying the MM4262/MM5262 device to any system three distinct types of interface must be considered. The inputs, the output and the clocks each has unique interface requirements.

The inputs are TTL compatible. Let's look in detail at what "TTL compatible" means. It does not mean that the user can drive the MM4262/MM5262 inputs with any TTL gate without giving it another thought. "TTL compatible" means that the MM4262/MM5262 can be driven by TTL, if done properly, without the need of voltage translation.

The hooker is of course, "if done properly." What is proper? The worst case TTL "0" level is 0.4 volts maximum when sinking 16 mA. The MM4262/MM5262 does not require any current sink, except for leakage, and its "0" level input voltage is 0.8 volts leaving 0.4 volts for noise margin. Clearly the TTL "0" level is no problem. The "1" level is not so straight forward. A worst case TTL "1" level is 2.4 volts and at V_{SS} = 5 volts the MM4262/MM5262 requires a minimum of (V_{SS} −1.5) = 3.5 volts as an input "1" level. Clearly this is in conflict. However an examination of the worst case TTL "1" level specification in more detail will make this picture considerably brighter.

Figure 3 is the schematic of a typical TTL gate. The "1" level output voltage is: $V_{out}(1) = V_{CC} - (I_{C2} \times 1.6K + V_{BE}(Q3) + V_{D1})$. With transistor Q_2 turned off Q_4 will be off and with no dc load on the output, $I_{C2} = 0$. The one level output voltage is then: $V_{out}(1) = V_{CC} - V_{BE}(Q3) - V_{D1}$. At 25°C $V_{BE}(Q3)$ and V_{D1} will be approximately 0.7 volts. The TTL "1" level output is $V_{out}(1) = V_{CC} - 1.4$ volts, giving 0.1 volts of noise margin. It is important to note that even though TTL "1" levels are specified as absolute voltages they actually follow the V_{CC} supply.

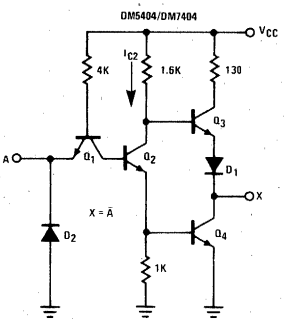


FIGURE 3. Typical TTL Gate

Under what conditions will the "1" level output of a TTL gate equal 2.4 volts? Several conditions have to exist simultaneously. For a military grade part (−55°C to +125°C) the "1" level output will equal 2.4 volts, when V_{CC} = 4.5 volts, $V_{in}(0)$ = 0.8 volts, I_{out} = 400μA and the ambient temperature is −55°C. Remember the 25°C value under the conditions of $V_{in}(0)$ = 0.4 volts, I_{out} = 0 is V_{CC} − 1.4 volts. The temperature coefficient of a forward biased diode is approximately −2 mv/°C. Going to −55°C will then degrade the "1" level by (25°C − (−55°C)) x 2 mv/°C = 0.16 volts or $V_{out}(1)/_{-55°C} = V_{CC} - 1.56$ volts. At V_{CC} = 4.5 volts $V_{out}(1)/_{-55°C} = 4.5 - 1.56 = 2.94$ volts. As the input "0" level degrades to 0.8 volts transistor Q_2 starts turning on causing a voltage drop of $I_{C2} \times 1.6K$ to further degrade the output. All these affects combine to produce a worst case "1" level output of 2.4 volts. If a "1" level of V_{SS} − 1.5 volts must be guaranteed, under all the above condition, the TTL gate by itself can not drive the MM4262/MM5262 inputs.

One solution, that will absolutely guarantee that the V_{SS} – 1.5 volts "1" level requirement is met, with ample noise margin, is to use a resistor connected between the TTL output and the V_{SS} supply. The penalties that are paid for this are increased number of components and a slight increase in power. The TTL output will pull to the V_{SS} supply with an RC time constant of the pull up resistor and the capacitance of the line, after the maximum TTL "1" level has been reached. *Figure 4* shows the form the TTL output would take when going from a "0" to a "1". There would be no appreciable difference between the "1" to "0" transistion with or without the pull-up resistor. The pull-up resistor should be selected to meet speed requirements and at the same time keep power dissipation and load on the TTL gate within allowable limits. Since most manufacturers of standard 54/74 TTL specify speed with 50 pF load, eight MM4262/MM5262 device inputs (8 x 7 pF = 56 pF) could be driven by a single 54/74 device. If more drive capability is required, other devices such as the DM7096/8096 hex Tri-State® inverters are capable of driving twice the capacitance that a 5404/7404 can drive, with the same rise time.

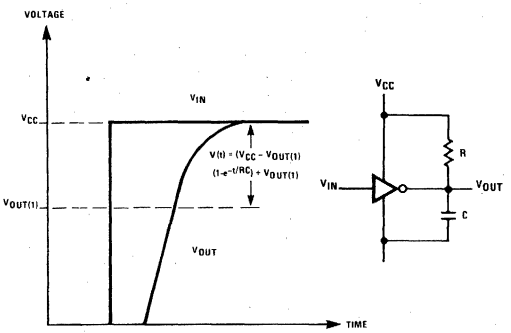


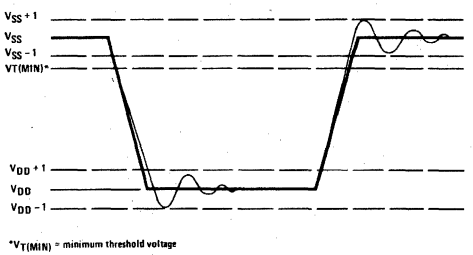
FIGURE 4. Form of TTL Output With Resistive Pull-Up Driving Capacitance Load

The output of the MM4262/MM5262 is of the current sourcing type. A "1" level is represented as current of at least 600μA (500μA for the MM4262) at an output voltage of 1.8 volts. A "0" level is represented as a current of less than 100μA at a voltage of 0 volts. It is desirable to be able to tie the outputs of many RAMs together. This can, in a large system represent a significant capacitance. Since p-channel MOS does not have large current drive capability current outputs are the logical choice. They minimize the amount of output voltage swing required. Which, for capacitive loads, greatly reduces current drive requirements. The current output does necessitate using a sense amplifier, but this is not a significant penalty. TTL output compatible MOS circuits can typically drive only one standard TTL load. They must therefore be buffered to increase fan-out. The sense amplifier, in the case of the MM4262/MM5262, takes the place of this buffer at no net increase in package count. It performs both the function of converting current to TTL levels as well as increasing fan-out.

The DS1605/3605 family and the DS3625 sense amplifiers are recommended for use with the MM4262/MM5262. The DS3625 is a dual sense amplifier and incorporates a latch. The DS1605/2605 family is a hex sense amplifier. All have Tri-State® outputs for bus interface capability.

The clock signals for the MM4262/MM5262 have three requirements which have the potential of generating problems for the user. These requirements, high speed, large voltage swing and large capacitive loads, combine to provide ample opportunity for inductive ringing on clock lines, coupling clock signals to other clocks and/or inputs and outputs and generating noise on the power supplies. All of these problems have the potential of causing the memory system to malfunction. Recognizing the source and potential of these problems early in the design of a memory system is the most critical step. The object here is to point out the source of these problems and give a quantitative feel for their magnitude.

Line ringing comes from the fact that at a high enough frequency any line must be considered as a transmission line with distributed inductance and capacitance. To see how much ringing can be tolerated we must examine the clock voltage specification. *Figure 6* shows the clock specification, in diagram form, with idealized ringing sketched in. The ringing of the clock about the V_{SS} level is particularly critical. If the V_{SS} – 1 volt is not maintained, at all times, the information stored in the memory could be altered. Referring to *Figure 1*, if the threshold voltage of a transistor were –1.3 volts, the clock going to V_{SS} – 1 would mean that all the devices, whose gates are tied to that clock, would be only 300 MV from turning on. The internal circuitry needs this noise margin and from the functional description of the RAM it is easy to see that turning a clock on at the wrong time can have disasterous results.



*$V_{T(MIN)}$ = minimum threshold voltage

FIGURE 6. Clock Waveform

Controlling the clock ringing is particularly difficult because of the relative magnitude of the allowable ringing, compared to the magnitude of the transition. In this case, it is 1 volt out of 20 volts or only 5%. Ringing can be controlled by damping the clock driver and minimizing the line inductance.

Damping the clock driver by placing a resistance in series with its output is effective, but there is a limit since excessive resistance will slow down the rise and fall time of the clock signal. Because the typical clock driver can be much faster than the worst case driver, the damping resistor serves the useful function of limiting the minimum rise and fall time. This is very important because the faster the rise and fall times the worse the ringing problem becomes. The size of the damping resistor varies because it is dependent on the details of the actual application. It must be determined empirically. In practice a resistance of 10Ω to 20Ω is usually optimum.

Limiting the inductance of the clock lines can be accomplished by minimizing their length and by laying out the lines such that the return current is closely coupled to the clock lines. When minimizing the length of clock lines it is important to minimize the distance from the clock driver output to the furthest point being driven. Because of this, memory boards are usually designed with clock drivers in the center of the memory array, rather than on one side, reducing the maximum distance by a factor of 2.

Using multilayer printed circuit boards with clock lines sandwiched between the V_{DD} and V_{SS} power plains minimizes the inductance of the clock lines. It also serves the function of preventing the clocks from coupling noise into input and output lines. Unfortunately multilayer printed circuit boards are more expensive than two sided boards. The user must make the decision as to the necessity of multilayer boards. Suffice it to say here, that reliable memory boards can be designed using two sided printed circuit boards. The 16K words x 10 bits memory board described in the example at the end of this application note demonstrates this.

The recommended clock driver for use with the MM4252/MM5262 is the DS0056/DS0056C dual clock driver. This device is designed specifically for use with dynamic circuits using a substrate, V_{BB} supply. Typically it will drive a 1000 pF load with 20 ns rise and fall times. *Figure 7* shows a schematic of a single driver.

In the case of the MM4262/MM5262 V+ is +5 volts and V_{BB} is +8.5 volts. V_{BB} should be connected to the V_{BB} pin shown in *Figure 7* through a 1K resistor. This allows transistor Q_8 to saturate pulling the output to within a VCE(SAT) of the V+ supply. This is critical because as was shown before the V_{SS} − 1.0 volt clock level must not be exceeded at any time. Without the V_{BB} pull up on the base of Q_4 the output at best will be 0.6 volt below the V+ supply and can be 1 volt below the V+ supply reducing the noise margin or this line to zero.

Because of the amount of current that the clock driver must supply to its capacitive load, the distribution of power to the clock driver must be considered. *Figure 8* gives the idealized voltage and current waveforms for a clock driver driving a 1000 pF capacitor with 20 ns rise and fall time.

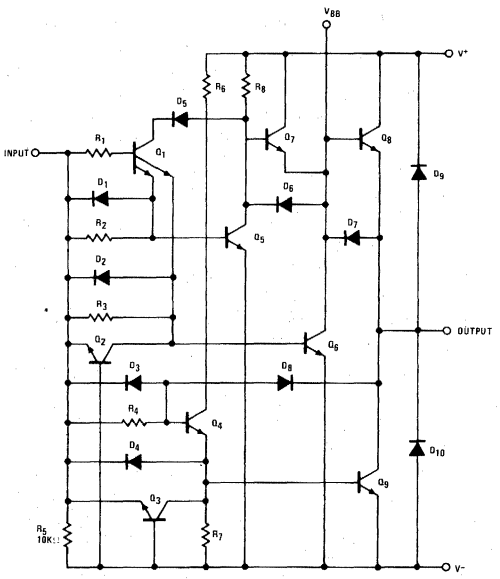


FIGURE 7. Schematic of 1/2 DS0056

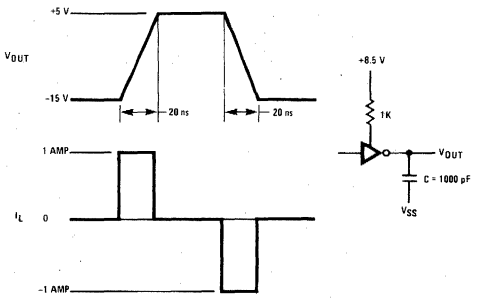


FIGURE 8. Clock Waveforms (Voltage and Current)

As can be seen the current is significant. This current flows in the V_{DD} and V_{SS} power lines. Any significant inductance in the lines will produce large voltage transients on the power supplies. A bypass capacitor, as close as possible to the clock driver, is essential in minimizing this problem. This bypass is most effective when connected between the V_{SS} and V_{DD} supplies. A bypass capacitor for each DS0056 is recommended. The size of the bypass capacitor depends on the amount of capacitance being driven. Using a low inductance capacitor, such as a ceramic or silver mica, is most effective. Another helpful technique is to run the V_{DD} and V_{SS} lines, to the clock driver, adjacent to each other. This tends to reduce the lines inductance and therefore the magnitude of the voltage transients.

The output current of the clock driver during the transition from high to low or low to high may be as high as 1.5 amps when driving a large capacitive load. During the transition from high to low this current is also conducted through the V– lead. If the external interconnective V– wire between the clock driver and the circuit driving the clock driver is electrically long, or has significant DC resistance, the current transient will appear as negative feedback and subtract from the switching response. To minimize this effect short interconnecting wires are necessary and high frequency power supply decoupling capacitors are again required.

While discussing the clock driver it should be pointed out that the DS0056 is a relatively low input impedance device. It is possible to couple current noise into the input without seeing a significant voltage. Since this noise is difficult to detect with an oscilloscope, it is often overlooked.

An excellent source of information on MOS clock drivers is Application Note AN-76, Applying Modern Clock Drivers to MOS Memories. AN-76 is of general application and it is recommended that the memory designer be familiar with it.

Lastly the clock lines must be considered as noise generators. *Figure 9* shows a clock coupled through a parasitic coupling capacitor, C_C, to eight data input lines being driven by a 7404. A parasitic lumped line inductance, L, is also shown. Let us assume for the sake of argument, that C_C is 1 pF and that the rise time of the clock is high enough to completely isolate the clock transient from the 7404 because of the inductance, L. With a clock transition of 20 volts the magnitude of the voltage generated across C_L is:

$$V = 20V \times \frac{C_C}{C_L + C_C} = 20V \times \frac{1}{56 + 1} = 0.35 \text{ volts}$$

This has been a hypothetical example to emphasize that, with 20V fast rise/fall time transitions, parasitic elements can not be neglected. In this example 1 pF of parasitic capacitance could cause system malfunction, because a 7404 without a pull up resistor has typically only 0.1 volts of noise margin in the "1" state at 25°C. Of course it is stretching things to assume that the inductance, L, completely isolates the clock transient from the 7404. However, it does point out the need to minimize inductance in input/output as well as clock lines.

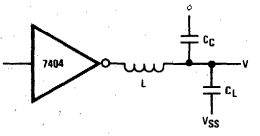


FIGURE 9. Clock Coupling

The output is current, so it is more meaningful to examine the current that is coupled through a 1 pF parasitic capacitance. The current would be:

$$I = C_C \times \frac{V}{t} = \frac{1 \times 10^{-12} \times 20}{20 \times 10^{-9}} = 1 \text{ mA}$$

This exceeds the total output current swing so it is obviously significant.

Clock coupling to inputs and outputs can be minimized by using multilayer printed circuit boards, as mentioned previously, physically isolating clock lines and/or running clock lines at right angles to input/output lines. All of these techniques tend to minimize parasitic coupling capacitance from the clocks to the signals in question.

In considering clock coupling it is also important to have a detail knowledge of the functional characteristics of the device being used. As an example, for the MM4262/MM5262, coupling noise from the ϕ_2 clock to the address lines is of no particular consequence. On the other hand the address inputs will be sensitive to noise coupled from the ϕ_1 clock.

B. System Timing

The timing diagram in *Figure 2* defines the critical timing parameters on the MM4262/MM5262. Timing parameters are either generated by the system or controlled by the physical characteristics of the MM4262/MM5262. There is sometimes confusion regarding the definition of maximum and minimum for these parameters. For instance, the ϕ_1 clock pulse width, T_{1PW}, is generated by the system and for the MM5262 has a minimum value of 95 ns and a typical value of 70 ns. It does not sound correct to have the typical value less than the minimum value. This specification simply means that the typical MM5262 will function properly with a T_{1PW} of 70 ns but a T_{1PW} of at least 95 ns must be supplied if all MM5262 devices are to function properly.

On the other hand Read Access Time, T_{ACC2}, is an MM4262/MM5262 characteristic. For the MM5262 it is specified as 195 ns maximum and 150 ns typical. This simply means that a typical MM5262 has a T_{ACC2} of 150 ns and no MM5262 has an access of greater than 195 ns.

Other parameters, such as T_{ACC1}, are dependent on both system generated timing (T_{AS} and T_{12}) and MM4262/MM5262 characteristics (T_{ACC1}). T_{ACC2} maximum is obtained by setting T_{AS} and T_{12} to their minimum and T_{ACC1} to its maximum.

When setting up the system timing adequate margins must be maintained such that under worst case conditions all of the timing requirements are met. The main point to consider in establishing these margins is the variation in propagation delay of the components driving

the MM4262/MM5262. An example will best serve to illustrate the type of problem that must be considered.

Let us look at the timing of the rising edge of ϕ_1 and address inputs to the RAM. As we saw before it is critical to maintain address setup and hold times (T_{AS} and T_{AH}) for proper operation. *Figure 10* shows the logic diagram and timing for this example. *Table 2* gives the minimum and maximum propagation delays to A_0 and ϕ_1.

		Minimum	Maximum
IN_A to A_0	tpd 1	5 ns	22 ns
	tpd 0	3 ns	15 ns
IN_B to ϕ_1	tpd 1	12 ns*	35 ns*
	tpd 0	11 ns*	34 ns*

*Estimated Using DS0056 Data Sheet

Table 2

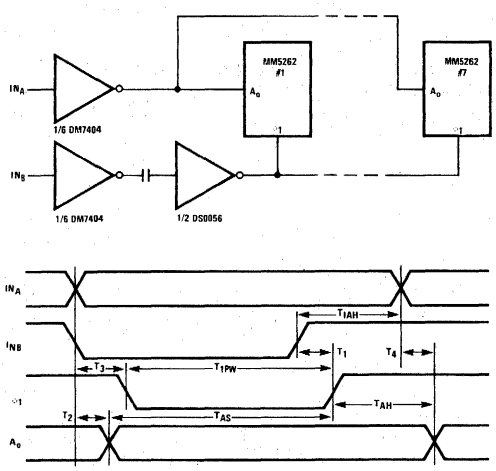


FIGURE 10.

In this case, assuming there is no tracking of delays, the worst case situation will occur for T_{AS} when the ϕ_1 delay is minimum and the A_0 delay is maximum. From *Figure 2*:

$$T_{AS} = T_3 + T_{1PW} - T_2$$

Setting T_{1PW} at its minimum allowable value gives:

$$T_{AS} = T_{3(min)} + 95\text{ ns} - T_{2(max)} \geqslant 80\text{ ns}$$

$$T_{3(min)} - T_{2(max)} \geqslant -15\text{ ns}$$

From table 2:

$$T_{3(min)} - T_{2(max)} = 11 - 12 = -11\text{ ns}$$

Therefore, since $-11\text{ ns} > -12\text{ ns}$ all is well.

The worst case conditions for T_{AH} occur when the ϕ_1 delay is maximum and the A_0 delay is minimum. From *Figure 2*:

$$T_{AH} = T_{IAH} + T_4(\text{min}) - T_1(\text{max}) \geqslant 90\text{ ns}$$

Substituting from table 2 gives:

$$T_{IAH} + 3\text{ ns} - 34\text{ ns} \geqslant 90\text{ ns}$$

or

$$T_{IAH} \geqslant 59\text{ ns}$$

With the estimated worst case time of *Table 2*, T_{IAH}, input address hold time must be at least 59 ns.

This example demonstrates how the memory system designer must account for variations in propagation delays of logic elements used to drive the MM4262/MM5262. As the details of the external logic vary the determination of critical timing paths also vary. Some tracking of delays in this logic can usually be anticipated. In the above example we have assumed none. Tracking of delays will produce, in general, a faster system. As system performance depends more and more on component tracking to reach speed goals the risk of failure also increases. The memory designer, with knowledge and experience, must trade off this improved performance against risk.

C. Refresh Requirements

In section I, detail description of operation of MM4262/MM5262, the need for restoring or "refreshing" the information stored in the RAM was indicated. The internal leakage is such that each cell of a MM5262 must be refreshed at least every 2 milliseconds and the MM4262 at least every 1 millisecond. Since the RAM refreshes on a row basis (32 rows) refresh could be accomplished by applying 32 ϕ_3 clocks every 2 ms (1 ms for MM4262). One ϕ_3 clock for each row.

Although address inputs A_0 through A_4, row addresses, must clearly be defined during refresh, it is also necessary that normal set up and hold times be observed for the column addresses, A_5 through A_{10}. A reasonable alternative is to force them to a logic "1" or "0" state and sequence A_0 through A_4 through their 32 states. If it is more convenient to let A_5 through A_{10} vary, T_{AS} and T_{AH} must be observed on those addresses during refresh.

D. Power Considerations

Power consumed by a memory system using the MM4262/MM5262 can be divided into four categories: (1) Power required for peripheral circuitry, (2) Clock power, (3) dc power required by the MM4262/MM5262 and, (4) ac power required by the MM4262/MM5262.

Calculation of peripheral circuit power, assuming it is TTL, is straight forward and won't be described here. Clock power, which is dissipated almost entirely in the clock driver, is completely described in application note AN-76 mentioned previously. Again it is recommended that the memory designer be familiar with this application note.

In describing power consumed by the MM4262/MM5262 the terms dc and ac power should be defined. When there is a resistive path for the current it is termed dc power, even though the current may be switching. When there is a capacitive path for the current it is termed ac power. These are not conventional definitions but it is necessary to make some distinction between the two types of current. DC power is proportional to the duty cycle of the clocks while AC power is proportional to the frequency of the clocks.

Figure 11 shows I_{DD} for a typical MM5262 operating at $T_A = 25°C$ with a cycle of 840 ns. As can be seen a large current transient, 150 mA peak, occurs during the ϕ_1 clock time. Current during ϕ_1 clock time is composed of dc and ac current. The dc current, 20 mA, is approximately constant throughout the ϕ_1 clock interval. The ac current results from precharging internal capacitive nodes during the ϕ_1 clock time. The remainder of the currents are basically a combination of ac and dc currents.

Note 17, on the MM4262/MM5262 data sheet, gives an approximate relationship for calculating I_{DD}. This relationship is:

$$I_{DD} = A \times \frac{T_{1PW}}{T_{CYC}} + B \times \frac{T_{2PW}}{T_{CYC}} + C \times \frac{1000\ ns}{T_{CYC}}$$

With the aid of *Figure 11* the terms A, B and C can be readily identified.

The A term is the value of the dc current during the ϕ_1 clock interval, T_{1PW}. The resulting average current is simply A times the duty cycle ($A \times T_{1PW}/T_{CYC}$). The B term is the same thing for the ϕ_2 clock interval, T_{2PW}.

The C term accounts for the shaded area, Q_C in *Figure 11*. Q_C is the amount of charge transferred to the internal node capacitance each cycle. Therefore the amount of charge per unit time, I, is: $I = Qc/T_{CYC}$. In the above formula for I_{DD}, $C = Qc/10^{-6}$ sec. This corresponds to an on chip capacitance of approximately 500 pF with which the chip bypass capacitors must charge share.

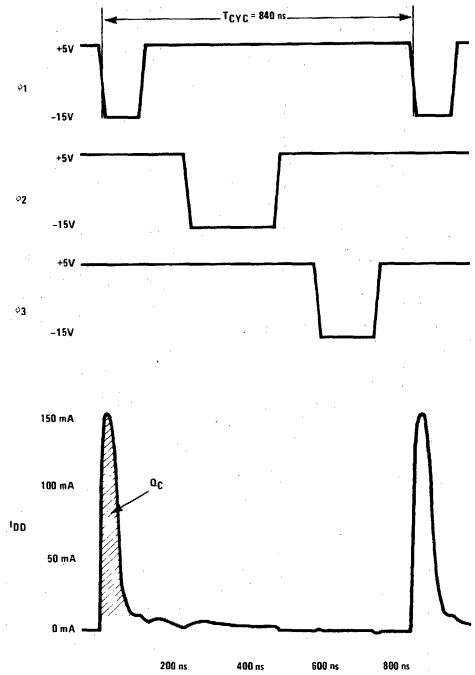


FIGURE 11. Typical I_{DD} at $T_A = 25°C$

The primary purpose for showing the I_{DD} current waveform is to point out the magnitude of the current transient during ϕ_1 time. If the worst case current is calculated using the above equation, with worst case value for A, B and C with $T_{CYC} = 635$ ns we get:

$$I_{DD}\ max = 3\ mA + 1.7\ mA + 15.7\ mA$$

$$= 20.4\ mA$$

The initial ac transient accounts for approximately 77% (15.7/20.4) of the total power dissipation of the RAM. In addition to the I_{DD} current there is also a current transient due to the input clock capacitance of ϕ_1 that must be considered. With 20 ns rise time on the ϕ_1 clock this current is:

$$I = 50 \times 10^{-12}\ farads \times 20\ volts/20 \times 10^{-9}\ sec = 50\ mA$$

The purpose of pointing out all these transient currents and their magnitude is to demonstrate the need for using bypass capacitors with the MM4262/MM5262. If there is significant inductance in the V_{DD}, V_{SS} and/or V_{BB} lines, serious voltage transients will result unless sufficient bypass capacitors are used. Requirements vary with actual application, but 0.1 μF, from V_{DD} to V_{SS} and from V_{DD} to V_{BB}, for every other RAM is usually sufficient. Again, since bypass capacitors are attempting to defeat line resistance and/or inductance, it is important to place them physically as close as possible

to the RAMs they are intended to bypass. Using one centrally located capacitor is effective for decoupling transients generated on one board from getting into another board, but usually will not help decouple transient internal to the board.

For techniques of minimizing total system power the reader is referred to application note AN-86. A Simple Power Saving Technique for the MM5262 2K RAM. AN-86 explores the use of clock decoding to minimize the number of clocks that must be applied. It is easy to see from the above discussion that this could produce significant power savings since an unclocked RAM draws only 100μA from the V_{DD} line.

E. Printed Circuit Layout Considerations

All of the consideration in laying out printed circuit boards for RAMs center around minimizing the inductance of lines and capacitance coupling from one line to another.

Capacitive coupling is minimized by physically isolating or shielding noise sources. Shielding using multilayer printed circuit boards is probably the most effective but is also the most expensive. Physical isolation can be accomplished by running sensitive lines such as the data out line at right angles to the clocks and addresses.

Inductance can be minimized by keeping line lengths as short as possible. Also running a line and the return for the line close together will reduce the effective inductance of the line. The effect of inductance on power supply lines can be reduced with the use of bypass capacitors. This solution is, of course, not acceptable for data or clock lines.

Clock lines are by far the worst noise generators. Their effects can be minimized by using series damping resistors to guarantee that the clock voltage transitions are no faster than is absolutely necessary.

Figure 12 gives a printed circuit pattern for laying out a memory array using the MM4262/MM5262. This pattern has been used successfully on RAM boards of up to 16K words by 10 bits.

III. A 16K words x 10 bits Memory Application Example

The MM4262/MM5262 has a wide variety of applications. One example is an 16K words x 10 bits memory board developed by National Semiconductor's Memory Systems Division. Photographs of the memory board are included.

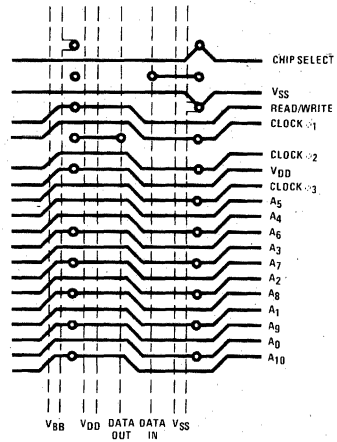


FIGURE 12.

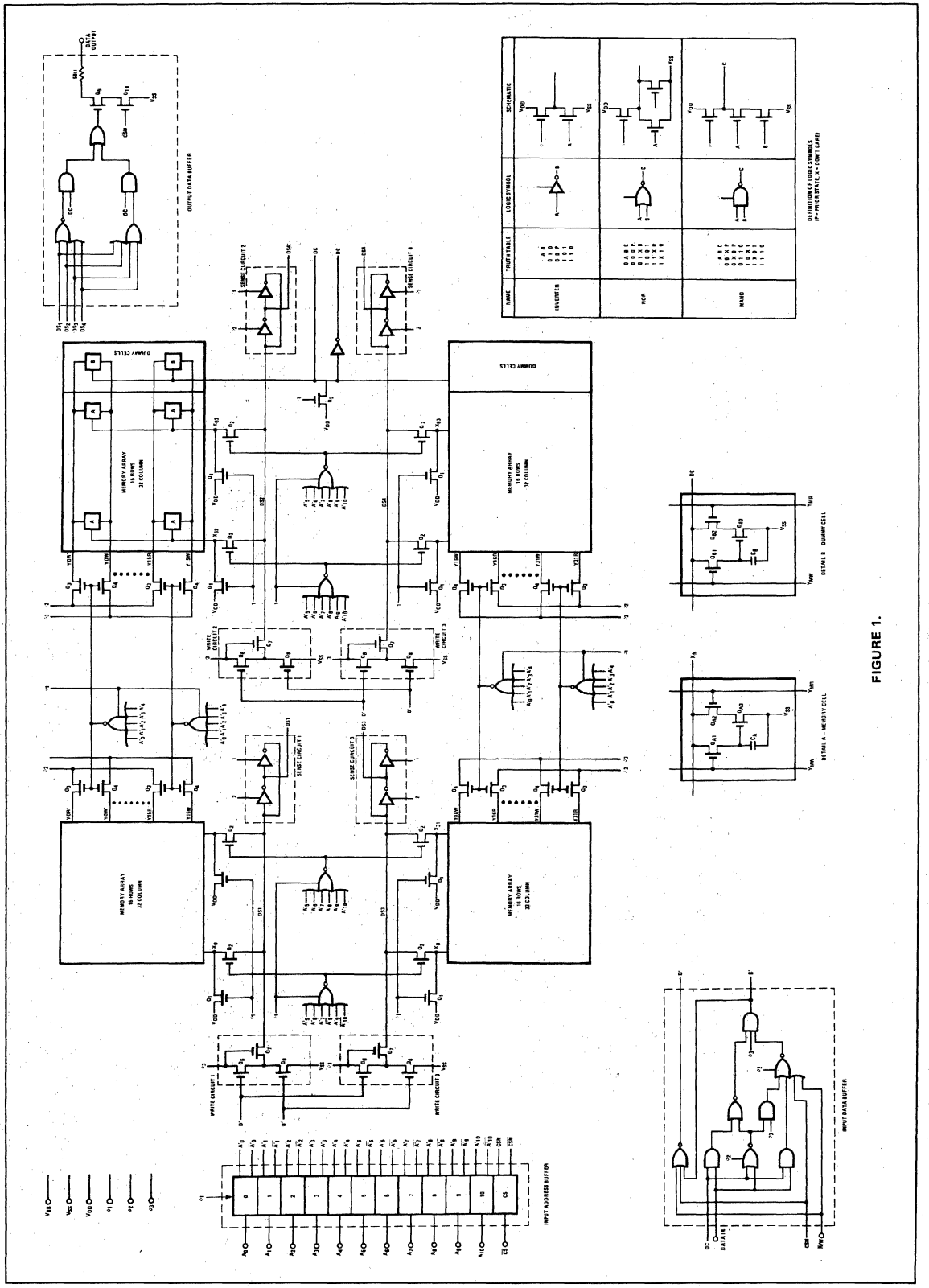
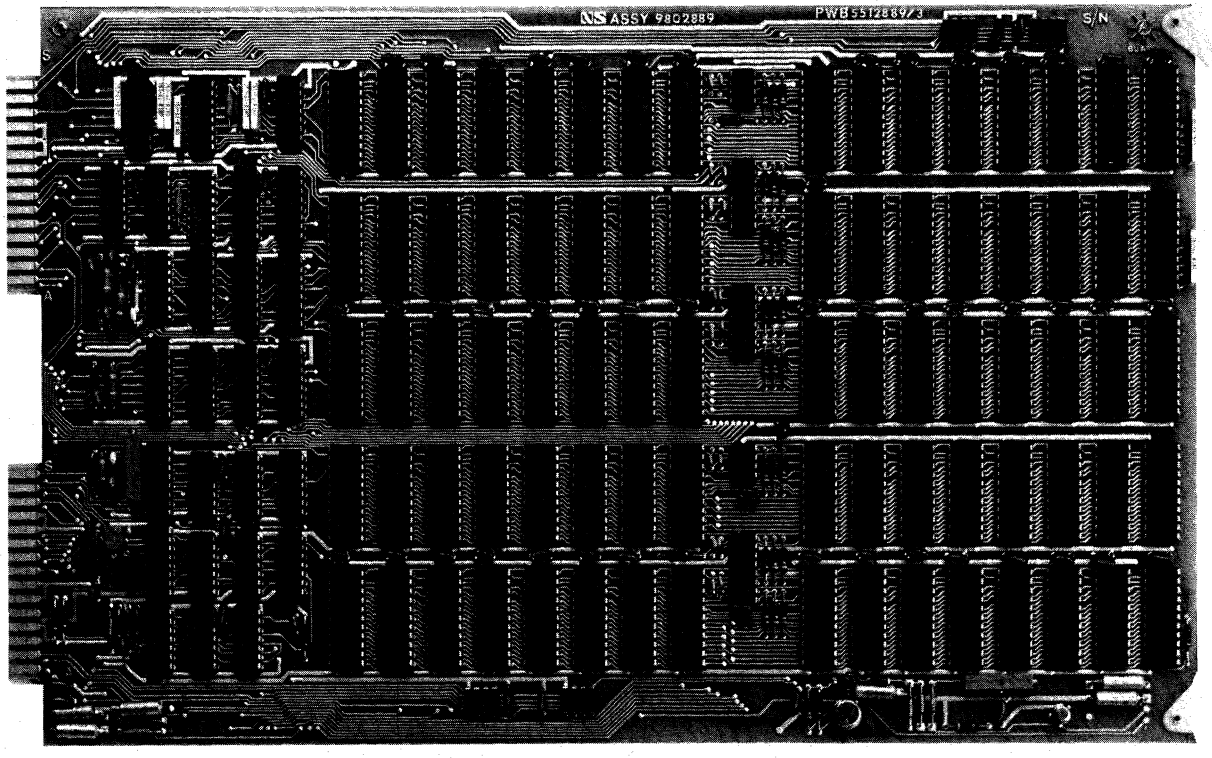


FIGURE 1.

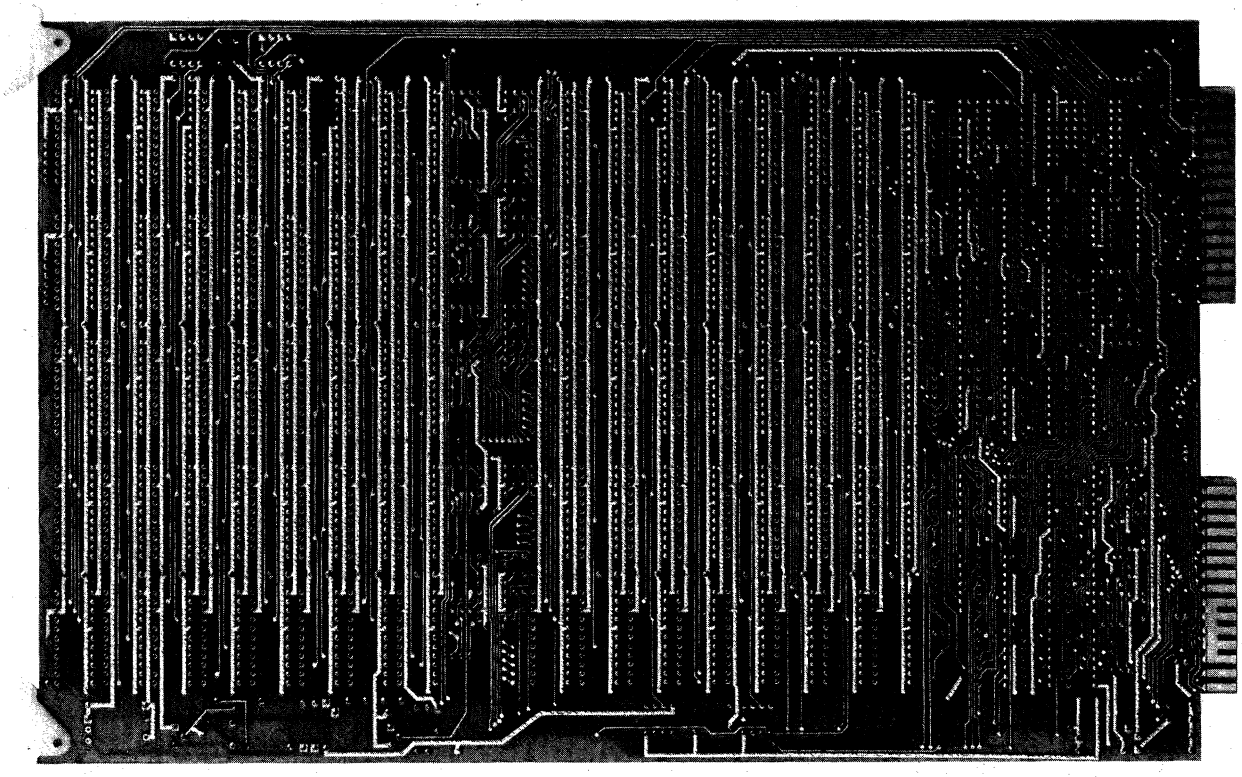


TOP VIEW

16K x 10 MEMORY BOARD

BOTTOM VIEW

16K x 10 MEMORY BOARD



TRIG FUNCTION GENERATORS

Accuracy is the major design variable of trigonometric lookup tables built with MOS read-only memories. Only a few ROMs are needed for most practical applications, but accuracy can be made to increase very rapidly with memory capacity if interpolation techniques are used.

For instance, without interpolation a single 1024-bit ROM can store 128 angular increments and generate an 8-bit output that will be better than 99.9% of the handbook value (Table 1).

ADDRESS	DEGREES	BINARY OUTPUT	DECIMAL SINE
0	0	.00000000	0.000
1	0.7	.00000011	0.012
2	1.4	.00000110	0.023
3	2.1	.00001001	0.035
.			
.			
.			
127	89.3	.11111111	0.996

TABLE 1. MM422BM/MM522BM Sine Function Generator

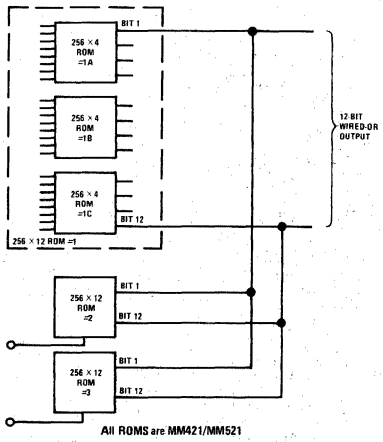
If one simply cascaded ROMs to improve input resolution and output accuracy for a high-accuracy trig solution (X=sin θ) as in Figure 1, large numbers of ROMs might be needed. This 24-ROM system stores 2048 12-bit values of sin x (or other trig functions), giving angular resolution of 1 part in 2^{11} (0.05%) and output accuracy of 1 part in 2^{12} (0.024%). The system in Figure 2 has the same resolution and is accurate to the limit of its 12 output bits (0.024%), which makes it just as good. But it only requires four 1024-bit ROMs and three 4-bit TTL full adders, so it only costs about one-fifth as much as the more obvious solution of Figure 1.

Instead of producing x = sin θ, the Figure 2 system divides the angle into two parts and implements the equation

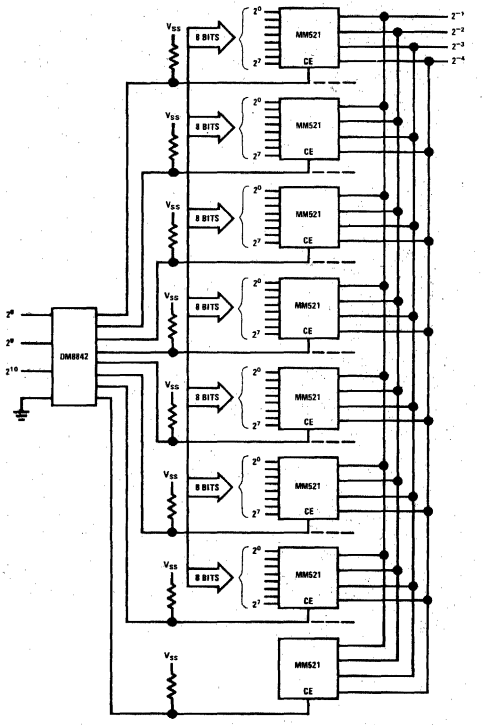
$$x = \sin\theta = \sin(M + L)$$
$$= \sin M \cos L + \cos M \sin L$$

It can be programmed for any angular range. Assume the range is 0 to 90 degrees and let M be the 8 most significant bits of θ and L be the 3 least significant bits of θ (θ being the 11-bit input angular increments, equal to 90°/2048, or 0.044 deg.) as in Table 2.

With an 8-bit address, the three 256x4 ROMs will give the 12-bit value of sin M at increments of $M = 90°/2^8$, or 0.352 deg. The cos L can only vary between 1 and 0.99998. So we assume cos L=1 and store values of sin M at 0.352 deg. resolution



(a)



(b)

FIGURE 1. Conventional 2048-Increment Sine Table Uses 24 ROMs

in the top three ROMs, reducing the equation to

$$\sin \theta = \sin M + \cos M \sin L$$

Values of the second term are stored in the fourth ROM. The maximum value of the second term in the above equation can only be cos Msin L = 0.00539 where $\cos M_{max} = 1$, $\sin L_{max}$ = 0.00539. This is the maximum value to be added to sin M above. Only the five least significant bits of a 12-bit output are needed to form the maximum output, so an MM522 is used in its 128x8 configuration.

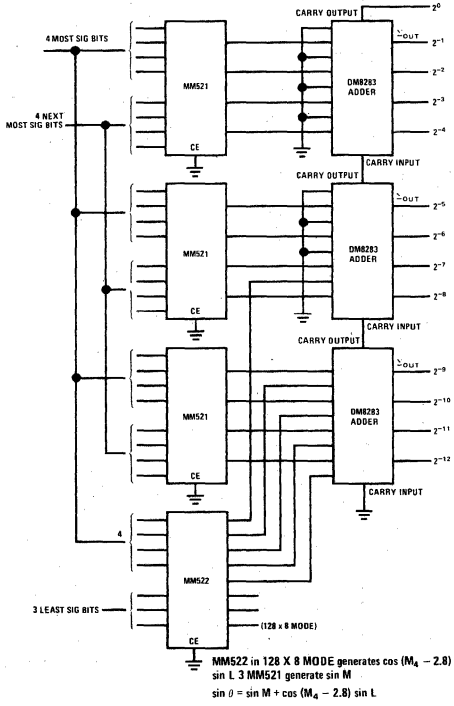


FIGURE 2. Four-ROM Lookup Table Generates 2048 Values of Sin x by Interpolation Technique.

Let the 4 most significant bits of M be called M_4 and the angle at these increments be $X_m = 90°/2^4$ = 5.63 deg. Sin L (the 3 least significant bits of θ) has the same maximum as before and cos M_4 has a maximum of cos 5.63 deg. = 0.99517, and continuing as follows:

$$\cos (11.26) = 0.98076$$

$$\cos (16.89) = 0.95686$$

$$\cos (84.37) = 0.09810$$

through the 16 increments of M_4. Now

$$\sin \theta = \sin M + \cos M_4 \sin L$$

and the appropriate cos M sin L values are stored in the fourth ROM. In effect, we have divided the 0° to 90° sine curve into 16 slope sectors with M_4, each sector into 16 subsections with M, and each subsection into 8 interpolation segments with L.

Since we are using an approximation, accuracy is not quite as good as the Figure 1 system. The additional error term is cos L, assumed 1 but actually is a variable between 1 and 0.99998. At every eighth increment, L is zero, making cos M

ADDRESS	M				L				
	M_4								
0					0				
1					1				L = 0.044°
2					1	0			
3					1	1			
4					1	0	0		
5					1	0	1		
6					1	1	0		
7					1	1	1		
8				1	0	0	0		M = 0.352°
9				1	0	0	1		
16			1	0	0	0	0		
32			1	0	0	0	0	0	
64		1	0	0	0	0	0	0	
128		1	0	0	0	0	0	0	M_4 = 5.63°
256	1	0	0	0	0	0	0	0	
512	1	0	0	0	0	0	0	0	
1024	1	0	0	0	0	0	0	0	
2048-1	1	1	1	1	1	1	1	1	

TABLE 2. Programming of 2048-Increment Sine Table

sin L=0, and sin x=sin M to 12-bit accuracy. Then the error rises to a limit of near 0.002% at every eighth increment where L is 0.352–0.044. This error can be halved by adjusting the fourth ROM's output so that

$$\sin \theta = \sin M + \cos (M - 2.81°) \sin L$$

If five ROMs are used—four MM521's and all eight outputs of the MM522—15-bit accuracy can be achieved, and thus improving the accuracy by a factor of eight. The resolution could also be smaller, of course, if the angular range were smaller as in an application involving a sensor with a limited field of view. Variations of the system could be used to space the increments irregularly to compensate for sensor nonlinearities, to improve accuracy in specific angular ranges.

This example has a binary fraction output, like the sine function generator in Table 1. For instance, the 8-bit output at the 64th increment representing sin x = sin 45° is 10110101. This equals $1 \times 2^{-1} + 0 \times 2^{-2} + 1 \times 2^{-3} + 1 \times 2^{-4} + 0 \times 2^{-5} + 1 \times 2^{-6} + 0 \times 2^{-7} + 1 \times 2^{-8}$, which reduces to 181/256 or 0.7070. Handbooks give the four-place sine of 45° as 0.7071, so at this increment the output is accurate to approximately 0.01%. This table, the MM422BM/MM522BM, is used in fast Fourier transform, radar, and other signal-processing applications.

Other standard tables that are available off the shelf include an arctan generator, several code generators (EBCDIC to ASCII, BCD to Selectric, and Selectric to BCD) and ASCII-addressed character generators for electronic, electrical and electromechanical display and printout systems. All interface with TTL logic and operate off 12-volt power supplies. Write for data sheets, or use one of our programming tables to jot down any special input-output logic functions you need.

NATIONAL

MASK PROGRAMMING SPECIALIZES MOS SHIFT REGISTER DESIGNS

A quick, economical way of customizing MOS shift register bit lengths is programming the metallization mask, the mask that defines the thin-film wiring pattern etched on the silicon wafer. Metallization etching is the most convenient process step to specialize because it is consistent from wafer to wafer and is the last major process step before testing.

Utilizing this technique, National Semiconductor has developed two variable-length dynamic MOS register designs. Both of them, MM4007/MM5007 and MM4019/MM5019, are bipolar compatible. Dual registers 20 to 256 bits long, single registers 40 to 512 bits long, and a variety of taps and pinouts provide the system designer with a method of obtaining custom length shift registers quickly and at reasonable cost.

Up to metal masking, wafer design and fabrication are standardized. No time is lost—or money spent—in developing custom arrays or tuning up the process. Automatic test systems further reduce turnaround time and production costs.

Programming the metallization mask mainly involves routing signal connections past selected storage cells to adjust total register length to the desired number of cells. Wire-bonding changes provide output tap options.

DUAL REGISTER DESIGNS

Basically, each of the variable-length types is a dual register (Figure 1 and Table 1A).

There are enough storage cells, I/O stages, clock and power supply lines on each MM4007 chip to make up to two 100-bit registers. The minimum length of each register half, M_A and M_B, is 20 bits. The programmable parts, P_A and P_B, may be 0 to 80 bits long. Lengths need not be equal. For instance, register A may be 29 bits and register B 76 bits (P_A = 9, P_B = 56).

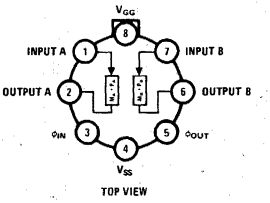


FIGURE 1. Dual Shift Registers

An MM4019/MM5019 chip is similarly organized, except that M_A and M_B are 40 bits and P_A and P_B vary from 0 to 216 bits. Again, lengths may be unequal, such as 240 bits in the A half and 136 bits in the B half.

Clock and supply line pin locations are standardized, but I/O pinouts are selectable. The I/O terminals on the chip may be bonded to package pins which are more convenient for the PC board layout. For example, a couple of board feedthroughs might be eliminated by bonding the A register input to Pin 7 (rather than Pin 1) if data comes in from the right and exits on the left. Or, A and B could share an input pin when they have the same signal source.

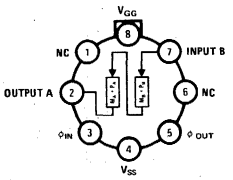
TABLE 1 Register Length Options

	MM4007/MM5007			MM4019/MM5019		
	M (BITS)	P (BITS)	TOTAL (BITS)	M (BITS)	P (BITS)	TOTAL (BITS)
A. DUAL REGISTERS						
A Register	20	0 to 80	20 to 100	40	0 to 216	40 to 256
B Register	20	0 to 80	20 to 100	40	0 to 216	40 to 256
B. SINGLE REGISTERS	$M_A + M_B$	$P_A + P_B$		$M_A + M_B$	$P_A + P_B$	
	40	0 to 160	40 to 200	80	0 to 432	80 to 512
C. TAPPED SINGLE REGISTERS						
Total register length same as single registers with tap locations determined by either half of the dual registers.						

SINGLE-REGISTER OPTIONS

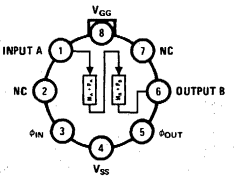
Since clock rates are synchronized by the common clock inputs, the registers may also be serially connected inside the package, as diagrammed in Figure 2. One output is internally connected to the other input.

This extends the maximum length of an MM4007/MM5007 to 200 bits and the MM4019/MM5019 maximum to 512 bits. However, each half still has the same minimum, so the minimums become 40 and 80 bits, respectively (Table 1B). Again, the customer specifies the most convenient I/O pin connections.



TOP VIEW

FIGURE 2a

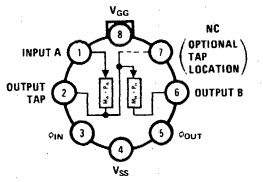


TOP VIEW

FIGURE 2b

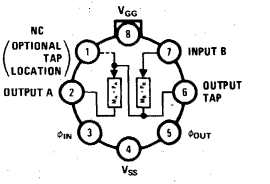
FIGURE 2. Single Registers

Going to the output tap designs of Figure 3 takes only one more wire bond; from the first register output to any available pin. Tap locations are selected by specifying the bit lengths of each of the dual registers. For example, an MM5007 105 bits long may be tapped at any stage from 20 to 85 bits. Generally, this flexibility makes input taps unnecessary—an output at 29 bits in a 105-bit register usually serves the same purpose as an input at 76 bits.



TOP VIEW

FIGURE 3a



TOP VIEW

FIGURE 3b

FIGURE 3. Output Tap Options

OPERATING CHARACTERISTICS

All specifications, except bit lengths, are the same as those of other MM4000/MM5000 series dynamic shift registers with the same number of I/O stages.

Clock-line capacitance, power dissipation, as well as other AC and DC parameters, are independent of the lengths programmed. This is accomplished by standardizing clock and supply wiring patterns to achieve minimum turnaround time and cost.

The MM4007/MM5007 and MM4019/MM5019 are fabricated using a low-threshold, p-channel enhancement-mode technology developed for the MM4000/MM5000 series of registers. This means that they are bipolar compatible, sensing TTL or DTL data without input pull-up resistors and driving TTL or DTL loads without output pull-down resistors. They operate on standard +5V and −12V supplies. The clock frequency range is also the same, from 300 Hz to 2.5 MHz, guaranteed.

Either TO-99 or dual-in-line packages may be specified. MM4007 and MM4019 operate at −55°C to +125°C. MM5007 and MM5019 are commerical types, specified for −25°C to +70°C.

DOUBLE-CLOCKING CUTS STANDARD REGISTERS TO NON-STANDARD SIZES

INTRODUCTION

It may be more economical to make a standard MOS register appear shorter, logically, than to have a special register made to order. A double-clocking technique uses up the unwanted length by causing input bits to be stored twice and then to be read out as individual bits when they reach the end of the register.

Figure 1 shows the clock format. A double clock applied for N of the normal input data intervals at a fixed portion of the total recirculation time

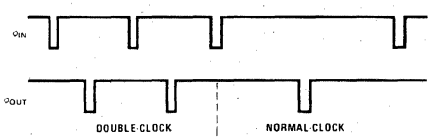


FIGURE 1. Clock rate is doubled for N data input periods to make the register appear shorter by N bits, and then resumes normal frequency.

will shorten the register by N stages and clock periods. If N is 2, a 1-0 input data sequence would be stored as 1-1-0-0. Since these appear as the output at the time the clock is again doubled, the output gate only detects 1-0.

Suppose a parallel array of eight 1991-bit registers is needed to store 1991 8-bit words in a buffer memory. Each could be a subassembly as in Figure 2. The MM5013 and MM5016 are standard 1024-bit and 512-bit register and the MM5019 is mask-programmed to order in sizes up to single 512 or dual 256-bits.

The design in Figure 3 provides the same length with two MM5013 registers. The eight registers are assembled with 16 instead of 24 packages.

Also, the second MM5013 costs less than an MM5016/MM5019 combination (the longer the register the less the cost per bit). The only addition to overhead logic is the decoder and dual clock generator formed with the logic in the dotted lines—one DM7473 dual J-K flip-flop and half a package each of DM7400 and DM7420 gates.

In the example, N = 2048 − 1991, or 57. Therefore, the registers should be clocked at double frequency for the first 57 data periods of the recirculation time. The extra logic decodes the bit-counter output and generates the 114 clocks needed.

There are some limitations to this technique. Obviously, the normal rate should not be more than half the maximum clock rate for the registers

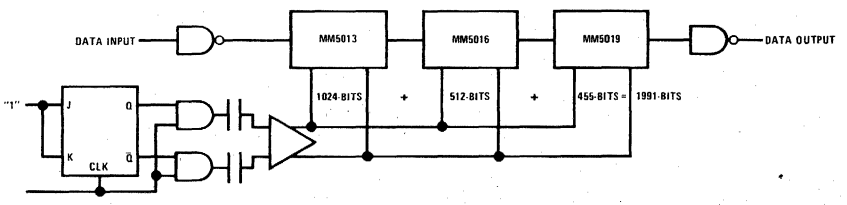


FIGURE 2. Mask-programmable MM5019 register may be used to assemble odd-length registers.

used. Also, if too many bits are subtracted, the clock-drive loading may be affected adversely. The driver power requirement is proportional to average frequency. In the example, it is increased by f(2048/1991) or 2.8%, which has little effect. But if an MM5016 was shortened from 512 to 397 bits, the increase in power would be 28%. In this case, instead of shortening the MM5016, it may be more practical to order an MM5019 at the desired length. At still shorter lengths, the MM5007 mask-programmable dual 100-bit programmable register should be considered. Generally speaking, double-clocking becomes more cost-effective when the system register length is long.

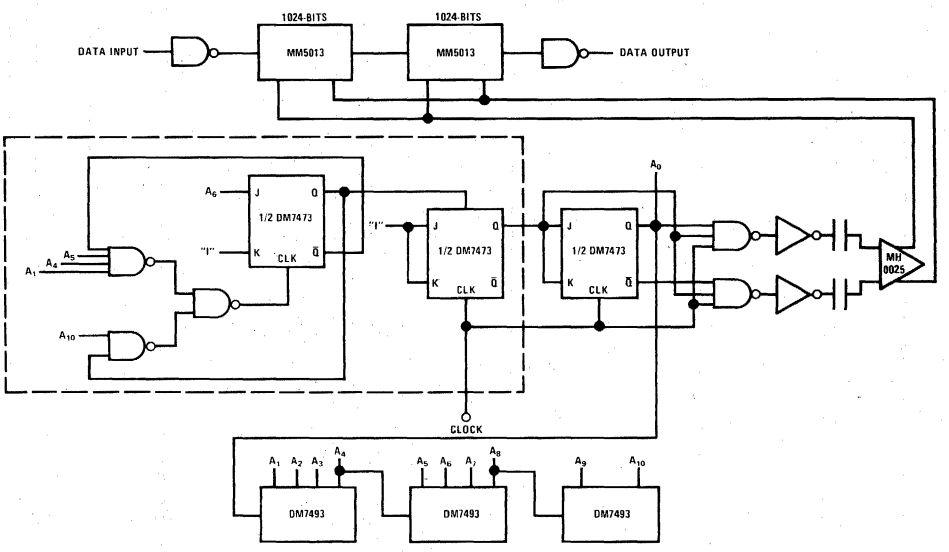


FIGURE 3. A 2048-bit register is made to appear only 1991 bits long by the logic within the dotted lines.

NATIONAL

Definition of Terms

Clock Repetition Rate: The range of clock frequencies for which register operation is guaranteed.

Clock Frequency ϕ_f: The range of clock frequencies which register operation is guaranteed. Maximum clock frequencies are dependent upon minimum and maximum clock pulse width restrictions, as presented by the Guaranteed Operating Curves.

Clock Delay ϕ_d: ϕ_d is defined to be that minimum amount of time that must expire after ϕ_1 has undergone a $V_{\phi L}$ to $V_{\phi H}$ transition and the start of a ϕ_2 $V_{\phi H}$ to $V_{\phi L}$ transition. The same spacings apply, when ϕ_2 preceeds ϕ_1.

Clock Phase Delay ϕ_d, $\bar{\phi}_d$: The time between the $V_{\phi H}$ levels of ϕ_{IN} and ϕ_{OUT}. ϕ_d is the time between the trailing edge of ϕ_{IN} and the leading edge of ϕ_{OUT}. $\bar{\phi}_d$ is the time between the trailing edge of ϕ_{OUT} and the leading edge of ϕ_{IN}.

Clock Pulse Risetime, $t_{r\phi}$: The time delay between the 10% and 90% voltage points on the clock pulse as it traverses between its logic $V_{\phi L}$ and logic $V_{\phi H}$ levels.

Clock Pulse Falltime, $t_{f\phi}$: The time delay between the 10% to 90% voltage points on the clock pulse as it traverses between its logic $V_{\phi H}$ and logic $V_{\phi L}$ levels.

Clock Pulse Width, ϕ_{PW}: The duration of time that the clock pulse is greater than 1.5V.

Clock Input Levels: The voltage levels (logic $V_{\phi L}$ or $V_{\phi H}$) which the clock driver must assume to insure proper device operation.

Clock Control Setup Time, t_{cs}: The time prior to the clock Low to High transition at which the clock control must be at its desired logic level.

Clock Control Hold Time, t_{ch}: The time after the High to Low transition for which the clock control must be held at its desired logic level.

Data Setup Time, t_{ds}: The time prior to the clock High to Low transition at which the data input level must be present to guarantee being clocked into the register by that clock pulse.

Data Pulse Width, t_{dw}: The time during which the data pulse is in its V_{IH} or V_{IL} state.

Data Hold Time, t_{dh}: The time after the clock High to Low transition which the data input level must be held to guarantee being clocked into the register by that clock pulse.

Data Input Voltage Levels: The voltage levels (logic V_{IL} or V_{IH}) which the data input terminal must assume to insure proper logic inputs.

Data Output Voltage Levels: The output voltage levels (logic V_{OL} or V_{OH}) which the output will assume under normal operating conditions.

Data Input Capacitance: The capacitance between the data input terminal and ground reference measured at 1 MHz.

Output Resistance to Ground: The resistance between the output terminal and ground with the output in the logic V_{OH} state.

Partial Bit Times T_{IN}, T_{OUT}: The time between leading edges of clocks, measured at the $V_{\phi H}$ levels. T_{IN} is the time between the leading edge of ϕ_{IN} and the leading edge of ϕ_{OUT}. T_{OUT} is the time between the leading edge of ϕ_{OUT} and the leading edge of ϕ_{IN}.

Output Sink Current: The current which flows into the output terminal of the register when the output is a logical low level. Conventional current flow is assumed.

Output Source Current: The current which flows out of the output terminal of the register when the output is a logical High level. Conventional current flow is assumed.

Output Voltage Levels: The logical Low level, V_{OL}, is the more negative level. This is the state in which the output is capable of sinking current. The logical High level, V_{OH}, is the more positive level. This is the state in which the output is capable of sourcing current.

V_{GG} Current Drain: The average current flow out of the V_{GG} terminal of the package with the output open circuited.

Power Supply Voltage, V_{GG}: The negative power supply potential required for proper device operation; referenced to V_{SS}.

Power Supply Return, V_{SS}: The V_{SS} terminal is the reference point for the device. It must always be the most positive potential applied to the device.

V_{SS} Current Drain: The average current flow into the V_{SS} terminal of the package. It is equal to the sum of the I_{GG} and I_{DD} currents.

Power Supply Voltage, V_{DD}: The negative power supply potential required for proper device operation, referenced to V_{SS}.

Clock Input Voltage Levels, $V_{\phi H}$ $V_{\phi L}$: The voltage levels (logic "1" or "0") which the clock driver must assume to insure proper device operation.

Data Output Voltage Levels, V_{OH}, V_{OL}: The output voltage levels (logic "1" or "0") which the output will assume with a specified load connected between output and V_{SS} line.

Data Input Voltage Levels, $V_{IH}V_{IL}$: The voltage levels (logic "1" or "0") which the data input terminal must assume to insure proper logic inputs.

Control Release Time, t_{cr}: The maximum time that a load command signal can be changed prior to the $V_{\phi L}$ to $V_{\phi H}$ transition of the output clock, ϕ_{OUT}, without affecting the data during bit time t_n.

Control Initiate Window: The time in which a load command signal must be applied to affect bit time t_n. This time extends from the start of t_{cr} to the start of t_{cs}.

Control Hold Time: The time that the load command signal must remain stable during t_n bit time. See control timing diagram.

Physical Dimensions

PACKAGES

DUAL-IN-LINE PACKAGES

(N) Devices ordered with "N" suffix are supplied in molded dual-in-line package. Molding material is EPOXY B, a highly reliable compound suitable for military as well as commercial temperature range applications. Lead material is Alloy 42 with a hot solder dipped surface to allow for ease of solderability.

(J) Devices ordered with the "J" suffix are supplied in either the 14-pin, 16-pin, or 24-pin ceramic dual-in-line package. The body of the package is made of ceramic and hermeticity is accomplished through a high temperature sealing of the package. Lead material is tin-plated kovar.

(D) Devices ordered with the "D" suffix are supplied in glass/metal dual-in-line package. The top and bottom of the package are gold-plated kovar as are the leads. The side walls are glass, through which the leads extend forming a hermetic seal.

(Q) Devices ordered with the "Q" suffix are supplied in a glass/metal dual-in-line with a quartz cover.

METAL CAN PACKAGES

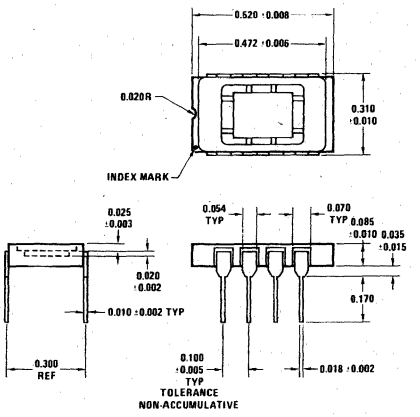
(H) Devices ordered with the "H" suffix are supplied in either 4-pin TO-72 style, 8-pin or 10-pin TO-5 style metal can package. The cap is chrome-plated kovar and the leads are gold-plated kovar.

(G) Devices ordered with the "G" suffix are supplied in a 12-pin TO-8 style metal can package. The cap is chrome-plated kovar and the leads are gold plated kovar.

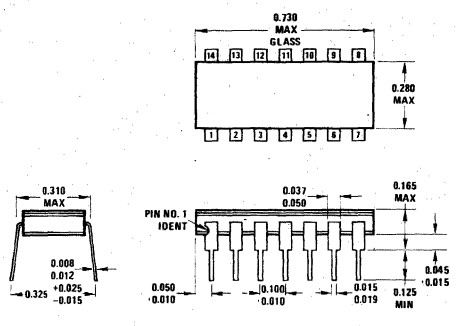
FLAT PACKAGES

(W) Devices ordered with the "W" suffix are supplied in the 14-pin, ceramic flat package. The body of the package is made of ceramic and hermeticity is accomplished through a high temperature sealing of the package. Lead material is tin-plated kovar.

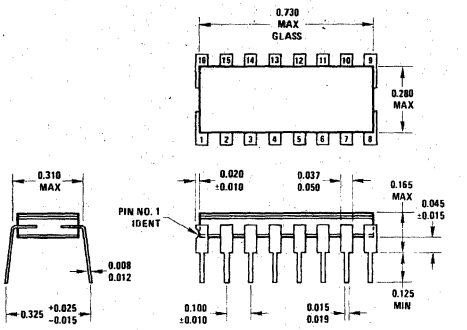
(F) Devices ordered with the "F" suffix are supplied in the 14-pin, glass/metal flat package. The top and bottom of the package are gold-plated kovar as are the leads. The side walls are glass, through which the leads extend forming a hermetic seal.



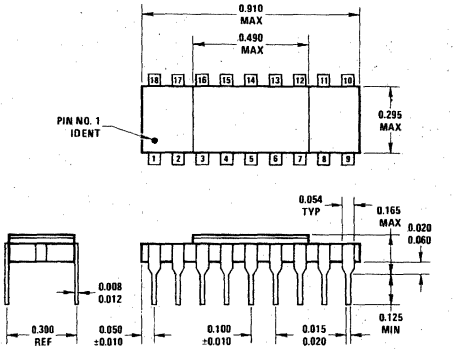
Package 1
8-Lead Cavity DIP (D)



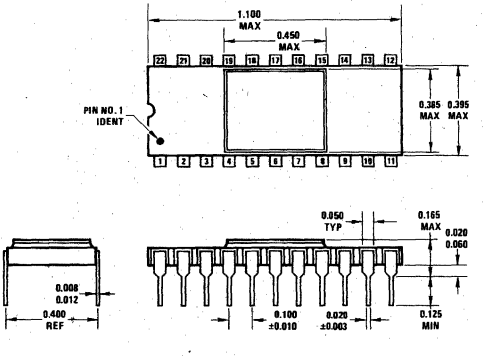
Package 2
14-Lead Cavity DIP (D)



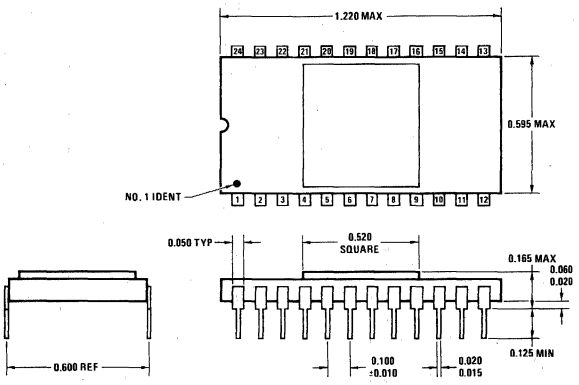
Package 3
16-Lead Cavity DIP (D)



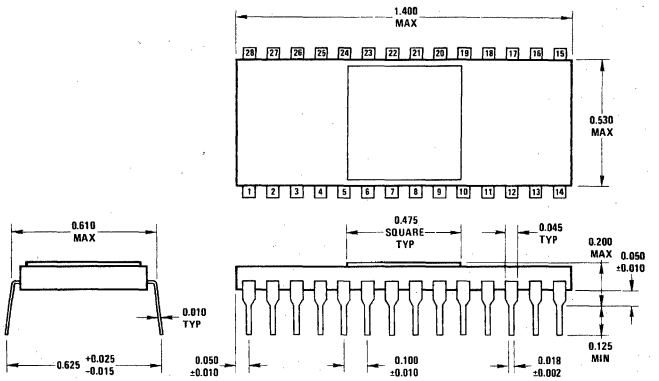
Package 4
18-Lead Cavity DIP (D)



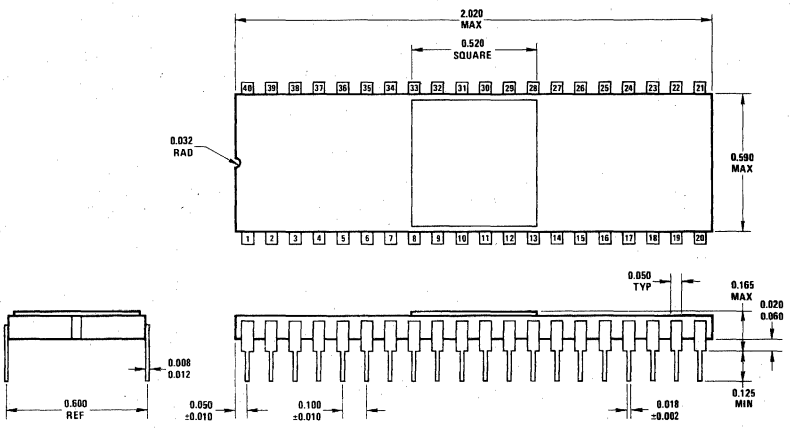
Package 5
22-Lead Cavity DIP (D)



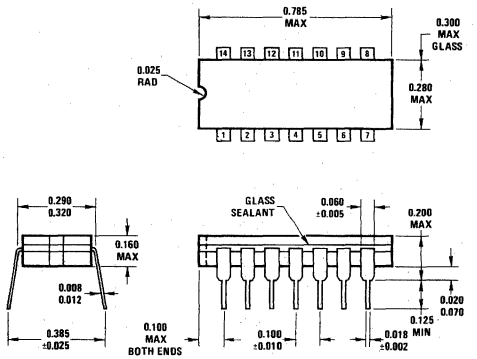
Package 6
24-Lead Cavity DIP (D)



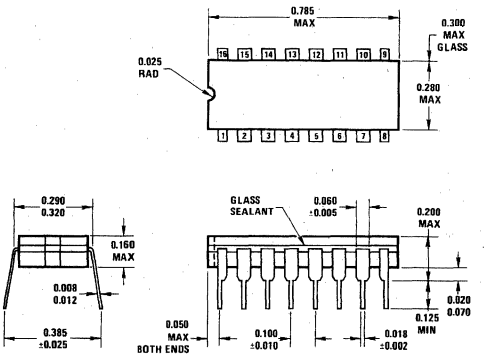
Package 7
28-Lead Cavity DIP (D)



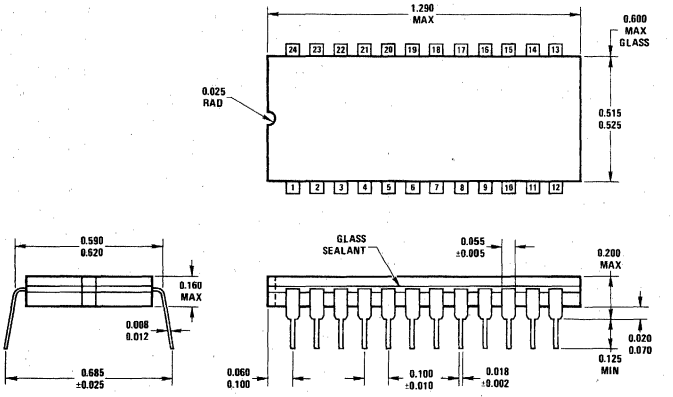
Package 8
40-Lead Cavity DIP (D)



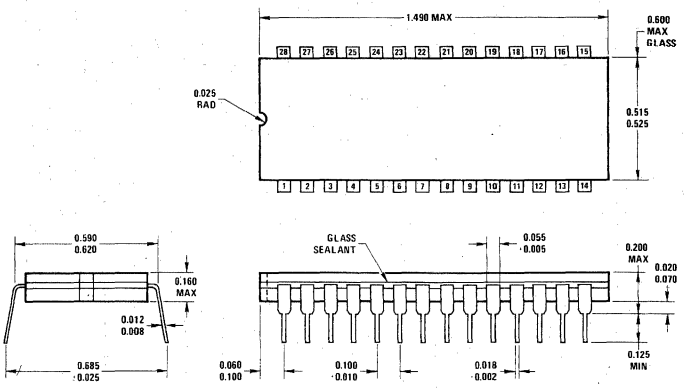
Package 9
14-Lead Cavity DIP (J)



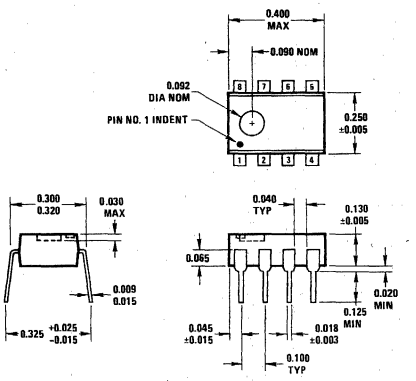
Package 10
16-Lead Cavity DIP (J)



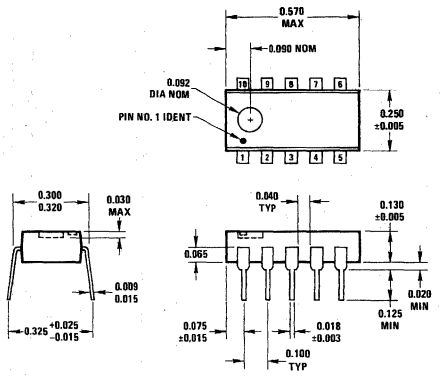
Package 11
24-Lead Cavity DIP (J)



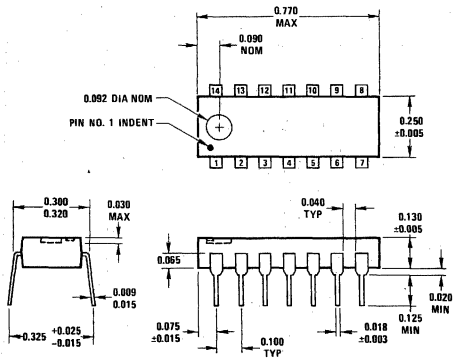
Package 11A
28 Lead Cavity DIP (J)



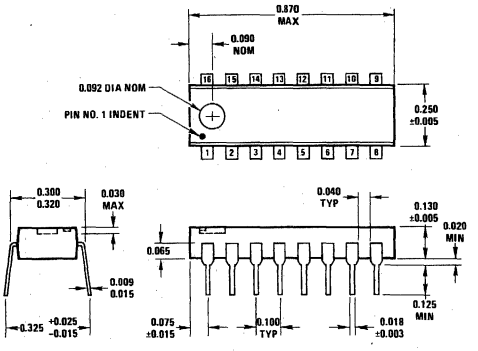
Package 12
8-Lead Molded DIP (N)



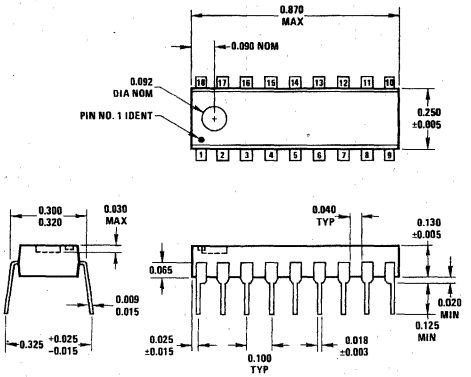
Package 13
10-Lead Molded DIP (N)



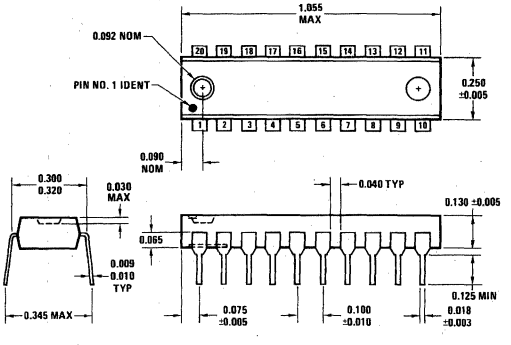
Package 14
14-Lead Molded DIP (N)



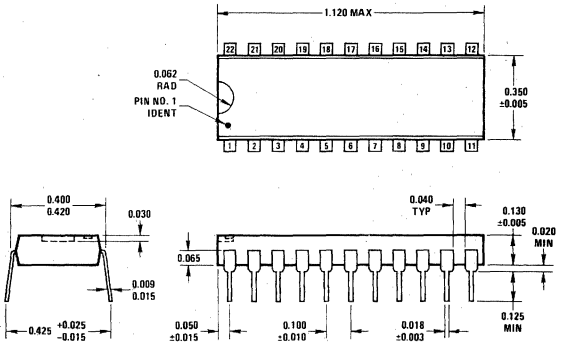
Package 15
16-Lead Molded DIP (N)



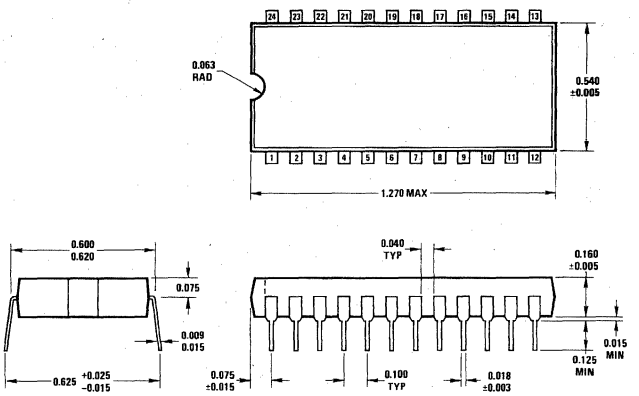
Package 16
18-Lead Molded DIP (N)



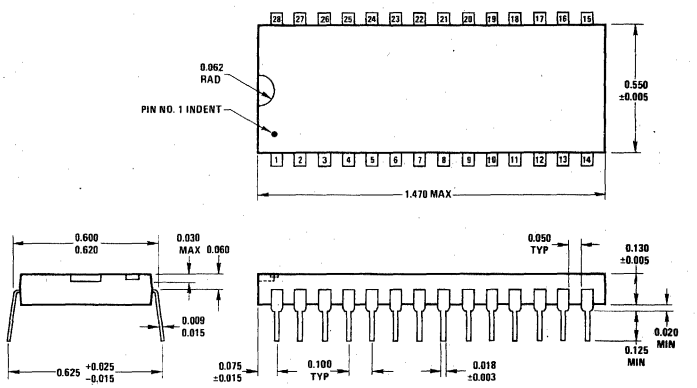
Package 16A
20-Lead Molded DIP (N)



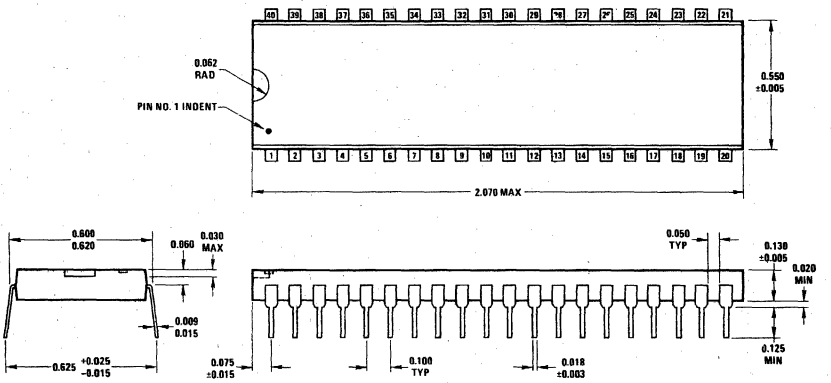
Package 17
22-Lead Molded DIP (N)



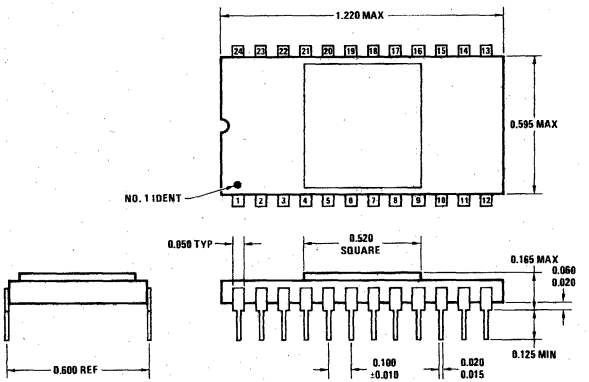
Package 18
24-Lead Molded DIP (N)



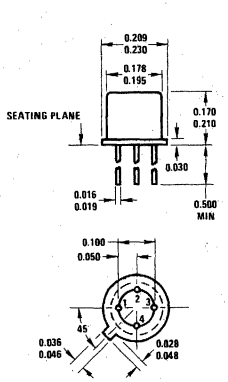
Package 19
28-Lead Molded DIP (N)



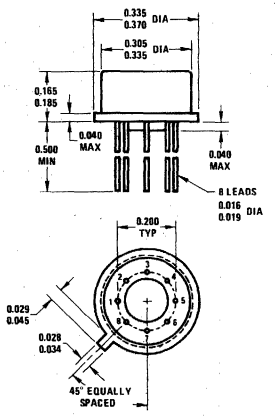
Package 20
40-Lead Molded DIP (N)



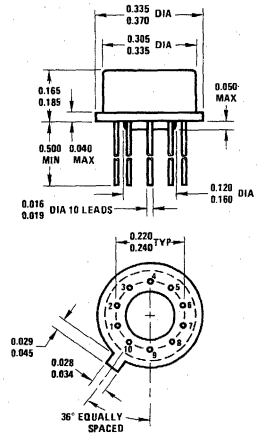
Package 21
24-Lead Quartz Lid Cavity DIP (Q)



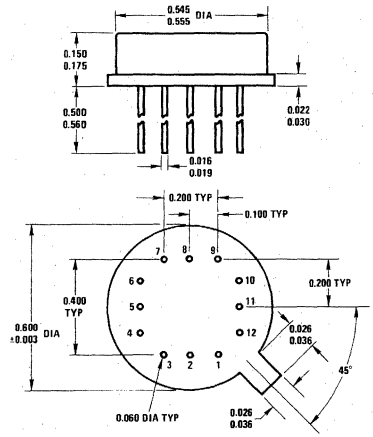
Package 22
4-Lead TO-72 Metal Can Package (H)



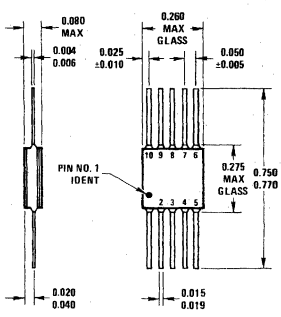
Package 23
8-Lead TO-5 Metal Can Package (H)



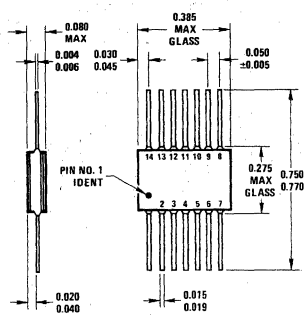
Package 24
10-Lead TO-5 Metal Can Package (H)



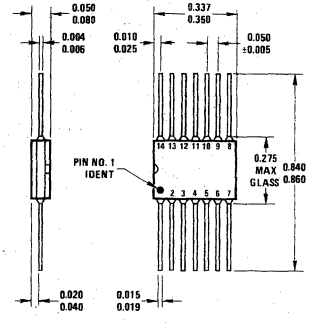
Package 25
12-Lead TO-8 Metal Can Package (G)



Package 25A
10-Lead Flat Package (F)



Package 26
14-Lead Flat Package (F)



Package 27
14-Lead Flat Package (W)

INCHES TO MILLIMETERS CONVERSION TABLE

INCHES	MM	INCHES	MM	INCHES	MM
0.001	0.0254	0.010	0.254	0.100	2.54
0.002	0.0508	0.020	0.508	0.200	5.08
0.003	0.0762	0.030	0.762	0.300	7.62
0.004	0.1016	0.040	1.016	0.400	10.16
0.005	0.1270	0.050	1.270	0.500	12.70
0.006	0.1524	0.060	1.524	0.600	15.24
0.007	0.1778	0.070	1.778	0.700	17.78
0.008	0.2032	0.080	2.032	0.800	20.32
0.009	0.2286	0.090	2.286	0.900	22.86

National Semiconductor Corporation
2900 Semiconductor Drive
Santa Clara, California 95051
(408) 732-5000
TWX: 910-339-9240

NS Electronics SDN BHD
Batu Berendam
Free Trade Zone
Malacca, Malaysia
Telephone: 5171
Telex: NSELECT 519 MALACCA (c/o Kuala Lumpur)

National Semiconductor GmbH
808 Fuerstenfeldbruck
Industriestrasse 10
West Germany
Telephone: (08141) 1371
Telex: 05-27649

National Semiconductor (UK) Ltd.
Larkfield Industrial Estate
Greenock, Scotland
Telephone: GOUROCK 33251
Telex: 778 632

NS Electronics (PTE) Ltd.
No. 1100 Lower Delta Rd.
Singapore 3
Telephone: 630011
Telex: NATSEMI RS 21402