CMOS
INTEGRATED CIRCUITS

National

CMOS INTEGRATED CIRCUITS
MAR 1975
National

INTRODUCTION TO 74C

74C is a CMOS pin for pin, function for function, equivalent to the 7400 TTL family. This new concept in CMOS was designed with the engineer in mind. Strict design rules were adhered to in the input and output characteristics, such as making all outputs capable of sinking 360 μA (two LPT^{2}L loads) and specifying all AC parameters at 50 pF loads. These consistent design rules will simplify system design by giving the engineer realistic and workable parameters. The engineer can take full advantage of his knowledge of the 7400 line and utilize the design tricks he has learned.

For those designs that require 4000 Series, National manufactures these circuits.

Manufactured under one or more of the following U.S. patents: 3083262, 3189758, 3231797, 3303356, 3317671, 3323071, 3381071, 3408542, 3421025, 3426423, 3440498, 3518750, 3519897, 3557431, 3560765, 3566218, 3571630, 3575609, 3579059, 3593069, 3597640, 3607469, 3617859, 3631312, 3633052, 3638131, 3648071, 3651565, 3693248.

NUMERICAL INDEX AND TABLE OF CONTENTS

74C DATA SHEETS IN NUMERICAL ORDER

CD4000 DATA SHEETS IN NUMERICAL ORDER

APPLICATION NOTES/BRIEFS

CMOS GUIDE

GATES

MM74C00	Quad 2-Input NAND Gate
MM74C02	Quad 2-Input NOR Gate
MM74C04	Hex Inverter
MM74C08	Quad 2-Input AND Gate
MM74C10	Triple 3-Input AND Gate
MM74C20	Dual 4-Input NAND Gate
MM74C30	8-Input NAND Gate
MM74C32	Quad 2-Input OR Gate
MM74C86	Quad 2-Input EXCLUSIVE-OR Gate
CD4001	Quad 2-Input NOR Gate
CD4002	Dual 4-Input NOR Gate
CD4007	Dual Complementary Pair Plus Inverter
CD4011	Quad 2-Input NAND Gate
CD4012	Dual 4-Input NAND Gate
CD4019	Quad AND-OR Select Gate
CD4023	Triple 3-Input NAND Gate
CD4025	Triple 3-Input NOR Gate
CD4030	Quad EXCLUSIVE-OR Gate
CD4069	Hex Inverter
CD4070B	Quad EXCLUSIVE-OR Gate

BUFFERS

MM74C901	Hex Inverting TTL Buffer
MM74C902	Hex Non-Inverting TTL Buffer
MM74C903	Hex Inverting PMOS Buffer
MM74C904	Hex Non-Inverting PMOS Buffer
MM74C906	Open Drain Buffer (Active Pull Down)
MM74C907	Open Drain Buffer (Active Pull Up)
MM80C95	TRI-STATE® Hex Buffer
MM80C97	TRI-STATE® Hex Buffer
CD4009	Hex Buffer (Inverting)
CD4010	Hex Buffer
CD4049	Hex Buffer (4009)
CD4050	Hex Buffer (4010)

FLIP-FLOPS

MM74C73	Dual J-K Flip-Flop
MM74C74	Dual D Flip-Flop
MM74C76	Dual J-K Flip-Flop
MM74C107	Dual J-K Flip-Flop
MM74C173	TRI-STATE® Quad D Flip-Flop
MM74C174	Hex D Flip-Flop
MM74C175	Quad D Flip-Flop
CD4013	Dual D Flip-Flop
CD4027	Dual J-K Flip-Flop
CD4042	Quad D Latch
CD4076	TRI-STATE® Quad D Flip-Flop

COUNTERS

MM74C90	Decade Counter
MM74C93	Binary Counter
MM74C160	Sync Decade Counter
MM74C161	Sync Binary Counter
MM74C162	Fully Sync Decade Counter
MM74C163	Fully Sync Binary Counter
MM74C192	Sync Up/Down Decade Counter

COUNTERS (CON'T)

MM74C193	Sync Up/Down Binary Counter
CD4017	Divide-by-10 Counter/Divider with 10 Decoded Outputs
CD4018	Presettable Divide-by-"N" Counter
CD4020	14 Stage Ripple Carry Binary Counter/Divider
CD4022	Divide-by-8 Counter/Divider with 8 Decoded Outputs
CD4024	Divide-by-8 Counter/Divider
CD4029	Presettable Up/Down Counter
CD4040	12-Bit Binary Ripple Counter
CD40192	Sync Up/Down Decade Counter
CD40193	Sync Up/Down Binary Counter

SHIFT REGISTERS

MM74C95	4-Bit R-S L-S Register
MM74C164	8-Bit S-In P-Out Shift Register
MM74C165	8-Bit S-In P-Out Shift Register
MM74C195	4-Bit Parallel Shift Register
CD4006	18-Bit Shift Register
CD4014	8-Bit Static Shift Register
CD4015	Dual 4-Bit Shift Register
CD4021	8-Bit Shift Register
CD4035	4-Bit Parallel-In/Parallel-Out Shift Register

DECODERS/MULTIPLEXERS

MM74C42	BCD-to-Decimal Decoder
MM74C48	BCD-to-7 Segment Decoder
MM74C151	8 Channel Digital Multiplexer
MM74C154	4:16 Decoder/Demultiplexer
MM74C157	Quad 2-Input Multiplexer
CD4016	Quad Bilateral Switch
CD4066	Quad Bilateral Switch
CD4028	BCD-to-Decimal Decoder
CD4511	BCD-to-7 Segment Decoder

MEMORIES

MM74C89	64-Bit TRI-STATE® Random Access Read/Write Memory
MM74C200	256-Bit TRI-STATE® Random Access Read/Write Memory

ARITHMETIC FUNCTIONS

MM74C83	4-Bit Binary Full Adder
MM74C85	4-Bit Magnitude Comparator

SPECIAL FUNCTIONS

MM74C14	Hex Schmitt Trigger
MM74C221	Dual Monostable Multivibrator
MM74C905	Successive Approximation Register
MM74C908	Dual −30V 250 mA Buffer
MM74C909	Linear Comparator
MM88C29	Dual Line and Clock Driver
MM88C30	Dual Line Driver
CD4016	Quad Bilateral Switch
CD40106	Hex Schmitt Trigger

54C/74C POWER CONSUMPTION CHARACTERISTICS GUIDE

Typical characteristics $T_A = 25°C$.

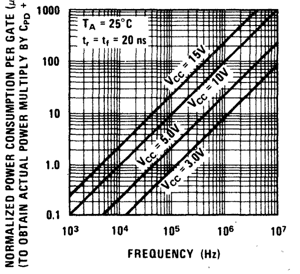
DEVICE TYPE/PRODUCT DESCRIPTION	C_{PD} (pF) (Note 3)	t_{pd} (ns) $C_L = 50$ pF $V_{CC} = 5.0V$	Δt_{pd}/pF CURVE	LTTL (TTL)* FAN OUT
MM54C00/MM74C00 Quad 2-Input NAND Gate	12	50	A	2
MM54C02/MM74C02 Quad 2-Input NOR Gate	12	50	A	2
MM54C04/MM74C04 Hex Inverter	12	50	A	2
MM54C08/MM74C08 Quad 2-Input AND Gate	14	80	A	2
MM54C10/MM74C10 Triple 3-Input AND Gate	18	60	A	2
MM54C14/MM74C14 Hex Schmitt Trigger	20	220	A	2
MM54C20/MM74C20 Dual 4-Input NAND Gate	30	70	A	2
MM54C30/MM74C30 8-Input NAND Gate	26	125	A	2
MM54C32/MM74C32 Quad 2-Input OR Gate	15	80	A	2
MM54C42/MM74C42 BCD-to-Decimal Decoder	50	200	A	2
MM54C48/MM74C48 BCD-to-7 Segment Decoder	NA	450 (1)	NA	2
MM54C73/MM74C73 Dual J-K Flip-Flop	40	180	A	2
MM54C74/MM74C74 Dual D Flip-Flop	40	180	A	2
MM54C76/MM74C76 Dual J-K Flip-Flop	40	180	A	2
MM54C83/MM74C83 4-Bit Binary Full Adder	120	300	A	2
MM54C85/MM74C85 4-Bit Magnitude Comparator	45	220 (1)	A	2
MM54C86/MM74C86 Quad 2-Input EXCLUSIVE-OR Gate	20	110	A	2
MM54C89/MM74C89 64-bit TRI-STATE® Random Access Memory	230	270	A	2
MM54C90/MM74C90 4-Bit Decade Counter	45	400	A	2
MM54C93/MM74C93 4-Bit Binary Counter	45	400	A	2
MM54C95/MM74C95 4-Bit R-S/L-S Register	100	200	A	2
MM54C107/MM74C107 Dual J-K Flip-Flop	40	180	A	2
MM54C151/MM74C151 8-Channel Digital Multiplexer	50	200 (1)	A	2
MM54C154/MM74C154 4:16 Decoder/Demultiplexer	60	275 (1)	A	2
MM54C157/MM74C157 Quad 2-Input Multiplexer	20	150 (1)	A	2
MM54C160/MM74C160 Sync Decade Counter	95	250 (2)	A	2
MM54C161/MM74C161 Sync 4-Bit Binary Counter	95	250 (2)	A	2
MM54C162/MM74C162 Sync Decade Counter	95	250 (2)	A	2
MM54C163/MM74C163 Sync 4-Bit Binary Counter	95	250 (2)	A	2
MM54C164/MM74C164 8-Bit SI/PO S/R	140	230 (2)	A	2
MM54C165/MM74C165 8-Bit PI/SO S/R	55	210 (2)	A	2
MM54C173/MM74C173 TRI-STATE® Quad D Flip-Flop	180	220 (2)	A	2
MM54C174/MM74C174 Hex D Flip-Flop	95	150 (2)	A	2
MM54C175/MM74C175 Quad D Flip-Flop	130	190 (2)	A	2
MM54C192/MM74C192 Sync Up/Down Decade Counter	70	250 (2)	A	2
MM54C193/MM74C193 Sync Up/Down Binary Counter	70	250 (2)	A	2
MM54C195/MM74C195 4-Bit Parallel S/R	130	200 (2)	A	2
MM54C221/MM74C221 Dual Monostable Multivibrators	NA	250 (2)	A	2
MM54C901/MM74C901 Hex Inverting TTL Buffer	30	38	B	2*
MM54C902/MM74C902 Hex Non-Inverting TTL Buffer	50	57	B	2*
MM54C903/MM74C903 Hex Inverting TTL Buffer	30	38	B	2*
MM54C904/MM74C904 Hex Non-Inverting TTL Buffer	50	57	B	2*
MM54C905/MM74C905 12-Bit Successive Approximation Register	100	200	A	2
MM54C906/MM74C906 Hex Open Drain N-Channel Buffers	30	NA	NA	2*
MM54C907/MM74C907 Hex Open Drain P-Channel Buffers	30	NA	NA	2*
MM54C908/MM74C908 Dual High Voltage CMOS Driver	NA	150 (1)	NA	NA
MM54C918/MM74C918 Dual High Voltage CMOS Driver	NA	150 (1)	NA	NA
MM70C95/MM80C95 TRI-STATE® Hex Non-Inverting Buffer	60	60	B	1*
MM70C97/MM80C97 TRI-STATE® Hex Non-Inverting Buffer	60	60	B	1*
MM78C29/MM88C29 Quad Single Ended Line Driver	150	200	NA	5*
MM78C30/MM88C30 Dual Differential Line Driver	200	350	NA	5*

Note 1: t_{pd} shown is from data input to output. For more detailed specifications see individual data sheet.

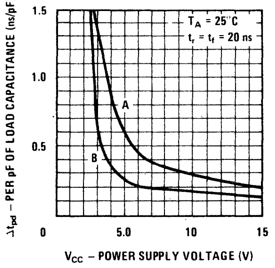
Note 2: t_{pd} shown is from clock to output. For more detailed specifications see individual data sheet.

Note 3: C_{PD} numbers shown are for independent identical functions within a package. For instance the total C_{PD} for a MM75C157 is 4 x 20 pF = 80 pF while the total C_{PD} for the MM74C173 is 180 pF because all flip-flops have a common clock.

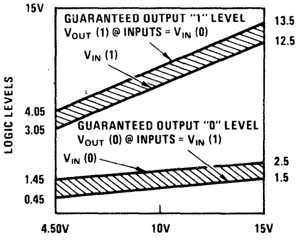
Normalized Typical Power Consumption vs Frequency



Typical Propagation Delay per pF of Load Capacitance vs Power Supply



Guaranteed Noise Margin Over Temperature vs V_{CC}



TOTAL POWER = $V_{CC}^2 \times f \times (C_{PD} + C_L) + V_{CC}\, I_{LEAKAGE}$

t_{pd} $\left. t_{pd} \right|_{C_L = C} = (C - 50)\ \text{pF} \times \dfrac{\Delta t_{pd}}{\text{pF}} + \left. t_{pd} \right|_{C_L = 50\ \text{pF}}$

For complete explanation on use of curves see application note AN-90, 54C/74C Family Characteristics.

CROSS REFERENCE GUIDE

74C CROSS REFERENCE

National	RCA	Harris	Teledyne	Motorola	TI	Fairchild
MM74C00		HD74C00	MM74C00			
MM74C02		HD74C02	MM74C02			
MM74C04	CD4069	HD74C04	MM74C04			
MM74C08						
MM74C10		HD74C10	MM74C10			
MM74C14	CD40106					
MM74C20		HD74C20	MM74C20			
MM74C30						
MM74C32						
MM74C42		HD74C42	MM74C42			
MM74C48	*CD4511			*MC14511		
MM74C73		HD74C73	MM74C73			
MM74C74		HD74C74	MM74C74			
MM74C76		HD74C76	MM74C76			
MM74C83						
MM74C85				*MC14585		
MM74C86	CD4030A CD4070B			MC14030 MC14507		
MM74C89						F340089
MM74C90						
MM74C93						
MM74C95			MM74C95			
MM74C107		HD74C107				
MM74C151		HD74C151	MM74C151			
MM74C154		HD74C154	MM74C154			
MM74C157		HD74C157	MM74C157			
MM74C160		HD74C160	MM74C160		TP4360	F340160
MM74C161		HD74C161	MM74C161		TP4361	F340161
MM74C162		HD74C162	MM74C162		TP4362	F340162
MM74C163		HD74C163	MM74C163		TP4363	F340163
MM74C164		HD74C164	MM74C164			
MM74C165		HD74C165				
MM74C173	CD4076A	HD74C173	MM74C173			
MM74C174						F340174
MM74C175						F340175
MM74C192	CD40192	HD74C192	MM74C192			F340192
MM74C193	CD40193	HD74C193	MM74C193			F340193
MM74C195			MM74C195			F340195
MM74C200						
MM74C221						
MM74C901		HD74C901				
MM74C902		HD74C902				
MM74C903		HD74C903				
MM74C904		HD74C904				
MM74C905						
MM74C906		HD74C906				
MM74C907		HD74C907				
MM74C908						
MM74C918						
MM80C95						
MM80C97						F340097
MM80C98						F340098
MM88C29						
MM88C30						

*Functional equivalents.

4000 CROSS REFERENCE

National	RCA	Motorola	Solid State Scientific	Solitron	Harris	Fairchild	TI
CD4001	CD4001A	MC14001A	SCL4001A	CM4001A	HD4001A	F34001A	TP4001A
CD4002	CD4002A	MC14002A	SCL4002A	CM4002A	HD4002A	F34002A	TP4002A
CD4006	CD4006A	MC14006A	SCL4006A	CM4006A			
CP4007	CD4007A	MC14007A	SCL4007A	CM4007A	HD4007A		TP4007A
CD4009	CD4009A	MC14009A	SCL4009A	CM4009A	HD4009A		TP4009A
CD4010	CD4010A	MC14010A	SCL4010A	CM4010A	HD4010A		TP4010A
CD4011	CD4011A	MC14011A	SCL4011A	CM40011A	HD4011A	F34011A	TP4011A
CD4012	CD4012A	MC14012A	SCL4012A	CM40012A	HD4012A	F34012A	TP4012A
CD4013	CD4013A	MC14013A	SCL4013A	CM4013A	HD4013A	F34013A	TP4013A
CD4014	CD4014A		SCL4014A	CM4014A	HD4014A		TP4014A
CD4015	CD4015A	MC14015A			HD4015		TP4015A
CD4016	CD4016A	MC14016A	SCL4016A	CM4016A			TP4016A
CD4017	CD4017A	MC14017A		CM4017A	HD4017A		
CD4018	CD4018A				HD4018		
CD4019	CD4019A		SCL4019A	CM40019A	HD4019A	F34019A	TP4019A
CD4020	CD4020A	MC14020A	SCL4020A	CM4020A	HD4020A		
CD4021	CD4021A	MC14021A	SCL4021A	CM4021A	HD4021A		TP4021A
CD4022	CD4022A	MC14022A	SCL4022A	CM4022A	HD4022A		
CD4023	CD4023A	MC14023A	SCL4023A	CM4023A	HD4023A	F34023A	TP4023A
CD4024	CD4024A	MC14024A	SCL4024A	CM4024A	HD4024A		
CD4025	CD4025A	MC14025A		CM4025A	HD4025A	F34025A	
CD4027	CD4027A	MC14027A	SCL4027A		HD4027A	F34027A	TP4027A
CD4028	CD4028A	MC14028A			HD4028		TP4028A
CD4029	CD4029A				HD4029		TP4029A
CD4030	CD4030A		SCL4030A		HD4030A	F34030A	
CD4035	CD4035A	MC14035A			HD4035A		
CD4040	CD4040A	MC14040A			HD4040		
CD4042	CD4042A	MC14042A			HD4042		
CD4049	CD4049A	MC14049A			HD4049A	F34049A	TP4049A
CD4050	CD4050A	MC14050A			HD4050A	F34050A	TP4050A
CD4066	CD4066A				HD4066		
CD4069	CD4069A						
CD4070B	CD4070B	MC14507A					
CD4076	CD4076A						
CD40106	CD40106						
CD40192	CD40192A						
CD40193	CD40193A						
CD4511	CD4511A	MC14511A					

MM54C00/MM74C00 quad two-input NAND gate
MM54C02/MM74C02 quad two-input NOR gate
MM54C04/MM74C04 hex inverter
MM54C10/MM74C10 triple three-input NAND gate
MM54C20/MM74C20 dual four-input NAND gate

general description

These logic gates employ complementary MOS (CMOS) to achieve wide power supply operating range, low power consumption, high noise immunity and symmetric controlled rise and fall times. With features such as this the 54C/74C logic family is close to ideal for use in digital systems. Function and pin out compatibility with series 54/74 devices minimizes design time for those designers already familiar with the standard 54/74 logic family.

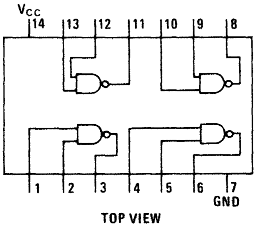
All inputs are protected from damage due to static discharge by diode clamps to V_{CC} and GND.

features

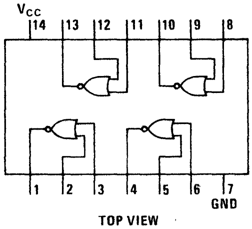
■ Wide supply voltage range	3.0V to 15V
■ Guaranteed noise margin	1.0V
■ High noise immunity	0.45 V_{CC} typ.
■ Low power consumption	10 nW/package typ.
■ Low power TTL compatibility	fan out of 2 driving 74L

connection diagrams

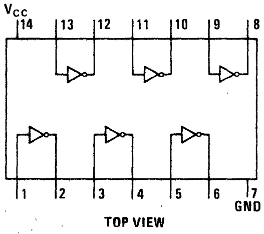
MM54C00/MM74C00



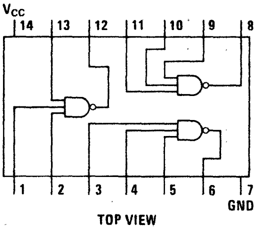
MM54C02/MM74C02



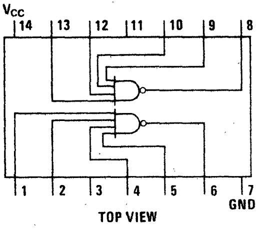
MM54C04/MM74C04



MM54C10/MM74C10



MM54C20/MM74C20



absolute maximum ratings (Note 1)

Voltage at Any Pin	$-0.3V$ to $V_{CC} + 0.3V$
Operating Temperature Range	
54C	−55°C to +125°C
74C	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Maximum V_{CC} Voltage	16V
Package Dissipation	500 mW
Lead Temperature (Soldering, 10 seconds)	300°C

dc electrical characteristics

Min/max limits apply across the guaranteed temperature range unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CMOS TO CMOS					
Logical "1" Input Voltage ($V_{IN(1)}$)	V_{CC} = 5.0V	3.5			V
	V_{CC} = 10V	8.0			V
Logical "0" Input Voltage ($V_{IN(0)}$)	V_{CC} = 5.0V			1.5	V
	V_{CC} = 10V			2.0	V
Logical "1" Output Voltage ($V_{OUT(1)}$)	V_{CC} = 5.0V, I_O = −10μA	4.5			V
	V_{CC} = 10V, I_O = −10μA	9.0			V
Logical "0" Output Voltage ($V_{OUT(0)}$)	V_{CC} = 5.0V, I_O = +10μA			0.5	V
	V_{CC} = 10V, I_O = +10μA			1.0	V
Logical "1" Input Current ($I_{IN(1)}$)	V_{CC} = 15V, V_{IN} = 15V		0.005	1.0	μA
Logical "0" Input Current ($I_{IN(0)}$)	V_{CC} = 15V, V_{IN} = 0V	−1.0	−0.005		μA
Supply Current (I_{CC})	V_{CC} = 15V		0.01	15	μA
LOW POWER TO CMOS					
Logical "1" Input Voltage ($V_{IN(1)}$)	54C, V_{CC} = 4.5V	V_{CC} − 1.5			V
	74C, V_{CC} = 4.75V	V_{CC} − 1.5			V
Logical "0" Input Voltage ($V_{IN(0)}$)	54C, V_{CC} = 4.5V			0.8	V
	74C, V_{CC} = 4.75V			0.8	V
Logical "1" Output Voltage ($V_{OUT(1)}$)	54C, V_{CC} = 4.5V, I_O = −10μA	4.4			V
	74C, V_{CC} = 4.75V, I_O = −10μA	4.4			V
Logical "0" Output Voltage ($V_{OUT(0)}$)	54C, V_{CC} = 4.5V, I_O = +10μA			0.4	V
	74C, V_{CC} = 4.75V, I_O = +10μA			0.4	V
CMOS TO LOW POWER					
Logical "1" Input Voltage ($V_{IN(1)}$)	54C, V_{CC} = 4.5V	4.0			V
	74C, V_{CC} = 4.75V	4.0			V
Logical "0" Input Voltage ($V_{IN(0)}$)	54C, V_{CC} = 4.5V			1.0	V
	74C, V_{CC} = 4.75V			1.0	V
Logical "1" Output Voltage ($V_{OUT(1)}$)	54C, V_{CC} = 4.5V, I_O = −360μA	2.4			V
	74C, V_{CC} = 4.75V, I_O = −360μA	2.4			V
Logical "0" Output Voltage ($V_{OUT(0)}$)	54C, V_{CC} = 4.5V, I_O = 360μA			0.4	V
	74C, V_{CC} = 4.75, I_O = 360μA			0.4	V
OUTPUT DRIVE (See 54C/74C Family Characteristics Data Sheet)					
Output Source Current (I_{SOURCE})	V_{CC} = 5.0V, $V_{IN(0)}$ = 0V T_A = 25°C, V_{OUT} = 0V	1.75			mA
Output Source Current (I_{SOURCE})	V_{CC} = 10V, $V_{IN(0)}$ = 0V T_A = 25°C, V_{OUT} = 0V	8.0			mA
Output Sink Current (I_{SINK})	V_{CC} = 5.0V, $V_{IN(1)}$ = 5.0V T_A = 25°C, V_{OUT} = V_{CC}	1.75			mA
Output Sink Current (I_{SINK})	V_{CC} = 10V, $V_{IN(1)}$ = 10V T_A = 25°C, V_{OUT} = V_{CC}	8.0			mA

ac electrical characteristics

$T_A = 25°C$, $C_L = 50$ pF, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
MM54C00/MM74C00, MM54C02/MM74C02, MM54C04/MM74C04					
Propagation Delay Time to Logical "1" or "0" (t_{pd})	$V_{CC} = 5.0V$ $V_{CC} = 10V$		50 30	90 60	ns ns
Input Capacitance (C_{IN})	(Note 2)		6.0		pF
Power Dissipation Capacitance (C_{PD})	(Note 3) Per Gate or Inverter		12		pF
MM54C10/MM74C10					
Propagation Delay Time to Logical "1" or "0" (t_{pd})	$V_{CC} = 5.0V$ $V_{CC} = 10V$		60 35	100 70	ns ns
Input Capacitance (C_{IN})	(Note 2)		7.0		pF
Power Dissipation Capacitance (C_{PD})	(Note 3) Per Gate		18		pF
MM54C20/MM74C20					
Propagation Delay Time to Logical "1" or "0" (t_{pd})	$V_{CC} = 5.0V$ $V_{CC} = 10V$		70 40	115 80	ns ns
Input Capacitance (C_{IN})	(Note 2)		9		pF
Power Dissipation Capacitance (C_{PD})	(Note 3) Per Gate		30		pF

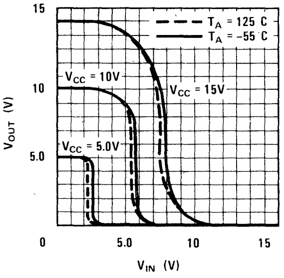
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

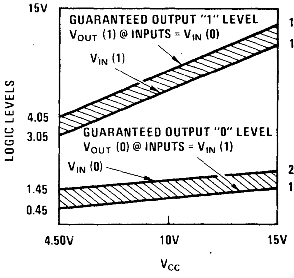
Note 3: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note — AN-90

typical performance characteristics

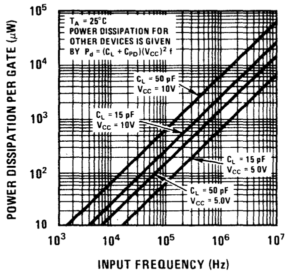
Gate Transfer Characteristics



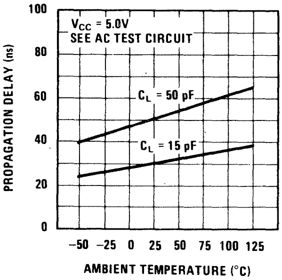
Guaranteed Noise Margin Over Temperature vs V_{CC}



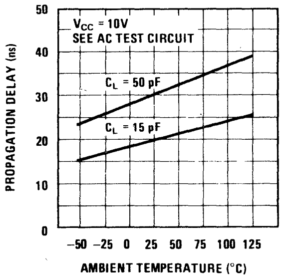
Power Dissipation vs Frequency MM54C00/MM74C00, MM54C02/MM74C02, MM54C04/MM74C04



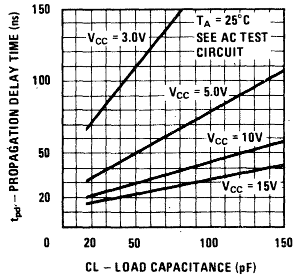
Propagation Delay vs Ambient Temperature MM54C00/MM74C00, MM54C02/MM74C02, MM54C04/MM74C04



Propagation Delay vs Ambient Temperature MM54C00/MM74C00, MM54C02/MM74C02, MM54C04/MM74C04

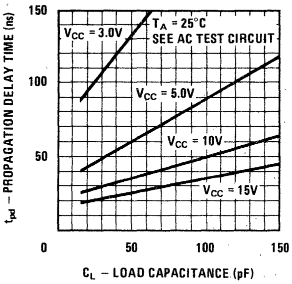


Propagation Delay Time vs Load Capacitance MM54C00/MM74C00, MM54C02/MM74C02, MM54C04/MM74C04

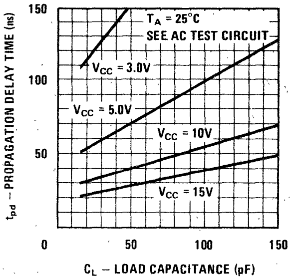


typical performance characteristics (con't)

Propagation Delay Time vs Load Capacitance MM54C10/MM74C10

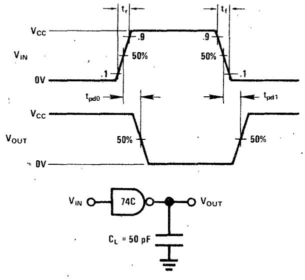


Propagation Delay Time vs Load Capacitance MM54C20/MM74C20



switching time waveforms and ac test circuits

CMOS to CMOS



NOTE: DELAYS MEASURED WITH INPUT t_r, $t_f \leq 20$ ns.

MM54C08/MM74C08 quad 2-input AND gate
MM54C86/MM74C86 quad 2-input EXCLUSIVE-OR gate

general description

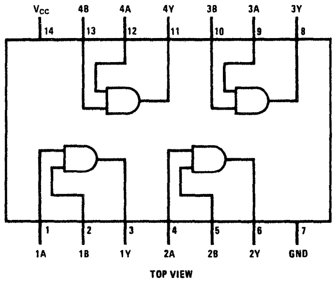
Employing complementary MOS (CMOS) transistors to achieve wide power supply operating range, low power consumption and high noise margin these gates provide basic functions used in the implementation of digital integrated circuit systems. The N and P-channel enchancement mode transistors provide a symmetrical circuit with output swing essentially equal to the supply voltage. No dc power other than that caused by leakage current is consumed during static condition. All inputs are protected from damage due to static discharge by diode clamps to V_{CC} and GND.

features

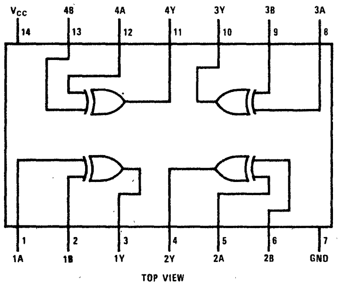
■ Wide supply voltage range	3.0V to 15V
■ Guaranteed noise margin	1.0V
■ High noise immunity	0.45 V_{CC} typ
■ Low power TTL compatibility	fan out of 2 driving 74L
■ Low power consumption	10 nW/package typ

connection diagrams

MM54C08/MM74C08



MM54C86/MM74C86



truth tables

MM54C08/MM74C08

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	L
H	L	L
H	H	H

H = High Level L= Low Level

MM54C86/MM74C86

INPUTS		OUTPUTS
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

absolute maximum ratings (Note 1)

Voltage at Any Pin	–0.3V to V_{CC} +0.3V
Operating Temperature Range	
MM54C08, MM54C86	–55°C to +125°C
MM74C08, MM74C86	–40°C to +85°C
Storage Temperature Range	–65°C to +150°C
Package Dissipation	500 mW
Operating V_{CC} Range	3.0V to 15V
Absolute Maximum V_{CC}	16V
Lead Temperature (Soldering, 10 seconds)	300°C

dc electrical characteristics

Min/max limits apply across temperature range, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CMOS TO CMOS					
Logical "1" Input Voltage ($V_{IN(1)}$)	V_{CC} = 5.0V V_{CC} = 10V	3.5 8.0			V V
Logical "0" Input Voltage ($V_{IN(0)}$)	V_{CC} = 5.0V V_{CC} = 10V			1.5 2.0	V V
Logical "1" Output Voltage ($V_{OUT(1)}$)	V_{CC} = 5.0V, I_O = –10μA V_{CC} = 10V, I_O = –10μA	4.5 9.0			V V
Logical "0" Output Voltage ($V_{OUT(0)}$)	V_{CC} = 5.0V, I_O = +10μA V_{CC} = 10V, I_O = +10μA			0.5 1.0	V V
Logical "1" Input Current ($I_{IN(1)}$)	V_{CC} = 15V, V_{IN} = 15V		0.005	1.0	μA
Logical "0" Input Current ($I_{IN(0)}$)	V_{CC} = 15V, V_{IN} = 0V	–1.0	–0.005		μA
Supply Current (I_{CC})	V_{CC} = 15V		0.01	15	μA
CMOS/LPTTL INTERFACE					
Logical "1" Input Voltage ($V_{IN(1)}$)	54C, V_{CC} = 4.5V 74C, V_{CC} = 4.75V	V_{CC} – 1.5 V_{CC} – 1.5			V V
Logical "0" Input Voltage ($V_{IN(0)}$)	54C, V_{CC} = 4.5V 74C, V_{CC} = 4.75V			0.8 0.8	V V
Logical "1" Output Voltage ($V_{OUT(1)}$)	54C, V_{CC} = 4.5V, I_O = –360μA 74C, V_{CC} = 4.75V, I_O = –360μA	2.4 2.4			V V
Logical "0" Output Voltage ($V_{OUT(0)}$)	54C, V_{CC} = 4.5V, I_O = +360μA 74C, V_{CC} = 4.75V, I_O = +360μA			0.4 0.4	V V
OUTPUT DRIVE (See 54C/74C Family Characteristics Data Sheet)					
Output Source Current (I_{SOURCE}) (P-Channel)	V_{CC} = 5.0V, V_{OUT} = 0V T_A = 25°C	–1.75	–3.3		mA
Output Source Current (I_{SOURCE}) (P-Channel)	V_{CC} = 10V, V_{OUT} = 0V T_A = 25°C	–8.0	–15		mA
Output Sink Current (I_{SINK}) (N-Channel)	V_{CC} = 5.0V, V_{OUT} = V_{CC} T_A = 25°C	1.75	3.6		mA
Output Sink Current (I_{SINK}) (N-Channel)	V_{CC} = 10V, V_{OUT} = V_{CC} T_A = 25°C	8.0	16		mA

ac electrical characteristics

(MM54C08/MM74C08) $T_A = 25°C$, $C_L = 50$ pF, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Propagation Delay Time to Logical "1" or "0" (t_{pd})	$V_{CC} = 5.0V$		80	140	ns
	$V_{CC} = 10V$		40	70	ns
Input Capacitance (C_{IN})	Note 2		5.0		pF
Power Dissipation Capacitance (C_{pd})	Note 3 Per Gate		14		pF

ac electrical characteristics

(MM54C86/MM74C86) $T_A = 25°C$, $C_L = 50$ pF, unless otherwise specified

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Propagation Delay Time to Logical "1" or "0" (t_{pd})	$V_{CC} = 5.0V$		110	185	ns
	$V_{CC} = 10V$		50	90	ns
Input Capacitance (C_{IN})	Note 2		5.0		pF
Power Dissipation Capacitance (C_{pd})	Note 3 Per Gate		20		pF

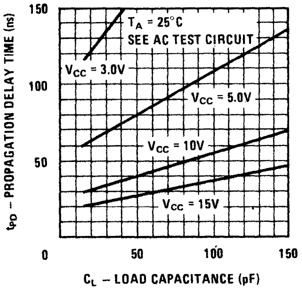
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

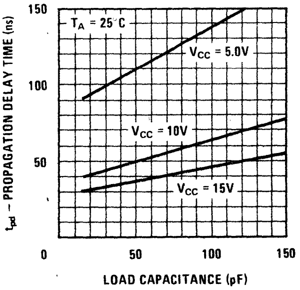
Note 3: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note, AN-90.

typical performance characteristics

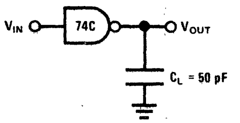
Propagation Delay Time vs Load Capacitance MM54C08/MM74C08



Propagation Delay Time vs Load Capacitance MM54C86/MM74C86

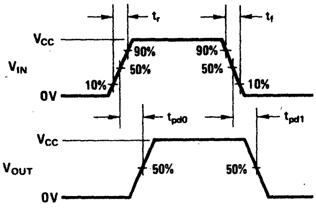


ac test circuit



NOTE: DELAYS MEASURED WITH INPUT t_r, t_f = 20 ns

switching time waveforms



MM54C14/MM74C14 hex schmitt trigger

general description

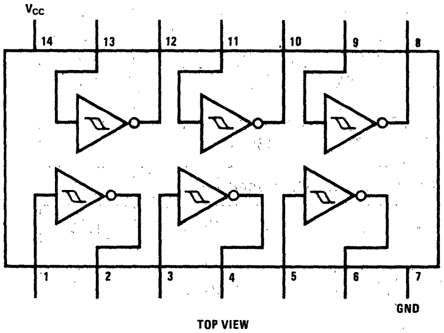
The MM54C14/MM74C14 Hex Schmitt Trigger is a monolithic complementary MOS (CMOS) integrated circuit constructed with N and P-channel enhancement transistors. The positive and negative going threshold voltages, V_{T+} and V_{T-}, show low variation with respect to temperature (typ 0.0005V/°C at V_{CC} = 10V), and hysteresis, $V_{T+} - V_{T-} \geq 0.2\ V_{CC}$ is guaranteed.

All inputs are protected from damage due to static discharge by diode clamps to V_{CC} and GND.

features

■ Wide supply voltage range	3.0V to 15V
■ High noise immunity	0.70 V_{CC} typ
■ Low power TTL compatibility	fan out of 2 driving 74L
■ Hysteresis	0.4 V_{CC} typ 0.2 V_{CC} guaranteed

connection diagram



TOP VIEW

absolute maximum ratings

Voltage at Any Pin	−0.3V to V_{CC} + 0.3V
Operating Temperature Range	
MM54C14	−55°C to +125°C
MM74C14	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C

Package Dissipation	500 mW
Operating V_{CC} Range	3.0V to 15V
Absolute Maximum V_{CC}	16V
Lead Temperature (Soldering, 10 seconds)	300°C

dc electrical characteristics

Min/max limits apply across temperature range, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CMOS TO CMOS					
V_{T+} Positive Going Threshold Voltage	V_{CC} = 5V	3.0	3.6	4.3	V
	V_{CC} = 10V	6.0	6.8	8.6	V
	V_{CC} = 15V	9.0	10.0	12.9	
V_{T-} Negative Going Threshold Voltage	V_{CC} = 5V	0.7	1.4	2.0	V
	V_{CC} = 10V	1.4	3.2	4.0	V
	V_{CC} = 15V	2.1	5.0	6.0	
Hysteresis ($V_{T+} - V_{T-}$)	V_{CC} = 5V	1.0	2.2	3.6	V
	V_{CC} = 10V	2.0	3.6	7.2	V
	V_{CC} = 15V	3.0	5.0	10.8	V
Logical "1" Output Voltage ($V_{OUT(1)}$)	V_{CC} = 5V, I_O = −10µA	4.5			V
	V_{CC} = 10V, I_O = −10µA	9.0			V
Logical "0" Output Voltage ($V_{OUT(0)}$)	V_{CC} = 5V, I_O = +10µA			0.5	V
	V_{CC} = 10V, I_O = +10µA			1.0	V
Logical "1" Input Current ($I_{IN(1)}$)	V_{CC} = 15V, V_{IN} = 15V		0.005	1.0	µA
Logical "0" Input Current ($I_{IN(0)}$)	V_{CC} = 15V, V_{IN} = 0V	−1.0	−0.005		µA
Supply Current (I_{CC})	V_{CC} = 15V, V_{IN} = 0V/15V		0.05	15	µA
	V_{CC} = 5V, V_{IN} = 2.5V (Note 4)		20		µA
	V_{CC} = 10V, V_{IN} = 5V (Note 4)		200		µA
	V_{CC} = 15V, V_{IN} = 7.5V (Note 4)		600		µA
CMOS/LPTTL INTERFACE					
Logical "1" Input Voltage ($V_{IN(1)}$)	V_{CC} = 5V	4.3			V
Logical "0" Input Voltage ($V_{IN(0)}$)	V_{CC} = 5V			0.7	V
Logical "1" Output Voltage ($V_{OUT(1)}$)	54C, V_{CC} = 4.5V, I_O = −360µA	2.4			V
	74C, V_{CC} = 4.75V, I_O = −360µA	2.4			V
Logical "0" Output Voltage ($V_{OUT(0)}$)	54C, V_{CC} = 4.5V, I_O = 360µA			0.4	V
	74C, V_{CC} = 4.75V, I_O = 360µA			0.4	V
OUTPUT DRIVE (See 54C/74C Family Characteristics Data Sheet)					
Output Source Current (I_{SOURCE}) (P-Channel)	V_{CC} = 5V, V_{OUT} = 0V, T_A = 25°C	−1.75	−3.3		mA
Output Source Current (I_{SOURCE}) (P-Channel)	V_{CC} = 10V, V_{OUT} = 0V, T_A = 25°C	−8.0	−15		mA
Output Sink Current (I_{SINK}) (N-Channel)	V_{CC} = 5V, V_{OUT} = V_{CC}, T_A = 25°C	1.75	3.6		mA
Output Sink Current (I_{SINK}) (N-Channel)	V_{CC} = 10V, V_{OUT} = V_{CC}, T_A = 25°C	8.0	16		mA

ac electrical characteristics

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Propagation Delay from Input to Output (t_{pd0} or t_{pd1})	V_{CC} = 5V V_{CC} = 10		220 80	400 200	ns ns
Input Capacitance	Any Input (Note 2)		5.0		pF
Power Dissipation Capacitance (C_{PD})	(Note 3) Per Gate		20		pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

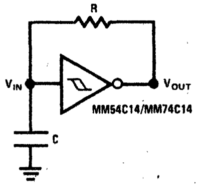
Note 2: Capacitance is guaranteed by periodic testing.

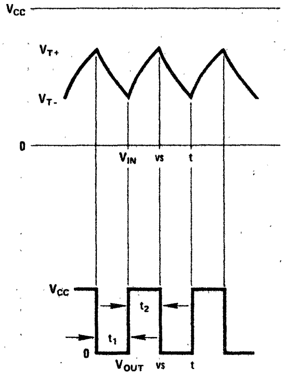
Note 3: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note, AN-90.

Note 4: Only one of the six inputs is at 1/2 V_{CC}, the others are either at V_{CC} or GND.

typical application

Low Power Oscillator





$$t_1 \approx RC\,\ell n\,\frac{V_{T+}}{V_{T-}}$$

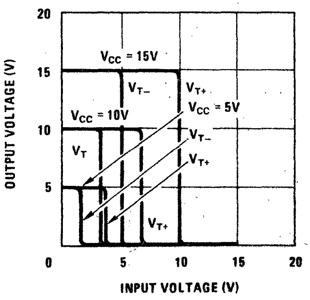
$$t_2 \approx RC\,\ell n\,\frac{V_{CC}-V_{T-}}{V_{CC}-V_{T+}}$$

$$f \approx \frac{1}{RC\,\ell n\,\dfrac{V_{T+}\,(V_{CC}-V_{T-})}{V_{T-}\,(V_{CC}-V_{T+})}}$$

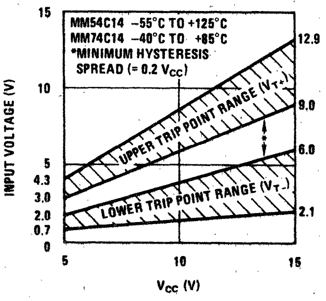
Note: The equations assume $t_1 + t_2 >> t_{pd0} + t_{pd1}$

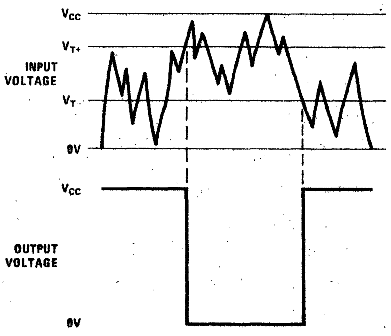
typical performance characteristics

Typical Transfer Characteristics



Guaranteed Trip Point Range





Note: For more information on output drive characteristics, power dissipation, and propagation delays, see AN-90.

MM54C30/MM74C30 8-input NAND gate

general description

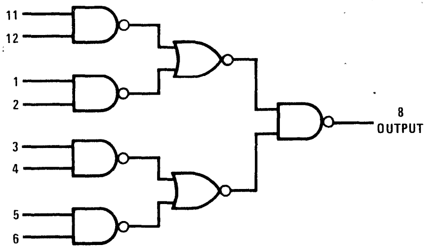
The logic gate employs complementary MOS (CMOS) to achieve wide power supply operating range, low power consumption and high noise immunity. Function and pin out compatibility with series 54/74 devices minimizes design time for those designers familiar with the standard 54/74 logic family.

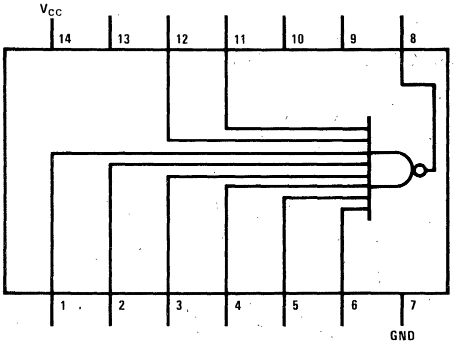
All inputs are protected from damage due to static discharge by diode clamps to V_{CC} and GND.

features

■ Wide supply voltage range	3.0V to 15V
■ Guaranteed noise margin	1.0V
■ High noise immunity	0.45 V_{CC} typ
■ Low power TTL compatibility	fan out of 2 driving 74L

logic and connection diagrams





TOP VIEW

absolute maximum ratings (Note 1)

Voltage at Any Pin	−0.3V to V_{CC} + 0.3V
Operating Temperature Range	
MM54C30	−55°C to +125°C
MM74C30	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500 mW
Operating V_{CC} Range	3.0V to 15V
Absolute Maximum V_{CC}	16V
Lead Temperature (Soldering, 10 seconds)	300°C

dc electrical characteristics

Min/max limits apply across temperature range, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CMOS TO CMOS					
Logical "1" Input Voltage ($V_{IN(1)}$)	V_{CC} = 5.0V V_{CC} = 10V	3.5 8.0			V V
Logical "0" Input Voltage ($V_{IN(0)}$)	V_{CC} = 5.0V V_{CC} = 10V			1.5 2.0	V V
Logical "1" Output Voltage ($V_{OUT(1)}$)	V_{CC} = 5.0V, I_O = −10μA V_{CC} = 10V, I_O = −10μA	4.5 9.0			V V
Logical "0" Output Voltage ($V_{OUT(0)}$)	V_{CC} = 5.0V, I_O = +10μA V_{CC} = 10V, I_O = +10μA			0.5 1.0	V V
Logical "1" Input Current ($I_{IN(1)}$)	V_{CC} = 15V, V_{IN} = 15V		0.005	1.0	μA
Logical "0" Input Current ($I_{IN(0)}$)	V_{CC} = 15V, V_{IN} = 0V	−1.0	−0.005		μA
Supply Current (I_{CC})	V_{CC} = 15V		0.01	15	μA
CMOS/LPTTL INTERFACE					
Logical "1" Input Voltage ($V_{IN(1)}$)	54C, V_{CC} = 4.5V 74C, V_{CC} = 4.75V	V_{CC}−1.5 V_{CC}−1.5			V V
Logical "0" Input Voltage ($V_{IN(0)}$)	54C, V_{CC} = 4.5V 74C, V_{CC} = 4.75V			0.8 0.8	V V
Logical "1" Output Voltage ($V_{OUT(1)}$)	54C, V_{CC} = 4.5V, I_O = −360μA 74C, V_{CC} = 4.75V, I_O = −360μA	2.4 2.4			V V
Logical "0" Output Voltage ($V_{OUT(0)}$)	54C, V_{CC} = 4.5V, I_O = 360μA 74C, V_{CC} = 4.75V, I_O = 360μA			0.4 0.4	V V
OUTPUT DRIVE (See 54C/74C Family Characteristics Data Sheet)					
Output Source Current (I_{SOURCE}) (P-Channel)	V_{CC} = 5.0V, V_{OUT} = 0V, T_A = 25°C	−1.75	−3.3		mA
Output Source Current (I_{SOURCE}) (P-Channel)	V_{CC} = 10V, V_{OUT} = 0V, T_A = 25°C	−8.0	−15		mA
Output Sink Current (I_{SINK}) (N-Channel)	V_{CC} = 5.0V, V_{OUT} = V_{CC}, T_A = 25°C	1.75	3.6		mA
Output Sink Current (I_{SINK}) (N-Channel)	V_{CC} = 10V, V_{OUT} = V_{CC}, T_A = 25°C	8.0	16		mA

ac electrical characteristics $T_A = 25°C$, $C_L = 50$ pF, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Propagation Delay Time to Logical "1" or "0" (t_{pd})	$V_{CC} = 5.0V$ $V_{CC} = 10V$		125 55	180 90	ns ns
Input Capacitance (C_{IN})	(Note 2)		4.0		pF
Power Dissipation Capacitance (C_{pd})	(Note 3) Per Gate		26		pF

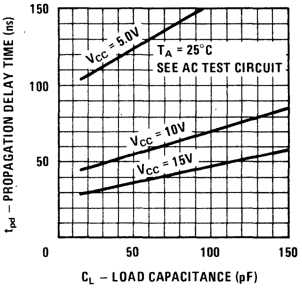
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

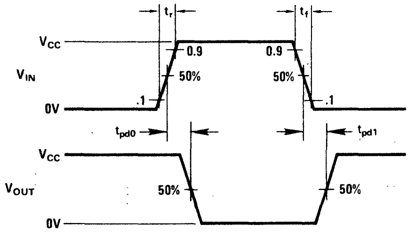
Note 3: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note, AN-90.

typical performance characteristics

Propagation Delay Time vs Load Capacitance

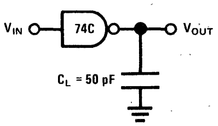


switching time waveforms



NOTE: DELAYS MEASURED WITH INPUT t_r, t_f = 20 ns.

ac test circuit



MM54C32/MM74C32 quad 2-input OR gate

general description

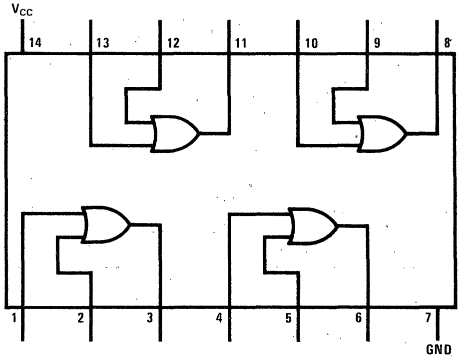
Employing complementary MOS (CMOS) transistors to achieve low power and high noise margin, these gates provide the basic functions used in the implementation of digital integrated circuit systems. The N and P-channel enhancement mode transistors provide a symmetrical circuit with output swings essentially equal to the supply voltage. This results in high noise immunity over a wide supply voltage range. No dc power other than that caused by leakage current is consumed during static conditions. All inputs are protected against static discharge damage.

features

■ Wide supply voltage range	3.0V to 15V
■ Guaranteed noise margin	1.0V
■ High noise immunity	0.45 V_{CC} typ
■ Low power TTL compatibility	fan out of 2 driving 74L

---

connection diagram



TOP VIEW

absolute maximum ratings (Note 1)

Voltage at Any Pin	−0.3V to V_{CC} +0.3V
Operating Temperature Range	
MM54C32	−55°C to +125°C
MM74C32	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500 mW
Operating V_{CC} Range	3.0V to 15V
Absolute Maximum V_{CC}	16V
Lead Temperature (Soldering, 10 seconds)	300°C

dc electrical characteristics

Min/max limits apply across temperature range, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CMOS TO CMOS					
Logical "1" Input Voltage ($V_{IN(1)}$)	V_{CC} = 5.0V	3.5			V
	V_{CC} = 10V	8.0			V
Logical "0" Input Voltage ($V_{IN(0)}$)	V_{CC} = 5.0V			1.5	V
	V_{CC} = 10V			2.0	V
Logical "1" Output Voltage ($V_{OUT(1)}$)	V_{CC} = 5.0V, I_O = −10μA	4.5			V
	V_{CC} = 10V, I_O = −10μA	9.0			V
Logical "0" Output Voltage ($V_{OUT(0)}$)	V_{CC} = 5.0V, I_O = 10μA			0.5	V
	V_{CC} = 10V, I_O = 10μA			1.0	V
Logical "1" Input Current ($I_{IN(1)}$)	V_{CC} = 15V, V_{IN} = 15V		0.005	1.0	μA
Logical "0" Input Current ($I_{IN(0)}$)	V_{CC} = 15V, V_{IN} = 0V	−1.0	−0.005		μA
Supply Current (I_{CC})	V_{CC} = 15V		0.05	15	μA
CMOS/LPTTL INTERFACE					
Logical "1" Input Voltage ($V_{IN(1)}$)					
MM54C32	V_{CC} = 4.5V	V_{CC}−1.5			V
MM74C32	V_{CC} = 4.75V	V_{CC}−1.5			V
Logical "0" Input Voltage ($V_{IN(0)}$)					
MM54C32	V_{CC} = 4.5V			0.8	V
MM74C32	V_{CC} = 4.75V			0.8	V
Logical "1" Output Voltage ($V_{OUT(1)}$)					
MM54C32	V_{CC} = 4.5V, I_O = −360μA	2.4			V
MM74C32	V_{CC} = 4.75V, I_O = −360μA	2.4			V
Logical "0" Output Voltage ($V_{OUT(0)}$)					
MM54C32	V_{CC} = 4.5V, I_O = 360μA			0.4	V
MM74C32	V_{CC} = 4.75V, I_O = 360μA			0.4	V
OUTPUT DRIVE (See 54C/74C Family Characteristics Data Sheet)					
Output Source Current (I_{SOURCE}) (P-Channel)	V_{CC} = 5.0V, V_{OUT} = 0V T_A = 25°C	−1.75	−3.3		mA
Output Source Current (I_{SOURCE}) (P-Channel)	V_{CC} = 10V, V_{OUT} = 0V T_A = 25°C	−8.0	−15		mA
Output Sink Current (I_{SINK}) (N-Channel)	V_{CC} = 5.0V, V_{OUT} = V_{CC} T_A = 25°C	1.75	3.6		mA
Output Sink Current (I_{SINK}) (N-Channel)	V_{CC} = 10V, V_{OUT} = V_{CC} T_A = 25°C	8.0	16		mA

ac electrical characteristics

T_A = 25°C, C_L = 50 pF, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Propagation Delay Time to Logical "1" (t_{pd1}) or "0" (t_{pd0})	V_{CC} = 5V		80	150	ns
	V_{CC} = 10V		35	70	ns
Input Capacitance (C_{IN})	Any Input (Note 2)		5		pF
Power Dissipation Capacitance (C_{pd})	Per Gate (Note 3)		15		pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note, AN-90.

MM54C42/MM74C42 BCD to decimal decoder

general description

The MM54C42/MM74C42 one-of-ten decoder is a monolithic complementary MOS (CMOS) integrated circuit constructed with N- and P-channel enhancement transistors. This decoder produces a logical "0" at the output corresponding to a four bit binary input from zero to nine, and a logical "1" at the other outputs. For binary inputs from ten to fifteen all outputs are logical "1".

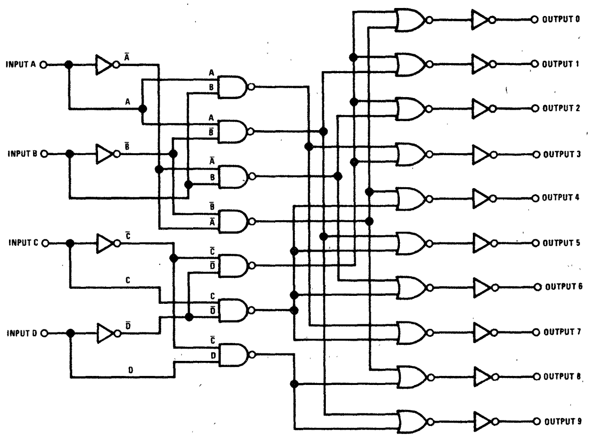
features

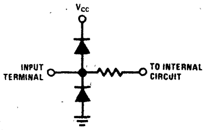
■ Supply voltage range	3V to 15V
■ Tenth power TTL compatible	drive 2 LPTTL loads
■ High noise immunity	0.45 V_{CC} (typ.)
■ Low power	50 nW (typ.)
■ Medium speed operation	10 MHz (typ.) with 10V V_{CC}

applications

- Automotive
- Data terminals
- Instrumentation
- Medical electronics
- Alarm systems
- Industrial electronics
- Remote metering
- Computers

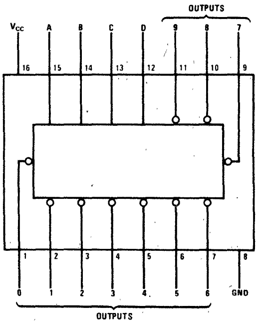
schematic diagram





INPUT PROTECTION FOR ALL INPUTS

connection diagram



TOP VIEW

truth table

INPUTS				OUTPUTS									
D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	0	0	0	0	1	1	1	1	1	1	1	1	1
0	0	0	1	1	0	1	1	1	1	1	1	1	1
0	0	1	0	1	1	0	1	1	1	1	1	1	1
0	0	1	1	1	1	1	0	1	1	1	1	1	1
0	1	0	0	1	1	1	1	0	1	1	1	1	1
0	1	0	1	1	1	1	1	1	0	1	1	1	1
0	1	1	0	1	1	1	1	1	1	0	1	1	1
0	1	1	1	1	1	1	1	1	1	1	0	1	1
1	0	0	0	1	1	1	1	1	1	1	1	0	1
1	0	0	1	1	1	1	1	1	1	1	1	1	0
1	0	1	0	1	1	1	1	1	1	1	1	1	1
1	0	1	1	1	1	1	1	1	1	1	1	1	1
1	1	0	0	1	1	1	1	1	1	1	1	1	1
1	1	0	1	1	1	1	1	1	1	1	1	1	1
1	1	1	0	1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1	1	1	1	1

absolute maximum ratings

Voltage at Any Pin (Note 1)	$-0.3V$ to V_{CC} $+0.3V$	Storage Temperature	$-65^{\circ}C$ to $+150^{\circ}C$
Operating Temperature MM54C42	$-55^{\circ}C$ to $+125^{\circ}C$	Package Dissipation	500 mW
MM74C42	$-40^{\circ}C$ to $+85^{\circ}C$	Operating V_{CC} Range	3V to 15V
Maximum V_{CC} Voltage	16V	Lead Temperature (Soldering, 10 sec)	$300^{\circ}C$

electrical characteristics

Min/Max limits apply across temperature range unless otherwise specified

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
CMOS TO CMOS						
Logical "1" Input Voltage	$V_{IN(1)}$	$V_{CC} = 5.0V$	3.5			V
		$V_{CC} = 10.0V$	8			V
Logical "0" Input Voltage	$V_{IN(0)}$	$V_{CC} = 5.0V$			1.5	V
		$V_{CC} = 10.0V$			2	V
Logical "1" Output Voltage	$V_{OUT(1)}$	$V_{CC} = 5.0V$, $I_O = -10\,\mu A$	4.5			V
		$V_{CC} = 10.0V$, $I_O = -10\,\mu A$	9.0			V
Logical "0" Output Voltage	$V_{OUT(0)}$	$V_{CC} = 5.0V$, $I_O = +10\,\mu A$			0.5	V
		$V_{CC} = 10.0V$, $I_O = +10\,\mu A$			1	V
Logical "1" Input Current	$I_{IN(1)}$	$V_{CC} = 15.0V$, $V_{IN} = 15V$			1	μA
Logical "0" Input Current	$I_{IN(0)}$	$V_{CC} = 15.0V$, $V_{IN} = 0V$	-1			μA
Supply Current	I_{CC}	$V_{CC} = 15.0V$		0.05	300	μA
Input Capacitance		Any Input		5		pF
Propogation Delay Time to a Logical "0" or Logical "1"		$V_{CC} = 5.0V$, $C_L = 50$ pF, $T_A = 25^{\circ}C$		200	300	ns
		$V_{CC} = 10.0V$, $C_L = 50$ pF, $T_A = 25^{\circ}C$		90	140	ns
CMOS TO TENTH POWER INTERFACE						
Logical "1" Input Voltage	$V_{IN(1)}$	54C, $V_{CC} = 4.5V$	$V_{CC} - 1.5$			V
		74C, $V_{CC} = 4.75V$				
Logical "0" Input Voltage	$V_{IN(0)}$	54C, $V_{CC} = 4.5V$			0.8	V
		74C, $V_{CC} = 4.75V$				
Logical "1" Output Voltage	$V_{OUT(1)}$	54C, $V_{CC} = 4.5V$, $I_O = -360\,\mu A$	2.4			V
		74C, $V_{CC} = 4.75V$, $I_O = -360\,\mu A$				
Logical "0" Output Voltage	$V_{OUT(0)}$	54C, $V_{CC} = 4.5V$, $I_O = 360\,\mu A$			0.4	V
		74C, $V_{CC} = 4.75V$, $I_O = 360\,\mu A$				
Propagation Delay Time to a Logical "0" or Logical "1"		$V_{CC} = 5.0V$, $C_L = 50$ pF, $T_A = 25^{\circ}C$		250	400	ns

Note 1: This device should not be connected to circuits with the power on because high transient voltages may cause permanent damage.

MM54C48/MM74C48 BCD-to-7 segment decoder

general description

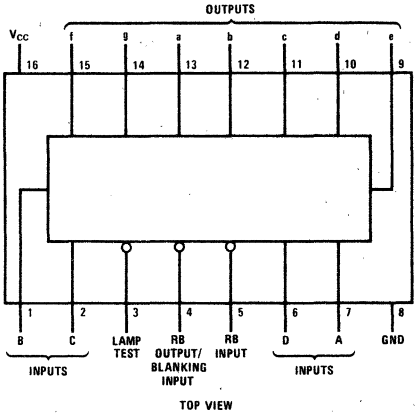
The MM54C48/MM74C48 BCD-to-7 segment decoder is a monolithic complementary MOS (CMOS) integrated circuit constructed with N- and P-channel enhancement transistors. Seven NAND gates and one driver are connected in pairs to make binary-coded decimal (BCD) data and its complement available to the seven decoding AND-OR-INVERT gates. The remaining NAND gate and three input buffers provide test blanking input/ripple-blanking output, and ripple-blanking inputs.

features

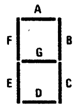
- Wide supply voltage range 3.0V to 15V
- Guaranteed noise margin 1.0V
- High noise immunity 0.45 V_{CC} typ
- Low power TTL compatibility fan out of 2 driving 74L
- High current sourcing output (up to 50 mA)
- Ripple blanking for leading or trailing zeros (optional)
- Lamp test provision

---

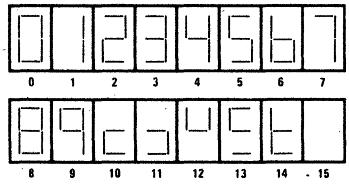
connection diagram



TOP VIEW



Segment Identification



Numerical Designations and Resultant Displays

absolute maximum ratings (Note 1)

Voltage at Any Pin	$-0.3V$ to $V_{CC} + 0.3V$
Operating Temperature Range	
MM54C48	−55°C to +125°C
MM74C48	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500 mW
Operating V_{CC} Range	3.0V to 15V
Absolute Maximum V_{CC}	16V
Lead Temperature (Soldering, 10 seconds)	300°C

dc electrical characteristics

Min/max limits apply across temperature range, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CMOS TO CMOS					
Logical "1" Input Voltage ($V_{IN(1)}$)	$V_{CC} = 5.0V$	3.5			V
	$V_{CC} = 10V$	8.0			V
Logical "0" Input Voltage ($V_{IN(0)}$)	$V_{CC} = 5.0V$			1.5	V
	$V_{CC} = 10V$			2.0	V
Logical "1" Output Voltage ($V_{OUT(1)}$)	$V_{CC} = 5.0V$, $I_O = -10\mu A$	4.5			V
(RB Output Only)	$V_{CC} = 10V$, $I_O = -10\mu A$	9.0			V
Logical "0" Output Voltage ($V_{OUT(0)}$)	$V_{CC} = 5.0V$, $I_O = +10\mu A$			0.5	V
	$V_{CC} = 10V$, $I_O = +10\mu A$			1.0	V
Logical "1" Input Current ($I_{IN(1)}$)	$V_{CC} = 15V$, $V_{IN} = 15V$		0.005	1.0	µA
Logical "0" Input Current ($I_{IN(0)}$)	$V_{CC} = 15V$, $V_{IN} = 0V$	−1.0	−0.005		µA
Supply Current (I_{CC})	$V_{CC} = 15V$		0.05	300	µA
CMOS/LPTTL INTERFACE					
Logical "1" Input Voltage ($V_{IN(1)}$)	54C, $V_{CC} = 4.5V$	$V_{CC}-1.5$			V
	74C, $V_{CC} = 4.75V$	$V_{CC}-1.5$			V
Logical "0" Input Voltage ($V_{IN(0)}$)	54C, $V_{CC} = 4.5V$			0.8	V
	74C, $V_{CC} = 4.75V$			0.8	V
Logical "1" Output Voltage ($V_{OUT(1)}$)	54C, $V_{CC} = 4.5V$, $I_O = -50\mu A$	2.4			V
(RB Output Only)	74C, $V_{CC} = 4.75V$, $I_O = -50\mu A$	2.4			V
Logical "0" Output Voltage ($V_{OUT(0)}$)	54C, $V_{CC} = 4.5V$, $I_O = 360\mu A$			0.4	V
	74C, $V_{CC} = 4.75V$, $I_O = 360\mu A$			0.4	V
OUTPUT DRIVE (See 54C/74C Family Characteristics Data Sheet)					
Output Source Current (I_{SOURCE}) (P-Channel) (RB Output Only)	$V_{CC} = 4.75V$, $V_{OUT} = 0.4V$			−0.80	mA
Output Sink Current (I_{SINK}) (N-Channel)	$V_{CC} = 5.0V$, $V_{OUT} = V_{CC}$ $T_A = 25°C$	1.75	3.6		mA
Output Sink Current (I_{SINK}) (N-Channel)	$V_{CC} = 10V$, $V_{OUT} = V_{CC}$ $T_A = 25°C$	8.0	16		mA
Output Source Current	$V_{CC} = 5.0V$, $V_{OUT} = 3.4$	20		50	mA
(NPN Bipolar)	$V_{CC} = 5.0V$, $V_{OUT} = 3.0$			65	mA
	$V_{CC} = 10V$, $V_{OUT} = 8.4$	20		50	mA
	$V_{CC} = 10V$, $V_{OUT} = 8.0$			65	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

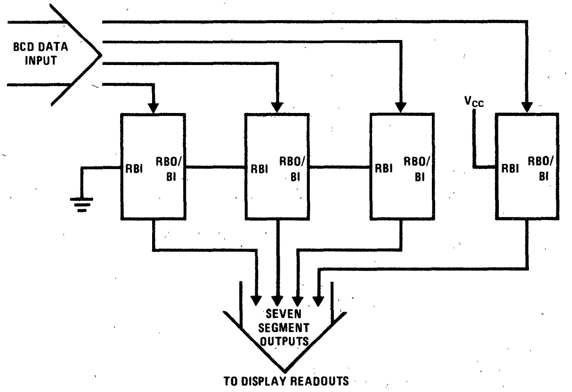
Note 3: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note, AN-90.

ac electrical characteristics $T_A = 25°C, C_L = 50\ pF$, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Propagation Delay to a "1" or "0" on Segment Outputs from Data Inputs	$V_{CC} = 5.0V$ $V_{CC} = 10V$		450 160	1500 500	ns ns
Propagation Delay to a "0" on Segment Outputs from RB Input	$V_{CC} = 5.0V$ $V_{CC} = 10V$		500 180	1600 550	ns ns
Propagation Delay to a "0" on Segment Outputs from Blanking Input	$V_{CC} = 5.0V$ $V_{CC} = 10V$		350 140	1200 450	ns ns
Propagation Delay to a "1" on Segment Outputs from Lamp Test	$V_{CC} = 5.0V$ $V_{CC} = 10V$		450 160	1500 500	ns ns
Propagation Delay to a "1" on RB Output from RB Input	$V_{CC} = 5.0V$ $V_{CC} = 10V$		600 250	2000 800	ns ns
Propagation Delay to a "0" on RB Output from RB Input	$V_{CC} = 5.0V$ $V_{CC} = 10V$		140 50	450 150	ns ns

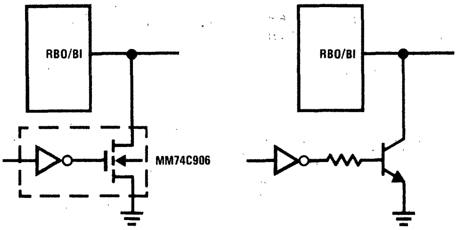
typical applications

Typical Connection Utilizing the Ripple-Blanking Feature



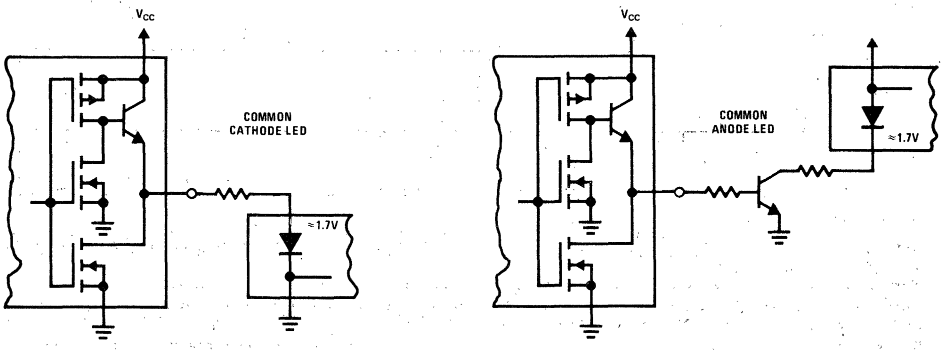
(First three stages will blank leading zeros, the fourth stage will not blank zeros)

Blanking Input Connection Diagram



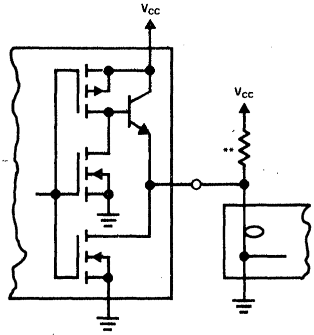
(When RBO/BI is forced low, all segment outputs are off regardless of the state of any other input condition)

Light Emitting Diode (LED) Readout



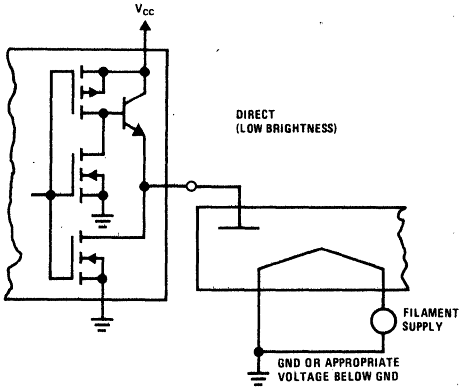
typical applications (con't)

Incandescent Readout

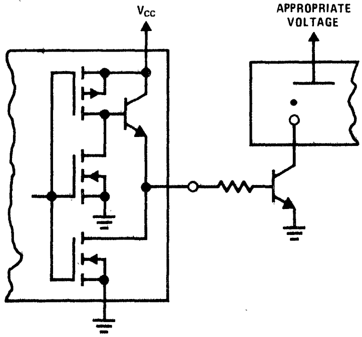


**A filament pre-warm resistor is recommended to reduce filament thermal shock and increase the effective cold resistance of the filament.

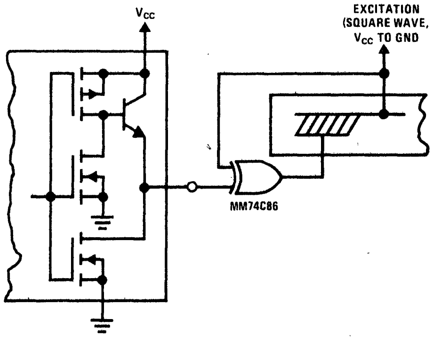
Fluorescent Readout



Gas Discharge Readout



Liquid Crystal (LC) Readout



Direct dc drive of LC's not recommended for life of LC readouts.

truth table

DECIMAL OR FUNCTION	INPUTS						BI/RBO†	OUTPUTS							NOTE
	LT	RBI	D	C	B	A		a	b	c	d	e	f	g	
0	H	H	L	L	L	L	H	H	H	H	H	H	H	L	1
1	H	X	L	L	L	H	H	L	H	H	L	L	L	L	1
2	H	X	L	L	H	L	H	H	H	L	H	H	L	H	
3	H	X	L	L	H	H	H	H	H	H	H	L	L	H	
4	H	X	L	H	L	L	H	L	H	H	L	L	H	H	
5	H	X	L	H	L	H	H	H	L	H	H	L	H	H	
6	H	X	L	H	H	L	H	L	L	H	H	H	H	H	
7	H	X	L	H	H	H	H	H	H	H	L	L	L	L	
8	H	X	H	L	L	L	H	H	H	H	H	H	H	H	
9	H	X	H	L	L	H	H	H	H	H	L	L	H	H	
10	H	X	H	L	H	L	H	L	L	L	H	H	L	H	
11	H	X	H	L	H	H	H	L	L	H	H	L	L	H	
12	H	X	H	H	L	L	H	L	H	L	L	L	H	H	
13	H	X	H	H	L	H	H	H	L	L	H	L	H	H	
14	H	X	H	H	H	L	H	L	L	L	H	H	H	H	
15	H	X	H	H	H	H	H	L	L	L	L	L	L	L	
BI	X	X	X	X	X	X	L	L	L	L	L	L	L	L	2
RBI	H	L	L	L	L	L	L	L	L	L	L	L	L	L	3
LT	L	X	X	X	X	X	H	H	H	H	H	H	H	H	4

H = high level, L = low level, X = irrelevant

Note 1: The blanking input (BI) must be open when output functions 0–15 are desired. The ripple-blanking input (RBI) must be high, if blanking of a decimal zero is not desired.

Note 2: When a low logic level is applied directly to the blanking input (BI), all segment outputs are low regardless of the level of any other input.

Note 3: When ripple-blanking input (RBI) and inputs A, B, C, and D are at a low level with the lamp-test input high, all segment outputs go low and the ripple-blanking output (RBO) goes to a low level (response condition).

Note 4: When the blanking input/ripple-blanking output (BI/RBO) is open and a low is applied to the lamp-test input, all segment outputs are high.

† One BI/RBO is wire-AND logic serving as blanking input (BI) and/or ripple-blanking output (RBO).

MM54C73/MM74C73 dual J-K flip-flops with clear
MM54C76/MM74C76 dual J-K flip-flops with clear and preset
MM54C107/MM74C107 dual J-K flip-flops with clear

general description

These dual J-K flip-flops are monolithic complementary MOS (CMOS) integrated circuits constructed with N- and P-channel enhancement transistors. Each flip-flop has independent J, K, clock and clear inputs and Q and $\overline{Q}$ outputs. The MM54C76/MM74C76 flip flops also include preset inputs and are supplied in 16 pin packages. These flip flops are edge sensitive to the clock input and change state on the negative going transition of the clock pulses. Clear or preset is independent of the clock and is accomplished by a low level on the respective input.

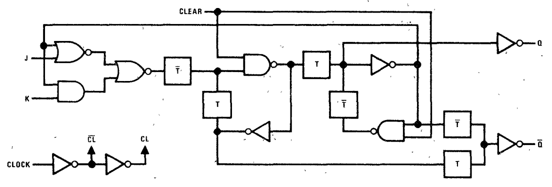
features

■ Supply voltage range	3V to 15V
■ Tenth power TTL compatible	drive 2 LPTTL loads
■ High noise immunity	0.45 V_{CC} (typ)
■ Low power	50 nW (typ)
■ Medium speed operation	10 MHz (typ) with 10V supply

applications

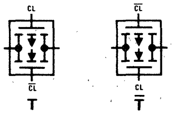
- Automotive
- Data terminals
- Instrumentation
- Medical electronics
- Alarm systems
- Industrial electronics
- Remote metering
- Computers

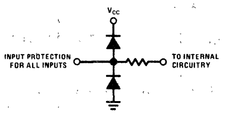
logic and connection diagrams

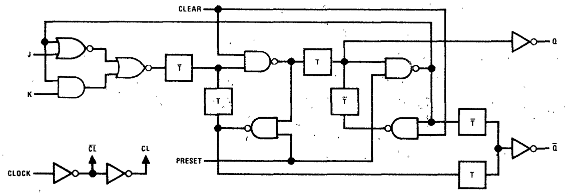


MM54C73/MM74C73 and MM54C107/MM74C107

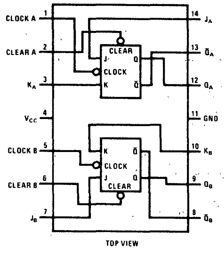
Transmission Gate





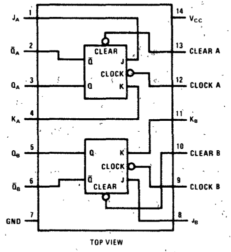


MM54C76/MM74C76



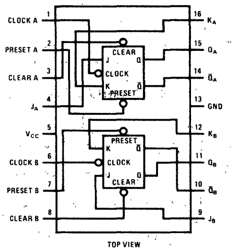
Note: A logic "0" on clear sets Q to logic "0."

MM54C73/MM74C73



Note: A logic "0" on clear sets Q to logic "0."

MM54C107/MM74C107



Note 1: A logic "0" on clear sets Q to a logic "0."
Note 2: A logic "0" on preset sets Q to a logic "1."

MM54C76/MM74C76

absolute maximum ratings

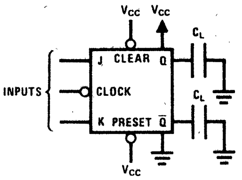
Voltage at any pin (Note 1)	$-0.3V$ to V_{CC} $+0.3V$
Operating Temperature MM54CXX	−55°C to 125°C
MM74CXX	−40°C to +85°C
Storage Temperature	−65°C to 150°C
Maximum V_{CC} Voltage	16V
Package Dissipation	500 mW
Lead Temperature (Soldering, 10 sec)	300°C
Operating V_{CC} Range	+3V to 15V

electrical characteristics

PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNITS
CMOS TO CMOS					
Logical "1" Input Voltage $V_{IN(1)}$	V_{CC} = 5.0V V_{CC} = 10.0V	3.5 8			V V
Logical "0" Input Voltage $V_{IN(0)}$	V_{CC} = 5.0V V_{CC} = 10.0V			1.5 2.0	V V
Logical "1" Output Voltage $V_{OUT(1)}$	V_{CC} = 5.0V V_{CC} = 10.0V	4.5 9.0			V V
Logical "0" Output Voltage $V_{OUT(0)}$	V_{CC} = 5.0V V_{CC} = 10.0V			0.5 1.0	V V
Logical "1" Input Current $I_{IN(1)}$	V_{CC} = 15.0V			1.0	μA
Logical "0" Input Current $I_{IN(0)}$	V_{CC} = 15.0V	−1.0			μA
Supply Current I_{CC}	V_{CC} = 15.0V		0.050	60	μA
Input Capacitance	Any Input		5		pF
Propagation Delay Time to a Logical "0" t_{pd0} or Logical "1" t_{pd1} From Clock to Q or $\overline{Q}$	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C V_{CC} = 10.0V, C_L = 50 pF, T_A = 25°C		180 70	300 110	ns ns
Propagation Delay Time to a Logical "0" From Preset or Clear	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C V_{CC} = 10.0V, C_L = 50 pF, T_A = 25°C		200 80	300 130	ns ns
Propagation Delay Time to a Logical "1" From Preset or Clear	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C V_{CC} = 10.V, C_L = 50 pF, T_A = 25°C		200 80	300 130	ns ns
Time Prior to Clock Pulse That Data Must be Present, t_{SETUP}	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C V_{CC} = 10V, C_L = 50 pF, T_A = 25°C		110 45	175 70	ns ns
Time After Clock Pulse That J and K Must be Held	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C V_{CC} = 10.0V, C_L = 50 pF, T_A = 25°C		−40 −20	0 0	ns ns
Minimum Clock Pulse Width $t_{WL} = t_{WH}$	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C V_{CC} = 10.0V, C_L = 50 pF, T_A = 25°C		120 50	190 80	ns ns
Minimum Preset and Clear Pulse Width	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C V_{CC} = 10.0V, C_L = 50 pF, T_A = 25°C		90 40	130 60	ns ns
Maximum Toggle Frequency	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C V_{CC} = 10.0V, C_L = 50 pF, T_A = 25°C	2.5 7.0	4.0 11.0		MHz MHz
Clock Pulse Rise and Fall Time	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C V_{CC} = 10.0V, C_L = 50 pF, T_A = 25°C			15 5	μs μs
LOW POWER TTL TO CMOS INTERFACE					
Logical "1" Input Voltage $V_{IN(1)}$	54C, V_{CC} = 4.5V 74C, V_{CC} = 4.75V	V_{CC}−1.5			V
Logical "0" Input Votlage $V_{IN(0)}$	54C, V_{CC} = 4.5V 74C, V_{CC} = 4.75V			0.8	V
Logical "1" Output Voltage $V_{OUT(1)}$	54C, V_{CC} = 4.5V, I_0 = −360μA 74C, V_{CC} = 4.75V, I_0 = −360μA	2.4			V
Logical "0" Output Voltage $V_{OUT(0)}$	54C, V_{CC} = 4.5V, I_0 = 360μA 74C, V_{CC} = 4.75V, I_0 = 360μA			0.4	V

Note 1: This device should not be connected to circuits with the power on because high transient voltages may cause permanent damage.

ac test circuit



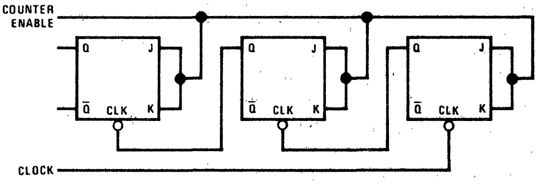
truth table

t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q}_n$

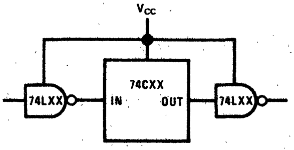
t_n = bit time before clock pulse.
t_{n+1} = bit time after clock pulse.

typical applications

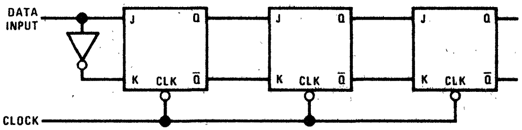
Ripple Binary Counters



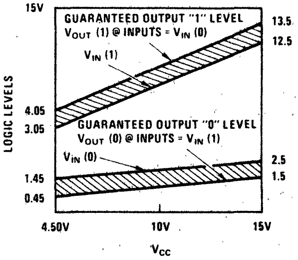
74C Compatibility



Shift Registers

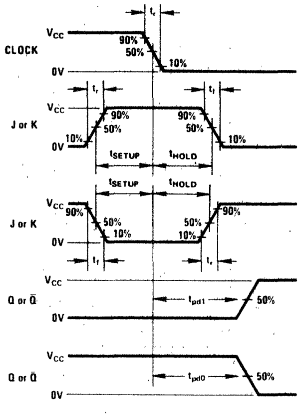


Guaranteed Noise Margin as a Function of V_{CC}



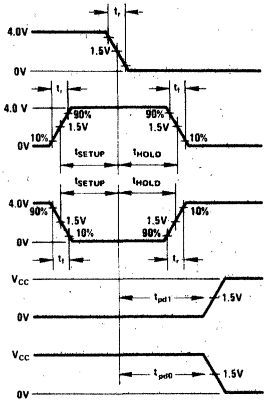
switching time waveforms

CMOS to CMOS



$t_r = t_f = 20$ ns

TTL to CMOS



MM54C74/MM74C74 dual D flip-flop

general description

The MM54C74/MM74C74 dual D flip flop is a monolithic complementary MOS (CMOS) integrated circuit constructed with N- and P-channel enhancement transistors. Each flip flop has independent data, preset, clear and clock inputs and Q and $\overline{Q}$ outputs. The logic level present at the data input is transferred to the output during the positive going transition of the clock pulse. Preset or clear is independent of the clock and accomplished by a low level at the preset or clear input.

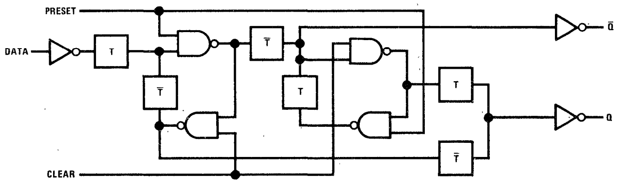
features

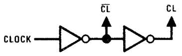
■ Supply voltage range	3V to 15V
■ Tenth power TTL compatible	drive $2LPT^2L$ loads
■ High noise immunity	0.45 V_{CC} (typ)
■ Low power	50 nW (typ)
■ Medium speed operation	10 MHz (typ) with 10V supply

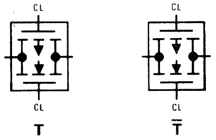
applications

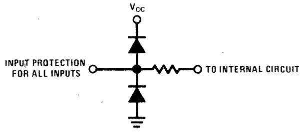
- Automotive
- Data terminals
- Instrumentation
- Medical electronics
- Alarm system
- Industrial electronics
- Remote metering
- Computers

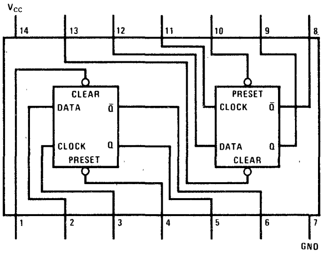
logic and connection diagrams











TOP VIEW

Note: A logic "0" on clear sets Q to logic "0."
A logic "0" on preset sets Q to logic "1."

absolute maximum ratings

Voltage at any pin (Note 1)	−0.3V to V_{CC} + 0.3V
Operating temperature MM54C74	−55°C to 125°C
MM74C74	−40°C to +85°C
Storage temperature	−65°C to 150°C
Maximum V_{CC} Voltage	16V
Package dissipation	500 mW
Lead temperature (Soldering, 10 sec)	300°C
Operating V_{CC} range	+3V to +15V

electrical characteristics

Min/Max limits apply across temperature range unless otherwise specified.

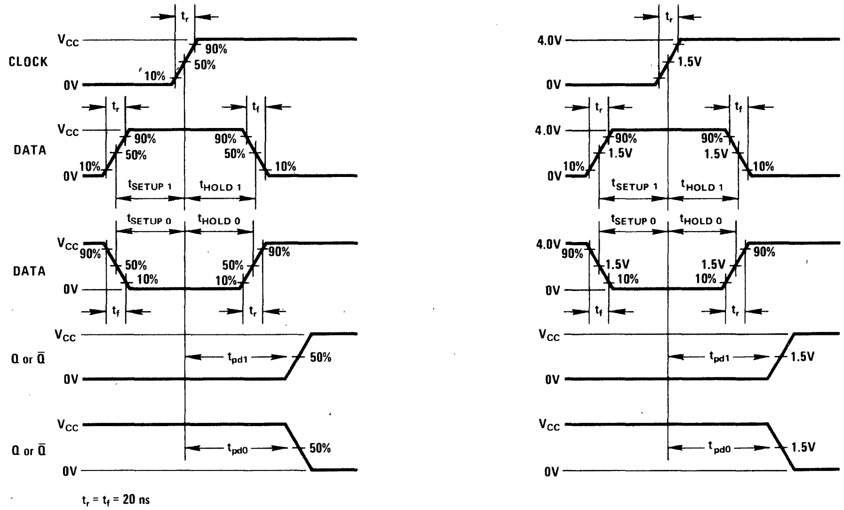
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CMOS TO CMOS					
Logical "1" Input Voltage $V_{IN(1)}$	V_{CC} = 5.0V	3.5			V
	V_{CC} = 10.0V	8.0			V
Logical "0" Input Voltage $V_{IN(0)}$	V_{CC} = 5.0V			1.5	V
	V_{CC} = 10.0V			2.0	V
Logical "1" Output Voltage $V_{OUT(1)}$	V_{CC} = 5.0V	4.5			V
	V_{CC} = 10.0V	9.0			V
Logical "0" Output Voltage $V_{OUT(0)}$	V_{CC} = 5.0V			0.5	V
	V_{CC} = 10.0V			1.0	V
Logical "1" Input Current $I_{IN(1)}$	V_{CC} = 15.0V			1.0	μA
Logical "0" Input Current $I_{IN(0)}$	V_{CC} = 15.0V	−1.0			μA
Supply Current I_{CC}	V_{CC} = 15.0V		0.05	60	μA
Input Capacitance	Any Input		5.0		pF
Propagation Delay Time to a Logical "0" t_{pd0} or Logical "1" t_{pd1} from clock to Q or $\overline{Q}$	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C		180	300	ns
	V_{CC} = 10.0V, C_L = 50 pF, T_A = 25°C		70	110	ns
Propagation Delay Time to a Logical "0" from Preset or Clear	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C		180	300	ns
	V_{CC} = 10.0V, C_L = 50 pF, T_A = 25°C		70	110	ns
Propagation Delay Time to a Logical "1" from Preset or Clear	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C		250	400	ns
	V_{CC} = 10.0V, C_L = 50 pF, T_A = 25°C		100	150	ns
Time Prior to Clock Pulse That Data Must be Present t_{SETUP}	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C	100	50		ns
	V_{CC} = 10.0V, C_L = 50 pF, T_A = 25°C	40	20		ns
Time After Clock Pulse That Data Must be Held	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C		−20	0	ns
	V_{CC} = 10.0V, C_L = 50 pF, T_A = 25°C		−8.0	0	ns
Minimum Clock Pulse Width ($t_{WL} = t_{WH}$)	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C		100	250	ns
	V_{CC} = 10.0V, C_L = 50 pF, T_A = 25°C		40	100	ns
Minimum Preset and Clear Pulse Width	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C		100	160	ns
	V_{CC} = 10.0V, C_L = 50 pF, T_A = 25°C		40	70	ns
Maximum Clock Rise and Fall Time	V_{CC} = 5.0V, C_L = 50 pF	15.0			μs
	V_{CC} = 10.0V, C_L = 50 pF	5.0			μs
Maximum Clock Frequency	V_{CC} = 5.0 V, C_L = 50 pF, T_A = 25°C	2.0	3.5		MHz
	V_{CC} = 10.0V, C_L = 50 pF, T_A = 25°C	5.0	8.0		MHz
LOW POWER TTL/CMOS INTERFACE					
Logical "1" Input Voltage $V_{IN(1)}$	54C, V_{CC} = 4.5V	V_{CC} − 1.5			
	74C, V_{CC} = 4.75V				
Logical "0" Input Voltage $V_{IN(0)}$	54C, V_{CC} = 4.75V			0.8	V
	74C, V_{CC} = 4.75V				
Logical "1" Output Voltage $V_{OUT(1)}$	54C, V_{CC} = 4.5V, I_D = − 360 μA	2.4			V
	74C, V_{CC} = 4.75V, I_D = − 360 μA				
Logical "0" Output Voltage $V_{OUT(0)}$	54C, V_{CC} = 4.50V, I_D = 360 μA			0.4	V
	74C, V_{CC} = 4.75V, I_D = 360 μA				

Note 1: These devices should not be connected under power on conditions.

switching time waveforms

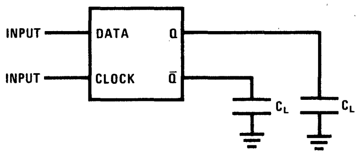
CMOS to CMOS

TTL to CMOS



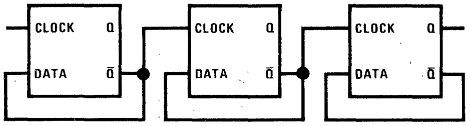
$t_r = t_f = 20$ ns

ac test circuit

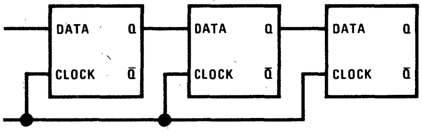


typical applications

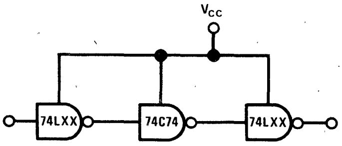
Ripple Counter (Divide by 2^n)



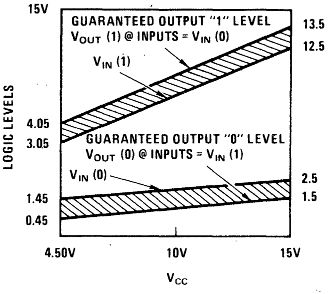
Shift Register



74C Compatibility



Guaranteed Noise Margin as a Function of V_{CC}



MM54C83/MM74C83 4-bit binary full adder

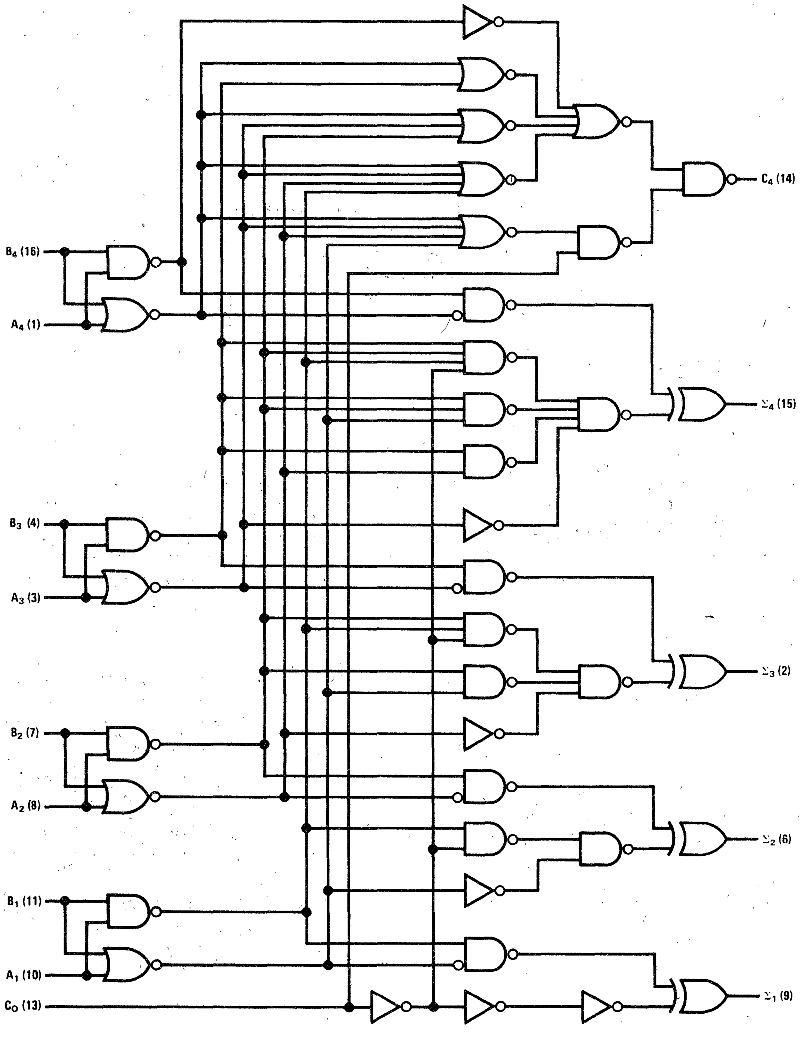
general description

The MM54C83/MM74C83 4-bit binary full adder performs the addition of two 4-bit binary numbers. A carry input (C_0) is included and the sum (Σ) outputs are provided for each bit and the resultant carry (C_4) is obtained from the fourth bit. Since the carry-ripple-time is the limiting delay in the addition of a long word length, carry look-ahead circuitry has been included in the design to minimize this delay. Also, the logic levels of the input and output, including the carry, are in their true form. Thus the end-around carry is accomplished without the need for level inverison.

features

- Wide supply voltage range 3V to 15V
- Guaranteed noise margin 1V
- High noise immunity 0.45 V_{CC} typ
- Low power TTL compatibility fan out of 2 driving 74L
- Fast carry ripple (C_0 to C_4) 50 ns typ @ V_{CC} = 10V and C_L = 50 pF
- Fast summing (Σ_{IN} to Σ_{OUT}) 125 ns typ @ V_{CC} = 10V and C_L = 50 pF

logic diagram



absolute maximum ratings (Note 1)

Voltage at Any Pin	−0.3V to V_{CC} + 0.3V
Operating Temperature Range	
MM54C83	−55°C to +125°C
MM74C83	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500 mW
Operating V_{CC} Range	3V to 15V
Absolute Maximum V_{CC}	16V
Lead Temperature (Soldering, 10 seconds)	300°C

dc electrical characteristics

Min/max limits apply across temperature range, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CMOS TO CMOS					
Logical "1" Input Voltage ($V_{IN(1)}$)	V_{CC} = 5.0V V_{CC} = 10V	3.5 8.0			V V
Logical "0" Input Voltage ($V_{IN(0)}$)	V_{CC} = 5.0V V_{CC} = 10V			1.5 2.0	V V
Logical "1" Output Voltage ($V_{OUT(1)}$)	V_{CC} = 5.0V, I_O = −10µA V_{CC} = 10V, I_O = −10µA	4.5 9.0			V V
Logical "0" Output Voltage ($V_{OUT(0)}$)	V_{CC} = 5.0V, I_O = +10µA V_{CC} = 10V, I_O = +10µA			0.5 1.0	V V
Logical "1" Input Current ($I_{IN(1)}$)	V_{CC} = 15V, V_{IN} = 15V		0.005	1.0	µA
Logical "0" Input Current ($I_{IN(0)}$)	V_{CC} = 15V, V_{IN} = 0V	−1.0	−0.005		µA
Supply Current (I_{CC})	V_{CC} = 15V		0.05	300	µA
CMOS/LPTTL INTERFACE					
Logical "1" Input Voltage ($V_{IN(1)}$)	54C, V_{CC} = 4.5V 74C, V_{CC} = 4.75V	V_{CC} − 1.5 V_{CC} − 1.5			V V
Logical "0" Input Voltage ($V_{IN(0)}$)	54C, V_{CC} = 4.5V 74C, V_{CC} = 4.75V			0.8 0.8	V V
Logical "1" Output Voltage ($V_{OUT(1)}$)	54C, V_{CC} = 4.5V, I_O = −360µA 74C, V_{CC} = 4.75V, I_O = −360µA	2.4 2.4			V V
Logical "0" Output Voltage ($V_{OUT(0)}$)	54C, V_{CC} = 4.5V, I_O = 360µA 74C, V_{CC} = 4.75V, I_O = 360µA			0.4 0.4	V V
OUTPUT DRIVE (See 54C/74C Family Characteristics Data Sheet)					
Output Source Current (I_{SOURCE}) (P-Channel)	V_{CC} = 5.0V, V_{OUT} = 0V T_A = 25°C	−1.75	−3.3		mA
Output Source Current (I_{SOURCE}) (P-Channel)	V_{CC} = 10V, V_{OUT} = 0V T_A = 25°C	−8.0	−15		mA
Output Sink Current (I_{SINK}) (N-Channel)	V_{CC} = 5.0V, V_{OUT} = V_{CC} T_A = 25°C	1.75	3.6		mA
Output Sink Current (I_{SINK}) (N-Channel)	V_{CC} = 10V, V_{OUT} = V_{CC} T_A = 25°C	8.0	16		mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

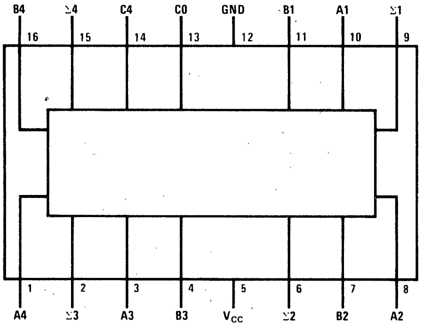
Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note, AN-90.

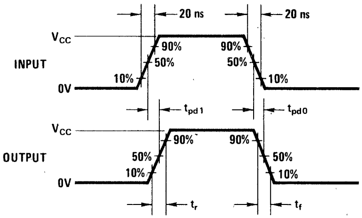
ac electrical characteristics $T_A = 25°C$, $C_L = 50$ pF, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Propagation Delay from C_0 to C_4 (t_{PD0} or t_{PD1})	$V_{CC} = 5.0V$		120	200	ns
	$V_{CC} = 10V$		50	80	ns
Propagation Delay from Sum Inputs to C_4 (t_{PD0} or t_{PD1})	$V_{CC} = 5.0V$		250	450	ns
	$V_{CC} = 10V$		90	150	ns
Propagation Delay from C_0 to Sum Outputs (t_{PD0} or t_{PD1})	$V_{CC} = 5.0V$		350	550	ns
	$V_{CC} = 10V$		125	200	ns
Propagation Delay from Sum Inputs to Sum Outputs (t_{PD0} or t_{PD1})	$V_{CC} = 5.0V$		300	550	ns
	$V_{CC} = 10V$		110	180	ns
Input Capacitance	Any Input (Note 2)		5.0		pF
Power Dissipation Capacitance (C_{PD})	Per Package (Note 3)		120		pF

connection diagram



switching time waveforms



Inputs must be tied to appropriate logic level.

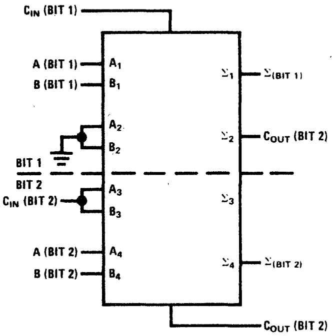
truth table

INPUT				OUTPUT					
				WHEN C0 = L WHEN C2 = L			WHEN C0 = H WHEN C2 = H		
A1 A3	B1 B3	A2 A4	B2 B4	Σ1 Σ3	Σ2 Σ4	C2 C4	Σ1 Σ3	Σ2 Σ4	C2 C4
L	L	L	L	L	L	L	H	L	L
H	L	L	L	H	L	L	L	H	L
L	H	L	L	H	L	L	L	H	L
H	H	L	L	L	H	L	H	H	L
L	L	H	L	L	H	L	H	H	L
H	L	H	L	H	H	L	L	L	H
L	H	H	L	H	H	L	L	L	H
H	H	H	L	L	L	H	H	L	H
L	L	L	H	L	H	L	H	H	L
H	L	L	H	H	H	L	L	L	H
L	H	L	H	H	H	L	L	L	H
H	H	L	H	L	L	H	H	L	H
L	L	H	H	L	L	H	H	L	H
H	L	H	H	H	L	H	L	H	H
L	H	H	H	H	L	H	L	H	H
H	H	H	L	H	H	H	H	H	H

H = high level, L = low level

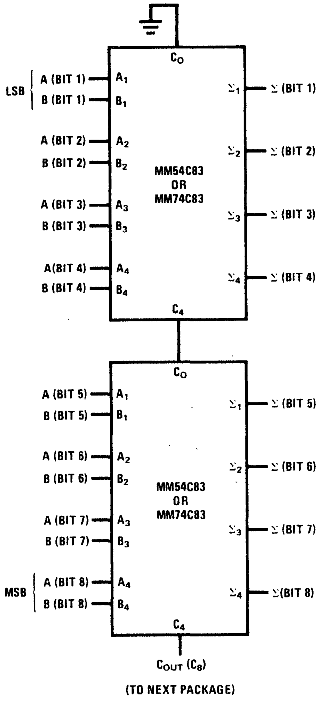
Note: Input conditions at A3, A2, B2 and C0 are used to determine outputs Σ1 and Σ2 and the value of the internal carry C2. The values at C2, A3, B3, A4, and B4 are then used to determine outputs Σ3, Σ4, and C4.

typical applications



APPLICATION

Connect the MM54C83/MM74C83 in the following manner to implement a dual single bit full adder.



CASCADING

Connect the MM54C83/MM74C83 in the following manner to implement full adders with more than 4 bits.

MM54C85/MM74C85 4-bit magnitude comparator

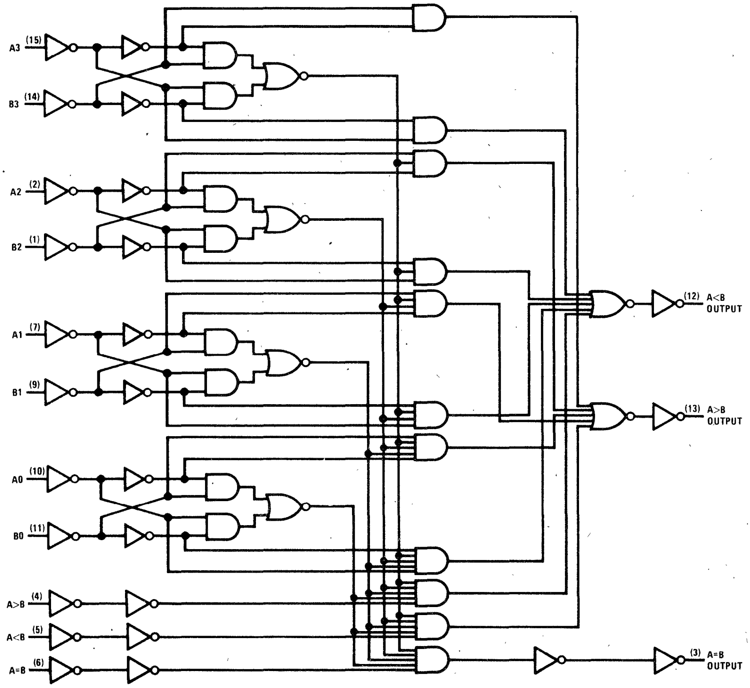
general description

The MM54C85/MM74C85 is a four-bit magnitude comparator which will perform comparison of straight binary or BCD codes. The circuit consists of eight comparing inputs (A0, A1, A2, A3, B0, B1, B2, B3), three cascading inputs (A>B, A<B and A=B), and three outputs (A>B, A<B and A=B). This device compares two four-bit words (A and B) and determines whether they are "greater than," "less than," or "equal to" each other by a high level on the appropriate output. For words greater than four-bits, units can be cascaded by connecting the outputs (A>B, A<B, and A=B) of the least-significant stage to the cascade inputs (A>B, A<B and A=B) of the next-significant stage. In addition the least significant stage must have a high level voltage ($V_{IN(1)}$) applied to the A=B input and low level voltages ($V_{IN(0)}$) applied to A>B and A<B inputs.

features

■ Wide supply voltage range	3.0V to 15V
■ Guaranteed noise margin	1.0V
■ High noise immunity	0.45 V_{CC} typ
■ Low power TTL compatibility	fan out of 2 driving 74L
■ Expandable to 'N' stages	
■ Applicable to binary or BCD	

logic diagram



absolute maximum ratings (Note 1)

Voltage at Any Pin	−0.3V to V_{CC} +0.3V
Operating Temperature Range	
MM54C85	−55°C to +125°C
MM74C85	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500 mW
Operating V_{CC} Range	3.0V to 15V
V_{CC}	16V
Lead Temperature (Soldering, 10 seconds)	300°C

dc electrical characteristics

Min/max limits apply across temperature range, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CMOS TO CMOS					
Logical "1" Input Voltage ($V_{IN(1)}$)	V_{CC} = 5.0V V_{CC} = 10V	3.5 8.0			V V
Logical "0" Input Voltage ($V_{IN(0)}$)	V_{CC} = 5.0V V_{CC} = 10V			1.5 2.0	V V
Logical "1" Output Voltage ($V_{OUT(1)}$)	V_{CC} = 5.0V, I_O = 10µA V_{CC} = 10V, I_O = −10µA	4.5 9.0			V V
Logical "0" Output Voltage ($V_{OUT(0)}$)	V_{CC} = 5.0V, I_O = +10µA V_{CC} = 10V, I_O = +10µA			0.5 1.0	V V
Logical "1" Input Current ($I_{IN(1)}$)	V_{CC} = 15V, V_{IN} = 15V		0.005	1.0	µA
Logical "0" Input Current ($I_{IN(0)}$)	V_{CC} = 15V, V_{IN} = 0V	−1.0	−0.005		µA
Supply Current (I_{CC})	V_{CC} = 15V		0.05	300	µA
CMOS/LPTTL INTERFACE					
Logical "1" Input Voltage ($V_{IN(1)}$)	54C, V_{CC} = 4.5V 74C, V_{CC} = 4.75V	$V_{CC} - 1.5$ $V_{CC} - 1.5$			V V
Logical "0" Input Voltage ($V_{IN(0)}$)	54C, V_{CC} = 4.5V 74C, V_{CC} = 4.75V			0.8 0.8	V V
Logical "1" Output Voltage ($V_{OUT(1)}$)	54C, V_{CC} = 4.5V, I_O = −360µA 74C, V_{CC} = 4.75V, I_O = −360µA	2.4 2.4			V V
Logical "0" Output Voltage ($V_{OUT(0)}$)	54C, V_{CC} = 4.5V, I_O = 360µA 74C, V_{CC} = 4.75V, I_O = 360µA			0.4 0.4	V V
OUTPUT DRIVE (See 54C/74C Family Characteristics Data Sheet)					
Output Source Current (I_{SOURCE}) (P-Channel)	V_{CC} = 5.0V, V_{OUT} = 0V T_A = 25°C	−1.75	−3.3		mA
Output Source Current (I_{SOURCE}) (P-Channel)	V_{CC} = 10V, V_{OUT} = 0V T_A = 25°C	−8.0	−15		mA
Output Sink Current (I_{SINK}) (N-Channel)	V_{CC} = 5.0V, V_{OUT} = V_{CC} T_A = 25°C	1.75	3.6		mA
Output Sink Current (I_{SINK}) (N-Channel)	V_{CC} = 10V, V_{OUT} = V_{CC} T_A = 25°C	8.0	16		mA

ac electrical characteristics T_A = 25°C, C_L = 50 pF, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Propagation Delay Time from any A or B Data Input to any Data Output (t_{pd0} or t_{pd1})	V_{CC} = 5.0V V_{CC} = 10V		250 100	600 300	ns ns
Propagation Delay Time from any Cascade Input to any Output (t_{pd0} or t_{pd1})	V_{CC} = 5.0V V_{CC} = 10V		200 100	500 250	ns ns
Input Capacitance	Any Input		5.0		pF
Power Dissipation Capacitance (C_{pd})	(Note 3) Per Package		45		pF

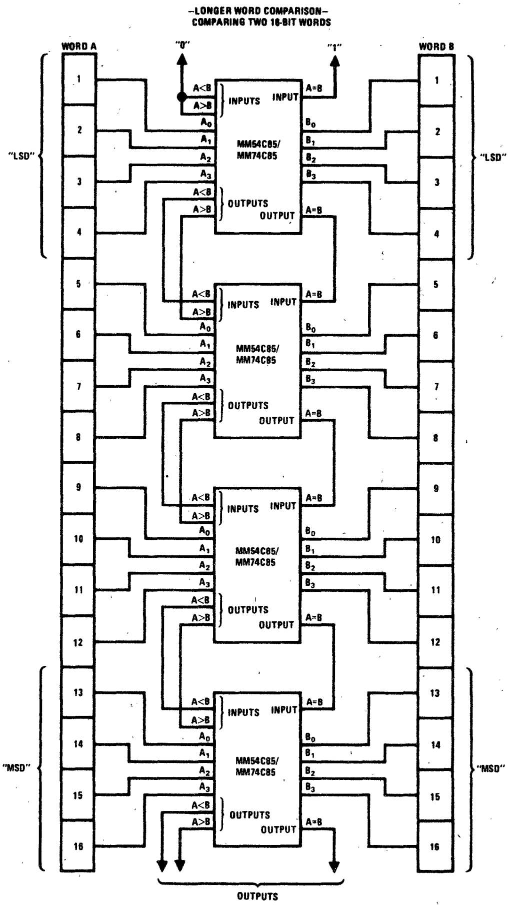
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

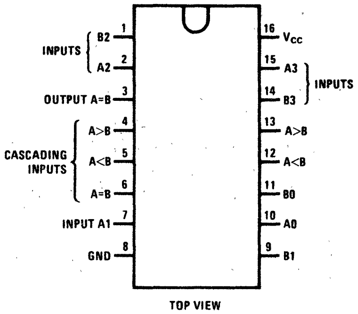
Note 3: C_{pd} determines the no load ac power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note, AN-90.

typical application

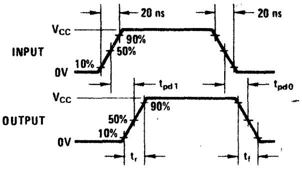
Four Digit Comparator



connection diagram



switching time waveform



Unused inputs must be tied to an appropriate logic level.

truth table

COMPARING INPUTS				CASCADING INPUTS			OUTPUTS		
A3, B3	A2, B2	A1, B1	A0, B0	A > B	A < B	A = B	A > B	A < B	A = B
A3 > B3	X	X	X	X	X	X	H	L	L
A3 < B3	X	X	X	X	X	X	L	H	L
A3 = B3	A2 > B2	X	X	X	X	X	H	L	L
A3 = B3	A2 < B2	X	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 > B1	X	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 < B1	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 > B0	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 < B0	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	L	L	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	H	L	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	H	L	L	H
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	H	H	L	H	H
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	L	H	H	L	H
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	H	H	H	H	H
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	H	L	H	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	L	L	L	L

H = high level, L = low level, X = irrelevant

MM54C89/MM74C89 64-bit TRI-STATE® random access read/write memory

general description

The MM54C89/MM74C89 is a 16-word by 4-bit random access read/write memory. Inputs to the memory consist of four address lines, four data input lines, a $\overline{\text{write enable}}$ line and a $\overline{\text{memory enable}}$ line. The four binary address inputs are decoded internally to select each of the 16 possible word locations. An internal address register, latches the address information on the positive to negative transition of the $\overline{\text{memory enable}}$ input. The four TRI-STATE® data output lines working in conjunction with the $\overline{\text{memory enable}}$ input provides for easy memory expansion.

Address Operation: Address inputs must be stable t_{SA} prior to the positive to negative transition of $\overline{\text{memory enable}}$. It is thus not necessary to hold address information stable for more than t_{HA} after the memory is enabled (positive to negative transition of $\overline{\text{memory enable}}$).

Note: The timing is different than the DM7489 in that a positive to negative transition of the $\overline{\text{memory enable}}$ must occur for the memory to be selected.

Write Operation: Information present at the data inputs is written into the memory at the selected address by bringing $\overline{\text{write enable}}$ and $\overline{\text{memory enable}}$ low.

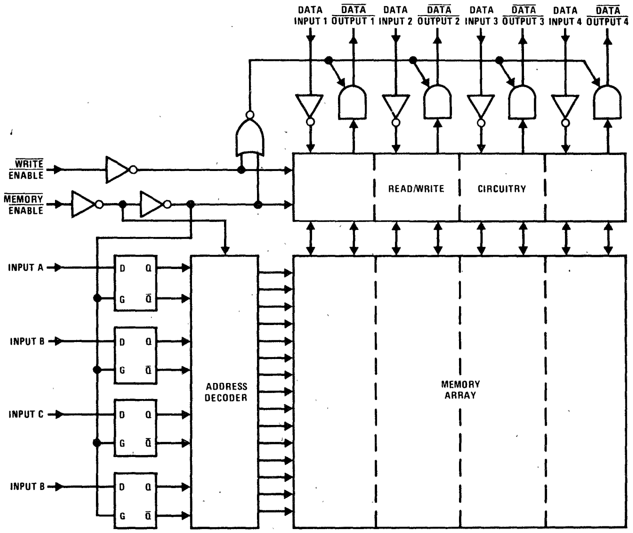
Read Operation: The complement of the information which was written into the memory is non-destructively read out at the four outputs. This is accomplished by selecting the desired address and bringing $\overline{\text{memory enable}}$ low and $\overline{\text{write enable}}$ high.

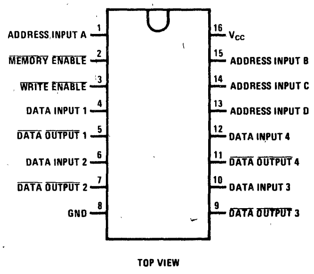
When the device is writing or disabled the output assumes a TRI-STATE (Hi-z) condition.

features

■ Wide supply voltage range	3.0V to 15V
■ Guaranteed noise margin	1.0V
■ High noise immunity	0.45 V_{CC} typ
■ Low power TTL compatibility	fan out of 2 driving 74L
■ Input address register	
■ Low power consumption	100 nW/package typ @ V_{CC} = 5V
■ Fast access time	130 ns typ at V_{CC} = 10V
■ TRI-STATE output	

logic and connection diagrams





TOP VIEW

absolute maximum ratings

Voltage at Any Pin	−0.3V to V_{CC} + 0.3V
Operating Temperature Range	
MM54C89	−55°C to +125°C
MM74C89	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500 mW
Operating V_{CC} Range	3.0V to 15V
Absolute Maximum V_{CC}	16V
Lead Temperature (Soldering, 10 seconds)	300°C

dc electrical characteristics

Min/max limits apply across temperature range, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CMOS TO CMOS					
Logical "1" Input Voltage ($V_{IN(1)}$)	V_{CC} = 5.0V	3.5			V
	V_{CC} = 10V	8.0			V
Logical "0" Input Voltage ($V_{IN(0)}$)	V_{CC} = 5.0V			1.5	V
	V_{CC} = 10V			2.0	V
Logical "1" Output Voltage ($V_{OUT(1)}$)	V_{CC} = 5.0V, I_O = −10μA	4.5			V
	V_{CC} = 10V, I_O = −10μA	9.0			V
Logical "0" Output Voltage ($V_{OUT(0)}$)	V_{CC} = 5.0V, I_O = +10μA			0.5	V
	V_{CC} = 10V, I_O = +10μA			1.0	V
Logical "1" Input Current ($I_{IN(1)}$)	V_{CC} = 15V, V_{IN} = 15V		0.005	1.0	μA
Logical "0" Input Current ($I_{IN(0)}$)	V_{CC} = 15V, V_{IN} = 0V	−1.0	−0.005		μA
Output Current in High Impedance State	V_{CC} = 15V, V_O = 15V		0.005	1.0	μA
	V_{CC} = 15V, V_O = 0V	−1.0	−0.005		μA
Supply Current (I_{CC})	V_{CC} = 15V		0.05	300	μA
CMOS/LPTTL INTERFACE					
Logical "1" Input Voltage ($V_{IN(1)}$)	54C, V_{CC} = 4.5V	V_{CC} − 1.5			V
	74C, V_{CC} = 4.75V	V_{CC} − 1.5			V
Logical "0" Input Voltage ($V_{IN(0)}$)	54C, V_{CC} = 4.5V			0.8	V
	74C, V_{CC} = 4.75V			0.8	V
Logical "1" Output Voltage ($V_{OUT(1)}$)	54C, V_{CC} = 4.5V, I_O = −360μA	2.4			V
	74C, V_{CC} = 4.75V, I_O = −360μA	2.4			V
Logical "0" Output Voltage ($V_{OUT(0)}$)	54C, V_{CC} = 4.5V, I_O = +360μA			0.4	V
	74C, V_{CC} = 4.75V, I_O = +360μA			0.4	V
OUTPUT DRIVE (See 54C/74C Family Characteristics Data Sheet)					
Output Source Current (I_{SOURCE}) (P-Channel)	V_{CC} = 5.0V, V_{OUT} = 0V T_A = 25°C	−1.75	−3.3		mA
Output Source Current (I_{SOURCE}) (P-Channel)	V_{CC} = 10V, V_{OUT} = 0V T_A = 25°C	−8.0	−15		mA
Output Sink Current (I_{SINK}) (N-Channel)	V_{CC} = 5.0V, V_{OUT} = V_{CC} T_A = 25°C	1.75	3.6		mA
Output Sink Current (I_{SINK}) (N-Channel)	V_{CC} = 10V, V_{OUT} = V_{CC} T_A = 25°C	8.0	16		mA

ac electrical characteristics (T_A = 25°C, C_L = 50 pF, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Propagation Delay from $\overline{\text{Memory}}$ $\overline{\text{Enable}}$ (t_{pd})	V_{CC} = 5.0V		270	500	ns
	V_{CC} = 10V		100	220	ns
Access Time from Address Input (t_{acc})	V_{CC} = 5.0V		350	650	ns
	V_{CC} = 10V		130	280	ns
Address Input Setup Time (t_{SA})	V_{CC} = 5.0V	150			ns
	V_{CC} = 10V	60			ns
Address Input Hold Time (t_{HA})	V_{CC} = 5.0V	60			ns
	V_{CC} = 10V	40			ns
$\overline{\text{Memory}}$ $\overline{\text{Enable}}$ Pulse Width (t_{ME})	V_{CC} = 5.0V	400	250		ns
	V_{CC} = 10V	150	90		ns
$\overline{\text{Memory}}$ $\overline{\text{Enable}}$ Pulse Width ($t_{\overline{ME}}$)	V_{CC} = 5.0V	400	200		ns
	V_{CC} = 10V	150	70		ns

ac electrical characteristics (con't)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{\text{Write}}$ $\overline{\text{Enable}}$ Setup Time for a Read (t_{SR})	V_{CC} = 5.0V V_{CC} = 10V	0 0			ns ns
$\overline{\text{Write}}$ $\overline{\text{Enable}}$ Setup Time for a Write (t_{WS})	V_{CC} = 5.0V V_{CC} = 10V			t_{ME} t_{ME}	ns ns
$\overline{\text{Write}}$ $\overline{\text{Enable}}$ Pulse Width ($t_{\overline{WE}}$)	V_{CC} = 5.0V, t_{WS} = 0 V_{CC} = 10V, t_{WS} = 0	300 100	160 60		ns ns
Data Input Hold Time (t_{HD})	V_{CC} = 5.0V V_{CC} = 10V	50 25			ns ns
Data Input Setup (t_{SD})	V_{CC} = 5.0V V_{CC} = 10V	50 25			ns ns
Propagation Delay from a Logical "1" or Logical "0" to the High Impedance State from $\overline{\text{Memory}}$ $\overline{\text{Enable}}$ (t_{1H}, t_{0H})	V_{CC} = 5.0V, C_L = 5.0 pF, R_L = 10k V_{CC} = 10V, C_L = 5.0 pF, R_L = 10k		180 85	300 120	ns ns
Propagation Delay from a Logical "1" or Logical "0" to the High Impedance State from $\overline{\text{Write}}$ $\overline{\text{Enable}}$ (t_{1H}, t_{0H})	V_{CC} = 5.0V, C_L = 5.0 pF, R_L = 10k V_{CC} = 10V, C_L = 5.0 pF, R_L = 10k		180 85	300 120	ns ns
Input Capacity (C_{IN})	Any Input (Note 2)		5.0		pF
Output Capacity (C_{OUT})	Any Output (Note 2)		6.5		pF
Power Dissipation Capacity (C_{pd})	(Note 3)		230		pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

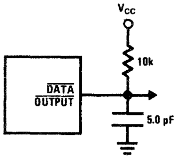
Note 3: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note, AN-90.

truth table

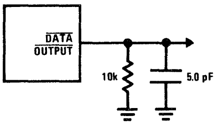
ME	WE	OPERATION	CONDITION OF OUTPUTS
L	L	Write	TRI-STATE
L	H	Read	Complement of Selected Word
H	L	Inhibit, Storage	TRI-STATE
H	H	Inhibit, Storage	TRI-STATE

ac test circuits

t_{0H}

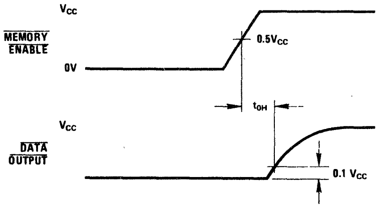


t_{1H}

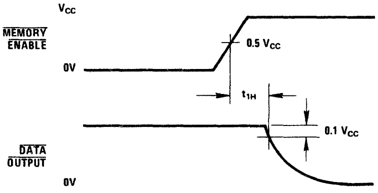


switching time waveforms

t_{0H}

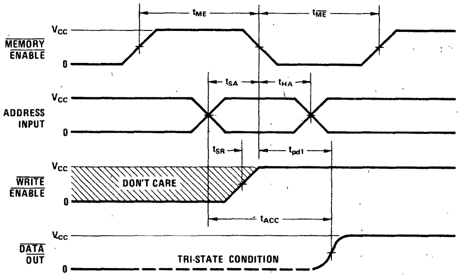


t_{1H}

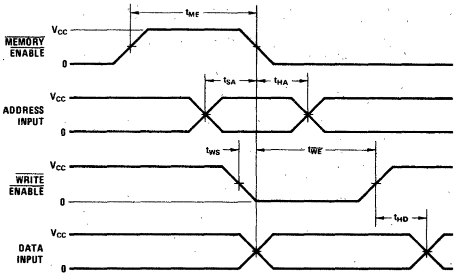


switching time waveforms (con't)

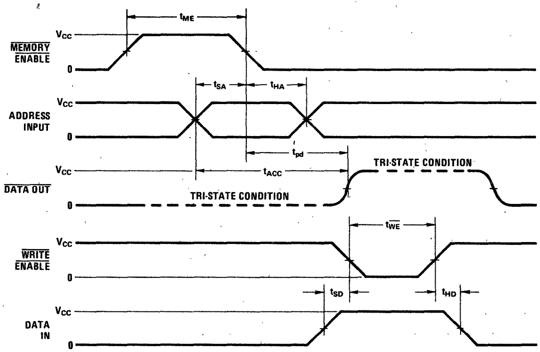
Read Cycle



Write Cycle



Read Modify Write Cycle



NOTE: $t_r = 60$ ns
$t_f = 10$ ns

MM54C90/MM74C90 4-bit decade counter
MM54C93/MM74C93 4-bit binary counter

general description

The MM54C90/MM74C90 decade counter and the MM54C93/MM74C93 binary counter are complementary MOS (CMOS) integrated circuits constructed with N and P-channel enhancement mode transistors. The 4-bit decade counter can be reset to zero or preset to nine by applying appropriate logic level on the R_{01}, R_{02}, R_{91} and R_{92} inputs, also a separate flip-flop on the A-bit enables the user to operate it as a divide-by-2, 5 or 10 frequency counter. The 4-bit binary counter can be reset to zero by applying high logic level on inputs R_{01} and R_{02}, also a separate flip-flop on the A-bit enables the user to operate it as a divide-by-2, 8 or 16 divider.

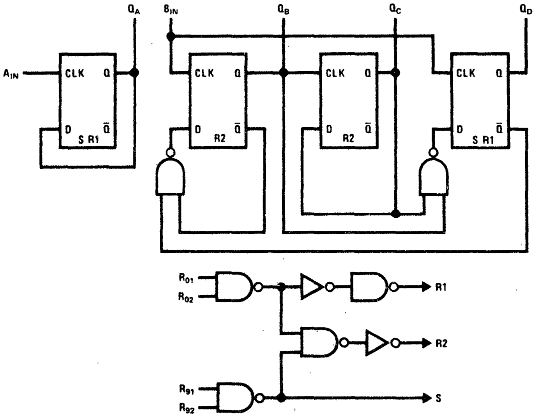
All inputs are protected against static discharge damage.

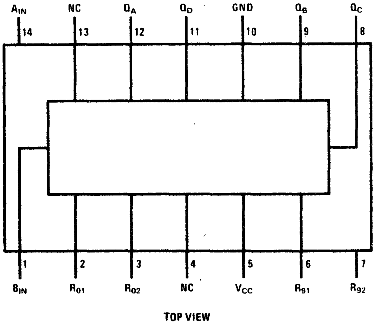
features

■ Wide supply voltage range	3V to 15V
■ Guaranteed noise margin	1V
■ High noise immunity	0.45 V_{CC} (typ)
■ Low power TTL compatibility	fan out of 2 driving 74L

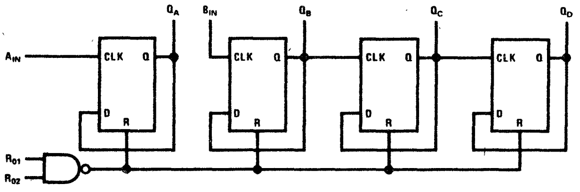
logic and connection diagrams

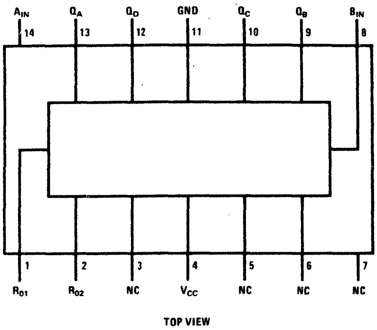
MM54C90/MM74C90





MM54C93/MM74C93





absolute maximum ratings (Note 1)

Voltage at Any Pin	−0.3V to V_{CC} +0.3V	Operating V_{CC} Range	3V to 15V
Operating Temperature Range		Absolute Maximum V_{CC}	16V
MM54C90, MM54C93	−55°C to +125°C	Storage Temperature Range	−65°C to +150°C
MM74C90, MM74C93	−40°C to +85°C	Lead Temperature (Soldering, 10 seconds)	300°C
Package Dissipation	500 mW		

dc electrical characteristics Min/max limits apply across temperature range, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CMOS TO CMOS					
Logical "1" Input Voltage ($V_{IN(1)}$)	V_{CC} = 5V V_{CC} = 10V	3.5 8			V V
Logical "0" Input Voltage ($V_{IN(0)}$)	V_{CC} = 5V V_{CC} = 10V			1.5 2	V V
Logical "1" Output Voltage ($V_{OUT(1)}$)	V_{CC} = 5V, I_O = −10μA V_{CC} = 10V, I_O = −10μA	4.5 9			V V
Logical "0" Output Voltage ($V_{OUT(0)}$)	V_{CC} = 5V, I_O = +10μA V_{CC} = 10V, I_O = +10μA			0.5 1	V V
Logical "1" Input Current ($I_{IN(1)}$)	V_{CC} = 15V, V_{IN} = 15V		0.005	1	μA
Logical "0" Input Current ($I_{IN(0)}$)	V_{CC} = 15V, V_{IN} = 0V	−1	−0.005		μA
Supply Current (I_{CC})	V_{CC} = 15V		0.05	300	μA
CMOS/LPTTL INTERFACE					
Logical "1" Input Volage ($V_{IN(1)}$) MM54C90, MM54C93 MM74C90, MM74C93	 V_{CC} = 4.5V V_{CC} = 4.75V	 V_{CC}−1.5 V_{CC}−1.5			 V V
Logical "0" Input Voltage ($V_{IN(0)}$) MM54C90, MM54C93 MM74C90, MM74C93	 V_{CC} = 4.5V V_{CC} = 4.75V			 0.8 0.8	 V V
Logical "1" Output Voltage ($V_{OUT(1)}$) MM54C90, MM54C93 MM74C90, MM74C93	 V_{CC} = 4.5V, I_O = −360μA V_{CC} = 4.75V, I_O = −360μA	 2.4 2.4			 V V
Logical "0" Output Voltage ($V_{OUT(0)}$) MM54C90, MM54C93 MM74C90, MM74C93	 V_{CC} = 4.5V, I_O = 360μA V_{GC} = 4.75V, I_O = 360μA			 0.4 0.4	 V V
OUTPUT DRIVE (See 54C/74C Family Characteristics Data Sheet)					
Output Source Current (I_{SOURCE}) (P-Channel)	V_{CC} = 5V, V_{OUT} = 0V, T_A = 25°C	−1.75	−3.3		mA
Output Source Current (I_{SOURCE}) (P-Channel)	V_{CC} = 10V, V_{OUT} = 0V, T_A = 25°C	−8	−15		mA
Output Sink Current (I_{SINK}) (N-Channel)	V_{CC} = 5V, V_{OUT} = V_{CC}, T_A = 25°C	1.75	3.6		mA
Output Sink Current (I_{SINK}) (N-Channel)	V_{CC} = 10V, V_{OUT} = V_{CC}, T_A = 25°C	8	16		mA

ac electrical characteristics T_A = 25°C, C_L = 50 pF, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Propagation Delay Time From A_{IN} to Q_A (t_{pd0} or t_{pd1})	V_{CC} = 5V V_{CC} = 10V		200 80	400 150	ns ns
Propagation Delay Time From A_{IN} to Q_B (t_{pd0} or t_{pd1}) (MM54C93/MM74C93)	V_{CC} = 5V V_{CC} = 10V		450 160	850 300	ns ns
Propagation Delay Time From A_{IN} to Q_B (t_{pd0} or t_{pd1}) (MM54C90/MM74C90)	V_{CC} = 5V V_{CC} = 10V		450 160	800 300	ns ns
Propagation Delay Time From A_{IN} to Q_C (t_{pd0} or t_{pd1}) (MM54C93/MM74C93)	V_{CC} = 5V V_{CC} = 10V		500 200	1050 400	ns ns
Propagation Delay Time From A_{IN} to Q_C (t_{pd0} or t_{pd1}) (MM54C90/MM74C90)	V_{CC} = 5V V_{CC} = 10V		500 200	1000 400	ns ns
Propagation Delay Time From A_{IN} to Q_D (t_{pd0} or t_{pd1}) (MM54C93/MM74C93)	V_{CC} = 5V V_{CC} = 10V		600 250	1200 500	ns ns
Propagation Delay Time From A_{IN} to Q_D (t_{pd0} or t_{pd1}) (MM54C90/MM74C90)	V_{CC} = 5V V_{CC} = 10V		450 160	800 300	ns ns

ac electrical characteristics (con't)

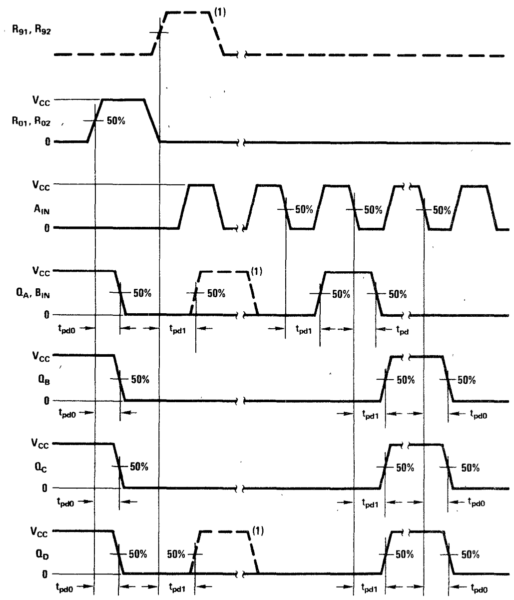
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Propagation Delay Time From R_{01} or R_{02} to Q_A, Q_B, Q_C or Q_D (t_{pd0} or t_{pd1}) (MM54C93/MM74C93)	V_{CC} = 5V V_{CC} = 10V		150 75	300 150	ns ns
Propagation Delay Time From R_{01} or R_{02} to Q_A, Q_B, Q_C or Q_D (t_{pd0} or t_{pd1}) (MM54C90/MM74C90)	V_{CC} = 5V V_{CC} = 10V		200 75	400 150	ns ns
Propagation Delay Time From R_{91} or R_{92} to Q_A or Q_D (t_{pd0} or t_{pd1}) (MM54C90/MM74C90)	V_{CC} = 5V V_{CC} = 10V		250 100	500 200	ns ns
Maximum Clock Rise and Fall Time	V_{CC} = 5V V_{CC} = 10V			15 5	µs µs
Minimum Clock Pulse Width (t_W)	V_{CC} = 5V V_{CC} = 10V	250 100	100 50		ns ns
Maximum Clock Frequency	V_{CC} = 5V V_{CC} = 10V	2 5			MHz MHz
Input Capacitance	Any Input (Note 2)		5		pF
Power Dissipation Capacitance (C_{PD})	Per Package (Note 3)		45		pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

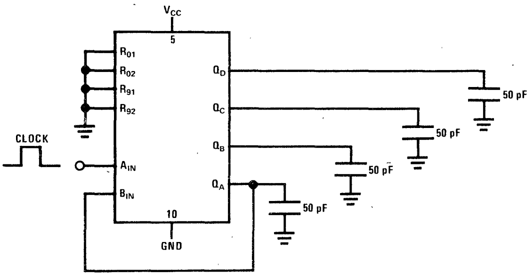
Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note, AN-90.

switching time waveforms and ac test circuits

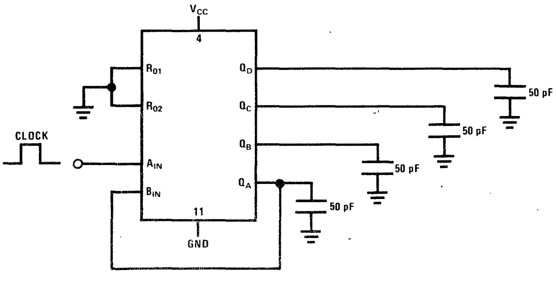


Note 1: MM54790, MM74C90 and MM54793, MM74C43 are solid line waveforms. Dashed line waveforms are for MM54C90/MM74C90 only.



Clock rise and fall time $t_r = t_f = 20$ ns

MM54C90/MM74C90



Clock rise and fall time $t_r = t_f = 20$ ns

MM54C93/MM74C93

truth tables

MM54C90/MM74C90 4-Bit Decade Counter

BCD Count Sequence

COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

Output Q_A is connected to input B for BCD count.

H = High level
L = Low level
X = Irrelevant

Reset/Count Function Table

RESET INPUTS				OUTPUT			
R_{01}	R_{02}	R_{91}	R_{92}	Q_D	Q_C	Q_B	Q_A
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
X	L	X	L	COUNT			
L	X	L	X	COUNT			
L	X	X	L	COUNT			
X	L	L	X	COUNT			

MM54C93/MM74C93 4-Bit Binary Counter

Binary Count Sequence

COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	H
13	H	H	L	L
14	H	H	H	L
15	H	H	H	H

Output Q_A is connected to input B for binary count sequence.

H = High level
L = Low level
X = Irrelevant

Reset/Count Function Table

RESET INPUTS		OUTPUT			
R_{01}	R_{02}	Q_D	Q_C	Q_B	Q_A
H	H	L	L	L	L
L	X	COUNT			
X	L	COUNT			

MM54C95/MM74C95 4-bit right-shift left-shift register

general description

This 4-bit shift register is a monolithic complementary MOS (CMOS) integrated circuit composed of four D flip flops. This register will perform right-shift or left-shift operations dependent upon the logical input level to the mode control. A number of these registers may be connected in series to form an N-bit right shift or left shift register.

When a logical "0" level is applied to the mode control input, the output of each flip flop is coupled to the D input of the succeeding flip flop. Right-shift operation is performed by clocking at the clock 1 input, and serial data entered at the serial input, clock 2 and parallel inputs A through D are inhibited. With a logical "1" level applied to the mode control, outputs to succeeding stages are decoupled and parallel loading is possible, or with external interconnection, shift-left operation can be accomplished by connecting the output of each flip flop to the parallel input of the previous flip flop and serial data is entered at input D.

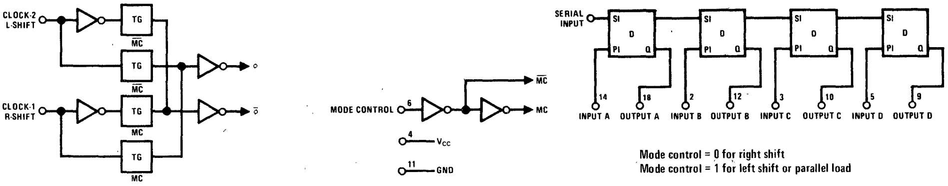
features

■ Medium speed operation	10 MHz typ V_{CC} = 10V, C_L = 50 pF
■ High noise immunity	0.45 V_{CC} typ
■ Low power	100 nW typ
■ Tenth power TTL compatible	Drive 2 LTTL loads
■ Wide supply voltage range	3V to 15V
■ Synchronous parallel load	
■ Parallel inputs and outputs from each flip flop	
■ Negative edge triggered clocking	

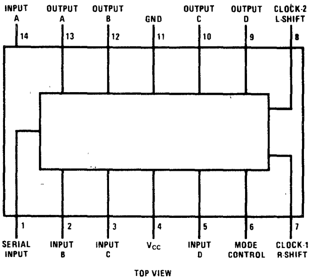
applications

- Data terminals
- Instrumentation
- Automotive
- Medical electronics
- Alarm systems
- Remote metering
- Industrial electronics
- Computers

block and connection diagrams



Mode control = 0 for right shift
Mode control = 1 for left shift or parallel load



TOP VIEW

absolute maximum ratings

Voltage at Any Pin (Note 1)	$-0.3V$ to V_{CC} $+0.3V$	Maximum V_{CC} Voltage	16V
Operating Temperature MM54C95	$-55°C$ to $+125°C$	Package Dissipation	500 mW
MM74C95	$-40°C$ to $+85°C$	Operating V_{CC} Range	+3V to +15V
Storage Temperature	$-65°C$ to $+150°C$	Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics

Max/min limits apply across temperature range unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CMOS TO CMOS					
Logical "1" Input Voltage $V_{IN(1)}$	V_{CC} = 5.0V V_{CC} = 10.0V	3.5 8			V V
Logical "0" Input Voltage $V_{IN(0)}$	V_{CC} = 5.0V V_{CC} = 10.0V			1.5 2	V V
Logical "1" Output Voltage $V_{OUT(1)}$	V_{CC} = 5.0V V_{CC} = 10.0V	4.5 9			V V
Logical "0" Output Voltage $V_{OUT(0)}$	V_{CC} = 5.0V V_{CC} = 10.0V			.5 1	V V
Logical "1" Input Current $I_{IN(1)}$	V_{CC} = 15.0V			1	µA
Logical "0" Input Current $I_{IN(0)}$	V_{CC} = 15.0V	−1			µA
Supply Current I_{CC}	V_{CC} = 15.0V		0.050	300	µA
Input Capacitance	Any Input		5		pF
Propagation Delay Time to a Logical "0" t_{pd0} or Logical "1" t_{pd1} From Clock to Q or $\bar{Q}$	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C V_{CC} = 10.0V, C_L = 50 pF, T_A = 25°C		200 80	400 160	ns ns
Time Prior to Clock Pulse That Data Must be Preset t_{SETUP}	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C V_{CC} = 10.0V, C_L = 50 pF, T_A = 25°C	60 25	30 10		ns ns
Time After Clock Pulse That Data Must be Held	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C V_{CC} = 10.0V, C_L = 50 pF, T_A = 25°C	25 10	10 50		ns ns
Minimum Clock Pulse Width ($t_{WL} = t_{WH}$)	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C V_{CC} = 10.0V, C_L = 50 pF, T_A = 25°C		100 50		ns ns
Time Prior to Clock Pulse that Mode Control must be Preset	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C V_{CC} = 10.0V, C_L = 50 pF, T_A = 25°C	200 100	100 50		ns ns
Maximum Input Clock Frequency	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C V_{CC} = 10.0V, C_L = 50 pF, T_A = 25°C	3 6.5	5 10		MHz MHz
LOW POWER TTL/CMOS INTERFACE					
Logical "1" Input Voltage $V_{IN(1)}$	54C, V_{CC} = 4.5V 74C, V_{CC} = 4.75V	$V_{CC}-1.5$			V
Logical "0" Input Voltage $V_{IN(0)}$	54C, V_{CC} = 4.5V 74C, V_{CC} = 4.75V			0.8	V
Logical "1" Output Voltage $V_{OUT(1)}$	54C, V_{CC} = 4.5V, I_D = −100 µA 74C, V_{CC} = 4.75V, I_D = −100 µA	2.4			V
Logical "0" Output Voltage $V_{OUT(0)}$	54C, V_{CC} = 4.5V, I_D = 360 µA 74C, V_{CC} = 4.75V, I_D = 360 µA			0.4	V
Propagation Delay Time to a Logical "0" t_{pd0} or Logical "1" t_{pd1} From Clock to Q or $\bar{Q}$	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C		175		ns

Note 1: These devices should not be connected under "Power On" conditions.

function table

INPUTS								OUTPUTS			
MODE CONTROL	CLOCKS		SERIAL	PARALLEL				Q_A	Q_B	Q_C	Q_D
	2 (L)	1 (R)		A	B	C	D				
H	H	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	↓	X	X	a	b	c	d	a	b	c	d
H	↓	X	X	Q_B†	Q_C†	Q_D†	d	Q_{Bn}	Q_{Cn}	Q_{Dn}	d
L	L	H	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
L	X	↓	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}
L	X	↓	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}
↑	L	L	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↓	L	L	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↓	L	H	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↑	H	L	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↑	H	H	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↑	L	H	X	X	X	X	X	Undefined			
↓	H	L	X	X	X	X	X	Operating Conditions			

†Shifting left requires external connection of Q_B to A, Q_C to B, and Q_D to C. Serial data is entered at input D.

H = high level (steady state), L = low level (steady state), X = irrelevant (any input, including transitions)

↓ = transition from high to low level, ↑ = transition from low to high level

a, b, c, d = the level of steady-state input at inputs A, B, C or D, respectively.

Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady-state input conditions were established.

Q_{An}, Q_{Bn}, Q_{Cn}, Q_{Dn} = the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the most-recent ↓ transition of the clock.

MM54C151/MM74C151 8 channel digital multiplexer

general description

The MM54C151/MM74C151 multiplexer is a monolithic complementary MOS (CMOS) integrated circuit constructed with N- and P-channel enhancement transistors.

This data selector/multiplexer contains on-chip binary decoding. Two outputs provide true (output Y) and complement (output W) data. A logical "1" on the strobe input forces W to a logical "1" and Y to a logical "0."

All inputs are protected against electrostatic effects.

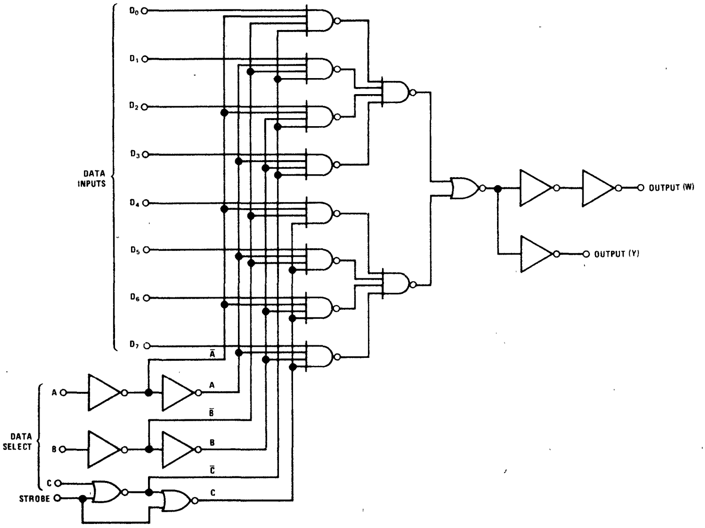
features

- Supply voltage range 3V to 15V
- Tenth power TTL compatible drive 2 LPTTL loads
- High noise immunity 0.45 V_{CC} typ
- Low power 50 nW typ

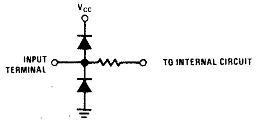
applications

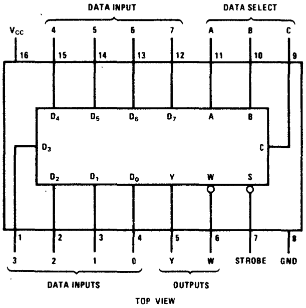
- Automotive
- Data terminals
- Instrumentation
- Medical electronics
- Alarm systems
- Industrial electronics
- Remote metering
- Computers

logic and connection diagrams



Input Protection For All Inputs





TOP VIEW

absolute maximum ratings

Voltage at Any Pin (Note 1)		$-0.3V$ to V_{CC} $+0.3V$
Operating Temperature	MM54C151	$-55°C$ to $+125°C$
	MM74C151	$-40°C$ to $+85°C$
Storage Temperature		$-65°C$ to $+150°C$
Maximum V_{CC} Voltage		16V
Package Dissipation		500 mW
Operating V_{CC} Range		3V to 15V
Lead Temperature (Soldering, 10 sec)		300°C

electrical characteristics

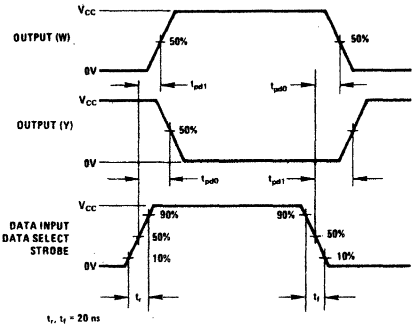
Min/Max limits apply across temperature range across otherwise specified

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CMOS TO CMOS					
Logical "1" Input Voltage $V_{IN(1)}$	$V_{CC} = 5.0V$ $V_{CC} = 10.0V$	3.5 8			V V
Logical "0" Input Voltage $V_{IN(0)}$	$V_{CC} = 5.0V$ $V_{CC} = 10.0V$			1.5 2	V V
Logical "1" Output Voltage $V_{OUT(1)}$	$V_{CC} = 5.0V$, $I_O = -10\mu A$ $V_{CC} = 10.0V$, $I_O = -10\mu A$	4.5 9			V V
Logical "0" Output Voltage $V_{OUT(0)}$	$V_{CC} = 5.0V$, $I_O = +10\mu A$ $V_{CC} = 10.0V$, $I_O = +10\mu A$			0.5 1	V V
Logical "1" Input Current $I_{IN(1)}$	$V_{CC} = 15.0V$, $V_{IN} = 15V$			1	μA
Logical "0" Input Current $I_{IN(0)}$	$V_{CC} = 15.0V$, $V_{IN} = 0V$	-1			μA
Supply Current I_{CC}	$V_{CC} = 15.0V$		0.05	300	μA
Input Capacitance	Any Input		5		pF
Propagation Delay Time to a Logical "0" or Logical "1" from Data to Y	$V_{CC} = 5.0V$, $C_L = 50$ pF, $T_A = 25°C$ $V_{CC} = 10.0V$, $C_L = 50$ pF, $T_A = 25°C$		170 80	270 130	ns ns
Propagation Delay Time to a Logical "0" or Logical "1" from Data to W	$V_{CC} = 5.0V$, $C_L = 50$ pF, $T_A = 25°C$ $V_{CC} = 10.0V$, $C_L = 50$ pF, $T_A = 25°C$		200 90	300 140	ns ns
Propagation Delay Time to a Logical "0" or Logical "1" from Strobe or Data Select to Y	$V_{CC} = 5.0V$, $C_L = 50$ pF, $T_A = 25°C$ $V_{CC} = 10.0V$, $C_L = 50$ pF, $T_A = 25°C$		240 110	360 170	ns ns
CMOS TO TENTH POWER INTERFACE					
Logical "1" Input Voltage $V_{IN(1)}$	54C, $V_{CC} = 4.5V$ 74C, $V_{CC} = 4.75V$	$V_{CC} - 1.5$			V
Logical "0" Input Voltage $V_{IN(0)}$	54C, $V_{CC} = 4.5V$ 74C, $V_{CC} = 4.75V$			0.8	V
Logical "1" Output Voltage $V_{OUT(1)}$	54C, $V_{CC} = 4.5V$, $I_O = -360\mu A$ 74C, $V_{CC} = 4.75V$, $I_O = -360\mu A$	2.4			V
Logical "0" Output Voltage $V_{OUT(0)}$	54C, $V_{CC} = 4.5V$, $I_O = 360\mu A$ 74C, $V_{CC} = 4.75V$, $I_O = 360\mu A$			0.4	V
Propagation Delay Time to a Logical "0" t_{pd0} or a Logical "1" t_{pd1} from Data Input, to Y	$V_{CC} = 5.0V$, $C_L = 50$ pF, $T_A = 25°C$		200	320	ns

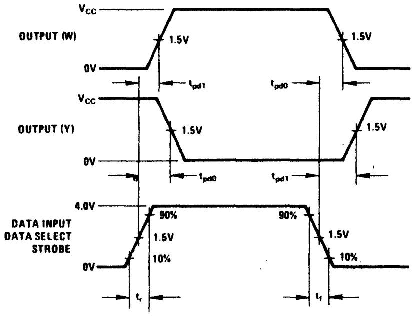
Note 1: This device should not be connected under power on conditions.

switching time waveforms

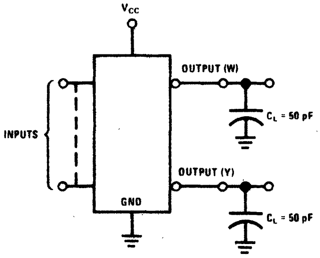
CMOS to CMOS (t_{pd1} & t_{pd0})



TTL to CMOS (t_{pd1} & t_{pd0})



ac test circuit



truth table

INPUTS												OUTPUTS	
C	B	A	STROBE	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	Y	W
X	X	X	1	X	X	X	X	X	X	X	X	0	1
0	0	0	0	0	X	X	X	X	X	X	X	0	1
0	0	0	0	1	X	X	X	X	X	X	X	1	0
0	0	1	0	X	0	X	X	X	X	X	X	0	1
0	0	1	0	X	1	X	X	X	X	X	X	1	0
0	1	0	0	X	X	0	X	X	X	X	X	0	1
0	1	0	0	X	X	1	X	X	X	X	X	1	0
0	1	1	0	X	X	X	0	X	X	X	X	0	1
0	1	1	0	X	X	X	1	X	X	X	X	1	0
1	0	0	0	X	X	X	X	0	X	X	X	0	1
1	0	0	0	X	X	X	X	1	X	X	X	1	0
1	0	1	0	X	X	X	X	X	0	X	X	0	1
1	0	1	0	X	X	X	X	X	1	X	X	1	0
1	1	0	0	X	X	X	X	X	X	0	X	0	1
1	1	0	0	X	X	X	X	X	X	1	X	1	0
1	1	1	0	X	X	X	X	X	X	X	0	0	1
1	1	1	0	X	X	X	X	X	X	X	1	1	0

MM54C154/MM74C154 4-line to 16-line decoder/demultiplexer

general description

The MM54C154/MM74C154 one of sixteen decoder is a monolithic complementary MOS (CMOS) integrated circuit constructed with N and P-channel enhancement transistors. The device is provided with two strobe inputs, both of which must be in the logical "0" state for normal operation. If either strobe input is in the logical "1" state, all 16 outputs will go to the logical "1" state.

To use the product as a demultiplexer, one of the strobe inputs serves as a data input terminal, while the other strobe input must be maintained in the logical "0" state. The information will then be transmitted to the selected output as determined by the 4-line input address.

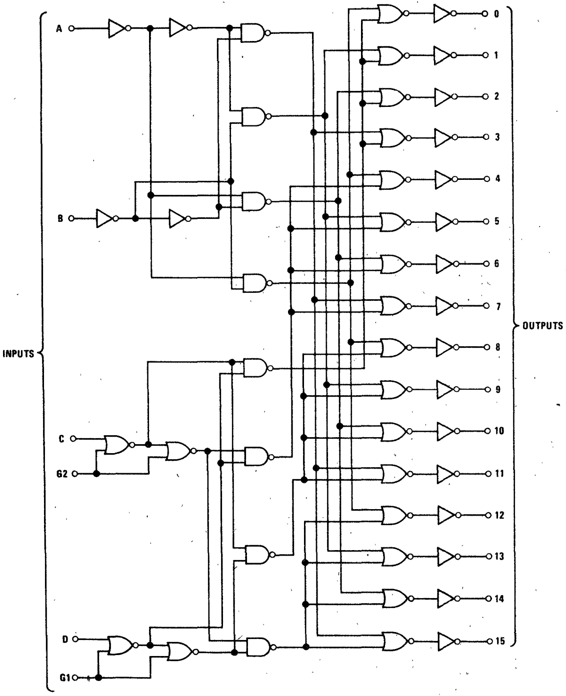
features

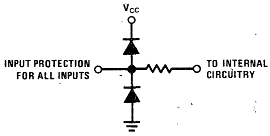
- Supply voltage range 3V to 15V
- Tenth power TTL compatible drive 2 LPTTL loads
- High noise margin 1V guaranteed
- High noise immunity 0.45 V_{CC} typ
- Low power 750 nW typ

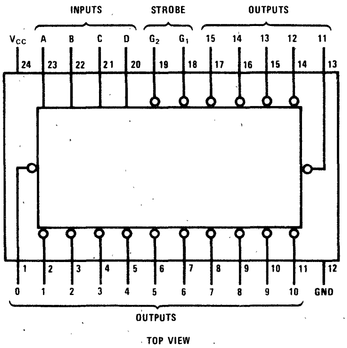
applications

- Automotive
- Data terminals
- Instrumentation
- Medical electronics
- Alarm systems
- Industrial electronics
- Remote metering
- Computers

logic and connection diagrams







TOP VIEW

absolute maximum ratings

Voltage at Any Pin (Note 1)	−0.3V to V_{CC} +0.3V
Operating Temperature Range	
MM54C154	−55°C to +125°C
MM74C154	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Maximum V_{CC} Voltage	16V
Package Dissipation	500 mW
Operating Range, V_{CC}	+3V to +15V
Lead Temperature (Soldering, 10 sec)	300°C

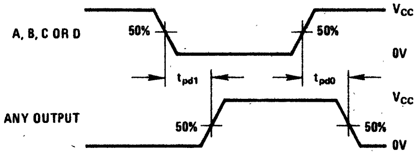
electrical characteristics

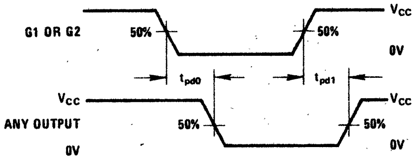
(Min/max limits apply across temperature range unless otherwise specified.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CMOS TO CMOS					
Logical "1" Input Voltage ($V_{IN(1)}$)	V_{CC} = 5V V_{CC} = 10V	3.5 8			V V
Logical "0" Input Voltage ($V_{IN(0)}$)	V_{CC} = 5V V_{CC} = 10 V			1.5 2	V V
Logical "1" Output Voltage ($V_{OUT(1)}$)	V_{CC} = 5V, I_O = −10μA V_{CC} = 10V, I_O = −10μA	4.5 9			V V
Logical "0" Output Voltage ($V_{OUT(0)}$)	V_{CC} = 5V, I_O = +10μA V_{CC} = 10V, I_O = +10μA			0.5 1	V V
Logical "1" Input Current ($I_{IN(1)}$)	V_{CC} = 15V, V_{IN} = 15V		0.005	1	μA
Logical "0" Input Current ($I_{IN(0)}$)	V_{CC} = 15V, V_{IN} = 0V	−1	-0.005		μA
Supply Current (I_{CC})	V_{CC} = 15V		0.05	300	μA
Input Capacitance	Any Input		5		pF
Propagation Delay to a Logical "0" From Any Input to Any Output (t_{pd0})	V_{CC} = 5V, C_L = 50 pF, T_A = 25°C V_{CC} = 10V, C_L = 50 pF, T_A = 25°C		275 100	400 200	ns ns
Propagation Delay to a Logical "0" From G1 or G2 to Any Output (t_{pd0})	V_{CC} = 5V, C_L = 50 pF, T_A = 25°C V_{CC} = 10V, C_L = 50 pF, T_A = 25°C		275 100	400 200	ns ns
Propagation Delay to a Logical "1" From Any Input to Any Output (t_{pd1})	V_{CC} = 5V, C_L = 50 pF, T_A = 25°C V_{CC} = 10V, C_L = 50 pF, T_A = 25°C		265 100	400 200	ns ns
Propagation Delay to a Logical "1" From G1 or G2 to Any Output (t_{pd1})	V_{CC} = 5V, C_L = 50 pF, T_A = 25°C V_{CC} = 10V, C_L = 50 pF, T_A = 25°C		265 100	400 200	ns ns
LOW POWER TTL/CMOS INTERFACE					
Logical "1" Input Voltage ($V_{IN(1)}$)	54C V_{CC} = 4.5 74C V_{CC} = 4.75	V_{CC} − 1.5			V
Logical "0" Input Voltage ($V_{IN(0)}$)	54C V_{CC} = 4.5 74C V_{CC} = 4.75			0.8	V
Logical "1" Output Voltage ($V_{OUT(1)}$)	54C V_{CC} = 4.5V, I_O = −100μA 74C V_{CC} = 4.75V, I_O = −100μA	2.4			V
Logical "0" Output Voltage ($V_{OUT(0)}$)	54C V_{CC} = 4.5V, I_O = 360μA 74C V_{CC} = 4.75V, I_O = 360μA			0.4	V

Note 1: This device should not be connected to circuits with the power on because high transient voltages may cause permanent damage.

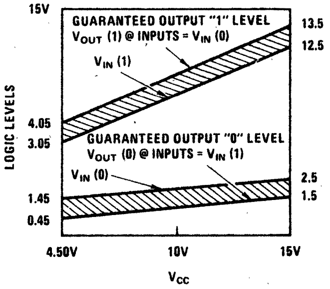
switching time waveforms





$t_r = t_f = 20$ ns

Guaranteed Noise Margin as a Function of V_{CC}



truth table

INPUTS						OUTPUTS															
G1	G2	D	C	B	A	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	L	L	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	H	H	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H

X = "Don't Care" Condition

MM54C157/MM74C157 quad 2-input multiplexers

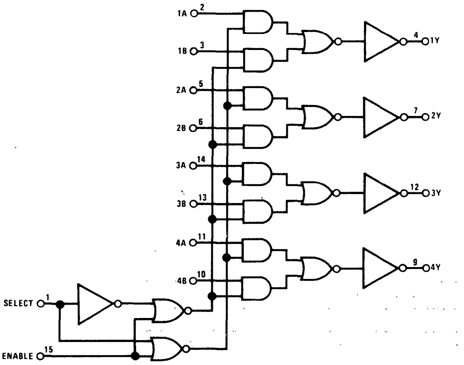
general description

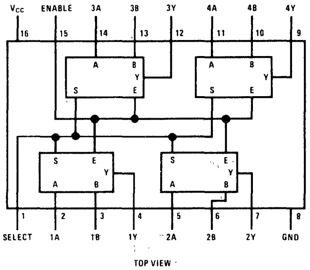
These multiplexers are monolithic complementary MOS (CMOS) integrated circuits constructed with N and P channel enhancement transistors. They consist of four 2-input multiplexers with a common select and enable inputs. When the enable input is at logical "0" the four outputs assume the values as selected from the inputs. When the enable input is at logical "1" the outputs assume logical "0." Select decoding is done internally resulting in a single select input only.

features

■ Supply voltage range	3V to 15V
■ High noise immunity	0.45 V_{CC} typ
■ Low power	50 nW (typ)
■ Tenth power TTL compatible	drive 2 LPTTL loads

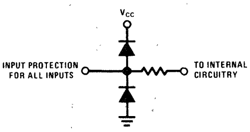
schematic and connection diagrams

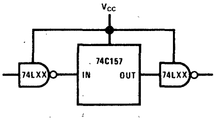




truth table

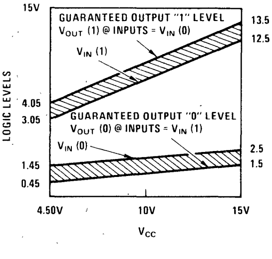
ENABLE	SELECT	A	B	OUTPUT Y
1	X	X	X	0
0	0	0	X	0
0	0	1	X	1
0	1	X	0	0
0	1	X	1	1





74L Compatibility

Guaranteed Noise Margin as a Function of V_{CC}



absolute maximum ratings

Voltage at Any Pin (Note 1)		$-0.3V$ to V_{CC} to 0.3V	Storage Temperature	$-65°C$ to 150°C
Operating Temperature	MM54C157	$-55°C$ to 125°C	Package Dissipation	500 nW
	MM74C157	$-40°C$ to +85°C	Lead Temperature (Soldering, 10 sec)	300°C
Maximum V_{CC} Voltage		16V	Operating V_{CC} Range	+3V to 15V

electrical characteristics

Min/Max limits apply across temperature range unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CMOS TO CMOS					
Logical "1" Input Voltage $V_{IN(1)}$	$V_{CC} = 5.0V$ $V_{CC} = 10.0V$	3.5 8			V V
Logical "0" Input Voltage $V_{IN(0)}$	$V_{CC} = 5.0V$ $V_{CC} = 10.0V$			1.5 2.0	V V
Logical "1" Output Voltage $V_{OUT(1)}$	$V_{CC} = 5.0V$ $V_{CC} = 10.0V$	4.5 9.0			V V
Logical "0" Output Voltage $V_{OUT(0)}$	$V_{CC} = 5.0V$ $V_{CC} = 10.0V$			0.5 1.0	V V
Logical "1" Input Current $I_{IN(1)}$	$V_{CC} = 15.0V$		0.005	1.0	μA
Logical "0" Input Current $I_{IN(0)}$	$V_{CC} = 15.0V$	-1.0	-0.005		μA
Supply Current I_{CC}	$V_{CC} = 15.0V$		0.050	60	μA
Input Capacitance	Any Input		5		pF
Propagation Delay from Data to Output (t_{pd0} or t_{pd1})	$V_{CC} = 5.0V$ $C_L = 50$ pF, $T_A = 25°C$ $V_{CC} = 10.0V$ $C_L = 50$ pF, $T_A = 25°C$		150 70	250 110	ns ns
Propagation Delay from Select to Output (t_{pd0} or t_{pd1})	$V_{CC} = 5.0V$ $C_L = 50$ pF, $T_A = 25°C$ $V_{CC} = 10.0V$ $C_L = 50$ pF, $T_A = 25°C$		180 80	300 130	ns ns
Propagation Delay from Enable to Output (t_{pd0})	$V_{CC} = 5.0V$ $C_L = 50$ pF, $T_A = 25°C$ $V_{CC} = 10.0V$ $C_L = 50$ pF, $T_A = 25°C$		180 80	300 130	ns ns
CMOS TO TENTH POWER INTERFACE					
Logical "1" Input Voltage $V_{IN(1)}$	54C $V_{CC} = 4.5V$ 74C $V_{CC} = 4.75V$	$V_{CC} - 1.5$			V
Logical "0" Input Voltage $V_{IN(0)}$	54C $V_{CC} = 4.5V$ 74C $V_{CC} = 4.75V$			0.8	V
Logical "1" Output Voltage $V_{OUT(1)}$	54C $V_{CC} = 4.5V$, $I_O = -360 \mu A$ 74C $V_{CC} = 4.75V$, $I_O = -360 \mu A$	2.4			V
Logical "0" Output Voltage $V_{OUT(0)}$	54C $V_{CC} = 4.5V$, $I_O = 360 \mu A$ 74C $V_{CC} = 4.75V$, $I_O = 360 \mu A$			0.4	V
Propagation Delay from Select to Output (t_{pd0} or t_{pd1})	$V_{CC} = 5.0V$ $C_L = 50$ pF, $T_A = 25°C$		250		ns

Note 1: This device should not be connected to circuits with the power on because high transient voltage may cause permanent damage.

MM54C160/MM74C160 decade counter with asynchronous clear
MM54C161/MM74C161 binary counter with asynchronous clear
MM54C162/MM74C162 decade counter with synchronous clear
MM54C163/MM74C163 binary counter with synchronous clear

general description

These (synchronous presettable up) counters are monolithic complementary MOS (CMOS) integrated circuits constructed with N and P channel enhancement mode transistors. They feature an internal carry lookahead for fast counting schemes and for cascading packages without additional gating.

A low level at the load input disables counting and causes the outputs to agree with the data input after the next positive clock edge. The clear function for the C162 and C163 is synchronous and a low level at the clear input sets all four outputs low after the next positive clock edge. The clear function for the C160 and C161 is asynchronous and a low level at the clear input sets all four outputs low regardless of the state of the clock.

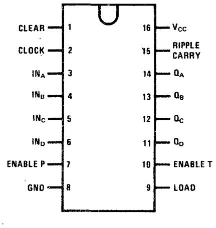
Counting is enabled when both count enable inputs are high. Input T is fed forward to also enable the carry out. The carry output is a positive pulse with a duration approximately equal to the positive portion of Q_A and can be used to enable successive cascaded stages. Logic transitions at the enable P or T inputs can occur when the clock is high or low.

features

■ High noise margin	1V guaranteed
■ High noise immunity	0.45 V_{CC} typ
■ Tenth power TTL compatible	drives 2 LPTTL loads
■ Wide supply voltage range	3V to 15V

- Internal look-ahead for fast counting scemes
- Carry output for N-bit cascading
- Load control line
- Synchronously programmable

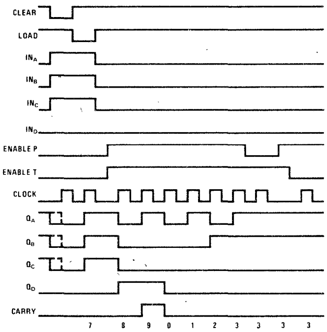
connection diagram



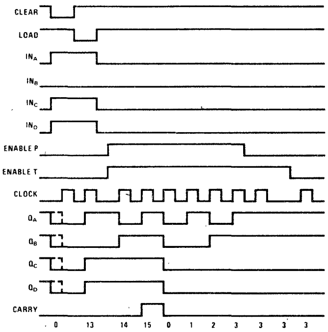
TOP VIEW

logic waveforms

C160, --- C162 Decade Counters



C161, --- C163 Binary Counters



absolute maximum ratings

Voltage at Any Pin (Note 1)	−0.3V to V_{CC} +0.3V
Operating Temperature MM54C160/1/2/3	−55°C to +125°C
MM74C160/1/2/3	−40°C to +85°C
Storage Temperature	−65°C to +150°C
Maximum V_{CC} Voltage	16V
Package Dissipation	500 mW
Operating V_{CC} Range	+3V to +15V
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics

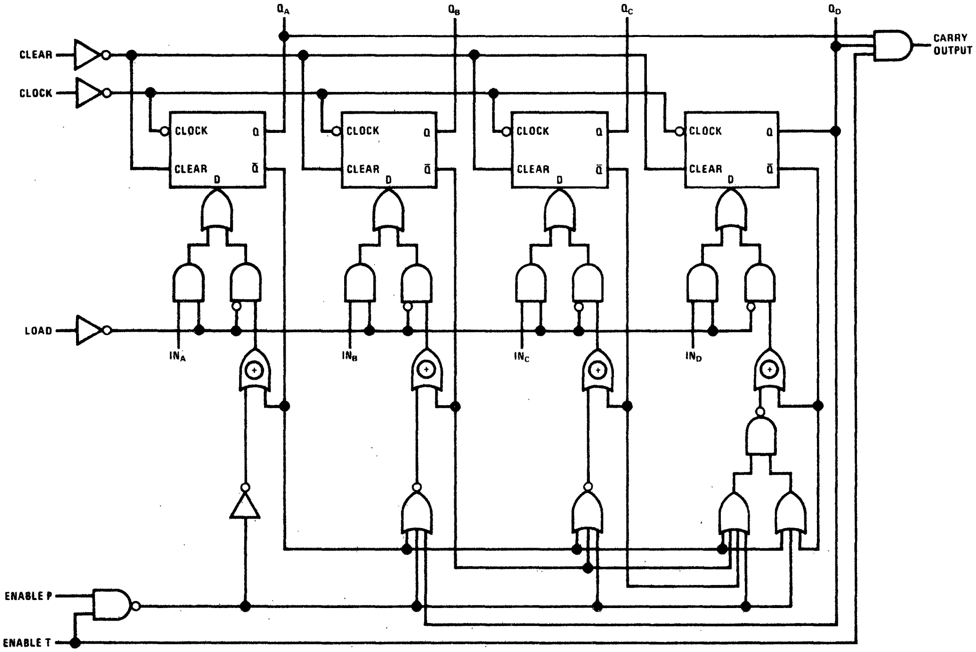
Min/Max limits apply across temperature range unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CMOS to CMOS					
Logical "1" Input Voltage $V_{IN(1)}$	V_{CC} = 5V	3.5			V
	V_{CC} = 10V	8.0			V
Logical "0" Input Voltage $V_{IN(0)}$	V_{CC} = 5V			1.5	V
	V_{CC} = 10V			2.0	V
Logical "1" Output Voltage $V_{OUT(1)}$	V_{CC} = 5V, I_O = −10 μA	4.5			V
	V_{CC} = 10V, I_O = −10 μA	9.0			V
Logical "0" Output Voltage $V_{OUT(0)}$	V_{CC} = 5V, I_O = +10 μA			0.5	V
	V_{CC} = 10V, I_O = +10 μA			1.0	V
Logical "1" Input Current $I_{IN(1)}$	V_{CC} = 15V, V_{IN} = 15V		0.005	1.0	μA
Logical "0" Input Current $I_{IN(0)}$	V_{CC} = 15V, V_{IN} = 0V	−1.0	−0.005		μA
Supply Current I_{CC}	V_{CC} = 15V		0.05	300	μA
Input Capacitance	Any Input		5		pF
Propagation delay time from clock to Q t_{pd0} or t_{pd1}	V_{CC} = 5V, C_L = 50 pF, T_A = 25°C		250	400	ns
	V_{CC} = 10V, C_L = 50 pF, T_A = 25°C		100	160	ns
Propagation delay time from clock to carry out t_{pd0} or t_{pd1}	V_{CC} = 5V, C_L = 50 pF, T_A = 25°C		290	450	ns
	V_{CC} = 10V, C_L = 50 pF, T_A = 25°C		120	190	ns
Propagation delay time from T enable to carry out t_{pd0} or t_{pd1}	V_{CC} = 5V, C_L = 50 pF, T_A = 25°C		180	290	ns
	V_{CC} = 10V, C_L = 50 pF, T_A = 25°C		70		ns
Propagation time from clear to Q (C162 and C163 only) t_{pd0}	V_{CC} = 5V, C_L = 50 pF, T_A = 25°C		190	300	ns
	V_{CC} = 10V, C_L = 50 pF, T_A = 25°C		80		ns
Time prior to clock that data or load must be present t_{SETUP}	V_{CC} = 5V, C_L = 50 pF, T_A = 25°C		120		ns
	V_{CC} = 10V, C_L = 50 pF, T_A = 25°C		30		ns
Time prior to clock that enable P or T must be present t_{SETUP}	V_{CC} = 5V, C_L = 50 pF, T_A = 25°C		170	280	ns
	V_{CC} = 10V, C_L = 50 pF, T_A = 25°C		70	120	ns
Time prior to clock that clear must be present (162, 163 only) t_{SETUP}	V_{CC} = 5V, C_L = 50 pF, T_A = 25°C		120	190	ns
	V_{CC} = 10V, C_L = 50 pF, T_A = 25°C		50	80	ns
Minimum clock pulses width t_{WL} or t_{WH}	V_{CC} = 5V, C_L = 50 pF, T_A = 25°C		90	170	ns
	V_{CC} = 10V, C_L = 50 pF, T_A = 25°C		35	70	ns
Maximum clock rise or fall time	V_{CC} = 5V, C_L = 50 pF, T_A = 25°C			15	μs
	V_{CC} = 10V, C_L = 50 pF, T_A = 25°C			5.0	μs
Maximum clock frequency	V_{CC} = 5V, C_L = 50 pF, T_A = 25°C	2.0	3.0		MHz
	V_{CC} = 10V, C_L = 50 pF, T_A = 25°C	5.5	8.5		MHz
CMOS/LPTTL INTERFACE					
Logical "1" Input Voltage	54C V_{CC} = 4.5V	V_{CC} − 1.5			V
	74C V_{CC} = 4.75V				
Logical "0" Input Voltage	54C V_{CC} = 4.5V			0.8	V
	74C V_{CC} = 4.75V				
Logical "1" Output Voltage	54C V_{CC} = 4.5V, I_O = −360 μA	2.4			V
	74C V_{CC} = 4.75V				
Logical "0" Output Voltage	54C V_{CC} = 4.5V, I_O = 360 μA				V
	74C V_{CC} = 4.75V			0.4	

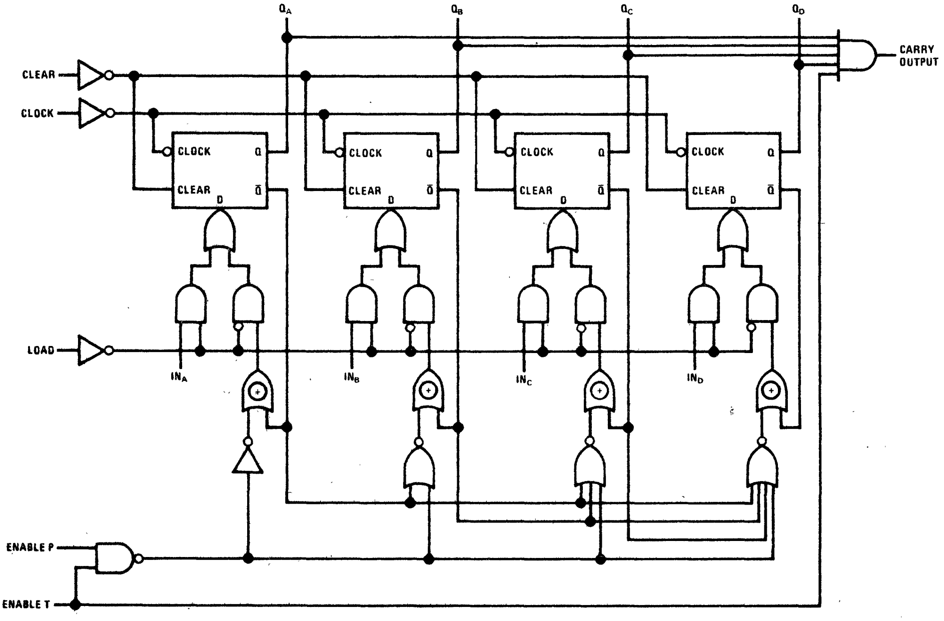
Note 1: This device should not be connected during power on conditions.

logic diagrams

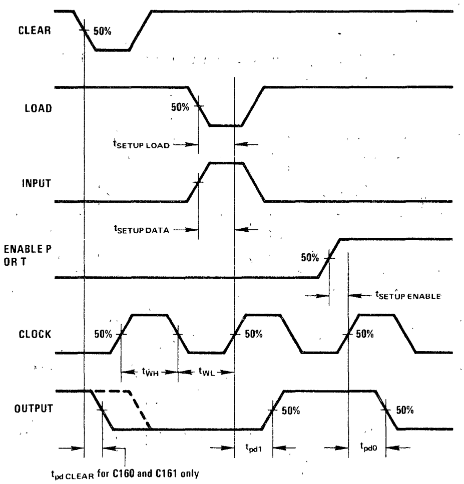
MM74C160, MM74C162; Clear is Synchronous for the MM74C162



MM74C161, MM74C163; Clear is Synchronous for the MM74C163



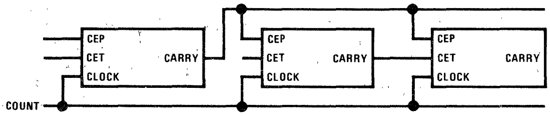
switching time waveforms



Note 1: All input pulses are from generators having the following characteristics: $t_r = t_f = 20$ ns PRR ≤ 1 MHz duty cycle $\leq 50\%$, $Z_{OUT} \approx 50\Omega$.

Note 2: All times are measured from 50% to 50%.

cascading packages



MM54C164/MM74C164

8-bit parallel-out serial shift register

general description

The MM54C164/MM74C164 shift registers are a monolithic complementary MOS (CMOS) integrated circuit constructed with N- and P-channel enhancement transistors. These 8-bit shift registers have gated serial inputs and clear. Each register bit is a D-type master/slave flip flop. A high-level input enables the other input which will then determine the state of the flip flop.

Data is serially shifted in and out of the 8-bit register during the positive going transition of clock pulse. Clear is independent of the clock and accomplished by a low level at the clear input. All inputs are protected against electrostatic effects.

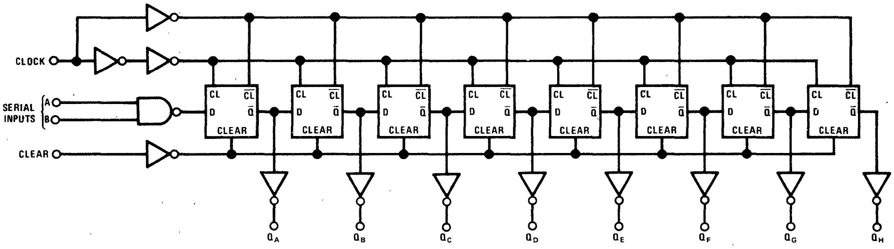
features

■ Supply voltage range	3V to 15V
■ Tenth power TTL compatible	drive 2 LPTTL loads
■ High noise immunity	0.45 V_{CC} typ
■ Low power	50 nW typ
■ Medium speed operation	8.0 MHz typ with 10V supply

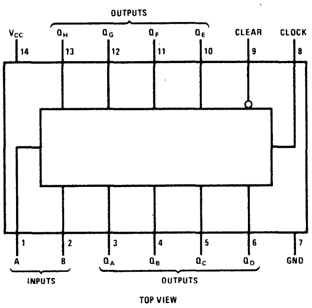
applications

- Data terminals
- Instrumentation
- Medical electronics
- Alarm systems
- Industrial electronics
- Remote meterly
- Computers

block diagram



connection diagram



truth table

Serial Inputs A and B

INPUTS t_n		OUTPUT t_{n+1}
A	B	Q_A
1	1	1
0	1	0
1	0	0
0	0	0

absolute maximum ratings

Voltage at Any Pin (Note 1)		$-0.3V$ to V_{CC} $+0.3V$
Operating Temperature	MM54C164	−55°C to +125°C
	MM74C164	−40°C to +85°C
Storage Temperature		−65°C to +150°C
Package Dissipation		500 mW
Maximum V_{CC} Voltage		16V
Operating V_{CC} Range		3V to 15V
Lead Temperature (Soldering, 10 sec)		300°C

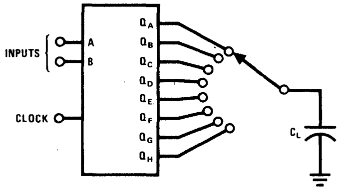
electrical characteristics

Min/max limits apply across temperature range unless otherwise specified.

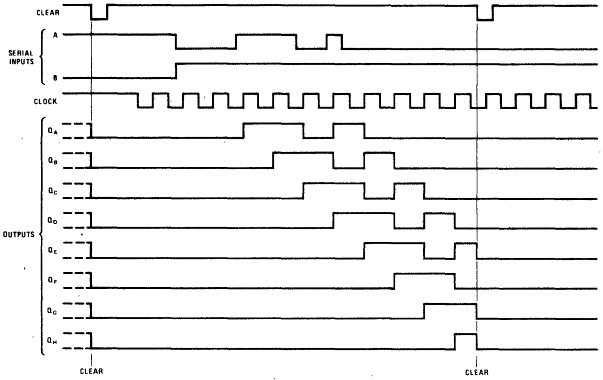
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CMOS TO CMOS					
Logical "1" Input Voltage $V_{IN(1)}$	V_{CC} = 5.0V V_{CC} = 10.0V	3.5 8			V V
Logical "0" Input Voltage $V_{IN(0)}$	V_{CC} = 5.0V V_{CC} = 10.0V			1.5 2	V V
Logical "1" Output Voltage $V_{OUT(1)}$	V_{CC} = 5.0V $I_O = -10\mu A$ V_{CC} = 10.0V $I_O = -10\mu A$	4.5 9.0			V V
Logical "0" Output Voltage $V_{OUT(0)}$	V_{CC} = 5.0V $I_O = -10\mu A$ V_{CC} = 10.0V $I_O = -10\mu A$			0.5 1	V V
Logical "1" Input Current $I_{IN(1)}$	V_{CC} = 15.0V V_{IN} = 15V		0.005	1	µA
Logical "0" Input Current $I_{IN(0)}$	V_{CC} = 15.0V V_{IN} = 0V	−1	-0.005		µA
Supply Current I_{CC}	V_{CC} = 15.0V		0.05	300	µA
Input Capacitance	Any Input		5		pF
Propagation Delay Time to a Logical "0" or Logical "1" From Clock to Q	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C V_{CC} = 10.0V, C_L = 50 pF, T_A = 25°C		230 90	310 120	ns ns
Propagation Delay Time to a Logical "1" From Clear to Q	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C V_{CC} = 10.0V, C_L = 50 pF, T_A = 25°C		280 110	380 150	ns ns
Time Prior to Clock Pulse That Data Must be Present t_{SETUP}	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C V_{CC} = 10.0V, C_L = 50 pF, T_A = 25°C		110 30		ns ns
Time After Clock Pulse That Data Must be Held	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C V_{CC} = 10.0V, C_L = 50 pF, T_A = 25°C		0 0		ns ns
Maximum Clock Frequency	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C V_{CC} = 10.0V, C_L = 50 pF, T_A = 25°C	2 5.5	3 8		MHz MHz
Minimum Clear Pulse Width	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C V_{CC} = 10.0V, C_L = 50 pF, T_A = 25°C		150 55		ns ns
Maximum Clock Rise and Fall Time	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C V_{CC} = 10.0V, C_L = 50 pF, T_A = 25°C	15 5			µs µs
CMOS TO TENTH POWER INTERFACE					
Logical "1" Input Voltage $V_{IN(1)}$	54C V_{CC} = 4.5V 74C V_{CC} = 4.75V	V_{CC}−1.5			V
Logical "0" Input Voltage $V_{IN(0)}$	54C V_{CC} = 4.5V 74C V_{CC} = 4.75V			0.8	V
Logical "1" Output Voltage $V_{OUT(1)}$	54C V_{CC} = 4.5V, $I_O = -360\mu A$ 74C V_{CC} = 4.75V, $I_O = -360\mu A$	2.4			V
Logical "0" Output Voltage $V_{OUT(0)}$	54C V_{CC} = 4.5V, $I_O = 360\mu A$ 74C V_{CC} = 4.75V, $I_O = 360\mu A$			0.4	V
Propagation Delay Time to a Logical "0" or Logical "1" From Clock To Q			320		ns

Note 1: These devices should not be connected under power on conditions.

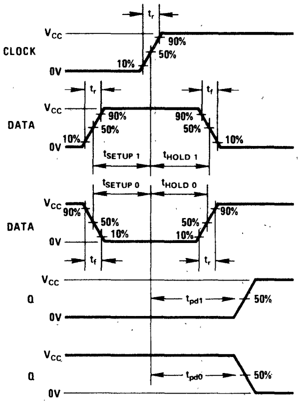
ac test circuit



switching time waveforms

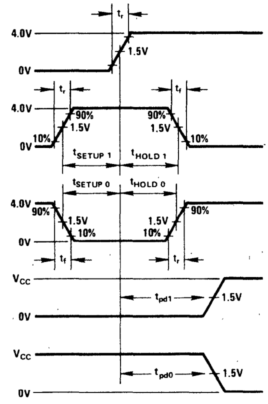


CMOS to CMOS



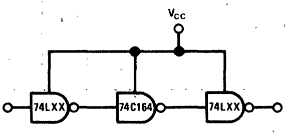
$t_r = t_f = 20$ ns

TTL to CMOS

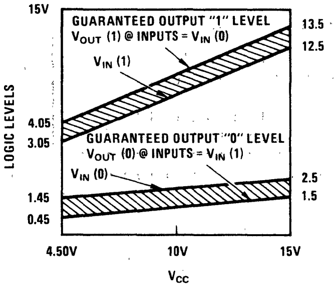


typical applications

74C Compatibility



Guaranteed Noise Margin as a Function of V_{CC}



MM54C165/MM74C165 parallel-load 8-bit shift register

general description

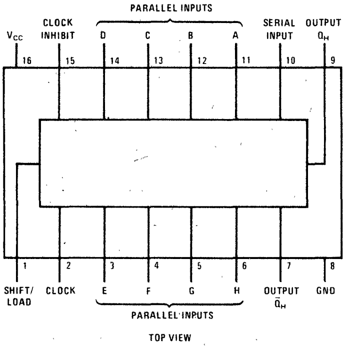
The MM54C165/MM74C165 is an 8-bit serial shift register which shifts data from Q_A to Q_H when clocked. Parallel inputs to each stage are enabled by a low level at the shift/load input. Also included is a gated clock input and a complementary output from the eighth-bit.

Clocking is accomplished through a 2-input NOR-gate permitting one input to be used as a clock-inhibit function. Holding either of the clock inputs high inhibits clocking, and holding either clock input low with the shift/load input high enables the other clock input. Data transfer occurs on the positive edge of the clock. The clock inhibit input should be changed to a high level only while the clock input is high. Parallel loading is inhibited as long as the shift/load input is high. When taken low, data at the parallel inputs is loaded directly into the register independent of the state of the clock.

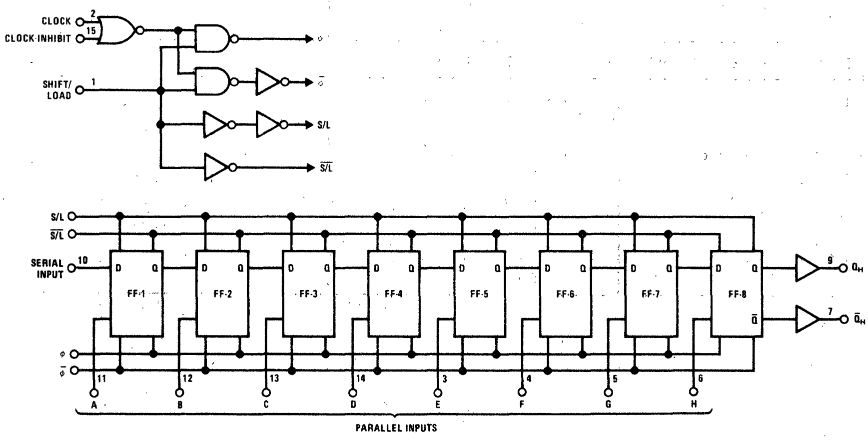
features

■ Wide supply voltage range	3.0V to 15V
■ Guaranteed noise margin	1.0V
■ High noise immunity	0.45 V_{CC} typ
■ Low power TTL compatibility	fan out of 2 driving 74L
■ Direct overriding load	
■ Gated clock inputs	
■ Fully static operation	

connection diagram



block diagram



absolute maximum ratings (Note 1)

Voltage at Any Pin	−0.3V to V_{CC} +0.3V
Operating Temperature Range	
MM54C165	−55°C to +125°C
MM74C165	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500 mW
Operating V_{CC} Range	3.0V to 15V
Absolute Maximum V_{CC}	16V
Lead Temperature (Soldering, 10 seconds)	300°C

dc electrical characteristics

Min/max limits apply across temperature range, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CMOS TO CMOS					
Logical "1" Input Voltage ($V_{IN(1)}$)	V_{CC} = 5.0V	3.5			V
	V_{CC} = 10V	8.0			V
Logical "0" Input Voltage ($V_{IN(0)}$)	V_{CC} = 5.0V			1.5	V
	V_{CC} = 10V			2.0	V
Logical "1" Output Voltage ($V_{OUT(1)}$)	V_{CC} = 5.0V, I_O = −10μA	4.5			V
	V_{CC} = 10V, I_O = −10μA	9.0			V
Logical "0" Output Voltage ($V_{OUT(0)}$)	V_{CC} = 5.0V, I_O = +10μA			0.5	V
	V_{CC} = 10V, I_O = +10μA			1.0	V
Logical "1" Input Current ($I_{IN(1)}$)	V_{CC} = 15V, V_{IN} = 15V		0.005	1.0	μA
Logical "0" Input Current ($I_{IN(0)}$)	V_{CC} = 15V, V_{IN} = 0V	−1.0	−0.005		μA
Supply Current (I_{CC})	V_{CC} = 15V		0.05	300	μA
CMOS/LPTTL INTERFACE					
Logical "1" Input Voltage ($V_{IN(1)}$)	54C, V_{CC} = 4.5V	V_{CC}−1.5			V
	74C, V_{CC} = 4.75V	V_{CC}−1.5			V
Logical "0" Input Voltage ($V_{IN(0)}$)	54C, V_{CC} = 4.5V			0.8	V
	74C, V_{CC} = 4.75V			0.8	V
Logical "1" Output Voltage ($V_{OUT(1)}$)	54C, V_{CC} = 4.5V, I_O = −360μA	2.4			V
	74C, V_{CC} = 4.75V, I_O = −360μA	2.4			V
Logical "0" Output Voltage ($V_{OUT(0)}$)	54C, V_{CC} = 4.5V, I_O = 360μA			0.4	V
	74C, V_{CC} = 4.75V, I_O = 360μA			0.4	V
OUTPUT DRIVE (See 54C/74C Family Characteristics Data Sheet)					
Output Source Current (I_{SOURCE}) (P-Channel)	V_{CC} = 5.0V, V_{OUT} = 0V, T_A = 25°C	−1.75	−3.3		mA
Output Source Current (I_{SOURCE}) (P-Channel)	V_{CC} = 10V, V_{OUT} = 0V, T_A = 25°C	−8.0	−15		mA
Output Sink Current (I_{SINK}) (N-Channel)	V_{CC} = 5.0V, V_{OUT} = V_{CC}, T_A = 25°C	1.75	3.6		mA
Output Sink Current (I_{SINK}) (N-Channel)	V_{CC} = 10V, V_{OUT} = V_{CC}, T_A = 25°C	8.0	16		mA

ac electrical characteristics $T_A = 25°C$, $C_L = 50$ pF, unless otherwise specified.

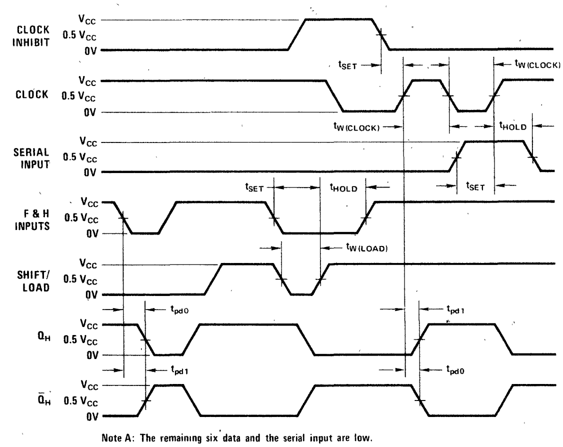
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Propagation Delay Time to a Logical "0" (t_{pd0}), or Logical "1" (t_{pd1}), from Clock or Load to Q or $\overline{Q}$	$V_{CC} = 5.0V$ $V_{CC} = 10V$		200 80	400 200	ns ns
Propagation Delay Time to a Logical "0" (t_{pd0}), or Logical "1" (t_{pd1}), from H to Q or $\overline{Q}$	$V_{CC} = 5.0V$ $V_{CC} = 10V$		200 80	400 200	ns ns
Clock Inhibit Set-up Time	$V_{CC} = 5.0V$ $V_{CC} = 10V$	150 60	75 30		ns ns
Serial Input Set-up Time	$V_{CC} = 5.0V$ $V_{CC} = 10V$	50 30	25 15		ns ns
Serial Input Hold Time	$V_{CC} = 5.0V$ $V_{CC} = 10V$	50 30	0 0		ns ns
Parallel Input Set-up Time	$V_{CC} = 5.0V$ $V_{CC} = 10V$	150 60	75 30		ns ns
Parallel Input Hold Time	$V_{CC} = 5.0V$ $V_{CC} = 10V$	50 30	0 0		ns ns
Minimum Clock Pulse Width	$V_{CC} = 5.0V$ $V_{CC} = 10V$		70 30	200 100	ns ns
Minimum Load Pulse Width	$V_{CC} = 5.0V$ $V_{CC} = 10V$		85 30	180 90	ns ns
Maximum Clock Frequency	$V_{CC} = 5.0V$ $V_{CC} = 10V$		6.0 12	2.5 5.0	MHz MHz
Maximum Clock Rise and Fall Time	$V_{CC} = 5.0V$ $V_{CC} = 10V$	10 5.0			µs µs
Input Capacitance (C_{IN})	(Note 2)		5.0		pF
Power Dissipation Capacitance (C_{pd})	(Note 3)		65		pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{pd} determines the no load ac power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note, AN-90.

switching time waveforms



Note A: The remaining six data and the serial input are low.
Note B: Prior to test, high level data is loaded into H input.

truth table

INPUTS					INTERNAL OUTPUTS		OUTPUT Q_H
SHIFT/ LOAD	CLOCK INHIBIT	CLOCK	SERIAL	PARALLEL A . . . H	Q_A	Q_B	
L	X	X	X	a . . . h	a	b	h
H	L	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	L	↑	H	X	H	Q_{An}	Q_{Gn}
H	L	↑	L	X	L	Q_{An}	Q_{Gn}
H	H	↑	X	X	Q_{A0}	Q_{B0}	Q_{H0}

H = $V_{IN(1)}$, L = $V_{IN(0)}$

X = irrelevant

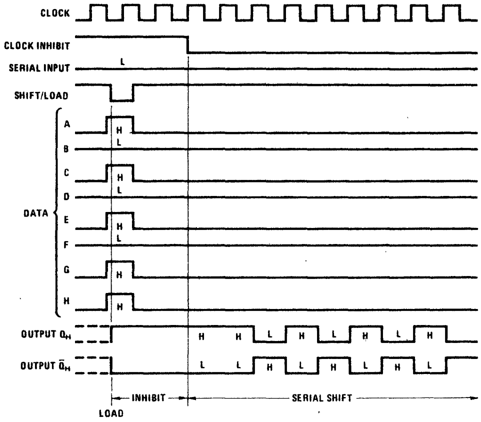
↑ = transition from $V_{IN(0)}$ to $V_{IN(1)}$

a . . . h = the level at data inputs A thru H

Q_{A0}, Q_{B0}, Q_{H0} = the level of Q_A, Q_B or Q_H, before the indicated input conditions were established

Q_{An}, Q_{6n} = the level of Q_A or Q_6 before the most recent ↑ transition of the clock

logic waveforms



MM54C173/MM74C173 TRI-STATE® quad D flip–flop

general description

The MM54C173/MM74C173 TRI-STATE quad D flip flop is a monolithic complementary MOS (CMOS) integrated circuit constructed with N and P-channel enhancement transistors. The four D type flip flops operate synchronously from a common clock. The TRI-STATE output allows the device to be used in bus organized systems. The outputs are placed in the TRI-STATE mode when either of the two output disable pins are in the logic "1" level. The input disable allows the flip flop to remain in their present states without disrupting the clock. If either of the two input disables are taken to a logic "1" level, the Q outputs are fed back to the inputs and in this manner the flip flops do not change state.

Clearing is enabled by taking the input to a logic "1" level. Clocking occurs on the positive going transition.

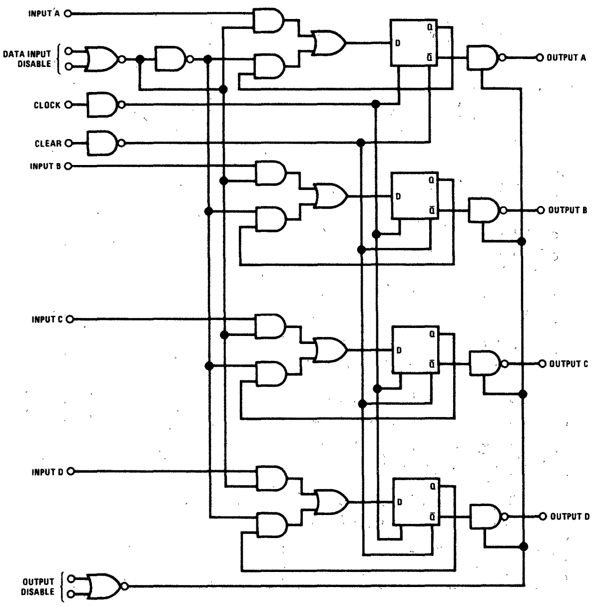
features

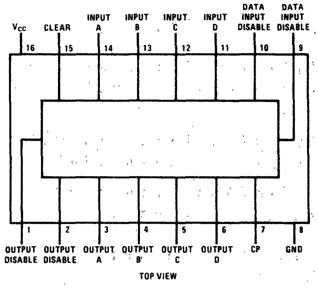
- Supply voltage range 3V to 15V
- Tenth power TTL compatible Drive 2 LPTTL loads
- High noise immunity $0.45\ V_{CC}$ typ
- Low power
- Medium speed operation
- High impedance TRI-STATE
- Input disabled without gating the clock

applications

- Automotive
- Data terminals
- Instrumentation
- Medical electronics
- Alarm systems
- Industrial electronics
- Remote metering
- Computers

logic and connection diagrams





absolute maximum ratings

Voltage at Any Pin (Note 1)		–0.3 to V_{CC} +0.3V
Operating Temperature	MM54C173	–55°C to +125°C
	MM74C173	–40°C to +85°C
Storage Temperature		–65°C to +150°C
Maximum V_{CC} Voltage		16V
Package Dissipation		500 mW
Operating V_{CC} Range		+3V to +15V
Lead Temperature (Soldering, 10 sec)		300°C

electrical characteristics

Min/max limits apply across temperature range unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CMOS TO CMOS					
Logical "1" Input Voltage $V_{IN(1)}$	V_{CC} = 5.0V	3.5			V
	V_{CC} = 10.0V	8			V
Logical "0" Input Voltage $V_{IN(0)}$	V_{CC} = 5.0V			1.5	V
	V_{CC} = 10.0V			2	V
Logical "1" Output Voltage $V_{OUT(1)}$	V_{CC} = 5.0V	4.5			V
	V_{CC} = 10.0V	9			V
Logical "0" Output Voltage $V_{OUT(0)}$	V_{CC} = 5.0V			0.5	V
	V_{CC} = 10.0V			1	V
Logical "1" Input Current $I_{IN(1)}$	V_{CC} = 15.0V		0.005	1	μA
Logical "0" Input Current $I_{IN(0)}$		–1	–0.005		μA
Output Current in High Impedance State	V_{CC} = 15V, V_O = 15V		0.001		μA
	V_O = 0V		0.001		μA
Supply Current I_{CC}	V_{CC} = 15V		0.05	300	μA
Input Capacitance	Any Input		5		pF
Propagation Delay Time to a Logical "0" (t_{pd0}) or Logical "1" (t_{pd1}) From Clock to Output	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C		220	400	ns
	V_{CC} = 10.0V, C_L = 50 pF, T_A = 25°C		80	200	ns
Input Data Setup Time, $t_{S\ DATA}$	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C		40	80	ns
	V_{CC} = 10.0V, C_L = 50 pF, T_A = 25°C		15	30	ns
Input Data Hold Time, $t_{H\ DATA}$	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C		0		ns
	V_{CC} = 10.0V, C_L = 50 pF, T_A = 25°C		0		ns
Input Disable Setup Time, $t_{S\ DISS}$	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C		100	200	ns
	V_{CC} = 10.0V, C_L = 50 pF, T_A = 25°C		35	70	ns
Input Disable Hold Time, $t_{H\ DISS}$	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C		0		ns
	V_{CC} = 10.0V, C_L = 50 pF, T_A = 25°C		0		ns
Delay From Output Disable to High Impedance State (From Logical "1" or Logical "0" Level), t_{IH}, t_{OH}	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C		170	340	ns
	V_{CC} = 10.0V, C_L = 50 pF, T_A = 25°C		70	140	ns
Delay From Output Disable to Logical "1" Level, t_{HI} (From High Impedance State)	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C		170	340	ns
	V_{CC} = 10.0V, C_L = 50 pF, T_A = 25°C		70	140	ns
Delay From Output Disable to Logical "0" Level, t_{HO} (From High Impedance State)	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C		170	340	ns
	V_{CC} = 10.0V, C_L = 50 pF, T_A = 25°C		70	140	ns
Propagation Delay From Clear to Output t_{pdR}	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C		240	490	ns
	V_{CC} = 10.0V, C_L = 50 pF, T_A = 25°C		90	180	
Maximum Clock Frequency	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C	3.0	4.0		MHz
	V_{CC} = 10.0V, C_L = 50 pF, T_A = 25°C	7	12		
Minimum Clear Pulse Width	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C		150		ns
	V_{CC} = 10.0V, C_L = 50 pF, T_A = 25°C		70		
Maximum Clock Rise and Fall Time	V_{CC} = 5.0V, C_L = 50 pF	10			μs
	V_{CC} = 10.0V, C_L = 50 pF	5			μs

Note 1: These devices should not be connected under "Power On" conditions.

electrical characteristics (con't)

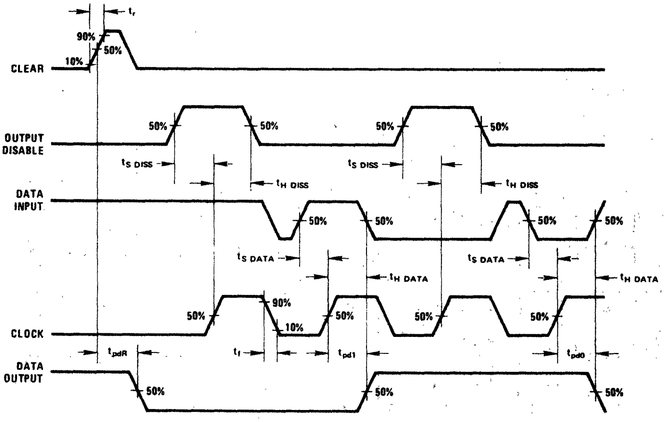
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
LOW POWER TTL/CMOS INTERFACE					
Logical "1" Input Voltage $V_{IN(1)}$	54C, V_{CC} = 4.5V 74C, V_{CC} = 4.75V	V_{CC}−1.5			V
Logical "0" Input Voltage $V_{IN(0)}$	54C, V_{CC} = 4.5V 74C, V_{CC} = 4.75V			.8	V
Logical "1" Output Voltage $V_{OUT(1)}$	54C, V_{CC} = 4.5V, I_O = −360μA 74C, V_{CC} = 4.75V, I_O = −360μA	2.4			V
Logical "0" Output Voltage $V_{OUT(0)}$	54C, V_{CC} = 4.5V, I_O = 360μA 74C, V_{CC} = 4.75V, I_O = 360μA			.4	V
Propagation Delay Time to a Logical "0", t_{pd0} or Logical "1" t_{pd1} From Clock	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C		500		ns

truth table

Truth Table (Both Output Disables Low)

t_n		t_{n+1}
DATA INPUT DISABLE	DATA INPUT	OUTPUT
Logic "1" on One or Both Inputs	X	Q_n
Logic "0" on Both Inputs	1	1
Logic "0" on Both Inputs	0	0

switching time waveforms



MM54C174/MM74C174 hex D flip-flop

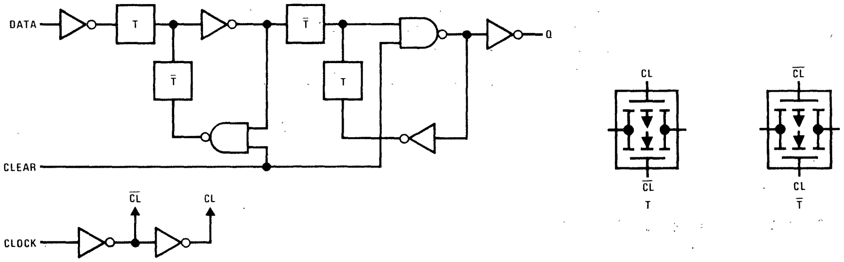
general description

The MM54C174/MM74C174 hex D flip-flop is a monolithic complementary MOS (CMOS) integrated circuit constructed with N- and P-channel enhancement transistors. All have a direct clear input. Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clear is independent of clock and accomplished by a low level at the clear input. All inputs are protected by diodes to V_{CC} and GND.

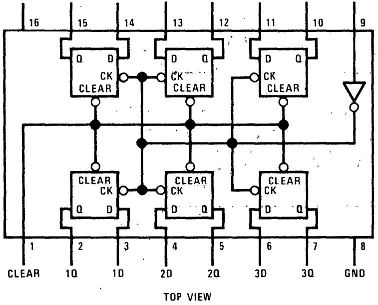
features

■ Wide supply voltage range	3.0V to 15V
■ Guaranteed noise margin	1.0V
■ High noise immunity	0.45 V_{CC} typ
■ Low power TTL compatibility	fan out of 2 driving 74L

logic diagram



connection diagram



truth table

INPUTS			OUTPUT
CLEAR	CLOCK	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q

absolute maximum ratings (Note 1)

Voltage at Any Pin	−0.3V to V_{CC} +0.3V
Operating Temperature Range	
MM54C174	−55°C to +125°C
MM74C174	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500 mW
Operating V_{CC} Range	3.0V to 15V
Absolute Maximum V_{CC}	16V
Lead Temperature (Soldering, 10 seconds)	300°C

dc electrical characteristics

Min/max limits apply across temperature range, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CMOS TO CMOS					
Logical "1" Input Voltage ($V_{IN(1)}$)	V_{CC} = 5.0V	3.5			V
	V_{CC} = 10V	8.0			V
Logical "0" Input Voltage ($V_{IN(0)}$)	V_{CC} = 5.0V			1.5	V
	V_{CC} = 10V			2.0	V
Logical "1" Output Voltage ($V_{OUT(1)}$)	V_{CC} = 5.0V, I_O = −10μA	4.5			V
	V_{CC} = 10V, I_O = −10μA	9.0			V
Logical "0" Output Voltage ($V_{OUT(0)}$)	V_{CC} = 5.0V, I_O = +10μA			0.5	V
	V_{CC} = 10V, I_O = +10μA			1.0	V
Logical "1" Input Current ($I_{IN(1)}$)	V_{CC} = 15V, V_{IN} = 15V		0.005	1.0	μA
Logical "0" Input Current ($I_{IN(0)}$)	V_{CC} = 15V, V_{IN} = 0V	−1.0	−0.005		μA
Supply Current (I_{CC})	V_{CC} = 15V		0.05	300	μA
CMOS/LPTTL INTERFACE					
Logical "1" Input Voltage ($V_{IN(1)}$)	54C, V_{CC} = 4.5V	V_{CC}−1.5			V
	74C, V_{CC} = 4.75V	V_{CC}−1.5			V
Logical "0" Input Voltage ($V_{IN(0)}$)	54C, V_{CC} = 4.5V			0.8	V
	74C, V_{CC} = 4.75V			0.8	V
Logical "1" Output Voltage ($V_{OUT(1)}$)	54C, V_{CC} = 4.5V, I_O = −360μA	2.4			V
	74C, V_{CC} = 4.75V, I_O = −360μA	2.4			V
Logical "0" Output Voltage ($V_{OUT(0)}$)	54C, V_{CC} = 4.5V, I_O = 360μA			0.4	V
	74C, V_{CC} = 4.75V, I_O = 360μA			0.4	V
OUTPUT DRIVE (See 54C/74C Family Characteristics Data Sheet)					
Output Source Current (I_{SOURCE}) (P-Channel)	V_{CC} = 5.0V, V_{OUT} = 0V, T_A = 25°C	−1.75	−3.3		mA
Output Source Current (I_{SOURCE}) (P-Channel)	V_{CC} = 10V, V_{OUT} = 0V, T_A = 25°C	−8.0	−15		mA
Output Sink Current (I_{SINK}) (N-Channel)	V_{CC} = 5.0V, V_{OUT} = V_{CC}, T_A = 25°C	1.75	3.6		mA
Output Sink Current (I_{SINK}) (N-Channel)	V_{CC} = 10V, V_{OUT} = V_{CC}, T_A = 25°C	8.0	16		mA

ac electrical characteristics $T_A = 25°C$, $C_L = 50$ pF, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Propagation Delay Time to a Logical "0" (t_{pd0}) or Logical "1" (t_{pd1}) from Clock to Q	$V_{CC} = 5.0V$ $V_{CC} = 10V$		150 70	300 110	ns ns
Propagation Delay Time to a Logical "0" from Clear	$V_{CC} = 5.0V$ $V_{CC} = 10V$		110 50	300 110	ns ns
Time Prior to Clock Pulse that Data Must be Present (t_{SETUP})	$V_{CC} = 5.0V$ $V_{CC} = 10V$	75 25			ns ns
Time After Clock Pulse that Data Must be Held (t_{HOLD})	$V_{CC} = 5.0V$ $V_{CC} = 10V$	75 25			ns ns
Minimum Clock Pulse Width	$V_{CC} = 5.0V$ $V_{CC} = 10V$		50 35		ns ns
Minimum Clear Pulse Width	$V_{CC} = 5.0V$ $V_{CC} = 10V$		65 35	140 70	ns ns
Maximum Clock Rise and Fall Time	$V_{CC} = 5.0V$ $V_{CC} = 10V$	15 5.0	>1200 >1200		μs μs
Maximum Clock Frequency	$V_{CC} = 5.0V$ $V_{CC} = 10V$	2.0 5.0	6.5 12		MHz MHz
Input Capacitance (C_{IN})	Clear Input (Note 2) Any Other Input		11 5.0		pF pF
Power Dissipation Capacitance (C_{pd})	Per Package (Note 3)		95		pF

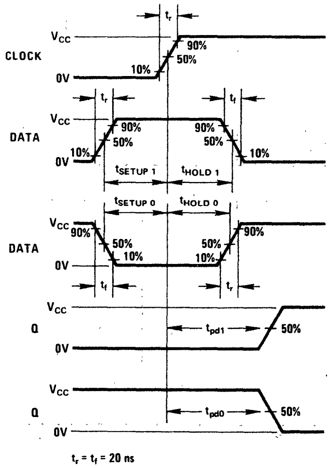
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{pd} determines the no load ac power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note, AN-90.

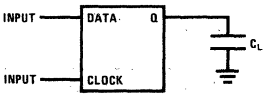
switching time waveforms

CMOS to CMOS



$t_r = t_f = 20$ ns

ac test circuit



MM54C175/MM74C175 quad D flip-flop

general description

The MM54C175/MM74C175 consists of four positive-edge-triggered D-type flip-flops implemented with monolithic CMOS technology. Both true and complemented outputs from each flip-flop are externally available. All four flip-flops are controlled by a common clock and a common clear. Information at the D inputs meeting the set-up time requirements is transferred to the Q outputs on the positive going edge of the clock pulse. The clearing operation, enabled by a negative pulse at Clear input, clears all four Q outputs to logical "0" and $\overline{Q}$'s to logical "1."

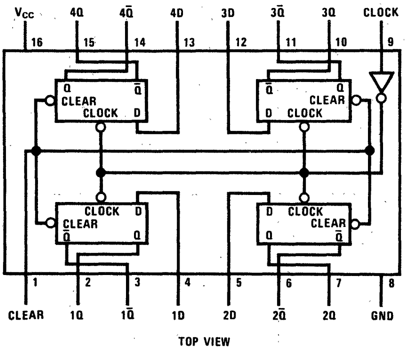
All inputs are protected from static discharge by diode clamps to V_{CC} and GND.

features

■ Wide supply voltage range	3.0V to 15V
■ Guaranteed noise margin	1.0V
■ High noise immunity	0.45 V_{CC} typ
■ Low power TTL compatibility	fan out of 2 driving 74L

---

connection diagram and truth table



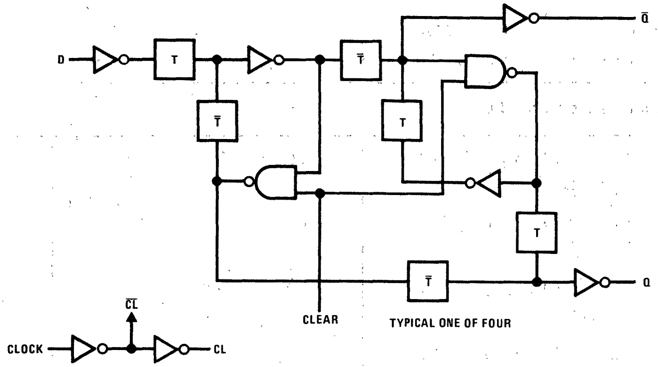
TOP VIEW

Each Flip-Flop

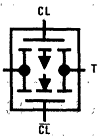
INPUTS			OUTPUTS	
CLEAR	CLOCK	D	Q	$\overline{Q}$
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	H	X	NC	NC
H	L	X	NC	NC

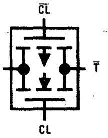
H = High level
L = Low level
X = Irrelevant
↑ = Transition from low to high level
NC = No change

logic diagrams



TYPICAL ONE OF FOUR





absolute maximum ratings (Note 1)

Voltage at Any Pin	−0.3V to V_{CC} +0.3V
Operating Temperature Range	
MM54C175	−55°C to +125°C
MM74C175	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500 mW
Operating V_{CC} Range	3.0V to 15V
Absolute Maximum V_{CC}	16V
Lead Temperature (Soldering, 10 seconds)	300°C

dc electrical characteristics

Min/max limits apply across temperature range, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CMOS TO CMOS					
Logical "1" Input Voltage ($V_{IN(1)}$)	V_{CC} = 5.0V V_{CC} = 10V	3.5 8.0			V V
Logical "0" Input Voltage ($V_{IN(0)}$)	V_{CC} = 5.0V V_{CC} = 10V			1.5 2.0	V V
Logical "1" Output Voltage ($V_{OUT(1)}$)	V_{CC} = 5.0V, I_O = −10μA V_{CC} = 10V, I_O = −10μA	4.5 9.0			V V
Logical "0" Output Voltage ($V_{OUT(0)}$)	V_{CC} = 5.0V, I_O = 10μA V_{CC} = 10V, I_O = 10μA			0.5 1.0	V V
Logical "1" Input Current ($I_{IN(1)}$)	V_{CC} = 15V, V_{IN} = 15V		0.005	1.0	μA
Logical "0" Input Current ($I_{IN(0)}$)	V_{CC} = 15V, V_{IN} = 0V	−1.0	−0.005		μA
Supply Current (I_{CC})	V_{CC} = 15V		0.05	300	μA
CMOS/LPTTL INTERFACE					
Logical "1" Input Voltage ($V_{IN(1)}$)					
MM54C175	V_{CC} = 4.5V	V_{CC}−1.5			V
MM74C175	V_{CC} = 4.75V	V_{CC}−1.5			V
Logical "0" Input Voltage ($V_{IN(0)}$)					
MM54C175	V_{CC} = 4.5V			0.8	V
MM74C175	V_{CC} = 4.75V			0.8	V
Logical "1" Output Voltage ($V_{OUT(1)}$)					
MM54C175	V_{CC} = 4.5V, I_O = −360μA	2.4			V
MM74C175	V_{CC} = 4.75V, I_O = −360μA	2.4			V
Logical "0" Output Voltage ($V_{OUT(0)}$)					
MM54C175	V_{CC} = 4.5V, I_O = 360μA			0.4	V
MM74C175	V_{CC} = 4.75V, I_O = 360μA			0.4	V
OUTPUT DRIVE (See 54C/74C Family Characteristics Data Sheet)					
Output Source Current (I_{SOURCE}) (P-Channel)	V_{CC} = 5.0V, V_{OUT} = 0V T_A = 25°C	−1.75	−3.3		mA
Output Source Current (I_{SOURCE}) (P-Channel)	V_{CC} = 10V, V_{OUT} = 0V T_A = 25°C	−8.0	−15		mA
Output Sink Current (I_{SINK}) (N-Channel)	V_{CC} = 5.0V, V_{OUT} = V_{CC} T_A = 25°C	1.75	3.6		mA
Output Sink Current (I_{SINK}) (N-Channel)	V_{CC} = 10V, V_{OUT} = V_{CC} T_A = 25°C	8.0	16		mA

ac electrical characteristics $T_A = 25°C$, $C_L = 50$ pF, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Propagation Delay Time to a Logical "0" (t_{pd0}) or Logical "1" (t_{pd1}) from Clock to Q or $\overline{Q}$	$V_{CC} = 5.0V$ $V_{CC} = 10V$		190 75	300 110	ns ns
Propagation Delay Time to a Logical "0" from Clear to Q	$V_{CC} = 5.0V$ $V_{CC} = 10V$		180 70	300 110	ns ns
Propagation Delay Time to a Logical "1" from Clear to $\overline{Q}$	$V_{CC} = 5.0V$ $V_{CC} = 10V$		230 90	400 150	ns ns
Time Prior to Clock Pulse that Data must be Present (t_{SET-UP})	$V_{CC} = 5.0V$ $V_{CC} = 10V$	100 40	45 16		ns ns
Time after Clock Pulse that Data must be Held (t_{HOLD})	$V_{CC} = 5.0V$ $V_{CC} = 10V$		−11 −4	0 0	ns ns
Minimum Clock Pulse Width	$V_{CC} = 5.0V$ $V_{CC} = 10V$		130 45	250 100	ns ns
Minimum Clear Pulse Width	$V_{CC} = 5.0V$ $V_{CC} = 10V$		120 45	250 100	ns ns
Maximum Clock Rise Time	$V_{CC} = 5.0V$ $V_{CC} = 10V$	15 5.0	450 125		µs µs
Maximum Clock Fall Time	$V_{CC} = 5.0V$ $V_{CC} = 10V$	15 5.0	50 50		µs µs
Maximum Clock Frequency	$V_{CC} = 5.0V$ $V_{CC} = 10V$	2.0 5.0	3.5 10		MHz MHz
Input Capacitance (C_{IN})	Clear Input (Note 2) Other Input		10 5.0		pF pF
Power Dissipation Capacitance (C_{pd})	Per Package (Note 3)		130		pF

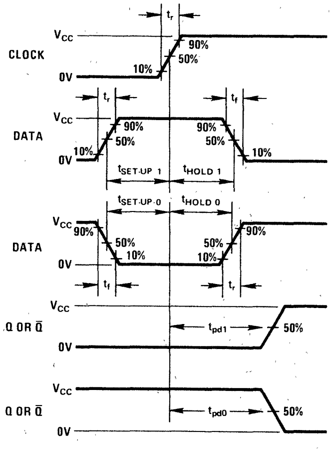
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note, AN-90.

switching time waveforms

CMOS to CMOS



$t_r = t_f = 20$ ns

MM54C192/MM74C192 synchronous 4-bit up/down decade counter
MM54C193/MM74C193 synchronous 4-bit up/down binary counter

general description

These up/down counters are monolithic complementary MOS (CMOS) integrated circuits. The MM54C192 and MM74C192 are BCD counters. While the MM54C193 and MM74C193 are binary counters.

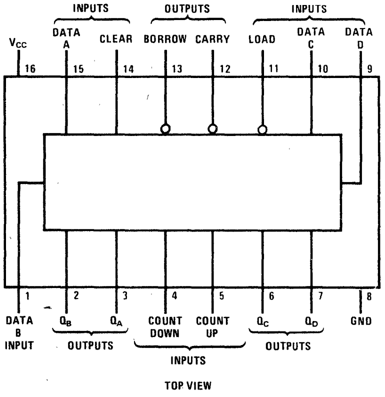
Counting up and counting down is performed by two count inputs, one being held high while the other is clocked. The outputs change on the positive going transition of this clock.

These counters feature preset inputs that are set when load is a logical "0" and a clear which forces all outputs to "0" when it is at logical "1." The counters also have carry and borrow outputs so that they can be cascaded using no external circuitry.

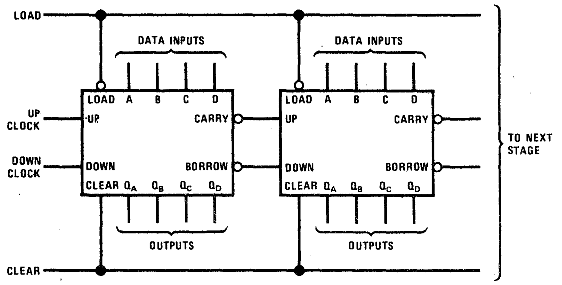
features

- High noise margin — 1V guaranteed
- Tenth power TTL compatible — drive 2 LPTTL loads
- Wide supply range — 3V to 15V
- Carry and borrow outputs for N-bit cascading
- Asynchronous clear
- High noise immunity — 0.45 V_{CC} typ

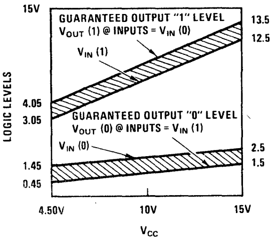
connection diagram



cascading packages



Guaranteed Noise Margin as A Function of V_{CC}



absolute maximum ratings

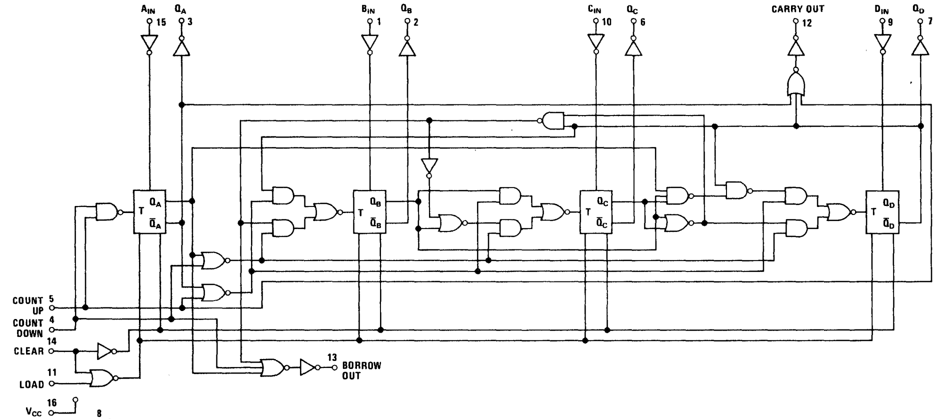
Voltage at Any Pin (Note 1)	$-0.3V$ to $V_{CC} + 0.3V$
Operating Temperature Range	
MM54C192, MM54C193	−55°C to +125°C
MM74C192, MM74C193	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Maximum V_{CC} Voltage	16V
Package Dissipation	500 mW
Operating V_{CC} Range	+3V to +15V
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics (Min/max limits apply across temperature range unless otherwise specified.)

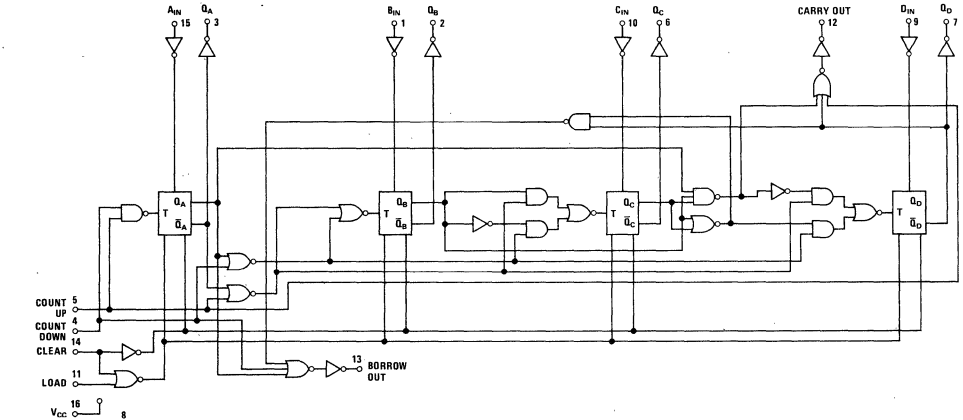
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CMOS TO MOS					
Logical "1" Input Voltage ($V_{IN(1)}$)	$V_{CC} = 5V$	3.5			V
	$V_{CC} = 10V$	8			V
Logical "0" Input Voltage ($V_{IN(0)}$)	$V_{CC} = 5V$			1.5	V
	$V_{CC} = 10V$			2	V
Logical "1" Output Voltage ($V_{OUT(1)}$)	$V_{CC} = 5V$, $I_O = -10\mu A$	4.5			V
	$V_{CC} = 10V$, $I_O = -10\mu A$	9			V
Logical "0" Output Voltage ($V_{OUT(0)}$)	$V_{CC} = 5V$, $I_O = +10\mu A$			0.5	V
	$V_{CC} = 10V$, $I_O = +10\mu A$			1	V
Logical "1" Input Current ($I_{IN(1)}$)	$V_{CC} = 15V$, $V_{IN} = 15V$		0.005	1.0	µA
Logical "0" Input Current ($I_{IN(0)}$)	$V_{CC} = 15V$, $V_{IN} = 0V$	−1.0	−0.005		µA
Supply Current (I_{CC})	$V_{CC} = 15V$		0.05	300	µA
Input Capacitance	Any Input		5		pF
Propagation Delay Time to Q From Count Up or Down (t_{pd0} or t_{pd1})	$V_{CC} = 5V$, $C_L = 50$ pF, $T_A = 25°C$		250	400	ns
	$V_{CC} = 10V$, $C_L = 50$ pF, $T_A = 25°C$		100	160	ns
Propagation Delay Time to Borrow From Count Down (t_{pd0} or t_{pd1})	$V_{CC} = 5V$, $C_L = 50$ pF, $T_A = 25°C$		120	200	ns
	$V_{CC} = 10V$, $C_L = 50$ pF, $T_A = 25°C$		50	80	ns
Propagation Delay Time to Carry From Count Up (t_{pd0} or t_{pd1})	$V_{CC} = 5V$, $C_L = 50$ pF, $T_A = 25°C$		120	200	ns
	$V_{CC} = 10V$, $C_L = 50$ pF, $T_A = 25°C$		50	80	ns
Time Prior to Load That Data Must be Present (t_{SETUP})	$V_{CC} = 5V$, $C_L = 50$ pF, $T_A = 25°C$		100	160	ns
	$V_{CC} = 10V$, $C_L = 50$ pF, $T_A = 25°C$		30	50	ns
Minimum Clear Pulse Width	$V_{CC} = 5V$, $C_L = 50$ pF, $T_A = 25°C$		300	480	ns
	$V_{CC} = 10V$, $C_L = 50$ pF, $T_A = 25°C$		120	190	ns
Minimum Load Pulse Width	$V_{CC} = 5V$, $C_L = 50$ pF, $T_A = 25°C$		100	160	ns
	$V_{CC} = 10V$, $C_L = 50$ pF, $T_A = 25°C$		40	65	ns
Propagation Delay Time to Q From Load (t_{pd0} or t_{pd1})	$V_{CC} = 5V$, $C_L = 50$ pF, $T_A = 25°C$		300	480	ns
	$V_{CC} = 10V$, $C_L = 50$ pF, $T_A = 25°C$		120	190	ns
Minimum Count Pulse Width	$V_{CC} = 5V$, $C_L = 50$ pF, $T_A = 25°C$		120	200	ns
	$V_{CC} = 10V$, $C_L = 50$ pF, $T_A = 25°C$		35	80	ns
Maximum Count Frequency	$V_{CC} = 5V$, $C_L = 50$ pF, $T_A = 25°C$	2.5	4		MHz
	$V_{CC} = 10V$, $C_L = 50$ pF, $T_A = 25°C$	6	10		MHz
Count Rise and Fall Time	$V_{CC} = 5V$, $C_L = 50$ pF, $T_A = 25°C$			15	µs
	$V_{CC} = 10V$, $C_L = 50$ pF, $T_A = 25°C$			5	µs
CMOS TO TENTH POWER INTERFACE					
Logical "1" Input Voltage ($V_{IN(1)}$)	54C $V_{CC} = 4.5V$	$V_{CC}-1.5$			V
	74C $V_{CC} = 4.75V$	$V_{CC}-1.5$			V
Logical "0" Input Voltage ($V_{IN(0)}$)	54C $V_{CC} = 4.5V$			0.8	V
	74C $V_{CC} = 4.75V$			0.8	V
Logical "1" Output Voltage ($V_{OUT(1)}$)	54C $V_{CC} = 4.5V$, $I_O = -100\mu A$	2.4			V
	74C $V_{CC} = 4.75V$, $I_O = -100\mu A$	2.4			V
Logical "0" Output Voltage ($V_{OUT(0)}$)	54C $V_{CC} = 4.5V$, $I_O = 360\mu A$			0.4	V
	74C $V_{CC} = 4.75V$, $I_O = 360\mu A$			0.4	V

Note 1: This device should not be connected to circuits with the power on because high transient voltage may cause permanent damage.

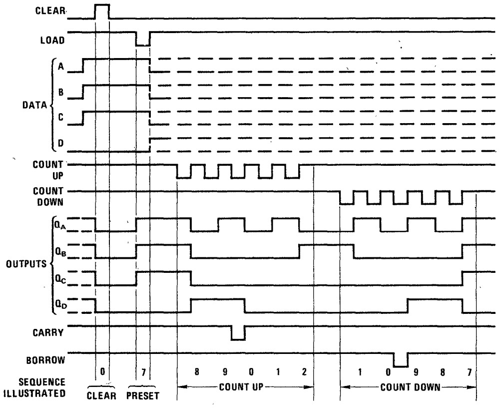
schematic diagrams



MM54C192 Synchronous 4-Bit Up/Down Decade Counter

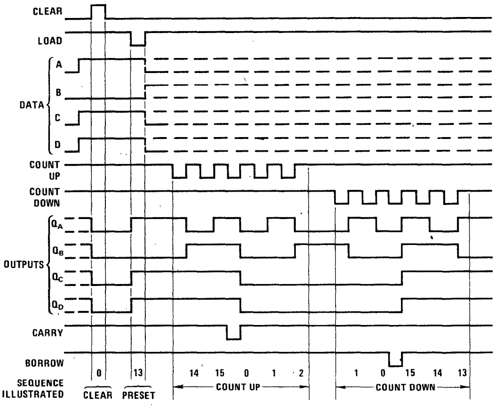


MM54C193 Synchronous 4-Bit Up/Down Binary Counter



Note 1: Clear outputs to zero.
Note 2: Load (preset) to BCD seven.
Note 3: Count up to eight, nine, carry, zero, one, and two.
Note 4: Count down to one, zero, borrow, nine, eight, and seven.

MM54C192/MM74C192



Note 1: Clear outputs to zero.
Note 2: Load (preset) to binary thirteen.
Note 3: Count up to fourteen, fifteen, carry, zero, one, and two.
Note 4: Count down to one, zero, borrow, fifteen, fourteen, and thirteen.

MM54C193/MM74C193

NOTE A: CLEAR OVERRIDES LOAD, DATA, AND COUNT INPUTS.
NOTE B: WHEN COUNTING UP, COUNT DOWN INPUT MUST BE HIGH; WHEN COUNTING DOWN, COUNT-UP INPUT MUST BE HIGH.

MM54C195/MM74C195 4-bit registers

general description

The MM54C195/MM74C195 CMOS 4-bit registers feature parallel inputs, parallel outputs, J-K serial inputs, shift/load control input and a direct overriding clear. The following two modes of operation are possible.

Parallel Load
Shift in direction Q_A towards Q_D

Parallel loading is accomplished by applying the four bits of data and taking the shift/load control input low. The data is loaded into the associated flip-flops and appears at the outputs after the positive transition of the clock input. During parallel loading, serial data flow is inhibited.

Serial shifting is accomplished synchronously when the shift/load control input is high. Serial data for this mode is entered at the J-$\overline{K}$ inputs. These inputs allow the first stage to perform as a J-$\overline{K}$, D or T-type flip flop as shown in the truth table.

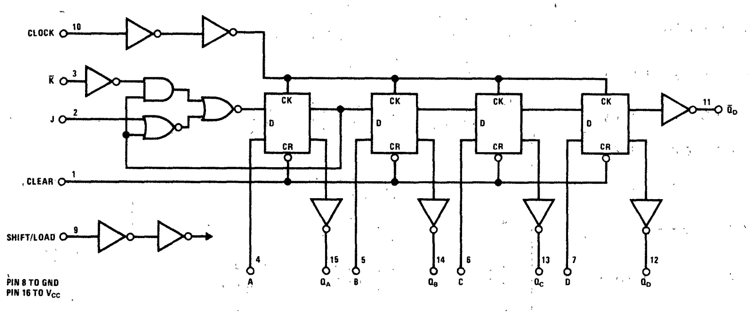
features

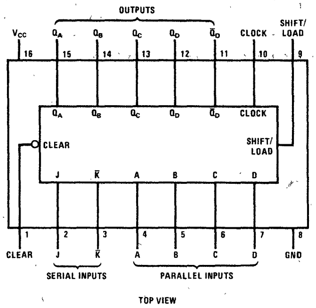
- Medium speed operation 8.5 MHz (typ) with 10V supply and 50 pF load
- High noise immunity 0.45 V_{CC} (typ)
- Low power 100 nW (typ)
- Tenth power TTL compatible drive 2 LPTTL loads
- Supply voltage range 3V to 15V
- Synchronous parallel load
- Parallel inputs and outputs from each flip-flop
- Direct overriding clear
- J and $\overline{K}$ inputs to first stage
- Complementary outputs from last stage
- Positive edge triggered clocking
- Diode clamped inputs to protect against static charge

applications

- Automotive
- Data terminals
- Instrumentation
- Medical electronics
- Alarm systems
- Remote metering
- Industrial electronics
- Computers

schematic and connection diagrams





absolute maximum ratings

Voltage at Any Pin (Note 1)		$-0.3V$ to V_{CC} $+0.3V$
Operating Temperature	MM54C195	−55°C to +125°C
	MM74C195	−40°C to +85°C
Storage Temperature		−65°C to 150°C
Maximum V_{CC} Voltage		16V
Package Dissipation		500 mW
Lead Temperature (Soldering, 10 sec)		300°C
Operating V_{CC} Range		+3V to +15V

electrical characteristics

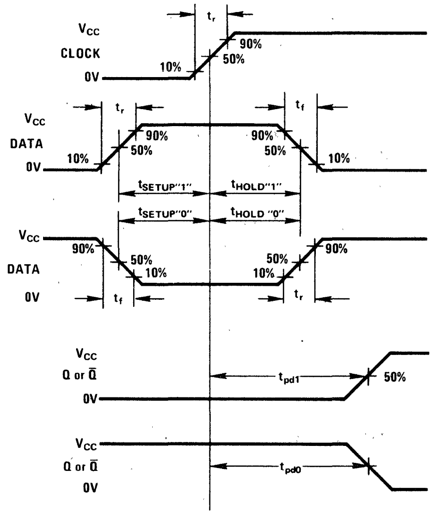
Max/Min limits apply across temperature range unless otherwise specified.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
CMOS TO CMOS						
Logical "1" Input Voltage $V_{IN(1)}$	V_{CC} = 5.0V		3.5			V
	V_{CC} = 10.0V		8.0			V
Logical "0" Input Voltage $V_{IN(0)}$	V_{CC} = 5.0V				1.5	V
	V_{CC} = 10.0V				2.0	V
Logical "1" Output Voltage $V_{OUT(1)}$	V_{CC} = 5.0V		4.5			V
	V_{CC} = 10.0V		9.0			V
Logical "0" Output Voltage $V_{OUT(0)}$	V_{CC} = 5.0V				0.5	V
	V_{CC} = 10.0V				1.0	V
Logical "1" Input Current $I_{IN(1)}$	V_{CC} = 15.0V			0.005	1.0	µA
Logical "0" Input Current $I_{IN(0)}$	V_{CC} = 15.0V		−1.0	−0.005		µA
Supply Current I_{CC}	V_{CC} = 15.0V			0.050	300	µA
Input Capacitance	Any Input			5.0		pF
Propagation Delay Time to a Logical "0" t_{pd0} or Logical "1" t_{pd1} from Clock to Q or $\overline{Q}$	V_{CC} = 5.0V	C_L = 50 pF, T_A = 25°C		150	300	ns
	V_{CC} = 10.0V	C_L = 50 pF, T_A = 25°C		75	130	ns
Propagation Delay Time to a Logical "0" or Logical "1" From Clear to Q or $\overline{Q}$	V_{CC} = 5.0V	C_L = 50 pF, T_A = 25°C		150	300	ns
	V_{CC} = 10.0V	C_L = 50 pF, T_A = 25°C		50	130	ns
Time Prior to Clock Pulse That Data Must be Present t_{SETUP}	V_{CC} = 5.0V	C_L = 50 pF, T_A = 25°C		80	200	ns
	V_{CC} = 10.0V	C_L = 50 pF, T_A = 25°C		35	70	ns
Time Prior to Clock Pulse That Shift/Load Must be Present t_{SETUP}	V_{CC} = 5.0V	C_L = 50 pF, T_A = 25°C		110	150	ns
	V_{CC} = 10.0V	C_L = 50 pF, T_A = 25°C		60	90	ns
Time After Clock Pulse That Data Must be Held	V_{CC} = 5.0V	C_L = 50 pF, T_A = 25°C		−10	0	ns
	V_{CC} = 10.0V	C_L = 50 pF, T_A = 25°C		−5	0	ns
Minimum Clock Pulse Width (t_{WL} = t_{WH})	V_{CC} = 5.0V	C_L = 50 pF, T_A = 25°C		100	200	ns
	V_{CC} = 10.0V	C_L = 50 pF, T_A = 25°C		50	100	ns
Minimum Clear Pulse Width	V_{CC} = 5.0V	C_L = 50 pF, T_A = 25°C		90	130	ns
	V_{CC} = 10V	C_L = 50 pF, T_A = 25°C		40	60	ns
Maximum Clock Rise and Fall Time	V_{CC} = 5.0V	C_L = 50 pF	5.0			µs
	V_{CC} = 10.0V	C_L = 50 pF	2.0			µs
Maximum Input Clock Frequency	V_{CC} = 5.0V	C_L = 50 pF, T_A = 25°C	2.0	3.0		MHz
	V_{CC} = 10.0V	C_L = 50 pF, T_A = 25°C	5.5	8.5		MHz
LOW POWER TTL/CMOS INTERFACE						
Logical "1" Input Voltage $V_{IN(1)}$	54C	V_{CC} = 4.5V	V_{CC}-1.5			V
	74C	V_{CC} = 4.75V				
Logical "0" Input Voltage $V_{IN(0)}$	54C	V_{CC} = 4.5V			0.8	V
	74C	V_{CC} = 4.75V				
Logical "1" Output Voltage $V_{OUT(1)}$	54C	V_{CC} = 4.5V, I_D = −360 µA	2.4			V
	74C	V_{CC} = 4.75V, I_D = −360 µA				
Logical "0" Output Voltage $V_{OUT(0)}$	54C	V_{CC} = 4.5V, I_D = 360 µA			0.4	V
	74C	V_{CC} = 4.75V, I_D = 360 µA				

Note: These devices should not be connected under power on condition.

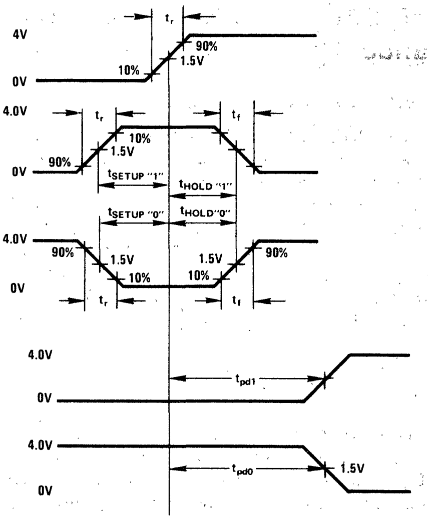
switching time waveforms

CMOS to CMOS



$t_r = t_f = 20$ ns

TTL to CMOS



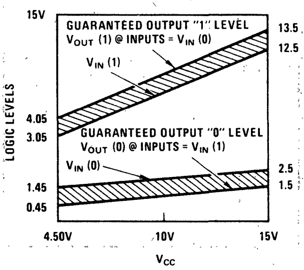
$t_r = t_f = 20$ ns

truth table

INPUTS AT t_n		OUTPUTS AT t_{n+1}				
J	$\overline{K}$	Q_A	Q_B	Q_C	Q_D	$\overline{Q}_D$
L	H	Q_{An}	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
L	L	L	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	H	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	L	$\overline{Q}_{An}$	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$

Note: H = HIGH LEVEL, L = LOW LEVEL
t_n = bit time before clock pulse
t_{n+1} = bit time after clock pulse
Q_{An} = State of Q_A at t_n

Guaranteed noise Margin as a Function of V_{CC}



MM54C200/MM74C200 256-bit TRI-STATE® random access read/write memory

general description

The MM54C200/MM74C200 is a 256-bit random access read/write memory. Inputs consist of eight address lines, a data input line, a $\overline{\text{write enable}}$ line, and three chip enables. The eight binary address inputs are decoded internally to select each of the 256 locations. An internal address register, latches and address information on the positive to negative edge of $\overline{CE}_3$. The TRI-STATE data output line working in conjunction with $\overline{CE}_1$ or $\overline{CE}_2$ inputs provides for easy memory expansion.

Address Operation: Address inputs must be stable t_{SA} prior to the positive to negative transition of $\overline{CE}_3$. It is thus not necessary to hold address information stable for more than t_{HA} after the memory is enabled (positive to negative transition).

Note: The timing is different than the DM74200 in that a positive to negative transition of the $\overline{\text{memory enable}}$ must occur for the memory to be selected.

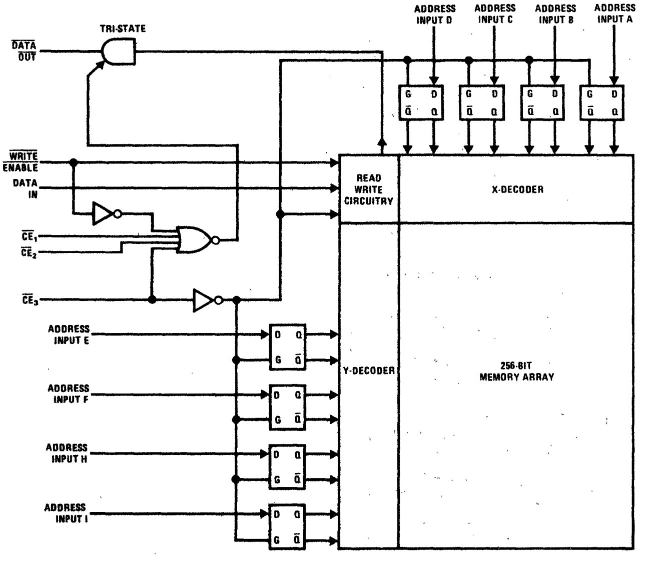
Read Operation: The data is read out by selecting the proper address and bringing $\overline{CE}_3$ low and $\overline{\text{write enable}}$ high. Holding $\overline{CE}_1$ or $\overline{CE}_2$ or $\overline{CE}_3$ at a high level forces the output into TRI-STATE. When used in bus organized systems, $\overline{CE}_1$, or $\overline{CE}_2$, a TRI-STATE control, provides for fast access times by not totally disabling the chip.

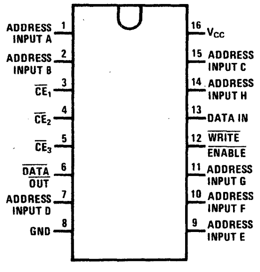
Write Operation: Data is written into the memory with $\overline{CE}_3$ low and $\overline{\text{write enable}}$ low. The state of $\overline{CE}_1$ or $\overline{CE}_2$ has no effect on the write cycle. The output assumes TRI-STATE with $\overline{\text{write enable}}$ low.

features

■ Wide supply voltage range	3.0V to 15V
■ Guaranteed noise margin	1.0V
■ High noise immunity	0.45 V_{CC} typ
■ TTL compatibility	fan out of 1 driving standard TTL
■ Low power	500 nW typ
■ Internal address register	

logic and connection diagrams





TOP VIEW

absolute maximum ratings (Note 1)

Voltage at Any Pin	$-0.3V$ to V_{CC} $+0.3V$
Operating Temperature Range	
MM54C200	$-55°C$ to $+125°C$
MM74C200	$-40°C$ to $+85°C$
Storage Temperature Range	$-65°C$ to $+150°C$
Package Dissipation	500 mW
Operating V_{CC} Range	3.0V to 15V
Absolute Maximum V_{CC}	16V
Lead Temperature (Soldering, 10 seconds)	300°C

dc electrical characteristics

Min/max limits apply across temperature range, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CMOS TO CMOS					
Logical "1" Input Voltage ($V_{IN(1)}$)	$V_{CC} = 5.0V$ $V_{CC} = 10V$	3.5 8.0			V V
Logical "0" Input Voltage ($V_{IN(0)}$)	$V_{CC} = 5.0V$ $V_{CC} = 10V$			1.5 2.0	V V
Logical "1" Output Voltage ($V_{OUT(1)}$)	$V_{CC} = 5.0V$, $I_O = -10\mu A$ $V_{CC} = 10V$, $I_O = -10\mu A$	4.5 9.0			V V
Logical "0" Output Voltage ($V_{OUT(0)}$)	$V_{CC} = 5.0V$, $I_O = +10\mu A$ $V_{CC} = 10V$, $I_O = +10\mu A$			0.5 1.0	V V
Logical "1" Input Current ($I_{IN(1)}$)	$V_{CC} = 15V$, $V_{IN} = 15V$		0.005	1.0	μA
Logical "0" Input Current ($I_{IN(0)}$)	$V_{CC} = 15V$, $V_{IN} = 0V$	-1.0	-0.005		μA
Supply Current (I_{CC})	$V_{CC} = 15V$		0.10		μA
CMOS/LPTTL INTERFACE					
Logical "1" Input Voltage ($V_{IN(1)}$)	54C, $V_{CC} = 4.5V$ 74C, $V_{CC} = 4.75V$	$V_{CC} - 1.5$ $V_{CC} - 1.5$			V V
Logical "0" Input Voltage ($V_{IN(0)}$)	54C, $V_{CC} = 4.5V$ 74C, $V_{CC} = 4.75V$			0.8 0.8	V V
Logical "1" Output Voltage ($V_{OUT(1)}$)	54C, $V_{CC} = 4.5V$, $I_O = -1.6$ mA 74C, $V_{CC} = 4.75V$, $I_O = -1.6$ mA	2.4 2.4			V V
Logical "0" Output Voltage ($V_{OUT(0)}$)	54C, $V_{CC} = 4.5V$, $I_O = 1.6$ mA 74C, $V_{CC} = 4.75V$, $I_O = 1.6$ mA			0.4 0.4	V V
OUTPUT DRIVE (See 54C/74C Family Characteristics Data Sheet)					
Output Source Current (I_{SOURCE}) (P-Channel)	$V_{CC} = 5.0V$, $V_{OUT} = 0V$ $T_A = 25°C$	-4.0	-6.0		mA
Output Source Current (I_{SOURCE}) (P-Channel)	$V_{CC} = 10V$, $V_{OUT} = 0V$ $T_A = 25°C$	-16.0	-25		mA
Output Sink Current (I_{SINK}) (N-Channel)	$V_{CC} = 5.0V$, $V_{OUT} = V_{CC}$ $T_A = 25°C$	5.0	8.0		mA
Output Sink Current (I_{SINK}) (N-Channel)	$V_{CC} = 10V$, $V_{OUT} = V_{CC}$ $T_A = 25°C$	20.0	30		mA

ac electrical characteristics $T_A = 25°C$, $C_L = 50$ pF, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Access Time From Address (t_{ACC})	$V_{CC} = 5.0V$ $V_{CC} = 10V$		450 200	900 400	ns ns
Propagation Delay From $\overline{CE}_3$ (t_{pd})	$V_{CC} = 5.0V$ $V_{CC} = 10V$		360 120	700 300	ns ns
Propagation Delay From $\overline{CE}_1$ or $\overline{CE}_2$ ($t_{p\overline{CE}1}$)	$V_{CC} = 5.0V$ $V_{CC} = 10V$		250 85	500 200	ns ns
Address Setup Time (t_{SA})	$V_{CC} = 5.0V$ $V_{CC} = 10V$	200 100	80 30		ns ns
Address Hold Time (t_{HA})	$V_{CC} = 5.0V$ $V_{CC} = 10V$	50 25	15 5		ns ns

ac electrical characteristics (con't)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Write Enable Pulse Width ($t_{\overline{WE}}$)	V_{CC} = 5.0V V_{CC} = 10V	300 150	160 70		ns ns
$\overline{CE}_3$ Pulse Widths (t_{CE})	V_{CC} = 5.0V V_{CC} = 10V	400 160	200 80		ns ns
Input Capacity (C_{IN})	Any Input (Note 2)		5.0		pF
Output Capacity in TRI-STATE (C_{OUT})	(Note 2)		9.0		pF
Power Dissipation Capacity (C_{pd})	(Note 3)		400		pF

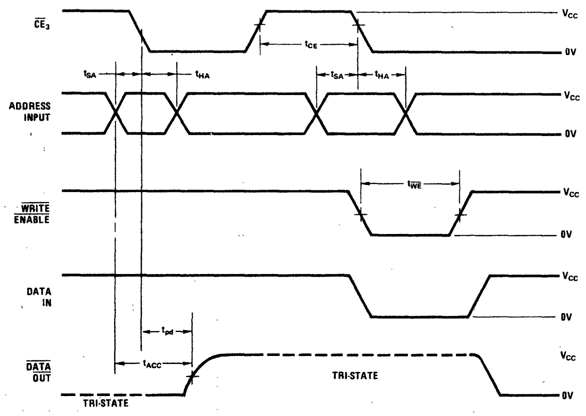
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

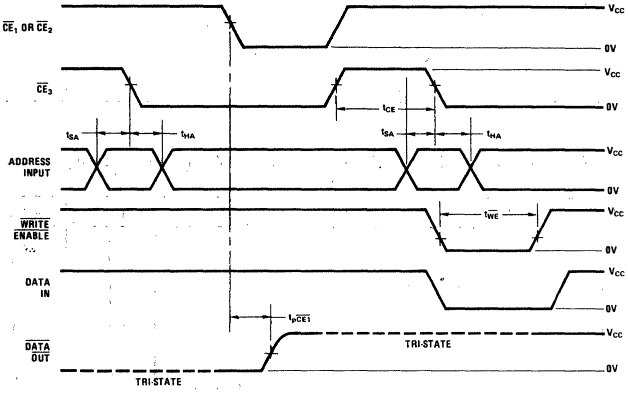
Note 3: C_{pd} determines the no load ac power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note, AN-90.

switching time waveforms

Read and Write Cycles Using $\overline{CE}_3$ ($\overline{CE}_1$ = $\overline{CE}_2$ = logic 0)



Read and Write Cycles Using $\overline{CE}_3$ and $\overline{CE}_1$ (or $\overline{CE}_2$)



Note: Used for fast access time in bused systems.

MM54C221/MM74C221 dual monostable multivibrator

general description

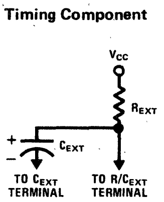
The MM54C221/MM74C221 dual monostable multivibrator is monolithic complementary MOS integrated circuit. Each multivibrator features a negative-transition-triggered input and a positive-transition-triggered input either of which can be used as an inhibit input, and a clear input.

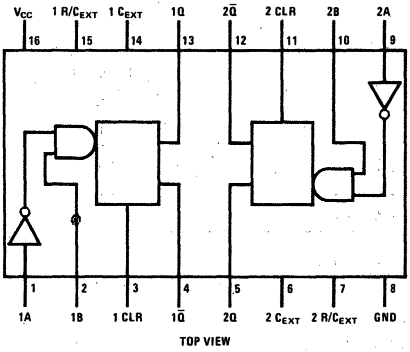
Once fired, the output pulses are independent of further transitions of the A and B inputs and are a function of the external timing components C_{EXT} and R_{EXT}. The pulse width is stable over a wide range of temperature and V_{CC}. Pulse stability will be limited by the accuracy of external timing components. The pulse width is approximately defined by the relationship $t_{W(OUT)} \approx C_{EXT} R_{EXT}$. For further information and applications, see AN-138.

features

■ Wide supply voltage range	4.5V to 15V
■ Guaranteed noise margin	1.0V
■ High noise immunity	0.45 V_{CC} typ
■ Low power TTL compatibility	fan out of 2 driving 74L

connection diagrams





truth table

INPUTS			OUTPUTS	
CLEAR	A	B	Q	$\overline{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⎍	⊔
H	↓	H	⎍	⊔

H = High level
L = Low level
↑ = Transition from low to high
↓ = Transition from high to low
⎍ = One high level pulse
⊔ = One low level pulse
X = Irrelevant

absolute maximum ratings (Note 1)

Voltage at Any Pin	−0.3V to V_{CC} + 0.3V	Package Dissipation	500 mW
Operating Temperature Range		Operating V_{CC} Range	4.5V to 15V
MM54C221	−55°C to +125°C	Absolute Maximum V_{CC}	16V
MM74C221	−40°C to +85°C	$R_{EXT} \geq 80\ V_{CC}$ (Ω)	
Storage Temperature Range	−65°C to +150°C	Lead Temperature (Soldering, 10 seconds)	300°C

dc electrical characteristics Min/max limits apply across temperature range, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CMOS TO CMOS					
Logical "1" Input Voltage ($V_{IN(1)}$)	V_{CC} = 5.0V	3.5			V
	V_{CC} = 10V	8.0			V
Logical "0" Input Voltage ($V_{IN(0)}$)	V_{CC} = 5.0V			1.5	V
	V_{CC} = 10V			2.0	V
Logical "1" Output Voltage ($V_{OUT(1)}$)	V_{CC} = 5.0V, I_O = −10μA	4.5			V
	V_{CC} = 10V, I_O = −10μA	9.0			V
Logical "0" Output Voltage ($V_{OUT(0)}$)	V_{CC} = 5.0V, I_O = 10μA			0.5	V
	V_{CC} = 10V, I_O = 10μA			1.0	V
Logical "1" Input Current ($I_{IN(1)}$)	V_{CC} = 15V, V_{IN} = 15V		0.005	1.0	μA
Logical "0" Input Current ($I_{IN(0)}$)	V_{CC} = 15V, V_{IN} = 0V	−1.0	−0.005		μA
Supply Current (I_{CC})	V_{CC} = 15V, R_{EXT} = ∞, Q1, Q2 = Logic 0 (Note 3)		0.05	300	μA
	V_{CC} = 15V, Q1 = Logic 1, Q2 = Logic 0		15		mA
	V_{CC} = 5.0V, Q1 = Logic 1, Q2 = Logic 0		2		mA
Leakage Current at R/C_{EXT} Pin	V_{CC} = 15V, V_{CEXT} = 5.0V		0.01	3	μA
CMOS/LPTTL INTERFACE					
Logical "1" Input Voltage ($V_{IN(1)}$)					
MM54C221	V_{CC} = 4.5V	V_{CC}−1.5			V
MM74C221	V_{CC} = 4.75V	V_{CC}−1.5			V
Logical "0" Input Voltage ($V_{IN(0)}$)					
MM54C221	V_{CC} = 4.5V			0.8	V
MM74C221	V_{CC} = 4.75V			0.8	V
Logical "1" Output Voltage ($V_{OUT(1)}$)					
MM54C221	V_{CC} = 4.5V, I_O = −360μA	2.4			V
MM74C221	V_{CC} = 4.75V, I_O = −360μA	2.4			V
Logical "0" Output Voltage ($V_{OUT(0)}$)					
MM54C221	V_{CC} = 4.5V, I_O = 360μA			0.4	V
MM74C221	V_{CC} = 4.75V, I_O = 360μA			0.4	V
OUTPUT DRIVE (See 54C/74C Family Characteristics Data Sheet)					
Output Source Current (I_{SOURCE}) (P-Channel)	V_{CC} = 5.0V, V_{OUT} = 0V, T_A = 25°C	−1.75	−3.3		mA
Output Source Current (I_{SOURCE}) (P-Channel)	V_{CC} = 10V, V_{OUT} = 0V, T_A = 25°C	−8.0	−15		mA
Output Sink Current (I_{SINK}) (N-Channel)	V_{CC} = 5.0V, V_{OUT} = V_{CC}, T_A = 25°C	1.75	3.6		mA
Output Sink Current (I_{SINK}) (N-Channel)	V_{CC} = 10V, V_{OUT} = V_{CC}, T_A = 25°C	8.0	16		mA

ac electrical characteristics $T_A = 25°C$, $C_L = 50$ pF, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Propagation Delay from Trigger Input (A, B) to Output Q, $\overline{Q}$ ($t_{PD\ A,B}$)	$V_{CC} = 5.0V$		250	500	ns
	$V_{CC} = 10V$		120	250	ns
Propagation Delay from Clear Input (CL) to Output Q, $\overline{Q}$ (t_{PDCL})	$V_{CC} = 5.0V$		250	500	ns
	$V_{CC} = 10V$		120	250	ns
Time Prior to Trigger Input (A,B) that Clear must be set (t_{SET})	$V_{CC} = 5.0V$	150	50		ns
	$V_{CC} = 10V$	60	20		ns
Trigger Input (A, B) Pulse Width ($t_{W(A,B)}$)	$V_{CC} = 5.0V$	150	50		ns
	$V_{CC} = 10V$	70	30		ns
Clear Input (CL) Pulse Width ($t_{W(CL)}$)	$V_{CC} = 5.0V$	150	50		ns
	$V_{CC} = 10V$	70	30		ns
Q or $\overline{Q}$ Output Pulse Width ($t_{W(OUT)}$)	$V_{CC} = 5.0V$, $R_{EXT} = 10k$, $C_{EXT} = 0$ pF		900		ns
	$V_{CC} = 10V$, $R_{EXT} = 10k$, $C_{EXT} = 0$ pF		350		ns
	$V_{CC} = 15V$, $R_{EXT} = 10k$, $C_{EXT} = 0$ pF		320		ns
	$V_{CC} = 5.0V$, $R_{EXT} = 10k$, $C_{EXT} = 1000$ pF	9	10.6	12.2	µs
	$V_{CC} = 10V$, $R_{EXT} = 10k$, $C_{EXT} = 1000$ pF	9	10	11	µs
	$V_{CC} = 15V$, $R_{EXT} = 10k$, $C_{EXT} = 1000$ pF	8.9	9.8	10.8	µs
	$V_{CC} = 5.0V$, $R_{EXT} = 10k$, $C_{EXT} = 0.1\mu F$	900	1020	1200	µs
	$V_{CC} = 10V$, $R_{EXT} = 10k$, $C_{EXT} = 0.1\mu F$	900	1000	1100	µs
	$V_{CC} = 15V$, $R_{EXT} = 10k$, $C_{EXT} = 0.1\mu F$	900	990	1100	µs
ON Resistance of Transistor Between R/C_{EXT} to C_{EXT} (R_{ON})	$V_{CC} = 5.0V$ (Note 4)		50	150	Ω
	$V_{CC} = 10V$ (Note 4)		25	65	Ω
	$V_{CC} = 15V$ (Note 4)		16.7	45	Ω
Output Duty Cycle	R = 10k, C = 1000 pF			90	%
	R = 10k, C = 0.1µF			95	%
Input Capacitance (C_{IN})	R/C_{EXT} Input (Note 2)		15	25	pF
	Any Other Input (Note 2)		5		pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

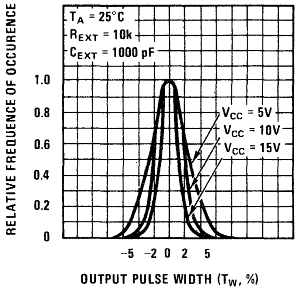
Note 2: Capacitance is guaranteed by periodic testing.

Note 3: In Standby (Q = Logic 0) the power dissipated equals the leakage current plus V_{CC}/R_{EXT}.

Note 4: See An-138 for detailed explanation of R_{ON}.

typical performance characteristics

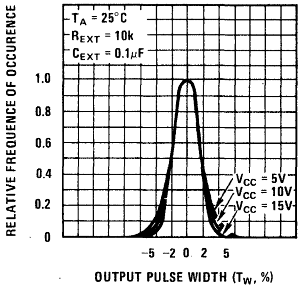
Typical Distribution of Units for Output Pulse Width



0% Point pulse width:
At V_{CC} = 5V, T_W = 10.6µs
At V_{CC} = 10V, T_W = 10µs
At V_{CC} = 15V, T_W = 9.8µs

Percentage of units within ±4%:
At V_{CC} = 5V, 90% of units
At V_{CC} = 10V, 95% of units
At V_{CC} = 15V, 98% of units

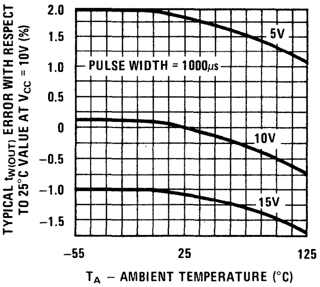
Typical Distribution of Units for Output Pulse Width



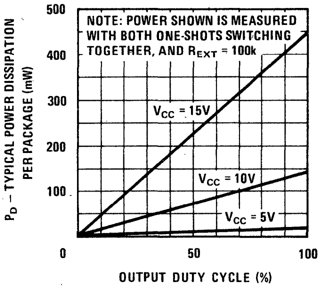
0% Point pulse width:
At V_{CC} = 5V, T_W = 1020µs
At V_{CC} = 10V, T_W = 1000µs
At V_{CC} = 15V, T_W = 982µs

Percentage of units within ±4%:
At V_{CC} = 5V, 95% of units
At V_{CC} = 10V, 97% of units
At V_{CC} = 15V, 98% of units

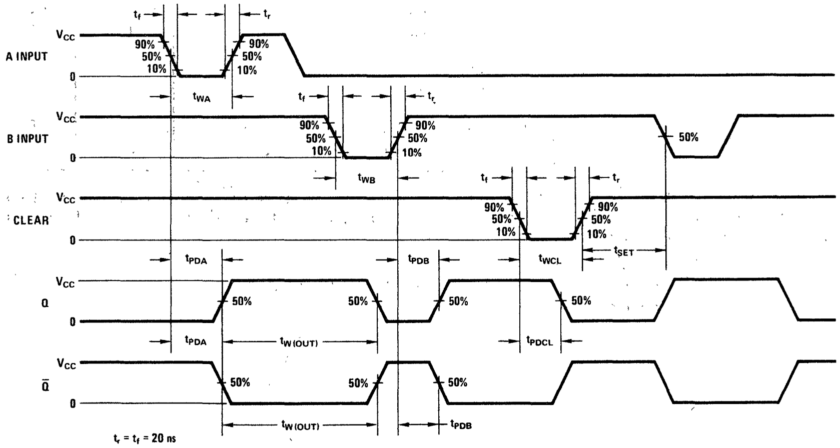
Typical Variation in Output Pulse Width vs Temperature



Typical Power Dissipation per Package



switching time waveforms



MM54C901/MM74C901 hex inverting TTL buffer
MM54C902/MM74C902 hex non-inverting TTL buffer
MM54C903/MM74C903 hex inverting PMOS buffer
MM54C904/MM74C904 hex non-inverting PMOS buffer

general description

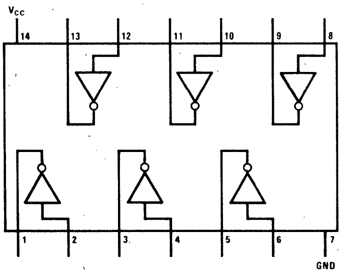
These hex buffers employ complementary MOS to achieve wide supply operating range, low power consumption, high noise immunity. These buffers provide direct interface from PMOS into CMOS or TTL and direct interface from CMOS to TTL or CMOS operating at a reduced V_{CC} supply. For specific applications see MOS Brief 18 in the back of this catalog.

features

■ Wide supply voltage range	3.0V to 15V
■ Guaranteed noise margin	1.0V
■ High noise immunity	0.45 V_{CC} typ
■ TTL compatibility	fan out of 2 driving standard TTL

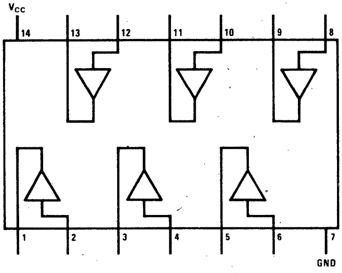
connection and logic diagrams

MM54C901/MM74C901
MM54C903/MM74C903



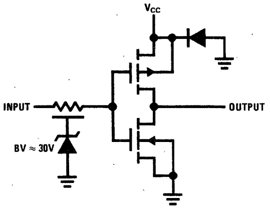
TOP VIEW

MM54C902/MM74C902
MM54C904/MM74C904

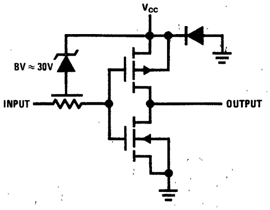


TOP VIEW

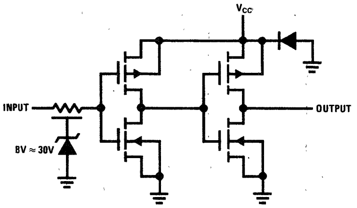
MM54C901/MM74C901
CMOS to TTL Inverting Buffer



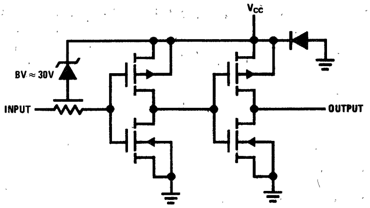
MM54C903/MM74C903
PMOS to TTL or CMOS Inverting Buffer



MM54C902/MM74C902
CMOS to TTL Buffer



MM54C904/MM74C904
PMOS to TTL or CMOS Buffer



absolute maximum ratings (Note 1)

Voltage at Any Output Pin	−0.3V to V_{CC} +0.3V
Voltage at Any Input Pin	
MM54C901/MM74C901	−0.3V to +15V
MM54C902/MM74C902	−0.3V to +15V
MM54C903/MM74C903	V_{CC} −17V to V_{CC} +0.3V
MM54C904/MM74C904	V_{CC} −17V to V_{CC} +0.3V
Operating Temperature Range	
MM54C901, MM54C902, MM54C903, MM54C904	−55°C to +125°C
MM74C901, MM74C902, MM74C903, MM74C904	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500 mW
Operating V_{CC} Range	3.0V to 15V
Absolute Maximum V_{CC}	16V
Lead Temperature (Soldering, 10 seconds)	300°C

dc electrical characteristics

Min/max limits apply across temperature range, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CMOS TO CMOS					
Logical "1" Input Voltage ($V_{IN(1)}$)	V_{CC} = 5.0V	3.5			V
	V_{CC} = 10V	8.0			V
Logical "0" Input Voltage ($V_{IN(0)}$)	V_{CC} = 5.0V			1.5	V
	V_{CC} = 10V			2.0	V
Logical "1" Output Voltage ($V_{OUT(1)}$)	V_{CC} = 5.0V, I_O = −10μA	4.5			V
	V_{CC} = 10V, I_O = −10μA	9.0			V
Logical "0" Output Voltage ($V_{OUT(0)}$)	V_{CC} = 5.0V, I_O = +10μA			0.5	V
	V_{CC} = 10V, I_O = +10μA			1.0	V
Logical "1" Input Current ($I_{IN(1)}$)	V_{CC} = 15V, V_{IN} = 15V		0.005	1.0	μA
Logical "0" Input Current ($I_{IN(0)}$)	V_{CC} = 15V, V_{IN} = 0V	−1.0	−0.005		μA
Supply Current (I_{CC})	V_{CC} = 15V		0.05	15	μA
TTL TO CMOS					
Logical "1" Input Voltage ($V_{IN(1)}$)	54C, V_{CC} = 4.5V	V_{CC}−1.5			V
	74C, V_{CC} = 4.75V	V_{CC}−1.5			V
Logical "0" Input Voltage ($V_{IN(0)}$)	54C, V_{CC} = 4.5V			0.8	V
	74C, V_{CC} = 4.75V			0.8	V
CMOS TO TTL					
Logical "1" Input Voltage ($V_{IN(1)}$)					
MM54C901, MM54C903	V_{CC} = 4.5V	4.0			V
MM54C902, MM54C904	V_{CC} = 4.5V	V_{CC}−1.5			V
MM74C901, MM74C903	V_{CC} = 4.75	4.25			V
MM74C902, MM74C904	V_{CC} = 4.75	V_{CC}−1.5			V
Logical "0" Input Voltage ($V_{IN(0)}$)					
MM54C901, MM54C903	V_{CC} = 4.5V			1.0	V
MM54C902, MM54C904	V_{CC} = 4.5V			1.5	V
MM74C901, MM74C903	V_{CC} = 4.75			1.0	V
MM74C902, MM74C904	V_{CC} = 4.75			1.5	V
Logical "1" Output Voltage ($V_{OUT(1)}$)	54C, V_{CC} = 4.5V, I_O = −800μA	2.4			V
	74C, V_{CC} = 4.75V, I_O = −800μA	2.4			V
Logical "0" Output Voltage ($V_{OUT(0)}$)					
MM54C901, MM54C903	V_{CC} = 4.5V, I_O = 2.6 mA			0.4	V
MM54C902, MM54C904	V_{CC} = 4.5V, I_O = 3.2 mA			0.4	V
MM74C901, MM74C903	V_{CC} = 4.75V, I_O = 2.6 mA			0.4	V
MM74C902, MM74C904	V_{CC} = 4.75V, I_O = 3.2 mA			0.4	V
OUTPUT DRIVE (MM54C901/MM74C901, MM54C903/MM74C903) (See 54C/74C Family Characteristics Data Sheet)					
Output Source Current (I_{SOURCE}) (P-Channel)	V_{CC} = 5.0V, V_{OUT} = 0V T_A = 25°C, V_{IN} = 0V	5.0			mA
Output Source Current (I_{SOURCE}) (P-Channel)	V_{CC} = 10V, V_{OUT} = 0V T_A = 25°C, V_{IN} = 0V	20			mA
Output Sink Current (I_{SINK}) (N-Channel)	V_{CC} = 5.0V, V_{OUT} = V_{CC} T_A = 25°C, V_{IN} = V_{CC}	9			mA
Output Sink Current (I_{SINK}) (N-Channel)	V_{CC} = 5.0V, V_{OUT} = 0.4V T_A = 25°C, V_{IN} = V_{CC}	3.8			mA

dc electrical characteristics (con't)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
OUTPUT DRIVE (MM54C902/MM74C902, MM54C904/MM74C904 (See 54C/74C Family Characteristics Data Sheet)					
Output Source Current (I_{SOURCE}) (P-Channel)	V_{CC} = 5.0V, V_{OUT} = 0V T_A = 25°C, V_{IN} = V_{CC}	5.0			mA
Output Source Current (I_{SOURCE}) (P-Channel)	V_{CC} = 10V, V_{OUT} = 0V T_A = 25°C, V_{IN} = V_{CC}	20			mA
Output Sink Current (I_{SINK}) (N-Channel)	V_{CC} = 5.0V, V_{OUT} = V_{CC} T_A = 25°C, V_{IN} = 0V	9			mA
Output Sink Current (I_{SINK}) (N-Channel)	V_{CC} = 5.0V, V_{OUT} = 0.4V T_A = 25°C, V_{IN} = 0V	3.8			mA

ac electrical characteristics T_A = 25°C, C_L = 50 pF, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
MM54C901/MM74C901, MM54C903/MM74C903					
Input Capacitance (C_{IN})	Any Input (Note 2)		14		pF
Power Dissipation Capacity (C_{pd})	(Note 3) Per Buffer		30		pF
Propagation Delay Time to a Logical "1" ($t_{pd(1)}$)	V_{CC} = 5.0V		38	70	ns
	V_{CC} = 10V		22	30	ns
Propagation Delay Time to a Logical "0" ($t_{pd(0)}$)	V_{CC} = 5.0V		21	35	ns
	V_{CC} = 10V		13	20	ns
MM54C902/MM74C902, MM54C904/MM74C904					
Input Capacitance (C_{IN})	Any Input (Note 2)		5.0		pF
Power Dissipation Capacity (C_{pd})	(Note 3) Per Buffer		50		pF
Propagation Delay Time to a Logical "1" ($t_{pd(1)}$)	V_{CC} = 5.0V		57	90	ns
	V_{CC} = 10V		27	40	ns
Propagation Delay Time to a Logical "0" ($t_{pd(0)}$)	V_{CC} = 5.0V		54	90	ns
	V_{CC} = 10V		25	40	ns

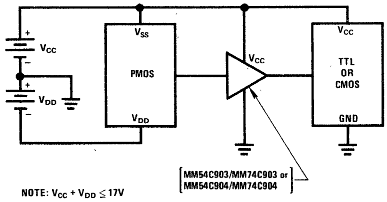
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note, AN-90.

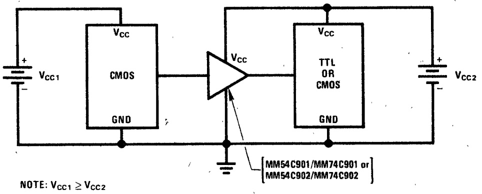
typical applications

PMOS to CMOS or TTL Interface



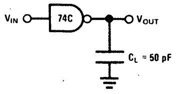
NOTE: $V_{CC} + V_{DD} \leq 17V$
$V_{CC} \leq 15V$

CMOS to TTL or CMOS at a Lower V_{CC}



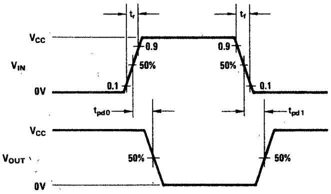
NOTE: $V_{CC1} \geq V_{CC2}$

ac test circuit and switching time waveforms



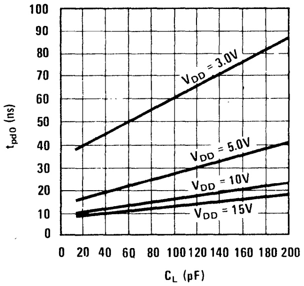
Note: Delays measured with input t_r, t_f = 20 ns.

CMOS to CMOS

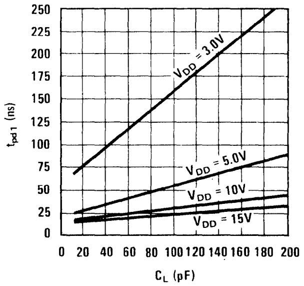


typical performance characteristics

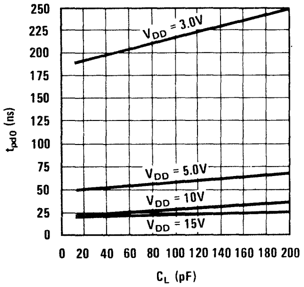
Typical Propagation Delay to a Logical "0" for the MM54C901/MM74C901 and MM54C903/MM74C903



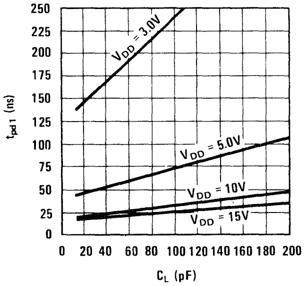
Typical Propagation Delay to a Logical "1" for the MM54C901/MM74C901 and MM54C903/MM74C903



Typical Propagation Delay to a Logical "0" for the MM54C902/MM74C902 and MM54C904/MM74C904



Typical Propagation Delay to a Logical "1" for the MM54C902/MM74C902 and MM54C904/MM74C904



MM54C905/MM74C905 12-bit successive approximation register

general description

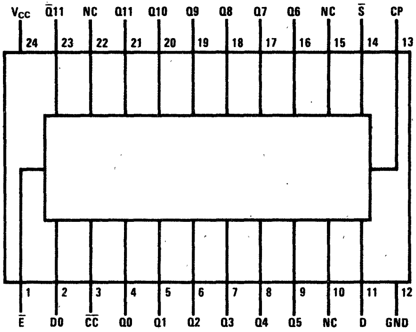
The MM54C905/MM74C905 CMOS 12-bit successive approximation register contains all the digit control and storage necessary for successive approximation analog-to-digital conversion. Because of the unique capability of CMOS to switch to each supply rail without any offset voltage, it can also be used in digital systems as the control and storage element in repetitive routines.

features

- Wide supply voltage range 3.0V to 15V
- Guaranteed noise margin 1.0V
- High noise immunity 0.45 V_{CC} typ
- Low power TTL compatibility fan out of 2 driving 74L
- Provision for register extension or truncation
- Operates in START/STOP or continuous conversion mode
- Drive ladder switches directly. For 10 bits or less with 50k/100k R/2R ladder network

---

connection diagram



truth table

TIME	INPUTS			OUTPUTS													
t_n	D	$\overline{S}$	$\overline{E}$	D0	Q11	Q10	Q9	Q8	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0	$\overline{CC}$
0	X	L	L	X	X	X	X	X	X	X	X	X	X	X	X	X	X
1	D11	H	L	X	L	H	H	H	H	H	H	H	H	H	H	H	H
2	D10	H	L	D11	D11	L	H	H	H	H	H	H	H	H	H	H	H
3	D9	H	L	D10	D11	D10	L	H	H	H	H	H	H	H	H	H	H
4	D8	H	L	D9	D11	D10	D9	L	H	H	H	H	H	H	H	H	H
5	D7	H	L	D8	D11	D10	D9	D8	L	H	H	H	H	H	H	H	H
6	D6	H	L	D7	D11	D10	D9	D8	D7	L	H	H	H	H	H	H	H
7	D5	H	L	D6	D11	D10	D9	D8	D7	D6	L	H	H	H	H	H	H
8	D4	H	L	D5	D11	D10	D9	D8	D7	D6	D5	L	H	H	H	H	H
9	D3	H	L	D4	D11	D10	D9	D8	D7	D6	D5	D4	L	H	H	H	H
10	D2	H	L	D3	D11	D10	D9	D8	D7	D6	D5	D4	D3	L	H	H	H
11	D1	H	L	D2	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	L	H	H
12	D0	H	L	D1	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	L	H
13	X	H	L	D0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	L
14	X	X	L	X	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	L
	X	X	H	X	H	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC

H = High level
L = Low level
X = Don't care
NC = No change

absolute maximum ratings (Note 1)

Voltage at Any Pin	$-0.3V$ to V_{CC} $+0.3V$
Operating Temperature Range	
MM54C905	−55°C to +125°C
MM74C905	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500 mW
Operating V_{CC} Range	3.0V to 15V
Absolute Maximum V_{CC}	16V
Lead Temperature (Soldering, 10 seconds)	300°C

dc electrical characteristics

Min/max limits apply across temperature range, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CMOS TO CMOS					
Logical "1" Input Voltage ($V_{IN(1)}$)	$V_{CC} = 5.0V$	3.5			V
	$V_{CC} = 10V$	8.0			V
Logical "0" Input Voltage ($V_{IN(0)}$)	$V_{CC} = 5.0V$			1.5	V
	$V_{CC} = 10V$			2.0	V
Logical "1" Output Voltage ($V_{OUT(1)}$)	$V_{CC} = 5.0V$, $I_O = -10\mu A$	4.5			V
	$V_{CC} = 10V$, $I_O = -10\mu A$	9.0			V
Logical "0" Output Voltage ($V_{OUT(0)}$)	$V_{CC} = 5.0V$, $I_O = 10\mu A$			0.5	V
	$V_{CC} = 10V$, $I_O = 10\mu A$			1.0	V
Logical "1" Input Current ($I_{IN(1)}$)	$V_{CC} = 15V$, $V_{IN} = 15V$		0.005	1.0	μA
Logical "0" Input Current ($I_{IN(0)}$)	$V_{CC} = 15V$, $V_{IN} = 0V$	−1.0	−0.005		μA
Supply Current (I_{CC})	$V_{CC} = 15V$		0.05	300	μA
CMOS/LPTTL INTERFACE					
Logical "1" Input Voltage ($V_{IN(1)}$)					
MM54C905	$V_{CC} = 4.5V$	$V_{CC}-1.5$			V
MM74C905	$V_{CC} = 4.75V$	$V_{CC}-1.5$			V
Logical "0" Input Voltage ($V_{IN(0)}$)					
MM54C905	$V_{CC} = 4.5V$			0.8	V
MM74C905	$V_{CC} = 4.75V$			0.8	V
Logical "1" Output Voltage ($V_{OUT(1)}$)					
MM54C905	$V_{CC} = 4.5V$, $I_O = -360\mu A$	2.4			V
MM74C905	$V_{CC} = 4.75V$, $I_O = -360\mu A$	2.4			V
Logical "0" Output Voltage ($V_{OUT(0)}$)					
MM54C905	$V_{CC} = 4.5V$, $I_O = 360\mu A$			0.4	V
MM74C905	$V_{CC} = 4.75V$, $I_O = 360\mu A$			0.4	V
OUTPUT DRIVE (See 54C/74C Family Characteristics Data Sheet)					
Output Source Current (I_{SOURCE}) (P-Channel)	$V_{CC} = 5.0V$, $V_{OUT} = 0V$ $T_A = 25°C$	−1.75	−3.3		mA
Output Source Current (I_{SOURCE}) (P-Channel)	$V_{CC} = 10V$, $V_{OUT} = 0V$ $T_A = 25°C$	−8.0	−15		mA
Output Sink Current (I_{SINK}) (N-Channel)	$V_{CC} = 5.0V$, $V_{OUT} = V_{CC}$ $T_A = 25°C$	1.75	3.6		mA
Output Sink Current (I_{SINK}) (N-Channel)	$V_{CC} = 10V$, $V_{OUT} = V_{CC}$ $T_A = 25°C$	8.0	16		mA
Q11–Q0 Outputs R_{SOURCE}	$V_{CC} = 10V \pm 5\%$ $V_{OUT} = V_{CC} - 0.3V$ $T_A = 25°C$	150		350	Ω
R_{SINK}	$V_{CC} = 10V \pm 5\%$ $V_{OUT} = 0.3V$ $T_A = 25°C$	80		230	Ω

ac electrical characteristics $T_A = 25°C$, $C_L = 50$ pF, unless otherwise specified.

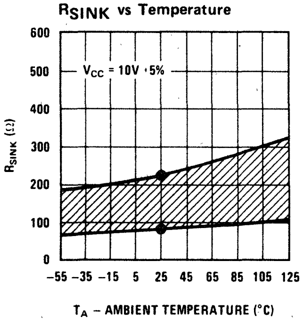
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Propagation Delay Time From Clock Input To Outputs (Q0–Q11) ($t_{pd(Q)}$)	$V_{CC} = 5.0V$ $V_{CC} = 10V$		200 80	350 150	ns ns
Propagation Delay Time From Clock Input To D_O ($t_{pd(D_O)}$)	$V_{CC} = 5.0V$ $V_{CC} = 10V$		180 70	325 125	ns ns
Propagation Delay Time From Register Enable ($\overline{E}$) To Output (Q11) ($t_{pd(\overline{E})}$)	$V_{CC} = 5.0V$ $V_{CC} = 10V$		190 75	350 150	ns ns
Propagation Delay Time From Clock To $\overline{CC}$ ($t_{pd(\overline{CC})}$)	$V_{CC} = 5.0V$ $V_{CC} = 10V$		190 75	350 0.50	ns ns
Data Input Set-Up Time (t_{DS})	$V_{CC} = 5.0V$ $V_{CC} = 10V$	80 30			ns ns
Start Input Set-Up Time (t_{SS})	$V_{CC} = 5.0V$ $V_{CC} = 10V$	80 30			ns ns
Minimum Clock Pulse Width (t_{PWL}, t_{PWH})	$V_{CC} = 5.0V$ $V_{CC} = 10V$	250 100	125 50		ns ns
Maximum Clock Rise and Fall Time (t_r, t_f)	$V_{CC} = 5.0V$ $V_{CC} = 10V$			15 5	μs μs
Maximum Clock Frequency (f_{MAX})	$V_{CC} = 5.0V$ $V_{CC} = 10V$	2 5	4 10		MHz MHz
Clock Input Capacitance (C_{CLK})	Clock Input (Note 2)		10		pF
Input Capacitance (C_{IN})	Any Other Input (Note 2)		5		pF
Power Dissipation Capacitance (C_{PD})	(Note 3)		100		pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

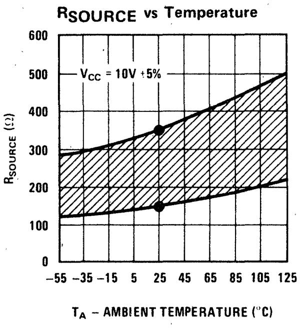
Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note, AN-90.

typical performance characteristics

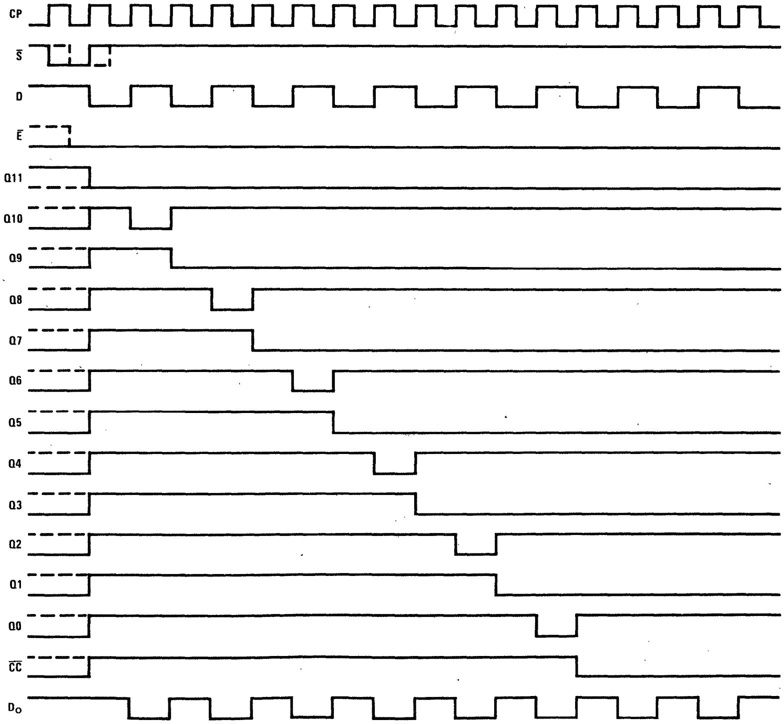

R_{SINK} vs Temperature

● These points are guaranteed by automatic testing.

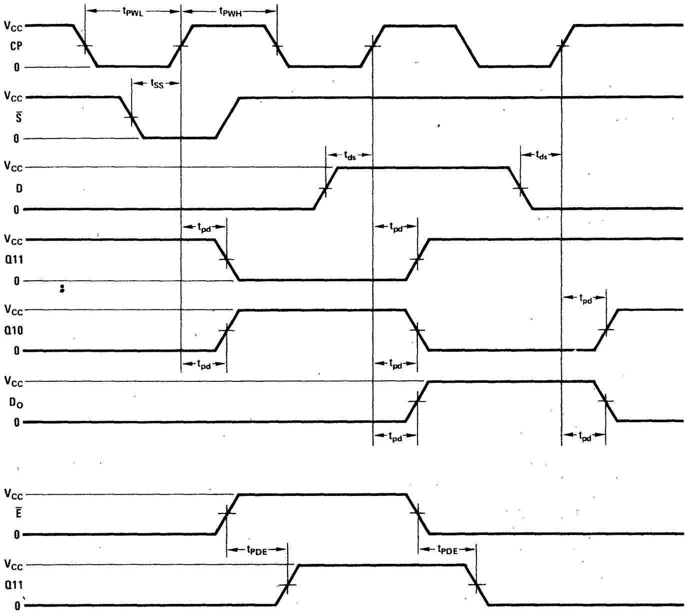

R_{SOURCE} vs Temperature

● These points are guaranteed by automatic testing.

timing diagram



switching time waveforms



USER NOTES FOR A/D CONVERSION

The register can be used with either current switches that require a low voltage level to turn the switch ON or current switches that require a high voltage level to turn the switch ON. If current switches are used which turn ON with a low logic level, the resulting digit output from the register is active low. That is, a logic "1" is represented as a low voltage level. If current switches are used which turn ON with a high logic level, the resulting digit output is active high. A logic "1" is represented as a high voltage level.

For a maximum error of ±1/2 LSB, the comparator must be biased. If current switches that require a high voltage level to turn ON are used, the comparator should be biased +1/2 LSB and if the current switches require a low logic level to turn ON, then the comparator must be biased −1/2 LSB.

The register can be used to perform 2's complement conversion by offsetting the comparator one half full range +1/2 LSB and using the complement of the MSB $\overline{Q11}$ as the sign bit.

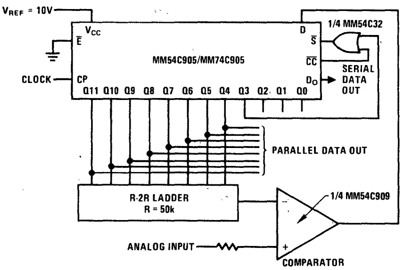
If the register is truncated and operated in the continuous conversion mode, a lock-up condition may occur on power-ON. This situation can be overcome by making the START input the "OR" function of $\overline{CC}$ and the appropriate register output.

The register, by suitable selection of register ladder network, can be used to perform either binary or BCD conversion.

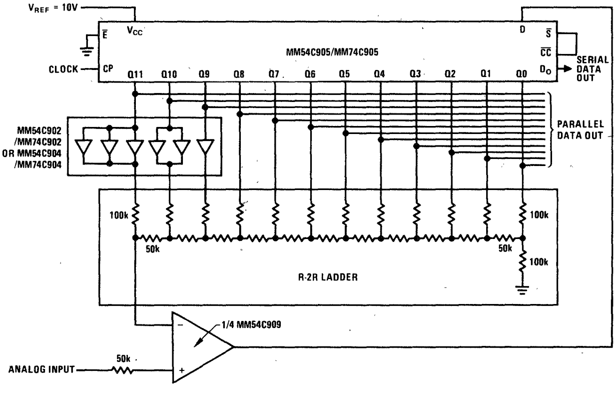
The register outputs can drive the 10 bits or less with 50k/100k R/2R ladder network directly for V_{CC} = 10V or higher. In order to drive the 12-bit 50k/100k ladder network and have the ±1/2 LSB resolution, the MM54C902/MM74C902 or MM54C904/MM74C904 is used as buffers, three buffers for MSB (Q11), two buffers for Q10, and one buffer for Q9.

typical applications

12-Bit Successive Approximation A-to-D Converter Operating in Continuous 8-Bit Truncated Mode



12-Bit Successive Approximation A-to-D Converter, Operating in Continuous Mode, Drives the 50k/100k Ladder Network Directly



definition of terms

CP: Register *clock* input.

$\overline{CC}$: *Conversion complete*—this output remains at $V_{OUT(1)}$ during a conversion and goes to $V_{OUT(0)}$ when conversion is complete.

D: Serial *data* input—connected to comparator output in A-to-D applications.

$\overline{E}$: *Register enable*—this input is used to expand the length of the register. When $\overline{E}$ is at $V_{IN(1)}$ Q11 is forced to $V_{OUT(1)}$ and inhibits conversion. When not used for expansion $\overline{E}$ must be connected to $V_{IN(0)}$ (GND).

Q11: True register MSB output.

$\overline{Q11}$: Complement of register MSB output.

Qi (i = 0 to 11): Register outputs.

$\overline{S}$: *Start input*—holding start input at $V_{IN(0)}$ for at least one clock period will initiate a conversion by setting MSB (Q11) at $V_{OUT(0)}$ and all other output (Q10–Q0) at $V_{OUT(1)}$. If set-up time requirements are met, a conversion may be initiated by holding start input at $V_{IN(0)}$ for less than one clock period.

DO: *Serial data output*—D input delayed by one clock period.

MM54C906/MM74C906 hex open drain N-channel buffers MM54C907/MM74C907 hex open drain P-channel buffers

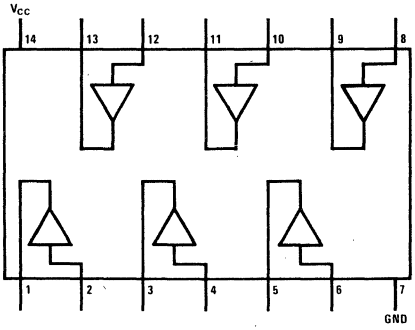
general description

These buffers employ monolithic CMOS technology in achieving open drain outputs. The MM54C906/MM74C906 consists of six inverters driving six N-channel devices; and the MM54C907/MM74C907 consists of six inverters driving six P-channel devices. The open drain feature of these buffers makes level shifting or wire AND and wire OR functions by just the addition of pull-up or pull-down resistors. All inputs are protected from static discharge by diode clamps to V_{CC} and to ground.

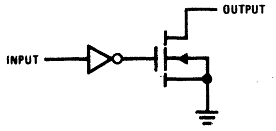
features

- Wide supply voltage range 3.0V to 15V
- Guaranteed noise margin 1.0V
- High noise immunity 0.45 V_{CC} typ
- High current sourcing and sinking open drain outputs

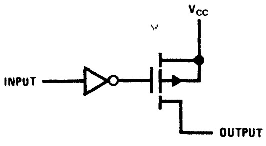
connection diagram



logic diagrams



MM54C906/MM74C906



MM54C907/MM74C907

absolute maximum ratings (Note 1)

Voltage at Any Input Pin	−0.3V to V_{CC} + 0.3V
Voltage at Any Output Pin	
MM54C906/MM74C906	−0.3V to +18V
MM54C907/MM74C907	V_{CC} − 18V to V_{CC} + 0.3V
Operating Temperature Range	
MM54C906/MM54C907	−55°C to +125°C
MM74C906/MM74C907	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500 mW
Operating V_{CC} Range	3.0V to 15V
Absolute Maximum V_{CC}	16V
Lead Temperature (Soldering, 10 seconds)	300°C

dc electrical characteristics

Min/max limits apply across temperature range, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CMOS TO CMOS					
Logical "1" Input Voltage ($V_{IN(1)}$)	V_{CC} = 5.0V	3.5			V
	V_{CC} = 10V	8.0			V
Logical "0" Input Voltage ($V_{IN(0)}$)	V_{CC} = 5.0V			1.5	V
	V_{CC} = 10V			2.0	V
Logical "1" Input Current ($I_{IN(1)}$)	V_{CC} = 15V, V_{IN} = 15V		0.005	1.0	μA
Logical "0" Input Current ($I_{IN(0)}$)	V_{CC} = 15V, V_{IN} = 0V	−1.0	−0.005		μA
Supply Current (I_{CC})	V_{CC} = 15V, Output Open		0.05	15	μA
Output Leakage					
MM54C906	V_{CC} = 4.5V, V_{IN} = V_{CC}−1.5		0.005	5	μA
	V_{CC} = 4.5V, V_{OUT} = 18V				
MM74C906	V_{CC} = 4.75V, V_{IN} = V_{CC}−1.5		0.005	5	μA
	V_{CC} = 4.75V, V_{OUT} = 18V				
MM54C907	V_{CC} = 4.5V, V_{IN} = 1.0V + 0.1 V_{CC}		0.005	5	μA
	V_{CC} = 4.5V, V_{OUT} = V_{CC}−18V				
MM74C907	V_{CC} = 4.75V, V_{IN} = 1.0V + 0.1 V_{CC}		0.005	5	μA
	V_{CC} = 4.75V, V_{OUT} = V_{CC}−18V				
CMOS/LPTTL INTERFACE					
Logical "1" Input Voltage ($V_{IN(1)}$)	54C, V_{CC} = 4.5V	V_{CC}−1.5			V
	74C, V_{CC} = 4.75V	V_{CC}−1.5			V
Logical "0" Input Voltage ($V_{IN(0)}$)	54C, V_{CC} = 4.5V			0.8	V
	74C, V_{CC} = 4.75V			0.8	V
OUTPUT DRIVE CURRENT					
MM54C906	V_{CC} = 4.5V, V_{IN} = 1.0V + 0.1 V_{CC}				
	V_{CC} = 4.5V, V_{OUT} = 0.5V		8		mA
	V_{CC} = 4.5V, V_{OUT} = 1.0V		12		mA
MM74C906	V_{CC} = 4.75V, V_{IN} = 1.0V + 0.1 V_{CC}				
	V_{CC} = 4.75V, V_{OUT} = 0.5V		8		mA
	V_{CC} = 4.75V, V_{OUT} = 1.0V		12		mA
MM54C907	V_{CC} = 4.5V, V_{IN} = V_{CC}−1.5				
	V_{CC} = 4.5V, V_{OUT} = V_{CC}−0.5V		1.5		mA
	V_{CC} = 4.5V, V_{OUT} = V_{CC}−1.0V		3.0		mA
MM74C907	V_{CC} = 4.75V, V_{IN} = V_{CC}−1.5				
	V_{CC} = 4.75V, V_{OUT} = V_{CC}−0.5V		1.5		mA
	V_{CC} = 4.75V, V_{OUT} = V_{CC}−1.0V		3.0		mA
MM54C906/MM74C906	V_{CC} = 10V, V_{IN} = 2.0V				
	V_{CC} = 10V, V_{OUT} = 0.5V		20		mA
	V_{CC} = 10V, V_{OUT} = 1.0V		30		mA
MM54C907/MM74C907	V_{CC} = 10V, V_{IN} = 8.0V				
	V_{CC} = 10V, V_{OUT} = 9.5V		4.0		mA
	V_{CC} = 10V, V_{OUT} = 9.0V		8.0		mA

ac electrical characteristics $T_A = 25°C$, $C_L = 50$ pF, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Propagation Delay to a Logical "0" (t_{pd0})					
MM54C906/MM74C906	V_{CC} = 5V, R = 10k			150	ns
	V_{CC} = 10V, R = 10k			75	ns
MM54C907/MM74C907	V_{CC} = 5V, (Note 4)			150 + 0.7 RC	ns
	V_{CC} = 10V, (Note 4)			75 + 0.7 RC	ns
Propagation Delay to a Logical "1" (t_{pd1})					
MM54C906/MM74C906	V_{CC} = 5V, (Note 4)			150 + 0.7 RC	ns
	V_{CC} = 10V (Note 4)			75 + 0.7 RC	ns
MM54C907/MM74C907	V_{CC} = 5V, R = 10k			150	ns
	V_{CC} = 10V, R = 10k			75	ns
Input Capacity (C_{IN})	(Note 2)		5		pF
Output Capacity (C_{OUT})	(Note 2)		20		pF
Power Dissipation Capacity (C_{pd})	(Note 3) Per Buffer		30		pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

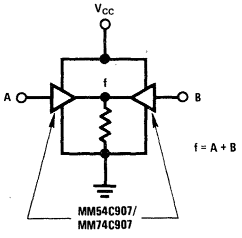
Note 2: Capacitance is guranteed by periodic testing.

Note 3: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note, AN-90. (Assumes outputs are open.)

Note 4: "C" used in calculating propagation includes output load capacity (C_L) plus device output capacity (C_{OUT}).

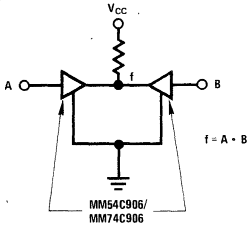
typical applications

Wire OR Gate



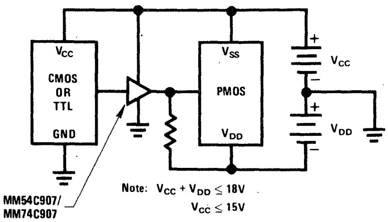
Note: Can be extended to more than 2 inputs.

Wire AND Gate



Note: Can be extended to more than 2 inputs.

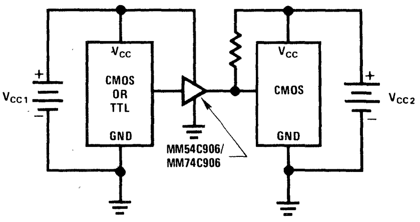
CMOS or TTL to PMOS Interface



Note: $V_{CC} + V_{DD} \leq 18V$

$V_{CC} \leq 15V$

CMOS or TTL to CMOS at a Higher V_{CC}



MM74C908, MM74C918 dual high voltage CMOS drivers

general description

The MM74C908 and MM74C918 are general purpose dual high voltage drivers, each capable of sourcing a minimum of 250 mA at $V_{OUT} = V_{CC} - 3V$, and $T_j = +65°C$.

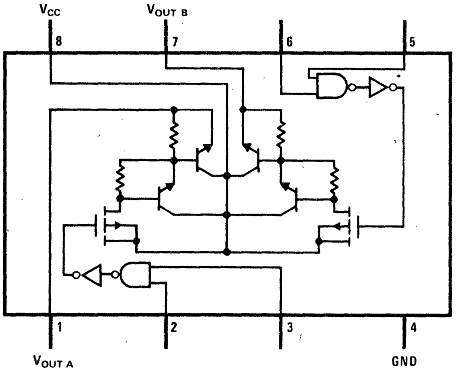
The MM74C908 and MM74C918 consist of two CMOS NAND gates driving an emitter follower darlington output to achieve high current drive and high voltage capabilities. In the "OFF" state the outputs can withstand a maximum of 30V across the device. These CMOS drivers are useful in interfacing normal CMOS voltage levels to driving relays, regulators, lamps, etc.

features

■ Wide supply voltage range	3V to 18V
■ High noise immunity	0.45 V_{CC} (typ)
■ Low output "ON" resistance	8Ω (typ)
■ High voltage	30V
■ High current	250 mA

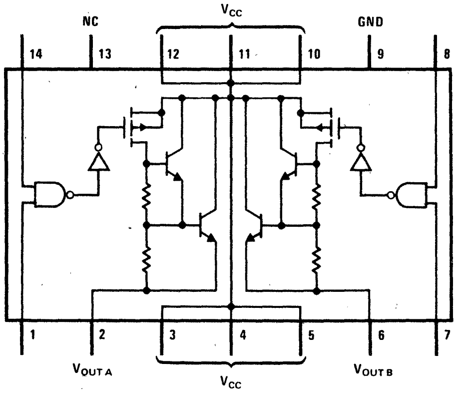
connection diagrams

MM74C908



TOP VIEW

MM74C918



TOP VIEW

absolute maximum ratings (Note 1)

Voltage at Any Input Pin	−0.3V to V_{CC} +0.3V
Voltage at Any Output Pin	32V
Operating Temperature Range	
MM74C908/MM74C918	−40°C to +85°C
Operating V_{CC} Range	3V to 18V
Absolute Maximum V_{CC}	19V
I_{SOURCE}	500 mA
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C
Package Dissipation	Refer to Maximum Power Dissipation vs Ambient Temperature Graph

dc electrical characteristics

Min/max limits apply across temperature range, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CMOS TO CMOS					
Logical "1" Input Voltage ($V_{IN(1)}$)	V_{CC} = 5V V_{CC} = 10V	3.5 8			V V
Logical "0" Input Voltage ($V_{IN(0)}$)	V_{CC} = 5V V_{CC} = 10V			1.5 2	V V
Logical "1" Input Current ($I_{IN(1)}$)	V_{CC} = 15V, V_{IN} = 15V		0.005	1	µA
Logical "0" Input Current ($I_{IN(0)}$)	V_{CC} = 15V, V_{IN} = 0V	−1	−0.005		µA
Supply Current (I_{CC})	V_{CC} = 15V, Outputs Open Circuit		0.05	15	µA
Output "OFF" Voltage	V_{IN} = V_{CC}, I_{OUT} = −200µA	30	56		V
CMOS/LPTTL INTERFACE					
Logical "1" Input Voltage ($V_{IN(1)}$) MM74C908/MM74C918	V_{CC} = 4.75V	V_{CC}−1.5			V
Logical "0" Input Voltage ($V_{IN(0)}$) MM74C908/MM74C918	V_{CC} = 4.75V		0.8		V
OUTPUT DRIVE					
Output Voltage (V_{OUT})	I_{OUT} = −300 mA, $V_{CC} \geq$ 5V, T_j = 25°C I_{OUT} = −250 mA, $V_{CC} \geq$ 5V, T_j = 65°C I_{OUT} = −200 mA, $V_{CC} \geq$ 5V, T_j = 150°C		V_{CC}−1.8 V_{CC}−1.9 V_{CC}−2.0	V_{CC}−2.7 V_{CC}−3.0 V_{CC}−3.6	V V V
Output Resistance (R_{ON})	I_{OUT} = −300 mA, $V_{CC} \geq$ 5V, T_j = 25°C I_{OUT} = −250 mA, $V_{CC} \geq$ 5V, T_j = 65°C I_{OUT} = −200 mA, $V_{CC} \geq$ 5V, T_j = 150°C		6 7.5 10	9 12 18	Ω Ω Ω
Output Resistance Temperature Coefficient			0.55	0.80	%/°C
Thermal Resistance (θ_{jA}) MM74C908 MM74C918	 (Note 3) (Note 3)		 100 45	 110 55	 °C/W °C/W

ac electrical characteristics

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Propagation Delay to a Logic "1" (t_{pd1})	V_{CC} = 5V, R_L = 50Ω, C_L = 50 pF, T_A = 25°C V_{CC} = 10V, R_L = 50Ω, C_L = 50 pF, T_A = 25°C		150 65	300 120	ns ns
Propagation Delay to a Logic "0" (t_{pd0})	V_{CC} = 5V, R_L = 50Ω, C_L = 50 pF, T_A = 25°C V_{CC} = 10V, R_L = 50Ω, C_L = 50 pF, T_A = 25°C		2 4	10 20	µs µs
Input Capacitance (C_{IN})	(Note 2)		5.0		pF

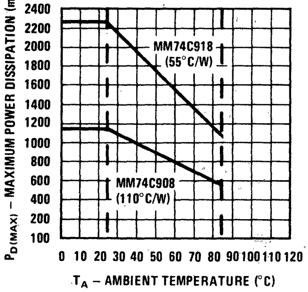
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

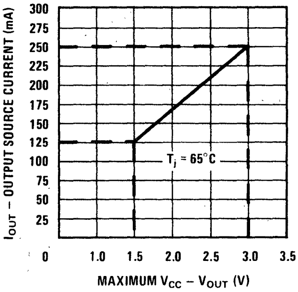
Note 3: θ_{jA} measured in free air with device soldered into printed circuit board.

typical performance characteristics

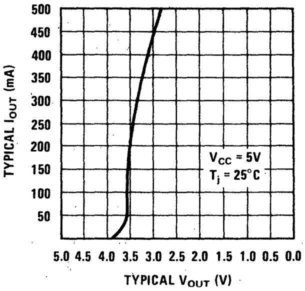
Maximum Power Dissipation vs Ambient Temperature



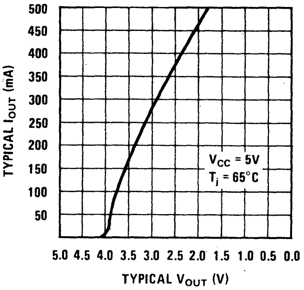
Maximum $V_{CC} - V_{OUT}$ vs I_{OUT}



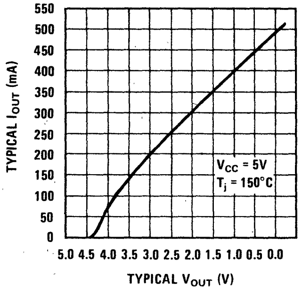
Typical I_{OUT} vs Typical V_{OUT}



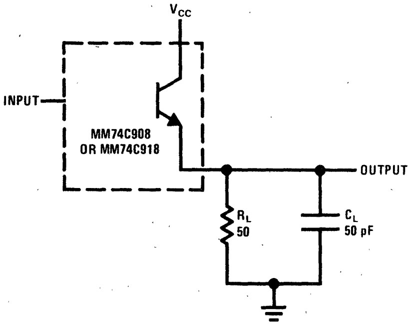
Typical I_{OUT} vs Typical V_{OUT}



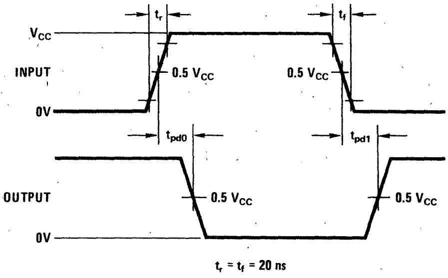
Typical I_{OUT} vs Typical V_{OUT}



ac test circuit



switching time waveforms



power considerations

Calculating Output "ON" Resistance ($R_L > 18\Omega$)

The output "ON" resistance, R_{ON}, is a function of the junction temperature, T_j, and is given by:

$$R_{ON} = 9\,(T_j - 25)\,(0.008) + 9 \tag{1}$$

and T_j is given by:

$$T_j = T_A + P_{DAV}\,\theta_{jA}, \tag{2}$$

where T_A = ambient temperature, θ_{jA} = thermal resistance, and P_{DAV} is the average power dissipated within the device. P_{DAV} consists of normal CMOS power terms (due to leakage currents, internal capacitance, switching, etc.) which are insignificant when compared to the power dissipated in the outputs. Thus, the output power term defines the allowable limits of operation and includes both outputs, A and B. P_D is given by:

$$P_D = I_{OA}^{\,2}\,R_{ON} + I_{OB}^{\,2}\,R_{ON}, \tag{3}$$

where I_O is the output current, given by:

$$I_O = \frac{V_{CC} - V_L}{R_{ON} + R_L} \tag{4}$$

V_L is the load voltage.

The average power dissipation, P_{DAV}, is a function of the duty cycle:

$$P_{DAV} = I_{OA}^{\,2}\,R_{ON}\,(\text{Duty Cycle}_A) + I_{OB}^{\,2}\,R_{ON}\,(\text{Duty Cycle}_B) \tag{5}$$

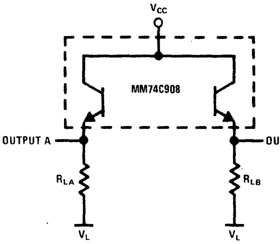
where the duty cycle is the % time in the current source state. Substituting equations (1) and (5) into (2) yields:

$$T_j = T_A + \theta_{jA}\,[9\,(T_j - 25)\,(0.008) + 9]\,[I_{OA}^{\,2}\,(\text{Duty Cycle}_A) + I_{OB}^{\,2}\,(\text{Duty Cycle}_B)] \tag{6a}$$

simplifying:

$$T_j = \frac{T_A + 7.2\,\theta_{jA}\,[I_{OA}^{\,2}\,(\text{Duty Cycle}_A) + I_{OB}^{\,2}\,(\text{Duty Cycle}_B)]}{1 - 0.072\,\theta_{jA}\,[I_{OA}^{\,2}\,(\text{Duty Cycle}_A) + I_{OB}^{\,2}\,(\text{Duty Cycle}_B)]} \tag{6b}$$

Equations (1), (4), and (6b) can be used in an iterative method to determine the output current, output resistance and junction temperature.



For example, let $V_{CC} = 15V$, $R_{LA} = 100\Omega$, $R_{LB} = 100\Omega$, $V_L = 0V$, $T_A = 25°C$, $\theta_{jA} = 110°C/W$, Duty $\text{Cycle}_A = 50\%$, Duty $\text{Cycle}_B = 75\%$.
Assuming $R_{ON} = 11\Omega$, then:

$$I_{OA} = \frac{V_{CC} - V_L}{R_{ON} + R_{LA}} = \frac{15}{11 + 100} = 135.1\text{ mA},$$

$$I_{OB} = \frac{V_{CC} - V_L}{R_{ON} + R_{LB}} = 135.1\text{ mA}$$

and

$$T_j = \frac{T_A + 7.2\,\theta_{jA}\,[I_{OA}^{\,2}\,(\text{Duty Cycle}_A) + I_{OB}^{\,2}\,(\text{Duty Cycle}_B)]}{1 - 0.072\,\theta_{jA}\,[I_{OA}^{\,2}\,(\text{Duty Cycle}_A) + I_{OB}^{\,2}\,(\text{Duty Cycle}_B)]}$$

$$T_j = \frac{25 + (7.2)\,(110)\,[(0.1351)^2\,(0.5) + (0.1351)^2\,(0.75)]}{1 - (0.072)\,(110)\,[(0.1351)^2\,(0.5) + (0.1351)^2\,(0.75)]}$$

$T_j = 52.6°C$

and $R_{ON} = 9\,(T_j - 25)\,(0.008) + 9 =$
$9\,(52.6 - 25)\,(0.008) + 9 = 11\Omega$

MM54C909/MM74C909 quad comparator

general description

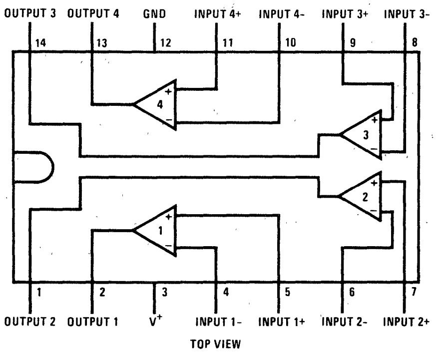
The MM54C909/MM74C909 contains four independent voltage comparators designed to operate from standard 54C/74C power supplies. The output allows current sinking only thus the wire OR function is possible using a common resistor pull up.

Not only does the MM54C909/MM74C909 function as a comparator for analog inputs but also has many applications as a voltage translator and buffer when interfacing the 54C/74C family to other logic systems.

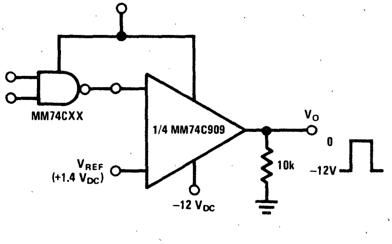
features

■ Wide supply voltage range	3.0V to 15V
■ TTL compatibility	fan out of 1 driving 74
■ Low power consumption	I_{CC} = 800μA typ at V_{CC} = 5.0 V_{DC}
■ Low input bias current	250 nA max
■ Low input offset current	±50 nA max
■ Low input offset voltage	±5.0 mV max
■ Large common mode input voltage range	0V to V_{CC}−1.5V
■ Large differential input voltage range	V_{CC}

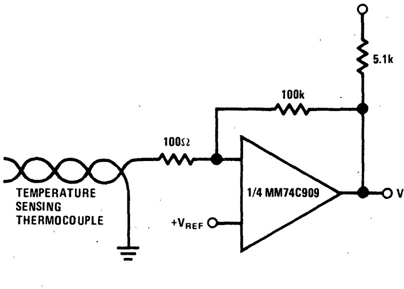
connection diagram



typical applications $(V^+ = 5.0\ V_{DC})$



CMOS/TTL to MOS Logic Converter



Ground Referenced Thermocouple in Single Supply System

absolute maximum ratings (Note 1)

Voltage at Any Pin	−0.3V to V_{CC} +0.3V
Operating Temperature Range	
MM54C909	−55°C to +125°C
MM74C909	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation (Notes 2 and 3)	500 mW
Operating V_{CC} Range	3.0V to 15V
Absolute Maximum V_{CC}	18V
Input Current ($V_{IN} < -0.3V$) (Note 4)	50 mA
Lead Temperature (Soldering, 10 seconds)	300°C

dc electrical characteristics

Min/max limits apply across temperature range, unless otherwise noted. (V_{CC} = +5.0 V_{DC})

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage (Note 9)				±9	mV
	T_A = 25°C		±2	±5	mV
Input Bias Current ($I_{IN(+)}$ or $I_{IN(-)}$) (Note 5)	T_A = 25°C, With Output in Linear Range		25	250	nA
				400	nA
Input Offset Current ($I_{IN(+)} - I_{IN(-)}$)				±150	nA
	T_A = 25°C		±5	±50	nA
Input Common Mode Voltage (Note 6)		0		V_{CC}−2	V
	T_A = 25°C	0		V_{CC}−1.5	V
Supply Current (I_{CC})	T_A = 25°C, $R_L = \infty$ On All Outputs		800	2000	µA
Voltage Gain	T_A = 25°C, $R_L \geq 15\ k\Omega$		200		V/mV
OUTPUT DRIVE (See 54C/74C Family Characteristics Data Sheet)					
Output Sink Current (I_{SINK}) MM54C909 MM74C909	V_{CC} = 4.50V V_{CC} = 4.75V, V_{OUT} = 0.4V $V_{IN(-)} \geq 1.0\ V_{DC}$ $V_{IN(+)} = 0\ V_{DC}$	1.6	3.2		mA
Output Leakage Current	$V_{IN(+)} \geq 1.0\ V_{DC}$, $V_{IN(-)} = 0\ V_{DC}$, $V_{OUT} = 15\ V_{DC}$			1	µA
	$V_{IN(+)} \geq 1.0\ V_{DC}$, $V_{IN(-)} = 0\ V_{DC}$, $V_{OUT} = 5\ V_{DC}$, T_A = 25°C		0.1		nA
Differential Input Voltage (Note 8)	All V_{IN}'s $\geq 0\ V_{DC}$			15	V

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: For operating at high temperatures, the MM74C909 must be derated based on +125°C maximum junction temperature and a thermal resistance of +175°C/W which applies to the device soldered in a printed circuit board, operating in a still air ambient. The MM54C909 must be derated based on a +150°C maximum junction temperature. The low bias dissipation and the ON-OFF characteristic of the outputs keeps the chip dissipation very small ($P_d \leq 100$ mW), provided the output sink current is within specified limits.

Note 3: Short circuits from the output to V^+ can cause excessive heating and eventual destruction. The maximum output current is approximately 20 mA independent of the magnitude of V^+.

Note 4: This input current will only exist when the voltage at any of the input leads is driven negative. There is a lateral NPN parasitic transistor action on the IC chip. The transistor action can cause the output voltages of the comparators to go to the V^+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will reestablish when the input voltage, which was negative, again returns to a value greater than −0.3V.

Note 5: The direction of the input current is out of the IC. This current is essentially constant, independent of the state of the output so no loading change exists on the reference or input lines.

Note 6: The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is $V^+ - 1.5V$, but either or both inputs can go to +15V without damage.

Note 7: The response time specified is for a 100 mV input step with 5.0 mV overdrive. For larger overdrive signals 300 ns can be obtained, see typical performance characteristics section.

Note 8: The positive excursions of the input can equal V_{CC} supply voltage level, and if the other input voltage remains within the common-mode voltage range, the comparator will provide a proper output state. The low input voltage state must not be less than −0.3V.

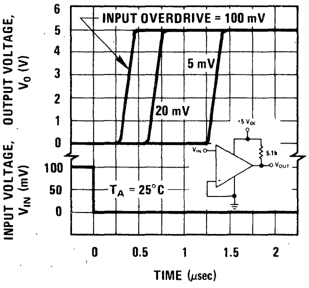
Note 9: At output switch point, $V_O = 1.4\ V_{DC}$, $R_S = 0\Omega$ with V^+ from 5 V_{DC} to 30 V_{DC} and over the full input common mode range (0V_{DC}) to $V^+ \pm 1.5\ V_{DC}$).

ac electrical characteristics $R_L = 5.1\ k\Omega$, $V_{RL} = 5.0\ V_{DC}$, unless otherwise specified.

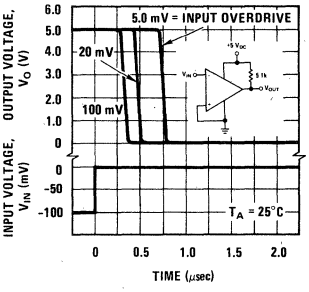
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Large Signal Response Time	V_{IN} = TTL Swing $V_{REF} = 1.4\ V_{DC}$		300		ns
Response Time	$T_A = 25°C$		1.3		μs

typical performance characteristics

Response Time for Various Input Overdrives — Positive Transition



Response Time for Various Input Overdrives — Negative Transition



application hints

The MM54C909/MM74C909 is a high gain, wide bandwidth device; which, like most comparators, can easily oscillate if the output lead is inadvertently allowed to capacitively couple to the inputs via stray capacitance. This shows up only during the output voltage transition intervals as the comparator changes states. Power supply bypassing is not required to solve this problem. Standard PC board layout is helpful as it reduces stray input-output coupling. Reducing the input resistors to <10 kΩ reduces the feedback signal levels and finally, adding even a small amount (1 to 10 mV) of positive feedback (hysteresis) causes such a rapid transition that oscillations due to stray feedback are not possible. Simply socketing the I/C and attaching resistors to the pins will cause input-output oscillations during the small transition intervals unless hysteresis is used. If the input signal is a pulse waveform, with relatively fast rise and fall times, hysteresis is not required.

All pins of any unused comparators should be grounded.

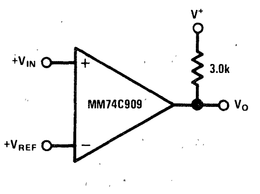
The bias network of the MM54C909/MM74C909 establishes an I_{CC} current which is independent of the magnitude of the power supply voltage over the range of from 3.0V to 15V.

It is usually unnecessary to use a bypass capacitor across the power supply line.

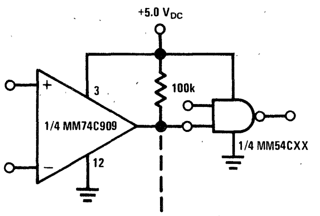
The differential input voltage may be larger than V^+ without damaging the device. Protection should be provided to prevent the input voltages from going negative more than $-0.3\ V_{DC}$ (at 25°C). An input clamp diode and input resistor can be used as shown in the applications section.

Many outputs can be tied together to provide an output OR'ing function. An output "pull-up" resistor can be connected to any available power supply voltage within the permitted supply voltage range and there is no restriction on this voltage due to the magnitude of the voltage which is applied to the V^+ terminal of the MM54C909/MM74C909 package. The output can also be used as a simple SPST switch to ground (when a "pull-up" resistor is not used). The amount of current which the output device can sink is limited by the drive available (which is independent of V^+) and the gain of the output device. When the maximum current limit is reached (approximately 16 mA), the output transistor will come out of saturation and the output voltage will rise very rapidly.

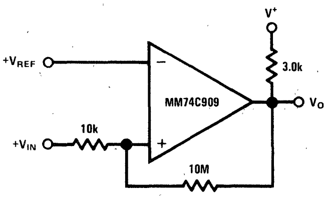
typical applications (con't) ($V^+ = 5.0\ V_{DC}$)



Basic Comparator

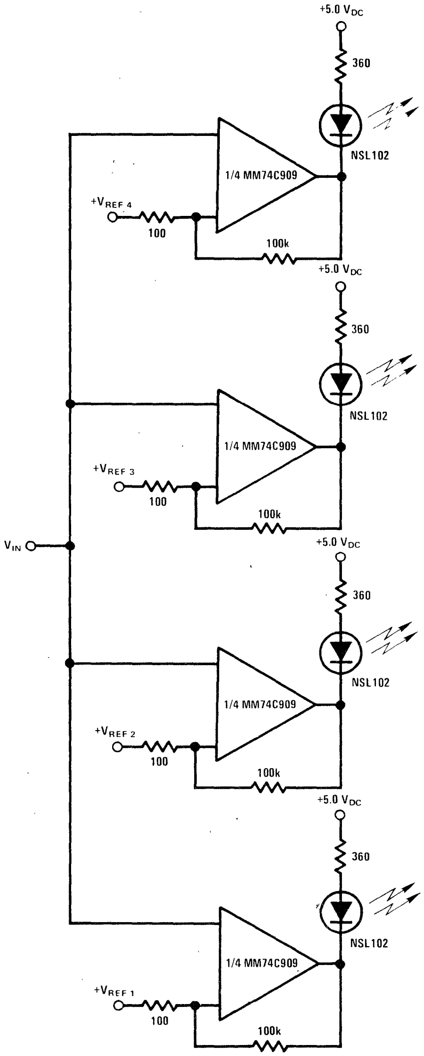


Driving CMOS

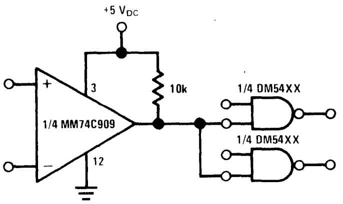


Non-Inverting Comparator with Hysteresis

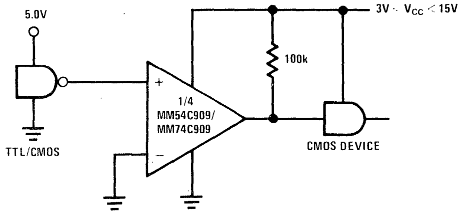
typical applications (con't) ($V^+ = 5.0\ V_{DC}$)



Visible Voltage Indicator

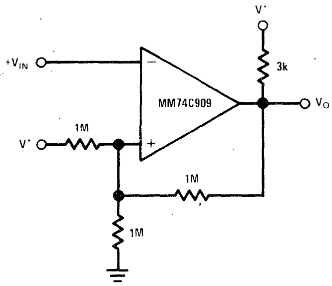


Driving TTL

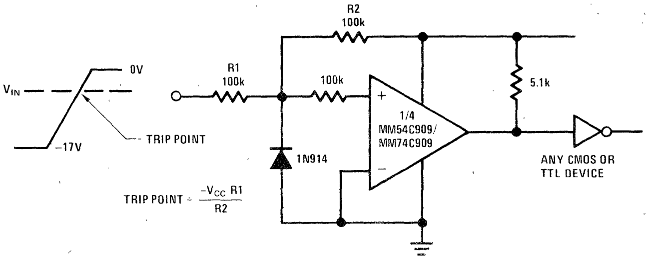


Note: For inverting buffer reverse input connection.

5V Logic to CMOS Operating at $V_{CC} \neq 5V$



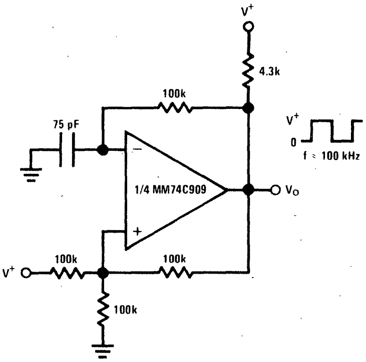
Inverting Comparator with Hysteresis



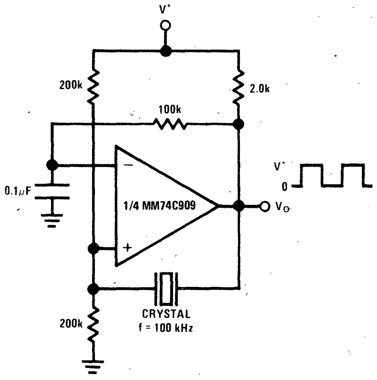
Note For non-inverting buffer reverse input connection

Hi Voltage Inverting PMOS to CMOS or TTL

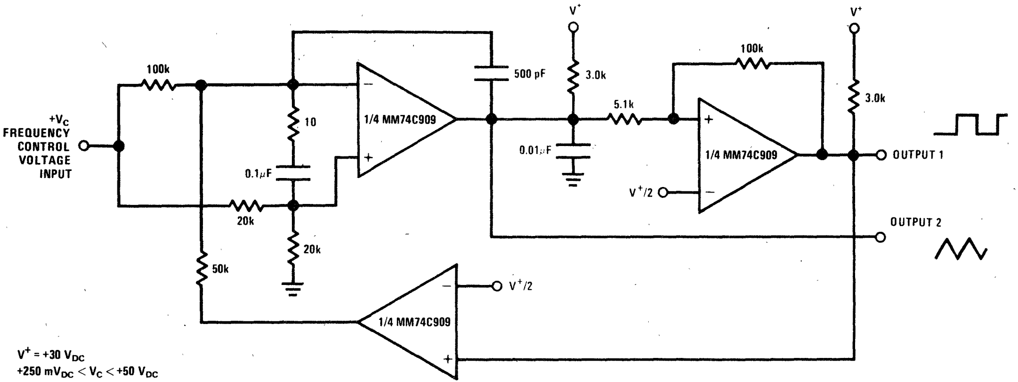
typical applications (con't) $(V^+ = 5.0\ V_{DC})$



Squarewave Oscillator

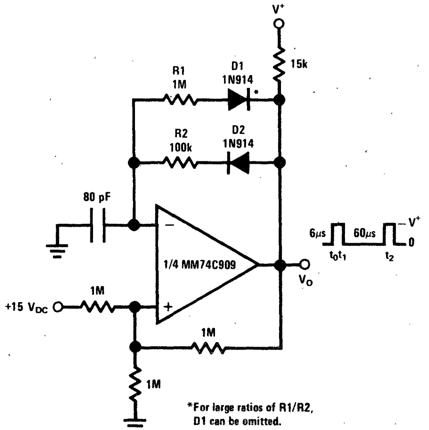


Crystal Controlled Oscillator



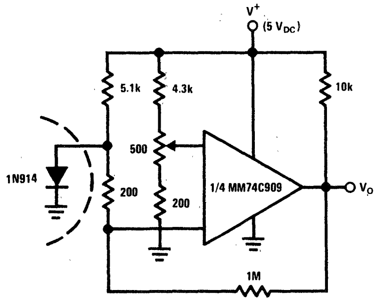
$V^+ = +30\ V_{DC}$
$+250\ mV_{DC} < V_C < +50\ V_{DC}$
$700\ Hz < f_O < 100\ kHz$

Two-Decade High-Frequency VCO



*For large ratios of R1/R2, D1 can be omitted.

Pulse Generator



Remote Temperature Sensing

Advance Information

MM54C910/MM74C910 256-bit TRI-STATE® random access read/write memory

general description

The MM54C910/MM74C910 is a 64 word by 4 bit random access memory. Inputs consist of six address lines, four data input lines, a write enable, and a memory enable line. The six address lines are internally decoded to select one of 64 word locations. An internal address register, latches the address information on the positive to negative transition of memory enable. The TRI-STATE outputs allow for easy memory expansion. This circuit operates on a 3 to 5V power supply.

Address Operation: Address inputs must be stable t_{SA} prior to the positive to negative transition of memory enable, and t_{HA} after the positive to negative transition of memory enable. The address register holds the information and stable address inputs are not needed at any other time.

Write Operation: Data is written into memory at the selected address if write enable goes low while memory enable is low. Write enable must be held low for $t_{\overline{WE}}$ and data must remain stable t_{HD} after write enable returns high.

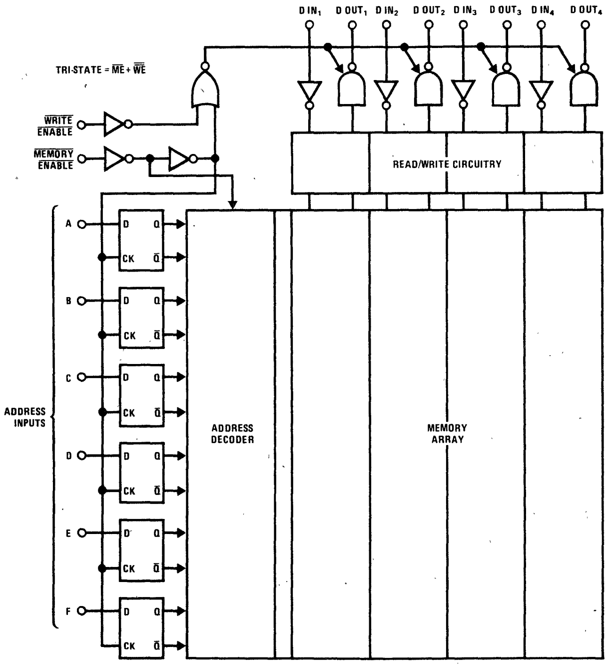
Read Operation: Data is nondestructively read from a memory location by an address operation with write enable held high.

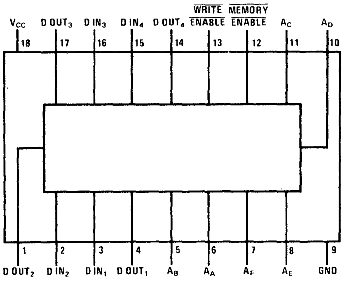
Outputs are in the TRI-STATE (Hi-Z) condition when the device is writing or disabled.

features

■ Supply voltage range	3V to 6V
■ High noise immunity	0.45 V_{CC} typ
■ TTL compatible fan out	1 TTL load
■ Input address register	
■ Low power consumption	200 nW/ package
■ Fast access time	300 ns typ at 5V
■ TRI-STATE outputs	

logic and connection diagrams

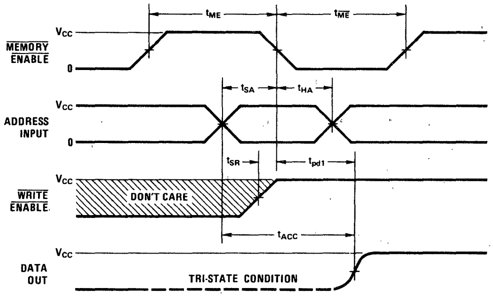




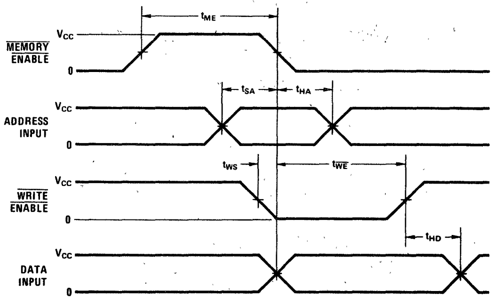
TOP VIEW

switching time waveforms

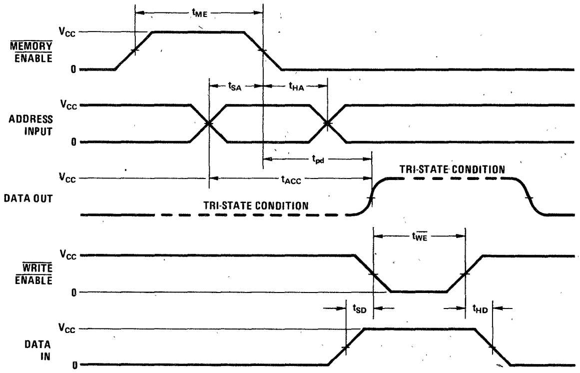
Read Cycle



Write Cycle



Read Modify Write Cycle



NOTE: $t_r = 60$ ns
$t_f = 10$ ns

truth table

$\overline{\text{ME}}$	$\overline{\text{WE}}$	OPERATION	OUTPUTS
L	L	Write	TRI-STATE
L	H	Read	Data
H	L	Inhibit, Store	TRI-STATE
H	H	Inhibit, Store	TRI-STATE

MM54C914/MM74C914 hex schmitt trigger

general description

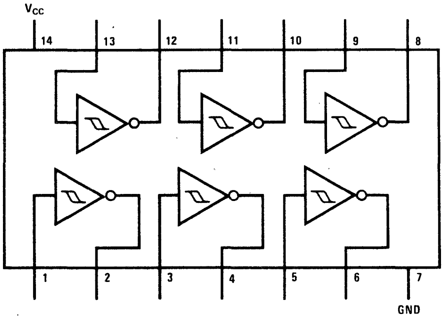
The MM54C914/MM74C914 is a monolithic CMOS Hex Schmitt trigger with special input protection scheme. This scheme allows the input voltage levels to exceed V_{CC} or ground by at least 25V, and is valuable for applications involving voltage level shifting or mismatched power supplies.

The positive and negative-going threshold voltages, V_{T+} and V_{T-}, show low variation with respect to temperature (typ 0.005 V/°C at V_{CC} = 10V). And the hysteresis, $V_{T+} - V_{T-} \geq 0.2\ V_{CC}$ is guaranteed.

features

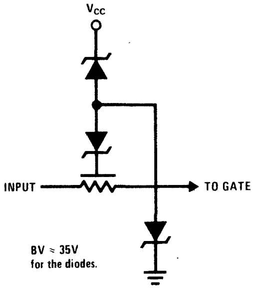
■ Hysteresis	0.4 V_{CC} typ 0.2 V_{CC} guaranteed
■ Special input protection	Extended Input Voltage Range
■ Wide supply voltage range	3.0V to 15V
■ High noise immunity	0.70 V_{CC} typ
■ Low power TTL compatibility	fan out of 2 driving 74L

connection diagram



TOP VIEW

Special Input Protection



absolute maximum ratings

Voltage at Any Input Pin	V_{CC} −25V to V_{CC} +25V
Voltage at Any Other Pin	−0.3V to V_{CC} +0.3V
Operating Temperature Range	
MM54C914	−55°C to +125°C
MM74C914	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500 mW
Operating V_{CC} Range	3.0V to 15V
Absolute Maximum V_{CC}	16V
Lead Temperature (Soldering, 10 seconds)	300°C

dc electrical characteristics

Min/max limits apply across temperature range, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CMOS TO CMOS					
V_{T+} Positive Going Threshold Voltage	V_{CC} = 5V	3.0	3.6	4.3	V
	V_{CC} = 10V	6.0	6.8	8.6	V
	V_{CC} = 15V	9.0	10.0	12.9	
V_{T-} Negative Going Threshold Voltage	V_{CC} = 5V	0.7	1.4	2.0	V
	V_{CC} = 10V	1.4	3.2	4.0	V
	V_{CC} = 15V	2.1	5.0	6.0	
Hysteresis ($V_{T+} - V_{T-}$)	V_{CC} = 5V	1.0	2.2	3.6	V
	V_{CC} = 10V	2.0	3.6	7.2	V
	V_{CC} = 15V	3.0	5.0	10.8	V
Logical "1" Output Voltage ($V_{OUT(1)}$)	V_{CC} = 5V, I_O = −10μA	4.5			V
	V_{CC} = 10V, I_O = −10μA	9.0			V
Logical "0" Output Voltage ($V_{OUT(0)}$)	V_{CC} = 5V, I_O = +10μA			0.5	V
	V_{CC} = 10V, I_O = +10μA			1.0	V
Logical "1" Input Current ($I_{IN(1)}$)	V_{CC} = 15V, V_{IN} = 15V		0.005	5.0	μA
Logical "0" Input Current ($I_{IN(0)}$)	V_{CC} = 15V, V_{IN} = −10V	−100.0	−0.005		μA
Supply Current (I_{CC})	V_{CC} = 15V, V_{IN} = −10V/25V		0.05	300	μA
	V_{CC} = 5V, V_{IN} = 2.5V (Note 4)		20		μA
	V_{CC} = 10V, V_{IN} = 5V (Note 4)		200		μA
	V_{CC} = 15V, V_{IN} = 7.5V (Note 4)		600		μA
CMOS/LPTTL INTERFACE					
Logical "1" Input Voltage ($V_{IN(1)}$)	V_{CC} = 5V	4.3			V
Logical "0" Input Voltage ($V_{IN(0)}$)	V_{CC} = 5V			0.7	V
Logical "1" Output Voltage ($V_{OUT(1)}$)	54C, V_{CC} = 4.5V, I_O = −360μA	2.4			V
	74C, V_{CC} = 4.75V, I_O = −360μA	2.4			V
Logical "0" Output Voltage ($V_{OUT(0)}$)	54C, V_{CC} = 4.5V, I_O = 360μA			0.4	V
	74C, V_{CC} = 4.75V, I_O = 360μA			0.4	V
OUTPUT DRIVE (See 54C/74C Family Characteristics Data Sheet)					
Output Source Current (I_{SOURCE}) (P-Channel)	V_{CC} = 5V, V_{OUT} = 0V, T_A = 25°C	−1.75	−3.3		mA
Output Source Current (I_{SOURCE}) (P-Channel)	V_{CC} = 10V, V_{OUT} = 0V, T_A = 25°C	−8.0	−15		mA
Output Sink Current (I_{SINK}) (N-Channel)	V_{CC} = 5V, V_{OUT} = V_{CC}, T_A = 25°C	1.75	3.6		mA
Output Sink Current (I_{SINK}) (N-Channel)	V_{CC} = 10V, V_{OUT} = V_{CC}, T_A = 25°C	8.0	16		mA

ac electrical characteristics $T_A = 25°C$, $C_L = 50$ pF, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Propagation Delay from Input to Output (t_{pd0} or t_{pd1})	$V_{CC} = 5V$		220	400	ns
	$V_{CC} = 10$		80	200	ns
Input Capacitance	Any Input (Note 2)		5.0		pF
Power Dissipation Capacitance (C_{PD})	(Note 3) Per Gate		20		pF

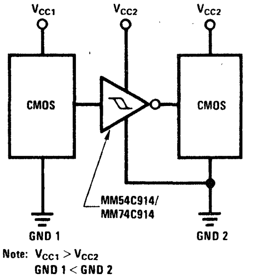
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note, AN-90.

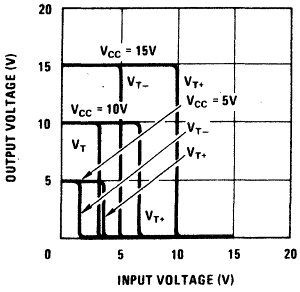
Note 4: Only one input is at 1/2 V_{CC}, the others are either at V_{CC} or GND.

typical application

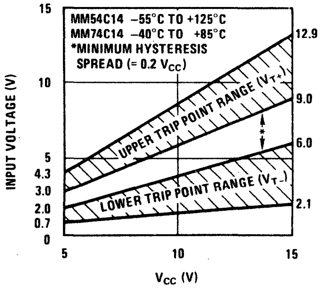


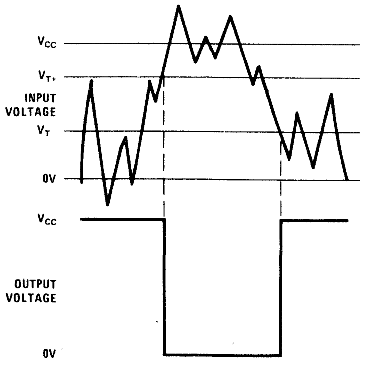
typical performance characteristics

Typical Transfer Characteristics



Guaranteed Trip Point Range





Advance Information

MM54C925/MM74C925, MM54C926/MM74C926, MM54C927/MM74C927, MM54C928/MM74C928

4-digit counter with multiplexed 7-segment output drivers

general description

These CMOS counters consist of a 4-digit counter, an internal output latch, NPN output sourcing drivers for a 7-segment display, and internal multiplexing circuitry with 4 multiplexing outputs. The counters have a reset and count on the negative edge of clock. The multiplexing circuit has its own free running oscillator and requires no external clock. This circuit operates on a 3 to 5V power supply.

The MM54C925/MM74C925 is a 4-decade counter and has Latch Enable, Clock and Reset inputs.

The MM54C926/MM74C926 is like the MM54C925/MM74C925 except that it has a Carry Out used for cascading counters, and it has a Display Select that allows the user to select whether the number in the latch or the number in the counter is displayed.

The MM54C927/MM74C927 is like the MM54C926/MM74C926 except the second most significant digit divides by 6 rather than 10. Thus, if the clock input frequency was 10 Hz, the display would read tenths of seconds, seconds, tens of seconds, and minutes (i.e. 9:59.9).

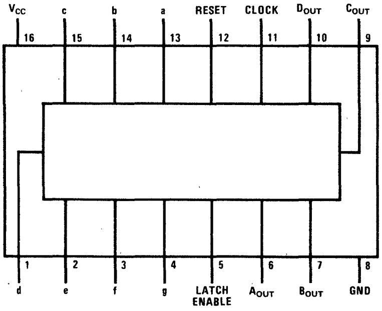
The MM54C928/MM74C928 is like the MM54C926/MM74C926 except the most significant digit, divides by 2 rather than 10 and the Carry Out is an overflow indicator. Thus, this is a "3 1/2 digit counter."

features

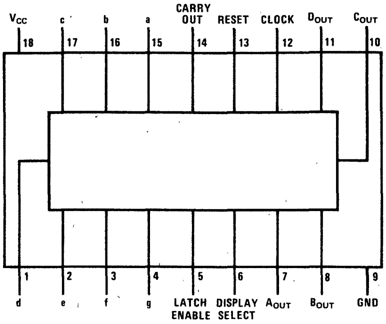
■ Supply range	3.0V to 6.0V
■ Guaranteed noise margin	1.0V
■ High noise immunity	0.45 typ
■ High segment sourcing current	40 mA @ V_{CC} −1.6V
■ Internal multiplexing circuitry	

connection diagrams

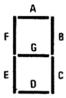
MM54C925/MM74C925



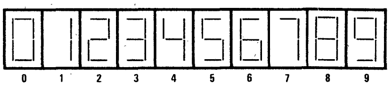
MM54C926/MM74C926, MM54C927/MM74C927, MM54C928/MM74C928



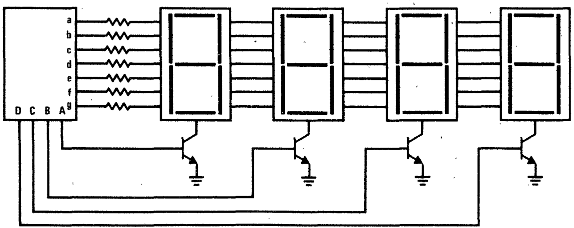
Segment Identification



Display



typical application



MM70C95/MM80C95, MM70C97/MM80C97 TRI-STATE® hex non-inverting buffers

general description

These gates are monolithic complementary MOS (CMOS) integrated circuits constructed with N and P-channel enhancement mode transistors. Each of the devices are used to convert CMOS or TTL outputs to TRI-STATE® outputs with no logic inversion. The MM70C95/MM80C95 has common TRI-STATE controls for all six buffers. The MM70C97/MM80C97 has two TRI-STATE controls, one for two buffers and one for the other four.

Inputs are protected from damage due to static discharge by diode clamps to V_{CC} and GND.

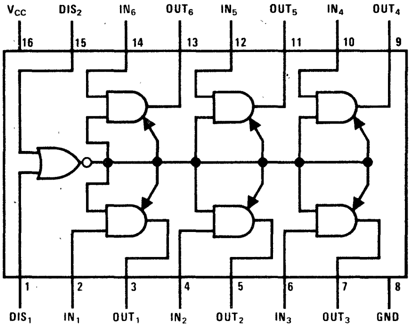
features

■ Wide supply voltage range	3.0V to 15V
■ Guaranteed noise margin	1.0V
■ High noise immunity	0.45 V_{CC} (typ)
■ TTL compatible	Drive 1 TTL load

applications

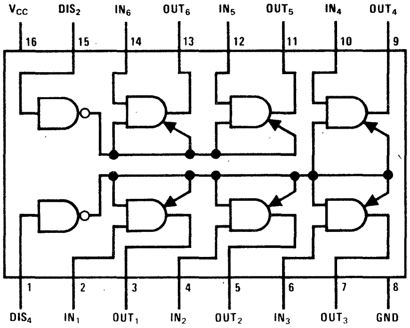
■ Bus drivers	typical propagation delay into a 150 pF load is 40 ns

connection diagrams



TOP VIEW

MM70C95/MM80C95



TOP VIEW

MM70C97/MM80C97

truth tables

MM70C95/MM80C95

DISABLE INPUT		INPUT	OUTPUT
DIS_1	DIS_2		
0	0	0	0
0	0	1	1
0	1	X	H-z
1	0	X	H-z
1	1	X	H-z

MM70C97/MM80C97

DISABLE INPUT		INPUT	OUTPUT
DIS_4	DIS_2		
0	0	0	0
0	0	1	1
X	1	X	H-z*
1	X	X	H-z**

*Output 5-6 only

**Output 1-4 only

X = Irrelevant

absolute maximum ratings (Note 1)

Voltage at Any Pin	-0.3V to V_{CC} +0.3V	Storage Temperature Range	-65°C to +150°C
Operating Temperature Range		Package Dissipation	500 mW
MM70C95, MM70C97	-55°C to +125°C	Power Supply Voltage, V_{CC}	16V
MM80C95, MM80C97	-40°C to +85°C	Lead Temperature (Soldering, 10 seconds)	300°C

dc electrical characteristics Min/max limits apply across temperature range unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CMOS TO CMOS					
Logical "1" Input Voltage ($V_{IN(1)}$)	V_{CC} = 5.0V	3.5			V
	V_{CC} = 10V	8.0			V
Logical "0" Input Voltage ($V_{IN(0)}$)	V_{CC} = 5.0V			1.5	V
	V_{CC} = 10V			2.0	V
Logical "1" Output Voltage ($V_{OUT(1)}$)	V_{CC} = 5.0V	4.5			V
	V_{CC} = 10V	9.0			V
Logical "0" Output Voltage ($V_{OUT(0)}$)	V_{CC} = 5.0V			0.5	V
	V_{CC} = 10V			1.0	V
Logical "1" Input Current ($I_{IN(1)}$)	V_{CC} = 15V		0.005	1.0	μA
Logical "0" Input Current ($I_{IN(0)}$)		1.0	-0.005		μA
Output Current in High Impedance State	V_{CC} = 15V, V_O = 15V		0.005	1.0	μA
	V_{CC} = 15V, V_O = 0V	1.0	-0.005		μA
Supply Current (I_{CC})	V_{CC} = 15V		0.01	15	μA
TTL INTERFACE					
Logical "1" Input Voltage ($V_{IN(1)}$)	70C V_{CC} = 4.5V	V_{CC} - 1.5			V
	80C V_{CC} = 4.75V	V_{CC} - 1.5			V
Logical "0" Input Voltage ($V_{IN(0)}$)	70C V_{CC} = 4.5V			0.8	V
	80C V_{CC} = 4.75V			0.8	V
Logical "1" Output Voltage ($V_{OUT(1)}$)	70C V_{CC} = 4.5V, I_O = -1.6 mA	2.4			V
	80C V_{CC} = 4.75V, I_O = -1.6 mA	2.4			V
Logical "0" Output Voltage ($V_{OUT(0)}$)	70C V_{CC} = 4.5V, I_O = 1.6 mA			0.4	V
	80C V_{CC} = 4.75V, I_O = 1.6 mA			0.4	V
OUTPUT DRIVE CURRENT					
Output Source Current (I_{SOURCE})	V_{CC} = 5.0V, $V_{IN(1)}$ = 5.0V T_A = 25°C, V_{OUT} = 0V	4.35			mA
Output Source Current (I_{SOURCE})	V_{CC} = 10V, $V_{IN(1)}$ = 10V T_A = 25°C, V_{OUT} = 0V	20			mA
Output Sink Current (I_{SINK})	V_{CC} = 5.0V, $V_{IN(0)}$ = 0V T_A = 25°C, V_{OUT} = V_{CC}	4.35			mA
Output Sink Current (I_{SINK})	V_{CC} = 10V, V_{IN} = 0V T_A = 25°C, V_{OUT} = V_{CC}	20			mA

ac electrical characteristics T_A = 25°C, C_L = 50 pF, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Capacitance	Any Input (Note 2)		5.0		pF
Output Capacitance TRI-STATE (C_{OUT})	Any Output (Note 2)		9.0		pF
Power Dissipation Capacity (C_{pd})	(Note 3)		60		pF
Propagation Delay Time to a Logical "0" (t_{pd0}) or Logical "1" (t_{pd1}) From Data Input to Output	V_{CC} = 5.0V		60	100	ns
	V_{CC} = 10V		25	40	ns
Delay From Disable Input to High Impedance State (From Logical "1" or Logical "0" Level)(t_{1H}, t_{0H}) MM70C95/MM80C95	V_{CC} = 5.0V, C_L = 5.0 pF, R_L = 10k		80	135	ns
	V_{CC} = 10V, C_L = 5.0 pF, R_L = 10k		50	90	ns
Delay From Disable Input to Logical "1" Level (t_{H1}) or to Logical "0" Level (t_{H0})(From High Impedance State) MM70C95/MM80C95	V_{CC} = 5.0V, C_L = 50 pF, R_L = 10k		120	200	ns
	V_{CC} = 10V, C_L = 50 pF, R_L = 10k		50	90	ns
Delay From Disable Input to High Impedance State (From Logical "1" or Logical "0" Level) (t_{1H}, t_{0H})MM70C97/MM80C97	V_{CC} = 5.0V, R_L = 10k		70	125	ns
	V_{CC} = 10V, R_L = 10k		50	90	ns
Delay From Disable Input to Logical "1" Level (t_{H1}) or to Logical "0" Level (t_{H0})(From High Impedance State) MM70C97/MM80C97	V_{CC} = 5.0V, R_L = 10k		95	175	ns
	V_{CC} = 10V, R_L = 10k		40	80	ns
Propagation Delay Time to a Logical "0" (t_{pd0}) or Logical "1" (t_{pd1}) From Data Input to Output	V_{CC} = 5.0V, C_L = 150 pF, T_A = 25°C		85	160	ns
	V_{CC} = 10V, C_L = 150 pF, T_A = 25°C		40	80	ns

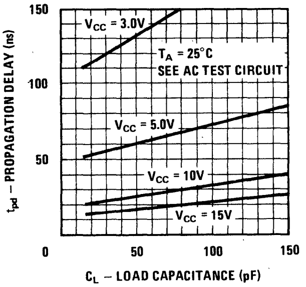
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

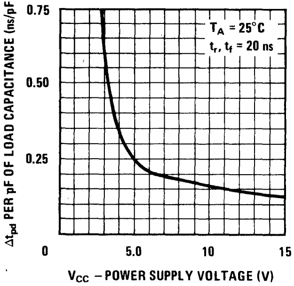
Note 3: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note, AN-90.

typical performance characteristics

Propagation Delay vs Load Capacitance

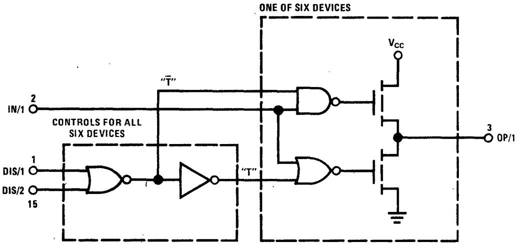


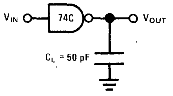
Δt_{pd}/pF vs Power Supply Voltage



ac test circuits and switching time waveforms

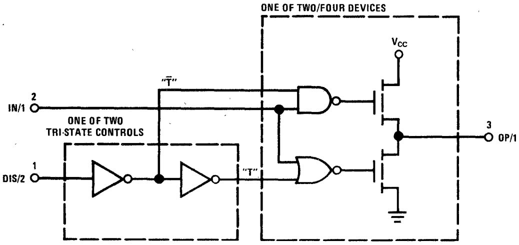
MM70C95/MM80C95 TRI-STATE



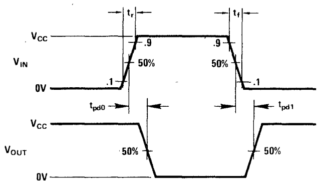


(For TRI-STATE® Parameters)

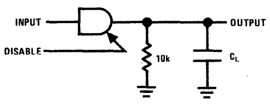
MM70C97/MM80C97



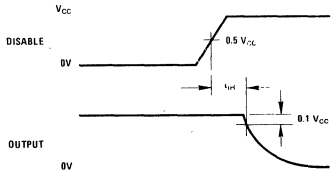
CMOS to CMOS



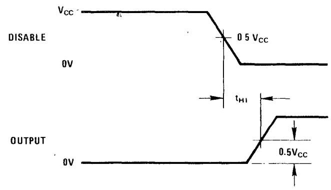
t_{1H} and t_{H1}



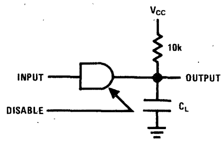
t_{1H}



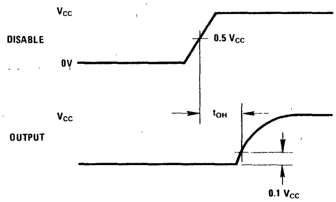
t_{H1}



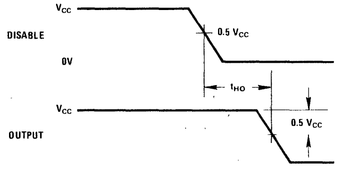
t_{0H} and t_{H0}



t_{0H}



t_{H0}



Note: Delays measured with input t_r, $t_f \leq 20$ ns.

MM78C29/MM88C29 quad single ended line driver
MM78C30/MM88C30 dual differential line driver

general description

The MM78C30/MM88C30 is a dual differential line driver that also performs the dual four-input NAND or dual four-input AND function. The absence of a clamp diode to V_{CC} in the input protection circuitry allows a CMOS user to interface systems operating at different voltage levels. Thus, a CMOS digital signal source can operate at a V_{CC} voltage greater than the V_{CC} voltage of the MM78C30 line driver. The differential output of the MM78C30/MM88C30 eliminates ground-loop errors.

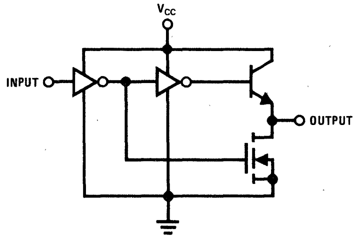
The MM78C29/MM88C29 is a non-inverting single-wire transmission line driver with a similar input protection circuit. And since the output ON resistance is a low 20Ω typ, the device can be used to drive lamps, relays, solenoids, and clock lines, besides driving data lines.

features

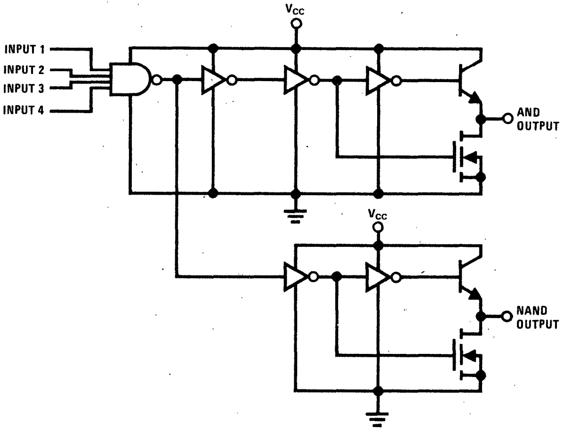
■ Wide supply voltage range	3.0V to 15V
■ High noise immunity	0.45 V_{CC} typ
■ Low output ON resistance	20Ω typ

logic and connection diagrams

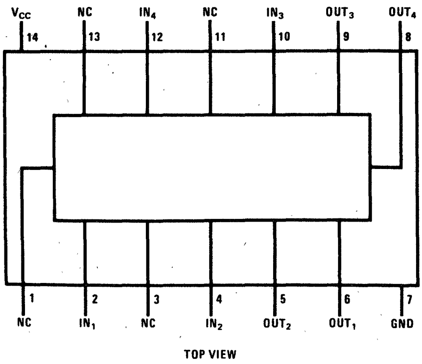
1/4 MM78C29/MM88C29



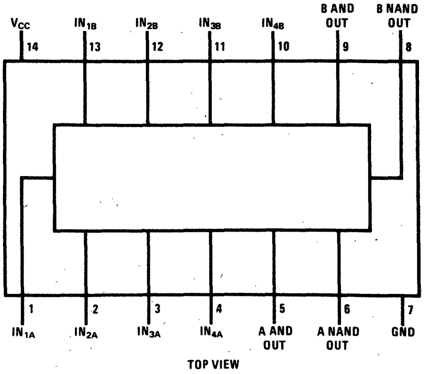
1/2 MM78C30/MM88C30



MM78C29/MM88C29



MM78C30/MM88C30



absolute maximum ratings (Note 1)

Voltage at Any Pin	−0.3V to +16V
Operating Temperature Range	
MM78C29/MM78C30	−55°C to +125°C
MM88C29/MM88C30	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500 mW
Operating V_{CC} Range	3.0V to 15V
Absolute Maximum V_{CC}	16V
Average Current at V_{CC} and Ground	100 mA
Average Current at Output	
MM78C30/MM88C30	50 mA
MM78C29/MM88C29	25 mA
Maximum Junction Temperature, T_j	150°C
Lead Temperature (Soldering, 10 seconds)	300°C

dc electrical characteristics Min/max limits apply across temperature range, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CMOS TO CMOS					
Logical "1" Input Voltage ($V_{IN(1)}$)	V_{CC} = 5.0V	3.5			V
	V_{CC} = 10V	8.0			V
Logical "0" Input Voltage ($V_{IN(0)}$)	V_{CC} = 5.0V			1.5	V
	V_{CC} = 10V			2.0	V
Logical "1" Input Current ($I_{IN(1)}$)	V_{CC} = 15V, V_{IN} = 15V		0.005	1.0	µA
Logical "0" Input Current ($I_{IN(0)}$)	V_{CC} = 15V, V_{IN} = 0V	−1.0	−0.005		µA
Supply Current (I_{CC})	V_{CC} = 15V		0.05	100	µA
OUTPUT DRIVE (See 54C/74C Family Characteristics Data Sheet)					
Output Source Current					
MM78C29/MM78C30	V_{OUT} = V_{CC} −1.6V,				
	$V_{CC} \geq 4.5V$, T_j = 25°C	57	80		mA
	T_j = 125°C	32	50		mA
MM88C29/MM88C30	V_{OUT} = V_{CC} −1.6V,				
	$V_{CC} \geq 4.75V$, T_j = 25°C	47	80		mA
	T_j = 85°C	32	60		mA
Output Sink Current					
MM78C29/MM78C30	V_{OUT} = 0.4V, V_{CC} = 4.50V				
	T_j = 25°C	11	20		mA
	T_j = 125°C	8	14		mA
	V_{OUT} = 0.4V, V_{CC} = 10V				
	T_j = 25°C	22	40		mA
	T_j = 125°C	16	28		mA
MM88C29/MM88C30	V_{OUT} = 0.4V, V_{CC} = 4.75V				
	T_j = 25°C	9.5	22		mA
	T_j = 85°C	8	18		mA
	V_{OUT} = 0.4V, V_{CC} = 10V				
	T_j = 25°C	19	40		mA
	T_j = 85°C	15.5	33		mA
Output Source Resistance					
MM78C29/MM78C30	V_{OUT} = V_{CC} −1.6V,				
	$V_{CC} \geq 4.5V$, T_j = 25°C		20	28	Ω
	T_j = 125°C		32	50	Ω
MM88C29/MM88C30	V_{OUT} = V_{CC} −1.6V,				
	$V_{CC} \geq 4.75V$, T_j = 25°C		20	34	Ω
	T_j = 85°C		27	50	Ω

dc electrical characteristics (con't)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output Sink Resistance					
MM78C29/MM78C30	$V_{OUT} = 0.4V$, $V_{CC} = 4.5V$				
	$T_j = 25°C$		20	36	Ω
	$T_j = 125°C$		28	50	Ω
	$V_{OUT} = 0.4V$, $V_{CC} = 10V$				
	$T_j = 25°C$		10	18	Ω
	$T_j = 125°C$		14	25	Ω
MM88C29/MM88C30	$V_{OUT} = 0.4V$, $V_{CC} = 4.75V$				
	$T_j = 25°C$		18	41	Ω
	$T_j = 85°C$		22	50	Ω
	$V_{OUT} = 0.4V$, $V_{CC} = 10V$				
	$T_j = 25°C$		10	21	Ω
	$T_j = 85°C$		12	26	Ω
Output Resistance Temperature Coefficient					
Source			0.55		%/°C
Sink			0.40		%/°C
Thermal Resistance, θ_{jA}					
MM78C29/MM78C30 (D-Package)			100		°C/W
MM88C29/MM88C30 (N-Package)			150		°C/W

ac electrical characteristics $T_A = 25°C$, $C_L = 50\ pF$

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Propagation Delay Time to Logical "1" or "0" (t_{pd})	*(See Figure 2)*				
MM78C29/MM88C29	$V_{CC} = 5V$		80	200	ns
	$V_{CC} = 10V$		35	10	ns
MM78C30/MM88C30	$V_{CC} = 5V$		110	350	ns
	$V_{CC} = 10V$		50	150	ns
Power Dissipation Capacitance (C_{PD})					
MM78C29/MM88C29	(Note 3)		150		pF
MM78C30/MM88C30	(Note 3)		200		pF
Input Capacitance (C_{IN})					
MM78C29/MM88C29	(Note 2)		5.0		pF
MM78C30/MM88C30	(Note 2)		5.0		pF
Differential Propagation Delay Time to Logical "1" or "0"	$R_L = 100Ω$, $C_L = 5000\ pF$ *(See Figure 1)*				
MM78C30/MM88C30	$V_{CC} = 5V$			400	ns
	$V_{CC} = 10V$			150	ns

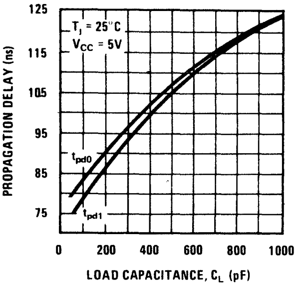
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

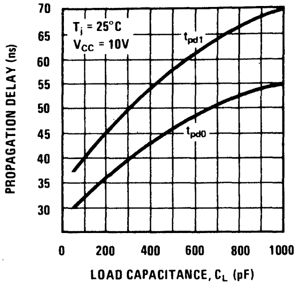
Note 3: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note, AN-90.

typical performance characteristics

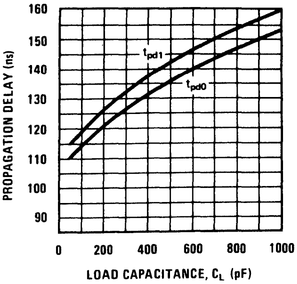
MM78C29/MM88C29
Typical Propagation Delay vs Load Capacitance



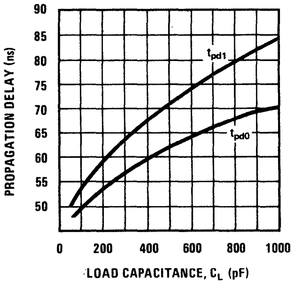
MM78C29/MM88C29
Typical Propagation Delay vs Load Capacitance



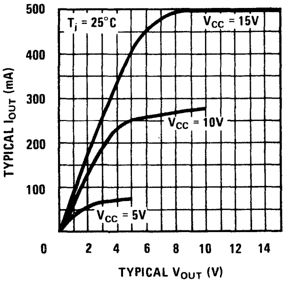
MM78C30/MM88C30
Typical Propagation Delay vs Load Capacitance



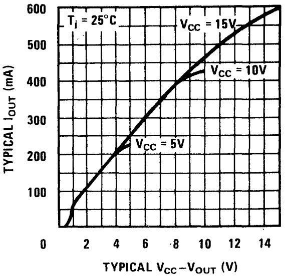
MM78C30/MM88C30
Typical Propagation Delay vs Load Capacitance



Typical Sink Current vs Output Voltage



Typical Source Current vs Output Voltage



ac test circuits

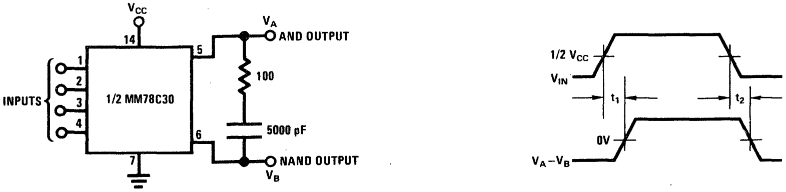


FIGURE 1.

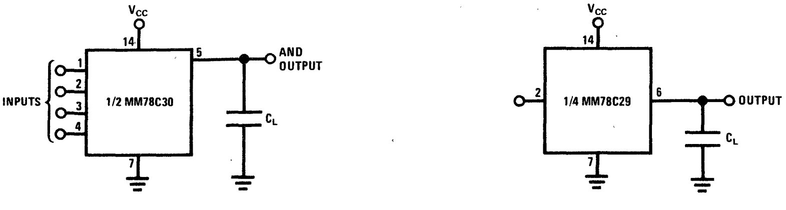
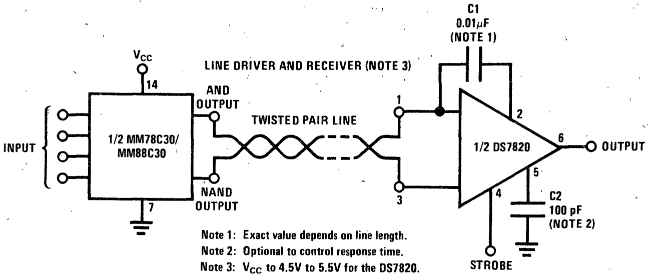


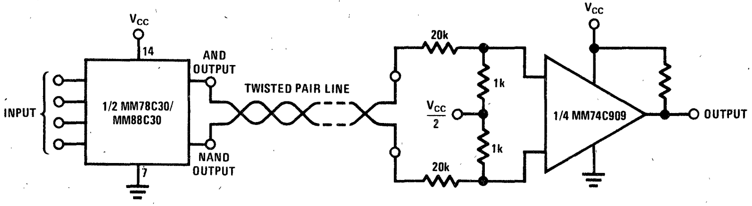
FIGURE 2.

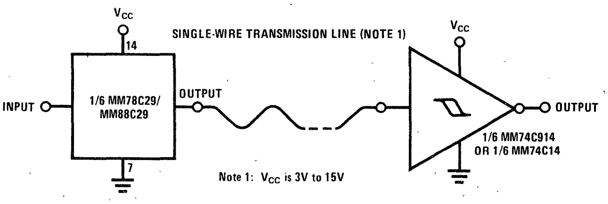
typical applications

Digital Data Transmission



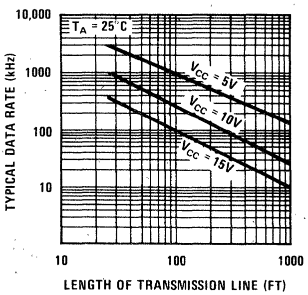
Note 1: Exact value depends on line length.
Note 2: Optional to control response time.
Note 3: V_{CC} to 4.5V to 5.5V for the DS7820.





Note 1: V_{CC} is 3V to 15V

Typical Data Rate vs Transmission Line Length



Note 1: The transmission line used was #22 guage unshielded twisted pair (40k termination).

Note 2: The curves generated assume that both drivers are driving equal lines, and that the maximum power is 500 mW/package.

CD4001M/CD4001C quadruple 2-input NOR gate

general description

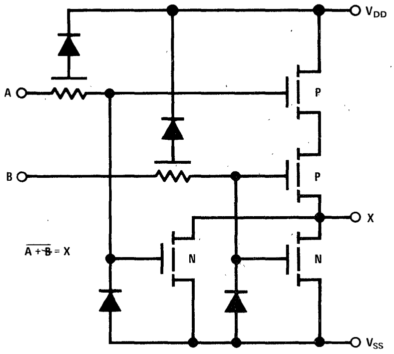
The CD4001M/CD4001C is a monolithic complementary MOS (CMOS) quadruple two-input NOR gate integrated circuit. N and P-channel enhancement mode transistors provide a symmetrical circuit with output swings essentially equal to the supply voltage. This results in high noise immunity over a wide supply voltage range. No dc power other than that caused by leakage current is consumed during static conditions.

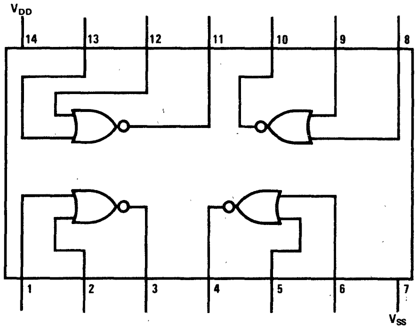
All inputs are protected against static discharge and latching conditions.

features

■ Wide supply voltage range	3V to 15V
■ Low power	10 nW (typ)
■ High noise immunity	0.45 V_{DD} (typ)

schematic and connection diagrams





TOP VIEW

absolute maximum ratings

Voltage at Any Pin (Note 1)	V_{SS} – 0.3V to V_{DD} + 0.3V
Operating Temperature Range	
CD4001M	–55°C to +125°C
CD4001C	–40°C to +85°C
Storage Temperature Range	–65°C to +150°C
Package Dissipation	500 mW
Operating V_{DD} Range	V_{SS} + 3.0V to V_{SS} + 15V
Lead Temperature (Soldering, 10 seconds)	300°C

dc electrical characteristics CD4001M

PARAMETER	CONDITIONS	LIMITS									UNITS
		–55°C			25°C			125°C			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Quiescent Device Current (I_L)	V_{DD} = 5V			0.05		0.001	0.05			3	μA
	V_{DD} = 10V			0.1		0.001	0.1			6	μA
Quiescent Device Dissipation/Package (P_D)	V_{DD} = 5V			0.25		0.005	0.25			15	μW
	V_{DD} = 10V			1		0.01	1			60	μW
Output Voltage Low Level (V_{OL})	V_{DD} = 5V, V_I = V_{DD}, I_O = 0A			0.01		0	0.01			0.05	V
	V_{DD} = 10V, V_I = V_{DD}, I_O = 0A			0.01		0	0.01			0.05	V
Output Voltage High Level (V_{OH})	V_{DD} = 5V, V_I = V_{SS}, I_O = 0A	4.99			4.99	5		4.95			V
	V_{DD} = 10V, V_I = V_{SS}, I_O = 0A	9.99			9.99	10		9.95			V
Noise Immunity (V_{NL}) (All Inputs)	V_{DD} = 5V, V_O = 3.6V, I_O = 0A	1.5			1.5	2.25		1.4			V
	V_{DD} = 10V, V_O = 7.2V, I_O = 0A	3			3	4.5		2.9			V
Noise Immunity (V_{NH}) (All Inputs)	V_{DD} = 5V, V_O = 0.95V, I_O = 0A	1.4			1.5	2.25		1.5			V
	V_{DD} = 10V, V_O = 2.9V, I_O = 0A	2.9			3	4.5		3			V
Output Drive Current N-Channel (I_DN)	V_{DD} = 5V, V_O = 0.4V, V_I = V_{DD}	0.5			0.40	1		0.28			mA
	V_{DD} = 10V, V_O = 0.5V, V_I = V_{DD}	1.1			0.9	2.5		0.65			mA
Output Drive Current P-Channel (I_DP)	V_{DD} = 5V, V_O = 2.5V, V_I = V_{SS}	–0.62			–0.5	–2		–0.35			mA
	V_{DD} = 10V, V_O = 9.5V, V_I = V_{SS}	–0.62			–0.5	–1		–0.35			mA
Input Current (I_I)						10					pA

dc electrical characteristics CD4001C

PARAMETER	CONDITIONS	LIMITS									UNITS
		–40°C			25°C			85°C			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Quiescent Device Current (I_L)	V_{DD} = 5V			0.5		0.005	0.5			15	μA
	V_{DD} = 10V			5		0.005	5			30	μA
Quiescent Device Dissipation/Package (P_D)	V_{DD} = 5V			2.5		0.025	2.5			75	μW
	V_{DD} = 10V			50		0.05	50			300	μW
Output Voltage Low Level (V_{OL})	V_{DD} = 5V, V_I = V_{DD}, I_O = 0A			0.01		0	0.01			0.05	V
	V_{DD} = 10V, V_I = V_{DD}, I_O = 0A			0.01		0	0.01			0.05	V
Output Voltage High Level (V_{OH})	V_{DD} = 5V, V_I = V_{SS}, I_O = 0A	4.99			4.99	5		4.95			V
	V_{DD} = 10V, V_I = V_{SS}, I_O = 0A	9.99			9.99	10		9.95			V
Noise Immunity (V_{NL}) (All Inputs)	V_{DD} = 5V, V_O = 3.6V, I_O = 0A	1.5			1.5	2.25		1.4			V
	V_{DD} = 10V, V_O = 7.2V, I_O = 0A	3			3	4.5		2.9			V
Noise Immunity (V_{NH}) (All Inputs)	V_{DD} = 5V, V_O = 0.95V, I_O = 0A	1.4			1.5	2.25		1.5			V
	V_{DD} = 10V, V_O = 2.9V, I_O = 0A	2.9			3	4.5		3			V
Output Drive Current N-Channel (I_DN)	V_{DD} = 5V, V_O = 0.4V, V_I = V_{DD}	0.35			0.3	1		0.24			mA
	V_{DD} = 10V, V_O = 0.5V, V_I = V_{DD}	0.72			0.6	2.5		0.48			mA
Output Drive Current P-Channel (I_DP)	V_{DD} = 5V, V_O = 2.5V, V_I = V_{SS}	–0.35			–0.3	–2		–0.24			mA
	V_{DD} = 10V, V_O = 9.5V, V_I = V_{SS}	–0.3			–0.25	–1		–0.2			mA
Input Current (I_I)						10					pA

Note 1: This device should not be connected to circuits with the power on because high transient voltages may cause permanent damage.

ac electrical characteristics CD4001M

T_A = 25°C and C_L = 15 pF and input rise and fall times = 20 ns. Typical temperature coefficient for all values of V_{DD} = 0.3%/°C.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Propagation Delay Time High to Low Level (t_{PHL})	V_{DD} = 5V V_{DD} = 10V		35 25	65 40	ns ns
Propagation Delay Time Low to High Level (t_{PLH})	V_{DD} = 5V V_{DD} = 10V		35 25	65 40	ns ns
Transition Time High to Low Level (t_{THL})	V_{DD} = 5V V_{DD} = 10V		65 35	125 70	ns ns
Transition Time Low to High Level (t_{TLH})	V_{DD} = 5V V_{DD} = 10V		65 35	175 75	ns ns
Input Capacitance (C_I)	Any Input		5		pF

ac electrical characteristics CD4001C

T_A = 25°C and C_L = 15 pF and input rise and fall times = 20 ns. Typical temperature coefficient for all values of V_{DD} = 0.3%/°C.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Propagation Delay Time High to Low Level (t_{PHL})	V_{DD} = 5V V_{DD} = 10V		35 25	80 55	ns ns
Propagation Delay Time Low to High Level (t_{PLH})	V_{DD} = 5V V_{DD} = 10V		35 25	120 65	ns ns
Transition Time High to Low Level (t_{THL})	V_{DD} = 5V V_{DD} = 10V		65 35	200 115	ns ns
Transition Time Low to High Level (t_{TLH})	V_{DD} = 5V V_{DD} = 10V		65 35	300 125	ns ns
Input Capacitance (C_I)	Any Input		5		pF

CD4002M/CD4002C dual 4-input NOR gate

general description

These NOR gates are monolithic complementary MOS (CMOS) integrated circuits. The N and P channel enhancement mode transistors provide a symmetrical circuit with output swings essentially equal to the supply voltage. This results in high noise immunity over a wide supply voltage range. No DC power other than that caused by leakage current is consumed during static conditions. All inputs are protected against static discharge and latching conditions.

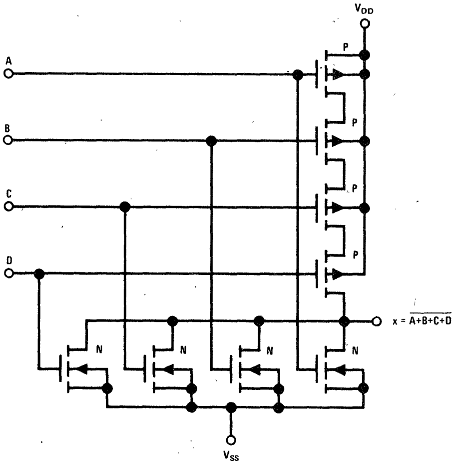
features

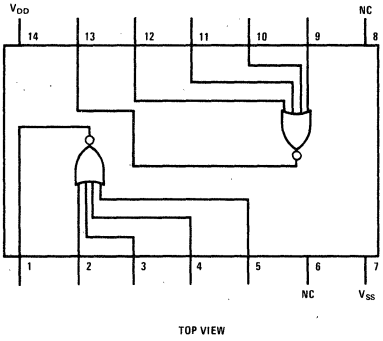
- Wide supply voltage range 3V to 15V
- Low power 10 nW (typical)
- High noise immunity 0.45 V_{DD} (typical)

applications

- Automotive
- Data terminals
- Instrumentation
- Medical electronics
- Alarm system
- Industrial controls
- Remote metering
- Computers

schematic and connection diagrams





TOP VIEW

absolute maximum ratings

Voltage at Any Pin (Note 1)	V_{SS} -0.3V to V_{SS} +15.5V	Package Dissipation	500 mW
Operating Temperature Range CD4002M	-55°C to +125°C	Lead Temperature (Soldering, 10 sec)	300°C
CD4002C	-40°C to +85°C	Operating V_{DD} Range	V_{SS} +3V to V_{SS} +15V
Storage Temperature Range	-65°C to +150°C		

electrical characteristics

CHARACTERISTIC	TEST CONDITIONS		LIMITS																		UNITS
			CD4002M									CD4002C									
			-55°C			25°C			125°C			-40°C			25°C			85°C			
	V_O VOLTS	V_{DD} VOLTS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Quiescent Device Current (I_L)		5	–	–	0 5	–	0 001	0.05	–	–	3	–	–	0 5	–	0.005	0.5	–	–	15	μA
		10	–	–	0.1	–	0.001	0 1	–	–	6	–	–	5	–	0.005	5	–	–	30	
Quiescent Device Dissipation/Package (P_D)		5	–	–	0.25	–	0.005	0.25	–	–	15	–	–	2 5	–	0.025	2 5	–	–	75	μW
		10	–	–	1	–	0 01	1	–	–	60	–	–	50	–	0.05	50	–	–	300	
Output Voltage Low Level (V_{OL})		5	–	–	0.01	–	0	0.01	–	–	0.05	–	–	0 01	–	0	0.01	–	–	0.05	V
		10	–	–	0.01	–	0	0.01	–	–	0.05	–	–	0 01	–	0	0.01	–	–	0.05	
High Level (V_{OH})		5	4.99	–	–	4.99	5	–	4.95	–	–	4 99	–	–	4.99	5	–	4.95	–	–	V
		10	9.99	–	–	9.99	10	–	9.95	–	–	9.99	–	–	9.99	10	–	9.95	–	–	
Noise Immunity (All Inputs) (V_{NI})	$V_O > 3.5$	5	1 5	–	–	1.5	2.25	–	1 4	–	–	1.5	–	–	1 5	2.25	–	1.4	–	–	V
	$V_O > 7.0$	10	3	–	–	3	4.5	–	2.9	–	–	3	–	–	3	4.5	–	2.9	–	–	
(V_{NH})	$V_O < 1 5$	5	1.4	–	–	1 5	2.25	–	1 5	–	–	1 4	–	–	1.5	2.25	–	1.5	–	–	V
	$V_O < 3.0$	10	2.9	–	–	3	4.5	–	3	–	–	2.9	–	–	3	4.5	–	3	–	–	
Output Drive Current N-Channel (I_DN)	$V_I = V_{DD}$ 0.4	5	0.5	–	–	0 40	–	–	0.28	–	–	0.35	–	–	0 3	1	–	0.24	–	–	mA
	0.5	10	1 1	–	–	0 9	–	–	0.65	–	–	0 72	–	–	0.6	2.5	–	0.48	–	–	
P-Channel (I_DP)	$V_I = V_{SS}$ 2.5	5	-0.62	–	–	-0 5	–	–	-0.35	–	–	-0 35	–	–	-0.3	-2	–	-0 24	–	–	mA
	9.5	10	-0 62	–	–	-0.5	–	–	-0.35	–	–	-0.3	–	–	-0.25	-1	–	-0.2	–	–	
Input Current (I_I)			–	–	–	–	10	–	–	–	–	–	–	–	–	10	–	–	–	–	pA

Note 1: This device should not be connected to circuits with the power on because high transient voltage may cause permanent damage.

CHARACTERISTICS	TEST CONDITIONS	LIMITS						UNITS
		CD4002M			CD4002C			
	V_{DD} (VOLTS)	MIN	TYP	MAX	MIN	TYP	MAX	
Propagation Delay Time: Low-to-High Level (t_{PLH})	5	–	35	50	–	35	80	ns
	10	–	25	40	–	25	55	
High-to-Low Level (t_{PHL})	5	–	35	95	–	35	120	ns
	10	–	25	45	–	25	65	
Transition Time: Low-to-High Level (t_{TLH})	5	–	65	125	–	65	200	ns
	10	–	35	70	–	35	115	
High-to-Low Level (t_{THL})	5	–	65	175	–	65	300	ns
	10	–	35	75	–	35	125	
Input Capacitance (C_I)	Any Input	–	5	–	–	5	–	pF

CD4006M/CD4006C 18-stage static shift register

general description

The CD4006M/CD4006C 18-stage static shift register is comprised of four separate shift register sections, two sections of four stages and two sections of five stages. Each section has an independent data input. Outputs are available at the fourth stage and the fifth stage of each section. A common clock signal is used for all stages. Data is shifted to the next stage on the negative-going transition of the clock. Through appropriate connections of inputs and outputs, multiple register sections of 4, 5, 8 and 9 stages or single register section of 10, 12, 13, 14, 16, 17, and 18 stages can be implemented using one package.

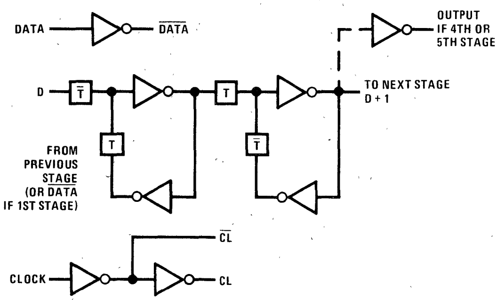
features

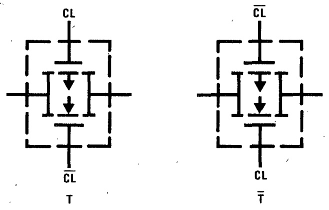
■ Wide supply voltage range	3.0V to 15V
■ High noise immunity	0.45 V_{DD} typ
■ Low clock input capacitance	6 pF typ
■ Medium speed operation	10 MHz typ with V_{DD} = 10V
■ Low power	
■ Fully static operation	

applications

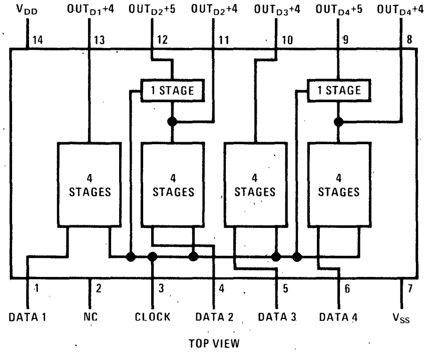
- Automotive
- Data terminals
- Instrumentation
- Medical electronics
- Alarm system
- Industry control
- Remote metering
- Computers

logic diagrams





connection diagram



truth table

D	CL^{Δ}	D+1
0	↓	0
1	↓	1
X	↑	NC

X = Don't care
Δ = Level change
NC = No change

absolute maximum ratings

Voltage at Any Pin (Note 1)	V_{SS} − 0.3V to V_{DD} + 0.3V
Operating Temperature Range	
CD4006M	−55°C to +125°C
CD4006C	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500 mW
Operating V_{DD} Range	V_{SS} + 3.0V to V_{SS} + 15V
Lead Temperature (Soldering, 10 seconds)	300°C

dc electrical characteristics CD4006M

PARAMETER	CONDITIONS	LIMITS									UNITS
		−55°C			25°C			125°C			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Quiescent Device Current (I_L)	V_{DD} = 5.0V			0.5		0.01	0.5			30	µA
	V_{DD} = 10V			1.0		0.01	1.0			60	µA
Quiescent Device Dissipation/Package (P_D)	V_{DD} = 5.0V			2.5		0.05	2.5			150	µW
	V_{DD} = 10V			10		0.1	10			600	µW
Output Voltage Low Level (V_{OL})	V_{DD} = 5.0V			0.01		0	0.01			0.05	V
	V_{DD} = 10V			0.01		0	0.01			0.05	V
Output Voltage High Level (V_{OH})	V_{DD} = 5.0V	4.99				4.99	5	4.95			V
	V_{DD} = 10V	9.99				9.99	10	9.95			V
Noise Immunity (V_{NL}) (All Inputs)	V_{DD} = 5.0V	1.5			1.5	2.25		1.4			V
	V_{DD} = 10V	3.0			3.0	4.5		2.9			V
Noise Immunity (V_{NH}) (All Inputs)	V_{DD} = 5.0V	1.4			1.5	2.25		1.5			V
	V_{DD} = 10V	2.9			3.0	4.5		3.0			V
Output Drive Current N-Channel (I_DN)	V_{DD} = 5.0V, V_O = 0.5V	0.155			0.125	0.25		0.085			mA
	V_{DD} = 10V, V_O = 0.5V	0.31			0.25	0.5		0.175			mA
Output Drive Current P-Channel (I_DP)	V_{DD} = 5.0V, V_O = 4.5V	−0.125			−0.1	−0.15		−0.07			mA
	V_{DD} = 10V, V_O = 9.5V	−0.25			−0.2	−0.3		−0.14			mA
Input Current (I_I)	Any Input					10					pA

dc electrical characteristics CD4006C

PARAMETER	CONDITIONS	LIMITS									UNITS
		−40°C			25°C			85°C			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Quiescent Device Current (I_L)	V_{DD} = 5.0V			5		0.03	5			70	µA
	V_{DD} = 10V			10		0.05	10			140	µA
Quiescent Device Dissipation/Package (P_D)	V_{DD} = 5.0V			25		0.15	25			350	µW
	V_{DD} = 10V			100		0.5	100			1400	µW
Output Voltage Low Level (V_{OL})	V_{DD} = 5.0V			0.01		0	0.01			0.05	V
	V_{DD} = 10V			0.01		0	0.01			0.05	V
Output Voltage High Level (V_{OH})	V_{DD} = 5.0V	4.99			4.99	5		4.95			V
	V_{DD} = 10V	9.99			9.99	10		9.95			V
Noise Immunity (V_{NL}) (All Inputs)	V_{DD} = 5.0V	1.5			1.5	2.25		1.4			V
	V_{DD} = 10V	3			3	4.5		2.9			V
Noise Immunity (V_{NH}) (All Inputs)	V_{DD} = 5.0V	1.4			1.5	2.25		1.5			V
	V_{DD} = 10V	2.9			3	4.5		3			V
Output Drive Current N-Channel (I_DN)	V_{DD} = 5.0V, V_O = 0.5V	0.072			0.06	0.25		0.048			mA
	V_{DD} = 10V, V_O = 0.5V	0.15			0.125	0.5		0.10			mA
Output Drive Current P-Channel (I_DP)	V_{DD} = 5.0V, V_O = 4.5V	−0.06			−0.05	−0.15		−0.04			mA
	V_{DD} = 10V, V_O = 9.5V	−0.12			−0.1	−0.3		−0.08			mA
Input Current (I_I)	Any Input					10					pA

Note 1: This device should not be connected to circuits with power on because high transient voltages may cause permanent damage.

ac electrical characteristics

CD4006M at T_A = 25°C and C_L = 15 pF. Typical temperature coefficient for all values of V_{DD} = 0.3%/°C.

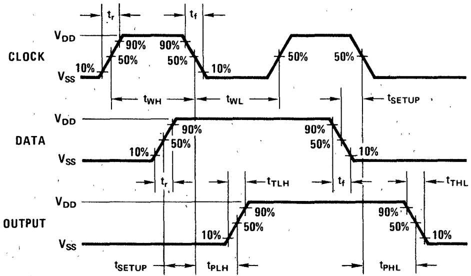
PARAMETER	CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Propagation Delay Time ($t_{PLH} = t_{PHL}$)	V_{DD} = 5.0V		180	400	ns
	V_{DD} = 10V		80	200	ns
Transition Time ($t_{TLH} = t_{THL}$)	V_{DD} = 5.0V		150	400	ns
	V_{DD} = 10V		60	200	ns
Minimum Clock Pulse Width ($T_{WL} = T_{WH}$)	V_{DD} = 5.0V		100	500	ns
	V_{DD} = 10V		50	200	ns
Clock Rise and Fall Time ($t_{rCl} = t_{fCl}$)*	V_{DD} = 5.0V			15	μs
	V_{DD} = 10V			5	μs
Set-Up Time	V_{DD} = 5.0V		50	80	ns
	V_{DD} = 10V		25	40	ns
Maximum Clock Frequency (f_{cl})	V_{DD} = 5.0V	1	5		MHz
	V_{DD} = 10V	2.5	10		MHz
Input Capacitance (C_I)	Data Input		5		pF
	Clock Input		6		pF

ac electrical characteristics CD4006C

PARAMETER	CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Propagation Delay Time ($t_{PLH} = t_{PHL}$)	V_{DD} = 5.0V		180	500	ns
	V_{DD} = 10V		80	250	ns
Transition Time ($t_{TLH} = t_{THL}$)	V_{DD} = 5.0V		150	400	ns
	V_{DD} = 10V		60	250	ns
Minimum Clock Pulse Width ($T_{WH} = T_{WL}$)	V_{DD} = 5.0V		100	830	ns
	V_{DD} = 10V		50	250	ns
Clock Rise and Fall Time ($t_{rCl} = t_{fCl}$)*	V_{DD} = 5.0V			15	μs
	V_{DD} = 10V			5	μs
Set-Up Time	V_{DD} = 5.0V		50	100	ns
	V_{DD} = 10V		25	50	ns
Maximum Clock Frequency (f_{cl})	V_{DD} = 5.0V	0.6	5		MHz
	V_{DD} = 10V	2	10		MHz
Input Capacitance (C_I)	Data Input		5		pF
	Clock Input		6		pF

*If more than one unit is cascaded t_{rCl} should be made less than or equal to the sum of the fixed propagation delay time at 15 pF and the transition time of the output stage for the estimated capacitive load.

switching time waveforms



$t_r = t_f$ = 20 ns

CD4007M/CD4007C dual complementary pair plus inverter

general description

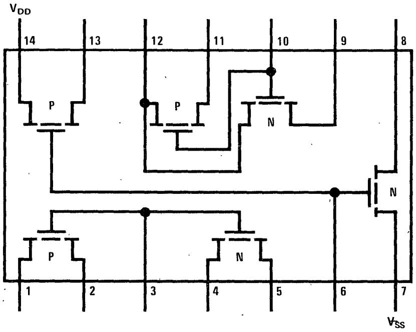
The CD4007M/CD4007C consists of three complementary pairs of N-channel and P-channel enhancement mode MOS transistors. All inputs are protected from static discharge by diode clamps to V_{DD} and V_{SS}.

For proper operation the voltages at all pins must be constrained to be between $V_{SS} - 0.3V$ and $V_{DD} + 0.3V$ at all times.

features

■ Wide supply voltage range	3.0V to 15V
■ High noise immunity	0.45 V_{CC} typ

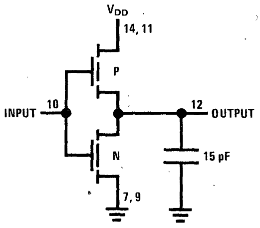
connection diagram

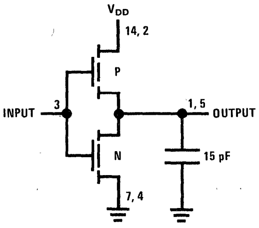


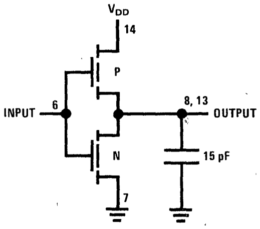
TOP VIEW

Note: All P-channel substrates are connected to V_{DD}, and all N-channel substrates are connected to V_{SS}.

ac test circuits







absolute maximum ratings (Note 1)

Voltage at Any Pin	V_{SS} − 0.3V to V_{DD} + 0.3V
Operating Temperature Range	
CD4007M	−55°C to +125°C
CD4007C	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500 mW
Operating V_{DD} Range	V_{SS} + 3.0V to V_{SS} + 15V
Lead Temperature (Soldering, 10 seconds)	300°C

dc electrical characteristics CD4007M

PARAMETER	CONDITIONS	LIMITS									UNITS
		−55°C			25°C			125°C			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Quiescent Device Current (I_L)	V_{DD} = 5V			0.05		0.001	0.05			3	µA
	V_{DD} = 10V			0.1		0.001	0.1			6	µA
Quiescent Device Dissipation/Package (P_D)	V_{DD} = 5V			0.25		0.005	0.25			15	µW
	V_{DD} = 10V			1		0.01	1			60	µW
Output Voltage Low Level (V_{OL})	V_{DD} = 5V			0.01		0	0.01			0.05	V
	V_{DD} = 10V			0.01		0	0.01			0.05	V
Output Voltage High Level (V_{OH})	V_{DD} = 5V	4.99			4.99	5		4.95			V
	V_{DD} = 10V	9.99			9.99	10		9.95			V
Noise Immunity (V_{NL}) (All Inputs)	V_{DD} = 5V, V_O = 3.6V	1.5			1.5	2.25		1.4			V
	V_{DD} = 10V, V_O = 7.2V	3			3	4.5		2.9			V
Noise Immunity (V_{NH}) (All Inputs)	V_{DD} = 5V, V_O = 0.95V	1.4			1.5	2.25		1.5			V
	V_{DD} = 10V, V_O = 2.9V	2.9			3	4.5		3			V
Output Drive Current N-Channel (I_DN)	V_{DD} = 5V, V_O = 0.4V, V_I = V_{DD}	0.75			0.6	1		0.4			mA
	V_{DD} = 10V, V_O = 0.5V, V_I = V_{DD}	1.6			1.3	2.5		0.95			mA
Output Drive Current P-Channel (I_DP)	V_{DD} = 5V, V_O = 2.5V, V_I = V_{SS}	−1.75			−1.4	−4		−1			mA
	V_{DD} = 10V, V_O = 9.5V, V_I = V_{SS}	−1.35			−1.1	−2.5		−0.75			mA
Input Current (I_I)						10					pA

dc electrical characteristics CD4007C

PARAMETER	CONDITIONS	LIMITS									UNITS
		−40°C			25°C			85°C			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Quiescent Device Current (I_L)	V_{DD} = 5V			0.5		0.005	0.5			15	µA
	V_{DD} = 10V			1		0.005	1			30	µA
Quiescent Device Dissipation/Package (P_D)	V_{DD} = 5V			2.5		0.025	2.5			75	µW
	V_{DD} = 10V			10		0.05	10			300	µW
Output Voltage Low Level (V_{OL})	V_{DD} = 5V			0.01		0	0.01			0.05	V
	V_{DD} = 10V			0.01		0	0.01			0.05	V
Output Voltage High Level (V_{OH})	V_{DD} = 5V	4.99			4.99	5		4.95			V
	V_{DD} = 10V	9.99			9.99	10		9.95			V
Noise Immunity (V_{NL}) (All Inputs)	V_{DD} = 5V, V_O = 3.6V	1.5			1.5	2.25		1.4			V
	V_{DD} = 10V, V_O = 7.2V	3			3	4.5		2.9			V
Noise Immunity (V_{NH}) (All Inputs)	V_{DD} = 5V, V_O = 0.95V	1.4			1.5	2.25		1.5			V
	V_{DD} = 10V, V_O = 2.9V	2.9			3	4.5		3			V
Output Drive Current N-Channel (I_DN)	V_{DD} = 5V, V_O = 0.4V, V_I = V_{DD}	0.35			0.3	1		0.24			mA
	V_{DD} = 10V, V_O = 0.5V, V_I = V_{DD}	1.2			1	2.5		0.8			mA
Output Drive Current P-Channel (I_DP)	V_{DD} = 5V, V_O = 2.5V, V_I = V_{SS}	−1.3			−1.1	−4		−0.9			mA
	V_{DD} = 10V, V_O = 9.5V, V_I = V_{SS}	−0.65			−0.55	−2.5		−0.45			mA
Input Current (I_I)						10					pA

Note 1: This device should not be connected to circuits with the power on because high transient voltages may cause permanent damage.

ac electrical characteristics CD4007M

T_A = 25°C and C_L = 15 pF and input rise and fall times = 20 ns. Typical temperature coefficient for all values of V_{DD} = 0.3%/°C.

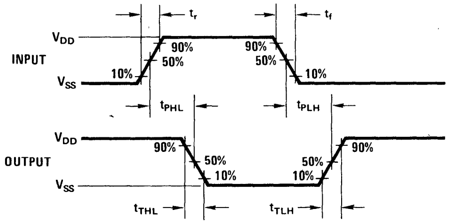
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Propagation Delay Time ($t_{PLH} = t_{PHL}$)	V_{DD} = 5V		35	60	ns
	V_{DD} = 10V		20	40	ns
Transition Time ($t_{TLH} = t_{THL}$)	V_{DD} = 5V		50	75	ns
	V_{DD} = 10V		30	40	ns
Input Capacitance (C_I)	Any Input		5		pF

ac electrical characteristics CD4007C

T_A = 25°C and C_L = 15 pF and input rise and fall times = 20 ns. Typical temperature coefficient for all values of V_{DD} = 0.3%/°C.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Propagation Delay Time ($t_{PLH} = t_{PHL}$)	V_{DD} = 5V		35	75	ns
	V_{DD} = 10V		20	50	ns
Transition Time ($t_{TLH} = t_{THL}$)	V_{DD} = 5V		50	100	ns
	V_{DD} = 10V		30	50	ns
Input Capacitance (C_I)	Any Input		5		pF

switching time waveforms



$t_r = t_f = 20$ ns

CD4009M/CD4009C hex buffers (inverting)
CD4010M/CD4010C hex buffers (non-inverting)

general description

These hex buffers are monolithic complementary MOS (CMOS) integrated circuits. The N and P channel enhancement mode transistors provide a symmetrical circuit with output swings essentially equal to the supply voltage. This results in high noise immunity over a wide supply voltage range. No DC power other than that caused by leakage current is consumed during static conditions. All inputs are protected against static discharge. These gates may be used as hex buffers, CMOS to DTL or TTL interface or as CMOS current drivers. Conversion ranges are from 3 to 15 volts providing $V_{CC} \leq V_{DD}$.

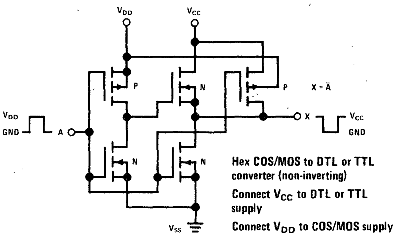
features

- Wide supply voltage range 3V to 15V
- Low power 100 nW (typical)
- High noise immunity 0.45 V_{DD} (typical)
- High current sinking capability 8 mA (min) at VO = 0.5V and V_{DD} = 10V

applications

- Automotive
- Data terminals
- Instrumentation
- Medical electronics
- Alarm system
- Industrial controls
- Remote metering
- Computers

schematic and connection diagrams

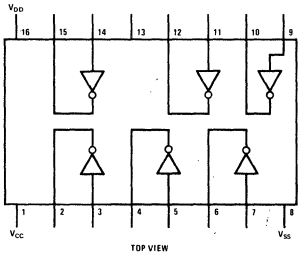


Hex COS/MOS to DTL or TTL converter (non-inverting)

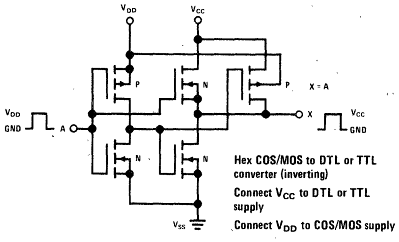
Connect V_{CC} to DTL or TTL supply

Connect V_{DD} to COS/MOS supply

CD4009M/CD4009C



TOP VIEW

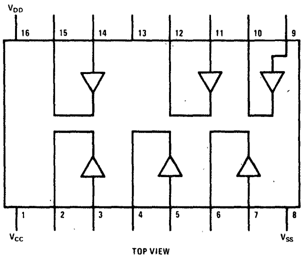


Hex COS/MOS to DTL or TTL converter (inverting)

Connect V_{CC} to DTL or TTL supply

Connect V_{DD} to COS/MOS supply

CD4010M/CD4010C



TOP VIEW

absolute maximum ratings

Voltage at Any Pin (Note 1)	V_{SS} - 0.3V to V_{SS} + 15.5V	Package Dissipation	500 mW
Operating Temperature Range CD40XXM	-55°C to +125°C	Lead Temperature (Soldering, 10 sec)	300°C
CD40XXC	-40°C to +85°C	Operating V_{DD} Range	V_{SS} + 3V to V_{SS} + 15V
Storage Temperature Range	-65°C to +150°C		

dc electrical characteristics

CHARACTERISTIC	TEST CONDITIONS		LIMITS																	UNITS
			CD40XXM									CD40XXC								
			-55°C			25°C			125°C			-40°C			25°C			85°C		
	V_O VOLTS	V_{DD} VOLTS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Quiescent Device Current (I_L)		5	–	–	0 3	–	0 01	0.3	–	–	20	–	–	3	–	0.03	3	–	–	42	µA
		10			0 5	–	0.01	0 5	–	–	30	–	–	5	–	0.05	5	–	–	70	
Quiescent Device Dissipation/Package (P_D)		5	–		1 5	–	0.05	1 5	–		100	–	–	15	–	0.15	15	–	–	210	µW
		10	–	–	5	–	0.1	5	–	–	300	–	–	50	–	0.5	50	–	–	700	
Output Voltage: Low-Level (V_{OL})		5	–		0 01	–	0	0.01	–	–	0 05	–	–	0 01	–	0	0.01	–	–	0.05	V
		10	–	–	0.01	–	0	0.01	–	–	0.05	–	–	0.01	–	0	0 01	–	–	0.05	
High-Level (V_{OH})		5	4 99	–		4.99	5	–	4.95	–	–	4.99	–	–	4.99	5	–	4.95	–	–	V
		10	9 99			9.99	10	–	9.95	–	–	9 99	–	–	9.99	10	–	9.95	–	–	
Noise Immunity (All Inputs)																					
(V_{NL}) CD4009M	$V_O \geq 4.0$	5	1	–	–	1	2.25	–	0.9	–	–	1	–	–	1	2.25	–	0.9	–	–	V
	$V_O \geq 8.0$	10	2	–	–	2	4.5	–	1.2	–	–	2	–	–	2	4.5	–	1.9	–	–	
(V_{NL}) CD4010M	$V_O \leq 1.5$	5	1 6	–	–	1 5	2.25	–	1.4	–	–	1.6	–	–	1.5	2.25	–	1.4	–	–	
	$V_O \leq 3 0$	10	3.2	–		3	4.5	–	2 9	–	–	3.2	–	–	3	4 5	–	2.9	–	–	
(V_{NH})	$V_O \geq 3.5$	5	1 4	–	–	1 5	2.25	–	1 5	–	–	1.4	–	–	1.5	2.25	–	1.5	–	–	V
	$V_O \geq 7.0$	10	2 9	–	–	3	4.5	–	3	–	–	2.9	–	–	3	4.5	–	3	–	–	
Output Drive Current: N-Channel (I_DN)	0.4	5	3.75	-	–	3	4	–	2.1	–	–	3.6	–	–	3	–	–	2.4	–	–	mA
	0.5	10	10	–	–	8	10	–	5 6	–	–	9.6	–	–	8	–	–	6.4	–	–	
P-Channel (I_DP)	2.5	5	-1.85	–	–	-1.25	-1.75	–	-0.9	–	–	-1 5	–	–	-1.25	–	–	-1	–	–	mA
	9.5	10	-0.9	–	–	-0.6	-0.8	–	-0.4	–	–	-0.72	–	–	-0.6	–	–	-0.48	–	–	
Input Current (I_I)			–	–	–	–	10	–	–	–	–	–	–	–	–	10	–	–	–	–	pA

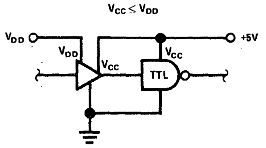
Note 1: This device should not be connected to circuits with the power on because high transient voltage may cause permanent damage.

ac electrical characteristics at T_A = 25°C and C_L = 15 pF

Typical Temperature Coefficient for all values of V_{DD} = 0.3%/°C

CHARACTERISTIC	TEST CONDITIONS		LIMITS						UNITS
			CD40XXM			CD40XXC			
		V_{DD} (VOLTS)	MIN	TYP	MAX	MIN	TYP	MAX	
Propagation Delay Time: High-to-Low Level (t_{PHL})	$V_{CC} = V_{DD}$	5	–	15	55	-	15	70	ns
		10	–	10	30	–	10	40	
	V_{DD} = 10V V_{CC} = 5V		–	10	25	–	10	35	
Low-to-High Level (t_{PLH})	$V_{CC} = V_{DD}$	5	–	50	80	–	50	100	ns
		10	–	25	55	–	25	70	
	V_{DD} = 10V V_{CC} = 5V		–	15	30	–	15	40	
Transition Time: High-to-Low Level (t_{THL})	$V_{CC} = V_{DD}$	5	–	20	45	–	20	60	ns
		10	–	16	40	–	16	50	
Low-to-High Level (t_{TLH})	$V_{CC} = V_{DD}$	5	–	80	125	–	80	160	ns
		10	–	50	100	–	50	120	
Input Capacitance (C_I)	Any Input		–	5	–	–	5	–	pF

typical applications



CD4011M/CD4011C quad 2-input NAND gate
CD4012M/CD4012C dual 4-input NAND gate
CD4023M/CD4023C triple 3-input NAND gate

general description

These NAND gates are monolithic complementary MOS (CMOS) integrated circuits. The N and P channel enhancement mode transistors provide a symmetrical circuit with output swings essentially equal to the supply voltage. This results in high noise immunity over a wide supply voltage range. No DC power other than that caused by leakage current is consumed during static conditions. All inputs are protected against static discharge and latching conditions.

features

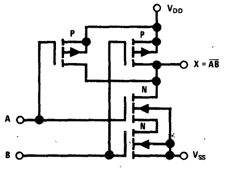
■ Wide supply voltage range	3V to 15V
■ Low power	10 nW (typical)
■ High noise immunity	0.45 V_{DD} (typical)

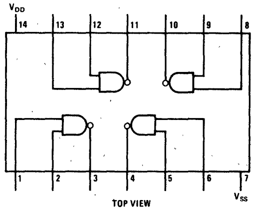
applications

- Automotive
- Data Terminals
- Instrumentation
- Medical Electronics
- Alarm System
- Industrial Controls
- Remote Metering
- Computers

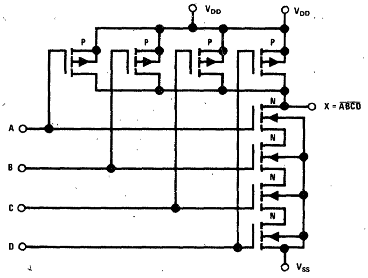
schematic and connection diagrams

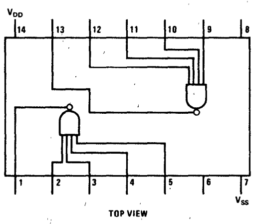
CD4011M/CD4011C SCHEMATIC



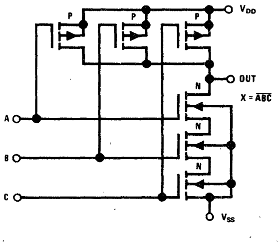


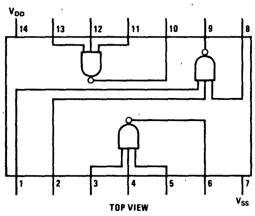
CD4012M/CD4012C SCHEMATIC





CD4023M/CD4023C SCHEMATIC





absolute maximum ratings

Voltage at Any Pin (Note 1)	V_{SS} - 0.3V to V_{SS} + 15.5V	Package Dissipation	500 mW
Operating Temperature Range CD40XXM	-55°C to +125°C	Lead Temperature (Soldering, 10 sec)	300°C
CD40XXC	-40°C to +85°C	Operating V_{DD} Range	V_{SS} + 3V to V_{SS} + 15V
Storage Temperature Range	-65°C to +150°C		

Note 1: This device should not be connected to circuits with the power on because high transient voltage may cause permanent damage.

dc electrical characteristics

CHARACTERISTIC	TEST CONDITIONS		LIMITS																		UNITS
			CD40XXM									CD40XXC									
			-55°C			25°C			125°C			-40°C			25°C			85°C			
	V_O VOLTS	V_{DD} VOLTS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Quiescent Device Current (I_L)		5	–	–	0.05	–	0.001	0.05	–	–	3	–	–	0.5	–	0.005	0.5	–	–	15	μA
		10	–	–	0.1	–	0.001	0.1	–	–	6	–	–	5	–	0.005	5	–	–	30	
Quiescent Device Dissipation/Package (P_D)		5	–	–	0.25	–	0 005	0.25	–	–	15	–	–	2.5	–	0.025	2.5	–	–	75	μW
		10	–	–	1	–	0.01	1	–	–	60	–	–	50	–	0.05	50	–	–	300	
Output Voltage. Low-Level (V_{OL})		5	–	–	0.01	–	0	0.01	–	–	0.05	–	–	0.01	–	0	0.01	–	–	0.05	V
		10	–	–	0.01	–	0	0.01	–	–	0.05	–	–	0.01	–	0	0.01	–	–	0.05	
High-Level (V_{OH})		5	4.99	–	–	4.99	5	–	4.95	–	–	4.99	–	–	4.99	5	–	4.95	–	–	V
		10	9.99	–	–	9.99	10	–	9.95	–	–	9.99	–	–	9.99	10	–	9.95	–	–	
Noise Immunity (All Inputs) (V_{NL})	$V_O \geq 3.5$	5	1.5	–	–	1.5	2.25	–	1.4	–	–	1.5	–	–	1.5	2.25	–	1.4	–	–	V
	$V_O \geq 7.0$	10	3	–	–	3	4.5	–	2.9	–	–	3	–	–	3	4.5	–	2.9	–	–	
(V_{NH})	$V_O \leq 1.5$	5	1.4	–	–	1.5	2.25	–	1.5	–	–	1.4	–	–	1.5	2.25	–	1.5	–	–	V
	$V_O \leq 3.0$	10	2.9	–	–	3	4.5	–	3	-	–	2.9	–	–	3	4.5	–	3	–	–	
Output Drive Current N-Channel (I_DN)	0.5	5	0.31	–	–	0.25	0.5	–	0 175	–	–	0.145	–	–	0.12	0.5	–	0.95	–	–	mA
	0.5	10	0.62	–	–	0.5	0.6	–	0.35	–	–	0.3	–	–	0.25	0.6	–	0.2	–	–	
P-Channel (I_DP)	4.5	5	-0.31	–	–	-0.25	-0.5	–	-0.175	–	–	-0.145	–	–	-0.12	-0.5	–	-0.95	–	–	mA
	9.5	10	-0.75	–	–	-0.6	-1.2	–	-0.4	–	–	-0.35	–	–	-0.3	-1.2	–	-0.24	–	–	
Input Current (I_I)				–	–	–	10	–	–	–	–	–	–	–	–	10	–	–	–	–	pA

ac electrical characteristics @ T_A = 25°C and C_L = 15pF

Typical Temperature Coefficient for all values of V_{DD} = 0.3%/°C

CHARACTERISTICS	TEST CONDITIONS	LIMITS						UNITS
		CD40XXM			CD40XXC			
	V_{DD} (VOLTS)	MIN	TYP	MAX	MIN	TYP	MAX	
Propagation Delay Time: Low-to-High Level (t_{PLH})	5	–	50	75	–	50	100	ns
	10	–	25	40	–	25	50	
High-to Low Level (t_{PHL})	5	–	50	75	–	50	100	ns
	10	–	25	40	–	25	50	
Transition Time: Low-to-High Level (t_{TLH})	5	–	75	100	–	75	125	ns
	10	–	40	60	–	40	75	
High-to-Low Level (t_{THL})	5	–	75	125	–	75	150	ns
	10	–	50	75	–	50	100	
Input Capacitance (C_I)	Any Input	–	5	–	–	5	–	pF

CD4013M/CD4013C dual D flip-flop

general description

The CD4013M/CD4013C dual D flip-flop is a monolithic complementary MOS (CMOS) integrated circuit constructed with N and P channel enhancement transistors. Each flip flop has independent data, set, reset, and clock inputs and, "Q" and "$\overline{Q}$" outputs. These devices can be used for shift register applications, and, by connecting "$\overline{Q}$" output to the data input, for counter and toggle applications. The logic level present at the "D" input is transfered to the Q output during the positive-going transition of the clock pulse. Setting or resetting is independent of the clock and is accomplished by a high level on the set or reset line respectively.

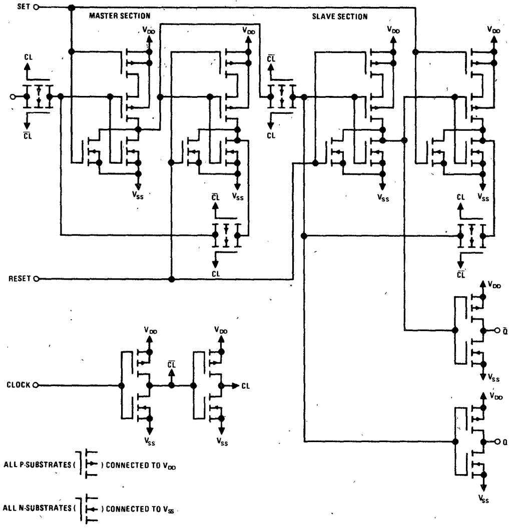
features

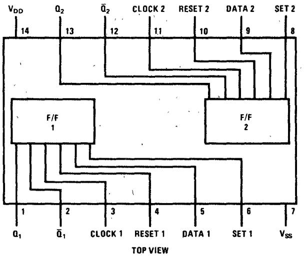
■ Supply voltage range	3V to 15V
■ Noise Immunity	0.45 V_{DD} (typ)
■ Low power	50 nW (typ)
■ Medium speed operation	10 MHz (typ) with 10 volt supply

applications

- Automotive
- Data terminals
- Instrumentation
- Medical electronics
- Alarm system
- Industrial electronics
- Remote metering
- Computers

schematic and connection diagrams





absolute maximum ratings

Voltage at Any Pin (Note 1)	V_{SS} – 0.3V to V_{SS} + 15.5V
Operating Temperature Range	
CD4013M	-55°C to +125°C
CD4013C	-40°C to +85°C
Storage Temperature Range	-65°C to +150°C
Package Dissipation	500 mW
Lead Temperature (Soldering, 10 sec)	300°C
Operating V_{DD} Range	V_{SS} + 3V to V_{SS} + 15V

dc electrical characteristics

CHARACTERISTIC	TEST CONDITIONS		LIMITS																		UNITS
			CD4013M									CD4013C									
			-55°C			25°C			125°C			-40°C			25°C			85°C			
	V_O VOLTS	V_{DD} VOLTS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Quiescent Device Current (I_L)		5	–	–	1	–	0.005	1	–	–	60	–	–	10		0.01	10	–	–	140	μA
		10	–	–	2	–	0.005	2	–	–	120		–	20	–	0.02	20	–	–	280	
Quiescent Device Dissipation/Package (P_D)		5	–	–	5	–	0.025	5		–	300	–	–	50	–	0.05	50	–	–	700	μW
		10	–	–	20	–	0.05	20	–	–	1200	–	–	200		0.2	200	–	–	2800	
Output Voltage Low-Level (V_{OL})	V_{IN} = 5	5	–	–	0.01	–	0	0.01	–	–	0.05	–	–	0.01	–	0	0.01	–	–	0.05	V
	V_{IN} = 10	10	–	–	0.01	–	0	0.01	–	–	0.05	–		0.01	–	0	0.01	–	–	0.05	
High-Level (V_{OH})	V_{IN} = 0	5	4.99	–	–	4.99	5	–	4.95	–		4.99	–	–	4.99	5	–	4.95	–	–	V
	V_{IN} = 0	10	9.99	–	–	9.99	10	–	9.95	–	–	9.99	–	–	9.99	10	–	9.95	–	–	
Noise Immunity (All Inputs) (V_{NL})	$V_O \geq 3.5$	5	1.5	–	–	1.5	2.25		1.4	–	–	1.5	–	–	1.5	2.25	–	1.4	–	–	V
	$V_O \geq 7.0$	10	3	–	–	3	4.5	–	2.9	–	–	3	–	–	3	4.5	–	2.9	–	–	
(V_{NH})	$V_O < 1.5$	5	1.4	–	–	1.5	2.25	–	1.5	–	–	1.4	–	–	1.5	2.25	–	1.5	–	–	V
	$V_O \leq 3.0$	10	2.9	–	–	3	4.5	–	3	–	–	2.9	–	–	3	4.5	–	3	–	–	
Output Drive Current N-Channel (I_DN)	V_O = 0.5	5	0.65	–	–	0.5	1	–	0.35	–	–	0.35	–	–	0.3	1	–	0.24	–	–	mA
	V_O = 0.5	10	1.25	–	–	1.0	2.5	–	0.75	–	–	0.72	–	–	0.6	2.5	–	0.5	–	–	
P-Channel (I_DP)	V_O = 4.5	5	-0.31	–	–	-0.25	-0.5	–	-0.175	–	–	-0.17	–	–	-0.14	-0.5	–	-0.095	–	–	mA
	V_O = 9.5	10	-0.8	–	–	-0.65	-1.3	–	-0.45	–	–	-0.4		–	-0.33	-1.3	–	-0.27	–	–	
Input Current (I_I)			–	–	–	–	10	–	–	–	–	–	–	–	–	10	–	–	–	–	pA

Note 1: Devices should not be connected with power on.

*Test performed with the following sequence of 1's and 0's.

C_L	D	S	R
0	1	0	1
0	0	1	1
0	0	1	0
1	0	1	0

ac electrical characteristics at T_A = 25°C and C_L = 15 pF

Typical Temperature Coefficient for all values of V_{DD} = 0.3%/°C

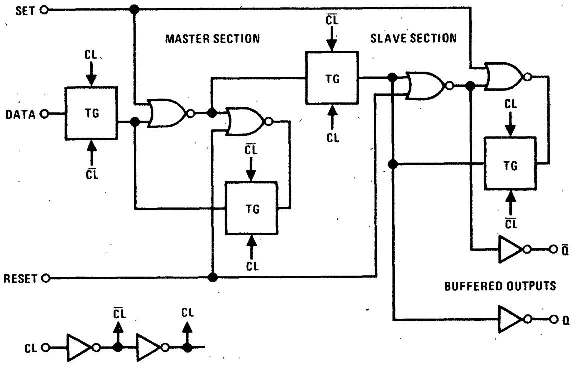
CHARACTERISTICS	TEST CONDITIONS		LIMITS						UNITS
			CD4013M			CD4013C			
		V_{DD} (VOLTS)	MIN	TYP	MAX	MIN	TYP	MAX	
CLOCKED OPERATION									
Propagation Delay Time. ($t_{PHL} = t_{PLH}$)		5	–	150	250	–	150	250	ns
		10	–	75	110	–	75	125	
Transition Time ($t_{THL} = t_{TLH}$)		5	–	75	125	–	75	150	ns
		10	–	50	70	–	50	75	
Minimum Clock Pulse Width ($t_{WL} = t_{WH}$)		5	–	125	175	–	125	200	ns
		10	–	50	80	–	50	100	
Maximum Clock Rise & Fall Time (*$t_{rCL} = t_{fCL}$)		5	15	–	–	15		–	μs
		10	5	–	–	5		–	
Set-Up Time		5	–	20	40	–	20	50	
		10	–	10	20	–	10	25	
Maximum Clock Frequency (f_{CL})		5	3	4	–	2.5	4	–	MHz
		10	7	10	–	5	10	–	
Input Capacitance (C_I)	Any Input		–	5	–	–	5	–	pF
SET & RESET OPERATION									
Propagation Delay Time ($t_{PHL(R)}$) ($t_{PLH(S)}$)		5	–	175	225		175	250	ns
		10		75	110		[illegible]	125	
Minimum Set and Reset Pulse Widths ($t_{WH(S)}$, $t_{WH(R)}$)		5		125	175	–	125	200	ns
		10	–	50	80	–	50	100	

truth table

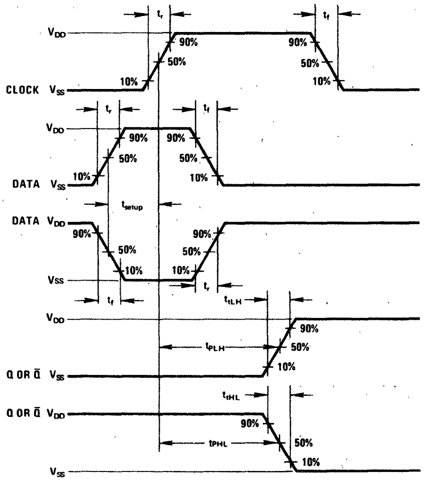
CL†	D	R	S	Q	$\bar{Q}$
↑	0	0	0	0	1
↑	1	0	0	1	0
↓	x	0	0	Q	$\bar{Q}$
x	x	1	0	0	1
x	x	0	1	1	0
x	x	1	1	*	*

No change
* = Invalid condition
** = FF1/FF2 terminal assignments
† = Level change
x = Don't care case

logic diagram



switching time waveforms



CD4014M/CD4014C 8-stage static shift register

general description

The CD4014M/CD4014C is an 8-stage parallel input/serial output shift register. A parallel/serial control input enables individual "jam" inputs to each of 8-stages. Q outputs are available from the sixth, seventh and eighth stages.

When the parallel/serial control input is in the logical "0" state, data is serially shifted into the register synchronously with the positive transition of the clock. When the parallel/serial control input is in the logical "1" state, data is jammed into each stage of the register synchronously with the positive transition of the clock.

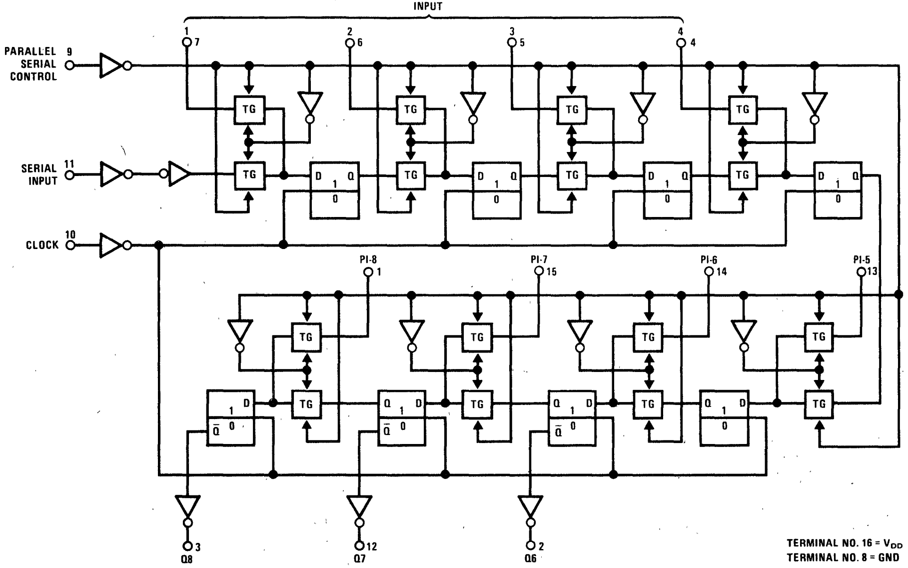
features

- Synchronous operation
- Wide supply voltage range 3.0V to 15V
- High noise immunity 0.45 V_{CC} typ
- Medium speed operation 5 MHz typ
  clock rate at $V_{DD} - V_{SS} = 10V$
- Fully static operation
- Low power

applications

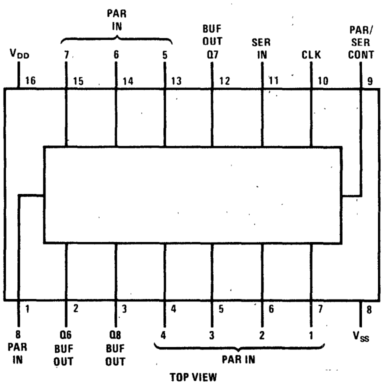
- Parallel to serial conversion
- General purpose register

logic diagram



TERMINAL NO. 16 = V_{DD}
TERMINAL NO. 8 = GND

connection diagram



truth table

CL▲	SERIAL INPUT	PARALLEL/ SERIAL CONTROL	PI 1	PI n	Q1 (INTERNAL)	Q_n	
↑	X	1	0	0	0	0	
↑	X	1	1	0	1	0	
↑	X	1	0	1	0	1	
↑	X	1	1	1	1	1	
↑	0	0	X	X	0	Q_n 1	
↑	1	0	X	X	1	Q_n 1	
↓	X	X	X	X	Q1	Q_n	NO CHANGE

▲ = LEVEL CHANGE X = DON'T CARE CASE

absolute maximum ratings (Note 1)

Voltage at Any Pin	V_{SS} – 0.3V to V_{DD} + 0.3V
Operating Temperature Range	
CD4014M	–55°C to +125°C
CD4014C	–40°C to +85°C
Storage Temperature Range	–65°C to +150°C
Package Dissipation	500 mW
Operating V_{DD} Range	V_{SS} + 3V to V_{SS} + 15V
Lead Temperature (Soldering, 10 seconds)	300°C

dc electrical characteristics CD4014M

PARAMETERS	CONDITIONS	LIMITS									UNITS
		–55°C			25°C			125°C			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Quiescent Device Current (I_L)	V_{DD} = 5V			5		0.5	5			300	µA
	V_{DD} = 10V			10		1	10			600	µA
Quiescent Device Dissipation Package (P_D)	V_{DD} = 5V			25		2.5	25			1,500	µW
	V_{DD} = 10V			100		10	100			6,000	µW
Output Voltage Low-Level (V_{OL})	V_{DD} = 5V			0.01		0	0.01			0.05	V
	V_{DD} = 10V			0.01		0	0.01			0.05	V
Output Voltage High-Level (V_{OH})	V_{DD} = 5V	4.99			4.99	5		4.95			V
	V_{DD} = 10V	9.99			9.99	10		9.95			V
Noise Immunity (All Inputs) (V_{NL})	V_O = 0.8V, V_{DD} = 5V	1.5			1.5	2.25		1.4			V
	V_O = 1V, V_{DD} = 10V	3			3	4.5		2.9			V
Noise Immunity (All Inputs) (V_{NH})	V_O = 4.2V, V_{DD} = 5V	1.4			1.5	2.25		1.5			V
	V_O = 9V, V_{DD} = 10V	2.9			3	4.5		3			V
Output Drive Current N-Channel (I_DN)	V_O = 0.5V, V_{DD} = 5V	0.15			0.12	0.3		0.085			mA
	V_O = 0.5V, V_{DD} = 10V	0.31			0.25	0.5		0.175			mA
Output Drive Current P-Channel (I_DP)	V_O = 4.5V, V_{DD} = 5V	–0.1			–0.08	–0.16		–0.055			mA
	V_O = 9.5V, V_{DD} = 10V	–0.25			–0.20	–0.44		–0.14			mA
Input Current (I_I)						10					pA

dc electrical characteristics CD4014C

PARAMETERS	CONDITIONS	LIMITS									UNITS
		–40°C			25°C			85°C			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Quiescent Device Current (I_L)	V_{DD} = 5V			50		0.5	50			700	µA
	V_{DD} = 10V			100		1	100			1,400	µA
Quiescent Device Dissipation Package (P_D)	V_{DD} = 5V			250		2.5	250			3,500	µW
	V_{DD} = 10V			1,000		10	1,000			14,000	µW
Output Voltage Low-Level (V_{OL})	V_{DD} = 5V			0.01		0	0.01			0.05	V
	V_{DD} = 10V			0.01		0	0.01			0.05	V
Output Voltage High-Level (V_{OH})	V_{DD} = 5V	4.99			4.99	5		4.95			V
	V_{DD} = 10V	9.99			9.99	10		9.95			V
Noise Immunity (All Inputs) (V_{NL})	V_O = 0.8V, V_{DD} = 5V	1.5			1.5	2.25		1.4			V
	V_O = 1V, V_{DD} = 10V	3			3	4.5		2.9			V
Noise Immunity (All Inputs) (V_{NH})	V_O = 4.2V, V_{DD} = 5V	1.4			1.5	2.25		1.5			V
	V_O = 9V, V_{DD} = 10V	2.9			3	4.5		3			V
Output Drive Current N-Channel (I_DN)	V_O = 0.5V, V_{DD} = 5V	0.072			0.06	0.3		0.05			mA
	V_O = 0.5V, V_{DD} = 10V	0.12			0.1	0.5		0.08			mA
Output Drive Current P-Channel (I_DP)	V_O = 4.5V, V_{DD} = 5V	–0.06			–0.05	–0.16		–0.04			mA
	V_O = 9.5V, V_{DD} = 10V	–0.12			–0.1	–0.44		–0.08			mA
Input Current (I_I)						10					pA

ac electrical characteristics CD4014M

PARAMETERS	CONDITIONS	LIMITS			UNITS
		MIN	TYP	MAX	
Propagation Delay Time (t_{PHL}, t_{PLH})	V_{DD} = 5V		300	750	ns
	V_{DD} = 10V		100	225	ns
Transition Time (t_{THL}, t_{TLH})	V_{DD} = 5V		150	300	ns
	V_{DD} = 10V		75	125	ns
Minimum Clock Pulse Width (t_{WL}, t_{WH})	V_{DD} = 5V		200	500	ns
	V_{DD} = 10V		100	175	ns
Minimum High Level Parallel/Serial Control Pulse Width ($t_{WH(P/S)}$)	V_{DD} = 5V		200	500	ns
	V_{DD} = 10V		100	175	ns
Clock Rise Time (t_{rCL}) or Clock Fall Time (t_{fCL})	V_{DD} = 5V			15	μs
	V_{DD} = 10V			15	μs
Set-up Time	V_{DD} = 5V		100	350	ns
	V_{DD} = 10V		50	80	ns
Maximum Clock Frequency (f_{CL})	V_{DD} = 5V	1	2.5		MHz
	V_{DD} = 10V	3	5		MHz
Input Capacitance (C_I) (Note 2)	Any Input		5		pF

ac electrical characteristics CD4014C

PARAMETERS	CONDITIONS	LIMITS			UNITS
		MIN	TYP	MAX	
Propagation Delay Time (t_{PHL}, t_{PLH})	V_{DD} = 5V		300	1,000	ns
	V_{DD} = 10V		100	300	ns
Transition Time (t_{THL}, t_{TLH})	V_{DD} = 5V		150	400	ns
	V_{DD} = 10V		75	150	ns
Minimum Clock Pulse Width (t_{WL}, t_{WH})	V_{DD} = 5V		200	830	ns
	V_{DD} = 10V		100	200	ns
Minimum High Level Parallel/Serial Control Pulse Width ($t_{WH(P/S)}$)	V_{DD} = 5V		200	830	ns
	V_{DD} = 10V		100	200	ns
Clock Rise Time (t_{rCL}) or Clock Fall Time (t_{fCL})	V_{DD} = 5V			15	μs
	V_{DD} = 10V			15	μs
Set-up Time	V_{DD} = 5V		100	500	ns
	V_{DD} = 10V		50	100	ns
Maximum Clock Frequency (f_{CL})	V_{DD} = 5V	0.6	2.5		MHz
	V_{DD} = 10V	2.5	5		MHz
Input Capacitance (C_I) (Note 2)	Any Input		5		pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

CD4015M/CD4015C dual 4-bit static register

general description

The CD4015M/CD4015C consist of two identical, independent, 4-stage serial-input/parallel-output registers. Each register has independent "Clock" and "Reset" inputs as well as a single serial "Data" input. "Q" outputs are available from each of the four stages on both registers. All register stages are D-type, master-slave flip-flops. The logic level present at the data input is transferred into the first register stage and shifted over one stage at each positive-going clock transition. Resetting of all stages is accomplished by a high level on the reset line. Register expansion to 8 stages using one CD4015M/CD4015C package, or to more than 8 stages using additional CD4015M/CD4015C is possible. All inputs are protected from static discharge by diode clamps to V_{DD} and V_{SS}.

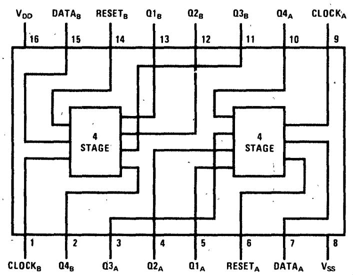
features

■ Wide supply voltage range	3.0V to 15V
■ High noise immunity	0.45 V_{CC} typ
■ Medium speed operation	9 MHz (typ) clock rate at $V_{DD} - V_{SS} = 10V$
■ Fully static operation	

applications

- Serial-input/parallel-output data queueing
- Serial to parallel data conversion
- General purpose register

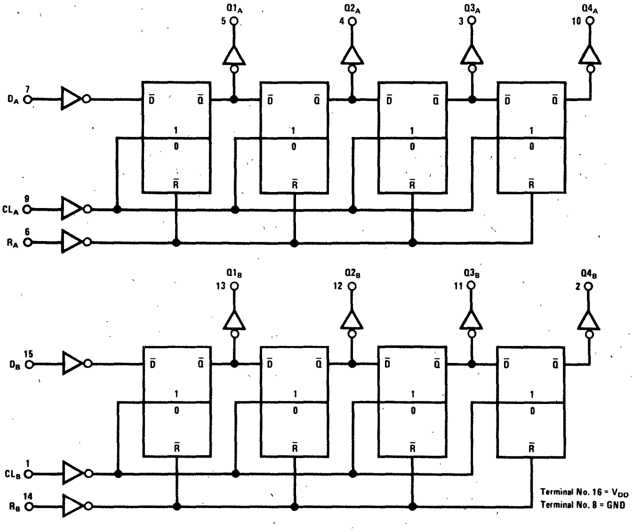
connection diagram and truth table



CL▲	D	R	Q1	Q_n	
↗	0	0	0	Q_{n-1}	
↗	1	0	1	Q_{n-1}	
↘	X	0	Q1	Q_n	(No change)
X	X	1	0	0	

▲ Level change.
X Don't care case.

logic diagrams



Terminal No. 16 = V_{DD}
Terminal No. 8 = GND

absolute maximum ratings (Note 1)

Voltage at Any Pin	V_{SS} – 0.3V to V_{DD} + 0.3V
Operating Temperature Range	
CD4015M	–55°C to +125°C
CD4015C	–40°C to +85°C
Storage Temperature Range	–65°C to +150°C
Package Dissipation	500 mW
Operating V_{DD} – V_{SS} Range	3.0V to 15V
Lead Temperature (Soldering, 10 seconds)	300°C

dc electrical characteristics CD4015M

PARAMETER	CONDITIONS	LIMITS									UNITS
		–55°C			25°C			125°C			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Quiescent Device Current (I_L)	V_{DD} = 5V			5		0.5	5			300	µA
	V_{DD} = 10V			10		1	10			600	µA
Quiescent Device Dissipation/Package (P_D)	V_{DD} = 5V			25		2.5	25			1500	µW
	V_{DD} = 10V			100		10	100			6000	µW
Output Voltage Low Level (V_{OL})	V_{DD} = 5V			0.01		0	0.01			0.05	V
	V_{DD} = 10V			0.01		0	0.01			0.05	V
Output Voltage High Level (V_{OH})	V_{DD} = 5V	4.99			4.99	5		4.95			V
	V_{DD} = 10V	9.99			9.99	10		9.95			V
Noise Immunity (Any Input) (V_{NL})	V_{DD} = 5V, V_O = 0.8V	1.5			1.5	2.25		1.4			V
	V_{DD} = 10V, V_O = 1.0V	3			3	4.5		2.9			V
Noise Immunity (Any Input) (V_{NH})	V_{DD} = 5V, V_O = 4.2V	1.4			1.5	2.25		1.5			V
	V_{DD} = 10V, V_O = 9.0V	2.9			3	4.5		3			V
Output Drive Current N-Channel (I_DN)	V_{DD} = 5V, V_O = 0.5V	0.15			0.12	0.3		0.085			mA
	V_{DD} = 10V, V_O = 0.5V	0.31			0.25	0.5		0.175			mA
Output Drive Current P-Channel (I_DP)	V_{DD} = 5V, V_O = 4.5V	–0.1			–0.08	–0.16		–0.055			mA
	V_{DD} = 10V, V_O = 9.5V	–0.25			–0.20	–0.44		–0.14			mA
Input Current (I_I)						10					pA

dc electrical characteristics CD4015C

PARAMETER	CONDITIONS	LIMITS									UNITS
		–40°C			25°C			85°C			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Quiescent Device Current (I_L)	V_{DD} = 5V			50		0.5	50			700	µA
	V_{DD} = 10V			100		1	100			1400	µA
Quiescent Device Dissipation/Package (P_D)	V_{DD} = 5V			250		2.5	250			3500	µW
	V_{DD} = 10V			1000		10	1000			14000	µW
Output Voltage Low Level (V_{OL})	V_{DD} = 5V			0.01		0	0.01			0.05	V
	V_{DD} = 10V			0.01		0	0.01			0.05	V
Output Voltage High Level (V_{OH})	V_{DD} = 5V	4.99			4.99	5		4.95			V
	V_{DD} = 10V	9.99			9.99	10		9.95			V
Noise Immunity (Any Input (V_{NL})	V_{DD} = 5V, V_O = 0.8V	1.5			1.5	2.25		1.4			V
	V_{DD} = 10V, V_O = 1.0V	3			3	4.5		2.9			V
Noise Immunity (Any Input (V_{NH})	V_{DD} = 5V, V_O = 4.2V	1.4			1.5	2.25		1.5			V
	V_{DD} = 10V, V_O = 9.0V	2.9			3	4.5		3			V
Output Drive Current N-Channel (I_DN)	V_{DD} = 5V, V_O = 0.5V	0.072			0.06	0.3		0.05			mA
	V_{DD} = 10V, V_O = 0.5V	0.12			0.1	0.5		0.08			mA
Output Drive Current P-Channel (I_DP)	V_{DD} = 5V, V_O = 4.5V	–0.06			–0.05	–0.16		–0.04			mA
	V_{DD} = 10V, V_O = 9.5V	–0.12			–0.1	–0.44		–0.08			mA
Input Current (I_I)						10					pA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

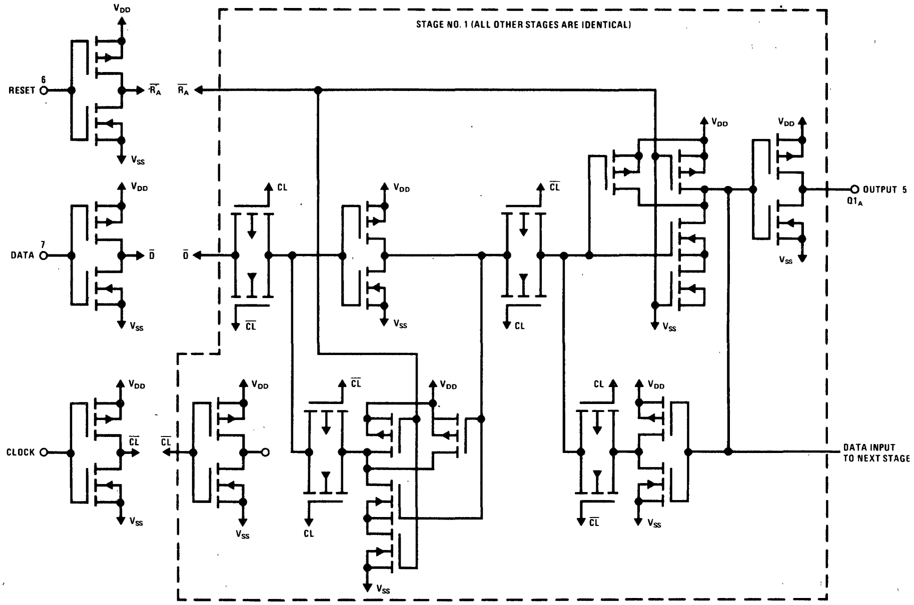
ac electrical characteristics CD4015M

PARAMETER	CONDITIONS	LIMITS			UNITS
		MIN	TYP	MAX	
CLOCKED OPERATION					
Propagation Delay Time (t_{PHL}, t_{PLH})	$V_{DD} = 5V$		250	750	ns
	$V_{DD} = 10V$		100	225	ns
Transition Time (t_{THL}, t_{TLH})	$V_{DD} = 5V$		150	300	ns
	$V_{DD} = 10V$		75	125	ns
Minimum Clock Pulse Width (t_{WL}, t_{WH})	$V_{DD} = 5V$		100	500	ns
	$V_{DD} = 10V$		50	175	ns
Clock Rise and Fall Time (t_{rCL}, t_{fCL})	$V_{DD} = 5V$			15	μs
	$V_{DD} = 10V$			15	μs
Set-Up Time	$V_{DD} = 5V$		50	350	ns
	$V_{DD} = 10V$		25	80	ns
Maximum Clock Frequency (f_{CL})	$V_{DD} = 5V$	1	4		MHz
	$V_{DD} = 10V$	3	9		MHz
Input Capacitance (C_I)			5		pF
RESET OPERATION					
Propagation Delay Time ($t_{PHL(R)}$)	$V_{DD} = 5V$		200	750	ns
	$V_{DD} = 10V$		100	225	ns
Minimum Set and Reset Pulse Widths ($t_{WH(R)}$)	$V_{DD} = 5V$		150	500	ns
	$V_{DD} = 10V$		100	175	ns

ac electrical characteristics CD4015C

PARAMETER	CONDITIONS	LIMITS			UNITS
		MIN	TYP	MAX	
CLOCKED OPERATION					
Propagation Delay Time (t_{PHL}, t_{PLH})	$V_{DD} = 5V$		250	1000	ns
	$V_{DD} = 10V$		100	300	ns
Transition Time (t_{THL}, t_{TLH})	$V_{DD} = 5V$		150	400	ns
	$V_{DD} = 10V$		75	150	ns
Minimum Clock Pulse Width (t_{WL}, t_{WH})	$V_{DD} = 5V$		100	830	ns
	$V_{DD} = 10V$		50	200	ns
Clock Rise and Fall Time	$V_{DD} = 5V$			15	μs
	$V_{DD} = 10V$			15	μs
Set-Up Time	$V_{DD} = 5V$		50	500	ns
	$V_{DD} = 10V$		25	100	ns
Maximum Clock Frequency (f_{CL})	$V_{DD} = 5V$	0.6	4		MHz
	$V_{DD} = 10V$	2.5	9		MHz
Input Capacitance (C_I)			5		pF
RESET OPERATION					
Propagation Delay Time ($t_{PHL(R)}$)	$V_{DD} = 5V$		200	1000	ns
	$V_{DD} = 10V$		100	300	ns
Minimum Set and Reset Pulse Widths ($t_{WH(R)}$)	$V_{DD} = 5V$		150	830	ns
	$V_{DD} = 10V$		100	200	ns

schematic diagram



CD4016M/CD4016C quad bilateral switch

general description

The CD4016M/CD4016C is a quad bilateral switch which utilizes P-channel and N-channel complementary MOS (CMOS) circuits to provide an extremely high "OFF" resistance and low "ON" resistance switch. The switch will pass signals in either direction and is extremely useful in digital switching.

■ Extremely low leakage	$V_{is} = 5\ V_{p\text{-}p}$ $V_{DD} - V_{SS} = 10V$ $R_L = 10\ k\Omega$
■ Transmits frequencies up to 10 MHz	

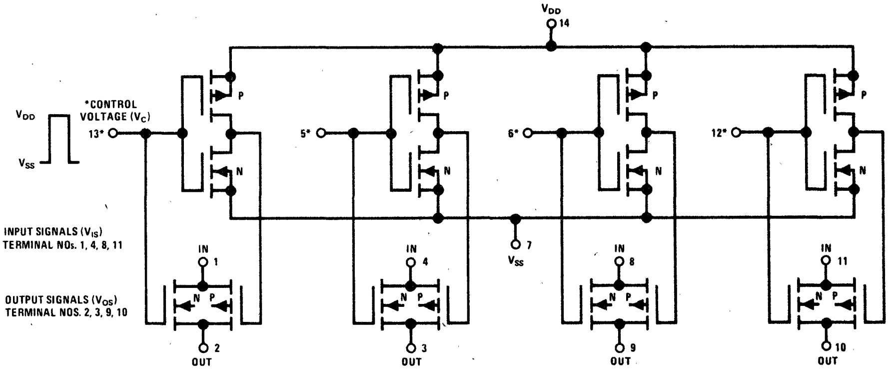
features

■ Wide supply voltage range	3V to 15V
■ High noise immunity	$0.45\ V_{CC}$ typ.
■ Wide range of digital and analog levels	$\pm 7.5\ V_{PEAK}$
■ Low "ON" resistance	300Ω typ. $V_{DD} - V_{SS} = 15V$
■ Matched switch characteristics	$\Delta R_{ON} = 40\Omega$ typ.
■ High "ON/OFF" output voltage ratio	65 dB typ. @ $f_{is} = 10$ kHz $R_L = 10k$
■ High degree of linearity	.5% distortion typ. @ $f_{is} = 1$ kHz

applications

- Analog signal switching/multiplexing
  - Signal gating
  - Squelch control
  - Chopper
  - Modulator
  - Demodulator
  - Commutating switch
- Digital signal switching/multiplexing
- CMOS logic implementation
- Analog to digital/digital to analog conversion
- Digital control of frequency, impedance, phase, and analog-signal gain

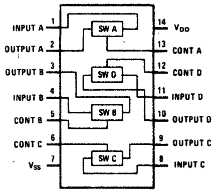
schematic and connection diagrams



Note 1: All switch P-channel substrates are internally connected to terminal No. 14.
Note 2: All switch N-channel substrates are internally connected to terminal No. 7.

Signal-level range: $V_{SS} < V_{is} > V_{DD}$

Normal operation: Control-line biasing, switch ON V_C "1" = V_{DD}, switch OFF V_C "0" = V_{SS}



TOP VIEW

absolute maximum ratings

Voltage at Any Pin (Note 1)		V_{SS} −0.3V to V_{SS} +15.5V
Operating Temperature Range	CD4016M	−55°C to +125°C
	CD4016C	−40°C to +85°C

Storage Temperature Range	−65°C to +150°C
Package Dissipation	500 mW
Lead Temperature (Soldering, 10 sec)	300°C
Operating V_{DD} Range	V_{SS} +3V to V_{SS} +15V

electrical characteristics CD4016M

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS									UNITS
			-55°C			25°C			125°C			
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Quiescent Dissipation per Package All Switches "OFF"	P_T	TERMINALS VOLTS APPLIED V_{DD} 14 +10 V_{SS} 7 GND V_C 5, 6, 12, 13 GND V_{is} 1, 4, 8, 11 ≤ +10 V_{os} 2, 3, 9, 10 ≤ +10			5		0.1	5			300	μW
All Switches "ON"		TERMINALS VOLTS APPLIED V_{DD} 14 +10 V_{SS} 7 GND V_C 5, 6, 12, 13 +10 $V_{is} = V_{OS}$ 1-4, 8-11 ≤ +10			5		0.1	5			300	μW
Threshold Voltage N-Channel	$V_{TH}N$	$I_{DS} = 10\ \mu A$ V_{DD} = 5V, 10V, or 15V		1.7			1.5			1.3		V
P-Channel	$V_{TH}P$	$I_{DS} = -10\ \mu A$ V_{DD} = 5V, 10V, or 15V		-1.7			-1.5			-1.3		V
SIGNAL INPUTS (V_{is}) AND OUTPUTS (V_{os})												
"ON" Resistance	R_{ON}	$R_L = 10k\Omega$ $V_C = V_{DD}$ V_{SS} V_{is}										
		+7.5V		120	360		200	400		300	600	
		+7.5V −7.5V −7.5V		120	360		200	400		300	600	Ω
		±0.25V		130	775		280	850		470	1230	
		+5V		130	600		250	660		400	960	
		+5V −5V -5V		130	600		250	660		400	960	Ω
		±0.25V		325	1870		580	2000		900	2600	
		+15V		120	360		200	400		300	600	
		+15V 0V +0.25V		120	360		200	400		300	600	Ω
		9.3V		150	775		300	850		490	1230	
		+10V		130	600		250	660		400	960	
		+10V 0V +0.25V		130	600		250	660		400	960	Ω
		5.6V		300	1870		560	2000		880	2600	
Δ "ON" Resistance Between Any 2 of 4 Switches	ΔR_{ON}	+7.5V −7.5V ±7.5V					10					Ω
		+5V −5V ±5V					15					
Sine Wave Response (Distortion)		R_L = 10 kΩ f_{is} = 1 kHz +5V −5V 5V(p-p) (Note 3)					0.4					%
Input or Output Leakage—Switch "OFF" (Effective "OFF" Resistance)		V_{DD} $V_C = V_{SS}$ V_{is}										
		+7.5V −7.5V +7.5V					±100					pA
		−7.5V					±100					
		+5V −5V +5V					(Note 2)	125				nA
		−5V					(Note 2)	125				
Frequency Response—Switch "ON" (Sine Wave Input)		$V_C = V_{DD}$ = +5V, V_{SS} = −5V R_L = 1 kΩ V_{is} = 5V(p-p) $20 \text{ Log}_{10} \frac{V_{os}}{V_{is}} = -3$ dB					40					MHz
Feedthrough Switch "OFF"		V_{DD} = +5V, $V_C = V_{SS}$ = −5V $20 \text{ Log}_{10} \frac{V_{os}}{V_{is}} = -50$ dB					1.25					MHz
Crosstalk Between any 2 of the 4 switches (Frequency at −50 dB)		R_L = 1 kΩ $V_{is}(A)$ = 5V(p-p) $V_C(A) = V_{DD}$ = +5V $V_C(B) = V_{SS}$ = −5V $20 \text{ Log}_{10} \frac{V_{os}(B)}{V_{is}(A)} = -50$ dB					0.9					MHz
Capacitance Input	C_{IS}	V_{DD} = +5V, $V_C = V_{SS}$ = −5V					4					
Output	C_{OS}						4					pF
Feedthrough	C_{IOS}						0.2					
Propagation Delay Signal Input to Signal Output	t_{pd}	$V_C = V_{DD}$ = +10V, V_{SS} = GND, C_L = 15 pF V_{is} = 10V (square wave) $t_r = t_f$ = 20 ns (input signal)					10					ns
CONTROL (V_C)												
Switch Threshold Voltage	$V_{TH}C$	$V_{is} \le V_{DD}$ $V_{DD} - V_{SS}$ = 15V, 10V, 5V I_{IS} = 10 μA	0.7		2.9	0.5	1.5	2.7	0.2		2.4	V
Input Current	I_C	$V_{DD} - V_{SS}$ = 10V $V_C \le V_{DD} - V_{SS}$					±10					pA
Average Input Capacitance	C_C						5					pF
Crosstalk – Control Input to Signal Output		$V_{DD} - V_{SS}$ = 10V V_C = 10V (square wave) R_L = 10 kΩ					50					mV
Turn "ON" Propagation Delay	$t_{pd}C$	$t_{rc} = t_{fc}$ = 20 ns $V_{is} \le 10V$, C_L = 15 pF					20					ns
Maximum Allowable Control Input Repetition Rate		V_{DD} = 10V, V_{SS} = GND, R_L = 1 kΩ C_L = 15 pF V_C = 10V (square wave) $t_r = t_f$ = 20 ns					10					MHz

Note 1: The device should not be connected to circuits with the power on.

Note 2: ±10 X 10^{-3}.

Note 3: Symmetrical about 0V.

electrical characteristics CD4016C

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS									UNITS
			−40°C			25°C			85°C			
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Quiescent Dissipation per Package All Switches "OFF"	P_T	TERMINALS VOLTS APPLIED V_{DD} 14 +10 V_{SS} 7 GND V_C 5, 6, 12, 13 GND V_{is} 1, 4, 8, 11 $\leq +10$ V_{os} 2, 3, 9, 10 $\leq +10$			5		0.1	5			80	µW
All Switches "ON"		TERMINALS VOLTS APPLIED V_{DD} 14 +10 V_{SS} 7 GND V_C 5, 6, 12, 13 +10 $V_{is} = V_{OS}$ 1-4, 8-11 $\leq +10$			5		0.1	5			80	µW
Threshold Voltage N-Channel	$V_{TH}N$	$I_{DS} = 10\ \mu A$ $V_{DD} = 5V, 10V$, or $15V$		1.7			1.5			1.3		V
P-Channel	$V_{TH}P$	$I_{DS} = 10\ \mu A$ $V_{DD} = 5V, 10V$, or $15V$		−1.7			−1.5			−1.3		V
SIGNAL INPUTS (V_{is}) AND OUTPUTS (V_{os})												
		$V_C = V_{DD}$ V_{SS} V_{is}										
		+7.5V		130	370		200	400		260	520	
		+7.5V −7.5V −7.5V		130	370		200	400		260	520	Ω
		±0.25V		160	790		280	850		400	1080	
		+5V		150	610		250	660		340	840	
		+5V −5V −5V		150	610		250	660		340	840	Ω
"ON" Resistance	R_{ON}	$R_L = 10k\Omega$ ±0.25V		370	1900		580	2000		770	2380	
		+15V		130	370		200	400		260	520	
		+15V 0V +0.25V		130	370		200	400		260	520	Ω
		9.3V		180	790		300	850		400	1080	
		+10V		150	610		250	660		340	840	
		+10V 0V +0.25V		150	610		250	660		340	2380	Ω
		5.6V		350	1900		560	2000		750	2380	
Δ "ON" Resistance Between Any 2 of 4 Switches	ΔR_{ON}	+7.5V −7.5V ±7.5V +5V −5V ±5V					10 15					Ω
Sine Wave Response (Distortion)		$R_L = 10\ k\Omega$ $f_{is} = 1\ kHz$ +5V −5V 5V(p-p) (Note 3)					0.4					%
		V_{DD} $V_C = V_{SS}$ V_{is}										
Input or Output Leakage—Switch "OFF" (Effective "OFF" Resistance)		+7.5V −7.5V +7.5V −7.5V					±100 ±100					pA
		+5V −5V +5V −5V					(Note 2) (Note 2)	125 125				nA
Frequency Response—Switch "ON" (Sine Wave Input)		$R_L = 1\ k\Omega$ $V_{is} = 5V(p\text{-}p)$ $V_C = V_{DD} = +5V$, $V_{SS} = -5V$ $20\ \text{Log}_{10} \frac{V_{os}}{V_{is}} = -3\ dB$					40					MHz
Feedthrough Switch "OFF"		$V_{DD} = +5V$, $V_C = V_{SS} = -5V$ $20\ \text{Log}_{10} \frac{V_{os}}{V_{is}} = -50\ dB$					1.25					MHz
Crosstalk Between any 2 of the 4 switches (Frequency at −50 dB)		$R_L = 1\ k\Omega$ $V_{is}(A) =$ 5V(p-p) $V_C(A) = V_{DD} = +5V$ $V_C(B) = V_{SS} = -5V$ $20\ \text{Log}_{10} \frac{V_{os}(B)}{V_{is}(A)} = -50\ dB$					0.9					MHz
Capacitance Input	C_{IS}	$V_{DD} = +5V$, $V_C = V_{SS} = -5V$					4					
Output	C_{OS}						4					pF
Feedthrough	C_{IOS}						0.2					
Propagation Delay Signal Input to Signal Output	t_{pd}	$V_C = V_{DD} = +10V$, $V_{SS} = GND$, $C_L = 15\ pF$ $V_{is} = 10V$ (square wave) $t_r = t_f = 20\ ns$ (input signal)					10					ns
CONTROL (V_C)												
Switch Threshold Voltage	$V_{TH}C$	$V_{is} \leq V_{DD}$ $V_{DD} - V_{SS} = 15V, 10V, 5V$ $I_{IS} = 10\ \mu A$				0.5	1.5	2.7				V
Input Current	I_C	$V_{DD} - V_{SS} = 10V$ $V_C \leq V_{DD} - V_{SS}$					±10					pA
Average Input Capacitance	C_C						5					pF
Crosstalk — Control Input to Signal Output		$V_{DD} - V_{SS} = 10V$ $V_C = 10V$ (square wave) $R_L = 10\ k\Omega$					50					mV
Turn "ON" Propagation Delay	$t_{pd}C$	$t_{rc} = t_{fc} = 20\ ns$ $V_{is} < 10V$, $C_L = 15\ pF$					20					ns
Maximum Allowable Control Input Repetition Rate		$V_{DD} = 10V$, $V_{SS} = GND$, $R_L = 1\ k\Omega$ $C_L = 15\ pF$ $V_C = 10V$ (square wave) $t_r = t_f = 20\ ns$					10					MHz

Note 1: The device should not be connected to circuits with the power on.

Note 2: $\pm 10 \times 10^{-3}$.

Note 3: Symmetrical about 0V.

typical ON resistance characteristics

CHARACTERISTIC*	SUPPLY CONDITIONS		LOAD CONDITIONS					
			R_L = 1 kΩ		R_L = 10 kΩ		R_L = 100 kΩ	
	V_{DD} (V)	V_{SS} (V)	VALUE (Ω)	V_{is} (V)	VALUE (Ω)	V_{is} (V)	VALUE (Ω)	V_{is} (V)
R_{ON}	+15	0	200	+15	200	+15	180	+15
			200	0	200	0	200	0
R_{ON} (max.)	+15	0	300	+11	300	+9.3	320	+9.2
R_{ON}	+10	0	290	+10	250	+10	240	+10
			290	0	250	0	300	0
R_{ON} (max.)	+10	0	500	+7.4	560	+5.6	610	+5.5
R_{ON}	+5	0	860	+5	470	+5	450	+5
			600	0	580	0	800	0
R_{ON} (max.)	+5	0	1.7k	+4.2	7k	+2.9	33k	+2.7
R_{ON}	+7.5	−7.5	200	+7.5	200	+7.5	180	+7.5
			200	−7.5	200	−7.5	180	−7.5
R_{ON} (max.)	+7.5	−7.5	290	±0.25	280	±25	400	±0.25
R_{ON}	+5	−5	260	+5	250	+5	240	+5
			310	−5	250	−5	240	−5
R_{ON} (max.)	+5	−5	600	±0.25	580	±0.25	760	±0.25
R_{ON}	+2.5	−2.5	590	+2.5	450	+2.5	490	+2.5
			720	−2.5	520	−2.5	520	−2.5
R_{ON} (max.)	+2.5	−2.5	232k	±0.25	300k	±0.25	870k	±0.25

*Variation from a perfect switch: R_{ON} = 0Ω.

CD4017M/CD4017C divide-by-10 counter/divider with 10 decoded outputs

general description

The CD4017M/CD4017C is a 5-stage divide-by-10 Johnson counter with 10 decoded outputs and a carry out bit. The counter is cleared to its zero count by a logical "1" on its reset line. The counter is advanced on the positive edge of the clock signal when the clock enable signal is in the logical "0" state.

The configuration of the CD4017M/CD4017C permits medium speed operation and assures a hazard free counting sequence. The 10 decoded outputs are normally in the logical "0" state and go to the logical "1" state only at their respective time slot. Each decoded output remains high for 1 full clock cycle. The carry-out signal completes a full cycle for every 10 clock input cycles and is used as a ripple carry signal to any succeeding stages.

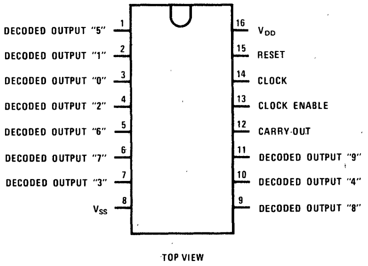
features

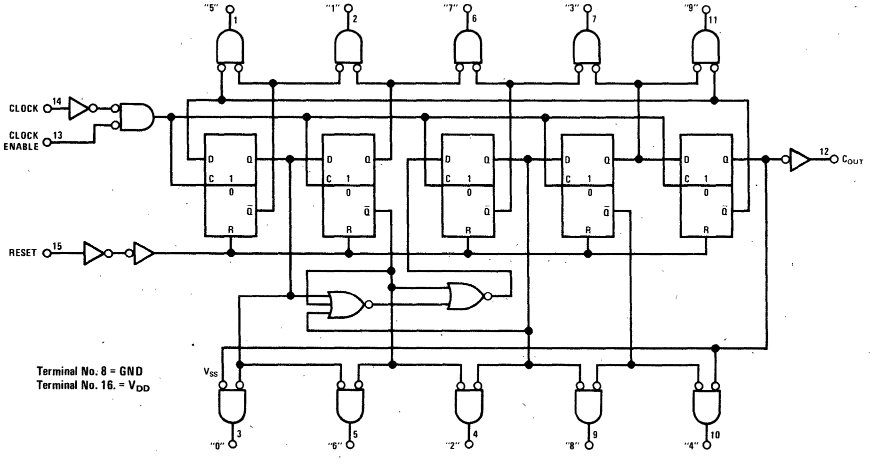
■ Wide supply voltage range	3.0V to 15V
■ High noise immunity	0.45 V_{DD} typ
■ Medium speed operation	5.0 MHz typ with 10V V_{DD}
■ Low power	10μW typ
■ Fully static operation	

applications

- Automotive
- Instrumentation
- Medical electronics
- Alarm systems
- Industrial electronics
- Remote metering

connection and logic diagrams





Terminal No. 8 = GND
Terminal No. 16 = V_{DD}

absolute maximum ratings

Voltage at Any Pin	V_{SS} − 0.3V to V_{SS} + 15.5V
Operating Temperature Range	
CD4017M	−55°C to +125°C
CD4017C	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500 mW
Operating V_{DD} Range	V_{SS} + 3.0V to V_{SS} + 15V
Lead Temperature (Soldering, 10 seconds)	300°C

dc electrical characteristics CD4017M

PARAMETER	CONDITIONS	LIMITS									UNITS
		-55°C			25°C			125°C			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Quiescent Device Current (I_L)	V_{DD} = 5.0V			5.0		0.3	5.0			300	µA
	V_{DD} = 10V			10		0.5	10			600	µA
Quiescent Device Dissipation/Package (P_D)	V_{DD} = 5.0V			25		1.5	25			1,500	µW
	V_{DD} = 10V			100		5.0	100			6,000	µW
Output Voltage Low Level (V_{OL})	V_{DD} = 5.0V			0.01		0	0.01			0.05	V
	V_{DD} = 10V			0.01		0	0.01			0.05	V
Output Voltage High Level (V_{OH})	V_{DD} = 5.0V	4.99			4.99	5.0		4.95			V
	V_{DD} = 10V	9.99			9.99	10		9.95			V
Noise Immunity (V_{NL}) (All Inputs)	V_{DD} = 5.0V, V_O = 0.8V	1.5			1.5	2.25		1.4			V
	V_{DD} = 10V, V_O = 1.0V	3.0			3.0	4.5		2.9			V
Noise Immunity (V_{NH}) (All Inputs)	V_{DD} = 5.0V, V_O = 4.2V	1.4			1.5	2.25		1.5			V
	V_{DD} = 10V, V_O = 9.0V	2.9			3.0	4.5		3.0			V
Output Drive Current N-Channel (I_DN)	Decoded Outputs										
	V_{DD} = 5.0V, V_O = 0.5V	0.06			0.05	0.1		0.035			mA
	V_{DD} = 10V, V_O = 0.5V	0.12			0.1	0.4		0.07			mA
Output Drive Current N-Channel (I_DN)	Carry Outputs										
	V_{DD} = 5.0V, V_O = 0.5V	0.185			0.15	0.4		0.105			mA
	V_{DD} = 10V, V_O = 0.5V	0.45			0.35	1.0		0.25			mA
Output Drive Current P-Channel (I_DP)	Decoded Outputs										
	V_{DD} = 5.0V, V_O = 4.5V	-0.0375			-0.03	-0.075		-0.021			mA
	V_{DD} = 10V, V_O = 9.5V	-0.12			-0.1	-0.2		-0.07			mA
Output Drive Current P-Channel (I_DP)	Carry Output										
	V_{DD} = 5.0V, V_O = 4.5V	-0.185			-0.15	-0.4		-0.105			mA
	V_{DD} = 10V, V_O = 9.5V	-0.45			-0.35	-1.0		-0.25			mA
Input Current (I_I)						10					pA

dc electrical characteristics CD4017C

PARAMETER	CONDITIONS	LIMITS									UNITS
		-40°C			25°C			85°C			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Quiescent Device Current (I_L)	V_{DD} = 5.0V			50		0.5	50			700	µA
	V_{DD} = 10V			100		1.0	100			1,400	µA
Quiescent Device Dissipation/Package (P_D)	V_{DD} = 5.0V			250		2.5	250			3,500	µW
	V_{DD} = 10V			1,000		10	1,000			14,000	µW
Output Voltage Low Level (V_{OL})	V_{DD} = 5.0V			0.01		0	0.01			0.05	V
	V_{DD} = 10V			0.01		0	0.01			0.05	V
Output Voltage High Level (V_{OH})	V_{DD} = 5.0V	4.99			4.99	5.0		4.95			V
	V_{DD} = 10V	9.99			9.99	10		9.95			V
Noise Immunity (V_{NL}) (All Inputs)	V_{DD} = 5.0V, V_O = 0.8V	1.5			1.5	2.25		1.4			V
	V_{DD} = 10V, V_O = 1.0V	3.0			3.0	4.5		2.9			V
Noise Immunity (V_{NH}) (All Inputs)	V_{DD} = 5.0V, V_O = 4.2V	1.4			1.5	2.25		1.5			V
	V_{DD} = 10V, V_O = 9.0V	2.9			3.0	4.5		3.0			V
Output Drive Current N-Channel (I_DN)	Decoded Outputs										
	V_{DD} = 5.0V, V_O = 0.5V	0.03			0.025	0.1		0.02			mA
	V_{DD} = 10V, V_O = 0.5V	0.085			0.07	0.4		0.055			mA
Output Drive Current N-Channel (I_DN)	Carry Outputs										
	V_{DD} = 5.0V, V_O = 0.5V	0.095			0.08	0.4		0.065			mA
	V_{DD} = 10V, V_O = 0.5V	0.3			0.25	1.0		0.2			mA
Output Drive Current P-Channel (I_DP)	Decoded Outputs										
	V_{DD} = 5.0V, V_O = 4.5V	-0.018			-0.015	-0.075		-0.012			mA
	V_{DD} = 10V, V_O = 9.5V	-0.085			-0.07	-0.2		-0.055			mA
Output Drive Current P-Channel (I_DP)	Carry Outputs										
	V_{DD} = 5.0V, V_O = 4.5V	-0.095			-0.08	-0.4		-0.065			mA
	V_{DD} = 10V, V_O = 9.5V	-0.3			-0.24	1.0		-0.20			mA
Input Current (I_I)						10					pA

ac electrical characteristics CD4017M

$T_A = 25°C$ and $C_L = 15$ pF. Typical Temperature Coefficient for all values of $V_{DD} = 0.3\%/°C$.

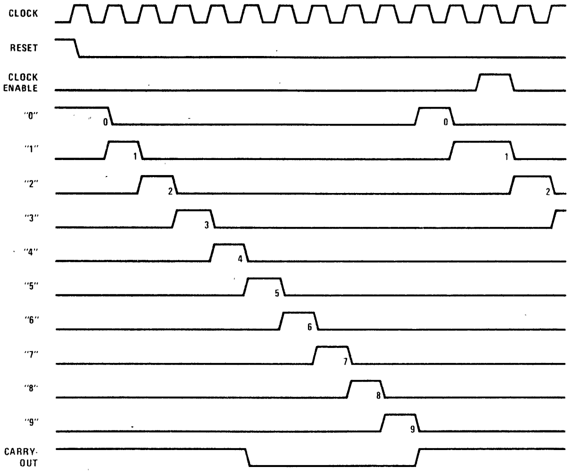
PARAMETER	CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
CLOCKED OPERATION					
Propagation Delay Time Carry-Out Line (t_{PHL})	$V_{DD} = 5.0V$		350	1000	ns
	$V_{DD} = 10V$		125	250	ns
Propagation Delay Time Decode Out Lines (t_{PLH})	$V_{DD} = 5.0V$		500	1200	ns
	$V_{DD} = 10V$		200	400	ns
Transition Time Carry-Out Line (t_{THL})	$V_{DD} = 5.0V$		100	300	ns
	$V_{DD} = 10V$		50	150	ns
Transition Time Decode-Out Line (t_{rLH})	$V_{DD} = 5.0V$		300	900	ns
	$V_{DD} = 10V$		125	350	ns
Minimum Clock Pulse Width (t_{WL})	$V_{DD} = 5.0V$		200	500	ns
Minimum Clock Pulse Width (t_{WH})	$V_{DD} = 10V$		100	170	ns
Clock Rise and Fall Time (t_{rCL})	$V_{DD} = 5.0V$			15	µs
Clock Rise and Fall Time (t_{fCL})	$V_{DD} = 10V$			15	µs
Set-Up Time	$V_{DD} = 5.0V$		100	500	ns
	$V_{DD} = 10V$		50	200	ns
Maximum Clock Frequency (f_{CL})	$V_{DD} = 5.0V$	1.0	2.5		MHz
	$V_{DD} = 10V$	3.0	5.0		MHz
Input Capacitance (C_I)	Any Input		5.0		pF
RESET OPERATION					
Propagation Delay Time To Carry Out Line ($t_{PHL(R)}$)	$V_{DD} = 5.0V$		350	1000	ns
	$V_{DD} = 10V$		125	250	ns
Propagation Delay Time To Decode Out Lines ($t_{PHL(R)}$)	$V_{DD} = 5.0V$		450	1200	ns
	$V_{DD} = 10V$		200	400	ns
Reset Pulse Width ($t_{WH(R)}$)	$V_{DD} = 5.0V$		200	500	ns
	$V_{DD} = 10V$		100	165	ns
Reset Removal Time	$V_{DD} = 5.0V$		300	750	ns
	$V_{DD} = 10V$		100	225	ns

ac electrical characteristics CD4017C

$T_A = 25°C$ and $C_L = 15$ pF. Typical Temperature Coefficient for all values of $V_{DD} = 0.3\%/°C$.

PARAMETER	CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
CLOCKED OPERATION					
Propagation Delay Time Carry-Out Line (t_{PHL})	$V_{DD} = 5.0V$		350	1300	ns
	$V_{DD} = 10V$		125	300	ns
Propagation Delay Time Decode Out Lines (t_{PLH})	$V_{DD} = 5.0V$		500	1600	ns
	$V_{DD} = 10V$		200	500	ns
Transition Time Carry-Out Line (t_{THL})	$V_{DD} = 5.0V$		100	350	ns
	$V_{DD} = 10V$		50	200	ns
Transition Time Decode-Out Line (t_{TLH})	$V_{DD} = 5.0V$		300	1200	ns
	$V_{DD} = 10V$		125	450	ns
Minimum Clock Pulse Width (t_{WL})	$V_{DD} = 5.0V$		200	830	ns
Minimum Clock Pulse Width (t_{WH})	$V_{DD} = 10V$		100	250	ns
Clock Rise and Fall Time (t_{rCL})	$V_{DD} = 5.0V$			15	µs
Clock Rise and Fall Time (t_{fCL})	$V_{DD} = 10V$			15	µs
Set-Up Time	$V_{DD} = 5.0V$		100	700	ns
	$V_{DD} = 10V$		50	300	ns
Maximum Clock Frequency (f_{CL})	$V_{DD} = 5.0V$	0.6	2.5		MHz
	$V_{DD} = 10V$	2.5	5.0		MHz
Input Capacitance (C_I)	Any Input		5.0		pF
RESET OPERATION					
Propagation Delay Time To Carry Out Line ($t_{PHL(R)}$)	$V_{DD} = 5.0V$		350	1300	ns
	$V_{DD} = 10V$		125	300	ns
Propagation Delay Time To Decode Out Lines ($t_{PHL(R)}$)	$V_{DD} = 5.0V$		450	1600	ns
	$V_{DD} = 10V$		200	500	ns
Reset Pulse Width ($t_{WH(R)}$)	$V_{DD} = 5.0V$		200	830	ns
	$V_{DD} = 10V$		100	250	ns
Reset Removal Time	$V_{DD} = 5.0V$		300	1000	ns
	$V_{DD} = 10V$		100	275	ns

switching time waveforms



CD4019M/CD4019C quad AND-OR select gate

general description

The CD4019M/CD4019C is a Complementary MOS quad AND-OR select gate. Low power and high noise margin over a wide voltage range is possible through implementation of N AND P-channel enhancement mode transistors. These Complementary MOS (CMOS) transistors provide the building blocks for the four "AND-OR select" gate configurations, each consisting of two 2-input AND gates driving a single 2-input OR gate. Selection is accomplished by control bits K_A and K_B. All inputs are protected against static discharge damage.

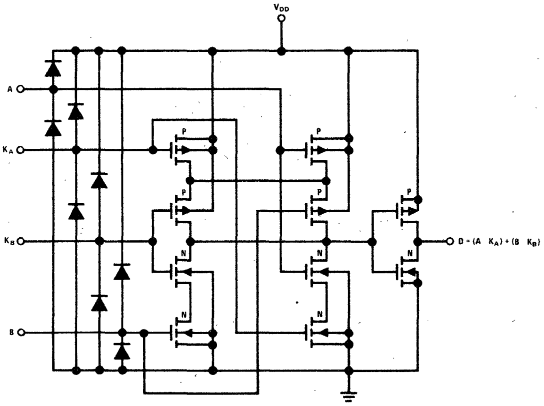
features

■ Wide Supply Voltage Range	3V to 15V
■ High Noise Immunity	$0.45 V_{CC}$ typ.
■ Medium-Speed Operation	$t_{PHL} = t_{PLH} =$ 50 ms typ at 15 pF

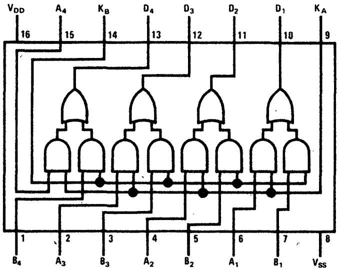
applications

- AND-OR Select Gating
- Shift-Right/Shift-Left Registers
- True/Complement Selection
- AND/OR/EXCLUSIVE-OR Selection

schematic and connection diagrams



Schematic diagram for 1 of 4 identical stages.



TOP VIEW

absolute maximum ratings

Voltage at any pin (Note 1)		V_{SS} −0.3V to V_{SS} +15.5V
Operating temperature range	CD4019M	−55°C to +125°C
	CD4019C	−40°C to +85°C
Storage temperature range		−65°C to +150°C
Package dissipation		500 mW
Lead temperature (soldering, 10 sec)		300°C
Operating V_{DD} range		V_{SS} +3V to V_{SS} +15V

Note 1: This device should not be connected to circuits with the power on because high transient voltage may cause permanent damage.

dc electrical characteristics

CHARACTERISTIC	SYMBOL	CONDITIONS			LIMITS																		UNITS
					CD4019M									CD4019C									
			V_O	V_{DD}	−55°C			25°C			125°C			−40°C			25°C			85°C			
			Volts	Volts	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Quiescent Device Current	I_L			5			5		0.03	5			300			50		0.1	50			700	μA
				10			10		0.05	10			600			100		0.2	100			1400	
Quiescent Device Dissipation/Package	P_D			5			25		0.15	25			1500			250		0.5	250			3500	μW
				10			100		0.5	100			6000			1000		2	1000			14000	
Output Voltage Low Level	V_{OL}			5			0.01		0	0.01			0.05			0.01		0	0.01			0.05	V
				10			0.01		0	0.01			0.05			0.01		0	0.01			0.05	
High Level	V_{OH}			5	4.99			4.99	5		4.95			4.99			4.99	5		4.95			V
				10	9.99			9.99	10		9.95			9.99			9.99	10		9.95			
Threshold Voltage N-Channel	$V_{TH}N$	I_D = 20 μA				1.7			1.5			1.3			1.7			1.5			1.3		V
P-Channel	$V_{TH}P$	I_D = −20 μA				−1.7			−1.5			−1.3			−1.7			−1.5			−1.3		V
Noise Immunity (All Inputs)	V_{NL}		0.95	5	1.5			1.5	2.25		1.4			1.5			1.5	2.25		1.4			V
			2.9	10	3			3	4.5		2.9			3			3	4.5		2.9			
	V_{NH}		3.6	5	1.4			1.5	2.25		1.5			1.4			1.5	2.25		1.5			V
			7.2	10	2.9			3	4.5		3			2.9			3	4.5		3			
Output Drive Current N-Channel	I_DN		0.5	5	0.6			0.45	1.5		0.30			0.37			0.30	1.0		0.23			mA
			0.5	10	0.9			0.75	2.5		0.55			0.8			0.65	1.5		0.6			
P-Channel	I_DP		4.5	5	−0.31			−0.25	−0.5		−0.175			−0.145			−0.12	−0.5		−0.095			mA
			9.5	10	−0.95			−0.7	−1.5		−0.5			−0.6			−0.5	−1.5		−0.4			
Input Current	I_I								10									10					pA

ac electrical characteristics

T_A = 25°C and C_L = 15 pF Typical Temperature Coefficient for all values of V_{DD} = 0.3%/°C

CHARACTERISTICS		SYMBOLS	CONDITIONS		LIMITS						UNITS
					CD4019M			CD4019C			
				V_{DD} (Volts)	Min	Typ	Max	Min	Typ	Max	
Propagation Delay Time:	High to Low Level	(t_{PHL}) =		5		100	225		100	300	ns
	Low to High Level	(t_{PLH})		10		50	100		50	125	
Transition Time	High to Low Level	(t_{THL}) =		5		100	200		100	275	ns
	Low to High Level	(t_{TLH})		10		40	65		40	80	
Input Capacitance		C_I	All A and B Inputs			5			5		pF
			K_A and K_B Inputs			12			12		

CD4020M/CD4020C

14-stage ripple-carry binary counter/divider

general description

The CD4020M/CD4020C is a 14-stage ripple-carry binary counter. Buffered outputs are externally available from stages 1, and 4 through 14. The counter is reset to its logical "0" state by a logical "1" on the reset input. The counter is advanced one count on the negative transition of each clock pulse.

features

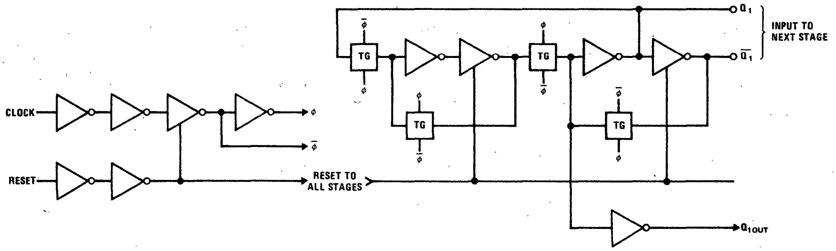
■ Wide supply voltage range	3.0V to 15V
■ High noise immunity	0.45 V_{CC} typ
■ Medium speed operation	10.0 MHz typ with V_{DD} = 10V
■ Low power	
■ Fully static operation	

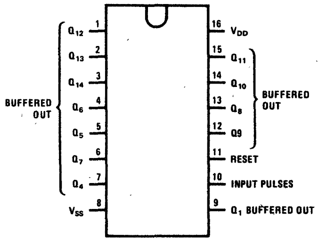
applications

- Automotive
- Instrumentation
- Medical electronics
- Alarm systems
- Industrial electronics
- Remote metering

logic and connection diagrams

Stage 1 of 14 Binary Stages





TOP VIEW

absolute maximum ratings

Voltage at Any Pin	V_{SS} – 0.3V to V_{SS} + 15.5
Operating Temperature Range	
CD4020M	–55°C to +125°C
CD4020C	–40°C to +85°C
Storage Temperature Range	–65°C to +150°C
Package Dissipation	500 mW
Operating V_{DD} Range	V_{SS} + 3.0V to V_{SS} + 15V
Lead Temperature (Soldering, 10 seconds)	300°C

dc electrical characteristics CD4020M

PARAMETER	CONDITIONS	LIMITS									UNITS
		–55°C			25°C			125°C			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Quiescent Device Current (I_L)	V_{DD} = 5.0V			15		0.5	15			900	μA
	V_{DD} = 10V			25		1.0	25			1500	μA
Quiescent Device Dissipation Package (P_D)	V_{DD} = 5.0V			75		2.5	75			4500	μW
	V_{DD} = 10V			250		10	250			15000	μW
Output Voltage Low Level (V_{OL})	V_{DD} = 5.0V			0.01		0	0.01			0.05	V
	V_{DD} = 10V			0.01		0	0.01			0.05	V
Output Voltage High Level (V_{OH})	V_{DD} = 5.0V	4.99			4.99	5.0		4.95			V
	V_{DD} = 10V	9.99			9.99	10		9.95			V
Noise Immunity (V_{NL}) (All Inputs)	V_{DD} = 5.0V, V_O = 0.8V	1.5			1.5	2.25		1.4			V
	V_{DD} = 10V, V_O = 1.0V	3.0			3.0	4.5		2.9			V
Noise Immunity (V_{NH}) (All Inputs)	V_{DD} = 5.0V, V_O = 4.2V	1.4			1.5	2.25		1.5			V
	V_{DD} = 10V, V_O = 9.0V	2.9			3.0	4.5		3.0			V
Output Drive Current N-Channel (I_DN)	V_{DD} = 5.0V, V_O = 0.5V	0.09			0.075	0.2		0.05			mA
	V_{DD} = 10V, V_O = 0.5V	0.185			0.15	0.4		0.105			mA
Output Drive Current P-Channel (I_DP)	V_{DD} = 5.0V, V_O = 4.5V	–0.11			–0.09	–0.25		–0.065			mA
	V_{DD} = 10V, V_O = 9.5V	–0.25			–0.20	–0.5		–0.14			mA
Input Current (I_I)	Any Input					10					pA

dc electrical characteristics CD4020C

PARAMETER	CONDITIONS	LIMITS									UNITS
		–40°C			25°C			85°C			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Quiescent Device Current (I_L)	V_{DD} = 5.0V			50		1.0	50			700	μA
	V_{DD} = 10V			100		2.0	100			1400	μA
Quiescent Device Dissipation Package (P_D)	V_{DD} = 5.0V			250		5.0	250			3500	μW
	V_{DD} = 10V			1000		20	1000			14000	μW
Output Voltage Low Level (V_{OL})	V_{DD} = 5.0V			0.01		0	0.01			0.05	V
	V_{DD} = 10V			0.01		0	0.01			0.05	V
Output Voltage High Level (V_{OH})	V_{DD} = 5.0V	4.99			4.99	5		4.95			V
	V_{DD} = 10V	9.99			9.99	10		9.95			V
Noise Immunity (V_{NL}) (All Inputs)	V_{DD} = 5.0V, V_O = 0.8V	1.5			1.5	2.25		1.4			V
	V_{DD} = 10V, V_O = 1.0V	3.0			3	4.5		2.9			V
Noise Immunity (V_{NH}) (All Inputs)	V_{DD} = 5.0V, V_O = 4.2V	1.4			1.5	2.25		1.5			V
	V_{DD} = 10V, V_O = 9.0V	2.9			3.0	4.5		3.0			V
Output Drive Current N-Channel (I_DN)	V_{DD} = 5.0V, V_O = 0.5V	0.085			0.07	0.33		0.06			mA
	V_{DD} = 10V, V_O = 0.5V	0.16			0.13	0.5		0.10			mA
Output Drive Current P-Channel (I_DP)	V_{DD} = 5.0V, V_O = 4.5V	–0.09			–0.06	–0.25		–0.05			mA
	V_{DD} = 10V, V_O = 9.5V	–0.18			–0.15	–0.5		–0.12			mA
Input Current (I_I)	Any Input					10					pA

ac electrical characteristics CD4020M $T_A = 25°C$, $C_L = 15$ pF, and input rise and fall times = 20 ns except t_{rCL}, t_{fCL}. Typical Temperature Coefficient (for all values of V_{DD}) = 0.3%/°C.

PARAMETER	CONDITIONS	LIMITS			UNITS
		MIN	TYP	MAX	
CLOCKED OPERATION					
Propagation Delay Time ($t_{PHL} = t_{PLH}$)	$V_{DD} = 5.0V$ $V_{DD} = 10V$		220 80	600 225	ns ns
Transition Time ($t_{THL} = t_{TLH}$)	$V_{DD} = 5.0V$ $V_{DD} = 10V$		120 60	600 300	ns ns
Minimum Clock Pulse Width ($t_{WL} = t_{WH}$)	$V_{DD} = 5.0V$ $V_{DD} = 10V$		150 50	335 125	ns ns
Clock Rise and Fall Time ($t_{rCL} = t_{fCL}$)	$V_{DD} = 5.0V$ $V_{DD} = 10V$			15 15	μs μs
Maximum Clock Frequency (f_{CL})	$V_{DD} = 5.0V$ $V_{DD} = 10V$	1.5 4.0	3.0 10		MHz MHz
Input Capacitance (C_I)	Any Input		5.0		pF
RESET OPERATION					
Propagation Delay Time ($t_{PHL(R)}$)	$V_{DD} = 5.0V$ $V_{DD} = 10V$		350 150	3000 775	ns ns
Minimum Reset Pulse Width ($t_{WH(R)}$)	$V_{DD} = 5.0V$ $V_{DD} = 10V$		350 150	2500 475	ns ns

ac electrical characteristics CD4020C $T_A = 25°C$, $C_L = 15$ pF, and input rise and fall times = 20 ns except t_{rCL}, t_{fCL}. Typical Temperature Coefficient (for all values of V_{DD}) = 0.3%/°C.

PARAMETER	CONDITIONS	LIMITS			UNITS
		MIN	TYP	MAX	
CLOCKED OPERATION					
Propagation Delay Time ($t_{PHL} = t_{PLH}$)	$V_{DD} = 5.0V$ $V_{DD} = 10V$		220 80	650 250	ns ns
Transition Time ($t_{THL} = t_{TLH}$)	$V_{DD} = 5.0V$ $V_{DD} = 10V$		120 60	650 350	ns ns
Minimum Clock Pulse Width ($t_{WL} = t_{WH}$)	$V_{DD} = 5.0V$ $V_{DD} = 10V$		150 50	500 165	ns ns
Clock Rise and Fall Time ($t_{rCL} = t_{fCL}$)	$V_{DD} = 5.0V$ $V_{DD} = 10V$			15 15	μs μs
Maximum Clock Frequency (f_{CL})	$V_{DD} = 5.0V$ $V_{DD} = 10V$	1.0 3.0	3.0 10		MHz MHz
Input Capacitance (C_I)	Any Input		5.0		pF
RESET OPERATION					
Propagation Delay Time ($t_{PHL(R)}$)	$V_{DD} = 5.0V$ $V_{DD} = 10V$		350 150	3500 900	ns ns
Minimum Reset Pulse Width ($t_{WH(R)}$)	$V_{DD} = 5.0V$ $V_{DD} = 10V$		350 150	3000 550	ns ns

CD4021M/CD4021C 8-stage static shift register

general description

The CD4021M/CD4021C is an 8-stage parallel input/serial output shift register. A parallel/serial control input enables individual "jam" inputs to each of 8-stages. Q outputs are available from the sixth, seventh and eighth stages.

When the parallel/serial control input is in the logical "0" state, data is serially shifted into the register synchronously with the positive transition of the clock. When the parallel/serial control is in the logical "1" state, data is "jammed" into each stage of the register asynchronously with the clock.

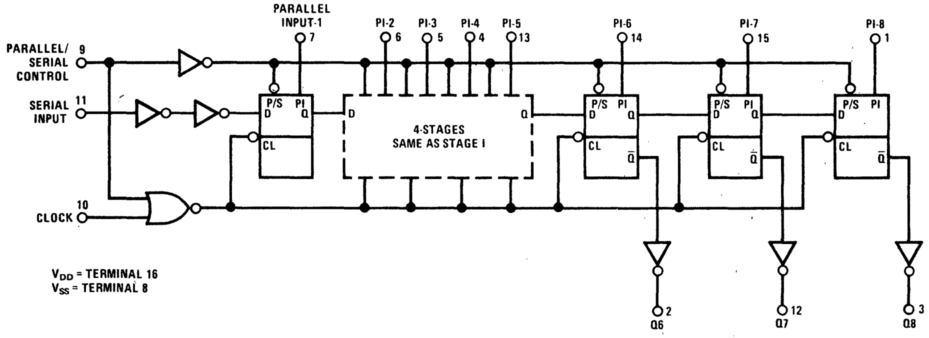
features

- Asynchronous parallel or synchronous serial operation.
- Wide supply voltage range 3.0V to 15V
- High noise immunity 0.45 V_{CC} typ
- Medium speed operation 5 MHz typ
  clock rate at $V_{DD} - V_{SS} = 10V$
- Fully static operation

applications

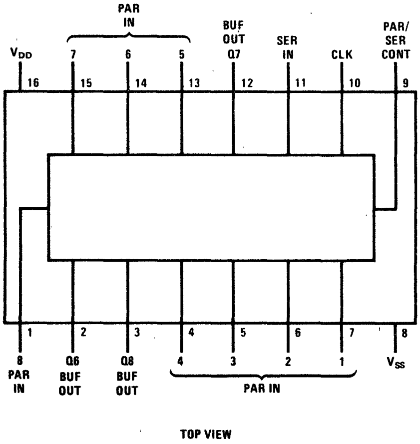
- Parallel to serial data conversion
- General purpose register

logic diagram



V_{DD} = TERMINAL 16
V_{SS} = TERMINAL 8

connection diagram



TOP VIEW

truth table

CL▲	SERIAL INPUT	PARALLEL/ SERIAL CONTROL	PI 1	PI n	Q1 (INTERNAL)	Q_n	
X	X	1	0	0	0	0	
X	X	1	0	1	0	1	
X	X	1	1	0	1	0	
X	X	1	1	1	1	1	
↑	0	0	X	X	0	Q_n 1	
↑	1	0	X	X	1	Q_n 1	
↓	X	0	X	X	Q1	Q_n	NO CHANGE

▲ = LEVEL CHANGE X = DON'T CARE CASE

absolute maximum ratings (Note 1)

Voltage at Any Pin	V_{SS} − 0.3V to V_{DD} + 0.3V
Operating Temperature Range	
CD4021M	−55°C to +125°C
CD4021C	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500 mW
Operating V_{DD} Range	V_{SS} + 3V to V_{SS} + 15V
Lead Temperature (Soldering, 10 seconds)	300°C

dc electrical characteristics CD4021M

PARAMETERS	CONDITIONS	LIMITS									UNITS
		−55°C			25°C			125°C			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Quiescent Device Current (I_L)	V_{DD} = 5V			5		0.5	5			300	µA
	V_{DD} = 10V			10		1	10			600	µA
Quiescent Device Dissipation Package (P_D)	V_{DD} = 5V			25		2.5	25			1,500	µW
	V_{DD} = 10V			100		10	100			6,000	µW
Output Voltage Low-Level (V_{OL})	V_{DD} = 5V			0.01		0	0.01			0.05	V
	V_{DD} = 10V			0.01		0	0.01			0.05	V
Output Voltage High-Level (V_{OH})	V_{DD} = 5V	4.99			4.99	5		4.95			V
	V_{DD} = 10V	9.99			9.99	10		9.95			V
Noise Immunity (All Inputs) (V_{NL})	V_O = 0.8V, V_{DD} = 5V	1.5			1.5	2.25		1.4			V
	V_O = 1V, V_{DD} = 10V	3			3	4.5		2.9			V
Noise Immunity (All Inputs) (V_{NH})	V_O = 4.2V, V_{DD} = 5V	1.4			1.5	2.25		1.5			V
	V_O = 9V, V_{DD} = 10V	2.9			3	4.5		3			V
Output Drive Current N-Channel (I_DN)	V_O = 0.5V, V_{DD} = 5V	0.15			0.12	0.3		0.085			mA
	V_O = 0.5V, V_{DD} = 10V	0.31			0.25	0.5		0.175			mA
Output Drive Current P-Channel (I_DP)	V_O = 4.5V, V_{DD} = 5V	−0.1			−0.08	−0.16		−0.055			mA
	V_O = 9.5V, V_{DD} = 10V	−0.25			−0.20	−0.44		−0.14			mA
Input Current (I_I)						10					pA

dc electrical characteristics CD4021C

PARAMETERS	CONDITIONS	LIMITS									UNITS
		−40°C			25°C			85°C			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Quiescent Device Current (I_L)	V_{DD} = 5V			50		0.5	50			700	µA
	V_{DD} = 10V			100		1	100			1,400	µA
Quiescent Device Dissipation Package (P_D)	V_{DD} = 5V			250		2.5	250			3,500	µW
	V_{DD} = 10V			1,000		10	1,000			14,000	µW
Output Voltage Low-Level (V_{OL})	V_{DD} = 5V			0.01		0	0.01			0.05	V
	V_{DD} = 10V			0.01		0	0.01			0.05	V
Output Voltage High-Level (V_{OH})	V_{DD} = 5V	4.99			4.99	5		4.95			V
	V_{DD} = 10V	9.99			9.99	10		9.95			V
Noise Immunity (All Inputs) (V_{NL})	V_O = 0.8V, V_{DD} = 5V	1.5			1.5	2.25		1.4			V
	V_O = 1V, V_{DD} = 10V	3			3	4.5		2.9			V
Noise Immunity (All Inputs) (V_{NH})	V_O = 4.2V, V_{DD} = 5V	1.4			1.5	2.25		1.5			V
	V_O = 9V, V_{DD} = 10V	2.9			3	4.5		3			V
Output Drive Current N-Channel (I_DN)	V_O = 0.5V, V_{DD} = 5V	0.072			0.06	0.3		0.05			mA
	V_O = 0.5V, V_{DD} = 10V	0.12			0.1	0.5		0.08			mA
Output Drive Current P-Channel (I_DP)	V_O = 4.5V, V_{DD} = 5V	−0.06			−0.05	−0.16		−0.04			mA
	V_O = 9.5V, V_{DD} = 10V	−0.12			−0.1	−0.44		−0.08			mA
Input Current (I_I)						10					pA

ac electrical characteristics CD4021M

PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNITS
Propagation Delay Time (t_{PHL}, t_{PLH})	V_{DD} = 5V V_{DD} = 10V		300 100	750 225	ns ns
Transition Time (t_{THL}, t_{TLH})	V_{DD} = 5V V_{DD} = 10V		150 75	300 125	ns ns
Minimum Clock Pulse Width (t_{WL}, t_{WH})	V_{DD} = 5V V_{DD} = 10V		200 100	500 175	ns ns
Minimum High Level Parallel/Serial Control Pulse Width ($t_{WH(P/S)}$)	V_{DD} = 5V V_{DD} = 10V		200 100	500 175	ns ns
Clock Rise Time (t_{rCL}) or Clock Fall Time (t_{fCL})	V_{DD} = 5V V_{DD} = 10V			15 15	μs μs
Set-up Time	V_{DD} = 5V V_{DD} = 10V		100 50	350 80	ns ns
Maximum Clock Frequency (f_{CL})	V_{DD} = 5V V_{DD} = 10V	1 3	2.5 5		MHz MHz
Input Capacitance (C_I) (Note 2)	Any Input		5		pF

ac electrical characteristics CD4021C

PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNITS
Propagation Delay Time (t_{PHL}, t_{PLH})	V_{DD} = 5V V_{DD} = 10V		300 100	1,000 300	ns ns
Transition Time (t_{THL}, t_{TLH})	V_{DD} = 5V V_{DD} = 10V		150 75	400 150	ns ns
Minimum Clock Pulse Width (t_{WL}, t_{WH})	V_{DD} = 5V V_{DD} = 10V		200 100	830 200	ns ns
Minimum High Level Parallel/Serial Control Pulse Width ($t_{WH(P/S)}$)	V_{DD} = 5V V_{DD} = 10V		200 100	830 200	ns ns
Clock Rise Time (t_{rCL}) or Clock Fall Time (t_{fCL})	V_{DD} = 5V V_{DD} = 10V			15 15	μs μs
Set-up Time	V_{DD} = 5V V_{DD} = 10V		100 50	500 100	ns ns
Maximum Clock Frequency (f_{CL})	V_{DD} = 5V V_{DD} = 10V	0.6 2.5	2.5 5		MHz MHz
Input Capacitance (C_I) (Note 2)	Any Input		5		pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

CD4022M/CD4022C divide-by-8 counter/divider with 8 decoded outputs

general description

The CD4022M/CD4022C is a 4-stage divide-by-8 Johnson counter with 8 decoded outputs and a carry-out bit. The counter is cleared to its zero count by a logical "1" on its reset line. The counter is advanced on the positive edge of the clock signal when the clock enable signal is in the logical "0" state.

The configuration of the CD4022M/CD4022C permits medium speed operation and assures an error free counting sequence. The 8 decoded outputs are normally in the logical "0" state and go to the logical "1" state only at their respective time slot. Each decoded output remains high for 1 full clock cycle. The carry-out signal completes a full cycle for every 8 clock input cycles and is used as a ripple carry signal to any succeeding stages.

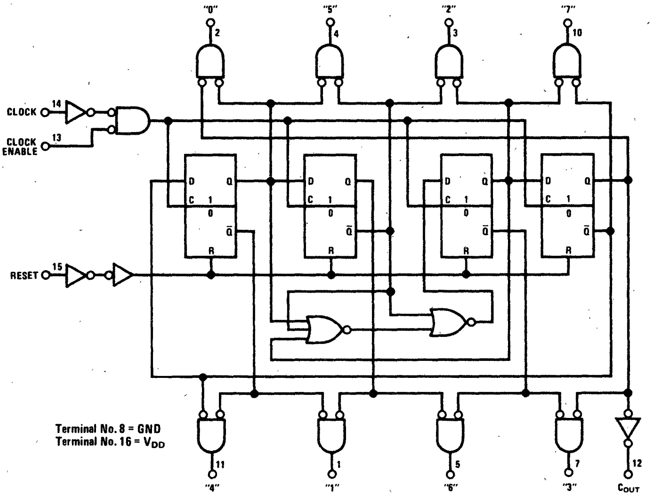
features

■ Wide supply voltage range	3.0V to 15V
■ High noise immunity	0.45 V_{DD} typ
■ Medium speed operation	5.0 MHz typ with 10V V_{DD}
■ Low power	10μW typ
■ Fully static operation	

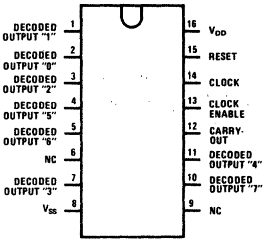
applications

- Automotive
- Instrumentation
- Medical electronics
- Alarm systems
- Industrial electronics
- Remote metering

logic and connection diagrams



Terminal No. 8 = GND
Terminal No. 16 = V_{DD}



TOP VIEW

absolute maximum ratings

Voltage at Any Pin	V_{SS} – 0.3V to V_{SS} + 15.5V
Operating Temperature Range	
CD4022M	–55°C to +125°C
CD4022C	–40°C to +85°C
Stoarge Temperature Range	–65°C to +150°C
Package Dissipation	500 mW
Operating V_{DD} Range	V_{SS} + 3.0V to V_{SS} + 15V
Lead Temperature (Soldering, 10 seconds)	300°C

dc electrical characteristics CD4022M

PARAMETER	CONDITIONS	LIMITS									UNITS
		-55°C			25°C			125°C			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Quiescent Device Current (I_L)	V_{DD} = 5.0V			5.0		0.3	5.0			300	μA
	V_{DD} = 10V			10		0.5	10			600	μA
Quiescent Device Dissipation/Package (P_D)	V_{DD} = 5.0V			25		1.5	25			1,500	μW
	V_{DD} = 10V			100		5.0	100			6,000	μW
Output Voltage Low Level (V_{OL})	V_{DD} = 5.0V			0.01		0	0.01			0.05	V
	V_{DD} = 10V			0.01		0	0.01			0.05	V
Output Voltage High Level (V_{OH})	V_{DD} = 5.0V	4.99			4.99	5.0		4.95			V
	V_{DD} = 10V	9.99			9.99	10		9.95			V
Noise Immunity (V_{NL}) (All Inputs)	V_{DD} = 5.0V, V_O = 0.8V	1.5			1.5	2.25		1.4			V
	V_{DD} = 10V, V_O = 1.0V	3.0			3.0	4.5		2.9			V
Noise Immunity (V_{NH}) (All Inputs)	V_{DD} = 5.0V, V_O = 4.2V	1.4			1.5	2.25		1.5			V
	V_{DD} = 10V, V_O = 9.0V	2.9			3.0	4.5		3.0			V
Output Drive Current N-Channel (I_DN)	Decoded Outputs										
	V_{DD} = 5.0V, V_O = 0.5V	0.062			0.05	0.15		0.035			mA
	V_{DD} = 10V, V_O = 0.5V	0.12			0.1	0.3		0.07			mA
Output Drive Current N-Channel (I_DN)	Carry Outputs										
	V_{DD} = 5.0V, V_O = 0.5V	0.185			0.15	0.5		0.105			mA
	V_{DD} = 10V, V_O = 0.5V	0.375			0.3	1.0		0.21			mA
Output Drive Current P-Channel (I_DP)	Decoded Outputs										
	V_{DD} = 5.0V, V_O = 4.5V	–0.038			–0.03	–0.075		–0.021			mA
	V_{DD} = 10V, V_O = 9.5V	–0.062			–0.05	–0.15		–0.035			mA
Output Drive Current P-Channel (I_DP)	Carry Outputs										
	V_{DD} = 5.0V, V_O = 4.5V	–0.185			–0.15	–0.4		–0.105			mA
	V_{DD} = 10V, V_O = 9.5V	–0.375			–0.3	–0.8		–0.21			mA
Input Current (I_I)						10					pA

dc electrical characteristics CD4022C

PARAMETER	CONDITIONS	LIMITS									UNITS
		–40°C			25°C			85°C			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Quiescent Device Current (I_L)	V_{DD} = 5.0V			50		0.5	50			700	μA
	V_{DD} = 10V			100		1.0	100			1,400	μA
Quiescent Device Dissipation/Package (P_D)	V_{DD} = 5.0V			350		2.5	250			3,500	μW
	V_{DD} = 10V			1,000		10	1,000			14,000	μW
Output Voltage Low Level (V_{OL})	V_{DD} = 5.0V			0.01		0	0.01			0.05	V
	V_{DD} = 10V			0.01		0	0.01			0.05	V
Output Voltage High Level (V_{OH})	V_{DD} = 5.0V	4.99			4.99	5.0		4.95			V
	V_{DD} = 10V	9.99			9.99	10		9.95			V
Noise Immunity (V_{NL}) (All Inputs)	V_{DD} = 5.0V, V_O = 0.8V	1.5			1.5	2.25		1.4			V
	V_{DD} = 10V, V_O = 1.0V	3.0			3.0	4.5		2.9			V
Noise Immunity (V_{NH}) (All Inputs)	V_{DD} = 5.0V, V_O = 4.2V	1.4			1.5	2.25		1.5			V
	V_{DD} = 10V, V_O = 9.0V	2.9			3.0	4.5		3.0			V
Output Drive Current N-Channel (I_DN)	Decoded Outputs										
	V_{DD} = 5.0V, V_O = 0.5V	0.03			0.025	0.15		0.02			mA
	V_{DD} = 10V, V_O = 0.5V	0.06			0.05	0.3		0.04			mA
Output Drive Current N-Channel (I_DN)	Carry Outputs										
	V_{DD} = 5.0V, V_O = 0.5V	0.095			0.08	0.5		0.065			mA
	V_{DD} = 10V, V_O = 0.5V	0.155			0.13	1.0		0.105			mA
Output Drive Current P-Channel (I_DP)	Decoded Outputs										
	V_{DD} = 5.0V, V_O = 4.5V	–0.018			–0.015	–0.075		–0.012			mA
	V_{DD} = 10V, V_O = 9.5V	–0.06			–0.05	–0.15		–0.04			mA
Output Drive Current P-Channel (I_DP)	Carry Outputs										
	V_{DD} = 5.0V, V_O = 4.5V	–0.095			–0.08	–0.4		–0.065			mA
	V_{DD} = 10V, V_O = 9.5V	–0.155			–0.13	–0.8		–0.105			mA
Input Current (I_I)						10					pA

ac electrical characteristics CD4022M

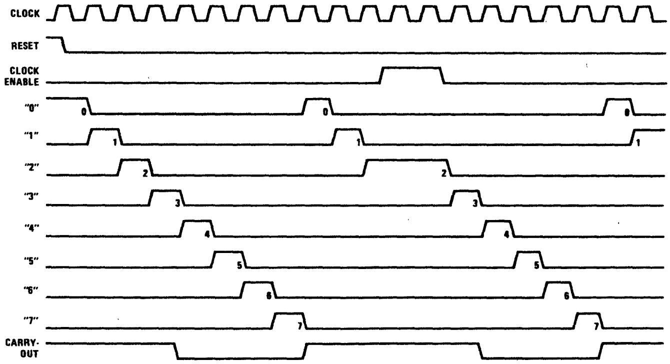
T_A = 25°C and C_L = 15 pF. Typical Temperature Coefficient for all values of V_{DD} = 0.3%/°C.

PARAMETER	CONDITIONS	LIMITS			UNITS
		MIN	TYP	MAX	
CLOCKED OPERATION					
Propagation Delay Time Carry-Out Line (t_{PHL} = t_{PLH})	V_{DD} = 5.0V V_{DD} = 10V		325 125	1,000 250	ns ns
Propagation Delay Time Decode-Out Lines (t_{PHL} = t_{PLH})	V_{DD} = 5.0V V_{DD} = 10V		400 200	1,200 400	ns ns
Transition Time Carry-Out Line (t_{THL} = t_{TLH})	V_{DD} = 5.0V V_{DD} = 10V		85 50	300 100	ns ns
Transition Time Decode-Out Lines (t_{THL} = t_{TLH})	V_{DD} = 5.0V V_{DD} = 10V		300 125	900 250	ns ns
Minimum Clock Pulse Width (t_{WL} = t_{WH})	V_{DD} = 5.0V		250	500	ns
Minimum Clock Pulse Width (t_{WL} = t_{WH})	V_{DD} = 10V		85	170	ns
Clock Rise and Fall Time (t_{rCL})	V_{DD} = 5.0V			15	μs
Clock Rise and Fall Time (t_{fCL})	V_{DD} = 10V			15	μs
Clock Enable Set-Up Time	V_{DD} = 5.0V V_{DD} = 10V	350 150	175 75		ns ns
Maximum Clock Frequency (f_{CL})	V_{DD} = 5.0V V_{DD} = 10V	1.0 3.0	2.5 5.0		MHz MHz
Input Capacitance (C_I)	Any Input		5.0		pF
RESET OPERATION					
Propagation Delay Time Carry-Out Line (t_{PLH})	V_{DD} = 5.0V V_{DD} = 10V		300 125	900 250	ns ns
Propagation Delay Time Decode-Out Line (t_{PLH})	V_{DD} = 5.0V V_{DD} = 10V		500 200	1,250 400	ns ns
Minimum Reset Pulse Width (t_{WL})	V_{DD} = 5.0V		150	300	ns
Minimum Reset Pulse Width (t_{WH})	V_{DD} = 10V		75	150	ns

ac electrical characteristics CD4022C

PARAMETER	CONDITIONS	LIMITS			UNITS
		MIN	TYP	MAX	
CLOCKED OPERATION					
Propagation Delay Time Carry-Out Line (t_{PHL} = t_{PLH})	V_{DD} = 5.0V V_{DD} = 10V		325 125	1,300 500	ns ns
Propagation Delay Time Decode-Out Line (t_{PHL} = t_{PLH})	V_{DD} = 5.0V V_{DD} = 10V		400 200	1,600 800	ns ns
Transition Time Carry-Out Line (t_{THL} = t_{TLH})	V_{DD} = 5.0V V_{DD} = 10V		85 50	340 200	ns ns
Transition Time Decode-Out Lines (t_{THL} = t_{TLH})	V_{DD} = 5.0V V_{DD} = 10V		300 125	1,200 500	ns ns
Minimum Clock Pulse Width (t_{WL} = t_{WH})	V_{DD} = 5.0V		250	830	ns
Minimum Clock Pulse Width (t_{WL} = t_{WH})	V_{DD} = 10V		85	250	ns
Clock Rise and Fall Time (t_{rCL})	V_{DD} = 5.0V			15	μs
Clock Rise and Fall Time (t_{fCL})	V_{DD} = 10V			15	μs
Clock Enable Set-Up Time	V_{DD} = 5.0V V_{DD} = 10V	700 300	175 75		ns ns
Maximum Clock Frequency (f_{CL})	V_{DD} = 5.0V V_{DD} = 10V	0.6 2.0	2.5 5.0		MHz MHz
Input Capacitance (C_I)	Any Input		5.0		pF
RESET OPERATION					
Propagation Delay Time Carry-Out Line (t_{PHL})	V_{DD} = 5.0V V_{DD} = 10V		300 125	1,200 500	ns ns
Propagation Delay Time Decode-Out Line (t_{PLH})	V_{DD} = 5.0V V_{DD} = 10V		500 200	2,500 800	ns ns
Minimum Reset Pulse Width (t_{WL})	V_{DD} = 5.0V		150	600	ns
Minimum Reset Pulse Width (t_{WH})	V_{DD} = 10V		75	300	ns

timing diagram



CD4024M/CD4024C 7-stage ripple-carry binary counter/divider

general description

The CD4024M/CD4024C is a 7-stage ripple-carry binary counter. Buffered outputs are externally available from stages 1 through 7. The counter is reset to its logical "0" state by a logical "1" on the reset input. The counter is advanced one count on the negative transition of each clock pulse.

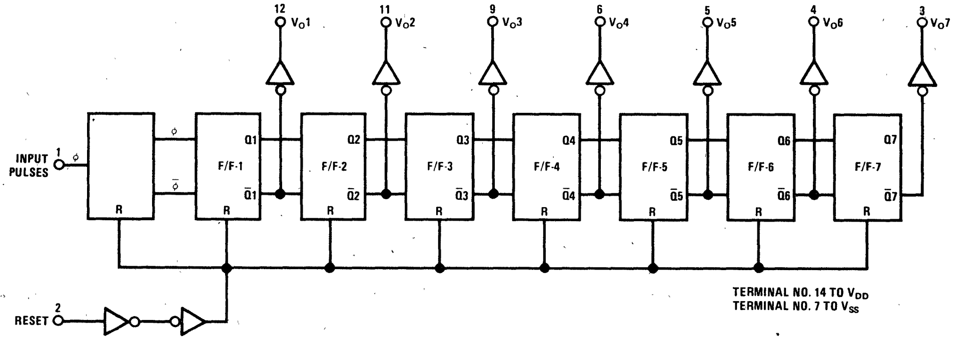
features

- Wide supply voltage range 3.0V to 15V
- High noise immunity 0.45 V_{CC} typ
- High speed 12 MHz (typ) input pulse rate $V_{DD}-V_{SS}$ = 10V
- Fully static operation
- Low power

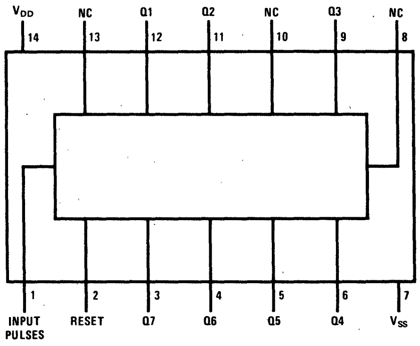
applications

- Frequency dividing circuits
- Time-delay circuits
- Counter control

logic diagram



connection diagram



TOP VIEW

absolute maximum ratings (Note 1)

Voltage at Any Pin	V_{SS} − 0.3V to V_{SS} + 15.5
Operating Temperature Range	
CD4024M	−55°C to +125°C
CD4024C	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500 mW
Operating V_{DD} Range	V_{SS} + 3.0V to V_{SS} + 15V
Leading Temperature (Soldering, 10 seconds)	300°C

dc electrical characteristics CD4024M

PARAMETERS	CONDITIONS	LIMITS									UNITS
		−55°C			25°C			125°C			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Quiescent Device Current (I_L)	V_{DD} = 5V			5		0.3	5			300	μA
	V_{DD} = 10V			10		0.5	10			600	μA
Quiescent Device Dissipation Package (P_D)	V_{DD} = 5V			25		1.5	25			1,500	μW
	V_{DD} = 10V			100		5	100			6,000	μW
Output Voltage Low-Level (V_{OL})	V_{DD} = 5V			0.01		0	0.01			0.05	V
	V_{DD} = 10V			0.01		0	0.01			0.05	V
Output Voltage High-Level (V_{OH})	V_{DD} = 5V	4.99			4.99	5		4.95			V
	V_{DD} = 10V	9.99			9.99	10		9.95			V
Noise Immunity (All Inputs) (V_{NL})	V_O = 0.8V, V_{DD} = 5V	1.5			1.5	2.25		1.4			V
	V_O = 1V, V_{DD} = 10V	3			3	4.5		2.9			V
Noise Immunity (All Inputs) (V_{NH})	V_O = 4.2V, V_{DD} = 5V	1.4			1.5	2.25		1.5			V
	V_O = 9V, V_{DD} = 10V	2.9			3	4.5		3			V
Output Drive Current N-Channel (I_DN)	V_{DD} = 5V	0.31			0.25	0.5		0.175			mA
	V_{DD} = 10V	0.62			0.5	1		0.35			mA
Output Device Current P-Channel (I_DP)	V_{DD} = 5V	−0.19			−0.15	−0.3		−0.105			mA
	V_{DD} = 10V	−0.45			−0.35	−0.7		−0.25			mA
Input Current (I_I)						10					pA

dc electrical characteristics CD4024C

PARAMETERS	CONDITIONS	LIMITS									UNITS
		−40°C			25°C			85°C			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Quiescent Device Current (I_L)	V_{DD} = 5V			50		0.5	50			700	μA
	V_{DD} = 10V			100		1	100			1,400	μA
Quiescent Device Dissipation Package (P_D)	V_{DD} = 5V			250		2.5	250			3,500	μA
	V_{DD} = 10V			1,000		10	1,000			14,000	μA
Output Voltage Low-Level (V_{OL})	V_{DD} = 5V			0.01		0	0.01			0.05	V
	V_{DD} = 10V			0.01		0	0.01			0.05	V
Output Voltage High-Level (V_{OH})	V_{DD} = 5V	4.99			4.99	5		4.95			V
	V_{DD} = 10V	9.99			9.99	10		9.95			V
Noise Immunity (All Inputs) (V_{NL})	V_O = 0.8V, V_{DD} = 5V	1.5			1.5	2.25		1.4			V
	V_O = 1V, V_{DD} = 10V	3			3	4.5		2.9			V
Noise Immunity (All Inputs) (V_{NH})	V_O = 4.2V, V_{DD} = 5V	1.4			1.5	2.25		1.5			V
	V_O = 9V, V_{DD} = 10V	2.9			3	4.5		3			V
Output Drive Current N-Channel (I_DN)	V_{DD} = 5V	0.15			0.12	0.5		0.95			mA
	V_{DD} = 10V	0.31			0.25	1		0.2			mA
Output Drive Current P-Channel (I_DP)	V_{DD} = 5V	−0.145			−0.12	−0.3		−0.95			mA
	V_{DD} = 10V	−0.31			−0.25	−0.7		−0.2			mA
Input Current (I_I)						10					pA

ac electrical characteristics CD4024M

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
ϕ INPUT OPERATION					
Propagation Delay Time (t_{PHL}, t_{PLH}) (Note 3)	V_{DD} = 5V		150	350	ns
	V_{DD} = 10V		70	125	ns
Transition Time (t_{THL}, t_{TLH})	V_{DD} = 5V		75	225	ns
	V_{DD} = 10V		40	125	ns
Minimum Input-Pulse Width (t_{WL}, t_{WH})	V_{DD} = 5V		75	330	ns
	V_{DD} = 10V		40	125	ns
Input Pulse Time ($t_{r\phi}$, $t_{f\phi}$)	V_{DD} = 5V			15	ns
	V_{DD} = 10V			10	ns
Maximum Input Pulse Frequency ($f\phi$)	V_{DD} = 5V	1.5	5		MHz
	V_{DD} = 10V	4	12		MHz
Input Capacitance (C_I) (Note 2)	Any Input		5		pF
RESET OPERATION					
Propagation Delay Time ($t_{PHL(R)}$)	V_{DD} = 5V		200	700	ns
	V_{DD} = 10V		100	350	ns
Minimum Pulse Reset Width ($t_{WH(R)}$)	V_{DD} = 5V		200	500	ns
	V_{DD} = 10V		100	300	ns

ac electrical characteristics CD4024C

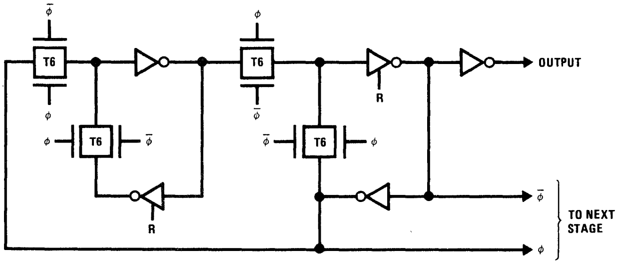
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
ϕ INPUT OPERATION					
Propagation Delay Time (t_{PHL}, t_{PLH}) (Note 3)	V_{DD} = 5V		150	400	ns
	V_{DD} = 10V		70	150	ns
Transition Time (t_{THL}, t_{TLH})	V_{DD} = 5V		75	250	ns
	V_{DD} = 10V		40	150	ns
Minimum Input-Pulse Width (t_{WL}, t_{WH})	V_{DD} = 5V		75	500	ns
	V_{DD} = 10V		40	165	ns
Input Pulse Time ($t_{r\phi}$, $t_{f\phi}$)	V_{DD} = 5V			15	ns
	V_{DD} = 10V			10	ns
Maximum Input Pulse Frequency ($f\phi$)	V_{DD} = 5V	1	5		MHz
	V_{DD} = 10V	3	12		MHz
Input Capacitance (C_I) (Note 2)	Any Input		5		pF
RESET OPERATION					
Propagation Delay Time ($t_{PHL(R)}$)	V_{DD} = 5V		200	800	ns
	V_{DD} = 10V		100	400	ns
Minimum Pulse Reset Width ($t_{WH(R)}$)	V_{DD} = 5V		200	600	ns
	V_{DD} = 10V		100	350	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

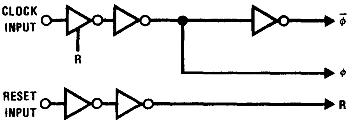
Note 2: Capacitance is guaranteed by periodic testing.

Note 3: To Q1 output.

schematic diagram



Flip-flop logic (1 of 7 identical stages).



Input Logic

CD4025M/CD4025C triple 3-input NOR gate

general description

These NOR gates are monolithic complementary MOS (CMOS) integrated circuits. The N and P-channel enhancement mode transistors provide a symmetrical circuit with output swings essentially equal to the supply voltage. This results in high noise immunity over a wide supply voltage range. No dc power other than that caused by leakage current is consumed during static conditions. All inputs are protected against static discharge and latching conditions.

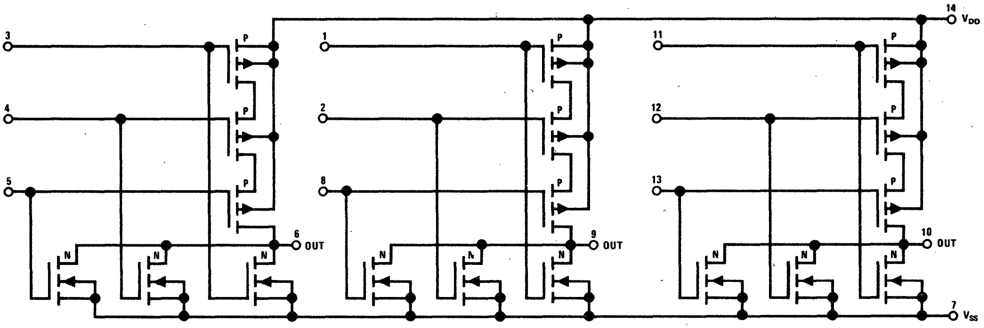
features

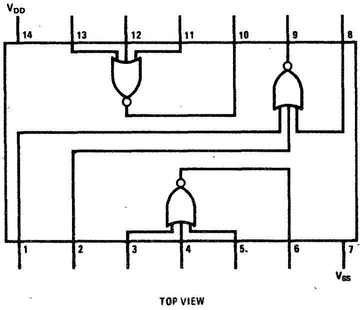
■ Wide supply voltage range	3.0V to 15V
■ Low power	10 nW (typ.)
■ High noise immunity	0.45 V_{DD} (typ.)
■ Medium speed operation	$t_{PHL} = t_{PLH} = 25$ ns (typ.) at $C_L = 15$ pF

applications

- Automotive
- Data terminals
- Instrumentation
- Medical electronics
- Industrial controls
- Remote metering
- Computers

logic and connection diagrams





absolute maximum ratings

Voltage at Any Pin (Note 1)	V_{SS} – 0.3V to V_{SS} + 15.5V
Operating Temperature Range	
CD4025M	–55°C to +125°C
CD4025C	–40°C to +85°C
Storage Temperature Range	–65°C to +150°C
Package Dissipation	500 mW
Operating V_{DD} Range	V_{SS} + 3.0V to V_{SS} + 15V
Lead Temperature (Soldering, 10 seconds)	300°C

dc electrical characteristics CD4025M

PARAMETER	CONDITIONS	LIMITS									UNITS
		–55°C			25°C			125°C			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Quiescent Device Current (I_L)	V_{DD} = 5.0V			0.05		0.001	0.05			3.0	µA
	V_{DD} = 10V			0.1		0.001	0.1			6.0	µA
Quiescent Device Dissipation Package (P_D)	V_{DD} = 5.0V			0.25		0.005	0.25			15	µW
	V_{DD} = 10V			1.0		0.01	1.0			60	µW
Output Voltage Low Level (V_{OL})	$V_I = V_{SS}$, I_O = 0A, V_{DD} = 5.0V			0.01		0	0.01			0.05	V
	$V_I = V_{SS}$, I_O = 0A, V_{DD} = 10V			0.01		0	0.01			0.05	V
Output Voltage High Level (V_{OH})	$V_I = V_{DD}$, I_O = 0A, V_{DD} = 5.0V	4.99			4.99	5.0		4.95			V
	$V_I = V_{DD}$, I_O = 0A, V_{DD} = 10V	9.99			9.99	10		9.95			V
Noise Immunity (V_{NL})(All Inputs)	I_O = 0, V_O = 4.3V, V_{DD} = 5.0V	1.5			1.5	2.25		1.4			V
	I_O = 0, V_O = 9.3V, V_{DD} = 10V	3.0			3.0	4.5		2.9			V
Noise Immunity (V_{NH})(All Inputs)	I_O = 0, V_O = 0.7V, V_{DD} = 5.0V	1.4			1.5	2.25		1.5			V
	I_O = 0, V_O = 0.7V, V_{DD} = 10V	2.9			3.0	4.5		3.0			V
Output Drive Current N-Channel (I_DN)	$V_I = V_{DD}$, V_O = 0.4, V_{DD} = 5.0V	0.5			0.40			0.28			mA
	$V_I = V_{DD}$, V_O = 0.5, V_{DD} = 10V	1.1			0.9			0.65			mA
Output Drive Current P-Channel (I_DP)	$V_I = V_{SS}$, $V_O \neq$ 2.5V, V_{DD} = 5.0V	–0.62			–0.5			–0.35			mA
	$V_I = V_{SS}$, V_O = 9.5V, V_{DD} = 10V	–0.62			–0.5			–0.35			mA
Input Current (I_I)						10					pA

dc electrical characteristics CD4025C

PARAMETER	CONDITIONS	LIMITS									UNITS
		–40°C			25°C			85°C			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Quiescent Device Current (I_L)	V_{DD} = 5.0V			0.5		0.005	0.5			15	µA
	V_{DD} = 10V			1.0		0.005	1.0			30	µA
Quiescent Device Dissipation Package (P_D)	V_{DD} = 5.0V			0.25		0.025	2.5			75	µA
	V_{DD} = 10V			10		0.05	10			300	µW
Output Voltage Low Level (V_{OL})	$V_I = V_{SS}$, I_O = 0A, V_{DD} = 5.0V			0.01		0	0.01			0.05	V
	$V_I = V_{SS}$, I_O = 0A, V_{DD} = 10V			0.01		0	0.01			0.05	V
Output Voltage High Level (V_{OH})	$V_I = V_{DD}$, I_O = 0A, V_{DD} = 5.0V	4.99			4.99	5.0		4.95			V
	$V_I = V_{DD}$, I_O = 0A, V_{DD} = 10V	9.99			9.99	10		9.95			V
Noise Immunity (V_{NL})(All Inputs)	I_O = 0, V_O = 4.3V, V_{DD} = 5.0V	1.5			1.5	2.25		1.4			V
	I_O = 0, V_O = 9.3V, V_{DD} = 10V	3.0			3.0	4.5		2.9			V
Noise Immunity (V_{NH})(All Inputs)	I_O = 0, V_O = 0.7V, V_{DD} = 5.0V	1.4			1.5	2.25		1.5			V
	I_O = 0, V_O = 0.7V, V_{DD} = 10V	2.9			3.0	4.5		3.0			V
Output Drive Current N-Channel (I_DN)	$V_I = V_{DD}$, V_O = 0.4V, V_{DD} = 5.0V	0.35			0.3	1.0		0.24			mA
	$V_I = V_{DD}$, V_O = 0.5V, V_{DD} = 10V	0.72			0.6	2.5		0.48			mA
Output Drive Current P-Channel (I_DP)	$V_I = V_{SS}$, $V_O \neq$ 2.5V, V_{DD} = 5.0V	–0.35			–0.3	–2.0		–0.24			mA
	$V_I = V_{SS}$, V_O = 9.5V, V_{DD} = 10V	–0.3			–0.25	–1.0		–0.2			mA
Input Current (I_I)						10					pA

Note 1: This device should not be connected to circuits with the power on because high transient voltages may cause permanent damage.

ac electrical characteristics CD4025M

$T_A = 25°C$ and $C_L = 15$ pF. Typical temperature coefficient for all values of $V_{DD} = 0.3\%/°C$.

PARAMETER	CONDITIONS	LIMITS			UNITS
		MIN	TYP	MAX	
Propagation Delay Time High to Low Level (t_{PHL})	$V_{DD} = 5.0V$		35	50	ns
	$V_{DD} = 10V$		25	40	ns
Propagation Delay Time Low to High Level (t_{PLH})	$V_{DD} = 5.0V$		35	70	ns
	$V_{DD} = 10V$		25	45	ns
Transition Time High to Low Level (t_{THL})	$V_{DD} = 5.0V$		65	125	ns
	$V_{DD} = 10V$		35	70	ns
Transition Time Low to High Level (t_{TLH})	$V_{DD} = 5.0V$		65	175	ns
	$V_{DD} = 10V$		35	75	ns
Input Capacitance (C_I)	Any Input		5.0		pF

ac electrical characteristics CD4025C

$T_A = 25°C$ and $C_L = 15$ pF. Typical temperature coefficient for all values of $V_{DD} = 0.3\%/°C$.

PARAMETER	CONDITIONS	LIMITS			UNITS
		MIN	TYP	MAX	
Propagation Delay Time High to Low Level (t_{PHL})	$V_{DD} = 5.0V$		35	80	ns
	$V_{DD} = 10V$		25	55	ns
Propagation Delay Time Low to High Level (t_{PLH})	$V_{DD} = 5.0V$		35	120	ns
	$V_{DD} = 10V$		25	65	ns
Transition Time High to Low Level (t_{THL})	$V_{DD} = 5.0V$		65	200	ns
	$V_{DD} = 10V$		35	115	ns
Transition Time Low to High Level (t_{TLH})	$V_{DD} = 5.0V$		65	300	ns
	$V_{DD} = 10V$		35	125	ns
Input Capacitance (C_I)	Any Input		5.0		pF

CD4027M/CD4027C dual JK master/slave flip-flop with set and reset

general description

These dual JK flip-flops are monolithic Complementary MOS (CMOS) integrated circuits constructed with N and P-channel enhancement mode transistors. Each flip-flop has independent J, K, set, reset and clock inputs and buffered Q and $\overline{Q}$ outputs. These flip-flops are edge sensitive to the clock input and change state on the positive going transition of the clock pulses. Set or reset is independent of the clock and is accomplished by a high level on the respective input.

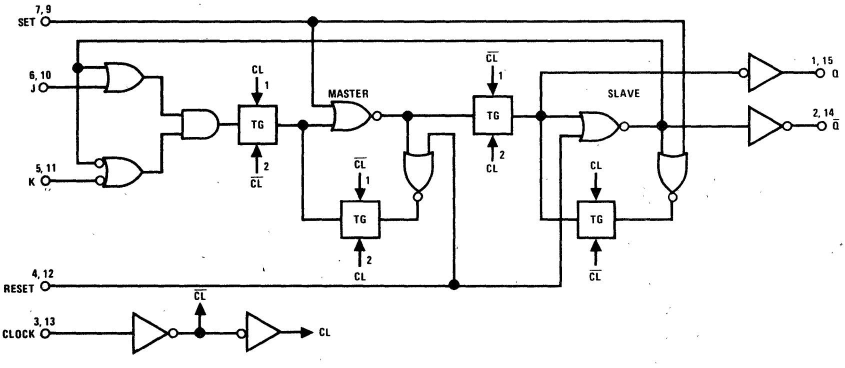
features

■ Wide supply voltage range	3.0V to 15V
■ Low power	50 nW typ
■ Medium speed operation	8.0 MHz typ with 10V supply
■ High noise immunity	0.45 V_{CC} typ

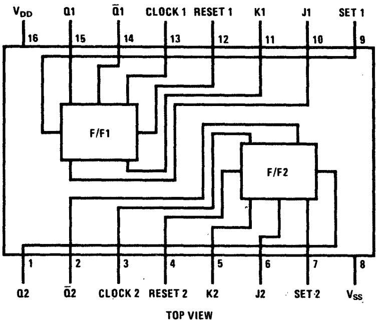
applications

- Automotive
- Data terminals
- Instrumentation
- Medical electronics
- Alarm systems
- Remote metering
- Computers

schematic diagram



connection diagram



truth table

●t_{n-1} INPUTS						◆t_n OUTPUTS	
CL▲	J	K	S	R	Q	Q	$\overline{Q}$
_/‾	I	X	O	O	O	I	O
_/‾	X	O	O	O	I	I	O
_/‾	O	X	O	O	O	O	I
_/‾	X	I	O	O	I	O	I
‾_	X	X	O	O	X	(No change)	
X	X	X	I	O	X	I	O
X	X	X	O	I	X	O	I
X	X	X	I	I	X	★	★

Where:

I = High Level
O = Low Level
▲ = Level Change
X = Don't Care
★ = Invalid Condition

● = t_{n-1} refers to the time interval prior to the positive clock pulse transition
◆ = t_n refers to the time intervals after the positive clock pulse transition

absolute maximum ratings

Voltage at Any Pin (Note 1)	V_{SS} − 0.3V to V_{SS} + 15.5V
Operating Temperature Range	
CD4027M	−55°C to +125°C
CD4027C	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500 mW
Operating V_{DD} Range	V_{SS} + 3.0V to V_{SS} + 15V
Lead Temperature (Soldering, 10 seconds)	300°C

dc electrical characteristics CD4027M

PARAMETER	CONDITIONS	LIMITS									UNITS
		-55°C			25°C			125°C			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Quiescent Device Current (I_L)	V_{DD} = 5.0V			1.0		0.005	1.0			60	μA
	V_{DD} = 10V			2.0		0.005	2.0			120	μA
Quiescent Device Dissipation/Package (P_D)	V_{DD} = 5.0V			5.0		0.025	5.0			300	μW
	V_{DD} = 10V			20		0.05	20			1,200	μW
Output Voltage Low Level (V_{OL})	V_{DD} = 5.0V			0.01		0	0.01			0.05	V
	V_{DD} = 10V			0.01		0	0.01			0.05	V
Output Voltage High Level (V_{OH})	V_{DD} = 5.0V	4.99			4.99	5.0		4.95			V
	V_{DD} = 10V	9.99			9.99	10		9.95			V
Noise Immunity (V_{NL}) (All Inputs)	V_{DD} = 5.0V	1.5			1.5	2.25		1.4			V
	V_{DD} = 10V	3.0			3.0	4.5		2.9			V
Noise Immunity (V_{NH})(All Inputs)	V_{DD} = 5.0V	1.4			1.5	2.25		1.5			V
	V_{DD} = 10V	2.9			3.0	4.5		3.0			V
Output Drive Current N-Channel (I_DN)	V_{DD} = 5.0V, V_O = 0.5V	0.63			0.5	1.0		0.33			mA
	V_{DD} = 10V, V_O = 0.5V	1.25			1.0	2.5		0.7			mA
Output Drive Current P-Channel (I_DP)	V_{DD} = 5.0V, V_O = 4.5V	−0.31			−0.25	−0.5		−0.175			mA
	V_{DD} = 10V, V_O = 9.5V	−0.8			−0.65	−1.3		−0.45			mA
Input Current (I_I)	Any Input					10					pA

dc electrical characteristics CD4027C

PARAMETER	CONDITIONS	LIMITS									UNITS
		-40°C			25°C			85°C			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Quiescent Device Current (I_L)	V_{DD} = 5.0V			10		0.01	10			140	μA
	V_{DD} = 10V			20		0.05	20			280	μA
Quiescent Device Dissipation/Package (P_D)	V_{DD} = 5.0V			50		0.05	50			700	μW
	V_{DD} = 10V			200		0.02	200			2,800	μW
Output Voltage Low Level (V_{OL})	V_{DD} = 5.0V			0.01		0	0.01			0.05	V
	V_{DD} = 10V			0.01		0	0.01			0.05	V
Output Voltage High Level (V_{OH})	V_{DD} = 5.0V	4.99			4.99	5.0		4.95			V
	V_{DD} = 10V	9.99			9.99	10		9.95			V
Noise Immunity (V_{NL})(All Inputs)	V_{DD} = 5.0V	1.5			1.5	2.25		1.4			V
	V_{DD} = 10V	3.0			3.0	4.5		2.9			V
Noise Immunity (V_{NH})(All Inputs)	V_{DD} = 5.0V	1.4			1.5	2.25		1.5			V
	V_{DD} = 10V	2.9			3.0	4.5		3.0			V
Output Drive Current N-Channel (I_DN)	V_{DD} = 5.0V, V_O = 0.5V	0.3			0.3	1.0		0.24			mA
	V_{DD} = 10V, V_O = 0.5V	0.72			0.6	2.5		0.5			mA
Output Drive Current P-Channel (I_DP)	V_{DD} = 5.0V, V_O = 4.5V	−0.17			−0.14	−0.5		−0.063			mA
	V_{DD} = 10V, V_O = 9.5V	−0.4			−0.33	−1.3		−0.27			mA
Input Current (I_I)	Any Input					10					pA

Note 1: This device should not be connected to circuits with power on because high transient voltages may cause permanent damage.

ac electrical characteristics CD4027M

T_A = 25°C, V_{SS} = 0V, C_L = 15 pF, and input rise and fall times = 20 ns, except t_{rCL} and t_{fCL}.

PARAMETERS	CONDITIONS	LIMITS			UNITS
		MIN	TYP	MAX	
Propagation Delay Time (t_{PHL})	V_{DD} = 5.0V		150	300	ns
Propagation Delay Time (t_{PLH})	V_{DD} = 10V		75	110	ns
Transition Time (t_{THL})	V_{DD} = 5.0V		75	125	ns
Transition Time (t_{TLH})	V_{DD} = 10V		50	70	ns
Minimum Clock Pulse Width (t_{WL})	V_{DD} = 5.0V		125	300	ns
Minimum Clock Pulse Width (t_{WH})	V_{DD} = 10V		50	100	ns
Maximum Clock Rise and Fall Time ($^*t_{rCL}$)	V_{DD} = 5.0V	15			µs
Maximum Clock Rise and Fall Time (t_{fCL})	V_{DD} = 10V	5.0			µs
Set-Up Time	V_{DD} = 5.0V V_{DD} = 10V		70 25	150 50	ns ns
Maximum Clock Frequency (Toggle Mode) (fCL)	V_{DD} = 5.0V V_{DD} = 10V	1.5 4.5	3.0 8.0		MHz MHz
Input Capacitance (C_I)			5.0		pF
SET AND RESET OPERATION					
Propagation Delay Time ($t_{PHL(R)}$)	V_{DD} = 5.0V		175	225	ns
Propagation Delay Time ($t_{PLH(S)}$)	V_{DD} = 10V		75	110	ns
Minimum Set and Reset Pulse Widths ($t_{WH(S)}$)	V_{DD} = 5.0V		125	200	ns
Minimum Set and Reset Pulse Widths ($t_{WL(R)}$)	V_{DD} = 10V		50	80	ns

ac electrical characteristics CD4027C

T_A = 25°C, V_{SS} = 0V, C_L = 15 pF, and input rise and fall times = 20 ns, except t_{rCL} and t_{fCL}.

PARAMETERS	CONDITIONS	LIMITS			UNITS
		MIN	TYP	MAX	
Propagation Delay Time (t_{PHL})	V_{DD} = 5.0V		150	400	ns
Propagation Delay Time (t_{PLH})	V_{DD} = 10V		75	150	ns
Transition Time (t_{THL})	V_{DD} = 5.0V		75	250	ns
Transition Time (t_{TLH})	V_{DD} = 10V		50	140	ns
Minimum Clock Pulse Width (t_{WL})	V_{DD} = 5.0V		125	400	ns
Minimum Clock Pulse Width (t_{WH})	V_{DD} = 10V		50	130	ns
Maximum Clock Rise and Fall Time ($^*t_{rCL}$)	V_{DD} = 5.0V	15			µs
Maximum Clock Rise and Fall Time (t_{fCL})	V_{DD} = 10V	5.0			µs
Set-Up Time	V_{DD} = 5.0V V_{DD} = 10V		70 25	200 75	ns ns
Maximum Clock Frequency (Toggle Mode) (fCL)	V_{DD} = 5.0V V_{DD} = 10V	1.0 3.0	3.0 8.0		MHz MHz
Input Capacitance (C_I)			5.0		pF
SET AND RESET OPERATION					
Propagation Delay Time ($t_{PHL(R)}$)	V_{DD} = 5.0V		175	350	ns
Propagation Delay Time ($t_{PLH(S)}$)	V_{DD} = 10V		75	150	ns
Minimum Set and Reset Pulse Widths ($t_{WH(S)}$)	V_{DD} = 5.0V		125	300	ns
Minimum Set and Reset Pulse Widths ($t_{WL(R)}$)	V_{DD} = 10V		50	120	ns

CD4028M/CD4028C BCD-to-decimal decoder

general description

The CD4028M/CD4028C is a BCD-to-decimal or binary-to-octal decoder consisting of four inputs, decoding logic gates, and ten output buffers. A BCD code applied to the four inputs, A, B, C and D, results in a high level at the selected one of ten decimal decoded outputs. Similarly, a 3-bit binary code applied to inputs A, B and C is decoded in octal at outputs 0 through 7. A high level signal at the D input inhibits octal decoding and causes outputs 0 through 7 to go low.

All inputs are protected against static discharge damage by diode clamps to V_{DD} and V_{SS}.

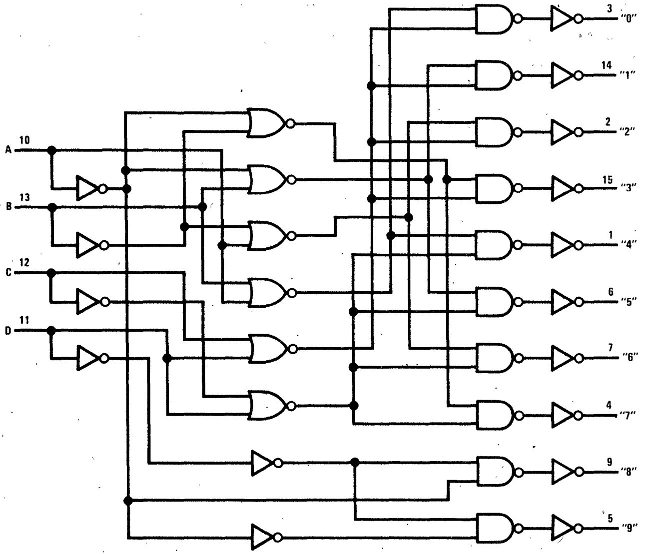
features

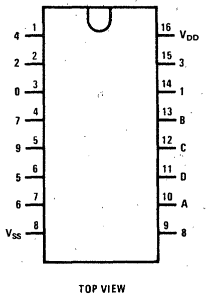
- Wide supply voltage range 3.0V to 15V
- High noise immunity 0.45 V_{CC} (typ)
- Low power
- Medium speed operation t_{THL}, t_{TLH} = 30 ns (typ) at V_{DD} = 10V
- Glitch free outputs
- High decoded output drive capability 8 mA (typ)
- "Positive logic" on inputs and outputs

applications

- Code conversion
- Address decoding
- Indicator—tube decoder

logic and connection diagrams





absolute maximum ratings

Voltage at Any Pin (Note 1)	$V_{SS} - 0.3V$ to $V_{DD} + 0.3V$
Operating Temperature Range	
CD4028M	−55°C to +125°C
CD4028C	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500 mW
Operating V_{DD} Range	$V_{SS} + 3.0V$ to $V_{SS} + 15V$
Lead Temperature (Soldering, 10 seconds)	300°C

dc electrical characteristics CD4028M

PARAMETER	CONDITIONS	LIMITS									UNITS
		−55°C			25°C			125°C			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Quiescent Device Current (I_L)	$V_{DD} = 5V$			5		0.5	5			300	µA
	$V_{DD} = 10V$			10		1	10			600	µA
Quiescent Device Dissipation/Package (P_D)	$V_{DD} = 5V$			25		2.5	25			1500	µW
	$V_{DD} = 10V$			100		10	100			6000	µW
Output Voltage Low Level (V_{OL})	$V_{DD} = 5V$			0.01		0	0.01			0.05	V
	$V_{DD} = 10V$			0.01		0	0.01			0.05	V
Output Voltage High Level (V_{OH})	$V_{DD} = 5V$	4.99			4.99	5			4.95		V
	$V_{DD} = 10V$	9.99			9.99	10			9.95		V
Noise Immunity (V_{NL}) (All Inputs)	$V_{DD} = 5V$	1.5			1.5	2.25		1.4			V
	$V_{DD} = 10V$	3			3	4.5		2.9			V
Noise Immunity (V_{NH}) (All Inputs)	$V_{DD} = 5V$	1.4			1.5	2.25		1.5			V
	$V_{DD} = 10V$	2.9			3	4.5		3			V
Output Drive Current N-Channel (I_DN)	$V_{DD} = 5V$, $V_O = 0.5V$	0.75			0.6	1.2		0.45			mA
	$V_{DD} = 10V$, $V_O = 0.5V$	1.5			1.2	2.4		0.9			mA
Output Drive Current P-Channel (I_DP)	$V_{DD} = 5V$, $V_O = 4.5V$	−0.7			−0.45	−0.9		−0.32			mA
	$V_{DD} = 10V$, $V_O = 9.5V$	−1.4			−0.95	−1.9		−0.65			mA
Input Current (I_I)	Any Input					10					pA

dc electrical characteristics CD4028C

PARAMETER	CONDITIONS	LIMITS									UNITS
		−40°C			25°C			85°C			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Quiescent Device Current (I_L)	$V_{DD} = 5V$			50		5	50			700	µA
	$V_{DD} = 10V$			100		10	100			1400	µA
Quiescent Device Dissipation/Package (P_D)	$V_{DD} = 5V$			250		25	250			3500	µW
	$V_{DD} = 10V$			1000		100	1000			14000	µW
Output Voltage Low Level (V_{OL})	$V_{DD} = 5V$			0.01		0	0.01			0.05	V
	$V_{DD} = 10V$			0.01		0	0.01			0.05	V
Output Voltage High Level (V_{OH})	$V_{DD} = 5V$	4.99			4.99	5		4.95			V
	$V_{DD} = 10V$	9.99			9.99	10		9.95			V
Noise Immunity (V_{NL}) (All Inputs)	$V_{DD} = 5V$	1.5			1.5	2.25		1.4			V
	$V_{DD} = 10V$	3.0			3	4.5		2.9			V
Noise Immunity (V_{NH}) (All Inputs)	$V_{DD} = 5V$	1.4			1.5	2.25		1.5			V
	$V_{DD} = 10V$	2.9			3	4.5		3			V
Output Drive Current N-Channel (I_DN)	$V_{DD} = 5V$, $V_O = 0.5V$	0.35			0.3	1.2		0.25			mA
	$V_{DD} = 10V$, $V_O = 0.5V$	0.7			0.6	2.4		0.5			mA
Output Drive Current P-Channel (I_DP)	$V_{DD} = 5V$, $V_O = 4.5V$	−0.32			−0.22	−0.9		−0.18			mA
	$V_{DD} = 10V$, $V_O = 9.5V$	−0.65			−0.48	−1.9		−0.4			mA
Input Current (I_I)	Any Input					10					pA

Note 1: This device should not be connected to circuits with power on because high transient voltages may cause permanent damage.

ac electrical characteristics CD4028M

T_A = 25°C, V_{SS} = 0V, C_L = 15 pF, and input rise and fall times = 20 ns.

PARAMETERS	CONDITIONS	LIMITS			UNITS
		MIN	TYP	MAX	
Propagation Delay Time (t_{PHL}, t_{PLH})	V_{DD} = 5V		200	480	ns
	V_{DD} = 10V		100	180	ns
Transition Time (t_{THL}, t_{TLH})	V_{DD} = 5V		60	150	ns
	V_{DD} = 10V		30	75	ns
Input Capacitance (C_I)	Any Input		5		pF

ac electrical characteristics CD4028C

T_A = 25°C, V_{SS} = 0V, C_L = 15 pF, and input rise and fall times = 20 ns.

PARAMETERS	CONDITIONS	LIMITS			UNITS
		MIN	TYP	MAX	
Propagation Delay Time (t_{PHL}, t_{PLH})	V_{DD} = 5V		200	700	ns
	V_{DD} = 10V		100	290	ns
Transition Time (t_{THL}, t_{TLH})	V_{DD} = 5V		60	300	ns
	V_{DD} = 10V		30	150	ns
Input Capacitance (C_I)	Any Input		5		pF

truth table

A	B	C	D	0	1	2	3	4	5	6	7	8	9
0	0	0	0	1	0	0	0	0	0	0	0	0	0
0	0	0	1	0	1	0	0	0	0	0	0	0	0
0	0	1	0	0	0	1	0	0	0	0	0	0	0
0	0	1	1	0	0	0	1	0	0	0	0	0	0
0	1	0	0	0	0	0	0	1	0	0	0	0	0
0	1	0	1	0	0	0	0	0	1	0	0	0	0
0	1	1	0	0	0	0	0	0	0	1	0	0	0
0	1	1	1	0	0	0	0	0	0	0	1	0	0
1	0	0	0	0	0	0	0	0	0	0	0	1	0
1	0	0	1	0	0	0	0	0	0	0	0	0	1

1 = High Level
0 = Low Level

CD4029M/CD4029C presettable, binary/decade, up/down counter

general description

The CD4029M/CD4029C is a presettable up/down counter which counts in either binary or decade mode depending on the voltage level applied at binary/decade input. When binary/decade is at logical "1" the counter counts in binary, otherwise it counts in decade. Similarly, the counter counts up when the up/down input is at logical "1" and vice versa.

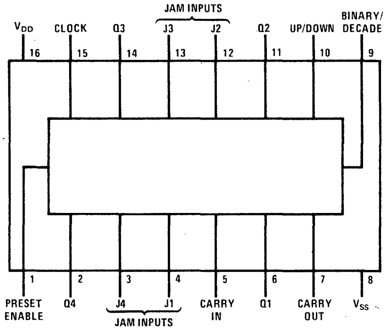
A logical "1" preset enable signal allows information at the "jam" inputs to preset the counter to any state asynchronously with the clock. The counter is advanced one count at the positive-going edge of the clock if the carry in and preset enable inputs are at logical "0." Advancement is inhibited when either or both of these two inputs is at logical "1." The carry out signal is normally at logical "1" state and goes to logical "0" state when the counter reaches its maximum count in the "up" mode or the minimum count in the "down" mode provided the carry input is at logical "0" state.

All inputs are protected against static discharge by diode clamps to both V_{DD} and V_{SS}.

features

■ Wide supply voltage range	3.0V to 15V
■ High noise immunity	0.45 V_{DD} typ
■ Medium speed operation	9.0 MHz typ with 10V V_{DD} and 15 pF load

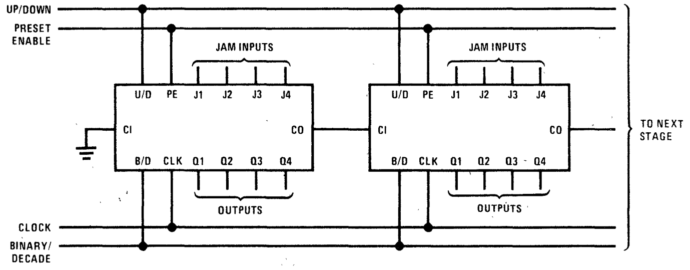
connection diagram



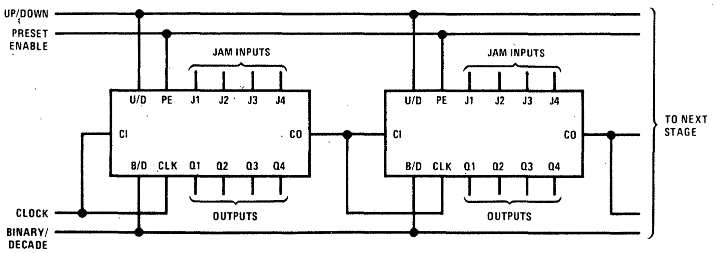
TOP VIEW

cascading packages

Parallel Clocking



Ripple Clocking



absolute maximum ratings

Voltage at Any Pin	V_{SS} −0.3V to V_{SS} +15.5V	Storage Temperature Range	−65°C to +150°C
Operating Temperature Range		Package Dissipation	500 mW
CD4029M	−55°C to +125°C	Operating V_{DD} Range	V_{SS} +3.0V to V_{SS} +15V
CD4029C	−40°C to +85°C	Lead Temperature (Soldering, 10 seconds)	300°C

dc electrical characteristics CD4029M

PARAMETER	CONDITIONS	LIMITS									UNITS
		−55°C			25°C			125°C			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Quiescent Device Current (I_L)	V_{DD} = 5.0V			5.0		0.3	5.0			300	µA
	V_{DD} = 10V			10		0.5	10			600	µA
Quiescent Device Dissipation/Package (P_D)	V_{DD} = 5.0V			25		1.5	25			1,500	µW
	V_{DD} = 10V			100		5.0	100			6,000	µW
Output Voltage Low Level (V_{OL})	V_{DD} = 5.0V			0.01			0.01			0.05	V
	V_{DD} = 10V			0.01			0.01			0.05	V
Output Voltage High Level (V_{OH})	V_{DD} = 5.0V	4.99			4.99	5.0		4.95			V
	V_{DD} = 10V	9.99			9.99	10		9.95			V
Noise Immunity (V_{NL}) (All Inputs)	V_{DD} = 5.0V, V_O = 0.8V	1.5			1.5	2.25		1.4			V
	V_{DD} = 10V, V_O = 1.0V	3.0			3.0	4.5		2.9			V
Noise Immunity (V_{NH}) (All Inputs)	V_{DD} = 5.0V, V_O = 4.2V	1.4			1.5	2.25		1.5			V
	V_{DD} = 10V, V_O = 9.0V	2.9			3.0	4.5		3.0			V
Output Drive Current N-Channel (I_DN)	Q Outputs										
	V_{DD} = 5.0V, V_O = 0.5V	0.5			0.4	1.8		0.28			mA
	V_{DD} = 10V, V_O = 0.5V	0.74			0.6	4.0		0.42			mA
Output Drive Current N-Channel (I_DN)	Carry Output										
	V_{DD} = 5.0V, V_O = 0.5V	0.1			0.08	1.8		0.06			mA
	V_{DD} = 10V, V_O = 0.5V	0.4			0.32	4.0		0.22			mA
Output Drive Current P-Channel (I_DP)	Q Outpus										
	V_{DD} = 5.0V, V_O = 4.5V	−0.18			−0.12	−0.9		−0.08			mA
	V_{DD} = 10V, V_O = 9.5V	−0.3			−0.2	−2.0		−0.14			mA
Output Drive Current P-Channel (I_DP)	Carry Output										
	V_{DD} = 5.0V, V_O = 4.5V	−0.09			−0.06	−0.9		−0.04			mA
	V_{DD} = 10V, V_O = 9.5V	−0.15			−0.1	−2.0		−0.07			mA
Input Current (I_I)						10					pA

dc electrical characteristics CD4029C

PARAMETER	CONDITIONS	LIMITS									UNITS
		−40°C			25°C			85°C			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Quiescent Device Current (I_L)	V_{DD} = 5.0V			50		0.5	50			700	µA
	V_{DD} = 10V			100		1.0	100			1,400	µA
Quiescent Device Dissipation/Package (P_D)	V_{DD} = 5.0V			250		2.5	250			3,500	µW
	V_{DD} = 10V			1,000		10	1,000			14,000	µW
Output Voltage Low Level (V_{OL})	V_{DD} = 5.0V			0.01		0	0.01			0.05	V
	V_{DD} = 10V			0.01		0	0.01			0.05	V
Output Voltage High Level (V_{OH})	V_{DD} = 5.0V	4.99			4.99	5.0		4.95			V
	V_{DD} = 10V	9.99			9.99	10		9.95			V
Noise Immunity (V_{NL}) (All Inputs)	V_{DD} = 5.0V, V_O = 0.8V	1.5			1.5	2.25		1.4			V
	V_{DD} = 10V, V_O = 1.0V	3.0			3.0	4.5		2.9			V
Noise Immunity (V_{NH}) (All Inputs)	V_{DD} = 5.0V, V_O = 4.2V	1.4			1.5	2.25		1.5			V
	V_{DD} = 10V, V_O = 9.0V	2.9			3.0	4.5		3.0			V
Output Drive Current N-Channel (I_DN)	Outputs										
	V_{DD} = 5.0V, V_O = 0.5V	0.24			0.2	1.8		0.16			mA
	V_{DD} = 10V, V_O = 0.5V	0.36			0.3	4.0		0.24			mA
Output Drive Current N-Channel (I_DN)	Carry Output										
	V_{DD} = 5.0V, V_O = 0.5V	0.05			0.04	1.8		0.03			mA
	V_{DD} = 10V, V_O = 0.5V	0.19			0.16	4.0		0.13			mA
Output Drive Current P-Channel (I_DP)	Outputs										
	V_{DD} = 5.0V, V_O = 4.5V	−0.07			−0.06	−0.9		−0.05			mA
	V_{DD} = 10V, V_O = 9.5V	−0.14			−0.1	−2.0		−0.08			mA
Output Drive Current P-Channel (I_DP)	Carry Output										
	V_{DD} = 5.0V, V_O = 4.5V	−0.04			−0.03	−0.9		−0.02			mA
	V_{DD} = 10V, V_O = 9.5V	−0.07			−0.05	−2.0		−0.04			mA
Input Current (I_I)						10					pA

ac electrical characteristics CD4029M

T_A = 25°C and C_L = 15 pF. Typical Temperature Coefficient for all values of V_{DD} = 0.3%/°C.

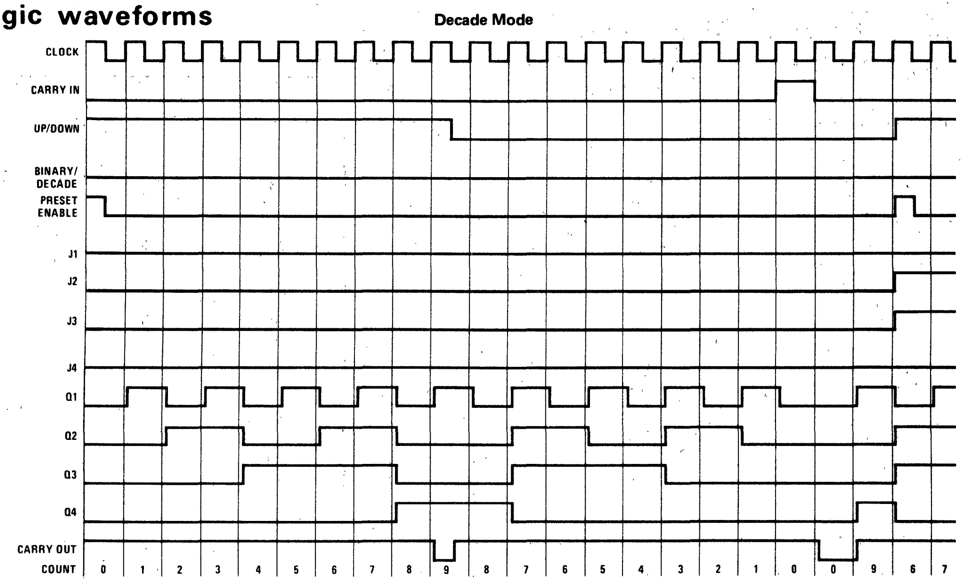
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CLOCKED OPERATION					
Propagation Delay Time to Q Outputs (t_{PHL}, t_{PLH})	V_{DD} = 5.0V V_{DD} = 10V		150 65	650 230	ns ns
Propagation Delay Time to Carry Output (t_{PHL}, t_{PLH})	V_{DD} = 5.0V V_{DD} = 10V		280 115	850 300	ns ns
Transition Time/Q Outputs (t_{THL}, t_{TLH})	V_{DD} = 5.0V V_{DD} = 10V		50 25	200 100	ns ns
Transition Time/Carry Output (t_{THL}, t_{TLH})	V_{DD} = 5.0V V_{DD} = 10V		40 20	400 200	ns ns
Minimum Clock Pulse Width (t_{WL}, t_{WH})	V_{DD} = 5.0V V_{DD} = 10V		80 30	340 170	ns ns
Clock Rise and Fall Time (t_{rCL}, t_{fCL})	V_{DD} = 5.0V V_{DD} = 10V			15 15	μs μs
Set-Up Time (t_{SHL}, t_{SLH})	V_{DD} = 5.0V V_{DD} = 10V		140 55	650 230	ns ns
Maximum Clock Frequency (f_{CL})	V_{DD} = 5.0V V_{DD} = 10V	1.5 3.0	3.3 9.0		MHz MHz
Input Capacitance (C_I)	Any Input		5.0		pF
PRESET ENABLE OPERATION					
Propagation Delay Time To Q Outputs (t_{PHL}, t_{PLH})	V_{DD} = 5.0V V_{DD} = 10V		230 100	650 230	ns ns
Propagation Delay Time to Carry Output (t_{PHL}, t_{PLH})	V_{DD} = 5.0V V_{DD} = 10V		340 150	850 300	ns ns
Minimum Preset Enable Pulse Width (t_{WH})	V_{DD} = 5.0V V_{DD} = 10V		80 30	330 160	ns ns
Minimum Preset Enable Removal Time ($t_{REMOVAL}$)	V_{DD} = 5.0V V_{DD} = 10V		145 60	650 230	ns ns
CARRY INPUT OPERATION					
Propagation Delay Time to Carry Output (t_{PHL}, t_{PLH})	V_{DD} = 5.0V V_{DD} = 10V		200 85	350 150	ns ns

ac electrical characteristics CD4029C

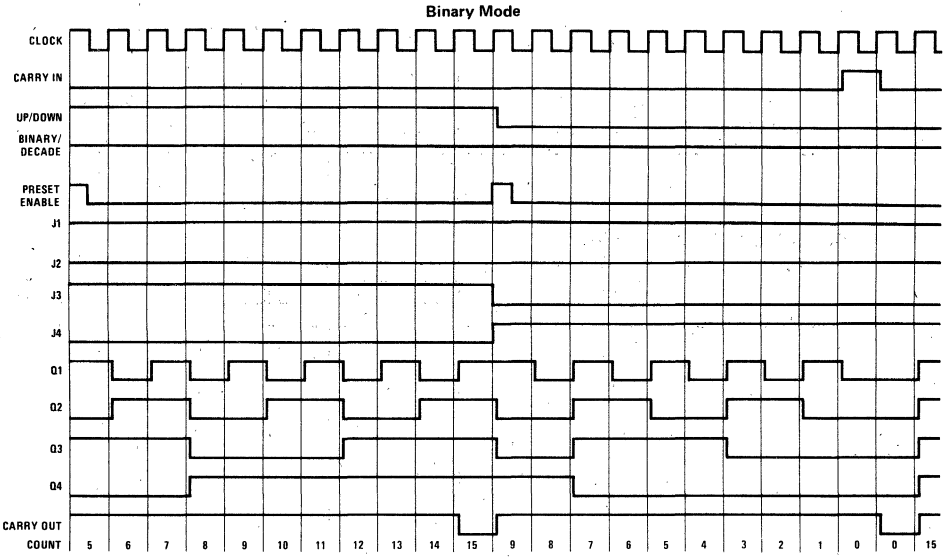
T_A = 25°C and C_L = 15 pF. Typical Temperature Coefficient for all values of V_{DD} = 0.3%/°C.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CLOCKED OPERATION					
Propagation Delay Time to Q Outputs (t_{PHL}, t_{PLH})	V_{DD} = 5.0V V_{DD} = 10V		150 65	1300 460	ns ns
Propagation Delay Time to Carry Output (t_{PHL}, t_{PLH})	V_{DD} = 5.0V V_{DD} = 10V		280 115	1700 600	ns ns
Transition Time/Q Outputs (t_{THL}, t_{TLH})	V_{DD} = 5.0V V_{DD} = 10V		50 25	400 200	ns ns
Transition Time/Carry Output (t_{THL}, t_{TLH})	V_{DD} = 5.0V V_{DD} = 10V		40 20	800 400	ns ns
Minimum Clock Pulse Width (t_{WL}, t_{WH})	V_{DD} = 5.0V V_{DD} = 10V		80 30	500 250	ns ns
Clock Rise and Fall Time (t_{rCL}, t_{fCL})	V_{DD} = 5.0V V_{DD} = 10V			15 15	μs μs
Set-Up Time (t_{SHL}, t_{SLH})	V_{DD} = 5.0V V_{DD} = 10V		140 55	1300 460	ns ns
Maximum Clock Frequency (f_{CL})	V_{DD} = 5.0V V_{DD} = 10V	1 2	3.3 9.0		MHz MHz
Input Capacitance (C_I)	Any Input		5.0		pF
PRESET ENABLE OPERATION					
Propagation Delay Time to Q Outputs (t_{PHL}, t_{PLH})	V_{DD} = 5.0V V_{DD} = 10V		230 100	1300 460	ns ns
Propagation Delay Time to Carry Output (t_{PHL}, t_{PLH})	V_{DD} = 5.0V V_{DD} = 10V		340 150	1700 600	ns ns
Minimum Preset Enable Pulse Width (t_{WH})	V_{DD} = 5.0V V_{DD} = 10V		80 30	660 320	ns ns
Minimum Preset Enable Removal Time ($t_{REMOVAL}$)	V_{DD} = 5.0V V_{DD} = 10V		145 60	1300 460	ns ns
CARRY INPUT OPERATION					
Propagation Delay Time to Carry Output (t_{PHL}, t_{PLH})	V_{DD} = 5.0V V_{DD} = 10V		200 85	700 200	ns ns

logic waveforms

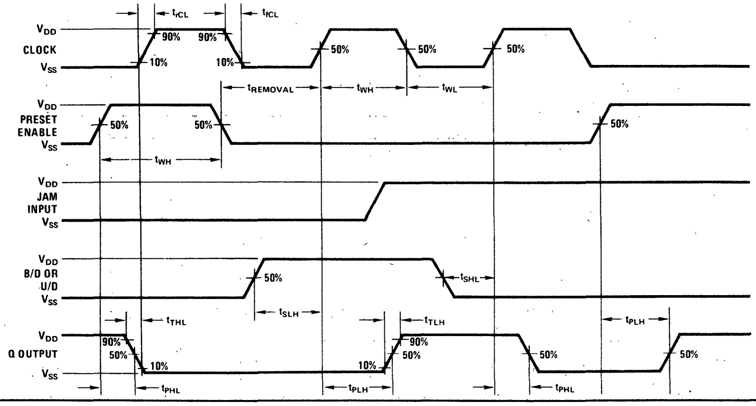


Decade Mode



Binary Mode

switching time waveforms



CD4030M/CD4030C quad EXCLUSIVE-OR gate

general description

These EXCLUSIVE-OR gates are monolithic Complementary MOS (CMOS) integrated circuits constructed with N and P-channel enhancement mode transistors. All inputs are protected against static discharge with diodes to V_{DD} and V_{SS}.

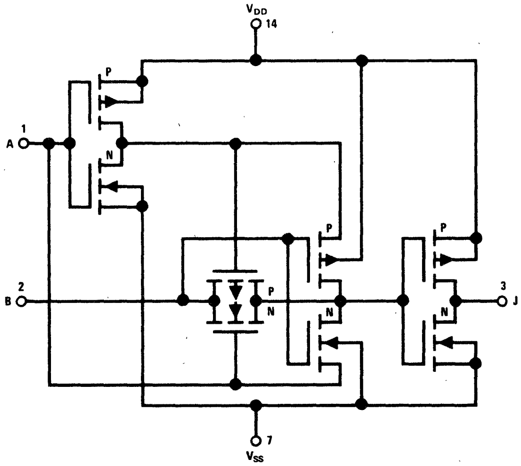
features

■ Wide supply voltage range	3.0V to 15V
■ Low power	100 nW (typ)
■ Medium speed operation	$t_{PHL} = t_{PLH}$ = 40 ns (typ) at C_L = 15 pF, 10V supply
■ High noise immunity	0.45 V_{CC} (typ)

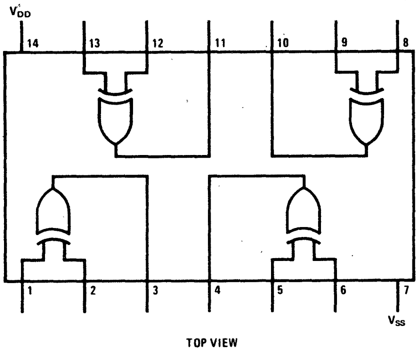
applications

- Automotive
- Data terminals
- Instrumentation
- Medical electronics
- Industrial controls
- Remote metering
- Computers

schematic diagram



connection diagram



absolute maximum ratings

Voltage at Any Pin (Note 1)	V_{SS} − 0.3V to V_{SS} + 15.5V
Operating Temperature Range	
CD4030M	−55°C to +125°C
CD4030C	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500 mW
Operating V_{DD} Range	V_{SS} + 3.0V to V_{SS} + 15V
Lead Temperature (Soldering, 10 seconds)	300°C

dc electrical characteristics CD4030M

PARAMETER	CONDITIONS	LIMITS									UNITS
		-55°C			25°C			125°C			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Quiescent Device Current (I_L)	V_{DD} = 5.0V			0.5		0.005	0.5			30	µA
	V_{DD} = 10V			1.0		0.01	1.0			60	µA
Quiescent Device Dissipation Package (P_D)	V_{DD} = 5.0V			2.5		0.025	2.5			150	µW
	V_{DD} = 10V			10		0.1	10			600	µW
Output Voltage Low Level (V_{OL})	V_{DD} = 5.0V			0.01		0	0.01			0.05	V
	V_{DD} = 10V			0.01		0	0.01			0.05	V
Output Voltage High Level (V_{OH})	V_{DD} = 5.0V	4.99			4.99	5.0		4.95			V
	V_{DD} = 10V	9.99			9.99	10		9.95			V
Noise Immunity (All Inputs) (V_{NL})	V_{DD} = 5.0V	1.5			1.5	2.25		1.4			V
	V_{DD} = 10V	3.0			3.0	4.5		2.9			V
Noise Immunity (All Inputs)(V_{NH})	V_{DD} = 5.0V	1.4			1.5	2.25		1.5			V
	V_{DD} = 10V	2.9			3.0	4.5		3.0			V
Output Drive Current N-Channel (I_DN)	V_{DD} = 5.0V	0.75			0.6	1.2		0.45			mA
	V_{DD} = 10V	1.5			1.2	2.4		0.9			mA
Output Drive Current P-Channel (I_DP)	V_{DD} = 5.0V	−0.45			−0.3	−0.6		−0.21			mA
	V_{DD} = 10V	−0.95			−0.65	−1.3		−0.45			mA
Input Current (I_I)	V_I = 0V or V_I = V_{DD}					10					pA

dc electrical characteristics CD4030C

PARAMETER	CONDITIONS	LIMITS									UNITS
		−40°C			25°C			85°C			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Quiescent Device Current (I_L)	V_{DD} = 5.0V			5.0		0.05	5.0			70	µA
	V_{DD} = 10V			10		0.1	10			140	µA
Quiescent Device Dissipation Package (P_D)	V_{DD} = 5.0V			25		0.25	25			350	µW
	V_{DD} = 10V			100		1.0	100			1,400	µW
Output Voltage Low Level (V_{OL})	V_{DD} = 5.0V			0.01		0	0.01			0.05	V
	V_{DD} = 10V			0.01		0	0.01			0.05	V
Output Voltage High Level (V_{OH})	V_{DD} = 5.0V	4.99			4.99	5.0		4.95			V
	V_{DD} = 10V	9.99			9.99	10		9.95			V
Noise Immunity (All Inputs)(V_{NL})	V_{DD} = 5.0V	1.5			1.5	2.25		1.4			V
	V_{DD} = 10V	3.0			3.0	4.5		2.9			V
Noise Immunity (All Inputs)(V_{NH})	V_{DD} = 5.0V	1.4			1.5	2.25		1.5			V
	V_{DD} = 10V	2.9			3.0	4.5		3.0			V
Output Drive Current N-Channel (I_DN)	V_{DD} = 5.0	0.35			0.3	1.2		0.25			mA
	V_{DD} = 10V	0.7			0.6	2.4		0.5			mA
Output Drive Current P-Channel (I_DP)	V_{DD} = 5.0V	−0.21			−0.15	−0.6		−0.12			mA
	V_{DD} = 10V	−0.45			−0.32	−1.3		−0.25			mA
Input Current (I_I)	V_I = 0V or V_I = V_{DD}					10					pA

Note 1: This device should not be connected to circuits with power on because high transient voltages may cause permanent damage.

ac electrical characteristics CD4030M

at $T_A = 25°C$, $V_{SS} = 0V$, and $C_L = 15\ pF$. Typical temperature coefficient for all values of $V_{DD} = 0.3\%/°C$.

PARAMETER	CONDITIONS	LIMITS			UNITS
		MIN	TYP	MAX	
Propagation Delay Time (t_{PHL})	$V_{DD} = 5.0V$		100	200	ns
	$V_{DD} = 10V$		40	100	ns
Propagation Delay Time (t_{PLH})	$V_{DD} = 5.0V$		100	200	ns
	$V_{DD} = 10V$		40	100	ns
Transition Time High to Low Level (t_{THL})	$V_{DD} = 5.0V$		70	150	ns
	$V_{DD} = 10V$		25	75	ns
Transition Time Low to High Level (t_{TLH})	$V_{DD} = 5.0V$		80	150	ns
	$V_{DD} = 10V$		30	75	ns
Input Capacitance (C_I)	$V_I = 0V$ or $V_I = V_{DD}$		5.0		pF

ac electrical characteristics CD4030C

PARAMETER	CONDITIONS	LIMITS			UNITS
		MIN	TYP	MAX	
Propagation Delay Time (t_{PHL})	$V_{DD} = 5.0V$		100	300	ns
	$V_{DD} = 10V$		40	150	ns
Propagation Delay Time (t_{PLH})	$V_{DD} = 5.0V$		100	300	ns
	$V_{DD} = 10V$		40	150	ns
Transition Time High to Low Level (t_{THL})	$V_{DD} = 5.0V$		70	300	ns
	$V_{DD} = 10V$		25	150	ns
Transition Time Low to High Level (t_{TLH})	$V_{DD} = 5.0V$		80	300	ns
	$V_{DD} = 10V$		30	150	ns
Input Capacitance (C_I)	$V_I = 0V$ or $V_I = V_{DD}$		5.0		pF

truth table (For One of Four Identical Gates)

A	B	J
0	0	0
1	0	1
0	1	1
1	1	0

Where: "1" = High Level
"0" = Low Level

CD4035M/CD4035C 4-bit parallel-in/parallel-out shift register

general description

The CD4035M/CD4035C 4-bit parallel-in/parallel-out shift register is a monolithic complementary MOS (CMOS) integrated circuit constructed with P and N-channel enhancement mode transistors. This shift register is a four-stage clocked serial register having provisions for synchronous parallel inputs to each stage and serial inputs to the first stage via J$\overline{K}$ logic. Register stages 2, 3, and 4 are coupled in a serial "D" flip-flop configuration when the register is in the serial mode (Parallel/Serial control low).

Parallel entry via the "D" line of each register stage is permitted only when the Parallel/Serial control is "high."

In the parallel or serial mode information is transferred on positive clock transitions.

When the True/Complement control is "high," the True contents of the register are available at the output terminals. When the True/Complement control is "low," the outputs are the complements of the data in the register. The True/Complement control functions asynchronously with respect to the clock signal.

J$\overline{K}$ input logic is provided on the first stage serial input to minimize logic requirements particularly in counting and sequence-generation applications. With J$\overline{K}$ inputs connected together, the first stage becomes a "D" flip-flop. An asynchronous common reset is also provided.

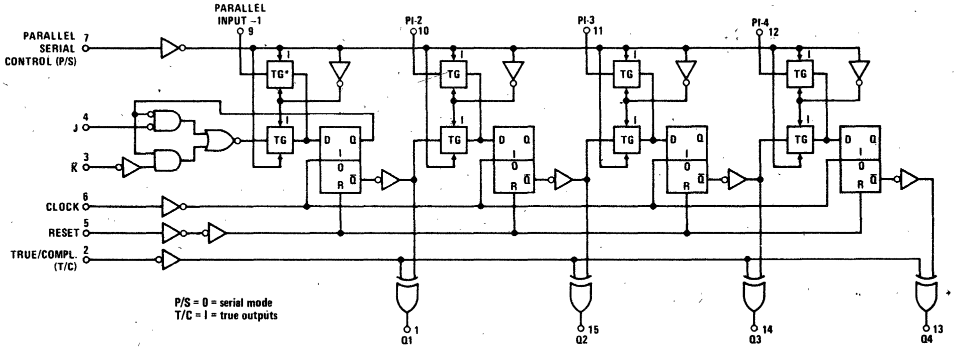
features

- Wide supply voltage range 3.0V to 15V
- 4-stage clocked shift operation
- Synchronous parallel entry on all 4 stages
- J$\overline{K}$ inputs on first stage
- Asynchronous True/Complement control on all outputs
- Reset control
- Static flip-flop operation; master/slave configuration
- Buffered outputs
- Low-power dissipation 5.0µW typ (ceramic)
- High speed to 5.0 MHz

applications

- Automotive
- Data terminals
- Instrumentation
- Medical electronics
- Alarm systems
- Industrial controls
- Remote metering
- Computers

logic diagram



P/S = 0 = serial mode
T/C = I = true outputs

absolute maximum ratings

Voltage at Any Pin (Note 1)	V_{SS} – 0.3V to V_{SS} + 15.5V
Operating Temperature Range	
CD4035M	–55°C to +125°C
CD4035C	–40°C to +85°C
Storage Temperature Range	–65°C to +150°C
Package Dissipation	500 mW
Operating V_{DD} Range	V_{SS} + 3.0V to V_{SS} + 15V
Lead Temperature (Soldering, 10 seconds)	300°C

dc electrical characteristics CD4035M

PARAMETER	CONDITIONS	LIMITS									UNITS
		-55°C			25°C			125°C			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Quiescent Device Current (I_L)	V_{DD} = 5.0V			5.0		0.3	5.0			300	μA
	V_{DD} = 10V			10		0.5	10			600	μA
Quiescent Device Dissipation Package (P_D)	V_{DD} = 5.0V			25		1.5	25			1,500	μW
	V_{DD} = 10V			100		5.0	100			6,000	μW
Output Voltage Low Level (V_{OL})	V_{DD} = 5.0V			0.01		0	0.01			0.05	V
	V_{DD} = 10V			0.01		0	0.01			0.05	V
Output Voltage High Level (V_{OH})	V_{DD} = 5.0V	4.99			4.99	5.0		4.95			V
	V_{DD} = 10V	9.99			9.99	10		9.95			V
Noise Immunity (V_{NL}) (All Inputs)	V_O = 0.8V, V_{DD} = 5.0V	1.5			1.5	2.25		1.4			V
	V_O = 1.0V, V_{DD} = 10V	3.0			3.0	4.5		2.9			V
Noise Immunity (V_{NH}) (All Inputs)	V_O = 4.2V, V_{DD} = 5.0V	1.4			1.5	2.25		1.5			V
	V_O = 9.0V, V_{DD} = 10V	2.9			3.0	4.5		3.0			V
Output Drive Current N-Channel (I_DN)	V_O = 0.5V, V_{DD} = 5.0V	0.62			0.50	1.0		0.35			mA
	V_O = 0.5V, V_{DD} = 10V	1.55			1.25	2.5		0.87			mA
Output Drive Current P-Channel (I_DP)	V_O = 4.5V, V_{DD} = 5.0V	–0.31			–0.25	–0.5		–0.17			mA
	V_O = 9.5V, V_{DD} = 10V	–0.81			–0.65	–1.3		–0.45			mA
Input Current (I_I)						10					pA

dc electrical characteristics CD4035C

PARAMETER	CONDITIONS	LIMITS									UNITS
		–40°C			25°C			85°C			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Quiescent Device Current (I_L)	V_{DD} = 5.0V			50		0.5	50			700	μA
	V_{DD} = 10V			100		1.0	100			1,400	μA
Quiescent Device Dissipation Package (P_D)	V_{DD} = 5.0V			250		2.5	250			3,500	μW
	V_{DD} = 10V			1,000		10	1,000			14,000	μW
Output Voltage Low Level (V_{OL})	V_{DD} = 5.0V			0.01		0	0.01			0.05	V
	V_{DD} = 10V			0.01		0	0.01			0.05	V
Output Voltage High Level (V_{OH})	V_{DD} = 5.0V	4.99			4.99	5.0		4.95			V
	V_{DD} = 10V	9.99			9.99	10		9.95			V
Noise Immunity (V_{NL})(All Inputs)	V_O = 0.8V, V_{DD} = 5.0V	1.5			1.5	2.25		1.4			V
	V_O = 1.0V, V_{DD} = 10V	3.0			3.0	4.5		2.9			V
Noise Immunity (V_{NH})(All Inputs)	V_O = 4.2V, V_{DD} = 5.0V	1.4			1.5	2.25		1.5			V
	V_O = 9.0V, V_{DD} = 10V	2.9			3.0	4.5		3.0			V
Output Drive Current N-Channel (I_DN)	V_O = 0.5V, V_{DD} = 5.0V	0.43			0.35	1.0		0.24			mA
	V_O = 0.5V, V_{DD} = 10V	1.05			0.85	2.5		0.59			mA
Output Drive Current P-Channel (I_DP)	V_O = 4.5V, V_{DD} = 5.0V	–0.2			–0.18	–0.5		–0.12			mA
	V_O = 9.5V, V_{DD} = 10V	–0.56			–0.45	–0.31		–0.31			mA
Input Current (I_I)						10					pA

Note 1: This device should not be connected to circuits with the power on because high transient voltages may cause permanent damage.

ac electrical characteristics CD4035M

at $T_A = 25°C$ and $C_L = 15\ pF$. Typical Temperature Coefficient for all values of $V_{DD} = 0.3\%/°C$.

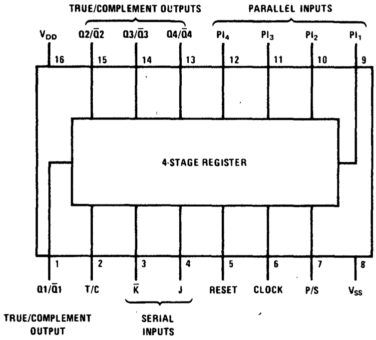
PARAMETER	CONDITIONS	LIMITS			UNITS
		MIN	TYP	MAX	
CLOCKED OPERATION					
Propagation Delay Time (t_{PLH})	$V_{DD} = 5.0V$		250	500	ns
Propagation Delay Time (t_{PHL})	$V_{DD} = 10V$		100	200	ns
Transition Time (t_{THL})	$V_{DD} = 5.0V$		100	200	ns
Transition Time (t_{TLH})	$V_{DD} = 10V$		50	100	ns
Minimum Clock Pulse Duration (t_{WL})	$V_{DD} = 5.0V$		200	335	ns
Minimum Clock Pulse Duration (t_{WH})	$V_{DD} = 10V$		100	165	ns
Clock Rise and Fall Time (t_{rCL})*	$V_{DD} = 5.0V$	15		15	μs
Clock Rise and Fall Time (t_{fCL})	$V_{DD} = 10V$	5.0		5.0	μs
J$\overline{K}$ Lines Setup Time	$V_{DD} = 5.0V$		250	500	ns
	$V_{DD} = 10V$		100	200	ns
Parallel-In Lines Setup Time	$V_{DD} = 5.0V$		100	350	ns
	$V_{DD} = 10V$		50	80	ns
Maximum Clock Frequency (f_{CL})	$V_{DD} = 5.0V$	1.5	2.5		MHz
	$V_{DD} = 10V$	3.0	5.0		MHz
Input Capacitance (C_I)	Any Input		5.0		pF
RESET OPERATION					
Propagation Delay Time (t_{PHL})	$V_{DD} = 5.0V$		250	500	ns
Propagation Delay Time (t_{PLH})	$V_{DD} = 10V$		100	200	ns
Minimum Reset Pulse Duration (t_{WL})	$V_{DD} = 5.0V$		200	400	ns
Minimum Reset Pulse Duration (t_{WH})	$V_{DD} = 10V$		100	175	ns

ac electrical characteristics CD4035C

PARAMETER	CONDITIONS	LIMITS			UNITS
		MIN	TYP	MAX	
CLOCKED OPERATION					
Propagation Delay Time (t_{PLH})	$V_{DD} = 5.0V$		250	700	ns
Propagation Delay Time (t_{PHL})	$V_{DD} = 10V$		100	300	ns
Transition Time (t_{THL})	$V_{DD} = 5.0V$		100	300	ns
Transition Time (t_{TLH})	$V_{DD} = 10V$		50	150	ns
Minimum Clock Pulse Duration (t_{WL})	$V_{DD} = 5.0V$		200	500	ns
Minimum Clock Pulse Duration (t_{WH})	$V_{DD} = 10V$		100	250	ns
Clock Rise and Fall Time (t_{rCL})*	$V_{DD} = 5.0V$	15		15	μs
Clock Rise and Fall Time (t_{fCL})	$V_{DD} = 10V$	5.0		5.0	μs
J$\overline{K}$ Lines Setup Time	$V_{DD} = 5.0V$		250	750	ns
J$\overline{K}$ Lines Setup Time	$V_{DD} = 10V$		100	250	ns
Parallel-In Lines Setup Time	$V_{DD} = 5.0V$		100	500	ns
	$V_{DD} = 10V$		50	100	ns
Maximum Clock Frequency (f_{CL})	$V_{DD} = 5.0V$	1.0	2.5		MHz
	$V_{DD} = 10V$	2.0	5.0		MHz
Input Capacitance (C_I)	Any Input		5.0		pF
RESET OPERATION					
Propagation Delay Time (t_{PHL})	$V_{DD} = 5.0V$		250	700	ns
Propagation Delay Time (t_{PLH})	$V_{DD} = 10V$		100	300	ns
Minimum Reset Pulse Duration (t_{WL})	$V_{DD} = 5.0V$		200	500	ns
Minimum Reset Pulse Duration (t_{WH})	$V_{DD} = 10V$		100	200	ns

*If more than one unit is cascaded t_rCL should be made less than or equal to the sum of the fixed propagation delay time at 15 pF and the transition time of the output driving stage for the estimated capacitive load.

connection diagram



truth table

C_L	t_{n-1} (INPUTS)				t_n (OUTPUTS)
	J	$\overline{K}$	R	Q_{n-1}	Q_n
↑	0	X	0	0	0
↑	1	X	0	0	1
↑	X	0	0	1	0
↑	1	0	0	Q_{n-1}	$\overline{Q_{n-1}}$ TOGGLE MODE
↑	X	1	0	1	1
↓	X	X	0	Q_{n-1}	Q_{n-1}
X	X	X	1	X	0

CD4040M/CD4040C 12-stage ripple-carry binary counter/divider

general description

The CD4040M/CD4040C is a 12-stage ripple-carry binary counter. Buffered outputs from each stage are externally available. The counter is reset to its logical "0" state by a logical "1" on the reset input. The counter is advanced one count on the negative transition of each clock pulse.

features

■ Wide supply voltage range	3.0V to 15V
■ High noise immunity	0.45 V_{CC} typ
■ Medium speed operation	10.0 MHz typ with V_{DD} = 10V

- Low power
- Fully static operation

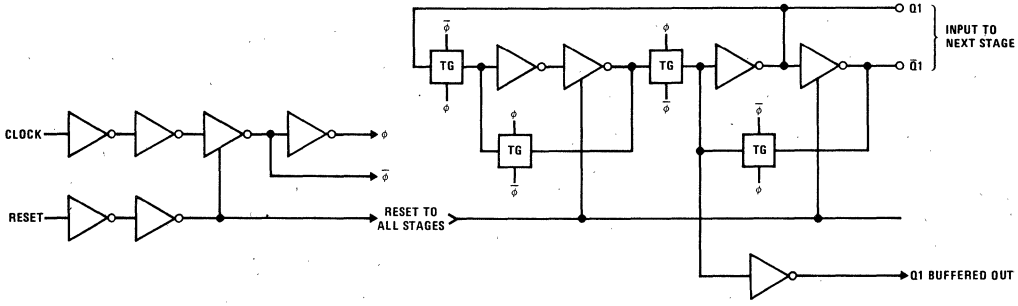
applications

- Automotive
- Instrumentation
- Medical electronics
- Alarm systems
- Industrial electronics
- Remote metering

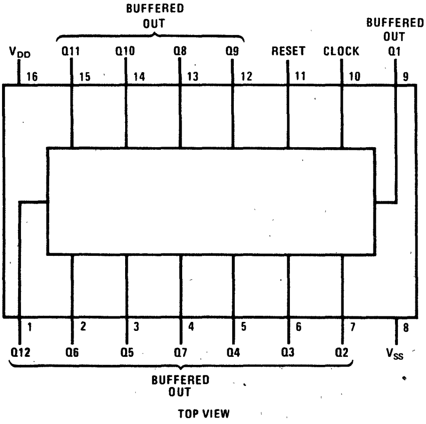
---

logic diagram

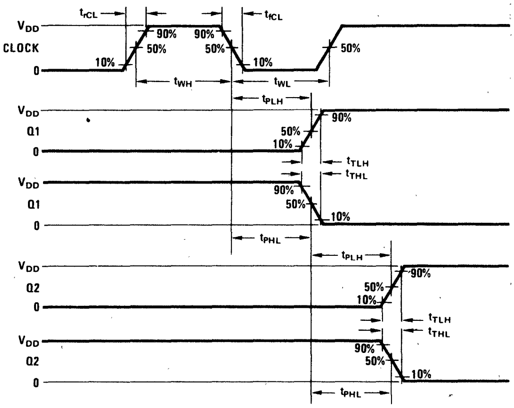
Stage 1 of 12 Binary Stages



connection diagram



switching time waveforms



absolute maximum ratings

Voltage at Any Pin	V_{SS} −0.3V to V_{DD} +0.3V
Operating Temperature Range	
CD4040M	−55°C to +125°C
CD4040C	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500 mW
Operating V_{DD} Range	V_{SS} +3.0V to V_{SS} +15V
Lead Temperature (Soldering, 10 seconds)	300°C

dc electrical characteristics CD4040M

PARAMETER	CONDITIONS	LIMITS									UNITS
		−55°C			25°C			125°C			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Quiescent Device Current (I_L)	V_{DD} = 5.0V			15		0.5	15			900	μA
	V_{DD} = 10V			25		1.0	25			1500	μA
Quiescent Device Dissipation/Package (P_D)	V_{DD} = 5.0V			75		2.5	75			4500	μW
	V_{DD} = 10V			250		10	250			15000	μW
Output Voltage Low Level (V_{OL})	V_{DD} = 5.0V			0.01		0	0.01			0.05	V
	V_{DD} = 10V			0.01		0	0.01			0.05	V
Output Voltage High Level (V_{OH})	V_{DD} = 5.0V	4.99			4.99	5.0		4.95			V
	V_{DD} = 10V	9.99			9.99	10		9.95			V
Noise Immunity (V_{NL}) (All Inputs)	V_{DD} = 5.0V, V_O = 0.8V	1.5			1.5	2.25		1.4			V
	V_{DD} = 10V, V_O = 1.0V	3.0			3.0	4.5		2.9			V
Noise Immunity (V_{NH}) (All Inputs)	V_{DD} = 5.0V, V_O = 4.2V	1.4			1.5	2.25		1.5			V
	V_{DD} = 10V, V_O = 9.0V	2.9			3.0	4.5		3.0			V
Output Drive Current N-Channel (I_DN)	V_{DD} = 5.0V, V_O = 0.5V	0.22			0.18	0.55		0.125			mA
	V_{DD} = 10V, V_O = 0.5V	0.44			0.36	1.1		0.25			mA
Output Drive Current P-Channel (I_DP)	V_{DD} = 5.0V, V_O = 4.5V	−0.15			−0.125	−0.35		−0.085			mA
	V_{DD} = 10V, V_O = 9.5V	−0.3			−0.25	−0.7		−0.175			mA
Input Current (I_I)	Any Input					10					pA

dc electrical characteristics CD4040C

PARAMETER	CONDITIONS	LIMITS									UNITS
		−40°C			25°C			85°C			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Quiescent Device Current (I_L)	V_{DD} = 5.0V			50		1.0	50			700	μA
	V_{DD} = 10V			100		2.0	100			1400	μA
Quiescent Device Dissipation/Package (P_D)	V_{DD} = 5.0V			250		5.0	250			3500	μW
	V_{DD} = 10V			1000		20	1000			14000	μW
Output Voltage Low Level (V_{OL})	V_{DD} = 5.0V			0.01		0	0.01			0.05	V
	V_{DD} = 10V			0.01		0	0.01			0.05	V
Output Voltage High Level (V_{OH})	V_{DD} = 5.0V	4.99			4.99	5		4.95			V
	V_{DD} = 10V	9.99			9.99	10		9.95			V
Noise Immunity (V_{NL}) (All Inputs)	V_{DD} = 5.0V, V_O = 0.8V	1.5			1.5	2.25		1.4			V
	V_{DD} = 10V, V_O = 1.0V	3.0			3	4.5		2.9			V
Noise Immunity (V_{NH}) (All Inputs)	V_{DD} = 5.0V, V_O = 4.2V	1.4			1.5	2.25		1.5			V
	V_{DD} = 10V, V_O = 9.0V	2.9			3.0	4.5		3.0			V
Output Drive Current N-Channel (I_DN)	V_{DD} = 5.0V, V_O = 0.5V	0.21			0.18	0.55		0.15			mA
	V_{DD} = 10V, V_O = 0.5V	0.42			0.36	1.1		0.3			mA
Output Drive Current P-Channel (I_DP)	V_{DD} = 5.0V, V_O = 4.5V	−0.145			−0.125	−0.35		−0.1			mA
	V_{DD} = 10V, V_O = 9.5V	−0.29			−0.25	−0.7		−0.2			mA
Input Current, (I_I)	Any Input					10					pA

ac electrical characteristics

CD4040M T_A = 25°C, C_L = 15 pF, and input rise and fall times = 20 ns except t_{rCL}, t_{fCL}. Typical Temperature Coefficient (for all values of V_{DD}) = 0.3%/°C.

PARAMETER	CONDITIONS	LIMITS			UNITS
		MIN	TYP	MAX	
CLOCKED OPERATION					
Propagation Delay Time (t_{PHL} = t_{PLH}) (Note 1)	V_{DD} = 5.0V		220	900	ns
	V_{DD} = 10V		80	450	ns
Transition Time (t_{THL} = t_{TLH})	V_{DD} = 5.0V		120	300	ns
	V_{DD} = 10V		60	150	ns
Minimum Clock Pulse Width (t_{WL} = t_{WH})	V_{DD} = 5.0V		150	400	ns
	V_{DD} = 10V		50	110	ns
Clock Rise and Fall Time (t_{rCL} = t_{fCL})	V_{DD} = 5.0V			15	μs
	V_{DD} = 10V			7.5	μs
Maximum Clock Frequency (f_{CL})	V_{DD} = 5.0V	1.5	3.0		MHz
	V_{DD} = 10V	4.0	10		MHz
Input Capacitance (C_I)	Any Input		5.0		pF
RESET OPERATION					
Propagation Delay Time ($t_{PHL(R)}$)	V_{DD} = 5.0V		350	1000	ns
	V_{DD} = 10V		150	500	ns
Minimum Reset Pulse Width ($t_{WH(R)}$)	V_{DD} = 5.0V		350	1000	ns
	V_{DD} = 10V		150	500	ns

ac electrical characteristics

CD4040C T_A = 25°C, C_L = 15 pF, and input rise and fall times = 20 ns except t_{rCL}, t_{fCL}. Typical Temperature Coefficient (for all values of V_{DD}) = 0.3%/°C.

PARAMETER	CONDITIONS	LIMITS			UNITS
		MIN	TYP	MAX	
CLOCKED OPERATION					
Propagation Delay Time (t_{PHL} = t_{PLH}) (Note 1)	V_{DD} = 5.0V		220	950	ns
	V_{DD} = 10V		80	475	ns
Transition Time (t_{THL} = t_{TLH})	V_{DD} = 5.0V		120	350	ns
	V_{DD} = 10V		60	175	ns
Minimum Clock Pulse Width (t_{WL} = t_{WH})	V_{DD} = 5.0V		150	500	ns
	V_{DD} = 10V		50	125	ns
Clock Rise and Fall Time (t_{rCL} = t_{fCL})	V_{DD} = 5.0V			15	μs
	V_{DD} = 10V			7.5	μs
Maximum Clock Frequency (f_{CL})	V_{DD} = 5.0V	1.0	3.0		MHz
	V_{DD} = 10V	3.25	10		MHz
Input Capacitance (C_I)	Any Input		5.0		pF
RESET OPERATION					
Propagation Delay Time ($t_{PHL(R)}$)	V_{DD} = 5.0V		350	1250	ns
	V_{DD} = 10V		150	600	ns
Minimum Reset Pulse Width ($t_{WH(R)}$)	V_{DD} = 5.0V		350	1250	ns
	V_{DD} = 10V		150	600	ns

Note 1: Measured from clock to Q1, or Q_i to Q_{i+1}. i = 1, . . ., 11.

CD4042M/CD4042C quad clocked D latch

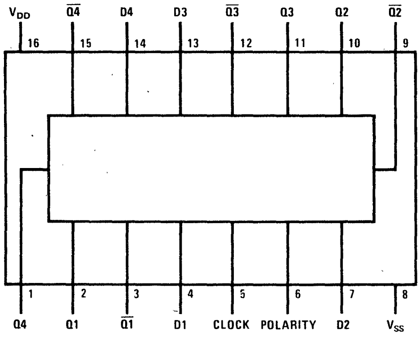
general description

The CD4042M/CD4042C quad clocked "D" latch is a monolithic complementary MOS (CMOS) integrated circuit constructed with P and N-channel enhancement mode transistors. The outputs Q and $\overline{Q}$ either latch or follow the data input depending on the clock level which is programmed by the polarity input. For polarity = 0; the information present at the data input is transferred to Q and $\overline{Q}$ during 0 clock level; and for polarity = 1 the transfer occurs during the 1 clock level. When a clock transition occurs (positive for polarity = 0 and negative for polarity = 1) the information present at the input during the clock transition is retained at the outputs until an opposite clock transition occurs.

features

■ Wide supply voltage range	3.0V to 15V
■ High noise immunity	0.45 V_{CC} typ
■ Clock polarity control	

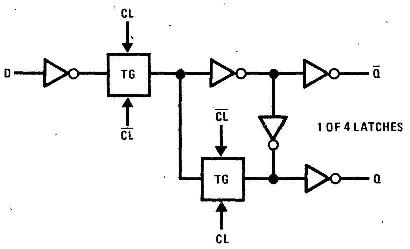
connection diagram and truth table

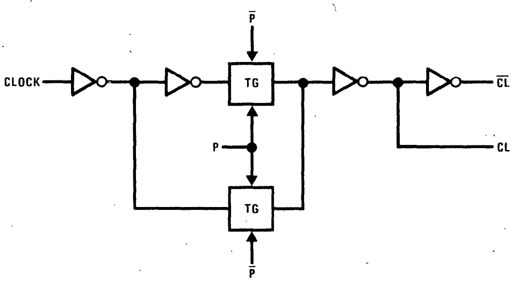


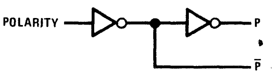
TOP VIEW

CLOCK	POLARITY	Q
0	0	D
↑	0	Latch
1	1	D
↓	1	Latch

logic diagrams







absolute maximum ratings (Note 1)

Voltage at Any Pin	V_{SS} – 0.3V to V_{DD} + 0.3V
Operating Temperature Range	
CD4042M	–55°C to +125°C
CD4042C	–40°C to +85°C
Storage Temperature Range	–65°C to +150°C
Package Dissipation	500 mW
Operating V_{DD} Range	V_{SS} + 3.0V to V_{SS} + 15V
Lead Temperature (Soldering, 10 seconds)	300°C

dc electrical characteristics CD4042M

PARAMETERS	CONDITIONS	LIMITS									UNITS
		–55°C			25°C			125°C			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Quiescent Device Current (I_L)	V_{DD} = 5V			1		0.005	1			60	μA
	V_{DD} = 10V			2		0.005	2			120	μA
Quiescent Device Dissipation/Package (P_D)	V_{DD} = 5V			5		0.025	5			300	μW
	V_{DD} = 10V			20		0.05	20			1200	μW
Output Voltage Low Level (V_{OL})	V_{DD} = 5V			0.01		0	0.01			0.05	V
	V_{DD} = 10V			0.01		0	0.01			0.05	V
Output Voltage High Level (V_{OH})	V_{DD} = 5V	4.99			4.99	5		4.95			V
	V_{DD} = 10V	9.99			9.99	10		9.95			V
Noise Immunity (All Inputs) (V_{NL})	V_{DD} = 5V, V_O = 0.95V	1.5			1.5	2.25		1.4			V
	V_{DD} = 10V, V_O = 2.9V	3			3	4.5		2.9			V
Noise Immunity (All Inputs) (V_{NH})	V_{DD} = 5V, V_O = 3.6V	1.4			1.5	2.25		1.5			V
	V_{DD} = 10V, V_O = 7.2V	2.9			3	4.5		3			V
Output Drive Current N-Channel (I_DN)	V_{DD} = 5V	0.5			0.4	1		0.27			mA
	V_{DD} = 10V	1.25			1	2		0.7			mA
Output Device Current P-Channel (I_DP)	V_{DD} = 5	–0.45			–0.35	–1		–0.25			mA
	V_{DD} = 10V	–1.15			–0.9	–2		–0.6			mA
Input Current (I_I)						10					pA

dc electrical characteristics CD4042C

PARAMETERS	CONDITIONS	LIMITS									UNITS
		–40°C			25°C			85°C			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Quiescent Device Current (I_L)	V_{DD} = 5V			10		0.01	10			140	μA
	V_{DD} = 10V			20		0.02	20			280	μA
Quiescent Device Dissipation/Package (P_D)	V_{DD} = 5V			50		0.05	50			700	μW
	V_{DD} = 10V			200		0.2	200			2800	μW
Output Voltage Low Level (V_{OL})	V_{DD} = 5V			0.01		0	0.01			0.05	V
	V_{DD} = 10V			0.01		0	0.01			0.05	V
Output Voltage High Level (V_{OH})	V_{DD} = 5V	4.99			4.99	5		4.95			V
	V_{DD} = 10V	9.99			9.99	10		9.95			V
Noise Immunity (All Inputs) (V_{NL})	V_{DD} = 5V, V_O = 0.95V	1.5			1.5	2.25		1.4			V
	V_{DD} = 10V, V_O = 2.9V	3			3	4.5		2.9			V
Noise Immunity (All Inputs) (V_{NH})	V_{DD} = 5V, V_O = 3.6V	1.4			1.5	2.25		1.5			V
	V_{DD} = 10V, V_O = 7.2V	2.9			3	4.5		3			V
Output Drive Current N-Channel (I_DN)	V_{DD} = 5V	0.24			0.2	1		0.18			mA
	V_{DD} = 10V	0.6			0.5	2		0.45			mA
Output Drive Current P-Channel (I_DP)	V_{DD} = 5V	–0.2			–0.175	–1		–0.15			mA
	V_{DD} = 10V	–0.34			–0.45	–2		–0.4			mA
Input Current (I_I)						10					pA

ac electrical characteristics CD4042M

PARAMETERS	CONDITIONS	LIMITS			UNITS
		MIN	TYP	MAX	
Propagation Delay Time (t_{PHL}, t_{PLH})	V_{DD} = 5V V_{DD} = 10V		150 75	300 125	ns ns
Transition Time (t_{THL}, t_{TLH})	V_{DD} = 5V V_{DD} = 10V		100 50	200 100	ns ns
Minimum Clock Pulse Width (t_{WL}, t_{WH})	V_{DD} = 5V V_{DD} = 10V		175 50	250 75	ns ns
Clock Rise Time (t_{rCL}) or Clock Fall Time (t_{fCL})	V_{DD} = 5V V_{DD} = 10V			15 5	μs μs
Set-up Time	V_{DD} = 5V V_{DD} = 10V		50 25	100 50	ns ns
Input Capacitance (C_I) (Note 2)	Any Input		5		pF

ac electrical characteristics CD4042C

PARAMETERS	CONDITIONS	LIMITS			UNITS
		MIN	TYP	MAX	
Propagation Delay Time (t_{PHL}, t_{PLH})	V_{DD} = 5V V_{DD} = 10V		150 75	400 200	ns ns
Transition Time (t_{THL}, t_{TLH})	V_{DD} = 5V V_{DD} = 10V		100 50	300 150	ns ns
Minimum Clock Pulse Width (t_{WL}, t_{WH})	V_{DD} = 5V V_{DD} = 10V		175 50	350 175	ns ns
Clock Rise Time (t_{rCL}) or Clock Fall Time (t_{fCL})	V_{DD} = 5V V_{DD} = 10V			15 5	μs μs
Set-up Time	V_{DD} = 5V V_{DD} = 10V		50 25	125 60	ns ns
Input Capacitance (C_I) (Note 2)	Any Input		5		pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

CD4049M/CD4049C, CD4050M/CD4050C
hex buffers

general description

These hex buffers are monolithic complementary MOS (CMOS) integrated circuits constructed with N- and P-Channel enhancement mode transistors. These devices feature logic-level conversion using only one supply voltage (V_{CC}). The input-signal high level (V_{IH}) can exceed the V_{CC} supply voltage when these devices are used for logic-level conversions. These devices are intended for use as hex buffers, CMOS to DTL/TTL converters, or as CMOS current drivers, and they can drive directly two DTL/TTL loads.

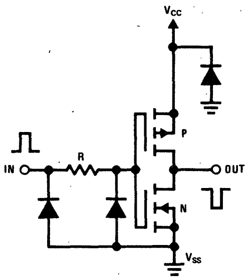
features

- Wide supply voltage range 3.0V to 15V
- High noise immunity 0.45 V_{CC} typ
- Low power 100 nW typ
- Direct drive to 2 TTL loads at 5.0V, V_{CC} = 5.0V, $V_{OL} \leq 0.4V$, $I_{DN} \geq 3.0$ mA
- High source and sink current capability

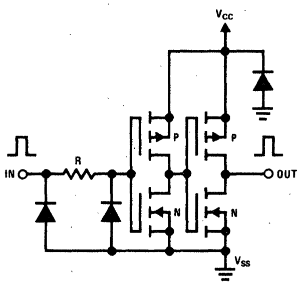
applications

- CMOS hex inverter
- CMOS to DTL/TTL hex converter
- CMOS current "Sink" or "Source" driver
- CMOS high-to-low logic-level converter

schematic diagrams



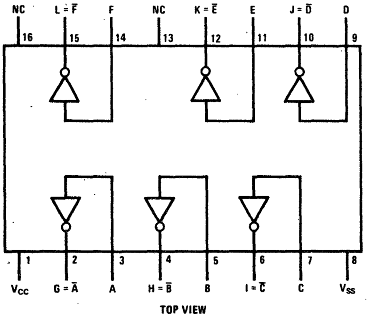
(a) Schematic Diagram of CD4049M, 1 of 6 Identical Units



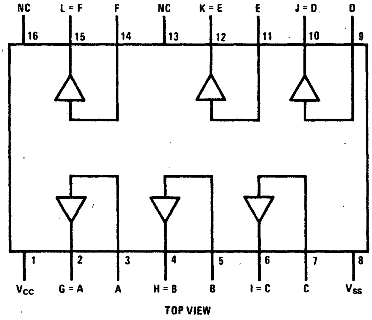
(b) Schematic Diagram of CD4050M, 1 of 6 Identical Units

connection diagrams

CD4049M/CD4049C



CD4050M/CD4050C



absolute maximum ratings (Note 1)

Voltage at Any Pin	V_{SS} – 0.3V to V_{SS} + 15.5V	Storage Temperature Range	–65°C to +150°C
Operating Temperature Range		Package Dissipation	500 mW
CD40XXM	–55°C to +125°C	Operating V_{DD} Range	V_{SS} + 3.0V to V_{SS} + 15V
CD40XXC	–40°C to +85°C	Lead Temperature (Soldering, 10 seconds)	300°C

dc electrical characteristics CD4049C, CD4050C

PARAMETER	CONDITIONS	LIMITS									UNITS
		–40°C			25°C			85°C			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Quiescent Device Current (I_L)	V_{CC} = 5.0V, V_{IH} = V_{CC}			3.0		0.03	3.0			42	μA
	V_{CC} = 10V, V_{IH} = V_{CC}			5.0		0.05	5.0			70	μA
Quiescent Device Dissipation Package (P_D)	V_{CC} = 5.0V, V_{IH} = V_{CC}			15		0.15	15			210	μW
	V_{CC} = 10V, V_{IH} = V_{CC}			50		0.5	50			700	μW
Output Voltage Low Level (V_{OL})	V_{CC} = 5.0V			0.01		0	0.01			0.05	V
	V_{CC} = 10V			0.01		0	0.01			0.05	V
Output Voltage High Level (V_{OH})	V_{CC} = 5.0V	4.99			4.99	5.0		4.95			V
	V_{CC} = 10V	9.99			9.99	10		9.95			V
Noise Immunity (V_{NL}) (All Inputs) CD4049M	V_{CC} = 5.0V, V_{OH} = 3.6V	1.0			1.0	2.25		0.9			V
	V_{CC} = 10V, V_{OH} = 7.2V	2.0			2.0	4.5		1.9			V
Noise Immunity (V_{NL}) (All Inputs) CD4050M	V_{CC} = 5.0V, V_{OL} = 0.95V	1.5			1.5	2.25		1.4			V
	V_{CC} = 10V, V_{OL} = 2.9V	3.0			3.0	4.5		2.9			V
Noise Immunity (V_{NH}) (All Inputs) CD4050M	V_{CC} = 10V, V_{OH} = 7.2V	2.9			3.0	4.5		3.0			V
	V_{CC} = 5.0V, V_{OH} = 3.6V	1.4			1.5	2.25		1.5			V
Noise Immunity (V_{NH}) (All Inputs) CD4049M	V_{CC} = 10V, V_{OL} = 2.9V	2.9			3.0	4.5		3.0			V
	V_{CC} = 5.0V, V_{OL} = 0.95V	1.4			1.5	2.25		1.5			V
Output Drive Current N-Channel (I_DN)	V_{CC} = 4.5V, V_O = 0.4V	3.1			2.6	5.2		2.1			mA
	V_{CC} = 5.0V, V_O = 0.4V	3.6			3.0	6.0		2.5			mA
	V_{CC} = 10V, V_O = 0.5V	9.6			8.0	16		6.6			mA
Output Drive Current P-Channel (I_DP)	V_{CC} = 5.0V, V_O = 4.5V	–0.6			–0.5	–1.0		–0.4			mA
	V_{CC} = 5.0V, V_O = 2.5V	–1.5			–1.25	–2.5		–1.0			mA
	V_{CC} = 10V, V_O = 9.5V	–1.5			–1.25	–2.5		–1.0			mA
Input Current (I_I)	V_{IH} = V_{CC}					10					pA

dc electrical characteristics CD4049M, CD4050M

PARAMETER	CONDITIONS	LIMITS									UNITS
		–55°C			25°C			125°C			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Quiescent Device Current (I_L)	V_{CC} = 5.0V, V_{IH} = V_{CC}			0.3		0.01	0.3			20	μA
	V_{CC} = 10V, V_{IH} = V_{CC}			0.5		0.01	0.5			30	μA
Quiescent Device Dissipation Package (P_D)	V_{CC} = 5.0V, V_{IH} = V_{CC}			1.5		0.05	1.5			100	μW
	V_{CC} = 10V, V_{IH} = V_{CC}			5.0		0.1	5.0			300	μW
Output Voltage Low Level (V_{OL})	V_{CC} = 5.0V			0.01		0	0.01			0.05	V
	V_{CC} = 10V			0.01		0	0.01			0.05	V
Output Voltage High Level (V_{OH})	V_{CC} = 5.0V	4.99			4.99	5.0		4.95			V
	V_{CC} = 10V	9.99			9.99	10		9.95			V
Noise Immunity (V_{NL}) (All Inputs) CD4049M	V_{CC} = 5.0V, V_{OH} = 3.6V	1.0			1.0	2.25		0.9			V
	V_{CC} = 10V, V_{OH} = 7.2V	2.0			2.0	4.5		1.9			V
Noise Immunity (V_{NL}) (All Inputs) CD4050M	V_{CC} = 5.0V, V_{OL} = 0.95V	1.5			1.5	2.25		1.4			V
	V_{CC} = 10V, V_{OL} = 2.9V	3.0			3.0	4.5		2.9			V
Noise Immunity (V_{NH}) (All Inputs) CD4050M	V_{CC} = 10V, V_{OH} = 7.2V	2.9			3.0	4.5		3.0			V
	V_{CC} = 5.0V, V_{OH} = 3.6V	1.4			1.5	2.25		1.5			V
Noise Immunity (V_{NH}) (All Inputs) CD4049M	V_{CC} = 10V, V_{OL} = 2.9V	2.9			3.0	4.5		3.0			V
	V_{CC} = 5.0V, V_{OL} = 0.95V	1.4			1.5	2.25		1.5			V
Output Drive Current N-Channel (I_DN)	V_{CC} = 4.5V, V_O = 0.4V	3.3			2.6	5.2		1.8			mA
	V_{CC} = 5.0V, V_O = 0.4V	3.75			3.0	6.0		2.1			mA
	V_{CC} = 10V, V_O = 0.5V	10			8.0	16		5.6			mA
Output Drive Current P-Channel (I_DP)	V_{CC} = 5.0V, V_O = 4.5V	–0.62			–0.5	–1.0		–0.35			mA
	V_{CC} = 5.0V, V_O = 2.5V	–1.85			–1.25	–2.5		–0.9			mA
	V_{CC} = 10V, V_O = 9.5V	–1.85			–1.25	–2.5		–0.9			mA
Input Current (I_I)	V_{IH} = V_{CC}					10					pA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

ac electrical characteristics CD4050M/CD4050C

T_A = 25°C, C_L = 15 pF, and input rise and fall times = 20 ns. Typical Temperature Coefficient for all values of V_{CC} = 0.3%/°C.

PARAMETER	CONDITIONS	LIMITS			UNITS
		MIN	TYP	MAX	
Propagation Delay Time High-to-Low Level (t_{PHL})	V_{CC} = 5.0V, V_{IH} = V_{CC} V_{CC} = 10V, V_{IH} = V_{CC}		55 25	110 55	ns ns
Propagation Delay Time Low-to-High Level (t_{PLH})	V_{CC} = 5.0V, V_{IH} = V_{CC} V_{CC} = 10V, V_{IH} = V_{CC}		90 40	140 85	ns ns
Transition Time High-to-Low Level (t_{THL})	V_{CC} = 5.0V, V_{IH} = V_{CC} V_{CC} = 10V, V_{IH} = V_{CC}		20 16	45 40	ns ns
Transition Time Low-to-High Level (t_{TLH})	V_{CC} = 5.0V, V_{IH} = V_{CC} V_{CC} = 10V, V_{IH} = V_{CC}		50 30	100 60	ns ns
Input Capacitance (C_I)	Any Input		5.0		pF

ac electrical characteristics CD4049M/CD4049C

T_A = 25°C, C_L = 15 pF, and input rise and fall times = 20 ns. Typical Temperature Coefficient for all values of V_{CC} = 0.3%/°C.

PARAMETER	CONDITIONS	LIMITS			UNITS
		MIN	TYP	MAX	
Propagation Delay Time High-to-Low Level (t_{PHL})	V_{CC} = 5.0V, V_{IH} = V_{CC} V_{CC} = 10V, V_{IH} = V_{CC}		15 10	55 30	ns ns
Propagation Delay Time Low-to-High Level (t_{PLH})	V_{CC} = 5.0V, V_{IH} = V_{CC} V_{CC} = 10V, V_{IH} = V_{CC}		50 25	80 55	ns ns
Transition Time High-to-Low Level (t_{THL})	V_{CC} = 5.0V, V_{IH} = V_{CC} V_{CC} = 10V, V_{IH} = V_{CC}		20 16	45 40	ns ns
Transition Time Low-to-High Level (t_{TLH})	V_{CC} = 5.0V, V_{IH} = V_{CC} V_{CC} = 10V, V_{IH} = V_{CC}		50 30	100 60	ns ns
Input Capacitance (C_I)	Any Input		5.0		pF

CD4066M/CD4066C quad bilateral switch

general description

The CD4066M/CD4066C is a quad bilateral switch intended for the transmission or multiplexing of analog or digital signals. It is pin-for-pin compatible with CD4016M/CD4016C, but has a much lower ON resistance, and ON resistance is relatively constant over the input-signal range.

features

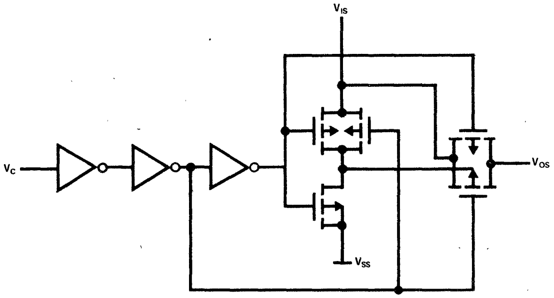
Wide supply voltage range	3V to 15V
High noise immunity	0.45 V_{DD} typ
Wide range of digital and analog switching	±7.5V_{PEAK}
ON resistance for 15V operation	80Ω typ
Matched ON resistance over 15V signal input	5Ω
ON resistance flat over peak-to-peak signal range	
High ON/OFF output voltage ratio	65 dB typ @ f_{is} = 10 kHz, R_L = 10 kΩ
High degree of linearity	<0.5% distortion typ @ f_{is} = 1 kHz, V_{is} = 5V(p-p), $V_{DD} - V_{SS}$ = 10V, R_L = 10 kΩ
Extremely low OFF switch leakage	10 pA typ @ $V_{DD} - V_{SS}$ = 10V, T_A = 25°C
Extremely high control input impedance	10^{12}Ω typ
Low crosstalk between switches	−50 dB typ @ f_{is} = 0.9 MHz, R_L = 1 kΩ
Frequency response, switch ON	40 MHz typ

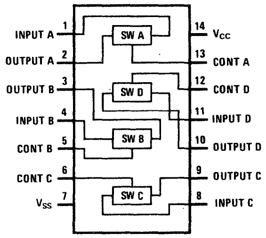
applications

- Analog signal switching/multiplexing
  - Signal gating
  - Squelch control
  - Chopper
  - Modulator/Demodulator
  - Commutating switch
- Digital signal switching/multiplexing
- CMOS logic implementation
- Analog to digital/digital to analog conversion
- Digital control of frequency, impedance, phase, and analog-signal gain

schematic and connection diagrams

1 of 4 Bilateral Switches





absolute maximum ratings

Voltage at Any Pin (Note 1)	V_{SS} −0.3V to V_{SS} +15.5V
Operating Temperature Range	
CD4066M	−55°C to +125°C
CD4066C	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500 mW
Operating V_{DD} Range	V_{SS} +3V to V_{SS} +15V
Lead Temperature (Soldering, 10 seconds)	300°C

electrical characteristics CD4066C

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS −40°C MIN	LIMITS −40°C TYP	LIMITS −40°C MAX	LIMITS 25°C MIN	LIMITS 25°C TYP	LIMITS 25°C MAX	LIMITS 85°C MIN	LIMITS 85°C TYP	LIMITS 85°C MAX	UNITS
Quiescent Dissipation per Package All Switches OFF	P_T	TERMINALS / VOLTS APPLIED V_{DD} 14 +10 V_{SS} 7 GND V_C 5, 6, 12, 13 GND V_{is} 1, 4, 8, 11 $\leq$ +10 V_{os} 2, 3, 9, 10 $\leq$ +10			50		0.1	50			300	μW
All Switches ON		TERMINALS / VOLTS APPLIED V_{DD} 14 +10 V_{SS} 7 GND V_C 5, 6, 12, 13 +10 $V_{is} = V_{OS}$ 1–4, 8–11 $\leq$ +10 (Thru 100Ω)			50		0.1	50			300	μW
SIGNAL INPUTS (V_{is}) AND OUTPUTS (V_{os})												
ON Resistance	R_{ON}	R_L = 10 kΩ; $V_C=V_{DD}$, V_{SS}, V_{is}: +7.5V −7.5V −7.5 to +7.5V +15V 0V 0V to 15V		80	250		80	280		130	300	Ω
		+5V −5V −5V to +5V +10V 0V 0V to 10V		100	450		120	500		170	520	Ω
		+2.5V −2.5V −2.5 to +2.5V +5V 0V 0V to 5V		190	3500		270	5000		330	5200	Ω
ΔON Resistance Between Any 2 of 4 Switches	ΔR_{ON}	R_L = 10 kΩ +7.5V −7.5V −7.5 to +7.5V +15V 0V 0V to 15V					5					Ω
		+5V −5V −5V to +5V +10V 0V 0V to 10V					10					Ω
Sine Wave Response (Distortion)		R_L = 10 kΩ, f_{is} = 1 kHz +5V −5V 5V(p-p) (Note 3)					0.4					%
Input or Output Leakage–Switch OFF (Effective OFF Resistance)		$V_C=V_{SS}$, V_{DD}, V_{is}: −7.5V +7.5V +7.5V −7.5V +7.5V −7.5V (Note 2)			±100		±0.1	±100			±200	nA
		−5V +5V +5V −5V +5V −5V (Note 2)			±100		±0.05	±100			±200	nA
Frequency Response–Switch ON (Sine Wave Input)		$V_C = V_{DD}$ = +5V, V_{SS} = −5V R_L = 1 kΩ, V_{is} = 5V(p-p) $20\ \text{Log}_{10} \frac{V_{os}}{V_{is}} = -3$ dB					40					MHz
Feedthrough Switch OFF		V_{DD} = +5V, $V_C = V_{SS}$ = −5V $20\ \text{Log}_{10} \frac{V_{os}}{V_{is}} = -50$ dB					1.25					MHz
Crosstalk Between Any 2 of the 4 Switches (Frequency at −50 dB)		R_L = 1 kΩ, $V_{is}(A)$ = 5V(p-p) $V_C(A) = V_{DD}$ = +5V $V_C(B) = V_{SS}$ = −5V $20\ \text{Log}_{10} \frac{V_{os}(B)}{V_{is}(A)} = -50$ dB					0.9					MHz
Capacitance Input	C_{IS}	V_{DD} = +5V, $V_C = V_{SS}$ = −5V					8					pF
Output	C_{OS}	V_{DD} = +5V, $V_C = V_{SS}$ = −5V					8					pF
Feedthrough	C_{IOS}	V_{DD} = +5V, $V_C = V_{SS}$ = −5V					0.5					pF
Propagation Delay Signal Input to Signal Output	t_{pd}	$V_C = V_{DD}$ = +10V, V_{SS} = GND, C_L = 15 pF V_{is} = 10V (square wave) $t_r = t_f$ = 20 ns (input signal)					10					ns

electrical characteristics CD4066C Continued

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS									UNITS
			−40°C			25°C			85°C			
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
CONTROL (V_C)												
Noise Immunity	V_{NL}	$V_{is} \leq V_{DD}$ $V_{DD} - V_{SS} = 10V$ $I_{is} = 10 \mu A$	2			2	4.5		2			V
Input Current	I_C	$V_{DD} - V_{SS} = 10V$ $V_C \leq V_{DD} - V_{SS}$					±10					pA
Average Input Capacitance	C_C						5					pF
Crosstalk—Control Input to Signal Output		$R_L = 10\ k\Omega$ $V_{DD} - V_{SS} = 10V$ $V_C = 10V$ (square wave)					50					mV
Turn ON Propagation Delay	$t_{pd}C$	$t_{rc} = t_{fc} = 20$ ns $V_{is} < 10V$, $C_L = 15$ pF					35					ns
Maximum Allowable Control Input Repetition Rate		$R_L = 1\ k\Omega$, $V_{DD} = 10V$, V_{SS} = GND $C_L = 15$ pF $V_C = 10V$ (square wave) $t_r = t_f = 20$ ns					10					MHz

Note 1: The device should not be connected to circuits with the power on.

Note 2: Limit determined by minimum feasible leakage measurement for automatic testing.

Note 3: Symmetrical about 0V.

electrical characteristics CD4066M

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS									UNITS
			−55°C			25°C			125°C			
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Quiescent Dissipation per Package All Switches OFF	P_T	TERMINALS / VOLTS APPLIED V_{DD} 14 +10 V_{SS} 7 GND V_C 5, 6, 12, 13 GND V_{is} 1, 4, 8, 11 $\leq +10$ V_{os} 2, 3, 9, 10 $\leq +10$			5		0.1	5			300	μW
All Switches ON		TERMINALS / VOLTS APPLIED V_{DD} 14 +10 V_{SS} 7 GND V_C 5, 6, 12, 13 +10 $V_{is} = V_{os}$ 1, 4, 8, 11 $\leq +10$ (Thru 100Ω)			5		0.1	5			300	μW
SIGNAL INPUTS (V_{is}) AND OUTPUTS (V_{os})												
ON Resistance	R_{ON}	$R_L = 10\ k\Omega$ $V_C=V_{DD}$ V_S V_{is} +7.5V −7.5V −7.5V to +7.5V +15V 0V 0V to 15V		60	220		80	280		145	320	Ω
		+5V −5V −5V to +5V +10V 0V 0V to 10V		85	400		120	500		190	550	Ω
		+2.5V −2.5V −2.5V to +2.5V +5V 0V 0V to 5V		160	3000		270	5000		360	5500	Ω
ΔON Resistance Between Any 2 of 4 Switches	ΔR_{ON}	$R_L = 10\ k\Omega$ +7.5V −7.5V −7.5V to +7.5V +15V 0V 0V to 15V					5					Ω
		+5V −5V −5V to +5V +10V 0V 0V to 10V					10					Ω
Sine Wave Response (Distortion)		$R_L = 10\ k\Omega$ +5V −5V 5V(p-p) $f_{is} = 1$ kHz (Note 3)					0.4					%
Input or Output Leakage—Switch OFF (Effective OFF Resistance)		$V_C=V_{SS}$ V_{DD} V_{is} −7.5V +7.5V +7.5V −7.5V +7.5V −7.5V (Note 2)			±100		±0.1	±100			±500	nA
		−5V +5V +5V −5V +5V −5V (Note 2)			±100		±0.01	±100			±500	nA
Frequency Response—Switch ON (Sine Wave Input)		$V_C = V_{DD} = +5V$, $V_{SS} = -5V$ $R_L = 1\ k\Omega$ $V_{is} = 5V$ (p-p) $20\ \text{Log}_{10} \frac{V_{os}}{V_{is}} = -3$ dB					40					MHz
Feedthrough Switch OFF		$V_{DD} = +5V$, $V_C = V_{SS} = -5V$ $20\ \text{Log}_{10} \frac{V_{os}}{V_{is}} = -50$ dB					1.25					MHz

electrical characteristics CD4066M Continued

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS									UNITS
			−55°C			25°C			125°C			
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Crosstalk Between Any 2 of the 4 Switches (Frequency at −50 dB)		$V_C(A) = V_{DD} = +5V$ $R_L = 1\ k\Omega$ $V_C(B) = V_{SS} = -5V$ $V_{is}(A) = 5V(p\text{-}p)$ $20 \text{ Log}_{10} \frac{V_{os}(B)}{V_{is}(A)} = -50\ dB$					0.9					MHz
Capacitance												
Input	C_{IS}	$V_{DD} = +5V, V_C = V_{SS} = -5V$					8					pF
Output	C_{OS}	$V_{DD} = +5V, V_C = V_{SS} = -5V$					8					pF
Feedthrough	C_{IOS}	$V_{DD} = +5V, V_C = V_{SS} = -5V$					0.5					pF
Propagation Delay Signal Input to Signal Output	t_{pd}	$V_C = V_{DD} = +10V, V_{SS} = GND, C_L = 15\ pF$ $V_{is} = 10V$ (square wave) $t_r = t_f = 20\ ns$ (input signal)					10					ns
CONTROL (V_C)												
Noise Immunity	V_{NL}	$V_{is} \leq V_{DD}$ $V_{DD} - V_{SS} = 10V$ $I_{is} = 10\mu A$	2			2	4.5		2			V
Input Current	I_C	$V_{DD} - V_{SS} = 10V$ $V_C \leq V_{DD} - V_{SS}$					±10					pA
Average Input Capacitance	C_C						5					pF
Crosstalk—Control Input to Signal Output		$V_{DD} - V_{SS} = 10V$ $R_L = 10\ k\Omega$ $V_C = 10V$ (square wave)					50					mV
Turn ON Propagation Delay	$t_{pd}C$	$t_{rc} = t_{fc} = 20\ ns$ $V_{is} \leq 10V, C_L = 15\ pF$					35					ns
Maximum Allowable Control Input Repetition Rate		$V_{DD} = 10V, V_{SS} = GND, R_L = 1\ k\Omega$ $C_L = 15\ pF$ $V_C = 10V$ (square wave) $t_r = t_f = 20\ ns$					10					MHz

Note 1: The device should not be connected to circuits with the power on.

Note 2: Limit determined by minimum feasible leakage measurement for automatic testing.

Note 3: Symmetrical about 0V.

special considerations

In applications where separate power sources are used to drive V_{DD} and the signal input, the V_{DD} current capability should exceed V_{DD}/R_L (R_L = effective external load of the 4 CD4066M/CD4066C bilateral switches). This provision avoids any permanent current flow or clamp action on the V_{DD} supply when power is applied or removed from CD4066M/CD4066C.

In certain applications, the external load-resistor current may include both V_{DD} and signal-line components. To avoid drawing V_{DD} current when switch current flows into terminals 1, 4, 8 or 11, the voltage drop across the bidirectional switch must not exceed 0.8V at $T_A \leq 25°C$, or 0.6V at $T_A > 25°C$ (calculated from R_{ON} values shown).

No V_{DD} current will flow through R_L if the switch current flows into terminals 2, 3, 9 or 10.

CD4069BM/CD4069BC hex inverters

(See MM74C04 Data Sheet) Page Number 1

CD4070BM/CD4070BC quad EXCLUSIVE-OR gate

(See MM74C86 Data Sheet) Page Number 5

CD4076BM/CD4076BC TRI-STATE® quad D flip-flop

(See MM74C173 Data Sheet) Page Number 64

CD40106BM/CD40106BC hex schmitt trigger

(See MM74C14 Data Sheet) Page Number 8

CD40192BM/CD40192BC sync up/down decade counter

(See MM74C192 Data Sheet) Page Number 73

CD40193BM/CD40193BC sync up/down binary counter

(See MM74C193 Data Sheet) Page Number 73

CD4511BM/CD4511BC BCD-to-7 segment latch/decoder/driver

general description

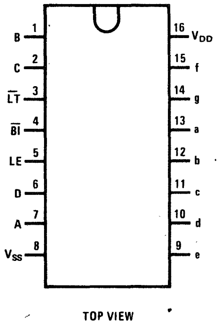
The CD4511BM/CD4511BC BCD-to-seven segment latch/decoder/driver is constructed with complementary MOS (CMOS) enhancement mode devices and NPN bipolar output drivers in a single monolithic structure. The circuit provides the functions of a 4-bit storage latch, an 8421 BCD-to-seven segment decoder, and an output drive capability. Lamp test (LT), blanking (BI), and latch enable (LE) inputs are used to test the display, to turn-off or pulse modulate the brightness of the display, and to store a BCD code, respectively. It can be used with seven-segment light emitting diodes (LED), incandescent, fluorescent, gas discharge, or liquid crystal readouts either directly or indirectly.

Applications include instrument (e.g., counter, DVM, etc.) display driver, computer/calculator display driver, cockpit display driver, and various clock, watch, and timer uses.

features

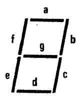
- Low logic circuit power dissipation
- High current sourcing outputs (up to 25 mA)
- Latch storage of code
- Blanking input
- Lamp test provision
- Readout blanking on all illegal input combinations
- Lamp intensity modulation capability
- Time share (multiplexing) facility
- Equivalent to Motorola MC14511

connection diagram



Display

Segment Identification



truth table

INPUTS							OUTPUTS							
LE	$\overline{BI}$	$\overline{LT}$	D	C	B	A	a	b	c	d	e	f	g	DISPLAY
X	X	0	X	X	X	X	1	1	1	1	1	1	1	8
X	0	1	X	X	X	X	0	0	0	0	0	0	0	
0	1	1	0	0	0	0	1	1	1	1	1	1	0	0
0	1	1	0	0	0	1	0	1	1	0	0	0	0	1
0	1	1	0	0	1	0	1	1	0	1	1	0	1	2
0	1	1	0	0	1	1	1	1	1	1	0	0	1	3
0	1	1	0	1	0	0	0	1	1	0	0	1	1	4
0	1	1	0	1	0	1	1	0	1	1	0	1	1	5
0	1	1	0	1	1	0	0	0	1	1	1	1	1	6
0	1	1	0	1	1	1	1	1	1	0	0	0	0	7
0	1	1	1	0	0	0	1	1	1	1	1	1	1	8
0	1	1	1	0	0	1	1	1	1	0	0	1	1	9
0	1	1	1	0	1	0	0	0	0	0	0	0	0	
0	1	1	1	0	1	1	0	0	0	0	0	0	0	
0	1	1	1	1	0	0	0	0	0	0	0	0	0	
0	1	1	1	1	0	1	0	0	0	0	0	0	0	
0	1	1	1	1	1	0	0	0	0	0	0	0	0	
0	1	1	1	1	1	1	0	0	0	0	0	0	0	
1	1	1	X	X	X	X				*				*

X = Don't care

*Depends upon the BCD code applied during the 0 to 1 transition of LE.

absolute maximum ratings

Voltage at Any Pin (Note 1)	V_{SS} − 0.3V to V_{DD} + 0.3V
Operating Temperature Range	
CD4511BM	−55°C to +125°C
CD4511BC	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500 mW
Operating V_{DD} Range	V_{SS} + 3V to V_{SS} + 15V
Lead Temperature (Soldering, 10 seconds)	300°C

dc electrical characteristics CD4511BM

PARAMETER	CONDITIONS	−55°C			+25°C			+125°C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Output Voltage Logical "0" Level (V_{OUT})	V_{DD} = 5V			0.01		0	0.01			0.05	V
	V_{DD} = 10V			0.01		0	0.01			0.05	V
	V_{DD} = 15V					0					V
Output Voltage Logical "1" Level (V_{OUT})	V_{DD} = 5V	4.1			4.1	4.57		4.1			V
	V_{DD} = 10V	9.1			9.1	9.58		9.1			V
	V_{DD} = 15V					14.59					V
Noise Immunity (V_{NL})	V_{DD} = 5V, $V_{OUT} \geq 3.5V$	1.5			1.5	2.25		1.4			V
	V_{DD} = 10V, $V_{OUT} \geq 7V$	3.0			3.0	4.5		2.9			V
	V_{DD} = 15V, $V_{OUT} \geq 10.5V$					6.75					V
Noise Immunity (V_{NH})	V_{DD} = 5V, $V_{OUT} \leq 1.5V$	1.4			1.5	2.25		1.5			V
	V_{DD} = 10V, $V_{OUT} \leq 3V$	2.9			3.0	4.5		3.0			V
	V_{DD} = 15V, $V_{OUT} \leq 4.5V$					6.75					V
Output (Source) Drive Voltage (V_{OH})	V_{DD} = 5V, I_{OH} = 0 mA				4.1	4.57					V
	V_{DD} = 5V, I_{OH} = 5 mA					4.24					V
	V_{DD} = 5V, I_{OH} = 10 mA				3.9	4.12					V
	V_{DD} = 5V, I_{OH} = 15 mA					3.94					V
	V_{DD} = 5V, I_{OH} = 20 mA				3.4	3.75					V
	V_{DD} = 5V, I_{OH} = 25 mA					3.54					V
	V_{DD} = 10V, I_{OH} = 0 mA				9.1	9.58					V
	V_{DD} = 10V, I_{OH} = 5 mA					9.26					V
	V_{DD} = 10V, I_{OH} = 10 mA				9.0	9.17					V
	V_{DD} = 10V, I_{OH} = 15 mA					9.04					V
	V_{DD} = 10V, I_{OH} = 20 mA				8.6	8.9					V
	V_{DD} = 10V, I_{OH} = 25 mA					8.75					V
	V_{DD} = 15V, I_{OH} = 0 mA					14.59					V
	V_{DD} = 15V, I_{OH} = 5 mA					14.27					V
	V_{DD} = 15V, I_{OH} = 10 mA					14.18					V
	V_{DD} = 15V, I_{OH} = 15 mA					14.07					V
	V_{DD} = 15V, I_{OH} = 20 mA					13.95					V
	V_{DD} = 15V, I_{OH} = 25 mA					13.8					V
Output (Sink) Drive Voltage (I_{OL})	V_{DD} = 5V, V_{OL} = 0.4V	0.5			0.4	0.78		0.28			mA
	V_{DD} = 10V, V_{OL} = 0.5V	1.1			0.9	2.0		0.65			mA
	V_{DD} = 15V, V_{OL} = 1.5V					7.8					mA
Input Current (I_{IN})						10					pA

Note 1: Devices should not be connected with power on.

dc electrical characteristics CD4511BC

PARAMETER	CONDITIONS	−40°C			+25°C			+85°C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Output Voltage Logical "0" Level (V_{OUT})	V_{DD} = 5V			0.01		0	0.01			0.05	V
	V_{DD} = 10V			0.01		0	0.01			0.05	V
	V_{DD} = 15V					0					V
Output Voltage Logical "1" Level (V_{OUT})	V_{DD} = 5V	4.1			4.1	4.57		4.1			V
	V_{DD} = 10V	9.1			9.1	9.58		9.1			V
	V_{DD} = 15V					14.59					V
Noise Immunity (V_{NL})	V_{DD} = 5V, $V_{OUT} \geq 3.5V$	1.5			1.5	2.25		1.4			V
	V_{DD} = 10V, $V_{OUT} \geq 7V$	3.0			3.0	4.5		2.9			V
	V_{DD} = 15V, $V_{OUT} \geq 10.5V$					6.75					V
Noise Immunity (V_{NH})	V_{DD} = 5V, $V_{OUT} \leq 1.5V$	1.4			1.5	2.25		1.5			V
	V_{DD} = 10V, $V_{OUT} \leq 3V$	2.9			3.0	4.5		3.0			V
	V_{DD} = 15V, $V_{OUT} \leq 4.5V$					6.75					V
Output (Source) Drive Voltage (V_{OH})	V_{DD} = 5V, I_{OH} = 0 mA				4.1	4.57					V
	V_{DD} = 5V, I_{OH} = 5 mA					4.24					V
	V_{DD} = 5V, I_{OH} = 10 mA				3.6	4.12					V
	V_{DD} = 5V, I_{OH} = 15 mA					3.94					V
	V_{DD} = 5V, I_{OH} = 20 mA				2.8	3.75					V
	V_{DD} = 5V, I_{OH} = 25 mA					3.54					V
	V_{DD} = 10V, I_{OH} = 0 mA				9.1	9.58					V
	V_{DD} = 10V, I_{OH} = 5 mA					9.26					V
	V_{DD} = 10V, I_{OH} = 10 mA				8.75	9.17					V
	V_{DD} = 10V, I_{OH} = 15 mA					9.04					V
	V_{DD} = 10V, I_{OH} = 20 mA				8.1	8.9					V
	V_{DD} = 10V, I_{OH} = 25 mA					8.75					V
	V_{DD} = 15V, I_{OH} = 0 mA					14.59					V
	V_{DD} = 15V, I_{OH} = 5 mA					14.27					V
	V_{DD} = 15V, I_{OH} = 10 mA					14.18					V
	V_{DD} = 15V, I_{OH} = 15 mA					14.07					V
	V_{DD} = 15V, I_{OH} = 20 mA					13.95					V
	V_{DD} = 15V, I_{OH} = 25 mA					13.8					V
Output (Sink) Drive Voltage (I_{OL})	V_{DD} = 5V, V_{OL} = 0.4V	0.23			0.2	0.78			0.16		mA
	V_{DD} = 10V, V_{OL} = 0.5V	0.6			0.5	2.0			0.4		mA
	V_{DD} = 15V, V_{OL} = 1.5V					7.8					mA
Input Current (I_{IN})						10					pA

ac electrical characteristics

$T_A = 25°C$ and $C_L = 15$ pF, typical temperature coefficient for all values of $V_{DD} = 0.3\%/°C$

PARAMETER	CONDITIONS	CD4511BM			CD4511BC			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Capacitance (C_{IN})	$V_{IN} = 0$		5.0			5.0		pF
Output Rise Time (t_r) (*Figure 1a*)	$V_{DD} = 5.0V$		30	175		30	200	ns
	$V_{DD} = 10V$		17	75		17	110	ns
	$V_{DD} = 15V$		15			15		ns
Output Fall Time (t_f) (*Figure 1a*)	$V_{DD} = 5.0V$		1000			1000		ns
	$V_{DD} = 10V$		1000			1000		ns
	$V_{DD} = 15V$		1000			1000		ns
Turn-Off Delay Time (Data) (t_{PLH}) (*Figure 1a*)	$V_{DD} = 5.0V$		640	1500		640	2250	ns
	$V_{DD} = 10V$		250	600		250	900	ns
	$V_{DD} = 15V$		175			175		ns
Turn-On Delay Time (Data) (t_{PHL}) (*Figure 1a*)	$V_{DD} = 5.0V$		720	1500		720	2250	ns
	$V_{DD} = 10V$		290	600		290	900	ns
	$V_{DD} = 15V$		195			195		ns
Turn-Off Delay Time (Blank) (t_{PLH}) (*Figure 1a*)	$V_{DD} = 5.0V$		320	1000		320	1500	ns
	$V_{DD} = 10V$		130	400		130	600	ns
	$V_{DD} = 15V$		100			100		ns
Turn-On Delay Time (Blank) (t_{PHL}) (*Figure 1a*)	$V_{DD} = 5.0V$		485	1000		485	1500	ns
	$V_{DD} = 10V$		200	400		200	600	ns
	$V_{DD} = 15V$		160			160		ns
Turn-Off Delay Time (Lamp Test) (t_{PHL}) (*Figure 1a*)	$V_{DD} = 5.0V$		290	625		290	940	ns
	$V_{DD} = 10V$		125	250		125	375	ns
	$V_{DD} = 15V$		85			85		ns
Turn-On Delay Time (Lamp Test) (t_{PHL}) (*Figure 1a*)	$V_{DD} = 5.0V$		290	625		290	940	ns
	$V_{DD} = 10V$		120	250		120	375	ns
	$V_{DD} = 15V$		90			90		ns
Setup Time (t_{SETUP}) (*Figure 1b*)	$V_{DD} = 5.0V$	180	90		270	90		ns
	$V_{DD} = 10V$	76	38		114	38		ns
	$V_{DD} = 15V$		20			20		ns
Hold Time (t_{HOLD}) (*Figure 1b*)	$V_{DD} = 5.0V$	0	−90		90	−90		ns
	$V_{DD} = 10V$	0	−38		38	−38		ns
	$V_{DD} = 15V$		−20			−20		ns
Minimum Latch Enable Pulse Width (PW_{LE}) (*Figure 1c*)	$V_{DD} = 5.0V$	520	260		780	260		ns
	$V_{DD} = 10V$	220	110		330	110		ns
	$V_{DD} = 15V$		65			65		ns

switching time waveforms

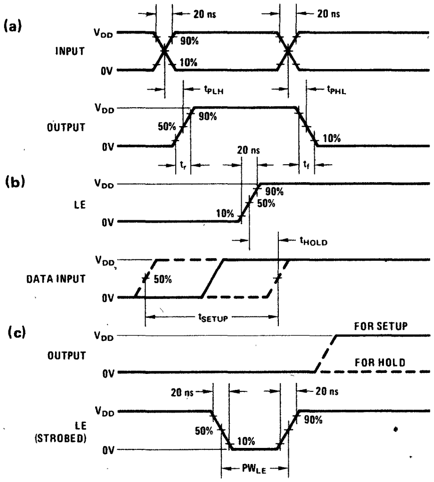
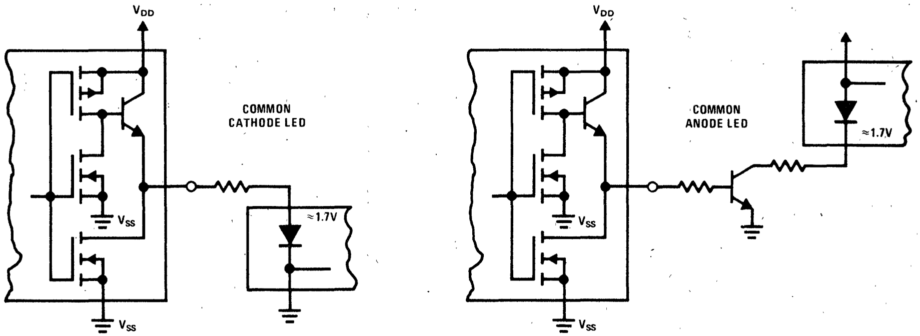


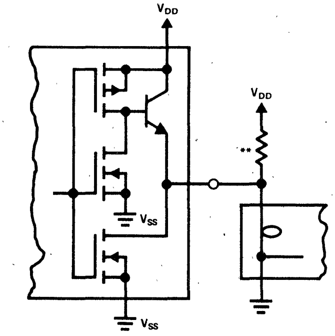
FIGURE 1.

typical applications

Light Emitting Diode (LED) Readout

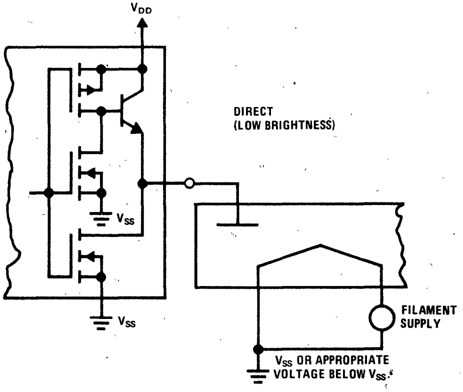


Incandescent Readout

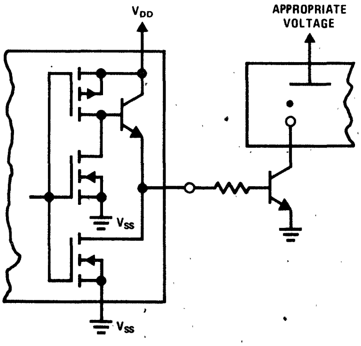


**A filament pre-warm resistor is recommended to reduce filament thermal shock and increase the effective cold resistance of the filament.

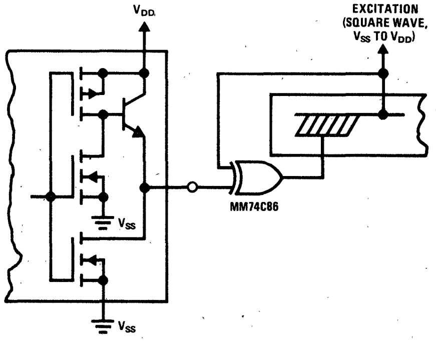
Flourescent Readout



Gas Discharge Readout



Liquid Crystal (LC) Readout



Direct dc drive of LC's not recommended for life of LC readouts.

Stephen Calebotta
National Semiconductor

CMOS, THE IDEAL LOGIC FAMILY

INTRODUCTION

Let's talk about the characteristics of an ideal logic family. It should dissipate no power, have zero propagation delay, controlled rise and fall times, and have noise immunity equal to 50% of the logic swing.

Well, that ideal logic family is here — almost. The properties of CMOS (complementary MOS) begin to approach these ideal characteristics.

First, CMOS dissipates low power. Typically, the static power dissipation is 10 nW per gate which is due to the flow of leakage currents. The active power depends on power supply voltage, frequency, output load and input rise time, but typically, gate dissipation at 1MHz with a 50 pF load is less than 10mW.

Second, the propagation delays through CMOS are short, though not quite zero. Depending on power supply voltage, the delay through a typical gate is on the order of 25 to 50 ns.

Third, rise and fall times are controlled, tending to be ramps rather than step functions. Typically, rise and fall times tend to be 20 to 40% longer than the propagation delays.

Last, but not least, the noise immunity approaches 50%, being typically 45% of the full logic swing.

Besides the fact that it approaches the characteristics of an ideal logic family and besides the obvious low power battery applications, why should designers choose CMOS for new systems? The answer is cost.

On a component basis, CMOS is still more expensive than TTL. However, system level cost may be lower. The power supplies in a CMOS system will be cheaper since they can be made smaller and with less regulation. Because of lower currents, the power supply distribution system can be simpler and therefore, cheaper. Fans and other cooling equipment are not needed due to the lower dissipation. Because of longer rise and fall times, the transmission of digital signals becomes simpler making transmission techniques less expensive. Finally, there is no technical reason why CMOS prices cannot approach present day TTL prices as sales volume and manufacturing experience increase. So, an engineer about to start a new design should compare the system level cost of using CMOS or some other logic family. He may find that, even at today's prices, CMOS is the most economical choice.

National is building two lines of CMOS. The first is a number of parts of the CD4000A series. The second is the 54C/74C series which National introduced and which will become the industry standard in the near future.

The 54C/74C line consists of CMOS parts which are pin and functional equivalents of many of the most popular parts in the 7400 TTL series. This line is typically 50% faster than the 4000A series and sinks 50% more current. For ease of design, it is spec'd at TTL levels as well as CMOS levels, and there are two temperature ranges available: 54C, −55°C to +125°C or 74C, −40°C to +85°C. Table 1 compares the port parameters of the 54C/74C CMOS line to those of the 54L/74L low power TTL line.

TABLE 1. Comparison of 54L/74L Low Power TTL and 54C/74C CMOS Port Parameters.

FAMILY	V_{CC}	V_{IL} MAX	I_{IL} MAX	V_{IH} MIN	I_{IH} 2.4V	V_{OL} MAX	I_{OL}	V_{OH} MIN	I_{OH}	t_{pd0} TYP	t_{pd1} TYP	P_{DISS}/GATE STATIC	P_{DISS}/GATE 1 MHz, 50 pF LOAD
54L/74L	5	0.7	0.18 mA	2.0	10 μA	0.3	2.0 mA	2.4	100μA	31	35	1 mW	2.25 mW
54C/74C	5	0.8	–	3.5	–	0.4	*360μA	2.4	*100μA	60	45	0.00001 mW	1.25 mW
54C/74C	10	2.0	–	8.0	–	1.0	**10μA	9.0	**10μA	25	30	0.00003 mW	5 mW

*Assumes interfacing to low power TTL.
**Assumes interfacing to CMOS.

CHARACTERISTICS OF CMOS

The aim of this section is to give the system designer not familiar with CMOS, a good feel for how it works and how it behaves in a system. Much has been written about MOS devices in general. Therefore, we will not discuss the design and fabrication of CMOS transistors and circuits.

The basic CMOS circuit is the inverter shown in Figure 2-1. It consists of two MOS enhancement mode transistors, the upper a P-channel type, the lower an N-channel type.

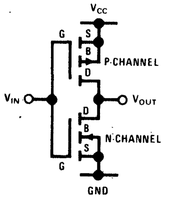


FIGURE 2-1. Basic CMOS Inverter.

The power supplies for CMOS are called V_{DD} and V_{SS}, or V_{CC} and Ground depending on the manufacturer. V_{DD} and V_{SS} are carryovers from conventional MOS circuits and stand for the drain and source supplies. These do not apply directly to CMOS since both supplies are really source supplies. V_{CC} and Ground are carryovers from TTL logic and that nomeclature has been retained with the introduction of the 54C/74C line of CMOS. V_{CC} and Ground is the nomenclature we shall use throughout this paper.

The logic levels in a CMOS system are V_{CC} (logic "1") and Ground (logic "0"). Since "on" MOS transistor has virtually no voltage drop across it if there is no current flowing through it, and since the input impedance to CMOS device is so high (the input characteristic of an MOS transistor is essentially capacitive, looking like a $10^{12}\Omega$ resistor shunted by a 5 pF capacitor), the logic levels seen in a CMOS system will be essentially equal to the power supplies.

Now let's look at the characteristic curves of MOS transistors to get an idea of how rise and fall times, propagation delays and power dissipation will vary with power supply voltage and capacitive loading. Figure 2-2 shows the characteristic curves of N-channel and P-channel enhancement mode transistors.

There are a number of important observations to be made from these curves. Refer to the curve of V_{GS} = 15V (Gate to Source Voltage) for the N-channel transistor. Note that for a constant drive voltage V_{GS}, the transistor behaves like a current source for V_{DS}'s (Drain to Source Voltage) greater than $V_{GS} - V_T$ (V_T is the threshold voltage of an MOS transistor). For V_{DS}'s below $V_{GS} - V_T$, the transistor behaves essentially like a resistor. Note also that for lower V_{GS}'s, there are similar curves except that the magnitude of the I_{DS}'s are significantly smaller and that in fact, I_{DS} increases approximately as the square of increasing V_{GS}. The P-channel transistor exhibits essentially identical, but complemented, characteristics.

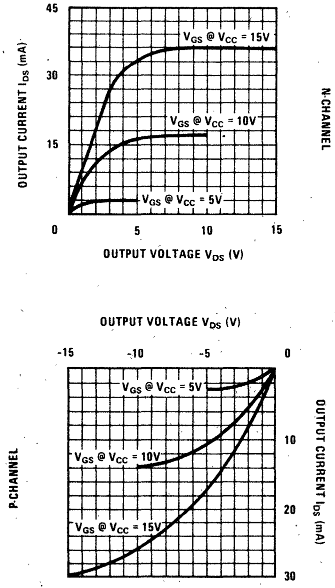


FIGURE 2-2. Logical "1" Output Voltage vs Source Current.

If we try to drive a capacitive load with these devices, we can see that the initial voltage change across the load will be ramp-like due to the current source characteristic followed by a rounding off due to the resistive characteristic dominating as V_{DS} approaches zero. Referring this to our basic CMOS inverter in Figure 2-1, as V_{DS} approaches zero, V_{OUT} will approach V_{CC} or Ground depending on whether the P-channel or N-channel transistor is conducting.

Now if we increase V_{CC} and, therefore, V_{GS} the inverter must drive the capacitor through a larger voltage swing. However, for this same voltage increase, the drive capability (I_{DS}) has increased roughly as the square of V_{GS} and, therefore, the rise times and the propagation delays through the inverter as measured in Figure 2-3 have decreased.

So, we can see that for a given design, and therefore fixed capacitive load, increasing the power supply voltage will increase the speed of the system.

Increasing V_{CC} increases speed but it also increases power dissipation. This is true for two reasons. First, CV^2f power increases. This is the power dissipated in a CMOS circuit, or any other circuit for that matter, when driving a capacitive load.

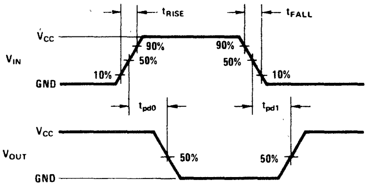
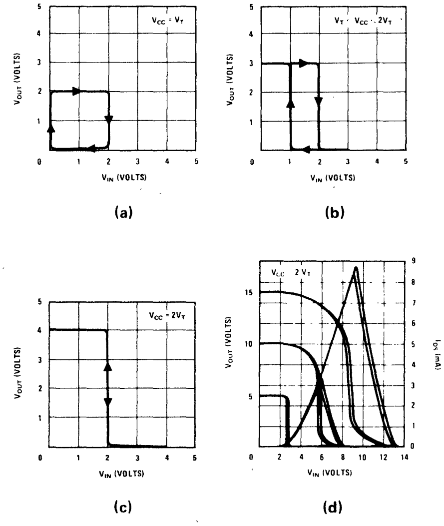


FIGURE 2-3. Rise and Fall Times and Propagation Delays as Measured in a CMOS System.

For a given capacitive load and switching frequency, power dissipation increases as the square of the voltage change across the load.

The second reason is that the VI power dissipated in the CMOS circuit increases with V_{CC} (for V_{CC}'s $> 2V_T$). Each time the circuit switches, a current momentarily flows from V_{CC} to Ground through both output transistors. Since the threshold voltages of the transistors do not change with increasing V_{CC}, the input voltage range through which the upper and lower transistors are conducting simultaneously increases as V_{CC} increases. At the same time, the higher V_{CC} provides higher V_{GS} voltages which also increase the magnitude of the I_{DS} currents. Incidently, if the rise time of the input signal was zero, there would be no current flow from V_{CC} to Ground through the circuit. This current flows because the input signal has a finite rise time and, therefore, the input voltage spends a finite amount of time passing through the region where both transistors conduct simultaneously. Obviously, input rise and fall times should be kept to a minimum to minimize VI power dissipation.

Let's look at the transfer characteristics, Figure 2-4, as they vary with V_{CC}. For the purposes of this discussion we will assume that both transistors in our basic inverter have identical but complementary characteristics and threshold voltages. Assume the threshold voltages, V_T, to be 2V. If V_{CC} is less than the threshold voltage of 2V, neither transistor can ever be turned on and the circuit cannot operate. If V_{CC} is equal to the threshold voltage exactly then we are on the curve Figure 2-4a. We appear to have 100% hysteresis. However, it is not truly hysteresis since both output transistors are off and the output voltage is being held on the gate capacitances of succeeding circuits. If V_{CC} is somewhere between one and two threshold voltages (Figure 2-4b), then we have diminishing amounts of "hysteresis" as we approach V_{CC} equal to $2V_T$ (Figure 2-4c). At V_{CC} equal to two thresholds we have no "hysteresis" and no current flow through both the upper and lower transistors during switching. As V_{CC} exceeds two thresholds the transfer curves begin to round off (Figure 2-4d). As V_{IN} passes through the region where both transistors are conducting, the currents flowing through the transistors cause voltage drops across them giving the rounded characteristic.



(a)

(b)

(c)

(d)

FIGURE 2-4. Transfer Characteristics vs V_{CC}.

Considering the subject of noise in a CMOS system, we must discuss at least two specs: noise immunity and noise margin.

National's CMOS circuits have a typical noise immunity of 0.45 V_{CC}. This means that a spurious input which is 0.45 V_{CC} or less away from V_{CC} or Ground typically will not propagate through the system as an erroneous logic level. This does not mean that no signal at all will appear at the output of the first circuit. In fact, there will be an output signal as a result of the spurious input, but it will be reduced in amplitude. As this signal propagates through the system, it will be attenuated even more by each circuit it passes through until it finally disappears. Typically, it will not change any signal to the opposite logic level. In a typical flip flop, a 0.45 V_{CC} spurious pulse on the clock line would not cause the flop to change state.

National also guarantees that its CMOS circuits have a 1V DC noise margin over the full power supply range and temperature range and with any combination of inputs. This is simply a variation of the noise immunity spec only now a specific set of input and output voltages have been selected and guaranteed. Stated verbally, the spec says that for the output of a circuit to be within 0.1 V_{CC} volts of a proper logic level (V_{CC} or Ground), the input can be as much as 0.1 V_{CC} plus 1V away from power supply rail. Shown graphically we have:

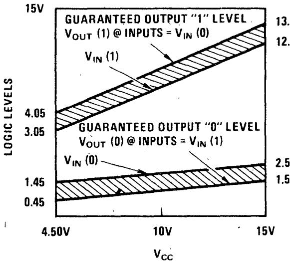


FIGURE 2-5. Guaranteed CMOS DC Margin Over Temperature as a Function of V_{CC}. CMOS Guarantees 1V.

This is similar in nature to the standard TTL noise margin spec which is 0.4V.

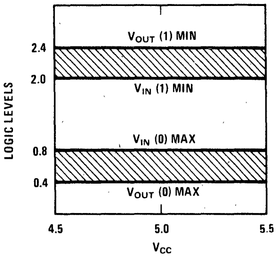


FIGURE 2-6. Guaranteed TTL DC Margin Over Temperature as a Function of V_{CC}. TTL Guarantees 0.4V.

For a complete picture of V_{OUT} vs V_{IN} refer to the transfer characteristic curves in Figure 2-4.

SYSTEM CONSIDERATIONS

This section describes how to handle many of the situations that arise in normal system design such as unused inputs, paralleling circuits for extra drive, data bussing, power considerations and interfaces to other logic families.

Unused inputs: simply stated, unused inputs should not be left open. Because of the very high impedance ($\sim 10^{12}\Omega$), a floating input may drift back and forth between a "0" and "1" creating some very intriguing system problems. All unused inputs should be tied to V_{CC}, Ground or another used input. The choice is not completely arbitrary, however, since there will be an effect on the output drive capability of the circuit in question. Take, for example, a four input NAND gate being used as a two input gate. The internal structure is shown in Figure 3-1. Let inputs A & B be the unused inputs.

If we were going to tie the unused inputs to a logic level, inputs A & B would have to be tied to V_{CC} to enable the other inputs to function. That would turn on the lower A and B transistors and turn off the upper A and B transistors. At most, only two of the upper transistors could ever be turned on. However, if inputs A and B were tied to input C, the input capacitance would triple, but each time C went low, the upper A, B and C transistors would turn on, tripling the available source current. If input D was low also, all four of the upper transistors would be on.

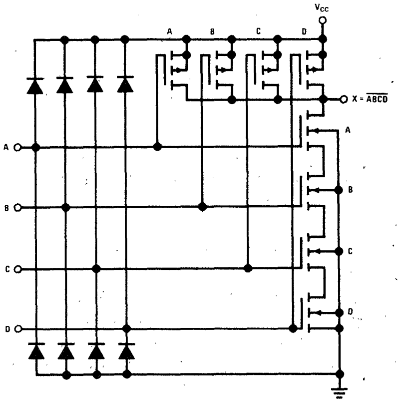


FIGURE 3-1. MM74C20 Four Input NAND Gate.

So, tying unused NAND gate inputs to V_{CC} (Ground for NOR gates) will enable them, but tying unused inputs to other used inputs guarantees an increase in source current in the case of NAND gates (sink current in the case of NOR gates). There is no increase in drive possible through the series transistors. By using this approach, a multiple input gate could be used to drive a heavy current load such as a lamp or a relay.

Parallel gates: depending on the type of gate, tying inputs together guarantees an increase in either source or sink current but not both. To guarantee an increase in both currents, a number of gates must be paralleled as in Figure 3-2. This insures that there are a number of parallel combinations of the series string of transistors (Figure 3-1), thereby increasing drive in that direction also.

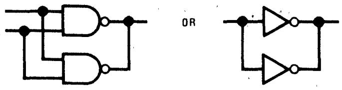
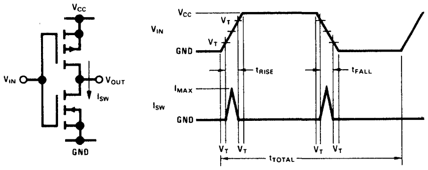


FIGURE 3-2. Paralleling Gates or Inverters Increases Output Drive in Both Directions.

Data bussing: there are essentially two ways to do this. First, connect ordinary CMOS parts to a bus using transfer gates (part no. CD4016C). Second, and the preferred way, is to use parts specifically designed with a CMOS equivalent of a TRI-STATE® output.

Power supply filtering: since CMOS can operate over a large range of power supply voltages (3V to 15V), the filtering necessary is minimal. The minimum power supply voltage required will be determined by the maximum frequency of operation of the fastest element in the system (usually only a very small portion of any system operates at maximum frequency). The filtering should be designed to keep the power supply voltage somewhere between this minimum voltage and the maximum rated voltage the parts can tolerate. However, if power dissipation is to be kept to a minimum, the power supply voltage should be kept as low as possible while still meeting all speed requirements.

Minimizing system power dissipation: to minimize power consumption in a given system, it should be run at the minimum speed to do the job with the lowest possible power supply voltage. AC and DC transient power consumption both increase with frequency and power supply voltage. The AC power is described as CV^2f power. This is the power dissipated in a driver driving a capacitive load. Obviously, AC power consumption increases directly with frequency and as the square of the power supply. It also increases with capacitive load, but this is usually defined by the system and is not alterable. The DC power is the VI power dissipated during switching. In any CMOS device during switching, there is a momentary current path from the power supply to ground, (when $V_{CC} > 2V_T$) Figure 3-3.



VI POWER IS GIVEN BY:

$$P_{VI} = V_{CC} \times \frac{1}{2} I_{MAX} \times \text{RISE TIME TO PERIOD RATIO}$$

$$\text{RISE TIME TO PERIOD RATIO} = \frac{V_{CC} - 2V_T}{V_{CC}} \times \frac{t_{RISE} + t_{FALL}}{t_{TOTAL}}$$

$$\text{WHERE } \frac{1}{t_{TOTAL}} = \text{FREQUENCY}$$

$$P_{VI} = 1/2\,(V_{CC} - 2V_T)\, I_{CC\,MAX}\, (t_{RISE} + t_{FALL})\text{ FREQ.}$$

FIGURE 3-3. DC Transient Power.

The maximum amplitude of the current is a rapidly increasing function of the input voltage which in turn is a direct function of the power supply voltage. See Figure 2-4d.

The actual amount of VI power dissipated by the system is determined by three things: power supply voltage, frequency and input signal rise time. A very important factor is the input rise time. If the rise time is long, power dissipation increases since the current path is established for the entire period that the input signal is passing through the region between the threshold voltages of the upper and lower transistors. Theoretically, if the rise time were zero, no current path would be established and the VI power would be zero. However, with a finite rise time there is always some current flow and this current flow increases rapidly with power supply voltage.

Just a thought about rise time and power dissipation. If a circuit is used to drive many loads, its output rise time will suffer. This will result in an increase in VI power dissipation in every device being driven by that circuit (but not in the drive circuit itself). If power consumption is critical, it may be necessary to improve the rise time of that circuit by buffering or by dividing the loads in order to reduce overall power consumption.

So, to summarize the effects of power supply voltage, input voltage, input rise time and output load capacitance on system power dissipation, we can say the following:

1. **Power supply voltage:** CV^2f power dissipation increases as the square of power supply voltage. VI power dissipation increases approximately as the square of the power supply voltage.
2. **Input voltage level:** VI power dissipation increases if the input voltage lies somewhere between Ground plus a threshold voltage and V_{CC} minus a threshold voltage. The highest power dissipation occurs when V_{IN} is at 1/2 V_{CC}. CV^2f dissipation is unaffected.
3. **Input rise time:** VI power dissipation increases with longer rise times since the DC current path through the device is established for a longer period. The CV^2f power is unaffected by slow input rise times.
4. **Output load capacitance:** the CV^2f power dissipated in a circuit increases directly with load capacitance. VI power in a circuit is unaffected by its output load capacitance. However, increasing output load capacitance will slow down the output rise time of a circuit which in turn will affect the VI power dissipation in the devices it is driving.

INTERFACES TO OTHER LOGIC TYPES

There are two main ideas behind all of the following interfaces to CMOS. First, CMOS outputs should satisfy the current and voltage requirements of the other family's inputs. Second, and probably most important, the other family's outputs should swing as near as possible to the full voltage range of the CMOS power supplies.

P-Channel MOS: there are a number of things to watch for when interfacing CMOS and P-MOS. The first is the power supply set. Most of the more popular P-MOS parts are specified with 17 to 24V power supplies while the maximum power supply voltage for CMOS is 15V. Another problem is that unlike CMOS, the output swing of a push-pull P-MOS output is significantly less than the power supply voltage across it. P-MOS swings from very close to its more positive supply (V_{SS}) to quite a few volts above its more negative supply (V_{DD}). So, even if P-MOS uses a 15V or lower power supply set, its output swing will not go low enough for a reliable interface to CMOS. There are a number of ways to solve this problem depending on the configuration of the system. We will discuss two solutions for systems that are built totally with MOS and one solution for systems that include bipolar logic.

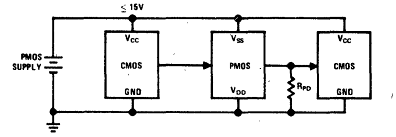
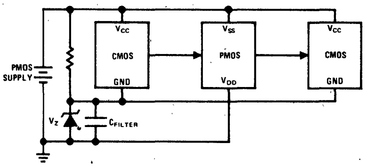


FIGURE 3-4. A One Power Supply System Built Entirely of CMOS and P-MOS.

First, MOS only. P-MOS and CMOS using the same power supply of less than 15V, Figure 3-4.

In this configuration CMOS drives P-MOS directly. However, P-MOS cannot drive CMOS directly because of its output will not pull down close enough to the lower power supply rail. R_{PD} (R pull down) is added to each P-MOS output to pull it all the way down to the lower rail. Its value is selected such that it is small enough to give the desired RC time constant when pulling down but not so small that the P-MOS output cannot pull it virtually all the way up to the upper power supply rail when it needs to. This approach will work with push-pull as well as open drain P-MOS outputs.

Another approach in a purely MOS system is to build a cheap zener supply to bias up the lower power supply rail of CMOS, Figure 3-5.

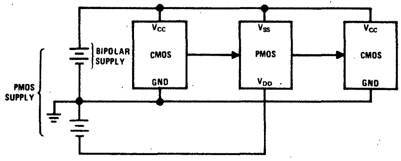


Use a bias supply to reduce the voltage across the CMOS to match the logic swing of the P-MOS. Make sure the resulting voltage across the CMOS is less than 15V.

FIGURE 3-5. A P-MOS and CMOS System Where The P-MOS Supply is Greater Than 15V.

In this configuration the P-MOS supply is selected to satisfy the P-MOS voltage requirement. The bias supply voltage is selected to reduce the total voltage across the CMOS (and therefore its logic swing) to match the minimum swing of the P-MOS outputs. The CMOS can still drive P-MOS directly and now the P-MOS can drive CMOS with no pull-down resistors. The other restrictions are that the total voltage across the CMOS is less than 15V and that the bias supply can handle the current requirements of all the CMOS. This approach is useful if the P-MOS supply must be greater than 15V and the CMOS current requirement is low enough to be done easily with a small discrete component regulator.

If the system has bipolar logic, it will usually have at least two power supplies. In this case, the CMOS is run off the bipolar supply and it interfaces directly to P-MOS, Figure 3-6.

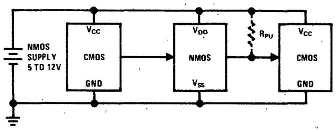


Run the CMOS from the bipolar supply and interface directly to P-MOS

FIGURE 3-6. A System With CMOS, P-MOS and Bipolar Logic.

N-Channel MOS: interfacing to N-MOS is somewhat simpler than interfacing to P-MOS although similar problems exist. First, N-MOS requires lower power supplies than P-MOS, being in the range of 5V to 12V. This is directly compatible with CMOS. Second, N-MOS logic levels range from slightly above the lower power supply rail to about 1 to 2V below the upper rail.

At the higher power supply voltages, N-MOS and CMOS can be interfaced directly since the N-MOS high logic level will be only about 10 to 20 percent below the upper rail. However, at lower supply voltages the N-MOS output level will be down 20 to 40 percent below the upper rail and something may have to be done to raise it. The simplest solution is to add pull up resistors on the N-MOS outputs as shown in Figure 3-7.



Both operate off same supply with pull up resistors optional from N-MOS to CMOS.

FIGURE 3-7. A System With CMOS and N-MOS Only.

TTL, LPTTL, DTL: two questions arise when interfacing bipolar logic families to CMOS. First, is the bipolar family's logic "1" output voltage high enough to drive CMOS directly?

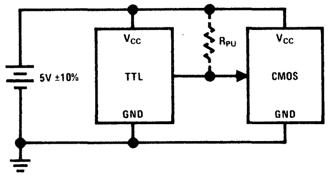
TTL, LPTTL, and DTL can drive 74C series CMOS directly over the commercial temperature range without external pull up resistors. However, TTL and LPTTL cannot drive 4000 series CMOS directly (DTL can) since 4000 series specs do not guarantee that a direct interface with no pull up resistors will operate properly.

DTL and LPTTL manufactured by National (NS LPTTL pulls up one diode drop higher than the LPTTL of other vendors) will also drive 74C directly over the entire military temperature range. LPTTL manufactured by other vendors and standard TTL will drive 74C directly over most of the mil temperature range. However, the TTL logic "1" drops to a somewhat marginal level toward the lower end of the mil temperature range and a pull up resistor is recommended.

According to the curve of DC margin vs V_{CC} for CMOS in Figure 2-5, if the CMOS sees an input voltage greater than $V_{CC} - 1.5V$ ($V_{CC} = 5V$), the output is guaranteed to be less than 0.5V from Ground. The next CMOS element will amplify this 0.5V level to the proper logic levels of V_{CC} or Ground. The standard TTL logic "1" spec is a V_{OUT} min. of 2.4V sourcing a current of 400μA. This is an extremely conservative spec since a TTL output will only approach a one level of 2.4V under the extreme worst case conditions of lowest temperature, high input voltage (0.8V), highest possible leakage currents (into succeeding TTL devices), and V_{CC} at the lowest allowable (V_{CC} = 4.5V).

Under nominal conditions (25°C, $V_{IN} = 0.4V$, nominal leakage currents into CMOS and V_{CC} = 5V) a TTL logic "1" will be more like $V_{CC} - 2V_D$, or $V_{CC} - 1.2V$. Varying only temperature, the output will change by two times −2mV per °C, or −4 mV per °C. $V_{CC} - 1.2V$ is more than enough to drive CMOS reliably without the use of a pull up resistor.

If the system is such that the TTL logic "1" output can drop below $V_{CC} - 1.5V$, use a pull up resistor to improve the logic "1" voltage into the CMOS.



Pull up resistor, R_{PU}, is needed only at the lower end of the Mil temperature range.

FIGURE 3-8. TTL to CMOS Interface.

The second question is, can CMOS sink the bipolar input current and not exceed the maximum value of the bipolar logic zero input voltage? The logic "1" input is no problem.

The LPTTL input current is small enough to allow CMOS to drive two loads directly. Normal power TTL input currents are ten times higher than those in LPTTL and consequently the CMOS output voltage will be well above the input logic "0" maximum of 0.8V. However, by carefully examining the CMOS output specs we will find that a two input NOR gate can drive one TTL load, albeit somewhat marginally. For example, the logical "0" output voltage for both an MM74C00 and MM74C02 over temperature is specified at 0.4V sinking 360μA (about 420μA at 25°C) with an input voltage of 4.0V and a V_{CC} of 4.75V. Both schematics are shown in Figure 3-9.

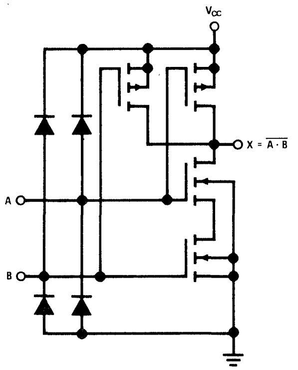


FIGURE 3-9a. MM74C00.

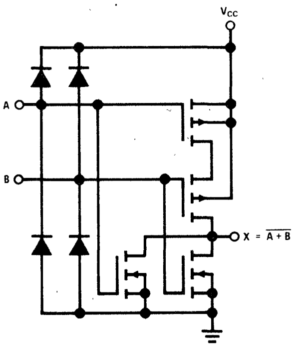


FIGURE 3-9b. MM74C02.

Both parts have the same current sinking spec but their structures are different. What this means is that either of the lower transistors in the MM74C02 can sink the same current as the two lower series transistors in the MM74C00. Both MM74C02 transistors together can sink twice the specified current for a given output voltage. If we allow the output voltage to go to 0.8V, then a MM74C02 can sink four times 360μA, or 1.44 mA which is nearly 1.6 mA. Actually, 1.6 mA is the maximum spec for the TTL input current and most TTL parts run at about 1 mA. Also, 360μA is the minimum CMOS sink current spec, the parts will really sink somewhere between 360 and 540μA (between 2 and 3 LPTTL input loads). The 360μA sink current is specified with an input voltage of 4.0V. With an input voltage of 5.0V, the sink current will be about 560μA over temperature, making it even easier to drive TTL. At room temperature with an input voltage of 5V, a CMOS output can sink about 800μA. A 2 input NOR gate, therefore, will sink about 1.6 mA with a V_{OUT} of about 0.4V if both NOR gate inputs are at 5V.

The main point of this discussion is that a common 2 input CMOS NOR gate such as an MM74C02 can be used to drive a normal TTL load in lieu of a special buffer. However, the designer must be willing to sacrifice some noise immunity over temperature to do so.

TIMING CONSIDERATIONS IN CMOS MSIs

There is one more thing to be said in closing. All the flip-flops used in CMOS designs are genuinely edge sensitive. This means that the J-K flip-flops do not "ones catch" and that some of the timing restrictions that applied to the control lines on MSI functions in TTL have been relaxed in the 74C series.

AN-88 CMOS LINEAR APPLICATIONS

Gene Taatjes
National Semiconductor

CMOS LINEAR APPLICATIONS

PNP and NPN bipolar transistors have been used for many years in "complementary" type of amplifier circuits. Now, with the arrival of CMOS technology, complementary P-channel/N-channel MOS transistors are available in monolithic form. The MM74C04 incorporates a P-channel MOS transistor and an N-channel MOS transistor connected in complementary fashion to function as an inverter.

Due to the symmetry of the P- and N-channel transistors, negative feedback around the complementary pair will cause the pair to self bias itself to approximately 1/2 of the supply voltage. Figure 1 shows an idealized voltage transfer characteristic curve of the CMOS inverter connected with negative feedback. Under these conditions the inverter is biased for operation about the midpoint in the linear segment on the steep transition of the voltage transfer characteristic as shown in Figure 1.

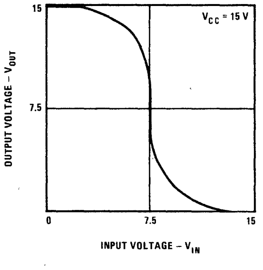


FIGURE 1. Idealized Voltage Transfer Characteristics of an MM74C04 Inverter.

Under AC conditions, a positive going input will cause the output to swing negative and a negative going input will have an inverse effect. Figure 2 shows 1/6 of a MM74C04 inverter package connected as an AC amplifier.

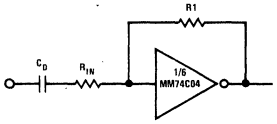


FIGURE 2. A 74CMOS Invertor Biased for Linear Mode Operation.

The power supply current is constant during dynamic operation since the inverter is biased for Class A operation. When the input signal swings near the supply, the output signal will become distorted because the P-N channel devices are driven into the non-linear regions of their transfer characteristics. If the input signal approaches the supply voltages, the P- or N-channel transistors become saturated and supply current is reduced to essentially zero and the device behaves like the classical digital inverter.

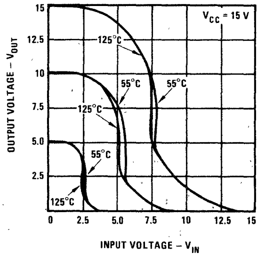


FIGURE 3. Voltage Transfer Characteristics for an Inverter Connected as a Linear Amplifier.

Figure 3 shows typical voltage characteristics of each inverter at several values of the V_{CC}. The shape of these transfer curves are relatively constant with temperature. Temperature affects for the self biased inverter with supply voltage is shown in Figure 4. When the amplifier is operating at 3 volts, the supply current changes drastically as a function of supply voltage because the MOS transistors are operating in the proximity of their gate-source threshold voltages.

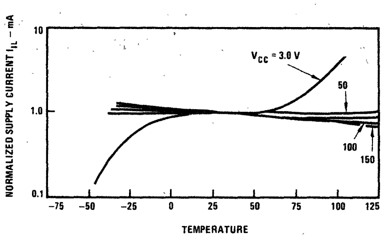


FIGURE 4. Normalized Amplifier Supply Current Versus Ambient Temperature Characteristics.

Figure 5 shows typical curves of voltage gain as a function of operating frequency for various supply voltages.

Output voltages can swing within millivolts of the supplies with either a single or dual supply.

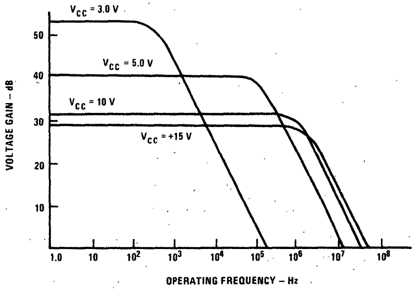


FIGURE 5. Typical Voltage Gain Versus Frequency Characteristics for Amplifier Shown in Figure 2.

APPLICATIONS

Cascading Amplifiers for Higher Gain.

By cascading the basic amplifier block shown in Figure 2 a high gain amplifier can be achieved. The gain will be multiplied by the number of stages used. If more than one inverter is used inside the feedback loop (as in Figure 6) a higher open loop gain is achieved which results in more accurate closed loop gains.

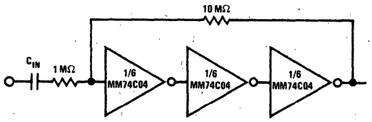


FIGURE 6. Three CMOS Inverters Used as an X10 AC Amplifier.

Post Amplifier for Op Amps.

A standard operational amplifier used with a CMOS inverter for a Post Amplifier has several advantages. The operational amplifier essentially sees no load condition since the input impedance to the inverter is very high. Secondly, the CMOS inverters will swing to within millivolts of either supply. This gives the designer the advantage of operating the operational amplifier under no load conditions yet having the full supply swing capability on the output. Shown in Figure 7 is the LM4250 micropower Op Amp used with a 74C04 inverter for increased output capability while maintaining the low power advantage of both devices.

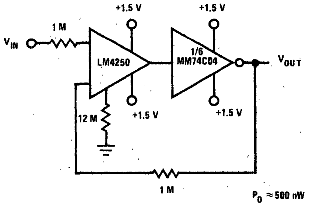


FIGURE 7. MM74C04 Inverter Used as a Post Amplifier for a Battery Operated Op Amp.

The MM74C04 can also be used with single supply amplifier such as the LM324. With the circuit shown in Figure 8, the open loop gain is approximately 160 dB. The LM324 has 4 amplifiers in a package and the MM74C04 has 6 amplifiers per package.

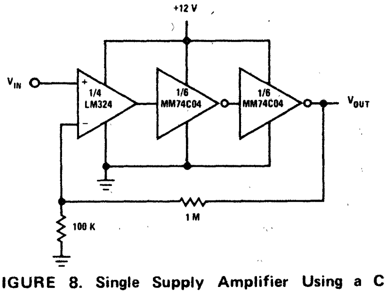


FIGURE 8. Single Supply Amplifier Using a CMOS Cascade Post Amplifier with the LM324.

CMOS inverters can be paralleled for increased power to drive higher current loads. Loads of 5.0 mA per inverter can be expected under AC conditions.

Other 74C devices can be used to provide greater complementary current outputs. The MM74C00 NAND Gate will provide approximately 10 mA from the V_{CC} supply while the MM74C02 will supply approximately 10 mA from the negative supply. Shown in Figure 9 is an operational amplifier using a CMOS power post amplifier to provide greater than 40 mA complementary currents.

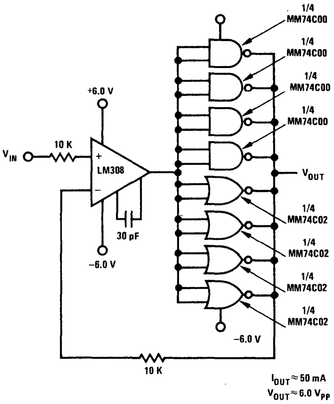


FIGURE 9. MM74C00 and MM74C02 Used as a Post Amplifier to Provide Increased Current Drive.

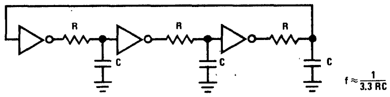
Other Applications.

Shown in Figure 10 is a variety of applications utilizing CMOS devices. Shown is a linear phase shift oscillator and an integrator which use the CMOS devices in the linear mode as well as a few circuit ideas for clocks and one shots.

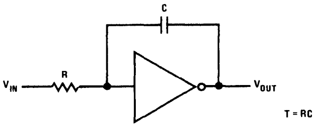
Conclusion

Careful study of CMOS characteristics show that CMOS devices used in a system design can be used for linear building blocks as well as digital blocks.

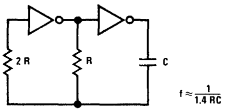
Utilization of these new devices will decrease package count and reduce supply requirements. The circuit designer now can do both digital and linear designs with the same type of device.



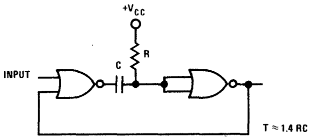
Phase Shift Oscillator Using MM74C04



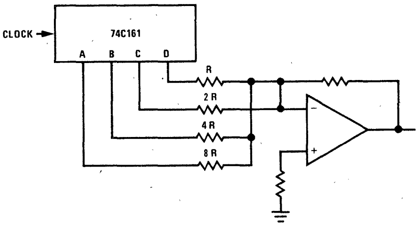
Integrator Using Any Inverting CMOS Gate



Square Wave Oscillator



One Shot



Staircase Generator

FIGURE 10. Variety of Circuit Ideas Using CMOS Devices.

Thomas P. Redfern
National Semiconductor

54C/74C FAMILY CHARACTERISTICS

INTRODUCTION

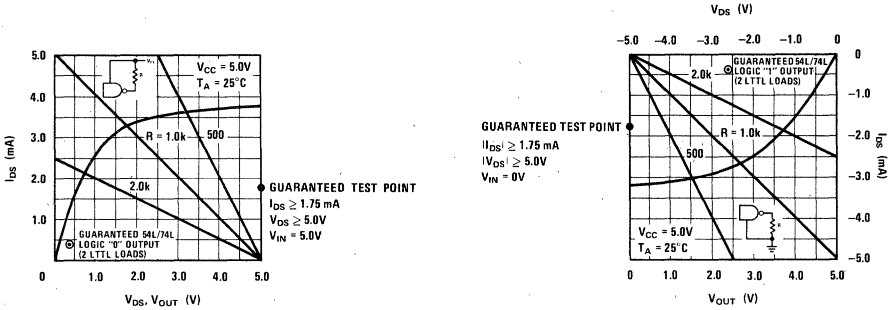
The purpose of this 54C/74C Family Characteristics application note is to set down, in one place, all those characteristics which are common to the devices in the MM54C/MM74C logic family. The characteristics which can be considered to apply are:

1. Output voltage-current characteristics
2. Noise characteristics
3. Power consumption
4. Propagation delay (speed)
5. Temperature characteristics

With a good understanding of the above characteristics the designer will have the necessary tools to optimize his system. An attempt will be made to present the information in as simple a manner as possible to facilitate its use. This coupled with the fact that 54C/74C has the same function and pin-out as standard series 54L/74L will make the application of CMOS to digital systems very straightforward.

OUTPUT CHARACTERISTICS

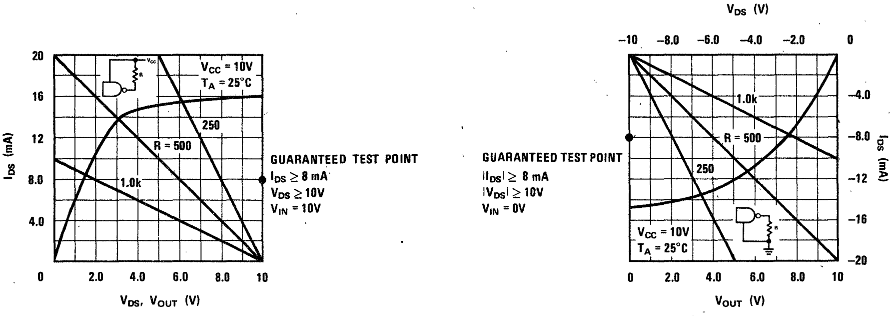
Figure 1 and Figure 2 show typical output drain characteristics for the basic inverter used in the 54C/74C family. For more detailed information on the operation of the basic inverter the reader is directed to application note AN-77, "CMOS, The Ideal Logic Family." Although more complex gates, and MSI devices, may be composed of combinations of parallel and series transistors the considerations that govern the output characteristics of the basic inverter apply to these more complex structures as well.



(A) Typical Output Sink Characteristic (N-Channel)

(B) Typical Output Source Characteristic (P-Channel)

FIGURE 1



(A) Typical Output Sink Characteristic (N-Channel)

(B) Typical Output Source Characteristic (P-Channel)

FIGURE 2

The 54C/74C family is designed so that the output characteristics of all devices are matched as closely as possible. To ensure uniformity all devices are tested at four output conditions (see Figures 1 and 2). These points are:

$V_{CC} = 5.0V$	$V_{IN} = 5.0V$ $I_{DS} \geq 1.75$ mA $V_{DS} \geq 5.0V$	$V_{IN} = 0V$ $\lvert I_{DS} \rvert \geq 1.75$ mA $\lvert V_{DS} \rvert \geq 5.0V$
$V_{CC} = 10V$	$V_{IN} = 10V$ $I_{DS} \geq 8.0$ mA $V_{DS} \geq 10V$	$V_{IN} = 0V$ $\lvert I_{DS} \rvert \geq 8.0$ mA $\lvert V_{DS} \rvert \geq 10V$

Note that each device data sheet guarantees these points in the table of electrical characteristics.

The output characteristics can be used to determine the output voltage for any load condition. Figures 1 and 2 show load lines for resistive loads to V_{CC} for sink currents and to GND for source currents. The intersections of this load line with the drain characteristic in question gives the output voltage. For example at $V_{CC} = 5.0V$, $V_{OUT} = 1.5V$ (typ) with a load of 500Ω to ground.

These figures also show the guaranteed points for driving two 54L/74L standard loads. As can be seen there is typically ample margin at $V_{CC} = 5.0V$.

In the case where the 54C/74C device is driving another CMOS device the load line is coincident with the $I_{DS} = 0$ axis and the output will then typically switch to either V_{CC} or ground.

NOISE CHARACTERISTICS

Definition of Terms

Noise Immunity: The noise immunity of a logic element is that voltage which applied to the input will cause the output to change its output state.

Noise Margin: The noise margin of a logic element is the difference between the guaranteed logical "1" ("0") level output voltage and the guaranteed logical "1" ("0") level input voltage.

The transfer characteristic of Figure 3 shows typical noise immunity and guaranteed noise margin for a 54C/74C device operating at V_{CC} = 10V. The typical noise immunity does not change with voltage and is 45% of V_{CC}.

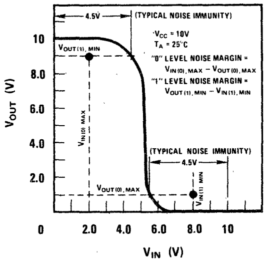


FIGURE 3. Typical Transfer Characteristic

All 54C/74C devices are guaranteed to have a noise margin of 1.0V or greater over all operating conditions (see Figure 4).

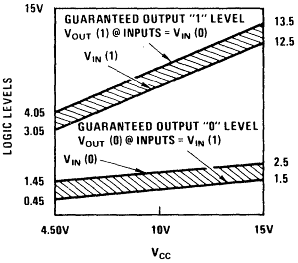
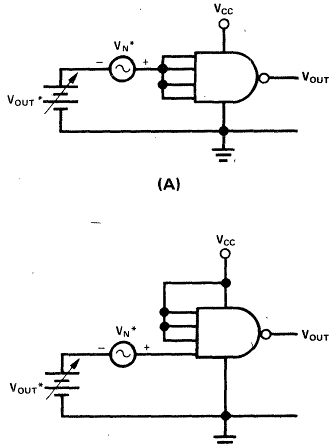


FIGURE 4. Guaranteed Noise Margin Over Temperature vs V_{CC}

Noise immunity is an important device characteristic. However, noise margin is of more use to the designer because it very simply defines the amount of noise a system can tolerate under any circumstances and still maintain the integrity of logic levels.

Any noise specification to be complete must define how measurements are to be made. Figure 5 indicates two extreme cases; driving all inputs simultaneously and driving one input at a time. Both conditions must be included because each represents one worst case extreme.



(A)

*$V_{OUT} = V_{OUT(1)MIN}, V_{OUT(0)MAX}$
V_N = ALLOWABLE NOISE VOLTAGE = 1.0V

(B)

FIGURE 5. Noise Margin Test Circuits

To guarantee a noise margin of 1.0V, all 54C/74C devices are tested under both conditions. It is important to note that this guarantees that every node within a system can have 1.0V of noise, in logic "1" or logic "0" state, without malfunctioning. This could not be guaranteed without testing for both conditions in Figure 5.

POWER CONSUMPTION

There are four sources of power consumption in CMOS devices: (1) leakage current (2) transient power due to load capacitance (3) transient power due to internal capacitance and (4) transient power due to current spiking during switching.

The first, leakage current, is the easiest to calculate and is simply the leakage current times V_{CC}. The data sheet for each specific device specifies this leakage current.

The second, transient power due to load capacitance, can be derived from the fact that the energy stored on a capacitor is $1/2\ CV^2$. Therefore every time the load capacitance is charged or discharged this amount of energy must be provided by the CMOS device. The energy per cycle is then $2\ [(1/2)\ CV_{CC}^2] = CV_{CC}^2$. Energy per unit time, or power, is then $CV_{CC}^2\ f$, where C is the load capacitance and f is the frequency.

The third, transient power due to internal capacitance takes exactly the same form as the load capacitance. Every device has some internal nodal capacitance which must be charged and discharged. This then represents another power term which must be considered.

The fourth, transient power due to switching current, is caused by the fact that whenever a CMOS device goes through a transition, with $V_{CC} \geq 2\ V_T$, there is a time when both N-channel and P-channel devices are both conducting. An expression for this current is derived in application note AN-77. The expression is:

$$P_{VI} = \frac{1}{2}\ (V_{CC} - 2\ V_T)\ I_{CC\,MAX}\ (t_{RISE} + t_{FALL})\ f$$

where:

V_T = threshold voltage

$I_{CC(MAX)}$ = peak non-capacitive current during switching

f = frequency

Note that this expression, like the capacitive power term is directly proportional to frequency. If the P_{VI} term is combined with the term arising from the internal capacitance, a capacitance C_{PD} may be defined which closely approximates the no load power consumption for a CMOS device when used in the following expression:

$$\text{Power (no load)} = C_{PD}\ V_{CC}^2\ f$$

The total power consumption is then simplified to:

$$\text{Total Power} = (C_{PD} + C_L)\ V_{CC}^2\ f + I_{LEAK}\ V_{CC} \quad (1)$$

The procedure for obtaining C_{PD} is to measure the no load power at V_{CC} = 10V vs frequency and calculate the value of C_{PD} which corresponds to the measured power consumption. This value of C_{PD} is given on each 54C/74C data sheet and with equation (1) the computation of power consumption is straightforward.

To simplify the task even further Figure 6 gives a graph of normalized power vs frequency for different power supply voltages. To obtain actual power consumption find the normalized power for a particular V_{CC} and frequency, then multiply by $C_{PD} + C_L$.

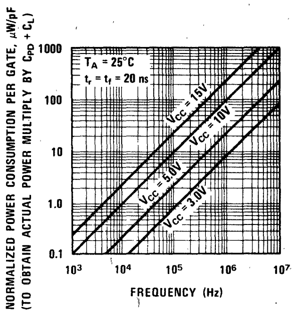


FIGURE 6. Normalized Typical Power Consumption vs Frequency

As an example let's find the total power consumption for an MM74C00 operating at f = 100 kHz, V_{CC} = 10V and C_L = 50 pF. From the curve, normalized power per gate equals 10μW/pF. From the data sheet C_{PD} = 12 pF; therefore, actual power per gate is:

$$\frac{\text{power}}{\text{gate}} = \frac{10\mu W}{pF} \times (12\ pF + 50\ pF) = \frac{0.62\ mW}{\text{gate}}$$

$$\text{total power} = \frac{\text{no. of gates}}{\text{package}} \times \frac{\text{power}}{\text{gate}} + I_{LEAKAGE} \times V_{CC}$$

$$= 4 \times 0.62\ mW + 0.01\mu A \times 10V \cong 2.48\ mW$$

Up to this point the discussion of power consumption has been limited to simple gate functions. Power consumption for an MSI function is more complex but the same technique just derived applies. To demonstrate the technique let's compute the total power consumption of a MM74C161, four bit binary counter, at V_{CC} = 10V, f = 1 MHz and C_L = 50 pF on each output.

The no load power is still given by P (no load) = $C_{PD}\ V_{CC}^2\ f$. This demonstrates the usefulness of the concept of the internal capacitance, C_{PD}. Even through the circuit is very complex and has many nodes charging and discharging at various rates, all of the effects can be easily lumped into one easy to use term, C_{PD}.

Calculation of transient power due to load capacitance is a little more complex since each output is switched at one half the rate of the previous output: Taking this into account the complete expression for power consumption is:

$$P_{TOTAL} = \underbrace{C_{PD} V_{CC}^2 f}_{\substack{\text{no load}\\ \text{power}}} + \underbrace{C_L V_{CC}^2 \frac{f}{2}}_{\substack{\text{output}\\ \text{power of}\\ \text{1st stage}}} + \underbrace{C_L V_{CC}^2 \frac{f}{4}}_{\text{2nd stage}}$$

$$+ \underbrace{C_L V_{CC}^2 \frac{f}{8}}_{\text{3rd stage}} + \underbrace{2 C_L V_{CC}^2 \frac{f}{16}}_{\substack{\text{4th stage}\\ \text{\& carry}\\ \text{output}}} + \underbrace{I_L V_{CC}}_{\substack{\text{leakage}\\ \text{term}}}$$

This reduces to:

$$P_{TOTAL} = (C_{PD} + C_L) V_{CC}^2 f + I_L V_{CC}$$

From the data sheet C_{PD} = 90 pF and $I_L = 0.05\mu A$. Using Figure 6 total power is then:

$$P_{TOTAL} = (90\text{ pF} + 50\text{ pF}) \text{ X } \frac{100\mu W}{\text{pF}} + 0.05 \text{ X } 10^{-6}$$

$$\text{X } 10V \cong 14\text{ mW}$$

This demonstrates that with more complex devices the concept of C_{PD} greatly simplifies the calculation of total power consumption. It becomes an easy task to compute power for different voltages and frequencies by use of Figure 6 and the equations above.

PROPAGATION DELAY

Propagation delay for all 54C/74C devices is guaranteed with a load of 50 pF and input rise and fall times of 20 ns. A 50 pF load was chosen, instead of 15 pF as in the 4000 series, because it is representative of loads commonly seen in CMOS systems. A good rule of thumb, in designing with CMOS, is to assume 10 pF of interwiring capacitance. Operating at the specified propagation delay would allow 5 pF fanout for the 4000 series while 54C/74C has a fanout of 40 pF. A fanout of 5 pF (one gate input) is all but useless, and specified propagation delay would most probably not be realized in an actual system.

Operating at loads other than 50 pF poses a problem since propagation is a function of load capacitance. To simplify the problem Figure 7 has been generated and gives the slope of the propagation delay vs load capacitance line (Δt_{pd}/pF) as a function of power supply voltage. Because the propagation delay for zero load capacitance is not zero and depends on the internal structure of each device, an offset term must be added that is unique to a particular device type. Since each data sheet gives propagation delay for 50 pF the actual delay for different loads can be computed with the aid of the following equation:

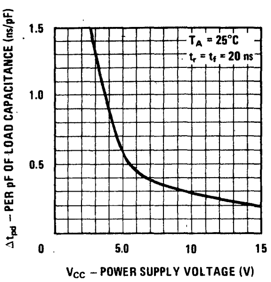


FIGURE 7. Typical Propagation Delay per pF of Load Capacitance vs Power Supply

$$t_{pd}\Big|_{C_L = C} = (C - 50)\text{ pF X } \frac{\Delta t_{pd}}{\text{pF}} + t_{pd}\Big|_{C_L = 50\text{ pF}}$$

where:

C = Actual load capacitance

$t_{pd}\Big|_{C_L = 50\text{ pF}}$ = propagation delay with 50 pF load, (specified on each device data sheet)

$\frac{\Delta t_{pd}}{\text{pF}}$ = Value obtained from Figure 7.

As an example let's compute the propagation delay for an MM74C00 driving 15 pF load and operating with a V_{CC} = 5.0V. The equation gives:

$$t_{pd}\Big|_{C_L = 15\text{ pF}} = (15 - 50)\text{ pF X } 0.57\frac{\text{ns}}{\text{pF}} + 50\text{ ns}$$

$$= -20\text{ ns} + 50\text{ ns} = 30\text{ ns}$$

The same formula and curves may be applied to more complex devices. For example the propagation delay from data to output for an MM74C157 operating at V_{CC} = 10V and C_L = 100 pF is:

$$t_{pd}\Big|_{C_L = 100\text{ pF}} = (100 - 50)\ 0.29\text{ ns} + 70\text{ ns}$$

$$= 14.5 + 70 \cong 85\text{ ns}$$

It is significant to note that this equation and Figure 7 apply to *all* 54C/74C devices. This is true because of the close match in drive characteristics of every device including MSI functions, i.e., the slope of the propagation delay vs load capacitance line at a given voltage is typically equal for all devices. The only exception is high fan-out buffers which have a smaller Δt_{pd}/pF.

Another point to consider in the design of a CMOS system is the affect of power supply voltage on propagation delay. Figure 8 shows propagation delay as a function of V_{CC} and propagation delay times power consumption vs V_{CC} for an MM74C00 operating with 50 pF load at f = 100 kHz.

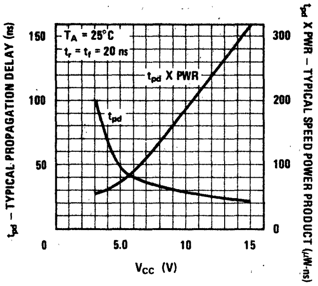


FIGURE 8. Speed Power Product and Propagation Delay vs V_{CC}

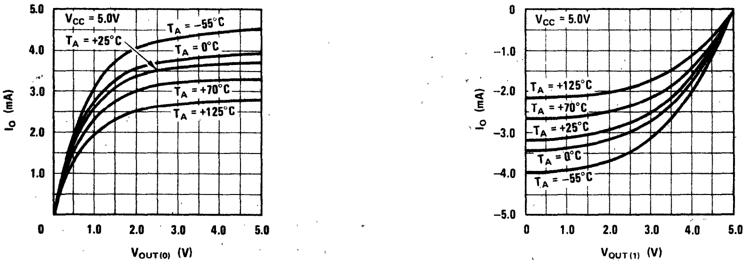
Above V_{CC} = 5.0V note the speed power product curve approaches a straight line. However the t_{pd} curve starts to "flatten out." Going from V_{CC} = 5.0V to V_{CC} = 10V gives a 40% decrease in propagation delay and going from V_{CC} = 10V to V_{CC} = 15V only decreases propagation delay by 25%. Clearly for $V_{CC} > 10V$ a small increase in speed is gained by a disproportionate increase in power. Conversely, for small decreases in power below V_{CC} = 5.0V large increases in propagation delay result.

Obviously it is optimum to use the lowest voltage consistent with system speed requirements. However in general it can be seen from Figure 8 that the best speed power performance will be obtained in the V_{CC} = 5.0V to V_{CC} = 10V range.

TEMPERATURE CHARACTERISTICS

Figures 9 and 10 give temperature variations in drain characteristics for the N-channel and P-channel devices operating at V_{CC} = 5.0V and V_{CC} = 10V respectively. As can be seen from these curves the output sink and source current decreases as temperature increases. The affect is almost linear and can be closely approximated by a temperature coefficient of −0.3% per degree centigrade.

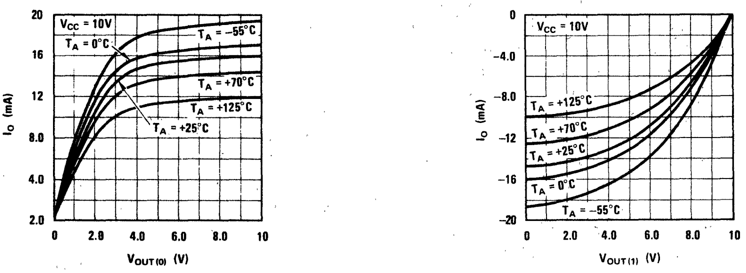
Since the t_{pd} can be entirely attributed to rise and fall time, the temperature dependance of t_{pd} is a function of the rate at which the output load capacitance can be charged and discharged. This in turn is a function of the sink/source current which was shown above to vary as −0.3% per degree centigrade. Consequently we can say that t_{pd} varies as −0.3% per degree centigrade. Actual measurements of t_{pd} with temperature verifies this number.



(A) Typical Output Drain Characteristic (N-Channel)

(B) Typical Output Drain Characteristic (P-Channel)

FIGURE 9



(A) Typical Output Drain Characteristic (N-Channel)

(B) Typical Output Drain Characteristic (P-Channel)

FIGURE 10

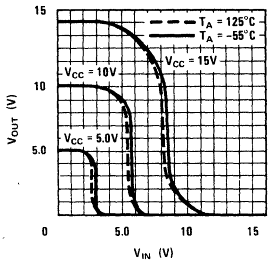


FIGURE 11. Typical Gate Transfer Characteristics

The drain characteristics of Figure 9 and 10 show considerable variation with temperature. Examination of the transfer characteristics of Figure 11 indicates that they are almost independent of temperature. The transfer characteristic is not dependent on temperature because although both the N-channel and P-channel device characteristics change with temperature these changes track each other closely. The proof of this tracking is the temperature independance of the transfer characteristics. Noise margin and maximum/minimum logic levels will then not be dependent on temperature.

As discussed previously power consumption is a function of C_{PD}, C_L, V_{CC}, f and $I_{LEAKAGE}$. All of these terms are essentially constant with temperature except $I_{LEAKAGE}$. However, the leakage current specified on each 54C/74C device applies across the entire temperature range and therefore represents a worst case limit.

Mike Watts
National Semiconductor

CMOS OSCILLATORS

INTRODUCTION

This note describes several square wave oscillators that can be built using CMOS logic elements. These circuits offer the following advantages:

- Guaranteed startability
- Relatively good stability with respect to power supply variations
- Operation over a wide supply voltage range (3V to 15V)
- Operation over a wide frequency range from less than 1 Hz to about 15 MHz
- Low power consumption (see AN-90)
- Easy interface to other logic families and elements including TTL

Several RC oscillators and two crystal controlled oscillators are described. The stability of the RC oscillator will be sufficient for the bulk of applications; however, some applications will probably require the stability of a crystal. Some applications that require a lot of stability are:

1. Timekeeping over a long interval. A good deal of stability is required to duplicate the performance of an ordinary wrist watch (about 12 ppm). This is, of course, obtainable with a crystal. However, if the time interval is short and/or the resolution of the timekeeping device is relatively large, an RC oscillator may be adequate. For example: if a stopwatch is built with a resolution of tenths of seconds and the longest interval of interest is two minutes, then an accuracy of 1 part in 1200 (2 minutes x 60 seconds/minute x 10 tenth/second) may be acceptable since any error is less than the resolution of the device.

2. When logic elements are operated near their specified limits. It may be necessary to maintain clock frequency accuracy within very tight limits in order to avoid exceeding the limits of the logic family being used, or in which the timing relationships of clock signals in dynamic MOS memory or shift register systems must be preserved.

3. Baud rate generators for communications equipment.

4. Any system that must interface with other tightly specified systems. Particularly those that use a "handshake" technique in which Request or Acknowledge pulses must be of specific widths.

LOGICAL OSCILLATORS

Before describing any specific circuits, a few words about logical oscillators may clear up some recurring confusion.

Any odd number of inverting logic gates will oscillate if they are tied together in a ring as shown in *Figure 1*. Many beginning logic designers have discovered this (to their chagrin) by inadvertently providing such a path in their designs. However, some people are confused by the circuit in *Figure 1* because they are accustomed to seeing sinewave oscillators implemented with positive feedback, or amplifiers with non-inverting gain. Since the concept of phase shift becomes a little strained when the inverters remain in their linear region for such a short period, it is far more straightforward to analyze the circuit from the standpoint of ideal switches with finite propagation delays rather than as amplifiers with 180° phase shift. It then becomes obvious that a "1" chases itself around the ring and the network oscillates.

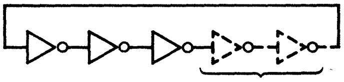


FIGURE 1. Odd Number of Inverters will Always Oscillate

The frequency of oscillation will be determined by the total propagation delay through the ring and is given by the following equation.

$$f = \frac{1}{2nTp}$$

Where:

f = frequency of oscillation
Tp = Propagation delay per gate
n = number of gates

This is not a practical oscillator, of course, but it does illustrate the maximum frequency at which such an oscillator will run. All that must be done to make this a useful oscillator is to slow it down to the desired frequency. Methods of doing this are described later.

To determine the frequency of oscillation, it is necessary to examine the propagation delay of the inverters. CMOS propagation delay depends on supply voltage and load capacitance. Several curves for propagation delay for National's 74C line of CMOS gates are reproduced in *Figure 2.* From these, the natural frequency of oscillation of an odd number of gates can be determined.

An example may be instructive.

Assume the supply voltage is 10V. Since only one input is driven by each inverter, the load capacitance on each inverter is at most about 8 pF. Examine the curve in *Figure 2c* that is drawn for V_{CC} = 10V and extrapolate it down to 8 pF. We see that the curve predicts a propagation delay of about 17 ns. We can then calculate the frequency of oscillation for three inverters using the expression mentioned above. Thus:

$$f = \frac{1}{2 \times 3 \times 17 \times 10^{-9}} = 9.8\ \text{MHz}$$

Lab work indicates this is low and that something closer to 16 MHz can be expected. This reflects the conservative nature of the curves in *Figure 2.*

Since this frequency is directly controlled by propagation delays, it will vary a great deal with temperature, supply voltage, and any external loading, as indicated by the graphs in *Figure 2.* In order to build a usefully stable oscillator it is necessary to add passive elements that determine oscillation frequency and minimize the effect of CMOS characteristics.

STABLE RC OSCILLATOR

Figure 3 illustrates a useful oscillator made with three inverters. Actually, any inverting CMOS gate or combination of gates could be used. This means left over portions of gate packages can be often used. The duty cycle will be close to 50% and will oscillate at a frequency that is given by the following expression.

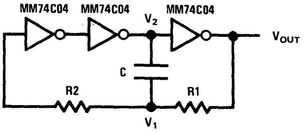


FIGURE 3. Three Gate Oscilaltor

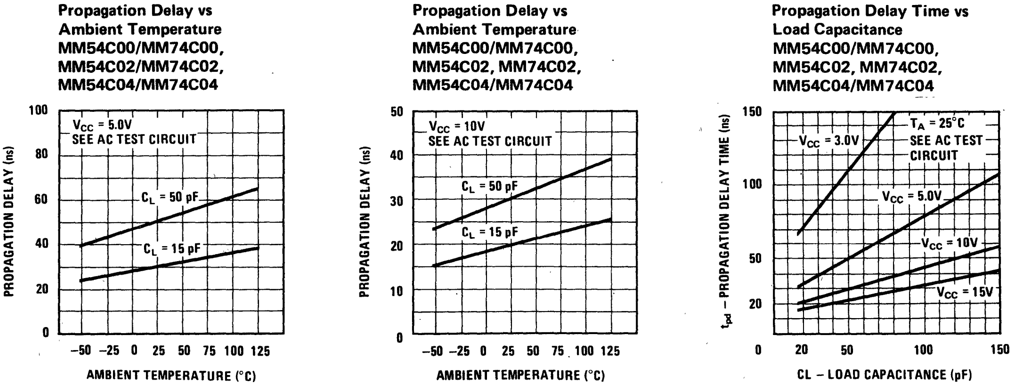
$$f \cong \frac{1}{2\,R1\,C\left(\frac{0.405\,R2}{R1 + R2} + 0.693\right)}$$

Another form of this expression is:

$$f \cong \frac{1}{2C\,(0.405\,R_{eq} + 0.693\,R1)}$$

Where:

$$R_{eq} = \frac{R1\,R2}{R1 + R2}$$



(a) (b) (c)

FIGURE 2. Propagation Delay for 74C Gates

The following three special cases may be useful.

If R1 = R2 = R $$f \cong \frac{0.559}{RC}$$

If R2 >>> R1 $$f \cong \frac{0.455}{RC}$$

If R2 <<< R1 $$f \cong \frac{0.722}{RC}$$

Figure 4 illustrates the approximate output waveform and the voltage V_1 at the charging node.

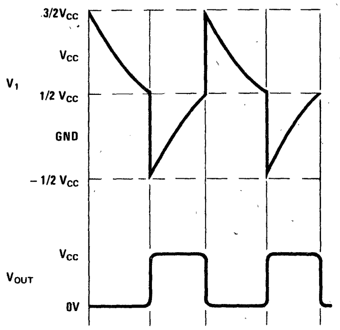


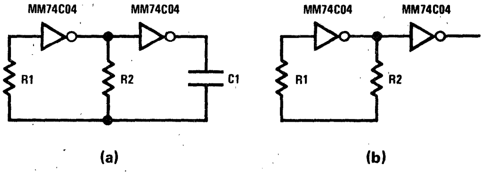
FIGURE 4. Waveforms for Oscillator in Figure 3

Note that the voltage V_2 will be clamped by input diodes when V_1 is greater than V_{CC} or more negative than ground. During this portion of the cycle current will flow through R2. At all other times the only current through R2 is a very minimal leakage term. Note also that as soon as V_1 passes through threshold (about 50% of supply) and the input to the last inverter begins to change, V_1 will also change in a direction that reinforces the switching action; i.e., providing positive feedback. This further enhances the stability and predictability of the network.

This oscillator is fairly insensitive to power supply variations due largely to the threshold tracking close to 50% of the supply voltage. Just how stable it is will be determined by the frequency of oscillation; the lower the frequency the more stability and vice versa. This is because propagation delay and the effect of threshold shifts comprise a smaller portion of the overall period. Stability will also be enhanced if R1 is made large enough to swamp any variations in the CMOS output resistance.

TWO GATE OSCILLATOR WILL NOT NECESSARILY OSCILLATE

A popular oscillator is shown in *Figure 5a.* The only undesirable feature of this oscillator is that it may not oscillate. This is readily demonstrated by letting the value of C go to zero. The network then degenerates into *Figure 5b,* which obviously will not oscillate. This illustrates that there is some value of C1 that will not force the network to oscillate. The real difference between this two gate oscillator and the three gate oscillator is that the former must be forced to oscillate by the capacitor while the three gate network will always oscillate willingly and is simply slowed down by the capacitor. The three gate network will always oscillate, regardless of the value of C1 but the two gate oscillator will not oscillate when C1 is small.



(a) (b)

FIGURE 5. Less Than Perfect Oscillator

The only advantage the two gate oscillator has over the three gate oscillator is that it uses one less inverter. This may or may not be a real concern, depending on the gate count in each user's specific application. However, the next section offers a real minimum parts count oscillator.

A SINGLE SCHMITT TRIGGER MAKES AN OSCILLATOR

Figure 6 illustrates an oscillator made from a single Schmitt trigger. Since the MM74C14 is a hex Schmitt trigger, this oscillator consumes only one sixth of a package. The remaining 5 gates can be used either as ordinary inverters like the MM74C04 or their Schmitt trigger characteristics can be used to advantage in the normal manner. Assuming these five inverters can be used elsewhere in the system, *Figure 6* must represent the ultimate in low gate count oscillators.

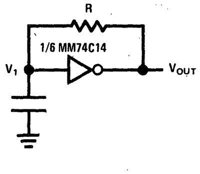


FIGURE 6. Schmitt Trigger Oscillator

Voltage V_1 is depicted in *Figure 7* and changes between the two thresholds of the Schmitt trigger. If these thresholds were constant percentages of V_{CC} over the supply voltage range, the oscillator would be insensitive to variations in V_{CC}. However, this is not the case. The thresholds of the Schmitt trigger vary enough to make the oscillator exhibit a good deal of sensitivity to V_{CC}.

Applications that do not require extreme stability or that have access to well regulated supplies should not be bothered by this sensitivity to V_{CC}. Variations in threshold can be expected to run as high as four or five percent when V_{CC} varies from 5V to 15V.

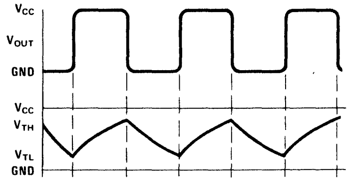


FIGURE 7. Waveforms for Schmitt Trigger Oscillator in Figure 6

A CMOS Crystal Oscillator

Figure 8 illustrates a crystal oscillator that uses only one CMOS inverter as the active element. Any odd number of inverters may be used, but the total propagation delay through the ring limits the highest frequency that can be obtained. Obviously, the fewer inverters that are used, the higher the maximum possible frequency.

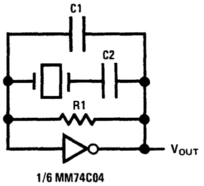


FIGURE 8. Crystal Oscillator

Capacitor C1 will pull the crystal down and C2 will pull it up. R1 simply insures a dc path around the inverter and will bias it on. R1 may be quite large, on the order of 1-5 megohms. The smaller R1 is, the more the crystal's Q will be reduced.

This oscillator is perfectly stable with respect to power supply variations as long as the propagation delay does not get so long that the oscillator cannot keep up with the crystal. A typical single inverter will oscillate quite readily at 9 MHz, even when V_{CC} is 3V.

A problem that must be addressed at the lower frequencies (below about 4 MHz) is that of overtone oscillation. Care must be taken to prevent the crystal from oscillating at its third harmonic. This is a problem in almost any design, whether or not CMOS is the active element. The problem is readily handled by simply increasing the propagation delay through the ring of inverters to a point where the ring will not oscillate at the harmonic frequency but will continue to oscillate at the fundamental frequency. *Figure 9* illustrates an acceptable method.

This network is the same as the one in *Figure 8* except that more inverters are used and R2 and C3 have been added to deteriorate the propagation delay as much as desired. The five inverters not only add delay but also increase the gain through the loop.

CONCLUSIONS

A large number of oscillator applications can be implemented with the extremely simple, reliable, inexpensive and versatile CMOS oscillators described in this note. These oscillators consume very little power compared to most other approaches. Each of the oscillators requires less than one full package of CMOS inverters of the MM74C04 variety. Frequently such an oscillator can be built using leftover gates of the MM74C00, MM74C02, MM74C10 variety. Stability superior to that easily attainable with TTL oscillators is readily attained, particularly at lower frequencies. These oscillators are so versatile, easy to build, and inexpensive that they should find their way into many diverse designs.

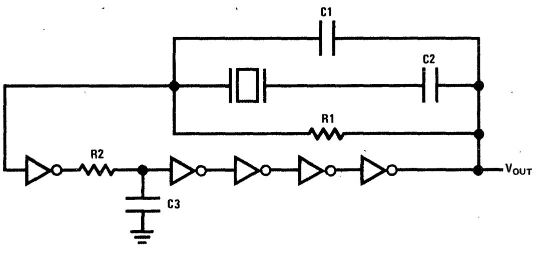


FIGURE 9. Crystal Oscillator with Overtone Protection

Thomas P. Redfern
National Semiconductor

USING THE CMOS DUAL MONOSTABLE MULTIVIBRATOR

INTRODUCTION

The MM54C221/MM74C221 is a dual CMOS monostable multivibrator. Each one-shot has three inputs (A, B and CLR) and two outputs (Q and $\bar{Q}$). The output pulse width is set by an external RC network.

The A and B inputs trigger an output pulse on a negative or positive input transition respectively. The CLR input when low resets the one-shot. Once triggered the A and B inputs have no further control on the output.

THEORY OF OPERATION

Figure 1 shows that in its stable state, the one-shot clamps C_{EXT} to ground by turning N1 ON and holds the positive comparator input at V_{CC} by turning N2 OFF. The prefix N is used to denote N-channel transistors.

The signal, G, gating N2 OFF also gates the comparator OFF thereby keeping the internal power dissipation to an absolute minimum. The only power dissipation when in the stable state is that generated by the current through R_{EXT}. The bulk of this dissipation is in R_{EXT} since the voltage drop across N1 is very small for normal ranges of R_{EXT}.

To trigger the one-shot the CLR input must be high. The gating, G, on the comparator is designed such that the comparator output is high when the one-shot is in its stable state. With the CLR input high the clear input to FF is disabled allowing the flip-flop to respond to the A or B input. A negative transition on A or a positive transition on B sets Q to a high state. This in turn gates N1 OFF, and N2 and the comparator ON.

Gating N2 ON establishes a reference of 0.63 V_{CC} on the comparator's positive input. Since the voltage on C_{EXT} can not change instantaneously $V1 = 0V$ at this time. The comparator then will maintain its one level on the output. Gating N1 OFF allows C_{EXT} to start charging through R_{EXT} toward V_{CC} exponentially.

Assuming a perfect comparator (zero offset and infinite gain) when the voltage on C_{EXT}, V1, equals 0.63 V_{CC} the comparator output will go from a high state to a low state resetting Q to a low state. *Figure 2* is a timing diagram summarizing this sequence of events.

This diagram is idealized by assuming zero rise and fall times and zero propagation delay but it shows the basic operation of the one-shot. Also shown is the effect of taking the CLR input low. Whenever CLR goes low FF

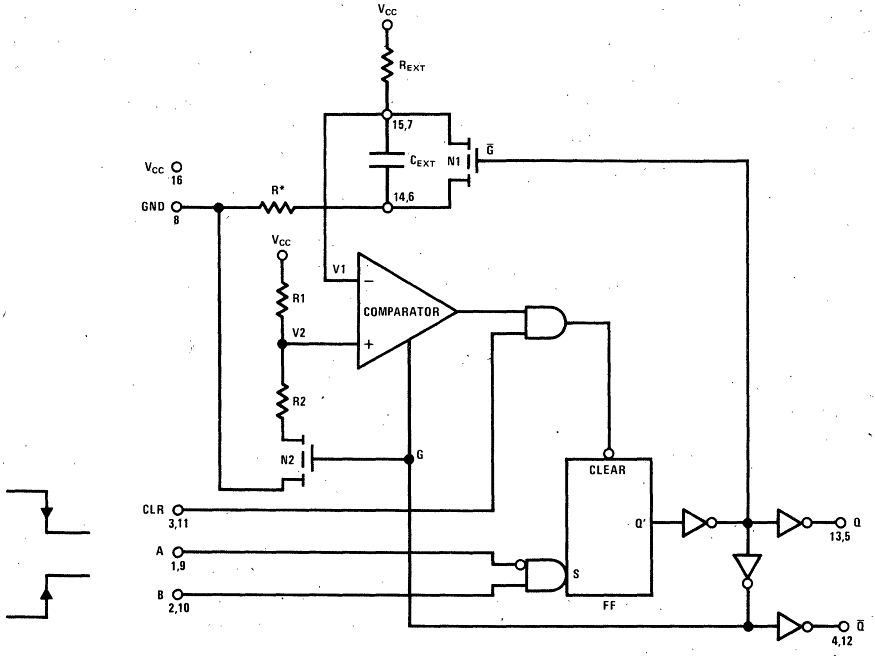


FIGURE 1. Monostable Multivibrator Logic Diagram

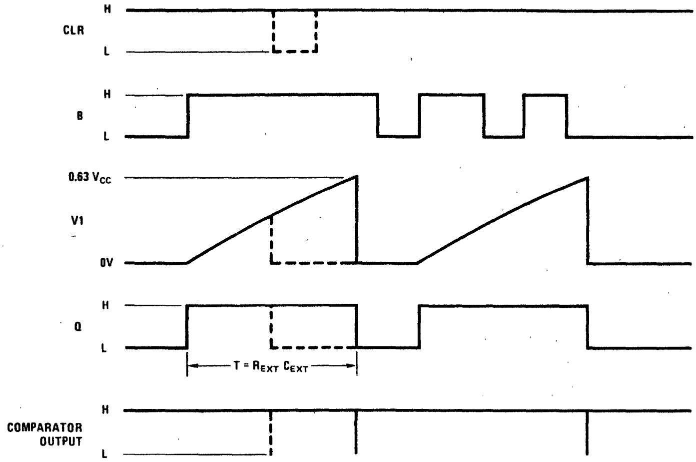


FIGURE 2. One-Shot Timing Diagram

is reset independent of all other inputs. *Figure 2* also shows that once triggered, the output is independent of any transitions on B (or A) until the cycle is complete.

The output pulse width is determined by the following equation:

$$V1 = V_{CC}\,(1 - e^{-T/R_{EXT}C_{EXT}}) = 0.63\,V_{CC} \qquad (1)$$

Solving for t gives:

$$T = R_{EXT}\,C_{EXT}\ln(1/0.37) = R_{EXT}\,C_{EXT} \qquad (2)$$

A word of caution should be given in regards to the ground connection of the external capacitor (C_{EXT}). It should always be connected as shown in *Figure 1* to pin 14 or 6 and never to pin 8. This is important because of the parasitic resistor R*. Because of the large discharge current through R*, if the capacitor is connected to pin 8, a four layer diode action can result causing the circuit to latch and possibly damage itself.

ACCURACY

There are many factors which influence the accuracy of the one-shot. The most important are:

a. Comparator input offset
b. Comparator gain
c. Comparator time delay
d. Voltage divider R1, R2
e. Delays in logic elements
f. ON impedance of N1 and N2
g. Leakage of N1
h. Leakage of C_{EXT}
i. Magnitude of R_{EXT} and C_{EXT}

The characteristics of C_{EXT} and R_{EXT} are, of course, not determined by the characteristics of the one-shot. In order to establish the accuracy of the one-shot, devices were tested using an external resistance of 10 kΩ and various capacitors. A resistance of 10 kΩ was chosen because the leakage and ON impedance of transistor N1 have a minimal effect on accuracy with this value of resistance.

Two values of C_{EXT} were chosen, 1000 pF and 0.1µF. These values give pulse widths of 10µs and 1000µs with R_{EXT} = 10 kΩ.

Figures 3 and 4 show the resulting distributions of pulse widths at 25°C for various power supply voltages. Because propagation delays, at the same power supply voltage, are the same independent of pulse width, the shorter the pulse width the more the accuracy is

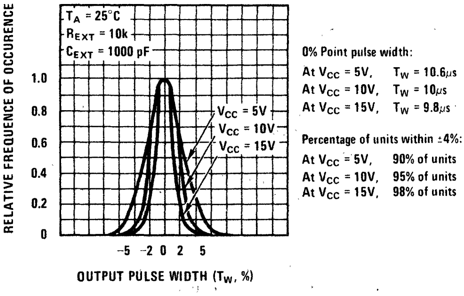


FIGURE 3. Typical Pulse Width Distribution for 10µs Pulse.

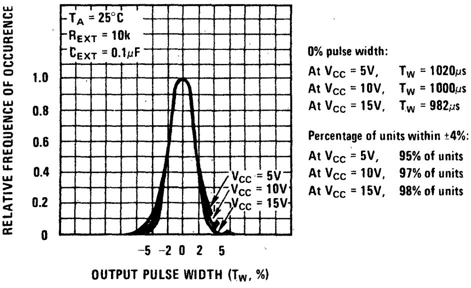


FIGURE 4. Typical Pulse Width Distribution for 1000µs Pulse.

affected by propagation delay. *Figures 3 and 4* clearly show this effect. As pointed out in application note AN-90, 54C/74C Family Characteristics, propagation delay is a function of V_{CC}. *Figure 3,* (Pulse Width = 10μs) shows much greater variation with V_{CC} than *Figure 4* (Pulse Width = 1000μs). This same information is shown in *Figures 5 and 6* in a different format. In these figures the percent deviation from the average pulse width at 10V V_{CC} is shown vs V_{CC}. In addition to the average value the 10% and 90% points are shown. These percentage points refer to the statistical distribution of pulse width error. As an example, at V_{CC} = 10V for 10μs pulse width, 90% of the devices have errors of less than +1.7% and 10% have errors less than −2.1%. In other words, 80% have errors between +1.7% and −2.1%.

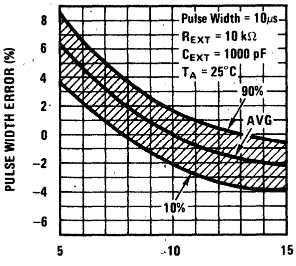


FIGURE 5. Typical Percentage Deviation from V_{CC} = 10V Value vs V_{CC} (PW = 10μs).

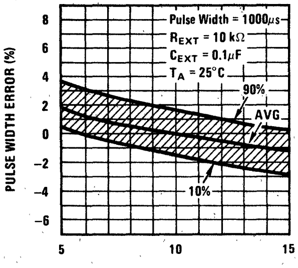


FIGURE 6. Typical Percentage Deviation from V_{CC} = 10V Value vs V_{CC} (PW = 1000μs).

The minimum error can be obtained by operating at the maximum V_{CC}. A price must be paid for this and this price is, of course, increased power dissipation.

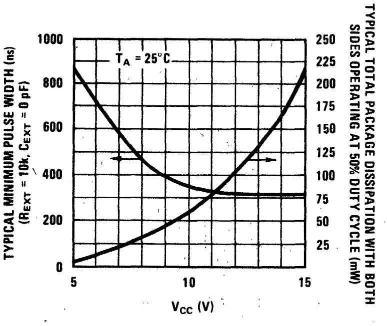


FIGURE 7. Typical Minimum Pulse Width and Power Dissipation vs V_{CC}.

Figure 7 shows typical power dissipation vs V_{CC} operating both sides of the one-shot at 50% duty cycle. Also shown in the same figure is typical minimum pulse width vs V_{CC}. The minimum pulse width is a strong function of internal propagation delays. It is obvious from these two curves that increasing V_{CC} beyond 10V will not appreciably improve inaccuracy due to propagation delay but will greatly increase power dissipation.

Accuracy is also a function of temperature. To determine the magnitude of its effects the one-shot was tested at temperature with the external resistance and capacitance maintained at 25°C. The resulting variation is shown in *Figures 8 and 9.*

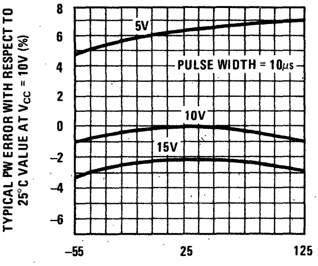


FIGURE 8. Typical Pulse Width Error vs Temperature (PW = 10μs).

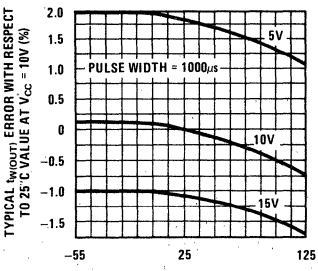


FIGURE 9. Typical Pulse Width Error vs Temperature (PW = 1000μs).

Up to this point the external timing resistor, R_{EXT}, has been held fixed at 10 kΩ. In actual applications other values may be necessary to achieve the desired pulse width. The question then arises as to what effect this will have on accuracy.

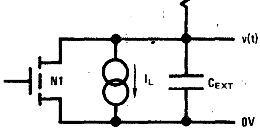


FIGURE 10.

As R_{EXT} becomes larger and larger the leakage current on transistor N1 becomes an ever increasing problem. The equivalent circuit for this leakage is shown in *Figure 10.*

v(t) is given by:

$$v(t) = (V_{CC} - I_L R_{EXT})(1 - e^{-t_L/R_{EXT} C_{EXT}})$$

As before, when v(t) = 0.63 V_{CC}, the output will reset. Solving for t_L gives:

$$t_L = R_{EXT} C_{EXT} \ell n \left(\frac{V_{CC} - I_L R_{EXT}}{0.37 V_{CC} - I_L R_{EXT}} \right) \qquad (3)$$

Using T as defined in Equation 2 the pulse width error is:

$$\text{PW Error} = \frac{t_L - T}{T} \times 100\%$$

Substituting Equations 2 and 3 gives:

$$\text{PW Error} = \frac{R_{EXT} C_{EXT} \ell n \left(\frac{V_{CC} - I_L R_{EXT}}{0.37 V_{CC} - I_L R_{EXT}} \right) - R_{EXT} C_{EXT} \ell n (1/0.37)}{R_{EXT} C_{EXT} \ell n (1/0.37)}$$

PW Error is plotted in *Figure 11* for V_{CC} = 5, 10 and 15V. As expected, decreasing V_{CC} causes PW Error to increase with fixed I_L. Note that the leakage current, although here assumed to flow through N1, is general and could also be interpreted as leakage through C_{EXT}. See MM54C221/MM74C221 data sheet for leakage limits.

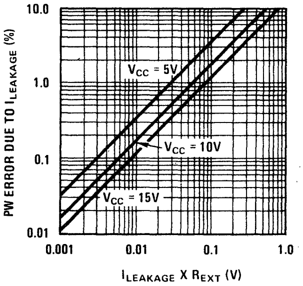


FIGURE 11. Percentage Pulse Width Error Due to Leakage.

To demonstrate the usefulness of *Figure 11* an example will be most helpful. Let us assume that N1 has a leakage of 250 x 10^{-9} amps, C_{EXT} has leakage of 150 x 10^{-9} amps, output pulse width = 0.1 seconds and V_{CC} = 5V. What R_{EXT} C_{EXT} should be used to guarantee an error due to leakage of less than 5%.

From *Figure 11* we see that to meet these conditions $R_{EXT}\ I_L < 0.14V$.

Then:

$$R_{EXT} < 0.14/(250 + 150) \times 10^{-9}$$

$$< 350\ k\Omega$$

Choosing standard component values of 250 kΩ and 0.004μF would satisfy the above conditions.

We have just defined the limitation on the maximum size of R_{EXT}. There is a corresponding limit on the minimum size that R_{EXT} can assume. This is brought about because of the finite ON impedance of N1. As R_{EXT} is made smaller and smaller the amount of voltage across N1 becomes significant. The voltage across N1 is:

$$V_{N1} = V_{CC}\ r_{ON}/(R_{EXT} + r_{ON}) \qquad (4)$$

The output pulse width is defined by:

$$v(t_O) = (V_{CC} - V_{N1})(1 - e^{-t_O/R_{EXT} C_{EXT}}) + V_{N1} = 0.63 V_{CC}$$

Solving for t_O gives:

$$t_O = R_{EXT} C_{EXT} \ell n \left(\frac{V_{CC} - V_{N1}}{0.37 V_{CC}} \right)$$

Pulse Width Error is then:

$$\text{PW Error} = \frac{t_O - T}{T} \times 100\%$$

Substituting Equations 2 and 4 gives:

$$= \frac{R_{EXT} C_{EXT} \ell n \left(\frac{V_{CC} - V_{N1}}{0.37 V_{CC}} \right) - R_{EXT} C_{EXT} \ell n (1/0.37)}{R_{EXT} C_{EXT} \ell n (1/0.37)}$$

This function is plotted in *Figure 12* for r_{ON} of 50Ω, 25Ω and 16.7Ω. These are the typical values of r_{ON} for a V_{CC} of 5V, 10V and 15V respectively.

As an example, assume that the pulse width error due to r_{ON} must be less than 0.5% operating at V_{CC} = 5V. The typical value of r_{ON} for V_{CC} = 5V is 50Ω. Referring to the 50Ω curve in *Figure 12,* R_{EXT} must be greater than 10 kΩ to maintain this accuracy. At V_{CC} = 10V, R_{EXT} must be greater than 5 kΩ as can be seen from the 25Ω curve in *Figure 12.*

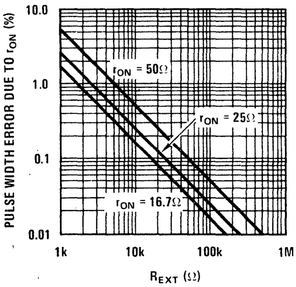
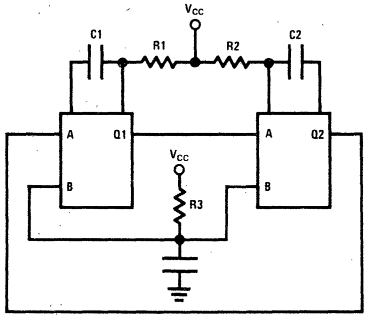


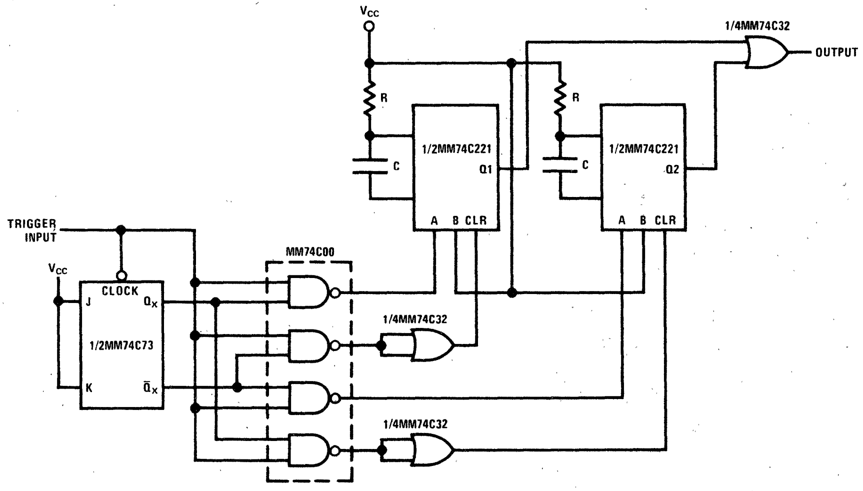
FIGURE 12. Percentage Pulse Width Error Due to Finite r_{ON} of Transistor N1 vs R_{EXT}.

Although clearly shown on the MM54C221/MM74C221 data sheet, it is worthwhile, for the sake of clarity, to point out that the parasitic capacitance between pins 7 (15) and 6 (14) is typically 15 pF. This capacitor is in parallel with C_{EXT} and must be taken into account when accuracy is critical.

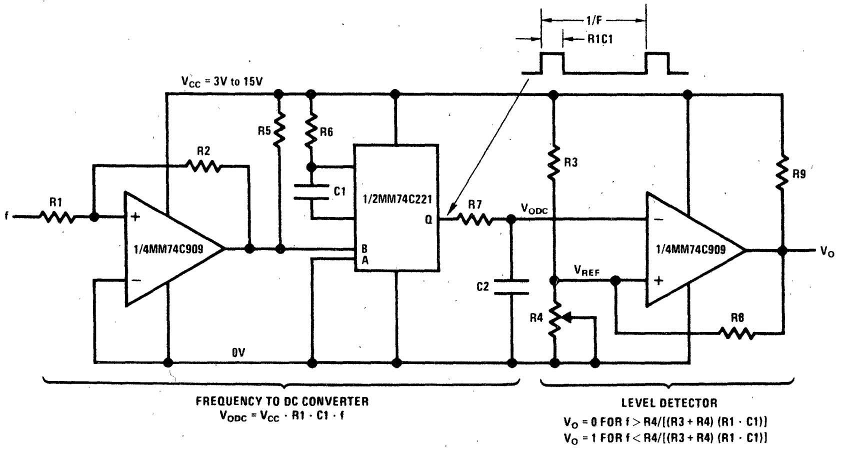
TYPICAL APPLICATIONS



Basic One-Shot Oscillator

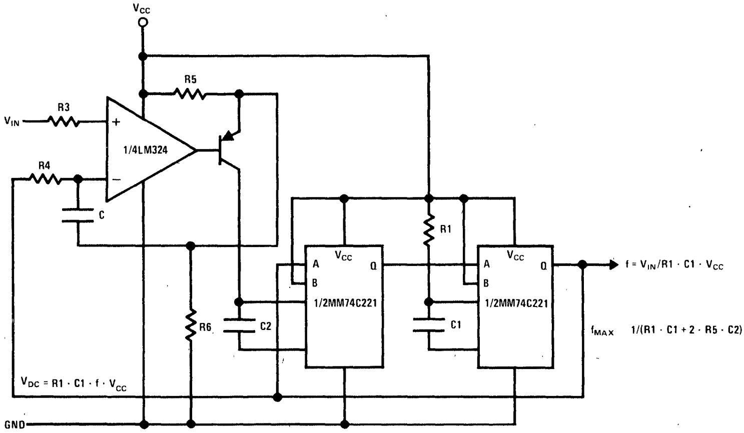


Retriggerable One-Shot

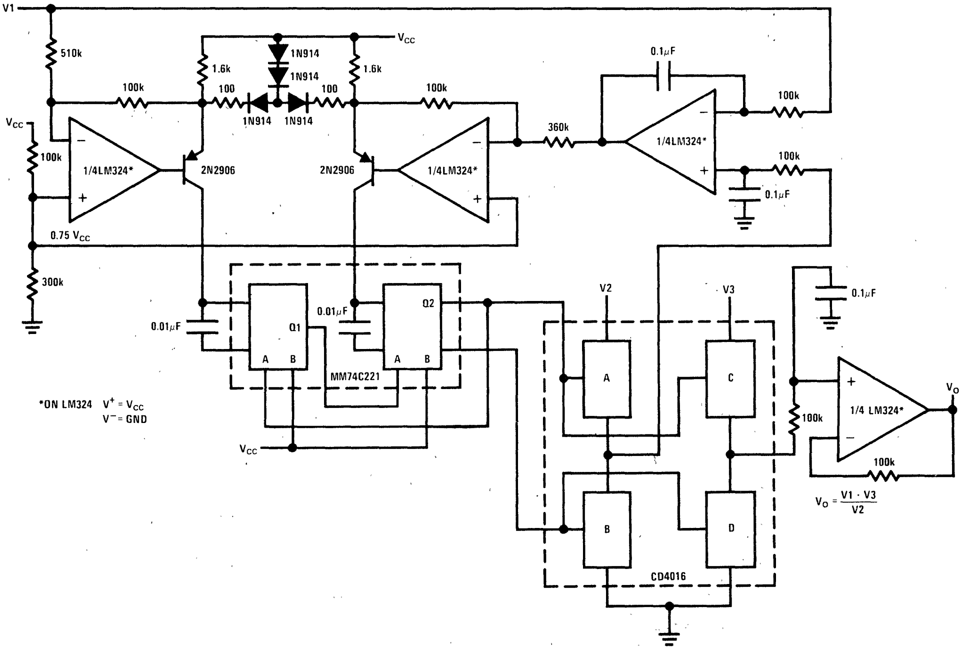


Frequency Magnitude Comparator

TYPICAL APPLICATIONS (Continued)



Linear VCO



Analog Multiplier/Divider

Gerald Buurma
National Semiconductor

CMOS SCHMITT TRIGGER
A UNIQUELY VERSATILE DESIGN COMPONENT

INTRODUCTION

The Schmitt trigger has found many applications in numerous circuits, both analog and digital. The versatility of a TTL Schmitt is hampered by its narrow supply range, limited interface capability, low input impedance and unbalanced output characteristics. The Schmitt trigger could be built from discrete devices to satisfy a particular parameter, but this is a careful and sometimes time-consuming design.

The CMOS Schmitt trigger, which comes six to a package, uses CMOS characteristics to optimize design and advance into areas where TTL could not go. These areas include: interfacing with op amps and transmission lines, which operate from large split supplies, logic level conversion, linear operation, and special designs relying on a CMOS characteristic. The CMOS Schmitt trigger has the following advantages:

- High impedance input ($10^{12}\Omega$ typical)
- Balanced input and output characteristics
  - Thresholds are typically symmetrical to 1/2 V_{CC}
  - Outputs source and sink equal currents
  - Outputs drive to supply rails
- Positive and negative-going thresholds show low variation with respect to temperature
- Wide supply range (3–15V), split supplies possible
- Low power consumption, even during transitions
- High noise immunity, 0.70 V_{CC} typical

Applications demonstrating how each of these characteristics can become a design advantage will be given later in the application note.

ANALYZING THE CMOS SCHMITT

The input of the Schmitt trigger goes through a standard input protection and is tied to the gates of four stacked devices. The upper two are P-channel and the lower two are N-channel. Transistors P3 and N3 are operating in the source follower mode and introduce hysteresis by feeding back the output voltage, out', to two different points in the stack.

When the input is at 0V, transistors P1 and P2 are ON, and N1, N2 and P3 are OFF. Since out' is high, N3 is ON and acting as a source follower, the drain of N1, which is the source of N2, is at $V_{CC}-V_{TH}$. If the input voltage is ramped up to one threshold above ground transistor N1 begins to turn ON, N1 and N3 both being ON form a voltage divider network biasing the source of N2 at roughly half the supply. When the input is a threshold above 1/2 V_{CC}, N2 begins to turn ON and regenerative switching is about to take over. Any more voltage on the input causes out' to drop. When out' drops, the source of N3 follows its gate, which is out', the influence of N3 in the voltage divider with N1 rapidly diminishes, bringing out' down further yet. Meanwhile P3 has started to turn ON, its gate being brought low by the rapidly dropping out'. P3 turning ON brings the source of P2 low and turns P2 OFF. With P2 OFF, out' crashes down. The snapping action is due to greater than unity loop gain through the stack caused by positive feedback through the source follower transistors. When the input is brought low again an identical process occurs in the upper portion of the stack and the snapping action takes place when the lower threshold is reached.

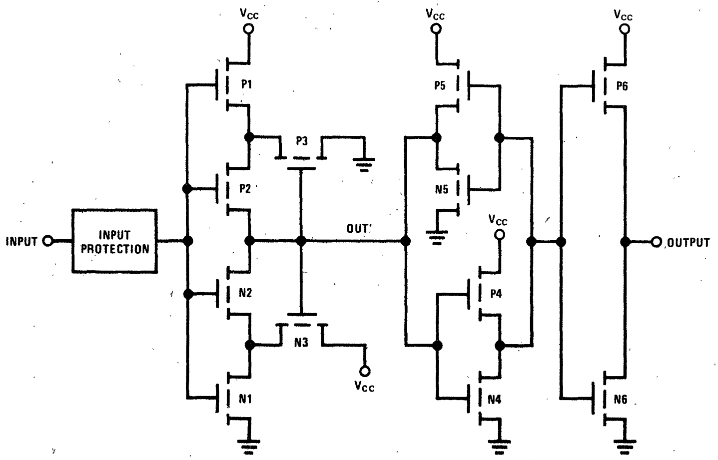


FIGURE 1. CMOS Schmitt Trigger

Out' is fed into the inverter formed by P4 and N4; another inverter built with very small devices, P5 and N5, forms a latch which stabilizes out'. The output is an inverting buffer capable of sinking 360µA or two LPTTL loads.

The typical transfer characteristics are shown in *Figure 2;* the guaranteed trip point range is shown in *Figure 3.*

WHAT HYSTERESIS CAN DO FOR YOUR

Hysteresis is the difference in response due to the direction of input change. A noisy signal that traverses the threshold of a comparator can cause multiple transitions at the output, if the response time of the comparator is less than the time between spurious effects. A Schmitt trigger has two thresholds: any spurious effects must be greater than the threshold difference to cause multiple transitions. With a CMOS Schmitt at V_{CC} = 10V there is typically 3.6V of threshold difference, enough hysteresis to overcome almost any spurious signal on the input.

A comparator is often used to recover information sent down an unbalanced transmission line. The threshold of the comparator is placed at one half the signal amplitude (See *Figure 4b*). This is doen to prevent slicing level distortion. If a 4µs wide signal is sent down a transmission line a 4µs wide signal should be received or signal distortion occurs. If the comparator has a threshold above half the signal amplitude, then positive pulses sent are shorter and negative pulses are lengthened (See *Figure 4c*). This is called slicing level distortion. The Schmitt trigger does have a positive offset, V_{T+}, but it also has a negative offset V_{T-}. In CMOS these offsets are approximately symmetrical to half the signal level so a 4µs wide pulse sent is also recovered (see *Figure 4d*). The recovered pulse is delayed in time but the length is not changed, so noise immunity is achieved and signal distortion is not introduced because of threshold offsets.

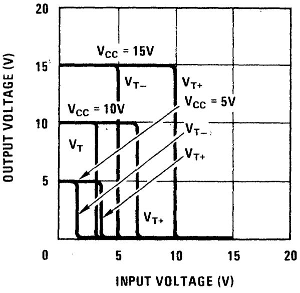


FIGURE 2. Typical CMOS Transfer Characteristics for Three Different Supply Voltages.

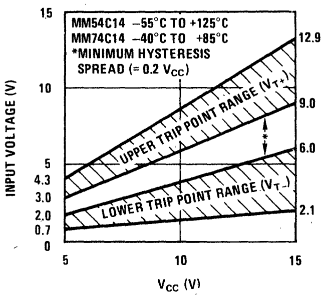
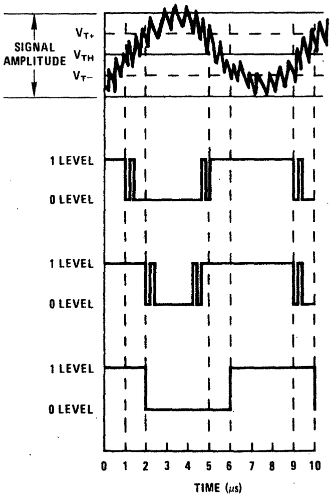


FIGURE 3. Guaranteed Trip Point Range.



a) Received signal from transmission line with thresholds at different amplitudes.

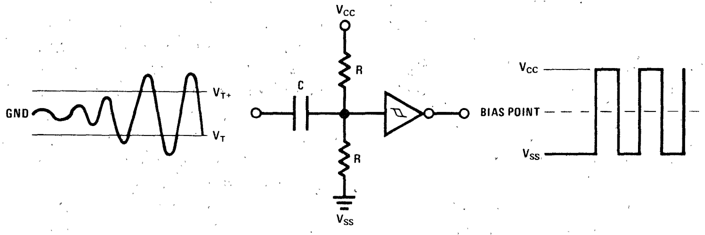
b) Recovered signal from comparator with threshold V_{TH} has multiple transitions.

c) Recovered signal from comparator with positive offset on threshold, V_{T+}, positive pulse shorten, negative pulse lengthen.

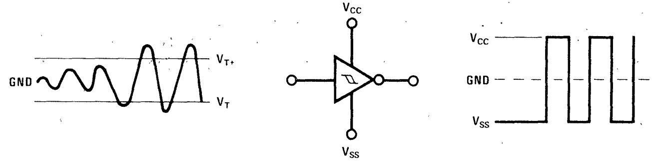
d) Recovered signal with CMOS Schmitt trigger, V_{T+} and V_{T} . Restores true waveform.

Recovered signal from Schmitt is same width as comparator with threshold at V_{TH}, and is only delayed in time.

FIGURE 4. CMOS Schmitt Trigger Ignores Noise

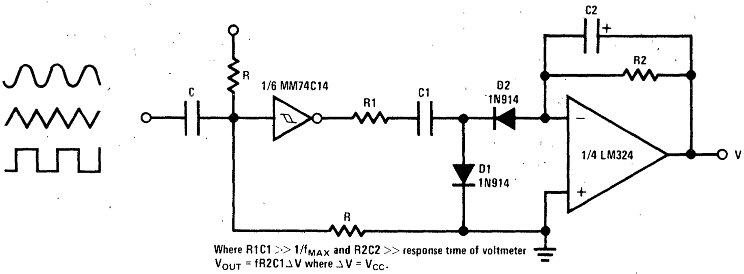


a) Capacitor impedance at lowest operating frequency should be much less than R R = 1/2 R.



b) By using split supply (±1.5 to ±7.5) direct interface is achieved.

FIGURE 5. Sine to Square Wave Converter with Symmetrical Level Detection.



Where $R1C1 >> 1/f_{MAX}$ and $R2C2 >>$ response time of voltmeter
$V_{OUT} = fR2C1\Delta V$ where $\Delta V = V_{CC}$.

FIGURE 6. Diode Dump Tach Accepts any Input Waveform.

APPLICATIONS OF THE CMOS SCHMITT

Most of the following applications use a CMOS Schmitt characteristic to either simplify design or increase performance. Some of the applications could not be done at all with another logic family.

The circuit in *Figure 5a* is the familiar sine to square wave converter. Because of input symmetry the Schmitt trigger is easily biased to achieve a 50% duty cycle. The high input impedance simplifies the selection of the biasing resistors and coupling capacitor. Since CMOS has a wide supply range the Schmitt trigger could be powered from split supplies (see *Figure 5b*). This biases the mean threshold value around zero and makes direct coupling from an op amp output possible.

In *Figure 4*, we see a frequency to voltage converter that accepts many waveforms with no change in output voltage. Although the energy in the waveforms are quite different, it is only the frequency that determines the output voltage. Since the output of the CMOS Schmitt pulls completely to the supply rails, a constant voltage swing across capacitor C1 causes a current to flow through the capacitor, dependent only on frequency. On positive output swings, the current is dumped to ground through D1. On negative output swings, current is pulled from the inverting op amp node through D2 and transformed into an average voltage by R2 and C2.

Since the CMOS Schmitt pulls completely to the supply rails the voltage change across the capacitor is just the supply voltage.

Schmitt triggers are often used to generate fast transitions when a slowly varying function exceeds a predetermined level. In *Figure 7*, we see a typical circuit, a light activated switch. The high impedance input of the CMOS Schmitt trigger makes biasing very easy. Most photo cells are several kΩ brightly illuminated and a couple MΩ dark. Since CMOS has a $10^{12}\Omega$ typical input impedance, no effects are felt on the input when the output changes. The selection of the biasing resistor is just the solution of a voltage divider equation.

A CMOS application note wouldn't be complete without a low power application. *Figure 8* shows a simple RC oscillator. With only six R's and C's and one Hex CMOS trigger, six low power oscillators can be built. The square wave output is approximately 50% duty cycle because of the balanced input and output characteristics of CMOS. The output frequency equation assumes that $t_1 = t_2 >> t_{pd0} + t_{pd1}$.

We earlier saw how the CMOS Schmitt increased noise immunity on an unbalanced transmission line. *Figure 9* shows an application for a balanced or differential transmission line. The circuit in *Figure 7a* is CMOS EXCLUSIVE OR, the MM74C86, which could also be built from inverters, and NAND gates. If unbalanced information is generated on the line by signal crosstalk or external noise sources, it is recognized as an error.

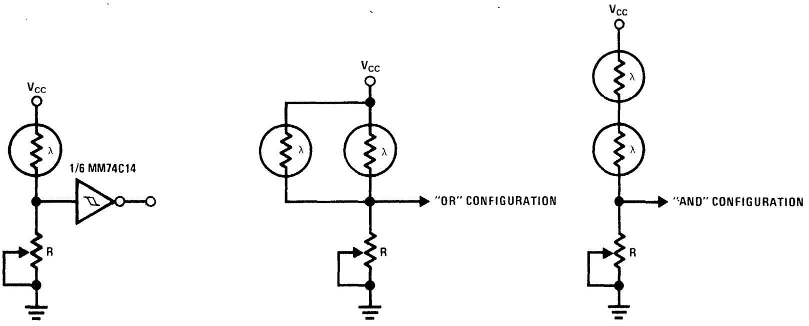
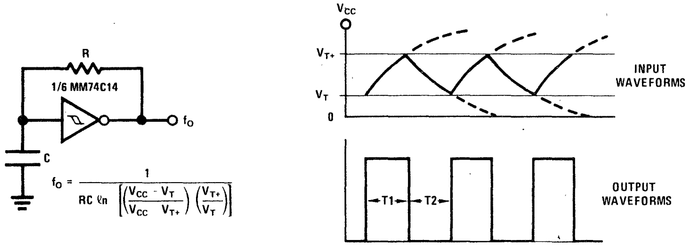
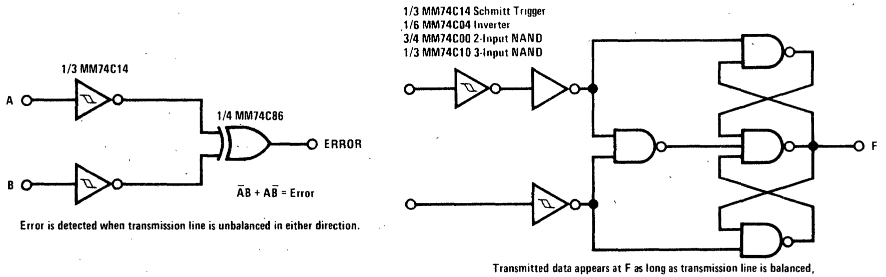


FIGURE 7. Light Activated Switch couldn't be Simpler. The Input Voltage Rises as Light Intensity Increases, when V_{T+} is Reached, the Output will go Low and Remain Low until the Intensity is Reduced Significantly.



$$f_O = \frac{1}{RC\,\ell n\left[\left(\frac{V_{CC}-V_T}{V_{CC}-V_{T+}}\right)\left(\frac{V_{T+}}{V_T}\right)\right]}$$

FIGURE 8. Simplest RC Oscillator? Six R's and C's make the CMOS Schmitt into Six Low Power Oscillators. Balanced Input and Output Characteristics give the Output Frequency a Typically 50% Duty Cycle.



Error is detected when transmission line is unbalanced in either direction.

Transmitted data appears at F as long as transmission line is balanced, unbalanced data is ignored and error is detected by above circuit.

Truth Table

A	B	F
0	0	NC
0	1	0
1	0	1
1	1	NC

NC = No Change

a) Differential Error Detector.

b) Differential Line Receiver.

FIGURE 9. Increase Noise Immunity by using the CMOS Schmitt Trigger to Demodulate a Balanced Transmission Line.

The circuit in *Figure 9b* is a differential line receiver that recovers balanced transmitted data but ignores unbalanced signals by latching up. If both circuits of *Figure 9* were used together, the error detector could signal the transmitter to stop transmission and the line receiver would remember the last valid information bit when unbalanced signals persisted on the line. When balanced signals are restored, the receiver can pick up where it left off.

The standard voltage range for CMOS inputs is V_{CC} +0.3V and ground −0.3V. This is because the input protection network is diode clamped to the supply rails. Any input exceeding the supply rails either sources or sinks a large amount of current through these diodes. Many times an input voltage range exceeding this is desirable; for example, transmission lines often operate from ±12V and op amps from ±15V. A solution to this problem is found in the MM74C914. This new device has an uncommon input protection that allows the input signal to go to 25V above ground, and 25V below V_{CC}. This means that the Schmitt trigger in the sine to square wave converter, in *Figure 5b*, could be powered by ±1.5V supplies and still be directly compatible with an op amp powered by ±15V supplies.

A standard input protection circuit and the new input protection are shown in *Figure 10*. The diodes shown have a 35V breakdown. The input voltage can go positive until reverse biased D2 breaks down through forward bias D3, which is 35V above ground. The input voltage can go negative until reverse biased D1 breaks down through forward bias D2, which is 35V below V_{CC}. Adequate input protection against static charge is still maintained.

CMOS can be linear over a wide voltage range if proper consideration is paid to the biasing of the inputs. *Figure 11* shows a simple VCO made with a CMOS inverter, acting as an integrator, and a CMOS Schmitt, acting as a comparator with hysteresis. The inverter integrates the positive difference between its threshold and the input voltage V_{IN}. The inverter output ramps up until the positive threshold of the Schmitt trigger is reached. At that time, the Schmitt trigger output goes low, turning on the transistor through R_s and speeding up capacitor C_s. Hysteresis keeps the output low until the integrating capacitor C is discharged through R_D. Resistor R_D should be kept much smaller than RC to keep reset time negligible. The output frequency is given by

$$f_O = \frac{V_{TH} - V_{IN}}{(V_{T+} - V_{T-})\ R_{CC}}.$$

The frequency dependence with control voltage is given by the derivative with respect to V_{IN} So,

$$\frac{d\,f_O}{d\,V_{IN}} = \frac{-1}{(V_{T+} - V_{T-})\ RC,}$$

where the minus sign indicates that the output frequency increases as the input is brought further below the inverter threshold. The maximum output frequency occurs when V_{IN} is at ground and the frequency will decrease as V_{IN} is raised up and will finally stop oscillating at the inverter threshold, approximately 0.55 V_{CC}.

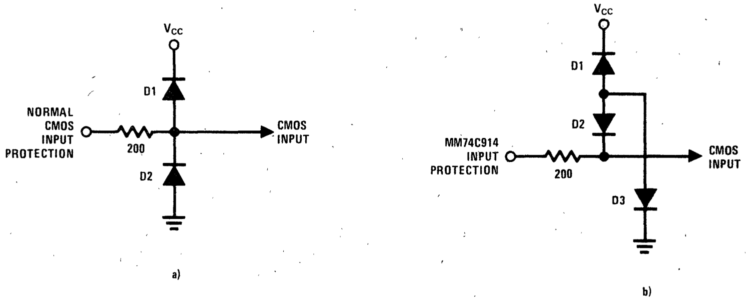


FIGURE 10. Input Protection Diodes, in a) Normally Limit the Input Voltage Swing to 0.3V above V_{CC} and 0.3V below Ground. In b) D2 or D1 is Reverse Biased Allowing Input Swings of 25V above Ground or 25V below V_{CC}.

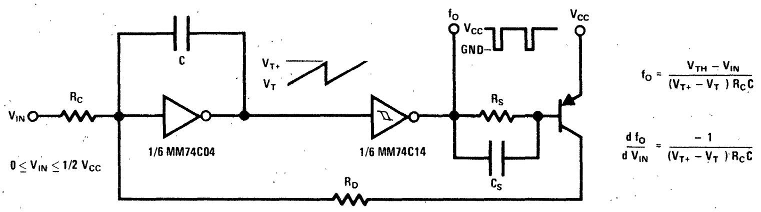


FIGURE 11. Linear CMOS.

The pulses from the VCO output are quite narrow because the reset time is much smaller than the integration time. Pulse stretching comes quite naturally to a Schmitt trigger. A one-shot or pulse stretcher made with an inverter and Schmitt trigger is shown in *Figure 12.* A positive pulse coming into the inverter causes its output to go low, discharging the capacitor through the diode D1. The capacitor is rapidly discharged, so the Schmitt input is brought low and the output goes positive. Check the size of the capacitor to make sure that inverter can fully discharge the capacitor in the input pulse time, or

$$I_{\text{SINK INVERTER}} > \frac{C\,\Delta V}{\Delta T} + \frac{\Delta V}{R}$$

where $\Delta V = V_{CC}$ for CMOS, and ΔT is the input pulse width.

For very narrow pulses, under 100 ns, the capacitor can be omitted and a large resistor will charge up the CMOS gate capacitance just like a capacitor.

When the inverter input returns to zero, the blocking diode prevents the inverter from charging the capacitor and the resistor must charge it from its supply. When the input voltage of the Schmitt reaches V_{T+}, the Schmitt output will go low sometime after the input pulse has gone low.

THE SCHMITT SOLUTION

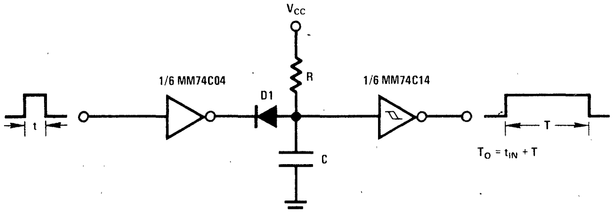
The Schmitt trigger, built from discrete parts, is a careful and sometimes time-consuming design. When introduced in integrated TTL, a few years ago, many circuit designers had renewed interest because it was a building block part. The input characteristics of TTL often make biasing of the trigger input difficult. The outputs don't source as much as they sink, so multivibrators don't have 50% duty cycle, and a limited supply range hampers interfacing with non 5V parts.

The CMOS Schmitt has a very high input impedance with thresholds approximately symmetrical to one half the supply. A high voltage input is available. The outputs sink and source equal currents and pull directly to the supply rails.

A wide threshold range, wide supply range, high noise immunity, low power consumption, and low board space make the CMOS Schmitt a uniquely versatile part.

Use the Schmitt trigger for signal conditioning, restoration of levels, discriminating noisy signals, level detecting with hysteresis, level conversion between logic families, and many other useful functions.

The CMOS Schmitt is one step closer to making design limited only by the imagination of the designer.



$$T = RC\,\ln\left(\frac{V_{CC} - V_{BE}}{V_{CC} - V_{T+}}\right) \quad \text{BE SURE THAT} \quad I_{\text{SINK INVERTER}} \quad \frac{C\,V_{CC}}{t} + \frac{V_{CC}}{R}$$

FIGURE 12. Pulse Stretcher. A CMOS Inverter Discharges a Capacitor, a Blocking Diode allows Charging through R only. Schmitt Trigger Output goes Low after the RC Delay.

John Jorgensen
Thomas P. Redfern
National Semiconductor

MM54C/MM74C VOLTAGE TRANSLATION/BUFFERING

INTRODUCTION

A new series of MM54C/MM74C buffers has been designed to interface systems operating at different voltage levels. In addition to performing voltage translation, the MM54C901/MM74C901 through MM54C904/MM74C904 hex buffers can drive two standard TTL loads at V_{CC} = 5V. This is an increase of ten times over the two LpTTL loads that the standard MM54C/MM74C gate can drive. These new devices greatly increase the flexibility of the MM54C/MM74C family when interfacing to other logic systems.

PMOS TO CMOS INTERFACE

Since most PMOS outputs normally can pull more negative than ground, the conventional CMOS input diode clamp from input to ground poses problems. The least of these is increased power consumption. Even though the output would be clamped at one diode drop (−0.6V), all the current that flows comes from the PMOS negative supply. For TTL compatible PMOS this is −12V. A PMOS output designed to drive one TTL load will typically sink 5 mA. The total power per TTL output is then 5 mA x 12V = 60 mW. The second problem is more serious. Currents of 5 mA or greater from a CMOS input clamp diode can cause four-layer diode action on the CMOS device. This, at best, will totally disrupt normal circuit operation and, at worst, will cause catastrophic failure.

To overcome this problem the MM74C903 and MM74C904 have been designed with a clamp diode from inputs to V_{CC} only. This single diode provides adequate static discharge protection and, at the same time, allows voltages of up to −17V on any input. Since there is essentially no current without the diode, both the high power dissipation and latch up problems are eliminated.

To demonstrate the above characteristics, *Figures 1, 2, and 3* show typical TTL compatible PMOS circuits driving standard CMOS with two clamp diodes, TTL compatible PMOS driving MM74C903/MM74C904, and the TTL compatible PMOS to CMOS system interface, respectively.

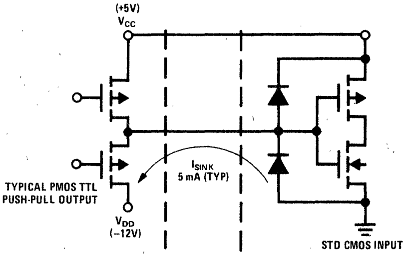


FIGURE 1.

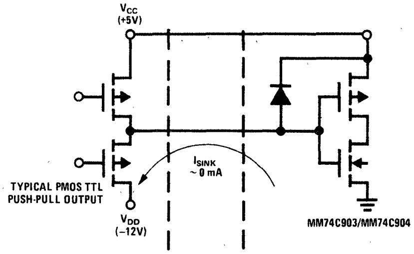


FIGURE 2.

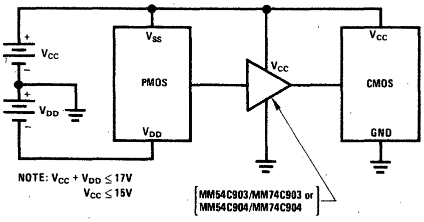


FIGURE 3. PMOS to CMOS or TTL Interface

CMOS TO CMOS OR TTL INTERFACE

When a CMOS system which is operating at V_{CC} = 10V must provide signals to a CMOS system whose V_{CC} = 5V, a problem similar to that found in PMOS-to-CMOS interface occurs. That is, current would flow through the upper input diode of the device operating at the lower V_{CC}. This current could be in excess of 10 mA on a typical 74C device, as shown in *Figure 4.* Again, this will cause increased power as well as possible four layer diode action.

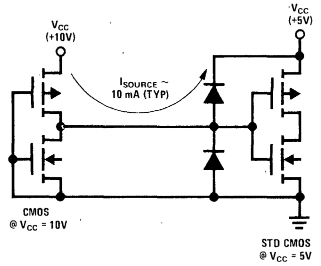


FIGURE 4.

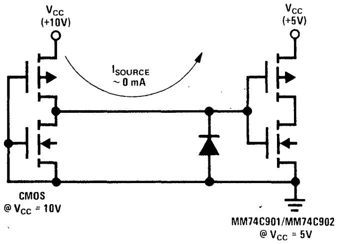
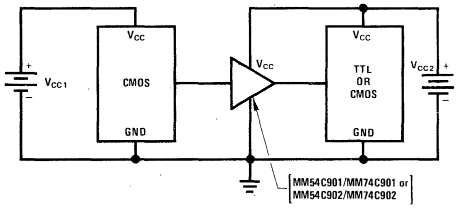


FIGURE 5.

Using the MM74C901 or MM74C902 will eliminate this problem. This occurs simply because these parts are designed with the upper diode removed, as shown in *Figure 5.* With this diode removed the current being sourced goes from about 10 mA to the leakage current of the reverse biased input diode.

Since the MM74C901 and MM74C902 are capable of driving two standard TTL loads with only normal input levels, the output can be used to directly drive TTL. With the example shown, the inputs of the MM74C901 are in excess of 5V. Therefore, they can drive more than two TTL loads. In this case the device would drive four loads with V_{IN} = 10V. If the MM74C902 were used, the output drive would not increase with increased input voltage. This is because the gate of the output n-channel device is always being driven by an internal inverter whose output equals that of V_{CC} of the device.

The example used was for systems of V_{CC} = 10V on one system and V_{CC} = 5V on the second, but the MM74C901 and MM74C902 are capable of using any combination of supplies up to 15V and greater than 3V, as long as V_{CC1} is greater than or equal to V_{CC2} and grounds are common. *Figure 6* diagrams this configuration.

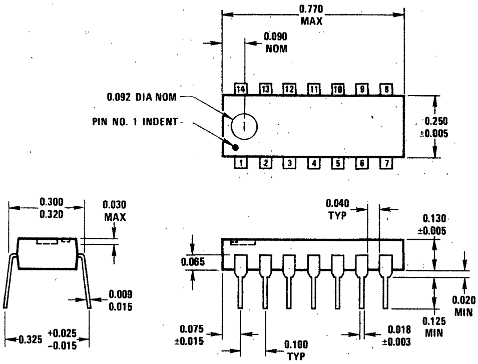


NOTE: $V_{CC1} \geq V_{CC2}$

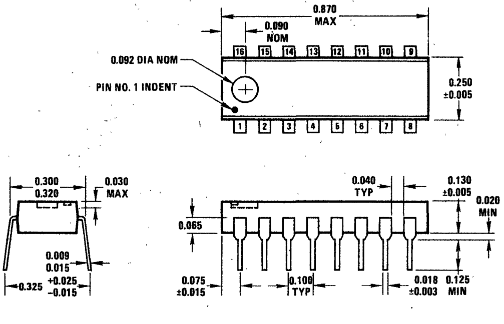
FIGURE 6. CMOS to TTL or CMOS at a Lower V_{CC}

The inputs on these devices are adequately protected with the single diode, but, as with all MOS devices, normal care in handling should be observed.

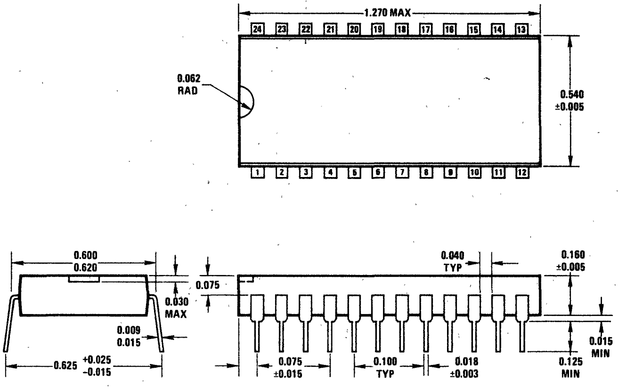
CMOS PACKAGES



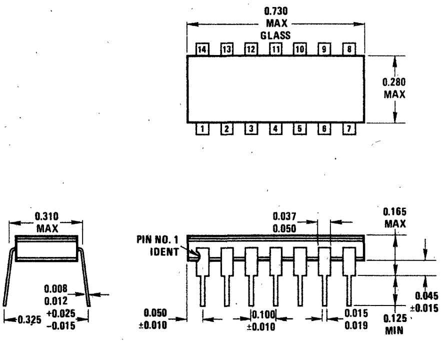
14 Lead Molded Dual-In-Line Package (N)



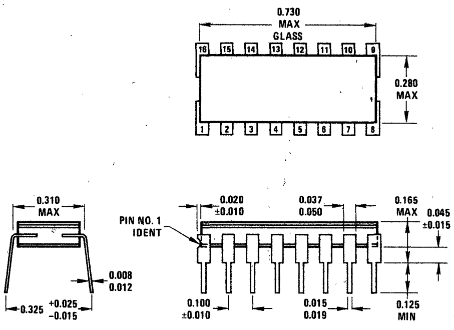
16 Lead Molded Dual-In-Line Package (N)



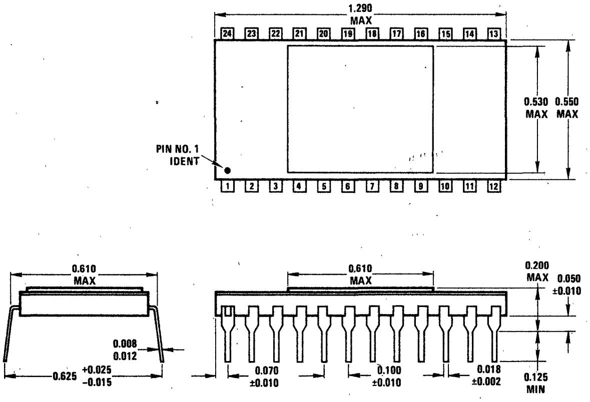
24 Lead Molded Dual-In-Line Package (N)



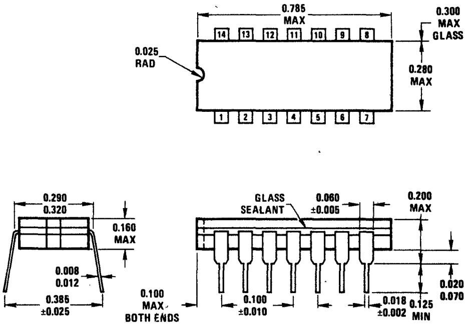
14 Lead Cavity Dual-In-Line Package (D)



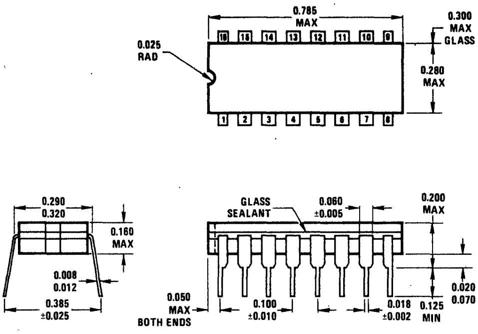
16 Lead Cavity Dual-In-Line Package (D)



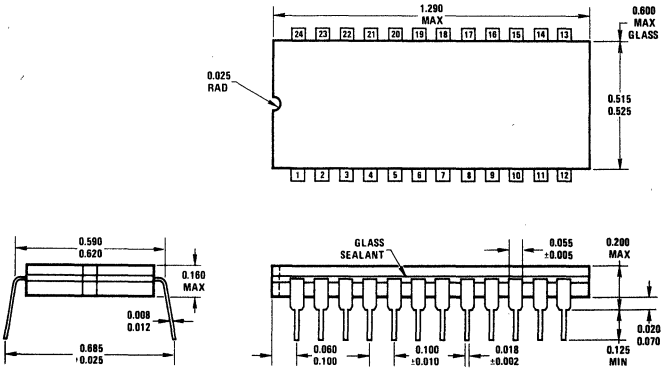
24 Lead Cavity Dual-In-Line Package (D)



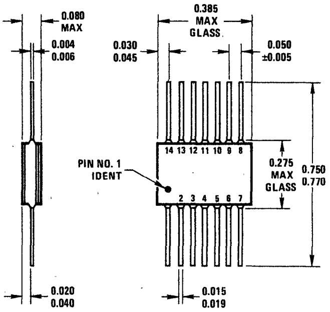
14 Lead Cavity Dual-In-Line Package (J)



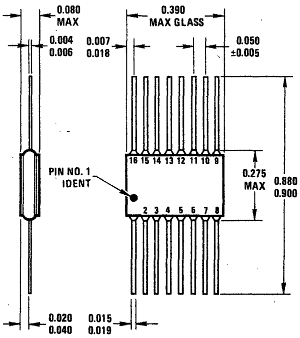
16 Lead Cavity Dual-In-Line Package (J)



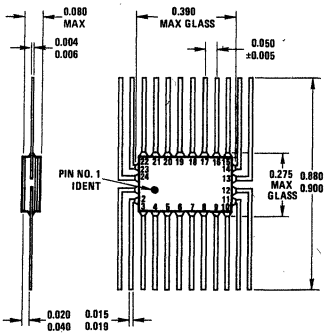
24 Lead Cavity Dual-In-Line Package (J)



14 Lead Flat Package (F)



16 Lead Flat Package (F)



24-Lead Flat Package (F)

INCHES TO MILLIMETERS CONVERSION TABLE					
INCHES	MM	INCHES	MM	INCHES	MM
0.001	0.0254	0.010	0.254	0.100	2.54
0.002	0.0508	0.020	0.508	0.200	5.08
0.003	0.0762	0.030	0.762	0.300	7.62
0.004	0.1016	0.040	1.016	0.400	10.16
0.005	0.1270	0.050	1.270	0.500	12.70
0.006	0.1524	0.060	1.524	0.600	15.24
0.007	0.1778	0.070	1.778	0.700	17.78
0.008	0.2032	0.080	2.032	0.800	20.32
0.009	0.2286	0.090	2.286	0.900	22.86

All package dimensions are in inches.

ORDERING INFORMATION

ORDER NUMBER	PACKAGE	TEMPERATURE RANGE
MM74CXXN	Molded DIP (N)	−40°C to +85°C
MM74CXXJ	Cavity DIP (J)	−40°C to +85°C
MM54CXXJ	Cavity DIP (J)	−55°C to +125°C
MM54CXXD	Cavity DIP (D)	−55°C to +125°C
MM54CXXF	Cavity Flat Pack (F)	−55°C to +125°C
MM80CXXN	Molded DIP (N)	−40°C to +85°C
MM80CXXJ	Cavity DIP (J)	−40°C to +85°C
MM70CXXJ	Cavity DIP (J)	−55°C to +125°C
MM70CXXD	Cavity DIP (D)	−55°C to +125°C
MM70CXXF	Cavity Flat Pack (F)	−55°C to +125°C

ORDER NUMBER	RCA EQUIVALENT DESIGNATION	PACKAGE	TEMPERATURE RANGE
CD40XXCN	CD40XXAE	Molded DIP (N)	−40°C to +85°C
CD40XXCJ		Cavity DIP (J)	−40°C to +85°C
CD40XXMJ	CD40XXAF	Cavity DIP (J)	−55°C to +125°C
CD40XXMD	CD40XXAD	Cavity DIP (D)	−55°C to +125°C
CD40XXMF	CD40XXAK	Cavity Flat Pack (F)	−55°C to +125°C
*CD45XXBCN	CD45XXBE	Molded DIP (N)	−40°C to +85°C
*CD45XXBCJ		Cavity DIP (J)	−40°C to +85°C
*CD45XXBMJ	CD45XXBF	Cavity DIP (J)	−55°C to +125°C
*CD45XXBMD	CD45XXBD	Cavity DIP (D)	−55°C to +125°C
*CD45XXBMF	CD45XXBK	Cavity Flat Pack (F)	−55°C to +125°C

*Equivalent to Motorola MC145XX Series