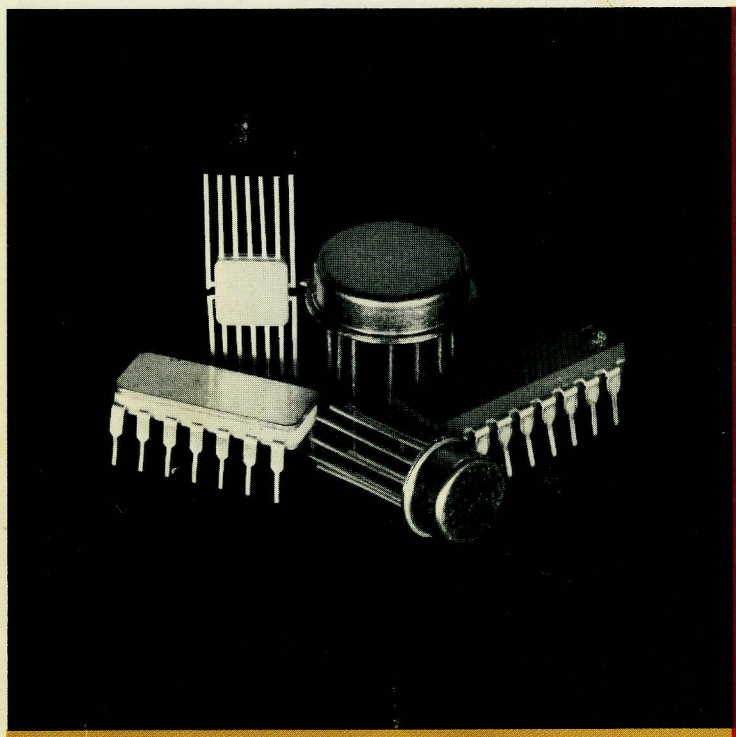
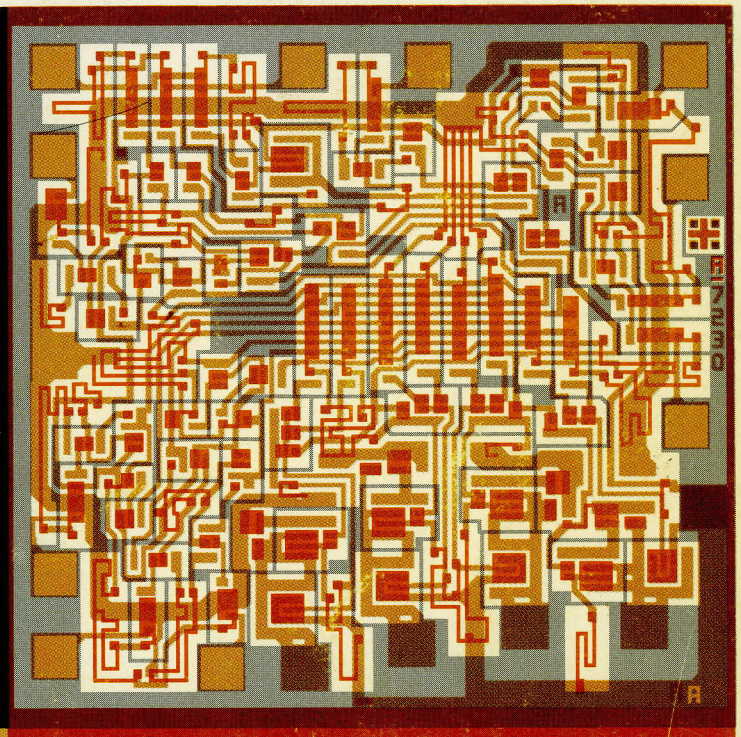
National Semiconductor Corporation

DIGITAL INTEGRATED CIRCUITS



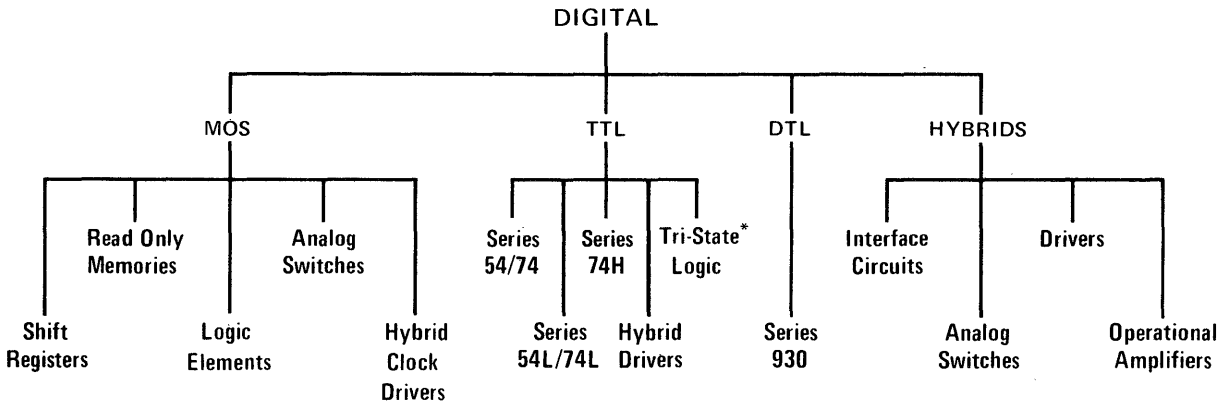


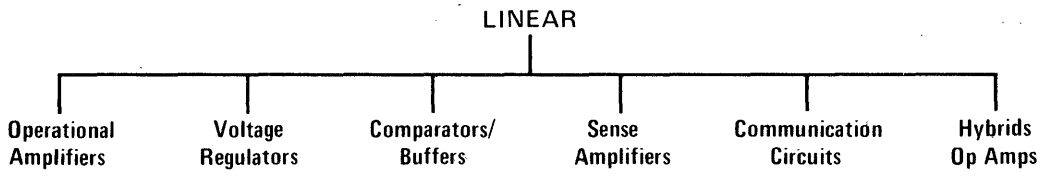
DIGITAL INTEGRATED CIRCUITS

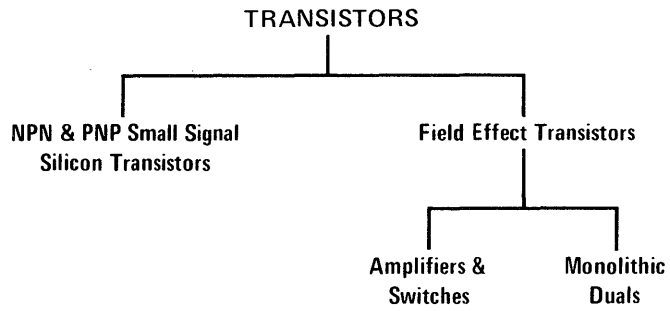
MAY 1971

Introduction

Here is National's latest catalog on Digital products. This catalog, and future ones on our major product lines, Linear ICs, MOS ICs, and Transistors, will be updated periodically by new product supplements. To keep current on our growing product lines, contact a National sales office, representative, or distributor, and ask to be placed on our mailing list.







*Trademark, National Semiconductor Corp.

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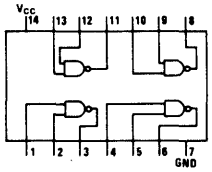
*Trade name of Burroughs Corp.

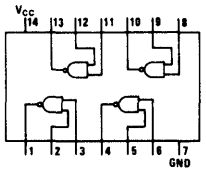
National TTL & Complex Functions

National's Series 54/74 devices and complex circuits are available in either cavity or molded DIPs.

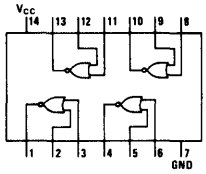
DM5400/DM7400
quad 2-input NAND gate



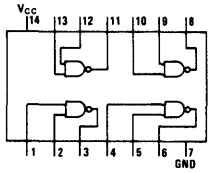
DM5401/DM7401
quad 2-input NAND gate



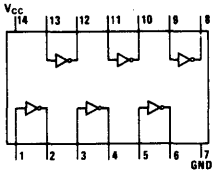
DM5402/DM7402
quad 2-input NOR gate



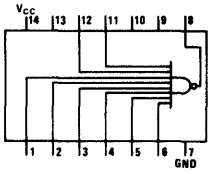
DM5403/DM7403
quad 2-input NAND gate



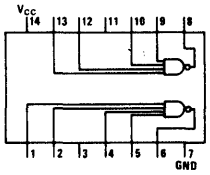
DM5404/DM7404
hex inverter



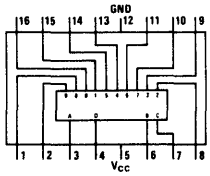
DM5430/DM7430
8-input NAND gate



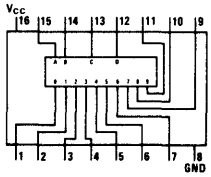
DM5440/DM7440
dual 4-input buffer



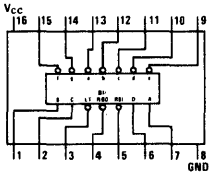
DM5441/DM7441
nixie* driver



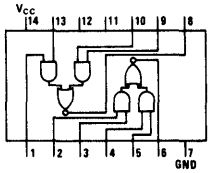
DM5442/DM7442
BCD to decimal decoder



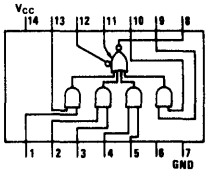
DM5446/DM7446
BCD to 7 seg. decoder/dvr



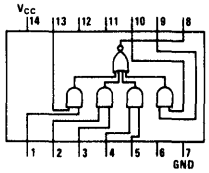
DM5451/DM7451
dual A-O-I gate



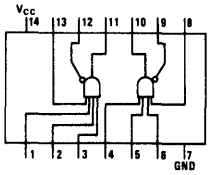
DM5453/DM7453
expandable A-O-I gate



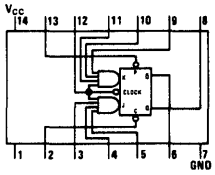
DM5454/DM7454
A-O-I gate



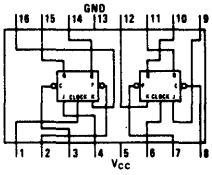
DM5460/DM7460
dual 4-input expander



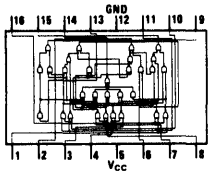
DM5472/DM7472
J-K m/s flip flop



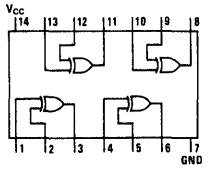
DM5476/DM7476
dual J-K flip flop



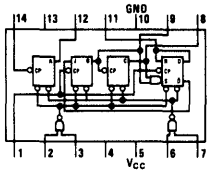
DM5483/DM7483
4 bit adder



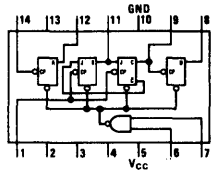
DM5486/DM7486
quad exclusive OR gate



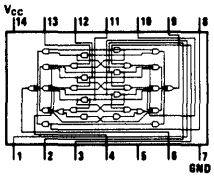
DM5490/DM7490
decade counter



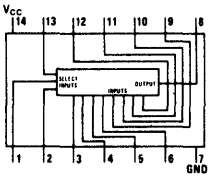
DM5492/DM7492
divide-by-twelve counter



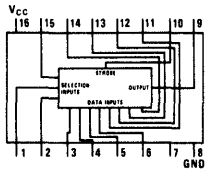
DM7200/DM8200
4 bit comparator



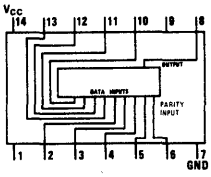
DM7210/DM8210
8 channel digital switch



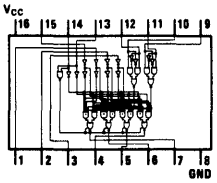
DM7211/DM8211
8 channel digital switch



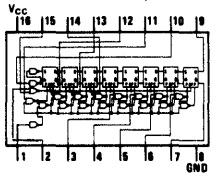
DM7220/DM8220
parity generator/checker



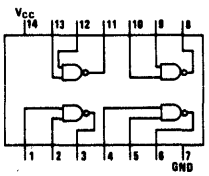
DM7230/DM8230
bus line demultiplexer



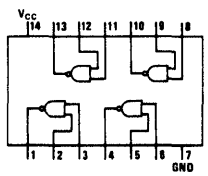
DM7590/DM8590
8 bit PI/SO register



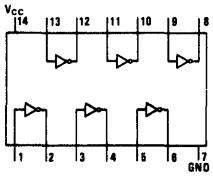
DM7810/DM8810
quad 2-input TTL-MOS gate



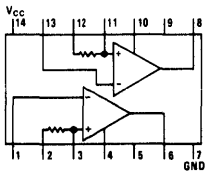
DM7811/DM8811
quad 2-input TTL-MOS gate



DM7812/DM8812
TTL-MOS hex inverter

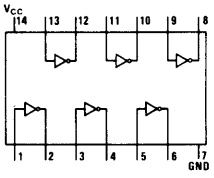


DM7820/DM8820
dual line receiver

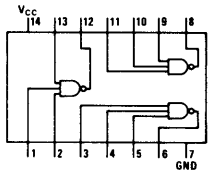


*Trade name of the Burroughs Corporation

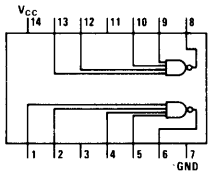
DM5405/DM7405
hex inverter



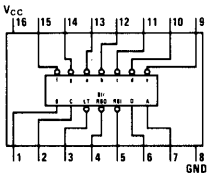
DM5410/DM7410
triple 3-input NAND gate



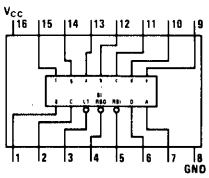
DM5420/DM7420
dual 4-input NAND gate



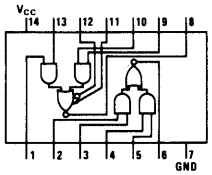
DM5447/DM7447
BCD to 7 seg. decoder/dvr.



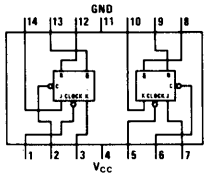
DM5448/DM7448
BCD to 7 seg. decoder



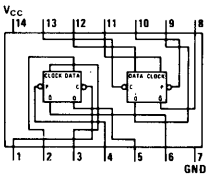
DM5450/DM7450
expandable A-O-I gate



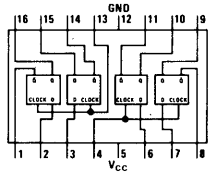
DM5473/DM7473
dual J-K flip flop



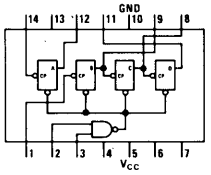
DM5474/DM7474
dual D flip flop



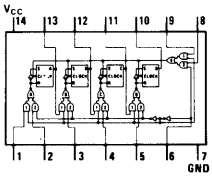
DM5475/DM7475
quad latch



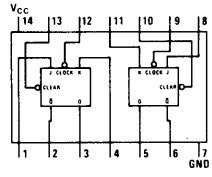
DM5493/DM7493
4 bit binary counter



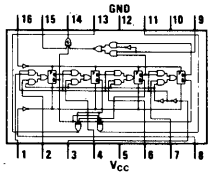
DM5495/DM7495
4 bit RS/LS register



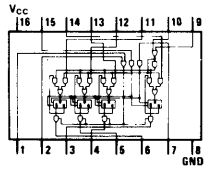
DM54107/DM74107
dual J-K m/s flip flop



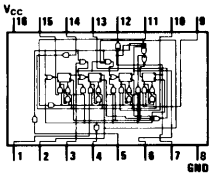
DM7520/DM8520
modulo-n divider



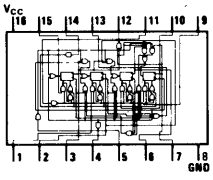
DM7551/DM8551
tri-state quad D flip flop



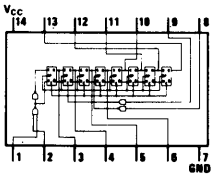
DM7560/DM8560
up/down decade counter



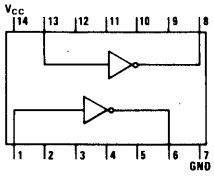
DM7563/DM8563
up/down binary counter



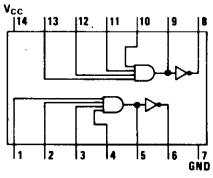
DM7570/DM8570
8 bit SI/PO register



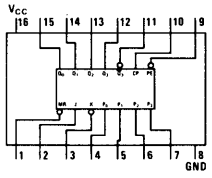
DM7822/DM8822
dual line receiver



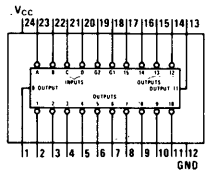
DM7830/DM8830
dual diff. line driver



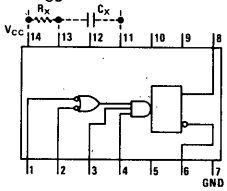
DM9300/DM8300
4 bit shift register



DM54154/DM74154
one of 16 decoder



DM9601/DM8601
retriggerable one shot



EQUIVALENT TABLE

Second Source Designation	New National Designation	Old National Designation
SN5400/SN7400	DM5400/DM7400	DM7000/DM8000
SN5401/SN7401	DM5401/DM7401	DM7001/DM8001
SN5402/SN7402	DM5402/DM7402	DM7002/DM8002
SN5403/SN7403	DM5403/DM7403	DM7003/DM8003
SN5404/SN7404	DM5404/DM7404	DM7004/DM8004
SN5405/SN7405	DM5405/DM7405	DM7005/DM8005
SN5410/SN7410	DM5410/DM7410	DM7010/DM8010
SN5420/SN7420	DM5420/DM7420	DM7020/DM8020
SN5430/SN7430	DM5430/DM7430	DM7030/DM8030
SN5440/SN7440	DM5440/DM7440	DM7040/DM8040
SN5441/SN7441	DM5441/DM7441	DM7840/DM8840
SN5442/SN7442	DM5442/DM7442	DM7842/DM8842
SN5446/SN7446	DM5446/DM7446	DM7846/DM8846
SN5447/SN7447	DM5447/DM7447	DM7847/DM8847
SN5448/SN7448	DM5448/DM7448	DM7848/DM8848
SN5450/SN7450	DM5450/DM7450	DM7050/DM8050
SN5451/SN7451	DM5451/DM7451	DM7051/DM8051
SN5453/SN7453	DM5453/DM7453	DM7053/DM8053
SN5454/SN7454	DM5454/DM7454	DM7054/DM8054
SN5460/SN7460	DM5460/DM7460	DM7060/DM8060
SN5472/SN7472	DM5472/DM7472	DM7540/DM8540
SN5473/SN7473	DM5473/DM7473	DM7501/DM8501
SN5474/SN7474	DM5474/DM7474	DM7510/DM8510
SN5475/SN7475	DM5475/DM7475	DM7550/DM8550
SN5476/SN7476	DM5476/DM7476	DM7500/DM8500
SN5483/SN7483	DM5483/DM7483	DM7283/DM8283
SN5486/SN7486	DM5486/DM7486	DM7086/DM8086
SN5490/SN7490	DM5490/DM7490	DM7530/DM8530
SN5492/SN7492	DM5492/DM7492	DM7532/DM8532
SN5493/SN7493	DM5493/DM7493	DM7533/DM8533
SN5495/SN7495	DM5495/DM7495	DM7580/DM8580
SN54107/SN74107	DM54107/DM74107	DM7502/DM8502
SN54192/SN74192	DM7560/DM8560	DM7560/DM8560
SN54193/SN74193	DM7563/DM8563	DM7563/DM8563
SN54154/SN74154	DM54154/DM74154	DM7213/DM8213
9300-51/9300-59	DM9300/DM8300	DM7600/DM8600
9601-51/9601-59	DM9601/DM8601	DM7850/DM8850

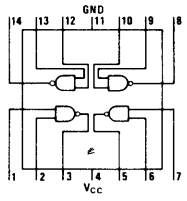
UNIQUELY NATIONAL

DM7200/DM8200	DM7520/DM8520	DM7811/DM8811
DM7210/DM8210	DM7551/DM8551	DM7812/DM8812
DM7211/DM8211	DM7570/DM8570	DM7820/DM8820
DM7220/DM8220	DM7590/DM8590	DM7822/DM8822
DM7230/DM8230	DM7810/DM8810	DM7830/DM8830

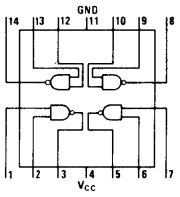
National Low Power TTL

Low power TTL devices are available in either the 1/4" x 1/4" flat package (shown as a square configuration) or the cavity or molded DIP (shown as a rectangular configuration).

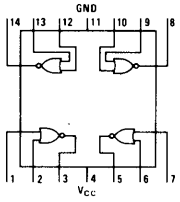
DM54L00/DM74L00
quad 2-input NAND gate



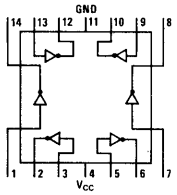
DM54L01/DM74L01
quad 2-input NAND gate



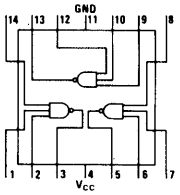
DM54L02/DM74L02
quad 2-input NOR gate



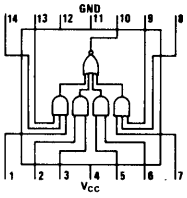
DM54L04/DM74L04
hex inverter



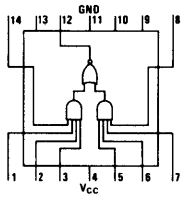
DM54L10/DM74L10
triple 3-input NAND gate



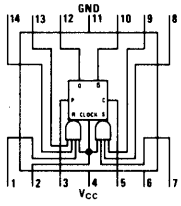
DM54L54/DM74L54
4-w 3-2-2-3 input A-O-I gate



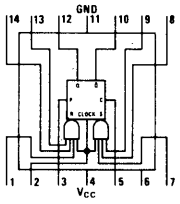
DM54L55/DM74L55
2 wide 4-input A-O-I gate



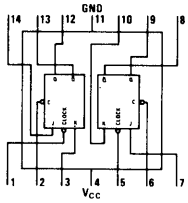
DM54L71/DM74L71
R-S m/s flip flop



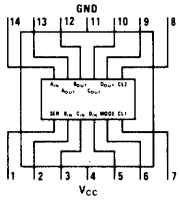
DM54L72/DM74L72
J-K m/s flip flop



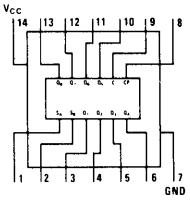
DM54L73/DM74L73
dual J-K m/s flip flop



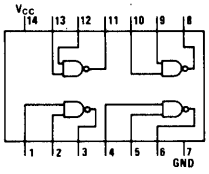
DM54L95/DM74L95
4 bit PI/PO shift register



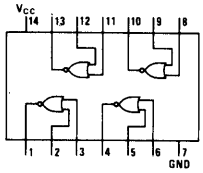
DM76L70/DM86L70
8 bit SI/PO shift register



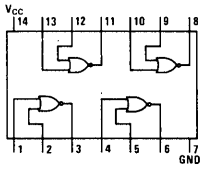
DM74L00
quad 2-input NAND gate



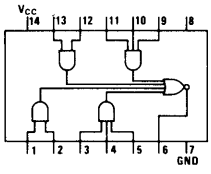
DM74L02
quad 2-input NOR gate



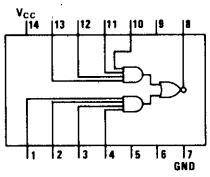
DM74L03
quad 2-input NAND gate



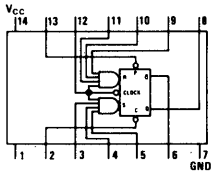
DM74L54
4-w 3-2-2-3 input A-O-I gate



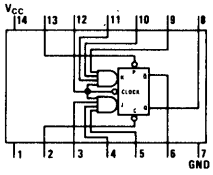
DM74L55
2-wide 4-input A-O-I gate



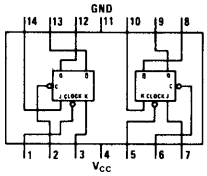
DM74L71
R-S m/s flip flop



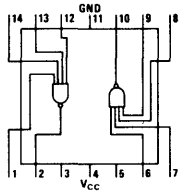
DM74L72
J-K m/s flip flop



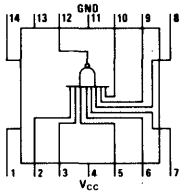
DM74L73
dual J-K m/s flip flop



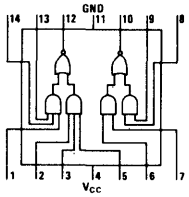
DM54L20/DM74L20
dual 4-input NAND gate



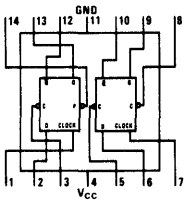
DM54L30/DM74L30
8-input NAND gate



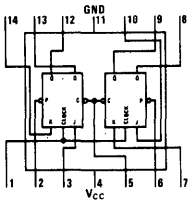
DM54L51/DM74L51
dual 2-wide A-O-I gate



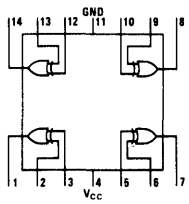
DM54L74/DM74L74
dual D flip flop



DM54L78/DM74L78
dual J-K m/s flip flop



DM54L86/DM74L86
quad 2-input excl. OR gate



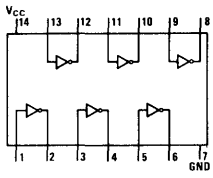
EQUIVALENT TABLE

Second Source Designation	New National Designation	Old National Designation
SN54L00/SN74L00	DM54L00/DM74L00	DM70L00/DM80L00
SN54L01/SN74L01	DM54L01/DM74L01	DM70L01/DM80L01
SN54L02/SN74L02	DM54L02/DM74L02	DM70L02/DM80L02
SN54L03/SN74L03	DM54L03/DM74L03	DM70L03/DM80L03
SN54L04/SN74L04	DM54L04/DM74L04	DM70L04/DM80L04
SN54L10/SN74L10	DM54L10/DM74L10	DM70L10/DM80L10
SN54L20/SN74L20	DM54L20/DM74L20	DM70L20/DM80L20
SN54L30/SN74L30	DM54L30/DM74L30	DM70L30/DM80L30
SN54L51/SN74L51	DM54L51/DM74L51	DM70L51/DM80L51
SN54L54/SN74L54	DM54L54/DM74L54	DM70L54/DM80L54
SN54L55/SN74L55	DM54L55/DM74L55	DM70L55/DM80L55
SN54L71/SN74L71	DM54L71/DM74L71	DM75L71/DM85L71
SN54L72/SN74L72	DM54L72/DM74L72	DM75L72/DM85L72
SN54L73/SN74L73	DM54L73/DM74L73	DM75L73/DM85L73
SN54L74/SN74L74	DM54L74/DM74L74	DM75L74/DM85L74
SN54L78/SN74L78	DM54L78/DM74L78	DM75L78/DM85L78
SN54L86/SN74L86	DM54L86/DM74L86	DM70L86/DM80L86
SN54L95/SN74L95	DM54L95/DM74L95	DM75L95/DM85L95

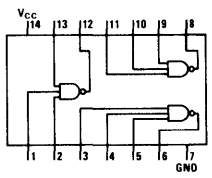
UNIQUELY NATIONAL

DM76L70/DM86L70

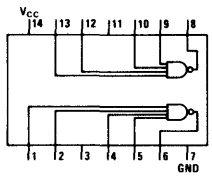
DM74L04
hex inverter



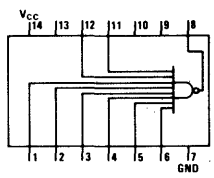
DM74L10
triple 3-input NAND gate



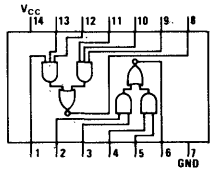
DM74L20
dual 4-input NAND gate



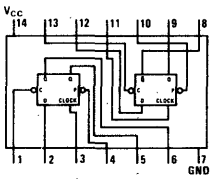
DM74L30
8-input NAND gate



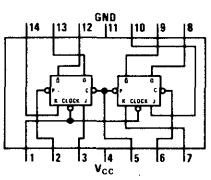
DM74L51
dual 2-wide A-O-I gate



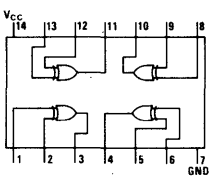
DM74L74
dual D flip flop



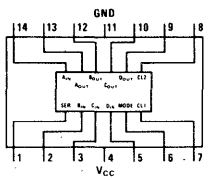
DM74L78
dual J-K m/s flip flop



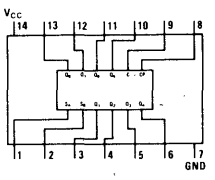
DM74L86
quad 2-input excl. OR gate



DM74L95
4-bit PI/PO shift register



DM86L70
8-bit SI/PO shift register



Package / Temperature Guide

Flat Package (F)		Cavity Dual-In-Line Package (D)		Molded Dual-In-Line Package (N)	
−55°C to +125°C	0°C to 70°C	−55°C to +125°C	0°C to 70°C	−55°C to +125°C	0°C to 70°C
		DM5400		DM5400	DM7400
		DM5401		DM5401	DM7401
		DM5402		DM5402	DM7402
		DM5403		DM5403	DM7403
		DM5404		DM5404	DM7404
		DM5405		DM5405	DM7405
		DM5408		DM5408	DM7408
		DM5409		DM5409	DM7409
		DM5410		DM5410	DM7410
		DM5411		DM5411	DM7411
		DM5413		DM5413	DM7413
		DM5420		DM5420	DM7420
					DM7426
		DM5430		DM5430	DM7430
		DM5432		DM5432	DM7432
		DM5440		DM5440	DM7440
		DM5441A			DM7441A
		DM5442			DM7442
		DM5446			DM7446
		DM5447			DM7447
		DM5448			DM7448
		DM5450		DM5450	DM7450
		DM5451		DM5451	DM7451
		DM5453		DM5453	DM7453
		DM5454		DM5454	DM7454
		DM5460		DM5460	DM7460
		DM5472		DM5472	DM7472
		DM5473		DM5473	DM7473
		DM5474		DM5474	DM7474
		DM5475		DM5475	DM7475
		DM5476		DM5476	DM7476
		DM5483			DM7483
		DM5486		DM5486	DM7486
		DM5488			DM7488
		DM5489			DM7489
		DM5490		DM5490	DM7490
		DM5492		DM5492	DM7492
		DM5493		DM5493	DM7493
		DM5495			DM7495
		DM5496			DM7496
		DM54107		DM54107	DM74107
		DM54153			DM74153
		DM54154			DM74154
		DM7090		DM7090	DM8090
		DM7091		DM7091	DM8091
		DM7093		DM7093	DM8093
		DM7094		DM7094	DM7094
		DM7200		DM7200	DM7200
		DM7210		DM7220	DM7210
		DM7211			DM7211
		DM7214			DM8214
		DM7220			DM8220
		DM7230			DM8230
		DM7280			DM8280
		DM7281			DM8281
		DM7288			DM8288
		DM7520			DM8520
		DM7551			DM8551
		DM7560			DM8560
		DM7563			DM8563
		DM7570			DM8570
		DM7590			DM8590
		DM7595			DM8595
		DM7598			DM8598
		DM7810		DM7810	DM8810
		DM7811		DM7811	DM8811
		DM7812		DM7812	DM8812
		DM7819		DM7819	DM8819
		DM7820A			DM8820A

Note: The DM7800/DM8800 is available in a 10-pin metal can package only.

Flat Package (F)		Cavity Dual-In-Line Package (D)		Molded Dual-In-Line Package (N)	
−55°C to +125°C	0°C to 70°C	−55°C to +125°C	0°C to 70°C	−55°C to +125°C	0°C to 70°C
		DM7822			DM8822
		DM7830			DM8830
		DM7831			DM8831
		DM9300	DM8300		DM8300
		DM9601	DM8601	DM9601	DM8601
DM54L00	DM74L00	DM54L00		DM54L00	DM74L00
DM54L01	DM74L01				
DM54L02	DM74L02	DM54L02		DM54L02	DM74L02
		DM54L03		DM54L03	DM74L03
DM54L04	DM74L04	DM54L04		DM54L04	DM74L04
DM54L10	DM74L10	DM54L10		DM54L10	DM74L10
DM54L20	DM74L20	DM54L20		DM54L20	DM74L20
DM54L30	DM74L30	DM54L30		DM54L30	DM74L30
DM54L51	DM74L51	DM54L51		DM54L51	DM74L51
DM54L54	DM74L54	DM54L54		DM54L54	DM74L54
DM54L55	DM74L55	DM54L55		DM54L55	DM74L55
DM54L71	DM74L71	DM54L71		DM54L71	DM74L71
DM54L72	DM74L72	DM54L72		DM54L72	DM74L72
DM54L73	DM74L73	DM54L73		DM54L73	DM74L73
DM54L74	DM74L74	DM54L74		DM54L74	DM74L74
DM54L78	DM74L78	DM54L78		DM54L78	DM74L78
DM54L86	DM74L86	DM54L86		DM54L86	DM74L86
DM54L90	DM74L90	DM54L90		DM54L90	DM74L90
DM54L93	DM74L93	DM54L93		DM54L93	DM74L93
DM54L95	DM74L95	DM54L95		DM54L95	DM74L95
					DM80L06
DM76L70	DM86L70	DM76L70		DM76L70	DM86L70
					DM74H00
					DM74H01
					DM74H04
					DM74H05
					DM74H08
					DM74H10
					DM74H11
					DM74H20
					DM74H21
					DM74H22
					DM74H30
					DM74H40
					DM74H50
					DM74H51
					DM74H52
					DM74H53
					DM74H54
					DM74H55
					DM74H60
					DM74H61
					DM74H62
					DM930
					DM932
					DM933
					DM935
					DM936
					DM937
					DM944
					DM945
					DM946
					DM948
					DM949
					DM957
					DM958
					DM961
					DM962
					DM963
					DM9093
					DM9094
					DM9097
					DM9099
					DM1800
					DM1801

Tri-State Logic

TTL-5

TRI-STATE LOGIC

INTRODUCTION

Occasionally, as a new concept matures, it often times loses some of the desirable features it possessed in its infancy. Such is the case with bipolar digital integrated circuits. When digital IC's entered the age of TTL, the ability to wire – OR or "bus" was lost. In systems design where this logic mode was required, however, the designer was forced to return to the older DTL output structure (passive pull-up) by utilizing open collector TTL devices. Effectively, most of the advantages of TTL were lost by going this route. Recognizing this obvious loss to the designer, National Semiconductor has committed itself to developing an entirely new concept in TTL. It, in fact, is the next level of maturity in digital IC's and it is here today. We, at National, call it Tri-State Logic. It may be referred to, at times, as bus – organized TTL, wire – OR'able TTL, or even bus OR'able logic. The "WIRE-OR" designation is commonly used with this type of concept, although in the case of tri-state logic no Boolean function is achieved. "Tri-State" basically defines a logic element which has three distinct output states: Zero, One (normal TTL levels) and OFF wherein an OFF state represents a high impedance condition which can neither sink nor source current at a definable logic level. At most, it may require 40 μA leakage current to be supplied to it from other devices connected to the same output line, or it may supply up to 40 μA current to another device on the line.

Effectively, then, we have devices that now have all the desirable features of TTL (greater noise immunity, good rise times, line driving capability, etc.) plus the ability to interconnect outputs of similar devices.

Tri-state is useful in many facets of system design. Specifically, it becomes obvious immediately that multiplexing (regardless of the function) can be performed right on the bus line! Examples of other feats that can be performed with tri-state logic are: high speed time sharing of decoder-drivers, fast random-access (or sequential) memory arrays, bi-directional line driving, etc.

These ideas will be further described in another section of this document. Also, since tri-state devices can be literally attached to a bus line at will, modular TTL designs become a practicality allowing for readily expandable systems.

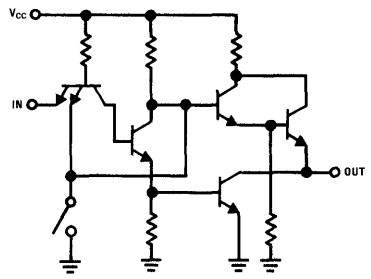


Figure 1

HOW IT'S DONE

Actually, the concept of creating a tri-state TTL device is relatively simple. Essentially, we provide a means of removing the drive current from the totem-pole output of the TTL device (see fig. 1). The output then resembles two semiconductor junctions biased in the non-conducting or high impedance state. As stated previously, these junctions do exhibit some leakage which must be provided for in the outputs of the device that is driving the bus line. For this reason all tri-state logic elements are designed to provide 5.2 mA in the logic "1" state (@ 2.4V minimum). If 128 tri-state outputs are connected to a bus line, the single ON device must supply (worst-case) the maximum leakage of 127 OFF devices and still have current left to drive the receiving TTL elements.

$$127 \times 40\ \mu A = 5.08\ mA$$
$$5.2\ mA - 5.08\ mA = 120\ \mu A$$

The above calculation indicated that three unit TTL loads can be driven even with 127 other devices connected to the line!

In order to provide the high output current required by tri-state connections the TTL output contains a darlington-connected upper stage.

The above essentially describes the basic device design considerations necessary to convert ordinary TTL to tri-state operation. There are some other minor changes but these are necessary primarily for fabrication reasons.

GENERAL COMMENTS CONCERNING TRI-STATE

Tri-state logic is unusual and therefore generates unusual considerations. For example, because of its

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higher source current capability, it has two distinct advantages over ordinary TTL. One advantage is that it can drive a greater length of line in line-driving applications. Ordinary TTL, having only 400 μA source capability, can drive approximately 10-12" of line before noise becomes a problem. All tri-state devices, however, can source 5.2 mA minimum and therefore can drive over 10 feet of cable reliably!

The other advantage attributable to the high source current capability of tri-state devices is the greatly reduced one-level output impedance which gives much better one-level noise immunity; being approximately a factor of 10 better. It is important to note that these advantages are only side benefits of tri-state. You get them in every tri-state device regardless of function. *Even if you don't use the bus-connection feature of tri-state logic devices there are inherent properties which still prove very useful in TTL system design.*

All tri-state devices behave like totem-pole TTL devices when they are in the ON state. It is necessary therefore that 1) all other devices connected to the same bus line must be OFF (Hi-Z state – see Fig. 2) and 2) that a convenient method of selecting the ON device in a system be provided.

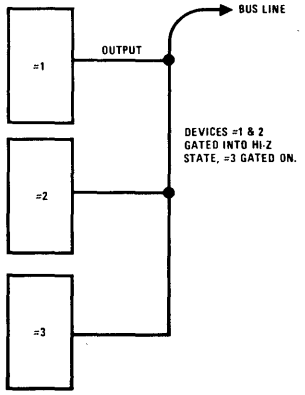


Figure 2

It is a relatively simple matter, in the DC sense, to insure that only one device at a time be in the ON state. However, in the real world of logic signals one must consider the system dynamics. In most cases, a singular transition of a system's state variables is used to determine the next state to be assumed by many elements of the system.

In the case of multiplexers, it will determine the next input to be selected to the MUX line. With tri-state logic devices, the transition will determine which device will go ON, while all others go OFF (Hi-Z). To insure that the condition of having two devices on at the same time never occurs, all tri-state devices are specified such that the time delay from the ON to the OFF state is *always* faster than the time delay from the OFF to the ON state. In cases where a system fault occurs, the data sheets guarantee that two devices may be in opposite low impedance states simultaneously for an indefinite period.

In-so-far as selection of devices is concerned we have provided for "0-0 coincidence" in those devices where it makes good design sense to do so. 0-0 coincidence is accomplished simply by using a two-input NOR gate as the device which determines the state of the tri-state device. Only when both inputs of a NOR function are zero (hence 0-0) will its output go to the "1" state. This "1" state is then allowed to enable the tri-state device. For all other conditions of inputs to the NOR gate the device will be disabled. The reason for this is that the outputs of most TTL decoders remain in their "1" state except for the particular output selected by the input signal to the decoder (it goes to a "0"). Two decoders can be used simply and effectively to choose any one single device in an array of many such devices. Where the two zeros coincide at an addressed location, the device turns ON. (See Fig. 3 for additional details.)

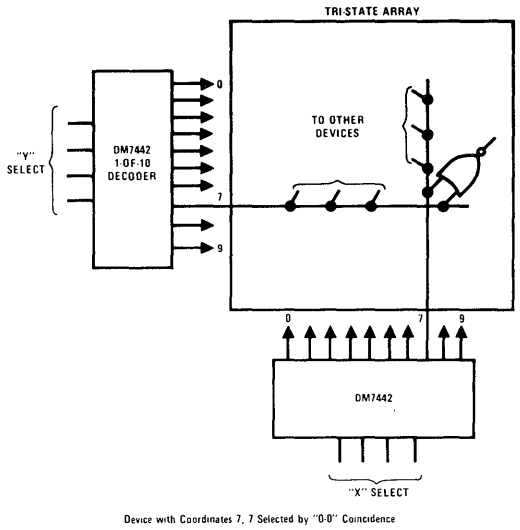
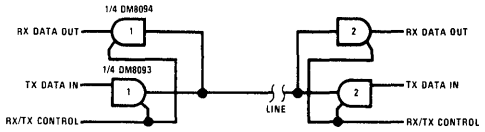


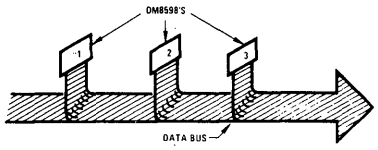
Figure 3

The final comment concerns itself with the logic currents needed by inputs of most tri-state devices when placed in the OFF condition. 40 μA is all that is required whether the input be either a "0" or a "1". The units are designed this way so that an array of devices can be driven from buffer type elements without having to handle the 1.6 mA zero level input current of all the OFF devices all the time. For example, a single DM8093 or DM8094 could drive an input array of greater than 128 devices and yet only have to sink less than 6.6 mA in the "0" state (approximately 5.08 mA for all the OFF devices and 1.6 mA for the ON device). So, in addition to making it easy to fan-out into large numbers of devices, we've made them easy to fan-into also.

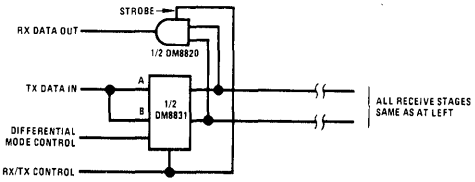
TYPICAL APPLICATIONS



SINGLE-ENDED TRANSMISSION

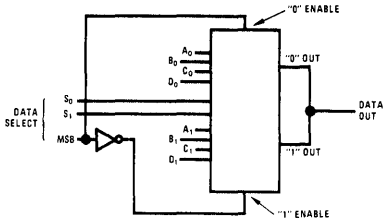


EXPANDABLE READ-ONLY MEMORY

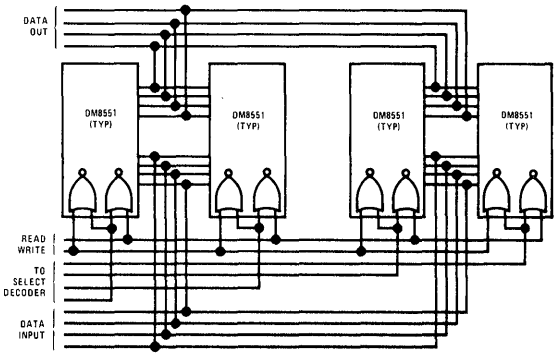


DIFFERENTIAL TRANSMISSION

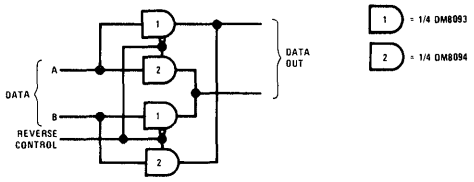
BI-DIRECTIONAL DATA LINES



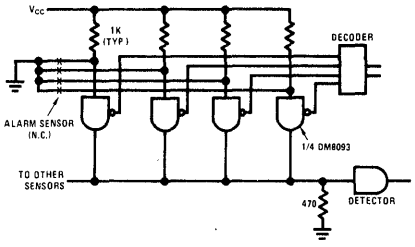
DM8214 AS AN 8-LINE TO 1-LINE MUX



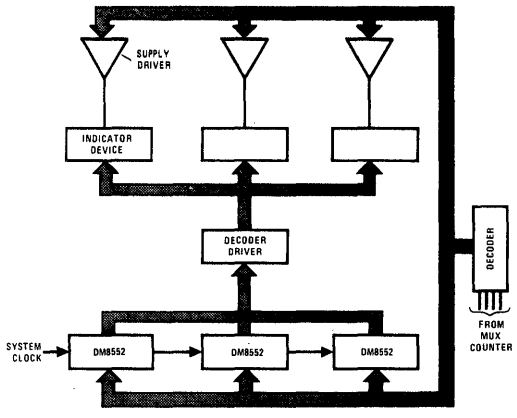
16 BIT (4 x 4) STORAGE FILE



DIGITAL REVERSING SWITCH



MULTIPLE-INPUT ALARM SCAN SYSTEM



DISPLAY SYSTEM WITH ONLY ONE DECODER-DRIVER

New Products

DM1800(MC1800) dual 5-input gate
DM1801(MC1801) dual 5-input gate

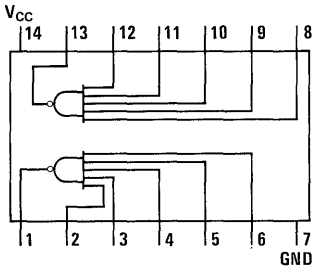
general description

The DM1800 and DM1801 are five-input NAND gates that are completely compatible with other devices in National's DTL 930 series. The DM1800 has a 6K pullup resistor and the DM1801 is the 2K option.

Typical power dissipation is 11 mW per gate. Maximum ratings agree completely with other DTL gates. Features include:

- Operating power supply 5.0V
- Maximum power supply (continuous) 8.0V
- Logic "1" output level (max at 25°C) 2.6V
- Logic "0" output level (max at 25°C) 0.45V
- Logic "1" input level (min at 25°C) 1.9V
- Logic "0" input level (max at 25°C) 1.1V
- Typical noise immunity 1.0V

connection diagram

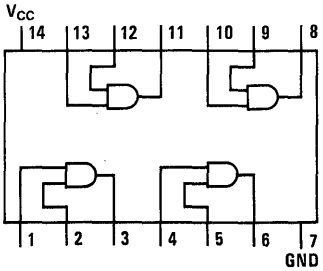


DM5408/DM7408(SN5408/SN7408) quad 2-input AND gate
DM5409/DM7409(SN5409/SN7409) quad 2-input AND gate (open collector)
DM5411/DM7411(SN5411/SN7411) triple 3-input AND gate

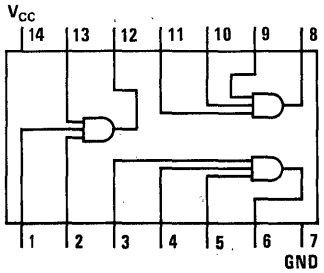
general description

Unlike most TTL devices, these gates directly implement the positive AND or negative OR functions. The DM5408/DM7408 and DM5411/DM7411 have normal totem-pole outputs and characteristics similar to other gates in the 54/74 TTL series. The DM5409/DM7409 has an open-collector output on each gate, allowing outputs to be wire-AND'ed for additional logic flexibility.

connection diagrams



DM5408/DM7408
DM5409/DM7409



DM5411/DM7411

DM5446/DM7446(SN5446/SN7446) 7 segment decoder/driver
DM5447/DM7447(SN5447/SN7447) 7 segment decoder/driver
DM5448/DM7448(SN5448/SN7448) 7 segment decoder/driver

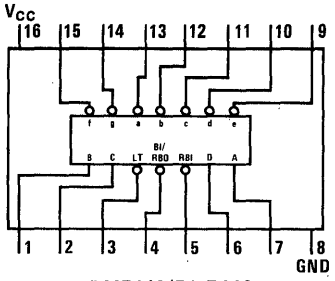
general description

Seven-segment indicator lamps, logic circuits and discrete active devices are driven by this series of BCD decoders. All types fully decode a 4-bit BCD input. BCD numbers from zero through 9 are decoded to the standard 7-segment display format and BCD numbers above 9 to unique patterns that verify operation. Features include:

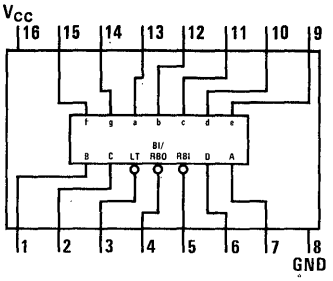
- Lamp-test input
- Leading/trailing zero suppression (RBI and RBO)
- Blanking input that may be used to modulate lamp intensity or inhibit output
- TTL and DTL compatible

The DM5446/DM5476 has active-low, open-collector outputs that will drive lamp segments requiring up to 20 mA. The outputs will withstand 30V, with reverse current of 250 μA. Normalized fanout is 12. The DM5447/DM7447 has similar output characteristics, except that the outputs withstand 15V. The DM5448/DM7448 has active-high, passive-pullup outputs with a fanout of 4. It is normally used to drive logic circuits or to operate high-voltage loads such as electroluminescent displays through buffer transistors or SCR switches.

connection diagrams



DM5446/DM7446
DM5447/DM7447



DM5448/DM7448

DM7488(SN7488) 256-bit read only memory

general description

Large-scale integration and programming in the wafer stage of processing make this TTL high-performance ROM economical in applications such as table lookup, subroutine storage and random logic synthesis. The 256 bits are organized as 32 8-bit words. Other features are:

- On-chip decoding of 5-bit address
- Open-collector outputs for expansion to greater number of words
- Typical access time of 30 ns
- Overriding strobe input
- Input clamp diodes
- TTL and DTL compatible
- Typical power dissipation only 240 mW.

ROM expansion method

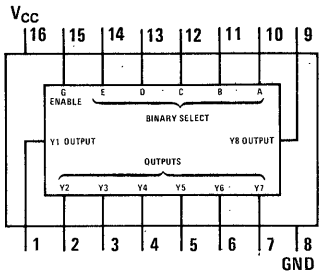
Word length may be expanded to n bits by operating several ROMs in parallel. The number of words may be expanded by wire-AND connecting the outputs, using pullup resistors connected to V_{CC} to define the "1" logic level. Chip-enable signals may be obtained from active-low TTL decoders addressed by the higher-order address bits. The strobe input enables an output if taken to the logical "0" level. All outputs are held high if the strobe input is high.

A tri-state replacement, the DM7598/DM8598 has been developed for applications where open-collector performance or pullup resistors are undesirable. It is expandable to 32,768 bits in word lengths from 8 bits to 1024 bits.

programming

Programming is ordered by filling in a truth table. The table is used to make changes in the metallization mask determining the storage transistor functions.

connection diagram



DM7488AA(SN7488AA) 256-bit read only memory

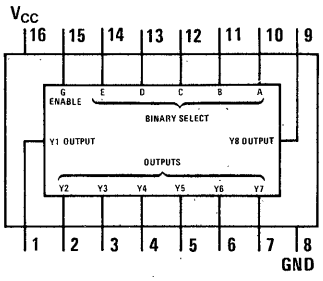
general description

The DM5488AA/DM7488AA is a DM5488/DM-7488 256-bit read-only memory programmed as a sine look-up table. The 5-bit address input code linearly divides 90° into 32 equal segments. The corresponding 8-bit output word is the sine value of the input angle in the form of a binary fraction. The output values are not rounded off, so that their accuracy may be extended by expanding the lookup table with additional ROMs.

Input/output functions of the lookup table are given by its truth table. For example, a binary input of 26 (11010) represents 26/32 of 90°, or about 73°. The corresponding output of 11110100 indicates (1/2 + 1/4 + 1/8 + 1/16 + 1/64) or about 0.95.

Open-collector outputs are provided to facilitate expansion by the methods indicated on the DM5488/DM7488 data sheet. Access time of 30 nanoseconds, typical, and other performance features are the same as those of the DM5488/DM7488.

connection diagram



DM5496/DM7496(SN5496/SN7496) 5-bit shift register

general description

The DM5496/DM7496 may be used as a serial-to-parallel converter, parallel-to-serial converter, or storage register. Inputs and outputs of the five R-S master-slave flip-flops are accessible, permitting parallel-in/parallel-out and serial-in/serial-out operation, as well as serial/parallel conversions. Key features include:

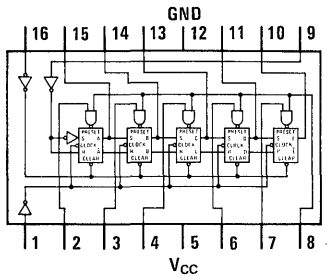
- Typical propagation delay of 25 ns
- Minimum clock pulse width of 35 ns
- Fanout of 10
- Multifunction capability
- Expansion to N bits as register or converter.

operation

A logical "0" voltage applied to the clear input simultaneously sets all flip-flops to the "0" state independent of the clock input state. Any flip-flops may be set independently to "1" by "1" inputs on the common preset input and on the preset inputs of the specific flip-flops to be set. Preset is also independent of clock state.

Information is transferred to the output pins when the clock input goes from a logical "0" to a logical "1". The clear input must be at "1" and the preset input at "0" when clocking occurs. Since the flip-flops are R-S master-slave type, the proper information must appear at the R-S inputs before the clock edge rises. The serial input provides this information to the first flip-flop and the flip-flop outputs provide the information to the remaining R-S inputs.

connection diagram



DM54153/DM74153(SN54153/SN74153) dual 4:1 multiplexer

general description

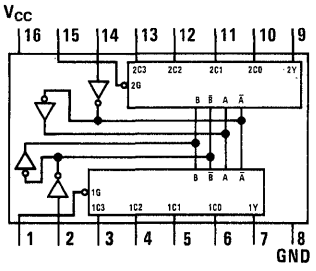
The DM54153/DM74153 can be operated as a dual 4:1 or single 4:2 multiplexer, data selector or parallel-to-serial converter. Several devices can be operated in cascade to form N-line-to-1-line and N-line-to-n-line switching subsystems. Features are:

- Common addressing, separate strobes
- Low propagation delays, typically 14 ns for data
- Fanout of 20 in high-level state facilitates connection of used and unused outputs
- Typical power dissipation of 170 mW
- Input clamp diodes
- TTL and DTL compatible.

operation

A 2-bit binary address selects one of four data inputs to be switched to the single output of both halves. Each half, however, has a separate strobe which holds the output of that half low when the strobe is taken to the logical "1" level. Thus, eight data inputs can be switched in a dual 4:1 mode, or four data lines connected to both sides may be switched in a 4:2 mode.

connection diagram



DM7090/DM8090 quad inverter/2-input NAND buffer

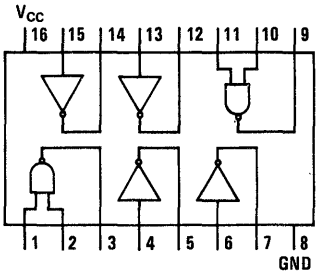
general description

This monolithic TTL device contains four inverters and two 2-input NAND gates. It was designed to reduce package counts in applications where a gate is needed occasionally in the same card location as inverters.

The two NAND gates may also be used as inverters, by making the two inputs common. DM7090/DM8090 characteristics are similar to those of other gates and inverters in the 54/74 series and are completely compatible with 54/74 devices. Other features are:

- Input clamp diodes
- Fanout of 10
- Typical propagation delay of 13 ns
- Typical power dissipation of 10 mW/gate or inverter
- Noise immunity is 1V typical, 400 mV guaranteed.

connection diagram



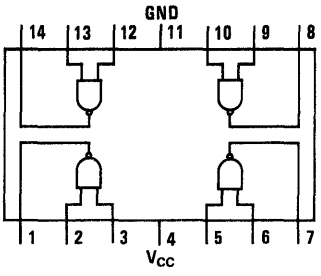
DM7091/DM8091 quad 2-input NAND buffer

general description

The DM7091/DM8091 has characteristics similar to the DM5440/DM7440 (SN5440/SN7440) dual 4-input NAND gate/buffer, but is configured as a quad NAND gate. It is used instead of conventional NAND gates for driving large numbers of TTL loads, long interconnection lines, clock drive in synchronous logic systems, and similar functions. The DM7091/DM8091 will also operate small lamps and relays. Key features are:

- Series 54/74 compatible
- Fanout of 30
- 50 mA drive current
- Noise immunity of 1V typical, 400 mV guaranteed
- Input clamp diodes.

connection diagram



DM7214/DM8214 tri-state dual 4:1 multiplexer

general description

The DM7214/DM8214 is pin-compatible with the DM54153/DM74153 dual 4:1 multiplexer, but has tri-state TTL outputs. These outputs can be bus-connected in large numbers, permitting expansion without pullup resistors or submultiplexers. Features include:

- Operates as dual 4:1 or single 8:1 multiplexer
- DM7214 may be connected 40-wide for expansion up to 160-line-to-1-line multiplexer
- DM8214 may be connected 128-wide for expansion up to 512-line-to-1-line multiplexer
- Output source current is −5.2 mA and sink current is 16 mA over the industrial temperature range, and −2 mA and 16 mA over the military temperature range
- Typical propagation delays of 20 ns
- High noise immunity and line-drive capability
- Complete compatibility with TTL devices in the 54/74 series and compatibility with DTL.

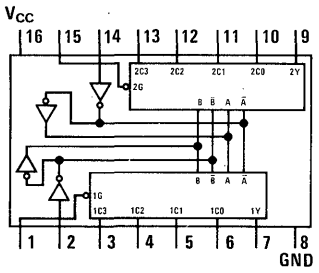
operation

For operation in the dual mode, four input data channels are connected to the A inputs and four channels to the B inputs. A common 2-bit address selects the A input switched to the A output and the B input switched to the B output. Either output is enabled with an "0" level strobe on that side or disabled by a "1" level strobe on that side. This permits 8-line-to-1-line operation if the two outputs are connected and alternately enabled while eight input data channels are applied to the A and B inputs.

The enabled states of the DM7214/DM8214 are the normal TTL "1" and "0" logic states. Outputs have active pullup when enabled, providing the low impedance, high fanout, speed and noise immunity of active-pullup TTL. However, when disabled, the outputs switch into a third, high-impedance state that permits only a maximum leakage current of 40 μA to flow regardless of the input data states. An enabled DM7214 output will supply leakage current to at least 39 outputs in the high-impedance state on the same output line and an enabled DM8214 output will supply leakage current into at least 127 high-impedance outputs, while driving at least three TTL loads.

Tri-state outputs therefore allow up to 40 DM7214 or 128 DM8214 outputs to be connected to one output data line without pullup resistors or significant degradation of data transfer rates. Fanout increases up to 10 if fewer outputs are connected. Noise immunity and length of lines that can be driven are generally much greater than provided by standard TTL outputs.

connection diagram



DM7280/DM8280(S8280/N8280)presettable decade counter
DM7281/DM8281(S8281/N8281)presettable binary counter
DM7288/DM8288(S8288/N8288) presettable ÷12 counter

general description

The counters in this series are four-bit monolithic subsystems containing a divide-by-two counter with one clock input and a second counter with a second clock input. The two clock inputs and the other logic functions provided will implement a wide variety of counter and storage register functions. Functionally equivalent to the 8280, 8281 and 8288, these counters were implemented with Series 54/74 technology. Key features include:

- Series 54/74 compatible
- Two clock inputs for additional flexibility
- Strobed parallel-entry capability
- Reset inputs common to all stages
- Typical toggle rates to 45 MHz
- Typical power dissipation of 130 mW.
- Direct-coupled stages.

The DM7280/DM8280 counter operates as a divide-by-two and divide-by-five counter with no external connections. When the A output is connected to the Clock 2 input, it counts in the familiar BCD mode. The bi-quinary mode is obtained by connecting the D output to the Clock 1 input while applying the clock to the Clock 2 input. This produces a square-wave output at f/10 on the A output that is particularly useful in frequency synthesizers.

The DM7281/DM8281 is a 2,2,4,8 counter when operated with two clock inputs and no external connections. It is a 2,4,8,16 counter when the A output is connected to the Clock 2 input. Thus, it may be used as a divide-by-two, -eight, or -sixteen counter.

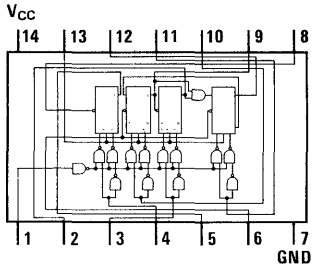
The DM7288/DM8288 consists of divide-by-two and divide-by-six counters. For divide-by-twelve operation, output A is connected to the Clock 2 input.

Counting is performed on the negative-going edge of the clock pulse in all three types. The divide-by-two stages may be toggled at up to 45 MHz, typical, approximately twice the maximum frequency of the Clock 2 input.

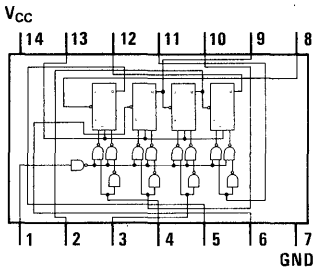
All three have parallel inputs which may be used to set the corresponding outputs to desired states. The parallel input logic levels are transferred to the outputs when the strobe line is placed at the logical "0" level. An "0" on the reset line will place all four outputs in the "0" state.

The register-storage function can be obtained by using the strobed parallel-entry capability. Data to be stored is entered by the method indicated above and retained on the outputs holding both clock inputs at logical "1" (V_{CC}). The register may be reloaded with a new parallel entry and strobe operation or cleared by the reset line.

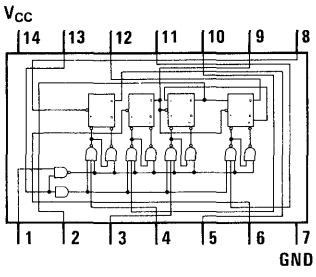
connection diagrams



DM7280/DM8280



DM7281/DM8281



DM7288/DM8288

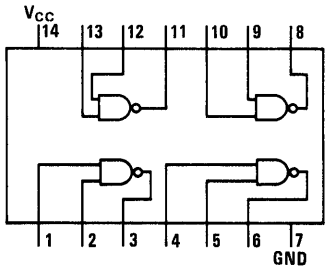
DM7426(SN7426) quad 2-input high voltage NAND gate

general description

The DM7426 is a quad two-input NAND gate with characteristics similar to the DM8810. It will interface standard TTL or DTL devices with low-threshold MOS memories and other devices operating on 12V power supplies, and drive low-current relays and lamps within its voltage range. Features are:

- Open-collector output withstands 15V pullup
- Standard 5V V_{CC}
- Output sinks 16 mA for high fanout
- Same pin configuration as DM7400.

connection diagram



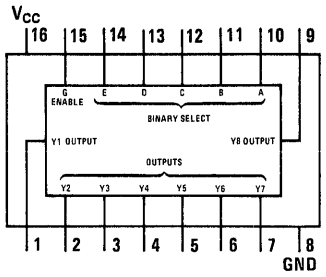
DM7598/DM8598 tri-state 256-bit read only memory

general description

The DM8598 is identical to the SN7488 except that the enable input on the SN7488 simply places all outputs in the logical "1" state, whereas the enable input on the DM8598 places the outputs in a high impedance state. This high impedance state allows many outputs to be connected in parallel for expansion to greater numbers of words and/or connection to a common bus line. Features include:

- Organized as 32 8-bit words
- Party line capability
- On-chip decoding
- Pin compatible with SN7488
- Typical access time — 30 ns
- Total power dissipation — 350 mW
- TTL and DTL compatible.
- Strobe input
- Input clamp diodes.

connection diagram

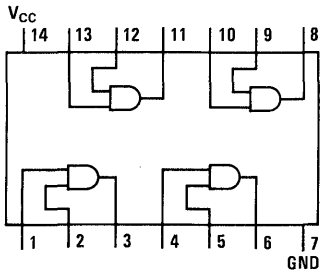


DM7819/DM8819 quad 2-input TTL-MOS AND gate

general description

The DM7819 is the high output voltage version of the SN5409. Its open-collector outputs may be "pulled-up" to +14 volts in the logical "1" state thus providing guaranteed interface between TTL and MOS logic levels.

connection diagram



Series 74H TTL integrated circuits

The gates, inverters and expanders in the 74H series are high speed versions of the similarly numbered devices in National's standard TTL family (Series 74). The two series are completely compatible, being specified to the same voltages and temperature range (0°C to 70°C). They can be used in combination, with Series 74H circuits located wherever minimum propagation delays are needed. The series features are:

- Typical gates delay down to 6 ns
- Typical DC noise margin of 1V
- Low susceptibility to AC noise
- Minimum output short-circuit current of −40 mA for gates
- Higher source and sink currents than standard TTL
- Fanout of 10 Series 74H loads or 12 Series 74 loads
- Waveform integrity over full load and temperature range
- AND gates and open-collector gates available.

Each Series 74H input has a maximum current flow of 2 mA out of the input at logical "0" voltage and a maximum current flow into the input of 50 μA at logical "1" voltage. Each Series 74H gate output is specified to drive 10 such loads and has a current sink capability of 20 mA. The typical power dissipation per NAND gate is 23 mW at 50% duty cycle.

Open-collector gates have a fanout of 10 when not wire-OR'd and a fanout up to 9 when wire-OR'd. The output is connected to V_{CC} through an external load resistor. Value of the load resistor is calculated by the same method used for Series 74 open-collector devices, except that the input and sink currents given above are substituted for the Series 74 current values.

To maintain optimum switching times and noise immunity, unused inputs should receive current at the logical "1" level (except that unused expander inputs should be left open). The unused inputs may be connected to used inputs on the same gate provided the fanout of the driving output is not exceeded. Unused inputs may also be connected to V_{CC}, if a resistor is placed in the supply line to protect the inputs from transients above 5.5V. Up to 25 inputs may be connected through a 1-kilohm resistor. Or, the unused inputs may be connected to an independent supply, preferably 2.4 to 3.5V.

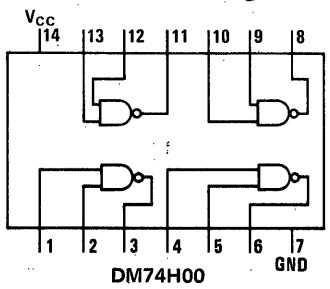
DM74H00(SN74H00) quad 2-input NAND gate
DM74H04(SN74H04) hex inverter
DM74H10(SN74H10) triple 3-input NAND gate
DM74H20(SN74H20) dual 4-input NAND gate
DM74H30(SN74H30) 8-input NAND gate

general description

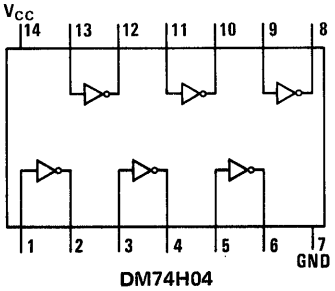
These TTL gates and inverter operate with about half the typical propagation delays of the same logic functions in Series 74 and have higher current ratings. However, the two series are completely compatible and may be used in combination. Key features are:

- Typical propagation delays down to 6 ns
- Typical DC noise margin of 1V and low susceptibility to AC noise
- Fanout of 10 Series 74H loads and 12 Series 74 loads.

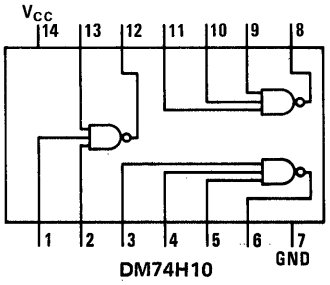
connection diagrams



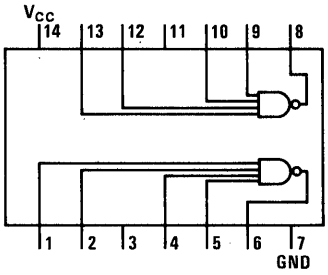
DM74H00



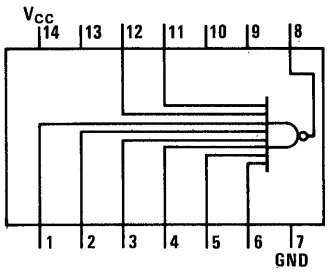
DM74H04



DM74H10



DM74H20



DM74H30

DM74H01(SN74H01) quad 2-input NAND gate (open collector)
DM74H05(SN74H05) hex inverter (open collector)
DM74H22(SN74H22) dual 4-input NAND gate (open collector)

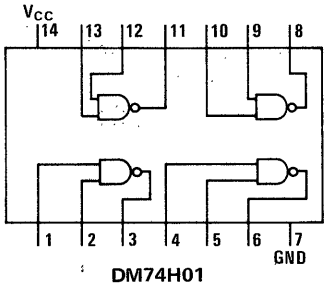
general description

These TTL circuits provide higher speed in wire-OR applications than Series 74 open-collector gates. Key features include:

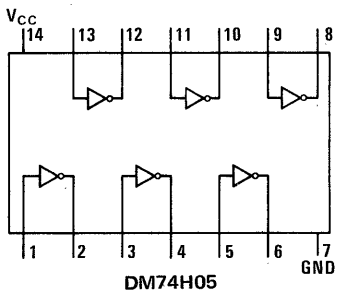
- Typical gate propagation delays of 7.5 ns to logical "0" output and 10 ns to logical "1" output
- Typical DC noise margin of 1V and low susceptibility to AC noise
- Fanout of 10 Series 74H loads when not wire-OR'd and up to 9 74H loads when wire-OR'd.

An output resistor connected to V_{CC} is needed. The load resistor value is calculated by the same method used for Series 74 open-collector circuits, except that the current values are higher. Series 74H input current maximums are 50 μA at logical "1" voltage and 2 mA at logical "0" voltage. Maximum output sink current is 20 mA.

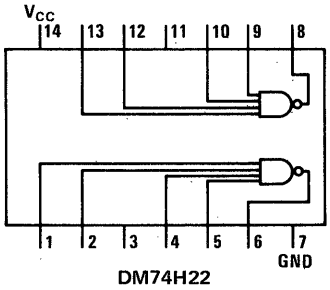
connection diagrams



DM74H01



DM74H05



DM74H22

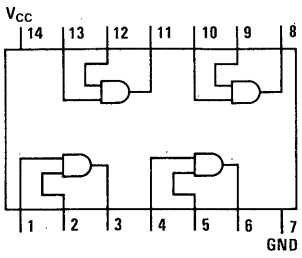
DM74H08(SN74H08) quad 2-input AND gate
DM74H11(SN74H11) triple 3-input AND gate
DM74H21(SN74H21) dual 4-input AND gate

general description

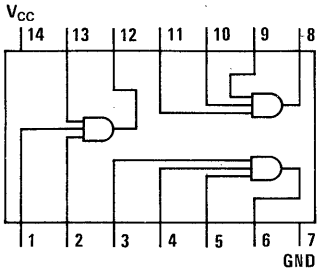
These Series 74H gates provide the non-inverting AND function with very low propagation delays. They are completely compatible with other TTL devices in the 74 and 74H series. Features include:

- Typical propagation delays less than 9 ns
- Fanout of 10 Series 74H loads or 12 Series 74 loads
- Typical DC noise margin of 1V and low susceptibility to AC noise.

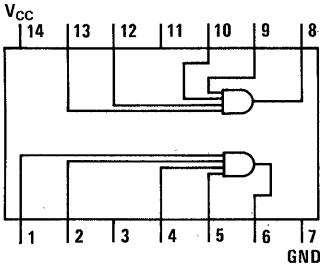
connection diagrams



DM74H08



DM74H11



DM74H21

DM74H40(SN74H40) dual 4-input NAND buffer

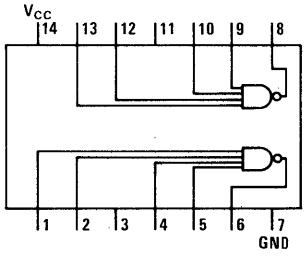
general description

The DM74H40 provides the same logic function as the DM7440 but has much lower propagation delay and much higher fanout. Key features are:

- Fanout of 30
- Typical propagation delays of 6.5 ns to logical "0" and 8.5 ns to logical "1" output
- Typical DC noise margin of 1V and low susceptibility to AC noise.

The DM74H40 is completely compatible with other devices in the 74H and 74 TTL series.

connection diagram



DM74H50(SN74H50) expandable dual 2-wide 2-input AND-OR-INVERT gate
DM74H51(SN74H51) dual 2-wide 2-input AND-OR-INVERT gate
DM74H52(SN74H52) expandable 2-2-2-3-input AND-OR gate
DM74H53(SN74H53) expandable 2-2-2-3-input AND-OR-INVERT gate
DM74H54(SN74H54) 4-wide 2-input AND-OR-INVERT gate
DM74H55(SN74H55) expandable 2-wide 4-input AND-OR-INVERT gate

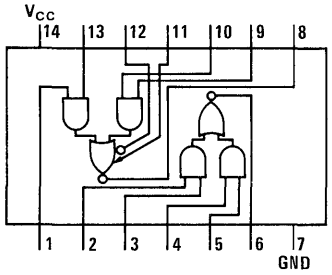
general description

These complex gates provide the same logic functions as similarly numbered Series 74 devices, but operate at much higher speeds. They are completely compatible with Series 74 TTL, except that 74H expanders should be used on the expandable gates. Key features are:

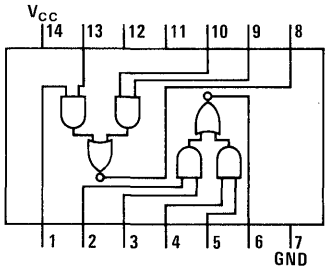
- Without expanders, typical propagation delays are about 10 ns for the DM74H52 and 7 ns or less for the other gates
- With expanders, typical propagation delays are less than 15 ns for the DM74H52 and about 11 ns for the DM74H50, DM74H53 and DM74H55
- Typical DC noise margin of 1V and low susceptibility to AC noise.

The DM74H51 and DM74H54 have the same pin configurations as the DM74H50 and DM74H53, but the expander inputs on the DM74H51 and DM74H54 are not functional. The DM74H50, DM74H53 and DM74H55 will accept one DM74H62 or up to four DM74H60 expanders. The DM74H52 will accept up to six DM74H61 expanders. Expander pins on the gates should be left open when not used.

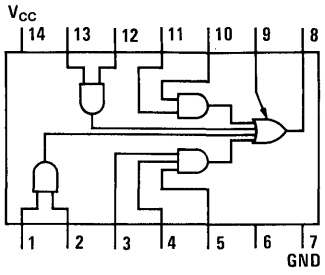
connection diagrams



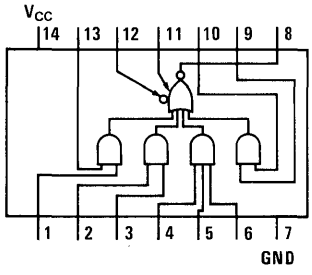
DM74H50



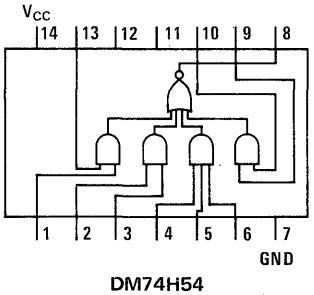
DM74H51



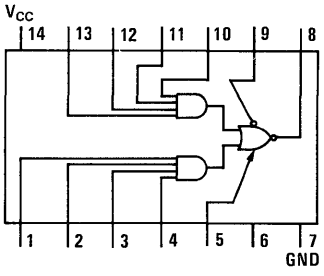
DM74H52



DM74H53



DM74H54



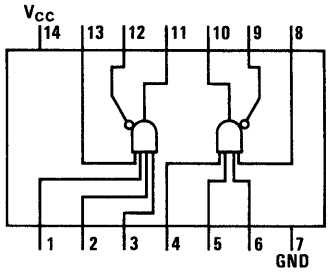
DM74H55

DM74H60(SN74H60) dual 4-input expander
DM74H61(SN74H61) triple 3-input expander
DM74H62(SN74H62) 3-2-2-3-input expander

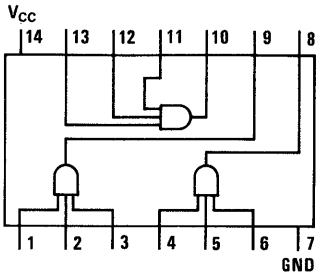
general description

These expanders are designed to be used on the high-speed expandable gates in the 74H series, adding only about 4 ns to the gate propagation delays. The DM74H50, DM74H53 or DM74H55 may be expanded with up to four DM74H60 expanders or one DM74H62 expander. Up to six DM74H62 expanders may be used on the DM74H52 gate.

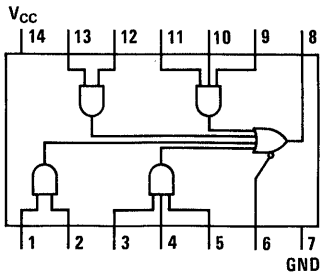
connection diagrams



DM74H60



DM74H61



DM74H62

DH0035/DH0035C PIN diode driver

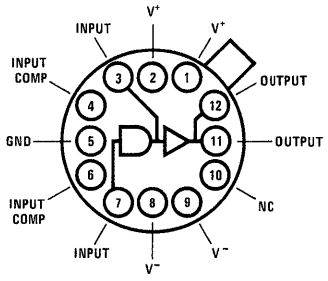
general description

The DH0035 is a high speed switch driver specification designed to supply the high peak currents needed for diode switching. Features include:

- High current drive lamp peak
- High voltage swing 12–30V
- Low standby power typ 30 mW
- Very fast rise and fall times typ.

These features make the NH0035 ideal for driving PIN diode RF switches.

connection diagrams



TOP VIEW

Tri-State Logic

DM7093/DM8093 tri-state quad buffers
DM7094/DM8094 tri-state quad buffers

general description

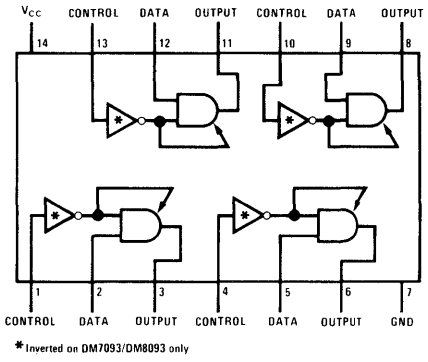
The DM7093/DM8093 and DM7094/DM8094 are quad 2-input buffers which accept normal TTL or DTL input levels and have outputs which provide either normal low-impedance TTL output characteristics or a high impedance state. One of the two inputs to each buffer is used as a control line to gate the output into the high impedance state. The other input simply passes the non-inverted data through the buffer. The DM7093/DM8093 and DM7094/DM8094 differ only in the activating logic state of the control input. The DM7093/DM8093 provides the high impedance state when a logical "1" is applied to the control input; the DM7094/DM8094 operates similarly with a logical "0". Features of these buffers include:

- Series 54/74 TTL and 930 DTL Compatible
- Same Pin Breakout as SN5400/SN7400 TTL and 946 DTL
- Up to 128 Buffers can be Connected to a Common Bus-Line
- 12 ns Propagation Delay
- High Capacitive Drive Capability
- Independent Control of each Buffer

This unique tri-state concept allows outputs to be tied together and then connected to a common bus line. Normal TTL outputs cannot be connected due to the low-impedance logical "1" output current which one device would have to sink from the other. If however on all but one of the connected devices both the upper and lower output transistors are turned off, then the one remaining device in the normal low impedance state will have to supply to or sink from the other devices only a small amount of leakage current. This is exactly what occurs on the DM7093/DM8093 and DM7094/DM8094.

(Continued on page 17)

logic and connection diagram



*Inverted on DM7093/DM8093 only

truth tables

DM7093/DM8093

DATA	CONTROL	OUTPUT
1	0	1
0	0	0
X	1	Hi-Z

X = Irrelevant

DM7094/DM8094

DATA	CONTROL	OUTPUT
1	1	1
0	1	0
X	0	Hi-Z

X = Irrelevant

absolute maximum ratings

Supply Voltage	7V
Input Voltage	5.5V
Output Voltage	5.5V
Time that two bus-connected devices may be in opposite low impedance states simultaneously (5% duty cycle)	10 msec
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	
DM7093, DM7094	−55°C to +125°C
DM8093, DM8094	0°C to +70°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics (Note 1)

PARAMETERS		CONDITIONS	MIN (NOTE 3)	TYP	MAX (NOTE 3)	UNITS
Input Clamp Voltage	DM7093/94	V_{CC} = 4.5V, T_A = 25°C, I_{IN} = −12 mA			−1.5	V
	DM8093/94	V_{CC} = 4.75V, T_A = 25°C, I_{IN} = −12 mA			−1.5	V
Logical "1" Input Voltage	DM7093/94	V_{CC} = 4.5V	2.0			V
	DM8093/94	V_{CC} = 4.75V	2.0			V
Logical "0" Input Voltage	DM7093/94	V_{CC} = 4.5V			0.8	V
	DM8093/94	V_{CC} = 4.75V			0.8	V
Logical "1" Input Current	DM7093/94	V_{CC} = 5.5V, V_{IN} = 2.4V			40	μA
	DM8093/94	V_{CC} = 5.25V, V_{IN} = 2.4V			40	μA
Logical "1" Input Current	DM7093/94	V_{CC} = 5.5V, V_{IN} = 5.5V			1	mA
	DM8093/94	V_{CC} = 5.25V, V_{IN} = 5.5V			1	mA
Logical "0" Input Current (Control Input Only)	DM7093/94	V_{CC} = 5.5V, V_{IN} = 0.4V			−1.6	mA
	DM8093/94	V_{CC} = 5.25V, V_{IN} = 0.4V			−1.6	mA
Logical "0" Input Current (Data Input Only)	DM7093/94	V_{CC} = 5.5V, V_{IN} = 0.4V, $V_{CONTROL}$ = 2.0V (DM7093/8093) 0.8V (DM7094/8094)			−40	μA
	DM8093/94	V_{CC} = 5.25V, V_{IN} = 0.4V, $V_{CONTROL}$ = 0.8V (DM7093/8093) 2.0V (DM7094/8094)			−1.6	mA
Logical "1" Output Voltage	DM7093/94	V_{CC} = 4.5V, I_o = −2.0 mA	2.4	3.3		V
	DM8093/94	V_{CC} = 4.75V, I_o = −5.2 mA	2.4	3.3		V
Logical "0" Output Voltage	DM7093/94	V_{CC} = 4.5, I_o = 16 mA		.23	0.4	V
	DM8093/94	V_{CC} = 4.75, I_o = 16 mA		.23	0.4	V
Output Short Current (Note 2)	DM7093/94	V_{CC} = 5.5V, V_o = 0V	−30	−45	−70	mA
	DM8093/94	V_{CC} = 5.25V, V_o = 0V	−28	−45	−70	mA
Supply Current	DM7093	V_{CC} = 5.5V		32	54	mA
	DM8093	V_{CC} = 5.25V		32	54	mA
Supply Current	DM7094	V_{CC} = 5.5V		36	62	mA
	DM8094	V_{CC} = 5.25V		36	62	mA
Output Disable Current	DM7093/94	V_{CC} = 5.5V, V_o = 2.4V			40	μA
	DM8093/94	V_{CC} = 5.25V, V_o = 0.4V			−40	μA
V_{CC} Clamp		V_{CC} = 0V, I_o = 12 mA			1.5	V
Ground Clamp		V_{CC} = 0V, I_o = −12 mA			−1.5	V
t_{pd1}	DM7093/8093	V_{CC} = 5.0V		12	23	ns
	DM7094/8094	T_A = 25°C		12	23	ns
t_{pd0}	DM7093/8093	V_{CC} = 5.0V		12	18	ns
	DM7094/8094	T_A = 25°C		12	18	ns
t_{1H}	DM7093/8093	V_{CC} = 5.0V		5	10	ns
	DM7094/8094	T_A = 25°C		12	18	ns
t_{0H}	DM7093/8093	V_{CC} = 5.0V		14	24	ns
	DM7094/8094	T_A = 25°C		18	29	ns
t_{H1}	DM7093/8093	V_{CC} = 5.0V		14	21	ns
	DM7094/8094	T_A = 25°C		14	21	ns
t_{H0}	DM7093/8093	V_{CC} = 5.0V		13	25	ns
	DM7094/8094	T_A = 25°C		13	25	ns

NOTE 1: Unless otherwise specified the min-max limits across the −55°C to +125°C temperature range for the DM7093 & DM7094 and across the 0°C to 70°C temperature range for the DM8093 & DM8094. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

NOTE 2: Only one output at a time should be shorted.

NOTE 3: MIN and MAX values refer to the absolute values.

general description (cont.)

A typical system connection is shown in Figure 1. While true that in a TTL system open-collector gates could be used to perform the logic function of these tri-state elements, neither waveform integrity nor optimum speed would be achieved. The low output impedance of the DM7093/DM8093 and DM7094/DM8094 provides good capacitance drive capability and rapid transition from the logical "0" to logical "1" level thus assuring both speed and waveform integrity.

It is possible to connect as many as 128 devices to a common bus-line and still have adequate drive capability to allow fan-out from the bus. The example shown in Figure 2 indicates how this guarantee can be made under worst-case conditions.

Another advantage of these buffers is that in the high impedance state their inputs do not present the normal loading to the driving device. This is significant when it is desirable to transmit in both directions over a common line. Figure 3 illustrates such a system. Assume one device in group A is driving the bus-line; and the gates at B are receiving the signals. All outputs at C and D are gated into the high-impedance state. Normally the fan-out from the driving gate at A would be calculated at 4—2 from B and 2 from D, plus additional slight loading from those outputs in the high impedance state. But since the logical "0" input current on D's inputs deliver only 40 μA when these devices are gated into the high impedance state, the loading is significantly reduced. It's true that the logical "1" fan-out remains the same (40 μA times the number of inputs and high-impedance-state outputs). However since the logical "1" fan-out capability of these tri-state devices is 130 while the logical "0" fan-out capability is only 10, it is obvious that the logical "0" fan-out is the limiting item and that a significant increase in the number of inputs which can be tied to the bus-line can be achieved by reducing the number of ~1.6 mA logical "0" loads.

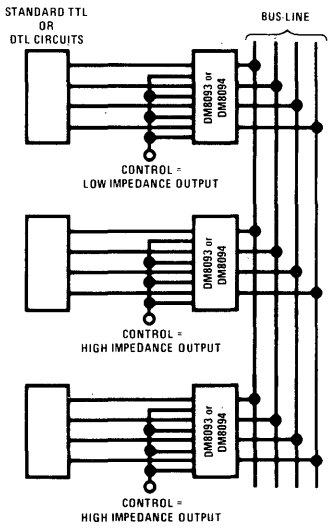


FIGURE 1

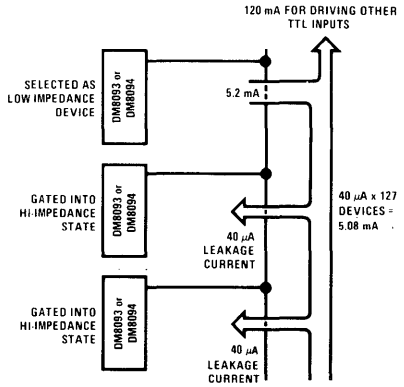


FIGURE 2

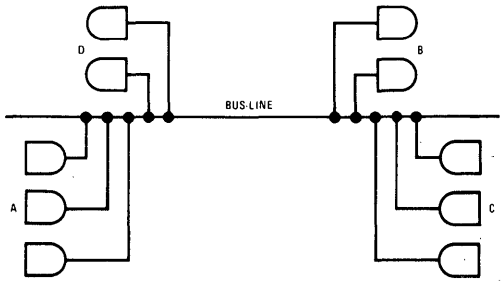
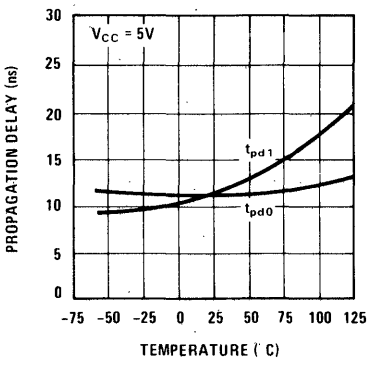


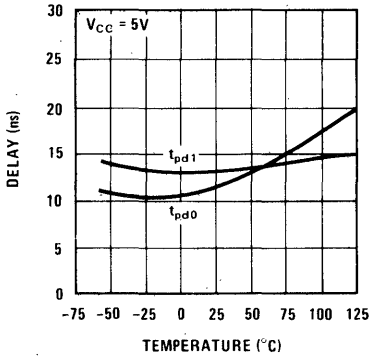
FIGURE 3

typical performance

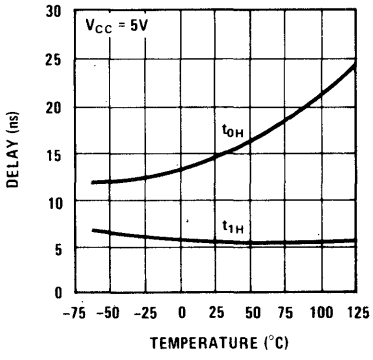
Propagation Delay vs Temperature (DM7093/DM8093)



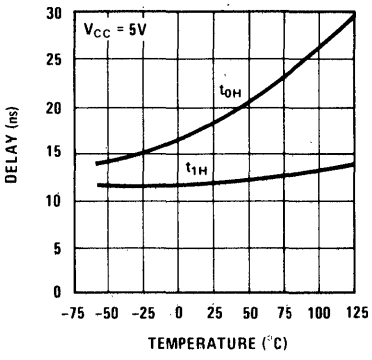
Propagation Delay vs Temperature (DM7094/DM8094)



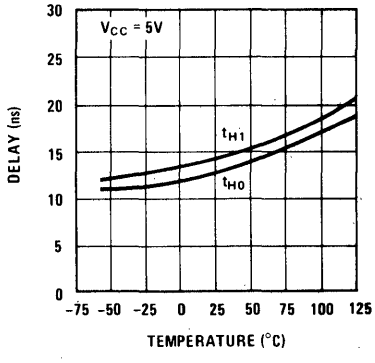
Delay From Control to High Impedance State (DM7093/DM8093)



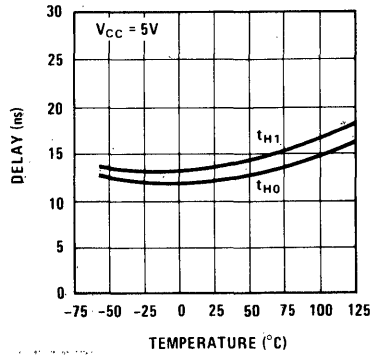
Delay from Control to High Impedance State (DM7094/DM8094)



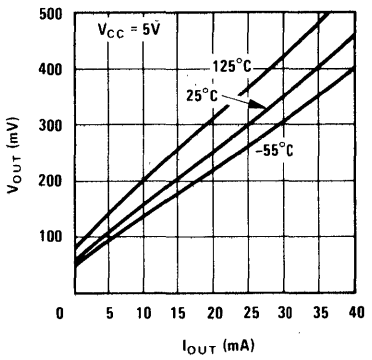
Delay from Control to Low Impedance State (DM7093/DM8093)



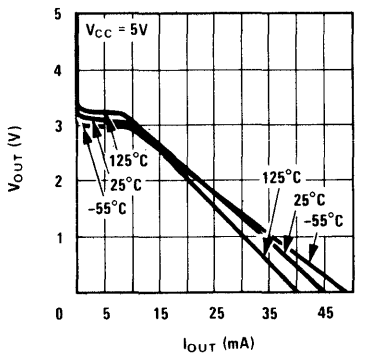
Delay from Control to Low Impedance State (DM7094/DM8094)



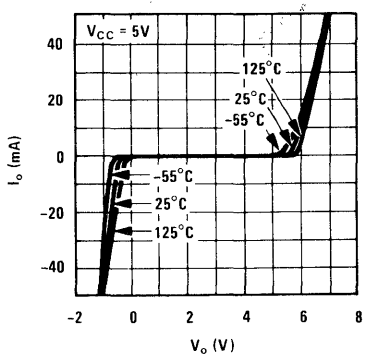
Logical "0" Output Voltage vs Sink Current



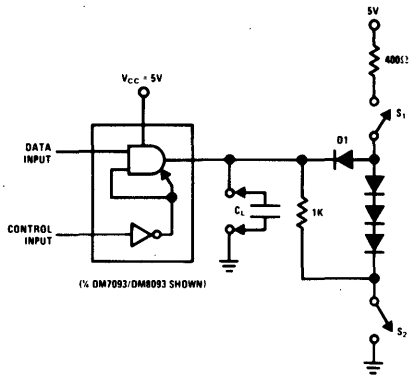
Logical "1" Output Voltage vs Source Current



I_{OUT} vs V_{OUT} (High Impedance Output State)



ac test circuit



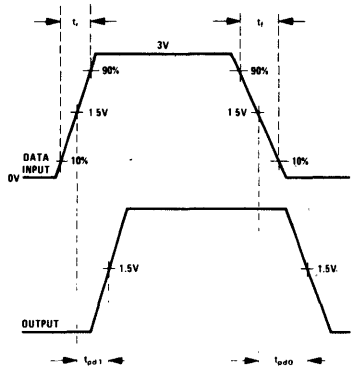
	S_1	S_2	C_L
t_{pd1}	CLOSED	CLOSED	50 pF
t_{pd0}	CLOSED	CLOSED	50 pF
t_{0H}	CLOSED	CLOSED	5 pF *
t_{1H}	CLOSED	CLOSED	5 pF *
t_{H0}	CLOSED	OPEN	50 pF
t_{H1}	OPEN	CLOSED	50 pF

*Approximate value of jig capacitance only

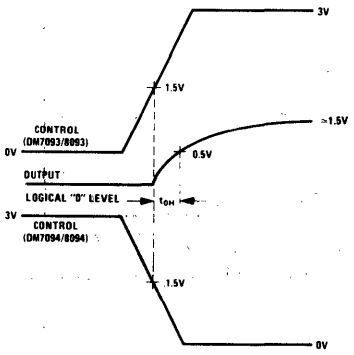
switching time waveforms

INPUT CHARACTERISTICS
FREQ: 1 MHz
PULSE WIDTH: 100 ns
$t_r = t_f \leq 10$ ns
AMPLITUDE = 3V

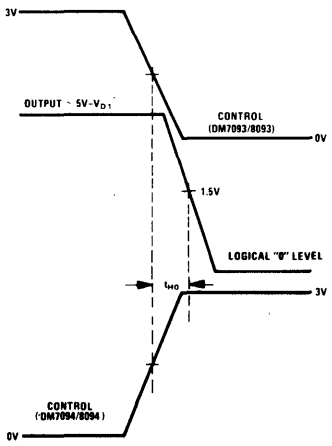
t_{pd1} & t_{pd0}



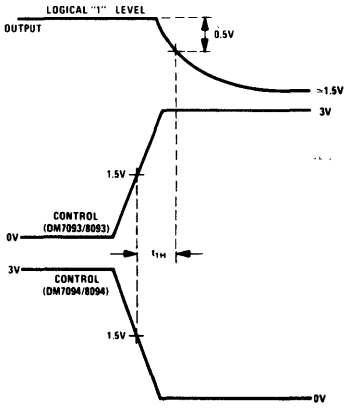
t_{0H}



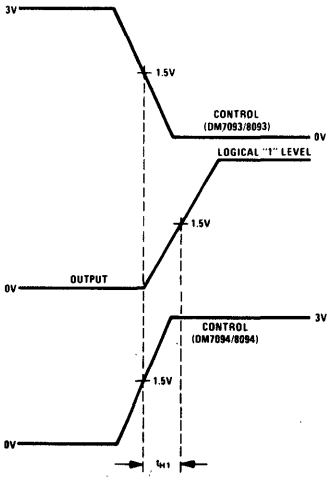
t_{H0}



t_{1H}



t_{H1}



Tri-State Logic

DM7230/DM8230 tri-state demultiplexer general description

The DM7230/DM8230 demultiplexer is another device in National's tri-state logic family.

Digital signals applied to two input lines can be routed to two-of-four output lines depending upon the logic on the Address inputs. Outputs can be directly connected to other similar outputs for use in bus-organized systems.

features

- Series 54/74 compatible
- 20 ns propagation delay
- Data complement capability
- Very low output impedance—high drive capability
- Separate input disable controls
- High-impedance output state which allows many outputs to be connected to a common bus-line.

mode of operation

COMPLEMENT AND DATA INPUTS

When Complement A is a logical "1", Data A will appear inverted at the output. When Complement A is a logical "0", Data A will appear non-inverted at the output.

This function is accomplished on the chip through the use of a two-input exclusive-OR gate with Complement A and Data A as the two inputs. Therefore, the A information that is routed to the outputs is actually (Complement A ⊕ Data A). That this is the case may be verified by examining the logic diagram.

The two inputs of this exclusive-OR gate have identical characteristics, allowing the functions of these two inputs to be reversed. Also the propagation delay from either input to the output will be the same. This is also true for the Complement B and Data B inputs.

ADDRESS INPUTS

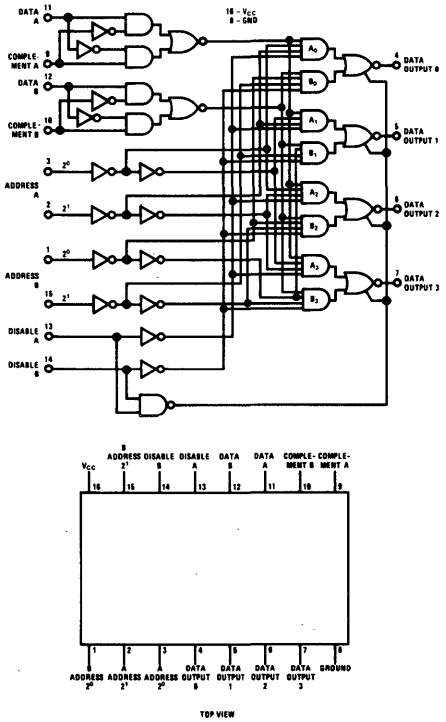
The Address A inputs select to which of the four outputs A information will be routed. The same is true for the Address B inputs and B information. If A and B information are both routed to the same output simultaneously, that output will be a logical "0" if either the A or B information is a logical "0". All outputs which are not selected for either A or B information will be in the logical "1" state.

DISABLE INPUTS

The Disable inputs are similar to higher order Address inputs in that when Disable A is a logical "1", A information is not routed to any output. All four outputs are nonselected for A information. The same is true for Disable B and B information. The Disable inputs have the additional feature that when both Disable A and Disable B are a logical "1" all outputs go to the High Impedance state. When multiple outputs are connected to a bus line, only one device at a time can be in the

(Continued on Page 22)

logic and connection diagrams



logic table

DATA A	COMP. A	DATA B	COMP. B	ADDRESS A 2^1	ADDRESS A 2^0	ADDRESS B 2^1	ADDRESS B 2^0	DIS. A	DIS. B	OUT 0	OUT 1	OUT 2	OUT 3
0	0	X	X	0	0	X	X	0	1	0	1	1	1
0	1	X	X	0	0	X	X	0	1	1	1	1	1
1	0	X	X	0	0	X	X	0	1	1	1	1	1
1	1	X	X	0	0	X	X	0	1	0	1	1	1
0	0	X	X	0	1	X	X	0	1	1	0	1	1
0	1	X	X	0	1	X	X	0	1	1	1	1	1
1	0	X	X	0	1	X	X	0	1	1	1	1	1
1	1	X	X	0	1	X	X	0	1	0	1	1	1
0	0	X	X	1	0	X	X	0	1	1	1	0	1
0	1	X	X	1	0	X	X	0	1	1	1	1	1
1	0	X	X	1	0	X	X	0	1	1	1	1	1
1	1	X	X	1	0	X	X	0	1	1	1	0	1
0	0	X	X	1	1	X	X	0	1	1	1	1	0
0	1	X	X	1	1	X	X	0	1	1	1	1	1
1	0	X	X	1	1	X	X	0	1	1	1	1	1
1	1	X	X	1	1	X	X	0	1	1	1	1	0
X	X	0	0	X	X	0	0	1	0	0	1	1	1
X	X	0	1	X	X	0	0	1	0	1	1	1	1
X	X	1	0	X	X	0	0	1	0	1	1	1	1
X	X	1	1	X	X	0	0	1	0	0	1	1	1
X	X	0	0	X	X	0	1	1	0	1	0	1	1
X	X	0	1	X	X	0	1	1	0	1	1	1	1
X	X	1	0	X	X	0	1	1	0	1	1	0	1
X	X	1	1	X	X	0	1	1	0	1	1	1	1
X	X	0	0	X	X	1	0	1	0	1	1	1	0
X	X	0	1	X	X	1	0	1	0	1	1	1	1
X	X	1	0	X	X	1	0	1	0	1	1	1	1
X	X	1	1	X	X	1	0	1	0	1	1	0	1
X	X	0	0	X	X	1	1	1	0	1	1	1	1
X	X	0	1	X	X	1	1	1	0	1	1	1	1
X	X	1	0	X	X	1	1	1	0	1	1	1	1
X	X	1	1	X	X	1	1	1	0	0	1	1	1
X	X	X	X	X	X	X	X	1	1	Hi Z	Hi Z	Hi Z	Hi Z

absolute maximum ratings

Supply Voltage	7V
Input Voltage	5.5V
Output Voltage	5.5V
Time that two bus-connected devices may be in opposite low impedance states simultaneously. (5% duty cycle)	10 msec
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	
DM7230	−55°C to +125°C
DM8230	0°C to +70°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics (Note 1)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	DM7230	V_{CC} = 4.5V	2.0			V
	DM8230	V_{CC} = 4.75V				
Logical "0" Input Voltage	DM7230	V_{CC} = 4.5V			0.8	V
	DM8230	V_{CC} = 4.75V				
Logical "1" Output Voltage	DM7230	V_{CC} = 4.5V, I_{OUT} = −2 mA	2.4	3.5		V
	DM8230	V_{CC} = 4.75V, I_{OUT} = −5.2 mA				
Logical "0" Output Voltage	DM7230	V_{CC} = 4.5V				
	DM8230	V_{CC} = 4.75V I_{OUT} = 16 mA		0.2	0.4	V
Logical "0" Input Current	DM7230	V_{CC} = 5.5V				
	DM8230	V_{CC} = 5.25V V_{IN} = 0.4V				
		Disable inputs		−2.0	−3.2	mA
		All other inputs		−1.0	−1.6	mA
Logical "1" Input Current	DM7230	V_{CC} = 5.5V				
	DM8230	V_{CC} = 5.25V V_{IN} = 2.4V				
		Disable inputs			80	μA
		All other inputs			40	μA
Logical "1" Input Current	DM7230	V_{CC} = 5.5V				
	DM8230	V_{CC} = 5.25V V_{IN} = 5.5V			1.0	mA
Output Disable Current	DM7230	V_{CC} = 5.5V V_O = 2.4V			40	μA
	DM8230	V_{CC} = 5.25V V_O = 0.4V			−40	μA
Output Short Current (Note 2)	DM7230	V_{CC} = 5.5V	−30			
	DM8230	V_{CC} = 5.25V V_O = 0.0V	−28		−70	mA
Supply Current	DM7230	V_{CC} = 5.5V				
	DM8230	V_{CC} = 5.25V V_{IN} = 5.0V		48	75	mA
Input Diode Clamp Voltage		V_{CC} = 5.0V, T_A = 25°C I_{IN} = −12 mA			−1.5	V
Output Diode Clamp Voltage		V_{CC} = 5.0V, T_A = 25°C				
		I_{OUT} = −12 mA			−1.5	V
		I_{OUT} = +12 mA			V_{CC} +1.5	V
Propagation Delay to Logical "1" from Data or Complement Input, t_{pd1}		V_{CC} = 5.0V, T_A = 25°C C_L = 50 pF				
		Noninverting		13	24	ns
		Inverting		20	36	ns
Propagation Delay to Logical "0" from Data or Complement Input, t_{pd0}		V_{CC} = 5.0V, T_A = 25°C C_L = 50 pF				
		Noninverting or Inverting		18	26	ns
Propagation Delay to Logical "1" from Address Input, t_{pd1} (Note 3)		V_{CC} = 5.0V, T_A = 25°C C_L = 50 pF		20	36	ns
Propagation Delay to Logical "0" from Address Input, t_{pd0} (Note 3)		V_{CC} = 5.0V, T_A = 25°C C_L = 50 pF		20	30	ns
Propagation Delay to Logical "1" from Disable Input, t_{pd1} (Note 4)		V_{CC} = 5.0V, T_A = 25°C C_L = 50 pF		13	25	ns
Propagation Delay to Logical "0" from Disable Input, t_{pd0} (Note 4)		V_{CC} = 5.0V, T_A = 25°C C_L = 50 pF		16	25	ns
Delay from Disable Input to High Impedance State (Note 5), t_{IH}		V_{CC} = 5.0V, T_A = 25°C		7	14	ns
t_{OH}				15	27	ns
Delay from Disable Input to Low Impedance State (Note 5), t_{HI}		V_{CC} = 5.0V, T_A = 25°C C_L = 50 pF		15	23	ns
t_{HO}				18	27	ns

Note 1: Min/max values apply across the −55°C to +125°C temperature range for the DM7230 and across the 0°C to 70°C range for the DM8230 unless otherwise specified. Typicals are given for T_A = 25°C and V_{CC} = 5.0V.

Note 2: Only one output at a time should be short circuited.

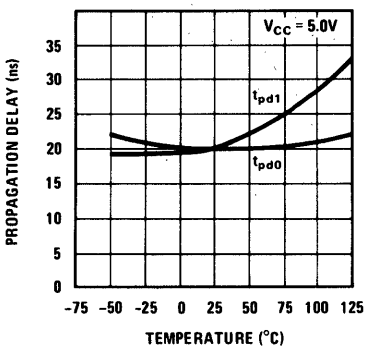
Note 3: The only conditions under which a t_{pd0} from the Address inputs can be observed is when an output goes from being nonselected to being selected and the information being routed to that output is a logical "0". If the information had been a logical "1", no change would have occurred and no measurement could have been made. Similarly, the only time a t_{pd1} from the Address inputs can be observed, is when an output goes from being selected to being nonselected and the information that had been routed to that output was a logical "0". If the information had been a logical "1", no change would have occurred and no measurement could have been made.

Note 4: Information in Note 3 concerning t_{pd0} and t_{pd1} from the address inputs are applicable here also.

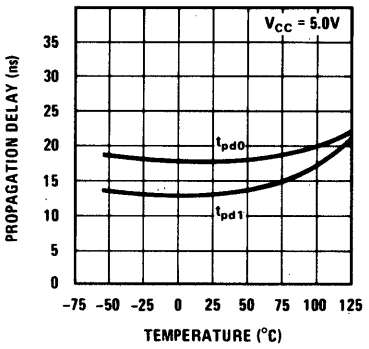
Note 5: All delays involving transitions to or from the High Impedance state are measured with respect to the Disable inputs. For example, with A information at a logical "0" and Disable B at a logical "1" the selected output will go from a logical "0" to the High Impedance state some time, t_{OH}, after Disable A has gone from a logical "0" to a logical "1"

typical performance

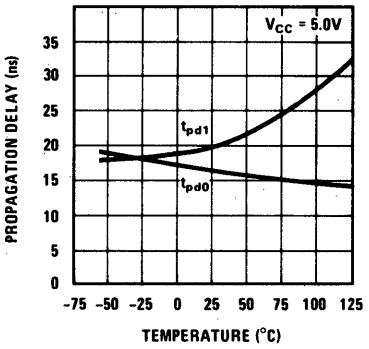
Propagation Delay from Address to Output (Inverted)



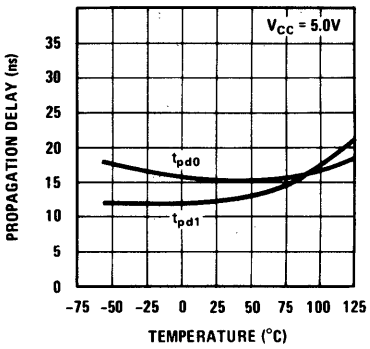
Propagation Delay from Data or Complement to Output (Noninverted)



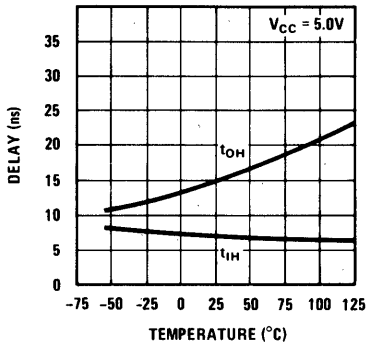
Propagation Delay from Data or Complement to Output (Inverted)



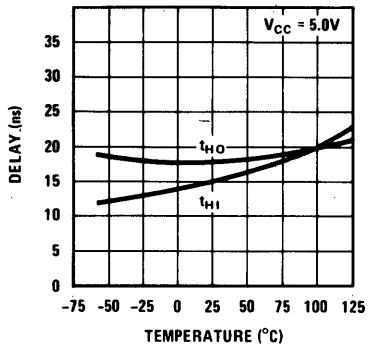
Propagation Delay from Disable to Output



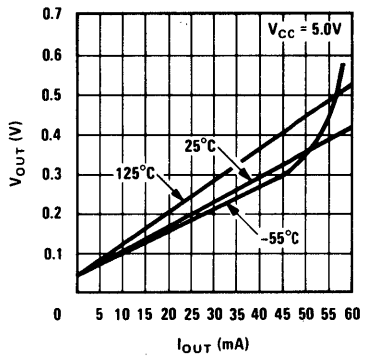
Delay from Disable to High Impedance State



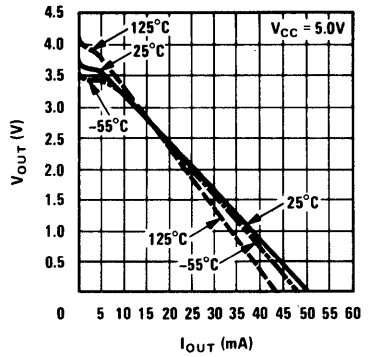
Delay from Disable to Low Impedance State



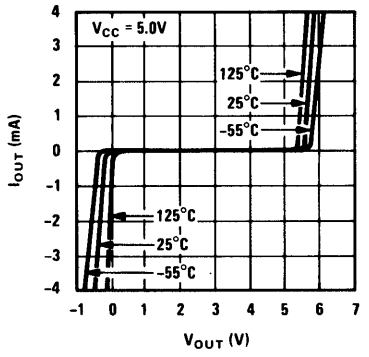
Logical "0" Output Voltage vs Sink Current



Logical "1" Output Voltage vs Source Current



I_{OUT} vs V_{OUT} High Impedance Output State



mode of operation (cont.)

normal low impedance state. All others should be gated into the high impedance state (Figure 1). The selected device therefore has the normal TTL low impedance output providing good capacitive drive capability and waveform integrity especially during the transition from the logical "0" to logical "1" state. The other outputs—in the high impedance state—take only a small amount of leakage current from the low impedance outputs. Since the logical "1" output current of the selected device is 13 times that of a conventional Series 54/74 device (5.2 mA vs 400 μA), the output is easily able to supply that leakage current to as many as 127 other DM7230/DM8230's and still have available drive for the bus-line. (Figure 2)

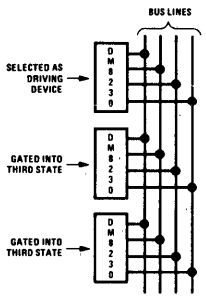


Figure 1

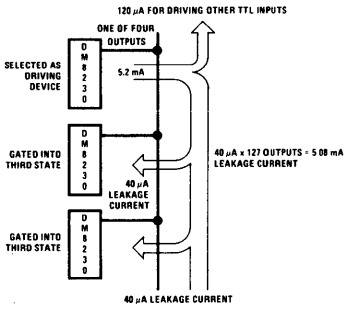
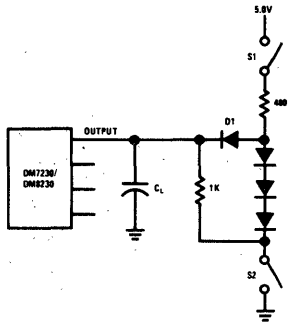


Figure 2

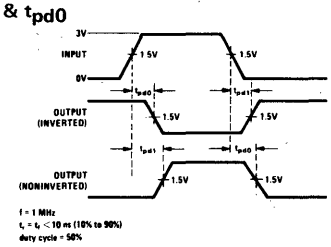
ac test circuit



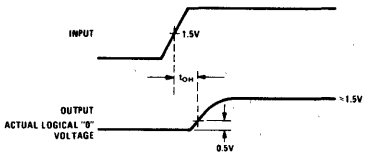
	SWITCH S1	SWITCH S2	C_L
t_{pd1}	closed	closed	50 pF
t_{pd0}	closed	closed	50 pF
t_{OH}	closed	closed	5 pF
t_{IH}	closed	closed	5 pF
t_{HO}	closed	open	50 pF
t_{HI}	open	closed	50 pF

switching time waveforms

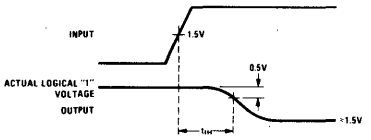
t_{pd1} & t_{pd0}



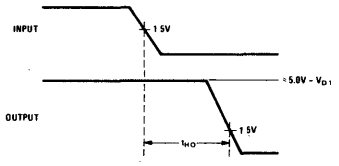
t_{OH}



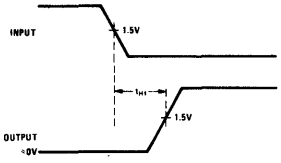
t_{IH}



t_{HO}



t_{HI}



Tri-State Logic

DM7551/DM8551 tri-state quad-D flip flop

general description

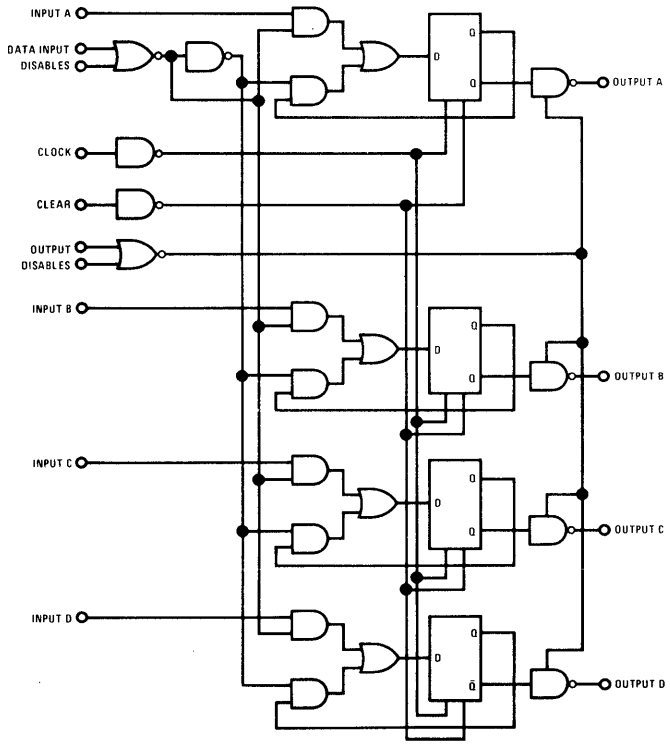
The DM7551/DM8551 is a tri-state logic device which provides four D-type flip flops in one package which operate synchronously from a common clock. Features of the device are:

- Series 54/74 compatible
- 23 ns typical propagation delay
- 250 mW typical power dissipation
- Outputs directly connectable for bus-line operation
- A "do-nothing" state accomplished without gating the clock
- Simple disable encoding

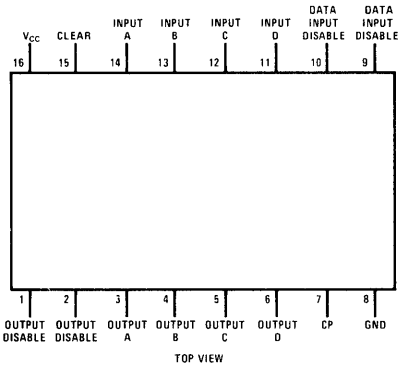
A unique three-state output allows the device to be used in bus-organized systems. The outputs can be directly wired to outputs of other DM7551/DM8551's without encountering the problems normally met with "collector-ORing" TTL circuits. This is accomplished by gating the normally low impedance logical "1" or logical "0" output into a high impedance state.

(Continued on page 26)

logic and connection diagrams



Dual-In-Line Package



TRUTH TABLE (Both Output Disables Low)

t_n		t_{n+1}
DATA INPUT DISABLE	DATA INPUT	OUTPUT
Logical "1" on 1 or both inputs	X	On
Logical "0" on both inputs	1	1
Logical "0" on both inputs	0	0

X = Don't Care

absolute maximum ratings (Note 1)

Supply Voltage		7V
Input Voltage		5.5V
Output Voltage		5.5V
Storage Temperature Range		−65°C to +150°C
Operating Temperature Range	DM7551	−55°C to +125°C
	DM8551	0°C to +70°C
Lead Temperature (Soldering, 10 sec)		300°C
Time that 2 bus-connected devices may be in opposite low impedance states simultaneously		Indefinitely

electrical characteristics (Note 2)

PARAMETERS		CONDITIONS		MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	DM7551	V_{CC} = 4.5V		2.0			V
	DM8551	V_{CC} = 4.75V					
Logical "0" Input Voltage	DM7551	V_{CC} = 4.5V				0.80	V
	DM8551	V_{CC} = 4.75V					
Logical "1" Output Voltage	DM7551	V_{CC} = 4.5V	I_{OUT} = −2.0 mA	2.4	3.3		V
	DM8551	V_{CC} = 4.75V	I_{OUT} = −5.2 mA				
Logical "0" Output Voltage	DM7551	V_{CC} = 4.5V					
	DM8551	V_{CC} = 4.75V	I_{OUT} = 16 mA		0.2	0.40	V
Logical "0" Input Current	DM7551	V_{CC} = 5.5V					
	DM8551	V_{CC} = 5.25V	V_{IN} = 0.40V		−1.0	−1.6	mA
Logical "1" Input Current	DM7551	V_{CC} = 5.25V	V_{IN} = 2.4V			40	μA
	DM8551	V_{CC} = 5.25V	V_{IN} = 5.5V			1	mA
Output Current	DM7551	V_{CC} = 5.5V	V_O = 2.4V			40	μA
In High Impedance State	DM8551	V_{CC} = 5.25V	V_O = 0.4V			−40	μA
Supply Current	DM7551	V_{CC} = 5.5V			50	72	mA
	DM8551	V_{CC} = 5.25V					
Output Short Current (Note 3)	DM7551	V_{CC} = 5.5V	V_{OUT} = 0.0V	−30		−70	mA
	DM8551	V_{CC} = 5.25V					
Maximum Clock Frequency		V_{CC} = 5.0V, C_L = 50 pF	T_A = 25°C		25		MHz
Propagation Delay from Clock to Logical "0", t_{pd0}		V_{CC} = 5.0V, C_L = 50 pF	T_A = 25°C	11	20	31	ns
Propagation Delay from Clock to Logical "1", t_{pd1}		V_{CC} = 5.0V, C_L = 50 pF	T_A = 25°C	11	27	43	ns
Input Data Setup Time, $t_{S\,DATA}$		V_{CC} = 5.0V	T_A = 25°C		3	10	ns
Input Data Hold Time, $t_{H\,DATA}$		V_{CC} = 5.0V	T_A = 25°C		4	10	ns
Input Disable Setup Time, $t_{S\,DIS}$		V_{CC} = 5.0V	T_A = 25°C		10	17	ns
Input Disable Hold Time, $t_{H\,DIS}$		V_{CC} = 5.0V	T_A = 25°C		−4	2	ns
Delay from "Output Disable" to High Impedance State (from Logical "1" Level), t_{1H}		V_{CC} = 5.0V	T_A = 25°C	3	5	30	ns
Delay from "Output Disable" to High Impedance State (from Logical "0" Level), t_{0H}		V_{CC} = 5.0V	T_A = 25°C	3	11	30	ns
Delay from "Output Disable" to Logical "1" Level (from High Impedance State), t_{H1}		V_{CC} = 5.0V	T_A = 25°C	7	16	30	ns
Delay from "Output Disable" to Logical "0" Level (from High Impedance State), t_{H0}		V_{CC} = 5.0V	T_A = 25°C	7	21	30	ns
Propagation Delay from Clear to Output, t_{pdR}		V_{CC} = 5.0V	T_A = 25°C		18	27	ns

Note 1: Absolute maximum ratings are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range", they are not meant to imply operating conditions.

Note 2: Unless otherwise specified the min-max limits across the −55°C to +125°C temperature range for the DM7551 and across the 0°C to 70°C temperature range for the DM8551. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

Note 3: Only 1 output at a time should be shorted.

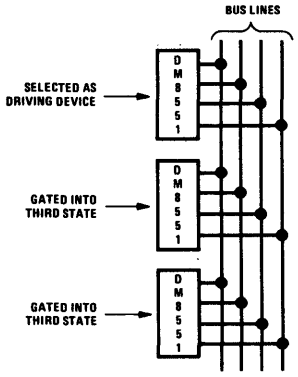


FIGURE 1

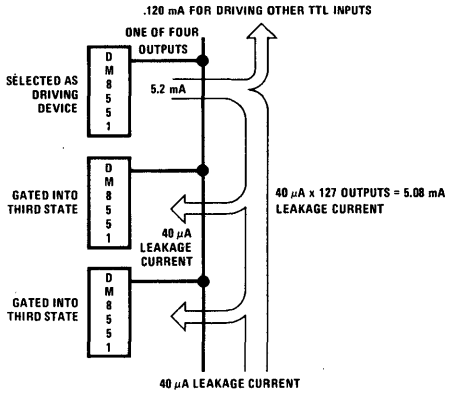


FIGURE 2

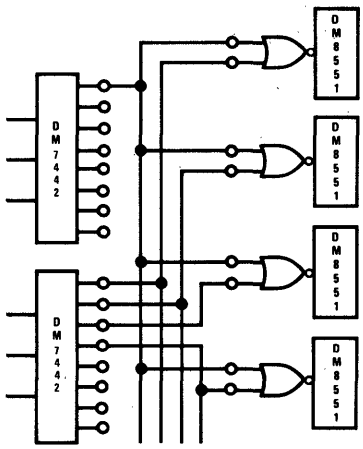


FIGURE 3

general description (con't)

The high impedance state occurs on all outputs of all devices except the four outputs of the one device selected (Figure 1). The result is that the selected device has a normal TTL low impedance output providing good capacitive drive capability and waveform integrity especially during the transition from a logical "0" to a logical "1". The other outputs are all in the "third-state" and take only a small amount of leakage current from the driving outputs. Since the logical "1" output current of the selected device is 13 times that of a normal Series 54/74 output (5.2 mA vs 400 μA), the output is easily able to supply that leakage current to as many as 127 connected devices and still retain enough drive for a full Series 54/74 fan-out of 3 at the end of the bus line (Figure 2).

A two-input NOR gate facilitates selection of the driving device through the use of only two octal decoders for as many as 64 DM7551/DM8551's (Figure 3).

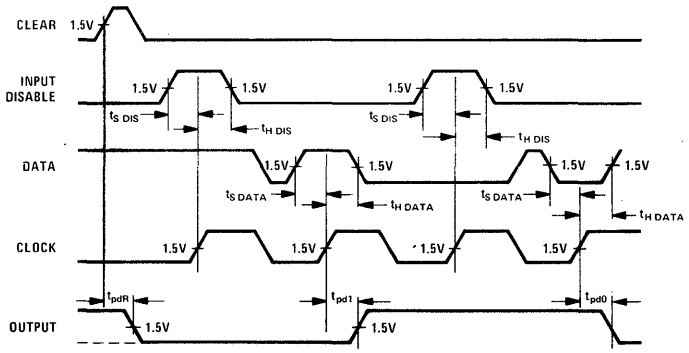
A problem inherent in conventional D-type flip flops is that it is impossible to code the data input in such a way as to cause the flip flop to remain in its present state when clocked. Because flexibility is not as great as with a J-K flip flop (and its J=0, K=0 state), to keep a D-type flip flop in its present state it is usually necessary to gate the clock, which increases the danger of false-clocking. The DM7551/DM8551 contains a gated input disable which does not disrupt clocking, but rather recirculates information from the Q output to the D input. In this manner the flip flop does not change state and the possibility of false-clocking is eliminated.

The following logic levels control the device:

- Clocking occurs on the positive-going transition.
- Clearing is enabled by taking the input to a Logical "1" level.
- Outputs are placed in the "third-state" if either of the two Output Disable inputs is taken to a Logical "1" level.
- The flip flops will remain in their previous state when clocked so long as either of the two Data Input Disable inputs is taken to a Logical "1" level.

The DM7551/DM8551 is completely compatible with other Series 54/74 devices.

switching time waveforms



Tri-State Logic

DM7831/DM8831 tri-state line driver

general description

Through simple logic control, the DM7831/DM8831 can be used as either a quad single-ended line driver or a dual differential line driver. It is specifically designed for party line (bus-organized) systems. Key features include:

- Series 54/74 compatible
- 17 ns propagation delay
- Very low output impedance—high drive capability
- 40 mA sink and source currents
- Gating control to allow either single-ended or differential operation
- High impedance output state which allows many outputs to be connected to a common bus line.

mode of operation

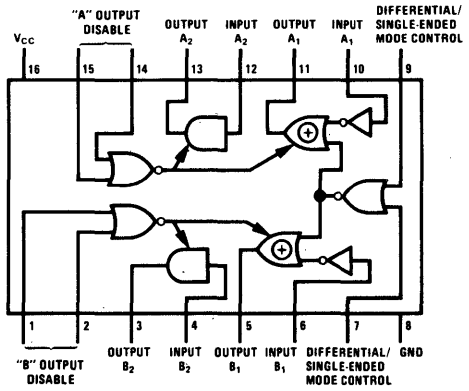
To operate as a quad single-ended line driver apply logical "0"s to the Output Disable pins (to keep the outputs in the normal low impedance mode) and apply logical "0"'s to both Differential/Single-ended Mode Control inputs. All four channels will then operate independently and no signal inversion will occur between inputs and outputs.

To operate as a dual differential line driver apply logical "0"s to the Output Disable pins and apply at least one logical "1" to the Differential/Single-ended Mode Control inputs. The inputs to the A channels should be connected together and the inputs to the B channels should be connected together. In this mode the signals applied to the resulting inputs will pass non-inverted on the A_2 and B_2 outputs and inverted on the A_1 and B_2 outputs.

When operating in a bus-organized system with outputs tied directly to outputs of other

(Continued on page 29)

connection and logic diagram



truth-table (Shown for A Channels Only)

"A" OUTPUT DISABLE		DIFFERENTIAL/ SINGLE-ENDED MODE CONTROL		INPUT A_1	OUTPUT A_1	INPUT A_2	OUTPUT A_2
0	0	0	0	Logical "1" or Logical "0"	Same as Input A_1	Logical "1" or Logical "0"	Same as Input A_2
0	0	X	1	Logical "1" or Logical "0"	Opposite of Input A_1	Logical "1" or Logical "0"	Same as Input A_2
		1	X				
1	X	X	X	X	High impedance state	X	High impedance state
X	1						

X = Don't Care

absolute maximum ratings

Supply Voltage	7V
Input Voltage	5.5V
Output Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range DM7831	−55°C to +125°C
DM8831	0°C to +70°C
Lead Temperature (Soldering, 10 sec.)	300°C
Time that 2 bus-connected devices may be in opposite low impedance states simultaneously	10 ms

electrical characteristics (Note 1)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	DM7831	V_{CC} = 4.5V		2.0			V
	DM8831	V_{CC} = 4.75V					
Logical "0" Input Voltage	DM7831	V_{CC} = 4.5V				0.8	V
	DM8831	V_{CC} = 4.75V					
Logical "1" Output Voltage	DM7831	V_{CC} = 4.5V	I_O = −40 mA	1.8	2.8		V
			I_O = −2 mA	2.4	3.1		V
	DM8831	V_{CC} = 4.75V	I_O = −40 mA	1.8	2.8		V
			I_O = −5.2 mA	2.4	3.0		V
Logical "0" Output Voltage	DM7831	V_{CC} = 4.5V	I_O = 40 mA		0.29	0.50	V
			I_O = 32 mA			.40	V
	DM8831	V_{CC} = 4.75V	I_O = 40 mA		0.29	0.50	V
			I_O = 32 mA			.40	V
Logical "1" Input Current	DM7831	V_{CC} = 5.5V	V_{IN} = 5.5V			1	mA
	DM8831	V_{CC} = 5.25V	V_{IN} = 2.4V			40	μA
Logical "0" Input Current	DM7831	V_{CC} = 5.5V	V_{IN} = 0.4V		−1.0	−1.6	mA
	DM8831	V_{CC} = 5.25V					
Output Disable Current	DM7831	V_{CC} = 5.5V	V_O = 2.4V			40	μA
	DM8831	V_{CC} = 5.25V	V_O = 0.4V			−40	μA
Output Short Circuit Current	DM7831	V_{CC} = 5.5V		−40 (Note 2)	−100	−120 (Note 2)	mA
	DM8831	V_{CC} 5.25V					
Supply Current	DM7831	V_{CC} = 5.5V			57	90	mA
	DM8831	V_{CC} = 5.25V					
Input Diode Clamp Voltage		V_{CC} = 5.0V, T_A = 25°C I_{IN} = −12 mA				−1.5	V
Output Diode Clamp Voltage		V_{CC} = 5.0V, T_A = 25°C I_{OUT} = −12 mA				−1.5	V
		I_{OUT} = +12 mA				V_{CC}+1.5	V
Propagation Delay to a Logical "0" from Inputs A_1, A_2, B_1, B_2, Differential Single-ended Mode Control to Outputs, t_{pd0}		V_{CC} = 5.0V, T_A = 25°C			13	25	ns
Propagation Delay to a Logical "1" from Inputs A_1, A_2, B_1, B_2, Differential Single-ended Mode Control to Outputs, t_{pd1}		V_{CC} = 5.0V, T_A = 25°C			13	25	ns
Delay from Disable Inputs to High Impedance State (from Logical "1" Level), t_{1H}		V_{CC} = 5.0V, T_A = 25°C			6	12	ns
Delay from Disable Inputs to High Impedance State (from Logical "0" Level), t_{0H}		V_{CC} = 5.0V, T_A = 25°C			14	22	ns
Propagation Delay from Disable Inputs to Logical "1" Level (from High Impedance State), t_{H1}		V_{CC} = 5.0V, T_A = 25°C			14	22	ns
Propagation Delay from Disable Inputs to Logical "0" Level (from High Impedance State), t_{H0}		V_{CC} = 5.0V, T_A = 25°C			18	27	ns

Note 1: Unless otherwise specified min/max limits apply across the −55° to +125°C temperature range for the DM7831 and across the 0°C to 70°C temperature range for the DM8831. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

Note 2: Applies for T_A = 125°C only. Only one output should be shorted at a time.

mode of operation (cont.)

DM7831/DM8831's (Figure 1), all devices except one must be placed in the "high impedance" state. This is accomplished by ensuring that a logical "1" is applied to at least one of the Output Disable pins of each device which is to be in the "high impedance" state. A NOR gate was purposely chosen for this function since it is possible with only two DM5442/DM7442, BCD-to-decimal decoders, to decode as many as 100 DM7831/DM8831's (Figure 2).

The unique device whose Disable inputs receive two logical "0" levels assumes the normal low impedance output state, providing good capacitive drive capability and waveform integrity especially during the transition from the logical "0" to logical "1" state. The other outputs—in the high impedance state—take only a small amount of leakage current from the low impedance outputs. Since the logical "1" output current from the selected device is 100 times that of a conventional Series 54/74 device (40 mA vs. 400 μA), the output is easily able to supply that leakage current for several hundred other DM7831/DM8831's and still have available drive for the bus line (Figure 3).

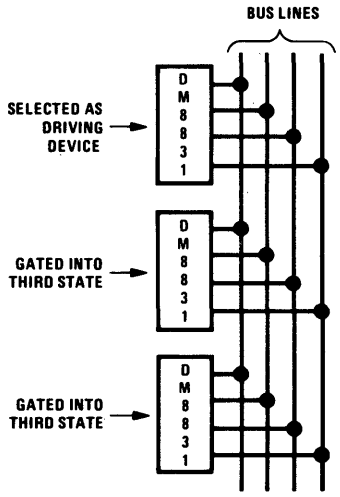


Figure 1

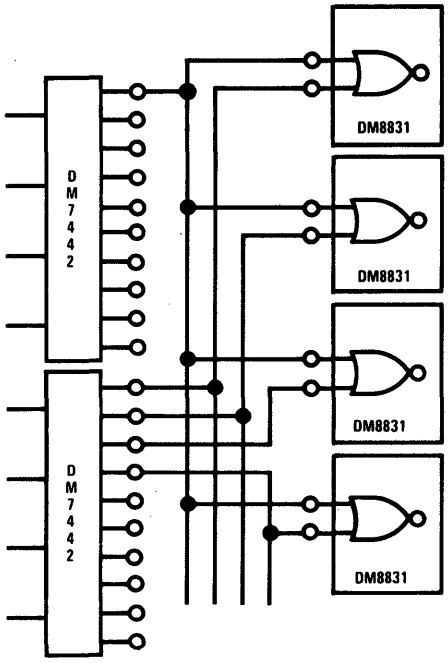


Figure 2

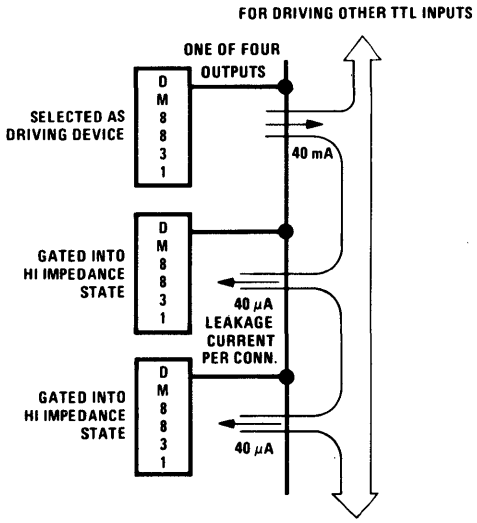
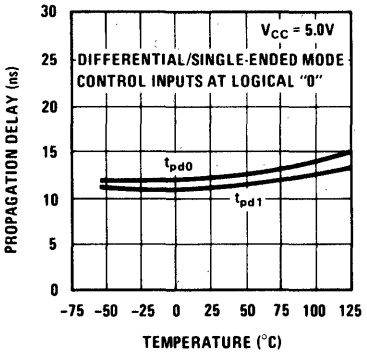


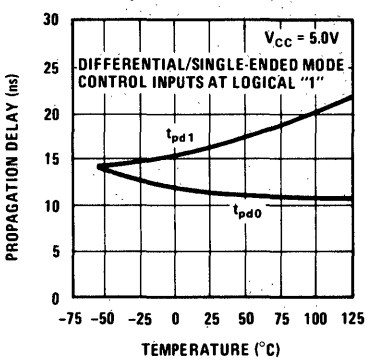
Figure 3

typical performance characteristics

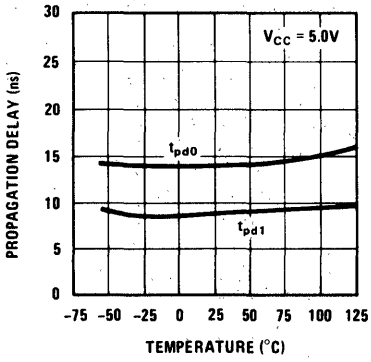
Propagation Delay from Input to Output (Channel 1)



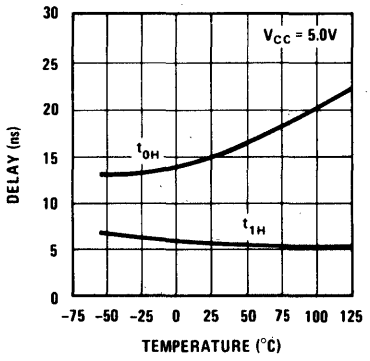
Propagation Delay from Input to Output (Channel 1)



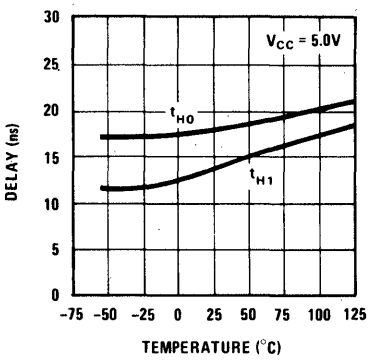
Propagation Delay from Input to Output (Channel 2)



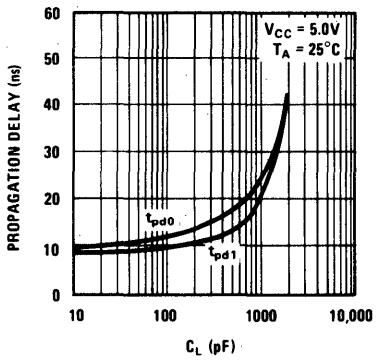
Delay from Disable to High Impedance State



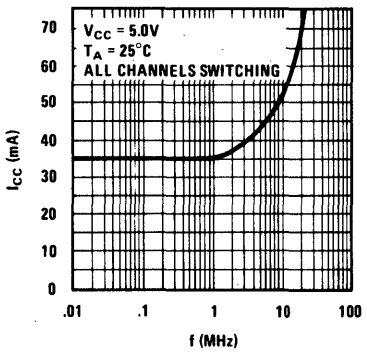
Delay from Disable to Low Impedance State



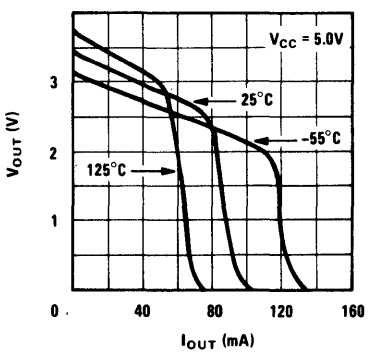
Propagation Delay vs Load Capacitance



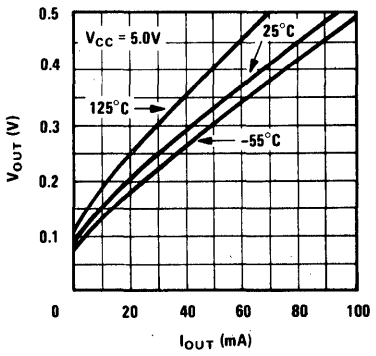
Total Supply Current vs Frequency



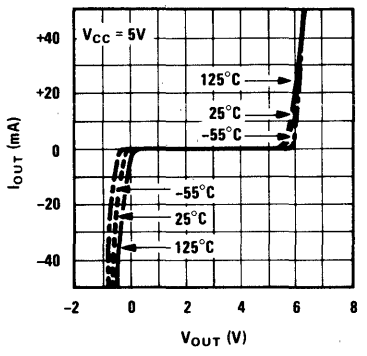
Logical "1" Output Voltage vs Source Current



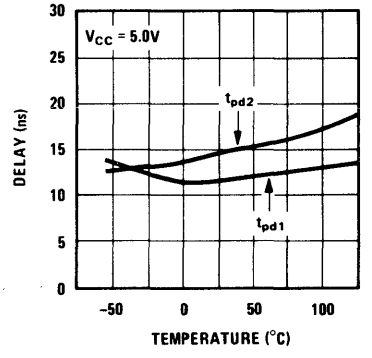
Logical "0" Output Voltage vs Sink Current

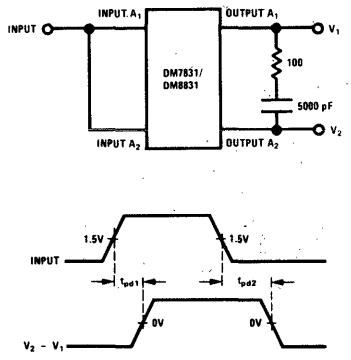


I_{OUT} vs V_{OUT} High Impedance Output State



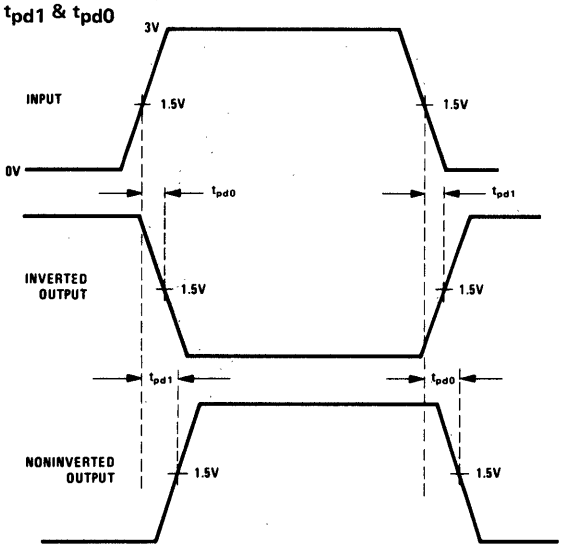
Propagation Delay in Differential Mode





switching time waveforms

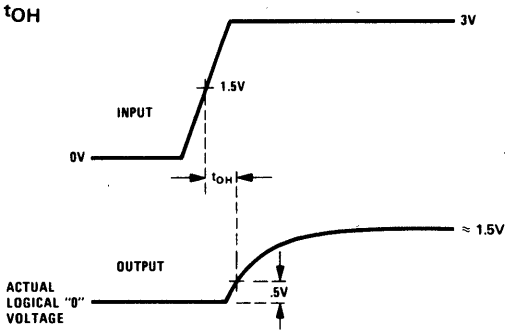
t_{pd1} & t_{pd0}



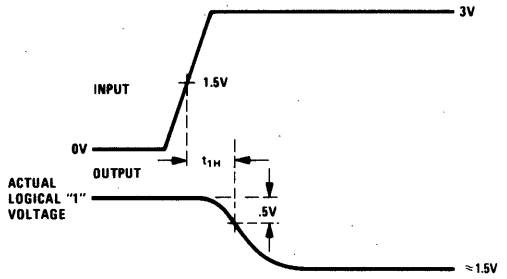
Input characteristic

Amplitude = 3V
frequency = 1 MHz, 50% duty cycle.
$t_r = t_f \leq 10$ nsec (10% to 90%)

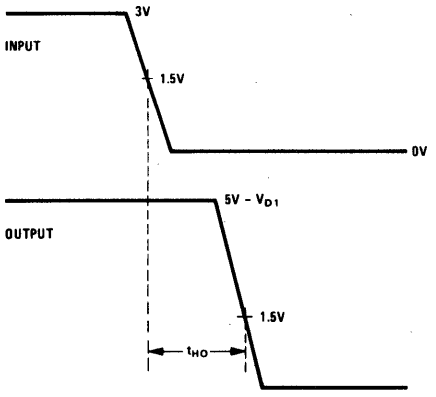
t_{OH}



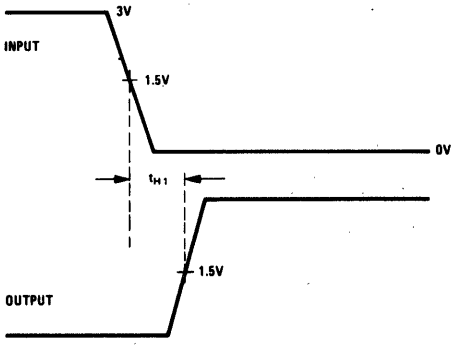
t_{1H}



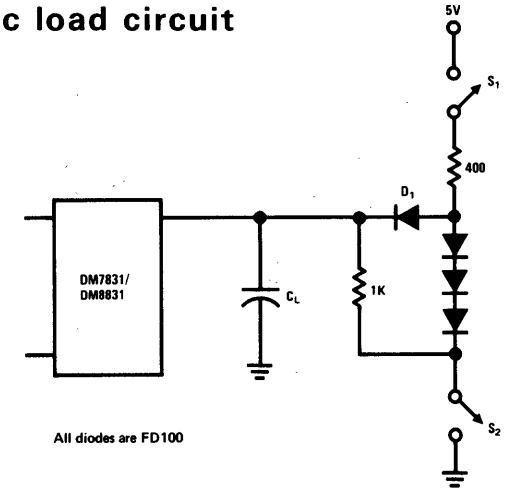
t_{HO}



t_{H1}



ac load circuit



All diodes are FD100

	Switch S_1	Switch S_2	C_L
t_{pd1}	closed	closed	50 pF
t_{pd0}	closed	closed	50 pF
t_{OH}	closed	closed	* 5 pF
t_{1H}	closed	closed	* 5 pF
t_{HO}	closed	open	50 pF
t_{H1}	open	closed	50 pF

*jig capacitance

Gates, Series 54/74

TTL(series 54N) gates

general description

For military temperature range (−55°C to +125°C) applications, National Semiconductor's DM5400 Series TTL gates described herein provide the popular Series 54 type products in the molded dual-in-line package.

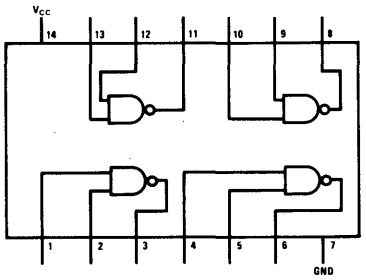
Individual device specifications can be obtained from the appropriate DM7400 Series data sheets. In only two areas do the Series 54N and Series 74N differ:

	Series 54N	Series 74N
Operating Temperature Range	−55°C to +125°C	0°C to 70°C
Allowable V_{CC} Range	4.5V to 5.5V	4.75V to 5.25V

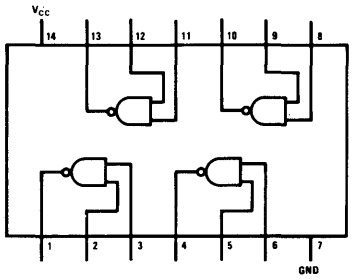
package description

The silicone dual-in-line package has been proven to be able to meet all, and exceeds many, of the requirements demanded by military environments. All devices are subjected to 100% temperature cycling from −65°C to +150°C fifteen times with a 15-minute dwell time at each extreme. After this thermal cycling, all units are 100% electrically tested to insure data sheet conformance.

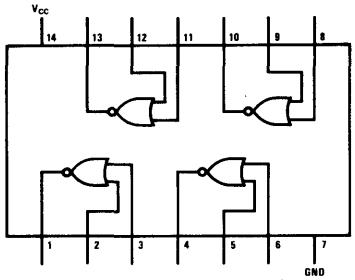
connection diagrams



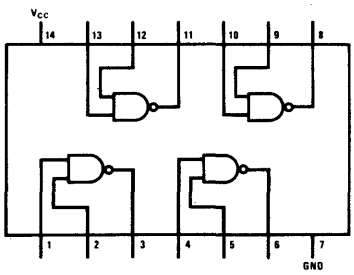
DM5400N (SN5400N)
Quad 2-Input Gate



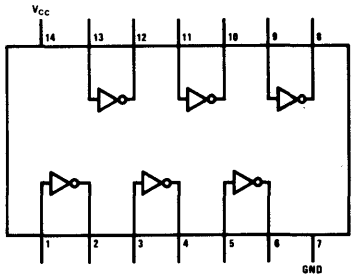
DM5401N (SN5401N)
Quad 2-Input Gate
(Open Collector)



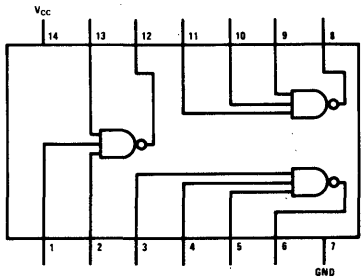
DM5402N (SN5402N)
Quad 2-Input NOR Gate



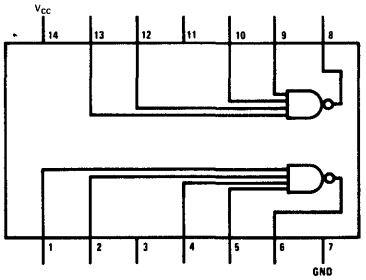
DM5403N (SN5403N)
Quad 2-Input Gate
(Open Collector)



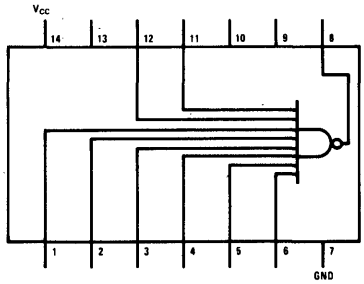
DM5404N (SN5404N)
Hex Inverter



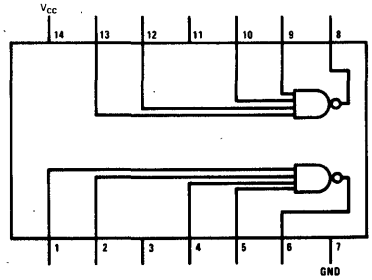
DM5410N (SN5410N)
Triple 3-Input Gate



DM5420N (SN5420N)
Dual 4-Input Gate

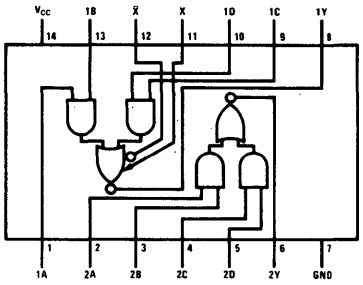


DM5430N (SN5430N)
Eight-Input Gate



DM5440N (SN5440N)
Dual 4-Input Buffer

connection diagrams

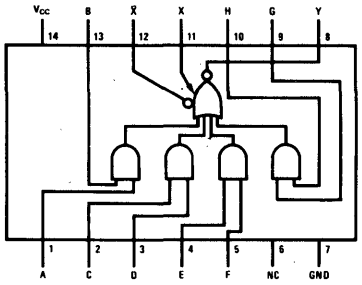


$Y = \overline{(AB) + (CD) + X}$

$X = ABCD$ from DM7060

NOTES: Expander nodes X and $\overline{X}$ are on the DM5450 only. If not used, leave open. Make no external connection to pins 11 and 12 of the DM5451. A total of four expander gates may be connected to the DM5450 expandable gates.

DM5450N (SN5450N)
DM5451N (SN5451N)
Expandable Dual AND-OR-INVERT Gate

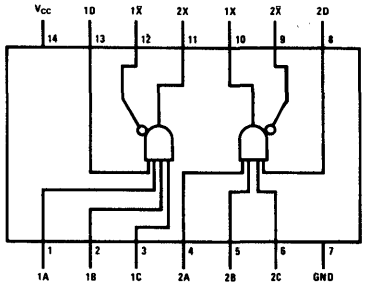


$Y = \overline{(AB) + (CD) + (EF) + (GH) + X}$

$X = ABCD$ from DM7060

NOTES: Expander nodes X and $\overline{X}$ are on the DM5453 only. If not used, leave open. Make no external connection to pins 11 and 12 of the DM5454. A total of four expander gates may be connected to the DM5453 expandable gate.

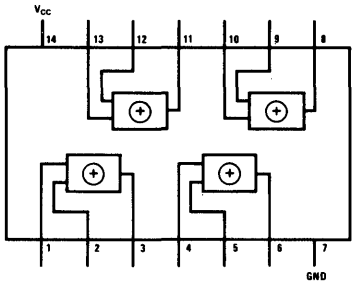
DM5453N (SN5453N)
DM5454N (SN5454N)
Expandable AND-OR-INVERT Gate



$X = ABCD$

NOTE: Connect pin 9 or 12 to pin 12 of DM5450N or DM5453N. Connect pin 10 or 11 to pin 11 of DM5450N or DM5453N.

DM5460N (SN5460N)
Dual 4-Input Expander



DM5486N (SN5486N)
Quad Exclusive-OR Gate

Gates, Series 54/74

DM7400 (SN7400) quadruple two-input NAND gate
DM7410 (SN7410) triple three-input NAND gate
DM7420 (SN7420) dual four-input NAND gate

general description

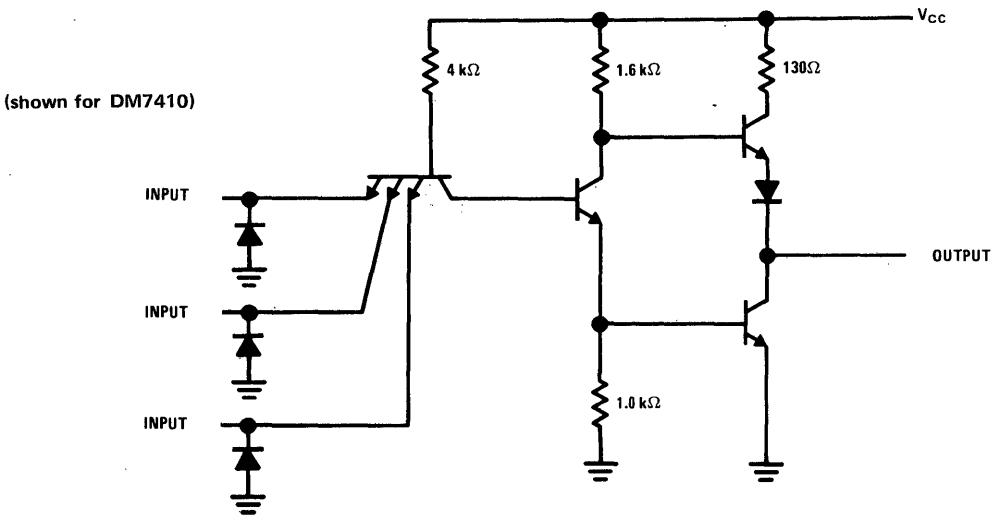
Employing TTL (Transistor-Transistor-Logic) to achieve high speed at moderate power dissipation, these gates provide the basic functions used in the implementation of digital integrated circuit systems. Characteristics of the circuits include high noise immunity, low output impedance, good capacitive drive capability, and minimal variation in switching times with temperature. The gates are compatible with and interchangeable with Series 74 equivalent.

Key features include:

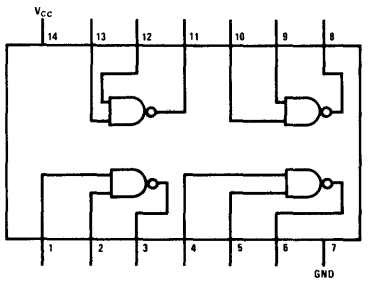
- Typical Noise Immunity 1V
- Guaranteed Noise Immunity 400 mV
- Fan Out 10
- Allowable Power Supply Variation 4.75V to 5.25V
- Average Propagation Delay 13 ns
- Average Power Dissipation 10 mW per gate

schematic and connection diagrams

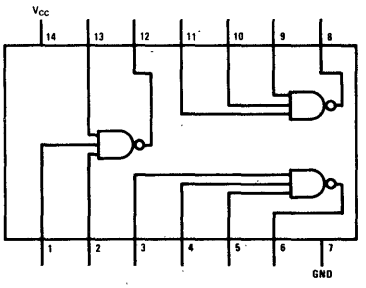
(shown for DM7410)



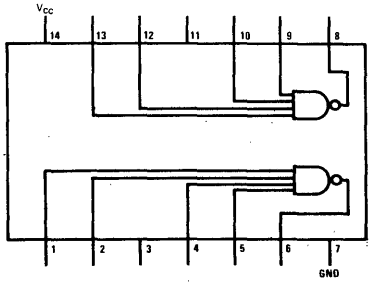
DM7400



DM7410



DM7420



absolute maximum ratings

Vcc	7.0V
Input Voltage	5.5V
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Fan-Out	10
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Diode Clamp Voltage	V_{CC} = 5.0V, T_A = 25°C, I_{IN} = −12 mA			−1.5	V
Logical "1" Input Voltage	V_{CC} = 4.75V	2.0			V
Logical "0" Input Voltage	V_{CC} = 4.75V			0.8	V
Logical "1" Output Voltage	V_{CC} = 4.75V V_{IN} = 0.8V, I_{OUT} = −400μA	2.4			V
Logical "0" Output Voltage	V_{CC} = 4.75V V_{IN} = 2.0V, I_{OUT} = 16 mA			0.4	V
Logical "1" Input Current	V_{CC} = 5.25V V_{IN} = 2.4V			40	μA
Logical "1" Input Current	V_{CC} = 5.25V V_{IN} = 5.5V			1	mA
Logical "0" Input Current	V_{CC} = 5.25V V_{IN} = 0.4V			−1.6	mA
Output Short Circuit Current (Note 2)	V_{CC} = 5.25V V_{IN} = 0V	−18		−55	mA
Supply Current— Logical "0" (Note 3)	V_{CC} = 5.25V V_{IN} = 5.0V		3	5.1	mA
Supply Current— Logical "1" (Note 3)	V_{CC} = 5.25V V_{IN} = 0V		1	1.8	mA
Propagation Delay Time to Logical "0", t_{pd0}	V_{CC} = 5.0V, T_A = 25°C, C = 50 pF		8	15	ns
Propagation Delay Time to Logical "1", t_{pd1}	V_{CC} = 5.0V, T_A = 25°C, C = 50 pF		13	25	ns

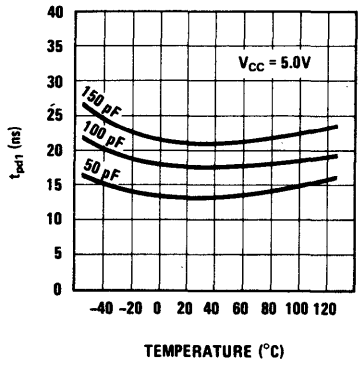
Note 1: Min/max limits apply across the guaranteed temperature range 0°C to 70°C unless otherwise specified. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

Note 2: Not more than 1 output should be shorted at a time.

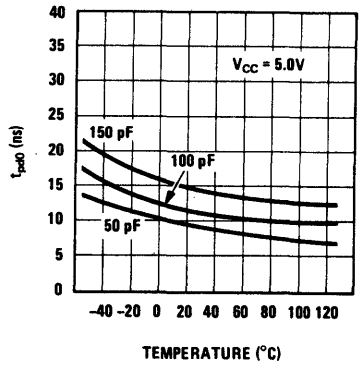
Note 3: Each gate.

typical performance characteristics

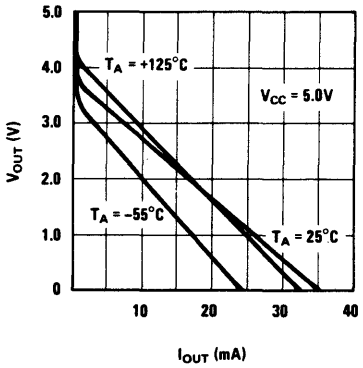
Transition Time to a Logical "1" (t_{pd1}) vs Temperature



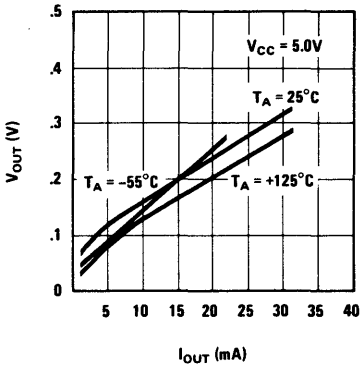
Transition Time to a Logical "0" (t_{pd0}) vs Temperature



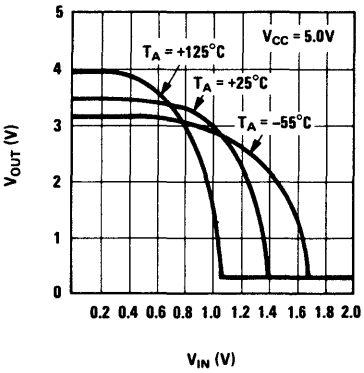
Logical "1" Output Voltage vs Source Current



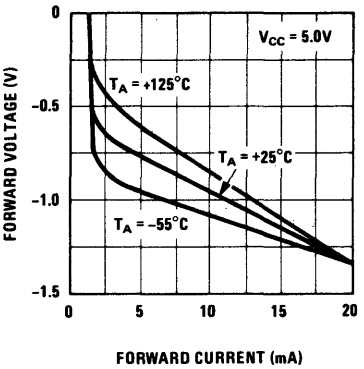
Logical "0" Output Voltage vs Sink Current



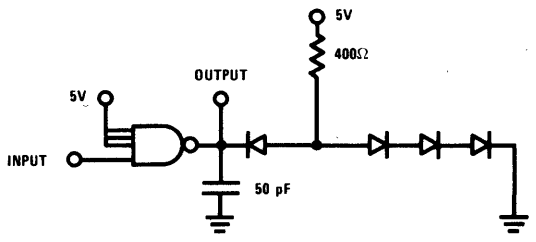
V_{IN} vs V_{OUT}



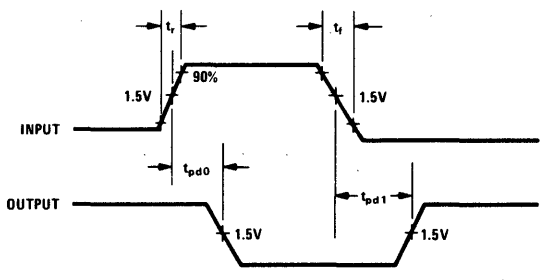
Input Clamp Diode Characteristics



ac test circuit



switching time waveform



$t_r = t_f = 10\ \mu s$
pw = 100 ns
frequency = 1 MHz
V_{CC} = 5.0V

Gates, Series 54/74

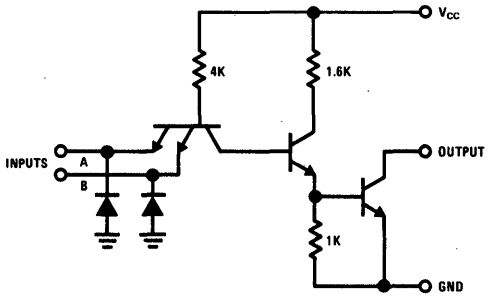
DM5401/DM7401 (SN5401/SN7401) quad two-input gate (open collector)
DM5403/DM7403 (SN5403/SN7403) quad two-input gate (open collector)
DM5405/DM7405 (SN5405/SN7405) hex inverter (open collector)

general description

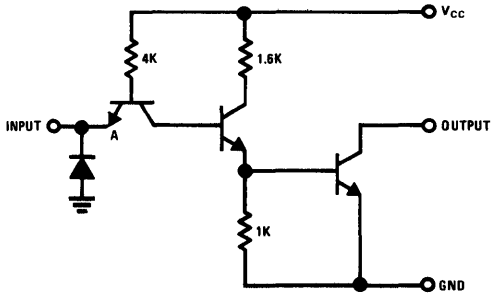
These Series 54/74 functions are designed for applications where the normal TTL "totem-pole" output configuration is not wanted. Such applications include implementation of the Wire-OR function.

Aside from the output, the circuitry is identical to the standard quad two-input gate (DM5400/DM7400) and hex inverter (DM5404/DM7404).

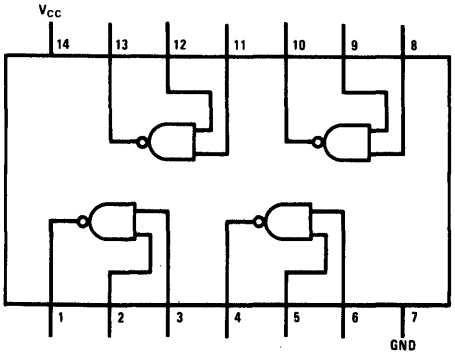
schematic and connection diagrams



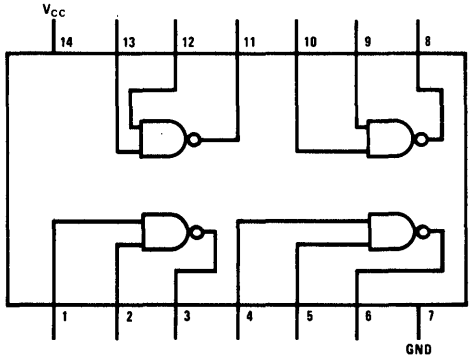
DM5401/DM7401
DM5403/DM7403



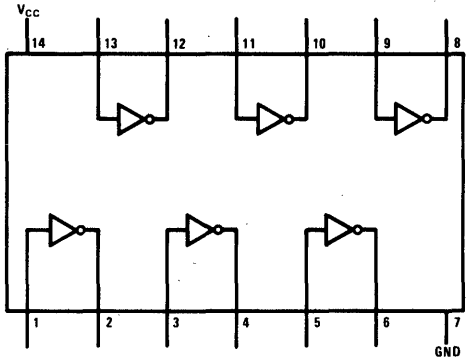
DM5405/DM7405



DM5401/DM7401



DM5403/DM7403



DM5405/DM7405

absolute maximum ratings

V_{CC}		7V
Input Voltage		5.5V
Operating Temperature Range	DM5401, DM5403, DM5405	−55°C to +125°C
	DM7401, DM7403, DM7405	0°C to 70°C
Storage Temperature Range		−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)		300°C

electrical characteristics (Note 1)

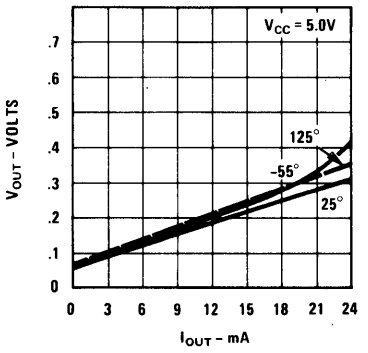
PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
Input Diode Clamp Voltage		V_{CC} = 5.0V, T_A = 25°C, I_{IN} = −12 mA			−1.5	V
Logical "1" Input Voltage	DM5401,3,5 / DM7401,3,5	V_{CC} = 4.5V / V_{CC} = 4.75V	2.0			V
Logical "0" Input Voltage	DM5401,3,5 / DM7401,3,5	V_{CC} = 4.5V / V_{CC} = 4.75V			0.8	V
Logical "1" Output Current	DM5401,3,5 / DM7401,3,5	V_{CC} = 5.5V / V_{CC} = 5.25V, V_{IN} = 0.8V			250	μA
		V_{OUT} = 5.5V, V_{IN} = 0.0V			40	μA
Logical "0" Output Voltage	DM5401,3,5 / DM7401,3,5	V_{CC} = 4.5V / V_{CC} = 4.75V, V_{IN} = 2.0V, I_{OUT} = 16 mA			0.4	V
Logical "1" Input Current	DM5401,3,5 / DM7401,3,5	V_{CC} = 5.5V / V_{CC} = 5.25V, V_{IN} = 2.4V			40	μA
Logical "1" Input Current	DM5401,3,5 / DM7401,3,5	V_{CC} = 5.5V / V_{CC} = 5.25V, V_{IN} = 5.5V			1	mA
Logical "0" Input Current	DM5401,3,5 / DM7401,3,5	V_{CC} = 5.5V / V_{CC} = 5.25V, V_{IN} = 0.4V			−1.6	mA
Supply Current—Logical "0" (Each Gate)	DM5401,3,5 / DM7401,3,5	V_{CC} = 5.5V / V_{CC} = 5.25V, V_{IN} = 5.0V		3.0	5.1	mA
Supply Current—Logical "1" (Each Gate)	DM5401,3,5 / DM7401,3,5	V_{CC} = 5.5V / V_{CC} = 5.25V, V_{IN} = 0V		1.0	1.8	mA
Propagation Delay Time to a Logical "0", t_{pd0}		V_{CC} = 5.0V, T_A = 25°C, C_{OUT} = 15 pF, R_L = 390Ω (Note 2)	3	7.5	15	ns
Propagation Delay Time to a Logical "1", t_{pd1}		V_{CC} = 5.0V, T_A = 25°C, C_{OUT} = 15 pF, R_L = 3.9 kΩ (Note 2)	18	28	45	ns

Note 1: Min/Max units apply across the guaranteed temperature range unless otherwise specified. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

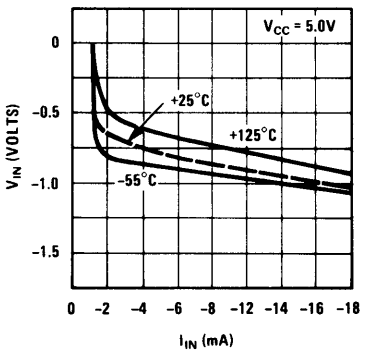
Note 2: C_{OUT} includes device output capacitance of approximately 8.5 pF and wiring capacitance.

typical performance characteristics

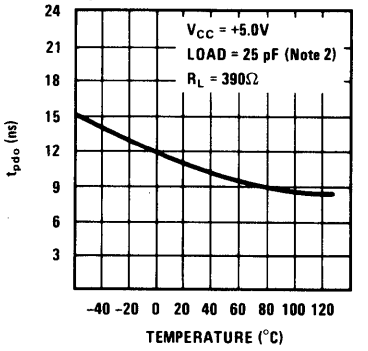
V_{OUT} vs I_{OUT} Logical "0"



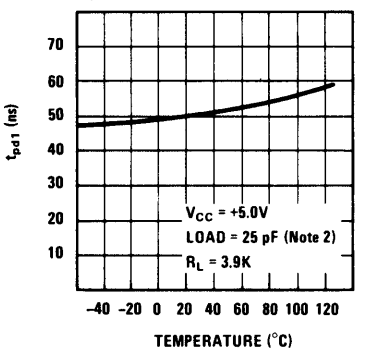
Input Clamp Diode Characteristics



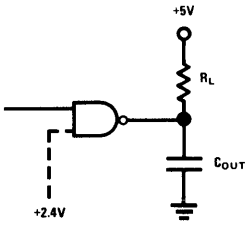
Transition Time to a Logical "0" (t_{pd0}) vs Temperature



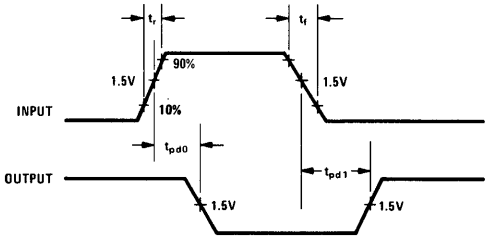
Transition Time to a Logical "1" (t_{pd1}) vs Temperature



ac test circuit



switching time waveform



$t_r = t_f = 10\ \mu s$
pw = 100 ns
frequency = 1 MHz
V_{CC} = 5.0V

Gates, Series 54/74

DM5402/DM7402 (SN5402/SN7402) quad two-input NOR gate

general description

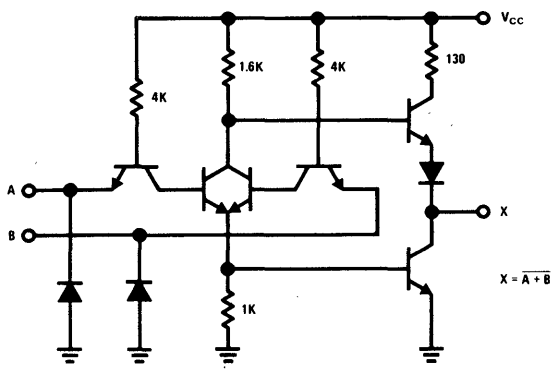
The DM5402/DM7402 is a quad 2-input NOR gate utilizing TTL (Transistor-Transistor Logic) to achieve high speed at nominal power dissipation. It is completely compatible with other Series 54/74 devices.

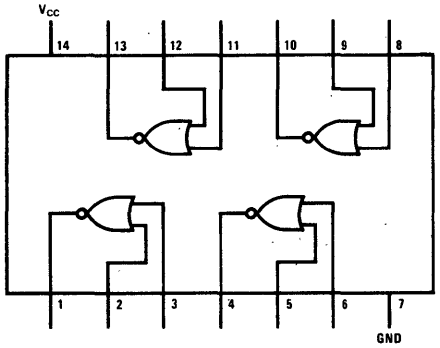
Features include:

- Input Clamping Diodes
- Typical Noise Immunity 1V
- Guaranteed Noise Immunity 400 mV
- Fan-out 10
- Allowable Power Supply Variation
  - DM5402 4.5V to 5.5V
  - DM7402 4.75V to 5.25V
- Average Propagation Delay 12 ns (with 50 pF)
- Average Power Dissipation 14 mW per gate

schematic and connection diagrams

DM5402/DM7402 (each gate)





absolute maximum ratings

V_{CC}	7V
Input Voltage	5.5V
Operating Temperature Range	
DM7402	0°C to 70°C
DM5402	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics (Note 1)

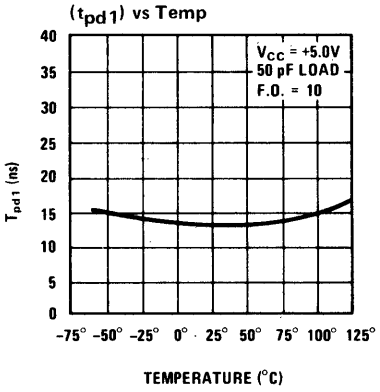
PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
Input Diode Clamp Voltage		V_{CC} = 5.0V T_A = 25°C, I_{IN} = −12 mA		−1.0	−1.5	V
Logical "1" Input Voltage	DM5402 / DM7402	V_{CC} = 4.5V / V_{CC} = 4.75V	2.0			V
Logical "0" Input Voltage	DM5402 / DM7402	V_{CC} = 4.5V / V_{CC} = 4.75V			0.8	V
Logical "1" Output Voltage	DM5402 / DM7402	V_{CC} = 4.5V / V_{CC} = 4.75V, V_{IN} = 0.8V, I_{OUT} = −400μA	2.4			V
Logical "0" Output Voltage	DM5402 / DM7402	V_{CC} = 4.5V / V_{CC} = 4.75V, V_{IN} = 2.0V, I_{OUT} = 16 mA			0.4	V
Logical "1" Input Current	DM5402 / DM7402	V_{CC} = 5.5V / V_{CC} = 5.25V, V_{IN} = 2.4V			40	μA
Logical "1" Input Current	DM5402 / DM7402	V_{CC} = 5.5V / V_{CC} = 5.25V, V_{IN} = 5.5V			1	mA
Logical "0" Input Current	DM5402 / DM7402	V_{CC} = 5.5V / V_{CC} = 5.25V, V_{IN} = 0.4V		−1.0	−1.6	mA
Output Short Circuit Current (Note 2)	DM5402 / DM7402	V_{CC} = 5.5V / V_{CC} = 5.25V, V_{OUT} = 0	−20 / −18	−32	−55	mA
Supply Current-Logical "0" (each gate)	DM5402 / DM7402	V_{CC} = 5.5V / V_{CC} = 5.25V, V_{IN} = 5.0V		3.6	6.3	mA
Supply Current-Logical "1" (each gate)	DM5402 / DM7402	V_{CC} = 5.5V / V_{CC} = 5.25V, V_{IN} = 0V		2.0	3.6	mA
Propagation Delay to a Logical "0", t_{pd0}		V_{CC} = 5.0V T_A = 25°C N = 10, C = 50 pF	3	9	15	ns
Propagation Delay to a Logical "1", t_{pd1}		V_{CC} = 5.0V T_A = 25°C N = 10, C = 50 pF	5	13	22	ns

Note 1: Min/max limits apply across the guaranteed temperature range of 0°C to 70°C for the DM7402 and −55°C to +125°C for the DM5402 unless otherwise specified. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

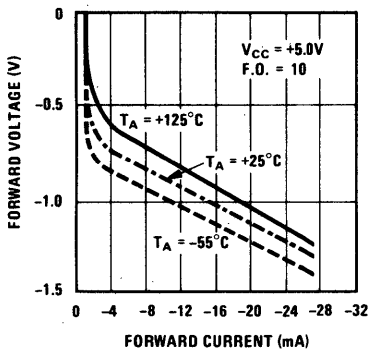
Note 2: Only one output at a time should be short circuited.

typical performance characteristics

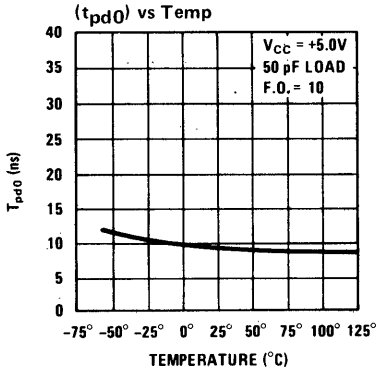
Transition Time to Logical "1" (t_{pd1}) vs Temp



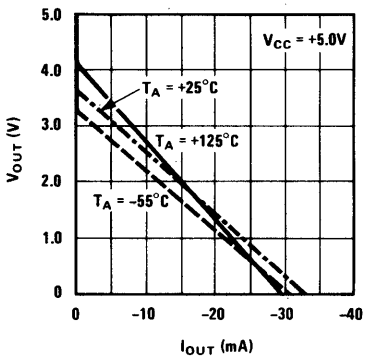
Input Clamp Diode Characteristics



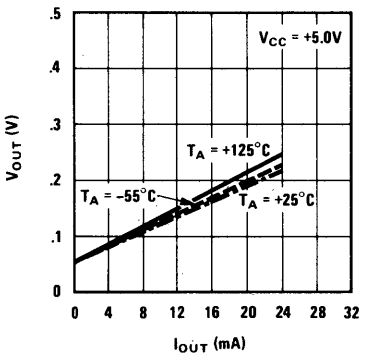
Transition Time to Logical "0" (t_{pd0}) vs Temp



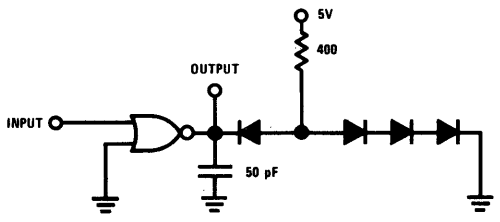
Logical "1" Output Voltage vs Source Current



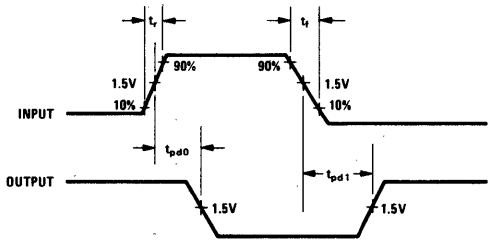
Logical "0" Output Voltage vs Sink Current



ac test circuit



switching time waveform



$t_r = t_f$ = 10 ns
pw = 100 ns
frequency = 1 MHz
V_{CC} = 5.0V

Gates, Series 54/74

DM5404/DM7404 (SN5404/SN7404) hex inverter

general description

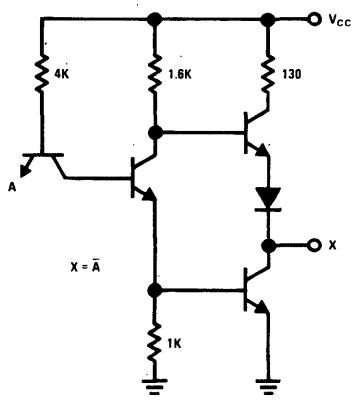
The DM5404/DM7404 is a hex inverter utilizing TTL to achieve high speed at nominal power dissipation. It is totally compatible with other Series 54/74 devices.

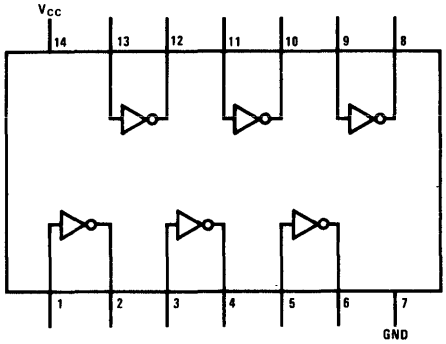
Features include:

- Input clamping diodes
- Typical Noise Immunity 1V
- Guaranteed Noise Immunity 400 mV
- Fan-out 10
- Allowable Power Supply Variation
  - DM5404 4.5V to 5.5V
  - DM7404 4.75V to 5.25V
- Average Propagation Delay 12 ns (with 50 pF)
- Average Power Dissipation 10 mW per gate

schematic and connection diagrams

DM5404/DM7404





absolute maximum ratings

V_{CC}	7V
Input Voltage	5.5V
Operating Temperature Range	
DM7404	0°C to 70°C
DM5404	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (soldering, 10 sec)	300°C

electrical characteristics (Note 1)

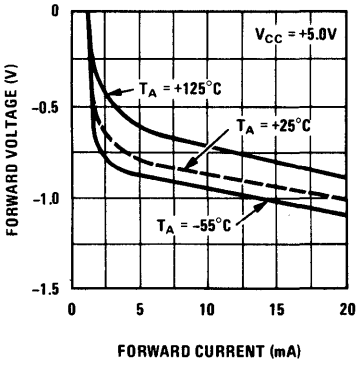
PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
Input diode clamp voltage		V_{CC} = 5.0V, I_{IN} = −12 mA	T_A = 25°C			−1.5	V
Logical "1" Input Voltage	DM5404	V_{CC} = 4.5V		2.0			V
	DM7404	V_{CC} = 4.75V					
Logical "0" Input Voltage	DM5404	V_{CC} = 4.5V				0.8	V
	DM7404	V_{CC} = 4.75V					
Logical "1" Output Voltage	DM5404	V_{CC} = 4.5V	V_{IN} = 0.8V, I_{OUT} = −400 μA	2.4			V
	DM7404	V_{CC} = 4.75V					
Logical "0" Output Voltage	DM5404	V_{CC} = 4.5V	V_{IN} = 2.0V, I_{OUT} = 16 mA			0.4	V
	DM7404	V_{CC} = 4.75V					
Logical "1" Input Current	DM5404	V_{CC} = 5.5V	V_{IN} = 2.4V			40	μA
	DM7404	V_{CC} = 5.25V					
Logical "1" Input Current	DM5404	V_{CC} = 5.5V	V_{IN} = 5.5V			1	mA
	DM7404	V_{CC} = 5.25V					
Logical "0" Input Current	DM5404	V_{CC} = 5.5V	V_{IN} = 0.4V		−1.0	−1.6	mA
	DM7404	V_{CC} = 5.25V					
Output Short Circuit Current (Note 2)	DM5404	V_{CC} = 5.5V	V_{OUT} = 0	−20	−30	−55	mA
	DM7404	V_{CC} = 5.25V		−18			
Supply Current - Logical "0" (each gate)	DM5404	V_{CC} = 5.5V	V_{IN} = 5.0V		3.0	5.1	mA
	DM7404	V_{CC} = 5.25V					
Supply Current - Logical "1" (each gate)	DM5404	V_{CC} = 5.5V	V_{IN} = 0		1.0	1.8	mA
	DM7404	V_{CC} = 5.25V					
Propagation Delay to a Logical "1", t_{pd1}		T_A = 25°C, N = 10	V_{CC} = 5.0V, C = 50 pF	5	16	22	ns
Propagation Delay to a Logical "0" t_{pd0}		T_A = 25°C, N = 10	V_{CC} = 5.0V, C = 50 pF	3	9	15	ns

Note 1. Min/Max limits apply across the guaranteed temperature range of 0°C to 70°C for the DM7404, and −55°C to +125°C for the DM5404, unless otherwise specified. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

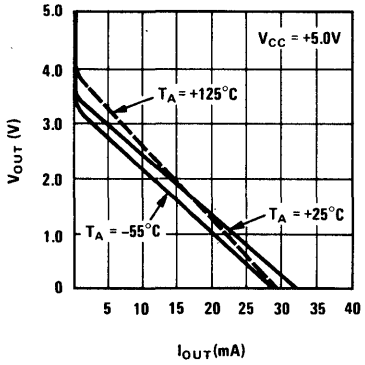
Note 2. Only one output at a time should be short circuited.

typical performance characteristics

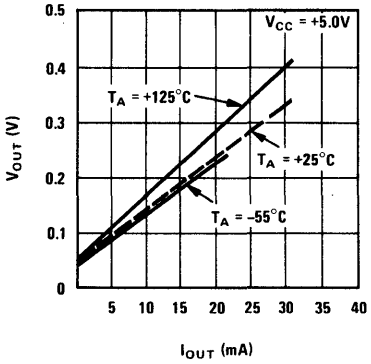
Input Clamp Diode Characteristics



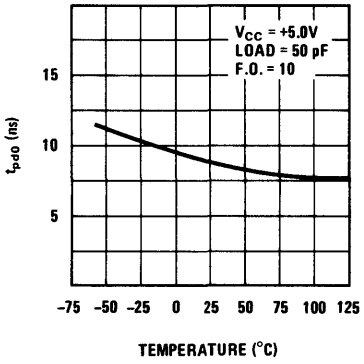
Logical "1" Output Voltage vs Source Current



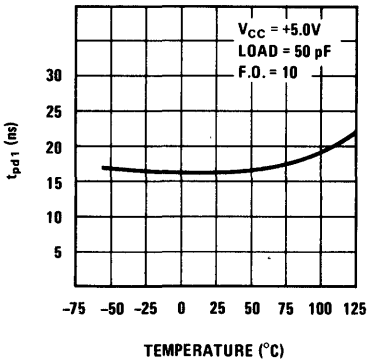
Logical "0" Output Voltage vs Sink Current



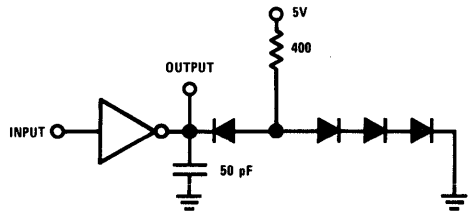
Transition Time to a Logical "0", t_{pd0} vs Temperature



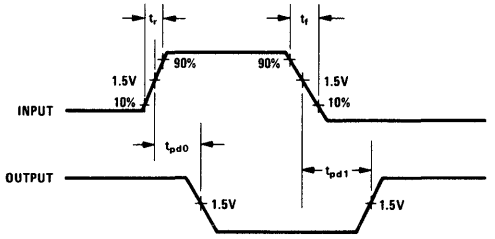
Transition Time to a Logical "1", t_{pd1} vs Temperature



ac test circuit



switching time waveform



$t_r = t_f$ = 10 ns
pw = 100 ns
frequency = 1 MHz
V_{CC} = 5.0V

Gates, Series 54/74

DM7430 (SN7430) eight-input gate

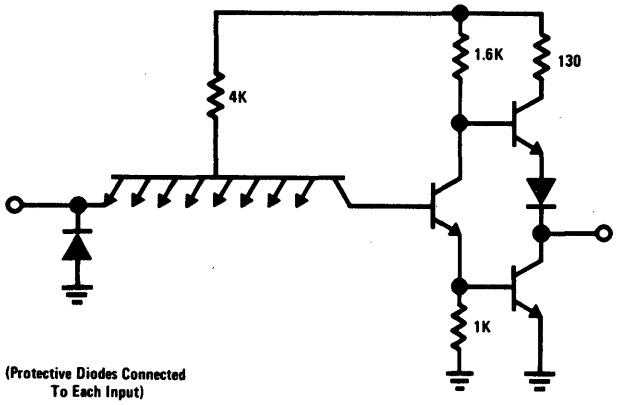
general description

Employing TTL (Transistor-Transistor Logic) to achieve high speed at moderate power dissipation, the DM7430 provides the basic functions used in the implementation of digital integrated circuit systems. Characteristics of the circuit includes high noise immunity, low output impedance, good capacitive drive capability, and minimal variation in switching times with temperature. The DM7430 is compatible and interchangeable with Series 74.

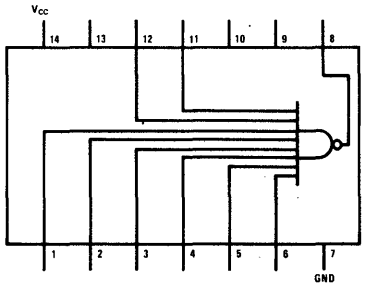
Key features include:

- Typical Noise Immunity 1V
- Guaranteed Noise Immunity 400 mV
- Fan Out 10
- Allowable Power Supply Variation 4.75V to 5.25V
- Average Propagation Delay 13 ns
- Average Power Dissipation 10 mW per gate

schematic and connection diagrams



(Protective Diodes Connected To Each Input)



absolute maximum ratings

V_{CC}	7V
Input Voltage	5.5V
Operating Temperature Range	0°C to 70°C
Storage Temperature Range	−65°C to +150°C
Fan-Out	10
Lead Temperature (Soldering, 10 sec.)	300°C

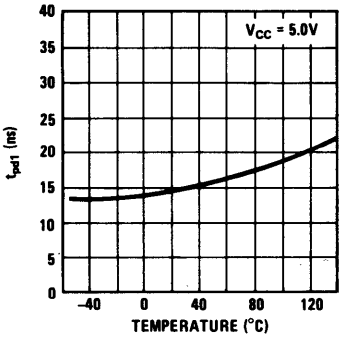
electrical characteristics (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Diode Clamp Voltage	V_{CC} = 5.0V, T_A = 25°C, I_{IN} = −12 mA			−1.5	V
Logical "1" Input Voltage	V_{CC} = 4.75V	2.0			V
Logical "0" Input Voltage	V_{CC} = 4.75V			0.8	V
Logical "1" Output Voltage	V_{CC} = 4.75V, V_{IN} = 0.8V, I_{OUT} = −400 μA	2.4			V
Logical "0" Output Voltage	V_{CC} = 4.75V, V_{IN} = 2.0V, I_{OUT} = 16 mA			0.4	V
Logical "1" Input Current	V_{CC} = 5.25V, V_{IN} = 2.4V			40	μA
Logical "1" Input Current	V_{CC} = 5.25V, V_{IN} = 5.5V			1	mA
Logical "0" Input Current	V_{CC} = 5.25V, V_{IN} = 0.4V			1.6	mA
Output Short Circuit Current	V_{CC} = 5.25V, V_{IN} = 0V	−18		−55	mA
Supply Current—Logical "0"	V_{CC} = 5.25V, V_{IN} = 5.0V			5.1	mA
Supply Current—Logical "1"	V_{CC} = 5.25V, V_{IN} = 0V			1.8	mA
Propagation Delay Time to a Logical "0", t_{pd0}	V_{CC} = 5.0V, T_A = 25°C, C = 50 pF			15	ns
Propagation Delay Time to a Logical "1", t_{pd1}	V_{CC} = 5.0V, T_A = 25°C, C = 50 pF			29	ns

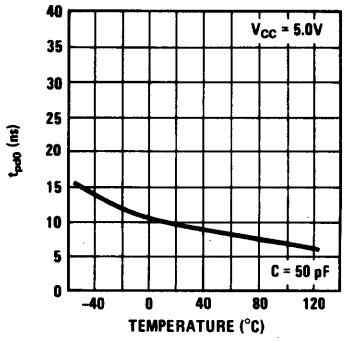
Note 1: Min/max units apply across the guaranteed temperature range of 0°C to 70°C unless otherwise specified. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

typical performance characteristics

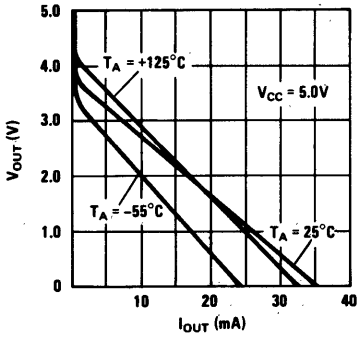
Transition Time to a Logical "1" (t_{pd}) vs Temperature



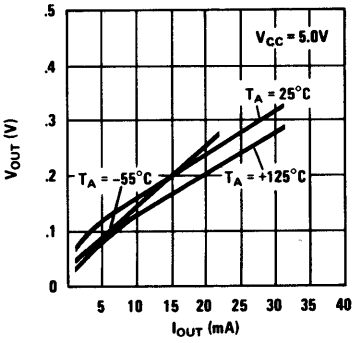
Transition Time to a Logical "0" (t_{pd0}) vs Temperature



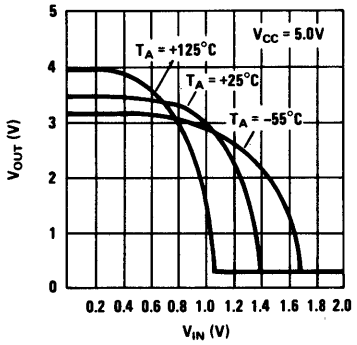
Logical "1" Output Voltage vs Source Current



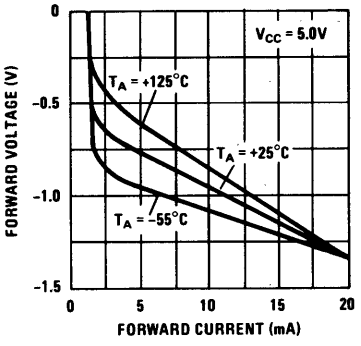
Logical "0" Output Voltage vs Sink Current



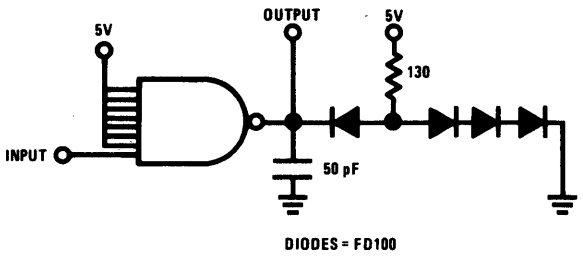
V_{in} vs V_{out}



Input Clamp Diode Characteristics

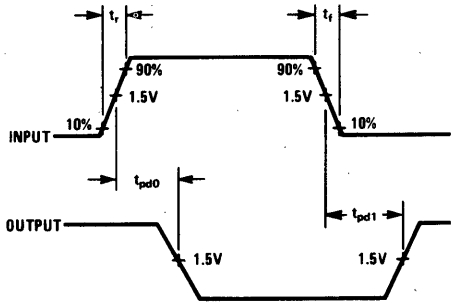


ac test circuit



DIODES = FD100

switching time waveform



$t_r = t_f$ = 10 ns
pw = 100 ns
frequency = 1 MHz
V_{CC} = 5.0V

Gates, Series 54/74

DM7440 (SN7440) dual four input buffer

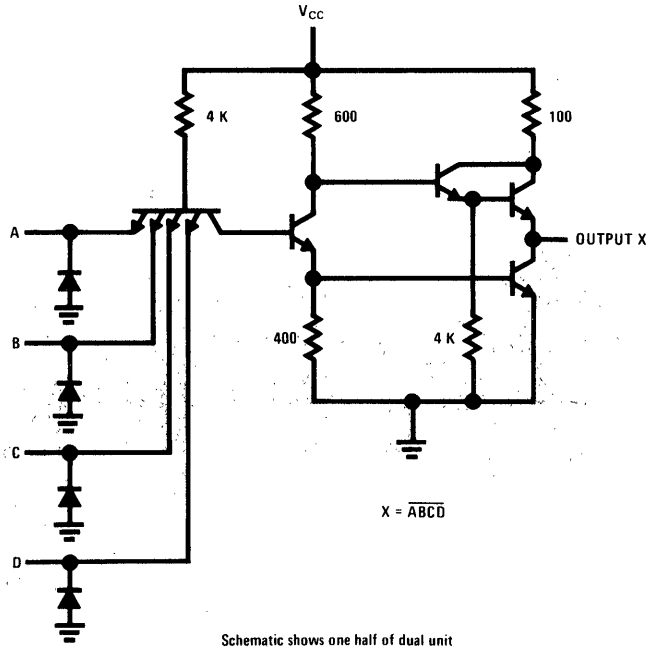
general description

Employing TTL (Transistor-Transistor-Logic) the DM7440 buffer is used when high fan-out is desirable. In addition to driving a large number of TTL inputs, this buffer can be used to drive lines between equipments, to operate small relays and lamps (50 mA), and to act as a clock driver for synchronous logic systems. It is completely compatible with other Series 74 devices.

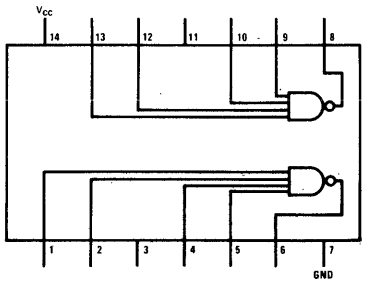
Key features include:

- Typical Noise Immunity 1V
- Guaranteed Noise Immunity 400 mV
- Fan Out 30
- Diode Clamps on Inputs

schematic and connection diagrams



Schematic shows one half of dual unit



absolute maximum ratings

V_{CC}	7.0V
Input Voltage	5.5V
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Fan-Out	30
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics (Note 1)

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Diode Clamp Voltage	V_{CC} = 5.0V, T_A = 25°C, I_{IN} = −12 mA		−1.0	−1.5	V
Logical "1" Input Voltage	V_{CC} = 4.75V	2.0			V
Logical "0" Input Voltage	V_{CC} = 4.75V			0.8	V
Logical "1" Output Voltage	V_{CC} = 4.75V, V_{IN} = 0.8V, I_{OUT} = −1.2 mA	2.4			V
Logical "0" Output Voltage	V_{CC} = 4.75V, V_{IN} = 2.0V, I_{OUT} = 48 mA			0.4	V
Logical "1" Input Current	V_{CC} = 5.25V, V_{IN} = 2.4V			40	μA
Logical "1" Input Current	V_{CC} = 5.25V, V_{IN} = 5.5V			1.0	mA
Logical "0" Input Current	V_{CC} = 5.25V, V_{IN} = 0.4V			−1.6	mA
Output Short Circuit Current (Note 2)	V_{CC} = 5.25V, V_{IN} = 0V	−24.0	−55	−70.0	mA
Supply Current — Logical "0" (Note 3)	V_{CC} = 5.25V, V_{IN} = 5.0V, 25°C		8.6	11.4	mA
Supply Current — Logical "1" (Note 3)	V_{CC} = 5.25V, V_{IN} = 0V, 25°C		2.0	3.6	mA
Propagation Delay Time to Logical "0", t_{pd0}	V_{CC} = 5.0V, T_A = 25°C, C = 50 pF F.O. = 30		10	15	ns
Propagation Delay Time to Logical "1", t_{pd1}	V_{CC} = 5.0V, T_A = 25°C, C = 50 pF F.O. = 30		8	25	ns

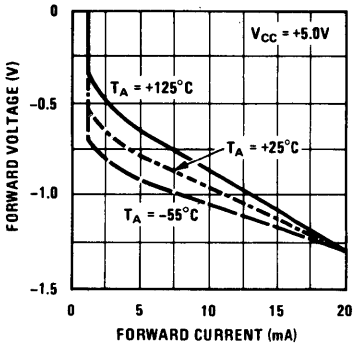
Note 1: Unless otherwise specified, min/max limits apply across the guaranteed temperature range of 0°C to 70°C. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

Note 2: Not more than 1 output should be shorted at a time.

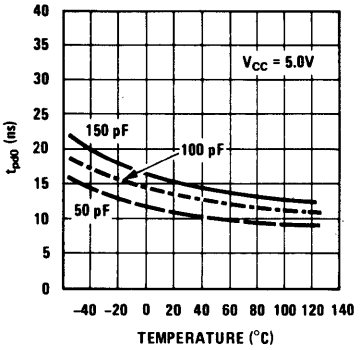
Note 3: Each gate.

typical performance characteristics

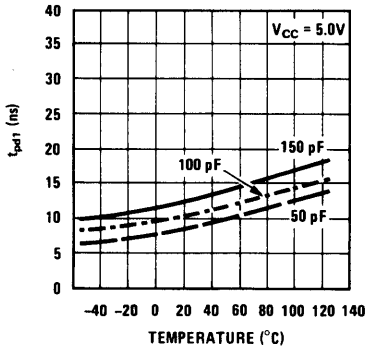
Input Clamp Diode Characteristics



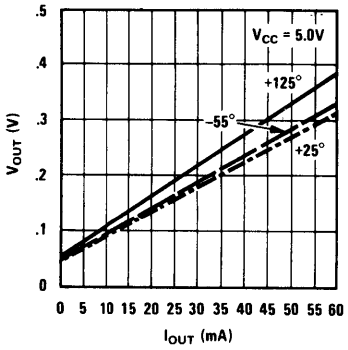
Transition Time to a Logical "0" (t_{pd0}) vs Temperature



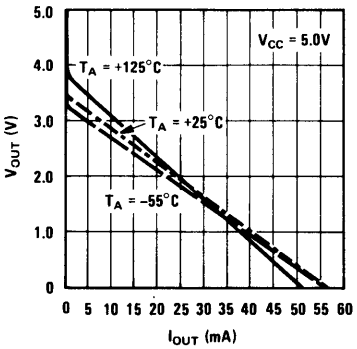
Transition Time to a Logical "1" (t_{pd1}) vs Temperature



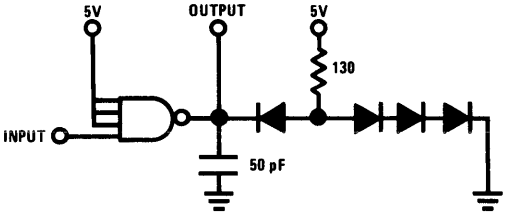
Logical "0" Output Voltage vs Sink Current



Logical "1" Output Voltage vs Source Current

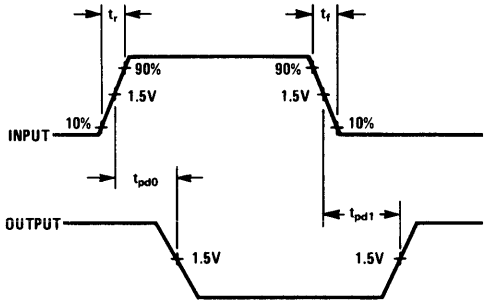


ac test circuit



DIODES = FD100

switching time waveform



$t_r = t_f = 10$ ns
pw = 100 ns
frequency = 1 MHz
V_{CC} = 5.0V

Gates, Series 54/74

DM7450 (SN7450) expandable dual 2-wide 2-input AND-OR-INVERT gate
DM7451 (SN7451) dual 2-wide 2-input AND-OR-INVERT gate
DM7453 (SN7453) expandable 4-wide 2-input AND-OR-INVERT gate
DM7454 (SN7454) 4-wide 2-input AND-OR-INVERT gate
DM7460 (SN7460) dual 4-input expander

general description

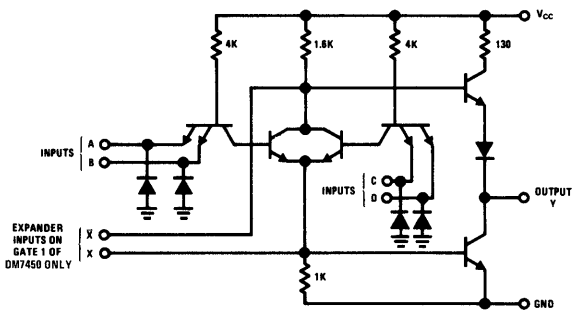
The devices described in this data sheet employ TTL to achieve high speed at moderate power dissipation. They are consolidated onto one sheet since they perform the AND-OR-INVERT function with only differing numbers of AND inputs and OR terms. Characteristics include high noise immunity, low output impedance, good capacitance drive capability, and minimal variation in switching time with temperature. The gates are compatible with and interchangeable with Series 74 devices.

Key features include:

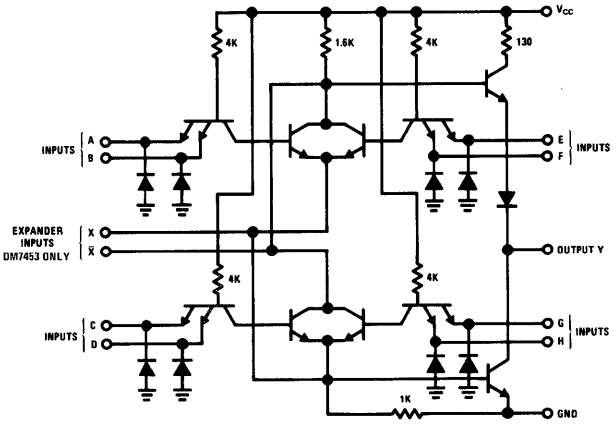
- Input Clamping Diodes
- Typical Noise Immunity 1 Volt
- Guaranteed Noise Immunity 400 mV
- Fan-out 10
- Allowable Power Supply Variation 4.75V to 5.25V
- Average Propagation Delay 13 ns
- Average Power Dissipation 14 mW/ gate

schematic diagrams

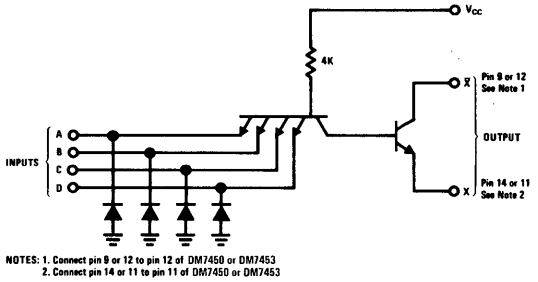
DM7450, DM7451 (each gate)



DM7453, DM7454



DM7460 (each gate)



NOTES: 1. Connect pin 9 or 12 to pin 12 of DM7450 or DM7453
2. Connect pin 14 or 11 to pin 11 of DM7450 or DM7453

absolute maximum ratings

V_{CC}	7V
Input Voltage	5.5V
Operating Temperature Range	0°C to 70°C
Storage Temperature Range	−65°C to +150°C
Fan-Out	10
Lead Temperature (Soldering, 10 sec.)	300°C

electrical characteristics (Notes 1, 3) (DM7450, DM7451, DM7453, DM7454)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Diode Clamp Voltage	V_{CC} = 5.0V, T_A = 25°C I_{IN} = −12 mA			−1.5	V
Logical "1" Input Voltage	V_{CC} = 4.75V	2.0			V
Logical "0" Input Voltage	V_{CC} = 4.75V			0.8	V
Logical "1" Output Voltage	V_{CC} = 4.75V, V_{IN} = 0.8V I_{OUT} = −400 μA	2.4			V
Logical "0" Output Voltage	V_{CC} = 4.75V, V_{IN} = 2.0V I_{OUT} = 16 mA			0.4	V
Logical "1" Input Current	V_{CC} = 5.25V, V_{IN} = 2.4V			40	μA
Logical "1" Input Current	V_{CC} = 5.25V, V_{IN} = 5.5V			1	mA
Logical "0" Input Current	V_{CC} = 5.25V, V_{IN} = 0.4V			−1.6	mA
Output Short Circuit Current (Note 2)	V_{CC} = 5.25V, V_{IN} = 0V	−18		−55	mA
Supply Current — Logical "0" (Each Gate)	V_{CC} = 5.25V, V_{IN} = 5.0V		3.7	6.5	mA
Supply Current — Logical "1" (Each Gate)	V_{CC} = 5.25V, V_{IN} = 0V		2.0	3.6	mA
Propagation Delay Time to a Logical "0", t_{pd0}	V_{CC} = 5.0V, T_A = 25°C C = 50 pF, N = 10			15	ns
Propagation Delay Time to a Logical "1", t_{pd1}	V_{CC} = 5.0V, T_A = 25°C C = 50 pF, N = 10			25	ns
Propagation Delay Time to Logical "0" Level (through DM7450 or DM7453)	V_{CC} = 5.0V, T_A = 25°C C = 50 pF, N = 10			20	ns
Propagation Delay Time to Logical "1" Level (through DM7450 or DM7453)	V_{CC} = 5.0V, T_A = 25°C C = 50 pF, N = 10			34	ns

Note 1: Min/Max units apply across the guaranteed temperature range of 0°C to 70°C unless otherwise specified. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

Note 2: Not more than 1 output should be shorted at a time.

Note 3: Measurements made with expandable inputs open.

electrical characteristics (Note 1) (DM7460)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Input Diode Clamp Voltage	V_{CC} = 5.0V I_{IN} = −12 mA	T_A = 25°C			−1.5	V
Logical "1" Input Voltage	V_{CC} = 4.75V, $R_{V_{CC}\text{ to COLLECTOR}}$ = 1.1 kΩ,	$V_{EMITTER}$ = 1V, T_A = 0°C	2			V
Logical "0" Input Voltage	V_{CC} = 4.75V, $R_{EMITTER\text{ to GRD}}$ = 1.2 kΩ, T_A = 0°C	$V_{COLLECTOR}$ = 4.5V, $I_{COLLECTOR}$ = 0.27 mA,			0.8	V
Logical "0" Output Voltage (With Respect to Emitter)	V_{CC} = 4.75V, $V_{EMITTER}$ = 1V, T_A = 0°C	V_{IN} = 2V, $R_{V_{CC}\text{ to COLLECTOR}}$ = 1.1 kΩ,			0.4	V
Logical "1" Output Current	V_{CC} = 4.75V, $V_{COLLECTOR}$ = 4.5V, T_A = 0°C	V_{IN} = 0.8V, $R_{EMITTER\text{ to GRD}}$ = 1.2 kΩ,			270	μA
Logical "0" Output Current	V_{CC} = 4.75V, $V_{EMITTER}$ = 1V	V_{IN} = 2V,	−0.43			mA
Logical "0" Input Current	V_{CC} = 5.25V,	V_{IN} = 0.4V			−1.6	mA
Logical "1" Input Current	V_{CC} = 5.25V, V_{CC} = 5.25V,	V_{IN} = 2.4V V_{IN} = 5.5V			40 1	μA mA
Logical "0" Supply Current (Each Gate)	V_{CC} = 5V, $V_{EMITTER}$ = 0.85V	V_{IN} = 5V,		0.6	1.25	mA
Logical "1" Supply Current (Each Gate)	V_{CC} = 5V, $V_{EMITTER}$ = 0.85V	V_{IN} = 0		1.0	1.8	mA

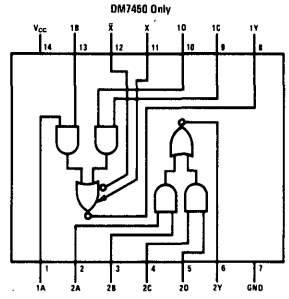
(DM7450, DM7453 only) using expander inputs, T_A = 0°C

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Expander Current	V_{CC} = 4.75V, I_{SINK} = 16 mA	$V_{PIN\ 11\text{ to PIN }12}$ = 0.4V			3.1	mA
Base-Emitter Voltage of Output Transistor (Q)	V_{CC} = 4.75V, $I_{PIN\ 11}$ = 0.62 mA,	I_{SINK} = 16 mA, $R_{PIN\ 11\text{ to PIN }12}$ = 0			1	V
Logical "1" Output Voltage	V_{CC} = 4.75V, $I_{PIN\ 11}$ = 0.27 mA,	I_{LOAD} = −400 μA, $I_{PIN\ 12}$ = −0.27 mA	2.4			V
Logical "0" Output Voltage	V_{CC} = 4.75V, $I_{PIN\ 11}$ = 0.43 mA,	I_{SINK} = 16 mA, $R_{PIN\ 11\text{ to }12}$ = 130Ω			0.4	V

Note 1: Min/Max units apply across the guaranteed temperature range of 0°C to 70°C unless otherwise specified. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

connection diagrams

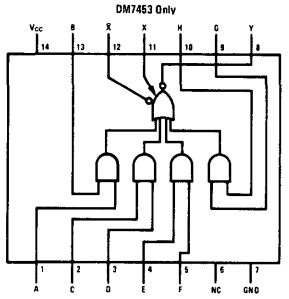
DM7450, DM7451



$Y = \overline{(AB) + (CD) + X}$ X = ABCD from DM7460

NOTES: Expander nodes X and $\overline{X}$ are on the DM7450 only. If not used, leave open. Make no external connection to pins 11 and 12 of the DM7451. A total of four expander gates may be connected to the DM7450 expandable gate.

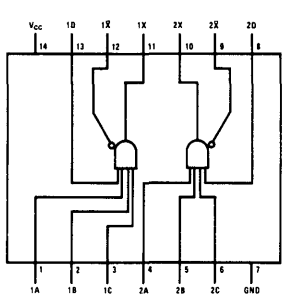
DM7453, DM7454



$Y = \overline{(AB) + (CD) + (EF) + (GH) + X}$ X = ABCD from DM7460

NOTES: Expander nodes X and $\overline{X}$ are on the DM7453 only. If not used, leave open. Make no external connection to pins 11 and 12 of the DM7454. A total of four expander gates may be connected to the DM7453 expandable gate.

DM7460



X = ABCD

NOTE: Connect Pin 9 or 12 to pin 12 of DM7450 or DM7453. Connect Pin 10 or 11 to pin 11 of DM7450 or DM7453.

Gates, Series 54/74

DM5486/DM7486 (SN5486/SN7486) quad exclusive-OR gate

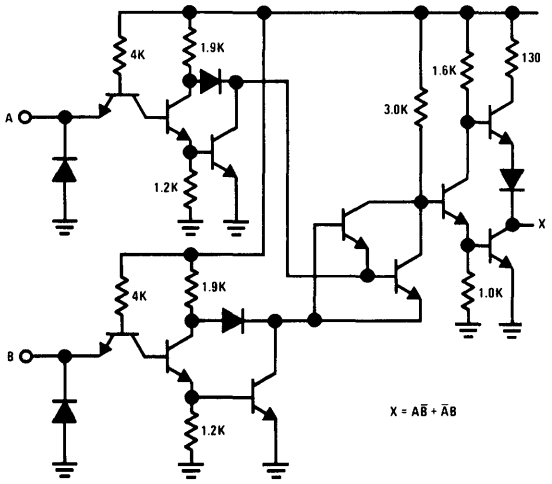
general description

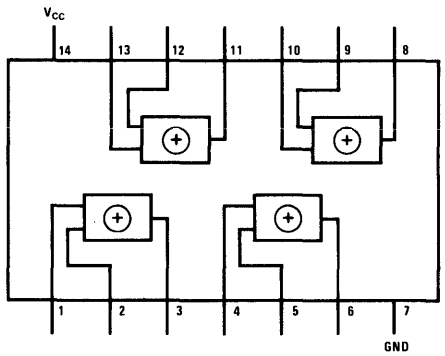
The DM5486/DM7486 utilizes TTL (Transistor-Transistor Logic) to provide four exclusive-OR gates in one package. Characteristics of the circuits include high noise immunity, low output impedance, good capacitive drive capability, and minimal variation in switching times with temperature. The device is completely compatible with other Series 54/74 devices.

Key features include:

- Input clamp diodes
- Typical noise immunity 1V
- Average propagation delay 15 ns
- Average power dissipation 40 mW per gate

schematic and connection diagrams





absolute maximum ratings

V_{CC}	7.0V
Input Voltage	5.5V
Operating Temperature Range DM7486	0°C to 70°C
DM5486	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Fan Out	10
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics (Note 1)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
Input Diode Clamp Voltage		V_{CC} = 5.0V, T_A = 25°C, I_{IN} = −12 mA				−1.5	V
Logical "1" Input Voltage	DM5486	V_{CC} = 4.5V		2.0			V
	DM7486	V_{CC} = 4.75V					
Logical "0" Input Voltage	DM5486	V_{CC} = 4.5V				0.8	V
	DM7486	V_{CC} = 4.75V					
Logical "1" Output Voltage	DM5486	V_{CC} = 4.5V					
	DM7486	V_{CC} = 4.75V, Input Conditions .8V & 2.0V or 2.0V & .8V, I_{OUT} = −400 μA		2.4			V
Logical "0" Output Voltage	DM5486	V_{CC} = 4.5V					
	DM7486	V_{CC} = 4.75V, Input Conditions .8V & .8V or 2.0V & 2.0V, I_{OUT} = 16 mA				0.4	V
Logical "1" Input Current	DM5486	V_{CC} = 5.5V					
	DM7486	V_{CC} = 5.25V, V_{IN} = 2.4V				40	μA
Logical "1" Input Current	DM5486	V_{CC} = 5.5V					
	DM7486	V_{CC} = 5.25V, V_{IN} = 5.5V				1	mA
Logical "0" Input Current	DM5486	V_{CC} = 5.5V					
	DM7486	V_{CC} = 5.25V, V_{IN} = 0.4V				−1.6	mA
Output Short Circuit Current (Note 2)	DM5486	V_{CC} = 5.5V					
	DM7486	V_{CC} = 5.25V, V_{IN} = 0V		−18.0		−55	mA
Supply Current Logical "0" (Each Gate)	DM5486	V_{CC} = 5.5V					
	DM7486	V_{CC} = 5.25V Both Inputs Logical "1" (Worst Case)			9.0	14.2	mA
Supply Current Logical "1" (Each Gate)	DM5486	V_{CC} = 5.5V					
	DM7486	V_{CC} = 5.25V, One Input Logical "1", One Input Logical "0"			7.0	10.5	mA
Propagation Delay Time to Logical "0", t_{pd0} (Note 3)		V_{CC} = 5.0V, T_A = 25°C, F.O. = 10 C_o = 50 pF	Inv.	7	12	20	ns
			Non-Inv.	7	12	20	ns
Propagation Delay Time to Logical "1", t_{pd1} (Note 3)		V_{CC} = 5.0V, T_A = 25°C, F.O. = 10 C_o = 50 pF	Inv.	10	19	30	ns
			Non-Inv.	8	14.5	23	ns

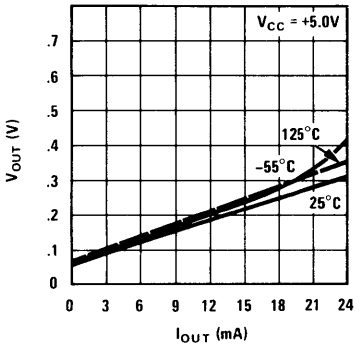
Note 1. Min/max limits apply across the guaranteed temperature range of 0°C to 70°C for the DM7486 and −55°C to +125°C for the DM5486 unless otherwise specified. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

Note 2. Not more than one output should be shorted at a time.

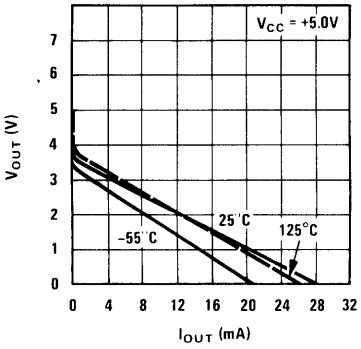
Note 3. For explanation of the inverting and non-inverting specs, see the AC test circuit and AC waveforms.

typical performance characteristics

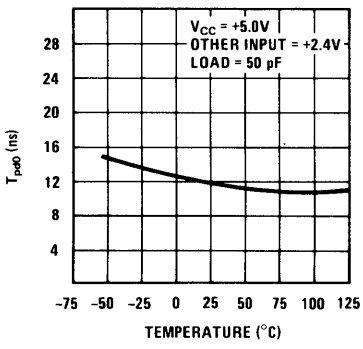
V_{OUT} vs I_{OUT} Logical "0"



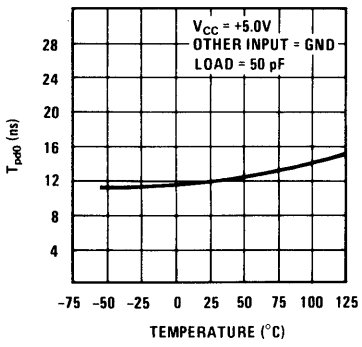
V_{OUT} vs I_{OUT} Logical "1"



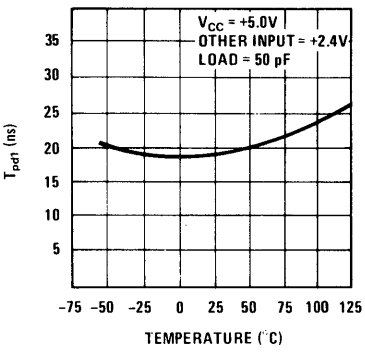
Transition Time To A Logical "0"



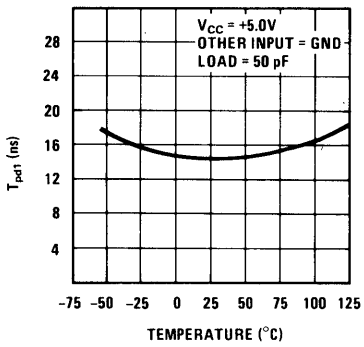
Transition Time To A Logical "0"



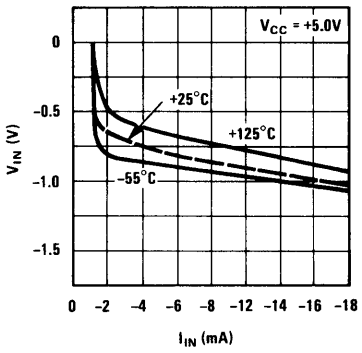
Transition Time To A Logical "1"



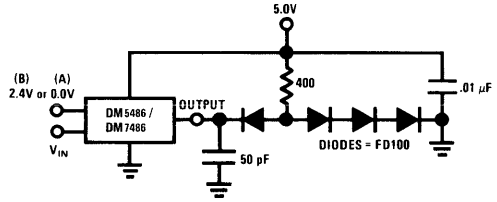
Transition Time To A Logical "1"



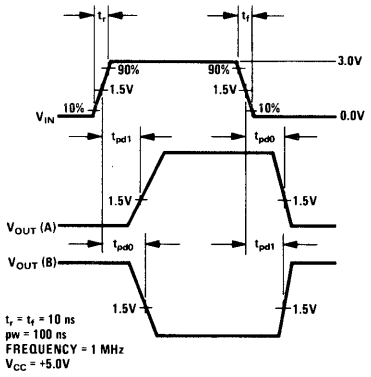
Input Clamp Diode Characteristics



ac test circuit



switching time waveform



Flip Flops, Series 54/74

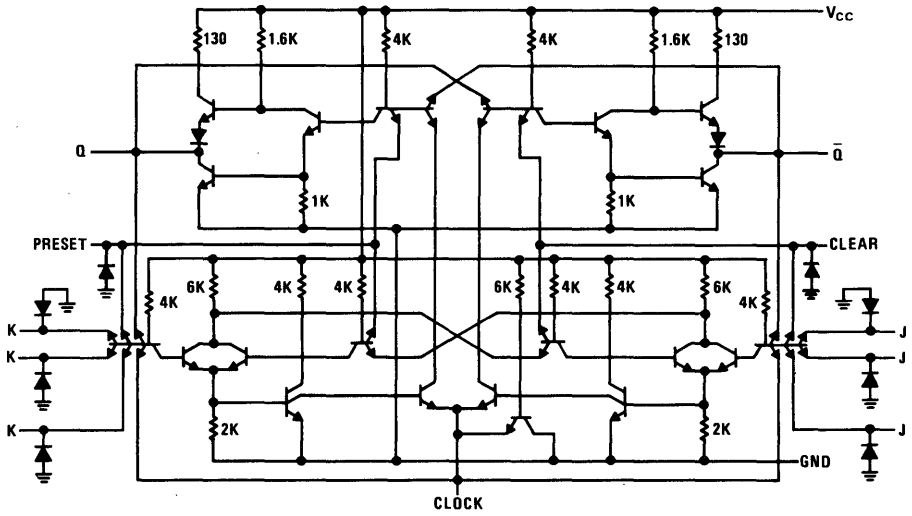
DM5472 / DM7472 (SN5472/SN7472)
J-K master slave flip flop

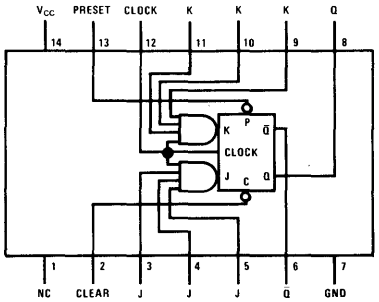
general description

The DM5472/DM7472 is a single flip flop with gating used to perform logic on the J and K inputs. Separate PRESET and CLEAR inputs override the clock and permit the flip flop to be directly set to either state. The flip flop is termed Master-Slave since the J and K information is loaded into the Master section when the clock voltage rises, and is transferred to the Slave section and outputs when the clock voltage falls.

The device also features a special clock line clamp to reduce ringing and prevent false clocking.

schematic and connection diagrams





absolute maximum ratings

V_{CC}	7V
Input Voltage	5.5V
Operating Temperature Range	
DM7472	0°C to 70°C
DM5472	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

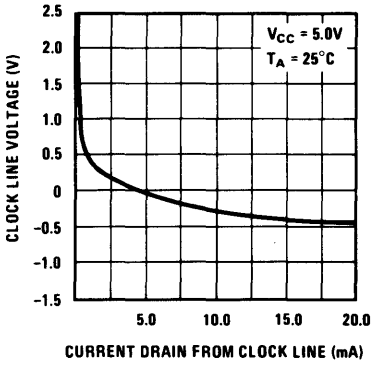
electrical characteristics (Note 1)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
Input Diode Clamp Voltage		V_{CC} = 5.0V T_A = 25°C I_{IN} = −12 mA			−1.5	V
Clock Line Clamp Voltage	DM5472 / DM7472	V_{CC} = 5.5V / V_{CC} = 5.25V I_{CLOCK} = −10 mA			−0.5	V
Logical "1" Input Voltage	DM5472 / DM7472	V_{CC} = 4.5V / V_{CC} = 4.75V	2.0			V
Logical "0" Input Voltage	DM5472 / DM7472	V_{CC} = 4.5V / V_{CC} = 4.75V			0.8	V
Logical "1" Output Voltage	DM5472 / DM7472	V_{CC} = 4.5V / V_{CC} = 4.75V I_{OUT} = −400 μA	2.4			V
Logical "0" Output Voltage	DM5472 / DM7472	V_{CC} = 4.5V / V_{CC} = 4.75V I_{OUT} = 16 mA			0.4	V
Logical "1" Input Current	DM5472 / DM7472	V_{CC} = 5.5V / V_{CC} = 5.25V V_{IN} = 2.4V				
J or K				10	40	μA
CLEAR or PRESET				20	80	μA
CLOCK				<0	80	μA
Logical "1" Input Current	DM5472 / DM7472	V_{CC} = 5.5V / V_{CC} = 5.25V V_{IN} = 5.5V			1	mA
Logical "0" Input Current	DM5472 / DM7472	V_{CC} = 5.5V / V_{CC} = 5.25V V_{IN} = 0.4V				
J or K					−1.6	mA
CLEAR, PRESET, or CLOCK					−3.2	mA
Output Short Circuit Current	DM5472 / DM7472	V_{CC} = 5.5V / V_{CC} = 5.25V V_{OUT} = 0	−20 / −18		−55	mA
Supply Current	DM5472 / DM7472	V_{CC} = 5.5V / V_{CC} = 5.25V		9	17	mA
Minimum Allowable Clock Pulse Width		V_{CC} = 5.0V T_A = 25°C			20	ns
Toggle Frequency		V_{CC} = 5.0V T_A = 25°C	15	27		MHz
Propagation Delay Time to a Logical "0" from Clock, t_{pd0}		V_{CC} = 5.0V T_A = 25°C N = 10 C = 50 pF	15	26	45	ns
Propagation Delay Time to a Logical "1" from Clock, t_{pd1}		V_{CC} = 5.0V T_A = 25°C N = 10 C = 50 pF	10	17	30	ns
Propagation Delay Time to a Logical "0" from CLEAR or PRESET		V_{CC} = 5.0V T_A = 25°C N = 10 C = 50 pF			40	ns
Propagation Delay Time to a Logical "1" from CLEAR or PRESET		V_{CC} = 5.0V T_A = 25°C N = 10 C = 50 pF			25	ns
Time after negative-going clock transition that J or K information must be held, t_{hold}		V_{CC} = 5.0V T_A = 25°C			−5	ns
Time prior to negative-going clock transition that J or K information must be set, t_{setup}		V_{CC} = 5.0V T_A = 25°C	Clock pulse width			ns
Clock Voltage Fall Time		V_{CC} = 5.0V T_A = 25°C			150	ns
Clock Skew ($t_{pd\,min} - t_{hold\,max}$)		V_{CC} = 5.0V T_A = 25°C	15			ns

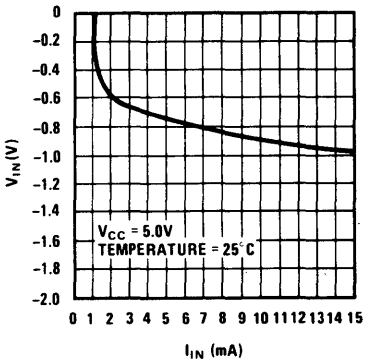
Note 1: Min/max limits apply across the guaranteed temperature range of 0°C to 70°C for the DM7472 and −55°C to +125°C for the DM5472 unless otherwise specified. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

typical performance characteristics

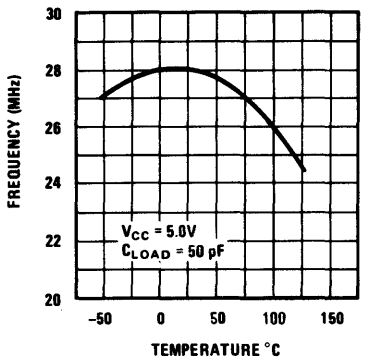
Clock Line Voltage vs Clock Line Current



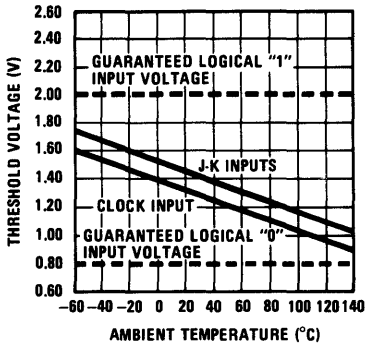
Input Clamp Diode Characteristics Inputs J1, J2, J3, K1, K2, K3



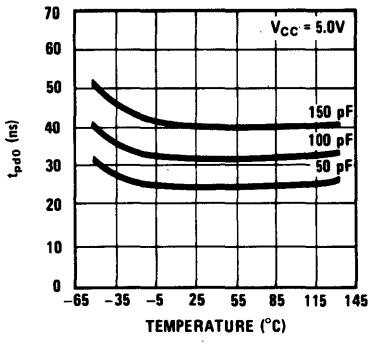
Maximum Toggle Frequency vs Temperature



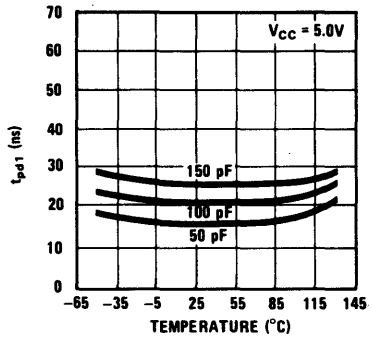
Threshold Voltage vs Temperature



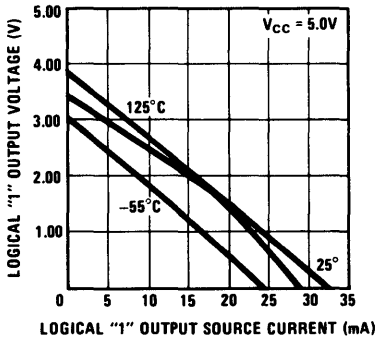
Transition Time to Logical "0" (t_{pd0}) vs Temperature



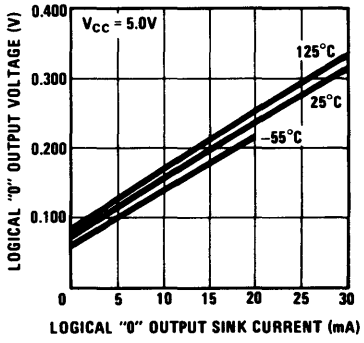
Transition Time to Logical "1" (t_{pd1}) vs Temperature



Logical "1" Output Voltage vs Source Current



Logical "0" Output Voltage vs Sink Current



Flip Flops, Series 54/74

DM5473 / DM7473 (SN5473/SN7473)
DM5476/DM7476 (SN5476/SN7476)
DM54107/DM74107 (SN54107/SN74107)
dual JK master/slave flip flops

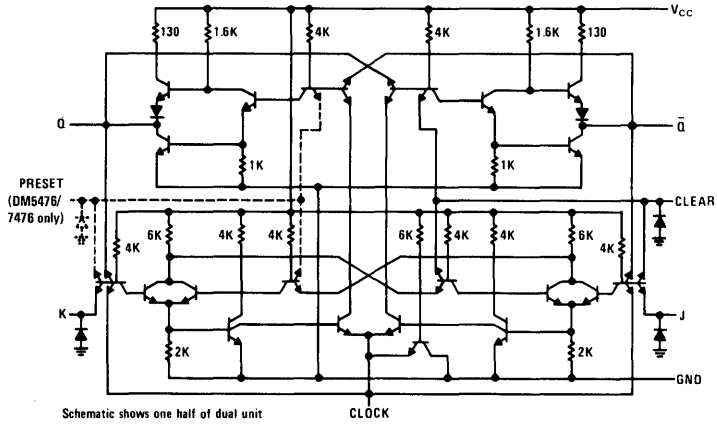
general description

The flip flops described herein are TTL (Transistor-Transistor Logic) dual JK Master/Slave flip flops. Asynchronous CLEAR inputs are provided on the DM5473/DM7473 and DM54107/DM74107 flip flops; and PRESET and CLEAR inputs are available on each of the DM5476/DM7476 flip flops. The latter devices are supplied in a 16 pin package. The devices are totally monolithic and designed for use in high speed control and counting applications, where economy is required, and multiple data inputs are not required. These devices meet all of the electrical and mechanical requirements of the equivalent Series 54/74 devices. They feature:

- High Speed of Operation — 25 MHz toggling
- Optimum Power Dissipation — 45 mW/ff
- High Noise Immunity — 1V
- Guaranteed Clock Skew — 15 ns

The devices also feature a special clock line clamp to reduce ringing and prevent false clocking. In addition, the usual speed-power efficiency and high output drive-capability normally gained with TTL circuits are retained.

schematic and connection diagrams

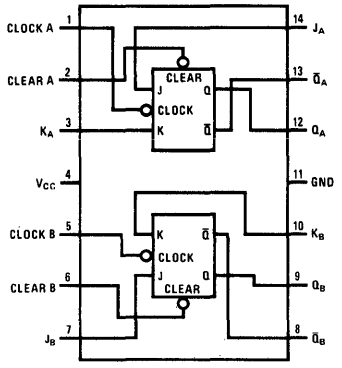


Schematic shows one half of dual unit

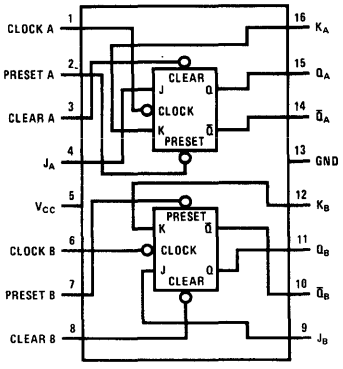
truth table

(Each Flip Flop)		
t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\bar{Q}_n$

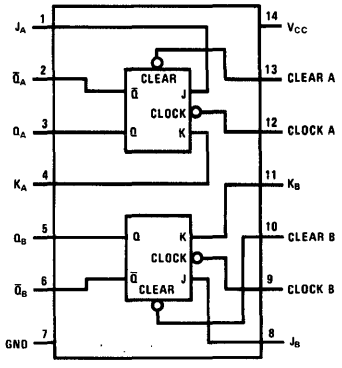
t_n = bit time before clock pulse.
t_{n+1} = bit time after clock pulse.



DM5473/DM7473



DM5476/DM7476



DM54107/DM74107

absolute maximum ratings

Supply Voltage	+7V
Input Voltage	5.5V
Fan Out	10
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	
DM5473/DM5476/DM54107	−55°C to +125°C
DM7473/DM7476/DM74107	0°C to +70°C
Lead Temperature (soldering, 10 sec)	300°C

electrical characteristics (Note 1)

PARAMETER		CONDITION		MIN.	TYP.	MAX.	UNITS
Clock Line Clamp Voltage	DM5473/DM5476/DM54107	V_{CC} = 5.5V	I_{CLOCK} = −10 mA		−.3	−0.5	V
	DM7473/DM7476/DM74107	V_{CC} = 5.25V					
Input Diode Clamp (J, K, Preset, Clear)		V_{CC} = 5.0V	T_A = 25°C, I_{IN} = −12 mA			−1.5	V
Logical "1" Input Voltage	DM5473/DM5476/DM54107	V_{CC} = 4.5V		2.0			V
	DM7473/DM7476/DM74107	V_{CC} = 4.75V					
Logical "0" Input Voltage	DM5473/DM5476/DM54107	V_{CC} = 4.5V				0.80	V
	DM7473/DM7476/DM74107	V_{CC} = 4.75V					
Logical "1" Output Voltage	DM5473/DM5476/DM54107	V_{CC} = 4.5V	I_{OUT} = −400 μA	2.4	3.3		V
	DM7473/DM7476/DM74107	V_{CC} = 4.75V					
Logical "0" Output Voltage	DM5473/DM5476/DM54107	V_{CC} = 4.5V	I_{OUT} = 16.0 mA		0.20	0.40	V
	DM7473/DM7476/DM74107	V_{CC} = 4.75V					
Logical "0" Input Current	DM5473/DM5476/DM54107	V_{CC} = 5.5V	V_{IN} = 0.40V, J or K		−1.0	−1.6	mA
	DM7473/DM7476/DM74107	V_{CC} = 5.25V	Clear, Preset or Clock		−2.0	−3.2	
Logical "1" Input Current	DM5473/DM5476/DM54107	V_{CC} = 5.5V	V_{IN} = 2.4V, J or K		10	40	μA
	DM7473/DM7476/DM74107	V_{CC} = 5.25V	Clear, Preset		20	80	
			Clock		<0	80	
Logical "1" Input Current	DM5473/DM5476/DM54107	V_{CC} = 5.5V	V_{IN} = 5.5V			1	mA
	DM7473/DM7476/DM74107	V_{CC} = 5.25V					
Output Short Current (Note 2)	DM5473/DM5476/DM54107	V_{CC} = 5.5V	V_{OUT} = 0V	−20		−55	mA
	DM7473/DM7476/DM74107	V_{CC} = 5.25V		−18			
Power Supply Current (each flip-flop)	DM5473/DM5476/DM54107	V_{CC} = 5.5V	V_{IN} = 5.0V		9	17	mA
	DM7473/DM7476/DM74107	V_{CC} = 5.25V					
Minimum Allowable Clock Pulse Width (Note 3)		V_{CC} = 5.0V, T_A = 25°C				20	ns
Toggle Frequency		V_{CC} = 5.0V, T_A = 25°C		15	25		MHz
Propagation Delay Time to a Logical "0" from Clock, t_{pd0}		V_{CC} = 5.0V, T_A = 25°C		15	26	45	ns
Propagation Delay Time to a Logical "1" from Clock, t_{pd1}		V_{CC} = 5.0V, T_A = 25°C		10	17	30	ns
Propagation Delay Time to a Logical "0" from Clear, or Preset		V_{CC} = 5.0V, T_A = 25°C		12	23	40	ns
Propagation Delay Time to a Logical "1" from Clear, or Preset		V_{CC} = 5.0V, T_A = 25°C		7	14	25	ns
Time after Negative going Clock Transition that J or K information must be held, t_{hold}		V_{CC} = 5.0V, T_A = 25°C				−5	ns
Clock Skew ($t_{pd\ min} - t_{hold\ max}$)		V_{CC} = 5.0V, T_A = 25°C		15			ns

Note 1: Min/max limits apply across the guaranteed operating temperature range of −55°C to +125°C for the DM5473/DM5476/DM54107 and 0°C to 70°C for the DM7473/DM7476/DM74107 unless specified. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

Note 2: Only one output may be shorted at a time.

Note 3: The flip flop will always recognize a 20 ns pulse, never recognize a 5 ns pulse.

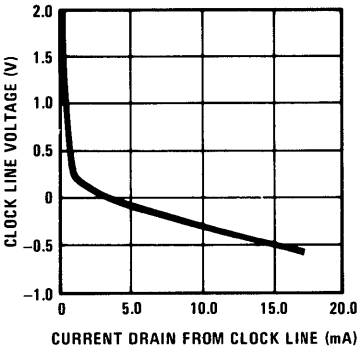
Note 4: No maximum rise and fall times are imposed upon clock or J and K waveforms. However, very slow transitions which allow an input to remain in the threshold region can cause noise problems.

Note 5: See explanation given under "Device Operation."

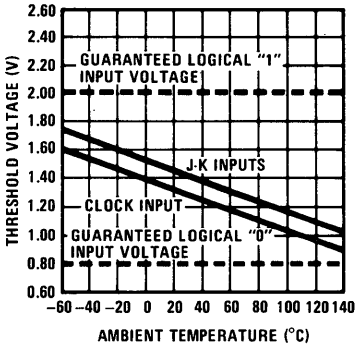
Note 6: J and K information will register properly even though the information is removed 5 ns before the clock pulse voltage falls. However when this occurs it must be assured that the Logical "1" clock pulse level and the desired J and K information occur simultaneously for at least 20 ns.

typical performance characteristics

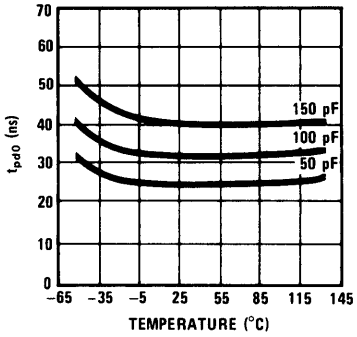
Typical Clock Line Voltage vs Clock Line Current



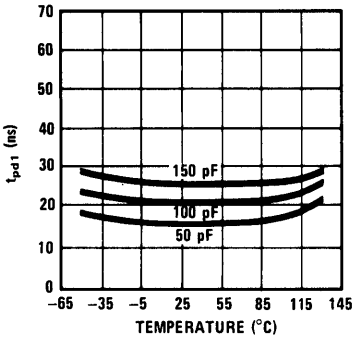
Typical Threshold Voltage vs Temperature



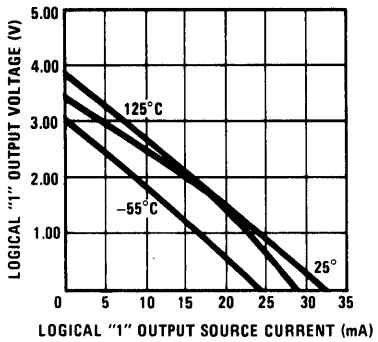
Transition Time to Logical "0" (t_{pd0}) vs Temperature



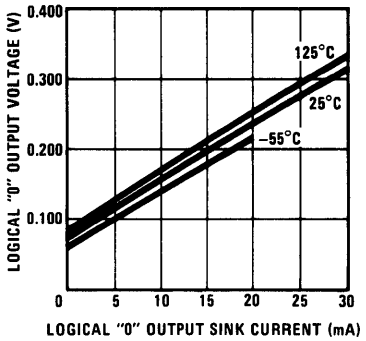
Transition Time to Logical "1" (t_{pd1}) vs Temperature



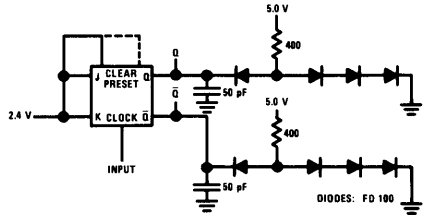
Logical "1" Output Voltage vs Source (Output) Current

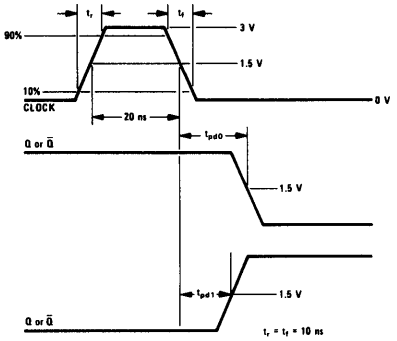


Logical "0" Output Voltage vs Sink Current

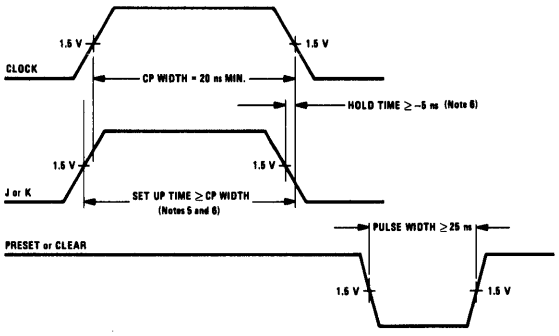


ac test circuit





switching time waveforms (Notes 4, 5)



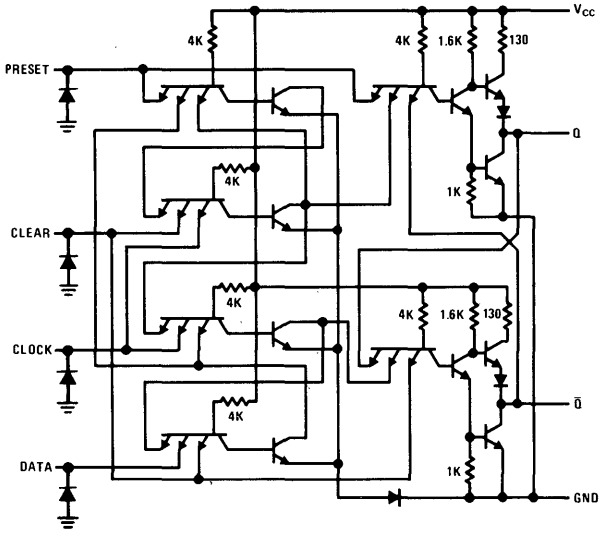
Flip Flops, Series 54/74

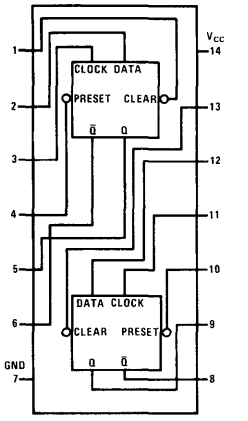
DM5474/DM7474 (SN5474/SN7474) dual D flip flops

general description

The DM5474/DM7474 dual D flip flops are designed for use where the flexibility of two inputs, such as on a JK or an RS flip flop, are not required. If only a single input (two logic combinations) can be utilized, then an extra input is superfluous. The DM5474/DM7474 have only a single DATA input. The logical level applied to this DATA input is transferred to the Q output when the clock pulse voltage rises to a logical 1. It is only necessary to set-up information on the DATA input several nanoseconds before the clock pulse voltage rises; likewise it is only necessary to hold that information several nanoseconds after the clock pulse voltage reaches the logical 1 level. DATA information is then free to change in preparation for the next clock pulse. Since only one pin is used for data entry, fully asynchronous (both PRESET and CLEAR) capability can be provided in a 14 pin dual-in-line package.

schematic and connection diagrams

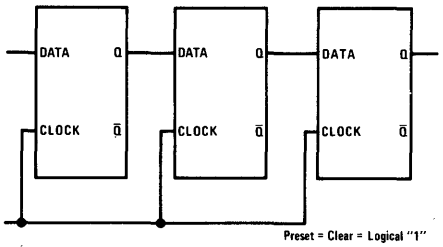




Note: A logical 0 on CLEAR sets Q to a logical 0.
A logical 0 on PRESET sets Q to a logical 1.

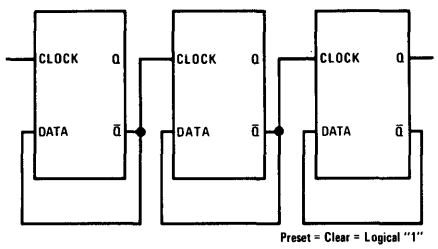
typical applications

shift register



Preset = Clear = Logical "1"

ripple counter (divide-by-2^n)



Preset = Clear = Logical "1"

absolute maximum ratings

Supply Voltage		+7V
Input Voltage		5.5V
Fan Out		10
Storage Temperature Range		−65°C to +150°C
Operating Temperature Range	DM5474	−55°C to +125°C
	DM7474	0°C to +70°C
Lead Temperature (soldering, 10 sec)		300°C

electrical characteristics (Note 1)

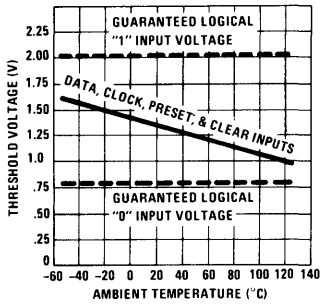
PARAMETER		CONDITION			MIN	TYP	MAX	UNITS
Input Diode Clamp Voltage		V_{CC} = 5.0V, I_{OUT} = −12 mA, T_A = 25°C					−1.5	V
Logical "1" Input Voltage	DM5474	V_{CC} = 4.5V			2.0			V
	DM7474	V_{CC} = 4.75V						
Logical "0" Input Voltage	DM5474	V_{CC} = 4.5V					0.80	V
	DM7474	V_{CC} = 4.75V						
Logical "1" Output Voltage	DM5474	V_{CC} = 4.5V	I_{OUT} = −400 μA		2.4	3.3		V
	DM7474	V_{CC} = 4.75V						
Logical "0" Output Voltage	DM5474	V_{CC} = 4.5V	I_{OUT} = 16.0 mA			0.15		V
	DM7474	V_{CC} = 4.75V						
Logical "0" Input Current	DM5474	V_{CC} = 5.5V	V_{IN} = 0.40V	Data or Preset		−1.0	−1.6	mA
	DM7474	V_{CC} = 5.25V		Clear or Clock		−2.0	−3.2	mA
Logical "1" Input Current	DM5474	V_{CC} = 5.5V	V_{IN} = 2.4V	Data or Preset			40.0	μA
	DM7474	V_{CC} = 5.25V		Clear or Clock			80.0	μA
Logical "1" Input Current	DM5474	V_{CC} = 5.5V	V_{IN} = 5.5V				1.0	mA
	DM7474	V_{CC} = 5.25V						
Output Short Current (Note 2)	DM5474	V_{CC} = 5.5V	V_{OUT} = 0V		−20.0		−55.0	mA
	DM7474	V_{CC} = 5.25V			−18.0			
Power Supply Current (each flip-flop)		V_{CC} = 5.0V, V_{IN} = 5.0V				8.2	13.0	mA
Maximum Clock Frequency		V_{CC} = 5.0V, T_A = 25°C	C = 50 pF		15.0	25.0		MHz
Propagation Delay Time to a Logical "0" from Clock — t_{pd0}		V_{CC} = 5.0V, T_A = 25°C	C = 50 pF		13.0	22.0	45.0	ns
Propagation Delay Time to a Logical "1" from Clock — t_{pd1}		V_{CC} = 5.0V, T_A = 25°C	C = 50 pF		10.0	16.0	30.0	ns
Propagation Delay Time to a Logical "0" from Clear, or Preset — t_{pd0}		V_{CC} = 5.0V, T_A = 25°C					40.0	ns
Propagation Delay Time to a Logical "1" from Clear, or Preset — t_{pd1}		V_{CC} = 5.0V, T_A = 25°C					25.0	ns
Time Prior to Clock Pulse that Data Information Must be Present — $t_{set\ up}$		V_{CC} = 5.0V, T_A = 25°C, C = 50 pF		Logical "1"		15.0	20.0	ns
				Logical "0"		15.0	20.0	ns
Time After Clock Pulse that Data Information Must be Held — t_{hold}		V_{CC} = 5.0V, T_A = 25°C, C = 50 pF		Logical "1"		−5.0	0	ns
				Logical "0"		0.6	3.0	ns

Note 1: Min/max limits apply across the guaranteed operating temperature range of −55°C to +125°C for DM5474 and 0°C to 70°C for DM7474 unless otherwise specified. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

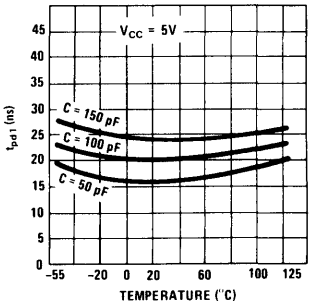
Note 2: Only one output may be shorted at a time.

typical performance characteristics

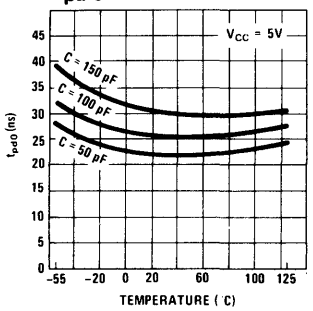
Threshold Voltage vs Temperature*



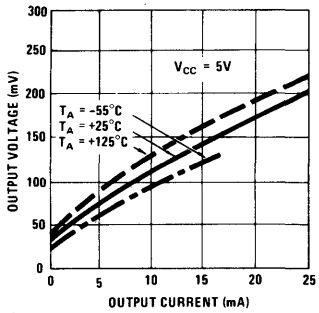
Transition Time to a Logical "1" ($t_{pd\ 1}$) vs Temperature*



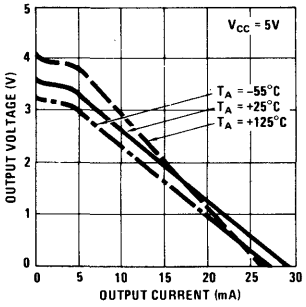
Transition Time to a Logical "0" ($t_{pd\ 0}$) vs Temperature*



Logical "0" Output Voltage vs Sink Current

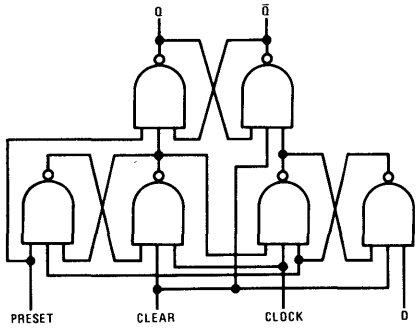


Logical "1" Output Voltage vs Source Current

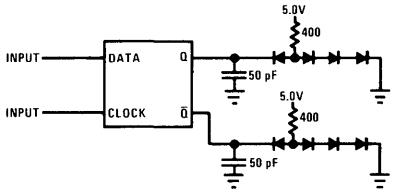


***Note:** Curves apply to DM7474 across 0°C to +70°C range only.

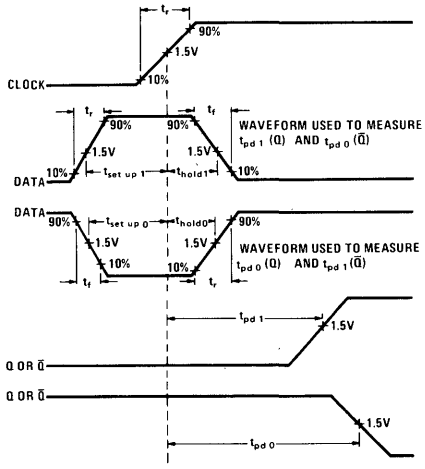
block diagram (each flip flop)



ac test circuit



switching time waveforms



Note: No maximum rise and fall times are imposed upon the clock voltage. However very slow transitions which allow an input to remain in the threshold region can cause noise problems.

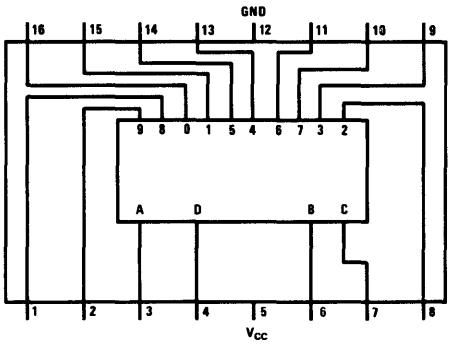
DM5441A/DM7441A (SN5441A/SN7441A) BCD to decimal decoder/nixie* driver

general description

The DM5441A/DM7441A is monolithic binary-coded-decimal to decimal decoder. The BCD number to be decoded is applied to the four input lines; and the unique output corresponding to the decimal equivalent of the input number falls to a logical 0 level. Outputs are designed to drive gas-filled-readout (Nixie*) tubes but are also able to operate with other low current lamps and relays.

An over-range feature provides that if binary numbers between 10 and 15 are applied to the input the least significant bit of these numbers (0 through 5) will be decoded on the output.

connection diagram

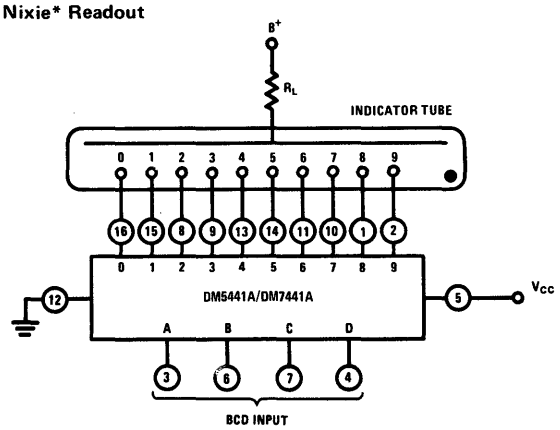


logic table

INPUT D	C	B	A	LOW OUTPUT
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
(OVER-RANGE)				
1	0	1	0	0
1	0	1	1	1
1	1	0	0	2
1	1	0	1	3
1	1	1	0	4
1	1	1	1	5

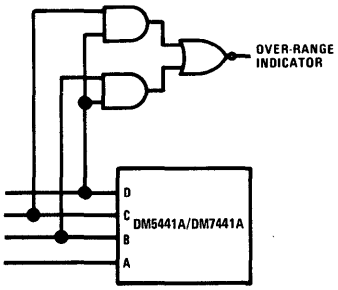
typical applications

Nixie* Readout



NOTE: Values for B+ and R_L are as specified by the tube manufacturer.

Over-Range Decoding



*Trademark of Burroughs Corporation

absolute maximum ratings

Supply Voltage (V_{CC})		7.0V
Output Voltage		70V
Input Voltage		5.5V
Operating Temperature Range	DM5441A	−55°C to +125°C
	DM7441A	0°C to +70°C
Storage Temperature Range		−65°C to +150°C
Lead Temperature (Soldering, 10 sec)		300°C

electrical characteristics (Note 1)

PARAMETER		CONDITIONS			MIN	TYP (Note 2)	MAX	UNITS
Logical 1 Input Voltage	DM5441A	V_{CC} = 4.5V			2.0			V
	DM7441A	V_{CC} = 4.75V						
Logical 0 Input Voltage	DM5441A	V_{CC} = 4.5V					0.8	V
	DM7441A	V_{CC} = 4.75V						
Logical 1 Input Current (all inputs)	DM5441A	V_{CC} = 5.5V	V_{IN} = 2.4V			3	40	μA
	DM7441A	V_{CC} = 5.25V						
Logical 1 Input Current	DM5441A	V_{CC} = 5.5V	V_{IN} = 5.5V				1	mA
	DM7441A	V_{CC} = 5.25V						
Logical 0 Input Current	DM5441A	V_{CC} = 5.5V	V_{IN} = 0.4V			−1.0	−1.6	mA
	DM7441A	V_{CC} = 5.25V						
Supply Current	DM5441A	V_{CC} = 5.5V	V_{IN} = 0.0V			21	36	mA
	DM7441A	V_{CC} = 5.25V						
Logical 1 Output Breakdown	DM5441A	V_{CC} = 5.5V	I_{OUT} = 1.0 mA		70	85		V
	DM7441A	V_{CC} = 5.25V						
Logical 1 Output Current	DM5441A	V_{CC} = 5.5V	V_{OUT} = 50V	125°			60	μA
				70°			40	
	DM7441A	V_{CC} = 5.25V		25°			1.8	
				0°			1.8	
				−55°			1.8	
Logical 0 Output Voltage	DM5441A	V_{CC} = 4.5V	I_{OUT} = 7 mA	125°			3.0	V
				70°			2.5	
	DM7441A	V_{CC} = 4.75V		25°		1.4	2.5	
				0°			2.5	
				−55°			2.5	

Note 1: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DM5441A, and the 0°C to 70°C temperature range for the DM7441A.

Note 2: All typicals apply at 25°C for V_{CC} = 5.0V.

TTL MSI

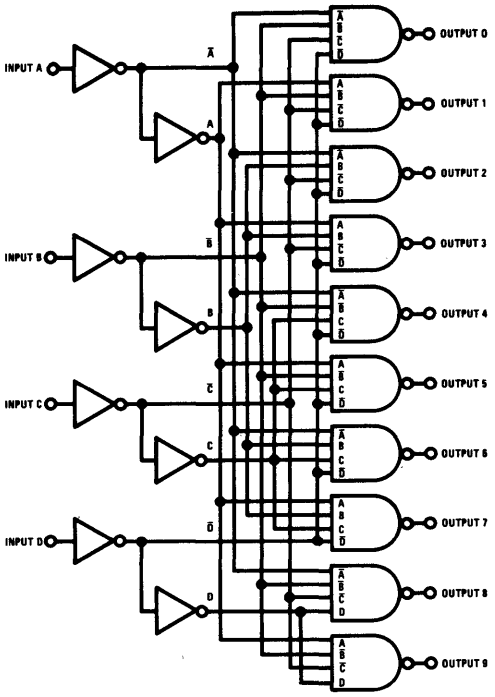
DM5442/DM7442 (SN5442/SN7442) BCD to decimal decoder

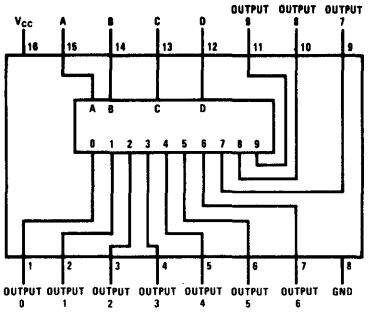
general description

The DM5442/DM7442 utilizes Series 54/74 compatible circuitry to decode a four-bit BCD number to one-of-ten decimal outputs. These ten decimal outputs are capable of driving 10 standard TTL loads each.

The decoding logic is designed such that when binary numbers between 10 and 15 are applied to the inputs, no outputs are enabled.

logic and connection diagrams

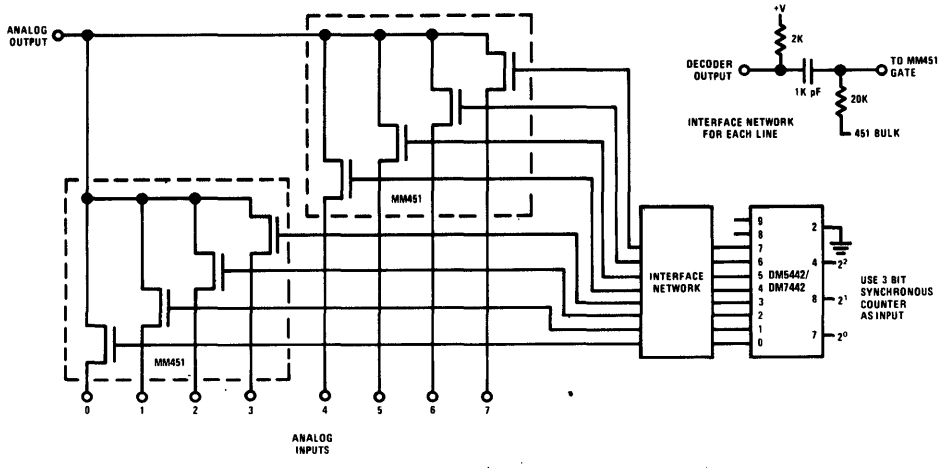




logic table

INPUTS				OUTPUTS									
D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	0	0	0	0	1	1	1	1	1	1	1	1	1
0	0	0	1	1	0	1	1	1	1	1	1	1	1
0	0	1	0	1	1	0	1	1	1	1	1	1	1
0	0	1	1	1	1	1	0	1	1	1	1	1	1
0	1	0	0	1	1	1	1	0	1	1	1	1	1
0	1	0	1	1	1	1	1	1	0	1	1	1	1
0	1	1	0	1	1	1	1	1	1	0	1	1	1
0	1	1	1	1	1	1	1	1	1	1	0	1	1
1	0	0	0	1	1	1	1	1	1	1	1	0	1
1	0	0	1	1	1	1	1	1	1	1	1	1	0
1	0	1	0	1	1	1	1	1	1	1	1	1	1
1	0	1	1	1	1	1	1	1	1	1	1	1	1
1	1	0	0	1	1	1	1	1	1	1	1	1	1
1	1	0	1	1	1	1	1	1	1	1	1	1	1
1	1	1	0	1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1	1	1	1	1

typical application



absolute maximum ratings

Supply Voltage	+7V
Input Voltage	+5.5V
Fan Out	10
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	
DM5442	−55°C to +125°C
DM7442	0°C to +70°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics (Note 1)

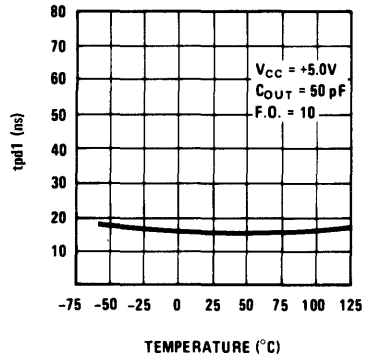
PARAMETER		CONDITION	MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	DM5442 / DM7442	V_{CC} = 4.5V / V_{CC} = 4.75V	2.0			V
Logical "0" Input Voltage	DM5442 / DM7442	V_{CC} = 4.5V / V_{CC} = 4.75V			0.8	V
Logical "1" Output Voltage	DM5442 / DM7442	V_{CC} = 4.5V / V_{CC} = 4.75V, I_{OUT} = −400 μA	2.4			V
Logical "0" Output Voltage	DM5442 / DM7442	V_{CC} = 4.5V / V_{CC} = 4.75V, I_{OUT} = 16 mA			0.4	V
Logical "1" Input Current	DM5442 / DM7442	V_{CC} = 5.5V / V_{CC} = 5.25V, V_{IN} = 2.4			40	μA
Logical "1" Input Current	DM5442 / DM7442	V_{CC} = 5.5V / V_{CC} = 5.25V, V_{IN} = 5.5V			1	mA
Logical "0" Input Current	DM5442 / DM7442	V_{CC} = 5.5V / V_{CC} = 5.25V, V_{IN} = 0.4V		−1.0	−1.6	mA
Input Clamp Diode (All Inputs)	DM5442 / DM7442	V_{CC} = 5.5V / V_{CC} = 5.25V, I_{IN} = −12 mA		−1.0	−1.5	V
Output Short Circuit Current (Note 2)	DM5442 / DM7442	V_{CC} = 5.5V / V_{CC} = 5.25V, V_{OUT} = 0V	−20 / −18	−32	−55	mA
Power Supply Current	DM5442 / DM7442	V_{CC} = 5.5V / V_{CC} = 5.25V		28	56	mA
Propagation Delay Time to a Logical "0" (2 Logic Levels)		V_{CC} = 5.0V, T_A = 25°C, C_{OUT} = 50 pF F.O. = 10	10	23	30	ns
Propagation Delay Time to a Logical "1" (2 Logic Levels)		V_{CC} = 5.0V, T_A = 25°C, C_{OUT} = 50 pF F.O. = 10	8	17	25	ns
Propagation Delay Time to a Logical "0" (3 Logic Levels)		V_{CC} = 5.0V, T_A = 25°C, C_{OUT} = 50 pF F.O. = 10	12	24	35	ns
Propagation Delay Time to a Logical "1" (3 Logic Levels)		V_{CC} = 5.0V, T_A = 25°C, C_{OUT} = 50 pF F.O. = 10	12	26	35	ns

Note 1: Min/max limits apply across the guaranteed operating temperature range −55°C to +125°C for DM5442 and 0°C to 70°C for the DM7442 unless otherwise specified. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

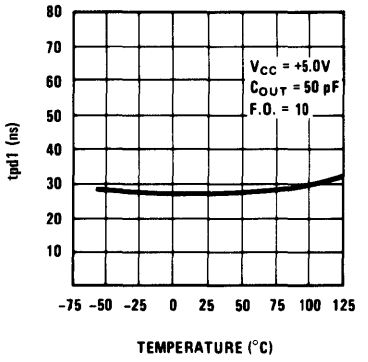
Note 2: Only one output may be shorted at a time.

typical performance characteristics

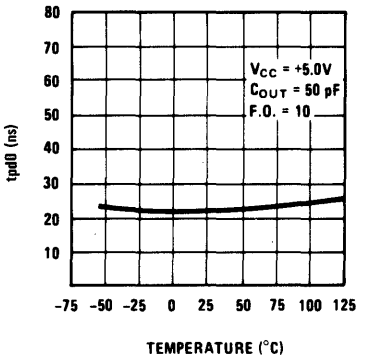
Transition Time to Logical "1" (t_{pd1}) (2 Logic Levels)



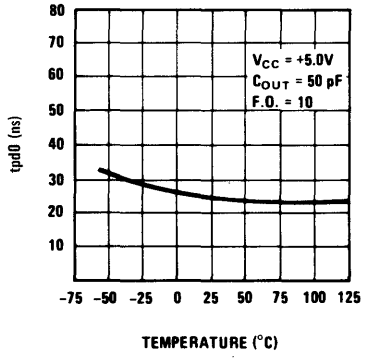
Transition Time to Logical "1" (t_{pd1}) (3 Logic Levels)



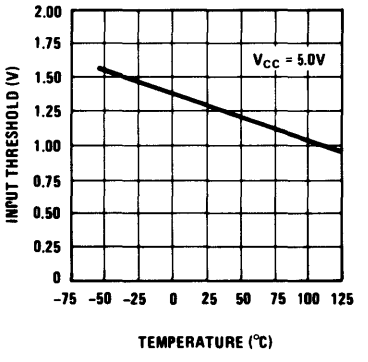
Transition Time to Logical "0" (t_{pd0}) (2 Logic Levels)



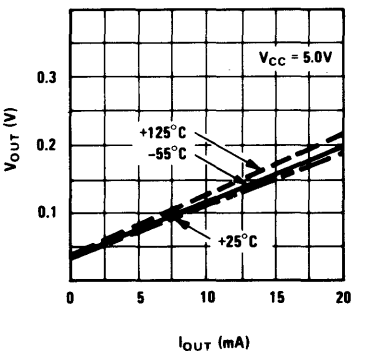
Transition Time to Logical "0" (t_{pd0}) vs Temperature (3 Logic Levels)



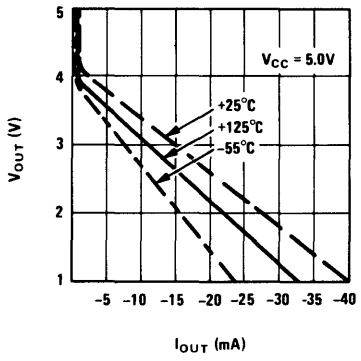
Input Threshold vs Temperature



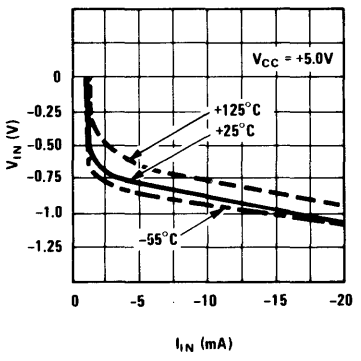
Logical "0" Output Voltage vs Sink Current



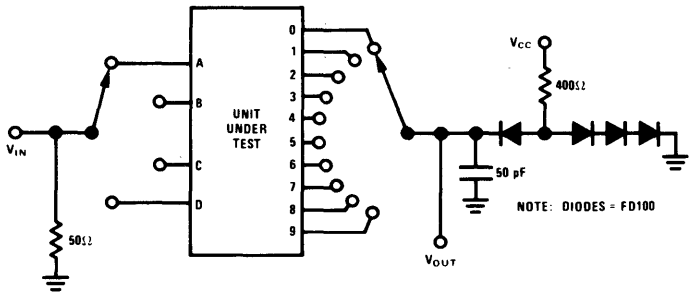
Logical "1" Output Voltage vs Source Current



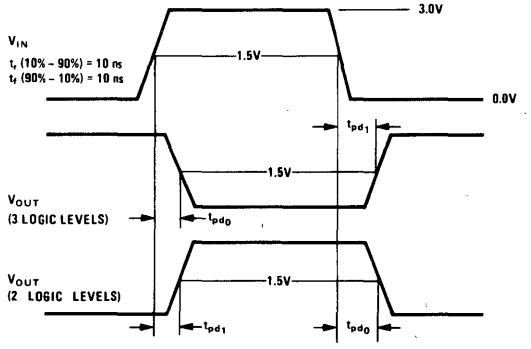
Input Clamp Diode Characteristics



ac test circuit



switching time waveforms



TTL MSI

DM5475/DM7475 (SN5475/SN7475) quad latch

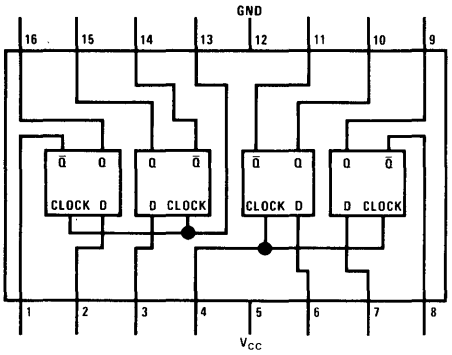
general description

The DM5475/DM7475 is a four-bit storage element utilizing latch-connected gates to perform the memory function. TTL circuitry is employed providing fast speed and high noise immunity.

The information bits to be stored are applied to the D inputs. If the CLOCK input is in the logical 1 state, the Q output will follow the information applied to the corresponding D input. When the CLOCK is taken to the logical 0 state, whatever binary state was present on the D input at the time of this transition will be stored on the Q output. $\overline{Q}$ is also provided for added flexibility.

Two separate clock input lines are provided, each controlling two latches, so that other applications—such as a two-phase flip-flop—can be performed.

logic and connection diagram



truth table

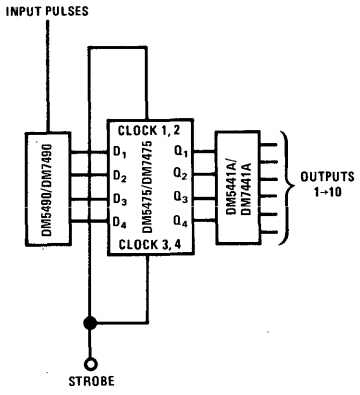
t_n	t_{n+1}	
D	Q	$\overline{Q}$
1	1	0
0	0	1

t_n = time previous to negative-going clock transition

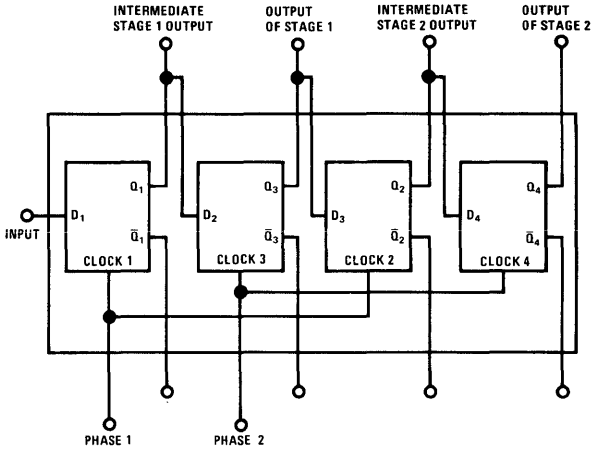
t_{n+1} = time after negative-going clock transition

typical applications

Buffer Storage for Indicators



Dual Rank Shift Register



absolute maximum ratings

Supply Voltage		+7V
Input Voltage		5.5V
Fanout		10
Storage Temperature Range		−65°C to +150°C
Operating Temperature Range	DM5475	−55°C to +125°C
	DM7475	0°C to +70°C
Lead Temperature (Soldering, 10 sec)		300°C

electrical characteristics (Note 1)

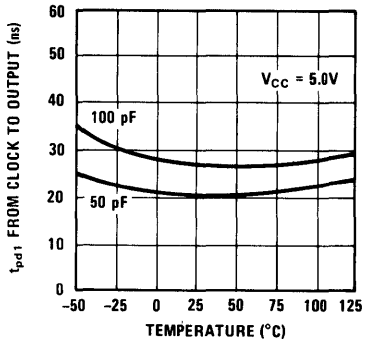
PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
Input Diode Clamp Voltage		V_{CC} = 5.0V I_{OUT} = −12 mA, T_A = 25°C		−.95	−1.5	V
Logical "1" Input Voltage	DM5475	V_{CC} = 4.5V	2.0			V
	DM7475	V_{CC} = 4.75V				
Logical "0" Input Voltage	DM5475	V_{CC} = 4.5V			0.8	V
	DM7475	V_{CC} = 4.75V				
Logical "1" Output Voltage	DM5475	V_{CC} = 4.5V, I_{OUT} = −400 μA	2.4			V
	DM7475	V_{CC} = 4.75V				
Logical "0" Output Voltage	DM5475	V_{CC} = 4.5V, I_{OUT} = 16 mA			0.4	V
	DM7475	V_{CC} = 4.75V				
Logical "1" Input Current	DM5475	V_{CC} = 5.5V, V_{IN} = 2.4V, D CLOCK			80	μA
	DM7475	V_{CC} = 5.25V			80	μA
Logical "1" Input Current	DM5475	V_{CC} = 5.5V, V_{IN} = 5.5V			1	mA
	DM7475	V_{CC} = 5.25V				
Logical "0" Input Current	DM5475	V_{CC} = 5.5V, V_{IN} = 0.4V, D CLOCK		−2.1	−3.2	mA
	DM7475	V_{CC} = 5.25V		−2.1	−3.2	mA
Output Short Current (Note 2)	DM5475	V_{CC} = 5.5V, V_{OUT} = 0V	−20	−32	−55	mA
	DM7475	V_{CC} = 5.25V	−18			
Supply Current	DM5475	V_{CC} = 5.5V		32	46	mA
	DM7475	V_{CC} = 5.25V			50	mA
Propagation Delay Time to a Logical "0" from Clock, t_{pd0}		V_{CC} = 5.0V, T_A = 25°C	3	7	15	ns
Propagation Delay Time to a Logical "1" from Clock, t_{pd1}		V_{CC} = 5.0V, T_A = 25°C	10	21	40	ns
Setup Time for a Logical "1", t_{s1}		V_{CC} = 5.0V, T_A = 25°C		10	20	ns
Setup Time for a Logical "0", t_{s0}		V_{CC} = 5.0V, T_A = 25°C		12	25	ns

Note 1: These specifications apply across the −55°C to +125°C temperature range for the DM5475 and the 0°C to +70°C temperature range for the DM7475 unless otherwise specified. Typicals apply only to 25°C @ V_{CC} = 5.0V.

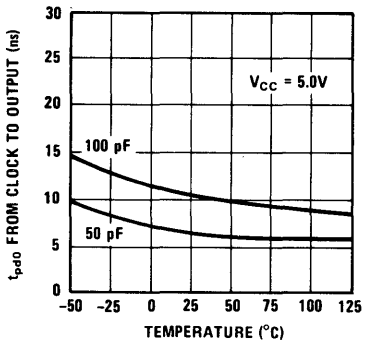
Note 2: Only one output should be shorted at a time.

typical performance characteristics

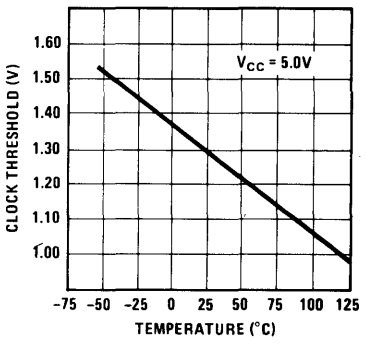
Transition Time to Logical "1" (t_{pd1}) vs Temperature



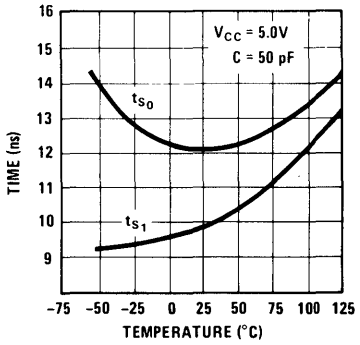
Transition Time to Logical "0" (t_{pd0}) vs Temperature



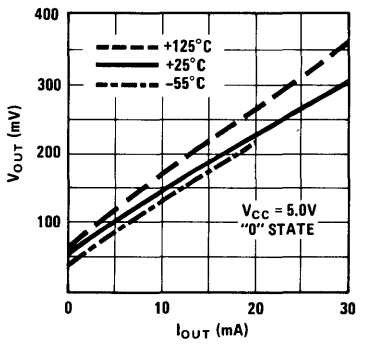
Clock Threshold vs Temperature



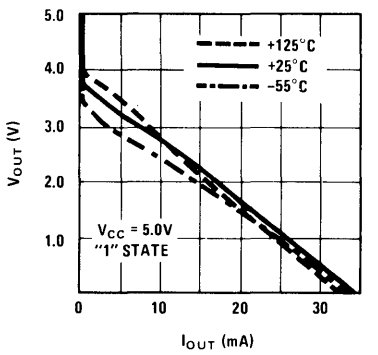
Setup Time vs Temperature



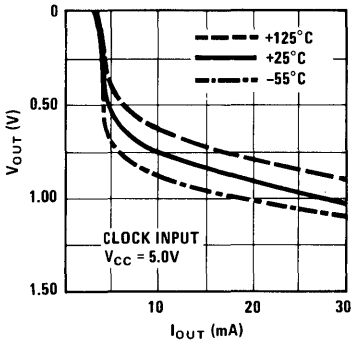
Logical "0" Output Voltage vs Sink Current



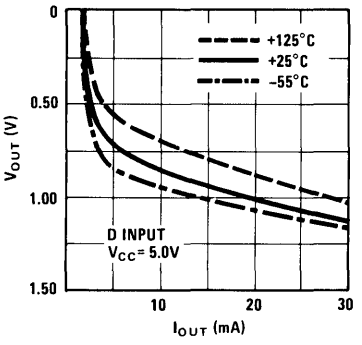
Logical "1" Output Voltage vs Source Current



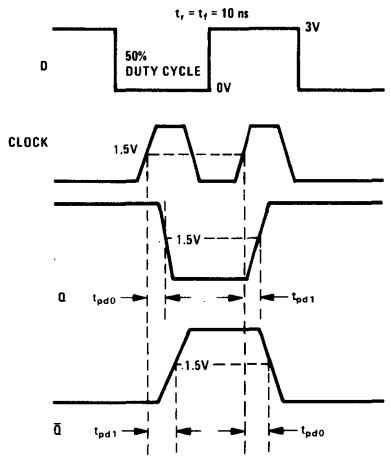
Input Clamp Diode Characteristics



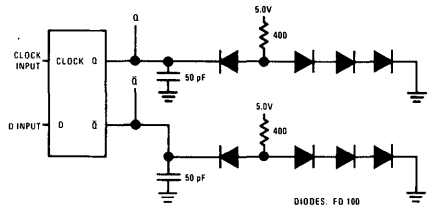
Input Clamp Diode Characteristics



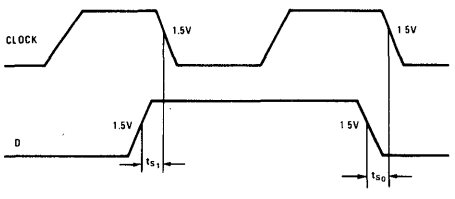
switching time waveforms



ac test circuit



timing requirements



TTL MSI

DM5483 / DM7483 (SN5483/SN7483) four-bit binary full adder and dual single-bit binary full adder

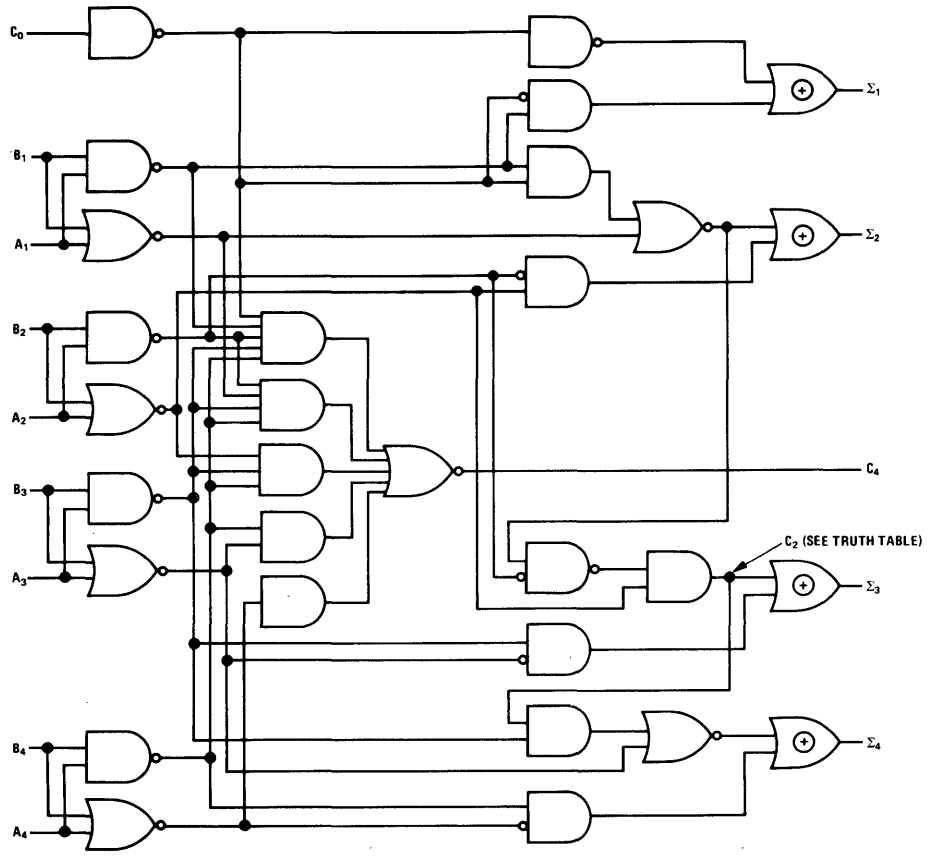
general description

The DM5483/DM7483 binary full adder adds two four-bit binary numbers. A carry input is included and four Σ outputs are provided along with the resultant carry. Since the carry-ripple-time is the limiting delay in the addition of a long word length, carry look-ahead circuitry has been included in the design to minimize this delay. Typical propagation delay from Carry-input to Carry output is 12 ns.

The device can also be used as a dual single-bit binary full adder. (See application.) In this application the Σ_2 output is used as the CARRY output for BIT 1; and the $A_3 B_3$ inputs are used as the CARRY input for Bit 2.

It is completely compatible with other Series 54/74 devices.

logic diagram



absolute maximum ratings

V_{CC}		7V
Input Voltage		5.5V
Operating Temperature Range	DM7483	0°C to 70°C
	DM5483	−55°C to +125°C
Storage Temperature Range		−65°C to +150°C
Lead Temperature (Soldering, 10 sec)		300°C

electrical characteristics (Note 1)

PARAMETER		CONDITION		MIN	TYP	MAX	UNITS
Input Diode Clamp Voltage		V_{CC} = 5.0V, T_A = 25°C, I_{IN} = −12 mA				−1.5	V
Logical "1" Input Voltage	DM5483	V_{CC} = 4.5V		2.0			V
	DM7483	V_{CC} = 4.75V					
Logical "0" Input Voltage	DM5483	V_{CC} = 4.5V				0.8	V
	DM7483	V_{CC} = 4.75V					
Logical "1" Output Voltage	DM5483	V_{CC} = 4.5V	V_{IN} = 0.8V, I_{OUT} = −400 μA (Note 3)	2.4			V
	DM7483	V_{CC} = 4.75V					
Logical "0" Output Voltage	DM5483	V_{CC} = 4.5V	V_{IN} = 2.0V, I_{OUT} = 16 mA (Note 3)			0.4	V
	DM7483	V_{CC} = 4.75V					
Logical "1" Input Current (all inputs)	DM5483	V_{CC} = 5.5V	V_{IN} = 2.4V			80	μA
	DM7483	V_{CC} = 5.25V					
Logical "1" Input Current	DM5483	V_{CC} = 5.5V	V_{IN} = 5.5V			1	mA
	DM7483	V_{CC} = 5.25V					
Logical "0" Input Current (all inputs)	DM5483	V_{CC} = 5.5V	V_{IN} = 0.4V			−3.2	mA
	DM7483	V_{CC} = 5.25V					
Output Short Circuit Current (Note 2) (except C_4)	DM5483	V_{CC} = 5.5V		−20		−55	mA
	DM7483	V_{CC} = 5.25V		−18			
Output Short Circuit Current (for C_4)	DM5483	V_{CC} = 5.5V		−27		−70	mA
	DM7483	V_{CC} = 5.25V					
Supply Current	DM5483	V_{CC} = 5.5V			58	79	mA
	DM7483	V_{CC} = 5.25V					

switching characteristics V_{CC} = 5V, T_A = 25°C

PARAMETER	FROM (INPUT)	TO (OUTPUT)	CONDITION	MIN	TYP	MAX	UNITS
t_{pd1}	C_{IN}	Σ_1	N = 10, C = 50 pF		23	34	ns
t_{pd0}			N = 10, C = 50 pF		20	34	ns
t_{pd1}	C_{IN}	Σ_2	N = 10, C = 50 pF		24	35	ns
t_{pd0}			N = 10, C = 50 pF		22	35	ns
t_{pd1}	C_{IN}	Σ_3	N = 10, C = 50 pF		30	50	ns
t_{pd0}			N = 10, C = 50 pF		24	40	ns
t_{pd1}	C_{IN}	Σ_4	N = 10, C = 50 pF		30	50	ns
t_{pd0}			N = 10, C = 50 pF		28	50	ns
t_{pd1}	C_{IN}	C_4	N = 5, C = 50 pF		12	20	ns
t_{pd0}			N = 5, C = 50 pF		12	20	ns
t_{pd1}	A_2 or B_2	Σ_2	N = 10, C = 50 pF			40	ns
t_{pd0}			N = 10, C = 50 pF			35	ns
t_{pd1}	A_4 or B_4	Σ_4	N = 10, C = 50 pF			40	ns
t_{pd0}			N = 10, C = 50 pF			35	ns

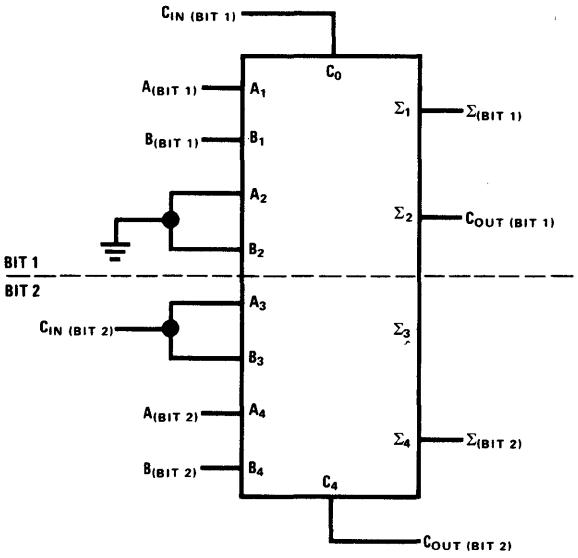
Note 1: Min/Max limits apply across the guaranteed temperature range of 0°C to 70°C for the DM7483 and −55°C to +125°C for the DM5483 unless otherwise specified. All typicals are given for V_{CC} = 5.0V and T_A = 25°C

Note 2: Only one output at a time should be short circuited.

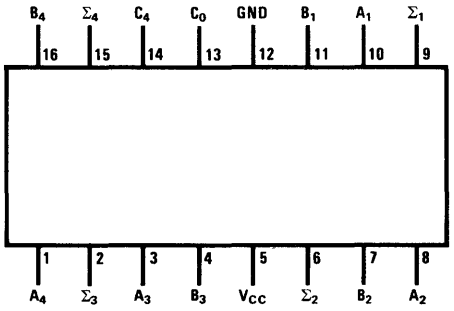
Note 3: For C_4 output, $I_{OUT(1)}$ = −200 μA, $I_{OUT(0)}$ = 8 mA.

typical application

Connect the DM5483/DM7483 in the following manner to implement a dual single-bit full adder.



connection diagram



truth table (See Note 1)

INPUT						OUTPUT					
				WHEN C_{in} = 0			WHEN C_{in} = 1		
				WHEN C_2 = 0			WHEN C_2 = 1		
A_1 / A_3	B_1 / B_3	A_2 / A_4	B_2 / B_4	Σ_1 / Σ_3	Σ_2 / Σ_4	C_2 / C_4	Σ_1 / Σ_3	Σ_2 / Σ_4	C_2 / C_4
0	0	0	0	0	0	0	1	0	0
1	0	0	0	1	0	0	0	1	0
0	1	0	0	1	0	0	0	1	0
1	1	0	0	0	1	0	1	1	0
0	0	1	0	0	1	0	1	1	0
1	0	1	0	1	1	0	0	0	1
0	1	1	0	1	1	0	0	0	1
1	1	1	0	0	0	1	1	0	1
0	0	0	1	0	1	0	1	1	0
1	0	0	1	1	1	0	0	0	1
0	1	0	1	1	1	0	0	0	1
1	1	0	1	0	0	1	1	0	1
0	0	1	1	0	0	1	1	0	1
1	0	1	1	1	0	1	0	1	1
0	1	1	1	1	0	1	0	1	1
1	1	1	1	0	1	1	1	1	1

Note 1: Input conditions at A_1, A_2, B_1, B_2, and C_{in} are used to determine outputs Σ_1 and Σ_2, and the value of the internal carry C_2. The values at C_2, A_3, B_3, A_4, and B_4, are then used to determine outputs Σ_3, Σ_4, and C_4.

DM5490/DM7490 (SN5490/SN7490)decade counter
DM5492/DM7492 (SN5492/SN7492) divide-by-twelve counter
DM5493/DM7493 (SN5493/SN7493) four-bit binary counter

general description

These TTL (Transistor-Transistor-Logic) monolithic counters are capable of counting pulses at a guaranteed frequency of 20 MHz. Gating is provided to reset the counters to the more popular states. Characteristics include high speed at moderate power dissipation, high noise immunity, and minimal variation in performance over temperature. These circuits are completely compatible with other series 54/74 devices.

To provide greater flexibility, the counters may be used in any of the modes as follows:

DM5490/DM7490

1. BCD decade counter—connect the A output to the BD input. This is the normal mode of operation.
2. Symmetrical divide-by-ten operation—connect the D output to the A input. When pulses are then applied to the BD input, a symmetrical waveform one tenth of the applied frequency will appear at the A output.
3. Divide-by-five operation—if no external connections are made a frequency division of five will result between the BD input and the D output. This allows the flip flop A to be used to divide-by-two if desired.

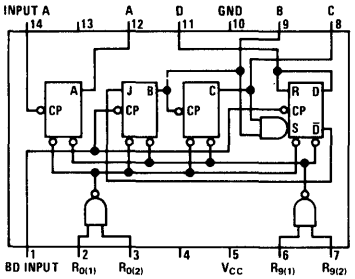
DM5492/DM7492

1. When used as a divide-by-twelve counter output A is connected to the BC input. In this mode outputs A, C, and D provide divisions by 2, 6, and 12 respectively.
2. When the connection is not made between A and BC, and when an input frequency is applied to the BC input, a frequency division of 3 and 6 results on the C and D outputs respectively. In this mode the A flip flop may be used independently except for the common reset input.

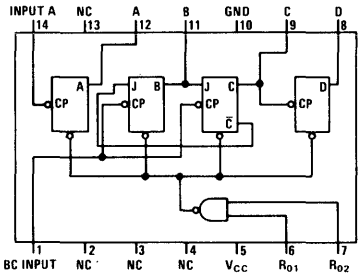
DM5493/DM7493

1. When used as a four-bit binary counter, output A is connected to the B input. In this mode outputs A, B, C, and D provide divisions by 2, 4, 8, and 16 respectively.
2. When the connection is not made between A and B and when an input frequency is applied to the B input, a frequency division of 2, 4 and 8 results on the B, C, and D outputs respectively. In this mode the A flip flop may be used independently except for the common reset input.

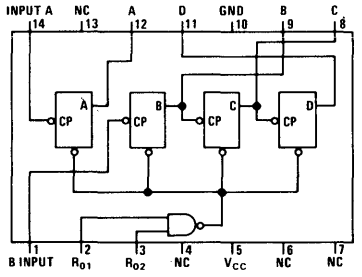
logic and connection diagrams



DM5490/DM7490



DM5492/DM7492



DM5493/DM7493

absolute maximum ratings

Supply Voltage	7V
Input Voltage	5.5V
Operating Temperature Range	
DM5490, DM5492, DM5493	−55°C to +125°C
DM7490, DM7492, DM7493	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (soldering, 10 sec)	300°C

electrical characteristics (Note 1)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
Input Diode Clamp Voltage		V_{CC} = 5.0V, T_A = 25°C	I_{OUT} = −12 mA		−1.0	−1.5	mA
Logical "1" Input Voltage	DM5490, 92, 93 / DM7490, 92, 93	V_{CC} = 4.5V / V_{CC} = 4.75V		2.0			V
Logical "0" Input Voltage	DM5490, 92 ,93 / DM7490, 92, 93	V_{CC} = 4.5V / V_{CC} = 4.75V				.8	V
Logical "1" Output Voltage	DM5490, 92, 93 / DM7490, 92, 93	V_{CC} = 4.5V / V_{CC} = 4.75V	I_{OUT} = −400 μA	2.4			V
Logical "0" Output Voltage	DM5490, 92, 93 / DM7490, 92, 93	V_{CC} = 4.5V / V_{CC} = 4.75V	I_{OUT} = 16 mA		.2	.4	V
Logical "1" Input Current	DM5490, 92, 93 / DM7490, 92, 93	V_{CC} = 5.5V / V_{CC} = 5.25V	V_{IN} = 5.5V			1	mA
Output Short Circuit Current	DM5490, 92, 93 / DM7490, 92, 93	V_{CC} = 5.5V / V_{CC} = 5.25V	(Note 2)	20 18		55 55	mA
DM5490/DM7490							
Logical "1" Input Current	DM5490 / DM7490	V_{CC} = 5.5V / V_{CC} = 5.25V	V_{IN} = 2.4V				
$R_{0(1)}$, $R_{0(2)}$, $R_{9(1)}$, $R_{9(2)}$						40	μA
A						80	μA
BD						160	μA
Logical "0" Input Current	DM5490 / DM7490	V_{CC} = 5.5V / V_{CC} 5.25V	V_{IN} = .4V				
$R_{0(1)}$, $R_{0(2)}$, $R_{9(1)}$, $R_{9(2)}$						1.6	mA
A						3.2	mA
BD						6.4	mA
Supply Current	DM5490 / DM7490	V_{CC} = 5.5V / V_{CC} = 5.25V			32	45	mA
Maximum Input Frequency		V_{CC} = 5.0V, F.O. = 10,	T_A = 25°C, C_O = 50 pF	20	32		MHz
Propagation Delay Time to a Logical "1" Level From Input to Output	A / B / C / D	F.O. = 10, C_{OUT} = 50 pF, All Outputs	V_{CC} = 5.0V, T_A = 25°C		16 35 50 35	35 60 80 60	ns ns ns ns
Propagation Delay Time to a Logical "0" Level From Input to Output	A / B / C / D	F.O. = 10, C_{OUT} = 50 pF, All Outputs	V_{CC} = 5.0V, T_A = 25°C		19 35 50 35	35 60 80 60	ns ns ns ns
Minimum Allowable Clock Pulse Width (Note 3)		V_{CC} = 5.0V, T_A = 25°C			8	15	ns
DM5492/DM7492							
Logical "1" Input Current	DM5492 / DM7492	V_{CC} = 5.5V / V_{CC} = 5.25V	V_{IN} = 2.4V				
$R_{0(1)}$, $R_{0(2)}$						40	μA
A						80	μA
BC						160	μA

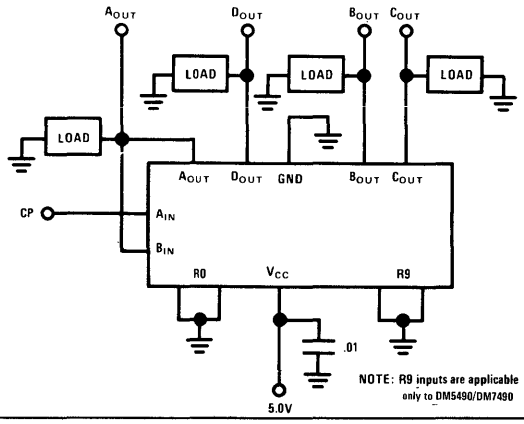
PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
DM5492/DM7492 (Continued)							
Logical "0" Input Current	DM5492 / DM7492	V_{CC} = 5.5V / V_{CC} = 5.25V	V_{IN} = .4V				
$R_{0(1)}$, $R_{0(2)}$						1.6	mA
A						3.2	mA
BC						6.4	mA
Supply Current	DM5492 / DM7492	V_{CC} = 5.5V / V_{CC} = 5.25V	V_{IN} (R_0) = 4.5V		30	43	mA
Maximum Input Frequency		V_{CC} = 5.0V, F.O. = 10,	T_A = 25°C, C_O = 50 pF	20	32		MHz
Propagation Delay Time to a Logical "1" Level From Input A to Output	A	F.O. = 10, C_{OUT} = 50 pF, All Outputs	V_{CC} = 5.0V, T_A = 25°C		16	35	ns
	B				35	60	ns
	C				35	60	ns
	D				50	80	ns
Propagation Delay Time to a Logical "0" Level From Input A to Output	A	F.O. = 10, C_{OUT} = 50 pF, All Outputs	V_{CC} = 5.0V, T_A = 25°C		19	35	ns
	B				35	60	ns
	C				35	60	ns
	D				50	80	ns
Minimum Allowable Clock Pulse Width (Note 3)		V_{CC} = 5.0V, T_A = 25°C			8	15	ns
DM5493/DM7493							
Logical "1" Input Current	DM5493 / DM7493	V_{CC} = 5.5V / V_{CC} = 5.25V	V_{IN} = 2.4V				
$R_{0(1)}$, $R_{0(2)}$						40	μA
A, B						80	μA
Logical "0" Input Current	DM5493 / DM7493	V_{CC} = 5.5V / V_{CC} = 5.25V	V_{IN} = .4V				
$R_{0(1)}$, $R_{0(2)}$						1.6	mA
A, B						3.2	mA
Supply Current	DM5493 / DM7493	V_{CC} = 5.5V / V_{CC} = 5.25V			30	43	mA
Maximum Input Frequency		V_{CC} = 5.0V, F.O. = 10,	T_A = 25°C, C_O = 50 pF	20	32		MHz
Propagation Delay Time to a Logical "1" Level From Input to Output	A	F.O. = 10, C_{OUT} = 50 pF, All Outputs	V_{CC} = 5.0V, T_A = 25°C		16	35	ns
	B				35	60	ns
	C				50	80	ns
	D				65	100	ns
Propagation Delay Time to a Logical "0" Level From Input to Output	A	F.O. = 10, C_{OUT} = 50 pF, All Outputs	V_{CC} = 5.0V, T_A = 25°C		19	35	ns
	B				35	60	ns
	C				50	80	ns
	D				64	100	ns
Minimum Allowable Clock Pulse Width (Note 3)		V_{CC} = 5.0V, T_A = 25°C			8	15	ns

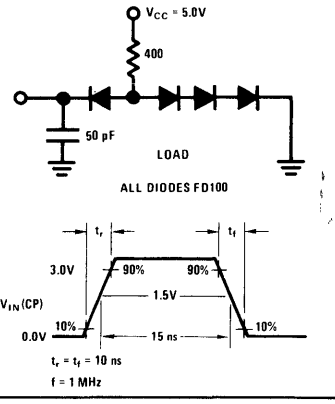
Note 1: Min/max limits apply across the guaranteed operating temperature range of −55°C to +125°C for the DM5490, DM5492 and DM5493 and 0°C to 70°C for the DM7490, DM7492 and DM7493 unless otherwise specified. All typicals are given for V_{CC} = 5.0V and T_A = 25 C.

Note 2: Only one output may be shorted at a time.

Note 3: The flip flop will always recognize a 15 ns pulse.

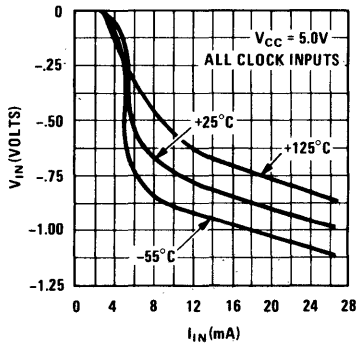
ac test circuit



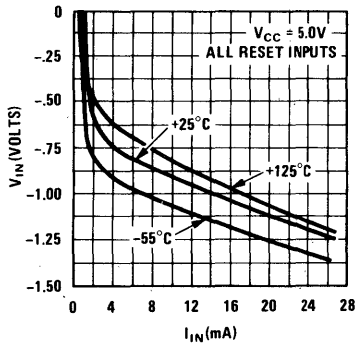


typical performance characteristics

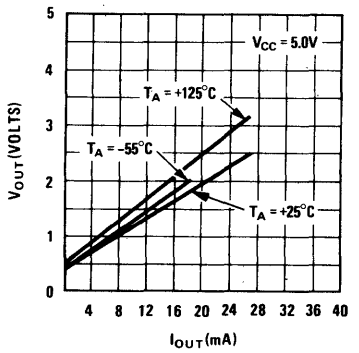
Input Clamp Diode Characteristic



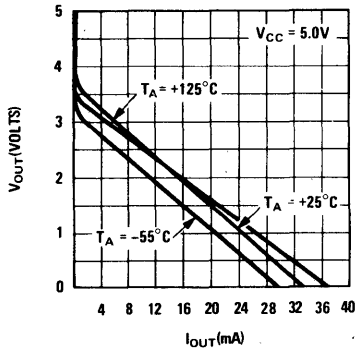
Input Clamp Diode Voltage



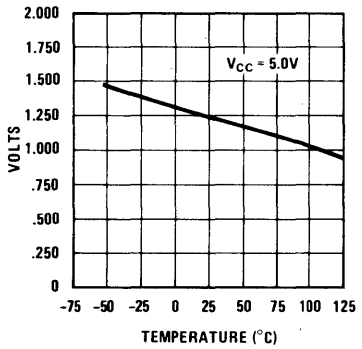
Logical "0" Output Voltage vs Sink Current



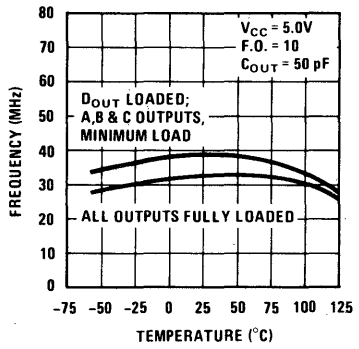
Logical "1" Output Voltage vs Source Current



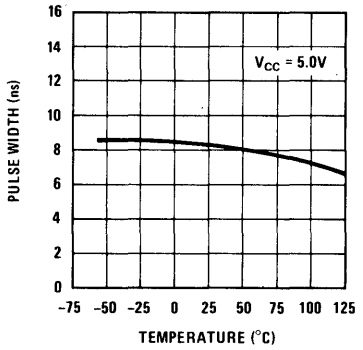
Clock Threshold vs Temperature



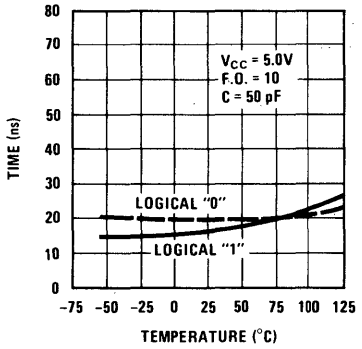
Maximum Frequency vs Temperature



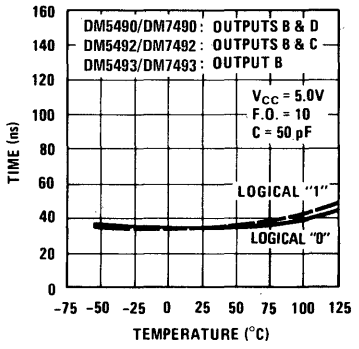
Minimum Clock Pulse Width vs Temperature



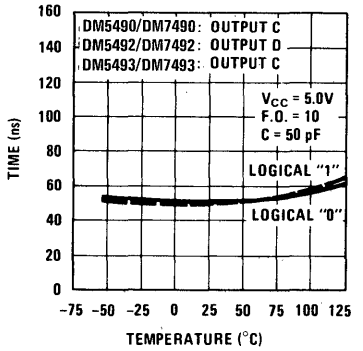
Transition Time to Output A



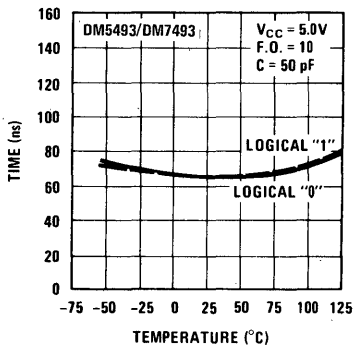
Transition Time to Outputs B, C, & D



Transition Time to Outputs C & D



Transition Time to Output D



BCD count sequence

DM5490/DM7490

COUNT	OUTPUT			
	D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

RESET OPERATION

To reset the counter to the BCD count of zero, both Reset 0 inputs must be at logical "1" levels while at least one Reset 9 input is at a logical "0" level.

To reset the counter to the BCD count of nine, both Reset 9 inputs must be at logical "1" levels; while at least one Reset 0 input is at a logical "0".

Notes:

1. Counting occurs on the negative-going edge of the input pulse.
2. At least one of the Reset 0 inputs and at least one of the Reset 9 inputs must be at a logical "0" for proper counting.
3. For ÷ 10 counting, connect the A output to the BD input.

count sequence

DM5492/DM7492

COUNT	OUTPUT			
	D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	1	0	0	0
7	1	0	0	1
8	1	0	1	0
9	1	0	1	1
10	1	1	0	0
11	1	1	0	1

RESET OPERATION

To reset the counter to the count of zero, both Reset 0 inputs must be at logical "1" levels.

Notes:

1. Counting occurs on the negative-going edge of the input pulse.
2. At least one of the Reset 0 inputs must be at a logical "0" for proper counting.
3. For ÷12 counting, connect the A output to the BC input.

DM5493/DM7493

COUNT	OUTPUT			
	D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1

RESET OPERATION

To reset the counter to the count of zero, both Reset 0 inputs must be at logical "1" levels.

Notes:

1. Counting occurs on the negative-going edge of the input pulse.
2. At least one of the Reset 0 inputs must be at a logical "0" for proper counting.
3. For ÷16 counting, connect the A output to the B input.

TTL MSI

DM5495/DM7495(SN5495/SN7495)
4-bit right-shift left-shift register

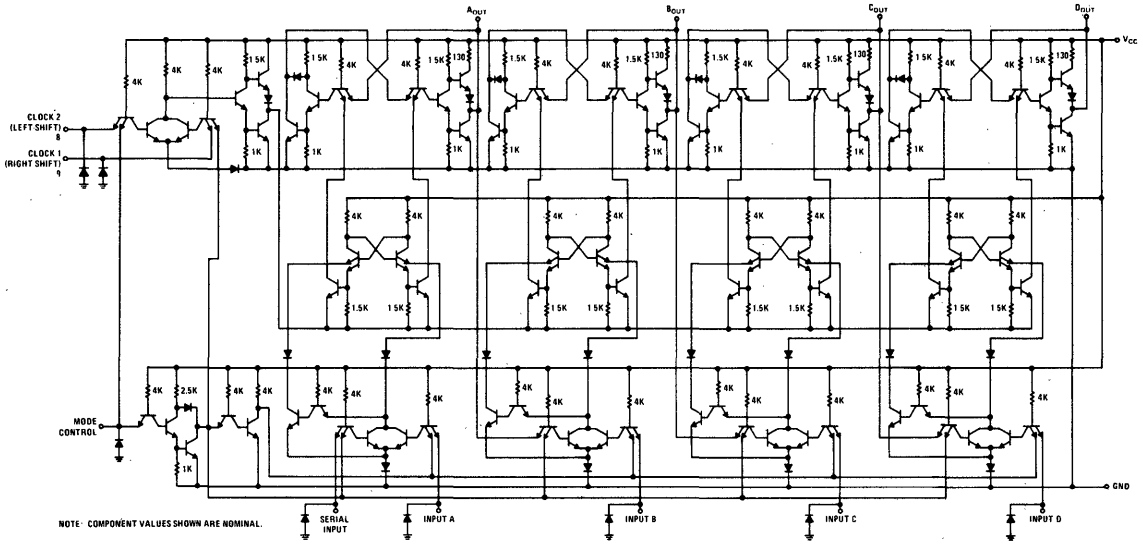
general description

The DM5495/DM7495 is a TTL (Transistor-Transistor Logic) monolithic four-bit parallel-in parallel-out shift register employing four R-S master-slave flip flops, internal clock buffers and control gating for either right-shift or left-shift operation. Separate clocks are provided for right-shift and left-shift operation. A mode control input enables right-shift or left-shift operation, depending on whether its input is a zero or one respectively. Data transfer occurs on the negative transition of the clock pulse. The three modes of operation are explained on page 4.

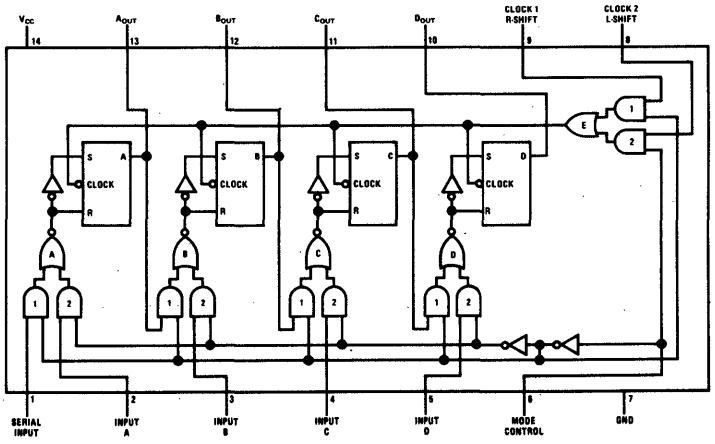
Features include:

- Input Clamping Diodes
- Typical Noise Immunity 1.0V
- High Clock Rate 35 MHz

schematic diagram



logic and connection diagram



POSITIVE LOGIC
MODE CONTROL = 0 FOR RIGHT SHIFT
MODE CONTROL = 1 FOR LEFT SHIFT OR PARALLEL LOAD

absolute maximum ratings

Supply Voltage		7V
Input Voltage		5.5V
Operating Temperature Range	DM5495	−55°C to +125°C
	DM7495	0°C to +70°C
Storage Temperature Range		−65°C to +150°C
Lead Temperature (Soldering, 10 sec)		300°C

electrical characteristics (Note 1)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	DM5495	V_{CC} = 4.5V	2			V
	DM7495	V_{CC} = 4.75V				
Logical "0" Input Voltage	DM5495	V_{CC} = 4.5V			0.8	V
	DM7495	V_{CC} = 4.75				
Logical "1" Output Voltage	DM5495	V_{CC} = 4.5V	2.4			V
	DM7495	V_{CC} = 4.75V, I_{load} = −400 μA				
Logical "0" Output Voltage	DM5495	V_{CC} = 4.5V			0.4	V
	DM7495	V_{CC} = 4.75V, I_{sink} = 16 mA				
Logical "0" Input Current (at any Input Except Mode Control)	DM5495	V_{CC} = 5.5V			−1.6	mA
	DM7495	V_{CC} = 5.25V, V_{IN} = 0.4V				
Logical "0" Input Current at Mode Control	DM5495	V_{CC} = 5.5V			−3.2	mA
	DM7495	V_{CC} = 5.25V, V_{IN} = 0.4V				
Logical "1" Input Current (at any Input Except Mode Control)	DM5495	V_{CC} = 5.5V			40	μA
	DM7495	V_{CC} = 5.25V, V_{IN} = 2.4V				
	DM5495	V_{CC} = 5.5V			1	mA
	DM7495	V_{CC} = 5.25V, V_{IN} = 5.5V				
Logical "1" Input Current at Mode Control	DM5495	V_{CC} = 5.5V			80	μA
	DM7495	V_{CC} = 5.25V, V_{IN} = 2.4V				
	DM5495	V_{CC} = 5.5V			1	mA
	DM7495	V_{CC} = 5.25V, V_{IN} = 5.5V				
Short-Circuit Output Current (Note 2)	DM5495	V_{CC} = 5.5V	−18		−57	mA
	DM7495	V_{CC} = 5.25V				
Supply Current	DM5495	V_{CC} = 5.5V		50	80	mA
	DM7495	V_{CC} = 5.25V				
Input Diode Clamp Voltage		T_A = 25°C, I_{IN} = −12 mA, V_{CC} = 5.0V			−1.5	V

switching characteristics

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Maximum Shift Frequency	C_L = 50 pF, R_L = 400Ω	20	35		MHz
Propagation Delay Time to Logical "1" Level from Clock 1 or 2 to Outputs	C_L = 50 pF, R_L = 400Ω		26	35	ns
Propagation Delay Time to Logical "0" from Clock 1 or 2 to Outputs	C_L = 50 pF, R_L = 400Ω		24	35	ns

Note 1: Min/Max limits apply across the guaranteed operating temperature range of −55°C to +125°C for the DM5495 and 0°C to 70°C for the DM7495 unless otherwise specified. All typicals are given for T_A = 25°C and V_{CC} = 5.0V.

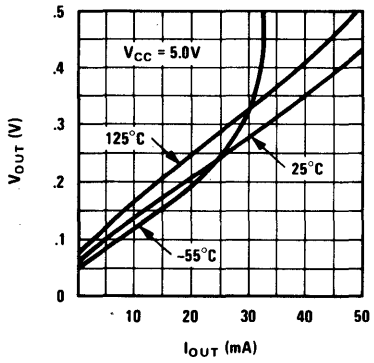
Note 2: Not more than one output should be shorted at a time.

recommended operating conditions

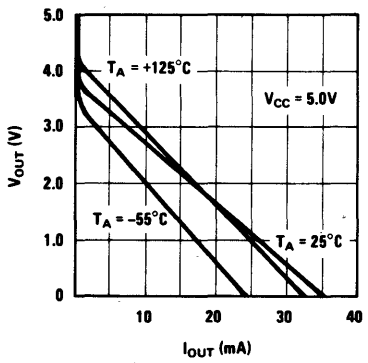
OPERATING CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage	DM5495	4.5	5	5.5	V
	DM7495	4.75	5	5.25	V
Clock Pulse Width, $t_{p\ (clock)}$		15	10		ns
Setup Time Required at Serial, A,B,C, or D Inputs, t_{setup}		20	10		ns
Hold Time Required at Serial, A,B,C, or D Inputs, t_{hold}		0	-10		ns
Logical "0" Level Setup Time Required at Mode Control $t_{A(0)}$ (With Respect to Clock 1 Input)		20			ns
Logical "1" Level Setup Time Required at Mode Control $t_{B(1)}$ (With Respect to Clock 2 Input)		15			ns
Logical "0" Level Setup Time Required at Mode Control $t_{C(0)}$ (With Respect to Clock 2 Input)		10			ns
Logical "1" Level Setup Time Required at Mode Control $t_{D(1)}$ (With Respect to Clock 1 Input)		10			ns

typical performance characteristics

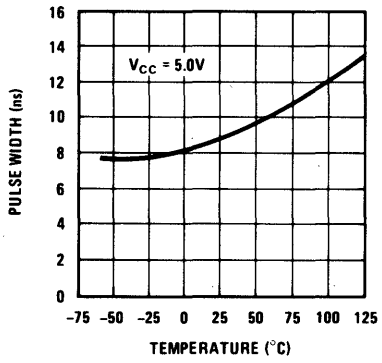
Logical "0" Output Voltage vs Sink Current



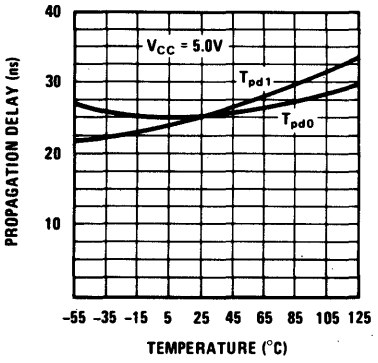
Logical "1" Output Voltage vs Source Current



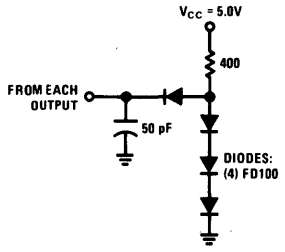
Minimum Clock Pulse Width vs Temperature



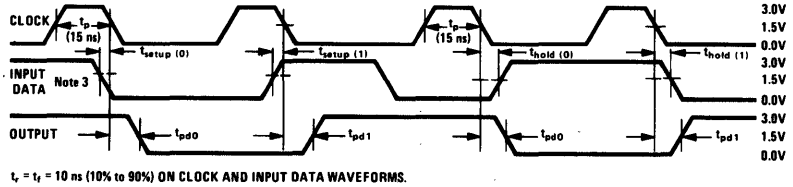
Propagation Delay Times vs Temperature



ac test circuit



switching time waveforms



$t_r = t_f = 10$ ns (10% to 90%) ON CLOCK AND INPUT DATA WAVEFORMS.

Note 3: Input data is applied to serial input when mode control equals a logical zero. Input data is applied to input A, B, C, or D, when mode control equals a logical one.

TTL MSI

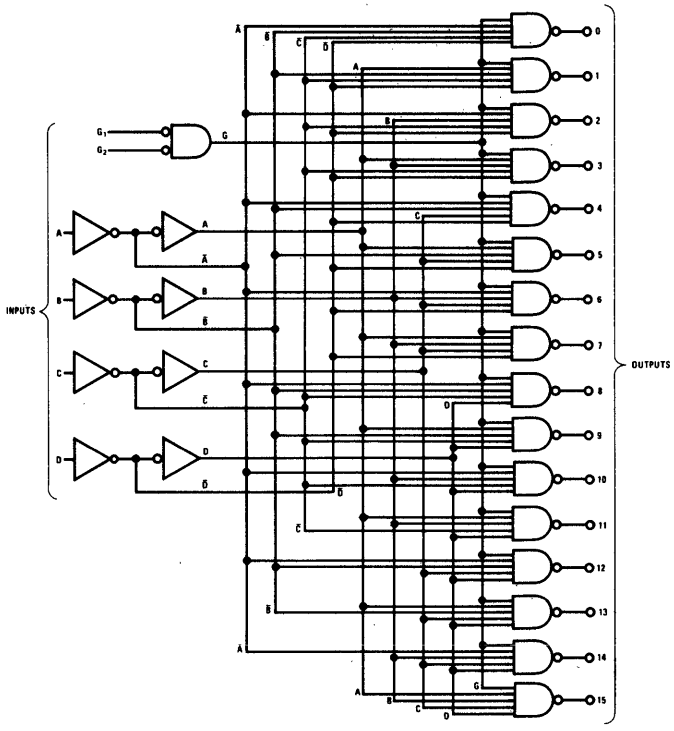
DM54154/DM74154 (SN54154/SN74154)
4-line-to-16-line decoder/demultiplexer

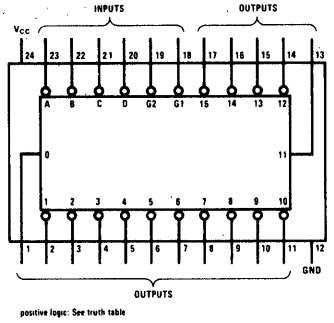
general description

The DM54154/DM74154 is a TTL monolithic 4-line-to-16-line decoder which allows decoding of a 4 bit binary coded input into one of 16 separate outputs. The device is provided with two strobe lines, both of which have to be in the low state in order to perform the decoding function; if either of the strobes is high, all 16 outputs will remain high. The device can be used as a demultiplexer by passing information from one of the strobes (the other being low) to an output selected by the 4 line input address. Other device features include:

- Equivalent to Fairchild's 9311-51/9311-59 and Texas Instruments' SN54154/SN74154
- All inputs contain clamp diodes
- Unit performs as a one line to 16 line demultiplexer
- Unit performs as a decoder of a 4 bit binary input to 1 of 16 outputs
- Typical propagation delay is 20 ns from inputs and 17 ns from strobe

logic and connection diagrams





positive logic: See truth table

truth table

INPUTS					OUTPUTS													
G1	G2	D	C	B	A	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	L	L	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	H	H	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H

X = "Don't Care" Condition

absolute maximum ratings

V_{CC}	7.0V
Input Voltage	5.5V
Operating Temperature Range	
DM54154	−55°C to +125°C
DM74154	0°C to 75°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

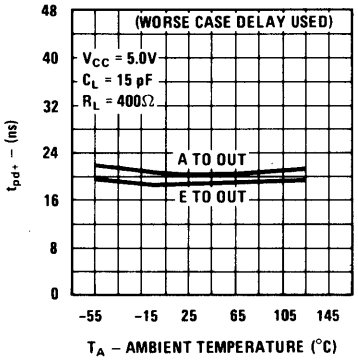
electrical characteristics (Note 1)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
Input Diode Clamp Voltage		V_{CC} = 5.0V, T_A = 25°C, I_{IN} = −12 mA			−1.5	V
Logical "1" Input Voltage	DM54154	V_{CC} = 4.5V	2.0			V
	DM74154	V_{CC} = 4.75V				
Logical "0" Input Voltage	DM54154	V_{CC} = 4.5V			0.8	V
	DM74154	V_{CC} = 4.75V				
Logical "1" Output Voltage	DM54154	V_{CC} = 4.5V	2.4	3.4		V
	DM74154	V_{CC} = 4.75V, I_{OUT} = −800 μA				
Logical "0" Output Voltage	DM54154	V_{CC} = 4.5V		0.25	0.4	V
	DM74154	V_{CC} = 4.75V, I_{OUT} = 16 mA				
Logical "1" Input Current	DM54154	V_{CC} = 5.5V			40	μA
	DM74154	V_{CC} = 5.25V, V_{IN} = 2.4V				
Logical "1" Input Current	DM54154	V_{CC} = 5.5V			1	mA
	DM74154	V_{CC} = 5.25V, V_{IN} = 5.5V				
Logical "0" Input Current	DM54154	V_{CC} = 5.5V			−1.6	mA
	DM74154	V_{CC} = 5.25V, V_{IN} = 0.4V				
Short Circuit Current	DM54154	V_{CC} = 5.5V	−20	−30	−55	mA
	DM74154	V_{CC} = 5.25V	−18		−57	mA
Supply Current	DM54154	V_{CC} = 5.5V		34	49	mA
	DM74154	V_{CC} = 5.25V		34	56	
Propagation Delay Time to Logical "1" from A,B,C or D		V_{CC} = 5.0V, C_L = 15 pF, R_L = 400Ω		18	36	ns
Propagation Delay Time to Logical "0" from A,B,C or D		V_{CC} = 5.0V, C_L = 15 pF, R_L = 400Ω		21	33	ns
Propagation Delay Time to Logical "1" from Strobe		V_{CC} = 5.0V, C_L = 15 pF, R_L = 400Ω		17	30	ns
Propagation Delay Time to Logical "0" from Strobe		V_{CC} = 5.0V, C_L = 15 pF, R_L = 400Ω		18	27	ns

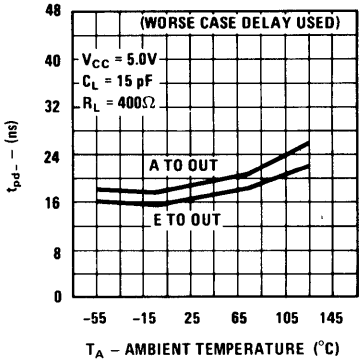
Note 1: Min/Max limits apply across the guaranteed temperature range unless otherwise specified. All typicals are given for V_{CC} = 5.0V and T_A = 25°C. Min/Max apply to absolute values.

typical performance characteristics

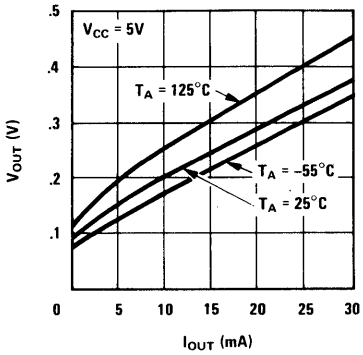
Propagation Delay to a Logical "0" (t_{pd0}) vs Temperature



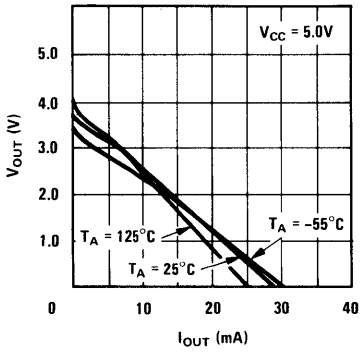
Propagation Delay to a Logical "1" (t_{pd1}) vs Temperature



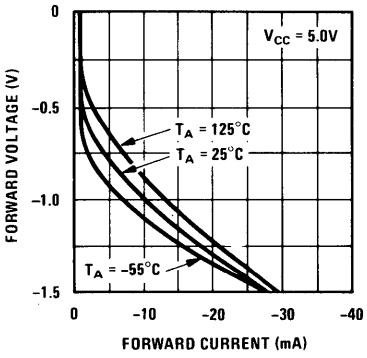
Logical "0" Output Voltage vs Sink Current



Logical "1" Output Voltage vs Source Current

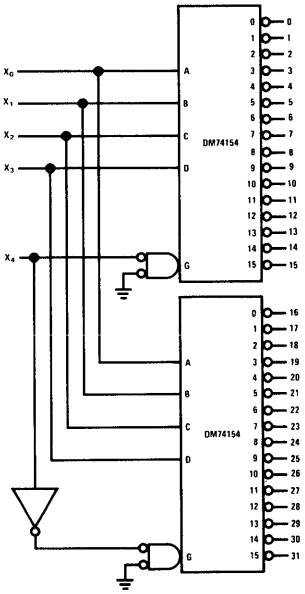


Input Clamp Diode

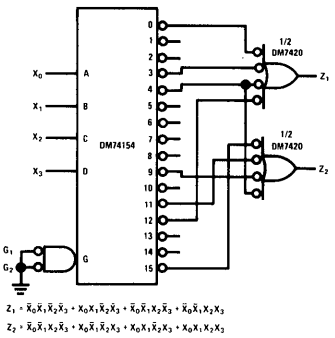


typical applications

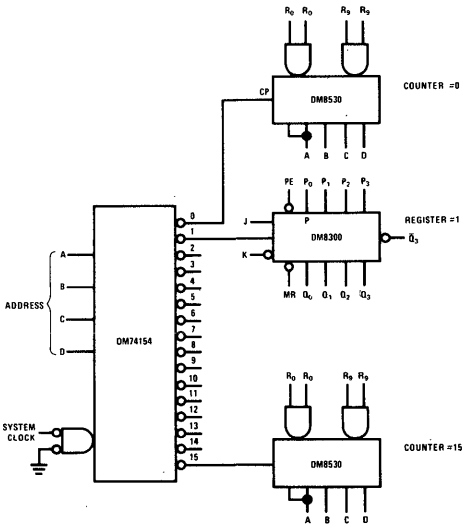
DM74154 Expanded to Perform 1 Out of 32 Decode Function



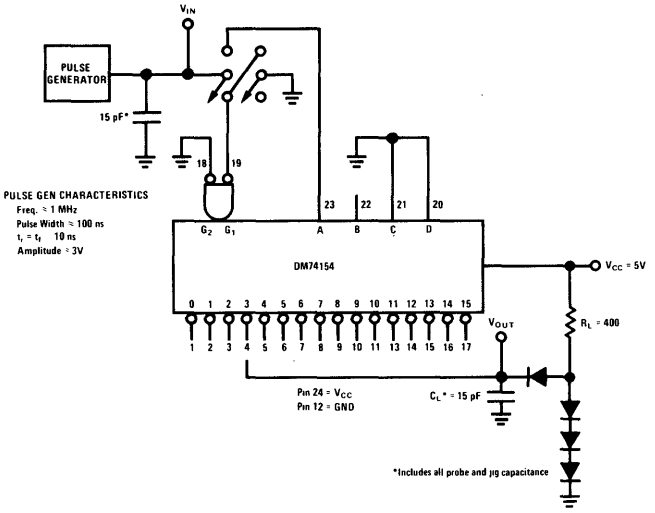
DM74154 Used as a Minterm Generator



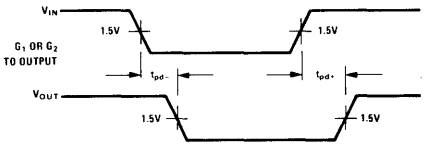
Demultiplexing System Clock

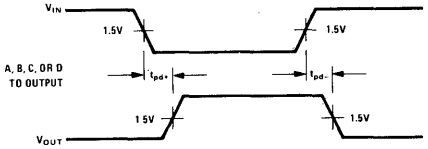


ac test circuit



switching time waveforms





TTL MSI

DM7200/DM8200 four bit comparator

general description

The DM7200/DM8200 is a monolithic TTL (Transistor-Transistor Logic) circuit which is used to compare the numerical values of two four-bit binary numbers. Outputs indicate (1) whether number A is greater than number B, (2) whether number B is greater than number A, or (3) whether the two numbers are equal. A strobe input overrides all other inputs and places the outputs in a definite state. The design chosen provides maximum speed with minimum circuit complexity. Numerical comparisons of words longer than four bits may be made by using additional DM7200/DM8200's only.

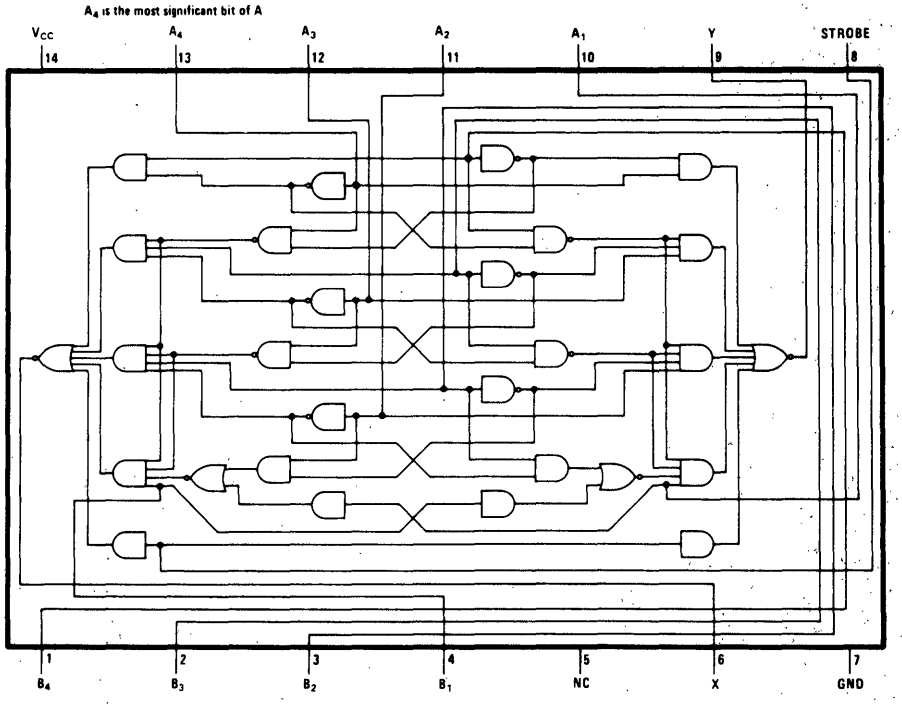
Features Include:

- Series 54/74 Compatible
- Typical Noise Immunity 1V
- Guaranteed Noise Immunity 400 mV
- Typical Propagation Delay 20 ns
- Typical Power Dissipation 175 mW

The DM7200/DM8200 has applications in:

- Digital stepping-motor control applications
- Convergence applications
- Summing junction for digital servo systems

logic and connection diagram



logic table

Input				Output	
Number $A_4A_3A_2A_1$		Number $B_4B_3B_2B_1$	Strobe	X	Y
A	>	B	0	1	0
A	<	B	0	0	1
A	=	B	0	1	1
A	≠	B	1	0	0

absolute maximum ratings

Supply Voltage		7V
Input Voltage		5.5V
Operating Temperature Range	DM7200	−55°C to +125°C
	DM8200	0°C to +70°C
Storage Temperature Range		−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)		300°C

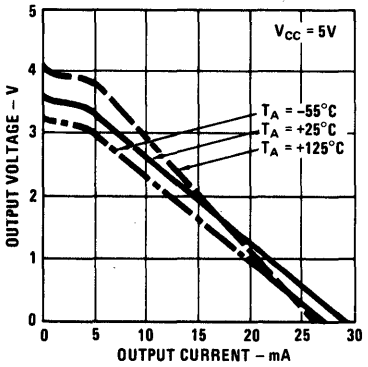
electrical characteristics (Note 1)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	DM7200	V_{CC} = 4.5V		2.0			V
	DM8200	V_{CC} = 4.75V					
Logical "0" Input Voltage	DM7200	V_{CC} = 4.5V				.8	V
	DM8200	V_{CC} = 4.75V					
Logical "1" Output Voltage	DM7200	V_{CC} = 4.5V	I_{OUT} = −400 μA	2.4			V
	DM8200	V_{CC} = 4.75V					
Logical "0" Output Voltage	DM7200	V_{CC} = 4.5V	I_{OUT} = 16 mA			.4	V
	DM8200	V_{CC} = 4.75V					
Logical "1" Input Current	DM7200	V_{CC} = 5.5V	V_{IN} = 2.4V			80	μA
	DM8200	V_{CC} = 5.25V					
Logical "0" Input Current	DM7200	V_{CC} = 5.5V	V_{IN} = 0.4V			−3.2	mA
	DM8200	V_{CC} = 5.25V					
Logical "1" Input Current	DM7200	V_{CC} = 5.5V	V_{IN} = 5.5V			1	mA
	DM8200	V_{CC} = 5.25V					
Output Short Circuit Current (Note 2)	DM7200	V_{CC} = 5.5V		−20		−55	mA
	DM8200	V_{CC} = 5.25V		−18		−55	
Supply Current	DM7200	V_{CC} = 5.5V			35	53	mA
	DM8200	V_{CC} = 5.25V					
Propagation Delay to a Logical "1" from Any Data Input to Output $t_{pd\,1}$		V_{CC} = 5.0V, T_A = 25°C			24	40	ns
Propagation Delay to a Logical "0" from Any Data Input to Output $t_{pd\,0}$		V_{CC} = 5.0V, T_A = 25°C			17	30	ns
Propagation Delay to a Logical "1" from Strobe Input to Output $t_{pd\,1}$		V_{CC} = 5.0V, T_A = 25°C			15	27	ns
Propagation Delay to a Logical "0" from Strobe Input to Output $t_{pd\,0}$		V_{CC} = 5.0V, T_A = 25°C			8	18	ns
Time Prior to Removal of Strobe that Data Inputs Must Be Stabilized; $t_{SET\ UP}$		V_{CC} = 5.0V, T_A = 25°C			0	10	ns
Time After Activation of Strobe that Data Inputs Must be Held; t_{HOLD}		V_{CC} = 5.0V, T_A = 25°C			−10	0	ns

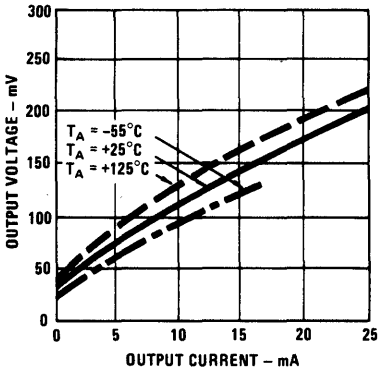
Note 1: Unless otherwise specified, limits shown apply from −55°C to +125°C for the DM7200 and 0°C to +70°C for the DM8200. Typical values apply to supply voltages of 5.0V.
Note 2: Only one output should be shorted at a time.

typical output characteristics

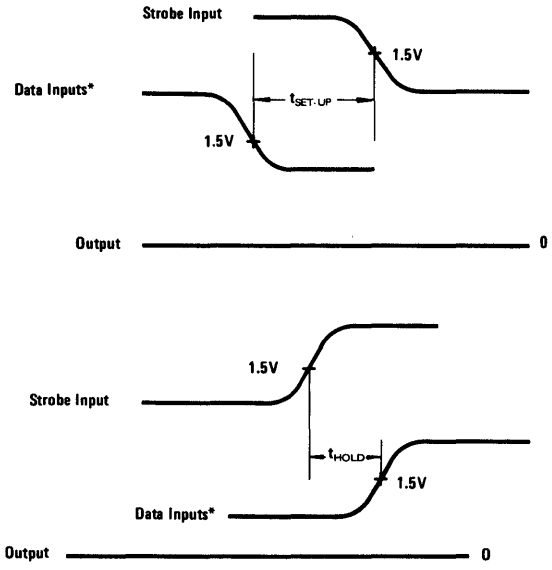
Logic "1" Output Voltage vs Source Current



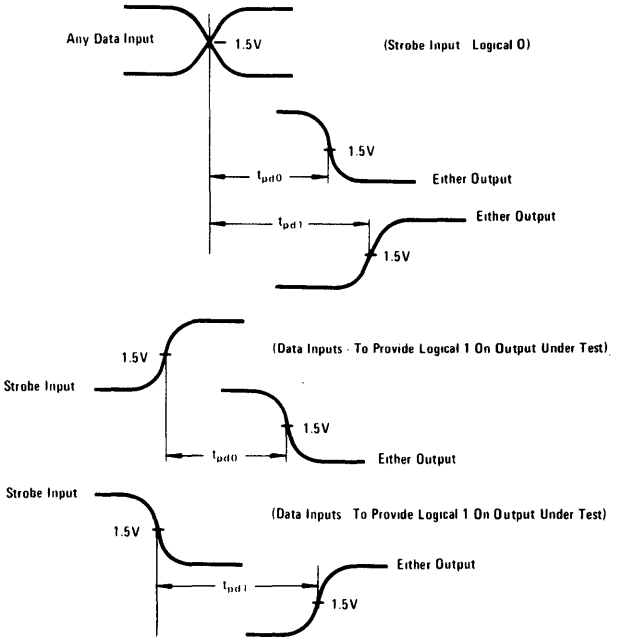
Logic "0" Output Voltage vs Sink Current



data input waveforms

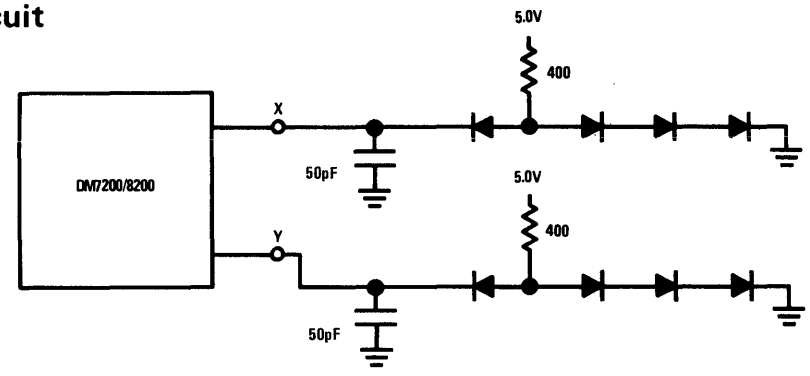


switching time waveforms



*The Data Input waveforms shown may not necessarily represent the actual direction of the transition for a particular Data Input pin. The transitions shown indicate also what an Output would do if it weren't for the Strobe input. In all cases the worst case input-to-output path is specified regardless of the transitions shown.

ac test circuit



DIODES: FD100

DM7210/DM8210 eight channel digital switch
DM7211/DM8211 eight channel digital switch

general description

The DM7210/DM8210 and DM7211/DM8211 are digital bipolar integrated circuits employing TTL, used to multiplex eight INPUT channels to a single OUTPUT. Depending upon the 3-bit binary number applied to the SELECT lines, the digital bit on the unique INPUT selected appears on the output.

The DM7211/DM8211 provides a strobe input which when taken to a logical "1" level places the output in the logical "1" state.

The circuit can also be used to convert parallel input information to serial output information. If eight bits of parallel information are applied to the inputs, and if the binary numbers 000 through 111 are sequenced on the select lines, the output will provide a serial presentation of the input bits. Key features include:

- TTL Circuitry
- Input Clamping Diodes
- 1 Volt Typical Noise Immunity
- 400 mV Guaranteed Noise Immunity

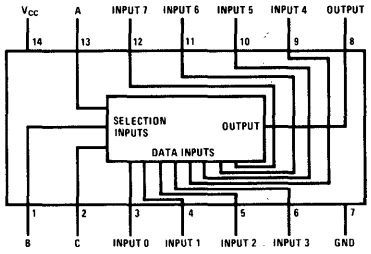
The devices are completely compatible with Series 54/74 circuits.

logic table

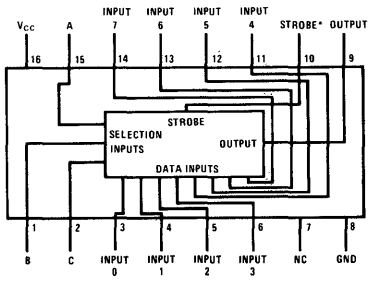
SELECTION INPUTS C	B	A	STROBE (DM7211/DM8211 ONLY)	DATA INPUTS 0	1	2	3	4	5	6	7	OUTPUT
0	0	0	0	0	X	X	X	X	X	X	X	0
0	0	0	0	1	X	X	X	X	X	X	X	1
0	0	1	0	X	0	X	X	X	X	X	X	0
0	0	1	0	X	1	X	X	X	X	X	X	1
0	1	0	0	X	X	0	X	X	X	X	X	0
0	1	0	0	X	X	1	X	X	X	X	X	1
0	1	1	0	X	X	X	0	X	X	X	X	0
0	1	1	0	X	X	X	1	X	X	X	X	1
1	0	0	0	X	X	X	X	0	X	X	X	0
1	0	0	0	X	X	X	X	1	X	X	X	1
1	0	1	0	X	X	X	X	X	0	X	X	0
1	0	1	0	X	X	X	X	X	1	X	X	1
1	1	0	0	X	X	X	X	X	X	0	X	0
1	1	0	0	X	X	X	X	X	X	1	X	1
1	1	1	0	X	X	X	X	X	X	X	0	0
1	1	1	0	X	X	X	X	X	X	X	1	1
X	X	X	1	X	X	X	X	X	X	X	X	1

X = "Don't Care" Condition

connection diagrams



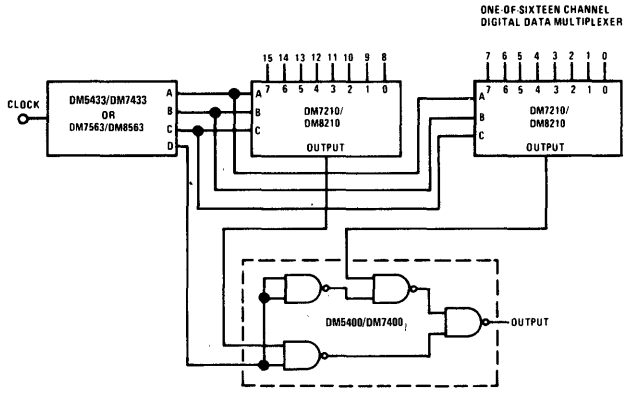
DM7210/DM8210



*A Logical 1 on the strobe input causes the output to go the Logical 1 state.
A Logical 0 on the strobe input allows information to be routed through the device.

DM7211/DM8211

typical application



absolute maximum ratings

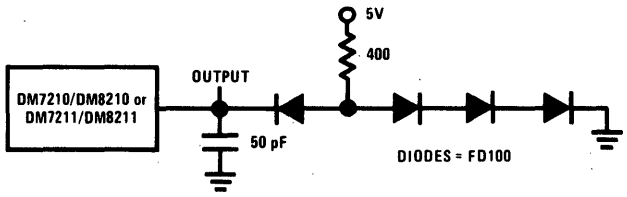
Supply Voltage		7V
Input Voltage		5.5V
Fanout		10
Storage Temperature Range		−65°C to +150°C
Operating Temperature Range	DM7210, DM7211	−55°C to +125°C
	DM8210, DM8211	0°C to +70°C
Lead Temperature (soldering, 10 sec)		300°C

electrical characteristics (Note 1)

PARAMETER		CONDITION	MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	DM7210/DM7211	V_{CC} = 4.5V	2.0			V
	DM8210/DM8211	V_{CC} = 4.75V				
Logical "0" Input Voltage	DM7210/DM7211	V_{CC} = 4.5V			0.8	V
	DM8210/DM8211	V_{CC} = 4.75V				
Logical "1" Output Voltage	DM7210/DM7211	V_{CC} = 4.5V, I_{OUT} = −400 μA	2.4			V
	DM8210/DM8211	V_{CC} = 4.75V				
Logical "0" Output Voltage	DM7210/DM7211	V_{CC} = 4.5V, I_{OUT} = 16 mA			0.4	V
	DM8210/DM8211	V_{CC} = 4.75V				
Logical "1" Input Current (All Inputs)	DM7210/DM7211	V_{CC} = 5.5V, V_{IN} = 2.4V			40	μA
	DM8210/DM8211	V_{CC} = 5.25V				
Logical "1" Input Current (All Inputs)	DM7210/DM7211	V_{CC} = 5.5V, V_{IN} = 5.5V			1	mA
	DM8210/DM8211	V_{CC} = 5.25V				
Logical "0" Input Current (All Inputs)	DM7210/DM7211	V_{CC} = 5.5V, V_{IN} = 0.4V		-1.0	-1.6	mA
	DM8210/DM8211	V_{CC} = 5.25V				
Input Clamp Diode (All Inputs)	DM7210/DM7211	V_{CC} = 5.5V, I_{IN} = −12 mA, T_A = 25°C		-1.0	-1.5	V
	DM8210/DM8211	V_{CC} = 5.25V				
Output Short Circuit Current	DM7210/DM7211	V_{CC} = 5.5V, V_{OUT} = 0	−20		-55	mA
	DM8210/DM8211	V_{CC} = 5.25V	−18			
Power Supply Current (All Inputs GND)	DM7210/DM7211	V_{CC} = 5.5V		20	33	mA
	DM8210/DM8211	V_{CC} = 5.25V				
Propagation Delay to a Logical "0" From Data Input to Output, t_{pd0}		V_{CC} = 5.0V, T_A = 25°C	10	21	30	ns
Propagation Delay to a Logical "0" From Strobe Input to Output		V_{CC} = 5.0V, T_A = 25°C	10	19	27	ns
Propagation Delay to a Logical "1" From Data Input to Output, t_{pd1}		V_{CC} = 5.0V, T_A = 25°C	10	23	32	ns
Propagation Delay to a Logical "1" From Strobe Input to Output		V_{CC} = 5.0V, T_A = 25°C	10	21	30	ns
Data Selection Settling Time From 0→1 Transition on A, B, C (t_{s1})		V_{CC} = 5.0V, T_A = 25°C	15	31	43	ns
Data Selection Settling Time From 1→0 Transition on A, B, C (t_{s0})		V_{CC} = 5.0V, T_A = 25°C	15	31	42	ns

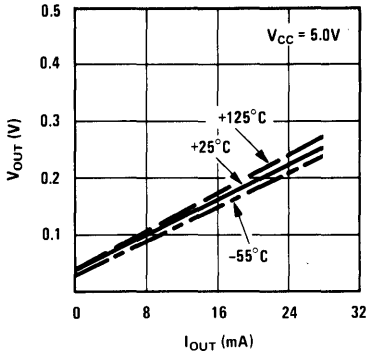
Note 1: Unless otherwise specified the min-max limits apply across the −55°C to +125°C temperature range for the DM7210 and DM7211 and across the 0°C to 70°C temperature range for the DM8210 and DM8211. Typicals are given for V_{CC} = 5.0V and 25°C.

ac test circuit

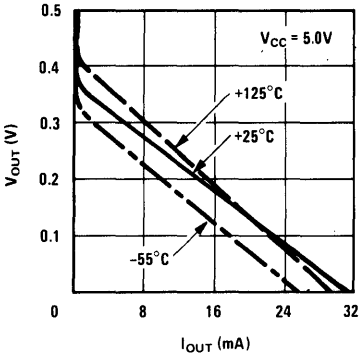


typical performance characteristics

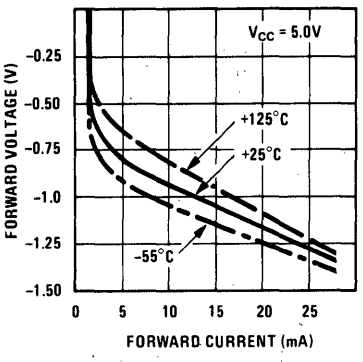
Logical "0" Output Voltage vs Sink Current



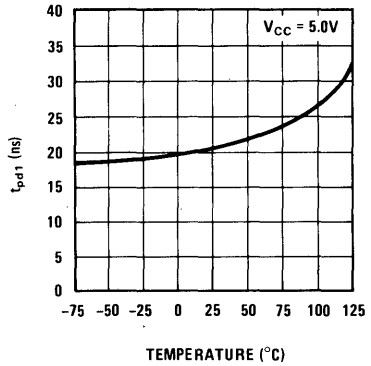
Logical "1" Output Voltage vs Source Current



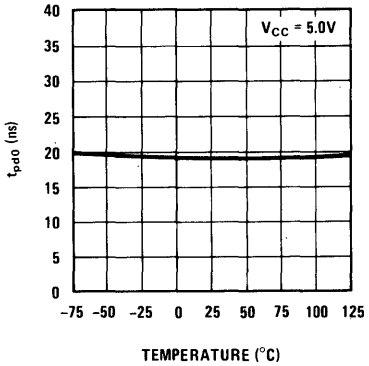
Input Clamp Diode Characteristics



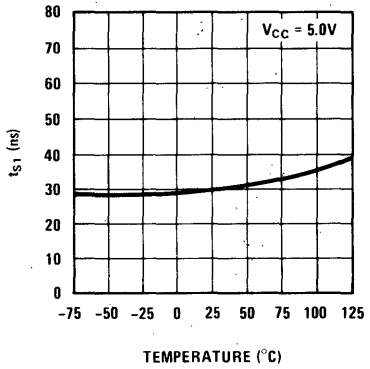
Transition Time to a Logical "1" from Strobe Input to Output, (t_{pd1}) vs Temperature – DM7211/DM8211



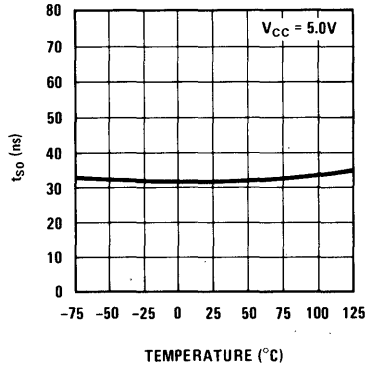
Transition Time to a Logical "0" from Strobe Input to Output, (t_{pd0}) vs Temperature– DM7211/DM8211



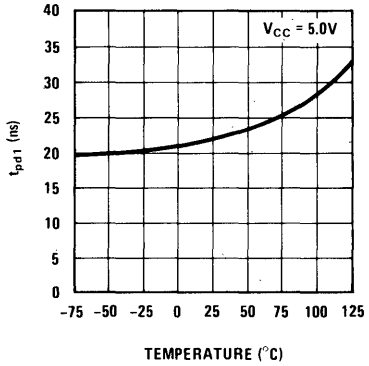
Data Selection Settling Time vs Temperature Logical "0" to Logical "1" Transition on Inputs A, B, C (t_{S1})



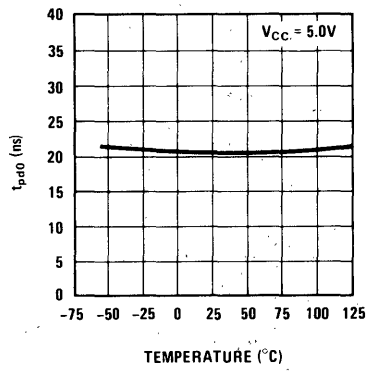
Data Selection Settling Time vs Temperature Logical "1" to Logical "0" Transition on Inputs A, B, C (t_{S0})



Transition Time to a Logical "1" from Data (Channel) Inputs to Output, (t_{pd1}) vs Temperature

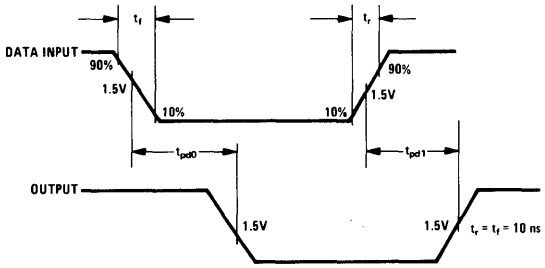


Transition Time to a Logical "0" from Data (Channel) Inputs to Output, (t_{pd0}) vs Temperature



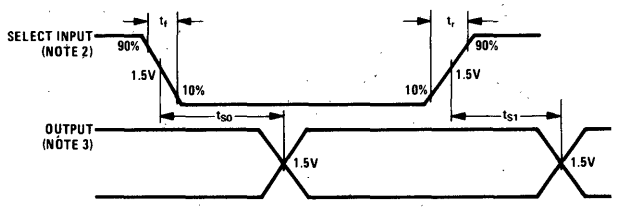
switching time waveforms

1. Propagation Delays From Data Inputs to Output



Set Inputs A, B, C such that tested input is routed to the output.

2. Settling Times From Change of A, B, or C to Correct Data Out



Data Inputs: Connected in any logic configuration.

Note 2: When the select inputs are taken to opposite logical levels simultaneously, the one (ones) making the Logical "1" to Logical "0" transition provide the worst-case path.
Note 3: Transition times specified are independent of the direction of the output waveform.

TTL MSI

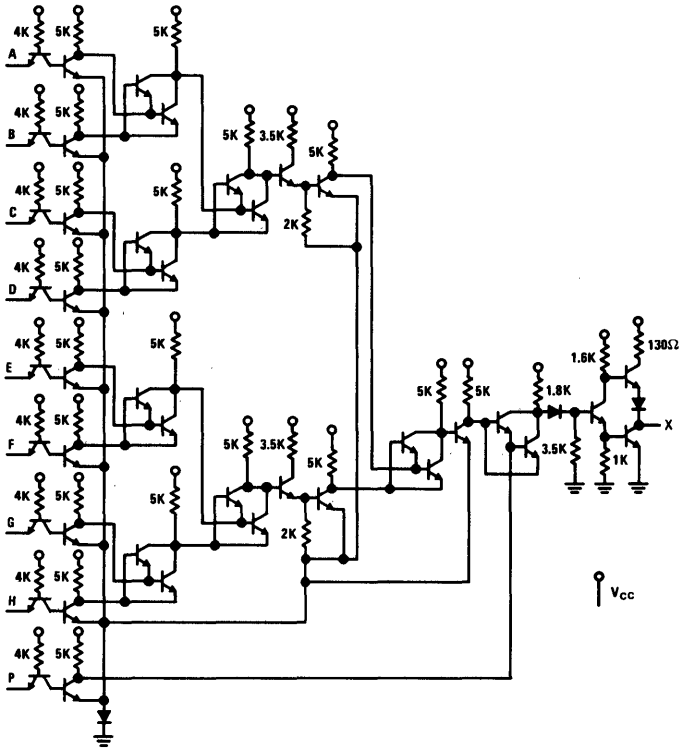
DM7220/DM8220 parity generator and checker

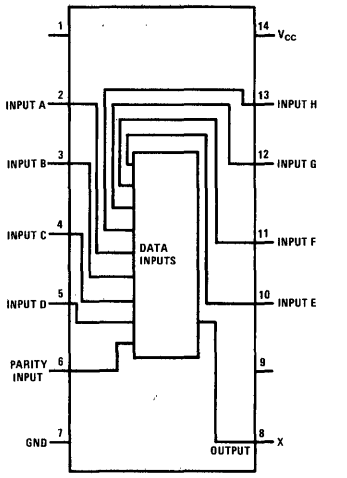
general description

The DM7220/DM8220 is a monolithic integrated circuit which can be used to both generate a parity bit and check for parity. Nine inputs and a single output are provided. When it is desired to generate a parity bit, eight of the nine inputs are connected to the eight data transmission lines. Depending upon whether odd parity or even parity is desired a logical 1 or a logical 0 is applied to the ninth input. For a parity check, the output of the parity generator (sending end) is connected to the ninth input of the parity checker (receiver end). The resulting output of the parity checker will remain in one particular logic state unless a bit is "lost" during transmission.

The device is fully compatible with other Series 54/74 circuits.

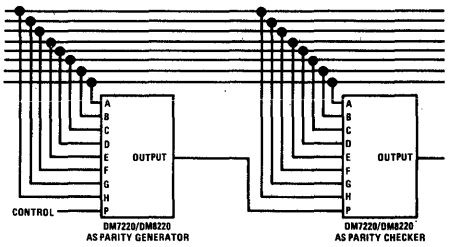
schematic and connection diagrams





$X = A \oplus B \oplus C \oplus D \oplus E \oplus F \oplus G \oplus H \oplus \overline{P}$

typical applications



If the control line is a logical "0" the parity generator will generate odd parity. The parity checker will acknowledge the presence of an odd number of "1"'s (odd parity) with a logical "0" on its output.

If the control line is a logical "1" the parity generator will generate even parity. The parity checker will acknowledge the presence of an even number of "1"'s (even parity) with a logical "1" on its output.

absolute maximum ratings

Supply Voltage		7V
Input Voltage		5.5V
Fan Out		10
Storage Temperature Range		−65°C to +150°C
Operating Temperature Range	DM7220	−55°C to +125°C
	DM8220	0°C to +70°C
Lead Temperature (Soldering, 10 sec.)		300°C

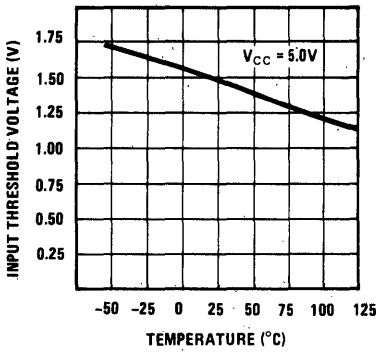
electrical characteristics (Note 1)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	DM7220	V_{CC} = 4.5V		2.0			V
	DM8220	V_{CC} = 4.75V					
Logical "0" Input Voltage	DM7220	V_{CC} = 4.5V				0.8	V
	DM8220	V_{CC} = 4.75V					
Logical "1" Output Voltage	DM7220	V_{CC} = 4.5V	I_{OUT} = −400 μA	2.4			V
	DM8220	V_{CC} = 4.75V					
Logical "0" Output Voltage	DM7220	V_{CC} = 4.5V	I_{OUT} = 16 mA			0.4	V
	DM8220	V_{CC} = 4.75V					
Logical "1" Input Current	DM7220	V_{CC} = 5.5V	V_{IN} = 2.4V			40	μA
	DM8220	V_{CC} = 5.25V					
Input Diode Clamp Voltage	DM7220	V_{CC} = 5.5V	I_{IN} = −12 mA		−1.1	−1.5	V
	DM8220	V_{CC} = 5.25V	T_A = 25°C				
Logical "1" Input Current	DM7220	V_{CC} = 5.5V	V_{IN} = 5.5V			1.0	mA
	DM8220	V_{CC} = 5.25V					
Logical "0" Input Current	DM7220	V_{CC} = 5.5V	V_{IN} = 0.4V		−1.0	−1.6	mA
	DM8220	V_{CC} = 5.25V					
Output Short Circuit Current	DM7220	V_{CC} = 5.5V	V_{OUT} = 0V	20		55	mA
	DM8220	V_{CC} = 5.25V		18			
Power Supply Current	DM7220	V_{CC} = 5.5V			26	35	mA
	DM8220	V_{CC} = 5.25V					
Propagation Delay to Logical "1", t_{pd1} Inputs A, B, C, D, E, F, G, H		V_{CC} = 5.0V, C_O = 50 pF	T_A = 25°C, F.O. = 10	15	36	58	ns
Propagation Delay to Logical "0", t_{pd0} Inputs A, B, C, D, E, F, G, H		V_{CC} = 5.0V, C_O = 50 pF	T_A = 25°C, F.O. = 10	11	32	52	ns
Propagation Delay to Logical "1", t_{pd1} Input P		V_{CC} = 5.0V, C_O = 50 pF	T_A = 25°C, F.O. = 10	8	21	35	ns
Propagation Delay to Logical "0", t_{pd0} Input P		V_{CC} = 5.0V, C_O = 50 pF	T_A = 25°C, F.O. = 10	7	14	25	ns

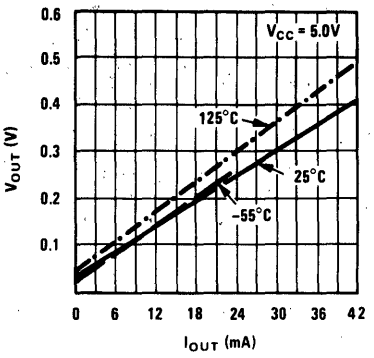
Note 1: Unless otherwise specified the min-max limits apply across the −55°C to +125°C temperature range for the DM7220 and across the 0°C to 70°C temperature range for the DM8220. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

typical performance characteristics

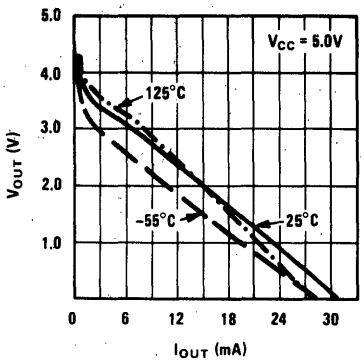
Threshold Voltage vs Temperature



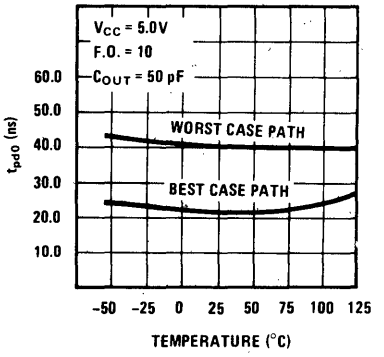
Logical "0" Output Voltage vs Sink Current



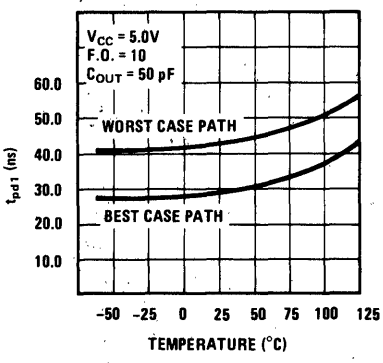
Logical "1" Output Voltage vs Source Current



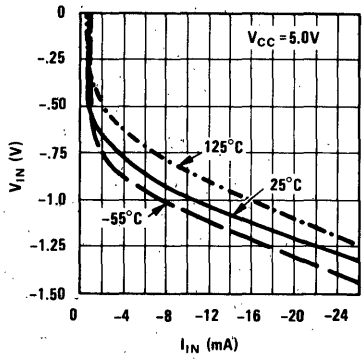
Transition Time to a Logical "0" vs Temperature (Inputs A, B, C, D, E, F, G, H to Output)



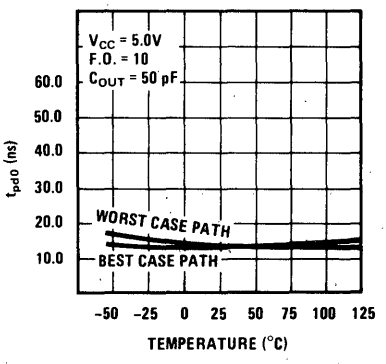
Transition Time to a Logical "1" vs Temperature (Inputs A, B, C, D, E, F, G, H to Output)



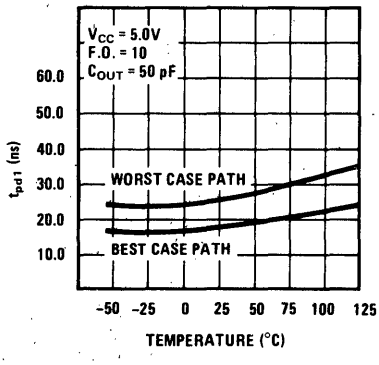
Input Clamp Diode Characteristics



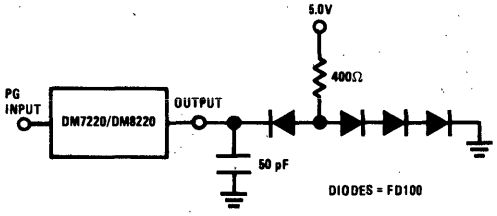
Transition Time to a Logical "0" vs Temperature (Input P to Output)



Transition Time to a Logical "1" vs Temperature (Input P to Output)

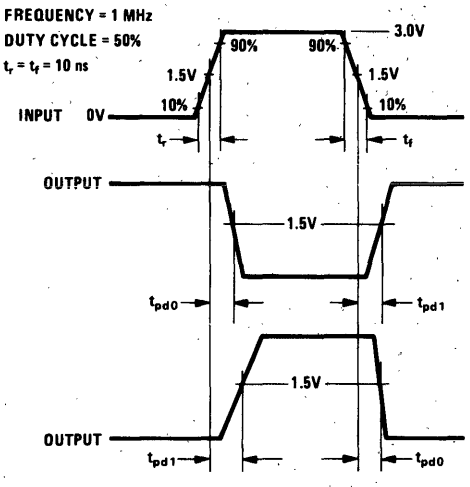


ac test circuit



timing requirements

FREQUENCY = 1 MHz
DUTY CYCLE = 50%
$t_r = t_f = 10$ ns



TTL MSI

DM7520/DM8520 modulo-n divider

general description

The DM7520/DM8520 combines TTL technology and MSI (Medium Scale Integration) design to provide a circuit equal in complexity to more than 50 gates.

Although extremely versatile in a number of digital applications, its primary usage will be realized in two areas:

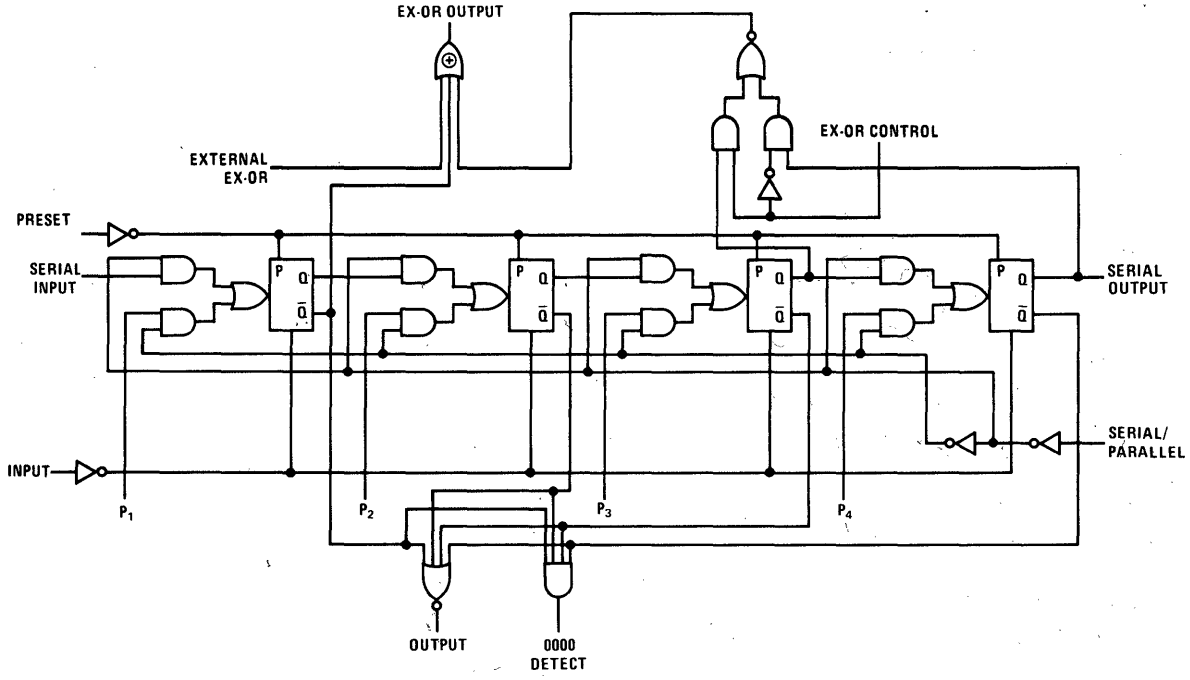
1. MODULO-N DIVIDER

A single DM7520/DM8520 can be programmed without external components to divide by any number from 2 to 15. Cascading of these dividers will provide division by any number from 2 to very large numbers.

2. SHIFT REGISTER

Since the basic organization of the logic is that of a serial shift register, the device may be used where four-bit parallel-in-serial out shifting is required.

logic diagram



connection diagram

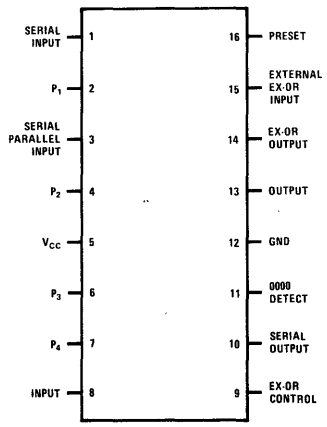


table for division by n

SETTING P_1	P_2	P_3	P_4	÷BY
1	1	1	0	2
1	1	0	0	3
1	0	0	0	4
0	0	0	1	5
0	0	1	0	6
0	1	0	0	7
1	0	0	1	8
0	0	1	1	9
0	1	1	0	10
1	1	0	1	11
1	0	1	0	12
0	1	0	1	13
1	0	1	1	14
0	1	1	1	15

absolute maximum ratings

Supply Voltage		7V
Input Voltage		5.5V
Operating Temperature Range	DM7520	−55°C to +125°C
	DM8520	0°C to +70°C
Storage Temperature Range		−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)		300°C

electrical characteristics (Note 1)

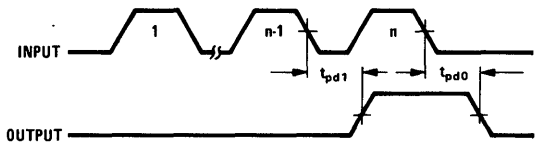
PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	DM7520	V_{CC} = 4.5V		2.0			V
	DM8520	V_{CC} = 4.75V					
Logical "0" Input Voltage	DM7520	V_{CC} = 4.5V				0.8	V
	DM8520	V_{CC} = 4.75V					
Logical "1" Output Voltage	DM7520	V_{CC} = 4.5V	I_{OUT} = −400 μA	2.4			V
	DM8520	V_{CC} = 4.75V					
Logical "0" Output Voltage	DM7520	V_{CC} = 4.5V	I_{OUT} = 16 mA			0.4	V
	DM8520	V_{CC} = 4.75V					
Logical "0" Input Current (All inputs except pin 9)	DM7520	V_{CC} = 5.5V	V_{IN} = 0.4V			1.6	mA
	DM8520	V_{CC} = 5.25V					
Logical "0" Input Current (Pin 9)	DM7520	V_{CC} = 5.5V	V_{IN} = 0.4V			3.2	μA
	DM8520	V_{CC} = 5.25V					
Logical "1" Input Current	DM7520	V_{CC} = 5.5V	V_{IN} = 2.4V			40	μA
	DM8520	V_{CC} = 5.25V					
Logical "1" Input Current (Pin 9)	DM7520	V_{CC} = 5.5V	V_{IN} = 2.4V			80	μA
	DM8520	V_{CC} = 5.25V					
Logical "1" Input Current (All inputs except pin 9)	DM7520	V_{CC} = 5.5V	V_{IN} = 5.5V			1	mA
	DM8520	V_{CC} = 5.25V					
Output Short Circuit Current (Note 3)	DM7520	V_{CC} = 5.5V	V_{OUT} = 0V (Note 2)	−20		55	mA
	DM8520	V_{CC} = 5.25V		−18			
Power Supply Current		V_{CC} = 5.0V	T_A = 25°C		50		mA
Counting Frequency		V_{CC} = 5.0V	T_A = 25°C		20		MHz

Note 1: Unless otherwise specified, limits shown apply across the −55°C to +125°C temperature range for the DM7520 and the 0°C to +70°C temperature range for the DM8520. Typical values apply to supply voltages of 5.0V.

Note 2: Only one output should be shorted at a time.

Note 3: Serial and exclusive OR outputs.

switching time waveforms



theory of operation

The basic operation of the DM7520/DM8520 is derived from the fact that when several outputs of a shift register are EXCLUSIVE OR'ed and the result fed back to the register's input, a unique progression of stable states results on the outputs of the flip-flops. Depending upon which outputs are EXCLUSIVE OR'ed the number of different states can be varied. Even if optimum gating is provided the most states which can be obtained is 2^n-1, where n is equal to the number of flip-flops in the register. The all-zero state is precluded; and, therefore, the maximum number of states is always one less than the theoretical maximum number. Since the DM7520/DM8520 contains four flip-flops, its maximum number of states is 15. Because the 1111 state occurs only once during a 15-state sequence, this state is detected; and its output becomes the output of the divider.

To obtain frequency division by numbers other than the maximum, it is necessary to cause the register to "jump" immediately from its initial 1111 to the state which it would normally reach in 16-m (m = desired frequency division) pulses. For example, to divide by eleven it would be necessary to jump to the fifth state and then simply allow the register to normally progress forward to its original state. The output of the divider is also used as a control pulse. Since the 1111 state is detected and since the "jump-state" information is of interest only at the time that this state is reached, the OUTPUT is used to gate the parallel inputs, through the SERIAL/PARALLEL input, so that it recognizes this "jump-state" information only at this time. Subsequently as the states change, the parallel input information is locked from the divider.

Should the divider ever be accidently set in the forbidden 0000 state, an output is provided to detect this state. If this output is in turn fed into the EXTERNAL EX-OR input, a 1 will be forced into the register at the next clock pulse, thus clearing the unallowed state.

A PRESET input is provided which when taken to a logical "1" level overrides all other inputs and sets the register to the 1111 state.

To divide by numbers greater than 15, it is necessary to cascade DM7520/DM8520's. Both the OUTPUT and the 0000 DETECT output are capable of being connected directly to other like outputs thus providing the "WIRED-OR" configuration. These outputs should be connected to the similar outputs on other dividers for proper operation. All SERIAL/PARALLEL inputs should be connected to the common OUTPUT.

Other connections are shown. (Figure 1 indicates connections for 2 dividers or a maximum frequency division of 255. For division by higher numbers, a more complete discussion of the interconnection techniques will be given in the final data sheet.)

To divide by numbers between 16 and 255, the table in Figure 2 will apply.

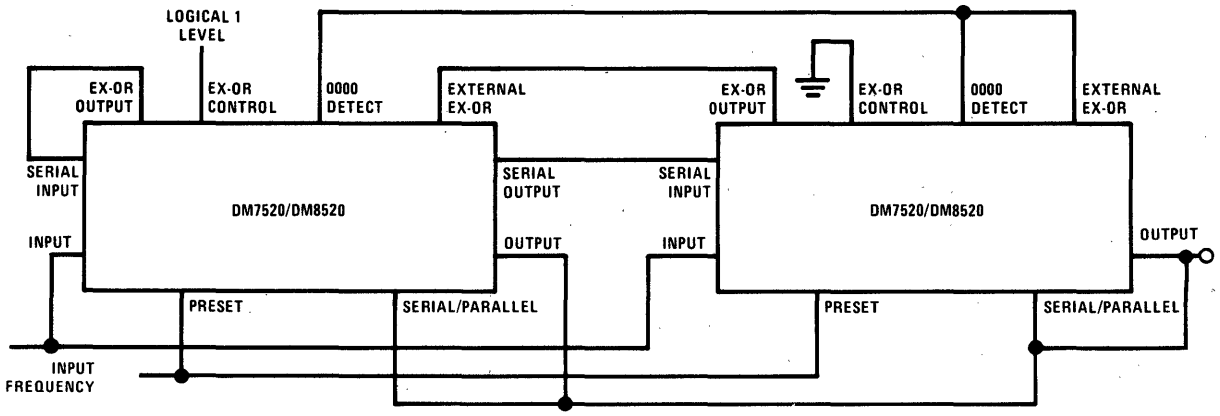


FIGURE 1. Connection for 2 Divider or Maximum Frequency Division of 255

SETTING								÷ BY
DIVIDER 1				DIVIDER 2				
P_1	P_2	P_3	P_4	P_1	P_2	P_3	P_4	
0	1	1	1	1	1	1	1	255
1	0	1	1	1	1	1	1	254
0	1	0	1	1	1	1	1	253
0	0	1	0	1	1	1	1	252
1	0	0	1	0	1	1	1	251
0	1	0	0	1	0	1	1	250
0	0	1	0	0	1	0	1	249
0	0	0	1	0	0	1	0	248
0	0	0	0	1	0	0	1	247
0	0	0	0	0	1	0	0	246
0	0	0	0	0	0	1	0	245
0	0	0	0	0	0	0	1	244
1	0	0	0	0	0	0	0	243
1	1	0	0	0	0	0	0	242
1	1	1	0	0	0	0	0	241
0	1	1	1	0	0	0	0	240
1	0	1	1	1	0	0	0	239
1	1	0	1	1	1	0	0	238
0	1	1	0	1	1	1	0	237
0	0	1	1	0	1	1	1	236
0	0	0	1	1	0	1	1	235
0	0	0	0	1	1	0	1	234
0	0	0	0	0	1	1	0	233
0	0	0	0	0	0	1	1	232
1	0	0	0	0	0	0	1	231
0	1	0	0	0	0	0	0	230
0	0	1	0	0	0	0	0	229
1	0	0	1	0	0	0	0	228
1	1	0	0	1	0	0	0	227
0	1	1	0	0	1	0	0	226
1	0	1	1	0	0	1	0	225
0	1	0	1	1	0	0	1	224
0	0	1	0	1	1	0	0	223
0	0	0	1	0	1	1	0	222
0	0	0	0	1	0	1	1	221
0	0	0	0	0	1	0	1	220
1	0	0	0	0	0	1	0	219
1	1	0	0	0	0	0	1	218
0	1	1	0	0	0	0	0	217
1	0	1	1	0	0	0	0	216
0	1	0	1	1	0	0	0	215
1	0	1	0	1	1	0	0	214
1	1	0	1	0	1	1	0	213
1	1	1	0	1	0	1	1	212
0	1	1	1	0	1	0	1	211
0	0	1	1	1	0	1	0	210
0	0	0	1	1	1	0	1	209
0	0	0	0	1	1	1	0	208
1	0	0	0	0	1	1	1	207
0	1	0	0	0	0	1	1	206
1	0	1	0	0	0	0	1	205
1	1	0	1	0	0	0	0	204
1	1	1	0	1	0	0	0	203
1	1	1	1	0	1	0	0	202
0	1	1	1	1	0	1	0	201
0	0	1	1	1	1	0	1	200
1	0	0	1	1	1	1	0	199
0	1	0	0	1	1	1	1	198
0	0	1	0	0	1	1	1	197
0	0	0	1	0	0	1	1	196
1	0	0	0	1	0	0	1	195
1	1	0	0	0	1	0	0	194
1	1	1	0	0	0	1	0	193
0	1	1	1	0	0	0	1	192
0	0	1	1	1	0	0	0	191
0	0	0	1	1	1	0	0	190
1	0	0	0	1	1	1	0	189
0	1	0	0	0	1	1	1	188
1	0	1	0	0	0	1	1	187
1	1	0	1	0	0	0	1	186
0	1	1	0	1	0	0	0	185
0	0	1	1	0	1	0	0	184
1	0	0	1	1	0	1	0	183
0	1	0	0	1	1	0	1	182
0	0	1	0	0	1	1	0	181
1	0	0	1	0	0	1	1	180
0	1	0	0	1	0	0	1	179
0	0	1	0	0	1	0	0	178
1	0	0	1	0	0	1	0	177
1	1	0	0	1	0	0	1	176
1	1	1	0	0	1	0	0	175
0	1	1	1	0	0	1	0	174
1	0	1	1	1	0	0	1	173
0	1	0	1	1	1	0	0	172
1	0	1	0	1	1	1	0	171
1	1	0	1	0	1	1	1	170
0	1	1	0	1	0	1	1	169
1	0	1	1	0	1	0	1	168
1	1	0	1	1	0	1	0	167
0	1	1	0	1	1	0	1	166
1	0	1	1	0	1	1	0	165
0	1	0	1	1	0	1	1	164
0	0	1	0	1	1	0	1	163
1	0	0	1	0	1	1	0	162
1	1	0	0	1	0	1	1	161
1	1	1	0	0	1	0	1	160
1	1	1	1	0	0	1	0	159
0	1	1	1	1	0	0	1	158
1	0	1	1	1	0	0	0	157
0	1	1	1	1	1	0	0	156
0	1	1	0	1	1	1	1	155
1	0	1	1	0	1	1	1	154
1	1	0	1	1	0	1	1	153
1	1	1	0	1	1	0	1	152
0	1	1	1	0	1	1	0	151
1	0	1	1	1	0	1	1	150
0	1	0	1	1	1	0	1	149
0	0	1	0	1	1	1	0	148
1	0	0	0	1	1	1	1	147
1	0	0	0	0	1	0	0	146
1	1	0	0	0	1	0	1	145
0	1	1	0	0	0	1	0	144
1	0	1	1	0	0	0	1	143
1	1	0	1	1	0	0	0	142
0	1	1	0	1	1	0	0	141
0	0	1	1	0	1	1	0	140
1	0	0	1	1	0	1	1	139
1	1	0	0	1	1	0	1	138
0	1	1	1	0	0	1	1	137
0	1	1	1	0	0	1	1	136
0	0	1	1	1	0	0	1	135
0	0	0	1	1	1	0	0	134
1	0	0	0	1	1	0	0	133
0	1	0	0	0	1	1	0	132
0	0	1	0	0	0	1	1	131
0	0	0	1	0	0	0	1	130
1	0	0	0	1	0	0	0	129
0	1	0	0	0	1	0	0	128
0	0	1	0	0	0	1	0	127
1	0	0	1	0	0	0	1	126
0	1	0	0	1	0	0	0	125
1	0	1	0	0	1	0	0	124
0	1	0	1	0	0	1	0	123
0	0	1	0	1	0	0	1	122
1	0	0	1	0	1	0	0	121
1	1	0	0	1	0	1	0	120
0	1	1	0	0	1	0	1	119
0	0	1	1	0	0	1	0	118
1	0	0	1	1	0	0	1	117
1	1	0	0	1	1	0	0	116
0	1	1	0	0	1	1	0	115
1	0	1	1	0	0	1	1	114
1	1	0	1	1	0	0	1	113
1	1	1	0	1	1	0	0	112
1	1	1	1	0	1	1	0	111
0	1	1	1	1	0	1	1	110
1	0	1	1	1	1	0	1	109
0	1	0	1	1	1	1	0	108
1	0	1	0	1	1	1	1	107
0	1	0	1	0	1	1	1	106
1	0	1	0	1	0	1	1	105
0	1	0	1	0	1	0	1	104
1	0	1	0	1	0	1	0	103
1	1	0	1	0	1	0	1	102
0	1	1	0	1	0	1	0	101
0	0	1	1	0	1	0	1	100
0	0	0	1	1	0	1	0	99
1	0	0	0	1	1	0	1	98
1	1	0	0	0	1	1	0	97
1	1	1	0	0	0	1	1	96
1	1	1	1	0	0	0	1	95
1	1	1	1	1	0	0	0	94
1	1	1	1	1	1	0	0	93
1	1	1	1	1	1	1	0	92

FIGURE 2. DM7520/8520 Shift Register Divider Input Coding Table (2 Package Combinations)

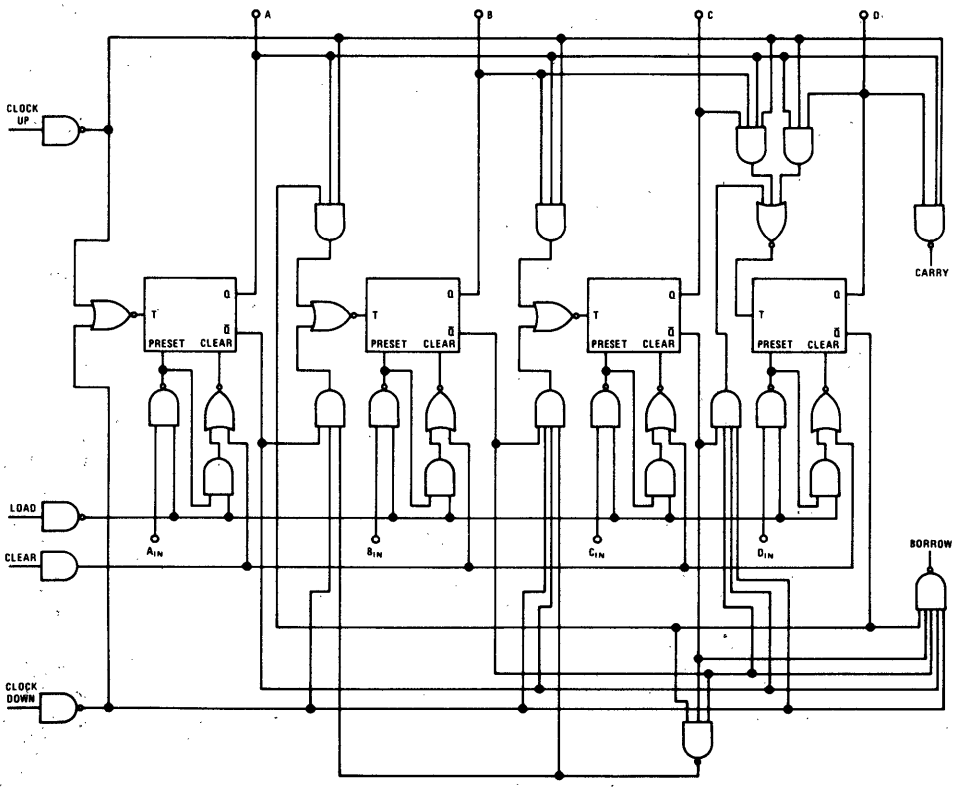
DM7560/DM8560 up/down decade counter

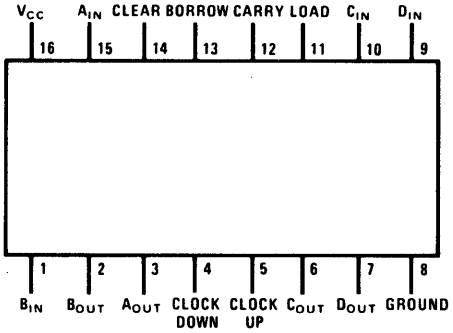
general description

The DM7560/DM8560 is a TTL, Series 54/74 compatible, up-down decade counter which is capable of being preset to any number from 0 through 9. A load input controls the asynchronous entry of these numbers, and sets all outputs to appropriate state.

Counting is performed through two clock lines—one controlling the count in the up direction, and the other in the down direction. Two outputs, Borrow and Carry, are connected to the clock inputs of subsequent counters to provide for counting to numbers greater than 9. The counter is synchronous by itself, and "semi-synchronous" (two gate delays between stages) when cascaded.

logic and connection diagrams





absolute maximum ratings

V_{CC}		7.0V
Input Voltage		5.5V
Operating Temperature Range	DM7560	−55°C to +125°C
	DM8560	0°C to +70°C
Storage Temperature Range		−65°C to +150°C
Fanout		10
Lead Temperature (Soldering, 10 sec)		300°C

electrical characteristics (Note 1)

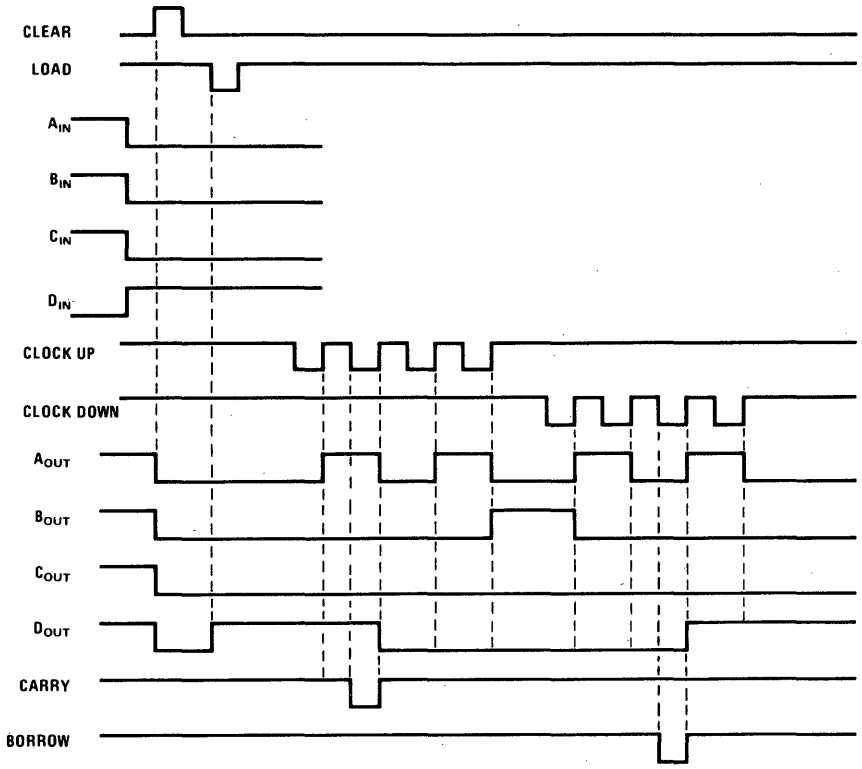
PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	DM7560	V_{CC} = 4.5V					
	DM8560	V_{CC} = 4.75V		2.0			V
Logical "0" Input Voltage	DM7560	V_{CC} = 4.5V					
	DM8560	V_{CC} = 4.75V				0.8	V
Logical "1" Output Voltage	DM7560	V_{CC} = 4.5V					
	DM8560	V_{CC} = 4.75V	I_{OUT} = −400 μA	2.4			V
Logical "0" Output Voltage	DM7560	V_{CC} = 4.5V					
	DM8560	V_{CC} = 4.75V	I_{OUT} = 16 mA			0.4	V
Logical "1" Input Current (All Inputs)	DM7560	V_{CC} = 5.5V					
	DM8560	V_{CC} = 5.25V	V_{IN} = 2.4V			40	μA
Logical "1" Input Current (All Inputs)	DM7560	V_{CC} = 5.5V					
	DM8560	V_{CC} = 5.25V	V_{IN} = 5.5V			1	mA
Logical "0" Input Current	DM7560	V_{CC} = 5.5V					
	DM8560	V_{CC} = 5.25V	V_{IN} = 0.4V			1.6	mA
Output Short Circuit Current (Note 2)	DM7560	V_{CC} = 5.5V		20			
	DM8560	V_{CC} = 5.25V	V_{OUT} = 0	18		55	mA
Supply Current	DM7560	V_{CC} = 5.5V					
	DM8560	V_{CC} = 5.25V			50		mA
Propagation Delay to a Logical "1", t_{pd1}		V_{CC} = 5.0V, T_A = 25°C	From Clock to Output		27		ns
			From Clock to Carry/Borrow		22		ns
Propagation Delay to a Logical "0", t_{pd0}		V_{CC} = 5.0V, T_A = 25°C	From Clock to Output		37		ns
			From Clock to Carry/Borrow		18		ns
Maximum Clock Frequency		V_{CC} = 5.0V, T_A = 25°C			30		MHz

Note 1: Specifications apply across −55°C to +125°C temperature range for the DM7560 and 0°C to 70°C for the DM8560 unless otherwise specified. Typicals are given for V_{CC} = 5V and T_A = 25°C only.

Note 2: Only 1 output may be shorted at a time.

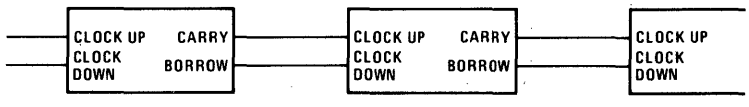
logic waveforms

[Example shown for (1) clearing, (2) asynchronously setting to eight count, (3) counting "up" to two, and (4) counting "down" to eight.]



NOTES: 1. LOAD AND CLEAR INPUTS SHOULD NEVER BE ENABLED TOGETHER.
2. A, B, C AND D INPUTS ARE FREE TO CHANGE AFTER LOAD INPUT IS DISABLED.
3. WHEN COUNTING "UP", THE "DOWN" CLOCK MUST BE IN THE LOGICAL 1 STATE, AND CONVERSELY.

cascading counters



TTL MSI

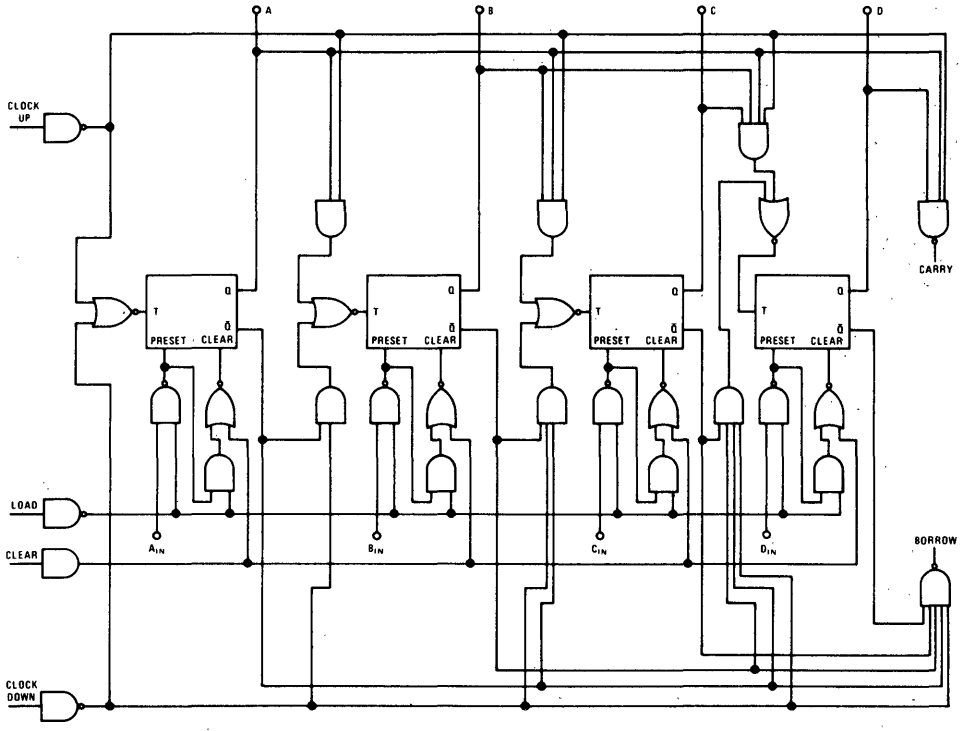
DM7563/DM8563 up/down binary counter

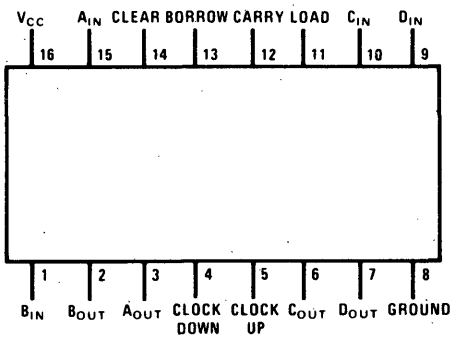
general description

The DM7563/DM8563 is a TTL, Series 54/74 compatible, up-down binary counter which is capable of being preset to any number from 0 through 15. A load input controls the asynchronous entry of these numbers, and sets all outputs to appropriate state.

Counting is performed through two clock lines—one controlling the count in the up direction, and the other in the down direction. Two outputs, Borrow and Carry, are connected to the clock inputs of subsequent counters to provide for counting to numbers greater than 15. The counter is synchronous by itself, and "semi-synchronous" (two gate delays between stages) when cascaded.

logic and connection diagrams





absolute maximum ratings

V_{CC}		7.0V
Input Voltage		5.5V
Operating Temperature Range	DM7563	−55°C to +125°C
	DM8563	0°C to +70°C
Storage Temperature Range		−65°C to +150°C
Fanout		10
Lead Temperature (Soldering, 10 sec)		300°C

electrical characteristics (Note 1)

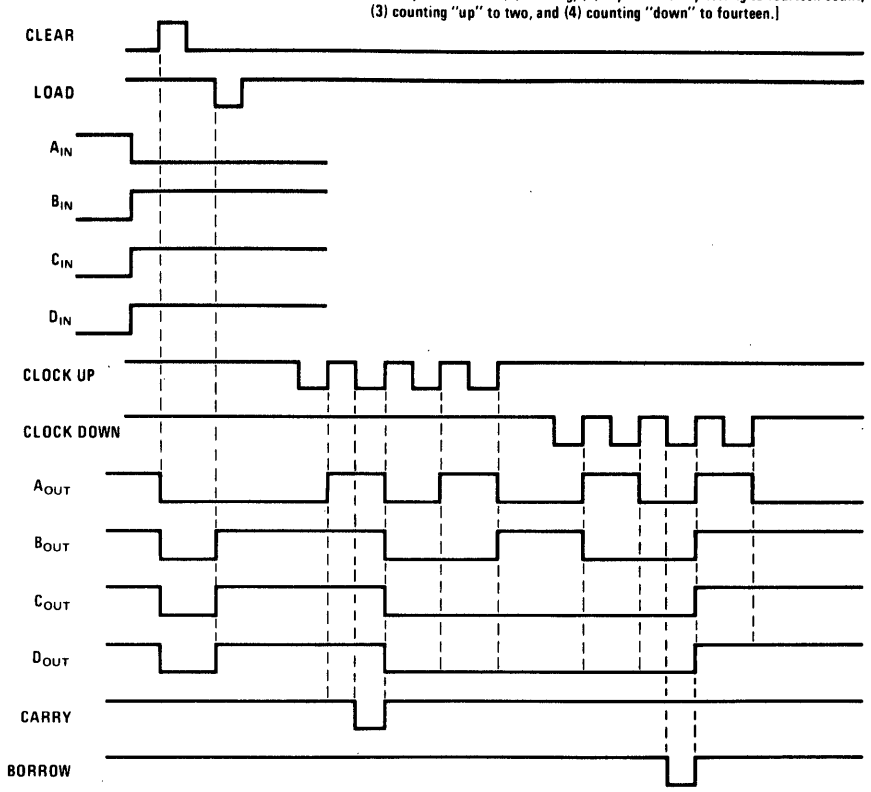
PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	DM7563	V_{CC} = 4.5V		2.0			V
	DM8563	V_{CC} = 4.75V					
Logical "0" Input Voltage	DM7563	V_{CC} = 4.5V				0.8	V
	DM8563	V_{CC} = 4.75V					
Logical "1" Output Voltage	DM7563	V_{CC} = 4.5V	I_{OUT} = −400 μA	2.4			V
	DM8563	V_{CC} = 4.75V					
Logical "0" Output Voltage	DM7563	V_{CC} = 4.5V	I_{OUT} = 16 mA			0.4	V
	DM8563	V_{CC} = 4.75V					
Logical "1" Input Current (All Inputs)	DM7563	V_{CC} = 5.5V	V_{IN} = 2.4V			40	μA
	DM8563	V_{CC} = 5.25V					
Logical "1" Input Current (All Inputs)	DM7563	V_{CC} = 5.5V	V_{IN} = 5.5V			1	mA
	DM8563	V_{CC} = 5.25V					
Logical "0" Input Current	DM7563	V_{CC} = 5.5V	V_{IN} = 0.4V			1.6	mA
	DM8563	V_{CC} = 5.25V					
Output Short Circuit Current (Note 2)	DM7563	V_{CC} = 5.5V	V_{OUT} = 0	20		55	mA
	DM8563	V_{CC} = 5.25V		18			
Supply Current	DM7563	V_{CC} = 5.5V			50		mA
	DM8563	V_{CC} = 5.25V					
Propagation Delay to a Logical "1", t_{pd1}		V_{CC} = 5.0V, T_A = 25°C	From Clock to Output		27		ns
			From Clock to Carry/Borrow		22		ns
Propagation Delay to a Logical "0", t_{pd0}		V_{CC} = 5.0V, T_A = 25°C	From Clock to Output		37		ns
			From Clock to Carry/Borrow		18		ns
Maximum Clock Frequency		V_{CC} = 5.0V, T_A = 25°C			30		MHz

Note 1: Specifications apply across −55°C to +125°C temperature range for the DM7563 and 0°C to 70°C for the DM8563 unless otherwise specified. Typicals are given for V_{CC} = 5V and T_A = 25°C only.

Note 2: Only 1 output may be shorted at a time.

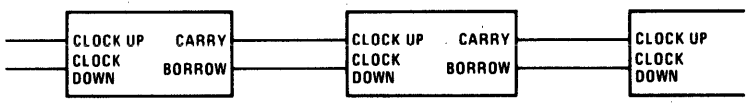
logic waveforms

[Example shown for (1) clearing, (2) asynchronously setting to fourteen count, (3) counting "up" to two, and (4) counting "down" to fourteen.]



NOTES:
1. LOAD AND CLEAR INPUTS SHOULD NEVER BE ENABLED TOGETHER.
2. A, B, C, and D INPUTS ARE FREE TO CHANGE AFTER LOAD INPUT IS DISABLED.
3. WHEN COUNTING "UP", THE "DOWN" CLOCK MUST BE IN THE LOGICAL 1 STATE, AND CONVERSELY.

cascading counters



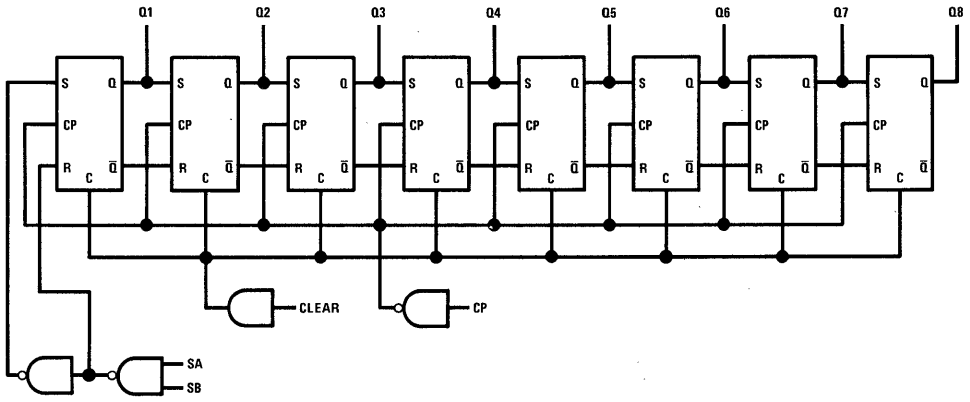
DM7570/DM8570 eight bit serial-in parallel-out shift register

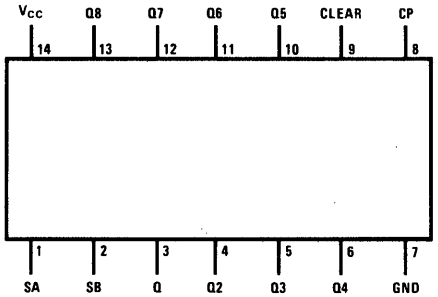
general description

The DM7570/DM8570 utilizes Series 54/74 compatible TTL circuitry to provide an eight-bit serial-in parallel-out shift register designed to operate at frequencies of 20 MHz. Other features include gated serial inputs for strobe capability and a clear input which, when taken to a logical 0, asynchronously sets all flip flops to the logical 0 state.

Because the flip flops are R-S instead of J-K, input information may be changed immediately prior to the triggering edge of the clock waveform. Logical 1 levels on SA and SB enter logical 1's into the shift register. Clocking occurs on the positive-going edge of the clock pulse.

logic and connection diagrams





absolute maximum ratings

Supply Voltage		7V
Input Voltage		5.5V
Fanout		5
Storage Temperature Range		−65°C to +150°C
Operating Temperature Range	DM7570	−55°C to +125°C
	DM8570	0°C to +70°C
Lead Temperature (Soldering, 10 sec.)		300°C

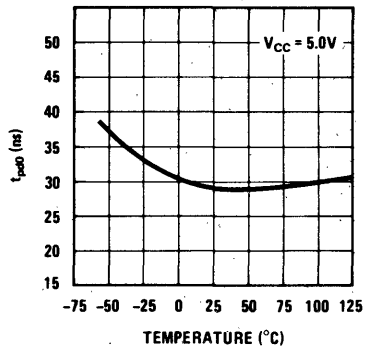
electrical characteristics (Note 1)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	DM7570	V_{CC} = 4.5V		2.0			V
	DM8570	V_{CC} = 4.75V					
Logical "0" Input Voltage	DM7570	V_{CC} = 4.5V				0.8	V
	DM8570	V_{CC} = 4.75V					
Logical "1" Output Voltage	DM7570	V_{CC} = 4.5V	I_{OUT} = −200 μA	2.4			V
	DM8570	V_{CC} = 4.75V					
Logical "0" Output Voltage	DM7570	V_{CC} = 4.5V	I_{OUT} = 8 mA			0.4	V
	DM8570	V_{CC} = 4.75V					
Logical "1" Input Current (Except Clear Input)	DM7570	V_{CC} = 5.5V	V_{IN} = 2.4V			40	μA
	DM8570	V_{CC} = 5.25V					
Logical "1" Input Current (Clear Input)	DM7570	V_{CC} = 5.5V	V_{IN} = 2.4V			80	μA
	DM8570	V_{CC} = 5.25V					
Logical "1" Input Current	DM7570	V_{CC} = 5.5V	V_{IN} = 5.5V			1	mA
	DM8570	V_{CC} = 5.25V					
Logical "0" Input Current (Except Clear Input)	DM7570	V_{CC} = 5.5V	V_{IN} = 0.4V			1.6	mA
	DM8570	V_{CC} = 5.25V					
Logical "0" Input Current (Clear Input)	DM7570	V_{CC} = 5.5V	V_{IN} = 0.4V			3.2	mA
	DM8570	V_{CC} = 5.25V					
Output Short Circuit Current (Note 2)	DM7570	V_{CC} = 5.5V	V_{OUT} = 0V	10		27.5	mA
	DM8570	V_{CC} = 5.25V		9			
Power Supply Current	DM7570	V_{CC} = 5.5V			36	54	mA
	DM8570	V_{CC} = 5.25V					
Maximum Clock Frequency		V_{CC} = 5.0V, 25°C, 50% Duty Cycle		14	20		mHz
Propagation Delay to a Logical "0" from Clock to Output, t_{pd0}		V_{CC} = 5.0V, T_A = 25°C, C = 50 pF		10	28	40	ns
Propagation Delay to a Logical "1" from Clock to Output, t_{pd1}		V_{CC} = 5.0V, T_A = 25°C, C = 50 pF		10	28	40	ns
Propagation Delay to a Logical "0" from Clear to Output		V_{CC} = 5.0V, T_A = 25°C, C = 50 pF			34	50	ns
Minimum Clock Pulse Width		V_{CC} = 5.0V, T_A = 25°C, C = 50 pF			25	45	ns
Minimum Clear Pulse Width		V_{CC} = 5.0V, T_A = 25°C, C = 50 pF			30	45	ns
Minimum Time that $S_A \cdot S_B$ Data Must be Set-up Prior to Clock Pulse, $t_{set\text{-}up}$		V_{CC} = 5.0V, T_A = 25°C, C = 50 pF, Clock Pulse Width = 50 ns			15	30	ns
Minimum Time that $S_A \cdot S_B$ Data Must be Held After Clock Pulse, t_{hold}		V_{CC} = 5.0V, T_A = 25°C, C = 50 pF, Clock Pulse Width = 50 ns			−15	0	ns

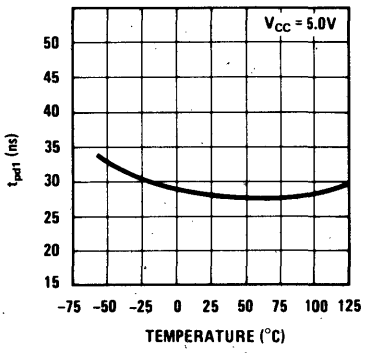
Note 1: Unless otherwise specified, limits shown apply from −55°C to +125°C for the DM7570 and 0°C to +70°C for the DM8570. Typical values apply to supply voltages of 5.0V and 25°C.
Note 2: Only one output should be shorted at a time.

typical performance characteristics

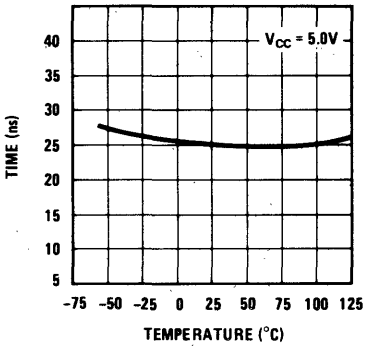
Transition Time to a Logical "0" (t_{pd0}) from Clock to Output vs Temperature



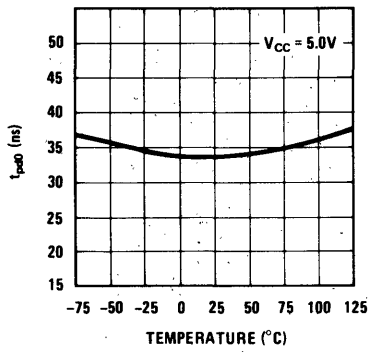
Transition Time to a Logical "1" (t_{pd1}) from Clock to Output vs Temperature



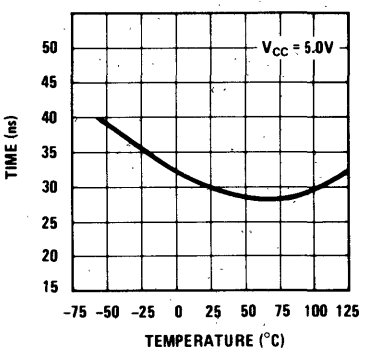
Minimum Clock Pulse Width vs Temperature



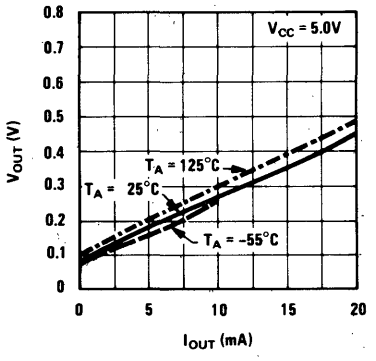
Transition Time to a Logical "0" (t_{pd0}) from Clear to Output vs Temperature



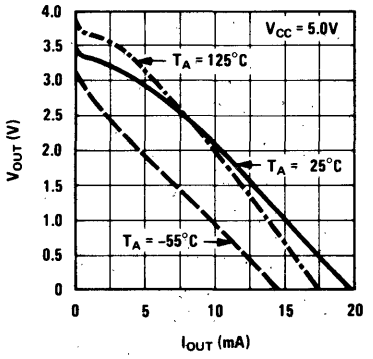
Minimum Clear Pulse Width vs Temperature



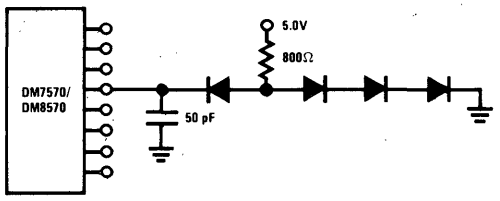
Logical "0" Output Voltage vs Sink Current



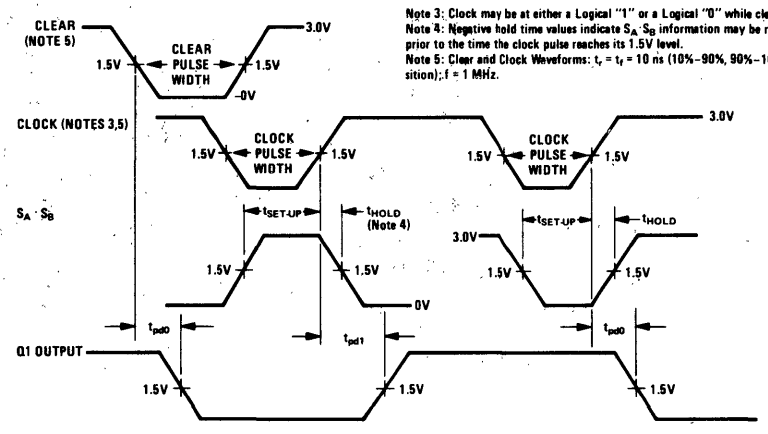
Logical "1" Output Voltage vs Source Current



ac test circuit



switching time waveforms



Note 3: Clock may be at either a Logical "1" or a Logical "0" while clearing.
Note 4: Negative hold time values indicate S_A, S_B information may be released prior to the time the clock pulse reaches its 1.5V level.
Note 5: Clear and Clock Waveforms: t_r = t_f = 10 ns (10%–90%, 90%–10% transition); f = 1 MHz.

TTL MSI

DM7590/DM8590 eight-bit parallel-in serial-out shift register

general description

The DM7590/DM8590 utilizes Series 54/74 compatible TTL circuitry to provide an eight-bit parallel-in serial-out shift register designed to operate at frequencies of 20 MHz. The device also features gating to inhibit clocking, parallel load control, and both Q and $\overline{Q}$ outputs from the last flip flop for added flexibility.

The following characteristics are applicable:

The Clock Inhibit input, when in the logical "1" state, will inhibit the Clock. It must be in the logical "0" state for clocking to occur.

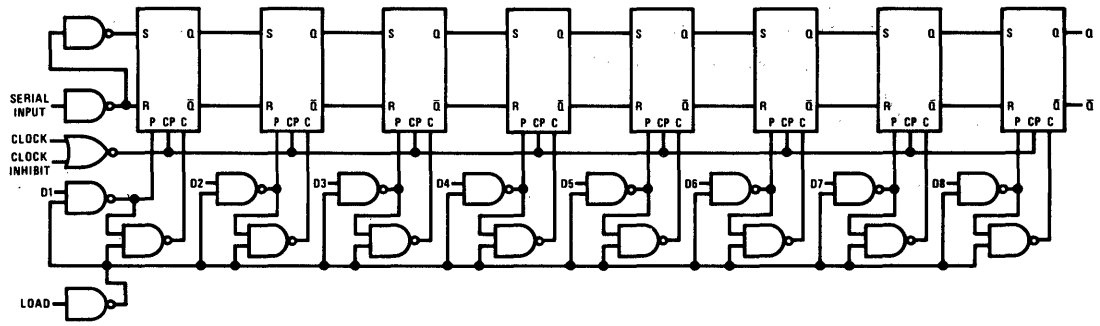
There is no difference between the Clock input and the Clock Inhibit input. Their functions may be reversed if ease of layout results.

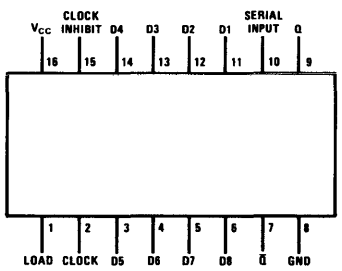
Clocking occurs on the positive-going transition of the Clock input.

Data on the D1 through D8 inputs will be entered on the negative-going transition of the Load input. This information is entered independent of the state of the Clock, Clock Inhibit, or Serial Input lines. Information on these parallel inputs may be changed while the Load line is enabled thus changing the information in the register.

The logic level applied to the Serial Input is entered into the first flip flop when the register is clocked.

logic and connection diagrams





absolute maximum ratings

Supply Voltage		+7V
Input Voltage		+5.5V
Fan Out		10
Storage Temperature Range		−65°C to +150°C
Operating Temperature Range	DM7590	−55°C to +125°C
	DM8590	0°C to +70°C

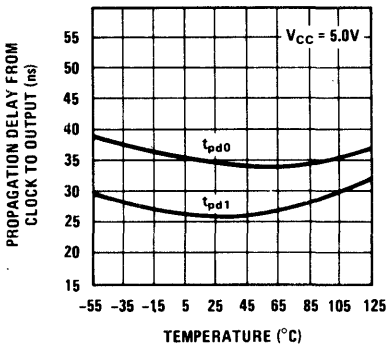
electrical characteristics (Note 1)

PARAMETER		CONDITION	MIN	TYP	MAX	UNITS
Input Diode Clamp Voltage		V_{CC} = 5.0V, T_A = 25°C, I_{IN} = −12 mA			−1.5	V
Logical "1" Input Voltage	DM7590	V_{CC} = 4.5V				
	DM8590	V_{CC} = 4.75V	2.0			V
Logical "0" Input Voltage	DM7590	V_{CC} = 4.5V				
	DM8590	V_{CC} = 4.75V			0.8	V
Logical "1" Output Voltage	DM7590	V_{CC} = 4.5V				
	DM8590	V_{CC} = 4.75V, I_{OUT} = −400 μA	2.4			V
Logical "0" Output Voltage	DM7590	V_{CC} = 4.5V				
	DM8590	V_{CC} = 4.75V, I_{OUT} = 16 mA			0.4	V
Logical "1" Input Current (All Inputs Except Load Input)	DM7590	V_{CC} = 5.5V				
	DM8590	V_{CC} = 5.25V, V_{IN} = 2.4V			40	μA
Logical "1" Input Current (Load Input)	DM7590	V_{CC} = 5.5V				
	DM8590	V_{CC} = 5.25V, V_{IN} = 2.4V			80	μA
Logical "1" Input Current	DM7590	V_{CC} = 5.5V				
	DM8590	V_{CC} = 5.25V, V_{IN} = 5.5V			1	mA
Logical "0" Input Current (All Inputs Except Load Input)	DM7590	V_{CC} = 5.5V				
	DM8590	V_{CC} = 5.25V, V_{IN} = 0.4V			−1.6	mA
Logical "0" Input Current (Load Input)	DM7590	V_{CC} = 5.5V				
	DM8590	V_{CC} = 5.25V, V_{IN} = 0.4V			−3.2	mA
Output Short Circuit Current	DM7590	V_{CC} = 5.5V	−20			
	DM8590	V_{CC} = 5.25V, V_{OUT} = 0V	−18		−55	mA
Power Supply Current	DM7590	V_{CC} = 5.5V				
	DM8590	V_{CC} = 5.25V		40	63	mA
Propagation Delay to a Logical "0" from Clock to Q or $\overline{Q}$, t_{pd0}		V_{CC} = 5.0V, T_A = 25°C		35	50	ns
Propagation Delay to a Logical "1" from Clock to Q or $\overline{Q}$, t_{pd1}		V_{CC} = 5.0V, T_A = 25°C		26	40	ns
Propagation Delay to a Logical "0" from D_8 to Q or $\overline{Q}$, $t_{pd0(D8)}$		V_{CC} = 5.0V, T_A = 25°C		36	50	ns
Propagation Delay to a Logical "1" from D_8 to Q or $\overline{Q}$, $t_{pd1(D8)}$		V_{CC} = 5.0V, T_A = 25°C		25	40	ns
Propagation Delay to a Logical "0" from Load to Q or $\overline{Q}$, $t_{pd0(load)}$		V_{CC} = 5.0V, T_A = 25°C		42	60	ns
Propagation Delay to a Logical "1" from Load to Q or $\overline{Q}$, $t_{pd1(load)}$		V_{CC} = 5.0V, T_A = 25°C		34	50	ns
Minimum Time That Serial Input Data Must Be Set Up Prior to Clock Pulse, $t_{set\ up\ (clock)}$		V_{CC} = 5.0V, T_A = 25°C		23	40	ns
Minimum Time That Serial Input Data Must Be Held after Clock Pulse, $t_{hold\ (clock)}$		V_{CC} = 5.0V, T_A = 25°C			0	ns
Minimum Time That D_1–D_8 Input Data Must Be Set Up Prior to Load Pulse Termination, $t_{set\ up\ (load)}$		V_{CC} = 5.0V, T_A = 25°C		10	25	ns
Minimum Time That D_1–D_8 Input Data Must Be Held after to Load Pulse Termination, $t_{hold\ (load)}$		V_{CC} = 5.0V, T_A = 25°C			5	ns
Minimum Clock Pulse Width		V_{CC} = 5.0V, T_A = 25°C		25	35	ns
Minimum Load Pulse Width		V_{CC} = 5.0V, T_A = 25°C		24	35	ns
Maximum Shift Frequency		V_{CC} = 5.0V, T_A = 25°C, Duty Cycle	14	20		MHz

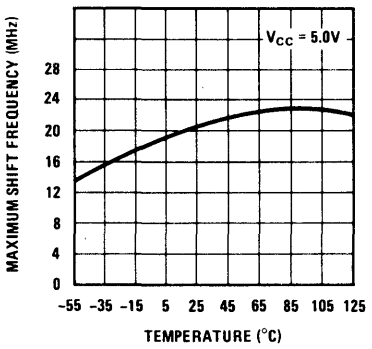
Note 1: Unless otherwise specified, limits shown apply from −55°C to +125°C for the DM7590 and 0°C to +70°C for the DM8590. Typical values apply to supply voltages of 5.0V.

typical performance characteristics

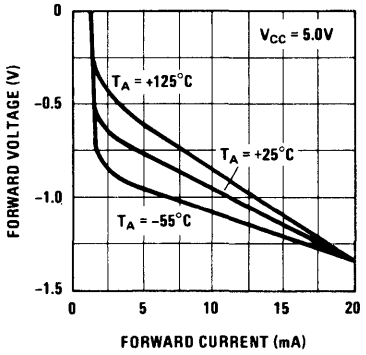
Propagation Delay Times vs Temperature



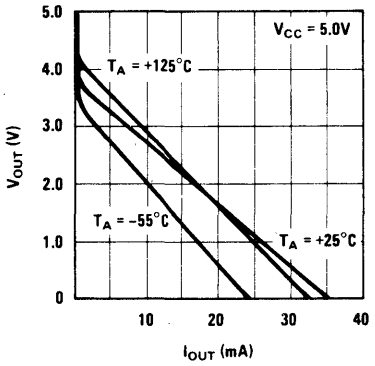
Maximum Shift Frequency vs Temperature



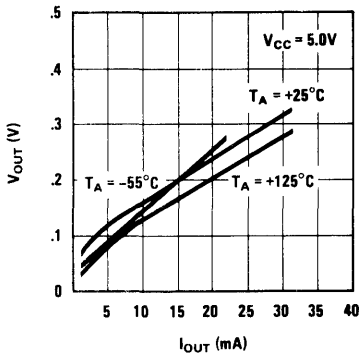
Input Clamp Diode Characteristics



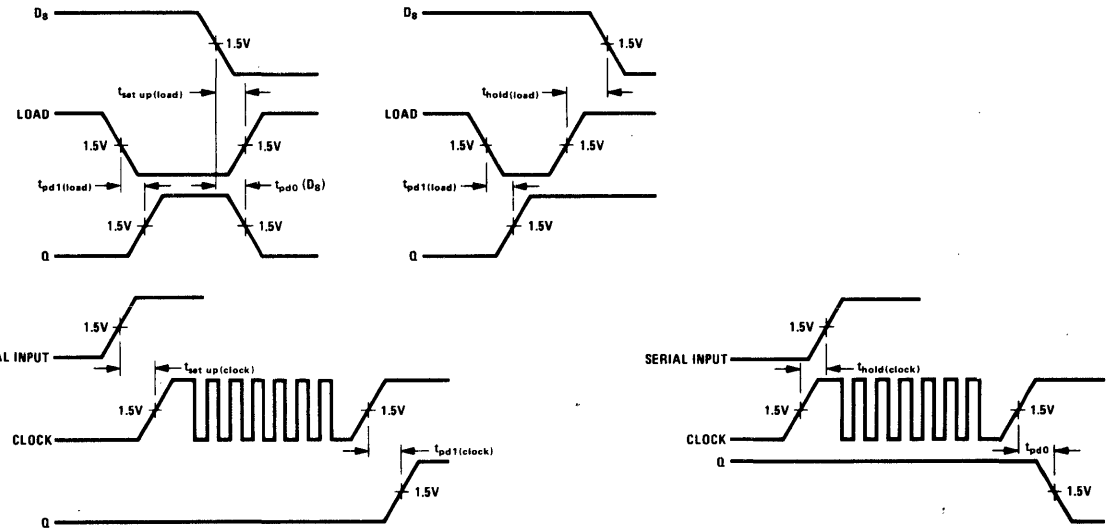
Logical "1" Output Voltage vs Source Current



Logical "0" Output Voltage vs Sink Current



switching time waveforms



DM9300/DM8300 (9300-51/9300-59) four-bit shift register

general description

The DM9300/DM8300 is a four-bit multi-function shift register designed to work at typical speeds of 25 MHz.

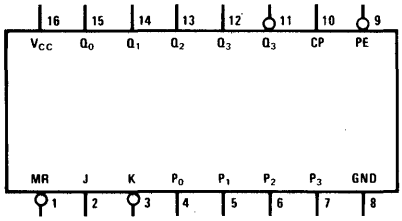
It features a common asynchronous Reset input which resets the register independent of any other input. In addition, the J and $\overline{K}$ inputs to the first flip flop enable greater flexibility in the operation of the register. (See truth table.)

The $\overline{PE}$ (Parallel Enable) control allows information to be entered from the parallel inputs or be shifted right. When the $\overline{PE}$ input is in the logical "0" state, the information on the parallel inputs will be entered into the flip flops on the subsequent clock pulse. A logical "1" level on the PE control will allow shifting to the right.

The outputs change state on the positive-going transition of the clock input.

This register is completely compatible with Series 54/74 and CCSL devices. Input diode clamps are provided for additional system reliability.

connection diagram



truth table

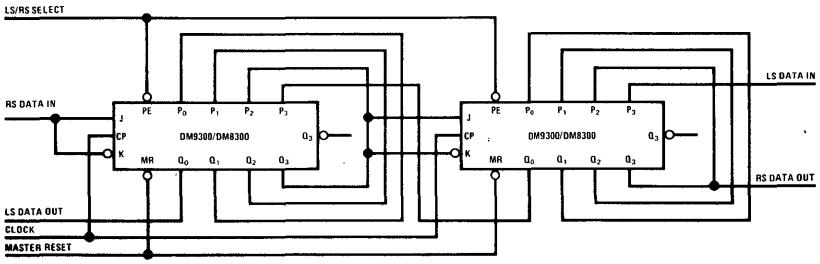
J	$\overline{K}$	Q_0 at t_{n+1}
0	0	0
0	1	Q_0 at t_n (no change)
1	0	$\overline{Q}_0$ at t_n (toggle)
1	1	1

($\overline{PE}$ = logical "1", $\overline{MR}$ = logical "1")

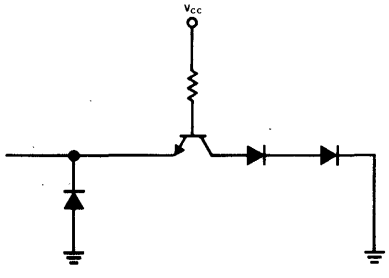
typical application

Eight Bit Left/Right Shift Register

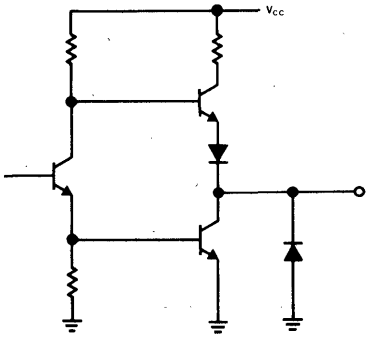
This register shifts left or right on each shift clock, depending upon the condition of the LS/RS select input. If this input is high, right shift occurs and if low, left shift occurs.



equivalent circuits



INPUT CURRENT VERSUS INPUT VOLTAGE



OUTPUT CURRENT VERSUS OUTPUT VOLTAGE
(Q_0, Q_1, Q_2, Q_3 AND $\overline{Q}_3$)

absolute maximum ratings

V_{CC} Voltage Range		-.5V to 7V
Input Voltage Range		-.5V to 5.5V
Output Voltage (Logical "1" state)		5.5V
Operating Temperature Range	DM9300(9300-51)	-55°C to +125°C
	DM8300(9300-59)	0°C to 75°C
Storage Temperature Range		-65°C to +150°C
Lead Temperature (Soldering, 10 sec)		300°C

electrical characteristics (T_A = -55°C to +125°C, V_{CC} = 5.0V ±10%)

SYMBOL	CHARACTERISTICS	LIMITS -55°C MIN	LIMITS -55°C MAX	LIMITS +25°C MIN	LIMITS +25°C TYP	LIMITS +25°C MAX	LIMITS +125°C MIN	LIMITS +125°C MAX	UNITS	CONDITIONS & COMMENTS
V_{OH}	Output High Voltage	2.4		2.4	2.7		2.4		Volts	V_{CC} = 4.5V, I_{OH} = -0.36 mA
V_{OL}	Output Low Voltage		0.4		0.2	0.4		0.4	Volts	V_{CC} = 5.5V, I_{OL} = 9.6 mA V_{CC} = 4.5V, I_{OL} = 7.44 mA
V_H	Input High Voltage	2.0		1.7			1.4		Volts	Guaranteed input high threshold for all inputs
V_L	Input Low Voltage		0.8			0.9		0.8	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current		-1.6		-1.10	-1.6		-1.6	mA	V_{CC} = 5.5V
	J, K, MR, P_0, P_1, P_2 & P_3		-1.24		-0.97	-1.24		-1.24	mA	V_{CC} = 4.5V V_F = 0.4V
I_R	Input Leakage Current J, K, MR, P_0, P_1, P_2 & P_3				15	60		60	μA	V_{CC} = 5.5V, V_R = 4.5V

electrical characteristics (T_A = 0°C to +75°C, V_{CC} = 5.0V ±5%)

SYMBOL	CHARACTERISTICS	LIMITS 0°C MIN	LIMITS 0°C MAX	LIMITS +25°C MIN	LIMITS +25°C TYP	LIMITS +25°C MAX	LIMITS +75°C MIN	LIMITS +75°C MAX	UNITS	CONDITIONS & COMMENTS
V_{OH}	Output High Voltage	2.4		2.4	3.0		2.4		Volts	V_{CC} = 4.75V, I_{OH} = -0.36 mA
V_{OL}	Output Low Voltage		0.45		0.2	0.45		0.45	Volts	V_{CC} = 5.25V, I_{OL} = 9.6 mA
V_H	Input High Voltage	1.9		1.8			1.6		Volts	V_{CC} = 4.75V, I_{OL} = 8.5 mA Guaranteed input high threshold for all inputs
V_L	Input Low Voltage		0.85			0.85		0.85	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current		-1.6		-1.0	-1.6		-1.6	mA	V_{CC} = 5.25V
	J, $\overline{K}$, MR, P_0, P_1, P_2 & P_3		-1.41		-0.9	-1.41		-1.41	mA	V_{CC} = 4.75V, V_F = 0.45V
I_R	Input Leakage Current J, $\overline{K}$, MR, P_0, P_1, P_2 & P_3				15	60		60	μA	V_{CC} = 5.25V, V_R = 4.5V

switching characteristics (T_A = 25°C)

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS & COMMENTS
t_{pd+}	Turn Off Delay		17	35	ns	V_{CC} = 5.0V, C_L = 15 pF
t_{pd-}	Turn On Delay		22	45	ns	(See Figs. 1 & 2a)
f_{sr}	Shift Right Frequency	15	30		MHz	V_{CC} = 5.0V, C_L = 15 pF (See Figs. 1 & 2c)
CP_{pw}	Clock Pulse Width	35	15		ns	
t_s	Set-up Time	35	10		ns	V_{CC} = 5.0V
t_r	Release Time		10	0	ns	C_L = 15 pF
$t_s(\overline{PE})$	Set-up Time for $\overline{PE}$	45	20		ns	(See Figs. 2a & 2b)
$t_r(\overline{PE})$	Release Time for $\overline{PE}$		17	10	ns	
$t_{pd-}(\overline{MR})$	Reset Time for $\overline{MR}$		28		ns	
$t_{rec}(\overline{MR})$	Recovery Time for $\overline{MR}$		13		ns	
$\overline{MR}_{pw}$	Min Reset Pulse Width		15		ns	

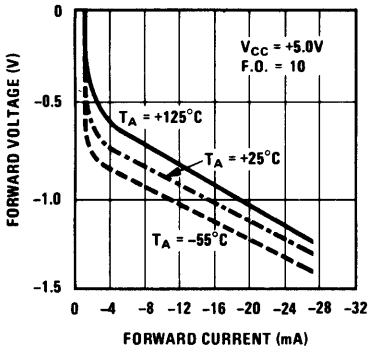
SET UP TIME: t_s is defined as the minimum time required for the logic level to be present at the logic input prior to the clock transition from low to high in order for the flip flop(s) to respond.

RELEASE TIME: t_r is defined as the maximum time allowed for the logic level to be present at the logic input prior to the clock transition from low to high in order for the flip flop(s) not to respond.

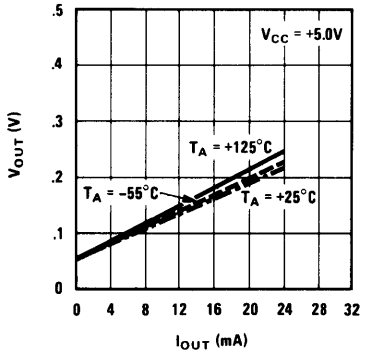
RECOVERY TIME FOR $\overline{MR}$: $t_{rec}(\overline{MR})$ is defined as the minimum time required between the end of the reset pulse and the clock transition from low to high in order for the flip flop(s) to respond to the clock.

typical performance characteristics

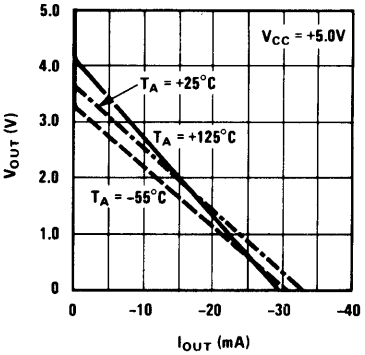
Input Clamp Diode Characteristics



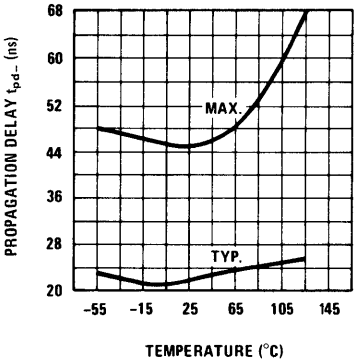
Logical "0" Output Voltage vs Sink Current



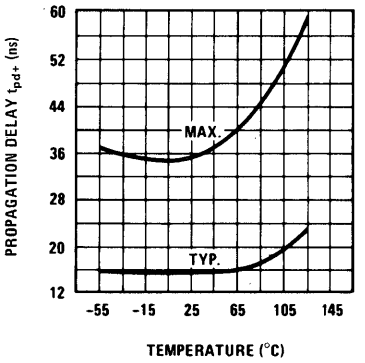
Logical "1" Output Voltage vs Source Current



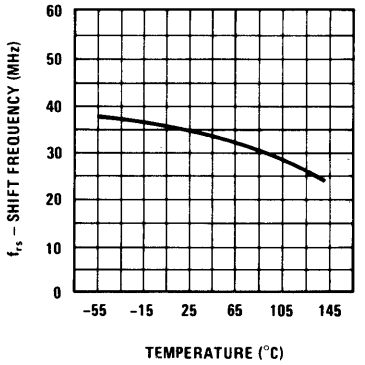
t_{pd-} Propagation Delay – Clock to Q_3 or $\overline{Q}_3$ Outputs vs Temp.



t_{pd+} Propagation Delay – Clock to Q_3 or $\overline{Q}_3$ Outputs vs Temp.



f_{rs} – Shift Frequency vs Temp.



ac test circuit

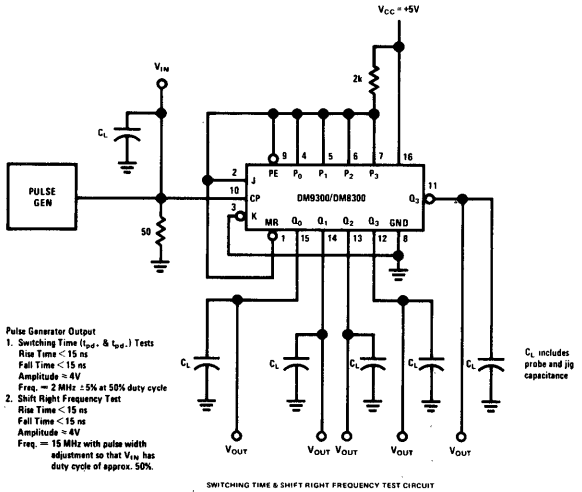


Figure 1

switching time waveforms

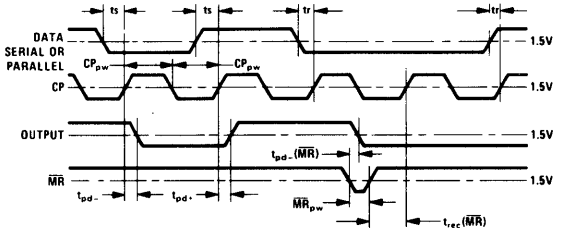


Figure 2a

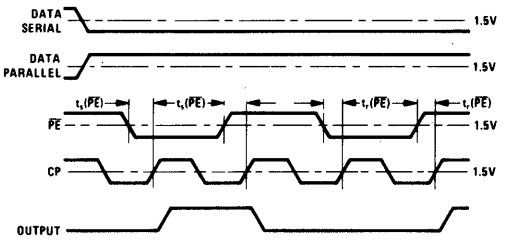


Figure 2b

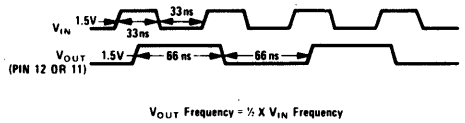


Figure 2c

TTL MSI

DM9601/DM8601 (9601-51/9601-59) retriggerable monostable multivibrator

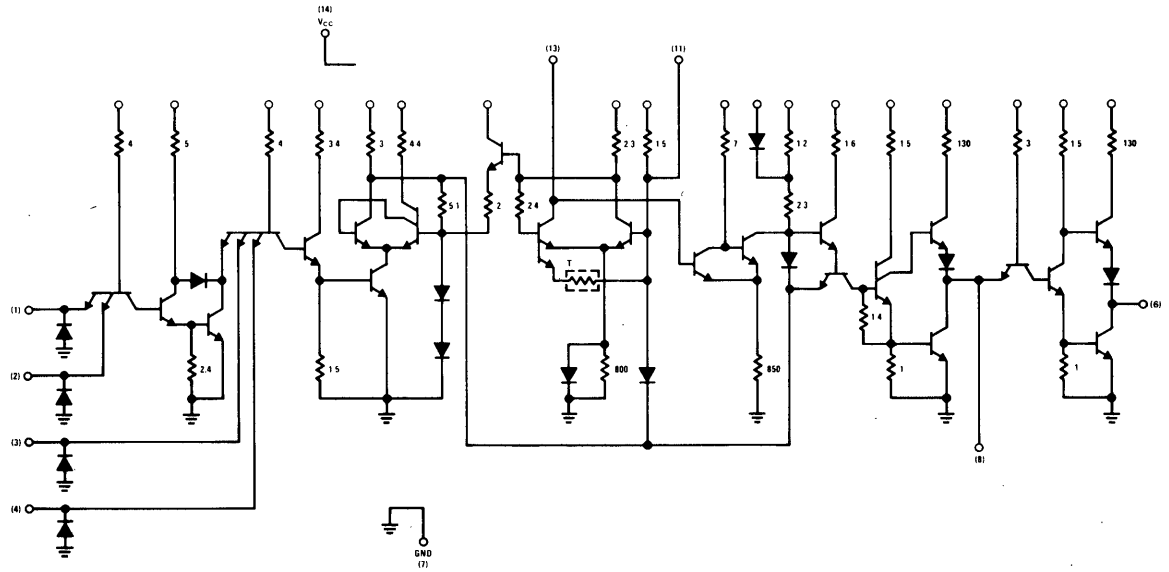
general description

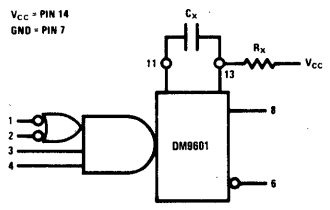
The DM9601/DM8601 is both pin-for-pin and spec-for-spec interchangeable with the 9601 one-shot. Pulse widths range from 50 ns upward depending upon the values of the external R&C used. The retriggerable feature allows for output pulse widths to be extended beyond the normal range attainable with just a resistor and capacitor.

Additional Features Include:

- Input Clamping Diodes
- Complementary DC Level Sensitive Inputs
- Flexibility of Operation—Optional Retriggering/Lockout Capability
- DTL/TTL Compatible Logic Levels
- High Speed Operation—Input Repetition Rate > 10 MHz
- Output Pulse Width Range 50 ns to ∞
- Leading or Trailing Edge Triggering
- Complementary Outputs

schematic and logic diagrams





absolute maximum ratings

Supply Voltage to Ground	−0.5V to +8.0V
Input Voltage	−0.5V to +5.5V
Voltage Applied to Outputs	−0.5V to $+V_{CC}$
Storage Temperature	−65°C to +150°C
Operating Temperature	
DM9601	−55°C to +125°C
DM8601	0°C to +75°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics DM9601(9601-51)

TABLE I

Symbol	Parameter	Limits							Units	Conditions (Note 1)
		−55°C		+25°C			+125°C			
		Min.	Max.	Min.	Typ.	Max.	Min.	Max.		
V_{OH}	Output High Voltage	2.4		2.4	3.3		2.4		V	V_{CC} = 4.5V I_{OH} = −0.72 mA (Note 2)
V_{OL}	Output Low Voltage		0.4		0.2	0.4		0.4	V	V_{CC} = 4.5V I_{OL} = 10 mA (Note 2)
V_{IH}	Input High Voltage	2.0		1.7			1.4		V	V_{CC} = 4.5V
V_{IL}	Input Low Voltage		0.85			0.90		0.85	V	V_{CC} = 5.5V (Note 3)
I_F	Input Load Current		−1.6		−1.1	−1.6		−1.6	mA	V_{CC} = 5.5V V_F = 0.4V
I_R	Input Leakage Current				15	60		60	μA	V_{CC} = 5.5V V_R = 4.5V
I_{SC}	Short Circuit Current			−10		−40				V_{CC} = 5.0V V_{OUT} = 0V (Note 2)
I_{PD}	Quiescent Power Supply Drain		25			25		25	mA	V_{CC} = 5.5V
t_{pd+}	Negative Trigger Input to True Output				25	40			ns	V_{CC} = 5.0V R_X = 5.0 KΩ
t_{pd-}	Negative Trigger Input to Complement Output				25	40			ns	C_X = 0 C_L = 15 pF
$t_{pw(min)}$	Minimum True Output Pulse Width				45	65			ns	
Δt_{pw}	Pulse Width Variation			3.08	3.42	3.76			μs	V_{CC} = 5.0V R_X = 10 KΩ, C_X = 1,000 pF
C_{stray}	Maximum Allowable Wiring Capacitance (Pin 13)		50			50		50	pF	Pin 13 to GND
R_X	External Timing Resistor	5.0	25	5.0		25	5.0	25	kΩ	

Note 1: Unless otherwise specified, R_X = 10 KΩ between Pin 13 and V_{CC} on all tests.

Note 2: Ground Pin 11 for V_{OL} test on Pin 6, V_{OH} test on Pin 8 and I_{SC} test on Pin 8. Open Pin 11 for V_{OL} test on Pin 8, V_{OH} test on Pin 6 and I_{SC} test on Pin 6.

Note 3: Pulse test to determine V_{IH} and V_{IL} (Min PW = 40 ns).

electrical characteristics DM8601(9601-59)

TABLE II

Symbol	Parameter	Limits							Units	Conditions (Note 1)
		0°C		+25°C			+75°C			
		Min.	Max.	Min.	Typ.	Max.	Min.	Max.		
V_{OH}	Output High Voltage	2.4		2.4	3.4		2.4		V	V_{CC} = 4.75V I_{OH} = -0.96 mA (Note 2)
V_{OL}	Output Low Voltage		0.45		0.2	0.45		0.45	V	V_{CC} = 4.75V I_{OL} = 12.8 mA (Note 2)
V_{IH}	Input High Voltage	1.9		1.8			1.6		V	V_{CC} = 4.75V
V_{IL}	Input Low Voltage		0.85			0.85		0.85	V	V_{CC} = 5.25V (Note 3)
I_F	Input Load Current		-1.6		-1.0	-1.6		-1.6	mA	V_{CC} = 5.25V V_F = 0.45V
I_R	Input Leakage Current				15	60		60	μA	V_{CC} = 5.25V V_R = 4.5V
I_{SC}	Short Circuit Current			-10		-40			mA	V_{CC} = 5.0V V_{OUT} = 0V (Note 2)
I_{PD}	Quiescent Power Supply Drain		25			25		25	mA	V_{CC} = 5.25V GND Pins 1 & 2
t_{pd+}	Negative Trigger Input to True Output				25	40			ns	V_{CC} = 5.0V R_X = 5.0 KΩ
t_{pd-}	Negative Trigger Input to Complement Output				25	40			ns	C_X = 0 C_L = 15 pF
$L_{pw(min)}$	Minimum True Output Pulse Width				45	65			ns	
Δt_{pw}	Pulse Width Variation			3.08	3.42	3.76			μs	V_{CC} = 5.0V R_X = 10 KΩ, C_X = 1,000 pF
C_{stray}	Maximum Allowable Wiring Capacitance (Pin 13)		50			50		50	pF	Pin 13 to GND
R_X	External Timing Resistor	5.0	50	5.0		50	5.0	50	kΩ	

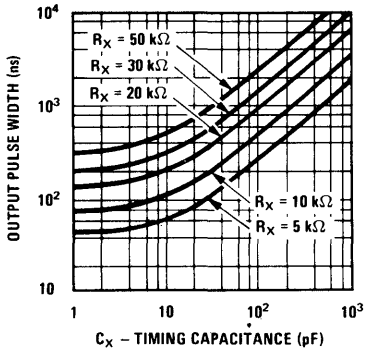
Note 1: Unless otherwise specified, R_X = 10 KΩ between Pin 13 and V_{CC} on all tests.

Note 2: Ground Pin 11 for V_{OL} test on Pin 6, V_{OH} test on Pin 8 and I_{SC} test on Pin 8. Open Pin 11 for V_{OL} test on Pin 8, V_{OH} test on Pin 6 and I_{SC} test on Pin 6.

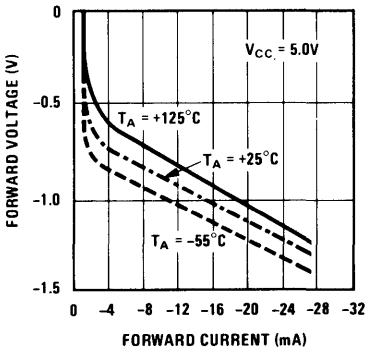
Note 3: Pulse test to determine V_{IH} and V_{IL} (Min PW = 40 ns).

typical performance characteristics

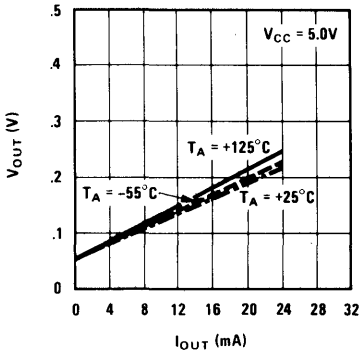
Output Pulse Width vs R_X and C_X for $C_X < 10^3$ pF



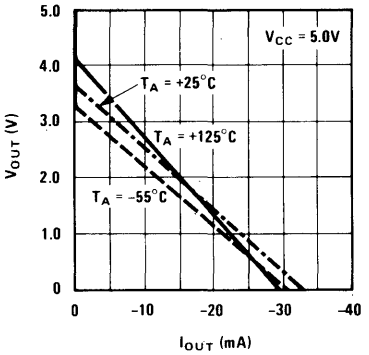
Input Clamp Diode Characteristics



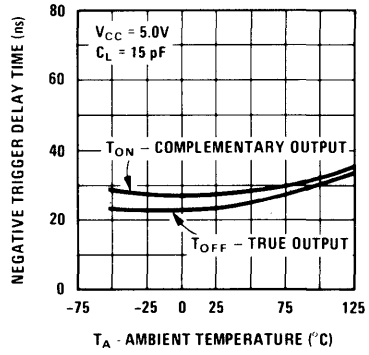
Logical "0" Output Voltage vs Sink Current



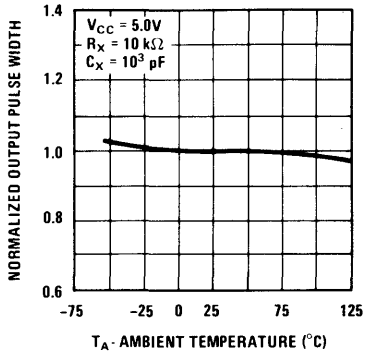
Logical "1" Output Voltage vs Source Current



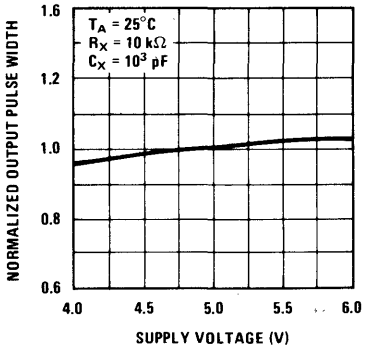
Negative Trigger Delay Time vs Ambient Temperature



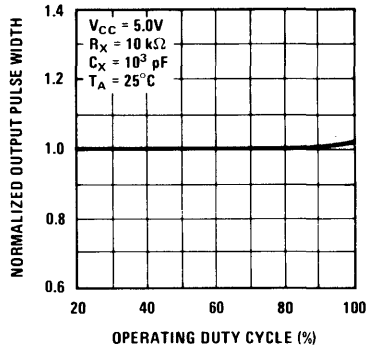
Normalized Output Pulse Width vs Ambient Temperature



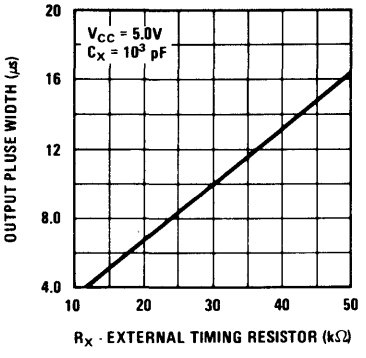
Normalized Output Pulse Width vs Supply Current



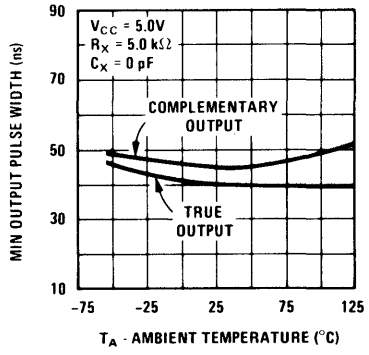
Normalized Output Pulse Width vs Operating Duty Cycle



Pulse Width vs Timing Resistance



Output Pulse Width vs Ambient Temperature



operating rules

1. An external resistor R_X and an external capacitor C_X are required for operation. The value of R_X can vary between the limits shown on tables I and II. The value of C_X is optional and may be adjusted to achieve the required output pulse width.
2. Output pulse width t_{pw} may be calculated as follows:

   $$t_{pw} = 0.32\ R_X C_X \left[1 + \frac{0.7}{R_X}\right] \text{ (for } C_X \geq 10^3 \text{ pF)}$$

   R_X in KΩ, C_X in pF and t_{pw} in ns

   For $C_X < 10^3$ pF, see curve.
3. R_X and C_X must be kept as close as possible to the circuit in order to minimize stray capacitance and noise pickup. If remote trimming is required, R_X may be split up such that at least $R_{X(MIN)}$ must be as close as possible to the circuit and the remote portion of the trimming resistor $R < R_{X(MAX)} - R_X$
4. Set-up time(t_1) for input trigger pulse >40 ns. (See Figure 1)

   Release time(t_2) for input trigger pulse >40 ns. (See Figure 2)
5. Retrigger pulse width (see Figure 3) is calculated as follows:

   $$t_w = t_{pw} + t_{pd+} = 0.32\ R_X C_X \left[1 + \frac{0.7}{R_X}\right] + t_{pd+}$$

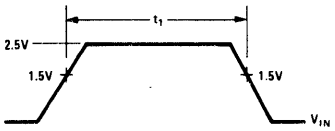


Figure 1

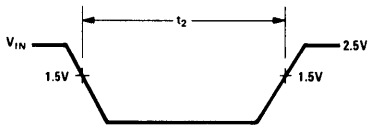


Figure 2

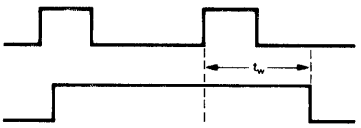
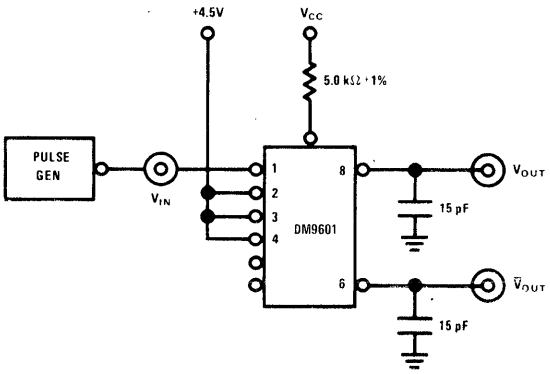
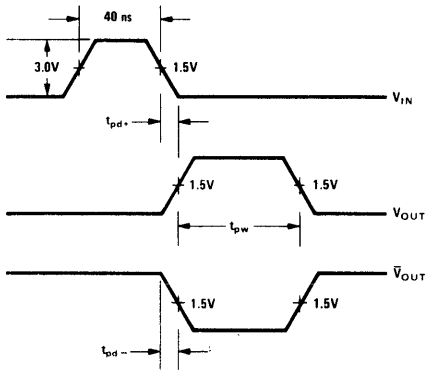


Figure 3

ac test circuit



switching time waveform



NOTE: Capacitance includes Jig and Probe

Interface Gates

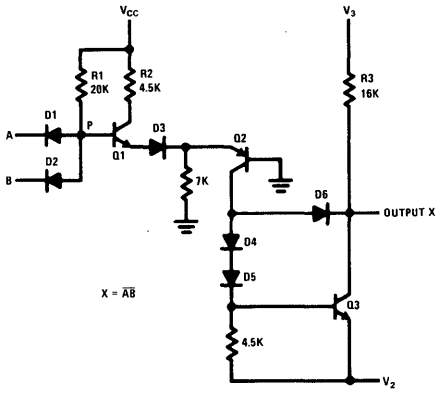
DM7800/DM8800 dual voltage translator general description

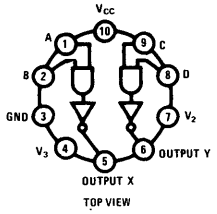
The DM7800/DM8800 are dual voltage translators designed for interfacing between conventional TTL or DTL voltage levels and those levels associated with high impedance junction or MOS FET-type devices. The design allows the user a wide latitude in his selection of power supply voltages, thus providing custom control of the output swing. The translator is especially useful in analog switching; and since low power dissipation occurs in the "off" state, minimum system power is required.

Additional features include:

- 31 volt (max) output swing
- 1 mW power dissipation in normal state
- Standard 5V power supply
- Temperature range:
  DM7800 −55°C to +125°C
  DM8800 0°C to +70°C
- Compatible with all MOS devices

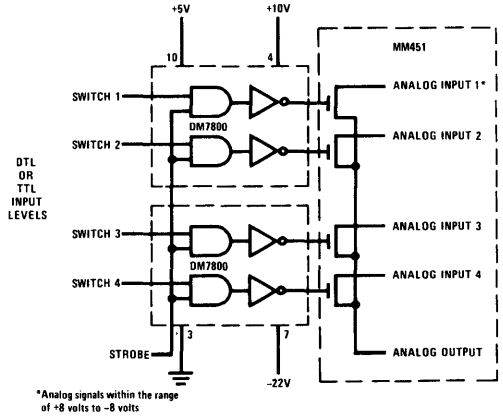
schematic and connection diagram



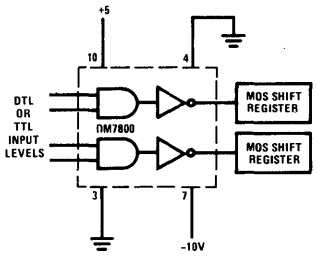


typical applications

4 channel analog switch



bipolar to MOS interfacing



absolute maximum ratings

V_{CC} Supply Voltage	7.0V
V_2 Supply Voltage	−30V
V_3 Supply Voltage	+30V
V_3-V_2 Voltage Differential	40V
Input Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	
DM7800	−55°C to +125°C
DM8800	0°C to 70°C
Lead Temperature (Soldering, 10 sec)	300°C

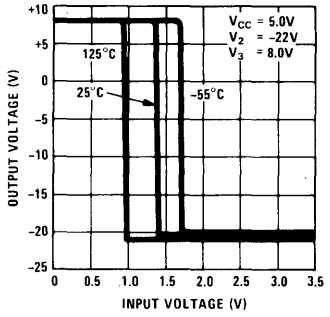
electrical characteristics (Note 1)

PARAMETER		CONDITIONS	MIN	TYP (Note 4)	MAX	UNITS
Logical "1" Input Voltage	DM7800 / DM8800	V_{CC} = 4.5V / V_{CC} = 4.75V	2.0			V
Logical "0" Input Voltage	DM7800 / DM8800	V_{CC} = 4.5V / V_{CC} = 4.75V			0.8	V
Logical "1" Input Current	DM7800 / DM8800	V_{CC} = 5.5V / V_{CC} = 5.25V V_{IN} = 2.4V			5	μA
Logical "1" Input Current	DM7800 / DM8800	V_{CC} = 5.5V / V_{CC} = 5.25V V_{IN} = 5.5V			1	mA
Logical "0" Input Current	DM7800 / DM8800	V_{CC} = 5.5V / V_{CC} = 5.25V V_{IN} = 0.4V		0.2	0.4	mA
Output Leakage Current (Note 2)	DM7800 / DM8800	V_{CC} = 5.5V / V_{CC} = 5.25V V_{IN} = 0.8V (Note 5)			10	μA
Output Collector Resistor		T_A = 25°C	11.5	16.0	20.0	kΩ
Logical "0" Output Voltage	DM7800 / DM8800	V_{CC} = 4.5V / V_{CC} = 4.75V V_{IN} = 2.0V (Note 5)			V_2 + 2.0	V
Power Supply Current Logical "0" (Note 3) (Each Gate)	DM7800 / DM8800	V_{CC} = 5.5V / V_{CC} = 5.25V V_{IN} = 4.5V		0.85	1.6	mA
Power Supply Current Logical "1" (Note 3) (Each Gate)	DM7800 / DM8800	V_{CC} = 5.5V / V_{CC} = 5.25V V_{IN} = 0V		0.22	0.41	mA
Transition Time to Logical "0" Output		T_A = 25°C C = 15 pF	25	70	125	ns
Transition Time to Logical "1" Output		T_A = 25°C C = 15 pF	25	62	125	ns

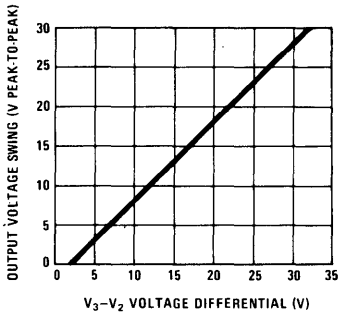
Note 1: Min/max limits apply across the guaranteed temperature range of −55°C to +125°C for the DM7800 and 0°C to +70°C for the DM8800 unless otherwise specified.
Note 2: Current measured is drawn from V_3 supply.
Note 3: Current measured is drawn from V_{CC} supply.
Note 4: All typical values are measured at T_A = 25°C with V_{CC} = 5.0V, V_2 = −22V, V_3 = +8V.
Note 5: Specification applies for all allowable values of V_2 and V_3.

typical performance characteristics (Note 6)

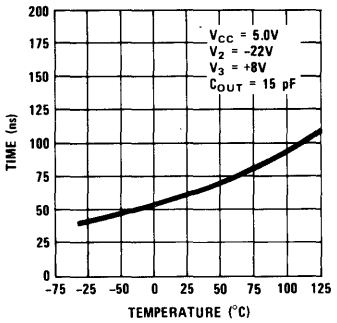
V_{IN}-V_{OUT}



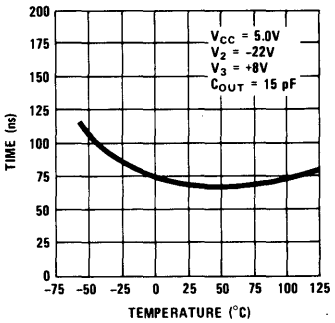
Output Voltage Swing



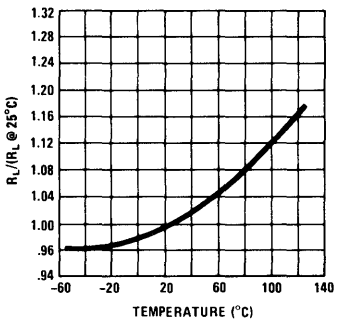
$T_{pd\ 1}$ vs Temperature



$T_{pd\ 0}$ vs Temperature



Logical "1" Output Resistance



Note 6: Curves also describe performance of DM8800 over 0°C to +70°C temperature range.

theory of operation

The two input diodes perform the AND function on TTL or DTL input voltage levels. When at least one input voltage is a logical "0", current from V_{CC} (nominally 5.0V) passes through R_1 and out the input(s) which is at the low voltage. Other than small leakage currents, this current drawn from V_{CC} through the 20 kΩ resistor is the only source of power dissipation in the logical "1" output state.

When both inputs are at logical "1" levels, current passes through R_1 and diverts to transistor Q_1, turning it on and thus pulling current through R_2. Current is then supplied to the PNP transistor, Q_2. The voltage losses caused by current through Q_1, D_3, and Q_2 necessitate that node P reach a voltage sufficient to overcome these losses before current begins to flow. To achieve this voltage at node P, the inputs must be raised to a voltage level which is one diode potential lower than node P. Since these levels are exactly the same as those experienced with conventional TTL and DTL, the interfacing with these types of circuits is achieved.

Transistor Q_2 provides "constant current switching" to the output due to the common base connection of Q_2. When at least one input is at the logical "0" level, no current is delivered to Q_2; so that its collector supplies essentially zero current to the output stage. But when both inputs are raised to a logical "1" level current is supplied to Q_2. Since this current is relatively constant, the collector of Q_2 acts as a constant current source for the output stage. Logic inversion is performed since logical "1" input voltages cause current to be supplied to Q_2 and to Q_3. And when Q_3 turns on the output voltage drops to the logical "0" level.

The reason for the PNP current source, Q_2, is so that the output stage can be driven from a high impedance. This allows voltage V_2 to be adjusted in accordance with the application. Negative voltages to –25V can be applied to V_2. Since the output will neither source nor sink large amounts of current, the output voltage range is almost exclusively dependent upon the values selected for V_2 and V_3.

Maximum leakage current through the output transistor Q_3 is specified at 10 μA under worst-case voltage between V_2 and V_3. This will result in a logical "1" output voltage which is 0.2V below V_3. Likewise the clamping action of diodes D_4, D_5, and D_6, prevents the logical "0" output voltage from falling lower than 2V above V_2, thus establishing the output voltage swing at typically 2 volts less than the voltage separation between V_2 and V_3.

Interface Gates

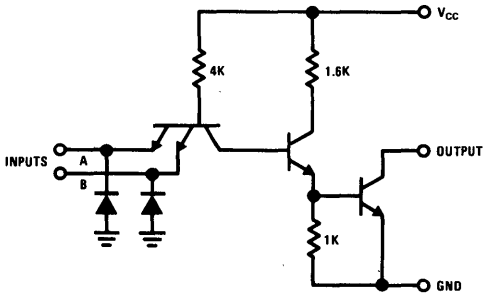
DM8810 quad two-input TTL-MOS interface gate
DM8811 quad two-input TTL-MOS interface gate
DM8812 TTL-MOS hex inverter

general description

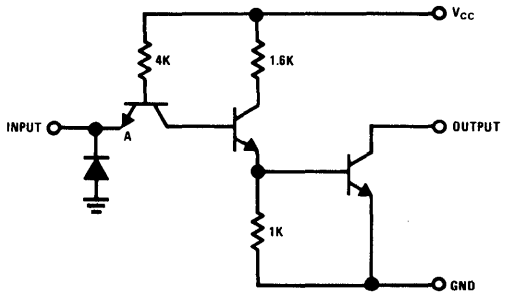
These Series 74 compatible gates are high output voltage versions of the DM7401 (SN7401), DM7403 (SN7403), and DM7405 (SN7405). Their open-collector outputs may be "pulled-up" to +14 volts in the logical "1" state thus providing guaranteed interface between TTL and MOS logic levels.

In addition the devices may be used in applications where it is desirable to drive low current relays or lamps that require up to 14 volts.

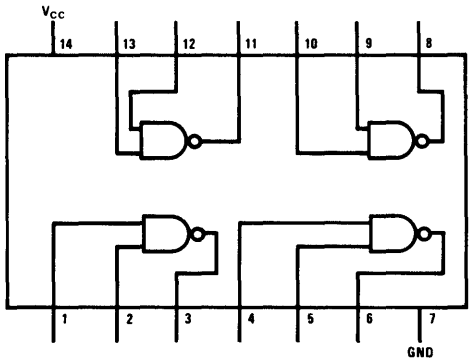
schematic and connection diagrams



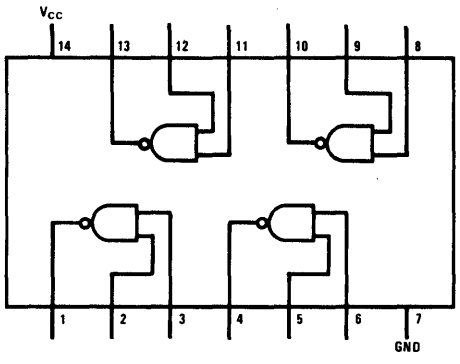
DM8810 and DM8811



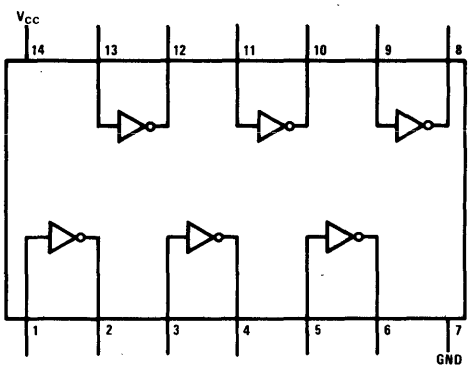
DM8812



DM8810



DM8811



DM8812

absolute maximum ratings

V_{CC}	7V
Input Voltage	5.5V
Output Voltage	14.V
Operating Temperature Range	0°C to 70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

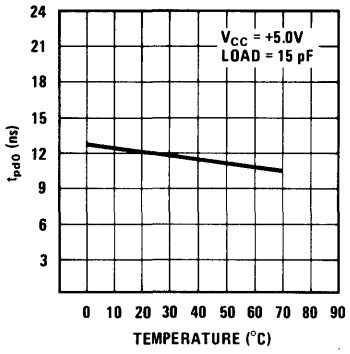
electrical characteristics (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Diode Clamp Voltage	V_{CC} = 5.0V, T_A = 25°C I_{IN} = −12 mA			−1.5	V
Logical "1" Input Voltage	V_{CC} = 4.75V	2.0			V
Logical "0" Input Voltage	V_{CC} = 4.75V			0.8	V
Logical "1" Output Current	V_{CC} = 4.75V, V_{IN} = 0.8V V_{OUT} = 10V, $\overline{V_{IN} = 0.0V}$			250 40	μA μA
Logical "1" Output Breakdown Voltage	V_{CC} = 4.75V, V_{IN} = 0V I_{OUT} = 1 mA	14			V
Logical "0" Output Voltage	V_{CC} = 4.75V, V_{IN} = 2.0V I_{OUT} = 16 mA			0.4	V
Logical "1" Input Current	V_{CC} = 5.25V, V_{IN} = 2.4V			40	μA
Logical "1" Input Current	V_{CC} = 5.25V, V_{IN} = 5.5V			1	mA
Logical "0" Input Current	V_{CC} = 5.25V, V_{IN} = 0.4V			−1.6	mA
Supply Current — Logical "0" (Each Gate)	V_{CC} = 5.25V, V_{IN} = 5.0V		3.0	5.1	mA
Supply Current — Logical "1" (Each Gate)	V_{CC} = 5.25V, V_{IN} = 0V		1.0	1.8	mA
Propagation Delay Time to a Logical "0", t_{pd0}	V_{CC} = 5.0V, T_A = 25°C C_{OUT} = 15 pF, R_L = 1k	4	12	18	ns
Propagation Delay Time to a Logical "1", t_{pd1}	V_{CC} = 5.0V, T_A = 25°C C_{OUT} = 15 pF, R_L = 1k	18	29	45	ns

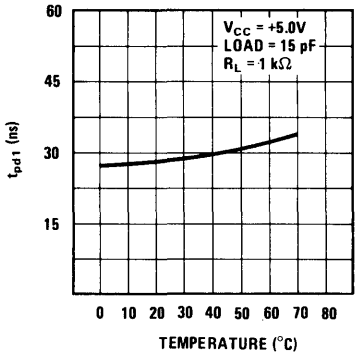
Note 1: Min/Max units apply across the guaranteed temperature range of 0°C to 70°C unless otherwise specified. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

typical performance characteristics

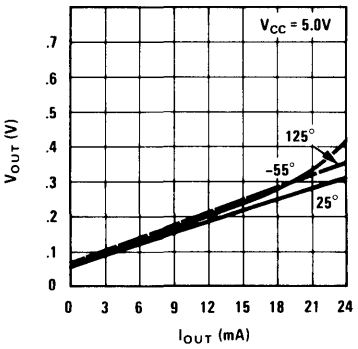
Transition Time to a Logical "0" (t_{pd0}) vs Temperature



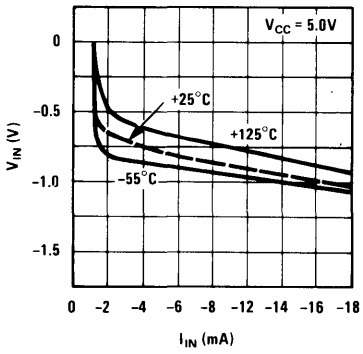
Transition Time to a Logical "1" (t_{pd1}) vs Temperature



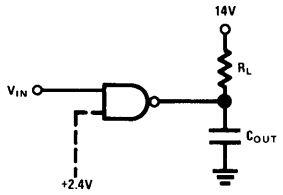
V_{OUT} vs I_{OUT} Logical "0"



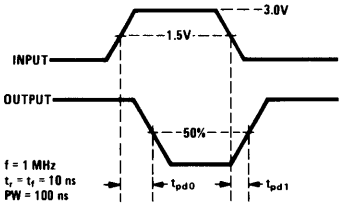
Input Clamp Diode Characteristics



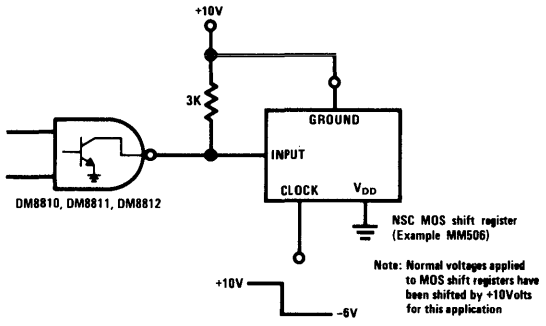
ac test circuit

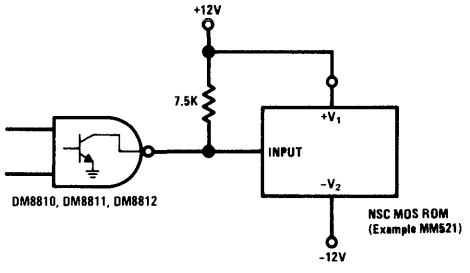


switching time waveform



typical applications





Interface Gates

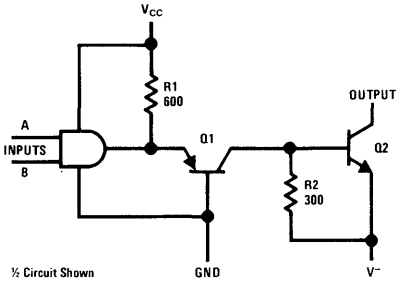
DH0034/DH0034C high speed dual level translator

general description

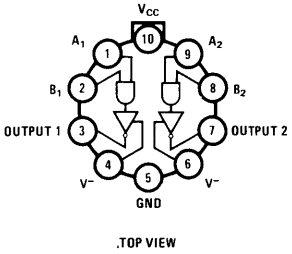
The DH0034/DH0034C is a high speed level translator suitable for interfacing to MOS or junction FET analog switches. It may also be used as a universal logic level shifter capable of accepting TTL/DTL input levels and shifting to CML, MOS, or SLT levels. Other important design features include:

- Fast switching, t_{pd0}: typically 15 ns; t_{pd1}: typically 35 ns
- Large output voltage range: 25V
- Input is TTL/DTL compatible
- Low output leakage: typically 0.1 μA
- High output currents: up to ±100 mA

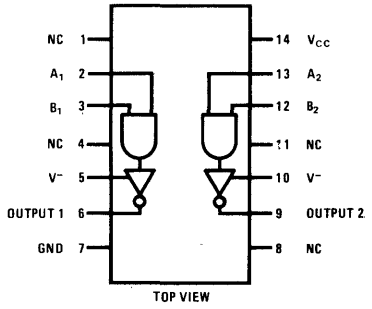
schematic and connection diagrams



Metal Can Package

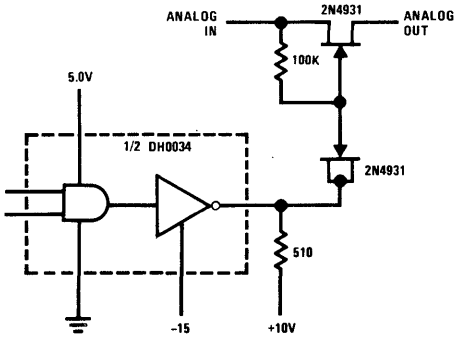


Dual-in-Line Package

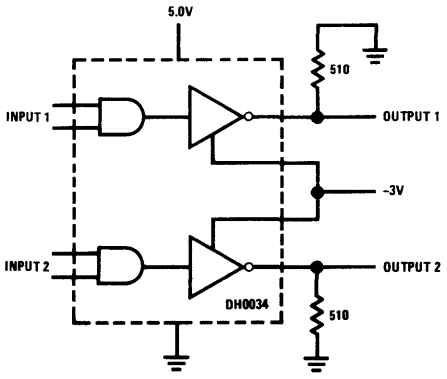


typical applications

5 MHz Analog Switch



TTL to IBM (SLT) Logic Levels



absolute maximum ratings

V_{CC} Supply Voltage		7.0V
Negative Supply Voltage		−30V
Positive Supply Voltage		+25V
Differential Supply Voltage		25V
Maximum Output Current		100 mA
Input Voltage		+5.5V
Operating Temperature Range:	DH0034	−55°C to +125°C
	DH0034C	0°C to +85°C
Storage Temperature Range		−65°C to +150°C
Lead Temperature (Soldering, 10 sec)		300°C

electrical characteristics (See Notes 1 & 2)

PARAMETER	CONDITIONS	DH0034			DH0034C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Logical "1" Input Voltage	V_{CC} = 4.5V	2.0						V
	V_{CC} = 4.75V				2.0			
Logical "0" Input Voltage	V_{CC} = 5.5V			0.8				V
	V_{CC} = 4.75V						0.8	
Logical "1" Input Current	V_{CC} = 5.5V, V_{IN} = 2.4V			40				μA
	V_{CC} = 5.25V, V_{IN} = 2.4V						40	
Logical "1" Input Current	V_{CC} = 5.5V, V_{IN} = 5.5V			1.0				mA
	V_{CC} = 5.25V, V_{IN} = 5.5V						1.0	
Logical "0" Input Current	V_{CC} = 5.5V, V_{IN} = 0.4V			1.6				mA
	V_{CC} = 5.25V, V_{IN} = 0.4V						1.6	
Power Supply Current Logic "0"	(Note 3) V_{CC} = 5.5V, V_{IN} = 4.5V		30	32				mA
	V_{CC} = 5.25V, V_{IN} = 4.5V					30	32	
Power Supply Current Logic "1"	(Note 3) V_{CC} = 5.5V, V_{IN} = 0V		37	42				mA
	V_{CC} = 5.25V, V_{IN} = 0V					37	42	
Logical "0" Output Voltage	V_{CC} = 4.5V, I_{OUT} = 100 mA		V^- + .50	V^- + .75		V^- + .50	V^- + .80	V
	V_{CC} = 4.5V, I_{OUT} = 50 mA		V^- + .3	V^- + .50		V^- + .3	V^- + .65	V
Output Leakage Current	V_{CC} = 5.5V, V_{IN} = 0.8V $V^+ - V^-$ = 25V		0.1	5		0.1	5	μA
Transition Time to Logical "0"	V_{CC} = 5.0V, V_3 = 0V V^- = −25V, R_L = 510Ω		15	25		15	35	ns
Transition Time to Logical "1"	V_{CC} = 5.0V, V^- = −25V, R_L = 510Ω		35	60		35	65	ns

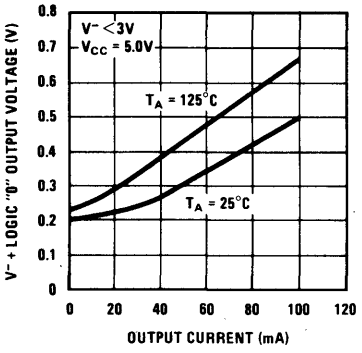
Note 1: These specifications apply over the temperature range −55°C to +125°C for the DH0034 and 0°C to +85°C for the DH0034C with a 510 ohm resistor connected between output and ground, and V^- connected to −25V.

Note 2: All typical values are for T_A = 25°C.

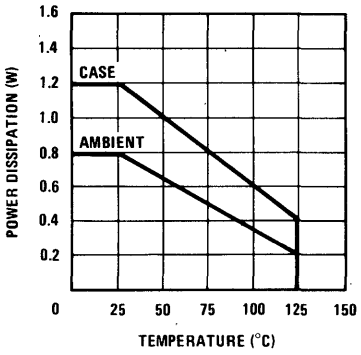
Note 3: Current measured is total drawn from V_{CC} supply.

typical performance characteristics

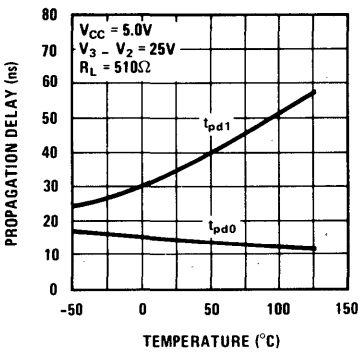
Logic "0" Output Voltage vs I_{OUT}



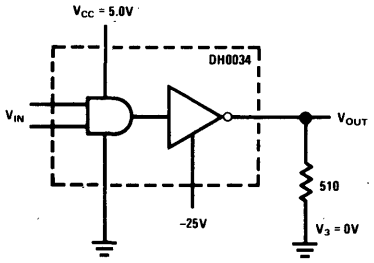
Maximum Power Dissipation

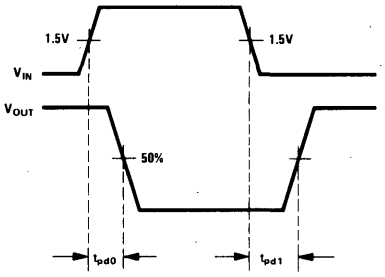


Propagation Delay vs Temperature



ac test circuit and waveforms





theory of operation

When both inputs of the DH0034 are raised to logic "1", the input AND gate is turned "on" allowing Q1's emitter to become forward biased. Q1 provides a level shift and constant output current. The collector current is essentially the same as the emitter which is given by $\frac{V_{CC} - V_{BE}}{R1}$ Approximately 7.0 mA flows out of Q1's collector.

About 2 mA of Q1's collector current is drawn off by pull down resistor, R2. The balance, 5 mA, is available as base drive to Q2 and to charge its associated Miller capacitance. The output is pulled to within a V_{SAT} of V^-. When either (or both) input to the DH0034 is lowered to logic "0," the AND gate output drops to 0.2V turning Q1 off. Deprived of base drive Q2 rapidly turns off causing the output to rise to the V_3 supply voltage. Since Q2's emitter operates between 0.6V and 0.2V, the speed of the DH0034 is greatly enhanced.

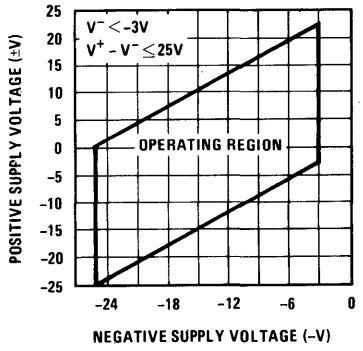
applications information

1. Paralleling the Outputs

The outputs of the DH0034 may be paralleled to increase output drive capability or to accomplish the "wire OR". In order to prevent current hogging by one output transistor or the other, resistors of 2 ohms/100 mA value should be inserted between the emitters of the output transistors and the minus supply.

2. Recommended Output Voltage Swing

The graph shows boundary conditions which govern proper operation of the DH0034. The range of operation for the negative supply is shown on the X axis and must be between -3V and -25V. The allowable range for the positive supply is governed by the value chosen for V^-. V^+ may be selected by drawing a vertical line through the selected value for V^- and terminated by the boundaries of the operating region. For example, a value of V^- equal to -6V would dictate values of



V^+ between -5V and +19V. In general, it is desirable to maintain at least 5V difference between the supplies.

Line Receivers/Drivers

DM7820A/DM8820A dual line receiver

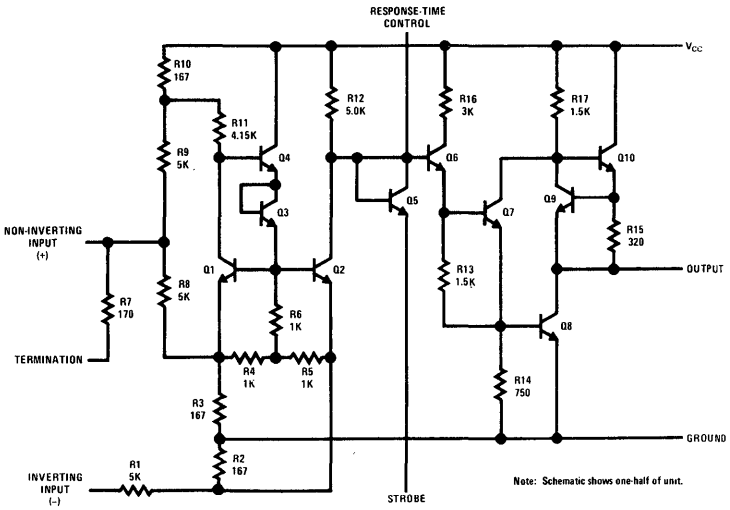
general description

The DM7820A and the DM8820A are improved performance digital line receivers with two completely independent units fabricated on a single silicon chip. Intended for use with digital systems connected by twisted pair lines, they have a differential input designed to reject large common mode signals while responding to small differential signals. The output is directly compatible with RTL, DTL or TTL integrated circuits. Some important design features include:

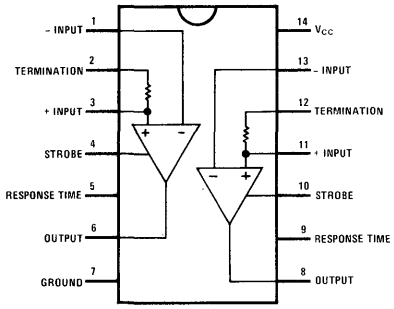
- Operation from a single +5V logic supply
- Input voltage range of ±15V
- Strobe low forces output to "1" state
- High input resistance
- Fanout of ten with either DTL or TTL integrated circuits
- Outputs can be wire OR'ed
- Series 54/74 compatible

The response time can be controlled with an external capacitor to reject input noise spikes. The output state is a logic "1" for both inputs open. Termination resistors for the twisted pair line are also included in the circuit. Both the DM7820A and the DM8820A are specified, worst case, over their full operating temperature range (−55°C to 125°C and 0°C to 70°C respectively), over the entire input voltage range, for ±10% supply voltage variations.

schematic and connection diagrams



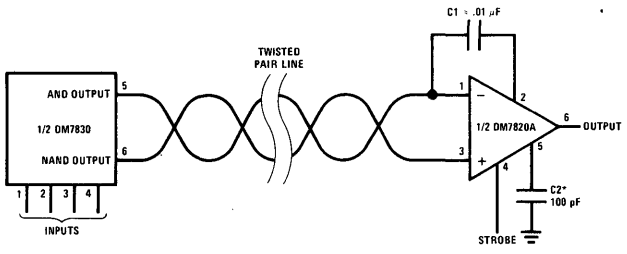
Dual-In-Line Package



Note: Pin 7 connected to bottom of cavity package.
TOP VIEW

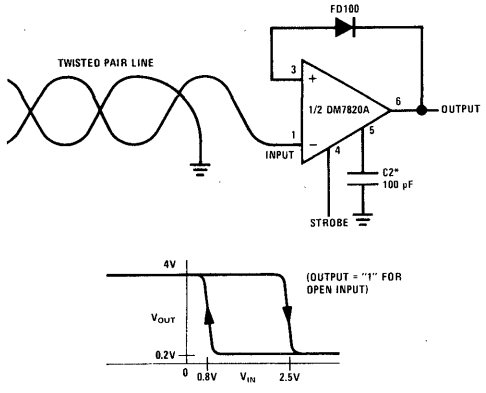
typical applications

Differential Line Driver and Receiver



*Optional to control response time.

Single Ended (EIA-RS232C) Receiver with Hysteresis



absolute maximum ratings

Supply Voltage	8.0V
Common-Mode Voltage	±20V
Differential Input Voltage	±20V
Strobe Voltage	8.0V
Output Sink Current	50 mA
Power Dissipation (Note 1)	600 mW
Operating Temperature Range	
DM7820A	−55°C to 125°C
DM8820A	0°C to 70°C
Storage Temperature Range	−65°C to 150°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics (Notes 2, 3 & 4)

PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
	V_{CM}	OUTPUT	OTHER				
Differential Threshold Voltage	$-3V \le V_{CM} \le +3V$	−400 μA	$V_{OUT} \ge 2.5V$		+0.06	+0.5	V
	$-15V \le V_{CM} \le +15V$	−400 μA	$V_{OUT} \ge 2.5V$		+0.06	+1.0	V
	$-3V \le V_{CM} \le +3V$	+16 mA	$V_{OUT} \le 0.4V$		−0.08	−0.5	V
	$-15V \le V_{CM} \le +15V$	+16 mA	$V_{OUT} \le 0.4V$		−0.08	−1.0	V
Inverting Input Resistance	$-15V \le V_{CM} \le +15V$			3.6	5		kΩ
Non-Inverting Input Resistance	$-15V \le V_{CM} \le +15V$			1.8	2.5		kΩ
Line Termination Resistance			$T_A = 25°C$	120	170	250	Ω
Inverting Input Current	+15V				+3.0	+4.2	mA
	0V				0	−0.5	mA
	−15V				−3.0	−4.2	mA
Non-Inverting Input Current	+15V				+5.0	+7.0	mA
	0V				−1.0	−1.4	mA
	−15V				−7.0	−9.8	mA
Power Supply Current	+15V	Logic "0"	$V_{DIFF} = -1V$		+3.9	+6.0	mA
	0V	Logic "0"	$V_{DIFF} = -0.5V$		+6.5	+10.2	mA
	−15V	Logic "0"	$V_{DIFF} = -1V$		+9.2	+14.0	mA
Logical "1" Output Voltage		−400 μA	$V_{DIFF} = +1V$	2.5	4.0	5.5	V
Logical "0" Output Voltage		+16 mA	$V_{DIFF} = -1V$	0	0.22	0.4	V
Logical "1" Strobe Input Voltage		+16 mA	$V_{OUT} \le 0.4V$, $V_{DIFF} = -3V$	2.1			V
Logical "0" Strobe Input Voltage		−400 μA	$V_{OUT} \ge 2.5V$, $V_{DIFF} = -3V$			0.9	V
Logical "1" Strobe Input Current			$V_{STROBE} = 5.5V$, $V_{DIFF} = +3V$		0.01	5.0	μA
Logical "0" Strobe Input Current			$V_{STROBE} = 0V$, $V_{DIFF} = -3V$		−1.0	−1.4	mA
Output Short Circuit Current		0V	$V_{CC} = 5.5V$, $V_{STROBE} = 0V$	−2.8	−4.5	−6.7	mA
Propagation Delays: (see waveforms)							
Differential Input to "0" Output			$V_{CC} = 5V$, $T_A = 25°C$		30	45	ns
Differential Input to "1" Output			$V_{CC} = 5V$, $T_A = 25°C$		24	40	ns
Strobe Input to "0" Output			$V_{CC} = 5V$, $T_A = 25°C$		16	25	ns
Strobe Input to "1" Output			$V_{CC} = 5V$, $T_A = 25°C$		18	30	ns

Note 1: For operating at elevated temperatures, the device must be derated based on a thermal resistance of 100°C/W and a maximum junction temperature of 160°C for the DM7820A, or 150°C/W and 115°C maximum junction temperature for the DM8820A.

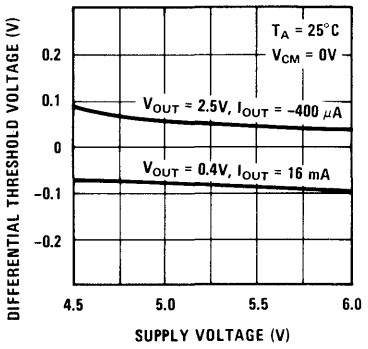
Note 2: These specifications apply for $4.5V \le V_{CC} \le 5.5V$, $-15V \le V_{CM} \le 15V$ and $-55°C \le T_A \le 125°C$ for the DM7820A or $0°C \le T_A \le 70°C$ for the DM8820A unless otherwise specified. Typical values given are for $V_{CC} = 5.0V$, $T_A = 25°C$ and $V_{CM} = 0V$ unless stated differently.

Note 3: The specifications and curves given are for one side only. Therefore, the total package dissipation and supply currents will be double the values given when both receivers are operated under identical conditions.

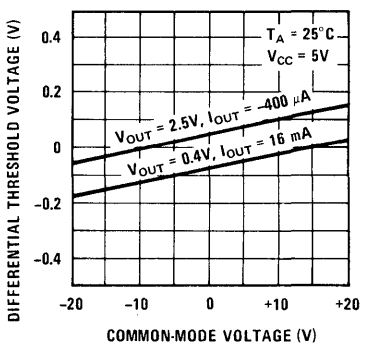
Note 4: Min and max limits apply to absolute values.

typical performance characteristics (Note 3)

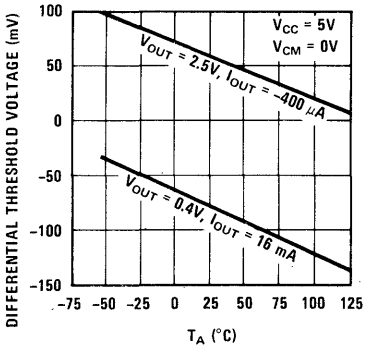
Supply Voltage Sensitivity



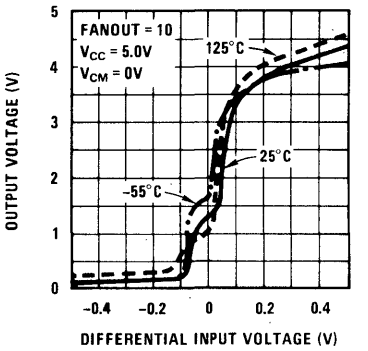
Common-Mode Voltage Sensitivity



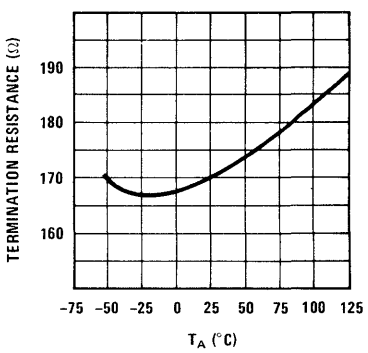
Temperature Sensitivity



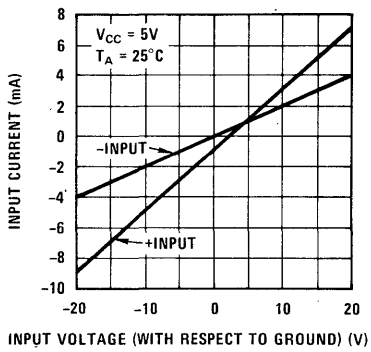
Transfer Function



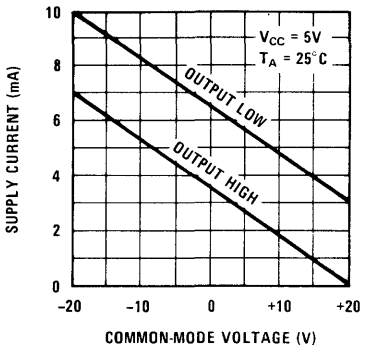
Termination Resistance



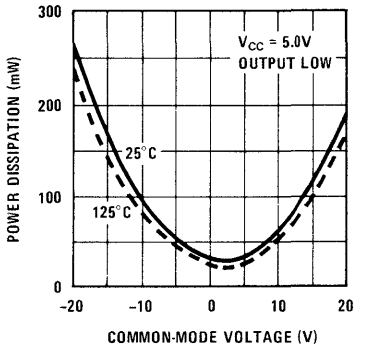
Input Characteristics



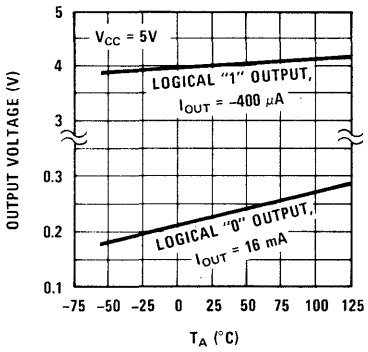
Power Supply Current



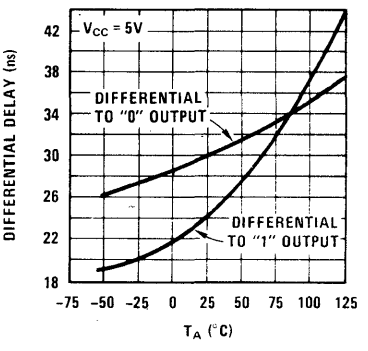
Internal Power Dissipation



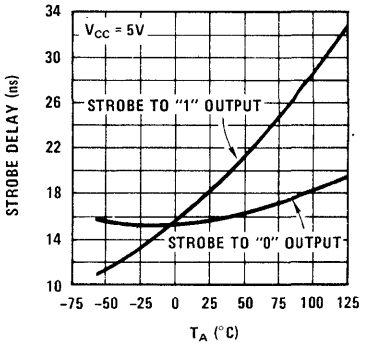
Output Voltage Levels



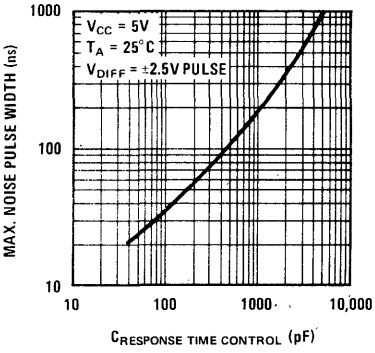
Differential Input Delays



Strobe Delays



Noise Rejection



definition of terms

Differential Voltage (V_{DIFF}): The applied voltage between the differential inputs with respect to the inverting (–) input.

Common-Mode Voltage (V_{CM}): The average applied D.C. voltage, with respect to ground (pin 7), of the two differential inputs.

Differential Threshold Voltages: The differential voltages required to secure the output in either the logical "1" or "0" state.

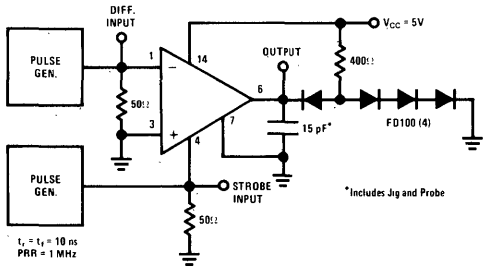
Input Resistance: The ratio of the change in input voltage to the change in input current.

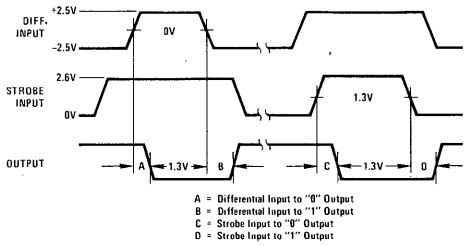
Line Termination Resistance: The ohmic value of the line termination resistor in the integrated circuit.

Current: Positive current is defined as current into the referenced pin.

Noise Rejection: The maximum pulse width of a ±2.5 volt ($t_r = t_f = 1$ ns) differentially applied noise pulse which will not change the output logic state.

ac test circuit and waveforms





Line Receivers/Drivers

DM7822/DM8822 dual line receiver

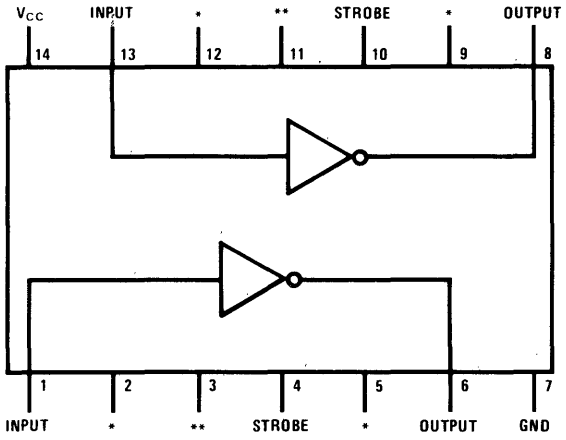
general description

The DM7822/DM8822 is a dual inverting line receiver which meets the requirements of EIA specification RS232 Revision B. The device contains both receivers on a single monolithic silicon chip. The receivers share common power supply and ground connections, otherwise their operation is fully independent.

In addition to meeting the requirements of RS232, the DM7822/DM8822 also has independent strobe inputs which allow the receiver to be placed in the high state independent of the information being received at the input.

The output of the DM7822/DM8822 is completely compatible with five volt DTL and TTL logic families.

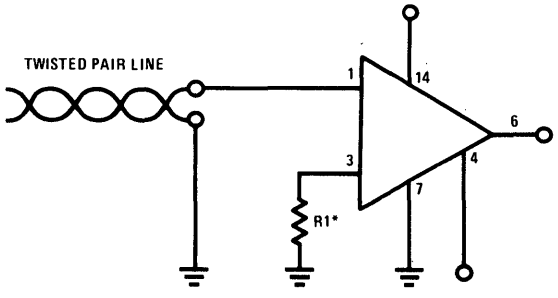
connection diagram



*Make no connection to these pins.

**For operation requiring "Mark Hold" with the input open connect a 470Ω resistors from each of these pins to ground.

typical connection



*For Mark Hold R1 = 470Ω, otherwise connect pin 3 to ground.

absolute maximum ratings

Supply Voltage		8.0V
Input Voltage		±30V
Strobe Voltage		8.0V
Output Sink Current		25 mA
Power Dissipation (Note 1)		600 mW
Operating Temperature Range	DM7822	−55°C to +125°C
	DM8822	0°C to 70°C
Storage Temperature Range		−65°C to +150°C
Lead Temperature (Soldering, 10 sec)		300°C

electrical characteristics (Note 2)

PARAMETER	PARAGRAPH IN RS-232	CONDITIONS	MIN	TYP	MAX	UNITS
Negative Input Threshold Voltage	4.8 (8)	$V_{OUT} \geq 2.5V$	−2.0			V
Positive Input Threshold Voltage (Note 3)		$V_{OUT} \leq 0.4V$			2.0	V
Input Resistance	4.5 and 4.8 (5)		3.0	5.0	7.0	kΩ
Input Current		$V_{IN} = 25V$	3.57	5	8.33	mA
		$V_{IN} = 0V$		0		mA
		$V_{IN} = -25V$	−8.33	−5	−3.57	mA
Open Circuit Input Voltage	4.5 and 4.8 (4)	$V_{IN} = 0V$		.03	0.5	V
Logical "1" Output Voltage		$I_{OUT} \leq -0.2$ mA	2.5			V
Logical "0" Output Voltage		$I_{OUT} = 3.5$ mA			0.4	V
Strobe Current		$V_{STROBE} = 0V$		1.0	1.4	mA
		$V_{STROBE} = 5.5V$		−5.0 μA	−1.0 mA	
Power Supply Current (Both Receivers)		$-25V \leq V_{IN} \leq 25V$			24.0	mA
Response Time, t_1 or t_2		$T_A = 25°C$, $V_{CC} = 5.0V$, Input Ramp Rate $\leq$ 10 ns		65	125	ns

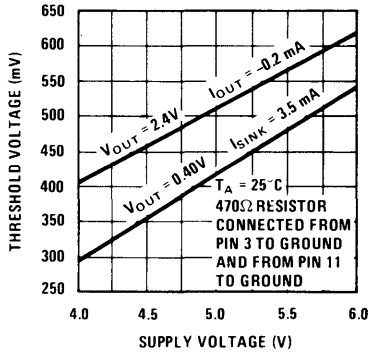
Note 1. For operating at elevated temperatures, the device must be derated in accordance with the "Maximum Power Dissipation" curve.

Note 2. Min/Max limits apply across the guaranteed temperature range of −55°C to +125°C for the DM7822 and 0°C to 70°C for the DM8822 unless otherwise specified. Likewise the limits apply across the guaranteed V_{CC} range of 4.5V to 5.5V for the DM7822 and 4.75V to 5.25V for the DM8822 unless otherwise specified. Typical values are given for $V_{CC} = 5.0V$ and $T_A = 25°C$.

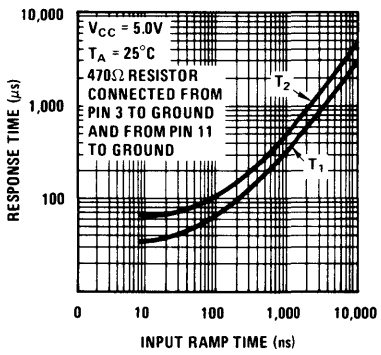
Note 3. Since the EIA RS-232 specification requires the threshold to be between −3V and +3V, the immunity limits shown here guarantee 1 volt additional noise immunity.

typical performance characteristics

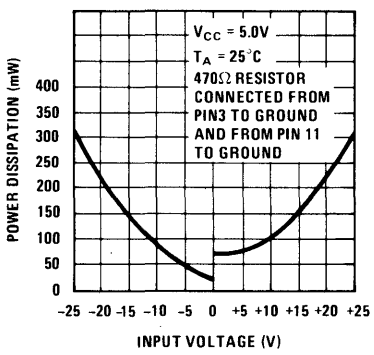
Threshold Voltage vs Supply Voltage



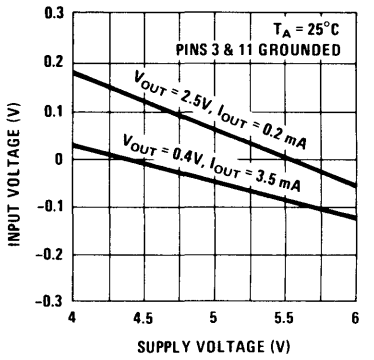
Response Time vs Input Ramp Time



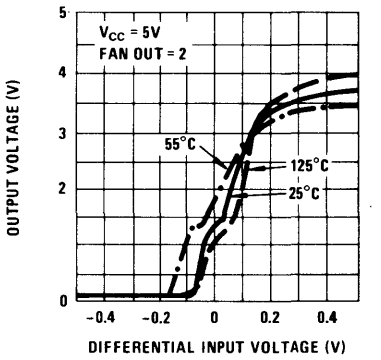
Internal Power Dissipation



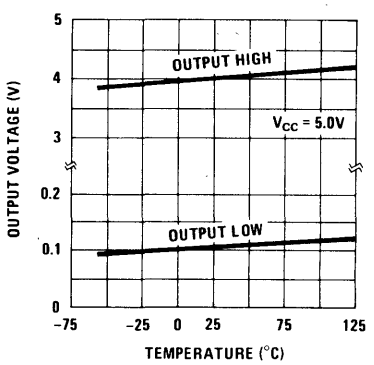
Threshold Voltage vs Supply Voltage



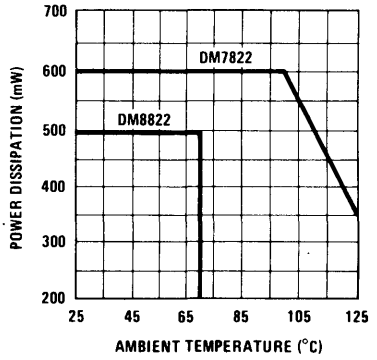
Transfer Function



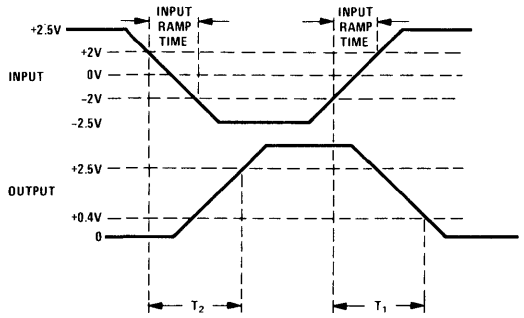
Output Voltage Levels



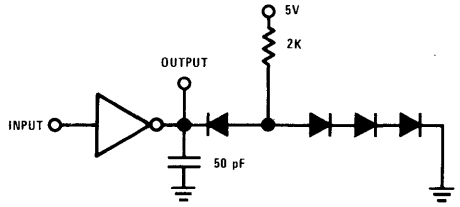
Maximum Power Dissipation



switching time waveforms



ac test circuit



Line Receivers/Drivers

DM7830/DM8830 dual differential line driver

general description

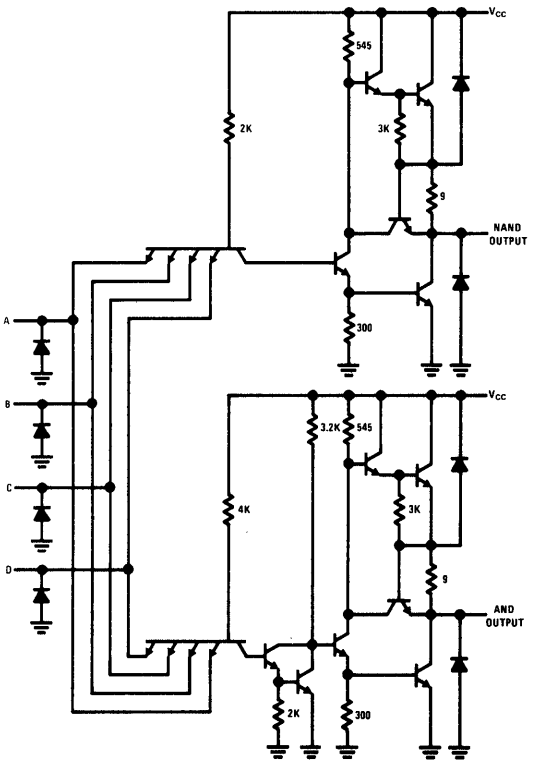
The DM7830/DM8830 is a dual differential line driver that also performs the dual four-input NAND or dual four-input AND function.

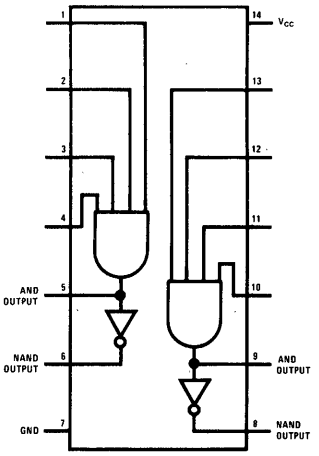
TTL (Transistor-Transistor-Logic) multiple emitter inputs allow this line driver to interface with standard TTL or DTL systems. The differential outputs are balanced and are designed to drive long lengths of coaxial cable, strip line, or twisted pair transmission lines with characteristic impedances of 50Ω to 500Ω. The differential feature of the output eliminates troublesome ground-loop errors normally associated with single-wire transmissions.

Key Features:

- Single 5 volt power supply
- Diode protected outputs for termination of positive and negative voltage transients
- Diode protected inputs to prevent line ringing
- High Speed
- Short Circuit Protection

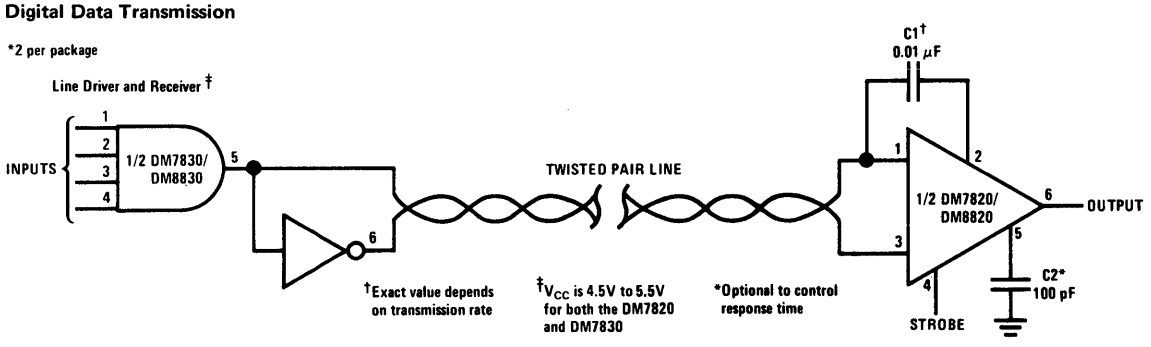
schematic* and connection diagram





typical application

Digital Data Transmission



absolute maximum ratings

V_{CC}		7.0V
Input Voltage		5.5V
Operating Temperature	DM7830	−55°C to +125°C
	DM8830	0°C to 70°C
Storage Temperature		−65°C to +150°C
Lead Temperature (soldering, 60 sec)		300°C
Output Short Circuit Duration (125°C)		1 second

electrical characteristics (Note 1)

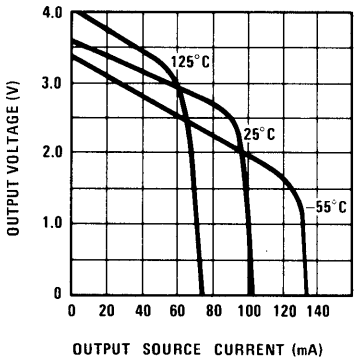
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Logical "1" Input Voltage		2.0			V
Logical "0" Input Voltage				0.8	V
Logical "1" Output Voltage	V_{IN} = 0.8V I_{OUT} = −0.8 mA	2.4			V
Logical "1"Output Voltage	V_{IN} = 0.8V I_{OUT} = 40 mA	1.8	3.3		V
Logical "0" Output Voltage	V_{IN} = 2.0V I_{OUT} = +32 mA		0.2	0.4	V
Logical "0" Output Voltage	V_{IN} = 2.0V I_{OUT} = +40 mA		0.22	0.5	V
Logical "1" Input Current	V_{IN} = +2.4V			120	μA
Logical "1" Input Current	V_{IN} = 5.5V			2	mA
Logical "0" Input Current	V_{IN} = 0.4V			4.8	mA
Output Short Circuit Current	V_{CC} = 5.0V	Note 2 40	100	Note 2 120	mA
Supply Current	V_{CC} = 5.0V V_{IN} = 5.0V (Each Driver)		11	18	mA
Propagation Delay AND Gate t_{pd1}	T_A = 25°C		8	12	ns
t_{pd0}	V_{CC} = 5.0V		11	18	ns
Propagation Delay NAND Gate t_{pd1}	C_L = 15 pF		8	12	ns
t_{pd0}	See Figure 1		5	8	ns
Differential Delay t_1	Load, 100Ω and 5000 pF		12	16	ns
Differential Delay t_2	See Figure 2		12	16	ns

Note 1: Specifications apply for DM7830 −55°C ≤ T_A ≤ +125°C, V_{CC} = +5V ±10%, DM8830 0°C ≤ T_A ≤ 70°C, V_{CC} = +5V ±5% unless otherwise stated. Typical values given are for T_A = 25°C, V_{CC} = 5.0V.

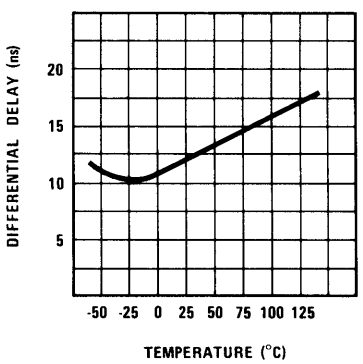
Note 2: Applies for T_A = +125°C only.

typical performance characteristics

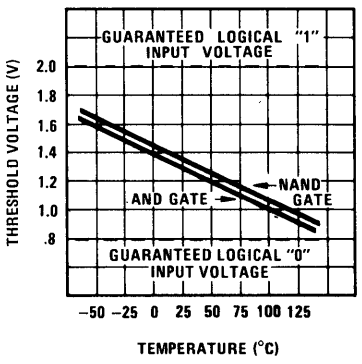
Output High Voltage (Logical "1") Vs Output Current



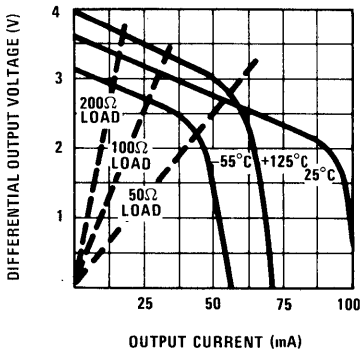
Differential Delay Vs Temperature



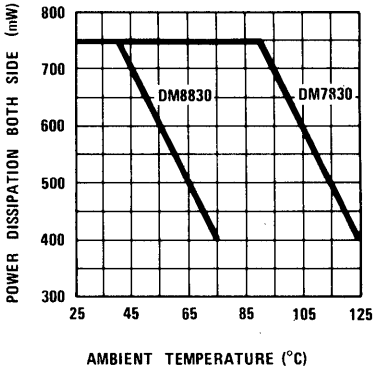
Threshold Voltage Vs Temperature



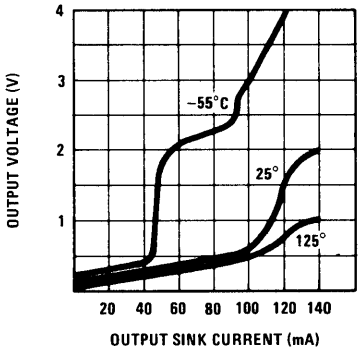
Differential Output Voltage ($|V_{AND} - V_{NAND}|$) Vs Differential Output Current



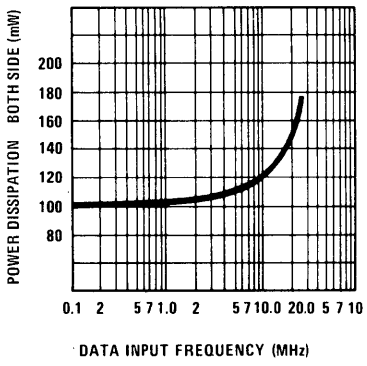
Maximum Power Dissipation



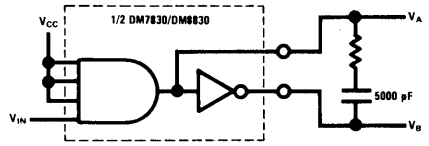
Output Low Voltage (Logical "0") Vs Output Current



Power Dissipation (No Load) Vs Data Input Frequency



ac test circuit



switching time waveforms

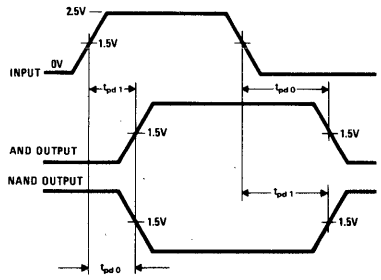


FIGURE 1

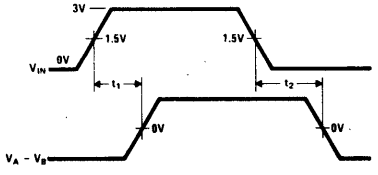


FIGURE 2

Current Drivers

NH0006/NH0006C current driver

general description

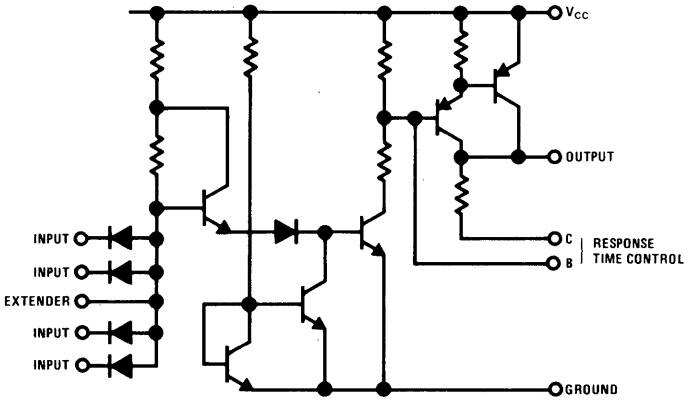
The NH0006/NH0006C is an integrated high voltage, high current driver designed to accept standard DTL or TTL logic levels and drive a load of up to 400 mA at 28 volts. AND inputs are provided along with an Expander connection, should additional gating be required. The addition of an external capacitor provides control of the rise and fall times of the output in order to decrease cold lamp surges or to minimize electromagnetic interference if long lines are driven.

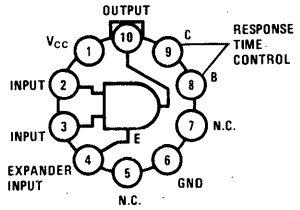
Since one side of the load is normally grounded, there is less likelihood of false turn-on due to an inadvertent short in the drive line.

Some important design features include:

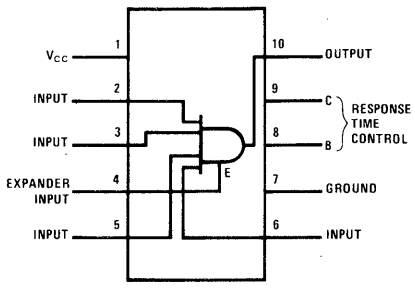
- Operation from a Single +10V to +45V Power Supply.
- Low Standby Power Dissipation of only 35 mW for 28V Power Supply.
- 1.5A, 50 ms, Pulse Current Capability.

schematic and connection diagrams



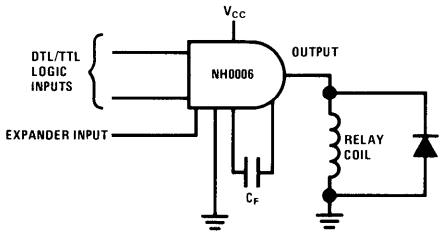


TOP VIEW

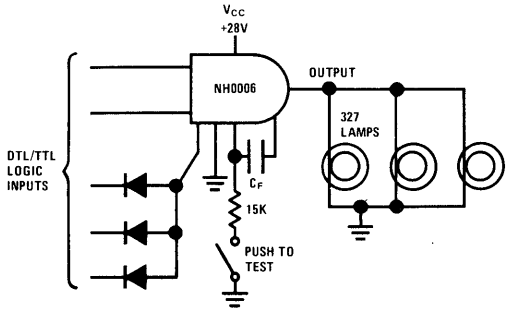


typical applications

Relay Driver



Lamp Driver with Expanded Inputs



absolute maximum ratings

Peak Power Supply Voltage (for 0.1 sec)	60V
Continuous Supply Voltage	45V
Input Voltage	5.5V
Input Extender Current	5.0 mA
Peak Output Current (50 ms On/1 sec Off)	1.5A
Operating Temperature	
NH0006	−55°C to +125°C
NH0006C, NH0006CN	0°C to +70°C
Storage Temperature	−65°C to +150°C

electrical characteristics (Note 1)

PARAMETER	CONDITIONS	MIN	TYP (Note 2)	MAX	UNITS
Logical "1" Input Voltage	V_{CC} = 45V to 10V	2.0			V
Logical "0" Input Voltage	V_{CC} = 45V to 10V			0.8	V
Logical "1" Output Voltage	V_{CC} = 28V, V_{IN} = 2.0V, I_{OUT} = 400 mA	26.5	27.0		V
Logical "0" Output Voltage	V_{CC} = 45V, V_{IN} = 0.8V, R_L = 1K		.001	.01	V
Logical "1" Output Voltage	V_{CC} = 10V, V_{IN} = 2.0V, I_{OUT} = 150 mA	8.8	9.2		V
Logical "0" Input Current	V_{CC} = 45V, V_{IN} = .4V		0.8	1.0	mA
Logical "1" Input Current	V_{CC} = 45V, V_{IN} = 2.4V		0.5	5.0	μA
	V_{CC} = 45V, V_{IN} = 5.5V			100	μA
"Off" Power Supply Current	V_{CC} = 45V, V_{IN} = 0.8V		1.6	2.0	mA
"On" Power Supply Current	V_{CC} = 45V, V_{IN} = 2.0V, I_{OUT} = 0 mA			8	mA
Rise Time	V_{CC} = 28V, R_L = 82Ω		0.10		μs
Fall Time	V_{CC} = 28V, R_L = 82Ω		0.8		μs
T_{on}	V_{CC} = 28V, R_L = 82Ω		0.26		μs
T_{off}	V_{CC} = 28V, R_L = 82Ω		2.2		μs

Note 1: Unless otherwise specified, limits shown apply from −55°C to 125°C for NH0006 and 0°C to 70°C for NH0006C/NH0006CN.

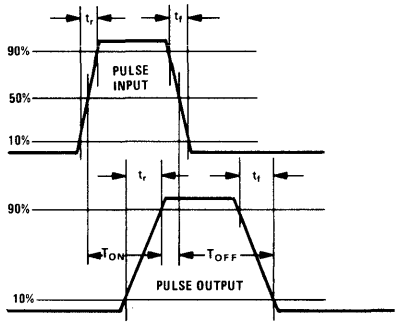
Note 2: Typical values are for 25°C ambient.

Note 3: Power ratings for the TO-5 based on a maximum junction temperature of +175°C and a ϕ_{JA} of 210°C/W.

Note 4: Power rating for the NH0006CN Molded DIP based on a maximum junction temperature of +150°C and a thermal resistance of 175°C/W when mounted in a standard DIP socket.

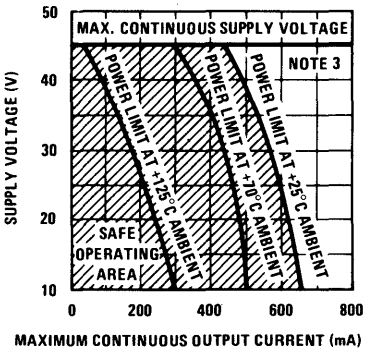
Note 5: Power rating for the NH0006CN Molded DIP based on a maximum junction temperature of +150°C and a thermal resistance of 150°C/W when mounted on a 1/16 inch thick, epoxy-glass board with ten 0.03 inch wide 2 ounce copper conductors.

switching time waveforms

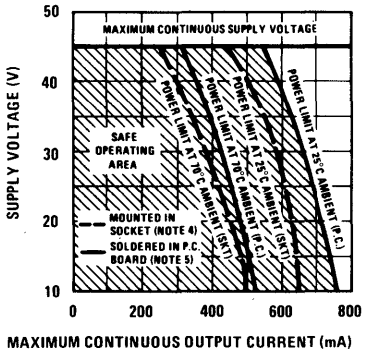


typical performance

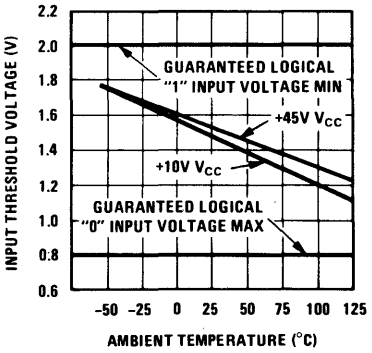
Maximum Continuous Output Current For TO-5



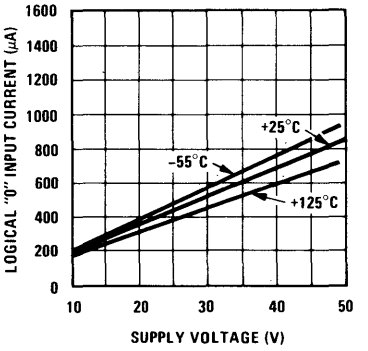
Maximum Continuous Output Current For Molded DIP



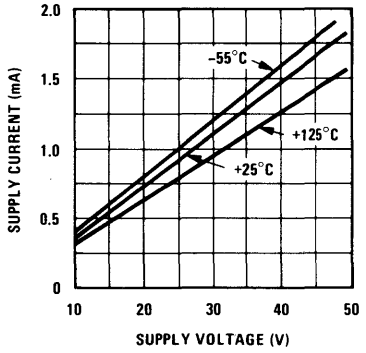
Input Threshold Voltage vs Temperature



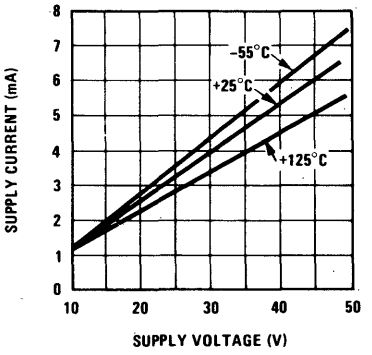
Logical "0" Input Current



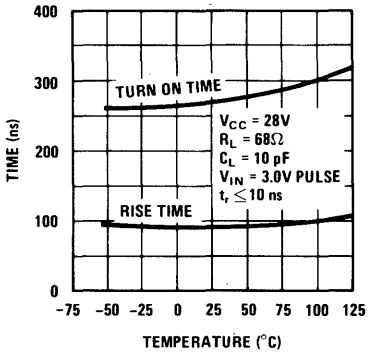
"OFF" Supply Current Drain



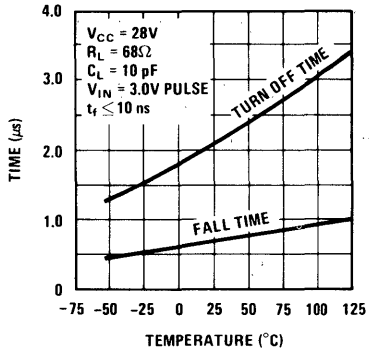
"ON" Supply Current Drain



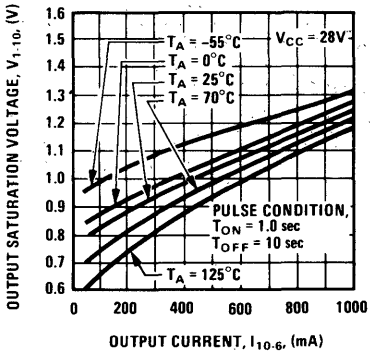
Turn On And Rise Time



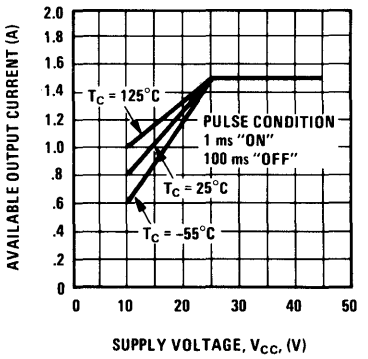
Turn Off and Fall Time



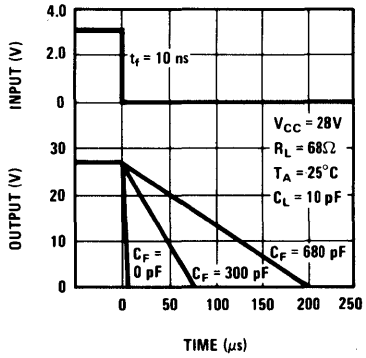
Output Saturation Voltage



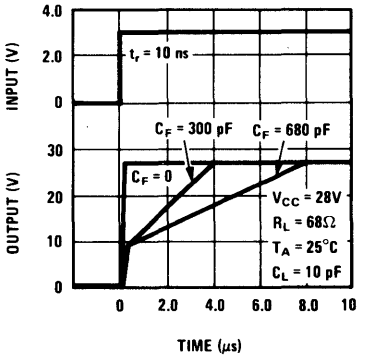
Available Output Current



Turn Off Control



Turn On Control



Current Drivers

NH0008/NH0008C
high voltage, high current driver

general description

The NH0008/NH0008C is an integrated high voltage, high current driver, designed to accept standard DTL or TTL input levels and provide a pulsed load of up to 3A from a continuous supply voltage up to 45V. AND inputs are provided with an EXPANDER connection, should additional gating be required.

Since one side of the load is normally grounded, there is less likelihood of false turn-on due to an inadvertent short in the drive line.

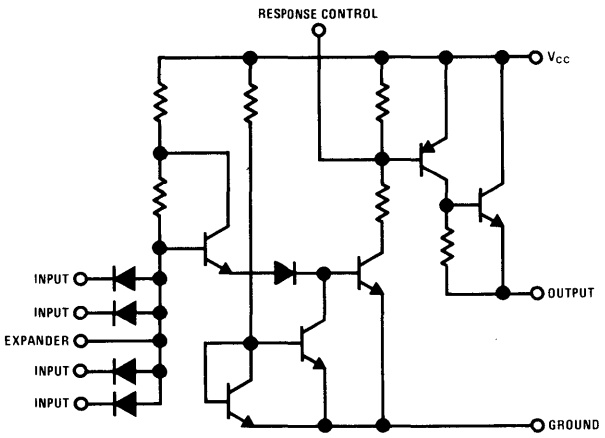
The high pulse current capability makes the NH0008/NH0008C ideal for driving nonlinear resistive loads such as incandescent lamps. The circuit also requires only one power supply for circuit functional operation.

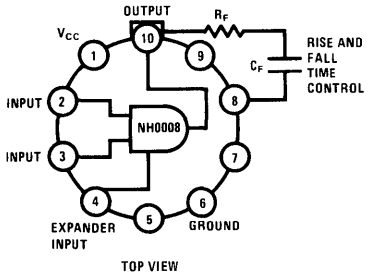
The NH0008 is available in a 10-pin TO-5 package; the NH0008C is also available in a 10-pin TO-5, in addition to a 10-lead molded dual-in-line package.

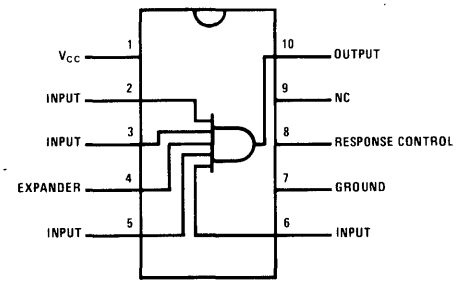
Some important design features include:

- Operation from a Single +10V to +45V Power Supply.
- Low Standby Power Dissipation of only 35 mW for 28V Power Supply.
- 3.0A, 50 ms, Pulse Current Capability.

schematic and connection diagrams

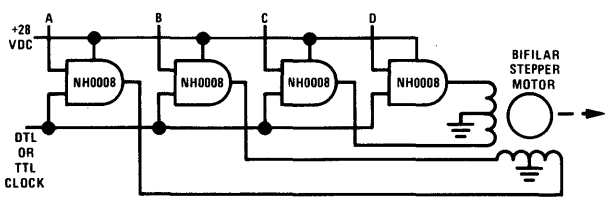






typical application

Controller for Closed Loop Stepper Motor



Switching Sequence

Step	A	B	C	D
1	1	0	1	0
2	1	0	0	1
3	0	1	0	1
4	0	1	1	0
1	1	0	1	0

To reverse the direction use a 4, 3, 2, 1 sequence

absolute maximum ratings

Peak Power Supply Voltage (for 0.1 sec)	60V
Continuous Supply Voltage	45V
Input Voltage	5.5V
Input Extender Current	5.0 mA
Peak Output Current	
(50 msec On/1 sec Off)	3.0 Amp
Continuous Output Current	
(See continuous operating curves.)	
Operating Temperature	
NH0008	−55°C to +125°C
NH0008C, NH0008CN	0°C to +70°C
Storage Temperature	−65°C to +150°C

electrical characteristics (Note 1)

PARAMETER	CONDITIONS	MIN	TYP (Note 2)	MAX	UNITS
Logical "1" Input Voltage	V_{CC} = 45V to 10V	2.0			V
Logical "0" Input Voltage	V_{CC} = 45V to 10V			0.8	V
Logical "1" Output Voltage	V_{CC} = 45V, V_{IN} = 2.0V, I_{OUT} = 1.6A 50 ms On/1 sec Off	43	43.5		V
Logical "0" Output Voltage	V_{CC} = 45V, V_{IN} = 0.8V, R_L = 1K		0.02	0.1	V
Logical "1" Output Voltage	V_{CC} = 28V, V_{IN} = 2.0V, I_{OUT} = 0.8A 50 ms On/1 sec Off	26.5	27.1		V
Logical "0" Input Current	V_{CC} = 45V, V_{IN} = 0.4V		0.8	1.0	mA
Logical "1" Input Current	V_{CC} = 45V, V_{IN} = 2.4V		0.5	5.0	μA
	V_{CC} = 45V, V_{IN} = 5.5V			100	μA
"Off" Power Supply Current	V_{CC} = 45V, V_{IN} = 0V		1.6	2.0	mA
Rise Time	V_{CC} = 28V, R_L = 39Ω, V_{IN} = 5.0V		0.2		μs
Fall Time	V_{CC} = 28V, R_L = 39Ω, V_{IN} = 5.0V		3.0		μs
T_{ON}	V_{CC} = 28V, R_L = 39Ω, V_{IN} = 5.0V		0.4		μs
T_{OFF}	V_{CC} = 28V, R_L = 39Ω, V_{IN} = 5.0V		7.0		μs

Note 1: Unless otherwise specified limits shown apply from −55°C to 125°C for NH0008 and 0°C to 70°C for NH0008C/NH0008CN.

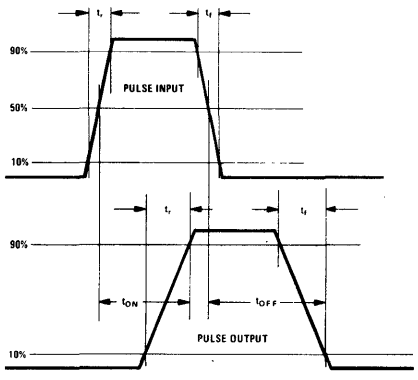
Note 2: Typical values are 25°C ambient.

Note 3: Power ratings for the TO-5 based on a maximum junction temperature of +175°C and a ϕ JA of 210°C/w.

Note 4: Power ratings for the NH0008CN Molded DIP based on a maximum junction temperature of 150°C and a thermal resistance of 150°C/w when mounted in a standard DIP socket.

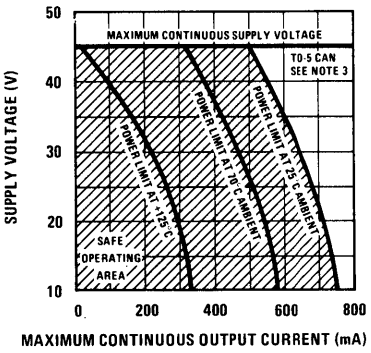
Note 5: Power ratings for the NH0008CN Molded DIP based on a maximum junction temperature of 150°C and a thermal resistance of 115°C/w when mounted on a 1/16 inch thick, epoxy-glass board with ten 0.03 inch wide 2 ounce copper conductors.

switching time waveforms

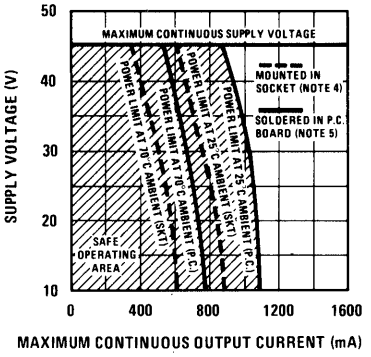


typical performance

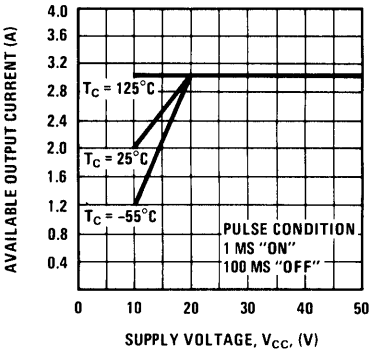
Maximum Continuous Output Current for TO-5 Package



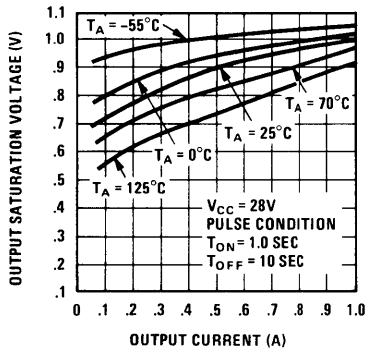
Maximum Continuous Output Current for Molded DIP



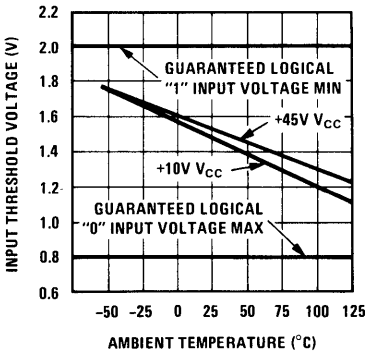
Available Output Current



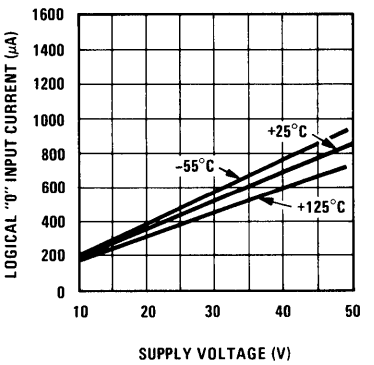
Output Saturation Voltage



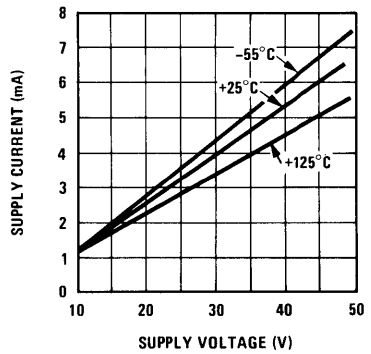
Input Threshold Voltage vs Temperature



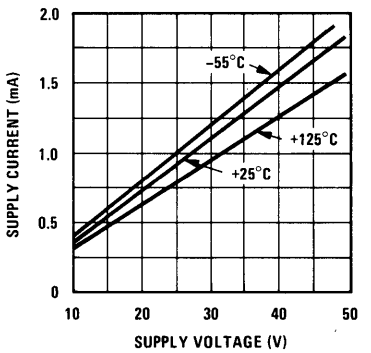
Logical "0" Input Current



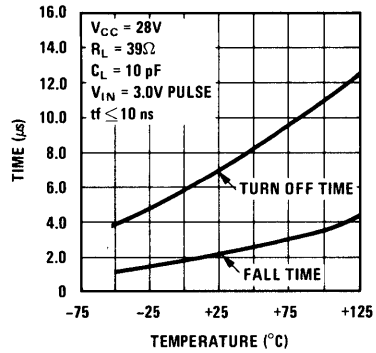
ON Supply Current Drain



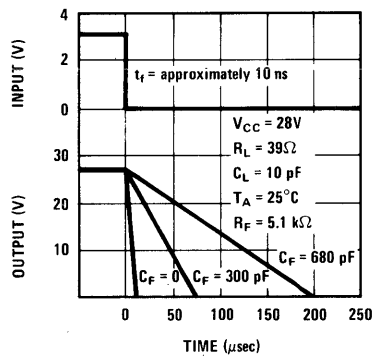
OFF Supply Current Drain



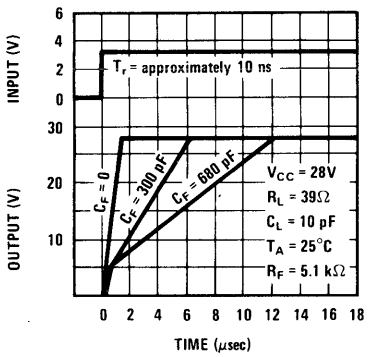
Turn OFF and Fall Times



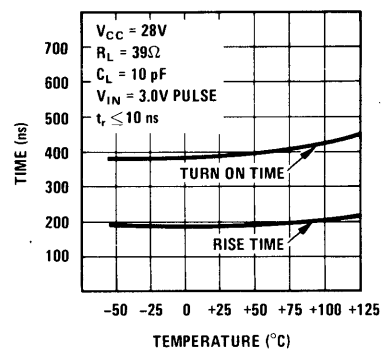
Turn ON Control



Turn OFF Control



Turn ON and Rise Time



Current Drivers

NH0011 (SH2001)
NH0011C (SH2002)
NH0011CN (SH2002P)

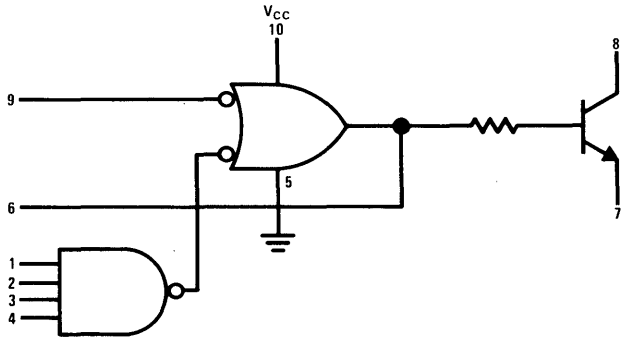
high voltage high current drivers

general description

The NH0011 high voltage, high current driver family consists of hybrid integrated circuits which provide a wide range of variations in temperature range, package, and output current drive capability. A summary of the variations is listed below.

Applications include driving lamps, relays, cores, and other devices requiring several hundred milliamp currents at voltages up to 40V. Logic flexibility is provided through a 4-input NAND gate, a NOR input and an input which bypasses the gating and connects the base of the output transistor.

logic diagram



NSC DESIGNATION	SH DESIGNATION	PACKAGE	TEMPERATURE RANGE	OUTPUT CURRENT CAPABILITY
NH0011	SH2001	TO-100	-55°C to +125°C	250 mA
NH0011C	SH2002	TO-100	0°C to +70°C	150 mA
NH0011CN	SH2002 P	Silicone DIP	0°C to +70°C	150 mA

absolute maximum ratings

V_{CC}	8V
Collector Voltage (Output)	40V
Input Reverse Current	1.0 mA
Power Dissipation	800 mW
Operating Temperature Range NH0011	−55°C to +125°C
NH0011C, NH0011CN	0°C to +70°C
Storage Temperature	−65°C to 150°C

electrical characteristics NH0011, NH0011C, NH0011CN

TEST NO.	PIN 1	PIN 2	PIN 3	PIN 4	PIN 5	PIN 6	PIN 7	PIN 8	PIN 9	PIN 10	SENSE	MIN	MAX
1	V_{IH}	V_{IH}	V_{IH}	V_{IH}	GND		GND	I_{OL1}		V_{CCL}	V_8		V_{OL}
2	V_{IL}				GND		GND	I_{OL1}	V_{IL}	V_{CCL}	V_8		V_{OL}
3	V_{IL}				GND	I_{OL2}				V_{CCL}	V_6		V_{OL2}
4		V_{IL}			GND	I_{OL2}				V_{CCL}	V_6		V_{OL2}
5			V_{IL}		GND	I_{OL2}				V_{CCL}	V_6		V_{OL2}
6				V_{IL}	GND	I_{OL2}				V_{CCL}	V_6		V_{OL2}
7				GND	GND	I_{OL2}			V_{IH}	V_{CCL}	V_6		V_{OL2}
8	V_R	GND	GND	GND	GND					V_{CCH}	I_1		I_R
9	GND	V_R	GND	GND	GND					V_{CCH}	I_2		I_R
10	GND	GND	V_R	GND	GND					V_{CCH}	I_3		I_R
11	GND	GND	GND	V_R	GND					V_{CCH}	I_4		I_R
12					GND				V_R	V_{CCH}	I_9		I_R
13	V_F	V_R	V_R	V_R	GND					V_{CCH}	I_1		$-I_F$
14	V_R	V_F	V_R	V_R	GND					V_{CCH}	I_2		$-I_F$
15	V_R	V_R	V_F	V_R	GND					V_{CCH}	I_3		$-I_F$
16	V_R	V_R	V_R	V_F	GND					V_{CCH}	I_4		$-I_F$
17				GND	GND				V_F	V_{CCH}	I_9		$-I_F$
18					GND		GND			V_{CCL}	V_6	V_{OH}	
19	GND				GND		GND	V_{OX}		V_{CCL}	I_8		I_{OX}
20					GND		GND			V_{PD}	I_{10}		I_{PDH}
21	GND				GND					V_{MAX}	I_{10}		I_{MAX}
22*					GND					V_{PD}			t_{ON}
23*					GND					V_{PD}			t_{OFF}

*See Test Circuits and Waveforms on Page 4.

forcing functions (Note 1) NH0011

PARAMETER	−55°C	+25°C	+125°C	UNITS
V_{CCL}	4.5	4.5	4.5	V
V_{CCH}	5.5	5.5	5.5	V
V_{PD}		5.0		V
V_{MAX}		8.0		V
V_{IL}	1.4	1.1	0.8	V
V_{IH}	2.1	1.9	1.7	V
V_R	4.0	4.0	4.0	V
V_F	0.0	0.0	0.0	V
I_{OL1}	250	250	250	mA
I_{OL2}	8.0	8.0	7.5	mA
V_{OX}	40.0	40.0	40.0	V

Note 1: Temperature Range −55°C to +125°C

forcing functions (Note 2) NH0011C, NH0011CN

PARAMETER	0°C	+25°C	+70°C	UNITS
V_{CCL}	5.00	5.0	5.0	V
V_{CCH}	5.00	5.0	5.0	V
V_{PD}		5.0		V
V_{MAX}		8.0		V
V_{IL}	1.20	1.1	.95	V
V_{IH}	2.00	1.9	1.8	V
V_R	4.00	4.0	4.0	V
V_F	0.45	0.45	0.5	V
I_{OL1}	150	150	150	mA
I_{OL2}	8.0	8.0	7.5	mA
V_{OX}	40.00	40.0	40.0	V

test limits (Note 1) NH0011

PARAMETER	-55°C		+25°C		+125°C		UNITS
	MIN	MAX	MIN	MAX	MIN	MAX	
V_{OL1}		0.45		0.4		0.45	V
V_{OL2}		0.45		0.4		0.45	V
V_{OH}	2.20		2.00		1.80		V
I_R				2.0		5.0	μA
$-I_F$		1.60		1.6		1.5	mA
I_{OX}				5.0		200	μA
I_{PDH}				30.6			mA
I_{MAX}				29.6			mA
t_{ON}				160			ns
t_{OFF}				220			ns

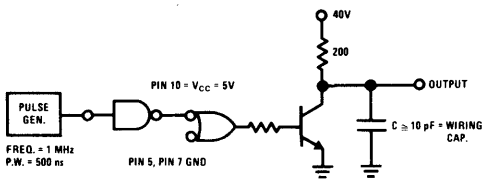
test limits (Note 2) NH0011C, NH0011CN

PARAMETER	0°C		+25°C		+70°C		UNITS
	MIN	MAX	MIN	MAX	MIN	MAX	
V_{OL1}		0.45		0.45		0.5	V
V_{OL2}		0.45		0.45		0.5	V
V_{OH}	2.05		1.95		1.85		V
I_R				5.0		10.0	μA
$-I_F$		1.40		1.4		1.35	mA
I_{OX}				5.0		200	μA
I_{PDH}				30.6			mA
I_{MAX}				34.0			mA

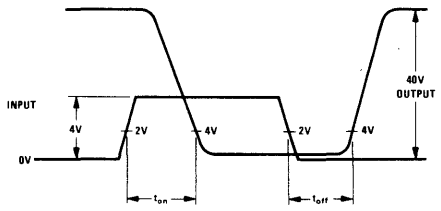
Note 1: Temperature Range −55°C to +125°C

Note 2: Temperature Range 0°C to +70°C

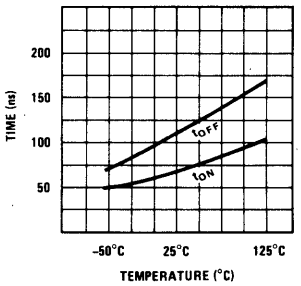
switching time test circuit



switching time waveform



Typical Switching Times



Current Drivers

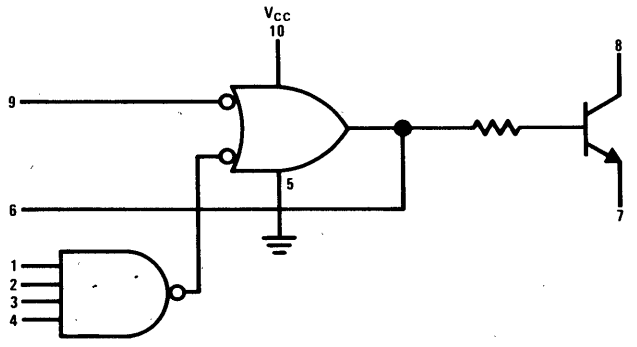
NH0016CN
NH0017CN(SH2200P)
NH0018CN

high voltage high current drivers

general description

This high-voltage, high-current driver family consists of hybrid integrated circuits which provide a wide range of output currents and output voltages. Applications include driving lamps, relays, cores, and other devices requiring up to 500 mA and withstanding voltages up to 100V. Logic flexibility is provided through a 4-input NAND gate, a NOR input and an input which bypasses the gating and connects to the base of the output transistor.

logic diagram



NSC DESIGNATION	SH DESIGNATION	PACKAGE	OUTPUT CHARACTERISTICS	
			Maximum Standoff Voltage	Current
NH0016CN	N/A	Silicone DIP	70V	250 mA
NH0017CN	SH2200P	Silicone DIP	50V	500 mA
NH0018CN	N/A	Silicone DIP	100V	500 mA

absolute maximum ratings

V_{CC}		8V
Input Voltage		8V
Collector Voltage	NH0016CN	70V
	NH0017CN	50V
	NH0018CN	100V
Output Surge Current	NH0016CN	1.0A
	NH0017CN & NH0018CN	2.0A
Power Dissipation		455mW
Operating Temperature Range		0°C to +70°C
Storage Temperature		−65°C to +150°C

electrical characteristics

TEST NO.	PIN 1	PIN 2	PIN 3	PIN 4	PIN 5	PIN 6	PIN 7	PIN 8	PIN 9	PIN 10	SENSE	LIMITS MIN	LIMITS MAX
2	V_{IH}	V_{IH}	V_{IH}	V_{IH}	GND		GND	I_{OL1}		V_{CC}	V_8		V_{OL1}
3	V_{IL}				GND		GND	I_{OL1}	V_{IL}	V_{CC}	V_8		V_{OL1}
4		V_{IL}			GND		GND	I_{OL1}	V_{IL}	V_{CC}	V_8		V_{OL1}
5			V_{IL}		GND		GND	I_{OL1}	V_{IL}	V_{CC}	V_8		V_{OL1}
6				V_{IL}	GND		GND	I_{OL1}	V_{IL}	V_{CC}	V_8		V_{OL1}
7	V_{IL}				GND	I_{OL2}				V_{CC}	V_6		V_{OL2}
8		V_{IL}			GND	I_{OL2}				V_{CC}	V_6		V_{OL2}
9			V_{IL}		GND	I_{OL2}				V_{CC}	V_6		V_{OL2}
10				V_{IL}	GND	I_{OL2}				V_{CC}	V_6		V_{OL2}
11				GND	GND	I_{OL2}			V_{IH}	V_{CC}	V_6		V_{OL2}
12	V_R	GND	GND	GND	GND					V_{CC}	I_1		I_R
13	GND	V_R	GND	GND	GND					V_{CC}	I_2		I_R
14	GND	GND	V_R	GND	GND					V_{CC}	I_3		I_R
15	GND	GND	GND	V_R	GND					V_{CC}	I_4		I_R
16					GND				V_R	V_{CC}	I_9		I_R
17	V_F	V_R	V_R	V_R	GND					V_{CC}	I_1		$-I_F$
18	V_R	V_F	V_R	V_R	GND					V_{CC}	I_2		$-I_F$
19	V_R	V_R	V_F	V_R	GND					V_{CC}	I_3		$-I_F$
20	V_R	V_R	V_R	V_F	GND					V_{CC}	I_4		$-I_F$
21				GND	GND				V_F	V_{CC}	I_9		$-I_F$
22					GND		GND			V_{CC}	V_6	V_{OH1}	
23	GND				GND	I_{OL3}	GND	V_{OX}		V_{CC}	I_8		I_{OX}
24					GND					V_{PD}	I_{10}		I_{PD}
25	GND				GND				GND	V_{MAX}	I_{10}		I_{MAX}

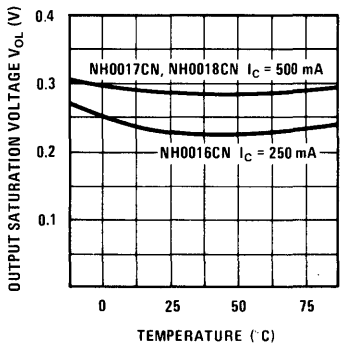
forcing functions

SYMBOL	0°C	+25°C	+70°C	UNITS
V_{CC}	5.0	5.0	5.0	V
V_{PD}		5.0		V
V_{MAX}		8.0		V
V_{IL}	0.85	0.85	0.85	V
V_{IH}	1.9	1.8	1.6	V
V_R	4.5	4.5	4.5	V
V_F	0.45	0.45	0.45	V
V_{OX} (NH0016CN)		70	70	V
V_{OX} (NH0017CN)		50	50	V
V_{OX} (NH0018CN)		100	100	V
I_{OL1} (NH0017CN, NH0018CN)	500	500	500	mA
I_{OL1} (NH0016CN)	250	250	250	mA
I_{OL2}	16	16	16	mA
I_{OL3}		8.0		mA

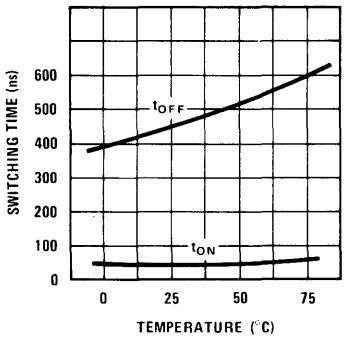
test limits

SYMBOL	0°C	+25°C	+70°C	UNITS
V_{OL1}	0.6	0.6	0.6	V
V_{OL2}	0.45	0.45	0.45	V
V_{OH1}	1.95	1.85	1.65	V
I_R		60	60	μA
$-I_F$	1.6	1.6	1.6	mA
I_{OX}		5.0	200	μA
I_{PD}		12.2		mA
I_{MAX}		10		mA

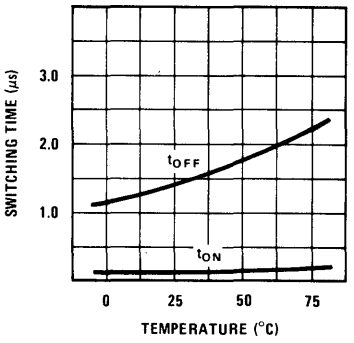
Typical Output Voltages vs Temperature



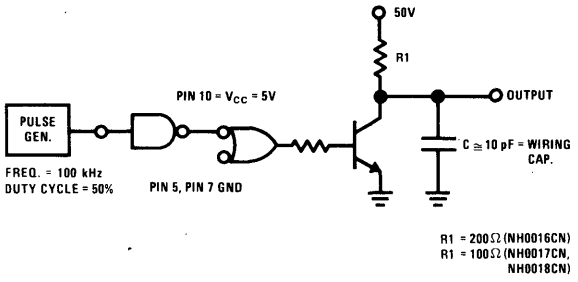
Typical Switching Times I_C = 250 mA
NH0016CN



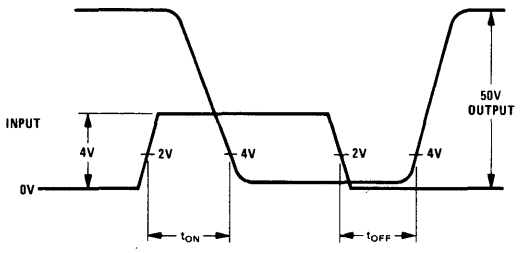
Typical Switching Times I_C = 500 mA
NH0017N, NH0018CN



switching time test circuit



switching time waveform



Current Drivers

NH0028C/NH0028CN hammer driver

general description

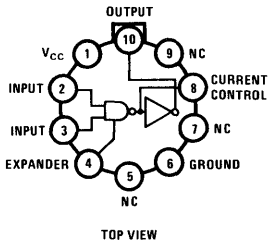
The NH0028C/NH0028CN is a high current hammer driver designed for utilization in a wide variety of printer applications. The device is capable of driving 6 amp pulsed loads at duty cycles up to 10% (1 ms ON/10 ms OFF). The input is DTL/TTL compatible and requires only a single voltage supply in the range of 10V to 45V.

Additional features include:

- Low standby power: 45 mW at V_{CC} = 36V, 35 mW at V_{CC} = 28V.
- AND input with expander affords logic flexibility.
- Fast turn-on, typically 200 ns.

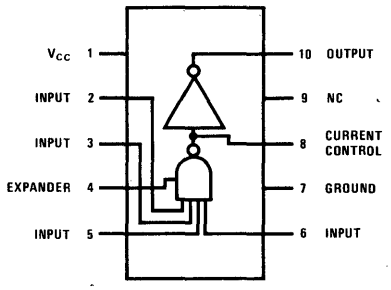
connection diagrams

Metal Can

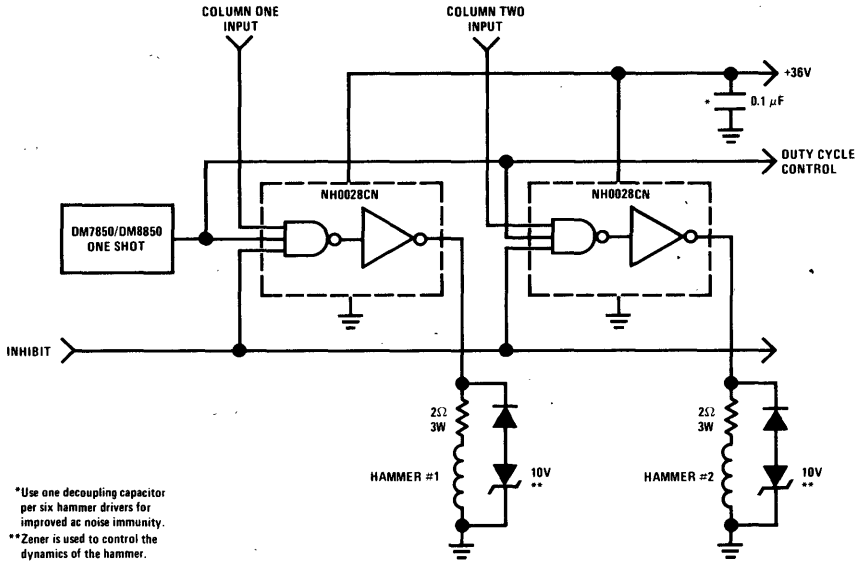


TOP VIEW

Molded Dual-In-Line



typical application



*Use one decoupling capacitor per six hammer drivers for improved ac noise immunity.
**Zener is used to control the dynamics of the hammer.

absolute maximum ratings

Continuous Supply Voltage	45V
Instantaneous Peak Supply Voltage (Pin 1 to Ground for 0.1 sec)	60V
Input Voltage	5.5V
Expander Input Current	5.0 mA
Peak Output Current (1 ms ON/10 ms OFF)	6.5A
Continuous Output Current NH0028C at 25°C	750 mA
NH0028CN at 25°C	1000 mA
Operating Temperature	0°C to 70°C
Storage Temperature	−65° to +175°C
Lead Soldering Temperature (10 sec)	300°C

electrical characteristics (Note 1)

PARAMETER	CONDITIONS	MIN	TYP (Note 1)	MAX	UNITS
Logical "1" Input Voltage	V_{CC} = 10V to 45V	2.0			V
Logical "0" Input Voltage	V_{CC} = 10V to 45V			0.8	V
Logical "0" Input Current	V_{CC} = 45V, V_{IN} = 0.4V		0.8	1.0	mA
Logical "1" Input Current	V_{CC} = 45V, V_{IN} = 2.4V		0.5	5.0	μA
	V_{CC} = 45V, V_{IN} = 5.5V			100.0	μA
Logical "1" Output Voltage	V_{CC} = 45V, V_{IN} = 2.0V, I_{OUT} = 1.6A	43.0	43.5		V
	V_{CC} = 36V, V_{IN} = 2.0V, I_{OUT} = 5A (Note 2)	33.5	34.0		V
Logical "0" Output Voltage	V_{CC} = 45V, R_L = 1k, V_{IN} = 0.8V		.020	100	V
OFF Power Supply Current	V_{CC} = 45V, V_{IN} = 0.0V		1.6	2.0	mA
Rise Time (10% to 90%)	V_{CC} = 45V, R_L = 39Ω, V_{IN} = 5.0V peak, PRF = 1 kHz		0.2		μs
Fall Time (90% to 10%)	V_{CC} = 45V, R_L = 39Ω, V_{IN} = 5.0V peak, PRF = 1 kHz		3.0		μs
T_{ON}	V_{CC} = 45V, R_L = 39Ω, V_{IN} = 5.0V peak, PRF = 1 kHz		0.4		μs
T_{OFF}	V_{CC} = 45V, R_L = 39Ω, V_{IN} = 5.0V peak, PRF = 1 kHz		7.0		μs

Note 1: These specifications apply for ambient temperatures from 0°C to 70°C unless otherwise specified. All typical values are for 25°C ambient.

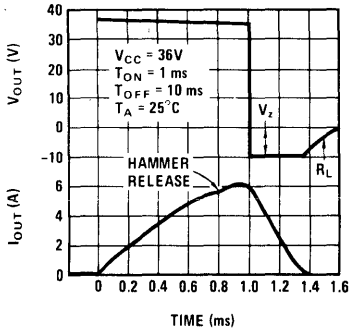
Note 2: Measurement made at 1 ms ON and 10 ms OFF.

Note 3: Power ratings for the NH0028C are based on a maximum junction temperature of 175°C and a thermal resistance of 210°C/W.

Note 4: Power ratings for the NH0028CN are based on a maximum junction temperature of 175°C and a thermal resistance of 150°C/W.

typical performance characteristics

Waveforms for Typical Drum Printer Hammer



Series 54L/74L

LOW POWER TRANSISTOR-TRANSISTOR LOGIC

general description

The Series 54L/74L family is designed for applications requiring very low power dissipation. Typically a system can be built with a factor-of-ten power saving over the conventional TTL integrated circuits, such as Series 54/74. Gates typically draw 0.2 mA from a 5 volt supply thus dissipating 1 mW. Flip flops pull about 1.0 mA and therefore dissipate about 5 mW. Speed however is not proportionately sacrificed. Flip flops can typically be clocked at 11 MHz. Gate delays are typically 25 ns.

The Series is manufactured with TTL circuitry and employs low impedance Darlington outputs which maintain output voltage waveform integrity when capacitively loaded. The Darlington outputs also allow greater guaranteed logical "1" fan out (20) in case it is desirable to connect unused inputs to used inputs.

National's Low Power Series is also guaranteed to drive two standard TTL unit loads from 0°C to 70°C.

features

- Low power dissipation—typically 1 mW/gate, 5 mW/flip flop.
- Relatively high speed
  - Typical gate propagation delay time of 25 ns.
  - Typical flip flop toggle frequency at 11 MHz.
  - Typical MSI shift register toggle frequency at 12 to 14 MHz.
- High dc noise margin—typically 1 volt at $T_A = 25°C$.
- Low impedance Darlington outputs provide low ac noise susceptibility.
- Fan Out
  - 10 Series 54L loads in logical "0" state
  - 20 Series 54L loads in logical "1" state
  - 2 Series 74 loads (74L only)
  - 1 Series 54 load and 2 Series 54L loads
  - 1 Series 54H load.
- TTL and DTL compatible.

Device types specified in the data sheet include:

NAND, NOR GATES

DM54L00/DM74L00 (SN54L00/SN74L00)
Quad 2-Input NAND Gate
DM54L01/DM74L01 (SN54L01/SN74L01)
Quad 2-Input NAND Gate, Open Collector
DM54L02/DM74L02 Quad 2-Input NOR Gate
DM54L03/DM74L03 Quad 2-Input NAND Gate, Open Collector
DM54L04/DM74L04 (SN54L04/SN74L04)
Hex Inverter
DM54L10/DM74L10 (SN54L10/SN74L10)
Triple 3-Input NAND Gate
DM54L20/DM74L20 (SN54L20/SN74L20)
Dual 4-Input NAND Gate
DM54L30/DM74L30 (SN54L30/SN74L30)
Eight-Input NAND Gate

AND-OR-INVERT GATES

DM54L51/DM74L51 (SN54L51/SN74L51)
Dual 2-wide AND-OR-INVERT Gate
DM54L54/DM74L54 (SN54L54/SN74L54)
Four-wide 3-2-2-3-Input AND-OR-INVERT Gate

DM54L55/DM74L55 (SN54L55/SN74L55)
Two-wide 4-Input AND-OR-INVERT Gate

table of contents

general description (cont.)

FLIP FLOPS

DM54L71/DM74L71 (SN54L71/SN74L71)
R-S Flip Flop

These R-S flip-flops use master-slave construction so the slave is stable when the clock is held either high or low. Clock disable at data inputs results in hold times of 0 ns, and also clock-controlled data entry.

DM54L72/DM74L72 (SN54L72/SN74L72)
J-K Flip Flop

These J-K flip-flops use master-slave construction so the slave is stable when the clock is held either high or low. Clock disable at data inputs results in hold times of 0 ns, and also clock-controlled data entry.

DM54L73/DM74L73 (SN54L73/SN74L73)
Dual J-K Flip Flop

Operation is the same as the DM54L72/DM74L72 except that only single J and K inputs are available.

DM54L74/DM74L74 (SN54L74/SN74L74)
Dual D Flip Flop

These monolithic, low-power, dual, edge-triggered flip flops utilize TTL circuitry to perform D-type flip flop logic. Each flip flop has individual clear and preset inputs, and complementary Q and $\overline{Q}$ outputs.

Information at D-input is transferred to the Q output on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D-input signal has no effect on the state of the output.

DM54L78/DM74L78 (SN54L78/SN74L78)
Dual J-K Flip Flop

Operation is the same as the DM54L73/DM74L73 except that common CLEAR and CLOCK inputs feed both flip flops. This frees two pins which are used for separate PRESET inputs.

EXCLUSIVE-OR GATES

DM54L86/DM74L86 (SN54L86/SN74L86)
Quad EXCLUSIVE-OR Gate

The DM54L86/DM74L86 (SN54L86/SN74L86) quad EXCLUSIVE-OR circuit performs as a half-adder: the output is a logical "1" only when the inputs are at different logical states.

SHIFT REGISTERS

DM54L95/DM74L95 (SN54L95/SN74L95)
Four-bit Parallel-in Parallel-out Shift Register

Parallel or serial operation is selected by the MODE input, which also enables one of the two clock inputs. Parallel information must be clocked-in allowing shift-left operation by connecting each output to the left-adjacent parallel input.

DM76L70/DM86L70 Eight-Bit Serial-In Parallel-Out Shift Register

The DM76L70/DM86L70 utilizes Series 54L/74L compatible TTL circuitry to provide an eight-bit serial-in parallel-out shift register. Other features include gated serial inputs for strobe capability and a clear input which, when taken to a logical "0", asynchronously sets all flip flops to the logical "0" state.

Because the flip flops are R-S instead of J-K, input information may be changed immediately prior to the triggering edge of the clock waveform. Logical "1" levels on SA and SB enter logical "1's" into the shift register. Clocking occurs on the positive-going edge of the clock pulse.

absolute maximum ratings

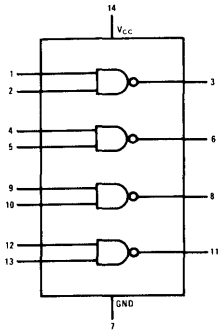
Power Supply Voltage	8.0V
Input Voltage	5.5V
Fan Out Logic "1"	20
Logic "0"	10
Storage Temperature Range	−65°C to 150°C
Lead Temperature (Soldering, 10 sec)	300°C

guaranteed operating conditions

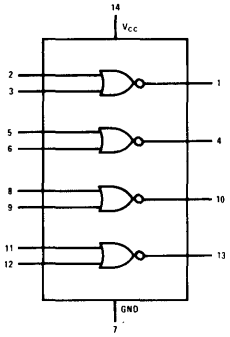
Power Supply Voltage	
DM54LXX, DM7XLXX	4.5V to 5.5V
DM74LXX, DM8XLXX	4.75V to 5.25V
Operating Temperature	
DM54LXX, DM7XLXX	−55°C to 125°C
DM74LXX, DM8XLXX	0°C to 70°C

SUMMARY

dual-in-line package connection diagrams



DM54L00/DM74L00



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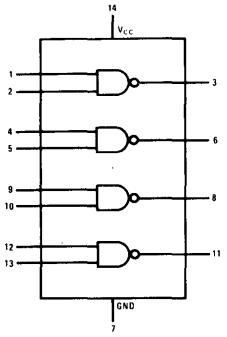

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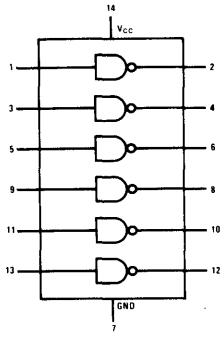

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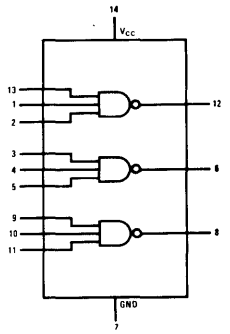

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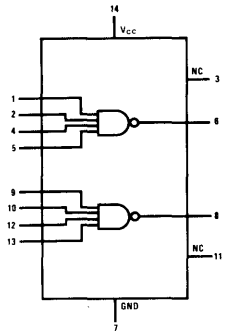

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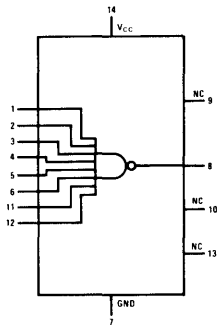

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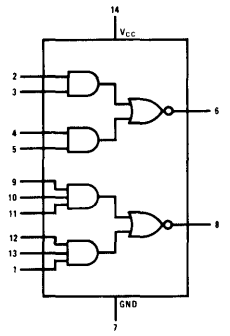
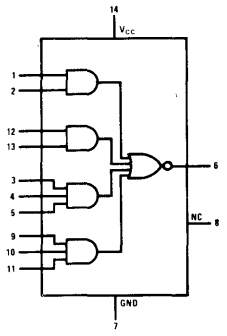


DM54L51/DM74L51



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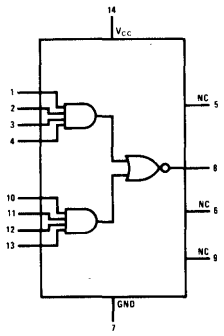

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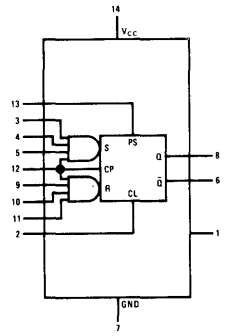
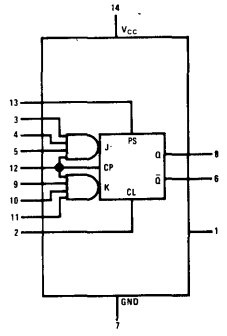
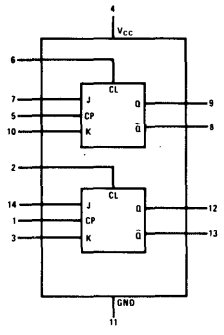


DM54L71/DM74L71

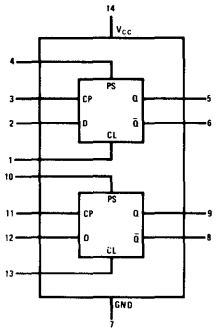


DM54L72/DM74L72

dual-in-line package connection diagrams (cont.)



DM54L73/DM74L73



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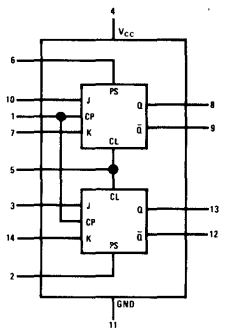

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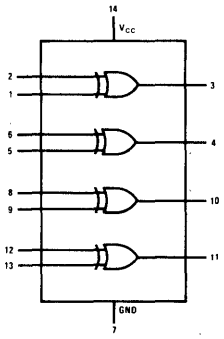

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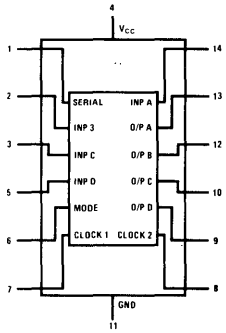

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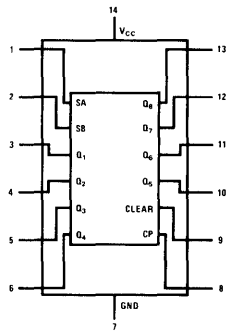
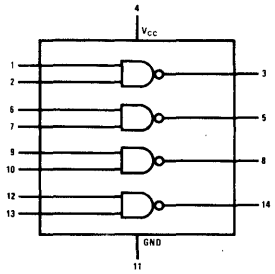


DM76L70/DM86L70

flat package connection diagrams



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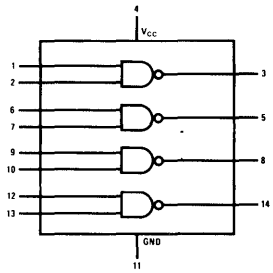

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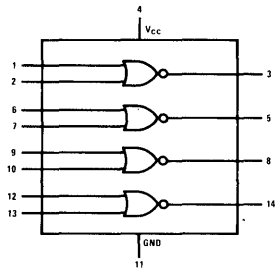

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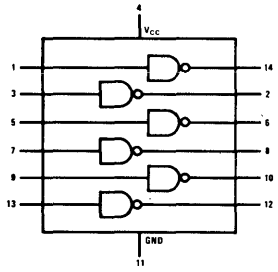

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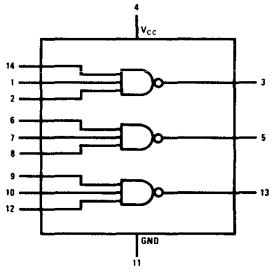

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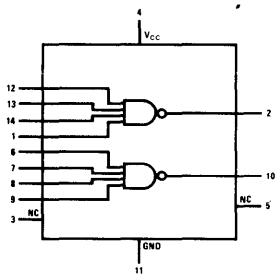
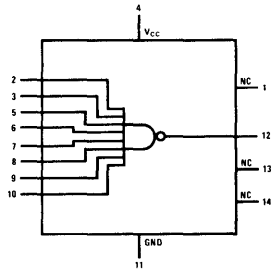


DM54L20/DM74L20

flat package connection diagrams (cont.)



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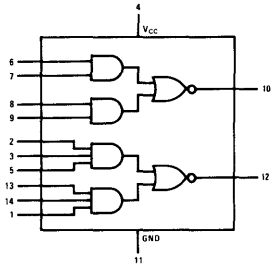

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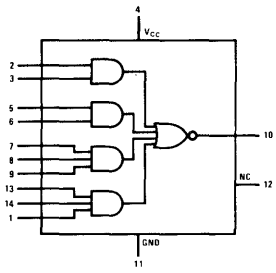

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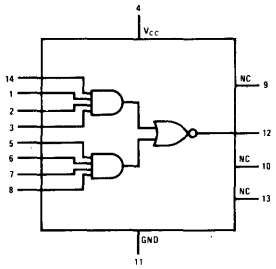

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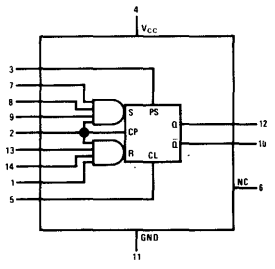
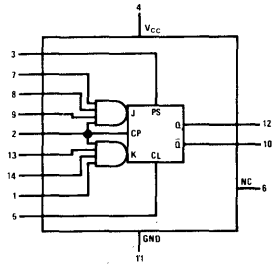
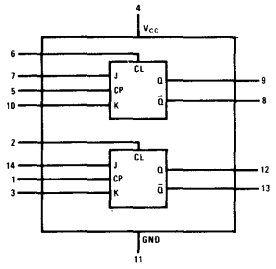


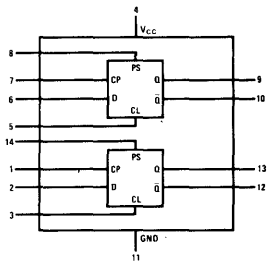
DM54L71/DM74L71



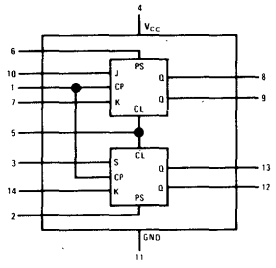
DM54L72/DM74L72



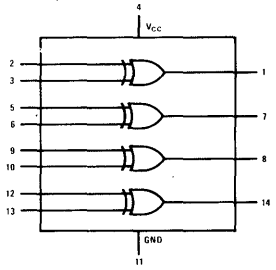
DM54L73/DM74L73



DM54L74/DM74L74



DM54L78/DM74L78



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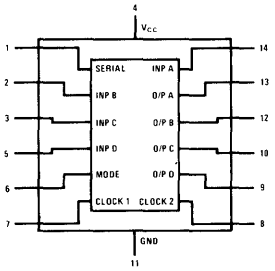

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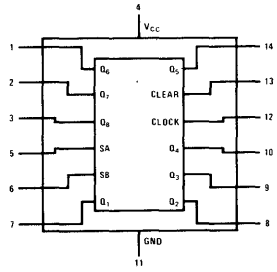
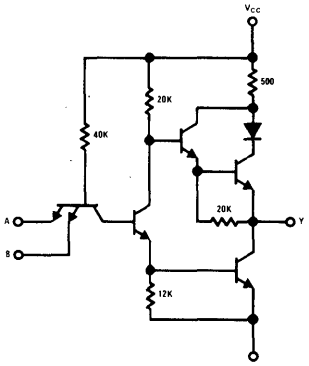


DM76L70/DM86L70

NAND, NOR GATES

DM54L00/DM74L00, DM54L01/DM74L01, DM54L02/DM74L02, DM54L03/DM74L03, DM54L04/DM74L04, DM54L10/DM74L10, DM54L20/DM74L20,DM54L30/DM74L30

schematic diagrams



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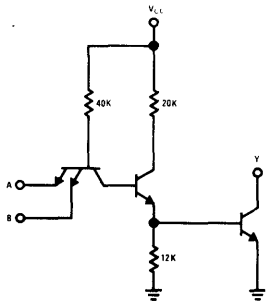
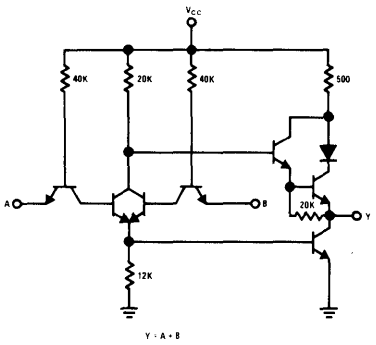
DM54L20/DM74L20, DM54L30/DM74L30



DM54L01/DM74L01
DM54L03/DM74L03



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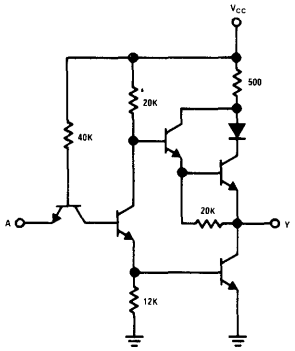
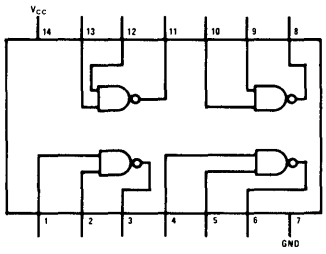
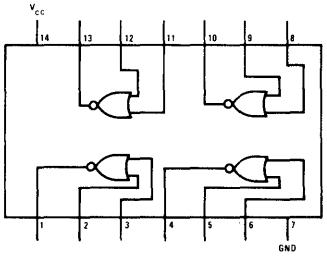


DM54L04/DM74L04

dual-in-line package connection diagrams



DM54L00/DM74L00
DM54L03/DM74L03



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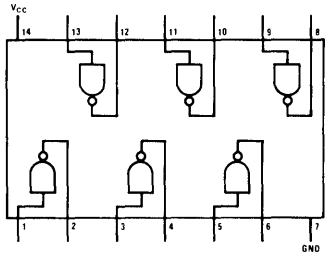

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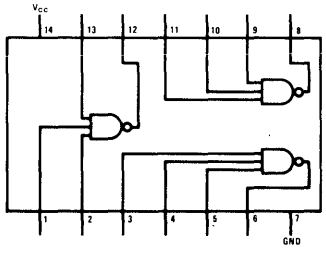

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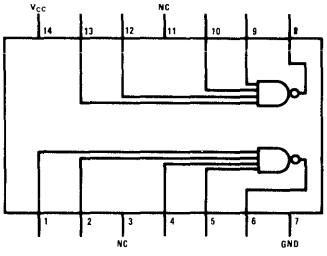

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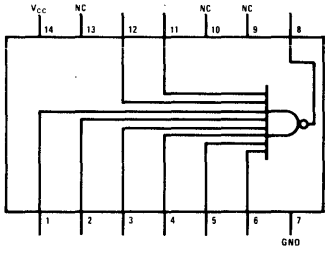
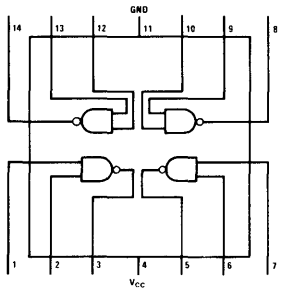
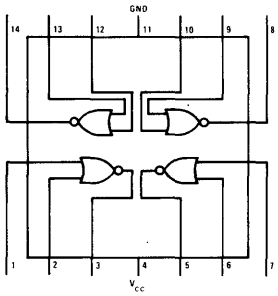


DM54L30/DM74L30

flat package connection diagrams



DM54L00/DM74L00
DM54L01/DM74L01



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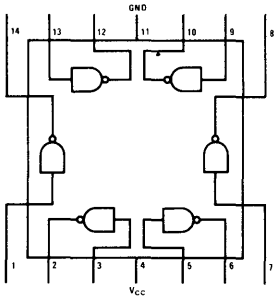

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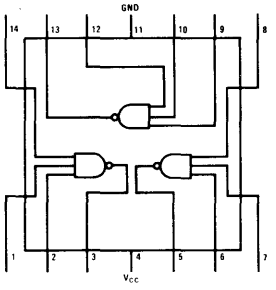

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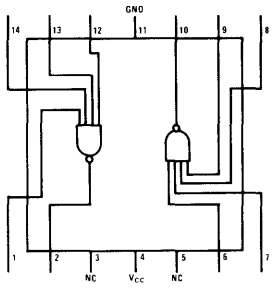

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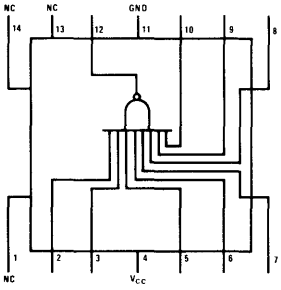


DM54L30/DM74L30

dc electrical characteristics

SYMBOL	PARAMETER	CONDITIONS	TEST FIGURE	MIN	TYP (NOTE 1)	MAX	UNITS
$V_{IN(1)}$	Logical "1" Input Voltage	V_{CC} = MIN	1	2	1.3		V
$V_{IN(0)}$	Logical "0" Input Voltage	V_{CC} = MIN	2		1.3	0.7	V
$V_{OUT(1)}$	Logical "1" Output Voltage (Except DM54L01/DM74L01, DM54L03/DM74L03)	V_{CC} = MIN, I_{OUT} = -200 μA, V_{IN} = 0.7V, Other Inputs = 2V	2	2.4	2.8		V
$I_{OUT(1)}$	Output Current DM54L01/DM74L03	V_{IN} = 0.3V, V_{CC} = MIN, V_{OUT} = 5.5V	6A			10	μA
	DM54L01/DM54L03	V_{IN} = 0.6V, V_{CC} = MIN, V_{OUT} = 5.5V	6A			200	μA
	DM74L01/DM74L03	V_{IN} = 0.7V, V_{CC} = MIN, V_{OUT} = 5.5V	6A			10	μA
$V_{OUT(0)}$	Logical "0" Output Voltage	V_{CC} = MIN, I_{OUT} = 2 mA, V_{IN} (All Inputs) = 2V	1		0.15	0.3	V
$V_{OUT(0)}$	Logical "0" Output Voltage (Series 74L Only)	V_{CC} = MIN, I_{OUT} = 3.2 mA, V_{IN} (All Inputs) = 2V	1			0.4	V
$I_{IN(1)}$	Logical "1" Input Current	V_{CC} = MAX, V_{IN} = 2.4V, Other Inputs = 0V	4		<1	10	μA
		V_{CC} = MAX, V_{IN} = 5.5V	4			100	μA
$I_{IN(0)}$	Logical "0" Input Current	V_{CC} = MAX, V_{IN} = 0.3V, Other Inputs = 4.5V	3		-120	-180	μA
I_{OS}	Logical "1" Output Short-Circuit Current (Except DM54L01/DM74L01, DM54L03/DM74L03)	V_{CC} = MAX, V_{IN} = 0V, V_{OUT} = 0V	5	-3	-8	-15	mA
$I_{CC(1)}$	Logical "1" State Power Supply Current (Per Gate) (Except DM54L02/DM74L02) (Note 2)	V_{CC} = MAX, V_{IN} (All Inputs) = 0V, I_{OUT} = 0	6		120	200	μA
$I_{CC(0)}$	Logical "0" State Power Supply Current (Per Gate) (Except DM54L02/DM74L02) (Note 3)	V_{CC} = MAX, V_{IN} (All Inputs) = 5V, I_{OUT} = 0	6		330	510	μA

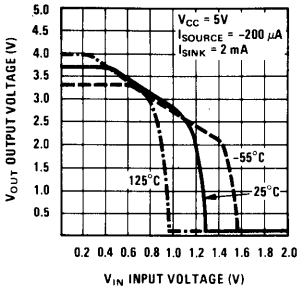
Note 1: All typicals at T_A = 25°C.
Note 2: For the DM54L02/DM74L02, $I_{CC(1)}$ = 400μA Max.
Note 3: For the DM54L02/DM74L02, $I_{CC(0)}$ = 600μA Max.

ac electrical characteristics

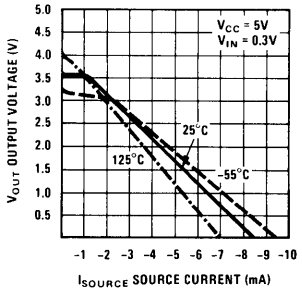
SYMBOL	PARAMETER	CONDITIONS	TEST FIGURE	MIN	TYP	MAX	UNITS
t_{pd0}	Propagation Delay to a Logical "0" (Except DM54L01/DM74L01 DM54L03/DM74L03)	V_{CC} = 5V, C_L = 50 pF, T_A = 25°C	7		30	60	ns
	DM54L30/DM74L30				60	100	ns
t_{pd1}	Propagation Delay to a Logical "1" (Except DM54L01/DM74L01 DM54L03/DM74L03)	V_{CC} = 5V, C_L = 50 pF, T_A = 25°C	7		25	60	ns
t_{pd0}	Propagation Delay to a Logical "0" DM54L01/DM74L01 DM54L03/DM74L03	V_{CC} = 5V, R_L = 4k, C_L = 15 pF, T_A = 25°C	(7)		25	60	ns
t_{pd1}	Propagation Delay to a Logical "1" DM54L01/DM74L01 DM54L03/DM74L03	V_{CC} = 5V, R_L = 4k, C_L = 15 pF, T_A = 25°C	(7)		40	90	ns

typical performance characteristics

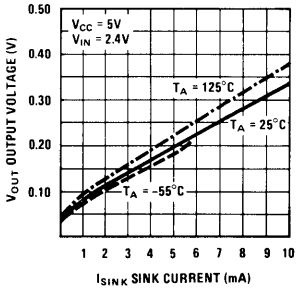
V_{IN} vs V_{OUT}



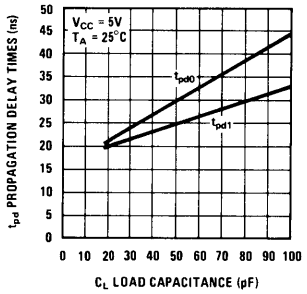
V_{OUT} vs I_{OUT} Logical "1"



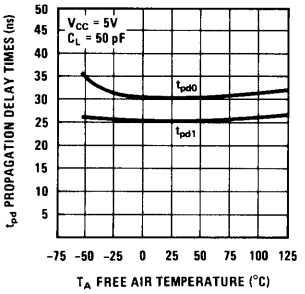
V_{OUT} vs I_{OUT} Logical "0"



Propagation Delay Times vs Load Capacitance



Propagation Delay Times vs Free Air Temperature



DM54L03/DM74L03 open collector application data

The DM54L03/DM74L03 is an open-collector LP TTL gate, that when supplied with a proper load resistor (R_L, can be paralleled with other similar LP TTL gates to perform the wire-AND function, and simultaneously, will drive from one to six loads. When only one gate is wire-AND connected, this gate can be used to drive eight LP TTL gates. To meet these conditions, an appropriate load resistor value must be determined for the desired circuit configuration. A maximum resistor value must be determined so that sufficient load currents (to LP TTL Gate Loads) and Off Currents (To wire-AND connections) will be available during a logical "1" level at output. Also, a minimum resistor value must be determined which will ensure that currents from the loads will not cause the output voltage to rise above the logical "0" level.

To meet both conditions (logical "0" and logical "1"), the value of R_L is determined by:

$$R_L = \frac{V_{RL}}{I_{RL}} \qquad (1)$$

Where;

V_{RL} = Voltage Drop (volts)
I_{RL} = Current (amps)

The following equations will be useful in determining the value of R_L (Max) and R_L (Min):

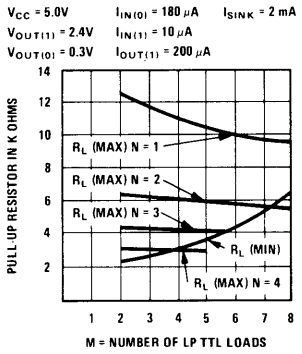
$$R_L\ (\text{Max}) = \frac{V_{CC} - V_{out}(1)}{N \cdot I_{out}(1) + M \cdot I_{in}(1)} \qquad (2)$$

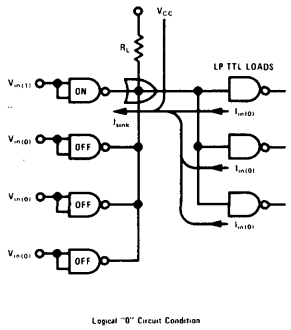
$$R_L\ (\text{Min}) = \frac{V_{CC} - V_{out}(0)}{I_{out}(0) - M\, I_{in}(0)} \qquad (3)$$

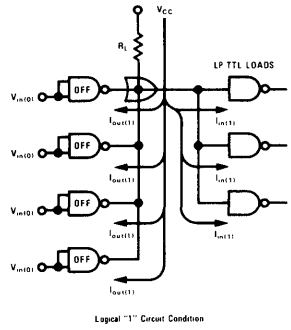
N = number of gates wire-AND connected
M = number of LP TTL loads

DM54L03/DM74LO3 open-collector application data

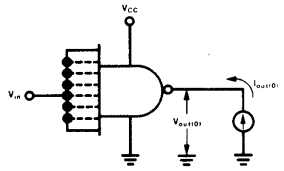
The maximum loads connected (M) under any wire-OR configuration (N) is shown respectively by the intersection of the R_L (Min) and R_L (Max) curves. For instance, for N = 2 and M = 5 the maximum loads connected is six.





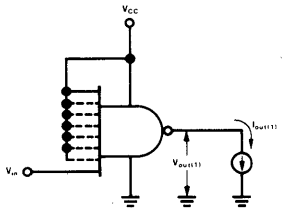


dc test circuits



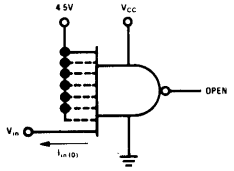
Note: All inputs are tested simultaneously.

Figure 1



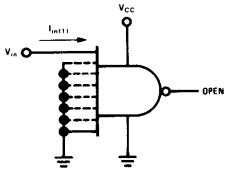
Note: Each input is tested separately.

Figure 2



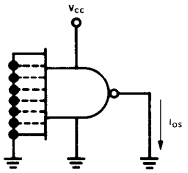
Note: Each input is tested separately.

Figure 3



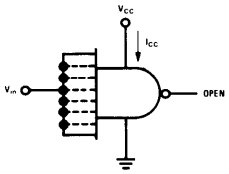
Note: Each input is tested separately.

Figure 4



Note: Each gate is tested separately.

Figure 5



Notes: 1. Logical "0" and Logical "1" conditions are tested.
2. All gates are tested simultaneously.

Figure 6

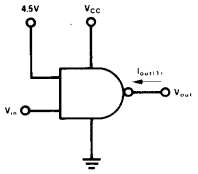
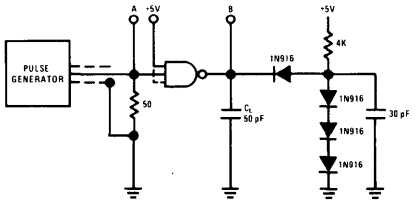
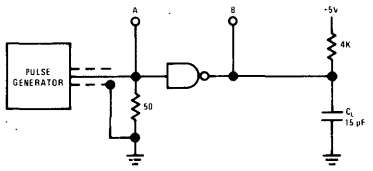


Figure 6a.

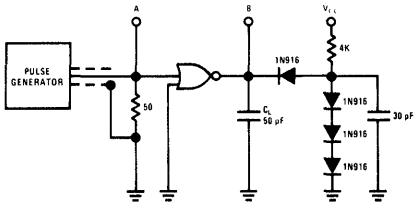
ac test circuits and waveforms



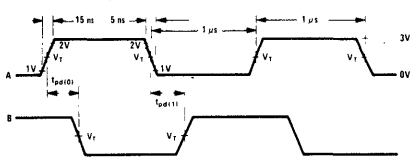
DM54L00/DM74L00, DM54L04/DM74L04
DM54L10/DM74L10, DM54L20/DM74L20
DM54L30/DM74L30



DM54L01/DM74L01
DM54L03/DM74L03



DM54L02/DM74L02



T_A	V_T
125°C	0.9V
70°C	1.1V
25°C	1.3V
0°C	1.4V
−55°C	1.6V

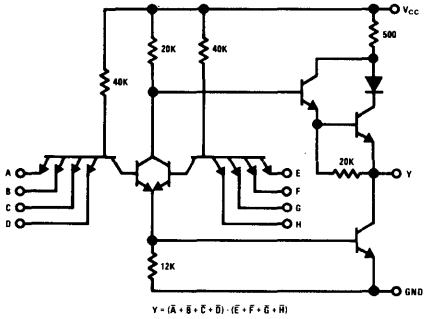
Note: C_L includes probe and jig capacitance.

Figure 7

AND-OR-INVERT GATES

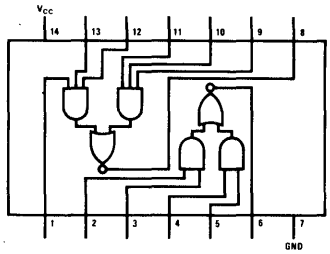
DM54L51/DM74L51, DM54L54/ DM74L54, DM54L55/DM74L55

schematic diagram

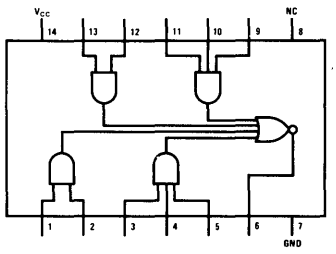


DM54L51/DM74L51, DM54L54/DM74L54, DM54L55/DM74L55
(DM54L55/DM74L55 Shown)

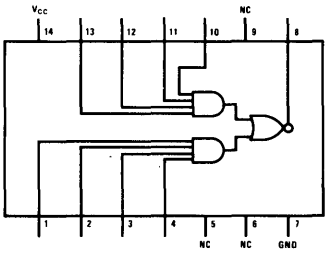
dual-in-line package connection diagrams



DM54L51/DM74L51

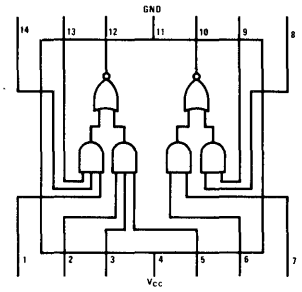


DM54L54/DM74L54

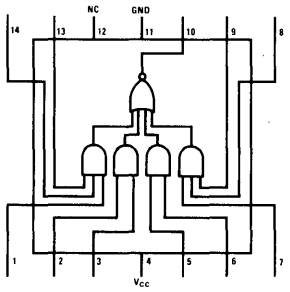


DM54L55/DM74L55

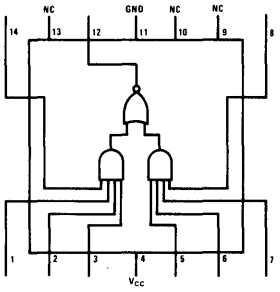
flat package connection diagrams



DM54L51/DM74L51



DM54L54/DM74L54



DM54L55/DM74L55

dc electrical characteristics

SYMBOL	PARAMETER	CONDITIONS (Note 1)	TEST FIGURE	MIN	TYP (Note 2)	MAX	UNITS
$V_{IN(1)}$	Logical "1" Input Voltage	V_{CC} = MIN	8	2	1.3		V
$V_{IN(0)}$	Logical "0" Input Voltage	V_{CC} = MIN	9		1.3	0.7	V
$V_{OUT(1)}$	Logical "1" Output Voltage	V_{CC} = MIN, I_{OUT} = -200 μA, V_{IN} = 0.7V (Each Input Tested Separately)	9	2.4	2.8		
$V_{OUT(0)}$	Logical "0" Output Voltage	V_{CC} = MIN, I_{OUT} = 2 mA, V_{IN} (All Inputs On One Section) = 2.0V, Other Inputs = 0V	8		0.15	0.3	V
$V_{OUT(0)}$	Logical "0" Output Voltage (Series 74L Only)	V_{CC} = MIN, I_{OUT} = 3.2 mA	1			0.4	V
$I_{IN(1)}$	Logical "1" Input Current	V_{CC} = MAX, V_{IN} = 2.4V, Other Inputs = 0V	11		<1	10	μA
		V_{CC} = MAX, V_{IN} = 5.5V, Other Inputs = 0V	11			100	μA
$I_{IN(0)}$	Logical "0" Input Current	V_{CC} = MAX, V_{IN} = 0.3V, Other Inputs = 4.5V	10		-120	-180	μA
I_{OS}	Logical "1" Output Short-Circuit Current	V_{CC} = MAX, V_{IN} (All Inputs) = 0V, V_{OUT} = 0V	12	-3	-8	-15	mA
$I_{CC(1)}$	Logical "1" State Power Supply Current (Per Gate)	V_{CC} = MAX, V_{IN} (All Inputs) = 0V, I_{OUT} = 0 DM54L51/DM74L51	13		240	400	μA
		DM54L54/DM74L54	13		480	800	μA
		DM54L55/DM74L55	13		240	400	μA
$I_{CC(0)}$	Logical "0" State Power Supply Current (Per Gate)	V_{CC} = MAX, V_{IN} (All Inputs) = 5V, I_{OUT} = 0 DM54L51/DM74L51	13		390	650	μA
		DM54L54/DM74L54	13		600	990	μA
		DM54L55/DM74L55	13		390	650	μA

Note 1: Each input "AND" section tested separately.

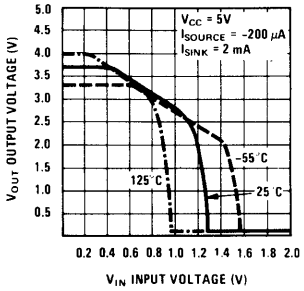
Note 2: All typicals at T_A = 25°C.

ac electrical characteristics

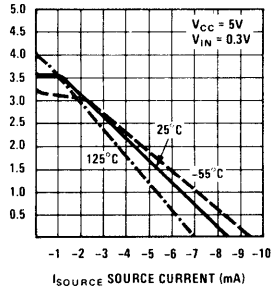
SYMBOL	PARAMETER	TEST CONDITIONS	TEST FIGURE	MIN.	TYP	MAX	UNITS
t_{pd1}	Propagation Delay to a Logical "1"	V_{CC} = 5V, C_L = 50 pF, T_A = 25°C	14		40	90	ns
t_{pd0}	Propagation Delay to a Logical "0"	V_{CC} = 5V, C_L = 50 pF, T_A = 25°C	14		30	60	ns

typical performance characteristics

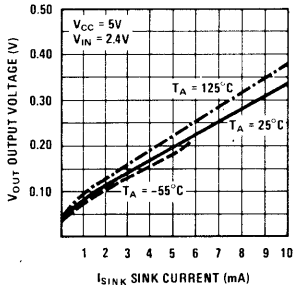
V_{IN} vs V_{OUT}



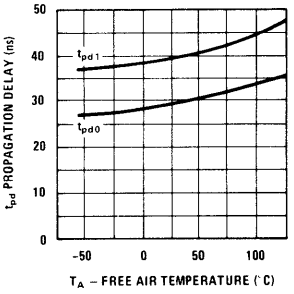
V_{OUT} vs I_{OUT}
Logical "1"



V_{OUT} vs I_{OUT}
Logical "0"

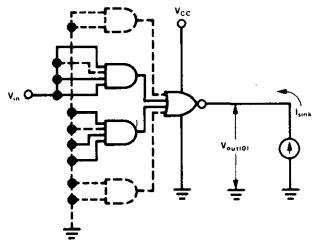


Propagation Delay Times
vs Free Air Temperature



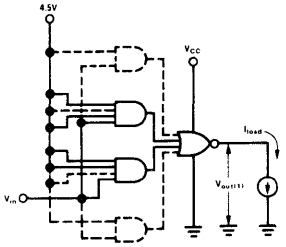
DM54L51/DM74L51
DM54L55/LM74L55

dc test circuits



Note: Each AND section is tested separately.

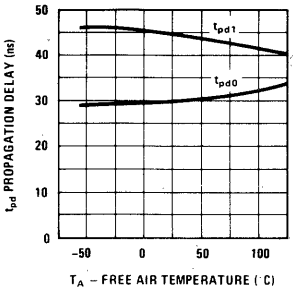
Figure 8



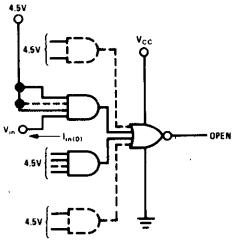
Note: Each set of inputs is tested separately.

Figure 9

Propagation Delay Times
vs Free Air Temperature

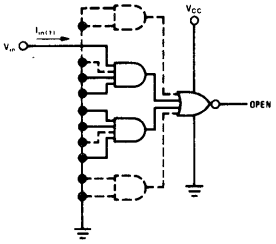


DM54L54/DM74L54 Only



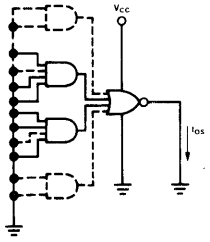
Note: Each input is tested separately.

Figure 10



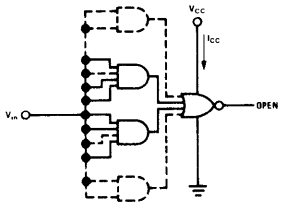
Note: Each input is tested separately.

Figure 11



Note: Each gate is tested separately.

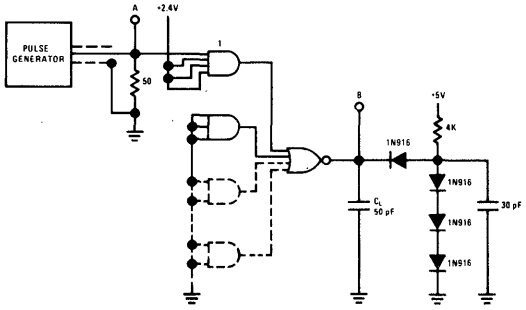
Figure 12

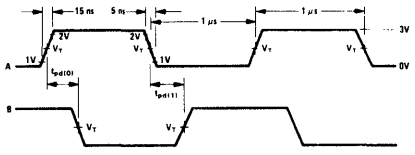


Note: All gates are tested simultaneously.

Figure 13

ac test circuit and waveforms





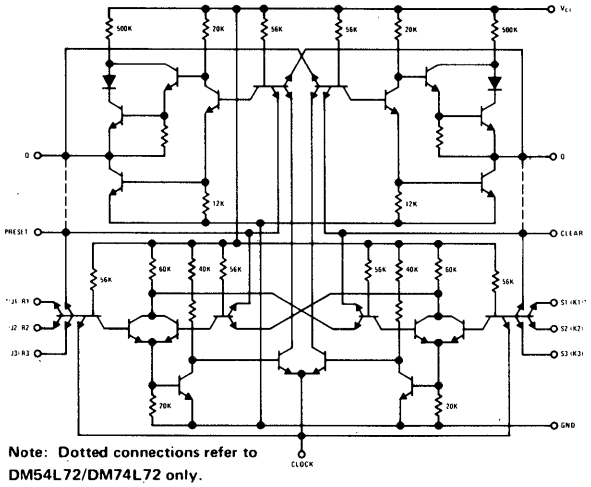
T_A	V_T
125°C	0.9V
70°C	1.1V
25°C	1.3V
0°C	1.4V
−55°C	1.6V

Note: C_L includes probe and jig capacitance.

Figure 14

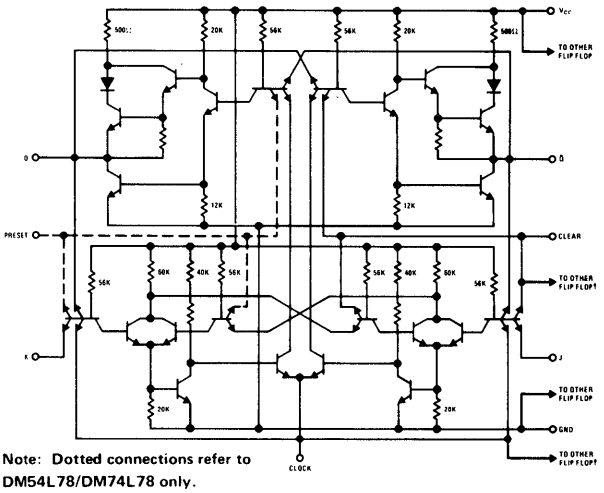
FLIP FLOPS DM54L71/DM74L71, DM54L72/DM74L72, DM54L73/DM74L73, DM54L74/DM74L74, DM54L78/DM74L78

schematic diagrams



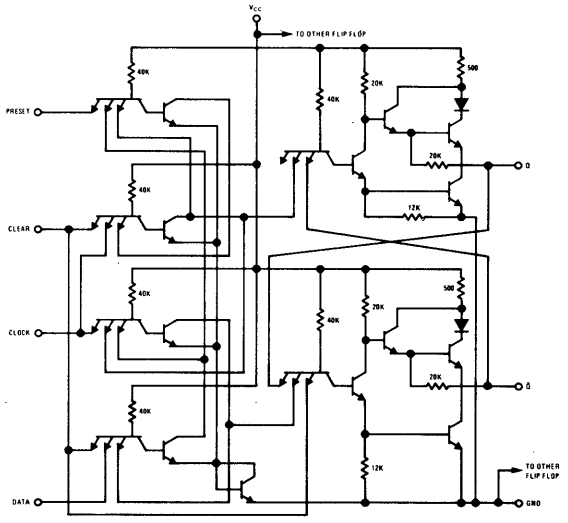
Note: Dotted connections refer to DM54L72/DM74L72 only.

DM54L71/DM74L71, DM54L72/DM74L72



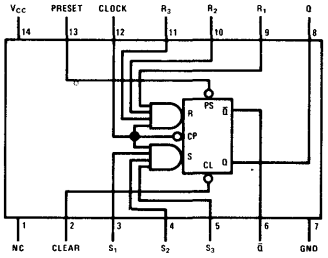
Note: Dotted connections refer to DM54L78/DM74L78 only.

DM54L73/DM74L73, DM54L78/DM74L78

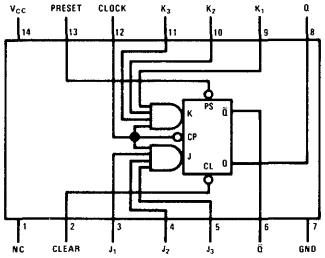


DM54L74/DM74L74
(Shows one flip flop only)

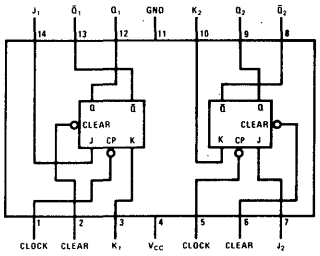
dual-in-line package connection diagrams



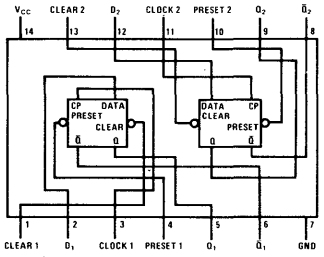
DM54L71/DM74L71



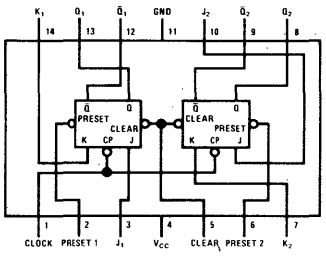
DM54L72/DM74L72



DM54L73/DM74L73

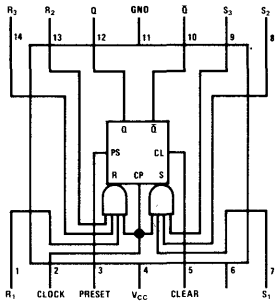


DM54L74/DM74L74

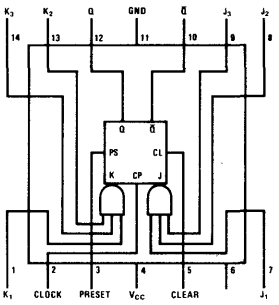


DM54L78/DM74L78

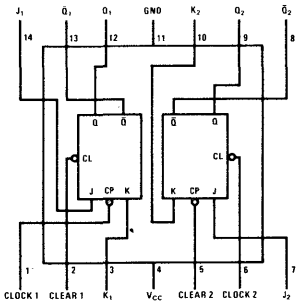
flat package connection diagrams



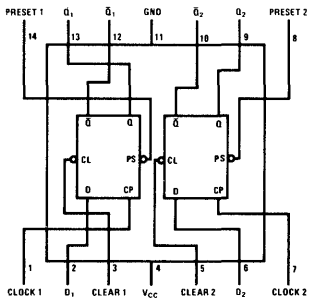
DM54L71/DM74L71



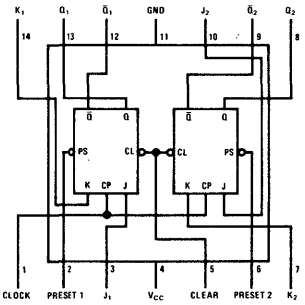
DM54L72/DM74L72



DM54L73/DM74L73



DM54L74/DM74L74



DM54L78/DM74L78

dc electrical characteristics

SYMBOL	PARAMETER	CONDITIONS		TEST FIGURE DM54L71/ DM74L71	DM54L72/ DM74L72	DM54L73/ DM74L73	DM54L74/ DM74L74	DM54L78/ DM74L78	MIN	TYP (Note 1)	MAX	UNITS
$V_{IN(1)}$	Logical "1" Input Voltage	V_{CC} = MIN		15, 16	20, 21	25, 26	31, 32	25, 26	2	1.3		V
$V_{IN(0)}$	Logical "0" Input Voltage	V_{CC} = MIN		15, 16	20, 21	25, 26	31, 32	25, 26		1.3	0.7	V
$V_{IN(0)CP}$	Logical "0" Input Voltage at Clock	V_{CC} = MIN		15, 16	20, 21	25, 26	31, 32	25, 26		1.2	0.6	V
$V_{OUT(1)}$	Logical "1" Output Voltage	V_{CC} = MIN, I_{OUT} = -200 μA		15	20	25	31	25	2.4	2.8		V
$V_{OUT(0)}$	Logical "0" Output Voltage	V_{CC} = MIN, I_{OUT} = 2 mA		16	21	26	32	26		0.15	0.3	V
$V_{OUT(0)}$	Logical "0" Output Voltage (Series 74L Only)	V_{CC} = MIN, I_{OUT} = 3.2 mA, V_{IN} (All Inputs) = 2V		16	21	26	32	26			0.4	V
$I_{IN(1)RSJKD}$	Logical "1" Input Current at R,S,J,K, or Data	V_{CC} = MAX, V_{IN} = 2.4V V_{CC} = MAX, V_{IN} = 5.5V		18 18	23 23	28 28	34 34	28 28		<1 	10 100	μA μA
$I_{IN(1)P}$	Logical "1" Input Current at Preset	V_{CC} = MAX, V_{IN} = 2.4V V_{CC} = MAX, V_{IN} = 5.5V		18 18	23 23	– –	34 –	28 –		<2 	20 200	μA μA
$I_{IN(1)C}$	Logical "1" Input Current at Clear	V_{CC} = MAX, V_{IN} = 2.4V	DM54L71/DM74L71 DM54L72/DM74L72 DM54L73/DM74L73	18	23	28	–	–		<2	20	μA
			DM54L74/DM74L74	–	–	–	34	–		<3	30	μA
			DM54L78/DM74L78	–	–	–	–	28		<4	40	μA
		V_{CC} = MAX, V_{IN} = 5.5V	DM54L71/DM74L71 DM54L72/DM74L72 DM54L73/DM74L73	18	23	28	–	–			200	μA
			DM54L74/DM74L74	–	–	–	34	–			300	μA
			DM54L78/DM74L78	–	–	–	–	28			400	μA
$I_{IN(1)CP}$	Logical "1" Input Current at Clock	V_{CC} = MAX, V_{IN} = 2.4V	DM54L71/DM74L71 DM54L72/DM74L72 DM54L73/DM74L73	18	23	28	–	–	0	-50	-200	μA
			DM54L74/DM74L74	–	–	–	34	–		<2	20	μA
			DM54L78/DM74L78	–	–	–	–	28	0	-100	-400	μA
		V_{CC} = MAX, V_{IN} = 5.5V	DM54L71/DM74L71 DM54L72/DM74L72 DM54L73/DM74L73 DM54L74/DM74L74	18	23	28	34	–			200	μA
			DM54L78/DM74L78	–	–	–	–	28			400	μA
$I_{IN(0)RSJKD}$	Logical "0" Input Current at R,S,J,K or Data	V_{CC} = MAX, V_{IN} = 0.3V		17	22	28	33	27		-120	-180	μA
$I_{IN(0)P}$	Logical "0" Input Current at Preset	V_{CC} = MAX, V_{IN} = 0.3V	DM54L71/DM74L71 DM54L72/DM74L72 DM54L78/DM74L78	17	22	–	–	27		-240	-360	μA
			DM54L74/DM74L74	–	–	–	33	–		-120	-180	μA
$I_{IN(0)C}$	Logical "0" Input Current at Clear	V_{CC} = MAX, V_{IN} = 0.3V	DM54L71/DM74L71 DM54L72/DM74L72 DM54L73/DM74L73 DM54L74/DM74L74	17	22	27	33	–		-240	-360	μA
			DM54L78/DM74L78	–	–	–	–	27		-480	-720	μA
I_{OS}	Short-Circuit Output Current	V_{CC} = MAX		19	24	29	35	30	-3	-9	-15	mA
I_{CC}	Power Supply Current (per F/F)	V_{CC} = MAX, V_{IN} CLOCK = 0V		18	23	28	34	28			1.44	mA

Note 1: All typicals at $T_A = 25°C$, $V_{CC} = 5V$

switching characteristics

SYMBOL	PARAMETER	CONDITIONS		TEST FIGURE DM54L71/ DM74L71	DM54L72/ DM74L72	DM54L73/ DM74L73	DM54L74/ DM74L74	DM54L78/ DM74L78	MIN	TYP (Note 1)	MAX	UNITS
F_{CLOCK}	Maximum Clock Frequency	C_L = 50 pF, R_L = 4 KΩ, V_{CC} = 5V All F/F		36	36	36	38	36	6	11		MHz
$t_{pd0\ CLOCK}$	Propagation Delay to a Logical "0" From Clock	C_L = 50 pF, R_L = 4 KΩ, V_{CC} = 5V	DM54L71/DM74L71 DM54L72/DM74L72 DM54L73/DM74L73 DM54L78/DM74L78	36	36	36	–	36	10	60	150	ns
			DM54L74/DM74L74	–	–	–	38	–	25	75	120	ns
$t_{pd1\ CLOCK}$	Propagation Delay to a Logical "1" From Clock		DM54L71/DM74L71 DM54L72/DM74L72 DM54L73/DM74L73 DM54L78/DM74L78	36	36	36		36	10	30	75	ns
			DM54L74/DM74L74	–	–	–	38	–	15	40	90	ns
$t_{pd1\ CLEAR,PRESET}$	Propagation Delay to a Logical "1" From Clear		DM54L71/DM74L71 DM54L72/DM74L72 DM54L73/DM74L73 DM54L78/DM74L78	37	37	37	–	37		30	75	ns
			DM54L74/DM74L74	–	–	–	37	–		25	60	ns
$t_{pd0\ CLEAR,PRESET}$	Propagation Delay to a Logical "0" From Preset	C_L = 50 pF, R_L = 4 KΩ, V_{CC} = 5V $V_{IN\ CLOCK}$ = 2.4 or 0V	DM54L71/DM74L71 DM54L72/DM74L72 DM54L73/DM74L73 DM54L78/DM74L78	37	37	37	–	37		70	150	ns
			DM54L74/DM74L74	–	–	–	37	–		60	120	ns

Note 1: All typicals at $T_A = 25°C$ and $V_{CC} = 5V$.

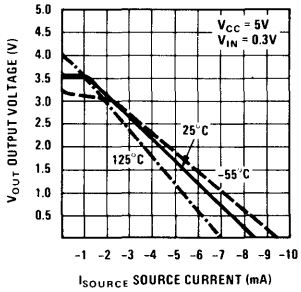
switching characteristics (cont.)

SYMBOL	PARAMETER	CONDITIONS		TEST FIGURE DM54L71/ DM74L71	DM54L72/ DM74L72	DM54L73/ DM74L73	DM54L74/ DM74L74	DM54L78/ DM74L78	MIN	TYP (Note 1)	MAX	UNITS
$t_{p\,CLOCK}$	Minimum Clock Pulse Width	C_L = 50 pF, R_L = 4 KΩ, V_{CC} = 5V	DM54L71/DM74L71 DM54L72/DM74L72 DM54L73/DM74L73 DM54L78/DM74L78	36	36	36	–	36	200	65		ns
			DM54L74/DM74L74	–	–	–	38	–	75	40		ns
$t_{p\,CLEAR,PRESET}$	Minimum Clear or Preset Pulse Width	C_L = 50 pF, R_L = 4 KΩ, V_{CC} = 5V	DM54L71/DM74L71 DM54L72/DM74L72 DM54L73/DM74L73 DM54L78/DM74L78	37	37	37	–	37	100	60		ns
			DM54L74/DM74L74	–	–	–	37	–	75	40		ns
t_{SETUP}	Data Setup Time	C_L = 50 pF, R_L = 4 KΩ, V_{CC} = 5V	DM54L71/DM74L71	36	–	–	–	–	100			ns
			DM54L72/DM74L72 DM54L73/DM74L73 DM54L78/DM74L78	–	36	36	–	36	$\geq t_{pw\,CLOCK}$			ns
			DM54L74/DM74L74	–	–	–	38	–	30	15		ns
t_{HOLD}	Data Hold Time	C_L = 50 pF, R_L = 4 KΩ, V_{CC} = 5V	DM54L71/DM74L71 DM54L72/DM74L72 DM54L73/DM74L73 DM54L78/DM74L78	36	36	36	–	36	0			ns
		Logical "1"	DM54L74/DM74L74	–	–	–	38	–		10	15	ns
		Logical "0"	DM54L74/DM74L74	–	–	–	38	–		5	10	ns

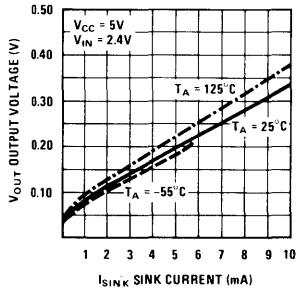
Note 1: All typicals at T_A = 25°C and V_{CC} = 5V.

all flip flops

I_{SOURCE} vs V_{OUT}

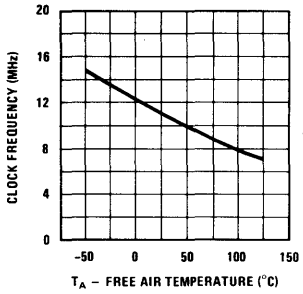


I_{SINK} vs V_{OUT}



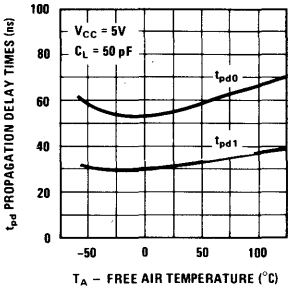
typical performance characteristics

Maximum Clock Frequency vs Free Air Temperature



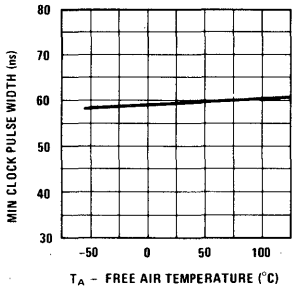
DM54L71/DM74L71
DM54L72/DM74L72
DM54L73/DM74L73
DM54L78/DM74L78

Propagation Delay From Clock vs Free Air Temperature



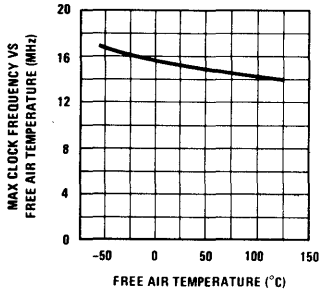
DM54L71/DM74L71
DM54L72/DM74L72
DM54L73/DM74L73
DM54L78/DM74L78

Minimum Clock Pulse Width vs Temperature



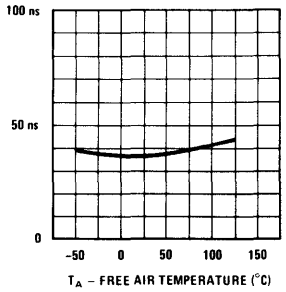
DM54L71/DM74L71
DM54L72/DM74L72
DM54L73/DM74L73
DM54L78/DM74L78

Maximum Clock Frequency vs Free Air Temperature



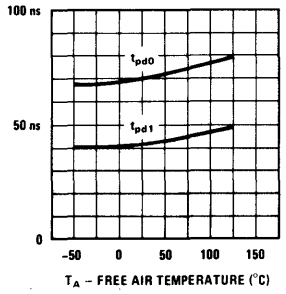
DM54L74/DM74L74

Minimum Clock Pulse Width



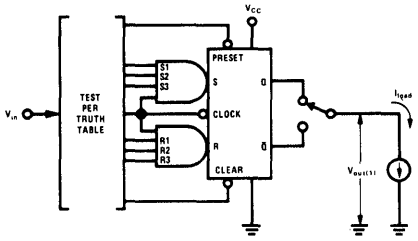
DM54L74/DM74L74

Propagation Delay From Clock vs Temperature



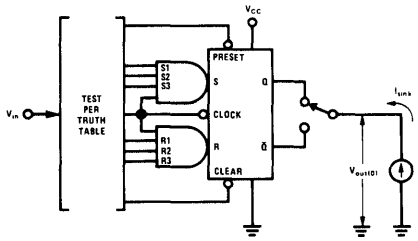
DM54L74/DM74L74

dc test circuits



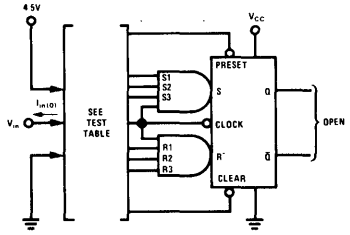
Note: Each input is tested separately.

Figure 15



Note: Each input is tested separately.

Figure 16

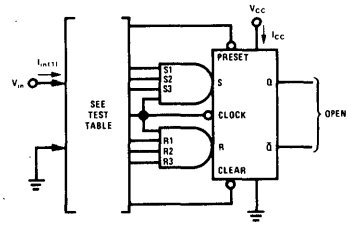


Note: Each input is tested separately.

TEST TABLE

Apply V_{in} (Test $I_{in(0)}$)	Apply 4.5 V
Clock	Preset, R1, R2, R3, S1, S2, and S3
Clock	Clear, R1, R2, R3, S1, S2, and S3
Preset	R1, R2, R3, S1, S2, and S3
Clear	R1, R2, R3, S1, S2, and S3
R1	Preset, Clock, R2, and R3
R2	Preset, Clock, R1, and R3
R3	Preset, Clock, R1, and R2
S1	Clear, Clock, S2, and S3
S2	Clear, Clock, S1, and S3
S3	Clear, Clock, S1, and S2

Figure 17

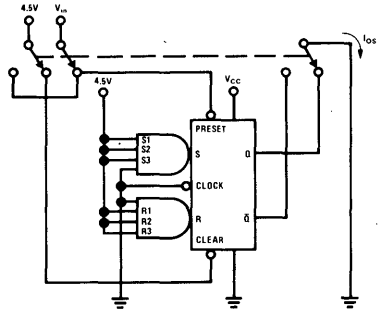


Note: Each output is tested separately.

TEST TABLE

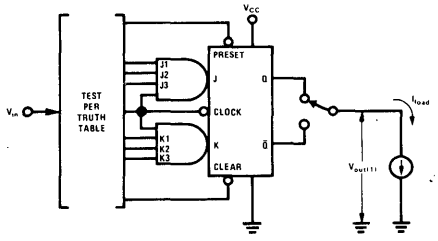
Apply V_{in} (Test $I_{in(1)}$)	Ground
Clock	Preset, Clear, R1, R2, R3, S1, S2, and S3
Preset	Clock, R1, R2, and R3
Clear	Clock, S1, S2, and S3
R1	Clock, Preset, R2, and R3
R2	Clock, Preset, R1, and R3
R3	Clock, Preset, R1, and R2
S1	Clock, Clear, S2, and S3
S2	Clock, Clear, S1, and S3
S3	Clock, Clear, S1, and S2

Figure 18



Note: Each output is tested separately.

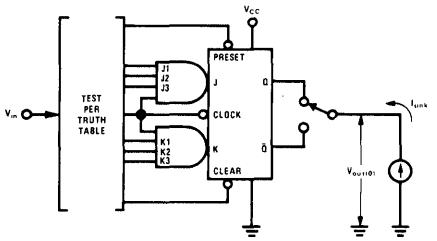
Figure 19



Note: Each input is tested separately.

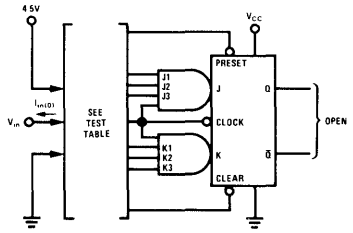
Figure 20

dc test circuits (cont.)



Note: Each output is tested separately.

Figure 21

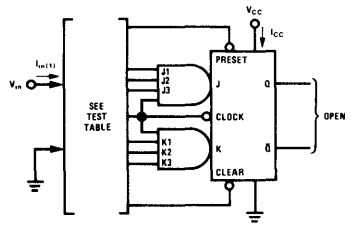


Note: Each output is tested separately.

TEST TABLE

Apply V_{in} (Test $I_{in(0)}$)	Apply Momentary GND, then 4.5V	Apply 4.5V
Clock	Preset	J1, J2, J3, K1, K2, and K3
Clock	Clear	J1, J2, J3, K1, K2, and K3
Preset	None	J1, J2, J3, K1, K2, and K3
Clear	None	J1, J2, J3, K1, K2, and K3
J1	Clear	Clock, J2, and J3
J2	Clear	Clock, J1, and J3
J3	Clear	Clock, J1, and J2
K1	Preset	Clock, K2, and K3
K2	Preset	Clock, K1, and K3
K3	Preset	Clock, K1, and K2

Figure 22

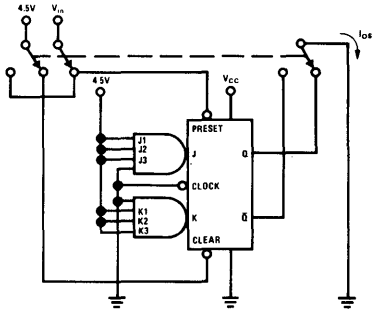


Note: Each input is tested separately.

TEST TABLE

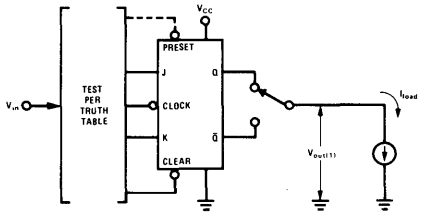
Apply V_{in} (Test $I_{in(1)}$)	Ground
Clock	Preset, Clear, J1, J2, J3, K1, K2, and K3
Preset	Clock, K1, K2, and K3
Clear	Clock, J1, J2, and J3
J1	Clock, Clear, J2, and J3
J2	Clock, Clear, J1, and J3
J3	Clock, Clear, J1, and J2
K1	Clock, Preset, K2, and K3
K2	Clock, Preset, K1, and K3
K3	Clock, Preset, K1, and K2

Figure 23



Note: Each output is tested separately.

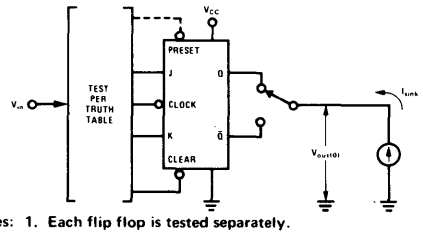
Figure 24



Notes: 1. Each flip flop is tested separately.
2. Each output is tested separately.
3. Preset is applicable for DM54L78/DM74L78 circuits only.

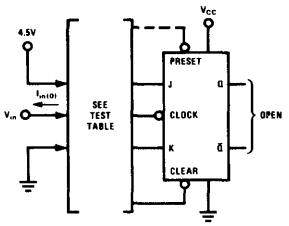
Figure 25

dc test circuits (cont.)



Notes: 1. Each flip flop is tested separately.
2. Each output is tested separately.
3. Preset is applicable for DM54L78/DM74L78 circuits only.

Figure 26

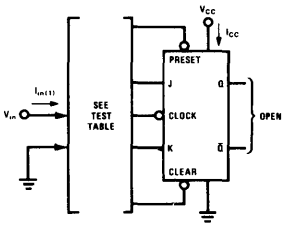


TEST TABLE

Apply V_{in} (Test $I_{in(0)}$)	Apply Momentary GND	Apply 4.5 V
Clock	Clear (See Note 2)	J and K
Clear	None	Clock and J
Preset	None (See Note 5)	Clock and K
J	Q (See Note 3)	Clock and Clear
K	$\bar{Q}$ (See Note 3)	Clock and Clear

Notes: 1. Each flip flop is tested separately.
2. Apply momentary ground, then 4.5V
3. After application of momentary ground, Q and $\bar{Q}$ are left floating.
4. Ground all input at the unused flip flop.
5. Preset is applicable for DM54L78/DM74L78 circuits only.

Figure 27



TEST TABLE

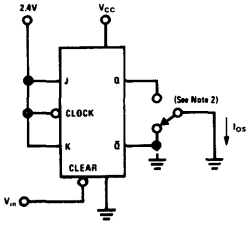
Apply V_{in} (Test $I_{in(1)}$)	Ground	Apply Momentary GND, then 4.5 V
Clock	Clear, J, and K	None
Clear	Clock and J	None
Preset (See Note 1)	Clock and K	None
J (See Note 1)	Clock and Clear	Preset
K (See Note 3)	Clock and Preset	Clear

Notes: 1. Preset is applicable for DM54L78/DM74L78 circuits only.
2. I_{CC} is measured (simultaneously for both flip flops) for the following conditions:
a. J = K = Clock = Clear = Gnd for DM54L78/DM74L78, Preset = 4.5V.
b. For DM54L73/DM74L73: J = Clear = 4.5V, K = Gnd, and apply momentary 4.5V, then Gnd, to Clock.
For DM54L78/DM74L78: J = K = Clock = Preset = Gnd and Clear = 4.5V.

$$\text{Average per flip flop} = \frac{I_{CC\ total}}{2}$$

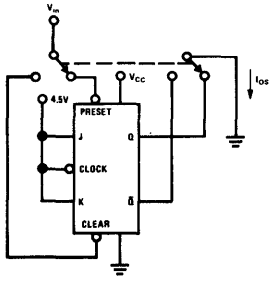
3. Each flip flop is tested separately for $I_{in(1)}$.

Figure 28



Notes: 1. Each flip flop is tested separately.
2. Test circuit shows setup for testing $\bar{Q}$. When testing Q, open all inputs and ground $\bar{Q}$.

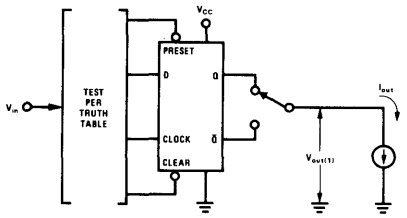
Figure 29



Note: Each flip flop is tested separately.

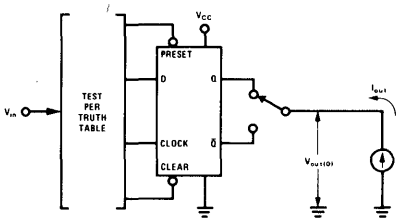
Figure 30

dc test circuits (cont.)



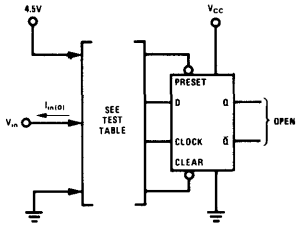
Notes: 1. Each flip flop is tested separately.
2. Each output is tested separately.

Figure 31



Notes: 1. Each flip flop is tested separately.
2. Each output is tested separately.

Figure 32

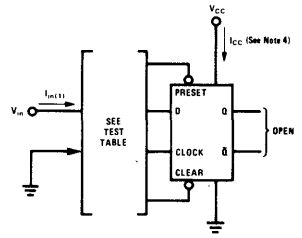


TEST TABLE

APPLY V_I (TEST I_{IL})	APPLY 4.5V	APPLY GND
Clock	Clear	Preset and D
Preset	None	Clear, Clock, and D
Clear	Clock and D	Preset
D	Clear and Clock	Preset

Notes: 1. Each flip flop is tested separately.
2. Each input is tested separately.

Figure 33

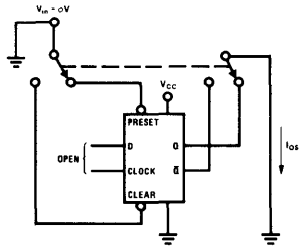


TEST TABLE

APPLY V_I (TEST I_{IH})	APPLY 4.5V	APPLY GND
Clock	Clear and D	Preset
Clock	Preset and D	Clear
Preset	Clear and D	Clock (See Note 3)
Clear	Preset	Clock and D
Clear	Preset	D and Clock (See Note 3)
D	Preset and clock	Clear

Notes: 1. Each flip flop is tested separately.
2. Each input is tested separately.
3. GND is momentarily applied to clock, then 4.5V.
4. I_{CC} is measured with D, clock, and preset at GND, then with D, clock and clear at GND.

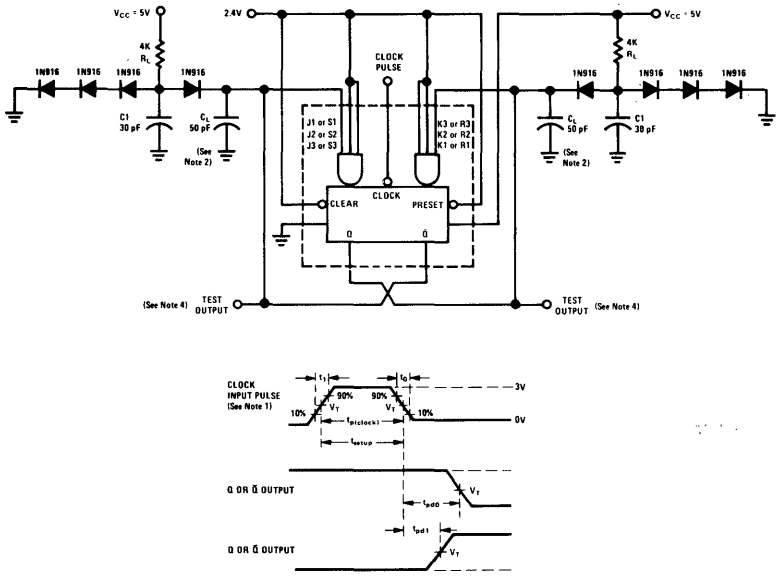
Figure 34



Note: Each output is tested separately.

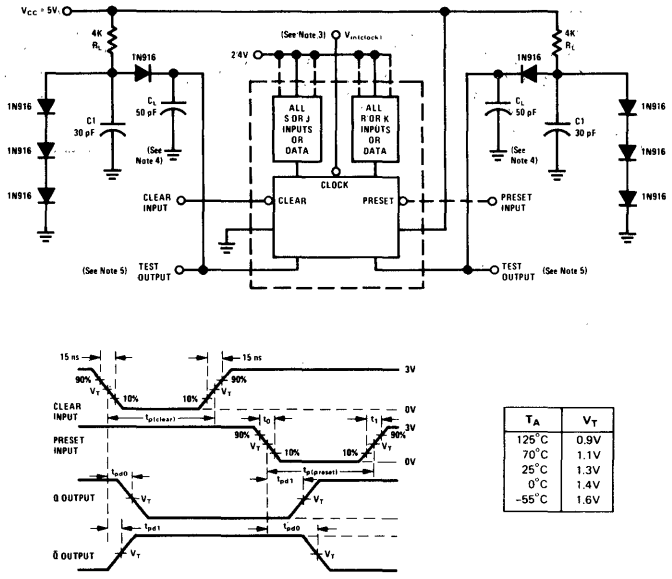
Figure 35

ac test circuits and waveforms



Notes: 1. Clock input characteristics: $t_1 = t_0 = 15$ ns, $t_p \geq 200$ ns, and PRR = 500 kHz. When testing f_{clock}, use 50% duty cycle.
2. C_L includes probe and jig capacitance.
3. DM54L73/DM74L73 and DM54L78/DM74L78, J = K = 2.4V.
4. Load is applied to both outputs.

Figure 36

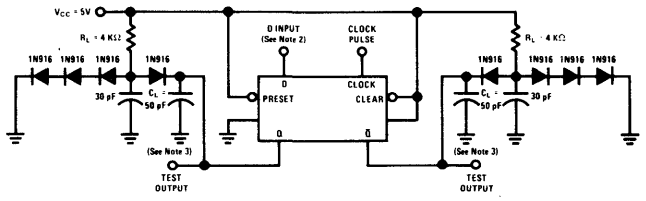


T_A	V_T
125°C	0.9V
70°C	1.1V
25°C	1.3V
0°C	1.4V
-55°C	1.6V

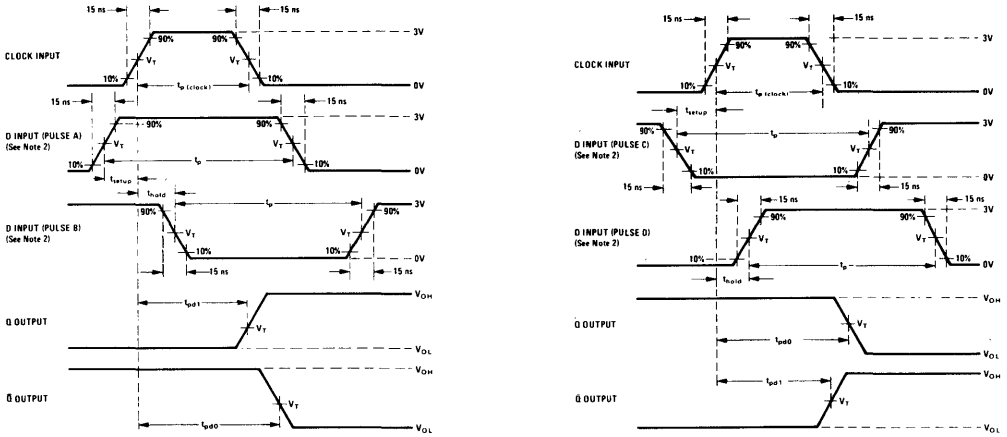
Notes: 1. Clear or preset inputs dominate regardless of the state of clock or logic inputs.
2. Clear or preset input pulse characteristics: $t_{p(clear)} = t_{p(preset)} \geq 100$ ns, and PRR = 500 kHz.
3. See applicable circuit type for actual synchronous and asynchronous input configuration.
4. C_L includes probe and jig capacitance.
5. Load is applied to both outputs.

Figure 37

ac test circuits and waveforms (cont.)



T_A	V_T
125°C	0.9V
70°C	1.1V
25°C	1.3V
0°C	1.4V
−55°C	1.6V

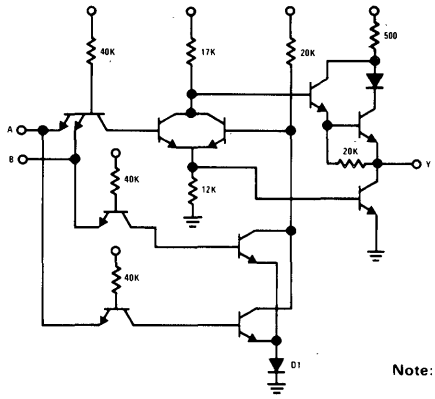


Notes: 1. Clock input pulse has the following characteristics: $t_{p(clock)} \geq 200$ ns and PRR = 500 kHz. When testing f_{clock}, use 50% duty cycle.
2. D input (pulse A and C) have the following characteristics: t_{setup} = 30 ns, t_p = 100 ns and PRR is 50% of the clock PRR.
D input (pulse B) has the following characteristics: t_{hold} = 15 ns, t_p = 80 ns and PRR is 50% of the clock PRR.
D input (pulse D) has the following characteristics: t_{hold} = 10 ns, t_p = 80 ns and PRR is 50% of the clock PRR.
3. C_L includes probe and jig capacitance.

Figure 38

EXCLUSIVE-OR GATES DM54L86/DM74L86

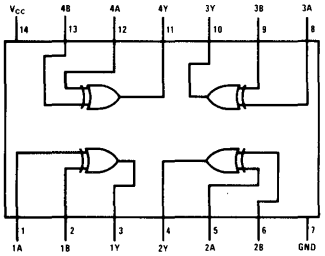
schematic diagram



Note: Schematic diagram shows only one of the four exclusive OR-gates.

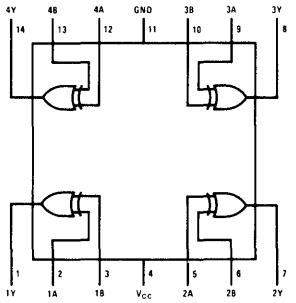
DM54L86/DM74L86

dual-in-line package connection diagram



DM54L86/DM74L86

flat package connection diagram



DM54L86/DM74L86

dc electrical characteristics

SYMBOL	PARAMETER	TEST FIGURE	CONDITIONS (Note 1)	MIN	TYP (Note 2)	MAX	UNITS
$V_{IN(1)}$	Input Voltage Required to Ensure Logical "1" at Any Input Terminal	39	V_{CC} = MIN	2	1.3		V
$V_{IN(0)}$	Input Voltage Required to Ensure Logical "0" at Any Input Terminal	39	V_{CC} = MIN		1.3	0.7	V
$V_{OUT(1)}$	Logical "1" Output Voltage	39	V_{CC} = MIN, $V_{IN(1)}$ = 2V, $V_{IN(0)}$ = 0.7V, I_{LOAD} = -200 μA	2.4	2.8		V
$V_{OUT(0)}$	Logical "0" Output Voltage	40	V_{CC} = MIN, $V_{IN(1)}$ = 2V, $V_{IN(0)}$ = 0.7V, I_{SINK} = 2 mA		0.15	0.3	V
$V_{OUT(0)}$	Logical "0" Output Voltage (Series 74L Only)	1	V_{CC} = MIN, I_{OUT} = 3.2 mA V_{IN} (All Inputs) = 2V		0.2	0.4	V
$I_{IN(1)}$	Logical "1" Level Input Current (Each Input)	41	V_{CC} = MAX, V_{IN} = 2.4V V_{CC} = MAX, V_{IN} = 5.5V		<2	20 200	μA μA
$I_{IN(0)}$	Logical "0" Level Input Current (Each Input)	42	V_{CC} = MAX, V_{IN} = 0.3V		-0.22	-0.36	mA
I_{OS}	Short Circuit Output Current	43	V_{CC} = MAX, $V_{IN(1)}$ = 4.5V, $V_{IN(0)}$ = 0	-3	-9	-15	mA
$I_{CC(0)}$	Supply Current (Per Gate)	44	V_{CC} = MAX			5.5	mA
$I_{CC(1)}$	Supply Current (Per Gate)	43	V_{CC} = MAX, $V_{IN(1)}$ = 4.5V, $V_{IN(0)}$ = 0			3.6	mA

Note 1: For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable circuit type.

Note 2: All typicals at T_A = 25°C and V_{CC} = 5V.

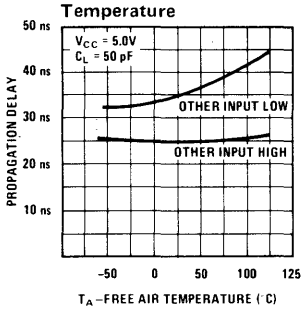
switching characteristics

SYMBOL	PARAMETER	TEST FIGURE	CONDITIONS	MIN	TYP (Note 1)	MAX	UNITS
t_{pd0}	Propagation Delay Time to Logical "0" Level (Other Input Low)	45	C_L = 50 pF, R_L = 4 kΩ		21	60	ns
t_{pd1}	Propagation Delay Time to Logical "1" Level (Other Input Low)	45	C_L = 50 pF, R_L = 4 kΩ		37	60	ns
t_{pd0}	Propagation Delay Time to Logical "0" Level (Other Input High)	45	C_L = 50 pF, R_L = 4 kΩ		35	60	ns
t_{pd1}	Propagation Delay Time to Logical "1" Level (Other Input High)	45	C_L = 50 pF, R_L = 4 kΩ		25	60	ns

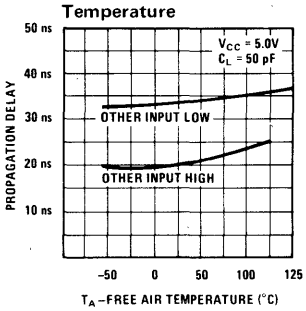
Note 1: All typicals at T_A = 25°C and V_{CC} = 5V.

typical performance characteristics

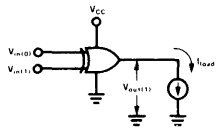
Propagation Delay to a Logical "1" vs Ambient Temperature



Propagation Delay to a Logical "0" vs Ambient Temperature

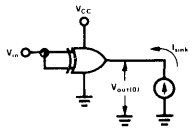


dc test circuits



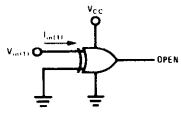
Note: Each input is tested separately.

Figure 39



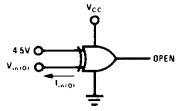
Note: Logical "0" and logical "1" input conditions are tested.

Figure 40



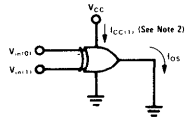
Note: Each input is tested separately.

Figure 41



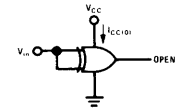
Note: Each input is tested separately.

Figure 42



Notes: 1. Each gate is tested separately.
2. When testing $I_{CC(1)}$, the output is open.

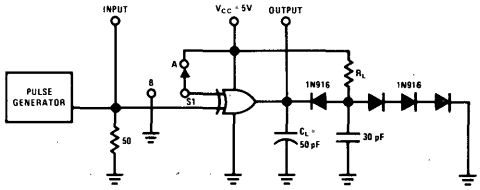
Figure 43



Note: Logical "0" and logical "1" input conditions are tested.

Figure 44

ac test circuit and waveforms



Note: C_L includes probe and jig capacitance.

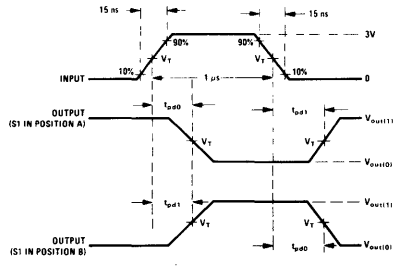


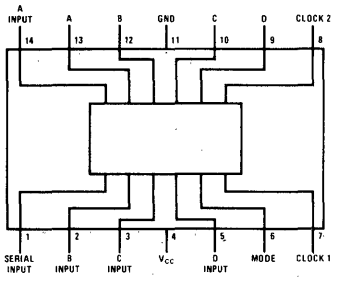
Figure 45

T_A	V_T
125°C	0.9V
70°C	1.1V
25°C	1.3V
0°C	1.4V
-55°C	1.6V

SHIFT REGISTERS DM54L95/DM74L95, DM76L70/DM86L70

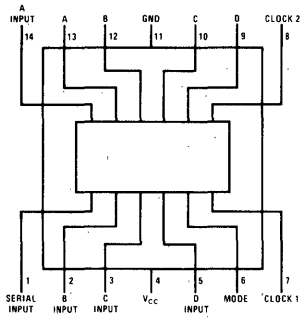
(DM54L95/DM74L95)

dual-in-line package connection diagram



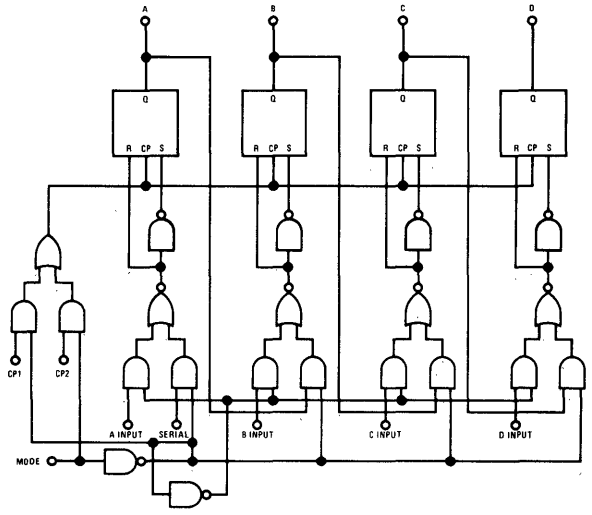
DM54L95/DM74L95

flat package connection diagram



DM54L95/DM74L95

logic diagram



TRUTH TABLE

Mode	Ser_n	Inp A_n	Inp B_n	Inp C_n	Inp D_n	A_{n+1}	B_{n+1}	C_{n+1}	D_{n+1}
1	–	1	1	1	1	1	1	1	1
1		0	0	0	0	0	0	0	0
0	1	–	–	–	–	1	An	Bn	Cn
0	0					0	An	Bn	Cn

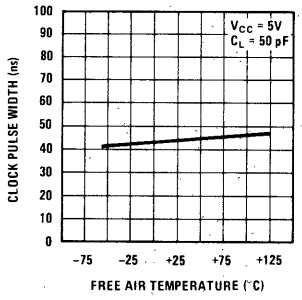
DM54L95/DM74L95

dc electrical characteristics (DM54L95/DM74L95)

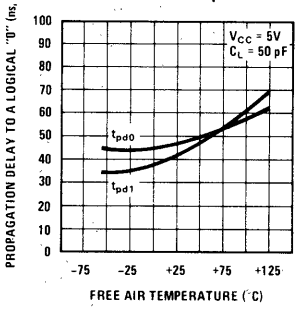
SYMBOL	PARAMETER	CONDITIONS		TEST FIGURE	MIN	TYP	MAX	UNITS
$V_{IN(1)}$	Logical "1" Input Voltage	V_{CC} = MIN		46, 48	2.0			V
$V_{IN(0)}$	Logical "0" Input Voltage	V_{CC} = MIN		47, 49			0.7	
$V_{OUT(1)}$	Logical "1" Output Voltage	V_{CC} = MIN	I_{OUT} = -200 μA	46, 48	2.4	3.1		
$V_{OUT(0)}$	Logical "0" Output Voltage	V_{CC} = MIN	I_{SINK} = +2 mA	47, 49		0.13	0.3	V
$V_{OUT(0)}$	Logical "0" Output Voltage	V_{CC} = MIN	I_{OUT} = 3.2 mA	47, 49		0.2	0.4	V
$I_{IN(0)}$	Logical "0" Input Current (Except Mode)	V_{CC} = MAX	V_{IN} = 0.3V	50		-0.1	-0.18	mA
$I_{IN(0)}$	Logical "0" Input Current (Mode Only)	V_{CC} = MAX	V_{IN} = 0.3V	50		-0.2	-0.36	mA
$I_{IN(1)}$	Logical "1" Input Current (Except Mode)	V_{CC} = MAX	V_{IN} = 2.4V V_{IN} = 5.5V	51			10 100	μA μA
$I_{IN(1)}$	Logical "1" Input Current (Mode Only)	V_{CC} = MAX	V_{IN} = 2.4V V_{IN} = 5.5V	51			20 200	μA μA
I_{OS}	Short-Circuit Output Current	V_{CC} = MAX	V_{OUT} = 0V	52	-3	-9	-15	mA
I_{CC}	Supply Current	V_{CC} = MAX		53		4.8	8.0	mA

typical performance characteristics (DM54L95/DM74L95)

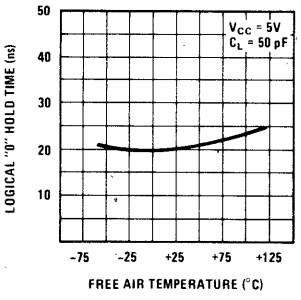
Minimum Clock Pulse Width vs Free Air Temperature



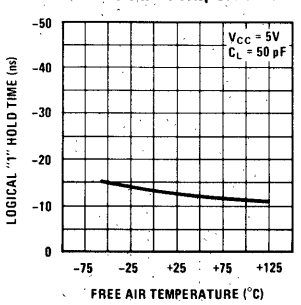
Propagation Delay vs Free Air Temperature



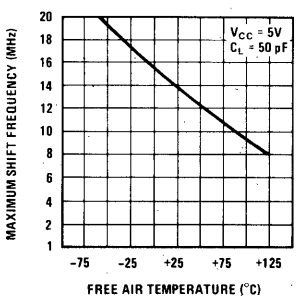
Logical "0" Hold Time vs Free Air Temperature



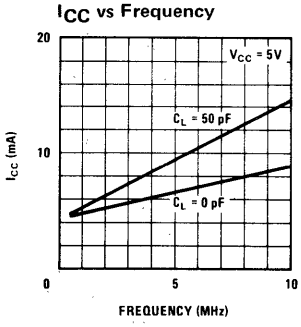
Logical "1" Hold Time vs Free Air Temperature



Shift Frequency



I_{CC} vs Frequency

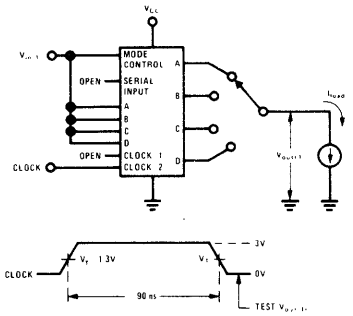


switching characteristics (DM54L95/DM74L95) (Note 1)

SYMBOL	PARAMETER	CONDITIONS	TEST FIGURE	MIN	TYP	MAX	UNITS
f_{MAX}	Maximum Shift Frequency	V_{CC} = 5.0V C_L = 50 pF	54	6.0	14		MHz
$t_{p(CLOCK)}$	Clock Pulse Width	V_{CC} = 5.0V C_L = 50 pF	54	90	44		ns
$t_{pd(1)}$	Propagation Delay to a Logical "1" A, B, C, or D	V_{CC} = 5.0V C_L = 50 pF	54	20	42	90	ns
$t_{pd(0)}$	Propagation Delay to a Logical "0" A, B, C, or D	V_{CC} = 5.0V C_L = 50 pF	54	20	48	90	ns
	Mode Control Logical "0" Setup Time With Respect to CP1 (t_1)	V_{CC} = 5.0V C_L = 50 pF	55	120	70		ns
	Mode Control Logical "1" Setup Time With Respect to CP2 (t_2)	V_{CC} = 5.0V C_L = 50 pF	56	120	45		ns
	Mode Control Logical "0" Setup Time With Respect to CP2 (t_3)	V_{CC} = 5.0V C_L = 50 pF	56	0	-43		ns
	Mode Control Logical "1" Setup Time With Respect to CP1 (t_4)	V_{CC} = 5.0V C_L = 50 pF	55	0	-50		ns
	Logical "1" Setup Time at (t_5) Serial, A, B, C, or D Inputs	V_{CC} = 5.0V C_L = 50 pF	54	90	20		ns
	Logical "0" Setup Time at (t_6) Serial, A, B, C, or D Inputs	V_{CC} = 5.0V C_L = 50 pF	54	90	13		ns
	Logical "1" Hold Time at (t_7) Serial, A, B, C, or D Inputs	V_{CC} = 5.0V C_L = 50 pF	54	0	-14		ns
	Logical "0" Hold Time at (t_8) Serial, A, B, C, or D Inputs	V_{CC} = 5.0V C_L = 50 pF	54	0	-20		ns

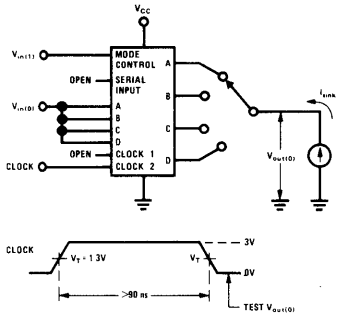
Note 1: Switching parameter limits, switching parameter typicals, and electrical parameter typicals are given for V_{CC} = 5V at T_A = 25°C only.

dc test circuits (DM54L95/DM74L95)



Note: Each output is tested separately.

Figure 46



Note: Each output is tested separately.

Figure 47

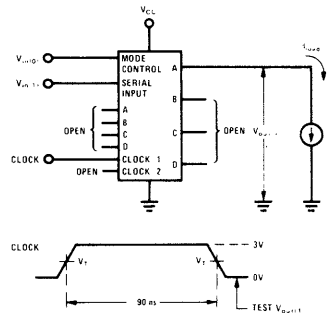


Figure 48

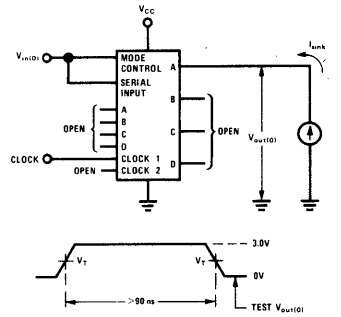
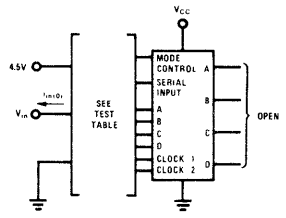


Figure 49

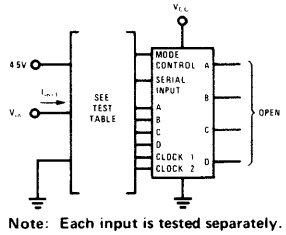


Note: Each input is tested separately.

TEST TABLE

TEST	APPLY 4.5V	APPLY GND
MODE CONTROL	CLOCK 2	NONE
SERIAL INPUT	NONE	MODE CONTROL
A INPUT	MODE CONTROL	NONE
B INPUT	MODE CONTROL	NONE
C INPUT	MODE CONTROL	NONE
D INPUT	MODE CONTROL	NONE
CLOCK 1	NONE	MODE CONTROL
CLOCK 2	MODE CONTROL	NONE

Figure 50



Note: Each input is tested separately.

TEST TABLE

TEST	APPLY 4.5V	APPLY GND
MODE CONTROL	NONE	CLOCK 2
SERIAL INPUT	MODE CONTROL	NONE
A INPUT	NONE	MODE CONTROL
B INPUT	NONE	MODE CONTROL
C INPUT	NONE	MODE CONTROL
D INPUT	NONE	MODE CONTROL
CLOCK 1	MODE CONTROL	NONE
CLOCK 2	NONE	MODE CONTROL

Figure 51

dc test circuits (cont.) (DM54L95/DM74L95)

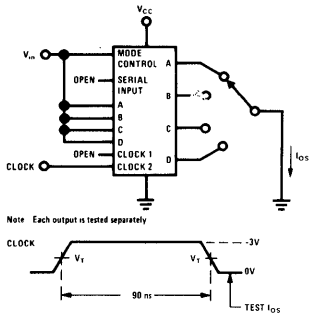


Figure 52

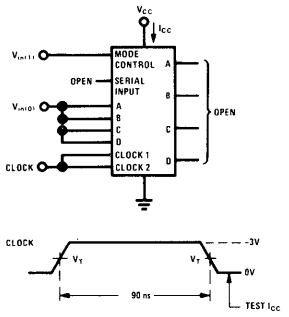
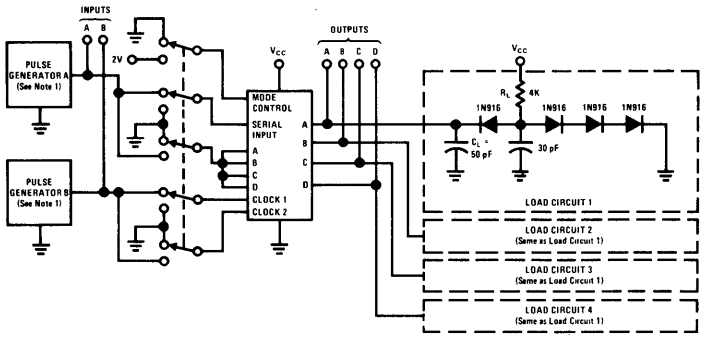
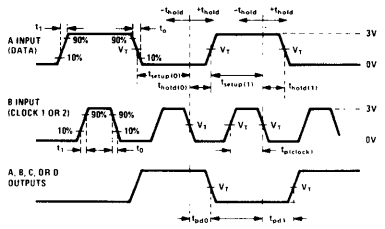


Figure 53

ac test circuits and waveforms (DM54L95/DM74L95)



Notes: 1. The pulse generators have the following characteristics: t_1 = 10 ns to 12 ns, t_0 = 10 ns to 12 ns, and $Z_{out} \approx 50\Omega$. For pulse generator A: t_p > 150 ns and PRR = 500 kHz. For pulse generator B: t_p > 10 ns and PRR = 1 MHz. When testing f_{max}, vary PRR.
2. Voltage values are with respect to network ground terminal.
3. C_L includes probe and jig capacitance.



T_A	V_T
125°C	0.9V
70°C	1.1V
25°C	1.3V
0°C	1.4V
-55°C	1.6V

Figure 54

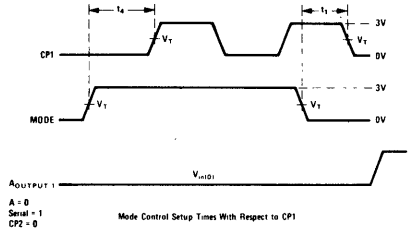


Figure 55

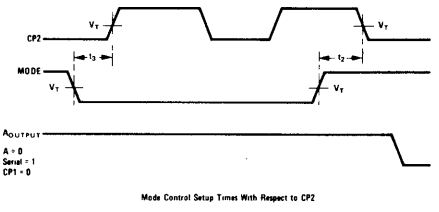
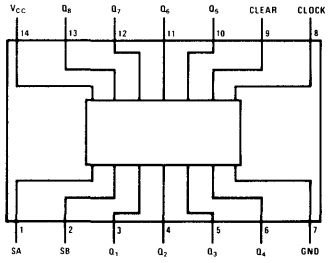


Figure 56

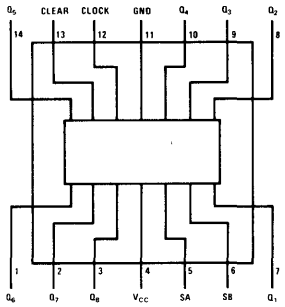
(DM76L70/DM86L70) SHIFT REGISTERS

dual-in-line package connection diagram



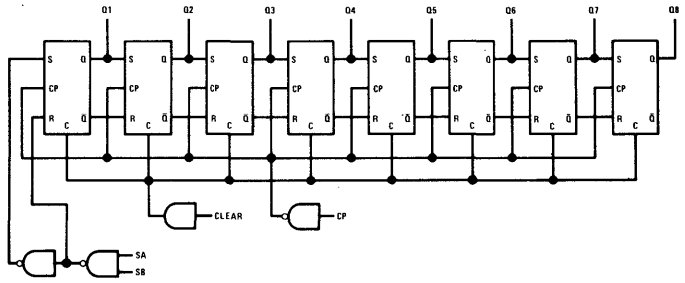
DM76L70/DM86L70

flat package connection diagram



DM76L70/DM86L70

logic diagram



DM76L70/DM86L70

electrical characteristics (DM76L70/DM86L70) (Note 1)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$V_{IN(1)}$	Logical "1" Input Voltage	V_{CC} = MIN	2.0	1.3		V
$V_{IN(0)}$	Logical "0" Input Voltage	V_{CC} = MAX		1.3	0.7	V
$V_{OUT(1)}$	Logical "1" Output Voltage	V_{CC} = MIN, I_{OUT} = −200 μA	2.4	2.8		V
$V_{OUT(0)}$	Logical "0" Output Voltage	V_{CC} = MIN, I_{OUT} = 2 mA			0.3	V
$V_{OUT(0)}$	Logical "0" Output Voltage (Series 74L Only)	V_{CC} = MIN, I_{OUT} = 3.2 mA			0.4	V
$I_{IN(1)}$	Logical "1" Input Current (Except Clear Input)	V_{CC} = MAX, V_{IN} = 2.4V		<1	10	μA
$I_{IN(1)}$	Logical "1" Input Current (Clear Input)	V_{CC} = MAX, V_{IN} = 2.4V		<2	20	μA
$I_{IN(1)}$	Logical "1" Input Current (Except Clear Input)	V_{CC} = MAX, V_{IN} = 5.5V			100	μA
$I_{IN(1)}$	Logical "1" Input Current (Clear Input)	V_{CC} = MAX, V_{IN} = 5.5V			200	μA
$I_{IN(1)}$	Logical "0" Input Current (Except Clear Input)	V_{CC} = MAX, V_{IN} = 0.3V		−120	−180	μA
$I_{IN(0)}$	Logical "0" Input Current (Clear Input)	V_{CC} = MAX, V_{IN} = 0.3V		−240	−360	μA
I_{OS}	Output Short Circuit Current (Note 2)	V_{CC} = MAX, V_{OUT} = 0V	−3	−9	−15	mA
I_{CC}	Power Supply Current	V_{CC} = MAX		6	9	mA

Note 1: Unless otherwise specified, limits shown apply from −55°C to +125°C for the DM76L70 and 0°C to +70°C for the DM86L70. All typicals at T_A = 25°C and V_{CC} = 5V.

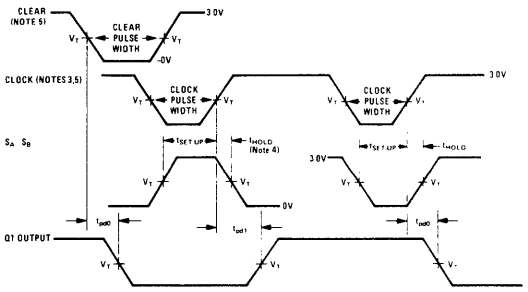
Note 2: Only one output should be shorted at a time.

switching characteristics (DM76L70/DM86L70)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
f_{MIN}	Minimum Clock Frequency	V_{CC} = 5.0V, 50% Duty Cycle	6	12		MHz
t_{pd0}	Propagation Delay to a Logical "0" From Clock to Output	V_{CC} = 5.0V, C_L = 50 pF		100		ns
t_{pd1}	Propagation Delay to a Logical "1" From Clock to Output	V_{CC} = 5.0V, C_L = 50 pF		60		ns
t_{pd0}	Propagation Delay to a Logical "0" From Clear to Output	V_{CC} = 5.0V, C_L = 50 pF		70		ns
$t_{PW(CLOCK)}$	Minimum Clock Pulse Width	V_{CC} = 5.0V, C_L = 50 pF		15		ns
$t_{PW(CLEAR)}$	Minimum Clear Pulse Width	V_{CC} = 5.0V, C_L = 50 pF		75		ns
t_{SET-UP}	Minimum Time That $S_A \cdot S_B$ Data Must be Set-up Prior to Clock Pulse, t_{set-up}	V_{CC} = 5.0V, C_L = 50 pF		25		ns
t_{HOLD}	Minimum Time That $S_A \cdot S_B$ Data Must be Held After Clock Pulse, t_{hold}	V_{CC} = 5.0V, C_L = 50 pF				ns
t_{CR}	Clear Recovery Time*	V_{CC} = 5.0V, T_A = 25°C, C_L = 50 pF		80		ns

*Time required after removal of clear signal for clocking to occur.

switching waveforms (DM76L70/DM86L70)



T_A	V_T
125 °C	0.9V
70 °C	1.1V
25 °C	1.3V
0 °C	1.4V
−55 °C	1.6V

Notes: 3. Clock may be at either a Logical "1" or a Logical "0" while clearing.
4. Negative hold time values indicate $S_A \cdot S_B$ information may be released prior to the time the clock pulse reaches its 1.3V level.
5. Clear and Clock Waveforms: $t_r = t_f$ = 15 ns (10%–90%, 90%–10% transtion); f = 1 MHz.

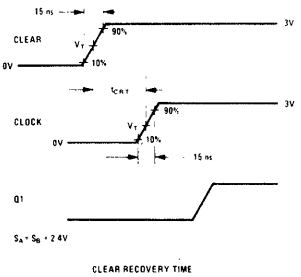


Figure 57

LOW POWER/883

scope

This specification covers the detailed screening and testing procedures for National Semiconductor's standard low power TTL devices produced under our 883 program. Low power 883 devices are those types submitted to and passing the special visual, process-conditioning, testing and screening requirements as specified herein and in Mil-Std-883 "Test Methods and Procedures for Microelectronics."

In addition to the devices specified, National will screen any of its low power TTL devices to any level of Mil-Std-883 upon customer request.

100% screening procedure (level B)

STEP	SCREEN	METHOD
1	Internal Visual	2010.1, condition B
2	Stabilization Bake	1008, condition C min, 200°C, 24 hours min
3	Temperature cycle	1010, condition C min T_A = -65°C to +200°C 15 minutes, each extreme 5 minutes, max transfer time
4	Centrifuge	2001, condition E 30,000 G's min, in Y_1 axis
5	Fine Leak Test (Helium)	1014, condition A 5×10^{-7} cc/sec
6	Gross Leak Test (Bubble)	1014, condition C omit vacuum portion of step 2
7	Burn-In	1005, condition B steady state (See appropriate burn-in figure.) T_A = 125°C T = 168 hours
8	Screen – Group A	Per dc electrical tables for standard series 54L
9	External Visual	2009 3X - 20X
10	Pack	Standard unless otherwise specified
11	Ship	Screening and group A data

pre and post burn-in critical electrical parameters

TABLE I

PARAMETER	CONDITIONS	LIMITS MIN	LIMITS MAX	UNITS
Logical "1" Input Current	Conditions and Limits per dc Electrical Tables for standard Series 54L devices			
Logical "0" Input Current				
Logical "1" Output Leakage Current				
Logical "1" Output Voltage				
Logical "0" Output Voltage				
Logical "1" Supply Current (each gate)				
Logical "0" Supply Current (each gate)				
Power Supply Current (F.F. or MSI)				

qualification procedures

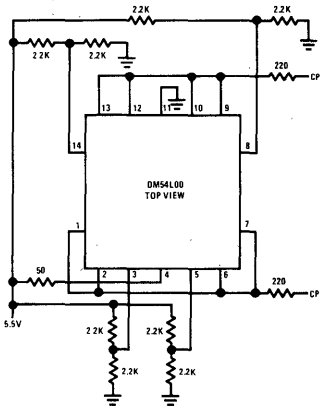
TABLE II – GROUP B ENVIRONMENTAL TESTS

TEST	METHOD	CONDITIONS	NATIONAL LTPD (LEVEL A)
Subgroup 1			
Physical dimensions	2008	Test condition A, visual 10X - 20X	10
Subgroup 2			
Marking permanency	2008	Test condition B, visual 10X - 20X	4 devices (no failures)
Visual and mechanical	2008	Marking 4X	1 device (no failures)
Bond strength	2011	Test condition D	5
Ultrasonic or wedge			
Subgroup 3			
Solderability	2003	Soldering temperature of 260°C - 10°C	10
Subgroup 4			
Lead fatigue	2004	Test condition B_2, weight = 3oz. Three 0° -90° -0° bends	10
Hermeticity	1014		10
Fine		Test condition A, 5×10^{-7} atmosphere cc/sec	
Gross		Test condition C, omit vacuum portion of step 2	
Subgroup 5			
Operating life testing	1005	Test condition B, 1000 hours min +125°C	Not required
Critical electrical parameters		Per table I	

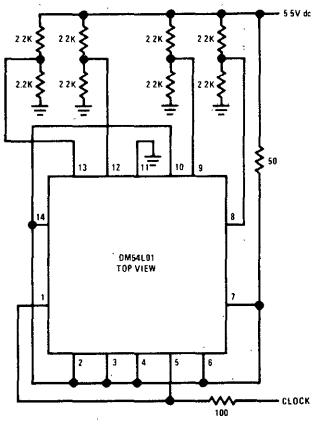
TABLE III – GROUP C ENVIRONMENTAL TESTS

TEST	METHOD	CONDITIONS	NATIONAL LTPD (LEVEL A)
Subgroup 1			
Thermal shock	1011	Test condition B	10
Temperature cycling	1010	Test condition C	
Moisture resistance	1004	Omit initial conditioning and step 7B	
Critical electrical parameters		Per table I	
Subgroup 2			
Mechanical shock	2002	Test condition B, 5 shock pulses at 1500 G's for a duration between 0.1 and 1.0 μs in orientation $X_1, X_2, Y_1, Y_2, Z_1, Z_2$	10
Vibration, variable frequency	2007	Test condition A, 20 G's frequency varied between 20 and 2000 cycles 4 times in orientation X, Y, Z	
Constant acceleration	2001	Test condition E, one minute in each of the orientations, $X_1, X_2, Y_1, Y_2, Z_1, Z_2$ at 30,000 G's	
Critical electrical parameters		Per table I	
Subgroup 3			
Salt atmosphere	1009	Test condition A	10
Subgroup 4			
High temperature storage	1008	$150\ ^{+50}_{-25}$ °C storage, 1000 hours min	7
Critical electrical parameters		Per table I	
Subgroup 5			
Operating life testing	1005	Test condition B, 1000 hours min +125°C	5
Critical electrical parameters		Per table I	

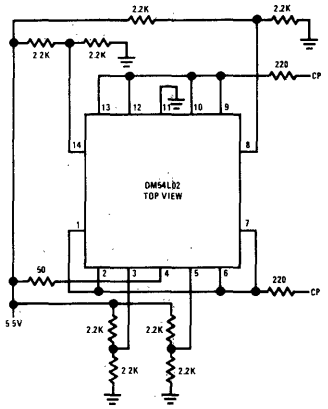
burn-in circuits



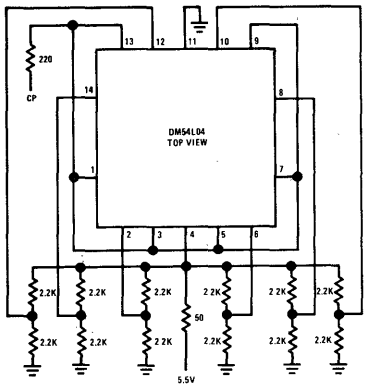
DM54L00/883



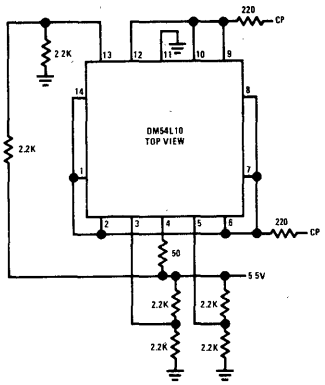
DM54L01/883



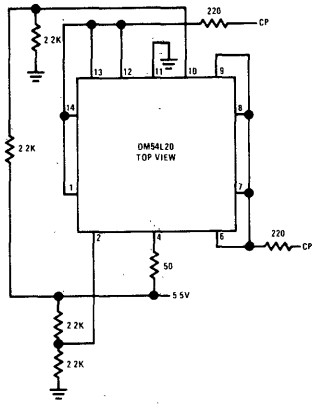
DM54L02/883



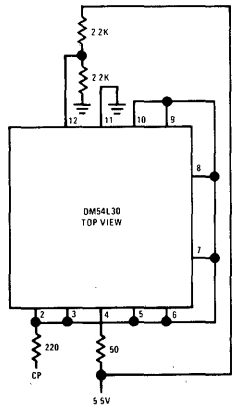
DM54L04/883



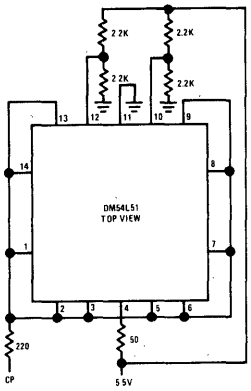
DM54L10/883



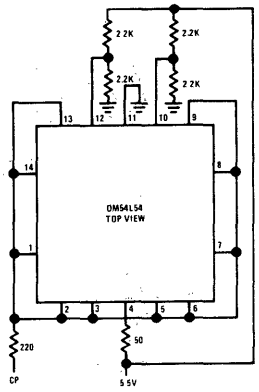
DM54L20/883



DM54L30/883



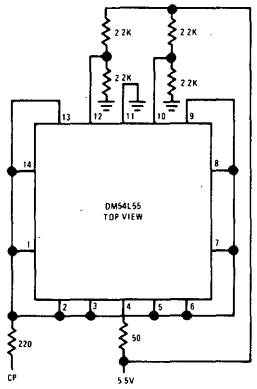
DM54L51/883



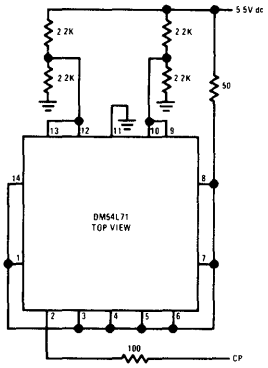
DM54L54/883

Note: All resistors ±5%, 1/4 watt unless otherwise designated, 125°C operating life circuit.

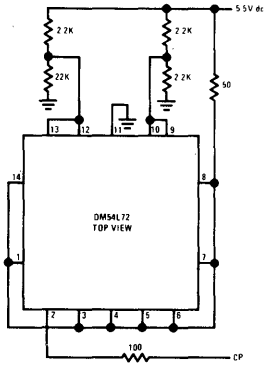
burn-in circuits (cont.)



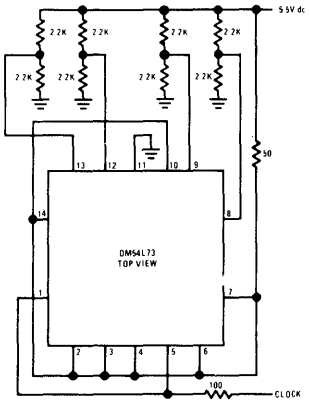
DM54L55/883



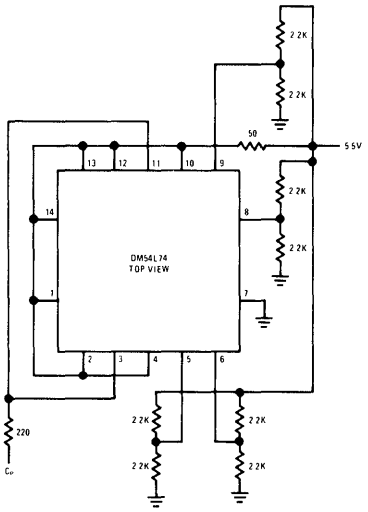
DM54L71/883



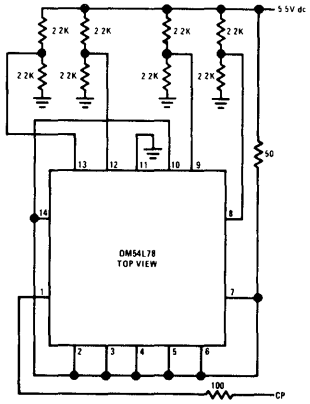
DM54L72/883



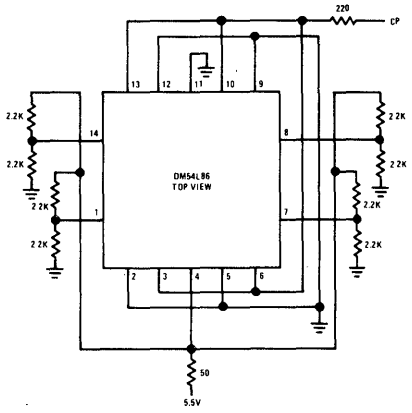
DM54L73/883



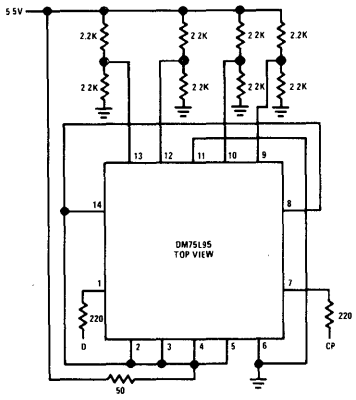
DM54L74/883



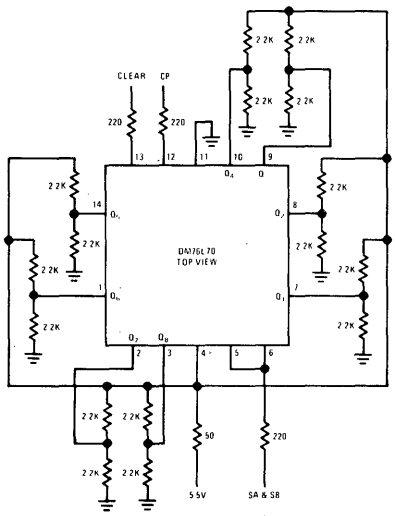
DM54L78/883



DM54L86/883



DM54L95/883



DM76L70/883

Note: All resistors ±5%, 1/4 watt unless otherwise designated, 125°C operating life circuit.

general

Lot Definition: An inspection lot is a collection of devices submitted at one time for inspection to determine compliance with the acceptance criteria of this document. Each inspection lot shall consist of devices of structurally similar device types. Inspection lot identification shall be maintained from the time the lot is assembled to the time it is accepted or given a final rejection.

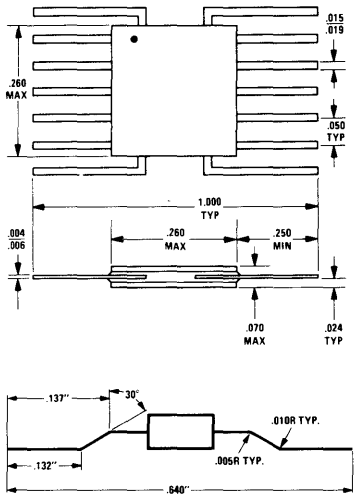
Traceability: All devices are assigned lot code identification that provides traceability back to the wafer lot.

Marking: All devices will be marked NS DM54LXX/883 (54LXX denoting product type number), 4 digit date code indicating week and year.

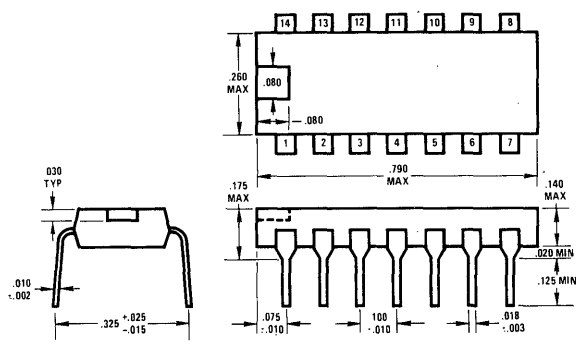
Data Requirements: Attributes summary will be supplied on Burn-In and Group A. Variables Data on qualification will be provided upon request.

Aged Devices: Devices that have been held for more than six months will be rescreened to Group A requirements prior to being shipped.

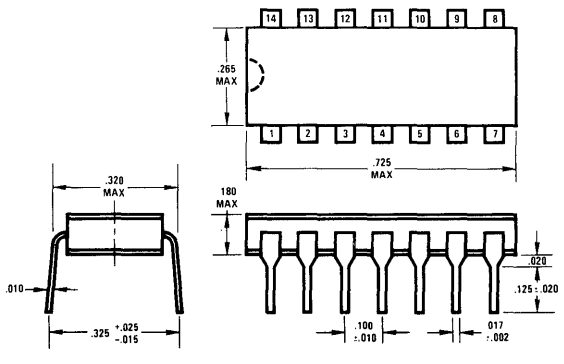
physical dimensions



Flat Package
(Both 883 and Standard Devices)



Molded Dual-In-Line Package
(Standard Devices Only)



Cavity Dual-In-Line Package
(Standard Devices Only)

standard ordering information

ORDER NUMBER	PACKAGE	TEMPERATURE RANGE
DM54LXXF or DM76L70F	Flat Package (F)	−55°C to +125°C
DM74LXXF or DM86L70F	Flat Package (F)	0°to +70°C
DM54LXXN or DM76L70N	Molded DIP (N)	−55°C to +125°C
DM74LXXN or DM86L70N	Molded DIP (N)	0° to+70°C
DM54LXXD or DM76L70D	Cavity DIP (D)	−55°C to +125°C

XX denotes the last two digits of the standard part number.

883 ordering information

ORDER NUMBER	FORMED LEADS	BOTTOM INSULATOR	TEMPERATURE RANGE
DM54LXXF-00/883	No	No	−55°C to +125°C
DM54LXXF-07/883	Yes	No	−55°C to +125°C
DM54LXXF-06/883	No	Yes	−55°C to +125°C
DM54LXXF-01/883	Yes	Yes	−55°C to +125°C

XX denotes the last two digits of the standard part number.

DTL Series 930

DTL series 930 integrated circuits

general description

The National Semiconductor family of DTL (Diode-Transistor-Logic) is a complete line of compatible monolithic integrated circuits designed to operate at medium speed with medium power dissipation and high fan-out. The DTL family is available in 14-pin, silicone, dual-in-line packages for operation over the 0°C to 75°C temperature range.

The DTL line is composed of a variety of NAND gates that allow complete design flexibility. The gates are available with either 6K pull-up resistors for low power dissipation, or 2K pull-up resistors for increased speed. The gate outputs can be wired together to achieve the wired-OR function.

The NAND gates are complemented with the DM932 and DM957 buffers which provide higher fan-out; the DM944 and DM958 power gates which have an open collector, and the DM933 extender which allows increased fan-in for both buffers and the DM930 and DM961 gates.

The binaries in this family are of the direct coupled master-slave type with direct clear and direct set lines. The dual flip flops include ones with either common or separate clocks.

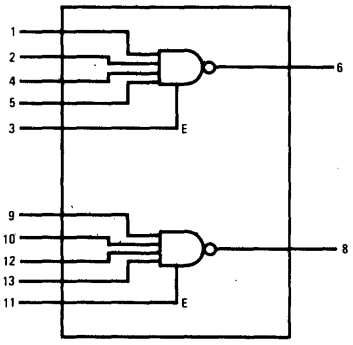
The DM930 series is directly compatible with the TTL devices manufactured by National and can be used in conjunction with them in those portions of a system where speed is not the main consideration.

table of contents

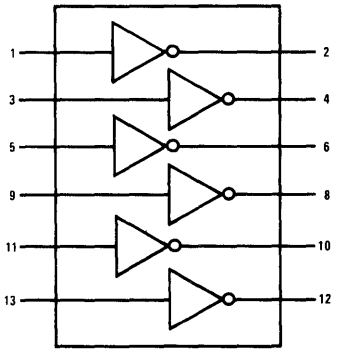
absolute maximum ratings

Power Supply Voltage	
Continuous	8.0V
Pulsed < 1 sec.	12.0V
Input Forward Current	10 mA
Input Reverse Current	1.0 mA
Output Current	
Gates and Binaries	30 mA
Buffers	100 mA
Storage Temperature	−65°C to 150°C
Operating Temperature	0°C to 75°C

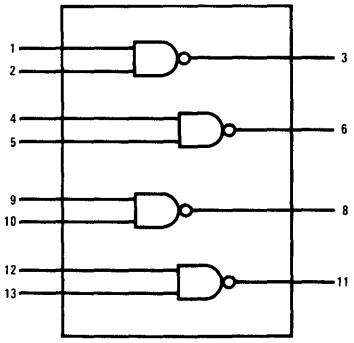
connection/logic diagrams



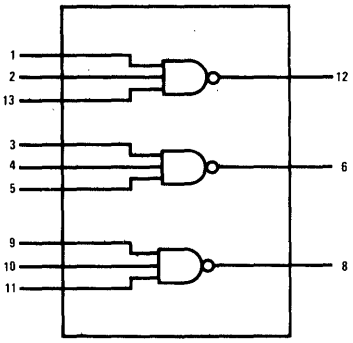
DM930/DM961
DM932/DM944



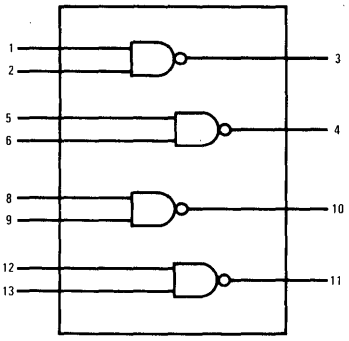
DM935/DM936/DM937



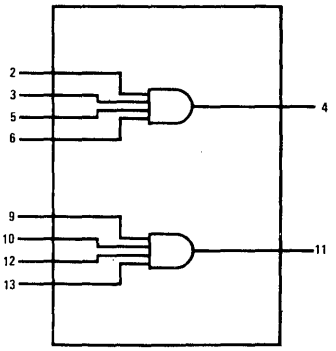
DM946/DM949



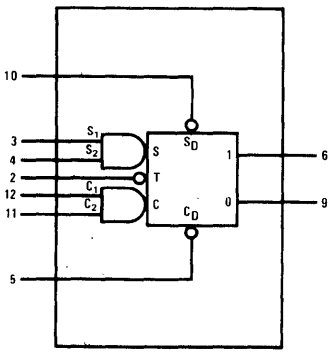
DM962/DM963



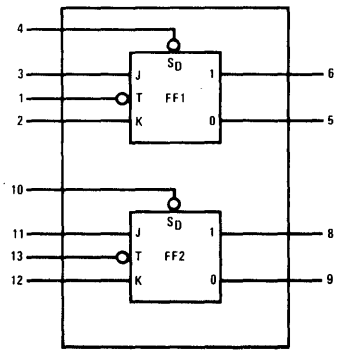
DM957/DM958



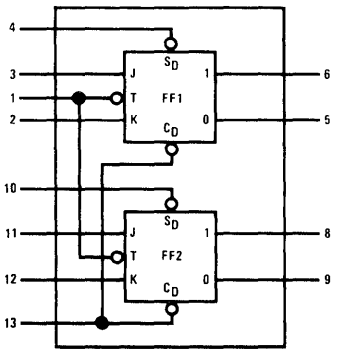
DM933



DM945/DM948



DM9093/DM9094



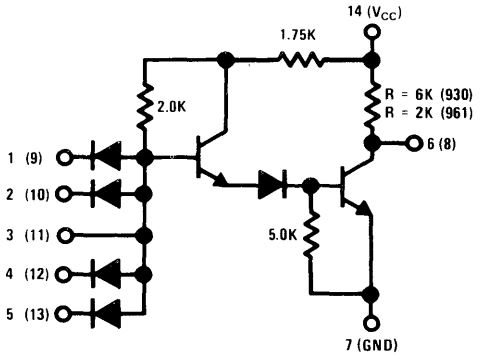
DM9097/DM9099

NAND gates

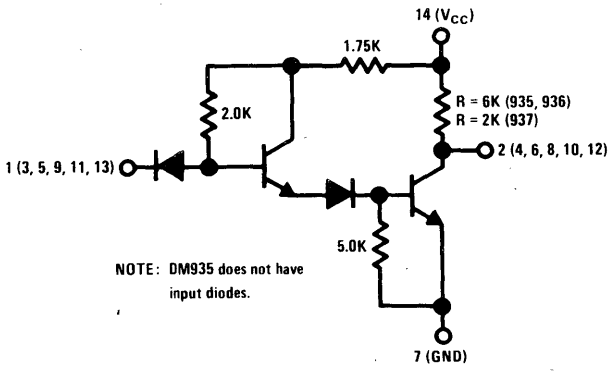
The DM930, DM936, DM946 and DM962 are a variety of NAND gates with a 6K pull-up resistor. The DM961, DM937, DM949 and DM963 are the 2K pull-up versions of the respective gates. The DM935 is a hex inverter similar to the DM936 with the exception that it has no input diodes.

The DM1800 and DM1801 dual 5-input NAND gates are new DTL gates completely compatible with DM930 series gates. See New Products section, page 1.

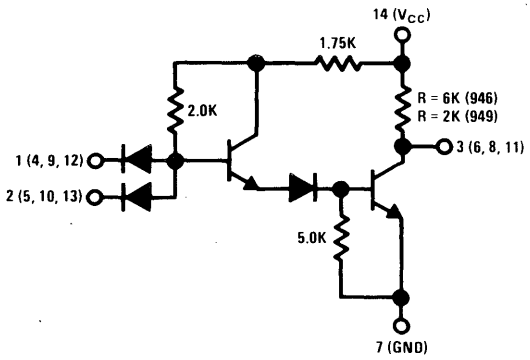
schematic diagrams*



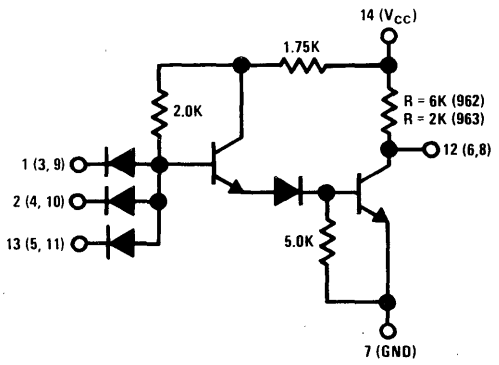
DM930/DM961



DM935/DM936/DM937



DM946/DM949



DM962/DM963

*Only one circuit element is shown. Pin connections are given in parentheses for other circuit elements.

electrical characteristics

Pin 14 (V_{CC}) = 5.0 volts, Pin 7 = GND, unspecified pins open unless otherwise stated.

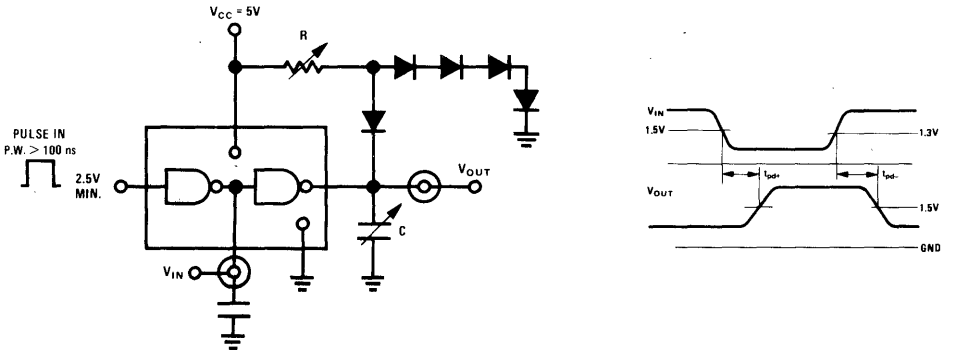
SYMBOL	PARAMETER	PART	CONDITIONS			LIMITS						UNITS
			INPUTS		OUTPUTS	0°C		25°C		75°C		
			INPUT UNDER TEST	OTHER		MIN	MAX	MIN	MAX	MIN	MAX	
V_{OL}	Output Low Voltage	All gates	V_{IH}	V_{IH}	I_{OL}	–	0.45	–	0.45	–	0.50	V
V_{OH}	Output High Voltage	All gates* except 935	V_{IL}	V_R	I_{OH}	2.6	–	2.6	–	2.5	–	V
I_R	Input Reverse Current	All except 935	V_R	GND	–	–	5	–	5	–	10	μA
I_F	Input Forward Current	All except 935	V_F	V_R	–	–	−1.40	–	−1.40	–	−1.33	mA
I_{IN}	Input Current	935*	V_F	–	–	–	−1.40	–	−1.40	–	−1.33	mA
I_{CEX}	Output Leakage Current	6k gates	GND	–	V_{CEX}	–	–	–	100	–	–	μA
		2k gates	GND	–	V_{CEX}	–	–	–	100	–	–	μA
I_{SC}	Output Short Circuit Current	6k gates	GND	–	GND	–	1.30	−0.61	−1.30	–	−1.25	mA
		2k gates	GND	–	GND	–	–	−1.85	−3.90	–	–	mA
I_{PD}	Power Supply Current per gate	6k gates				–	–	–	4	–	–	mA
		2k gates				–	–	–	5.9	–	–	mA
I_{MAX}	Max. Supply Current per gate (V_{CC} = 8V)	All	–	–	–	–	–	–	4	–	–	mA
t_{pd-}	Turn-On Delay	6k gates		R = 400Ω, C = 50 pF		–	–	10	30	–	–	ns
		2k gates		R = 400Ω, C = 50 pF		–	–	10	30	–	–	ns
t_{pd+}	Turn-On Delay	6k gates		R = 3.9kΩ, C = 30 pF		–	–	25	80	–	–	ns
		2k gates		R = 3.9kΩ, C = 30 pF		–	–	15	60	–	–	ns

*Use an FD600 diode or equivalent on input under test

test conditions

TEMP.	V_{IH} VOLTS	V_{IL} VOLTS	V_R VOLTS	V_F VOLTS	V_{CEX} VOLTS	(6k) I_{OL} mA	(6k) I_{OH} mA	(2k) I_{OL} mA	(2k) I_{OH} mA
0°C	2.0	1.2	4.0	0.45	–	12.0	−0.12	11.0	−0.5
+25°C	1.9	1.1	4.0	0.45	5.0	12.0	−0.12	11.0	−0.5
+75°C	1.8	0.95	4.0	0.50	–	11.4	−0.12	10.4	−0.5

switching time test circuit and waveform

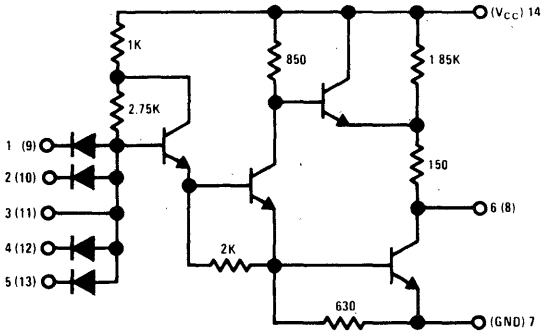


buffers and extender

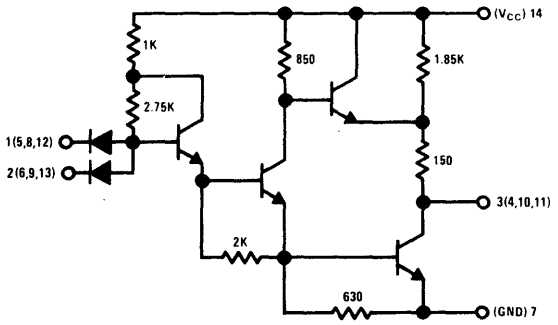
The DM932, DM944, DM957, and DM958 are power gates which are capable of sinking high currents.

The DM933 is an extender element which consists of two four input diode nodes and can be used to extend the fan-in of the DM930, DM961, DM932, and DM944.

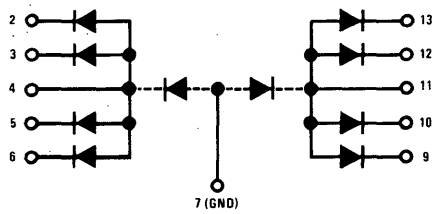
schematic diagrams*



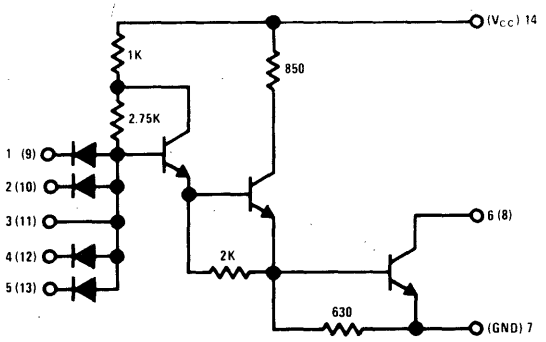
DM932



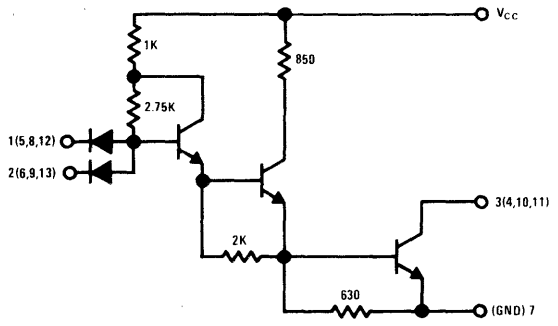
DM957



DM933



DM944



DM958

*Only one circuit element is shown. Pin connections are given in parentheses for other circuit elements.

electrical characteristics

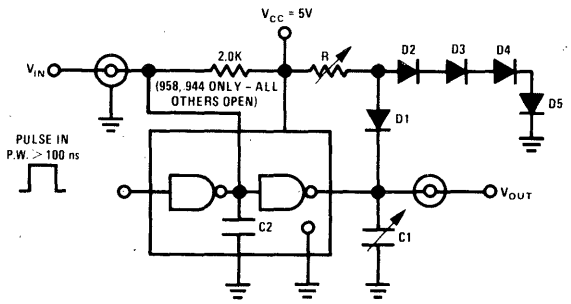
Pin 14 (V_{CC}) = 5.0 volts, Pin 7 = GND, unspecified pins open unless otherwise stated.

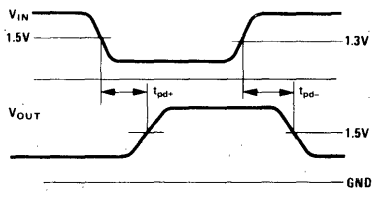
SYMBOL	PARAMETER	PART	CONDITIONS			LIMITS						UNITS
			INPUTS		OUTPUTS	0°C		25°C		75°C		
			INPUT UNDER TEST	OTHER		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
V_{OL}	Output Low Voltage	932,944 957,958	V_{IH}	V_{IH}	I_{OL}	–	0 45	–	0.45	–	0.50	V
V_{OH}	Output High Voltage	932,957	V_{IL}	V_R	I_{OH}	2.6	–	2.6	–	2.5	–	V
I_R	Input Reverse Current	932,944 957,958	V_R	GND	–	–	5	–	5	–	10	μA
I_R	Input Reverse Current	933	V_R	GND	GND	–	5	–	5	–	10	μA
I_F	Input Forward Current	932,944 957,958	V_F	V_R	–	–	-1.40	–	-1.40	–	-1.33	mA
V_{FD}	Input Forward Voltage	933	I_{FD}	GND	GND	0.75	0.90	0.68	0.82	0.60	0.75	V
I_{SC}	Output Short Cir. Cur	932,957	GND	–	GND	-16	–	-16	–	-14	–	mA
I_{CEX}	Output Leakage Current	932,957	GND	–	V_{CEX}	–	–	–	100	–	–	μA
		944,958	GND	–	V_{CEX}	–	25	–	100	–	200	μA
I_{PD}	Power Drain Current	932	–	–	–	–	–	–	30 0	–	–	mA
		957	–	–	–	–	–	–	60.0	–	–	mA
		944	–	–	–	–	–	–	22.5	–	–	mA
		958	–	–	–	–	–	–	45	–	–	mA
I_{MAX}	Max. Supply Current per gate (V_{CC} = 8V)	932,944 957,958	–	–	–		–	–	4	–	–	mA
t_{pd-}	Turn-on delay	932 957	R = 150Ω, C = 500 pF			–	–	15	40	–	–	ns
		944 958	R = 150Ω, C = 100 pF		–	–	–	10	35	–	–	ns
t_{pd+}	Turn-off delay	932 957	R = 510Ω, C = 500 pF		–	–	–	25	80	–	–	ns
		944 958	R = 510Ω, C = 20 pF		–	–	–	15	50	–	–	ns

test conditions

TEMP.	V_{IH} VOLTS	V_{IL} VOLTS	V_R VOLTS	V_F VOLTS	I_{FD} mA	V_{CEX} VOLTS	957 932 I_{OL} mA	958 944 I_{OL} mA	957 932 I_{OH} mA
0°C	2.0	1.2	4.0	0 45	-2	–	36	40	-2.0
+25°C	1.9	1 1	4.0	0.45	-2	5.0	36	40	-2 5
+75°C	1.8	0.95	4 0	0.50	-2	–	34	36	-3.0

switching time test circuit and waveforms





NOTE: When testing 958 or 944 short diode D1, remove diodes D2, D3, D4 and D5 and add capacitor C2 = 20 pF as shown.

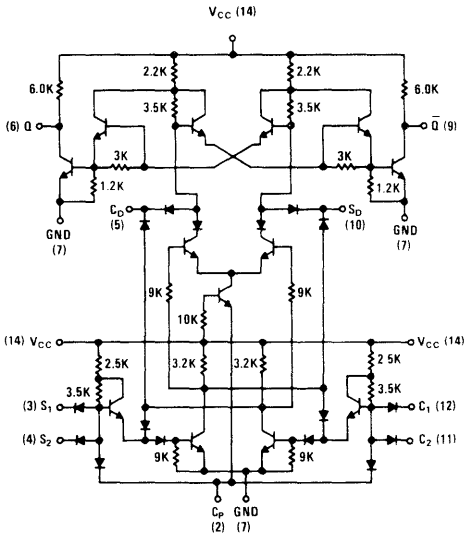
binaries

The DM945 and DM948 are R–S flip flops which can be externally cross coupled to perform in the JK mode. They are of the master slave type with output buffers to provide isolation from the output load. These flip flops feature both asynchronous set and clear lines. The DM945 has a 6K pull-up resistor and the DM948 has a 2K pull-up resistor.

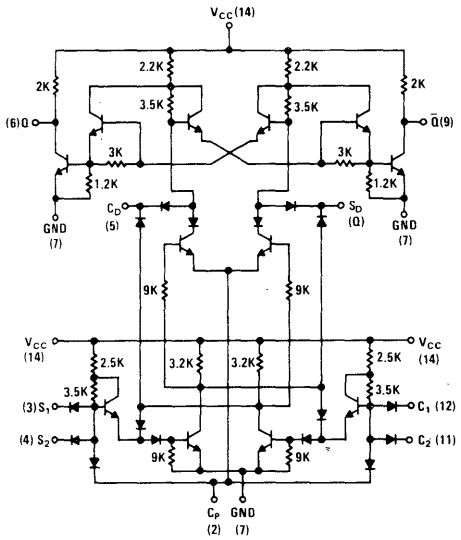
The DM9093 and DM9094 are dual JK flip flops of the DM945 and DM948 variety respectively. Both flip flops have separate clocks and no asynchronous clear lines.

The DM9097 and DM9099 are dual JK flip flops of the DM948 and DM945 variety respectively. Both flip flops have common clocks and both asynchronous set and clear lines.

schematic diagrams



DM945



DM948

truth tables

SYNCHRONOUS TRUTH TABLE

t_n				$t_n + 1$
S_1 Pin 3	S_2 Pin 4	C_1 Pin 12	C_2 Pin 11	Q Pin 6
0	X	0	X	Qn
0	X	X	0	Qn
X	0	0	X	Qn
X	0	X	0	Qn
0	X	1	1	0
X	0	1	1	0
1	1	0	X	1
1	1	X	0	1
1	1	1	1	U

0 – Low State (more negative)
1 – High State (more positive)
U – Indeterminate State
X – State of the input does not affect the state of the circuit

ASYNCHRONOUS TRUTH TABLE

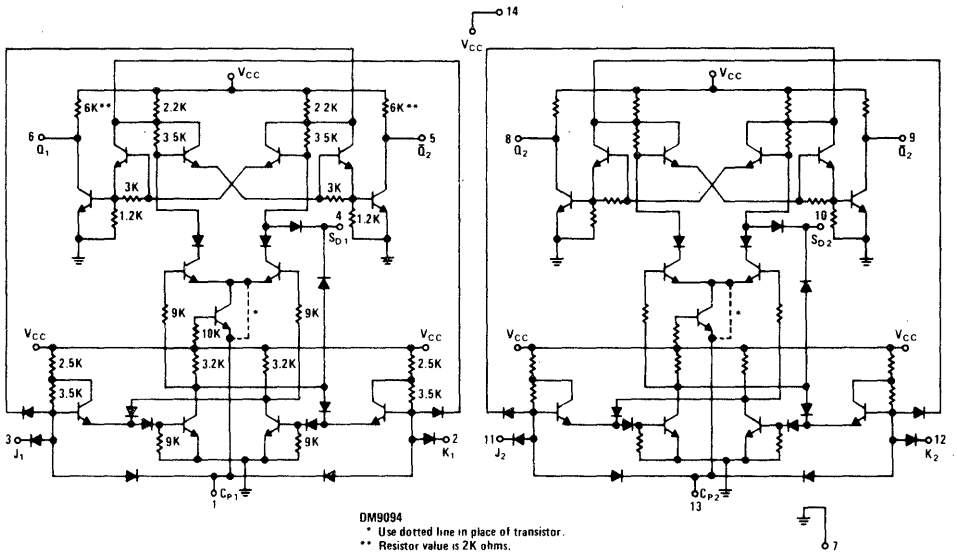
S_D Pin 10	C_D Pin 5	Q Pin 6	$\bar{Q}$ Pin 9
1	1	NC	NC
0	1	1	0
1	0	0	1
0	0	1	1

J–K TRUTH TABLE

t_n		$t_n + 1$
S_1 Pin 3	C_1 Pin 12	Q Pin 6
0	0	QN
1	0	1
0	1	0
1	1	$\bar{Q}$N

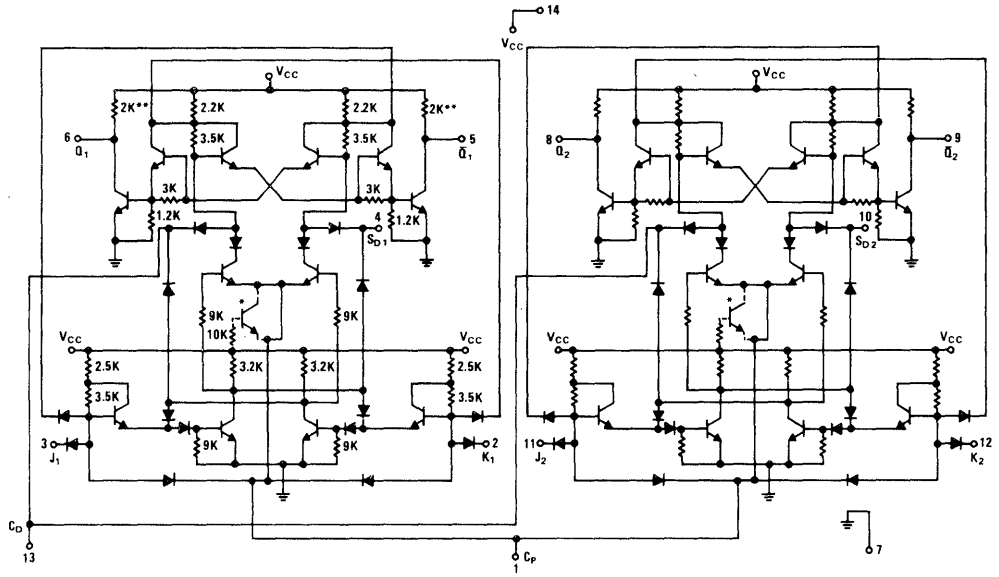
(Connect S_2 to $\bar{Q}$, C_2 to Q) Asynchronous inputs, direct set (S_D) and direct clear (C_D), override the synchronous inputs, they are independent of all other inputs.

schematic diagrams



DM9094
* Use dotted line in place of transistor.
** Resistor value is 2K ohms.

DM9093/DM9094 (DM9093 shown)



DM9099
* Use dotted line including resistor and transistor in place of direct Cp input.
** Resistor value is 6K ohms.

DM9097/DM9099 (DM9097 shown)

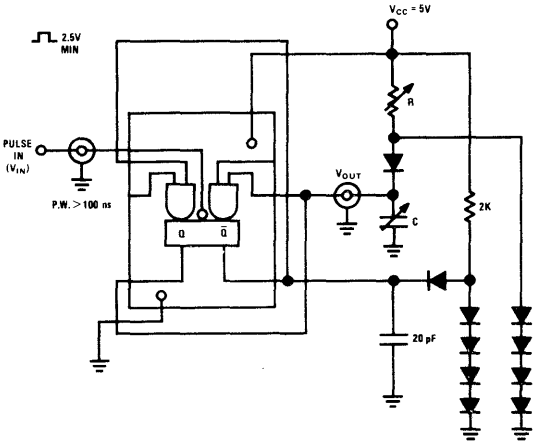
truth table

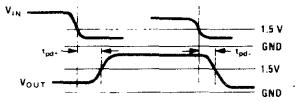
J–K TRUTH TABLE

t_n		$t_n + 1$
S_1 Pin 3	C_1 Pin 12	Q Pin 6
0	0	QN
1	0	1
0	1	0
1	1	$\overline{QN}$

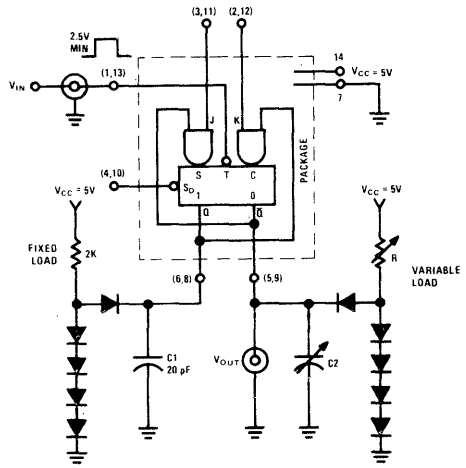
Direct set (S_D) and direct clear (C_D), override the synchronous inputs, they are independent of all other inputs

switching time test circuits and waveforms

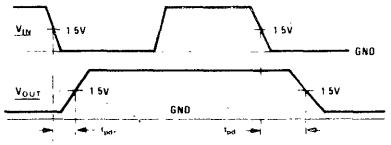




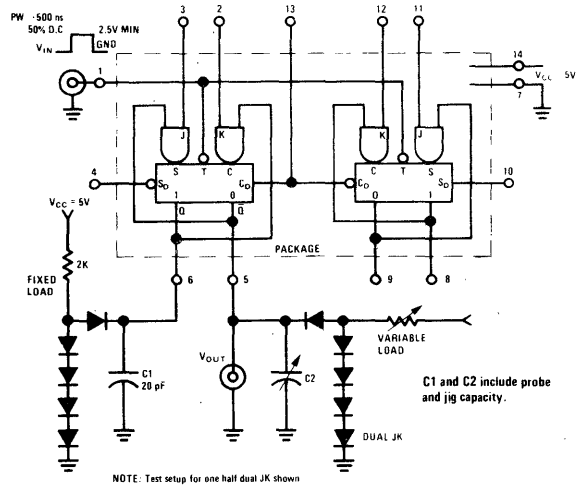
DM945/DM948



C1 and C2 include probe and jig capacity.
All diodes are FD600 or equivalent at +25 C.

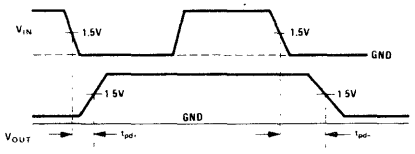


DM9093/DM9094 (one-half circuit shown)



C1 and C2 include probe and jig capacity.

NOTE: Test setup for one half dual JK shown



DM9097/DM9099

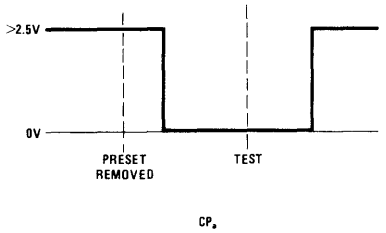
electrical characteristics (DM945/DM948)

Pin 14 (V_{CC}) = 5.0 volts, Pin 7 = GND, unspecified pins open unless otherwise stated.

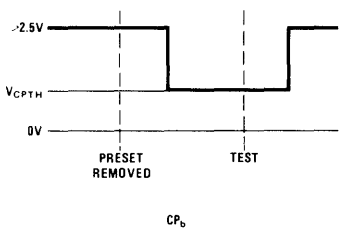
SYMBOL	PARAMETER	PART	CONDITIONS								LIMITS						UNITS	COMMENTS
			C_p	S_1	S_2	C_D	Q	S_D	C_2	C_1	0°C		25°C		75°C			
											MIN	MAX.	MIN	MAX.	MIN	MAX.		
V_{OL}	Output Low Voltage	Both	CP_b	GND	–	–	$\overline{Q}$	–	X	–	–	0.45	–	0.45	–	0.50	V	X=Momentary Gnd
V_{OH}	Output High Voltage (Data Inputs)	945	CP_a	V_{IH}	V_{IL}	X	I_{OH}	–	–	V_{IL}	2.6	–	2.6	–	2.5	–	V	X=Momentary Gnd
		948	CP_a	V_{IH}	V_{IL}	–	I_{OH}	–	–	V_{IL}	2.6	–	2.6	–	2.5	–	V	
V_{OH}	Output High Voltage (Set Reset Inputs)	Both	CP_a	GND	GND	V_{CC}	I_{OH}	V_{IL}	–	–	2.6	–	2.6	–	2.6	–	V	
I_{RD}	Input Reverse Current (Data Inputs)	Both	GND	V_R	–	–	–	–	–	–	–	5.0	–	5.0	–	10.0	μA	
I_R	Input Reverse Current (Set Reset Inputs)	Both	CP_a	GND	GND	V_R	–	V_{CC}	–	–	–	5.0	–	5.0	–	10.0	μA	
I_{RC}	Input Reverse Current (Clock Input)	Both	V_R	GND	GND	GND	–	–	–	–	–	30	–	30	–	40	μA	V_{AC} = 4.0 volts
I_{FD}	Input Forward Current (Data Inputs)	Both	V_R	V_F	V_R	–	–	–	–	–	–	–0.95	–	–0.95	–	–0.90	mA	
I_F	Input Forward Current (Set Reset Inputs)	Both	–	–	–	V_F	–	–	GND	GND	–	–2.8	–	–2.8	–	–2.67	mA	
I_{FC}	Input Forward Current (Clock Input)	945	V_F	–	–	V_{IL}	–	–	–	–	–	–2.8	–	–2.8	–	–2.66	mA	
		948	V_F	–	–	V_{IL}	–	–	–	–	–	–2.8	–	–2.8	–	–2.67	mA	
I_{CEX}	Output Leakage Current	Both	–	–	–	–	V_{CEX}	GND	–	–		–	–	100	–	–	μA	
I_{SC}	Short Circuit Current	945	V_{CC}	–	–	GND	GND	GND	–	–	–0.59	–1.41	–0.59	–1.41	–0.55	–1.38	mA	
		948	V_{CC}	–	–	GND	GND	GND	–	–	–1.77	–4.2	–1.77	–4.2	–1.60	–4.0	mA	
I_{PD}	Power Drain Current	945	V_{CC}	–	–	–	–	–	–	–	–	–	–	14	–	–	mA	
		948	V_{CC}	–	–	–	–	–	–	–	–	–	–	17	–	–	mA	
I_{MAX}	Max. Supply Current (V_{CC} = 8V)	945	–	GND	GND	GND	–	GND	GND	GND	–	–	–	18	–	–	mA	
		948	–	GND	GND	GND	–	GND	GND	GND	–	–	–	23	–	–	mA	
t_{pd-}	Turn–On Delay	945	R = 330Ω, C = 50 pF								–	–	15	55	–	–	ns	
		948	R = 330Ω, C = 50 pF								–	–	15	55	–	–	ns	
t_{pd+}	Turn–Off Delay	945	R = 2.0kΩ, C = 30 pF								–	–	25	100	–	–	ns	
		948	R = 2.0kΩ, C = 30 pF								–	–	25	75	–	–	ns	

test conditions

TEMP.	V_{IH} VOLTS	V_{IL} VOLTS	V_F VOLTS	V_R VOLTS	945(6K) V_{CPTH} VOLTS	948(2K) V_{CPTH} VOLTS	945(6K) I_{OL} mA	948(2K) I_{OL} mA	945(6K) I_{OH} mA	948(2K) I_{OH} mA	V_{CEX} VOLTS
0° C	2.0	1.2	0.45	4.0	1.15	1.30	16.8	15.4	–0.12	–0.5	–
+25° C	1.9	1.1	0.45	4.0	0.95	1.15	16.8	15.4	–0.12	–0.5	5.0
+75° C	1.8	0.95	0.50	4.0	0.65	0.85	16.0	14.6	–0.12	–0.5	–



CP_a



CP_b

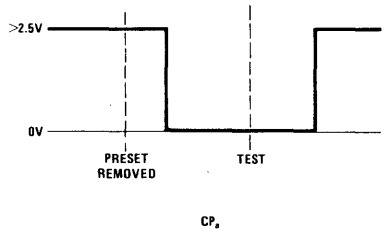
electrical characteristics (DM9093/DM9094/DM9097/DM9099)

Pin 14 (V_{CC}) = 5.0 volts, Pin 7 = GND, unspecified pins open unless otherwise stated.

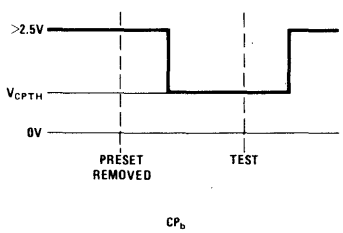
SYMBOL	PARAMETER	PART	CONDITIONS	LIMITS						UNITS
				0° C		+25° C		−75° C		
				MIN	MAX	MIN	MAX	MIN	MAX	
V_{OL}	Output Low Voltage	All	I_{OL} on output under test	–	0.45	–	0.45	–	0.50	V
V_{OH}	Output High Voltage	All	I_{OH} on output under test	2.6	–	2.6	–	2.5	–	V
I_{SC}	Output Short Circuit Current	2k	GND output under test	-1.77	-4.2	-1.77	-4.2	-1.60	-4.0	mA
		6k	GND output under test	-0.59	-1.41	-0.59	-1.41	-0.55	-1.38	mA
I_{FD}	Input Forward Current (Data Input)	All	V_F on input under test V_R on other inputs	–	−0.95	–	−0.95	–	−0.90	mA
I_{FC}	Input Forward Current (Clock and Direct Clear Inputs	9097 9099	V_F on input under test V_R on other inputs	–	−5.6	–	−5.6	–	−5.34	mA
I_{FC}	Input Forward Current (Clock Input)	9093 9094	V_F on input under test V_R on others	–	−2.8	–	−2.8	–	−2.67	mA
I_F	Input Forward Current (Direct Set Inputs)	All	V_F on input under test V_R on other inputs	–	−2.8	–	−2.8	–	−2.67	mA
I_R	Input Reverse Current (All except clock inputs and Direct clear input on 9097, 9099)	All	V_R on input under test GND on other inputs	–	5.0	–	5.0	–	10.0	μA
I_R	Input Reverse Current Direct (Clear Input)	9097 & 9099	V_R on input under test GND on other inputs	–	10	–	10	–	20	μA
I_R	Input Reverse Current (Clock Inputs)	9093 & 9094	V_R on input under test GND on other inputs	–	20	–	20	–	30	μA
		9097 & 9099	V_R on input under test GND on other inputs	–	40	–	40	–	60	μA
I_{PD}	Power Drain Current	9093	Inputs Open	–	–	–	28	–	–	mA
		9094	Inputs Open		–	–	34	–	–	mA
		9099	Inputs Open		–	–	28	–	–	mA
		9097	Inputs Open		–	–	34	–	–	mA
I_{MAX}	Max. Supply Current (V_{CC} = 8V)	9093 9099	GND all inputs	–	–	–	36	–	–	mA
		9094 9097		–	–	–	45	–	–	mA
t_{pd-}	Turn–On Delay	All	R = 330Ω, C = 50 pF	–	–	15	55	–	–	ns
t_{pd+}	Turn–Off Delay	6k	R = 2k, C = 30 pF	–	–	25	100	–	–	ns
		2k	R = 2k, C = 30 pF	–	–	25	75	–	–	ns

test conditions

TEMP.	(6k) I_{OL} mA	(2k) I_{OL} mA	(6k) I_{OH} mA	(2k) I_{OH} mA	V_F VOLTS	V_R VOLTS	V_{IH} VOLTS	V_{IL} VOLTS	9093-9 6K V_{CPTH}	9094-7 2K V_{CPTH}
0° C	16.8	15.4	−0.12	−0.5	0.45	4.0	2.0	1.2	1.15	1.30
+25° C	16.8	15.4	−0.12	−0.5	0.45	4.0	1.9	1.1	0.95	1.15
+75° C	16.0	14.6	−0.12	−0.5	0.50	4.0	1.8	0.95	0.65	0.85



CP_a



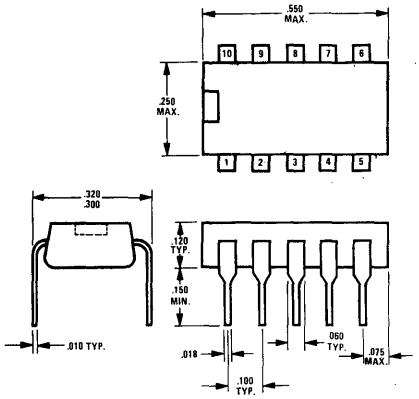
CP_b

Ordering Information/ Physical Dimensions

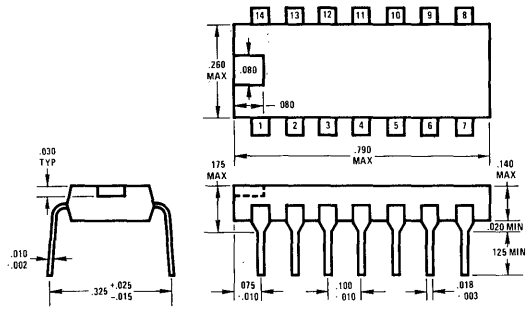
ORDERING INFORMATION

When ordering, indicate the appropriate part number followed by the package designation, e.g., DM7400N.

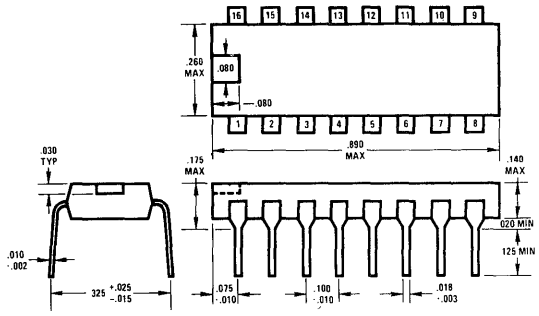
PACKAGE DESIGNATION	PACKAGE TYPE
N	Molded Dual-In-Line Package
D	Cavity Dual-In-Line Package
F	Flat Package
H	Metal Can Package



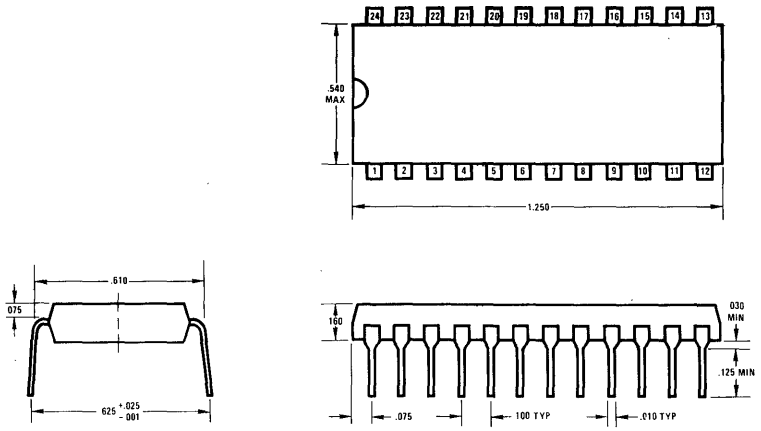
10 Pin Molded Dual-In-Line Package
(Hybrids Only)



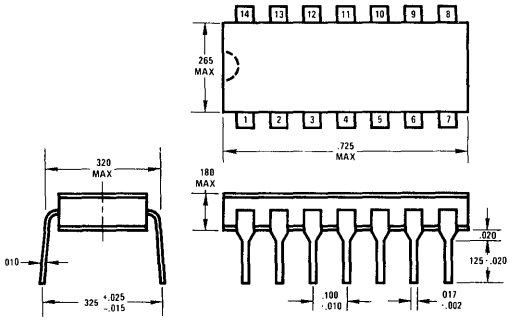
14 Pin Molded Dual-In-Line Package



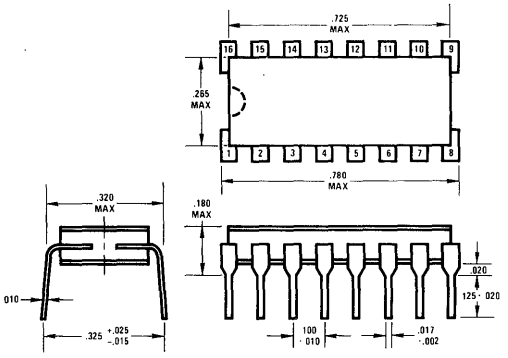
16 Pin Molded Dual-In-Line Package



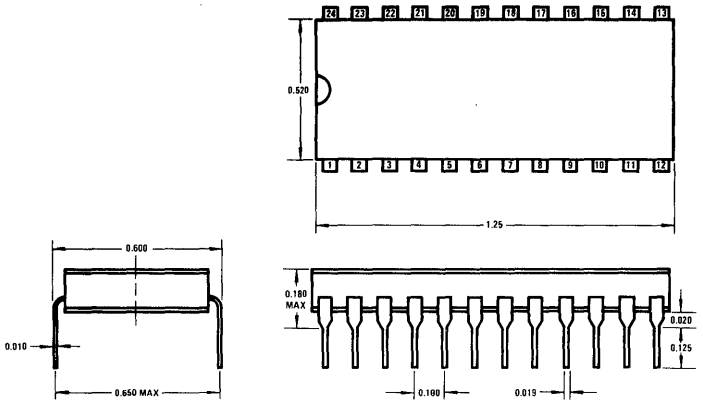
24 Pin Molded Dual-In-Line Package



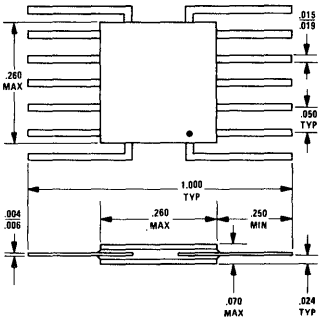
14 Pin Cavity Dual-In-Line Package



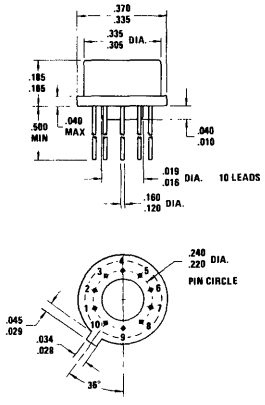
16 Pin Cavity Dual-In-Line Package



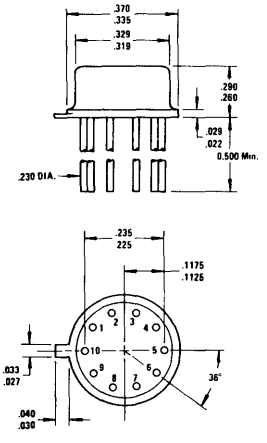
24 Pin Cavity Dual-In-Line Package



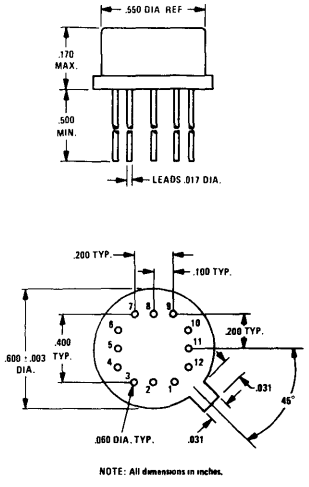
14 Pin Flat Package



10 Lead Metal Can Package



10 Lead Metal Can Package
(Hybrids Only)



NOTE: All dimensions in inches.

12 Lead Metal Can Package
(Hybrids Only)

Available Digital Applications Literature

The following is a listing of Digital applications literature. This literature, plus information on National's other product lines, is available through our sales offices, representatives, distributors, or our headquarters in Santa Clara.

application notes

AN-12 Applications of the DM7200/DM8200 digital comparator

AN-17 Programmable divider applications

AN-22 Integrated circuits for digital data transmissions

AN-35 High speed TTL adders

AN-36 TTL MSI applications

AN-37 TTL MSI multiplexers and demultiplexers

AN-43 TRI-STATE logic in modular systems

TTL-5 TRI-STATE logic

digital briefs

DB-2 Exclusive-OR code converters

DB-3 Grounded-load drivers

brochures

Transfer Mold Encapsulation Reliability Report

Digital Integrated Circuits Reliability Report

guides

TTL Guide

TTL Cross Reference Guide

DTL Cross Reference Guide

TTL/DTL Current Drivers Guide

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