Determining the Speed of the Dynamic RAM Needed When Interfacing the DP8419-80 to Most Major Microprocessors

National Semiconductor
Application Note 411
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April 1986

INTRODUCTION

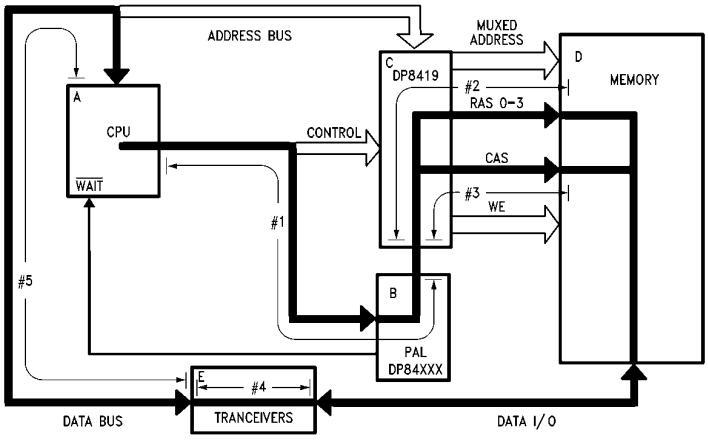
This application note looks at the individual delay elements of a CPU to memory access path for a typical memory system utilizing the DP8419-80 DRAM controller. In the final analysis the reader should be equipped with all the necessary equations to easily calculate the slowest/cheapest allowable DRAMS for no wait state CPU operation when using the DP8419-80 in his/her system.

Equations for calculating the maximum allowable DRAM "tRAC" ($\overline{RAS}$ access time) and "tCAC" ($\overline{CAS}$ access time) specifications for a particular microprocessor to operate at its maximum clock frequency without wait states are provided. Table I and *Figure 3* at the end of this application note give potential DP8419-80 users an illustration of what speed DRAM they may typically need to use in order to achieve no wait state operation with a particular microprocessor. It is important to note that even better performance can be achieved by using the faster DP8419-70.

THE 5 FUNCTIONAL BLOCKS

**Figure 1* illustrates the five functional blocks and the five main delay segments of our DP8419-80 based system example. For this particular example, the following functional block descriptions apply:

Functional Block	Functional Block Description
A)	The CPU issues an access request to the PAL then reads or writes data to or from the DRAMs;
B)	The PAL provides the refresh access arbitration logic which holds off a CPU access during a DRAM refresh and DRAM refresh during a CPU access. The PAL also provides the $\overline{RASIN}$ signal to the DP8419-80;
C)	The DP8419-80 generates the control signal timing required by the DRAMs. It also automatically multiplexes the row and column addresses during access, provides the refresh address during refresh and provides the on board capacitive drive for the direct interface with the DRAM array;
D)	The DRAM provides or stores data in response to the DP8419-80's control signal; and,
E)	The tranceivers isolate the DRAMs from the data bus when they are not being accessed in addition to passing data between the CPU and memory during read and write cycles.



DP84412: 32008/016/032 - DP8409A/18/19/28/29 Interface PAL
DP84512: NS32332 - DP8417/18/19/28/29 Interface PAL
DP84322/422: 68000/008/010 - DP8409A/18/19/28/29 Interface PALS
DP84522: 68020 - DP8418/19/28/29 Interface PAL
DP84432: 8086/88/186/188 - DP8409A/18/19/28/29 Interface PAL
DP84532: 80286 - DP8418/19/28/29 Interface PALS

FIGURE 1. Delay Elements of the CPU to Memory Data Access Path (DP8409A or DP8417/18/19/28/29 System)

RRD-B30M105/Printed in U. S. A.

Figure 2 may prove to be a helpful reference. It illustrates a hypothetical system timing pattern for memory accessing for a 4T state microprocessor.

DELAY SEGMENTS

Delay segments #1 through #5 are also shown in *Figure 1*. Delay segment #1 represents the timing delay from when the CPU initiates an access to the point where $\overline{\text{RASIN}}$ is issued by the PAL to the DP8419-80;

Delay segment #2 represents the $\overline{\text{RASIN}}$ to $\overline{\text{RAS}}$ out delay of the DP8419-80 DRAM controller;

Delay segment #3 represents the $\overline{\text{RASIN}}$ to $\overline{\text{CAS}}$ out delay of the DP8419-80 DRAM controller;

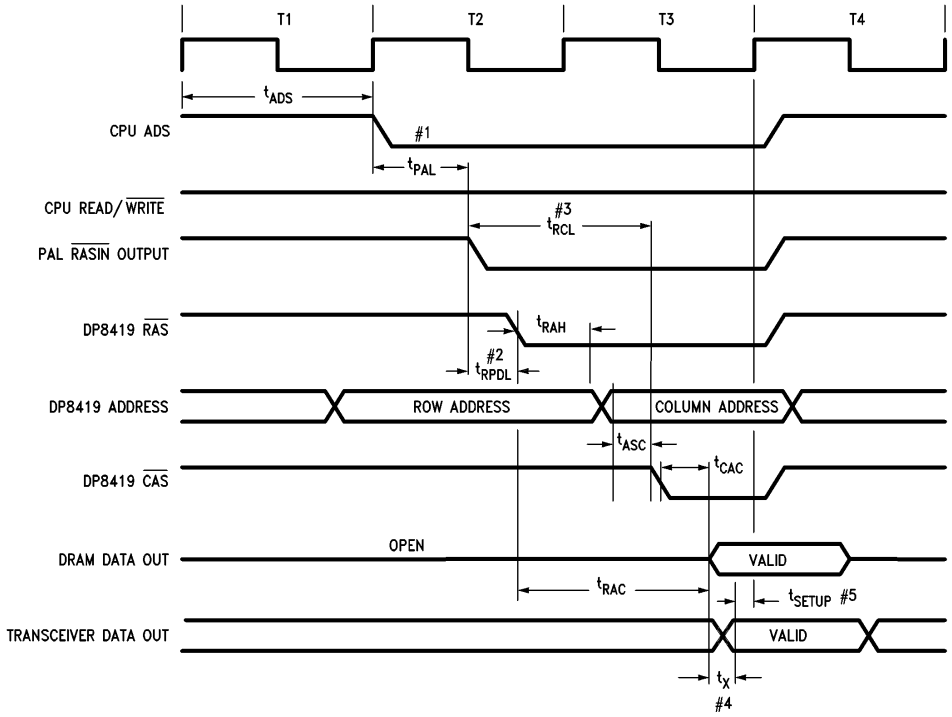
Delay segment #4 represents the inherent delay of the CPU/memory bus transceivers;

Delay segment #5 represents the required CPU data setup time.

The unique equations for determining the values of delay segments #1 through #5 for each of the major microprocessors are provided as the primary content of this application note.

Both ''tRAC'' and ''tCAC'' must be considered in determining what speed DRAM can be used in a particular system design. The DRAM chosen must meet both the ''tRAC'' and ''tCAC'' parameters calculated. If more information is desired on how ''tRAC'' and ''tCAC'' were calculated for a particular microprocessor, the reader should consult the microprocessor data sheet and the PAL data sheet for the particular microprocessor (ie. DP84412 Series 32000 processors, DP84422 68000 family processors. DP84522 68020 family processors, DP84432 iAPX88/86/188/186 processor, DP84532 iAPX286).

Most of the calculations contained in this application note use ''RAHS'' = 1 (15 ns guaranteed minimum row address hold time). Calculations only used ''RAHS'' = 0 (25 ns guaranteed minimum row address hold time) when the calculated access time from $\overline{\text{RAS}}$ equaled or exceeded 200 ns. This is because DRAMs can be found with $\overline{\text{RAS}}$ access times up to 150 ns that require only 15 ns row address hold times.



TL/F/8595–2

FIGURE 2. System Access Timing (4T State Microprocessor Example)

tRAC/tCAC CALCULATIONS FOR THE MAJOR MICROPROCESSORS

I) Series 32000 "tRAC" and "tCAC" Calculations

Series 32000 8 MHz No Wait State Calculations

#1) $\overline{\text{RASIN}}$ low = T1 − 2 ns (FCLK − PHI1 skew) + 12 ns ("B" PAL clocked output) = 125 − 2 + 12 = 135 ns maximum

#2) $\overline{\text{RASIN}}$ to $\overline{\text{RAS}}$ low = 20 ns maximum

#3) $\overline{\text{RASIN}}$ to $\overline{\text{CAS}}$ low = 80 ns (DP8419-80 $\overline{\text{RASIN}}$ − $\overline{\text{CAS}}$ low) − 3 ns (load of 72 DRAMs instead of 88 DRAMs speced in data sheet) = 77 ns

#4) 74F245 transceiver delay = 7 ns maximum

#5) CPU data setup time to "T4" = 20 ns minimum

"tRAC" = T1 + T2 + T3 − #1 − #2 − #4 − #5
= 25 + 125 + 125 − 135 − 20 − 7 − 20
= 193 ns

"tCAC" = T1 + T2 + T3 − #1 − #3 − #4 − #5
= 125 + 125 + 125 − 135 − 77 − 7 − 20
= 136 ns

Therefore the DRAM chosen should have a "tRAC" less than or equal to 193 ns and a "tCAC" less than or equal to 136 ns. Standard 150 ns DRAMs meet this criteria.

Series 32000 10 MHz No Wait State Calculations

#1) $\overline{\text{RASIN}}$ low = T1 − 2 ns (FCLK − PHI1 skew) + 12 ns ("B" PAL clocked (output) = 100 − 2 + 12 = 110 ns maximum

#2) $\overline{\text{RASIN}}$ to $\overline{\text{RAS}}$ low = 20 ns maximum

#3) $\overline{\text{RASIN}}$ to $\overline{\text{CAS}}$ low = 80 ns (DP8419 $\overline{\text{RASIN}}$ − $\overline{\text{CAS}}$ low) − 3 ns (load of 72 DRAMs instead of 88 DRAMs speced in data sheet) = 77 ns

#4) 74F245 transceiver delay = 7 ns maximum

#5) CPU data setup time to "T4" = 15 ns minimum

"tRAC" = T1 + T2 + T3 − #1 − #2 − #4 − #5
= 100 + 100 + 100 − 110 − 20 − 7 − 15
= 148 ns

"tCAC" = T1 + T2 + T3 − #1 − #3 − #4 − #5
= 100 + 100 + 100 − 100 − 77 − 7 − 15
= 91 ns

Therefore the DRAM chosen should have a "tRAC" less than or equal to 148 ns and a "tCAC" less than or equal to 91 ns. Standard 120 ns DRAMs meet this criteria.

II) 68000 Family "tRAC" and "tCAC" Calculations

68000 Family 8 MHz No Wait State Calculations

#1) $\overline{\text{RASIN}}$ low = S0 + S1 + $\overline{\text{AS}}$ low (maximum) + "B" PAL combinational output delay maximum = 125 + 60 + 15 = 200 ns maximum

#2) $\overline{\text{RASIN}}$ to $\overline{\text{RAS}}$ low = 20 ns maximum

#3) $\overline{\text{RASIN}}$ to $\overline{\text{CAS}}$ low = 80 ns (DP8419-80 $\overline{\text{RASIN}}$ − $\overline{\text{CAS}}$ low) − 3 ns (load of 72 DRAMs instead of 88 DRAMS speced in data sheet) = 77 ns

#4) 74F245 transceiver delay = 7 ns maximum

#5) CPU data setup time = 15 ns minimum

"tRAC" = (S0 + S1) + (S2 + S3) + (S4 + S5) + S6 (minimum) − #1 − #2 − #4 − #5
= 125 + 125 + 125 + 55 − 200 − 20 − 7 − 15
= 188 ns

"tCAC" = (S0 + S1) + (S2 + S3) + (S4 + S5) + S6 (minimum) − #1 − #3 − #4 − #5
= 125 + 125 + 125 + 55 − 200 − 77 − 7 − 15
= 131 ns

Therefore the DRAM chosen should have a "tRAC" less than or equal to 188 ns and a "tCAC" less than or equal to 131 ns. Standard 150 ns DRAMs meet this critieria.

68000 Family 9 MHz No Wait State Calculations

#1) $\overline{\text{RASIN}}$ low = S0 + S1 + $\overline{\text{AS}}$ low (maximum) + "B" PAL combinational output delay maximum = 111 + 55 + 15 = 181 ns maximum

#2) $\overline{\text{RASIN}}$ to $\overline{\text{RAS}}$ low = 20 ns maximum

#3) $\overline{\text{RASIN}}$ to $\overline{\text{CAS}}$ low = 80 ns (DP8419-80 $\overline{\text{RASIN}}$ − $\overline{\text{CAS}}$ low) − 3 ns (load of 72 DRAMs instead of 88 DRAMs speced in data sheet) = 77 ns

#4) 74F245 transceiver delay = 7 ns maximum

#5) CPU data setup time = 10 ns minimum

"tRAC" = (S0 + S1) + (S2 + S3) + (S4 + S5) + S6 (minimum) − #1 − #2 − #4 − #5
= 111 + 111 + 111 + 45 − 181 − 20 − 7 − 10
= 160 ns

"tCAC" = (S0 + S1) + (S2 + S3) + (S4 + S5) + S6 (minimum) − #1 − #3 − #4 − #5
= 111 + 111 + 111 + 45 − 181 − 77 − 7 − 10
= 103 ns

Therefore the DRAM chosen should have a "tRAC" less than or equal to 160 ns and a "tCAC" less than or equal to 103 ns. Standard 150 ns DRAMs meet this criteria.

68000 Family 10 MHz No Wait State Calculations

#1) $\overline{\text{RASIN}}$ low = S0 + S1 + $\overline{\text{AS}}$ low (maximum) + "B" PAL combinational output delay = 100 + 55 + 15 = 170 ns maximum

#2) $\overline{\text{RASIN}}$ to $\overline{\text{RAS}}$ low = 20 ns maximum

#3) $\overline{\text{RASIN}}$ to $\overline{\text{CAS}}$ low = 80 ns (DP8419-80 $\overline{\text{RASIN}}$ − $\overline{\text{CAS}}$ low) − 3 ns (load of 72 DRAMs instead of 88 DRAMs speced in data sheet) = 77 ns

#4) 74F245 transceiver delay = 7 ns maximum

#5) CPU data setup time = 10 ns minimum

"tRAC" = (S0 + S1) + (S2 + S3) + (S4 + S5) + S6 (minimum) − #1 − #2 − #4 − #5

= 100 + 100 + 100 + 45 − 170 − 20 − 7 − 10

= 138 ns

"tCAC" = (S0 + S1) + (S2 + S3) + (S4 + S5) + S6 (minimum) − #1 − #3 − #4 − #5

= 100 + 100 + 100 + 45 − 170 − 77 − 7 − 10

= 81 ns

Therefore the DRAM chosen have a "tRAC" less than or equal to 138 ns and a "tCAC" less than or equal to 81 ns. Standard 120 ns DRAMs meet this criteria.

68000 Family 11 MHz No Wait State Calculations

#1) $\overline{\text{RASIN}}$ low = S0 + S1 + $\overline{\text{AS}}$ low (maximum) + "B" PAL combinational output delay maximum = 91 + 55 + 15 = 161 ns maximum

#2) $\overline{\text{RASIN}}$ to $\overline{\text{RAS}}$ low = 20 ns maximum

#3) $\overline{\text{RASIN}}$ to $\overline{\text{CAS}}$ low = 80 ns (DP8419-80 $\overline{\text{RASIN}}$ − $\overline{\text{CAS}}$ low) − 3 ns (load of 72 DRAMs instead of 88 DRAMs speced in data sheet) = 77 ns

#4) 74F245 transceiver delay = 7 ns maximum

#5) CPU data setup time = 10 ns minimum

"tRAC" = (S0 + S1) + (S2 + S3) + (S4 + S5) + S6 (minimum) − #1 − #2 − #4 − #5

= 91 + 91 + 91 + 35 − 161 − 20 − 7 − 10

= 110 ns

"tCAC" = (S0 + S1) + (S2 + S3) + (S4 + S5) + S6 (minimum) − #1 − #3 − #4 − #5

= 91 + 91 + 91 + 35 − 161 − 77 − 7 − 10

= 53 ns

Therefore the DRAM chosen should have a "tRAC" less than or equal to 110 ns and a "tCAC" less than or equal to 53 ns. Standard 100 ns DRAMs meet this criteria.

68000 Family 12 MHz No Wait State Calculations

#1) $\overline{\text{RASIN}}$ low = S0 + S1 + $\overline{\text{AS}}$ low (maximum) + "B" PAL combinational output delay maximum = 83 + 55 + 15 = 153 ns maximum

#2) $\overline{\text{RASIN}}$ to $\overline{\text{RAS}}$ low = 20 ns maximum

#3) $\overline{\text{RASIN}}$ to $\overline{\text{CAS}}$ low = 80 ns (DP8419-80 $\overline{\text{RASIN}}$ − $\overline{\text{CAS}}$ low) − 3 ns (load of 72 DRAMs instead of 88 DRAMs speced in data sheet) = 77 ns

#4) 74F245 transceiver delay = 7 ns maximum

#5) CPU data setup time = 10 ns minimum

"tRAC" = (S0 + S1) + (S2 + S3) + (S4 + S5) + S6 (minimum) − #1 − #2 − #4 − #5

= 83.3 + 83.3 + 83.3 + 35 − 153 − 20 − 7 − 10 = 95 ns

"tCAC" = (S0 + S1) + (S2 + S3) + (S4 + S5) + S6 (minimum) − #1 − #3 − #4 − #5

= 83.3 + 83.3 + 83.3 + 35 − 153 − 77 − 7 − 10 = 38 ns

Therefore the DRAM chosen should have a "tRAC" less than or equal to 95 ns and a "tCAC" less than or equal to 38 ns.

III) 68020 "TRAC" AND "TCAC" Calculations

68020 6 MHz No Wait State Calculations

#1) $\overline{\text{RASIN}}$ low = S0 + S1 + "B" PAL combinational output delay maximum = 167 + 15 = 182 ns maximum

#2) $\overline{\text{RASIN}}$ to $\overline{\text{RAS}}$ low = 20 ns maximum

#3) $\overline{\text{RASIN}}$ to $\overline{\text{CAS}}$ low = 80 ns (DP8419-80 $\overline{\text{RASIN}}$ − $\overline{\text{CAS}}$ low) − 3 ns (load of 72 DRAMs instead of 88 DRAMS speced in data sheet) = 77 ns

#4) 74F244 transceiver delay = 7 ns maximum

#5) CPU data setup time = 10 ns minimum

"tRAC" = (S0 + S1) + (S2 + S3) + S4 (minimum) − #1 − #2 − #4 − #5

= 167 + 167 + 75 − 182 − 20 − 7 − 10 = 190 ns

"tCAC" = (S0 + S1) + (S2 + S3) + S4 (minimum) − #1 − #3 − #4 − #5

= 167 + 167 + 75 − 182 − 77 − 7 − 10 = 133 ns

Therefore the DRAM chosen should have a "tRAC" less than or equal to 190 ns and a "tCAC" less than or equal to 133 ns. Standard 150 ns DRAMs meet this criteria.

68020 7 MHz No Wait State Calculations

#1) $\overline{\text{RASIN}}$ low = S0 + S1 + "B" PAL combinational output delay maximum = 143 + 15 = 158 ns maximum

#2) $\overline{\text{RASIN}}$ to $\overline{\text{RAS}}$ low = 20 ns maximum

#3) $\overline{\text{RASIN}}$ to $\overline{\text{CAS}}$ low = 80 ns (DP8419-80 $\overline{\text{RASIN}}$ − $\overline{\text{CAS}}$ low) − 3 ns (load of 72 DRAMs instead of 88 DRAMS speced in data sheet) = 77 ns

#4) 74F244 transceiver delay = 7 ns maximum

#5) CPU data setup time = 10 ns minimum

"tRAC" = (S0 + S1) + (S2 + S3) + S4 (minimum) − #1 − #2 − #4 − #5

= 143 + 143 + 60 − 158 − 20 − 7 − 10 = 151 ns

"tCAC" = (S0 + S1) + (S2 + S3) + S4 (minimum) − #1 − #3 − #4 − #5

= 143 + 143 + 60 − 158 − 77 − 7 − 10 = 94 ns

Therefore the DRAM chosen should have a "tRAC" less than or equal to 151 ns and a "tCAC" less than or equal to 94 ns. Standard 150 ns DRAMs meet this criteria.

68020 8 MHz No Wait State Calculations

#1) $\overline{\text{RASIN}}$ low = S0 + S1 + "B" PAL combinational output delay maximum = 125 + 15 = 140 ns maximum

#2) $\overline{\text{RASIN}}$ to $\overline{\text{RAS}}$ low = 20 ns maximum

#3) $\overline{\text{RASIN}}$ to $\overline{\text{CAS}}$ low = 80 ns (DP8419-80 $\overline{\text{RASIN}}$ − $\overline{\text{CAS}}$ low) − 3 ns (load of 72 DRAMs instead of 88 DRAMS speced in data sheet) = 77 ns

#4) 74F244 transceiver delay = 7 ns maximum

#5) CPU data setup time = 10 ns minimum

"tRAC" = (S0 + S1) + (S2 + S3) + S4 (minimum) − #1 − #2 − #4 − #5

= 125 + 125 + 55 − 140 − 20 − 7 − 10 = 128 ns

''tCAC'' = (S0 + S1) + (S2 + S3) + S4 (minimum) − #1 − #3 − #4 − #5

= 125 + 125 + 55 − 140 − 77 − 7 − 10 = 71 ns

Therefore the DRAM chosen should have a ''tRAC'' less than or equal to 128 ns and a ''tCAC'' less than or equal to 71 ns. Standard 120 ns DRAMs meet this criteria.

68020 9 MHz No Wait State Calculations

#1) $\overline{\text{RASIN}}$ low = S0 + S1 + ''B'' PAL combinational output delay maximum = 111 + 15 = 131 ns maximum

#2) $\overline{\text{RASIN}}$ to $\overline{\text{RAS}}$ low = 20 ns maximum

#3) $\overline{\text{RASIN}}$ to CAS low = 80 ns (DP8419-80 $\overline{\text{RASIN}}$ − $\overline{\text{CAS}}$ low) − 3 ns (load of 72 DRAMs instead of 88 DRAMS speced in data sheet) = 77 ns

#4) 74F244 transceiver delay = 7 ns maximum

#5) CPU data setup time = 10 ns minimum

''tRAC'' = (S0 + S1) + (S2 + S3) + S4 (minimum) − #1 − #2 − #4 − #5

= 111 + 111 + 50 − 131 − 20 − 7 − 10

= 104 ns

''tCAC'' = (S0 + S1) + (S2 + S3) + S4 (minimum) − #1 − #3 − #4 − #5

= 111+ 111 + 50 − 131 − 77 − 7 − 10

= 47 ns

Therefore the DRAM chosen should have a ''tRAC'' less than or equal to 104 ns and a ''tCAC'' less than or equal to 47 ns.

IV) 68020 with 1 Wait State Inserted ''tRAC'' and ''tCAC'' Calculations

68020 10 MHz (1 Wait State) Calculations

#1) $\overline{\text{RASIN}}$ low = S0 + S1 + ''B'' PAL combinational output delay maximum = 100 + 15 = 115 ns maximum

#2) $\overline{\text{RASIN}}$ to $\overline{\text{RAS}}$ low = 20 ns maximum

#3) $\overline{\text{RASIN}}$ to CAS low = 80 ns (DP8419-80 $\overline{\text{RASIN}}$ − $\overline{\text{CAS}}$ low) − 3 ns (load of 72 DRAMs instead of 88 DRAMS speced in data sheet) = 77 ns

#4) 74F244 transceiver delay = 7 ns maximum

#5) CPU data setup time = 10 ns minimum

''tRAC'' = (S0 + S1) + (S2 + S3) + (SW + SW) + S4 (minimum) − #1 − #2 − #4 − #5

= 100 + 100 + 100 + 45 − 115 − 20 − 7 − 10

= 193 ns

''tCAC'' = (S0 + S1) + (S2 + S3) + (SW + SW) + S4 (minimum) − #1 − #3 − #4 − #5

= 100 + 100 + 100 + 45 − 115 − 77 − 7 − 10

= 136 ns

Therefore the DRAM chosen should have a ''tRAC'' less than or equal to 193 ns and a ''tCAC'' less than or equal to 136 ns. Standard 150 ns DRAMs meet this criteria.

68020 12 MHz (1 Wait State) Calculations

#1) $\overline{\text{RASIN}}$ low = S0 + S1 + ''B'' PAL combinational output delay maximum = 80 + 15 = 95 ns maximum

#2) $\overline{\text{RASIN}}$ to $\overline{\text{RAS}}$ low = 20 ns maximum

#3) $\overline{\text{RASIN}}$ to $\overline{\text{CAS}}$ low = 80 ns (DP8419-80 $\overline{\text{RASIN}}$ − $\overline{\text{CAS}}$ low) − 3 ns (load of 72 DRAMs instead of 88 DRAMS speced in data sheet) = 77 ns

#4) 74F244 transceiver delay = 7 ns maximum

#5) CPU data setup time = 10 ns minimum

''tRAC'' = (S0 + S1) + (S2 + S3) + (SW + SW) + S4 (minimum) − #1 − #2 − #4 − #5

= 83.3 + 83.3 + 83.3 + 35 − 95 − 20 − 7 − 10

= 153 ns

''tCAC'' = (S0 + S1) + (S2 + S3) + (SW + SW) + S4 (minimum) − #1 − #3 − #4 − #5

= 83.3 + 83.3 + 83.3 + 35 − 95 − 77 − 7 − 10

= 96 ns

Therefore the DRAM chosen should have a ''tRAC'' less than or equal to 153 ns and a ''tCAC'' less than or equal to 96 ns. Standard 150 ns DRAMs meet this criteria.

68020 14 MHz (1 Wait State) Calculations

#1) $\overline{\text{RASIN}}$ low = S0 + S1 + ''B'' PAL combinational output delay maximum = 72 + 15 = 87 ns maximum

#2) $\overline{\text{RASIN}}$ to $\overline{\text{RAS}}$ low = 20 ns maximum

#3) $\overline{\text{RASIN}}$ to $\overline{\text{CAS}}$ low = 80 ns (DP8419-80 $\overline{\text{RASIN}}$ − $\overline{\text{CAS}}$ low) − 3 ns (load of 72 DRAMs instead of 88 DRAMs speced in data sheet) = 77 ns

#4) 74F244 transceiver delay = 7 ns maximum

#5) CPU data setup time = 5 ns minimum

''tRAC'' = (S0 + S1) + (S2 + S3) + (SW + SW) + S4 (minimum) − #1 − #2 − #4 − #5

= 72 + 72 + 72 + 30 − 87 − 20 − 7 − 5

= 127 ns

''tCAC'' = (S0 + S1) + (S2 + S3) + (SW + SW) + S4 (minimum) − #1 − #3 − #4 − #5

= 72 + 72 + 72 + 30 − 87 − 77 − 7 − 5

= 70 ns

Therefore the DRAM chosen should have a ''tRAC'' less than or equal to 127 ns and a ''tCAC'' less than or equal to 70 ns. Standard 120 ns DRAMs meet this criteria.

68020 16 MHz (1 Wait State) Calculations

#1) $\overline{\text{RASIN}}$ low = S0 + S1 + ''B'' PAL combinational output delay maximum = 62.5 + 15 = 77.5 ns maximum

#2) $\overline{\text{RASIN}}$ to $\overline{\text{RAS}}$ low = 20 ns maximum

#3) $\overline{\text{RASIN}}$ to $\overline{\text{CAS}}$ low = 80 ns (DP8419-80 $\overline{\text{RASIN}}$ − $\overline{\text{CAS}}$ low) − 3 ns (load of 72 DRAMs instead of 88 DRAMS speced in data sheet) = 77 ns

#4) 74F244 transceiver delay = 7 ns maximum

#5) CPU data setup time = 5 ns minimum

''tRAC'' = (S0 + S1) + (S2 + S3) + (SW + SW) + S4 (minimum) − #1 − #2 − #4 − #5

= 62.5 + 62.5 + 62.5 + 25 − 77.5 − 20 − 7 − 5

= 103 ns

''tCAC'' = (S0 + S1) + (S2 + S3) + (SW + SW) + S4 (minimum) − #1 − #3 − #4 − #5

= 62.5 + 62.5 + 62.5 + 25 − 77.5 − 77 − 7 − 5

= 46 ns

Therefore the DRAM chosen should have a ''tRAC'' less than or equal to 103 ns and a ''tCAC'' less than or equal to 46 ns.

V) iAPX 86/88/186/188 Family ''tRAC'' and ''tCAC'' Calculations

iAPX 86/88 8 MHz No Wait State Calculations

#1) $\overline{\text{RASIN}}$ low = Maximum clock high + 15 ns (''B'' PAL combinational output delay) = 82 + 15 = 97 ns maximum

#2) $\overline{\text{RASIN}}$ to $\overline{\text{RAS}}$ low = 20 ns maximum

#3) $\overline{\text{RASIN}}$ to $\overline{\text{CAS}}$ low = 97 ns (DP8419-80 $\overline{\text{RASIN}}$ − $\overline{\text{CAS}}$ low) − 3 ns (load of 72 DRAMs instead of 88 DRAMs speced in data sheet) = 94 ns maximum (using 25 ns minimum row address hold time)

#4) 74F245 transceiver delay = 7 ns maximum

#5) CPU data setup time to ''T4'' = 20 ns minimum

''tRAC'' = T1 + T2 + T3 − #1 − #2 − #4 − #5

= 125 + 125 + 125 − 97 − 20 − 7 − 20

= 231 ns

''tCAC'' = T1 + T2 + T3 − #1 − #3 − #4 − #5

= 125 + 125 + 125 − 97 − 94 − 7 − 20

= 157 ns

Therefore the DRAM chosen should have a ''tRAC'' less than or equal to 231 ns and a ''tCAC'' less than or equal to 157 ns. Standard 200 ns DRAMs meet this criteria.

iPX 186/188 8 MHz No Wait State Calculations

#1) $\overline{\text{RASIN}}$ low = Maximum clock high + 15 ns (''B'' PAL combinational output delay) = 70 + 15 = 85 ns maximum

#2) $\overline{\text{RASIN}}$ to $\overline{\text{RAS}}$ low = 20 ns maximum

#3) $\overline{\text{RASIN}}$ to $\overline{\text{CAS}}$ low = 97 ns (DP8419-80 $\overline{\text{RASIN}}$ − $\overline{\text{CAS}}$ low) − 3 ns (load of 72 DRAMs instead of 88 DRAMs speced in data sheet) = 94 ns maximum (using 25 ns minimum row address hold time)

#4) 74F245 transceiver delay = 7 ns maximum

#5) CPU data setup time to ''T4'' = 20 ns minimum

''tRAC'' = T1 + T2 + T3 − #1 − #2 − #4 − #5

= 125 + 125 + 125 − 85 − 20 − 7 − 20

= 243 ns

''tCAC'' = T1 + T2 + T3 − #1 − #3 − #4 − #5

= 125 + 125 + 125 − 85 − 94 − 7 − 20

= 169 ns

Therefore the DRAM chosen should have a ''tRAC'' less than or equal to 243 ns and a ''tCAC'' less than or equal to 169 ns. Standard 200 ns DRAMs meet this criteria.

iAPX 86/88 10 MHz No Wait State Calculations

#1) $\overline{\text{RASIN}}$ low = Maximum clock high + 15 ns (''B'' PAL combinational output delay) = 61 + 15 = 76 ns maximum

#2) $\overline{\text{RASIN}}$ to $\overline{\text{RAS}}$ low = 20 ns maximum

#3) $\overline{\text{RASIN}}$ to $\overline{\text{CAS}}$ low = 80 ns (DP8419-80 $\overline{\text{RASIN}}$ − $\overline{\text{CAS}}$ low) − 3 ns (load of 72 DRAMs instead of 88 DRAMs speced in data sheet) = 77 ns maximum (using 15 ns minimum row address hold time)

#4) 74F245 transceiver delay = 7 ns maximum

#5) CPU data setup time to ''T4'' = 5 ns minimum

''tRAC'' = T1 + T2 + T3 − #1 − #2 − #4 − #5

= 100 + 100 + 100 − 76 − 20 − 7 − 5

= 192 ns

''tCAC'' = T1 + T2 + T3 − #1 − #3 − #4 − #5

= 100 + 100 + 100 − 76 − 77 − 7 − 5

= 135 ns

Therefore the DRAM chosen should have a ''tRAC'' less than or equal to 192 ns and a ''tCAC'' less than or equal to 135 ns. Standard 150 ns DRAMs meet this criteria.

VI) iAPX 286 ''tRAC'' and ''tCAC'' Calculations

6 MHz iAPX 286, 12 MHz Clock, No Wait State Calculations

#1) $\overline{\text{RASIN}}$ low = T1 + 74AS04 gate delay + ''B'' PAL clocked output delay = 83.3 + 4.5 + 12 = 100 ns maximum

#2) $\overline{\text{RASIN}}$ to $\overline{\text{RAS}}$ low = 20 ns maximum

#3) $\overline{\text{RASIN}}$ to $\overline{\text{CAS}}$ low = 80 ns (DP8419-80 $\overline{\text{RASIN}}$ − $\overline{\text{CAS}}$ low) − 3 ns (load of 72 DRAMs instead of 88 DRAMs speced in data sheet) = 77 ns maximum (using 15 ns minimum row address hold time)

#4) 74F244 transceiver delay = 7 ns maximum

#5) CPU data setup time to ''T4'' = 20 ns minimum

''tRAC'' = T1 + T2 + T3 + T4 − #1 − #2 − #4 − #5

= 83.3 + 83.3 + 83.3 + 83.3 − 100 − 20 − 7 − 20 = 186 ns

''tCAC'' = T1 + T2 + T3 + T4 − #1 − #3 − #4 − #5

= 83.3 + 83.3 + 83.3 + 83.3 − 100 − 77 − 7 − 20 = 129 ns

Therefore the DRAM chosen should have a ''tRAC'' less than or equal to 186 ns and a ''tCAC'' less than or equal to 129 ns. Standard 150 ns DRAMs meet this criteria.

7 MHz iAPX 286, 14 MHz Clock, No Wait State Calculations

#1) $\overline{\text{RASIN}}$ low = T1 + 74AS04 gate delay + ''B'' PAL clocked output delay = 71.4 + 4.5 + 12 = 88 ns maximum

#2) $\overline{\text{RASIN}}$ to $\overline{\text{RAS}}$ low = 20 ns maximum

#3) $\overline{\text{RASIN}}$ to $\overline{\text{CAS}}$ low = 80 ns (DP8419-80 $\overline{\text{RASIN}}$ − $\overline{\text{CAS}}$ low) − 3 ns (load of 72 DRAMs instead of 88 DRAMs speced in data sheet) = 77 ns maximum (using 15 ns minimum row address hold time)

#4) 74F244 transceiver delay = 7 ns maximum

#5) CPU data setup time to ''T4'' = 10 ns minimum

''tRAC'' = T1 + T2 + T3 + T4 − #1 − #2 − #4 − #5

= 71.4 + 71.4 + 71.4 + 71.4 − 88 − 20 − 7 − 10 = 160 ns

''tCAC'' = T1 + T2 + T3 + T4 − #1 − #3 − #4 − #5
= 71.4 + 71.4 + 71.4 + 71.4 − 88 − 77 − 7 − 10 = 103 ns

Therefore the DRAM chosen should have a ''tRAC'' less than or equal to 160 ns and a ''tCAC'' less than or equal to 103 ns. Standard 150 ns DRAMs meet this criteria.

8 MHz iAPX 286, 16 MHz Clock, No Wait State Calculations

#1) $\overline{\text{RASIN}}$ low = T1 + 74AS04 gate delay + ''B'' PAL clocked output delay = 62.5 + 4.5 + 12 = 79 ns maximum

#2) $\overline{\text{RASIN}}$ to $\overline{\text{RAS}}$ low = 20 ns maximum

#3) $\overline{\text{RASIN}}$ to $\overline{\text{CAS}}$ low = 80 ns (DP8419-80 $\overline{\text{RASIN}}$ − $\overline{\text{CAS}}$ low) − 3 ns (load of 72 DRAMs instead of 88 DRAMs speced in data sheet) = 77 ns maximum (using 15 ns minimum row address hold time)

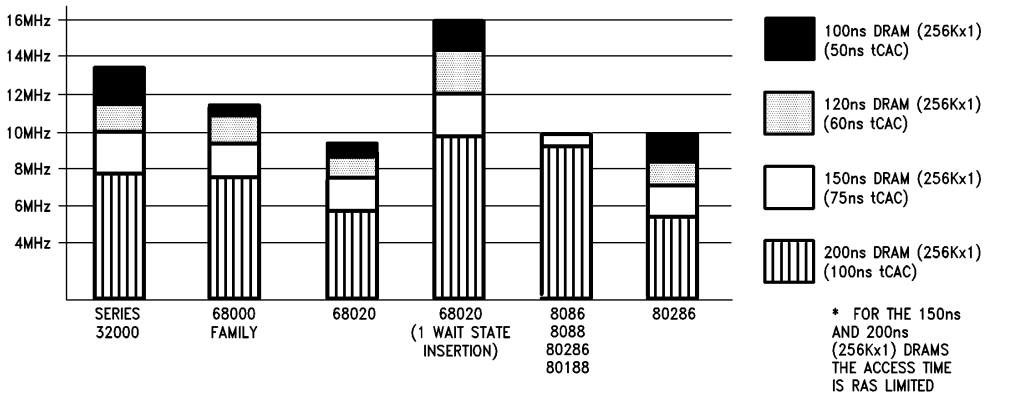
#4) 74F244 transceiver delay = 7 ns maximum

#5) CPU data setup time to ''T4'' = 10 ns minimum

''tRAC'' = T1 + T2 + T3 + T4 − #1 − #2 − #4 − #5
= 62.5 + 62.5 + 62.5 + 62.5 − 79 − 20 − 7 − 10 = 134 ns

''tCAC'' = T1 + T2 + T3 + T4 − #1 − #3 − #4 − #5
= 62.5 + 62.5 + 62.5 + 62.5 − 79 − 77 − 7 − 10 = 77 ns

Therefore the DRAM chosen should have a ''tRAC'' less than or equal to 134 ns and a ''tCAC'' less than or equal to 77 ns. Standard 120 ns DRAMs meet this criteria.



TL/F/8595–3

FIGURE 3

Note 1: The data presented in this figure is based on typical examples. Faster ''no wait state'' CPU performance is possible with several of the microprocessors shown above via the use of the DP8419-70 instead of the DP8419-80; the elimination of Data Bus Transceivers; a more tailored PAL (Refresh Access Arbitrator) approach; faster support logic; lower than the 15Ω damping resistor specified in the DP8419-80 data sheet; or, less than the specified capacitive load driven directly by the DP8419 (88 DRAMs).

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