Using Dynamic RAM With Series 32000® CPUs

National Semiconductor
Application Note 405
Microprocessor Applications
Engineering
July 1985

Recent advances in semiconductor technology have led to high-density, high-speed, low-cost dynamic random access memories (DRAMs), making large high-performance memory systems practical. DRAMs have complex timing and refresh requirements that can be met in different ways, depending on the size, speed, and processor interface requirements of the memory being designed. For low or intermediate performance, off-the-shelf components like the DP8419 can be used with a small amount of random logic. For higher performance, specialized high-speed circuitry must be designed

This application note presents the results of a timing analysis, and describes a DRAM interface for the NS32016 optimized for speed, simplicity and cost.

A future application note will discuss such features as error detection and correction, scrubbing, page mode and/or nibble mode support, in conjunction with future CPUs, such as the NS32332.

TIMING ANALYSIS RESULTS

Figures 1 and *2* show the number of CPU wait states required during a DRAM access cycle, for different CPU clock frequencies and DRAM access times.

Figure 1 is related to a DRAM interface using the DP8419 DRAM controller. Descriptions of the circuitry for use with the DP8419 and related timing diagrams are omitted. See the ''DP8400 Memory Interface Family Applications'' book for details.

Figure 2 shows the same data for a DRAM interface using standard TTL components, specially designed for the NS32016.

The special-purpose interface requires fewer wait states than the DP8419-based interface, especially at high frequencies.

These results assume a minimum amount of buffering between DRAM and CPU.

The results do not apply when CPU and DRAM reside on different circuit boards communicating through the system bus, since extra wait states may be required to provide for synchronization operations and extra levels of buffering.

INTERFACE DESCRIPTION

The DRAM interface presented here has been optimized for overall access time, while requiring moderate speed DRAMs, given the CPU clock frequency.

This may be significant when a relatively large DRAM array must be designed since a substantial saving can be achieved.

The result of these considerations has been the design of a high-speed DRAM interface capable of working with a CPU clock frequency of up to 15-MHz and 100-nsec DRAM chips, without wait states.

The only assumption has been that the DRAM array is directly accessible through the CPU local bus.

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RAM Access Time in nsec	CPU Wait States Required							
250	0	1	1	1	1	2		
200	0	0	1	1	1	1	2	2
150	0	0	0	0	1	1	1	1
120	0	0	0	0	0	1	1	1
100	0	0	0	0	0	0	1	1
	6	7	8	9	10	11	12	13

CPU Clock Frequency in MHz

FIGURE 1. Memory Speed vs. CPU Wait States When Using the DP8419 DRAM Controller

RAM Access Time in nsec	CPU Wait States Required									
250	0	0	1	1	1	1				
200	0	0	0	0	1	1	1	1		
150	0	0	0	0	0	0	1	1	1	1
120	0	0	0	0	0	0	0	0	1	1
100	0	0	0	0	0	0	0	0	0	0
	6	7	8	9	10	11	12	13	14	15

CPU Clock Frequency in MHz

FIGURE 2. Memory Speed vs. CPU Wait States When Using Random Logic

This configuration presents some speed advantages; for example, the amount of buffering interposed between CPU and DRAM array is minimal. This translates into shorter propagation delays for address, data and other relevant signals.

Another advantage is that the interface can work in complete synchronization with the CPU. This significantly improves performance since no time is spent for synchronization. Reliability also improves since the possibility of metastable states in synchronizing flip-flops is eliminated.

A block diagram of the DRAM interface is shown in *Figure 3*. *Figures 4* through *7* show circuit diagrams and timing diagrams.

Interface operation details follow.

$\overline{\text{RAS}}$ AND $\overline{\text{CAS}}$ GENERATION

This is the most critical part of the entire interface circuit. To avoid wait states during a CPU read cycle, the DRAM must provide the data before the falling edge of clock phase PH12 during state T3. This requires that the $\overline{\text{RAS}}$ signal be generated early in the CPU bus cycle to meet the DRAM access time. On the other hand, the $\overline{\text{RAS}}$ signal can be asserted only after the row address is valid and the $\overline{\text{RAS}}$ precharge time from a previous CPU access or refresh cycle has elapsed.

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The interface circuit shown in *Figures 4* and *5* relies on two advanced clock signals obtained from CTTL through a delay line and some standard TTL gates.

The advanced clock signals, CTTLA and $\overline{\text{CTTLB}}$, are used to clock the circuit that arbitrates between CPU access requests and refresh requests. The $\overline{\text{CTTLB}}$ signal is also used to enable an advanced $\overline{\text{RAS}}$ generation circuit, which causes the $\overline{\text{RAS}}$ signal to be asserted earlier than the CPU access-grant signal from the arbitration circuit. This speeds up the $\overline{\text{RAS}}$ signal by about 10 ns by avoiding the time required by the arbitration circuit to change state.

A different delay line is used to generate the $\overline{\text{CAS}}$ signal and to switch the multiplexers for the column addresses. Note that the $\overline{\text{CAS}}$ signal during write cycles is delayed until the beginning of CPU state T3, to guarantee that the data being written to the DRAM is valid at the time $\overline{\text{CAS}}$ is asserted. The $\overline{\text{CAS}}$ signal is deasserted after the trailing edge of $\overline{\text{RAS}}$ to guarantee the minimum pulse width requirement.

The timing diagrams in *Figures 6* and *7* show the signal sequences for both read and write cycles.

ADDRESS MULTIPLEXING

The multiplexing of the various addresses for the DRAM chips is accomplished via four 74AS153 multiplexer chips in addition to some standard TTL gates used to multiplex the top two address bits needed for 256k DRAMs. The resulting nine address lines are then buffered and sent to the DRAMs through series damping resistors. The function of these resistors is to minimize ringing.

REFRESH

The refresh circuitry includes an address counter, a timer and a number of flip-flops used to generate the refresh cycle and to latch the refresh request until the end of the refresh cycle.

The address counter is an 8-bit counter implemented by cascading the two 4-bit counters of a 74LS393 chip. This counter provides up to 256 refresh addresses and is incremented at the end of each refresh cycle.

The refresh timer is responsible for generating the refresh request signal whenever a refresh cycle is needed. This timer is implemented by cascading two 4-bit counters. Both counters are clocked by the $\overline{\text{CTTLB}}$ signal; the first is a presettable binary counter that divides the clock signal by a specified value; the second can be either a BCD or a binary counter depending on the CPU clock frequency.

With this arrangement, a refresh request is generated after a fixed time interval from the previous request, regardless of the CPU activity. A more sophisticated circuit that generates requests when the CPU is idle could also be implemented. However, such a circuit has not been considered here because the performance degradation due to the refresh is relatively small (less than 3.3 percent), and the improvement attainable by using a more sophisticated circuit would not justify the extra hardware required.

CONCLUSIONS

The DRAM interface described in this application uses two TTL-buffered delay lines to obtain speed advantages. One delay line is used to time the $\overline{\text{CAS}}$ signal and to enable the column address. The other is used to generate the advanced clock signals from CTTL.

Below 10 MHz, the advanced clocks might not be required, and the related delay line can be eliminated. When this is done, however, higher speed DRAMs must be used. If, on the other hand, advanced clocks must be used for frequencies lower than 10 MHz, a delay line with a larger delay (e.g. DDU-7J-100) might be needed.

Delay lines are extremely versatile for this kind of application due to their accuracy and the fact that different delays are easily available to accommodate different DRAM types.

The savings attainable by using slower DRAM chips, in addition to the reliability improvement and cleaner design, make delay lines a valid alternative, even though their cost is relatively high in comparison to standard TTL gates.

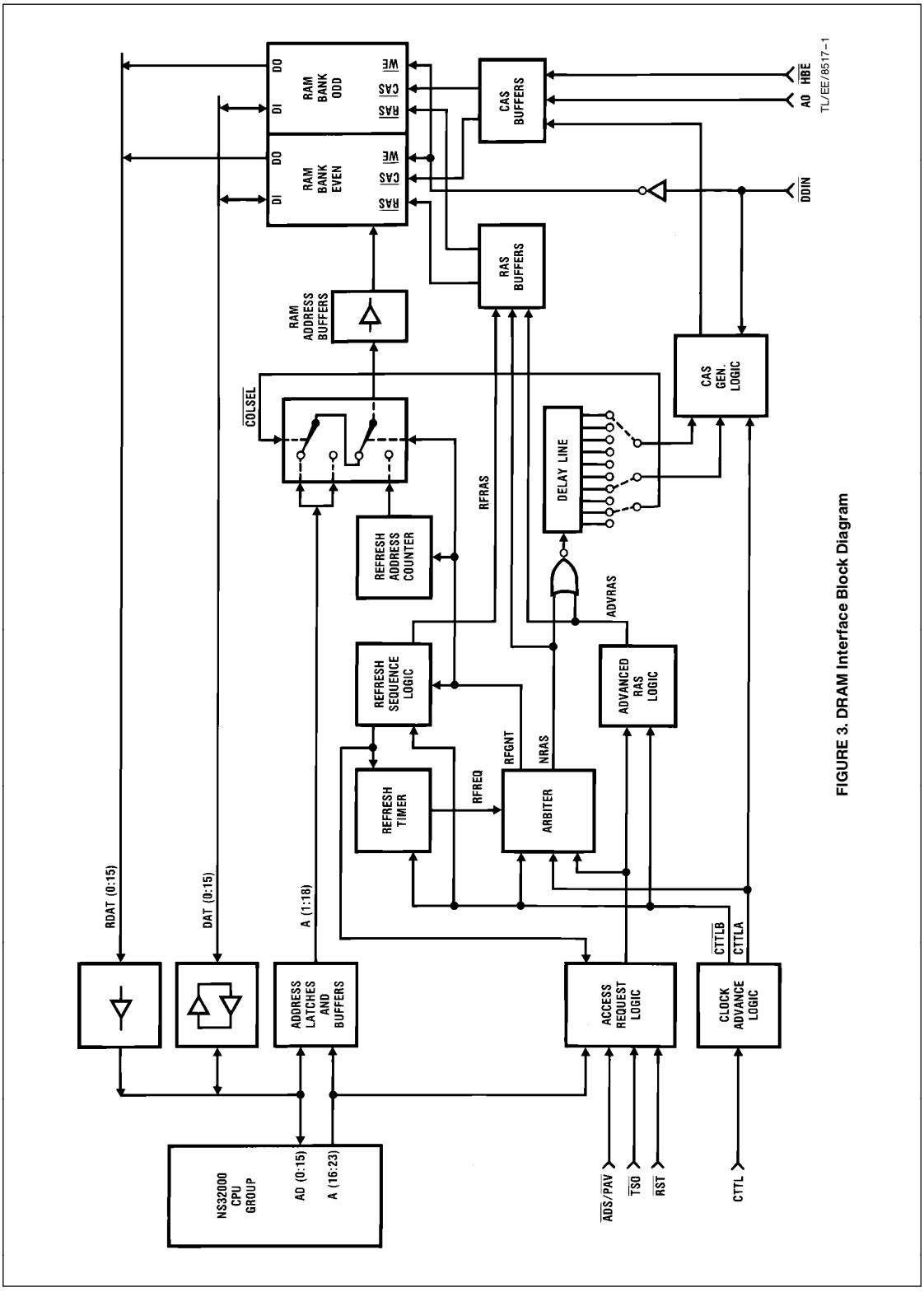

FIGURE 3. DRAM Interface Block Diagram

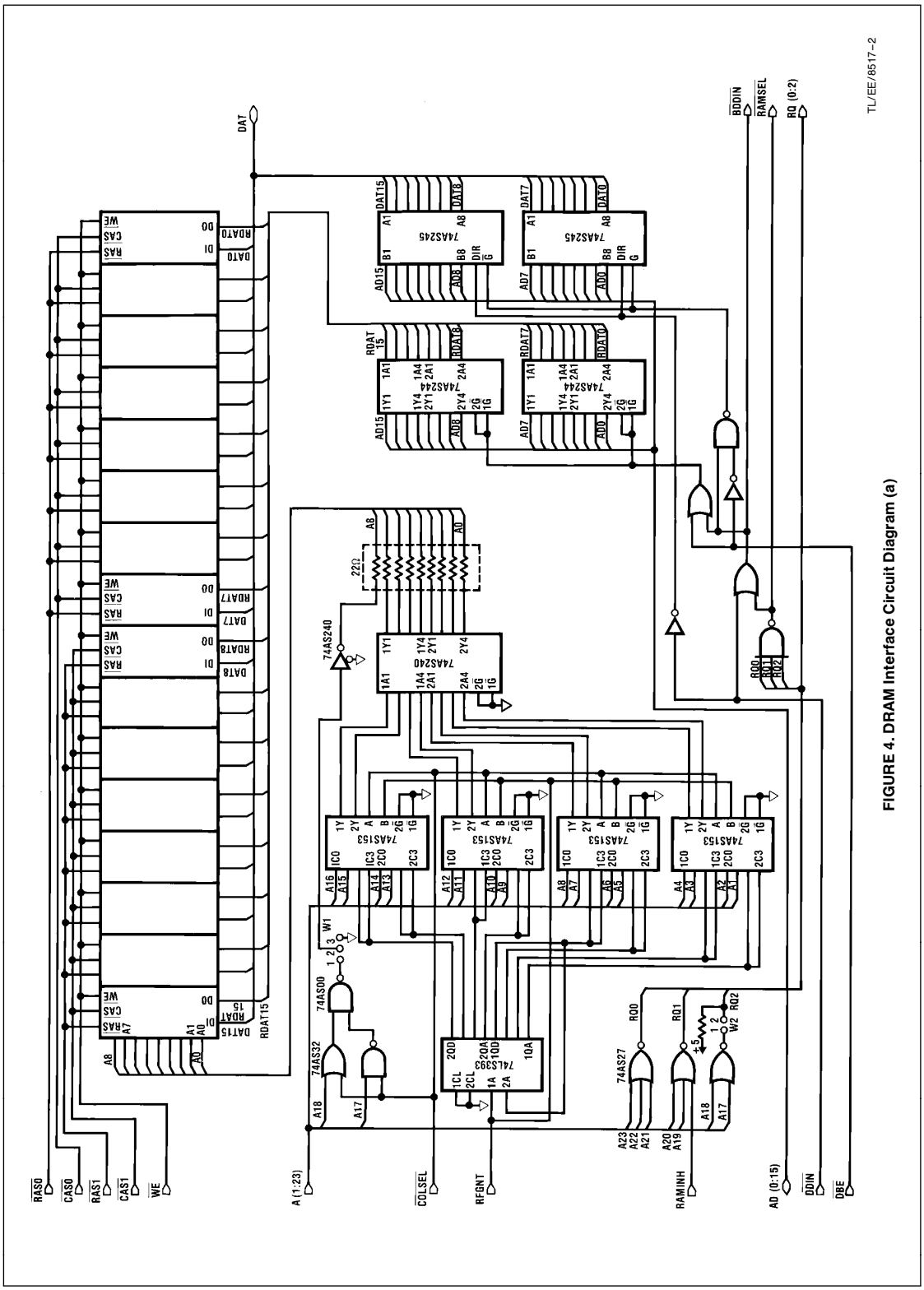

FIGURE 4. DRAM Interface Circuit Diagram (a)

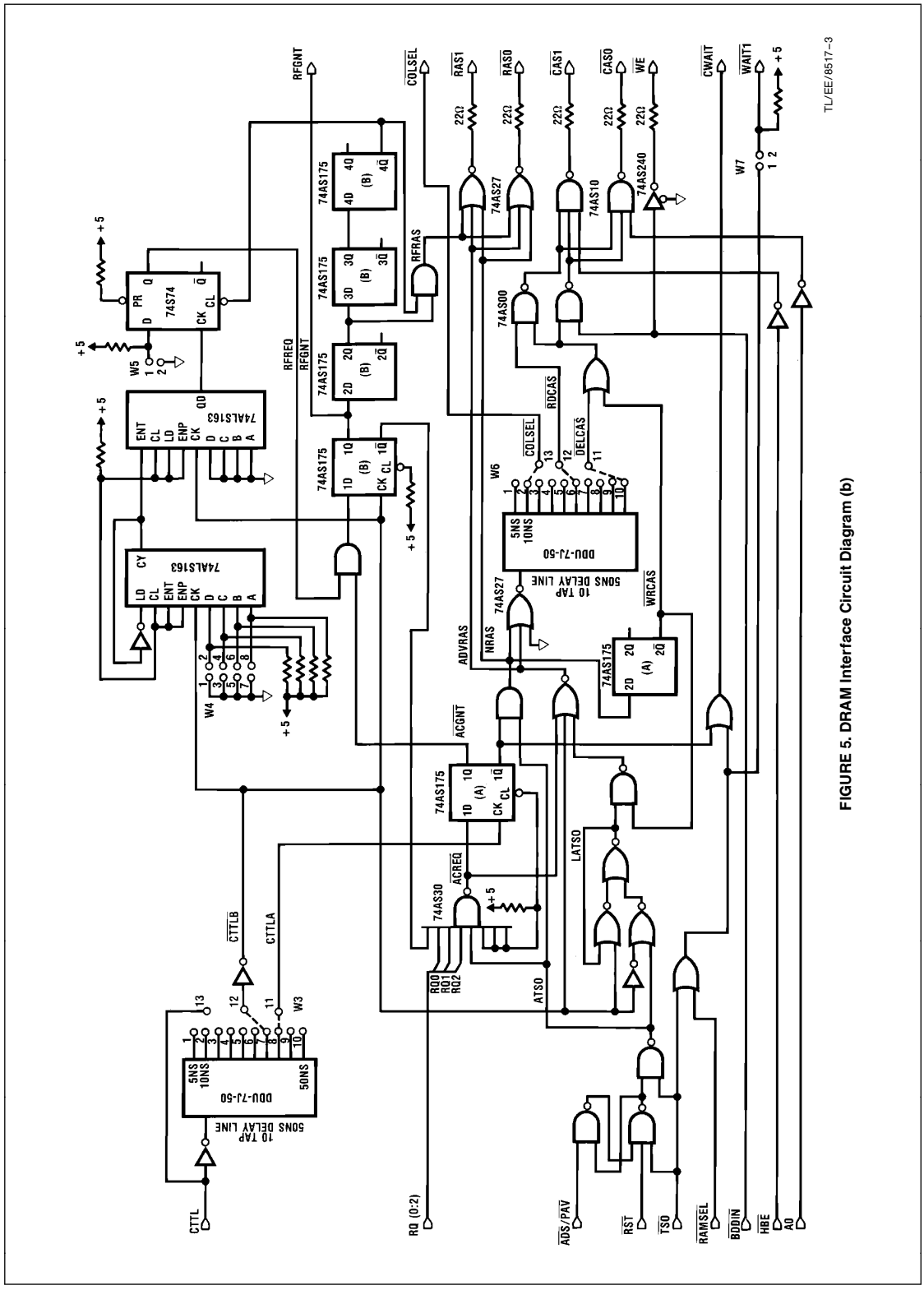

FIGURE 5. DRAM Interface Circuit Diagram (b)

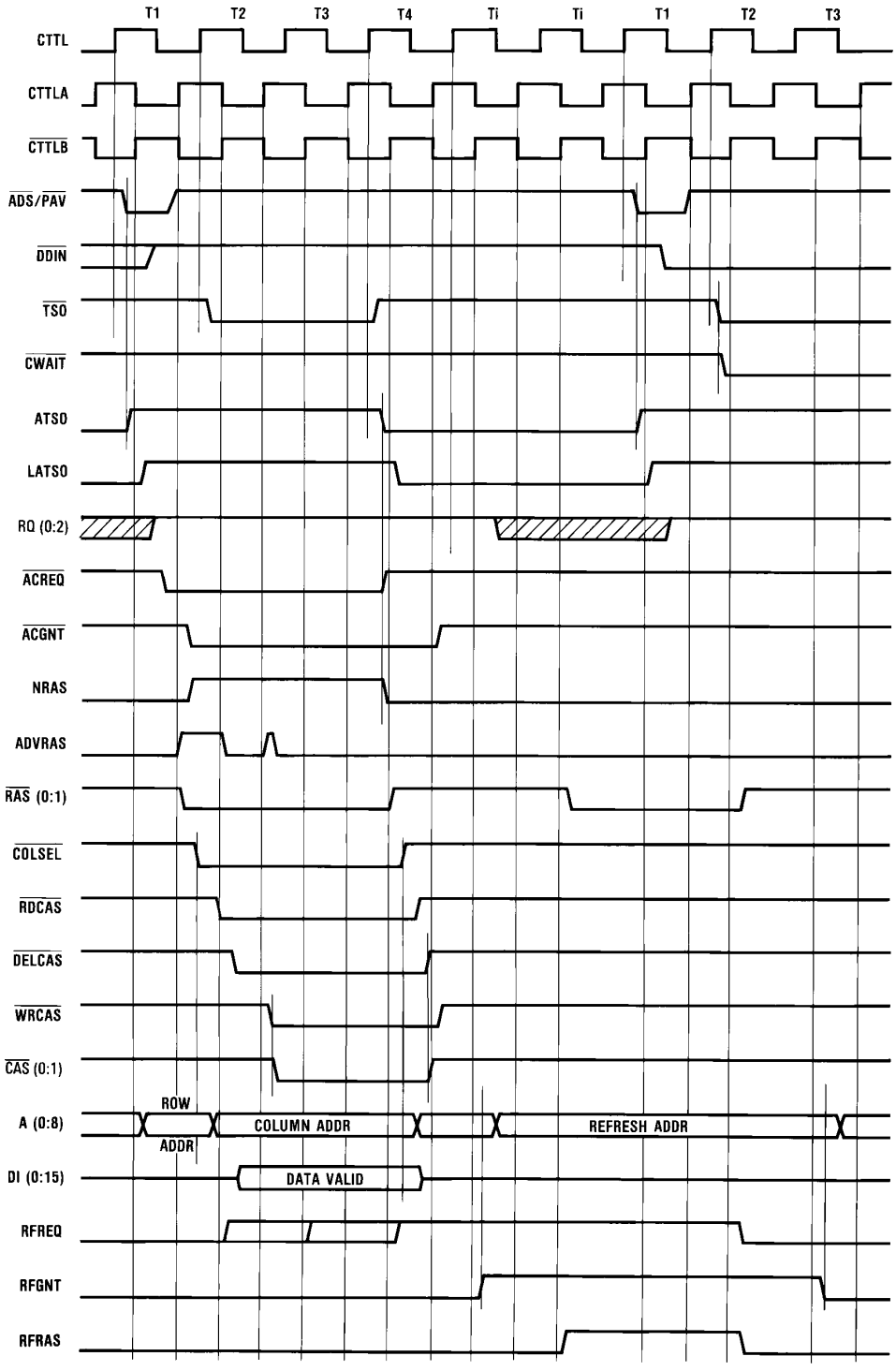

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FIGURE 6. Write Cycle Followed By a Refresh Cycle

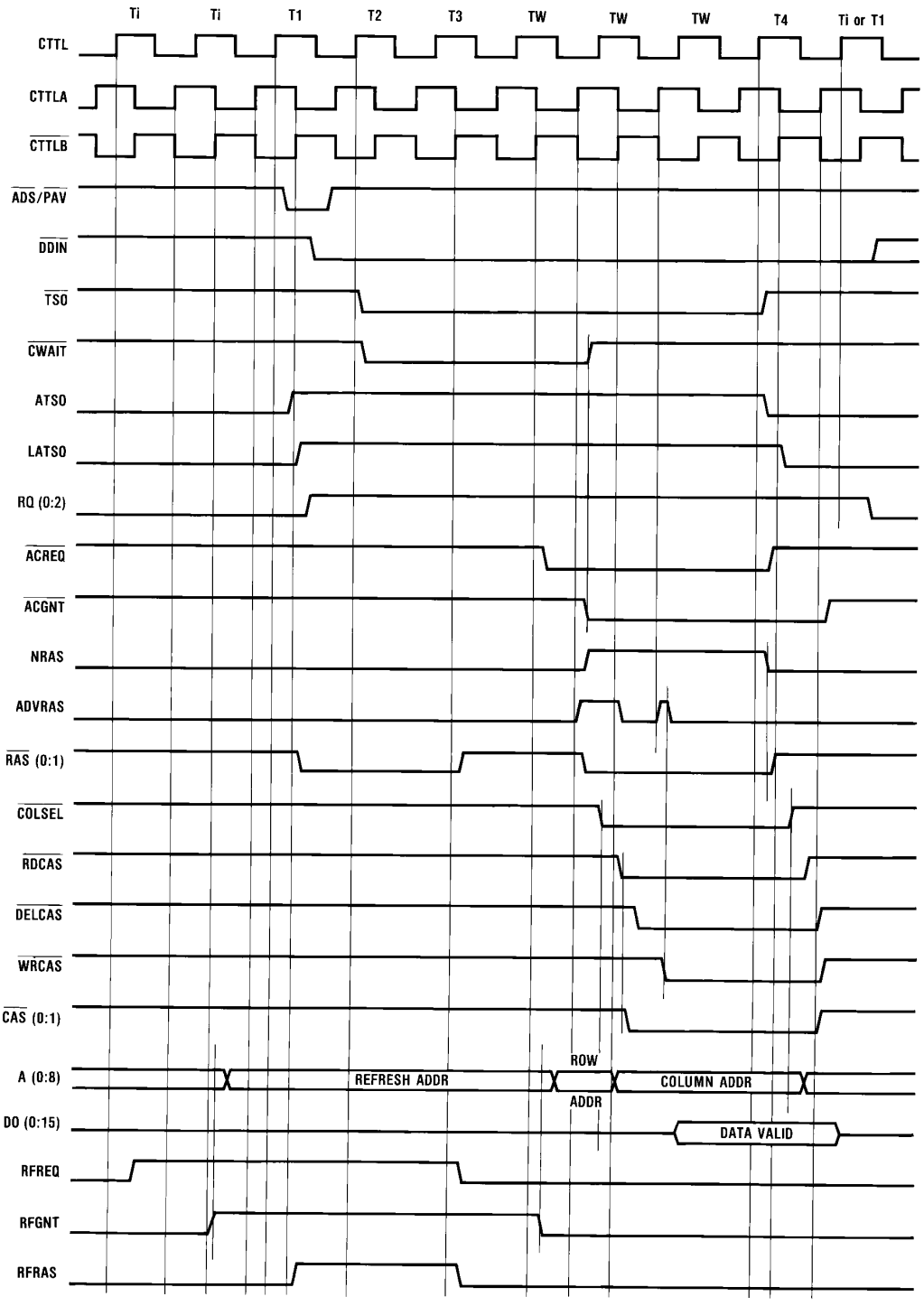

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FIGURE 7. Refresh Cycle Followed By a Read Cycle

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