MOTOROLA
SEMICONDUCTOR
**TECHNICAL DATA**

2N6545

Designers Data Sheet

SWITCHMODE SERIES
NPN SILICON POWER TRANSISTOR

The 2N6545 transistor is designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. It is particularly suited for 115 and 220 volt line operated switch-mode applications such as:

- Switching Regulators
- PWM Inverters and Motor Controls
- Solenoid and Relay Drivers
- Deflection Circuits

Specification Features —
   High Temperature Performance Specified for:
   Reversed Biased SOA with Inductive Loads
   Switching Times with Inductive Loads
   Saturation Voltages
   Leakage Currents
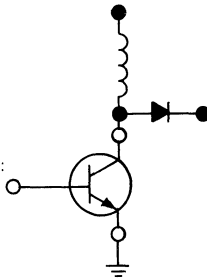
8 AMPERE
NPN SILICON
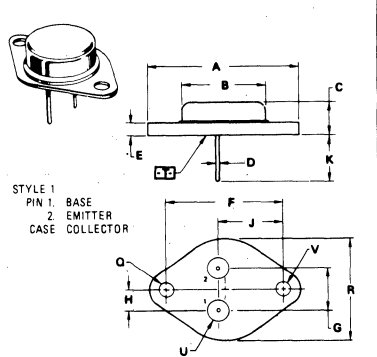### POWER TRANSISTOR

400 VOLTS
125 WATTS

Designer's Data for "Worst Case" Conditions

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.

STYLE 1
PIN 1. BASE
     2. EMITTER
CASE COLLECTOR

NOTES:
1. DIMENSIONS Q AND V ARE DATUMS.
2. ⊥ IS SEATING PLANE AND DATUM.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q:

⊕ | ⌀0.13 (0.005) Ⓜ | T | V Ⓜ |

FOR LEADS:

⊕ | ⌀0.13 (0.005) Ⓜ T | V Ⓜ | Q Ⓜ |

4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	–	26.67	–	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

CASE 1-05
TO-204AA

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*MAXIMUM RATINGS

Rating	Symbol	2N6545	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	400	Vdc
Collector-Emitter Voltage	$V_{CEX(sus)}$	450	Vdc
Collector-Emitter Voltage	V_{CEV}	850	Vdc
Emitter Base Voltage	V_{EB}	9.0	Vdc
Collector Current — Continuous	I_C	8.0	Adc
— Peak (1)	I_{CM}	16	
Base Current — Continuous	I_B	8.0	Adc
— Peak (1)	I_{BM}	16	
Emitter Current — Continuous	I_E	16	Adc
— Peak (1)	I_{EM}	32	
Total Power Dissipation @ T_C = 25°C	P_D	125	Watts
@ T_C = 100°C		71.5	
Derate above 25°C		0.714	W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.4	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	275	°C

*Indicates JEDEC Registered Data

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ⩽ 10%.

*ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS (1)				
Collector-Emitter Sustaining Voltage	$V_{CEO(sus)}$			Vdc
(I_C = 100 mA, I_B = 0) 2N6545		400	–	
Collector-Emitter Sustaining Voltage	$V_{CEX(sus)}$			Vdc
(I_C = 4.5 A, V_{clamp} = Rated V_{CEX}, T_C = 100°C)		450	–	
(I_C = 8.0 A, V_{clamp} = Rated V_{CEO} –100 V, T_C = 100°C)		300	–	
Collector Cutoff Current	I_{CEV}			mAdc
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc)		–	0.5	
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)		–	2.5	
Collector Cutoff Current	I_{CER}			mAdc
(V_{CE} = Rated V_{CEV}, R_{BE} = 50 Ω, T_C = 100°C)		–	3.0	
Emitter Cutoff Current	I_{EBO}			mAdc
(V_{EB} = 9.0 Vdc, I_C = 0)		–	1.0	
SECOND BREAKDOWN				
Second Breakdown Collector Current with base forward biased t = 1.0 s (non-repetitive) (V_{CE} = 100 Vdc)	$I_{S/b}$	0.2	–	Adc
ON CHARACTERISTICS (1)				
DC Current Gain	h_{FE}			–
(I_C = 2.5 Adc, V_{CE} = 3.0 Vdc)		12	60	
(I_C = 5.0 Adc, V_{CE} = 3.0 Vdc)		7.0	35	
Collector-Emitter Saturation Voltage	$V_{CE(sat)}$			Vdc
(I_C = 5.0 Adc, I_B = 1.0 Adc)		–	1.5	
(I_C = 8.0 Adc, I_B = 2.0 Adc)		–	5.0	
(I_C = 5.0 Adc, I_B = 1.0 Adc, T_C = 100°C)		–	2.5	
Base-Emitter Saturation Voltage	$V_{BE(sat)}$			Vdc
(I_C = 5.0 Adc, I_B = 1.0 Adc)		–	1.6	
(I_C = 5.0 Adc, I_B = 1.0 Adc, T_C = 100°C)		–	1.6	
DYNAMIC CHARACTERISTICS				
Current-Gain — Bandwidth Product	f_T	6.0	28	MHz
(I_C = 300 mAdc, V_{CE} = 10 Vdc, f_{test} = 1.0 MHz)				
Output Capacitance	C_{ob}	75	300	pF
(V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1.0 MHz)				
SWITCHING CHARACTERISTICS				
Resistive Load				
Delay Time	t_d	–	0.05	μs
Rise Time	t_r	–	1.0	μs
Storage Time	t_s	–	4.0	μs
Fall Time	t_f	–	1.0	μs
Inductive Load, Clamped				
Storage Time	t_s	–	4.0	μs
Fall Time	t_f	–	0.9	μs
		Typical		
Storage Time	t_s	1.2		μs
Fall Time	t_f	0.18		μs

Resistive Load: (V_{CC} = 250 Vdc, I_C = 5.0 A, I_{B1} = I_{B2} = 1.0 A, t_p = 100 μs, Duty Cycle ≤ 2.0%)

Inductive Load, Clamped: (I_C = 5.0 A(pk), V_{clamp} = Rated V_{CEX}, I_{B1} = 1.0 A, $V_{BE(off)}$ = 5.0 Vdc, T_C = 100°C)

Typical: (I_C = 5.0 A(pk), V_{clamp} = Rated V_{CEX}, I_{B1} = 1.0 A, $V_{BE(off)}$ = 5.0 Vdc, T_C = 25°C)

*Indicates JEDEC Registered Data.
(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2%.
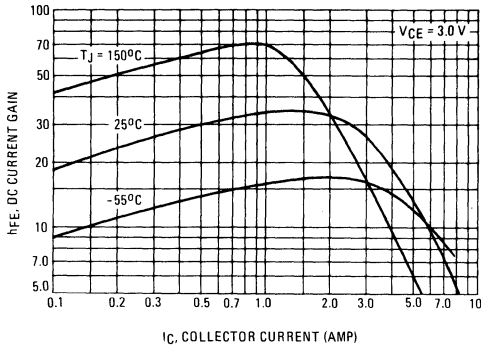
DC CHARACTERISTICS

FIGURE 1 – DC CURRENT GAIN

$V_{CE} = 3.0$ V

$T_J = 150°C$
$25°C$
$-55°C$

hFE, DC CURRENT GAIN

I_C, COLLECTOR CURRENT (AMP)

FIGURE 2 – COLLECTOR SATURATION REGION

V_{CE}, COLLECTOR-EMITTER VOLTAGE (VOLTS)

$T_J = 25°C$

$I_C = 0.25$ A   1.0 A   2.5   5.0 A

I_B, BASE CURRENT (AMP)

FIGURE 3 – "ON" VOLTAGE

$T_J = 25°C$

V, VOLTAGE (VOLTS)

$V_{BE(sat)}$ @ $I_C/I_B = 5.0$
$V_{BE(on)}$ @ $V_{CE} = 3.0$ V
$I_C/I_B = 5.0$
2.0
$V_{CE(sat)}$

I_C, COLLECTOR CURRENT (AMP)
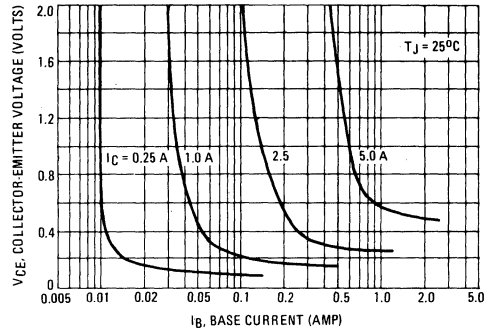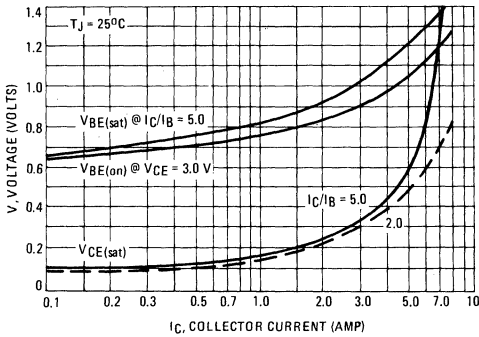
FIGURE 4 – TEMPERATURE COEFFICIENTS

θV, TEMPERATURE COEFFICIENTS (mV/°C)

*Applies for $I_C/I_B \leqslant h_{FE}/3$

*θVC for $V_{CE(sat)}$
$25°C$ to $150°C$
$-55°C$ to $25°C$
$25°C$ to $150°C$
θVB for V_{BE}
$-55°C$ to $25°C$

I_C, COLLECTOR CURRENT (AMP)

FIGURE 5 – TURN-ON TIME

$V_{CC} = 250$ V
$I_C/I_B = 5.0$
$T_J = 25°C$

t_r

t, TIME (ns)

t_d @ $V_{BE(off)} = 5.0$ V

I_C, COLLECTOR CURRENT (AMP)

FIGURE 6 – TURN-OFF TIME

$V_{CC} = 250$ V
$I_C/I_B = 5.0$
$I_{B1} = I_{B2}$
$T_J = 25°C$

t_s

t, TIME (ns)

t_f

I_C, COLLECTOR CURRENT (mA)

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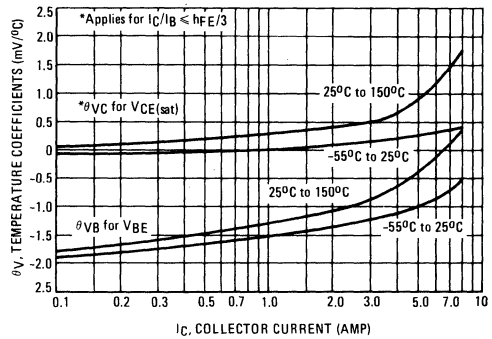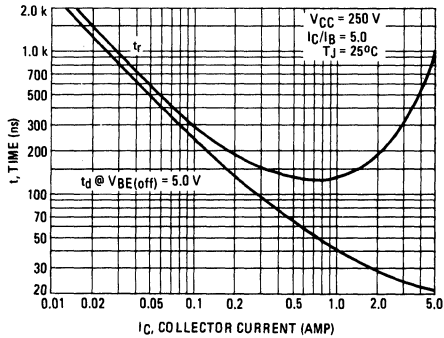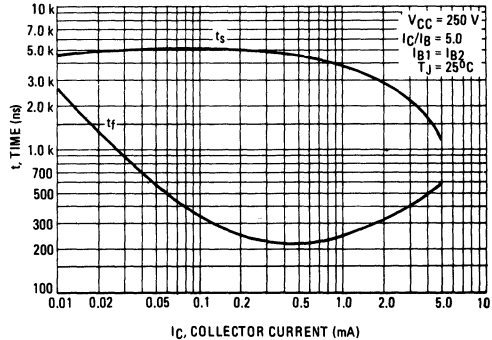
FIGURE 7 – FORWARD BIAS SAFE OPERATING AREA

I_C, COLLECTOR CURRENT (AMP)

V_CE, COLLECTOR-EMITTER VOLTAGE (VOLTS)
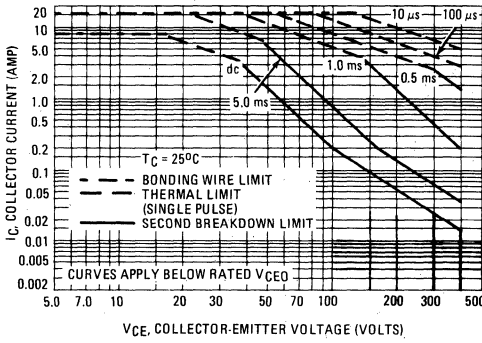
FIGURE 8 – REVERSE BIAS SAFE OPERATING AREA

I_C, COLLECTOR CURRENT (AMP)

V_CE, COLLECTOR-EMITTER VOLTAGE (VOLTS)

FIGURE 9 – POWER DERATING

POWER DERATING FACTOR (%)

T_C, CASE TEMPERATURE (°C)
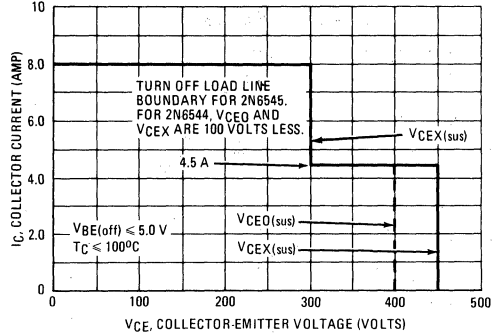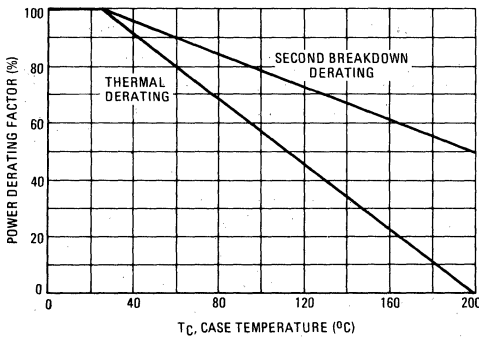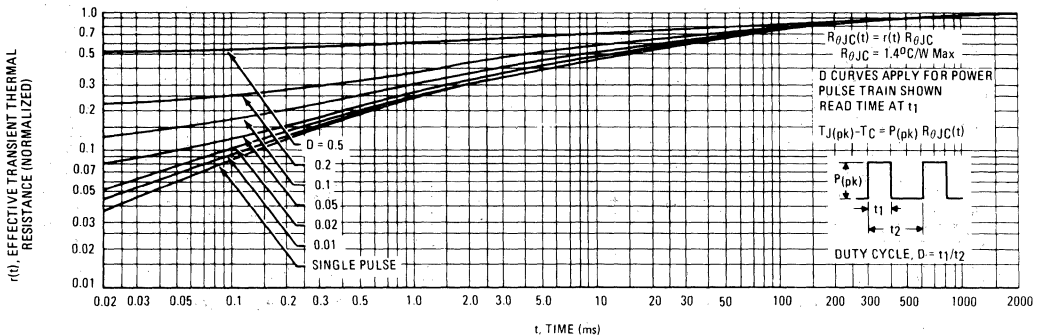
There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 7 is based on $T_C = 25^\circ C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geqslant 25^\circ C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 7 may be found at any case temperature by using the appropriate curve on Figure 9.

$T_{J(pk)}$ may be calculated from the data in Figure 10. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. The reverse biased safe operating area (Figure 8) is the boundary the load line may traverse during turn-off.

FIGURE 10 – THERMAL RESPONSE

r(t), EFFECTIVE TRANSIENT THERMAL RESISTANCE (NORMALIZED)

$R_{\theta JC}(t) = r(t) R_{\theta JC}$
$R_{\theta JC} = 1.4^\circ C/W$ Max
D CURVES APPLY FOR POWER PULSE TRAIN SHOWN READ TIME AT t_1
$T_{J(pk)} - T_C = P_{(pk)} R_{\theta JC}(t)$
DUTY CYCLE, D = t_1/t_2

t, TIME (ms)