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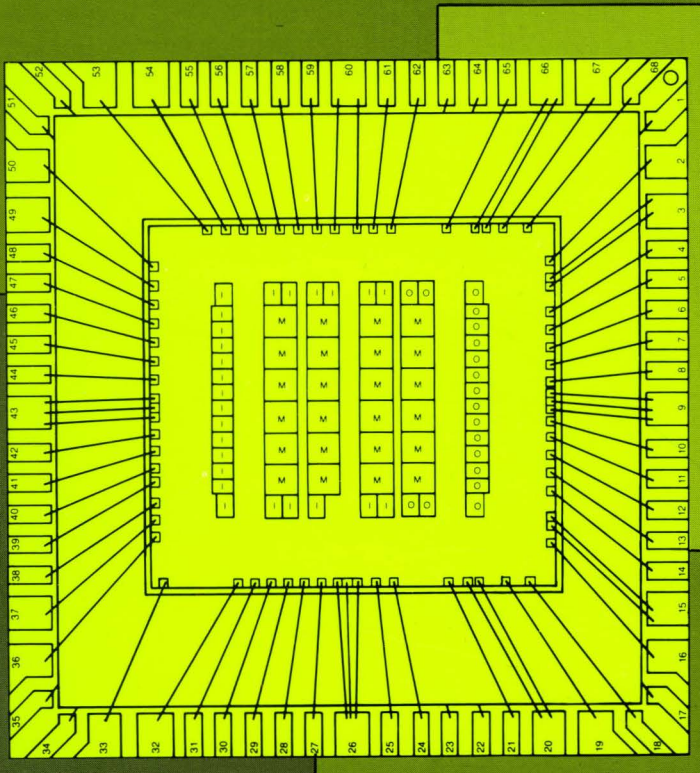
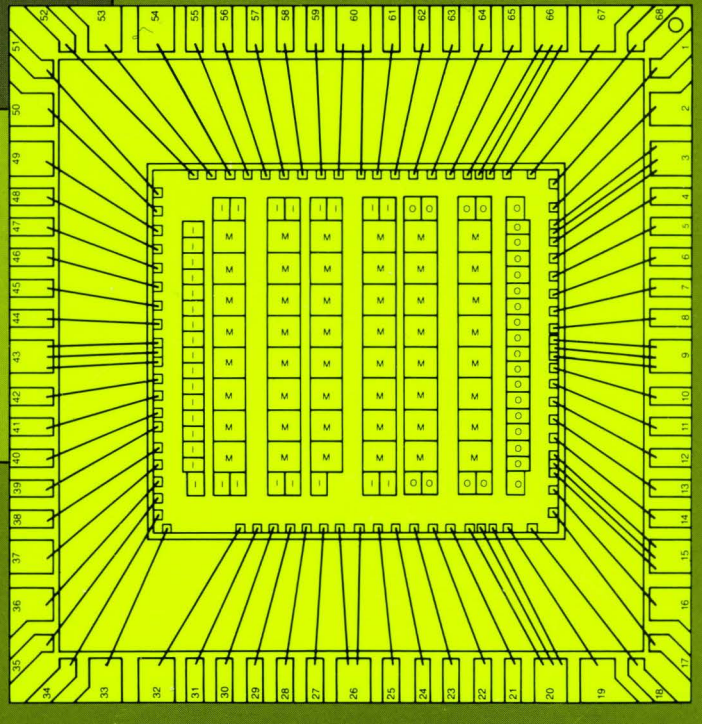
MOTOROLA

MCA600ECL and MCA1200ECL MECL 10,000 MACROCELL ARRAYS

design manual





DESIGN MANUAL

MCA600ECL and MCA1200ECL
MECL 10,000 MACROCELL ARRAYS

DESIGN GUIDELINES

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DESIGN GUIDELINES

The Macrocell Approach Toward
HIGH-SPEED VLSI DIGITAL CIRCUITS

To satisfy the demand for large-scale digital integrated circuits, the semiconductor industry has developed three basic approaches:

1. Standard, off-the-shelf circuits, 2. Custom Circuits, and 3. Gate arrays.

The first approach represents the lowest cost option for the LSI user because such circuits are normally sold in relatively large quantities to the entire industry, thereby benefitting from the cost advantage of large-volume manufacture. However, because of the high risk factor involved in having the industry adopt a particular LSI circuit as a standard (thereby permitting large-volume sales), the line of standard LSI circuits is limited.

The second approach provides each customer with exactly the circuits he needs (usually on a proprietary basis), but the cost per circuit is quite high unless the volume requirements are large enough to amortize the relatively high development costs. Moreover, development time of complex custom circuits can be on the order of 1 to 2 years.

The third approach involves a standard array of a large number of gate circuits diffused into a silicon chip. The circuit designer provides the semiconductor manufacturer with an interconnecting metallization pattern that converts these basic gates into functional custom circuits. This approach represents a trade-off between development cost and time on the one hand, and performance on the other hand. Performance is compromised because of the necessity for using a gate as the basic building block for LSI circuits. This results in longer propagation delays, compared with similar functions using ECL series-gating techniques (for example), and usually involves a relatively inefficient use of chip real estate.

To supplement the three techniques described above, Motorola has developed the Macrocell approach toward custom LSI – an approach that circumvents the excessive cost and time factor of custom circuits, and reduces the deficiencies of the conventional gate arrays.

I. THE MACROCELL ARRAY CONCEPT

The Macrocell Array is, actually, an extension of the gate-array concept. Instead of gates, however, each cell in the array contains a number of unconnected transistors and resistors. Stored within a computer are the specifications for creating interconnecting patterns that can transform the unconnected transistors and resistors within each cell into SSI/MSI logic functions, called Macros. These Macros take the form of standard logic elements such as dual type D flip-flops, dual full adders, quad latches, and many other predefined functions. Some comprise series-gated ECL structures for optimized performance.

Presently, the Macrocell library contains more than 100 different logic functions.

To generate an LSI design, the designer need only be concerned with developing his circuit by selecting the appropriate Macros from the Macro library, placing these in the desired cell location and creating the necessary cell interconnecting pattern. The computer itself generates the proper intra-connecting pattern within each cell.

This CAD (computer-aided design) approach, operated via standard time-sharing terminals, greatly speeds up the circuit development while simplifying the designer/Motorola interface. It serves to design the interconnects, to check out the performance of the designs and to generate the custom metal patterns which complete the IC processing sequence.

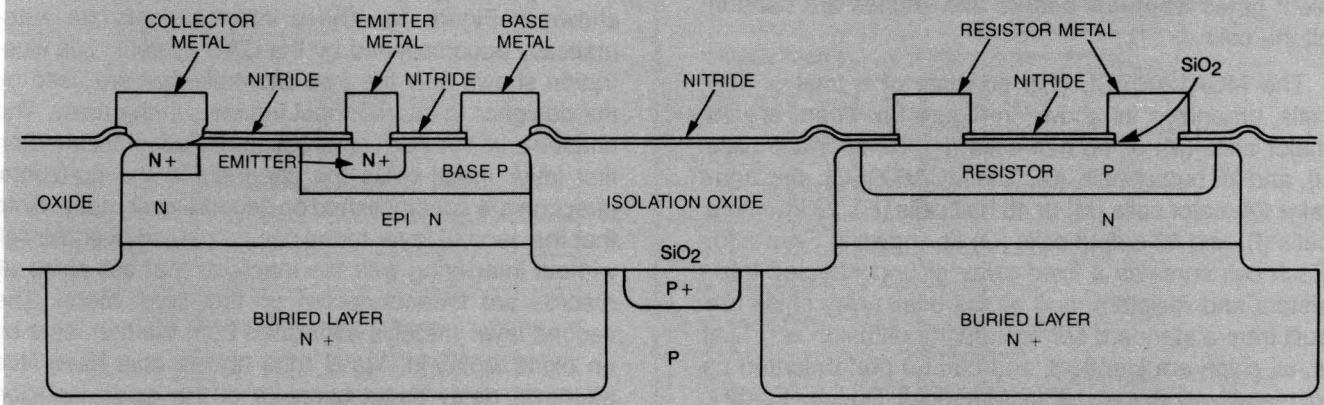
Compared with the conventional approach to custom LSI circuits, the Macrocell approach offers a tremendous reduction in delivery time. With a stockpile of fully diffused wafers, turnaround time (from the time the customer gives the go-ahead signal for generating the metal mask until he receives finished parts) is 7 weeks maximum.

Compared with gate arrays, the use of higher component density and more efficiently designed subcircuits (macros) yields a substantial improvement in performance (circuit speed), while a greater utilization of on-chip components reduces potential system costs.

Compared with equivalent systems developed with discrete logic (separately packaged SSI/MSI logic function) the high packing density of the MCA1200ECL chip offers up to 50-to-1 reduction in system component count, with a power dissipation improvement (reduction) of as much as 10 to 1.

MOSAIC I — A NEW PROCESS FOR HIGH DENSITY BIPOLAR CIRCUITS

A new process called MOSAIC I (see Figure 2) is used in the Macrocell Array in order to achieve the high performance requirements of .9ns (typical) for internal gate delays. The process forms a non-walled emitter and a walled base. An oxide isolation between devices is accomplished with an isotropic etch. The peaking of the oxide is controlled and monitored to guarantee flatness during processing. The peaking of the oxide is maintained to less than 4000 Å thick. The first layer metal is 10,000 Å thick which covers the peaking of the oxide reliably. A nitride surface covers the oxide so that the metal system is over nitride which is normal for other MECL processes. The base and emitter diffusions are controlled by ion implantation to a junction depth used in other processes. Also, the oxide isolated process achieves a high packing density while achieving good yields.



NOTE: MOSAIC IS THE ABBREVIATION OF "MOTOROLA OXIDE ISOLATED SELF-ALIGNED IMPLANTED CIRCUIT."

FIGURE 2. Cross-Section Of MOSAIC I Process

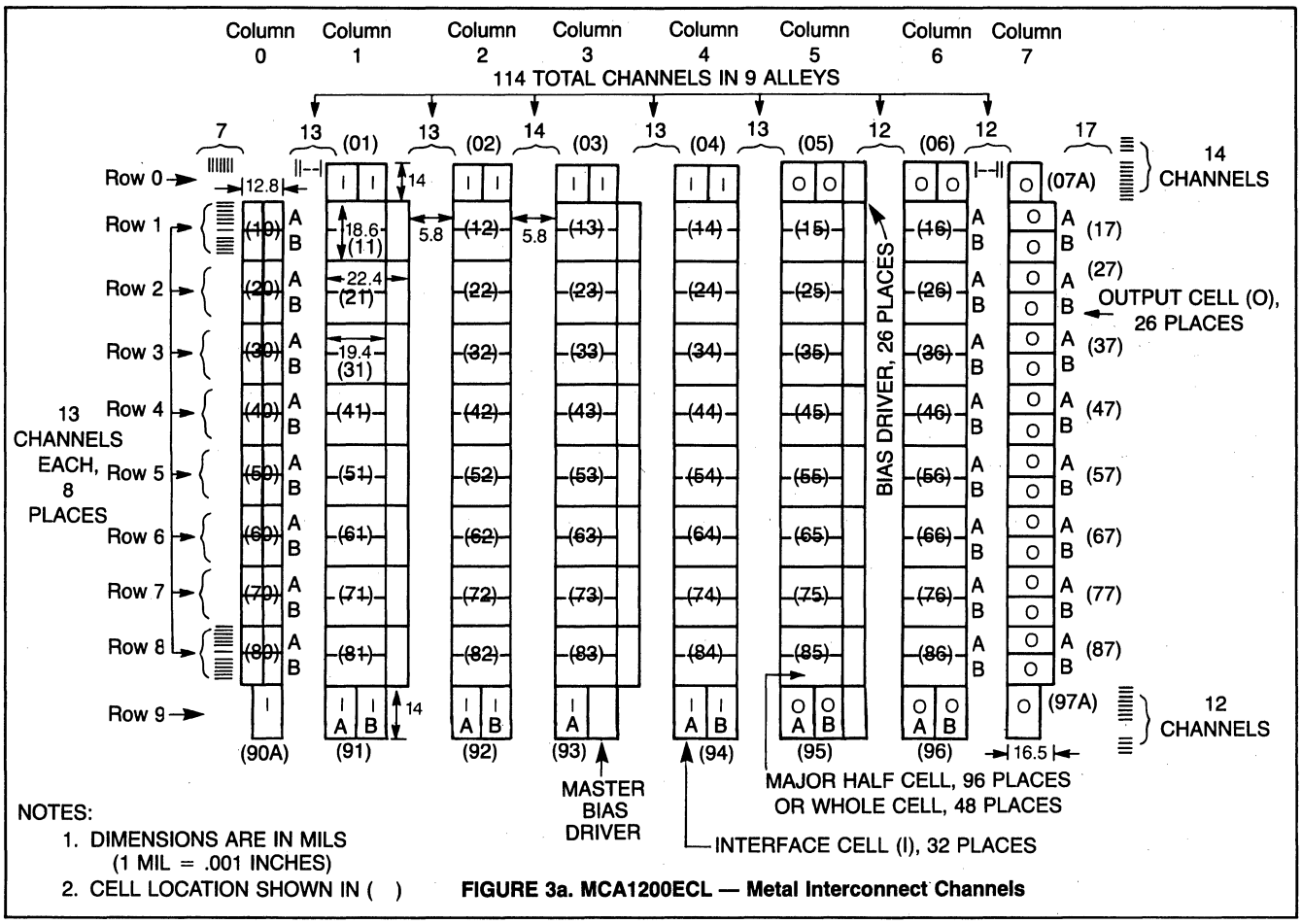


FIGURE 3a. MCA1200ECL — Metal Interconnect Channels

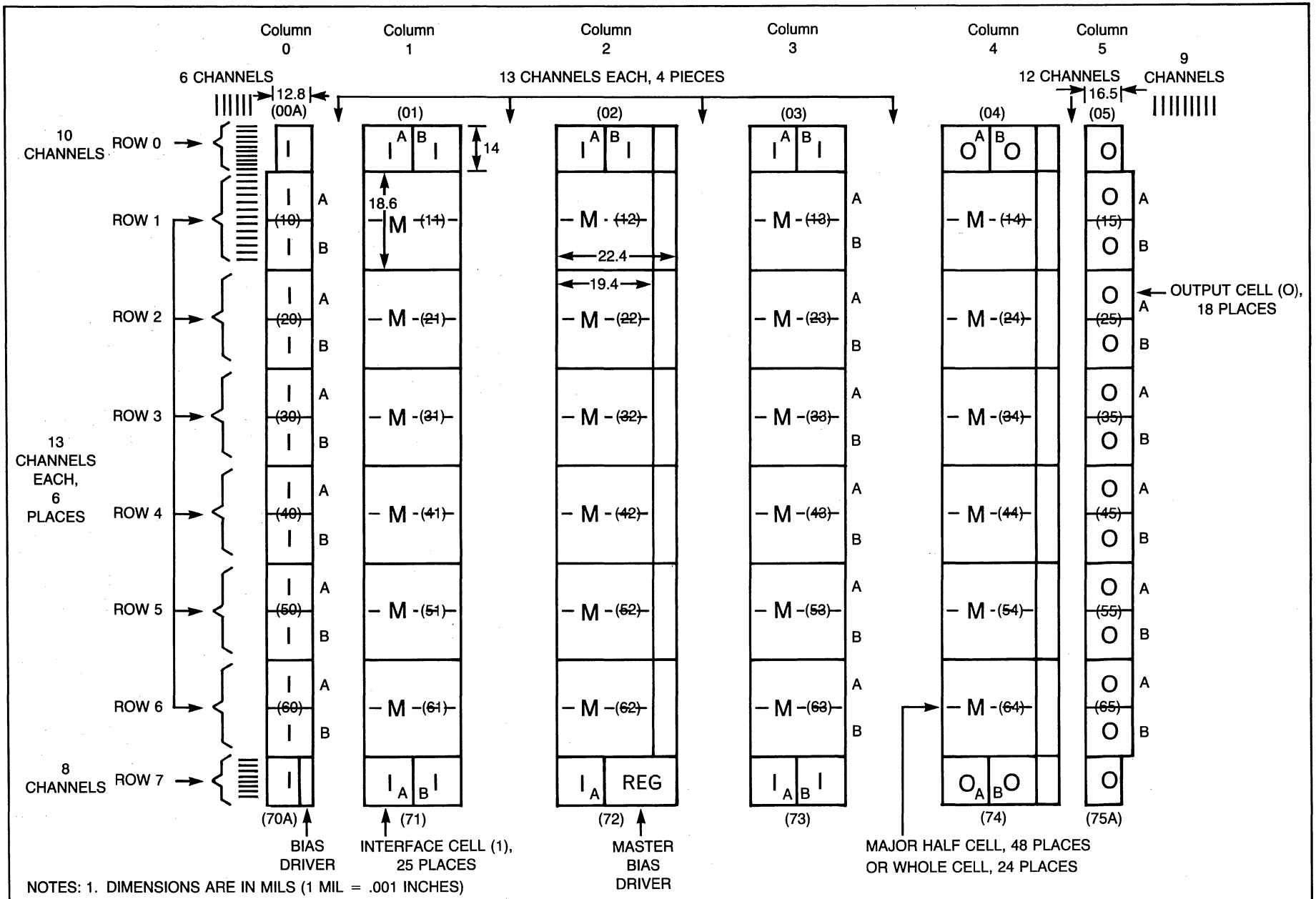
II. THE MACROCELL ARRAY PRODUCTS

There are two Macrocell Array (MCA) products available, that are compatible with the MECL 10,000 logic family, utilizing the MOSAIC I process. They have part numbers of MCA1200ECL and MCA600ECL. The MCA1200ECL has approximately 1192 equivalent gates, while the MCA600ECL has approximately 652 equivalent gates when full adders and latches are used in all the cells.

The MCA1200ECL chip consists of a total of 106 cells, organized as shown in Figure 3a. There are 48 major cells (M) or 96 half cells (H), 32 interface cells (I), and 26 output cells (0). The MCA600ECL chip contains 24 major cells (M) or 48 half cells (H), 25 interface cells (I), and 18 output cells (O) as shown in Figure 3b. Each cell contains a fixed array of unconnected transistors and resistors, and all marocell array chips are built from a standard semiconductor diffusion set. That is, all chips are identical, and can be prefabricated up to metallization step. The Macrocell Design Library, page 54, contains more than 100 logic functions called macros. A macro (sometimes called macrocell) is a first layer metal intraconnection pattern that interconnects the components (transistors and resistors) of a cell into a specific logic function. The CAD system contains the required first layer metallization pattern for each macro as well as the I/O ports.

Each major cell can be divided into two independent half cells, an upper half and a lower half. As an example, the upper half of a major cell could be designated a D flip-flop (H31 in the Macrocell library) and the lower half a full adder (H52).

The power, ground, and bias supply lines are not shown in Figure 3a. These inter-connects are automatically accomplished by the CAD system. The illustration shows only the free channels that are used by the designer to interconnect the cells in the array. The channels in the vertical direction are accomplished on first layer metal while the channels in the horizontal direction are accomplished on second layer metal. Note that the second layer metal can be placed over the cell without interfering with the macro in that cell since all macros are intraconnected on first layer metal. The second layer metal is separated from the first layer by an oxide isolation. Metal runs on the chip have little effect on delay times because of the oxide isolation between metal and active devices. Connections between 1st layer and 2nd layer metal are accomplished with VIA s. The interconnecting of cells on the array



NOTES: 1. DIMENSIONS ARE IN MILS (1 MIL = .001 INCHES)
2. CELL LOCATION SHOWN IN ( )

FIGURE 3b. MCA600ECL — Metal Interconnect Channels

can be compared to routing signal lines on a two-sided PC board.

The important features of the array are listed in Table 1. The MCA1200 array could contain up to 1192 equivalent gates if all the major cells contain dual full adders, H52 (a total of 96 adders at 10 gates per adder), and the interface and output cells contain latches, I14 and 014 (a total of 58 latches at four gates per latch). The number of equivalent gates for each macro can be found by counting the number of gates given in the macro-cell design library. Note that a 2-input exclusive OR gate is counted as three gates. If dual flip-flops, H31, were used in all the major cells (a total of 96 flip-flops at seven gates per flip-flop) instead of full adders, the array would contain 904 equivalent gates. The application example for an 8 x 8 2's complement multiplier (page 36), contains 888 equivalent gates with a 93% cell utilization.

Although the chips are large, good yields are experienced since most of the chip is composed of metal for interconnecting the macros. The total emitter area of the active device is the primary concern in determining the yield.

The macrocell array is voltage compensated for a ±10% tolerance of V_{EE}. Thus, a system designed with the macrocell array can operate with a V_{EE} of −4.68 volts resulting in approximately 10% less power at the same performance.

The maximum operating junction temperature is specified at 130°C with the package capable of dissipating 5 watts of power. A recommended heat sink and 1000 lfpm of air flow result in a thermal resistance, ΘJA, of only 10°C/Watt for MCA1200 in a 68-pin leadless package. The ambient temperature range is 0°C to 70°C.

The MCA600ECL requires only 500lfpm of air flow with no heat sink. This results in a typical ΘJ_A of 22°C/watt for all three package types (28, 40, and 68 pin packages).

TABLE 1 — — Basic Macrocell Array Features

1. *106 total cells for MCA1200, 67 total cells for MCA600.*
2. *Up to 1192 equivalent gates if Full adders and latches are used in all the cells for MCA1200, 652 gates for MCA600.*
3. *Up to 904 equivalent gates if flip-flops and latches are used in all the cells for MCA1200, 508 gates for MCA600.*
4. *Die size — 221 x 252 mils for MCA1200, 174 x 185 mils for MCA600.*
5. *Power Dissipation — 4.0 watts typical for MCA1200, 2.2 watts typical for MCA600.*
6. *4.4 mW per equivalent gate (for 904 gates and 4.0 watts).*
7. *Interface cell delay — 0.7 to 1.3 typ (1.05 to 1.7 ns max).*
8. *Major cell delay — 0.7 to 1.8 ns typ (1.05 to 2.35 ns max).*
9. *Output cell delay — 1.5 to 2.5 typ (2.8 to 3.8 ns max).*
10. *8 output cells can drive a 25 ohm load.*
11. *All output cells can drive 50 ohm loads.*
12. *Edge speed — 1.5 ns typ 20 to 80% (1.0 ns min).*
13. *Ambient temperature range (with heat sink and 1000 lfpm air flow for MCA1200, 500 lfpm from MCA600) = 0°C to 70°C.*
14. *ΘJA = 10°C/W with heatsink and 1000 lfpm air flow for MCA1200 in a 68 pin leadless package.*
15. *Maximum operating junction temperature, T_J = 130°C.*
16. *Voltage compensated, V_{EE} = −5.2 volts ±10%.*
17. *Interfaces with both MECL 10K and 10KH*

III. MACROCELL DESCRIPTION

A. Major Cells

The Major Cells in the array comprise the internal area on the chip and are used for the majority of the logic capability. Each Major Cell contains 52 transistors and 48 resistors as shown in Figure 4. These components are connected together on first layer metal to form logic functions with four series-gated structures. Figure 5 illustrates the interconnection of the components to form a 4-input Exclusive OR gate (H11). The maximum propagation delay, tpd, from the A or C input to the Y output is 1.2 ns. This value is for a 1.0 mA output-follower current (R8) with the output driving a fan-out of 1. Similarly, the maximum propagation delay, tpd*, from the B or D input to the Y output is 1.65 ns (tpd-*). The asterisk at the B and D input denotes that

each input is connected to an input follower which connects to the lower level of the series-gated current tree. The "-" in tpd-* refers to the output following edge delay.

The output follower current (through R8) can be selected by the designer for 0, 0.5, 1.0, or 2.0 mA if two outputs or less are used per half cell. If four outputs per half cell are used, the current can be selected for 0, 0.5, or 1.0 mA. A 1.0 mA current should be selected if the output is driving a fan-in of 3 or less . A 2.0 mA current should be selected for a higher number of fan-ins (>3) in order to minimize propagation delay degradation. A 0.5 mA current should be used, in order to save power, if the delay path is not critical.

The typical power dissipation, P_D, specified in the Macrocell library does not include the output follower current since different values can be specified. The power dissipation of the output follower can be calculated by multiplying 5.2 volts times the output follower current.

Outputs of a Major Cell macro can only drive inputs of other macros within the array. The current source for each current tree (in Figure 5) is 1 mA, which is formed by Q17 and R6, and Q16 and R7. The bias voltages are $V_{BB} = -1.3$ volts, $V_{BB} = -2.1$ volts, and Vcs $= -4.0$ volts typically. The 26 slave bias drivers are shown next to the major cells in three different columns in Figure 3a while the master bias driver cell is shown at the bottom of the array. Vcs tracks with V_{EE} to maintain a constant current in the current source.

The input followers, Q11 and Q14, each have an emitter current of 0.5 mA average for the input at B or D in the high or low state. The input follower current is about 10% higher when the input is in the high state and about 10% lower when the input is in the low state.

The logic power of series gating can be easily shown in Figure 5. Collector dotting in the top of the current tree (such as collectors Q3, Q5, Q8, and Q10) forms a wired AND logic function. Transistors Q1 and Q2 are used to clamp the voltage at the bases of Q19 and Q20 when more than 1.0 mA must be supplied through resistors R2 and R3. When collectors of two different current trees are tied together, a clamp transistor is provided in order to maintain a proper "low" level at the output. Collector dotting is allowed only within the cell since any capacitance at the collectors will degrade propagation delays appreciably.

Emitter dotting of output transistors forms a wired-OR logic function. The number in parenthesis at the logic output indicates the number of internal wire OR's. For the 4 input exclusive OR gate, there are two internal wire OR's.

The value of series-gating can be seen by the logic equation for the 4-input exclusive OR gate shown in

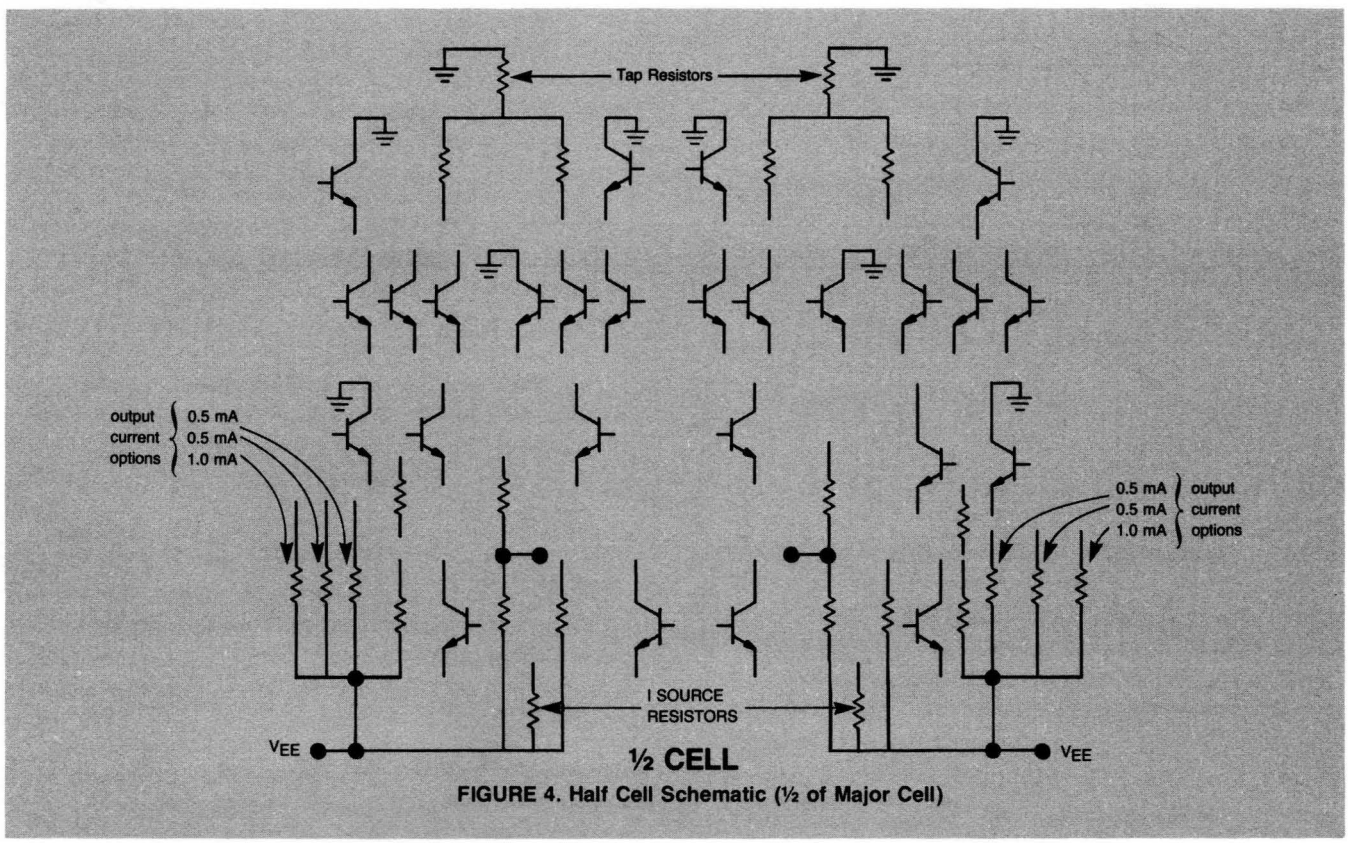


FIGURE 4. Half Cell Schematic (½ of Major Cell)

Figure 5. To implement this function with gates would require eight 4-input AND gates plus one 8-input OR gate. Gates also might be required to form the true and complement of each input. About 40 connections would be required if gates were used, compared to five connections for the series-gated macro.

The fan-in for each input when greater than one is also specified in the macrocell design library. For the circuit shown in Figure 5, the dc fan-in of all inputs is 1 even though some inputs go to more than one base. When an input goes to two different bases at the top of one current tree, the dc fan-in is considered to be 1. The reason is that the input driving the two bases has to switch a maximum of 1.0 mA since only 1.0 mA can flow into the current source Q17. If an input is connected to two different current trees (two series-gated structures), then the dc fan-in is specified as 2.

Inputs of Major Cell macros that are marked with an asterisk (with no circle around it) are not allowed to be connected to package pins or to the Y1 output of an Output Cell macro due to potential saturation problems.

B. Interface Cells

The Interface Cells are located around the left half periphery of the array. In addition to input buffering, the Interface Cell provides about one-fourth the logic capability of the Major Cell. These cells can be utilized for input interfacing and to provide extra logic power within the array.

Interface Cell macro outputs (as well as Major Cell macro outputs) can only be connected to internal macro inputs. These outputs do not have enough drive capability to drive signals off the chip. Only outputs from Output Cell macros can drive 50 ohm or 25 ohm loads.

Each Interface Cell contains 17 transistors and 14 resistors as shown in Figure 6. These components are connected together on first layer metal to form logic functions with one full series-gated structure. Two partial series-gated structures can be formed in one cell for dual gate macro functions. The Interface Cell Library lists the macros and their characteristics.

Figure 7 illustrates the interconnection of the components to form a latch. The maximum propagation delay, tpd, from the D input to the Q or $\overline{Q}$ output is 1.2 ns, while the delay, t_{pd+}*, from the E1 or E2 input to the Q or $\overline{Q}$ is 1.7 ns. These values are for a 1.0 mA output follower current (at R6 and R7) driving a fan-out of 1. The asterisk at the E1 and E2 input denotes they are connected to an input follower which connects to the lower portion of the series-gated current tree. The current source is 1.0 mA which is formed by Q15 and R10. The bias voltages are the same as the Major Cells.

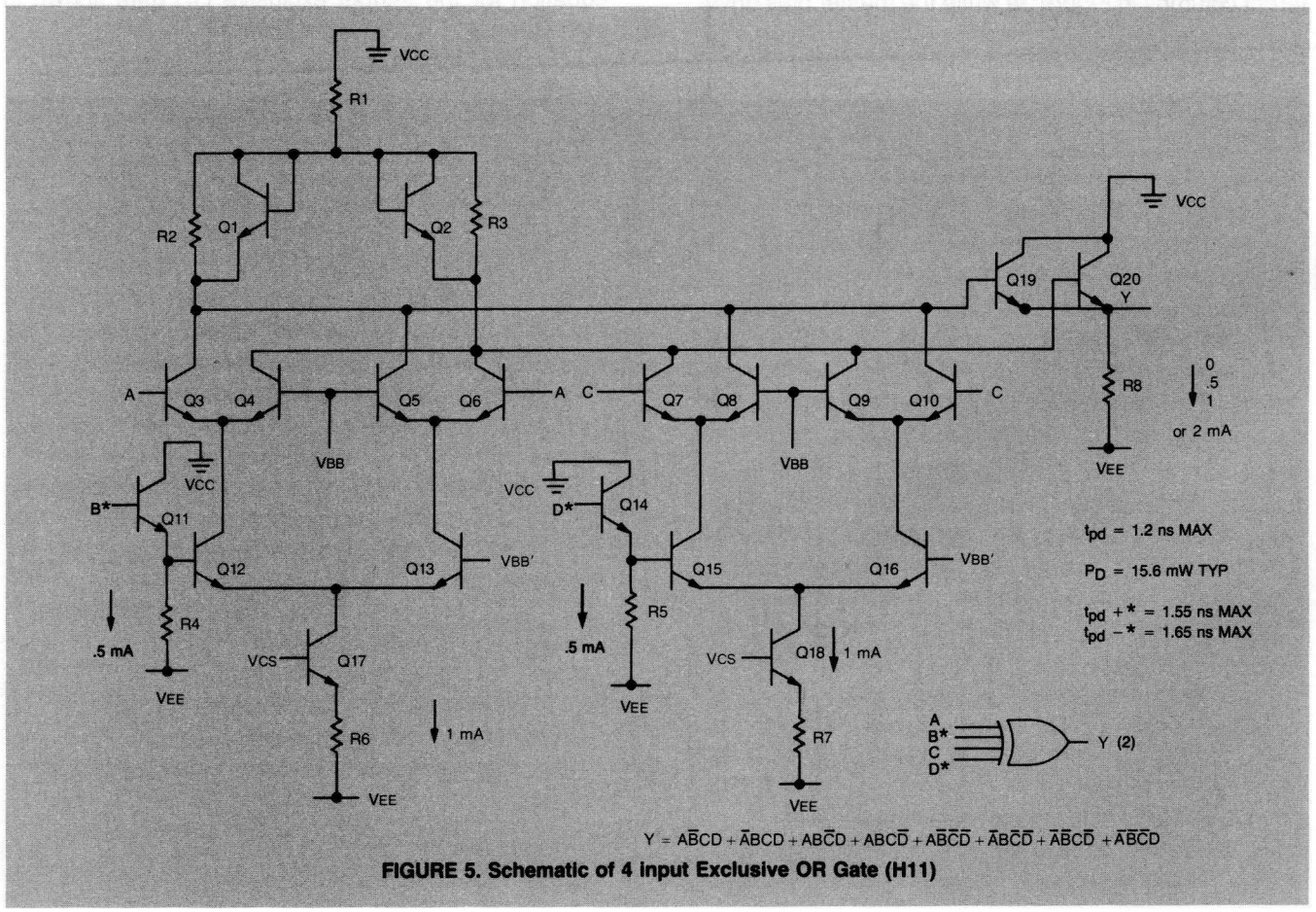


FIGURE 5. Schematic of 4 input Exclusive OR Gate (H11)

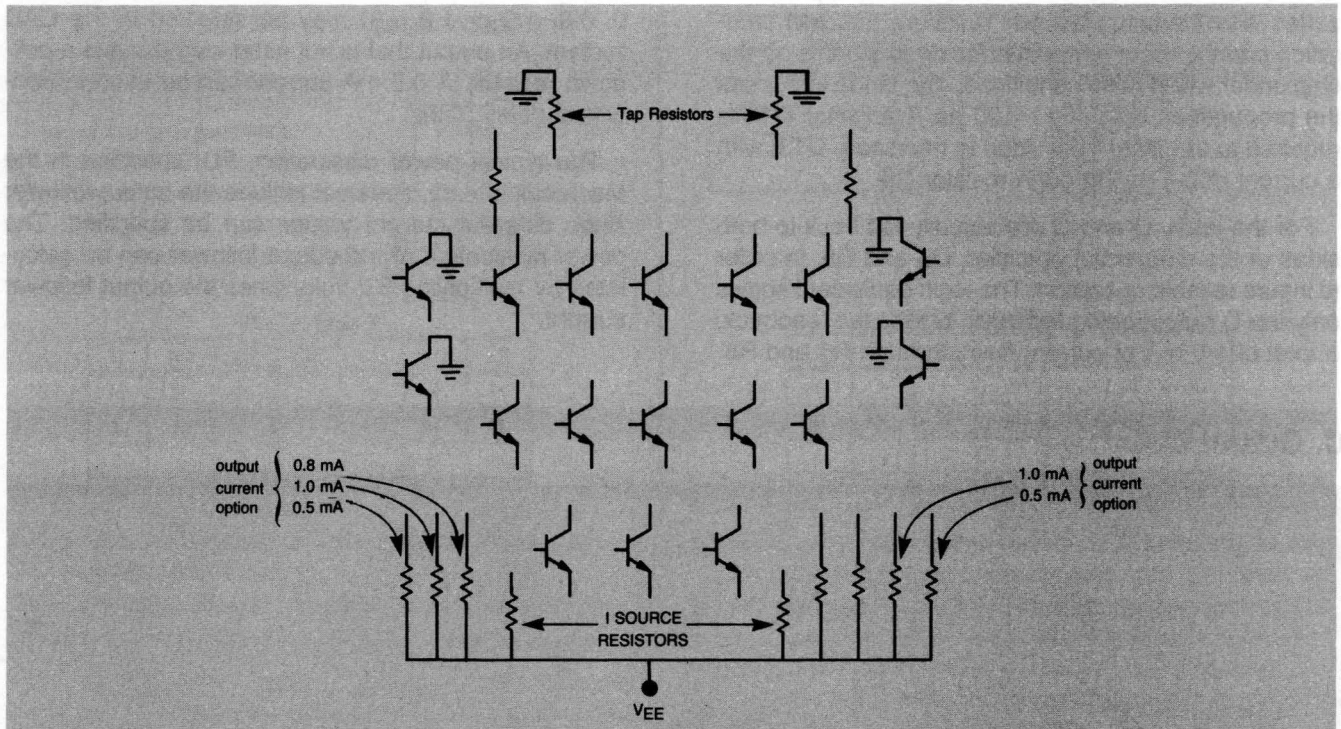
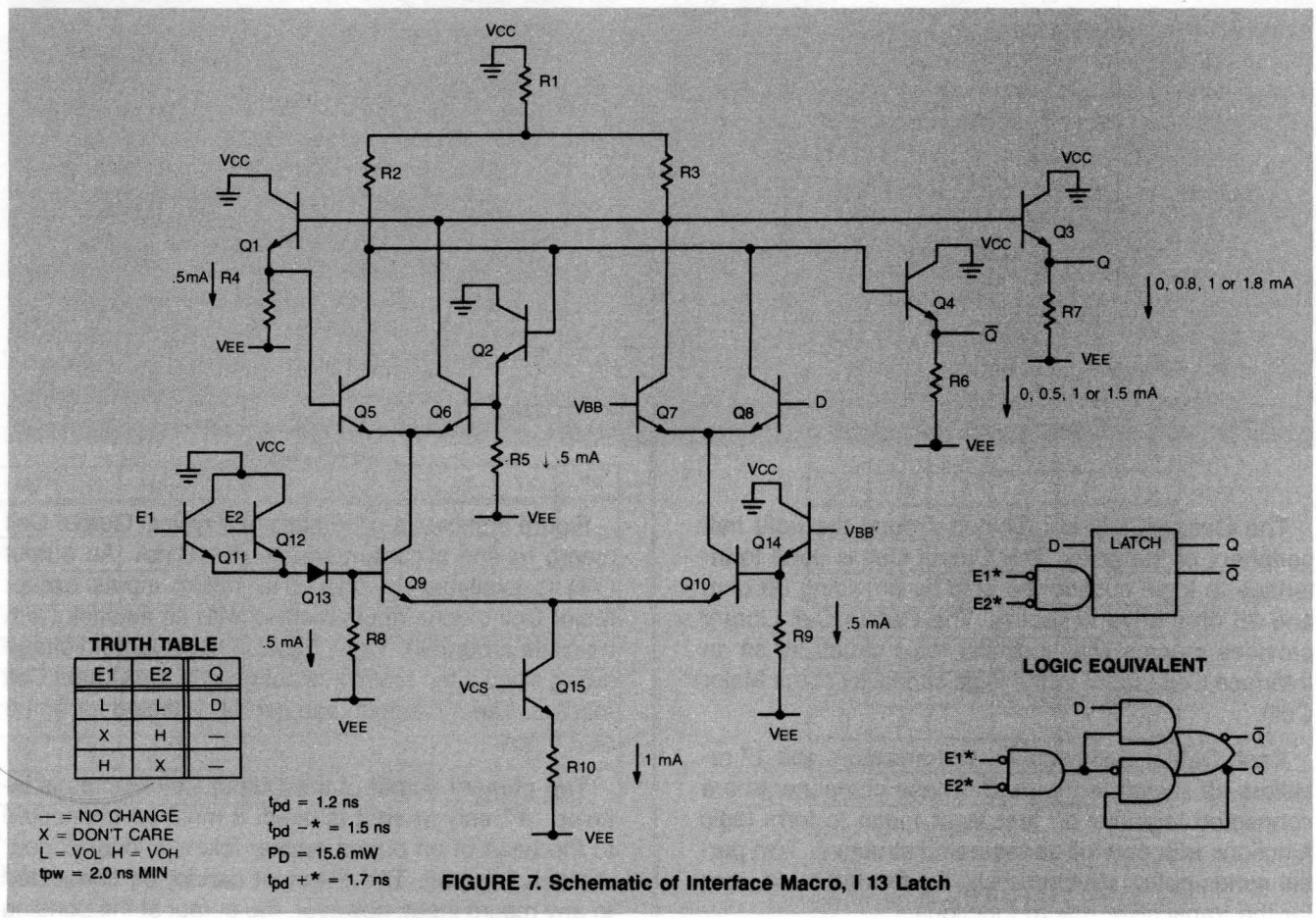


FIGURE 6. Interface Cell Schematic



E1	E2	Q
L	L	D
X	H	—
H	X	—

FIGURE 7. Schematic of Interface Macro, I 13 Latch

The input followers, Q11 and Q12, have an input follower current of 0.5 mA. A diode, Q13, is placed in series with the input follower to insure that soft saturation cannot occur when interfacing to signals off the chip under worst-case conditions. The diode increases the propagation delay by ~100 ps. Transistor Q14 is required to translate VBB′ (due to the diode, Q13) with a current of 0.5 mA through resistor R9.

For the latch, Q and $\overline{Q}$ are actually fed back to both sides of the differential amplifier, Q5 and Q6, in order to insure reliable operation. The logic equivalent shows only the Q output being fed back. Due to the feedback, a total of 1.0 mA of current flows through R4 and R5.

An output follower current of 0, 0.5, 1 or 1.5 mA (except the Q output of I13 and I14 can be selected for 0, 0.8, 1.0 or 1.8 mA) may be selected in the CAD system. An output that is not used will not have a pull-down resistor. A 0.5 mA current can be used in non-critical delay paths.

The typical power dissipation, PD, specified in the Macrocell Library, does not include the output follower since different current values can be specified. The power dissipation of the output follower can be calculated by multiplying 5.2 volts times the output follower current.

C. Output Cells

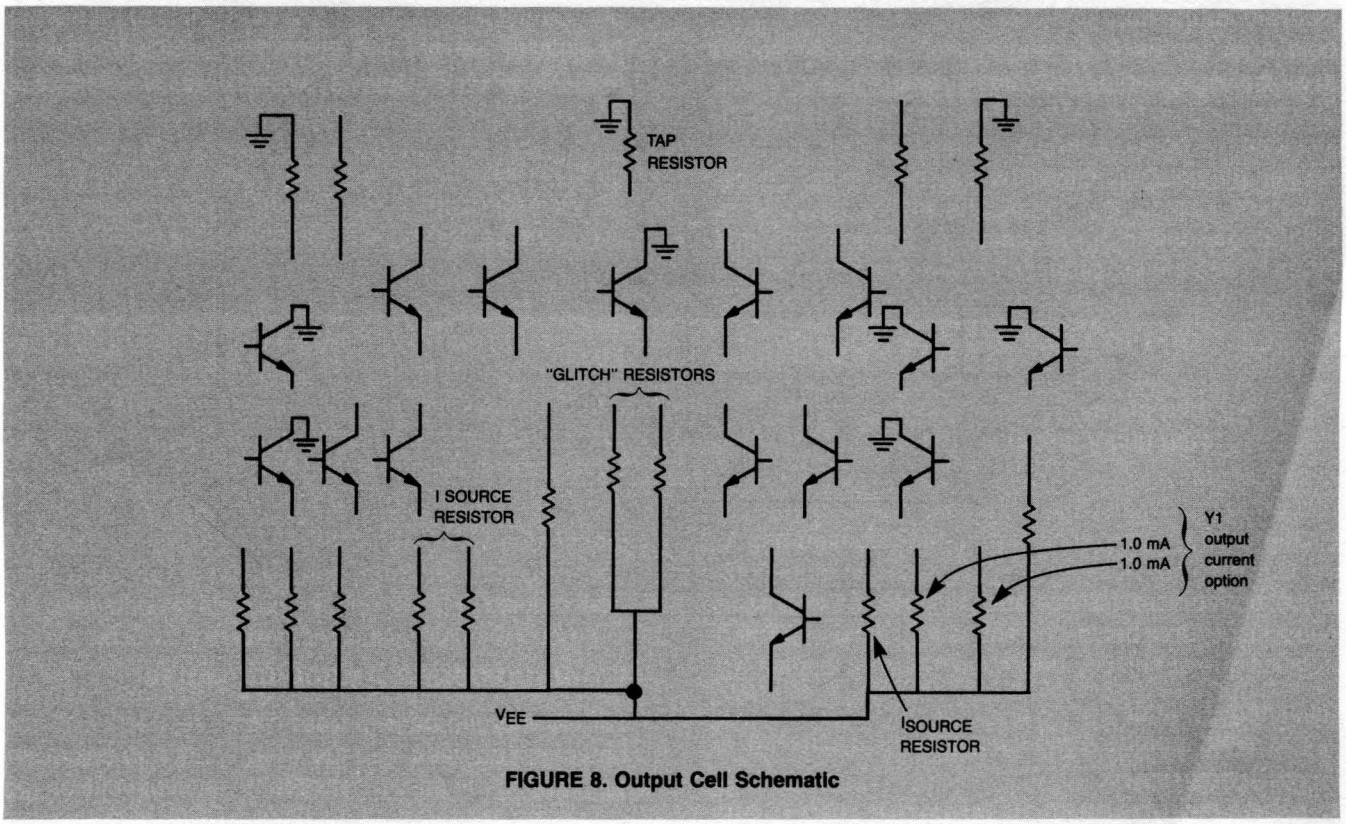


FIGURE 8. Output Cell Schematic

The Output Cells are located around the right half periphery of the array. The Output Cell is used to interface to logic outside the chip by providing 50 ohm and 25 ohm drive capability. The Output Cell Library provides macros with a similar logic capability as an Interface Cell (about ¼ the logic capability of the Major Cell).

Each Output Cell contains 15 transistors and 17 resistors as shown in Figure 8. These components are connected together on first layer metal to form logic functions with one full series-gated structure. Two partial series-gated structures can be formed in one cell for the transceiver macro functions.

Figure 9 shows a schematic of a typical Output Cell macro having a current source of 3.5 mA. An output (Y1) is available for driving all macro inputs except Major Cell macro inputs marked with an asterisk (with no circle around it). The Y1 output has a larger voltage swing since a tap resistor is not used in the Output Cell macros. The Y1 output load can be selected for 0, 1.0 or 2.0 mA.

The primary output of the Output Cell macros is labeled "Y" and when it is used, it must be connected to the base of an output emitter follower located near the bonding pad. The Y output cannot be connected to any macro input; however, the output at the bonding

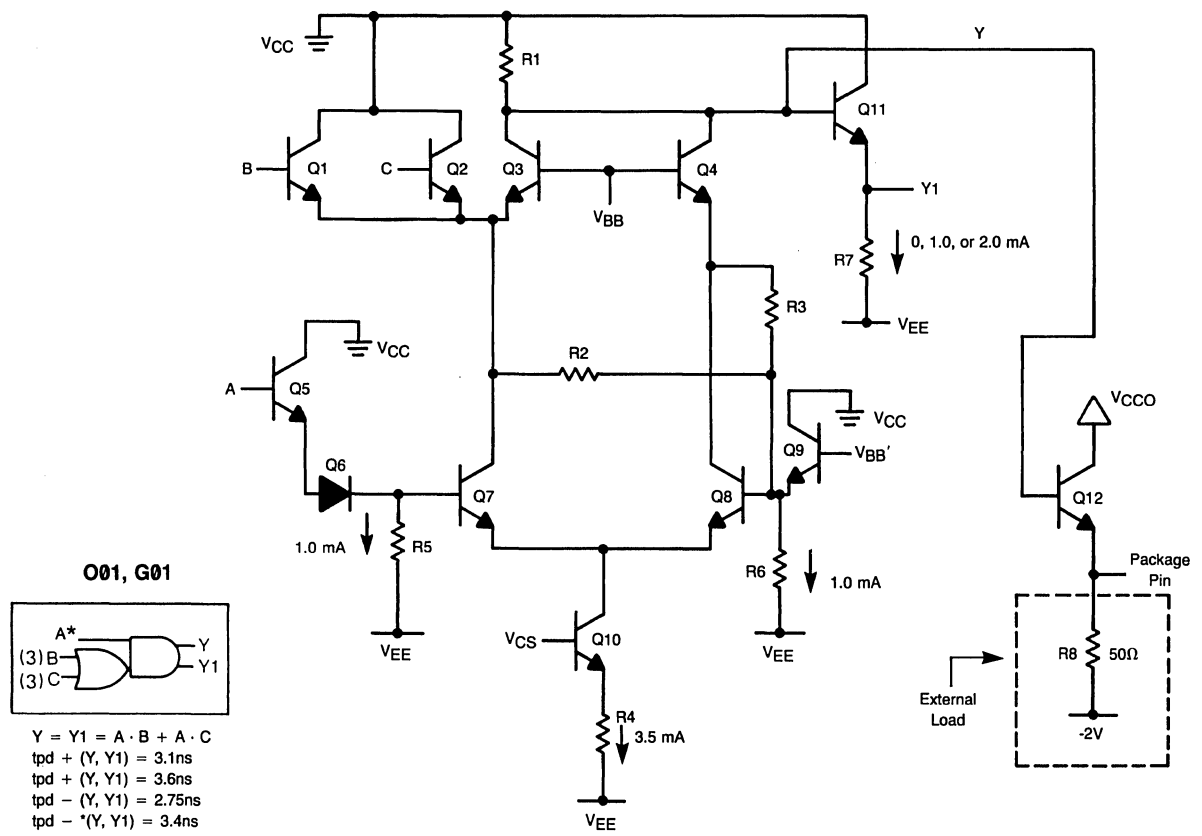


FIGURE 9. Schematic of Output Cell, O01-OR-AND gate.

pad can be connected to all macro inputs except Major Cell macro inputs marked with an asterisk (with no circle around it).

The O16 and O17 drivers are capable of driving 50 ohms to −2 volts with the V_{OL} state in the cutoff mode (V_{OL} max = −1.95 volts). 024 and 025 are drivers that are capable of driving 25 ohms to -2.0 volts. The current source for the 25 ohm driver is 10.5 mA versus 7.0 mA for the O16 driver. The Y output of the 25 ohm driver must be routed to pins that have two output emitter follower (OEF) transistors (the Y output is connected to the base of both transistors). Table 8, (page 51) shows the pins having two OEF transistors.

In Figure 9, note that a diode, Q6, is connected in series with the input follower at the "A" input in order to insure that soft saturation cannot occur when interfacing to signals off the chip.

Resistors R2 and R3 in Figure 9 are used in all Output Cell macros having a series gated structure. A small current flows through these resistors to insure that there are no floating nodes and therefore minimizes switching noise when switching the lower portion of the current tree (input A).

Figure 10 shows a schematic of the Transceiver Macro O16. The current source for the driver is 7 mA and the input follower is 1.3 mA. A diode is not placed in series with the input follower of the driver since it is not a series-gated function and soft saturation cannot occur. The output transistor Q6 is located near the bonding pad and not in the Output Cell. When the Y output of the cell is connected to the bonding pad via the CAD system, the collector of Q4 is actually routed to the base of Q6 with the emitter connected to the bonding pad. The load resistor, R4, is placed outside the package. For the receiver, the current source is 3.5 mA. The output emitter follower current of the receiver can be selected for 0, 1, or 2.0 mA. Note that the Z output of the receiver can drive any macro input since the output has a reduced logic swing due to the Tap resistor, R8.

The fan-in for the output macros is shown in parenthesis in the Macrocell Library. Normally, the fan-in is 3 for the upper tree input and 1 for the lower tree input. An exception is the inputs of the driver where the fan-in is 2.

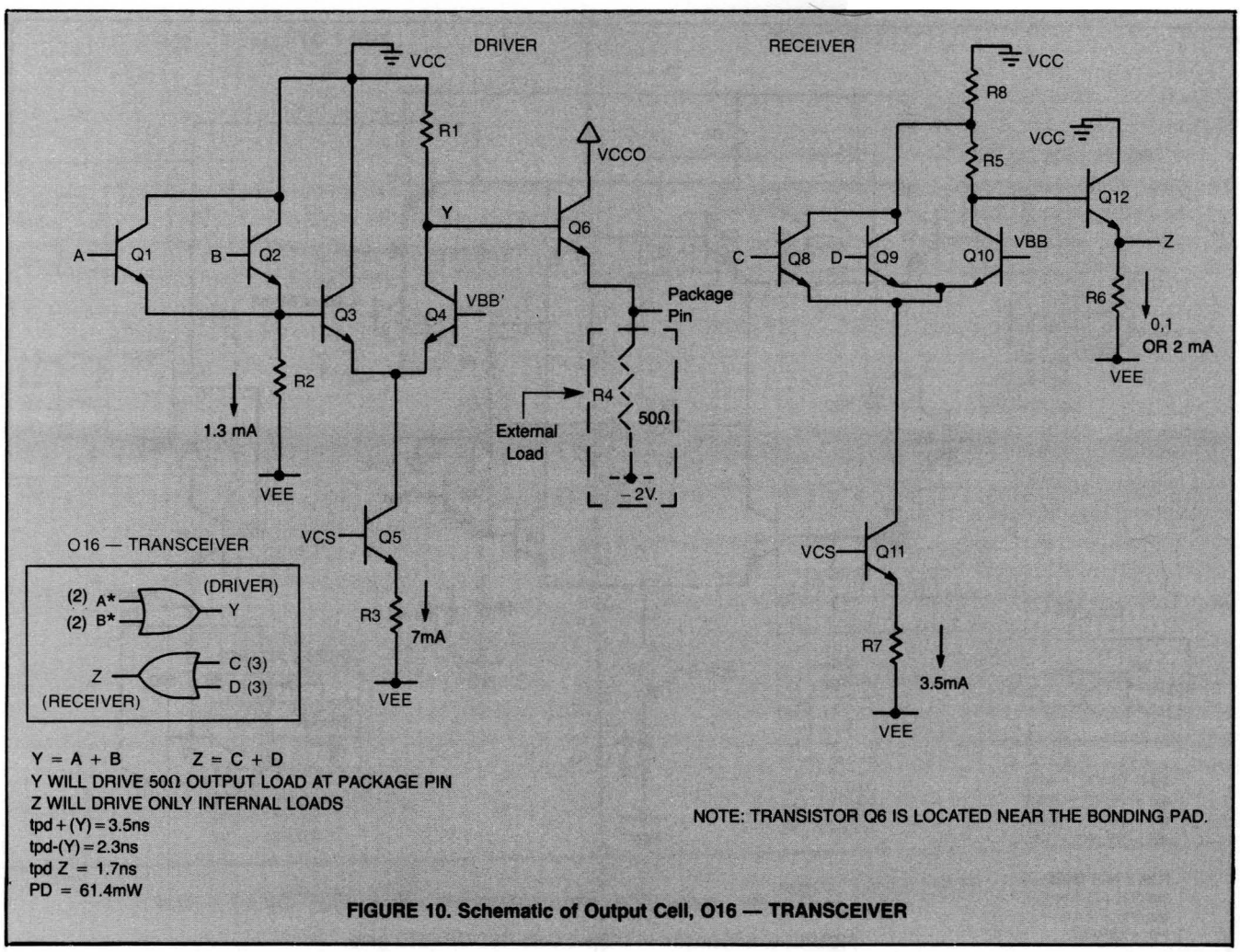


FIGURE 10. Schematic of Output Cell, O16 — TRANSCEIVER

IV. LOGIC DESIGN CONSIDERATIONS

This manual contains all the information necessary to transform a system into logic designs utilizing the Macrocell Array. The performance of the design can also be estimated since worst case delays are also included.

The first step in the design process is to partition the system into blocks of logic. The number of I/O pins and the amount of logic in each block should be organized in order to determine the number of options required to implement the system. The ratio of the number of pins to the amount of logic required in each block will help in determining whether to use the MCA1200, the MCA600, or a combination of the two arrays.

A. Pinouts

The pin assignments for the 68-pin leadless and 72-pin Grid-Array packages are illustrated in Figure 11 for the MCA1200 and the MCA600. Two leadless options are available for the MCA1200. One option uses four V_{CCO} pins, while the other option requires eight V_{CCO} pins in order to reduce noise due to outputs switching simultaneously. (See section on Simultaneous Switching Noise for more details.) The ground for the output followers of the Output cells (V_{CCO}) is separated from the ground for the rest of the logic (V_{CC}). The current supplied to V_{CC} is rather constant while the current supplied to V_{CCO} changes when outputs are switching. The V_{CC} and V_{CCO} pins should be connected together to a good ground outside the package, similar to normal MECL 10K grounding.

The signal pins are divided into two types: 1) I for input only, and 2) I/O for input or output, or both. The MCA600 can also be packaged in a 28-pin or 40-pin DIL ceramic package as shown in Figure 12. Pins having two transistors for 25 ohm outputs are listed in Table 8, page 51.

(a) MCA1200 ECL

48 M CELLS
32 I CELLS
26 O CELLS

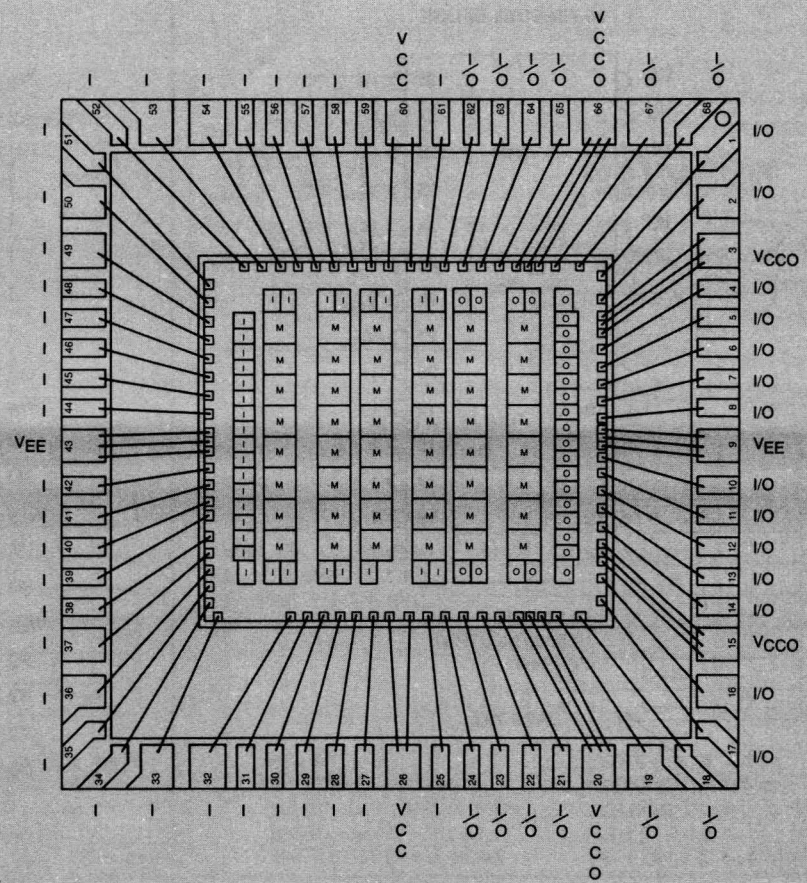
8 POWER PINS
34 INPUT PINS
26 INPUT/OUTPUT PINS

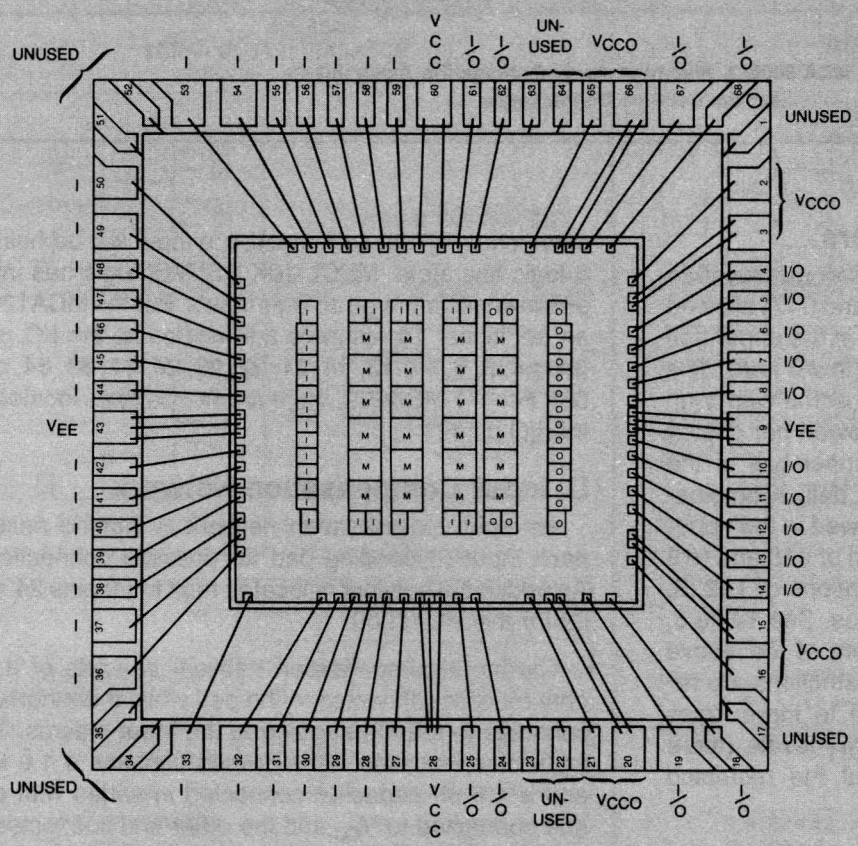
4 EXTRA V_{CCO} PIN OPTION IN 68-PIN LEADLESS PACKAGE (CASE 745B)

12 POWER PINS
32 INPUT PINS
24 INPUT/OUTPUT PINS
4 EXTRA V_{CCO} PINS ARE 7,11,25,61

(b) MCA600ECL

12 POWER PINS
28 INPUT
18 INPUT/OUTPUT
24 M CELLS
25 I CELLS
18 O CELLS





(c) 72-PIN GRID-ARRAY
(MCA600ECL and MCA1200ECL)
See Figure 25 for ZONE locations

PIN LOCATION

PIN	ZONE	PIN	ZONE	PIN	ZONE
1	B1	25	K5	49	C11
2	B2	26	L6	50	C10
3	C1	27	K6	51	B11
4	C2	28	L7	52	A10
5	D1	29	K7	53	B10
6	D2	30	L8	54	A9
7	E1	31	K8	55	B9
8	E2	32	L9	56	A8
9	F1	33	K9	57	B8
10	F2	34	L10	58	A7
11	G1	35	K11	59	B7
12	G2	36	K10	60	A6
13	H1	37	J11	61	B6
14	H2	38	J10	62	A5
15	J1	39	H11	63	B5
16	J2	40	H10	64	A4
17	K1	41	G11	65	B4
18	L2	42	G10	66	A3
19	K2	43	F11	67	B3
20	L3	44	F10	68	A2
21	K3	45	E11	69	A1
22	L4	46	E10	70	L1
23	K4	47	D11	71	L11
24	L5	48	D10	72	A11

NOTE: The 72-Pin Grid-Array package provides 4 additional V_{CCO} pins #69, 70, 71, 72 which connect to V_{CCO} Pins 3, 15, 20, and 66 on a buried layer ground plane.

FIGURE 11. Pin Assignments for 68-Pin Leadless and 72-Pin Grid-Array Packages

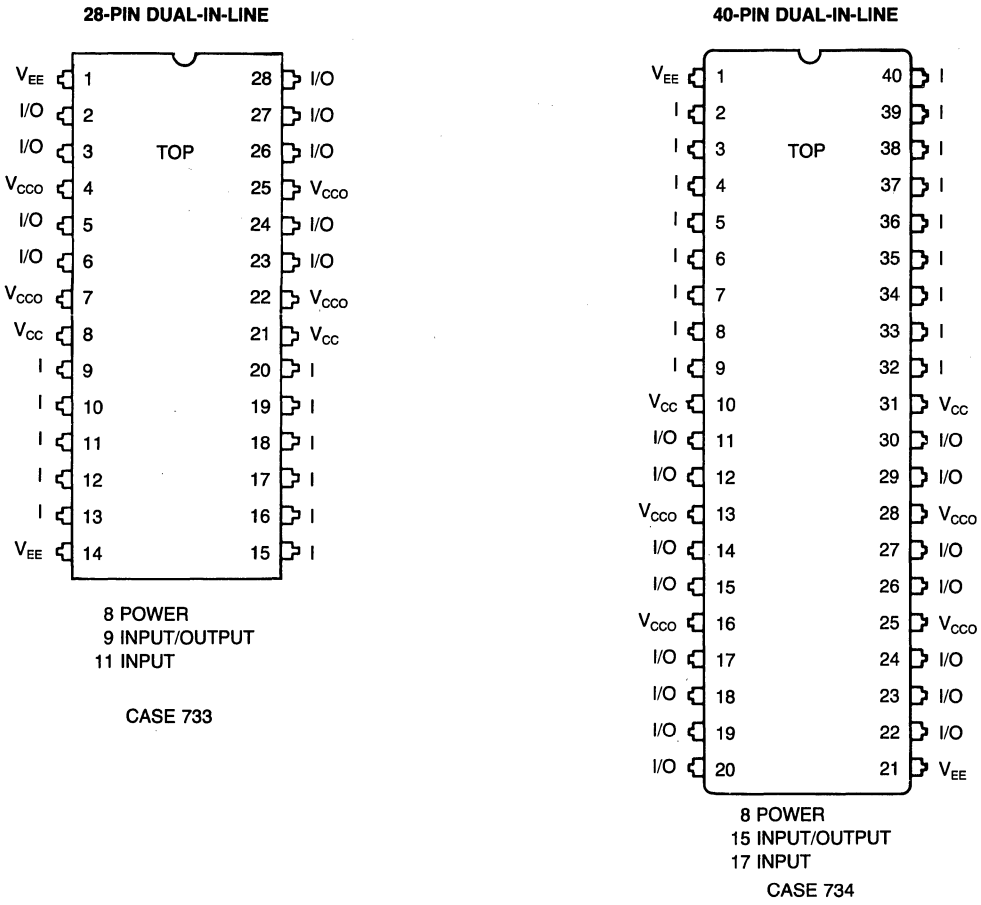


FIGURE 12. MCA 600ECL Macrocell Array Package Pin Assignments for the Ceramic Dil Packages

B. Maximum Number of Drivers

The maximum number of 25 ohm driver macros (024 and 025) or transceiver macros (016 and 017) allowed per design option is 10 (five maximum in the upper half of the array and five maximum in the lower half). The maximum number of 50 ohm driver macros with V_{OL} in the cut-off mode (018 and 019) allowed per design option is 18 (nine maximum in the upper half of the array and nine maximum in the lower half). Combination of the two above macro types allowed in the upper or lower half are 7, 5, 3, or 1 maximum of 018 and 019 when mixed respectively with combinations of 1, 2, 3, or 4 25 ohm driver or tranceiver macros. See Table 8, page 51 for details on CAD placement of the above mentioned output cell macros. The restrictions are required since these macros draw two to three times more current thus causing lower V_{OH} levels (more negative) due to large V_{CC} drops at the restricted locations.

C. Input Pulldown Resistors

An optional input pull-down resistor ($\approx$ 50 k Ω) is located near each input (I) bonding pad for possible connection. When connected, the input will be held in a logic low state. MECL 10K SSI/MSI logic has input pulldown resistors on all logic inputs. For the MCA1200, an additional 14 resistors are located at the I/O pins (pins 4, 5, 6, 12, 13, 14, 21, 22, 23, 24, 62, 63, 64, and 65). For the MCA600, there are no resistors located at the I/O pins.

D. Input Compensation Network

An input compensation network is located next to each input (I) bonding pad for possible connections. An additional network is located next to I/0 pins 24 and 62 for the MCA1200.

The input compensation network consists of a 75 ohm resistor connected to the pad while the other side connects to the metal going to the input macros. The input compensation network also contains a 1.0 k Ω and a 1.3 pF capacitor connected in series with one end connected to V_{CC} and the other end connected to the 75 ohm resistor on the side going to the input macros. The input compensation network should be connected to the bonding pad if it is also connected to an

input follower (input marked with * for Inputs and Output Cell macros and ⊛ for Major Cell macros in Macrocell Library). Note that * or ⊛ inputs do not require compensation networks when driven from an internal source. The compensation network insures that the real portion of the input impedance at the input pin will be positive. If the input pin goes to upper level inputs (inputs not having a *), a compensation network is not required since these inputs already have a positive real input impedance. The real portion of the input impedance does not normally go more negative than −10 ohms. In a transmission line environment, oscillation problems are minimized since the impedance of the driving circuitry is at least +10 ohms (with low inductance compared to nontransmission line environment). However, the compensation network should be used as indicated previously.

E. Maximum Input Fan-In at Package Pins

When the input compensation network is connected, the maximum fan-in is 10. When the input compensation network is not connected, the maximum fan-in is 30. The primary reason for the limitation is to minimize the high state noise margin reduction to less than 20 mV.

F. Package Pins Connected to Macro Inputs

All inputs of Interface and Output macros can be connected to package pins. For Major Cell macros, upper level inputs and lower level inputs marked with a circle around the asterisk (⊛) are allowed to be connected to package pins. Input of Major Cell macros marked with an asterisk (with no circle around it) are not allowed to be connected to package pins.

G. Package Pins Connected to Macro Outputs

It is not allowed to connect Interface or Major Cell macro outputs to package pins. Also, it is not allowed to connect the Y1 or Z output of an Output Cell macro to a package pin since these are used to drive internal loads. The Y output of an Output Cell macro can be connected to an I/O pin by connecting the Y output to the base of output emitter follower near the bonding pad.

H. Internal Connections

Outputs of Interface or Major Cell macros can be connected to any input of an Interface, Major, or Output Cell macro. For Output Cell macros, the Y1 output follows the same rules for package pins connected to macro inputs. The Y1 output can be connected to any input of an Interface or Output Cell macro. For Major Cell macros, upper level inputs and lower level inputs marked with a circle around the asterisk (⊛) are allowed to be connected to the Y1 output of the Output Cell macro.

The Y output of an Output Cell macro can only be connected to the output emitter follower near the bonding pad. The output at the bonding pad can be connected to macro inputs following the same rules for package pins connected to macro inputs.

I. Unused Inputs or Outputs

Unused outputs can be left floating unconnected. Unused inputs in the array will automatically be forced to a low voltage (logic "0") by the CAD system (the input base is shorted to the emitter). There are no special provisions for providing a high voltage (logic "1") on an unused input. A logic "1" can be generated using a spare inverter from an Interface or Major Cell.

J. Maximum Fan-out of Macro Outputs

The maximum fan-out should be limited to 15 due to ac delay considerations. The maximum dc fan-out is limited to 30 due to noise margin considerations.

For driving clock lines, it is recommended that the fan-out be limited to 10 or less with the driving gate having a 2.0 mA output follower current. For fan-outs of 5 or less, a 1.0 mA output follower current can be used, although a 2.0 mA current will result in better performance.

K. Wire ORing

Outputs of Interface Cell macros, Major Cell macros, and internal outputs (Y1, Z) of Output Cell macros can be tied together to form a wired OR function. The total number of wire OR's allowed per wired OR function is 8, which must include the macro internal wire OR's. The number of internal wire OR's for each macro output is shown in the Macro Cell Library. Table 3 (in the performance Section) lists the propagation delay degradation due to wire OR's.

Collector dotting of the Y output from Output Cell macros is not allowed. However, a wire OR of two outputs from two Output Cell macros can be accomplished by connecting the Y outputs to separate output emitter followers sharing a common output pin (see Table 8, page 51). A wire OR of two outputs on different output pins must be performed outside the package.

L. Designing Latches with Gates

When designing logic requiring latches, it is recommended that the designer use the latches and flip-flops in the library. As explained previously concerning the I13 latch (see Figure 7), the logic equivalent of the latch shows only the Q output being fed back. However, the actual circuit is implemented with Q and $\overline{Q}$ outputs fed back differentially to the input through separate emitter followers. This method eliminates race conditions caused by delay differences when switching the clock enable lines on the lower part of the current tree (*input). This insures reliable operations and superior noise margins compared to single-ended feedback.

The logic designer is *not allowed* to make latches out of gates in the MCA library using single-ended feed-

back as described below. As an example of a single-ended feedback latch, the 2 to 1 MUX (H41) can be made into a latch similar to the logic equivalent shown for I13. This could be accomplished by tying the Y output to the A1 input, using the A0 input as the data input, and using the SA input as a clock enable. Designing this type of latch is *not allowed.*

The logic designer is allowed to make a latch or flip-flop out of gates if double feedback is a part of the design. However, the gates must use macros with upper level inputs only (no *inputs) and the outputs of the gates must not contain internal or external wire ORing. An example of an allowed design is when using H01 to form a set/reset latch. The Z output is connected to the D input, the Y output is connected to the E input, A or B or C is the "set" input, and F or G is the "reset" input. Note that an indeterminate condition exists if the set and reset inputs are simultaneously switched from a high to low state. This is a normal condition for this type of flip-flop.

If a latch is needed with a number of data inputs, a latch in the library (such as H35) should be used with a gating function (such as M24) connected to the data input of the latch. If the designer needs a JK flip-flop, a $J\overline{K}$ flip-flop can be formed using ½ of an H41 and an H31. The flip-flop is made by connecting J to A0, $\overline{K}$ to A1, Q of H31 to SA of H41, and Y of H41 to D of H31. If the designer needs a D flip-flop using the Interface Cells, I13 and I14 latches can be used to form the function.

M. Power Limits for a Macrocell Design Option

For the MCA1200, the typical power per option must be between 2.0 and 4.5 watts. For the MCA600, the typical power per option must be between 1.0 and 3.0 watts. This power does not include the output emitter follower power of the Output Cells, or the bias driver power. The typical power per option is calculated by adding the typical power of all the macros (see Macrocell Library) used in the option plus the power of the output follower current selected for each macro output. The output follower power of the macro output is calculated by multiplying V_{EE} (−5.2 volts) times the selected output follower current.

N. Calculation of Min/Max Power Dissipation

The worst case power of a design option due to process variations can be calculated as follows:

1. Calculate, Pm, the total typical macro power.
2. Calculate, Pi, the total typical power of the output follower current selected for each macro output.
3. The typical bias driver power, Pb, for the MCA1200 is 327 mW and for the MCA600 is 230 mW.
4. Calculate, Po, the total average power dissipation of the output emitter follower transistor driven by the Output Cell macro (Y output). For 50 ohm terminations to −2 volts, the average power dissipation for the output transistor (not in the cutoff mode of −2.0 volts) is 15 mW. For the driver in the cutoff mode (V_{OL} = −2.0 volts), the power dissipation of the output transistor is 10 mW for a 50 ohm load and 20 mW for a 25 ohm load.

   Maximum Power = 1.25 (Pm + Pi + Pb) + Po

   Minimum Power = 0.75 (Pm + Pi + Pb) + Po

O. Voltage Levels

All input and output levels (including input thresholds) of the Macrocell Array are compatible with MECL 10K, MECL 10KH, MECL 10800, and MECL III families over the temperature range. In addition, the Macrocell Array is voltage-compensated so that it can be operated over a range of V_{EE} = −4.68 volts to −5.72 volts with little change in performance. The typical voltage tracking rates are:

1) ΔV_{OHV} = 10 mV/volt
2) ΔV_{BBV} = 20 mV/volt
3) ΔV_{OLV} = 60 mV/volt

The output levels and input thresholds are the same for devices that have the same ambient temperature with recommended heat sink and air flow even though the junction temperature of the devices can be different. This is partly accomplished in the design of the bias driver. The bias driver is designed to automatically adjust the bias voltages according to the current being drawn through the V_{CC} pin. If part A uses one watt (the junction temperature will be 35°C at 25°C ambient) and part B uses five watts (the junction temperature will be 75°C at 25°C ambient), the following voltages would result:

	PART A	PART B
V_{BB}	−1.2806	−1.2790
V_{BB}	−2.0639	−1.9701
V_{CS}	−3.9812	−4.0468
V_{OH}	−0.9296	−0.9146
V_{OL}	−1.7343	−1.7466

As can be seen above, the voltages remain fairly constant even though the difference in the junction temperature is large. These voltages also remain constant for two identical arrays from different lots. For instance, part B of lot 1 may dissipate 3.875 watts minimum and part B from lot 2 may draw 6.125 watts maximum.

In conclusion, the junction temperature differentials due to variations in IEE are taken care of as standard design practice in the design of every MECL device. The parametric voltage levels (such as V_{OHA}, V_{OLA}, V_{IHA}, and V_{ILA}) which specify noise margin are specified over temperature and include variations in IEE, θJA, and output power. These levels are specified for the Macrocell Array when using the recommended heat sink and air flow. See Section M of the Appendix (the MECL Macrocell Library) for table listing the DC specifications over temperature for the Macrocell Array.

P. Noise Margins

The worst-case noise margins guidelines (NM) for the Macrocell Array over temperature (0 to 70°C ambient) for a V_{EE} = −5.2 volts are NMhigh = 125 mV, NMlow = 155 mV. These values assume that the recommended heat sink and air flow are used. The V_{EE} regulation and the ambient temperature differentials between packages will reduce these numbers slightly.

Table 2 shows a tabulation of noise margins (using typical tracking rates) for a 10°C ambient temperature differential between packages combined with power supply regulation of ±2%, 0 to 5%, and ±5%. With a 1000 lfpm of air flow, a temperature differential of 10°C is realistic.

When the Macrocell Array is used, power supply regulation has a negligible effect on noise margins. It is interesting to note that it is actually possible to gain noise margin when intermixing the voltage-compensated Macrocell Array and MECL 10K.

Q. Internal Voltage Levels

The output voltage levels of the Interface, and Major Cell macros (and receivers of Output Cell macros) are as follows for inputs at V_{IHA} (min) and V_{ILA} (max) at 25°C with recommended heat sink and air flow.

OUTPUT FOLLOWER Current (mA)	V_{OH} (volts)	V_{OL} (volts)
2.0	−1.0	−1.64
1.0	−0.975	−1.62
0.5	−0.95	−1.6

Note that the internal output voltage swing is smaller than the external output voltage swing. The input threshold voltage is the same as specified for MECL 10K of V_{IHA} (min) = −1.105 volts and V_{ILA} (max) = −1.475. The reason for the smaller swing is to maintain high-speed operation.

As discussed in the previous section, noise margin between chips in a system is determined by the voltage regulation (line drops) and temperature differentials. However, on the chip, the temperature is constant with essentially 0°C temperature differential. Each of the macro functions on the chip have the same value of power supply voltage (due to common mode on the chip) regardless of the external power supply regulation. Therefore, the noise margin for the internal voltage swing is:

NMH = 1105 − 1000 = 105 mV
NML = 1600 − 1475 = 125 mV
at V_{EE} = −5.2 V

The noise margins get larger for V_{EE}>5.2 volts. If V_{EE} = −5.2 V ± 5% (V_{EE} will get as low as −4.96 volts), then the internal noise margins will typically be reduced slightly to NMH = 96 mV and NML = 121 mV.

The short line length of interconnections internal to the chip eliminates the need for transmission lines. In general, internal noise immunity will be greater than the noise immunity between chips in a system.

The output voltage swing for the Y1 output of the Output Cell macros is larger than the internal voltage swing of the other macros. The reason is that the Y output of the output cell must be 10K voltage compatible so the voltage at the base of the output emitter follower has a larger swing. If the Y output is loaded with 50 ohms to −2.0 volts, the Y1 output levels are V_{OH} = −0.90 volts and V_{OL} = −1.7 volts. If the Y output is not connected on chip, the Y1 output levels are V_{OH} = 0.83 volts and V_{OL} = −1.7 volts. The noise margin for the Y1 output is larger than the number indicated above, due to the larger voltage swing.

TABLE 2. — Noise margin guidelines (in millivolts) for MECL 10K and the 10K MACROCELL ARRAY. For an ambient temperature differential of 10°C between packages.

CONDITION		±2% REGULATION $-5.304 \leq V_{EE} \leq -5.096$V	0 to +5% REGULATION $-5.46 \leq V_{EE} \leq -5.2$V	± 5% REGULATION $-5.46 \leq V_{EE} \leq -4.94$V
MECL 10K Driving	NM_H	96	109	70
MECL 10K	NM_L	108	111	46
MACROCELL ARRAY Driving	NM_H	109	110	105
MACROCELL ARRAY	NM_L	140	144	128
MECL 10K Driving	NM_H	109	109	103
MACROCELL ARRAY	NM_L	121	144	79
MACROCELL ARRAY Driving	NM_H	97	110	72
MECL 10K	NM_L	128	111	95

For an ambient temperature differential of 10°C between packages.
(0°C ≤ ambient temperature ≤ 70°C)

V. PERFORMANCE GUIDELINES (not specification limits)

A. Input Current

The maximum input current (at VIH max) at the input pin can be found by adding the following:

1. Multiply 50 μA times the total fan-in.
2. Add 150 μA if the 50 kΩ pull-down resistor is connected to the bonding pad on the chip.

The minimum input current (at V_{IL} min) is 0.5 μA when the input pull-down resistor is connected to the bonding pad. In Final Test, this measurement insures that the resistor is connected. There is no test for minimum input current if the 50 k input pull-down resistor is not used.

B. I/O Capacitance

The maximum capacitance at the I/O pin can be found by adding the following:

1. Multiply 1.0 pF times the total fan-in.
2. Add 2.5 pF for the package, bonding wire and pad capacitance. Use 8.0 pF for 28/40-pin package.
3. Multiply 0.008 pF times the total metal length in mils from the input pin to the macro inputs.
4. Add 1.0 pF if the input compensation network is connected.
5. If the input pin is also driven by an output emitter follower (OEF) from an Output Cell, then 3.0 pF must be added for each OEF connected. A 25 ohm driver macro connects two OEFs to the I/O pin.
6. If a socket is used, add the capacitance specified by the socket manufacturer. The socket capacitance is about 1.5 pF for most sockets.

C. External Degradation Due to Input Capacitance

When a signal drives an input to the MCA with transmission lines using parallel termination, the signal will be degraded due to the I/O pin capacitance. The equations for the maximum propagation delay and rise time degradation *at the I/O pin* are:

$\Delta tpd = .5\ Z_0C$ (For transmission line)
$\Delta tr = .35\ Z_0C$ for $C<10$ pF
$\Delta tr = .6\ Z_0C$ for $10 \leq C<50$ pF

Where Z0 is the characteristic impedance of the transmission line and C is the total capacitance at the I/O pin (see Section B above). For Series terminated lines, the delay times are twice as long as the parallel terminated lines.

D. Propagation Delay Degradation of the Input Macro Due to Rise Time and Voltage Skew at the I/O Pin

When external inputs drive an input pin to the array, the rise and fall times should be 1ns (20 to 80%) in order to meet the propagation delay specified in the Macrocell Library. Although the driving source may provide a signal of 1ns rise and fall times, the capacitance at the end of the transmission line (see Section C) will degrade the signal. For each nanosecond, increase above 1ns in the rise or fall time at the input pin of the Macrocell Array, 175 ps delay degradation should be added to the input macro. This assumes that the 50% point of the input signal is not skewed by more than ±20 mV of nominal V_{BB}. For an ambient temperature of 25°C, the nominal $V_{BB} = -1.3$ volts. Over temperature, V_{BB} changes typically +1.1 mV/°C. The propagation delay degradation, in picoseconds, due to the rise or fall time of the input signal being larger than 1ns is:

Δtpd (Rise time) $= 0.175\ (t_r - 1000)$ where t_r is the 20 to 80% rise or fall time at the I/O pin in picoseconds.

If the 50% point of the input signal is skewed by more than ±20 mV from the switching point (V_{BB}) of the Output Macro, inaccurate propagation delay measurements can result when the measuring equipment uses the 50% point of the input and output signals as the reference point. When the input signal is skewed negative, the propagation delay will appear larger on the rising edge and shorter on the falling edge. The propagation delay change (in picoseconds) due to the input signal being skewed can be calculated using the following equation:

Δtpd (voltage skew) $= \pm 2.1\ (\Delta V \text{ skew})\ t_r$
Where t_r is the 20 to 80% rise (or fall) time of the input at the I/O pin in nanoseconds, ΔV skew is the amount of voltage difference in millivolts between the 50% point of the input signal and the actual V_{BB} voltage.

E. Propagation Delay Degradation of the Input Macro Due to Metal Resistance from the Input Pin to the Macro

Metal Resistance from the I/O pin to the input macro can cause the degradation of the rise and fall time due to the capacitance of the metal and the capacitance due to fan-in. If the resistance of the metal was 0 ohms, then the rise and fall times at the I/O pin would be about the same as at the input macro. However, the resistance of first metal is 0.2 ohms/mil, while the resistance of second metal is 0.062 ohms/mil. The following equations should be used for calculating the degradation due to metal and fan-in:

Δt_{pd} (input metal) = 0.4 ps/mil
Δt_{pd} (fan-in) = 20 ps/fan-in
These numbers are added together to find the total degradation.

F. Input Compensation Network and Input Degradation

The input compensation network is discussed in Section IV-D, page 14.

Since the input compensation network places 75 ohms at the input pad and in series with the metal going to the input macro, the rise and fall times are degraded as indicated in Section E. The following equations should be used for calculating the degradation due to metal and fan-in when the input compensation network is connected.

Δtpd (input metal) = 1ps/mil
Δtpd (fan-in) = 50 ps/fan-in

G. Delay Due to Package and Socket

The Interface and Major Cell macros in the Macrocell Library have the propagation delays specified from the input to the output of the macro for a fanout of 1 and does not include any delay due to the package or socket. For the Output Cell macros, the specified delay includes the delay of the packages at the output only. The delay of the package and the socket is mainly due to the physical length of the pins involved. The following delays for the package and socket should be added where appropriate:

Δtpd (68-pin package) = 75 ps
Δtpd (68-pin AMP Surface to Surface Socket) = 100 ps

If the socket is used, the above numbers should be added to the delay path at inputs while only the socket delay needs to be added for outputs.

H. Simultaneous Switching Delay

The V_{CCO} pins on the array provide a ground for the (50 ohm and 25 ohm drive) output emitter followers (OEF's) of the output macros. These pins provide the switching current to the outputs. The current supplied to V_{CC} is rather constant while the current supplied to V_{CCO} changes when outputs are switching. The V_{CC} and V_{CCO} pins should be connected together to a good ground outside the package, similar to normal MECL 10K grounding. Bypass capacitors should be used near the load resistors in order to supply the switching current.

For the MCA1200 with four V_{CCO} Pins, simultaneous switching of the outputs can cause a delay penalty of 1ns (Max) that should be added to the output delay when a socket such as the AMP surface to solder tail is used.

If Berg clips are used, a 750 ps (Max) delay penalty should be added to the output delay. The reason for the delay penalty is due to the inductance of the V_{CCO} pin of the package and socket which limits the response time of the bypass capacitor in supplying the switching current.

For the MCA1200 with eight V_{CCO} pins and the MCA600 in the 68-pin package, a delay penalty of 750 ps should be used with the AMP surface to solder tail socket and 650 ps with Berg clips.

I. Simultaneous Switching Noise

When switching all the outputs on a V_{CCO} pin except one, a noise pulse of about 2 ns wide is coupled to the non-switched outputs due to cross-talk and lead inductance.

For the MCA1200 with four V_{CCO} pins, the maximum noise amplitude is typically less than 200 mV (175 mV if berg clips are used) with no restrictions on the number of outputs switching simultaneously. The typical ac noise required to switch a latch in the macrocell array is 450 mV, giving a margin of 250 mV. This noise margin appears to be adequate in a well-designed system.

For the MCA1200 with typically eight V_{CCO} pins or the MCA600 in the 68-pin package, the maximum noise amplitude is typically less than 150 mV (130 mV if berg clips are used). The noise amplitude can be reduced by 25% if driver macros (with V_{OL} in the cutoff mode) are not used. Also, the noise amplitude can be reduced by limiting the number of outputs switching simultaneously on a common V_{CCO} pin. This can be accomplished by equally distributing the outputs on the V_{CCO} pins and using some of the pins as inputs.

Again, the noise margin is adequate in a well-designed system. Of primary concern to the system designer is to make sure that the clock lines of flip-flops and latches are designed with the considerations noted above.

J. Metal and Fanout Degradation

The metal interconnect between macros in the array represents a line capacitance (0.008 pF/mil maximum for the average of first and second metal) to the driving gate. This line capacitance primarily affects the fall time. Worst case curves are shown in Figures 13 through 19 for metal and fan-out degradation. Worst case includes process tolerances, temperature, and power supply variations. The first and second metal lengths are combined since their delays due to fan-out are approximately the same. The total length of the metal interconnect between the driver output and all the inputs should be used for the metal length in the degradation curves.

It is recommended that a 2.0 mA output follower current be used in critical delay paths. In order to save power, a 1.0 mA follower current can be used in critical paths where fan-outs are 3 or less and metal lengths are less than 150 mils. An 0.5 mA follower current can be used to save power on non-critical delay paths.

The maximum fan-out should be limited to 15 due to ac delay considerations. The maximum DC fan-out is limited to 30 due to noise margin considerations.

An analysis of some of the metal lengths in several MCA options was performed. The results showed that the metal length can be approximated by knowing the number of connections between macro cells. If the output of one cell is connected to another cell, the number of connections is two. If the output of one cell is connected to two other cells, the number of connections is three. More than one connection in the same cell is still counted as one connection. Multiplying 40 mils times the number of connections will give an average line length. This number can be used with the curves (Figures 13 through 19) to *estimate* worst case delays in a logic design before it is actually implemented into an MCA option. NOTE: This is an average estimate only. The actual line length after the layout is completed can be calculated using a program on the CAD system called FOIL. Also, a program called ACMCASIM can be used to calculate maximum input to output delays.

An example can be shown to illustrate the use of the curves shown in Figure 13 through 19. Assume that a 4 to 1 MUX (M36) is driving a fan-out of 5 and the total number of connections is 6. From the "rule of thumb" above, this represents a metal length of 240 mils. For a 2.0 mA follower, Figure 14 shows that the delay degradation is 450 ps. For a 1.0 mA follower, Figure 17 shows a delay degradation of 1600 ps. The propagation delay shown in the Macrocell Library for the data input to output driving a fan-out of 1 is 1.4 ns. Therefore, the total falling edge delay for a fan-out of 5 with 240 mils of metal is 1.85 ns for a 2.0 mA follower and 3.0 ns for a 1.0 mA follower. This illustrates the advantage of using a 2.0 mA follower current for decreasing the falling edge delay. However, note that the rising edge delay (Figure 13) increases by 250 ps for a 2.0 mA follower from 1920 ps to 2170 ps.

K. Wire ORing

Outputs of Interface Cell macros, Major Cell macros, and internal outputs (Y1, Z) of Output Cell macros can be tied together to form a wired OR function. The total number of wire OR's allowed per wired OR function is eight which must include the macro internal wire OR's (internal wire OR's are listed in the Macrocell Library).

Wire ORing of internal macro outputs will cause some degradation which should be added to the propagation delay specified in the Macrocell Library. The propagation delay degradation for the output falling, tpd− is a maximum of

$$\Delta tpd- = (20\ ps) \times (\text{total number of wire OR's})$$

This degradation is small since the delay is due to a very small capacitance associated with the additional output device on the line. The propagation delay for the output rising, tpd+, is much larger as shown in Table 3. When two macro outputs are wire ORed and both are in the "low" state, one output could be supplying more current to the load resistors than the other output (called current hogging). When the output that is supplying the smallest amount of current switches to the "high" state, it must now supply all of the current resulting in the additional delay shown in Table 3. The Table also shows the allowable combination of the number of wire OR's versus the required total output follower current.

The minimum output follower current allowed when wire ORing macros is 1.0 mA while the maximum is 2.0 mA. A 1.0 mA output follower can use up to four wire OR's, 1.5 mA up to six wire OR's, and 2.0 mA up to eight wire OR's.

As an example, suppose that the Y output of four M36's must be wire OR'ed. From the Macrocell Library, M36-Y already has two wire OR's internally. From Table 3, a 2.0 mA output follower current (0.5 mA at each M36-Y output) must be used and a 600 ps delay must be added on the rising edge of the output. For the falling edge delay, 160 ps (8 x 20 ps) must be added.

If the Y outputs of two M36's are wire OR'ed, the total number of wire OR's is four. A 1.0 mA or 2.0 mA current can be chosen resulting in a rising delay of 250 ps or 400 ps, respectively. The falling delay is 80 ps. For large fanouts and large metal runs, it is usually better to choose a 2.0 mA follower current in order to reduce the falling edge delay.

If the Y output of two M20's are wire OR'ed, the total number of wire OR's is eight. Thus, a 2.0 mA follower current must be used resulting in a 600 ps rising edge delay and 160 ps falling edge delay.

NOTE: The wire OR delay is only used for macro outputs that are externally wire OR'ed together. The wire OR delay is not added to the delay path for a macro output having no external wire OR connections, although internal wire OR's may exist.

TABLE 3 — Maximum Delay Degradation Guidelines for Output Rising, Δtpd+, versus the Number of Wire OR's and Output Follower Current.

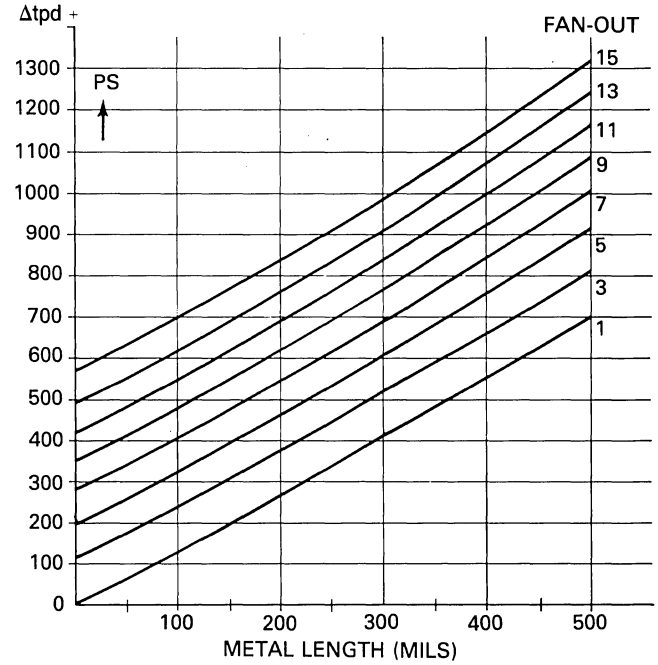
Total Output Follower Current (mA)	Δtpd + in ps						
	Total number of wire OR's						
	2	3	4	5	6	7	8
1.0	150	200	250	—	—	—	—
1.5	225	275	325	375	425	—	—
2.0	300	350	400	450	500	550	600

NOTE: The total number of wire OR's must include the internal wire OR's in each macro.

L. Minimum Propagation Delay

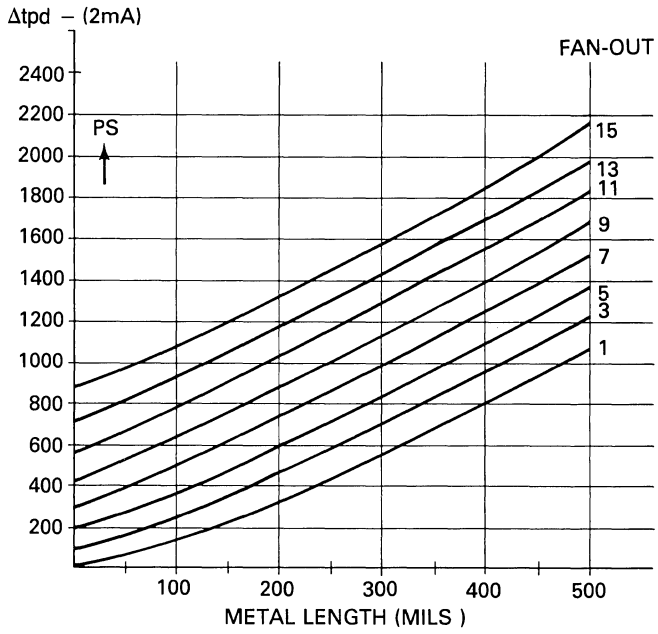
The minimum propagation delay guideline for Major Cell and Interface Cell macros is 40% of the maximum specified delay, while the guideline for Output Cell macros is 25% of the maximum specified delays. An exception to this rule is a Major Cell macro having an

FIGURE 13. RISING EDGE (METAL LENGTH AND FAN-OUT) PROPAGATION DELAY DEGRADATION FOR 0.5, 1.0, 1.5, 1.8, AND 2.0 mA OUTPUT FOLLOWER CURRENT



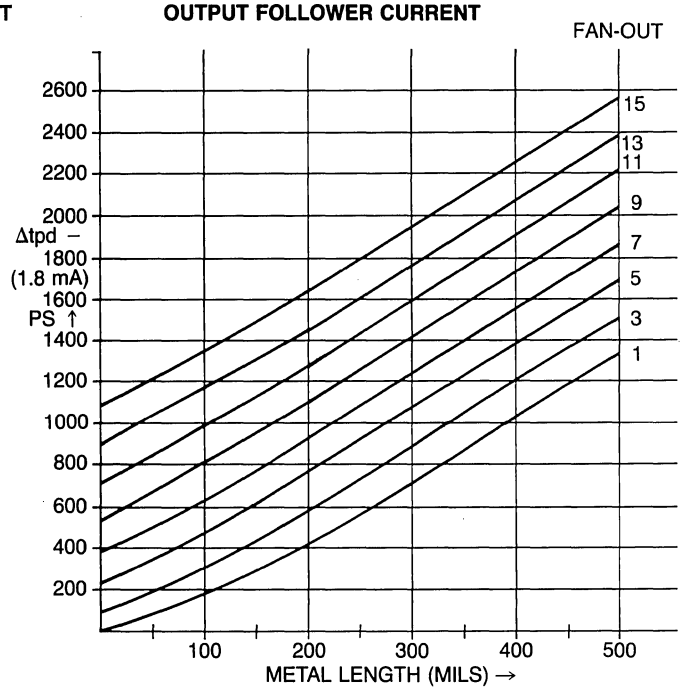
NOTES: 1. Add 250 ps if 2.0 mA is used.
2. Add 200 ps if 1.8 mA is used.
3. Add 125 ps if 1.5 mA is used.

FIGURE 14. FALLING EDGE (METAL LENGTH AND FAN-OUT) PROPAGATION DELAY DEGRADATION FOR 2.0 mA OUTPUT FOLLOWER CURRENT



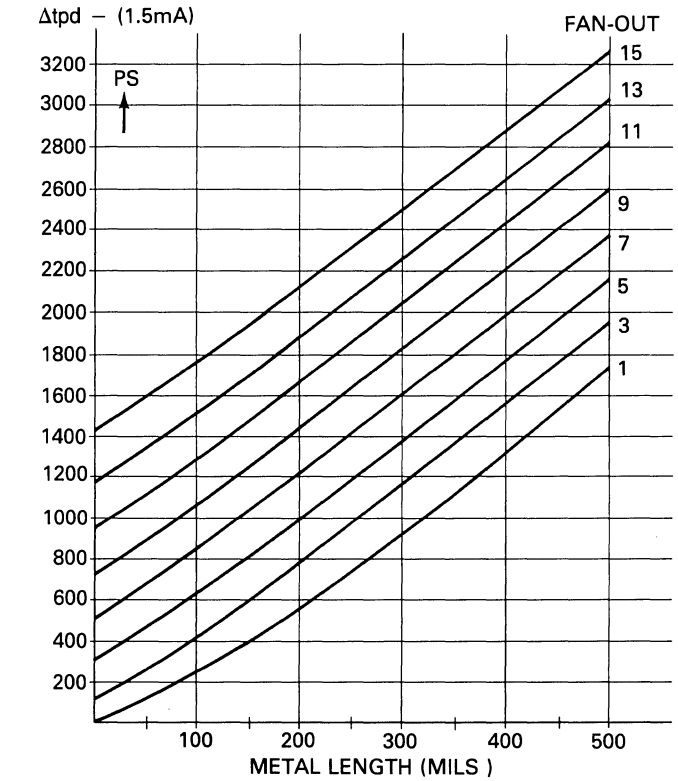
NOTE: Subtract 250 ps when 2.0 mA is used.

FIGURE 15. FALLING EDGE (METAL LENGTH AND FAN-OUT) PROPAGATION DELAY DEGRADATION FOR 1.8 mA OUTPUT FOLLOWER CURRENT



NOTE: Subtract 200 ps when 1.8 mA is used.

FIGURE 16. FALLING EDGE (METAL LENGTH AND FAN-OUT) PROPAGATION DELAY DEGRADATION FOR 1.5 mA OUTPUT FOLLOWER CURRENT



NOTE: Subtract 125 ps when 1.5 mA is used.

FIGURE 17. FALLING EDGE (METAL LENGTH AND FAN-OUT) PROPAGATION DELAY DEGRADATION FOR 1.0 mA OUTPUT FOLLOWER CURRENT

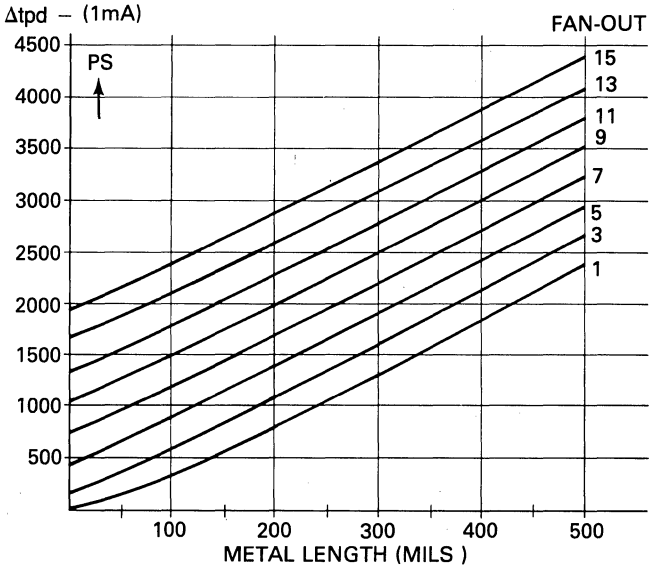
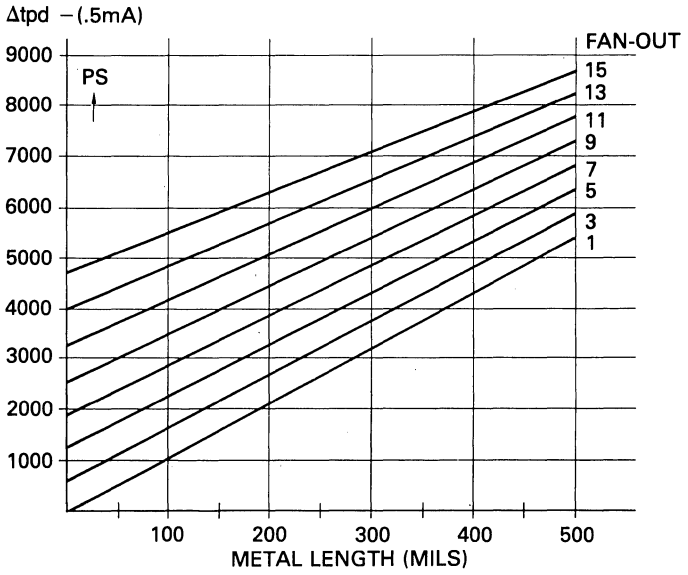
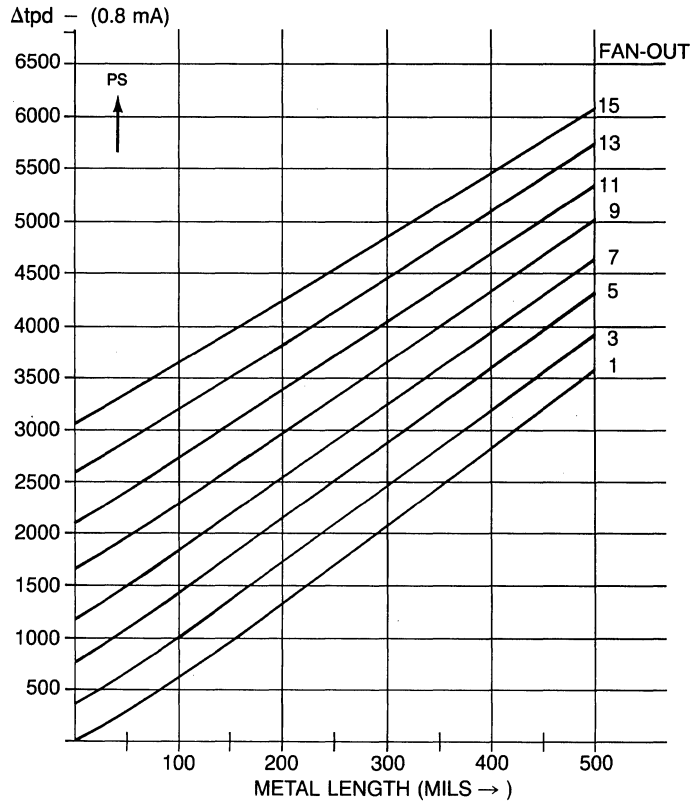


FIGURE 19. FALLING EDGE (METAL LENGTH AND FAN-OUT) PROPAGATION DELAY DEGRADATION FOR 0.5 mA OUTPUT FOLLOWER CURRENT



internal wire OR of 3 or 4. For these macros, 30% of the specified maximum delay should be used for *both* outputs. The minimum delay time due to metal length and fan-out can be calculated by multiplying the maximum delay by 25%. The maximum macro delay times can be found in the Macrocell Library. It should be noted that the minimum delay times occur at 0°C ambient temperature and assumes thermal equilibrium has been established.

FIGURE 18. FALLING EDGE (METAL LENGTH AND FAN-OUT) PROPAGATION DELAY DEGRADATION FOR 0.8 mA OUTPUT FOLLOWER CURRENT



To calculate the minimum delay between an input and output pin, the shortest delay path must be used in the calculation. Multiplying 25% times the maximum delay specified between an input and output pin does not guarantee a minimum delay.

M. On-Chip Propagation Delay Skew

Within the MCA chip, the guideline for difference in propagation delay for identical Interface Cell and Major Cell macros that are electrically adjacent is 100 ps if the inputs to these cells are driven from the same driving source. However, the delay difference due to metal and fan-out at the output of these cells must be taken into consideration. Electrically adjacent cells share the same V_{CC} and V_{EE} bus and bias driver. For the same conditions above for Output Cell macros, the delay difference guideline is 300 ps.

For the MCA1200ECL, electrically adjacent cells are cells in the same row in columns 1 & 2 and columns 5 & 6 (refer to Figure 3a.). For instance, cell at location 11 is adjacent to cell 12, cell 15 is adjacent to 16, etc. Note that cell 12 is not adjacent to cell 15. For the MCA600ECL, electrically adjacent cells are cells in the same row in columns 1 & 2 and columns 3 & 4 (refer to Figure 3b.). Also, the A and B of the same cell location are adjacent. For instance, interface cell at locations 10A and 10B are adjacent, half cell at locations 11A and 11B are adjacent.

The estimated maximum delay spread across the MCA chip can be calculated as follows:

1. For the macrocell delay spread, multiply the maximum delay by 25%.
2. For the metal and fan-out delay spread, multiply the maximum delay by 40%.

As an example, assume two different macros are specified with a delay of 1.2 ns and each has a metal and fan-out delay of 500 ps. Then, the maximum on-chip delay spread for the macro delay is 300 ps (1.2 ns x 25%) and for the metal and fan-out delay is 200 ps (500 ps x 40%) for total delay spread of 500 ps. Thus, one macro plus the associated metal and fan-out delay could be a maximum of 1.7 ns under worst case conditions, while the other macro (on the same chip) plus the associated metal and fan-out delay would be 1.2 ns minimum. The minimum delay for any chip can be calculated from Section L. The minimum delay is 0.605 ns (1.2 ns x 40% + 0.5 ns x 25%). Therefore, one macro plus the associated metal and fan-out could be a minimum of 0.605 ns under worst case conditions while the other macro (on the same chip) plus the associated metal and fan-out delay would be 1.105 ns maximum.

N. Setup and Hold Time Calculations

The worst case setup and hold times (minimums) for the flip-flop and latch macros are specified in the Macrocell Library. In order to calculate the setup and hold times for the data at the package pins, the maximum and minimum propagation delays for the data path and the clock path to the flip-flop or latch macro must be calculated.

The minimum setup time is the amount of time the data must be present at the data input pin before the latching edge of the clock at the clock input pin in order to insure the data is latched properly. The minimum hold time is the amount of time the data must remain unchanged at the data input pin after the latching edge of the clock at the clock input pin in order to insure the data will remain valid.

In general, the minimum setup time for a data input, t_S Min (data pin), can be calculated by adding the setup time specified for the flip-flop or latch macro t_{setup} (macro), to the maximum data path delay, t_{pdMax}(DP), and then subtracting the minimum clock path delay. The hold time for a data input, $t_{H\ Min}$ (data pin), can be calculated by adding the hold time specified for the flip-flop or latch macro, t_{HOLD}(macro), to the maximum clock path delay, t_{pdMax}(CP), and then subtracting the minimum data path delay.

The on-chip delay spread (see Section M) between the clock and data inputs can be used in the calculations. The following equations are derived for calculating the minimum setup and hold times, taking into account the minimum propagation delay (Section L) and the on-chip propagation delay skew (Section M).

If $t_{pdMax}(DP) \geq t_{pdMax}(CP)$, then:

(1) $t_{sMin}(\text{DATA PIN}) = T_{SETUP}(\text{MACRO}) + t_{pdMax}(DP) - 0.6\ t_{pdMax}(\text{CP MFO}) - 0.75\ t_{pdMax}(\text{CP MAC})$.

(2) $t_{HMin}(\text{DATA PIN}) = t_{HOLD}(\text{MACRO}) + 0.65\ t_{pdMax}(CP) - 0.25\ t_{pdMax}(\text{DP MFO}) - 0.4\ t_{pdMax}(\text{DP MAC})$.

If $t_{pdMax}(DP) < t_{pdMax}(CP)$, then:

(3) $t_{sMin}(\text{DATA PIN}) = t_{SETUP}(\text{MACRO}) + 0.65\ t_{pdMax}(DP) - 0.25\ t_{pdMax}(\text{CP MFO}) - 0.4\ t_{pdMax}(\text{CP MAC})$.

(4) $t_{HMin}(\text{DATA PIN}) = t_{HOLD}(\text{MACRO}) + t_{pdMax}(CP) - 0.6\ t_{pdMax}(\text{DP MFO}) - 0.75\ t_{pdMax}(\text{DP MAC})$.

where,

t_{pdMax}(DP) is the maximum data path delay from the data input pin to the data input of the flip-flop or latch macro.

t_{pdMax}(CP) is the maximum clock path delay from the clock input pin to the clock input of the flip-flop or latch macro.

t_{pdMax}(CP MFO) is the maximum delay due to the metal and fan-out in the clock path.

t_{pdMax}(CP MAC) is the maximum delay due to the macros in the clock path.

t_{pdMax}(DP MFO) is the maximum delay due to metal and fan-out in the data path.

t_{pdMax}(DP MAC) is the maximum delay due to the macros in the data path.

It should be noted that when calculating the minimum setup time for a data register, the longest data path and the shortest clock path should be used for the calculation. For the minimum hold time, the shortest data delay path and the longest clock path should be used.

Example: Suppose an MCA option has an ALU output driving a data register composed of H31's. To calculate the minimum setup time for the data, the longest data path to the register must be used. In this case, a binary addition operation from the least significant data bit to the most significant sum output of the ALU produces the longest delay path.

For this condition, $t_{pdMax}(DP) = 12.4$ ns, t_{pdMax}(DP MAC) = 7.9 ns, t_{pdMax}(DP MFO) = 4.5 ns, $t_{pdMax}(CP) = 2.1$ ns, t_{pdMax}(CP MAC) = 1.2 ns, t_{pdMax}(CP MFO) = 0.9 ns, and T_{SETUP}(H31) = 1.5 ns. Since $t_{pdMax}(DP) \geq t_{pdMax}(CP)$ equation (1) can be used to calculate the minimum setup time. Therefore,

$$t_{sMin}(\text{DATA PIN}) = 1.5 + 12.4 - 0.6\ (0.9) - 0.75\ (1.2) = 12.46 \text{ ns}$$

To calculate the minimum hold time for the data, the shortest data path to the register must be used. In this case, a data transfer operation produces the shortest data path. The clock path remains the same. For this condition,

t_{pdMax}(DP) = 9.0 ns, t_{pdMax}(DP MAC) = 5.7 ns,
t_{pdMax}(DP MFO) = 3.3 ns, and t_{HOLD}(H31) = 0 ns

Equation (2) can be used to calculate the minimum hold time, therefore:

$t_{H\ Min}$(DATA PIN) = 0 + 0.65 (2.1) − 0.25 (3.3) − 0.4 (5.7)
= −1.74 ns

The minus sign on the result indicates that the data can change up to 1.74 ns prior to the clock edge (rising edge).

O. Pulse Width Shrinkage

When driving clock lines to latches and flip-flops, the minimum pulse width specified for these macros must be maintained. Pulse shrinkage can occur due to the delay differences in the rising edge delay versus the falling edge delay for the macro and for the metal and fan-out. Even if the worst case rising and falling edge delay are specified the same, pulse shrinkage can still occur.

The maximum delay spread specified in Section M is slightly modified as applied to pulse shrinkage. The maximum delay spread for pulse shrinkage can be calculated as follows:

1. For the pulse going through a macro, the negative going output pulse will shrink due to the macro + and − delay skew a maximum of:

   (1) PW-(MAC, SHRINK) = t_{pd-}(MAC) − 0.75 t_{pd+}(MAC),

   while the positive going pulse will shrink a maximum of:

   (2) PW_+(MAC,shrink) = t_{pd+}(MAC) − 0.75 t_{pd-}(MAC),

   where:

   t_{pd-}(MAC) is the maximum macro propagation delay for the falling edge (−) output as specified in the Macrocell Library, and

   t_{pd+}(MAC) is the maximum macro propagation delay for the rising edge (+) output.

2. The metal and fan-out at the output of the macro will shrink the negative going pulse a maximum of:

   (3) PW_-(MFO,shrink) = t_{pd-}(MFO) − 0.6 t_{pd+}(MFO)

   while the positive going pulse will shrink a maximum of:

   (4) PW_+(MFO,shrink) = 0.65 t_{pd+}(MFO) − 0.25 t_{pd-}(MFO)

   where:

t_{pd-}(MFO) is the maximum falling edge delay for metal and fan-out from Figures 14–19.

t_{pd+}(MFO) is the maximum rising edge delay for metal and fan-out from Figure 13.

Equations (1) and (3) can be combined to produce the total negative pulse width shrinkage due to the driving macro, and the metal and fan-out.

(5) PW_-(shrink) = t_{pd-}(MAC) − 0.75 t_{pd+}(MAC) + t_{pd-}(MFO) − 0.6t_{pd+}(MFO).

Similarly, equations (2) and (4) can be combined to produce the total positive pulse width shrinkage due to the driving macro, and the metal and fan-out.

(6) PW_+(shrink) = t_{pd+}(MAC) − 0.75 t_{pd-}(MAC) + 0.65 t_{pd+}(MFO) − 0.25 t_{pd-} (MFO)

The external clock driver that drives the clock input pin must have rise and fall time capable of generating the minimum required pulse width as defined in equations (5) and (6). The minimum pulse width (in ns) that the external clock driver can generate is calculated as follows:

(7) PW_{MIN} (DRIVER) = 1.7 tr + 0.1 (FI-1) where tr is the 20 to 80% rise time (in ns) at the input pin and FI is the input fan-in.

Example 1: What is the minimum negative pulse width required at the clock input pin that drives a buffer OR gate (H01) which in turn drives 8-latch enable inputs (4-H35's)? The output follower current for the OR gate output is 2 mA with a metal length of 160 mils. All the parameters required in equation (5) can be found in the Macrocell Library and in Figures 13 and 14.

t_{pd}(MAC) = 1.2 ns, t_{pd-}(MFO) = 710 ps, t_{pd+}(MFO) = 520 ps.

Substituting in equation (5) results in:

PW_-(shrink) = 1.2 − 0.75(1.2) + .71 − 0.6 (0.52) = 0.698 ns

Since t_{pw}(H35) = 2.0 ns, the minimum negative pulse width required at the clock input pin is 2.7ns (2.698 rounded off).

Example 2: If eight master-slave flip-flops (8-H31's) are used in example 1 instead of latches, what is the highest frequency that can be applied at the clock input pin? The minimum negative pulse width is 2.7 ns as calculated in example 1. The maximum positive pulse width shrinkage can be calculated using equation (6) resulting in:

PW_+(shrink) = 1.2 − 0.75(1.2) + 0.65(0.52) − 0.25(0.71) = 0.46 ns

Since t_{pw}(H31) = 2.0 ns, the minimum positive pulse width required at the clock input pin is 2.5 ns (2.46 ns rounded off). Therefore, the highest frequency that can be used at the clock input pin is 1/5.4 ns = 185 MHz. (50% Duty Cycle)

Example 3: If a MECL 10KH gate drives the clock input pin which in turn drives 8-H78 clock inputs what is highest frequency that can be applied if the rise or

fall time is 2 ns maximum at the input pin? From equation (7) the minimum pulse width that can be generated is 1.7 (2.0) plus 0.1 (7) or 4.1 ns. Since this is larger than the minimum clock pulse width required for H78, the highest frequency that can be applied is 1/(4.1 + 4.1) = 121 MHz.

Pulse width shrinkage (and stretching) can be reduced to a minimum by using *pairs of electrically adjacent inverting gates* with approximately the same fan-out and metal length. See Section M for the definition of electrically adjacent cells. The following equations were derived for a pair of electrically adjacent inverting gates (gate 1 driving gate 2) where t_{pd-} (MF01) is the falling edge delay of the metal and fan-out at the output of the first inverting gate (gate 1) while t_{pd-}(MF02) is the falling edge delay of the metal and fan-out at the output of the second inverting gate (gate 2). For $t_{pd-}(MF01) \leq t_{pd-}(MF02)$

$$(8)\ PW_-(shrink) = 100ps + .2[t_{pd-}(MF01) + t_{pd+}(MF01)] + t_{pd-}(MF02) - t_{pd-}(MF01) - 0.6[t_{pd+}(MF02) - t_{pd+}(MF01)]$$

$$(9)\ PW_+(shrink) = 100ps + 0.2[t_{pd-}(MF01) + t_{pd+}(MF01)] + 0.65[t_{pd+}(MF02) - t_{pd+}(MF01)] - .25[t_{pd-}(MF02) - t_{pd-}(MF01)]$$

For $t_{pd-}(MF01) > t_{pd-}(MF02)$

$$(10)\ PW_-(shrink) = 100ps + 0.2[t_{pd-}(MF02) + t_{pd+}(MF02)] + 0.65[t_{pd+}(MF01) - t_{pd+}(MF02)] - 0.25[t_{pd-}(MF01) - t_{pd-}(MF02)]$$

$$(11)\ PW_+(shrink) = 100ps + 0.2[t_{pd-}(MF02) + t_{pd+}(MF02)] + [t_{pd-}(MF01) - t_{pd-}(MF02)] - 0.6\,[t_{pd+}(MF01) - t_{pd+}(MF02)]$$

If the input pulse is less than 10 ns and goes through more than one gate in series (inverting or non-inverting), additional delay must be added to the pulse width shrinkage, as indicated below, for each additional series gate.

1. For an input pulse width between 5 and 10 ns, 100 ps must be added to the pulse width shrinkage for each additional series gate.
2. For an input pulse width less than 5 ns, 200 ps must be added to the pulse width shrinkage for each additional series gate.

Internal pulse widths should be maintained at 2 ns or greater, taking into account the pulse shrinkage. If the pulse is going to an output pin from an output macro, the pulse at the pin must be 5 ns or greater after the pulse shrinkage is calculated.

The reason for the additional pulse width shrinkage (for both positive and negative pulses) for a pulse width of less than 10 ns is the following: For a negative going input pulse, t_{pd++} and t_{pd+-} (of the macro being driven) becomes faster as the input pulse width becomes narrower. Similarly, for a positive going input pulse, t_{pd--} and t_{pd-+} (of the macro being driven) becomes faster as the pulse width becomes narrower.

P. Clock Distribution and Clock Pulse Generation

The use of OR gates is recommended, such as H01, in developing a clock chain or tree. To minimize clock skew, the clock drivers should be electrically adjacent as described in Section M. A 2 mA output follower current should be selected at the clock driver outputs in order to reduce clock pulse shrinkage and a maximum fan out of 10 is recommended for optimum performance.

Clock distribution on the MCA option can be easily designed by the example shown in Figure 20. The previous sections M, N, and O can be used to calculate the important parameters of clock skew, pulse shrinkage and setup and hold times. If the clock drivers are connected to latches such as H33 or H35, the minimum negative pulse width must be greater than 2.0 ns at the latch enable input. To calculate the pulse width shrinkage, equation (5) of Section O. can be used, resulting in:

$$PW_-(shrink) = 1.2 - 0.75(1.2) + 1.1 - 0.6(0.75) = .95\ ns$$

Therefore, the negative clock pulse width at the clock input pin must be greater than 2.95 ns. If master-slave flip-flops such as H31 are being driven, the minimum positive pulse width at the macro clock input must also be greater than 2.0 ns. To calculate the pulse width shrinkage, equation (6) of Section O can be used, resulting in:

$$PW_+(shrink) = 1.2 - 0.75(1.2) + 0.65(0.75) - 0.25(1.1) = .5125\ ns$$

Therefore, the positive pulse width at the clock input pin must be greater than 2.52 ns.

The clock pulse can be generated on-chip by connecting the optional delay network shown in Figure 20. A high to low transition on the clock input pin results in a negative clock pulse that is dependent on the propagation delay of the delay network.

To calculate the delay required for the delay network, the on-chip propagation delay skew must be calculated as defined in Section M. The minimum pulse width required by the latch or flip-flop is specified for a slow chip. The delay network will automatically compensate for a fast or slow chip. The delay network must be designed to guarantee that a negative pulse width of greater than 2.0 ns (for H31, H33, H35) appears at the macro clock input for a slow chip. If it is a fast chip, then the minimum pulse width required can be smaller with the delay of the delay network also being smaller. If the clock pulse was generated off-chip, the delay

network would have to be designed using minimum delays (Section L).

The following equation is derived to calculate the pulse width generated by the delay network, PW(DN), taking into consideration the on-chip propagation delay skew.

(1) $PW(DN) = 0.75\ t_{pd}Max(DN\ MAC) + 0.6\ t_{pd}Max(DN\ MFO)$,

where, $t_{pd}Max(DN\ MAC)$ is the maximum delay due to the macros in the delay network,

$t_{pd}Max(DN\ MFO)$ is the maximum delay due to the metal and fan-out in the delay network.

Example: Calculate the pulse width generated by the delay network shown in Figure 20. The high to low transition on the clock pin causes a high to low transition on the first two gates and a low to high transition on the last gate of the delay network:

$t_{pd}Max(DN\ MAC) = 2(1.4) + 1.2 = 4.0$ ns

$t_{pd}Max(DN\ MFO) = 2(0.2) + 0.15 = .55$ ns

Substituting into equation 1 results in:

$PW(DN) = 0.75(4.0) + 0.6(.55) = 3.3$ns

The 3.3 ns pulse generated by the delay network is larger than the required pulse width of 2.95ns, resulting in a minimum pulse width at the macro clock input of 2.35 ns (due to pulse width shrinkage).

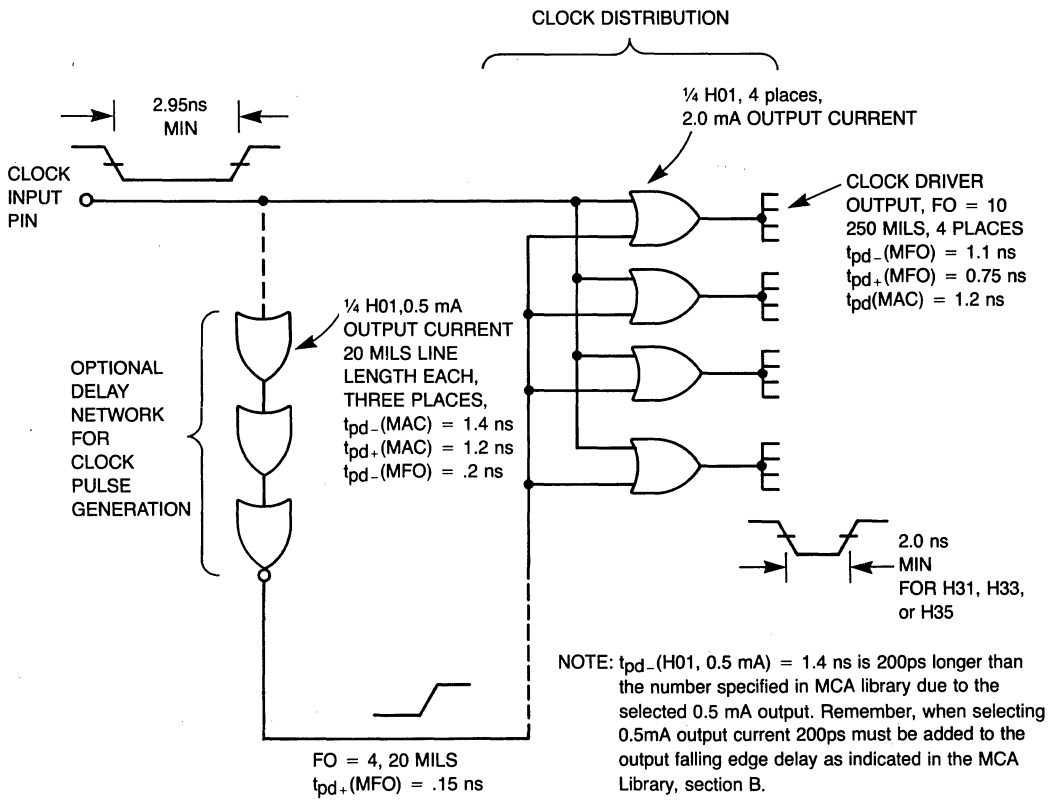


FIGURE 20. Clock Distribution Example

Q. AC Delay Variations Versus Temperature and Voltage

Figure 21 shows the typical ac delay variations of a macrocell test option versus temperature and power supply variations. Both the rising edge and falling edge delay are plotted. The delay path consists of seven Major Cell macros plus one Output Cell macro. Each Major Cell macro has a 1.0 mA output follower current driving a fan-out of three and an average metal length of 75 mils. All the macros in the path switch from the low to high state for the rising edge delay and from the high to low state for the falling edge delay.

Temperature increases both the rising and falling edge delays with the rising edge delay increasing twice as fast. A ± 10% power supply variation shows that the falling edge delay has almost three times greater variation than the rising edge delay. However, when the power supply voltage is decreased, the rising edge

delay becomes faster and the falling edge delay becomes slower. It is interesting to note that for V_{EE} = −4.68 V and a temperature (ambient) of 70° C, the rising and falling edge delays have increased about the same amount (15%) over the nominal value at room temperature and V_{EE} = −5.2 V.

Although the curves show typical values for a macrocell test option, it is typical for other options developed from the Macrocell Array such as the MC10900 family. If the delay path has at least one inversion, the percent delay increases are normally smaller than shown in Figure 21. The use of 2mA output follower currents in critical paths will normally reduce the percent increase in the falling edge delay since the metal delay will be a smaller percentage of the total delay. However, using 2.0 mA output currents with long metal runs and fan-out will bring the percent increases back in line with Figure 21.

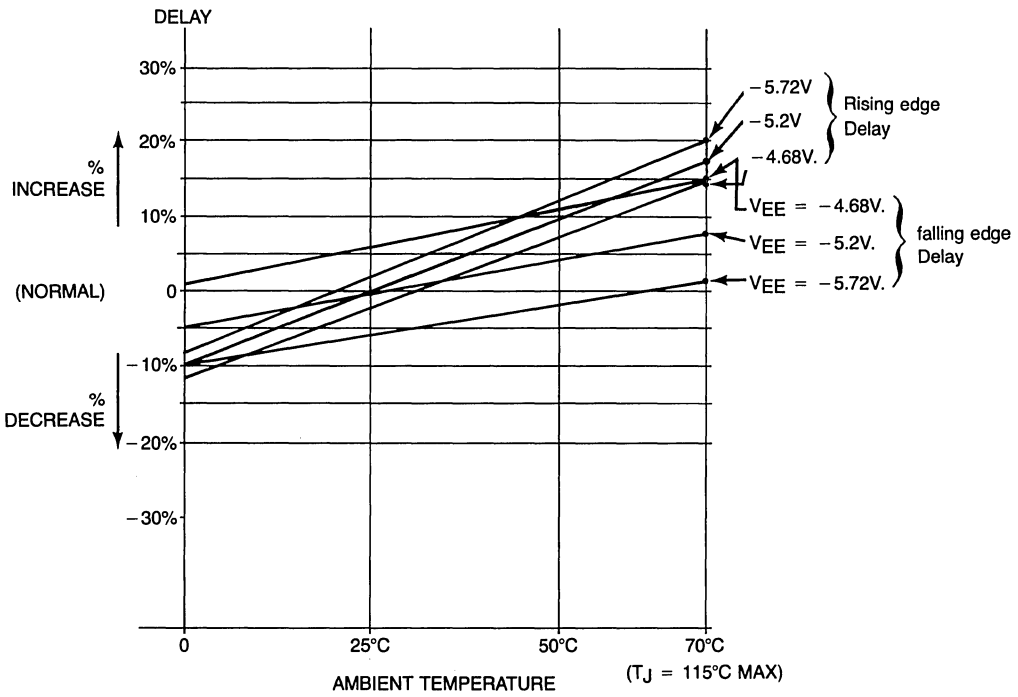


FIGURE 21. Typical AC Delay Variations versus Temperature and Voltage.

VI. CAD LAYOUT CONSIDERATIONS

A. Wire ORing

When outputs are tied together, current will flow from the output that is "high" to the load resistors located at other outputs. This current causes a small IR drop, which decreases the noise margin. The maximum IR drop allowed from output to input is 25 mV. The resistance of first layer metal is 0.2 ohms/mil while the resistance for second layer metal is 0.062 ohms/mil. For instance, assume there is a metal run of 100 mils total between two outputs tied together where 50 mils is on first layer and 50 mils is on second layer. A 1.0 mA output follower current at each output would mean that 1.0 mA of current would flow from the output that is "high" to the other output when in the "low" state. This could cause a voltage drop of 10 mV on first layer and 3.1 mV on second layer for a total drop of 13.1 mV. The wired OR outputs should be physically as close as possible to reduce loss of noise margin.

B. Via Placement

In the routing alleys (see Figure 3) the only restriction on via's (connection between 1st and 2nd layer metal) is that adjacent horizontal via's are not allowed. This restriction has very little impact on the layout of a circuit. Adjacent vertical and adjacent diagonal via s are allowed.

C. Y Output Metal Length to the Output Emitter Follower Transistor (OEF)

The maximum metal length allowed from the Y output of an Output Cell macro to the OEF near the bonding pad is 100 mils. On the CAD system, the metal length to the bonding pads is calculated using a FOIL program. Larger metal runs reduce noise margins and increase propagation delays.

D. Transceiver and Driver Macro Placement

When placing the transceiver macros (016 or 017) or the 25 ohm driver macros (024 and 025), locations 27, 37, 47, 57, 67, and 77 are not allowed for placement when designing with the MCA1200. For the MCA600, locations 25, 35, 45, and 55 are not allowed for placement. (See Figure 3a and 3b for all location assignments).

When placing the 50 ohm driver macros with V_{OL} in the cut-off mode (018 and 019), locations 37, 47, 57, and 67 are not allowed for placement in the MCA1200 while no restrictions exist for the MCA600. See Table 8, page 51 for details on CAD placement. Refer to Section IV-B for more details on the maximum number of drivers allowed.

E. Macro Placement

The V_{CC} current is divided between the two V_{CC} pins. If an imaginary line is drawn between pins 43 and 9 (for 68-pin package), the V_{CC} current to the top half of the array comes from pin 60, while the V_{CC} current to the bottom half of the array is connected to pin 26. The V_{EE} current is also divided between the two V_{EE} pins. By drawing an imaginary line between pin 60 and pin 26 (for 68-pin package), the two halves of the array are subdivided into quadrants.

The macros placed in various locations should be distributed evenly in the array in order to reduce skew delays and maintain noise margins between cells. There are two rules for macro placement:

1. The V_{CC} current of the upper half of the array (pin 60) should be within $\pm 10\%$ of the lower half of the array (pin 26). The typical power dissipation given in the MCA Library can be used for this calculation. This calculation should include the power due to the selected output follower currents. The bias driver power is not used in the calculation.
2. The macro placement should be distributed evenly on a quadrant basis in order to reduce skew delays caused by nonuniform bus drops. The power difference between quadrants (due to I_{CC} and I_{EE} current) must be less than 250 mW. The typical power dissipation given in the MCA may be used for this calculation. This calculation should include the power due to the selected output follower currents. The bias driver power is not used in the calculation. A "dummy" macrocell placement in unused cell locations may be required in some options in order to meet this rule.

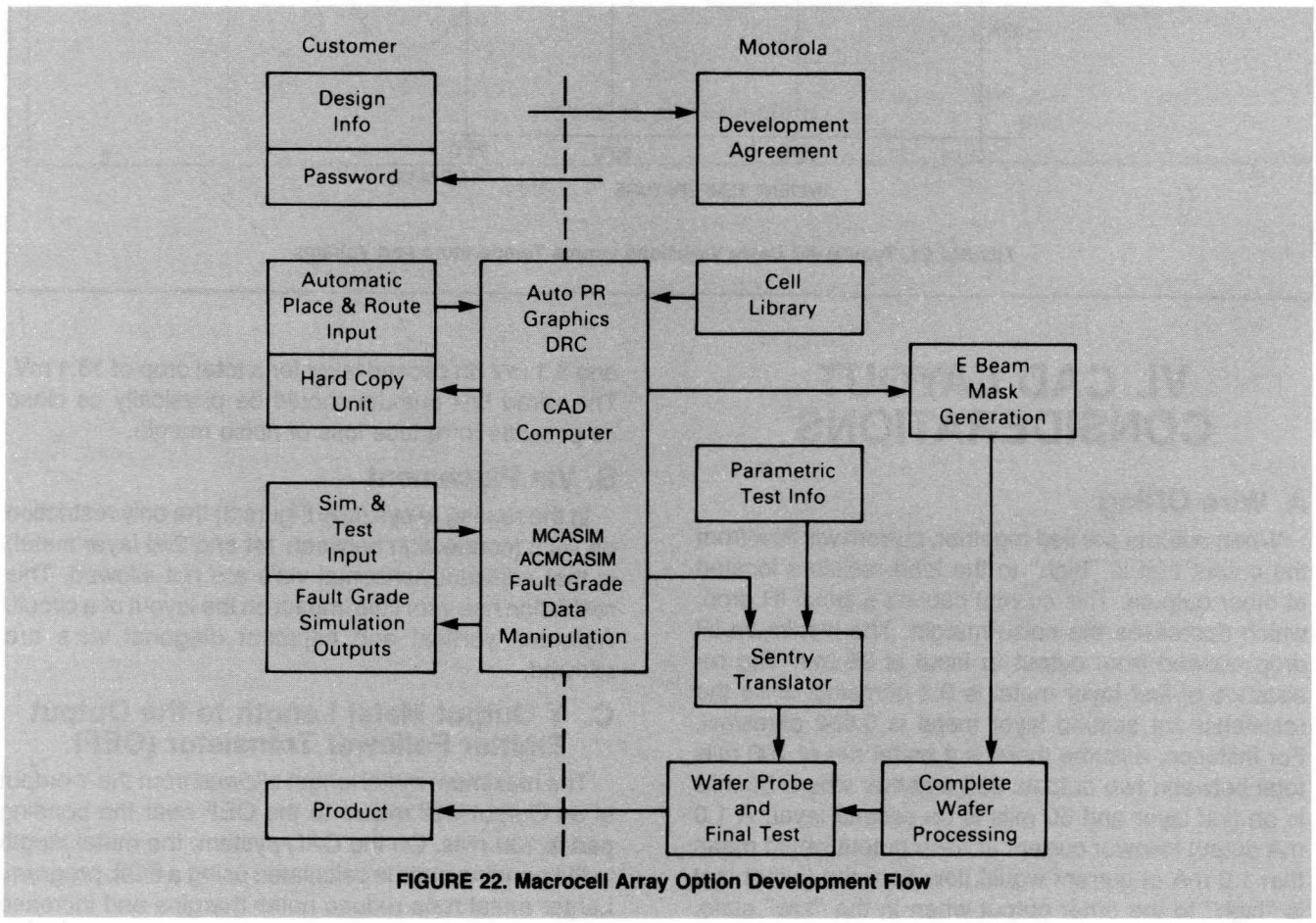


FIGURE 22. Macrocell Array Option Development Flow

VII. MCA OPTION DEVELOPMENT PROCEDURE

The customer needs to partition his system in order to determine the number of options required. A logic diagram for each option is then required, using the macro logic functions in the Macrocell Library. For the MCA1200, each option is constrained to using no more than 48 Major Cell, 32 Interface Cell, and 26 Output Cell macros. Most options will utilize 70 to 100% of the cells. The speed and power dissipation can be found in the library to determine performance.

After the customer is satisfied that the Macrocell Array will provide such benefits as lower system cost, lower power, and faster performance, a development contract is negotiated. The development contract specifies the business aspects such as the number of options, time schedules, and cost. The completion of the development contract is normally accomplished when the customer receives the 10 prototype devices for each option designed.

A Computer Aided Design (CAD) system is used to help the designer with the option development while simplifying the designer/Motorola interface.

The Macrocell Array option development flow is shown in Figure 22. The CAD system utilizes a WACC (Western Area Computer Center) computer at a Motorola facility in Scottsdale, Arizona and operates through the telephone line to graphics equipment at the user's location.

Starting with the development contract, the customer receives a CAD Design Manual and a password to access a Motorola timeshare computer system over phone lines. In order to communicate with the computer, the user is required to lease or buy the following hardware;

1. Tektronix 4014, 4113 or 4115 Computer Display Terminal
2. Tektronix 4662 or 4663 Interactive Digital Plotter
3. Tektronix 4952 Joystick (optional)
4. 300 baud or 1200 baud modem
5. TTY compatible keyboard - printer terminal

The next step requires a CAD Design Manual and a password to access the Motorola Timeshare Computer System over the phone lines. From the Logic Diagram, a CAD file of all the interconnect paths must be written. A test pattern must also be entered into the CAD system so that the logic network can be tested. A program called MCASIM is used to simulate the logic network with the test pattern. For the multiplier design, 29 test vectors were generated with the resulting MCASIM simulation shown in Table 5, page 39.

When the designer is satisfied that the network file is correct based on the results of the simulation, the next step is to lay out the circuit using the Automatic Place and Route software. For the multiplier design, an initial macro placement and pin assignment was entered into the CAD system. The Automatic Place software found a better macro placement.

Once the logic drawing for the MCA option is complete, the following design steps should be followed:

1. Build a CAD file (SNETWORK) of all the interconnect paths between macrocells and I/O pads.
2. Generate a functional test sequence (SPATTERN file) file for checking the option.
3. Run a CAD (MCASIM) simulation checking the interconnect net list against the test sequence.
4. When the test sequence verifies proper circuit operation, use the automatic place and route software to generate a macrocell array option layout.
5. Manually route any interconnects not covered by routing software. For some options, a manual place and route may be used. For manual routing, do the following steps:
   a. Place all macros on a worksheet in a manner that provides the shortest interconnects.
   b. Generate a worksheet (using plotter) showing all the I/O ports of the placed macros.
   c. Interconnect all the I/O ports of the macros according to the logic diagram.
   d. After the routing is completed, use the CRT terminal to transfer the routing information into the computer or use the plotter to digitize the channel routing.
   e. Generate a CAD plot and verify that the routing agrees with the logic diagram.
6. Generate a wiring list file based on the actual CAD interconnect.
7. Run a CAD simulation to verify that the actual layout agrees with the expected output pattern.
8. Run a fault grade program to qualify the test sequence.
9. Add additional test vectors to achieve the highest test grading possible.
10. Finalize the option design by selecting input pulldown resistors, input compensation networks, and macro output follower currents.
11. Generate ac test vectors for determining propagation delays of critical paths. These vectors should have only one input changing at a time (per cycle) since this is a requirement of final test equipment.
12. Run AC Simulation software to determine worst case propagation delays.
13. Notify Motorola the design is complete.

After completing an option design, information in the CAD system is converted to pattern generation and to IC masks. Then the metal masks are used to complete the IC processing. The circuits are then tested and shipped to the customer.

The prototypes are then tested by the customer to verify the parts. A production contract is then negotiated for volume deliveries.

Motorola's Macrocell Array CAD Customer Interface presently provides the following array design features:

1. All worksheets for option development
2. Interactive graphics for accepting design information
3. Full editing for design corrections or improvements
4. Error checking to catch design rule violations
5. Simulation programs to verify logic accuracy and metal interconnects
6. Customer documentation for each option
7. Test programming aids through simulation and fault grade
8. Macrocell Array automatic route and place software to simplify option development
9. AC Simulation software to provide worst case propagation delay times based on the ac test vectors

VIII. HARDWARE DESCRIPTION REQUIRED FOR OPTION DEVELOPMENT

The Tektronix 4014/4113/4115 Computer Display Terminal permits the user to interface with WACC computers in a manner understandable by both computer and human operator. By typing on the keyboard, a macrocell array option designer can instruct CAD software to perform various macrocell array design functions. The CAD system computer response is returned to the operator by way of a display screen, either alphanumerically or graphically. The terminal also communicates with the plotter unit and acts as a link between computer and plotter.

Tektronix 4662 or 4663 Interactive Plotters generate macrocell array worksheets and permanent design records. The plotters may also be used to digitize routing information into the CAD system. The 4662 accepts paper sizes up to 11 by 17 inches, while the larger 4663 handles paper up to 17 by 22 inches. Both the 4662 and 4663 plotters are connected in series between the 4014/4113/4115 graphics terminal and the telephone modem.

Several CAD array design operations do not require graphics interface. These include logic simulation, fault grade, design verification, and generating a net list for automatic route and place software. Although the 4014-1 terminal and hard copy unit could be used, a TTY compatible terminal (TI Silent 700 or equivalent) has proven more convenient. The terminal must communicate in ASCII format and operate at 300 or 1200 baud rate. The modem used to interface to the telephone lines is a Bell 103/113 or equivalent.

IX. PACKAGING

The MCA1200ECL and MCA600ECL are offered in both a 68-pin leadless package (JEDEC standard "type A") Figure 23, and a 72-pin grid-array package, Figure 25.

The leadless package has 17 connection terminals per side on 0.05″ centers. The IC chip mounts to a ceramic base measuring 0.95 inches on a side. Gold-plated metal on the base piece routes signals and power from the package edge to the IC chip. The Macrocell Array chip is die-attached to the package using a preform which provides an excellent thermal interface between the die and the ceramic. The thermal resistance of the device from the junction to the case is less than 5°C/W. Figure 11 shows the chip wire bonded to the package. A ceramic cover fits on top of the package to provide a hermetic seal.

The MCA1200ECL is also offered in a special 68-pin leadless package as shown in Figure 24. This package contains an extra buried layer with a ground plane that connects V_{CCO} pins 3, 15, 20, and 66 together. There are four additional V_{CCO} contacts on the heat sink side of the package that allow four parallel V_{CCO} connections to be made to the PC board when used with a special AMP socket (part #55254-1) with a grounded hold down frame. This package is made available to users that want to reduce the inductive noise generated by simultaneous switching.

The MCA600ECL is also offered in both the 40-pin and the 28-pin dual in-line ceramic package (CERDIP). The package outline for these packages is shown in Figure 26.

X. HEAT SINKS AND THERMAL CHARACTERISTICS

The worst case propagation delay in the Macrocell Library is specified for a maximum junction temperature of 115°C. In order to meet this specification for the MCA1200, a heat sink and air flow are required. The DC levels for the MCA1200 are specified with the MCA device having an attached heat sink (WAKEFIELD #4493 or equivalent) and a transverse air flow of 1000 LFPM resulting in a ΘJA of 10 ± 2°C/watt. In still air with no heat sink attached, the average ΘJA is 36°C/watt in the 68-pin leadless package and 29°C/watt in the 72-pin grid-array.

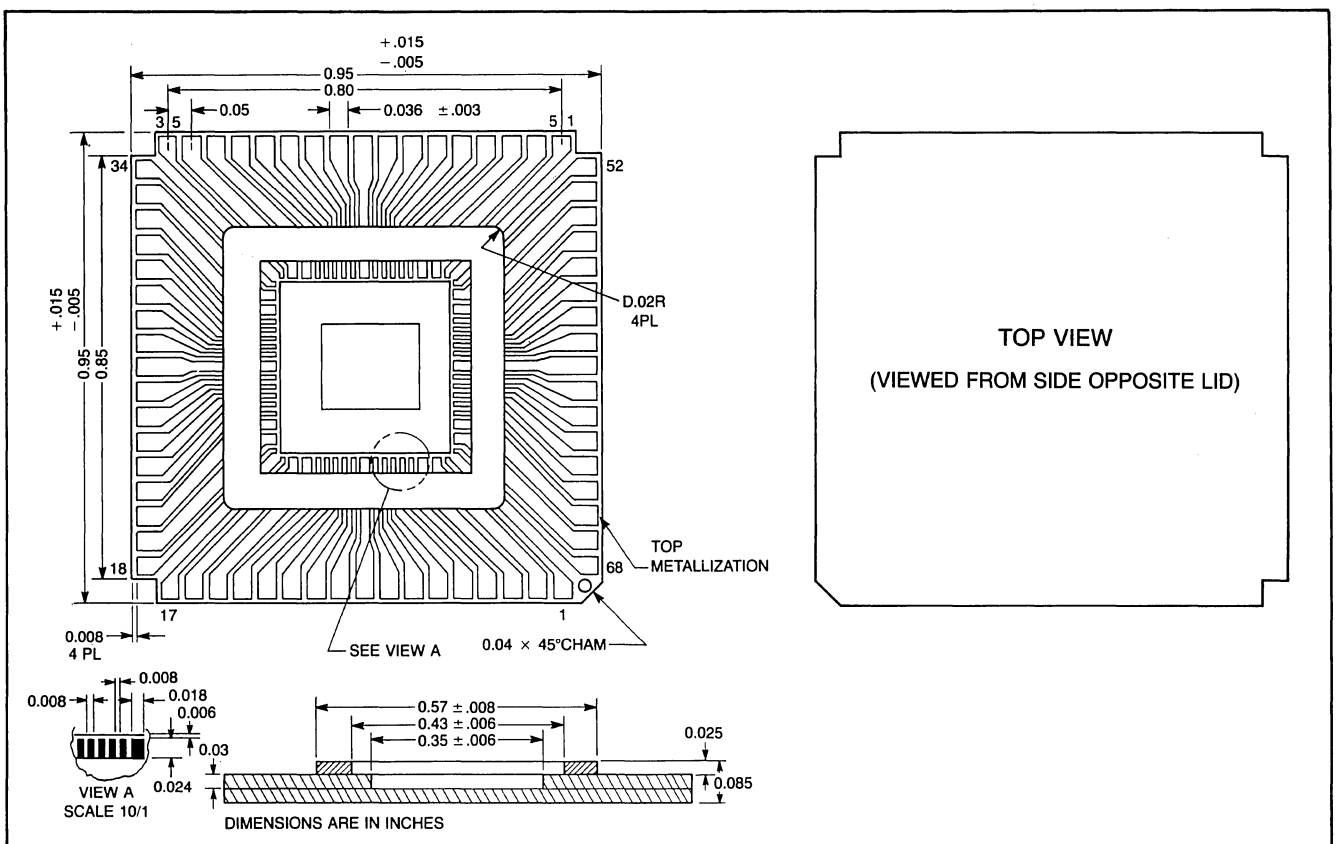


FIGURE 23. 68-Pin Leadless Package Case 745

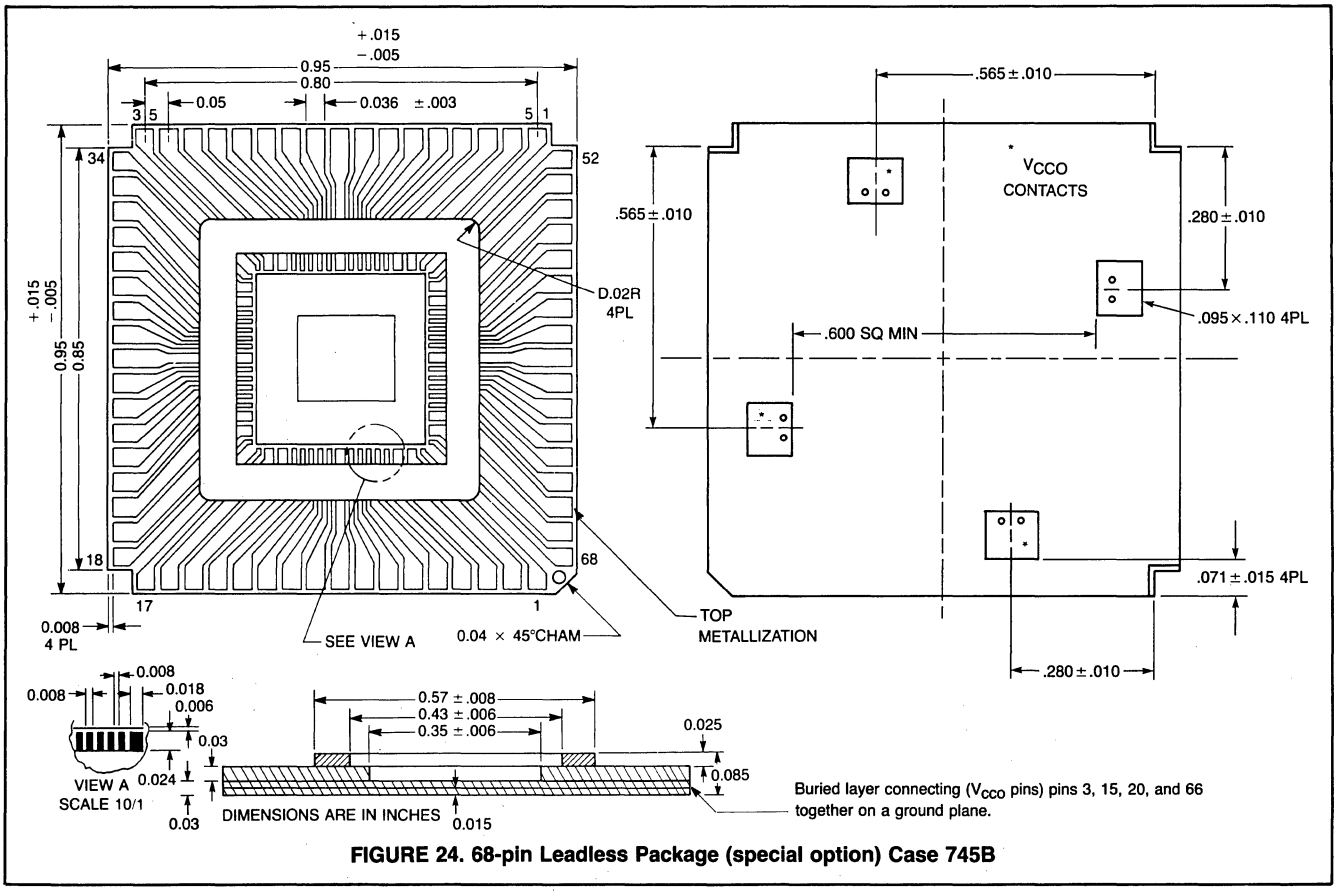
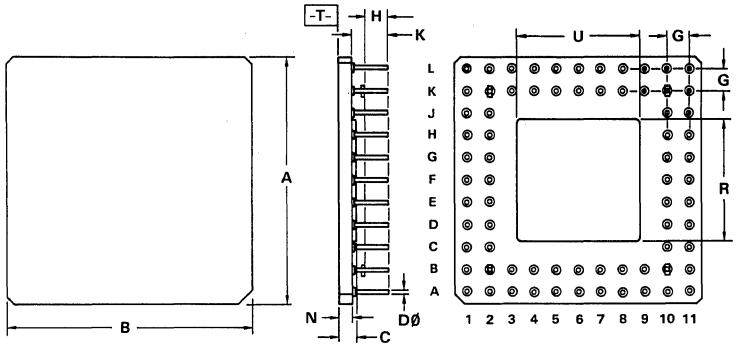


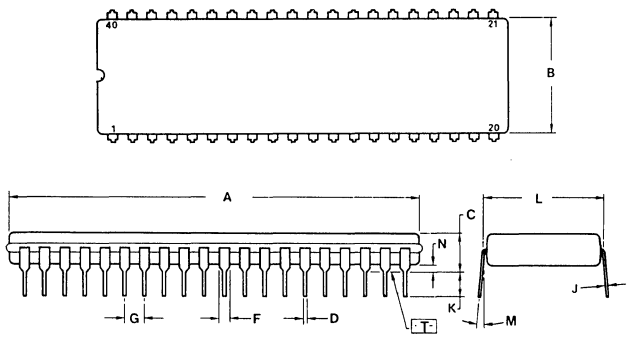
FIGURE 24. 68-pin Leadless Package (special option) Case 745B



NOTES:
1. DIMENSIONS A AND B ARE DATUMS AND -T- IS A DATUM SURFACE.
2. POSITIONAL TOLERANCE FOR LEADS (36 PL):
   ⌖ | ϕ 0.13 (0.005) Ⓜ | T | A Ⓢ | B Ⓢ
   FOR LEADS (36 PL):
   ⌖ | ϕ 0.13 (0.005) Ⓜ | T | B Ⓢ | A Ⓢ
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
4. CONTROLLING DIMENSION: INCH.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	29.34	30.35	1.155	1.195
B	29.34	30.35	1.155	1.195
C	1.90	2.79	0.075	0.110
D	0.43	0.48	0.017	0.019
G	2.54 BSC		0.100 BSC	
H	2.79	3.04	0.110	0.120
K	4.19	4.69	0.165	0.185
N	1.90	2.41	0.075	0.095
R	13.72	13.97	0.540	0.550
U	13.72	13.97	0.540	0.550

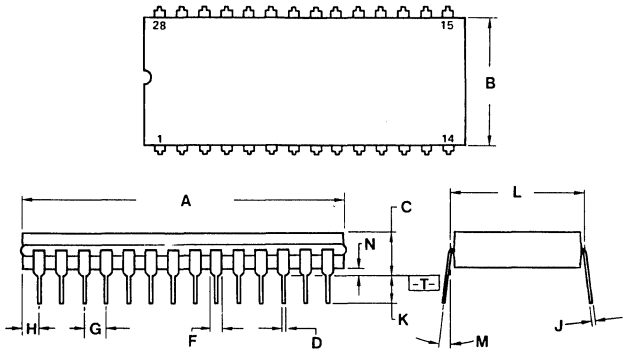
FIGURE 25. Case 785-02 72-Pin Grid-Array Package



NOTES:
1. DIM -A- IS DATUM.
2. POSITIONAL TOLERANCE FOR LEADS:
   ⌖ | Ø 0.25(0.010) Ⓜ | T | A Ⓜ
3. -T- IS SEATING PLANE.
4. DIM L TO CENTER OF LEADS WHEN FORMED PARALLEL.
5. DIMENSIONS A AND B INCLUDE MENISCUS.
6. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	51.31	53.24	2.020	2.096
B	12.70	15.49	0.500	0.610
C	4.06	5.84	0.160	0.230
D	0.38	0.56	0.015	0.022
F	1.27	1.65	0.050	0.065
G	2.54 BSC		0.100 BSC	
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	15.24 BSC		0.600 BSC	
M	5°	15°	5°	15°
N	0.51	1.27	0.020	0.050

Case 733 28-Pin CERDIP



NOTES:
1. DIM -A- IS DATUM.
2. POSITIONAL TOL FOR LEADS:
   ⌖ | Ø 0.25 (0.010) Ⓜ | T | A Ⓜ
3. -T- IS SEATING PLANE.
4. DIM A AND B INCLUDES MENISCUS.
5. DIM -L- TO CENTER OF LEADS WHEN FORMED PARALLEL.
6. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	36.45	37.85	1.435	1.490
B	12.70	15.37	0.500	0.605
C	4.06	5.84	0.160	0.230
D	0.38	0.56	0.015	0.022
F	1.27	1.65	0.050	0.065
G	2.54 BSC		0.100 BSC	
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	15.24 BSC		0.600 BSC	
M	5°	15°	5°	15°
N	0.51	1.27	0.020	0.050

Case 734 40-Pin CERDIP

FIGURE 26. CERDIP Packages

Table 4a shows a listing of some of the manufacturers of heat sinks and thermal epoxy. The recommended heat sinks are listed with the manufacturer's part number. Figure 27a shows the typical thermal characteristics for the MCA1200 using two different heat sinks.

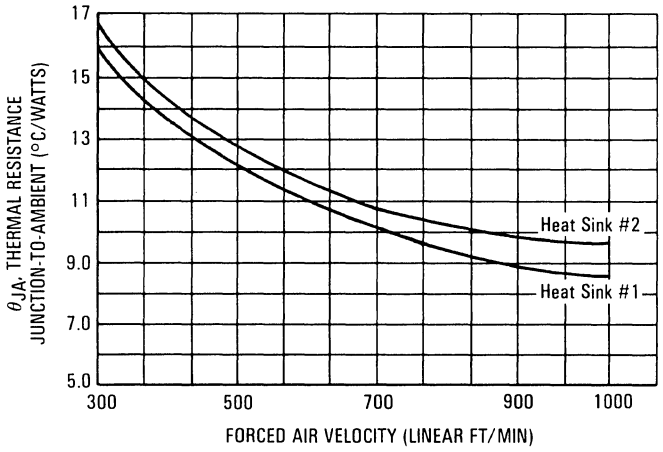
The MCA600ECL requires only 500 LFPM of air flow (no heat sink required) to meet the DC levels specified. However, the junction temperature must be maintained at less than 115°C in order to meet the AC specification. Figures 27 b and c show the typical thermal characteristics for the MCA600 for 3 different packages.

The typical ΘJA for the 40-pin and 28-pin CERDIP package is 28°C/watt and 500 LFPM. In still air, the ΘJA increases to 36°C/watt for the 40-pin and 42°C/watt for the 28-pin CERDIP. For the 68-pin leadless package, the MCA600 has a typical ΘJA of 22°C/watt with 500 LFPM of air flow and 19°C/watt with 1000 LFPM. In order to meet the maximum junction temperature of 115°C for AC specifications, a heat sink and air flow may be required. For the 68-pin leadless package, the MCA600 has a typical ΘJA of 17°C/watt with 500 LFPM of air flow and a heat sink with vertical fins. (#4493 in Table 4a).

To calculate the junction temperature, the equation shown in Figure 27 should be used.

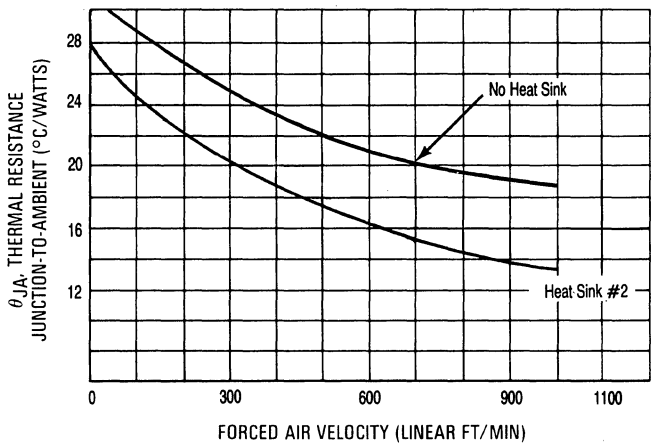
FIGURE 27. TYPICAL THERMAL CHARACTERISTICS

a) For MCA1200 in a 68-pin leadless package

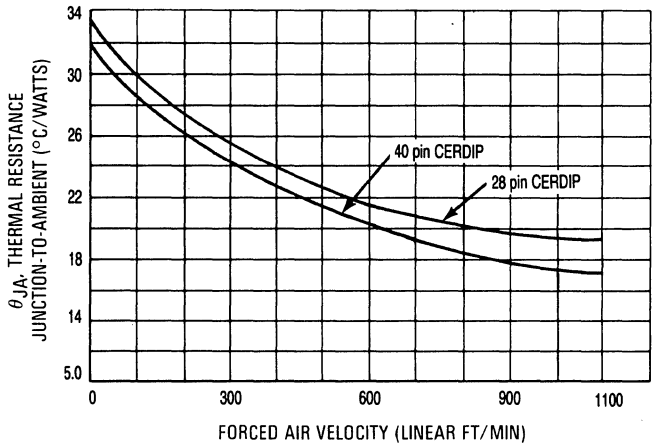


Heat Sink #1 is from THERMALLOY #15832-1. Horizontal Fins. 0.563 inches square, Model NO. 2284C.
Heat Sink #2 is from WAKEFIELD #4493. Vertical Fins. 0.5 inches square.
NOTE: $T_J = (\Theta_{JA})(P_D) + T_A$ WHERE T_J is the Junction Temperature. T_A is the Ambient Temperature.
$P_D = (I_{EE})(V_{EE}) + (15mW)$ (number of 50 Ω outputs).

b) For MCA600 in 68-pin leadless package



c) For MCA600 in 28- and 40-pin package



XI. CONNECTORS FOR 68 PIN LEADLESS PACKAGE

The package is mounted upside down from conventional IC practice with the base of the chip on the top side away from the PC board. A heat sink (such as the Wakefield # 4493) is attached (by customer) to the package on the same ceramic piece as the IC chip for very efficient heat transfer. Figure 28 shows the heat sink attached to the package being mounted in a connector manufactured by AMP. This connector can be soldered to the PC board or held in place with a mounting bolt. The leadless package is held in the connector with a spring clip. There are 68 metal tabs near the connector base providing access to all 68 package pins in order to facilitate testing and troubleshooting.

Another method of mounting the leadless package to the PC board is shown in Figure 29. The method consists of mounting stand-off pins or metal clips, manufactured by Berg Electronics, to the package. The metal clips come in strips that are connected to the leadless package by heating the strip that has been solder tinned. The strip is then clipped and connected to the PC board by using reflow soldering techniques.

Table 4b shows a listing of some of the manufacturers with part numbers for package connectors.

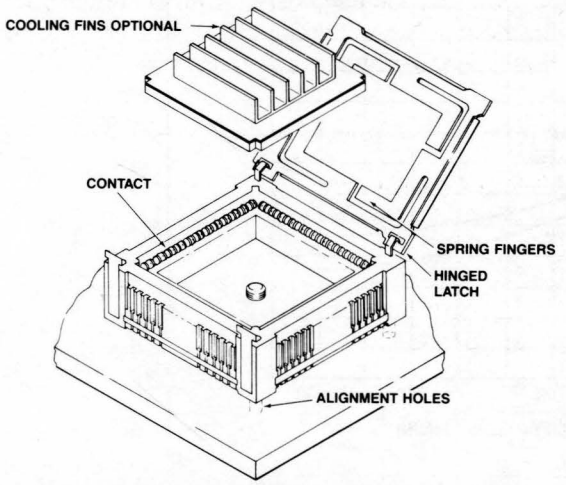


FIGURE 28. Leadless Package With Connector

TABLE 4. — Manufacturers of Related Materials for Use with the 68-Pin Leadless Package (Type A) and 72-Pin Grid Array

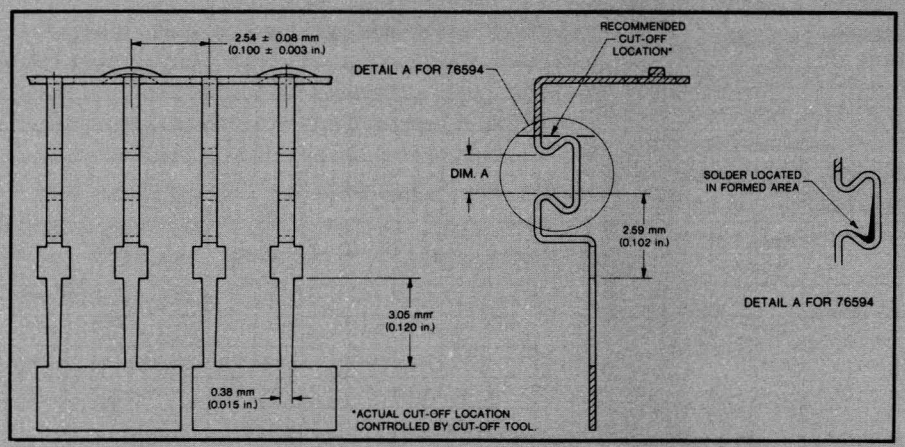
(a) Heat Sinks & Thermal Epoxy

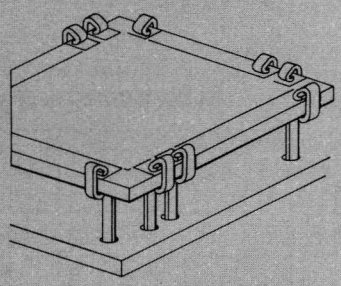
Manufacturer	Product Description
Thermalloy, Inc. Dallas, TX	Heat sink with horizontal fins. 0.563 in. square base Model 2284C
EG&G Wakefield Engineering	Heat sink with vertical fins. .5 in. square base Part No. 4493
Ablestik Labs Gardena, CA	Heat exchanger attachment epoxy Part No. 2931T

(b) Package to Circuit Board Connector/Socket and LSI Clips

Manufacturer	Product Description
AMP Inc. Harrisburg, PA 17105	Surface to Solder Tail Socket Part #55159 #55254 w/Ground Clips
Berg Electronics New Cumberland, PA 17070	LSI CLIPS - Surface Mount, Part #76525-027 w/o solder Thru Board Mount 76529-003 w/o solder
Augat Inc. Attleboro, MA 02703	Surface to Surface Socket Part #CCS68-1G1 Pin Grid Array Socket Part #PPS72-AG1D
Electronic Molding Corp. Woonsocket, RI 02895	Pin Grid Array Sockets

Accepts 1.57mm (0.062") thick chip
Thru-board Mount—Part Number 76594 — with solder
76529 — without solder





Material: ½ Hard Phosphor Bronze
Plating: 7.6μm (300μ") to 12.70μm (500μ") tin lead.

DUAL DIMENSIONS ARE SHOWN — AS: MILLIMETER / INCH

FIGURE 29. Leadless Package With Stand-Off Pins

XII. APPLICATIONS

Probably one of the most important features of the design is the logic flexibility provided by the Macrocell Library. The system value of the array can be shown by examining actual circuit options from the M10900 family that were developed using the microcell array.

With the Macrocell array it is possible to design system functions of twice the complexity and twice as fast as previous existing standard product. For instance, M10800 family has standard product with functions available in 4-bit slice configurations. The M10900 family produces 8-bit slice configurations at about twice the speed (or half the propagation delay).

Figure 30 shows the block diagrams for four members of the M10900 family along with a description of the main features. The design procedure will be described later for a fifth member of the M10900 family, the MC10901, 8 by 8-bit expandable multiplier (see Figure 31).

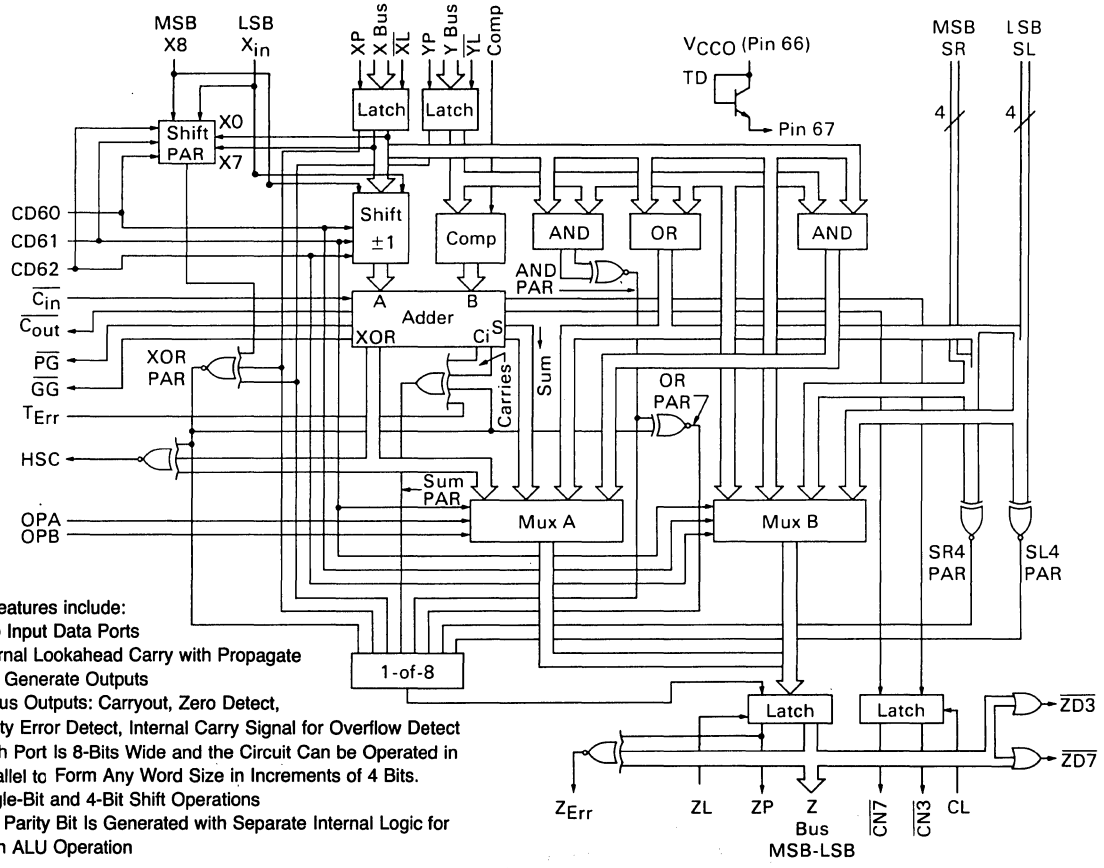
The MC10900 is an 8-bit ALU containing 9-bit data ports with full parity checking generated for each ALU operation independent of the ALU result. (see Figure 30a). Also a one bit shift (left or right) can be performed on the X bus for each ALU operation. A 4-bit shifter is included as an ALU function. Input and output latches exist for a high speed pipelined architecture. More than 94% of the cells in the MCA 1200 were utilized.

The MC10902 is an 8-bit binary/BCD ALU containing 3 input data ports with latches (see Figure 30b). More than 97% of the cells in the MCA1200 array were utilized. The ALU operations include binary and BCD addition and subtraction, shift left, shift right, increment, transfer, invert and various logic operations. The propagation delay for any ALU function from data in to data out is only 17.9 ns maximum.

The MC10904 is an 8-bit expandable micro-code sequencer which utilizes 92% of the cells in the MCA1200 (see Figure 30c). This circuit controls processor operations by generating the addresses and sequencing pattern for microprogram control storage. The sequencer contains a 4 level subroutine stack, a counter for repeating instructions or sequences, an incrementer, and instructions for jumps, conditional branching and multi-way branch.

FIGURE 30. M10900 Family of Standard Options

(a) MC10900 — 8-BIT PARITY ALU SLICE BLOCK DIAGRAM



Main features include:

- Two Input Data Ports
- Internal Lookahead Carry with Propagate and Generate Outputs
- Status Outputs: Carryout, Zero Detect, Parity Error Detect, Internal Carry Signal for Overflow Detect
- Each Port Is 8-Bits Wide and the Circuit Can be Operated in Parallel to Form Any Word Size in Increments of 4 Bits.
- Single-Bit and 4-Bit Shift Operations
- The Parity Bit Is Generated with Separate Internal Logic for Each ALU Operation

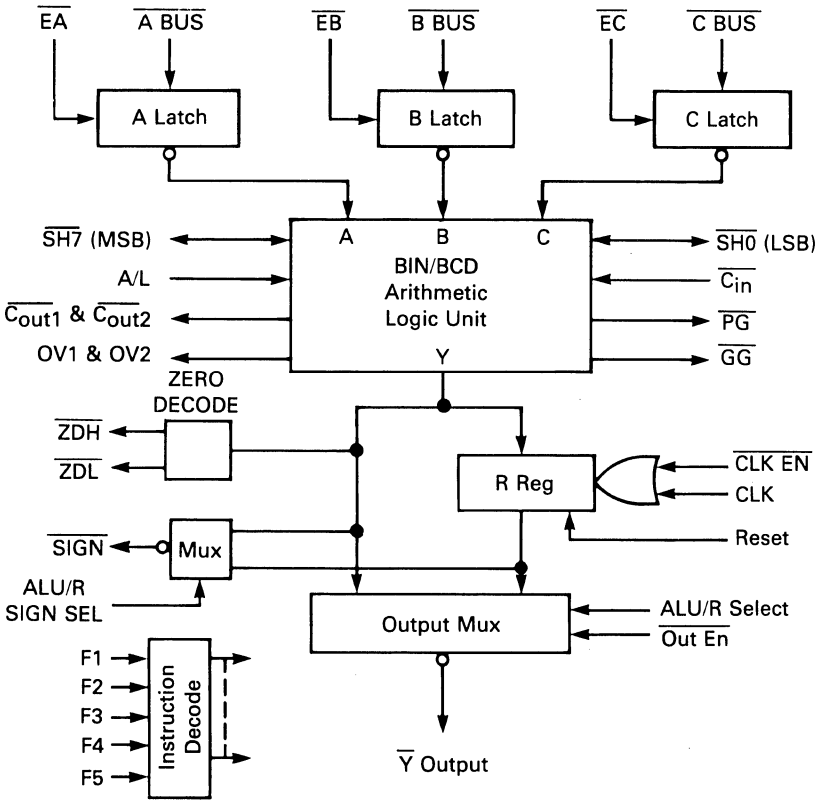
The MC10905 is a 16-bit error detection and correction unit that is expandable to 96 bits (see Figure 30d). The device is the link between memory and the CPU which will improve memory reliability by a minimum of 20 to 300 and greater depending on memory size. All single bit errors are corrected and all double bit errors are detected. The MC10905 is designed with a high speed pipelined architecture with on-chip latches on the input data, output data, check bits, and error flags. An error can be detected in only 21 ns (Max) in the 32-bit configuration (requires only 2 MC10905's) and corrected in 28 ns (Max) while the check bits can be generated in only 17 ns (Max). The MC10905 can also be used in the check-only mode with the delay from data-in to data-out of only 7.6 ns (Max). In the event of an error, the error flag will be activated generating an interrupt to the CPU so that the data can be rapidly corrected by switching the NC (No correct) pin from the high to low state. The MC10905 uses approximately 93% of the macrocells available in the MCA1200 array.

A. Multiplier Design Example

An example of the design procedure required for option development is shown in this section. The circuit is a high-speed array multiplier (MC10901) that is completely expandable in both directions.

The first step was to determine the highest number of bits that could be multiplied together using the cell library with various multiplier algorithms. It was determined that an 8 x 8 array would use a high percentage of the array and achieve an optimum speed. A block diagram of the design is shown in Figure 31. The indicated speed of the array was determined after the design was completed.

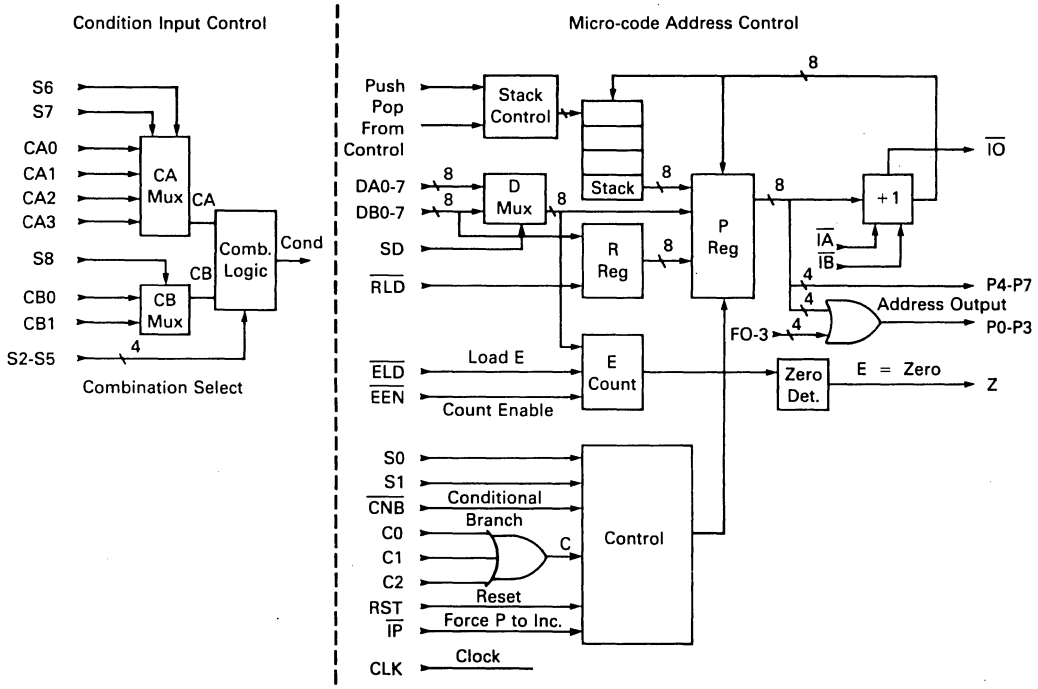
After determining the best multiplier partitioning, the logic diagram using the available macros in the Macrocell Library was completed. Figure 32 shows the completed logic drawing and a list of macros used in the design. Each of the macros is drawn using the labeling shown in the cell library.



Main features include:

- 34 functions including logic, shift, and both binary and BCD arithmetic.
- Internal 8-bit accumulator with externally available reset, clock, and clock enable.
- Internal look-ahead carry with Propagate and Generate outputs.
- Zero detects for upper and lower 4 bits.
- Select pin for logic or arithmetic shift right.

FIGURE 30. (Cont.)
(b) MC10902 — 8-BIT BINARY/BCD ALU SLICE BLOCK DIAGRAM



Main features include:

- 4 level subroutine stack that can be pushed and popped simultaneously.
- Two direct data inputs for jump and conditional branch destinations.
- A special P counter pin ($\overline{IP}$) simplifies loading RAM writeable macroprogram memory. The input can also be used to hold the system on a microinstruction for diagnostics.
- Multi-way branch on the lowest 4 P output bits allows a 16-way branch.
- Six branch condition inputs can be combined in 14 logic patterns to minimize external branch control logic.
- R register for holding microprogram address information.
- An 8-bit counter for repeating instructions or sequences. Can also be used to count events, conditions, or time.

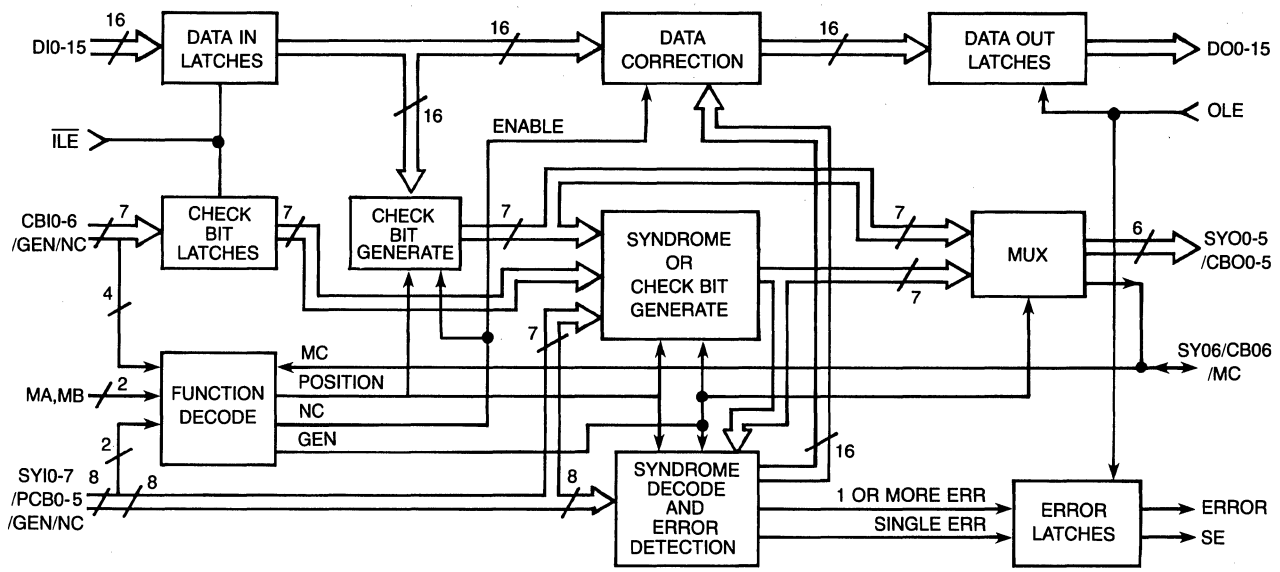
FIGURE 30. (Cont.)
(c) MC10904 — 8-BIT MICRO-CODE SEQUENCER BLOCK DIAGRAM

Each of the logic blocks is coded with symbols in order to differentiate the similar macros. So far, the amount of time required to design the option is the same as it would take when designing the system using standard MECL 10K or some other logic family.

The rest of the design process extensively uses the computer software in the Motorola time share CAD system. After signing the development contract, the customer receives a CAD Design Manual with detailed information on the CAD software for developing the design option.

Next, the circuit needs to be simulated in order to verify that the design performs the proper multiplication function. A SNETWORK file is generated from all the interconnect paths in a format defined by a program called MCASIM. A test pattern for the design is entered in a SPATTERN file while the order for printing the input and output pins is entered into a SCOMMAND file. A simulation of the circuit is then performed using MCASIM. The results of the simulation are shown in Table 5. Only 29 vectors were needed to initially test the multiplier design. The input pins are labeled with an "I" with each vector defined in the SPATTERN file. The output pins are labeled with a "P" with the results generated by MCASIM simulation. These results are checked with the expected pattern. The first two inputs, I34 and I35, control two's complement, or sign magnitude; input I53 is for sign bit expansion; I30 through I47 are the X7 through X0 data inputs; I29 through I45 are the Y7 through Y0 data inputs; I24 through I62 are the M7 through M0 expansion inputs; I32 through I64 are the K7 through K0 expansion; and P23 to P02 form the multiplication result (MSB to LSB).

After the simulation results have been verified, the circuit is ready to be automatically interconnected using the Automatic Place and Route software (called AUTOPR). Figure 33 shows a flow diagram of the Automatic Place and Route software in the CAD system and the interaction between the user and Motorola. For

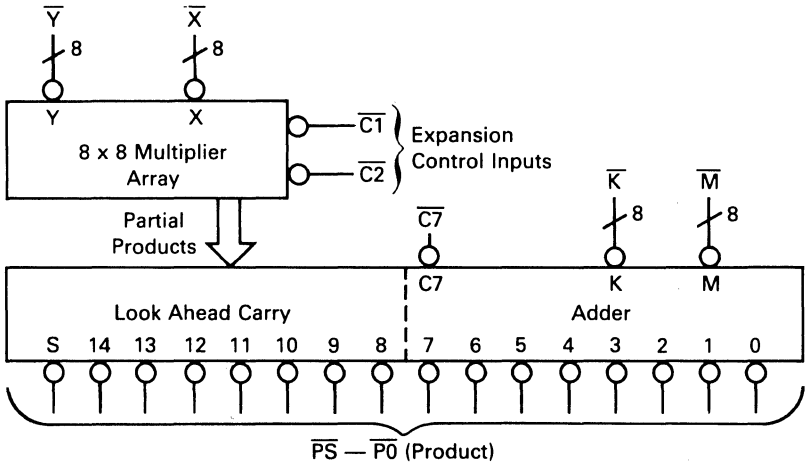


Main features include:

- High speed pipelined architecture
- On-chip latches for input data, check bits, output data, and error flags
- Separate input and output data bus for high speed operation
- Expandable to 96 bits
- Full single error correction and double error detection
- No data correct mode while checking for errors
- Very fast error detect
  - For 16 bits, 17.2 ns MAX
  - For 32 bits, 21 ns MAX
  - For 48 through 96 bits, 28.2 ns MAX
- Very fast data correct
  - For 16 bits, 19.7 ns MAX
  - For 32 bits, 28 ns MAX
  - For 48 through 96 bits, 31.3 ns MAX
- Very fast check bit generate
  - For 16 bits, 10.7 ns MAX
  - For 32 bits, 17 ns MAX
  - For 48 through 96 bits, 17.8 ns MAX

FIGURE 30. (Cont.)

(d) MC10905 — 16-BIT ERROR DETECTION AND CORRECTION UNIT BLOCK DIAGRAM



SIZE	8 X 8	16 X 16	24 X 24	32 X 32
PACKAGES	1	4	9	16
DELAY (NS MAX)	24.3	51.8	81.5	111.2

FIGURE 31. 8 X 8 Array Multiplier, MC10901

the multiplier design, an initial macro placement and pin assignment were entered into the FIX file. (The FIX file also contains package type, mA current setting and other miscellaneous items). For designs that use greater than 90% of the array, an initial placement will usually result in a more routable design. For the initial placement, a total wire length (Figure of merit) was calculated by the Automatic Placement program. Then, the initial placement was eliminated from the FIX file and the Automatic Placement program generated a new placement that had a smaller wire length (25,000). Using the computer generated placement, the Automatic Routing program generated the complete interconnect. Only 90 seconds of CPU time was required to automatically route the design. The automatic placement required 63 seconds of CPU time.

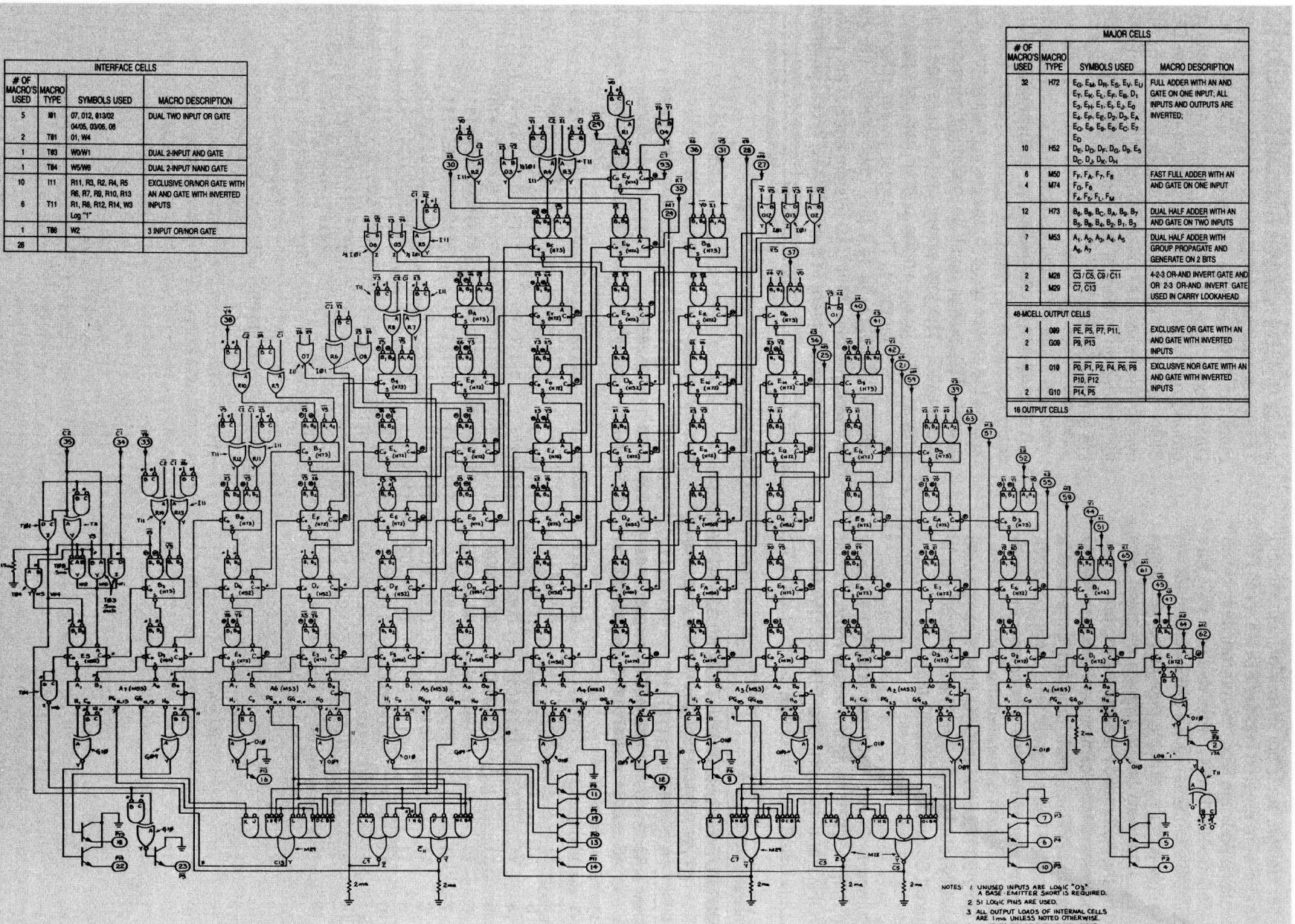
The Compare Circuit Program (CMPCKT) compares the SNETWORK file to the actual routed circuit (DNETWORK) and converts the FIX, SCOMMAND and SPATTERN to MAMP, DCOMMAND and DPATTERN, respectively. Input pad pulldown resistors and output current settings are updated using the MODAMP command. A VIOLATE command checks all ground rule violations. If no violations exist, the DESIGN file is converted by Motorola to an E-BEAM system that is used to make the metal masks required for the design option. A test tape is generated from the simulation results.

A manual power calculation for each quadrant of the design is shown in Table 6. The CAD system also calculates the power of each quadrant and the total IEE current. The power must be balanced as stated in Section VI-E. The total power of the upper half of the array is 6.6% less than the bottom half (this satisfies the ±10% tolerance). The largest power difference between quadrants is 84.4 mW (this satisfies the 250 mW requirement). The CAD system checks the power balance requirement in the VIOLATE check program.

TABLE 5. — Results of MCASIM Simulation for Multiplier Design

OUTPUT FOR NEW MULT ON 80.323 AT 13.05.54

	$\overline{C1}$ $\overline{C2}$	$\overline{C7}$	$\overline{X}$	$\overline{Y}$	$\overline{M}$	$\overline{K}$	$\overline{P}$
	33	5	33344554	23333444	22255566	32526566	2211111110100000
	45	3	06701217	93189245	47597812	28613554	3286439128067452
1	11	1	11111111	00000000	11111111	11111111	1111111111111111
2	11	1	11111110	00000000	11111111	11111111	1111111100000000
3	11	1	11111101	00000000	11111111	11111111	1111111000000001
4	11	1	11111011	00000000	11111111	11111111	1111110000000011
5	11	1	11110111	00000000	11111111	11111111	1111100000000111
6	11	1	11101111	00000000	11111111	11111111	1111000000001111
7	11	1	11011111	00000000	11111111	11111111	1110000000011111
8	11	1	10111111	00000000	11111111	11111111	1100000000111111
9	11	1	01111111	00000000	11111111	11111111	1000000001111111
10	11	1	00000000	11111111	11111111	11111111	1111111111111111
11	11	1	00000000	11111110	11111111	11111111	1111111100000000
12	11	1	00000000	11111101	11111111	11111111	1111111000000001
13	11	1	00000000	11111011	11111111	11111111	1111110000000011
14	11	1	00000000	11110111	11111111	11111111	1111100000000111
15	11	1	00000000	11101111	11111111	11111111	1111000000001111
16	11	1	00000000	11011111	11111111	11111111	1110000000011111
17	11	1	00000000	10111111	11111111	11111111	1100000000111111
18	11	1	00000000	01111111	11111111	11111111	1000000001111111
19	11	1	11111111	11111111	11111111	00000000	1111111100000000
20	11	1	11111111	11111111	00000000	11111111	1111111100000000
21	10	1	01111111	11111111	11111111	11111111	1000000001111111
22	01	1	11111111	01111111	11111111	11111111	1000000001111111
23	00	1	00000000	00000000	11111111	11111111	0000000011111111
24	00	1	01111111	11111111	11111111	11111111	0000000001111111
25	00	1	11111111	01111111	11111111	11111111	0000000001111111
26	01	1	11111111	11111111	11111111	11111111	1111111111111111
27	10	1	11111111	11111111	11111111	11111111	1111111111111111
28	11	0	11111111	11111111	11111111	11111111	1111111101111111
29	11	1	00000000	00000000	00000000	00000000	0000000000000000



INTERFACE CELLS			
# OF MACRO'S USED	MACRO TYPE	SYMBOLS USED	MACRO DESCRIPTION
5	I01	07, 012, 013/02 04/05, 03/06, 08	DUAL TWO INPUT OR GATE
2	T01	01, W4	
1	T03	W3/W1	DUAL 2-INPUT AND GATE
1	T04	W5/W6	DUAL 2-INPUT NAND GATE
10	I11	R11, R3, R2, R4, R5 R6, R7, R8, R10, R13	EXCLUSIVE OR/NOR GATE WITH AN AND GATE WITH INVERTED INPUTS
6	T11	R1, R8, R12, R14, W3 Log "1"	
1	T08	W2	3 INPUT OR/NOR GATE
28			

MAJOR CELLS			
# OF MACRO'S USED	MACRO TYPE	SYMBOLS USED	MACRO DESCRIPTION
32	H72	E_G, E_M, D_R, E_S, E_V, E_U E_T, E_K, E_C, E_P, E_B, D_I E_3, E_N, E_1, E_J, E_J, E_Q E_A, E_P, E_E, D_D, D_B, E_A E_O, E_B, E_B, E_B, E_C, E_7 E_D	FULL ADDER WITH AN AND GATE ON ONE INPUT; ALL INPUTS AND OUTPUTS ARE INVERTED;
10	H52	D_E, D_D, D_F, D_G, D_B, E_5 D_C, D_A, D_K, D_H	
6	M50	F_F, F_A, F_7, F_8	FAST FULL ADDER WITH AN AND GATE ON ONE INPUT
4	M74	F_G, F_8 F_4, F_5, F_L, F_M	
12	H73	B_9, B_8, B_C, B_A, B_9, B_7 B_5, B_8, B_4, B_2, B_1, B_3	DUAL HALF ADDER WITH AN AND GATE ON TWO INPUTS
7	M53	A_1, A_2, A_3, A_4, A_5 A_6, A_7	DUAL HALF ADDER WITH GROUP PROPAGATE AND GENERATE ON 2 BITS
2	M28	$\overline{C3}$ / $\overline{C5}$, $\overline{C6}$ / $\overline{C11}$	4-2-3 OR-AND INVERT GATE AND OR 2-3 OR-AND INVERT GATE USED IN CARRY LOOKAHEAD
2	M29	$\overline{C7}$, $\overline{C13}$	
48-MCELL OUTPUT CELLS			
4	009	$\overline{P_E}$, $\overline{P5}$, $\overline{P7}$, $\overline{P11}$,	EXCLUSIVE OR GATE WITH AN AND GATE WITH INVERTED INPUTS
2	G09	$\overline{P8}$, P13	
8	010	$\overline{P0}$, $\overline{P1}$, $\overline{P2}$, $\overline{P4}$, $\overline{P6}$, $\overline{P8}$ $\overline{P10}$, $\overline{P12}$	EXCLUSIVE NOR GATE WITH AN AND GATE WITH INVERTED INPUTS
2	G10	$\overline{P14}$, $\overline{P5}$	
16 OUTPUT CELLS			

NOTES:
1. UNUSED INPUTS ARE LOGIC "0" A BASE-EMITTER SHORT IS REQUIRED.
2. 51 LOGIC PINS ARE USED.
3. ALL OUTPUT LOADS OF INTERNAL CELLS ARE 1ma UNLESS NOTED OTHERWISE.
4. ALL OUTPUTS OF OUTPUT CELLS ARE LOADED WITH 50 Ω LOADS.

FIGURE 32. 8 X 8 Multiplier Logic Drawing

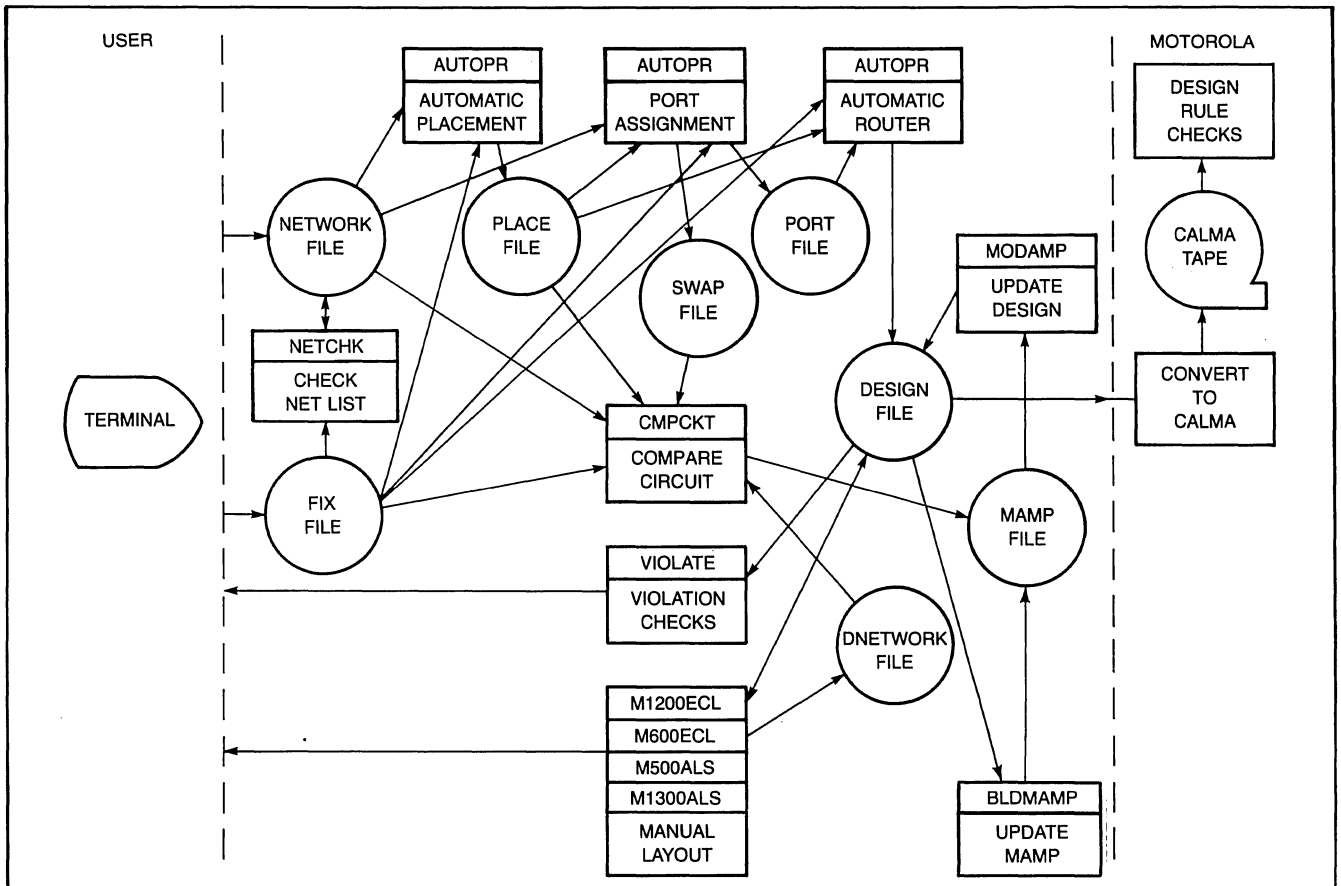


FIGURE 33. Automatic Place and Route — CAD System

The total output transistor power is 240 mW, while the bias driver is 327 mW. Adding these various powers, the total power of the design is 3.85 watts. The total number of equivalent gates amounts to 888 for an average of 4.3 mW per equivalent gate.

The chip utilization was computed to be 93%. The computation assumes that the major cells are worth a weight of 4 while the interface and output cells are each worth a weight of 1.

Figure 34 shows the CAD plot for the MC10901 plotted on a graphics terminal. All Macro I/O ports, macrocell types and channel interconnect are shown. Also, the logic diagram for the design is shown with the logic equivalent plotted for each macrocell. The Automatic Place and Route program can save about three to four manweeks of work compared to a manual layout.

To qualify the test sequence, a fault grade program (FLOGCAP) is available. The program holds every node sequentially at a "1" or a "0" and then compares the output results of the good and bad networks. The number of faults detected by the input vector sequence, divided by the total number of faults, is the test sequence efficiency. To verify a logic design, an efficiency of greater than 80% should be achieved. For production testing, an efficiency of greater than 95% should be achieved. For the MC10901, the 29 test vectors (Table 6) showed a test sequence efficiency of 82%. The number of vectors was increased to a total of 86. Figure 35 shows the fault grade results (from a file called FLOGLIST that was generated by FLOGCAP). The test sequence efficiency shows that 99% of the real faults were detected. 1627 real faults were detected and 5 real faults were not detected (1632 total real faults). There were 808 nodes and a total of 4359 total faults defined (real faults plus equivalent faults). The macro type, location and input or output node is listed for each undetected fault. Three of the undetected faults (2 on M53 and 1 on I11) are due to a logic "1" generator. The fault on the H52 is due to an input combination that can't be checked due to the multiplier algorithm. In other words, if the fault did occur, the output of the multiplier will be correct. Thus, the fault is undetected (since a correct output results) and does not affect operation of the circuit. The final undetected fault listed is an input fault on macro I08 (the SEQ=2, ISO and A92-Y states that the undetected fault is a logic "0" on the B input (SEQ=2) at location A92). This fault was actually detected by the test sequence as verified by a single fault analysis using LOGCAP. This means that the 86

TABLE 6. — MC10901 — POWER CALCULATIONS

Top Left 4			
Total # of Equivalent Gates	# Used and Macro Type	Total Macro Power (MW)	Output Follower Current (ma)
30	5-H73	43	10
140	14-H72	277.2	28
30	3-H52	54.6	6
11	1-M50	26	2
2	1-T01	10.4	1
4	1-T11	10.4	1
6	3-I01	31.2	5
16	4-I11	41.6	4
239	Total Pwr. = 790.8	494.4	57

Top Right 3			
Total # of Equivalent Gates	# Used and Macro Type	Total Macro Power (MW)	Output Follower Current (ma)
6	1-H73	8.6	2
70	7-H72	138.6	14
48	3-M53	85.8	15
22	2-M74	57	4
33	3-M50	78	6
4	1-T11	10.4	1
20	5-010	143	—
8	2-009	57.2	—
211	Total Pwr. = 797	578.6	42

Bottom Left 2			
Total # of Equivalent Gates	# Used and Macro Type	Total Macro Power (MW)	Output Follower Current (ma)
36	6-H73	51.6	12
110	11-H72	217.8	22
70	7-H52	127.4	14
2	1-T03	18.2	1
1	1-T08	5.2	.5
16	4-T11	41.6	4
4	2-I01	20.8	4
24	6-111	62.4	6
263	Total Pwr. = 875.2	545.0	63.5

Bottom Right 1			
Total # of Equivalent Gates	# Used and Macro Type	Total Macro Power (MW)	Output Follower Current (ma)
22	2-M74	57	4
64	4-M53	114.4	20
22	2-M50	52	4
10	2-M29	46.8	3
14	2-M28	46.8	8
2	1-T01	10.4	1.5
2	1-T04	18.2	2.0
8	2-G09	57.2	—
8	2-G10	57.2	—
8	2-009	57.2	—
12	3-010	85.8	—
172	Total Pwr. = 824	603	42.5

2-3 = 84.4 mW = the largest quadrant power difference

Top Power = 1587.8 mW −6.6%

Bottom Power = $\frac{1699.2 \text{ mW}}{3287 \text{ mW}}$

Bias Driver = $\frac{327 \text{ mW}}{3614}$ = 695 mA = I_{EE} (typ)

Total Output Emitter follower
Power from output cells = (16 outputs) (15 mW/output) = 240 mW
Total chip power with outputs loaded = 3614 + 240 ≈3.85 watts

Chip utilization = $\frac{232.5}{250} \times 100\% = 93\%$

Total Gates = 888
(3 gates are for wire ORs in logic)

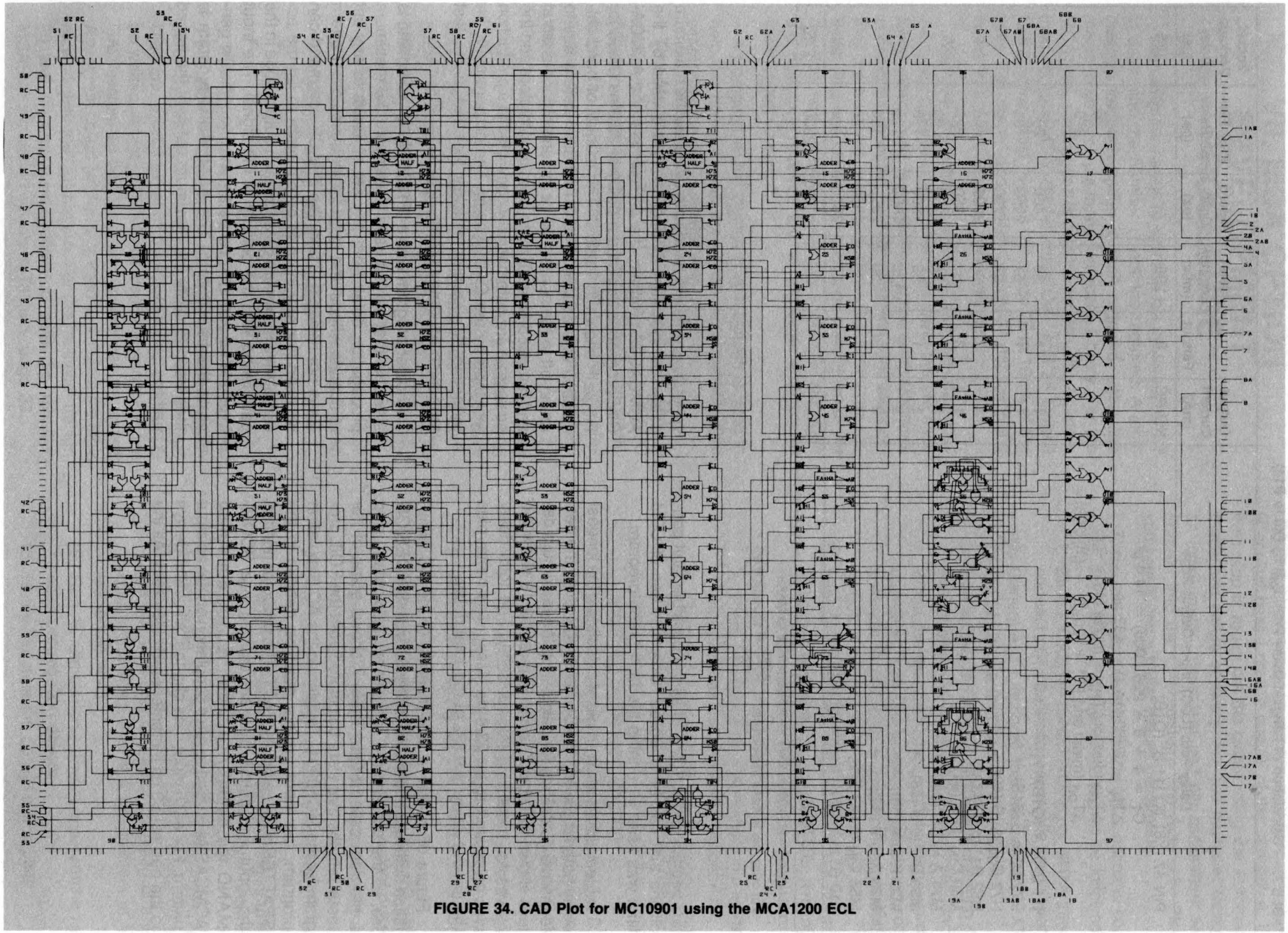


FIGURE 34. CAD Plot for MC10901 using the MCA1200 ECL

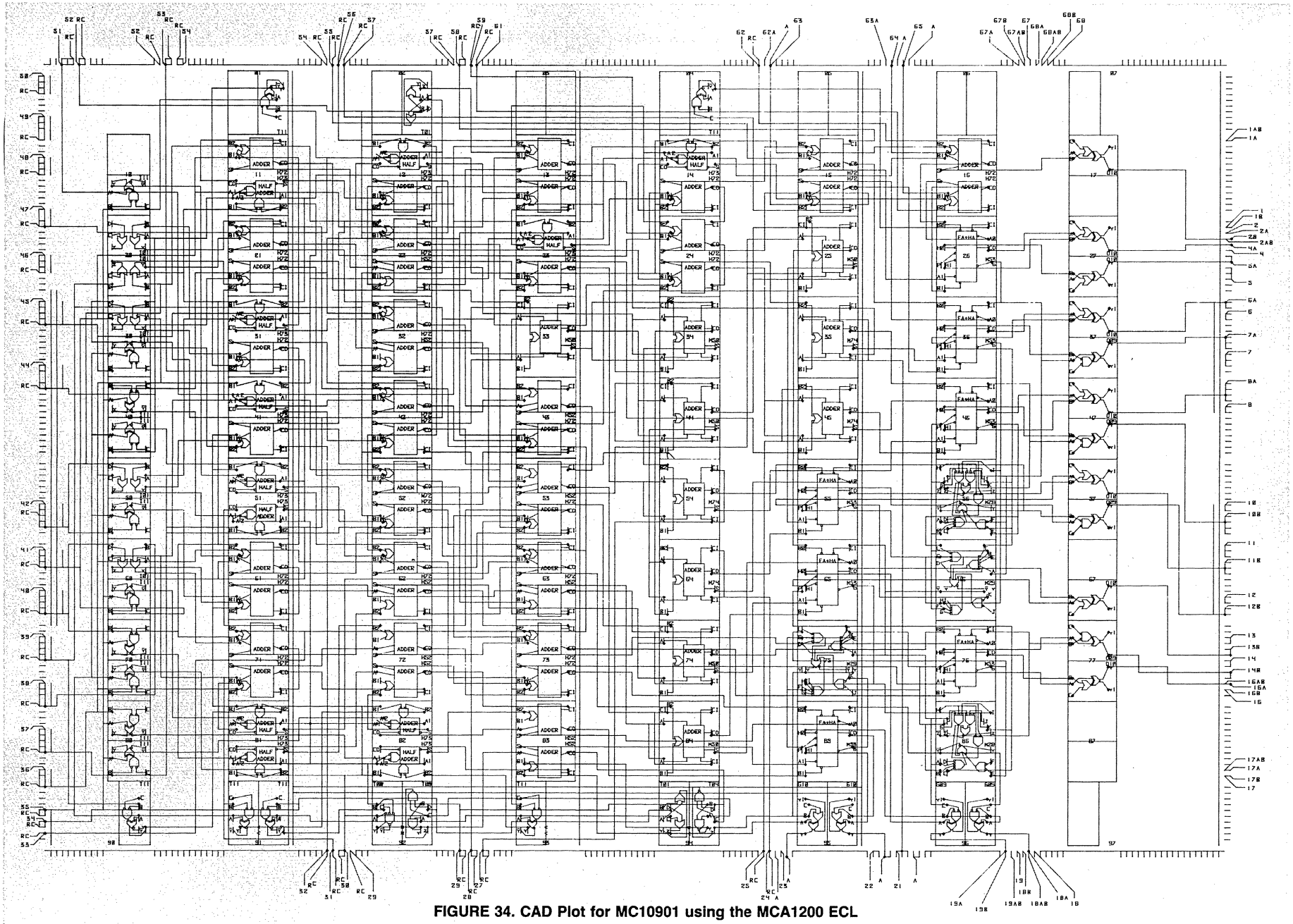


FIGURE 34. CAD Plot for MC10901 using the MCA1200 ECL

TABLE 7. — Calculation of Longest Delay Path, t_{pd-+} ($\overline{X0}$ to $\overline{P14}$)

Delay Path (LOC), Input-Output Edge	Output Current (mA)	Fanout	Metal Length (mils)	Macro Delay (ps)	Metal Plus Fan-out Delay (ps)	Socket, Package Delay (ps)
PIN 47 ($\overline{X0}$) TO I11-B* (O1B)	NO RC	8	298			175
C_T = 4 + 8 + 298 (.008) = 14.4 pf						
ΔT_R = .6 (50)(14.4) = 432 ps						
ΔT_{pd} (due to ΔT_R) = (.175) (432) =					76	
ΔT_{pd} (metal and F0) = (20)(8) + (.4)(298) =					279	
I11 B* to Y (O1B), − −	1	1	89	1400	290	
H72 B* to S (31B), − −	1	1	57	2950	185	
H72 C_{IN}* to S (42A), − −	1	1	29	1750	95	
H52 B1* to S (43A), − −	1	3	76	2800	495	
M50 C_{IN}* to S (44), − −	1	3	83	1350	525	
M74 A to CO (64), − −	1	1	28	1200	90	
M53 B1* to G (55), − −	1	1	60	1800	195	
M29 K to $\overline{Y}$ (66), − −	2	5	122	1500	170	
M28 A to $\overline{Y}$ (86), − −	2	2	58	1300	−120	
M53 C_{IN} to CO (85), − +	1	1	35	1550	50	
010 B* to Y (95B) to PIN 22 ($\overline{P14}$), + +	—	—	27	3600	—	100
TOTALS	—	—	—	21,200	2330	275

Total delay = (21,200 + 2330 + 275)ps = 23.8 ns MAX

% of delay due to metal and Fan-out = $\frac{2330}{23800} \times 100\% = 9.8\%$

test vectors check 100% of all the possible fault conditions that can be checked. Only 131 sec of CPU time was used in running the fault grade program.

Table 7 shows an example of calculating the longest delay path for the MC10901. Section V gives the performance guidelines for calculating the maximum delays shown in Table 7, while Figures 13-19 show the curves for metal and fan-out delay. The total delay was calculated to be 23.8 ns (Max). The metal plus the fan-out delay is 9.8% of the total delay.

Figure 36 shows a flow diagram of the AC Simulation software in the CAD system. From the DESIGN file, all the actual metal lengths are calculated using a program called FOIL. Table 7 shows some of the metal lengths that were calculated from the FOIL program for the MC10901. To operate the AC Simulation program, the input vectors must be defined in the SPATTERN file called ACPATT. The order for printing the input and output pins are defined in a SCOMMAND file called ACCOMM. A program called ACMCASIM is used to run a simulation on the ac input pattern. For each input data change, all output delays to the nearest 50 ps increment are calculated. All the various parameters needed to calculate the maximum delay (as indicated in Section V) are used by the ACMCASIM program. As an example, the ACMCASIM program calculated a delay of 23.9 ns (Max) for the path shown in Table 7. The manual or hand calculation was 23.8 ns. The 0.1 ns difference is due to round-off to the nearest 50 ps increment for the metal and fan-out delays. The dc functional vectors and the ac vectors are automatically converted to a production test tape by the CAD system. The dc parametric information is also automatically included in the test tape such as input current, I_{EE}, V_{OH}, and V_{OL}.

Another program with a "PROPDLAY" command is available that can be used to compute the maximum propagation delay from any set of inputs to any set of outputs without the need for input vectors (Pattern file is not needed). Then, the TRACE command can be used (for any input to output path) to list the accumulative maximum delay at each output node in the path along with the polarity of the signal. The input logic states can then be determined to logically generate the traced path. The ACMCASIM program is then used to verify the maximum delay of the traced path.

```
 INPUT >SIM A10901
 USER LIB
 M28          SUBNET
 M29          SUBNET
 M50          SUBNET
 H52          SUBNET
 M53          SUBNET
 H72          SUBNET
 H73          SUBNET
 M74          SUBNET
 I01          SUBNET
 I03          SUBNET
 I04          SUBNET
 I08          SUBNET
 I11          SUBNET
 O09          SUBNET
 O10          SUBNET
 BOUT         SUBNET
 SYS LIB
   808 NODES IN A10901
       COMPNET FILE CREATED
 INPUT >DEFINE
   4359 FAULTS DEFINED
 DEFINE FILE CREATED
 INPUT >SWEEP TO 86
 INPUT >GO
0FAULT SIMULATION STARTED
 FAULT SIMULATION COMPLETE — RESTART POINT AT CYCLE     87
 INPUT >COUNT
   1627 FAULTS DETECTED LAST SEGMENT
     99 PERCENT OF REAL FAULTS
      0 UNSTABLE FAULTS LAST SEGMENT
      5 UNDETECTED FAULTS REMAINING
      0 PERCENT OF REAL FAULTS
   1628 CUMULATIVE FAULTS DETECTED
     99 PERCENT OF REAL FAULTS
 INPUT >FPRINT       UNDET
1 A10901 ON 80.323 AT 16.01.46 UNDETECTED FAULTS TO CYCLE 87
   NAME              NUMBER I/O    SEQ    TYPE    CL
   B26-CI              3103  I       0     IS1     R   M53
   A92-Y               3656  I       2     IS0     R   I08
   B04-Y               3829  O       1      S1     R   I11
   B83-A               4042  I       0     IS0     R   H52
   B26-A0              4236  I       0     IS0     R   M53
 INPUT >EXIT
```

FIGURE 35. Fault Grade Results of FLOGCAP Program

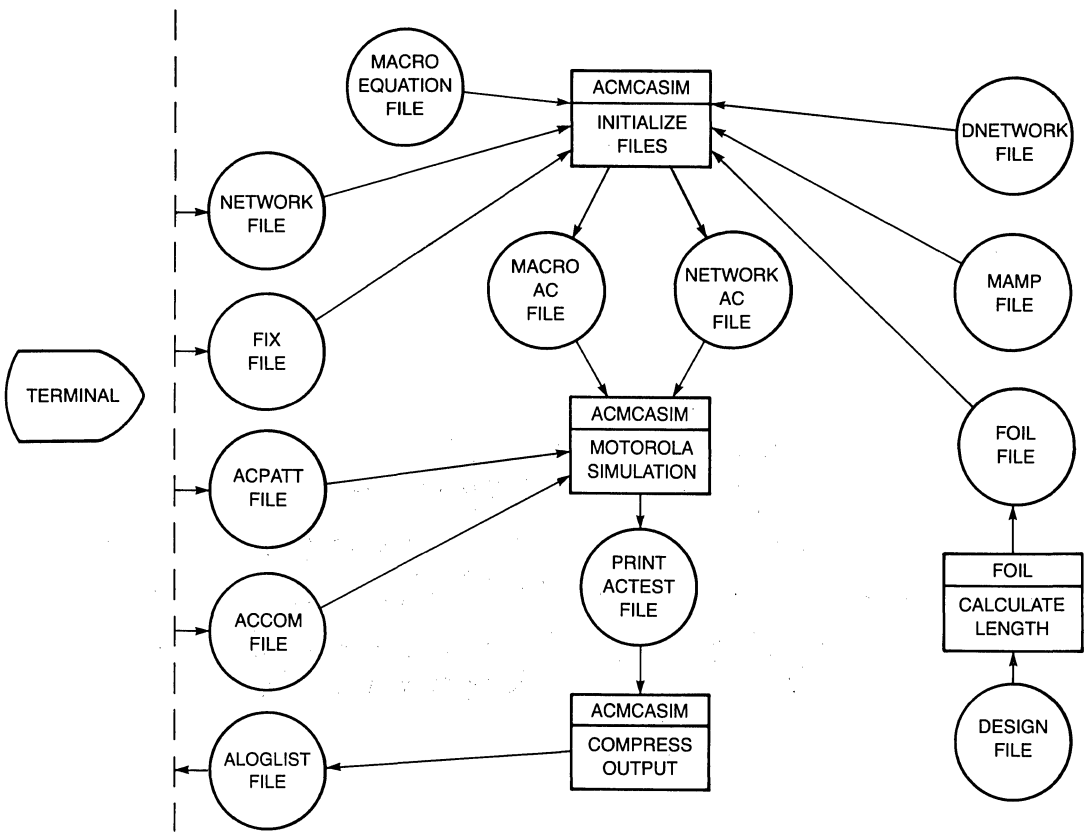


FIGURE 36. AC SIMULATION

APPENDIX — THE MECL MACROCELL ARRAY SPECIFICATION

THE MACROCELL LIBRARY — TECHNICAL DATA

The Macrocell library consists of three groups of cells:

1. MAJOR CELLS
2. INTERFACE CELLS
3. OUTPUT CELLS

A. Logic Symbology

Positive logic is assumed for all logic drawings where a logic "I" is a high voltage level (V_{OH}) and a logic "O" is a low voltage level (V_{OL}).

The library consists of more than 100 macros. All inputs and outputs are labeled with the symbols used in the CAD system for defining the I/O ports. A circle on an input to a logic gate or block denotes that an active "low" enables that input. The inputs to the logic block are denoted on the left and bottom side of the block. The outputs are on the right side of the logic block.

A circle on the output of a logic block denotes the output is active in the "low" state. Logic equations are given to define the simple gate functions; truth tables and logic equivalent diagrams are shown for the more complex macros.

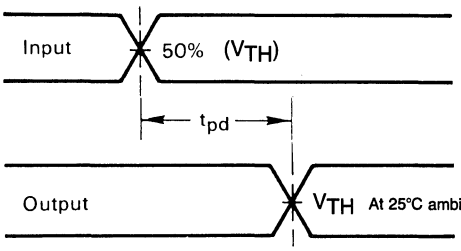
B. Propagation Delay

The worst case propagation delay is specified for $V_{EE} = -5.2$ volts ± 10%, and a maximum junction temperature of T_J max = 115°C. For the MCA1200, attaching a recommended heat sink or equivalent to the package and a 1000 LFPM of air flow will generally result in an ambient temperature range of 0°C to 70°C. For the MCA600, 500 LFPM of air flow (no heat sink required) will generally result in an ambient temperature range of 0°C to 70°C. In general, a lower junction temperature will result in faster propagation delays.

For the Major and Interface Cell macros, the values given for propagation delay are maximum values for a 1.0, 1.5, 1.8 or 2.0 mA output follower current driving a fan-out of 1. The numbers are also good for an 0.5 or 0.8 mA output follower driving a fan-out of 1 on the rising edge at the output (t_{pd+}) but for the falling edge delay (t_{pd-}), 200 ps must be added to the specified delay.

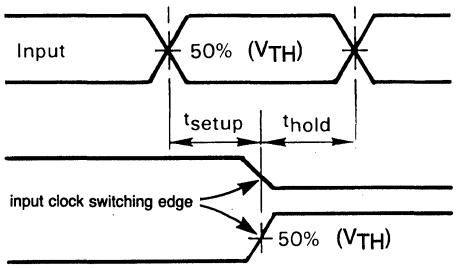
For Output cell macros, the values given for propagation delay are maximum for the output package pin driving 50 Ω (25 Ω for macro 024 or 025) to −2.0 volts. The propagation delays specified are measured from the 50% point of the input rising or falling edge to the V_{TH} point of the output rising or falling edge. V_{TH} is the V_{BB} threshold voltage which is equal to −1.3 volts (for $V_{CC} = 0$ volts) at 25°C ambient. The 50% point of the input and the V_{TH} point of the output are adjusted by +1.2 mV for each +1°C increase in ambient temperature.

Propagation Delays



At 25°C ambient, the output measurement is to the −1.3 volt point (V_{CC} = 0 volts).

Setup and Hold



TEST PROCEDURE:
a) Establish setup time with long t_{hold}
b) Keeping the leading edge of the input constant (t_{setup}) vary the trailing edge of the input to determine t_{hold}.

FIGURE 37. SWITCHING WAVEFORMS

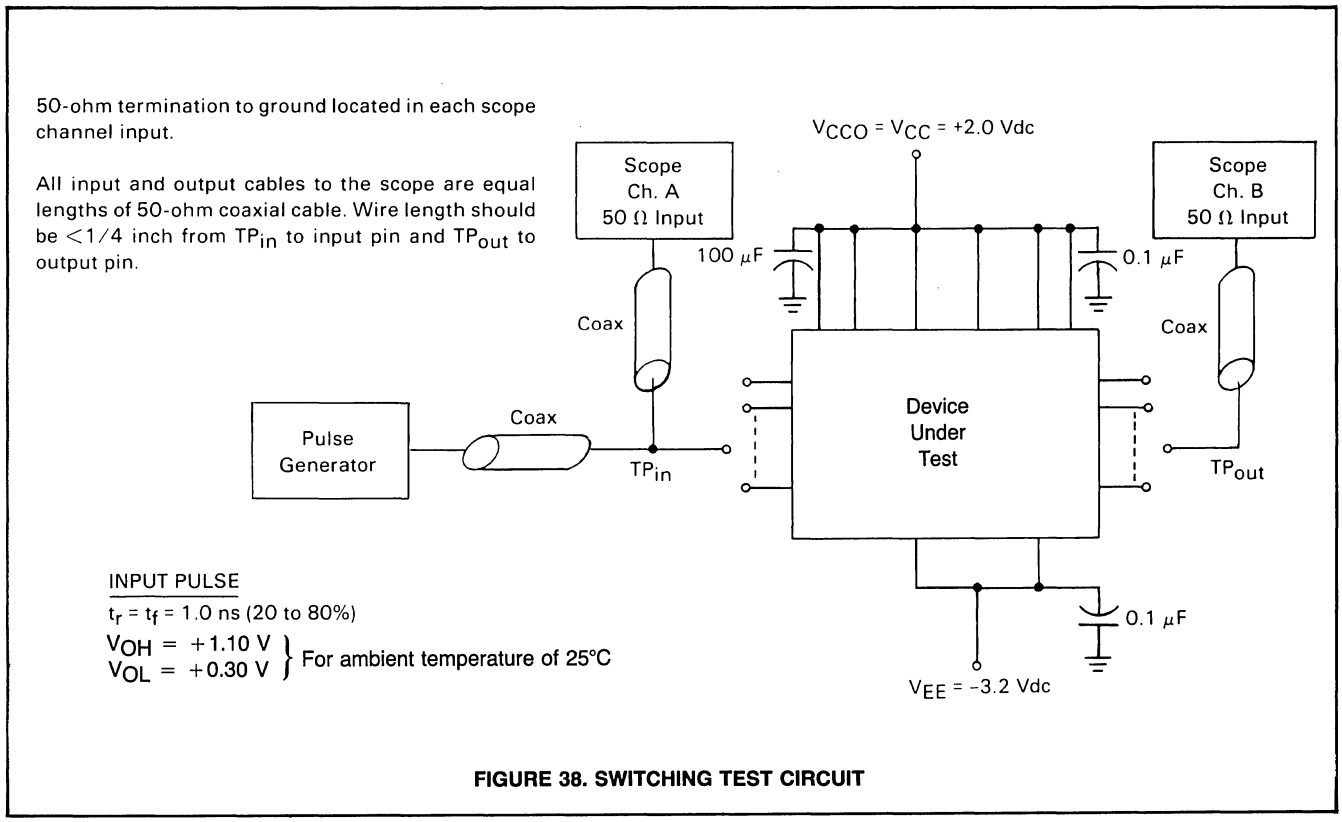


FIGURE 38. SWITCHING TEST CIRCUIT

Major cell macro H02 can be used as an example of the terminology. t_{pd} is the propagation delay from all upper level inputs (no asterisk) to all outputs. t_{pd}* (Y,Z) is the propagation delay from the lower level inputs (shown with asterisk) to the Y or Z output. t_{pd+}*($\overline{Y}$,$\overline{Z}$) is the propagation delay from the lower level inputs to the $\overline{Y}$ or $\overline{Z}$ outputs on the rising edge of the output (low to high voltage transition). t_{pd-}* ($\overline{Y}$,$\overline{Z}$) is the propagation delay from the lower level inputs to the $\overline{Y}$ or $\overline{Z}$ outputs on the falling edge of the output (high to low voltage transition).

Figure 37 shows the switching waveform definitions while Figure 38 shows the switching test circuit for testing the ac performance. Note that 1 ns input rise and fall times (20 to 80%) are required in order to meet the specified propagation delays.

C. Setup and Hold Time

The worst case setup and hold times are also listed for all flip-flops and latches. The setup time (t_{setup}) is the amount of time the data must be present before the latching edge of the clock in order to insure the data is latched properly. The hold time (t_{hold}) is the amount of time the data must remain unchanged after the latching edge of the clock in order to insure the data will remain valid.

D. Pulse Width

The worst case minimum pulse width (t_{PW}) is also specified for the clock inputs of latches and flip-flops in order to insure proper operation. If the clock input is being driven directly from an input pin, the specified t_{PW} is valid for a fan-in of 1 for input rise and fall times of 1.0 ns (20 to 80%). See Section V-O, Page 24, for more details.

E. Power Dissipation

The typical power dissipation is specified for each of the macros in the library. However, this power does not include the power of the output follower. To calculate the power due to the output follower for major and interface macros, multiply V_{EE} (−5.2 volts) times the selected output follower current. The maximum and minimum power for each macro can be calculated by multiplying the typical power by 1.25 and 0.75 respectively.

For the output cell, the load resistor for the output follower is placed outside the Macrocell Array package. Therefore, the output cell power dissipation does not include the output follower power. When calculating the package power, the power of the output transistor (near bonding pad) needs to be added to the total. For 50 Ω terminations to −2.0 volts, the average power dissipation for the output transistor is 15 mW. For driver macros that are cutoff in the low voltage state, the average power dissipation of the output transistor is 20 mW for a 25 Ω load or 10 mW for a 50 Ω load.

For major cell macros, the typical power dissipation, P_D, is given for each macro for the whole cell. If only a half cell is used (for half cell macros), divide the indicated power by 2.

F. Fan-in

The input fan-in is shown in parenthesis, ( ), at the logic input of each macrocell in the Library when the fan-in is not equal to 1. When the input fan-in is equal to 1, the (1) is not shown.

G. Wire OR

The number of internal wire OR connections is indicated in parentheses at the macro outputs. This number is needed only when calculating the wire OR delay due to a wire OR connection between macrocell outputs. See section on Wire ORing for more details.

H. Output Current

Each cell location contains a number of resistors designated to provide a variety of output-current options for the designer. These resistors are appropriately connected by the CAD-derived Macro metallization pattern in accordance with the designer's specifications.

For Major Cell Macros:

If a half-cell utilizes either one or two outputs, 0, 0.5, 1.0, or 2.0 mA can be specified for each output unless specified otherwise. For wholecell Macros utilizing up to four outputs, each output may be specified for 0, 0.5, 1.0 or 2.0 mA unless specified otherwise.

Each Major cell quadrant has three resistors, two providing a 0.5 mA load each and one with 1.0 mA load. The resistors are connected in parallel to select the desired output current levels. For half cells containing four outputs, two of the outputs are normally the complement of the other two (for instance, Y, Z and $\overline{Y}$, $\overline{Z}$). The Y and $\overline{Y}$ outputs are in one quadrant sharing the three resistors, while the Z and $\overline{Z}$ are in the other quadrant. The possible current options for outputs sharing the same quadrant are (0,0), (0,0.5), (0,1.0), (0,2.0), (0.5,0.5), and (1.0,1.0) mA.

For Interface Cell Macros:

An output follower current of 0, 0.5, 1.0, or 1.5 mA can be selected for each output even if both outputs are used unless specified otherwise. For I13 and I14, the Q output can be selected for 0, 0.8, 1.0, or 1.8 mA while the $\overline{Q}$ output can be selected for 0, 0.5, 1.0, or 1.5 mA.

For Output Cell Macros:

The Y1 output may be specified for 0, 1.0, or 2.0 mA. For Transceiver Macros 016 and 017, the receiver output can be specified as 0, 1.0, or 2.0 mA.

I. Lower Level Inputs

Inputs that are connected to an input follower are marked with an asterisk, *, and are connected to the lower level of a series gated structure. Unmarked inputs go directly to base of a transistor connected in the upper level of a series gated structure. These two different types of inputs are differentiated in order to specify different propagation delays, and different rules for connecting to input compensation networks and to input package pins.

All inputs of Interface and Output cell macros are allowed to be connected to package pins or to the Y1 output of an Output cell macro. An extra diode drop is used in these cells on lower level inputs to eliminate potential saturation problems.

For Major cell macros, upper level inputs and lower level inputs marked with a circle around the asterisk, ⊛, are allowed to be connected to package pins or to the Y1 output of an Output cell macro. Stated differently, Major cell macros with inputs marked with an asterisk (with no circle around it) are not allowed to be connected to package pins or to the Y1 output of an Output cell macro due to potential saturation problems.

J. Major Cell Macros

The macros in the Major Cell Library are labeled with an "H" or "M" followed by two numbers. The "H" represents a macro using only half (or less) the components of a Major cell and is called a half cell macro. The half cell macro can be placed in either the top or bottom half of a major cell. As an example, H31 (a D flip-flop) could be placed in the top half of a major cell and an H52 (a full adder) could be placed in the bottom half. The "M" represents a macro requiring more than half the components in the major cell and therefore requires the use of both the top and bottom half of the cell.

HØ1 through M3Ø include various combinations of gating functions that can be used in clock driving, parity checking, data transfer, carry lookahead generation. H31 and M32 are edge triggered D flip-flops that can be used for registers and counters. An asynchronous reset can be formed with these flip-flops by tying the reset and one of the clock inputs together. However, a narrow pulse can occur at the flip-flop output when it is reset as indicated in the truth table.

H33 through H54 produce useful logic functions such as latches, multiplexers, decoders and full adders. M53 contains a full adder plus a half adder with 2-bit propagate and generate functions. This is very useful in generating fast adders.

H59 through H62 are similar to HØ1 through HØ4 but contain an extra gating input. H63 through H69 are similar to other macros except they contain less logic and therefore less power.

H71 through M8Ø are similar to other macros except all the inputs are allowed to be connected to package pins or to the Y1 output of an output cell. All lower level inputs have a diode placed in series with the input follower, similar to an interface cell.

H81 is an edge triggered D flip-flop with a differential receiver on the clock and data inputs. Also, internally the master drives the slave differentially. The reason

for the differential drive is to minimize the skew or difference between the logic "1" and logic "0" setup and hold times. Separate reset inputs control the resetting of the master and slave portions of the flip-flop.

K. Interface Cell Macros

Most of the macros in the Interface Cell Library are labeled with an "I" followed by two numbers and a "T" followed by the same two numbers. When using CAD, the "I" designation is used to place the macro in a side interface cell (left side) and the "T" designation is used to place the macro in the top or bottom row of interface cells. Although the "I" and "T" cells are logically equivalent, a different internal cell metal pattern is required which results in different I/O port channel assignments.

All inputs of Interface Cell macros can be connected to input package pins or to the Y1 output of Output Cell macros. These cells can be utilized for input interfacing and to provide extra logic power within the array.

Dual gate functions are also available in the library in numerous combinations. Very useful macros like I05, I06, I07, and I10 (where one input is inverted) are not available in standard logic families. Macros I06 and I07, together, can be used to form a 1-of-4 decoder similar to M45, except that an enable line is not present. Macros I13 and I14, together, can be used to form a D flip-flop similar to H31.

I20 is a dual differential line receiver that can be used to receive logic information using twisted pair lines. The differential receiver is used to provide maximum system noise immunity. The common mode noise rejection is approximately ± 1 volt.

L. Output Cell MACROS

Most of the macros in the output cell are labeled with an "O" followed by two numbers and a "G" followed by the same two numbers. When using CAD, the "O" designation is used to place the macro in a side output cell (right side) and the "G" designation is used to place the macro in the top or bottom row of output cells. Although the "O" and "G" cells are logically equivalent, a different internal metal pattern is required which results in different I/O port channel assignments.

All inputs of Output Cell macros can be connected to input package pins or to the Y1 output of Output Cell macros. The output cells are primarily used to provide the interface between the internal logic and the logic outside the package providing 50 ohm and 25 ohm drive capability. Output Cell macros containing a Y1 output can be used as an Interface Cell macro since the Y1 output can drive inputs of Major Cell macros not marked with an asterisk (*). The Y1 output can also drive any input of an Interface Cell macro or an Output Cell macro.

Although the Output Cell macros are primarily used for interfacing, they also provide extra logic capability with logic functions such as OR-AND, exclusive OR with enable, 2 to 1 multiplexer with enable, and latches. There are several drivers that are capable of driving 50 ohm or 25 ohm loads with the V_{OL} state in the cutoff mode (V_{OL} (Max) = −1.95 volts). The driver output of 016, 017, 018, and 019 are capable of driving 50 ohms to −2.0 volts while 024 and 025 are capable of driving 25 ohms to −2.0 volts.

The Y output of Output Cell macros 016, 017, 018, and 019 can be routed to pins with one output emitter follower transistor. However, the Y output of the 25 ohm driver macros must be routed to pins that have two transistors.

Table 8 lists the package pins that have two transistors as well as cell locations restrictions for placing a transceiver macro (016 or 017) or the driver macros (018, 019, 024, and 025). See Figure 3a and 3b for cell location assignments.

In addition, no more than 10 total 25 ohm drivers (024 and 025) or transceiver macros (016 and 017) may be placed in the array (5 max. in the upper half and 5 max. in the lower half). The maximum number of 50 ohm driver macros with V_{OL} in the cut-off mode (018 and 019) allowed per design option is 18 (9 maximum in the upper half of the array and 9 maximum in the lower half). Refer to Section IV-B, page 14, for more details on the maximum number of drivers allowed.

TABLE 8 — Package Pins Having Two Transistors and Driver Placement Restrictions

MCA TYPE	PACKAGE TYPE	PINS HAVING TWO TRANSISTORS	CELL LOCATIONS NOT ALLOWED FOR DRIVER PLACEMENT	
			FOR MACROS 016, 017, 024, 025	FOR MACROS 018, 019
MCA1200	68 PIN LCC	1, 2, 16, 17, 18, 19, 67, 68	27, 37, 47, 57, 67, 77	37, 47, 57, 67
MCA600	68 PIN LCC	4, 5, 13, 14, 18, 19, 67, 68	25, 35, 45, 55	—
	40 PIN DIL	14, 15, 17, 18, 23, 24, 26, 27		
	28 PIN DIL	2, 3, 5, 6, 23, 24, 26, 27		
	72 PGA	C2, D1, H1, H2, L2, K2, B3, A2		
MCA1200	72 PGA	B1, B2, J2, K1, L2, K2, B3, A2	27, 37, 47, 57, 67, 77	37, 47, 57, 67

M. MCA ECL DC Parameters

Input Forcing Voltages	Parameter	Spec Limits [1] Ambient Temperature 0°C	25°C	70°C	Unit	Comments
V_{IH} MAX and V_{IL} MIN	V_{OH} MAX[4]	−0.840	−0.810	−0.730	Vdc	For all outputs
	V_{OH} MIN	−1.000	−0.96	−0.905	Vdc	For all outputs
	V_{OL} MAX	−1.665	−1.650	−1.625	Vdc	For all outputs, excluding drivers
	V_{OL} MAX [2]	−1.950	−1.950	−1.950		Drivers only
	V_{OL} MIN	−1.950	−1.950	−1.950	Vdc	For all outputs, excluding drivers
	V_{OL} MIN [2]	−2.020	−2.020	−2.020		Drivers only
V_{IHA} MIN and V_{ILA} MAX	V_{OHA} MIN	−1.020	−0.980	−0.925	Vdc	For all outputs
	V_{OLA} MAX	−1.645	−1.630	−1.605	Vdc	For all outputs, excluding drivers
	V_{OLA} MAX [2]	−1.950	−1.950	−1.950	Vdc	Drivers only
V_{IH} MAX	I_{INH} MAX	50	50	50	μA	For each fan-in
		150	150	150		For input pulldown (≈ 50 kΩ)
V_{IL} MIN	I_{INL} MIN [3]	0.5	0.5	0.5	μA	Measured only if input pulldown is used
	V_{IH} MAX	−0.840	−0.810	−0.730	Vdc	Input forcing voltages
	V_{IL} MIN	−1.950	−1.950	−1.950	Vdc	
	V_{IHA} MIN	−1.145	−1.105	−1.050	Vdc	
	V_{ILA} MAX	−1.490	−1.475	−1.450	Vdc	

① DC test limits are specified after thermal equilibrium has been established with the MCA device having an attached heat sink and a transverse air flow of 1000 LFPM for the MCA1200 and 500 LfPM and no heat sink for the MCA600. V_{EE} = −5.2 v ± 0.010 v. All outputs are loaded with 50 Ω to −2.0 volts except the 25 Ω drivers (024, 025) which are loaded with 25 Ω to −2.0 volts.

② These voltage limits are for the driver output of macros with V_{OL} in the cutoff mode (driver macros include 016, 017, 018, 019, 024, 025).

③ In Final Test, this measurement insures that the input pulldown resistor is connected. There is no test for minimum input current if the input pulldown resistor is not used.

④ For an output pin having a wire OR of two output cell macros, +60 mV must be added to the V_{OH} MAX specification limit.

It is not necessary to measure all points on the transfer curves. To guarantee correct operation it is sufficient to measure two sets of min/max logic level parameters.

The first set is obtained by applying test voltages, V_{IL} min and V_{IH} max (sequentially) to the gate inputs, and measuring the output levels to make sure they are between V_{OL} max and V_{OL} min, and V_{OH} max and V_{OH} min specifications.

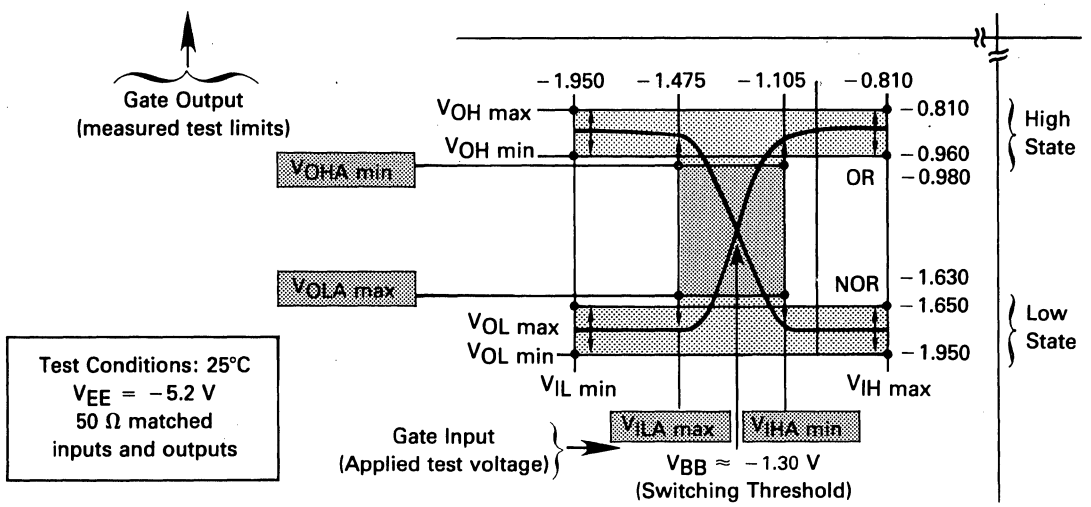


FIGURE 39. MECL TRANSFER CURVES (MCA ECL EXAMPLE) and SPECIFICATION TEST POINTS

The second set of logic level parameters relates to the switching thresholds. This set of data is distinguished by an "A" in symbol subscripts. A test voltage, $V_{ILA\ max}$, is applied to the inputs and the outputs are measured to see that they are above the V_{OHA} min and below the $V_{OLA\ max}$ levels, respectively. Similar checks are made using the test input voltage V_{IHA} min.

The result of these specifications insures that:

a) The switching threshold ($\approx V_{BB}$) falls within the darkest rectangle; i.e., switching does not begin outside this rectangle;

b) Quiescent logic levels fall in the lightest shaded ranges;

c) Noise immunity guideline is met.

N. Limits Beyond Which Device Life May Be Impaired

Characteristic	Symbol	Unit	Value
Supply Voltage (V_{CC} = 0)	V_{EE}	Vdc	−7.0 to 0
Input Voltage (V_{CC} = 0)	V_{in}	Vdc	0 to V_{EE} (−5.2 v)
Input Voltage Bus (V_{CC} = 0)	V_{in}	Vdc	0 to −2.0 ①
Output Source Current Continuous (50 Ω drive)	I_{out}	mAdc	30
Output Source Current Surge (50 Ω drive) ③	I_{out}	mAdc	100
Output Source Current Continuous (25 Ω drive)	I_{out}	mAdc	60
Output Source Current Surge (25 Ω drive) ③	I_{out}	mAdc	200
Storage Temperature	T_{stg}	°C	−55 to +150
Junction Temperature ②	T_J	°C	165

① Input voltage limit is V_{CC} to −2.0 volts when bus is used as an input and the output drivers are disabled.

② Maximum T_J may be exceeded (≤250°C) for short periods of time (≤240 hours) without significant reduction in device life.

③ The surge current is defined as an output current between 30 mA and 100 mA for 50 Ω drive and 60 mA and 200 mA for 25 Ω drive lasting for ≤10 μs and having a duty cycle of not more than 1%.

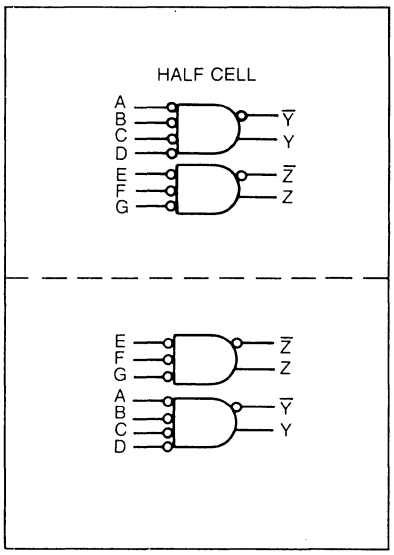
O. Recommended Operating Conditions

Characteristic	Symbol	Unit	Value
Supply Voltage (V_{CC} = 0)	V_{EE}	Vdc	−4.68 to −5.72
Operating Temperature With Heat Sink and 1000LFM for MCA1200, No Heat Sink and 500LFM for MCA600 (DC & Functional)	T_A	°C	0 to +70
Maximum Junction Temperature (Functional)	T_J	°C	130
Maximum Junction Temperature (For AC Specifications)	T_J	°C	115
Maximum Clock Input Rise & Fall Times (20 to 80%)	t_r, t_f	ns	10

Major Cell Library

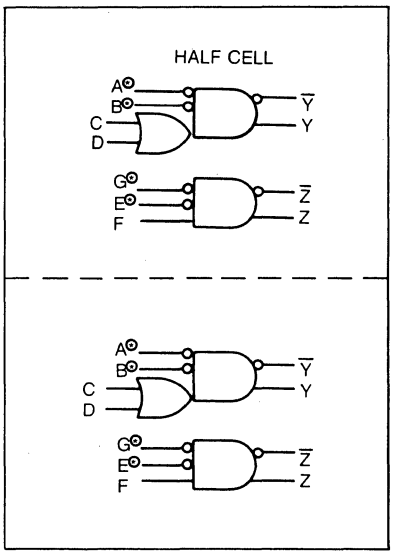
NOTES: Values given for prop. delay, tpd, are max. for 1mA or 2mA output follower current driving a fan-out of 1. Values given for power dissipation, PD, are typical with unloaded outputs. Output follower current can be selected for 0, 0.5, 1, or 2mA. Number in ( ) at the inputs indicate fan-in other than 1. *Inputs are connected to an input follower. Number in ( ) at the outputs indicate the total number of internal wire OR's. Unmarked upper level inputs and ⊙Inputs can be connected to input package pins while * inputs cannot.

H01



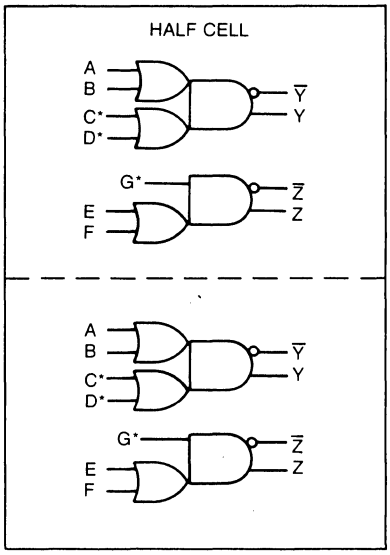
$Y = \overline{A} \cdot \overline{B} \cdot \overline{C} \cdot \overline{D}$
$\overline{Y} = A + B + C + D$
$Z = \overline{E} \cdot \overline{F} \cdot \overline{G}$
$\overline{Z} = E + F + G$
tpd = 1.2ns
PD = 20.8mW

H02



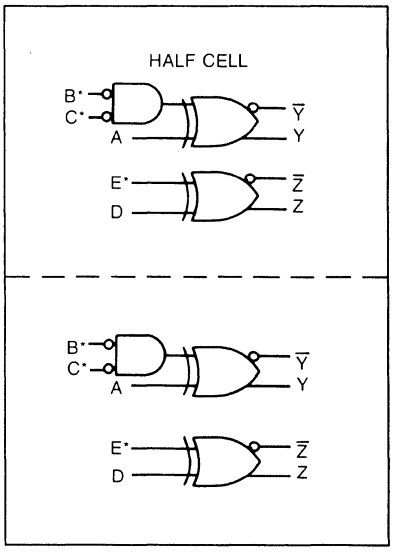
$Y = \overline{A} \cdot \overline{B} \cdot (C + D)$
$Z = \overline{G} \cdot \overline{E} \cdot F$
tpd = 1.1ns
tpd*(Y, Z) = 1.3ns
tpd+*($\overline{Y}$, $\overline{Z}$) = 1.3ns
tpd−*($\overline{Y}$, $\overline{Z}$) = 1.5ns
PD = 31.2mW

H03



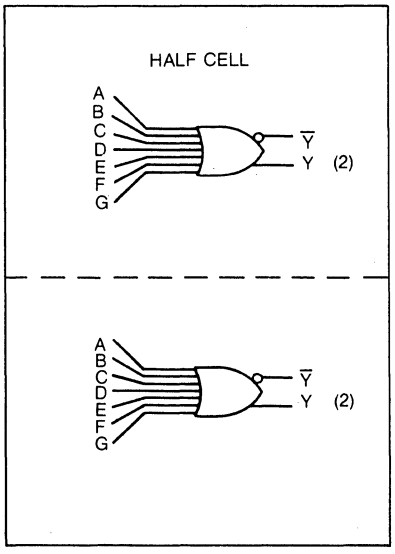
$Y = (A + B) \cdot (C + D)$
$Z = (E + F) \cdot G$
tpd = 1.1ns
tpd* = 1.4ns
PD = 31.2mW

H04



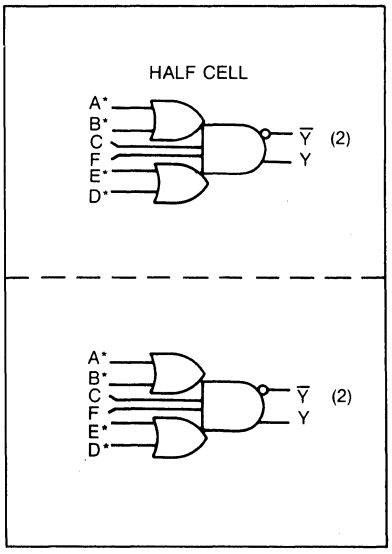
$Y = A \oplus (\overline{B} \cdot \overline{C})$
$Z = D \oplus E$
tpd = 1.05ns
tpd* = 1.4ns
PD = 31.2mW

H05



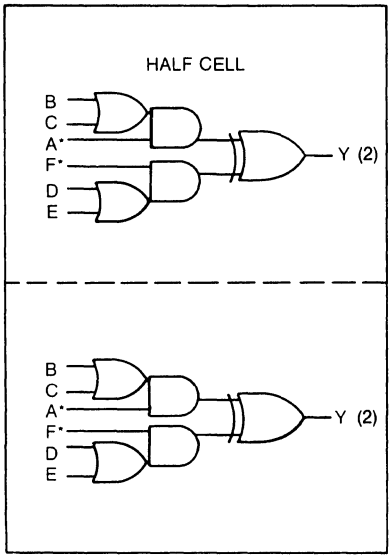
Y = A + B + C + D + E + F + G
tpd (Y) = 1.1 ns
tpd−($\overline{Y}$) = 1.7 ns
tpd+($\overline{Y}$) = 2.0 ns
PD = 20.8 mW

H06



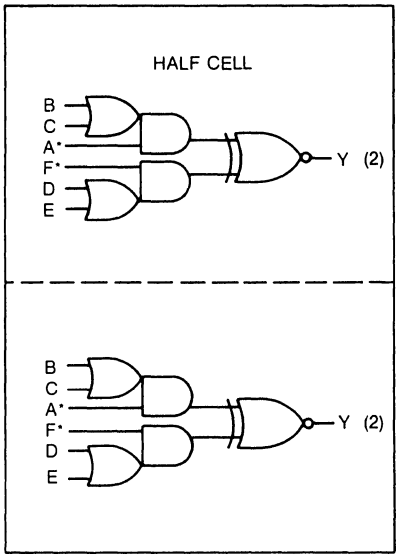
$Y = (A + B) \cdot (D + E) \cdot C \cdot F$
tpd (Y) = 1.5ns
tpd*(Y) = 1.6ns
tpd ($\overline{Y}$) = 1.0ns
tpd*($\overline{Y}$) = 1.4ns
PD = 31.2mW

H07



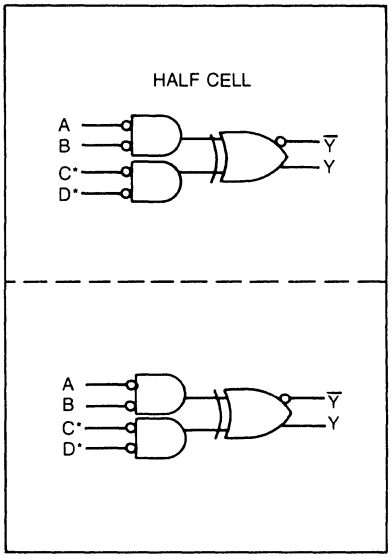
$Y = [A \bullet (B + C)] \oplus [F \bullet (D + E)]$
tpd = 1.45ns
tpd* = 1.90ns
PD = 31.2mW

H08



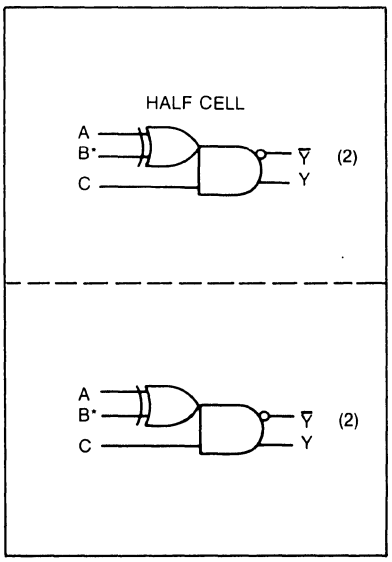
$Y = \overline{[A \bullet (B + C)] \oplus [F \bullet (D + E)]}$
tpd = 1.45ns
tpd* = 1.90ns
PD = 31.2mW

H09



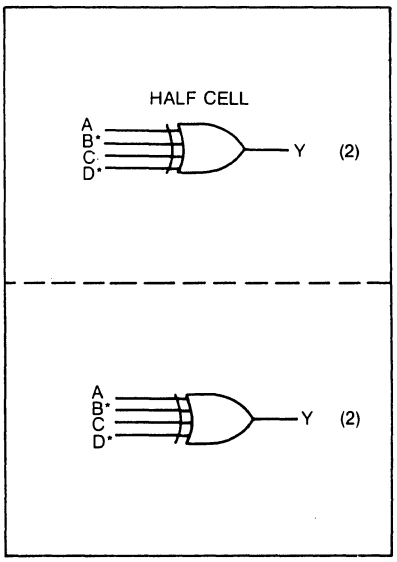
$Y = (\overline{A} \bullet \overline{B}) \oplus (\overline{C} \bullet \overline{D})$
tpd = 1.2ns
tpd* = 1.55ns
PD = 15.6mW

H10



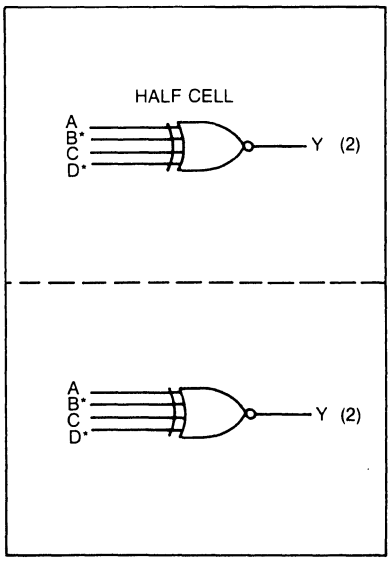
$Y = (A \oplus B) \bullet C$
tpd ($\overline{Y}$) = 1.05 ns
tpd −(Y) = 1.15 ns
tpd +(Y) = 1.45 ns
tpd*($\overline{Y}$) = 1.4 ns
tpd*(Y) = 1.7 ns
PD = 26 mW

H11



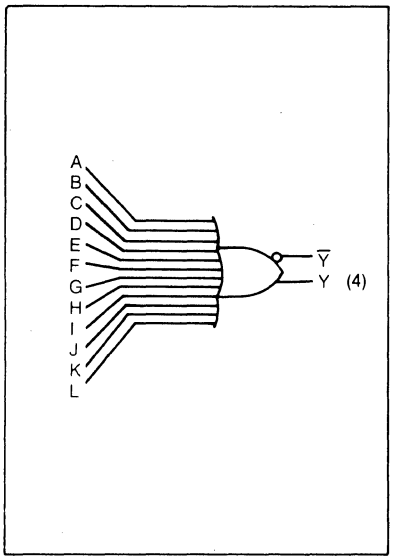
$Y = A \oplus B \oplus C \oplus D$
tpd = 1.2ns
tpd +* = 1.55ns
tpd −* = 1.65ns
PD = 31.2mW

H12



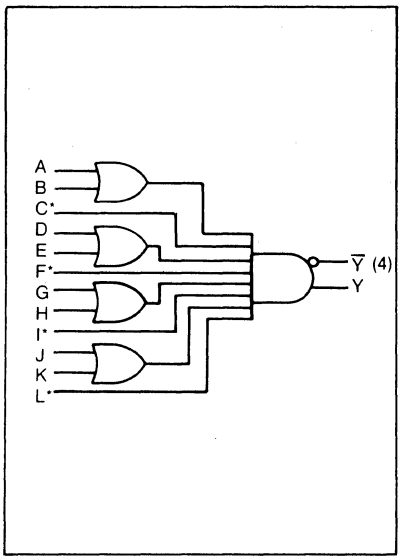
$Y = \overline{A \oplus B \oplus C \oplus D}$
tpd = 1.2ns
tpd +* = 1.55ns
tpd −* = 1.65ns
PD = 31.2mW

M13



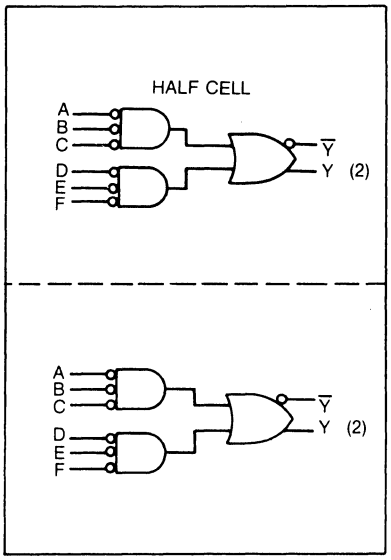
$Y = A + B + C + D + E + F + G + H + I + J + K + L$
tpd (Y) = 1.15ns
tpd – ($\overline{Y}$) = 2.1ns
tpd + ($\overline{Y}$) = 2.35ns
PD = 20.8mW

M14



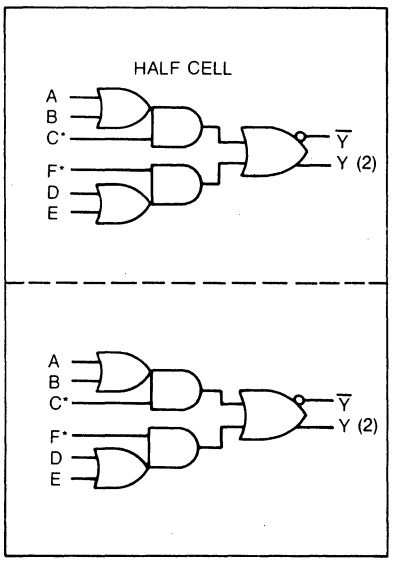
$Y = (A + B) \bullet (D + E) \bullet (G + H) \bullet (J + K) \bullet C \bullet F \bullet I \bullet L$
tpd (Y) = 1.8ns
tpd*(Y) = 1.9ns
tpd ($\overline{Y}$) = 1.1ns
tpd*($\overline{Y}$) = 1.35ns
PD = 31.2mW

H15



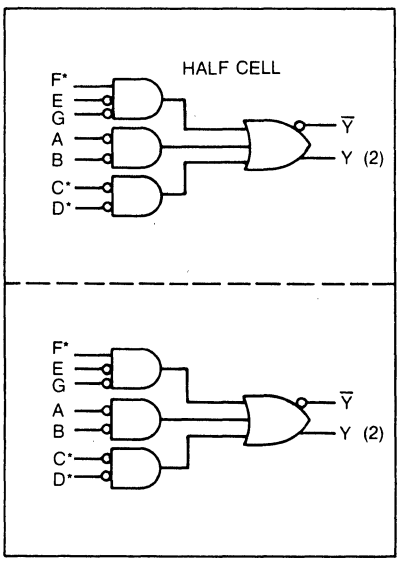
$Y = \overline{A} \bullet \overline{B} \bullet \overline{C} + \overline{D} \bullet \overline{E} \bullet \overline{F}$
tpd = 1.3ns
PD = 20.8mW

H16



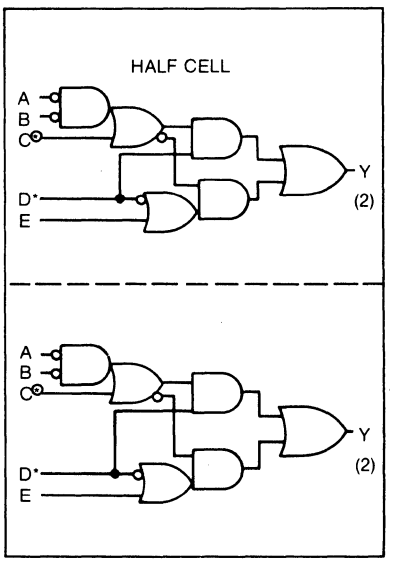
$Y = (A + B) \bullet C + (D + E) \bullet F$
tpd (Y) = 1.25ns
tpd*(Y) = 1.45ns
tpd – ($\overline{Y}$) = 1.25ns
tpd – *($\overline{Y}$) = 1.45ns
tpd + ($\overline{Y}$) = 1.45ns
tpd + *($\overline{Y}$) = 1.60ns
PD = 31.2mW

H17



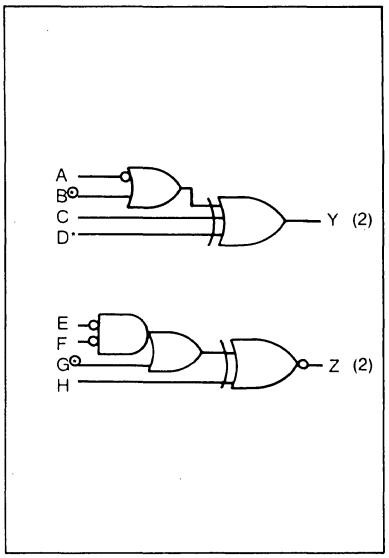
$Y = \overline{A} \bullet \overline{B} + \overline{C} \bullet \overline{D} + F \bullet \overline{E} \bullet \overline{G}$
tpd (Y) = 1.35ns
tpd*(Y) = 1.55ns
tpd – ($\overline{Y}$) = 1.35ns
tpd – *($\overline{Y}$) = 1.55ns
tpd + ($\overline{Y}$) = 1.5ns
tpd + *($\overline{Y}$) = 1.75ns
PD = 31.2mW

H18



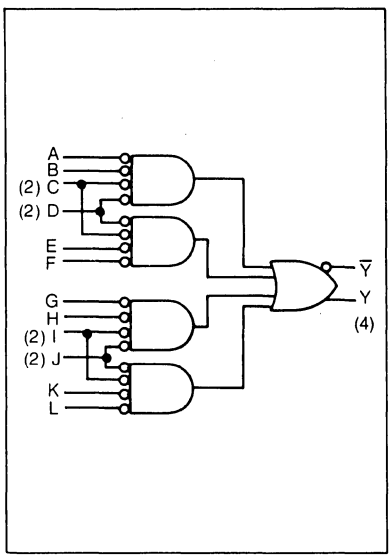
$Y = (\overline{A} \bullet \overline{B} + C) \bullet D + \overline{(\overline{A} \bullet \overline{B} + C)} \bullet (\overline{D} + E)$
tpd = 1.4ns
tpd* = 1.6ns
PD = 31.2mW

M19



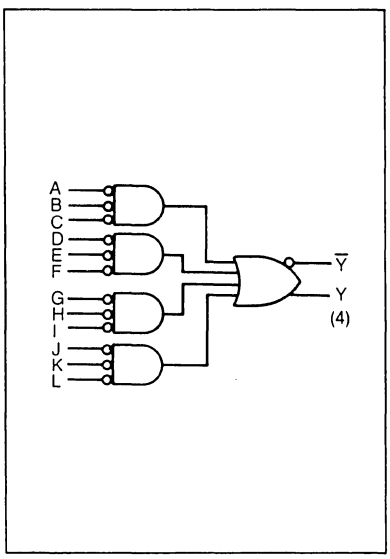
$Y = (\overline{A} + B) \oplus C \oplus D$
$Z = (\overline{E} \bullet \overline{F} + G) \oplus H$
tpd (Y) = 1.4ns
tpd (Z) = 1.25ns
tpd*(B → Y, G → Z) = 1.6ns
tpd*(D → Y) = 1.8ns
PD = 28.6mW

M20



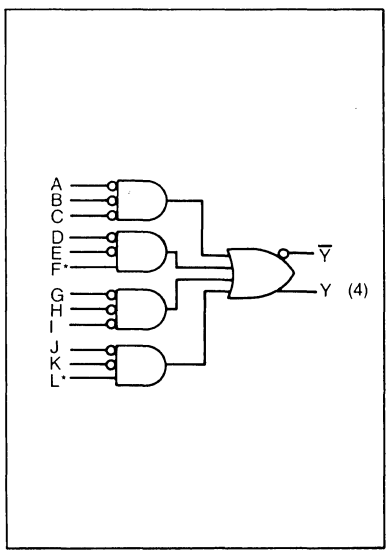
$Y = \overline{A} \bullet \overline{B} \bullet \overline{C} \bullet \overline{D} + \overline{E} \bullet \overline{F} \bullet \overline{C} \bullet \overline{D} + \overline{G} \bullet \overline{H} \bullet \overline{I} \bullet \overline{J} + \overline{K} \bullet \overline{L} \bullet \overline{I} \bullet \overline{J}$
tpd (Y) = 1.2ns
tpd – ($\overline{Y}$) = 1.3ns
tpd + ($\overline{Y}$) = 1.5ns
PD = 20.8mW

M21



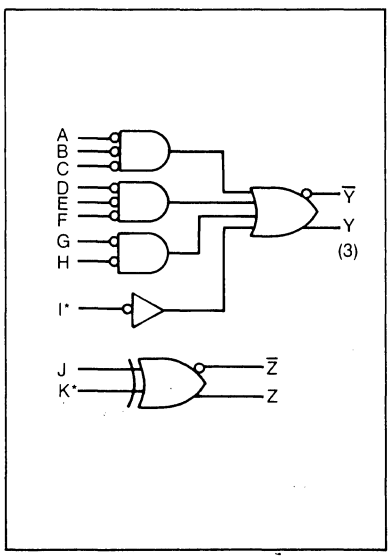
$Y = \overline{A} \bullet \overline{B} \bullet \overline{C} + \overline{D} \bullet \overline{E} \bullet \overline{F} + \overline{G} \bullet \overline{H} \bullet \overline{I} + \overline{J} \bullet \overline{K} \bullet \overline{L}$
tpd (Y) = 1.2ns
tpd – ($\overline{Y}$) = 1.3ns
tpd + ($\overline{Y}$) = 1.5ns
PD = 20.8mW

M22



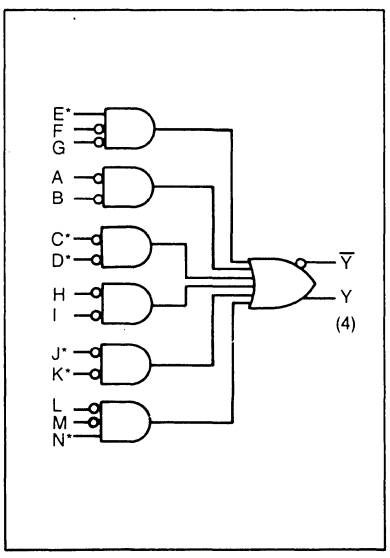
$Y = \overline{A} \bullet \overline{B} \bullet \overline{C} + \overline{D} \bullet \overline{E} \bullet F + \overline{G} \bullet \overline{H} \bullet \overline{I} + \overline{J} \bullet \overline{K} \bullet L$
tpd (Y) = 1.15ns
tpd*(Y) = 1.3ns
tpd – ($\overline{Y}$) = 1.35ns
tpd + ($\overline{Y}$) = 1.55ns
tpd – *($\overline{Y}$) = 1.75ns
tpd + *($\overline{Y}$) = 2.0ns
PD = 26mW

M23



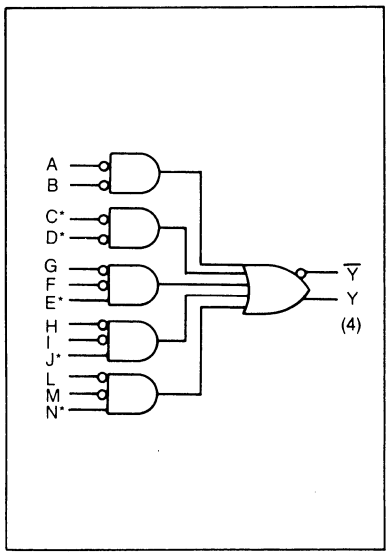
$Y = \overline{A} \bullet \overline{B} \bullet \overline{C} + \overline{D} \bullet \overline{E} \bullet \overline{F} + \overline{G} \bullet \overline{H} + \overline{I}$
$Z = J \oplus K$
tpd (Y) = 1.15 ns
tpd*(Y) = 1.45 ns
tpd (Z,$\overline{Z}$) = 1.05 ns
tpd*(Z,$\overline{Z}$) = 1.4 ns
tpd – ($\overline{Y}$) = 1.3 ns
tpd – *($\overline{Y}$) = 1.55 ns
tpd + ($\overline{Y}$) = 1.5 ns
tpd + ($\overline{Y}$) = 1.7 ns
PD = 26mW

M24



$Y = \overline{A} \bullet \overline{B} + \overline{C} \bullet \overline{D} + E \bullet \overline{F} \bullet \overline{G} + \overline{H} \bullet \overline{I} + \overline{J} \bullet \overline{K} + \overline{L} \bullet \overline{M} \bullet N$
tpd (Y) = 1.1ns
tpd – *(Y) = 1.35ns
tpd + *(Y) = 1.55ns
tpd – ($\overline{Y}$) = 1.7ns
tpd + ($\overline{Y}$) = 1.55ns
tpd – *($\overline{Y}$) = 1.75ns
tpd + *($\overline{Y}$) = 1.95ns
PD = 31.2mW

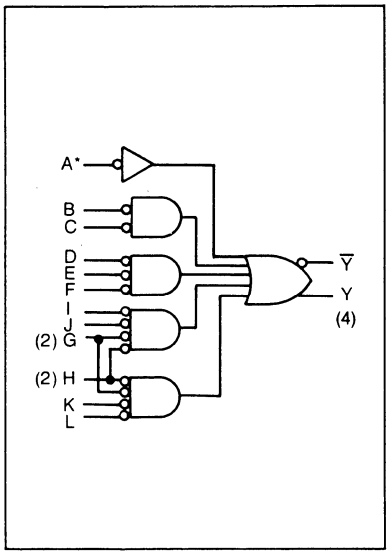
M25



$Y = \overline{A} \bullet \overline{B} + \overline{C} \bullet \overline{D} + E \bullet \overline{F} \bullet \overline{G} + \overline{H} \bullet \overline{I} \bullet \overline{J} + \overline{L} \bullet \overline{M} \bullet N$

tpd (Y) = 1.1ns
tpd −*(Y) = 1.35ns
tpd +*(Y) = 1.55ns
tpd − ($\overline{Y}$) = 1.7ns
tpd + ($\overline{Y}$) = 1.55ns
tpd −*($\overline{Y}$) = 1.75ns
tpd +*($\overline{Y}$) = 1.95ns
PD = 31.2mW

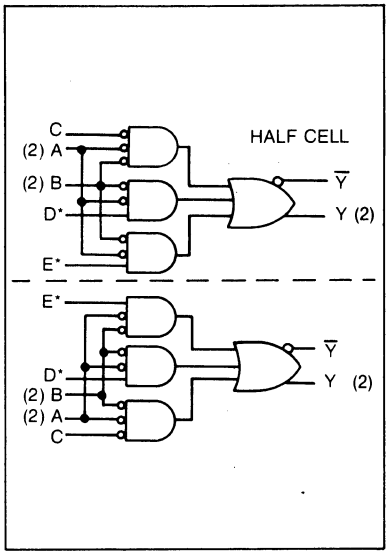
M26



$Y = \overline{A} + \overline{B} \bullet \overline{C} + \overline{D} \bullet \overline{E} \bullet \overline{F} + \overline{I} \bullet \overline{J} \bullet \overline{G} \bullet \overline{H} + \overline{K} \bullet \overline{L} \bullet \overline{G} \bullet \overline{H}$

tpd (Y) = 1.2ns
tpd − ($\overline{Y}$) = 1.45ns
tpd + ($\overline{Y}$) = 1.6ns
tpd*(Y) = 1.55ns
tpd −*($\overline{Y}$) = 1.65ns
tpd +*($\overline{Y}$) = 1.85ns
PD = 23.4mW

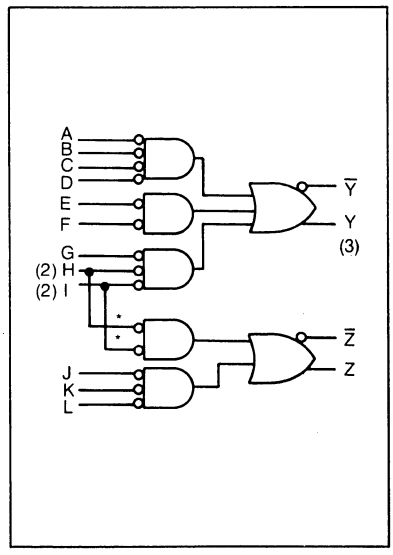
H27



$Y = \overline{C} \bullet \overline{A} \bullet \overline{B} + \overline{D} \bullet \overline{A} \bullet \overline{B} + E \bullet \overline{A} \bullet \overline{B}$

tpd(Y) = 1.0 ns
tpd*(Y) = 1.4 ns
tpd − ($\overline{Y}$) = 1.1 ns
tpd + ($\overline{Y}$) = 1.3 ns
tpd −*($\overline{Y}$) = 1.5 ns
tpd +*($\overline{Y}$) = 1.7 ns
PD = 26 mW

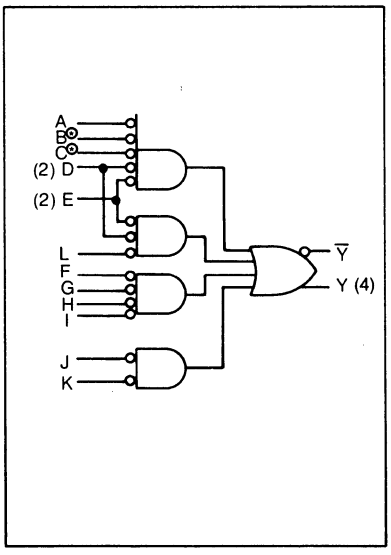
M28



$Y = \overline{A} \bullet \overline{B} \bullet \overline{C} \bullet \overline{D} + \overline{E} \bullet \overline{F} + \overline{G} \bullet \overline{H} \bullet \overline{I}$
$Z = \overline{H} \bullet \overline{I} + \overline{J} \bullet \overline{K} \bullet \overline{L}$

tpd (Y) = 1.15ns
tpd − ($\overline{Y}$) = 1.3ns
tpd + ($\overline{Y}$) = 1.5ns
tpd (Z, $\overline{Z}$) = 1.1ns
tpd +*(Z, $\overline{Z}$) = 1.3ns
tpd −*(Z, $\overline{Z}$) = 1.5ns
PD = 23.4mW

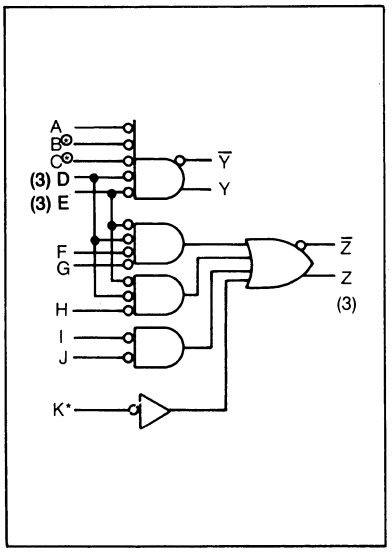
M29



$Y = \overline{A} \bullet \overline{B} \bullet \overline{C} \bullet \overline{D} \bullet \overline{E} + \overline{L} \bullet \overline{D} \bullet \overline{E} + \overline{F} \bullet \overline{G} \bullet \overline{H} \bullet \overline{I} + \overline{J} \bullet \overline{K}$

tpd (Y) = 1.4ns
tpd ($\overline{Y}$) = 1.5ns
tpd*(Y) = 1.7ns
tpd*($\overline{Y}$) = 1.8ns
PD = 23.4mW

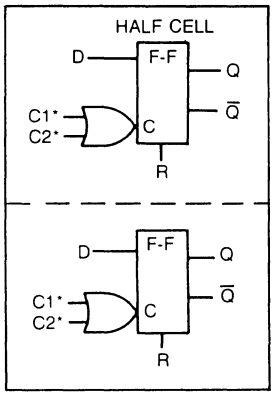
M3ø



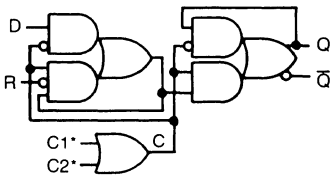
$Y = \overline{A} \bullet \overline{B} \bullet \overline{C} \bullet \overline{D} \bullet \overline{E}$
$Z = \overline{F} \bullet \overline{G} \bullet \overline{D} \bullet \overline{E} + \overline{H} \bullet \overline{D} \bullet \overline{E} + \overline{I} \bullet \overline{J} + \overline{K}$

tpd (Y,$\overline{Y}$) = 1.1ns
tpd* (Y, $\overline{Y}$) = 1.4 ns
tpd (Z) = 1.15 ns
tpd*(Z) = 1.45 ns
tpd − ($\overline{Z}$) = 1.3 ns
tpd + ($\overline{Z}$) = 1.5 ns
tpd −*($\overline{Z}$) = 1.55 ns
tpd +*($\overline{Z}$) = 1.7 ns
PD = 26 mW

H31 — DUAL D F/F



LOGIC EQUIVALENT



TRUTH TABLE

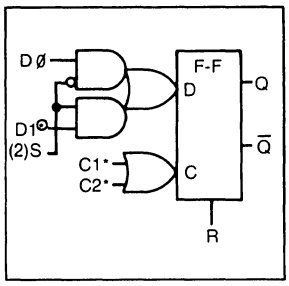
R	D	C	Q
L	X	H	—
L	X	L	—
L	L	L→H	L
L	H	L→H	H
H	X	H	L
H	X	L	—
H	L	L→H	L
H	H	L→H	⎍

tpw+ (R) = 2.5 ns min
for C1 + C2 = "H"
tpw+ (R and C1/C2 tied
together) = 4.0 ns min

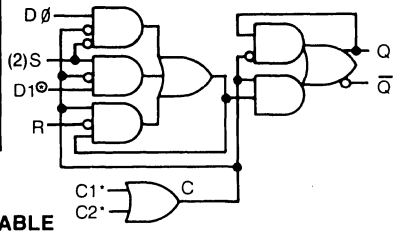
— = NO CHANGE
X = DON'T CARE
L = "LOW"
H = "HIGH"
L➔H = LOW TO HIGH TRANSITION
C = C1 + C2

tpd* = 1.5 ns
tpd (R → Q, $\overline{Q}$) = 3.5 ns
tSETUP(D) = 1.5 ns
tHOLD(D) = 0 ns
PD = 46.8 mW
tpw (C1, C2) = 2.0 ns min

M32 — D F/F W/MUX



LOGIC EQUIVALENT



TRUTH TABLE

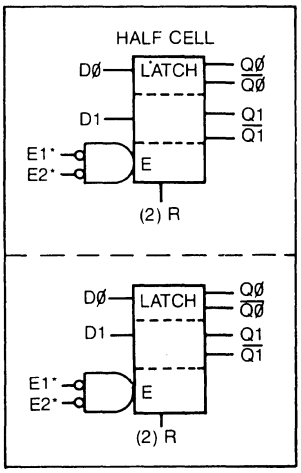
R	D	C	Q
L	X	H	—
L	X	L	—
L	L	L→H	L
L	H	L→H	H
H	X	H	L
H	X	L	—
H	L	L→H	L
H	H	L→H	⎍

tpw+ (R) = 3.5 ns min
tpw+ (R and C1/C2 tied
together) = 4.6 ns min

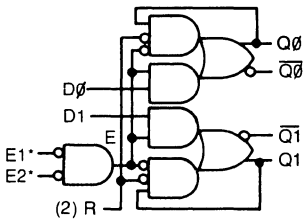
C = C1 + C2
D = DØ • $\overline{S}$ + D1 • S
tpd (C1, C2 → Q, $\overline{Q}$) = 1.6ns
tpd (R → Q, $\overline{Q}$) = 4.2 ns
tpw − (C1, C2) = 3 ns min

tSETUP(DØ, S) = 2 ns
t(SETUP(D1) = 2.5 ns
tHOLD(DØ, D1, S) = 0 ns
PD = 31.2 mW
tpw + (C1, C2) = 2 ns min

H33 — DUAL 2 BIT LATCH



LOGIC EQUIVALENT



TRUTH TABLE

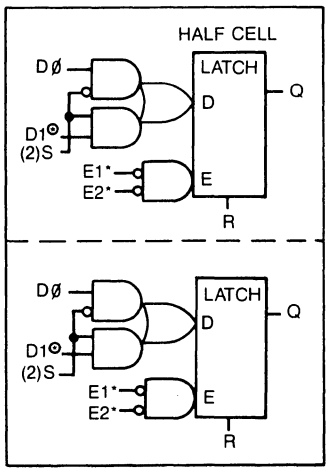
R	Di	E1	E2	Qi
L	X	H	X	—
L	X	X	H	—
H	X	H	X	L
H	X	X	H	L
X	L	L	L	L
X	H	L	L	H

tpw + (R and E1/E2 tied
together) = 2.5 ns min

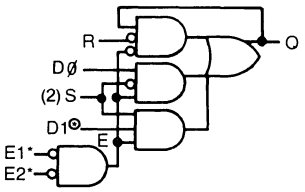
− = NO CHANGE
X = DON'T CARE
i = 0 or 1
E = $\overline{E1}$ • $\overline{E2}$
tpd = (Di→Q,$\overline{Q}$) = 1.2 ns
tpw (E1, E2) = 2.0 ns min

tpd* = 1.7 ns
tpd (R → Q,$\overline{Q}$) = 2.0 ns
tSETUP(D) = 1.5ns
tHOLD(D) = 0ns
PD = 46.3mW

H34 — DUAL LATCH W/MUX



LOGIC EQUIVALENT



TRUTH TABLE

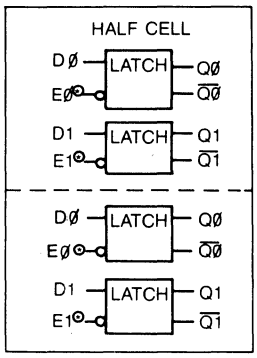
R	Di	E1	E2	Qi
L	X	H	X	—
L	X	X	H	—
H	X	H	X	L
H	X	X	H	L
X	L	L	L	L
X	H	L	L	H

tpw + (R) = 3.5 ns min
tpw + (R and E1/E2 tied
together) = 3.5 ns min

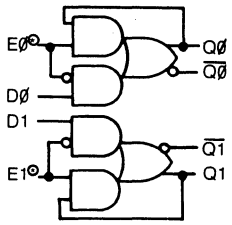
E = $\overline{E1}$ • $\overline{E2}$
D = D0 • $\overline{S}$ + D1 • S
tpd + = 1.4 ns
tpd +* = 1.65 ns
tpd− = 1.95 ns
tpd −* = 2.45 ns
tpw (E1, E2) = 3 ns min

tpd (R➔ Q) = 2.75ns
tSETUP(DØ, S) = 2ns
tSETUP(D1) = 2.5ns
tHOLD(DØ, D1, S) = 0ns
PD = 41.6mW

H35 — QUAD LATCH



LOGIC EQUIVALENT

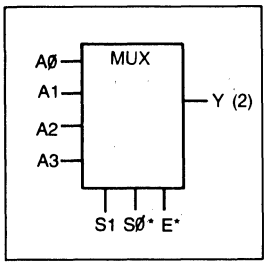


TRUTH TABLE

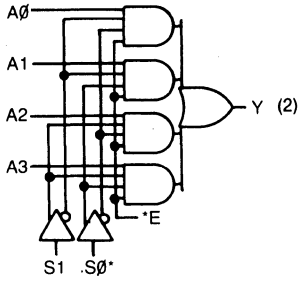
Di	Ei	Qi
X	H	—
L	L	L
H	L	H

— = NO CHANGE
X = DON'T CARE
i = 0 or 1
tpd = 1.2 ns
tpd* = 1.5 ns
tSETUP(DØ, D1) = 1.5 ns
tHOLD(DØ, D1) = 0 ns
PD = 52 mW
tpw = 2.0 ns min

M36 — 4 TO 1 MUX W/E



LOGIC EQUIVALENT

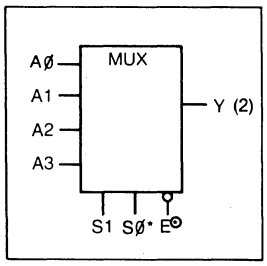


TRUTH TABLE

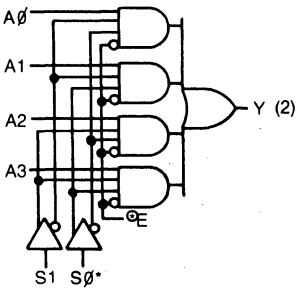
E	S1	SØ	Y
L	X	X	L
H	L	L	AØ
H	L	H	A1
H	H	L	A2
H	H	H	A3

tpd = 1.4ns
tpd*(E) = 1.4ns
tpd*(SØ) = 1.7ns
PD = 26mW

M37 — 4 TO 1 MUX W/E



LOGIC EQUIVALENT

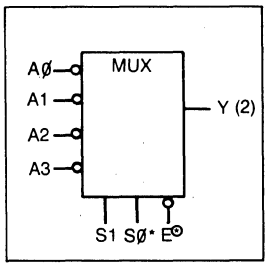


TRUTH TABLE

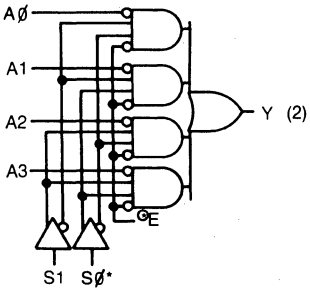
E	S1	SØ	Y
H	X	X	L
L	L	L	AØ
L	L	H	A1
L	H	L	A2
L	H	H	A3

tpd = 1.4ns
tpd*(E) = 1.4ns
tpd*(SØ) = 1.7ns
PD = 26mW

M38 — 4 TO 1 MUX W/E



LOGIC EQUIVALENT

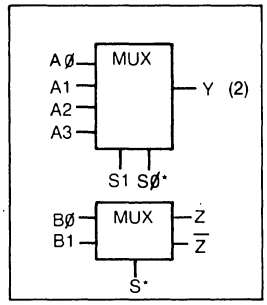


TRUTH TABLE

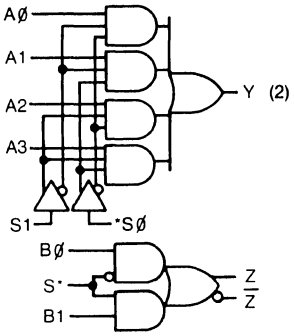
E	S1	SØ	Y
H	X	X	L
L	L	L	$\overline{AØ}$
L	L	H	$\overline{A1}$
L	H	L	$\overline{A2}$
L	H	H	$\overline{A3}$

tpd = 1.5ns
tpd*(E) = 1.6ns
tpd*(SØ) = 1.95ns
PD = 26mW

M39 — 4 TO 1, 2 TO 1 MUX



LOGIC EQUIVALENT



TRUTH TABLES

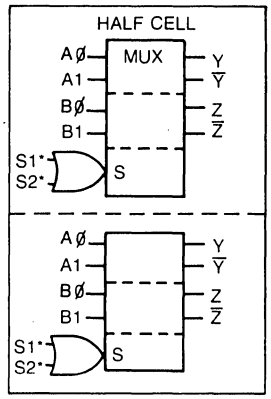
S1	SØ	Y
L	L	AØ
L	H	A1
H	L	A2
H	H	A3

S	Z
L	BØ
H	B1

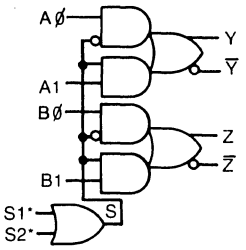
tpd (Y) = 1.4ns
tpd –*(Y) = 1.95ns
tpd +*(Y) = 2.1ns

tpd (Z, $\overline{Z}$) = 1.05 ns
tpd*(Z, $\overline{Z}$) = 1.35 ns
PD = 26 mW

H40 — QUAD 2 TO 1 MUX, COM SEL



LOGIC EQUIVALENT

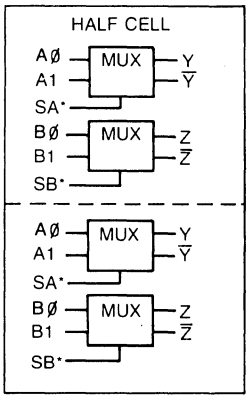


TRUTH TABLE

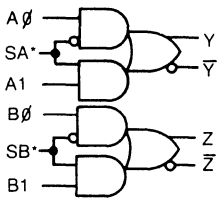
S	Y	Z
L	AØ	BØ
H	A1	B1

S = S1 + S2
tpd = 1.05ns
tpd* = 1.4ns
PD = 26mW

H41 — QUAD 2 TO 1 MUX



LOGIC EQUIVALENT

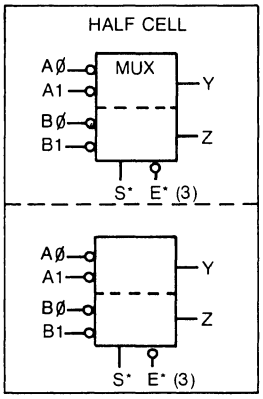


TRUTH TABLES

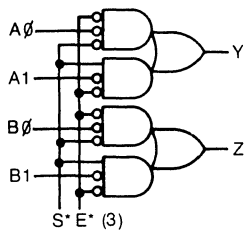
SA	Y	SB	Z
L	AØ	L	BØ
H	A1	H	B1

tpd = 1.05ns
tpd* = 1.4ns
PD = 31.2mW

H42 — QUAD TO 1 MUX W/E



LOGIC EQUIVALENT

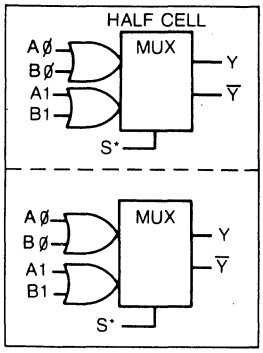


TRUTH TABLES

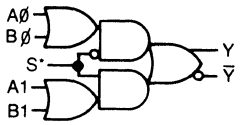
E	S	Y	Z
H	X	L	L
L	L	$\overline{AØ}$	$\overline{BØ}$
L	H	$\overline{A1}$	$\overline{B1}$

tpd = 1.15ns
tpd –*(S) = 1.55ns
tpd +*(S) = 1.9ns
tpd –*(E) = 1.65ns
tpd +*(E) = 2.0ns
PD = 26mW

H43 — DUAL 2 TO 1 MUX



LOGIC EQUIVALENT

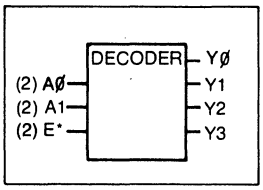


TRUTH TABLE

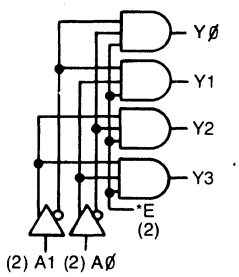
S	Y
L	AØ+BØ
H	A1+B1

tpd = 1.3ns
tpd* = 1.6ns
PD = 15.6mW

M44 — 1/4 DECODER (HIGH)



LOGIC EQUIVALENT

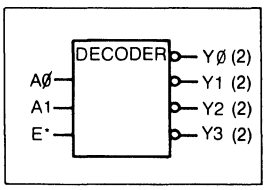


TRUTH TABLE

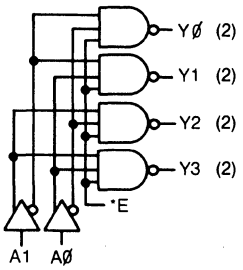
E	A1	AØ	YØ	Y1	Y2	Y3
L	X	X	L	L	L	L
H	L	L	H	L	L	L
H	L	H	L	H	L	L
H	H	L	L	L	H	L
H	H	H	L	L	L	H

tpd = 1.2ns
tpd* = 1.4ns
PD = 26mW

M45 — 1/4 DECODER (LOW)



LOGIC EQUIVALENT

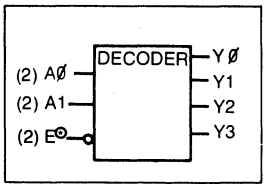


TRUTH TABLE

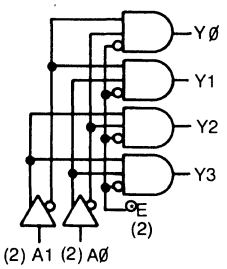
E	A1	AØ	YØ	Y1	Y2	Y3
L	X	X	H	H	H	H
H	L	L	L	H	H	H
H	L	H	H	L	H	H
H	H	L	H	H	L	H
H	H	H	H	H	H	L

tpd = 1.3ns
tpd+* = 1.7ns
tpd−* = 1.9ns
PD = 13mW

M46 — 1/4 DECODER (HIGH)



LOGIC EQUIVALENT

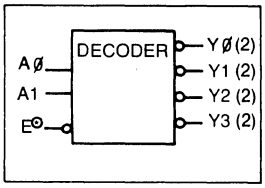


TRUTH TABLE

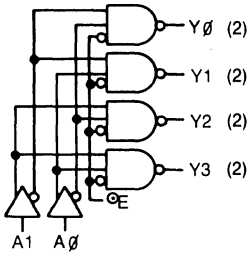
E	A1	AØ	YØ	Y1	Y2	Y3
H	X	X	L	L	L	L
L	L	L	H	L	L	L
L	L	H	L	H	L	L
L	H	L	L	L	H	L
L	H	H	L	L	L	H

tpd = 1.2ns
tpd* = 1.4ns
PD = 26mW

M47 — 1/4 DECODE (LOW)



LOGIC EQUIVALENT

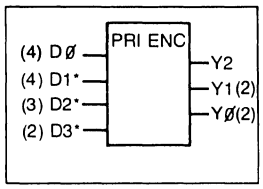


TRUTH TABLE

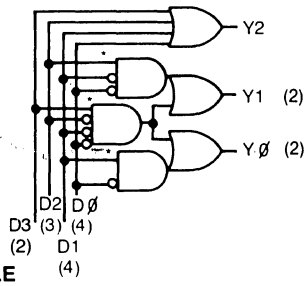
E	A1	AØ	YØ	Y1	Y2	Y3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

tpd = 1.3ns
tpd +* = 1.7ns
tpd −* = 1.9ns
PD = 13mW

M48 — PRIORITY ENCODER



LOGIC EQUIVALENT

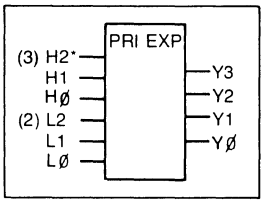


TRUTH TABLE

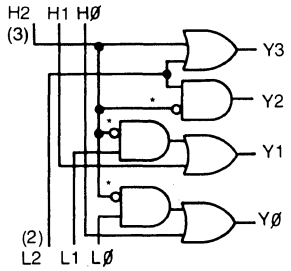
DØ	D1	D2	D3	Y2	Y1	YØ
L	L	L	L	L	L	L
H	X	X	X	H	L	L
L	H	X	X	H	L	H
L	L	H	X	H	H	L
L	L	L	H	H	H	H

tpd = 1.2ns
tpd −* = 1.35ns
tpd +* = 1.65ns
PD = 28.6mW

M49 — PRIORITY EXPANDER



LOGIC EQUIVALENT

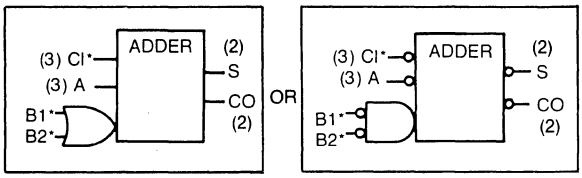


TRUTH TABLE

H2	H1	HØ	L2	L1	LØ	Y3	Y2	Y1	Y0
L	L	L	L	L	L	L	L	L	L
H	L	L	X	X	X	H	L	L	L
H	L	H	X	X	X	H	L	L	H
H	H	L	X	X	X	H	L	H	L
H	H	H	X	X	X	H	L	H	H
L	L	L	H	L	L	H	H	L	L
L	L	L	H	L	H	H	H	L	H
L	L	L	H	H	L	H	H	H	L
L	L	L	H	H	H	H	H	H	H

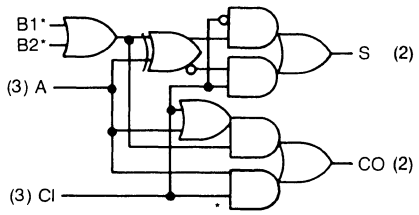
tpd = 1.1ns
tpd* = 1.4ns
PD = 26mW

M5Ø — FULL ADDER



NOTE: CIRCLE AT INPUT OR OUTPUT INDICATE AN ACTIVE "LOW" SIGNAL

LOGIC EQUIVALENT

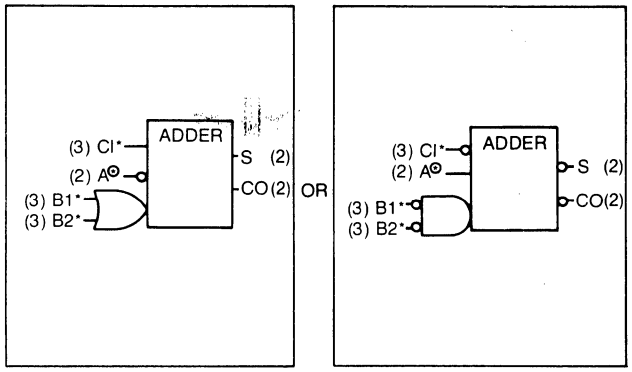


TRUTH TABLE

A	B1	B2	CI	S	CO
L	L	L	L	L	L
L	L	L	H	H	L
L	H	X	L	H	L
L	X	H	L	H	L
L	H	X	H	L	H
L	X	H	H	L	H
H	L	L	L	H	L
H	L	L	H	L	H
H	H	X	L	L	H
H	X	H	L	L	H
H	H	X	H	H	H
H	X	H	H	H	H

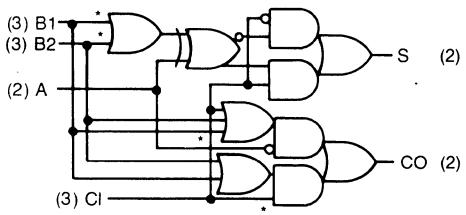
tpd (A, CI → S) = 1.35ns
tpd (A → CO) = 1.2ns
tpd (B1, B2 → S) = 1.7ns
tpd (B1, B2, CI → CO) = 1.35ns
PD = 26mW

M51 — FULL ADDER



NOTE: CIRCLE AT INPUT OR OUTPUT INDICATE AN ACTIVE "LOW" SIGNAL

LOGIC EQUIVALENT

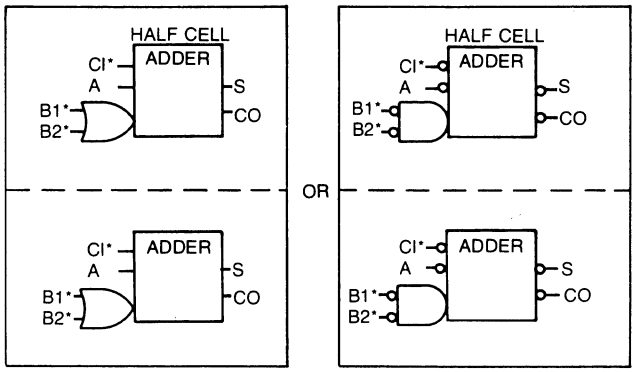


TRUTH TABLE

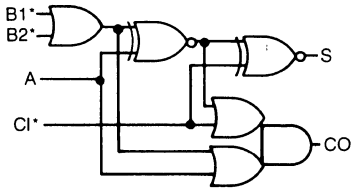
A	B1	B2	CI	S	CO
H	L	L	L	L	L
H	L	L	H	H	L
H	H	X	L	H	L
H	X	H	L	H	L
H	H	X	H	L	H
H	X	H	H	L	H
L	L	L	L	H	L
L	L	L	H	L	H
L	H	X	L	L	H
L	X	H	L	L	H
L	H	X	H	H	H
L	X	H	H	H	H

tpd (A, CI → S) = 1.35ns
tpd (B1, B2 → S) = 1.7ns
tpd (B1, B2 → CO) = 1.2ns
tpd (A, CI → CO) = 1.4ns
PD = 28.6mW

H52 — DUAL FULL ADDER



LOGIC EQUIVALENT

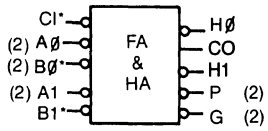


TRUTH TABLE

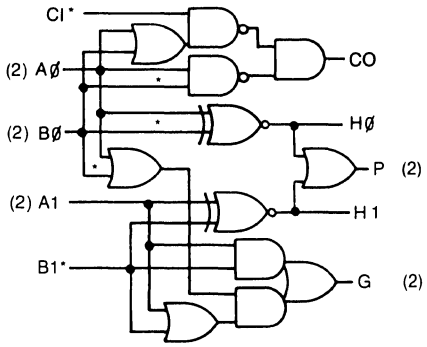
A	B1	B2	CI	S	CO
L	L	L	L	L	L
L	L	L	H	H	L
L	H	X	L	H	L
L	X	H	L	H	L
L	H	X	H	L	H
L	X	H	H	L	H
H	L	L	L	H	L
H	L	L	H	L	H
H	H	X	L	L	H
H	X	H	L	L	H
H	H	X	H	H	H
H	X	H	H	H	H

tpd (CI → S, CO) = 1.6ns
tpd (A → S, CO) = 2.2ns
tpd (B1, B2 → S, CO) = 2.8ns
PD = 36.4mW

M53 — FULL ADDER & HALF ADDER



LOGIC EQUIVALENT



NOTE: If P and H1 outputs are both loaded, output current is limited to 0.5 or 1.0 mA.

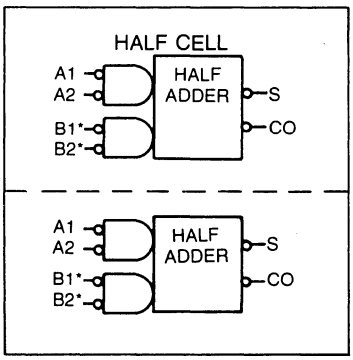
TRUTH TABLES

A1	B1	AØ	BØ	G	P	HØ	H1
L	L	L	L	L	H	H	H
L	L	L	H	L	H	L	H
L	L	H	L	L	H	L	H
L	L	H	H	L	H	H	H
L	H	L	L	L	H	H	L
L	H	L	H	H	L	L	L
L	H	H	L	H	L	L	L
L	H	H	H	H	H	H	L
H	L	L	L	L	H	H	L
H	L	L	H	H	L	L	L
H	L	H	L	H	L	L	L
H	L	H	H	H	H	H	L
H	H	L	L	H	H	H	H
H	H	L	H	H	H	L	H
H	H	H	L	H	H	L	H
H	H	H	H	H	H	H	H

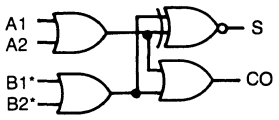
AØ	BØ	CI	CO
L	L	L	H
L	L	H	H
L	H	L	H
L	H	H	L
H	L	L	H
H	L	H	L
H	H	L	L
H	H	H	L

tpd = 1.35 ns
tpd−(BØ, B1 → P, G, HØ, H1) = 1.8 ns
tpd+(BØ, B1 → P, G, HØ, H1) = 2.0 ns
tpd (BØ, C1 → CO) = 1.55 ns
PD = 28.6 mW

H54 — DUAL HALF ADDER



LOGIC EQUIVALENT

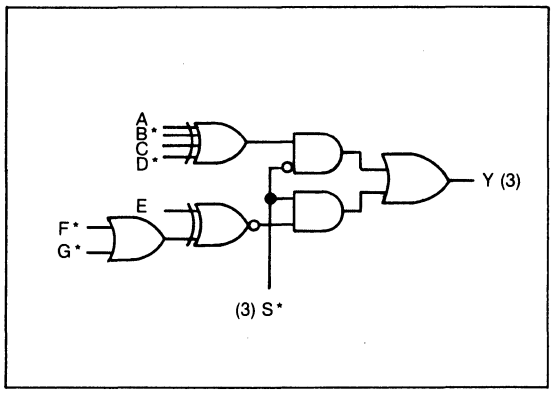


TRUTH TABLE

A1	A2	B1	B2	S	CO
L	L	L	L	H	L
L	L	H	X	L	H
L	L	X	H	L	H
H	X	L	L	L	H
X	H	L	L	L	H
X	H	X	H	H	H
X	H	H	X	H	H
H	X	X	H	H	H
H	X	H	X	H	H

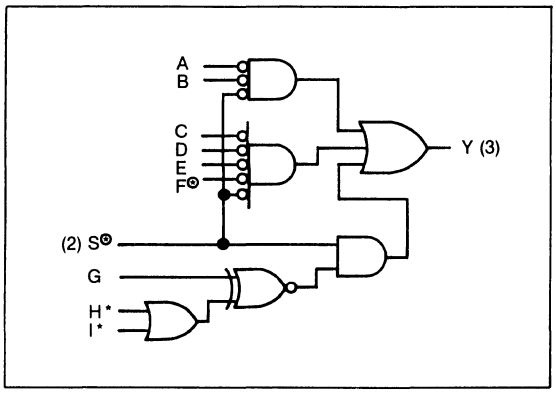
tpd = 1.2ns
tpd* = 1.5ns
PD = 15.6mW

M55



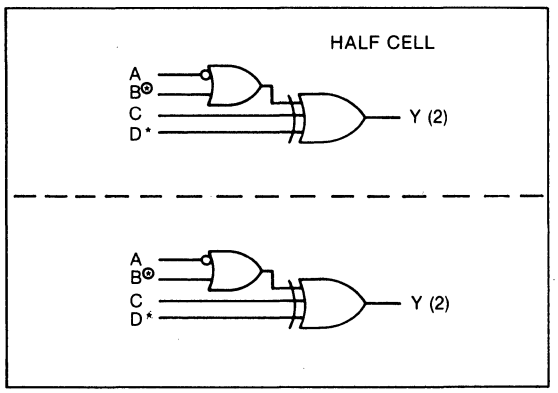
$Y = (A \oplus B \oplus C \oplus D) \cdot \overline{S} + [\overline{E} \oplus (F + G)] \cdot S$
tpd = 1.45 ns
tpd*(F,G) = 1.75 ns
tpd *(B,D) = 1.95 ns
tpd*(S) = 2.15 ns
PD = 28.6 mW

M56



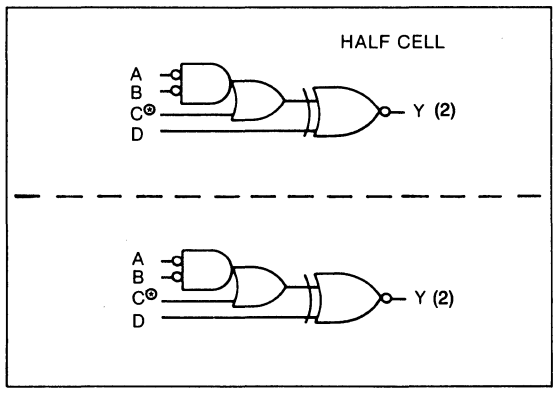
$Y = \overline{A} \cdot \overline{B} \cdot \overline{S} + \overline{C} \cdot \overline{D} \cdot \overline{E} \cdot \overline{F} \cdot \overline{S}$
$+[\overline{G} \oplus (H+I)] \cdot S$
tpd = 1.45 ns
tpd*(F) = 1.6 ns
tpd*(H,I,S) = 1.75 ns
PD = 28.6 mW

H57



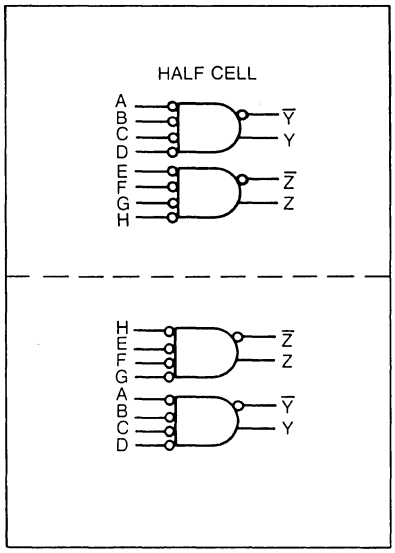
$Y = (\overline{A} + B) \oplus C \oplus D$
tpd = 1.4ns
tpd* (B → Y) = 1.6ns
tpd* (D → Y) = 1.8ns
PD = 31.2mW

H58



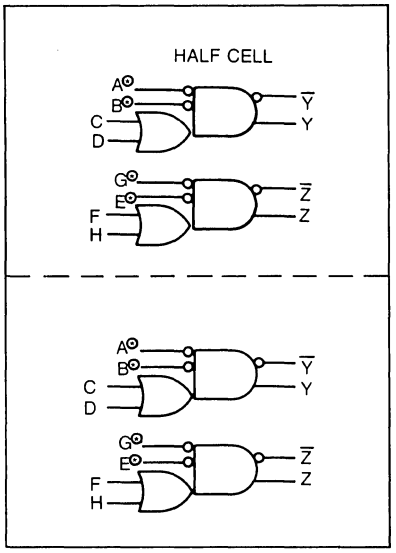
$Y = (\overline{A} \cdot \overline{B} + C) \overline{\oplus} D$
tpd = 1.25ns
tpd* = 1.6ns
PD = 26mW

H59



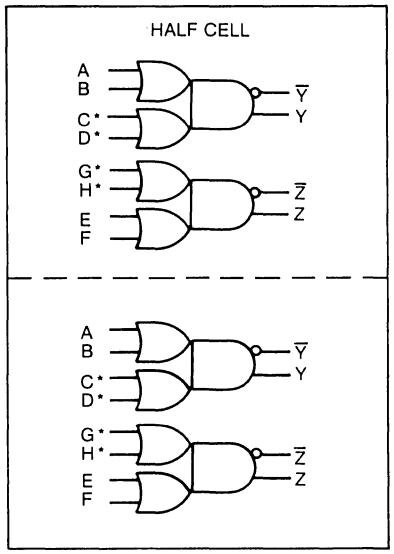
$Y = \overline{A} \bullet \overline{B} \bullet \overline{C} \bullet \overline{D}$
$\overline{Y} = A + B + C + D$
$Z = \overline{E} \bullet \overline{F} \bullet \overline{G} \bullet \overline{H}$
$\overline{Z} = E + F + G + H$
tpd = 1.2ns
PD = 20.8mW

H60



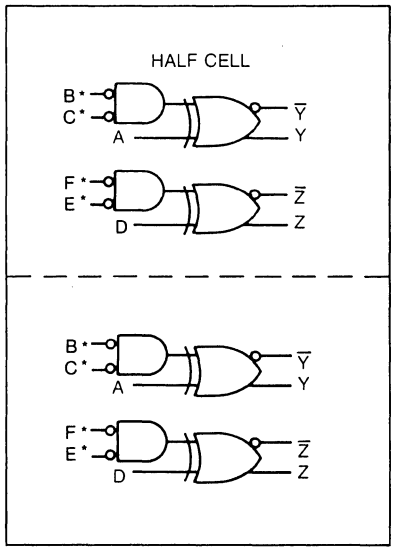
$Y = \overline{A} \bullet \overline{B} \bullet (C + D)$
$Z = \overline{G} \bullet \overline{E} \bullet (F + H)$
tpd = 1.1ns
tpd* (Y, Z) = 1.3ns
tpd+* $(\overline{Y}, \overline{Z})$ = 1.3ns
tpd−*$(\overline{Y}, \overline{Z})$ = 1.5ns
PD = 31.2mW

H61



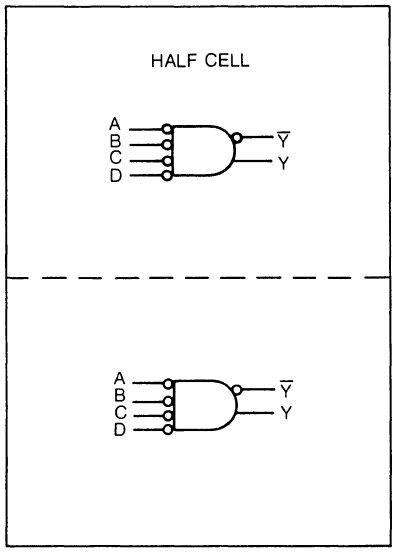
$Y = (A + B) \bullet (C + D)$
$Z = (E + F) \bullet (G + H)$
tpd = 1.1ns
tpd* = 1.4ns
PD = 31.2mW

H62



$Y = A \oplus (\overline{B} \bullet \overline{C})$
$Z = D \oplus (\overline{E} \bullet \overline{F})$
tpd = 1.05ns
tpd* = 1.4ns
PD = 31.2mW

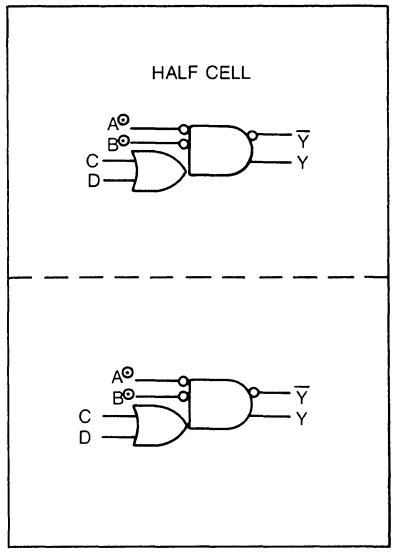
H63



$Y = \overline{A} \bullet \overline{B} \bullet \overline{C} \bullet \overline{D}$
$\overline{Y} = A + B + C + D$
tpd = 1.2ns
PD = 10.4mW

NOTE: Y and $\overline{Y}$ outputs are limited to .5 or 1 mA output current if both outputs are loaded.

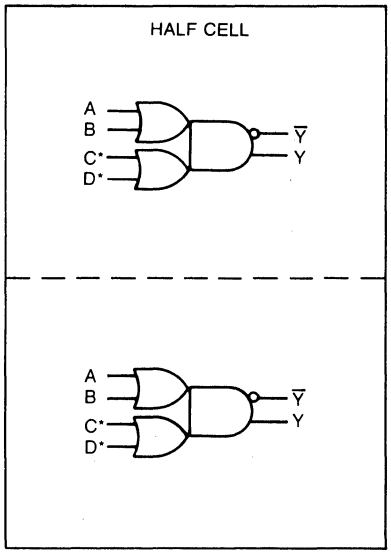
H64



$Y = \overline{A} \bullet \overline{B} \bullet (C + D)$
tpd = 1.1 ns
tpd*(Y) = 1.3 ns
tpd+*$(\overline{Y})$ = 1.3 ns
tpd−*$(\overline{Y})$ = 1.5 ns
PD = 15.6 mW

NOTE: Y and $\overline{Y}$ outputs are limited to .5 or 1 mA output current if both outputs are loaded.

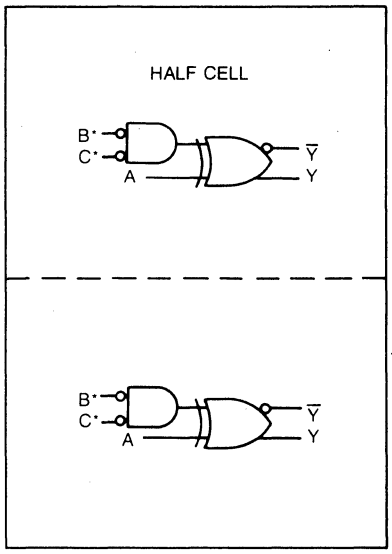
H65



$Y = (A + B) \bullet (C + D)$
tpd = 1.1ns
tpd* = 1.4ns
PD = 15.6mW

NOTE: Y and $\overline{Y}$ outputs are limited to .5 or 1 mA output current if both outputs are loaded.

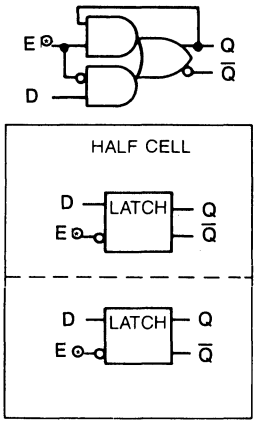
H66



$Y = A \oplus (\overline{B} \bullet \overline{C})$
tpd = 1.05ns
tpd* = 1.4ns
PD = 15.6mW

NOTE: Y and $\overline{Y}$ outputs are limited to .5 or 1 mA output current if both outputs are loaded.

H67 — DUAL LATCH LOGIC EQUIVALENT



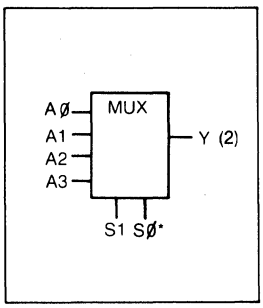
NOTE: Q and $\overline{Q}$ outputs are limited to .5 or 1 mA output current if both outputs are loaded.

TRUTH TABLE

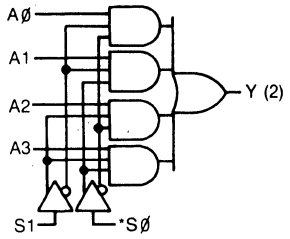
D	E	Q
X	H	—
L	L	L
H	L	H

— = NO CHANGE
X = DON'T CARE
tpd = 1.2 ns
tpd* = 1.5 ns
tSETUP = 1.5 ns
tHOLD = 0 ns
PD = 26 mW
tpw = 2.0 ns min

M68 — 4 TO 1 MUX



LOGIC EQUIVALENT

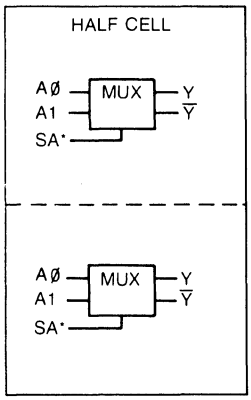


TRUTH TABLES

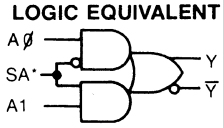
S1	SØ	Y
L	L	AØ
L	H	A1
H	L	A2
H	H	A3

tpd (Y) = 1.4ns
tpd +*(Y) = 2.1ns
tpd −*(Y) = 1.95ns
PD = 18.2mW

H69 — DUAL 2 TO 1 MUX



LOGIC EQUIVALENT



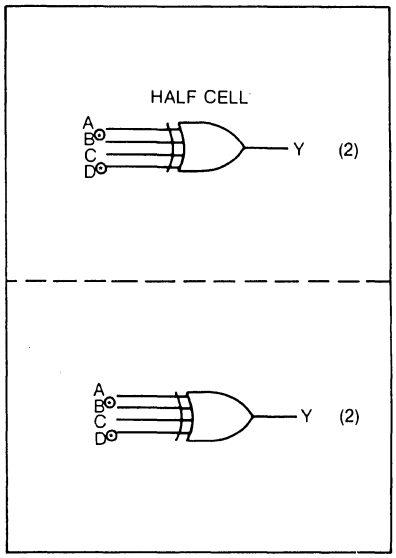
TRUTH TABLES

SA	Y
L	AØ
H	A1

tpd = 1.05ns
tpd* = 1.4ns
PD = 13mW

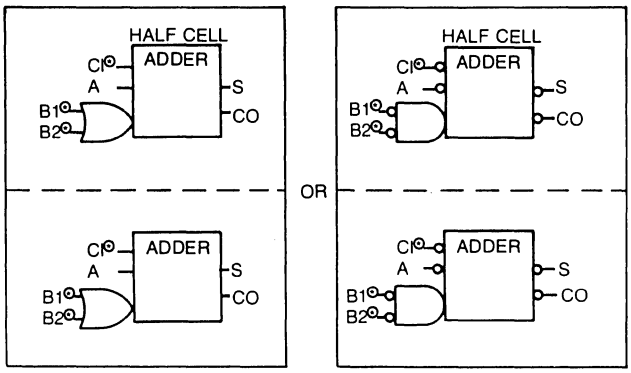
NOTE: Y and $\overline{Y}$ outputs are limited to .5 or 1 mA output current if both outputs are loaded.

H71

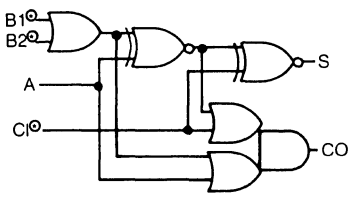


$Y = A \oplus B \oplus C \oplus D$
tpd = 1.2 ns
tpd +* = 1.7 ns
tpd −* = 1.8 ns
PD: = 34.4 mW

H72 — DUAL FULL ADDER



LOGIC EQUIVALENT



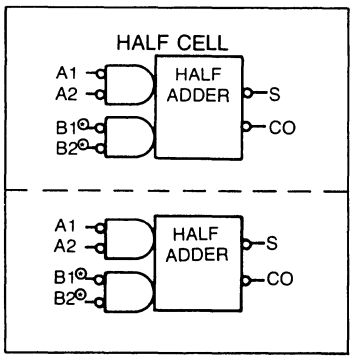
TRUTH TABLE

A	B1	B2	CI	S	CO
L	L	L	L	L	L
L	L	L	H	H	L
L	H	X	L	H	L
L	X	H	L	H	L
L	H	X	H	L	H
L	X	H	H	L	H
H	L	L	L	H	L
H	L	L	H	L	H
H	H	X	L	L	H
H	X	H	L	L	H
H	H	X	H	H	H
H	X	H	H	H	H

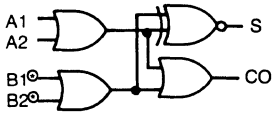
tpd (CI → S, CO) = 1.75 ns tpd (A → S, CO) = 2.2 ns
tpd (B1, B2 → S, CO) = 2.95 ns
PD = 39.6 mW

NOTE: outputs can be selected for 0, .5, or 1 mA only.

H73 — DUAL HALF ADDER



LOGIC EQUIVALENT

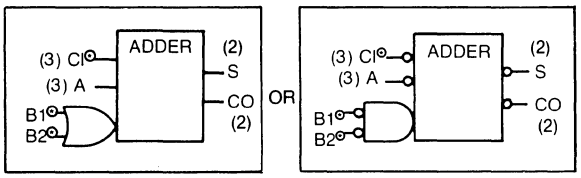


TRUTH TABLE

A1	A2	B1	B2	S	CO
L	L	L	L	H	L
L	L	H	X	L	H
L	L	X	H	L	H
H	X	L	L	L	H
X	H	L	L	L	H
X	H	X	H	H	H
X	H	H	X	H	H
H	X	X	H	H	H
H	X	H	X	H	H

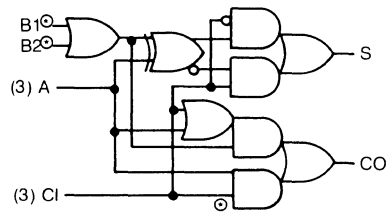
tpd = 1.2 ns
tpd* = 1.65 ns
PD = 17.2 mW

M74 — FULL ADDER



NOTE: CIRCLE AT INPUT OR OUTPUT INDICATE AN ACTIVE "LOW" SIGNAL

LOGIC EQUIVALENT

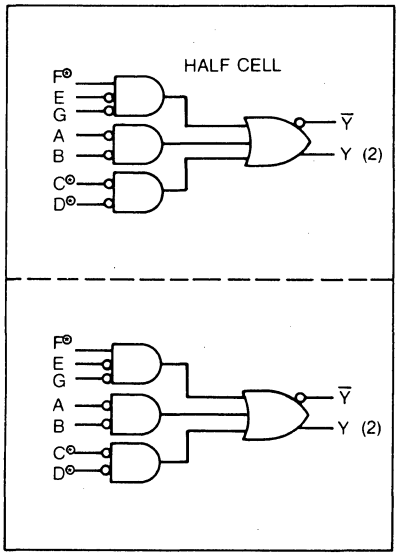


TRUTH TABLE

A	B1	B2	CI	S	CO
L	L	L	L	L	L
L	L	L	H	H	L
L	H	X	L	H	L
L	X	H	L	H	L
L	H	X	H	L	H
L	X	H	H	L	H
H	L	L	L	H	L
H	L	L	H	L	H
H	H	X	L	L	H
H	X	H	L	L	H
H	H	X	H	H	H
H	X	H	H	H	H

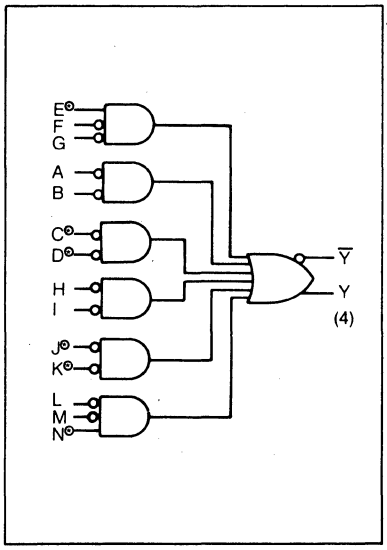
tpd (A, CI → S) = 1.35 ns
tpd (A → CO) = 1.2 ns
PD = 28.5 mW
tpd (B1, B2 → S) = 1.85 ns
tpd (B1, B2, CI → CO) = 1.5 ns

H75



$Y = \overline{A} \cdot \overline{B} + \overline{C} \cdot \overline{D} + F \cdot \overline{E} \cdot \overline{G}$
tpd (Y) = 1.35 ns
tpd*(Y) = 1.7 ns
tpd−($\overline{Y}$) = 1.35 ns
tpd+($\overline{Y}$) = 1.5 ns
tpd−*($\overline{Y}$) = 1.7 ns
tpd+*($\overline{Y}$) = 1.9 ns
PD = 31.2 mW

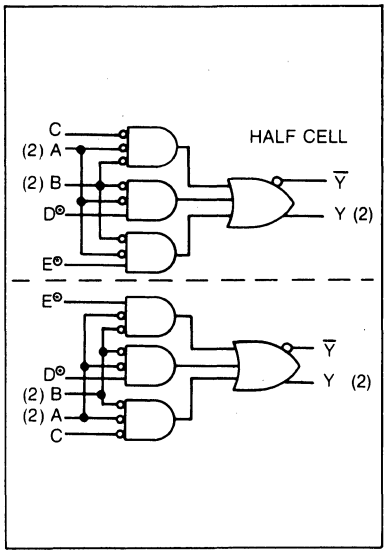
M76



$Y = \overline{A} \cdot \overline{B} + \overline{C} \cdot \overline{D} + E \cdot \overline{F} \cdot \overline{G} + \overline{H} \cdot \overline{I} + \overline{J} \cdot \overline{K} + \overline{L} \cdot \overline{M} \cdot N$
tpd−*(Y) = 1.5 ns
tpd+*(Y) = 1.7 ns
PD = 31.2 mW

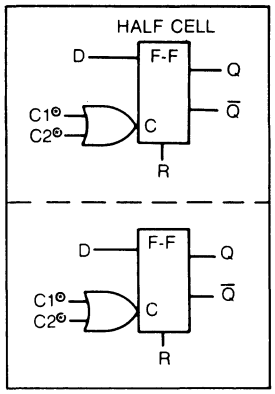
tpd (Y) = 1.1 ns
tpd−($\overline{Y}$) = 1.7 ns
tpd+($\overline{Y}$) = 1.55 ns
tpd−*($\overline{Y}$) = 1.9 ns
tpd+*($\overline{Y}$) = 2.1 ns

H77

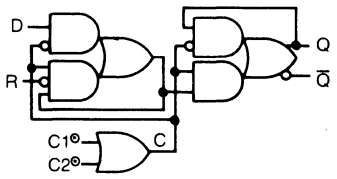


$Y = \overline{C} \cdot \overline{A} \cdot \overline{B} + D \cdot \overline{A} \cdot \overline{B} + E \cdot \overline{A} \cdot \overline{B}$
tpd(Y) = 1.0 ns
tpd−($\overline{Y}$) = 1.1ns
tpd+($\overline{Y}$) = 1.3 ns
PD = 30 mW
tpd*(Y) = 1.55 ns
tpd−*($\overline{Y}$) = 1.65 ns
tpd+*($\overline{Y}$) = 1.85 ns

H78 — DUAL D F/F



LOGIC EQUIVALENT



$t_{SETUP}(D)$ = 1.5 ns
$t_{HOLD}(D)$ = 0 ns
tpw (C1, C2) = 2.0 ns min

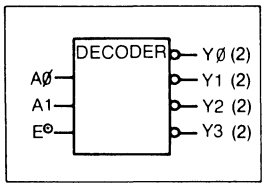
TRUTH TABLE

R	D	C	Q
L	X	H	—
L	X	L	—
L	L	L→H	L
L	H	L→H	H
H	X	H	L
H	X	L	—
H	L	L→H	L
H	H	L→H	⊓

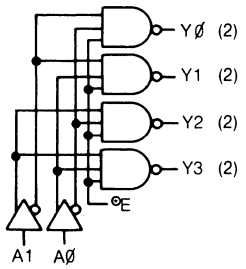
tpw+ (R) = 2.5 ns min
for C1 + C2 = "H"
tpw+ (R and C1/C2 tied together) = 3.85 ns min

$\overline{Q}$ output cannot be selected for 2 mA
— = No Change X = Don't Care
L = "Low", H = "High"
L→H = Low to High Transition
C = C1 + C2 tpd* = 1.65 ns
tpd (R → Q,$\overline{Q}$) = 3.5 ns PD = 52.8 mW

M79 — 1/4 DECODER (LOW)



LOGIC EQUIVALENT



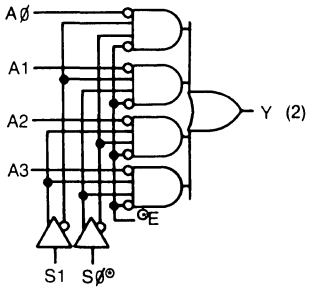
TRUTH TABLE

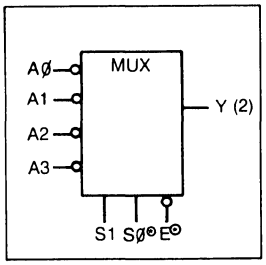
E	A1	AØ	YØ	Y1	Y2	Y3
L	X	X	H	H	H	H
H	L	L	L	H	H	H
H	L	H	H	L	H	H
H	H	L	H	H	L	H
H	H	H	H	H	H	L

tpd = 1.3 ns
tpd+* = 1.85 ns
tpd−* = 2.05 ns
PD = 15.5 mW

M80 — 4 TO 1 MUX W/E

LOGIC EQUIVALENT





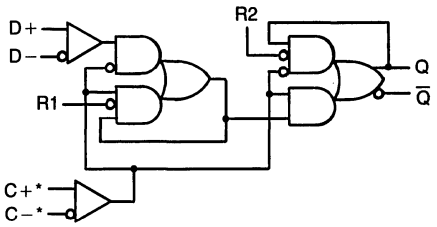
TRUTH TABLE

E	S1	SØ	Y
H	X	X	L
L	L	L	$\overline{AØ}$
L	L	H	$\overline{A1}$
L	H	L	$\overline{A2}$
L	H	H	$\overline{A3}$

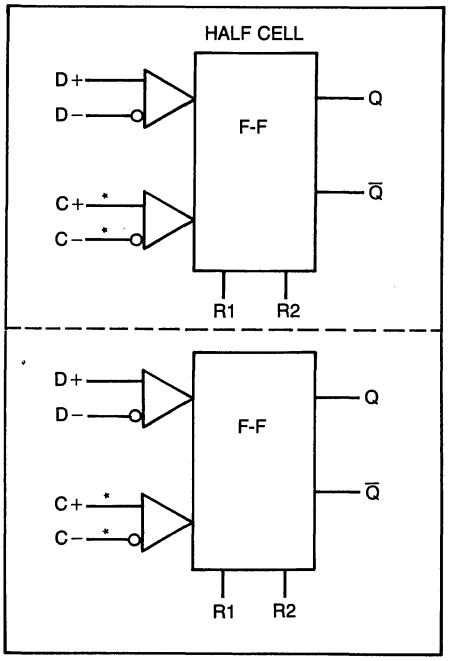
tpd = 1.5 ns
tpd*(E) = 1.75 ns
tpd*(SØ) = 2.1 ns
PD = 28.5 mW

H81 — DUAL D F/F WITH DIFF, CLOCK AND DATA

LOGIC EQUIVALENT



tpw (C) = 2.0 ns min tpd* = 1.5 ns
tSETUP(D) = 1.5 ns tHOLD(D) = 0 ns
PD = 52 mW (for 2−H81's)
tpd (R1 → Q, $\overline{Q}$) = 3.5 ns tpd (R2 → Q, $\overline{Q}$) = 2.0 ns
D = "H" means D+ = H and D− = L
D = "L" means D+ = L and D− = H
C = "H" means C+ = H and C− = L
C = "L" means C+ = L and C− = H
tpw+ (R1 or R2) = 2.5 ns min



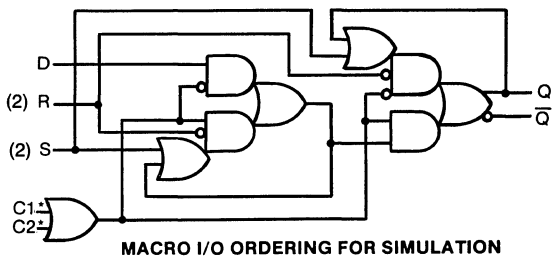
TRUTH TABLE

R1	R2	D	C	Q^{n+1}
L	L	X	H	—
L	L	X	L	—
L	L	L	L→H	L
L	L	H	L→H	H
H	X	X	H	L
H	L	X	L	—
X	H	X	L	L
L	H	X	H	—
H	H	H	L→H	⎍
X	X	L	L→H	L
H	L	H	L→H	⎍
L	H	H	L→H	⎍

— = NO CHANGE
X = DON'T CARE
L = LOW
H = HIGH
L→H = LOW TO HIGH TRANSITION

H82 — DUAL D F/F WITH ASYNCHRONOUS SET AND RESET

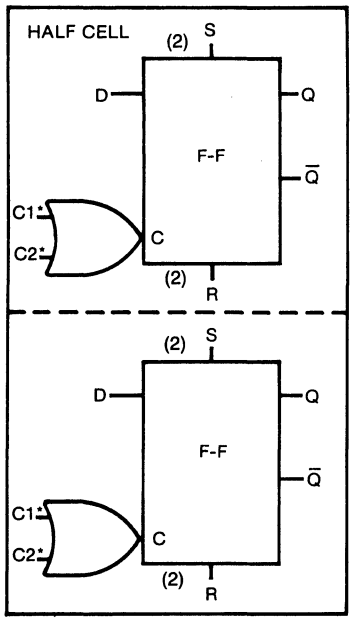
LOGIC EQUIVALENT



MACRO I/O ORDERING FOR SIMULATION

H82
QB Q
C1 C2 D R S

tpd* = 1.7 ns
tpd (R, S → Q, $\overline{Q}$) = 3.7 ns, 2.2 ns for C = "L"
tSETUP(D) = 1.5 ns
tHOLD(D) = 0 ns
PD = 46.8 mW
tpw (C1, C2) = 2.0 ns min
tpw (R, S) = 2.5 ns min
tpw + (R/S and C1/C2 tied together) = 4 ns min
NOTE: Outputs can be selected for 0.5 or 1.0 mA only; however, $\overline{Q}$ can be selected for 2.0 mA if Q is 0 mA.



TRUTH TABLE

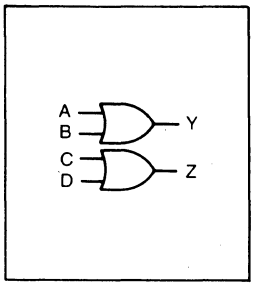
R	S	D	C	Q^{n+1}
L	L	X	H	—
L	L	X	L	—
L	L	L	L→H	L
L	L	H	L→H	H
H	L	X	X	L
L	H	X	X	H
H	H	X	X	N.D.
H	L	H	L→H	⎍
H	L	L	L→H	L
L	H	L	L→H	⎍
L	H	H	L→H	H

— = NO CHANGE
X = DON'T CARE
L = LOW
H = HIGH
L→H = LOW TO HIGH TRANSITION
N.D. = NOT DEFINED (INDETERMINATE)
C = C1 + C2

Interface Cells

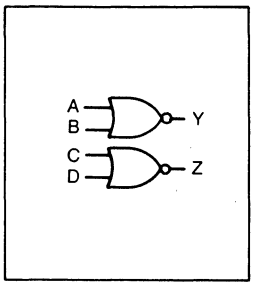
NOTES: Values given for prop. delay tpd, are max. for 1 mA or 1.5 mA output follower current driving a fan-out of 1. Values given for power dissipation, PD, are typical for unloaded outputs. Output follower current can be selected for 0, 0.5, 1 or 1.5 mA (except the Q output of I13 and I14 where 0, 0.8, 1, or 1.8 mA can be selected). All inputs including *Inputs can be connected to input package pins.

IØ1, TØ1



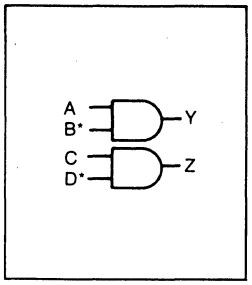
$Y = A + B$
$Z = C + D$
tpd = 1.05ns
PD = 10.4mW

IØ2, TØ2



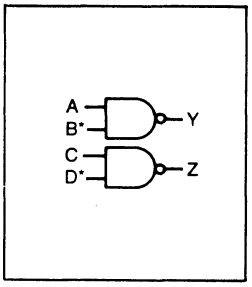
$Y = \overline{A} \bullet \overline{B}$
$Z = \overline{C} \bullet \overline{D}$
tpd = 1.05ns
PD = 10.4mW

IØ3, TØ3



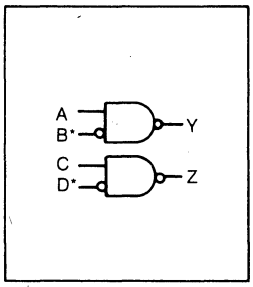
$Y = A \bullet B$
$Z = C \bullet D$
tpd = 1.2ns
tpd* = 1.4ns
PD = 18.2mW

IØ4, TØ4



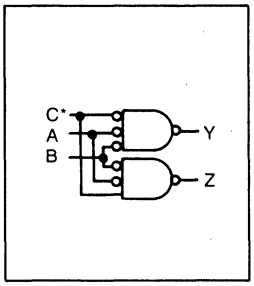
$Y = \overline{A} + \overline{B}$
$Z = \overline{C} + \overline{D}$
tpd = 1.2ns
tpd* = 1.4ns
PD = 18.2mW

IØ5, TØ5



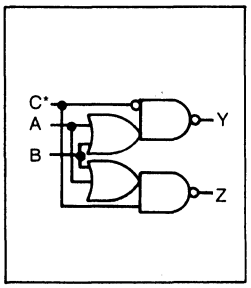
$Y = \overline{A} + B$
$Z = \overline{C} + D$
tpd = 1.2ns
tpd* = 1.4ns
PD = 18.2mW

IØ6, TØ6



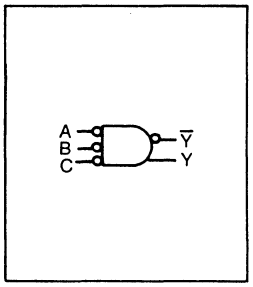
$Y = A + B + C$
$Z = A + B + \overline{C}$
tpd = .95ns
tpd*(Z) = 1.4ns
tpd+*(Y) = 1.25ns
tpd−*(Y) = 1.55ns
PD = 10.4mW

IØ7, TØ7



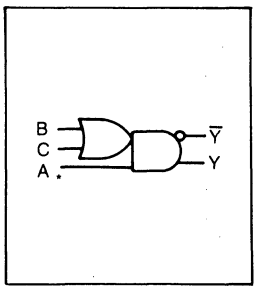
$Y = \overline{A} \bullet \overline{B} + C$
$Z = \overline{A} \bullet \overline{B} + \overline{C}$
tpd = .95ns
tpd*(Z) = 1.4ns
tpd+*(Y) = 1.25ns
tpd−*(Y) = 1.55ns
PD = 10.4mW

IØ8, TØ8



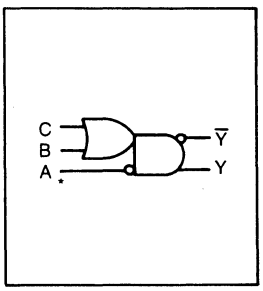
$Y = \overline{A} \bullet \overline{B} \bullet \overline{C}$
tpd = 1.05ns
PD = 5.2mW

IØ9, TØ9



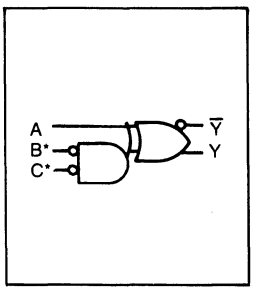
$Y = A \bullet B + A \bullet C$
tpd = 1.1ns
tpd*(Y) = 1.2ns
tpd*($\overline{Y}$) = 1.4ns
PD = 10.4mW

I10, T10



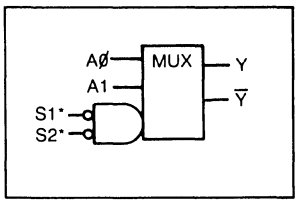
$Y = \overline{A} \bullet B + \overline{A} \bullet C$
tpd = 1.1ns
tpd*(Y) = 1.2ns
tpd*($\overline{Y}$) = 1.4ns
PD = 10.4mW

I11, T11

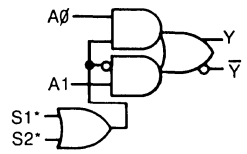


$Y = A \oplus (\overline{B} \bullet \overline{C})$
tpd = 1.05ns
tpd* = 1.4ns
PD = 10.4mW

I12, T12 — 2 TO 1 MUX



LOGIC EQUIVALENT

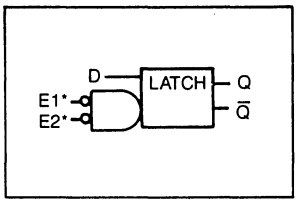


TRUTH TABLE

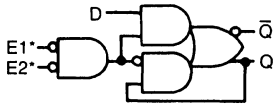
S2	S1	Y
L	L	A1
L	H	AØ
H	L	AØ
H	H	AØ

tpd = 1.05ns
tpd* = 1.4ns
PD = 10.4mW

I13, T13 — LATCH



LOGIC EQUIVALENT

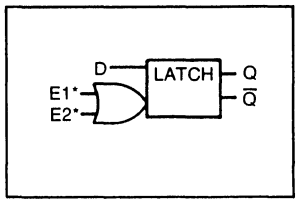


TRUTH TABLE

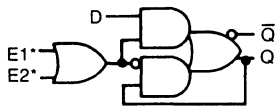
E1	E2	Q
L	L	D
X	H	—
H	X	—

— = NO CHANGE
tpd = 1.2 ns
tpd−* = 1.5 ns
tpd+* = 1.7 ns
tSETUP = 1.5 ns
tHOLD = 0 ns
PD = 15.6 mW
t_{pw} = 2.0 ns min

I14, T14 — LATCH



LOGIC EQUIVALENT



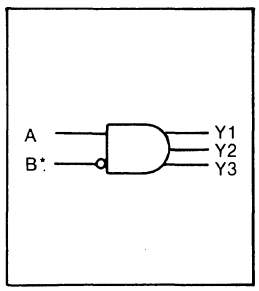
TRUTH TABLE

E1	E2	Q
L	L	—
X	H	D
H	X	D

— = NO CHANGE
tpd = 1.2 ns
tpd−* = 1.5 ns
tpd+* = 1.7 ns
tSETUP = 1.5 ns
tHOLD = 0 ns
PD = 15.6 mW
t_{pw} = 2.0 ns min

I15 — AND GATE

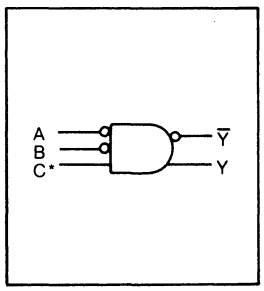
(LOCATIONS 10, 20, 30, 40, 50, 60, 70, AND 80 ONLY)



$Y1 = Y2 = Y3 = A \bullet \overline{B}$
tpd = 1.3ns
tpd* = 1.5ns
PD = 10.4mW
Y2 OUTPUT CAN BE SELECTED FOR 0mA ONLY.

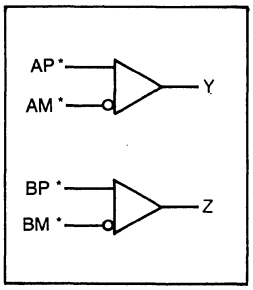
I16 — AND GATE

(LOCATIONS 10, 20, 30, 40, 50, 60, 70, AND 80 ONLY)



$Y = \overline{A} \bullet \overline{B} \bullet C$
tpd = 1.05ns
tpd* = 1.5ns
PD = 10.4mW

I20, T20 — DUAL DIFFERENTIAL LINE RECEIVER



TRUTH TABLES

AP	AM	Y
L	L	X
L	H	L
H	L	H
H	H	X

BP	BM	Z
L	L	X
L	H	L
H	L	H
H	H	X

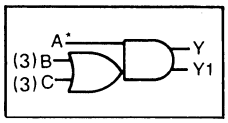
X = UNDEFINED
tpd* = 1.4 ns WITH 800 mV SWING ON 1 INPUT
PD = 26 mW

NOTES:
1. Choice of ouput follower current is 1 ma only.
2. Input voltage range is Ø to − 2 volts on the most positive input. The voltage range on the most negative input is O to V_{EE}.
3. Differential input voltage ≥ 200 mV.

Output Cells

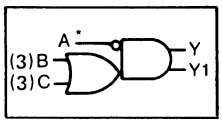
NOTES: Values given for power dissipation, PD, are typical with unloaded outputs. Propagation delay for the Y output is specified when driving 50 Ω (25 Ω for macro O24 or O25) to −2 volts. The Y1 output can only drive internal loads selected with an output follower current of 0, 1, or 2 mA. Number in ( ) indicate fan-in other than 1. All inputs including *Inputs can be connected to input package pins. The Y output in the cell is a collector output that connects to an output emitter follower near the bonding pad. The output rise and fall times are specified at 1 ns minimum and 4 ns maximum (20 to 80%) for all output cell macros when driving 50 ohms (25 ohms for 024 and 025) to −2 volts.

O01, G01



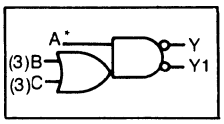
$Y = Y1 = A \cdot B + A \cdot C$
tpd+(Y, Y1) = 3.1 ns
tpd+*(Y, Y1) = 3.6 ns
tpd−(Y, Y1) = 2.75 ns
tpd−*(Y, Y1) = 3.4 ns
FOR Y NOT USED
tpd (Y1) = 1.9 ns
tpd*(Y1) = 2.4 ns
PD = 28.6 mW

O02, G02



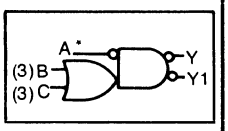
$Y = Y1 = \overline{A} \cdot B + \overline{A} \cdot C$
tpd+(Y, Y1) = 3.1 ns
tpd+*(Y, Y1) = 3.6 ns
tpd−(Y, Y1) = 2.75 ns
tpd−*(Y, Y1) = 3.4 ns
FOR Y NOT USED
tpd (Y1) = 1.9 ns
tpd*(Y1) = 2.4 ns
PD = 28.6 mW

O03, G03



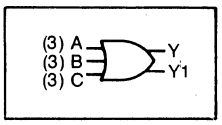
$Y = Y1 = \overline{A} + \overline{B} + A \cdot \overline{C}$
tpd+(Y, Y1) = 3.1 ns
tpd+*(Y, Y1) = 3.6 ns
tpd−(Y, Y1) = 2.75 ns
tpd−*(Y, Y1) = 3.4 ns
FOR Y NOT USED
tpd (Y1) = 1.9 ns
tpd*(Y1) = 2.4 ns
PD = 28.6 mW

O04, G04



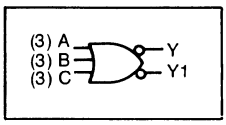
$Y = Y1 = A + \overline{B} \cdot \overline{C}$
tpd+(Y, Y1) = 3.1 ns
tpd+*(Y, Y1) = 3.6 ns
tpd − (Y, Y1) = 2.75 ns
tpd−*(Y, Y1) = 3.4 ns
FOR Y NOT USED
tpd (Y1) = 1.9 ns
tpd*(Y1) = 2.4 ns
PD = 28.6 mW

O05, G05



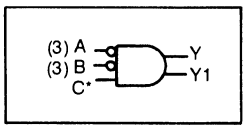
$Y = Y1 = A + B + C$
tpd+(Y, Y1) = 3.1 ns
tpd−(Y, Y1) = 2.8 ns
FOR Y NOT USED
tpd (Y1) = 1.7 ns
PD = 18.2 mW

O06, G06



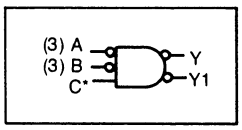
$Y = Y1 = \overline{A} \cdot \overline{B} \cdot \overline{C}$
tpd+(Y, Y1) = 3.1 ns
tpd−(Y, Y1) = 2.8 ns
FOR Y NOT USED
tpd (Y1) = 1.7 ns
PD = 18.2 mW

O07, G07



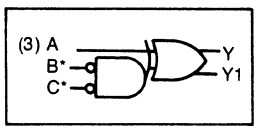
$Y = Y1 = \overline{A} \cdot \overline{B} \cdot C$
tpd (Y, Y1) = 3ns
tpd*(Y, Y1) = 3.6ns
FOR Y NOT USED
tpd (Y1) = 1.6ns
tpd*(Y1) = 2.2ns
PD = 28.6mW

O08, G08



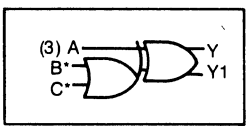
$Y = Y1 = A + B + \overline{C}$
tpd (Y, Y1) = 3ns
tpd*(Y, Y1) = 3.6ns
FOR Y NOT USED
tpd (Y1) = 1.6ns
tpd*(Y1) = 2.2ns
PD = 28.6mW

O09, G09



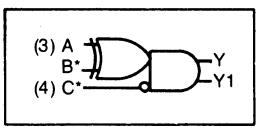
$Y = Y1 = A \oplus (\overline{B} \cdot \overline{C})$
tpd (Y, Y1) = 3ns
tpd*(Y, Y1) = 3.6ns
FOR Y NOT USED
tpd (Y1) = 1.6ns
tpd*(Y1) = 2.2ns
PD = 28.6mW

O10, G10



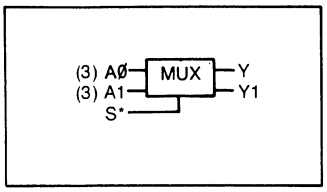
$Y = Y1 = A \oplus (B + C)$
tpd (Y, Y1) = 3ns
tpd*(Y, Y1) = 3.6ns
FOR Y NOT USED
tpd (Y1) = 1.6ns
tpd*(Y1) = 2.2ns
PD = 28.6mW

O11, G11

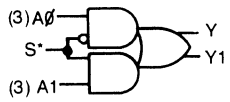


$Y = Y1 = (A \oplus B) \cdot \overline{C}$
tpd (Y, Y1) = 3.1ns
tpd*(Y, Y1) = 3.7ns
FOR Y NOT USED
tpd (Y1) = 1.7ns
tpd*(Y1) = 2.3ns
PD = 28.6mW

O12, G12 — 2 TO 1 MUX



LOGIC EQUIVALENT

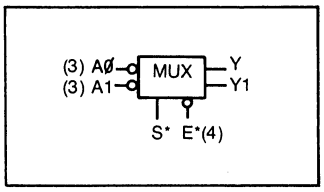


TRUTH TABLE

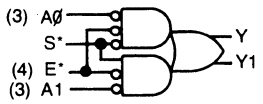
S	Y
L	AØ
H	A1

Y = Y1
tpd (Y, Y1) = 3.0ns
tpd*(Y, Y1) = 3.6ns
FOR Y NOT USED
tpd (Y1) = 1.6ns
tpd*(Y1) = 2.2ns
PD = 28.6mW

O13, G13 — 2 TO 1 MUX W/E



LOGIC EQUIVALENT

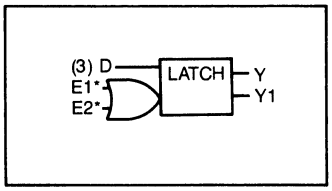


TRUTH TABLE

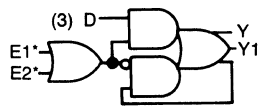
E	S	Y
H	X	L
L	L	$\overline{AØ}$
L	H	$\overline{A1}$

Y = Y1
tpd (Y, Y1) = 3.1ns
tpd*(Y, Y1) = 3.7ns
FOR Y NOT USED
tpd (Y1) = 1.7ns
tpd*(Y1) = 2.3ns
PD = 28.6mW

O14, G14 — LATCH



LOGIC EQUIVALENT

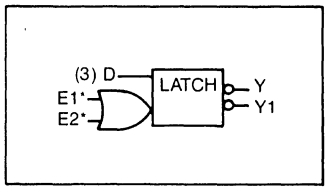


TRUTH TABLE

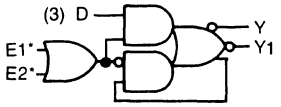
E1	E2	Y
L	L	—
X	H	D
H	X	D

— = NO CHANGE
Y = Y1
tpd (Y, Y1) = 3.3 ns
tpd* (Y, Y1) = 3.8 ns
FOR Y NOT USED
tpd (Y1) = 1.8 ns
tpd* (Y1) = 2.4 ns
tpw = 2.5 ns min
tpw = 2.5 ns min
tSETUP(D) = 2.0 ns
tHOLD(D) = 0 ns
PD = 33.8 mW

O15, G15 — LATCH



LOGIC EQUIVALENT

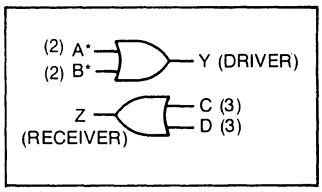


TRUTH TABLE

E1	E2	Y
L	L	—
X	H	$\overline{D}$
H	X	$\overline{D}$

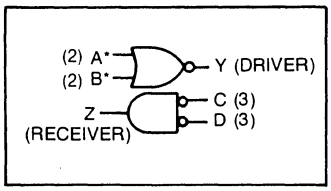
— = NO CHANGE
Y = Y1
tpd (Y, Y1) = 3.3 ns
tpd* (Y, Y1) = 3.8 ns
FOR Y NOT USED
tpd (Y1) = 1.8 ns
tpd* (Y1) = 2.4 ns
tpw = 2.5 ns min
tSETUP(D) = 2.0 ns
tHOLD(D) = 0 ns
PD = 33.8 mW

O16, G16 — TRANSCEIVER



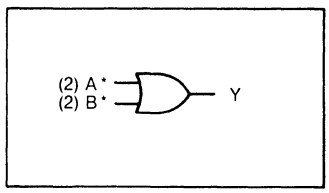
Y = A + B
Z = C + D
tpd Z = 1.7 ns
tpd+(Y) = 3.5 ns
tpd−(Y) = 2.3 ns
PD = 61.4 mW
Z WILL DRIVE ONLY INTERNAL LOADS
V_{OL} MAX = −1.95 V AT Y OUTPUT

O17, G17 — TRANSCEIVER



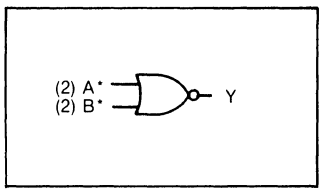
$Y = \overline{A} \cdot \overline{B}$
$Z = \overline{C} \cdot \overline{D}$
tpd Z = 1.7 ns
tpd+(Y) = 3.5 ns
tpd−(Y) = 2.3 ns
PD = 61.4 mW
Z WILL DRIVE ONLY INTERNAL LOADS
V_{OL} MAX = −1.95 V AT Y OUTPUT

O18, G18 — DRIVER (OR)



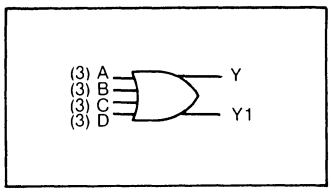
Y = A+B
tpd+ = 3.5 ns
tpd− = 2.3 ns
PD = 43.2 mW
V_{OL} MAX = −1.95 V

O19, G19 — DRIVER (NOR)



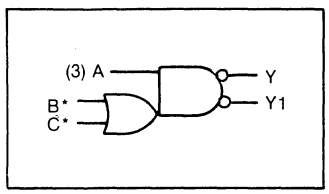
$Y = \overline{A} \cdot \overline{B}$
tpd+ = 3.5 ns
tpd− = 2.3 ns
PD = 43.2 mW
V_{OL} MAX = −1.95 V

O20, G20 — 4 INPUT OR GATE



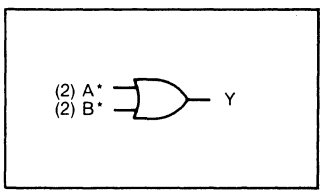
Y = Y1 = A+B+C+D
tpd+(Y, Y1) = 3.2 ns
tpd−(Y, Y1) = 2.9 ns
FOR Y NOT USED
tpd (Y1) = 1.8 ns
PD = 18.2 mW

O21, G21 — OR/AND GATE



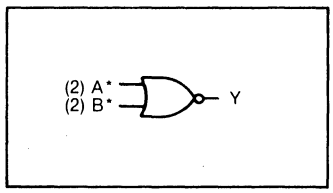
$Y = Y1 = \overline{A \cdot B + A \cdot C}$
tpd +(Y, Y1) = 3.1 ns
tpd+*(Y, Y1) = 3.6 ns
tpd−(Y, Y1) = 2.75 ns
tpd−*(Y, Y1) = 3.4 ns
FOR Y NOT USED
tpd (Y1) = 1.9 ns
tpd*(Y1) = 2.4 ns
PD = 28.6 mW

O24, G24 — 25 Ω OR DRIVER



Y = A+B
Y WILL DRIVE 25 OHMS TO −2 VOLTS
tpd+ = 3.8 ns
tpd− = 3.0 ns
PD = 61.4 mW
V_{OL} MAX = −1.95 V

O25, G25 — 25 Ω NOR DRIVER



$Y = \overline{A} \cdot \overline{B}$
Y WILL DRIVE 25 OHMS TO −2 VOLTS
tpd+ = 3.8 ns
tpd− = 3.0 ns
PD = 61.4 mW
V_{OL} MAX = −1.95 V

MECL Related Literature — For Copies of MECL Literature, Contact a Motorola Sales Office or Authorized Distributor.

Application Notes

AN-417B IC Crystal Controlled Oscillators
Crystal controlled squarewave oscillators can be used as clock drivers, harmonic sources for frequency markers, in frequency synthesizers, frequency comparators, etc. It is difficult to obtain high frequency squarewaves due to the long propagation delays of the most integrated circuits. The MECL 10,000 circuits with 2ns propagation delays eliminate this problem. This note describes squarewave oscillator circuits with crystal control that are capable of output frequencies, inverted and noninverted, up to 200 MHz.

AN-556 Interconnection Techniques for Motorola's MECL 10,000 Series Emitter Coupled Logic
This application note describes some of the characteristics of high-speed digital signal lines and gives wiring rules for MECL 10,000 emitter coupled logic. The note includes discussions of printed circuit board interconnects, board-to-board interconnects, and wirewrapping techniques.

AN-567 MECL Positive and Negative Logic
Eight positive or negative logic assignments may prove convenient to the MECL system designer. This note describes the equivalences between the two approaches and provides guides for converting between them.

AN-579 Testing MECL 10,000 Integrated Logic Circuits
Circuit testing techniques become increasingly important as circuit speeds approach and exceed the 2ns range. With MECL 10,000 and MECL III circuits, it is possible to exploit their 50-ohm output drive capability to obtain highly accurate test data. This application note describes techniques for testing MECL 10,000 circuits for laboratory evaluation, and discusses key parameters which should be measured during incoming inspection rapid testing.

AN-592 AC Noise Immunity of MECL 10,000 Integrated Circuits
This application note discusses AC noise immunity as it relates to MECL systems. Test circuits for measuring AC noise immunity are shown, and results to be expected for typical MECL 10,000 circuits are presented.

AN-700 Simulate MECL System Interconnections With A Computer Program
Circuit interconnections are an important part of system design when using high-speed logic circuits. The design of interconnecting paths affects both system speed and system accuracy. This application note describes the use of a computer program to simulate interconnections for high-speed digital systems.

AN-701 Understanding MECL 10,000 DC and AC Data Sheet Specifications
The DC and AC specifications for emitter-coupled logic are somewhat different than those for saturated logic. This application note describes the specifications found on a MECL 10,000 data sheet and provides information for understanding these specifications for persons unfamiliar with emitter-coupled logic.

AN-720 Interfacing with MECL 10,000
This article describes some of the MECL circuits used to interface with signals not meeting MECL input or output requirements. The characteristics of these circuits, such as: input impedance, output drive, gain, and bandwidth allow the system designer to use these parts to optimize his system. MECL interface circuits overcome a problem area of many system designs, which is the efficient coupling on noncompatible signals.

AN-726 Bussing with MECL 10,000 Integrated Circuits
High-speed data bus lines are an important part of modern computer systems. Features of the MECL 10,000 family allow construction of data busses in a transmission line environment. This application note describes some of the guidelines to consider when designing high-speed bus lines and shows how the MC10123 can be used for maximum bus performance.

AN-730 A High Speed FIFO Memory Using the MECL MC10143 Register File
First in/first out memories are commonly used to store information in digital processing systems. However, these memories can also be designed to interface subsystems operating asynchronously or at different data rates. This application note describes a high-speed first in/first out memory design based on the MECL MC10143 8 x 2 Multiport Register File.

AN-774 A Simple High-Speed Bipolar Microprocessor

AN-776 The M10800 MECL LSI Processor Family

AN-792 M10800 MECL LSI Circuits are Designed for High-Performance Microprogrammed Processors.

AN-874 Macrocell Arrays: Concept — Features — Cad Interface
High technology array-based products offer the advantages of custom LSI circuits, yet overcome the problems of high costs and long design cycles. Recent developments in Array technology make use of Macrocell building blocks rather than primitive gates for easier design and higher performance. Additional developments in computer-aided-design customer interface systems simplify the job of developing Array circuit options. This note examines Motorola's Macrocell Array concept with special emphasis on the CAD user interface.

AR108 Macrocell Arrays — An Alternative To Custom LSI

AR-110 Remote CAD System Helps Designeers Develop CUstom VLSI Chips

The MECL System Design Handbook, Revised Edition

This handbook contains over 200 illustrations providing circuit and waveform diagrams, as well as numerical data. An appendix lists examples of hardware available for use with MECL systems.

This fourth edition is the compilation of a decade of knowledge gained through designing high-speed circuitry and assisting designers with its application. Wiring rules and system techniques are covered for MECL III, and the popular, low-power, high-speed MECL 10,000 and 10KH families.

Comprised of eight chapters, the handbook has 253 pages.

HB205R1

NEW MECL Device Data Book — MECL High-Speed Integrated Circuits

This Data Book provides family and systems characteristics for the MECL family of digital integrated circuits, as well as comprehensive specifications for the MECL 10,000, 10KH, and MECL III Series devices. Overviews of the phase-locked loop functions , MECL memories, and arrays are included in this 458 page book.

DL122R1

MECL M10800 and M10900 FAMILY DATA SHEETS ARE AVAILABLE
MECL Reliability Reports — Available Upon Special Request.

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