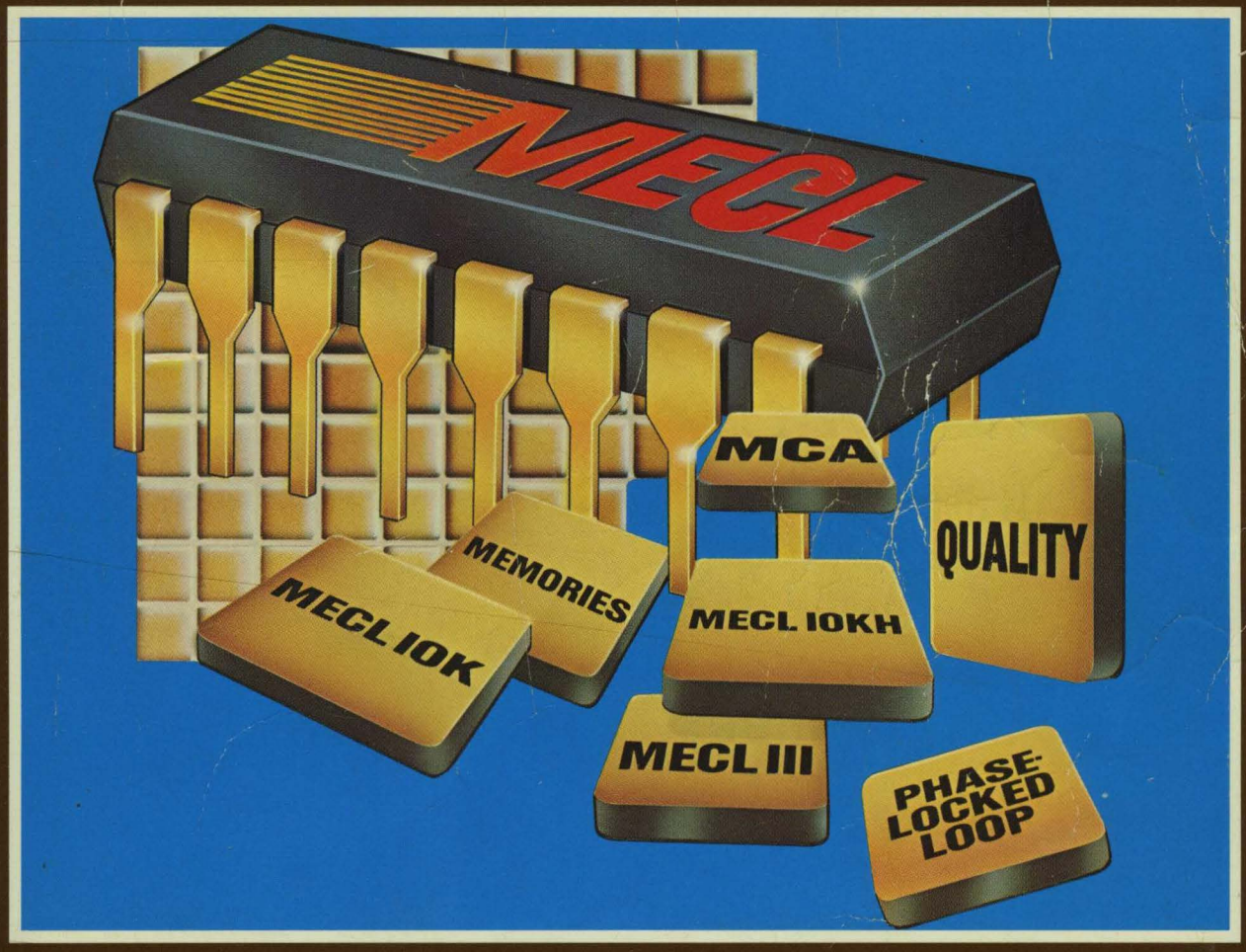
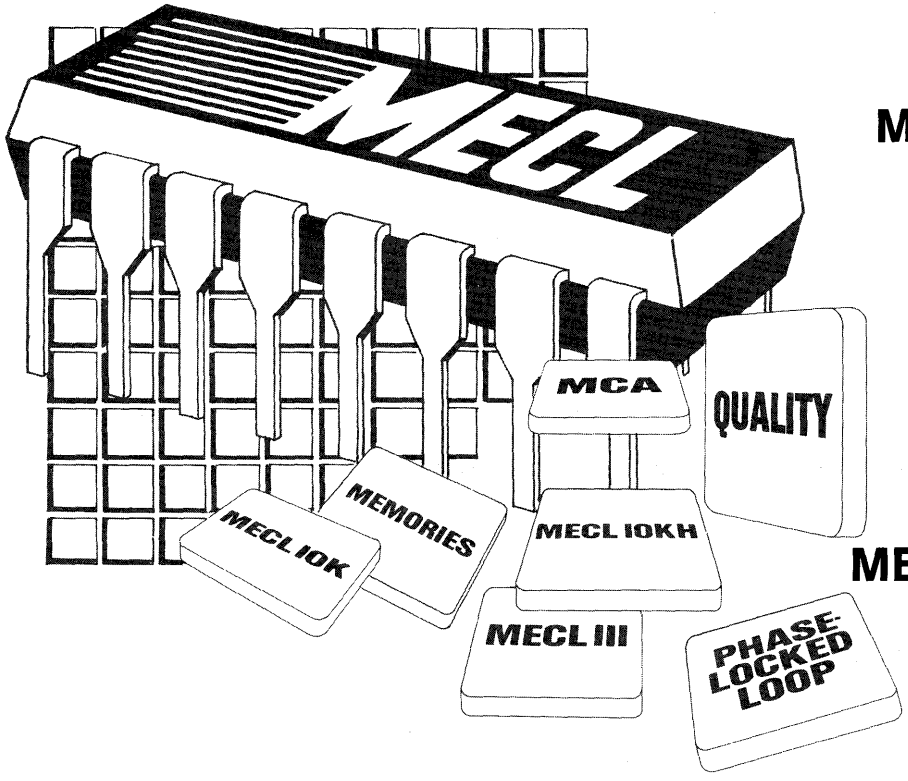
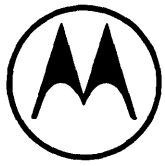
DL122R1

MOTOROLA INC.



MECL DEVICE DATA





MOTOROLA

MECL INTEGRATED CIRCUITS

Prepared by
Technical Information Center

This book presents technical data for a broad line of MECL integrated circuits. Complete specifications for the individual circuits are provided in the form of data sheets. In addition, selector guides are included to simplify the task of choosing the best combination of circuits for optimum system architecture.

The information in this book has been carefully checked and is believed to be reliable; however, no responsibility is assumed for inaccuracies. Furthermore, this information does not convey to the purchaser of microelectronic devices any license under the patent right of any manufacturer.

Series D

Printed in U.S.A.

CONTENTS

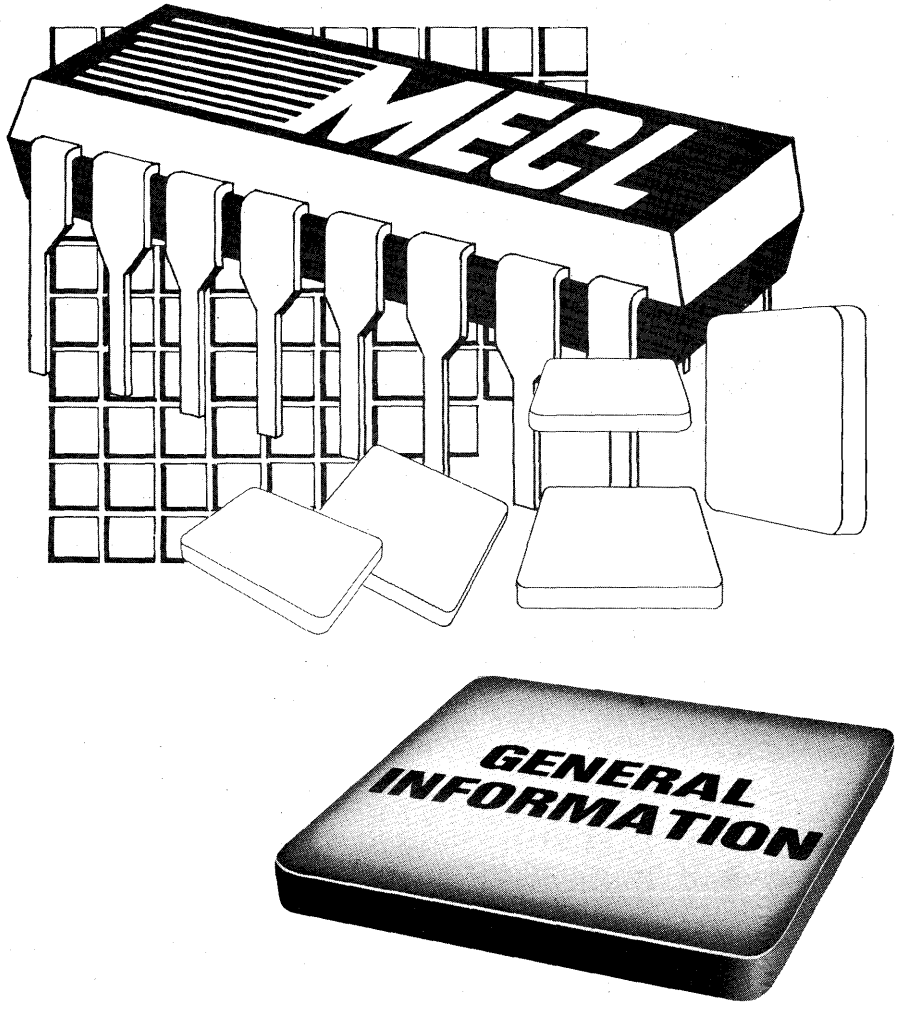
DEVICE INDEX

DEVICE INDEX (continued)

DEVICE INDEX (continued)

DEVICE INDEX (continued)

DEVICE INDEX (continued)


MECL
GENERAL
INFORMATION

GENERAL INFORMATION
SECTION 1 — HIGH-SPEED LOGICS

High speed logic is used whenever improved system performance would increase a product's market value. For a given system design, high-speed logic is the most direct way to improve system performance and emitter-coupled logic (ECL) is today's fastest form of digital logic. Emitter-coupled logic offers both the logic speed and logic features to meet the market demands for higher performance systems.

MECL PRODUCTS

Motorola introduced the original monolithic emitter-coupled logic family with MECL I (1962) and followed this with MECL II (1966). These two families are now obsolete and have given way to the MECL III (MC1600 series), MECL 10K, PLL (MC12000 series) and the new MECL 10KH families.

Chronologically the third family introduced, MECL III (1968) is a higher power, higher speed logic. Typical 1 ns edge speeds and propagation delays along with greater than 500 MHz flip-flop toggle rates, make MECL III useful for high-speed test and communications equipment. Also, this family is used in the high-speed sections and critical timing delays of larger systems. For more general purpose applications, however, trends in large high-speed systems showed the need for an easy-to-use logic family with propagation delays on the order of 2 ns. To match this requirement, the MECL 10,000 Series was introduced in 1971.

An important feature of MECL 10K is its compatibility with MECL III to facilitate using both families in the same system. A second important feature is its significant power economy — MECL 10K gates use less than one-half the power of MECL III. Finally, low gate power and advanced circuit design techniques have permitted a new level of complexity for MECL 10K circuits. For example, the complexity of the MC10901 8X8-Bit Multiplier Function compares favorably to that of any bipolar integrated circuit on the market.

Motorola introduced the MECL 10KH product family in 1981. This latest MECL family features 100% improvements in propagation delay and clock speeds while maintaining power supply currents equal to MECL 10K. MECL 10KH is voltage compensated allowing guaranteed dc and switching parameters over a ±5% power supply range. Noise margins have been improved by 75% over the MECL 10K series.

Compatibility with MECL 10K and MECL III is a key element in allowing users to enhance existing systems by increasing the speed in critical timing areas. Also, many MECL 10KH devices are pin out/functional duplications of the MECL 10K series devices. The emphasis of this new family will be placed on more powerful logic functions having more complexity and greater performance. With 1.0 ns propagation delays and 25 mW per gate, MECL 10KH features the best speed-power product of any ECL logic family available today.

MECL FAMILY COMPARISONS

Feature	MECL 10KH	MECL 10K		MECL III
		10,100 Series 10,500 Series	10,200 Series 10,600 Series	
1. Gate Propagation Delay	1.0 ns	2 ns	1.5 ns	1 ns
2. Output Edge Speed	1.5 ns	3.5 ns	2.5 ns	1 ns
3. Flip-Flop Toggle Speed	250 MHz min	125 MHz min	200 MHz min	300–500 MHz min
4. Gate Power	25 mW	25 mW	25 mW	60 mW
5. Speed Power Product	25 pJ	50 pJ	37 pJ	60 pJ

FIGURE 1a — GENERAL CHARACTERISTICS

Ambient Temperature Range	MECL 10KH	MECL 10K	MECL III	PLL
0° to 75°C	MC10H100 Series		MC1697P	MC12000 Series
−30°C to +85°C		MC10100 Series MC10200 Series	MC1600 Series	MC12000 Series
−55°C to 125°C	—	MC10500 Series MC10600 Series MCM10500 Series	MC1648M	MC12500 Series

FIGURE 1b — OPERATING TEMPERATURE RANGE

MECL IN PERSPECTIVE

In evaluating any logic line, speed and power requirements are the obvious primary considerations. Figure 1 provides the basic parameters of the MECL 10KH, MECL 10K, and MECL III families. But these provide only the start of any comparative analysis, as there are a number of other important features that make MECL highly desirable for system implementation. Among these:

Complementary Outputs cause a function and its complement to appear simultaneously at the device outputs, without the use of external inverters. It reduces package count by eliminating the need for associated invert functions and, at the same time, cuts system power requirements and reduces timing differential problems arising from the time delays introduced by inverters.

High Input Impedance and Low Output Impedance permit large fan out and versatile drive characteristics.

Insignificant Power Supply Noise Generation, due to differential amplifier design which eliminates current spikes even during signal transition period.

Nearly Constant Power Supply Current Drain simplifies power-supply design and reduces costs.

Low Cross-Talk due to low-current switching in signal path and small (typically 850 mV) voltage swing, and to relatively long rise and fall times.

Wide Variety of Functions, including complex functions facilitated by low power dissipation (particularly in MECL 10KH and MECL 10K series). A basic MECL 10K gate consumes less than 8 mW in on-chip power in some complex functions.

Wide Performance Flexibility due to differential amplifier design which permits MECL circuits to be used as linear as well as digital circuits.

Transmission Line Drive Capability is afforded by the open emitter outputs of MECL devices. No "Line Drivers" are listed in MECL families, because *every* device is a line driver.

Wire-ORing reduces the number of logic devices required in a design by producing additional OR gate functions with only an interconnection.

Twisted Pair Drive Capability permits MECL circuits to drive twisted-pair transmission lines as long as 1000 feet.

Wire-Wrap Capability is possible with MECL 10KH and the MECL 10K family because of the slow rise and fall time characteristic of the circuits.

Open Emitter-Follower Outputs are used for MECL outputs to simplify signal line drive. The outputs match any line impedance and the absence of internal pulldown resistors saves power.

Input Pulldown Resistors of approximately 50 kΩ permit unused inputs to remain unconnected for easier circuit board layout.

MECL APPLICATIONS

Motorola's MECL product lines are designed for a wide range of systems needs. Within the computer market, MECL 10K is used in systems ranging from special purpose peripheral controllers to large mainframe computers. Big growth areas in this market include disk and communication channel controllers for larger systems and high performance minicomputers.

The industrial market primarily uses MECL for high performance test systems such as IC or PC board testers. However, the high bandwidths of MECL 10KH, MECL 10K, MECL III, and MC12,000 are required for many frequency synthesizer systems using high speed phase lock loop networks. MECL will continue to grow in the industrial market through complex medical electronic products and high performance process control systems.

MECL 10K and MECL III have been accepted within the Federal market for numerous signal processors and navigation systems. Full military temperature range MECL 10K is offered in the MC10500 and MC10600 Series, and in the PLL family as the MC12500 Series.

BASIC CONSIDERATIONS FOR HIGH-SPEED LOGIC DESIGN

High-speed operation involves only four considerations that differ significantly from operation at low and medium speeds:

1. Time delays through interconnect wiring, which may have been ignored in medium-speed systems, become highly important at state-of-the-art speeds.
2. The possibility of distorted waveforms due to reflections on signal lines increases with edge speed.
3. The possibility of "crosstalk" between adjacent signal leads is proportionately increased in high-speed systems.
4. Electrical noise generation and pick-up are more detrimental at higher speeds.

In general, these four characteristics are speed- and frequency-dependent, and are virtually independent of the type of logic employed. The merit of a particular logic family is measured by how well it compensates for these deleterious effects in system applications.

The interconnect-wiring time delays can be reduced only by reducing the length of the interconnecting lines. At logic speeds of two nanoseconds, an equivalent "gate delay" is introduced by every foot of interconnecting wiring. Obviously, for functions interconnected within a single monolithic chip, the time delays of signals travelling from one function to another are insignificant. But for a great many externally interconnected parts, this can soon add up to an appreciable delay time. Hence, the greater the number of functions per chip, the higher the system speed. *MECL circuits, particularly those of the MECL 10K and MECL 10KH Series are designed with a propensity toward complex functions to enhance overall system speed.*

Waveform distortion due to line reflections also becomes troublesome principally at state-of-the-art speeds. At slow and medium speeds, reflections on interconnecting lines are not usually a serious problem. At higher speeds, however, line lengths can approach the wavelength of the signal and improperly terminated lines can result in reflections that will cause false triggering (see Figure 2). The solution, as in RF technology, is to employ "transmission-line" practices and properly terminate each signal line with its characteristic impedance at the end of its run. *The low-impedance, emitter-follower outputs of MECL circuits facilitate transmission-line practices without upsetting the voltage levels of the system.*

The increased affinity for crosstalk in high-speed circuits is the result of very steep leading and trailing edges (fast rise and fall times) of the high-speed signal. These steep wavefronts are rich in harmonics that couple readily to adjacent circuits. *In the design of MECL 10K and*

MECL 10KH, the rise and fall times have been deliberately slowed. This reduces the affinity for crosstalk without compromising other important performance parameters.

From the above, it is evident that the MECL logic line is not simply capable of operating at high speed, but has been specifically designed to reduce the problems that are normally associated with high-speed operation.

CIRCUIT DESCRIPTION

The typical MECL 10K circuit, Figure 3, consists of a differential-amplifier input circuit, a temperature and voltage compensated bias network, and emitter-follower outputs to restore dc levels and provide buffering for transmission line driving. High fan-out operation is possible be-

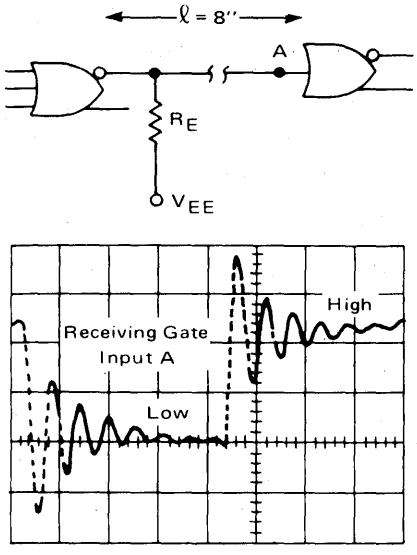


FIGURE 2a — UNTERMINATED TRANSMISSION LINE (No Ground Plane Used)

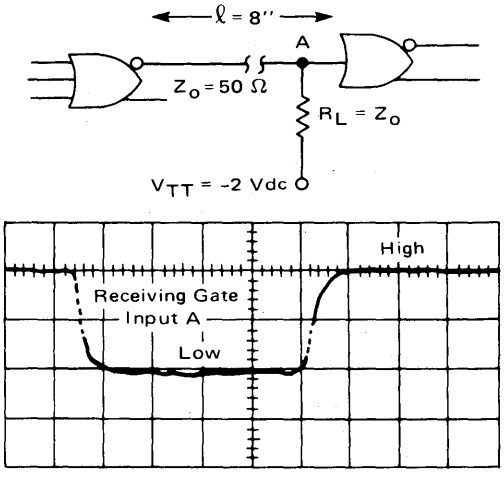


FIGURE 2b — PROPERLY TERMINATED TRANSMISSION LINE (Ground Plane Added)

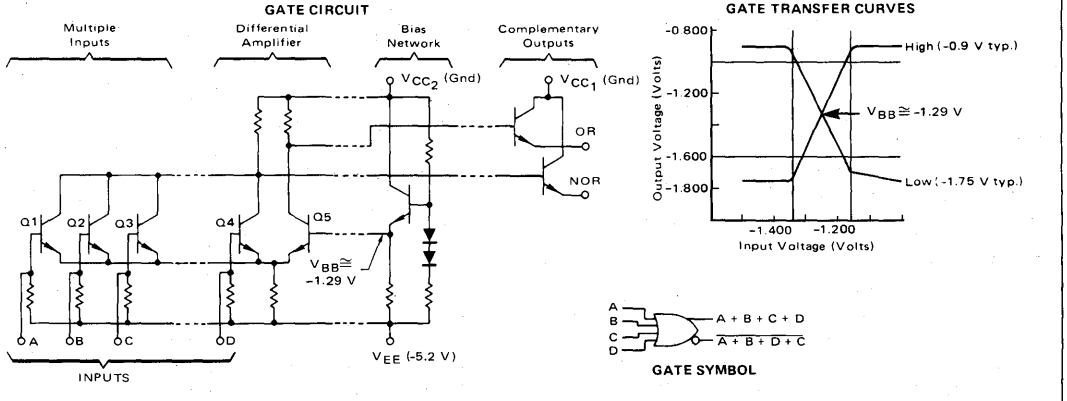


FIGURE 3 — MECL 10K GATE STRUCTURE AND SWITCHING BEHAVIOR

cause of the high input impedance of the differential amplifier input and the low output impedance of the emitter follower outputs. Power-supply noise is virtually eliminated by the nearly constant current drain of the differential amplifier, even during the transition period. Basic gate design provides for simultaneous output of both the OR function and its complement, the NOR function. The design of the MECL 10KH gate is unchanged, with two exceptions. The bias network has been replaced with a voltage regulator, and the differential amplifier source resistor has been replaced with a constant current source. (See section 2 for additional MECL 10KH information.)

Power-Supply Connections — Any of the power supply levels, V_{TT}, V_{CC}, or V_{EE} may be used as ground; however, the use of the V_{CC} node as ground results in best noise immunity. In such a case: $V_{CC} = 0$, $V_{TT} = -2.0$ V, $V_{EE} = -5.2$ V.

System Logic Specifications — The output logic swing of 0.85 V, as shown by the typical transfer characteristics curve, varies from a LOW state of $V_{OL} = -1.75$ V to a HIGH state of $V_{OH} = -0.9$ V with respect to ground.

Positive logic is used when reference is made to logical "0's" or "1's." Then

"0" = −1.75 V = LOW

typical

"1" = −0.9 V = HIGH

Circuit Operation — Beginning with all logic inputs LOW (nominal −1.75 V), assume that Q1 through Q4 are cut off because their P-N base-emitter junctions are not conducting, and the forward-biased Q5 is conducting. Under these conditions, with the base of Q5 held at −1.29 V by the V_{BB} network, its emitter will be one diode drop (0.8 V) more negative than its base, or −2.09 V. (The 0.8 V differential is a characteristic of this P-N junction.) The base-to-emitter differential across Q1 — Q4 is then the difference between the common emitter voltage (−2.09 V) and the LOW logic level (−1.75 V) or 0.34 V. This is less than the threshold voltage of Q1 through Q4 so that these transistors will remain cut off.

When any one (or all) of the logic inputs are shifted upward from the −1.75 V LOW state to the −0.9 V HIGH state, the base voltage of that transistor increases beyond the threshold point and the transistor turns on. When this happens, the voltage at the common-emitter point rises from −2.09 V to −1.7 (one diode drop below the −0.9 V base voltage of the input transistor), and since the base voltage of the fixed-bias transistor (Q5) is held at −1.29 V, the base-emitter voltage Q5 cannot sustain conduction. Hence, this transistor is cut off.

This action is reversible, so that when the input signal(s) return to the LOW state, Q1 – Q4 are again turned off and Q5 again becomes forward biased. The collector voltages resulting from the switching action of Q1 – Q4 and Q5 are transferred through the output emitter-follower to the output terminal. Note that the differential action of the switching transistors (one section being off when the other is on) furnishes simultaneous complementary signals at the output. This action also maintains constant power supply current drain.

DEFINITIONS OF LETTER SYMBOLS AND ABBREVIATIONS

Current:

I_{CC}	Total power supply current drawn from the positive supply by a MECL unit under test.
I_{CBO}	Leakage current from input transistor on MECL devices without pulldown resistors when test voltage is applied.
I_{CCH}	Current drain from V_{CC} power supply with all inputs at logic HIGH level.
I_{CCL}	Current drain from V_{CC} power supply with all inputs at logic LOW level.
I_E	Total power supply current drawn from a MECL test unit by the negative power supply.
I_F	Forward diode current drawn from an input of a saturated logic-to-MECL translator when that input is at ground potential.
I_{in}	Current into the input of the test unit when a maximum logic HIGH ($V_{IH\ max}$) is applied at that input.
I_{INH}	HIGH level input current into a node with a specified HIGH level ($V_{IH\ max}$) logic voltage applied to that node. (Same as I_{in} for positive logic.)
I_{INL}	LOW level input current, into a node with a specified LOW level ($V_{IL\ min}$) logic voltage applied to that node.
I_L	Load current that is drawn from a MECL circuit output when measuring the output HIGH level voltage.
I_{OH}	HIGH level output current: the current flowing into the output, at a specified HIGH level output voltage.
I_{OL}	LOW level output current: the current flowing into the output, at a specified LOW level output voltage.
I_{OS}	Output short circuit current.
I_{out}	Output current (from a device or circuit, under such conditions mentioned in context).
I_R	Reverse current drawn from a transistor input of a test unit when V_{EE} is applied at that input.
I_{SC}	Short-circuit current drawn from a translator saturating output when that output is at ground potential.

Voltage:

V_{BB}	Reference bias supply voltage.
V_{BE}	Base-to-emitter voltage drop of a transistor at specified collector and base currents.
V_{CB}	Collector-to-base voltage drop of a transistor at specified collector and base currents.
V_{CC}	General term for the most positive power supply voltage to a MECL device (usually ground, except for translator and interface circuits).
V_{CC1}	Most positive power supply voltage (output devices). (Usually ground for MECL devices.)

Voltage (cont.):

V_{CC2} Most positive power supply voltage (current switches and bias driver). (Usually ground for MECL devices.)

V_{EE} Most negative power supply voltage for a circuit (usually −5.2 V for MECL devices).

V_F Input voltage for measuring I_F on TTL interface circuits.

V_{IH} Input logic HIGH voltage level (nominal value).

$V_{IH\ max}$ Maximum HIGH level input voltage: The most positive (least negative) value of high-level input voltage, for which operation of the logic element within specification limits is guaranteed.

V_{IHA} Input logic HIGH threshold voltage level.

$V_{IHA\ min}$ Minimum input logic HIGH level (threshold) voltage for which performance is specified.

$V_{IH\ min}$ Minimum HIGH level input voltage: The least positive (most negative) value of HIGH level input voltage for which operation of the logic element within specification limits is guaranteed.

V_{IL} Input logic LOW voltage level (nominal value).

$V_{IL\ max}$ Maximum LOW level input voltage: The most positive (least negative) value of LOW level input voltage for which operation of the logic element within specification limits is guaranteed.

V_{ILA} Input logic LOW threshold voltage level.

$V_{ILA\ max}$ Maximum input logic LOW level (threshold) voltage for which performance is specified.

$V_{IL\ min}$ Minimum LOW level input voltage: The least positive (most negative) value of LOW level input voltage for which operation of the logic element within specification limits is guaranteed.

V_{in} Input voltage (to a circuit or device).

V_{max} Maximum (most positive) supply voltage, permitted under a specified set of conditions.

V_{OH} Output logic HIGH voltage level: The voltage level at an output terminal for a specified output current, with the specified conditions applied to establish a HIGH level at the output.

V_{OHA} Output logic HIGH threshold voltage level.

$V_{OHA\ min}$ Minimum output HIGH threshold voltage level for which performance is specified.

$V_{OH\ max}$ Maximum output HIGH or high-level voltage for given inputs.

$V_{OH\ min}$ Minimum output HIGH or high-level voltage for given inputs.

V_{OL} Output logic LOW voltage level: The voltage level at the output terminal for a specified output current, with the specified conditions applied to establish a LOW level at the output.

V_{OLA} Output logic LOW threshold voltage level.

$V_{OLA\ max}$ Maximum output LOW threshold voltage level for which performance is specified.

$V_{OL\ max}$ Maximum output LOW level voltage for given inputs.

$V_{OL\ min}$ Minimum output LOW level voltage for given inputs.

V_{TT} Line load-resistor terminating voltage for outputs from a MECL device.

V_{OLS1} Output logic LOW level on MECL 10,000 line receiver devices with all inputs at V_{EE} voltage level.

V_{OLS2} Output logic LOW level on MECL 10,000 line receiver devices with all inputs open.

Time Parameters:

$t+$ Waveform rise time (LOW to HIGH), 10% to 90%, or 20% to 80%, as specified.

$t-$ Waveform fall time (HIGH to LOW), 90% to 10%, or 80% to 20%, as specified.

t_r Same as $t+$

t_f Same as $t-$

$t+-$ Propagation Delay, see Figure 9.

$t-+$ Propagation Delay, see Figure 9.

t_{pd} Propagation delay, input to output from the 50% point of the input waveform at pin × (falling edge noted by — or rising edge noted by +) to the 50% point of the output waveform at pin y (falling edge noted by − or rising edge noted by +). (Cf Figure 9.)

$t_{x\pm y\pm}$

t_{x+} Output waveform rise time as measured from 10% to 90% or 20% to 80% points on waveform (whichever is specified) at pin x with input conditions as specified.

t_{x-} Output waveform fall time as measured from 90% to 10% or 80% to 20% points on waveform (whichever is specified) at pin x, with input conditions as specified.

f_{Tog} Toggle frequency of a flip-flop or counter device.

f_{shift} Shift rate for a shift register.

Read Mode (Memories)

t_{ACS} Chip Select Access Time

t_{RCS} Chip Select Recovery Time

t_{AA} Address Access Time

Write Mode (Memories)

t_W Write Pulse Width

t_{WSD} Data Setup Time Prior to Write

t_{WHD} Data Hold Time After Write

t_{WSA} Address setup time prior to write

t_{WHA} Address hold time after write

t_{WSCS} Chip select setup time prior to write

t_{WHCS} Chip select hold time after write

t_{WS} Write disable time

t_{WR} Write recovery time

Temperature:

T_{stg}	Maximum temperature at which device may be stored without damage or performance degradation.
T_J	Junction (or die) temperature of an integrated circuit device.
T_A	Ambient (environment) temperature existing in the immediate vicinity of an integrated circuit device package.
θ_{JA}	Thermal resistance of an IC package, junction to ambient.
θ_{JC}	Thermal resistance of an IC package, junction to case.
lfpm	Linear feet per minute.
θ_{CA}	Thermal resistance of an IC package, case to ambient.

Miscellaneous:

e_g	Signal generator inputs to a test circuit.
TP_{in}	Test point at input of unit under test.
TP_{out}	Test point at output of unit under test.
D.U.T.	Device under test.
C_{in}	Input capacitance.
C_{out}	Output capacitance.
Z_{out}	Output impedance.
P_D	The total dc power applied to a device, not including any power delivered from the device to a load.
R_L	Load Resistance.
R_T	Terminating (load) resistor.
R_p	An input pull-down resistor (i.e., connected to the most negative voltage).
P.U.T.	Pin under test.

SECTION II — TECHNICAL DATA

GENERAL CHARACTERISTICS AND SPECIFICATIONS

(See pages 1-5 through 1-7 for definitions of symbols and abbreviations.)

In subsequent sections of this Data Book, the important MECL parameters are identified and characterized, and complete data provided for each of the functions. To make this data as useful as possible, and to avoid a great deal of repetition, the data that is common to all functional blocks in a line is not repeated on each individual sheet. Rather, these common characteristics, as well as the application information that applies to each family, are discussed in this section.

In general, the common characteristics of major importance are:

Maximum Ratings, including both dc and ac characteristics and temperature limits;

Transfer Characteristics, which define logic levels and switching thresholds;

DC Parameters, such as output levels, threshold levels, and forcing functions.

AC Parameters, such as propagation delays, rise and fall times and other time dependent characteristics.

In addition, this section will discuss general layout and design guides that will help the designer in building and testing systems with MECL circuits.

LETTER SYMBOLS AND ABBREVIATIONS

Throughout this section, and in the subsequent data sheets, letter symbols and abbreviations will be used in discussing electrical characteristics and specifications. The symbols used in this book, and their definitions, are listed on the preceding pages.

MAXIMUM RATINGS

The limit parameters beyond which the life of the devices may be impaired are given in Figure 4a. In addition, Table 4b provides certain limits which, if exceeded, will not damage the devices, but could degrade the performance below that of the guaranteed specifications.

FIGURE 4a — LIMITS BEYOND WHICH DEVICE LIFE MAY BE IMPAIRED

Characteristic	Symbol	Unit	MECL 10KH	MECL 10K	MECL III
Power Supply	V_{EE}	Vdc	−8.0 to 0	−8.0 to 0	−8.0 to 0
Input Voltage (V_{CC} = 0)	V_{in}	Vdc	0 to V_{EE}	0 to V_{EE}	0 to V_{EE}
Output Source Current Continuous	I_{out}	mAdc	50	50	40
Output Source Current Surge	I_{out}	mAdc	100	100	—
Storage Temperature	T_{stg}	°C	−55 to +150	−55 to +150	−55 to +150
Junction Temperature Ceramic Package ①	T_J	°C	165	165	165 ②
Junction Temperature Plastic Package ③	T_J	°C	140	140	140

NOTES: 1. Maximum T_J may be exceeded (≤ 250°C) for short periods of time (≤ 240 hours) without significant reduction in device life.

2. Except MC1666 – MC1670 which have maximum junction temperatures = 145°C.

3. For long term (≥ 10 yrs.) max T_J of 110°C required. Max T_J may be exceeded (≤ 175°C) for short periods of time (≤ 240 hours) without significant reduction in device life.

FIGURE 4b — LIMITS BEYOND WHICH PERFORMANCE MAY BE DEGRADED

Characteristics	Symbol	Unit	MECL 10KH	MECL 10K	MECL III
Operating Temperature Range Commercial ①	T_A	°C	0 to +75	-30 to +85	−30 to +85
Operating Temperature Range MIL ①	T_A	°C	—	−55 to +125	−55 to +125 (MC1648M)
Supply Voltage (V_{CC} = 0)	V_{EE}	Vdc	-4.94 to -5.46 ⑤	−4.68 to −5.72 ②	−4.68 to −5.72 ②
Supply Voltage (V_{CC} = 0)	V_{TT}	Vdc	—	—	—
Output Drive Commercial	—	Ω	50 Ω to −2.0 Vdc	50 Ω to -2.0 Vdc	50 Ω to −2.0 Vdc ④
Output Drive MIL	—	Ω	—	100 Ω to −2.0 Vdc	—
Maximum Clock Input Rise and Fall Time (20% to 80%)	t_r, t_f	ns	—	—	③

NOTES: 1. With airflow ≥ 500 lfpm.

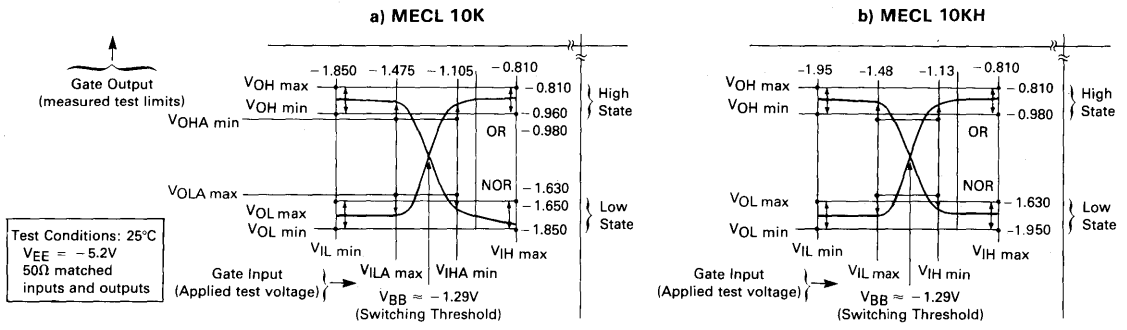
2. Functionality only. Data sheet limits are specified for −5.2 V ± 0.010 V.

3. 10 ns maximum limit for MC1690, MC1697, and MC1699.

4. Except MC1648 which has an internal output pulldown resistor.

5. Functional and Data sheet limits.

FIGURE 5 — MECL TRANSFER CURVES
and SPECIFICATION TEST POINTS



MECL TRANSFER CURVES

For MECL logic gates, the dual (complementary) outputs must be represented by two transfer curves: one to describe the OR switching action and one to describe the NOR switching action. Typical transfer curves and associated data for the MECL 10K/10KH family are shown in Figure 5.a and 5.b respectively.

It is not necessary to measure transfer curves at all points of the curves. To guarantee correct operation it is sufficient merely to measure two sets of min/max logic level parameters.

The first set is obtained for 10K by applying test voltages, $V_{IL\ min}$ and $V_{IH\ max}$ (sequentially) to the gate inputs, and measuring the OR and NOR output levels to make sure they are between $V_{OL\ max}$ and $V_{OL\ min}$, and $V_{OH\ max}$ and $V_{OH\ min}$ specifications.

The second set of logic level parameters relates to the switching thresholds. This set of data is distinguished by an "A" in symbol subscripts. A test voltage, $V_{ILA\ max}$, is applied to the gate and the NOR and OR outputs are measured to see that they are above the $V_{OHA\ min}$ and below the $V_{OLA\ max}$ levels, respectively. Similar checks are made using the test input voltage $V_{IHA\ min}$.

The result of these specifications insures that:

a) The switching threshold ($\approx V_{BB}$) falls within the darkest rectangle; i.e. switching does not begin outside this rectangle;

b) Quiescent logic levels fall in the lightest shaded ranges;

c) Guaranteed noise immunity is met.

As shown in Figure 6, MECL 10K outputs rise with increasing ambient temperature. All circuits in each family have the same worst-case output level specifications regardless of power dissipation or junction temperature differences to reduce loss of noise margin due to thermal differences.

All of these specifications assume −5.2 V power supply operation. Operation at other power-supply voltages is possible, but will result in further transfer curve changes. Figure 7 gives rate of change of output voltages as a function of power supply.

FIGURE 6 — TYPICAL TRANSFER
CHARACTERISTICS AS A FUNCTION
OF TEMPERATURE (MECL 10K)

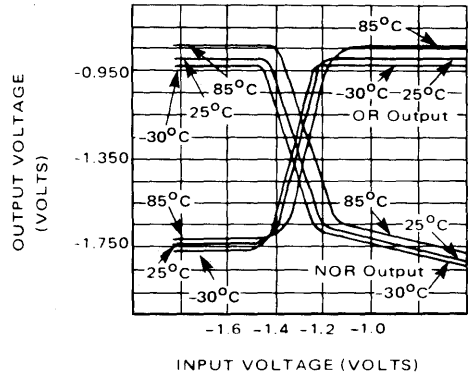


FIGURE 7 — TYPICAL LEVEL CHANGE RATES

Voltage	MECL 10KH	MECL 10K*	MECL III
$\Delta V_{OH}/\Delta V_{EE}$	0.008	0.016	
$\Delta V_{OL}/\Delta V_{EE}$	0.020	0.250	0.270
$\Delta V_{BB}/\Delta V_{EE}$	0.010	0.148	0.140

* and subsets: 10,200; 10,500; 10,600.

NOISE MARGIN

"Noise margin" is a measure of logic circuit's resistance to undesired switching. MECL noise margin is defined in terms of the specification points surrounding the switching threshold. The critical parameters of interest here are those designated with the "A" subscript (V_{OHA} min, V_{OLA} max, V_{IHA} min, V_{ILA} max) in the transfer characteristic curves. MECL 10KH is specified and tested with V_{OHA} min equal V_{OH} min, V_{OLA} max equal V_{OL} max, V_{IHA} min equal V_{IH} min and V_{ILA} max equal V_{IL} max. Guaranteed noise margin (NM) is defined as follows:

$NM_{HIGH\ LEVEL} = V_{OHA}\ min - V_{IHA}\ min$
$NM_{LOW\ LEVEL} = V_{ILA}\ max - V_{OLA}\ max$

To see how noise margin is computed, assume a MECL gate drives a similar MECL gate, Figure 8.

At a gate input (point B) equal to $V_{ILA\ max}$, MECL gate #2 can begin to enter the shaded transition region.

This is a "worst case" condition, since the V_{OLA} max specification point guarantees that no device can enter the transition region before an input equal to V_{ILA} max is reached. Clearly then, $V_{ILA\ max}$ is one critical point for noise margin computation, since it is the edge of the transition region.

To find the other critical voltage, consider the output from MECL gate #1 (point A). What is the most positive value possible for this voltage (considering worst case specifications)? From Figure 8 it can be observed that the V_{OLA} max specification insures that the LOW state OR output from gate #1 can be no greater than V_{OLA} max.

Note that V_{OLA} max is more negative than V_{ILA} max. Thus, with V_{OLA} max at the input to gate #2, the transition region is not yet reached. (The input voltage to gate #2 is still to the left of V_{ILA} max on the transfer curve.)

In order to ever run the chance of switching gate #2, we would need an additional voltage, to move the input from V_{OLA} max to V_{ILA} max. This constitutes the "safety factor" known as noise margin. It can be calculated as the magnitude of the difference between the two specification voltages, or for the MECL 10K levels shown:

NM_{LOW} $= -V_{ILA}\ max - V_{OLA}\ max$
$= -1.475\ V - (-1.630\ V)$
$= 155\ mV.$

Similarly, for the HIGH state:

NM_{HIGH} $= -V_{OHA}\ min - V_{IHA}\ min$
$= -0.980\ V - (-1.105\ V)$
$= 125\ mV$

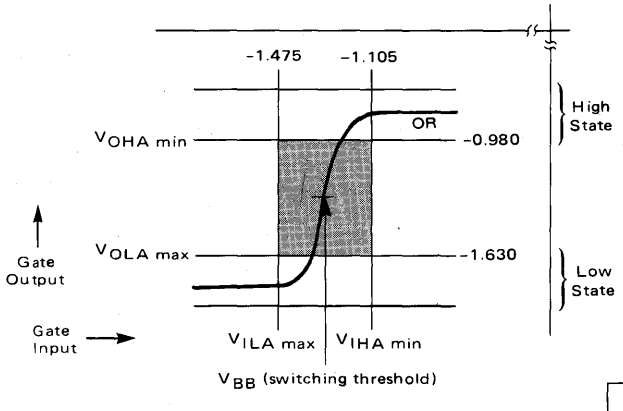
Analogous results are obtained when considering the "NOR" transfer data.

Note that these noise margins are absolute worst case conditions. The lessor of the two noise margins is that for the HIGH state, 125 mV. This then, constitutes the guaranteed margin against signal undershoot, and power or thermal disturbances.

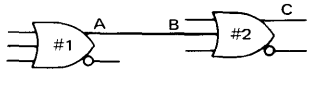
As shown in the table, typical noise margins are usually better than guaranteed — by about 75 mV. For MECL 10KH the "noise margin" is 150 mV for NM low and NM high. (See Section 3 for details.)

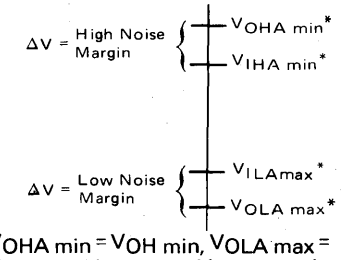
Noise margin is a dc specification that can be calculated, since it is defined by specification points tabulated on MECL data sheets. However, by itself, this specification does not give a complete picture regarding the noise immunity of a system built with a particular set of circuits. Overall system noise immunity involves not only noise-margin specifications, but also other circuit-related factors that determine how difficult it is to apply a noise signal of sufficient magnitude and duration to cause the circuit to propagate a false logic state. In general, then, noise immunity involves line impedances, circuit output impedances, and propagation delay in addition to noise-margin specifications. This subject is discussed in greater detail in Application Note AN-592.

FIGURE 8 — MECL Noise Margin Data



Specification Points for Determining Noise Margin





*V_{OHA} min = V_{OH} min, V_{OLA} max = V_{OL} max, V_{IHA} min = V_{IH} min and V_{ILA} max = V_{IL} max for MECL 10KH.

Noise Margin Computations

Family	Guaranteed Worst-Case dc Noise Margin (V)	Typical dc Noise Margin (V)
MECL 10kH	0.150	0.270
MECL 10k	0.125	0.210
MECL III	0.115	0.200

AC OR SWITCHING PARAMETERS

Time-dependent specifications are those that define the effects of the circuit on a specified input signal, as it travels through the circuit. They include the time delay involved in changing the output level from one logic state to another. In addition, they include the time required for the output of a circuit to respond to the input signal, designated as propagation delay, MECL waveform and propagation delay terminologies are depicted in Figure 9. Specific rise, fall, and propagation delay times are given on the data sheet for each specific functional block, but like the transfer characteristics, ac parameters are temperature and voltage dependent. Typical variations for MECL 10K are given in the curves of Figure 10.

FIGURE 9 — TYPICAL LOGIC WAVEFORMS

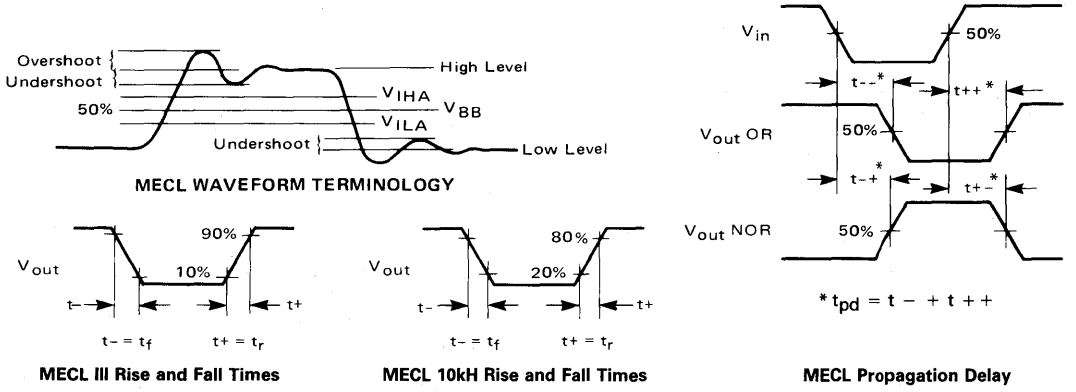


FIGURE 10a — TYPICAL PROPAGATION DELAY t- - versus V_{EE} AND TEMPERATURE (MECL 10K)

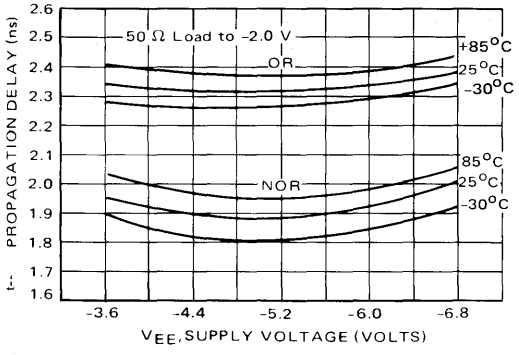


FIGURE 10b — TYPICAL PROPAGATION DELAY t+ + versus V_{EE} AND TEMPERATURE (MECL 10K)

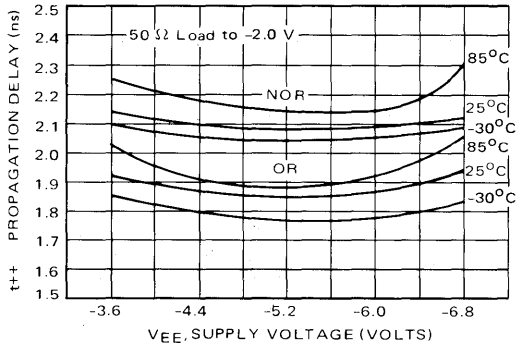


FIGURE 10c — TYPICAL FALL TIME (90% to 10%) versus TEMPERATURE AND SUPPLY VOLTAGE (MECL 10K)

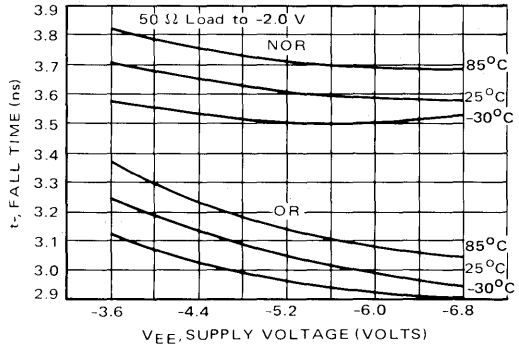
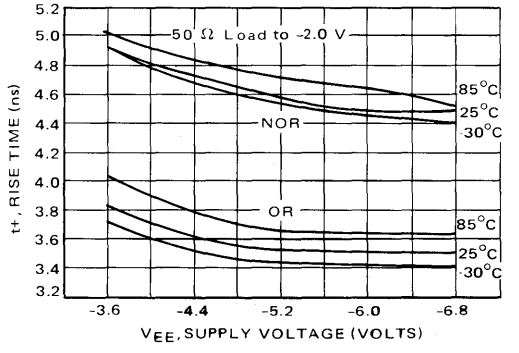


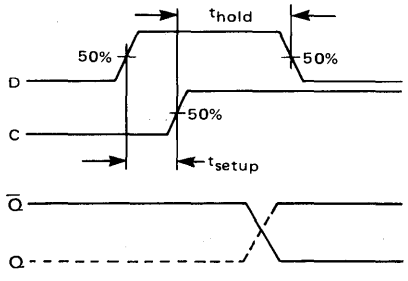
FIGURE 10d — TYPICAL RISE TIME (10% to 90%) versus TEMPERATURE AND SUPPLY VOLTAGE (MECL 10K)



SETUP AND HOLD TIMES

Setup and hold times are two ac parameters which can easily be confused unless clearly defined. For MECL logic devices, t_{setup} is the minimum time (50% – 50%) before the positive transition of the clock pulse (C) that information must be present at the Data input (D) to insure proper operation of the device. The t_{hold} is defined similarly as the minimum time after the positive transition of the clock pulse (C) that the information must remain unchanged at the Data input (D) to insure proper operation. Setup and hold waveforms for logic devices are shown in Figure 11.

FIGURE 11 — SETUP AND HOLD WAVEFORMS FOR MECL LOGIC DEVICES



TESTING MECL 10KH, MECL 10K and MECL III

To obtain results correlating with Motorola circuit specifications certain test techniques must be used. A schematic of a typical gate test circuit is shown in Figure 12. This test circuit is the standard ac test configuration for most MECL devices. (Exceptions are shown with the device specification.)

A solid ground plane is used in the test setup, and capacitors bypass V_{CC1}, V_{CC2}, and V_{EE} pins to ground. All power leads and signal leads are kept as short as possible.

The sampling scope interface runs directly to the 50-ohm inputs of Channel A and B via 50-ohm coaxial cable. Equal-length coaxial cables must be used between the test set and the A and B scope inputs. A 50-ohm coax cable such as RG58/U or RG188A/U, is recommended.

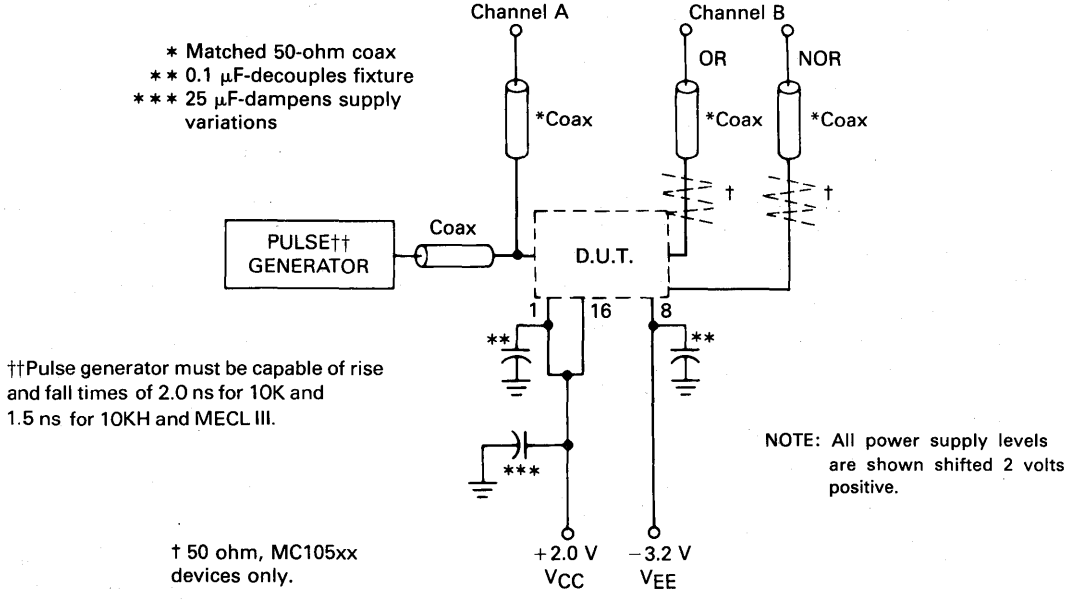
Interconnect fittings should be 50-ohm GR, BNC, Sealectro Conhex, or equivalent. Wire length should be < ¼ inch from TP_{in} to input pin and TP_{out} to output pin.

The pulse generator must be capable of 2.0 ns rise and fall times for MECL 10K and 1.5 ns for MECL 10KH and MECL III. In addition, the generator voltage must have an offset to give MECL signal swings of ≈ ±400 mV about a threshold of ≈ + 0.7 V when V_{CC} = +2.0 V and V_{EE} = –3.2 V for ac testing of logic devices.

The power supplies are shifted +2.0 V, so that the device under test has only one resistor value to load into – the precision 50-ohm input impedance of the sampling oscilloscope. Use of this technique yields a close correlation between Motorola and customer testing. Unused outputs are loaded with a 50-ohm resistor (100-ohm for MC105XX devices) to ground. The positive supply (V_{CC}) should be decoupled from the test board by RF type 25μF capacitors to ground. The V_{CC} pins are bypassed to ground with 0.1 μF, as is the V_{EE} pin.

Additional information on testing MECL 10K and understanding data sheets is found in Application Notes AN-579 and AN-701.

FIGURE 12 — MECL LOGIC SWITCHING TIME TEST SETUP



SECTION III — OPERATIONAL DATA

POWER SUPPLY CONSIDERATIONS

MECL circuits are characterized with the V_{CC} point at ground potential and the V_{EE} point at −5.2 V. While this MECL convention is not necessarily mandatory, it does result in maximum noise immunity. This is so because any noise induced on the V_{EE} line is applied to the circuit as a common-mode signal which is rejected by the differential action of the MECL input circuit. Noise induced into the V_{CC} line is not cancelled out in this fashion. Hence, a good system ground at the V_{CC} bus is required for best noise immunity. Also, MECL 10KH circuits may be operated with V_{EE} at −4.5 V with a negligible loss of noise immunity.

Power supply regulation which will achieve 10% regulation or better at the device level is recommended. The −5.2 V power supply potential will result in best circuit speed. Other values for V_{EE} may be used. A more negative voltage will increase noise margins at a cost of increased power dissipation. A less negative voltage will have just the opposite effect. (Noise margins and performance specifications of MECL 10KH are unaffected by variations in V_{EE} because of the internal voltage regulation.)

On logic cards, a ground plane or ground bus system should be used. A bus system should be wide enough to prevent significant voltage drops between supply and device and to produce a low source inductance.

Although little power supply noise is generated by MECL logic, power supply bypass capacitors are recommended to handle switching currents caused by stray capacitance and asymmetric circuit loading. A parallel combination of a 1.0 μF and a 100 pF capacitor at the power entrance to the board, and a 0.01 μF low-inductance capacitor between ground and the −5.2 V line every four to six packages, are recommended.

Most MECL 10KH, MECL 10K and MECL III circuits have two V_{CC} leads. V_{CC1} supplies current to the output transistors and V_{CC2} is connected to the circuit logic transistors. The separate V_{CC} pins reduce cross-coupling between individual circuits within a package when the outputs are driving heavy loads. Circuits with large drive capability, similar to the MC10110, have two V_{CC1} pins. All V_{CC} pins should be connected to the ground plane or ground bus as close to the package as possible.

For further discussion of MECL power supply considerations to be made in system designing, see MECL System Design Handbook.

POWER DISSIPATION

The power dissipation of MECL functional blocks is specified on their respective data sheets. This specification does not include power dissipated in the output devices due to output termination. The omission of internal output pulldown resistors permits the use of external terminations designed to yield best system performance. To obtain total operating power dissipation of a particular functional block in a system, the dissipation of the output transistor, under load, must be added to the circuit power dissipation.

The table in Figure 13 lists the power dissipation in the output transistors plus that in the external terminating resistors, for the more commonly used termination values and circuit configurations. To obtain true package power dissipation, one output-transistor power-dissipation value must be added to the specified package power dissipation for each external termination resistor used in conjunction with that package. To obtain system power dissipation, the stated dissipation in the external terminating resistors must be added as well. Unused outputs draw no power and may be ignored.

FIGURE 13 — AVERAGE POWER DISSIPATION IN OUTPUT CIRCUIT WITH EXTERNAL TERMINATING RESISTORS

Terminating Resistor Value	Output Transistor Power Dissipation (mW)	Terminating Resistor Power Dissipation (mW)
150 ohms to −2.0 Vdc	5.0	4.3
100 ohms to −2.0 Vdc	7.5	6.5
75 ohms to −2.0 Vdc	10	8.7
50 ohms to −2.0 Vdc	15	13
2.0 k ohms to V_{EE}	2.5	7.7
1.0 k ohm to V_{EE}	4.9	15.4
680 ohms to V_{EE}	7.2	22.6
510 ohms to V_{EE}	9.7	30.2
270 ohms to V_{EE}	18.3	57.2
82 ohms to V_{CC} and 130 ohms to V_{EE}	15	140

LOADING CHARACTERISTICS

The differential input to MECL circuits offers several advantages. Its common-mode-rejection feature offers immunity against power-supply noise injection, and its relatively high input impedance makes it possible for any circuit to drive a relatively large number of inputs without deterioration of the guaranteed noise margin. Hence, dc fanout with MECL circuits does not normally present a design problem.

Graphs showing typical output voltage levels as a function of load current for MECL 10KH, MECL 10K and MECL III shown in Figure 14. These graphs can be used to determine the actual output voltages for loads exceeding normal operation.

While dc loading causes a change in output voltage levels, thereby tending to affect noise margins, ac loading increases the capacitances associated with the circuit and, therefore, affects circuit speed, primarily rise and fall times.

MECL circuits typically have a 7 ohm output impedance and are relatively unaffected by capacitive loading on a positive-going output signal. However, the negative-going edge is dependent on the output pulldown or termination resistor. Loading close to a MECL output pin will cause an additional propagation delay of 0.1 ns per fanout load with a 50 ohm resistor to −2.0 Vdc or 270 ohms to −5.2 Vdc. A 100 ohm resistor to −2.0 Vdc or

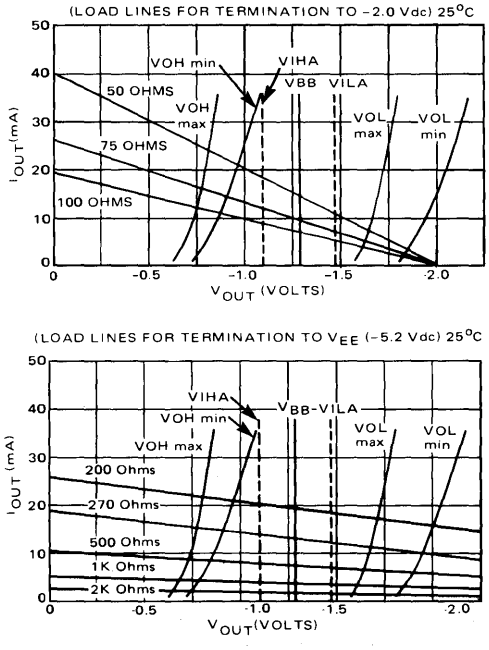
510 ohms to −5.2 Vdc results in an additional 0.2 ns propagation delay per fanout load.

Terminated transmission line signal interconnections are used for best system performance. The propagation delay and rise time of a driving gate are affected very liitle by capacitance loading along a matched parallel-terminated transmission line. However, the delay and characteristic impedance of the transmission line itself are affected by the distributed capacitance. Signal propagation down the line will be increased by a factor, $\sqrt{1+C_d/C_o}$. Here C_o is the normal intrinsic line capacitance, and C_d is the distributed capacitance due to loading and stubs off the line.

Maximum allowable stub lengths for loading off of a MECL 10K transmission line vary with the line impedance. For example, with Z_o = 50 ohns, maximum stub length would be 4.5 inches (1.8 in. for MECL III). But when Z_o = 100 ohms, the maximum allowable stub length is decreased to 2.8 inches (1.0 in. for MECL III).

The input loading capacitance of a MECL 10KH and MECL 10K gate is about 2.9 pF and 3.3 pF for MECL III. To allow for the IC connector or solder connection and a short stub length, 5 to 7 pF is commonly used in loading calculations.

FIGURE 14 — OUTPUT VOLTAGE LEVELS versus DC LOADING



UNUSED MECL INPUTS

The input impedance of a differential amplifier, as used in the typical MECL input circuit, is very high when the applied signal level is low. Under low-signal conditions, therefore, any leakage to the input capacitance of the gate could cause a gradual buildup of voltage on the input lead, thereby adversely affecting the switching characteristics at low repetition rates.

All single-ended input MECL logic circuits contain input pulldown resistors between the input transistor bases and V_{EE}. As a result, unused inputs may be left unconnected (the resistor provides a sink for I_{CBO} leakage currents, and inputs are held sufficiently negative that circuits will not trigger due to noise coupled into such inputs). Input pulldown resistor values are typically 50 kΩ and are not to be used as pulldown resistors for preceding open-emitter outputs.

MECL devices do not have input pulldowns. Examples are the differential line receivers. If a single differential receiver within a package is unused, one input of that receiver must be tied to the V_{BB} pin provided, and the other input goes to V_{EE}.

MECL circuits do not operate properly when inputs are connected to V_{CC} for a HIGH logic level. Proper design practice is to set a HIGH level as about-0.9 volts below V_{CC} with a resistor divider, a diode drop, or an unused gate output.

SECTION IV — SYSTEM DESIGN CONSIDERATIONS

THERMAL MANAGEMENT

Circuit performance and long-term circuit reliability are affected by die temperature. Normally, both are improved by keeping the IC junction temperatures low.

Electrical power dissipated in any integrated circuit is a source of heat. This heat source increases the temperature of the die relative to some reference point, normally the ambient temperature of 25°C in still air. The temperature increase, then, depends on the amount of power dissipated in the circuit and on the net thermal resistance between the heat source and the reference point.

The temperature at the junction is a function of the packaging and mounting system's ability to remove heat generated in the circuit — from the junction region to the ambient environment. The basic formula (a) for converting power dissipation to estimated junction temperature is:

$$T_J = T_A + P_D(\bar{\theta}_{JC} + \bar{\theta}_{CA}) \quad (1)$$

or

$$T_J = T_A + P_D(\bar{\theta}_{JA}) \quad (2)$$

where

T_J = maximum junction temperature
T_A = maximum ambient temperature
P_D = calculated maximum power dissipation including effects of external loads (see Power Dissipation in section III).

$\bar{\theta}_{JC}$ = average thermal resistance, junction to case
$\bar{\theta}_{CA}$ = average thermal resistance, case to ambient
$\bar{\theta}_{JA}$ = average thermal resistance, junction to ambient

This Motorola recommended formula has been approved by RADC and DESC for calculating a "practical" maximum operating junction temperature for MIL-M-38510 (JAN) MECL 10K devices.

Only two terms on the right side of equation (1) can be varied by the user — the ambient temperature, and the device case-to-ambient thermal resistance, $\bar{\theta}_{CA}$. (To some extent the device power dissipation can be also controlled, but under recommended use the V_{EE} supply and loading dictate a fixed power dissipation.) Both system air flow and the package mounting technique affect the $\bar{\theta}_{CA}$ thermal resistance term. $\bar{\theta}_{JC}$ is essentially independent of air flow and external mounting method, but is sensitive to package material, die bonding method, and die area.

FIGURE 15 — THERMAL RESISTANCE VALUES FOR STANDARD MECL I/C PACKAGES

THERMAL RESISTANCE IN STILL AIR										
PACKAGE DESCRIPTION							θ_{JA} (°C/WATT)		θ_{JC} (°C/WATT)	
NO. LEADS	BODY STYLE	BODY MATERIAL	BODY WxL	DIE BOND	DIE AREA (SQ. MILS)	FLAG AREA (SQ. MILS)	AVG.	MAX.	AVG.	MAX.
8	DIL	EPOXY	1/4"x3/8"	EPOXY	2496	8100	102	133	50	80
8	DIL	ALUMINA	1/4"x3/8"	GOLD	2496	N/A	140	182	35	56
14	FLAT	ALUMINA	1/4"x1/4"	GOLD	4096	N/A	165	215	28	45
14	DIL	EPOXY	1/4"x3/4"	EPOXY	4096	6400	84	109	38	61
14	DIL	ALUMINA	1/4"x3/4"	GOLD	4096	N/A	100	130	25	40
16	FLAT	BEO	1/4"x3/8"	GOLD	4096	N/A	88	114	13	21
16	FLAT	ALUMINA	1/4"x3/8"	GOLD	4096	N/A	140	182	24	38
16	DIL	EPOXY	1/4"x3/4"	EPOXY	4096	12100	70	91	34	54
16	DIL	ALUMINA	1/4"x3/4"	GOLD	4096	N/A	100	130	25	40
24	FLAT	BEO	3/8"x5/8"	GOLD	8192	N/A	40	52	6	10
24	FLAT	ALUMINA	3/8"x5/8"	GOLD	8192	N/A	64	83	11	18
24	DIL	EPOXY	1/2"x1-1/4"	EPOXY	8192	22500	67	87	31	50
24	DIL	ALUMINA	1/2"x1-1/4"	GOLD	8192	N/A	50	65	10	16

NOTES:
1. All plastic packages use copper lead frames—ceramic packages use alloy 42 frames.
2. Body style DIL is "Dual-In-Line".
3. BEO body material is only used for military temperature range products.
4. Standard Mounting Methods:
   a. Dual-In-Line In Socket or P/C board with no contact between bottom of package and socket or P/C board.
   b. Flat Pack—Bottom of package in direct contact with non-metallized area of P/C board.

For applications where the case is held at essentially a fixed temperature by mounting on a large or temperature-controlled heat sink, the estimated junction temperature is calculated by:

$$T_J = T_C + P_D(\bar{\theta}_{JC}) \quad (3)$$

where T_C = maximum case temperature and the other parameters are as previously defined.

The maximum and average thermal resistance values for standard MECL IC packages are given in Figure 15. In Figure 16, this basic data is converted into graphs showing the maximum power dissipation allowable at various ambient temperatures (still air) for circuits mounted in the different packages, taking into account the maximum permissible operating junction temperature for long term life (≥ 100,000 hours).

AIR FLOW

The effect of air flow over the packages on $\bar{\theta}_{JA}$ (due to a decrease in $\bar{\theta}_{CA}$) is illustrated in the graphs of Figure 17. This air flow reduces the thermal resistance of the package, therefore permitting a corresponding increase in power dissipation without exceeding the maximum permissible operating junction temperature.

As an example of the use of the information above, the maximum junction temperature for a 16 lead ceramic dual-in-line packaged MECL 10K quad OR/NOR gate (MC10101L) loaded with four 50 ohm loads can be calculated. Maximum total power dissipation (including 4 output loads) for this quad gate is 195 mW. Assume for this thermal study that air flow is 500 linear feet per minute. From Figure 17, $\bar{\theta}_{JA}$ is 50°C/W. With T_A (air flow temperature at the device) equal to 25°C, the following maximum junction temperature results:

$$T_J = P_D(\bar{\theta}_{JA}) + T_A$$
$$T_J = (0.195\ W)\ (50°C/W + 25°C = 34.8°C$$

Under the above operating conditions, the MECL 10k quad gate has its junction elevated above ambient temperature by only 9.8°C.

Even though different device types mounted on a printed circuit board may each have different power dissipations, all will have the same input and output levels provided that each is subject to identical air flow and the same ambient air temperature. This eases design, since the only change in levels between devices is due to the increase in ambient temperatures as the air passes over

FIGURE 16A—AMBIENT TEMPERATURE DERATING CURVES (CERAMIC DUAL-IN-LINE PACKAGE)

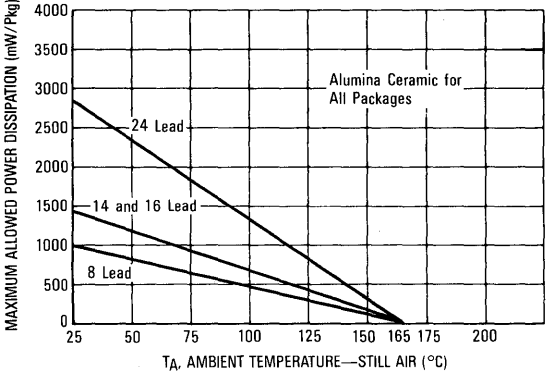


FIGURE 17A—AIRFLOW VERSUS THERMAL RESISTANCE (CERAMIC DUAL-IN-LINE PACKAGE)

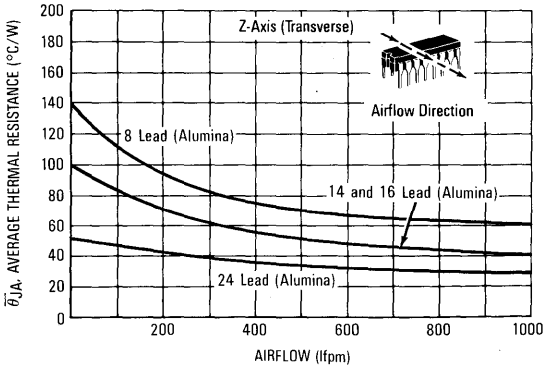


FIGURE 16B—AMBIENT TEMPERATURE DERATING CURVES (CERAMIC FLAT PACKAGE)

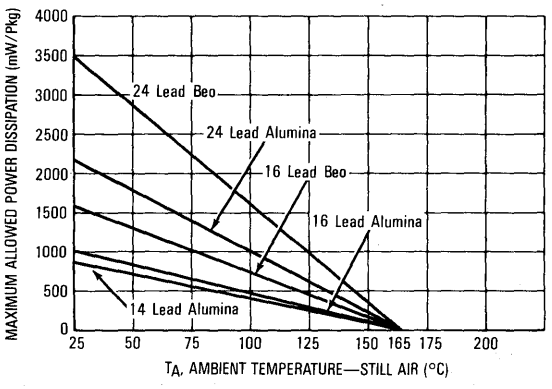


FIGURE 17B—AIRFLOW VERSUS THERMAL RESISTANCE (CERAMIC FLAT PACKAGE)

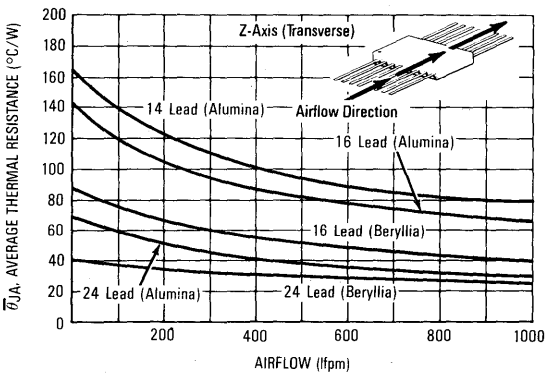


FIGURE 16C—AMBIENT TEMPERATURE DERATING CURVES (PLASTIC DUAL-IN-LINE PACKAGE)

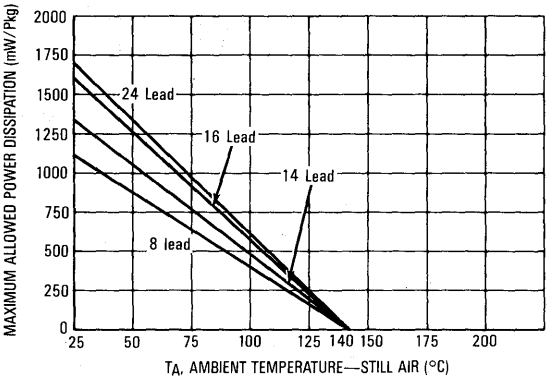
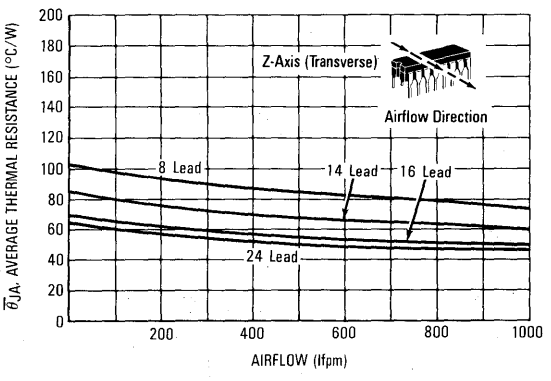


FIGURE 17C—AIRFLOW VERSUS THERMAL RESISTANCE (PLASTIC DUAL-IN-LINE PACKAGE)



the devices, or differences in ambient temperature between two devices.

The majority of MECL 10KH, MECL 10K, and MECL III users employ some form of air-flow cooling. As air passes over each device on a printed circuit board, it absorbs heat from each package. This heat gradient from the first package to the last package is a function of the air flow rate and individual package dissipations. Figure 18 provides gradient data at power levels of 200 mW, 250mW, 300 mW, and 400 mW with an air flow rate of 500 lfpm. These figures show the proportionate increase in the junction temperature of each dual in-line package as the air passes over each device. For higher rates of air flow the change in junction temperature from package to package down the airstream will be lower due to greater cooling.

FIGURE 18 — THERMAL GRADIENT OF JUNCTION TEMPERATURE (16-Pin MECL Dual-In-Line Package)

Power Dissipation (mW)	Junction Temperature Gradient (°C/Package)
200	0.4
250	0.5
300	0.63
400	0.88

Devices mounted on 0.062" PC board with Z axis spacing of 0.5". Air flow is 500 lfpm along the Z axis.

THERMAL EFFECTS ON NOISE MARGIN

The data sheet dc specifications for standard MECL 10K and MECL III devices are given for an operating temperature range from −30°C to +85°C (0° to +75°C for MECL 10KH and memories.) These values are based on having an airflow of 500 lfpm over socket or P/C board mounted packages with no special heat sinking (i.e., dual-in-line package mounted on lead seating plane with no contact between bottom of package and socket or P/C board and flat package mounted with bottom in direct contact with non-metallized area of P/C board). Under these conditions, adequate cooling is provided to keep the maximum operating junction temperatures below 145°C for MECL III device types 1666–1670 and below 165°C for all other MECL device types.

The designer may want to use MECL devices under conditions other than those given above. The majority of the low-power device types may be used without air and with higher θ_{JA}. However, the designer must bear in mind that junction temperatures will be higher for higher θ_{JA}, even though the ambient temperature is the same. Higher junction temperatures will cause logic levels to shift.

As an example, a 300 mW 16 lead dual-in-line ceramic device operated at θ_{JA} = 100°C/W (in still air) shows a HIGH logic level shift of about 21 mV above the HIGH logic level when operated with 500 lfpm air flow and a θ_{JA} = 50°C/W. (Level shift = $\Delta T_J \times 1.4$ mV/°C).

If logic levels of individual devices shift by different amounts (depending on P_D and θ_{JA}), noise margins are somewhat reduced. Therefore, the system designer must lay out his system bearing in mind that the mounting procedures to be used should minimize thermal effects on noise margin.

The following sections on package mounting and heat sinking are intended to provide the designer with sufficient information to insure good noise margins and high reliability in MECL system use.

MOUNTING AND HEAT SINK SUGGESTIONS

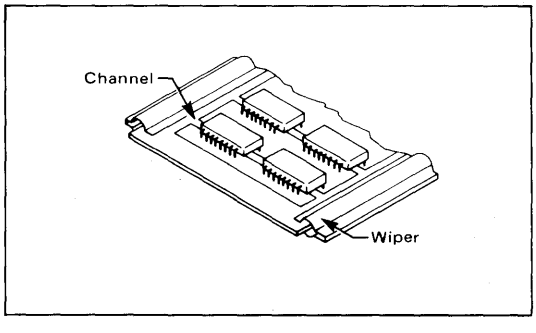
With large high-speed logic systems, the use of multilayer printed circuit boards is recommended to provide both a better ground plane and a good thermal path for heat dissipation. Also, a multilayer board allows the use of microstrip line techniques to provide transmission line interconnections.

Two-sided printed circuit boards may be used where board dimensions and package count are small. If possible, the V_{CC} ground plane should face the bottom of the package to form the thermal conduction plane. If signal lines must be placed on both sides of the board, the V_{EE} plane may be used as the thermal plane, and at the same time may be used as a pseudo ground plane. The pseudo ground plane becomes the ac ground reference under the signal lines placed on the same side as the V_{CC} ground plane (now on the opposite side of the board from the packages), thus maintaining a microstrip signal line environment.

Two-ounce copper P/C board is recommended for thermal conduction and mechanical strength. Also, mounting holes for low power devices may be countersunk to allow the package bottom to contact the heat plane. This technique used along with thermal paste will provide good thermal conduction.

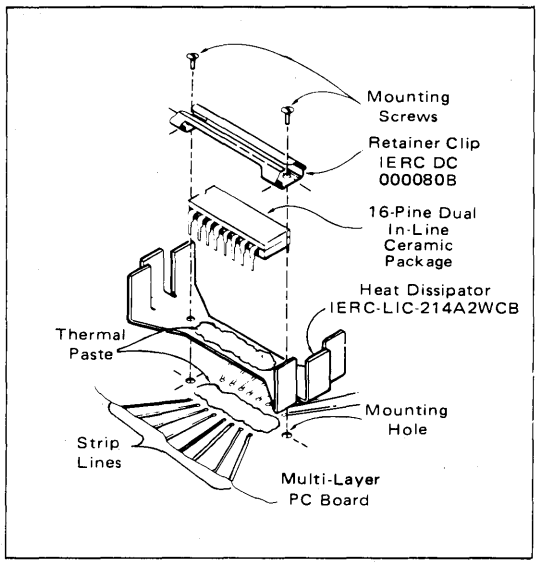
Printed channeling is a useful technique for conduction of heat away from the packages when the devices are soldered into a printed circuit board. As illustrated in Figure 19, this heat dissipation method could also serve as V_{EE} voltage distribution or as a ground bus. The channels should terminate into channel strips at each side or the rear of a plug-in type printed circuit board. The heat can then be removed from the circuit board, or board slide rack, by means of wipers that come into thermal contact with the edge channels.

FIGURE 19 — CHANNEL/WIPER HEAT SINKING ON DOUBLE LAYER BOARD



For operating some of the higher power device types*in 16 lead dual-in-line packages in still air, requiring θ_{JA} <100°C/W, a suitable heat sink is the IERC LIC-214A2WCB shown in Figure 20. This sink reduces the still air θ_{JA} to around 55°C/W. By mounting this heat sink directly on a copper ground plane (using silicone paste) and passing 500 lfpm air over the packages, θ_{JA} is reduced to approximately 35°C/W, permitting use at higher ambient temperatures than +85°C (+75°C for MECL 10KH memories) or in lowering TJ for improved reliability.

FIGURE 20 — MECL HIGH-POWER DUAL-IN-LINE PACKAGE MOUNTING METHOD



It should be noted that the use of a heat sink on the top surface of the dual-in-line package is not very effective in lowering the θ_{JA}. This is due to the location of the die near the bottom surface of the package. Also, very little (< 10%) of the internal heat is withdrawn through the package leads due to the isolation from the ceramic by the solder glass seals and the limited heat conduction from the die through 1.0 to 1.5 mil aluminum bonding wires.

INTERFACING MECL TO SLOWER LOGIC TYPES

MECL circuits are interfaceable with most other logic forms. For MECL/TTL/DTL interfaces, when MECL is operated at the recommended -5.2 volts and TTL/DTL at +5.0 V supply, currently available translator circuits, such as the MC10124 and MC10125, may be used.

For systems where a dual supply (-5.2 V and +5 V) is not practical, the MC12000 includes a single supply MECL to TTL and TTL to MECL translator, or a discrete component translator can be designed. For details, see MECL System Design Handbook. Such circuits can easily be made fast enough for any available TTL.

MECL also interfaces readily with MOS. With CMOS operating at +5 V, any of the MECL to TTL translators works very well. On the other hand, CMOS will drive MECL directly when using a common −5.2 V supply.

Specific circuitry for use in interfacing MECL families to other logic types is given in detail in the MECL System Design Handbook.

Complex MECL 10K devices are presently available for interfacing MECL with MOS logic, MOS memories, TTL three-state circuits, and IBM bus logic levels. See Application Note AN-720 for additional interfacing information.

CIRCUIT INTERCONNECTIONS

Though not necessarily essential, the use of multilayer printed circuit boards offers a number of advantages in the development of high-speed logic cards. Not only do multilayer boards achieve a much higher package density, interconnecting leads are kept shorter, thus minimizing propagation delay between packages. This is particularly beneficial with MECL III which has relatively fast (1 ns) rise and fall times. Moreover, the unbroken ground planes made possible with multilayer boards permit much more precise control of transmission line impedances when these are used for interconnecting purposes. Thus multilayer boards are recommended for MECL III layouts and are justified when operating MECL 10KH and MECL 10K at top circuit speed, when high-density packaging is a requirement, or when transmission line interconnects are used.

Point-to-point back-plane wiring without matched line terminations may be employed for MECL interconnections if line runs are kept short. At MECL 10K speeds, this applies to line runs up to 6 inches, for MECL 10KH up to 3.5", and for MECL III up to 1 inch (Maximum open wire lengths for less than 100 mV undershoot). But, because of the open-emitter outputs of MECL 10KH, MECL 10K and MECL III circuits, pull-down resistors are always required. Several ways of connecting such pull-down resistors are shown in Figure 21.

Resistor values for the connection in Figure 21a may range from 270 ohms to kΩ depending on power and load requirements. (See MECL System Design Handbook.) Power may be saved by connecting pull-down resistors in the range of 50 ohms (100 ohm minimum for MC10,500 and MC10,600 Series parts) to 150 ohms, to −2.0 Vdc, as shown in Figure 21b. Use of a series damping resistor, Figure 21c, will extend permissible lengths of unmatched-impedance interconnections, with some loss of edge speed.

With proper choice of the series damping resistor, line lengths can be extended to any length,** while limiting overshoot and undershoot to a predetermined amount. Damping resistors usually range in value from 10 ohms to 100 ohms, depending on the line length, fanout, and line impedance. The open emitter-follower outputs of MECL 10KH, MECL III and MECL 10K give the system designer all possible line driving options.

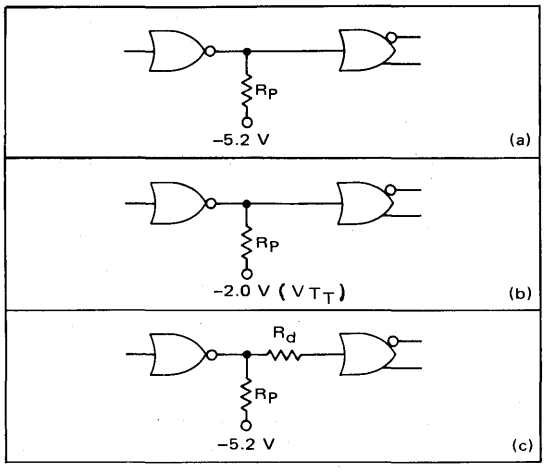
One major advantage of MECL over saturated logic is its capability for driving matched-impedance transmis-

* MC1654, 1678, 1694, 10128, 10129, 10136, 10137, 10177, 10182, and 10804, MaxP_D>800mW.

** Limited only by line attenuation and band-width characteristics.

sion lines. Use of transmission lines retains signal integrity over long distances. The MECL 10KH and MECL 10K emitter-follower output transistors will drive a 50-ohm transmission line (100 ohms or greater MECL 10,500 and MC10,600 Series) terminated to −2.0 Vdc. This is the equivalent current load of 22 mA in the HIGH logic state and 6 mA in the LOW state.

FIGURE 21 — PULL-DOWN RESISTOR TECHNIQUES



Parallel termination of transmission lines can be done in two ways. One, as shown in Figure 22a, uses a single resistor whose value is equal to the impedance (Z_o) of the line. A terminating voltage (V_{TT}) of −2.0 Vdc must be supplied to the terminating resistor.

Another method of parallel termination uses a pair of resistors, R1 and R2. Figure 22b illustrates this method. The following two equations are used to calculate the values of R1 and R2:

$$R1 = 1.6\,Z_o$$
$$R2 = 2.6\,Z_o$$

Another popular approach is the series-terminated transmission line (see Figure 23). This differs from parallel termination in that only one-half the logic swing is propagated through the lines. The logic swing doubles at the end of the transmission line due to reflection on an open line, again establishing a full logic swing.

FIGURE 22a — PARALLEL TERMINATED LINE

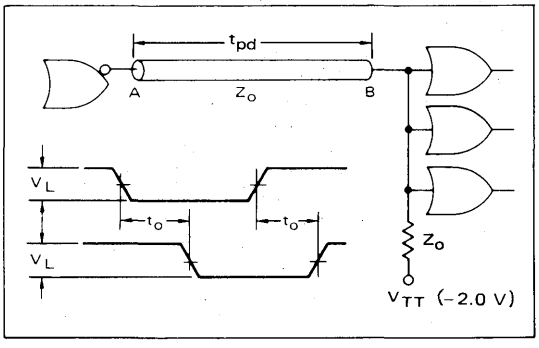
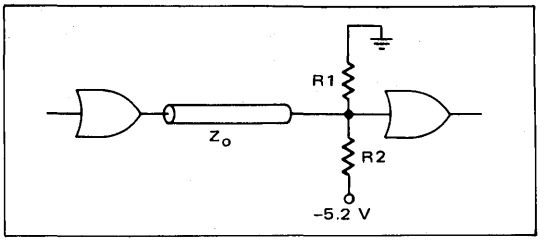
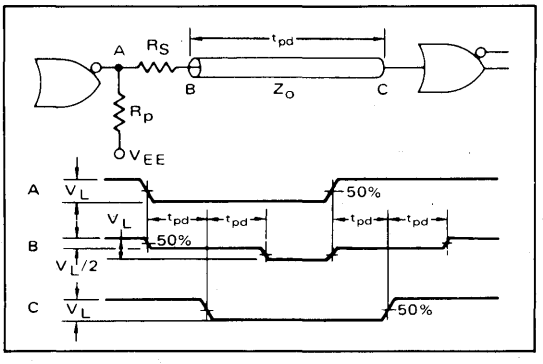


FIGURE 22b — PARALLEL TERMINATION—THEVENIN EQUIVALENT



To maintain clean wave fronts, the input impedance of the driven gate must be much greater than the characteristic impedance of the transmission line. This condition is satisfied by MECL circuits which have high impedance inputs. Using the appropriate terminating resistor (R_S) at point A (Figure 23), the reflections in the transmission line will be terminated.

FIGURE 23 — SERIES TERMINATED LINE



The advantages of series termination include ease of driving multiple series-terminated lines, low power consumption, and low cross talk between adjacent lines. The disadvantage of this system is that loads may not be distributed along the transmission line due to the one-half logic swing present at intermediate points.

For board-to-board interconnections, coaxial cable may be used for signal conductors. The termination techniques just discussed also apply when using coax. Coaxial cable has the advantages of good noise immunity and low attenuation at high frequencies.

Twisted pair lines are one of the most popular methods of interconnecting cards or panels. The complementary outputs of any MECL function may be connected to one end of the twisted pair line, and any MECL differential line receiver to the other as shown in the example, Figure 24. R_T is used to terminate the twisted pair line. The 1 to 1.5 V common-mode noise rejection of the line receiver ignores common-mode cross talk, permitting multiple twisted pair lines to be tied into cables. MECL signals may be sent very long distances (> 1000 feet) on twisted pair, although line attenuation will limit bandwidth, degrading edge speeds when long line runs are made.

If timing is critical, parallel signals paths (shown in Figure 25) should be used when fanout to several cards

is required. This will eliminate distortion caused by long stub lengths off a signal path.

Wire-wrapped connections can be used with MECL 10KH and MECL 10K. For MECL III, the fast edge speeds (1 ns) create a mismatch at the wire-wrap connections which can cause reflections, thus reducing noise immunity, The mismatch occurs also with MECL 10K, but the distance between the wire-wrap connections and the end of the line is generally short enough so the reflections cause no problem.

Series damping resistors may be used with wire-wrapped lines to extend permissible backplane wiring lengths. Twisted pair lines may be used for even longer distances across large wire-wrapped cards. The twisted pair gives a more defined characteristic impedance (than a single wire), and can be connected either single-ended, or differentially using a line receiver.

The recommended wire-wrapped circuit cards have a ground plane on one side and a voltage plane on the other side to insure a good ground and a stable voltage source for the circuits. In addition, the ground plane near the wire-wrapped lines lowers the impedance of those lines and facilitates terminating the line. Finally, the ground plane serves to minimize cross talk between parallel paths in the signal lines. Point-to-point wire routing is recommended because cross talk will be minimized and line lengths will be shortest. Commercial wire-wrap boards designed for MECL 10K are available from several vendors.

FIGURE 24 — TWISTED PAIR LINE DRIVER/RECEIVER

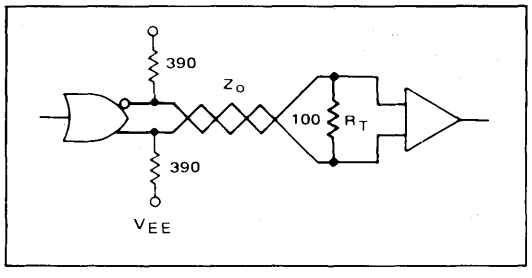
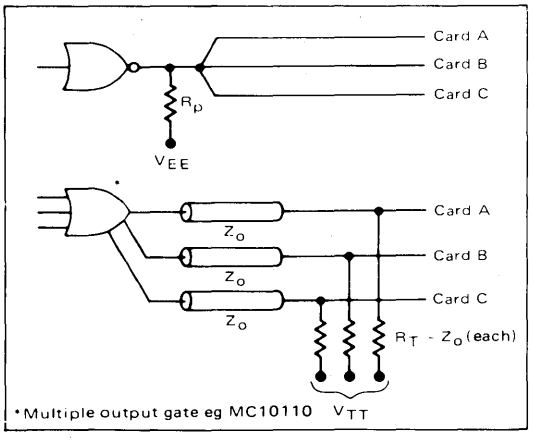


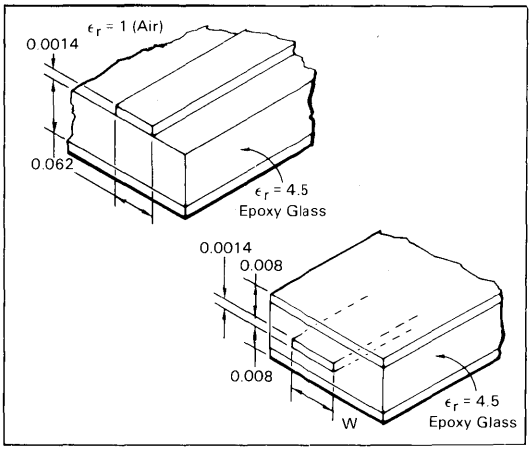
FIGURE 25 — PARALLEL FANOUT TECHNIQUES



Microstrip and Stripline

Microstrip and stripline techniques are used with printed circuit boards to form transmission lines. Microstrip consists of a constant-width conductor on one side of a circuit board, with a ground plane on the other side (shown in Figure 26). The characteristic impedance is determined by the width and thickness of the conductor, the thickness of the circuit board, and the dielectric constant of the circuit board material.

FIGURE 26 — PC INTERCONNECTION LINES FOR USE WITH MECL



Stripline is used with multilayer circuit boards as shown in Figure 26. Stripline consists of a constant-width conductor between two ground planes.

Refer to MECL System Design Handbook for a full discussion of the properties and use of these.

CLOCK DISTRIBUTION

Clock distribution can be a system problem. At MECL 10K speeds, either coaxial cable or twisted pair line (using the MC10101 and MC10115) can be used to distribute clock signals throughout a system. Clock line lengths should be controlled and matched when timing could be critical. Once the clocking signals arrive on card, a tree distribution should be used for large-fanouts at high frequency. An example of the application of ths technique is shown in Figure 27.

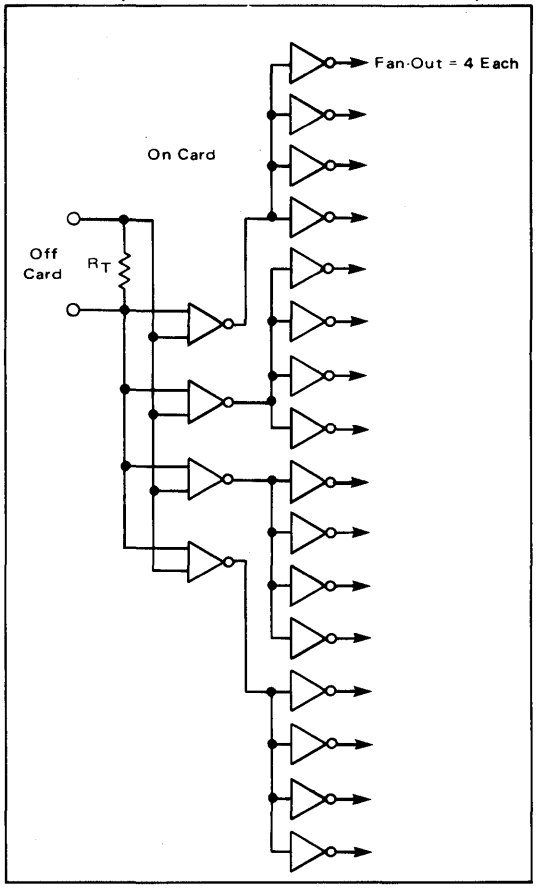
Because of the very high clock rates encountered in MECL III systems, rules for clocking are more rigorous than in slower systems.

The following guidelines should be followed for best results:

A. On-card Synchronous Clock Distribution via Transmission Line

1. Use the NOR output in developing clock chains or trees. Do not mix OR and NOR outputs in the chain.
2. Use balanced fanouts on the clock drivers.
3. Overshoot can be reduced by using two parallel drive lines in place of one drive line with twice the lumped load.

FIGURE 27 — 64 FANOUT CLOCK DISTRIBUTION (PROPER TERMINATION REQUIRED)



4. To minimize clock skewing problems on synchronous sections of the system, line delays should be matched to within 1 ns.

5. Parallel drive gates should be used when clocking repetition rates are high, or when high capacitance loads occur. The bandwidth of a MECL III gate may be extended by paralleling both halves of a dual gate. Approximately 40 or 50 MHz bandwidth can be gained by paralleling two or three clock driver gates.

6. Fanout limits should be applied to clock distribution drivers. Four to six loads should be the maximum load per driver for best high speed performance. Avoid large lumped loads at the end of lines greater than 3 inches. A lumped load, if used, should be four or fewer loads.

7. For wire-OR (emitter dotting), two-way lines (busses) are recommended. To produce such lines, both ends of a transmission line are terminated with 100-ohms impedance. This method should be used when wire-OR connections exceed 1 inch apart on a drive line.

B. Off-Card Clock Distribution

1. The OR/NOR outputs of an MC1660 may be used to drive into twisted pair lines or into flat, fixed-impedance ribbon cable. At the far end of the twisted pair an MC1692 differential line receiver is used. The line should be terminated as shown in Figure 24. This method not only provides high speed, board-to-board clock distribution, but also provides system noise margin advantages. Since the line receiver operates independently of the V_{BB} reference voltage (differential inputs) the noise margin from board to board is also independent of temperature differentials.

LOGIC SHORTCUTS

MECL circuitry offers several logic design conveniences. Among these are:

1. **Wire-OR** (can be produced by wiring MECL output emitters together outside packages).

2. **Complementary Logic Outputs** (both OR and NOR are brought out to package pins in most cases).

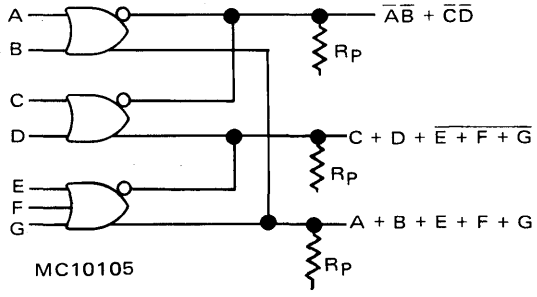
An example of the use of these two features to reduce gate and package count is shown in Figure 28.

The connection shown saves several gate circuits over performing the same functions with non-ECL type logic. Also, the logic functions in Figure 29 are all accomplished with one gate propagation delay time for best system speed. Wire-ORing permits direct connections of MECL circuits to busses. (MECL System Design Handbook and Application Note AN-726).

Propagation delay is increased approximately 50 ps per wire-OR connection. In general, wire-OR should be limited to 6 MECL outputs to maintain a proper LOW logic level. The MC10123 is an exception to this rule because it has a special V_{OL} level that allows very high fanout on a bus or wire-OR line. The use of a single output pull-down resistor is recommended per wire-OR, to economize on power dissipation. However, two pull-down resistors per wired-OR can improve fall times and be used for double termination of busses.

Wire-OR should be done between gates in a package or nearby packages to avoid spikes due to line propagation delay. This does not apply to bus lines which activate only one driver at a time.

FIGURE 28 — USE OF WIRE-OR AND COMPLEMENTARY OUTPUTS



SYSTEM CONSIDERATIONS — A SUMMARY OF RECOMMENDATIONS

	MECL 10KH	MECL 10K	MECL III
Power Supply Regulation	±5%①	10%②	10%②
On-Card Temperature Gradient	20°C	Less Than 25°C	Less Than 25°C
Maximum Non-Transmission Line Length (No Damping Resistor)	4″	8″	1″
Unused Inputs	Leave Open③	Leave Open③	Leave Open③
PC Board	Standard 2-Sided or Multilayer	Standard 2-Sided or Multilayer	Multilayer
Cooling Requirements	500 lfpm Air	500 lfpm Air	500 lfpm Air
Bus Connection Capability	Yes (Wire-OR)	Yes (Wire-OR)	Yes (Wire-OR)
MSI/LSI Parts	Yes	Yes	Yes (MSI)
Maximum Twisted Pair Length (Differential Drive)	Limited By Cable Response Only, Usually >1000′	Limited by Cable Response Only, Usually >1000′	Limited by Cable Response Only, Usually >1000′
The Ground Plane to Occupy Percent Area of Card	>75%	>50%	>75%
Wire Wrap may be used	Yes	Yes	Not Recommended
Compatible with MECL 10,000	Yes	—	Yes

① All dc and ac parameters guaranteed for $V_{EE} = -5.2\ V \pm 5\%$.

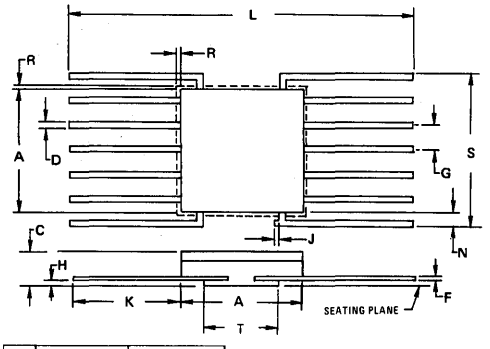
② At the devices (functional only).

③ Except special functions without input pull-down resistors.

PACKAGE OUTLINE DIMENSIONS

A letter suffix to the MECL logic function part number is used to specify the package style (see drawings below). See appropriate selector guide for specific packaging available for a given device type.

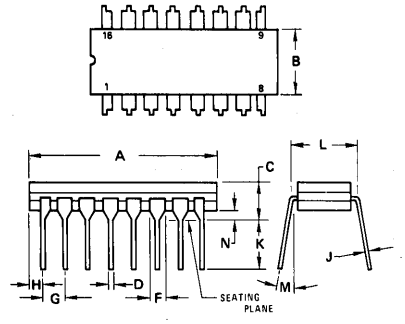
F SUFFIX
CERAMIC PACKAGE
CASE 607-04



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	6.10	6.99	0.240	0.275
C	0.76	2.03	0.030	0.070
D	0.25	0.48	0.010	0.019
F	0.08	0.15	0.003	0.006
G	1.27 BSC		0.050 BSC	
H	0.13	0.89	0.005	0.035
J	–	0.38	–	0.015
K	6.35	–	0.250	–
L	18.80	–	0.740	–
N	0.25	–	0.010	–
R	–	0.38	–	0.015
S	7.62	8.38	0.300	0.330
T	4.45	4.95	0.175	0.195

NOTES:
1. ALL NOTES ASSOCIATED WITH TO-86 OUTLINE SHALL APPLY.
2. LEADS WITHIN 0.13 mm (0.005) TOTAL OF TRUE POSITION RELATIVE TO "A" AT MAXIMUM MATERIAL CONDITION.

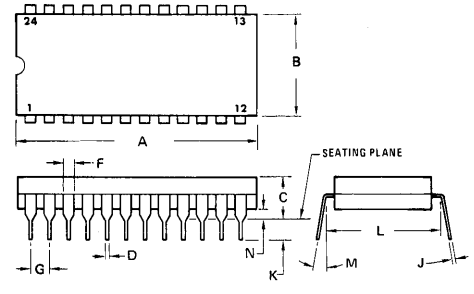
L SUFFIX
CERAMIC PACKAGE
CASE 620-02



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	19.05	19.81	0.750	0.780
B	6.22	6.98	0.245	0.275
C	4.06	5.08	0.160	0.200
D	0.38	0.51	0.015	0.020
F	1.40	1.65	0.055	0.065
G	2.54 BSC		0.100 BSC	
H	0.51	1.14	0.020	0.045
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	7.37	7.87	0.290	0.310
M	–	15°	–	15°
N	0.51	1.02	0.020	0.040

NOTES:
1 LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION
2 PKG. INDEX: NOTCH IN LEAD NOTCH IN CERAMIC OR INK DOT
3 DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL

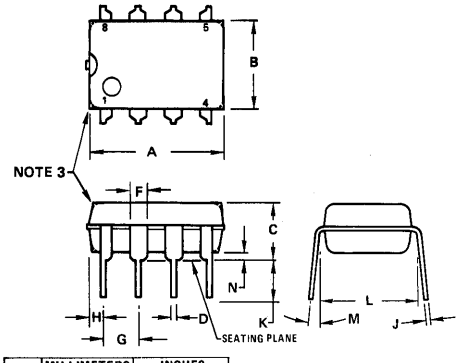
L SUFFIX
CERAMIC PACKAGE
CASE 623-05



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	31.24	32.77	1.230	1.290
B	12.70	15.49	0.500	0.610
C	4.06	5.59	0.160	0.220
D	0.41	0.51	0.016	0.020
F	1.27	1.52	0.050	0.060
G	2.54 BSC		0.100 BSC	
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.27	0.020	0.050

NOTES:
1. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
2. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION. (WHEN FORMED PARALLEL).

P SUFFIX
PLASTIC PACKAGE
CASE 626-04

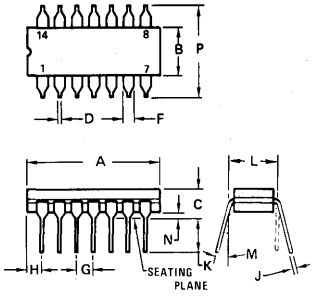


DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	9.40	10.16	0.370	0.400
B	6.10	6.60	0.240	0.260
C	3.94	4.45	0.155	0.175
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	0.76	1.27	0.030	0.050
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	–	10°	–	10°
N	0.51	0.76	0.020	0.030

NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. PACKAGE CONTOUR OPTIONAL (ROUND OR SQUARE CORNERS)

PACKAGE OUTLINE DIMENSIONS (continued)

L SUFFIX
CERAMIC PACKAGE
CASE 632-02

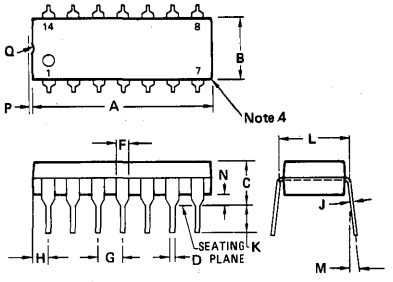


DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	16.8	19.9	0.660	0.785
B	5.59	7.11	0.220	0.280
C	–	5.08	–	0.200
D	0.381	0.584	0.015	0.023
F	0.77	1.77	0.030	0.070
G	2.54 BSC		0.100 BSC	
J	0.203	0.381	0.008	0.015
K	2.54	–	0.100	–
L	7.62 BSC		0.300 BSC	
M	–	15°	–	15°
N	0.51	0.76	0.020	0.030
P	–	8.25	–	0.325

All JEDEC dimensions and notes apply.

NOTES:
1. ALL RULES AND NOTES ASSOCIATED WITH MO-001 AA OUTLINE SHALL APPLY.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. LEADS WITHIN 0.25mm (0.010) DIA OF TRUE POSITION AT SEATING PLANE AND MAXIMUM MATERIAL CONDITION.

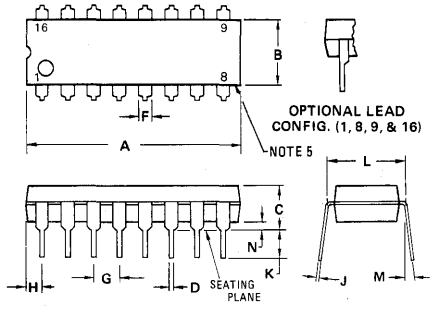
P SUFFIX
PLASTIC PACKAGE
CASE 646-05



DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	18.16	19.56	0.715	0.770
B	6.10	6.60	0.240	0.260
C	4.06	5.08	0.160	0.200
D	0.38	0.53	0.015	0.021
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	1.32	2.41	0.052	0.095
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0°	10°	0°	10°
N	0.51	1.02	0.020	0.040

NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
4. ROUNDED CORNERS OPTIONAL.

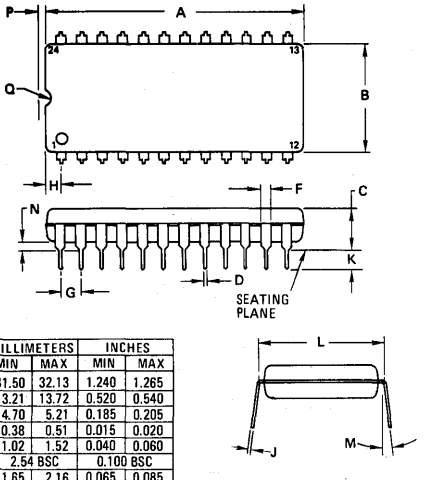
P SUFFIX
PLASTIC PACKAGE
CASE 648-05



DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	18.80	21.34	0.740	0.840
B	6.10	6.60	0.240	0.260
C	4.06	5.08	0.160	0.200
D	0.38	0.53	0.015	0.021
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	0.38	2.41	0.015	0.095
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0°	10°	0°	10°
N	0.51	1.02	0.020	0.040

NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
4. "F" DIMENSION IS FOR FULL LEADS. "HALF" LEADS ARE OPTIONAL AT LEAD POSITIONS 1, 8, 9, and 16).
5. ROUNDED CORNERS OPTIONAL.

P SUFFIX
PLASTIC PACKAGE
CASE 649-03

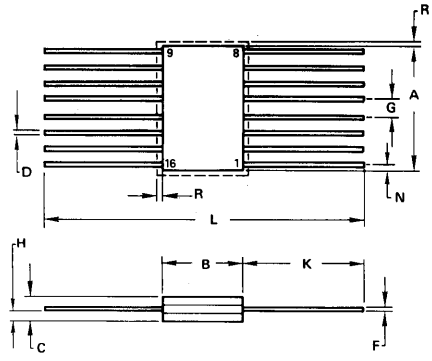


DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	31.50	32.13	1.240	1.265
B	13.21	13.72	0.520	0.540
C	4.70	5.21	0.185	0.205
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	14.99	15.49	0.590	0.610
M	–	10°	–	10°
N	0.51	1.02	0.020	0.040
P	0.13	0.38	0.005	0.015
Q	0.51	0.76	0.020	0.030

NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.

PACKAGE OUTLINE DIMENSIONS (continued)

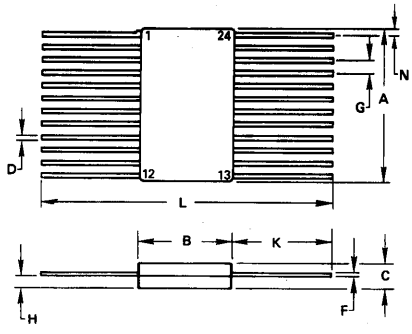
F SUFFIX
CERAMIC PACKAGE
CASE 650-03



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	9.40	10.16	0.370	0.400
B	6.22	7.24	0.245	0.285
C	1.52	2.03	0.060	0.080
D	0.41	0.48	0.016	0.019
F	0.08	0.15	0.003	0.006
G	1.27 BSC		0.050 BSC	
H	0.64	0.89	0.025	0.035
K	6.35	9.40	0.250	0.370
L	18.92	–	0.745	–
N	–	0.51	–	0.020
R	–	0.38	–	0.015

NOTES:
1. LEAD NO. 1 IDENTIFIED BY TAB ON LEAD OR DOT ON COVER.
2. LEADS WITHIN 0.13 mm (0.005) TOTAL OF TRUE POSITION AT MAXIMUM MATERIAL CONDITION.

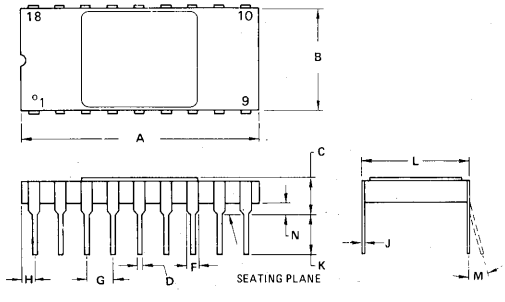
F SUFFIX
CERAMIC PACKAGE
CASE 652-02



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.99	15.49	0.590	0.610
B	9.27	9.91	0.365	0.390
C	1.27	2.03	0.050	0.080
D	0.38	0.48	0.015	0.019
F	0.08	0.15	0.003	0.006
G	1.27 BSC		0.050 BSC	
H	0.69	1.02	0.027	0.040
K	6.35	9.40	0.250	0.370
L	21.97	–	0.865	–
N	0.25	0.63	0.010	0.025

NOTES:
1. LEADS WITHIN 0.25 mm (0.010) TOTAL OF TRUE POSITION AT MAXIMUM MATERIAL CONDITION.

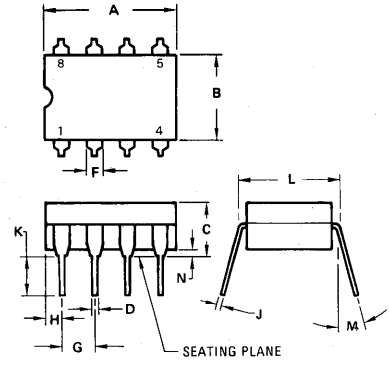
L SUFFIX
SIDE BRAISED
CERAMIC PACKAGE
CASE 680-06



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	22.48	23.24	0.885	0.915
B	7.16	7.75	0.282	0.305
C	3.18	4.27	0.125	0.168
D	0.38	0.58	0.015	0.023
F	0.76	1.52	0.030	0.060
G	2.54 BSC		0.100 BSC	
H	1.02	1.52	0.040	0.060
J	0.20	0.30	0.008	0.012
K	2.68	4.44	0.105	0.175
L	7.37	7.87	0.290	0.310
M	–	10°	–	10°
N	0.38	1.40	0.015	0.055

NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RAD OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.

L SUFFIX
CERAMIC PACKAGE
CASE 693-02

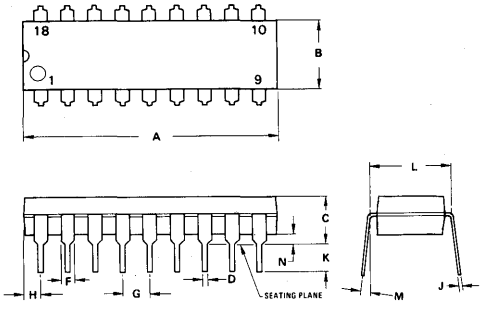


DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	9.91	10.92	0.390	0.430
B	6.22	6.99	0.245	0.275
C	4.32	5.08	0.170	0.200
D	0.41	0.51	0.016	0.020
F	1.40	1.65	0.055	0.065
G	2.54 BSC		0.100 BSC	
H	1.14	1.65	0.045	0.065
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	7.37	7.87	0.290	0.310
M	–	15°	–	15°
N	0.51	1.02	0.020	0.040

NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RAD OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.

PACKAGE OUTLINE DIMENSIONS (continued)

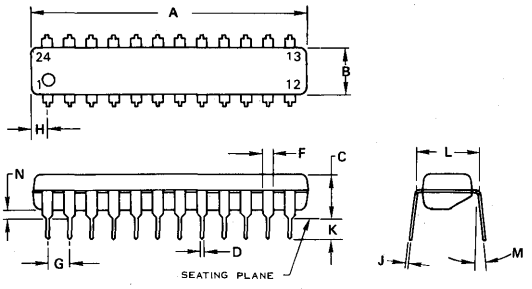
P SUFFIX
PLASTIC PACKAGE
CASE 707-02



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	22.22	23.24	0.875	0.915
B	6.10	6.60	0.240	0.260
C	3.56	4.57	0.140	0.180
D	0.36	0.56	0.014	0.022
F	1.27	1.78	0.050	0.070
G	2.54 BSC		0.100 BSC	
H	1.02	1.52	0.040	0.060
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25mm(0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

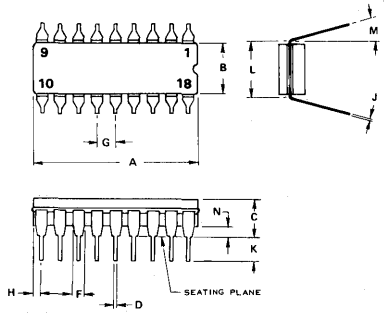
P SUFFIX
PLASTIC PACKAGE
CASE 724-02



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	31.24	32.13	1.230	1.265
B	6.35	6.86	0.250	0.270
C	4.06	4.57	0.160	0.180
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.60	2.11	0.063	0.083
J	0.18	0.30	0.007	0.012
K	2.92	3.43	0.115	0.135
L	7.37	7.87	0.290	0.310
M	–	10°	–	10°
N	0.51	1.02	0.020	0.040

NOTE:
1. LEADS, TRUE POSITIONED WITHIN 0.25 mm (0.010) DIA AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION (DIM D).

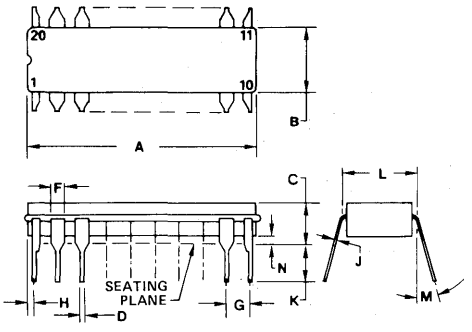
L SUFFIX
CERAMIC PACKAGE
CASE 726-04



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	22.35	23.11	0.880	0.910
B	6.10	7.49	0.240	0.295
C	–	5.08	–	0.200
D	0.38	0.53	0.015	0.021
F	1.40	1.78	0.055	0.070
G	2.54 BSC		0.100 BSC	
H	0.51	1.14	0.020	0.045
J	0.20	0.30	0.008	0.012
K	3.18	4.32	0.125	0.170
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

NOTES:
1. LEADS, TRUE POSITIONED WITHIN 0.25 mm (0.010) DIA. AT SEATING PLANE, AT MAXIMUM MATERIAL CONDITION.
2. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIM "A" & "B" INCLUDES MENISCUS.

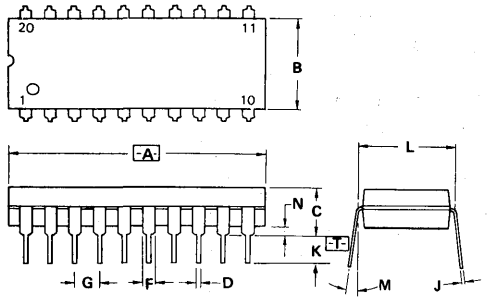
L SUFFIX
CERAMIC PACKAGE
CASE 732-03



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	23.88	25.15	0.940	0.990
B	6.60	7.49	0.260	0.295
C	3.81	5.08	0.150	0.200
D	0.38	0.56	0.015	0.022
F	1.40	1.65	0.055	0.065
G	2.54 BSC		0.100 BSC	
H	0.51	1.27	0.020	0.050
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.25	1.02	0.010	0.040

NOTES:
1. LEADS WITHIN 0.25 mm (0.010) DIA., TRUE POSITION AT SEATING PLANE, AT MAXIMUM MATERIAL CONDITION.
2. DIM L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIM A AND B INCLUDES MENISCUS.

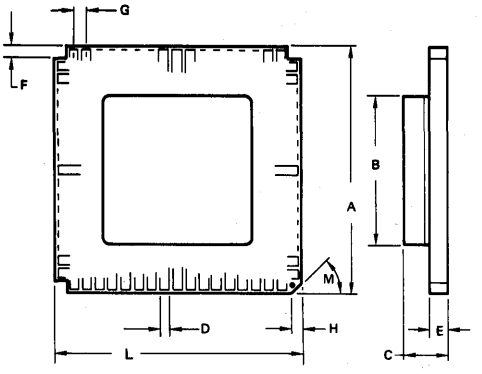
P SUFFIX
PLASTIC PACKAGE
CASE 738-02



DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	25.65	27.18	1.010	1.070
B	6.10	6.60	0.240	0.260
C	3.94	4.57	0.155	0.180
D	0.38	0.56	0.015	0.022
F	1.27	1.78	0.050	0.070
G	2.54 BSC		0.100 BSC	
J	0.20	0.38	0.008	0.015
K	2.79	3.56	0.110	0.140
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

NOTES:
1. DIM -A- IS DATUM.
2. POSITIONAL TOL FOR LEADS:
   ⌖ ⌀ 0.25 (0.010) Ⓜ T A Ⓜ
3. -T- IS SEATING PLANE.
4. DIM "B" DOES NOT INCLUDE MOLD FLASH.
5. DIM -L- TO CENTER OF LEADS WHEN FORMED PARALLEL.
6. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

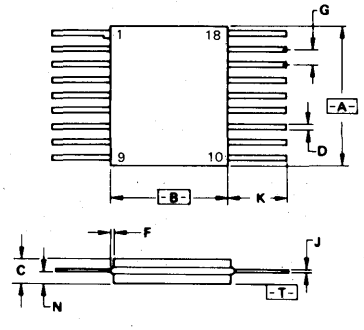
Z SUFFIX
CERAMIC PACKAGE
CASE 745-01



DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	24.00	24.51	0.945	0.965
B	14.22	14.73	0.560	0.580
C	–	4.57	–	0.180
D	0.84	0.99	0.033	0.039
E	1.27	1.78	0.050	0.070
F	1.14	1.40	0.045	0.055
G	1.27 BSC		0.050 BSC	
H	0.89	1.14	0.035	0.045
L	24.00	24.51	0.945	0.965
M	45° NOM		45° NOM	

NOTES:
1. DIMENSIONS A AND L ARE DATUMS.
2. POSITIONAL TOLERANCES FOR COVER:
   ⌖ 0.25 (0.010) Ⓜ A Ⓜ L Ⓜ
3. DIMENSION D – 68 PLACES
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

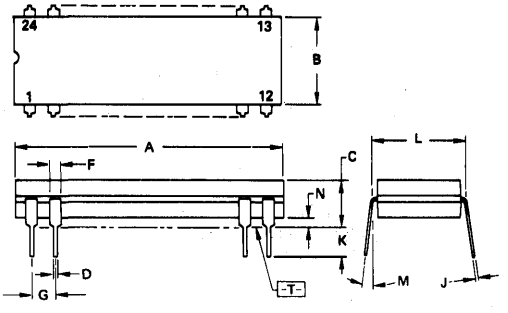
F SUFFIX
CERAMIC PACKAGE
CASE 747-01



DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	–	11.43	–	0.450
B	9.14	9.91	0.360	0.390
C	1.52	2.03	0.060	0.080
D	0.41	0.46	0.016	0.018
F	–	0.25	–	0.010
G	1.27 BSC		0.050 BSC	
J	0.10	0.15	0.004	0.006
K	–	7.75	–	0.305
N	–	0.89	–	0.035

NOTES:
1. -A-, -B-, AND -T- ARE DATUMS.
2. -T- IS SEATING PLANE.
3. LEADS POSITIONAL TOLERANCE.
   ⌖ 0.13 (0.005) Ⓜ T A Ⓜ B Ⓜ
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

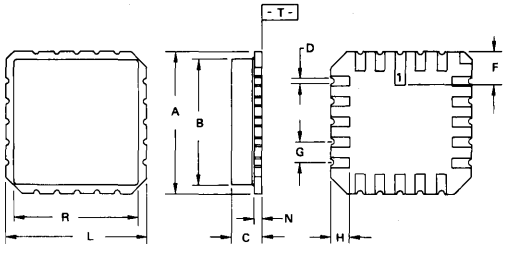
L SUFFIX
CERAMIC PACKAGE
CASE 748-01



NOTES:
1. DIMENSIONS -A- AND -B- ARE DATUM.
2. POSITIONAL TOLERANCES FOR LEADS:
   Ⓘ ⌀ 0.25 (0.010) Ⓜ T A Ⓜ B Ⓜ
3. -T- IS SEATING PLANE.
4. DIMENSIONS A AND B INCLUDE MENISCUS.
5. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
6. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	29.21	31.75	1.150	1.250
B	9.40	10.16	0.370	0.400
C	–	5.72	–	0.225
D	0.38	0.56	0.015	0.022
F	1.27	1.65	0.050	0.065
G	2.54 BSC		0.100 BSC	
J	0.20	0.30	0.008	0.012
K	2.54	4.32	0.100	0.170
L	10.16 BSC		0.400 BSC	
M	0°	15°	0°	15°
N	0.51	1.27	0.020	0.050

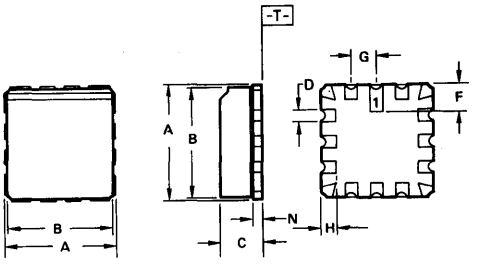
Z SUFFIX
CERAMIC PACKAGE
CASE 756-01



	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	8.64	9.14	0.340	0.360
B	7.75	8.00	0.305	0.315
C	—	2.54	—	0.100
D	0.31	0.51	0.012	0.020
F	1.91	2.41	0.075	0.095
G	1.27 BSC		0.050 BSC	
H	1.14	1.39	0.045	0.055
L	8.64	9.14	0.340	0.360
N	0.46	0.71	0.018	0.028
R	7.75	8.00	0.305	0.315

NOTES:
1. DIMENSIONS A AND L ARE DATUMS.
2. -T- IS GAUGE PLANE.
3. POSITIONAL TOLERANCE FOR TERMINALS (D): 20 PLACES
   ⌖ 0.25 (0.010) Ⓜ T A Ⓜ L Ⓜ
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

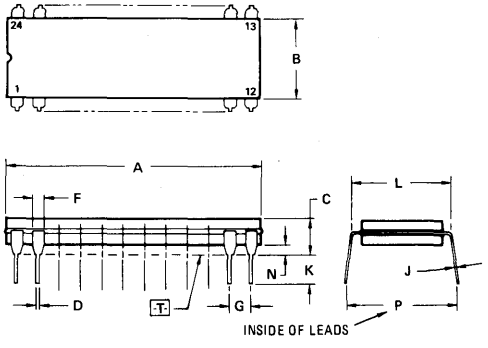
ZA SUFFIX
CERAMIC PACKAGE
CASE 757-01



	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.32	4.82	0.170	0.190
B	4.24	4.72	0.167	0.186
C	2.03	2.28	0.060	0.085
D	0.30	0.51	0.012	0.020
F	1.02	1.27	0.040	0.050
G	1.02 BSC		0.040 BSC	
H	0.51	0.76	0.020	0.030
N	0.25	0.51	0.010	0.020

NOTES:
1. DIMENSIONS A AND B ARE DATUMS.
2. -T- IS GAUGE PLANE.
3. POSITIONAL TOLERANCE FOR TERMINALS (D): 16 PLACES
   ⌖ 0.25 (0.010) Ⓜ T Ⓢ A Ⓢ B Ⓢ
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

L SUFFIX
CERAMIC PACKAGE
CASE 758-01



	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	31.50	32.64	1.240	1.285
B	7.24	7.75	0.285	0.305
C	3.68	4.44	0.145	0.175
D	0.38	0.53	0.015	0.021
F	1.14	1.57	0.045	0.062
G	2.54 BSC		0.100 BSC	
J	0.20	0.33	0.008	0.013
K	2.54	4.19	0.100	0.165
L	7.62	7.87	0.300	0.310
N	0.51	1.27	0.020	0.050
P	9.14	10.16	0.360	0.400

NOTES:
1. DIMENSION A IS DATUM.
2. POSITIONAL TOLERANCE FOR LEADS: 24 PLACES
   ⌖ 0.25 (0.010) Ⓜ T A Ⓜ
3. -T- IS SEATING PLANE.
4. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

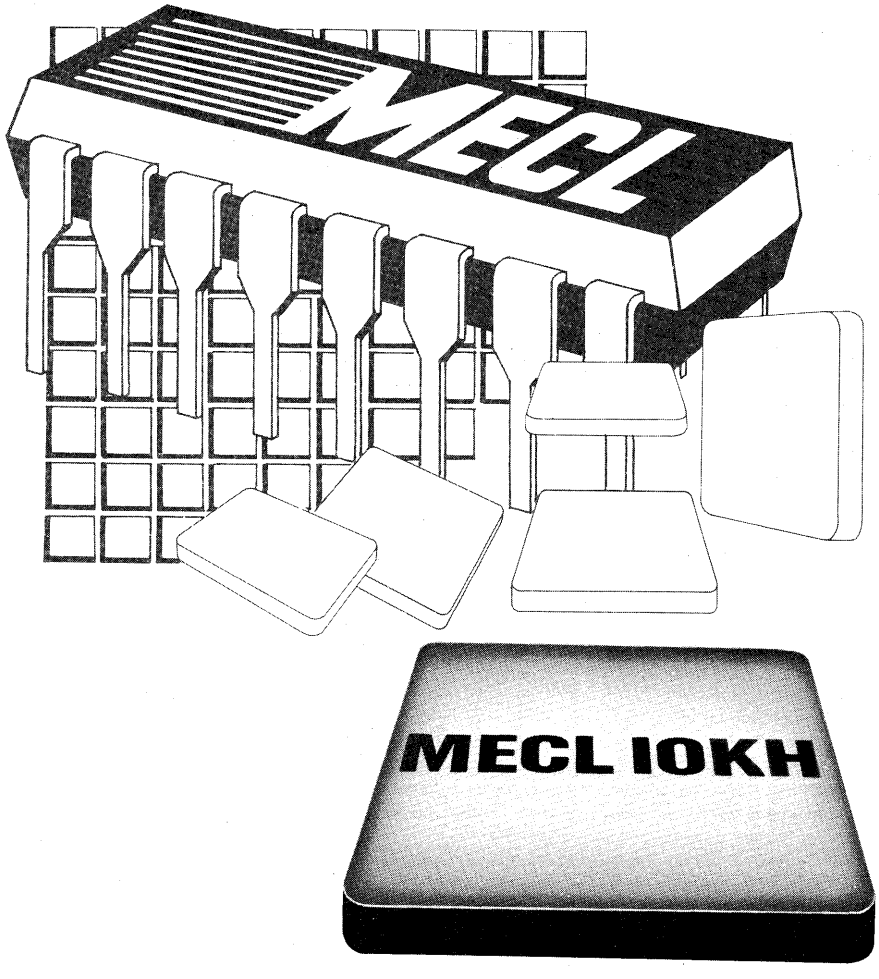
SUPPLEMENTARY LITERATURE

1. "Improve Fast-Logic Designs," by Bill Blood, Electronic Design, May 10, 1973.
2. "Interface TTL Systems with ECL Circuits," by George Adams, EDN, September 5, 1973.
3. "Increasing Minicomputer Speed with Emitter-Coupled Logic," by Jon De Laune, Computer Design, February 1974.
4. "An Engineering Comparison Study MECL 10,000 and Schottky TTL," Motorola Inc., 1974.
5. "ECL Circuits Drive Light-Emitting Diodes," by Bill Blood, EDN, January 20, 1974.
6. "Four-Digit BCD Programmability Featured in Variable Modulus 60 MHz Counter," by Tom Balph and Bill Blood, Electronic Design, March 15, 1974.
7. "Build a Low Cost ECL Logic Probe," by Tom Balph, Electronic Design, August 16, 1974.
8. "A CAD Program for High Speed Logic Element Interconnections," by Thomas Balph, William Blood, and Jerry Prioste, Computer Design, May 1975.
9. "Build a Clock Bias Circuit for ECL Flip-Flops," by T. Balph and H. Gnauden, EDN, May 5, 1975.
10. "Get the Best Processor Performance by Building It From ECL Bit Slices," By Tom Balph and Bill Blood, Electronic Design, June 7, 1977.
11. "MECL System Design Handbook," by Bill Blood, Motorola Inc.

APPLICATION NOTES

Copies of these Application Notes and Engineering Bulletins can be obtained from your Motorola representative or authorized distributor, or from Technical Information Center, Motorola Semiconductor Products Inc., P.O. Box 20912, Phoenix, Arizona 85036.

AN-270 Nanosecond Pulse Handling Techniques
AN-504 The MC1600 Series MECL III Gates
AN-535 Phase-Locked Loop Design Fundamentals
AN-553 A New Generation of Integrated Avionic Synthesizers
AN-556 Interconnection Techniques for Motorola's MECL 10K Series Emitter Coupled Logic
AN-565 Using Shift Registers as Pulse Delay Networks
AN-567 MECL Positive and Negative Logic
AN-579 Testing MECL 10K Integrated Logic Circuits
AN-581 An MSI 500 MHz Frequency Counter Using MECL and TTL
AN-586 Measure Frequency and Propagation Delay with High Speed MECL Circuits
AN-592 AC Noise Immunity of MECL 10K Integrated Circuits
AN-700 Simulate MECL System Interconnections with a Computer Program
AN-701 Understanding MECL 10K DC and AC Data Sheet Specifications
AN-709 MECL 10k Arithmetic Elements, MC10179, MC10180, MC10181
AN-720 Interfacing with MECL 10K Integrated Circuits
AN-726 Bussing with MECL 10K Integrated Circuits
AN-730 A High-Speed FIFO Memory Using the MECL MCM10143 Register File
AN-742 A 200 MHz Autroranging MECL-McMOS Frequency Counter
AN-774 A Simple High Speed Bipolar Microprocessor Illustrates System Design and Microprogram Techniques
AN-827 Technique of Direct Programming Using Two-Modulus Prescaler
EB-47 Event Counter and Storage Latches for High Frequency, High Resolution Counters
EB-48 A Time Base and Control Logic Subsystem for High Frequency, High Resolution Counters

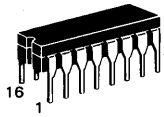

MECL
MECL 10KH

MECL 10KH
INTEGRATED CIRCUITS

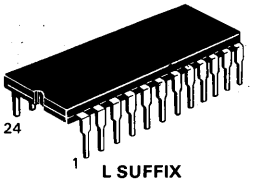
MC10H100 Series
0 to 75°C

2

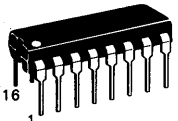
Standard Packages



L SUFFIX
CERAMIC PACKAGE
CASE 620

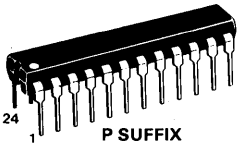


L SUFFIX
CERAMIC PACKAGE
CASE 623

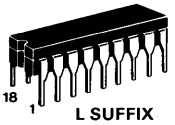


P SUFFIX
PLASTIC PACKAGE
CASE 648

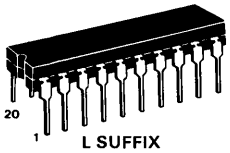
P SUFFIX
PLASTIC PACKAGE
CASE 707



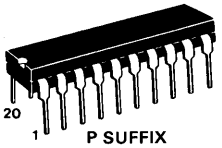
P SUFFIX
PLASTIC PACKAGE
CASE 724



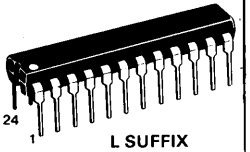
L SUFFIX
CERAMIC PACKAGE
CASE 726



L SUFFIX
CERAMIC PACKAGE
CASE 732

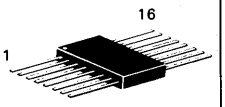


P SUFFIX
PLASTIC PACKAGE
CASE 738

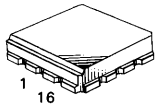


L SUFFIX
CERAMIC PACKAGE
CASE 758

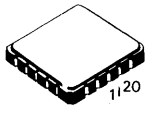
Special Packages



F SUFFIX
CERAMIC PACKAGE
CASE 650



ZA SUFFIX
CERAMIC PACKAGE
CASE 757



Z SUFFIX
CERAMIC PACKAGE
CASE 756

Function Selection—(0 to +75°C)

Function	Device	Case
NOR Gate		
Quad-2-Input with Strobe	MC10H100	620, 648
Quad-2-Input	MC10H102	620, 648
Triple 4-3-3 Input	MC10H106	620, 648
Dual 3-Input 3-Output	MC10H211	620, 648
OR Gate		
Quad 2-Input	MC10H103	620, 648
Dual 3-Input 3-Output	MC10H210	620, 648
AND Gates		
Quad AND	MC10H104	620, 648
Complex Gates		
Quad OR/NOR	MC10H101	620, 648
Triple 2-3-2 Input OR/NOR	MC10H105	620, 648
Triple Exclusive OR/NOR	MC10H107	620, 648
Dual 4-5 Input OR/NOR	MC10H109	620, 648
Quad Exclusive OR	MC10H113	620, 648
Dual 2-Wide OR-AND/OR-AND INVERT	MC10H117	620, 648
Dual 2-Wide 3-Input OR/AND	MC10H118	620, 648
4-Wide 4-3-3-3 Input OR-AND	MC10H119	620, 648
4-Wide OR-AND/OR-AND INVERT	MC10H121	620, 648
Hex Buffer w/Enable	MC10H188	620, 648
Hex Inverter w/Enable	MC10H189	620, 648

Function	Device	Case
Translators		
Quad TTL to MECL	MC10H124	620, 648
Quad MECL TO TTL	MC10H125	620, 648
Quad MECL-to-TTL Translator, Single Power Supply (-5.2 V or +5.0 V)	MC10H350	620, 648
Quad TTL to MECL, ECL Strobe	MC10H424	620, 648
Receivers		
Quad Line Receiver	MC10H115	620, 648
Triple Line Receiver	MC10H116	620, 648
Flip-Flop Latches		
Dual D Master Slave Flip-Flop	MC10H131	620, 648
Dual J-K Master Slave Flip-Flop	MC10H135	620, 648
Hex D Flip-Flop	MC10H176	620, 648
Dual D Latch	MC10H130	620, 648
Quint Latch	MC10H175	620, 648
Hex D Flip-Flop w/Common Reset	MC10H186A	620, 648
Parity Checker		
12-Bit Parity Generator-Checker	MC10H160	620, 648

Function	Device	Case
Encoders Decoders		
Binary to 1-8 (Low)	MC10H161	620, 648
Binary to 1-8 (High)	MC10H162	620, 648
Dual Binary to 1-4 (Low)	MC10H171	620, 648
Dual Binary to 1-4 (High)	MC10H172	620, 648
8-Input Priority Encoder	MC10H165	620, 648
Data Selector Multiplexer		
Quad Bus Driver/Receiver with 2-to-1 Output Multiplexers	MC10H330	758, 724
Dual Bus Driver/Receiver with 4-to-1 Output Multiplexers	MC10H332	732, 738
Quad 2-Input Multiplexers (Noninverting)	MC10H158	620, 648
Quad 2-Input Multiplexers (Inverting)	MC10H159	620, 648
8-Line Multiplexer	MC10H164	620, 648
Quad 2-Input Multiplexer Latch	MC10H173	620, 648
Dual 4-1 Multiplexer	MC10H174	620, 648
Counters		
Universal Hexadecimal	MC10H136	620, 648
Binary Counter	MC10H016	620, 648
Arithmetic Functions		
Look Ahead Carry Block	MC10H179	620, 648
Dual High Speed Adder/ Subtractor	MC10H180	620, 648
4-Bit ALU	MC10H181	623, 649 724, 758

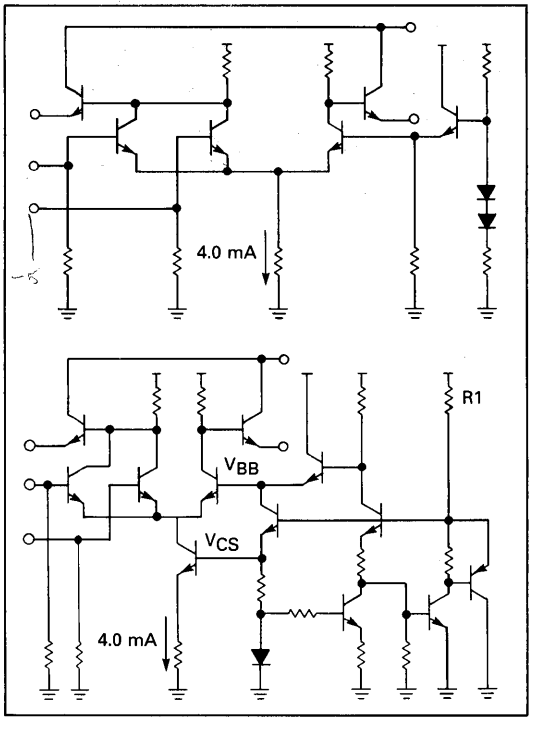
Function	Device	Case
Special Function		
4-Bit Universal Shift Register	MC10H141	620, 648
16 × 4 Bit Register File	MC10H145	620, 648
5-Bit Magnitude Comparator	MC10H166	620, 648
Quad Bus Driver/Receiver with Transmit and Receiver Latches	MC10H334	732, 738
Memories		
16 × 4 Bit Register File	MC10H145	620, 648
8 × 2 Bit Content Addressable Memory	MC10H155	707, 726
Bus Driver (25 ohm outputs)		
Triple 4-3-3 Input Bus Driver (25 Ohms)	MC10H123	620, 648
Quad Bus Driver/Receiver with 2-to-1 Output Multiplexers	MC10H330	724, 758
Dual Bus Driver/Receiver with 4-to-1 Output Multiplexers	MC10H332	732, 738
Quad Bus Driver/Receiver with Transmit and Receiver Latches	MC10H334	732, 738
Triple 3-Input Bus Driver with Enable (25 Ohm)	MC10H423	620, 648
OR/NOR Gate		
Dual 4-5-Input OR/NOR Gate	MC10H209	620, 648

MECL 10KH INTRODUCTION

2

Motorola's new MECL 10KH family features 100% improvement in propagation delay and clock speeds while maintaining power supply current equal to MECL 10K. This new MECL family is voltage compensated which allows guaranteed dc and switching parameters over a ±5% power supply range. Noise margins of MECL 10KH are 75% better than the MECL 10K series over the ±5% power supply range. MECL 10KH is compatible with MECL 10K and MECL III, a key element in allowing users to enhance existing systems by increasing the speed in critical timing areas. Also, many MECL 10KH devices are pinout/functional duplications of the MECL 10K series devices.

FIGURE 1 — MECL 10K versus MECL 10KH GATE DESIGN



The schematics in Figure 1 compare the basic gate structure of the MECL 10KH to that of MECL 10K devices. The gate switch current is established with a current source in the MECL 10KH family as compared to a resistor source in MECL 10K. The bias generator in the MECL 10K device has been replaced with a voltage regulator in the MECL 10KH series. The advantages of these design changes are: current-sources permit-matched collector resistors that yield correspondingly better matched delays, less variation in the output-voltage level with power supply changes, and matched output-tracking rates with temperature. These circuit changes increase complexity at the gate level; however, the added performance more than compensates.

The MECL 10KH family is being fabricated using Motorola's MOSAIC I (Motorola Oxide Self Aligned Implanted Circuits). The switching transistor's geometries obtained in the MOSAIC I process show a two-fold improvement in f_T, a reduction of more than 50% in parasitic capacitance and a decrease in device area of almost 76%.

FIGURE 2 — MOSAIC versus MECL 10K SWITCHING TRANSISTOR GEOMETRY

With improved geometry, the MECL 10KH switching transistors (left) are one-seventh the size of the older MECL 10K transistors (right). Along with the smaller area comes an improved f_T and reduced parasitic capacitances.

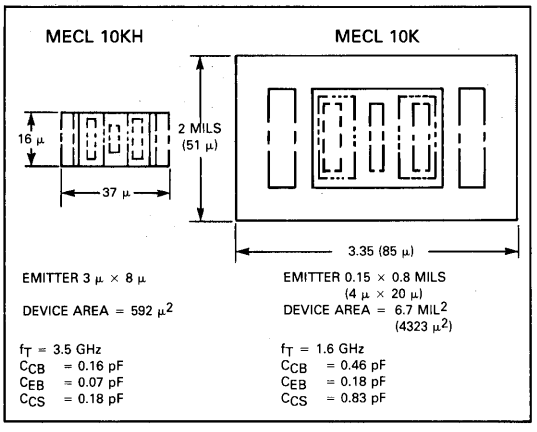


Figure 2 illustrates the relative size difference between the junction isolated transistor of MECL 10K and the MOSAIC I transistor of MECL 10KH. This suggests that performance could be improved twofold at lower power levels. However, at the gate level, the power of the output transistor cannot be reduced without sacrificing output characteristics because of the 50 ohm drive requirements of MECL. In more complex functions, where part of the delay is associated with internal gates, MECL 10KH devices use less power than the equivalent MECL 10K devices and provide an even more significant improvement in ac performance.

Table 1. — TYPICAL FAMILY CHARACTERISTICS FOR 10K AND 10KH CIRCUITS

	10K	10KH
Propagation delay (ns)	2.0	1.0
Power (mW)	25	25
Power-speed product (pJ)	50	25
Rise/fall times (ns) (20–80%)	2.0	1.5
Temperature range (°C)	−30 to +85	0 to +75
Voltage regulated	No	Yes
Technology	Junction isolated	Oxide isolated
V_{EE} = −5.2 V		

Supply & Temperature Variation

MECL 10KH temperature and voltage compensation is designed to guarantee compatibility with MECL 10K, MECL III, MECL Memories and the MC10900 and Macrocell Array products. Table 1 summarizes some performance characteristics of the MECL 10K and 10KH logic families in a 16-pin DIP. The MECL 10KH devices offer typical propagation delays of 1.0 ns at 25 mW per gate when operated from a V_{EE} of −5.2 V. The resulting speed-power product of 25 picojoules is the best of any ECL logic family available today.

The operating temperature range is changed from −30°C to +85°C of the MECL 10K family to the narrower range of 0°C to 75°C for MECL 10KH. This change matches the constraints established by the memory and array products. Operation at −30°C would require compromises in performance and power. With few exceptions, commercial applications are satisfied by 0°C min.

Table 2. — MECL 10KH AC SPECIFICATIONS AND TRACKING

Parameter	0°C Min	0°C Typ	0°C Max	25°C Min	25°C Typ	25°C Max	75°C Min	75°C Typ	75°C Max	Units
t_{PD}	0.7	1.1	1.6	0.7	1.0	1.5	0.7	1.1	1.7	ns
	Min		Max	Min		Max	Min		Max	
t_R (20–80%)	0.8		2.2	0.7		2.0	0.8		2.2	ns
t_F (20–80%)	0.8		2.2	0.7		2.0	0.8		2.2	ns

V_{EE} = −5.2 V ±5%

Parameter		Propagation delay (ns)* Typ	Propagation delay (ns)* Max	Delay variation vs temp (ps/°C) Typ	Delay variation vs temp (ps/°C) Max	Delay variation vs supply (ps/V) Typ	Delay variation vs supply (ps/V) Max
t_{PD}	10K	2.0	2.9	2.0	7.0	80	
	10KH	1.0	1.5	0.5	4.0	0	0

*V_{EE} = −5.2 V, Temp = 25°C

AC specifications of MECL 10KH products appear in Table 2. In the MECL 10KH family, all ac specifications have guaranteed minimums and maximums for extremes of both temperature and supply — a first in ECL logic. In addition, flip flops, latches and counters will have guaranteed limits for setup time, hold time, and clock pulse width. The limits in Table 2 are guaranteed for a power supply variation of ±5%. MECL 10K typically has a propagation delay (t_{PD}) variation of 80 ps/V with no guaranteed maximum. The typical variation in t_{PD} for MECL 10KH circuits is only 38 ps typically over the entire specified temperature range and power-supply tolerance, and is guaranteed not to exceed 300 ps.

The improved performance in temperature over MECL 10K are a result of the internal voltage regulator. The primary difference being the flatter tracking rate of the output "0" level voltage (V_{OL}). This difference does not affect the compatibility with existing MECL families.

Changes in output "1" level voltages (V_{OH}) with supply variations are 10 mV/V less for the MECL 10KH family. V_{OH} varies with the supply, primarily because of changes in chip temperature caused by the changes in power dissipation. However, the current in the MECL 10KH circuits remains almost constant with supply changes, since the circuits are voltage compensated and use current sources for all internal emitter followers. Threshold voltage (V_{BB}) and output "0" level voltage (V_{OL}) variations are shown with respect to MECL 10K in Table 3. In both cases voltage compensation has reduced the variations significantly.

Table 3. — LOGIC LEVEL DC TRACKING RATE FOR 10K AND 10KH CIRCUITS

		Min	Typ	Max
$\Delta V_{OH}/\Delta T$ (mV/°C)	10KH	1.2	1.3	1.5
	10K	1.2	1.3	1.5
$\Delta V_{BB}/\Delta T$ (mV/°C)	10KH	0.8	1.0	1.2
	10K	0.8	1.0	1.2
$\Delta V_{OL}/\Delta T$ (mV/°C)	10KH	0	0.4	0.6
	10K	0.35	0.5	0.75
		0.75	1.0	1.55
$\Delta V_{OH}/\Delta V_{EE}$ (mV/V)	10KH	−20		0
	10K	−30		0
$\Delta V_{BB}/\Delta V_{EE}$ (mV/V)	10KH	0	10	25
	10K	110	150	190
$\Delta V_{OL}/\Delta V_{EE}$ (mV/V)	10KH	0	20	50
	10K	200	250	320

Noise Margin Considerations

Specification of input voltage levels (V_{IHA}, V_{ILA}) are changed from those of MECL 10K resulting in improved noise margins for MECL 10KH.

The MECL 10K circuits have two sets of output voltage specifications (V_{OH}, V_{OHA} and V_{OL}, V_{OLA}). The first output voltage specification in each set (V_{OH} and V_{OL}) are guaranteed maximum and minimum output levels for typical input levels. The second specification in each set (V_{OHA} and V_{OLA}) is the guaranteed worst-case output level for input threshold voltages. System analysis for worst-case noise margin considers V_{OHA} and V_{OLA} only. The MECL 10KH family has only one set of output voltages (V_{OH} and V_{OL}) with minimum and maximum values specified. The minimum value of V_{OH} and the maximum value for V_{OL} of the MECL 10KH family is synonomous with the V_{OHA} and V_{OLA} specifications of MECL 10K family.

The V_{OH} values for the MECL 10KH circuits are equal to or better than the MECL 10K levels at all temperatures. Input threshold voltages (V_{IHA} and V_{ILA}, which are synonymous with $V_{IH\ min}$ and $V_{IL\ max}$ for 10KH) are also improved and guaranteed V_{IHA} has been decreased by 25 mV over the entire operating temperature range, resulting in a "1" level noise margin of 150 mV (compared to

Table 4. — NOISE MARGIN versus POWER-SUPPLY CONDITIONS

Parameter		V_{EE} −10% Typ	V_{EE} −10% Min	V_{EE} −5% Typ	V_{EE} −5% Min	V_{EE} Typ	V_{EE} Min	V_{EE} +5% Typ	V_{EE} +5% Min
Noise Margin High	10KH	224	150	227	150	230	150	233	150
V_{NH} (mV)	10K	127	47	166	86	205	125	241	164
Noise Margin Low	10KH	264	150	267	150	270	150	273	150
V_{NL} (mV)	10K	223	103	249	129	275	155	301	181

*Temp = 0 to 75°C

125 mV for the MECL 10K circuits). V_{ILA} has been decreased by 5.0 mV, providing a "0" level noise margin equal to the "1" level noise margin. The V_{OL} minimum of the MECL 10KH is more negative than for MECL 10K (−1950 mV instead of −1850 mV). The V_{OL} level for the MECL 10K family was selected to ensure that the gate would not saturate at high temperatures and high supply voltages. The reduction in operating temperature range for the MECL 10KH family and the improvement in tracking rate allow the lower V_{OL} level. The change in this level does not affect system noise margins. Although some of the interface levels change with temperature, the changes in voltage levels are well within the tolerance ranges that would keep the families compatible. Table 4 lists some noise margins for V_{EE} supply variations.

The compatibility of MECL 10KH with MECL 10K may be demonstrated by applying the tracking rates in Table 3 to the dc specifications. The method for determining compatibility is to show acceptable noise margins for MECL 10KH, MECL 10K and mixed MECL 10K/MECL 10KH systems. The asssumption is that the families are compatible if the noise margin for a mixed system is equal to or better than the same system using only the MECL 10K series.

Using an all MECL 10K system as a reference, three possible logic mixes must be considered: MECL 10K driving MECL 10KH; MECL 10KH driving MECL 10K; and MECL 10KH driving MECL 10KH. The system noise margin for the three configurations can now be calculated for the following cases (See Figure 3):

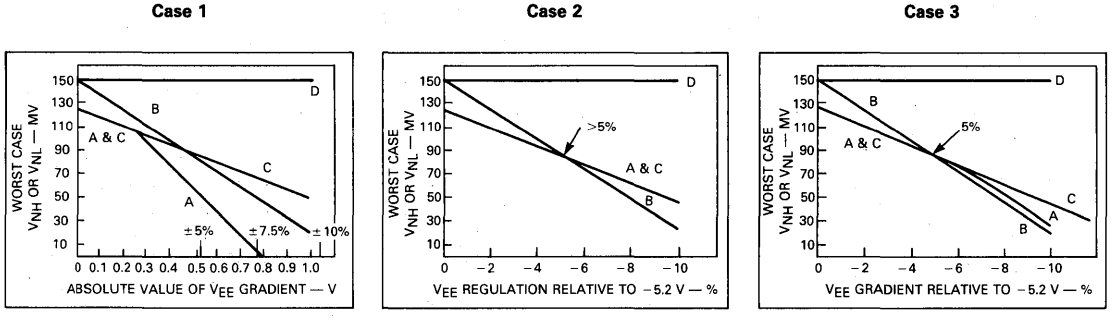
In Case 1, the system uses multiple power supplies, each independently voltage regulated to some percentage tolerance. Worst-case is where one device is at the plus extreme and the other device is at the minus extreme of the supply tolerance.

In Case 2, a system operates on a single supply or several supplies slaved to a master supply. The entire system can drift, but all devices are at the same supply voltage.

In Case 3, a system has excessive supply drops throughout. Supply gradients are due to resistive drops in V_{EE} bus.

The analysis indicates that the noise margins for a MECL 10K/10KH system equal or exceed the margins for an all 10K system for supply tolerance up to ±5%. The results of the analysis are shown in Figure 3.

FIGURE 3 — NOISE MARGIN versus POWER-SUPPLY VARIATION



A. MECL 10K DRIVING MECL 10K B. MECL 10K DRIVING MECL 10KH C. MECL 10KH DRIVING MECL 10K D. MECL 10KH DRIVING MECL10KH

MOTOROLA

MC10H016

Advance Information

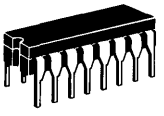
MECL 10KH HIGH-SPEED EMITTER-COUPLED LOGIC

The MC10H016 is a member of Motorola's new MECL family. The MC10H016 is a high-speed synchronous, presettable, cascadable 4-bit binary counter. It is useful for a large number of conversion, counting and digital integration applications.

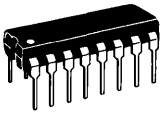
- Counting Frequency, 200 MHz Minimum
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible

MECL 10KH

4-BIT BINARY COUNTER



L SUFFIX
CERAMIC PACKAGE
CASE 620



P SUFFIX
PLASTIC PACKAGE
CASE 648

MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply (V_{CC} = 0)	V_{EE}	-8.0 to 0	Vdc
Input Voltage (V_{CC} = 0)	V_I	0 to V_{EE}	Vdc
Output Current — Continuous — Surge	I_{out}	50 100	mA
Operating Temperature Range	T_A	0 to +75	°C
Storage Temperature Range — Plastic — Ceramic	T_{stg}	-55 to +150 -55 to +165	°C

ELECTRICAL CHARACTERISTICS (V_{EE} = -5.2 V ± 5%) (See Note)

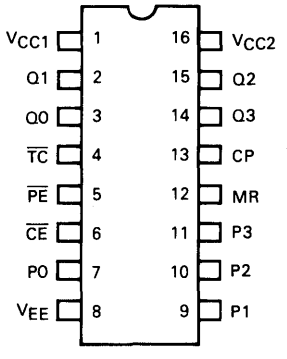
Characteristic	Symbol	0°		25°		75°		Unit
		Min	Max	Min	Max	Min	Max	
Power Supply Current	I_E	—	126	—	115	—	126	mA
Input Current High All Except MR Pin 12 MR	I_{inH}	 — —	 450 1190	 — —	 265 700	 — —	 265 700	μA
Input Current Low	I_{inL}	0.5	—	0.5	—	0.3	—	μA
High Output Voltage	V_{OH}	-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
Low Output Voltage	V_{OL}	-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
High Input Voltage	V_{IH}	-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
Low Input Voltage	V_{IL}	-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc

AC PARAMETERS

Propagation Delay Clock to Q Clock to $\overline{TC}$ MR to Q	t_{pd}	 0.7 0.7 0.7	 3.5 3.5 3.5	 0.7 0.7 0.7	 3.2 3.2 3.0	 0.7 0.7 0.7	 3.5 3.5 3.5	ns
Set-up Time P_n to Clock $\overline{CE}$ or $\overline{PE}$ to Clock	t_{set}	 2.0 2.5	 — —	 2.0 2.5	 — —	 2.0 2.5	 — —	ns
Hold Time Clock to P_n Clock to $\overline{CE}$ or $\overline{PE}$	t_{hold}	 1.0 0.5	 — —	 1.0 0.5	 — —	 1.0 0.5	 — —	ns
Counting Frequency	f_{count}	200	—	200	—	200	—	MHz
Rise Time	t_r	0.7	2.3	0.7	2.1	0.7	2.3	ns
Fall Time	t_f	0.7	2.3	0.7	2.1	0.7	2.3	ns

NOTE:
Each MECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts.

PIN ASSIGNMENT



TRUTH TABLE

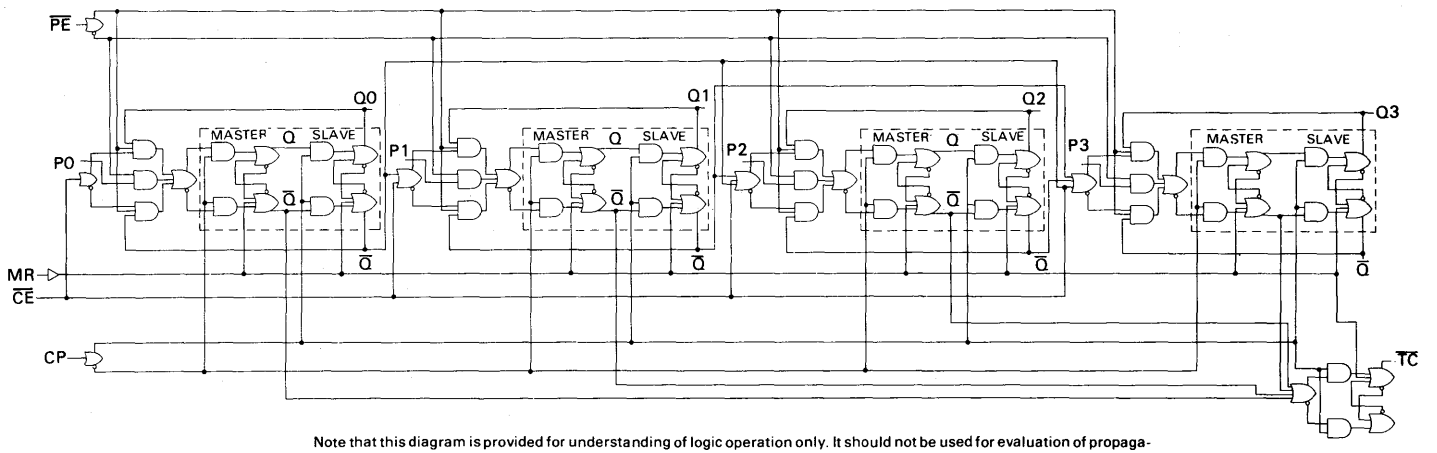
$\overline{CE}$	$\overline{PE}$	MR	CP	Function
L	L	L	Z	Load Parallel (P_n to Q_n)
H	L	L	Z	Load Parallel (P_n to Q_n)
L	H	L	Z	Count
H	H	L	Z	Hold
X	X	L	ZZ	Masters Respond; Slaves Hold
X	X	H	X	Reset (Q_n = LOW, $\overline{T}_C$ = HIGH)

Z = Clock Pulse (Low to High); ZZ = Clock Pulse (High to Low)

Features include assertion inputs and outputs on each of the four master/slave counting flip-flops. Terminal count is generated internally in a manner that allows synchronous loading at nearly the speed of the basic counter.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

4-BIT BINARY COUNTER LOGIC DIAGRAM



Note that this diagram is provided for understanding of logic operation only. It should not be used for evaluation of propagation delays as many gate functions are achieved internally without incurring a full gate delay.

MOTOROLA

MC10H100

Advance Information

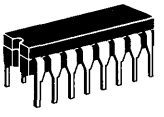
MECL 10KH

2

MECL 10KH HIGH-SPEED EMITTER-COUPLED LOGIC

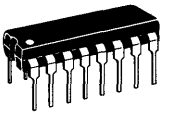
The MC10H100 is a member of Motorola's new MECL family. This MECL 10KH part is a functional/pinout duplication of the standard MECL 10K family part, with 100% improvement in propagation delay, and no increases in power supply current.

- Propagation Delay, 1.0 ns Typical
- 25 mW Typ/Gate (No Load)
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K—Compatible



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648



MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply (V_{CC} = 0)	V_{EE}	-8.0 to 0	Vdc
Input Voltage (V_{CC} = 0)	V_I	0 to V_{EE}	Vdc
Output Current — Continuous — Surge	I_{out}	50 100	mA
Operating Temperature Range	T_A	0 to +75	°C
Storage Temperature Range — Plastic — Ceramic	T_{stg}	-55 to +150 -55 to +165	°C

ELECTRICAL CHARACTERISTICS (V_{EE} = -5.2 V ± 5%) (See Note)

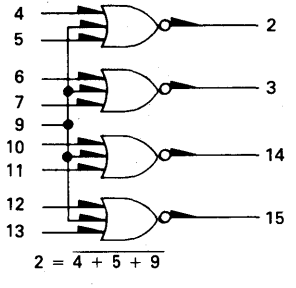
Characteristic	Symbol	0°		25°		75°		Unit
		Min	Max	Min	Max	Min	Max	
Power Supply Current	I_E	—	29	—	26	—	29	mA
Input Current High Pin 9 All Other Inputs	I_{inH}	 — —	 900 500	 — —	 560 310	 — —	 560 310	μA
Input Current Low	I_{inL}	0.5	—	0.5	—	0.3	—	μA
High Output Voltage	V_{OH}	-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
Low Output Voltage	V_{OL}	-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
High Input Voltage	V_{IH}	-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
Low Input Voltage	V_{IL}	-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc

AC PARAMETERS

Propagation Delay	t_{pd}	0.7	1.5	0.7	1.5	0.7	1.7	ns
Rise Time	t_r	0.7	1.9	0.7	1.9	0.7	2.3	ns
Fall Time	t_f	0.7	1.7	0.7	1.8	0.7	2.0	ns

NOTE:
Each MECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts.

Quad 2-Input
NOR Gate With Strobe



V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

The MC10H100 is a quad NOR gate. Each gate has 3 inputs, two of which are independent and one of which is tied common to all four gates.

This document contains information on a new product. Specifications and information herein are subject to change without notice. MECL, MECL III, MECL 10K and MECL 10KH are trademarks of Motorola Inc.

MOTOROLA

MC10H101
MC10H102
MC10H105

Advance Information

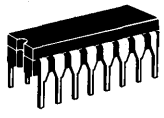
2

MECL 10KH HIGH-SPEED EMITTER-COUPLED LOGIC

The MC10H101, MC10H102 and MC10H105 are members of Motorola's new MECL family. These MECL 10KH parts are functional/pinout duplications of the standard MECL 10K family parts, with 100% improvement in propagation delay, and no increases in power-supply current.

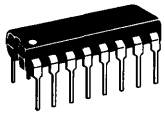
- Propagation Delay, 1 ns typical
- Power Dissipation 25 mW/Gate (same as MECL 10K)
- Improved Noise Margin 150 mV (over operating voltage and temperature range)
- Voltage Compensated
- MECL 10K-Compatible

MECL 10KH



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648



MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply (V_{CC} = 0)	V_{EE}	-8.0 to 0	Vdc
Input Voltage (V_{CC} = 0)	V_I	0 to V_{EE}	Vdc
Output Current — Continuous — Surge	I_{out}	50 100	mA
Operating Temperature Range	T_A	0-75	°C
Storage Temperature Range — Plastic — Ceramic	T_{stg}	-55 to 150 -55 to 165	°C °C

ELECTRICAL CHARACTERISTICS (V_{EE} = – 5.2 V ±5%)

Characteristic	Symbol	0°		25°		75°		Unit
		Min	Max	Min	Max	Min	Max	
Power Supply Current MC10H101, 102 MC10H105	I_E	 — —	 29 23	 — —	 26 21	 — —	 29 23	mA
Input Current High MC10H101, 102, 105 MC10H101 (Pin 12 only)	I_{inH}	 — —	 425 850	 — —	 265 535	 — —	 265 535	μA
Input Current Low	I_{inL}	0.5	—	0.5	—	0.3	—	μA
High Output Voltage	V_{OH}	-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
Low Output Voltage	V_{OL}	-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
High Input Voltage	V_{IH}	-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
Low Input Voltage	V_{IL}	-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc

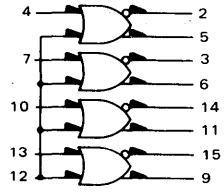
AC PARAMETERS

Propagation Delay	t_{pd}	0.7	1.6	0.7	1.5	0.7	1.7	ns
Rise Time	t_r	0.7	2.2	0.7	2.0	0.7	2.2	ns
Fall Time	t_f	0.7	2.2	0.7	2.0	0.7	2.2	ns

NOTE:
Each MECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater then 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts.

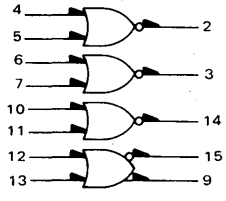
This document contains information on a new product. Specifications and information herein are subject to change without notice.

MC10H101



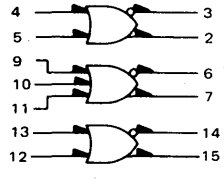
Quad OR/NOR Gate

MC10H102



Quad 2-Input NOR Gate

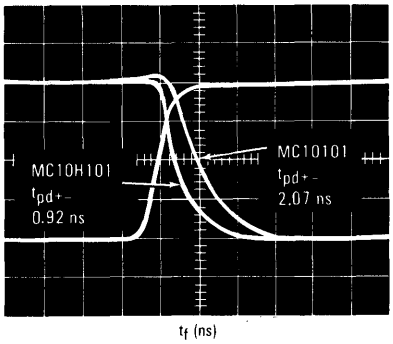
MC10H105



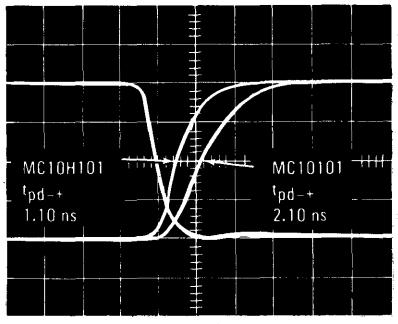
Triple 2-3-2 Input OR/NOR Gate

SWITCHING TIME COMPARISON
MECL 10KH versus MECL 10K

NOR OUTPUTS

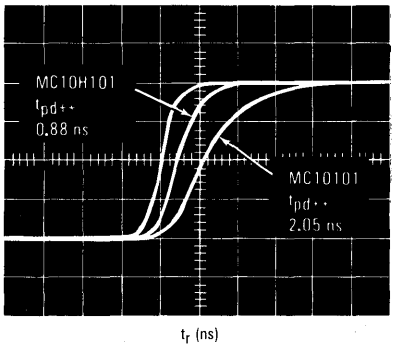


t_f (ns)
MC10H101 — 1.49
MC10101 — 2.4

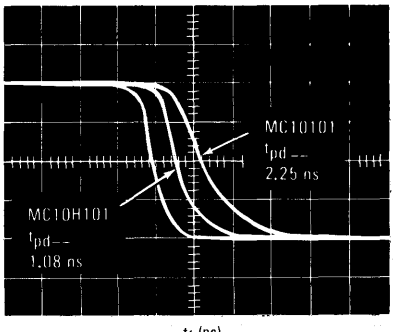


t_r (ns)
MC10H101 — 1.52
MC10101 — 2.62

OR OUTPUTS



t_r (ns)
MC10H101 — 1.48
MC10101 — 2.51



t_f (ns)
MC10H101 — 1.42
MC10101 — 2.45

MOTOROLA

MC10H103

Advance Information

2

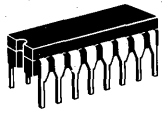
MECL 10KH HIGH-SPEED EMITTER-COUPLED LOGIC

The MC10H103 is a member of Motorola's new MECL family. This MECL 10KH part is a functional/pinout duplication of the standard MECL 10K family part with 100% improvement in propagation delay, and no increases in power-supply current.

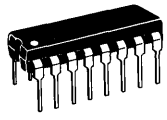
- Propagation Delay, 1.0 ns Typical
- Power Dissipation 25 mW/Gate (Same as MECL 10K)
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible

MECL 10KH

QUAD 2-INPUT OR GATE



P SUFFIX
PLASTIC PACKAGE
CASE 648



L SUFFIX
CERAMIC PACKAGE
CASE 620

MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply (V_{CC} = 0)	V_{EE}	-8.0 to 0	Vdc
Input Voltage (V_{CC} = 0)	V_I	0 to V_{EE}	Vdc
Output Current — Continuous — Surge	I_{out}	50 100	mA
Operating Temperature Range	T_A	0–+75	°C
Storage Temperature Range — Plastic — Ceramic	T_{stg}	-55 to +150 -55 to +165	°C °C

ELECTRICAL CHARACTERISTICS (V_{EE} = -5.2 V ±5%) (See Note)

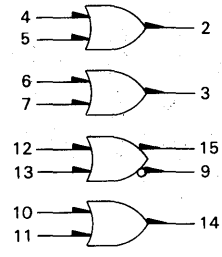
Characteristic	Symbol	0°		25°		75°		Unit
		Min	Max	Min	Max	Min	Max	
Power Supply Current	I_E	—	29	—	26	—	29	mA
Input Current High	I_{inH}	—	425	—	265	—	265	μA
Input Current Low	I_{inL}	0.5	—	0.5	—	0.3	—	μA
High Output Voltage	V_{OH}	-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
Low Output Voltage	V_{OL}	-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
High Input Voltage	V_{IH}	-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
Low Input Voltage	V_{IL}	-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc

AC PARAMETERS

Propagation Delay	t_{pd}	0.7	1.6	0.7	1.5	0.7	1.7	ns
Rise Time	t_r	0.7	2.2	0.7	2.0	0.7	2.2	ns
Fall Time	t_f	0.7	2.2	0.7	2.0	0.7	2.2	ns

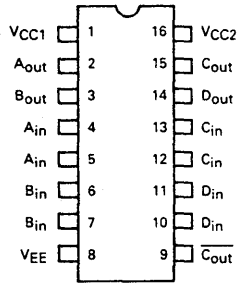
NOTE:
Each MECL 10 KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Outputs are terminated through a 50 ohm resistor to -2.0 volts.

LOGIC DIAGRAM



V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

PIN ASSIGNMENT



MOTOROLA

MC10H104
MC10H107
MC10H109

Advance Information

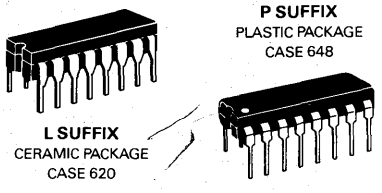
MECL 10KH

2

MECL 10KH HIGH-SPEED EMITTER-COUPLED LOGIC

The MC10H104, MC10H107 and MC10H109 are members of Motorola's new MECL family. These MECL 10KH parts are functional/pinout duplications of the standard MECL 10K family parts, with 100% improvement in propagation delay, and no increase in power-supply current.

- Propagation Delay, 1 ns Typical
- Power Dissipation 35 mW/Gate Typical (same as MECL 10K)
- Improved Noise Margin 150 mV (over operating voltage and temperature range)
- Voltage Compensated
- MECL 10K-Compatible



P SUFFIX
PLASTIC PACKAGE
CASE 648

L SUFFIX
CERAMIC PACKAGE
CASE 620

MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply (V_{CC} = 0)	V_{EE}	-8.0 to 0	Vdc
Input Voltage (V_{CC} = 0)	V_I	0 to V_{EE}	Vdc
Output Current — Continuous — Surge	I_{out}	50 100	mA
Operating Temperature Range	T_A	0–75	°C
Storage Temperature Range — Plastic — Ceramic	T_{stg}	-55 to 150 -55 to 165	°C °C

ELECTRICAL CHARACTERISTICS (V_{EE} = 5.2 V ±5%) (See Note)

Characteristic	Symbol	0°		25°		75°		Unit
		Min	Max	Min	Max	Min	Max	
Power Supply Current	I_E							mA
MC10H104		—	39	—	35	—	39	
MC10H107		—	31	—	28	—	31	
MC10H109		—	15	—	14	—	15	
Input Current High	I_{inH}	—	425	—	265	—	265	mA
Input Current Low	I_{inL}	0.5	—	0.5	—	0.3	—	μA
High Output Voltage	V_{OH}	-1.02	-0.84	-0.98	-0.81	-0.92	0.735	Vdc
Low Output Voltage	V_{OL}	-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
High Input Voltage	V_{IH}	-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
Low Input Voltage	V_{IL}	-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc

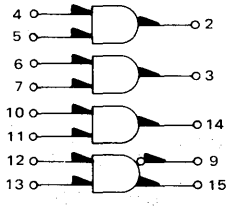
AC PARAMETERS

Propagation Delay	t_{pd}							ns
MC10H104		0.7	2.2	0.7	2.0	0.7	2.2	
MC10H107		0.7	2.0	0.7	1.9	0.7	2.0	
MC10H109		0.7	1.6	0.7	1.5	0.7	1.7	
Rise Time	t_r	0.7	2.2	0.7	2.0	0.7	2.2	ns
Fall Time	t_f	0.7	2.2	0.7	2.0	0.7	2.2	ns

NOTE:
Each MECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater then 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts.

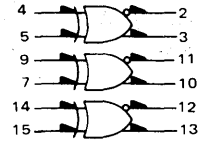
This document contains information on a new product. Specifications and information herein are subject to change without notice.

MC10H104



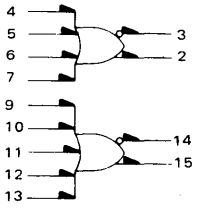
Quad 2-Input AND Gate

MC10H107



Triple 2-Input Exclusive OR/NOR Gate

MC10H109

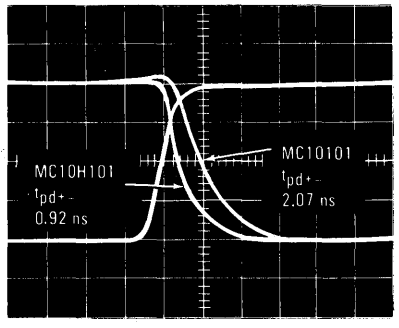


Dual 4-5 Input OR/NOR Gate

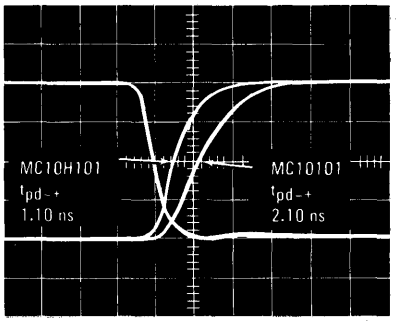
2

SWITCHING TIME COMPARISON
MECL 10KH versus MECL 10K

NOR OUTPUTS

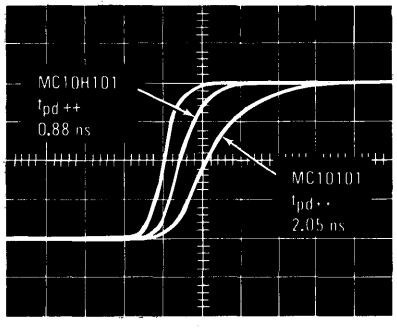


t_f (ns)
MC10H101 — 1.49
MC10101 — 2.4

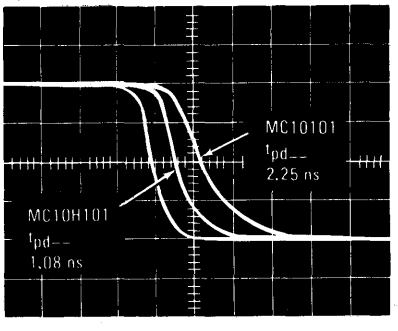


t_r (ns)
MC10H101 — 1.52
MC10101 — 2.62

OR OUTPUTS



t_r (ns)
MC10H101 — 1.48
MC10101 — 2.51



t_f (ns)
MC10H101 — 1.42
MC10101 — 2.45

MOTOROLA

MC10H106

Advance Information

MECL 10KH

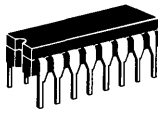
TRIPLE 4-3-3 INPUT NOR GATE

2

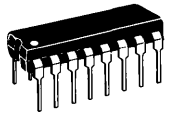
MECL 10KH HIGH-SPEED EMITTER-COUPLED LOGIC

The MC10H106 is a member of Motorola's new MECL family. This device is a triple 4-3-3 input NOR gate. This 10KH part is a functional/pinout duplication of the standard MECL 10K family part, with 100% improvement in propagation delay and no increase in power-supply current.

- Propagation Delay, 1.0 ns Typical
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible



P SUFFIX
PLASTIC PACKAGE
CASE 648



L SUFFIX
CERAMIC PACKAGE
CASE 620

MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply (V_{CC} = 0)	V_{EE}	−8.0 to 0	Vdc
Input Voltage (V_{CC} = 0)	V_I	0 to V_{EE}	Vdc
Output Current — Continuous — Surge	I_{out}	50 100	mA
Operating Temperature Range	T_A	0 − +75	°C
Storage Temperature Range — Plastic — Ceramic	T_{stg}	−55 to +150 −55 to +165	°C °C

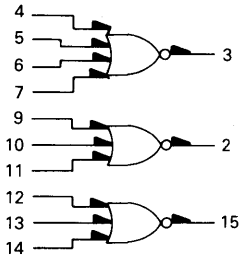
ELECTRICAL CHARACTERISTICS (V_{EE} = −5.2 V ±5%) (See Note)

Characteristic	Symbol	0°		25°		75°		Unit
		Min	Max	Min	Max	Min	Max	
Power Supply Current	I_E	—	23	—	21	—	23	mA
Input Current High	I_{inH}	—	500	—	310	—	310	μA
Input Current Low	I_{inL}	0.5	—	0.5	—	0.3	—	μA
High Output Voltage	V_{OH}	−1.02	−0.84	−0.98	−0.81	−0.92	−0.735	Vdc
Low Output Voltage	V_{OL}	−1.95	−1.63	−1.95	−1.63	−1.95	−1.60	Vdc
High Input Voltage	V_{IH}	−1.17	−0.84	−1.13	−0.81	−1.07	−0.735	Vdc
Low Input Voltage	V_{IL}	−1.95	−1.48	−1.95	−1.48	−1.95	−1.45	Vdc
AC PARAMETERS								
Propagation Delay	t_{pd}	0.7	1.6	0.7	1.5	0.7	1.7	ns
Rise Time	t_r	0.7	2.2	0.7	2.0	0.7	2.2	ns
Fall Time	t_f	0.7	2.2	0.7	2.0	0.7	2.2	ns

NOTE
Each MECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts.

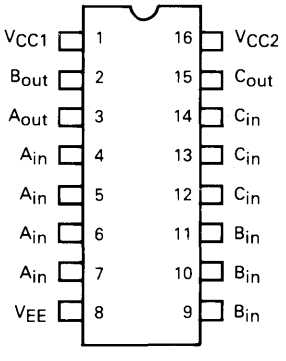
This document contains information on a new product. Specifications and information herein are subject to change without notice.

LOGIC DIAGRAM



V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

PIN ASSIGNMENT



MOTOROLA

MC10H113

Advance Information

2

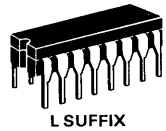
QUAD EXCLUSIVE OR GATE

The MC10H113 is a member of Motorola's new MECL family. The MC10H113 is a Quad Exclusive OR Gate with an enable common to all four gates. The outputs may be wire-ORed together to perform a 4-bit comparison function (A=B). The enable is active LOW.

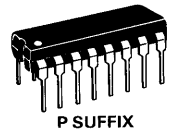
- Propagation delay 1.3 ns typ.
- Power dissipation 175 mw typ/pkg (no load)
- Improved noise margin 150 mV (over operating voltage and temperature range)
- Voltage compensated
- MECL 10K-compatible

MECL 10KH

QUAD EXCLUSIVE OR GATE



L SUFFIX
CERAMIC PACKAGE
CASE 620



P SUFFIX
PLASTIC PACKAGE
CASE 648

MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply (V_{CC} = 0)	V_{EE}	-8.0 to 0	Vdc
Input Voltage (V_{CC} = 0)	V_I	0 to V_{EE}	Vdc
Output Current — Continuous — Surge	I_{out}	50 100	mA
Operating Temperature Range	T_A	0 to +75	°C
Storage Temperature Range — Plastic — Ceramic	T_{stg}	-55 to +150 -55 to +165	°C °C

ELECTRICAL CHARACTERISTICS (V_{EE} = -5.2 V ±5%) (See Note)

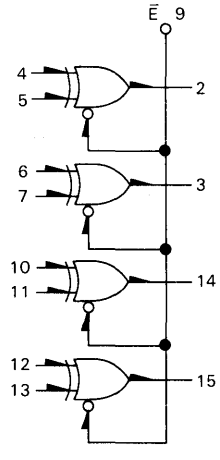
Characteristic	Symbol	0°		25°		75°		Unit
		Min	Max	Min	Max	Min	Max	
Power Supply Current	I_E	—	46	—	42	—	46	mA
Input Current High Pins 5, 7, 11, 13 Pins 4, 6, 10, 12 Pin 9	I_{inH}	 — — —	 430 510 1100	 — — —	 270 320 740	 — — —	 270 320 740	μA
Input Current Low	I_{inL}	0.5	—	0.5	—	0.3	—	μA
High Output Voltage	V_{OH}	-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
Low Output Voltage	V_{OL}	-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
High Input Voltage	V_{IH}	-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
Low Input Voltage	V_{IL}	-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc

AC PARAMETERS

Propagation Delay Data Enable	t_{pd}	 0.7 0.7	 2.5 2.8	 0.7 0.7	 2.3 2.5	 0.7 0.7	 2.5 2.8	ns
Rise Time	t_r	0.7	2.4	0.7	2.2	0.7	2.4	ns
Fall Time	t_f	0.7	2.4	0.7	2.2	0.7	2.4	ns

NOTE:
Each MECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Outputs are terminated through a 50 ohm resistor to -2.0 volts.

LOGIC DIAGRAM



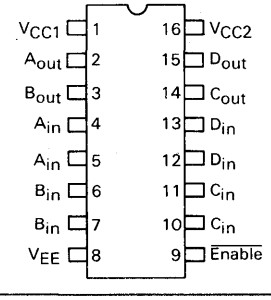
TRUTH TABLE

IN		$\overline{E}$	OUTPUT
L	L	L	L
L	H	L	H
H	L	L	H
H	H	L	L
ϕ	ϕ	H	L

ϕ = Don't Care

V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

PIN ASSIGNMENT



MOTOROLA

MC10H115

Advance Information

MECL 10KH HIGH-SPEED EMITTER-COUPLED LOGIC

The MC10H115 is a member of Motorola's new MECL family. The MC10H115 is a quad differential amplifier designed for use in sensing differential signals over long lines. This MECL 10KH part is a functional/pinout duplication of the standard MECL 10K family part, with 100% improvement in counting frequency and no increase in power-supply current.

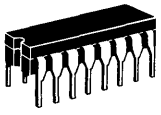
The base bias supply (V_{BB}) is made available at Pin 9 to make the device useful as a Schmitt trigger, or in other applications where a stable reference voltage is necessary. Active current sources provide the MC10H115 with excellent common mode rejection. If any amplifier in a package is not used, one input of that amplifier must be connected to V_{BB} (Pin 9) to prevent upsetting the current source bias network.

- Propagation Delay, 1.0 ns Typical
- Power Dissipation 110 mW Typ/Pkg (No Load)
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible

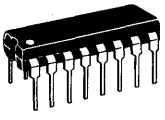
MECL 10KH

QUAD LINE RECEIVER

2



P SUFFIX
PLASTIC PACKAGE
CASE 648

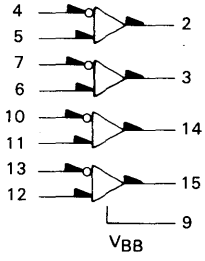


L SUFFIX
CERAMIC PACKAGE
CASE 620

MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply (V_{CC} = 0)	V_{EE}	-8.0 to 0	Vdc
Input Voltage (V_{CC} = 0)	V_I	0 to V_{EE}	Vdc
Output Current — Continuous — Surge	I_{out}	50 100	mA
Operating Temperature Range	T_A	0–+75	°C
Storage Temperature Range — Plastic — Ceramic	T_{stg}	-55 to +150 -55 to +165	°C °C

LOGIC DIAGRAM

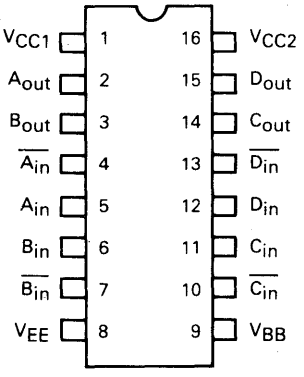


V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

ELECTRICAL CHARACTERISTICS (V_{EE} = -5.2 V ±5%) (See Note)

Characteristic	Symbol	0°		25°		75°		Unit
		Min	Max	Min	Max	Min	Max	
Power Supply Current	I_E	—	29	—	26	—	29	mA
Input Current	I_{inH}	—	150	—	95	—	95	μA
	I_{CBO}	—	1.5	—	1.0	—	1.0	μA
High Output Voltage	V_{OH}	-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
Low Output Voltage	V_{OL}	-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
High Input Voltage	V_{IH}	-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
Low Input Voltage	V_{IL}	-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc
Reference Voltage	V_{BB}	-1.42	-1.28	-1.35	-1.23	-1.295	-1.15	Vdc

PIN ASSIGNMENT



AC PARAMETERS

Propagation Delay	t_{pd}	0.7	1.6	0.7	1.5	0.7	1.7	ns
Rise Time	t_r	0.7	2.2	0.7	2.0	0.7	2.2	ns
Fall Time	t_f	0.7	2.2	0.7	2.0	0.7	2.2	ns

NOTE:
Each MECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Outputs are terminated through a 50 ohm resistor to -2.0 volts.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

MOTOROLA

MC10H116

Advance Information

2

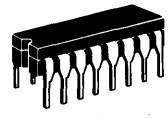
MECL 10KH HIGH-SPEED EMITTER-COUPLED LOGIC

The MC10H116 is a member of Motorola's new MECL family. It is a functional/pinout duplication of the MC10116, with 100% improvement in propagation delay and no increase in power-supply current.

- Propagation Delay, 1 ns typical
- Power Dissipation 85 mW typ/pkg (same as MECL 10K)
- Improved Noise Margin 150 mV (over operating voltage and temperature range) (1)
- Voltage Compensated
- MECL 10K Compatible.

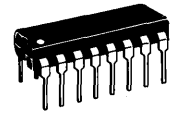
MECL 10KH

TRIPLE LINE RECEIVER



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648



MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply (V_{CC} = 0)	V_{EE}	-8.0 to 0	Vdc
Input Voltage (V_{CC} = 0)	V_I	0 to V_{EE}	Vdc
Output Current — Continuous — Surge	I_{out}	50 100	mA
Operating Temperature Range	T_A	0–75	°C
Storage Temperature Range — Plastic — Ceramic	T_{stg}	-55 to 150 -55 to 165	°C °C

ELECTRICAL CHARACTERISTICS (V_{EE} = 5.2 V ±5%) (2)

Characteristic	Symbol	0°		25°		75°		Unit
		Min	Max	Min	Max	Min	Max	
Power Supply Current	I_E	—	23	—	21	—	23	mA
Input Current High	I_{inH}	—	150	—	95	—	95	μA
Input Leakage Current	I_{CBO}	—	1.5	—	1.0	—	1.0	μA
Reference Voltage	V_{BB}	-1.42	-1.28	-1.35	-1.23	-1.29	-1.15	Vdc
High Output Voltage	V_{OH}	-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
Low Output Voltage	V_{OL}	-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
High Input Voltage (1)	V_{IH}	-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
Low Input Voltage (1)	V_{IL}	-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc
Common Mode Range (3)	V_{CMR}	—	—	-2.85 to -0.8		—	—	Vdc
Input Sensitivity (4)	V_{PP}	—	—	150 typ		—	—	mVpp

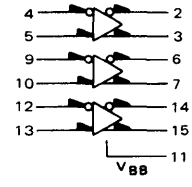
AC PARAMETERS

Propagation Delay	t_{pd}	0.7	1.6	0.7	1.5	0.7	1.7	ns
Rise Time	t_r	0.7	2.2	0.7	2.0	0.7	2.2	ns
Fall Time	t_f	0.7	2.2	0.7	2.0	0.7	2.2	ns

NOTES:
1. When V_{BB} is used as the reference voltage
2. Each MECL 10KH series circuit has been designed to meet the specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts.
3. Differential input not to exceed 1.0 Vdc
4. Differential input required to obtain full logic swing on output.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

MC10H116



Triple Line Receiver

The MC10H116 is designed to be used in sensing differential signals over long lines. The bias supply (V_{BB}) is made available to make the device useful as a Schmitt trigger, or in other applications where a stable reference voltage is necessary.

Active current sources provide these receivers with excellent common-mode noise rejection. If any amplifier in a package is not used, one input of that amplifier must be connected to V_{BB} to prevent unbalancing the current-source bias network.

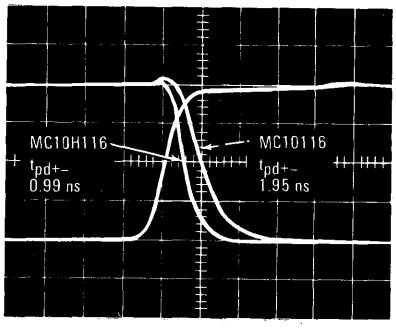
The MC10H116 does not have internal-input pull-down resistors. This provides high impedance to the amplifier input and facilitates differential connections.

Applications:

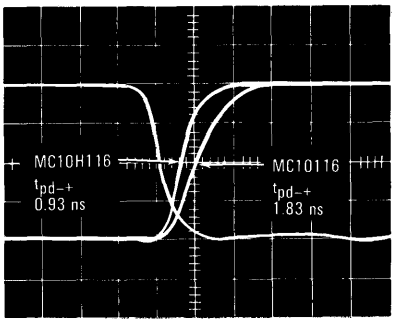
- Low Level Receiver
- Schmitt Trigger
- Voltage Level Interface

SWITCHING TIME COMPARISON
MECL 10KH versus MECL 10K

NOR OUTPUTS

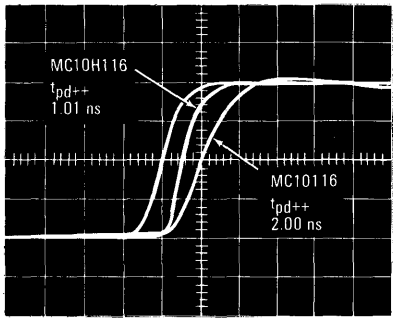


t_f (ns)
MC10H116 — 1.08
MC10116 — 1.74

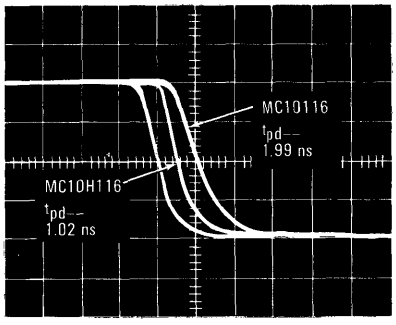


t_r (ns)
MC10H116 — 1.12
MC10116 — 1.86

OR OUTPUTS



t_r (ns)
MC10H116 — 1.23
MC10116 — 1.98



t_f (ns)
MC10H116 — 1.21
MC10116 — 1.84

MOTOROLA

MC10H117
MC10H118

Advance Information

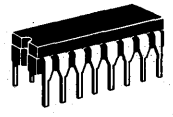
2

MECL 10KH HIGH-SPEED EMITTER-COUPLED LOGIC

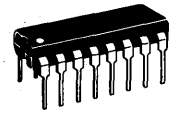
The MC10H117 and MC10H118 are members of Motorola's new MECL family. These MECL 10KH parts are functional/pinout duplications of the standard MECL 10K family parts, with 100% improvement in propagation delay, and no increase in power-supply current.

- Propagation Delay, 1 ns Typical
- Power Dissipation 100 mW/Gate Typical (same as MECL 10K)
- Improved Noise Margin 150 mV (over operating voltage and temperature range)
- Voltage Compensated
- MECL 10K-Compatible.

MECL 10KH



P SUFFIX
PLASTIC PACKAGE
CASE 648



L SUFFIX
CERAMIC PACKAGE
CASE 620

MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply (V_{CC} = 0)	V_{EE}	-8.0 to 0	Vdc
Input Voltage (V_{CC} = 0)	V_I	0 to V_{EE}	Vdc
Output Current — Continuous — Surge	I_{out}	50 100	mA
Operating Temperature Range	T_A	0-75	°C
Storage Temperature Range — Plastic — Ceramic	T_{stg}	-55 to 150 -55 to 165	°C °C

ELECTRICAL CHARACTERISTICS (V_{EE} = 5.2 V ±5%) (See Note)

Characteristic	Symbol	0°		25°		75°		Unit
		Min	Max	Min	Max	Min	Max	
Power Supply Current	I_E		29		26		29	mA
Input Current High Pins 3*, 4, 5, 12, 13, 14* Pins 6, 7, 10, 11 Pin 9	I_{inH}		 465 545 710		 275 320 415		 275 320 415	µA
Input Current Low	I_{inL}	0.5	—	0.5	—	0.3	—	µA
High Output Voltage	V_{OH}	-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
Low Output Voltage	V_{OL}	-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
High Input Voltage	V_{IH}	-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
Low Input Voltage	V_{IL}	-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc

AC PARAMETERS

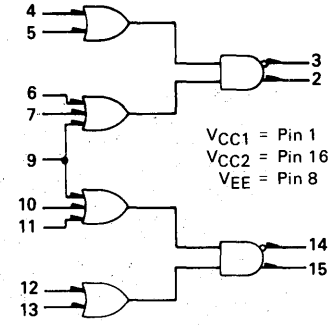
Propagation Delay	t_{pd}	0.7	2.0	0.7	1.8	0.8	1.9	ns
Rise Time	t_r	0.7	2.0	0.7	2.0	0.7	2.2	ns
Fall Time	t_f	0.7	2.0	0.7	2.0	0.7	2.2	ns

*MC10H118 only

NOTE:
Each MECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater then 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts.

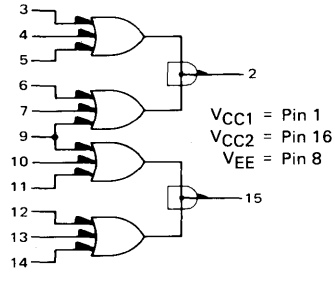
This document contains information on a new product. Specifications and information herein are subject to change without notice.

MC10H117



Dual 2-Wide 2-3 Input OR-AND/OR-AND-INVERT Gate

MC10H118



Dual 2-Wide 3-Input OR-AND Gate

MOTOROLA

MC10H119
MC10H121

Advance Information

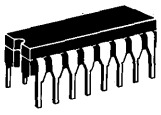
MECL 10KH

2

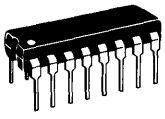
MECL 10KH HIGH-SPEED EMITTER-COUPLED LOGIC

The MC10H119 and MC10H121 are members of Motorola's new MECL family. These MECL 10KH parts are functional/pinout duplications of the standard MECL 10K family parts, with 100% improvement in propagation delay, and no increase in power-supply current.

- Propagation Delay, 1 ns Typical
- Power Dissipation 100 mW/Gate Typical (same as MECL 10K)
- Improved Noise Margin 150 mV (over operating voltage and temperature range)
- Voltage Compensated
- MECL 10K-Compatible.



P SUFFIX
PLASTIC PACKAGE
CASE 648



L SUFFIX
CERAMIC PACKAGE
CASE 620

MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply (V_{CC} = 0)	V_{EE}	-8.0 to 0	Vdc
Input Voltage (V_{CC} = 0)	V_I	0 to V_{EE}	Vdc
Output Current — Continuous — Surge	I_{out}	50 100	mA
Operating Temperature Range	T_A	0-75	°C
Storage Temperature Range — Plastic — Ceramic	T_{stg}	-55 to 150 -55 to 165	°C °C

ELECTRICAL CHARACTERISTICS (V_{EE} = 5.2 V ±5%) (See Note)

Characteristic	Symbol	0°		25°		75°		Unit
		Min	Max	Min	Max	Min	Max	
Power Supply Current	I_E		29		26		29	mA
Input Current High Pins 3*, 4, 5, 6, 7, 9, 11, 12, 13, 14, 15 Pin 10	I_{inH}		 500 610		 295 360		 295 360	μA
Input Current Low	I_{inL}	0.5	—	0.5	—	0.3	—	μA
High Output Voltage	V_{OH}	-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
Low Output Voltage	V_{OL}	-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
High Input Voltage	V_{IH}	-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
Low Input Voltage	V_{IL}	-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc

AC PARAMETERS

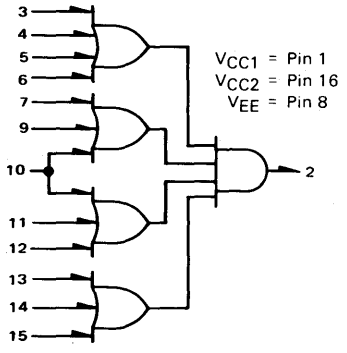
Propagation Delay	t_{pd}	0.7	2.4	0.7	2.3	0.7	2.4	ns
Rise Time	t_r	0.7	2.4	0.7	2.3	0.7	2.4	ns
Fall Time	t_f	0.7	2.4	0.7	2.3	0.7	2.4	ns

*MC10H119 only

NOTE:
Each MECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater then 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts.

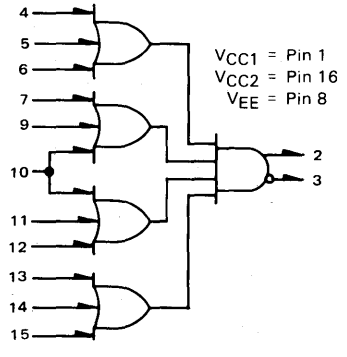
This document contains information on a new product. Specifications and information herein are subject to change without notice.

MC10H119



4-Wide 4-3-3-3 Input OR-AND Gate

MC10H121



4-Wide OR-AND/OR-AND-INVERT Gate

MOTOROLA

MC10H123

Advance Information

2

TRIPLE 4-3-3 INPUT BUS DRIVER

The MC10H123 is a member of Motorola's new MECL family. The device is a triple 4-3-3 Input Bus Driver.

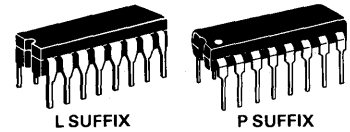
The MC10H123 consists of three NOR gates designed for bus driving applications on card or between cards. Output low logic levels are specified with $V_{OL} \leqslant -2.0$ Vdc so that the bus may be terminated to -2.0 Vdc. The gate output, when low, appears as a high impedance to the bus, because the output emitter-followers of the MC10H123 are "turned-off." This eliminates discontinuities in the characteristic impedance of the bus.

The V_{OH} level is specified when driving a 25-ohm load terminated to -2.0 Vdc, the equivalent of a 50-ohm bus terminated at both ends. Although 25 ohms is the lowest characteristic impedance that can be driven by the MC10H123, higher impedance values may be used with this part. A typical 50-ohm bus is shown in Figure 1.

- Propagation Delay, 1.5 ns Typical
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible

MECL 10KH

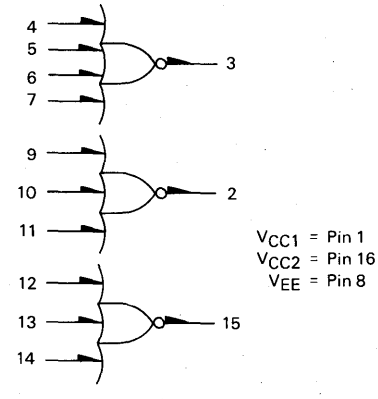
TRIPLE 4-3-3 INPUT BUS DRIVER



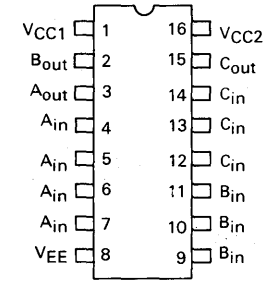
L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

LOGIC DIAGRAM



PIN ASSIGNMENT



MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply (V_{CC} = 0)	V_{EE}	-8.0 to 0	Vdc
Input Voltage (V_{CC} = 0)	V_I	0 to V_{EE}	Vdc
Output Current — Continuous — Surge	I_{out}	50 100	mA
Operating Temperature Range	T_A	0 to +75	°C
Storage Temperature Range — Plastic — Ceramic	T_{stg}	-55 to +150 -55 to +165	°C °C

ELECTRICAL CHARACTERISTICS (V_{EE} = -5.2 V ±5%) (See Note)

Characteristic	Symbol	0°		25°		75°		Unit
		Min	Max	Min	Max	Min	Max	
Power Supply Current	I_E	—	60	—	56	—	60	mA
Input Current High	I_{inH}		495		310		310	μA
Input Current Low	I_{inL}	0.5	—	0.5	—	0.3	—	μA
High Output Voltage	V_{OH}	-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
Low Output Voltage	V_{OL}	-2.1	-2.03	-2.1	-2.03	-2.1	-2.03	Vdc
High Input Voltage	V_{IH}	-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
Low Input Voltage	V_{IL}	-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc

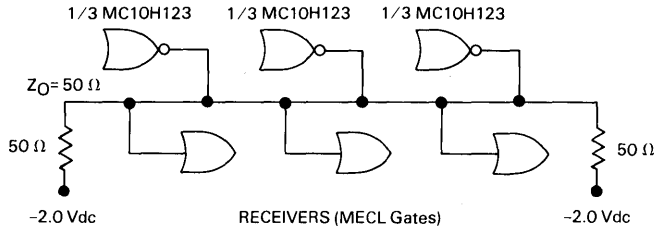
AC PARAMETERS

Propagation Delay	t_{pd}	0.7	2.3	0.7	2.3	0.7	2.3	ns
Rise Time	t_r	0.7	2.5	0.7	2.5	0.7	2.5	ns
Fall Time	t_f	0.7	2.5	0.7	2.5	0.7	2.5	ns

NOTE:
Each MECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Outputs are terminated through a 50 ohm resistor to -2.0 volts.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

FIGURE 1—50-OHM BUS DRIVER



MOTOROLA

MC10H124

Advance Information

2

MECL 10KH HIGH-SPEED EMITTER-COUPLED LOGIC

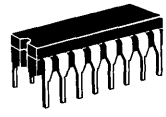
The MC10H124 is a member of Motorola's new MECL family. The MC10H124 is a quad translator for interfacing data and control signals between a saturated logic section and the MECL section of digital systems. The 10KH part is a functional/pinout duplication of the standard MECL 10K family part, with 100% improvement in propagation delay, and no increase in power-supply current.

- Propagation Delay, 1.5 ns Typical
- Voltage Compensated
- Improved Noise Margin 150 mV
- MECL 10K-Compatible

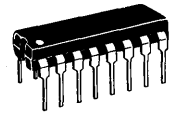
(Over Operating Voltage and Temperature Range)

MECL 10KH

QUAD TTL-TO-MECL TRANSLATOR

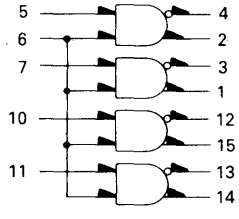


P SUFFIX
PLASTIC PACKAGE
CASE 648



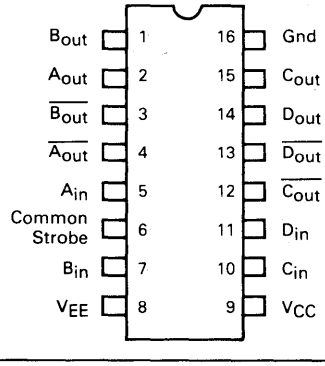
L SUFFIX
CERAMIC PACKAGE
CASE 620

QUAD TTL-TO-ECL TRANSLATOR



Gnd = Pin 16
V_{CC} (+5.0 Vdc) = Pin 9
V_{EE} (−5.2 Vdc) = Pin 8

PIN ASSIGNMENT



MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply (V_{CC} = 5.0 V)	V_{EE}	−8.0 to 0	Vdc
Power Supply (V_{EE} = −5.2 V)	V_{CC}	0 to +7.0	Vdc
Input Voltage (V_{CC} = 5.0 V) TTL	V_I	0 to V_{CC}	Vdc
Output Current — Continuous — Surge	I_{out}	50 100	mA
Operating Temperature Range	T_A	0 to +75	°C
Storage Temperature Range — Plastic — Ceramic	T_{stg}	−55 to +150 −55 to +165	°C

ELECTRICAL CHARACTERISTICS (V_{EE} = −5.2 V ±5%, V_{CC} = 5.0 V ±5.0 %)

Characteristic	Symbol	0°		25°		75°C		Unit
		Min	Max	Min	Max	Min	Max	
Negative Power Supply Drain Current	I_E	—	72	—	66	—	72	mAdc
Positive Power Supply Drain Current	I_{CCH}	—	16	—	16	—	18	mAdc
	I_{CCL}	—	25	—	25	—	25	mAdc
Reverse Current Pin 6	I_R	—	200	—	200	—	200	μAdc
Pin 7		—	50	—	50	—	50	
Forward Current Pin 6	I_F	—	−12.8	—	−12.8	—	−12.8	mAdc
Pin 7		—	−3.2	—	−3.2	—	−3.2	
Input Breakdown Voltage	$V_{(BR)in}$	5.5	—	5.5	—	5.5	—	Vdc
Input Clamp Voltage	V_I	—	−1.5	—	−1.5	—	−1.5	Vdc
High Output Voltage	V_{OH}	−1.02	−0.84	−0.98	−0.81	−0.92	−0.735	Vdc
Low Output Voltage	V_{OL}	−1.95	−1.63	−1.95	−1.63	−1.95	−1.60	Vdc
High Input Voltage	V_{IH}	2.0	—	2.0	—	2.0	—	Vdc
Low Input Voltage	V_{IL}	—	0.8	—	0.8	—	0.8	Vdc

AC PARAMETERS

Propagation Delay	t_{pd}	0.7	2.5	0.7	2.2	0.7	2.5	ns
Rise Time	t_r	0.7	1.5	0.7	1.5	0.7	1.7	ns
Fall Time	t_f	0.7	1.5	0.7	1.5	0.7	1.7	ns

NOTE:
Each MECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

APPLICATIONS INFORMATION

The MC10H124 has TTL-compatible inputs and MECL complementary open-emitter outputs that allow use as an inverting/non-inverting translator or as a differential line driver. When the common strobe input is at the low-logic level, it forces all true outputs to a MECL low-logic state and all inverting outputs to a MECL high-logic state.

An advantage of this device is that TTL-level information can be transmitted differentially, via balanced twisted pair lines, to MECL equipment, where the signal can be received by the MC10H115 or MC10H116 differential line receivers. The power supply requirements are ground, +5.0 volts, and −5.2 volts.

MOTOROLA

MC10H125

Advance Information

2

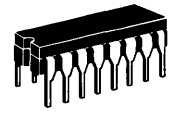
MECL 10KH HIGH-SPEED EMITTER-COUPLED LOGIC

The MC10H125 is a member of Motorola's new MECL family. The MC10H125 is a quad translator for interfacing data and control signals between the MECL section and saturated logic section of digital systems. The 10KH part is a functional/pinout duplication of the standard MECL 10K family part, with 100% improvement in propagation delay, and no increase in power-supply current.

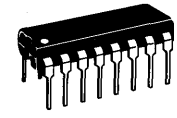
- Propagation Delay, 2.5 ns Typical
- Voltage Compensated
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- MECL 10K-Compatible

MECL 10KH

QUAD MECL-TO-TTL TRANSLATOR



P SUFFIX
PLASTIC PACKAGE
CASE 648



L SUFFIX
CERAMIC PACKAGE
CASE 620

MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply (V_{CC} = 5.0 V)	V_{EE}	-8.0 to 0	Vdc
Power Supply (V_{EE} = -5.2V)	V_{CC}	0 to +7.0	Vdc
Input Voltage (V_{CC} = 5.0 V)	V_I	0 to V_{EE}	Vdc
Operating Temperature Range	T_A	0 to +75	°C
Storage Temperature Range — Plastic — Ceramic	T_{stg}	-55 to +150 -55 to +165	°C

ELECTRICAL CHARACTERISTICS (V_{EE} = -5.2 V ± 5%, V_{CC} = 5.0 V ± 5.0%) (See Note)

Characteristic	Symbol	0°		25°		75°C		Unit
		Min	Max	Min	Max	Min	Max	
Negative Power Supply Drain Current	I_E	—	44	—	40	—	44	mAdc
Positive Power Supply Drain Current	I_{CCH}	—	63	—	63	—	63	mAdc
	I_{CCL}	—	40	—	40	—	40	mAdc
Input Current	I_{inH}	—	225	—	145	—	145	μAdc
Input Leakage Current	I_{CBO}	—	1.5	—	1.0	—	1.0	μAdc
High Output Voltage I_{OH} = -1 mA	V_{OH}	2.5	—	2.5	—	2.5	—	Vdc
Low Output Voltage I_{OL} = +20 mA	V_{OL}	—	0.5	—	0.5	—	0.5	Vdc
High Input Voltage	V_{IH}	-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
Low Input Voltage	V_{IL}	-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc
Short Circuit Current	I_{OS}	60	150	60	150	60	150	mAdc
Reference Voltage	V_{BB}	-1.42	-1.28	-1.35	-1.23	-1.295	-1.15	Vdc

AC PARAMETERS

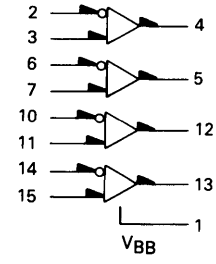
Propagation Delay*	t_{pd}	1.0	3.6	1.0	3.6	1.0	3.6	ns
Rise Time	t_r	—	2.0	—	2.0	—	2.0	ns
Fall Time	t_f	—	2.0	—	2.0	—	2.0	ns

NOTE: Each MECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

*Drives a 25 pF load.

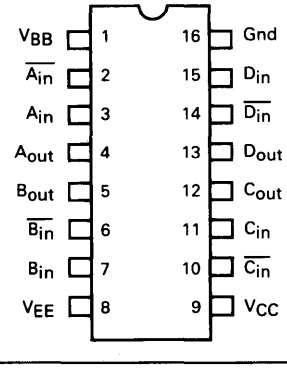
This document contains information on a new product. Specifications and information herein are subject to change without notice.

QUAD MECL-TO-TTL TRANSLATOR



Gnd = Pin 16
V_{CC} (+5.0 Vdc) = Pin 9
V_{EE} (-5.2 Vdc) = Pin 8

PIN ASSIGNMENT



APPLICATION INFORMATION

The MC10H125 incorporates differential inputs and Schottky TTL "totem pole" outputs. Differential inputs allow for use as an inverting/non-inverting translator or as a differential line receiver. The V_{BB} reference voltage is available on Pin 1 for use in single-ended input biasing. The outputs of the MC10H125 go to a low-logic level whenever the inputs are left floating.

An advantage of this device is that MECL-level information can be received, via balanced twisted pair lines, in the TTL equipment. This isolates the MECL-logic from the noisy TTL environment. Power supply requirements are ground, +5.0 volts and −5.2 volts.

MOTOROLA

MC10H130

Advance Information

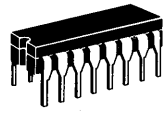
2

MECL 10KH HIGH-SPEED EMITTER-COUPLED LOGIC

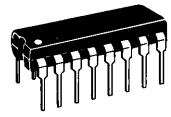
The MC10H130 is a member of Motorola's new MECL family. This MECL 10KH part is a functional/pinout duplication of the standard MECL 10K family part, with 100% improvement in clock speed and propagation delay and no increase in power-supply current.

- Propagation Delay, 1 ns Typical
- Power Dissipation, 155 mW Typical
- Improved Noise Margin 150 mV (over operating voltage and temperature range)
- Voltage Compensated
- MECL 10K-Compatible

MECL 10KH



P SUFFIX
PLASTIC PACKAGE
CASE 648



L SUFFIX
CERAMIC PACKAGE
CASE 620

MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply (V_{CC} = 0)	V_{EE}	-8.0 to 0	Vdc
Input Voltage (V_{CC} = 0)	V_I	0 to V_{EE}	Vdc
Output Current — Continuous — Surge	I_{out}	50 100	mA
Operating Temperature Range	T_A	0-75	°C
Storage Temperature Range — Plastic — Ceramic	T_{stg}	-55 to 150 -55 to 165	°C °C

ELECTRICAL CHARACTERISTICS (V_{EE} = -5.2 V ±5%) (See Note)

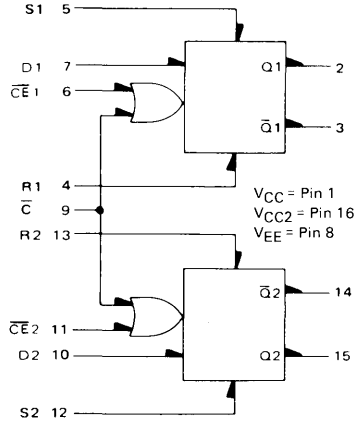
Characteristic	Symbol	0° Min	0° Max	25° Min	25° Max	75° Min	75° Max	Unit
Power Supply Current	I_E	—	38	—	35	—	38	mA
Input Current High	I_{inH}							µA
Pins 6, 11		—	468	—	275	—	275	
Pins 7, 9, 10		—	545	—	320	—	320	
Pins 4, 5, 12, 13		—	434	—	255	—	255	
Input Current Low	I_{inL}	0.5	—	0.5	—	0.3	—	µA
High Output Voltage	V_{OH}	-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
Low Output Voltage	V_{OL}	-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
High Input Voltage	V_{IH}	-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
Low Input Voltage	V_{IL}	-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc

AC PARAMETERS

Propagation Delay	t_{pd}							ns
Data, Set, Reset		0.7	2.0	0.7	1.8	0.7	2.0	
Clock		0.7	2.2	0.7	2.1	0.7	2.2	
Rise Time	t_r	0.7	2.2	0.7	2.0	0.7	2.2	ns
Fall Time	t_f	0.7	2.2	0.7	2.0	0.7	2.2	ns
Setup Time	t_{set}	2.2	—	2.2	—	2.2	—	ns
Hold Time	t_{hold}	0.7	—	0.7	—	0.7	—	ns

NOTE:
Each MECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater then 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts.

DUAL LATCH



TRUTH TABLE

D	$\overline{C}$	$\overline{CE}$	Q_{n+1}
L	L	L	L
H	L	L	H
Φ	L	H	Q_n
Φ	H	L	Q_n
Φ	H	H	Q_n

Φ = Don't Care

MECL is a trademark of Motorola Inc.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

APPLICATION INFORMATION

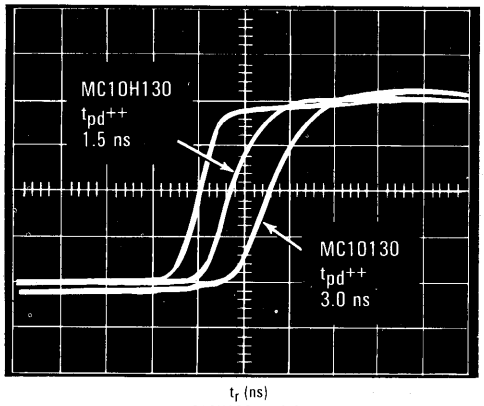
The MC10H130 is a clocked dual D type latch. Each latch may be clocked separately by holding the common clock in the low state, and using the clock enable inputs for the clocking function. If the common clock is to be used to clock the latch, the clock enable ($\overline{CE}$) inputs must be in the low state. In this mode, the enable inputs perform the function of controlling the common clock ($\overline{C}$).

Any change at the D input will be reflected at the output while the clock is low. The outputs are latched on the positive transition of the clock. While the clock is in the high state, a change in the information present at the data inputs will not affect the output information.

The set and reset inputs do not override the clock and D inputs. They are effective only when either $\overline{C}$ or $\overline{CE}$ or both are high.

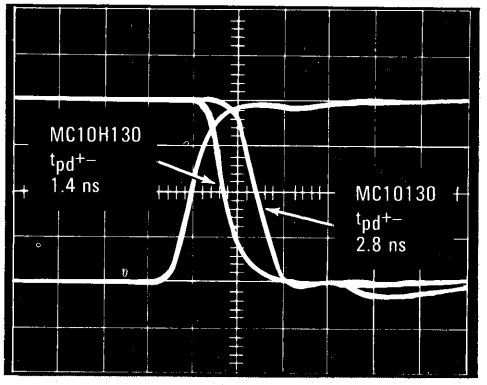
SWITCHING TIME COMPARISON
MECL 10KH versus MECL 10K

Clock to Q



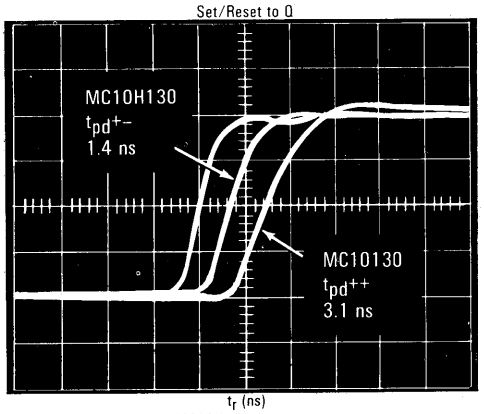
t_r (ns)
MC10H130 — 1.4 ns
MC10130 — 2.0 ns

Clock to $\overline{Q}$



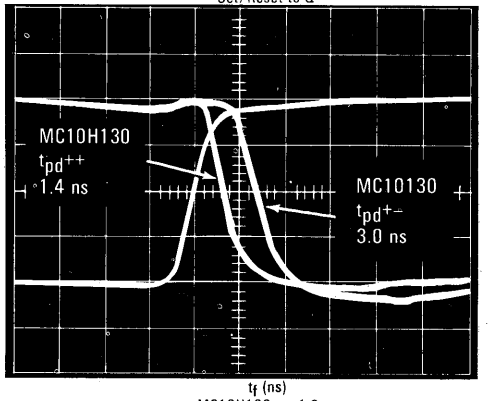
t_f (ns)
MC10H130 — 1.2 ns
MC10130 — 1.4 ns

Set/Reset to Q



t_r (ns)
MC10H130 — 1.5 ns
MC10130 — 2.1 ns

Set/Reset to $\overline{Q}$



t_f (ns)
MC10H130 — 1.2 ns
MC10130 — 1.5 ns

MOTOROLA

MC10H131

Advance Information

2

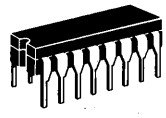
MECL 10KH HIGH-SPEED EMITTER-COUPLED LOGIC

The MC10H131 is a member of Motorola's new MECL family. This MECL 10KH part is a functional/pinout duplication of the standard MECL 10K family part, with 100% improvement in clock speed and propagation delay and no increase in power-supply current.

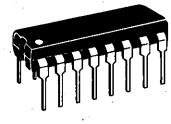
- Propagation Delay, 1 ns Typical
- Power Dissipation, 235 mW Typical
- Improved Noise Margin 150 mV (over operating voltage and temperature range)
- Voltage Compensated
- MECL 10K-Compatible

MECL 10KH

DUAL TYPE D MASTER-SLAVE FLIP FLOP



P SUFFIX
PLASTIC PACKAGE
CASE 648



L SUFFIX
CERAMIC PACKAGE
CASE 620

MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply (V_{CC} = 0)	V_{EE}	-8.0 to 0	Vdc
Input Voltage (V_{CC} = 0)	V_I	0 to V_{EE}	Vdc
Output Current — Continuous — Surge	I_{out}	50 100	mA
Operating Temperature Range	T_A	0–75	°C
Storage Temperature Range — Plastic — Ceramic	T_{stg}	-55 to 150 -55 to 165	°C °C

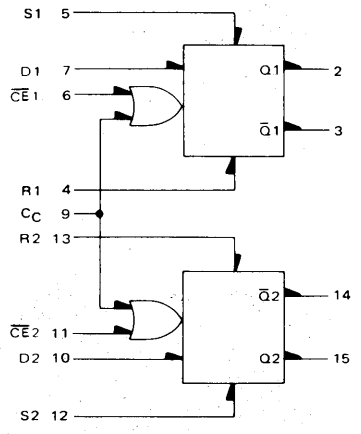
ELECTRICAL CHARACTERISTICS (V_{EE} = -5.2 V ±5%) (See Note)

Characteristic	Symbol	0°		25°		75°		Unit
		Min	Max	Min	Max	Min	Max	
Power Supply Current	I_E	—	62	—	56	—	62	mA
Input Current High	I_{inH}							µA
Pins 6, 11		—	530	—	310	—	310	
Pin 9		—	660	—	390	—	390	
Pins 7, 10		—	485	—	285	—	285	
Pins 4, 5, 12, 13		—	790	—	465	—	465	
Input Current Low	I_{inL}	0.5	—	0.5	—	0.3	—	µA
High Output Voltage	V_{OH}	-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
Low Output Voltage	V_{OL}	-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
High Input Voltage	V_{IH}	-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
Low Input Voltage	V_{IL}	-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc

AC PARAMETERS

Propagation Delay	t_{pd}							ns
Clock		0.7	2.0	0.7	2.0	0.7	2.1	
Set, Reset		0.7	2.0	0.7	2.0	0.7	2.1	
Rise Time	t_r	0.7	2.3	0.7	2.3	0.7	2.5	ns
Fall Time	t_f	0.7	2.3	0.7	2.3	0.7	2.5	ns
Setup Time	t_{set}	0.7	—	0.7	—	0.7	—	ns
Hold Time	t_{hold}	0.7	—	0.7	—	0.7	—	ns
Toggle Frequency	f_{tog}	250	—	250	—	250	—	MHz

NOTE:
Each MECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater then 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts.



MC10H131

R-S TRUTH TABLE

R	S	Q_{n+1}
L	L	Q_n
L	H	H
H	L	L
H	H	N.D.

N.D. = Not Defined

CLOCKED TRUTH TABLE

C	D	Q_{n+1}
L	ϕ	Q_n
H	L	L
H	H	H

ϕ = Don't Care
$C = \overline{C_E} + C_C$
A clock H is a clock transition from a low to a high state.

Dual D Master-Slave Flip-Flop

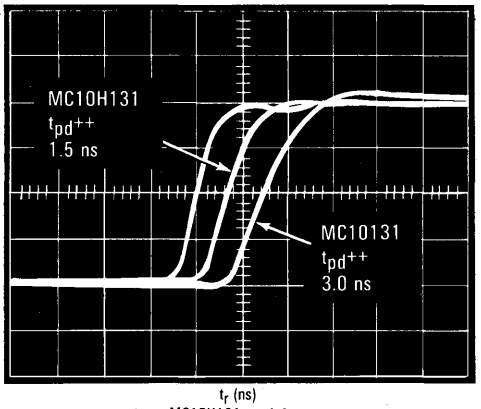
APPLICATION INFORMATION

The MC10H131 is a dual master-slave type D flip-flop. Asynchronous Set (S) and Reset (R) override Clock (C_C) and Clock Enable ($\overline{CE}$) inputs. Each flip-flop may be clocked separately by holding the common clock in the new low state and using the enable inputs for the clocking function. If the common clock is to be used to clock the flip-flop, the Clock Enable inputs must be in the low state. In this case, the enable inputs perform the function of controlling the common clock.

The output states of the flip-flop change on the positive transition of the clock. A change in the information present at the data (D) input will not affect the output information at any other time due to master slave construction.

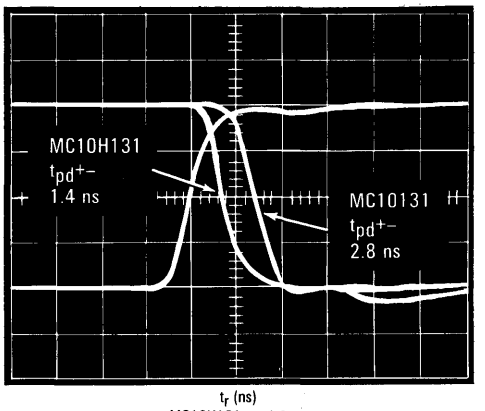
SWITCHING TIME COMPARISON
MECL 10KH versus MECL 10K

Clock to Q



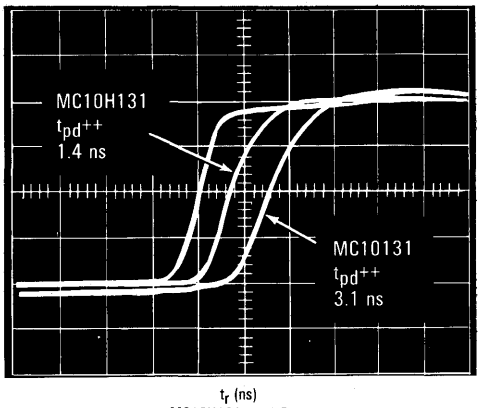
t_r (ns)
MC10H131 — 1.4 ns
MC10131 — 2.0 ns

Clock to $\overline{Q}$



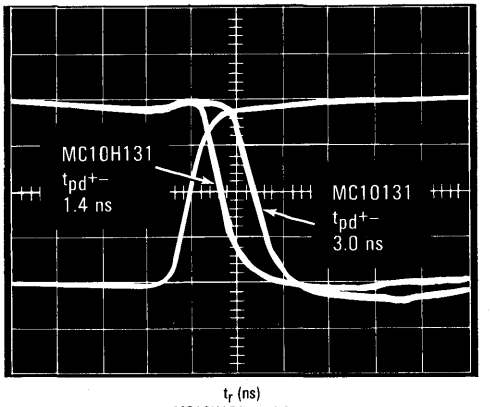
t_r (ns)
MC10H131 — 1.2 ns
MC10131 — 1.4 ns

Set/Reset to Q



t_r (ns)
MC10H131 — 1.5 ns
MC10131 — 2.1 ns

Set/Reset to $\overline{Q}$



t_r (ns)
MC10H131 — 1.2 ns
MC10131 — 1.5 ns

MOTOROLA

MC10H135

Advance Information

2

DUAL J-K MASTER SLAVE FLIP-FLOP

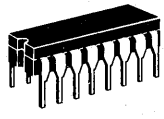
The MC10H135 is a member of Motorola's new MECL family. The MC10H135 is a dual J-K master slave flip-flop. The device is provided with an asynchronous set(s) and reset(R). These set and reset inputs overide the clock.

A common clock is provided with separate $\overline{J}$-$\overline{K}$ inputs. When the clock is static, the $\overline{JK}$ inputs do not effect the output. The output states of the flip flop change on the positive transition of the clock.

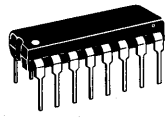
- Propagation Delay, 1.5 ns Typical
- Power Dissipation, 280 mW Typical/Pkg. (No Load)
- f_{tog} 250 MHz Max
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible

MECL 10KH

DUAL J-K MASTER SLAVE FLIP-FLOP



P SUFFIX
PLASTIC PACKAGE
CASE 648



L SUFFIX
CERAMIC PACKAGE
CASE 620

MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply (V_{CC} = 0)	V_{EE}	-8.0 to 0	Vdc
Input Voltage (V_{CC} = 0)	V_I	0 to V_{EE}	Vdc
Output Current — Continuous — Surge	I_{out}	50 100	mA
Operating Temperature Range	T_A	0 to +75	°C
Storage Temperature Range — Plastic — Ceramic	T_{stg}	-55 to +150 -55 to +165	°C °C

ELECTRICAL CHARACTERISTICS (V_{EE} = -5.2 V ±5%) (See Note)

Characteristic	Symbol	0°		25°		75°		Unit
		Min	Max	Min	Max	Min	Max	
Power Supply Current	I_E	—	75	—	68	—	75	mA
Input Current High Pins 6, 7, 10, 11 Pins 4, 5, 12, 13 Pin 9	I_{inH}	 — — —	 460 800 675	 — — —	 285 500 420	 — — —	 285 500 420	μA
Input Current Low	I_{inL}	0.5	—	0.5	—	0.3	—	μA
High Output Voltage	V_{OH}	-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
Low Output Voltage	V_{OL}	-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
High Input Voltage	V_{IH}	-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
Low Input Voltage	V_{IL}	-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc

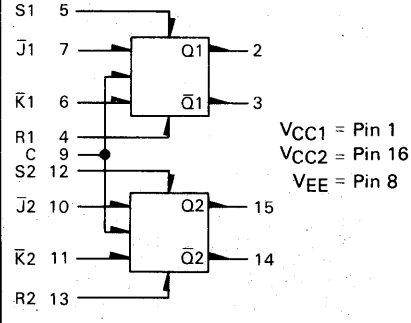
AC PARAMETERS

Propagation Delay Set, Reset, Clock	t_{pd}	0.7	2.6	0.7	2.3	0.7	2.6	ns
Rise Time	t_r	0.7	2.2	0.7	2.0	0.7	2.2	ns
Fall Time	t_f	0.7	2.2	0.7	2.0	0.7	2.2	ns
Set-up Time	t_{set}	1.5	—	1.5	—	1.5	—	ns
Hold Time	t_{hold}	1.0	—	1.0	—	1.0	—	ns
Toggle Frequency	f_{tog}		250		250		250	MHz

NOTE:
Each MECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Outputs are terminated through a 50 ohm resistor to -2.0 volts.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

LOGIC DIAGRAM



R-S TRUTH TABLE

R	S	Q_{n+1}
L	L	Q_n
L	H	H
H	L	L
H	H	N.D.

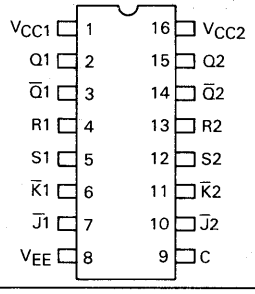
N.D. = Not Defined

CLOCK J-K TRUTH TABLE*

J	K	Q_{n+1}
L	L	Q_n
H	L	L
L	H	H
H	H	Q_n

*Output states change on positive transition of clock for $\overline{J}$-$\overline{K}$ input condition present.

PIN ASSIGNMENT



MOTOROLA

MC10H136

Advance Information

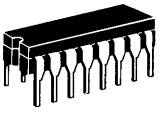
MECL 10KH HIGH-SPEED EMITTER-COUPLED LOGIC

The MC10H136 is a member of Motorola's new MECL family. The MC10H136 is a high speed synchronous hexadecimal counter. This 10KH part is a functional/pinout duplication of the standard MECL 10K family part, with 100% improvement in counting frequency and no increase in power-supply current.

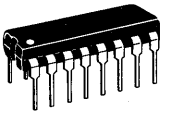
- Counting frequency, 250 MHz minimum
- Power Dissipation, 625 mW Typical
- Improved Noise Margin 150 mV (over operating voltage and temperature range)
- Voltage Compensated
- MECL 10K-Compatible

MECL 10KH

UNIVERSAL HEXADECIMAL COUNTER



P SUFFIX
PLASTIC PACKAGE
CASE 648



L SUFFIX
CERAMIC PACKAGE
CASE 620

MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply (V_{CC} = 0)	V_{EE}	-8.0 to 0	Vdc
Input Voltage (V_{CC} = 0)	V_I	0 to V_{EE}	Vdc
Output Current — Continuous — Surge	I_{out}	50 100	mA
Operating Temperature Range	T_A	0–75	°C
Storage Temperature Range — Plastic — Ceramic	T_{stg}	-55 to 150 -55 to 165	°C °C

ELECTRICAL CHARACTERISTICS (V_{EE} = -5.2 V ±5%) (See Note)

Characteristic	Symbol	0°		25°		75°		Unit
		Min	Max	Min	Max	Min	Max	
Power Supply Current	I_E	—	165	—	150	—	165	mA
Input Current High	I_{inH}							μA
Pins 5, 6, 11, 12, 13		—	430	—	275	—	275	
Pin 9		—	670	—	420	—	420	
Pin 7		—	535	—	335	—	335	
Pin 10		—	380	—	240	—	240	
Input Current Low	I_{inL}	0.5	—	0.5	—	0.3	—	μA
High Output Voltage	V_{OH}	-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
Low Output Voltage	V_{OL}	-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
High Input Voltage	V_{IH}	-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
Low Input Voltage	V_{IL}	-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc

AC PARAMETERS

Propagation Delay	t_{pd}							ns
Clock to Q		0.7	3.5	0.7	3.2	0.7	3.5	
Clock to Carry Out		0.7	7.7	0.7	7.0	0.7	7.7	
Carry in to Carry Out		0.7	3.5	0.7	3.0	0.7	3.5	
Set-up Time	t_{set}							ns
Data (D0 to C)		2.0	—	2.0	—	2.0	—	
Select (S to C)		3.5	—	3.5	—	3.5	—	
Carry In (C_{in} to C)		2.0	—	2.0	—	2.0	—	
(C to C_{in})		0	—	0	—	0	—	
Hold Time	t_{hold}							ns
Data (C to D0)		0	—	0	—	0	—	
Select (C to S)		-0.5	—	-0.5	—	-0.5	—	
Carry In (C to C_{in})		0	—	0	—	0	—	
(C_{in} to C)		2.2	—	2.2	—	2.2	—	
Counting Frequency	f_{count}	250	—	250	—	250	—	MHz
Rise Time	t_r	0.7	2.3	0.7	2.1	0.7	2.3	ns
Fall Time	t_f	0.7	2.3	0.7	2.1	0.7	2.3	ns

NOTE:
Each MECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater then 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts.

FUNCTION SELECT TABLE

S1	S2	Operating Mode
L	L	Preset (Program)
L	H	Increment (Count Up)
H	L	Decrement (Count Down)
H	H	Hold (Stop Count)

SEQUENTIAL TRUTH TABLE*

INPUTS								OUTPUTS				
S1	S2	D0	D1	D2	D3	$\overline{\text{Carry In}}$	Clock **	Q0	Q1	Q2	Q3	$\overline{\text{Carry Out}}$
L	L	L	L	H	H	ϕ	H	L	L	H	H	L
L	H	ϕ	ϕ	ϕ	ϕ	L	H	H	L	H	H	H
L	H	ϕ	ϕ	ϕ	ϕ	L	H	L	H	H	H	H
L	H	ϕ	ϕ	ϕ	ϕ	L	H	H	H	H	H	L
L	H	ϕ	ϕ	ϕ	ϕ	H	L	H	H	H	H	H
L	H	ϕ	ϕ	ϕ	ϕ	H	H	H	H	H	H	H
H	H	ϕ	ϕ	ϕ	ϕ	ϕ	H	H	H	H	H	H
L	L	H	H	L	L	ϕ	H	H	H	L	L	L
H	L	ϕ	ϕ	ϕ	ϕ	L	H	L	H	L	L	H
H	L	ϕ	ϕ	ϕ	ϕ	L	H	H	L	L	L	H
H	L	ϕ	ϕ	ϕ	ϕ	L	H	L	L	L	L	L
H	L	ϕ	ϕ	ϕ	ϕ	L	H	H	H	H	H	H

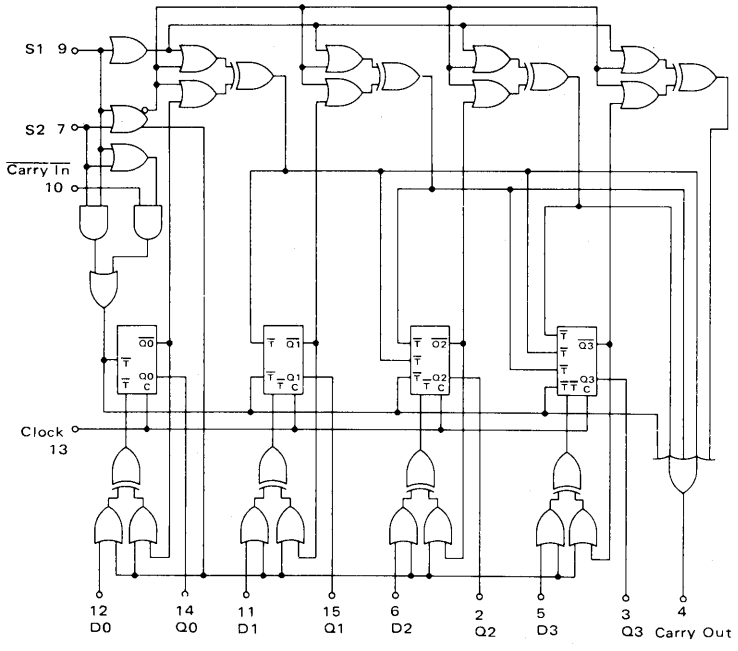
ϕ = Don't care.
* Truth table shows logic states assuming inputs vary in sequence shown from top to bottom.
** A clock H is defined as a clock input transition from a low to a high logic level.

MECL is a trademark of Motorola Inc.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

2

HEXADECIMAL COUNTER



APPLICATION INFORMATION

The MC10H136 is a high speed synchronous counter that operates at 250 MHz. Counter operating modes include count up, count down, pre-set and hold count. This device allows the designer to use one basic counter for many applications.

The S1, S2, control lines determine the operating modes of the counter. In the pre-set mode, a clock pulse is necessary to load the counter with the information present on the data inputs (D0, D1, D2, and D3). Carry out goes low on the terminal count or when the counter is being pre-set.

MOTOROLA

MC10H141

Advance Information

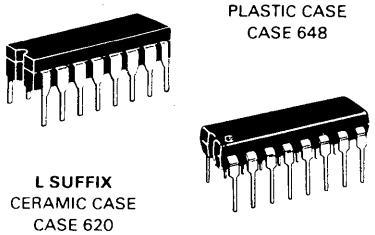
MECL 10KH HIGH-SPEED EMITTER-COUPLED LOGIC

The MC10H141 is a four-bit universal shift register. This device is a functional/pinout duplication of the standard MECL 10K part with 100% improvement in propagation delay and operation frequency and no increase in power supply current.

- Shift frequency, 250 MHz Min
- Power Dissipation, 425 mW Typical
- Improved Noise Margin 150 mV (over operating voltage and temperature range)
- Voltage Compensated
- MECL 10K-Compatible

MECL 10KH

2



P SUFFIX
PLASTIC CASE
CASE 648

L SUFFIX
CERAMIC CASE
CASE 620

MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply (V_{CC} = 0)	V_{EE}	−8.0 to 0	Vdc
Input Voltage (V_{CC} = 0)	V_I	0 to V_{EE}	Vdc
Output Current — Continuous — Surge	I_{out}	50 100	mA
Operating Temperature Range	T_A	0–75	°C
Storage Temperature Range — Plastic — Ceramic	T_{stg}	−55 to 150 −55 to 165	°C °C

ELECTRICAL CHARACTERISTICS (V_{EE} = −5.2 V ± 5%)

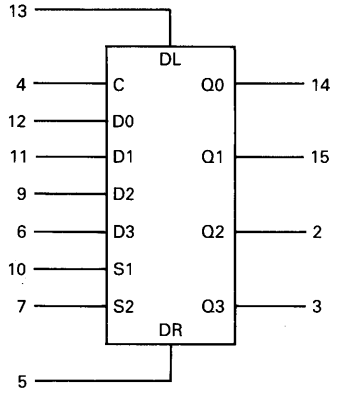
Characteristic	Symbol	0° Min	0° Max	25° Min	25° Max	75° Min	75° Max	Unit
Power Supply Current	I_E		112		102		112	mA
Input Current High Pins 5, 6, 9, 11, 12, 13 Pin 7,10 Pin 4	I_{inH}	 — — —	 405 416 510	 — — —	 255 260 320	 — — —	 255 260 320	µA
Input Current Low	I_{inL}	0.5	—	0.5	—	0.3	—	µA
High Output Voltage	V_{OH}	−1.02	−0.84	−0.98	−0.81	−0.92	−0.735	Vdc
Low Output Voltage	V_{OL}	−1.95	−1.63	−1.95	−1.63	−1.95	−1.60	Vdc
High Input Voltage	V_{IH}	−1.17	−0.84	−1.13	−0.81	−1.07	−0.735	Vdc
Low Input Voltage	V_{IL}	−1.95	−1.48	−1.95	−1.48	−1.95	−1.45	Vdc

AC PARAMETERS

Propagation Delay	t_{pd}	1.1	2.0	1.0	1.9	1.1	2.1	ns
Hold Time	t_{hold}	1.0	—	1.0	—	1.0	—	ns
Set up Time Data Select	t_{set}	 1.5 3.0	 — —	 1.5 3.0	 — —	 1.5 3.0	 — —	ns
Rise Time Fall Time	t_r t_f	0.7 0.7	2.4 2.3	0.7 0.7	2.2 2.2	0.7 0.7	2.4 2.4	ns
Shift Frequency	f_{shift}	250	—	250	—	250	—	MHz

NOTE:
Each MECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts.

Four-Bit Universal Shift Register



V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

TRUTH TABLE

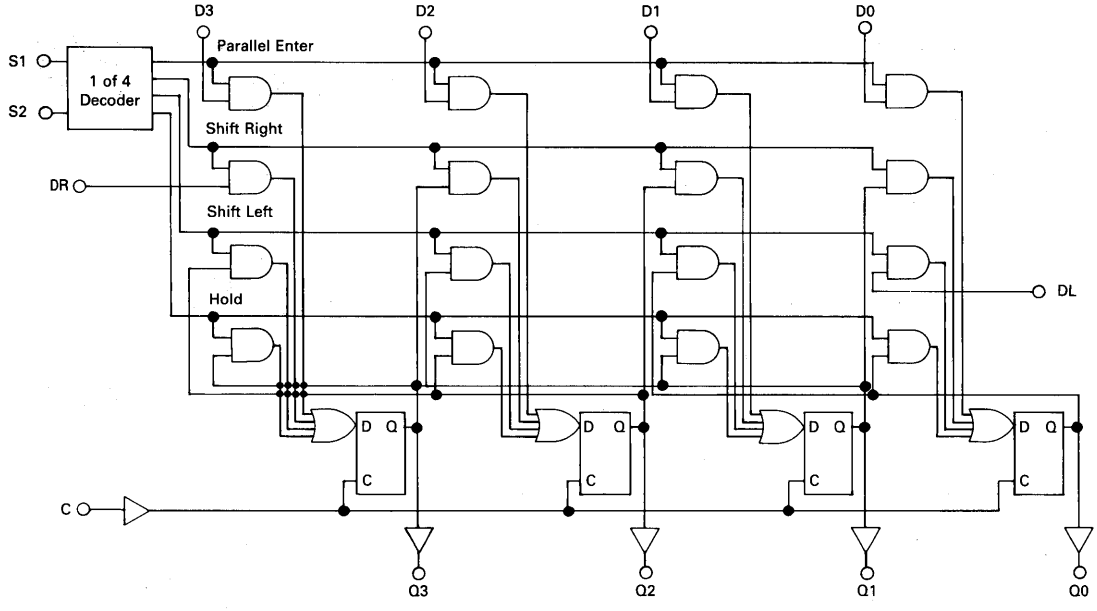
SELECT S1	SELECT S2	OPERATING MODE	OUTPUTS $Q0_{n+1}$	$Q1_{n+1}$	$Q2_{n+1}$	$Q3_{n+1}$
L	L	Parallel Entry	D0	D1	D2	D3
L	H	Shift Right*	$Q1_n$	$Q2_n$	$Q3_n$	DR
H	L	Shift Left*	DL	$Q0_n$	$Q1_n$	$Q2_n$
H	H	Stop Shift	$Q0_n$	$Q1_n$	$Q2_n$	$Q3_n$

* Outputs as exist after pulse appears at "C" input with input conditions as shown (Pulse Positive transition of clock input).

This document contains information on a new product. Specifications and information herein are subject to change without notice.

2

LOGIC DIAGRAM



APPLICATION INFORMATION

The MC10H141 is a four-bit universal shift register which performs shift left, or shift right, serial/parallel in, and serial/parallel out operations with no external gating. Inputs S1 and S2 control the four possible operations of the register without external gating of the clock. The flip-flops shift information on the positive edge of the clock. The four operations are stop shift, shift left, shift right, and parallel entry of data. The other six inputs are all data type inputs; four for parallel entry data, and one for shifting in from the left (DL) and one for shifting in from the right (DR).

MOTOROLA

MC10H145

Advance Information

MECL 10KH HIGH-SPEED EMITTER-COUPLED LOGIC

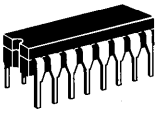
The MC10H145 is a member of Motorola's new MECL family. The MC10H145 is a 16 × 4 bit register file. The active-low chip select allows easy expansion.

The operating mode of the register file is controlled by the $\overline{WE}$ input. When $\overline{WE}$ is "low" the device is in the write mode, the outputs are "low" and the data present at D_n input is stored at the selected address. when $\overline{WE}$ is "high", the device is in the read mode — the data state at the selected location is present at the Q_n outputs.

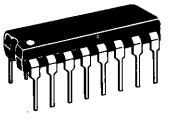
- Address Access Time, 3.5 ns Typical
- Power Dissipation, 700 mW Typical
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible

MECL 10KH

16 × 4 BIT REGISTER FILE



P SUFFIX
PLASTIC PACKAGE
CASE 648



L SUFFIX
CERAMIC PACKAGE
CASE 620

MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply (V_{CC} = 0)	V_{EE}	-8.0 to 0	Vdc
Input Voltage (V_{CC} = 0)	V_I	0 to V_{EE}	Vdc
Output Current — Continuous — Surge	I_{out}	50 100	mA
Operating Temperature Range	T_A	0 to +75	°C
Storage Temperature Range — Plastic — Ceramic	T_{stg}	-55 to +150 -55 to +165	°C

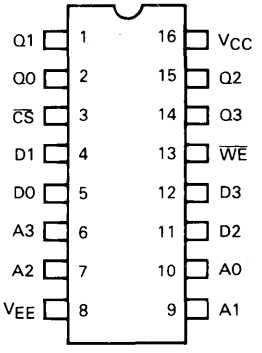
ELECTRICAL CHARACTERISTICS (V_{EE} = -5.2 V ± 5%) (See Note)

Characteristic	Symbol	0°		25°		75°		Unit
		Min	Max	Min	Max	Min	Max	
Power Supply Current	I_E	—	165	—	150	—	165	mA
Input Current High	I_{inH}	—	375	—	220	—	220	μA
Input Current Low	I_{inL}	0.5	—	0.5	—	0.3	—	μA
High Output Voltage	V_{OH}	-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
Low Output Voltage	V_{OL}	-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
High Input Voltage	V_{IH}	-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
Low Input Voltage	V_{IL}	-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc

NOTE:
Each MECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts.

This document contains information on a new product. Specifications and information herein are subject to change without notice. MECL, MECL 10K and MECL 10KH are trademarks of Motorola Inc.

PIN ASSIGNMENT



TRUTH TABLE

MODE	INPUT			OUTPUT
	$\overline{CS}$	$\overline{WE}$	D_n	Q_n
Write "0"	L	L	L	L
Write "1"	L	L	H	L
Read	L	H	ϕ	Q
Disabled	H	ϕ	ϕ	L

ϕ = Don't Care

Q-State of Addressed Cell

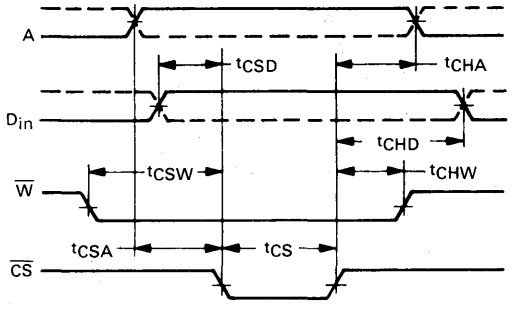
2

AC PARAMETERS

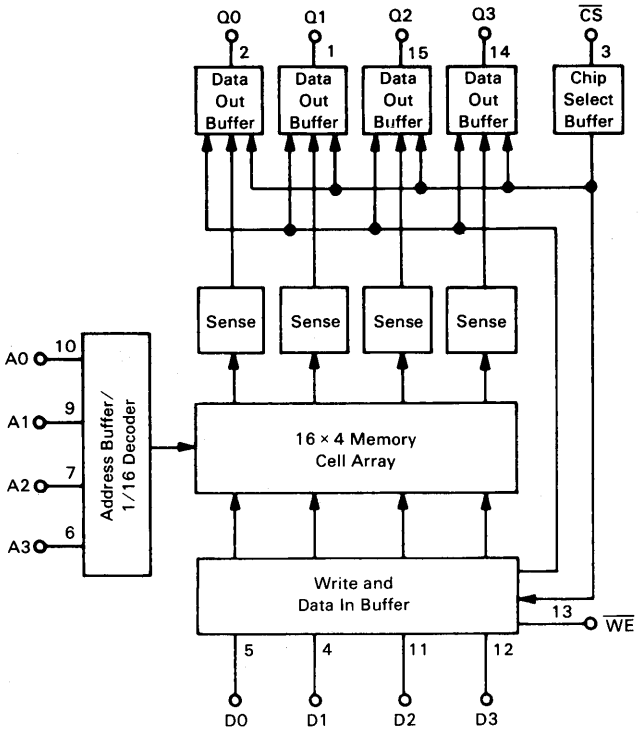
Characteristics	Symbol	MC10H145 T_A = 0 to +75°C, V_{EE} = -5.2 Vdc ±5% Min	Max	Unit	Conditions
Read Mode				ns	Measured from 50% of input to 50% of output. See Note 2.
Chip Select Access Time	t_{ACS}	1.0	4.0		
Chip Select Recovery Time	t_{RCS}	1.0	4.0		
Address Access Time	t_{AA}	2.0	6.0		
Write Mode				ns	t_{WSA} = 3.5 ns
Write Pulse Width	t_W	4.0	—		Measured at 50% of input to 50% of output. t_W = 4.0 ns.
Data Setup Time Prior to Write	t_{WSD}	0	—		
Data Hold Time After Write	t_{WHD}	1.5	—		
Address Setup Time Prior to Write	t_{WSA}	3.5	—		
Address Hold Time After Write	t_{WHA}	0.5	—		
Chip Select Setup Time Prior to Write	t_{WSCS}	0	—		
Chip Select Hold Time After Write	t_{WHCS}	1.5	—		
Write Disable Time	t_{WS}	1.0	6.0		
Write Recovery Time	t_{WR}	1.0	6.0		
Chip Enable Strobe Mode				ns	Guaranteed but not tested on standard product. See Figure 1.
Data Setup Prior to Chip Select	t_{CSD}	0	—		
Write Enable Setup Prior to Chip Select	t_{CSW}	0	—		
Address Setup Prior to Chip Select	t_{CSA}	0	—		
Data Hold Time After Chip Select	t_{CHD}	1.0	—		
Write Enable Hold Time After Chip Select	t_{CHW}	0	—		
Address Hold Time After Chip Select	t_{CHA}	2.0	—		
Chip Select Minimum Pulse Width	t_{CS}	10	—		
Rise and Fall Time	t_r, t_f			ns	Measured between 20% and 80% points.
Address to Output		0.7	2.5		
CS to Output		0.7	2.5		
Capacitance				pF	Measured with a pulse technique.
Input Capacitance	C_{in}	—	6.0		
Output Capacitance	C_{out}	—	8.0		

NOTES: 1. Test circuit characteristics: R_T = 50 Ω, MC10H145. $C_L \leq 5.0$ pF (including jig and Stray Capacitance). Delay should be derated 30 ps/pF for capacitive loads up to 50 pF.
2. The maximum Address Access Time is guaranteed to be the worst-case bit in the memory.
3. For proper use of MECL in a system environment, consult MECL System Design Handbook.

FIGURE 1 — CHIP ENABLE STROBE MODE



16 × 4 Bit Register File



MOTOROLA

MC10H158

Advance Information

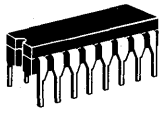
2

MECL 10KH HIGH-SPEED EMITTER-COUPLED LOGIC

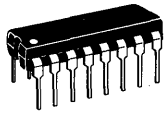
The MC10H158 is a member of Motorola's new MECL family. The MC10H158 is a quad two channel multiplexer with common input select. A "high" level select enables input D00, D10, D20 and D30 and a "low" level select enables input D01, D11, D21 and D31. This MECL 10KH part is a functional/pinout duplication of the standard MECL 10K family part, with 100% improvement in propagation delay and no increase in power-supply current.

- Propagation Delay, 1.5 ns Typical
- Power Dissipation, 197 mW Typical
- Improved Noise Margin 150 mV (over operating voltage and temperature range)
- Voltage Compensated
- MECL 10K-Compatible

MECL 10KH

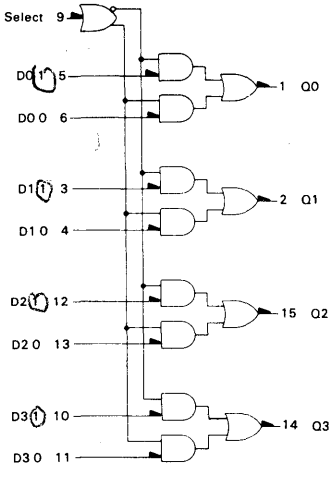


P SUFFIX
PLASTIC PACKAGE
CASE 648



L SUFFIX
CERAMIC PACKAGE
CASE 620

Quad 2-Input Multiplexer



V_{CC} = Pin 16
V_{EE} = Pin 8

MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply (V_{CC} = 0)	V_{EE}	-8.0 to 0	Vdc
Input Voltage (V_{CC} = 0)	V_I	0 to V_{EE}	Vdc
Output Current — Continuous — Surge	I_{out}	50 100	mA
Operating Temperature Range	T_A	0-75	°C
Storage Temperature Range — Plastic — Ceramic	T_{stg}	-55 to 150 -55 to 165	°C °C

ELECTRICAL CHARACTERISTICS (V_{EE} = -5.2 V ±5%)

Characteristic	Symbol	0°		25°		75°		Unit
		Min	Max	Min	Max	Min	Max	
Power Supply Current	I_E	—	53	—	48	—	53	mA
Input Current High Pin 9 Pins 3-6 and 10-13	I_{inH}	 — —	 475 515	 — —	 295 320	 — —	 295 320	µA
Input Current Low	I_{inL}	0.5	—	0.5	—	0.3	—	µA
High Output Voltage	V_{OH}	-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
Low Output Voltage	V_{OL}	-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
High Input Voltage	V_{IH}	-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
Low Input Voltage	V_{IL}	-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc

AC PARAMETERS

Propagation Delay Data Select	t_{pd}	 1.0 1.0	 1.9 2.9	 1.0 1.0	 1.8 2.7	 1.0 1.0	 2.0 2.9	ns
Rise Time	t_r	0.7	2.2	0.7	2.0	0.7	2.2	ns
Fall Time	t_f	0.7	2.2	0.7	2.0	0.7	2.2	ns

NOTE:
Each MECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater then 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

TRUTH TABLE

Select	D0	D1	Q
L	ϕ	L	L
L	ϕ	H	H
H	L	ϕ	L
H	H	ϕ	H

ϕ = Don't care

MOTOROLA

MC10H159

Advance Information

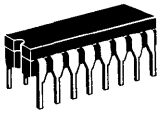
MECL 10KH

2

MECL 10KH HIGH-SPEED EMITTER-COUPLED LOGIC

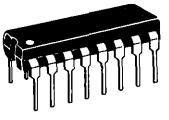
The MC10H159 is a member of Motorola's new MECL family. The MC10H159 is a quad 2-input multiplexer with enable. This MECL 10KH part is a functional/pinout duplication of the standard MECL 10K family part, with 100% improvement in propagation delay and no increase in power-supply current.

- Propagation Delay, 1.5 ns Typical
- Power Dissipation, 218 mW Typical
- Improved Noise Margin 150 mV (over operating voltage and temperature range)
- Voltage Compensated
- MECL 10K-Compatible

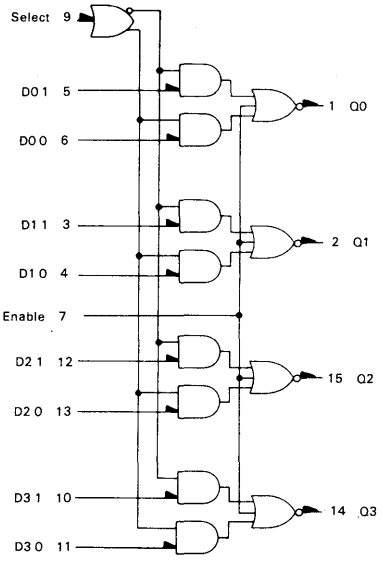


P SUFFIX
PLASTIC PACKAGE
CASE 648

L SUFFIX
CERAMIC PACKAGE
CASE 620



QUAD 2-INPUT MULTIPLEXER



V_{CC} Pin 16
V_{EE} Pin 8

MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply (V_{CC} = 0)	V_{EE}	-8.0 to 0	Vdc
Input Voltage (V_{CC} = 0)	V_I	0 to V_{EE}	Vdc
Output Current — Continuous — Surge	I_{out}	50 100	mA
Operating Temperature Range	T_A	0-75	°C
Storage Temperature Range — Plastic — Ceramic	T_{stg}	-55 to 150 -55 to 165	°C °C

ELECTRICAL CHARACTERISTICS (V_{EE} = -5.2 V ±5%) (See Note)

Characteristic	Symbol	0°		25°		75°		Unit
		Min	Max	Min	Max	Min	Max	
Power Supply Current	I_E	—	58	—	53	—	58	mA
Input Current High Pin 9 Pins 3-7 and 10-13	I_{inH}	 — —	 475 515	 — —	 295 320	 — —	 295 320	μA
Input Current Low	I_{inL}	0.5	—	0.5	—	0.3	—	μA
High Output Voltage	V_{OH}	-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
Low Output Voltage	V_{OL}	-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
High Input Voltage	V_{IH}	-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
Low Input Voltage	V_{IL}	-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc

AC PARAMETERS

Propagation Delay Data Select Enable	t_{pd}	 1.0 1.0 1.0	 2.2 3.2 3.2	 1.0 1.0 1.0	 2.0 3.0 3.0	 1.0 1.0 1.0	 2.2 3.2 3.2	ns
Rise Time	t_r	0.7	2.2	0.7	2.0	0.7	2.2	ns
Fall Time	t_f	0.7	2.2	0.7	2.0	0.7	2.2	ns

NOTE:
Each MECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater then 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts.

TRUTH TABLE

Enable	Select	D0	D1	Q
L	L	ϕ	L	H
L	L	ϕ	H	L
L	H	L	ϕ	H
L	H	H	ϕ	L
H	ϕ	ϕ	ϕ	L

ϕ = Don't Care

This document contains information on a new product. Specifications and information herein are subject to change without notice.

APPLICATION INFORMATION

The MC10H159 is a quad two channel multiplexer with enable. It incorporates common enable and common data select inputs. The select input determines which data inputs are enabled. A high (H) level enables data inputs D0 0, D1 0, D2 0, and D3 0. A low (L) level enables data inputs D0 1, D1 1, D2 1, and D3 1. Any change on the data inputs will be reflected at the outputs while the enable is low. Input levels are inverted at the output.

MOTOROLA

MC10H160

Advance Information

MECL 10KH HIGH-SPEED EMITTER-COUPLED LOGIC

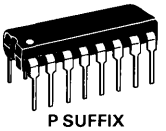
The MC10H160 is a member of Motorola's new MECL family. The MC10H160 is a 12-bit parity generator-checker. The output goes high when an odd number of inputs are high providing the odd parity function. Unconnected inputs are pulled to a logic low allowing parity detection and generation for less than 12 bits. The MC10H160 is a functional pin duplication of the standard 10K family part with 100% improvement in propagation delay and no increase in power-supply current.

- Propagation Delay, 2.5 ns Typical
- Power Dissipation, 320 mW Typical
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible

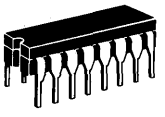
MECL 10KH

12-BIT PARITY GENERATOR-CHECKER

2



L SUFFIX
CERAMIC PACKAGE
CASE 620



P SUFFIX
PLASTIC PACKAGE
CASE 648

MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply (V_{CC} = 0)	V_{EE}	-8.0 to 0	Vdc
Input Voltage (V_{CC} = 0)	V_I	0 to V_{EE}	Vdc
Output Current — Continuous — Surge	I_{out}	50 100	mA
Operating Temperature Range	T_A	0–+75	°C
Storage Temperature Range — Plastic — Ceramic	T_{stg}	-55 to +150 -55 to +165	°C °C

ELECTRICAL CHARACTERISTICS (V_{EE} = -5.2 V ±5%) (See Note)

Characteristic	Symbol	0°		25°		75°		Unit
		Min	Max	Min	Max	Min	Max	
Power Supply Current	I_E	—	88	—	78	—	86	mA
Input Current High Pins 3,5,7,10,12,14 Pins 4,6,9,11,13,15	I_{inH}	 — —	 391 457	 — —	 246 285	 — —	 246 285	μA
Input Current Low	I_{inL}	0.5	—	0.5	—	0.3	—	μA
High Output Voltage	V_{OH}	-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
Low Output Voltage	V_{OL}	-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
High Input Voltage	V_{IH}	-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
Low Input Voltage	V_{IL}	-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc

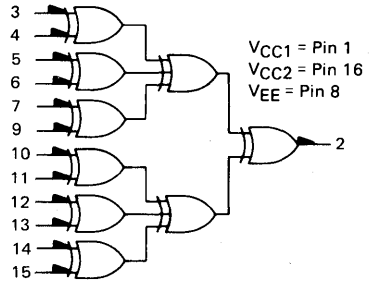
AC PARAMETERS

Propagation Delay	t_{pd}	0.7	4.8	0.7	4.5	0.7	4.8	ns
Rise Time	t_r	0.7	2.0	0.7	1.9	0.7	2.0	ns
Fall Time	t_f	0.7	1.5	0.7	1.4	0.7	1.45	ns

NOTE:
Each MECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Outputs are terminated through a 50 ohm resistor to -2.0 volts.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

LOGIC DIAGRAM



TRUTH TABLE

INPUT	OUTPUT
Sum of High Level Inputs	Pin 2
Even	Low
Odd	High

MOTOROLA

MC10H161

Advance Information

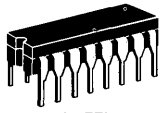
2

MECL 10KH HIGH-SPEED EMITTER-COUPLED LOGIC

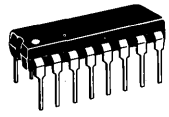
The MC10H161 is a member of Motorola's new MECL family. This part provides parallel decoding of a three bit binary word to one of eight lines. The MC10H161 is useful in high-speed multiplexer/demultiplexer applications.

- Propagation Delay, 1 ns Typical
- Power Dissipation 315 mW Typical (same as MECL 10K)
- Improved Noise Margin 150 mV (over operating voltage and temperature range)
- Voltage Compensated
- MECL 10K-Compatible.

MECL 10KH

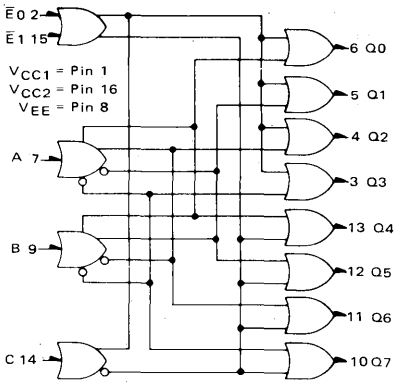


L SUFFIX
CERAMIC PACKAGE
CASE 620



P SUFFIX
PLASTIC PACKAGE
CASE 648

Binary to 1-of-8 Decoder



TRUTH TABLE

ENABLE INPUTS		INPUTS			OUTPUTS							
$\overline{E}1$	$\overline{E}0$	C	B	A	Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7
L	L	L	L	L	L	H	H	H	H	H	H	H
L	L	L	L	H	H	L	H	H	H	H	H	H
L	L	L	H	L	H	H	L	H	H	H	H	H
L	L	L	H	H	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	L	H	H	H
L	L	H	L	H	H	H	H	H	H	L	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	L
H	ϕ	ϕ	ϕ	ϕ	H	H	H	H	H	H	H	H
ϕ	H	ϕ	ϕ	ϕ	H	H	H	H	H	H	H	H

ϕ = Don't Care

The MC10H161 is designed to decode a three bit input word to one of eight output lines. The MC10H161 output will be low when selected while all other output are high. The enable inputs, when either or both are high, force all outputs high.

The MC10H161 is a true parallel decoder. This eliminates unequal parallel path delay times found in other decoder designs. These devices are ideally suited for multiplexer/demultiplexer applications.

MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply (V_{CC} = 0)	V_{EE}	-8.0 to 0	Vdc
Input Voltage (V_{CC} = 0)	V_I	0 to V_{EE}	Vdc
Output Current — Continuous — Surge	I_{out}	50 100	mA
Operating Temperature Range	T_A	0–75	°C
Storage Temperature Range — Plastic — Ceramic	T_{stg}	-55 to 150 -55 to 165	°C °C

ELECTRICAL CHARACTERISTICS (V_{EE} = -5.2 V ±5%) (See Note)

Characteristic	Symbol	0°		25°		75°		Unit
		Min	Max	Min	Max	Min	Max	
Power Supply Current	I_E	—	84	—	76	—	84	mA
Input Current High	I_{inH}	—	465	—	275	—	275	μA
Input Current Low	I_{inL}	0.5	—	0.5	—	0.3	—	μA
High Output Voltage	V_{OH}	-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
Low Output Voltage	V_{OL}	-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
High Input Voltage	V_{IH}	-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
Low Input Voltage	V_{IL}	-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc

AC PARAMETERS

Propagation Delay	t_{pd}	0.7	3.1	0.7	3.0	0.7	3.2	ns
Rise Time	t_r	0.7	2.2	0.7	2.0	0.7	2.2	ns
Fall Time	t_f	0.7	2.2	0.7	2.0	0.7	2.2	ns

NOTE:
Each MECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater then 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

TYPICAL APPLICATIONS

FIGURE 1 — HIGH SPEED 16-BIT MULTIPLEXER/DEMULTIPLEXER

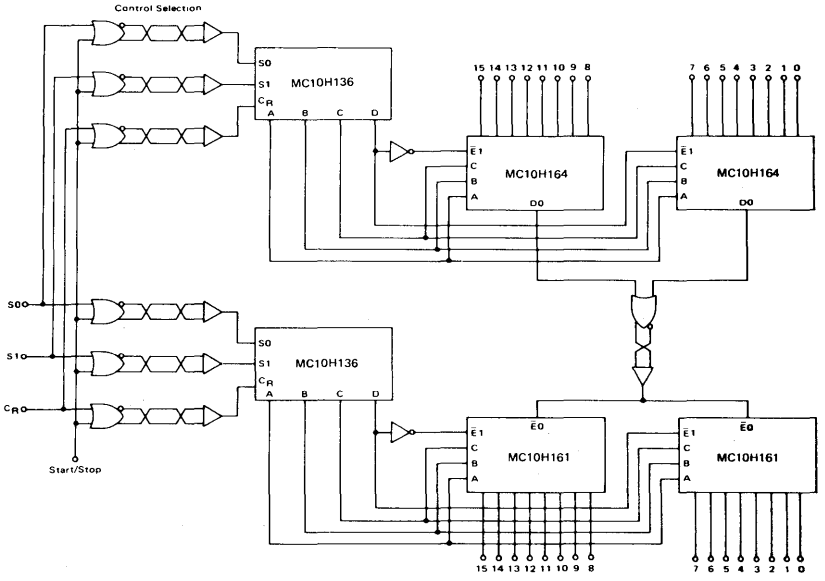
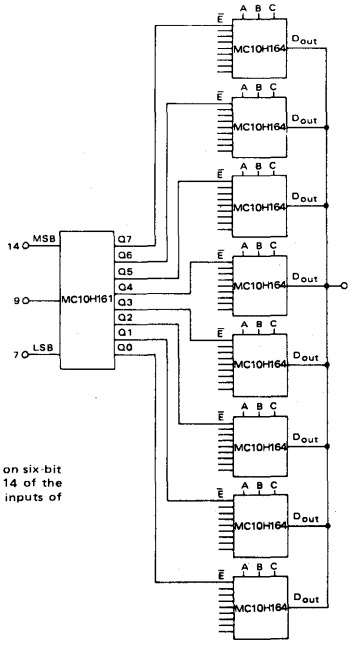


FIGURE 2 — 1-OF-64 LINE MULTIPLEXER



The Bit chosen is dependent on six-bit code present on inputs 7, 9, 14 of the MC10H161 and the A, B, C inputs of the MC10H164.

MOTOROLA

MC10H162

Advance Information

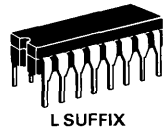
2

MECL 10KH HIGH-SPEED EMITTER-COUPLED LOGIC

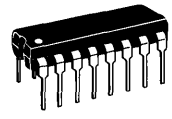
The MC10H162 is a member of Motorola's new MECL family. This part provides parallel decoding of a three bit binary word to one of eight lines. The MC10H162 is useful in high-speed multiplexer/demultiplexer applications.

- Propagation Delay, 1 ns Typical
- Power Dissipation 315 mW Typical (same as MECL 10K)
- Improved Noise Margin 150 mV (over operating voltage and temperature range)
- Voltage Compensated
- MECL 10K-Compatible.

MECL 10KH

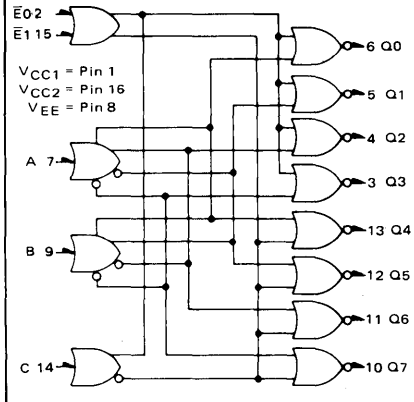


L SUFFIX
CERAMIC PACKAGE
CASE 620



P SUFFIX
PLASTIC PACKAGE
CASE 648

Binary to 1-of-8 Decoder



MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply (V_{CC} = 0)	V_{EE}	-8.0 to 0	Vdc
Input Voltage (V_{CC} = 0)	V_I	0 to V_{EE}	Vdc
Output Current — Continuous — Surge	I_{out}	50 100	mA
Operating Temperature Range	T_A	0–75	°C
Storage Temperature Range — Plastic — Ceramic	T_{stg}	-55 to 150 -55 to 165	°C °C

ELECTRICAL CHARACTERISTICS (V_{EE} = -5.2 V ±5%) (See Note)

Characteristic	Symbol	0° Min	0° Max	25° Min	25° Max	75° Min	75° Max	Unit
Power Supply Current	I_E	—	84	—	76	—	84	mA
Input Current High	I_{inH}	—	465	—	275	—	275	μA
Input Current Low	I_{inL}	0.5	—	0.5	—	0.3	—	μA
High Output Voltage	V_{OH}	-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
Low Output Voltage	V_{OL}	-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
High Input Voltage	V_{IH}	-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
Low Input Voltage	V_{IL}	-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc

AC PARAMETERS

Propagation Delay	t_{pd}	0.7	3.1	0.7	3.0	0.7	3.2	ns
Rise Time	t_r	0.7	2.2	0.7	2.0	0.7	2.2	ns
Fall Time	t_f	0.7	2.2	0.7	2.0	0.7	2.2	ns

NOTE:
Each MECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater then 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

TRUTH TABLE

INPUTS					OUTPUTS							
$\overline{E0}$	$\overline{E1}$	C	B	A	Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7
L	L	L	L	L	H	L	L	L	L	L	L	L
L	L	L	L	H	L	H	L	L	L	L	L	L
L	L	L	H	L	L	L	H	L	L	L	L	L
L	L	L	H	H	L	L	L	H	L	L	L	L
L	L	H	L	L	L	L	L	L	H	L	L	L
L	L	H	L	H	L	L	L	L	L	H	L	L
L	L	H	H	L	L	L	L	L	L	L	H	L
L	L	H	H	H	L	L	L	L	L	L	L	H
H	Φ	Φ	Φ	Φ	L	L	L	L	L	L	L	L
Φ	H	Φ	Φ	Φ	L	L	L	L	L	L	L	L

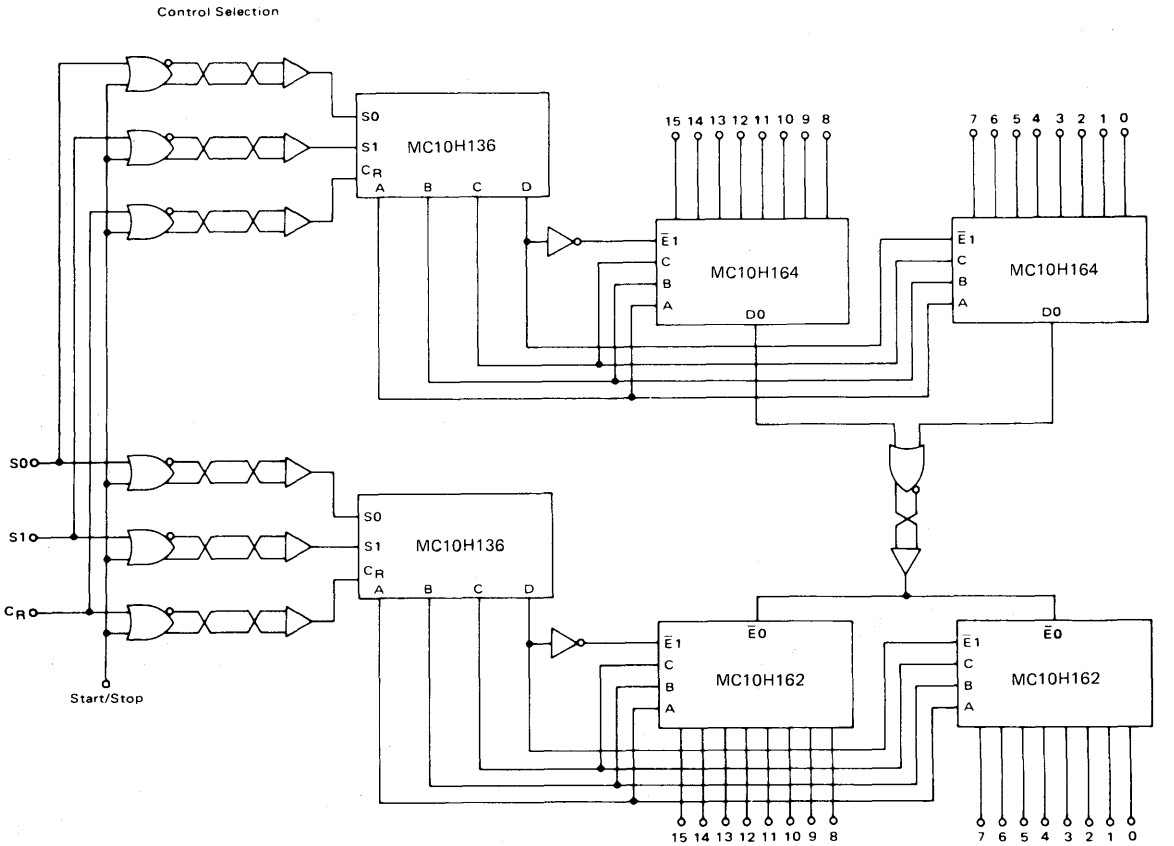
Φ = Don't Care

The MC10H162 is designed to decode a three bit input word to one of eight output lines. The MC10H162 output will be high when selected while all other output are low. The enable inputs, when either or both are high, force all outputs low.

The MC10H162 is a true parallel decoder. This eliminates unequal parallel path delay times found in other decoder designs. These devices are ideally suited for multiplexer/demultiplexer applications.

TYPICAL APPLICATIONS

FIGURE 1 – HIGH SPEED 16-BIT MULTIPLEXER/DEMULTIPLEXER



MOTOROLA

MC10H164

Advance Information

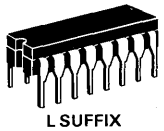
2

MECL 10KH HIGH-SPEED EMITTER-COUPLED LOGIC

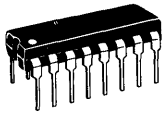
The MC10H164 is a member of Motorola's new MECL family. This MECL 10KH part is a functional/pinout duplication of the standard MECL 10K family part, with 100% improvement in propagation delay, and no increase in power supply current.

- Propagation Delay, 1 ns Typical
- Power Dissipation 310 mW Typical (same as MECL 10K)
- Improved Noise Margin 150 mV (over operating voltage and temperature range)
- Voltage Compensated
- MECL 10K-Compatible.

MECL 10KH

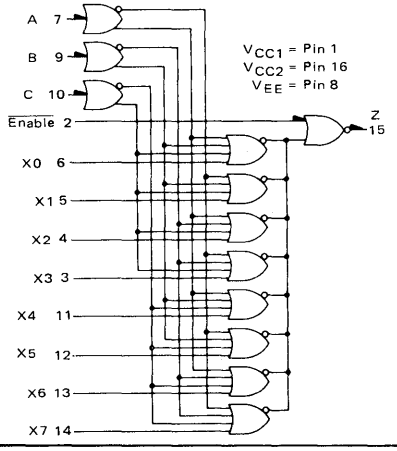


L SUFFIX
CERAMIC PACKAGE
CASE 620



P SUFFIX
PLASTIC PACKAGE
CASE 648

8-Line Multiplexer



TRUTH TABLE

ENABLE	ADDRESS INPUTS C	B	A	Z
L	L	L	L	X0
L	L	L	H	X1
L	L	H	L	X2
L	L	H	H	X3
L	H	L	L	X4
L	H	L	H	X5
L	H	H	L	X6
L	H	H	H	X7
H	ϕ	ϕ	ϕ	L

ϕ = Don't Care

MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply (V_{CC} = 0)	V_{EE}	-8.0 to 0	Vdc
Input Voltage (V_{CC} = 0)	V_I	0 to V_{EE}	Vdc
Output Current — Continuous — Surge	I_{out}	50 100	mA
Operating Temperature Range	T_A	0–75	°C
Storage Temperature Range — Plastic — Ceramic	T_{stg}	-55 to 150 -55 to 165	°C °C

ELECTRICAL CHARACTERISTICS (V_{EE} = -5.2 V ±5%) (See Note)

Characteristic	Symbol	0° Min	0° Max	25° Min	25° Max	75° Min	75° Max	Unit
Power Supply Current	I_E	—	83	—	75	—	83	mA
Input Current High	I_{inH}	—	512	—	320	—	320	μA
Input Current Low	I_{inL}	0.7	—	0.7	—	0.7	—	μA
High Output Voltage	V_{OH}	-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
Low Output Voltage	V_{OL}	-1.95	-1.63	-1.95	-1.63	-0.735	-1.60	Vdc
High Input Voltage	V_{IH}	-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
Low Input Voltage	V_{IL}	-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc

AC PARAMETERS

Propagation Delay	t_{pd}							ns
X_0-X_7		1.0	2.8	0.7	2.7	0.7	2.9	
A, B, C		1.0	3.8	0.7	3.6	0.7	3.9	
$\overline{\text{Enable}}$		1.0	1.9	0.7	1.7	0.7	1.9	
Rise Time	t_r	0.7	2.1	0.7	2.0	0.7	2.2	ns
Fall Time	t_f	0.7	2.1	0.7	2.0	0.7	2.2	ns

NOTE:
Each MECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater then 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts.

The MC10H164 is designed to be used in data multiplexing and parallel to serial conversion applications. Full parallel gating provides equal delays through any data path. The MC10H164 incorporates an output buffer, eight inputs and an enable. A high on the enable forces the output low. The open emitter output allows the MC10H164 to be connected directly to a data bus. The enable line allows an easy means of expanding to more than 8 lines using additional MC10H164's.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

TYPICAL APPLICATIONS

FIGURE 1 — HIGH SPEED 16-BIT MULTIPLEXER/DEMULTIPLEXER

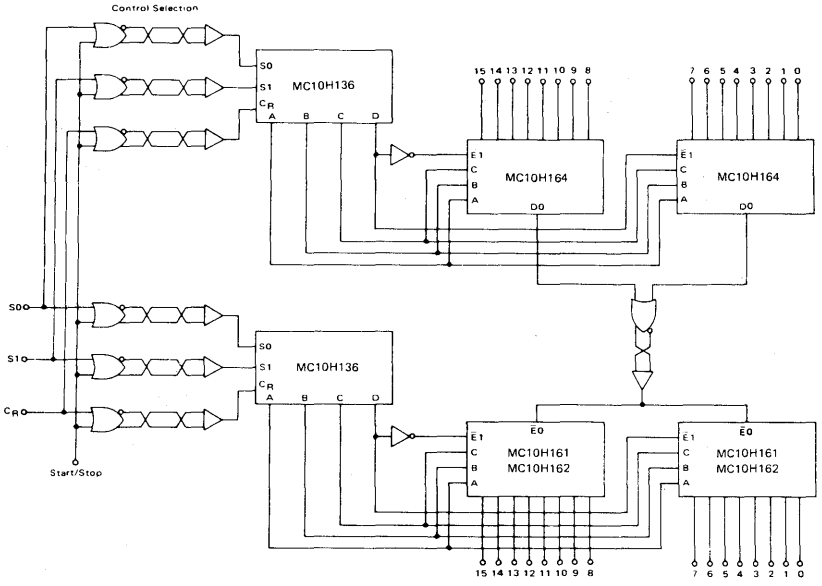
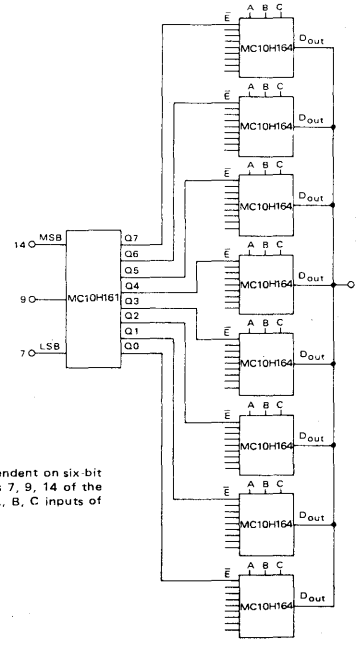


FIGURE 2 — 1-OF-64 LINE MULTIPLEXER



The Bit chosen is dependent on six-bit code present on inputs 7, 9, 14 of the MC10H161 and the A, B, C inputs of the MC10H164.

MOTOROLA

MC10H165

Advance Information

2

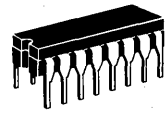
8-INPUT PRIORITY ENCODER

The MC10H165 is a member of Motorola's new MECL family. The MC10H165 is an 8-Input Priority Encoder. This 10KH part is a functional/pinout duplication of the standard MECL 10K family part, with 100% improvement in propagation delay, and no increases in power supply current.

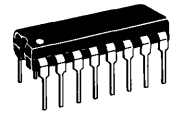
- Propagation Delay, Data-to-Output, 2.2 ns Typical
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible

MECL 10KH

8-INPUT PRIORITY ENCODER



L SUFFIX
CERAMIC PACKAGE
CASE 620



P SUFFIX
PLASTIC PACKAGE
CASE 648

MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply (V_{CC} = 0)	V_{EE}	−8.0 to 0	Vdc
Input Voltage (V_{CC} = 0)	V_I	0 to V_{EE}	Vdc
Output Current — Continuous — Surge	I_{out}	50 100	mA
Operating Temperature Range	T_A	0 to +75	°C
Storage Temperature Range — Plastic — Ceramic	T_{stg}	−55 to +150 −55 to +165	°C

ELECTRICAL CHARACTERISTICS (V_{EE} = −5.2 V ±5.0%) (See Note)

		0°		25°		75°C		
Characteristic	Symbol	Min	Max	Min	Max	Min	Max	Unit
Power Supply Current	I_E	—	144	—	131	—	144	mA
Input Current High Pin 4 Data Inputs	I_{inH}	 — —	 510 600	 — —	 320 370	 — —	 320 370	μAdc
Input Current Low	I_{inL}	0.5	—	0.5	—	0.3	—	μA
High Output Voltage	V_{OH}	−1.02	−0.84	−0.98	−0.81	−0.92	−0.735	Vdc
Low Output Voltage	V_{OL}	−1.95	−1.63	−1.95	−1.63	−1.95	−1.60	Vdc
High Input Voltage	V_{IH}	−1.17	−0.84	−1.13	−0.81	−1.07	−0.735	Vdc
Low Input Voltage	V_{IL}	−1.95	−1.48	−1.95	−1.48	−1.95	−1.45	Vdc

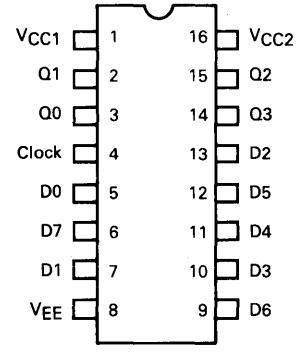
AC PARAMETERS

Propagation Delay Data input → Output Clock Input → Output	t_{pd}	 0.7 0.7	 3.4 2.2	 0.7 0.7	 3.2 2.0	 0.7 0.7	 3.4 2.2	ns
Setup Time	t_{set}	3.0	—	3.0	—	3.0	—	ns
Hold Time	t_{hold}	0.5	—	0.5	—	0.5	—	ns
Rise Time	t_r	0.7	2.4	0.7	2.2	0.7	2.4	ns
Fall Time	t_f	0.7	2.4	0.7	2.2	0.7	2.4	ns

NOTE:
Each MECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

PIN ASSIGNMENT



TRUTH TABLE

DATA INPUTS								OUTPUTS			
D0	D1	D2	D3	D4	D5	D6	D7	Q3	Q2	Q1	Q0
H	ϕ	ϕ	ϕ	ϕ	ϕ	ϕ	ϕ	H	L	L	L
L	H	ϕ	ϕ	ϕ	ϕ	ϕ	ϕ	H	L	L	H
L	L	H	ϕ	ϕ	ϕ	ϕ	ϕ	H	L	H	L
L	L	L	H	ϕ	ϕ	ϕ	ϕ	H	L	H	H
L	L	L	L	H	ϕ	ϕ	ϕ	H	H	L	L
L	L	L	L	L	H	ϕ	ϕ	H	H	L	H
L	L	L	L	L	L	H	ϕ	H	H	H	L
L	L	L	L	L	L	L	H	H	H	H	H
L	L	L	L	L	L	L	L	L	L	L	L

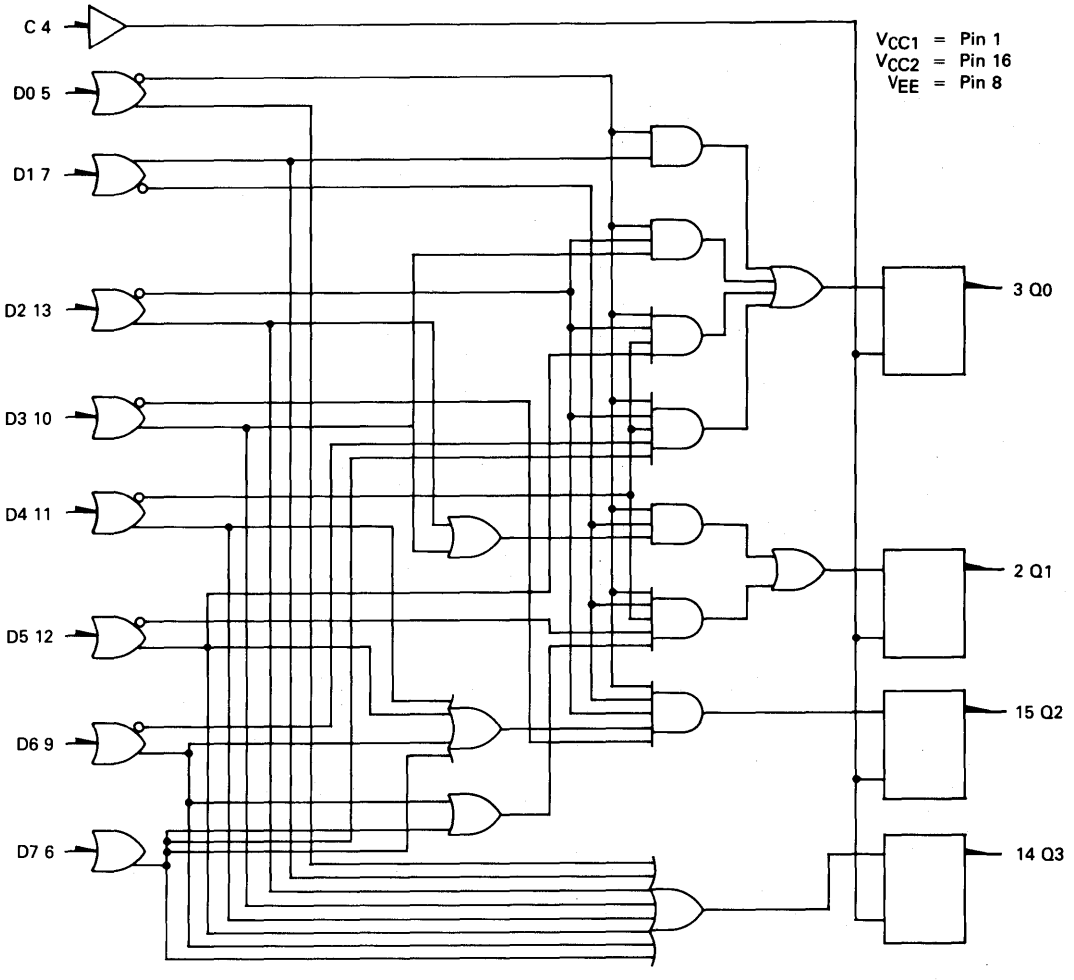
ϕ = Don't Care

8-INPUT PRIORITY ENCODER

The MC10H165 is a device designed to encode eight inputs to a binary coded output. The output code is that of the highest order input. Any input of lower priority is ignored. Each output incorporates a latch allowing synchronous operation. When the clock is low the outputs follow the inputs and latch when the clock goes high. This device is very useful for a variety of applications in checking system status in control processors, peripheral controllers, and testing systems.

The input is active when high, (e.g., the three binary outputs are low when input D0 is high). The Q3 output is high when any input is high. This allows direct extension into another priority encoder when more than eight inputs are necessary. The MC10H165 can also be used to develop binary codes from random logic inputs, for addressing ROMs, RAMs, or for multiplexing data.

LOGIC DIAGRAM

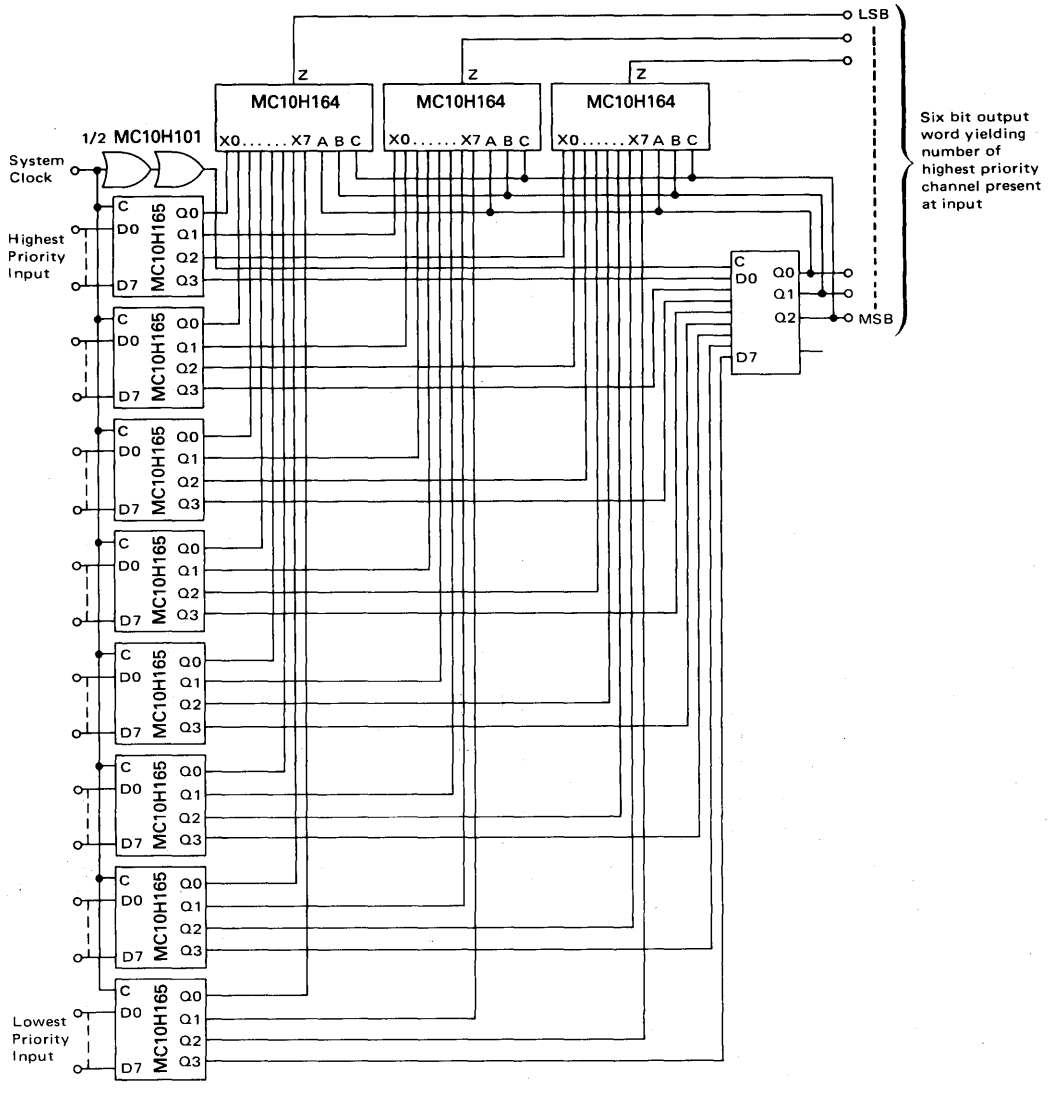


Numbers at ends of terminals denote pin numbers for L and P packages.

APPLICATION INFORMATION

A typical application of the MC10H165 is the decoding of system status on a priority basis. A 64-line priority encoder is shown in the figure below. System status lines are connected to this encoder such that, when a given condition exists, the respective input will be at a logic high level. This scheme will select the one of 64 different system conditions, as represented at the encoder inputs, which has priority in determining the next system operation to be performed. The binary code showing the address of the highest priority input present will appear at the encoder outputs to control other system logic functions.

64-LINE PRIORITY ENCODER



MOTOROLA

MC10H166

Advance Information

5-BIT MAGNITUDE COMPARATOR

The MC10H166 is a member of Motorola's new MECL family. The MC10H166 is a 5-Bit Magnitude Comparator and is a functional/pinout duplication of the standard MECL 10K part with 100% improvement in propagation delay and no increase in power-supply current.

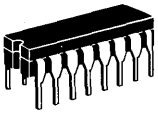
The MC10H166 is a high-speed expandable 5-bit comparator for comparing the magnitude of two binary words. Two outputs are provided: A<B and A>B. The A=B function can be obtained by wire-ORing these outputs (a low level indicates A=B) or by wire-NORing the outputs (a high level indicates A≠B). A high level on the enable function forces both outputs low.

- Propagation Delay, Data-to-Output, 2.0 ns Typical
- Power Dissipation 440 mW Typical
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible

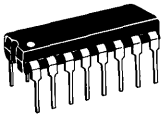
MECL 10KH

5-BIT MAGNITUDE COMPARATOR

2

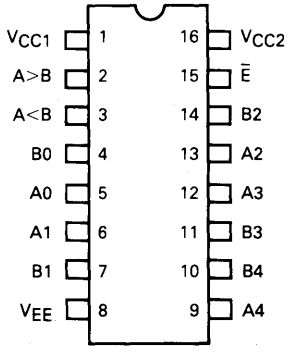


L SUFFIX
CERAMIC PACKAGE
CASE 620



P SUFFIX
PLASTIC PACKAGE
CASE 648

PIN ASSIGNMENT



MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply (V_{CC} = 0)	V_{EE}	-8.0 to 0	Vdc
Input Voltage (V_{CC} = 0)	V_I	0 to V_{EE}	Vdc
Output Current — Continuous — Surge	I_{out}	50 100	mA
Operating Temperature Range	T_A	0 to +75	°C
Storage Temperature Range — Plastic — Ceramic	T_{stg}	-55 to +150 -55 to +165	°C °C

ELECTRICAL CHARACTERISTICS (V_{EE} = -5.2 V ±5.0%) (See Note)

		0°		25°		75°C		
Characteristic	Symbol	Min	Max	Min	Max	Min	Max	Unit
Power Supply Current	I_E	—	117	—	106	—	117	mA
Input Current High	I_{inH}	—	350	—	220	—	220	μA
Input Current Low	I_{inL}	0.5	—	0.5	—	0.3	—	μA
High Output Voltage	V_{OH}	-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
Low Output Voltage	V_{OL}	-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
High Input Voltage	V_{IH}	-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
Low Input Voltage	V_{IL}	-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc

AC PARAMETERS

Propagation Delay	t_{pd}							ns
Data-to-Output		0.7	4.1	0.7	3.8	0.7	4.1	
Enable-to-Output		0.7	2.0	0.7	1.8	0.7	2.0	
Rise Time	t_r	0.7	2.2	0.7	2.0	0.7	2.2	ns
Fall Time	t_f	0.7	2.2	0.7	2.0	0.7	2.2	ns

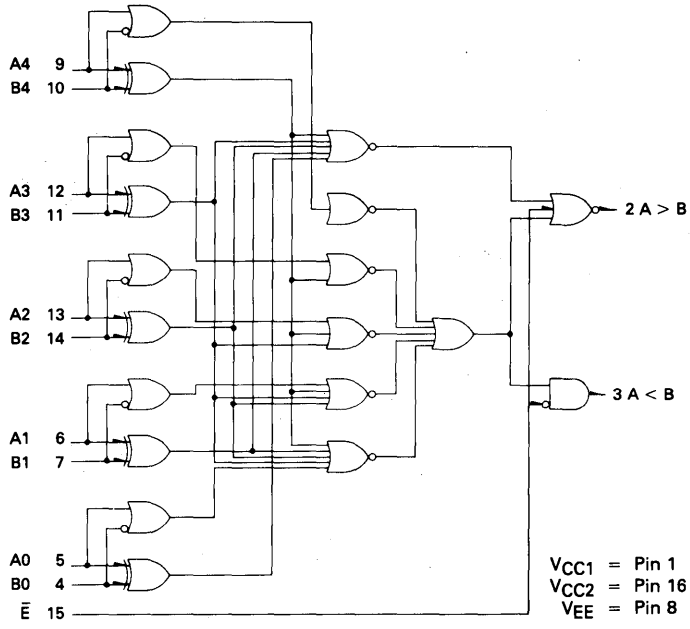
TRUTH TABLE

Inputs			Outputs	
$\bar{E}$	A	B	A < B	A > B
H	X	X	L	L
L	Word A = Word B		L	L
L	Word A > Word B		L	H
L	Word A < Word B		H	L

This document contains information on a new product Specifications and information herein is subject to change without notice.

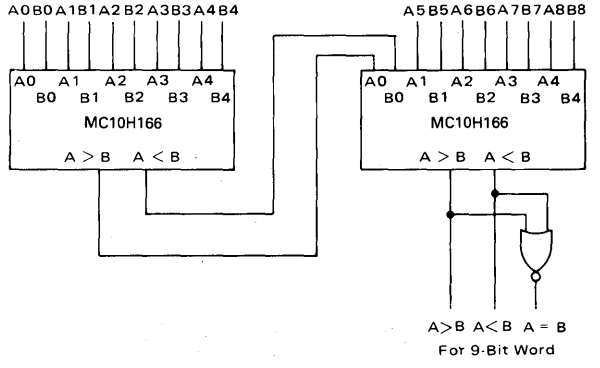
2

LOGIC DIAGRAM



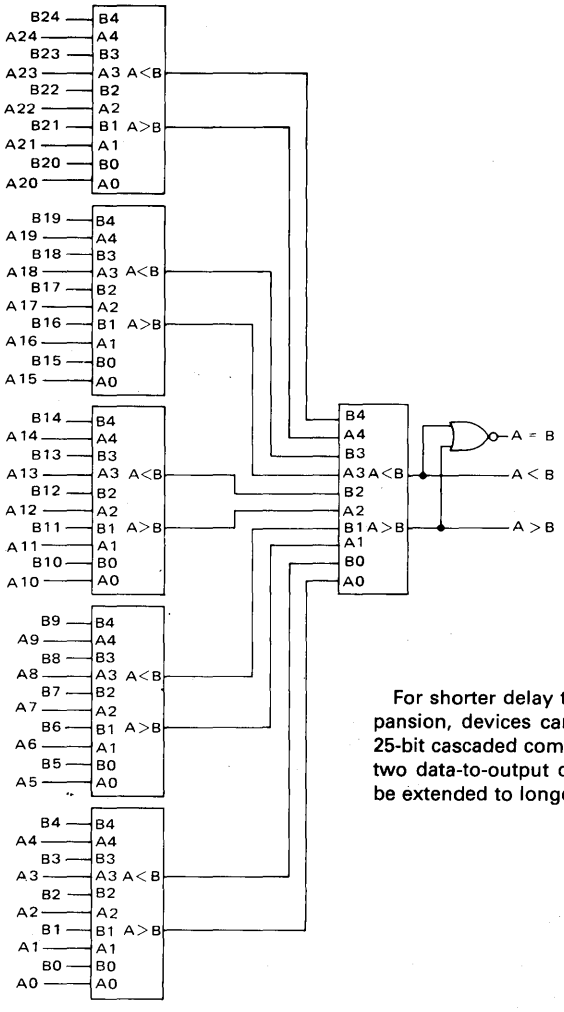
NOTE:
Each MECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts.

FIGURE 1 — 9-BIT MAGNITUDE COMPARATOR



For longer word lengths, the MC10H166 can be serially expanded or cascaded. Figure 1 shows two devices in a serial expansion for a 9-bit word length. The A >B and A <B outputs are fed to the A0 and B0 inputs respectively of the next device. The connection for an A = B output is also shown. The worst case delay time of serial expansion is equal to the number of comparators times the data-to-output delay.

FIGURE 2 — 25-BIT MAGNITUDE COMPARATOR



For shorter delay times than possible with serial expansion, devices can be cascaded. Figure 2 shows a 25-bit cascaded comparator whose worst case delay is two data-to-output delays. The cascaded scheme can be extended to longer word lengths.

MOTOROLA

MC10H173

Advance Information

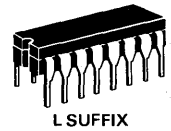
2

MECL 10KH HIGH-SPEED EMITTER-COUPLED LOGIC

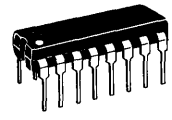
The MC10H173 is a quad 2-input multiplexer with latch. This device is a functional/pinout duplication of the standard MECL 10K part, with 100% improvement in propagation delay and no increase in power supply current.

- Data Propagation Delay, 1.5 ns Typical
- Power Dissipation, 275 mW Typical
- Improved Noise Margin 150 mV (over operating voltage and temperature range)
- Voltage Compensated
- MECL 10K-Compatible

MECL 10KH



P SUFFIX
PLASTIC PACKAGE
CASE 648



L SUFFIX
CERAMIC PACKAGE
CASE 620

MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply (V_{CC} = 0)	V_{EE}	-8.0 to 0	Vdc
Input Voltage (V_{CC} = 0)	V_I	0 to V_{EE}	Vdc
Output Current — Continuous — Surge	I_{out}	50 100	mA
Operating Temperature Range	T_A	0–75	°C
Storage Temperature Range — Plastic — Ceramic	T_{stg}	-55 to 150 -55 to 165	°C °C

ELECTRICAL CHARACTERISTICS (V_{EE} = -5.2 V ± 5%) (See note)

Characteristic	Symbol	0° Min	0° Max	25° Min	25° Max	75°C Min	75°C Max	Unit
Power Supply Current	I_E		73		66		73	mAdc
Input Current High Pins 3-7 & 10-13 Pin 9	I_{inH}		 510 475		 320 300		 320 300	μA
Input Current Low	I_{inL}	0.5	—	0.5	—	0.3	—	μA
High Output Voltage	V_{OH}	-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
Low Output Voltage	V_{OL}	-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
High Input Voltage	V_{IH}	-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
Low Input Voltage	V_{IL}	-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc

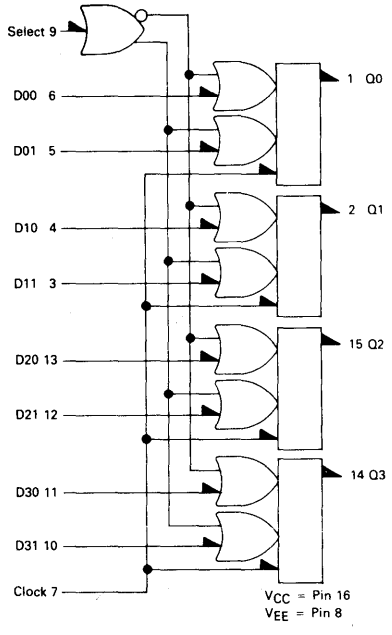
AC PARAMETERS

Propagation Delay Data Clock Select	t_{pd}	 0.7 1.0 1.0	 2.3 3.7 3.6	 0.7 1.0 1.0	 2.1 3.5 3.4	 0.7 1.0 1.0	 2.3 3.7 3.6	ns
Set Up Time Data Select	t_{set}	 0.7 1.0	 — —	 0.7 1.0	 — —	 0.7 1.0	 — —	ns
Hold Time Data Select	t_{hold}	 0.7 1.0	 — —	 0.7 1.0	 — —	 0.7 1.0	 — —	ns
Rise Time	t_r	0.7	2.4	0.7	2.1	0.7	2.4	ns
Fall Time	t_f	0.7	2.4	0.7	2.1	0.7	2.4	ns

NOTE:
Each MECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

Quad 2-input Multiplexer/Latch



TRUTH TABLE

SELECT	CLOCK	$Q0_{n+1}$
H	L	D00
L	L	D01
ϕ	H	$Q0_n$

ϕ = Don't Care

APPLICATION INFORMATION

The MC10173 is a quad two-channel multiplexer with latch. It incorporates common clock and common data select inputs. The select input determines which data input is enabled. A high (H) level enables data inputs D00, D10, D20, and D30 and a low (L) level enables data inputs D01, D11, D21, D31. Any change on the data input will be reflected at the outputs while the clock is low. The outputs are latched on the positive transition of the clock. While the clock is in the high state, a change in the information present at the data inputs will not affect the output information.

MOTOROLA

MC10H174

Advance Information

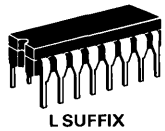
2

MECL 10KH HIGH-SPEED EMITTER-COUPLED LOGIC

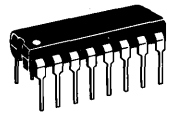
The MC10H174 is a Dual 4-to-1 Multiplexer. This device is a functional/pinout duplication of the standard MECL 10K part, with 100% improvement in propagation delay and no increase in power supply current.

- Propagation Delay, 1.5 ns Typical
- Power Dissipation, 305 mW Typical
- Improved Noise Margin 150 mV (over operating voltage and temperature range)
- Voltage Compensated
- MECL 10K-Compatible

MECL 10KH

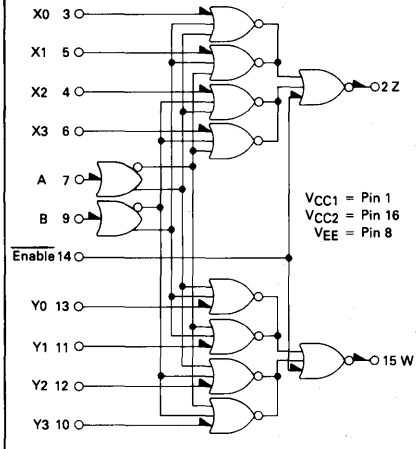


P SUFFIX
PLASTIC PACKAGE
CASE 648



L SUFFIX
CERAMIC PACKAGE
CASE 620

Dual 4-to-1 Multiplexer



MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply (V_{CC} = 0)	V_{EE}	−8.0 to 0	Vdc
Input Voltage (V_{CC} = 0)	V_I	0 to V_{EE}	Vdc
Output Current — Continuous — Surge	I_{out}	50 100	mA
Operating Temperature Range	T_A	0–75	°C
Storage Temperature Range — Plastic — Ceramic	T_{stg}	−55 to 150 −55 to 165	°C °C

ELECTRICAL CHARACTERISTICS (V_{EE} = −5.2 V ± 5%) (See note)

Characteristic	Symbol	0° Min	0° Max	25° Min	25° Max	75° Min	75° Max	Unit
Power Supply Current	I_E		80		73		80	mAdc
Input Current High Pins 3–7 & 9–13 Pin 14	I_{inH}		 475 670		 300 420		 300 420	µAdc
Input Current Low	I_{inL}	0.5	—	0.5	—	0.3	—	µA
High Output Voltage	V_{OH}	−1.02	−0.84	−0.98	−0.81	−0.92	−0.735	Vdc
Low Output Voltage	V_{OL}	−1.95	−1.63	−1.95	−1.63	−1.95	−1.60	Vdc
High Input Voltage	V_{IH}	−1.17	-0.84	−1.13	-0.81	−1.07	-0.735	Vdc
Low Input Voltage	V_{IL}	-1.95	−1.48	-1.95	−1.48	-1.95	-1.45	Vdc

AC PARAMETERS

Propagation Delay Data Select (A, B) Enable	t_{pd}	 1.0 1.0 1.0	 2.9 3.8 1.9	 0.7 0.7 0.7	 2.7 3.6 1.7	 0.7 0.7 0.7	 2.9 3.8 1.9	ns
Rise Time	t_r	0.7	2.2	0.7	2.0	0.7	2.2	ns
Fall Time	t_f	0.7	2.2	0.7	2.0	0.7	2.2	ns

NOTE:
Each MECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts.

TRUTH TABLE

ENABLE	ADDRESS INPUTS		OUTPUTS	
E	B	A	Z	W
H	ϕ	ϕ	L	L
L	L	L	X0	Y0
L	L	H	X1	Y1
L	H	L	X2	Y2
L	H	H	X3	Y3

ϕ = Don't Care

This document contains information on a new product. Specifications and information herein are subject to change without notice.

MOTOROLA

MC10H175

Advance Information

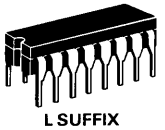
MECL 10KH

2

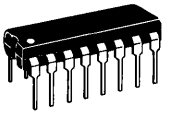
MECL 10KH HIGH-SPEED EMITTER-COUPLED LOGIC

The MC10H175 is a member of Motorola's new MECL family. The MC10H175 is a quint D type latch with common reset and clock lines. This MECL 10KH part is a functional/pinout duplication of the standard MECL 10K family part, with 100% improvement in propagation delay and no increase in power-supply current.

- Propagation Delay, 1.2 ns Typical
- Power Dissipation, 400 mW Typical
- Improved Noise Margin 150 mV (over operating voltage and temperature range)
- Voltage Compensated
- MECL 10K-Compatible



L SUFFIX
CERAMIC PACKAGE
CASE 620



P SUFFIX
PLASTIC PACKAGE
CASE 648

MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply (V_{CC} = 0)	V_{EE}	-8.0 to 0	Vdc
Input Voltage (V_{CC} = 0)	V_I	0 to V_{EE}	Vdc
Output Current — Continuous — Surge	I_{out}	50 100	mA
Operating Temperature Range	T_A	0-75	°C
Storage Temperature Range — Plastic — Ceramic	T_{stg}	-55 to 150 -55 to 165	°C °C

ELECTRICAL CHARACTERISTICS (V_{EE} = -5.2 V ±5%) (See Note)

Characteristic	Symbol	0°		25°		75°		Unit
		Min	Max	Min	Max	Min	Max	
Power Supply Current	I_E	—	107	—	97	—	107	mA
Input Current High Pins 5,6,7,9,10,12,13 Pin 11	I_{inH}	 — —	 565 1120	 — —	 335 660	 — —	 335 660	µA
Input Current Low	I_{inL}	0.5	—	0.5	—	0.3	—	µA
High Output Voltage	V_{OH}	-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
Low Output Voltage	V_{OL}	-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
High Input Voltage	V_{IH}	-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
Low Input Voltage	V_{IL}	-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc

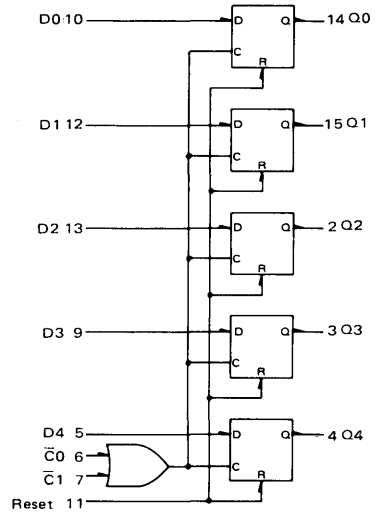
AC PARAMETERS

Propagation Delay Data Clock Reset	t_{pd}	 0.7 0.7 0.7	 1.8 2.3 2.1	 0.7 0.7 0.7	 1.7 2.2 2.0	 0.7 0.7 0.7	 1.8 2.2 2.1	ns
Set-up Time	t_{set}	1.5	—	1.5	—	1.5	—	ns
Hold Time	t_{hold}	1.0	—	1.0	—	1.0	—	ns
Rise Time	t_r	0.7	1.8	0.7	1.8	0.7	1.9	ns
Fall Time	t_f	0.7	1.8	0.7	1.8	0.7	1.9	ns

NOTE:
Each MECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater then 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

QUINT LATCH



V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

TRUTH TABLE

D	$\overline{C0}$	$\overline{C1}$	Reset	Q_{n+1}
L	L	L	ϕ	L
H	L	L	ϕ	H
ϕ	H	ϕ	L	Q_n
ϕ	ϕ	H	L	Q_n
ϕ	H	ϕ	H	L
ϕ	ϕ	H	H	L

ϕ = don't care

APPLICATION INFORMATION

The MC10H175 is a high speed, low power quint latch. It features five D type latches with common reset and a common two-input clock. Data is transferred on the negative edge of the clock and latched on the positive edge. The two clock inputs are "OR"ed together.

Any change on the data input will be reflected at the outputs while the clock is low. The outputs are latched on the positive transition of the clock. While the clock is in the high state, a change in the information present at the data inputs will not affect the output information. The reset input is enabled only when the clock is in the high state.

MOTOROLA

MC10H176

Advance Information

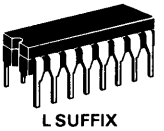
MECL 10KH

2

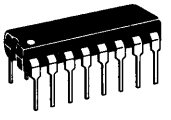
MECL 10KH HIGH-SPEED EMITTER-COUPLED LOGIC

The MC10H176 is a member of Motorola's new MECL family. The MC10H176 contains six master slave type "D" flip-flops with a common clock. This MECL 10KH part is a functional/pinout duplication of the standard MECL 10K family part, with 100% improvement in clock frequency and propagation delay and no increase in power-supply current.

- Propagation Delay 1.7 ns Typical
- Power Dissipation, 460 mW Typical
- Improved Noise Margin 150 mV (over operating voltage and temperature range)
- Voltage Compensated
- MECL 10K-Compatible

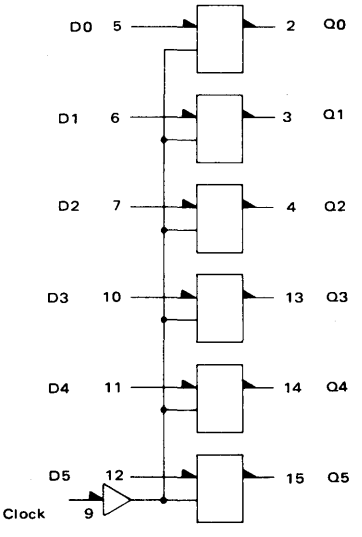


L SUFFIX
CERAMIC PACKAGE
CASE 620



P SUFFIX
PLASTIC PACKAGE
CASE 648

HEX D MASTER-SLAVE FLIP-FLOP



V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

CLOCKED TRUTH TABLE

C	D	Q_{n+1}
L	ϕ	Q_n
H*	L	L
H*	H	H

ϕ = Don't Care
*A clock H is a clock transition from a low to a high state.

MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply (V_{CC} = 0)	V_{EE}	-8.0 to 0	Vdc
Input Voltage (V_{CC} = 0)	V_I	0 to V_{EE}	Vdc
Output Current — Continuous — Surge	I_{out}	50 100	mA
Operating Temperature Range	T_A	0–75	°C
Storage Temperature Range — Plastic — Ceramic	T_{stg}	-55 to 150 -55 to 165	°C °C

ELECTRICAL CHARACTERISTICS (V_{EE} = -5.2 V ±5%) (See Note)

Characteristic	Symbol	0°		25°		75°		Unit
		Min	Max	Min	Max	Min	Max	
Power Supply Current	I_E	—	123	—	112	—	123	mA
Input Current High Pins 5,6,7,10,11,12 Pin 9	I_{inH}	 — —	 425 670	 — —	 265 420	 — —	 265 420	μA
Input Current Low	I_{inL}	0.5	—	0.5	—	0.3	—	μA
High Output Voltage	V_{OH}	-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
Low Output Voltage	V_{OL}	-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
High Input Voltage	V_{IH}	-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
Low Input Voltage	V_{IL}	-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc

AC PARAMETERS

Propagation Delay	t_{pd}	1.0	2.9	1.0	2.7	1.0	3.0	ns
Set-up Time	t_{set}	1.5	—	1.5	—	1.5	—	ns
Hold Time	t_{hold}	0.8	—	0.8	—	0.8	—	ns
Rise Time	t_r	0.8	2.5	0.7	2.4	0.8	2.6	ns
Fall Time	t_f	0.8	2.5	0.7	2.4	0.8	2.6	ns
Toggle Frequency	f_{tog}	250	—	250	—	250	—	MHz

NOTE:
Each MECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater then 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

APPLICATION INFORMATION

The MC10H176 contains six high-speed, master slave type "D" flip-flops. Data is entered into the master when the clock is low. Master-to-slave data transfer takes place on the positive-going Clock transition. Thus, outputs may change only on a positive-going Clock transition. A change in the information present at the data (D) input will not affect the output information any other time due to the master-slave construction of this device.

MOTOROLA

MC10H179

Advance Information

MECL 10KH HIGH-SPEED EMITTER-COUPLED LOGIC

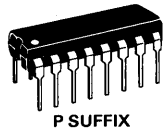
The MC10H179 is a member of Motorola's new MECL family. It is a functional/pinout duplication of the standard MECL 10K part, with 100% improvement in propagation delay and no increase in power supply current.

- Power Dissipation, 300 mW Typical
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible

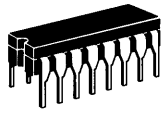
MECL 10KH

LOOK-AHEAD CARRY BLOCK

2



L SUFFIX
CERAMIC PACKAGE
CASE 620



P SUFFIX
PLASTIC PACKAGE
CASE 648

MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply (V_{CC} = 0)	V_{EE}	-8.0 to 0	Vdc
Input Voltage (V_{CC} = 0)	V_I	0 to V_{EE}	Vdc
Output Current — Continuous — Surge	I_{out}	50 100	mA
Operating Temperature Range	T_A	0–+75	°C
Storage Temperature Range — Plastic — Ceramic	T_{stg}	-55 to +150 -55 to +165	°C °C

ELECTRICAL CHARACTERISTICS (V_{EE} = -5.2 V ± 5%) (See Note)

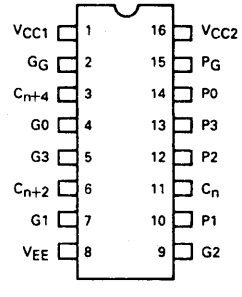
Characteristic	Symbol	0°		25°		75°		Unit
		Min	Max	Min	Max	Min	Max	
Power Supply Current	I_E	—	79	—	72	—	79	mA
Input Current High	I_{inH}							μA
Pins 5 and 9		—	465	—	275	—	275	
Pins 4, 7 and 11		—	545	—	320	—	320	
Pin 14		—	705	—	415	—	415	
Pin 12		—	790	—	465	—	465	
Pins 10 and 13		—	870	—	510	—	510	
Input Current Low	I_{inL}	0.5	—	0.5	—	0.3	—	μA
High Output Voltage	V_{OH}	-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
Low Output Voltage	V_{OL}	-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
High Input Voltage	V_{IH}	-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
Low Input Voltage	V_{IL}	-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc

AC PARAMETERS

Propagation Delay	t_{pd}							ns
Pins 5, 7, 9, 10, 11, 13 to 3 or 6		0.7	2.8	0.7	2.5	0.7	2.8	
G to G_G		0.7	2.8	0.7	2.5	0.7	2.8	
P to P_G		0.7	2.0	0.7	1.8	0.7	2.0	
P to G_G		0.7	2.8	0.7	2.5	0.7	2.8	
Rise Time	t_r	0.7	2.4	0.7	2.2	0.7	2.4	ns
Fall Time	t_f	0.7	2.4	0.7	2.2	0.7	2.4	ns

NOTE:
Each MECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts.

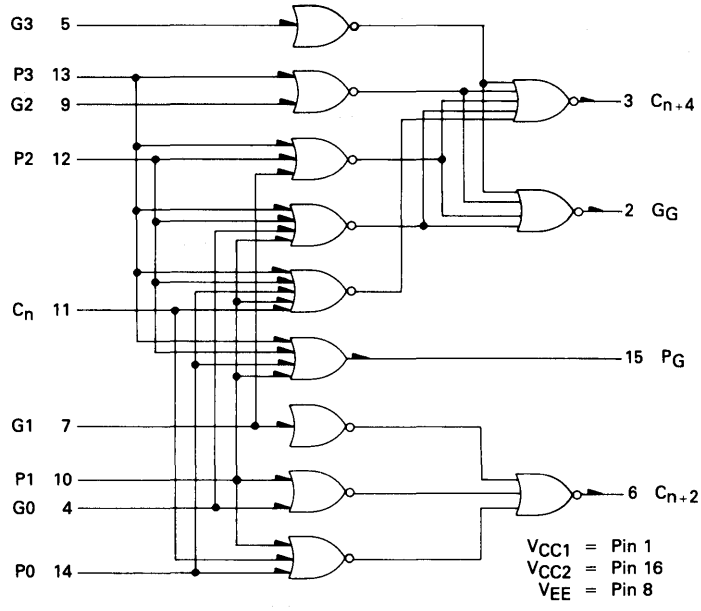
PIN ASSIGNMENT



This document contains information on a new product. Specifications and information herein are subject to change without notice.

2

LOGIC DIAGRAM



$P_G = P0 + P1 + P2 + P3$

$G_G = (G0 + P1 + P2 + P3)(G1 + P2 + P3)(G2 + P3)\,G3$

$C_{n+2} = (C_n + P0 + P1)(G0 + P1)\,G1$

$C_{n+4} = (C_n + P0 + P1 + P2 + P3)(G0 + P1 + P2 + P3)(G1 + P2 + P3)(G2 + P3)\,G3$

TYPICAL APPLICATIONS

The MC10H179 is a high-speed, low-power, standard MECL complex function that is designed to perform the look-ahead carry function. This device can be used with the MC10H181 4-bit ALU directly, or with the MC10H180 dual arithmetic unit in any computer, instrumentation or digital communication application requiring high speed arithmetic operation on long words.

When used with the MC10H181, the MC10H179 performs a second order or higher look-ahead. Figure 2 shows a 16-bit look-ahead carry arithmetic unit. Second order carry is valuable for longer binary words. As an example, addition of two 32-bit words is improved from 30 nanoseconds with ripple-carry techniques. A block diagram of a 32-bit ALU is shown in Figure 1. The MC10H179 may also be used in many other applications. It can, for example, reduce system package count when used to generate functions of several variables.

FIGURE 1 — 32-BIT ALU WITH CARRY LOOK-AHEAD

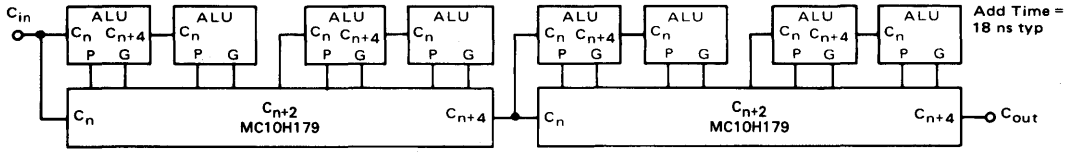
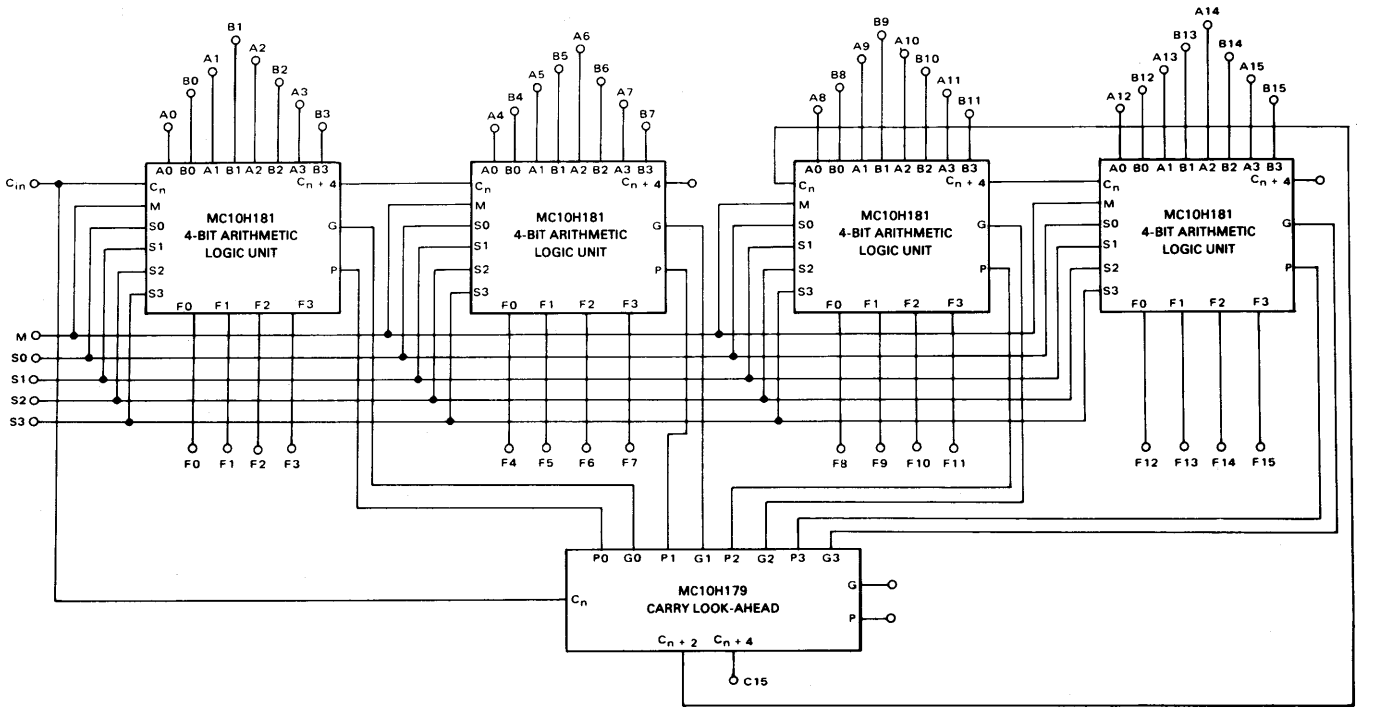


FIGURE 2 — 16-BIT FULL LOOK-AHEAD CARRY ARITHMETIC LOGIC UNIT



MOTOROLA

MC10H180

Advance Information

2

MECL 10KH HIGH-SPEED EMITTER-COUPLED LOGIC

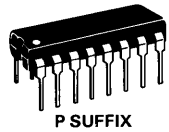
The MC10H180 is a member of Motorola's new MECL family. It is a high-speed, low-power, general-purpose adder/subtractor. It is designed to be used in special purpose adders/subtractors or in high-speed multiplier arrays.

Inputs for each adder are Carry-in, Operand A, and Operand B; outputs are Sum, $\overline{\text{Sum}}$ and Carry-out. The common select inputs serve as a control line to Invert A for subtract, and a control line to Invert B.

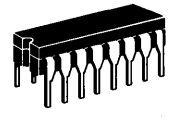
- Propagation Delay, 1.8 ns Typical, Operand and Select to Output
- Power Dissipation, 360 mW Typical
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible

MECL 10KH

DUAL 2-BIT ADDER/SUBTRACTOR



P SUFFIX
PLASTIC PACKAGE
CASE 648



L SUFFIX
CERAMIC PACKAGE
CASE 620

MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply (V_{CC} = 0)	V_{EE}	-8.0 to 0	Vdc
Input Voltage (V_{CC} = 0)	V_I	0 to V_{EE}	Vdc
Output Current — Continuous — Surge	I_{out}	50 100	mA
Operating Temperature Range	T_A	0–+75	°C
Storage Temperature Range — Plastic — Ceramic	T_{stg}	-55 to +150 -55 to +165	°C °C

ELECTRICAL CHARACTERISTICS (V_{EE} = -5.2 V ± 5%) (See Note)

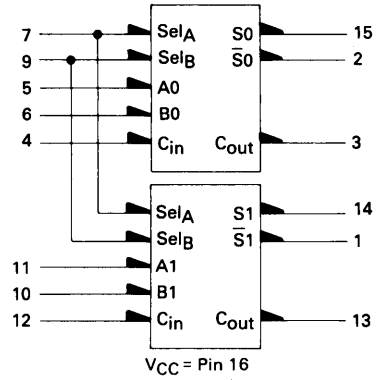
Characteristic	Symbol	0°		25°		75°		Unit
		Min	Max	Min	Max	Min	Max	
Power Supply Current	I_E	—	95	—	86	—	95	mA
Input Current High Pins 4, 12 Pins 7, 9 Pin 5, 6, 10, 11	I_{inH}	 — — —	 665 515 410	 — — —	 417 320 255	 — — —	 417 320 255	µA
Input Current Low	I_{inL}	0.5	—	0.5	—	0.3	—	µA
High Output Voltage	V_{OH}	-1.020	-0.840	-0.980	-0.810	-0.920	-0.735	Vdc
Low Output Voltage	V_{OL}	-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
High Input Voltage	V_{IH}	-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
Low Input Voltage	V_{IL}	-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc

AC PARAMETERS

Propagation Delay Operand to Output Select to Output Carry-in to Output	t_{pd}	 0.7 0.7 0.7	 3.8 3.8 2.1	 0.7 0.7 0.7	 3.5 3.5 1.8	 0.7 0.7 0.7	 3.8 3.8 2.1	ns
Rise Time	t_r	0.7	2.2	0.7	2.0	0.7	2.2	ns
Fall Time	t_f	0.7	2.2	0.7	2.0	0.7	2.2	ns

NOTE:
Each MECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts.

LOGIC DIAGRAM



V_{CC} = Pin 16
V_{EE} = Pin 8

Positive Logic Only

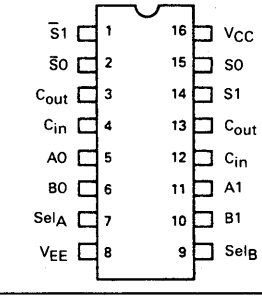
$A' = \overline{A \oplus Sel_A} = A \odot Sel_A$

$B' = \overline{B \oplus Sel_B} = B \odot Sel_B$

$S = \overline{C}_{in}(\overline{A'}\,B' + A'\,\overline{B'}) +$
$C_{in}(A'\,B' + \overline{A'}\,\overline{B'})$

$C_{out} = C_{in}A' + C_{in}\,B' + A'\,B'$

PIN ASSIGNMENT



This document contains information on a new product. Specifications and information herein are subject to change without notice.

FUNCTION SELECT TABLE

Sel_A	Sel_B	Function
H	H	S = A plus B
H	L	S = A minus B
L	H	S = B minus A
L	L	S = 0 minus A minus B

TRUTH TABLE

FUNCTION	INPUTS							
	Sel_A	Sel_B	A0	B0	C_{in}	S0	$\overline{S0}$	C_{out}
ADD	H	H	L	L	L	L	H	L
	H	H	L	L	H	H	L	L
	H	H	L	H	L	H	L	L
	H	H	L	H	H	L	H	H
	H	H	H	L	L	H	L	L
	H	H	H	L	H	L	H	H
	H	H	H	H	L	L	H	H
	H	H	H	H	H	H	L	H
SUBTRACT	H	L	L	L	L	H	L	L
	H	L	L	L	H	L	H	H
	H	L	L	H	L	L	H	L
	H	L	L	H	H	H	L	L
	H	L	H	L	L	L	H	H
	H	L	H	L	H	H	L	H
	H	L	H	H	L	H	L	L
	H	L	H	H	H	L	H	H

FUNCTION	INPUTS							
	Sel_A	Sel_B	A0	B0	C_{in}	S0	$\overline{S0}$	C_{out}
REVERSE SUBTRACT	L	H	L	L	L	H	L	L
	L	H	L	L	H	L	H	H
	L	H	L	H	L	L	H	H
	L	H	L	H	H	H	L	H
	L	H	H	L	L	L	H	L
	L	H	H	L	H	H	L	L
	L	H	H	H	L	H	L	L
	L	H	H	H	H	L	H	H
	L	L	L	L	L	L	H	H
	L	L	L	L	H	H	L	H
	L	L	L	H	L	H	L	L
	L	L	L	H	H	L	H	H
	L	L	H	L	L	L	H	L
	L	L	H	L	H	L	H	H
	L	L	H	H	L	L	H	L
	L	L	H	H	H	H	L	L

MOTOROLA

MC10H181

Advance Information

2

MECL 10KH HIGH-SPEED EMITTER-COUPLED LOGIC

The MC10H181 is a high-speed arithmetic logic unit capable of performing 16 logic operations and 16 arithmetic operations on two four-bit words. Full internal carry is incorporated for ripple through operation.

Arithmetic logic operations are selected by applying the appropriate binary word to the select inputs (S0 through S3) as indicated in the tables of arithmetic/logic functions. Group carry propagate (P_G) and carry generate (G_G) are provided to allow fast operations on very long words using a second order look-ahead. The internal carry is enabled by applying a low level voltage to the mode control input (M).

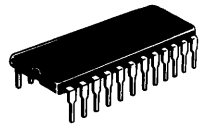
When used with the MC10H179, full-carry look-ahead, as a second order look-ahead block, the MC10H181 provides high-speed arithmetic operations on very long words.

This 10KH part is a functional/pinout duplication of the standard MECL 10K family part with 100% improvement in propagation delay and no increase in power supply current.

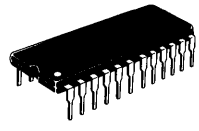
- Improved Noise Margin, 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible

MECL 10KH

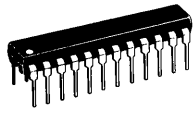
4-BIT ARITHMETIC LOGIC UNIT/ FUNCTION GENERATOR



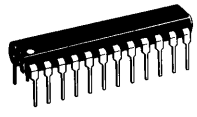
L SUFFIX
CERAMIC PACKAGE
CASE 623



P SUFFIX
PLASTIC PACKAGE
CASE 649



P SUFFIX
PLASTIC PACKAGE
CASE 724



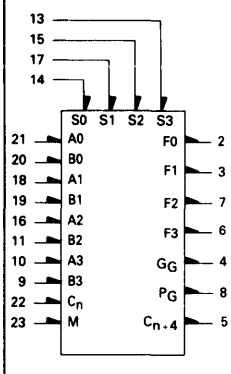
L SUFFIX
CERAMIC PACKAGE
CASE 758

MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply (V_{CC} = 0)	V_{EE}	−8.0 to 0	Vdc
Input Voltage (V_{CC} = 0)	V_I	0 to V_{EE}	Vdc
Output Current — Continuous — Surge	I_{out}	50 100	mA
Operating Temperature Range	T_A	0 to +75	°C
Storage Temperature Range — Plastic — Ceramic	T_{stg}	−55 to +150 −55 to +165	°C °C

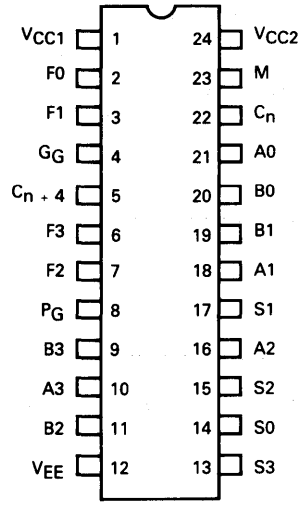
LOGIC DIAGRAM

V_{CC1} = Pin 1
V_{CC2} = Pin 24
V_{EE} = Pin 12

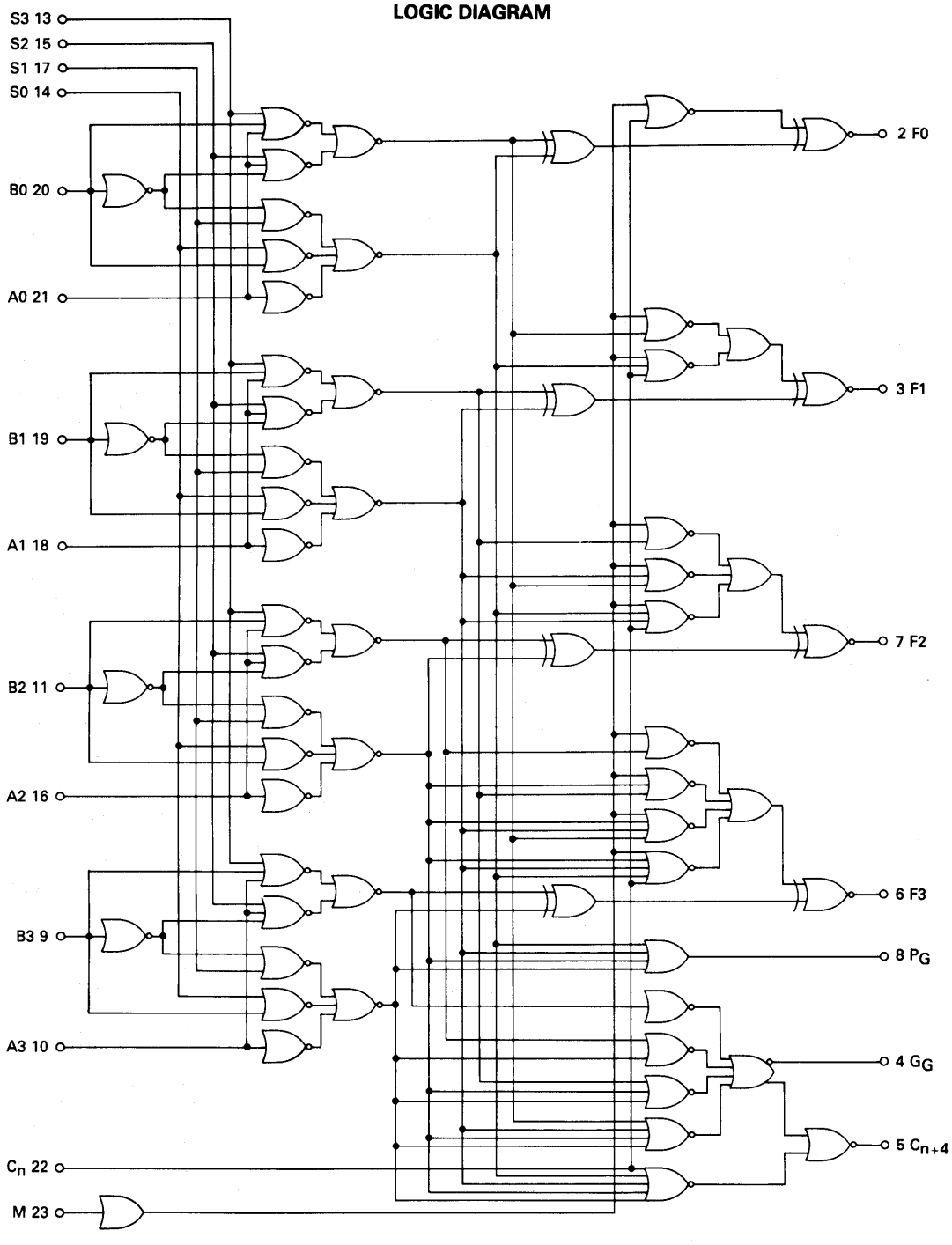


Function Select S3	S2	S1	S0	Logic Functions M is High C = D.C. F	Arithmetic Operation M is Low C_n is low F
L	L	L	L	$F = \overline{A}$	F = A
L	L	L	H	$F = \overline{A} + \overline{B}$	F = A plus $(A + \overline{B})$
L	L	H	L	$F = \overline{A} + B$	F = A plus (A + B)
L	L	H	H	F = Logical "1"	F = A times 2
L	H	L	L	$F = \overline{A} \cdot \overline{B}$	F = (A + B) plus 0
L	H	L	H	$F = \overline{B}$	F = (A + B) plus $(A + \overline{B})$
L	H	H	L	$F = A \odot B$	F = A plus B
L	H	H	H	$F = A + \overline{B}$	F = A plus (A + B)
H	L	L	L	$F = \overline{A} \cdot B$	F = (A + $\overline{B}$) plus 0
H	L	L	H	$F = A \oplus B$	F = A minus B minus 1
H	L	H	L	F = B	F = (A + $\overline{B}$) plus (A + B)
H	L	H	H	F = A + B	F = A plus (A + $\overline{B}$)
H	H	L	L	F = Logical "0"	F = minus 1 (two's complement)
H	H	L	H	$F = A \cdot \overline{B}$	F = (A + $\overline{B}$) minus 1
H	H	H	L	F = A + B	F = (A + B) minus 1
H	H	H	H	F = A	F = A minus 1

PIN ASSIGNMENT



LOGIC DIAGRAM



ELECTRICAL CHARACTERISTICS (V_{EE} = −5.2 V ±5.0%) (See Note)

Characteristic	Symbol	0° Min	0° Max	25° Min	25° Max	75°C Min	75°C Max	Unit
Power Supply Current	I_E	—	159	—	145	—	159	mA
Input Current High	I_{inH}							μA
Pin 22		—	720	—	450	—	450	
Pins 14,23		—	405	—	255	—	255	
Pins 13,15,17		—	515	—	320	—	320	
Pins 10,16,18,21		—	475	—	300	—	300	
Pins 9,11,19,20		—	465	—	275	—	275	
Input Current Low Pins 9–11, 13–22	I_{inL}	0.5	—	0.5	—	0.3	—	μA
High Output Voltage	V_{OH}	−1.02	−0.84	−0.98	−0.81	−0.92	−0.735	Vdc
Low Output Voltage	V_{OL}	−1.95	−1.63	−1.95	−1.63	−1.95	−1.60	Vdc
High Input Voltage	V_{IH}	−1.17	−0.84	−1.13	−0.81	−1.07	−0.735	Vdc
Low Input Voltage	V_{IL}	−1.95	−1.48	−1.95	−1.48	−1.95	−1.45	Vdc

NOTE:
Each MECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts.

AC PARAMETERS

Characteristic	Symbol	Input	Output	Conditions†	AC Switching Characteristics 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit
Propagation Delay	t+ +,t− −	C_n	C_{n+4}	A0,A1,A2,A3	0.7	2.0	0.7	2.0	0.7	2.0	ns
Rise Time, Fall Time	t+,t−	C_n	C_{n+4}	A0,A1,A2,A3	0.7	2.2	0.7	2.0	0.7	2.2	ns
Propagation Delay	t+ +,t+ −	C_n	F1	A0	0.7	3.8	0.7	3.5	0.7	3.8	ns
	t− +,t− −	C_n	F1		0.7	3.8	0.7	3.5	0.7	3.8	
Rise Time, Fall Time	t+,t−	C_n	F1		0.7	2.2	0.7	2.0	0.7	2.2	
Propagation Delay	t+ +,t+ −	A1	F1		0.7	5.5	0.7	5.0	0.7	5.5	ns
	t− +,t− −	A1	F1		0.7	5.5	0.7	5.0	0.7	5.5	
Rise Time, Fall Time	t+,t−	A1	F1		0.7	2.2	0.7	2.0	0.7	2.2	
Propagation Delay	t+ +,t− −	A1	P_G	S0,S3	0.7	3.8	0.7	3.5	0.7	3.8	ns
Rise Time, Fall Time	t+,t−	A1	P_G	S0,S3	0.7	2.2	0.7	2.0	0.7	2.2	ns
Propagation Delay	t+ +,t− −	A1	G_G	A0,A2,A3,C_n	0.7	5.0	0.7	4.5	0.7	5.0	ns
Rise Time, Fall Time	t+,t−	A1	G_G	A0,A2,A3,C_n	0.7	2.2	0.7	2.0	0.7	2.2	ns
Propagation Delay	t+ −,t− +	A1	C_{n+4}	A0,A2,A3,C_n	0.7	6.0	0.7	5.4	0.7	6.0	ns
Rise Time, Fall Time	t+,t−	A1	C_{n+4}	A0,A2,A3,C_n	0.7	2.2	0.7	2.0	0.7	2.2	ns
Propagation Delay	t+ +,t− +	B1	F1	S3,C_n	0.7	7.0	0.7	6.5	0.7	7.0	ns
Rise Time, Fall Time	t+,t−	B1	F1	S3,C_n	0.7	2.2	0.7	2.0	0.7	2.2	ns
Propagation Delay	t+ +,t− −	B1	P_G	S0,A1	0.7	3.8	0.7	3.5	0.7	3.8	ns
Rise Time, Fall Time	t+,t−	B1	P_G	S0,A1	0.7	2.2	0.7	2.0	0.7	2.2	ns
Propagation Delay	t+ +,t− −	B1	G_G	S3,C_n	0.7	5.0	0.7	4.5	0.7	5.0	ns
Rise Time, Fall Time	t+,t−	B1	G_G	S3,C_n	0.7	2.2	0.7	2.0	0.7	2.2	ns
Propagation Delay	t+ −,t− +	B1	C_{n+4}	S3,C_n	0.7	6.0	0.7	5.4	0.7	6.0	ns
Rise Time, Fall Time	t+,t−	B1	C_{n+4}	S3,C_n	0.7	2.2	0.7	2.0	0.7	2.2	ns
Propagation Delay	t+ +,t+ −	M	F1	—	0.7	3.7	0.7	3.5	0.7	3.7	ns
Rise Time, Fall Time	t+,t−	M	F1	—	0.7	2.2	0.7	2.0	0.7	2.2	ns
Propagation Delay	t+ −,t− +	S1	F1	A1,B1	0.7	5.5	0.7	5.0	0.7	5.5	ns
Rise Time, Fall Time	t+,t−	S1	F1	A1,B1	0.7	2.2	0.7	2.0	0.7	2.2	ns
Propagation Delay	t− +,t+ −	S1	P_G	A3,B3	0.7	3.8	0.7	3.5	0.7	3.8	ns
Rise Time, Fall Time	t+,t−	S1	P_G	A3,B3	0.7	2.2	0.7	2.0	0.7	2.2	ns
Propagation Delay	t+ −,t− +	S1	C_{n+4}	A3,B3	0.7	6.0	0.7	5.4	0.7	6.0	ns
Rise Time, Fall Time	t+,t−	S1	C_{n+4}	A3,B3	0.7	2.2	0.7	2.0	0.7	2.2	ns
Propagation Delay	t+ −,t− +	S1	G_G	A3,B3	0.7	5.0	0.7	4.5	0.7	5.0	ns
Rise Time, Fall Time	t+,t−	S1	G_G	A3,B3	0.7	2.2	0.7	2.0	0.7	2.2	ns

†Logic high level (+1.11 Vdc) applied to pins listed. All other input pins are left floating or tied to +0.31 Vdc.
V_{CC1} = V_{CC2} = +2.0 Vdc, V_{EE} = −3.2 Vdc

MOTOROLA

MC10H186A

Advance Information

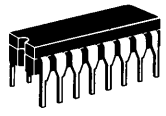
MECL 10KH HIGH-SPEED EMITTER-COUPLED LOGIC

The MC10H186A is a member of Motorola's new MECL family. The MC10H186A is a hex D type flip-flop with common reset and clock lines. This MECL 10KH part is a functional/pinout duplication of the standard MECL 10K family part, with 100% improvement in clock toggle frequency and propagation delay and no increase in power-supply current.

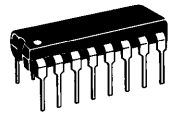
- Propagation Delay, 1.7 ns Typical
- Power Dissipation, 460 mW Typical
- Improved Noise Margin 150 mV (over operating voltage and temperature range)
- Voltage Compensated
- MECL 10K-Compatible

MECL 10KH

HEX-D FLIP FLOP



L SUFFIX
CERAMIC PACKAGE
CASE 620



P SUFFIX
PLASTIC PACKAGE
CASE 648

MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply (V_{CC} = 0)	V_{EE}	-8.0 to 0	Vdc
Input Voltage (V_{CC} = 0)	V_I	0 to V_{EE}	Vdc
Output Current — Continuous — Surge	I_{out}	50 100	mA
Operating Temperature Range	T_A	0–75	°C
Storage Temperature Range — Plastic — Ceramic	T_{stg}	-55 to 150 -55 to 165	°C °C

ELECTRICAL CHARACTERISTICS (V_{EE} = -5.2 V ±5%) (See Note)

Characteristic	Symbol	0°		25°		75°		Unit
		Min	Max	Min	Max	Min	Max	
Power Supply Current	I_E	—	121	—	110	—	121	mA
Input Current High	I_{inH}							μA
Pins 5,6,7,10,11,12		—	430	—	265	—	265	
Pin 9		—	670	—	420	—	420	
Pin 1		—	1900	—	1200	—	1200	μA
Input Current Low	I_{inL}	0.5	—	0.5	—	0.3	—	μA
High Output Voltage	V_{OH}	-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
Low Output Voltage	V_{OL}	-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
High Input Voltage	V_{IH}	-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
Low Input Voltage	V_{IL}	-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc

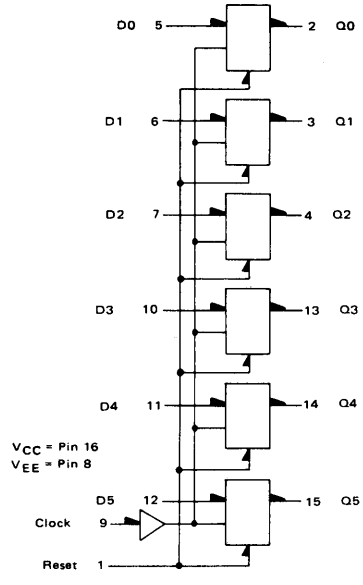
AC PARAMETERS

Propagation Delay	t_{pd}	0.7	3.0	0.7	2.7	0.7	3.0	ns
Set-up Time	t_{set}	1.5	—	1.5	—	1.5	—	ns
Hold Time	t_{hold}	1.0	—	1.0	—	1.0	—	ns
Rise Time	t_r	0.7	2.6	0.7	2.4	0.7	2.6	ns
Fall Time	t_f	0.7	2.6	0.7	2.4	0.7	2.6	ns
Toggle Frequency	f_{tog}	250	—	250	—	250	—	MHz
Reset Recovery Time (t_{1-9+})	t_{rr}	3.0	—	3.0	—	3.0	—	ns

NOTE:
Each MECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater then 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

HEX D MASTER—SLAVE FLIP-FLOP WITH RESET



CLOCKED TRUTH TABLE

R	C	Q	Qn+1
L	L	ϕ	Qn
L	H *	L	L
L	H *	H	H
H	I ϕ	ϕ	L

ϕ = Don't Care
*A clock H is a clock transition from a low to a high state.

APPLICATION INFORMATION

The MC10H186A contains six high-speed, master slave type "D" flip-flops. Data is entered into the master when the clock is low. Master-to-slave data transfer takes place on the positive-going Clock transition. Thus outputs may change only on a positive-going Clock transition. A change in the information present at the data (D) input will not affect the output information any other time due to the master-slave construction of this device. A common Reset is included in this circuit. The Reset overrides the clock.

MOTOROLA

MC10H188

Advance Information

MECL 10KH HIGH-SPEED EMITTER-COUPLED LOGIC

The MC10H188 is a member of Motorola's new MECL family. The MC10H188 is a high-speed Hex Buffer with a common Enable input. When Enable is in the high-state, all outputs are in the low-state. When Enable is in the low-state, the outputs take the same state as the inputs.

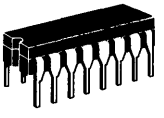
This MECL 10KH part is a functional/pinout duplication of the standard MECL 10K family part, with 100% improvement in propagation delay and no increase in power-supply current.

- Propagation Delay, 1.3 ns Typical Data-to-Output
- Power Dissipation 180 mW Typ/Pkg (No Load)
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible

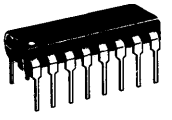
MECL 10KH

HEX BUFFER WITH ENABLE

2

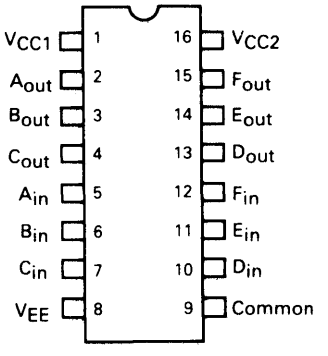


L SUFFIX
CERAMIC PACKAGE
CASE 620



P SUFFIX
PLASTIC PACKAGE
CASE 648

PIN ASSIGNMENT



MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply (V_{CC} = 0)	V_{EE}	-8.0 to 0	Vdc
Input Voltage (V_{CC} = 0)	V_I	0 to V_{EE}	Vdc
Output Current — Continuous — Surge	I_{out}	50 100	mA
Operating Temperature Range	T_A	0–+75	°C
Storage Temperature Range — Plastic — Ceramic	T_{stg}	-55 to +150 -55 to +165	°C °C

ELECTRICAL CHARACTERISTICS (V_{EE} = -5.2 V ±5%) (See Note)

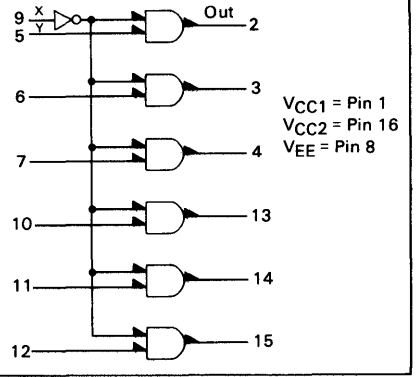
Characteristic	Symbol	0°		25°		75°		Unit
		Min	Max	Min	Max	Min	Max	
Power Supply Current	I_E	—	46	—	42	—	46	mA
Input Current High	I_{inH}	—	495	—	310	—	310	μA
Input Current Low	I_{inL}	0.5	—	0.5	—	0.3	—	μA
High Output Voltage	V_{OH}	-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
Low Output Voltage	V_{OL}	-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
High Input Voltage	V_{IH}	-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
Low Input Voltage	V_{IL}	-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc

AC PARAMETERS

Propagation Delay Enable Data	t_{pd}	 0.7 0.7	 2.2 1.9	 0.7 0.7	 2.0 1.7	 0.7 0.7	 2.2 1.9	ns
Rise Time	t_r	0.7	2.4	0.7	2.2	0.7	2.4	ns
Fall Time	t_f	0.7	2.4	0.7	2.2	0.7	2.4	ns

NOTE:
Each MECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Outputs are terminated through a 50 ohm resistor to -2.0 volts.

LOGIC DIAGRAM



This document contains information on a new product. Specifications and information herein are subject to change without notice.

TRUTH TABLE

Inputs		Output
X	Y	OUT
L	L	L
L	H	H
H	L	L
H	H	L

MOTOROLA

MC10H189

Advance Information

MECL 10KH HIGH-SPEED EMITTER-COUPLED LOGIC

The MC10H189 is a member of Motorola's new MECL family. The MC10H189 is a Hex Inverter with a common Enable input. The hex inverting function is provided when Enable is in the low-state. When Enable is in the high-state, all outputs are low.

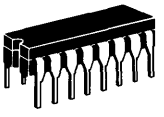
This MECL 10KH part is a functional/pinout duplication of the standard MECL 10K family part, with 100% improvement in propagation delay and no increase in power-supply current.

- Propagation Delay, 1.3 ns Typical Data-to-Output
- Power Dissipation 180 mW Typ/Pkg (No Load)
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible

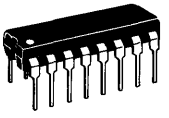
MECL 10KH

HEX INVERTER WITH ENABLE

2



L SUFFIX
CERAMIC PACKAGE
CASE 620



P SUFFIX
PLASTIC PACKAGE
CASE 648

MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply (V_{CC} = 0)	V_{EE}	-8.0 to 0	Vdc
Input Voltage (V_{CC} = 0)	V_I	0 to V_{EE}	Vdc
Output Current — Continuous — Surge	I_{out}	50 100	mA
Operating Temperature Range	T_A	0–+75	°C
Storage Temperature Range — Plastic — Ceramic	T_{stg}	-55 to +150 -55 to +165	°C °C

ELECTRICAL CHARACTERISTICS (V_{EE} = -5.2 V ±5%) (See Note)

Characteristic	Symbol	0°		25°		75°		Unit
		Min	Max	Min	Max	Min	Max	
Power Supply Current	I_E	—	46	—	42	—	46	mA
Input Current High	I_{inH}	—	495	—	310	—	310	μA
Input Current Low	I_{inL}	0.5	—	0.5	—	0.3	—	μA
High Output Voltage	V_{OH}	-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
Low Output Voltage	V_{OL}	-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
High Input Voltage	V_{IH}	-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
Low Input Voltage	V_{IL}	-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc

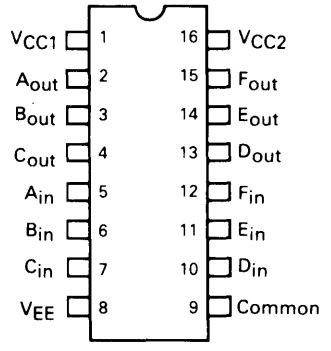
AC PARAMETERS

Propagation Delay Enable Data	t_{pd}	 0.7 0.7	 2.2 1.9	 0.7 0.7	 2.1 1.7	 0.7 0.7	 2.3 1.9	ns
Rise Time	t_r	0.7	2.4	0.7	2.2	0.7	2.4	ns
Fall Time	t_f	0.7	2.4	0.7	2.2	0.7	2.4	ns

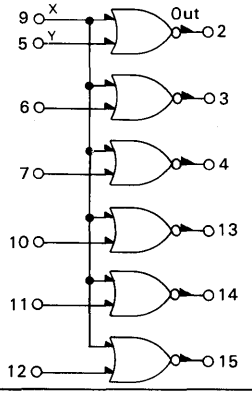
NOTE:
Each MECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Outputs are terminated through a 50 ohm resistor to -2.0 volts.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

PIN ASSIGNMENT



LOGIC DIAGRAM



V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

TRUTH TABLE

Inputs		Output
X	Y	OUT
L	L	H
L	H	L
H	L	L
H	H	L

MOTOROLA

MC10H209

Advance Information

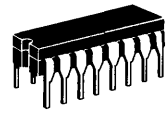
MECL 10KH

2

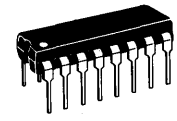
MECL 10KH HIGH-SPEED EMITTER—COUPLED LOGIC

The MC10H209 is a member of Motorola's new MECL family. It is a Dual 4-5-Input OR/NOR Gate. This MECL part is a functional/pinout duplication of the MECL III part MC1688.

- Propagation Delay Average, 0.75 ns Typical
- Power Dissipation 125 mW Typical
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible

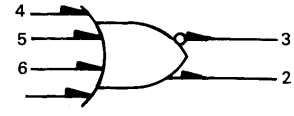


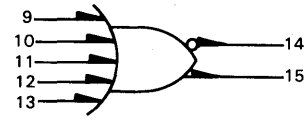
L SUFFIX
CERAMIC PACKAGE
CASE 620



P SUFFIX
PLASTIC PACKAGE
CASE 648

Dual 4-5-Input OR/NOR Gate





V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply (V_{CC} = 0)	V_{EE}	-8.0 to 0	Vdc
Input Voltage (V_{CC} = 0)	V_I	0 to V_{EE}	Vdc
Output Current — Continuous — Surge	I_{out}	50 100	mA
Operating Temperature Range	T_A	0–75	°C
Storage Temperature Range — Plastic — Ceramic	T_{stg}	-55 to +150 -55 to +165	°C °C

ELECTRICAL CHARACTERISTICS (V_{EE} = -5.2 V ±5%) (See Note)

Characteristic	Symbol	0°		25°		75°		Unit
		Min	Max	Min	Max	Min	Max	
Power Supply Current	I_E	—	—	—	30	—	—	mA
Input Current High	I_{inH}	—	640	—	400	—	400	μA
Input Current Low	I_{inL}	0.5	—	0.5	—	0.3	—	μA
High Output Voltage	V_{OH}	-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
Low Output Voltage	V_{OL}	-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
High Input Voltage	V_{IH}	-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
Low Input Voltage	V_{IL}	-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc

AC PARAMETERS

Propagation Delay	t_{pd}	0.4	1.0	0.4	1.0	0.4	1.1	ns
Rise Time	t_r	0.4	1.5	0.4	1.5	0.4	1.6	ns
Fall Time	t_f	0.4	1.5	0.4	1.5	0.4	1.6	ns

NOTE:
Each MECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Outputs are terminated through a 50 ohm resistor to -2.0 volts.

MOTOROLA

MC10H210
MC10H211

Advance Information

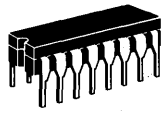
2

MECL 10KH HIGH-SPEED EMITTER-COUPLED LOGIC

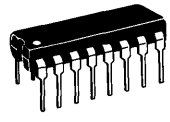
The MC10H210 and MC10H211 are members of Motorola's new MECL family. These devices are dual 3-input, 3-output "OR" and "NOR" gates respectively. These MECL 10KH parts are functional/pinout duplications of the standard MECL 10K family parts, with 100% improvement in propagation delay and no increase in power-supply current.

- Propagation Delay, 1.0 ns Typical
- Power Dissipation, 160 mW Typical
- Improved Noise Margin 150 mV (over operating voltage and temperature range)
- Voltage Compensated
- MECL 10K-Compatible

MECL 10KH

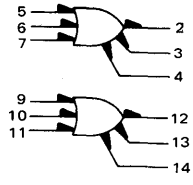


L SUFFIX
CERAMIC PACKAGE
CASE 620



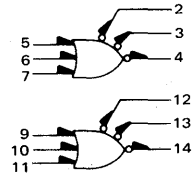
P SUFFIX
PLASTIC PACKAGE
CASE 648

MC10H210
3-INPUT 3-OUTPUT "OR" GATE



V_{CC1} = Pin 1, 15*
V_{CC2} = Pin 16
V_{EE} = Pin 8

MC10H211
3-INPUT 3-OUTPUT "NOR" GATE



MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply (V_{CC} = 0)	V_{EE}	-8.0 to 0	Vdc
Input Voltage (V_{CC} = 0)	V_I	0 to V_{EE}	Vdc
Output Current — Continuous — Surge	I_{out}	50 100	mA
Operating Temperature Range	T_A	0–75	°C
Storage Temperature Range — Plastic — Ceramic	T_{stg}	-55 to 150 -55 to 165	°C °C

ELECTRICAL CHARACTERISTICS (V_{EE} = -5.2 V ±5%) (See Note)

Characteristic	Symbol	0°		25°		75°		Unit
		Min	Max	Min	Max	Min	Max	
Power Supply Current	I_E	—	42	—	38	—	42	mA
Input Current High	I_{inH}	—	720	—	450	—	450	μA
Input Current Low	I_{inL}	0.5	—	0.5	—	0.3	—	μA
High Output Voltage	V_{OH}	-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
Low Output Voltage	V_{OL}	-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
High Input Voltage	V_{IH}	-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
Low Input Voltage	V_{IL}	-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc

AC PARAMETERS

Propagation Delay	t_{pd}	0.7	1.6	0.7	1.5	0.7	1.7	ns
Rise Time	t_r	0.7	2.2	0.7	2.0	0.7	2.2	ns
Fall Time	t_f	0.7	2.2	0.7	2.0	0.7	2.2	ns

*Pin 1 and 15 internally connected.

NOTE:
Each MECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater then 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

Note: If crosstalk is present, double bypass capacitor to 0.2μF.

MOTOROLA

MC10H330

Advance Information

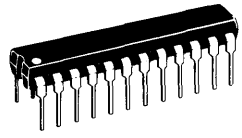
QUAD BUS DRIVER/RECEIVER WITH 2-TO-1 OUTPUT MULTIPLEXERS

The MC10H330 is a member of Motorola's new MECL family. The MC10H330 is a Quad Bus Driver/Receiver with two-to-one output multiplexers. These multiplexers have a common select and output enable. When disabled, ($\overline{OE}$ = high) the bus outputs go to −2.0 V. The receivers have 200 mV of hysteresis on their bus inputs. Their output can be brought to a low state (V_{OL}) by applying a high level to the receiver enable ($\overline{RE}$ = High). The parameters specified are with 25 Ω loading on the bus drivers and 50 Ω loads on the receivers.

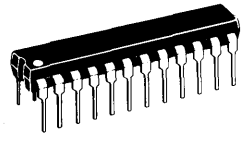
- Propagation Delay 1.5 ns Typical Data-to-Output
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible

MECL 10KH

QUAD BUS DRIVER/RECEIVER WITH 2-TO-1 OUTPUT MULTIPLEXERS

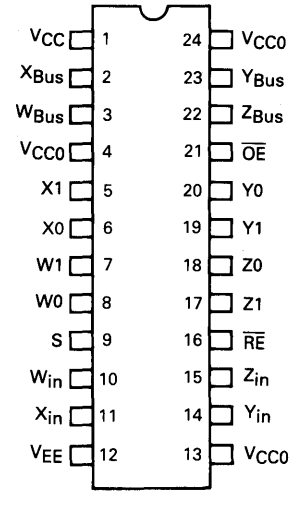


L SUFFIX
CERAMIC CASE
CASE 758



P SUFFIX
PLASTIC CASE
CASE 724

PIN ASSIGNMENT



MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply (V_{CC} = 0)	V_{EE}	−8.0 to 0	Vdc
Input Voltage (V_{CC} = 0)	V_I	0 to V_{EE}	Vdc
Output Current — Continuous — Surge	I_{out}	50 100	mA
Operating Temperature Range	T_A	0 to +75	°C
Storage Temperature Range — Plastic — Ceramic	T_{stg}	−55 to +150 −55 to +165	°C °C

ELECTRICAL CHARACTERISTICS (V_{EE} = −5.2 V ±5.0%) (See Note)

		0°		25°		75°C		
Characteristic	Symbol	Min	Max	Min	Max	Min	Max	Unit
Power Supply Current	I_E	—	157	—	143	—	157	mA
Input Current High Pins 5-8, 17-20 Pins 16, 21 Pin 9	I_{inH}	 — — —	 667 514 475	 — — —	 417 321 297	 — — —	 417 321 297	μA
Input Current Low	I_{inL}	0.5	—	0.5	—	0.3	—	μA
High Output Voltage	V_{OH}	−1.02	−0.84	−0.98	−0.81	−0.92	−0.735	Vdc
Low Output Voltage	V_{OL}	−1.95	−1.63	−1.95	−1.63	−1.95	−1.60	Vdc
High Input Voltage	V_{IH}	−1.17	−0.84	−1.13	−0.81	−1.07	−0.735	Vdc
Low Input Voltage	V_{IL}	−1.95	−1.48	−1.95	−1.48	−1.95	−1.45	Vdc

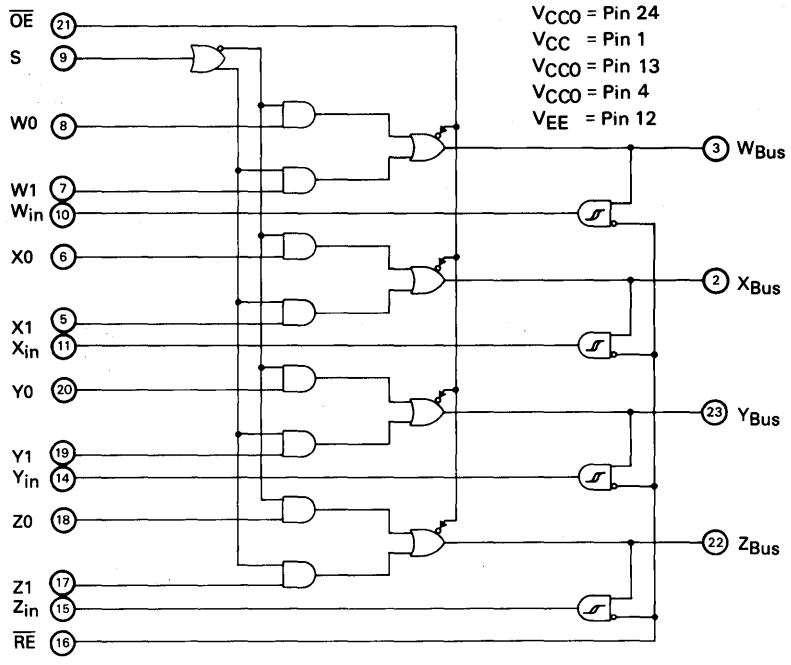
AC PARAMETERS

Propagation Delay Data-to-Bus Output Select-to-Bus Output $\overline{OE}$-to-Bus Output Bus-to-Input $\overline{RE}$-to-Input	t_{pd}	 0.8 1.0 1.0 0.8 0.8	 2.0 3.2 2.4 2.1 2.2	 0.8 1.0 1.0 0.8 0.8	 2.0 3.2 2.4 2.1 2.2	 0.8 1.0 1.0 0.8 0.8	 2.2 3.4 2.5 2.4 2.5	ns
Rise Time	t_r	0.8	2.0	0.8	2.0	0.8	2.1	ns
Fall Time	t_f	0.8	2.0	0.8	2.0	0.8	2.1	ns

NOTE:
Each MECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts.

2

LOGIC DIAGRAM



MULTIPLEXER TRUTH TABLE

$\overline{OE}$	S	W_{Bus}	X_{Bus}	Y_{Bus}	Z_{Bus}
H	X	−2.0 V	−2.0 V	−2.0 V	−2.0 V
L	L	W0	X0	Y0	Z0
L	H	W1	X1	Y1	Z1

X — Don't care

RECEIVER TRUTH TABLE

$\overline{RE}$	W_{in}	X_{in}	Y_{in}	Z_{in}
H	L	L	L	L
L	W_{Bus}	X_{Bus}	Y_{Bus}	Z_{Bus}

MOTOROLA

MC10H332

Advance Information

DUAL BUS DRIVER/RECEIVER WITH 4-TO-1 OUTPUT MULTIPLEXERS

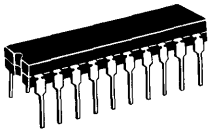
The MC10H332 is a member of Motorola's new MECL family. The MC10H332 is a Dual Bus Driver/Receiver with four-to-one output multiplexers. These multiplexers have common selects and output enable. When disabled, ($\overline{OE}$ = high) the bus outputs go to −2.0 V. The receivers have 200 mV of hysteresis on their bus inputs. The parameters specified are with 25 Ω loading on the bus drivers and 50 Ω loads on the receivers.

- Propagation Delay, 1.5 ns Typical Data-to-Output
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K — Compatible

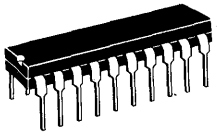
MECL 10KH

DUAL BUS DRIVER/RECEIVER WITH 4-TO-1 OUTPUT MULTIPLEXERS

2

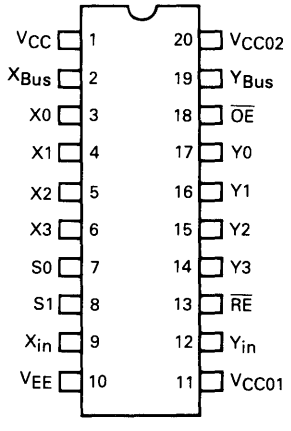


L SUFFIX
CERAMIC CASE
CASE 732



P SUFFIX
PLASTIC CASE
CASE 738

PIN ASSIGNMENT



MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply (V_{CC} = 0)	V_{EE}	−8.0 to 0	Vdc
Input Voltage (V_{CC} = 0)	V_I	0 to V_{EE}	Vdc
Output Current — Continuous — Surge	I_{out}	50 100	mA
Operating Temperature Range	T_A	0 to +75	°C
Storage Temperature Range — Plastic — Ceramic	T_{stg}	−55 to +150 −55 to +165	°C °C

ELECTRICAL CHARACTERISTICS (V_{EE} = −5.2 V ±5.0%) (See Note)

		0°		25°		75°C		
Characteristic	Symbol	Min	Max	Min	Max	Min	Max	Unit
Power Supply Current	I_E	—	115	—	110	—	115	mA
Input Current High Pins 3,4,5,6,14,15,16,17 Pins 7,8 Pin 13,18	I_{inH}	 — — —	 667 437 456	 — — —	 417 273 285	 — — —	 417 273 285	μA
Input Current Low	I_{inL}	0.5	—	0.5	—	0.3	—	μA
High Output Voltage	V_{OH}	−1.02	−0.84	−0.98	−0.81	−0.92	−0.735	Vdc
Low Output Voltage	V_{OL}	−1.95	−1.63	−1.95	−1.63	−1.95	−1.60	Vdc
High Input Voltage	V_{IH}	−1.17	−0.84	−1.13	−0.81	−1.07	−0.735	Vdc
Low Input Voltage	V_{IL}	−1.95	−1.48	−1.95	−1.48	−1.95	−1.45	Vdc

AC PARAMETERS

Propagation Delay Data-to-Bus Output Select-to-Bus Output $\overline{OE}$-to-Bus Output Bus-to-Input $\overline{RE}$-to-Input	t_{pd}	 1.0 1.0 0.8 0.8 0.8	 3.2 3.6 2.4 2.1 2.2	 1.0 1.0 0.8 0.8 0.8	 3.2 3.6 2.2 2.1 2.2	 1.0 1.0 0.8 0.8 0.8	 3.4 4.0 2.6 2.4 2.5	ns
Rise Time	t_r	0.8	2.0	0.8	2.0	0.8	2.1	ns
Fall Time	t_f	0.8	2.0	0.8	2.0	0.8	2.1	ns

NOTE:
Each MECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts.

MULTIPLEXER TRUTH TABLE

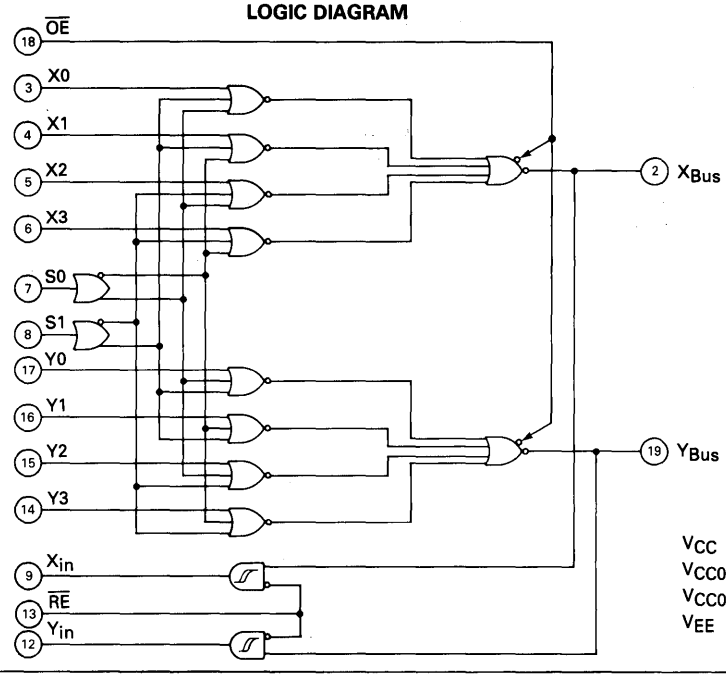
$\overline{OE}$	S1	S0	X_{Bus}	Y_{Bus}
H	X	X	-2.0 V	-2.0 V
L	L	L	X0	Y0
L	L	H	X1	Y1
L	H	L	X2	Y2
L	H	H	X3	Y3

X — Don't care

RECEIVER TRUTH TABLE

$\overline{RE}$	X_{in}	Y_{in}
H	L	L
L	X_{Bus}	Y_{Bus}

LOGIC DIAGRAM



MOTOROLA

MC10H334

Advance Information

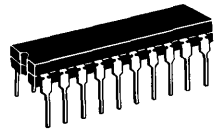
QUAD BUS DRIVER/RECEIVER WITH TRANSMIT AND RECEIVER LATCHES

The MC10H334 is a member of Motorola's new MECL family. The MC10H334 is a Quad Bus Driver/Receiver with transmit and receiver latches. When disabled, ($\overline{OE}$ = high) the bus outputs will fall to −2.0 V. Data to be transmitted or received is passed through its respective latch when the respective latch enable ($\overline{DLE}$ and $\overline{RLE}$) is at a low level. Information is latched on the positive transition of $\overline{DLE}$ and $\overline{RLE}$. The receivers have 200 mV of hysteresis on their bus inputs. The parameters specified are with 25 Ω loading on the bus drivers and 50 Ω loads on the receivers.

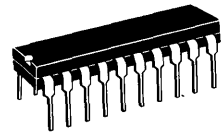
- Propagation Delay, 1.6 ns Typical Data-to-Output
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible

MECL 10KH

QUAD BUS DRIVER/RECEIVER WITH TRANSMIT AND RECEIVER LATCHES

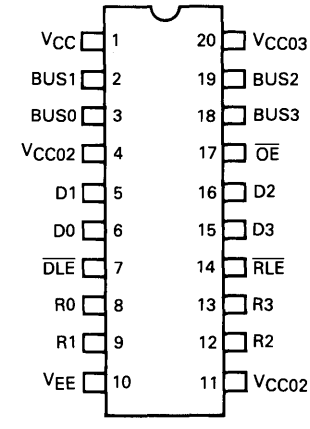


L SUFFIX
CERAMIC CASE
CASE 732



P SUFFIX
PLASTIC CASE
CASE 738

PIN ASSIGNMENT



MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply (V_{CC} = 0)	V_{EE}	−8.0 to 0	Vdc
Input Voltage (V_{CC} = 0)	V_I	0 to V_{EE}	Vdc
Output Current — Continuous — Surge	I_{out}	50 100	mA
Operating Temperature Range	T_A	0 to +75	°C
Storage Temperature Range — Plastic — Ceramic	T_{stg}	−55 to +150 −55 to +165	°C °C

ELECTRICAL CHARACTERISTICS (V_{EE} = −5.2 V ±5.0 %) (See Note)

		0°		25°		75°C		
Characteristic	Symbol	Min	Max	Min	Max	Min	Max	Unit
Power Supply Current	I_E	—	161	—	161	—	161	mA
Input Current High Pins 5,6,15,16 Pin 7, 14 Pin 17	I_{inH}	 — — —	 397 460 520	 — — —	 273 297 357	 — — —	 273 297 357	μA
Input Current Low	I_{inL}	0.5	—	0.5	—	0.3	—	μA
High Output Voltage	V_{OH}	−1.02	−0.84	−0.98	−0.81	−0.92	−0.735	Vdc
Low Output Voltage	V_{OL}	−1.95	−1.63	−1.95	−1.63	−1.95	−1.60	Vdc
High Input Voltage	V_{IH}	−1.17	−0.84	−1.13	−0.81	−1.07	−0.735	Vdc
Low Input Voltage	V_{IL}	−1.95	−1.48	−1.95	−1.48	−1.95	−1.45	Vdc

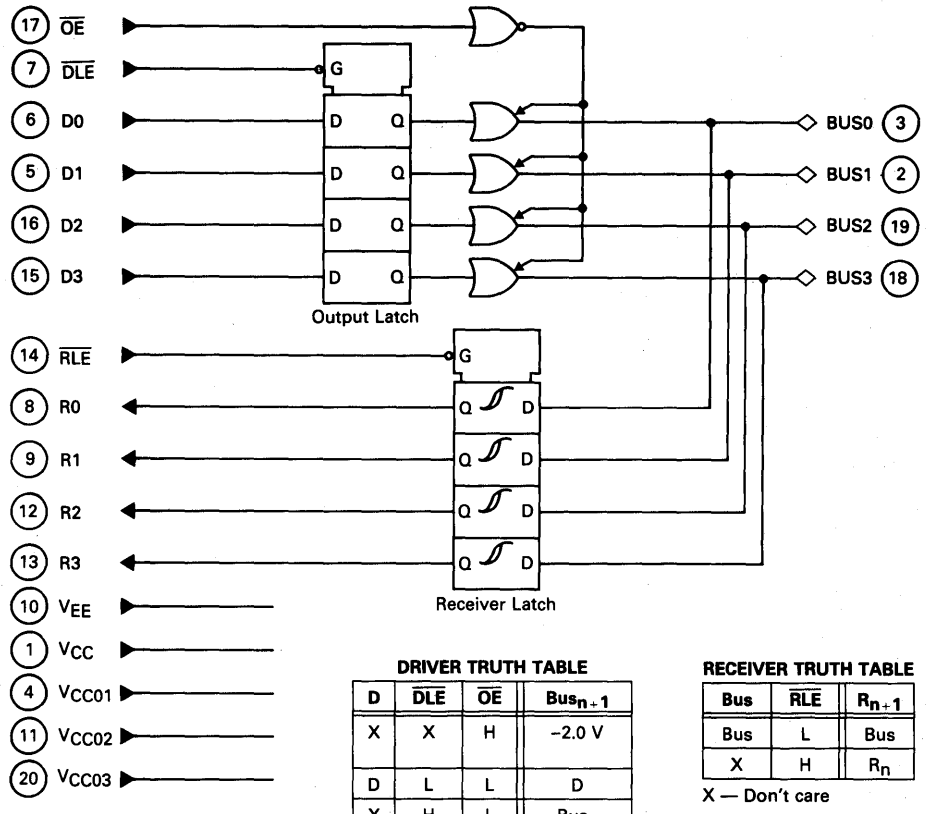
AC PARAMETERS

Propagation Delay Data-to-Bus Output $\overline{DLE}$-to-Bus Output $\overline{OE}$-to-Bus Output Bus-to-R0 $\overline{RLE}$-to-R0	t_{pd}	 — — — — —	 2.5 2.7 2.5 1.9 2.1	 — — — — —	 2.5 2.7 2.5 1.9 2.0	 — — — — —	 2.5 3.0 2.5 1.9 2.1	ns
Rise Time	t_r	0.8	2.2	0.7	2.0	0.8	2.2	ns
Fall Time	t_f	0.8	2.2	0.7	2.0	0.8	2.2	ns

NOTE:
Each MECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts.

2

LOGIC DIAGRAM



DRIVER TRUTH TABLE

D	$\overline{DLE}$	$\overline{OE}$	Bus_{n+1}
X	X	H	−2.0 V
D	L	L	D
X	H	L	Bus_n

X — Don't care

RECEIVER TRUTH TABLE

Bus	$\overline{RLE}$	R_{n+1}
Bus	L	Bus
X	H	R_n

X — Don't care

MOTOROLA

MC10H350

Advance Information

SINGLE ECL TO TTL TRANSLATOR SUPPLY

The MC10H350 is a member of Motorola's new MECL family, MECL 10KH. The MC10H350 is an ECL to TTL translator which was designed to operate from a single power supply of either V_{CC} = +5.0 V or V_{EE} = -5.2 V.

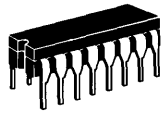
The MC10H350 incorporates ECL differential inputs and Schottky 3-state outputs. Differential inputs allow for use as an inverting/non-inverting translator, as a differential line receiver or as a high performance comparator. The 3-state outputs produce a high impedance output when the output enable ($\overline{OE}$) is brought high.

- Propagation Delay, 3.5 ns Typical
- MECL 10K-Compatible
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)

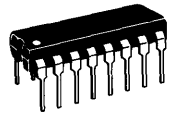
MECL 10KH

ECL TO TTL TRANSLATOR

2



L SUFFIX
CERAMIC PACKAGE
CASE 620



P SUFFIX
PLASTIC PACKAGE
CASE 648

MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply (V_{EE} = Gnd)	V_{CC}	7.0	Vdc
Operating Temperature Range	T_A	0 to +75	°C
Storage Temperature Range—Plastic —Ceramic	T_{stg}	-55 to +150 -55 to +165	°C °C

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V ±5%) (See Note)

Characteristic		Symbol	T_A = 0°C to 75°C Min	T_A = 0°C to 75°C Max	Unit
Power Supply Current	TTL ECL	I_{CC}		27 3.0	mA
Input Current High	TTL ECL	I_{IH}		20 50	μA
Input Current Low	TTL ECL	I_{IL}		-0.6 50	mA μA
Input Voltage High	TTL	V_{IH}	2.0		Vdc
Input Voltage Low	TTL	V_{IL}		0.8	Vdc
Differential Input Voltage		V_{DIFF}	200		mV
Voltage Common Mode		V_{CM}	2.8	5.0	Vdc
Output Voltage High I_{OH} = 3 mA		V_{OH}	2.7		Vdc
Output Voltage Low I_{OL} = 20 mA		V_{OL}		0.5	Vdc
Short Circuit Current V_{OUT} = 0V		I_{OS}	-60	-150	mA
Output Disable Current High V_{OUT} = 2.7 V		I_{OZH}		50	μA
Output Disable Current Low V_{OUT} = 0.5 V		I_{OZL}		-50	μA

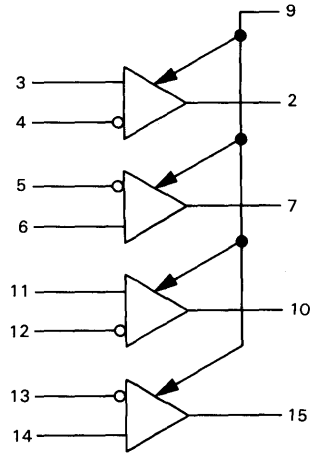
AC PARAMETERS (C_L = 50 PF) (V_{CC} = 5.0 ±5%) (T_A = 0°C to 75°C)

Propagation Delay	t_{pd}			
Data		—	5.0	ns
Enable	t_{PLZ}	—	7.0	ns
	t_{PHZ}	—	8.0	ns
	t_{PZL}	—	5.0	ns
	t_{PZH}	—	5.5	ns

NOTE: Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

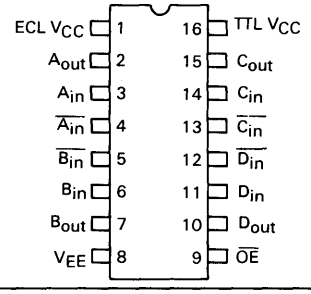
This document contains information on a new product. Specifications and information herein are subject to change without notice.

LOGIC DIAGRAM



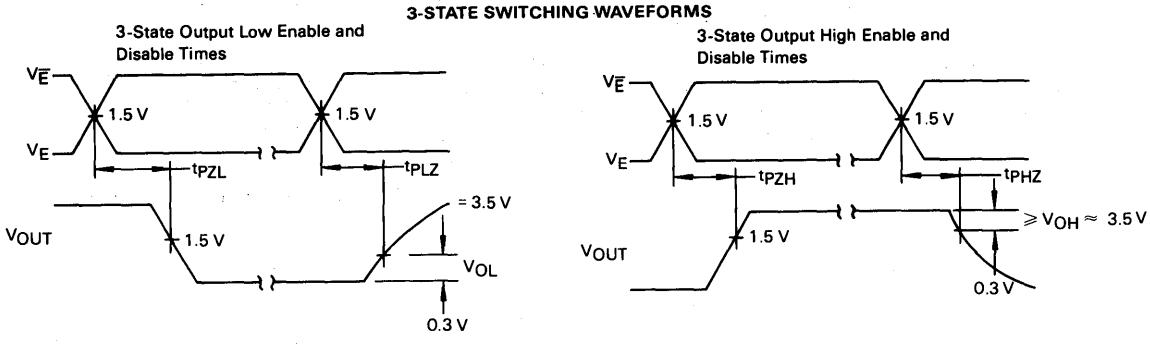
V_{CC} (+5.0 Vdc) = Pins 1 and 16
V_{EE} (Gnd) = Pin 8

PIN ASSIGNMENT

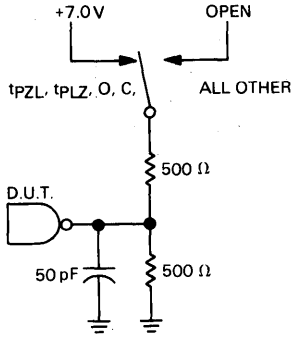


2

3-STATE SWITCHING WAVEFORMS



TEST LOAD



*INCLUDES JIG AND PROBE CAPACITANCE

MOTOROLA

MC10H423

Advance Information

TRIPLE 3 INPUT BUS DRIVER WITH ENABLE

The MC10H423 is a member of Motorola's new MECL family. The MC10H423 is a triple 3 Input Bus Driver with a common enable.

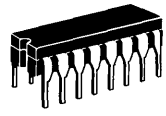
The MC10H423 consists of three NOR gates designed for bus driving applications on card or between cards. Output low logic levels are specified with $V_{OL} \leq -2.0$ Vdc so that the bus may be terminated to -2.0 Vdc. The gate output, when low, appears as a high impedance to the bus, because the output emitter-followers of the MC10H423 are "turned off." This eliminates discontinuities in the characteristic impedance of the bus.

The V_{OH} level is specified when driving a 25-ohm load terminated to -2.0 Vdc, the equivalent of a 50-ohm bus terminated at both ends. Although 25 ohms is the lowest characteristic impedance that can be driven by the MC10H423, higher impedance values may be used with this part. A typical 50-ohm bus is shown in Figure 1.

- Propagation Delay, 1.5 ns Typical
- Voltage Compensated
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- MECL 10K-Compatible

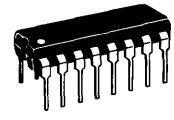
MECL 10KH

TRIPLE 3 INPUT BUS DRIVER WITH ENABLE



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648



MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply (V_{CC} = 0)	V_{EE}	-8.0 to 0	Vdc
Input Voltage (V_{CC} = 0)	V_I	0 to V_{EE}	Vdc
Output Current — Continuous — Surge	I_{out}	50 100	mA
Operating Temperature Range	T_A	0 to +75	°C
Storage Temperature Range — Plastic — Ceramic	T_{stg}	-55 to +150 -55 to +165	°C °C

ELECTRICAL CHARACTERISTICS (V_{EE} = -5.2 V ±5%) (See Note)

Characteristic	Symbol	0°		25°		75°		Unit
		Min	Max	Min	Max	Min	Max	
Power Supply Current	I_E	—	60	—	56	—	60	mA
Input Current High Pins 4,5,6,9,10,11,12,13,14 Pin 7	I_{inH}	— —	495 765	— —	310 475	— —	310 475	μA
Input Current Low	I_{inL}	0.5	—	0.5	—	0.3	—	μA
High Output Voltage	V_{OH}	-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
Low Output Voltage	V_{OL}	-2.1	-2.03	-2.1	-2.03	-2.1	-2.03	Vdc
High Input Voltage	V_{IH}	-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
Low Input Voltage	V_{IL}	-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc

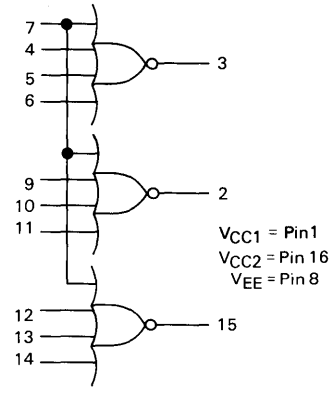
AC PARAMETERS

Propagation Delay	t_{pd}	0.7	2.3	0.7	2.3	0.7	2.3	ns
Rise Time	t_r	0.7	2.5	0.7	2.5	0.7	2.5	ns
Fall Time	t_f	0.7	2.5	0.7	2.5	0.7	2.5	ns

NOTE:
Each MECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Outputs are terminated through a 50 ohm resistor to -2.0 volts.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

LOGIC DIAGRAM



PIN ASSIGNMENT

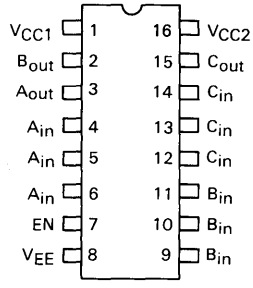
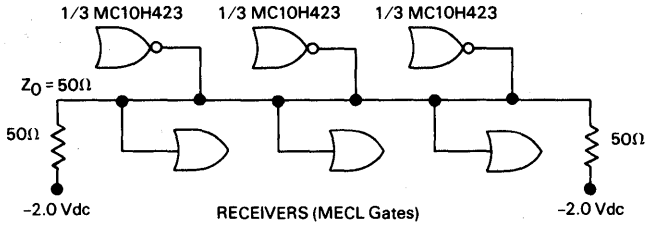


FIGURE 1 — 50-OHM BUS DRIVER



MOTOROLA

MC10H424

Advance Information

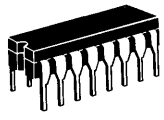
MECL 10KH HIGH-SPEED EMITTER-COUPLED LOGIC

The MC10H424 is a member of Motorola's new MECL family. The MC10H424 is a Quad TTL-to-ECL translator with an ECL strobe. Power supply requirements are ground, +5.0 volts, and −5.2 volts.

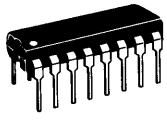
- Propagation Delay, 1.5 ns Typical
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible

MECL 10KH

QUAD TTL-TO-ECL TRANSLATOR WITH AN ECL STROBE



L SUFFIX
CERAMIC PACKAGE
CASE 620



P SUFFIX
PLASTIC PACKAGE
CASE 648

MAXIMUM RATINGS

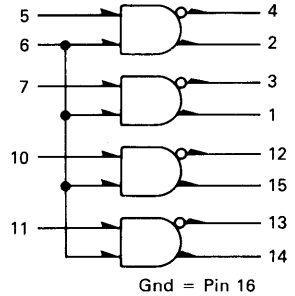
Characteristic	Symbol	Rating	Unit
Power Supply (V_{CC} = 5.0 V)	V_{EE}	−8.0 to 0	Vdc
Power Supply (V_{EE} = −5.2 V)	V_{CC}	0 to +7.0	Vdc
Input Voltage (ECL)	V_I	0 to V_{EE}	Vdc
Input Voltage (TTL)	V_I	0 to V_{CC}	Vdc
Output Current — Continuous — Surge	I_{out}	50 100	mA
Operating Temperature Range	T_A	0 to +75	°C
Storage Temperature Range — Plastic — Ceramic	T_{stg}	−55 to +150 −55 to +165	°C

ELECTRICAL CHARACTERISTICS (V_{EE} = −5.2 V ± 5%, V_{CC} = 5.0 V ± 5.0%)

Characteristic	Symbol	0° Min	0° Max	25° Min	25° Max	75°C Min	75°C Max	Unit
Negative Power Supply Drain Current	I_E	—	72	—	66	—	72	mAdc
Positive Power Supply Drain Current	I_{CCH}	—	16	—	16	—	18	mAdc
	I_{CCL}	—	25	—	25	—	25	mAdc
Reverse Current Pin 5,7,10,11	I_R	—	50	—	50	—	50	μAdc
Forward Current Pin 5,7,10,11	I_F	—	−3.2	—	−3.2	—	−3.2	mAdc
Input HIGH Current Pin 6	I_{inH}	—	450	—	310	—	310	μAdc
Input LOW Current Pin 6	I_{inL}	0.5	—	0.5	—	0.3	—	μAdc
Input Breakdown Voltage	$V_{(BR)in}$	5.5	—	5.5	—	5.5	—	Vdc
Input Clamp Voltage	V_I	—	−1.5	—	−1.5	—	−1.5	Vdc
High Output Voltage	V_{OH}	−1.02	−0.84	−0.98	−0.81	−0.92	−0.735	Vdc
Low Output Voltage	V_{OL}	−1.95	−1.63	−1.95	−1.63	−1.95	−1.60	Vdc
High Input Voltage Pin 5,7,10,11	V_{IH}	2.0	—	2.0	—	+2.0	—	Vdc
Low Input Voltage Pin 5,7,10,11	V_{IL}	—	0.8	—	0.8	—	0.8	Vdc
High Input Voltage Pin 6	V_{IH}	−1.17	−0.84	−1.13	−0.81	−1.07	−0.735	Vdc
Low Input Voltage Pin 6	V_{IL}	−1.95	−1.48	−1.95	−1.48	−1.95	−1.45	Vdc

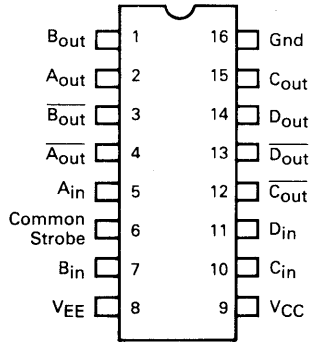
This document contains information on a new product. Specifications and information herein are subject to change without notice.

QUAD TTL-TO-ECL TRANSLATOR (ECL STROBE)



Gnd = Pin 16
V_{CC} (+5.0 Vdc) = Pin 9
V_{EE} (−5.2 Vdc) = Pin 8

PIN ASSIGNMENT



AC PARAMETERS

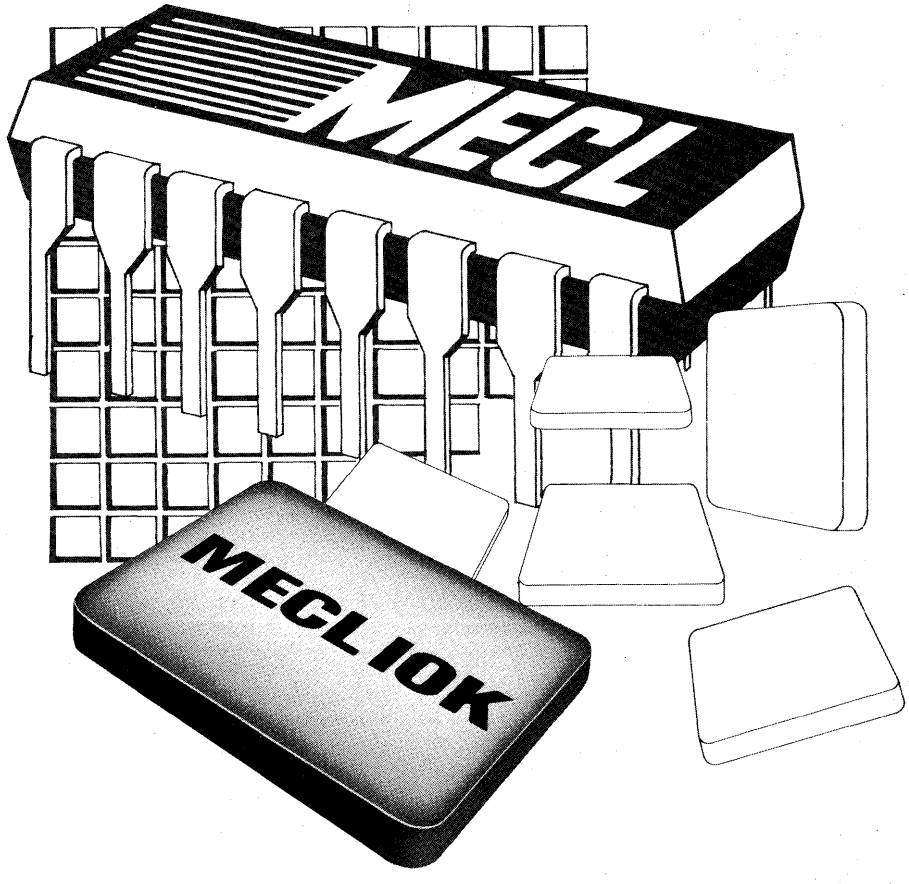
Propagation Delay	t_{pd}	0.7	3.4	0.7	3.0	0.7	3.4	ns
Rise Time	t_r	0.7	2.2	0.7	2.0	0.7	2.2	ns
Fall Time	t_f	0.7	2.2	0.7	2.0	0.7	2.2	ns

NOTE:
Each MECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts.

APPLICATIONS INFORMATION

The MC10H424 has TTL-compatible inputs, an ECL strobe and MECL complementary open-emitter outputs that allow use as an inverting/non-inverting translator or as a differential line driver. When the common strobe input is at the low-logic level, it forces all true outputs to a MECL low-logic state and all inverting outputs to a MECL high-logic state.

An advantage of this device is that TTL-level information can be transmitted differentially, via balanced twisted pair lines, to MECL equipment, where the signal can be received by the MC10H115 or MC10H116 differential line receivers.

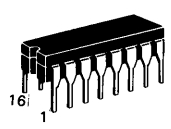

MECL
MECL 10K

MECL 10K
INTEGRATED CIRCUITS

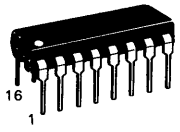
MC10,100/10,200 Series
−30 to 85°C

3

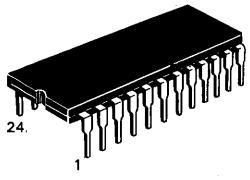
Standard Packages



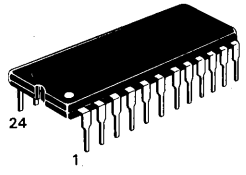
L SUFFIX
CERAMIC PACKAGE
CASE 620



P SUFFIX
PLASTIC PACKAGE
CASE 648

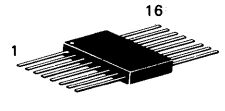


L SUFFIX
CERAMIC PACKAGE
CASE 623

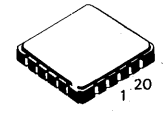


P SUFFIX
PLASTIC PACKAGE
CASE 649

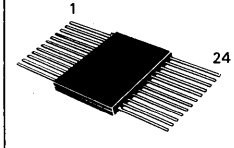
Special Packages



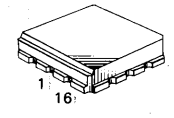
F SUFFIX
CERAMIC PACKAGE
CASE 650



Z SUFFIX
CERAMIC PACKAGE
CASE 756



F SUFFIX
CERAMIC PACKAGE
CASE 652



ZA SUFFIX
CERAMIC PACKAGE
CASE 757

Function Selection—(-30° to +85°C)

Function	Device	Case
NOR Gates		
Quad 2-Input Gate/Strobe	MC10100	620, 648
Quad 2-Input Gate	MC10102	620, 648
Triple 4-3-3 Input Gate	MC10106	620, 648
Dual 3-Input 3-Output Gate	MC10111	620, 648
Dual 3-Input 3-Output Gate	MC10211	620, 648
OR Gates		
Quad 2-Input Gate	MC10103	620, 648
Dual 3-Input 3-Output Gate	MC10110	620, 648
Dual 3-Input 3-Output Gate	MC10210	620, 648
AND Gates		
Quad 2-Input Gate	MC10104	620, 648
Hex Gate	MC10197	620, 648
Complex Gates		
Quad OR/NOR Gate	MC10101	620, 648
Triple 2-3-2 Input OR/NOR Gate	MC10105	620, 648
Dual 4-5 Input OR/NOR Gate	MC10109	620, 648
Dual 3-Input 3-Output OR/NOR Gate	MC10212	620, 648
Triple 2-Input Exclusive OR/NOR Gate	MC10107	620, 648
Quad 2-Input Exclusive OR/NOR Gate	MC10113	620, 648
Dual 2-Wide 2-3 Input OR-AND/OR-AND INVERT	MC10117	620, 648
Dual 2-Wide 3-Input OR-AND	MC10118	620, 648
4-Wide 4-3-3-3 Input OR-AND	MC10119	620, 648
4-Wide 3-Input OR-AND/OR-AND-INVERT	MC10121	620, 648

Function	Device	Case
Buffers/Inverters		
Hex Buffer/Enable	MC10188	620, 648
Hex Inverter/Enable	MC10189	620, 648
Hex Inverter/Buffer	MC10195	620, 648
Line Drivers/Line Receivers		
Triple Line Receiver	MC10114	620, 648
Quad Line Receiver	MC10115	620, 648
Triple Line Receiver	MC10116	620, 648
Quad Bus Receiver	MC10129	620, 648
Quad Bus Driver	MC10192	620, 648
Triple Line Receiver	MC10216	620, 648
Triple 4-3-3 Input Bus Driver	MC10123	620, 648
Dual Bus Driver	MC10128	620
Dual Transceiver	MC10194	620, 648
Translators		
Quad TTL-MECL	MC10124	620, 648
Quad MECL-TTL	MC10125	620, 648
Triple MECL-MOS	MC10177	620, 648
Quad MST to MECL	MC10190	620, 648
Hex MECL-MST	MC10191	620, 648

Function	Device	Case
Flip-Flop/Latches		
Dual D Master Slave Flip-Flop	MC10131	620, 648
Dual J-K Master Slave Flip-Flop	MC10135	620, 648
Hex D Master Slave Flip-Flop	MC10176	620, 648
Hex D Common Reset Flip-Flop	MC10186	620, 648
Dual D Master Slave Flip-Flop	MC10231	620, 648
Quad Latch	MC10133	620, 648
Quint Latch	MC10175	620, 648
Quad/Common Clock Latch	MC10168	620, 648
Quad/Negative Clock Latch	MC10153	620, 648
Dual Latch	MC10130	620, 648
Encoders		
8-Input Encoder	MC10165	620, 648
Decoders		
Binary to 1-8 (Low)	MC10161	620, 648
Binary to 1-8 (High)	MC10162	620, 648
Dual Binary to 1-4 (Low)	MC10171	620, 648
Dual Binary to 1-4 (High)	MC10172	620, 648
Parity Generator/Checkers		
12-Bit Parity Generator-Checker	MC10160	620, 648
9 + 2 Bit Parity	MC10170	620, 648
Error Detector/Correction		
IBM Code	MC10163	620, 648
Motorola Code	MC10193	620, 648

Function	Device	Case
Counters		
Hexadecimal	MC10136	620, 648
Decade	MC10137	620, 648
Biquinary	MC10138	620, 648
Binary Down Counter	MC10154	620, 648
Binary	MC10178	620, 648
Arithmetic Functions		
5-Bit Magnitude Comparator	MC10166	620, 648
Look Ahead Carry Block	MC10179	620, 648
Dual 2-Bit Adder/Subtractor	MC10180	620, 648
4-Bit Arithmetic Function Gen.	MC10181	620, 648
2-Bit Arithmetic Function Gen.	MC10182	620, 648
4 × 2 Multiplier	MC10183	623
2-Bit Multiplier	MC10287	620, 648
Shift Register		
4-Bit Universal	MC10141	620, 648
Multivibrators		
Monostable Multivibrators	MC10198	620, 648
Multiplexer		
Quad 2-Input/Noninverting	MC10158	620, 648
Dual Multiplexer/Latch	MC10132	620, 648
Dual Multiplexer/Latch	MC10134	620, 648
Quad 2-Input/Inverting	MC10159	620, 648
8-Line	MC10164	620, 648
Quad 2-Input/Latch	MC10173	620, 648
Dual 4-1	MC10174	620, 648

MOTOROLA

MC10100

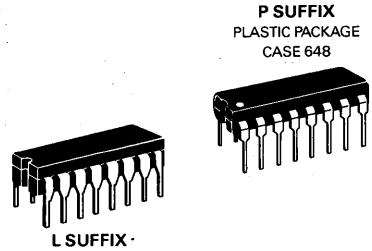
MECL 10K SERIES

QUAD 2-INPUT NOR GATE WITH STROBE

The MC10100 is a quad NOR gate. Each gate has 3 inputs, two of which are independent and one of which is tied common to all four gates.

P_D = 25 mW typ/gate (No Load)
t_{pd} = 2.0 ns typ
t_r, t_f = 2.0 ns typ (20-80%)

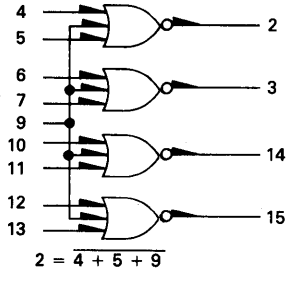
QUAD 2-INPUT NOR GATE WITH STROBE



P SUFFIX
PLASTIC PACKAGE
CASE 648

L SUFFIX
CERAMIC PACKAGE
CASE 620

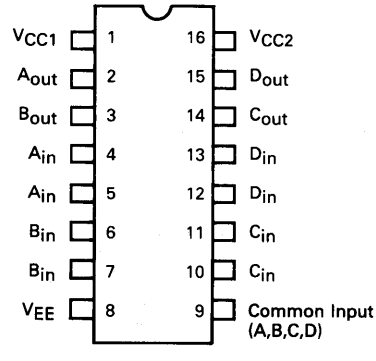
LOGIC DIAGRAM



$2 = \overline{4 + 5 + 9}$

V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

PIN ASSIGNMENT



ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown for only one input and one output. The other inputs and outputs are tested in the same manner.

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10100 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	29	–	21	26	–	29	mAdc	–	–	–	–	8	1,16
Input Current	I_{inH}	4*	–	390	–	–	245	–	245	μAdc	4*	–	–	–	8	1,16
		9	–	750	–	–	470	–	470	μAdc	9	–	–	–	8	1,16
	I_{inL}	4*	0.5	–	0.5	–	–	0.3	–	μAdc	–	4*	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	–	–	–	–	8	1,16
		14	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	–	–	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	4,5,9	–	–	–	8	1,16
		14	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	9,10,11	–	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	2	-1.090	–	-0.980	–	–	-0.910	–	Vdc	–	–	–	9	8	1,16
		3	-1.090	–	-0.980	–	–	-0.910	–	↓	–	–	–	9	↓	↓
		14	-1.090	–	-0.980	–	–	-0.910	–	↓	–	–	–	9	↓	↓
		15	-1.090	–	-0.980	–	–	-0.910	–	↓	–	–	–	9	↓	↓
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	9	–	8	1,16
		3	–	-1.655	–	–	-1.630	–	-1.595	↓	–	–	9	–	↓	↓
		14	–	-1.655	–	–	-1.630	–	-1.595	↓	–	–	9	–	↓	↓
		15	–	-1.655	–	–	-1.630	–	-1.595	↓	–	–	9	–	↓	↓
Switching Times (50-ohm load)													Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{4+2-}	2	1.0	3.1	1.0	2.0	2.9	1.0	3.3	ns	–	–	4	2	8	1,16
	t_{4-2+}	2	1.0	3.1	1.0	↓	2.9	1.0	3.3	↓	–	–	↓	↓	↓	↓
Rise Time (20% to 80%)	t_{2+}	2	1.1	3.6	1.1	↓	3.3	1.1	3.7	↓	–	–	↓	↓	↓	↓
Fall Time (20% to 80%)	t_{2-}	2	1.1	3.6	1.1	↓	3.3	1.1	3.7	↓	–	–	↓	↓	↓	↓

*Individually test each input applying V_{IH} or V_{IL} to input under test.

MOTOROLA

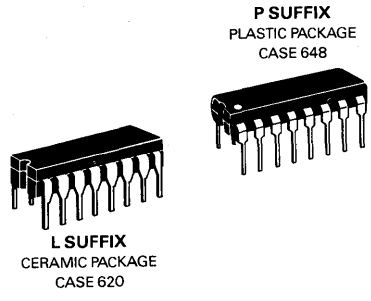
MC10101

MECL 10K SERIES

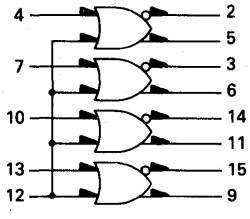
QUAD OR/NOR GATE

The MC10101 is a quad 2-input OR/NOR gate with one input from each gate common to pin 12.

P_D = 25 mW typ/gate (No Load)
t_{pd} = 2.0 ns typ
t_r, t_f = 2.0 ns typ (20%–80%)

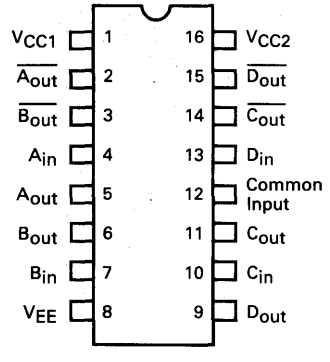


LOGIC DIAGRAM



V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

PIN ASSIGNMENT



ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

@ Test Temperature	TEST VOLTAGE VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}
−30°C	−0.890	−1.890	−1.205	−1.500	−5.2
+25°C	−0.810	−1.850	−1.105	−1.475	−5.2
+85°C	−0.700	−1.825	−1.035	−1.440	−5.2

Characteristic	Symbol	Pin Under Test	MC10101 Test Limits −30°C Min	−30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	29	–	20	26	–	29	mAdc	–	–	–	–	8	1,16
Input Current	I_{inH}	4	–	425	–	–	265	–	265	μAdc	4	–	–	–	8	1,16
		12	–	850	–	–	535	–	535	μAdc	12	–	–	–	8	1,16
	I_{inL}	4	0.5	–	0.5	–	–	0.3	–	μAdc	–	4	–	–	8	1,16
		12	0.5	–	0.5	–	–	0.3	–	μAdc	–	12	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	5	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	12	–	–	–	8	1,16
		5	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	↓	4	–	–	–	↓	↓
		2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	↓	–	–	–	–	↓	↓
		2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	↓	–	–	–	–	↓	↓
Logic "0" Output Voltage	V_{OL}	5	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	–	–	–	–	8	1,16
		5	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	↓	–	–	–	–	↓	↓
		2	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	↓	12	–	–	–	↓	↓
		2	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	↓	4	–	–	–	↓	↓
Logic "1" Threshold Voltage	V_{OHA}	5	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	12	–	8	1,16
		5	-1.080	–	-0.980	–	–	-0.910	–	↓	–	–	4	–	↓	↓
		2	-1.080	–	-0.980	–	–	-0.910	–	↓	–	–	–	12	↓	↓
		2	-1.080	–	-0.980	–	–	-0.910	–	↓	–	–	–	4	↓	↓
Logic "0" Threshold Voltage	V_{OLA}	5	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	–	12	8	1,16
		5	–	-1.655	–	–	-1.630	–	-1.595	↓	–	–	–	4	↓	↓
		2	–	-1.655	–	–	-1.630	–	-1.595	↓	–	–	12	–	↓	↓
		2	–	-1.655	–	–	-1.630	–	-1.595	↓	–	–	4	–	↓	↓
Switching Times (50-ohm load)													Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{4+2-}	2	1.0	3.1	1.0	2.0	2.9	1.0	3.3	ns	–	–	4	2	8	1,16
	t_{4-2+}	2	↓	↓	↓	↓	↓	↓	↓	↓	–	–	↓	2	↓	↓
	t_{4+5+}	5	↓	↓	↓	↓	↓	↓	↓	↓	–	–	↓	5	↓	↓
	t_{4-5-}	5	↓	↓	↓	↓	↓	↓	↓	↓	–	–	↓	5	↓	↓
Rise Time	t_{2+}	2	1.1	3.6	1.1	↓	3.3	1.1	3.7	↓	–	–	↓	2	↓	↓
(20 to 80%)	t_{5+}	5	↓	↓	↓	↓	↓	↓	↓	↓	–	–	↓	5	↓	↓
Fall Time	t_{2-}	2	↓	↓	↓	↓	↓	↓	↓	↓	–	–	↓	2	↓	↓
(20 to 80%)	t_{5-}	5	↓	↓	↓	↓	↓	↓	↓	↓	–	–	↓	5	↓	↓

MOTOROLA

MC10102

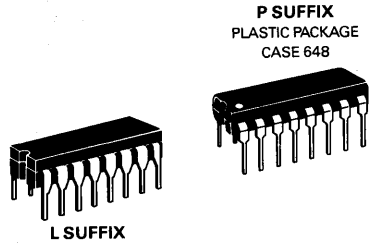
MECL 10K SERIES

QUAD 2-INPUT NOR GATE

The MC10102 is a quad 2-input NOR gate. The MC10102 provides one gate with OR/NOR outputs.

P_D = 25 mW typ/gate (No Load)
t_{pd} = 2.0 ns typ
t_r, t_f = 2.0 ns typ (20%–80%)

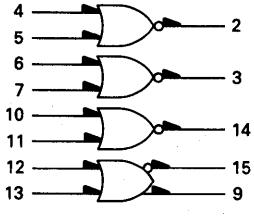
QUAD 2-INPUT NOR GATE



P SUFFIX
PLASTIC PACKAGE
CASE 648

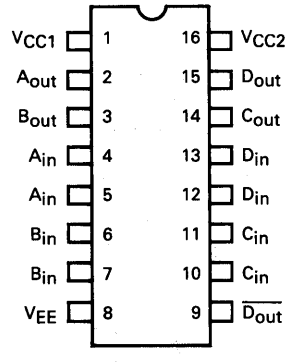
L SUFFIX
CERAMIC PACKAGE
CASE 620

LOGIC DIAGRAM



V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

PIN ASSIGNMENT



ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
−30°C	−0.890	−1.890	−1.205	−1.500	−5.2
+25°C	−0.810	−1.850	−1.105	−1.475	−5.2
+85°C	−0.700	−1.825	−1.035	−1.440	−5.2

Characteristic	Symbol	Pin Under Test	MC10102 Test Limits −30°C Min	−30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	29	–	20	26	–	29	mAdc	–	–	–	–	8	1,16
Input Current	I_{inH}	12	–	425	–	–	265	–	265	µAdc	12	–	–	–	8	1,16
	I_{inL}	12	0.5	–	0.5	–	–	0.3	–	µAdc	–	12	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	9	−1.060	−0.890	−0.960	–	−0.810	−0.890	−0.700	Vdc	12	–	–	–	8	1,16
		9	−1.060	−0.890	−0.960	–	−0.810	−0.890	−0.700		13	–	–	–		
		15	−1.060	−0.890	−0.960	–	−0.810	−0.890	−0.700		–	–	–	–		
		15	−1.060	−0.890	−0.960	–	−0.810	−0.890	−0.700		–	–	–	–		
Logic "0" Output Voltage	V_{OL}	9	−1.890	−1.675	−1.850	–	−1.650	−1.825	−1.615	Vdc	–	–	–	–	8	1,16
		9	−1.890	−1.675	−1.850	–	−1.650	−1.825	−1.615		–	–	–	–		
		15	−1.890	−1.675	−1.850	–	−1.650	−1.825	−1.615		12	–	–	–		
		15	−1.890	−1.675	−1.850	–	−1.650	−1.825	−1.615		13	–	–	–		
Logic "1" Threshold Voltage	V_{OHA}	9	−1.080	–	−0.980	–	–	−0.910	–	Vdc	–	–	12	–	8	1,16
		9	−1.080	–	−0.980	–	–	−0.910	–		–	–	13	–		
		15	−1.080	–	−0.980	–	–	−0.910	–		–	–	–	12		
		15	−1.080	–	−0.980	–	–	−0.910	–		–	–	–	13		
Logic "0" Threshold Voltage	V_{OLA}	9	–	−1.655	–	–	−1.630	–	−1.595	Vdc	–	–	–	12	8	1,16
		9	–	−1.655	–	–	−1.630	–	−1.595		–	–	–	13		
		15	–	−1.655	–	–	−1.630	–	−1.595		–	–	12	–		
		15	–	−1.655	–	–	−1.630	–	−1.595		–	–	13	–		
Switching Times (50-ohm load)													Pulse In	Pulse Out	−3.2 V	+2.0 V
Propagation Delay	t_{12+15-}	15	1.0	3.1	1.0	2.0	2.9	1.0	3.3	ns	–	–	12	15	8	1,16
	t_{12-15+}	15									–	–		15		
	t_{12+9+}	9									–	–		9		
	t_{12-9-}	9									–	–		9		
Rise Time	t_{15+}	15	1.1	3.6	1.1		3.3	1.1	3.7		–	–		15		
(20 to 80%)	t_{9+}	9									–	–		9		
Fall Time	t_{15-}	15									–	–		15		
(20 to 80%)	t_{9-}	9									–	–		9		

MOTOROLA

MC10103

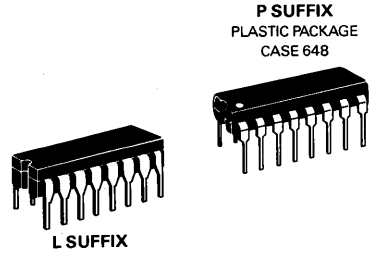
MECL 10K SERIES

QUAD 2-INPUT OR GATE

The MC10103 is a quad 2-input OR gate. The MC10103 provides one gate with OR/NOR outputs.

P_D = 25 mW typ/gate (No Load)
t_{pd} = 2.0 ns typ
t_r, t_f = 2.0 ns typ (20%–80%)

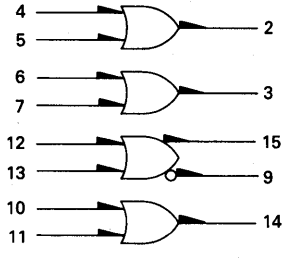
QUAD 2-INPUT OR GATE



P SUFFIX
PLASTIC PACKAGE
CASE 648

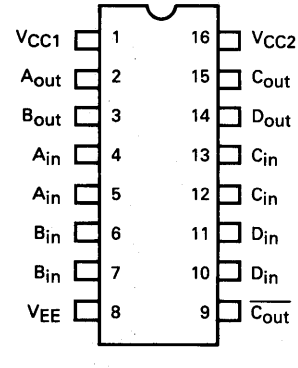
L SUFFIX
CERAMIC PACKAGE
CASE 620

LOGIC DIAGRAM



V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

PIN ASSIGNMENT



ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown for only one input and one output. The other inputs and outputs are tested in the same manner.

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10103 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	29	–	21	26	–	29	mAdc	–	–	–	–	8	1,16
Input Current	I_{inH}	4*	–	390	–	–	245	–	245	μAdc	4*	–	–	–	8	1,16
	I_{inL}	4*	0.5	–	0.5	–	–	0.3	–	μAdc	–	4*	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	4,5	–	–	–	8	1,16
		9	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	–	–	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	–	–	–	–	8	1,16
		9	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	12,13	–	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	2	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	4,5	–	8	1,16
		9	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	–	12,13	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	–	4,5	8	1,16
		9	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	12,13	–	8	1,16
Switching Times (50-ohm load)													Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{4+2+}	2	1.0	3.1	1.0	2.0	2.9	1.0	3.3	ns	–	–	4	2	8	1,16
	t_{12+9-}	9	1.0	3.1	1.0	↓	2.9	1.0	3.3	↓	–	–	12	9	↓	↓
Rise Time (20% to 80%)	t_{2+}	2	1.1	3.6	1.1		3.3	1.1	3.7		–	–	4	2		
Fall Time (20% to 80%)	t_{2-}	2	1.1	3.6	1.1		3.3	1.1	3.7		–	–	4	2		

*Individually test each input applying V_{IH} or V_{IL} to input under test.

MOTOROLA

MC10104

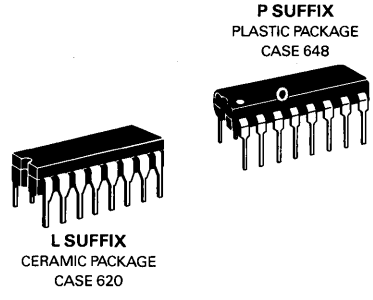
QUAD 2-INPUT AND GATE

The MC10104 is a quad 2-input AND gate. One of the gates has both AND/NAND outputs available.

P_D = 35 mW typ/gate (No Load)
t_{pd} = 2.7 ns typ
t_r, t_f = 2.0 ns typ (20%–80%)

MECL 10K SERIES

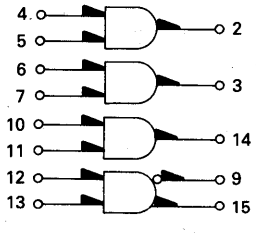
QUAD 2-INPUT AND GATE



P SUFFIX
PLASTIC PACKAGE
CASE 648

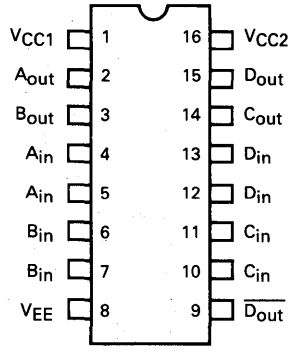
L SUFFIX
CERAMIC PACKAGE
CASE 620

LOGIC DIAGRAM



V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

PIN ASSIGNMENT



ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

@ Test Temperature	TEST VOLTAGE VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Test	MC10104 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BLEOW: $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	39	–	–	35	–	39	mAdc	–	–	–	–	8	1,16
Input Current	I_{inH}*	12	–	425	–	–	265	–	265	μAdc	12,13	–	–	–	8	1,16
		13	–	350	–	–	220	–	220	μAdc	13	–	–	–	8	1,16
	I_{inL}	12	0.5	–	0.5	–	–	0.3	–	μAdc	–	12	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	15	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	12,13	–	–	–	8	1,16
		9	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	–	–	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	15	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	–	–	–	–	8	1,16
		9	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	12,13	–	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	9	-1.090	–	-0.980	–	–	-0.910	–	Vdc	–	–	–	12	8	1,16
		9	-1.090	–	-0.980	–	–	-0.910	–	↓	–	–	–	13	↓	↓
		15	-1.090	–	-0.980	–	–	-0.910	–		12	–	13	–		
		15	-1.090	–	-0.980	–	–	-0.910	–		13	–	12	–		
Lgoic "0" Threshold Voltage	V_{OLA}	9	–	-1.655	–	–	-1.630	–	-1.595	Vdc	12	–	13	–	8	1,16
		9	–	-1.655	–	–	-1.630	–	-1.595	↓	13	–	12	–	↓	↓
		15	–	-1.655	–	–	-1.630	–	-1.595		–	–	–	12		
		15	–	-1.655	–	–	-1.630	–	-1.595		–	–	–	13		
Switching Times* (50-ohm load)											+1.11 V		Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{12+15+}	15	1.0	4.3	1.0	2.2	4.0	1.0	4.2	ns	13	–	12	15	8	1,16
	t_{12-15-}	15	↓	↓	↓	↓	↓	↓	↓	↓	↓	–	↓	15	↓	↓
	t_{12+9-}	9	↓	↓	↓	↓	↓	↓	↓		↓	–	↓	9		
	t_{12-9+}	9	↓	↓	↓	↓	↓	↓	↓		↓	–	↓	9		
	t_{13+15+}	15	↓	↓	↓	2.7	↓	↓	↓		12	–	13	15		
	t_{13+9-}	9	↓	↓	↓	2.7	↓	↓	↓		12	–	13	9		
Rise Time (20 to 80%)	t_{15+}	15	1.5	3.7	1.5	2.0	3.5	1.5	3.6		↓	–	↓	15		
	t_{9+}	9	↓	↓	↓	↓	↓	↓	↓			–		9		
Fall Time (20 to 80%)	t_{15-}	15	↓	↓	↓	↓	↓	↓	↓		↓	–	↓	15	↓	↓
	t_{9-}	9	↓	↓	↓	↓	↓	↓	↓	↓	↓	–	↓	9	↓	↓

*Inputs 4, 7, 10, and 13 will behave similarly for ac and I_{inH} values.

Inputs 5, 6, 11, and 12 will behave similarly for ac and I_{inH} values.

MOTOROLA

MC10105

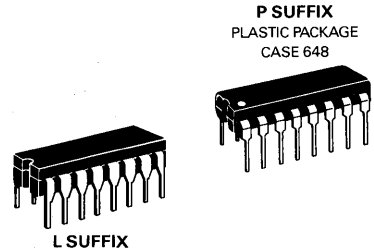
MECL 10K SERIES

TRIPLE 2-3-2-INPUT OR/NOR GATE

The MC10105 is a triple 2-3-2 input OR/NOR gate.

P_D = 30 mW typ/gate (No Load)
t_{pd} = 2.0 ns typ
t_r, t_f = 2.0 ns typ (20%–80%)

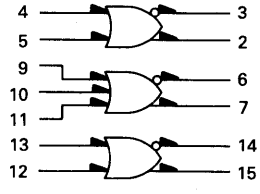
TRIPLE 2-3-2-INPUT OR/NOR GATE



P SUFFIX
PLASTIC PACKAGE
CASE 648

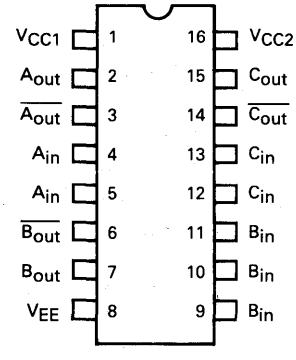
L SUFFIX
CERAMIC PACKAGE
CASE 620

LOGIC DIAGRAM



V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

PIN ASSIGNMENT



ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown for only one input and one output. The other inputs and outputs are tested in the same manner.

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
−30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10105 Test Limits −30°C Min	−30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	23	–	17	21	–	23	mAdc	–	–	–	–	8	1,16
Input Current	I_{inH}	4		425	–	–	265	–	265	μAdc	4	–	–	–	8	1,16
	I_{inL}	4	0.5	–	0.5	–	–	0.3	–	μAdc	–	4	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	3	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	–	–	–	–	8	1,16
		2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	4	–	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	3	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	4	–	–	–	8	1,16
		2	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	–	–	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	3	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	–	4	8	1,16
		2	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	4	–	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	3	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	4	–	8	1,16
		2	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	–	4	8	1,16
Switching Times (50-ohm load)													Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{4+3-}	3	1.0	3.1	1.0	2.0	2.9	1.0	3.3	ns	–	–	4	3	8	1,16
	t_{4-3+}	3	↓	↓	↓	↓	↓	↓	↓	↓	–	–	↓	3	↓	↓
	t_{4+2+}	2	↓	↓	↓	↓	↓	↓	↓	↓	–	–	↓	2	↓	↓
	t_{4-2-}	2	↓	↓	↓	↓	↓	↓	↓	↓	–	–	↓	2	↓	↓
Rise Time	t_{3+}	3	1.1	3.6	1.1	↓	3.3	1.1	3.7	↓	–	–	↓	3	↓	↓
(20 to 80%)	t_{2+}	2	↓	↓	↓	↓	↓	↓	↓	↓	–	–	↓	2	↓	↓
Fall Time	t_{3-}	3	↓	↓	↓	↓	↓	↓	↓	↓	–	–	↓	3	↓	↓
(20 to 80%)	t_{2-}	2	↓	↓	↓	↓	↓	↓	↓	↓	–	–	↓	2	↓	↓

MOTOROLA

MC10106

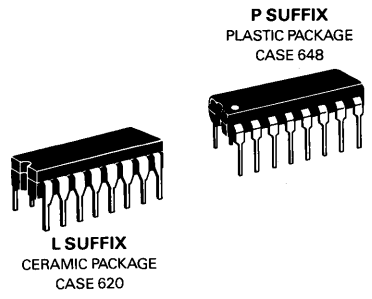
MECL 10K SERIES

TRIPLE 4-3-3-INPUT NOR GATE

The MC10106 is a triple 4-3-3 input NOR gate.

P_D = 30 mW typ/gate (No Load)
t_{pd} = 2.0 ns typ
t_r, t_f = 2.0 ns typ (20%–80%)

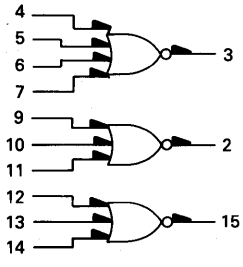
TRIPLE 4-3-3-INPUT NOR GATE



P SUFFIX
PLASTIC PACKAGE
CASE 648

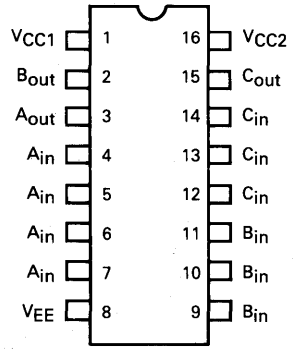
L SUFFIX
CERAMIC PACKAGE
CASE 620

LOGIC DIAGRAM



V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

PIN ASSIGNMENT



ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown for only one input and one output. The other inputs and outputs are tested in the same manner.

@ Test Temperature	TEST VOLTAGE VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10106 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	23	–	17	21	–	23	mAdc	–	–	–	–	8	1,16
Input Current	I_{inH}	4	–	425	–	–	265	–	265	μAdc	4	–	–	–	8	1,16
	I_{inL}	4	0.5	–	0.5	–	–	0.3	–	μAdc	–	4	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	3	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	–	–	–	–	8	1,16
		2	-1.060	-0.890	-0.960		-0.810	-0.890	-0.700		–	–	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	3	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	4	–	–	–	8	1,16
		2	-1.890	-1.675	-1.850		-1.650	-1.825	-1.615		9	–	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	3	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	–	4	8	1,16
		2	-1.080		-0.980			-0.910			–	–	–	9	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	3	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	4	–	8	1,16
		2		-1.655			-1.630		-1.595		–	–	9	–	8	1,16
Switching Times (50-ohm load)													Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{4+3-}	3	1.0	3.1	1.0	2.0	2.9	1.0	3.3	ns	–	–	4	3	8	1,16
	t_{4-3+}	↓	1.0	3.1	1.0	↓	2.9	1.0	3.3	↓	–	–	↓	↓	↓	↓
Rise Time (20 to 80%)	t_{3+}		1.1	3.6	1.1		3.3	1.1	3.7		–	–				
Fall Time (20 to 80%)	t_{3-}	↓	1.1	3.6	1.1	↓	3.3	1.1	3.7	↓	–	–	↓	↓	↓	↓

MOTOROLA

MC10107

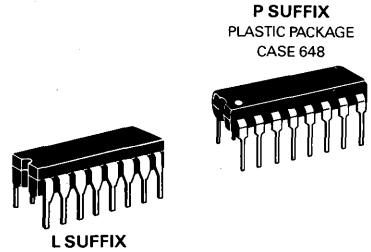
MECL 10K SERIES

TRIPLE 2-INPUT EXCLUSIVE "OR"/EXCLUSIVE "NOR"

The MC10107 is a triple-2 input exclusive OR/NOR gate.

P_D = 40 mW typ/gate (No Load)
t_{pd} = 2.8 ns typ
t_r, t_f = 2.5 ns typ (20%–80%)

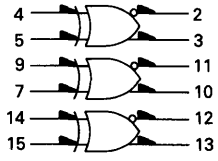
TRIPLE 2-INPUT EXCLUSIVE "OR"/EXCLUSIVE "NOR"



P SUFFIX
PLASTIC PACKAGE
CASE 648

L SUFFIX
CERAMIC PACKAGE
CASE 620

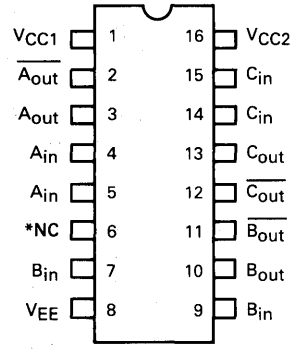
LOGIC DIAGRAM



$3 = (4 \cdot \bar{5}) + (\bar{4} \cdot 5)$
$2 = (\bar{4} \cdot \bar{5}) + (4 \cdot 5)$

V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

PIN ASSIGNMENT



*NC = No Connection

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10107 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	31	–	28	–	31	mAdc	5,7,15	–	–	–	8	1,16
Input Current	$I_{in\ H}$	4,9,14	–	425	–	265	–	265	μAdc	*	–	–	–	8	1,16
		5,7,15	–	350	–	220	–	220	μAdc	*	–	–	–	8	1,16
	$I_{in\ L}$	*	0.5	–	0.5	–	0.3	–	μAdc	–	*	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	2	-1.060	-0.890	-0.960	-0.810	-0.890	-0.700	Vdc	4,5	–	–	–	8	1,16
		2	-1.060	-0.890	-0.960	-0.810	-0.890	-0.700		–	–	–	–		
		3	-1.060	-0.890	-0.960	-0.810	-0.890	-0.700		4	–	–	–		
		3	-1.060	-0.890	-0.960	-0.810	-0.890	-0.700		5	–	–	–		
Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.675	-1.850	-1.650	-1.825	-1.615	Vdc	4	–	–	–	8	1,16
		2	-1.890	-1.675	-1.850	-1.650	-1.825	-1.615		5	–	–	–		
		3	-1.890	-1.675	-1.850	-1.650	-1.825	-1.615		4,5	–	–	–		
		3	-1.890	-1.675	-1.850	-1.650	-1.825	-1.615		–	–	–	–		
Logic "1" Threshold Voltage	V_{OHA}	2	-1.080	–	-0.980	–	-0.910	–	Vdc	5	–	4	–	8	1,16
		2	-1.080	–	-0.980	–	-0.910	–		–	–	–	4		
		3	-1.080	–	-0.980	–	-0.910	–		–	–	4	–		
		3	-1.080	–	-0.980	–	-0.910	–		–	–	5	–		
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.655	–	-1.630	–	-1.595	Vdc	–	–	4	–	8	1,16
		2	–	-1.655	–	-1.630	–	-1.595		–	–	5	–		
		3	–	-1.655	–	-1.630	–	-1.595		5	–	4	–		
		3	–	-1.655	–	-1.630	–	-1.595		–	–	–	4		
Switching Times (50 Ω Load)					Min	Typ	Max		Unit	+1.1 V		Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t++	Inputs	1.1	3.8	1.1	2.0	3.7	1.1	4.0	ns	5,7,15	–	Input	Corresponding	8	1,16
	t+−	4, 9 or 14										–	4, 9, or	Ex-OR/Ex-NOR		
	t−+	to either										–	14	Outputs		
	t−−	Output										–				
	t++	Inputs				2.8					4,9,14	–	Input	Corresponding		
	t+−	5,7, or 15										–	5, 7, or	Ex-OR/Ex-NOR		
	t−+	to either										–	15	Outputs		
	t−−	Output										–				
Rise Time (20 to 80%)	t+	**	1.1	3.5		2.5	3.5		3.8		4,9,14	–	Any Input	Corresponding Ex-OR/Ex NOR Outputs		
Fall Time (20 to 80%)	t−	**	1.1	3.5		2.5	3.5		3.8		4,9,14	–	Any Input			

*Individually test each input applying V_{IH} or V_{IL} to input under test.
**Any Output

MOTOROLA

MC10109

MECL 10K SERIES

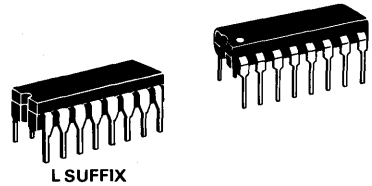
DUAL 4-5-INPUT "OR/NOR" GATE

The MC10109 is a dual 4-5 input OR/NOR gate.

P_D = 30 mW typ/gate (No Load)
t_{pd} = 2.0 ns typ
t_r, t_f = 2.0 ns typ (20%–80%)

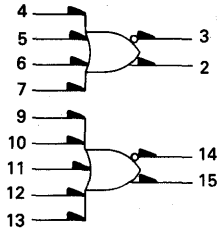
DUAL 4-5-INPUT "OR/NOR" GATE

P SUFFIX
PLASTIC PACKAGE
CASE 648



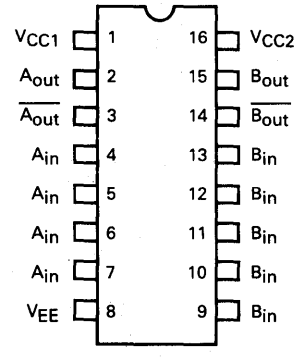
L SUFFIX
CERAMIC PACKAGE
CASE 620

LOGIC DIAGRAM



V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

PIN ASSIGNMENT



ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown for only one input and one output. The other inputs and outputs are tested in the same manner.

@ Test Temperature	TEST VOLTAGE VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}
−30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10109 Test Limits −30°C Min	−30°C Max	+25°C Min	+25°C Typ	+85°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS BELOW: $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	15	–	11	14	–	15	mAdc	–	–	–	–	8	1,16
Input Current	I_{inH}	4	–	425	–	–	265	–	265	μAdc	4	–	–	–	8	1,16
	I_{inL}	4	0.5	–	0.5	–	–	0.3	–	μAdc	–	4	–	–	8	1,16
High Output Voltage	V_{OH}	2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	4	–	–	–	8	1,16
		3	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	–	–	–	–	8	1,16
Low Output Voltage	V_{OL}	2	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	–	–	–	–	8	1,16
		3	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	4	–	–	–	8	1,16
High Threshold Voltage	V_{OHA}	2	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	4	–	8	1,16
		3	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	–	4	8	1,16
Low Threshold Voltage	V_{OLA}	2	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	–	4	8	1,16
		3	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	4	–	8	1,16
Switching Times (50-ohm load)													Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{4+2+}	2	1.0	3.1	1.0	2.0	2.9	1.0	3.3	ns	–	–	4	2	8	1,16
	t_{4-2-}	2	↓	↓	↓	↓	↓	↓	↓	↓	–	–	↓	2	↓	↓
	t_{4+3-}	3									–	–		3		
	t_{4-3+}	3									–	–		3		
Rise Time (20 to 80%)	t_{2+}	2	1.1	3.6	1.1		3.3	1.1	3.7		–	–		2		
	t_{3+}	3	↓	↓	↓		↓	↓	↓		–	–		3		
Fall Time (20 to 80%)	t_{2-}	2									–	–	↓	2	↓	↓
	t_{3-}	3									–	–		3		

MOTOROLA

MC10110

MECL 10K SERIES

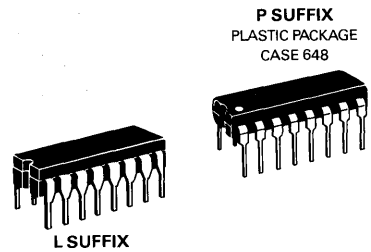
DUAL 3-INPUT 3-OUTPUT "OR" GATE

The MC10110 is designed to drive up to three transmission lines simultaneously. The multiple outputs of this device also allow the wire "OR" ing of several levels of gating for minimization of gate and package count.

The ability to control three parallel lines from a single point makes the MC10110 particularly useful in clock distribution applications where minimum clock skew is desired. Three V_{CC} pins are provided and each one should be used.

P_D = 80 mW typ/gate (No Load)
t_{pd} = 2.4 ns typ (All Outputs Loaded)
t_r, t_f = 2.2 ns typ (20%–80%)

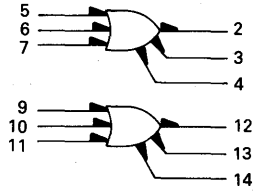
DUAL 3-INPUT 3-OUTPUT "OR" GATE



P SUFFIX
PLASTIC PACKAGE
CASE 648

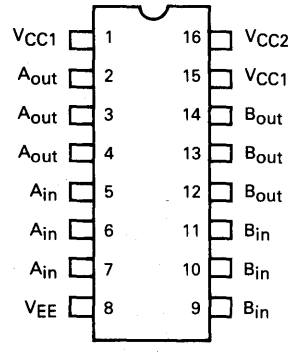
L SUFFIX
CERAMIC PACKAGE
CASE 620

LOGIC DIAGRAM



V_{CC1} = Pin 1, 15
V_{CC2} = Pin 16
V_{EE} = Pin 8

PIN ASSIGNMENT



ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown for only one input and one output. The other inputs and outputs are tested in the same manner.

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
−30°C	−0.890	−1.890	−1.205	−1.500	−5.2
+25°C	−0.810	−1.850	−1.105	−1.475	−5.2
+85°C	−0.700	−1.825	−1.035	−1.440	−5.2

Characteristic	Symbol	Pin Under Test	MC10110 Test Limits −30°C Min	−30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	42	–	30	38	–	42	mAdc	–	–	–	–	8	1,15,16
Input Current	I_{inH}	5,6,7	–	680	–	–	425	–	425	μAdc	*	–	–	–	8	1,15,16
	I_{inL}	5,6,7	0.5	–	0.5	–	–	0.3	–	μAdc	–	*	–	–	8	1,15,16
Logic "1" Output Voltage	V_{OH}	2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	5	–	–	–	8	1,15,16
		3	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	6	–	–	–	8	1,15,16
		4	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	7	–	–	–	8	1,15,16
Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	–	–	–	–	8	1,15,16
		3	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	–	–	–	–	8	1,15,16
		4	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	–	–	–	–	8	1,15,16
Logic "1" Threshold Voltage	V_{OHA}	2	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	5	–	8	1,15,16
		3	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	6	–	8	1,15,16
		4	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	7	–	8	1,15,16
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	–	5	8	1,15,16
		3	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	–	6	8	1,15,16
		4	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	–	7	8	1,15,16
Switching Times (50-ohm load)													Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{5+2+}	2	1.4	3.5	1.4	2.4	3.5	1.5	3.8	ns	–	–	5	2	8	1,15,16
	t_{5-2-}	2	↓	↓	↓	↓	↓	↓	↓	↓	–	–	↓	2	↓	↓
	t_{5+3+}	3									–	–		3		
	t_{5-3-}	3									–	–		3		
	t_{5+4+}	4									–	–		4		
	t_{5-4-}	4	↓		↓	↓		↓			–	–		4		
Rise Time (20 to 80%)	t_{2+}	2	1.0		1.1	2.2		1.2			–	–		2		
	t_{3+}	3	↓		↓	↓		↓			–	–		3		
	t_{4+}	4									–	–		4		
Fall Time (20 to 80%)	t_{2-}	2									–	–		2		
	t_{3-}	3									–	–		3		
	t_{4-}	4	↓	↓	↓	↓	↓	↓	↓	↓	–	–	↓	4	↓	↓

*Individually test each input using the pin connections shown.

MOTOROLA

MC10111

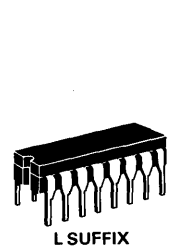
MECL 10K SERIES

DUAL 3-INPUT 3-OUTPUT "NOR" GATE

The MC10111 is designed to drive up to three transmission lines simultaneously. The multiple outputs of this device also allow the wire "OR"-ing of several levels of gating for minimization of gate and package count.

The ability to control three parallel lines from a single point makes the MC10111 particularly useful in clock distribution applications where minimum clock skew is desired. Three V_{CC} pins are provided and each one should be used.

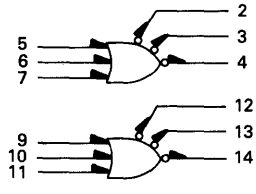
P_D = 80 mW typ/gate (No Load)
t_{pd} = 2.4 ns typ (All Outputs Loaded)
t_r, t_f = 2.2 ns typ (20%–80%)



P SUFFIX
PLASTIC PACKAGE
CASE 648

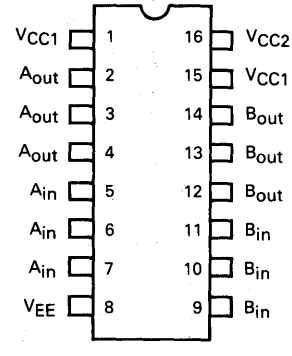
L SUFFIX
CERAMIC PACKAGE
CASE 620

LOGIC DIAGRAM



V_{CC1} = Pin 1, 15
V_{CC2} = Pin 16
V_{EE} = Pin 8

PIN ASSIGNMENT



ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown for only one input and one output. The other inputs and outputs are tested in the same manner.

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10111 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	42	–	–	38	–	42	mAdc	–	–	–	–	8	1,15,16
Input Current	I_{inH}	5,6,7	–	680	–	–	425	–	425	μAdc	*	–	–	–	8	1,15,16
	I_{inL}	5,6,7	0.5	–	0.5	–	–	0.3	–	μAdc	–	*	–	–	8	1,15,16
Logic "1" Output Voltage	V_{OH}	2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	–	–	–	–	8	1,15,16
		3	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	–	–	–	–	8	1,15,16
		4	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	–	–	–	–	8	1,15,16
Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	5	–	–	–	8	1,15,16
		3	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	6	–	–	–	8	1,15,16
		4	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	7	–	–	–	8	1,15,16
Logic "1" Threshold Voltage	V_{OHA}	2	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	–	5	8	1,15,16
		3	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	–	6	8	1,15,16
		4	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	–	7	8	1,15,16
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	5	–	8	1,15,16
		3	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	6	–	8	1,15,16
		4	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	7	–	8	1,15,16
Switching Times (50-ohm load)													Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{5+2-}	2	1.4	3.5	1.4	2.4	3.5	1.5	3.8	ns	–	–	5	2	8	1,15,16
	t_{5-2+}	2									–	–		2		
	t_{5+3-}	3									–	–		3		
	t_{5-3+}	3									–	–		3		
	t_{5+4-}	4									–	–		4		
	t_{5-4+}	4									–	–		4		
Rise Time (20 to 80%)	t_{2+}	2	1.0		1.1	2.2	3.5	1.2	3.8		–	–		2		
	t_{3+}	3									–	–		3		
	t_{4+}	4									–	–		4		
Fall Time (20 to 80%)	t_{2-}	2									–	–		2		
	t_{3-}	3									–	–		3		
	t_{4-}	4									–	–		4		

*Individually test each input using the pin connections shown.

MOTOROLA

MC10113

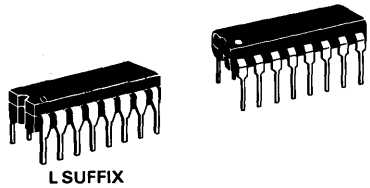
MECL 10K SERIES

QUAD EXCLUSIVE OR GATE

The MC10113 is a quad Exclusive OR gate, with an enable common to all four gates. The outputs may be wire-ORed together to perform a 4-bit comparison function (A = B). The enable is active low.

P_D = 175 mW typ/pkg (No Load)
t_{pd} = 2.5 ns typ
t_r, t_f = 2.0 ns typ (20% to 80%)

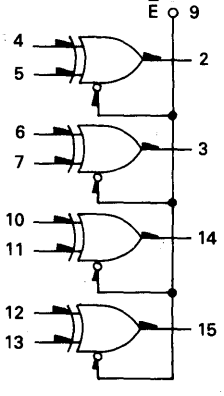
QUAD EXCLUSIVE OR GATE



P SUFFIX
PLASTIC PACKAGE
CASE 648

L SUFFIX
CERAMIC PACKAGE
CASE 620

LOGIC DIAGRAM



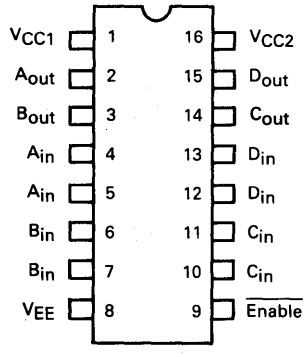
TRUTH TABLE

IN		E	OUTPUT
L	L	L	L
L	H	L	H
H	L	L	H
H	H	L	L
ϕ	ϕ	H	L

ϕ = Don't Care

V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

PIN ASSIGNMENT



ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown only for selected inputs and outputs. Other inputs and outputs are tested in a similar manner.

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10113 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	46	–	42	–	46	mAdc	–	–	–	–	8	1,16
Input Current	$I_{in\ H}$	4,7,10,13	–	425	–	265	–	265	μAdc	*	–	–	–	8	1,16
		5,6,11,12	–	350	–	220	–	220	μAdc	*	–	–	–	8	1,16
		9	–	870	–	545	–	545	μAdc	9	–	–	–	8	1,16
	$I_{in\ L}$	*	0.5	–	0.5	–	0.3	–	μAdc	–	*	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	2	-1.060	-0.890	-0.960	-0.810	-0.890	-0.700	Vdc	4	–	–	–	8	1,16
		3	-1.060	-0.890	-0.960	-0.810	-0.890	-0.700		7	–	–	–		
		14	-1.060	-0.890	-0.960	-0.810	-0.890	-0.700		11	–	–	–		
		15	-1.060	-0.890	-0.960	-0.810	-0.890	-0.700		13	–	–	–		
Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.675	-1.850	-1.650	-1.825	-1.615	Vdc	–	4	–	–	8	1,16
		3	-1.890	-1.675	-1.850	-1.650	-1.825	-1.615		–	7	–	–		
		14	-1.890	-1.675	-1.850	-1.650	-1.825	-1.615		–	11	–	–		
		15	-1.890	-1.675	-1.850	-1.650	-1.825	-1.615		–	13	–	–		
Logic "1" Threshold Voltage	V_{OHA}	2	-1.080	–	-0.980	–	-0.910	–	Vdc	–	–	4	–	8	1,16
		3	-1.080	–	-0.980	–	-0.910	–		–	–	6	–		
		14	-1.080	–	-0.980	–	-0.910	–		–	–	10	–		
		15	-1.080	–	-0.980	–	-0.910	–		–	–	12	–		
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.655	–	-1.630	–	-1.595	Vdc	–	–	–	5	8	1,16
		3	–	-1.655	–	-1.630	–	-1.595		–	–	–	7		
		14	–	-1.655	–	-1.630	–	-1.595		–	–	–	11		
		15	–	-1.655	–	-1.630	–	-1.595		–	–	–	13		
Switching Times (50 Ω Load)					Min	Typ	Max		Unit	+1.11 V		Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{4+2+}	2	1.1	4.7	1.3	2.6	4.5	1.3	5.0	ns	–	–	4	2	8	1,16
	t_{4-2-}	2	1.1	4.7	1.3	2.6	4.5	1.3	5.0		–	–	4			
	t_{9+2-}	2	1.3	5.2	1.5	3.4	5.0	1.5	5.5		4	–	9			
	t_{9-2+}	2	1.3	5.2	1.5	3.4	5.0	1.5	5.5		4	–	9			
Rise Time (20 to 80%)	t_{2+}	2	1.1	4.2	1.1	2.5	3.9	1.1	4.4		–	–	4			
Fall Time (20 to 80%)	t_{2-}	2	1.1	4.2	1.1	2.5	3.9	1.1	4.4		–	–	4			

*Individually test each input applying V_{IH} or V_{IL} to input under test.

MC10114

MECL 10K SERIES

TRIPLE LINE RECEIVER

TRIPLE LINE RECEIVER

The MC10114 is a triple line receiver designed for use in sensing differential signals over long lines. An active current source and translated emitter follower inputs provide the line receiver with a common mode noise rejection limit of one volt in either the positive or the negative direction. This allows a large amount of common mode noise immunity for extra long lines.

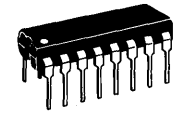
Another feature of the MC10114 is that the OR outputs go to a logic low level whenever the inputs are left floating. The outputs are each capable of driving 50 ohm transmission lines.

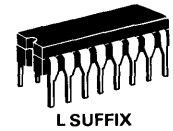
This device is useful in high speed central processors, minicomputers, peripheral controllers, digital communication systems, testing and instrumentation systems. The MC10114 can also be used for MOS to MECL interfacing and it is ideal as a sense amplifier for MOS RAM's.

A V_{BB} reference is provided which is useful in making the MC10114 a Schmitt trigger, allowing single-ended driving of the inputs, or other applications where a stable reference voltage is necessary.

P_D = 145 mW typ/pkg
t_{pd} = 2.4 ns typ (Single Ended Input)
t_{pd} = 2.0 ns typ (Differential Input)
t_r, t_f = 2.1 ns typ (20% to 80%)

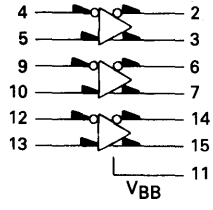
P SUFFIX
PLASTIC PACKAGE
CASE 648





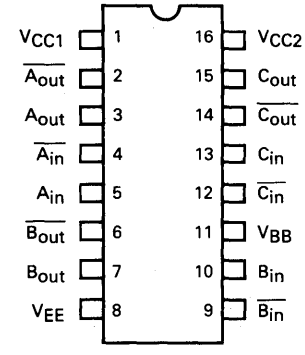
L SUFFIX
CERAMIC PACKAGE
CASE 620

LOGIC DIAGRAM



V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

PIN ASSIGNMENT



ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

@ Test Temperature	TEST VOLTAGE VALUES (Volts)									
	V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{BB}	V_{IHH}*	V_{ILH}*	V_{IHL}*	V_{ILL}*	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	From	+0.110	-0.890	-1.890	-2.890	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	Pin	+0.190	-0.850	-1.810	-2.850	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	11	+0.300	-0.825	-1.700	-2.825	-5.2

Characteristic	Symbol	Pin Under Test	MC10114 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{BB}	V_{IHH}*	V_{ILH}*	V_{IHL}*	V_{ILL}*	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	39	–	28	35	–	39	mAdc	–	4,9,12	–	–	5,10,13	–	–	–	–	8	1,16
Input Current	I_{inH}	4	–	70	–	–	45	–	45	μAdc	4	9,12	–	–	5,10,13	–	–	–	–	8	1,16
	I_{CBO}	4	–	1.5	–	–	1.0	–	1.0	μAdc	–	9,12	–	–	5,10,13	–	–	–	–	8,4	1,16
Logic "1" Output Voltage	V_{OH}	2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	4	9,12	–	–	5,10,13	–	–	–	–	8	1,16
		3	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	9,12	4	–	–	5,10,13	–	–	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	9,12	4	–	–	5,10,13	–	–	–	–	8	1,16
		3	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	4	9,12	–	–	5,10,13	–	–	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	2	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	9,12	4	–	5,10,13	–	–	–	–	8	1,16
		3	-1.080	–	-0.980	–	–	-0.910	–	Vdc	9,12	–	–	4	5,10,13	–	–	–	–	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.655	–	–	-1.630	–	-1.595	Vdc	9,12	–	–	4	5,10,13	–	–	–	–	8	1,16
		3	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	9,12	4	–	5,10,13	–	–	–	–	8	1,16
Reference Voltage	V_{BB}	11	-1.420	-1.280	-1.350	–	-1.230	-1.295	-1.150	Vdc	–	–	–	–	5,10,13	–	–	–	–	8	1,16
Common Mode Rejection Test	V_{OH}	2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	–	–	–	–	–	4	5	–	–	8	1,16
		3	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	–	–	–	–	–	–	–	5	4	8	1,16
	V_{OL}	2	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	–	–	–	–	–	–	–	5	4	8	1,16
		3	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	–	–	–	–	–	4	5	–	–	8	1,16
Switching Times (50-ohm Load)			Min	Max	Min	Typ	Max	Min	Max				Pulse In	Pulse Out						-3.2 V	+2.0 V
Propagation Delay**	t_{4+2+}	2	1.0	4.4	1.0	2.4	4.0	0.9	4.3	ns	–	–	4	2	5,10,13	–	–	–	–	8	1,16
	t_{4-2-}	2	↓	↓	↓	↓	↓	↓	↓		–	–	↓	2	↓	–	–	–	–	↓	↓
	t_{4+3-}	3	↓	↓	↓	↓	↓	↓	↓		–	–	↓	3	↓	–	–	–	–	↓	↓
	t_{4-3+}	3	↓	↓	↓	↓	↓	↓	↓		–	–	↓	3	↓	–	–	–	–	↓	↓
Rise Time (20% to 80%)	t_{2+}	2	1.5	3.8	1.5	2.1	3.5	1.5	3.7		–	–	↓	2	↓	–	–	–	–	↓	↓
	t_{3+}	3	↓	↓	↓	↓	↓	↓	↓		–	–	↓	3	↓	–	–	–	–	↓	↓
Fall Time (20% to 80%)	t_{2-}	2	↓	↓	↓	↓	↓	↓	↓		–	–	↓	2	↓	–	–	–	–	↓	↓
	t_{3-}	3	↓	↓	↓	↓	↓	↓	↓	↓	–	–	↓	3	↓	–	–	–	–	↓	↓

*V_{IHH} - Input logic "1" level shifted positive one volt for common mode rejection tests
V_{ILH} - Input logic "0" level shifted positive one volt for common mode rejection tests
V_{IHL} - Input logic "1" level shifted negative one volt for common mode rejection tests
V_{ILL} - Input logic "0" level shifted negative one volt for common mode rejection tests
**Delay is 2.0 ns with differential input

MOTOROLA

MC10115

MECL 10K SERIES

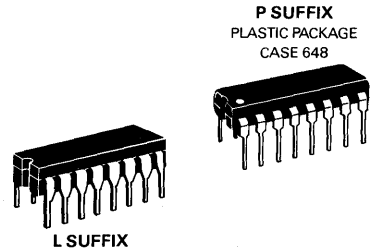
QUAD LINE RECEIVER

QUAD LINE RECEIVER

The MC10115 is a quad differential amplifier designed for use in sensing differential signals over long lines. The base bias supply (V_{BB}) is made available at pin 9 to make the device useful as a Schmitt trigger, or in other applications where a stable reference voltage is necessary.

Active current sources provide the MC10115 with excellent common mode noise rejection. If any amplifier in a package is not used, one input of that amplifier must be connected to V_{BB} (pin 9) to prevent upsetting the current source bias network.

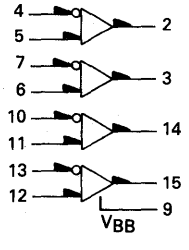
P_D = 110 mW typ/pkg (No Load)
t_{pd} = 2.0 ns typ
t_r, t_f = 2.0 ns typ (20%–80%)



P SUFFIX
PLASTIC PACKAGE
CASE 648

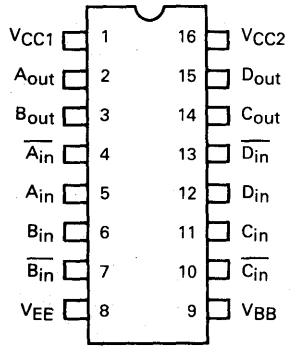
L SUFFIX
CERAMIC PACKAGE
CASE 620

LOGIC DIAGRAM



V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

PIN ASSIGNMENT



ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

@ Test Temperature	TEST VOLTAGE VALUES					
	V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{BB}	V_{EE}
−30°C	−0.890	−1.890	−1.205	−1.500	From Pin 9	-5.2
+25°C	−0.810	−1.850	−1.105	−1.475		-5.2
+85°C	−0.700	−1.825	−1.035	−1.440		-5.2

Characteristic	Symbol	Pin Under Test	MC10115 Test Limits −30°C Min	−30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{BB}	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	29	–	26	–	29	mAdc	–	4,7,10,13	–	–	5,6,11,12	8	1,16
Input Current	$I_{in\ H}$	4	–	150	–	95	–	95	μAdc	4	7,10,13	–	–	5,6,11,12	8	1,16
	I_{CBO}	4	–	1.5	–	1.0	–	1.0	μAdc	–	7,10,13	–	–	5,6,11,12	8,4	1,16
Logic "1" Output Voltage	V_{OH}	2	-1.060	-0.890	-0.960	-0.810	-0.890	-0.700	Vdc	7,10,13	4	–	–	5,6,11,12	8	1,16
Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.675	-1.850	-1.650	-1.825	-1.615	Vdc	4	7,10,13	–	–	5,6,11,12	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	2	-1.080	–	-0.980	–	-0.910	–	Vdc	–	7,10,13	–	4	5,6,11,12	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.655	–	-1.630	–	-1.595	Vdc	–	7,10,13	4	–	5,6,11,12	8	1,16
Reference Voltage	V_{BB}	9	1.420	1.280	-1.350	-1.230	1.295	-1.150	Vdc	–	–	–	–	5,6,11,12	8	1,16
Switching Times (50 Ω Load)										Pulse In		Pulse Out			-3.2 V	+2.0 V
Propagation Delay	t_{4-2+}	2	1.0	3.1	1.0	2.9	1.0	3.3	ns	4		2		5,6,11,12	8	1,16
	t_{4+2-}	2	1.0	3.1	1.0	2.9	1.0	3.3								
Rise Time (20% to 80%)	t_{2+}	2	1.1	3.6	1.1	3.3	1.1	3.7								
Fall Time (20% to 80%)	t_{2-}	2	1.1	3.6	1.1	3.3	1.1	3.7								

MC10116

MECL 10K SERIES

TRIPLE LINE RECEIVER

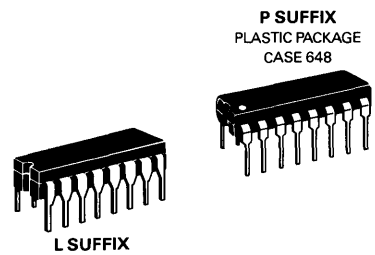
TRIPLE LINE RECEIVER

The MC10116 is a triple differential amplifier designed for use in sensing differential signals over long lines. The base bias supply (V_{BB}) is made available at pin 11 to make the device useful as a Schmitt trigger, or in other applications where a stable reference voltage is necessary.

Active current sources provide the MC10116 with excellent common mode noise rejection. If any amplifier in a package is not used, one input of that amplifier must be connected to V_{BB} (pin 11) to prevent upsetting the current source bias network.

Complementary outputs are provided to allow driving twisted pair lines, to enable cascading of several amplifiers in a chain, or simply to provide complement outputs of the input logic function.

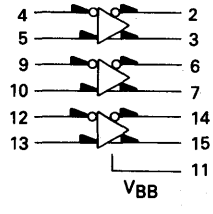
P_D = 85 mW typ/pkg (No Load)
t_{pd} = 2.0 ns typ
t_r, t_f = 2.0 ns typ (20%–80%)



P SUFFIX
PLASTIC PACKAGE
CASE 648

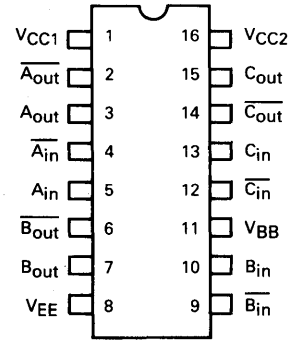
L SUFFIX
CERAMIC PACKAGE
CASE 620

LOGIC DIAGRAM



V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

PIN ASSIGNMENT



ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

@ Test Temperature	TEST VOLTAGE VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{BB}	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	From	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	Pin	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	11	-5.2

Characteristic	Symbol	Pin Under Test	MC10116 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS BELOW: $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{BB}	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	23	–	17	21	–	23	mAdc	–	4,9,12	–	–	5,10,13	8	1,16
Input Current	I_{inH}	4	–	150	–	–	95	–	95	μAdc	4	9,12	–	–	5,10,13	8	1,16
	I_{CBO}	4	–	1.5	–	–	1.0	–	1.0	μAdc	–	9,12	–	–	5,10,13	8,4	1,16
High Output Voltage	V_{OH}	2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	4	9,12	–	–	5,10,13	8	1,16
		3	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	9,12	4	–	–	5,10,13	8	1,16
Low Output Voltage	V_{OL}	2	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	9,12	4	–	–	5,10,13	8	1,16
		3	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	4	9,12	–	–	5,10,13	8	1,16
High Threshold Voltage	V_{OHA}	2	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	9,12	4	–	5,10,13	8	1,16
		3	-1.080	–	-0.980	–	–	-0.910	–	Vdc	9,12	–	–	4	5,10,13	8	1,16
Low Threshold Voltage	V_{OLA}	2	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	9,12	–	4	5,10,13	8	1,16
		3	–	-1.655	–	–	-1.630	–	-1.595	Vdc	9,12	–	4	–	5,10,13	8	1,16
Reference Voltage	V_{BB}	11	-1.420	-1.280	-1.350	–	-1.230	-1.295	-1.150	Vdc	–	–	–	–	5,10,13	8	1,16
Switching Times (50 Ω Load)			Min	Max	Min	Typ	Max	Min	Max				Pulse In	Pulse Out		-3.2 V	+2.0 V
Propagation Delay	t_{4+2+}	2	1.0	3.1	1.0	2.0	2.9	1.0	3.3	ns	–	–	4	2	5,10,13	8	1,16
	t_{4-2-}	2	↓	↓	↓	↓	↓	↓	↓	↓	–	–	↓	2	↓	↓	↓
	t_{4+3-}	3	↓	↓	↓	↓	↓	↓	↓	↓	–	–	↓	3	↓	↓	↓
	t_{4-3+}	3	↓	↓	↓	↓	↓	↓	↓	↓	–	–	↓	3	↓	↓	↓
Rise Time (20% to 80%)	t_{2+}	2	1.1	3.6	1.25	↓	3.3	1.1	3.7	↓	–	–	↓	2	↓	↓	↓
	t_{3+}	3	↓	↓	↓	↓	↓	↓	↓	↓	–	–	↓	3	↓	↓	↓
Fall Time (20% to 80%)	t_{2-}	2	↓	↓	↓	↓	↓	↓	↓	↓	–	–	↓	2	↓	↓	↓
	t_{3-}	3	↓	↓	↓	↓	↓	↓	↓	↓	–	–	↓	3	↓	↓	↓

MC10117

3

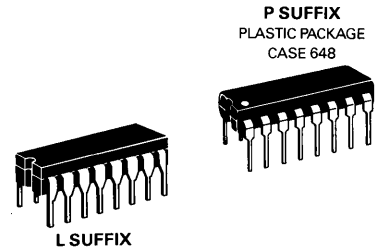
DUAL 2-WIDE 2-3-INPUT "OR-AND/OR-AND-INVERT" GATE

The MC10117 is a general purpose logic element designed for use in data control, such as digital multiplexing or data distribution. Pin 9 is common to both gates.

P_D = 100 mW typ/pkg (No Load)
t_{pd} = 2.3 ns typ
t_r, t_f = 2.2 ns typ (20%–80%)

MECL 10K SERIES

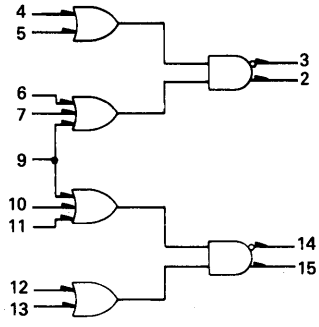
DUAL 2-WIDE 2-3-INPUT "OR-AND/OR-AND-INVERT" GATE



P SUFFIX
PLASTIC PACKAGE
CASE 648

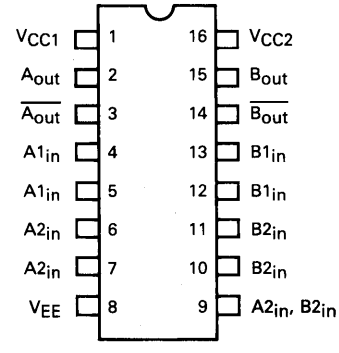
L SUFFIX
CERAMIC PACKAGE
CASE 620

LOGIC DIAGRAM



V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

PIN ASSIGNMENT



ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10117 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	29	–	20	26	–	29	mAdc	–	–	–	–	8	1,16
Input Current	$I_{in\ H}$*	6	–	425	–	–	265	–	265	μAdc	4	–	–	–	8	1,16
		9	–	560	–	–	350	–	350	μAdc	9	–	–	–	8	1,16
		4	–	390	–	–	245	–	245	μAdc	–	4	–	–	8	1,16
	$I_{in\ L}$	4	0.5	–	0.5	–	–	0.3	–	μAdc	–	9	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	2	-1.060	-0.780	-0.960	–	-0.700	-0.890	-0.590	Vdc	4,9	–	–	–	8	1,16
		3	-1.060	-0.780	-0.960	–	-0.700	-0.890	-0.590	Vdc	–	–	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	2	1.890	-1.675	1.850	–	-1.650	-1.825	-1.615	Vdc	–	–	–	–	8	1,16
		3	1.890	-1.675	1.850	–	-1.650	-1.825	-1.615	Vdc	4,9	–	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	2	-1.080	–	-0.980	–	–	-0.910	–	Vdc	9	–	4	–	8	1,16
		3	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	–	4	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	–	4	8	1,16
		3	–	-1.655	–	–	-1.630	–	-1.595	Vdc	9	–	4	–	8	1,16
Switching Times (50 Ω Load)											+1.11 V		Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{4+2+}	2	1.4	3.9	1.4	2.3	3.4	1.4	3.8	ns	9	–	4	2	8	1,16
	t_{4-2-}	2	↓	↓	↓	↓	↓	↓	↓	↓	↓	–	↓	2	↓	↓
	t_{4+3-}	3	↓	↓	↓	↓	↓	↓	↓	↓	↓	–	↓	3	↓	↓
	t_{4-3+}	3	↓	↓	↓	↓	↓	↓	↓	↓	↓	–	↓	3	↓	↓
Rise Time (20 to 80%)	t_{2+}	2	0.9	4.1	1.1	2.2	4.0	1.1	4.6	↓	↓	–	↓	2	↓	↓
	t_{3+}	3	↓	↓	↓	↓	↓	↓	↓	↓	↓	–	↓	3	↓	↓
Fall Time (20 to 80%)	t_{2-}	2	↓	↓	↓	↓	↓	↓	↓	↓	↓	–	↓	2	↓	↓
	t_{3-}	3	↓	↓	↓	↓	↓	↓	↓	↓	↓	–	↓	3	↓	↓

* Inputs 4, 5, 12 and 13 Have Same $I_{in\ H}$ Limit
Inputs 6, 7, 10 and 11 Have Same $I_{in\ H}$ Limit

MOTOROLA

MC10118

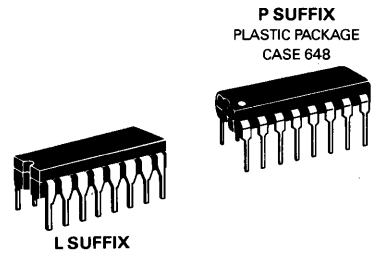
MECL 10K SERIES

DUAL 2-WIDE 3-INPUT "OR-AND" GATE

DUAL 2-WIDE 3-INPUT "OR-AND" GATE

The MC10118 is a basic logic building block providing the OR/AND function, useful in data control and digital multiplexing applications.

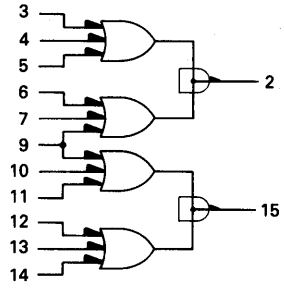
P_D = 100 mW typ/pkg (No Load)
t_{pd} = 2.3 ns typ
t_r, t_f = 2.5 ns typ (20%–80%)



P SUFFIX
PLASTIC PACKAGE
CASE 648

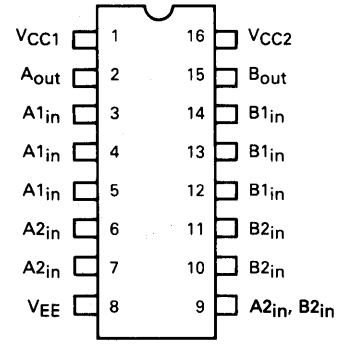
L SUFFIX
CERAMIC PACKAGE
CASE 620

LOGIC DIAGRAM



V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

PIN ASSIGNMENT



ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

@ Test Temperature	V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
	TEST VOLTAGE VALUES (Volts)				
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10118 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	29	–	20	26	–	29	mAdc	–	–	–	–	8	1,16
Input Current	$I_{in\ H}$*	6	–	425	–	–	265	–	265	μAdc	6	–	–	–	8	1,16
		12	–	390	–	–	245	–	245	↓	7	–	–	–	↓	↓
		9	–	560	–	–	350	–	350		9	–	–	–		
	$I_{in\ L}$	6	0.5	–	0.5	–	–	0.3	–	μAdc	–	6	–	–	8	1,16
		7	↓	–	↓	–	–	↓	–		–	7	–	–	↓	↓
		9		–		–	–		–	↓	–	9	–	–		
Logic "1" Output Voltage	V_{OH}	2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	3,9	–	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	–	–	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	2	-1.080	–	-0.980	–	–	-0.910	–	Vdc	9	–	3	–	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	–	3	8	1,16
Switching Times (50 Ω Load)											+1.11 V		Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{6+2+}	2	1.4	3.9	1.4	2.3	3.4	1.4	3.8	ns	3	–	6	2	8	1,16
	t_{6-2-}	↓	1.4	3.9	1.4	2.3	3.4	1.4	3.8	↓	↓	–	↓	↓	↓	↓
Rise Time (20 to 80%)	t_+		0.8	4.1	1.5	2.5	4.0	1.5	4.6			–				
Fall Time (20 to 80%)	t_-	↓	0.8	4.1	1.5	2.5	4.0	1.5	4.6	↓	↓	–	↓	↓	↓	↓

* Inputs 3, 4, 5, 12, 13 and 14 Have Same $I_{in\ H}$ Limit
Inputs 6, 7, 10 and 11 have same $I_{in\ H}$ Limit

MOTOROLA

MC10119

MECL 10K SERIES

4-WIDE 4-3-3-3-INPUT "OR-AND" GATE

The MC10119 is a 4-Wide 4-3-3-3-Input OR/AND gate with one input from two gates common to pin 10.

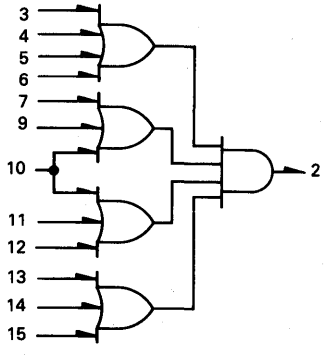
P_D = 100 mW typ/pkg (No Load)
t_{pd} = 2.3 ns typ
t_r, t_f = 2.5 ns typ (20%–80%)

4-WIDE 4-3-3-3-INPUT "OR-AND" GATE

P SUFFIX
PLASTIC PACKAGE
CASE 648

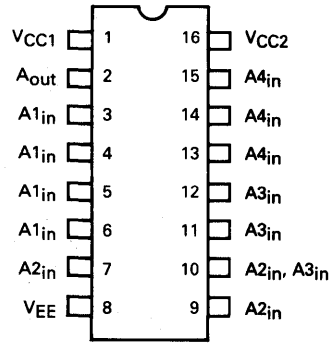
L SUFFIX
CERAMIC PACKAGE
CASE 620

LOGIC DIAGRAM



V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

PIN ASSIGNMENT



ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
−30°C	−0.890	−1.890	−1.205	−1.500	−5.2
+25°C	−0.810	−1.850	−1.105	−1.475	−5.2
+85°C	−0.700	−1.825	−1.035	−1.440	−5.2

Characteristic	Symbol	Pin Under Test	MC10119 Test Limits −30°C Min	−30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	29	–	20	26	–	29	mAdc	–	–	–	–	8	1,16
Input Current	$I_{in\ H}$ *	3	–	390	–	–	245	–	245	μAdc	7	–	–	–	8	1,16
		10	–	495	–	–	310	–	310	↓	10	–	–	–	↓	↓
	$I_{in\ L}$	7	0.5	–	0.5	–	–	0.3	–	μAdc	–	7	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	3,10,15	–	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	2	-2.000	-1.675	-1.990	–	-1.650	-1.920	-1.615	Vdc	–	–	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	2	-1.080	–	-0.980	–	–	-0.910	–	Vdc	10,15	–	3	–	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	–	3	8	1,16
Switching Times (50 Ω Load)											+1.11 V		Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{3+2+}	2	1.4	3.9	1.4	2.3	3.4	1.4	3.8	ns	10,13	–	3	2	8	1,16
	t_{3-2-}	↓	1.4	3.9	1.4	2.3	3.4	1.4	3.8	↓	↓	–	↓	↓	↓	↓
Rise Time (20 to 80%)	t_+		0.8	4.1	1.5	2.5	4.0	1.5	4.6			–				
Fall Time (20 to 80%)	t_-	↓	0.8	4.1	1.5	2.5	4.0	1.5	4.6	↓	↓	–	↓	↓	↓	↓

*Inputs 3,4,5,6,7,9,11,12,13,14,15 Have Same $I_{in\ H}$ Limit

MOTOROLA

MC10121

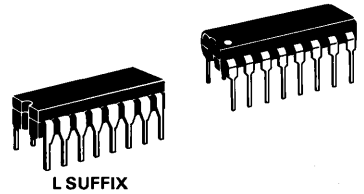
MECL 10K SERIES

4-WIDE "OR-AND/OR-AND-INVERT" GATE

The MC10121 is a basic logic building block providing the simultaneous OR-AND/OR-AND-INVERT function, useful in data control and digital multiplexing applications.

P_D = 100 mW typ/pkg (No Load)
t_{pd} = 2.3 ns typ
t_r, t_f = 2.5 ns typ (20%–80%)

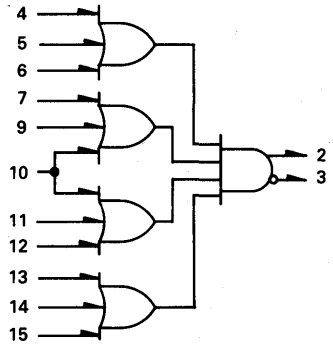
4-WIDE "OR-AND/OR-AND-INVERT" GATE



P SUFFIX
PLASTIC PACKAGE
CASE 648

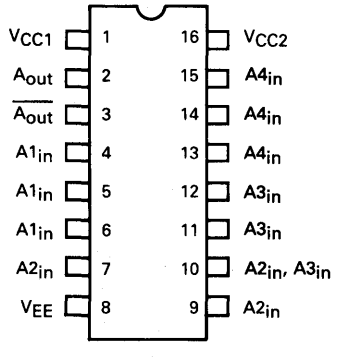
L SUFFIX
CERAMIC PACKAGE
CASE 620

LOGIC DIAGRAM



V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

PIN ASSIGNMENT



ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

@ Test Temperature	TEST VOLTAGE VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}
−30°C	−0.890	−1.890	−1.205	−1.500	−5.2
+25°C	−0.810	−1.850	−1.105	−1.475	−5.2
+85°C	−0.700	−1.825	−1.035	−1.440	−5.2

Characteristic	Symbol	Pin Under Test	MC10121 Test Limits −30°C Min	−30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	**29**	–	20	26	–	**29**	mAdc	–	–	–	–	8	1,16
Input Current	$I_{in\ H}$	7	–	**390**	–	–	**245**	–	**245**	μAdc	7	–	–	–	8	1,16
		9	–	**390**	–	–	**245**	–	**245**	↓	9	–	–	–	↓	↓
		10	–	**495**	–	–	**310**	–	**310**	↓	10	–	–	–	↓	↓
	$I_{in\ L}$	7	**0.5**	–	0.5	–	–	**0.3**	–	μAdc	–	7	–	–	8	1,16
		9	↓	–	↓	–	–	↓	–	↓	–	9	–	–	↓	↓
		10	↓	–	↓	–	–	↓	–	↓	–	10	–	–	↓	↓
Logic "1" Output Voltage	V_{OH}	3	−1.060	−0.780	−0.960	–	−0.700	−0.890	−0.590	Vdc	–	–	–	–	8	1,16
		2	−1.060	−0.780	−0.960	–	−0.700	−0.890	−0.590	Vdc	4,10,13	–	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	3	−2.000	−1.675	−1.990	–	−1.650	−1.920	−1.615	Vdc	4,10,13	–	–	–	8	1,16
		2	−2.000	−1.675	−1.990	–	−1.650	−1.920	−1.615	Vdc	–	–	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	3	−1.080	–	−0.980	–	–	−0.910	–	Vdc	–	–	–	4	8	1,16
		2	−1.080	–	−0.980	–	–	−0.910	–	Vdc	10,13	–	4	–	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	3	–	−1.655	–	–	−1.630	–	−1.595	Vdc	–	–	4	–	8	1,16
		2	–	−1.655	–	–	−1.630	–	−1.595	Vdc	10,13	–	–	4	8	1,16
Switching Times (50 Ω Load)											+1.11 V		Pulse In	Pulse Out	−3.2 V	+2.0 V
Propagation Delay	t_{4+3-}	3	**1.4**	**3.9**	**1.4**	2.3	**3.4**	**1.4**	**3.8**	ns	10,13	–	4	3	8	1,16
	t_{4-3+}	3	↓	↓	↓	↓	↓	↓	↓	↓	↓	–	↓	3	↓	↓
	t_{4+2+}	2	↓	↓	↓	↓	↓	↓	↓	↓	↓	–	↓	2	↓	↓
	t_{4-2-}	2	↓	↓	↓	↓	↓	↓	↓	↓	↓	–	↓	2	↓	↓
Rise Time (20 to 80%)	t_{3+}	3	**0.9**	**4.1**	**1.1**	2.5	**4.0**	**1.1**	**4.6**	↓	↓	–	↓	3	↓	↓
	t_{2+}	2	↓	↓	↓	↓	↓	↓	↓	↓	↓	–	↓	2	↓	↓
Fall Time (20 to 80%)	t_{3-}	3	↓	↓	↓	↓	↓	↓	↓	↓	↓	–	↓	3	↓	↓
	t_{2-}	2	↓	↓	↓	↓	↓	↓	↓	↓	↓	–	↓	2	↓	↓

*This is advance information and specifications are subject to change without notice.

MOTOROLA

MC10123

TRIPLE 4-3-3 INPUT BUS DRIVER

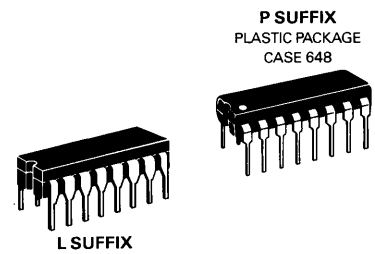
The MC10123 consists of three NOR gates designed for bus driving applications on card or between cards. Output low logic levels are specified with $V_{OL} \leq -2.0$ Vdc so that the bus may be terminated to -2.0 Vdc. The gate output, when low, appears as a high impedance to the bus, because the output emitter-followers of the MC10123 are "turned-off." This eliminates discontinuities in the characteristic impedance of the bus.

The V_{OH} level is specified when driving a 25-ohm load terminated to -2.0 Vdc, the equivalent of a 50-ohm bus terminated at both ends. Although 25 ohms is the lowest characteristic impedance that can be driven by the MC10123, higher impedance values may be used with this part. A typical 50-ohm bus is shown in Figure 1.

P_D = 310 mW typ/pkg (No Load)
t_{pd} = 3.0 ns typ
t_r, t_f = 2.5 ns typ (20%–80%9

MECL 10K SERIES

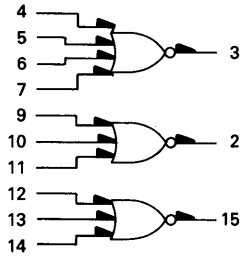
TRIPLE 4-3-3 INPUT BUS DRIVER



P SUFFIX
PLASTIC PACKAGE
CASE 648

L SUFFIX
CERAMIC PACKAGE
CASE 620

LOGIC DIAGRAM



V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

PIN ASSIGNMENT

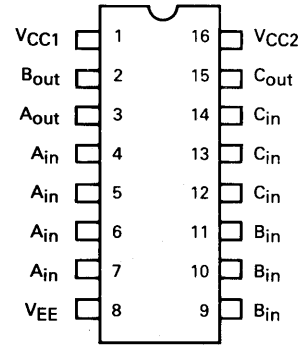
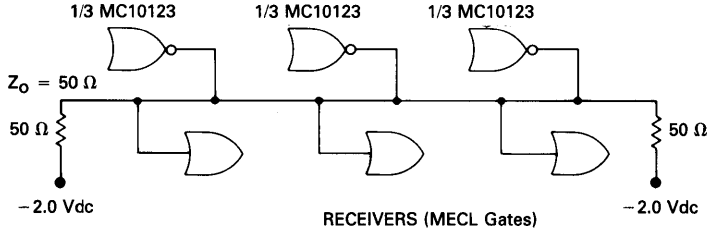


FIGURE 1 — 50-OHM BUS DRIVER



ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 25-ohm resistor to −2.1 volts. Test procedures are shown for only one input an one output. The other inputs and outputs are tested in the same manner.

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
−30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10123 Test Limits −30°C Min	−30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	82	–	71	75	–	82	mAdc	4,5,6,7,9,10 11,12,13,14	–	–	–	8	1,16
Input Current	I_{inH}	4	–	350	–	–	220	–	220	μAdc	4	–	–	–	8	1,16
	I_{inL}	4	–	–	0.5	–	–	–	–	μAdc	–	4			8	1,16
Logic "1" Output Voltage	V_{OH}	3	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	–	–	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	3	-2.15	-2.030	-2.15	–	-2.030	-2.15	-2.030	Vdc	4,5,6,7,9,12	–	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	3	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	–	4,5,6,7	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	3	–	-2.010	–	–	-2.010	–	-2.010	Vdc	9,12	–	4,5,6,7	–	8	1,16
Switching Times (25-ohm load)													Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{4+3-}	3	1.2	4.6	1.2	3.0	4.4	1.2	4.8	ns	–	–	4	3	8	1,16
	t_{4-3+}		1.2	4.6	1.2	3.0	4.4	1.2	4.8		–	–				
Rise Time (20 to 80%)	t_{3+}		1.0	3.7	1.0	2.5	3.5	1.0	3.9		–	–				
Fall Time (20 to 80%)	t_{3-}		1.0	3.7	1.0	2.5	3.5	1.0	3.9		–	–				

MOTOROLA

MC10124

QUAD TTL TO MECL TRANSLATOR

The MC10124 is a quad translator for interfacing data and control signals between a saturated logic section and the MECL section of digital systems. The MC10124 has TTL compatible inputs, and MECL complementary open-emitter outputs that allow use as an inverting/non-inverting translator or as a differential line driver. When the common strobe input is at the low logic level, it forces all true outputs to a MECL low logic state and all inverting outputs to a MECL high logic state.

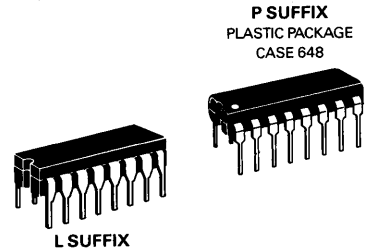
Power supply requirements are ground, +5.0 Volts, and −5.2 Volts. Propagation delay of the MC10124 is typically 3.5 ns. The dc levels are standard or Schottky TTL in, MECL 10,000 out.

An advantage of this device is that TTL level information can be transmitted differentially, via balanced twisted pair lines, to the MECL equipment, where the signal can be received by the MC10115 or MC10116 differential line receivers. The MC10124 is useful in computers, instrumentation, peripheral controllers, test equipment, and digital communications systems.

P_D	= 380 mW typ/pkg (No Load)
t_{pd}	= 3.5 ns typ (+ 1.5 Vdc in to 50% out)
t_r, t_f	= 2.5 ns typ (20%–80%)

MECL 10K SERIES

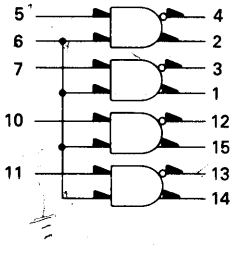
QUAD TTL TO MECL TRANSLATOR



P SUFFIX
PLASTIC PACKAGE
CASE 648

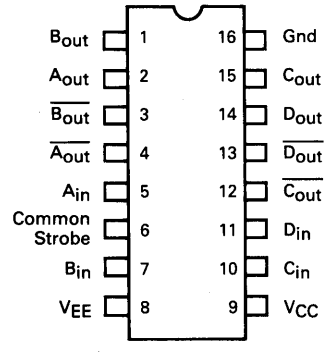
L SUFFIX
CERAMIC PACKAGE
CASE 620

LOGIC DIAGRAM



Gnd = Pin 16
V_{CC} (+5.0 Vdc) = Pin 9
V_{EE} (−5.2 Vdc) = Pin 8

PIN ASSIGNMENT



ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown for only one translator. The other translators are tested in the same manner.

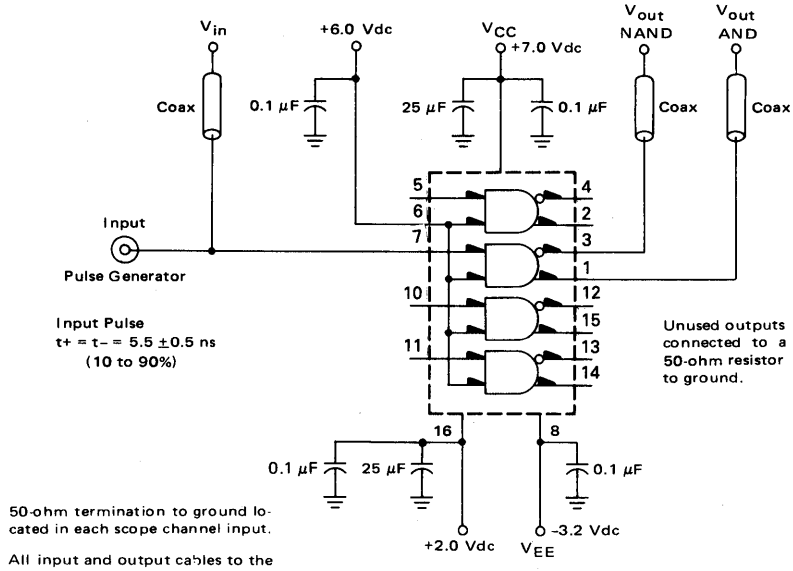
@ Test Temperature	TEST VOLTAGE/CURRENT VALUES									
	Volts								mA	
	V_{IH}	$V_{IL\ max}$	$V_{IHA'}$	$V_{ILA'}$	V_F	V_R	V_{CC}	V_{EE}	I_I	I_{in}
-30°C	+4.0	+0.40	+2.00	+1.10	+0.40	+2.40	+5.00	-5.2	-10	+1.0
+25°C	+4.0	+0.40	+1.80	+1.10	+0.40	+2.40	+5.00	-5.2	-10	+1.0
+85°C	+4.0	+0.40	+1.80	+0.90	+0.40	+2.40	+5.00	-5.2	-10	+1.0

Characteristic	Symbol	Pin Under Test	MC10124 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW: V_{IH}	$V_{IL\ max}$	$V_{IHA'}$	$V_{ILA'}$	V_F	V_R	V_{CC}	V_{EE}	I_I	I_{in}	Gnd
Negative Power Supply Drain Current	I_E	8	–	**72**	–	–	-66	–	**72**	mAdc	–	–	–	–	–	–	9	8	–	–	16
Positive Power Supply Drain Current	I_{CCH}	9	–	**16**	–	–	16	–	**18**	mAdc	5,6,7,10,11	–	–	–	–	–	9	8	–	–	16
	I_{CCL}	9	–	**25**	–	–	25	–	**25**	mAdc	–	–	–	–	–	–	9	8	–	–	5,6,7,10,11,16
Reverse Current	I_R	6	–	**200**	–	–	200	–	**200**	μAdc	–	–	–	–	5,7,10,11	6	9	8	–	–	16
		7	–	**50**	–	–	50	–	**50**	μAdc	–	–	–	–	6	7	9	8	–	–	16
Forward Current	I_F	6	–	**−12.8**	–	–	-12.8	–	**−12.8**	mAdc	5,7,10,11	–	–	–	6	–	9	8	–	–	16
		7	–	**−3.2**	–	–	-3.2	–	**−3.2**	mAdc	6	–	–	–	7	–	9	8	–	–	16
Input Breakdown Voltage	BV_{in}	6	**5.5**		5.5	–	–	**5.5**	–	Vdc	–	–	–	–	–	–	9	8	–	6	5,7,10,11,16
		7	**5.5**	–	5.5	–	–	**5.5**	–	Vdc	–	–	–	–	–	–	9	8	–	7	6,16
Clamp Input Voltage	V_I	6	–	**−1.5**	–	–	-1.5	–	**−1.5**	Vdc	–	–	–	–	–	–	9	8	6	–	16
		7	–	**−1.5**	–	–	-1.5	–	**−1.5**	Vdc	–	–	–	–	–	–	9	8	7	–	16
High Output Voltage	V_{OH}	1	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	6,7	–	–	–	–	–	9	8	–	–	16
		3	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	–	6,7	–	–	–	–	9	8	1 –	–	16
Low Output Voltage	V_{OL}	1	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	–	6,7	–	–	–	–	9	8	–	–	16
		3	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	6,7	–	–	–	–	–	9	8	–	–	16
High Threshold Voltage	V_{OHA}	1	-1.080	–	-0.980	–	–	-0.910	–	Vdc	6	–	7	–	–	–	9	8	–	–	16
		3	-1.080	–	-0.980	–	–	-0.910	–	Vdc	6	–	–	7	–	–	9	8	–	–	16
Low Threshold Voltage	V_{OLA}	1	–	-1.655	–	–	-1.630	–	-1.595	Vdc	6	–	–	7	–	–	9	8	–	–	16
		3	–	-1.655	–	–	-1.630	–	-1.595	Vdc	6	–	7	–	–	–	9	8	–	–	16
Switching Time (50-Ω load)											**+6.0 Vdc**	**Pulse In**	**Pulse Out**				**+7.0 Vdc**	**-3.2 Vdc**			**+2.0 Vdc**
Propagation Delay (+3.5 Vdc to 50%)①	t_{6+1+}	1	**1.0**	**6.8**	1.0	3.5	6.0	**1.0**	**6.8**	ns	7	6	1	–	–	–	9	8	–	–	16
	t_{6-1-}	↓	↓	↓	↓	↓	↓	↓	↓	↓	7	6	↓	–	–	–	↓	↓	–	–	↓
	t_{7+1+}										6	7		–	–	–			–	–	
	t_{7-1-}										↓	↓		–	–	–			–	–	
	t_{7+3-}	3											3	–	–	–			–	–	
	t_{7-3+}	3											3	–	–	–			–	–	
Rise Time (20% to 80%)	t_{1+}	1	**1.0**	**4.2**	1.1	2.5	3.9	**1.1**	**4.3**				1	–	–	–			–	–	
Fall Time (80% to 20%)	t_{1-}	1	↓	↓	1.1	2.5	3.9	↓	↓	↓	↓	↓	1	–	–	–	↓	↓	–	–	↓

① See switching time test circuit. Propagation delay for this circuit is specified from +1.5 Vdc in to the 50% point on the output waveform. The +3.5 Vdc is shown here because all logic and supply levels are shifted 2 volts positive.)

3

SWITCHING TIME TEST CIRCUIT



NOTE: All power supply and logic levels are shown shifted 2 volts positive.

MOTOROLA

MC10125

QUAD MECL TO TTL TRANSLATOR

The MC10125 is a quad translator for interfacing data and control signals between the MECL section and saturated logic sections of digital systems. The MC10125 incorporates differential inputs and Schottky TTL "totem pole" outputs. Differential inputs allow for use as an inverting/non-inverting translator or as a differential line receiver. The V_{BB} reference voltage is available on pin 1 for use in single-ended input biasing. The outputs of the MC10125 go to a low logic level whenever the inputs are left floating.

Power supply requirements are ground, +5.0 Volts and −5.2 Volts. Propagation delay of the MC10125 is typically 4.5 ns. The MC10125 has fanout of 10 TTL loads. The dc levels are MECL 10,000 in and Schottky TTL, or TTL out. This device has an input common mode noise rejection of ± 1.0 Volt.

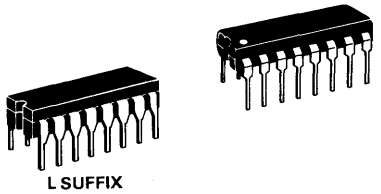
An advantage of this device is that MECL level information can be received, via balanced twisted pair lines, in the TTL equipment. This isolates the MECL logic from the noisy TTL environment. This device is useful in computers, instrumentation, peripheral controllers, test equipment and digital communications systems.

P_D	= 380 mW typ/pkg (No Load)
t_{pd}	= 4.5 ns typ (50% to + 1.5 Vdc out)
t_r, t_f	= 2.5 ns typ (1.0 V to 2.0 V)

MECL 10K SERIES

QUAD MECL TO TTL TRANSLATOR

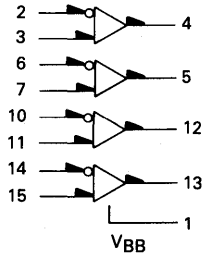
3



P SUFFIX
PLASTIC PACKAGE
CASE 648

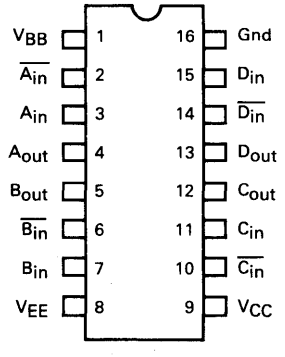
L SUFFIX
CERAMIC PACKAGE
CASE 620

LOGIC DIAGRAM



Gnd = Pin 16
V_{CC} (+5.0 Vdc) = Pin 9
V_{EE} (−5.2 Vdc) = Pin 8

PIN ASSIGNMENT



ELECTRICAL CHARACTERISTICS

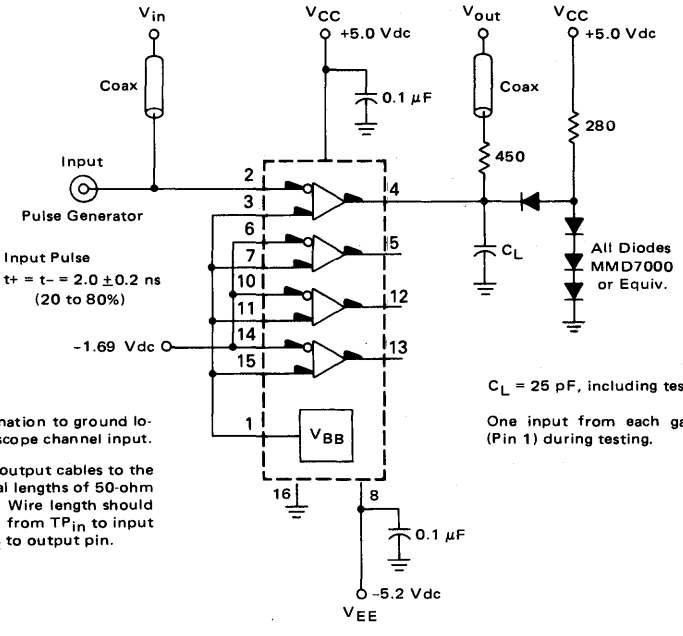
Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Test procedures are shown for only one translator. The other translators are tested in the same manner.

@ Test Temperature	$V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{IHH}	V_{ILH}	V_{IHL}	V_{ILL}	V_{BB}	V_{CC}	V_{EE}
	TEST VOLTAGE VALUES (Volts)										
-30°C	-0.890	-1.890	-1.205	-1.500	+0.110	-0.890	-1.890	-2.890	From Pin 1	+5.0	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	+0.190	-0.850	-1.810	-2.850		+5.0	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	+0.300	-0.825	-1.700	-2.825		+5.0	-5.2

Characteristic	Symbol	Pin Under Test	MC10125 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{IHH}	V_{ILH}	V_{IHL}	V_{ILL}	V_{BB}	V_{CC}	V_{EE}	Gnd	Output Condition
Negative Power Supply Drain Current	I_E	8	–	44	–	–	40	–	44	mAdc	–	–	–	–	–	–	–	–	3,7,11,15	9	8	16	–
Positive Power Supply Drain Current	I_{CCH}	9	–	52	–	–	52	–	52	mAdc	2,6,10,14	–	–	–	–	–	–	–	3,7,11,15	9	8	16	–
	I_{CCL}	9	–	39	–	–	39	–	39	mAdc	–	2,6,10,14	–	–	–	–	–	–	3,7,11,15	9	8	16	–
Input Current	$I_{in\ H}$ ①	2	–	180	–	–	115	–	115	μAdc	2,6,10,14	–	–	–	–	–	–	–	3,7,11,15	9	8	16	–
Input Leakage Current	I_{CBO}	2	–	1.5	–	–	1.0	–	1.0	μAdc	–	–	–	–	–	–	–	–	3,7,11,15	9	2,6,8,10,14	16	–
High Output Voltage	V_{OH}	4	2.5	–	2.5	–	–	2.5	–	Vdc	–	2,6,10,14	–	–	–	–	–	–	3,7,11,15	9	8	16	-2.0 mA
Low Output Voltage	V_{OL}	4	–	0.5	–	–	0.5	–	0.5	Vdc	2,6,10,14	–	–	–	–	–	–	–	3,7,11,15	9	8	16	20 mA
High Threshold Voltage	V_{OHA}	4	2.5	–	2.5	–	–	2.5	–	Vdc	–	6,10,14	–	2	–	–	–	–	3,7,11,15	9	8	16	-2.0 mA
Low Threshold Voltage	V_{OLA}	4	–	0.5	–	–	0.5	–	0.5	Vdc	6,10,14	–	2	–	–	–	–	–	3,7,11,15	9	8	16	20 mA
Indeterminate Input Protection Tests	V_{OLS1}	4	–	0.5	–	–	0.5	–	0.5	Vdc	–	–	–	–	–	–	–	–	–	9	2,3,6,7,8, 10,11,14,15	16	20 mA
	V_{OLS2}	4	–	0.5	–	–	0.5	–	0.5	Vdc	–	–	–	–	–	–	–	–	–	9	8	16	20 mA
Short-Circuit Current	I_{OS}	4	40	100	40	–	100	40	100	mA	–	2,6,10,14	–	–	–	–	–	–	3,7,11,15	9	8	4,16	–
Reference Voltage	V_{BB}	1	-1.420	-1.28	-1.350	–	-1.230	-1.295	-1.150	Vdc	–	2,6,10,14	–	–	–	–	–	–	3,7,11,15	–	–	–	–
Common Mode Rejection Tests	V_{OH}	4	2.5	–	2.5	–	–	2.5	–	Vdc	–	–	–	–	3	2	–	–	–	9	8	16	-2.0 mA
		4	2.5	–	2.5	–	–	2.5	–		–	–	–	–	–	–	3	2	–	9	8	16	-2.0 mA
	V_{OL}	4	–	0.5	–	–	0.5	–	0.5	Vdc	–	–	–	–	2	3	–	–	–	9	8	16	20 mA
		4	–	0.5	–	–	0.5	–	0.5		–	–	–	–	–	–	2	3	–	9	8	16	20 mA
Switching Times											Pulse In	Pulse Out	C_L (pF)										
Propagation Delay (50% to +1.5 Vdc)	t_{6+5-}	5	1.0	6.0	1.0	4.5	6.0	1.0	6.0	ns	6	5	25	–	–	–	–	–	3,7,11,15	9	8	16	–
	t_{6-5+}	5	↓	↓	↓	↓	↓	↓	↓	↓	6	5	↓	–	–	–	–	–	↓	↓	↓	↓	–
	t_{2+4-}	4	↓	↓	↓	↓	↓	↓	↓	↓	2	4	↓	–	–	–	–	–	↓	↓	↓	↓	–
	t_{2-4+}	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	–	–	–	–	–	↓	↓	↓	↓	–
Rise Time (+1.0 Vdc to 2.0 Vdc)	t_{4+}	↓	–	3.3	–	–	3.3	–	3.3	↓	↓	↓	↓	–	–	–	–	–	↓	↓	↓	↓	–
Fall Time (+1.0 Vdc to 2.0 Vdc)	t_{4-}	↓	–	3.3	–	–	3.3	–	3.3	↓	↓	↓	↓	–	–	–	–	–	↓	↓	↓	↓	–

① Individually test each input, apply $V_{IH\ max}$ to pin under test.

SWITCHING TIME TEST CIRCUIT



C_L = 25 pF, including test fixture

One input from each gate must be tied to V_{BB} (Pin 1) during testing.

50-ohm termination to ground located in each scope channel input.

All input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be < 1/4 inch from TP_{in} to input pin and TP_{out} to output pin.

MOTOROLA

MC10128

BUS DRIVER

The MC10128 is designed to provide outputs which are compatible with IBM-type bus levels; or, if desired, it will drive TTL type loads and/or provide TTL three-state outputs. The inputs accept MECL 10,000 levels. The MC10128 output levels can be accepted by the MC10129 Bus Receiver.

The operating mode IBM or TTL is selected by tying the external control pins to ground or leaving them open. Leaving a control pin open selects the TTL mode, and tying a control pin to ground selects the IBM mode.

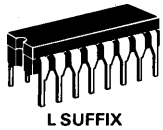
The TTL mode will drive a 25-ohm load, terminated to +1.5 Vdc or a 50-ohm load, terminated to ground. The device has totem-pole type outputs, but it also has a disable input for three-state logic operation when the circuit is used in the TTL mode. When in the high state the disable input causes the output to exhibit a high impedance state when it would normally be a positive logic "1" state. When the strobe is in the high state it inhibits the output data in the low state.

Latches are provided on each data input for temporary storage. When the clock input is in the low logic state, information present at the data inputs D1 and D2 will be fed directly to the latch output. When the clock goes high, the input data is latched. The outputs are gated to allow full bus driving and strobing capability.

The MC10128 is useful in interfacing and bus applications in central processors, mini-computers, and peripheral equipment.

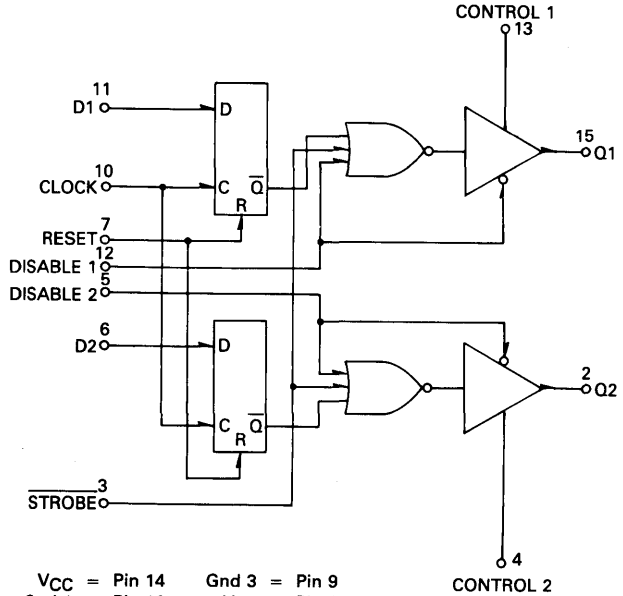
MECL 10K SERIES

BUS DRIVER



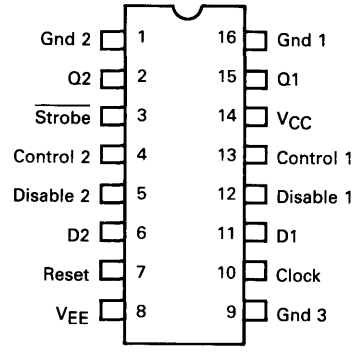
L SUFFIX
CERAMIC PACKAGE
CASE 620

LOGIC DIAGRAM



V_{CC} = Pin 14 Gnd 3 = Pin 9
Gnd 1 = Pin 16 V_{EE} = Pin 8
Gnd 2 = Pin 1

PIN ASSIGNMENT



ELECTRICAL CHARACTERISTICS — TTL MODE

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained.

@ Test Temperature	TEST VOLTAGE/CURRENT VALUES: TEST VOLTAGE VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	V_{CC}	mAdc I_{OH1}	µAdc I_{OH2}	mAdc I_{OL}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2	**5.00**	-50	-100	+56
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2	**5.00**	-50	-100	+56
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2	**5.00**	-50	-100	+56

Characteristic	Symbol	Pin Under Test	MC10128 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	V_{CC}	I_{OH1}	I_{OH2}	I_{OL}	Gnd
Negative Power Supply Drain Current	I_E	8	–	100	–	91	–	100	mAdc	6,11	–	–	–	8	14	–	–	–	1, 9,16
Positive Power Supply Drain Current	I_{CC}	14	–	50	–	50	–	50	mAdc	6,11	–	–	–	8	14	–	–	–	1, 9,16
Input Leakage Current	I_{inH}	3	–	490	–	620	–	620	µAdc	3	–	–	–	8	14	–	–	–	1, 9,16
		7	–	560	–	350	–	350		7	–	–	–			–	–	–	
		10	–	425	–	265	–	265		10	–	–	–			–	–	–	
		11	–	425	–	265	–	265		11	–	–	–			–	–	–	
		12	–	775	–	485	–	485		12	–	–	–			–	–	–	
	I_{inL}	All	0.5	–	0.5	–	0.3	–	µAdc	–	*	–	–	8	14	–	–	–	1, ,9 ,16
Logic "1" Output Voltage	V_{OH}	15	2.5	–	2.5	–	2.5	–	Vdc	11	–	–	–	8	14	2,15	–	–	1, ,9 ,16
		15	2.7	–	2.7	–	2.7	–	Vdc	11	–	–	–	8	14	–	2,15	–	1, ,9 ,16
Logic "0" Output Voltage	V_{OL}	15	–	0.5	–	0.5	–	0.5	Vdc	3	–	–	–	8	14	–	–	2,15	1, ,9 ,16
		2	–	0.5	–	0.5	–	0.5	Vdc	3	–	–	–	8	14	–	–	2,15	1, ,9 ,16
Logic "1" Threshold Voltage	V_{OHA}	15	2.5	–	2.5	–	2.5	–	Vdc	11	7	–	10 ③	8	14	2,15	–	–	1, ,9 ,16
		2	2.5	–	2.5	–	2.5	–	Vdc	6	7	–	10 ③	8	14	2,15	–	–	1, ,9 ,16
Logic "0" Threshold Voltage	V_{OLA}	15	–	0.5	–	0.5	–	0.5	Vdc	11	7,10	3	–	8	14	–	–	2,15	1, ,9 ,16
		2	–	0.5	–	0.5	–	0.5	Vdc	6	7,10	3	–	8	14	–	–	2,15	1, ,9 ,16
Output Short Circuit Current	I_{SC}	15	–	260	–	260	–	260	mAdc	11	–	–	–	8	14	–	–	–	1,2, ,9 ,15,16
		2	–	260	–	260	–	260	mAdc	6	–	–	–	8	14	–	–	–	1,2, ,9 ,15,16
Switching Times † Propagation Delay					T[illegible]					-0.890 V	-1.690 V	Pulse In	Pulse Out						
Data Input	t_{11+15+}	15	1.0	17	1.0	18	1.0	24	ns	–	10	11	15	8	14	–	–	–	1, 9 ,16
	t_{11-15-}	15	1.0	17	1.0	18	1.0	24		–	10	11				–	–	–	
Clock Input	t_{10-15+}	15 ①	1.0	20	1.0	20	1.0	25		–	–	10,11				–	–	–	
	t_{10-15-}	15 ②	1.0	20	1.0	20	1.0	25		–	–	10,11				–	–	–	
Reset Input	t_{7+15-}	15 ②	1.0	20	1.0	20	1.0	25		11	–	7,10				–	–	–	
	t_{7+2-}	2 ②	1.0	20	1.0	20	1.0	25		6	–	7,10	2			–	–	–	
$\overline{\text{STROBE}}$ Input	t_{3+15-}	15	1.0	17	1.0	18	1.0	24		11	10	3	15			–	–	–	
	t_{3-15+}	15	1.0	17	1.0	18	1.0	24		–			15			–	–	–	
	t_{3+2-}	2	1.0	17	1.0	18	1.0	24		6			2			–	–	–	
	t_{3-2+}	2	1.0	17	1.0	18	1.0	24		–			2			–	–	–	
Setup Time	t_{setupH}	15	–	–	0.6	0.9	–	–		–	–	10,11	15			–	–	–	
	t_{setupL}	15	–	–	0.5	0.8	–	–		–	–					–	–	–	
Hold Time	t_{holdH}	15	–	–	0.7	1.1	–	–		–	–					–	–	–	
	t_{holdL}	15	–	–	0.6	0.8	–	–		–	–					–	–	–	
Rise Time (20% to 80%)	t_{15+}	15	1.0	9.0	1.0	8.0	1.0	9.0		–	10	11				–	–	–	
Fall Time (20% to 80%)	t_{15-}	15	1.0	9.0	1.0	8.0	1.0	9.0		–	10	11				–	–	–	

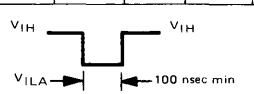
* Apply V_{ILmin} individually to pin under test.

① Output latched to logic Low state prior to test.

② Output latched to logic High state prior to test.

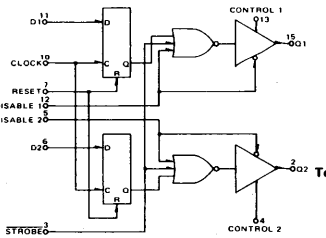
† See waveforms

③ A pulse is applied to pin 10.



ELECTRICAL CHARACTERISTICS – IBM MODE

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained.



@ Test Temperature	TEST VOLTAGE/CURRENT VALUES: TEST VOLTAGE VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	V_{CC}	mAdc I_{OH1}	µAdc I_{OH2}	µAdc I_{OL}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2	+6.00	-59.3	-30	-230
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2	+6.00	-59.3	-30	-230
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2	+6.00	-59.3	-30	-230

Characteristic	Symbol	Pin Under Test	MC10128 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	V_{CC}	I_{OH1}	I_{OH2}	I_{OL}	Gnd
Negative Power Supply Drain Current	I_E	8	–	107	–	97	–	107	mAdc	6,11	–	–	–	8	14	–	–	–	1,4,9,13,16
Positive Power Supply Drain Current	I_{CC}	14	–	73	–	73	–	73	mAdc	6,11	–	–	–	8	14	–	–	–	1,4,9,13,16
Input Leakage Current	I_{inH}	3	–	990	–	620	–	620	µAdc	3	–	–	–	8	14	–	–	–	1,4,9,13,16
		7	–	560	–	350	–	350		7	–	–	–			–	–	–	
		10	–	425	–	265	–	265		10	–	–	–			–	–	–	
		11	–	425	–	265	–	265		11	–	–	–			–	–	–	
		12	–	775	–	485	–	485		12	–	–	–			–	–	–	
	I_{inL}	All	0.5	–	0.5	–	0.3	–	µAdc	–	*	–	–	8	14	–	–	–	1,4,9,13,16
Logic "1" Output Voltage	V_{OH}	15	3.11	–	3.11	–	3.11	–	Vdc	11	–	–	–	8	14	2,15	–	–	1,4,9,13,16
		15	–	5.85	–	5.85	–	5.85	Vdc	11	–	–	–	8	14	–	2,15	–	1,4,9,13,16
Logic "0" Output Voltage	V_{OL}	15	-0.5	0.15	-0.5	0.15	-0.5	0.15	Vdc	3	–	–	–	8	14	–	–	2,15	1,4,9,13,16
		2	-0.5	0.15	-0.5	0.15	-0.5	0.15	Vdc	3	–	–	–	8	14	–	–	2,15	1,4,9,13,16
Logic "1" Threshold Voltage	V_{OHA}	15	3.11	–	3.11	–	3.11	–	Vdc	11	7	–	10 ③	8	14	2,15	–	–	1,4,9,13,16
		2	–	–	–	–	–	–	Vdc	6	7	–	10 ③	8	14	2,15	–	–	1,4,9,13,16
Logic "0" Threshold Voltage	V_{OLA}	15	-0.5	0.25	-0.5	0.25	-0.5	0.25	Vdc	11	7,10	3	–	8	14	–	–	2,15	1,4,9,13,16
		2	-0.5	0.25	-0.5	0.25	-0.5	0.25	Vdc	6	7,10	3	–	8	14	–	–	2,15	1,4,9,13,16
Output Short Circuit Current	I_{SC}	15	–	320	–	320	–	320	mAdc	11	–	–	–	8	14	–	–	–	1,2,4,9,13,15,16
		2	–	320	–	320	–	320	mAdc	6	–	–	–	8	14	–	–	–	1,2,4,9 13,15,16
Switching Times † Propagation Delay					Min	Max				-0.890 V	-1.690 V	Pulse In	Pulse Out						
Data Input	t_{11+15+}	15	1.0	21	1.0	23.0	1.0	33.0	ns	–	10	11	15	8	14	–	–	–	1,4,9,13,16
	t_{11-15-}	15		21						–	10	11				–	–	–	
Clock Input	t_{10-15+}	15 ①		20							–	10,11				–	–	–	
	t_{10-15-}	15 ②		20						–	–	10,11				–	–	–	
Reset Input	t_{7+15-}	15 ②		20						11	–	7,10				–	–	–	
	t_{7+2-}	2 ②		20						6	–	7,10	2			–	–	–	
STROBE Input	t_{3+15-}	15		21						11	10	3	15			–			
	t_{3-15+}	15		21						–			15			–			
	t_{3+2-}	2		21						6			2			–			
	t_{3-2+}	2		21						–			2			–			
Setup Time	t_{setupH}	15	–	–	.7	1.0	–	–		–	–	10,11	15			–			
	t_{setupL}	15	–	–	.7	1.2	–	–		–	–					–			
Hold Time	t_{holdH}	15	–	–	.7	1.1	–	–		–	–					–			
	t_{holdL}	15	–	–	.7	1.0	–	–		–	–					–			
Rise Time (20% to 80%)	t_{15+}	15	1.0	8.0	1.0	8.0	1.0	9.0		–	10	11				–			
Fall Time (20% to 80%)	t_{15-}	15	1.0	8.0	1.0	8.0	1.0	9.0		–	10	11				–			

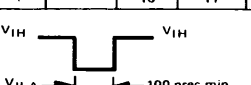
* Apply V_{ILmin} individually to pin under test.

① Output latched to logic Low state prior to test.

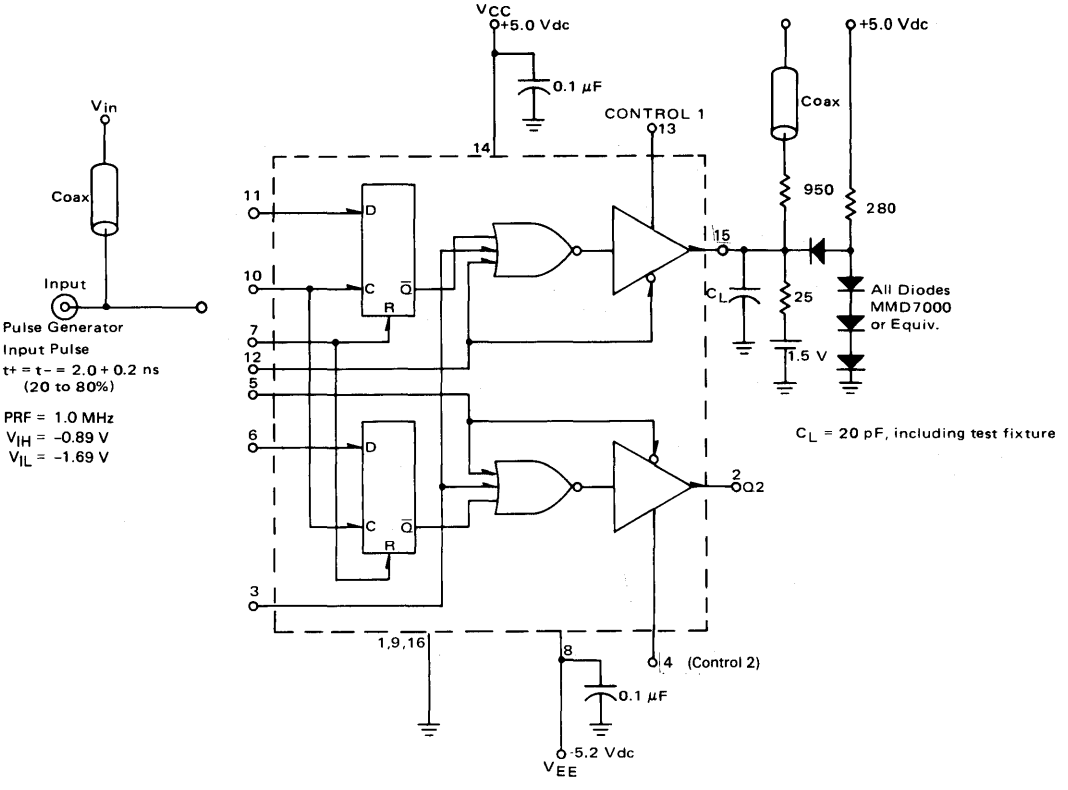
② Output latched to logic High state prior to test.

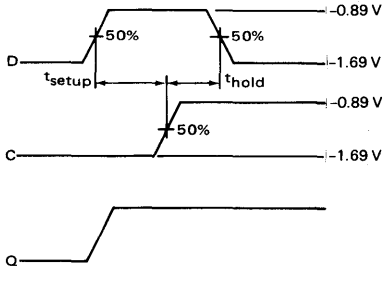
† See waveforms

③ A pulse is applied to pin 10.



SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C – TTL MODE



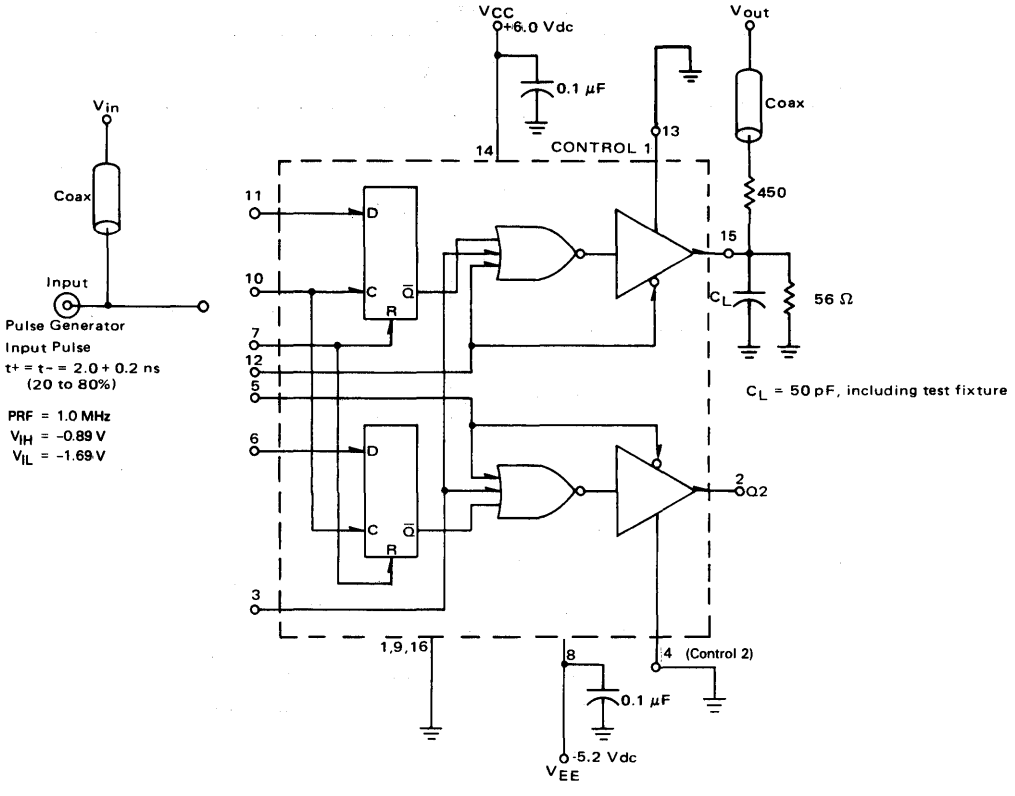


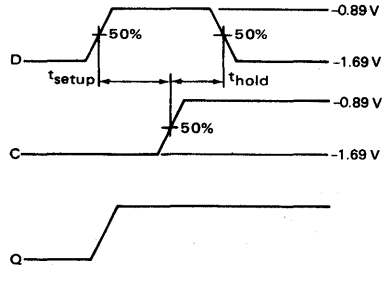
50-ohm termination to ground located in each scope channel input.

All input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be < 1/4 inch from TP_{in} to input pin and TP_{out} to output pin.

3

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C – IBM MODE



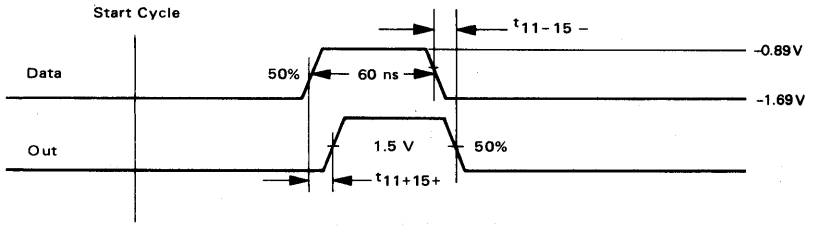


50-ohm termination to ground located in each scope channel input.

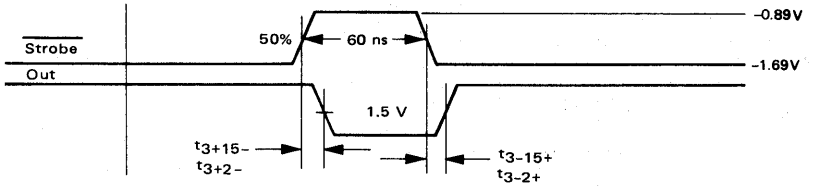
All input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be < 1/4 inch from TP_{in} to input pin and TP_{out} to output pin.

VOLTAGE WAVEFORMS

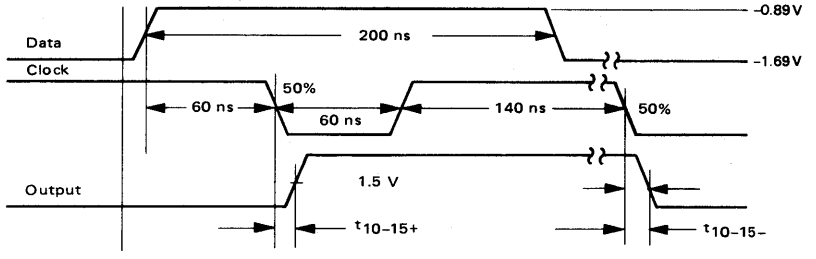
DATA INPUT



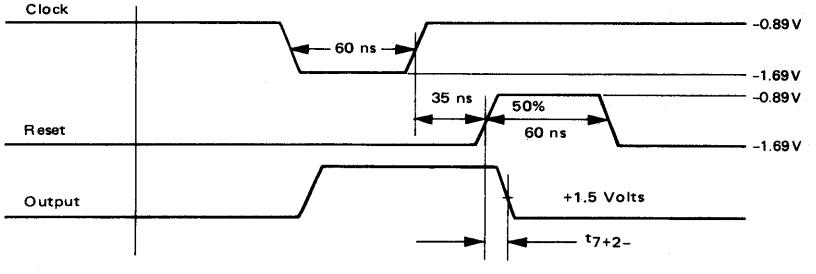
STROBE INPUT



CLOCK INPUT



RESET INPUT



TTL – MODE
V_{OL} = 0.5 Volts Max
V_{OH} = 2.5 Volts Min

IBM – MODE
V_{OL} = 0.25 Volts Max
V_{OH} = 3.11 Volts Min

QUAD BUS RECEIVER

The MC10129 bus receiver works in conjunction with the MC10128 to allow interfacing of MECL 10,000 to other forms of logic and logic buses. The data inputs are compatible with, and accept TTL logic levels as well as levels compatible with IBM-type buses. The clock, strobe, and reset inputs accept MECL 10,000 logic levels.

The data inputs accept the bus levels, and storage elements are provided to yield temporary latch storage of the information after receiving it from the bus. The outputs can be strobed to allow accurate synchronization of signals and/or connection to MECL 10,000 level buses. When the clock is low, the outputs will follow the D inputs, and the reset input is disabled. The latches will store the data on the rising edge of the clock. The outputs are enabled when the strobe input is high. Unused D inputs must be tied to V_{CC} or Gnd. The clock, strobe, and reset inputs each have 50 k ohm pulldown resistors to V_{EE}. They may be left floating, if not used.

The MC10129 will operate in either of two modes. The first mode is obtained by tying the hysteresis control input to V_{EE}. In this mode, the input threshold points of the D inputs are fixed. The second mode is obtained by tying the hysteresis control input to ground. In this mode, input hysteresis is achieved as shown in the test table. This hysteresis is desirable where extra noise margin is required on the D inputs. The outer input pins are unaffected by the mode of operation used.

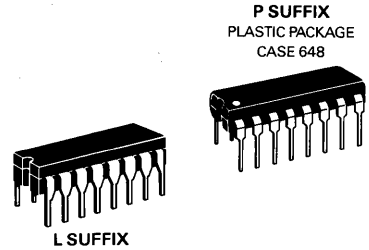
The MC10129 is especially useful in interface applications for central processors, mini-computers, and peripheral equipment.

P_D = 750 mW typ/pkg (No Load)
t_{pd} = 10 ns typ
V_{CC} Max = 7.0 Vdc

MC10129

MECL 10K SERIES

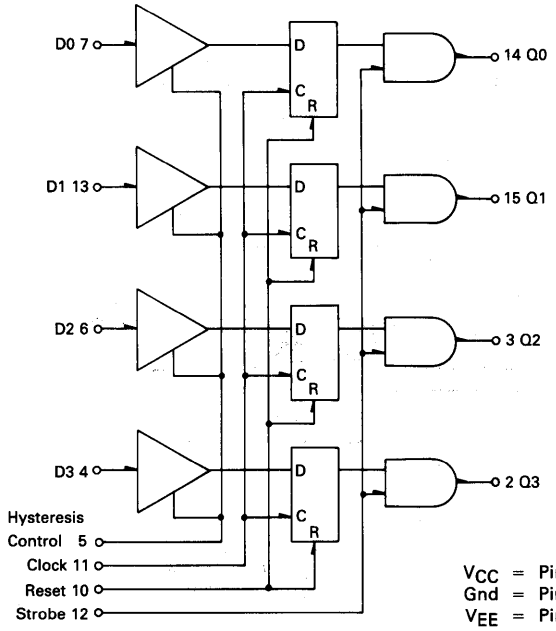
QUAD BUS RECEIVER



P SUFFIX
PLASTIC PACKAGE
CASE 648

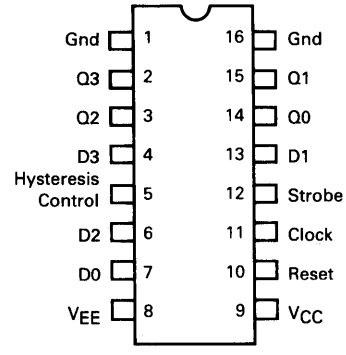
L SUFFIX
CERAMIC PACKAGE
CASE 620

LOGIC DIAGRAM



V_{CC} = Pin 9
Gnd = Pins 1 and 16
V_{EE} = Pin 8

PIN ASSIGNMENT



TRUTH TABLE

D	C	STROBE	RESET	Q_{n+1}
ϕ	ϕ	L	ϕ	L
ϕ	H	ϕ	H	L
L	L	H	ϕ	L
ϕ	H	H	L	Q_n
H	L	H	ϕ	H

ϕ = Don't Care

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown for only one input/output combination. Other combinations are tested in the same manner.

@ Test Temperature	MECL 10,000 INPUT LEVELS V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	* TTL INPUT LEVELS V_{IH}	V_{IL}	$V_{IHA'}$	$V_{ILA'}$	*IBM INPUT LEVELS V_{IH}	V_{IL}	$V_{IHA'}$	$V_{ILA'}$	HYSTERESIS MODE $V_{IHA''}$	$V_{ILA''}$	$V_{IHA'''}$	$V_{ILA'''}$	V_{CC} ①	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	3.000	0.400	2.000	0.800	3.11	0.150	–	–	2.90	2.00	2.20	1.30	+5.0	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	3.000	0.400	2.000	0.800	3.11	0.150	1.700	0.70	2.600	1.700	1.900	1.000	+5.0	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	3.000	0.400	2.000	0.800	3.11	0.150	–	–	2.30	1.400	1.60	0.70	+5.0	-5.2

Characteristic	Symbol	Pin Under Test	MC10129 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{IH}	V_{IL}	$V_{IHA'}$	$V_{ILA'}$	V_{IH}	V_{IL}	$V_{IHA'}$	$V_{ILA'}$	$V_{IHA''}$	$V_{ILA''}$	$V_{IHA'''}$	$V_{ILA'''}$	V_{CC} ①	V_{EE}	Gnd
Negative Power Supply Drain Current	I_E	8	–	167	–	–	152	–	167	mAdc	11	12	–	–	–	–	–	–	–	–	–	–	–	–	–	–	9	8	1,5,16
		8	–	189	–	–	172	–	189	mAdc	11	12	–	–	–	–	–	–	–	–	–	–	–	–	–	–	9	5,8	1,16
Positive Power Supply Drain Current	I_{CC}	9	–	8.0	–	–	8.0	–	8.0	mAdc	–	–	–	–	–	4,6,7,13	–	–	–	4,6,7,13	–	–	–	–	–	–	9	5,8	1,16
Input Current	I_{inH}	4	–	150	–	–	95	–	95	μAdc	–	–	–	–	4	–	–	–	4	–	–	–	–	–	–	–	9	8	1,16
		6	–	150	–	–	95	–	95		–	–	–	–	6	–	–	–	6	–	–	–	–	–	–	–			
		7	–	150	–	–	95	–	95		–	–	–	–	7	–	–	–	7	–	–	–	–	–	–	–			
		10	–	720	–	–	450	–	450		10,11	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–			
		11	–	390	–	–	245	–	245		11	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–			
		12	–	390	–	–	245	–	245		12	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–			
		13	–	150	–	–	95	–	95		–	–	–	–	13	–	–	–	13	–	–	–	–	–	–	–			
	I_{CBO} ⑤	4	–	1.5	–	–	1.0	–	1.0	μAdc	–	–	–	–	–	4	–	–	–	4	–	–	–	–	–	–	9	8	1,16
		6	–	↓	–	–	↓	–	↓		–	–	–	–	–	6	–	–	–	6	–	–	–	–	–	–			
		7	–		–	–		–			–	–	–	–	–	7	–	–	–	7	–	–	–	–	–	–			
		13	–		-1.0	–		–			–	–	–	–	13	–	–	–	13	–	–	–	–	–	–	–			
	I_{inL}	10	0.5	–	0.5	–	–	0.3	–		–	10	–	–	–	–	–	–	–	–	–	–	–	–	–	–			
		11	↓	–	↓	–	–	↓	–		–	11	–	–	–	–	–	–	–	–	–	–	–	–	–	–			
		12	–	–	–	–	–	–	–		–	12	–	–	–	–	–	–	–	–	–	–	–	–	–	–			
Logic "1" Output Voltage	V_{OH}	2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	12	10,11	–	–	4	–	–	–	4	–	–	–	–	–	–	–	9	5,8	1,16
		3	↓	↓	↓	–	↓	↓	↓		↓	↓	–	–	6	–	–	–	6	–	–	–	–	–	–	–		5,8	1,16
		2				–							–	–	4	–	–	–	4	–	–	–	–	–	–	–		8	1,5,16
		3				–							–	–	6	–	–	–	6	–	–	–	–	–	–	–		8	1,5,16
Logic "0" Output Voltage	V_{OL}	2	-1.08	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	12	10,11	–	–	–	4	–	–	–	4	–	–	–	–	–	–	9	5,8	1,16
		3	↓	↓	↓	–	↓	↓	↓		↓	↓	–	–	–	6	–	–	–	6	–	–	–	–	–	–		5,8	1,16
		2				–							–	–	–	4	–	–	–	4	–	–	–	–	–	–		8	1,5,16
		3				–							–	–	–	6	–	–	–	6	–	–	–	–	–	–		8	1,5,16
Logic "1" Threshold Voltage	V_{OHA}	2 ④	-1.08	–	-0.980	–	–	-0.910	–	Vdc	11,12	–	–	10	4	–	–	–	4	–	–	–	–	–	–	–	9	5,8	1,16
		2	↓	–	↓	–	–	↓	–		–	10,11	12	–	4	–	–	–	4	–	–	–	–	–	–	–			
		2		–		–	–		–		10,12	–	–	11	4	–	–	–	4	–	–	–	–	–	–	–			
		2		–		–	–		–		12	10,11	–	–	–	–	–	–	–	–	4	–	–	–	–	–		8	
		2 ②		–		–	–		–		↓	↓	–	–	–	–	–	–	–	–	–	–	4	–	–	–		8	1,5,16
		2 ③		–		–	–		–				–	–	–	–	–	–	–	–	–	–	–	–	4	–		8	1,5,16
Logic "0" Threshold Voltage	V_{OLA}	2 ④	–	-1.655	–	–	-1.630	–	-1.595	Vdc	11,12	–	10	–	4	–	–	–	4	–	–	–	–	–	–	–	9	5,8	1,16
		2	↓	↓	↓	–	↓	↓	↓		–	10,11	–	12	4	–	–	–	4	–	–	–	–	–	–	–			
		2④				–					10,12	–	11	–	4	–	–	–	4	–	–	–	–	–	–	–			
		2				–					12	10,11	–	–	–	–	4	–	–	–	4	–	–	–	–	–		8	
		2 ②				–					↓	↓	–	–	–	–	–	–	–	–	–	–	4	–	–	–		8	1,5,16
		2 ③				–							–	–	–	–	–	–	–	–	–	–	–	–	4	–		8	1,5,16
Switching Times Propagation Delay											+1,11 V	+0.31 V	Pulse In	Pulse Out	+5.0 V	+2.40 V	Figure		+5.0 V	+2.40 V	Figure						+7.0 V	-3.2 V	+2.0 V
Data Input	t_{7+14+}	14	3.7	15	3.7	10.0	15	3.7	30	ns	12	10,11	7	14	–	–	1		–	–	1		–	–	–	–	9	5,8	1,16
	t_{7-14-}	14	3.7	15	3.7	10.0	15	3.7	40		12	10,11	7	14	–	–	1		–	–	1		–	–	–	–			
Clock Input	t_{11-14+}	14	2.7	11	2.7	5.0	9.0	2.7	11		12	10	7,11	14	–	–	4		–	–	4		–	–	–	–			
	t_{11-14-}	14	2.7	11	2.7	5.0	9.0	2.7	11		12	10	7,11	14	–	–	4		–	–	4		–	–	–	–			
Strobe Input	t_{12+14+}	14	1.6	8.0	1.6	4.0	7.0	1.6	8.0		–	10,11	12	14	7	–	2		7	–	2		–	–	–	–			
	t_{12-14-}	14	1.6	8.0	1.6	4.0	7.0	1.6	8.0		–	10,11	12	14	7	–	2		7	–	2		–	–	–	–			
Reset Input	t_{10+14-}	14	2.0	8.0	2.0	5.0	6.5	2.0	8.0		12	–	10,11	14	7	7	3		7	–	3		–	–	–	–			
Hysteresis Mode	t_{7+14+}	14	6.6	30	6.7	18.0	25	6.6	30		12	10,11	7	14	–	–	1		–	–	1		–	–	–	–		8	1,5,16
	t_{7-14-}	14	3.7	17	3.7	10.0	15	3.7	40		12	10,11	7	14	–	–	1		–	–	1		–	–	–	–		8	1,5,16
Setup Time	t_{setup}	14	30	–	2.5	15.0	–	30	–		12	10	7,11	14	–	–	5		–	–	5		–	–	–	–		5,8	1,16
Hold Time	t_{hold}	14	0	–	-2.0	15.0	–	-2.0	–		12	10	7,11	14	–	–	5		–	–	5		–	–	–	–			
Rise Time	t_+	14	1.5	5.0	1.5	2.0	4.3	1.5	5.0		12	10,11	7	14	–	–	1		–	–	1		–	–	–	–			
Fall Time	t_-	14	1.5	5.0	1.5	2.0	4.3	1.5	5.0		12	10,11	7	14	–	–	1		–	–	1		–	–	–	–			

*When testing choose either TTL or IBM Input Levels.

① Operation and limits shown also apply for V_{CC} = +6.0 V.

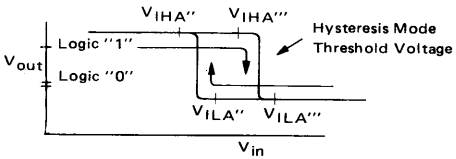
② Input level on data input taken from +0.4 V up to voltage level given.

③ Input level on data input taken from +4.0 V down to voltage level given.

④ Output latched to logic high state prior to test.

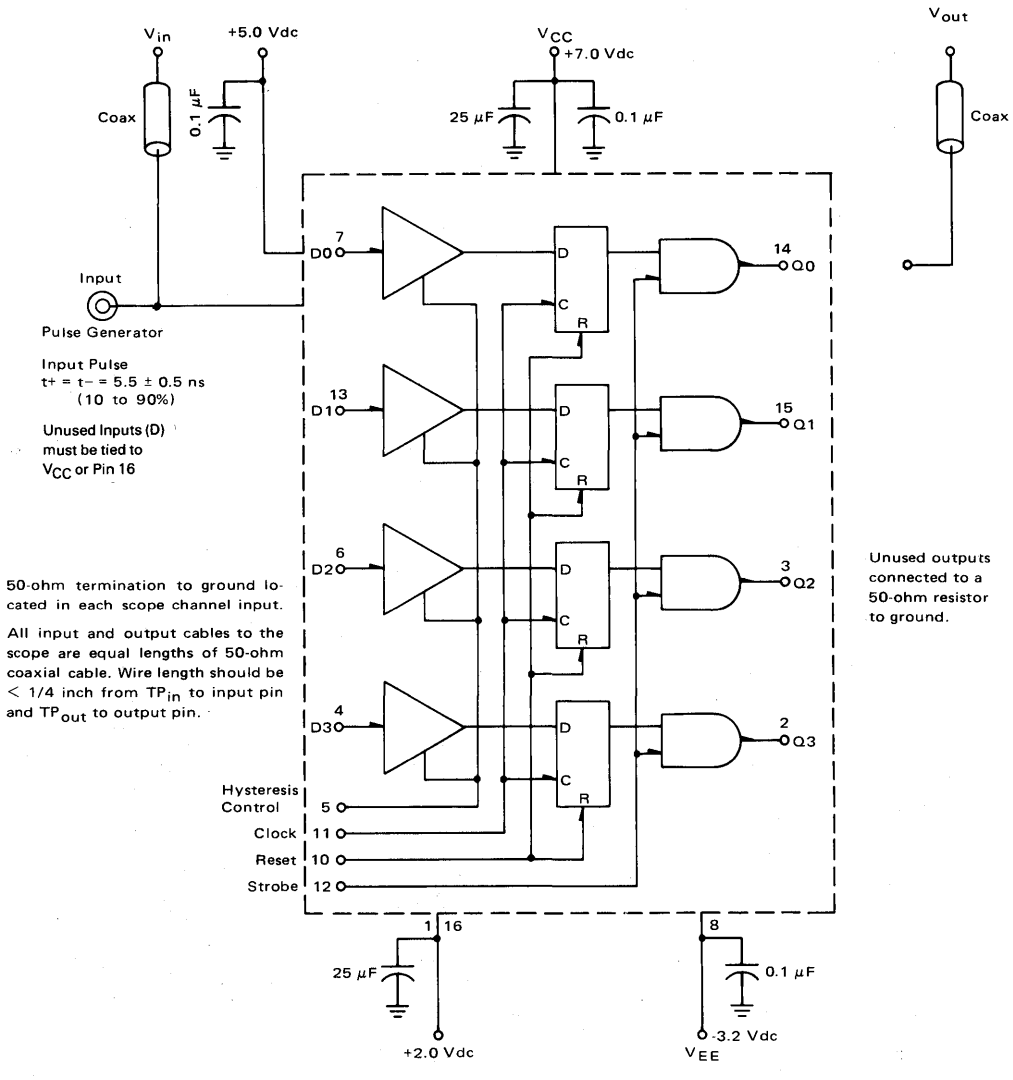
$V_{IHA'}$, $V_{ILA'}$ are standard logic "1" and logic "0" MTTL threshold voltages.
$V_{IHA''}$, $V_{ILA''}$, $V_{IHA'''}$ and $V_{ILA'''}$ are logic "1" and logic "0" threshold voltages in the hysteresis mode as shown in diagram.

⑤ Pin 5 to V_{EE}, V_{IL} to Data input one at a time



3

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C



NOTE: All power supplies and logic levels are shifted 2 volts positive.

FIGURE 1 – DATA to OUTPUT
(Clock and Reset are low, Strobe is high)

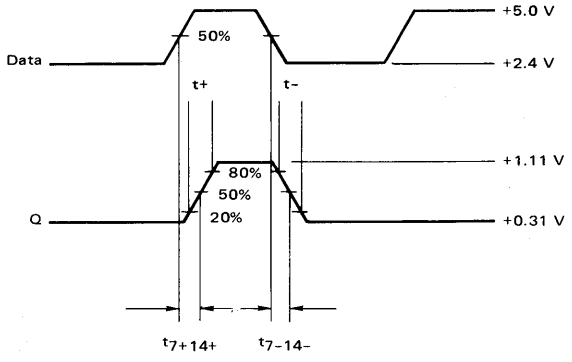


FIGURE 2 – STROBE to OUTPUT
(Data is high, Clock and Reset are low)

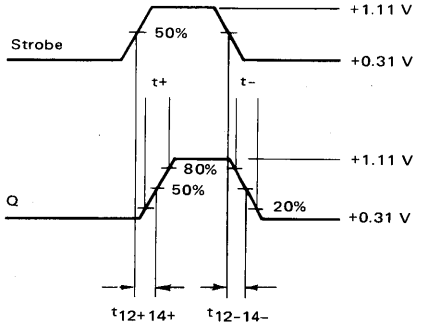


FIGURE 3 – RESET to OUTPUT
(Data and Strobe are high)

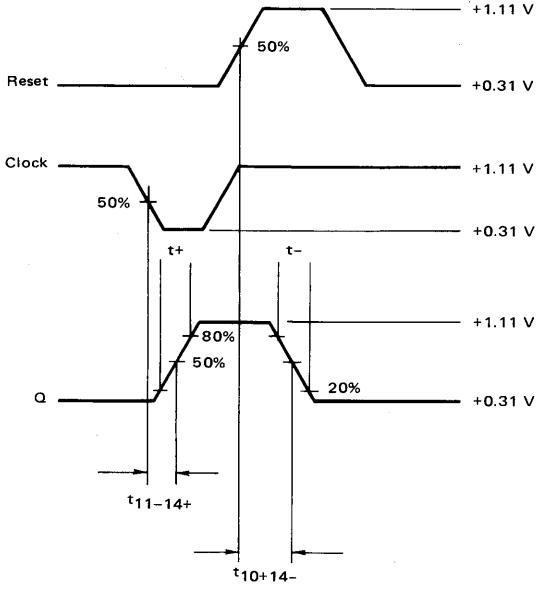


FIGURE 4 – CLOCK to OUTPUT
(Reset is low, Strobe is high)

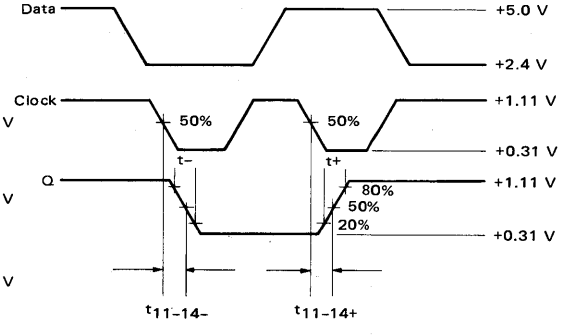
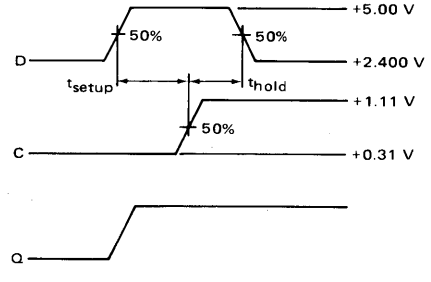


FIGURE 5 – $T_{SET\ UP}$ AND T_{HOLD} WAVEFORMS



MOTOROLA

MC10130

MECL 10K SERIES

DUAL LATCH

DUAL LATCH

The MC10130 is a clocked dual D type latch. Each latch may be clocked separately by holding the common clock in the low state, and using the clock enable inputs for the clocking function. If the common clock is to be used to clock the latch, the clock enable ($\overline{C}_E$) inputs must be in the low state. In this mode, the enable inputs perform the function of controlling the common clock ($\overline{C}$).

Any change at the D input will be reflected at the output while the clock is low. The outputs are latched on the positive transition of the clock. While the clock is in the high state, a change in the information present at the data inputs will not affect the output information.

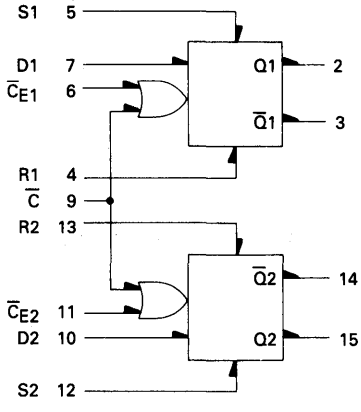
The set and reset inputs do not override the clock and D inputs. They are effective only when either $\overline{C}$ or $\overline{CE}$ or both are high.

P_D = 155 mW typ/pkg (No Load)
t_{pd} = 2.5 ns typ
t_r, t_f = 2.7 ns typ (20%–80%)

P SUFFIX
PLASTIC PACKAGE
CASE 648

L SUFFIX
CERAMIC PACKAGE
CASE 620

LOGIC DIAGRAM



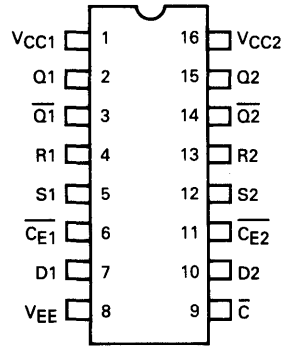
V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

TRUTH TABLE

D	$\overline{C}$	$\overline{CE}$	Q_{n+1}
L	L	L	L
H	L	L	H
ϕ	L	H	Q_n
ϕ	H	L	Q_n
ϕ	H	H	Q_n

ϕ = Don't Care

PIN ASSIGNMENT



ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown for only one latch. The other latch is tested in the same manner.

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
−30°C	−0.890	−1.890	−1.205	−1.500	−5.2
+25°C	−0.810	−1.850	−1.105	−1.475	−5.2
+85°C	−0.700	−1.825	−1.035	−1.440	−5.2

Characteristic	Symbol	Pin Under Test	MC10130 Test Limits −30°C Min	−30°C Max	+25°C Min	+25°C Typ	+85°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	38	–	30	35	–	38	mAdc	–	–	–	–	8	1,16
Input Current	I_{inH}	6,11	–	350	–	–	220	–	220	µAdc	6,11	–	–	–	8	1,16
		9	–	425	–	–	265	–	265		9	–	–	–		
		4,5,7	–	–	–	–	–	–	–		4,5	–	–	–		
		10,12,13	–	455	–	–	285	–	285		7,10,12,13	9	–	–		
	I_{inL}	4*	0.5	–	0.5	–	–	0.3	–	µAdc	–	4	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	5	–	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	4	–	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	2	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	9	7	–	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	9	–	–	8	1,16
Switching Times (50 Ω Load) (See Figure 1)											+1.11 V		Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{7+2+}	2	1.0	3.6	1.0	2.5	3.5	1.0	3.8	ns	–	–	7	2	8	1,16
	t_{5+2+}					2.7			3.9		6	–	5			
	t_{4+2-}					2.7			3.9		6	–	4			
	t_{6-2+}			4.3		–	4.0		4.1		–	–	6			
Rise Time (20% to 80%)	t_{2+}			3.6	1.1	2.7	3.5	1.1	3.8		–	–	7			
Fall Time (20% to 80%)	t_{2-}			3.6	1.1	2.7	3.5	1.1	3.8		–	–	7			
Setup Time	t_{setup}	2	2.5	–	2.5	–	–	2.5	–	ns	①	–	6,7	2	8	1,16
Hold Time	t_{hold}	2	1.5	–	1.5	–	–	1.5	–	ns	①	–	6,7	2	8	1,16

*All other inputs are tested in the same manner

MOTOROLA

MC10131

DUAL TYPE D MASTER-SLAVE FLIP-FLOP

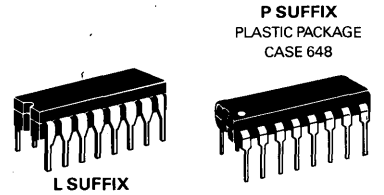
The MC10131 is a dual master-slave type D flip-flop. Asynchronous Set (S) and Reset (R) override Clock (C_C) and Clock Enable (C_E) inputs. Each flip-flop may be clocked separately by holding the common clock in the low state and using the enable inputs for the clocking function. If the common clock is to be used to clock the flip-flop, the Clock Enable inputs must be in the low state. In this case, the enable inputs perform the function of controlling the common clock.

The output states of the flip-flop change on the positive transition of the clock. A change in the information present at the data (D) input will not affect the output information at any other time due to master slave construction.

P_D = 235 mW typ/pkg (No Load)
f_{Tog} = 160 MHz typ
t_{pd} = 3.0 ns typ
t_r, t_f = 2.5 ns typ (20%–80%)

MECL 10K SERIES

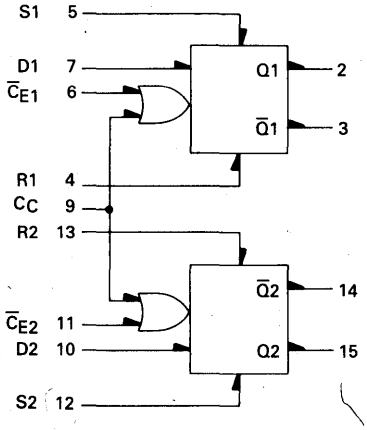
DUAL TYPE D MASTER-SLAVE FLIP-FLOP



P SUFFIX
PLASTIC PACKAGE
CASE 648

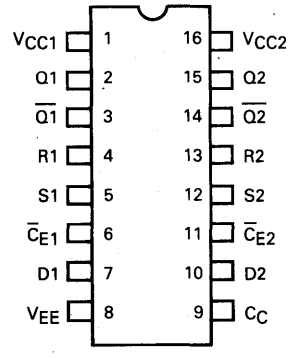
L SUFFIX
CERAMIC PACKAGE
CASE 620

LOGIC DIAGRAM



V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

PIN ASSIGNMENT



CLOCKED TRUTH TABLE

C	D	Q_{n+1}
L	ϕ	Q_n
H↑	L	L
H↑	H	H

ϕ = Don't Care
C = C_E + C_C.
A clock H is a clock transition from a low to a high state.

R-S TRUTH TABLE

R	S	Q_{n+1}
L	L	Q_n
L	H	H
H	L	L
H	H	N.D.

N.D. = Not Defined

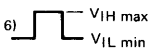
ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown for only one input, or for one set of input conditions. Other inputs tested in the same manner.

@ Test Temperature	TEST VOLTAGE VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}
−30°C	−0.890	−1.890	−1.205	−1.500	−5.2
+25°C	−0.810	−1.850	−1.105	−1.475	−5.2
+85°C	−0.700	−1.825	−1.035	−1.440	−5.2

Characteristic	Symbol	Pin Under Test	MC10131 Test Limits −30°C Min	−30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	VOLTAGE APPLIED TO PINS LISTED BELOW: $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	62	–	45	56	–	62	mAdc	–	–	–	–	8	1, 16
Input Current	I_{inH}	4	–	525	–	–	330	–	330	μAdc	4	–	–	–	8	1, 16
		5	–	525	–	–	330	–	330		5	–	–	–		
		6	–	350	–	–	220	–	220		6	–	–	–		
		7	–	390	–	–	245	–	245		7	–	–	–		
		9	–	425	–	–	265	–	265		9	–	–	–		
Input Leakage Current	I_{inL}	4,5,*	0.5	–	0.5	–	–	0.3	–	μAdc	–	*	–	–	8	1, 16
		6,7,9*	0.5	–	0.5	–	–	0.3	–	μAdc	–	*	–	–	8	1, 16
Logic "1" Output Voltage	V_{OH}	2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	5	–	–	–	8	1, 16
		2†	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	7	–	–	–	8	1, 16
Logic "0" Output Voltage	V_{OL}	3	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	5	–	–	–	8	1, 16
		3†	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	7	–	–	–	8	1, 16
Logic "1" Threshold Voltage	V_{OHA}	2	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	5	–	8	1, 16
		2†	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	7	9	8	1, 16
Logic "0" Threshold Voltage	V_{OLA}	3	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	5	–	8	1, 16
		3†	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	7	9	8	1, 16
Switching Times Clock Input											+1.11 Vdc		Pulse In	Pulse Out	−3.2 Vdc	+2.0 Vdc
Propagation Delay	t_{9+2-}	2	1.7	4.6	1.8	3.0	4.5	1.8	5.0	ns	–	–	9	2	8	1, 16
	t_{9+2+}	2									7	–	9	2		
	t_{6+2+}	2									7	–	6	2		
	t_{6+2-}	2									–	–	6	2		
Rise Time (20 to 80%)	t_{2+}	2	1.0		1.1	2.5		1.1	4.9		7	–	9	2		
Fall Time (20 to 80%)	t_{2-}	2	1.0		1.1	2.5		1.1	4.9		–	–	9	2		
Set Input Propagation Delay	t_{5+2+}	2	1.7	4.4	1.8	2.8	4.3	1.8	4.8	ns	–	–	5	2	8	1, 16
	t_{12+15+}	15									6	–	12	15		
	t_{5+3-}	3									–	–	5	3		
	t_{12+14-}	14									9	–	12	14		
Reset Input Propagation Delay	t_{4+2-}	2	1.7	4.4	1.8	2.8	4.3	1.8	4.8	ns	–	–	4	2	8	1, 16
	t_{13+15-}	15									6	–	13	15		
	t_{4+3-}	3									–	–	4	3		
	t_{13+14+}	14									9	–	13	14		
Setup Time	t_{setup}	7	2.5	–	2.5	–	–	2.5	–	ns	–	–	6,7	2	8	1, 16
Hold Time	t_{hold}	7	1.5	–	1.5	–	–	1.5	–	ns	–	–	6,7	2	8	1, 16
Toggle Frequency (Max)	f_{Tog}	2	125	–	125	160	–	125	–	MHz	–	–	6	2	8	1, 16

*Individually test each input; apply $V_{IL\ min}$ to pin under test.

†Output level to be measured after a clock pulse has been applied to the $\overline{C}_E$ input (pin 6) 

MOTOROLA

MC10132

DUAL MULTIPLEXER WITH LATCH AND COMMON RESET

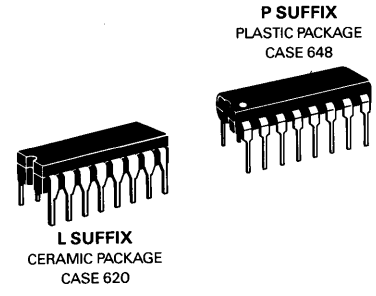
The MC10132 is a dual multiplexer with clocked D type latches. It incorporates common data select and reset inputs. Each latch may be clocked separately by holding the common clock in the low state, and using the clock enable inputs for a clocking function. If the common clock is to be used to clock the latch, the clock enable ($\overline{CE}$) inputs must be in the low state. In this mode, the enable inputs perform the function of controlling the common clock (C_C).

The data select (A) input determines which data input is enabled. A high (H) level enables data inputs D12 and D22 and a low (L) level enables data inputs D11 and D21. Any change on the data input will be reflected at the outputs while the clock is low. The outputs are latched on the positive transition of the clock. While the clock is in the high state, a change in the information present at the data inputs will not affect the output information. The reset input is enabled when the clock is in the high state, and disabled when the clock is low.

P_D = 225 mW typ/pkg (No Load)
t_{pd} = 3.0 ns typ
t_r, t_f = 2.5 ns typ (20%–80%)

MECL 10K SERIES

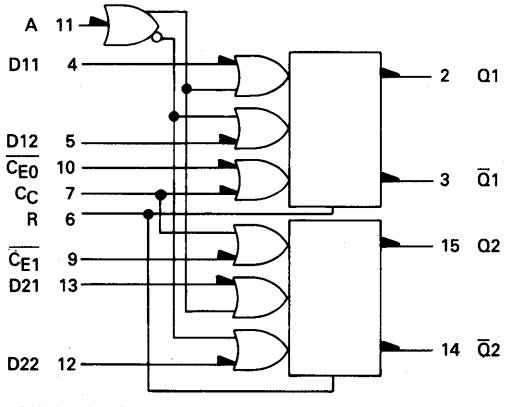
DUAL MULTIPLEXER WITH LATCH AND COMMON RESET



P SUFFIX
PLASTIC PACKAGE
CASE 648

L SUFFIX
CERAMIC PACKAGE
CASE 620

LOGIC DIAGRAM



TRUTH TABLE

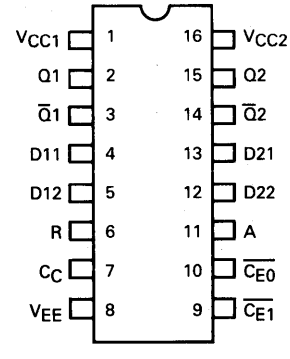
R	D	C_C	$\overline{CE}$	Q_{n+1}
ϕ	L	L	L	L
L	L	L	H	Q_n
L	L	H	L	Q_n
L	L	H	H	Q_n
ϕ	H	L	L	H
L	H	L	H	Q_n
L	H	H	L	Q_n
L	H	H	H	Q_n
H	ϕ	ϕ	H	L

ϕ = Don't Care

$D = (\overline{A} \bullet D11) + (A \bullet D12)$

V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

PIN ASSIGNMENT



ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown for only one latch. The outer latches are tested in the same manner.

@ Test Temperature	TEST VOLTAGE VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10132 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}	(V_{CC}) Gnd
Power Supply Current	I_E	8	–	60	–	44	55	–	60	mAdc	–	–	–	–	8	1,16
Input Current	$I_{in\ H}$	4	–	460	–	–	290	–	290	μAdc	4	–	–	–	8	1,16
		5	–	460	–	–	290	–	290		5	–	–	–		
		6	–	620	–	–	390	–	390		6	–	–	–		
		7	–	460	–	–	290	–	290		7	–	–	–		
		10	–	425	–	–	265	–	265		10	–	–	–		
		11	–	425	–	–	265	–	265		11	–	–	–		
	$I_{in\ L}$	4*	0.5	–	0.5	–	–	0.3	–	μAdc	–	4	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	4	7,9,10	–	–	8	1,16
		2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	5,11	7,9,10	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	3	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	4	7,9,10	–	–	8	1,16
		3	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	5,11	7,9,10	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	2	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	7,9,10	4	–	8	1,16
		2	-1.080	–	-0.980	–	–	-0.910	–	Vdc	11	7,9,10	5	–	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	3	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	7,9,10	4	–	8	1,16
		3	–	-1.655	–	–	-1.630	–	-1.595	Vdc	11	7,9,10	5	–	8	1,16
Switching Times (50-ohm load)											+1.11 V	+0.31 V	Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay Data	t_{4+2+}	2	1.0	3.6	1.0	–	3.3	1.0	3.7	ns	–	7,9,10	4	2	8	1,16
Reset	t_{6+2-}			4.0	1.0	–	3.8		4.2		7	–	6			
Clock	t_{7-2+}			6.0	1.0	–	5.7		6.3		4	–	7			
Select	t_{11+2+}			4.8	1.0	–	4.6		5.0		5	7	11			
Setup Time Data	t_{setup}	2	2.5	–	2.5	–	–	2.5	–	ns	–	11	4,10	2	8	1,16
Select	t_{setup}	2	3.5	–	3.5	–	–	3.5	–	ns	5	7	10,11	2	8	1,16
Hold Time Data	t_{hold}	2	1.5	–	1.5	–	–	1.5	–	ns	–	11	4,10	2	8	1,16
Select	t_{hold}	2	1.0	–	1.0	–	–	1.0	–	ns	5	7	10,11	2	8	1,16
Rise Time (20% to 80%)	t_{2+}	2	1.5	3.7	1.5	–	3.5	1.5	3.8	ns	–	7,9,10	4	2	8	1,16
Fall Time (20% to 80%)	t_{2-}	2	1.5	3.7	1.5	–	3.5	1.5	3.8	ns	–	7,9,10	4	2	8	1,16

*All other inputs tested in the same manner.

MOTOROLA

MC10133

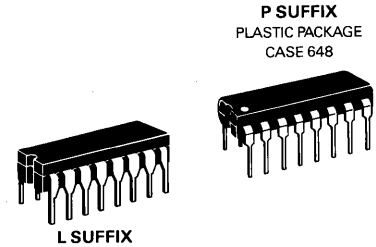
MECL 10K SERIES

QUAD LATCH

The MC10133 is a high speed, low power, quad latch consisting of four bistable latch circuits with D type inputs and gated Q outputs, allowing direct wiring to a bus. When the clock is high, outputs will follow D inputs. Information is latched on the negative going transition of the clock.

The outputs are gated when the output enable ($\overline{G}$) is low. All four latches may be clocked at one time with the common clock (C_C), or each half may be clocked separately with its clock enable ($\overline{CE}$).

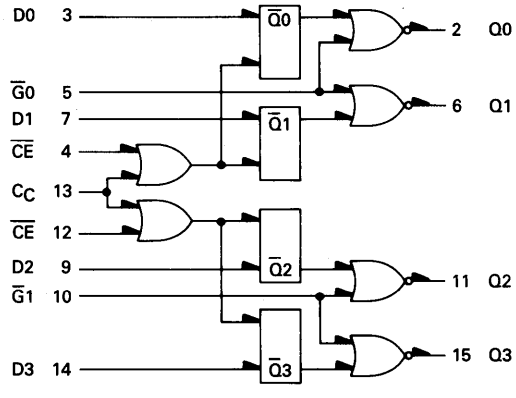
P_D = 310 mW typ/pkg (No Load)
t_{pd} = 4.0 ns typ
t_r, t_f = 2.0 ns typ (20%–80%)



P SUFFIX
PLASTIC PACKAGE
CASE 648

L SUFFIX
CERAMIC PACKAGE
CASE 620

LOGIC DIAGRAM



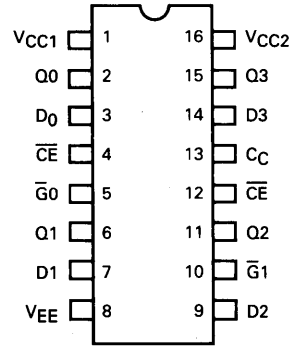
TRUTH TABLE

$\overline{G}$	C	D	Q_{n+1}
H	ϕ	ϕ	L
L	L	ϕ	Q_n
L	H	L	L
L	H	H	H

ϕ = Don't Care
C = C_C + CE

V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

PIN ASSIGNMENT



ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10133 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	82	–	–	75	–	82	mAdc	–	13	–	–	8	1,16
Input Current	I_{inH}	3	–	390	–	–	245	–	245	μAdc	3	–	–	–	8	1,16
		4	–	425	–	–	265	–	265		4	–	–	–		
		5	–	560	–	–	350	–	350		5	–	–	–		
		13	–	560	–	–	350	–	350		13	–	–	–		
	I_{inL}	3	0.5	–	0.5	–	–	0.3	–	μAdc	–	3	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	3,4	–	–	–	8	1,16
		2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	3,13	–	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	13	3	–	–	8	1,16
		2				–					3,5,13	–	–	–		
		2				–					4	3	–	–		
Logic "1" Threshold Voltage	V_{OHA}	2	-1.080	–	-0.980	–	–	-0.910	–	Vdc	3,4	–	–	5	8	1,16
		2		–		–	–		–		4	–	3	–		
		2		–		–	–		–		3,4	–	–	–		
		2†		–		–	–		–		3	–	–	–		
		2††		–		–	–		–		–	–	–	–		
		2††		–		–	–		–		–	–	–	4		
		2		–		–	–		–		3	–	4	–		
		2		–		–	–		–		3	–	13	–		
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.655	–	–	-1.630	–	-1.595	Vdc	3,4	–	5	–	8	1,16
		2	–		–	–		–			4	–	–	3		
		2	–		–	–		–			4	–	–	–		
		2†	–		–	–		–			–	–	–	–		
		2††	–		–	–		–			3	–	–	–		
		2††	–		–	–		–			3	–	–	13		
Switching Times (50 Ω Load)											+1.11 V		Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{3+2+}	2	1.0	5.6	1.0	4.0	5.4	1.1	5.9	ns	4	–	3	2	8	1,16
	t_{4+2+}	2		5.4		4.0	5.4	1.2	6.0		3 *	–	4	2		
	t_{5-2+}	2		3.2		2.0	3.1	1.0	3.4		–	–	5	2		
	t_{Setup}	3	2.5	–	2.5	0.7	–	2.5	–		–	–	3	2		
	t_{Hold}	3	1.5	–	1.5	0.7	–	1.5	–		–	–	3	2		
Rise Time (20% to 80%)	t_{2+}	2	1.0	3.6	1.1	2.0	3.5	1.1	3.8		4	–	3	2		
Fall Time (20% to 80%)	t_{2-}	2	1.0	3.6	1.1	2.0	3.5	1.1	3.8		4	–	3	2		

†Output level to be measured after a clock pulse has been applied to the clock input (Pin 4).

††Data input at proper high/low level while clock pulse is high so that device latches at proper high/low level for test. Levels are measured after device has latched.

V_{IH} max
V_{IL} min

*Latch set to zero state before test.

MOTOROLA

MC10134

DUAL MULTIPLEXER WITH LATCH

The MC10134 is a dual multiplexer with clocked D type latches. Each latch may be clocked separately by holding the common clock in the low state, and using the clock enable inputs for the clocking function. If the common clock is to be used to clock the latch, the clock enable ($\overline{CE}$) inputs must be in the low state. In this mode, the enable inputs perform the function of controlling the common clock (C_C).

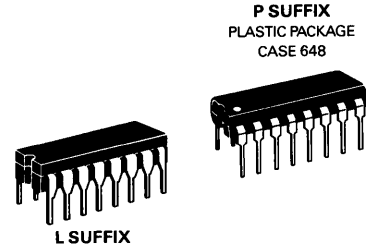
The data select inputs determine which data input is enabled. A high (H) level on the A0 input enables data input D12 and a low (L) level on the A0 input enables data input D11. A high (H) level on the A1 input enables data input D22 and a low (L) level on the A1 input enables data input D21.

Any change on the data input will be reflected at the outputs while the clock is low. The outputs are latched on the positive transition of the clock. While the clock is in the high state, a change in the information present at the data inputs will not affect the output information.

P_D = 225 mW typ/pkg (No Load)
t_{pd} = 3.0 ns typ
t_r, t_f = 2.5 ns typ (20%–80%)

MECL 10K SERIES

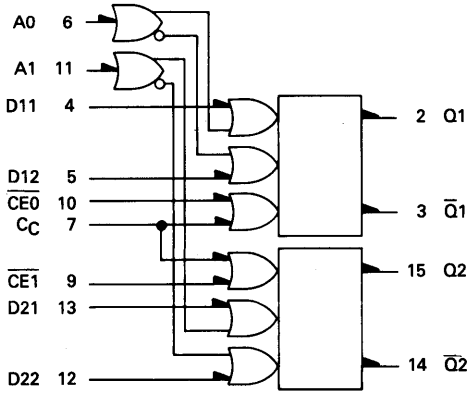
DUAL MULTIPLEXER WITH LATCH



P SUFFIX
PLASTIC PACKAGE
CASE 648

L SUFFIX
CERAMIC PACKAGE
CASE 620

LOGIC DIAGRAM



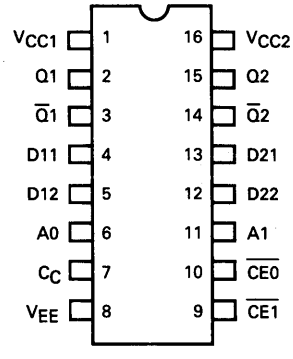
TRUTH TABLE

C	A0	D11	D12	Q_{n+1}
L	L	L	ϕ	L
L	L	H	ϕ	H
L	H	ϕ	L	L
L	H	ϕ	H	H
H	ϕ	ϕ	ϕ	Q_n

ϕ = Don't Care
C = $\overline{CE}$ + C_C

V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

PIN ASSIGNMENT



ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown for only one latch. The other latches are tested in the same manner.

@ Test Temperature	TEST VOLTAGE VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.625	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10134 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	60	–	55	–	60	mAdc	–	–	–	–	8	1,16
Input Current	$I_{in\ H}$	4	–	460	–	290	–	290	μAdc	4	–	–	–	8	1,16
		5	–	460	–	290	–	290		5	–	–	–		
		6	–	425	–	265	–	265		6	–	–	–		
		7	–	460	–	290	–	290		7	–	–	–		
		10	–	425	–	265	–	265		10	–	–	–		
	$I_{in\ L}$	4*	0.5	–	0.5	–	0.3	–	μAdc	–	4	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	2	-1.060	-0.890	-0.960	-0.810	-0.890	-0.700	Vdc	4	6,7,10,	–	–	8	1,16
		2	-1.060	-0.890	-0.960	-0.810	-0.890	-0.700	Vdc	5,6	7,10	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.675	-1.850	-1.650	-1.825	-1.615	Vdc	–	4,6,7,10,	–	–	8	1,16
		2	-1.890	-1.675	-1.850	-1.650	-1.825	-1.615	Vdc	6	5,7,10	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	2	-1.080	–	-0.980	–	-0.910	–	Vdc	–	6,7,10	4	–	8	1,16
		2	-1.080	–	-0.980	–	-0.910	–	Vdc	6	7,10	5	–	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.655	–	-1.630	–	-1.595	Vdc	–	6,7,10	–	4	8	1,16
		2	–	-1.655	–	-1.630	–	-1.595	Vdc	6	7,10	–	5	8	1,16
Switching Times (50-ohm load)										+1.11 V	+0.31 V	Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay Data	t_{4+2+}	2	1.0	3.5	1.0	3.3	1.0	3.6	ns	–	6,7,10	4	2	8	1,16
Clock	t_{10-2+}		1.0	6.0	1.0	5.7	1.0	6.3		4	7	10			
Select	t_{6+2+}		1.0	4.8	1.0	4.6	1.0	5.0		5	7,10	6			
Setup Time Data	t_{setup}	2	2.5	–	2.5	–	2.5	–	ns	–	6,7	4,10	2	8	1,16
Select	t_{setup}	2	3.5	–	3.5	–	3.5	–	ns	5	7,11	6,10	2	8	1,16
Hold Time Data	t_{hold}	2	1.5	–	1.5	–	1.5	–	ns	–	6,7	4,10	2	8	1,16
Select	t_{hold}	2	1.0	–	1.0	–	1.0	–	ns	5	7,11	6,10	2	8	1,16
Rise Time (20% to 80%)	t_{2+}	2	1.5	3.7	1.5	3.5	1.5	3.8	ns	–	6,7,10	4	2	8	1,16
Fall Time (20% to 80%)	t_{2-}	2	1.5	3.7	1.5	3.5	1.5	3.8	ns	–	6,7,10	4	2	8	1,16

*All other inputs tested in the same manner.

MOTOROLA

MC10135

MECL 10K SERIES

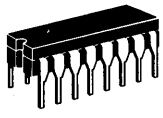
DUAL J-K MASTER-SLAVE FLIP-FLOP

The MC10135 is a dual master-slave dc coupled J-K flip-flop. Asynchronous set (S) and reset (R) are provided. The set and reset inputs override the clock.

A common clock is provided with separate $\overline{J}$-$\overline{K}$ inputs. When the clock is static, the $\overline{J}$-$\overline{K}$ inputs do not effect the output.

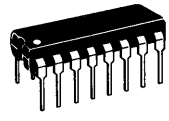
The output states of the flip-flop change on the positive transition of the clock.

P_D = 280 mW typ/pkg (No Load)
f_{Tog} = 140 MHz typ
t_{pd} = 3.0 ns typ
t_r, t_f = 2.5 ns typ (20%–80%)

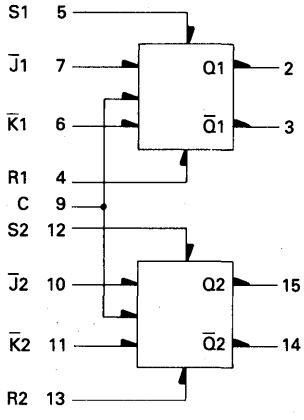


L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

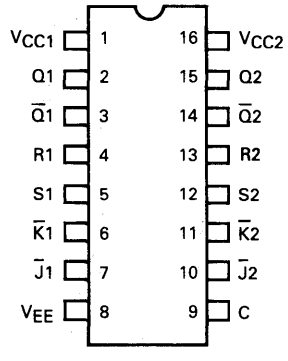


LOGIC DIAGRAM



V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

PIN ASSIGNMENT



R-S TRUTH TABLE

R	S	Q_{n+1}
L	L	Q_n
L	H	H
H	L	L
H	H	N.D.

N.D. = Not Defined

CLOCK J-K TRUTH TABLE*

$\overline{J}$	$\overline{K}$	Q_{n+1}
L	L	$\overline{Q_n}$
H	L	L
L	H	H
H	H	Q_n

*Output states change on positive transition of clock for $\overline{J}$-$\overline{K}$ input condition present.

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established in an ambient temperature of 25°C, while the circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown for only one input, or for one set of input conditions. Other inputs tested in the same manner.

@ Test Temperature	TEST VOLTAGE VALUES (Vdc ± 1%) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10135 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	VOLTAGE APPLIED TO PINS LISTED BELOW: $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	--	75	--	54	68	--	75	mAdc	--	--	--	--	8	1,16
Input Current	$I_{in\ H}$	6,7,9,10,11	--	425	--	--	265	--	265	µAdc	①	--	--	--	8	1,16
		4,5,12,13	--	620	--	--	390	--	390	µAdc	①	--	--	--	8	1,16
Input Leakage Current	$I_{in\ L}$	4,5,6,7,9,	0.5	--	0.5	--	--	0.3	--	µAdc	--	②	--	--	8	1,16
		10,11,12,13	0.5	--	0.5	--	--	0.3	--	µAdc	--	②	--	--	8	1,16
Logic "1" Output Voltage	V_{OH}	2	-1.060	-0.890	-0.960	--	-0.810	-0.890	-0.700	Vdc	5	--	--	--	8	1,16
		2 ③	-1.060	-0.890	-0.960	--	-0.810	-0.890	-0.700	Vdc	6	--	--	--	8	1,16
Logic "0" Output Voltage	V_{OL}	3	-1.890	-1.675	-1.850	--	-1.650	-1.825	-1.615	Vdc	5	--	--	--	8	1,16
		3 ③	-1.890	-1.675	-1.850	--	-1.650	-1.825	-1.615	Vdc	6	--	--	--	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	2	-1.080	--	-0.980	--	--	-0.910	--	Vdc	--	--	5	--	8	1,16
		2 ④	-1.080	--	-0.980	--	--	-0.910	--	Vdc	6	--	--	--	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	3	--	-1.655	--	--	-1.630	--	-1.595	Vdc	--	--	5	--	8	1,16
		3 ④	--	-1.655	--	--	-1.630	--	-1.595	Vdc	6	--	--	--	8	1,16
Switching Times													**Pulse In**	**Pulse Out**	**-3.2 Vdc**	**+2.0 Vdc**
Clock Input																
Propagation Delay	t_{g+2+}	2	1.8	5.0	1.8	3.0	4.5	1.8	4.6	ns	--	--	9	2	8	1,16
	t_{g+2-}	2	1.8	5.0	1.8	3.0	↓	1.8	4.6	↓	--	--	9	2	↓	↓
Rise Time (20 to 80%)	$t_{2+,3+}$	2,3	1.1	4.8	1.1	2.0	↓	1.1	4.7	↓	--	--	9	2,3	↓	↓
Fall Time (20 to 80%)	$t_{2-,3-}$	2,3	1.1	4.8	1.1	2.0	↓	1.1	4.7	↓	--	--	9	2,3	↓	↓
Set Input																
Propagation Delay	t_{5+2+}	2	1.8	5.6	1.8	3.0	5.0	1.8	5.2	ns	--	--	5	2	8	1,16
	t_{12+15+}	15	↓	↓	↓	↓	↓	--	↓	↓	--	--	12	15	↓	↓
	t_{5+3-}	3	↓	↓	↓	↓	↓	--	↓	↓	--	--	5	3	↓	↓
	t_{12+14-}	14	↓	↓	↓	↓	↓	--	↓	↓	--	--	12	14	↓	↓
Reset Input																
Propagation Delay	t_{4+2-}	2	1.8	5.6	1.8	3.0	5.0	1.8	5.2	ns	--	--	4	2	8	1,16
	t_{4+3+}	3	↓	↓	↓	↓	↓	↓	↓	↓	--	--	4	3	↓	↓
	t_{13+15-}	15	↓	↓	↓	↓	↓	↓	↓	↓	--	--	13	15	↓	↓
	t_{13+14+}	14	↓	↓	↓	↓	↓	↓	↓	↓	--	--	13	14	↓	↓
Setup Time	t_{setup}	7	2.5	--	2.5	1.0	--	2.5	--	ns	--	--	6,9 ⑤	2	8	1,16
Hold Time	t_{hold}	7	1.5	--	1.5	1.0	--	1.5	--	ns	--	--	6,9 ⑤	2	8	1,16
Toggle Frequency	f_{Tog}	2	125	--	125	140	--	125	--	MHz	--	--	9	2	9	1,16

NOTES:

① Individually test each input; apply $V_{IH\ max}$ to pin under test.

② Individually test each input; apply $V_{IL\ min}$ to pin under test.

③ Output level to be measured after a clock pulse has been applied to the C input (pin 9)

④ Output level to be measured after a clock pulse has been applied to the C input (pin 9)

⑤ See Figure 2 for timing test diagram.

MOTOROLA

MC10136

UNIVERSAL HEXADECIMAL COUNTER

The MC10136 is a high speed synchronous counter that can count up, count down, preset, or stop count at frequencies exceeding 100 MHz. The flexibility of this device allows the designer to use one basic counter for most applications, and the synchronous count feature makes the MC10136 suitable for either computers or instrumentation.

Three control lines (S1, S2, and $\overline{\text{Carry In}}$) determine the operation mode of the counter. Lines S1 and S2 determine one of four operations; preset (program), increment (count up), decrement (count down), or hold (stop count). Note that in the preset mode a clock pulse is necessary to load the counter, and the information present on the data inputs (D0, D1, D2, and D3) will be entered into the counter. $\overline{\text{Carry Out}}$ goes low on the terminal count, or when the counter is being preset.

This device is not designed for use with gated clocks. Control is via S1 and S2.

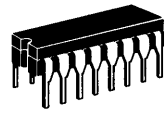
P_D = 625 mW typ/pkg (No Load)
f_{count} = 150 MHz typ
t_{pd} = 3.3 ns typ (C-Q)
7.0 ns typ (C-C_{out})
5.0 ns typ (C_{in}-C_{out})

FUNCTION SELECT TABLE

S1	S2	Operating Mode
L	L	Preset (Program)
L	H	Increment (Count Up)
H	L	Decrement (Count Down)
H	H	Hold (Stop Count)

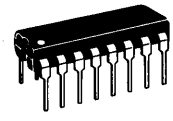
MECL 10K SERIES

UNIVERSAL HEXADECIMAL COUNTER

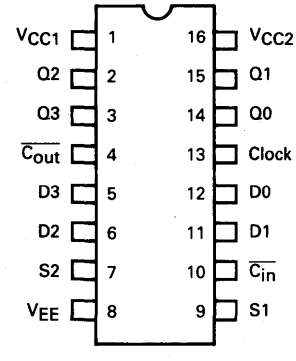


L SUFFIX
CERAMIC PACKAGE
CASE 620

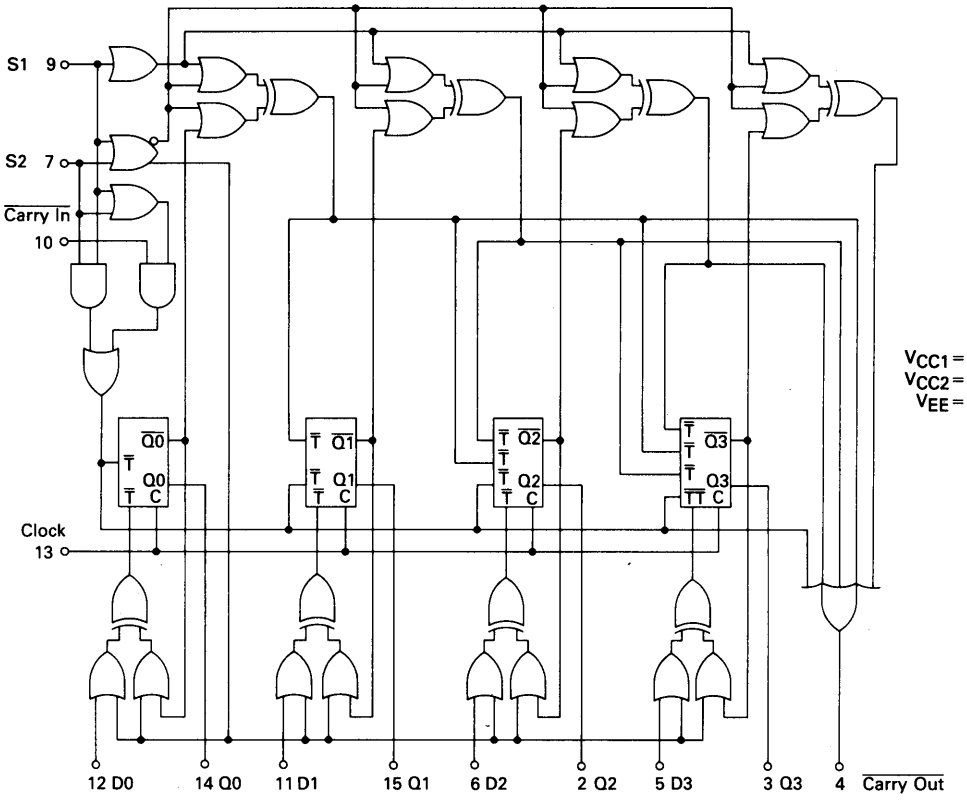
P SUFFIX
PLASTIC PACKAGE
CASE 648



PIN ASSIGNMENT



LOGIC DIAGRAM



SEQUENTIAL TRUTH TABLE*

INPUTS								OUTPUTS				
S1	S2	D0	D1	D2	D3	Carry In	Clock **	Q0	Q1	Q2	Q3	Carry Out
L	L	L	L	H	H	ϕ	H	L	L	H	H	L
L	H	ϕ	ϕ	ϕ	ϕ	L	H	H	L	H	H	H
L	H	ϕ	ϕ	ϕ	ϕ	L	H	L	H	H	H	H
L	H	ϕ	ϕ	ϕ	ϕ	L	H	H	H	H	H	L
L	H	ϕ	ϕ	ϕ	ϕ	H	L	H	H	H	H	H
L	H	ϕ	ϕ	ϕ	ϕ	H	H	H	H	H	H	H
H	H	ϕ	ϕ	ϕ	ϕ	ϕ	H	H	H	H	H	H
L	L	H	H	L	L	ϕ	H	H	H	L	L	L
H	L	ϕ	ϕ	ϕ	ϕ	L	H	L	H	L	L	H
H	L	ϕ	ϕ	ϕ	ϕ	L	H	H	L	L	L	H
H	L	ϕ	ϕ	ϕ	ϕ	L	H	L	L	L	L	L
H	L	ϕ	ϕ	ϕ	ϕ	L	H	H	H	H	H	H

ϕ = Don't care.
* Truth table shows logic states assuming inputs vary in sequence shown from top to bottom.
** A clock H is defined as a clock input transition from a low to a high logic level.

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Test procedures are shown for only one output. The other outputs are tested in the same manner.

@ Test Temperature	TEST VOLTAGE VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ max}$	$V_{ILA\ max}$	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10136 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ max}$	$V_{ILA\ max}$	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	138	–	125	150	–	138	mAdc	–	–	–	–	8	1, 16
Input Current	$I_{in\ H}$	5,6,11,12	–	350	–	–	220	–	220	μAdc	5,6,11,12	–	–	–	8	1, 16
		7	–	425	–	–	265	–	265		7	–	–	–		
		9,10	–	390	–	–	245	–	245		9,10	–	–	–		
		13	–	460	–	–	290	–	290		13	–	–	–		
	$I_{in\ L}$	All	0.5	–	0.5	–	–	0.3	–	μAdc	–	①	–	–	8	1, 16
Logic "1" Output Voltage	V_{OH}	14 ②	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	12	7, 9	–	–	8	1, 16
Logic "0" Output Voltage 10136	V_{OL}	14 ②	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	–	7, 9	–	–	8	1, 16
Logic "1" Threshold Voltage	V_{OHA}	14 ②	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	7, 9	12	–	8	1, 16
Logic "0" Threshold Voltage	V_{OLA}	14 ②	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	7, 9	–	12	8	1, 16
Switching Times (50-ohm Load)											+1.11 V	+0.31 V	Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay																
Clock Input	t_{13+14+}	14	0.8	4.8	1.0	3.3	4.5	1.4	5.0	ns	12	–	13	14	8	1, 16
	t_{13+14-}	14	0.8	4.8	1.0	3.3	4.5	1.4	5.0		–	–		14		
	t_{13+4+}	4	2.0	10.9	2.5	7.0	10.5	2.4	11.5		7	–		4		
	t_{13+4-}	4	2.0	10.9	2.5	7.0	10.5	2.4	11.5		7	–		4		
$\overline{\text{Carry In}}$ To $\overline{\text{Carry Out}}$	t_{10-4-}	4 ③	1.6	7.4	1.6	5.0	6.9	1.9	7.5		7	13	10	4		
	t_{10+4+}	4	1.6	7.4	1.6	5.0	6.9	1.9	7.5		7	13	10	4		
Set Up Time																
Data Inputs	t_{12+13+}	14	3.5	–	3.5	–	–	3.5	–		–	7, 9	12, 13	14		
	t_{12-13+}	14	3.5	–	3.5	–	–	3.5	–		–	7, 9	12, 13			
Select Inputs	t_{9+13+}	14	6.0	–	6.0	–	–	6.0	–		–	–	9, 13			
	t_{7+13+}	14	6.0	–	6.0	–	–	6.0	–		–	–	7, 13			
$\overline{\text{Carry In}}$ Input	t_{10-13+}	14	2.5	–	2.5	–	–	3.0	–		7	9	10, 13	14		
	t_{13+10+}	14	0	–	0	–	–	0	–		7	–	10, 13	14		
Hold Time																
Data Inputs	t_{13+12+}	14	0	–	0	–	–	0	–		–	7, 9	12, 13	14		
	t_{13+12-}	14	0	–	0	–	–	0	–		–	7, 9	12, 13			
Select Inputs	t_{13+9+}	14	-1	–	-1.0	–	–	-1	–		–	–	9, 13			
	t_{13+7+}	14	-1	–	-1.0	–	–	-1	–		–	–	7, 13			
$\overline{\text{Carry In}}$ Input	t_{13+10-}	14	0	–	0	–	–	0	–		7	9	10, 13			
	t_{10+13+}	14	1.5	–	1.5	–	–	1.5	–		7	9	10, 13			
Counting Frequency	$f_{countup}$	14	125	–	125	150	–	125	–	MHz	7	–	13			
	$f_{countdown}$	14	125	–	125	150	–	125	–	MHz	9	–				
Rise Time (20% to 80%)	t_{4+}	4	0.9	3.3	1.1	2.0	3.3	1.1	3.5	ns	7	–		4		
	t_{14+}	14				2.0						–		14		
Fall Time (20% to 80%)	t_{4-}	4				2.0						–		4		
	t_{14-}	14				2.0						–		14		

① Individually apply $V_{IL\ min}$ to pin under test. ② Measure output after clock pulse V_{IL} ⌐ V_{IH} appears at clock input (pin 13)

③ Before test set all Q outputs to a logic high.

To preserve reliable performance, the MC10136 (plastic-packaged device only) is to be operated in ambient temperatures above 70°C only when 500 lfpm blown air or equivalent heat sinking is provided.

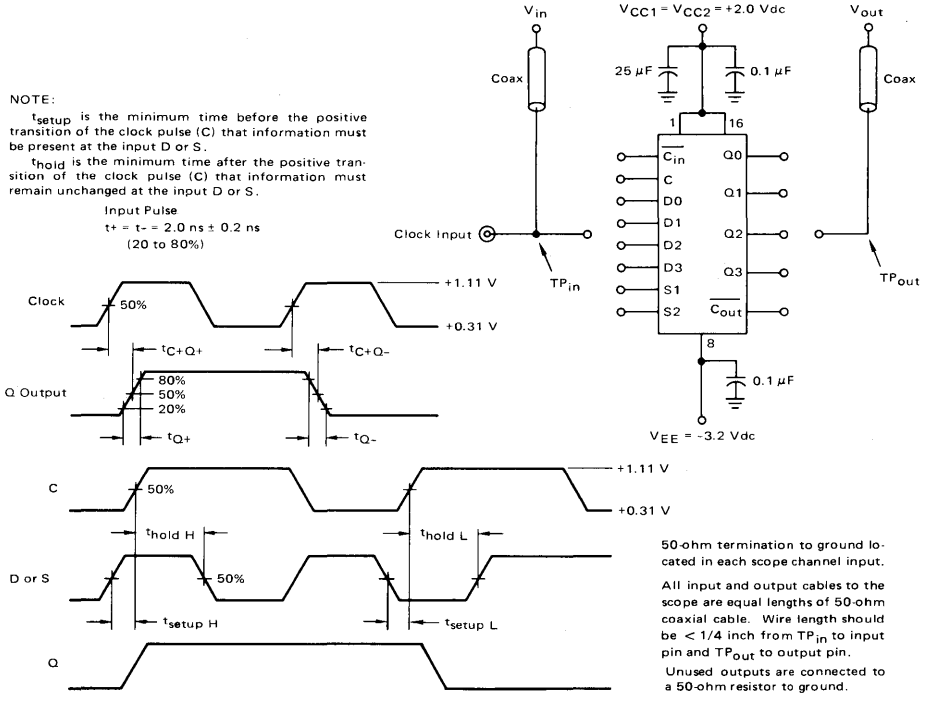
SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C

NOTE:

t_{setup} is the minimum time before the positive transition of the clock pulse (C) that information must be present at the input D or S.

t_{hold} is the minimum time after the positive transition of the clock pulse (C) that information must remain unchanged at the input D or S.

Input Pulse
$t+ = t- = 2.0$ ns ± 0.2 ns
(20 to 80%)



50-ohm termination to ground located in each scope channel input.

All input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be < 1/4 inch from TP_{in} to input pin and TP_{out} to output pin.

Unused outputs are connected to a 50-ohm resistor to ground.

SET UP AND HOLD TIMES

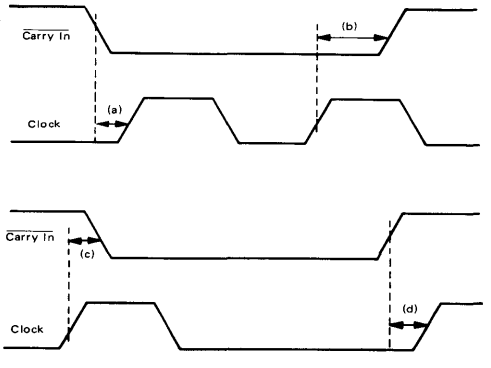
(a) is the minimum time to wait after the counter has been enabled to clock it.

(b) is the minimum time before the counter has been disabled that it may be clocked.

(c) is the minimum time before the counter is enabled that a clock pulse may be applied with no effect on the state of the counter.

(d) is the minimum time to wait after the counter is disabled that a clock pulse may be applied with no effect in the state of the counter.

(b) and (c) may be negative numbers.



APPLICATIONS INFORMATION

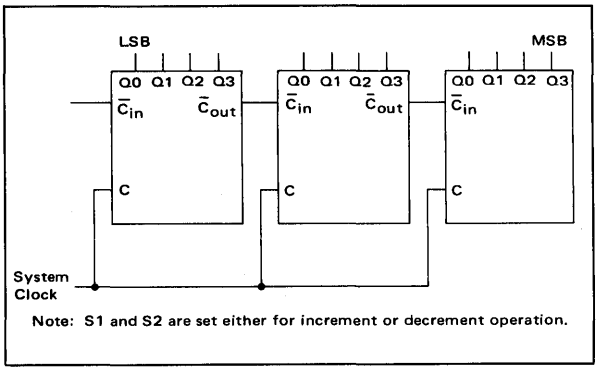
To provide more than four bits of counting capability several MC10136 counters may be cascaded. The $\overline{\text{Carry In}}$ input overrides the clock when the counter is either in the increment mode or the decrement mode of operation. This input allows several devices to be cascaded in a fully synchronous multistage counter as illustrated in Figure 1. The carry is advanced between stages as shown with no external gating. The $\overline{\text{Carry In}}$ of the first device may be left open. The system clock is common to all devices.

The various operational modes of the counter make it useful for a wide variety of applications. If used with MECL III devices, prescalers with input toggle frequencies in excess of 300 MHz are possible. Figure 2 shows such a prescaler using the MC10136 and MC1670. Use of the MC10231 in place of the MC1670 permits 200 MHz operation.

The MC10136 may also be used as a programmable counter. The configuration of Figure 3 requires no additional gates, although maximum frequency is limited to about 50 MHz. The divider modulus is equal to the program input plus one (M = N + 1), therefore, the counter will divide by a modulus varying from 1 to 16.

A second programmable configuration is also illustrated in Figure 4. A pulse swallowing technique is used to speed the counter operation up to 110 MHz typically. The divider modulus for this figure is equal to the program input (M = N). The minimum modulus is 2 because of the pulse swallowing technique, and the modulus may vary from 2 to 15. This programmable configuration requires an additional gate, such as ½MC10109 and a flip-flop such as ½MC10131.

FIGURE 1 — 12 BIT SYNCHRONOUS COUNTER



Note: S1 and S2 are set either for increment or decrement operation.

FIGURE 2 — 300 MHz PRESCALER

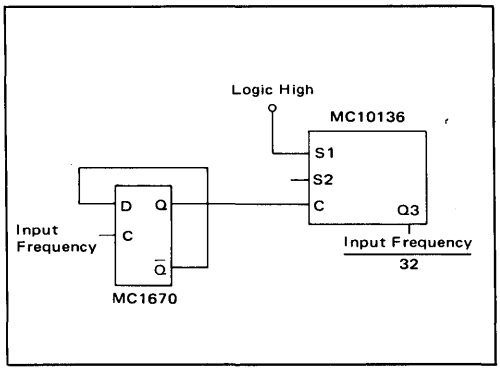
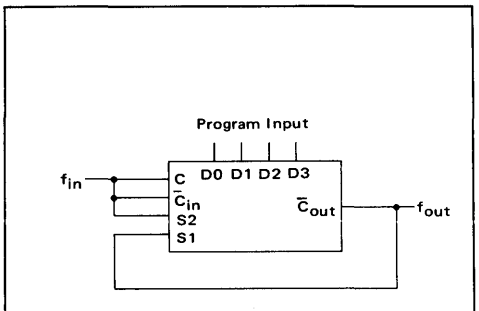


FIGURE 3 — 50 MHz PROGRAMMABLE COUNTER

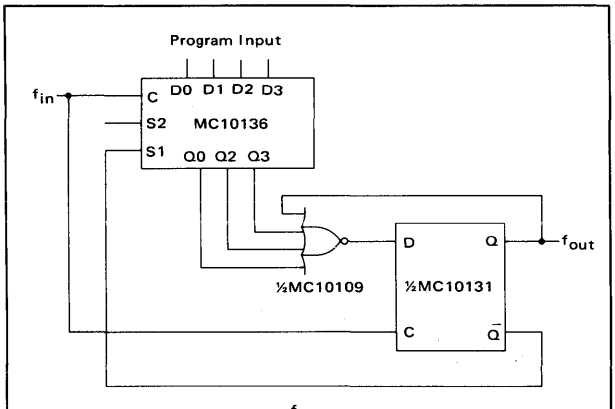


1 $f_{out} = \dfrac{f_{in}}{\text{Program Input} + 1}$

2 $f_{max} \cong 50$ MHz Typ.

3 Divide Ratio is from 1 to 16.

FIGURE 4 — 100 MHz PROGRAMMABLE COUNTER



1 $f_{out} = \dfrac{f_{in}}{\text{Program Input}}$

2 $f_{max} \cong 110$ MHz Typ.

3 Divide Ratio is from 2 to 15.

MOTOROLA

MC10137

MECL 10K SERIES

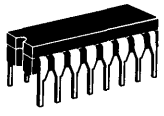
UNIVERSAL DECADE COUNTER

UNIVERSAL DECADE COUNTER

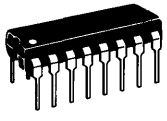
The MC10137 is a high speed synchronous counter that can count up, down, preset, or stop count at frequencies exceeding 100 MHz. The flexibility of this device allows the designer to use one basic counter for most applications. The synchronous count feature makes the MC10137 suitable for either computers or instrumentation.

Three control lines (S1, S2, and $\overline{\text{Carry In}}$) determine the operation mode of the counter. Lines S1 and S2 determine one of four operations; preset (program), increment (count up), decrement (count down), or hold (stop count). Note that in the preset mode a clock pulse is necessary to load the counter, and the information present on the data inputs (D0, D1, D2, and D3) will be entered into the counter. $\overline{\text{Carry Out}}$ goes low on the terminal count. The $\overline{\text{Carry Out}}$ on the MC10137 is partially decoded from Q1 and Q2 directly, so in the preset mode the condition of the $\overline{\text{Carry Out}}$ after the Clock's positive excursion will depend on the condition of Q1 and/or Q2. The counter changes state only on the positive going edge of the clock. Any other input may change at any time except during the positive transition of the clock. The sequence for counting out of improper states is as shown in the State Diagrams.

P_D = 625 mW typ/pkg (No Load)
f_{count} = 150 MHz typ
t_{pd} = 3.3 ns typ (C-Q)
= 7.0 ns typ (C-$\overline{C}_{out}$)
= 5.0 ns typ ($\overline{C}_{in}$-$\overline{C}_{out}$)



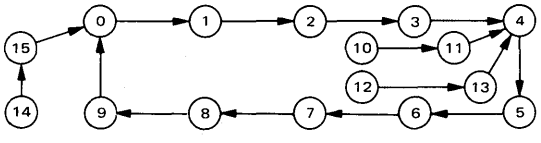
L SUFFIX
CERAMIC PACKAGE
CASE 620



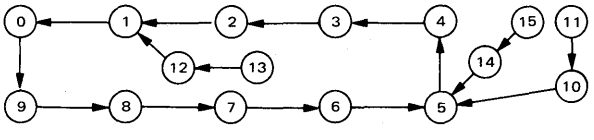
P SUFFIX
PLASTIC PACKAGE
CASE 648

STATE DIAGRAMS

COUNT UP



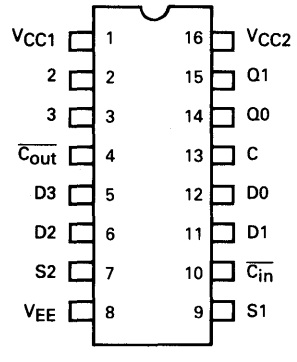
COUNT DOWN



FUNCTION SELECT TABLE

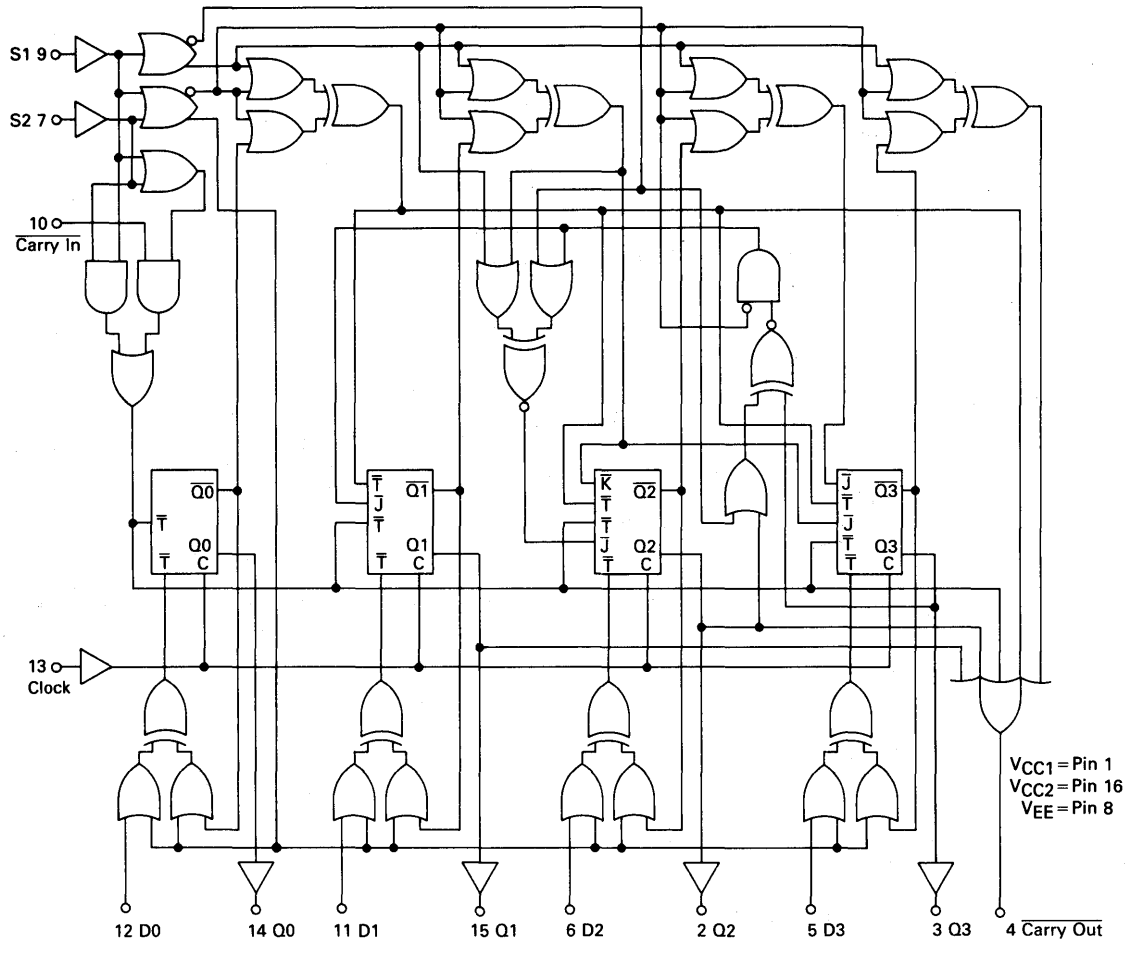
S1	S2	Operating Mode
L	L	Preset (Program)
L	H	Increment (Count Up)
H	L	Decrement (Count Down)
H	H	Hold (Stop Count)

PIN ASSIGNMENT



3

LOGIC DIAGRAM



SEQUENTIAL TRUTH TABLE*

INPUTS								OUTPUTS				
S1	S2	D0	D1	D2	D3	$\overline{\text{Carry In}}$	Clock **	Q0	Q1	Q2	Q3	$\overline{\text{Carry Out}}$
L	L	H	H	H	L	ϕ	↑ H	H	H	H	L	H
L	H	ϕ	ϕ	ϕ	ϕ	↓ L	↑ H	L	L	L	H	H
L	H	ϕ	ϕ	ϕ	ϕ	↓ L	↑ H	H	L	L	H	L
L	H	ϕ	ϕ	ϕ	ϕ	↓ L	↑ H	L	L	L	L	H
L	H	ϕ	ϕ	ϕ	ϕ	↓ L	H	H	L	L	L	H
L	H	ϕ	ϕ	ϕ	ϕ	↑ H	L	H	L	L	L	H
L	H	ϕ	ϕ	ϕ	ϕ	H	H	H	L	L	L	H
H	H	ϕ	ϕ	ϕ	ϕ	ϕ	H	H	L	L	L	H
L	L	H	H	L	L	ϕ	H	H	H	L	L	H
H	L	ϕ	ϕ	ϕ	ϕ	L	H	L	H	L	L	H
H	L	ϕ	ϕ	ϕ	ϕ	L	H	H	L	L	L	H
H	L	ϕ	ϕ	ϕ	ϕ	L	H	L	L	L	L	L

COUNT DOWN

ϕ = Don't care.

* Truth table shows logic states assuming inputs vary in sequence shown from top to bottom.

** A clock H is defined as a clock input transition from a low to a high logic level.

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Test Procedures are shown only for selected inputs and outputs. Other inputs and outputs are tested in a similar manner.

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

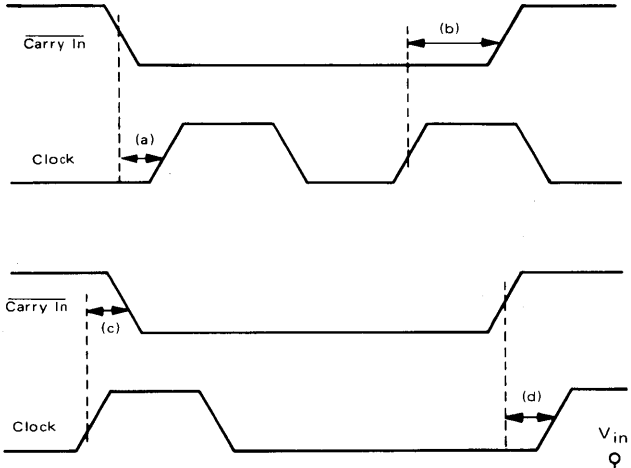
Characteristic	Symbol	Pin Under Test	MC10137L Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	--	165	--	120	150	--	165	mAdc	--	--	--	--	8	1, 16
Input Current	$I_{in\ H}$	5,6,11,12	--	350	--	--	220	--	220	µAdc	5,6,11,12	--	--	--	8	1, 16
		7	--	425	--	--	265	--	265		7	--	--	--	↓	↓
		9,10	--	390	--	--	245	--	24[illegible]		9,10	--	--	--		
		13	--	460	--	--	290	--	29[illegible]							
								0.3							8	1, 16
Logic "1" Output Voltage								-0.890	-0.[illegible]							
Logic "0" Output Voltage								-1.825	-1							
Logic "1" Threshold Voltage								-0.910								
Logic "0" Threshold Voltage								--	--							
Switching Times (50-ohm Load)																
Propagation Delay Cl[illegible]								1.1								
								1.1								
								2.5								
								2.5								
$\overline{\text{Carry In}}$ To $\overline{\text{Carry Out}}$								1.5								
								1.5								
Set Up Time Dat								3.5								
Selec								3.5								
$\overline{\text{Carry}}$								7.5								
								7.5								
								4.5								
								−1.0								
Hold Time Dati								0								
								0								
Selec								−2.5								
$\overline{\text{Carry I}}$								−2.5								
								−1.6								
								4.0								
Counting Frequency								125	--	MHz						
						150	--	125	--	MHz	9					
Rise Time (20% to 80%)	t_{4+}	4	0.9	3.3	1.1	2.0	3.3	1.1	3.5	ns	7	--			4	
	t_{14+}	14	↓	↓	↓	2.0	↓	↓	↓	↓	↓	--	↓	↓	14	↓
Fall Time (20% to 80%)	t_{4-}	4				2.0						--			4	
	t_{14-}	14				2.0						--			14	

Margie
Ed Lopez

Wayne,
We didn't connect @ 1:15. Would you come by and see me when you get a chance re: the synthesizer milestones.
Thanks.
Kurt
x1267

① Individually apply $V_{IL\ min}$ to pin under test. ② Measure output after clock pulse V_{IL} ⌐ V_{IH} appears at clock input (pin 13) ③ Before test set Q1 and Q2 outputs to a logic low.

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C



(a) is the minimum time to wait after the counter has been enabled to clock it.

(b) is the minimum time before the counter has been disabled that it may be clocked.

(c) is the minimum time before the counter is enabled that a clock pulse may be applied with no effect on the state of the counter.

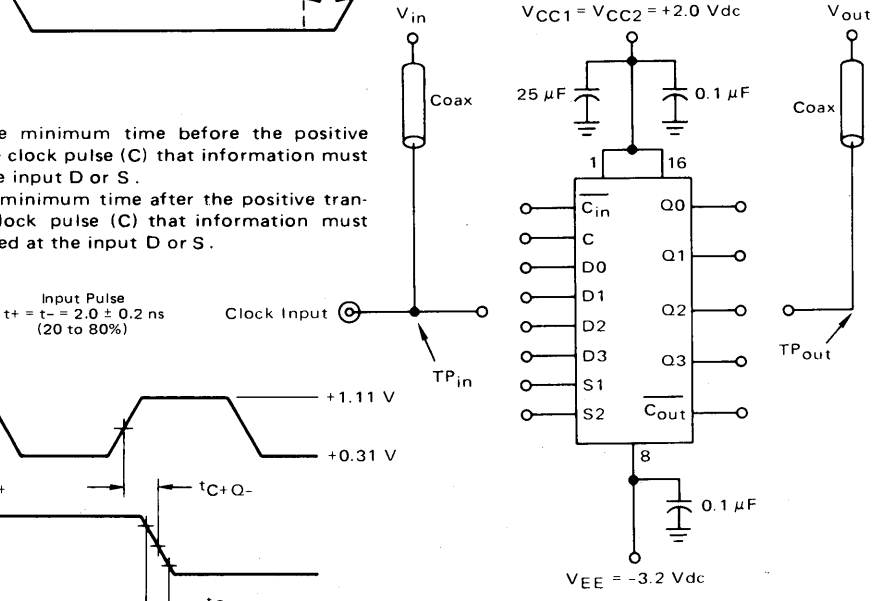
(d) is the minimum time to wait after the counter is disabled that a clock pulse may be applied with no effect in the state of the counter.

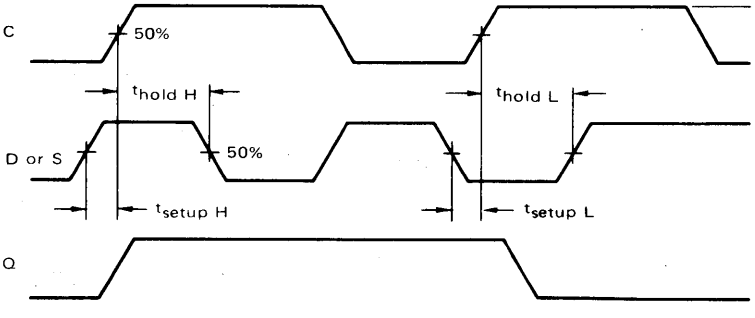
(b) and (c) may be negative numbers.

NOTE:

t_{setup} is the minimum time before the positive transition of the clock pulse (C) that information must be present at the input D or S.

t_{hold} is the minimum time after the positive transition of the clock pulse (C) that information must remain unchanged at the input D or S.





50-ohm termination to ground located in each scope channel input.

All input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be 1/4 inch from TP_{in} to input pin and TP_{out} to output pin.

Unused outputs are connected to a 50-ohm resistor to ground.

ELECTRICAL CHARACTERISTICS

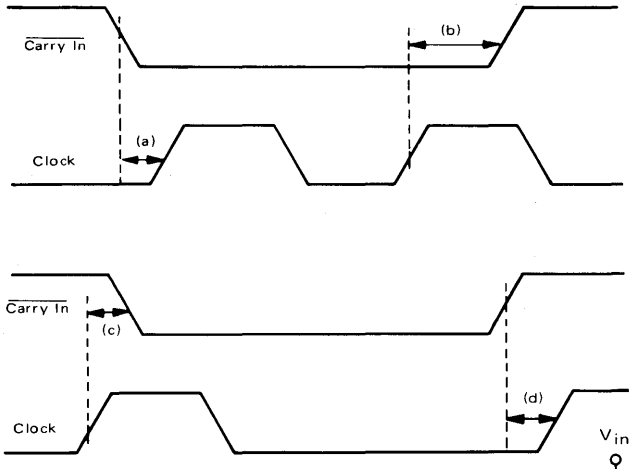
Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Test Procedures are shown only for selected inputs and outputs. Other inputs and outputs are tested in a similar manner.

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10137L Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	--	165	--	120	150	--	165	mAdc	--	--	--	--	8	1, 16
Input Current	$I_{in\ H}$	5,6,11,12	--	350	--	--	220	--	220	µAdc	5,6,11,12	--	--	--	8	1, 16
		7	--	425	--	--	265	--	265		7	--	--	--		
		9,10	--	390	--	--	245	--	245		9,10	--	--	--		
		13	--	460	--	--	290	--	290		13	--	--	--		
	$I_{in\ L}$	All	0.5	--	0.5	--	--	0.3	--	µAdc	--	①	--	--	8	1, 16
Logic "1" Output Voltage	V_{OH}	14 ②	-1.060	-0.890	-0.960	--	-0.810	-0.890	-0.700	Vdc	12	7, 9	--	--	8	1, 16
Logic "0" Output Voltage	V_{OL}	14 ②	-1.890	-1.675	-1.850	--	-1.650	-1.825	-1.615	Vdc	--	7, 9	--	--	8	1, 16
Logic "1" Threshold Voltage	V_{OHA}	14 ②	-1.080	--	-0.980	--	--	-0.910	--	Vdc	--	7, 9	12	--	8	1, 16
Logic "0" Threshold Voltage	V_{OLA}	14 ②	--	-1.655	--	--	-1.630	--	-1.595	Vdc	--	7, 9	--	12	8	1, 16
Switching Times (50-ohm Load)											+1.11 V	+0.31 V	Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay																
Clock Input	t_{13+14+}	14	0.8	4.8	1.0	3.3	4.5	1.1	5.0	ns	12	--	13	14	8	1, 16
	t_{13+14-}	14	0.8	4.8	1.0	3.3	4.5	1.1	5.0		--	--		14		
	t_{13+4+}	4	2.0	10.9	2.5	7.0	10.5	2.5	11.5		7	--		4		
	t_{13+4-}	4	2.0	10.9	2.5	7.0	10.5	2.5	11.5		7	--		4		
$\overline{\text{Carry In}}$ To $\overline{\text{Carry Out}}$	t_{10-4-}	4 ③	1.4	7.4	1.6	5.0	6.9	1.5	7.5		7	13	10	4		
	t_{10+4+}	4	1.4	7.4	1.6	5.0	6.9	1.5	7.5		7	13	10	4		
Set Up Time																
Data Inputs	t_{12+13+}	14	3.5	--	3.5	--	--	3.5	--		--	7, 9	12, 13	14		
	t_{12-13+}	14	3.5	--	3.5	--	--	3.5	--		--	7, 9	12, 13			
Select Inputs	t_{9+13+}	14	7.5	--	7.5	--	--	7.5	--		--	--	9, 13			
	t_{7+13+}	14	7.5	--	7.5	--	--	7.5	--		--	--	7, 13			
$\overline{\text{Carry In}}$ Input	t_{10-13+}	14	4.5	--	3.7	--	--	4.5	--		7	9	10, 13	14		
	t_{13+10+}	14	−1.0	--	-1.0	--	--	−1.0	--		7	9	10, 13	14		
Hold Time																
Data Inputs	t_{13+12+}	14	0	--	0	--	--	0	--		--	7, 9	12, 13	14		
	t_{13+12-}	14	0	--	0	--	--	0	--		--	7, 9	12, 13			
Select Inputs	t_{13+9+}	14	−2.5	--	-2.5	--	--	−2.5	--		--	--	9, 13			
	t_{13+7+}	14	−2.5	--	-2.5	--	--	−2.5	--		--	--	7, 13			
$\overline{\text{Carry In}}$ Input	t_{13+10-}	14	−1.6	--	-1.6	--	--	−1.6	--		7	9	10, 13			
	t_{10+13+}	14	4.0	--	3.1	--	--	4.0	--		7	9	10, 13			
Counting Frequency	$f_{countup}$	14	125	--	125	150	--	125	--	MHz	7	--	13			
	$f_{countdown}$	14	125	--	125	150	--	125	--	MHz	9	--				
Rise Time (20% to 80%)	t_{4+}	4	0.9	3.3	1.1	2.0	3.3	1.1	3.5	ns	7	--		4		
	t_{14+}	14				2.0						--		14		
Fall Time (20% to 80%)	t_{4-}	4				2.0						--		4		
	t_{14-}	14				2.0						--		14		

① Individually apply $V_{IL\ min}$ to pin under test. ② Measure output after clock pulse V_{IL} ⎍ V_{IH} appears at clock input (pin 13) ③ Before test set Q1 and Q2 outputs to a logic low.

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C



(a) is the minimum time to wait after the counter has been enabled to clock it.

(b) is the minimum time before the counter has been disabled that it may be clocked.

(c) is the minimum time before the counter is enabled that a clock pulse may be applied with no effect on the state of the counter.

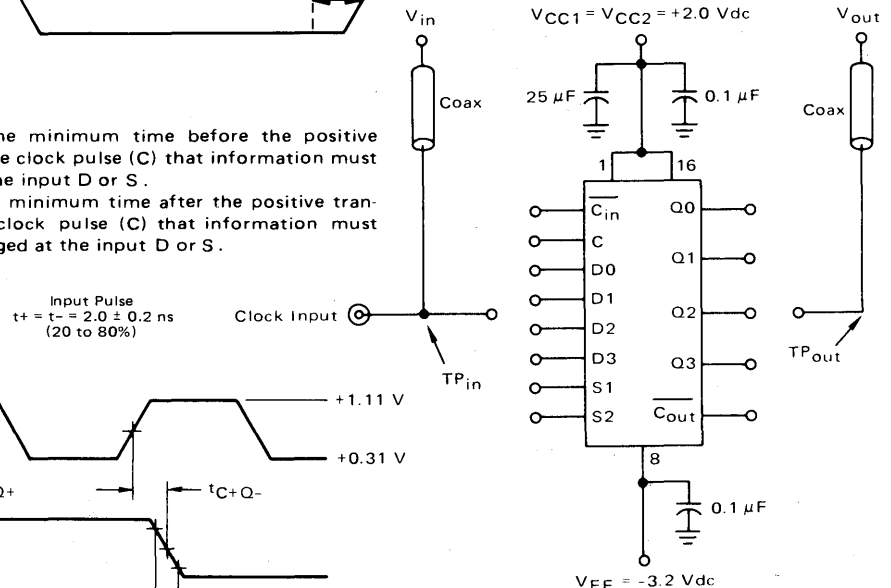
(d) is the minimum time to wait after the counter is disabled that a clock pulse may be applied with no effect in the state of the counter.

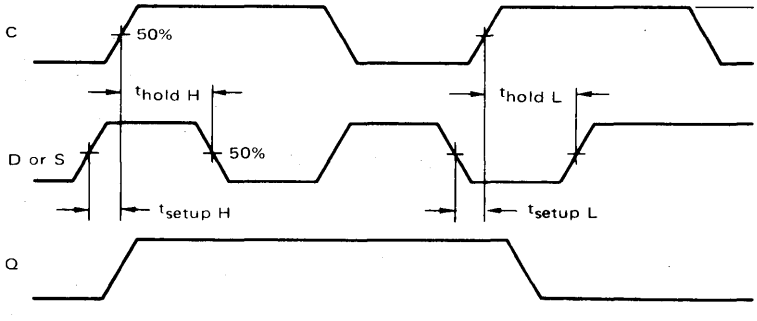
(b) and (c) may be negative numbers.

NOTE:

t_{setup} is the minimum time before the positive transition of the clock pulse (C) that information must be present at the input D or S.

t_{hold} is the minimum time after the positive transition of the clock pulse (C) that information must remain unchanged at the input D or S.





50-ohm termination to ground located in each scope channel input.

All input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be 1/4 inch from TP_{in} to input pin and TP_{out} to output pin.

Unused outputs are connected to a 50-ohm resistor to ground.

MOTOROLA

MC10138

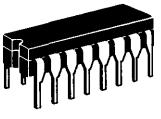
MECL 10K SERIES

BI-QUINARY COUNTER

The MC10138 is a four bit counter capable of divide by two, five, or ten functions. It is composed of four set-reset master-slave flip-flops. Clock inputs trigger on the positive going edge of the clock pulse.

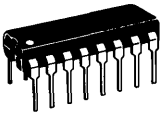
Set or reset input override the clock, allowing asynchronous "set" or "clear." Individual set and common reset inputs are provided, as well as complementary outputs for the first and fourth bits.

P_D = 370 mW typ/pkg (No Load)
f_{tog} = 150 MHz typ
t_r, t_f = 2.5 ns typ (20%–80%)

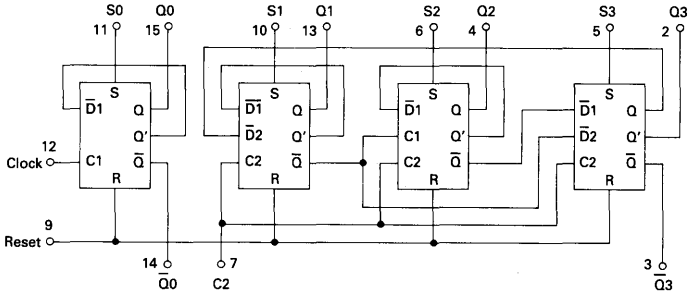


L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648



LOGIC DIAGRAM



V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

COUNTER TRUTH TABLES

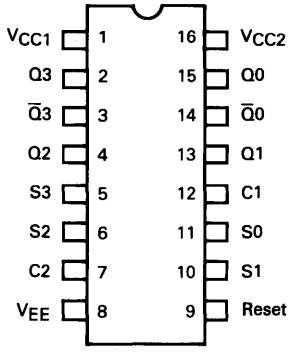
BI-QUINARY
(Clock connected to C2 and Q3 connected to C1)

COUNT	Q1	Q2	Q3	Q0
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	L	L	L	H
6	H	L	L	H
7	L	H	L	H
8	H	H	L	H
9	L	L	H	H

BCD
(Clock connected to C1 and $\overline{Q0}$ connected to C2)

COUNT	Q0	Q1	Q2	Q3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H

PIN ASSIGNMENT



ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts.

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10138 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	--	97	--	70	88	--	97	mAdc	9	--	--	--	8	1,16
Input Current	$I_{in}H$	12	--	350	--	--	220	--	220		12	--	--	--		
		5,6,10,11	--	390	--	--	245	--	245		5,6,10,11	--	--	--		
		7	--	460	--	--	290	--	290		7	--	--	--		
		9	--	650	--	--	410	--	410		9	--	--	--		
	$I_{in}L$	All	0.5	--	0.5	--		0.3	--	μAdc	--	*	--	--	8	1,16
Logic "1" Output Voltage	V_{OH}	3,14 ②	-1.060	-0.890	-0.960	--	-0.810	-0.890	-0.700	Vdc	9	--	--	--	8	1,16
		2,4,13,15 ①	-1.060	-0.890	-0.960	--	-0.810	-0.890	-0.700	Vdc	5,6,10,11	--	--	--	8	1,16
Logic "0" Output Voltage	V_{OL}	3,14 ①	-1.890	-1.675	-1.850	--	-1.650	-1.825	-1.615	Vdc	5,6,10,11	--	--	--	8	1,16
		2,4,13,15 ②	-1.890	-1.675	-1.850	--	-1.650	-1.825	-1.615	Vdc	9	--	--	--	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	2,4,13,15 ①	-1.080	--	-0.980	--	--	-0.910	--	Vdc	--	--	5,6,10,11	--	8	1,16
		3,14 ②	↓	--	↓	--	--	↓	--	↓	--	--	9	--	↓	↓
		13,15 ①		--		--	--		--		--	--	7,12	--		
Logic "0" Threshold Voltage	V_{OLA}	2,4,13,15 ②	--	-1.655	--	--	-1.630	--	-1.595	Vdc	--	--	--	5,6,10,11	8	1,16
		3,14 ①	--	↓	--	--	↓	--	↓	↓	--	--	--	9	↓	↓
		13,15 ②	--		--	--		--			--	--	--	7,12		
Switching Times (50-ohm Load)													Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay																
Clock Delays 50 Ω Loads	t_{12+15+}	15	1.4	5.0	1.5	3.5	4.8	1.5	5.3	ns	--	--	12	15	8	1,16
	t_{12+14+}	14	↓	5.0	↓	↓	4.8	↓	5.3	↓	--	--	12	14	↓	↓
	t_{7+13+}	13		5.2			5.0		5.5		--	--	7	13		
	t_{7+4+}	4		↓			↓		↓		--	--	↓	4		
	t_{7+2+}	2									--	--		2		
	t_{7+3+}	3									--	--		3		
	t_{12+15-}	15		5.0			4.8		5.3		--	--	12	15		
	t_{12+14-}	14		5.0			4.8		5.3		--	--	12	14		
	t_{7+13-}	13		5.2			5.0		5.5		--	--	7	13		
	t_{7+4-}	4		↓			↓		↓		--	--	↓	4		
	t_{7+2-}	2									--	--		2		
	t_{7+3-}	3				↓					--	--		3		
Set Delay	t_{11+15+}	15		5.2		—					--	--	11	15		
	t_{11+14-}	14		5.2		—					--	--	11	14		
Reset Delay	t_{9+14+}	14				—					--	--	9	14		
	t_{9+15-}	15		↓		—	↓		↓	↓	--	--	9	15		
Rise Time (20% to 80%)	t_{14+}	14	1.1	4.7	1.1	2.5	4.5	1.1	5.0	ns	--	--	11	14		
	t_{15+}	15	1.1	4.7	1.1	↓	4.5	1.1	5.0	↓	--	--	11	15		
Fall Time (20% to 80%)	t_{14-}	14	↓	↓	↓		↓	↓	↓		--	--	9	14		
	t_{15-}	15								↓	--	--	9	15		
Counting Frequency	f_{count}	2	125		125	150	--	125	--	MHz	--	--	7	2		
		15	125		125	150	--	125	--	MHz	--	--	12	15		

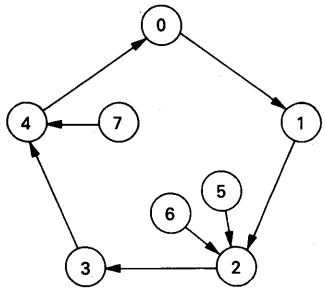
*Individually apply V_{ILmin} to pin under test.

① Set all four flip-flops by applying pulse V_{IHmax} / V_{ILmin} to pins 5,6,10,11 prior to applying test voltage indicated.

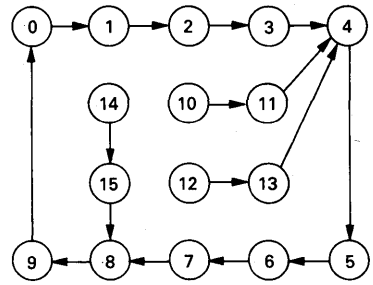
② Reset all four flip-flops by applying pulse V_{IHmax} / V_{ILmin} to pin 9 prior to applying test voltage indicated.

COUNTER STATE DIAGRAM — POSITIVE LOGIC

Clock connected to C2



$\overline{Q0}$ connected to C2



MOTOROLA

MC10141

FOUR-BIT UNIVERSAL SHIFT REGISTER

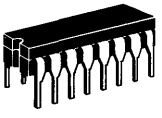
The MC10141 is a four-bit universal shift register which performs shift left, or shift right, serial/parallel in, and serial/parallel out operations with no external gating. Inputs S1 and S2 control the four possible operations of the register without external gating of the clock. The flip-flops shift information on the positive edge of the clock. The four operations are stop shift, shift left, shift right, and parallel entry of data. The other six inputs are all data type inputs; four for parallel entry data, and one for shifting in from the left (DL) and one for shifting in from the right (DR).

P_D = 425 mW typ/pkg (No Load)
f_{Shift} = 200 MHz typ
t_r, t_f = 2.0 ns typ (20%–80%)

MECL 10K SERIES

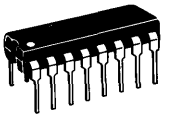
FOUR-BIT UNIVERSAL SHIFT REGISTER

3

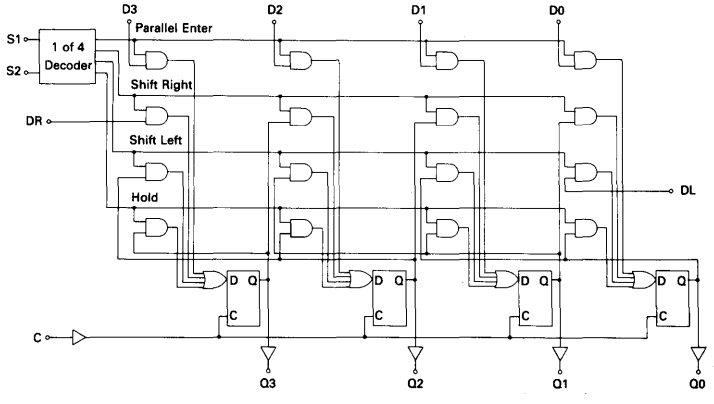


L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

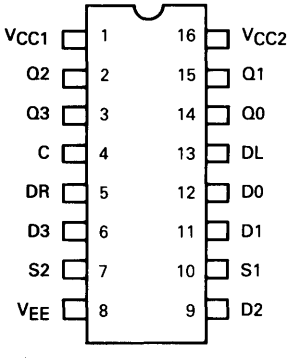


LOGIC DIAGRAM



V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

PIN ASSIGNMENT



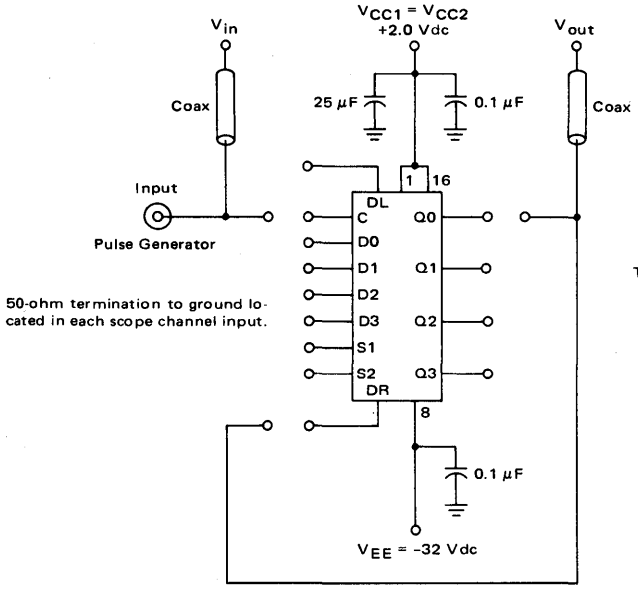
TRUTH TABLE

SELECT			OUTPUTS			
S1	S2	OPERATING MODE	$Q0_{n+1}$	$Q1_{n+1}$	$Q2_{n+1}$	$Q3_{n+1}$
L	L	Parallel Entry	D0	D1	D2	D3
L	H	Shift Right*	$Q1_n$	$Q2_n$	$Q3_n$	DR
H	L	Shift Left*	DL	$Q0_n$	$Q1_n$	$Q2_n$
H	H	Stop Shift	$Q0_n$	$Q1_n$	$Q2_n$	$Q3_n$

*Outputs as exist after pulse appears at "C" input with input conditions as shown. (Pulse = Positive transition of clock input).

3

SHIFT FREQUENCY TEST CIRCUIT



All input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be < 1/4 inch from TP_{in} to input pin and TP_{out} to output pin.

50-ohm termination to ground located in each scope channel input.

Test Procedures:

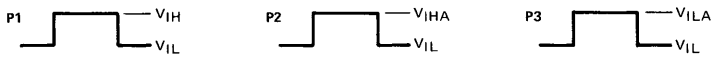
1. Set D1, D2, D3 = +0.31 Vdc (Logic L)
   D0 = +1.11 Vdc (Logic H)
2. Apply Clock pulse V_{IH} / V_{IL} to set Q0 high.
3. Maintain Clock Low.
   Set S1 = +0.31 Vdc (Logic L)
   S2 = +1.11 Vdc (Logic H)
4. Test Shift Frequency

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established in an ambient temperature of 25°C, while the circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown for only one input, or for one set of input conditions. Other inputs tested in the same manner.

@ Test Temperature	TEST VOLTAGE VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10141 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}	P1	P2	P3	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	112	–	82	102	–	112	mAdc	–	–	–	–	8	–	–	–	1,16
Input Current	$I_{in\ H}$	5	–	350	–	–	220	–	220	μAdc	5	–	–	–	8	–	–	–	1,16
		6	–	350	–	–	220	–	220		6	–	–	–		–	–	–	
		7	–	390	–	–	245	–	245		7	–	–	–		–	–	–	
		4	–	425	–	–	265	–	265		4	–	–	–		–	–	–	
	$I_{in\ L}$	12	0.5	–	0.5	–	–	0.3	–	μAdc	4,5,6,7,9, 10,11,13	12	–	–	8	–	–	–	1,16
Logic "1" Output Voltage	V_{OH}	3	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	6	–	–	–	8	4	–	–	1,16
Logic "0" Output Voltage	V_{OL}	3	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	–	–	–	–	8	4	–	–	1,16
Logic "1" Threshold Voltage	V_{OHA} ①	3	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	6	–	8	4	–	–	1,16
				–		–	–		–		6	④	–	7		4	–	–	
				–		–	–		–		6	④	–	–		–	4	–	
				–		–	–		–		–	–	–	–		–	–	4	
Logic "0" Threshold Voltage	V_{OLA} ①	3	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	–	6	8	4	–	–	1,16
			–		–	–		–			–	⑤	–	7		4	–	–	
			–		–	–		–			–	⑤	–	–		–	4	–	
			–		–	–		–			6	–	–	–		–	–	4	
Switching Times (50 Ω Load)																			
Propagation Delay	t_{4+3+}	3	1.7	3.9	1.8	2.9	3.8	2.0	4.2	ns	②	–	–	–	-3.2 V	–	–	–	+2.0 V
Setup Time (t_{setup})	t_{12+4+}	14	2.5	–	2.5	–	–	2.5	–		–	–	–	–	8	–	–	–	1,16
	t_{10+4+}	14	5.5	–	5.0	–		5.5	–		–	–	–	–		–	–	–	
Hold Time (t_{hold})	t_{4+12+}	14	1.5	–	1.5	–	–	1.5	–		–	–	–	–		–	–	–	
Rise Time (20% to 80%)	t_{3+}	3	1.0	3.4	1.1	2.0	3.3	1.1	3.6		②	–	–	–		–	–	–	
Fall Time (20% to 80%)	t_{3-}	3	1.0	3.4	1.1	2.0	3.3	1.1	3.6		②	–	–	–		–	–	–	
Shift Frequency	f_{Shift}	–	150	–	150	200	–	150	–	MHz	③	–	–	–		–	–	–	



① These tests to be performed in sequence as shown.
② See switching time test circuit for test procedures.
③ See shift frequency test circuit for test procedures.
④ Reset to zero before performing test
⑤ Reset to one before performing test.

MOTOROLA

MC10153

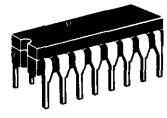
MECL 10K SERIES

QUAD LATCH

QUAD LATCH

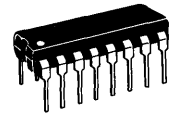
The MC10153 is a high speed, low power, MECL quad latch consisting of four bistable latch circuits with D type inputs and gated Q outputs. Open emitters allow a large number of outputs to be wire-ORed together. Latch outputs are gated, allowing direct wiring to a bus. When the clock is low, outputs will follow D inputs. Information is latched on positive going transition of the clock. The MC10153 provides the same logic function as the MC10133, except for inversion of the clock.

P_D = 310 mW typ/pkg (No Load)
t_{pd} = 4.0 ns typ
t_r, t_f = 2.0 ns typ (20%–80%)

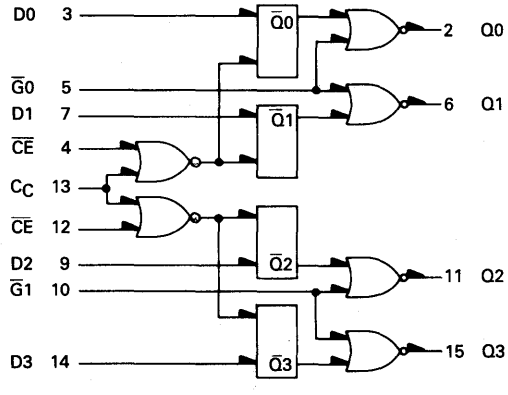


L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648



LOGIC DIAGRAM



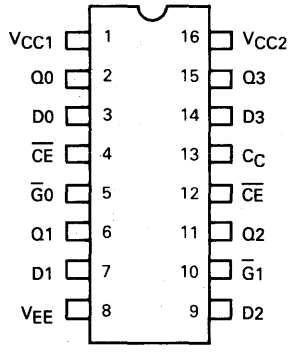
TRUTH TABLE

$\overline{G}$	C	D	Q_{n+1}
H	ϕ	ϕ	L
L	H	ϕ	Q_n
L	L	L	L
L	L	H	H

ϕ = Don't Care
C = C_C + $\overline{CE}$

V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

PIN ASSIGNMENT



ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown for only selected inputs and outputs. Other inputs and outputs are tested in a similar manner.

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10153 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	83	–	–	75	–	83	mAdc	–	13	–	–	8	1,16
Input Current	I_{inH}	3	–	390	–	–	245	–	245	µAdc	3	–	–	–	8	1,16
		4	–	390	–	–	245	–	245		4	–	–	–		
		5	–	560	–	–	350	–	350		5	–	–	–		
		13	–	460	–	–	290	–	290		13	–	–	–		
	I_{inL}	3	0.5	–	0.5	–	–	0.3	–	µAdc	–	3	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	3	4	–	–	8	1,16
		2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	3	13	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	–	3,13	–	–	8	1,16
		2				–					3,5	13	–	–		
		2				–					–	3,4	–	–		
Logic "1" Threshold Voltage	V_{OHA}	2	-1.080	–	-0.980	–	–	-0.910	–	Vdc	3	4	–	5	8	1,16
		2		–		–	–		–		–	4	3	–		
		2		–		–	–		–		3	4	–	–		
		2†		–		–	–		–		3	–	–	–		
		2††		–		–	–		–		–	–	–	–		
		2††		–		–	–		–		–	–	–	–		
		2		–		–	–		–		3	–	–	4		
		2		–		–	–		–		3	–	–	13		
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.655	–	–	-1.630	–	-1.595	Vdc	3	4	5	–	8	1,16
		2	–		–	–		–			–	4	–	3		
		2	–		–	–		–			–	4	–	–		
		2†	–		–	–		–			–	–	–	–		
		2††	–		–	–		–			3	–	–	–		
		2††	–		–	–		–			3	–	–	13		
Switching Times (50 Ω Load)											+1.11 V		Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{3+2+}	2	1.0	5.6	1.0	4.0	5.4	1.1	5.9	ns	–	–	3	2	8	1,16
	t_{4-2+}	2	1.0	5.6	1.0	4.0	5.6	1.2	6.2		3 *	–	4	2		
	t_{5-2+}	2	1.0	3.2	1.0	2.0	3.1	1.0	3.4		–	–	5	2		
	t_{Setup}	3	2.5	–	2.5	0.7	–	2.5	–		–	–	3	2		
	t_{Hold}	3	1.5	–	1.5	0.7	–	1.5	–		–	–	3	2		
Rise Time (20% to 80%)	t_{2+}	2	1.0	3.6	1.1	2.0	3.5	1.1	3.8		–	–	3	2		
Fall Time (20% to 80%)	t_{2-}	2	1.0	3.6	1.1	2.0	3.5	1.1	3.8		–	–	3	2		

†Output level to be measured after a clock pulse has been applied to the clock input (Pin 4).

††Data input at proper high/low level while clock pulse is low so that device latches at proper high/low level for test. Levels are measured after device has latched.

V_{IH} max
V_{IL} min

*Latch set to zero state before test.

MOTOROLA

MC10154

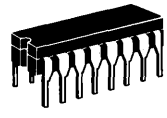
MECL 10K SERIES

BINARY COUNTER

The MC10154 is a four-bit counter capable of divide-by-two, divide-by-four, divide-by-eight or a divide-by-sixteen function.

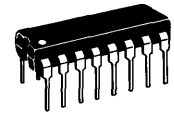
Clock inputs trigger on the positive going edge of the clock pulse. Set and Reset inputs override the clock, allowing asynchronous "set" or "clear." Individual Set and common Reset inputs are provided, as well as complementary outputs for the first and fourth bits. True outputs are available at all bits.

P_D	=	370 mW typ./pkg. (No Load)
f_{toggle}	=	150 m Hz (typ.)
t_{pd}	=	3.5 ns typ. (C to Q_0)
t_{pd}	=	11 ns typ. (C to Q_3)

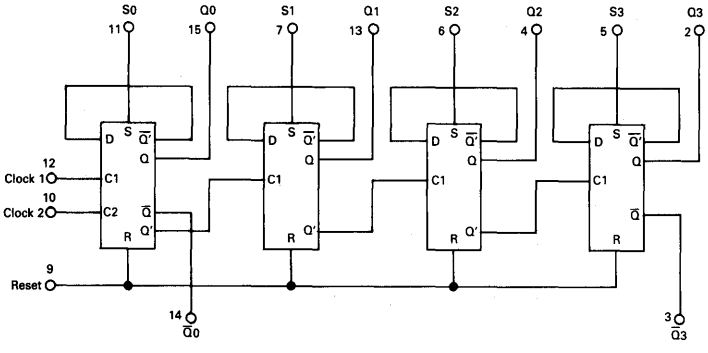


L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648



LOGIC DIAGRAM



V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

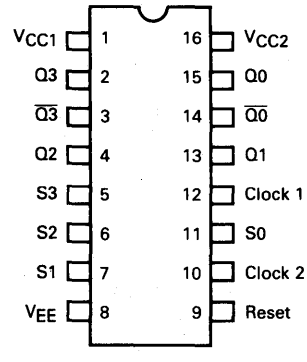
TRUTH TABLE

INPUTS							OUTPUTS			
R	S_0	S_1	S_2	S_3	C_1	C_2	Q_0	Q_1	Q_2	Q_3
H	L	L	L	L	ϕ	ϕ	L	L	L	L
L	H	H	H	H	ϕ	ϕ	H	H	H	H
L	L	L	L	L	H	ϕ	No Count			
L	L	L	L	L	ϕ	H	No Count			
L	L	L	L	L	*	*	H	H	H	H
L	L	L	L	L	*	*	L	H	H	H
L	L	L	L	L	*	*	H	L	H	H
L	L	L	L	L	*	*	L	L	H	H
L	L	L	L	L	*	*	H	H	L	H
L	L	L	L	L	*	*	L	H	L	H
L	L	L	L	L	*	*	H	L	L	H
L	L	L	L	L	*	*	L	L	L	H
L	L	L	L	L	*	*	H	H	H	L
L	L	L	L	L	*	*	L	H	H	L
L	L	L	L	L	*	*	H	L	H	L
L	L	L	L	L	*	*	L	L	H	L
L	L	L	L	L	*	*	H	H	L	L
L	L	L	L	L	*	*	L	H	L	L
L	L	L	L	L	*	*	H	L	L	L
L	L	L	L	L	*	*	L	L	L	L

ϕ = Don't Care
*

V_{IL} / V_{IH} Clock transitions from V_{IL} to V_{IH} may be applied to C_1 or C_2 or both for same effect.

PIN ASSIGNMENT



ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown for only selected inputs and outputs. Other inputs and outputs tested in the same manner.

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10154 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	97	–	–	88.5	–	97	mAdc	9	–	–	–	8	1,16
Input Current	I_{inH}	12	–	390	–	–	245	–	245	µAdc	12	–	–	–	8	1,16
		11	–	350	–	–	220	–	220	µAdc	11	–	–	–	8	1,16
		9	–	650	–	–	410	–	410	µAdc	9	–	–	–	8	1,16
	I_{inL}	*	0.5	–	0.5	–	–	0.3	–	µAdc	–	*	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	14	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	9	–	–	–	8	1,16
		15	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	11	–	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	14	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	11	–	–	–	8	1,16
		15	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	9	–	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	3	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	5	–	8	1,16
		14	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	11	–	8	1,16
		15	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	9	–	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	3	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	–	5	8	1,16
		14	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	–	11	8	1,16
		15	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	–	9	8	1,16
Switching Times													Pulse In	Pulse Out	-3.2 Vdc	+2.0 Vdc
Clock Input Propagation Delay	t_{12+15+}	15	1.4	5.0	1.5	3.5	4.8	1.5	5.3	ns	–	–	12	15	8	1,16
	t_{12-13-}	13	1.9	9.4	2.0	6.0	9.2	2.0	9.8		–	–		13		
	t_{12+4-}	4	2.9	12.3	3.0	8.5	12	3.0	12.8		–	–		4		
	t_{12-3+}	3	3.9	14.9	4.0	11	14.5	4.0	15.5		–	–		3		
Rise Time (20 to 80%)	t_{15+}	15	1.1	4.7	1.1	2.5	4.5	1.1	5.0		–	–		15		
Fall Time (20 to 80%)	t_{15-}	15	1.1	4.7	1.1	2.5	4.5	1.1	5.0		–	–		15		
Set Input	t_{11-15+}	15	1.4	5.2	1.5	—	5.0	1.5	5.5	ns	–	–	11	15	8	1,16
Reset Input	t_{9-15+}	15	1.4	5.2	1.5	—	5.0	1.5	5.5	ns	–	–	9	15	8	1,16
Counting Frequency	f_{count}	15	125	–	125	150	–	125	–	MHz	–	–	12	15	8	1,16

*Individually test each input applying V_{IL} to input under test.

MOTOROLA

MC10158

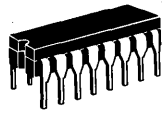
QUAD 2-INPUT MULTIPLEXER (NON-INVERTING)

The MC10158 is a quad two channel multiplexer. A common select input determines which data inputs are enabled. A high (H) level enables data inputs D00, D10, D20, and D30 and a low (L) level enables data inputs D01, D11, D21, and D31.

P_D = 197 mW typ/pkg (No Load)
t_{pd} = 2.5 ns typ (Data to Q)
3.2 ns typ (Select to Q)
t_r, t_f = 2.5 ns typ (20%–80%)

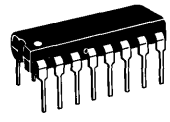
MECL 10K SERIES

QUAD 2-INPUT MULTIPLEXER (NON-INVERTING)

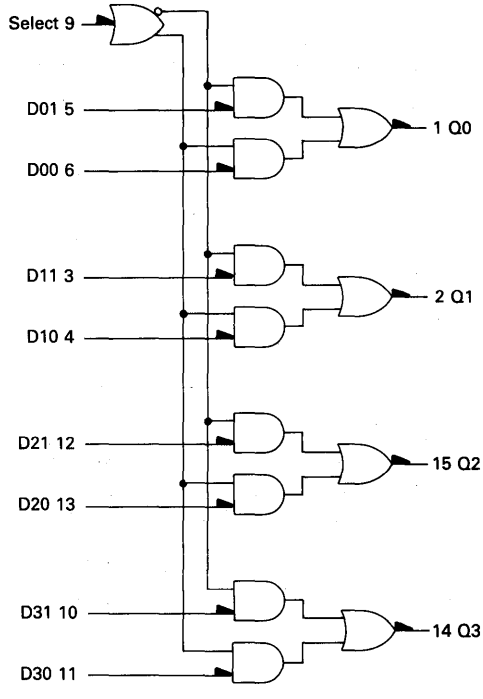


L SUFFIX
CERAMIC PACKAGE
CASE 620

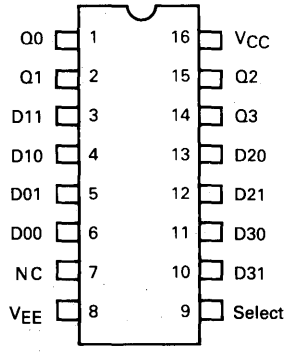
P SUFFIX
PLASTIC PACKAGE
CASE 648



LOGIC DIAGRAM



PIN ASSIGNMENT



TRUTH TABLE

Select	D0	D1	Q
L	ϕ	L	L
L	ϕ	H	H
H	L	ϕ	L
H	H	ϕ	H

ϕ = Don't care

V_{CC} = Pin 16
V_{EE} = Pin 8

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown for only selected inputs and outputs. Other inputs and outputs are tested in a similar manner.

@ Test Temperature	TEST VOLTAGE VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10158 TEST LIMITS −30°C Min	−30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	53	–	38	48	–	53	mAdc	–	–	–	–	8	16
Input Current	I_{inH}	9	–	360	–	–	225	–	225	μAdc	9	–	–	–	8	16
		5	–	400	–	–	250	–	250	μAdc	5	–	–	–	8	16
	I_{inL}	5	0.5		0.5		–	0.3	–	μAdc	–	5	–	–	8	16
Logic "1" Output Voltage	V_{OH}	1	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	5	–	–	–	8	16
Logic "0" Output Voltage	V_{OL}	1	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	–	–	–	–	8	16
Logic "1" Threshold Voltage	V_{OHA}	1	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	5	–	8	16
Logic "0" Threshold Voltage	V_{OLA}	1	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	–	5	8	16
Switching Times (50 Ω Load)											+1.11 Vdc	+0.31 Vdc	Pulse In	Pulse Out	-3.2 Vdc	+2.0 Vdc
Propagation Delay										ns					8	16
Data Input	t_{5-1-}	1	1.3	3.1	1.2	2.5	3.0	1.3	3.2		–	–	5	1		
Select Input	t_{9+1+}	1	2.5	4.8	2.4	3.2	4.5	2.5	4.8		6	–	9	1		
Rise Time (20% to 80%)	t_{1+}	1	1.6	3.4	1.5	2.5	3.3	1.6	3.4		–	–	5	1		
Fall Time (20% to 80%)	t_{1-}	1	1.6	3.4	1.5	2.5	3.3	1.6	3.4		–	–	5	1		

MOTOROLA

MC10159

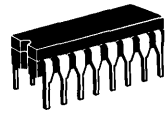
QUAD 2-INPUT MULTIPLEXER (INVERTING)

The MC10159 is a quad two channel multiplexer with enable. It incorporates common enable and common data select inputs. The select input determines which data inputs are enabled. A high (H) level enables data inputs D00, D10, D20, and D30. A low (L) level enables data inputs D01, D11, D21, and D31. Any change on the data inputs will be reflected at the outputs while the enable is low. Input levels are inverted at the output.

P_D = 218 mW typ/pkg (No Load)
t_{pd} = 2.5 ns typ (Data to Q)
3.2 ns typ (Select to Q)
t_r, t_f = 2.5 ns typ (20%–80%)

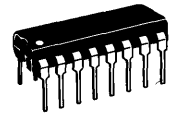
MECL 10K SERIES

QUAD 2-INPUT MULTIPLEXER (INVERTING)

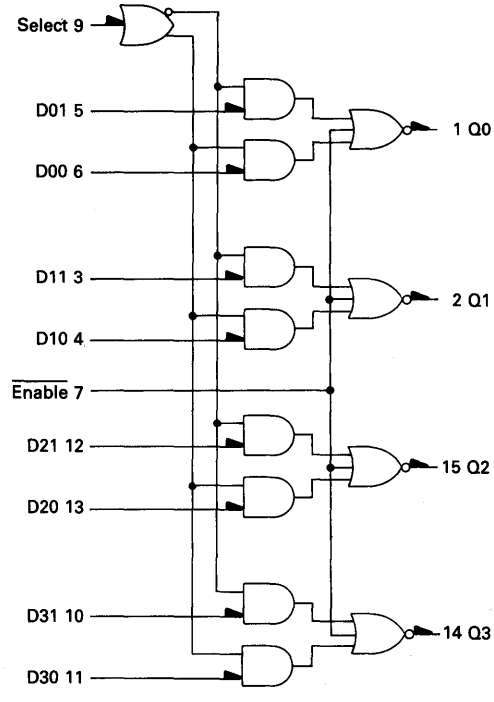


L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648



LOGIC DIAGRAM



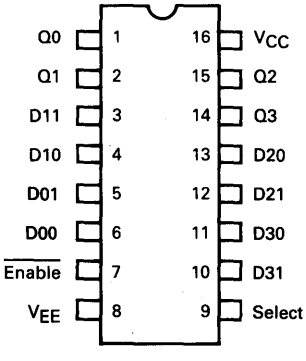
TRUTH TABLE

Enable	Select	D0	D1	Q
L	L	ϕ	L	H
L	L	ϕ	H	L
L	H	L	ϕ	H
L	H	H	ϕ	L
H	ϕ	ϕ	ϕ	L

ϕ = Don't Care

V_{CC} = Pin 16
V_{EE} = Pin 8

PIN ASSIGNMENT



ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown for only selected inputs and outputs. Other inputs and outputs are tested in a similar manner.

@ Test Temperature	TEST VOLTAGE VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10159 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	58	–	42	53	–	58	mAdc	–	–	–	–	8	16
Input Current	I_{inH}	9	–	360	–	–	225	–	225	µAdc	9	–	–	–	8	16
		5	–	400	–	–	250	–	250	µAdc	5	–	–	–	8	16
	I_{inL}	5	0.5		0.5		–	0.3	–	µAdc	–	5	–	–	8	16
Logic "1" Output Voltage	V_{OH}	1	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	–	–	–	–	8	16
Logic "0" Output Voltage	V_{OL}	1	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	5	–	–	–	8	16
Logic "1" Threshold Voltage	V_{OHA}	1	-1.080	–	-0.980	–	–	-0.910	–	Vdc	9	–	–	6	8	16
Logic "0" Threshold Voltage	V_{OLA}	1	–	-1.655	–	–	-1.630	–	-1.595	Vdc	9	–	6	–	8	16
Switching Times (50 Ω Load)											+1.11 Vdc	+0.31 Vdc	Pulse In	Pulse Out	-3.2 Vdc	+2.0 Vdc
Propagation Delay										ns					8	16
Data Input	t_{5+1-}	1	1.1	3.8	1.2	2.5	3.3	1.1	3.8		–	–	5	1		
Select Input	t_{9+1-}	1	1.5	5.3	1.5	3.2	5.0	1.5	5.3		6	–	9	1		
Enable Input	t_{7+1-}	1	1.4	5.3	1.5	2.5	5.0	1.4	5.3		3,12	–	7	1		
Rise Time (20% to 80%)	t_{1+}	1	1.0	3.7	1.1	2.5	3.5	1.0	3.7		9	–	5	1		
Fall Time (20% to 80%)	t_{1-}	1	1.0	3.7	1.1	2.5	3.5	1.0	3.7		9	–	5	1		

MOTOROLA

MC10160

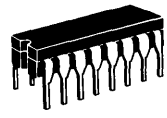
MECL 10K SERIES

12-BIT PARITY GENERATOR-CHECKER

The MC10160 consists of nine EXCLUSIVE-OR gates in a single package, internally connected to provide odd parity checking or generation. Output goes high when an odd number of inputs are high. Unconnected inputs are pulled to low logic levels allowing parity detection and generation for less than 12 bits.

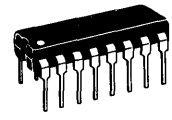
P_D = 320 mW typ/pkg (No Load)
t_{pd} = 5.0 ns typ
t_r, t_f = 2.0 ns typ (20%–80%)

12-BIT PARITY GENERATOR-CHECKER

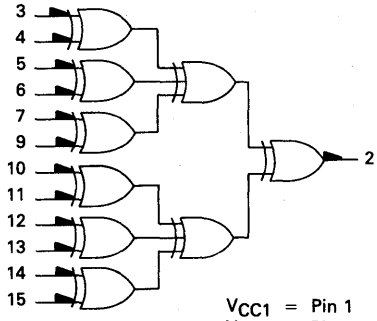


L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648



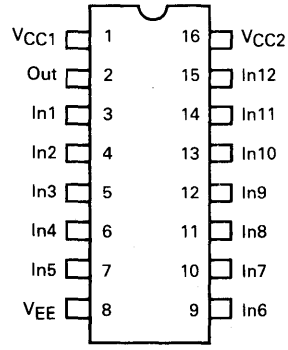
LOGIC DIAGRAM



V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

INPUT	OUTPUT
Sum of High Level Inputs	Pin 2
Even	Low
Odd	High

PIN ASSIGNMENT



ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown for one set of conditions. Complete testing according to truth table.

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10160 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	86	–	62	78	–	86	mAdc	4,5,9,10,13,14	–	–	–	8	1,16
Input Current	I_{inH}*	3	–	425	–	–	265	–	265	µAdc	3	–	–	–	8	1,16
		4	–	350	–	–	220	–	220	µAdc	4	–	–	–	8	1,16
	I_{inL}	3	0.5	–	0.5	–	–	0.3	–	µAdc	–	3	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	3	4,5,6,7,9,10, 11,12,13,14,15	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	–	3,4,5,6,7,9,10, 11,12,13,14,15	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	2	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	4,5,6,7,9,10,11, 12,13,14,15	3	–	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	3,5,6,7,9,10,11 12,13,14,15	–	4	8	1,16
Switching Times (50 Ω Load) Propagation Delay											+1.11 V		Pulse In	Pulse Out	-3.2 V	+2.0 V
	t_{3+2+}	2	1.8	8.1	2.0	5.0	7.5	2.0	8.0	ns	–	–	3	2	8	1,16
	t_{3+2-}										4	–				
	t_{3-2-}										–	–				
	t_{3-2+}										4	–				
	t_{4+2+}										–	–	4			
	t_{4+2-}										3	–				
	t_{4-2-}										–	–				
	t_{4-2+}										3	–				
Rise Time (20% to 80%)	t_{2+}		1.1	3.5	1.1	2.0	3.3	1.0	3.5		–	–	3			
Fall Time (20% to 80%)	t_{2-}		1.1	3.5	1.1	2.0	3.3	1.0	3.5		–	–	3			

*Pins 3, 6, 7, 11, 12, 15 are similar
Pins 4, 5, 9, 10, 13, 14 are similar

MC10161

MECL 10K SERIES

BINARY TO 1–8 DECODER (LOW)

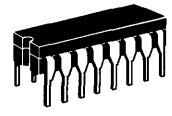
BINARY TO 1–8 DECODER (LOW)

The MC10161 is designed to decode a three bit input word to a one of eight line output. The selected output will be low while all other outputs will be high. The enable inputs, when either or both are high, force all outputs high.

The MC10161 is a true parallel decoder. No series gating is used internally, eliminating unequal delay times found in other decoders. This design provides the identical 4 ns delay from any address or enable input to any output.

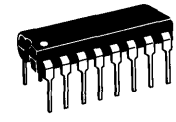
A complete mux/demux operation on 16 bits for data distribution is illustrated in Figure 1. This system, using the MC10136 control counters, has the capability of incrementing, decrementing or holding data channels. When both S0 and S1 are low, the index counters reset, thus initializing both the mux and demux units. The four binary outputs of the counter are buffered by the MC10101s to send twisted-pair select data to the multiplexer/demultiplexer units.

P_D = 315 mW typ/pkg (No Load)
t_{pd} = 4.0 ns type
t_r, t_f = 2.0 ns typ (20%–80%)

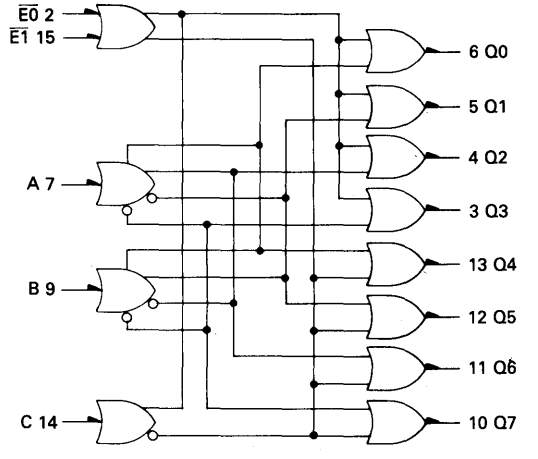


L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648



LOGIC DIAGRAM

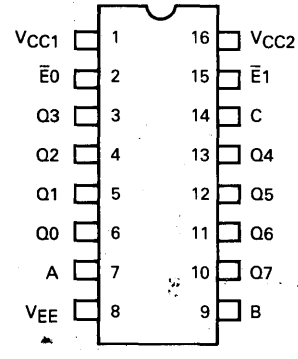


V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

TRUTH TABLE

ENABLE INPUTS		INPUTS			OUTPUTS							
$\overline{E1}$	$\overline{E0}$	C	B	A	Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7
L	L	L	L	L	L	H	H	H	H	H	H	H
L	L	L	L	H	H	L	H	H	H	H	H	H
L	L	L	H	L	H	H	L	H	H	H	H	H
L	L	L	H	H	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	L	H	H	H
L	L	H	L	H	H	H	H	H	H	L	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	L
H	ϕ	ϕ	ϕ	ϕ	H	H	H	H	H	H	H	H
ϕ	H	ϕ	ϕ	ϕ	H	H	H	H	H	H	H	H

PIN ASSIGNMENT



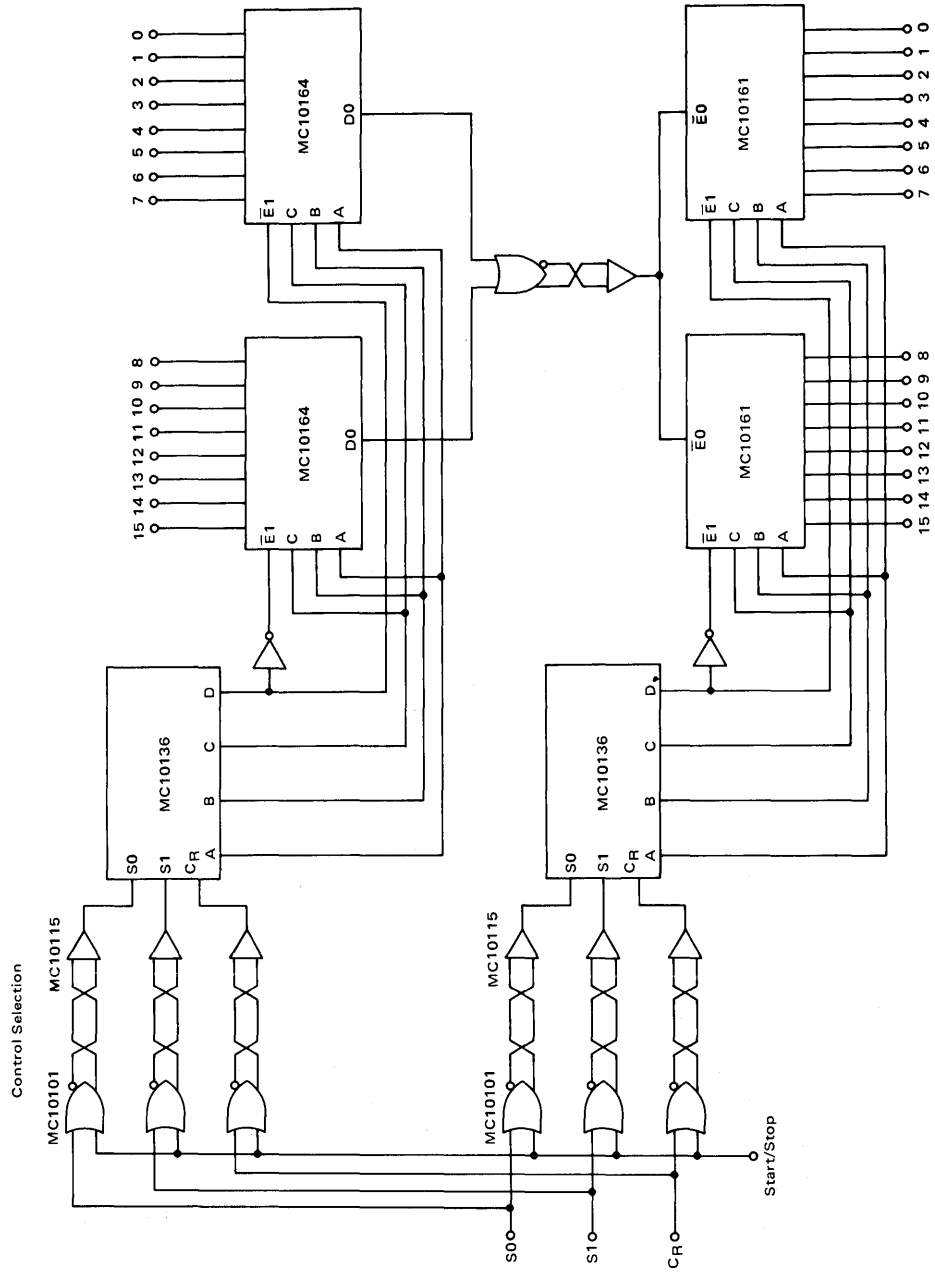
ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only one input/output combination. Other combinations are tested according to the truth table.

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10161 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	**84**	–	61	76	–	**84**	mAdc	2,7,9,14,15	–	–	–	8	1,16
Input Current	I_{inH}	14	–	**350**	–	–	220	–	**220**	μAdc	14	–	–	–	8	1,16
	I_{inL}	14	**0.5**	–	0.5	–	–	**0.3**	–	μAdc	–	14	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	13	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	2	–	–	–	8	1,16
		13	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	15	–	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	13	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	14	–	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	13	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	2	–	8	1,16
		13	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	15	–	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	13	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	14	–	8	1,16
Switching Times (50 Ω Load)													Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{14+13-}	13	1.5	6.2	1.5	4.0	6.0	1.5	6.4	ns	–	–	14	13	8	1,16
	t_{14-13+}	13	1.5	6.2	1.5	4.0	6.0	1.5	6.4		–	–				
Rise Time (20% to 80%)	t_{13+}	13	1.0	3.3	1.1	2.0	3.3	1.1	3.5		–	–				
Fall Time (20% to 80%)	t_{13-}	13	1.0	3.3	1.1	2.0	3.3	1.1	3.5		–	–				

FIGURE 1 – HIGH SPEED 16-BIT MULTIPLEXER/DEMULTIPLEXER



MOTOROLA

MC10162

BINARY TO 1–8 DECODER (HIGH)

The MC10162 is designed to convert three lines of input data to a one-of-eight output. The selected output will be high while all other outputs are low. The enable inputs, when either or both are high, force all outputs low.

The MC10162 is a true parallel decoder. No series gating is used internally, eliminating unequal delay times found in other decoders.

This device is ideally suited for demultiplexer applications. One of the two enable inputs is used as the data input, while the other is used as a data enable input.

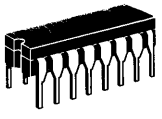
A complete mux/demux operation on 16 bits for data distribution is illustrated in Figure 1 of the MC10161 data sheet.

P_D = 315 ns typ/pkg (No Load)
t_{pd} = 4.0 ns typ
t_r, t_f = 2.0 ns typ (20%–80%)

MECL 10K SERIES

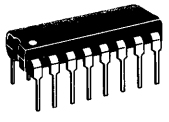
BINARY TO 1–8 DECODER (HIGH)

3

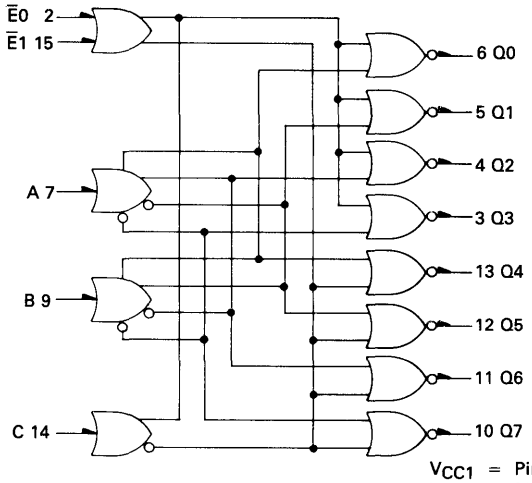


L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648



LOGIC DIAGRAM



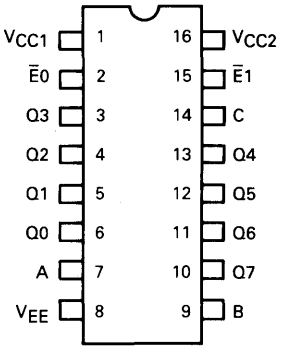
V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

TRUTH TABLE

INPUTS					OUTPUTS							
Ē0	Ē1	C	B	A	Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7
L	L	L	L	L	H	L	L	L	L	L	L	L
L	L	L	L	H	L	H	L	L	L	L	L	L
L	L	L	H	L	L	L	H	L	L	L	L	L
L	L	L	H	H	L	L	L	H	L	L	L	L
L	L	H	L	L	L	L	L	L	H	L	L	L
L	L	H	L	H	L	L	L	L	L	H	L	L
L	L	H	H	L	L	L	L	L	L	L	H	L
L	L	H	H	H	L	L	L	L	L	L	L	H
H	ϕ	ϕ	ϕ	ϕ	L	L	L	L	L	L	L	L
ϕ	H	ϕ	ϕ	ϕ	L	L	L	L	L	L	L	L

ϕ = Don't Care

PIN ASSIGNMENT



ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown for only input/output combination. Other combinations are tested according to the truth table.

@Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
−30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10162 Test Limits −30°C Min	−30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	84	–	61	76	–	84	mAdc	–	–	–	–	8	1,16
Input Current	I_{inH}	14	–	350	–	–	220	–	220	μAdc	14	–	–	–	8	1,16
	I_{inL}	14	0.5	–	0.5	–	–	0.3	–	μAdc	–	14	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	13	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	14	–	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	13	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	2	–	–	–	8	1,16
		13	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	15	–	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	13	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	14	–	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	13	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	2	–	8	1,16
		13	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	15	–	8	1,16
Switching Times (50-ohm load)													Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{14+13+}	13	1.5	6.2	1.5	4.0	6.0	1.5	6.4	ns	–	–	14	13	8	1,16
	t_{14-13-}	13	1.5	6.2	1.5	4.0	6.0	1.5	6.4		–	–				
Rise Time (20% to 80%)	t+	13	1.0	3.3	1.1	2.0	3.3	1.1	3.5		–	–				
Fall Time (20% to 80%)	t-	13	1.0	3.3	1.1	2.0	3.3	1.1	3.5		–	–				

MOTOROLA

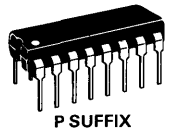
MC10163/MC10193

ERROR DETECTION- CORRECTION CIRCUIT

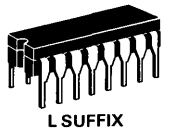
The MC10163 and the MC10193 are error detection and correction circuits. They are building blocks designed for use with memory systems. They offer economy in the design of error detection/correction subsystems for mainframe and add-on memory systems. For example, using eight MC10163s together with eight 12-bit parity checkers (MC10160), single-bit error detection/correction and double-bit error detection can be done on a word of 64-bit length. Only eight check bits (B0–B7) need be added to the word. A useful feature of this building block is that the MC10193 option generates the parity of all inputs to the block. Thus, if the MC10193 is applied in a byte sequence, individual byte parity is automatically available.

MECL 10K SERIES

ERROR DETECTION — CORRECTION CIRCUIT



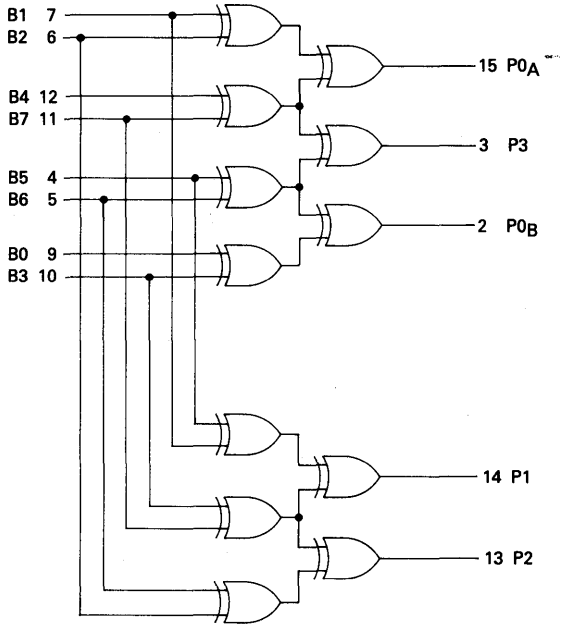
P SUFFIX
PLASTIC PACKAGE
CASE 648



L SUFFIX
CERAMIC PACKAGE
CASE 620

3

MC10163 LOGIC DIAGRAM



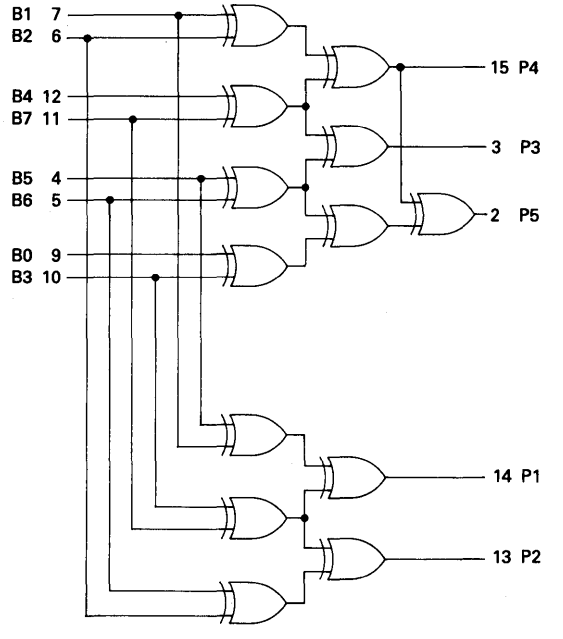
IBM CODE

$P0_A$ = B1, B2, B4, B7
$P0_B$ = B0, B3, B5, B6
P1 = B1, B3, B5, B7
P2 = B2, B3 B6, B7
P3 = B4, B5, B6, B7

V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

P_D = 520 mW typ/pkg (No Load)
t_{pd} = 5.0 ns typ

MC10193 LOGIC DIAGRAM



MOTOROLA CODE

P1 = B1, B3, B5, B7
P2 = B2, B3, B6, B7
P3 = B4, B5, B6, B7
P4 = B1, B2, B4, B7
P5 = Byte (B0 1, 2, 3, 4, 5, 6, 7)

V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

P_D = 520 mW typ/pkg (No Load)
t_{pd} = 7.5 ns typ (pin 7 to pin 2)
t_{pd} = 5.0 ns typ (pin 7 to pin 14)

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown only for selected inputs and outputs. Other inputs and outputs are tested in a similar manner.

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10163 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	137	–	–	125	–	137	mAdc	–	–	–	–	8	1,16
Input Current	I_{inH}	4,6,10	–	350	–	–	220	–	220	μAdc	4,6,10	–	–	–	8	1,16
		5,7,9,11,12	–	425	–	–	265	–	265	μAdc	5,7,9,11,12	–	–	–	8	1,16
	I_{inL}	*	0.5	–	0.5	–	–	0.3	–	μAdc	–	*	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	4	–	–	–	8	1,16
		3	↓	↓	↓	–	↓	↓	↓	↓	4	–	–	–	↓	↓
		13				–					11	–	–	–		
		14				–					11	–	–	–		
Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	–	4	–	–	8	1,16
		3	↓	↓	↓	–	↓	↓	↓	↓	–	11	–	–	↓	↓
		13				–					–	11	–	–		
		14				–					–	11	–	–		
Logic "1" Threshold Voltage	V_{OHA}	2	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	5	–	8	1,16
		3	↓	–	↓	–	–	↓	–	↓	–	–	11	–	↓	↓
		13		–		–	–		–		–	–	5	–		
		14		–		–	–		–		–	–	4	–		
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	–	5	8	1,16
		3	–	↓	–	–	↓	–	↓	↓	–	–	–	11	↓	↓
		13	–		–	–		–			–	–	–	5		
		14	–		–	–		–			–	–	–	4		
Switching Times (50 Ω Load)											+1.11 V		Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{7+15+}	15	1.3	6.8	1.5	5.0	6.5	1.5	7.1	ns	–	–	7	15	8	1,16
	t_{4+14+}	14	1.3	6.8	1.5	5.0	6.5	1.5	7.1	↓	–	–	4	14	↓	↓
Rise Time (20% to 80%)	t_{15+}	15	1.1	4.2	1.1	2.0	3.9	1.1	4.4		–	–	7	15		
Fall Time (20% to 80%)	t_{15-}	15	1.1	4.2	1.1	2.0	3.9	1.1	4.4		–	–	7	15		

*Individually test each input, apply V_{ILmin} to pin under test.

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown only for selected inputs and outputs. Other inputs and outputs are tested in a similar manner.

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10193 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	137	–	–	125	–	137	mAdc	–	–	–	–	8	1,16
Input Current	I_{inH}	4,6,10	–	350	–	–	220	–	220	μAdc	4,6,10	–	–	–	8	1,16
		5,7,9,11,12	–	425	–	–	265	–	265	μAdc	5,7,9,11,12	–	–	–	8	1,16
	I_{inL}	*	0.5	–	0.5	–	–	0.3	–	μAdc	–	*	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	4	–	–	–	8	1,16
		3	↓	↓	↓	–	↓	↓	↓	↓	4	–	–	–	↓	↓
		13				–					11	–	–	–		
		14				–					11	–	–	–		
Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	–	4	–	–	8	1,16
		3	↓	↓	↓	–	↓	↓	↓	↓	–	11	–	–	↓	↓
		13				–					–	11	–	–		
		14				–					–	11	–	–		
Logic "1" Threshold Voltage	V_{OHA}	2	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	5	–	8	1,16
		3	↓	–	↓	–	–	↓	–	↓	–	–	11	–	↓	↓
		13		–		–	–		–		–	–	5	–		
		14		–		–	–		–		–	–	4	–		
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	–	5	8	1,16
		3	–	↓	–	–	↓	–	↓	↓	–	–	–	11	↓	↓
		13	–		–	–		–			–	–	–	5		
		14	–		–	–		–			–	–	–	4		
Switching Times (50 Ω Load)											+1.11 V		Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{7+15+}	15	1.3	6.8	1.5	5.0	6.5	1.5	7.1	ns	–	–	7	15	8	1,16
	t_{4+14+}	14	1.3	6.8	1.5	5.0	6.5	1.5	7.1	↓	–	–	4	14	↓	↓
	t_{7+2+}	2	1.8	8.9	2.0	7.5	8.5	2.0	9.2		–	–	7	2		
	t_{4+2+}	2	1.8	8.9	2.0	7.5	8.5	2.0	9.2		–	–	4	2		
Rise Time (20% to 80%)	t_{15+}	15	1.1	4.2	1.1	2.5	3.9	1.1	4.4		–	–	7	15		
Fall Time (20% to 80%)	t_{15-}	15	1.1	4.2	1.1	2.5	3.9	1.1	4.4	↓	–	–	7	15	↓	↓

*Individually test each input, apply V_{ILmin} to pin under test.

MC10163 APPLICATIONS INFORMATION

The MC10163 is a building block for generating the modified Hamming single-error-correction, double-error-detection (SEC-DED) code used in the IBM 370/145 memory. While the MC10163 can also be used for generating other patterns, it is optimized for generating the pattern shown in the H matrix of Figure 1.

When writing into a memory, the MC10163 is used to generate the eight check bits (C0–C32, CT) which are stored with the 65 data bits (B0–B63). These check bits are generated by taking the parity of all data bits marked with an X in the appropriate row of the H matrix. (C0, C1, C32, CT, are even parity; C2, C4, C8, C17, are odd parity.) To generate these check bits with the building blocks, eight MC10163s and eight MC10160 parity checkers are used. One MC10163 is connected to each byte of data and the outputs of these building blocks are connected to the eight MC10160 parity checkers, one for each check bit. Figure 2 shows which connections are required (i.e., C0 is the even parity of output $P0_A$ of the MC10163 on the "zero" byte of data, output $P0_B$ of the "zero" byte, $P0_A$ of the "one" byte, —, $P0_B$ of the "three" byte and data bit 32.)

During the memory read operation, the fetched check bits previously generated (as described) are exclusive-ORed with newly generated C0-C32 to generate syndrome bits S0-S32. Syndrome ST is a special case where ST is the even parity of all eight fetched check bits and all 64 fetched data bits. For determining the type and location of an error:

1. If all syndromes (S0–S32 and ST) are false, there is no error.
2. If ST is true and S0–S32 are false, the CT is in error.
3. If ST is false and one or more of S0–S32 is true, an uncorrectable error has occurred.
4. If ST is true and one or more of S0–S32 is true, simply add the S1–S32 bits to get the binary location of the error (S1 has weight, 1, S2 weight 2, S4 weight 4, etc.)

Data bits B0 and B32 are special cases of this location technique: B0 is in error if ST, S0, and S32 are true; B32 is in error if ST, S0, S1, and S32 are true.

FIGURE 1 — 370/145 PATTERN

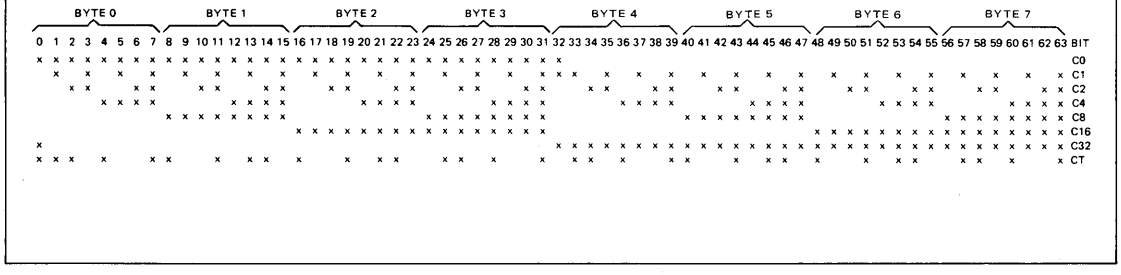


FIGURE 2 — 370/145 PATTERN GENERATION

C0 = $P0_{A0}$	$P0_{B0}$	$P0_{A1}$	$P0_{B1}$	$P0_{A2}$	$P0_{B2}$	$P0_{A3}$	$P0_{B3}$	B(32)
C1 = P10	P11	P12	P13	P14	P15	P16	P17	B(32)
C2 = P20	P21	P22	P23	P24	P25	P26	P27	
C4 = P30	P31	P32	P33	P34	P35	P36	P37	
C8 = $P0_{A1}$	$P0_{B1}$	$P0_{A3}$	$P0_{B3}$	$P0_{A5}$	$P0_{B5}$	$P0_{A7}$	$P0_{B7}$	
C16 = $P0_{A2}$	$P0_{A2}$	$P0_{A3}$	$P0_{B3}$	$P0_{A6}$	$P0_{B6}$	$P0_{A7}$	$P0_{B7}$	
C32 = $P0_{A4}$	$P0_{B4}$	$P0_{A5}$	$P0_{B5}$	$P0_{A6}$	$P0_{B6}$	$P0_{A7}$	$P0_{B7}$	B(0)
CT = $P0_{A0}$	$P0_{B1}$	$P0_{B2}$	$P0_{A3}$	$P0_{A4}$	$P0_{B5}$	$P0_{B6}$	$P0_{A7}$	B(0)

Where for P_{NM}: N = MC10163 Output
M = Byte Number

MC10193 APPLICATIONS INFORMATION

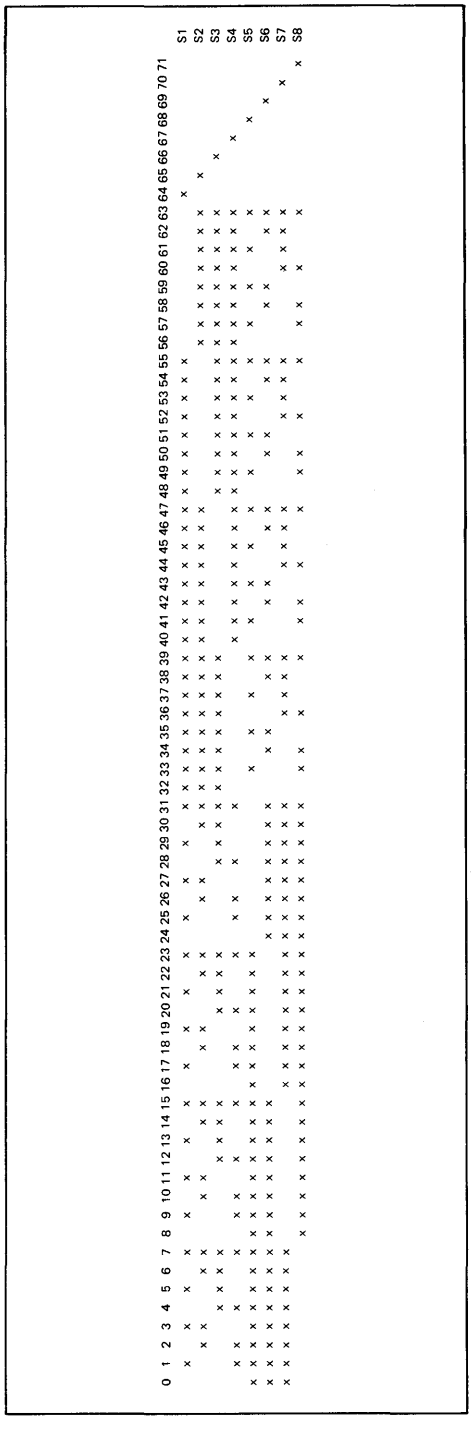


FIGURE 3 — MOTOROLA PATTERN EXAMPLE

The MC10193 is a building block for generating modified Hamming SEC-DED codes. It can be used for any length data word and for a variety of codes. The MC10193 is optimized for codes organized on a byte repetitive basis and has the advantage of automatically supplying whole byte parity (P5 output). While it is possible to use a number of criteria for choosing a pattern, the pattern of Figure 3 was chosen on the basis of speed and ease of error location decode. As can be seen in the H matrix of Figure 3, the pattern is repetitive by byte with the various rows generated by only five combinations of bit parities within the bytes. For the 64 bit data word in the example of Figure 3, the eight check bits (B64 to B71) are generated by the odd parity of all data bits indicated by an -X in the appropriate row. The syndromes S1 to S8 are generated by including the fetched check bits in the same generator that originally generated the check bits.

The pattern of Figure 3 is easily generated by using eight MC10193 devices, one for each data byte and eight MC10160 parity checkers, one for each syndrome/check bit. The connections of building blocks and parity checkers are shown in tabular form in Figure 4 and in schematic form in Figure 6.

Once the syndrome bits (S1 to S8) have been formed from fetched data (B0 to B63) and fetched check bits (B64 to B71), the determination of type and location of error is simply done:

1. If all syndromes are false, there is no error.
2. If one syndrome is true, the corresponding check bit is in error.
3. If more than one syndrome is true, and the parity of all syndromes is even, a multiple (uncorrectable) error has occurred.
4. If more than one syndrome is true, and the parity of all syndromes is odd, a single error has occurred and is easily located by the circuit of Figure 5.

Figure 5 gives the error location circuit for the example pattern. The outputs EB0 to EB7 are a one-of-eight-high code giving the byte in error. Outputs EC0 to EC3 give the binary location of the bit in error within the located byte. Since this location process can occur simultaneously with the determination of error type described, the entire error correction sequence (using a toggling fetched data latch) takes less than 20 ns. This is because an error occurrence detector is a simple ORing of S1 to S8. The error locator has simultaneously located the error which is then corrected as though the error was a single (and therefore correctable) error. The parity of syndromes then determines if the error was indeed single, and interrupts the CPU if the error was an uncorrectable (multiple) error. Since uncorrectable data is unusable without special handling, the CPU would be interrupted anyway; therefore this automatic correction of any error as if it were single does not create any problems. This fast error correction technique allows single error correction on a noninterrupt basis with only a 20 ns memory system access time penalty.

These techniques can, of course, be extended to large or smaller data words.

FIGURE 4 — M2 PATTERN BUILDING BLOCK

S1 =	P10	P11	P12	P13	P54	P55	P56	B(64)
S2 =	P20	P21	P22	P23	P54	P55	P57	B(65)
S3 =	P30	P31	P32	P33	P54	P56	P57	B(66)
S4 =	P40	P41	P42	P43	P55	P56	P57	B(67)
S5 =	P14	P15	P16	P17	P50	P51	P52	B(68)
S6 =	P24	P25	P26	P27	P50	P51	P53	B(69)
S7 =	P34	P35	P36	P37	P50	P52	P53	B(70)
S8 =	P44	P45	P46	P47	P51	P52	P53	B(71)

Where for P_{NM}: N = MC10193 Output
M = Byte Number

FIGURE 5 — M2 PATTERN CORRECTION MATRIX

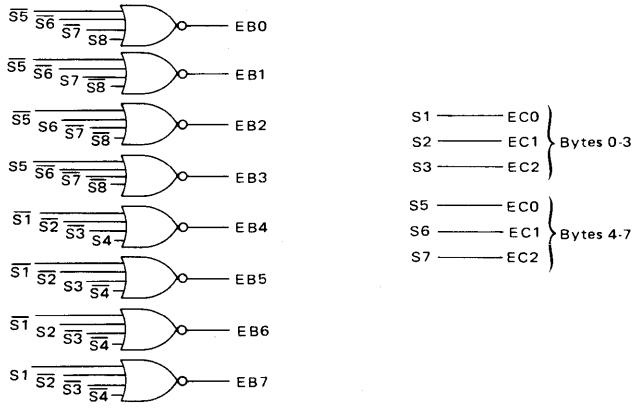
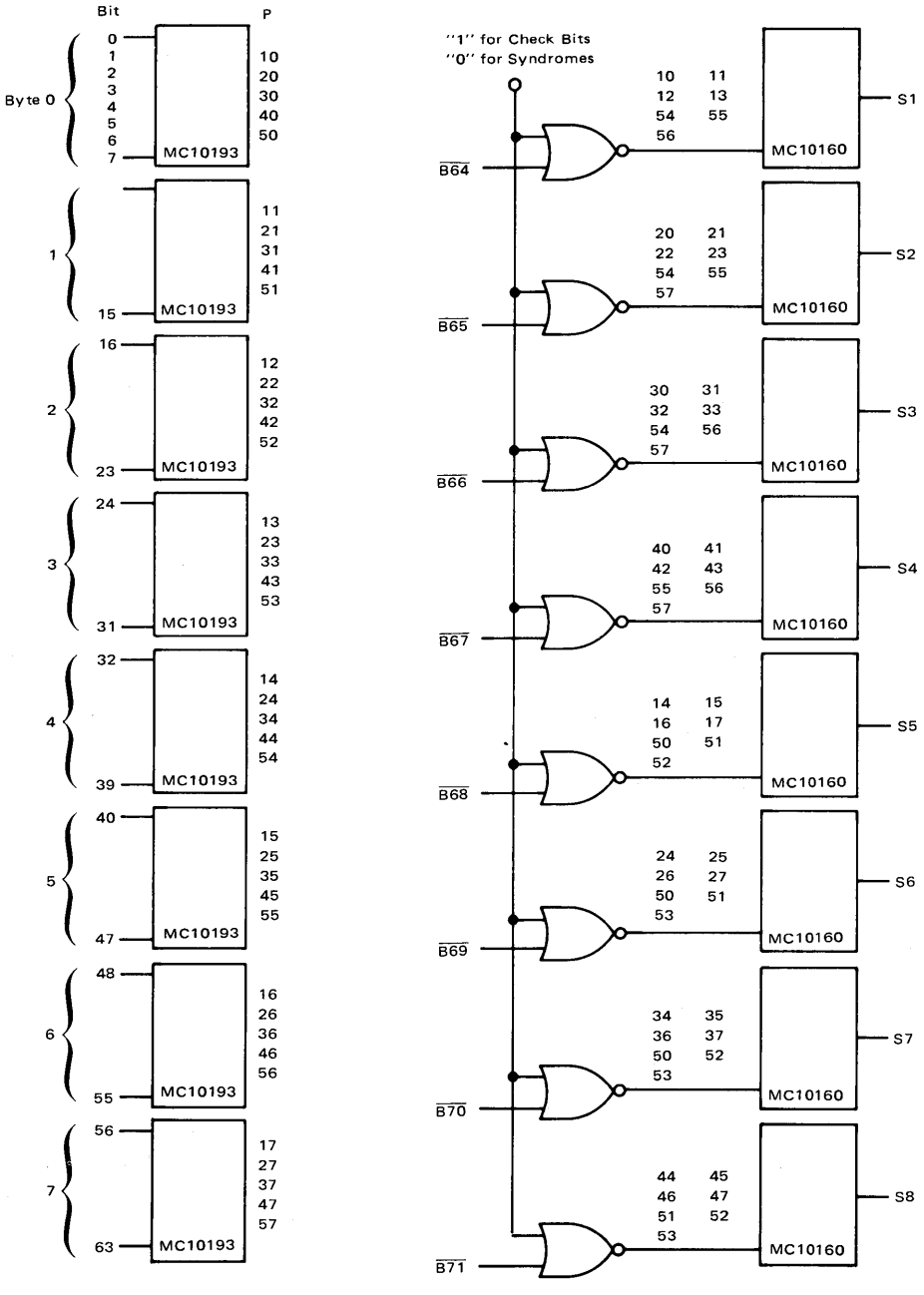


FIGURE 6 — SYNDROME AND CHECK BIT GENERATOR, M2 PATTERN



MOTOROLA

MC10164

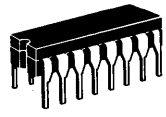
8-LINE MULTIPLEXER

The MC10164 is a high speed, low power eight-channel data selector which routes data present at one-of-eight inputs to the output. The data is routed according to the three bit code present on the address inputs. An enable input is provided for easy bit expansion.

P_D = 310 mW typ/pkg (No Load)
t_{pd} = 3.0 ns typ (Data to Output)
t_r, t_f = 2.0 ns typ (20%–80%)

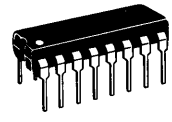
MECL 10K SERIES

8-LINE MULTIPLEXER

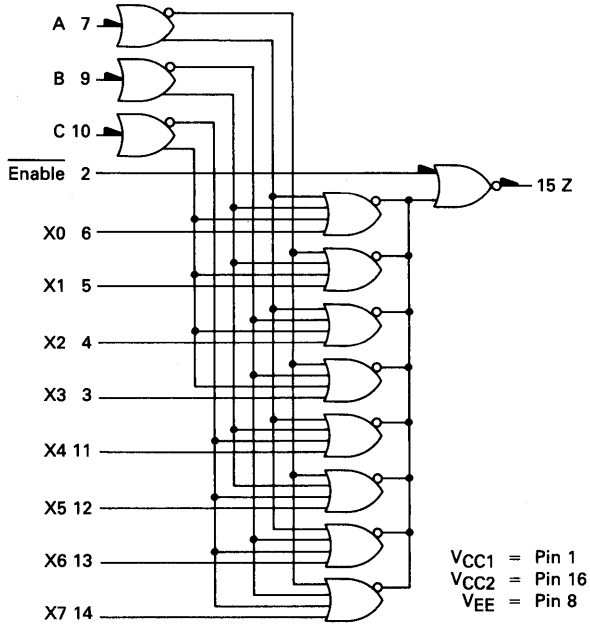


L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648



LOGIC DIAGRAM

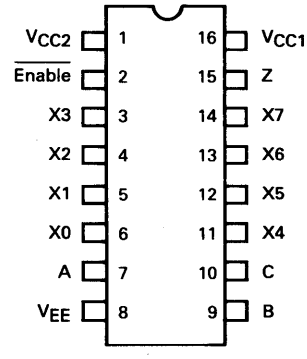


TRUTH TABLE

	ADDRESS INPUTS			
ENABLE	C	B	A	Z
L	L	L	L	X0
L	L	L	H	X1
L	L	H	L	X2
L	L	H	H	X3
L	H	L	L	X4
L	H	L	H	X5
L	H	H	L	X6
L	H	H	H	X7
H	ϕ	ϕ	ϕ	L

ϕ = Don't Care

PIN ASSIGNMENT



ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established in an ambient temperature of 25°C, while the circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown for only one input, or for one set of input conditions. Other inputs tested in the same manner.

@Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

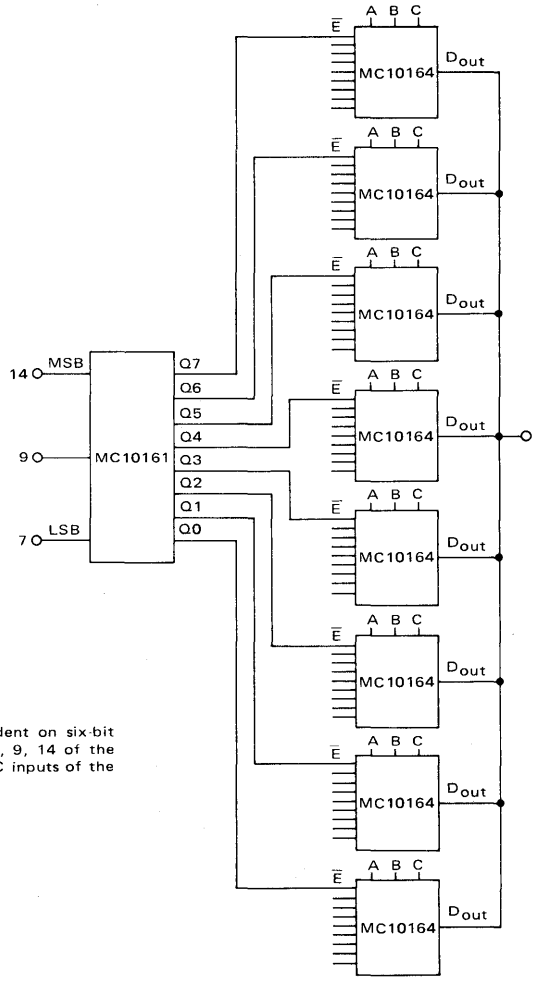
Characteristic	Symbol	Pin Under Test	MC10164 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	83	–	60	75	–	83	mAdc	–	–	–	–	8	1,16
Input Current	$I_{in\ H}$	2	–	425	–	–	265	–	265	μAdc	4	–	–	–	8	1,16
	$I_{in\ L}$	4	0.5	–	0.5	–	–	0.3	–	μAdc	–	4	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	15	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	4,9	–	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	15	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	9	–	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	15	-1.080	–	-0.980	–	–	-0.910	–	Vdc	4,9	–	–	2	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	15	–	-1.655	–	–	-1.630	–	-1.595	Vdc	9	–	–	2	8	1,16
Switching Times (50 Ω Load)											+1.11 V		Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{4+15+}	15	1.5	4.7	1.5	3.0	4.5	1.6	4.8	ns	9	–	4	15	8	1,16
	t_{4-15-}	15	1.5	4.7	1.5	3.0	4.5	1.6	4.8		9	–	4			
	t_{7+15+}	15	1.9	6.3	2.0	4.0	6.0	2.2	6.5		5	–	7			
	t_{7-15-}	15	1.9	6.3	2.0	4.0	6.0	2.2	6.5		5	–	7			
	t_{2+15-}	15	0.9	3.3	1.0	2.0	2.9	1.0	3.1		7,5	–	2			
	t_{2-15+}	15			1.0		2.9	1.0	3.1		7,5	–	2			
Rise Time (20% to 80%)	t^+	15			1.1		3.3	1.2	3.6		9	–	4			
Fall Time (20% to 80%)	t^-	15			1.1		3.3	1.2	3.6		9	–	4			

APPLICATION INFORMATION

The MC10164 can be used wherever data multiplexing or parallel to serial conversion is desirable. Full parallel gating permits equal delays through any data path. The output of the MC10164 incorporates a buffer gate with eight data inputs and an enable. A high level on the enable forces the output low. The MC10164 can be connected directly to a data bus, due to its open emitter output and output enable.

Figure one illustrates how a 1-of-64 line multiplexer can be built with eight MC10164's wire ORed at their outputs and one MC10161 to drive the enables on each multiplexer, without speed degradation over a single MC10164 being experienced.

FIGURE 1 – 1-OF-64 LINE MULTIPLEXER



The Bit chosen is dependent on six-bit code present on inputs 7, 9, 14 of the MC10161 and the A, B, C inputs of the MC10164.

MOTOROLA

MC10165

8-INPUT PRIORITY ENCODER

The MC10165 is a device designed to encode eight inputs to a binary coded output. The output code is that of the highest order input. Any input of lower priority is ignored. Each output incorporates a latch allowing synchronous operation. When the clock is low the outputs follow the inputs and latch when the clock goes high. This device is very useful for a variety of applications in checking system status in control processors, peripheral controllers, and testing systems.

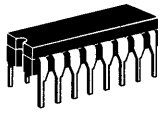
The input is active when high, (e.g., the three binary outputs are low when input D0 is high). The Q3 output is high when any input is high. This allows direct extension into another priority encoder when more than eight inputs are necessary. The MC10165 can also be used to develop binary codes from random logic inputs, for addressing ROMs, RAMs, or for multiplexing data.

P_D = 545 mW typ/pkg (No Load)
t_{pd} = 4.5 ns typ (Data to Output)
t_r, t_f = 2.0 ns typ (2%–80%)

MECL 10K SERIES

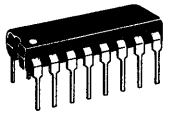
8-INPUT PRIORITY ENCODER MC10165

3



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

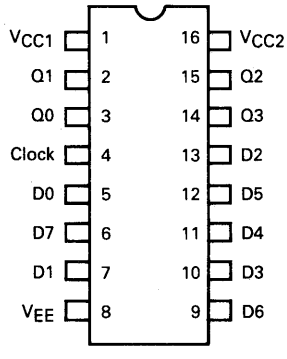


TRUTH TABLE

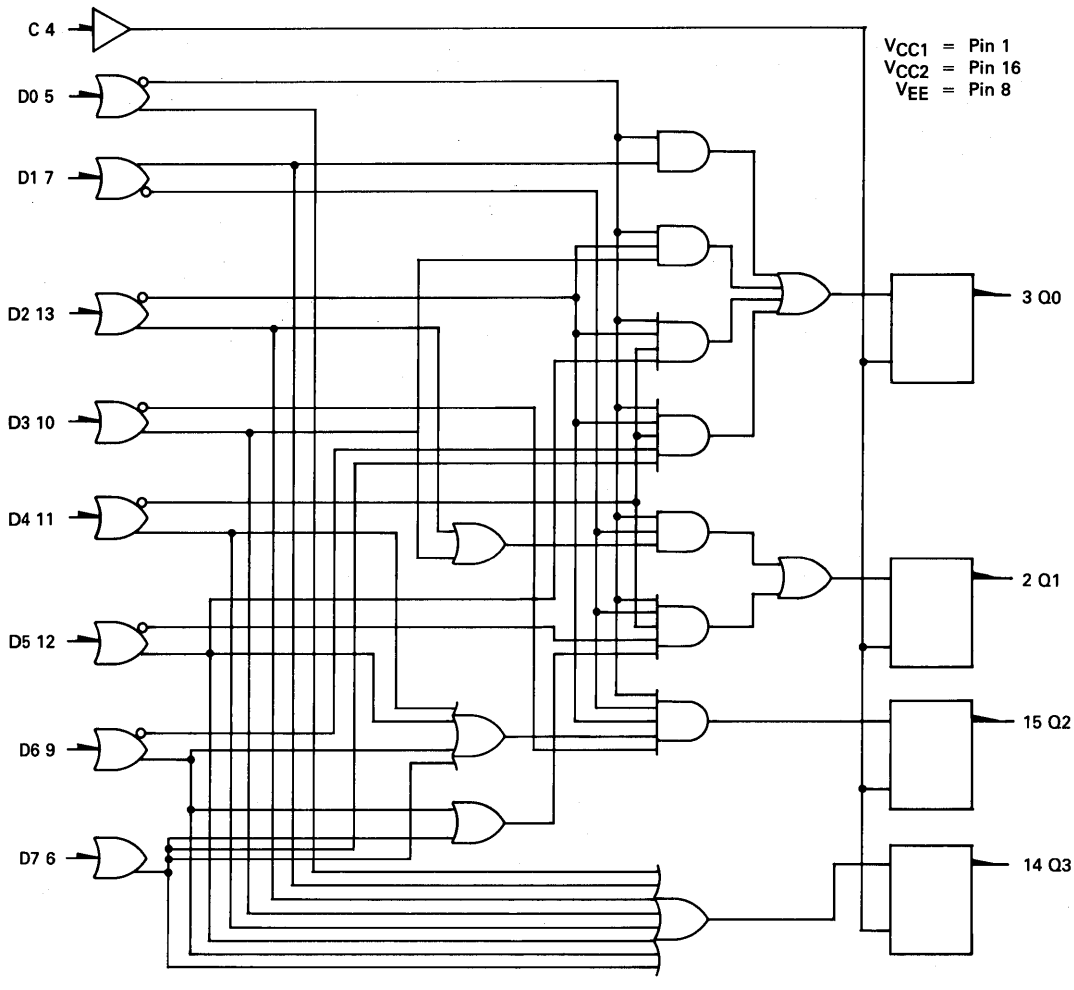
DATA INPUTS								OUTPUTS			
D0	D1	D2	D3	D4	D5	D6	D7	Q3	Q2	Q1	Q0
H	ϕ	ϕ	ϕ	ϕ	ϕ	ϕ	ϕ	H	L	L	L
L	H	ϕ	ϕ	ϕ	ϕ	ϕ	ϕ	H	L	L	H
L	L	H	ϕ	ϕ	ϕ	ϕ	ϕ	H	L	H	L
L	L	L	H	ϕ	ϕ	ϕ	ϕ	H	L	H	H
L	L	L	L	H	ϕ	ϕ	ϕ	H	H	L	L
L	L	L	L	L	H	ϕ	ϕ	H	H	L	H
L	L	L	L	L	L	H	ϕ	H	H	H	L
L	L	L	L	L	L	L	H	H	H	H	H
L	L	L	L	L	L	L	L	L	L	L	L

ϕ = Don't Care

PIN ASSIGNMENT



LOGIC DIAGRAM



Numbers at ends of terminals denote pin numbers for L and P packages.
Numbers in parenthesis denote pin numbers for F package.

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established in an ambient temperature of 25°C, while the circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown for only one input, or for one set of input conditions. Other inputs tested in the same manner.

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10165 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	144	–	105	131	–	144	mAdc	–	–	–	–	8	1,16
Input Current	$I_{in\ H}$	4	–	390	–	–	245	–	245	μAdc	4	–	–	–	8	1,16
		5	–	350	–	–	220	–	220	μAdc	5 ①	–	–	–	8	1,16
	$I_{in\ L}$	4	0.5	–	0.5	–	–	0.3	–	μAdc	–	4	–	–	8	1,16
		5	0.5	–	0.5	–	–	0.3	–	μAdc	–	5①	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	6	4	–	–	8	1,16
		3	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700				–	–		
		14	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700				–	–		
		15	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700				–	–		
Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	–	4	–	–	8	1,16
		3	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615		–		–	–		
		14	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615		–		–	–		
		15	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615		–		–	–		
Logic "1" Threshold Voltage	V_{OHA}	2	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	4	6	–	8	1,16
		3	-1.080	–	-0.980	–	–	-0.910	–		–			–		
		14	-1.080	–	-0.980	–	–	-0.910	–		–			–		
		15	-1.080	–	-0.980	–	–	-0.910	–		–			–		
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	4	–	6	8	1,16
		3	–	-1.655	–	–	-1.630	–	-1.595		–		–			
		14	–	-1.655	–	–	-1.630	–	-1.595		–		–			
		15	–	-1.655	–	–	-1.630	–	-1.595		–		–			
Switching Times (50-ohm Load)										Unit	+1.11 V	+0.31 V	Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay Data Input	t_{5+14+}	14	2.0	7.0	3.0	–	7.0	2.0	8.0	ns	–	4	5	14	8	1,16
	t_{5-14-}	14				–					–		5	14		
	t_{7+3+}	3				–					–		7	3		
	t_{11+15+}	15				–					–		11	15		
	t_{13+2+}	2				–					–		13	2		
Clock Input	t_{4-3+}	3 ②	1.5	4.5	2.0	–	4.0	1.5	4.5		7	–	4	3		
	t_{4-3-}	3 ③				–					–	–		3		
	t_{4-14+}	14 ②				–					7	–		14		
	t_{4-14-}	14 ③				–					–	–		14		
Setup Time	$t_{setup\ H}$	3	6.0	–	6.0	3.4	–	6.0	–		–	–	4,7	3		
	$t_{setup\ L}$		6.0	–	6.0	3.0	–	6.0	–		–	–				
Hold Time	$t_{hold\ H}$		1.0	–	1.0	-2.3	–	1.0	–		–	–				
	$t_{hold\ L}$		1.0	–	1.0	-2.7	–	1.0	–		–	–				
Rise Time (20% to 80%)	t_{3+}		1.1	3.5	1.1	2.0	3.3	1.1	3.5		–	4	7			
Fall Time (20% to 80%)	t_{3-}		1.1	3.5	1.1	2.0	3.3	1.1	3.5		–	4	7			

① The same limit applies for all D type input pins. To test input currents for other D inputs, individually apply proper voltage to pin under test.
② Output latched to low state prior to test.
③ Output latched to high state prior to test.

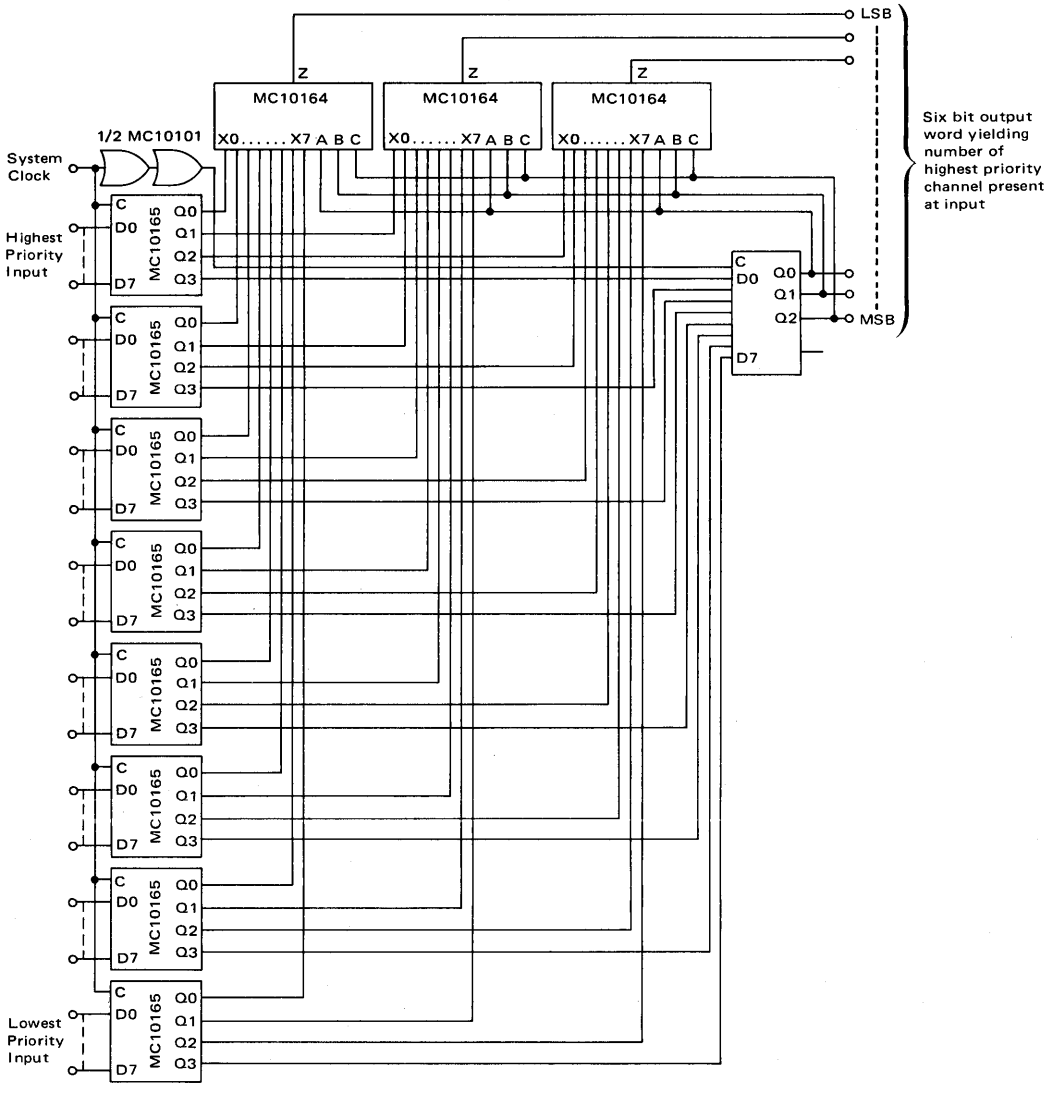
* To preserve reliable performance, the MC10165P (plastic-packaged device only) is to be operated in ambient temperatures above 70°C only when 500 lfpm blown air or equivalent heat sinking is provided.

3

APPLICATION INFORMATION

A typical application of the MC10165 is the decoding of system status on a priority basis. A 64 line priority encoder is shown in the figure below. System status lines are connected to this encoder such that, when a given condition exists, the respective input will be at a logic high level. This scheme will select the one of 64 different system conditions, as represented at the encoder inputs, which has priority in determining the next system operation to be performed. The binary code showing the address of the highest priority input present will appear at the encoder outputs to control other system logic functions.

64-LINE PRIORITY ENCODER



MOTOROLA

MC10166

5-BIT MAGNITUDE COMPARATOR

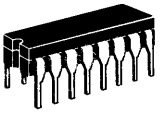
The MC10166 is a high speed expandable 5-bit comparator for comparing the magnitude of two binary words. Two outputs are provided: A < B and A > B. A = B can be obtained by NORing the two outputs with an additional gate. A high level on the enable function forces both outputs low. Multiple MC10166s may be used for larger word comparisons.

P_D = 440 mW typ/pkg (No Load)
t_{pd} = Data to output 6.0 ns typ
$\overline{E}$ to output 2.5 ns typ
t_r, t_f = 2.0 ns typ (20%–80%)

MECL 10K SERIES

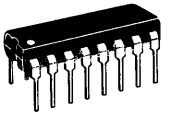
5-BIT MAGNITUDE COMPARATOR

3

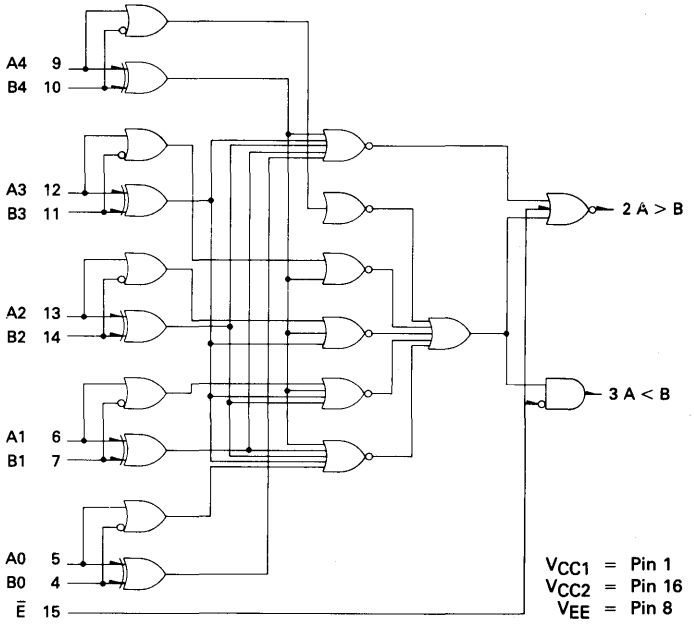


L SUFFIX
CERAMIC PACKAGE
CASE 620

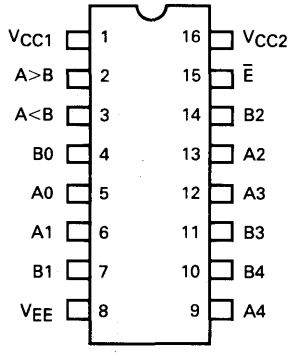
P SUFFIX
PLASTIC PACKAGE
CASE 648



LOGIC DIAGRAM



PIN ASSIGNMENT



TRUTH TABLE

Inputs			Outputs	
$\overline{E}$	A	B	A < B	A > B
H	X	X	L	L
L	Word A = Word B		L	L
L	Word A > Word B		L	H
L	Word A < Word B		H	L

ELECTRICAL CHARACTERISTICS

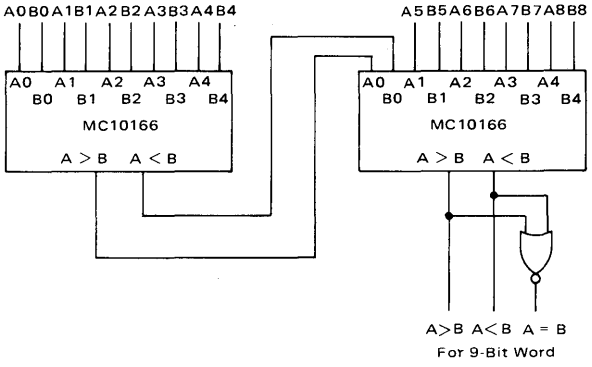
Each MECL 10,000 series has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown for only selected inputs and outputs. Other inputs and outputs are tested in a similar manner.

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10166 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	117	–	85	106	–	117	mAdc	–	4,7,10,11,14	–	–	8	1,16
Input Current	I_{inH}	5	–	350	–	–	220	–	220	μAdc	5	–	–	–	8	1,16
	I_{inL}	5	0.5	–	0.5	–	–	0.3	–	μAdc	–	5	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	5	–	–	–	8	1,16
		3	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	4	–	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	5,15	–	–	–	8	1,16
		3	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	4,15	–	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	2	-1.080	–	-0.980	–	–	-0.910	–	Vdc	5	–	–	15	8	1,16
		3	-1.080	–	-0.980	–	–	-0.910	–	Vdc	4	–	–	15	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.655	–	–	-1.630	–	-1.595	Vdc	5	–	15	–	8	1,16
		3	–	-1.655	–	–	-1.630	–	-1.595	Vdc	4	–	15	–	8	1,16
Switching Times (50 Ω Load)											+1.11 V		Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay Data to Output	t_{9+2+}	2	1.0	8.0	1.0	6.0	7.6	1.0	8.4	ns	–	–	9	2	8	1,16
	t_{9-2-}	2	↓	↓	↓	↓	↓	↓	↓	↓	–	–	9	2	↓	↓
	t_{11-2+}	2	↓	↓	↓	↓	↓	↓	↓	↓	12	–	11	2	↓	↓
	t_{11+2-}	2	↓	↓	↓	↓	↓	↓	↓	↓	12	–	11	2	↓	↓
	t_{7+3+}	3	↓	↓	↓	↓	↓	↓	↓	↓	6	–	7	3	↓	↓
	t_{7-3-}	3	↓	↓	↓	↓	↓	↓	↓	↓	6	–	7	3	↓	↓
Enable to Output	t_{15-3+}	3	↓	3.8	↓	2.5	3.6	↓	4.0	↓	10	–	15	3	↓	↓
	t_{15+3-}	3	↓	3.8	↓	2.5	3.6	↓	4.0	↓	10	–	15	3	↓	↓
Rise Time (20% to 80%)	t_{2+}	2	↓	3.6	1.1	2.0	3.5	1.1	3.8	↓	–	–	9	2	↓	↓
Fall Time (20% to 80%)	t_{2-}	2	↓	3.6	1.1	2.0	3.5	1.1	3.8	↓	–	–	9	2	↓	↓

APPLICATION INFORMATION

FIGURE 1 — 9-BIT MAGNITUDE COMPARATOR



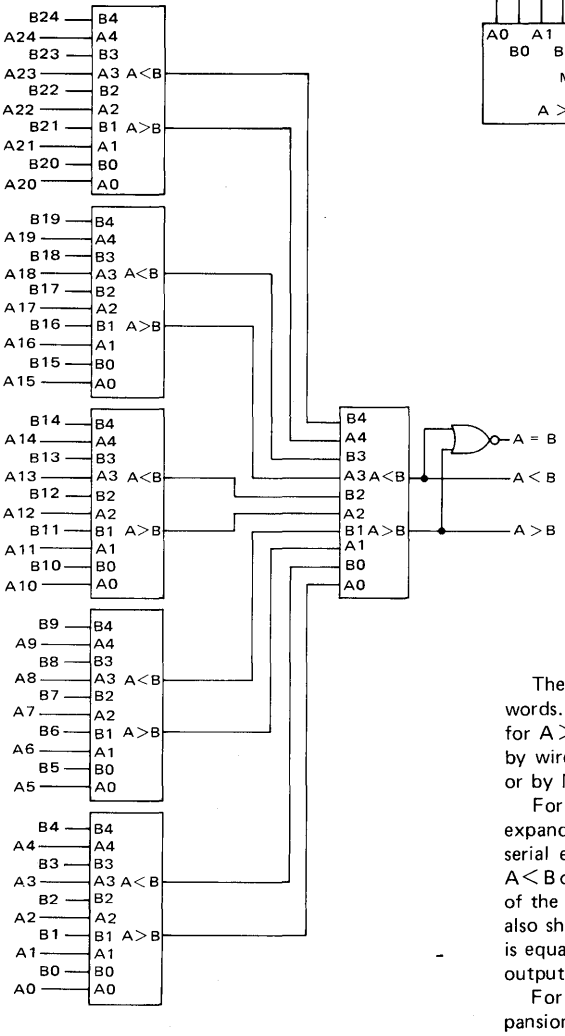


FIGURE 2 — 25-BIT MAGNITUDE COMPARATOR

The MC10166 compares the magnitude of two 5-bit words. Two outputs are provided which give a high level for A > B and A < B. The A = B function can be obtained by wire-ORing these outputs (a low level indicates A = B) or by NORing the outputs (a high level indicates A = B).

For longer word lengths, the MC10166 can be serially expanded or cascaded. Figure 1 shows two devices in a serial expansion for a 9-bit word length. The A > B and A < B outputs are fed to the A0 and B0 inputs respectively of the next device. The connection for an A = B output is also shown. The worst case delay time of serial expansion is equal to the number of comparators times the data-to-output delay.

For shorter delay times than possible with serial expansion, devices can be cascaded. Figure 2 shows a 25-bit cascaded comparator whose worst case delay is two data-to-output delays. The cascaded scheme can be extended to longer word lengths.

MOTOROLA

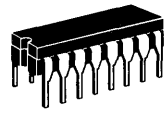
MC10168

MECL 10K SERIES

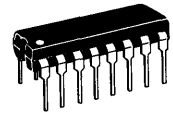
QUAD LATCH

The MC10168 is a Quad Latch with common clocking to all four latches. Separate output enabling gates are provided for each latch, allowing direct wiring to a bus. When the clock is high, outputs will follow the D inputs. Information is latched on the negative-going transition of the clock.

P_D = 310 mW typ/pkg (No Load)
t_{pd} = $\overline{G}$ to Q = 2 ns typ
D to Q = 3 ns typ
C to Q = 4 ns typ
t_r, t_f = 2.0 ns typ (20%–80%)

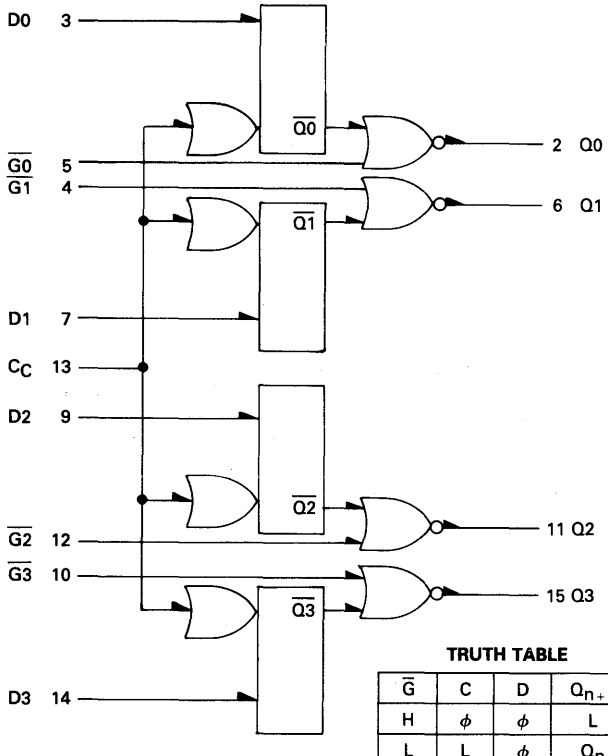


L SUFFIX
CERAMIC PACKAGE
CASE 620



P SUFFIX
PLASTIC PACKAGE
CASE 648

LOGIC DIAGRAM



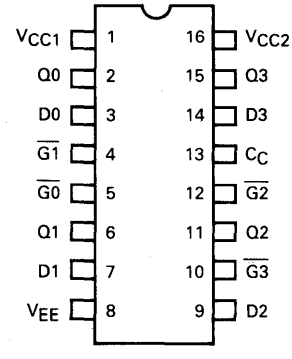
V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

TRUTH TABLE

$\overline{G}$	C	D	Q_{n+1}
H	ϕ	ϕ	L
L	L	ϕ	Q_n
L	H	L	L
L	H	H	H

ϕ = don't care

PIN ASSIGNMENT



ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown for only selected inputs and outputs. The other inputs and outputs are tested in the same manner.

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
-30°C	-1.890	-1.890	-1.205	-1.500	-5.2
+25°C	-1.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10168 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	82	–	60	75	–	82	mAdc	–	–	–	–	8	1,16
Input Current	I_{inH}	3,7,9,14	–	390	–	–	245	–	245	μAdc	*	–	–	–	8	1,16
		4,5,10,12	–	425	–	–	265	–	265	↓	*	–	–	–	↓	↓
		13	–	460	–	–	290	–	290	↓	13	–	–	–	↓	↓
	I_{inL}	*	0.5	–	0.5	–	–	0.3	–	μAdc	–	*	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	3,13	–	–	–	8	1,16
		6	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	7,13	–	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	3,5	–	–	–	8	1,16
		6	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	4,7	–	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	2	-1.080	–	-0.980	–	–	-0.910	–	Vdc	13	–	3	–	8	1,16
		6	-1.080	–	-0.980	–	–	-0.910	–	Vdc	13	–	7	–	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.655	–	–	-1.630	–	-1.595	Vdc	13	–	–	3	8	1,16
		6	–	-1.655	–	–	-1.630	–	-1.595	Vdc	13	–	–	7	8	1,16
Switching Times (50 Ω Load)											+1.11 V		Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay: Data	t_{3+2+}	2	1.0	5.6	1.0	3.0	5.4	1.1	5.9	ns	–	–	3	2	8	1,16
Gate	t_{5-2+}	2	↓	3.2	↓	2.0	3.1	1.0	3.4	↓	–	–	5	2	↓	↓
Clock	t_{13+2+}	2	↓	5.8	↓	4.0	5.6	1.2	6.2	↓	–	–	13	2	↓	↓
Setup Time	t_{3+13+}	2	2.5	–	2.5	–	–	2.5	–	↓	–	–			↓	↓
Hold Time	t_{13+3+}	2	1.0	–	1.0	–	–	1.0	–	↓	–	–			↓	↓
Rise Time (20% to 80%)	t_{2+}	2	↓	3.6	1.1	2.0	3.5	1.1	3.8	↓	–	–	3	2	↓	↓
Fall Time (20% to 80%)	t_{2-}	2	↓	3.6	1.1	2.0	3.5	1.1	3.8	↓	–	–	3	2	↓	↓

*Individually test each input applying V_{IH} or V_{IL} to input under test.

MOTOROLA

MC10170

9 + 2-BIT PARITY GENERATOR-CHECKER

The MC10170 is a 11-bit parity circuit, which is segmented into 9 data bits and 2 control bits.

Output A generates odd parity on 9 bits; that is, Output A goes high for an odd number of high logic levels on the bit inputs in only 2 gate delays.

The Control Inputs can be used to expand parity to larger numbers of bits with minimal delay or can be used to generate even parity. To expand parity to larger words, the MC10170 can be used with the MC10160 or other MC10170's. The MC10170 can generate both even and odd parity.

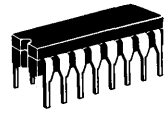
P_D = 300 mW typ/pkg (No Load)

t_{pd} = 2.5 ns typ (Control Inputs to B Output)
4.0 ns typ (Data Inputs to A Output)
6.0 ns typ (Data Inputs to B Output)

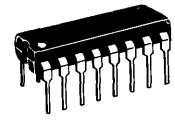
t_r, t_f = 2.0 ns typ (20%–80%)

MECL 10K SERIES

9 + 2-BIT PARITY GENERATOR-CHECKER

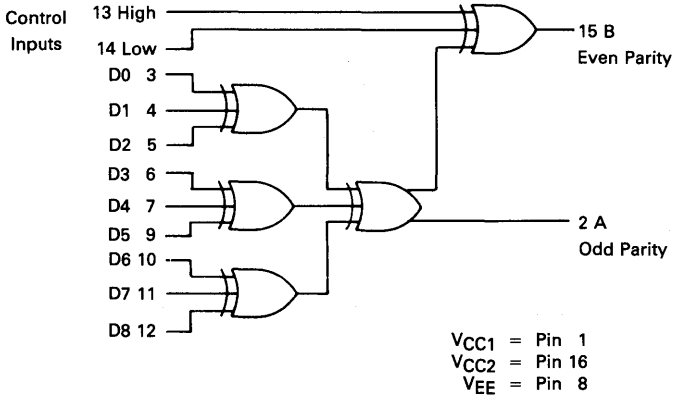


L SUFFIX
CERAMIC PACKAGE
CASE 620



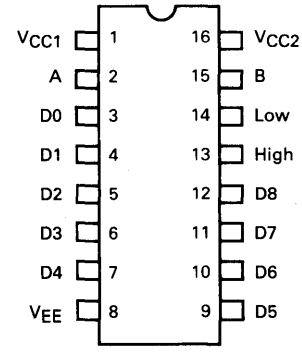
P SUFFIX
PLASTIC PACKAGE
CASE 648

LOGIC DIAGRAM



INPUTS	OUTPUTS	
Sum of D Inputs at High Level	Odd Parity Output A	Even Parity Output B
Even	Low	High
Odd	High	Low

PIN ASSIGNMENT



ELECTRICAL CHARACTERISTICS

Each MECI 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown for only selected inputs and outputs. Other inputs and outputs tested in the same manner.

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10170 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	78	–	57	71	–	78	mAdc	–	–	–	–	–	1,16
Input Current	I_{inH}	3	–	350	–	–	200	–	220	µAdc	3	–	–	–	8	1,16
		5	–	350	–	–	220	–	220	µAdc	5	–	–	–	8	1,16
	I_{inL}	3	0.5	–	0.5	–	–	0.3	–	µAdc	–	3	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	3,4,5	–	–	–	8	1,16
		15	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	14	–	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	4,5	–	–	–	8	1,16
		15	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	13,14	–	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	2	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	5	–	8	1,16
		15	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	13	–	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	–	5	8	1,16
		15	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	–	13	8	1,16
Switching Times (50-ohm Load) Propagation Delay													Pulse In	Pulse Out	-3.2 V	+2.0 V
	t_{13+15+}	15	1.5	4.2	1.5	2.5	4.0	1.5	4.4	ns	–	–	13	15	8	1,16
	t_{14-15-}	15	1.5	4.2	1.5	2.5	4.0	1.5	4.4		–	–	14	15		
	t_{3+2-}	2	2.0	6.6	2.0	4.0	6.0	2.0	6.6		–	–	3	2		
	t_{3-15+}	15	4.0	9.5	4.0	6.0	8.8	4.0	9.5		–	–	3	15		
Rise Time (20% to 80%)	t_{2+}	2	1.5	4.3	1.5	2.0	3.9	1.5	4.3	ns	–	–	3	2	8	1,16
Fall Time (20% to 80%)	t_{2-}	2	1.5	4.3	1.5	2.0	3.9	1.5	4.3	ns	–	–	3	2	8	1,16

MOTOROLA

MC10171

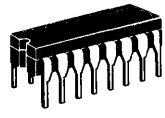
BINARY TO 1-4-DECODER (LOW)

The MC10171 is a binary coded 2 line to dual 4 line decoder with selected outputs low. With either $\overline{E}0$ or $\overline{E}1$ high, the corresponding selected 4 outputs are high. The common enable $\overline{E}$, when high, forces all outputs high.

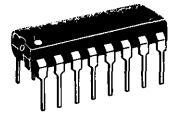
P_D = 325 mW typ/pkg (No Load)
t_{pd} = 4.0 ns typ
t_r, t_f = 2.0 ns typ (20%–80%)

MECL 10K SERIES

BINARY TO 1-4-DECODER (LOW)

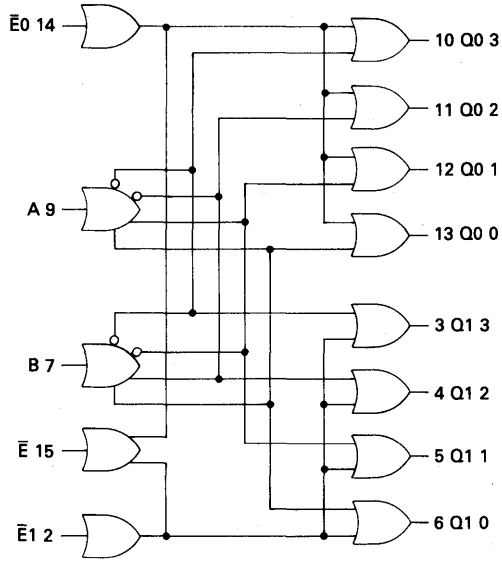


L SUFFIX
CERAMIC PACKAGE
CASE 620



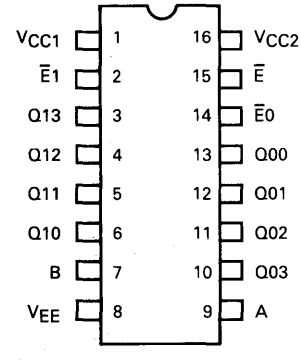
P SUFFIX
PLASTIC PACKAGE
CASE 648

LOGIC DIAGRAM



V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

PIN ASSIGNMENT



TRUTH TABLE

ENABLE INPUTS			INPUTS		OUTPUTS							
$\overline{E}$	$\overline{E}0$	$\overline{E}1$	A	B	Q10	Q11	Q12	Q13	Q00	Q01	Q02	Q03
L	L	L	L	L	L	H	H	H	L	H	H	H
L	L	L	L	H	H	L	H	H	H	L	H	H
L	L	L	H	L	H	H	L	H	H	H	L	H
L	L	L	H	H	H	H	H	L	H	H	H	L
L	L	H	L	L	H	H	H	H	L	H	H	H
L	H	L	L	L	L	H	H	H	H	H	H	H
H	ϕ	ϕ	ϕ	ϕ	H	H	H	H	H	H	H	H

ϕ = Don't Care

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test Procedures are shown only for selected inputs and outputs. Other inputs and outputs are tested in a similar manner.

@ Test Temperature	TEST VOLTAGE VALUES (Volts)				
	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10171 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	85	–	65	77	–	85	mAdc	2,7,9,14,15	–	–	–	8	1,16
Input Current	I_{inH}	14	–	350	–	–	220	–	220	μAdc	14	–	–	–	8	1,16
	I_{inL}	14	0.5	–	0.5	–	–	0.3	–	μAdc	–	14	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	6	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	15	–	–	–	8	1,16
		13	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	15	–	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	13	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	–	2,7,9,14,15	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	6	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	15	–	8	1,16
		13	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	15	–	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	6	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	2,9,14,15	–	7	8	1,16
		13	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	2,7,14,15	–	9	8	1,16
Switching Times (50 Ω Load)												+0.31 V	Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{7+6+}	6	1.5	6.2	1.5	4.0	6.0	1.5	6.4	ns	–	2,9,14,15	7	6	8	1,16
	t_{7-6-}	6	↓	↓	↓	↓	↓	↓	↓	↓	–	↓	↓	6	↓	↓
	t_{7+13+}	13	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	13	↓	↓
	t_{7-13-}	13	↓	↓	↓	↓	↓	↓	↓	↓	–	↓	↓	13	↓	↓
	t_{6+}	6	1.0	3.3	1.1	2.0	3.3	1.1	3.4	↓	–	–	↓	6	↓	↓
Rise Time (20% to 80%)	t_{13+}	13	↓	↓	↓	↓	↓	↓	↓	↓	–	–	↓	13	↓	↓
	t_{6-}	6	↓	↓	↓	↓	↓	↓	↓	↓	–	–	↓	6	↓	↓
Fall Time (20% to 80%)	t_{13-}	13	↓	↓	↓	↓	↓	↓	↓	↓	–	–	↓	13	↓	↓

MOTOROLA

MC10172

DUAL BINARY TO 1-4-DECODER (HIGH)

The MC10172 is a binary-coded 2 line to dual 4 line decoder with selected outputs high. With either $\overline{E}0$ or $\overline{E}1$ low, the corresponding selected 4 outputs are low. The common enable $\overline{E}$, when high, forces all outputs low.

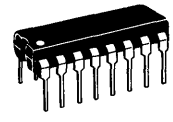
P_D = 325 mW typ/pkg (No Load)
t_{pd} = 4.0 ns typ
t_r, t_f = 2.0 ns typ (20%–80%)

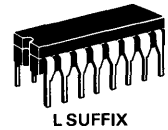
3

MECL 10K SERIES

DUAL BINARY TO 1-4-DECODER (HIGH)

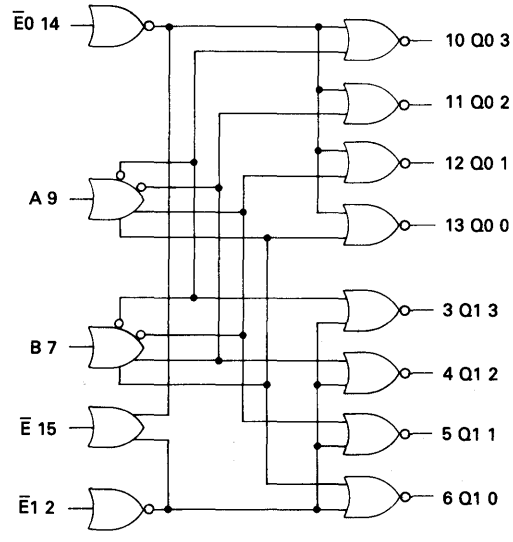
P SUFFIX
PLASTIC PACKAGE
CASE 648





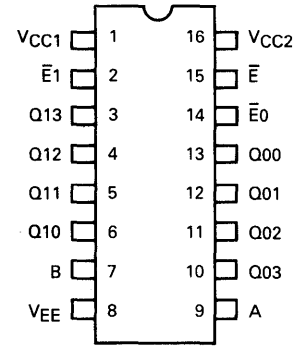
L SUFFIX
CERAMIC PACKAGE
CASE 620

LOGIC DIAGRAM



V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

PIN ASSIGNMENT



TRUTH TABLE

$\overline{E}$	$\overline{E}1$	$\overline{E}0$	A	B	Q1 0	Q1 1	Q1 2	Q1 3	Q0 0	Q0 1	Q0 2	Q0 3
L	H	H	L	L	H	L	L	L	H	L	L	L
L	H	H	L	H	L	H	L	L	L	H	L	L
L	H	H	H	L	L	L	H	L	L	L	H	L
L	H	H	H	H	L	L	L	H	L	L	L	H
L	L	H	L	L	L	L	L	L	H	L	L	L
L	H	L	L	L	H	L	L	L	L	L	L	L
H	ϕ	ϕ	ϕ	ϕ	L	L	L	L	L	L	L	L

ϕ = Don't Care

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown only for selected inputs and outputs. Other inputs and outputs are tested in a similar manner.

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10172 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	85	–	62	77	–	85	mAdc	–	–	–	–	8	1,16
Input Current	I_{inH}	14	–	350	–	–	220	–	220	μAdc	14	–	–	–	8	1,16
	I_{inL}	14	0.5	–	0.5	–	–	0.3	–	μAdc	–	14	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	6	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	2	–	–	–	8	1,16
		13	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	14	–	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	13	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	15	2,7,9,14	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	6	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	2	–	8	1,16
		13	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	14	–	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	6	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	2,9,14	–	7	8	1,16
		13	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	2,7,14	–	9	8	1,16
Switching Times (50 Ω Load)											+1.11 V	+0.31 V	Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{7+6-}	6	1.5	6.2	1.5	4.0	6.0	1.5	6.4	ns	2	9,14	7	6	8	1,16
	t_{7-6+}	6	↓	↓	↓	↓	↓	↓	↓	↓	2	9,14	↓	6	↓	↓
	t_{7+13-}	13	↓	↓	↓	↓	↓	↓	↓	↓	14	2,9	↓	13	↓	↓
	t_{7-13+}	13	↓	↓	↓	↓	↓	↓	↓	↓	14	2,9	↓	13	↓	↓
Rise Time (20% to 80%)	t_{6+}	6	1.0	3.3	1.1	2.0	3.3	1.1	3.4	↓	2	9,14	↓	6	↓	↓
	t_{13+}	13	↓	↓	↓	↓	↓	↓	↓	↓	14	2,9	↓	13	↓	↓
Fall Time (20% to 80%)	t_{6-}	6	↓	↓	↓	↓	↓	↓	↓	↓	2	9,14	↓	6	↓	↓
	t_{13-}	13	↓	↓	↓	↓	↓	↓	↓	↓	14	2,9	↓	13	↓	↓

MOTOROLA

MC10173

QUAD 2-INPUT MULTIPLEXER/LATCH

The MC10173 is a quad two channel multiplexer with latch. It incorporates common clock and common data select inputs. The select input determines which data input is enabled. A high (H) level enables data inputs D00, D10, D20, and D30 and a low (L) level enables data inputs D01, D11, D21, D31. Any change on the data input will be reflected at the outputs while the clock is low. The outputs are latched on the positive transition of the clock. While the clock is in the high state, a change in the information present at the data inputs will not affect the output information.

P_D = 275 mW typ/pkg (No Load)
t_{pd} = 2.5 ns typ
t_r, t_f = 2.0 ns typ (20%–80%)

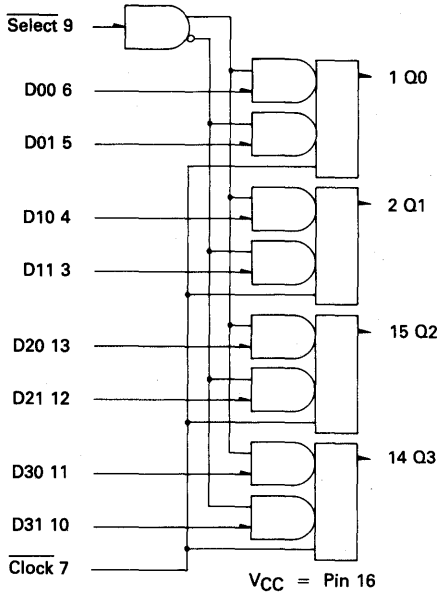
MECL 10K SERIES

QUAD 2-INPUT MULTIPLEXER/LATCH

P SUFFIX
PLASTIC PACKAGE
CASE 648

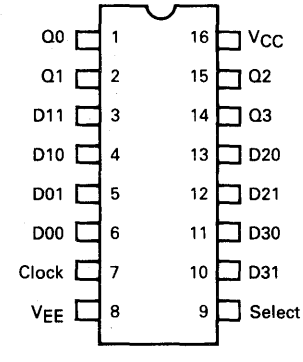
L SUFFIX
CERAMIC PACKAGE
CASE 620

LOGIC DIAGRAM



V_{CC} = Pin 16
V_{EE} = Pin 8

PIN ASSIGNMENT



TRUTH TABLE

SELECT	CLOCK	$Q0_{n+1}$
H	L	D00
L	L	D01
ϕ	H	$Q0_n$

ϕ = Don't Care

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts.

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
−30°C	−0.890	−1.890	−1.205	−1.500	−5.2
+25°C	−0.810	−1.850	−1.105	−1.475	−5.2
+85°C	−0.700	−1.825	−1.035	−1.440	−5.2

Characteristic	Symbol	Pin Under Test	MC10173 Test Limits −30°C Min	−30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	73	–	–	66	–	73	mAdc	–	–	–	–	8	16
Input Current	I_{inH}	5	–	470	–	–	295	–	295	μAdc	5	–	–	–	8	16
		6	–	470	–	–	295	–	295		6	–	–	–	↓	↓
		7	–	400	–	–	250	–	250		7	–	–	–		
		9	–	400	–	–	250	–	250	↓	9	–	–	–		
Input Leakage Current	I_{inL}	All	0.5	–	0.5	–	–	0.3	–	μAdc	–	*	–	–	8	16
Logic "1" Output Voltage	V_{OH}	1	−1.060	−0.890	−0.960	–	−0.810	−0.890	−0.700	Vdc	6,9	7	–	–	8	16
		2	−1.060	−0.890	−0.960	–	−0.810	−0.890	−0.700	Vdc	5	7	–	–	8	16
Logic "0" Output Voltage	V_{OL}	1	−1.890	−1.675	−1.850	–	−1.650	−1.825	−1.615	Vdc	9	7	–	–	8	16
		2	−1.890	−1.675	−1.850	–	−1.650	−1.825	−1.615	Vdc	–	7	–	–	8	16
Logic "1" Threshold Voltage	V_{OHA}	1	−1.080	–	−0.980	–	–	−0.910	–	Vdc	9	7	6	–	8	16
		2	−1.080	–	−0.980	–	–	−0.910	–	Vdc	–	7	5	–	8	16
Logic "0" Threshold Voltage	V_{OLA}	1	–	−1.655	–	–	−1.630	–	−1.595	Vdc	9	7	–	6	8	16
		2	–	−1.655	–	–	−1.630	–	−1.595	Vdc	–	7	–	5	8	16
Switching Times											+1.11 Vdc	+0.31 Vdc	Pulse In	Pulse Out	−3.2 Vdc	+2.0 Vdc
Propagation Delay																
Data Input	t_{6+1+}	1	0.8	3.7	1.0	2.5	3.5	1.1	5.3	ns	9	7	6	1	8	16
	t_{6-1-}		↓	↓	↓	↓	↓	↓	↓		9	↓	6	↓	↓	↓
	t_{5+1+}										–		5			
	t_{5-1-}										–		5			
Clock Input	t_{7-1+}		1.6	7.2	1.6	4.5	6.8	1.4	6.8		–	–	5,7			
	t_{7-1-}		1.6	7.2	1.6	4.5	6.8	1.4	6.8		–	–	5,7			
Select Input	t_{9+1+}		1.1	6.2	1.3	3.5	5.7	1.2	6.7		6	7	9			
	t_{9+1-}										5					
	t_{9-1+}										5					
	t_{9-1-}										6					
Setup Time																
Data Input	t_{setup}		2.0	–	2.0	1.5	–	2.0	–		–	–	5,7			
Select Input	t_{setup}		3.0	–	3.0	2.5	–	3.0	–		6	–	7,9			
Hold Time																
Data Input	t_{hold}		2.5	–	2.5	0.0	–	2.5	–		–	–	5,7			
Select Input	t_{hold}		1.5	–	1.5	-0.5	–	1.5	–		6	–	7,9			
Rise Time (20 to 80%)	t^+		1.2	4.0	1.5	2.0	3.5	1.4	4.0		5	–	7			
Fall Time (20 to 80%)	t^-	↓	1.2	4.0	1.5	2.0	3.5	1.4	4.0	↓	–	–	7	↓	↓	↓

*V_{ILmin} applied to each input pin, one at a time.

MOTOROLA

MC10174

DUAL 4 TO 1 MULTIPLEXER

The MC10174 is a high speed dual channel multiplexer with output enable capability. The select inputs determine one of four active data inputs for each multiplexer. An output enable forces both outputs low when in the high state.

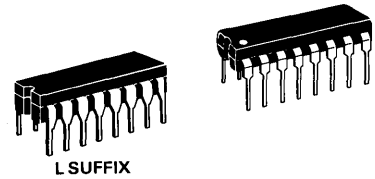
P_D = 305 mW typ/pkg (No Load)
t_{pd} = 3.5 ns typ (Data to output)
t_r, t_f = 2.0 ns typ (20%–80%)

MECL 10K SERIES

DUAL 4 TO 1 MULTIPLEXER

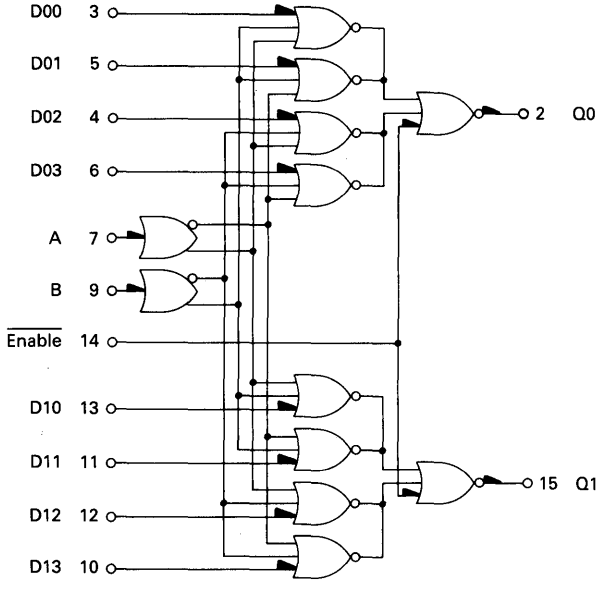
3

P SUFFIX
PLASTIC PACKAGE
CASE 648



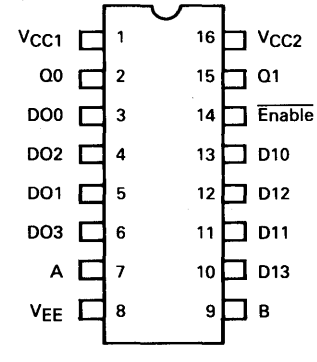
L SUFFIX
CERAMIC PACKAGE
CASE 620

LOGIC DIAGRAM



V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

PIN ASSIGNMENT



TRUTH TABLE

ENABLE	ADDRESS INPUTS		OUTPUTS	
$\overline{E}$	B	A	Q0	Q1
H	ϕ	ϕ	L	L
L	L	L	D00	D10
L	L	H	D01	D11
L	H	L	D02	D12
L	H	H	D03	D13

ϕ = Don't Care

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established in an ambient temperature of 25°C, while the circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown for only one input, or for one set of input conditions. Other inputs tested in the same manner.

@Test Temperature	TEST VOLTAGE VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10174 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	80	–	58	73	80	–	mAdc	–	–	–	–	8	1,16
Input Current	$I_{in\ H}$	4	–	350	–	–	220	–	220	µAdc	4	–	–	–	8	1,16
		14	–	525	–	–	330	–	330		14	–	–	–	8	1,16
	$I_{in\ L}$	4	0.5	–	0.5	–	–	0.3	–	µAdc	–	4	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	15	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	13	–	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	15	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	14	–	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	15	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	13	–	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	15	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	14	–	8	1,16
Switching Times (50 Ω Load)											+1.11 V		Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{13+15+}	15	1.4	4.8	1.5	3.5	4.5	1.4	4.8	ns	–	–	13	15	8	1,16
	t_{13-15-}	15	1.4	4.8	1.5	3.5	4.5	1.4	4.8		–	–	13			
	t_{7+15-}	15	1.9	6.4	2.0	5.0	6.0	2.1	6.4		11	–	7			
	t_{7-15+}	15	1.9	6.4	2.0	5.0	6.0	2.1	6.4		11	–	7			
	t_{14+15-}	15	1.0	3.1	1.0	2.0	2.9	0.9	3.2		13	–	14			
	t_{14-15+}	15		3.1	1.0	2.0	2.9	0.9	3.2			–	14			
Rise Time (20% to 80%)	t+	15		3.4	1.1	2.0	3.3	1.1	3.6			–	14			
Fall Time (20% to 80%)	t-	15		3.4	1.1	2.0	3.3	1.1	3.6			–	14			

MOTOROLA

MC10175

QUINT LATCH

The MC10175 is a high speed, low power quint latch. It features five D type latches with common reset and a common two-input clock. Data is transferred on the negative edge of the clock and latched on the positive edge. The two clock inputs are "OR"ed together.

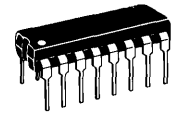
Any change on the data input will be reflected at the outputs while the clock is low. The outputs are latched on the positive transition of the clock. While the clock is in the high state, a change in the information present at the data inputs will not affect the output information. The reset input is enabled only when the clock is in the high state.

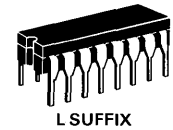
P_D = 400 mW typ/pkg (No Load)
t_{pd} = 2.5 ns typ (Data to Output)
t_r, t_f = 2.0 ns typ (20%–80%)

MECL 10K SERIES

QUINT LATCH

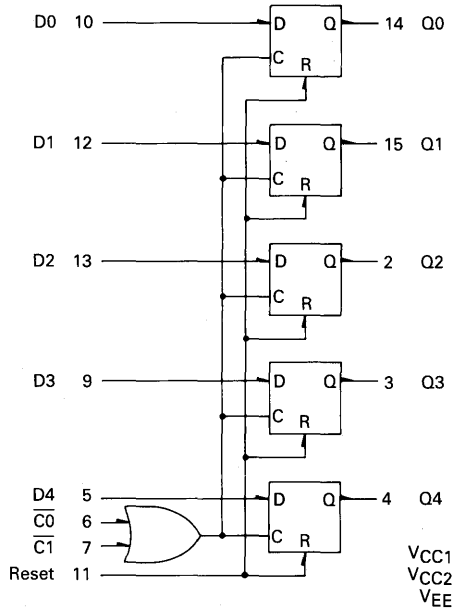
P SUFFIX
PLASTIC PACKAGE
CASE 648





L SUFFIX
CERAMIC PACKAGE
CASE 620

LOGIC DIAGRAM



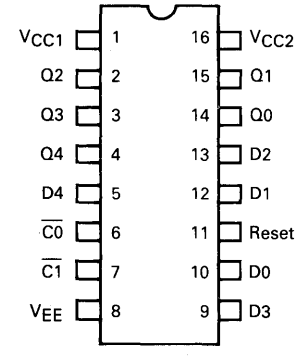
V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

TRUTH TABLE

D	$\overline{C0}$	$\overline{C1}$	Reset	Q_{n+1}
L	L	L	ϕ	L
H	L	L	ϕ	H
ϕ	H	ϕ	L	Q n
ϕ	ϕ	H	L	Q n
ϕ	H	ϕ	H	L
ϕ	ϕ	H	H	L

ϕ = Don't Care

PIN ASSIGNMENT



ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown only for selected inputs and outputs. Other inputs and outputs are tested in a similar manner.

@ Test Temperature	TEST VOLTAGE VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}
−30°C	−0.890	−1.890	−1.205	−1.500	−5.2
+25°C	−0.810	−1.850	−1.105	−1.475	−5.2
+85°C	−0.700	−1.825	−1.035	−1.440	−5.2

Characteristic	Symbol	Pin Under Test	MC10175L Test Limits −30°C Min	−30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	VOLTAGE APPLIED TO PINS LISTED BELOW: $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}	Gnd
Power Supply Drain Current	I_E	8	–	107	–	78	97	–	107	mAdc	–	–	–	–	8	1,16
Input Current	I_{inH}	6	–	460	–	–	290	–	290	µAdc	6	–	–	–		
		7	–	460	–	–	290	–	290		7	–	–	–		
		10	–	460	–	–	290	–	290		10	–	–	–	↓	↓
		11	–	1000	–	–	650	–	650	↓	11	–	–	–		
Input Leakage Current	I_{inL}	All	0.5	–	0.5	–	–	0.3	–	µAdc	–	①	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	14	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	10	6	–	–	8	1,16
		15	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	12	6	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	14	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	–	6,10	–	–	8	1,16
		15	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	–	6,12	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	14	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	6	10	–	8	1,16
		15	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	6	12	–	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	14	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	6	–	10	8	1,16
		15	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	6	–	12	8	1,16
Switching Times											+1.11 Vdc	+0.31 Vdc	Pulse In	Pulse Out	-3.2 Vdc	+2.0 Vdc
Data Input	t_{10+14+}	14	1.0	3.6	1.0	–	3.5	1.0	3.6	ns	–	6,7	10	14	8	1,16
	t_{10-14-}			3.6		–	3.5		3.6		–	6,7	10			
Clock Input	t_{6-14+}			4.7		–	4.3		4.4		–	7	10,6			
	t_{6-14-}	↓	↓	4.7	↓	–	4.3	↓	4.4	↓	–	7	10,6	↓	↓	↓
Reset Input	t_{11+4-}	4	1.0	4.0	1.0	–	3.9	1.0	4.2	ns	5	6	7,11	4 ②	8	1,16
	t_{11+14-}	14	1.0	4.0	1.0	–	3.9	1.0	4.2	↓	10	6	7,11	14 ②	8	1,16
Setup Time	t_{setup}	14	2.5	–	2.5	–	–	2.5	–	ns	–	7	6,10	14	8	1,16
Hold Time	t_{hold}	14	1.5	–	1.5	–	–	1.5	–		–	7	6,10			
Rise Time (20 to 80%)	t_+	14	1.0	3.6	1.1	–	3.5	1.1	3.7		–	6,7	10			
Fall Time (20 to 80%)	t_-	14	1.0	3.6	1.1	–	3.5	1.1	3.7	↓	–	6,7	10	↓	↓	↓

① Individually test each input; apply $V_{IL\ min}$ to pin under test.

② Output latched to high logic state prior to test.

MC10176

HEX "D" MASTER-SLAVE FLIP-FLOP

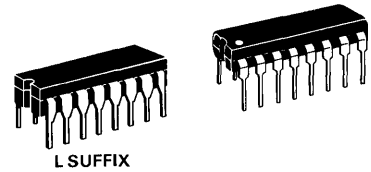
The MC10176 contains six high-speed, master slave type "D" flip-flops. Clocking is common to all six flip-flops. Data is entered into the master when the clock is low. Master to slave data transfer takes place on the positive-going Clock transition. Thus, outputs may change only on a positive-going Clock transition. A change in the information present at the data (D) input will not affect the output information any other time due to the master-slave construction of this device.

P_D = 460 mW typ/pkg (No Load)
f_{toggle} = 150 MHz (typ)
t_r, t_f = 2.0 ns typ (20%–80%)

MECL 10K SERIES

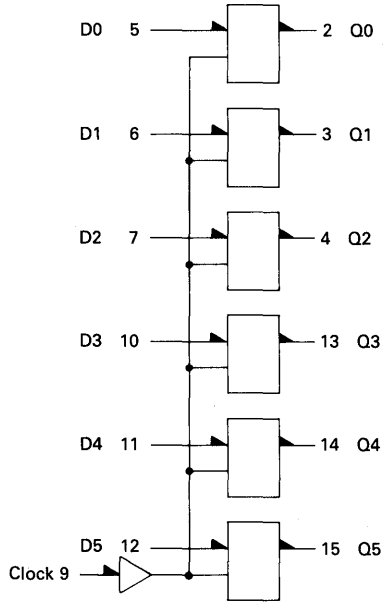
HEX "D" MASTER-SLAVE FLIP-FLOP

P SUFFIX
PLASTIC PACKAGE
CASE 648



L SUFFIX
CERAMIC PACKAGE
CASE 620

LOGIC DIAGRAM



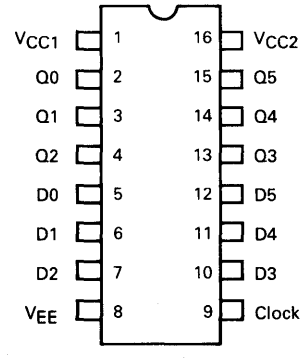
CLOCKED TRUTH TABLE

C	D	Q_{n+1}
L	ϕ	Q_n
H*	L	L
H*	H	H

ϕ = Don't Care
*A clock H is a clock transition from a low to a high state.

V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

PIN ASSIGNMENT



ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown for only one data input, and the clock input, and for one output. Other inputs and outputs tested in the same manner.

@Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{IHAmin}	$V_{ILA\ max}$	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10176 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	121	–	88	110	–	121	mAdc	–	–	–	–	8	1,16
Input Current	I_{inH}	5	–	350	–	–	220	–	220	µAdc	5	–	–	–	8	1,16
		9	–	495	–	–	310	–	310		9	–	–	–	8	1,16
Input Leakage Current	I_{inL}	5	0.5	–	0.5	–	–	0.3	–	µAdc	–	5	–	–	8	1,16
		9	0.5	–	0.5	–	–	0.3	–	µAdc	–	9	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	2†	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	5	–	–	–	8	1,16
		15†	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	12	–	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	2†	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	–	5	–	–	8	1,16
		15†	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	–	12	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	2†	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	5	–	8	1,16
		15†	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	12	–	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	2†	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	–	5	8	1,16
		15†	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	–	12	8	1,16
Switching Times Clock Input **											+1.11 Vdc	+0.31 Vdc	Pulse In	Pulse Out	-3.2 Vdc	+2.0 Vdc
Progagation Delay	t_{9+2+}	2	1.6	4.6	1.6	–	4.5	1.6	5.0	ns	–	–	5,9	2	8	1,16
	t_{9+2-}	2	1.6	4.6	1.6	–	4.5	1.6	5.0		–	–				
Rise Time (20 to 80%)	t_{2+}	2	1.0	4.1	1.1	–	4.0	1.1	4.4		–	–				
Fall Time (20 to 80%)	t_{2-}	2	1.0	4.1	1.1	–	4.0	1.1	4.4		–	–				
Setup Time	t_{setup}	2	2.5	–	2.5	–	–	2.5	–	ns	–	–	5.9	2	8	1,16
Hold Time	t_{hold}	2	1.5	–	1.5	–	–	1.5	–	ns	–	–	5,9	2	8	1,16
Toggle Frequency	f_{tog}	2	125	–	125	150	–	125	–	MHz	–	–	–	–	8	1,16

† Output level to be measured after a clock pulse has been applied to C input (pin 9) $V_{IH\ max}$ $V_{IL\ min}$

MOTOROLA

MC10177

TRIPLE MECL TO NMOS TRANSLATOR

The MC10177 consists of three MECL to MOS translators which convert MECL 10,000 logic levels to NMOS levels. It is designed for use in N-channel memory systems as a Read/Write, Data/Address driver. It may also be used as a high fanout (30) MECL to TTL translator, or in other applications requiring the capability to drive high capacitive loads. A separate lead from each of the three translators is brought out of the package. These leads may be connected to V_{SS} or to an external capacitor (0.01 to 0.05 μF to ground), for waveform improvement, and short circuit protection. When connection is made to an external capacitor, V_{SS} line fluctuations due to transient currents are also reduced.

Max Load: 350 pF

P_D = 1.0 W typ/pkg @ 5.0 MHz

Operating rate: 5.0 MHz typ.
(all 3 translators in use simultaneously)

INPUT: MECL 10,000 (differential)

OUTPUT: NMOS + 0.5 V V_{OLmax}
+ 3.0 V V_{OHmin}*

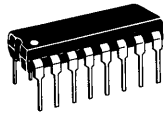
t_r, t_f = 6.0 ns typ (20%–80%)

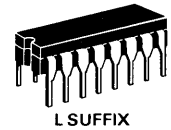
*May be raised by increasing V_{SS}.

MECL 10K SERIES

TRIPLE MECL TO NMOS TRANSLATOR

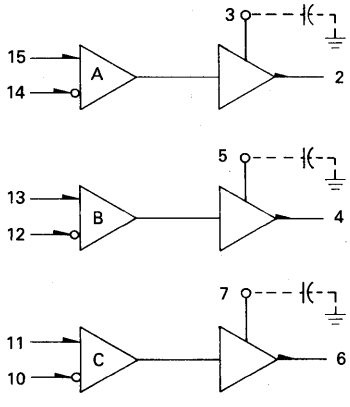
P SUFFIX
PLASTIC PACKAGE
CASE 648





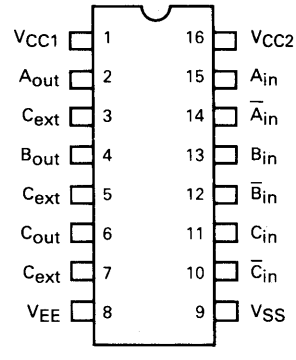
L SUFFIX
CERAMIC PACKAGE
CASE 620

LOGIC DIAGRAM



V_{CC} = Gnd = Pins 1, 16
V_{EE} = Pin 8 = −5.2 Vdc ±5%
V_{SS} = Pin 9 (+5.0 Vdc or +6.0 Vdc ± 10%)

PIN ASSIGNMENT



ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained.
In general test procedures are shown for only one input and one output. The other inputs and outputs are tested in a similar manner.

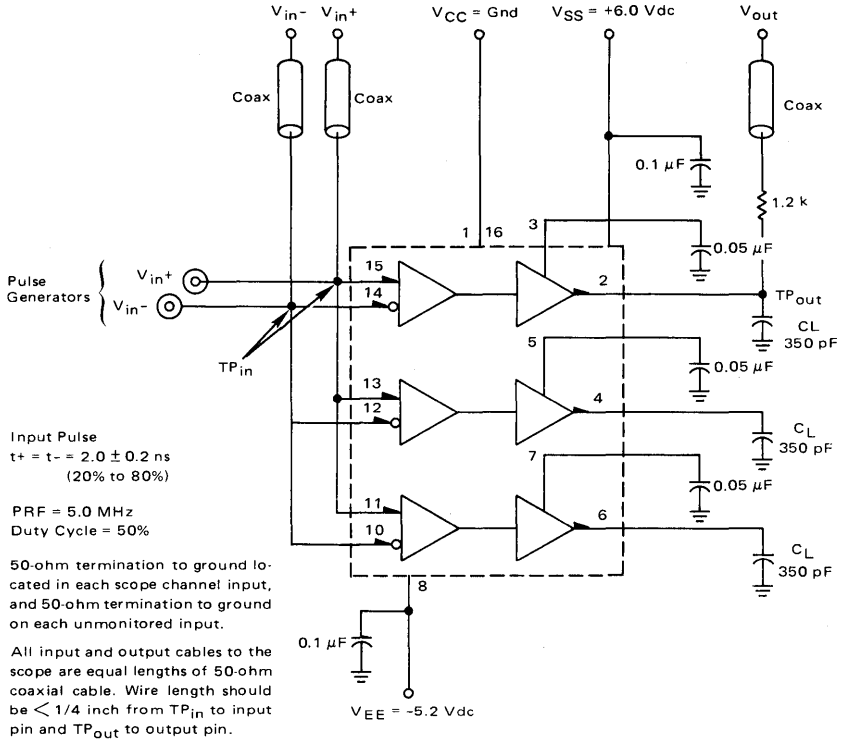
@ Test Temperature	TEST VOLTAGE/CURRENT VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	V_{SC}	V_{SS}	(mAdc ±1%) I_{OL1}	I_{OL2}	I_{OH}	(μF ±5%) C#
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2	+5.0	+6.0	+1.0	+20	-15	0.05
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2	+5.0	+6.0	+1.0	+20	-15	0.05
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2	+5.0	+6.0	+1.0	+20	-15	0.05

Characteristic	Symbol	Pin Under Test	MC10177 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+85°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	V_{SC}	V_{SS}	I_{OL1}	I_{OL2}	I_{OH}	C#	(V_{CC}) Gnd
Power Supply Drain	I_E	8	–	106	–	–	96	–	106	mAdc	–	–	–	–	8	–	–	–	–	–	–	1,16
Negative	I_{SSO}	9	–	88	–	–	88	–	88	mAdc	–	–	–	–	8	9	–	–	–	–	–	1,16
Positive Output Low	I_{SSL}	9	–	88	–	–	88	–	88	↓	10,12,14	11,13,15	–	–	↓	↓	–	–	–	–	–	↓
Positive Output High	I_{SSH}	9	–	44	–	–	44	–	44	↓	11,13,15	10,12,14	–	–	↓	↓	–	–	–	–	–	↓
Input Current	I_{inH}	10	–	1.6	–	–	0.35	–	1.0	mAdc	10	11	–	–	8	9	–	–	–	–	–	1,16
		11	–	↓	–	–	↓	–	↓	↓	11	10	–	–	↓	↓	–	–	–	–	–	↓
		12	–	↓	–	–	↓	–	↓	↓	12	13	–	–	↓	↓	–	–	–	–	–	↓
		13	–	↓	–	–	↓	–	↓	↓	13	12	–	–	↓	↓	–	–	–	–	–	↓
		14	–	↓	–	–	↓	–	↓	↓	14	15	–	–	↓	↓	–	–	–	–	–	↓
		15	–	↓	–	–	↓	–	↓	↓	15	14	–	–	↓	↓	–	–	–	–	–	↓
Input Leakage Current	I_{CBO}	11	–	1.5	-1.0	–	–	–	1.0	μAdc	10	–	–	–	8,11	9	–	–	–	–	–	1,16
		13	–	↓	↓	–	–	–	↓	↓	12	–	–	–	8,13	↓	–	–	–	–	–	↓
		15	–	↓	↓	–	–	–	↓	↓	14	–	–	–	8,15	↓	–	–	–	–	–	↓
Logic "1" Output Voltage	V_{OH}	2	3.0	–	3.0	–	–	3.0	–	Vdc	15	14	–	–	8	9	–	–	–	2	–	1,16
		2	4.0	–	4.0	–	–	4.0	–	Vdc	15	14	–	–	8	–	9	–	–	2	–	1,16
Logic "0" Output Voltage	V_{OL}	2	–	0.5	–	–	0.5	–	0.5	Vdc	14	15	–	–	8	9	–	2	–	–	–	1,16
		2	–	0.6	–	–	0.6	–	0.6	Vdc	14	15	–	–	8	9	–	–	2	–	–	1,16
Logic "1" Threshold Voltage	V_{OHA}	2	3.0	–	3.0	–	–	3.0	–	Vdc	–	14	15	–	8	9	–	–	–	2	–	1,16
		2	4.0	–	4.0	–	–	4.0	–	Vdc	–	14	15	–	8	–	9	–	–	2	–	1,16
Logic "0" Threshold Voltage	V_{OLA}	2	–	0.5	–	–	0.5	–	0.5	Vdc	14	–	–	15	8	9	–	2	–	–	–	1,16
		2	–	0.6	–	–	0.6	–	0.6	Vdc	14	–	–	15	8	9	–	–	2	–	–	1,16
Output Short-Circuit Current	I_{SC}	2	-50	-90	-50	–	-90	-50	-90	mAdc	15	14	–	–	8	9	–	–	–	–	–	1,2,16
											-1.29 V	-1.69 V	Pulse In	Pulse Out	-5.2 V							
Switching Times	t_{15+2+}	2	2.0	12.5	2.0	6.0	12.5	2.0	12.5	ns	14	11,13	15	2	8	9	–	–	–	–	3,5,7	1,16
(350 pF Load)	t_{15-2-}	2	↓	↓	↓	↓	↓	↓	↓	↓	14	↓	15	↓	↓	↓	–	–	–	–	↓	↓
Propagation Delay	t_{14+2-}	2	↓	↓	↓	↓	↓	↓	↓	↓	15	↓	14	↓	↓	↓	–	–	–	–	↓	↓
	t_{14-2+}	2	↓	↓	↓	↓	↓	↓	↓	↓	15	↓	14	↓	↓	↓	–	–	–	–	↓	↓
Rise Time (10% to 90%)	t_{2+}	2	3.0	12	3.0	↓	11	3.0	11	↓	14	↓	15	↓	↓	↓	–	–	–	–	↓	↓
Fall Time (10% to 90%)	t_{2-}	2	3.0	12	3.0	↓	11	3.0	11	↓	14	↓	15	↓	↓	↓	–	–	–	–	↓	↓
Supply Source Current (@ 5.0 MHz) (350 pF Load)	I_{SS}	9	–	110	–	83	110	–	110	mA	10,12,14	–	11,13,15	–	8	–	9	–	–	–	3,5,7	1,16

#See test circuit.

3

SWITCHING TIME TEST CIRCUIT



Input Pulse
t+ = t- = 2.0 ± 0.2 ns
(20% to 80%)

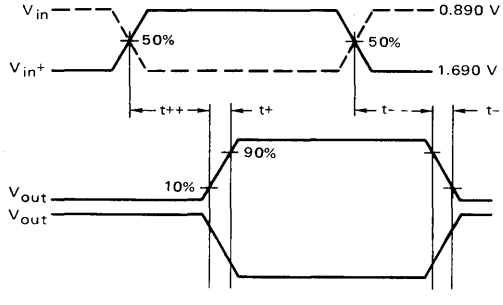
PRF = 5.0 MHz
Duty Cycle = 50%

50-ohm termination to ground located in each scope channel input, and 50-ohm termination to ground on each unmonitored input.

All input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be < 1/4 inch from TP_{in} to input pin and TP_{out} to output pin.

SWITCHING WAVEFORMS @ 25°C

Switching times are measured after the device under test reaches a stabilized temperature (air flow ≥ 500 lfpm)



MOTOROLA

MC10178

BINARY COUNTER

The MC10178 is a four-bit counter capable of divide-by-two, divide-by-four, divide-by-eight or a divide-by-sixteen function.

Clock inputs trigger on the positive going edge of the clock pulse. Set and Reset inputs override the clock, allowing asynchronous "set" or "clear." Individual Set and common Reset inputs are provided, as well as complementary outputs for the first and fourth bits. True outputs are available at all bits.

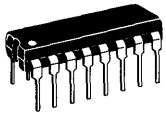
P_D = 370 mW typ/pkg (No Load)
f_{toggle} = 150 MHz (typ)
t_r, t_f = 2.7 ns typ (20%–80%)

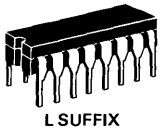
MECL 10K SERIES

BINARY COUNTER

3

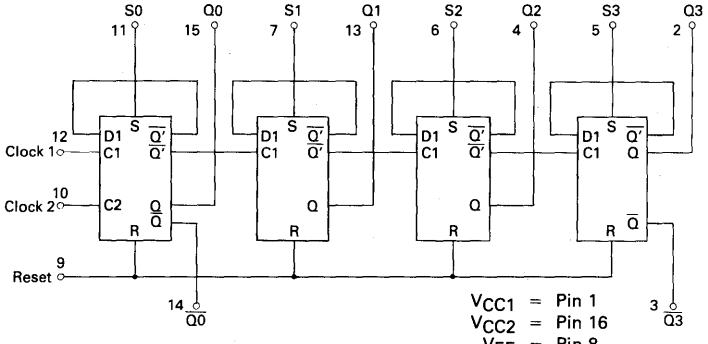
P SUFFIX
PLASTIC PACKAGE
CASE 648





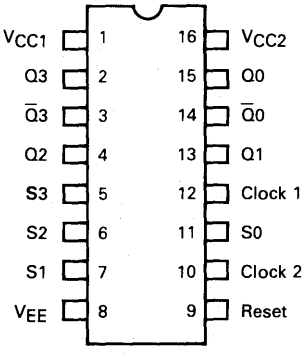
L SUFFIX
CERAMIC PACKAGE
CASE 620

LOGIC DIAGRAM



V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

PIN ASSIGNMENT



TRUTH TABLE

INPUTS							OUTPUTS			
R	S0	S1	S2	S3	C1	C2	Q0	Q1	Q2	Q3
H	L	L	L	L	ϕ	ϕ	L	L	L	L
L	H	H	H	H	ϕ	ϕ	H	H	H	H
L	L	L	L	L	H	ϕ	No Count			
L	L	L	L	L	ϕ	H	No Count			
L	L	L	L	L	**		L	L	L	L
L	L	L	L	L	**		H	L	L	L
L	L	L	L	L	**		L	H	L	L
L	L	L	L	L	**		H	H	L	L
L	L	L	L	L	**		L	L	H	L
L	L	L	L	L	**		H	L	H	L
L	L	L	L	L	**		L	H	H	L
L	L	L	L	L	**		H	H	H	L
L	L	L	L	L	**		L	L	L	H
L	L	L	L	L	**		H	L	L	H
L	L	L	L	L	**		L	H	L	H
L	L	L	L	L	**		H	H	L	H
L	L	L	L	L	**		L	L	H	H
L	L	L	L	L	**		H	L	H	H
L	L	L	L	L	**		L	H	H	H
L	L	L	L	L	**		H	H	H	H

ϕ = Don't Care

**  V_{IH}
V_{IL}

Clock transition from V_{IL} to V_{IH} may be applied to C1 or C2 or both for same effect.

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown for only selected inputs and outputs. Other inputs and outputs tested in the same manner.

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10178 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	97	–	–	88	–	97	mAdc	9	–	–	–	8	1,16
Input Current	I_{inH}	12	–	390	–	–	245	–	245	µAdc	12	–	–	–	8	1,16
		11	–	350	–	–	220	–	220	µAdc	11	–	–	–	8	1,16
		9	–	650	–	–	410	–	410	µAdc	9	–	–	–	8	1,16
	I_{inL}	*	0.5	–	0.5	–	–	0.3	–	µAdc	–	*	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	14	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	9	–	–	–	8	1,16
		15	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	11	–	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	14	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	11	–	–	–	8	1,16
		15	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	9	–	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	3	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	5	–	8	1,16
		14	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	11	–	8	1,16
		15	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	9	–	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	3	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	–	5	8	1,16
		14	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	–	11	8	1,16
		15	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	–	9	8	1,16
Switching Times													Pulse In	Pulse Out	-3.2 Vdc	+2.0 Vdc
Clock Input Propagation Delay	t_{12+15+}	15	1.4	5.0	1.5	3.5	4.8	1.5	5.3	ns	–	–	12	15	8	1,16
	t_{12-13-}	13	1.9	9.4	2.0	6.0	9.2	2.0	9.8		–	–		13		
	t_{12+4-}	4	2.9	12.3	3.0	8.5	12	3.0	12.8		–	–		4		
	t_{12-3+}	3	3.9	14.9	4.0	11	14.5	4.0	15.5		–	–		3		
Rise Time (20 to 80%)	t_{15+}	15	1.1	4.7	1.1	2.5	4.5	1.1	5.0		–	–		15		
Fall Time (20 to 80%)	t_{15-}	15	1.1	4.7	1.1	2.5	4.5	1.1	5.0		–	–		15		
Set Input	t_{11-15+}	15	1.4	5.2	1.5	–	5.0	1.5	5.5	ns	–	–	11	15	8	1,16
Reset Input	t_{9-15+}	15	1.4	5.2	1.5	–	5.0	1.5	5.5	ns	–	–	9	15	8	1,16
Counting Frequency	f_{count}	15	125	–	125	150	–	125	–	MHz	–	–	12	15	8	1,16

*Individually test each input applying V_{IL} to input under test.

MOTOROLA

MC10179

LOOK-AHEAD CARRY BLOCK

The MC10179 is a high speed, low power, standard MECL complex function that is designed to perform the look-ahead carry function. This device can be used with the MC10181 4-bit ALU directly, or with the MC10180 dual arithmetic unit in any computer, instrumentation or digital communication application requiring high speed arithmetic operation on long words.

When used with the MC10181, the MC10179 performs a second order or higher look-ahead. Figure 2 shows a 16-bit look-ahead carry arithmetic unit. Second order carry is valuable for longer binary words. As an example, addition of two 32-bit words is improved from 30 nanoseconds with ripple-carry techniques. A block diagram of a 32-bit ALU is shown in Figure 1. The MC10179 may also be used in many other applications. It can, for example, reduce system package count when used to generate functions of several variables.

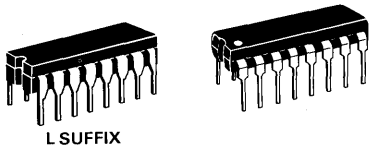
P_D = 300 mW typ/pkg (No Load)
t_{pd} = 3.0 ns typ (Carry, Propogate)
4.0 ns typ (Generate)
t_r, t_f = 2.3 ns typ (20%–80%)

MECL 10K SERIES

LOOK-AHEAD CARRY BLOCK

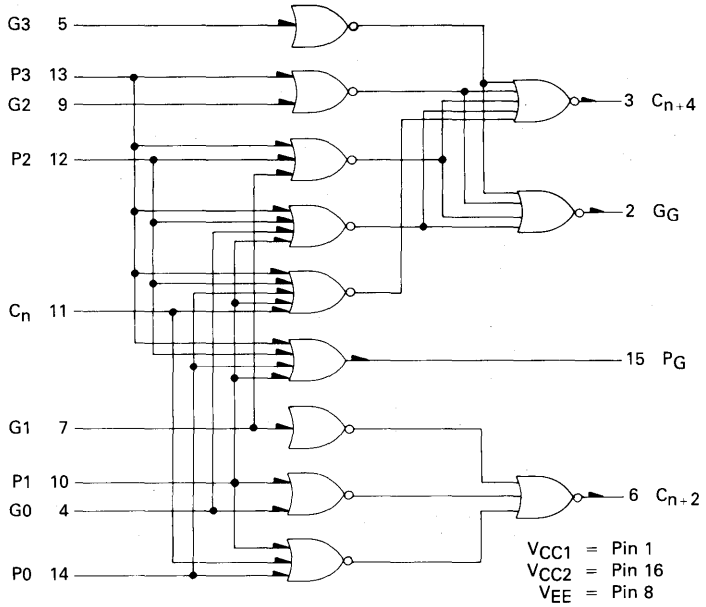
3

P SUFFIX
PLASTIC PACKAGE
CASE 648



L SUFFIX
CERAMIC PACKAGE
CASE 620

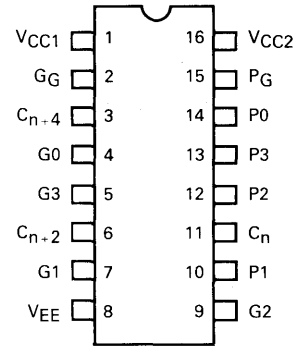
LOGIC DIAGRAM



V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

$P_G = P0 + P1 + P2 + P3$
$G_G = (G0 + P1 + P2 + P3)(G1 + P2 + P3)(G2 + P3)\,G3$
$C_{n+2} = (C_n + P0 + P1)(G0 + P1)\,G1$
$C_{n+4} = (C_n + P0 + P1 + P2 + P3)(G0 + P1 + P2 + P3)(G1 + P2 + P3)(G2 + P3)\,G3$

PIN ASSIGNMENT



ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series device has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown only for selected inputs and outputs. Other inputs and outputs are tested in a similar manner.

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10179 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	79	–	58	72	–	79	mAdc	–	–	–	–	8	1,16
Input Current	I_{inH}	4,7,11	–	430	–	–	270	–	270	µAdc	4,7,11	–	–	–	8	1,16
		5,9	–	360	–	–	225	–	225	↓	5,9	–	–	–	↓	↓
		10,13	–	700	–	–	440	–	440		10,13	–	–	–		
		12	–	630	–	–	395	–	395		12	–	–	–		
		14	–	565	–	–	355	–	355		14	–	–	–		
	I_{inL}	4	0.5	–	0.5	–	–	0.3	–	µAdc	–	4	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	4,5,7,9	–	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	3	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	–	–	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	2	-1.080	–	-0.980	–	–	-0.910	–	Vdc	13	–	5	–	8	1,16
		2	↓	–	↓	–	–	↓	–	↓	5,12	–	9	–	↓	↓
		2		–		–	–		–		5,9	–	12	–		
		2		–		–	–		–		5	–	13	–		
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.655	–	–	-1.630	–	-1.595	Vdc	13	–	–	5	8	1,16
		2	–		–	–		–			5	–	–	13		
		2	–	↓	–	–	↓	–	↓	↓	5	–	–	9	↓	↓
		2	–		–	–		–			5,9	–	–	12		
											+1.11 V		Pulse In	Pulse Out	-3.2 V	+2.0 V
Switching Times (50 Ω Load)	t_{10+15+}	15	1.0	3.7	1.0	2.5	3.5	1.0	3.9	ns	4.7	–	10	15	8	1,16
	t_{10-15-}	15	↓	3.7	↓	2.5	3.5	↓	3.9	↓	4.7	–	10	15	↓	↓
Propagation Delay	t_{11+6+}	6		5.8		3.0	4.5		6.1		4,7	–	11	6		
	t_{11-6-}	6		↓		3.0	4.5		↓		4,7	–	11	6		
	t_{5+2+}	2				4.0	5.5				4,7,9	–	5	2		
	t_{5-2-}	2		↓		4.0	5.5		↓		4,7,9	–	5	2		
Rise Time (20% to 80%)	t_{6+}	6	1.1	3.7	1.1	2.5	3.5	1.1	3.9		4,7	–	11	6		
Fall Time (20% to 80%)	t_{6-}	6	1.1	3.7	1.1	2.5	3.5	1.1	3.9	↓	4,7	–	11	6	↓	↓

FIGURE 1 — 32-BIT ALU WITH CARRY LOOK-AHEAD

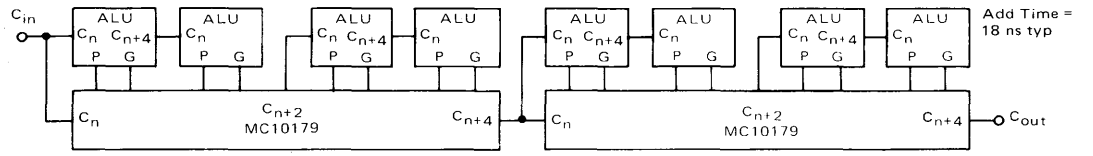
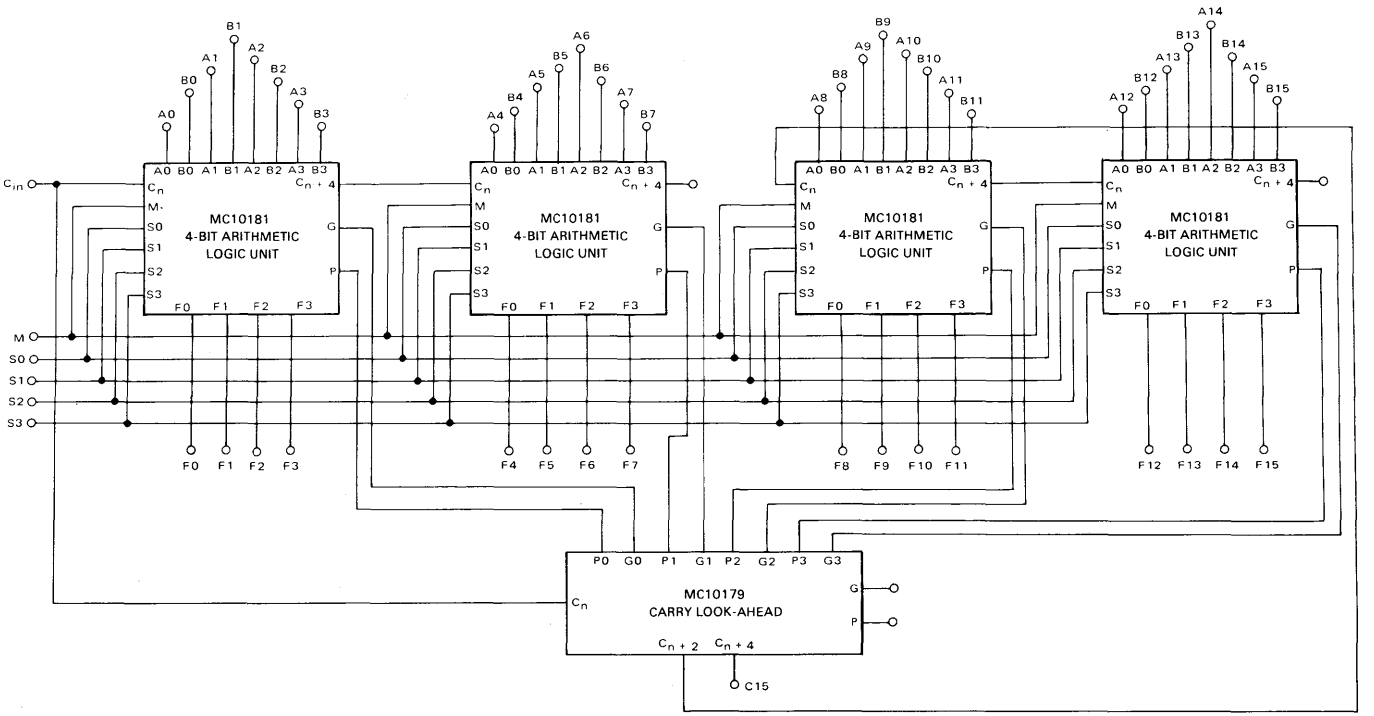


FIGURE 2 — 16-BIT FULL LOOK-AHEAD CARRY ARITHMETIC LOGIC UNIT



MC10180

MECL 10K SERIES

DUAL 2-BIT ADDER/SUBTRACTOR

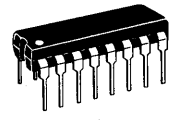
DUAL 2-BIT ADDER/SUBTRACTOR

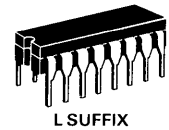
The MC10180 is a high speed, low power general-purpose adder/subtractor. It is designed to be used in special purpose adders/subtractors or in high speed multiplier arrays. The MC10180 can be used in any piece of equipment where these operations are necessary.

Inputs for each adder are Carry-in, operand A, and operand B; outputs are Sum, $\overline{\text{Sum}}$, and Carry-out. The common Select inputs serve as a control line to invert A for subtract, and a control line to invert B.

P_D = 360 mW typ/pkg (No Load)
C_{in} to C_{out} = 2.2 ns
A0 to S0 = 4.5 ns
A0 to C_{out} = 4.5 ns
t_r, t_f = 2.4 ns typ (20%–80%)

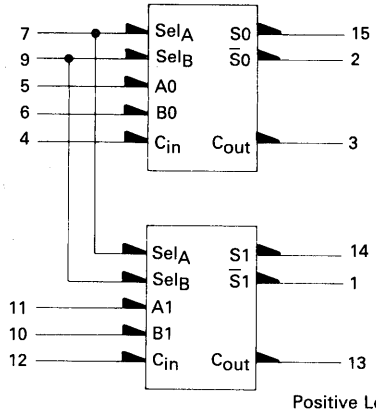
P SUFFIX
PLASTIC PACKAGE
CASE 648





L SUFFIX
CERAMIC PACKAGE
CASE 620

LOGIC DIAGRAM



V_{CC} = pin 16
V_{EE} = pin 8

Positive Logic Only

$A' = \overline{A \oplus Sel_A} = A \odot Sel_A$

$B' = \overline{B \oplus Sel_B} = B \odot Sel_B$

$S = \overline{C}_{in}(\overline{A'B'} + A'\overline{B'}) +$

$C_{in}(A'B' + \overline{A'B'})$

$C_{out} = C_{in}A' + C_{in}B' + A'B'$

FUNCTION SELECT TABLE

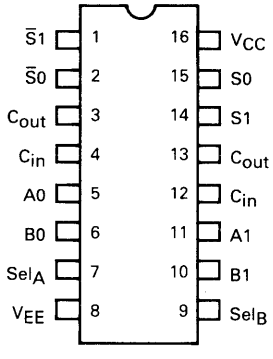
Sel_A	Sel_B	Function
H	H	S = A plus B
H	L	S = A minus B
L	H	S = B minus A
L	L	S = 0 minus A minus B

TRUTH TABLE

FUNCTION	INPUTS							
	Sel_A	Sel_B	A0	B0	C_{in}	S0	$\overline{S0}$	C_{out}
ADD	H	H	L	L	L	L	H	L
	H	H	L	L	H	H	L	L
	H	H	L	H	L	H	L	L
	H	H	L	H	H	L	H	H
	H	H	H	L	L	H	L	L
	H	H	H	L	H	L	H	H
	H	H	H	H	L	L	H	L
	H	H	H	H	H	H	L	H
SUBTRACT	H	L	L	L	L	H	L	L
	H	L	L	L	H	L	H	H
	H	L	L	H	L	L	H	L
	H	L	L	H	H	H	L	L
	H	L	H	L	L	L	H	H
	H	L	H	L	H	H	L	L
	H	L	H	H	L	L	H	H
	H	L	H	H	H	H	L	H

FUNCTION	INPUTS							
	Sel_A	Sel_B	A0	B0	C_{in}	S0	$\overline{S0}$	C_{out}
REVERSE SUBTRACT	L	H	L	L	L	H	L	L
	L	H	L	L	H	L	H	H
	L	H	L	H	L	L	H	H
	L	H	L	H	H	H	L	H
	L	H	H	L	L	L	H	L
	L	H	H	L	H	H	L	L
	L	H	H	H	L	L	H	L
	L	H	H	H	H	H	L	H
	L	L	L	L	L	L	H	H
	L	L	L	L	H	H	L	H
	L	L	L	H	L	L	H	L
	L	L	L	H	H	H	L	L
	L	L	H	L	L	L	H	H
	L	L	H	L	H	H	L	H
	L	L	H	H	L	L	H	L
	L	L	H	H	H	H	L	L

PIN ASSIGNMENT



ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts.

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10180 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	95	–	70	86	–	95	mAdc	–	–	–	–	8	16
Input Current	I_{inH}	4	–	590	–	–	370	–	370	μAdc	4	–	–	–	8	16
		5	–	350	–	–	220	–	220		5	–	–	–		
		6	–	350	–	–	220	–	220		6	–	–	–		
		7	–	460	–	–	290	–	290		7	–	–	–		
		9	–	460	–	–	290	–	290		9	–	–	–		
		10	–	350	–	–	220	–	220		10	–	–	–		
		11	–	350	–	–	220	–	220		11	–	–	–		
		12	–	590	–	–	370	–	370		12	–	–	–		
	I_{inL}	All	0.5	–	0.5	–	–	0.3	–	μAdc	–	*	–	–	8	16
Logic "1" Output Voltage	V_{OH}	2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	7,9	–	–	–	8	16
		3	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700		4,5,7,9	–	–	–		
		15	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700		4,7,9	–	–	–		
Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	5,7,9	–	–	–	8	16
		3	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615		7,9	–	–	–		
		15	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615		7,9	–	–	–		
Logic "1" Threshold Voltage	V_{OHA}	2	-1.080	–	-0.980	–	–	-0.910	–	Vdc	7,9	–	–	4	8	16
		3	-1.080	–	-0.980	–	–	-0.910	–		4,7,9	–	5	–		
		15	-1.080	–	-0.980	–	–	-0.910	–		7,9	–	4	–		
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.655	–	–	-1.630	–	-1.595	Vdc	7,9	–	4	–	8	16
		3	–	-1.655	–	–	-1.630	–	-1.595		7,9	–	–	4		
		15	–	-1.655	–	–	-1.630	–	-1.595		4,7,9	–	5	–		
Switching Times Propagation Delay											+1.11 V		Pulse In	Pulse Out	-3.2 V	+2.0 V
Operand Input	t_{5+15+}	15	1.3	5.8	1.3	–	5.4	1.1	5.8	ns	7,9	–	5	15	8	16
	t_{6+15+}	15	1.3	5.8	1.3	–	5.4	1.1	5.8		7,9	–	6	15		
Carry-in Input	t_{4+15+}	15	1.0	3.4	1.0	–	3.3	0.9	3.6		7,9	–	4	15		
	t_{4+3+}	3	1.0	3.4	1.0	–	3.3	0.9	3.6		5,7,9	–	4	3		
Select Input	t_{7+15+}	15	1.3	5.8	1.3	–	5.4	1.1	5.8		4,9	–	7	15		
	t_{9+15+}	15	1.3	5.8	1.3	–	5.4	1.1	5.8		7,4	–	9			
Rise Time (20 to 80%)	t_{15+}	15	1.0	3.8	1.1	–	3.7	1.1	3.9		7,9	–	5			
Fall Time	t_{15-}	15	1.0	3.8	1.1	–	3.7	1.1	3.9		7,9	–	5			

*Individually apply $V_{IL\ min}$ to pin under test.

MOTOROLA

MC10181

4-BIT ARITHMETIC LOGIC UNIT/FUNCTION GENERATOR

The MC10181 is a high-speed arithmetic logic unit capable of performing 16 logic operations and 16 arithmetic operations on two four-bit words. Full internal carry is incorporated for ripple through operation.

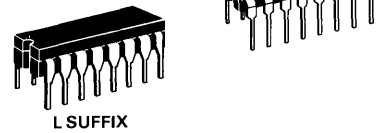
Arithmetic logic operations are selected by applying the appropriate binary word to the select inputs (S0 through S3) as indicated in the tables of arithmetic/logic functions. Group carry propagate (P_G) and carry generate (G_G) are provided to allow fast operations on very long words using a second order look ahead. The internal carry is enabled by applying a low level voltage to the mode control input (M).

When used with the MC10179, full-carry look-ahead, as a second order look ahead block, the MC10181 provides high speed arithmetic operations on very long words.

P_D = 600 mW typ/pkg (No Load)
t_{pd} (typ): A1 to F = 6.5 ns
C_n to C_{n+4} = 3.1 ns
A1 to P_G = 5.0 ns
A1 to G_G = 4.5 ns
A1 to C_{n+4} = 5.0

MECL 10K SERIES

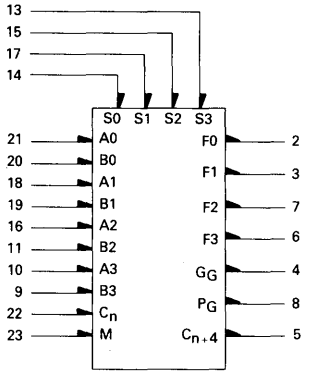
4-BIT ARITHMETIC LOGIC UNIT/FUNCTION GENERATOR



P SUFFIX
PLASTIC PACKAGE
CASE 648

L SUFFIX
CERAMIC PACKAGE
CASE 620

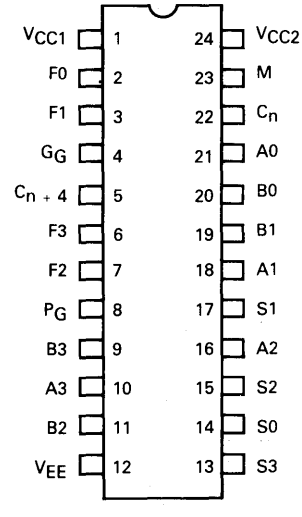
LOGIC DIAGRAM



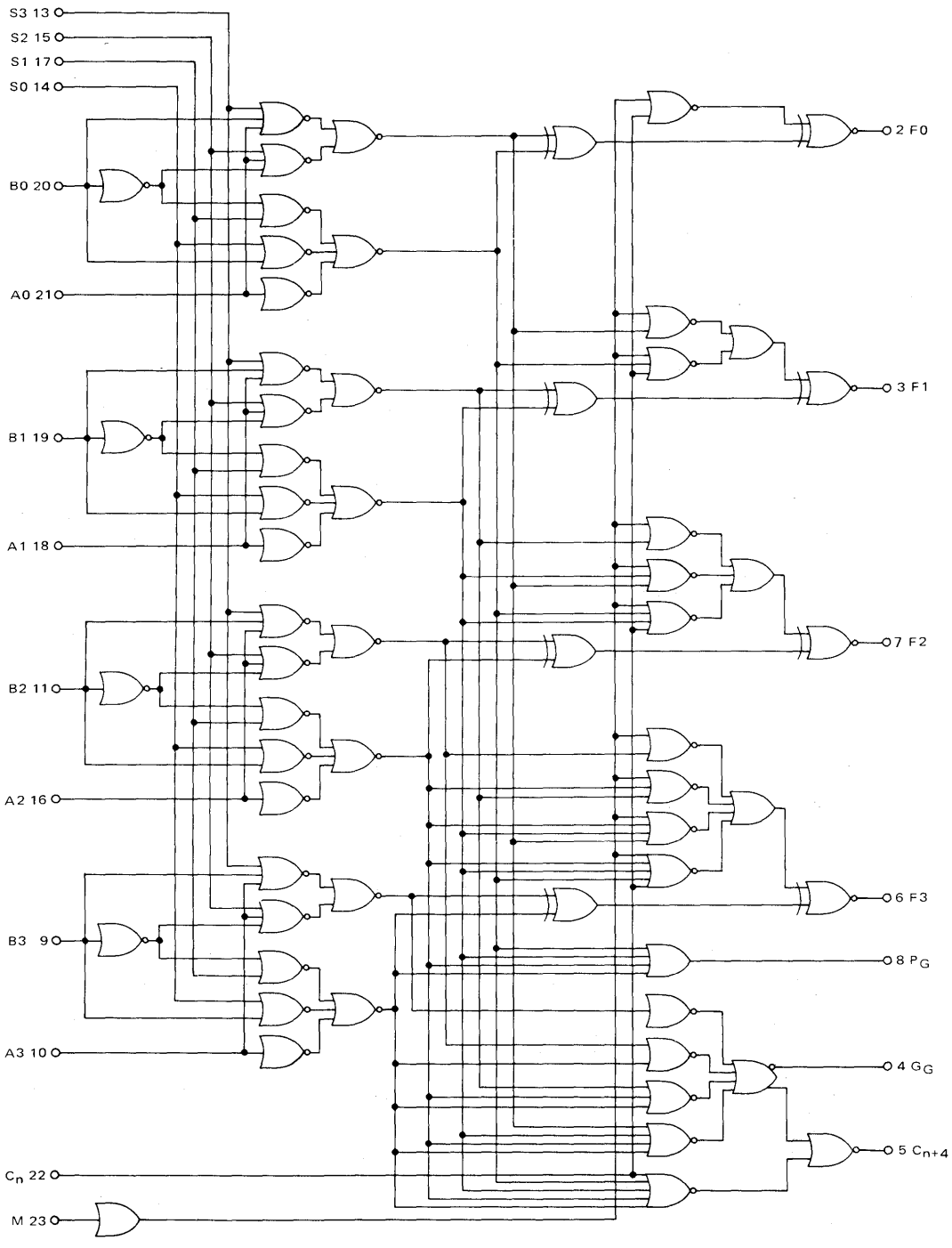
V_{CC1} = Pin 1
V_{CC2} = Pin 24
V_{EE} = Pin 12

Function Select S3	S2	S1	S0	Logic Functions M is High C = D.C. F	Arithmetic Operation M is Low C_n is low F
L	L	L	L	$F = \overline{A}$	F = A
L	L	L	H	$F = \overline{A} + \overline{B}$	F = A plus $(A \cdot \overline{B})$
L	L	H	L	$F = \overline{A} + B$	F = A plus $(A \cdot B)$
L	L	H	H	F = Logical "1"	F = A times 2
L	H	L	L	$F = \overline{A \cdot B}$	F = (A + B) plus 0
L	H	L	H	$F = \overline{B}$	F = (A + B) plus $(A \cdot \overline{B})$
L	H	H	L	$F = A \odot B$	F = A plus B
L	H	H	H	$F = A + \overline{B}$	F = A plus (A + B)
H	L	L	L	$F = \overline{A} \cdot B$	F = (A + $\overline{B}$) plus 0
H	L	L	H	$F = A \oplus B$	F = A minus B minus 1
H	L	H	L	F = B	F = (A + $\overline{B}$) plus $(A \cdot B)$
H	L	H	H	$F = A + B$	F = A plus (A + $\overline{B}$)
H	H	L	L	F = Logical "0"	F = minus 1 (two's complement)
H	H	L	H	$F = A \cdot \overline{B}$	F = $(A \cdot \overline{B})$ minus 1
H	H	H	L	$F = A \cdot B$	F = $(A \cdot B)$ minus 1
H	H	H	H	F = A	F = A minus 1

PIN ASSIGNMENT



POSITIVE LOGIC DIAGRAM



ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts.

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
−30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10181 Test Limits −30°C Min	−30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	Gnd
Power Supply Drain Current	I_E	12	–	159	–	–	145	–	159	mAdc	–	–	–	–	12	1,24
Input Current	I_{inH}	9	–	390	–	–	245	–	245	µAdc	9	–	–	–	12	1,24
		10	–	350	–	–	220	–	220		10	–	–	–		
		11	–	390	–	–	245	–	245		11	–	–	–		
		13	–	320	–	–	200	–	200		13	–	–	–		
		14	–	425	–	–	265	–	265		14	–	–	–		
		15	–	425	–	–	265	–	265		15	–	–	–		
		16	–	350	–	–	220	–	220		16	–	–	–		
		17	–	425	–	–	265	–	265		17	–	–	–		
		18	–	350	–	–	220	–	220		18	–	–	–		
		19	–	390	–	–	245	–	245		19	–	–	–		
		20	–	390	–	–	245	–	245		20	–	–	–		
		21	–	350	–	–	220	–	220		21	–	–	–		
		22	–	460	–	–	290	–	290		22	–	–	–		
		23	–	320	–	–	200	–	200		23	–	–	–		
Input Leakage Current	I_{inL}	9	0.5	–	0.5	–	–	0.3	–	µAdc	–	9	–	–	12	1,24
		10		–		–	–		–		–	10	–	–		
		11		–		–	–		–		–	11	–	–		
		13		–		–	–		–		–	13	–	–		
		14		–		–	–		–		–	14	–	–		
		15		–		–	–		–		–	15	–	–		
		16		–		–	–		–		–	16	–	–		
		17		–		–	–		–		–	17	–	–		
		18		–		–	–		–		–	18	–	–		
		19		–		–	–		–		–	19	–	–		
		20		–		–	–		–		–	20	–	–		
		21		–		–	–		–		–	21	–	–		
		22		–		–	–		–		–	22	–	–		
		23		–		–	–		–		–	23	–	–		
High Output Voltage	V_{OH}	*	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	*	*	–	–	12	1,24
Low Output Voltage	V_{OL}	*	-2.000	-1.675	-1.990	–	-1.650	-1.920	-1.615	Vdc	*	*	–	–	12	1,24
High Threshold Voltage	V_{OHA}	*	-1.080	—	-0.980	–	—	-0.910	—	Vdc	—	—	**	**	12	1,24
Low Threshold Voltage	V_{OLA}	*	–	-1.655	—	–	-1.630	—	-1.595	Vdc	—	—	**	**	12	1,24

* Test all input-output combinations according to Function Table.

** For threshold level test, apply threshold input level to only one input pin at a time.

Characteristic	Symbol	Input	Output	Conditions†	AC Switching Characteristics							Unit
					-30°C *		+25°C			+85°C *		
					Min	Max	Min	Typ	Max	Min	Max	
Propagation Delay	t++, t- -	C_n	C_{n+4}	A0,A1,A2,A3	1.0	5.1	1.1	3.1	5.0	1.1	5.4	ns
Rise Time, Fall Time	t+,t-	C_n	C_{n+4}	A0,A1,A2,A3	1.0	3.2	1.0	2.0	3.0	1.0	3.2	ns
Propagation Delay	t++, t+-	C_n	F1	A0	1.7	7.2	2.0	4.5	7.0	2.0	7.5	ns
	t-+, t- -	↓	↓	↓	1.7	7.2	2.0	4.5	7.0	2.0	7.5	↓
Rise Time, Fall Time	t+, t-	↓	↓	↓	1.3	5.3	1.5	3.0	5.0	1.5	5.3	↓
Propagation Delay	t++, t+-	A1	F1		2.6	10.4	3.0	6.5	10	3.0	10.8	ns
	t-+, t- -	↓	↓		2.6	10.4	3.0	6.5	10	3.0	10.8	↓
Rise Time, Fall Time	t+, t-	↓	↓		1.3	5.4	1.5	3.0	5.0	1.5	5.3	↓
Propagation Delay	t++, t- -	A1	P_G	S0,S3	1.6	7.0	2.0	5.0	6.5	2.0	7.0	ns
Rise Time, Fall Time	t+, t-	A1	P_G	S0,S3	0.8	3.7	1.1	2.0	3.5	1.1	3.8	ns
Propagation Delay	t++, t- -	A1	G_G	A0,A2,A3,C_n	1.1	7.4	2.0	4.5	7.0	1.3	7.7	ns
Rise Time, Fall Time	t+, t-	A1	G_G	A0,A2,A3,C_n	1.2	5.1	1.5	4.0	5.0	1.2	5.3	ns
Propagation Delay	t+-, t-+	A1	C_{n+4}	A0,A2,A3,C_n	1.7	7.3	2.0	5.0	7.0	2.0	7.8	ns
Rise Time, Fall Time	t+, t-	A1	C_{n+4}	A0,A2,A3,C_n	1.0	3.1	1.0	2.0	3.0	1.0	3.2	ns
Propagation Delay	t++, t-+	B1	F1	S3, C_n	2.7	11.3	3.0	8.0	11	3.0	11.9	ns
Rise Time, Fall Time	t+, t-	B1	F1	S3,C_n	1.2	5.3	1.5	3.5	5.0	1.5	5.3	ns
Propagation Delay	t++, t- -	B1	P_G	S0, A1	1.6	7.7	2.0	6.0	7.5	2.0	8.0	ns
Rise Time, Fall Time	t+, t-	B1	P_G	S0, A1	1.0	3.6	1.1	2.0	3.5	1.1	3.9	ns
Propagation Delay	t++, t- -	B1	G_G	S3, C_n	1.7	8.2	2.0	6.0	8.0	2.0	8.6	ns
Rise Time, Fall Time	t+, t-	B1	G_G	S3.C_n	1.4	5.2	1.5	3.0	5.0	1.2	5.4	ns
Propagation Delay	t+-, t-+	B1	C_{n+4}	S3, C_n	1.8	8.2	2.0	6.0	8.0	2.0	8.7	ns
Rise Time, Fall Time	t+, t-	B1	C_{n+4}	S3,C_n	0.9	3.1	1.0	2.0	3.0	1.0	3.2	ns
Propagation Delay	t++, t+-	M	F1	–	2.4	10.3	3.0	6.5	10	3.0	10.8	ns
Rise Time, Fall Time	t+, t-	M	F1	–	1.1	5.1	1.5	4.0	5.0	1.5	5.3	ns
Propagation Delay	t+-, t-+	S1	F1	A1, B1	2.5	10.7	3.0	6.5	10	3.0	10.8	ns
Rise Time, Fall Time	t+, t-	S1	F1	A1, B1	1.0	5.4	1.5	3.0	5.0	1.5	5.4	ns
Propagation Delay	t-+, t+-	S1	P_G	A3, B3	1.7	8.3	2.0	6.0	8.0	2.0	8.4	ns
Rise Time, Fall Time	t+, t-	S1	P_G	A3, B3	0.8	5.1	1.1	3.0	5.0	1.1	5.2	ns
Propagation Delay	t+-, t-+	S1	C_{n+4}	A3, B3	1.6	9.3	2.0	6.0	9.0	2.0	9.9	ns
Rise Time, Fall Time	t+, t-	S1	C_{n+4}	A3, B3	0.9	5.3	1.1	3.0	5.0	1.0	5.2	ns
Propagation Delay	t+-, t-+	S1	G_G	A3, B3	1.5	9.6	2.0	6.0	9.0	1.9	9.7	ns
Rise Time, Fall Time	t+, t-	S1	G_G	A3, B3	0.8	6.2	0.8	3.0	6.0	0.8	6.5	ns

†Logic high level (+1.11 Vdc) applied to pins listed. All other input pins are left floating or tied to +0.31 Vdc.
$V_{CC1} = V_{CC2} = +2.0$ Vdc, $V_{EE} = -3.2$ Vdc

*L Suffix Only

MC10182

MECL 10K SERIES

2-BIT ARITHMETIC LOGIC UNIT/FUNCTION GENERATOR

2-BIT ARITHMETIC LOGIC UNIT/FUNCTION GENERATOR

The MC10182 is a high-speed arithmetic logic unit capable of performing 4 logic operations and 4 arithmetic operations on two 2-bit words. Full internal carry is incorporated for arithmetic operation.

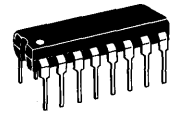
Arithmetic logic operations are selected by applying the appropriate binary word to the select inputs (S0 and S1) as indicated in the tables of arithmetic/logic functions. Group carry propagate (P_G) and carry generate (G_G) are provided for a second order look ahead carry using the MC10179. The internal carry is enabled by applying a low level voltage to the mode control input (M).

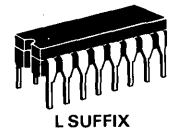
The MC10182 provides an alternate to the MC10181 four-bit ALU for applications not requiring the extended functions of the MC10181 or for applications requiring a 16-pin package. The MC10182 also differs from the MC10181 in that Word A and Word B are treated equally for addition and subtraction (A plus B, A minus B, B minus A).

P_D = 575 mW typ/pkg (No Load)

t_{pd} (typ): A1 to F = 7.5 ns
C_n to C_{n+2} = 2.7 ns
A1 to P_G = 6.5 ns
A1 to G_G = 5.5 ns
A1 to C_{n+2} = 7.0 ns
t_r, t_f = 2.5 ns typ (20%–80%)

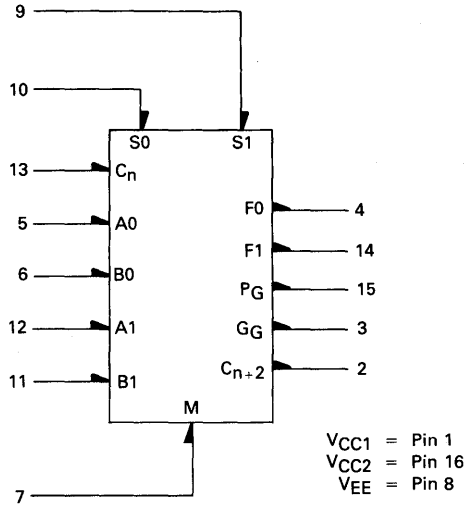
P SUFFIX
PLASTIC PACKAGE
CASE 648





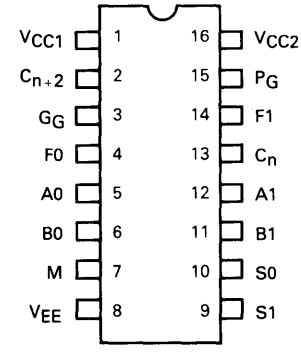
L SUFFIX
CERAMIC PACKAGE
CASE 620

LOGIC DIAGRAM

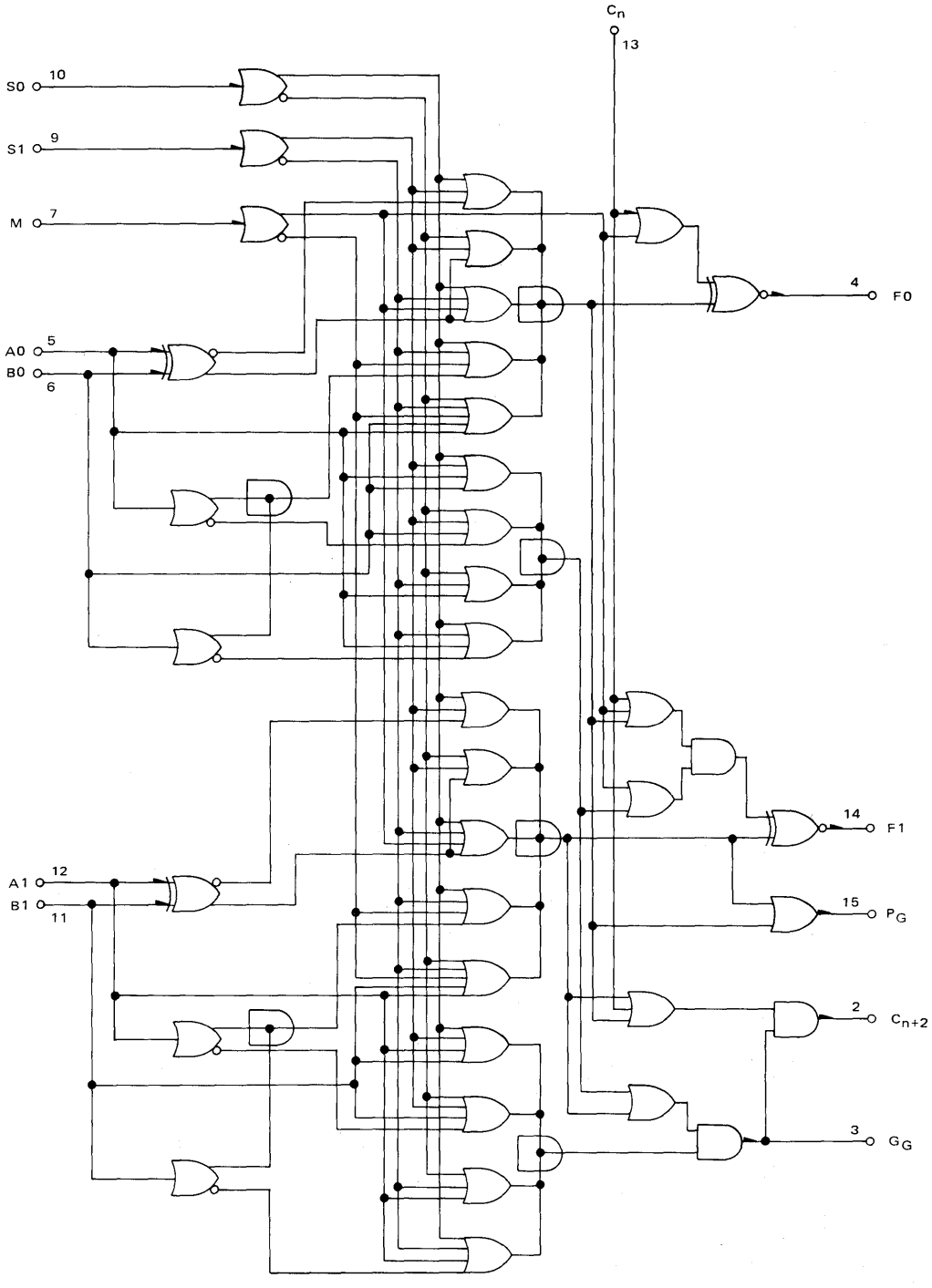


Function Select		POSITIVE LOGIC	
		Logic Function M is High	Arithmetic Operation M is Low
S1	S0	F	F
L	L	F = A ⊙ B	F = $\overline{A}$ plus B plus Carry
L	H	F = A ⊕ B	F = $\overline{A}$ plus $\overline{B}$ plus Carry
H	L	F = A • B	F = A plus $\overline{B}$ plus Carry
H	H	F = A + B	F = A times 2

PIN ASSIGNMENT



POSITIVE LOGIC DIAGRAM



TRUTH TABLE

Input						M	L					L					L					L					L					H					H					H					H				
						S1	L					L					H					H					L					L					H					H				
						S0	L					H					L					H					L					H					L					H				
A1	B1	A0	B0	C_n	F1	F0	P_G	G_G	C_{n+2}	F1	F0	P_G	G_G	C_{n+2}	F1	F0	P_G	G_G	C_{n+2}	F1	F0	P_G	G_G	C_{n+2}	F1	F0	P_G	G_G	C_{n+2}	F1	F0	P_G	G_G	C_{n+2}	F1	F0	P_G	G_G	C_{n+2}	F1	F0	P_G	G_G	C_{n+2}	F1	F0	P_G	G_G	C_{n+2}
L	L	L	L	L	L	L	H	L	L	H	H	L	H	L	H	H	L	H	L	L	L	H	H	L	H	H	H	H	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
L	L	L	L	H	L	H	H	L	L	L	L	L	H	H	L	L	L	H	H	L	H	H	L	L	H	H	H	L	L	L	L	H	H	L	L	L	H	H	L	H	H	L	L	L	H	H	L	H	H
L	L	L	H	L	L	H	H	L	L	L	L	H	H	H	H	L	H	L	L	L	L	H	L	L	H	H	H	H	L	L	L	L	L	L	H	H	L	L	H	H	L	L	H	H	L	L	H	H	L	L
L	L	L	H	H	H	L	H	L	L	L	H	H	H	H	H	H	H	L	L	L	H	H	L	L	H	L	H	L	L	L	H	H	H	H	L	L	L	L	L	L	H	H	L	L	H	H	L	L	H	L
L	L	H	L	L	L	H	H	L	L	H	L	H	L	L	L	L	H	H	H	H	L	H	L	L	H	H	H	L	L	L	H	H	L	L	L	L	L	H	L	L	H	H	L	L	H	H	L	L	H	L
L	L	H	L	H	H	L	H	L	L	H	H	L	H	L	L	L	H	H	H	H	L	H	L	L	H	H	H	L	L	L	H	H	L	L	L	L	L	H	L	L	H	H	L	L	H	H	L	L	H	L
L	L	H	H	L	H	L	H	L	L	H	H	H	L	L	H	H	L	H	L	H	L	H	L	L	H	H	H	L	L	L	H	H	L	L	L	L	L	H	L	L	H	H	L	L	H	H	L	L	H	L
L	L	H	H	H	H	H	H	L	L	L	L	L	H	H	H	H	L	H	L	H	L	H	L	L	H	H	H	L	L	L	H	H	L	L	L	L	L	H	L	L	H	H	L	L	H	H	L	L	H	L
L	H	L	L	L	H	L	H	L	L	L	H	H	H	H	L	H	H	L	L	L	L	H	L	L	H	H	L	L	L	L	L	L	L	L	H	L	H	L	L	H	H	L	L	L	L	L	L	H	L	L
L	H	L	L	H	H	H	H	L	L	H	L	H	H	H	H	L	H	L	L	L	H	H	L	L	H	H	L	L	L	L	L	L	L	L	H	L	H	L	L	H	H	L	L	L	L	L	L	H	L	L
L	H	L	H	L	H	H	L	H	L	H	H	L	H	H	L	L	H	H	H	L	L	H	L	L	H	H	L	L	L	L	L	L	L	L	H	H	H	L	L	H	H	L	L	L	L	L	L	H	H	L
L	H	L	H	H	L	L	L	H	H	H	H	H	H	H	L	H	H	L	L	L	L	H	L	L	H	H	L	L	L	L	L	L	L	L	H	H	H	L	L	H	H	L	L	L	L	L	L	H	H	L
L	H	H	L	L	H	H	L	H	L	L	L	H	H	H	H	L	H	L	L	H	H	H	L	L	H	H	L	L	L	L	L	L	L	L	H	H	H	L	L	H	H	L	L	L	L	L	L	H	H	L
L	H	H	L	H	L	L	L	H	H	L	H	H	H	H	H	H	H	L	L	H	H	H	L	L	H	H	L	L	L	L	L	L	L	L	H	H	H	L	L	H	H	L	L	L	L	L	L	H	H	L
L	H	H	H	L	L	L	H	H	H	L	H	H	H	H	H	L	H	L	L	H	L	H	L	L	H	H	H	L	L	L	H	H	L	L	L	L	H	H	L	L	H	H	L	L	H	H	L	L	H	L
L	H	H	H	H	L	H	H	H	H	H	L	H	H	H	H	L	H	L	L	H	H	H	L	L	H	H	H	L	L	L	H	H	L	L	L	L	H	H	L	L	H	H	L	L	H	H	L	L	H	L
H	L	L	L	L	H	L	H	L	L	L	H	H	L	H	L	H	H	H	H	L	L	H	H	H	L	H	H	L	L	L	L	L	H	L	H	H	H	L	L	L	L	H	L	L	L	L	H	H	H	H
H	L	L	L	H	H	H	H	L	L	H	L	H	H	H	L	H	H	H	H	L	H	H	H	H	L	H	H	L	L	L	L	L	H	H	H	L	L	L	L	L	H	H	L	L	L	L	H	H	H	H
H	L	L	H	L	H	H	L	H	L	H	L	L	H	H	L	L	H	H	H	L	L	H	H	H	L	L	L	H	L	L	L	L	L	L	H	H	H	L	L	L	L	H	H	H	L	L	L	H	H	H
H	L	L	H	H	L	L	L	H	H	H	H	H	L	H	L	H	H	H	H	L	H	H	H	H	L	L	L	H	H	H	H	L	L	L	H	H	H	L	L	L	L	H	H	H	L	L	L	H	H	H
H	L	H	L	L	H	H	L	H	L	L	L	H	L	H	H	L	H	H	H	L	L	H	H	H	L	L	L	H	L	H	H	L	L	L	H	H	H	L	L	L	L	H	H	H	L	L	L	H	H	H
H	L	H	L	H	L	L	L	H	H	L	H	H	L	H	H	H	H	H	H	L	L	H	H	H	L	H	H	H	L	L	L	L	L	L	H	H	H	L	L	L	L	H	H	H	L	L	L	H	H	H
H	L	H	H	L	L	L	H	H	H	L	H	H	L	H	H	L	H	H	H	L	H	H	H	H	L	L	L	H	L	H	H	L	L	L	H	H	H	L	L	L	L	H	H	H	L	L	L	H	H	H
H	L	H	H	H	L	H	H	H	H	H	L	H	H	H	H	L	H	H	H	L	H	H	H	H	L	H	H	H	L	L	L	L	L	L	H	H	H	L	L	L	L	H	H	H	L	L	L	H	H	H
H	H	L	L	L	L	L	H	H	H	H	H	L	H	L	H	H	H	H	H	H	H	H	H	H	L	L	L	H	L	H	H	H	H	L	H	H	H	L	L	L	L	H	H	H	L	L	L	H	H	H
H	H	L	L	H	L	H	H	H	H	L	L	L	H	H	L	L	L	H	H	L	H	H	H	H	L	L	L	H	L	H	H	H	H	L	H	L	H	H	L	L	L	H	H	H	L	L	L	H	H	H
H	H	L	H	L	L	H	H	H	H	L	L	H	H	H	H	L	H	L	L	L	L	H	H	H	H	L	H	H	L	H	H	H	H	L	H	L	H	H	L	L	L	H	H	H	L	L	L	H	H	H
H	H	L	H	H	H	L	H	H	H	L	H	H	H	H	H	H	L	L	L	L	L	H	H	H	H	L	H	H	L	H	H	H	H	L	H	H	H	H	L	L	L	H	H	H	L	L	L	H	H	H
H	H	H	L	L	L	H	H	H	H	H	L	H	H	H	H	L	H	H	H	H	L	H	H	H	H	L	H	H	L	H	H	L	L	L	H	H	H	H	L	L	L	H	H	H	L	L	L	H	H	H
H	H	H	L	H	H	L	H	H	H	H	H	L	H	H	L	L	H	H	H	H	L	H	H	H	H	L	H	H	L	H	H	L	L	L	H	H	H	H	L	L	L	H	H	H	L	L	L	H	H	H
H	H	H	H	L	H	L	H	H	H	H	H	H	L	H	L	H	H	H	H	H	L	H	H	H	H	L	H	H	L	L	L	H	L	L	H	H	H	H	L	L	L	H	H	H	L	L	L	H	H	H
H	H	H	H	H	L	H	H	H	H	L	L	L	H	H	H	H	H	H	H	H	L	H	H	H	H	L	H	H	L	L	L	H	L	L	H	H	H	H	L	L	L	H	H	H	L	L	L	H	H	H

These outputs are not normally used during logic operation.

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts.

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10182 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	152	–	110	138	–	152	mAdc	–	–	–	–	8	1,16
Input Current	I_{inH}	7	–	350	–	–	220	–	220	μAdc	7	–	–	–	8	1,16
		5	–	620	–	–	390	–	390		5	–	–	–		
		6	–	460	–	–	290	–	290		6	–	–	–		
		13	–	560	–	–	350	–	350		13	–	–	–		
	I_{inL}	5	0.5	–	0.5	–	–	0.3	–	μAdc	–	5	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	5,6,11	–	–	–	8	1,16
		3				–					12,13	–	–	–		
		4				–						–	–	–		
		14				–						–	–	–		
		15				–						–	–	–		
Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	7,9,10	–	–	–	8	1,16
		3				–						–	–	–		
		4				–						–	–	–		
		14				–						–	–	–		
		15				–						–	–	–		
Logic "1" Threshold Voltage	V_{OHA}	2	-1.080	–	-0.980	–	–	-0.910	–	Vdc	6,7,9	–	5	–	8	1,15
		3		–		–	–		–		5,10,13	–	6	–		
		4		–		–	–		–		7,9,10	–	5	–		
		14		–		–	–		–		9,10	–	5	–		
		15		–		–	–		–		6,7,9	–	5	–		
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.655	–	–	-1.630	–	-1.595	Vdc	6,7,9	–	–	5	8	1,16
		3	–		–	–		–			5,10,13	–	–	6		
		4	–		–	–		–			7,9,10	–	–	5		
		14	–		–	–		–			9,10	–	–	5		
		15	–		–	–		–			6,7,9	–	–	5		
Switching Times												+1.11 V	Pulse In	Pulse Out	-3.2V	+2.0 V
(50 Ω Load)	t_{13+2+}	2	1.5	5.9	1.5	2.7	5.6	1.6	6.2	ns	–	10	13	2	8	1,16
Propagation Delay	t_{13+4-}	4	1.5	5.9	1.5	2.7	5.6	1.6	6.2		–	5	13	4		
	t_{5+4-}	4	2.3	10.5	2.3	7.0	10	2.4	11		–	7	5	4		
	t_{6-4-}	4				7.0					–	9,10	6	4		
	t_{12-14+}	14				7.0					–	–	12	14		
	t_{11-14-}	14				7.0					–	–	11	14		
	t_{5+2+}	2				7.0					–	9	5	2		
	t_{12-2-}	2				7.0					–	9,10	12	2		
	t_{6-2-}	2				7.0					–	10	6	2		
	t_{11+2+}	2	2.8	12.6	2.8	7.0	12	2.9	13.2		–	12	11	2		
	t_{5-15-}	15	2.3	10.5	2.3	6.5	10	2.4	11		–	10	5	15		
	t_{6+15+}	15				6.5					–	10	6	15		
	t_{5+3-}	3				5.5					–	10	5	3		
	t_{6-3+}	3				5.5					–	9	6	3		
	t_{7-4+}	4	2.3	10.5	2.3	4.0	10	2.4	11		–	9,10	7	4		
	t_{10-4-}	4	2.3	10.5	2.3	6.0	10	2.4	11		–	6,11,13	10	4		
Rise Time (20% to 80%)	t_{4+}	4	1.5	4.7	1.5	2.5	4.5	1.6	5.0	ns	–	–	5	4	8	1,16
Fall Time (20% to 80%)	t_{4-}	4	1.5	4.7	1.5	2.5	4.5	1.6	5.0	ns	–	–	5	4	8	1,16

MC10183

MECL 10K SERIES

4 X 2 MULTIPLIER

4 X 2 MULTIPLIER

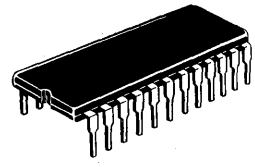
The MC10183 is a 4 x 2 bit multiplier that can multiply 2's complement numbers producing a 2's complement product without correction. The device can be used as a 4 x 2 bit multiplier cell to build larger iterative arrays.

The part performs the function defined as F = XY + K, where K is an input field used to add partial products in an array or to add a constant to the least significant part of the array product. The algorithm used is a modified Booth's algorithm or multiplier coding technique. The device consists of a shift network and an adder/subtracter in which 0, 1 times X, or 2 times X is either added or subtracted to input constant K. The Y inputs control multiplication as shown in the Truth Table.

The most significant digit in a word carries a negative weight allowing 2's complement numbers of various lengths to be multiplied. An M-bit by N-bit multiplication produces an M + N bit product.

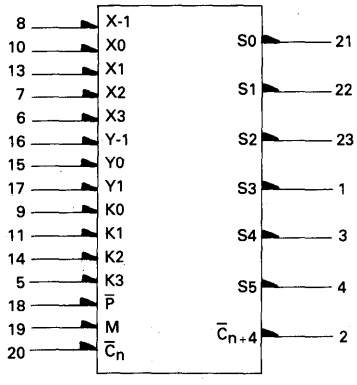
The $\overline{P}$ polarity input allows multiplication in either positive logic ($\overline{P}$ = high) or negative logic ($\overline{P}$ = low) representation. Also, mode control M inverts $\overline{C}_n$ when high and passes $\overline{C}_n$ directly when left low.

P_D = 760 mW typ/pkg (No Load)
t_{pd} = 50 ns typ (8 x 8 bit product)
t_r, t_f = 3.5 ns typ (20%–80%)



L SUFFIX
CERAMIC PACKAGE
CASE 623

LOGIC DIAGRAM



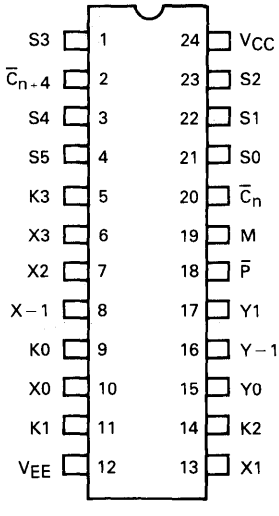
X-1, X0, X1, X2, X3	Multiplicand Inputs
Y-1, Y0, Y1	Multiplier Inputs
K0, K1, K2, K3	Constant Inputs
$\overline{C}_n$	Carry Input
$\overline{P}$	Polarity Control
M	Mode Control
S0, S1, S2, S3, S4, S5	Product Output
$\overline{C}_{n+4}$	Carry Output

V_{CC} = Pin 24
V_{EE} = Pin 12

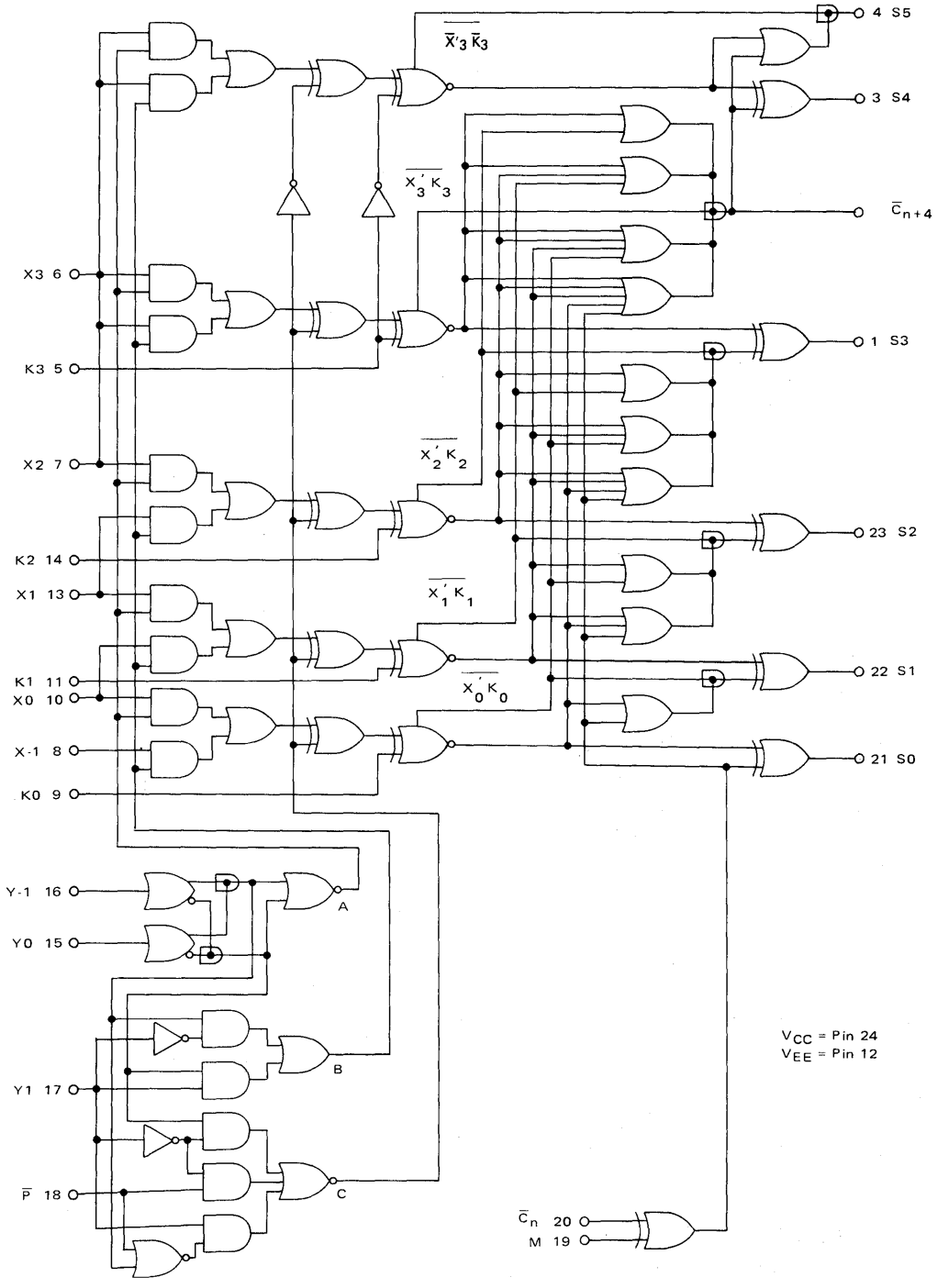
TRUTH TABLE

Y-2	Y0	Y1	$\overline{P}$	A	B	C	Operation	Complementor
L	L	L	L	L	L	L	Add Zero	Direct
H	L	L	L	H	L	L	Add 1X	Direct
L	H	L	L	H	L	L	Add 1X	Direct
H	H	L	L	L	H	L	Add 2X	Direct
L	L	H	L	L	H	H	Sub 2X	Invert
H	L	H	L	H	L	H	Sub 1X	Invert
L	H	H	L	H	L	H	Sub 1X	Invert
H	H	H	L	L	L	H	Sub Zero	Invert
L	L	L	H	L	L	L	Sub Zero	Direct
H	L	L	H	H	L	H	Sub 1X	Invert
L	H	L	H	H	L	H	Sub 1X	Invert
H	H	L	H	L	H	H	Sub 2X	Invert
L	L	H	H	L	H	L	Add 2X	Direct
H	L	H	H	H	L	L	Add 1X	Direct
L	H	H	H	H	L	L	Add 1X	Direct
H	H	H	H	L	L	H	Add Zero	Invert

PIN ASSIGNMENT



POSITIVE LOGIC DIAGRAM



ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown for only selected inputs and outputs. Other inputs and outputs are tested in a similar manner.

@Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10183 TEST LIMITS -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	12	–	201	–	146	183	–	201	mAdc	–	–	–	–	12	24
Input Current	I_{inH}	6	–	390	–	–	245	–	245	μAdc	6	–	–	–	12	24
		8	–	350	–	–	220	–	220	↓	8	–	–	–	↓	↓
		18	–	320	–	–	200	–	220	↓	18	–	–	–	↓	↓
	I_{inL}	8	0.5	–	0.5	–	–	0.3	–	μAdc	–	8	–	–	12	24
Logic "1" Output Voltage	V_{OH}	2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	8,16,19	–	–	–	12	24
		21	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	8,16,19	–	–	–	12	24
Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	17,18,19,20	–	–	–	12	24
		21	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	17,18,19,20	–	–	–	12	24
Logic "1" Threshold Voltage	V_{OHA}	2	-1.080	–	-0.980	–	–	-0.910	–	Vdc	8,16,19	–	–	5	12	24
		21	-1.080	–	-0.980	–	–	-0.910	–	Vdc	8,16,19	–	–	15	12	24
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.655	–	–	-1.630	–	-1.595	Vdc	8,16,19	–	5	–	12	24
		21	–	-1.655	–	–	-1.630	–	-1.595	Vdc	8,16,19	–	10	–	12	24
Switching Times (50 Ω Load)													Pulse In	Pulse Out	-3.2 Vdc	-2.0 Vdc
Propagation Delay	t_{20+2-}	2	1.0	5.3	1.0	4.5	5.0	1.0	5.5	ns	–	–	20	2	12	24
	t_{20+22+}	22	1.8	8.4	1.8	6.0	8.0	1.8	8.8	↓	–	–	20	22	↓	↓
	t_{20+3-}	3	1.8	8.4	1.8	8.0	8.0	1.8	8.8	↓	–	–	20	3	↓	↓
	t_{9+2-}	2	1.6	7.3	1.6	5.5	7.0	1.6	7.7	↓	–	–	9	2	↓	↓
	t_{9+1+}	1	2.5	11	2.5	8.0	10.5	2.5	11.5	↓	–	–	9	1	↓	↓
	t_{14+3-}	3	2.5	11	2.5	8.5	10.5	2.5	11.5	↓	–	–	14	3	↓	↓
	t_{10-2+}	2	1.8	8.4	1.8	6.0	8.0	1.8	8.8	↓	–	–	10	2	↓	↓
	t_{13+23+}	23	2.5	11	2.5	9.5	10.5	2.5	11.5	↓	–	–	13	23	↓	↓
	t_{14-3+}	3	2.5	11	2.5	10.0	10.5	2.5	11.5	↓	–	–	14	3	↓	↓
	t_{15-2-}	2	3.2	14.1	3.2	10.5	13.5	3.2	14.8	↓	–	–	15	2	↓	↓
	t_{15+23+}	23	↓	↓	↓	10.5	↓	↓	↓	↓	–	–	15	23	↓	↓
	t_{15-3+}	3	↓	↓	↓	11.5	↓	↓	↓	↓	–	–	15	3	↓	↓
Rise Time (20% to 80%)	t_{22+}	22	1.0	6.3	1.0	3.5	6.0	1.0	6.6	ns	–	–	9	22	12	24
Fall Time (20% to 80%)	t_{22-}	22	1.0	6.3	1.0	3.5	6.0	1.0	6.6	ns	–	–	9	22	12	24

MC10183 APPLICATIONS INFORMATION

The MC10183 is a 4 X 2 bit multiplier that uses a modified Booth's algorithm or multiplier coding technique. The device generates the function: S = X • Y + K

where

X = 4-bit multiplicand
Y = 2-bit multiplier
K = 4-bit constant

The addition of the constant allows the device to be used in an iterative array of parts for larger words. The algorithm for multiplication is:

Y_{i-1}	Y_i	Y_{i+1}	Operation
0	0	0	add zero
1	0	0	add multiplicand
0	1	0	add multiplicand
1	1	0	add 2 times multiplicand
0	0	1	sub 2 times multiplicand
1	0	1	sub multiplicand
0	1	1	sub multiplicand
1	1	1	sub zero

DEVICE OPERATION

The device consists of three main sections; a decoder, a shifter, and a high speed look-ahead carry adder/subtractor.

1. The decoder uses the Y inputs to generate the control signals for the shifter and the adder/subtractor. Also, the polarity control $\overline{P}$ is used to allow operation in either positive or negative logic. Referring to the logic diagram, the control signals are:

$A = Y_{-1} \oplus Y_0$ (1 times multiplicand)

$B = Y_{-1}Y_0\overline{Y}_1 + \overline{Y}_{-1}\overline{Y}_0Y_1$ (2 times multiplicand)

$\overline{C} = \overline{P}\overline{Y}_1 + \overline{Y}_{-1}\overline{Y}_0\overline{Y}_1 + PY_1(\overline{Y}_{-1} + \overline{Y}_0)$ (add/subtract)

The $\overline{P}$ input is tied to a high logic level or ground for positive logic operation.

2. The shift network is a multiplexer that ripples through number X (1 times multiplicand), shifts number X by one bit (2 times multiplicand), or sets the output to zero. The network is controlled by decoder functions A and B which are generated in accordance with the multiply algorithm.

3. The adder/subtractor follows the shift network which performs the actual multiplication. The adder/subtractor produces the sum or difference of the newly formed partial product and the accumulated partial product (constant K). Subtraction is accomplished by inverting the shifted product and doing a two's complement addition. The carry in of the least significant bit must be a logic one during subtraction.

The two most significant bits of the product are used for sign detection and overflow for a two's complement multiply. These outputs are used only as the two most significant bits of the accumulated product at each addition level within a multiplier array.

Overflow can occur either as the result of 2 times the multiplicand, and/or of an addition or subtraction. To show all possible conditions (including overflow), the most significant bit (S5) must carry a negative binary weight. To show this for a 4 X 2 bit multiply plus constant, consider the following addition:

$X'_4 \cdot X'_3\ X'_2\ X'_1\ X'_0$	shifter outputs
+ K3 • K3 K2 K1 K0	constant
S5 S4 • S3 S2 S1 S0	sum

The shift network produces 5 product bits (maximum value of 2 times multiplicand) and a 4-bit constant is added to the least signficant end of the product. The K3 bit is repeated to hold the proper binary weight. Because S5 has a negative weight all possible combinations are represented properly.

If no overflow occurs S4 = S5, and S4 can be used as a sign bit. Under overflow conditions S4 ≠ S5, and overflow can be detected by EXCLUSIVE-ORing S4 and S5.

USAGE RULES

The MC10183 can be used in larger arrays to produce a two's complement product of 2 two's complement numbers. The following rules apply:

1. For an M-bit by N-bit multiplier, an (M+N)-bit product is formed. The number of MC10183's equals (M * N)/8. As an example, an 8 X 8 bit (Figure 1) array requires (8X8)/8 = 8 packages.

2. The MC10183 can be used directly for both positive logic and negative logic representations. The $\overline{P}$ input can be tied to ground or to a high logic level for positive logic operation, or left at a low logic level for negative logic operation.

3. The M mode control input is used to invert $\overline{C}_n$ when placed at a high logic level or ground, or passes $\overline{C}_n$ directly when left as a low logic level. When $\overline{C}_n$ is driven from $\overline{C}_{n+4}$ of a preceding device, M control is left in a low logic state. When $\overline{C}_n$ is the least significant input carry bit for a level of addition within an array, $\overline{C}_n$ is tied to Y_1 of the same device, and the M input is placed at a high logic level. Y_1 controls when subtraction occurs, and carry in must be equal to a logic one during subtraction.

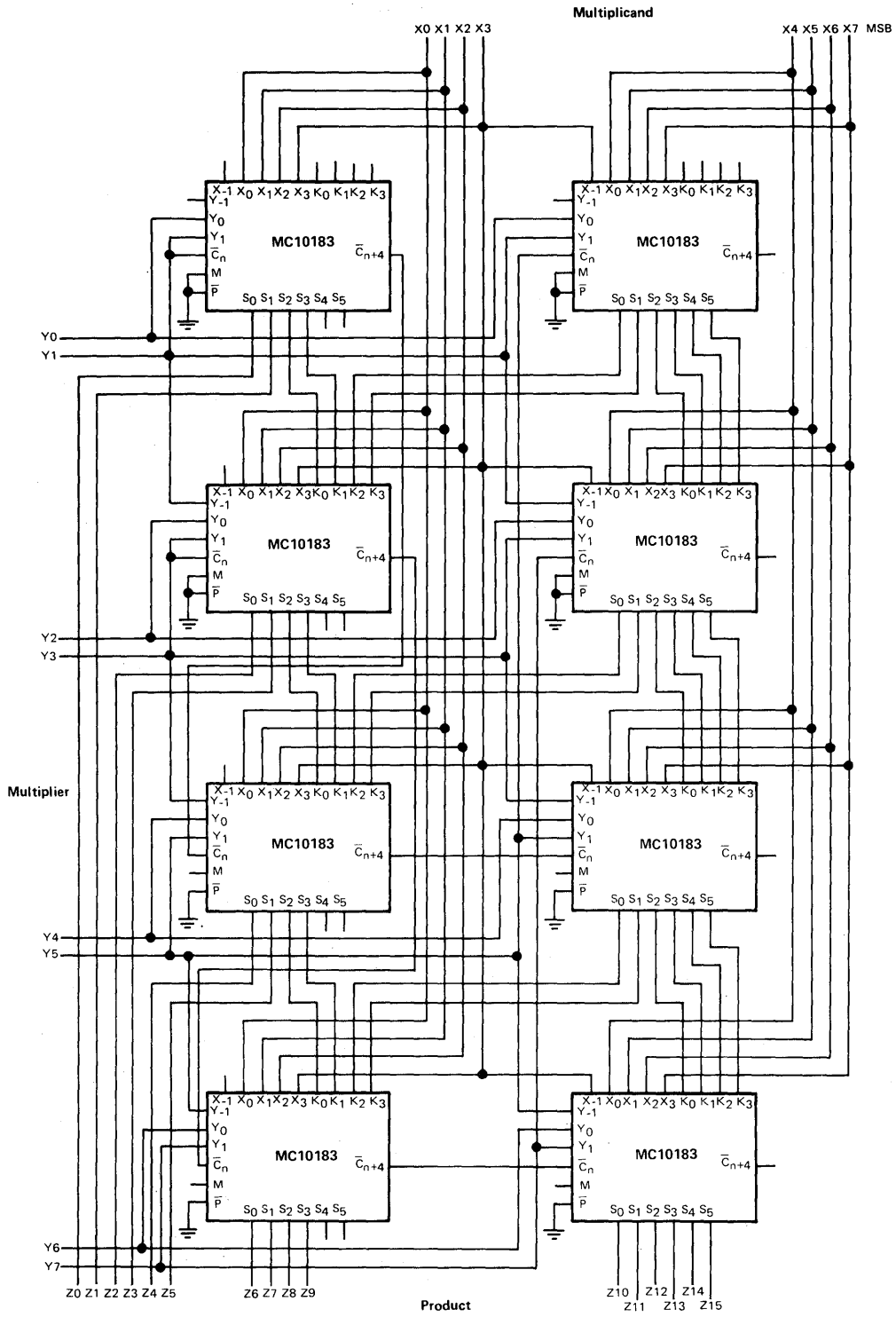


FIGURE 1 – 8-BIT X 8-BIT 2's COMPLEMENT MULTIPLIER

8 X 4 BIT EXAMPLE

Figure 2 shows 4 MC10183's in an 8 X 4 bit array. A 12-bit two's complement product is produced from a 4-bit multiplier and an 8-bit multiplicand. The array is used for positive logic representation, and all $\overline{P}$ inputs are tied to ground. At the first level of multiplication, the X_{-1} and Y_{-1} inputs are left open (logic "0") because the initial condition is treated as an add operation. The K inputs are used to add the accumulated partial product at each level of the array. If the initial partial product is zero, the least significant K inputs are left at a zero logic state (CONSTANT inputs in the figure). However, these inputs can also be used to add a constant to the least significant end of the product.

When the MC10183 is expanded to longer numbers, the carry out ($\overline{C}_{n+4}$) of a device must be rippled to the carry in ($\overline{C}_n$) of the next most significant device at the same level of multiplication. The least significant device must have the carry input equal to zero for an add and equal to one for a subtraction. In observing the multiplication algorithm y_{i+1} is always equal to 1 for a subtraction, and the carry input can be tied to Y_1. However, the M mode input must be tied to ground for this device to invert the carry input ($\overline{C}_n$) because the input requires a complemented signal.

The S4 and S5 outputs are used only at the most significant part of the array. These two sum outputs only have meaning as the two most significant bits of a two's complement number.

OTHER ARRAYS

The normal parallelogram structure consists of several stages, each multiplying two bits of multiplier times the multiplicand and adds the partial product. In larger arrays, faster configurations can be made by moving some multiplier blocks while maintaining the relative weight of each partial product. The typical times possible for various N-bit X N-bit arrays are:

Number of Bits	Total Multiply Time (ns)	Package Count
8	43	8
12	67	18
16	90	32

The times do not include wiring delays.

Because of the versatility of the MC10183, many other types of arrays can also be built. Faster arrays using additional adders, pipeline techniques, one's complement and magnitude multipliers, and truncated product multipliers can all be built.

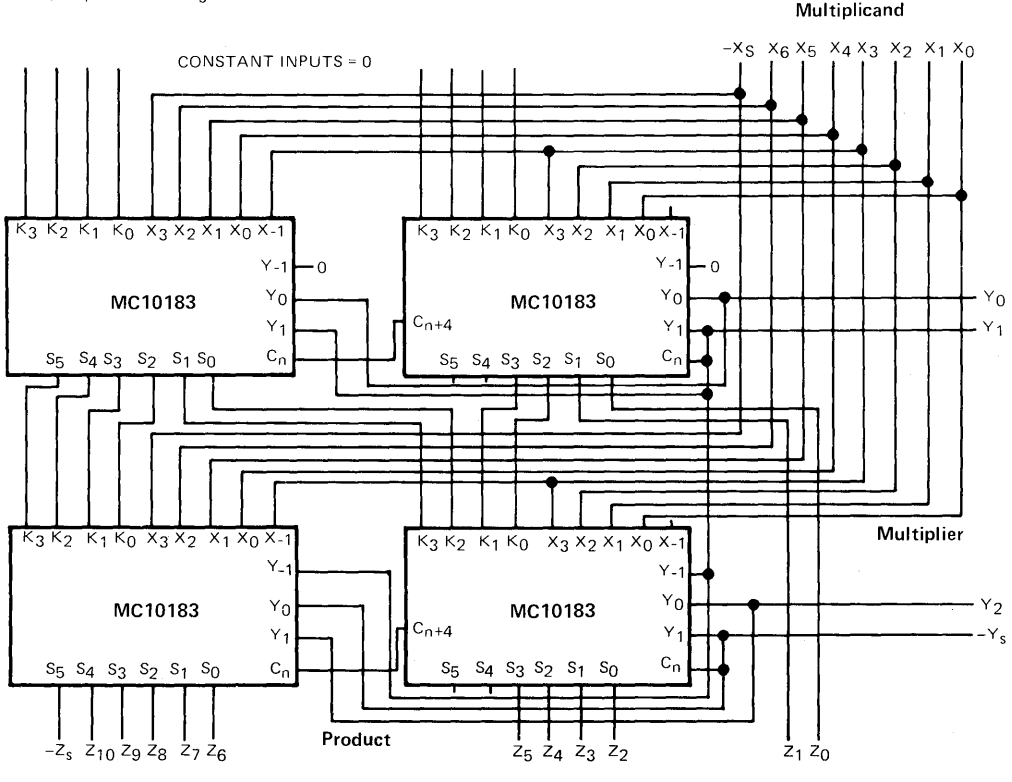


FIGURE 2 – 8-BIT BY 4-BIT 2's COMPLEMENT MULTIPLIER

MOTOROLA

MC10186

HEX "D" MASTER-SLAVE FLIP-FLOP/WITH RESET

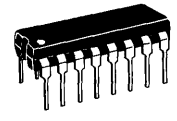
The MC10186 contains six high-speed, master slave type "D" flip-flops. Clocking is common to all six flip-flops. Data is entered into the master when the clock is low. Master to slave data transfer takes place on the positive-going Clock transition. Thus, outputs may change only on a positive-going Clock transition. A change in the information present at the data (D) input will not affect the output information any other time due to the master-slave construction of this device. A common Reset is included in this circuit. Reset only functions when clock is low.

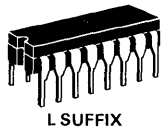
P_D = 460 mW typ/pkg (No Load)
f_{toggle} = 150 MHz (typ)
t_r, t_f = 2.0 ns typ (20%–80%)

MECL 10K SERIES

HEX "D" MASTER-SLAVE FLIP-FLOP/WITH RESET

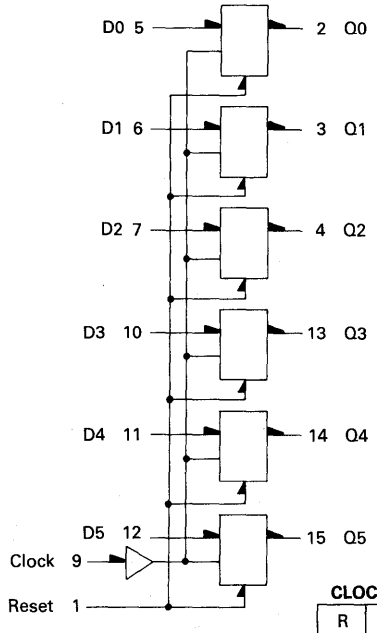
P SUFFIX
PLASTIC PACKAGE
CASE 648





L SUFFIX
CERAMIC PACKAGE
CASE 620

LOGIC DIAGRAM



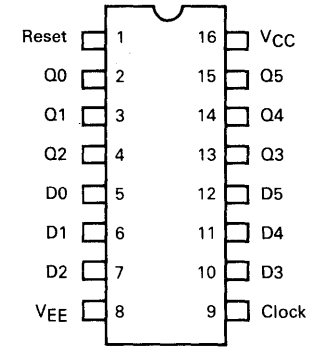
V_{CC} = Pin 16
V_{EE} = Pin 8

CLOCKED TRUTH TABLE

R	C	Q	Q_{n+1}
L	L	ϕ	Q_n
L	H	L	L
L	H	H	H
H	L	ϕ	L

ϕ = Don't Care
*A clock H is a clock transition from a low to a high state.

PIN ASSIGNMENT



ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown for only one data input, the clock input, and the reset input, and for one output. Other inputs and outputs tested in the same manner.

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-1.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10186 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	121	–	88	110	–	121	mAdc	–	–	–	–	8	16
Input Current	I_{inH}	5	–	350	–	–	220	–	220	μAdc	5	–	–	–	8	16
		9	–	495	–	–	310	–	310	↓	9	–	–	–	8	16
		1	–	920	–	–	575	–	575	↓	1	–	–	–	8	16
Input Leakage Current	I_{inL}	5	0.5	–	0.5	–	–	0.3	–	μAdc	–	5	–	–	8	16
Logic "1" Output Voltage	V_{OH}	2†	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	5	–	–	–	8	16
		15†	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	12	–	–	–	8	16
Logic "0" Output Voltage	V_{OL}	2†	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	–	5	–	–	8	16
		15†	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	–	12	–	–	8	16
Logic "1" Threshold Voltage	V_{OHA}	2†	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	5	–	8	16
		15†	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	12	–	8	16
Logic "0" Threshold Voltage	V_{OLA}	2†	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	–	5	8	16
		15†	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	–	12	8	16
Switching Times											+1.11 Vdc	+0.31 Vdc			-3.2 Vdc	+2.0 Vdc
Propagation Delay (50 Ω Load)	t_{1+3-}	3	1.6	4.6	1.6	2.5	4.5	1.6	5.0	ns	6	–	1,9	3	8	16
	t_{1+4-}	4	↓	↓	↓	2.5	↓	↓	↓	↓	7	–	1,9	4	↓	↓
	t_{9+2+}	2	↓	↓	↓	3.5	↓	↓	↓	↓	–	–	5,9	2	↓	↓
	t_{9+2-}	2	↓	↓	↓	3.5	↓	↓	↓	↓	–	–	↓	↓	↓	↓
Rise Time (20 to 80%)	t_{2+}	2	1.0	4.1	1.1	1.8	4.0	1.1	4.4	↓	–	–	↓	↓	↓	↓
Fall Time (20 to 80%)	t_{2-}	2	1.0	4.1	1.1	1.8	4.0	1.1	4.4	↓	–	–	↓	↓	↓	↓
Setup Time	t_{setup}	2	2.5	–	2.5	2.5	–	2.5	–	ns	–	–	5,9	2	8	16
Hold Time	t_{hold}	2	1.5	–	1.5	-1.5	–	1.5	–	ns	–	–	5,9	2	8	16
Toggle Frequency	f_{tog}	2	125	–	125	150	–	125	–	MHz	–	–	–	–	8	16

†Output level to be measured after a clock pulse. V_{IL} ⟋ V_{IH} appears at clock input (pin 9).

MOTOROLA

MC10188

MECL 10K SERIES

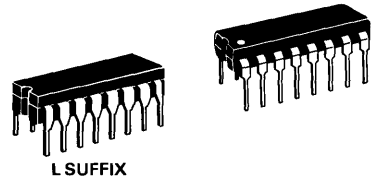
HEX BUFFER WITH ENABLE

The MC10188 is a high-speed hex buffer with a common Enable input. When Enable is in the high state, all outputs are in the low state. When Enable is in the low state, the outputs take the same state as the inputs.

Power Dissipation = 180 mW typ/pkg (No Load)
Propagation Delay = 2.0 ns typ (B - Q)
2.5 ns typ (A - Q)

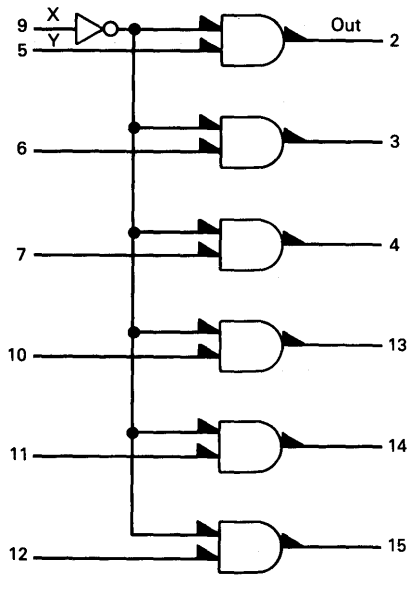
HEX BUFFER WITH ENABLE

P SUFFIX
PLASTIC PACKAGE
CASE 648



L SUFFIX
CERAMIC PACKAGE
CASE 620

LOGIC DIAGRAM

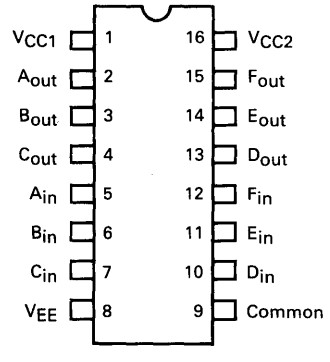


TRUTH TABLE

Inputs		Output
X	Y	OUT
L	L	L
L	H	H
H	L	L
H	H	L

V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

PIN ASSIGNMENT



ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for one set of conditions. Complete testing according to truth table.

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	—	46	—	42	—	46	mAdc	—	—	—	—	8	1,16
Input Current	I_{inH}	5	—	425	—	265	—	265	μAdc	5	—	—	—	8	1,16
	I_{inH}	9	—	460	—	290	—	290	μAdc	9	—	—	—	8	1,16
Logic "1" Output Voltage	V_{OH}	2	-1.060	-0.890	-0.960	-0.810	-0.890	-0.700	Vdc	5	—	—	—	8	1,16
Logic "0" Output Voltage	V_{OL}	2	1.890	-1.675	-1.850	-1.650	-1.825	-1.615	Vdc	—	9	—	—	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	2	-1.080	—	-0.980	—	-0.910	—	Vdc	—	—	5	—	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	2	—	-1.655	—	-1.630	—	-1.595	Vdc	—	—	—	5	8	1,16
Switching Times (50 Ω Load) Propagation Delay	t_{PHL} t_{PLH}								ns			Pulse In	Pulse Out	-3.2 V	+2.0 V
Enable		2	1.1	3.9	1.1	3.5	1.1	3.9		—	—	9	2	8	1, 16
Data		2	1.0	3.3	1.0	2.9	1.0	3.3		—	—	5	↓	↓	↓
Rise Time, Fall Time (20% to 80%)	t_{TLH}, t_{THL}	2	1.1	3.7	1.1	3.3	1.1	3.7	↓	—	—	↓	↓	↓	↓

MOTOROLA

MC10189

HEX INVERTER WITH ENABLE

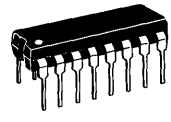
The MC10189 provides a high-speed Hex Inverter with a common Enable input. The hex inverting function is provided when Enable is in the low state. When Enable is in the high state all outputs are low.

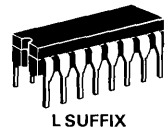
P_D = 200 mW typ/pkg (No Load)
t_{pd} = 2.0 ns typ (B – Q)
= 2.5 ns typ (A – Q)

MECL 10K SERIES

HEX INVERTER WITH ENABLE

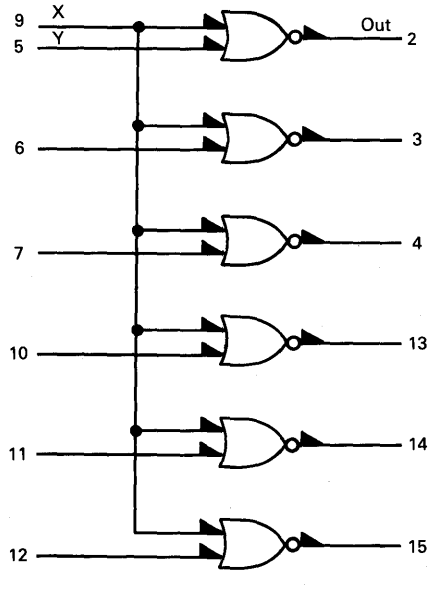
P SUFFIX
PLASTIC PACKAGE
CASE 648





L SUFFIX
CERAMIC PACKAGE
CASE 620

LOGIC DIAGRAM

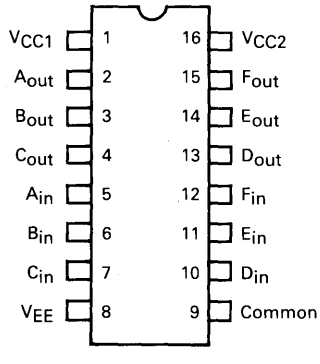


TRUTH TABLE

Inputs		Output
X	Y	OUT
L	L	H
L	H	L
H	L	L
H	H	L

V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

PIN ASSIGNMENT



ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for one set of conditions. Complete testing according to truth table.

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	—	44	—	40	—	44	mAdc	—	—	—	—	8	1,16
Input Current	I_{inH}	5	—	425	—	265	—	265	μAdc	5	—	—	—	8	1,16
	I_{inH}	9	—	890	—	555	—	555	μAdc	9	—	—	—	8	1,16
Logic "1" Output Voltage	V_{OH}	2	-1.060	-0.890	-0.960	-0.810	-0.890	-0.700	Vdc	—	5	—	—	8	1,16
Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.675	-1.850	-1.650	-1.825	-1.615	Vdc	9	—	—	—	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	2	-1.080	—	-0.980	—	-0.910	—	Vdc	—	—	—	5	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	2	—	-1.655	—	-1.630	—	-1.595	Vdc	—	—	5	—	8	1,16
Switching Times (50 Ω Load)									ns			Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{PHL}, t_{PLH}														
Enable		2	1.1	3.9	1.1	3.5	1.1	3.9		—	—	9	2	8	1, 16
Data		2	1.0	3.3	1.0	2.9	1.0	3.3		—	—	5			
Rise Time, Fall Time (20% to 80%)	t_{TLH}, t_{THL}	2	1.1	3.7	1.1	3.3	1.1	3.7		—	—				

MOTOROLA

MC10190

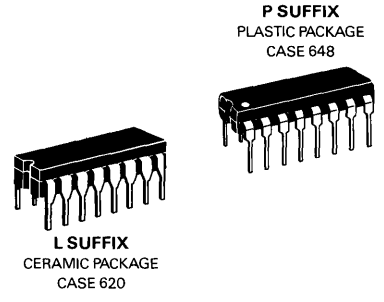
QUAD MST TO MECL 10,000 TRANSLATOR

The MC101090 is a quad translator for interfacing from IBM MST-type logic signals to standard MECL 10,000 logic levels. This circuit features differential inputs for high noise environments or may be used with single ended lines by tieing one of the inputs to ground. Since the MC10190 is designed to accept signals centered around ground, it is a useful interface element for many communication systems. When pin 9 is connected to V_{CC} the circuit becomes a line receiver for MECL signals. The outputs go to a low level whenever the inputs are left floating.

P_D = 215 mW typ/pkg (No Load)
t_{pd} = 2.5 ns typ
t_r, t_f = 2.0 ns typ (20%–80%)

MECL 10K SERIES

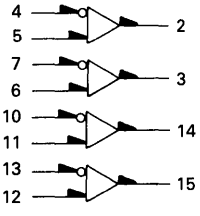
QUAD MST TO MECL 10,000 TRANSLATOR



P SUFFIX
PLASTIC PACKAGE
CASE 648

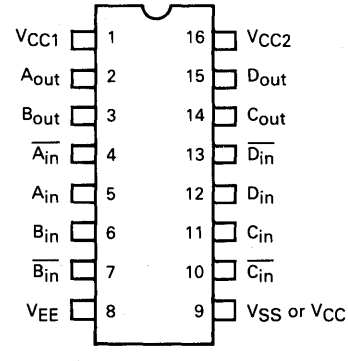
L SUFFIX
CERAMIC PACKAGE
CASE 620

LOGIC DIAGRAM



V_{CC1} = Pin1
V_{CC2} = Pin 16
V_{EE} = Pin 8
V_{SS} = Pin 9 Translator
V_{CC} = Pin 9 Receiver

PIN ASSIGNMENT



ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown for only selected inputs and outputs. Other inputs and outputs tested in the same manner.

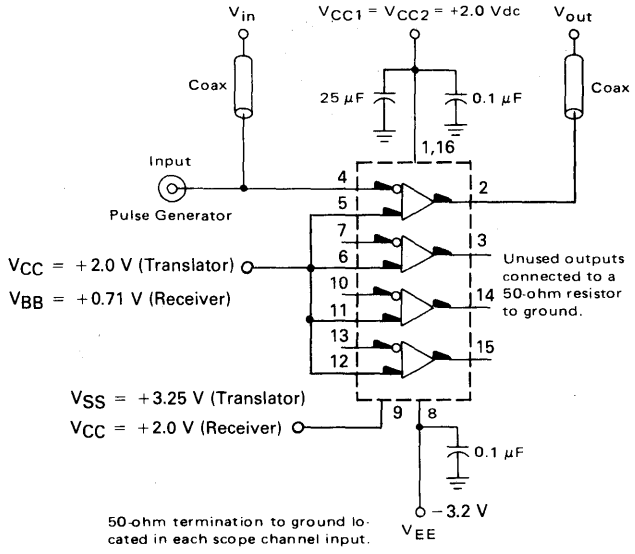
@ Test Temperature	V_{IHmax}	V_{ILmin}	V_{ILAmin}	V_{ILAmax}	V_{IHM}*	V_{ILM}*	V_{IHH}*	V_{ILH}*	V_{IHL}*	V_{ILL}*	V_{SS}*	V_{EE}
−30°C	-0.890	-1.890	-1.205	-1.500	+0.374	-0.523	+0.186	-0.850	-1.486	-2.53	+1.25	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	+0.440	-0.490	+0.186	-0.850	-1.486	-2.53	+1.25	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	+0.548	-0.454	+0.186	-0.850	-1.486	-2.53	+1.25	-5.2

Characteristic	Symbol	Pin Under Test	MC10190 Test Limits −30°C Min	−30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{ILAmin}	V_{ILAmax}	V_{IHM}*	V_{ILM}*	V_{IHH}*	V_{ILH}*	V_{IHL}*	V_{ILL}*	V_{SS}*	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	57	–	41	52	–	57	mAdc	4,6,10,12	5,7,11,13	–	–	–	–	–	–	–	–	9	8	1,16
	I_{CC}	9	–	27	–	22	27	–	27	mAdc	4,6,10,12	5,7,11,13	–	–	–	–	–	–	–	–	9	8	1,16
Input Current	I_{inH}	4	–	70	–	–	45	–	45	μAdc	4	5	–	–	–	–	–	–	–	–	9	8	1,16
		5	–	70	–	–	45	–	45	μAdc	5	4	–	–	–	–	–	–	–	–	9	8	1,16
Reverse Leakage Current	I_{CBO}	4	–	1.5	1.0	–	–	–	1.0	μAdc	–	–	–	–	–	–	–	–	–	–	9	4,8	1,16
Logic "1" Output Voltage	V_{OH}	2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	5	4	–	–	–	–	–	–	–	–	–	8	1,9,16
		2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	–	–	–	–	5	4	–	–	–	–	9	8	1,16
Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	4	5	–	–	–	–	–	–	–	–	–	8	1,9,16
		2	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	–	–	–	–	4	5	–	–	–	–	9	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	2	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	5	4	–	–	–	–	–	–	–	8	1,9,16
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	4	5	–	–	–	–	–	–	–	8	1,9,16
Common Mode Rejection Test	V_{OH}	2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	–	–	–	–	–	–	5	4	–	–	–	8	1,9,16
		2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	–	–	–	–	–	–	–	–	5	4	–	8	1,9,16
	V_{OL}	2	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	–	–	–	–	–	–	4	5	–	–	–	8	1,9,16
		2	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	–	–	–	–	–	–	–	–	4	5	–	8	1,9,16
Switching Times (50 ohm load)													Pulse In	Pulse Out							+3.25 V	-3.2 V	+2.0 V
Propagation Delay	t_{4-2+}	2	1.0	3.9	1.0	2.5	3.7	1.0	4.1	ns	–	–	4	2	–	–	–	–	–	–	9	8	1,5,6,11,12
	t_{4+2-}	2	1.0	3.9	1.0	2.5	3.7	1.0	4.1	ns	–	–	4	2	–	–	–	–	–	–	9	8	1,5,6,11,12
Rise Time (20% to 80%)	t_{2+}	2	1.1	4.5	1.5	2.0	4.3	1.1	4.7	ns	–	–	4	2	–	–	–	–	–	–	9	8	1,5,6,11,12
Fall Time (20% to 80%)	t_{2-}	2	1.1	4.5	1.5	2.0	4.3	1.1	4.7	ns	–	–	4	2	–	–	–	–	–	–	9	8	1,5,6,11,12

*V_{SS} = IBM Supply Voltage.
V_{IHM} = Input Logic "1" for IBM levels.
V_{ILM} = Input Logic "0" for IBM levels.
V_{IHH} = Input logic "1" level shifted positive for common mode rejection tests.
V_{ILH} = Input logic "0" level shifted positive for common mode rejection tests.
V_{IHL} = Input logic "1" level shifted negative for common mode rejection tests.
V_{ILL} = Input logic "0" level shifted negative for common mode rejection tests.

3

SWITCHING TIME TEST CIRCUIT



MOTOROLA

MC10191

MECL 10K SERIES

HEX MECL 10,000 TO MST TRANSLATOR

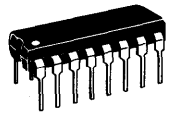
HEX MECL 10,000 TO MST TRANSLATOR

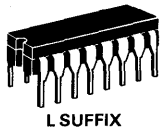
The MC10191 is a hex MECL to IBM MST type logic translator. A common enable (active low) is provided for gating. Open emitter outputs are provided for gating. Open emitter outputs are provided to permit direct transmission line driving.

The MC10191 is useful for interfacing to both MST-II and MST-IV systems.

P_D = 170 mW typ/pkg (No Load)
t_{pd} = 2.2 ns typ Input to Output
= 3.3 ns typ Enable to Output

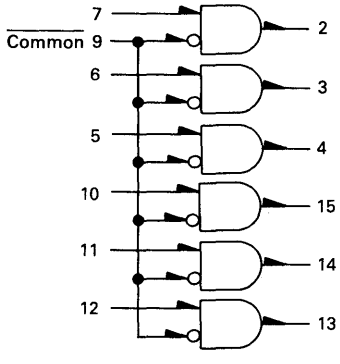
P SUFFIX
PLASTIC PACKAGE
CASE 648





L SUFFIX
CERAMIC PACKAGE
CASE 620

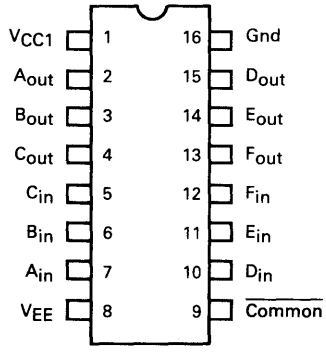
LOGIC DIAGRAM



Data	Common	Output
L	L	L
L	H	L
H	L	H
H	H	L

V_{CC1} = Pin 1 = +1.25 Vdc
V_{CC2} = Pin 16 = Gnd
V_{EE} = Pin 8 = −5.2 Vdc

PIN ASSIGNMENT



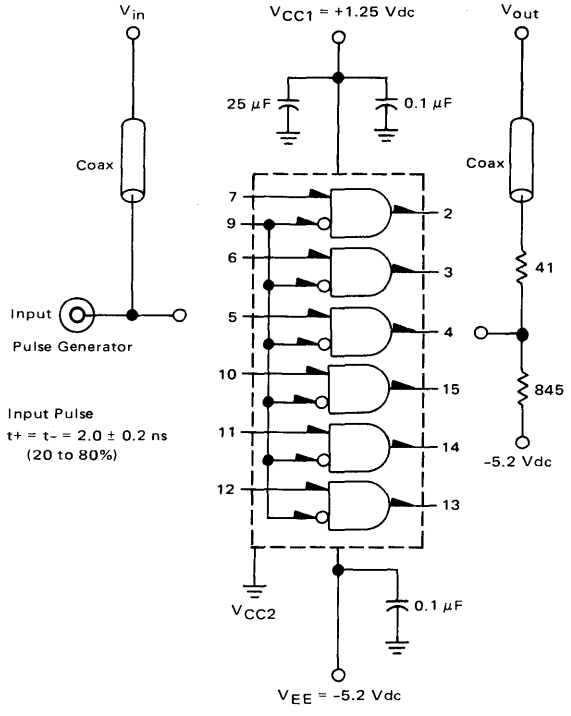
ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Test procedures are shown for only one translator. The other translators are tested in the same manner.

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	V_{CC1}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2	+1.25
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2	+1.25
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2	+1.25

Characteristic	Symbol	Pin Under Test	MC10191 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	V_{CC1}	(V_{CC2}) Gnd
Power Supply Drain Current	I_E	8	–	39	–	28	35	–	39	mAdc	9	–	–	–	8	1	16
	I_{CC}	1	–	23	–	–	23	–	23	mAdc	9	–	–	–	8	1	16
Input Current	I_{inH}	5	–	390	–	–	245	–	245	μAdc	5	–	–	–	8	1	16
		9	–	425	–	–	265	–	265	μAdc	9	–	–	–	8	1	16
	I_{inL}	7	0.5	–	0.5	–	–	0.3	–	μAdc	–	7	–	–	8	1	16
Logic "1" Output Voltage	V_{OH}	2	+0.156	+0.374	+0.255	–	+0.440	+0.327	+0.548	Vdc	7	9	–	–	8	1	16
Logic "0" Output Voltage	V_{OL}	2	-0.523	-0.323	-0.490	–	-0.290	-0.454	-0.254	Vdc	–	9	–	–	8	1	16
Logic "1" Threshold Voltage	V_{OHA}	2	+0.136	–	+0.235	–	–	+0.307	–	Vdc	–	9	7	–	8	1	16
Logic "0" Threshold Voltage	V_{OLA}	2	–	-0.303	–	–	-0.270	–	-0.234	Vdc	–	9	–	7	8	1	16
Switching Times (50 Ω Load)											**-0.890 V**	**-1.690 V**	**Pulse In**	**Pulse Out**	**-5.2 V**	**+1.25 V**	**+2.0 V**
Propagation Delay	t_{7+2+}	2	1.0	3.6	1.0	2.2	3.4	1.0	3.7	ns	5,6,10, 11,12	9	7	2	8	1	16
	t_{7-2-}	2	1.0	3.6	1.0	2.2	3.4	1.0	3.7		5,6,10, 11,12	9	7	2			
	t_{9-2+}	2	1.0	4.7	1.0	3.3	4.5	1.0	5.0		7	5,6,10, 11,12	9	2			
	t_{9+2-}	2	1.0	4.7	1.0	3.3	4.5	1.0	5.0		7	5,6,10, 11,12	9	2			
Rise Time (20% to 80%)	t_{2+}	2	1.1	4.5	1.1	2.5	4.3	1.1	4.7		5,6,10, 11,12	9	7	2			
Fall Time (20% to 80%)	t_{2-}	2	1.1	4.5	1.1	2.5	4.3	1.1	4.7		5,6,10, 11,12	9	7	2			

SWITCHING TIME TEST CIRCUIT



50-ohm termination to ground located in each scope channel input.

All input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be < 1/4 inch from TP_{in} to input pin and TP_{out} to output pin.

MOTOROLA

MC10192

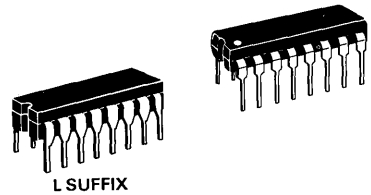
QUAD BUS DRIVER

The MC10192 contains four line drivers with complementary outputs. Each driver has a Data (D) input and shares an Enable ($\overline{E}$) input with another driver. The two driver outputs are the uncommitted collectors of a pair of NPN transistors operating as a current switch. Each driver accepts 10K MECL input signals and provides a nominal signal swing of 800 mV across a 50 Ω load at each output collector. Outputs can drive higher values of load resistance, provided that the combination of I_R drop and load return voltage V_{LR} does not cause an output collector to go more negative than −2.4 V with respect to V_{CC}. To avoid output transistor breakdown, the load return voltage should not be more positive than +5.5 V with respect to V_{CC}. When the $\overline{E}$ input is high, both output transistors of a driver are nonconducting. When not used, the $\overline{E}$ inputs, as well as the D inputs, may be left open.

- Open Collector Outputs Drive Terminated Lines or Transformers
- 50 kΩ Input Pulldown Resistors on All Inputs (Unused Inputs May Be Left Open)
- Power Dissipation = 575 mW typ/pkg (No Load)
- Propagation Delay = 3.5 ns typ ($\overline{E}$ — Output)
  3.0 ns typ (D — Output)

MECL 10K SERIES

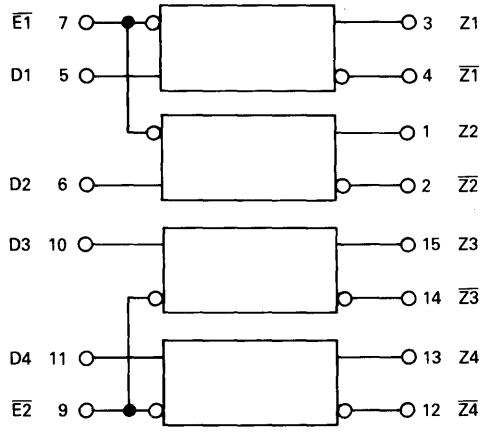
QUAD BUS DRIVER



P SUFFIX
PLASTIC PACKAGE
CASE 648

L SUFFIX
CERAMIC PACKAGE
CASE 620

LOGIC DIAGRAM



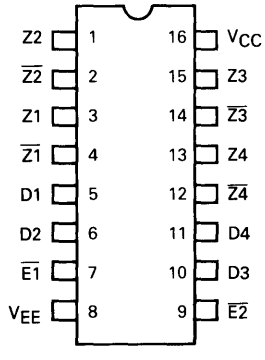
TRUTH TABLE

Inputs		Output	
$\overline{E}$	D	Z	$\overline{Z}$
H	X	H	H
L	H	H	L
L	L	L	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

V_{CC} = Pin 16
V_{EE} = Pin 8

PIN ASSIGNMENT



ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to ground volts. Test procedures are shown for one set of conditions. Complete testing according to truth table.

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
−30°C	−0.890	−1.890	−1.205	−1.500	−5.2
+25°C	−0.810	−1.850	−1.105	−1.475	−5.2
+85°C	−0.700	−1.825	−1.035	−1.440	−5.2

Characteristic	Symbol	Pin Under Test	Test Limits −30°C Min	−30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	—	154	—	140	—	154	mAdc	—	—	—	—	8	16
Input Current	I_{inH}	5	—	350	—	220	—	220	µAdc	5	—	—	—	8	16
	I_{inL}	5	0.5	—	0.5	—	0.3	—	µAdc	—	5	—	—	8	16
Logic "1" Output Current High	I_{OH}	2	—	—	—	2.0	—	—	mAdc	—	5,6,10,11	—	—	8	16
Logic "0" Output Current Low	I_{OL}	2	13.5	+18	14	18	14	19	mAdc	5,6,10,11	—	—	—	8	16
Logic "1" Output Current High	I_{OHC}	2	—	2.0	—	2.0	—	2.0	mAdc	—	5,7,9,10,11	—	6	8	16
Logic "0" Output Current Low	I_{OLC}	2	13.5	—	14	—	14	—	mAdc	5,10,11	7,9	6	—	8	16
Logic "0" Output Sink Current Low	I_{OS}	2	13.3	—	13.9	—	13.3	—	mAdc	5,6,10,11	—	—	—	8	16
Load Return Voltage Absolute Max Rating (Note 1)	V_{LR}			5.5		5.5		5.5	Volts	—	—	—	—	8	16
Output Voltage Low (Note 2)	V_{OLS}				−2.4				Volts	—	—	—	—	8	16
Switching Times (50 Ω Load)									ns						
Propagation Delay	t_{PHL} t_{PLH}														
E to Output		—	—	—	2.0	6.0	—	—							
D to Output		—	—	—	1.5	4.5	—	—							
Rise Time, Fall Time (20% to 80%)	t_{TLH} t_{THL}	—	—	—	—	3.3	—	—							

NOTE 1 The 5.5 V value is a maximum rating, do not exceed. A 270 OHM resistor will prevent output transistor breakdown.
NOTE 2 Limitations of load resistor and load return voltage combinations. Refer to page 1 description.

MOTOROLA

MC10194

DUAL SIMULTANEOUS BUS TRANSCEIVER

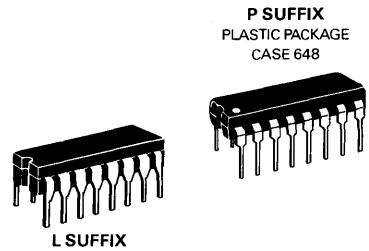
The MC10194 is a dual line driver/receiver which is capable of transmitting and receiving full duplex digital signals on a high speed bus line. Because of the current source line driver, two independent messages may be transmitted on one line at the same time.

The MC10194 is designed to work with a wide range of line impedances by connecting a resistor equal to one half the line impedance between the R_{E1} and R_{E2} inputs and V_{EE}. Each driver in the circuit will drive lines down to 75 ohms or the two drivers may be operated in parallel for lines down to 37 ohms. The data inputs and outputs on the MC10194 are fully compatible with other MECL 10,000 circuits.

P_D = 405 mW typ/pkg (No Load)
t_{pd} = 2.5 ns typ
t_r, t_f = 2.0 ns typ (20%–80%)

MECL 10K SERIES

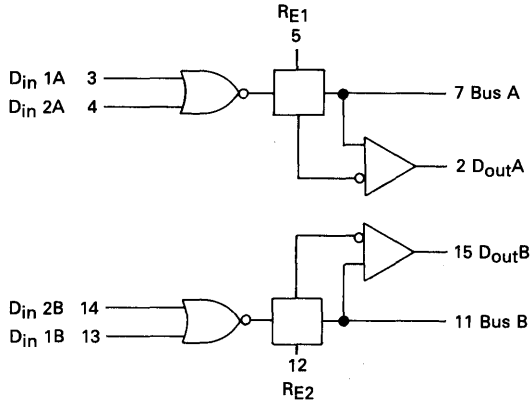
DUAL SIMULTANEOUS BUS TRANSCEIVER



P SUFFIX
PLASTIC PACKAGE
CASE 648

L SUFFIX
CERAMIC PACKAGE
CASE 620

LOGIC DIAGRAM

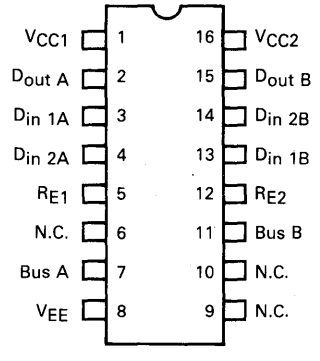


TRUTH TABLE

Inputs		Outputs	
D_{in} 1	D_{in} 2	Bus	D_{out}
L	L	V_{BusO}	H
H	L	V_{BusH}	H
L	H	V_{BusH}	H
H	H	V_{BusH}	H
L	L	V_{BusH}	L
H	L	V_{BusL}	L
L	H	V_{BusL}	L
H	H	V_{BusL}	L

V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

PIN ASSIGNMENT



ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Data outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown only for selected inputs and outputs. Other inputs and outputs are tested in a similar manner.

@ Test Temperature	TEST VOLTAGE/CURRENT VALUES (mAdc) I_{CS1}	I_{CS0A}	I_{CS1A}	(Volts) V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{CL}	V_{CH}	V_{EE}
−30°C	−21.1	6.35	14.50	−0.890	−1.890	−1.205	−1.500	−1.508	0	−5.2
+25°C	−22.6	6.80	15.27	−0.810	−1.850	−1.105	−1.475	−1.618	0	−5.2
+85°C	−24.2	7.27	16.35	−0.700	−1.825	−1.035	−1.440	−1.738	0	−5.2

Characteristic	Symbol	Pin Under Test	TEST LIMITS −30°C Min	−30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW: I_{CS1}	I_{CS0A}	I_{CS1A}	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{CL}	V_{CH}	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	107	–	78	97	–	107	mAdc	–	–	–	–	3,4,13,14	–	–	–	–	8	1,16
Input Current	I_{inH}	3	–	525	–	–	330	–	330	μAdc	–	–	–	3	–	–	–	–	–	8	1,16
		7	–	40	–	–	25	–	25	μAdc	–	–	–	–	–	–	–	–	7	8	1,16
Input Leakage Current	I_{inL}	4	–	32	0.5	–	2.0	–	20	μAdc	–	–	–	3,13,14	–	–	–	–	–	8	1,16
		7	–	32	–	–	20	–	20	μAdc	–	–	–	–	–	–	–	7	–	8	1,16
Logic "1" Output Voltage	V_{OH}	2	−1.060	−0.890	−0.960	–	−0.810	−0.890	−0.700	Vdc	–	–	–	3,4	–	–	–	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	2	−1.890	−1.675	−1.850	–	−1.650	−1.825	−1.615	Vdc	7	–	–	3,4	–	–	–	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	2	−1.080	–	−0.980	–	–	−0.910	–	Vdc	–	7	–	①	①	–	–	–	–	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	2	–	−1.655	–	–	−1.630	–	−1.595	Vdc	–	–	7	①	①	–	–	–	–	8	1,16
Bus Driver Zero Voltage Level	V_{Bus0}	7	−10	+10	−10	–	+10	−10	+10	mVdc	–	–	–	–	–	–	–	–	–	8	1,16
Bus Driver High Voltage Level	V_{BusH}	7	−0.915	−0.715	−0.970	–	−0.770	−1.030	−0.830	Vdc	–	–	–	3,4	–	–	–	–	–	8	1,16
Bus Driver Low Voltage Level	V_{BusL}	7	−1.708	−1.508	−1.818	–	−1.618	−1.938	−1.738	Vdc	7	–	–	3,4	–	–	–	–	–	8	1,16
Bus Driver Zero Threshold Voltage Level	V_{Bus0A}	7	−30	–	−30	–	–	−30	–	mVdc	–	–	–	–	–	–	3,4	–	–	8	1,16
Bus Driver High Threshold Voltage Level	V_{BusHA+} ②	7	−0.935	−0.695	−0.990	–	−0.750	−1.050	−0.810	Vdc	–	–	–	–	–	3,4	–	–	–	8	1,16
Bus Driver High Threshold Voltage Level	V_{BusHA-} ③	7	−0.935	−0.695	−0.990	–	−0.750	−1.050	−0.810	Vdc	7	–	–	–	–	–	3,4	–	–	8	1,16
Bus Driver Low Threshold Voltage Level	V_{BusLA}	7	–	−1.488	–	–	−1.598	–	−1.718	Vdc	7	–	–	–	–	3,4	–	–	–	8	1,16
															R_{E1}*	R_{E2}*	+0.31Vdc	Pulse In	Pulse Out	-3.2 V	+2.0 V
Switching Times (50-ohm load) Propagation Delay	t_{3-7+}	7	1.0	3.1	1.0	1.5	2.9	1.0	3.2	ns	–	–	–	–	5	7	4	3	7	8	1,16
	t_{3+7-}	7	↓	3.1	↓	1.5	2.9	1.0	3.2	↓	–	–	–	–	↓	↓	4	3	7	↓	↓
	t_{7-2-}	2		4.5		2.5	4.3	1.0	4.7		–	–	–	–			3,4	7	2		
	t_{7+2+}	2		4.5		2.5	4.3	1.0	4.7		–	–	–	–			3,4	7	2		
Rise Time (20% to 80%)	t_{2+}	2	1.1	4.4	1.1	2.0	4.2	1.1	4.6	ns	–	–	–	–	5	7	4	7	2	8	1,16
Fall Time (20% to 80%)	t_{2-}	2	1.1	3.5	1.1	2.0	3.3	1.1	3.6	ns	–	–	–	–	5	7	4	7	2	8	1,16

① V_{OHA} and V_{OLA} threshold test limits remain the same with V_{IHmax} or V_{ILmin} applied.

② V_{BusHA+} denotes the upper output threshold level with V_{IHAmin} applied and the external current source, I_{CS} off.

③ V_{BusHA-} denotes the lower output threshold level with V_{ILAmax} applied and the external current source, I_{CS} on.

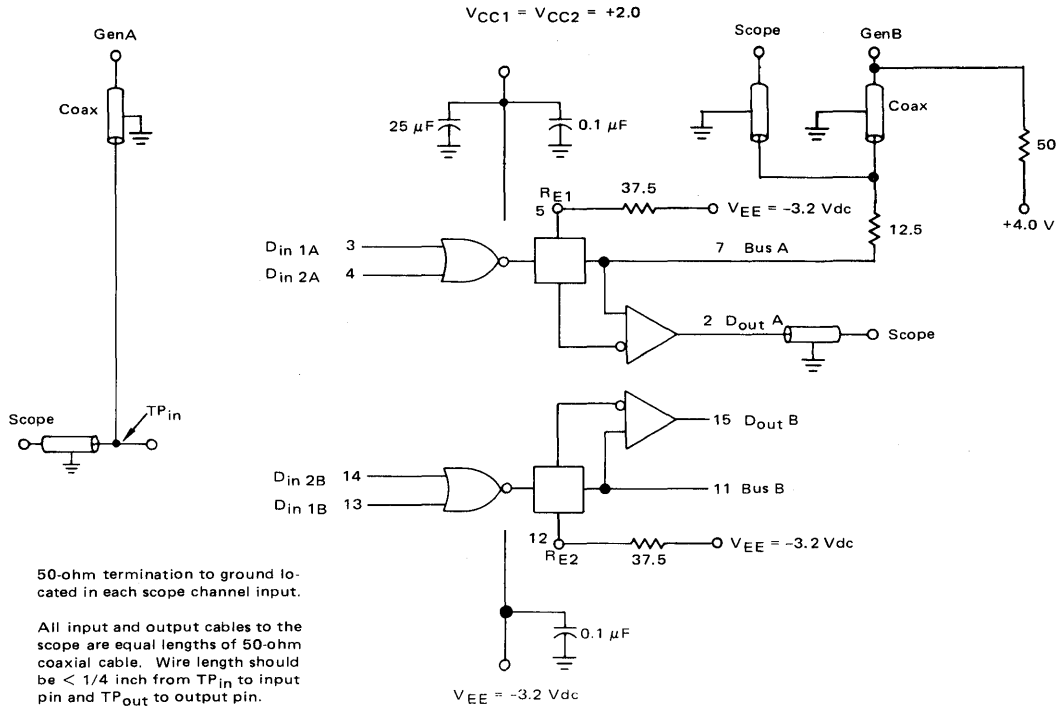
*R_{E1} = 37.5 ohms connected to V_{EE}, R_{E2} = 37.5 ohms connected to V_{CC}.

Definitions

V_{CL} = Low bias voltage for testing bus driver input loading
V_{CH} = High bias voltage for testing bus driver input loading
I_{CS1} = External current source input to the bus driver
I_{CS1A} = Upper threshold level of external current source input to the bus driver
I_{CS0A} = Lower threshold level of external current source input to the bus driver

3

SWITCHING TIME TEST CIRCUIT

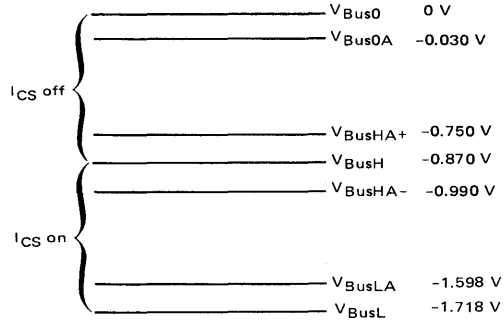


50-ohm termination to ground located in each scope channel input.

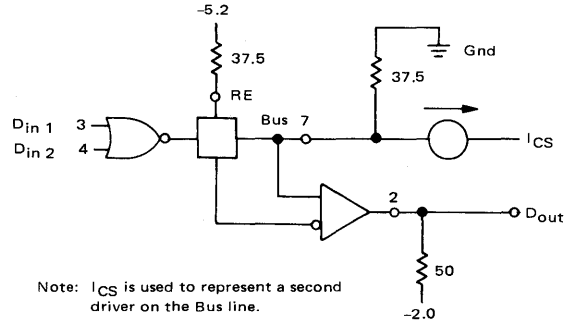
All input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be < 1/4 inch from TP_{in} to input pin and TP_{out} to output pin.

DC LOGIC LEVEL DESCRIPTION

The bus terminal (pin 7) can be at any one of three possible levels V_{BusO}, V_{BusH}, or V_{BusL} depending upon the combination of inputs applied. The MECL inputs (pins 3 and 4) cause the bus terminal to switch between two levels, V_{BusO} and V_{BusH} when the external current source (I_{CS}) is off, and V_{BusH} and V_{BusL} when the external current source is on. The bus ouput threshold voltage levels caused by applying input threshold voltages V_{ILA} and V_{IHA} at pins 3 and 4, are also translated depending upon the state of I_{CS}. These threshold levels are V_{BusOA} and V_{BusHA+} when I_{CS} is off, and V_{BusHA-} and V_{BusLA} when I_{CS} is on. These relative voltage levels are shown in the figure on the right.



DC TEST CONFIGURATION



Note: I_{CS} is used to represent a second driver on the Bus line.

APPLICATIONS INFORMATION

The MC10194 Dual Simultaneous Bus Driver/Receiver is designed for high speed data transfer over multi-port bus lines. Full duplex data transmission can improve system performance by increasing message density and overcoming the requirement to wait two line propagation delay times between messages.

Figure 1 illustrates system uses for the MC10194. One mode of operation is with two drivers on the bus line at locations X and Z. Any input to D_{in} X is seen at D_{out} Z one line propagation delay later. Similarly, any input to D_{in} Z is transmitted to D_{out} X. Each driver inhibits the data being sent on the bus from appearing at its receiver output, so full duplex signal transmission is possible. In addition, current source drivers allow two messages to pass on the same line so there are no timing restrictions between sending messages.

A second type of system operation is with a multi-terminal bus as illustrated in Figure 1 by points X, Y, and Z. In this mode, any one terminal can transmit data and all other points will receive the message. Alternately, any two terminals can simultaneously exchange data, but the other receivers will not see valid data.

The MC10194 uses current source line driving and is designed to operate with a load to V_{CC} (normally ground). This load is usually the line termination resistors at each end of the line as shown in Figure 2. In addition, to match the driver to a given impedance line, an external resistor equal to one-half the line termination resistor value is connected between the R_E output and V_{EE}. When the circuit is used with a multi-terminal bus, each driver must have the resistor between R_E and V_{EE}, but the termination resistors are required only at each end of the bus line.

Each MC10194 driver in a package is capable of driving 75-ohm lines. Higher impedance lines may be used with no loss of performance if the line is properly matched with R_E. If it is desirable to drive 50-ohm lines, both drivers in a package should be operated in parallel with each having 50-ohm resistors at R_E and the driver outputs both connected to the 50-ohm bus line.

To allow very high data rates, the rise and fall times on the bus line are quite fast (typically 1.0 ns). With full duplex operation, it is possible to get a crosstalk pulse of several hundred mV at a receiver output. A 10-20 pF capacitor connected between each driver output and V_{EE} will slow down the rise and fall times, greatly reduce any crosstalk pulse, and still give good system performance.

The adjustable current source drive feature of the MC10194 makes this circuit a useful output driver for many applications. For example, it is possible to drive the 50-ohm to ground load required by many interface systems. This driver will sink the 14 to 18 mA required to meet the AEC Committee specification for Nuclear Instrument Modules. The MC10114 MECL Line Receiver makes a good interface receiver for the MC10194 driver in these applications.

FIGURE 1 – MC10194 SYSTEM OPERATION

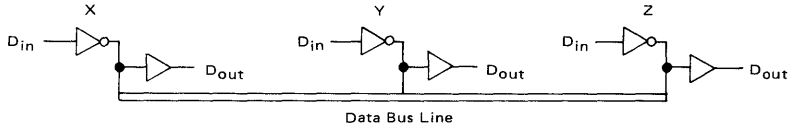
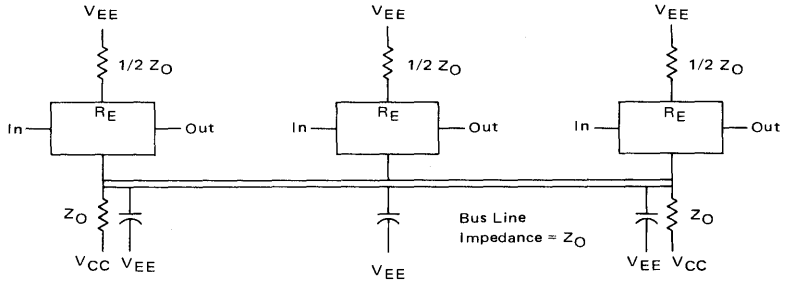


FIGURE 2 – BUS LINE INTERFACE



MOTOROLA

MC10195

MECL 10K SERIES

HEX INVERTER/BUFFER

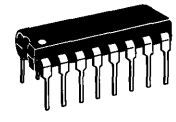
3

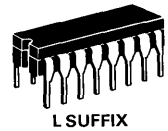
HEX INVERTER/BUFFER

The MC10195 is a Hex Buffer Inverter which is built using six EXCLUSIVE NOR gates. There is a common input to these gates which when placed low or left open allows them to act as inverters. With the common input connected to a high logic level the MC10195 is a hex buffer, useful for high fanout clock driving and reducing stub lengths on long bus lines.

P_D = 200 mW typ/pkg (No Load)
t_{pd} = 2.8 ns typ (B–Q)
t_{pd} = 3.8 ns typ (A–Q)
t_r, t_f = 2.5 ns typ (20%–80%)

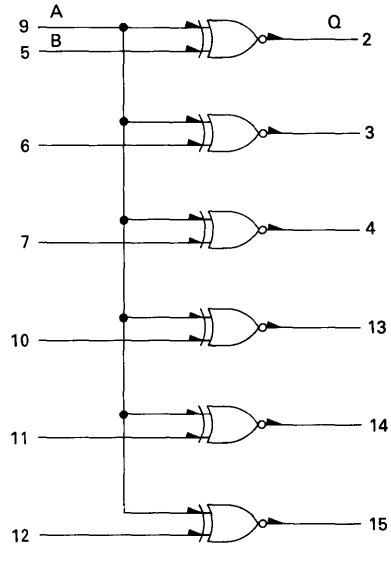
P SUFFIX
PLASTIC PACKAGE
CASE 648





L SUFFIX
CERAMIC PACKAGE
CASE 620

LOGIC DIAGRAM

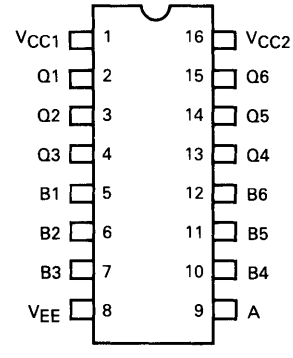


V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

TRUTH TABLE

Inputs		Output
A	B	Q
L	L	H
L	H	L
H	L	L
H	H	H

PIN ASSIGNMENT



ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown for only selected inputs and outputs. Other inputs and outputs tested in the same manner.

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10195 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	54	–	39	49	–	54	mAdc	–	–	–	–	8	1,16
Input Current	I_{inH}	5	–	425	–	–	265	–	265	μAdc	5	–	–	–	8	1,16
		9	–	460	–	–	290	–	290	μAdc	9	–	–	–	8	1,16
	I_{inL}	5	–	–	0.5	–	–	–	–	μAdc	–	5	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	–	–	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	9	–	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	2	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	–	5	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	5	–	8	1,16
Switching Time (50 ohm load)													Pulse In	Pulse Out	-3.2 Vdc	+2.0 Vdc
Propagation Delay	t_{5+2-}	2	1.1	4.2	1.1	2.8	4.0	1.1	4.4	ns	–	–	5	2	8	1,16
	t_{7-4+}	4									–	–	7	4		
	t_{10+13+}	13									–	–	10	13		
	t_{11-14-}	14									–	–	11	14		
	t_{9-14-}	14	1.1	5.2	1.1	3.8	5.0	1.1	5.4				9	14		
Rise Time (20% to 80%)	t_{2+}	2	1.1	4.7	1.1	2.5	4.5	1.1	5.0		–	–	5	2		
Fall Time (20% to 80%)	t_{2-}	2	1.1	4.7	1.1	2.5	4.5	1.1	5.0		–	–	5	2		

MOTOROLA

MC10197

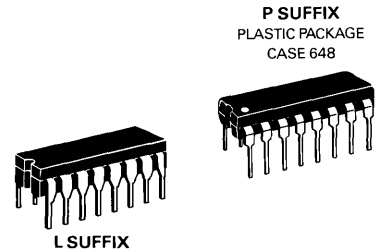
MECL 10K SERIES

HEX "AND" GATE

The MC10197 provides a high speed hex AND function with strobe capability.

P_D = 200 mW typ/pkg (No Load)
t_{pd} = 2.8 ns typ (B–Q)
t_{pd} = 3.8 ns typ (A–Q)
t_r, t_f = 2.5 ns typ (20%–80%)

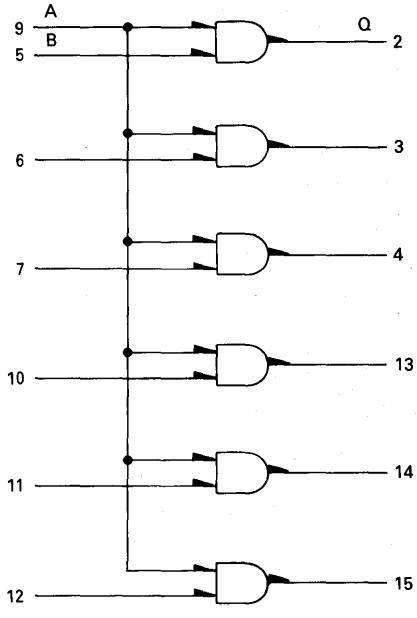
HEX "AND" GATE



P SUFFIX
PLASTIC PACKAGE
CASE 648

L SUFFIX
CERAMIC PACKAGE
CASE 620

LOGIC DIAGRAM

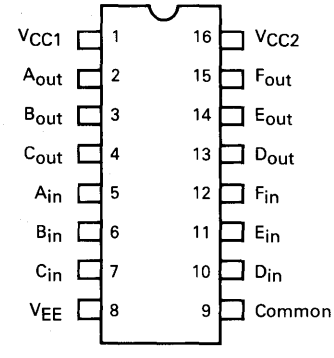


V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

TRUTH TABLE

Inputs		Output
A	B	Q
L	L	L
L	H	L
H	L	L
H	H	H

PIN ASSIGNMENT



ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown for only selected inputs and outputs. Other inputs and outputs tested in the same manner.

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
−30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10197 Test Limits −30°C Min	−30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	54	–	39	49	–	54	mAdc	–	–	–	–	8	1,16
Input Current	I_{inH}	5	–	425	–	–	265	–	265	µAdc	5	–	–	–	8	1,16
		9	–	460	–	–	290	–	290	µAdc	9	–	–	–	8	1,16
	I_{inL}	5	0.5	–	0.5	–	0.3	–	–	µAdc	–	5	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	5,9	–	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	–	–	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	2	-1.080	–	-0.980	–	–	-0.910	–	Vdc	9	–	5	–	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.655	–	–	-1.630	–	-1.595	Vdc	9	–	–	5	8	1,16
Switching Time (50 ohm load)												+1.11Vdc	Pulse In	Pulse Out	-3.2 Vdc	+2.0 Vdc
Propagation Delay	t_{5+2+}	2	1.1	4.2	1.1	2.8	4.0	1.1	4.4	ns	–	9	5	2	8	1,16
	t_{9+2+}	2	1.1	5.3	1.1	3.5	5.0	1.1	5.5		–	5	9			
Rise Time (20% to 80%)	t_{2+}	2	1.1	4.7	1.1	2.5	4.5	1.1	5.0		–	9	5			
Fall Time (20% to 80%)	t_{2-}	2	1.1	4.7	1.1	2.5	4.5	1.1	5.0		–	9	5			

MOTOROLA

MC10198

MONOSTABLE MULTIVIBRATOR

The MC10198 is a retriggerable monostable multivibrator. Two enable inputs permit triggering on any combination of positive or negative edges as shown in the accompanying table. The trigger input is buffered by Schmitt triggers making it insensitive to input rise and fall times.

The pulse width is controlled by an external capacitor and resistor. The resistor sets a current which is the linear discharge rate of the capacitor. Also, the pulse width can be controlled by an external current source or voltage (see applications information).

For high-speed response with minimum delay, a hi-speed input is also provided. This input bypasses the internal Schmitt triggers and the output responds within 2 nanoseconds typically.

Output logic and threshold levels are standard MECL 10,000. Test conditions are per Table 2. Each "Precondition" referred to in Table 2 is per the sequence of Table 1.

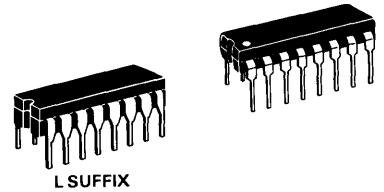
P_D = 415 mW typ/pkg (No Load)
t_{pd} = 4.0 ns typ Trigger Input to Q
2.0 ns typ Hi-Speed Input to Q

Min Timing Pulse Width	PW_{Qmin}	10 ns typ[1]
Max Timing Pulse Width	PW_{Qmax}	>10 ns typ[2]
Min Trigger Pulse Width	PW_T	2.0 ns typ
Min Hi-Speed Trigger Pulse Width	PW_{HS}	3.0 ns typ
Enable Setup Time	t_{set}	1.0 ns typ
Enable Hold Time	t_{hold}	1.0 ns typ

[1] C_{Ext} = 0 (Pin 4 open), R_{Ext} = 0 (Pin 6 to V_{EE})
[2] C_{Ext} = 10 μF, R_{Ext} = 2.7 kΩ

MECL 10K SERIES

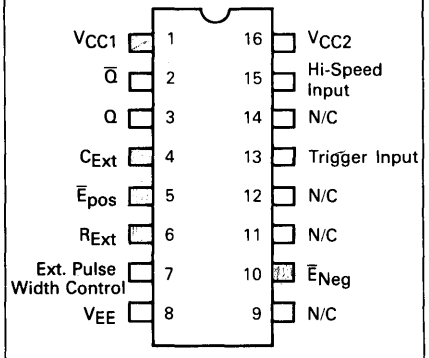
MONOSTABLE MULTIVIBRATOR



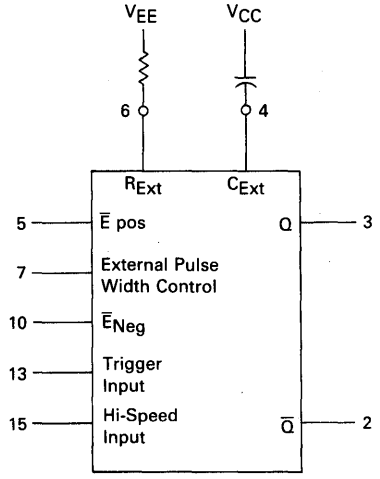
P SUFFIX
PLASTIC PACKAGE
CASE 648

L SUFFIX
CERAMIC PACKAGE
CASE 620

PIN ASSIGNMENT



LOGIC DIAGRAM

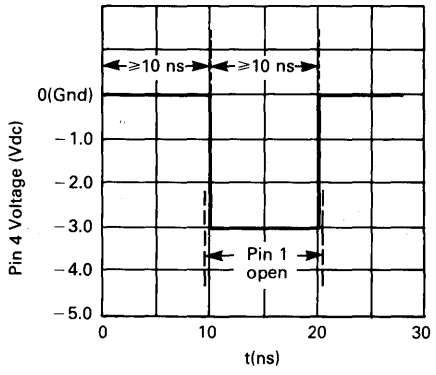


V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

TRUTH TABLE

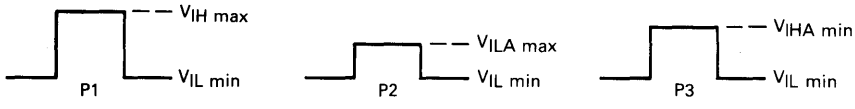
INPUT		OUTPUT
$\overline{E}_{Pos}$	$\overline{E}_{Neg}$	
L	L	Triggers on both positive & negative input slopes
L	H	Triggers on positive input slope
H	L	Triggers on negative input slope
H	H	Trigger is disabled

TABLE 1 — PRECONDITION SEQUENCE



1. At t = 0 a.) Apply V_{IHmax} to Pin 5 and 10.
   b.) Apply V_{ILmin} to Pin 15.
   c.) Ground Pin 4.
2. At t ≥10 ns a.) Open Pin 1.
   b.) Apply −3.0 Vdc to Pin 4. Hold these conditions for ≥10 ns.
3. Return Pin 4 to Ground and perform test as indicated in Table 2.

TABLE 2 — CONDITIONS FOR TESTING OUTPUT LEVELS
(See Table 1 for Precondition Sequence)



Pins 1, 16 = V_{CC} = Ground
Pins 6, 8 = V_{EE} ≈ −5.2 Vdc
Outputs loaded 50 Ω to −2.0 Vdc

Test	P.U.T.	Pin Conditions 5	10	13	15
Precondition					
V_{OH}	2			V_{IL} min	
V_{OH}	3			P1	
Precondition					
V_{OL}	3			V_{IL} min	
V_{OL}	2			P1	
Precondition					
V_{OHA}	2				V_{ILA} max
V_{OHA}	3				V_{IHA} min
Precondition					
V_{OHA}	2			V_{IL} min	
V_{OHA}	3			P3	
Precondition					
V_{OHA}	2			P2	
V_{OHA}	3			P3	
Precondition					
V_{OHA}	2		V_{IH} max	P2	
V_{OHA}	3		V_{IH} max	P3	
Precondition					
V_{OHA}	2		V_{IH} max	P1	
V_{OHA}	3		V_{IH} max	P1	

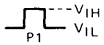
Test	P.U.T.	Pin Conditions 5	10	13	15
Precondition					
V_{OHA}	2		V_{IHA} min	P1	
V_{OHA}	3		V_{ILA} max	P1	
Precondition					
V_{OLA}	3				V_{ILA} max
V_{OLA}	2				V_{IHA} min
Precondition					
V_{OLA}	2			V_{IL} min	
V_{OLA}	3			V_{IL} min	
Precondition					
V_{OLA}	3			P2	
V_{OLA}	2			P3	
Precondition					
V_{OLA}	3		V_{IH} max	P2	
V_{OLA}	2		V_{IH} max	P3	
Precondition					
V_{OLA}	3	V_{IHA} min	V_{IH} max	P1	
V_{OLA}	2	V_{ILA} max	V_{IH} max	P1	
Precondition					
V_{OLA}	3	V_{IH} max	V_{IHA} min	P1	
V_{OLA}	2	V_{IH} max	V_{ILA} max	P1	

ELECTRICAL CHARACTERISTICS

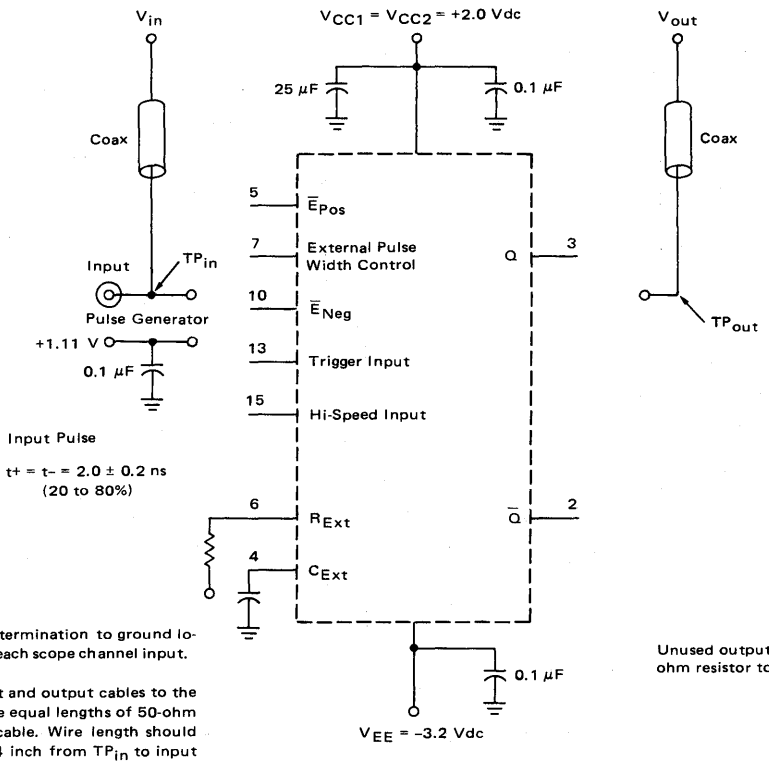
Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown for only selected inputs and outputs. Other inputs and outputs tested in the same manner.

@Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10198 TEST LIMITS -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	110	–	80	100	–	110	mAdc	–	–	–	–	6,8	1,4,16
Input Current	I_{inH}	5,10	–	415	–	–	260	–	260	µAdc	5,10	–	–	–	6,8	1,4,16
		13	–	350	–	–	220	–	220		13	–	–	–		
							390					–	–	–		
		15	–	560	–	–	350	–	350		15	–	–	–		
	I_{inL}	5	0.5	–	0.5	–	–	0.3	–	µAdc	–	5	–	–		
Logic "1" Output Voltage	V_{OH}	2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	14 ④	13	–	–	6,8	1,4,16
		3	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	13 ④	14	–	–	6,8	1,4,16
Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	13 ④	14	–	–	6,8	1,4,16
		3	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	14 ④	13	–	–	6,8	1,4,16
Logic "1" Threshold Voltage	V_{OHA}	2	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	14	–	15	6,8	1,16,4
		3	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	14	15	–	6,8	1,16,4
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	14	15	–	6,8	1,16,4
		3	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	14	–	15	6,8	1,16,4
Switching Times											1.11 Vdc		Pulse In	Pulse Out	-3.2 Vdc	+2.0 Vdc
Trigger Input	t_{T+Q+}	3	2.5	6.5	2.5	4.0	5.5	2.5	6.5	ns	10	–	13	3	6,8	1,16,4
	t_{T-Q+}	3	2.5	6.5	2.5	4.0	5.5	2.5	6.5		5	–	13	3		
Hi-Speed Trigger Input	t_{HS+Q+}	3	1.5	3.2	1.5	2.0	2.8	1.5	3.2		–	–	15	3		
Minimum Timing Pulse Width	PW_{Qmin}	3	–	–	–	10.0	–	–	–		–	–	–	②		
Maximum Timing Pulse Width	PW_{Qmax}	3	–	–	–	>10	–	–	–	ms	–	–	–	③		
Minimum Trigger Pulse Width	PW_T	3	-	–	–	2.0	–	–	–	ns	–	–	13	3		
Minimum Hi-Speed Trigger Pulse Width	PW_{HS}	3	–	–	–	3.0	–	–	–		–	–	15	3		
Rise Time (20% to 80%)		3	1.5	4.0	1.5	—	3.5	1.5	4.0							
Fall Time (20% to 80%)		3	1.5	4.0	1.5	—	3.5	1.5	4.0							
Enable Setup Time	$t_{setup(E)}$	3	–	–	–	1.0	–	–	–		–	–	5	3		
Enable Hold Time	$t_{hold(E)}$	3	–	–	–	1.0	–	–	–		–	–	5	3		

Notes: ① The monostable is in the timing mode at the time of this test.
② C_{EXT} = 0 (Pin 4 open)
R_{EXT} = 0 (Pin 6 tied to V_{EE})
③ C_{EXT} = 10 µF (Pin 4)
R_{EXT} = 2.7 k (Pin 6)
④ 

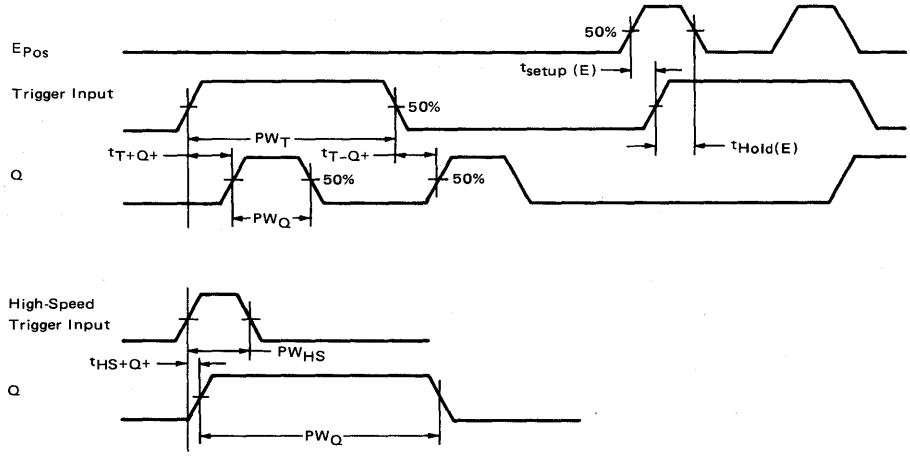
SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C



50-ohm termination to ground located in each scope channel input.

All input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be < 1/4 inch from TP_{in} to input pin and TP_{out} to output pin.

Unused outputs are tied to a 50-ohm resistor to ground.



APPLICATIONS INFORMATION

CIRCUIT OPERATION:

1. PULSE WIDTH TIMING — The pulse width is determined by the external resistor and capacitor. The MC10198 also has an internal resistor (nominally 284 ohms) that can be used in series with R_{Ext}. Pin 7, the external pulse width control, is a constant voltage node (−3.60 V nominally). A resistance connected in series from this node to V_{EE} sets a constant timing current I_T. This current determines the discharge rate of the capacitor:

$$I_T = C_{Ext} \frac{\Delta V}{\Delta T}$$

where

ΔT = pulse width
ΔV = 1.9 V change in capacitor voltage

Then:

$$\Delta T = C_{Ext} \frac{1.9\ V}{I_T}$$

If $R_{Ext} + R_{Int}$ are in series to V_{EE}:

$I_T = [(-3.60\ V) - (-5.2\ V)] \div [R_{Ext} + 284\ \Omega]$
$I_T = 1.6\ V/(R_{Ext} + 284)$

The timing equation becomes:

$\Delta T = [(C_{Ext})(1.9\ V)] \div [1.6\ V/(R_{Ext} + 284)]$
$\Delta T = C_{Ext}\ (R_{Ext} + 284)\ 1.19$

where ΔT = Sec
R_{Ext} = Ohms
C_{Ext} = Farads

FIGURE 1 —

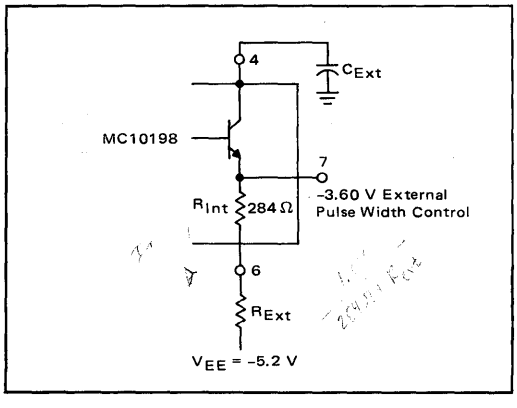


Figure 2 shows typical curves for pulse width versus C_{Ext} and R_{Ext} (total resistance includes R_{Int}). Any low leakage capacitor can be used and R_{Ext} can vary from 0 to 16 k-ohms.

2. TRIGGERING — The $\overline{E}_{Pos}$ and $\overline{E}_{Neg}$ inputs control the trigger input. The MC10198 can be programmed to trigger on the positive edge, negative edge, or both. Also, the trigger input can be totally disabled. The truth table is shown on the first page of the data sheet.

The device is totally retriggerable. However, as duty cycle approaches 100%, pulse width jitter can occur due to the recovery time of the circuit. Recovery time is basically dependent on capacitance C_{Ext}. Figure 3 shows typical recovery time versus capacitance at I_T = 5 mA.

FIGURE 2 — TIMING PULSE WIDTH versus C_{Ext} and R_{Ext}

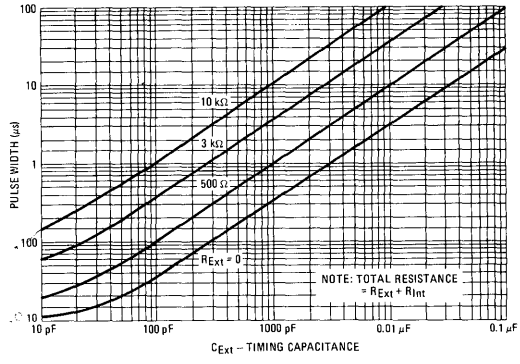
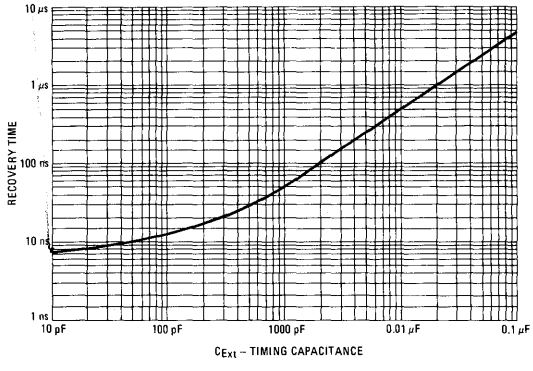


FIGURE 3 — RECOVERY TIME versus C_{Ext} @ I_T = 5 mA

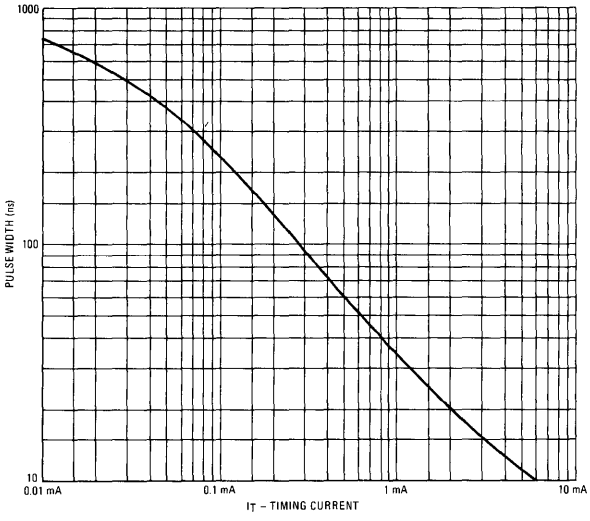


3. HI-SPEED INPUT — This input is used for stretching very narrow pulses with minimum delay between the output pulse and the trigger pulse. The trigger input should be disabled when using the high-speed input. The MC10198 triggers on the rising edge, using this input, and input pulse width should narrow, typically less than 10 nanoseconds.

USAGE RULES:

1. Capacitor lead lengths should be kept very short to minimize ringing due to fast recovery rise times.
2. The $\overline{E}$ inputs should not be tied to ground to establish a high logic level. A resistor divider or diode can be used to establish a −0.7 to −0.9 voltage level.
3. For optimum temperature stability; 0.5 mA is the best timing current I_T. The device is designed to have a constant voltage at the EXTERNAL PULSE WIDTH CONTROL over temperature at this current value.
4. Pulse Width modulation can be attained with the EXTERNAL PULSE WIDTH CONTROL. The timing current can be altered to vary the pulse width. Two schemes are:
   (a) The internal resistor is not used. A dependent current source is used to set the timing current as shown in Figure 4. A graph of pulse width versus timing current (C_{Ext} = 13 pF) is shown in Figure 5.

FIGURE 5 — PULSE WIDTH versus I_T @ C_{Ext} = 13 pF



   (b) A control voltage can also be used to vary the pulse width using an additional resistor (Figure 6). The current (I_T + I_C) is set by the voltage drop across R_{Int} + R_{Ext}. The control current IC modifies I_T and alters the pulse width. Current I_C should never force I_T to zero. R_C typically 1 kΩ.

FIGURE 4 —

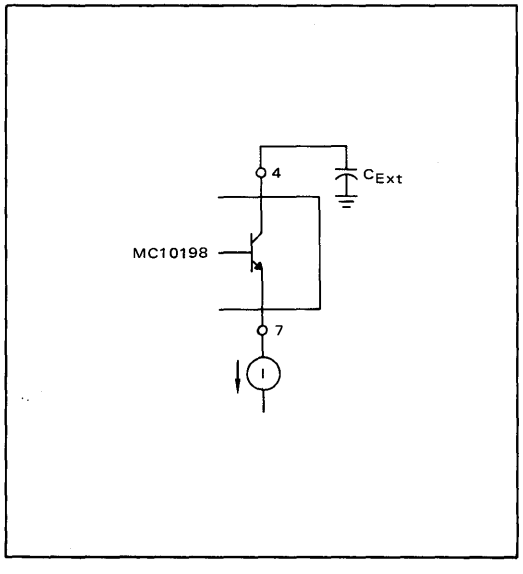
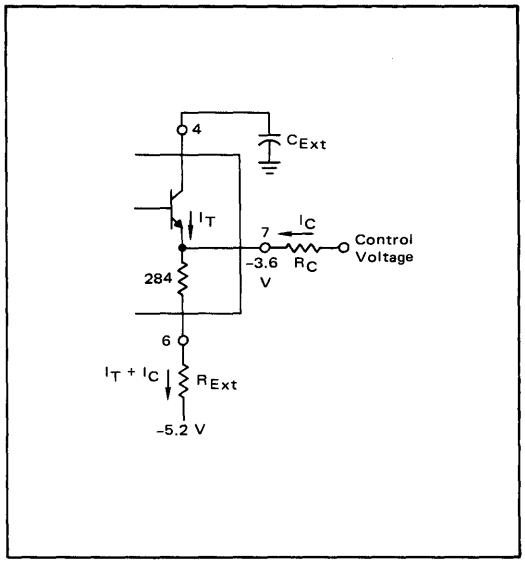
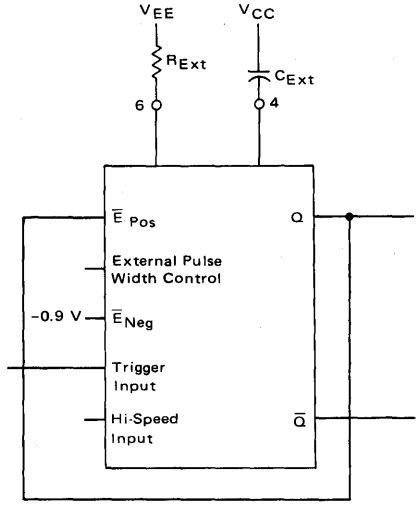


FIGURE 6 —



5. The MC10198 can be made non-retriggerable. The Q output is fed back to disable the trigger input during the triggered state (Logic Diagram). Figure 7 shows a positive triggered configuration; a similar configuration can be made for negative triggering.

FIGURE 7 —



MOTOROLA

MC10210

DUAL 3-INPUT 3-OUTPUT "OR" GATE

The MC10210 is designed to drive up to six transmission lines simultaneously. The multiple outputs of this device also allow the wire "OR" -ing of several levels of gating for minimization of gate and package count.

The ability to control three parallel lines with minimum propagation delay from a single point makes the MC10210 particularly useful in clock distribution applications where minimum clock skew is desired.

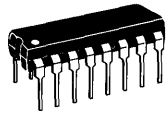
P_D = 160 mW typ/pkg (No Loads)
t_{pd} = 1.5 ns typ (All Output Loaded)
t_r, t_f = 1.5 ns typ (20%–80%)

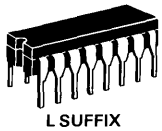
MECL 10K SERIES

DUAL 3-INPUT 3-OUTPUT "OR" GATE

3

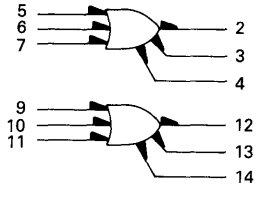
P SUFFIX
PLASTIC PACKAGE
CASE 648





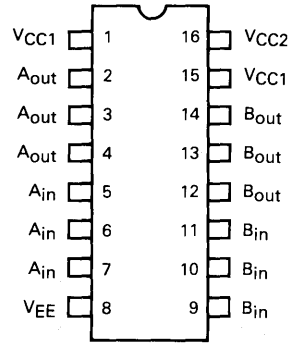
L SUFFIX
CERAMIC PACKAGE
CASE 620

LOGIC DIAGRAM



V_{CC1} = Pin 1, 15
V_{CC2} = Pin 16
V_{EE} = Pin 8

PIN ASSIGNMENT



ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown for only one gate. The other gate is tested in the same manner.

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10210 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	42	–	–	38	–	42	mAdc	–	–	–	–	8	1,15,16
Input Current	I_{inH}	5,6,7	–	650	–	–	410	–	410	μAdc	*	–	–	–	8	1,15,16
	I_{inL}	5,6,7	0.5	–	0.5	–	–	0.3	–	μAdc	–	*	–	–	8	1,15,16
Logic "1" Output Voltage	V_{OH}	2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	5	–	–	–	8	1,15,16
		3	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	6	–	–	–	8	1,15,16
		4	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	7	–	–	–	8	1,15,16
Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	–	–	–	–	8	1,15,16
		3	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	–	–	–	–	8	1,15,16
		4	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	–	–	–	–	8	1,15,16
Logic "1" Threshold Voltage	V_{OHA}	2	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	5	–	8	1,15,16
		3	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	6	–	8	1,15,16
		4	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	7	–	8	1,15,16
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	–	5	8	1,15,16
		3	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	–	6	8	1,15,16
		4	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	–	7	8	1,15,16
Switching Times (50-ohm load)													Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{5+2+}	2	1.0	2.6	1.0	1.5	2.5	1.0	2.8	ns	–	–	5	2	8	1,15,16
	t_{5-2-}	2									–	–		2		
	t_{5+3+}	3									–	–		3		
	t_{5-3-}	3									–	–		3		
	t_{5+4+}	4									–	–		4		
	t_{5-4-}	4									–	–		4		
Rise Time (20 to 80%)	t_{2+}	2									–	–		2		
	t_{3+}	3									–	–		3		
	t_{4+}	4									–	–		4		
Fall Time (20 to 80%)	t_{2-}	2									–	–		2		
	t_{3-}	3									–	–		3		
	t_{4-}	4									–	–		4		

*Individually test each input using the pin connections shown.

MOTOROLA

MC10211

MECL 10K SERIES

DUAL 3-INPUT 3-OUTPUT "NOR" GATE

The MC10211 is designed to drive up to six transmission lines simultaneously. The multiple outputs of this device also allow the wire "OR"-ing of several levels of gating for minimization of gate and package count.

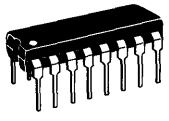
The ability to control three parallel lines with minimum propagation delay from a single point makes the MC10211 particularly useful in clock distribution applications where minimum clock skew is desired.

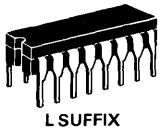
P_D = 160 mW typ/pkg (No Loads)
t_{pd} = 1.5 ns typ (All Output Loaded)
t_r, t_f = 1.5 ns typ (20%–80%)

DUAL 3-INPUT 3-OUTPUT "NOR" GATE

3

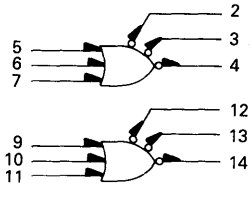
P SUFFIX
PLASTIC PACKAGE
CASE 648





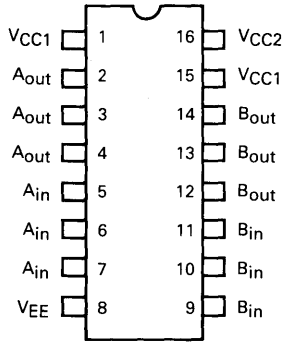
L SUFFIX
CERAMIC PACKAGE
CASE 620

LOGIC DIAGRAM



V_{CC1} = Pin 1, 15
V_{CC2} = Pin 16
V_{EE} = Pin 8

PIN ASSIGNMENT



ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown for only one gate. The other gate is tested in the same manner.

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10211 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	42	–	30	38	–	42	mAdc	–	–	–	–	8	1,15,16
Input Current	I_{inH}	5,6,7	–	650	–	–	410	–	410	μAdc	*	–	–	–	8	1,15,16
	I_{inL}	5,6,7	0.5	–	0.5	–	–	0.3	–	μAdc	–	*	–	–	8	1,15,16
Logic "1" Output Voltage	V_{OH}	2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	–	–	–	–	8	1,15,16
		3	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	–	–	–	–	8	1,15,16
		4	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	–	–	–	–	8	1,15,16
Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	5	–	–	–	8	1,15,16
		3	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	6	–	–	–	8	1,15,16
		4	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	7	–	–	–	8	1,15,16
Logic "1" Threshold Voltage	V_{OHA}	2	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	–	5	8	1,15,16
		3	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	–	6	8	1,15,16
		4	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	–	7	8	1,15,16
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	5	–	8	1,15,16
		3	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	6	–	8	1,15,16
		4	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	7	–	8	1,15,16
Switching Times (50-ohm load)													Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{5+2-}	2	1.0	2.6	1.0	1.5	2.5	1.0	2.8	ns	–	–	5	2	8	1,15,16
	t_{5-2+}	2	↓	↓	↓	↓	↓	↓	↓	↓	–	–	↓	2	↓	↓
	t_{5+3-}	3									–	–		3		
	t_{5-3+}	3									–	–		3		
	t_{5+4-}	4									–	–		4		
	t_{5-4+}	4									–	–		4		
Rise Time (20 to 80%)	t_{2+}	2									–	–		2		
	t_{3+}	3									–	–		3		
	t_{4+}	4									–	–		4		
Fall Time (20 to 80%)	t_{2-}	2									–	–		2		
	t_{3-}	3									–	–		3		
	t_{4-}	4	↓	↓	↓	↓	↓	↓	↓	↓	–	–	↓	4	↓	↓

*Individually test each input using the pin connections shown.

MOTOROLA

MC10212

MECL 10K SERIES

HIGH SPEED DUAL 3-INPUT 3-OUTPUT OR/NOR GATE

The MC10212 is designed to drive up to six transmission lines simultaneously. The multiple outputs of this device also allow the wire "OR"-ing of several levels of gating for minimization of gate and package count.

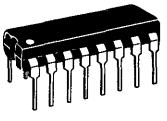
The ability to control three parallel lines with minimum propagation delay from a single point makes the MC10212 particularly useful in clock distribution applications where minimum clock skew is desired.

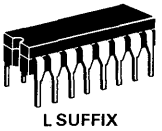
P_D = 160 mW typ/pkg (No Load)
t_{pd} = 1.5 ns typ (All Outputs Loaded)
t_r, t_f = 1.5 ns typ (20% to 80%)

HIGH SPEED DUAL 3-INPUT 3-OUTPUT OR/NOR GATE

3

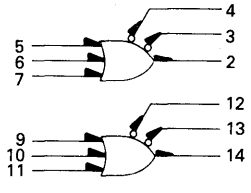
P SUFFIX
PLASTIC PACKAGE
CASE 648





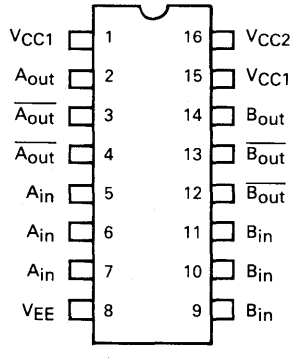
L SUFFIX
CERAMIC PACKAGE
CASE 620

LOGIC DIAGRAM



V_{CC1} = Pins 1, 15
V_{CC2} = Pin 16
V_{EE} = Pin 8

PIN ASSIGNMENT



ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specification shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown for only one gate. The other gate is tested in the same manner.

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10212 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	42	–	30	38	–	42	mAdc	–	–	–	–	8	1,15,16
Input Current	I_{inH}	5,6,7	–	650	–	–	410	–	410	μAdc	5,6,7*	–	–	–	8	1,15,16
	I_{inL}	5,6,7	0.5	–	0.5	–	–	0.3	–	μAdc	–	5,6,7*	–	–	8	1,15,16
Logic "1" Output Voltage	V_{OH}	2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	5	–	–	–	8	1,15,16
		3	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	–	–	–	–	8	1,15,16
		4	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	–	–	–	–	8	1,15,16
Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	–	–	–	–	8	1,15,16
		3	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	5	–	–	–	8	1,15,16
		4	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	5	–	–	–	8	1,15,16
Logic "1" Threshold Voltage	V_{OHA}	2	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	5	–	8	1,15,16
		3	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	–	5	8	1,15,16
		4	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	–	5	8	1,15,16
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	–	5	8	1,15,16
		3	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	5	–	8	1,15,16
		4	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	5	–	8	1,15,16
Switching Times (50-ohm load)													Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{5+2+}	2	1.0	2.6	1.0	1.5	2.5	1.0	2.8	ns	–	–	5	2	8	1,15,16
	t_{5-2-}	2									–	–		2		
	t_{5+3-}	3									–	–		3		
	t_{5-3+}	3									–	–		3		
	t_{5+4-}	4									–	–		4		
	t_{5-4+}	4									–	–		4		
Rise Time (20 to 80%)	t_{2+}	2									–	–		2		
	t_{3+}	3									–	–		3		
	t_{4+}	4									–	–		4		
Fall Time (20 to 80%)	t_{2-}	2									–	–		2		
	t_{3-}	3									–	–		3		
	t_{4-}	4									–	–		4		

*Individually test each input using the pin connections shown.

MC10216

HIGH SPEED TRIPLE LINE RECEIVER

The MC10216 is a high speed triple differential amplifier designed for use in sensing differential signals over long lines. The base bias supply (V_{BB}) is made available at pin 11 to make the device useful as a Schmitt trigger, or in other applications where a stable reference voltage is necessary.

Active current sources provide the MC10216 with excellent common mode noise rejection. If any amplifier in a package is not used, one input of that amplifier must be connected to V_{BB} (pin 11) to prevent upsetting the current source bias network.

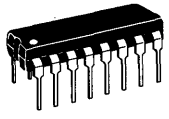
Complementary outputs are provided to allow driving twisted pair lines, to enable cascading of several amplifiers in a chain, or simply to provide complement outputs of the input logic function.

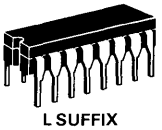
P_D = 100 mW typ/pkg (No Load)
t_{pd} = 1.8 ns typ (Single ended)
= 1.5 ns typ (Differential)
t_r, t_f = 1.5 ns typ (20%–80%)

MECL 10K SERIES

HIGH SPEED TRIPLE LINE RECEIVER

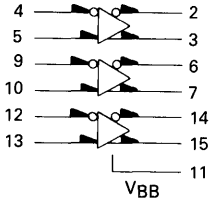
P SUFFIX
PLASTIC PACKAGE
CASE 648





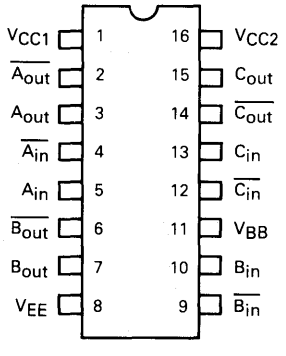
L SUFFIX
CERAMIC PACKAGE
CASE 620

LOGIC DIAGRAM



V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

PIN ASSIGNMENT



ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

@ Test Temperature	TEST VOLTAGE VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{BB}	V_{EE}
−30°C	−0.890	−1.890	−1.205	−1.500	From	−5.2
+25°C	−0.810	−1.850	−1.105	−1.475	Pin	−5.2
+85°C	−0.700	−1.825	−1.035	−1.440	11	−5.2

Characteristic	Symbol	Pin Under Test	MC10216 Test Limits −30°C Min	−30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS BELOW: $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{BB}	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	27	–	20	25	–	27	mAdc	4,9,12	–	–	–	5,10,13	8	1,16
Input Current	I_{inH}	4	–	180	–	–	115	–	115	μAdc	4	9,12	–	–	5,10,13	8	1,16
	I_{CBO}	4	–	1.5	–	–	1.0	–	1.0	μAdc	–	9,12	–	–	5,10,13	8,4	1,16
		9	–	1.5	–	–	1.0	–	1.0	μAdc	–	4,12	–	–	5,10,13	8,9	1,16
High Output Voltage	V_{OH}	2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	4	9,12	–	–	5,10,13	8	1,16
		3	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	9,12	4	–	–	5,10,13	8	1,16
Low Output Voltage	V_{OL}	2	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	9,12	4	–	–	5,10,13	8	1,16
		3	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	4	9,12	–	–	5,10,13	8	1,16
High Threshold Voltage	V_{OHA}	2	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	9,12	4	–	5,10,13	8	1,16
		3	-1.080	–	-0.980	–	–	-0.910	–	Vdc	9,12	–	–	4	5,10,13	8	1,16
Low Threshold Voltage	V_{OLA}	2	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	9,12	–	4	5,10,13	8	1,16
		3	–	-1.655	–	–	-1.630	–	-1.595	Vdc	9,12	–	4	–	5,10,13	8	1,16
Reference Voltage	V_{BB}	11	-1.420	-1.280	-1.350	–	-1.230	-1.295	-1.150	Vdc	–	–	–	–	5,10,13	8	1,16
Switching Times (50-ohm Load)													Pulse In	Pulse Out		-3.2 Vdc	+2.0 Vdc
Propagation Delay	t_{4+2+}	2	1.0	2.6	1.0	1.8*	2.5	1.0	2.8	ns	–	–	4	2	5,10,13	8	1,16
	t_{4-2-}	2									–	–		2			
	t_{4+3-}	3									–	–		3			
	t_{4-3+}	3									–	–		3			
Rise Time (20% to 80%)	t_{2+}	2				1.5					–	–		2			
	t_{3+}	3									–	–		3			
Fall Time (20% to 80%)	t_{2-}	2									–	–		2			
	t_{3-}	3									–	–		3			

*Delay is 1.5 ns when inputs are driven differentially
Delay is 1.8 ns when inputs are driven single ended

MOTOROLA

MC10231

HIGH SPEED DUAL TYPE D MASTER-SLAVE FLIP-FLOP

The MC10231 is a dual master-slave type D flip-flop. Asynchronous Set (S) and Reset (R) override Clock (C_C) and Clock Enable ($\overline{C_E}$) inputs. Each flip-flop may be clocked separately by holding the common clock in the low state and using the enable inputs for the clocking function. If the common clock is to be used to clock the flip-flop, the Clock Enable inputs must be in the low state. In this case, the enable inputs perform the function of controlling the common clock.

The output states of the flip-flop change on the positive transition of the clock. A change in the information present at the data (D) input will not affect the output information at any other time due to master-slave construction.

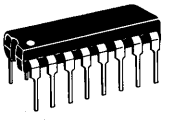
P_D = 270 mW typ/pkg (No Load)
t_{pd} = 2 ns typ
t_{Tog} = 225 MHz typ
t_r, t_f = 2.0 ns typ (20%–80%)

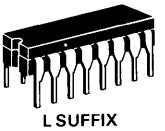
MECL 10K SERIES

HIGH SPEED DUAL TYPE D MASTER-SLAVE FLIP-FLOP

3

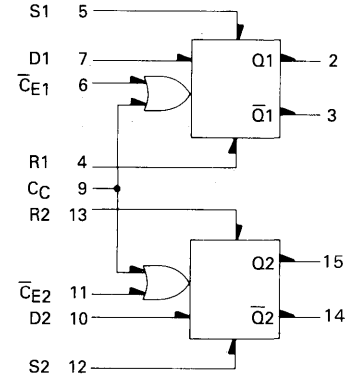
P SUFFIX
PLASTIC PACKAGE
CASE 648





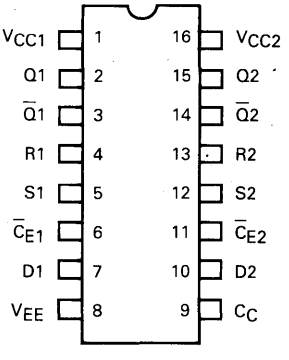
L SUFFIX
CERAMIC PACKAGE
CASE 620

LOGIC DIAGRAM



V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

PIN ASSIGNMENT



CLOCK TRUTH TABLE

C	D	Q_{n+1}
L	ϕ	Q_n
H	L	L
H	H	H

ϕ = Don't Care
C = $\overline{C}_E$ + C_C.
A clock H is a clock transition from a low to a high state.

R-S TRUTH TABLE

R	S	Q_{n+1}
L	L	Q_n
L	H	H
H	L	L
H	H	N.D.

N.D. = Not Defined

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table after the thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown for only one input, or for one set of input conditions. Other inputs tested in the same manner.

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
−30°C	−0.890	−1.890	−1.205	−1.500	−5.2
+25°C	−0.810	−1.850	−1.105	−1.475	−5.2
+85°C	−0.700	−1.825	−1.035	−1.440	−5.2

Characteristic	Symbol	Pin Under Test	MC10231 Test Limits −30°C Min	−30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	72	–	52	65	–	72	mAdc	–	–	–	–	8	1, 16
Input Current	I_{inH}	4	–	650	–	–	410	–	410	µAdc	4	–	–	–	8	1, 16
		5	–	650	–	–	410	–	410		5	–	–	–		
		6	–	350	–	–	220	–	220		6	–	–	–		
		7	–	350	–	–	220	–	220		7	–	–	–		
		9	–	460	–	–	290	–	290		9	–	–	–		
Input Leakage Current	I_{inL}	4,5,*	–	–	0.5	–	–	–	–	µAdc	–	*	–	–	8	1, 16
		6,7,9*	–	–	0.5	–	–	–	–	µAdc	–	*	–	–	8	1, 16
Logic "1" Output Voltage	V_{OH}	2	−1.060	−0.890	−0.960	–	−0.810	−0.890	−0.700	Vdc	5	–	–	–	8	1, 16
		2†	−1.060	−0.890	−0.960	–	−0.810	−0.890	−0.700	Vdc	7	–	–	–	8	1, 16
Logic "0" Output Voltage	V_{OL}	3	−1.890	−1.675	−1.850	–	−1.650	−1.825	−1.615	Vdc	5	–	–	–	8	1, 16
		3†	−1.890	−1.675	−1.850	–	−1.650	−1.825	−1.615	Vdc	7	–	–	–	8	1, 16
Logic "1" Threshold Voltage	V_{OHA}	2	−1.080	–	−0.980	–	–	−0.910	–	Vdc	–	–	5	–	8	1, 16
		2†	−1.080	–	−0.980	–	–	−0.910	–	Vdc	–	–	7	9	8	1, 16
Logic "0" Threshold Voltage	V_{OLA}	3	–	−1.655	–	–	−1.630	–	−1.595	Vdc	–	–	5	–	8	1, 16
		3†	–	−1.655	–	–	−1.630	–	−1.595	Vdc	–	–	7	9	8	1, 16
Switching Times Clock Input											+1.11 Vdc		Pulse In	Pulse Out	−3.2 Vdc	+2.0 Vdc
Propagation Delay	t_{9+2-}	2	1.5	3.4	1.5	2.0	3.3	1.6	3.7	ns	–	–	9	2	8	1, 16
	t_{6+2+}	2	1.5	3.4	1.5	2.0	3.3	1.6	3.7		7	–	6	2		
Rise Time (20 to 80%)	t_{2+}	2	0.9	3.3	1.0	1.3	3.1	1.0	3.6		7	–	9	2		
Fall Time (20 to 80%)	t_{2-}	2	0.9	3.3	1.0	1.3	3.1	1.0	3.6		–	–	9	2		
Set Input Propagation Delay	t_{5+2+}	2	1.1	3.4	1.1	2.0	3.3	1.2	3.7	ns	–	–	5	2	8	1, 16
	t_{12+15+}	15									6	–	12	15		
	t_{5+3+}	3									–	–	5	3		
	t_{12+14-}	14									9	–	12	14		
Reset Input Propagation Delay	t_{4+2-}	2	1.1	3.4	1.1	2.0	3.3	1.2	3.7	ns	–	–	4	2	8	1, 16
	t_{13+15-}	15									6	–	13	15		
	t_{4+3-}	3									–	–	4	3		
	t_{13+14+}	14									9	–	13	14		
Setup Time	t_{Setup}	7	1.5	–	1.0	–	–	1.5	–	ns	–	–	6,7	2	8	1, 16
Hold Time	t_{Hold}	7	0.9	–	0.75	–	–	0.9	–	ns	–	–	6,7	2	8	1, 16
Toggle Frequency (Max)	f_{Tog}	2	200	–	200	225	–	200	–	MHz	*	–	6	2	8	1, 16

*Individually test each input; apply $V_{IL\ min}$ to pin under test.

†Output level to be measured after a clock pulse has been applied to the $\overline{C}_E$ input (pin 6) 

MOTOROLA

MC10287

HIGH SPEED 2 x 1 BIT ARRAY MULTIPLIER BLOCK

The MC10287 is a dual high speed iterative multiplier. It is designed for use as an array multiplier block. Each device is a modified full adder/subtractor that forms a single-bit binary product at each operand input of the adder. Internal carry lookahead is employed for high speed operation.

An addition or subtraction is selected by mode controls (M0, M1). The mode controls are buffered such that they can be grounded or taken to a standard high logic level to accomplish subtraction. When left open or taken to a low logic level, M0 and M1 cause addition.

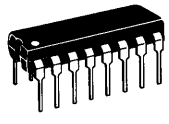
P_D = 400 mW typ/pkg (No Load)
t_{pd}: (Outputs loaded 1 kΩ to V_{EE})
C0 to C2 = 1.7 ns typ
a0 to C2 = 2.8
a0 to S0 = 2.7
b0 to S0 = 3.1
a0 to S1 = 3.9
b0 to S1 = 4.4
M0 to S1 = 8.7

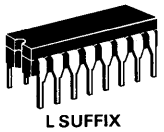
MECL 10K SERIES

HIGH SPEED 2 x 1 BIT ARRAY MULTIPLIER BLOCK

3

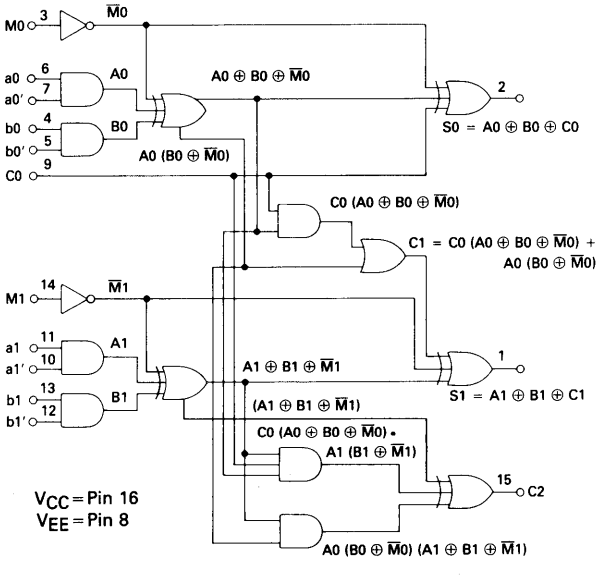
P SUFFIX
PLASTIC PACKAGE
CASE 648



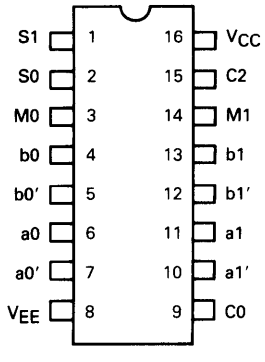


L SUFFIX
CERAMIC PACKAGE
CASE 620

LOGIC DIAGRAM



PIN ASSIGNMENT



ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown for only selected inputs and outputs. Other inputs and outputs tested in the same manner.

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10287 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	106	–	77	96	–	106	mAdc	–	–	–	–	8	16
Input Current	I_{inH}	3	–	320	–	–	200	–	200	μAdc	3	–	–	–	8	16
		4	–	350	–	–	220	–	220		4	–	–	–		
		6	–	425	–	–	265	–	265		6	–	–	–		
		9	–	650	–	–	410	–	410		9	–	–	–		
	I_{inL}	3	0.5	–	0.5	–	–	0.3	–	μAdc	–	3	–	–	8	16
Logic "1" Output Voltage	V_{OH}	1	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	5,9	–	–	–	8	16
		2				–					9	–	–	–		
		15				–					6,9,10	–	–	–		
Logic "0" Output Voltage	V_{OL}	1	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	–	–	–	–	8	16
		2				–					–	–	–	–		
		15				–					–	–	–	–		
Logic "1" Threshold Voltage	V_{OHA}	1	-1.080	–	-0.980	–	–	-0.910	–	Vdc	6,7	–	9	–	8	16
		2		–		–	–		–		–	–	4	–		
		15		–		–	–		–		6,7,10,11	–	9	–		
Logic "0" Threshold Voltage	V_{OLA}	1	–	-1.655	–	–	-1.630	–	-1.595	Vdc	6,7	–	–	9	8	16
		2	–		–	–		–			–	–	–	4		
		15	–		–	–		–			6,7,10,11	–	–	9		
Switching Times											+1.11 V	+0.31 V	Pulse In	Pulse Out	-3.2 Vdc	+2.0 Vdc
Propagation Delay (50 ohm load)	t_{9+15+}	15	1.1	3.6	1.1	2.0	3.4	1.1	3.7	ns	3	*	9	15	8	16
	t_{6-1-}	1	1.4	6.1	1.4	4.5	5.8	1.4	6.4		3		6	1		
	t_{4+2-}	2	1.1	4.9	1.1	3.5	4.7	1.1	5.2		6		4	2		
	t_{4-1+}	1	1.1	4.7	1.1	4.5	4.5	1.1	4.8		6		4	1		
	t_{11+1-}	1	1.1	4.7	1.1	3.0	4.5	1.1	4.8		13		11	1		
	t_{13+1-}	1	1.1	4.7	1.1	3.5	4.5	1.1	4.8		3,9		13	1		
	t_{3+1+}	1	3.0	13	3.0	8.5	12.5	3.0	13.5		9		3	1		
	t_{3+15+}	15	2.5	13	3.0	8.0	12.5	2.5	13.5		9,14		3	15		
	t_{14+15+}	15	3.0	13	3.0	8.0	12.5	3.0	13.5		11		14	15		
Rise Time (20% to 80%)	t_{15+}	15	1.1	3.3	1.1	2.0	3.1	1.1	3.4		–		3	15		
Fall Time (20% to 80%)	t_{15-}	15	1.1	3.3	1.1	2.0	3.1	1.1	3.4		–		3	15		

*Apply +0.31 V to all other inputs.

APPLICATION INFORMATION

The MC10287 is a stand alone fully iterative dual multiplier cell. It is intended for use in parallel multiplier arrays where maximum speed is desired. Each cell is a modified gated adder/subtractor individually controlled by a mode select line. Internal carry lookahead (also called anticipated carry) is used to minimize sum and carry out delay times.

The mode controls are specifically buffered such that they can be grounded. Normally, MECL 10,000 device inputs should not be placed at ground to establish a high logic level. However, M0 and M1 can be used at ground potential for ease of layout in large arrays.

An array multiplier is defined as a multi-input, multi-output combinational logic circuit that forms the product of two binary numbers. Binary multiplication can be treated in two categories, that is, simple magnitude multiplication and 4-quadrant multiplication (requiring both positive and negative numbers).

MAGNITUDE BINARY MULTIPLICATION

Magnitude multiplication consists of the product of two binary numbers in which all digits are number bits (no sign bit). Magnitude representation then includes only positive numbers.

Thus, for a 4-bit number X the representation is:

$$X = x_3\, x_2\, x_1\, x_0$$

A 4-bit by 4-bit product becomes:

$$Z = X \cdot Y = (x_3\, x_2\, x_1\, x_0) \cdot (y_3\, y_2\, y_1\, y_0)$$

The product consists of the sum of the single-bit products formed by this expression. The standard "parallelogram" matrix of the single-bit products (or summands) can be written:

			x_3y_0	x_2y_0	x_1y_0	x_0y_0	
		x_3y_1	x_2y_1	x_1y_1	x_0y_1		
	x_3y_2	x_2y_2	x_1y_2	x_0y_2			
x_3y_3	x_2y_3	x_1y_3	x_0y_3				
z_7	z_6	z_5	z_4	z_3	z_2	z_1	z_0

The MC10287 is used in an array summing the single-bit products to form the final result. It is observed that the arithmetic product of binary digits x_j and y_i is also the logical product (x_j times y_i = x_j AND y_i). The AND function on the operand inputs of the MC10287 forms the single-bit products of the matrix directly and sums them internally. For magnitude binary multiplication, the MC10287 functions as a dual full adder (M0, M1 and both low).

The partial product array can be summed using a number of different techniques. The fastest technique is some form of matrix reduction scheme that prevents carry propagation until the final level of summation. Several of these schemes are discussed in detail in Reference 1.

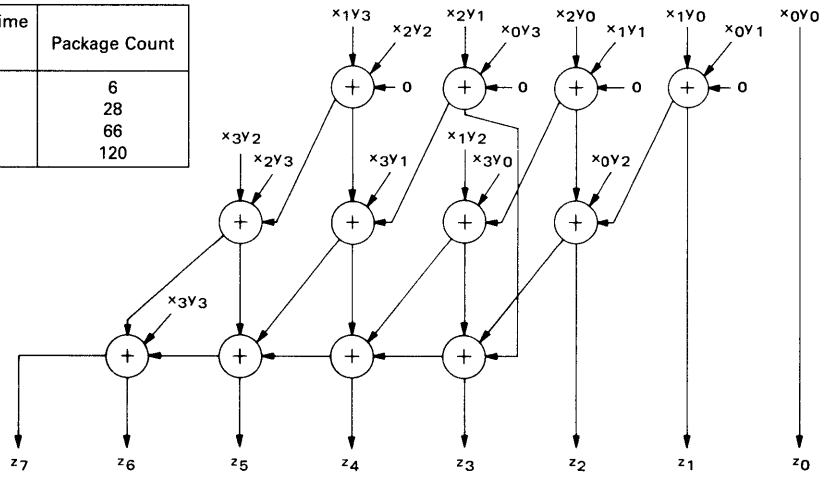
As an example, if the matrix is rearranged and written in a different form:

			x_0y_3				
		x_1y_3	x_3y_0	x_2y_0	x_1y_0	x_0y_0	
	x_2y_3	x_3y_1	x_2y_1	x_1y_1	x_0y_1		
x_3y_3	x_3y_2	x_2y_2	x_1y_2	x_0y_2			
z_7	z_6	z_5	z_4	z_3	z_2	z_1	z_0

TABLE 1 — TYPICAL MULTIPLY TIME FOR AN n-BIT BY n-BIT BINARY MAGNITUDE ARRAY MULTIPLIER

Number of Bits	Total Multiply Time (ns)	Package Count
4	14	6
8	25	28
12	39	66
16	44	120

FIGURE 1 — 4-BIT BY 4-BIT MAGNITUDE ARRAY MULTIPLIER



A basic adder/subtractor can then handle all the varying situations that appear in the multiplication matrix.

If the 2's complement matrix is rearranged:

$$
\begin{array}{cccccccc}
 & & & -x_0y_3 & & & & \\
 & & -x_1y_3 & -x_3y_0 & x_2y_0 & x_1y_0 & x_0y_0 & \\
 & -x_2y_3 & -x_3y_1 & x_2y_1 & x_1y_1 & x_0y_1 & & \\
x_3y_3 & -x_3y_2 & x_2y_2 & x_1y_2 & x_0y_2 & & & \\
\hline
-z_7 & z_6 & z_5 & z_4 & z_3 & z_2 & z_1 & z_0
\end{array}
$$

The adder/subtractor array for this configuration is shown in Figure 2. Care must be taken to insure that the proper mode of operation (add or subtract) appears at each summing node as a function of the positive and negative weighted inputs.

The summand matrix can be altered different ways to speed up the multiplier array. Reference 2 discusses the algorithm used with the MC10287 in detail. Also, the techniques of Reference 1 also apply to 2's complement arrays using the MC10287.

Table 2 gives typical multiply times for 2's complement arrays for n-bit by n-bit multipliers.

TABLE 2 — TYPICAL MULTIPLY TIME FOR AN n-BIT BY n-BIT 2's COMPLEMENT ARRAY MULTIPLIER

Number of Bits	Total Multiply Time (ns)	Package Count
4	14	6
8	25	28
12	39	66
16	44	120

IMPROVED SWITCHING DELAYS

The specified ac switching delays are given for output loading of 50 Ω to −2 volts. With lower output current, propagation delays will be improved and decreased multiply times can result. For output loading of 1 kΩ to V_{EE}, the following delays are typical.

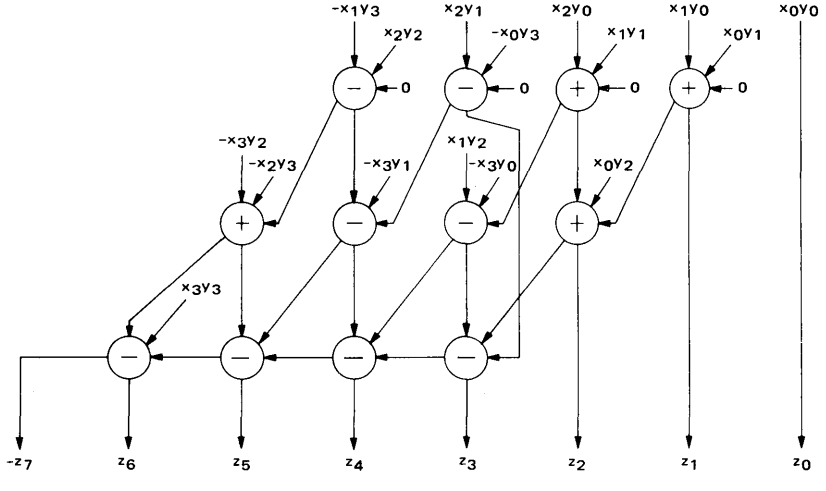
Input	Output	Delay (ns)
C0	C2	1.7
A0	C2	2.8
A0	S0	2.8
B0	S0	3.1
A0	S1	3.9
B0	S1	4.4
M0	S1	8.7

REFERENCE AND ACKNOWLEDGEMENT

The techniques for implementing the MC10287 in multiplier arrays resulted from work done originally at M.I.T. Lincoln Laboratories. Also, applications information presented here developed in part from personal correspondence with P. Blankenship of Lincoln Labs. The following references are useful in developing multipliers using the MC10287:

1. A. Habibi and P. A. Wintz, "Fast Multipliers," *IEEE Trans. Computers* (Short Notes), Vol. C-19, Feb. 1970, pp. 153–157.
2. S. D. Pezaris, "A 40-ns 17-Bit by 17-Bit Array Multiplier," *IEEE Trans. Computers,* Vol. C-20, Number 4, April, 1971; pp. 442–447.

FIGURE 2 — 4-BIT BY 4-BIT 2's COMPLEMENT ARRAY MULTIPLIER



The summation of the partial products for this configuration is shown in Figure 1. The number of MC10287's for an n-bit by n-bit array is $n(n-1)/2$. Note also that the least significant product bit ($z_0 = x_0y_0$) is formed by an individual AND gate (negative logic).

Table 1 gives package count and typical multiplication times for n-bit by n-bit magnitude multiplier arrays. The multiply times do not include wiring delays, and the package count does not include the gate for the least significant product bit.

FOUR-QUADRANT MULTIPLICATION

Sign-magnitude and 2's complement representations are commonly used for 4-quadrant multiplication. For sign-magnitude representation, the binary word consists of a sign bit and magnitude bits which indicate the absolute value of the number. For a 4-bit example:

$$X = x_s\, x_2\, x_1\, x_0$$

For $X \cdot Y = Z$

$$Z = X \cdot Y = (x_s\, x_2\, x_1\, x_0) \cdot (y_s\, y_2\, y_1\, y_0)$$

An array multiplier for this representation consists of an $(n-1)$-bit by $(n-1)$-bit magnitude multiplier that produces the product of the magnitude bits of X and Y and of logic that produces the proper product sign bit ($z_s = x_s \bigcirc y_s$).

2's complement representation also includes a sign bit which is a negative bit. That is:

$$X = -x_3\, x_2\, x_1\, x_0$$

where x_3 is the sign bit. The product of two 4-bit 2's complement numbers becomes:

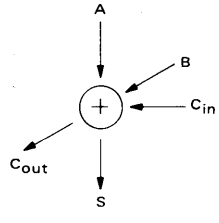
$$Z = X \cdot Y = (-x_3\, x_2\, x_1\, x_0) \cdot (-y_3\, y_2\, y_1\, y_0)$$

The matrix for this expression is:

$$\begin{array}{cccccccc}
 & & & -x_3y_0 & x_2y_0 & x_1y_0 & x_0y_0 & \\
 & & -x_3y_1 & x_2y_1 & x_1y_1 & x_0y_1 & & \\
 & -x_3y_2 & x_2y_2 & x_1y_2 & x_0y_2 & & & \\
x_3y_3 & -x_2y_3 & -x_1y_3 & -x_0y_3 & & & & \\
\hline
-z_7 & z_6 & z_5 & z_4 & z_3 & z_2 & z_1 & z_0
\end{array}$$

The product is the sum of this array of single-bit products. However, notice that several summands are negative quantities. Therefore, they can not be simply added as is the magnitude binary multiplier. The subtraction capability of the MC10287 is utilized when considering these negative quantities.

A standard full adder is symbolized as:



in which all inputs are positive quantities. If one input is negative (such as B), the outputs C_{out} and S must be coded such that they can represent the 4 possible output conditions. If B can be a negative one or zero, the net output can then be:

$$\text{net output} = \begin{cases} -1 \\ 0 \\ +1 \\ +2 \end{cases}$$

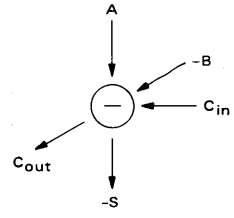
If C_{out}, whose weight is twice that of S, is assigned a positive value and S is a negative value, the above values can be represented:

$$\text{net output} = 2 \cdot C_{out} - S$$

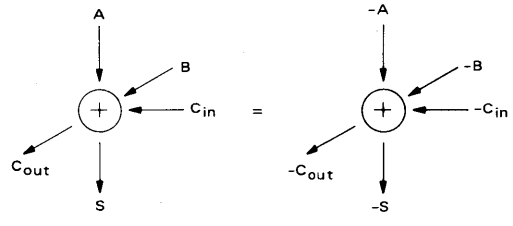
where:

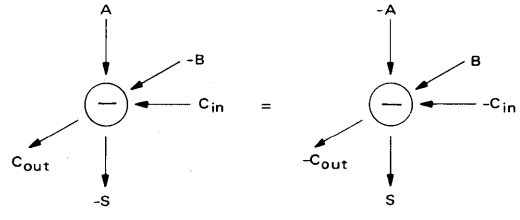
$$\begin{aligned} -1 &= 0 - 1 \\ 0 &= 0 - 0 \\ +1 &= 2 - 1 \\ +2 &= 2 - 0 \end{aligned}$$

If the truth table is written and logic equations generated, the result is a subtractor. That is, a subtractor used in place of a full adder produces the proper outputs. The symbol for the subtractor is:



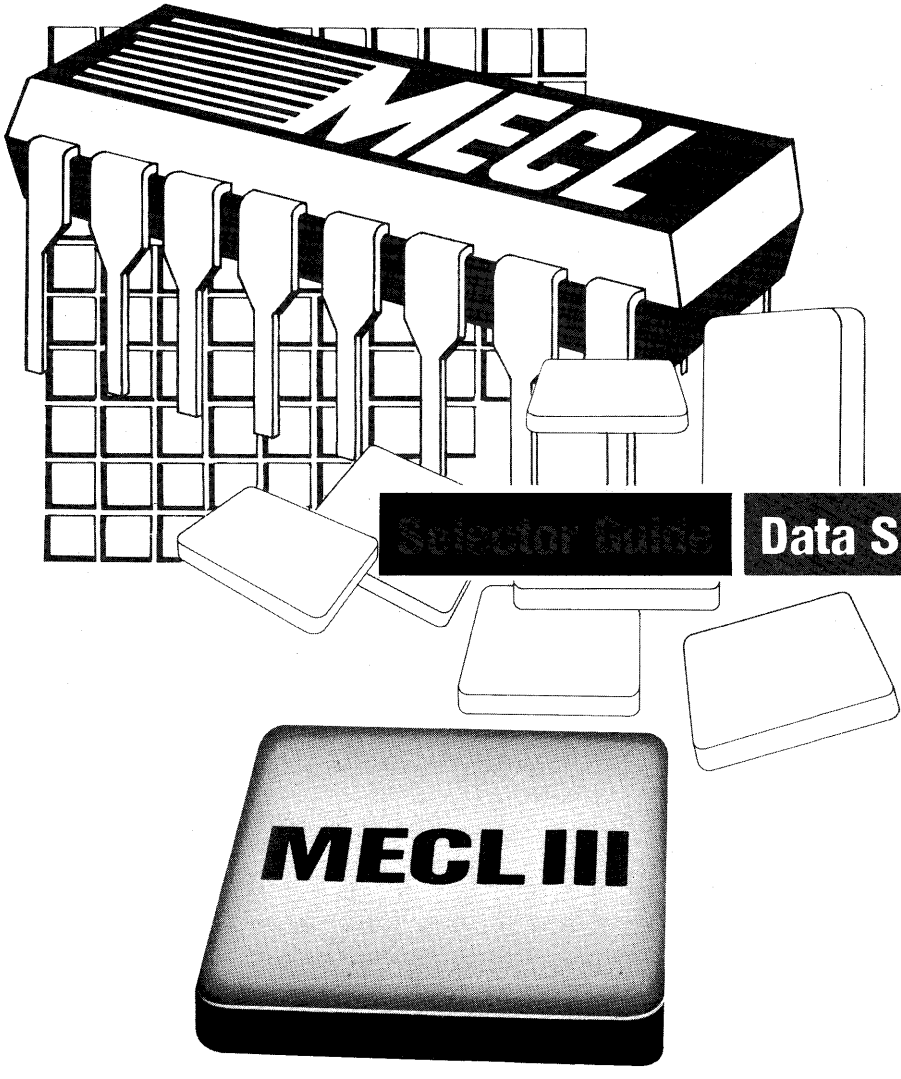
Also, if the input variables are multiplied by -1, the outputs also are multiplied by -1. Thus, the following devices are equivalent:





MC10287 FUNCTIONAL TRUTH TABLE

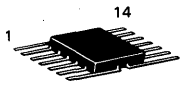
M1	M0	b1	b1′	a1	a1′	b0	b0′	a0	a0′	C0	S0	S1	C2	
14	3	13	12	11	10	4	5	6	7	9	2	1	15	Word
H	H	H	H	H	H	H	H	H	H	H	H	H	H	0
H	H	H	H	H	H	H	H	H	H	L	L	L	L	1
H	H	H	H	H	H	H	H	L	L	H	L	L	L	2
H	H	H	H	H	H	H	H	L	L	L	H	L	L	3
H	H	H	H	H	H	L	L	H	H	H	L	H	H	4
H	H	H	H	H	H	L	L	H	H	L	H	H	H	5
H	H	H	H	H	H	L	L	L	L	H	H	H	H	6
H	H	H	H	H	H	L	L	L	L	L	L	L	L	7
H	H	H	H	L	L	H	H	H	H	H	H	L	L	8
H	H	H	H	L	L	H	H	H	H	L	L	H	L	9
H	H	H	H	L	L	H	H	L	L	H	L	H	L	10
H	H	H	H	L	L	H	H	L	L	L	H	H	L	11
H	H	H	H	L	L	L	L	H	H	H	L	L	L	12
H	H	H	H	L	L	L	L	H	H	L	H	L	L	13
H	H	H	H	L	L	L	L	L	L	H	H	L	L	14
H	H	H	H	L	L	L	L	L	L	L	L	H	L	15
H	H	L	L	H	H	H	H	H	H	H	H	L	H	16
H	H	L	L	H	H	H	H	H	H	L	L	H	H	17
H	H	L	L	H	H	H	H	L	L	H	L	H	L	18
H	H	L	L	H	H	H	H	L	L	L	H	H	H	19
H	H	L	L	H	H	L	L	H	H	H	L	L	H	20
H	H	L	L	H	H	L	L	H	H	L	H	L	H	21
H	H	L	L	H	H	L	L	L	L	H	H	L	L	22
H	H	L	L	H	H	L	L	L	L	L	L	H	H	23
H	H	L	L	L	L	H	H	H	H	H	H	H	H	24
H	H	L	L	L	L	H	H	H	H	L	L	L	L	25
H	H	L	L	L	L	H	H	L	L	H	L	L	L	26
H	H	L	L	L	L	H	H	L	L	L	H	L	L	27
H	H	L	L	L	L	L	L	H	H	H	L	H	H	28
H	H	L	L	L	L	L	L	H	H	L	H	H	H	29
H	H	L	L	L	L	L	L	L	L	H	H	H	H	30
H	H	L	L	L	L	L	L	L	L	L	L	L	L	31
H	L	H	H	H	H	H	H	H	H	H	H	H	H	32
H	L	H	H	H	H	H	H	H	H	L	L	H	H	33
H	L	H	H	H	H	H	H	L	L	H	L	H	H	34
H	L	H	H	H	H	H	H	L	L	L	H	L	L	35
H	L	H	H	H	H	L	L	H	H	H	L	H	H	36
H	L	H	H	H	H	L	L	H	H	L	H	L	L	37
H	L	H	H	H	H	L	L	L	L	H	H	L	L	38
H	L	H	H	H	H	L	L	L	L	L	L	L	L	39
H	L	H	H	L	L	H	H	H	H	H	H	L	L	40
H	L	H	H	L	L	H	H	H	H	L	L	L	L	41
H	L	H	H	L	L	H	H	L	L	H	L	L	L	42
H	L	H	H	L	L	H	H	L	L	L	H	H	L	43
H	L	H	H	L	L	L	L	H	H	H	L	L	H	44
H	L	H	H	L	L	L	L	H	H	L	H	H	L	45
H	L	H	H	L	L	L	L	L	L	H	H	H	L	46
H	L	H	H	L	L	L	L	L	L	L	L	L	H	47
H	L	L	L	H	H	H	H	H	H	H	H	L	H	48
H	L	L	L	H	H	H	H	H	H	L	L	L	H	49
H	L	L	L	H	H	H	H	L	L	H	L	L	H	50
H	L	L	L	H	H	H	H	L	L	L	H	H	H	51
H	L	L	L	H	H	L	L	H	H	H	L	L	H	52
H	L	L	L	H	H	L	L	H	H	L	H	H	H	53
H	L	L	L	H	H	L	L	L	L	H	H	H	H	54
H	L	L	L	H	H	L	L	L	L	L	L	H	H	55
H	L	L	L	L	L	H	H	H	H	H	H	H	H	56
H	L	L	L	L	L	H	H	H	H	L	L	H	H	57
H	L	L	L	L	L	H	H	L	L	H	L	H	H	58
H	L	L	L	L	L	H	H	L	L	L	H	L	L	59
H	L	L	L	L	L	L	L	H	H	H	L	H	H	60
H	L	L	L	L	L	L	L	H	H	L	H	L	L	61
H	L	L	L	L	L	L	L	L	L	H	H	L	L	62
H	L	L	L	L	L	L	L	L	L	L	L	L	L	63
L	H	H	H	H	H	H	H	H	H	H	H	H	H	64
L	H	H	H	H	H	H	H	H	H	L	L	L	H	65
L	H	H	H	H	H	H	H	L	L	H	L	L	H	66
L	H	H	H	H	H	H	H	L	L	L	H	L	H	67
L	H	H	H	H	H	L	L	H	H	H	L	H	H	68
L	H	H	H	H	H	L	L	H	H	L	L	H	H	69
L	H	H	H	H	H	L	L	L	L	H	H	H	H	70
L	H	H	H	H	H	L	L	L	L	L	L	L	H	71
L	H	H	H	L	L	H	H	H	H	H	H	L	H	72
L	H	H	H	L	L	H	H	H	H	L	L	H	L	73
L	H	H	H	L	L	H	H	L	L	H	L	H	L	74
L	H	H	H	L	L	H	H	L	L	L	H	H	L	75
L	H	H	H	L	L	L	L	H	H	H	L	L	H	76
L	H	H	H	L	L	L	L	H	H	L	H	L	H	77
L	H	H	H	L	L	L	L	L	L	H	H	L	H	78
L	H	H	H	L	L	L	L	L	L	L	L	H	L	79
L	H	L	L	H	H	H	H	H	H	H	H	L	H	80
L	H	L	L	H	H	H	H	H	H	L	L	H	L	81
L	H	L	L	H	H	H	H	L	L	H	L	H	L	82
L	H	L	L	H	H	H	H	L	L	L	H	H	L	83
L	H	L	L	H	H	L	L	H	H	H	L	L	H	84
L	H	L	L	H	H	L	L	H	H	L	H	H	L	85
L	H	L	L	H	H	L	L	L	L	H	H	L	H	86
L	H	L	L	H	H	L	L	L	L	L	L	H	L	87
L	H	L	L	L	L	H	H	H	H	H	H	H	L	88
L	H	L	L	L	L	H	H	H	H	L	L	L	L	89
L	H	L	L	L	L	H	H	L	L	H	H	L	L	90
L	H	L	L	L	L	H	H	L	L	L	L	H	L	91
L	H	L	L	L	L	L	L	H	H	H	L	H	L	92
L	H	L	L	L	L	L	L	H	H	L	H	H	L	93
L	H	L	L	L	L	L	L	L	L	H	H	H	L	94
L	H	L	L	L	L	L	L	L	L	L	L	L	L	95
L	L	H	H	H	H	H	H	H	H	H	H	H	H	96
L	L	H	H	H	H	H	H	H	H	L	L	H	H	97
L	L	H	H	H	H	H	H	L	L	H	L	H	H	98
L	L	H	H	H	H	H	H	L	L	L	H	L	H	99
L	L	H	H	H	H	L	L	H	H	H	L	H	H	100
L	L	H	H	H	H	L	L	H	H	L	H	L	H	101
L	L	H	H	H	H	L	L	L	L	H	H	L	H	102
L	L	H	H	H	H	L	L	L	L	L	L	L	H	103
L	L	H	H	L	L	H	H	H	H	H	L	L	H	104
L	L	H	H	L	L	H	H	L	L	L	H	L	H	105
L	L	H	H	L	L	H	H	L	L	H	L	L	H	106
L	L	H	H	L	L	H	H	L	L	L	H	H	L	107
L	L	H	H	L	L	L	L	H	H	H	L	L	H	108
L	L	H	H	L	L	L	L	H	H	L	H	H	L	109
L	L	H	H	L	L	L	L	L	L	H	H	H	L	110
L	L	H	H	L	L	L	L	L	L	L	L	H	L	111
L	L	L	L	H	H	H	H	H	H	H	H	L	H	112
L	L	L	L	H	H	H	H	H	H	L	L	L	H	113
L	L	L	L	H	H	H	H	L	L	H	L	L	H	114
L	L	L	L	H	H	H	H	L	L	L	H	H	L	115
L	L	L	L	H	H	L	L	H	H	H	L	L	H	116
L	L	L	L	H	H	L	L	H	H	L	H	H	L	117
L	L	L	L	H	H	L	L	L	L	H	H	H	L	118
L	L	L	L	H	H	L	L	L	L	L	L	H	L	119
L	L	L	L	L	L	H	H	H	H	H	H	H	L	120
L	L	L	L	L	L	H	H	H	H	L	L	H	L	121
L	L	L	L	L	L	H	H	L	L	H	L	H	L	122
L	L	L	L	L	L	H	H	L	L	L	H	L	L	123
L	L	L	L	L	L	L	L	H	H	H	L	H	L	124
L	L	L	L	L	L	L	L	H	H	L	H	L	L	125
L	L	L	L	L	L	L	L	L	L	H	H	L	L	126
L	L	L	L	L	L	L	L	L	L	L	L	L	L	127
L	L	H	L	L	L	L	L	L	L	L	L	H	L	128
L	L	L	H	L	L	L	L	L	L	L	L	H	L	129
L	L	L	L	H	L	L	L	L	L	L	L	H	L	130
L	L	L	L	L	H	L	L	L	L	L	L	H	L	131
L	L	L	L	L	L	H	L	L	L	L	H	L	L	132
L	L	L	L	L	L	L	H	L	L	L	H	L	L	133
L	L	L	L	L	L	L	L	H	L	L	H	L	L	134
L	L	L	L	L	L	L	L	L	H	L	H	L	L	135



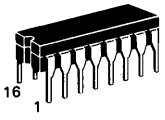
Selector Guide | Data Sheets | 4

MECL III
INTEGRATED CIRCUITS

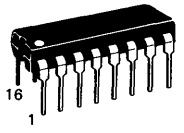
MC1600 Series
(−30 to +85°C)



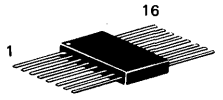
F SUFFIX
CERAMIC PACKAGE
CASE 607



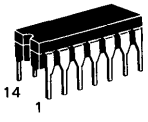
L SUFFIX
CERAMIC PACKAGE
CASE 620



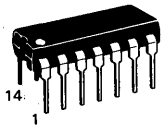
P SUFFIX
PLASTIC PACKAGE
CASE 648



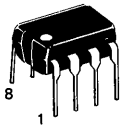
F SUFFIX
CERAMIC PACKAGE
CASE 650



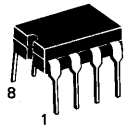
L SUFFIX
CERAMIC PACKAGE
CASE 632



P SUFFIX
PLASTIC PACKAGE
CASE 646



P SUFFIX
PLASTIC PACKAGE
CASE 626



L SUFFIX
CERAMIC PACKAGE
CASE 693

4

Function Selection—(−30 to +85°C)

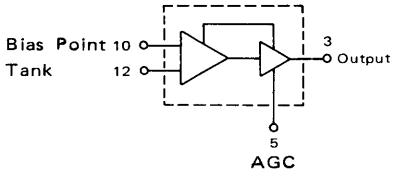
Function	Device	Case
Gates		
Dual 4-Input OR/NOR	MC1660	620
Dual 4-5-Input OR/NOR	MC1688	620, 650
Quad 2-Input NOR	MC1662	620
Triple 2-Input Exclusive NOR	MC1674	620
Quad 2-Input OR	MC1664	620
Triple 2-Input Exclusive OR	MC1672	620
Flip-Flops		
Dual Clocked R-S	MC1666	620
Dual Clocked Latch	MC1668	620
Master-Slave Type D	MC1670	620
UHF Prescaler Type D	MC1690	620
Counters		
Binary	MC1654	620
Bi-Quinary	MC1678	620
1 GHz Divide-by-Four	MC1699	620, 648

Function	Device	Case
Shift Register		
4-Bit Shift	MC1694	620
Multivibrator		
Voltage-Controlled	MC1658	620, 648
Oscillator		
Emitter Coupled	MC1648	607, 632, 646
Comparator		
Dual A/D	MC1650/ MC1651	620, 650
Receiver		
Quad-Line	MC1692	620, 650
Prescaler		
1 GHz Divide-by-Four	MC1697*	626, 693

*0°C to 75°C

MC1648/MC1648M

VOLTAGE-CONTROLLED OSCILLATOR



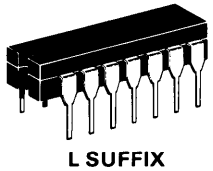
Input Capacitance = 6 pF typ
Maximum Series Resistance for L (External Inductance) = 50 Ω typ
Power Dissipation = 150 mW typ/pkg (+5.0 Vdc Supply)
Maximum Output Frequency = 225 MHz typ

The MC1648 requires an external parallel tank circuit consisting of the inductor (L) and capacitor (C).

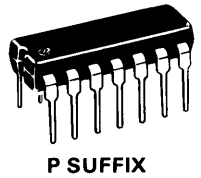
A varactor diode may be incorporated into the tank circuit to provide a voltage variable input for the oscillator (VCO). The MC1648 was designed for use in the Motorola Phase-Locked Loop shown in Figure 9. This device may also be used in many other applications requiring a fixed or variable frequency clock source of high spectral purity. (See Figure 2.)

The MC1648 may be operated from a +5.0 Vdc supply or a −5.2 Vdc supply, depending upon system requirements.

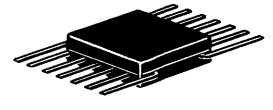
Supply Voltage	Gnd Pins	Supply Pins
+5.0 Vdc	7, 8	1, 14
−5.2 Vdc	1, 14	7, 8



L SUFFIX
CERAMIC PACKAGE
CASE 632

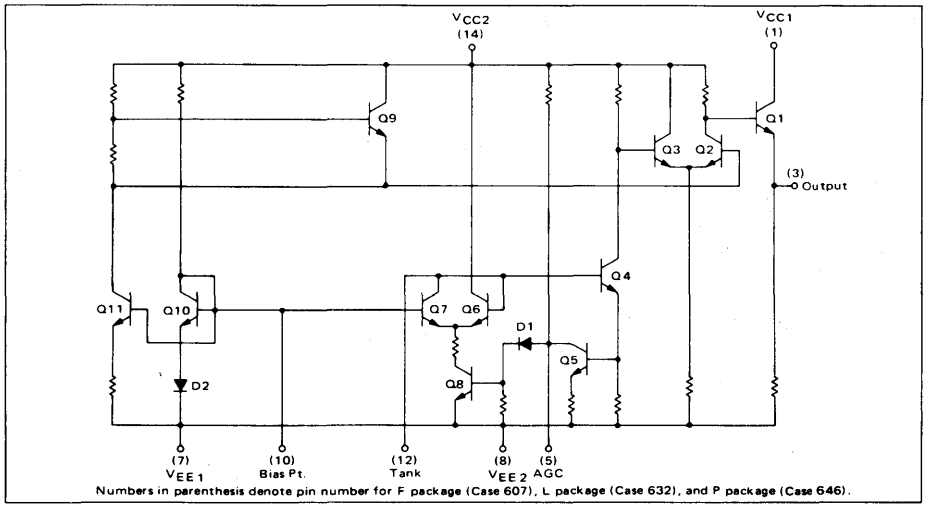


P SUFFIX
PLASTIC PACKAGE
CASE 646



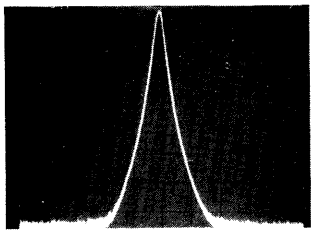
F SUFFIX
CERAMIC PACKAGE
CASE 607

FIGURE 1 – CIRCUIT SCHEMATIC

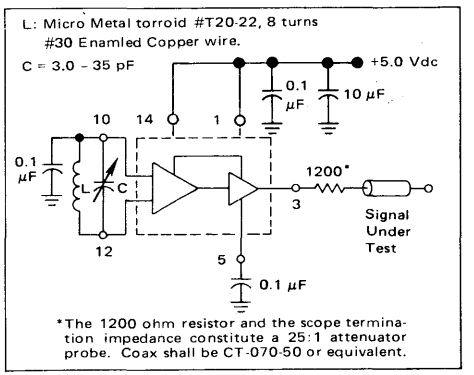


Numbers in parenthesis denote pin number for F package (Case 607), L package (Case 632), and P package (Case 646).

FIGURE 2 – SPECTRAL PURITY OF SIGNAL AT OUTPUT



B.W. = 10 kHz
Center Frequency = 100 MHz
Scan Width = 50 kHz/div
Vertical Scale = 10 dB/div



@ Test Temperature	TEST VOLTAGE/CURRENT VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{CC}	mAdc I_L
MC1648				
-30°C	+2.00	+1.50	5.0	-5.0
+25°C	+1.85	+1.35	5.0	-5.0
+85°C	+1.70	+1.20	5.0	-5.0
MC1648M				
-55°C	+2.07	+1.57	5.0	-5.0
+25°C	+1.85	+1.35	5.0	-5.0
+125°C	+1.60	+1.10	5.0	-5.0

ELECTRICAL CHARACTERISTICS

Supply Voltage = +5.0 Volts

Characteristic	Symbol	-55°C			-30°C			+25°C			+85°C			+125°C			Unit	Conditions
		Min		Max	Min		Max	Min		Max	Min		Max	Min		Max		
Power Supply Drain Current	I_E	–		–	–		–	–		41	–		–	–		–	mAdc	Inputs and outputs open.
Logic "1" Output Voltage	V_{OH}	3.92		4.13	3.955		4.185	4.04		4.25	4.11		4.36	4.16		4.40	Vdc	V_{ILmin} to Pin 12, I_L @ Pin 3.
Logic "0" Output Voltage	V_{OL}	3.13		3.38	3.16		3.40	3.20		3.43	3.22		3.475	3.23		3.51	Vdc	V_{IHmax} to Pin 12, I_L @ Pin 3.
Bias Voltage	V_{Bias}*	1.67		1.97	1.60		1.90	1.45		1.75	1.30		1.60	1.20		1.50	Vdc	V_{ILmin} to Pin 12.
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
Peak-to-Peak Tank Voltage	V_{P-P}	–	–	–	–	–	–	–	400	–	–	–	–	–	–	–	mV	See Figure 3.
Output Duty Cycle	V_{DC}	–	–	–	–	–	–	–	50	–	–	–	–	–	–	–	%	
Oscillation Frequency	f_{max}**	–	225	–	–	225	–	200	225	–	–	225	–	–	225	–	MHz	

*This measurement guarantees the dc potential at the bias point for purposes of incorporating a varactor turning diode at this point.

**Frequency variation over temperature is a direct function of the $\Delta C/\Delta$ Temperature and $\Delta L/\Delta$ Temperature.

@ Test Temperature	TEST VOLTAGE/CURRENT VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{CC}	mAdc I_L
	MC1648			
-30°C	-3.20	-3.70	-5.2	-5.0
+25°C	-3.35	-3.85	-5.2	-5.0
+85°C	-3.50	-4.00	-5.2	-5.0
	MC1648M			
-55°C	-3.13	-3.63	-5.2	-5.0
+25°C	-3.35	-3.85	-5.2	-5.0
+125°C	-3.60	-4.10	-5.2	-5.0

ELECTRICAL CHARACTERISTICS

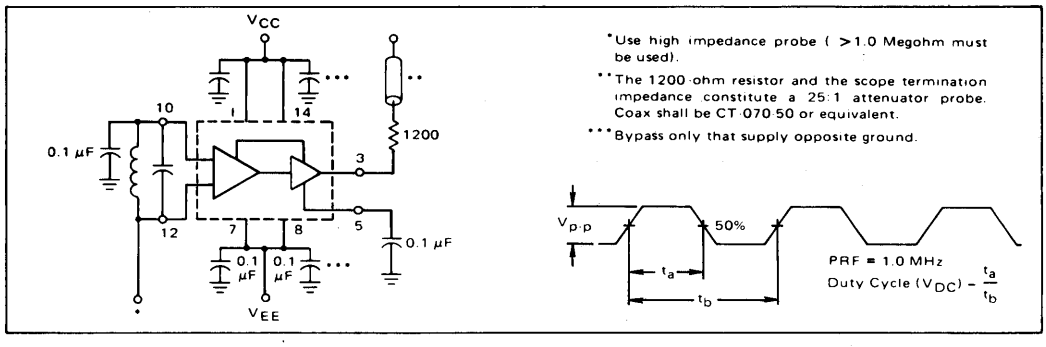
Supply Voltage = -5.2 Volts

Characteristic	Symbol	-55°C			-30°C			+25°C			+85°C			+125°C			Unit	Conditions
		Min		Max	Min		Max	Min		Max	Min		Max	Min		Max		
Power Supply Drain Current	I_E	–		–	–		–	–		41	–		–	–		–	mAdc	Inputs and outputs open.
Logic "1" Output Voltage	V_{OH}	-1.080		-0.870	-1.045		-0.815	-0.960		-0.750	-0.890		-0.640	-0.840		-0.600	Vdc	V_{ILmin} to Pin 12, I_L @ Pin 3.
Logic "0" Output Voltage	V_{OL}	-1.920		-1.670	-1.890		-1.650	-1.850		-1.620	-1.830		-1.575	-1.820		-1.540	Vdc	V_{IHmax} to Pin 12, I_L @ Pin 3.
Bias Voltage	V_{Bias}*	-3.53		-3.23	-3.60		-3.30	-3.75		-3.45	-3.90		-3.60	-4.00		-3.70	Vdc	V_{ILmin} to Pin 12.
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
Peak-to-Peak Tank Voltage	V_{P-P}	–	–	–	–	–	–	–	400	–	–	–	–	–	–	–	mV	See Figure 3.
Output Duty Cycle	V_{DC}	–	–	–	–	–	–	–	50	–	–	–	–	–	–	–	%	
Oscillation Frequency	f_{max}**	–	225	–	–	225	–	200	225	–	–	225	–	–	225	–	MHz	

*This measurement guarantees the dc potential at the bias point for purposes of incorporating a varactor turning diode at this point.

**Frequency variation over temperature is a direct function of the $\Delta C/\Delta$ Temperature and $\Delta L/\Delta$ Temperature.

FIGURE 3 – TEST CIRCUIT AND WAVEFORMS



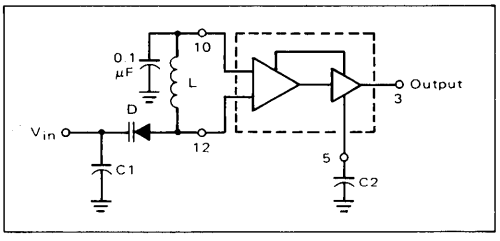
OPERATING CHARACTERISTICS

Figure 1 illustrates the circuit schematic for the MC1648. The oscillator incorporates positive feedback by coupling the base of transistor Q6 to the collector of Q7. An automatic gain control (AGC) is incorporated to limit the current through the emitter-coupled pair of transistors (Q7 and Q6) and allow optimum frequency response of the oscillator.

In order to maintain the high Q of the oscillator, and provide high spectral purity at the output, transistor Q4 is used to translate the oscillator signal to the output differential pair Q2 and Q3. Q2 and Q3, in conjunction with output transistor Q1, provides a highly buffered output which produces a square wave. Transistors Q9 and Q11 provide the bias drive for the oscillator and output buffer. Figure 2 indicates the high spectral purity of the oscillator output (pin 3).

When operating the oscillator in the voltage controlled mode (Figure 4), it should be noted that

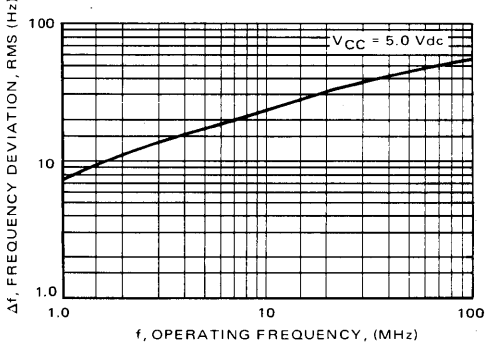
FIGURE 4 – THE MC1648 OPERATING IN THE VOLTAGE CONTROLLED MODE



the cathode of the varactor diode (D) should be biased at least 2 V_{BE} above V_{EE} (≈1.4 V for positive supply operation).

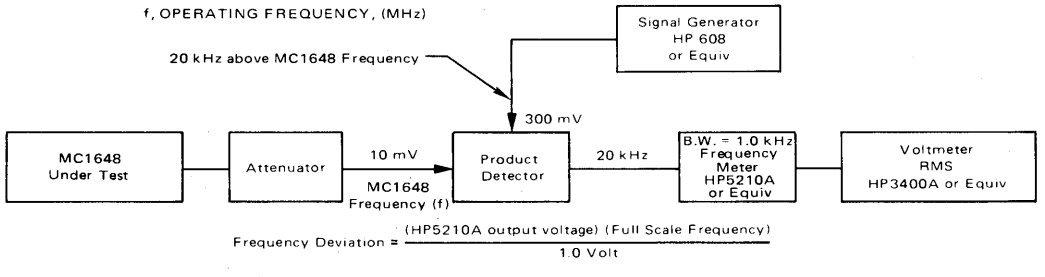
When the MC1648 is used with a constant dc voltage to the varactor diode, the output frequency will vary slightly because of internal noise. This variation is plotted versus operating frequency in Figure 5.

FIGURE 5 – NOISE DEVIATION TEST CIRCUIT AND WAVEFORM



Oscillator Tank Components
(Circuit of Figure 4)

f MHz	D	L μH
1.0-10	MV2115	100
10-60	MV2115	2.3
60-100	MV2106	0.15



$$\text{Frequency Deviation} = \frac{\text{(HP5210A output voltage) (Full Scale Frequency)}}{\text{1.0 Volt}}$$

NOTE: Any frequency deviation caused by the signal generator and MC1648 power supply should be determined and minimzed prior to testing.

TRANSFER CHARACTERISTICS IN THE VOLTAGE CONTROLLED MODE USING EXTERNAL VARACTOR DIODE AND COIL. $T_A = 25^oC$

FIGURE 6

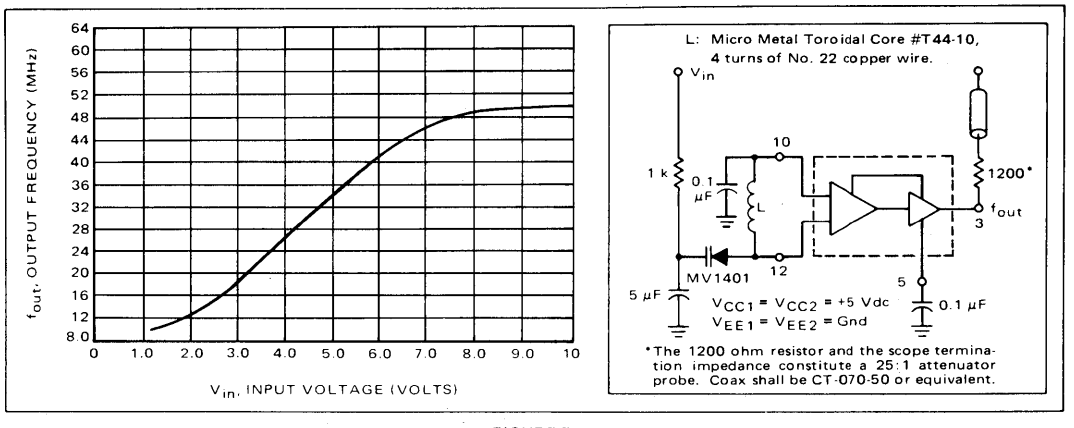


FIGURE 7

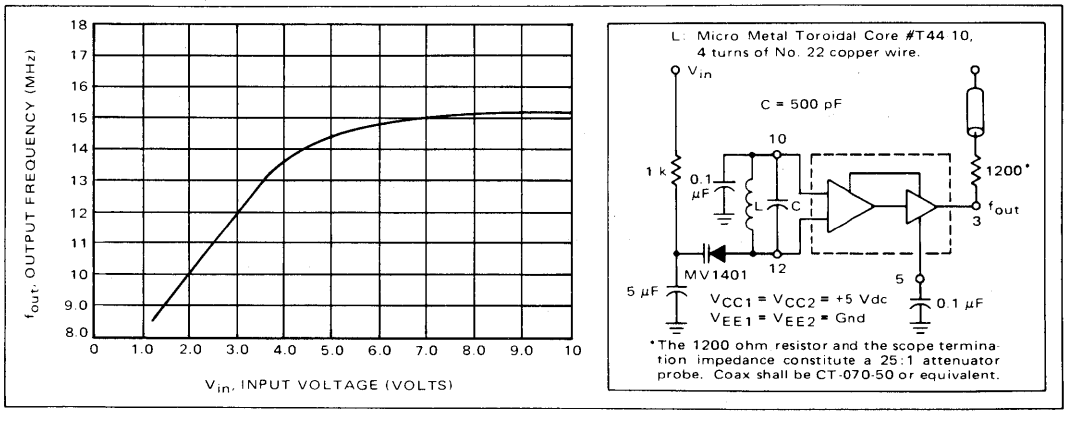
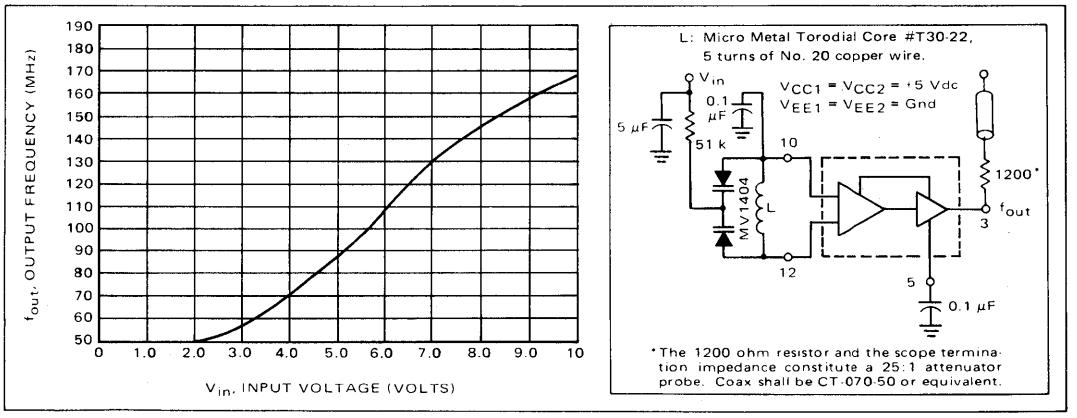


FIGURE 8



4

Typical transfer characteristics for the oscillator in the voltage controlled mode are shown in Figures 6, 7, and 8. Figures 6 and 8 show transfer characteristics employing only the capacitance of the varactor diode (plus the input capacitance of the oscillator, 6 pF typical). Figure 7 illustrates the oscillator operating in a voltage controlled mode with the output frequency range limited. This is achieved by adding a capacitor in parallel with the tank circuit as shown. The 1 kΩ resistor in Figures 6 and 7 is used to protect the varactor diode during testing. It is not necessary as long as the dc input voltage does not cause the diode to become forward biased. The larger-valued resistor (51 kΩ) in Figure 8 is required to provide isolation for the high-impedance junctions of the two varactor diodes.

The tuning range of the oscillator in the voltage controlled mode may be calculated as:

$$\frac{f_{max}}{f_{min}} = \frac{\sqrt{C_D(max) + C_S}}{\sqrt{C_D(min) + C_S}}$$

where $f_{min} = \frac{1}{2\pi\sqrt{L(C_D(max) + C_S)}}$

C_S = shunt capacitance (input plus external capacitance).

C_D = varactor capacitance as a function of bias voltage.

Good RF and low-frequency bypassing is necessary on the power supply pins. (See Figure 2.)

Capacitors (C1 and C2 of Figure 4) should be used to bypass the AGC point and the VCO input (varactor diode), guaranteeing only dc levels at these points.

For output frequency operation between 1 MHz and 50 MHz a 0.1 μF capacitor is sufficient for C1 and C2. At higher frequencies, smaller values of capacitance should be used; at lower frequencies, larger values of capacitance. At high frequencies the value of bypass capacitors depends directly upon the physical layout of the system. All bypassing should be as close to the package pins as possible to minimize unwanted lead inductance.

The peak-to-peak swing of the tank circuit is set internally by the AGC circuitry. Since voltage swing of the tank circuit provides the drive for the output buffer, the AGC potential directly affects the output waveform. If it is desired to have a sine wave at the output of the MC1648, a series resistor is tied from the AGC point to the most negative power potential (ground if +5.0 volt supply is used, −5.2 volts if a negative supply is used) as shown in Figure 10.

At frequencies above 100 MHz typ, it may be desirable to increase the tank circuit peak-to-peak voltage in order to shape the signal at the output of the MC1648. This is accomplished by tying a series resistor (1 kΩ minimum) from the AGC to the most positive power potential (+5.0 volts if a +5.0 volt supply is used, ground if a −5.2 volt supply is used). Figure 11 illustrates this principle.

APPLICATIONS INFORMATION

The phase locked loop shown in Figure 9 illustrates the use of the MC1648 as a voltage controlled oscillator. The figure illustrates a frequency synthesizer useful in tuners for FM broadcast, general aviation, maritime and landmobile communications, amateur and CB receivers. The system operates from a single +5.0 Vdc supply, and requires no internal translations, since all components are compatible.

Frequency generation of this type offers the advantages of single crystal operation, simple channel selection, and elimination of special circuitry to prevent harmonic lockup. Additional features include dc digital switching (preferable over RF switching with a multiple crystal system), and a broad range of tuning (up to 150 MHz, the range being set by the varactor diode).

The output frequency of the synthesizer loop is determined by the reference frequency and the number programmed at the programmable counter; $f_{out} = Nf_{ref}$. The channel spacing is equal to frequency (f_{ref}).

For additional information on applications and designs for phase locked-loops and digital frequency synthesizers. see Motorola Application Notes AN-532A, AN-535, AN-553, AN-564 or AN594.

FIGURE 9 – TYPICAL FREQUENCY SYNTHESIZER APPLICATION

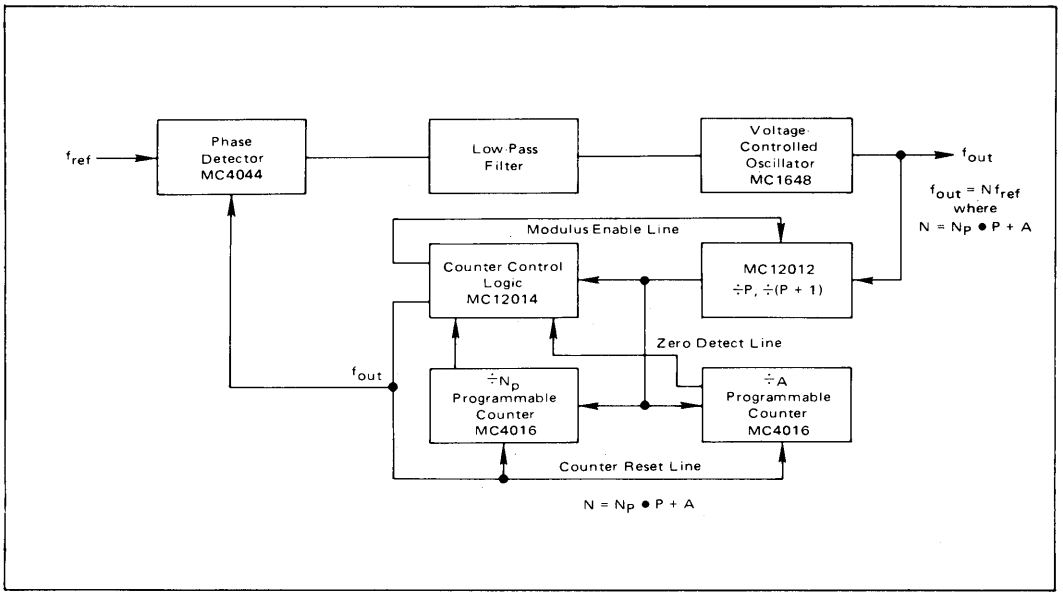


Figure 10 shows the MC1648 in the variable frequency mode operating from a +5.0 Vdc supply. To obtain a sine wave at the output, a resistor is added from the AGC circuit (pin 5) to V_{EE}.

Figure 11 shows the MC1648 in the variable frequency mode operating from a +5.0 Vdc supply. To extend the useful range of the device (maintain a square wave output above 175 MHz), a resistor is added to the AGC circuit at pin 5 (1 k-ohm minimum).

Figure 12 shows the MC1648 operating from +5.0 Vdc and +9.0 Vdc power supplies. This permits a higher voltage swing and higher output power than is possible from the MECL output (pin 3). Plots of output power versus total collector load resistance at pin 1 are given in Figures 13 and 14 for 100 MHz and 10 MHz operation. The total collector load includes R in parallel with Rp of L1 and C1 at resonance. The optimum value for R at 100 MHz is approximately 850 ohms.

FIGURE 10 – METHOD OF OBTAINING A SINE-WAVE OUTPUT

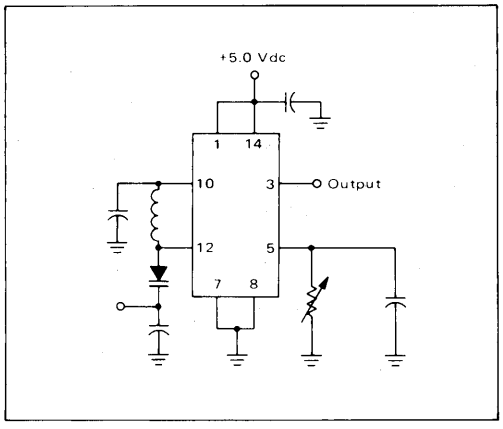


FIGURE 11 – METHOD OF EXTENDING THE USEFUL RANGE OF THE MC1648 (SQUARE WAVE OUTPUT)

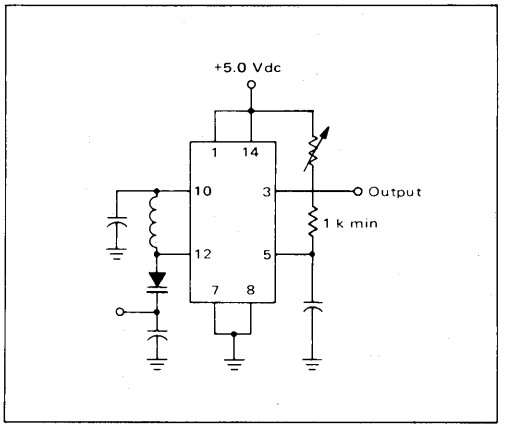


FIGURE 12 – CIRCUIT USED FOR COLLECTOR OUTPUT OPERATION

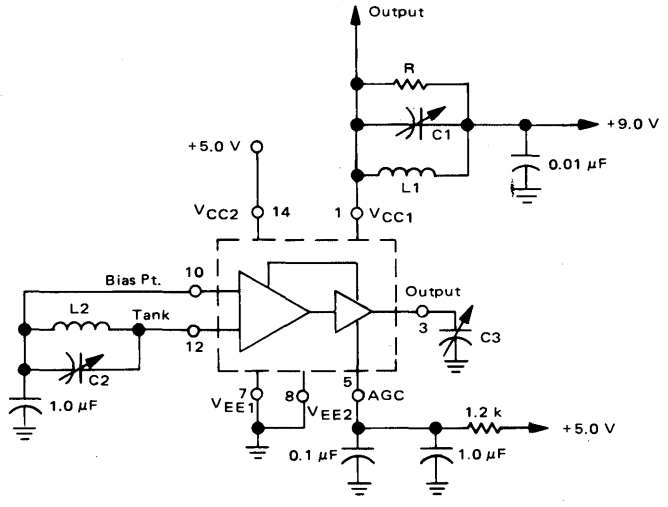


FIGURE 13 – POWER OUTPUT versus COLLECTOR LOAD

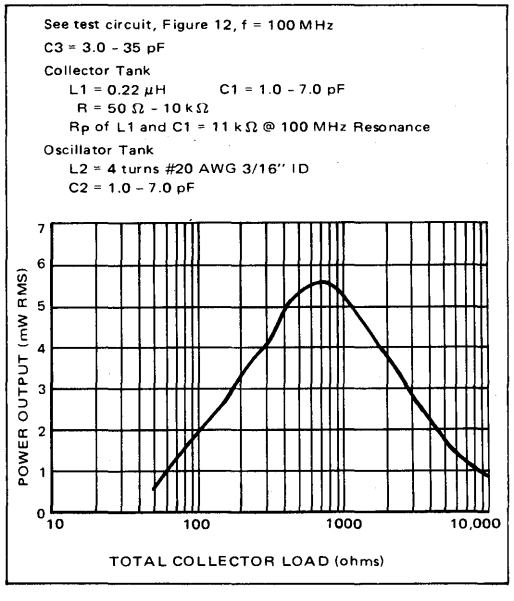
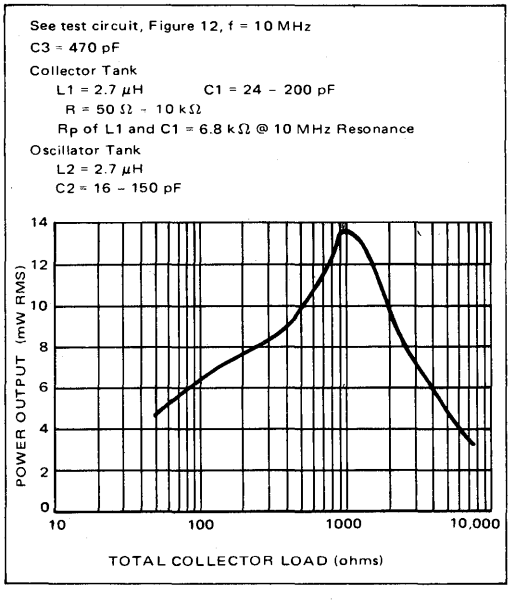
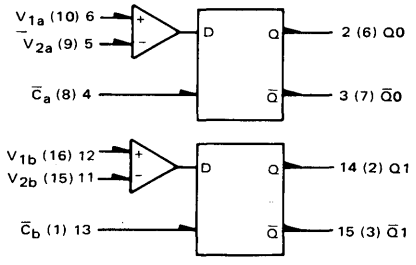


FIGURE 14 – POWER OUTPUT versus COLLECTOR LOAD



MC1650/MC1651

DUAL A/D CONVERTER



V_{CC} = +5.0 V = Pin 7,10 - (11), (14)
V_{EE} = -5.2 V = Pin 8 (12)
Gnd = Pin 1,16 (4) (5)

- P_D = 330 mW typ/pkg (No Load)
- t_{pd} = 3.5 ns typ (MC1650)
  = 3.0 ns typ (MC1651)
- Input Slew Rate = 350 V/μs (MC1650)
  = 500 V/μs (MC1651)
- Differential Input Voltage:
  5.0 V (-30°C to +85°C)
- Common Mode Range:
  -3.0 V to +2.5 V (-30°C to +85°C) (MC1651)
  -2.5 V to +3.0 V (-30°C to +85°C) (MC1650)
- Resolution: ≤20 mV (-30°C to +85°C)
- Drives 50 Ω lines

Number at end of terminal denotes pin number for L package (Case 620).
Number in parenthesis denotes pin number for F package (Case 650).

The MC1650 and the MC1651 are very high speed comparators utilizing differential amplifier inputs to sense analog signals above or below a reference level. An output latch provides a unique sample-hold feature. The MC1650 provides high impedance Darlington inputs, while the MC1651 is a lower impedance option, with higher input slew rate and higher speed capability.

The clock inputs ($\overline{C}_a$ and $\overline{C}_b$) operate from MECL III or MECL 10,000 digital levels. When $\overline{C}_a$ is at a logic high level, Q0 will be at a logic high level provided that $V_1 > V_2$ (V_1 is more positive than V_2). $\overline{Q}0$ is the logic complement of Q0. When the clock input goes to a low logic level, the outputs are latched in their present state.

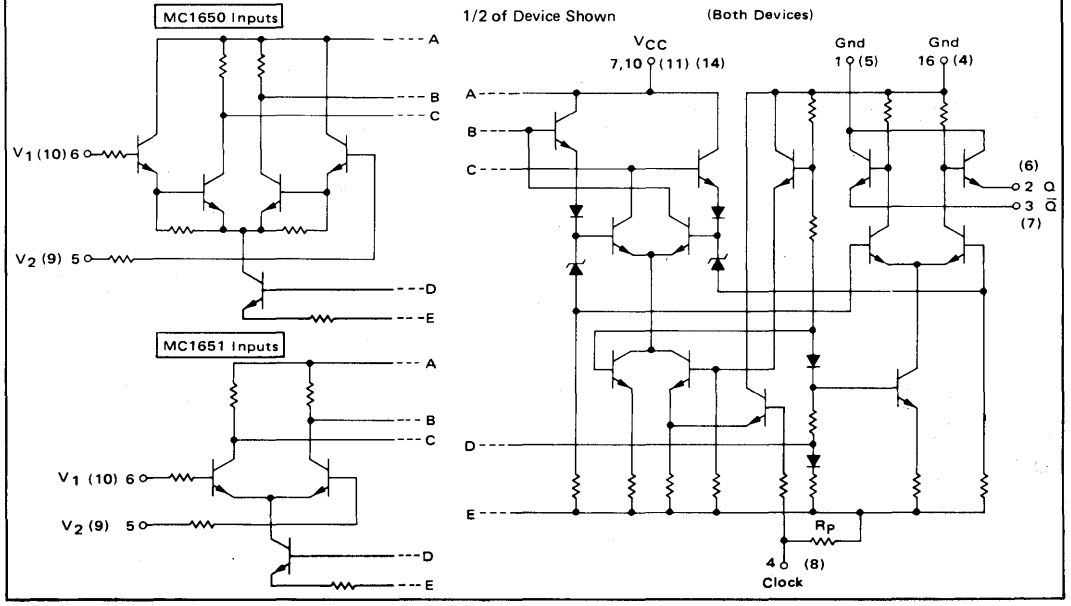
Assessment of the performance differences between the MC1650 and the MC1651 may be based upon the relative behaviors shown in Figures 4 and 7.

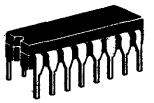
TRUTH TABLE

$\overline{C}$	V_1, V_2	$Q0_{n+1}$	$\overline{Q0}_{n+1}$
H	$V_1 > V_2$	H	L
H	$V_1 < V_2$	L	H
L	ϕ ϕ	$Q0_n$	$\overline{Q0}_n$

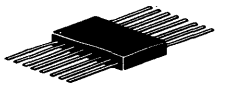
ϕ = Don't Care

CIRCUIT SCHEMATIC
1/2 of Device Shown (Both Devices)





L SUFFIX
CERAMIC PACKAGE
CASE 620



F SUFFIX
CERAMIC PACKAGE
CASE 650

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{A1}	V_{A2}	V_{A3}	V_{A4}	V_{A5}	V_{A6}	V_{CC} ③	V_{EE} ③
-30°C	-0.875	-1.890	-1.180	-1.515	+0.020	-0.020	See Note ④				+5.0	-5.2
+25°C	-0.810	-1.850	-1.095	-1.485	+0.020	-0.020					+5.0	-5.2
+85°C	-0.700	-1.830	-1.025	-1.440	+0.020	-0.020					+5.0	-5.2

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	-30°C Min	-30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{A1}	V_{A2}	V_{A3}	V_{A4}	V_{A5}	V_{A6}	Gnd
Power Supply Drain Current								mAdc											
Positive	I_{CC}	–	–	–	25*	–	–		–	4,13	–	–	6,12	–	–	–	–	–	1,5,11,16
Negative	I_E				55*				4,13	–	–	–	6,12	–	–	–	–	–	1,5,11,16
Input Current	I_{in}							μAdc											
MC1650		–	–	–	10	–	–		4	13	–	–	12	–	6	–	–	–	1,5,11,16
MC1651		–	–	–	40	–	–												
Input Leakage Current	I_R							μAdc											
MC1650		–	–	–	7.0	–	–		4	13	–	–	12	–	–	–	6	–	1,5,11,16
MC1651		–	–	–	10	–	–												
Clock Input Current	I_{inH}	–	–	–	350	–	–	μAdc	4	13	–	–	6,12	–	–	–	–	–	1,5,11,16
Logic "1" Output Voltage	V_{OH}	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc	4,13	–	–	–	6,12	–	–	–	–	–	1,5,11,16
									↓	–	–	–	–	5,11	–	–	–	–	1,6,12,16
										–	–	–	–	–	6,12	5,11	–	–	1,16
										–	–	–	–	–	–	–	5.11	6.12	1,16
										–	–	–	–	6,12	–	–	–	–	1,5,11,16
										–	–	–	5,11	–	–	–	–	–	1,6,12,16
										–	–	–	–	–	5,11	6,12	–	–	1,16
										–	–	–	–	–	–	–	6,12	5,11	1,16
Logic "0" Output Voltage	V_{OL}	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	4,13	–	–	–	–	6,12	–	–	–	–	1,5,11,16
									↓	–	–	–	5,11	–	–	–	–	–	1,6,12,16
										–	–	–	–	–	5,11	6,12	–	–	1,16
										–	–	–	–	–	–	–	6,12	5,11	1,16
										–	–	–	6,12	–	–	–	–	–	1,5,11,16
										–	–	–	–	5,11	–	–	–	–	1,6,12,16
										–	–	–	–	–	6,12	5,11	–	–	1,16
										–	–	–	–	–	–	–	5,11	6,12	1,16
Logic "1" Threshold Voltage ②	V_{OHA}	-1.065	–	-0.980	–	-0.910	–	Vdc		13	4	–	6	–	–	–	–	–	1,5,16
									–	↓	–	4	–	6	–	–	–	–	↓
									–		4	–	–	6	–	–	–	–	
									–		–	4	6	–	–	–	–	–	
Logic "0" Threshold Voltage ②	V_{OLA}	–	-1.630	–	-1.600	–	-1.555	Vdc	–	13	4	–	6	–	–	–	–	–	1,5,16
									–	↓	–	4	–	6	–	–	–	–	↓
									–		4	–	–	6	–	–	–	–	
									–		–	4	6	–	–	–	–	–	

NOTES: ① All data is for 1/2 MC1650 or MC1651, except data marked (*) which refers to the entire package.

② These tests done in order indicated. See Figure 5.

③ Maximum Power Supply Voltages (beyond which device life may be impaired):
$|V_{EE}| + |V_{CC}| \geq 12$ Vdc.

④

All Temperatures	V_{A3}	V_{A4}	V_{A5}	V_{A6}
MC1650	+3.000	+2.980	-2.500	-2.480
MC1651	+2.500	+2.480	-3.000	-2.980

@ Test Temperature	SWITCHING TEST VOLTAGE VALUES (Volts)						
	V_{R1}	V_{R2} V_{R3}	V_X	V_{XX}	V_{CC} (1)	V_{EE} (1)
-30°C	+2.000	See Note (4)	+1.040	+2.00	+7.00	-3.20
+25°C	+2.000		+1.110	+2.00	+7.00	-3.20
+85°C	+2.000		+1.190	+2.00	+7.00	-3.20

Characteristic	Symbol	-30°C Min	-30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit	Conditions (See Figures 1-3)
Switching Times								ns	
Propagation Delay (50% to 50%) V-Input	t_{pd}	2.0	5.0	2.0	5.0	2.0	5.7		V_{R1} to V_2, V_X to Clock, P_1 to V_1, or, V_{R2} to V_2, V_X to Clock, P_2 to V_1, or, V_{R3} to V_2, V_X to Clock, P_3 to V_1.
Clock (2)		2.0	4.7	2.0	4.7	2.0	5.2		V_{R1} to V_2, P_1 to V_1 and P_4 to Clock, or, V_{R1} to V_1, P_1 to V_2 and P_4 to Clock.
Clock Enable (3)	t_{setup}	–	–	2.5	–	–	–	ns	V_{R1} to V_2, P_1 to V_1, P_4 to Clock
Clock Aperture (3)	t_{ap}	–	–	1.5	–	–	–	ns	
Rise Time (10% to 90%)	t+	1.0	3.5	1.0	3.5	1.0	3.8	ns	V_{R1} to V_2, V_X to Clock, P_1 to V_1.
Fall Time (10% to 90%)	t-	1.0	3.0	1.0	3.0	1.0	3.3	ns	

NOTES: (1) Maximum Power Supply Voltages (beyond which device life may be impaired: $|V_{CC}| + |V_{EE}| \geqslant 12$ Vdc.

(2) Unused clock inputs may be tied to ground.

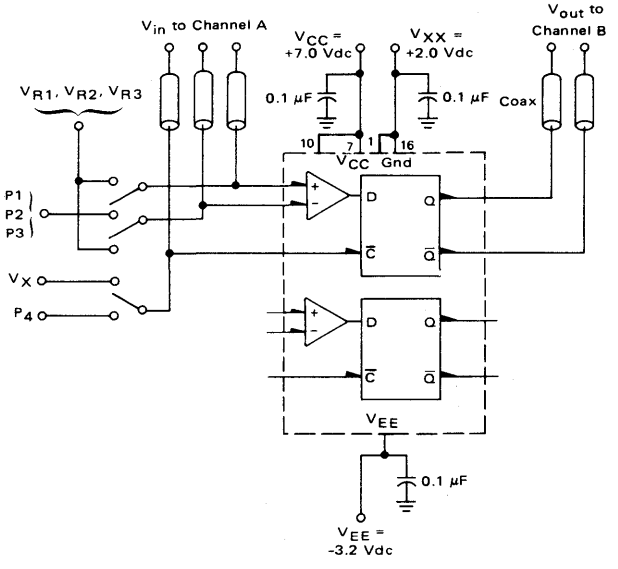
(3) See Figure 3.

(4)

All Temperatures	V_{R2}	V_{R3}
MC1650	+4.900	-0.400
MC1651	+4.400	-0.900

4

FIGURE 1 – SWITCHING TIME TEST CIRCUIT @ 25°C



Note: All power supply and logic levels are shown shifted 2 volts positive.

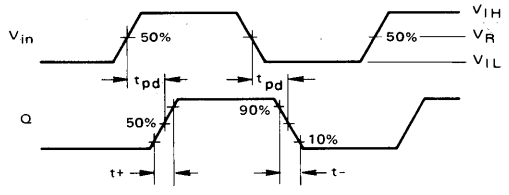
50-ohm termination to ground located in each scope channel input.

All input and output cables to the scope are equal lengths of 50-ohm coaxial cable.

FIGURE 2 – SWITCHING AND PROPAGATION WAVEFORMS @ 25°C

The pulse levels shown are used to check ac parameters over the full common-mode range.

V – Input to Output

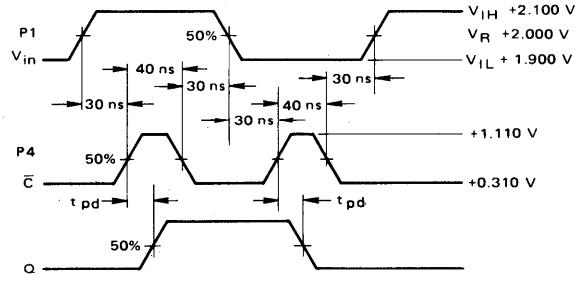


Test pulses: t_+, t_- = 1.5 ±0.2 ns (10% to 90%)
f = 5.0 MHz
50% Duty Cycle

TEST PULSE LEVELS

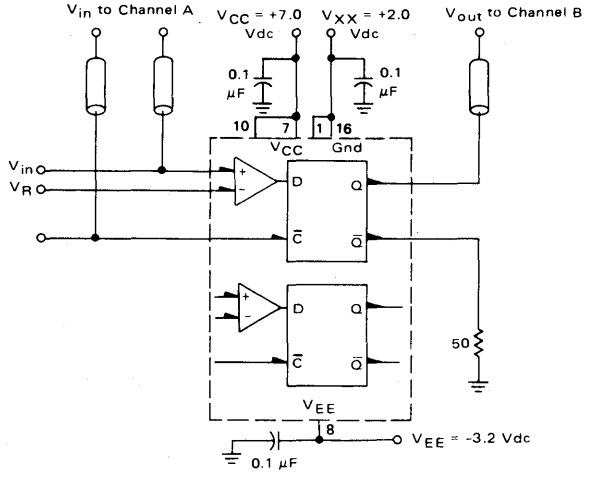
	P1		P2		P3	
	MC1650	MC1651	MC1650	MC1651	MC1650	MC1651
V_{IH}	+2.100 V	+2.100 V	+5.000 V	+4.500 V	-0.300 V	-0.800 V
V_R	+2.000 V	+2.000 V	+4.900 V	+4.400 V	-0.400 V	-0.900 V
V_{IL}	+1.900 V	+1.900 V	+4.800 V	+4.300 V	-0.500 V	-1.000 V

Clock to Output



P4: t_+, t_- = 1.5 ± 0.2 ns.

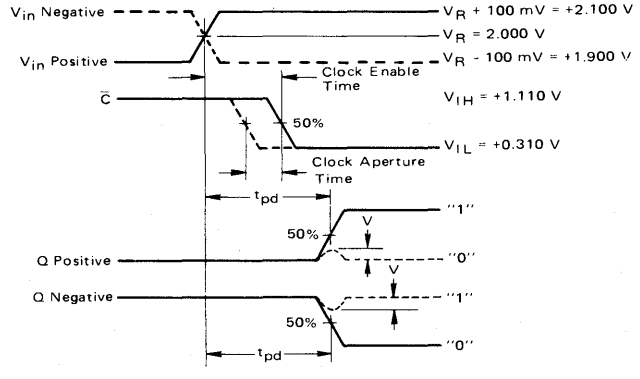
FIGURE 3 – CLOCK ENABLE AND APERTURE TIME TEST CIRCUIT AND WAVEFORMS @ 25°C



50-ohm termination to ground located in each scope channel input.

All input and output cables to the scope are equal lengths of 50-ohm coaxial cable.

Analog Signal Positive and Negative Slew Case



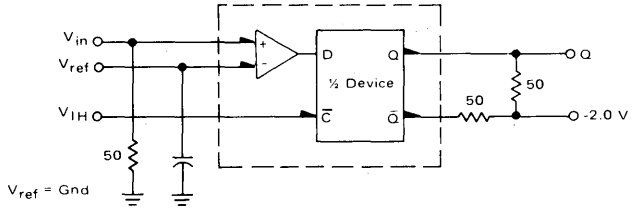
——— Clock enable time = minimum time between analog and clock signal such that output switches, and t_{pd} (analog to Q) is not degraded by more than 200 ps.

– – – – – – Clock aperture time = time difference between clock enable time and time that output does not switch and V is less than 150 mV.

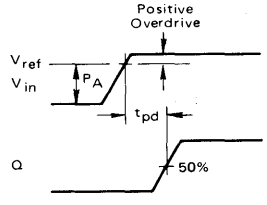
Note: All power supply and logic levels are shown shifted 2 volts positive.

FIGURE 4 – PROPAGATION DELAY (t_{pd}) versus INPUT PULSE AMPLITUDE AND CONSTANT OVERDRIVE

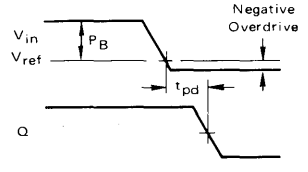
Test Circuit



Positive Pulse Diagram

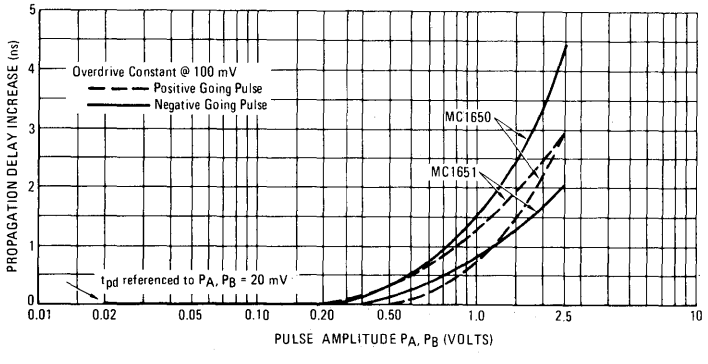


Negative Pulse Diagram



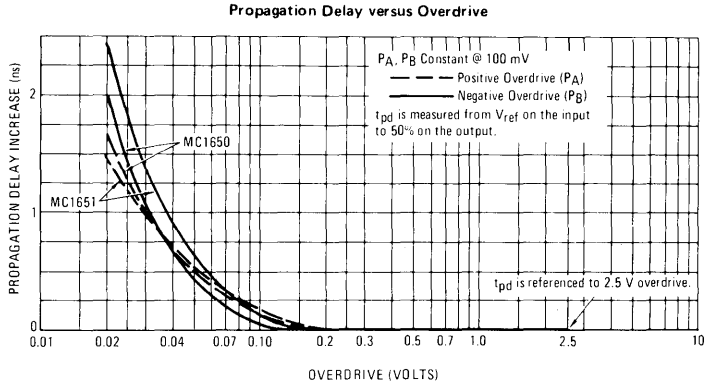
Input switching time is constant at 1.5 ns (10% to 90%).

Propagation Delay versus Pulse Amplitude



(continued)

FIGURE 4 (continued)



4

FIGURE 5 – LOGIC THRESHOLD TESTS (WAVEFORM SEQUENCE DIAGRAM)

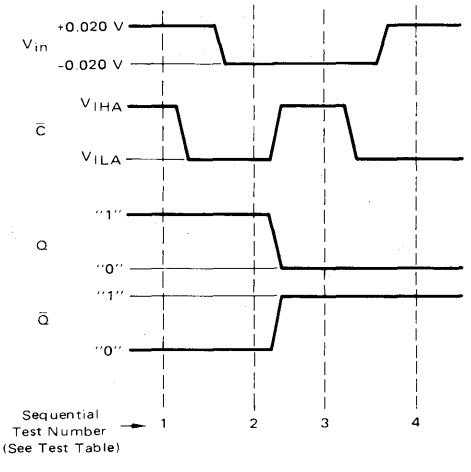
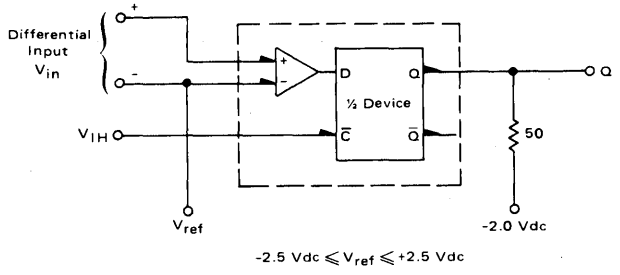


FIGURE 6 – TRANSFER CHARACTERISTICS (Q versus V_{in})

Test Configuration



$-2.5\ \text{Vdc} \leqslant V_{ref} \leqslant +2.5\ \text{Vdc}$

Typical Transfer Curves

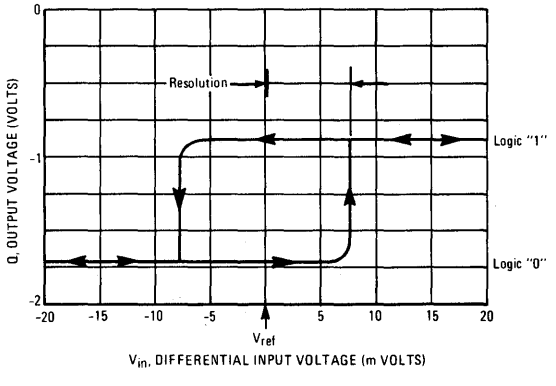
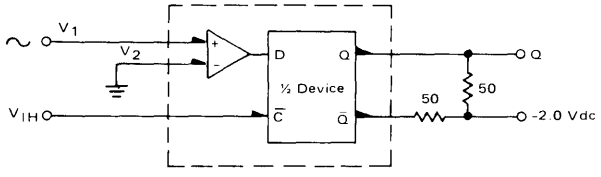
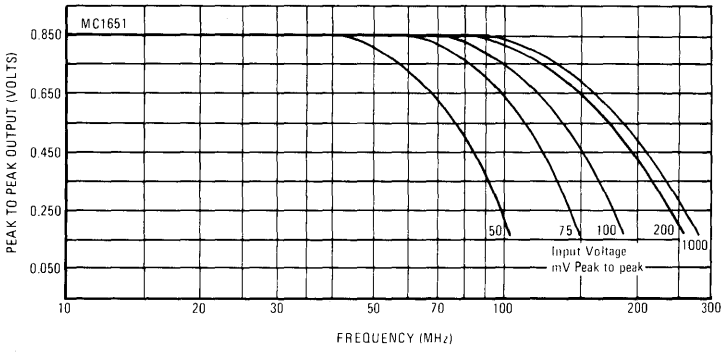


FIGURE 7 – OUTPUT VOLTAGE SWING versus FREQUENCY

(A) Test Circuit



(B) Typical Output Logic Swing versus Frequency



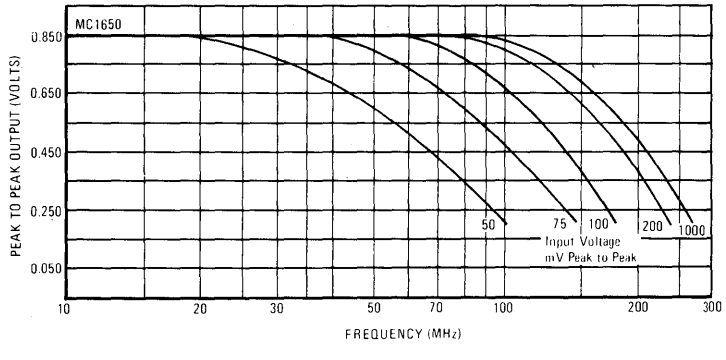
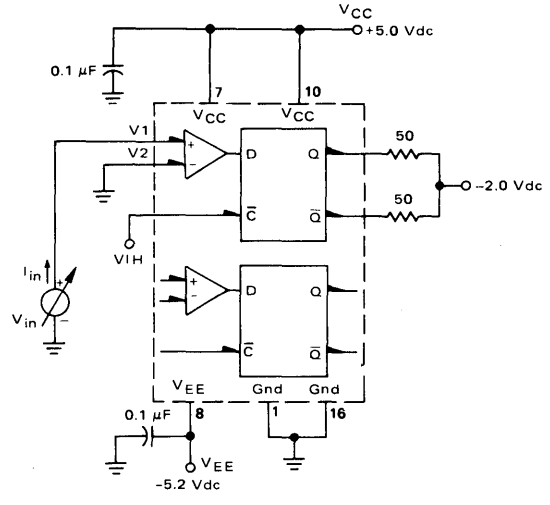
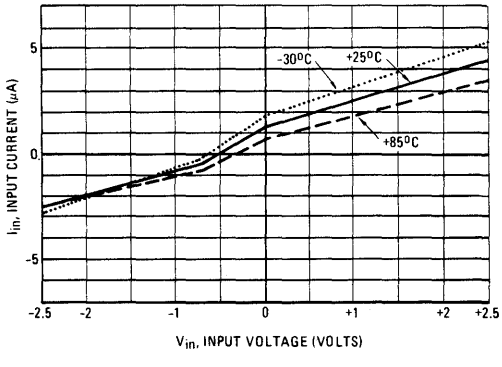


FIGURE 8 – INPUT CURRENT versus INPUT VOLTAGE

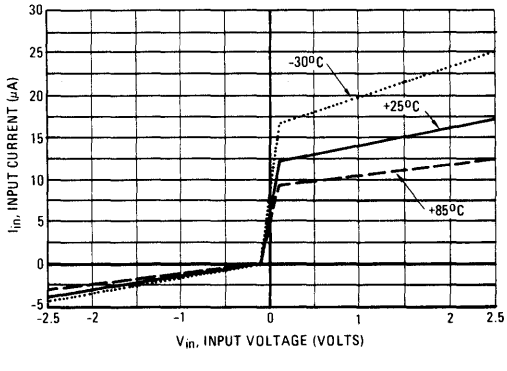
TEST CIRCUIT



Typical MC1650 (Complementary Input Grounded)



Typical MC1651 (Complementary Input Grounded)



MC1654

BINARY COUNTER

TRUTH TABLE

INPUTS							OUTPUTS			
R	S0	S1	S2	S3	C1	C2	Q0	Q1	Q2	Q3
1	0	0	0	0	ϕ	ϕ	0	0	0	0
0	1	1	1	1	ϕ	ϕ	1	1	1	1
0	0	0	0	0	1	ϕ	No Count			
0	0	0	0	0	ϕ	1	No Count			
0	0	0	0	0	••		0	0	0	0
0	0	0	0	0	••		1	0	0	0
0	0	0	0	0	••		0	1	0	0
0	0	0	0	0	••		1	1	0	0
0	0	0	0	0	••		0	0	1	0
0	0	0	0	0	••		1	0	1	0
0	0	0	0	0	••		0	1	1	0
0	0	0	0	0	••		1	1	1	0
0	0	0	0	0	••		0	0	0	1
0	0	0	0	0	••		1	0	0	1
0	0	0	0	0	••		0	1	0	1
0	0	0	0	0	••		1	1	0	1
0	0	0	0	0	••		0	0	1	1
0	0	0	0	0	••		1	0	1	1
0	0	0	0	0	••		0	1	1	1
0	0	0	0	0	••		1	1	1	1

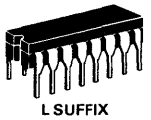
ϕ = Don't Care

•• V_{IL} ⟋ V_{IH} Clock transition from V_{IL} to V_{IH} may be applied to C1 or C2 or both for same effect.

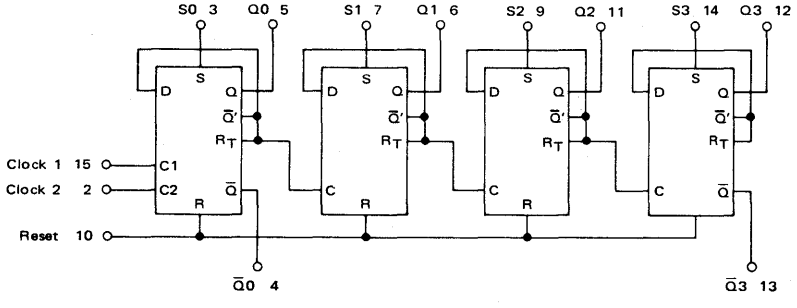
The MC1654 is a four-bit counter capable of divide-by-two, divide-by-four, divide-by-eight, or divide-by-16 functions. When used independently, the divide-by-16 section will toggle at 325 MHz typically. Clock inputs trigger on the positive-going edge of the Clock pulse.

Set and Reset inputs override the Clock, allowing asynchronous "set" or "clear." Individual Set and common Reset inputs are provided, as well as complementary outputs for the first and fourth bits. True outputs are available at all bits.

Power Dissipation = 750 mW typ
f_{Tog} = 325 MHz typ



L SUFFIX
CERAMIC PACKAGE
CASE 620

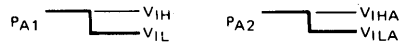


V_{CC} = 1, 16
V_{EE} = 8

ELECTRICAL CHARACTERISTICS

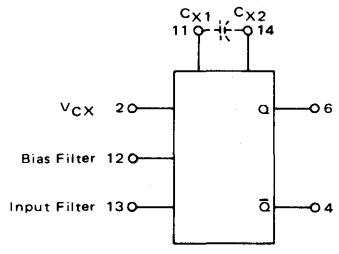
Characteristic	Symbol	-30°C		+25°C		+85°C		Unit
		Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_E	–	–	–	200	–	–	mAdc
Input Current	I_{inH}							mAdc
Reset		–	–	–	1.00	–	–	
Set, Clock		–	–	–	0.60	–	–	
Switching Times								ns
Propagation Delay	t_{pd}							
Clock (Pin 2 or 15 to pins 4, 5)		1.0	2.9	1.0	2.7	1.0	3.1	
Set, Reset		2.0	3.9	2.0	3.7	2.0	4.1	
Rise Time (10% to 90%)	t+	1.0	2.9	1.0	2.7	1.0	3.1	ns
Fall Time (10% to 90%)	t–	1.0	2.8	1.0	2.6	1.0	3.0	ns
Maximum Toggle Frequency	f_{tog}	260	–	300	–	260	–	MHz

(1) For V_{OH}/V_{OL} testing reset all four flip-flops by applying R_{A1} to Reset and apply V_{ILmin} to Set inputs, or set all four flip-flops by applying R_{A1} simultaneously to all Set inputs and apply V_{ILmin} to Reset. For V_{OHA}/V_{OLA} testing follow the same procedure using P_{A2} and V_{ILAmax}.



MC1658

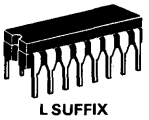
VOLTAGE-CONTROLLED MULTIVIBRATOR



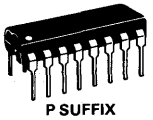
V_{CC1} = Pin 1
V_{CC2} = Pin 5
V_{EE} = Pin 8

The MC1658 is a voltage-controlled multivibrator which provides appropriate level shifting to produce an output compatible with MECL III and MECL 10,000 logic levels. Frequency control is accomplished through the use of voltage-variable current sources which control the slew rate of a single external capacitor.

The bias filter may be used to help eliminate ripple on the output voltage levels at high frequencies and the input filter may be used to decouple noise from the analog input signal.



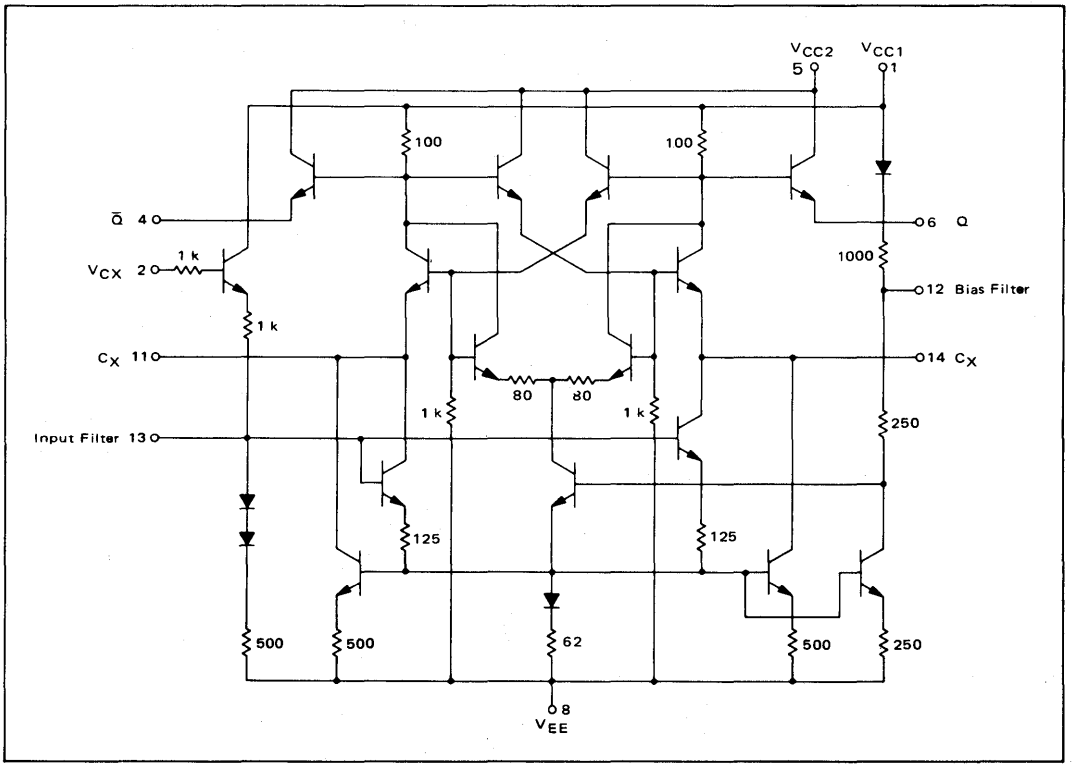
L SUFFIX
CERAMIC PACKAGE
CASE 620



P SUFFIX
PLASTIC PACKAGE
CASE 648

4

FIGURE 1 – CIRCUIT SCHEMATIC



@ Test Temperature	TEST VOLTAGE VALUES Vdc ±1% V_{IH}	V_{IL}	V_3	V_{IHA}	V_{EE}
-30°C	0.0	-2.0	-1.0	+2.0	-5.2
+25°C	0.0	-2.0	-1.0	+2.0	-5.2
+85°C	0.0	-2.0	-1.0	+2.0	-5.2

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	-30°C Min	-30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit	Conditions
Power Supply Drain Current	I_E	–	–	–	32	–	–	mAdc	V_{IH} to V_{CX} Limit applies for (1) or (2)
Input Current	I_{inH}	–	–	–	350	–	–	μAdc	V_{IH} to V_{CX} (1)
"Q" High Output Voltage	V_{OH}	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc	V_3 to V_{CX}. Limits apply for (1) or (2)
"$\bar{Q}$" Low Output Voltage	V_{OL}	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	

AC CHARACTERISTICS

	Symbol	Min	Max	Min	Typ	Max	Min	Max	Unit	Conditions See Figure 2.
Rise Time (10% to 90%)	t+	–	2.7	–	1.6	2.7	–	3.0	ns	V_{IHA} to V_{CX}, C_{X2} (5) from pin 11 to pin 14.
Fall Time (10% to 90%)	t-	–	2.7	–	1.4	2.7	–	3.0	ns	
Oscillator Frequency	f_{osc1}	130	–	130	155	175	110	–	MHz	
	f_{osc2}	–	–	78	90	100	–	–	MHz	V_{IHA} to V_{CX}, CX1 (4) from pin 11 to pin 14.
Tuning Ration Test	TR (3)	–	–	3.1	4.5	–	–	–	–	CX1 (4) from pin 11 to pin 14.

(1) Germanium diode (0.4 drop) forward biased from 11 to 14 (11 —▶|— 14).

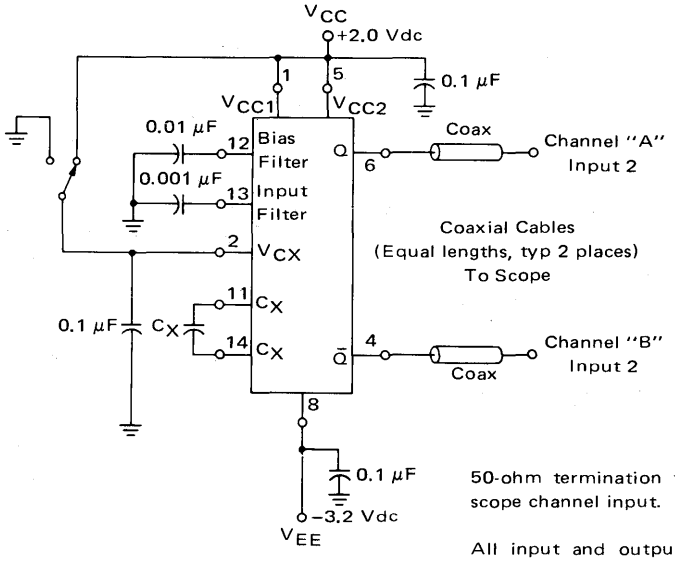
(2) Germanium diode (0.4 drop) forward biased from 14 to 11 (11 —|◀— 14).

(3) $TR = \dfrac{\text{Output frequency at } V_{CX} = \text{Gnd}}{\text{Output frequency at } V_{CX} = -2.0\ V}$

(4) C_{X1} = 10 pF connected from pin 11 to pin 14.

(5) C_{X2} = 5 pF connected from pin 11 to pin 14.

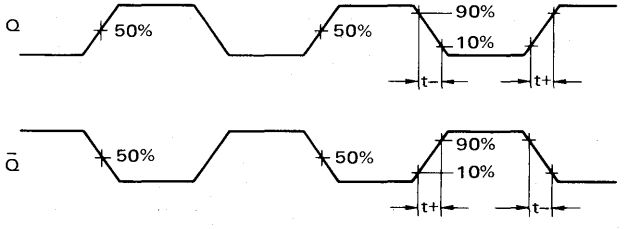
FIGURE 2 – AC TEST CIRCUIT AND WAVEFORMS



50-ohm termination to ground located in each scope channel input.

All input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be < 1/4 inch from TP_{in} to input pin and TP_{out} to output pin.

Note: All power supply and logic levels are shown shifted 2 volts positive.



4

FIGURE 3 – OUTPUT FREQUENCY versus CAPACITANCE FOR VARIOUS VALUES OF INPUT VOLTAGE

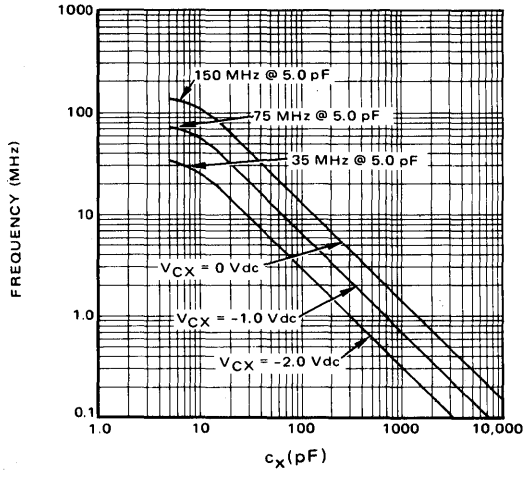
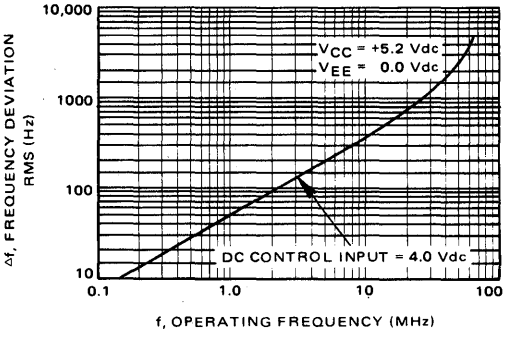
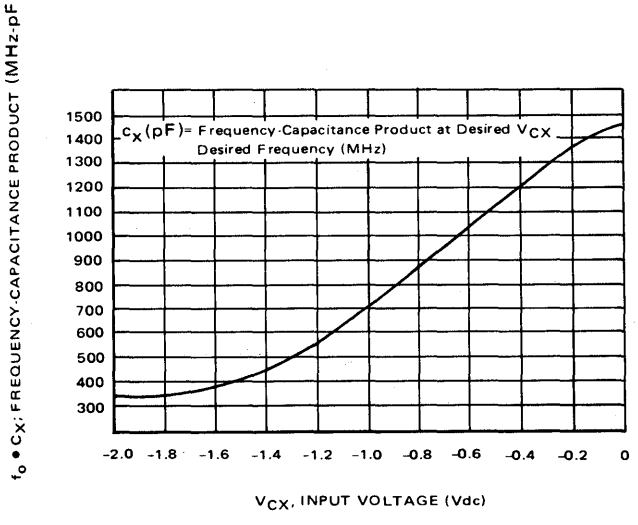


FIGURE 4 – RMS NOISE DEVIATION versus OPERATING FREQUENCY



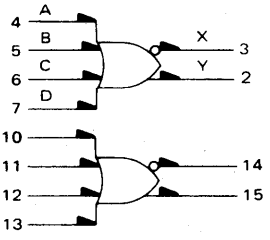
4

FIGURE 5 – FREQUENCY-CAPACITANCE PRODUCT versus CONTROL VOLTAGE (V_{CX})



MC1660

DUAL 4-INPUT GATE



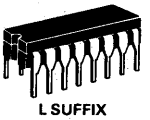
$X = \overline{A + B + C + D}$

$Y = A + B + C + D$

V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

t_{pd} = 0.9 ns typ (510-ohm load)
= 1.1 ns typ (50-ohm load)

P_D = 120 mW typ/pkg (No load)
Full Load Current, I_L = −25 mAdc max



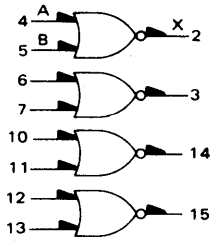
L SUFFIX
CERAMIC PACKAGE
CASE 620

Numbers at ends of terminals denote pin numbers for L package

Characteristic	Symbol	-30°C		+25°C		+85°C		Unit
		Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_E	–	–	–	28	–	–	mAdc
Input Current	I_{inH}	–	–	–	350	–	–	μAdc
Switching Times								ns
Propagation Delay	t^{+-}	0.6	1.8	0.6	1.7	0.6	1.9	
	t^{-+}	0.6	1.6	0.6	1.5	0.6	1.7	
Rise Time, Fall Time (10% to 90%)	t^+, t^-	0.6	2.2	0.6	2.1	0.6	2.3	ns

MC1662

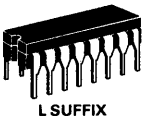
QUAD 2-INPUT NOR GATE



$X = \overline{A + B}$

V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

t_{pd} = 0.9 ns typ (510-ohm load)
= 1.1 ns typ (50-ohm load)
P_D = 240 mW typ/pkg (No load)
Full Load Current, I_L = -25 mAdc max



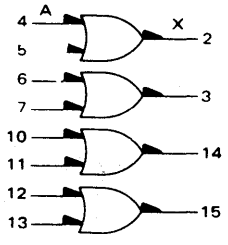
L SUFFIX
CERAMIC PACKAGE
CASE 620

Number at end of terminals denotes pin number of L package.

Characteristic	Symbol	-30°C		+25°C		+85°C		Unit
		Min	Max	Max	Max	Min	Max	
Power Supply Drain Current	I_E	–	–	–	56	–	–	mAdc
Input Current	I_{inH}	–	–	–	350	–	–	μAdc
Switching Times								ns
Propagation Delay	t^{-+}	0.6	1.6	0.6	1.5	0.6	1.7	
	t^{+-}	0.6	1.8	0.6	1.7	0.6	1.9	
Rise Time, Fall Time (10% to 90%)	t^+, t^-	0.6	2.2	0.6	2.1	0.6	2.3	ns

MC1664

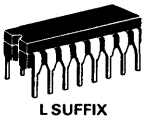
QUAD 2-INPUT OR GATE



X = A + B

V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

t_{pd} = 0.9 ns typ (510-ohm load)
= 1.1 ns typ (50-ohm load)
P_D = 240 mW typ/pkg (No load)
Full Load Current, I_L = -25 mAdc max



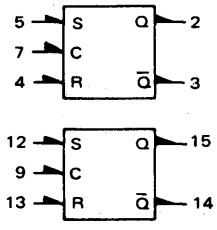
L SUFFIX
CERAMIC PACKAGE
CASE 620

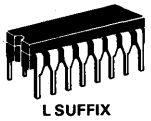
Number at end of terminals denotes pin number of L package.

Characteristic	Symbol	-30°C		+25°C		+85°C		Unit
		Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_E	–	–	–	56	–	–	mAdc
Input Current	I_{inH}	–	–	–	350	–	–	μAdc
Switching Times								ns
Propagation Delay	t^{++}	0.6	1.6	0.6	1.5	0.6	1.7	
	t^{--}	0.6	1.8	0.6	1.7	0.6	1.9	
Rise Time, Fall Time (10% to 90%)	t^+,t^-	0.6	2.2	0.6	2.1	0.6	2.3	ns

MC1666

DUAL CLOCKED R-S FLIP-FLOP





L SUFFIX
CERAMIC PACKAGE
CASE 620

TRUTH TABLE

S	R	C	Q_{n+1}
ϕ	ϕ	0	Q_n
0	0	1	Q_n
1	0	1	1
0	1	1	0
1	1	1	N.D.

ϕ = Don't Care
N.D. = Not Defined

t_{pd} = 1.6 ns typ (510-ohm load)
= 1.8 ns typ (50-ohm load)
P_D = 220 mW typ/pkg (No Load)

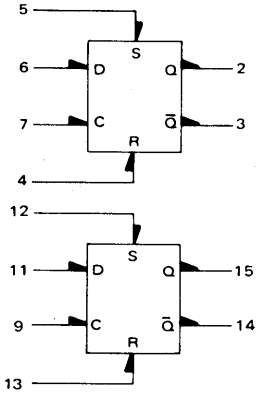
V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

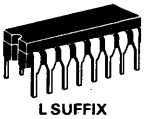
Number at end of terminal denotes pin number for L package

Characteristic	Symbol	−30°C Min	−30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit
Power Supply Drain Current	I_E	–	–	–	55	–	–	mAdc
Input Current	I_{inH}							μAdc
Set, Reset		–	–	–	370	–	–	
Clock		–	–	–	225	–	–	
Switching Times								ns
Propagation Delay	t_{pd}							
Clock		1.0	2.7	1.0	2.5	1.1	2.8	
Set, Reset		1.0	2.5	1.1	2.3	1.1	2.7	
Rise Time (10% to 90%)	t+	0.8	2.8	0.8	2.5	0.9	2.9	ns
Fall Time (10% to 90%)	t−	0.5	2.4	0.5	2.2	0.5	2.6	ns

MC1668

DUAL CLOCKED LATCH





L SUFFIX
CERAMIC PACKAGE
CASE 620

TRUTH TABLE

S	R	D	C	Q_{n+1}
0	0	φ	0	Q_n
1	0	φ	0	1
0	1	φ	0	0
1	1	φ	0	**
φ	φ	0	1	0
φ	φ	1	1	1

**Output state not defined φ = Don't Care

V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

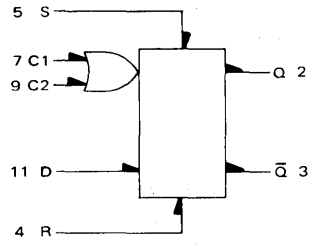
t_{pd} = 1.6 ns typ (510-ohm load)
= 1.8 ns typ (50-ohm load)
P_D = 220 mW typ/pkg (No load)

Number at end of terminal denotes pin number for L package

Characteristic	Symbol	−30°C Min	−30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit
Power Supply Drain Current	I_E	–	–	–	55	–	–	mAdc
Input Current	I_{inH}							μAdc
Data, Set, Reset		–	–	–	370	–	–	
Clock		–	–	–	225	–	–	
Switching Times								ns
Propagation Delay	t_{pd}							
Clock		1.0	2.7	1.0	2.5	1.1	2.8	
Set, Reset		1.0	2.5	1.0	2.3	1.1	2.7	
Rise Time (10% to 90%)	t+	0.8	2.8	0.9	2.5	0.9	2.9	ns
Fall Time (10% to 90%)	t-	0.5	2.4	0.5	2.2	0.5	2.6	ns

MC1670

MASTER-SLAVE FLIP-FLOP



TRUTH TABLE

R	S	D	C	Q_{n+1}
L	H	ϕ	ϕ	H
H	L	ϕ	ϕ	L
H	H	ϕ	ϕ	N.D.
L	L	L	L	Q_n
L	L	L	↗	L
L	L	L	H	Q_n
L	L	H	L	Q_n
L	L	H	↗	H
L	L	H	H	Q_n

ϕ = Don't Care
ND = Not Defined
C = C1 + C2

V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

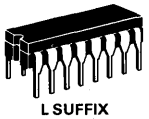
Master slave construction renders the MC1670 relatively insensitive to the shape of the clock waveform, since only the voltage levels at the clock inputs control the transfer of information from data input (D) to output.

When both clock inputs (C1 and C2) are in the low state, the data input affects only the "Master" portion of the flip-flop. The data present in the "Master" is transferred to the "Slave" when clock inputs (C1 "OR" C2) are taken from a low to a high level. In other words, the output state of the flip-flop changes on the positive transition of the clock pulse.

While either C1 "OR" C2 is in the high state, the "Master" (and data input) is disabled.

Asynchronous Set (S) and Reset (R) override Clock (C) and Data (D) inputs.

Power Dissipation = 220 mW typical (No Load)
f_{Tog} = 350 MHz typ



L SUFFIX
CERAMIC PACKAGE
CASE 620

Number at end of terminal denotes pin number for L package

Characteristic	Symbol	−30°C Min	−30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit
Power Supply Drain Current	I_E	–	–	–	48	–	–	mAdc
Input Current	I_{inH}							μAdc
Set, Reset		–	–	–	550	–	–	
Clock		–	–	–	250	–	–	
Data		–	–	–	270	–	–	
Switching Times								ns
Propagation Delay	t_{pd}	1.0	2.7	1.1	2.5	1.1	2.9	
Rise Time (10% to 90%)	t+	0.9	2.7	1.0	2.5	1.0	2.9	ns
Fall Time (10% to 90%)	t−	0.5	2.1	0.6	1.9	0.6	2.3	ns
Setup Time	$t_{S"1"}$	–	–	0.4	–	–	–	ns
	$t_{S"0"}$	–	–	0.5	–	–	–	
Hold Time	$t_{H"1"}$	–	–	0.3	–	–	–	ns
	$t_{H"0"}$	–	–	0.5	–	–	–	
Toggle Frequency	f_{Tog}	270	–	300	–	270	–	MHz

FIGURE 1 – TOGGLE FREQUENCY WAVEFORMS

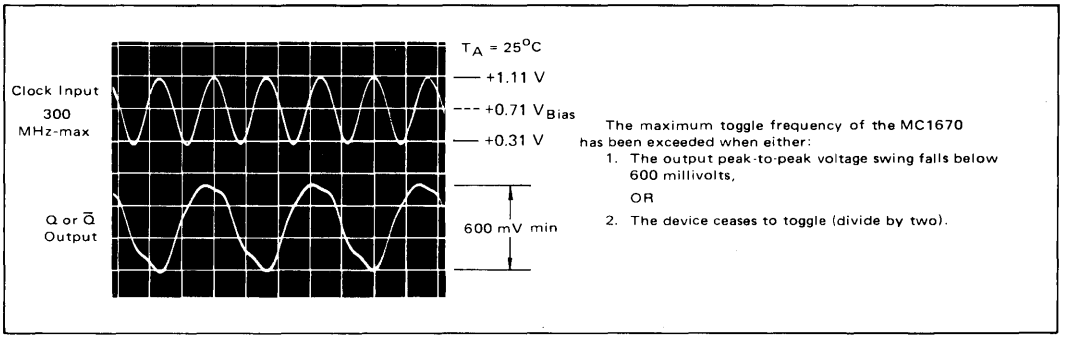


FIGURE 2 – MAXIMUM TOGGLE FREQUENCY (TYPICAL)

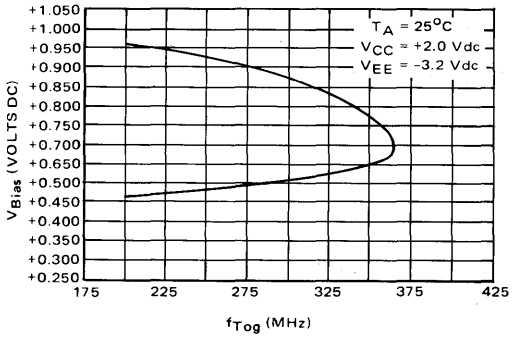
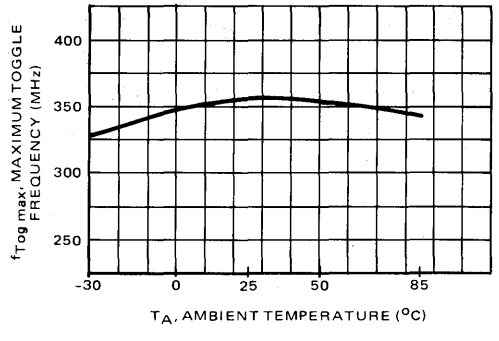


Figure 2 illustrates the variation in toggle frequency with the dc offset voltage (V_{Bias}) of the input clock signal.

Figures 4 and 5 illustrate minimum clock pulse width recommended for reliable operation of the MC1670.

4

FIGURE 3 – TYPICAL MAXIMUM TOGGLE FREQUENCY versus TEMPERATURE



Temperature	-30°C	+25°C	+85°C
V_{Bias}	+0.660 Vdc	+0.710 Vdc	+0.765 Vdc

Note: All power supply and logic levels are shown shifted 2 volts positive.

FIGURE 4 – MINIMUM "DOWN TIME" TO CLOCK
OUTPUT LOAD = 50Ω

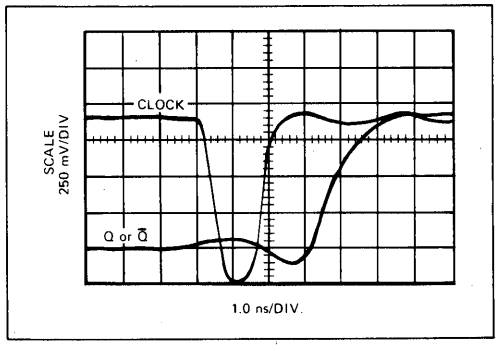
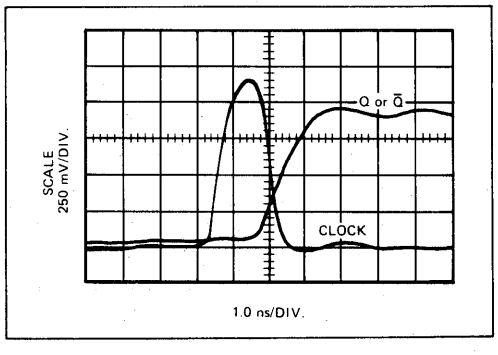
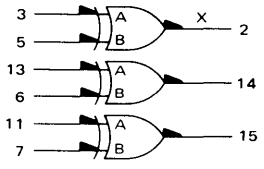


FIGURE 5 – MINIMUM "UP TIME" TO CLOCK
OUTPUT LOAD = 50Ω

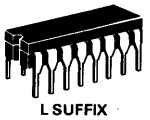


MC1672

TRIPLE 2-INPUT EXCLUSIVE-OR GATE



$X = A \bullet \overline{B} + \overline{A} \bullet B$



L SUFFIX
CERAMIC PACKAGE
CASE 620

V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

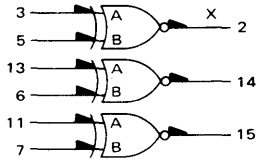
t_{pd} = 1.1 ns typ (510-ohm load)
= 1.3 ns typ (50-ohm load)
P_D = 220 mW typ/pkg
Full Load Current, I_L = −25 mAdc max

Number at end of terminal denotes pin number for L package.

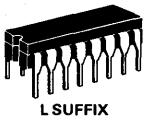
Characteristic	Symbol	−30°C Min	−30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit
Power Supply Drain Current	I_E	–	–	–	55	–	–	mAdc
Input Current								μAdc
A Inputs	I_{inH}	–	–	–	350	–	–	
B Inputs	I_{inH}	–	–	–	270	–	–	
Switching Times								ns
Propagation Delay A Inputs	t++,t−+	–	2.0	–	1.8	–	2.3	
	t+−,t−−	–	2.1	–	1.9	–	2.4	
Propagation Delay B Inputs	t++,t−+	–	2.5	–	2.3	–	2.8	
	t+−,t−−	–	2.5	–	2.3	–	2.8	
Rise Time (10% to 90%)	t+	–	2.7	–	2.5	–	2.9	ns
Fall Time (10% to 90%)	t−	–	2.4	–	2.2	–	2.6	ns

MC1674

TRIPLE 2-INPUT EXCLUSIVE-NOR GATE



$X = \overline{A} \bullet \overline{B} + A \bullet B$



L SUFFIX
CERAMIC PACKAGE
CASE 620

V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

t_{pd} = 1.1 ns typ (510-ohm load)
= 1.3 ns typ (50-ohm load)
P_D = 220 mW typ/pkg
Full Load Current, I_L = −25 mAdc max

Number at end of terminal denotes pin number for L package.

Characteristic		Symbol	−30°C Min	−30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit
Power Supply Drain Current		I_E	–	–	–	55	–	–	mAdc
Input Current									μAdc
	A Inputs	I_{inH}	–	–	–	350	–	–	
	B Inputs	I_{inH}	–	–	–	270	–	–	
Switching Times									ns
Propagation Delay	A Inputs	t++,t−+	–	2.0	–	1.8	–	2.3	
		t+−,t−−	–	2.1	–	1.9	–	2.4	
	B Inputs	t++,t−+	–	2.5	–	2.3	–	2.8	
		t+−,t−−	–	2.5	–	2.3	–	2.8	
Rise Time (10% to 90%)		t+	–	2.7	–	2.5	–	2.9	ns
Fall Time (10% to 90%)		t−	–	2.4	–	2.2	–	2.6	ns

MC1678

BI-QUINARY COUNTER

The MC1678 is a four-bit counter capable of divide-by-two, divide-by-five, or divide-by-10 functions. When used independently, the divide-by-two section will toggle at 350 MHz typically, while the divide-by-five section will toggle at 325 MHz typically. Clock inputs trigger on the positive going edge of the clock pulse.

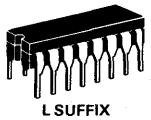
Set and Reset inputs override the clock, allowing asynchronous "set" or "clear". Individual Set and common Reset inputs are provided, as well as complementary outputs for the first and fourth bits. True outputs are available at all bits.

DC Input Loading Factor R = 2.40
C1 = 0.77
C2 = 1.23
S = 1.00

DC Output Loading Factor = 70

Power Dissipation = 750 mW typ

f_{Tog} = 350 MHz typ



L SUFFIX
CERAMIC PACKAGE
CASE 620

4

COUNTER TRUTH TABLES

BCD
(Clock connected to C1 and $\bar{Q}0$ connected to C2)

COUNT	Q0	Q1	Q2	Q3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H

BI-QUINARY
(Clock connected to C2 and $\bar{Q}3$ connected to C1)

COUNT	Q1	Q2	Q3	Q0
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	L	L	L	H
6	H	L	L	H
7	L	H	L	H
8	H	H	L	H
9	L	L	H	H

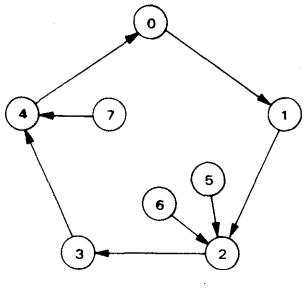
R-S

C	R	S	Q_{n+1}
ϕ	L	L	Q_n
ϕ	H	L	L
ϕ	L	H	H
ϕ	H	H	ND

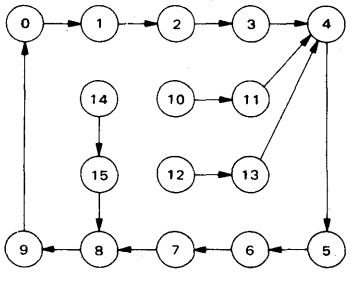
ϕ = Don't Care
ND = Not Defined

COUNTER STATE DIAGRAM – POSITIVE LOGIC

Clock connected to C2



$\bar{Q}0$ connected to C2



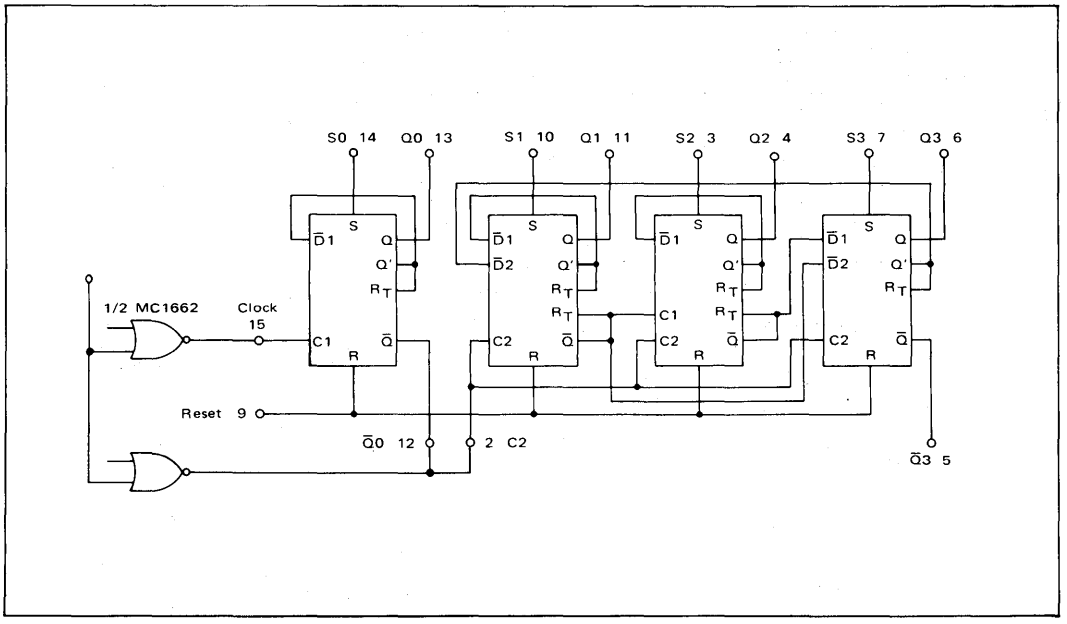
ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	−30°C		+25°C		+85°C		Unit
		Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_E	–	–	–	200	–	–	mAdc
Input Current	I_{inH}							mAdc
Reset		–	–	–	1.00	–	–	
C2		–	–	–	0.70	–	–	
Set, Clock		–	–	–	0.45	–	–	
Switching Times								ns
Propagation Delay	t_{pd}							
Clock to $\overline{Q}0$, Q0		1.0	2.9	1.0	2.7	1.0	3.1	
C2 to Q1, Q2, Q3, $\overline{Q}3$		1.0	3.2	1.0	3.0	1.0	3.4	
Set, Reset		2.0	3.9	2.0	3.7	2.0	4.1	
Rise Time (10% to 90%)	t+	1.0	2.9	1.0	2.7	1.0	3.1	ns
Fall Time (10% to 90%)	t−	1.0	2.8	1.0	2.6	1.0	3.0	ns
Toggle Frequency	f_{Tog}							MHz
Q0		260	–	300	–	260	–	
Q3		250	–	275	–	250	–	

4

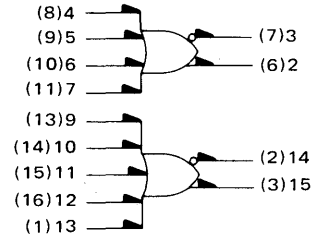
APPLICATIONS INFORMATION

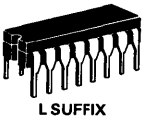
With the addition of a single gate package, the MC1678 will count in a fully synchronous mode, as shown below.



MC1688

DUAL 4-5-INPUT OR/NOR GATE

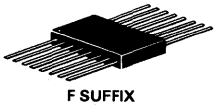




L SUFFIX
CERAMIC PACKAGE
CASE 620

V_{CC1} = Pin 1(5)
V_{CC2} = Pin 16(4)
V_{EE} = Pin 8(12)

t_{pd} = 0.8 ns typ
P_D = 125 mW typ/pkg (No Load)
Output Rise and Fall Times
(10% to 90%) 1.1 ns



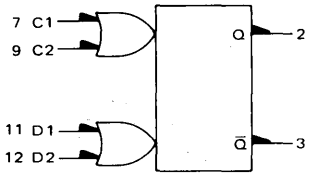
F SUFFIX
CERAMIC PACKAGE
CASE 650

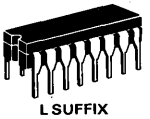
Number at end of terminal denotes pin number for L package
Number in parenthesis denotes pin number for F package

Characteristic	Symbol	−30°C		+25°C		+85°C		Unit
		Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_E	–	–	–	28	–	–	mAdc
Input Current	I_{inH}	–	–	–	350	–	–	μAdc
Switching Times								ns
Propagation Delay	t_{pd}	0.5	1.5	0.5	1.3	0.5	1.5	
Rise Time, Fall Time (10% to 90%)	t+,t−	0.5	1.6	0.5	1.4	0.5	1.6	ns

MC1690

UHF PRESCALER
TYPE D FLIP-FLOP





L SUFFIX
CERAMIC PACKAGE
CASE 620

4

TRUTH TABLE

C	D	Q_{n+1}
L	ϕ	Q_n
H	ϕ	Q_n
⎍	L	L
⎍	H	H

C = C1 + C2 ϕ = Don't Care
D = D1 + D2

V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

P_D = 200 mW typ/pkg (No Load)
f_{Tog} = 500 MHz min

Number at end of terminal denotes pin number for L package

Characteristic	Symbol	-30°C		+25°C			+85°C		Unit
		Min	Max	Min	Typ	Max	Min	Max	
Power Supply Drain Current	I_E	–	–	–		59	–	–	mAdc
Input Current	I_{inH}								μAdc
Pins 7,9		–	–	–		250	–	–	
Pins 11,12		–	–	–		270	–	–	
Switching Times				Min	Typ	Max			ns
Propagation Delay	t_{pd}	–	–	–	1.5	–	–	–	
Rise Time, Fall Time (10% to 90%)	t+,t–	–	–	–	1.3	–	–	–	ns
Setup Time	t_{setup}	–	–	–	0.3	–	–	–	ns
Hold Time	t_{hold}	–	–	–	0.3	–	–	–	
Toggle Frequency	f_{Tog}	500	–	500	540	–	500	–	MHz

FIGURE 1 – TOGGLE FREQUENCY TEST CIRCUIT

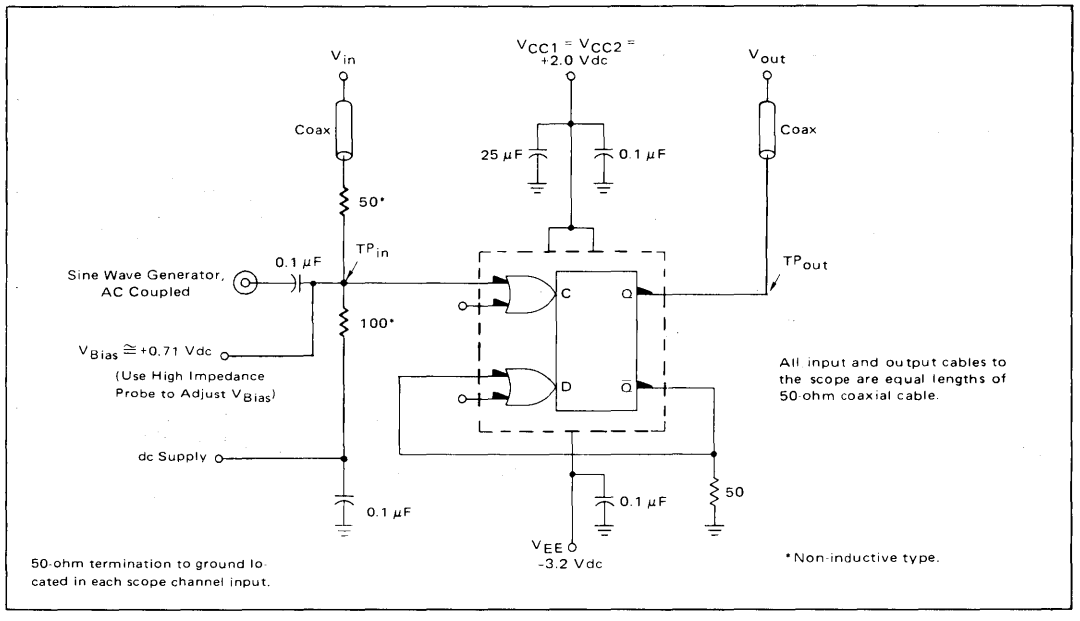
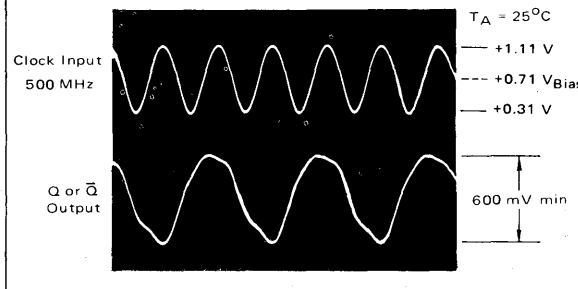


FIGURE 2 – TOGGLE FREQUENCY WAVEFORMS



The maximum toggle frequency of the MC1690 has been exceeded when either:

1. The output peak-to-peak voltage swing falls below 600 millivolts,

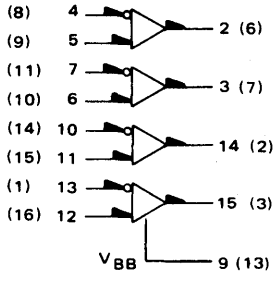
   OR

2. The device ceases to toggle (divide by two).

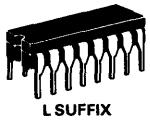
Note: All power supply and logic levels are shown shifted 2 volts positive.

MC1692

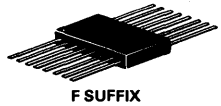
QUAD LINE RECEIVER



V_{CC1} = Pin 1 (5)
V_{CC2} = Pin 16 (4)
V_{EE} = Pin 8 (12)



L SUFFIX
CERAMIC PACKAGE
CASE 620



F SUFFIX
CERAMIC PACKAGE
CASE 650

t_{pd} = 0.9 ns typ (510-ohm load)
= 1.1 ns typ (50-ohm load)

P_D = 220 mW typ/pkg (No Load)
Full Load Current, I_L = -25 mAdc max

Numbers at ends of terminals denote pin numbers for L package
Numbers in parenthesis denote pin numbers for F package

Characteristic	Symbol	-30°C		+25°C		+85°C		Unit
		Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_E	–	–	–	50	–	–	mAdc
Input Current	I_{in}	–	–	–	250	–	–	μAdc
Input Leakage Current	I_R	–	–	–	100	–	–	μAdc
Reference Voltage	V_{BB}	- 1.375	-1.275	-1.35	-1.25	-1.30	-1.20	Vdc
Switching Times								ns
Propagation Delay	t^{-+}	0.6	1.6	0.6	1.5	0.6	1.7	
	t^{+-}	0.6	1.8	0.6	1.7	0.6	1.9	
Rise Time, Fall Time (10% to 90%)	t^+,t^-	0.6	2.2	0.6	2.1	0.6	2.3	ns

APPLICATION INFORMATION

The MC1692 quad line receiver is used primarily to receive data from balanced twisted pair lines, as indicated in Figure 1. The line is driven with a MC1660 OR/NOR gate. The MC1660 is terminated with 50 ohm resistors to -2.0 volts. At the end of the twisted pair a 100 ohm termination resistor is placed across the differential line receiver inputs of the MC1692. Illustrated in Figure 2 is the sending and receiving waveforms at a data rate of 400 megabits per second over an 18 foot twisted pair cable. The waveform picture of Figure 3 shows a 5 nanosecond pulse being propagated down the 18 foot line. The delay time for the line is 1.68 ns/foot.

The MC1692 may also be applied as a high frequency schmitt trigger as illustrated in Figure 4. This circuit has been used in excess of 200 MHz. The MC1692 when loaded into 50 ohms will produce an output rising edge of about 1.5 nanoseconds.

FIGURE 1 – LINE DRIVER/RECEIVER

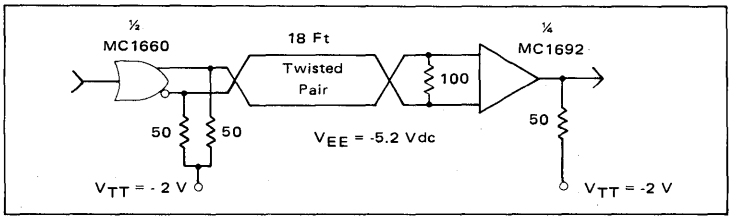


FIGURE 2 – 400 MBS WAVEFORMS

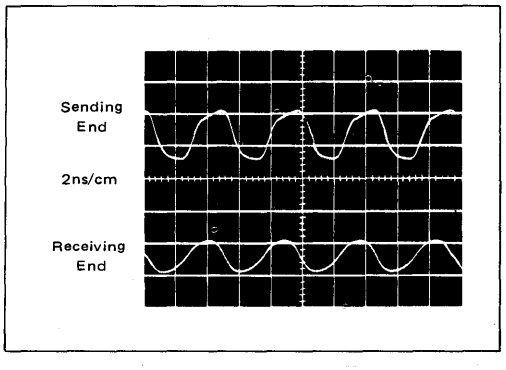
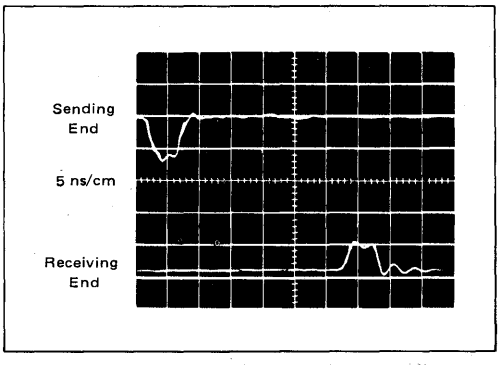


FIGURE 3 – PULSE PROPAGATION WAVEFORMS



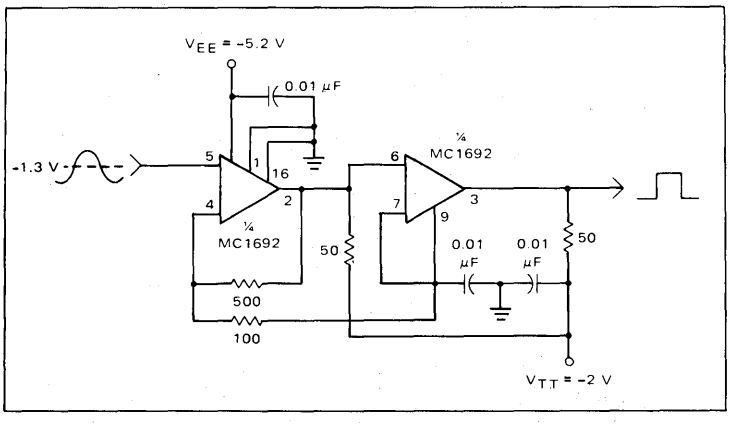


FIGURE 4 – 200 MHz SCHMITT TRIGGER

MC1694

4-BIT SHIFT REGISTER

FLIP-FLOP TRUTH TABLE

Inputs				Output
D	C	R	S	Q_n
0	0	0	0	Q_{n-1}
0	0	0	1	1
0	0	1	0	0
0	0	1	1	*
0	1	0	0	0
0	1	0	1	1
0	1	1	0	0
0	1	1	1	*
1	0	0	0	Q_{n-1}
1	0	0	1	1
1	0	1	0	0
1	0	1	1	*
1	1	0	0	1
1	1	0	1	1
1	1	1	0	0
1	1	1	1	*

*Output State Undefined

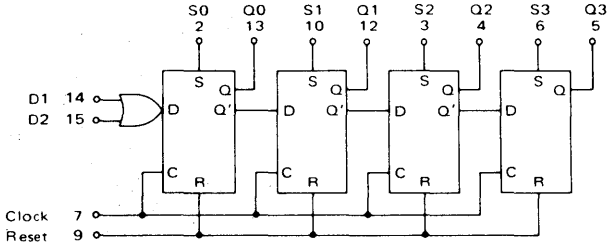
V_{CC1} = 1
V_{CC2} = 16
V_{EE} = 8

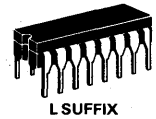
The MC1694 is a 4-Bit register capable of shift rates up to 325 MHz (typical) in the shift-right mode, accepting serial data at either data input D1 or D2. A master reset and individual set inputs override the clock allowing asynchronous entry of information.

DC Input Loading Factors
Reset = 2.5 Set = 1.0
Clock = 1.6 Data = 0.9

DC Output Loading Factor = 70

Total Power Dissipation = 750 mW typ/pkg
Shift Frequency = 325 MHz typ





L SUFFIX
CERAMIC PACKAGE
CASE 620

Characteristic	Symbol	−30°C Min	−30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit
Power Supply Drain Current	I_E	–	–	–	200	–	–	mAdc
Input Current	I_{inH}							mAdc
Pin 9		–	–	–	1.0	–	–	
Pin 7		–	–	–	0.75	–	–	
Pins 2,3,6,10		–	–	–	0.6	–	–	
Pins 14,15		–	–	–	0.5	–	–	
Switching Times								ns
Propagation Delay	t_{pd}							
Clock		1.0	3.2	1.0	3.0	1.0	3.4	
Set, Reset		2.0	3.9	2.0	3.7	2.0	4.1	
Rise Time (10% to 90%)	t+	1.0	2.9	1.0	2.7	1.0	3.1	ns
Fall Time (10% to 90%)	t−	1.0	2.8	1.0	2.6	1.0	3.0	ns
Shift Rate		240	–	275	–	250	–	MHz

MC1697

1-GHz DIVIDE-BY-FOUR PRESCALER

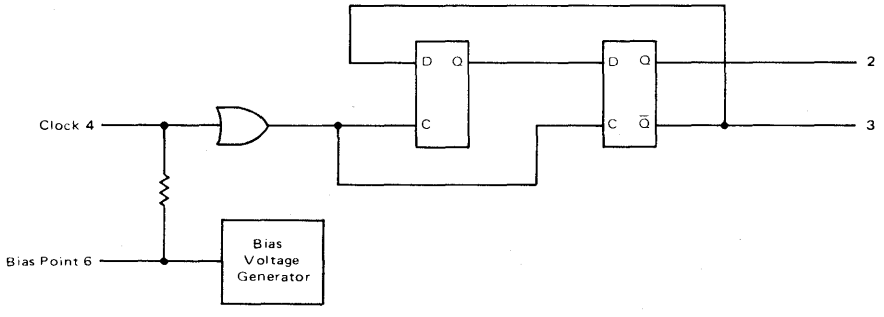
The MC1697 is a divide-by-four gigahertz prescaler in an 8 pin package. The clock input requires an ac coupled driving signal of 800 mV amplitude (typical). The clock toggles two divide-by-two stages, and the complementary outputs (50% duty cycle) are taken from the second stage.

The complementary outputs are capable of driving 50-ohm lines.

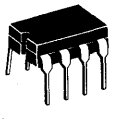
Pin 6 is available for connection of a decoupling capacitor to ground. This capacitor stabilizes the reference point which is internally coupled to the clock input.

V_{CC1} = Pin 1
V_{CC2} = Pin 8
V_{EE} = Pin 5

Power Dissipation = 320 mW Typ/Pkg
(No Load — 7.0 V Supply)

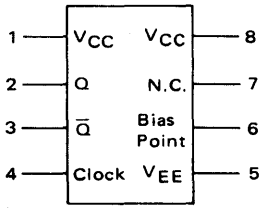


P SUFFIX
PLASTIC PACKAGE
CASE 626



L SUFFIX
CERAMIC PACKAGE
CASE 693

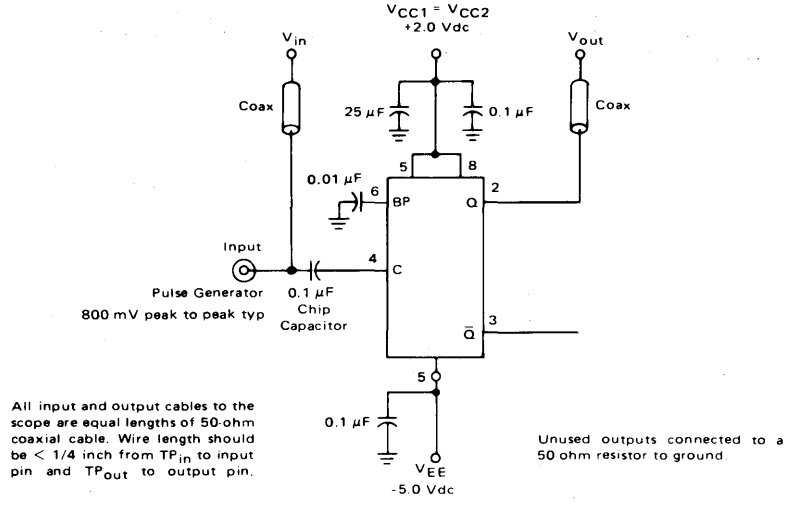
PIN ASSIGNMENT



ELECTRICAL CHARACTERISTICS

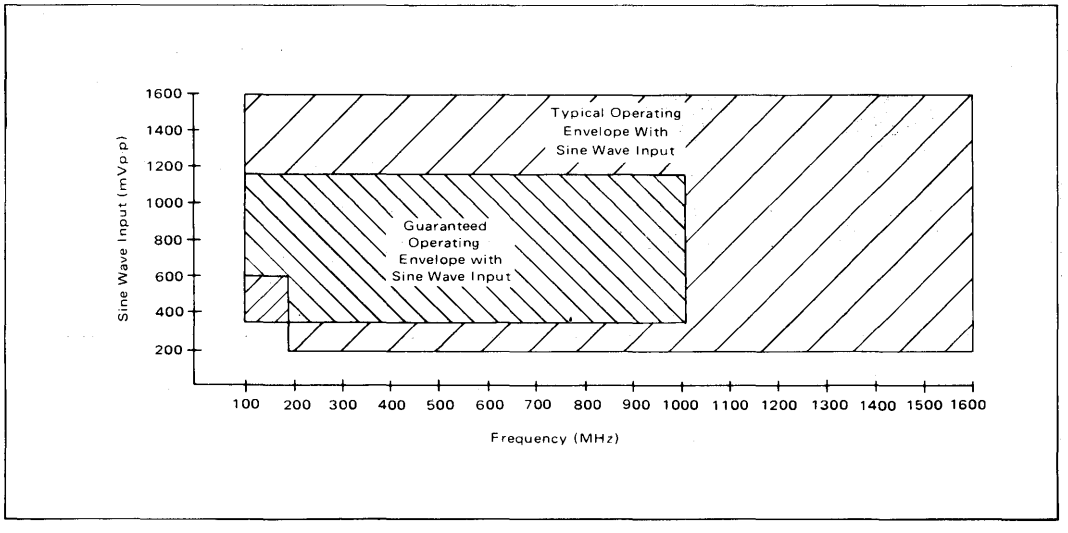
Characteristic	Symbol	MC1697P Test Limits						Unit
		0°C		+25°C		+75°C		
		Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_E	–	–	–	57	–	–	mAdc
Toggle Frequency (high frequency operation)	f_{Tog}	1.0	–	1.0	–	1.0	–	GHz
Toggle Frequency (low frequency sine wave input)	f_{Tog}	–	–	–	100	–	–	MHz

COUNT FREQUENCY TEST CIRCUIT



Note: All power supply and logic levels are shown shifted 2 volts positive.

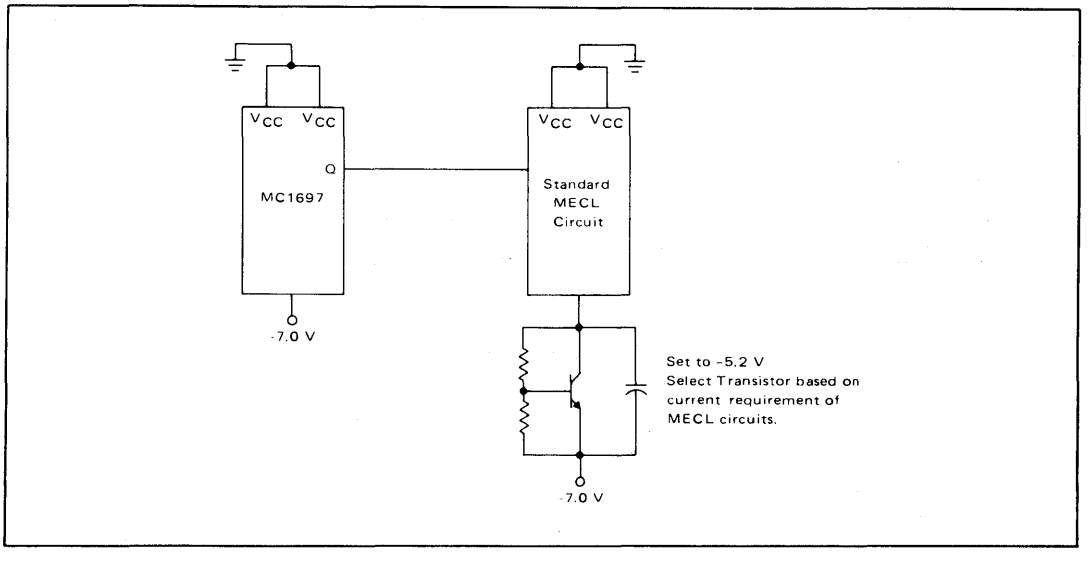
TIMING DIAGRAM



APPLICATION INFORMATION

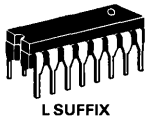
The MC1697 is a very high speed divide-by-four prescaler designed to operate on a nominal supply voltage of -7.0 volt. In some applications it may be necessary to interface the output of the MC1697 with other MECL circuits requiring a supply voltage of -5.2 volts. One method of interfacing the circuits is shown below. This configuration is adequate for frequencies up to 1 GHz over the temperature range of 0^{o} to $+75^{o}C$. For best performance it is recommended that separate regulated supplies be used.

METHOD OF INTERFACING MC1697 WITH STANDARD MECL CIRCUITS

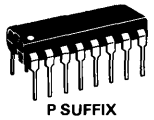


MC1699

DIVIDE-BY-FOUR GIGAHERTZ COUNTER



L SUFFIX
CERAMIC PACKAGE
CASE 620

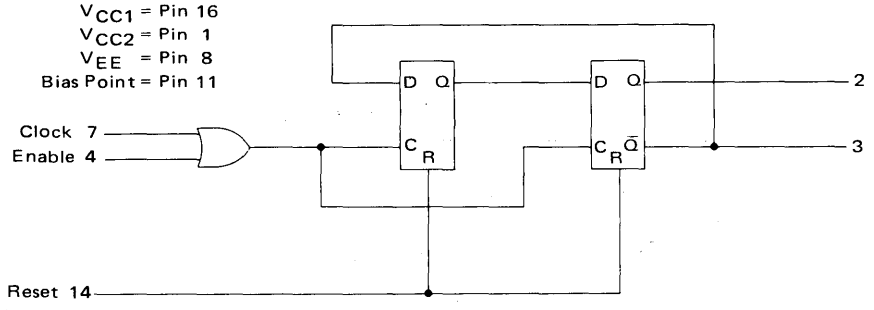


P SUFFIX
PLASTIC PACKAGE
CASE 648

The MC1699 is a divide-by-four gigahertz counter. The clock input requires an ac coupled driving signal of 800 mV amplitude (typical). The clock toggles two divide-by-two stages, and the complementary outputs (50% duty cycle) are taken from the second stage.

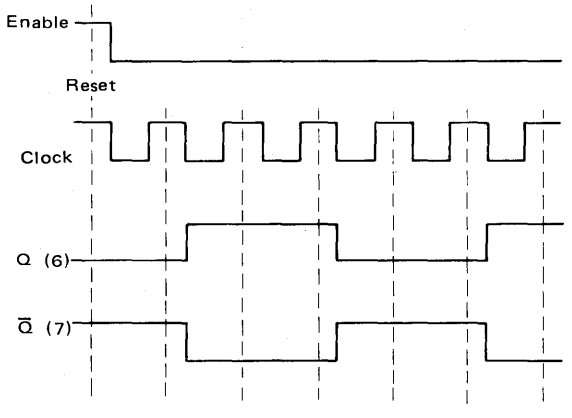
The MC1699 includes clock enable and reset. The reset is compatible with MECL III voltage levels. The enable input requires a V_{IL} of -2.0 V max. Reset operates only when either the clock or the enable is high.

Pin 11 (13) is available for connection of a decoupling capacitor to ground. This capacitor stabilizes the reference point which is internally coupled to the clock input.



Number at end of terminal denotes pin number for L package (Case 620), P package (Case 648).

TIMING DIAGRAM

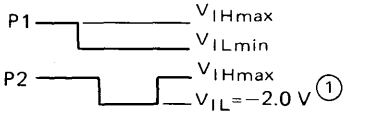


ELECTRICAL CHARACTERISTICS

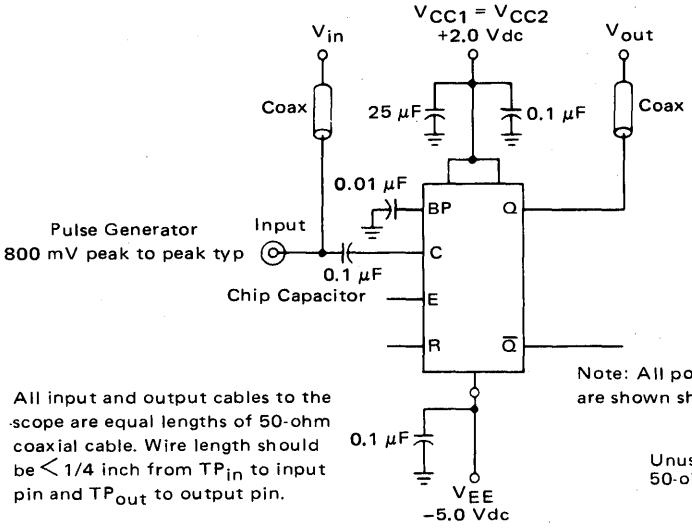
Characteristic	Symbol	-30°C		+25°C		+85°C		Unit	Conditions
		Min	Max	Min	Max	Min	Max		
Power Supply Drain Current	I_E	–	–	–	57	–	–	mAdc	All inputs and outputs open except Clock = $V_{IHC} \cong$ -4.0 Vdc
Input Current	I_{inH}							μAdc	
Reset		–	–	–	500	–	–		V_{IHmax} to Reset, V_{IL} to Enable, V_{EE} to Clock.
Enable		–	–	–	265	–	–		V_{ILmin} to reset, V_{IHmax} to Enable, V_{EE} to Clock.
Logic "1" Output Voltage	V_{OH}	-1.085	-0.875	-1.000	-0.810	-0.930	-0.700	Vdc	See Note ②. Or, apply P1 to Reset and V_{IHmax} to Enable
Logic "0" Output Voltage	V_{OL}	–	-1.630	–	-1.600	–	-1.555	Vdc	
Toggle Frequency (high frequency operation)	f_{Tog}	1.0	–	1.0	–	1.0	–	GHz	V_{IL} ① to Enable. See Test Circuit and Application Information on next page.
Toggle Frequency (low frequency sine wave input)	f_{Tog}	–	–	–	100	–	–	MHz	

① Enable input requires V_{IL} = -2.0 V max.

② Reset counter by applying pulse P1 to pin 14, then toggle outputs by applying pulse P2 to pin 4 for 2 cycles. Hold power during pulse sequence. Hold clock input @ V_{EE}.



TOGGLE FREQUENCY TEST CIRCUIT



All input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be < 1/4 inch from TP_{in} to input pin and TP_{out} to output pin.

Note: All power supply and logic levels are shown shifted 2 volts positive.

Unused outputs connected to a 50-ohm resistor to ground.

4

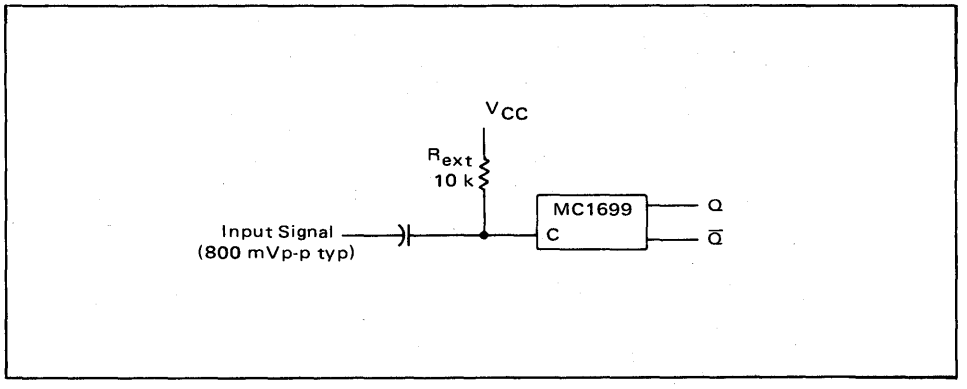
APPLICATION INFORMATION

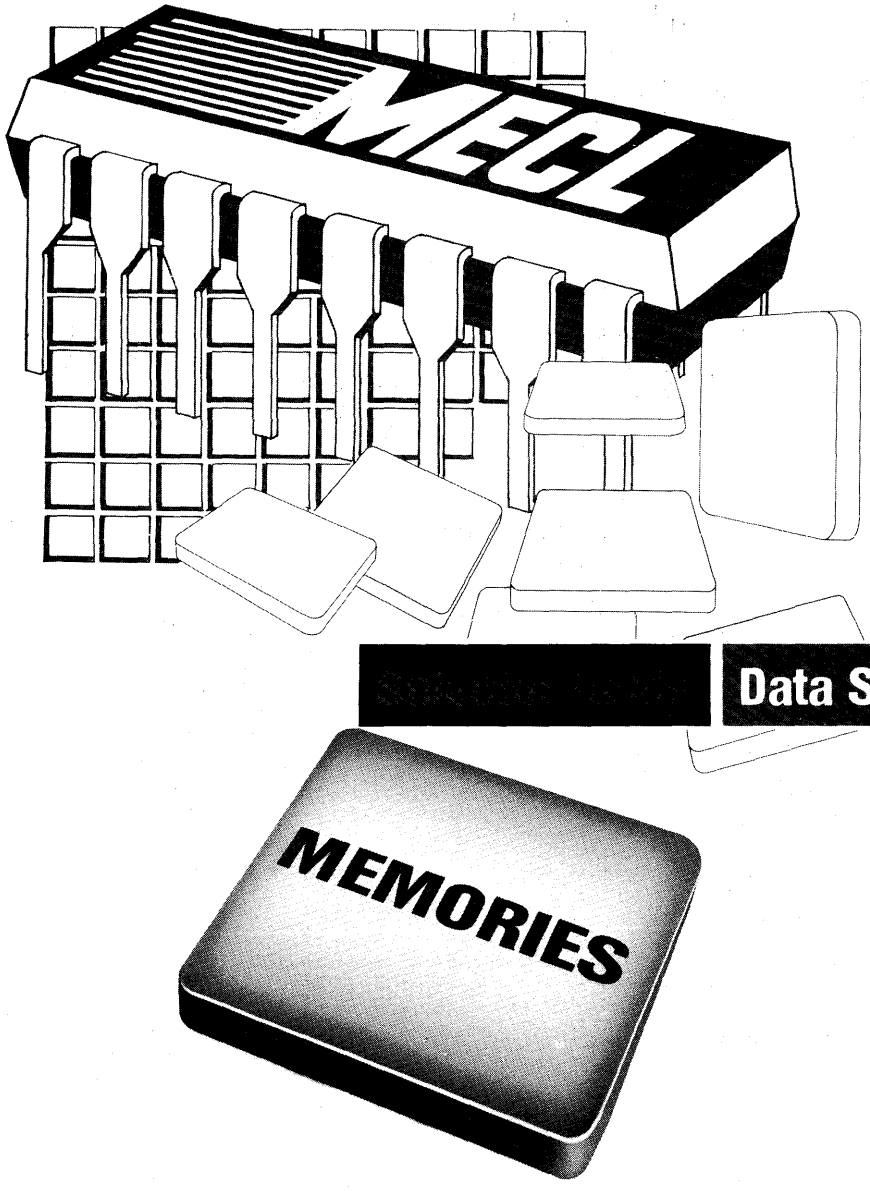
The MC1699 is a very high speed divide-by-four counter intended for prescaler applications. The reset provides increased flexibility for counter and time measuring requirements.

The clock input is designed to accept a capacitor-coupled sine wave signal for frequencies above 100 MHz. Below 100 MHz waveshaping is recommended to obtain good MECL III or MECL 10,000 edge speeds.

With a continuous input signal the clock can be capacitor-coupled with no problems. However, if the clock is interrupted and the clock input floats to the bias point reference voltage, the counter may oscillate. To prevent this oscillation, an external resistor can be added as shown in Figure 1. This resistor is recommended only when the clock is interrupted and serves no useful function with a continuous signal. Also, this external resistor is not required when the enable input is used to gate the clock signal.

FIGURE 1

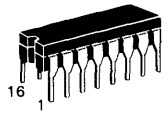




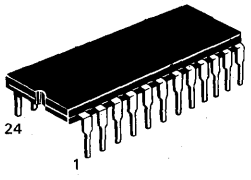
Data Sheets

5

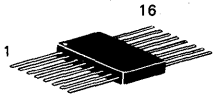
MECL Memories
INTEGRATED CIRCUITS



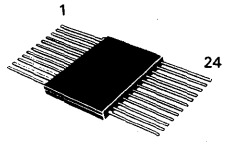
L SUFFIX
CERAMIC PACKAGE
CASE 620



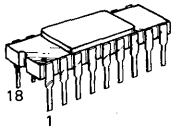
L SUFFIX
CERAMIC PACKAGE
CASE 623



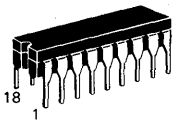
F SUFFIX
CERAMIC PACKAGE
CASE 650



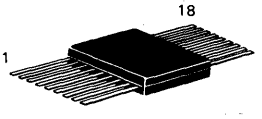
F SUFFIX
CERAMIC PACKAGE
CASE 652



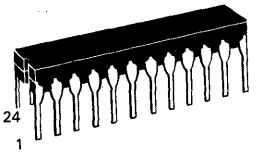
L SUFFIX
SIDE BRAISED
CERAMIC PACKAGE
CASE 680



L SUFFIX
CERAMIC PACKAGE
CASE 726



F SUFFIX
CERAMIC PACKAGE
CASE 747



L SUFFIX
CERAMIC PACKAGE
CASE 748

5

Device	Organization (Word × Bit)	Access Time	Pins	Case
ECL 10K, 10KH				
MC10H145	16 × 4	6	16	620, 648
MCM10143	8 × 2	15.3	24	623, 652
MCM10144	256 × 1	26	16	620, 650
MCM10145	16 × 4	15	16	620, 650
MCM10146	1024 × 1	29	16	620, 650
MCM10147	128 × 1	15	16	620, 650
MCM10148	64 × 1	15	16	620, 650
MCM10152	256 × 1	15	16	620, 650
MCM10415-20	1024 × 1	20	16	620, 650
MCM10415-15	1024 × 1	15	16	620, 650
MCM10415-10*	1024 × 1	10	16	620, 650
MCM10422-15*	256 × 4	15	24	748
MCM10422-10*	256 × 4	10	24	748
MCM10470-25*	4096 × 1	25	18	680, 747
MCM10470-15*	4096 × 1	15	18	680, 747
MCM10474-25*	1024 × 4	25	24	748
MCM10474-15*	1024 × 4	15	24	748
MCM10480-20*	16384 × 1	20	20	747, 748
MCM10484-20*	4096 × 4	20	TBD	TBD
ECL 100K				
MCM100415-10	1024 × 1	10	16	620, 650
MCM100422-10	256 × 4	10	24	652, 748
MCM100470-15	4096 × 1	15	18	726, 747
MCM100474-15	1024 × 4	15	24	748
MCM100480-20	16384 × 1	20	20	747, 748
MCM100484-20	4096 × 4	20	TBD	TBD
PROMS				
MCM10139*	32 + 8	20	16	620, 650
MCM10149**	256 + 4	25	16	620, 650
MCM10149A*	256 + 4	15	16	620, 650

*—**To be introduced.**

** Available in 10500 series -55°C to +125°C temperature range.

MOTOROLA

MCM10139

MECL

32 X 8 BIT PROGRAMMABLE READ-ONLY MEMORY

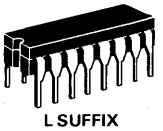
256-BIT PROGRAMMABLE READ ONLY MEMORY (PROM)

The MCM10139 is a 256-bit programmable read only memory (PROM). The circuit is organized as 32 words of 8 bits. Prior to programming, all stored bits are at logic 0 (low) levels. The logic state of each bit can then be changed by on-chip programming circuitry. The MCM10139 has a single negative logic chip enable. When the chip is disabled ($\overline{CS}$ = high), all outputs are forced to a logic 0 (low).

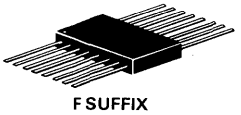
The MCM10139 is fully compatible with the MECL 10,000 logic family. It is designed for use in microprogramming, code conversion, logic simulation, and look-up table storage.

P_D = 520 mW typ/pkg (No Load)

t_{Access} = 15 ns typ (Address Inputs)



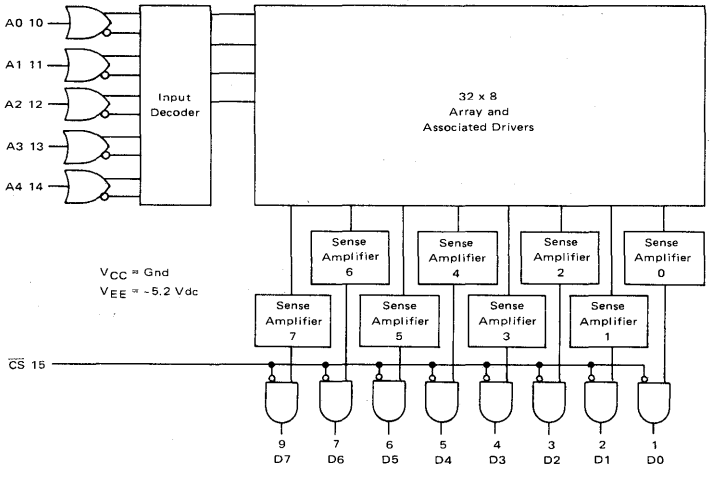
L SUFFIX
CERAMIC PACKAGE
CASE 620



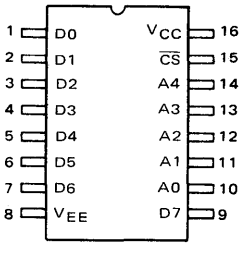
F SUFFIX
CERAMIC PACKAGE
CASE 650

5

LOGIC DIAGRAM



PIN ASSIGNMENT



ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage (V_{CC} = 0)	V_{EE}	-8 to 0	Vdc
Base Input Voltage (V_{CC} = 0)	V_{in}	0 to V_{EE}	Vdc
Output Source Current — Continuous — Surge	I_O	<50 <100	mAdc
Junction Operating Temperature	T_J	<165	°C
Storage Temperature Range	T_{stg}	-55 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.

ELECTRICAL CHARACTERISTICS

	DC Test Voltage Values (Volts)				
Test Temperature	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
0°C	-0.840	-1.870	-1.145	-1.490	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+75°C	-0.720	-1.830	-1.045	-1.450	-5.2

Each MECL Memory circuit has been designed to meet the dc and ac specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts.

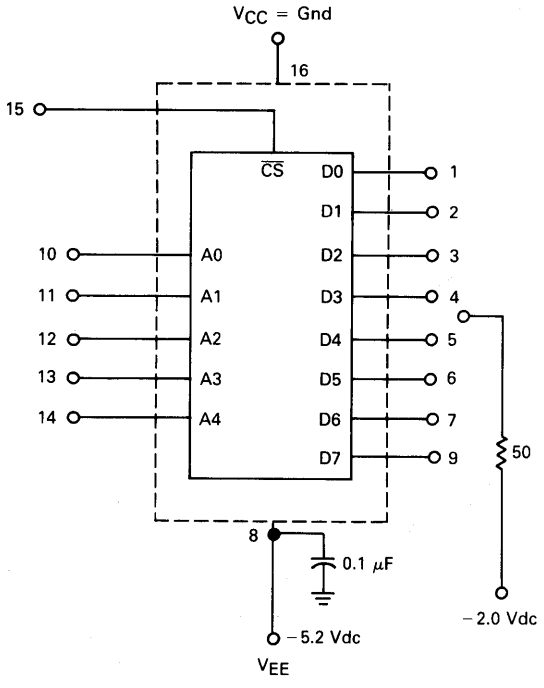
		MCM10139 Test Limits							
		0°C		+25°C		+75°C			
DC Characteristics	Symbol	Min	Max	Min	Max	Min	Max	Unit	Conditions
Power Supply Drain Current	I_{EE}	—	150	—	145	—	140	mAdc	Typ I_{EE} @ 25°C = 100 mA. All outputs and inputs open. Measure pin 8.
Input Current High	$I_{in}H$	—	265	—	265	—	265	μAdc	Test one input at a time, all other inputs are open. $V_{in} = V_{IH}$.
Input Current Low	$I_{in}L$	0.5	—	0.5	—	0.3	—	μAdc	Test one input at a time, all other inputs are open. $V_{in} = V_{IL}$.
Logic "1" Output Voltage	V_{OH}	-1.000	-0.840	-0.960	-0.810	-0.900	-0.720	Vdc	Load 50 Ω to -2.0 V.
Logic "0" Output Voltage	V_{OL}	-2.010	-1.665	-1.990	-1.650	-1.970	-1.625	Vdc	
Logic "1" Threshold Voltage	V_{OHA}	-1.020	—	-0.980	—	-0.920	—	Vdc	Threshold testing is performed and guaranteed on one input at a time.
Logic "0" Threshold Voltage	V_{OLA}	—	-1.645	—	-1.630	—	-1.605	Vdc	$V_{in} = V_{ILH}$ or V_{ILA}. Load 50 Ω to -2.0 V.

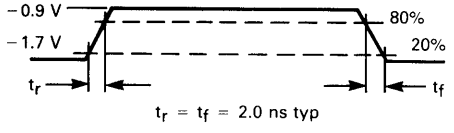
SWITCHING CHARACTERISTICS (T_A = 0° to +75°C, V_{EE} = -5.2 Vdc ±5%; Output Load—See Figure 1 and Note 1)

		Test Limits				
Characteristic	Symbol	Min	Typ	Max	Unit	Conditions
Chip Select Access Time	t_{ACS}	—	10	15	ns	See Figures 2 and 3.
Chip Select Recovery Time	t_{RCS}	—	10	15	ns	Measured from 50% of input to 50%
Address Access Time	t_{AA}	—	15	20	ns	of output. See Note 2.
Output Rise and Fall Time	t_r, t_f	—	3.0	—	ns	Measured between 20% and 80% points.
Input Capacitance	C_{in}	—	4.0	5.0	pF	
Output Capacitance	C_{out}	—	7.0	8.0	pF	

Notes: 1. Contact your Motorola Sales Representative for details if extended temperature operation is desired.
2. The maximum Address Access Time is guaranteed to be the Worst-Case Bit in the memory.

FIGURE 1 — SWITCHING TIME TEST CIRCUIT





All timing measurements referenced to 50% of input levels.
All outputs loaded 50 ohms to −2.0 Vdc.

FIGURE 2 — CHIP SELECT ACCESS TIME

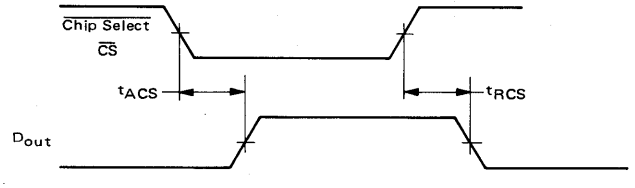
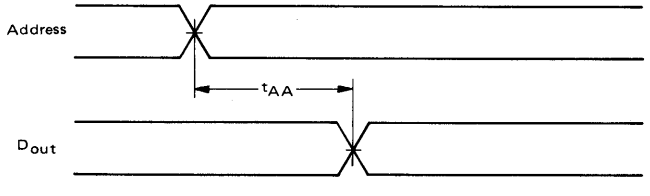


FIGURE 3 — ADDRESS ACCESS TIME



RECOMMENDED PROGRAMMING PROCEDURE*

The MCM10139 is shipped with all bits at logical "0" (low). To write logical "1s", proceed as follows.

MANUAL (See Figure 4)

Step 1 Connect V_{EE} (Pin 8) to -5.2 V and V_{CC} (Pin 16) to 0.0 V. Address the word to be programmed by applying -1.2 to -0.6 volts for a logic "1" and -5.2 to -4.2 volts for a logic "0" to the appropriate address inputs.

Step 2 Raise V_{CC} (Pin 16) to +6.8 volts.

Step 3 After V_{CC} has stabilized at +6.8 volts (including any ringing which may be present on the V_{CC} line), apply a current pulse of 2.5 mA to the output pin corresponding to the bit to be programmed to a logic "1".

Step 4 Return V_{CC} to 0.0 Volts.

CAUTION

To prevent excessive chip temperature rise, V_{CC} should not be allowed to remain at +6.8 volts for more than 1 second.

Step 5 Verify that the selected bit has programmed by connecting a 460 Ω resistor to -5.2 volts and measuring the voltage at the output pin. If a logic "1" is not detected at the output, the procedure should be repeated once. During verification V_{IH} should be -1.0 to -0.6 volts.

Step 6 If verification is positive, proceed to the next bit to be programmed.

AUTOMATIC (See Figure 5)

Step 1 Connect V_{EE} (Pin 8) to -5.2 volts and V_{CC} (Pin 16) to 0.0 volts. Apply the proper address data and raise V_{CC} (Pin 16) to +6.8 volts.

Step 2 After a minimum delay of 100 μs and a maximum delay of 1.0 ms, apply a 2.5 mA current pulse to the first bit to be programmed ($0.1 \leqslant PW \leqslant 1$ ms).

Step 3 Repeat Step 2 for each bit of the selected word specified as a logic "1". (Program only one bit at a time. The delay between output programming pulses should be equal to or less than 1.0 ms.)

Step 4 After all the desired bits of the selected word have been programmed, change address data and repeat Steps 2 and 3.

NOTE: If all the maximum times listed above are maintained, the entire memory will program in less than 1 second. Therefore, it would be permissible for V_{CC} to remain at +6.8 volts during the entire programming time.

Step 5 After stepping through all address words, return V_{CC} to 0.0 volts and verify that each bit has programmed. If one or more bits have not programmed, repeat the entire procedure once. During verification V_{IH} should be -1.0 to -0.6 volts.

*NOTE: For devices that program incorrectly—return serialized units with individual truth tables. Noncompliance voids warranty.

5

PROGRAMMING SPECIFICATIONS

Characteristic	Symbol	Limits			Units	Conditions
		Min	Typ	Max		
Power Supply Voltage	V_{EE}	-5.46	-5.2	-4.94	Vdc	
To Program	V_{CCP}	+6.04	+6.8	+7.56	Vdc	
To Verify	V_{CCV}	0	0	0	Vdc	
Programming Supply Current	I_{CCP}	–	200	600	mA	V_{CC} = +6.8 Vdc
Address Voltage	V_{IH} Program	-1.2	–	-0.6	Vdc	
Logical "1"	V_{IH} Verify	-1.0	–	-0.6	Vdc	
Logical "0"	V_{IL}	-5.2	–	-4.2	Vdc	
Maximum Time at $V_{CC} = V_{CCP}$	–	–	–	1.0	sec	
Output Programming Current	I_{OP}	2.0	2.5	3.0	mAdc	
Output Program Pulse Width	t_p	0.5	–	1.0	ms	
Output Pulse Rise Time	–	–	–	10	μs	
Programming Pulse Delay (1)						
Following V_{CC} change	t_d	0.1	–	1.0	ms	
Between Output Pulses	t_{d1}	0.01	–	1.0	ms	

NOTE 1. Maximum is specified to minimize the amount of time V_{CC} is at +6.8 volts.

FIGURE 4 – MANUAL PROGRAMMING CIRCUIT

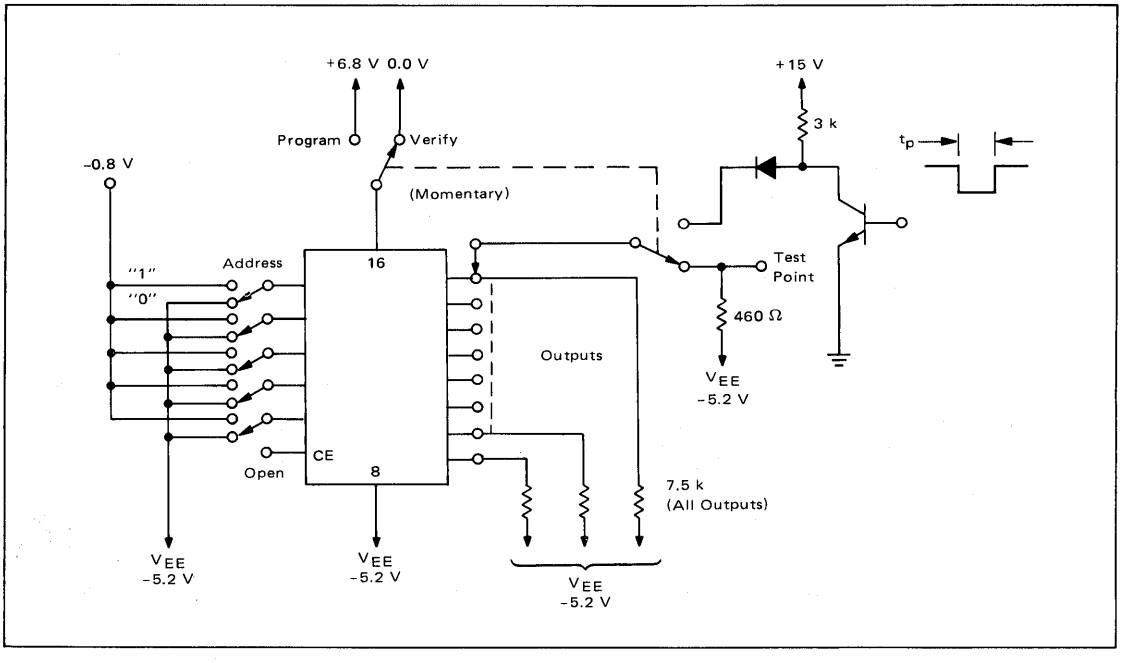
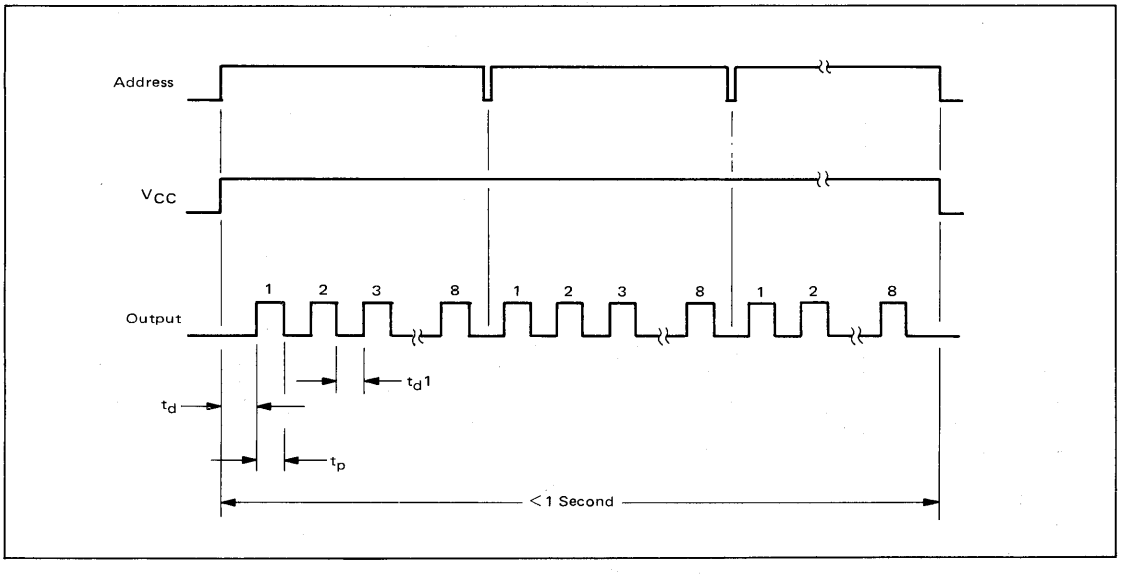


FIGURE 5 – AUTOMATIC PROGRAMMING CIRCUIT



5

MOTOROLA

MCM10143

MECL

8 x 2 MULTIPORT REGISTER FILE (RAM)

8 x 2 MULTIPORT REGISTER FILE (RAM)

The MC10143 is an 8 word by 2 bit multiport register file (RAM) capable of reading two locations and writing one location simultaneously. Two sets of eight latches are used for data storage in this LSI circuit.

WRITE

The word to be written is selected by addresses A_0–A_2. Each bit of the word has a separate write enable to allow more flexibility in system design. A write occurs on the positive transition of the clock. Data is enabled by having the write enables at a low level when the clock makes the transition. To inhibit a bit from being written, the bit enable must be at a high level when the clock goes low and not change until the clock goes high. Operation of the clock and the bit enables can be reversed. While the clock is low a positive transition of the bit enable will write that bit into the address selected by A_0–A_2

READ

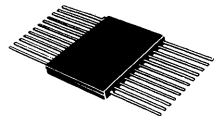
When the clock is high any two words may be read out simultaneously, as selected by addresses B_0–B_2 and C_0–C_2, including the word written during the preceding half clock cycle. When the clock goes low the addressed data is stored in the slaves. Level changes on the read address lines have no effect on the output until the clock again goes high. Read out is accomplished at any time by enabling output gates (B_0–B_1), (C_0–C_1).

t_{pd}:
Clock to Data out = 5 ns (typ)
(Read Selected)
Address to Data out = 10 ns (typ)
(Clock High)
$\overline{\text{Read Enable}}$ to Data out = 2.8 ns (typ)
(Clock high, Addresses present)
P_D = 610 mW/pkg (typ no load)

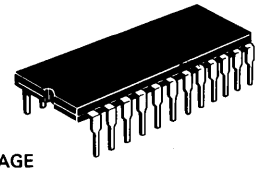
TRUTH TABLE

*MODE	INPUT							OUTPUT			
	**Clock	$\overline{WE}_0$	$\overline{WE}_1$	D_0	D_1	$\overline{RE}_B$	$\overline{RE}_C$	QB_0	QB_1	QC_0	QC_1
Write	L→H	L	L	H	H	H	H	L	L	L	L
Read	H	ϕ	ϕ	ϕ	ϕ	L	L	H	H	H	H
Read	H→L	ϕ	ϕ	ϕ	ϕ	L	L	H	H	H	H
Read	L→H→L	H	H	ϕ	ϕ	L	L	H	H	H	H
Write	L→H	L	L	L	H	H	H	L	L	L	L
Read	H	ϕ	ϕ	ϕ	ϕ	L	L	L	H	L	H

**Note: Clock occurs sequentially through Truth Table
*Note: A0-A2, B0-B2, and C0-C2 are all set to same address location throughout Table.
ϕ = Don't Care

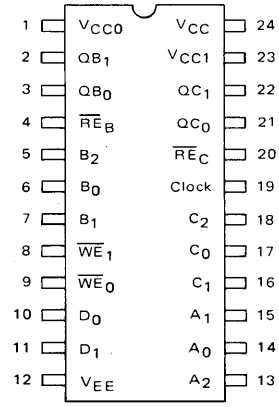


F SUFFIX
CERAMIC PACKAGE
CASE 652



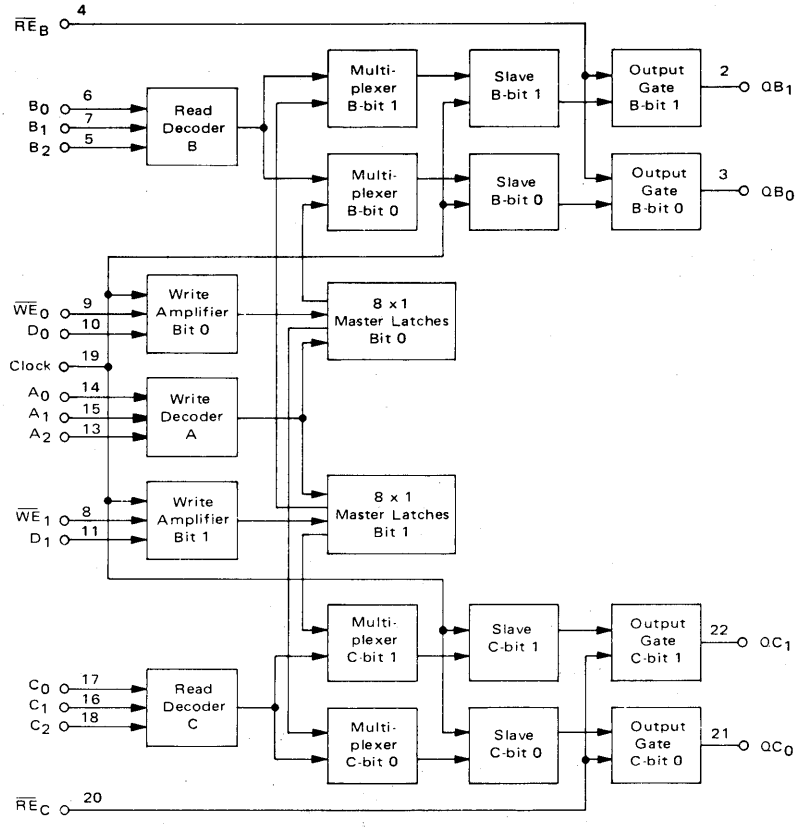
L SUFFIX
CERAMIC PACKAGE
CASE 623

PIN ASSIGNMENT



5

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage (V_{CC} = 0)	V_{EE}	-8 to 0	Vdc
Base Input Voltage (V_{CC} = 0)	V_{in}	0 to V_{EE}	Vdc
Output Source Current — Continuous — Surge	I_O	< 50 < 100	mAdc
Junction Operating Temperature	T_J	< 165	°C
Storage Temperature Range	T_{stg}	-55 to +150	°C

Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.

ELECTRICAL CHARACTERISTICS

Test Temperature	DC TEST VOLTAGE VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
0°C	-0.840	-1.870	-1.145	-1.490	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+75°C	-0.720	-1.830	-1.045	-1.450	-5.2

ELECTRICAL CHARACTERISTICS

Each MECL Memory circuit has been designed to meet the dc and ac specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts.

SWITCHING CHARACTERISTICS (T_A = 0° to +75°C, V_{EE} = −5.2 Vdc ± 5%)

Characteristics	Symbol	0°C Min	0°C Max	+25°C Min	+25°C Typ	+25°C Max	+75°C Min	+75°C Max	Unit
Power Supply Drain Current	I_E	—	150	—	118	150	—	150	mAdc
Input Current	I_{inH}								μAdc
Pins 10, 11, 19		—	245	—	—	245	—	245	
All other pins		—	200	—	—	200	—	200	
Switching Times ①									ns
Read Mode									
Address Input	$t_{B\pm QB\pm}$	4.0	15.3	4.5	10	14.5	4.5	15.5	
$\overline{\text{Read Enable}}$	$t_{\overline{RE}-QB+}$	1.1	5.3	1.2	3.5	5.0	1.2	5.5	
Data	$t_{Clock+QB-}$	1.7	7.3	2.0	5.0	7.0	2.0	7.6	
Setup									
Address	$t_{setup(B-Clock-)}$	—	—	8.5	5.5	—	—	—	
Hold									
Address	$t_{hold(Clock-B+)}$	—	—	-1.5	-4.5	—	—	—	
Write Mode									
Setup									
$\overline{\text{Write Enable}}$	$t_{setup(\overline{WE}-Clock+)}$	—	—	7.0	4.0	—	—	—	
	$t_{setup(\overline{WE}+Clock-)}$	—	—	1.0	-2.0	—	—	—	
Address	$t_{setup(A-Clock+)}$	—	—	8.0	5.0	—	—	—	
Data	$t_{setup(D-Clock+)}$	—	—	5.0	2.0	—	—	—	
Hold									
$\overline{\text{Write Enable}}$	$t_{hold(Clock-\overline{WE}+)}$	—	—	5.5	2.5	—	—	—	
	$t_{hold(Clock+\overline{WE}-)}$	—	—	1.0	-2.0	—	—	—	
Address	$t_{hold(Clock+A+)}$	—	—	1.0	-3.0	—	—	—	
Data	$t_{hold(Clock+D+)}$	—	—	1.0	-2.0	—	—	—	
Write Pulse Width	$PW_{\overline{WE}}$	—	—	8.0	5.0	—	—	—	
Rise Time, Fall Time (20% to 80%)	t_r, t_f	1.1	4.2	1.1	2.5	4.0	1.1	4.5	

① AC timing figures do not show all the necessary presetting conditions.

5

READ TIMING DIAGRAMS

Access (Clock High)

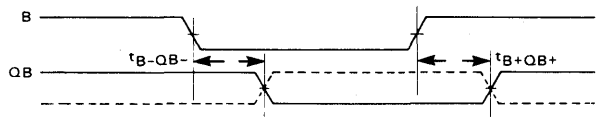


FIGURE 1

Enable

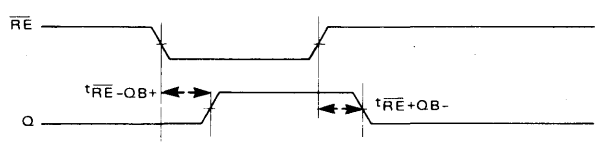


FIGURE 2

Data (Address Selected)

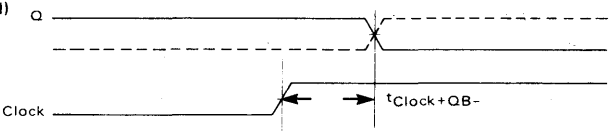


FIGURE 3

Setup and Hold

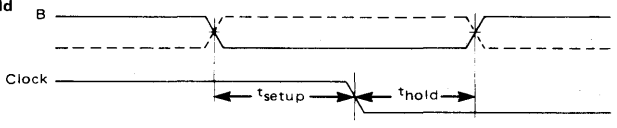


FIGURE 4

WRITE TIMING DIAGRAM

Enable Setup

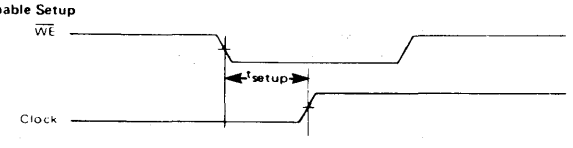


FIGURE 5

Enable Hold

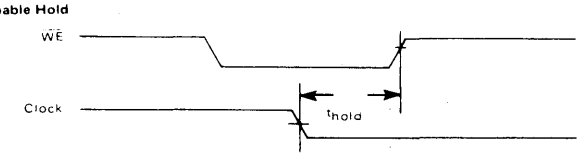


FIGURE 6

Disable

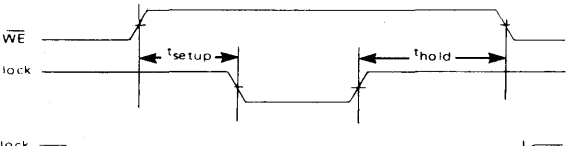


FIGURE 7

Pulse Width

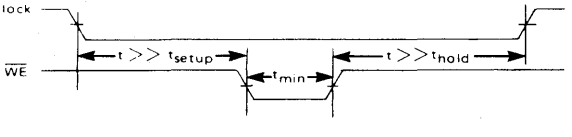


FIGURE 8

Address

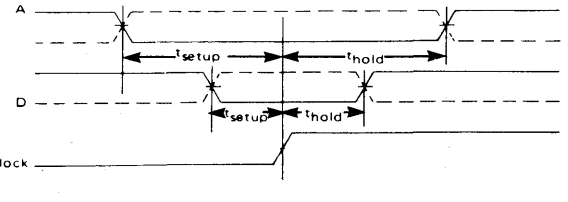


FIGURE 9

5

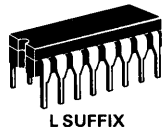
MOTOROLA

MCM10144

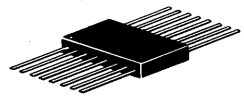
256 x 1-BIT RANDOM ACCESS MEMORY

The MCM10144 is a 256 word x 1-bit Read/Write Random Access Memory. Data is accessed or stored by means of an 8-bit address decoded on chip. It has a non-inverting data out, a separate data in line and 3 active-low chip select lines. It has a typical access time of 17 ns and is designed for high-speed scratch pad, control, cache, and buffer storage applications.

- Typical Address Access Time = 17 ns
- Typical Chip Select Access Time = 4.0 ns
- Operating Temperature Range = 0° to +75°C
- Open Emitter Output Permits Wired-OR for Easy Memory Expansion
- 50 kΩ Input Pulldown Resistors on Chip Select
- Power Dissipation Decreases with Increasing Temperature
- Fully Compatible with MECL 10,000 Logic Family
- Pin-for-Pin Replacement for F10410



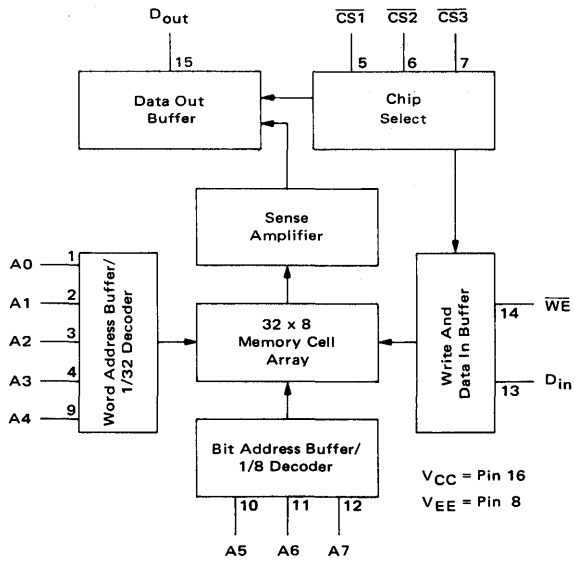
L SUFFIX
CERAMIC PACKAGE
CASE 620



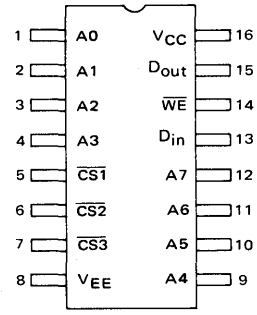
F SUFFIX
CERAMIC PACKAGE
CASE 650

5

BLOCK DIAGRAM



PIN ASSIGNMENT



PIN NOTATION

CS	Chip Select Input
A0 thru A7	Address Inputs
D_{in}	Data Input
D_{out}	Data Output
WE	Write Enable Input

TRUTH TABLE

MODE	INPUT			OUTPUT
	$\overline{CS}$*	$\overline{WE}$	D_{in}	D_{out}
Write "0"	L	L	L	L
Write "1"	L	L	H	L
Read	L	H	ϕ	Q
Disabled	H	ϕ	ϕ	L

*$\overline{CS} = \overline{CS1} + \overline{CS2} + \overline{CS3}$ ϕ = Don't Care.

FUNCTIONAL DESCRIPTION:

The MCM10144 is a 256 word x 1-bit RAM. Bit selection is achieved by means of an 8-bit address A0 thru A7.

The active-low chip select allows memory expansion up to 2048 words. The fast chip select access time allows memory expansion without affecting system performance.

The operating mode of the RAM ($\overline{CS}$ inputs low) is controlled by the $\overline{WE}$ input. With $\overline{WE}$ low the chip is in the write mode—the output is low and the data present at D_{in} is stored at the selected address. With $\overline{WE}$ high the chip is in the read mode—the data state at the selected memory location is presented non-inverted at D_{out}.

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage (V_{CC} = 0)	V_{EE}	-8 to 0	Vdc
Base Input Voltage (V_{CC} = 0)	V_{in}	0 to V_{EE}	Vdc
Output Source Current — Continuous — Surge	I_O	< 50 < 100	mAdc
Junction Operating Temperature	T_J	< 165	°C
Storage Temperature Range	T_{stg}	-55 to +150	°C

Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.

	DC TEST VOLTAGE VALUES (Volts)				
Test Temperature	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
0°C	-0.840	-1.870	-1.145	-1.490	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+75°C	-0.720	-1.830	-1.045	-1.450	-5.2

ELECTRICAL CHARACTERISTICS

Each MECL Memory circuit has been designed to meet the dc and ac specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts.

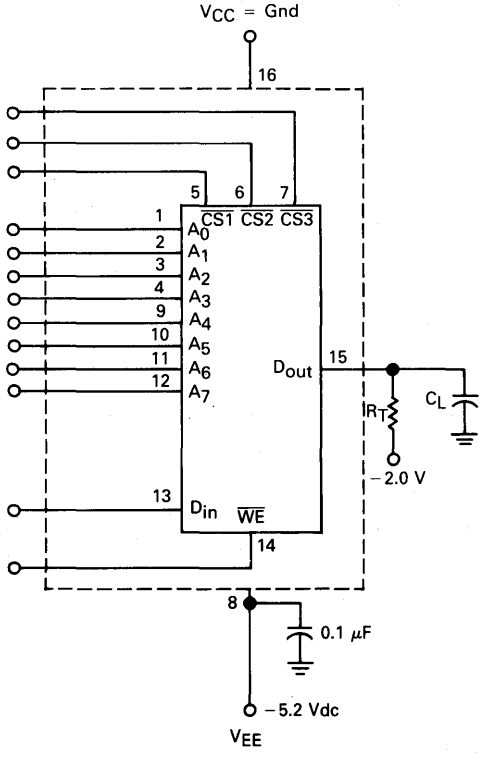
		MCM10144 Test Limits							
		0°C		+25°C		+75°C			
DC Characteristics	Symbol	Min	Max	Min	Max	Min	Max	Unit	Conditions
Power Supply Drain Current	I_{EE}	—	130	—	125	—	120	mAdc	Typ I_{EE} @ 25°C = 90 mA All outputs and inputs open. Measure pin 8.
Input Current High	$I_{in}H$	—	220	—	220	—	220	μAdc	Test one input at a time, all other inputs are open. $V_{in} = V_{IH}$.
Input Current Low	$I_{in}L$	0.5	—	0.5	—	0.3	—	μAdc	Test one input at a time, all other inputs are open. $V_{in} = V_{IL}$.
Logic "1" Output Voltage	V_{OH}	-1.000	-0.840	-0.960	-0.810	-0.900	-0.720	Vdc	Load 50 Ω to -2.0 V
Logic "0" Output Voltage	V_{OL}	-1.870	-1.665	-1.850	-1.650	-1.830	-1.625	Vdc	
Logic "1" Threshold Voltage	V_{OHA}	-1.020	—	-0.980	—	-0.920	—	Vdc	Threshold testing is performed and guaranteed on one input at a time. $V_{in} = V_{IHA}$ or V_{ILA}. Load 50 Ω to -2.0 V.
Logic "0" Threshold Voltage	V_{OLA}	—	-1.645	—	-1.630	—	-1.605	Vdc	

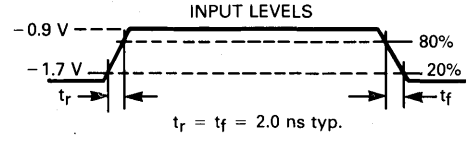
SWITCHING CHARACTERISTICS (T_A = 0° to +75°C, V_{EE} = -5.2 Vdc ± 5%; Output Load see Figure 1; see Note 1 & 3.)

Characteristic	Symbol	Test Limits Min	Typ	Max	Unit	Conditions
Read Mode						See Figures 2 and 3.
Chip Select Access Time	t_{ACS}	2.0	4.0	10	ns	Measured from 50% of input to 50% of
Chip Select Recovery Time	t_{RCS}	2.0	4.0	10	ns	output. See Note 2.
Address Access Time	t_{AA}	7.0	17	26	ns	
Write Mode						
Write Pulse Width	t_W	25	6.0	–	ns	t_{WSA} = 8.0 ns
Data Setup Time Prior to Write	t_{WSD}	2.0	-3.0	–	ns	Measured at 50% of input to 50% of
Data Hold Time After Write	t_{WHD}	2.0	-3.0	–	ns	output.
Address Setup Time Prior to Write	t_{WSA}	8.0	0	–	ns	t_W = 25 ns. See Figure 4.
Address Hold Time After Write	t_{WHA}	0.0	-4.0	–	ns	
Chip Select Setup Time Prior to Write	t_{WSCS}	2.0	-3.0	–	ns	
Chip Select Hold Time After Write	t_{WHCS}	2.0	-3.0	–	ns	
Write Disable Time	t_{WS}	2.5	5.0	10	ns	
Write Recovery Time	t_{WR}	2.5	5.0	10	ns	
Rise and Fall Time						Measured between 20% and 80% points.
Output Rise and Fall Time	t_r, t_f	1.5	3.0	7.0	ns	When driven from Address inputs.
Output Rise and Fall Time	t_r, t_f	1.5	3.0	5.0	ns	When driven from $\overline{CS}$ or $\overline{WE}$ inputs.
Capacitance						
Input Capacitance	C_{in}	–	4.0	5.0	pF	
Output Capacitance	C_{out}	–	7.0	8.0	pF	

Notes: (1) Contact your Motorola Sales Representative for details if extended temperature operation is desired.
(2) The maximum Address Access Time is guaranteed to be the Worst-Case Bit in the Memory.
(3) For proper use of MECL Memories in a system environment, consult: "MECL System Design Handbook."

FIGURE 1 — SWITCHING TIME TEST CIRCUIT





All timing measurements referenced to 50% of input levels.
R_T = 50 Ω
$C_L \leq$ 5.0 pF (including jig and stray capacitance)
Delay should be derated 30 ps/pF for capacitive load up to 50 pF

FIGURE 2 – CHIP SELECT ACCESS TIME

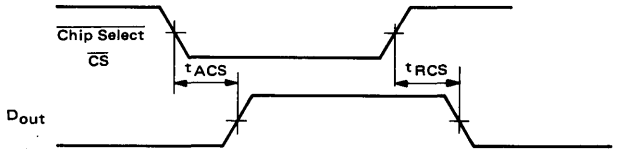


FIGURE 3 – ADDRESS ACCESS TIME

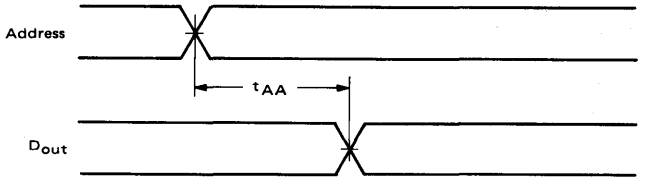
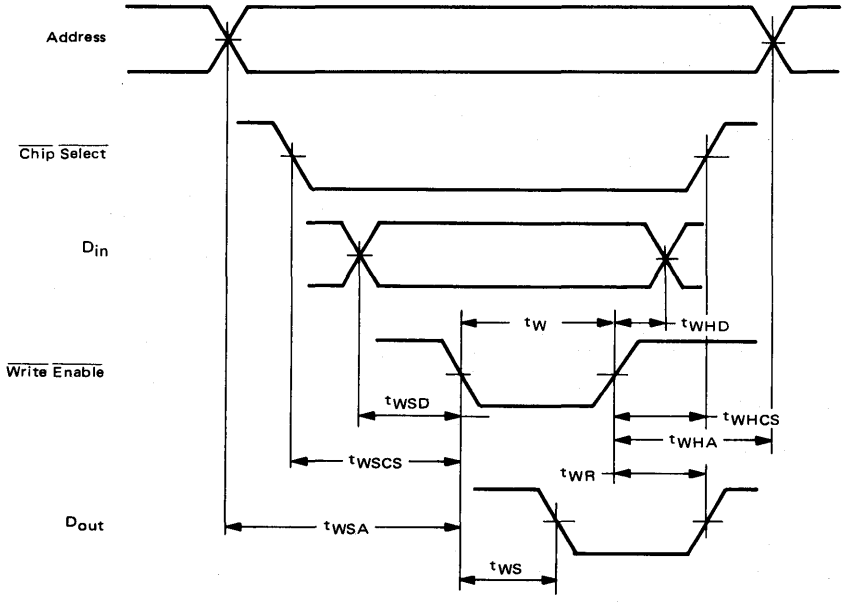


FIGURE 4 – WRITE MODE



5

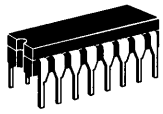
MOTOROLA

MCM10145

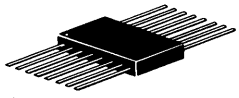
64-BIT REGISTER FILE (RAM)

The MCM10145 is a 64-Bit RAM organized as a 16 x 4 array. This organization and the high speed make the MCM10145 particularly useful in register file or small scratch pad applications. Fully decoded inputs, together with a chip enable, provide expansion of memory capacity. The Write Enable input, when low, allows data to be entered; when high, disables the data inputs. The Chip Select input when low, allows full functional operation of the device; when high, all outputs go to a low logic state. The Chip Select, together with open emitter outputs allow full wire-ORing and data bussing capability. On-chip input pulldown resistors allow unused inputs to remain open.

- Typical Address Access Time = 10 ns
- Typical Chip Select Access Time = 4.5 ns
- Operating Temperature Range = 0° to +75°C
- 50 kΩ Pulldown Resistors on All Inputs
- Fully Compatible with MECL 10,000
- Pin-for-Pin Compatible with the F10145



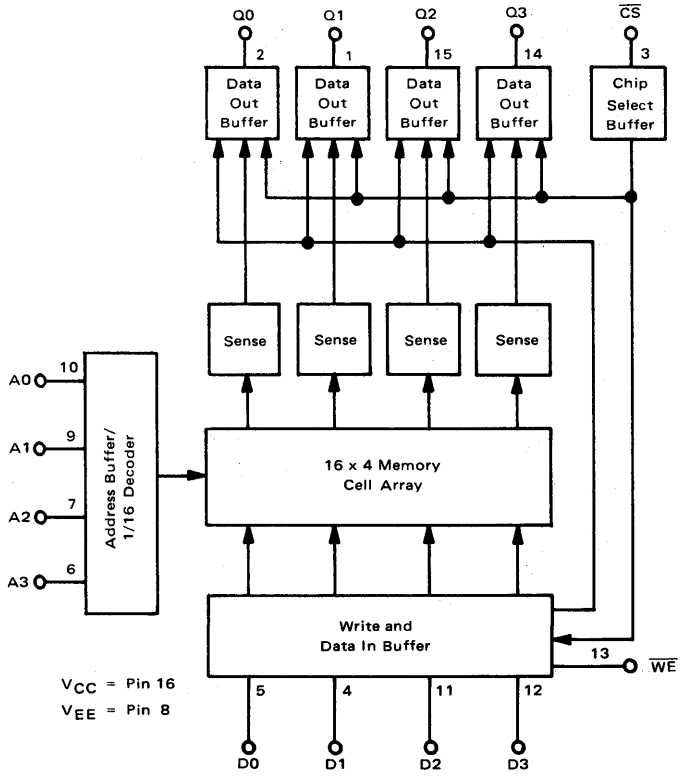
L SUFFIX
CERAMIC PACKAGE
CASE 620



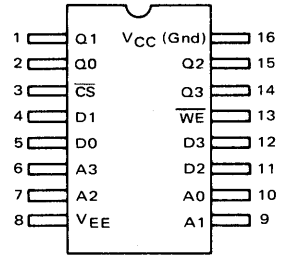
F SUFFIX
CERAMIC PACKAGE
CASE 650

5

BLOCK DIAGRAM



PIN ASSIGNMENT



PIN NOTATION

$\overline{CS}$	Chip Select Input
A0 thru A3	Address Inputs
D0 thru D3	Data Inputs
Q0 thru Q3	Data Outputs
$\overline{WE}$	Write Enable Input

TRUTH TABLE

MODE	INPUT			OUTPUT
	$\overline{CS}$	$\overline{WE}$	D_n	Q_n
Write "0"	L	L	L	L
Write "1"	L	L	H	L
Read	L	H	ϕ	Q
Disabled	H	ϕ	ϕ	L

ϕ = Don't Care.

FUNCTIONAL DESCRIPTION:

The MCM10145 is a 16 word x 4-bit RAM. Bit selection is achieved by means of a 4-bit address A0 thru A3.

The active-low chip select allows memory expansion up to 32 words. The fast chip select access time allows memory expansion without affecting system performance.

The operating mode of the RAM ($\overline{CS}$ input low) is controlled by the $\overline{WE}$ input. With $\overline{WE}$ low the chip is in the write mode—the output is low and the data present at D_n is stored at the selected address. With $\overline{WE}$ high the chip is in the read mode—the data state at the selected memory location is presented non-inverted at Q_n.

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage (V_{CC} = 0)	V_{EE}	-8 to 0	Vdc
Base Input Voltage (V_{CC} = 0)	V_{in}	0 to V_{EE}	Vdc
Output Source Current — Continuous — Surge	I_O	< 50 < 100	mAdc
Junction Operating Temperature	T_J	< 165	°C
Storage Temperature Range	T_{stg}	-55 to +150	°C

Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.

	DC TEST VOLTAGE VALUES (Volts)				
Test Temperature	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
0°C	-0.840	-1.870	-1.145	-1.490	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+75°C	-0.720	-1.830	-1.045	-1.450	-5.2

ELECTRICAL CHARACTERISTICS

Each MECL Memory circuit has been designed to meet the dc and ac specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts.

DC Characteristics	Symbol	MCM10145 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	Conditions
Power Supply Drain Current	I_{EE}	–	130	–	125	–	120	mAdc	Typ I_{EE} @ 25°C = 90 mA All outputs and inputs open. Measure pin 8.
Input Current High	$I_{in}H$	–	220	–	220	–	220	μAdc	Test one input at a time, all other inputs are open. $V_{in} = V_{IH}$.
Input Current Low	$I_{in}L$	0.5	–	0.5	–	0.3	–	μAdc	Test one input at a time, all other inputs are open. $V_{in} = V_{IL}$.
Logic "1" Output Voltage	V_{OH}	-1.000	-0.840	-0.960	-0.810	-0.900	-0.720	Vdc	Load 50 Ω to -2.0 V
Logic "0" Output Voltage	V_{OL}	-1.870	-1.665	-1.850	-1.650	-1.830	-1.625	Vdc	
Logic "1" Threshold Voltage	V_{OHA}	-1.020	–	-0.980	–	-0.920	–	Vdc	Threshold testing is performed and guaranteed on one input at a time. $V_{in} = V_{IHA}$ or V_{ILA}. Load 50 Ω to -2.0 V.
Logic "0" Threshold Voltage	V_{OLA}	–	-1.645	–	-1.630	–	-1.605	Vdc	

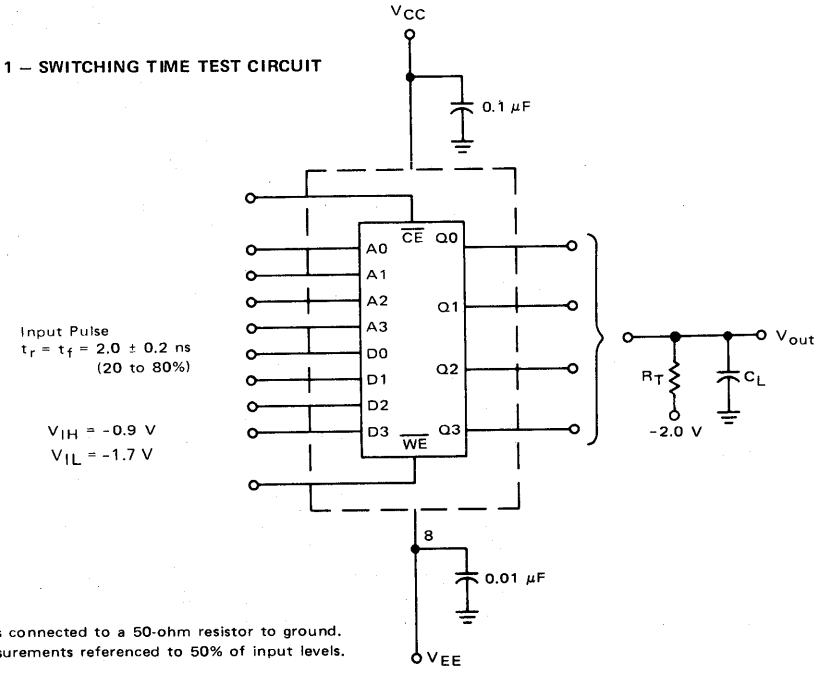
SWITCHING CHARACTERISTICS (T_A = 0° to +75°C, V_{EE} = −5.2 Vdc ±5°; Output Load see Figure 1; see Note 2.)

Characteristic	Symbol	Test Limits Min	Typ	Max	Unit	Conditions
Read Mode						See Figures 2 and 3.
Chip Select Access Time	t_{ACS}	2.0	4.5	8.0	ns	Measured from 50% of input to 50% of
Chip Select Recovery Time	t_{RCS}	2.0	5.0	8.0	ns	output. See Note 1.
Address Access Time	t_{AA}	4.0	10	15	ns	
Write Mode						
Write Pulse Width	t_W	8.0	–	–	ns	t_{WSA} = 5 ns
Data Setup Time Prior to Write	t_{WSD}	0	-6.0	–	ns	Measured at 50% of input to 50% of
Data Hold Time After Write	t_{WHD}	3.0	0	–	ns	output.
Address Setup Time Prior to Write	t_{WSA}	5.0	1.0	–	ns	t_W = 8 ns. See Figure 4.
Address Hold Time After Write	t_{WHA}	1.0	-3.0	–	ns	
Chip Select Setup Time Prior to Write	t_{WSCS}	0	-5.0	–	ns	
Chip Select Hold Time After Write	t_{WHCS}	0	-6.0	–	ns	
Write Disable Time	t_{WS}	2.0	5.0	8.0	ns	
Write Recovery Time	t_{WR}	2.0	5.0	8.0	ns	
Chip Enable Strobe Mode						
Data Setup Prior to Chip Select	t_{CSD}	0	-6.0	–	ns	Guaranteed but not tested on standard
Write Enable Setup Prior to Chip Select	t_{CSW}	0	-3.0	–	ns	product. See Figure 5.
Address Setup Prior to Chip Select	t_{CSA}	0	-3.0	–	ns	
Data Hold Time After Chip Select	t_{CHD}	2.0	-1.0	–	ns	
Write Enable Hold Time After Chip Select	t_{CHW}	0	-6.0	–	ns	
Address Hold Time After Chip Select	t_{CHA}	4.0	-1.0	–	ns	
Chip Select Minimum Pulse Width	t_{CS}	18	12	–	ns	
Rise and Fall Time						Measured between 20% and 80% points.
Address to Output	t_r, t_f	1.5	3.0	7.0	ns	
$\overline{CS}$ to Output	t_r, t_f	1.5	3.0	5.0	ns	
Capacitance						
Input Capacitance	C_{in}	–	4.0	6.0	pF	
Output Capacitance	C_{out}	–	5.0	8.0	pF	

Notes:
1. The maximum Address Access Time is guaranteed to be the worst-case bit in the memory.
2. For proper use of MECL Memories in a system environment, consult MECL System Design Handbook.

5

FIGURE 1 – SWITCHING TIME TEST CIRCUIT



Unused outputs connected to a 50-ohm resistor to ground.
All timing measurements referenced to 50% of input levels.
R_T = 50 Ω
$C_L \leq$ 5.0 pF (Including Jig and Stray Capacitance)
Delay should be derated 30 ps/pF for capacitive loads up to 50 pF.

FIGURE 2 – CHIP SELECT ACCESS TIME

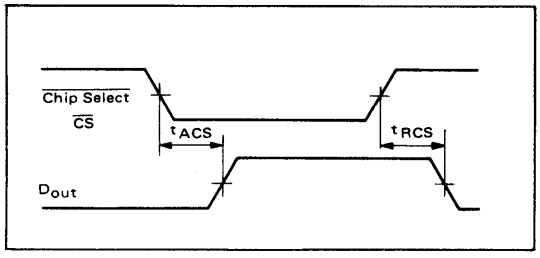


FIGURE 3 – ADDRESS ACCESS TIME

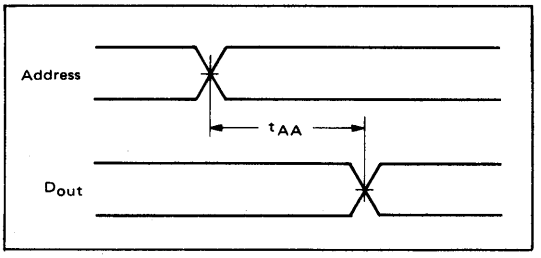


FIGURE 4 – WRITE MODE

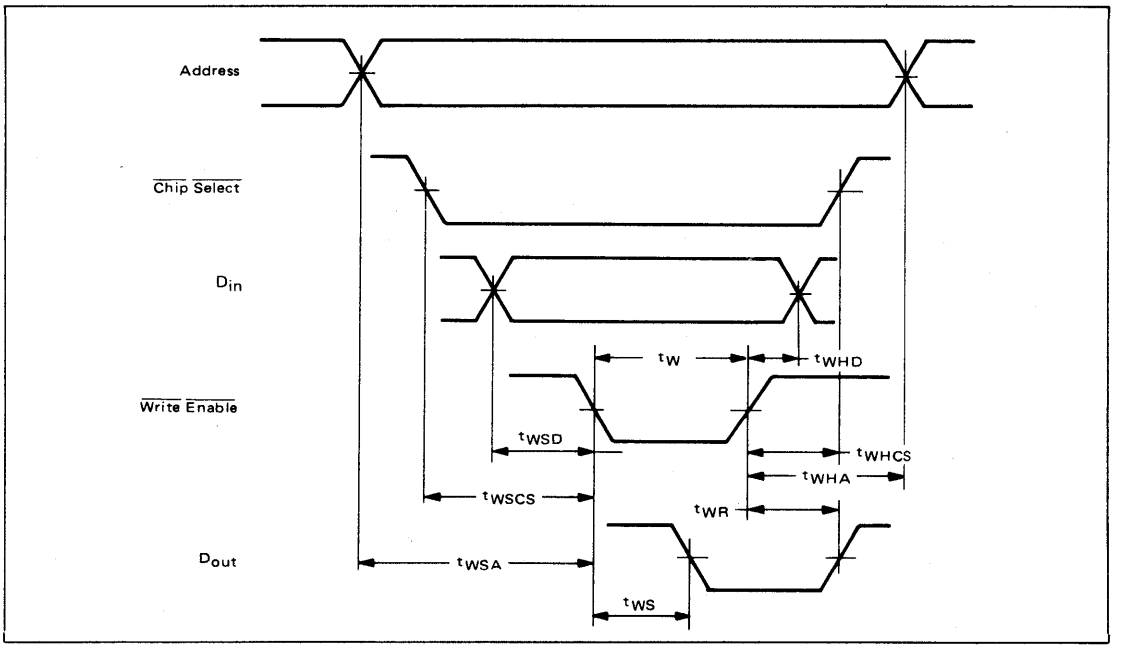
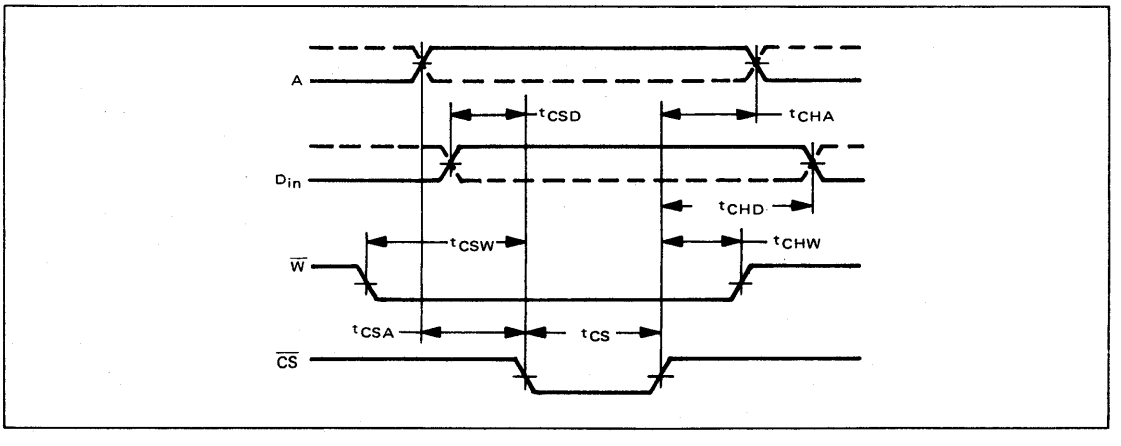


FIGURE 5 – CHIP ENABLE STROBE MODE



MOTOROLA

MCM10146

1024 x 1-BIT RANDOM ACCESS MEMORY

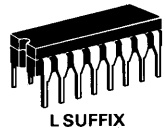
The MCM10146/10415 is a 1024-bit Read/Write Random Access Memory organized 1024 words by 1 bit. Data is selected or stored by means of a 10-bit address (A0 through A9) decoded on the chip. The chip is designed with a separate data in line, a non-inverting data output, and an active-low chip select.

This device is designed for use in high-speed scratch pad, control, cache and buffer storage applications.

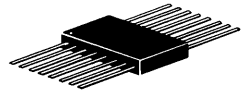
- Fully Compatible with MECL 10,000
- Pin-for-Pin Compatible with the 10415
- Temperature Range of 0° to 75°C (see note 1)
- Emitter-Follower Output Permits Full Wire-ORing (see note 3)
- Power Dissipation Decreases with Increasing Temperature
- Typical Address Access of 24 ns
- Typical Chip Select Access of 4.0 ns

PIN DESIGNATION

CS	Chip Select Input
A0 to A9	Address Inputs
D_{in}	Data Inputs
D_{out}	Data Output
WE	Write Enable Input



L SUFFIX
CERAMIC PACKAGE
CASE 620



F SUFFIX
CERAMIC PACKAGE
CASE 650

ORDERING INFORMATION

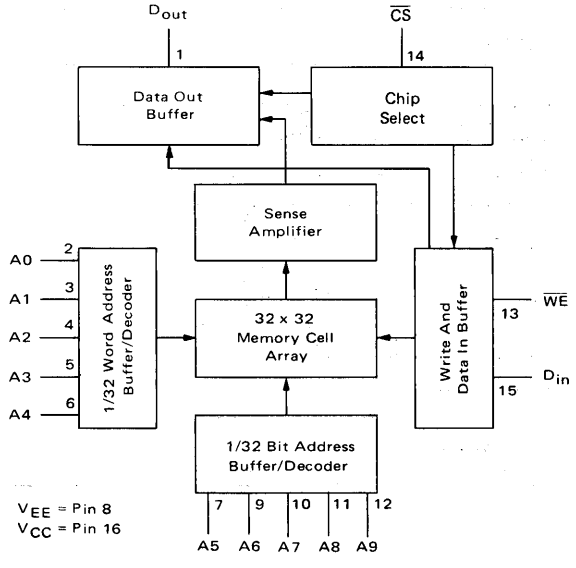
Suffix Denotes

MCM10146 – L Ceramic Dual-in-Line Package
– F Ceramic Flat Package

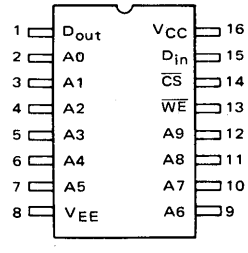
10415 – DC Ceramic Dual-in-Line Package
– FC Ceramic Flat Package

5

BLOCK DIAGRAM



PIN ASSIGNMENT



TRUTH TABLE

MODE	INPUT			OUTPUT
	$\overline{CS}$	$\overline{WE}$	D_{in}	D_{out}
Write "0"	L	L	L	L
Write "1"	L	L	H	L
Read	L	H	ϕ	Q
Disabled	H	ϕ	ϕ	L

ϕ = Don't Care.

FUNCTIONAL DESCRIPTION:

This device is a 1024 x 1-bit RAM. Bit selection is achieved by means of a 10-bit address, A0 to A9.

The active-low chip select is provided for memory expansion up to 2048 words.

The operating mode of the RAM (CS input low) is controlled by the $\overline{WE}$ input. With $\overline{WE}$ low, the chip is in the write mode, the output, D_{out}, is low and the data state present at D_{in} is stored at the selected address. With $\overline{WE}$ high, the chip is in the read mode and the data stored at the selected memory location will be presented non-inverted at D_{out}. (See Truth Table)

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage (V_{CC} = 0)	V_{EE}	-8 to 0	Vdc
Base Input Voltage (V_{CC} = 0)	V_{in}	0 to V_{EE}	Vdc
Output Source Current — Continuous — Surge	I_O	< 50 < 100	mAdc
Junction Operating Temperature	T_J	< 165	°C
Storage Temperature Range	T_{stg}	-55 to +150	°C

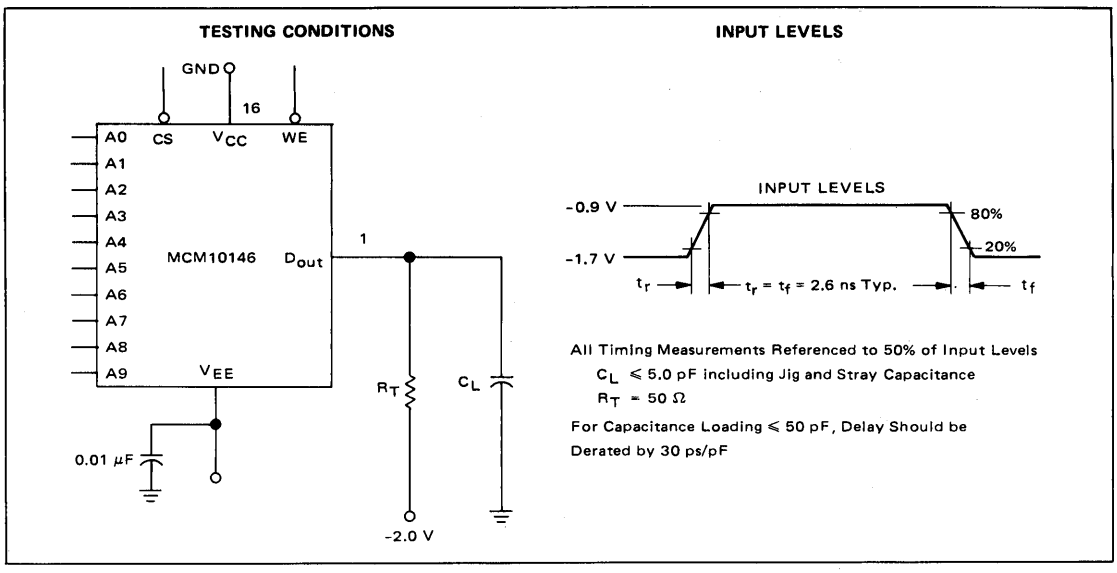
	DC TEST VOLTAGE VALUES (Volts)				
Test Temperature	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
0°C	-0.840	-1.870	-1.145	-1.490	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+75°C	-0.720	-1.830	-1.045	-1.450	-5.2

ELECTRICAL CHARACTERISTICS

Each MECL Memory circuit has been designed to meet the dc and ac specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts.

		MCM10146 Test Limits							
		0°C		+25°C		+75°C			
DC Characteristics	Symbol	Min	Max	Min	Max	Min	Max	Unit	Conditions
Power Supply Drain Current	I_{EE}	–	150	–	145	–	125	mAdc	Typ I_{EE} @ 25°C = 100 mA All outputs and inputs open. Measure pin 8.
Input Current High	$I_{in}H$	–	220	–	220	–	220	μAdc	Test one input at a time, all other inputs are open. $V_{in} = V_{IH}$.
Input Current Low	$I_{in}L$	0.5	–	0.5	–	0.3	–	μAdc	Test one input at a time, all other inputs are open. $V_{in} = V_{IL}$.
Logic "1" Output Voltage	V_{OH}	-1.000	-0.840	-0.960	-0.810	-0.900	-0.720	Vdc	Load 50 Ω to -2.0 V
Logic "0" Output Voltage	V_{OL}	-1.920	-1.665	-1.900	-1.650	-1.880	-1.625	Vdc	
Logic "1" Threshold Voltage	V_{OHA}	-1.020	–	-0.980	–	-0.920	–	Vdc	Threshold testing is performed and guaranteed on one input at a time. $V_{in} = V_{IHA}$ or V_{ILA}. Load 50 Ω to -2.0 V.
Logic "0" Threshold Voltage	V_{OLA}	–	-1.645	–	-1.630	–	-1.605	Vdc	

FIGURE 1 – SWITCHING TEST CIRCUIT AND WAVEFORMS



Guaranteed with V_{EE} = -5.2 Vdc ± 5.0%, T_A = 0°C to 75°C (see Note 1). Output Load see Figure 1.

Characteristic	Symbol	MCM10146 Test Limits Min	Typ	Max	Unit	Conditions
Read Mode						See Figures 2 and 3.
Chip Select Access Time	t_{ACS}	2.0	4.0	7.0	ns	Measured at 50% of input to 50% of output.
Chip Select Recovery Time	t_{RCS}	2.0	4.0	7.0	ns	See Note 2.
Address Access Time	t_{AA}	8.0	24	29	ns	
Write Mode						See Figure 4.
Write Pulse Width (To guarantee writing)	t_W	25	20	–	ns	t_{WSA} = 8.0 ns. Measured at 50% of input to 50% of output.
Data Setup Time Prior to Write	t_{WSD}	5.0	0	–	ns	
Data Hold Time After Write	t_{WHD}	5.0	0	–	ns	
Address Setup Time Prior to Write	t_{WSA}	8.0	0	–	ns	t_W = 25 ns
Address Hold Time After Write	t_{WHA}	2.0	0	–	ns	
Chip Select Setup Time Prior to Write	t_{WSCS}	5.0	0	–	ns	
Chip Select Hold Time After Write	t_{WHCS}	5.0	0	–	ns	
Write Disable Time	t_{WS}	2.8	5.0	7.0	ns	
Write Recovery Time	t_{WR}	2.8	5.0	7.0	ns	
Rise and Fall Time						Measured between 20% and 80% points.
Output Rise and Fall Time	t_r, t_f	1.5	2.5	4.0	ns	When driven from $\overline{CS}$ or $\overline{WE}$ inputs.
Output Rise and Fall Time	t_r, t_f	1.5	4.0	8.0	ns	When driven from Address inputs.
Capacitance						Measured with a pulse technique.
Input Lead Capacitance	C_{in}	–	4.0	5.0	pF	
Output Lead Capacitance	C_{out}	–	7.0	8.0	pF	

Notes:

(1) Contact your Motorola Sales Representative for details if extended temperature operation is desired.

(2) The maximum Address Access Time is guaranteed to be the Worst-Case Bit in the Memory.

(3) For proper use of MECL Memories in a system environment, consult: "MECL System Design Handbook."

(4) Typical limits are at V_{EE} = -5.2 Vdc, T_A = 25°C and standard loading.

FIGURE 2 – CHIP SELECT ACCESS TIME

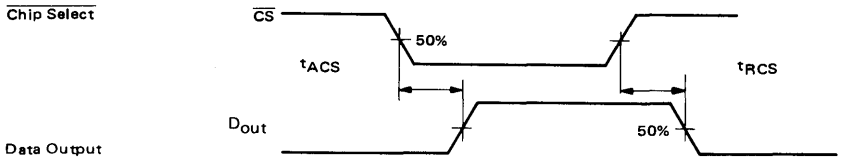


FIGURE 3 – ADDRESS ACCESS TIME

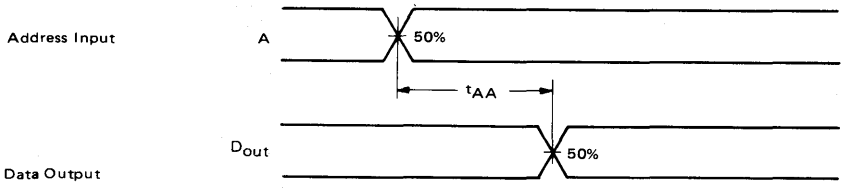
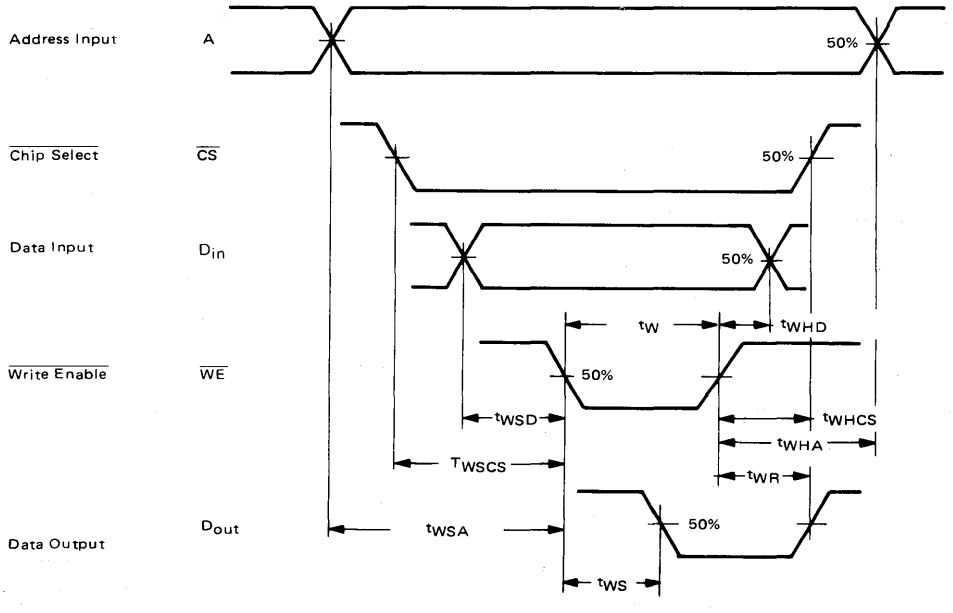


FIGURE 4 – WRITE STROBE MODE



5

MOTOROLA

MCM10147

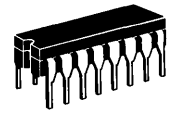
MECL

128-BIT RANDOM ACCESS MEMORY

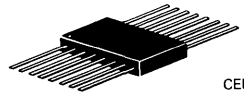
128 x 1-BIT RANDOM ACCESS MEMORY

The MCM10147 is a 128-word x 1-bit Read/Write Random Access Memory. Data is accessed or stored by means of a 7-bit address decoded on chip. It has a non-inverting data out, a separate data in line and 2 active-low chip select lines. It has a typical access time of 10 ns and is designed for high-speed scratch pads, control, cache, and buffer storage applications.

- Typical Address Access Time = 10 ns
- Typical Chip Select Access Time = 5.0 ns
- Operating Temperature Range = 0^{o} to $+75^{o}C$
- Open Emitter Output Permits Wired-OR for Easy Memory Expansion
- 50 kΩ Input Pulldown Resistors on All Inputs
- Power Dissipation Decreases with Increasing Temperature
- Fully Compatible with MECL 10,000 Logic Family
- Similar to F10405.



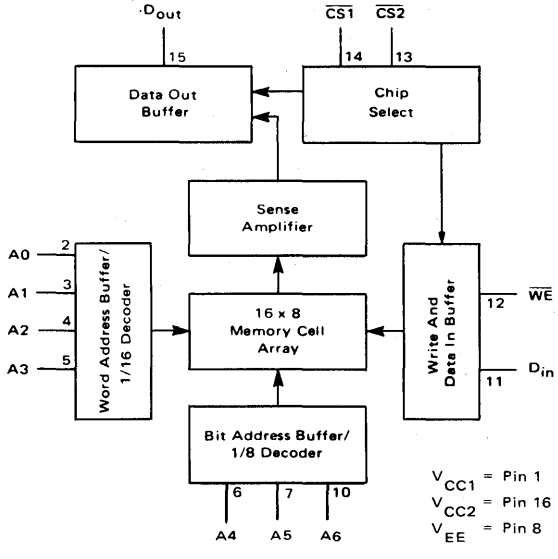
L SUFFIX
CERAMIC PACKAGE
CASE 620



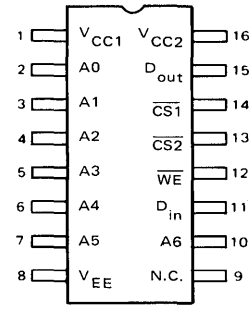
F SUFFIX
CERAMIC PACKAGE
CASE 650

5

BLOCK DIAGRAM



PIN ASSIGNMENT



PIN NOTATION

CS	Chip Select Input
A0 thru A6	Address Inputs
D_{in}	Data Input
D_{out}	Data Output
WE	Write Enable Input

TRUTH TABLE

MODE	INPUT			OUTPUT
	$\overline{CS}$*	$\overline{WE}$	D_{in}	D_{out}
Write "0"	L	L	L	L
Write "1"	L	L	H	L
Read	L	H	ϕ	Q
Disabled	H	ϕ	ϕ	L

*$\overline{CS} = \overline{CS1} + \overline{CS2}$ ϕ = Don't Care.

FUNCTIONAL DESCRIPTION:

The MCM 10147 is a 128 word x 1-bit RAM. Bit selection is achieved by means of a 7-bit address A0 thru A6.

The active-low chip select allows memory expansion up to 512 words. The fast chip select access time allows memory expansion without affecting system performance.

The operating mode of the RAM ($\overline{CS}$ inputs low) is controlled by the $\overline{WE}$ input. With $\overline{WE}$ low the chip is in the write mode—the output is low and the data present at D_{in} is stored at the selected address. With $\overline{WE}$ high the chip is in the read mode—the data state at the selected memory location is presented non-inverted at D_{out}.

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage (V_{CC} = 0)	V_{EE}	-8 to 0	Vdc
Base Input Voltage (V_{CC} = 0)	V_{in}	0 to V_{EE}	Vdc
Output Source Current — Continuous — Surge	I_O	< 50 < 100	mAdc
Junction Operating Temperature	T_J	< 165	°C
Storage Temperature Range	T_{stg}	-55 to +150	°C

Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.

	DC TEST VOLTAGE VALUES (Volts)				
Test Temperature	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
0°C	-0.840	-1.870	-1.145	-1.490	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+75°C	-0.720	-1.830	-1.045	-1.450	-5.2

ELECTRICAL CHARACTERISTICS

Each MECL Memory circuit has been designed to meet the dc and ac specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts.

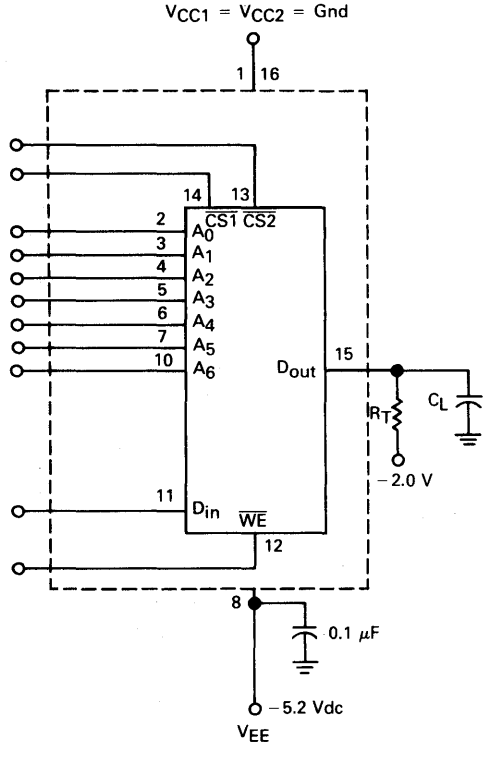
		MCM10144 Test Limits							
		0°C		+25°C		+75°C			
DC Characteristics	Symbol	Min	Max	Min	Max	Min	Max	Unit	Conditions
Power Supply Drain Current	I_{EE}	—	105	—	100	—	95	mAdc	Typ I_{EE} @ 25°C = 80 mA All outputs and inputs open. Measure pin 8.
Input Current High	$I_{in}H$	—	220	—	220	—	220	μAdc	Test one input at a time, all other inputs are open. $V_{in} = V_{IH}$.
Input Current Low	$I_{in}L$	0.5	—	0.5	—	0.3	—	μAdc	Test one input at a time, all other inputs are open. $V_{in} = V_{IL}$.
Logic "1" Output Voltage	V_{OH}	-1.000	-0.840	-0.960	-0.810	-0.900	-0.720	Vdc	Load 50 Ω to -2.0 V
Logic "0" Output Voltage	V_{OL}	-1.870	-1.665	-1.850	-1.650	-1.830	-1.625	Vdc	
Logic "1" Threshold Voltage	V_{OHA}	-1.020	—	-0.980	—	-0.920	—	Vdc	Threshold testing is performed and guaranteed on one input at a time. $V_{in} = V_{IHA}$ or V_{ILA}. Load 50 Ω to -2.0 V.
Logic "0" Threshold Voltage	V_{OLA}	—	-1.645	—	-1.630	—	-1.605	Vdc	

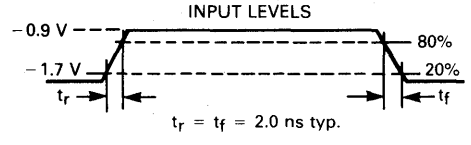
SWITCHING CHARACTERISTICS (T_A = 0° to +75°C, V_{EE} = -5.2 Vdc ± 5%; Output Load see Figure 1; see Note 1 & 3.)

Characteristic	Symbol	Test Limits Min	Typ	Max	Unit	Conditions
Read Mode						See Figures 2 and 3.
Chip Select Access Time	t_{ACS}	2.0	5.0	8.0	ns	Measured from 50% of input to 50% of
Chip Select Recovery Time	t_{RCS}	2.0	5.0	8.0	ns	output. See Note 2.
Address Access Time	t_{AA}	5.0	10	15	ns	
Write Mode						
Write Pulse Width	t_W	8.0	6.0	–	ns	t_{WSA} = 4.0 ns
Data Setup Time Prior to Write	t_{WSD}	1.0	-5.0	–	ns	
Data Hold Time After Write	t_{WHD}	3.0	-2.0	–	ns	
Address Setup Time Prior to Write	t_{WSA}	4.0	0	–	ns	t_W = 8.0 ns. See Figure 4.
Address Hold Time After Write	t_{WHA}	3.0	0	–	ns	
Chip Select Setup Time Prior to Write	t_{WSCS}	1.0	-5.0	–	ns	
Chip Select Hold Time After Write	t_{WHCS}	1.0	-5.0	–	ns	
Write Disable Time	t_{WS}	2.0	5.0	8.0	ns	Measured at 50% of input to 50%
Write Recovery Time	t_{WR}	2.0	5.0	8.0	ns	of output.
Rise and Fall Time						Measured between 20% and 80% points.
Output Rise and Fall Time	t_r, t_f	1.5	3.0	5.0	ns	
Capacitance						
Input Capacitance	C_{in}	–	4.0	5.0	pF	
Output Capacitance	C_{out}	–	7.0	8.0	pF	

Notes: (1) Contact your Motorola Sales Representative for details if extended temperature operation is desired.
(2) The maximum Address Access Time is guaranteed to be the Worst-Case Bit in the Memory.
(3) For proper use of MECL Memories in a system environment, consult: "MECL System Design Handbook."

FIGURE 1 — SWITCHING TIME TEST CIRCUIT





$t_r = t_f$ = 2.0 ns typ.

All timing measurements referenced to 50% of input levels.
R_T = 50 Ω
$C_L \leq$ 5.0 pF (including jig and stray capacitance)
Delay should be derated 30 ps/pF for capacitive load up to 50 pF

FIGURE 2 – CHIP SELECT ACCESS TIME

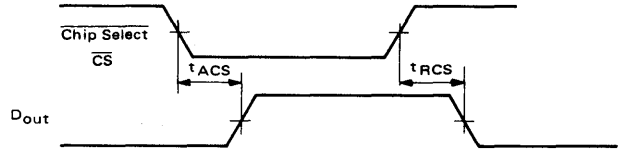


FIGURE 3 – ADDRESS ACCESS TIME

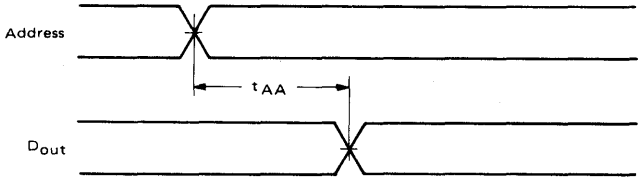
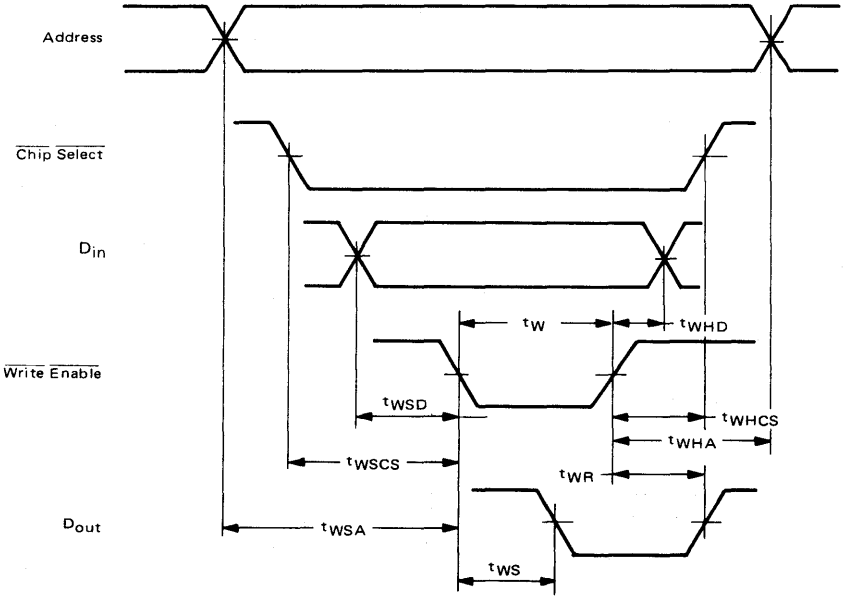


FIGURE 4 – WRITE MODE



5

MOTOROLA

MCM10149

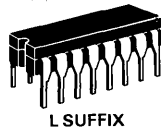
MECL

1024-BIT PROGRAMMABLE READ-ONLY MEMORY

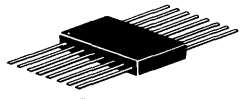
256 x 4-BIT PROGRAMMABLE READ-ONLY MEMORY

This device is a 256-word x 4-bit field programmable read only memory (PROM). Prior to programming, all stored bits are at logic 1 (high) levels. The logic state of each bit can then be changed by on-chip programming circuitry. The memory has a single negative logic chip enable. When the chip is disabled ($\overline{CS}$ = high), all outputs are forced to a logic 0 (low).

- Typical Address Access Time of 20 ns
- Typical Chip Select Access Timeof 8.0 ns
- 50 kΩ Input Pulldown Resistors on All Inputs
- Power Dissipation (540 mW typ @25°C)
  Decreases with Increasing Temperature

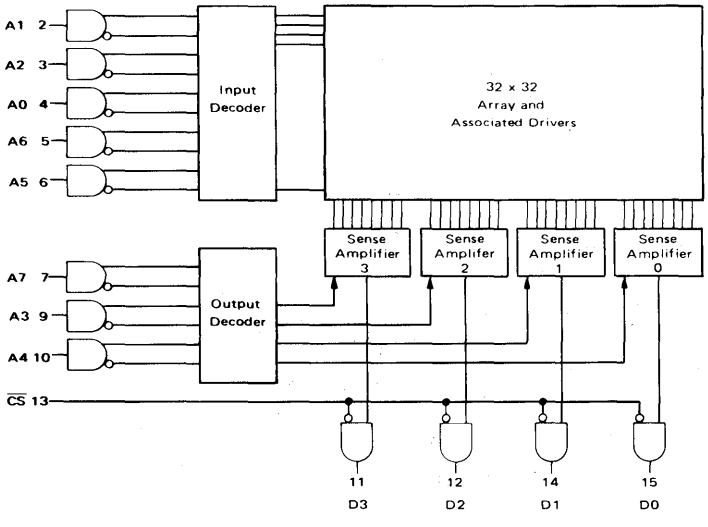


L SUFFIX
CERAMIC PACKAGE
CASE 620

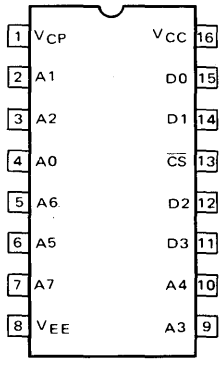


F SUFFIX
CERAMIC PACKAGE
CASE 650

5



PIN ASSIGNMENT



ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	−55°C		0°C		+25°C		+75°C		+125°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_{EE}	–	160	–	155	–	150	–	145	–	145	mAdc
Input Current High	I_{inH}	–	450	–	265	–	265	–	265	–	265	μAdc

-55°C and +125°C test values apply to MC105xx devices only.

Forcing Function	Parameter	-55°C ①	0°C ②	25°C ②	25°C ①	75°C ②	125°C ①
		MCM10500	MCM10100	MCM10100	MCM10500	MCM10100	MCM10500
V_{IHmax} =	V_{OHmax}	−0.880	−0.840	−0.810	−0.780	−0.720	−0.630
	V_{OHmin}	−1.080	−1.000	−0.960	−0.930	−0.900	−0.825
	V_{OHAmin}	−1.100	−1.020	−0.980	−0.950	−0.920	−0.845
V_{IHAmin}		−1.175	−1.130	−1.105	−1.105	−1.045	−1.000
V_{ILAmax}		−1.510	−1.490	−1.475	−1.475	−1.450	−1.400
	V_{OLAmax}	−1.635	−1.645	−1.630	−1.600	−1.605	−1.525
	V_{OLmax}	−1.655	−1.665	−1.650	−1.620	−1.625	−1.545
V_{ILmin} =	V_{OLmin}	−1.920	−1.870	−1.850	−1.850	−1.830	−1.820
V_{ILmin}	I_{NLmin}	0.5	0.5	0.5	0.5	0.3	0.3

NOTES: ① MCM10500 series specified driving 100Ω to −2.0 V.
② Memories (MCM10100) specified 0 - 75°C for commercial temperature range, 50Ω to -2.0V. Military temperature range memories (MCM10500) specified per Note 1.

SWITCHING CHARACTERISTICS (Note 1)

Characteristics	Symbol	MCM10149 T_A = 0 to +75°C, V_{EE} = −5.2 Vdc ± 5%		MCM10549 T_A = −55 to +125°C, V_{EE} = −5.2 Vdc ± 5%		Unit	Conditions
		Min	Max	Min	Max		
Read Mode						ns	Measured from 50% of input to 50% of output. See Note 1.
Chip Select Access Time	t_{ACS}	2.0	10	*	*		
Chip Select Recovery Time	t_{RCS}	2.0	10	*	*		
Address Access Time	t_{AA}	7.0	25	*	*		
Rise and Fall Time	t_r, t_f	1.5	7.0	*	*	ns	Measured between 20% and 80% points.
Capacitance						pF	Measured with a pulse technique.
Input Capacitance	C_{in}	–	5.0	–	5.0		
Output Capacitance	C_{out}	–	8.0	–	8.0		

NOTES: 1. Test circuit characteristics: R_T = 50 Ω, MCM10149; 100 Ω, MCM10549.
$C_L \leq 5.0$ pF (including jig and stray capacitance)
Delay should be derated 30 ps/pF for capacitive load up to 50 pF
2. The maximum Address Access Time is guaranteed to be the Worst-Case Bit in the Memory.
3. For proper use of MECL Memories in a system environment, consult MECL System Design Handbook.
4. $V_{CP} = V_{CC}$ = Gnd for normal operation.

*To be determined; contact your Motorola representative for up-to-date information.

PROGRAMMING THE MCM10149 †

During programming of the MCM 10149, input pins 7, 9, and 10 are addressed with standard MECL 10K logic levels. However, during programming input pins 2, 3, 4, 5, and 6 are addressed with $0 \text{ V} \leq V_{IH} \leq +0.25$ V and $V_{EE} \leq V_{IL} \leq -3.0$ V. It should be stressed that this deviation from standard input levels is required only during the programming mode. During normal operation, standard MECL 10,000 input levels must be used.

With these requirements met, and with $V_{CP} = V_{CC} =$ 0 V and $V_{EE} = -5.2$ V ± 5%, the address is set up. After a minimum of 100 ns delay, V_{CP} (pin 1) is ramped up to + 12 V ± 0.5 V (total voltage V_{CP} to V_{EE} is now 17.2 V, + 12 V − [− 5.2 V]). The rise time of this V_{CP} voltage pulse should be in the 1 − 10 μs range, while its pulse width (t_{W1}) should be greater than 100 μs but less than 1 ms. The V_{CP} supply current at + 12 V will be approximately 525 mA while current drain from V_{CC} will be approximately 175 mA. A current limit should therefore be

set on both of these supplies. The current limit on the V_{CP} supply should be set at 700 mA while the V_{CC} supply should be limited to 250 mA. It should be noted that the V_{EE} supply must be capable of sinking the combined current of the V_{CC} and V_{CP} supplies while maintaining a voltage of – 5.2 V ± 5%.

Coincident with, or at some delay after the V_{CP} pulse has reached its 100% level, the desired bit to be fused can be selected. This is done by taking the corresponding output pin to a voltage of + 2.85 V ± 5%. It is to be noted that only one bit is to be fused at a time. The other three unselected outputs should remain terminated through their 50 ohm load resistor (100 ohm for MCM 10549) to – 2.0 V. Current into the selected output is 5 mA maximum.

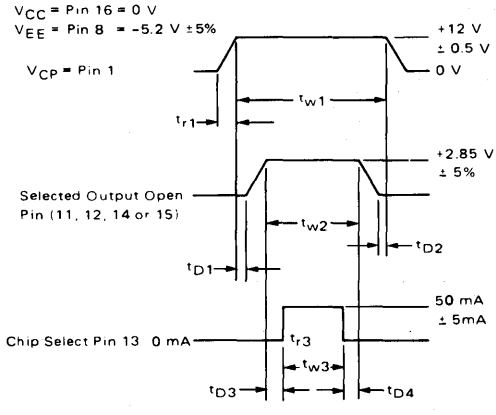
After the bit select pulse has been applied to the appropriate output, the fusing current is sourced out of the chip select pin 13. The 0% to 100% rise time of this current pulse should be 250 ns max. It pulse width should be greater than 100 μs. Pulse magnitude is 50 mA ± 5.0 mA. The voltage clamp on this current source is to be – 6.0 V.

After the fusing current source has returned 0 mA, the bit select pulse is returned to it initial level, i.e., the output is returned through its load to – 2.0 V. Thereafter, V_{CP} is returned to 0 V. Strobing of the outputs to determine success in programming should occur no sooner than 100 ns after V_{CP} has returned to 0 V. The remaining bits are programmed in a similar fashion.

† NOTE: For devices that program incorrectly, return serialized units with individual truth tables. Non compliance voids warranty.

PROGRAMMING SPECIFICATIONS

The following timing diagrams and fusing information represent programming specifications for the MCM10149.



The timing diagram is shown for programming one bit. Note that only one bit is blown at a time. All addressing must be done 100 ns prior to the beginning of the V_{CP} pulse, i.e., V_{CP} = 0 V. Likewise, strobing of the outputs to determine success in programming should occur no sooner than 100 ns after V_{CP} returns to 0 V.

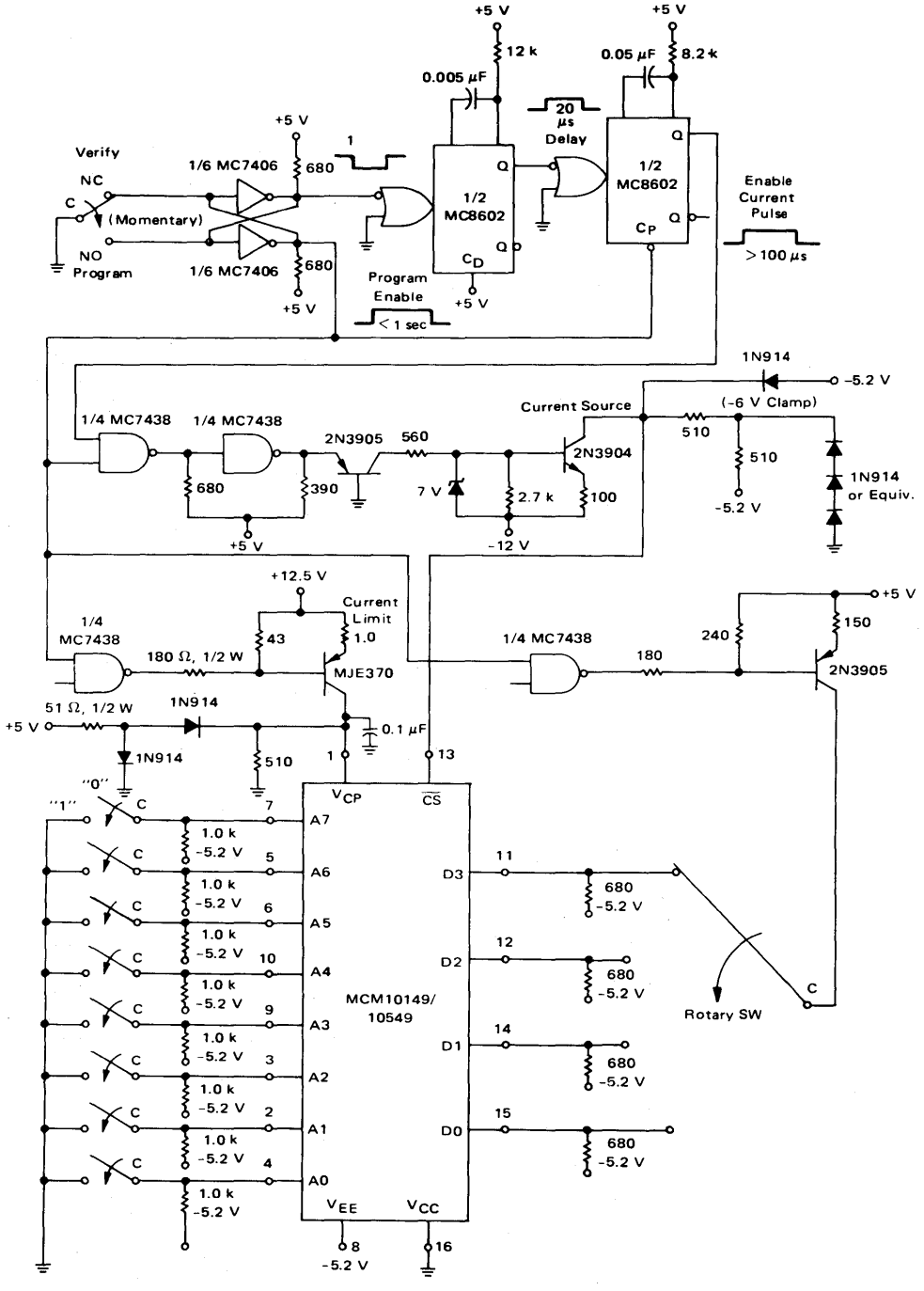
Note that the fusing current is defined as a positive current out of the chip select, pin 13. A programming duty cycle of ⩽ 15% is to be observed.

Definitions and values of timing symbols are as follows.

Symbol	Definition	Value
t_{r1}	Rise Time, Programming Voltage	⩾ 1 μs
t_{w1}	Pulse Width, Programming Voltage	⩾ 100 μs < 1 ms
t_{D1}	Delay Time, Programming Voltage Pulse to Bit Select Pulse	⩾ 0
t_{w2}	Pulse Width, Bit Select	⩾ 100 μs
t_{D2}	Delay Time, Bit Select Pulse to Programming Voltage Pulse	⩾ 0
t_{D3}	Delay Time, Bit Select Pulse to Programming Current Pulse	⩾ 1 μs
t_{r3}	Rise Time, Programming Current Pulse	250 ns max
t_{w3}	Pulse Width, Programming Current Pulse	⩾ 100 μs
t_{D4}	Delay Time, Programming Current Pulse to Bit Select Pulse	⩾ 1 μs

5

MANUAL PROGRAMMING CIRCUIT



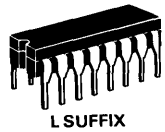
MOTOROLA

MCM10152

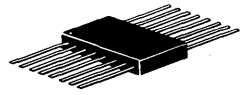
256 x 1-BIT RANDOM ACCESS MEMORY

The MCM10152 is a 256 word x 1-bit Read/Write Random Access Memory. Data is accessed or stored by means of an 8-bit address decoded on chip. It has a non-inverting data out, a separate data in line and 3 active-low chip select lines. It has a typical access time of 11 ns and is designed for high-speed scratch pad, control, cache, and buffer storage applications.

- Typical Address Access Time = 11 ns
- Typical Chip Select Access Time = 4.0 ns
- Operating Temperature Range = 0° to +75°C
- Open Emitter Output Permits Wired-OR for Easy Memory Expansion
- 50 kΩ Input Pulldown Resistors on All Inputs
- Power Dissipation Decreases with Increasing Temperature
- Fully Compatible with MECL 10,000 Logic Family



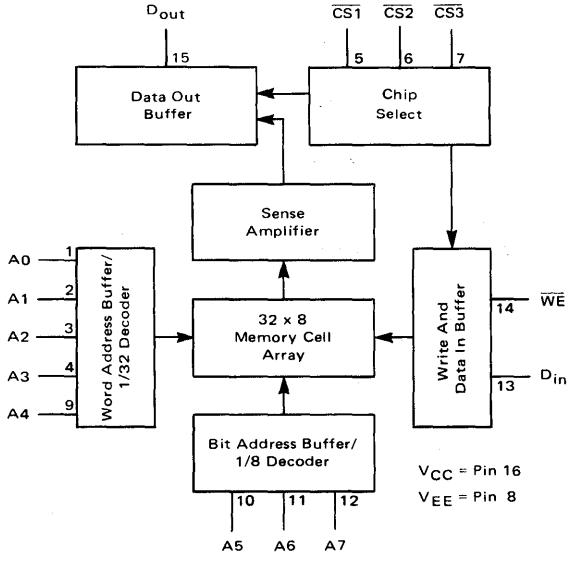
L SUFFIX
CERAMIC PACKAGE
CASE 620



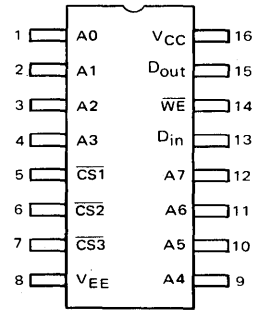
F SUFFIX
CERAMIC PACKAGE
CASE 650

5

BLOCK DIAGRAM



PIN ASSIGNMENT



PIN NOTATION

CS	Chip Select Input
A0 thru A7	Address Inputs
D_{in}	Data Input
D_{out}	Data Output
WE	Write Enable Input

TRUTH TABLE

MODE	INPUT			OUTPUT
	$\overline{CS}$*	$\overline{WE}$	D_{in}	D_{out}
Write "0"	L	L	L	L
Write "1"	L	L	H	L
Read	L	H	ϕ	Q
Disabled	H	ϕ	ϕ	L

*$\overline{CS} = \overline{CS1} + \overline{CS2} + \overline{CS3}$ ϕ = Don't Care.

FUNCTIONAL DESCRIPTION:

The MCM10152 is a 256 word x 1-bit RAM. Bit selection is achieved by means of an 8-bit address A0 thru A7.

The active-low chip select allows memory expansion up to 2048 words. The fast chip select access time allows memory expansion without affecting system performance.

The operating mode of the RAM ($\overline{CS}$ inputs low) is controlled by the $\overline{WE}$ input. With $\overline{WE}$ low the chip is in the write mode—the output is low and the data present at D_{in} is stored at the selected address. With $\overline{WE}$ high the chip is in the read mode—the data state at the selected memory location is presented non-inverted at D_{out}.

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage (V_{CC} = 0)	V_{EE}	-8 to 0	Vdc
Base Input Voltage (V_{CC} = 0)	V_{in}	0 to V_{EE}	Vdc
Output Source Current — Continuous — Surge	I_O	< 50 < 100	mAdc
Junction Operating Temperature	T_J	< 165	°C
Storage Temperature Range	T_{stg}	-55 to +150	°C

Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.

	DC TEST VOLTAGE VALUES (Volts)				
Test Temperature	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
0°C	-0.840	-1.870	-1.145	-1.490	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+75°C	-0.720	-1.830	-1.045	-1.450	-5.2

ELECTRICAL CHARACTERISTICS

Each MECL Memory circuit has been designed to meet the dc and ac specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts.

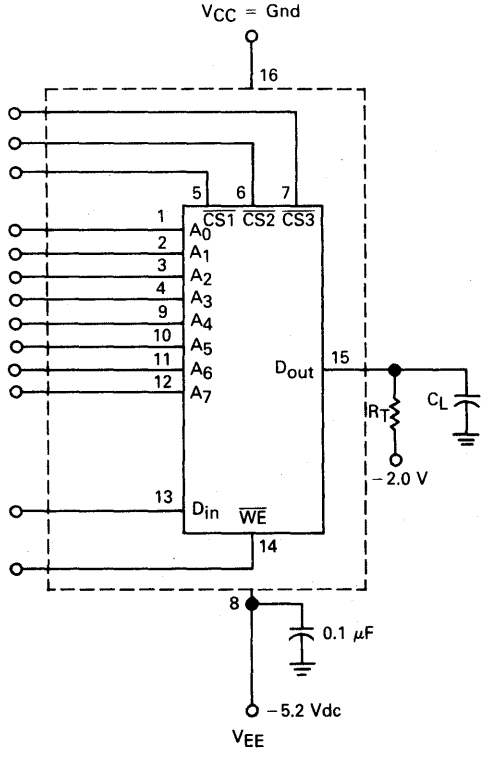
		MCM10152 Test Limits							
		0°C		+25°C		+75°C			
DC Characteristics	Symbol	Min	Max	Min	Max	Min	Max	Unit	Conditions
Power Supply Drain Current	I_{EE}	–	135	–	130	–	125	mAdc	Typ I_{EE} @ 25°C = 110 mA All outputs and inputs open. Measure pin 8.
Input Current High	$I_{in}H$	–	220	–	220	–	220	μAdc	Test one input at a time, all other inputs are open. $V_{in} = V_{IH}$.
Input Current Low	$I_{in}L$	0.5	–	0.5	–	0.3	–	μAdc	Test one input at a time, all other inputs are open. $V_{in} = V_{IL}$.
Logic "1" Output Voltage	V_{OH}	-1.000	-0.840	-0.960	-0.810	-0.900	-0.720	Vdc	Load 50 Ω to -2.0 V
Logic "0" Output Voltage	V_{OL}	-1.870	-1.665	-1.850	-1.650	-1.830	-1.625	Vdc	
Logic "1" Threshold Voltage	V_{OHA}	-1.020	–	-0.980	–	-0.920	–	Vdc	Threshold testing is performed and guaranteed on one input at a time. $V_{in} = V_{IHA}$ or V_{ILA}. Load 50 Ω to -2.0 V.
Logic "0" Threshold Voltage	V_{OLA}	–	-1.645	–	-1.630	–	-1.605	Vdc	

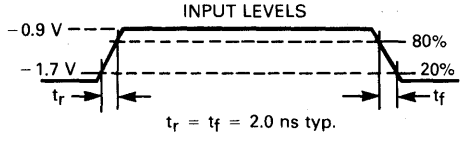
SWITCHING CHARACTERISTICS (T_A = 0° to +75°C, V_{EE} = -5.2 Vdc ± 5%; Output Load see Figure 1; see Note 1 & 3.)

Characteristic	Symbol	Test Limits Min	Typ	Max	Unit	Conditions
Read Mode						See Figures 2 and 3.
Chip Select Access Time	t_{ACS}	2.0	4.0	7.5	ns	Measured from 50% of input to 50% of
Chip Select Recovery Time	t_{RCS}	2.0	4.0	7.5	ns	output. See Note 2.
Address Access Time	t_{AA}	7.0	11	15	ns	
Write Mode						
Write Pulse Width	t_W	10	6.0	–	ns	t_{WSA} = 5.0 ns
Data Setup Time Prior to Write	t_{WSD}	2.0	-3.0	–	ns	Measured at 50% of input to 50% of
Data Hold Time After Write	t_{WHD}	2.0	-2.0	–	ns	output.
Address Setup Time Prior to Write	t_{WSA}	5.0	3.0	–	ns	t_W = 10 ns. See Figure 4.
Address Hold Time After Write	t_{WHA}	3.0	0	–	ns	
Chip Select Setup Time Prior to Write	t_{WSCS}	2.0	-3.0	–	ns	
Chip Select Hold Time After Write	t_{WHCS}	2.0	-3.0	–	ns	
Write Disable Time	t_{WS}	2.5	5.0	7.5	ns	
Write Recovery Time	t_{WR}	2.5	5.0	7.5	ns	
Rise and Fall Time						Measured between 20% and 80% points.
Output Rise and Fall Time	t_r, t_f	1.5	3.0	5.0	ns	
Capacitance						
Input Capacitance	C_{in}	–	4.0	5.0	pF	
Output Capacitance	C_{out}	–	7.0	8.0	pF	

Notes: (1) Contact your Motorola Sales Representative for details if extended temperature operation is desired.
(2) The maximum Address Access Time is guaranteed to be the Worst-Case Bit in the Memory.
(3) For proper use of MECL Memories in a system environment, consult: "MECL System Design Handbook."

FIGURE 1 — SWITCHING TIME TEST CIRCUIT





$t_r = t_f$ = 2.0 ns typ.

All timing measurements referenced to 50% of input levels.
R_T = 50 Ω
$C_L \leq$ 5.0 pF (including jig and stray capacitance)
Delay should be derated 30 ps/pF for capacitive load up to 50 pF

FIGURE 2 – CHIP SELECT ACCESS TIME

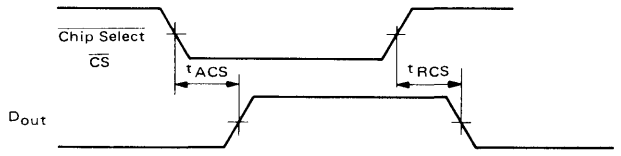


FIGURE 3 – ADDRESS ACCESS TIME

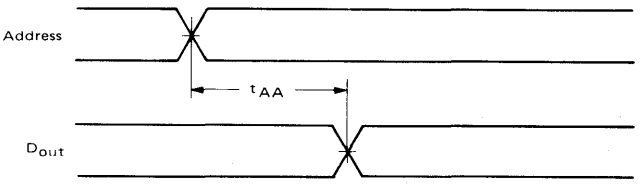
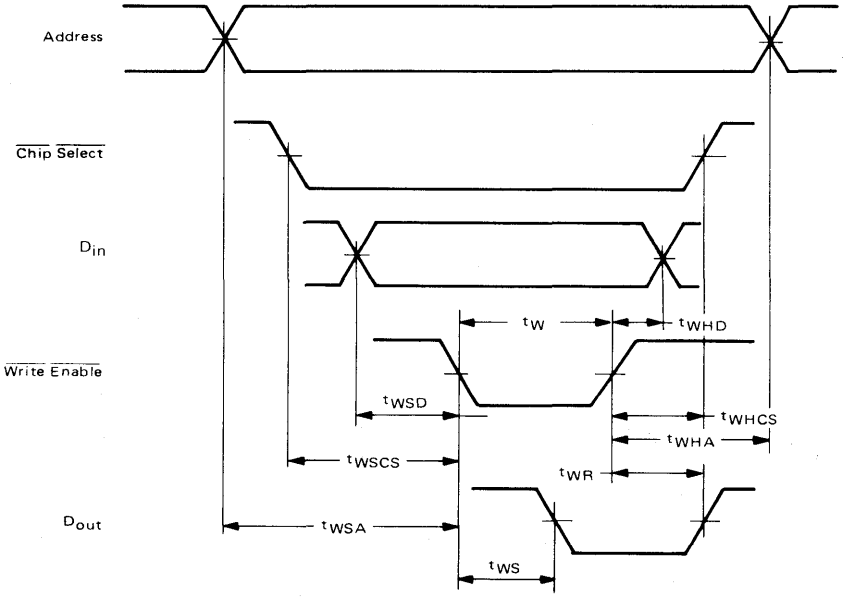


FIGURE 4 – WRITE MODE



MOTOROLA

MCM10415-15
MCM10415-20

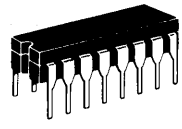
MECL 1024-BIT RANDOM ACCESS MEMORY

1024 x 1-BIT RANDOM ACCESS MEMORY

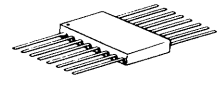
The MCM10415 is a 1024-bit Read/Write Random Access Memory organized 1024 words by 1 bit. Data is selected or stored by means of a 10-bit address (A0 through A9) decoded on the chip. The chip is designed with a separate data in line, a noninverting data output, and an active-low chip select.

This device is designed for use in high-speed scratch pad, control, cache and buffer storage applications.

- Address Access Time: MCM10415-20 20 ns (Max)
  MCM10415-15 15 ns (Max)
- Fully Compatible with MECL 10K/10KH
- Temperature Range of 0° to 75°C
- Emitter-Follower Output Permits Full Wire-ORing
- Power Dissipation Decreases with Increasing Temperature



L SUFFIX
CERAMIC PACKAGE
CASE 620

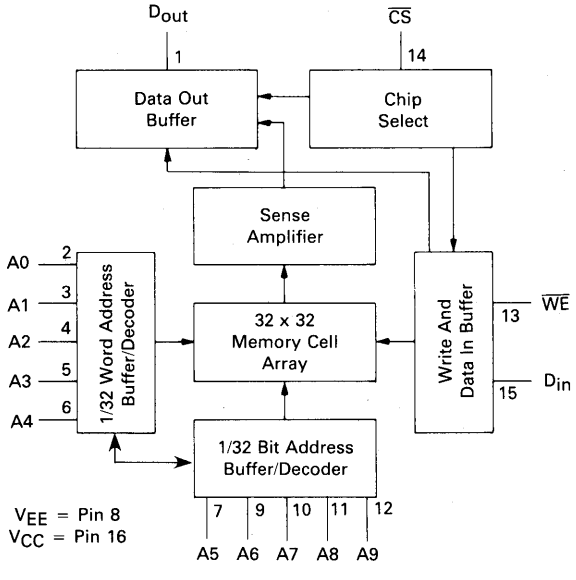


F SUFFIX
CERAMIC PACKAGE
CASE 650

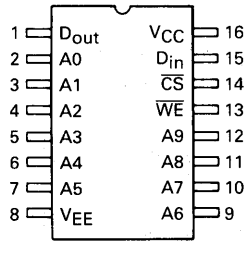
ORDERING INFORMATION
Suffix Denotes
MCM10415L15 — Ceramic Dual-in-Line Package
MCM10415F15 — Ceramic Flat Package
MCM10415L20 — Ceramic Dual-in-Line Package
MCM10415F20 — Ceramic Flat Package

5

BLOCK DIAGRAM



PIN ASSIGNMENT



PIN DESIGNATION

$\overline{CS}$	Chip Select Input
A0 to A9	Address Inputs
D_{in}	Data Inputs
D_{out}	Data Output
$\overline{WE}$	Write Enable Input

FUNCTIONAL DESCRIPTION:

This device is a 1024 x 1-bit RAM. Bit selection is achieved by means of a 10-bit address, A0 to A9.

The active-low chip select is provided for memory expansion up to 2048 words.

The operating mode of the RAM (CS input low) is controlled by the $\overline{WE}$ input. With $\overline{WE}$ low, the chip is in the write mode, the output, D_{out}, is low and the data state present at D_{in} is stored at the selected address. With $\overline{WE}$ high, the chip is in the read mode and the data stored at the selected memory location will be presented noninverted at D_{out}. (See Truth Table)

TRUTH TABLE

MODE	INPUT			OUTPUT
	$\overline{CS}$	$\overline{WE}$	D_{in}	D_{out}
Write "0"	L	L	L	L
Write "1"	L	L	H	L
Read	L	H	ϕ	Q
Disabled	H	ϕ	ϕ	L

ϕ = Don't Care.

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage (V_{CC} = 0)	V_{EE}	−8 to 0	Vdc
Base Input Voltage (V_{CC} = 0)	V_{in}	0 to V_{EE}	Vdc
Output Source Current — Continuous — Surge	I_O	<50 <100	mAdc
Junction Operating Temperature	T_J	<165	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C

	DC TEST VOLTAGE VALUES (Volts)				
Test Temperature	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
0°C	−0.840	−1.870	−1.145	−1.490	−5.2
+25°C	−0.810	−1.850	−1.105	−1.475	−5.2
+75°C	−0.720	−1.830	−1.045	−1.450	−5.2

ELECTRICAL CHARACTERISTICS

Each MECL Memory circuit has been designed to meet the dc and ac specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts.

		MCM10415 Test Limits							
		0°C		+25°C		+75°C			
DC Characteristics	Symbol	Min	Max	Min	Max	Min	Max	Unit	Conditions
Power Supply Drain Current	I_{EE}	—	150	—	145	—	125	mAdc	Typ I_{EE} @ 25°C = 100 mA All outputs and inputs open. Measure Pin 8.
Input Current High	I_{inH}	—	220	—	220	—	220	μAdc	Test one input at a time, all other inputs are open. $V_{in} = V_{IH}$.
Input Current Low ($\overline{CS}$ only) Input Curent Low (All Others)	I_{inL}	0.5 −50	—	0.5 −50	—	0.3 −50	—	μAdc	Test one input at a time, all other inputs are open. $V_{in} = V_{IL}$.
Logic "1" Output Voltage	V_{OH}	−1.000	−0.840	−0.960	−0.810	−0.900	−0.720	Vdc	Load 50 Ω to −2.0 V
Logic "0" Output Voltage	V_{OL}	−1.870	−1.665	−1.850	−1.650	−1.830	−1.625	Vdc	
Logic "1" Threshold Voltage	V_{OHA}	−1.020	—	−0.980	—	−0.920	—	Vdc	Threshold testing is performed and guaranteed on one input at a time. $V_{in} = V_{IHA}$ or V_{ILA}. Load 50 Ω to −2.0 V.
Logic "0" Threshold Voltage	V_{OLA}	—	−1.645	—	−1.630	—	−1.605	Vdc	

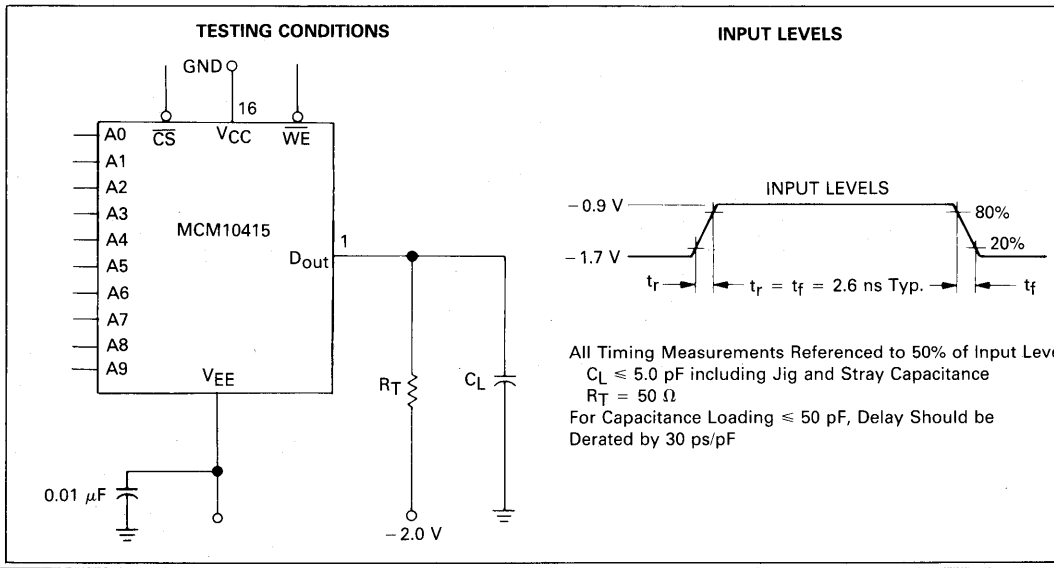
Guaranteed with V_{EE} = −5.2 Vdc ±5.0%, T_A = 0°C to 75°C (see Note 1). Output Load see Figure 1.

Characteristic	Symbol	MCM10415-20 Min	MCM10415-20 Max	MCM10415-15 Min	MCM10415-15 Max	Unit	Conditions
Read Mode							See Figures 2 and 3.
Chip Select Access Time	t_{ACS}	—	8.0	—	7.0	ns	Measured at 50% of input to 50% of output.
Chip Select Recovery Time	t_{RCS}	—	8.0	—	7.0	ns	See Note 2.
Address Access Time	t_{AA}	—	20	—	15	ns	
Write Mode							See Figure 4.
Write Pulse Width (To guarantee writing)	t_W	14	—	12	—	ns	t_{WSA} = 3.0 ns — MCM10415-20 t_{WSA} = 2.0 ns — MCM10415-15 Measured at 50% of input to 50% of output.
Data Setup Time Prior to Write	t_{WSD}	3.0	—	2.0	—	ns	
Data Hold Time After Write	t_{WHD}	3.0	—	1.0	—	ns	
Address Setup Time Prior to Write	t_{WSA}	3.0	—	2.0	—	ns	t_W = 14 ns — MCM10415-20 t_W = 12 ns — MCM10415-15
Address Hold Time After Write	t_{WHA}	3.0	—	1.0	—	ns	
Chip Select Setup Time Prior to Write	t_{WSCS}	3.0	—	2.0	—	ns	
Chip Select Hold Time After Write	t_{WHCS}	3.0	—	1.0	—	ns	
Write Disable Time	t_{WS}	—	8.0	—	7.0	ns	
Write Recovery Time	t_{WR}	—	8.0	—	7.0	ns	
Rise and Fall Time							Measured between 20% and 80% points.
Output Rise and Fall Time	t_r, t_f	1.5	4.0	1.5	4.0	ns	When driven from $\overline{CS}$ or $\overline{WE}$ inputs.
Output Rise and Fall Time	t_r, t_f	1.5	8.0	1.5	8.0	ns	When driven from Address inputs.
Capacitance							Measured with a pulse technique. See Note 4.
Input Lead Capacitance	C_{in}	—	5.0	—	5.0	pF	
Output Lead Capacitance	C_{out}	—	8.0	—	8.0	pF	

5

Notes:
(1) Contact your Motorola Sales Representative for details if extended temperature operation is desired.
(2) The maximum Address Access Time is guaranteed to be the Worst-Case Bit in the Memory.
(3) For proper use of MECL Memories in a System environment, consult: "MECL System Design Handbook."
(4) Typical ratings are 3.0 pF for C_{in} and 5.0 pF for C_{out}.

FIGURE 1 — SWITCHING TEST CIRCUIT AND WAVEFORMS



MOTOROLA

MCM10422-10
MCM10422-15

Advance Information

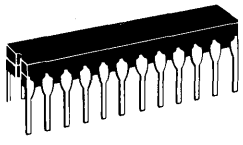
256 x 4-BIT RANDOM ACCESS MEMORY

The MCM10422 is a high-speed 1024-bit Read/Write RAM organized 256 words by 4 bits, designed for high speed scratch pad, control, cache, and buffer storage applications. Four independent active-low Block Selects permit use in 1024 x 1 and 512 x 2-bit applications. It has full address decoding on chip, separate data inputs, noninverting data outputs, and an active-low Write Enable.

- Address Access Time:
  MCM10422-15 15 ns (Max)
  MCM10422-10 10 ns (Max)
- Power Dissipation Decreases with Increasing Temperature
- Fully Compatible with MECL 10K and 10KH
- Operating Temperature Range 0°C to 75°C
- Four Independent Block Selects
- Emitter-Follower Outputs Permits Full Wire-OR'ing
- Standard 24-Pin, 400 Mil Wide, Dual In-Line Package

MECL

256 x 4-BIT RANDOM ACCESS MEMORY



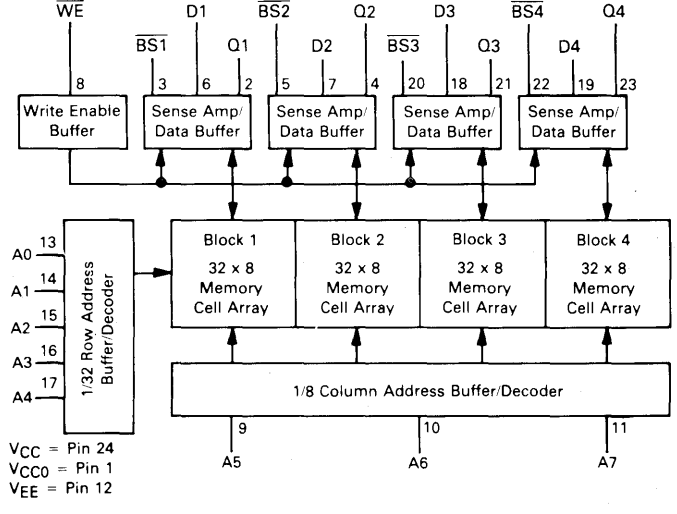
L SUFFIX
CERAMIC PACKAGE
CASE 748-01

ORDERING INFORMATION
Suffix Denotes
MCM10422L10 — Ceramic Dual-in-Line Package
MCM10422L15 — Ceramic Dual-in-Line Package

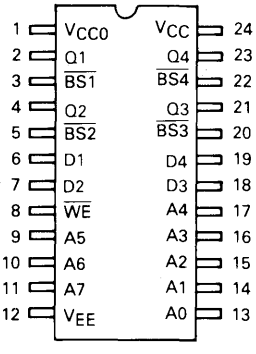
ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage (V_{CC} = 0)	V_{EE}	−8 to 0	Vdc
Base Input Voltage (V_{CC} = 0)	V_{in}	0 to V_{EE}	Vdc
Output Source Current	I_O	< 50	mAdc
Junction Operating Temperature	T_J	< 165	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

BLOCK DIAGRAM



PIN ASSIGNMENT



PIN DESIGNATION

$\overline{BS1}$	—	$\overline{BS4}$	Block Select Inputs
A0	—	A7	Address Inputs
	D_{in}		Data Inputs
	Q_{out}		Data Outputs
	$\overline{WE}$		Write Enable Input

TRUTH TABLE

MODE	INPUT			OUTPUT
	$\overline{BS_n}$	$\overline{WE}$	D_{in}	Q_{out}
Write "0"	L	L	L	L
Write "1"	L	L	H	L
Read	L	H	ϕ	Q
Block Disabled	H	ϕ	ϕ	L

ϕ Don't Care NOTE: Blocks Enable Independently

This document contains information on a new product. Specifications and information herein are subject to change without notice.

5

FUNCTIONAL DESCRIPTION:

This device is a 256 x 4-bit RAM. Word selection is achieved by means of an 8-bit address, A0–A7.

The operating mode of each block ($\overline{BS}_n$ input low) is controlled by the $\overline{WE}$ input. With $\overline{WE}$ low, the block is in the write mode, the output Q_{out} is low and the data state present at D_{in} is stored at the selected address in block n. With $\overline{WE}$ high, the block is in the read mode and the data stored at the selected memory location will be presented non-inverted at Q_{out}.

The independent, active-low Block Selects and the wire-OR capability of the emitter-follower outputs permit use as a 1024 x 1 or 512 x 2-bit RAM. For example, for use as a 1024 x 1-bit RAM tie all D_{in} inputs together to form a single D_{in}, wire-OR the Q_{out} lines together to form a single Q_{out} line, and drive the Block Selects with a 1-of-4 low decoder.

DC OPERATING CONDITIONS AND CHARACTERISTICS

	DC TEST VOLTAGE VALUES (Volts)				
Test Temperature	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
0°C	−0.840	−1.870	−1.145	−1.490	−5.2
+25°C	−0.810	−1.850	−1.105	−1.475	−5.2
+75°C	−0.720	−1.830	−1.045	−1.450	−5.2

ELECTRICAL CHARACTERISTICS

Each MECL Memory circuit has been designed to meet the dc and ac specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts.

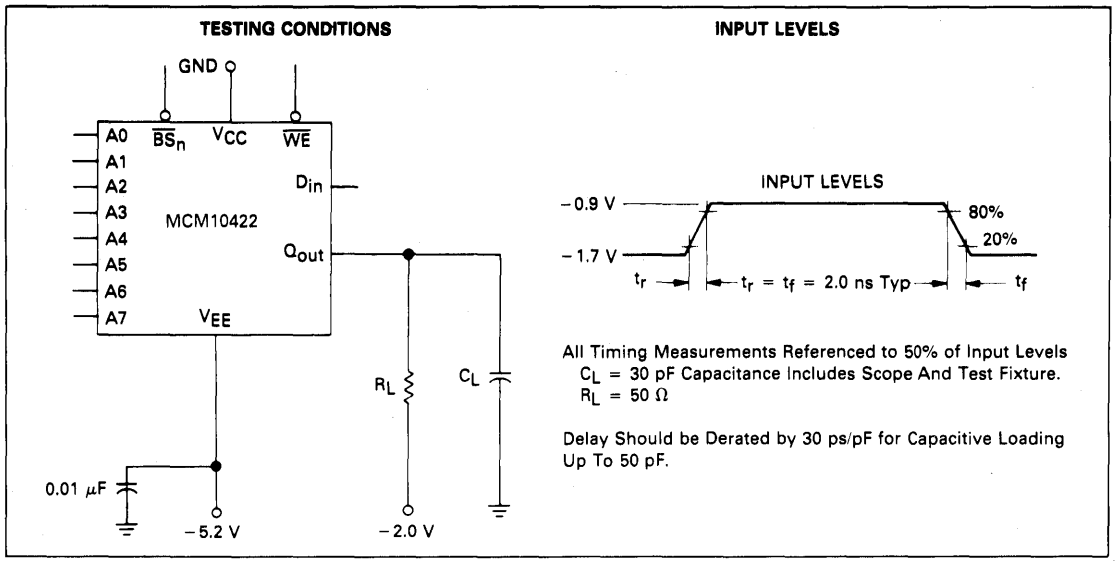
		MCM10422 Test Limits							
		0°C		+25°C		+75°C			
DC Characteristics	Symbol	Min	Max	Min	Max	Min	Max	Unit	Conditions
Power Supply Drain Current	I_{EE}	—	200	—	195	—	185	mAdc	All outputs and inputs open. Measure Pin 12.
Input Current High	I_{inH}	—	220	—	220	—	220	μAdc	Test one input at a time, all other inputs are open. $V_{in} = V_{IH(max)}$
Input Current Low (Block Selects)	I_{inL}	0.5	—	0.5	—	0.5	—	μAdc	Test one input at a time, all other inputs are open. $V_{in} = V_{IL(min)}$
Input Current Low*	I_{inL}	−50	—	−50	—	−50	—	μAdc	
Logic "1" Output Voltage	V_{OH}	−1.000	−0.840	−0.960	−0.810	−0.900	−0.720	Vdc	Load 50 Ω to −2.0 V
Logic "0" Output Voltage	V_{OL}	−1.870	−1.665	−1.850	−1.650	−1.830	−1.625	Vdc	
Logic "1" Threshold Voltage	V_{OHA}	−1.020	—	−0.980	—	−0.920	—	Vdc	Threshold testing is performed and guaranteed on one input at a time. $V_{in} = V_{IHA}$ or V_{ILA}. Load 50 Ω to −2.0 V.
Logic "0" Threshold Voltage	V_{OLA}	—	−1.645	—	−1.630	—	−1.605	Vdc	

*Minimum limit equals the maximum negative current the driving circuitry will be required to sink.

	θ_{JA} (Junction to Ambient)		θ_{JC}
Package	Blown*	Still	(Junction to Case)
L Suffix	35°C/W	55°C/W	15°C/W

*500 linear ft. per minute blown air.

FIGURE 1 — SWITCHING TEST CIRCUIT AND WAVEFORMS



AC OPERATING CONDITIONS AND CHARACTERISTICS

Guaranteed with V_{EE} = −5.2 Vdc ±5.0%, T_A = 0°C to 75°C (see Note 1). Output Load see Figure 1.

Characterstic	Symbol	MCM10422-15 Min	MCM10422-15 Max	MCM10422-10 Min	MCM10422-10 Max	Unit	Conditions
Read Mode							See Figures 2 and 3.
Block Select Access Time	t_{ABS}	—	6.0	—	5.0	ns	Measured at 50% of input
Block Select Recovery Time	t_{RBS}	—	6.0	—	5.0	ns	to 50% of output.
Address Access Time	t_{AA}	—	15	—	10	ns	See Note 1.
Write Mode							See Figure 4.
Write Pulse Width (To guarantee writing)	t_W	10	—	7.0	—	ns	t_{WSA} = 2.0 ns. MCM10422-15 t_{WSA} = 1.0 ns MCM10422-10 Measured at 50% of input to 50% of output.
Data Setup Time Prior to Write	t_{WSD}	1.0	—	1.0	—	ns	
Data Hold Time After Write	t_{WHD}	4.0	—	2.0	—	ns	
Address Setup Time Prior to Write	t_{WSA}	2.0	—	1.0	—	ns	t_W = 10 ns MCM10422-15 t_W = 7.0 ns MCM10422-10
Address Hold Time After Write	t_{WHA}	3.0	—	2.0	—	ns	
Block Select Setup Time Prior to Write	t_{WSBS}	2.0	—	1.0	—	ns	
Block Select Hold Time After Write	t_{WHBS}	3.0	—	2.0	—	ns	
Write Disable Time	t_{WS}	—	5.0	—	5.0	ns	
Write Recovery Time	t_{WR}	—	9.0	—	9.0	ns	
Rise and Fall Time		TYPICAL					Measured between 20% and 80% points.
Output Rise and Fall Time	t_r, t_f	2.0				ns	
Capacitance		TYPICAL					Measured with a pulse technique.
Input Lead Capacitance	C_{in}	5.0				pF	
Output Lead Capacitance	C_{out}	5.0				pF	

Notes:
(1) The maximum Address Access Time is guaranteed to be the Worst-Case Bit in the Memory.
(2) For proper use of MECL Memories in a system environment, consult: "MECL System Design Handbook."

5

FIGURE 2 — BLOCK SELECT ACCESS TIME

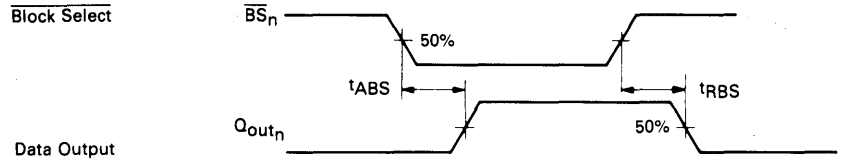


FIGURE 3 — ADDRESS ACCESS TIME

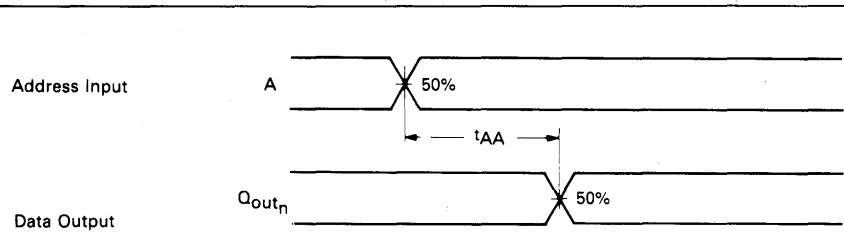
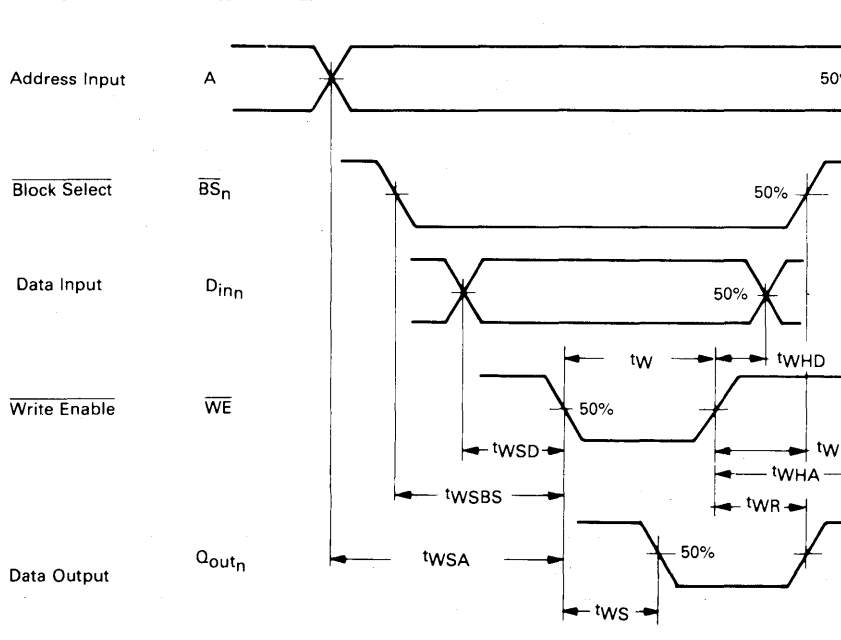


FIGURE 4 — WRITE STROBE MODE



5

MOTOROLA

SEMICONDUCTORS

P.O. BOX 20912 • PHOENIX, ARIZONA 85036

MCM10470-15
MCM10470-25

Advance Information

MECL

4096 x 1-BIT RANDOM ACCESS MEMORY

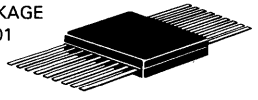
4096 x 1-BIT RANDOM ACCESS MEMORY

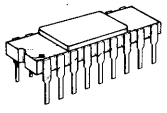
The MCM10470 is a 4096-bit Read/Write RAM organized for 4096 words by 1 bit. Data is selected or stored by means of a 12-bit address (A0 through A11) decoded on the chip. The chip is designed with a separate data-in line, a noninverting data output, and an active-low chip select.

This device is designed for use in high-speed scratch pad, control, cache and buffer storage applications.

- Fully Compatible with MECL 10K/10KH
- Pin-for-Pin Compatible with the Industry's Standard 10470
- Temperature Range of 0° to 75°C
- Emitter-Follower Output Permits Full Wire-ORing
- Power Dissipation Decreases with Increasing Temperature
- Address Access Time: MCM10470-25 25 ns (Max)
  MCM10470-15 15 ns (Max)

F SUFFIX
CERAMIC PACKAGE
CASE 747-01





L SUFFIX
CERAMIC PACKAGE
CASE 680-06

ORDERING INFORMATION

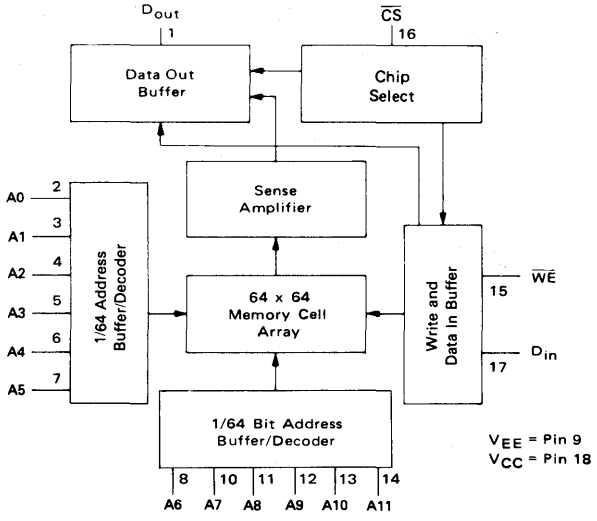
Suffix Denotes

MCM10470L15 — Ceramic Dual-in-Line Package
MCM10470F15 — Ceramic Flat Package
MCM10470L25 — Ceramic Dual-in-Line Package
MCM10470F25 — Ceramic Flat Package

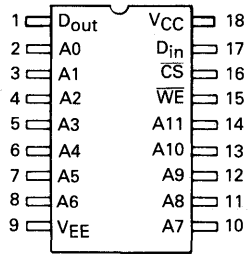
ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage (V_{CC} = 0)	V_{EE}	−8.0 to 0	Vdc
Base Input Voltage (V_{CC} = 0)	V_{in}	0 to V_{EE}	Vdc
Output Source Current	I_O	−30	mAdc
Junction Operating Temperature	T_J	≤ 165	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

BLOCK DIAGRAM



PIN ASSIGNMENT



PIN DESIGNATION

$\overline{CS}$	Chip Select
A0-A11	Address Inputs
$\overline{WE}$	Write Enable
D_{in}	Data Input
D_{out}	Data Output

TRUTH TABLE

MODE	INPUT			OUTPUT
	$\overline{CS}$	$\overline{WE}$	D_{in}	D_{out}
Write "0"	L	L	L	L
Write "1"	L	L	H	L
Read	L	H	φ	Q
Disabled	H	φ	φ	L

φ = Irrelevant

5

FUNCTIONAL DESCRIPTION:

This device is a 4096 x 1-bit RAM. Bit selection is achieved by means of a 12-bit address, A0 to A11.

The active-low chip select is provided for memory expansion.

The operating mode of the RAM ($\overline{CS}$ input low) is controlled by the $\overline{WE}$ input. With $\overline{WE}$ low, the chip is in the write mode, the output, D_{out}, is low and the data state present at D_{in} is stored at the selected address. With $\overline{WE}$ high, the chip is in the read mode and the data stored at the selected memory location will be presented non-inverted at D_{out}. (See Truth Table)

DC OPERATING CONDITIONS AND CHARACTERISTICS

	DC TEST VOLTAGE VALUES (Volts)				
Test Temperature	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
0°C	-0.840	-1.870	-1.145	-1.490	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+75°C	-0.720	-1.830	-1.045	-1.450	-5.2

ELECTRICAL CHARACTERISTICS

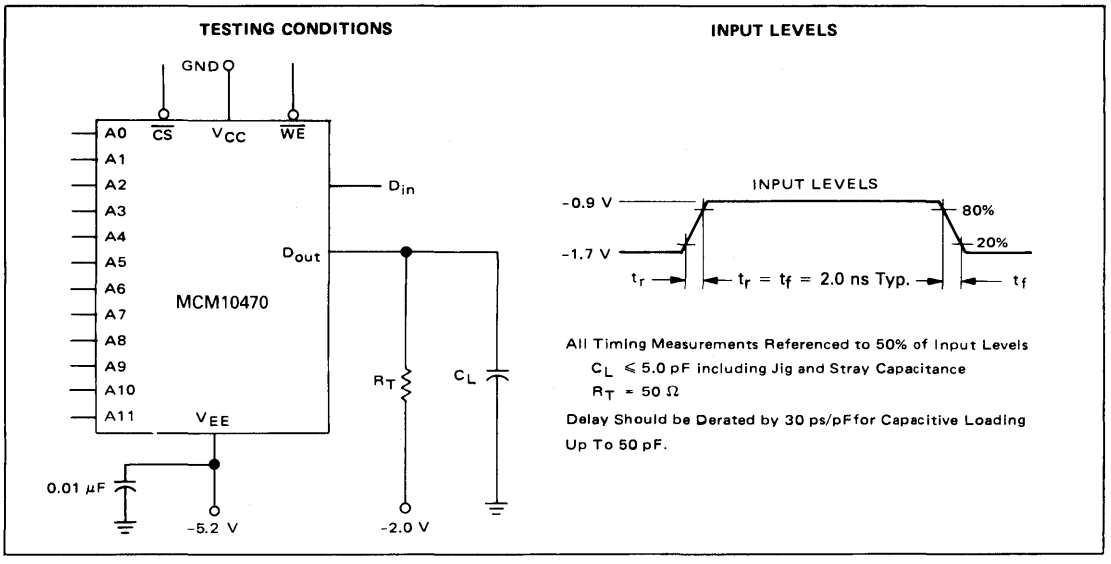
Each MECL Memory circuit has been designed to meet the dc and ac specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts.

		MCM10470 Test Limits							
		0°C		+25°C		+75°C			
DC Characteristics	Symbol	Min	Max	Min	Max	Min	Max	Unit	Conditions
Power Supply Drain Current MCM10470 MCM10470A	I_{EE}	— — —	— 205 205	— — —	— 200 200	— — —	— 190 190	mAdc	All outputs and inputs open. Measure Pin 9.
Input Current High	I_{inH}	—	220	—	220	—	220	μAdc	Test one input at a time, all other inputs are open. $V_{in} = V_{IH(max)}$.
Input Current Low Chip Select	I_{inL}	0.5	—	0.5	—	0.3	—	μAdc	Test one input at a time, all other inputs are open.
Input Current Low*	I_{inL}	-50	—	-50	—	-50	—	μAdc	$V_{in} = V_{IL(min)}$.
Logic "1" Output Voltage	V_{OH}	-1.000	-0.840	-0.960	-0.810	-0.900	-0.720	Vdc	Load 50 Ω to -2.0 V
Logic "0" Output Voltage	V_{OL}	-1.870	-1.665	-1.850	-1.650	-1.830	-1.625	Vdc	
Logic "1" Threshold Voltage	V_{OHA}	-1.020	—	-0.980	—	-0.920	—	Vdc	Threshold testing is performed and guaranteed on one input at a time. $V_{in} = V_{IHA}$ or V_{ILA}. Load 50 Ω to -2.0 V.
Logic "0" Threshold Voltage	V_{OLA}	—	-1.645	—	-1.630	—	-1.605	Vdc	

* Minimum limit equals the maximum negative current the driving circuitry will be required to sink.

5

FIGURE 1 – SWITCHING TEST CIRCUIT AND WAVEFORMS



AC OPERATING CONDITIONS AND CHARACTERISTICS

Guaranteed with V_{EE} = −5.2 Vdc ± 5.0%, T_A = 0°C to 75°C (see Note 1). Output Load see Figure 1.

Characteristic	Symbol	MCM10470-25 Min	MCM10470-25 Max	MCM10470-15 Min	MCM10470-15 Max	Unit	Conditions
Read Mode							See Figures 2 and 3.
Chip Select Access Time	t_{ACS}	—	10	—	8.0	ns	Measured at 50% of input to 50%
Chip Select Recovery Time	t_{RCS}	—	10	—	8.0	ns	of output.
Address Access Time	t_{AA}	—	25	—	15	ns	See Note 2.
Write Mode							See Figure 4.
Write Pulse Width (To guarantee writing)	t_W	25	—	15	—	ns	t_{WSA} = 3.0 ns MCM10470-25 t_{WSA} = 3.0 ns MCM10470-15 Measured at 50% of input to 50% of output.
Data Setup Time Prior to Write	t_{WSD}	2.0	—	2.0	—	ns	
Data Hold Time After Write	t_{WHD}	2.0	—	2.0	—	ns	
Address Setup Time Prior to Write	t_{WSA}	3.0	—	3.0	—	ns	t_W = 25 ns MCM10470-25 t_W = 15 ns MCM10470-15
Address Hold Time After Write	t_{WHA}	2.0	—	2.0	—	ns	
Chip Select Setup Time Prior to Write	t_{WSCS}	2.0	—	2.0	—	ns	
Chip Select Hold Time After Write	t_{WHCS}	2.0	—	2.0	—	ns	
Write Disable Time	t_{WS}	—	10	—	8.0	ns	
Write Recovery Time	t_{WR}	—	10	—	8.0	ns	
Rise and Fall Time		Typical					Measured between 20% and 80% points.
Output Rise and Fall Time	t_r, t_f	2.0				ns	
Capacitance		Typical					Measured with a pulse technique.
Input Lead Capacitance	C_{in}	3.0				pF	
Output Lead Capacitance	C_{out}	5.0				pF	

Notes:
(1) Contact your Motorola Sales Representative for details if extended temperature operation is desired.
(2) The maximum Address Access Time is guaranteed to be the Worst-Case Bit in the Memory.
(3) For proper use of MECL Memories in a system environment, consult: "MECL System Design Handbook."

FIGURE 2 – CHIP SELECT ACCESS TIME

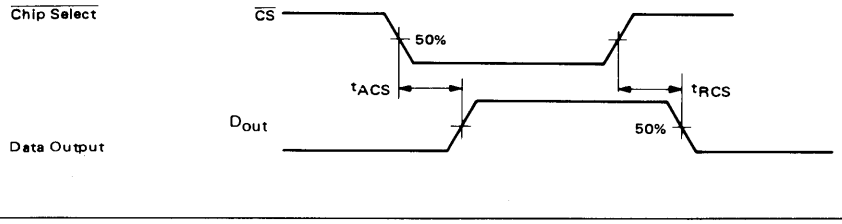


FIGURE 3 – ADDRESS ACCESS TIME

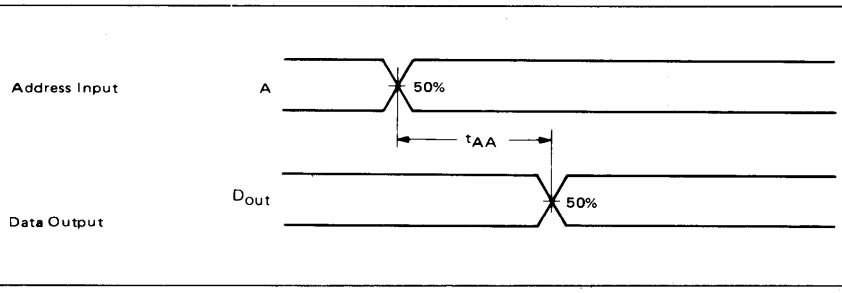
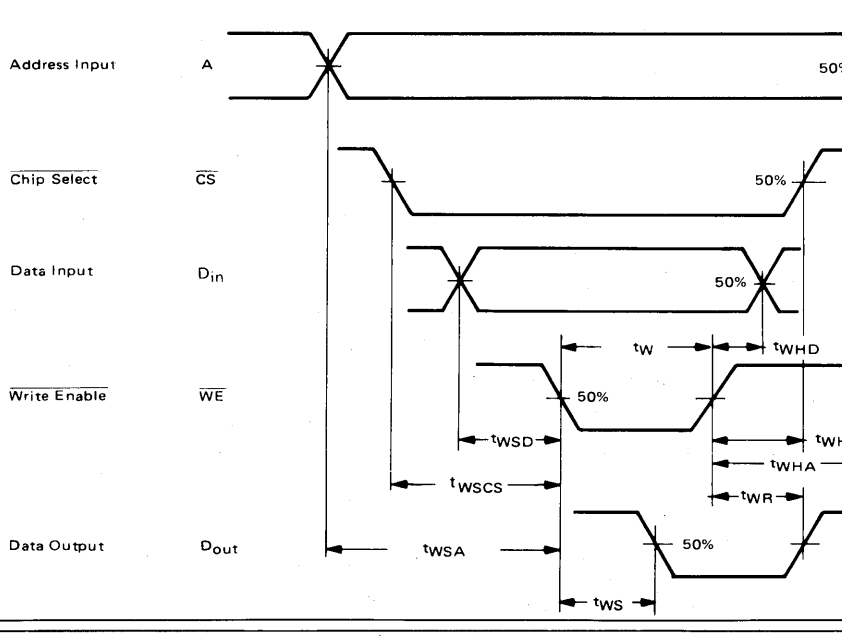


FIGURE 4 – WRITE STROBE MODE



5

MOTOROLA

MCM10474-15
MCM10474-25

Advance Information

1024 x 4-BIT RANDOM ACCESS MEMORY

The MCM10474 is a 4096-bit Read/Write RAM organized for 1024 words by 4 bits. Data is selected or stored by means of a 10-bit address (A0 through A9) decoded on the chip. The chip is designed with 4 separate data-in lines, 4 noninverting data outputs, and an active-low chip select.

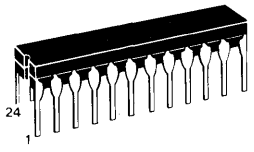
This device is designed for use in high-speed scratch pad, control, cache and buffer storage applications.

- Fully Compatible with MECL 10K/10KH
- Pin-for-Pin Compatible with the Industry's Standard 10474
- Temperature Range of 0° to 75°C
- Emitter-Follower Output Permits Full Wire-ORing
- Power Dissipation Decreases with Increasing Temperature
- Address Access Time: MCM10474-25 25 ns (Max)
  MCM10474-15 15 ns (Max)
- Chip Select Access Time: MCM10474-25 10 ns (Max)
  MCM10474-15 8.0 ns (Max)

MECL

1024 x 4 BIT
RANDOM ACCESS MEMORY

L SUFFIX
CERAMIC PACKAGE
CASE 748-01

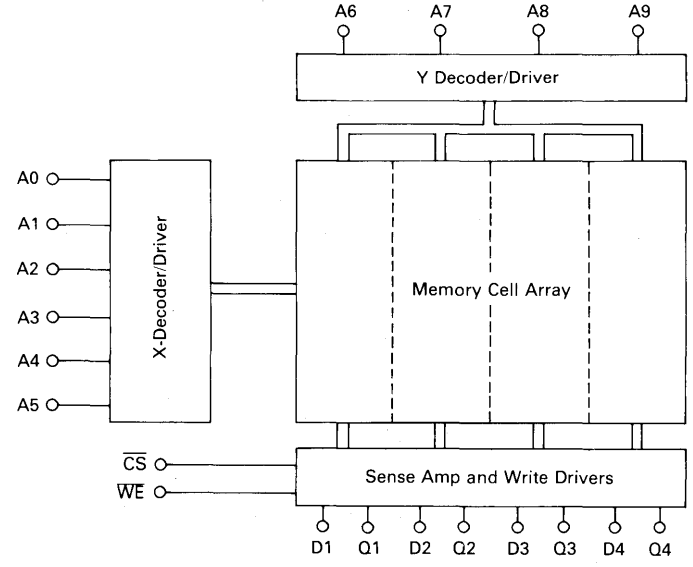


ORDERING INFORMATION
Suffix Denotes
MCM10474L15 — Ceramic Dual-in-Line Package
MCM10474L25 — Ceramic Dual-in-Line Package

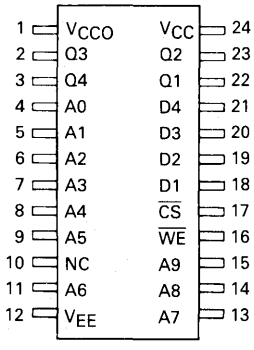
ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage (V_{CC} = 0)	V_{EE}	−8.0 to 0	Vdc
Base Input Voltage (V_{CC} = 0)	V_{in}	0 to V_{EE}	Vdc
Output Source Current	I_O	<50	mAdc
Junction Operating Temperature	T_J	≤ 165	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

BLOCK DIAGRAM



PIN ASSIGNMENT



PIN DESIGNATION

$\overline{CS}$	Chip Select
A0–A9	Address Inputs
$\overline{WE}$	Write Enable
D_{in}	Data Input
Q_{out}	Data Output

TRUTH TABLE

MODE	INPUT			OUTPUT
	$\overline{CS}$	$\overline{WE}$	D_{in}	D_{out}
Write "0"	L	L	L	L
Write "1"	L	L	H	L
Read	L	H	ϕ	DO
Disabled	H	ϕ	ϕ	L

ϕ = Irrelevant

5

FUNCTIONAL DESCRIPTION:

This device is a 1024 x 4-bit RAM. Bit selection is achieved by means of a 10-bit address, A0 to A9.

The active-low chip select is provided for memory expansion.

The operating mode of the RAM ($\overline{CS}$ input low) is controlled by the $\overline{WE}$ input. With $\overline{WE}$ low, the chip is in the write mode, the output, Q_{out}, is low and the data state present at D_{in} is stored at the selected address. With $\overline{WE}$ high, the chip is in the read mode and the data stored at the selected memory location will be presented noninverted at Q_{out}. (See Truth Table)

DC OPERATING CONDITIONS AND CHARACTERISTICS

	DC TEST VOLTAGE VALUES (Volts)				
Test Temperature	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
0°C	-0.840	-1.870	-1.145	-1.490	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+75°C	-0.720	-1.830	-1.045	-1.450	-5.2

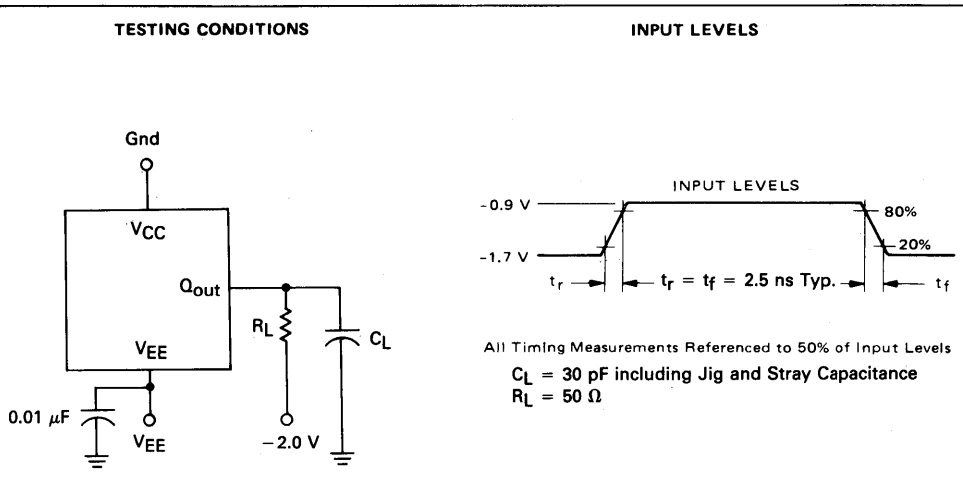
ELECTRICAL CHARACTERISTICS

Each MECL Memory circuit has been designed to meet the dc and ac specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts.

DC Characteristics	Symbol	MCM10474 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	Conditions
Power Supply Drain Current	I_{EE}	–	200	–	195	–	185	mAdc	All outputs and inputs open. Measure Pin 12.
Input Current High	I_{inH}	–	220	–	220	–	220	μAdc	Test one input at a time, all other inputs are open. $V_{in} = V_{IH(max)}$.
Input Current Low Chip Select	I_{inL}	0.5	–	0.5	–	0.3	–	μAdc	Test one input at a time, all other inputs are open. $V_{in} = V_{IL(min)}$.
Input Current Low*	I_{inL}	-50	–	-50	–	-50	–	μAdc	
Logic "1" Output Voltage	V_{OH}	-1.000	-0.840	-0.960	-0.810	-0.900	-0.720	Vdc	Load 50 Ω to -2.0 V
Logic "0" Output Voltage	V_{OL}	-1.870	-1.665	-1.850	-1.650	-1.830	-1.625	Vdc	
Logic "1" Threshold Voltage	V_{OHA}	-1.020	–	-0.980	–	-0.920	–	Vdc	Threshold testing is performed and guaranteed on one input at a time. $V_{in} = V_{IHA}$ or V_{ILA}. Load 50 Ω to -2.0 V.
Logic "0" Threshold Voltage	V_{OLA}	–	-1.645	–	-1.630	–	-1.605	Vdc	

* Minimum limit equals the maximum negative current the driving circuitry will be required to sink.

FIGURE 1 – SWITCHING TEST CIRCUIT AND WAVEFORMS



AC OPERATING CONDITIONS AND CHARACTERISTICS

Guaranteed with V_{EE} = -5.2 Vdc ± 5.0%, T_A = 0°C to 75°C (see Note 1). Output Load see Figure 1.

Characteristic	Symbol	MCM10474-25 Min	MCM10474-25 Max	MCM10474-15 Min	MCM10474-15 Max	Unit	Conditions
Read Mode							See Figures 2 and 3.
Chip Select Access Time	t_{ACS}	—	10	—	8.0	ns	Measured at 50% of input to 50% of output.
Chip Select Recovery Time	t_{RCS}	—	10	—	8.0	ns	
Address Access Time	t_{AA}	—	25	—	15	ns	
Write Mode							See Figure 4.
Write Pulse Width (To guarantee writing)	t_W	25	—	15	—	ns	t_{WSA} = 8.0 ns MCM10474-25 t_{WSA} = 3.0 ns MCM10474-15
Data Setup Time Prior to Write	t_{WSD}	5.0	—	2.0	—	ns	Measured at 50% of input to 50% of output.
Data Hold Time After Write	t_{WHD}	5.0	—	2.0	—	ns	t_W = 25 ns MCM10474-25
Address Setup Time Prior to Write	t_{WSA}	8.0	—	3.0	—	ns	t_W = 15 ns MCM10474-15
Address Hold Time After Write	t_{WHA}	5.0	—	2.0	—	ns	
Chip Select Setup Time Prior to Write	t_{WSCS}	5.0	—	2.0	—	ns	
Chip Select Hold Time After Write	t_{WHCS}	5.0	—	2.0	—	ns	
Write Disable Time	t_{WS}	—	10	—	8.0	ns	
Write Recovery Time	t_{WR}	—	15	—	8.0	ns	
Rise and Fall Time		Typical					Measured between 20% and 80% points.
Output Rise and Fall Time	t_r, t_f	2.5				ns	
Capacitance		Typical					Measured with a pulse technique.
Input Lead Capacitance	C_{in}	4.0				pF	
Output Lead Capacitance	C_{out}	7.0				pF	

Notes:
(1) The maximum Address Access Time is guaranteed to be the Worst-Case Bit in the Memory.
(2) For proper use of MECL Memories in a system environment, consult: "MECL System Design Handbook."

FIGURE 2 — CHIP SELECT ACCESS TIME

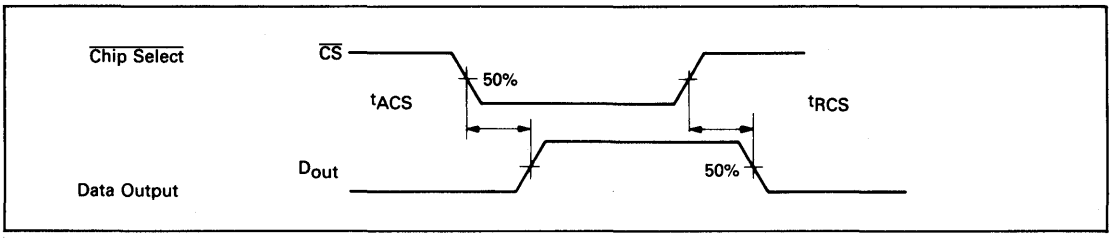


FIGURE 3 — ADDRESS ACCESS TIME

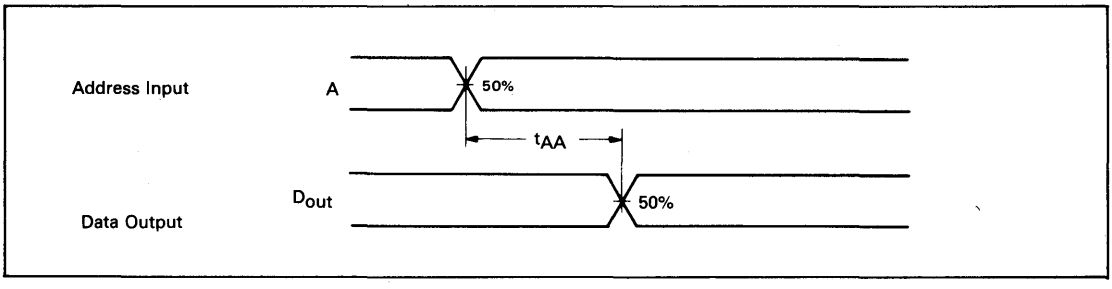
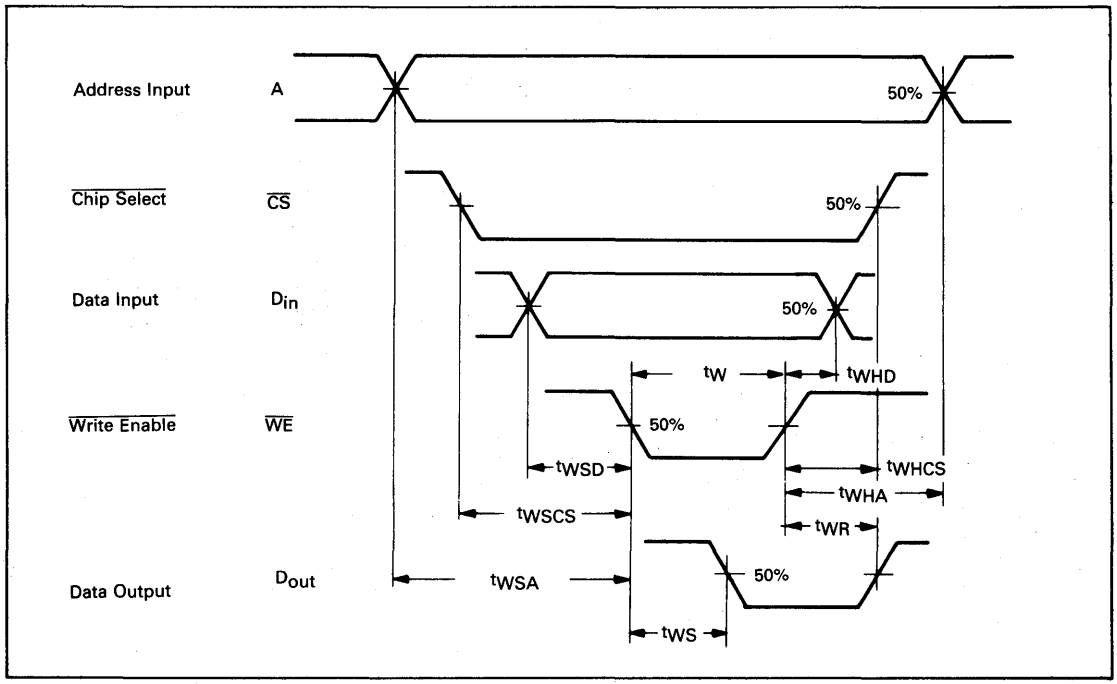
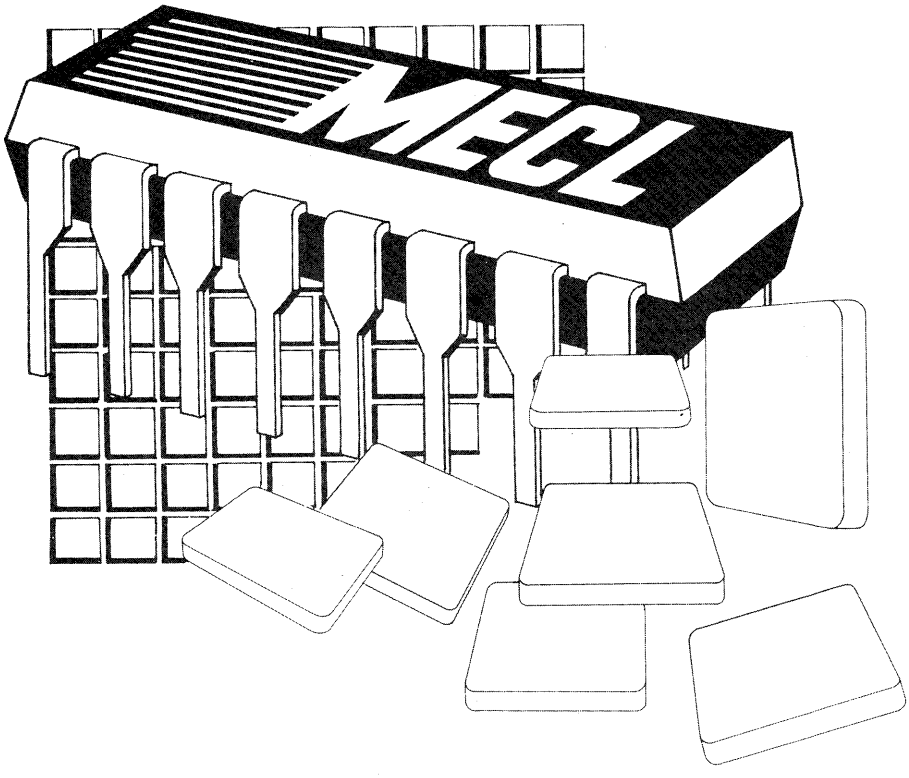


FIGURE 4 — WRITE STROBE MODE



5



Selection Guide **Data Sheets** 6

MECL Macrocell Array
INTEGRATED CIRCUITS

The Macrocell Array Concept combines a pre-diffused array of components with computer aided design techniques to offer system designers a rapid, cost-effective means of developing semi-custom high-speed digital logic systems with VLSI circuitry. Compared with the conventional approach to custom LSI circuits, the Macrocell approach offers a tremendous reduction in development time.

MECL Macrocell Array family members presently consist of the MCA600 ECL array, MCA1200 ECL array, MCA2500ECL array and the MC10900 family.

The MC10900 family is a series of very high performance LSI functions designed from the Macrocell Array product. While the Macrocell Array is normally used for custom circuits, the MC10900 family is a standard product offering.

Function	Device
8-Bit ALU with Parity	MC10900Z
8 × 8 Bit Expandable Multiplier	MC10901Z
8-Bit BCD/Binary ALU	MC10902Z
8-Bit Micro Code Sequencer Slice	MC10904Z
Error Detect & Correct Circuit	MC10905Z

	MCA 600ECL	MCA 1200ECL	MC 2500ECL
MAX GATE EQUIVALENT	652	1192	2472
MAJOR MACROCELLS	24	48	110
INPUT/INTERFACE CELLS	25	32	—
OUTPUT MACROCELLS	18	26	68
MEMORY BITS	—	—	—
MAX. GATE DELAY	1.2	1.2	0.5
MAX. TOGGLE FREQ.	160	160	300
POWER DISSIPATION	2.2	4.0	8
PACKAGE: DUAL-IN-LINE	28,40	—	—
PACKAGE: CHIP CARRIER	68	68,68PG	149PG
TEMPERATURE RANGE	0-70	0-70	0-70
I/O INTERFACE	10K	10K	10KH/100K
DESIGN INTERFACE	CAD	CAD	CAD
AVAILABILITY	NOW	NOW	NOW

MOTOROLA

MC10900

Advance Information

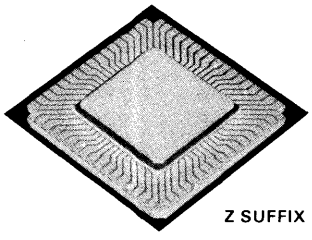
8-BIT PARITY ALU SLICE

The MC10900 8-Bit Parity ALU Slice is an LSI building block for digital processors. This circuit performs the necessary logic and arithmetic functions required to execute the various machine instructions. Each part is 8-bits wide and is "sliced" parallel to data flow. The MC10900 is fully expandable to larger word lengths by connecting circuits in parallel.

The 8-Bit Parity ALU Slice as shown in the block diagram contains logic functions, shift network, arithmetic logic, input-output latches, and parity detect logic in a single bipolar circuit. Six select lines and four latch lines are used to control all operations within the part.

- Two Input Data Ports
- Internal Lookahead Carry with Propagate and Generate Outputs
- Status Outputs: Carryout, Zero Detect, Parity Error Detect, Internal Carry Signal for Overflow Detect
- Each Port Is 8-Bits Wide and the Circuit Can be Operated in Parallel to Form Any Word Size in Increments of 4 Bits.
- Single-Bit and 4-Bit Shift Operations
- The Parity Bit Is Generated with Separate Internal Logic for Each ALU Operation.

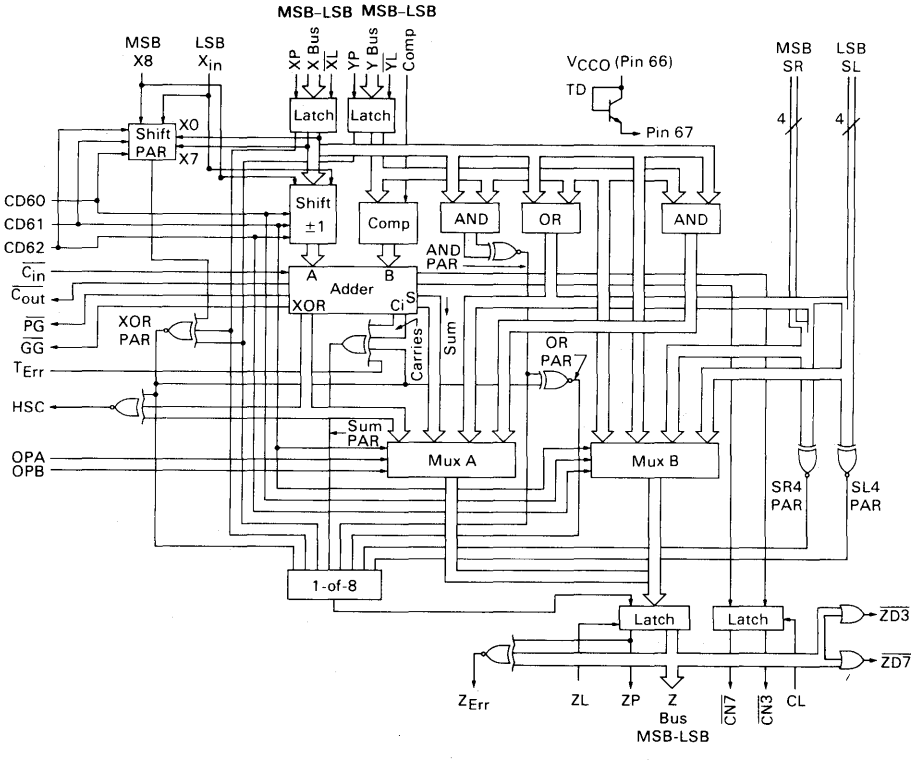
MECL-LSI
8-BIT PARITY ALU SLICE



Z SUFFIX

CASE 745
68-Pin, JEDEC Std
Leadless Package

FIGURE 1 — 8-BIT PARITY ALU SLICE BLOCK DIAGRAM



PIN ASSIGNMENTS

Pin Name	Pin Number	Description
X0	50	Input Bus — LSB Input
X1	48	Input Bus
X2	46	Input Bus
X3	44	Input Bus
X4	41	Input Bus
X5	39	Input Bus
X6	37	Input Bus
X7	35	Input Bus — MSB Input
X8	62	Shift Interconnect — MSB
XL	31	X Latch Enable
XP	32	X Input Parity
X_{in}	63	Shift Interconnect — LSB
Y0	51	Input Bus — LSB Input
Y1	49	Input Bus
Y2	47	Input Bus
Y3	45	Input Bus
Y4	42	Input Bus
Y5	40	Input Bus
Y6	38	Input Bus
Y7	36	Input Bus — MSB Input
YL	52	Y Latch Enable
YP	34	Y Input Parity
C_{in}	25	Carry Input
C_{out}	17	Carry Output
PG	18	Group Propagate Output
GG	13	Group Generate Output
CN3	7	Carry-In to Z3
CN7	8	Carry-In to Z7
SR0	27	Shift Right Input to Z4
SR1	29	Shift Right Input to Z5
SR2	28	Shift Right Input to Z6
SR3	30	Shift Right Input to Z7
SL4	53	Shift Left Input to Z0
SL5	33	Shift Left Input to Z1

Pin Name	Pin Number	Description
SL6	59	Shift Left Input to Z2
SL7	58	Shift Left Input to Z3
Z0	4	Output Bus — LSB Output
Z1	2	Output Bus
Z2	1	Output Bus
Z3	68	Output Bus
Z4	19	Output Bus
Z5	5	Output Bus
Z6	10	Output Bus
Z7	21	Output Bus — MSB Output
ZD3	14	Zero Detect
ZD7	16	Zero Detect
ZP	6	Parity Output
ZL	24	Z Latch Enable
Z_{Err}	11	Bus Error Detect Output
T_{Err}	12	Test Error Detect Input
Comp	57	Control Input Complement
CD60	56	Control Input
CD61	55	Control Input
CD62	54	Control Input
HSC	65	Half Sum Check Output
OPA	64	Control Input
OPB	61	Control Input
V_{EE}	9	-5.2-Volt Supply
V_{EE}	43	-5.2-Volt Supply
V_{CC}	26	Ground
V_{CC}	20	Ground
V_{CCO}	3	Ground
V_{CCO}	15	Ground
V_{CCO}	20	Ground
V_{CCO}	66	Ground
CL	22	Carry Latch Enable
TD	67	Test Diode
NC	23	Not Used

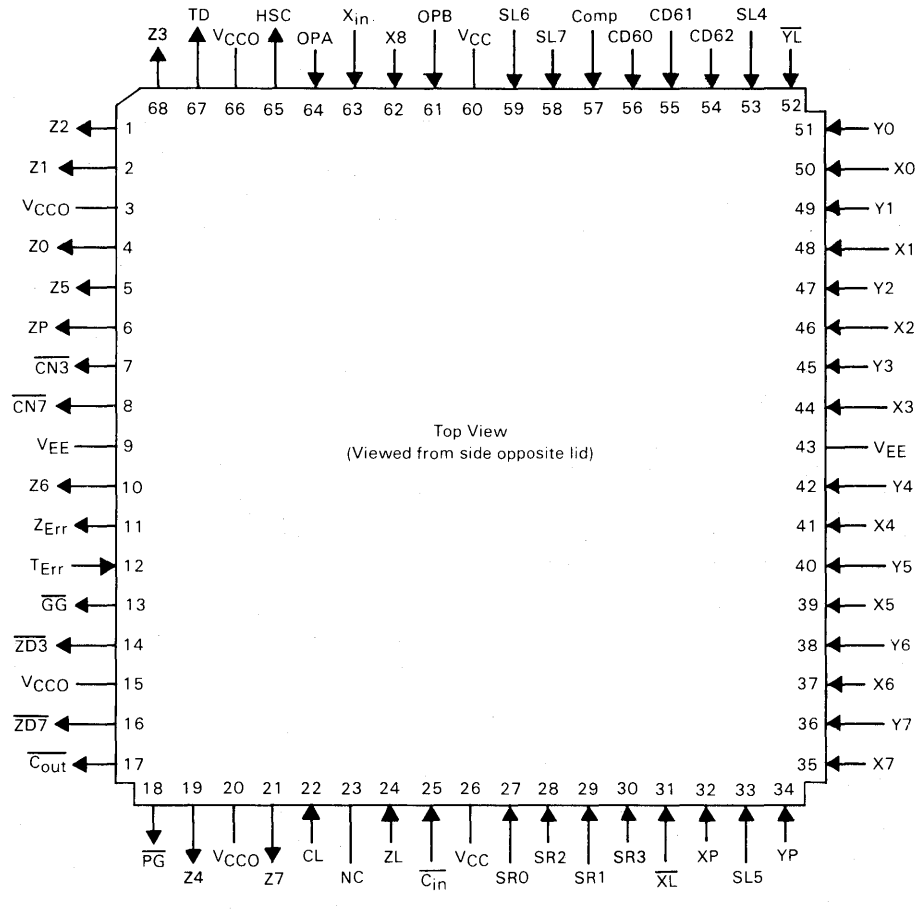
6

ABSOLUTE MAXIMUM RATINGS (see Note 1)

Rating	Symbol	Value	Unit
Supply Voltage (V_{CC} = 0)	V_{EE}	-8 to 0	Vdc
Input Voltage (V_{CC} = 0)	V_{in}	0 to V_{EE}	Vdc
Output Source Current — Continuous — Surge	I_o	<30 <100	mAdc
Storage Temperature	T_{stg}	-55 to +150	°C
Junction Temperature	T_J	165	°C

NOTE: 1. Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

FIGURE 2 — INPUT/OUTPUT DIAGRAM



ARCHITECTURAL DESCRIPTION

The MECL LSI 8-Bit Parity ALU Slice is a member of the M10900 family utilizing the MECL 10,000 Macrocell Array. The parity ALU slice has the capability of performing logic operations and binary arithmetic on combinations of one and two variables, X Bus and Y Bus. Single-bit data paths $\overline{C_{in}}$, $\overline{C_{out}}$, X_{in}, and X8 and four-bit data paths SL and SR are used to interconnect parallel MC10900s for larger word lengths. These data bits allow for arithmetic and shift operations on larger word lengths. Group propagate and group generate outputs can be used in conjunction with external lookahead carry logic for faster system operation. Two zero detect bits signal the all low condition of bits Z7–Z4 or Z3–Z0 of the Z output bus. Carry signals generated within the adder of the ALU, $\overline{CN3}$ and $\overline{CN7}$, are made available as outputs for determining overflow conditions. The circuit also contains two parity error signals which continuously checks data flow within the 8-bit ALU slice.

Data enters the ALU through the X Bus and Y Bus and exits through the Z bus. Each port is 9 bits wide consisting of 8 data bits, 1 odd parity bit, and a 9-bit latch. X and Y input data is routed to four logic networks which generate a 1-bit shift right or left of X, a complement of Y, a logic OR of X and Y, and a logical AND of X and Y. The adder network generates the arithmatic sum and the logical Exclusive-OR from the outputs of the shift and complement logic. Two 1-of-4 multiplexors select the data path to the Z output bus.

NOTE: All truth tables are expressed in positive logic.

Input X Bus

The X input bus consists of eight bits which serve as input data paths to an internal latch in the ALU. Data is passed through the latch when the latch control bit $\overline{XL}$ is at a logic L. Data is latched into the ALU when $\overline{XL}$ is at a logic H. The inputs are designated with X7 as the most significant bit (MSB) and X0 as the least signficant bit (LSB).

Input Y Bus

The Y input bus function is identical to the X bus described above.

Parity Inputs XP and YP

Parity input bits, XP and YP are used to detect system errors in data handling. With a single parity bit, it is possible to detect a single bit error or any combination of an odd number of bit errors.

XP is used to input the parity of the X bus. Likewise, YP is the parity input for the Y bus. These bits are used in determining the Z parity output, ZP, and parity error signals, HSC and Z_{Err}.

Shift Interconnects

X_{in}, X8, SL, and SR inputs are provided to interconnect 8-bit slice circuits for shift operations. For a 1-bit shift left, X_{in} is shifted into the X0 position. For a 1-bit shift right, X8 is shifted into the X7 position.

SL and SR inputs are provided for 4-bit shift operations. For a 4-bit shift left, bits SL7–SL4 are shifted into Z3–Z0, respectively, while the results of the OR function bits (X + Y)3–(X + Y)0 are shifted into Z7–Z4, respectively. For a 4-bit shift right, bits SR3–SR0 are shifted into Z7–Z4, respectively, while the results of the OR function bits (X + Y)7–(X + Y)4, are shifted into Z3–Z0, respectively.

Half Sum Check

Half sum check, HSC, is a parity check of X Bus and Y Bus along with an error check of the half sum adder network. The half sum check will detect a single-bit error or any combination of an odd number of bit errors.

Half sums are generated by the bit-by-bit Exclusive-OR of the X bus and Y bus. These half sum bits, along with the input parity bits XP and YP, are used to determine the error check. (See Table 3.)

$$HSC = HS7 \oplus HS6 \oplus HS5 \oplus HS4 \oplus HS3 \oplus HS2 \oplus \therefore$$
$$HS1 \oplus HS0 \oplus XP \oplus YP \oplus \text{Shift PAR}$$

Carry Signals

Carry Signals, $\overline{CN3}$ and $\overline{CN7}$, can be used to detect system overflow. Overflow detects when the maximum system word or byte value has been exceeded. In a system, only the overflow from the 8-bit slice operating on the most significant bits of the data word is used.

Overflow can be detected by the Exclusive-OR of the carry out and carry in of the most significant bit in a system. In an eight-bit increment system (, 16, 24, . . .) overflow can be generated by the Exclusive-OR of signals $\overline{C_{out}}$ and $\overline{CN7}$:

$$OF = \overline{C_{out}} \oplus \overline{CN7}$$

In a four-bit increment system (4, 12, 20 . . .) overflow can be generated by the Exclusive-NOR of signals Z4 and $\overline{CN3}$:

$$OF = \overline{Z4} \oplus \overline{CN3}$$

Z4 is in effect the carry out of the 8-bit slice ALU operating in a 4-bit slice mode.

Carry In

Carry in, $\overline{C_{in}}$, is used to interconnect 8-bit slice circuits in a system. For ripple carry, carry in is connected to carry out of the preceding 8-bit slice. Carry in is only used for arithmetic operations and has no effect on any logic operation.

Carry Out

Carry out, $\overline{C_{out}}$, signals that the calculated value within the ALU has exceeded the maximum capacity. Any binary count over 255 results in a carry out. When ripple carry is used, carry out is connected to carry in of the following 8-bit slice. The carry out in the 8-bit ALU is generated by lookahead carry logic. This improves speed for multi-slice systems. $C_{out} = PG \cdot C_{in} + GG$.

Output Z Bus

The Z output bus, Z0–Z7, consists of eight bits which serve as the output data paths from the ALU. Data passes through an internal latch and onto the Z bus when the latch control bit ZL is at a logic H. Data is latched onto the Z bus when ZL is at a logic L. The inputs are designated with Z7 as the most significant bit and Z0 as the least significant bit. (See Table 5.)

Zero Detect

Zero detect, $\overline{ZD7}$ and $\overline{ZD3}$, signals the all low condition at the output of Z latches. $\overline{ZD7}$ signals that Z7–Z4 are all low (0000) and $\overline{ZD3}$ signals that Z3–Z0 are all low. Zero detect is defined by the following equations:

$$\overline{ZD7} = Z7 + Z6 + Z5 + Z4$$
$$\overline{ZD3} = Z3 + Z2 + Z1 + Z0$$

Z Bus Error

Z bus error, Z_{Err}, is used to detect a single-bit error or any combination of an odd number of bit errors associated with data flow through the multiplexors and output latches. The output parity bit, ZP is compared with the parity of the Z bus output. If no error exists, Z_{Err} will be at a logic L. If an error exists, Z_{Err} will be at a logic H.

$$Z_{Err} = [Z0 \oplus Z1 \oplus Z2 \oplus Z3 \oplus Z4 \oplus Z5 \oplus Z6 \oplus Z7] \oplus ZP$$

Test Error

Test error bit, T_{Err}, is used to test the Z bus error signal, Z_{Err}. T_{Err} is enabled only when an arithmetic operation is being performed. A logic H on the T_{Err} input will result in an incorrect parity of the arithmetic operation output. This will be detected by the Z bus error logic (see Figure 1).

Parity Output

Parity output, ZP, is used to output the parity of the Z bus. ZP is generated independently of the Z bus, which adds another level of system error check. (See Tables 2, 3, 5.)

Group Propagate and Group Generate

The group propagate, PG, and group generate, GG, outputs are used in conjuction with external lookahead carry logic for faster system operation. Using this technique, the carry in signals to the 8-bit slice circuits are generated faster than with ripple carry.

$$PG = P7 \cdot P5 \cdot P3 \cdot P1$$
$$GG = G7 + P7 \cdot G5 + P7 \cdot P5 \cdot G3 + P7 \cdot P5 \cdot P3 \cdot G1$$
$$\text{Where } P_i = (A_i \oplus B_i) \cdot (A_{i-1} \oplus B_{i-1})$$
$$G_i = A_i \cdot B_i + (A_i + B_i) \cdot (A_{i-1} \cdot B_{i-1})$$

A is the output of the one-bit shifter and
B is the output of the complementer going to the adder.
(See Figure 1.)

Test Diode

A test diode, TD, is connected to Pin 67 for use in testing the junction temperature. Pin 66 is connected to the anode and Pin 67 is the cathode.

SELECT LINE OPERATION

One-Bit Shift Select

Control inputs CD60, CD61, and CD62 are used to give the MECL 8-bit slice a one-bit shift left or a one bit shift right. A logic L on CD62 results in a 1-bit shift left whereas a logic H results in a 1-bit shift right operation. When CD60 is held at a logic L or CD61 is held at a logic H, no shift operation is performed. Table 1 illustrates the 1-bit shift operation. During a SL, the X_{in} input is shifted into the LSB of the adder. During a SR the X8 input is shifted into the MSB of the adder.

TABLE 1

CD60	CD61	CD62	Operation
L	X	X	No Shift
X	H	X	No Shift
H	L	L	1 Bit Shift Left, XSL
H	L	H	1 Bit Shift Right, XSR

Mux B Select

Control inputs CD60, CD61, and CD62 are used to select the data path to the ALU output latch. When CD61 is held at a logic H, Mux B is enabled. CD60 and CD62 select ALU functions pass X, pass Y, shift left 4 bits or shift right 4 bits.

TABLE 2

CD61	CD60	CD62	Function	ZP
L	X	X	Not Enabled	See Table 3
H	L	L	Pass X	XP
H	L	H	Pass Y	YP
H	H	L	Shift Left 4 Bits	SL4 PAR
H	H	H	Shift Right 4 Bits	SR4 PAR

$SL4\ PAR = [SL4 \oplus SL5 \oplus SL6 \oplus SL7]\ \overline{\oplus}\ [(X0 + Y0) \oplus (X1 + Y1) \oplus (X2 + Y2) \oplus (X3 + Y3)]$

$SR4\ PAR = [SR0 \oplus SR1 \oplus SR2 \oplus SR3]\ \overline{\oplus}\ [(X4 + Y4) \oplus (X5 + Y5) \oplus (X6 + Y6) \oplus (X7 + Y7)]$

Mux A Select

Control inputs OPA, OPB, and CD61 are used to select the data path to the ALU output latch. When CD61 is held at a logic L, Mux A is enabled, OPA and OPB select ALU functions Sum, XOR, X +Y, or X · Y (see Figure 1).

TABLE 3

CD61	OPA	OPB	Function	ZP
H	X	X	Not Enabled	See Table 2
L	L	L	Sum	Sum PAR
L	L	H	XOR	XOR PAR
L	H	L	X · Y	AND PAR
L	H	H	X + Y	OR PAR

$XOR\ PAR = (Shift\ PAR)\ \overline{\oplus}\ [XP \oplus YP]$ where

$Shift\ PAR = [X7 \oplus X_{in}) \cdot \overline{CD62} + (X8 \oplus X0) \cdot \overline{CD62} \cdot \overline{CD60} \cdot \overline{CD61}$ ∴

$AND\ PAR = [(X0 \cdot Y0) \oplus (X1 \cdot Y1) \oplus (X2 \cdot Y2) \oplus (X3 \cdot Y3)] \oplus [(X4 \cdot Y4) \oplus (X5 \cdot Y5) \oplus (X6 \cdot Y6) \oplus (X7 \cdot Y7)]$ ∴

$OR\ PAR = [AND\ PAR)\ \overline{\oplus}\ (XOR\ PAR)$

$Sum\ PAR = C_{in} \oplus C1 \oplus C2 \oplus C3 \oplus C4 \oplus C5 \oplus C6 \oplus C7 \oplus T_{Err} \oplus (XOR\ PAR)$ ∴

where c_i is the carry-in for generating bit Z_i for i = 1 to 7.

Complement Y Select

Control input Comp inhibits or enables the complement operation. When Comp is at a logic L, Y data is passed. When Comp is at a logic H, Y is complemented.

TABLE 4

Comp	Operation
L	Pass Y
H	Complement Y

TABLE 5

CD61	CD60	CD62	OPA	OPB	Comp	Function	ZP
L	L	X	L	L	L	X Plus Y Plus C_{in}	Sum PAR
L	L	X	L	L	H	X Plus $\overline{Y}$ Plus C_{in}	Sum PAR
L	L	X	L	H	L	$X \oplus Y$	XOR PAR
L	L	X	L	H	H	$X \oplus \overline{Y}$	XOR PAR
L	H	L	L	L	L	XSL Plus Y Plus C_{in}	Sum PAR
L	H	L	L	L	H	XSL Plus $\overline{Y}$ Plus C_{in}	Sum PAR
L	H	L	L	H	L	XSL $\oplus$ Y	XOR PAR
L	H	L	L	H	H	XSL $\oplus \overline{Y}$	XOR PAR
L	H	H	L	L	L	XSR Plus Y Plus C_{in}	Sum PAR
L	H	H	L	L	H	XSR Plus $\overline{Y}$ Plus C_{in}	Sum PAR
L	H	H	L	H	L	XSR $\oplus$ Y	XOR PAR
L	H	H	L	H	H	XSR $\oplus \overline{Y}$	XOR PAR
L	X	X	H	L	X	X · Y	AND PAR
L	X	X	H	H	X	X + Y	OR PAR
H	L	L	X	X	X	X	XP
H	L	H	X	X	X	Y	YP
H	H	L	X	X	X	Shift Left 4 Bits (2)	SL4 PAR
H	H	H	X	X	X	Shift Right 4 Bits (1)	SR4 PAR

(1) The most significant 4 bits of X OR Y are shifted into the least significant 4 bits. The 4 most significant bits are replaced with SR3-SR0 inputs.

(2) The least significant 4 bits of X OR Y are shifted into the most significant 4 bits. The 4 least significant bits are replaced with SL7-SL4 inputs.

$\oplus$ Logical Exclusive-OR + Logical Inclusive-OR · Logical AND

FIGURE 3 — 24-BIT ALU

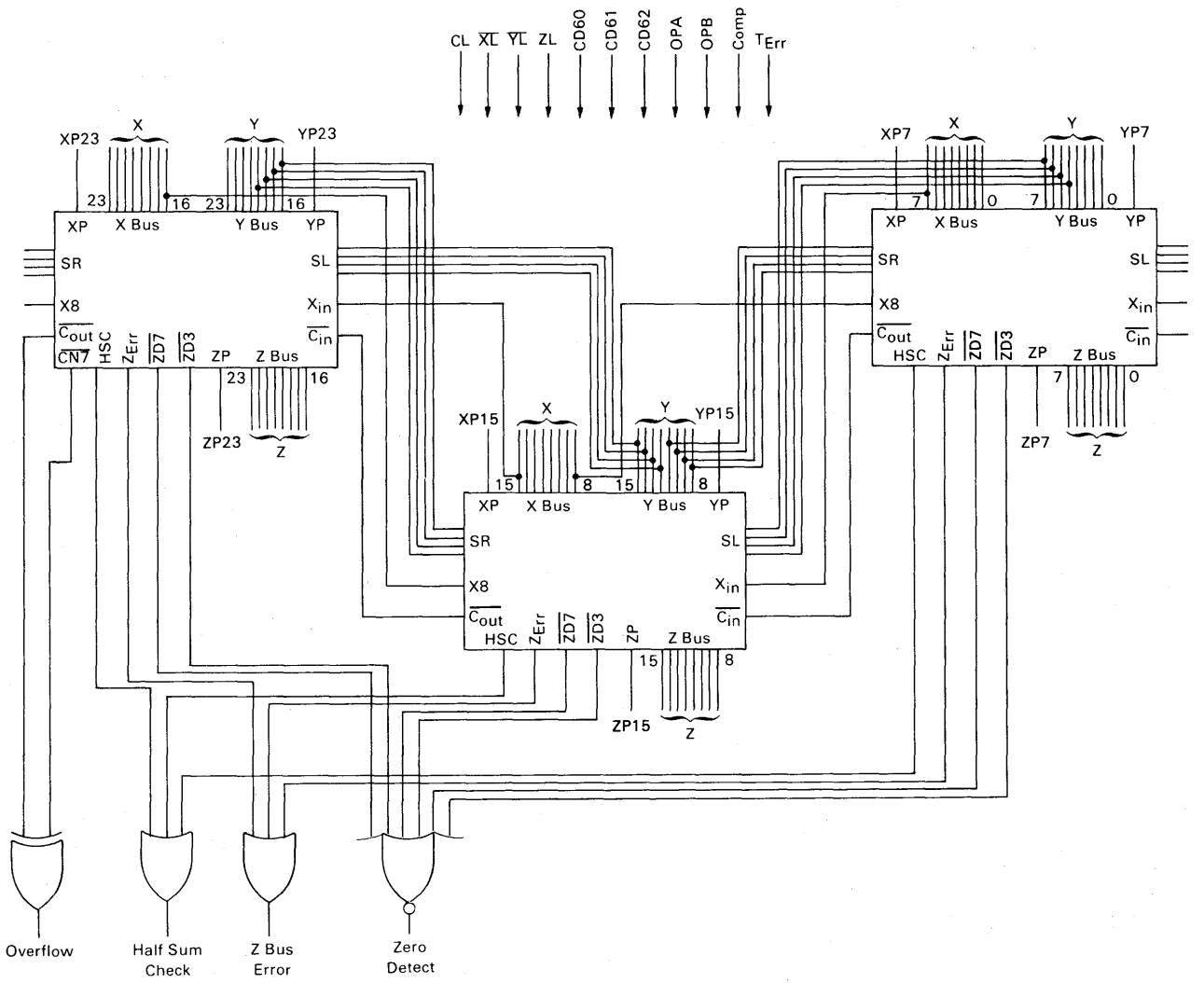


TABLE 6 — RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value	Unit
Supply Voltage (V_{CC} = 0 Volts)	V_{EE}	-4.68 to -5.72	Vdc
Operating Temperature (Functional)	T_A	0 to +70	°c
Output Drive	—	50 Ω to -2.0 Vdc	—
Junction Temperature	T_J	130 max	°C

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table (Table 7), after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board with heat sink and transverse air flow greater than 1000 linear fpm is maintained. Outputs are terminated through a 50-ohm transistor to -2.0 volts. Test procedures are shown for only one input, or for one set of input conditions. Other inputs tested in the same manner.

TABLE 7 — ELECTRICAL CHARACTERISTICS

@ Test Temperature	Test Voltage Values (Volts) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}
0°C	-0.840	-1.95	-1.145	-1.490	-5.2
+25°C	-0.810	-1.95	-1.105	-1.475	-5.2
+70°C	-0.730	-1.95	-1.050	-1.450	-5.2

Characteristics	Symbol	Pin Under Test	MC10900 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Typ	+25°C Max	+70°C Min	+70°C Max	Unit	Voltage Applied to Pins Listed Below: $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}	(V_{CCO}) (V_{CC}) Gnd
Power Supply Drain Current —	I_{EE}	9, 43	514	855	514	685	855	514	855	mAdc	—	—	—	—	9, 43	3, 15, 20 26, 60, 66
Input Current $\overline{CD61}$, $\overline{XL}$, $\overline{YL}$, ZL, $\overline{C_{in}}$, OPA	I_{inH}	55	—	600	—	—	600	—	600	μAdc	—	—	—	—		
All Others	I_{inH}	50	—	250	—	—	250	—	250		50	—	—	—		
	I_{inL}	50	0.5	—	0.5	—	—	0.5	—		—	50	—	—		
Logic High Output Voltage	V_{OH}	4	-1.000	-0.840	-0.960	—	-0.810	-0.905	-0.730	Vdc	50, 55, 24	31, 56, 54				
Logic Low Output Voltage	V_{OL}	4	-1.95	-1.665	-1.95	—	-1.650	-1.95	-1.625	Vdc	55, 24	50, 31, 56, 54	—	—		
Logic High Threshold Voltage	V_{OHA}	4	-1.02	—	-0.980	—	—	-0.925	—	Vdc	55, 24	31, 56, 54	50	—		
Logic Low Threshold Voltage	V_{OLA}	4	—	-1.645	—	—	-1.630	—	-1.605	Vdc	24, 55	31, 54, 56	—	50		

NOTE: All inputs have input pulldown resistors (~ 68 kΩ) between the input and V_{EE}.

SWITCHING CHARACTERISTICS OVER OPERATING VOLTAGE AND TEMPERATURE RANGE

Tables 8 and 9 define timing characteristics of the MC10900 over operating voltage and temperature ranges. Worst-Case Setup and Hold and Propagation Delays are *calculated* for V_{EE} = -5.2 Volts ± 10% and a $T_J$max = 115°C. The maximum recommended operating junction temperature is +130°C.

Calculated limits are based on several performance factors as described in Motorola's Preliminary Design Manual for the MECL 10,000 Macrocell Array. Factors include worst-case delays due to Macro selections, Fan-Out, Metal Lengths, Wire-OR, and Input Follower options. AC measurements are performed on each device to assure process integrity; however, Motorola does not guarantee limits at this time.

TABLE 8 — SETUP AND HOLD TIMES (nanoseconds)*
0° to +70°C T_A (T_J not to exceed +115°C)

Input	Clock (Ref. Edge)	Output	Setup (Min)	Hold (Min)
X Bus, XP	$\overline{XL}$ (L → H)	All	1.6	+1.0
Y Bus, YP	$\overline{YL}$ (L → H)	All	1.6	+1.0
X Bus, Y Bus, Comp	ZL (H → L)	Z Bus	17.8	0
		ZP	19.2	0
	CL (H → L)	$\overline{CN3}$, $\overline{CN7}$	14.5	0
XP, YP	ZL (H → L)	ZP	11.7	0
$\overline{C_{in}}$	ZL (H → L)	Z Bus	12.0	-1.0
		ZP	14.3	-1.0
	CL (H → L)	$\overline{CN3}$, $\overline{CN7}$	8.6	-1.0
SL, SR	ZL (H → L)	Z Bus	6.1	+0.5
		ZP	12.0	0
X8, X_{in}	ZL (H → L)	Z Bus	15.5	-1.0
		ZP	17.2	-1.0
	CL (H → L)	$\overline{CN3}$, $\overline{CN7}$	12.1	-1.0
OPA, OPB	ZL (H → L)	Z Bus, ZP	10.6	+0.5
CD60, CD61, CD62	ZL (H → L)	Z Bus	24.2	+0.5
		ZP	26.1	0
	CL (H → L)	$\overline{CN3}$, $\overline{CN7}$	21.1	-1.0
$\overline{XL}$, $\overline{YL}$ (H → L Edge)	ZL (H → L)	Z Bus	18.9	-0.5
		ZP	20.4	-1.0
	CL (H → L)	$\overline{CN3}$, $\overline{CN7}$	15.5	-1.0
T_{Err}	ZL (H → L)	ZP	7.0	0

*See Figures 4 and 5 for test definitions and circuit.

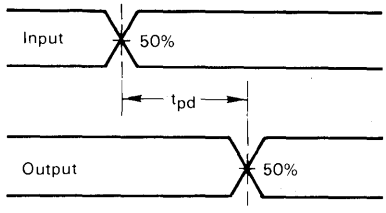
TABLE 9 — PROPAGATION DELAY (nanoseconds)*

Input	Path		Output	0° to 70°C T_A (T_J not to exceed 115°)	
	Via	Mode		Typ	Max
X Bus	Adder	XOR	Z Bus	7.9	12.2
Y Bus	Adder	Arith	Z Bus	11.6	17.8
Comp	Mux B	Logical	Z Bus	6.8	10.8
	Adder	Arith	ZP	12.5	19.2
			$\overline{C_{out}}$	7.5	11.5
			$\overline{CN3}$, $\overline{CN7}$	9.4	14.4
			$\overline{ZD7}$, $\overline{ZD3}$	13.9	20.7
			HSC	9.8	15.1
			Z_{Err}	16.7	25.7
			$\overline{PG}$	7.5	11.5
			$\overline{GG}$	7.4	11.3
XP			ZP	7.6	11.7
YP			HSC	6.8	10.4
			Z_{Err}	10.5	16.2
C_{in}	Adder	Arith	Z Bus	7.8	12.0
			ZP	9.3	14.3
			$\overline{C_{out}}$	2.8	4.3
			$\overline{CN3}$, $\overline{CN7}$	5.5	8.5
			$\overline{ZD7}$, $\overline{ZD3}$	10.0	15.3
			Z_{Err}	12.3	18.9
SL	Mux B	Shift 4 Bits	Z Bus	4.0	6.1
SR			ZP	7.8	12.0
			$\overline{ZD7}$, $\overline{ZD3}$	6.3	9.7
X8	Adder	Shift 1 Bit	Z Bus	10.1	15.5
			ZP	11.2	17.2
X_{in}			$\overline{C_{out}}$	6.0	9.2
			$\overline{CN3}$, $\overline{CN7}$	7.8	12.0
			$\overline{ZD7}$, $\overline{ZD3}$	12.3	18.9
			$\overline{PG}$	6.0	9.2
			$\overline{GG}$	5.8	8.9
			HSC	8.6	13.2
			Z_{Err}	15.5	23.8
T_{Err}		Z Parity Error Check	ZP	4.5	7.0
			Z_{Err}	7.5	11.5
$\overline{XL}$	Latch	Latch X, Y	Z Bus	12.3	18.9
$\overline{YL}$			ZP	13.3	20.4
			$\overline{C_{out}}$	8.3	12.7
			$\overline{CN3}$, $\overline{CN7}$	10.0	15.4
			$\overline{ZD7}$, $\overline{ZD3}$	14.5	22.0
			HSC	10.5	16.2
			Z_{Err}	17.4	26.8
			$\overline{PG}$	8.2	12.6
			$\overline{GG}$	8.1	12.4
OPA	Mux A	Select	Z Bus	6.9	10.6
OPB			ZP	5.9	9.1
			$\overline{ZD7}$, $\overline{ZD3}$	9.4	14.4
			Z_{Err}	11.4	17.5
CD60	Adder	Shift 1 Bit	Z Bus	15.7	24.2
CD61			ZP	17.0	26.1
CD62			$\overline{C_{out}}$	11.6	17.9
			$\overline{CN3}$, $\overline{CN7}$	13.7	21.0
			$\overline{ZD7}$, $\overline{ZD3}$	18.0	27.7
			HSC	14.4	22.1
			Z_{Err}	21.3	32.7
			$\overline{PG}$	12.0	18.5
			$\overline{GG}$	11.9	18.3
ZL	Latch	Latch Z	Z Bus, ZP	3.3	5.0
			$\overline{ZD7}$, $\overline{ZD3}$	5.5	8.7
			Z_{Err}	7.0	11.6
CL	Latch	Arith	$\overline{CN3}$, $\overline{CN7}$	2.8	4.3

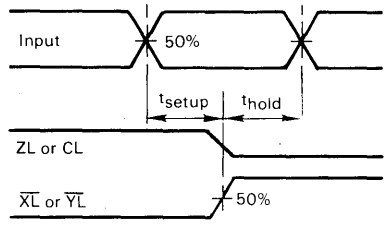
*See Figures 4 and 5 for test definitions and circuit.

FIGURE 4 — SWITCHING WAVEFORM DEFINITION

Propagation Delays



Setup and Hold



TEST PROCEDURE:

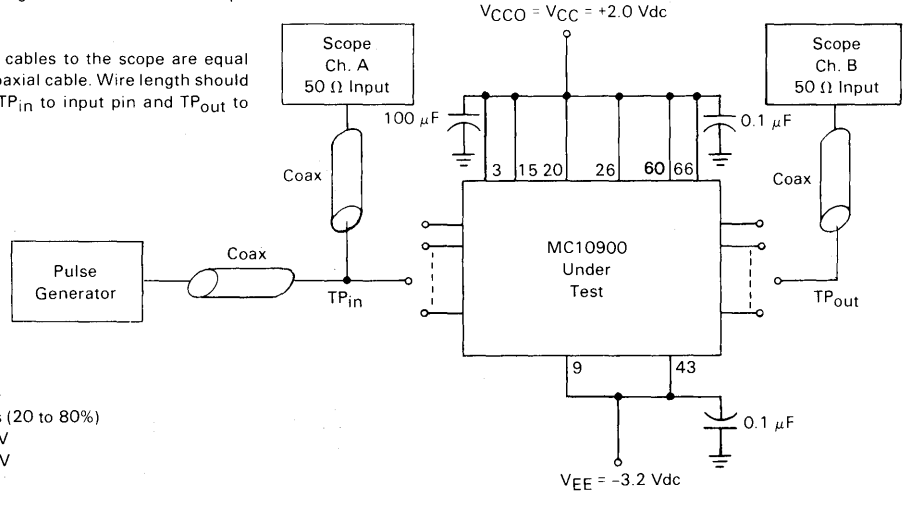
a) Establish setup time with long t_{hold}.

b) Keeping the leading edge of the input constant (t_{setup}) vary the trailing edge of the input to determine t_{hold}.

FIGURE 5 — SWITCHING TIME TEST CIRCUIT

50-ohm termination to ground located in each scope channel input.

All input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be <1/4 inch from TP_{in} to input pin and TP_{out} to output pin.



INPUT PULSE

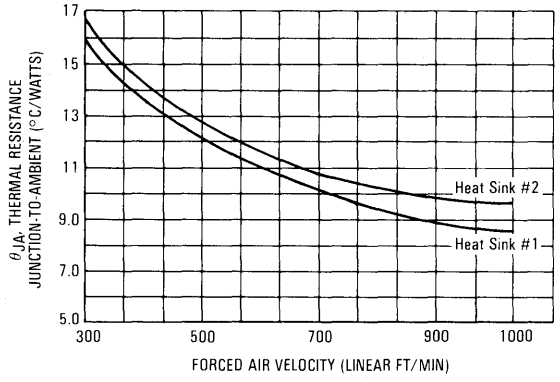
$t_r = t_f = 1.0$ ns (20 to 80%)

$V_{OH} = +1.11$ V

$V_{OL} = +0.31$ V

6

FIGURE 6 — THERMAL CHARACTERISTICS
(TYPICAL)



Heat Sink #1 is from THERMALLOY #15832-1, 3 Horizontal Fins, 0.563 inches square, Model No. 2284C.
Heat Sink #2 is from WAKEFIELD #4493, Vertical Fins, 0.5 inches square.
NOTE: $T_J = (\theta_{JA})(P_D) + T_A$ WHERE T_J is the Junction Temperature, T_A is the Ambient Temperature,
$P_D = (I_{EE})(V_{EE}) + (15\ mW)$ (number of 50 Ω outputs).
Still air θJA (no heat sink) = 35°C/W.

MOTOROLA

MC10901

Advance Information

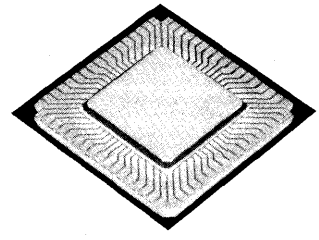
8 X 8 BIT EXPANDABLE MULTIPLIER

The MC10901 is a high speed 8 x 8-bit multiplier that can multiply two eight-bit unsigned or signed 2's complement numbers and generate the sixteen-bit unsigned or signed product. The device can be used as a stand-alone eight-bit multiplier or as a building block for larger multiplier arrays.

The part performs the algebraic function defined as P = XY + K + M + C7, where K and M are 8-bit input fields used to add partial products in an array or to add a constant to the least significant part of the array product. The algorithm used is an asynchronous, sequential add technique. This algorithm eliminates the need for subtractors which simplifies the multiplier network.

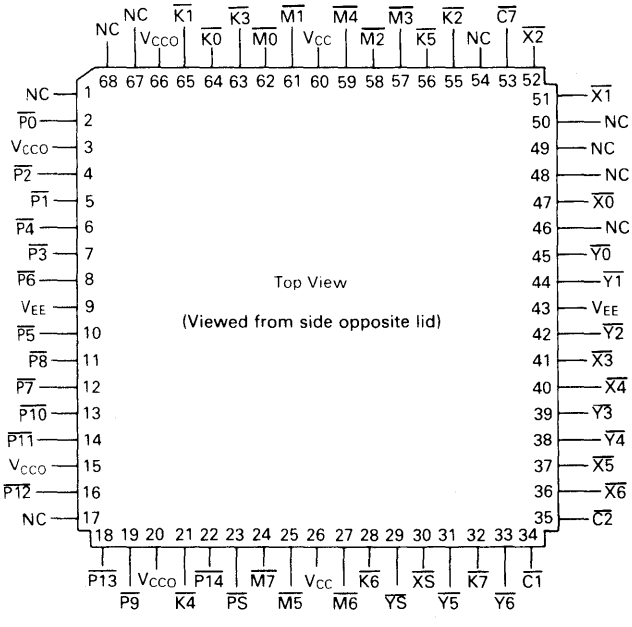
- 8 x 8-Bit Parallel Multiplication.
- Two's complement, Unsigned Magnitude, or Mixed Mode Multiplication.
- Two 8-Bit Expansion Inputs for Summing Partial Products.
- Easily Expandable Into Larger Arrays.
- Single Chip, Bipolar Technology.
- 17 Nanosecond Typical Multiply Time.

MECL-LSI
8 × 8-BIT MULTIPLIER

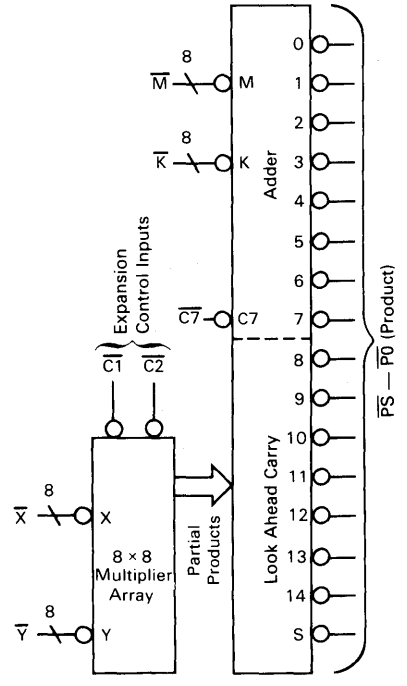


CASE 745 — Z Suffix
68 Pin, JEDEC Std.
Leadless Package
(Bottom view)

INPUT/OUTPUT DIAGRAM



LOGIC DIAGRAM



6

The MC10901 is a high-speed programmable 8 x 8-bit multiplier utilizing the MECL Macrocell Array. The MC10901 uses an asynchronous, sequential add technique for multiplying two numbers in either straight magnitude or two's complement notation. The device generates the function: P = X·Y + K + M + C7, where;

· = times
+ = plus
X = 8-bit multiplicand where X0 is LSB, XS is MSB
Y = 8-bit multiplier where Y0 is LSB, YS is MSB
K = 8-bit constant where K0 is LSB, K7 is MSB
M = 8-bit constant where M0 is LSB, M7 is MSB
C7 = 1-bit constant in bit position 2^7
P = 16-bit product where P0 is LSB and PS is MSB

Two control inputs, $\overline{C1}$ and $\overline{C2}$, are provided for simplifying expansion to larger array sizes. The control inputs can be programmed to select either two's complement or straight magnitude multiplication. A carry-lookahead technique is used to further improve multiplier performance.

DEVICE OPERATION

The multiplication matrix for the MC10901 is shown in Table 1. This matrix shows how the MC10901 calculates the product. The product is the binary sum of all the terms in the matrix. Note that all the terms in the matrix show positive values. The MC10901 requires negative or inverted inputs and produces a product of negative or inverted outputs when positive logic is used. If negative logic is used, no inversion is required on the inputs, while the outputs will be the "true" value.

Operation and expansion of the device are controlled by two inputs $\overline{C1}$ and $\overline{C2}$. When $\overline{C2}$ is at a logic H, the X inputs are in straight magnitude form. A low on $\overline{C2}$ indicates the X inputs are in two's complement form. The Y inputs and $\overline{C1}$ function the same as above. For a straight multiply, control inputs are programmed in the high state. For a two's complement multiply $\overline{C1}$ and $\overline{C2}$ are programmed in the low state. Due to the nature of the algorithm, correction terms need to be added to obtain the correct two's complement signed product. The sign bits of the X and Y inputs must be added to the product in their respective bit locations. This can be accomplished by connecting $\overline{X}$s and $\overline{Y}$s to the $\overline{M7}$ and $\overline{K7}$ inputs, see figure 1. For expansion into larger arrays, an additional input, $\overline{C7}$, has been provided. $\overline{C7}$ accomplishes the same function as a $\overline{M7}$ or $\overline{K7}$ input. If a straight magnitude number is to be multiplied by a two's complement number only the sign bit of the two's complement number is to be added in as correction.

EXPANSION RULES

The MC10901 can be used in larger arrays to produce a two's complement product of 2 two's complement numbers. The following rules apply:

1. For an M-bit by N-bit multiplier, an (M + N) bit product is formed. The number of MC10901's equals (M x N) /64. As an example, a 32 x 32-bit array (figure 3) requires (32 x 32) /64 = 16 packages.

TABLE 1 — MULTIPLICATION MATRIX FOR MC10901
(P = (X) times (Y) plus K plus M plus C7)

								C7							
								K7	K6	K5	K4	K3	K2	K1	K0
								M7	M6	M5	M4	M3	M2	M1	M0
								XS·(C2⊕Y0)	X6·Y0	X5·Y0	X4·Y0	X3·Y0	X2·Y0	X1·Y0	X0·Y0
							XS·(C2⊕Y1)	X6·Y1	X5·Y1	X4·Y1	X3·Y1	X2·Y1	X1·Y1	X0·Y1	
						XS·(C2⊕Y2)	X6·Y2	X5·Y2	X4·Y2	X3·Y2	X2·Y2	X1·Y2	X0·Y2		
	C1·C2·$\overline{YS}$				XS·(C2⊕Y3)	X6·Y3	X5·Y3	X4·Y3	X3·Y3	X2·Y3	X1·Y3	X0·Y3			
	C1·C2·$\overline{XS}$			XS·(C2⊕Y4)	X6·Y4	X5·Y4	X4·Y4	X3·Y4	X2·Y4	X1·Y4	X0·Y4				
	$\overline{C1}$·$\overline{C2}$·XS·YS		XS·(C2⊕Y5)	X6·Y5	X5·Y5	X4·Y5	X3·Y5	X2·Y5	X1·Y5	X0·Y5					
	$\overline{C1}$·C2·XS·$\overline{YS}$	XS·(C2⊕Y6)	X6·Y6	X5·Y6	X4·Y6	X3·Y6	X2·Y6	X1·Y6	X0·Y6						
C1·C2	XS·YS·(C1⊕C2)	YS·(C1⊕X6)	YS·(C1⊕X5)	YS·(C1⊕X4)	YS·(C1⊕X3)	YS·(C1⊕X2)	YS·(C1⊕X1)	YS·(C1⊕X0)							
PS	P14	P13	P12	P11	P10	P9	P8	P7	P6	P5	P4	P3	P2	P1	P0

Note: For magnitude operations (C1 = 0, C2 = 0 or C1 = H, C2 = H), the C7 input must be tied to a "High" voltage state in order to eliminate the possibility of overflow and invalid results. For X = 255, Y = 255, K = 255, and M = 255, the product will be the maximum value possible of 65,535 (PS – P0 = 1). If C7 was also used as an input during magnitude operations, the most significant product bit, PS will be a "1" (PS = L) during an overflow condition where the result exceeds 65,535.

For 2's complement or mixed mode multiplications, the multiplication matrix (Table 1) produces the proper product at the PS through P0 outputs.

2. The normal parallelogram structure consists of several stages, each multiplying 8 bits of multiplier times 8 bits of multiplicand and adds the partial products.
3. The sign bits of the multiplicand and multiplier must be added to the product. As an example, an 8 x 16-bit multiplier would require the sign bit of the 8-bit word to be added to the least significant 8th bit of the product. Likewise the sign bit of the 16-bit word is to be added to the least significant 16th bit of the product. The X sign bit and Y sign bit must be added to the product with a binary weight (power of 2) equivalent to their respective binary weights.
4. The control inputs $\overline{C1}$ and $\overline{C2}$ must be programmed correctly depending on the multiplier type and on the position of the MC10901 within the array:
   A) For magnitude arrays, all control inputs are programmed "H".
   B) For two's complement arrays, the programming is controlled by the position of the multiplier and the terms required by the algorithm.

A simple means of determining the required control line states is shown in the following table:

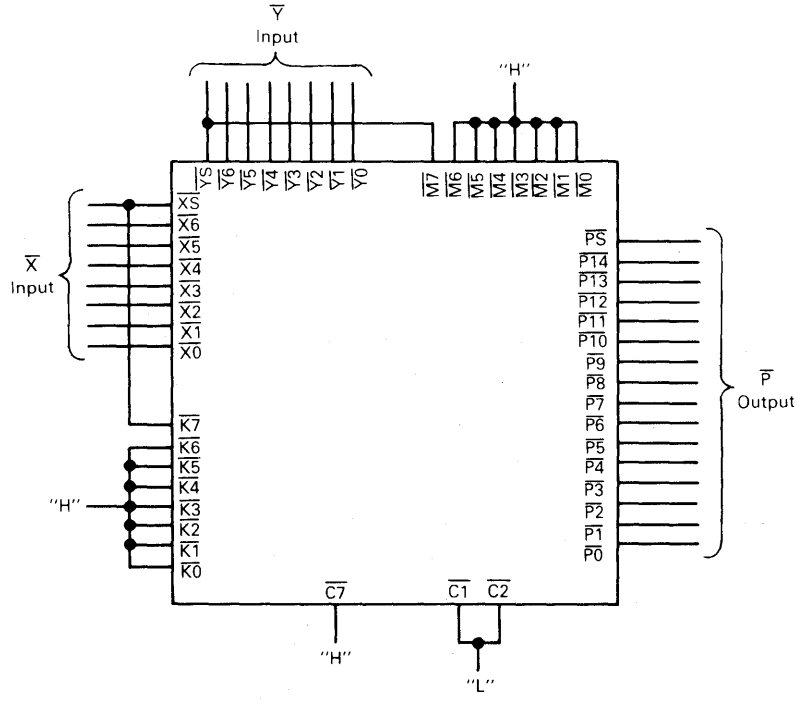
Multiplication Inputs	$\overline{C1}$	$\overline{C2}$
NO SIGN BITS	HI	HI
X_S ONLY	HI	LOW
X_S ONLY	LOW	HI
BOTH SIGN BITS	LOW	LOW

The maximum times possible for various N-bit by N-bit arrays are:

Number Of Bits	Total Multiply Time (ns) Max.	Package Count
8	24.3	1
16	51.8	4
24	81.5	9
32	111.2	16

Because of the versatility of the MC10901, many other arrays can be built. Faster arrays using additional adders, pipeline techniques, one's complement and magnitude multipliers, and truncated product multipliers can be constructed. Applications of such arrays include digital filters, FFT's, complex multipliers, and recursive and nonrecursive filter elements.

FIGURE 1
8 X 8-Bit 2's Complement Multiplier

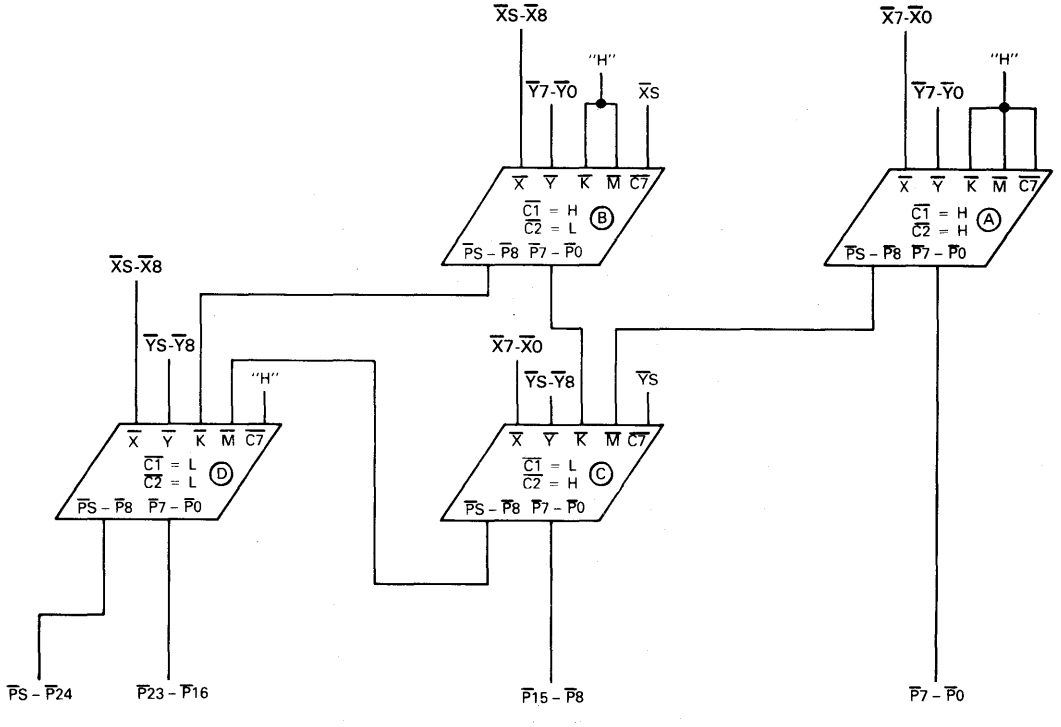


16 X 16-BIT EXAMPLE

Figure 2 shows 4 MC10901's in a 16 x 16-bit array. A 32-bit two's complement product is produced from a 16-bit multiplier and a 16-bit multiplicand. At the first level of multiplication, no partial products have been obtained so the $\overline{K}$ and $\overline{M}$ expansion inputs are tied high. These inputs on the first level can be used to add a constant to the least significant end of the product. Further levels require the $\overline{K}$ and $\overline{M}$ inputs to add the accumulated partial products. Control inputs $\overline{C1}$ and $\overline{C2}$ are programmed according to their relative position of each device in the array. Since both $\overline{X}$ and $\overline{Y}$ are in two's complement form, their respective sign bits must be added to the accumulated products for correction. This can be accomplished by inputing the sign bit of the $\overline{X}$ input to $\overline{C7}$ of device B and sign bit of the $\overline{Y}$ bus to $\overline{C7}$ of device C. The same expansion techniques are extended to the 32 x 32-bit multiplier in Figure 3.

However, when adding the sign bits to the array for correction, the sign bits must be added to the $\overline{C7}$ input of the devices that have $\overline{C1}$ = H, $\overline{C2}$ = L or $\overline{C1}$ = L, $\overline{C2}$ = H in the 32nd bit of the product, as indicated in Figure 3. The sign bits cannot be added to the $\overline{C7}$ input of devices that have $\overline{C1}$ = H and $\overline{C2}$ = H, as indicated in Table 1.

FIGURE 2 — 16 X 16-BIT 2'S COMPLEMENT MULTIPLIER



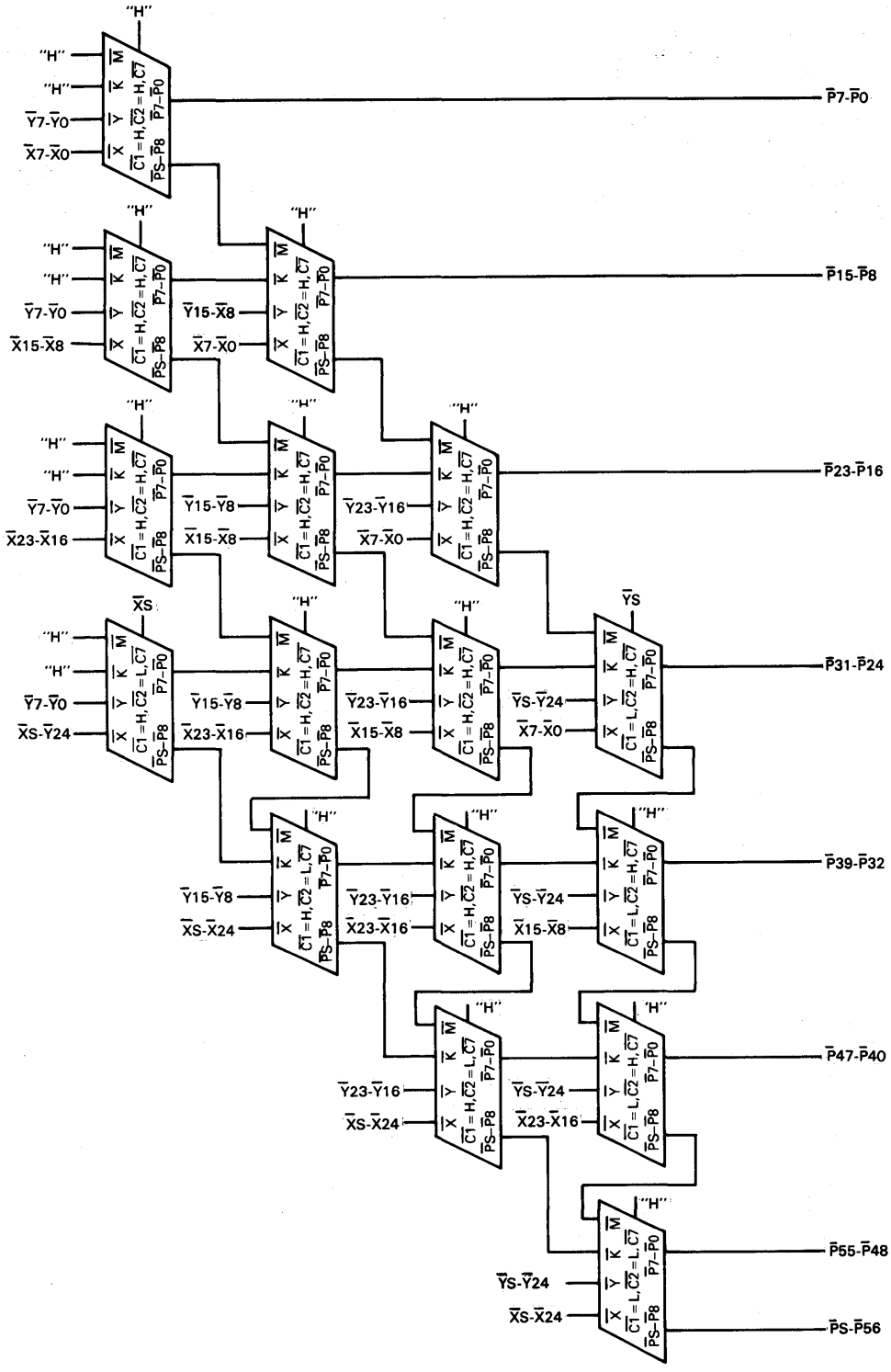


FIGURE 3 — 32 X 32-BIT 2'S COMPLEMENT MULTIPLIER

TABLE 2 — ABSOLUTE MAX RATINGS

Rating	Symbol	Value	Unit
Supply Voltage (V_{CC} = 0)	V_{EE}	-8 to 0	Vdc
Input Voltage (V_{CC} = 0)	V_{in}	0 to V_{EE}	Vdc
Output Source Current — Continuous — Surge	I_o	<30 <100	mAdc
Storage Temperature	T_{stg}	-55 to +150	°C
Junction Temperature	T_J	165	°C

NOTE: 1. Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

TABLE 3 — RECOMMENDED OPERATING CONDITIONS — MC10901

Parameter	Symbol	Value	Unit
Supply Voltage (V_{CC} = 0 Volts)	V_{EE}	−4.68 to −5.72	Vdc
Operating Temperature (Functional)	T_A	0 to +70	°C
Output Drive	—	50 Ω to −2.0 Vdc	—
Max Junction Temp	T_J	130	°C

TABLE 4 — ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board with heatsink and transverse air flow greater than 1000 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown for only one input, or for one set of input conditions. Other inputs tested in the same manner.

@ Test Temperature	Test Voltage Values (Volts) V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
0°C	−0.840	−1.95	−1.145	−1.490	−5.2
+25°C	−0.810	−1.95	−1.105	−1.475	−5.2
+70°C	−0.730	−1.95	−1.050	−1.450	−5.2

Characteristics	Symbol	Pin Under Test	MC10901 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Typ	+25°C Max	+70°C Min	+70°C Max	Unit	Voltage Applied to Pins Listed Below V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	(V_{CCO}) (V_{CC}) Gnd
Power Supply Drain Current	I_{EE}	9,43	—	868	—	695	868	—	868	mAdc	—	—	—	—	9,43	3,15,20 26,60,66
Input Current C1, C2, X, Y	I_{inH}	—	—	650	—	—	650	—	650	µAdc	47	—	—	—		
K4, M4, M5, M6, M7	I_{inH}	—	—	300	—	—	300	—	300	µAdc	47	—	—	—		
All Others	I_{inH}	—	—	200	—	—	200	—	200	µAdc	47	—	—	—		
	I_{INL}	—	—	—	0.5	—	—	—	—	µAdc	—	47	—	—		
Logic "H" Output Voltage	V_{OH}	2	−1.000	−0.840	−0.960	—	−0.810	−0.905	−0.730	Vdc	34,35,53 47	—	—	—		
Logic "L" Output Voltage	V_{OL}	2	−1.950	−1.665	−1.950	—	−1.650	−1.950	−1.625	Vdc	34,35,53	47	—	—		
Logic "H" Threshold Voltage	V_{OHA}	2	−1.02	—	−0.980	—	—	−0.925	—	Vdc	34,35,53	—	47	—		
Logic "L" Threshold Voltage	V_{OLA}	2	—	−1.645	—	—	−1.630	—	−1.605	Vdc	34,35,53	—	—	47		

NOTE: All inputs have input pulldown resistors (~68KΩ) between the input and V_{EE}.

SWITCHING CHARACTERISTICS OVER OPERATING VOLTAGE AND TEMPERATURE RANGE

Table 5 defines the timing characteristics of the MC10901 over operating voltage and temperature ranges. Worst-Case Setup and Hold and Propagation Delays are *calculated* for V_{EE} = −5.2 Volts ± 10% and a $T_J$max = 115°C. The maximum recommended operating junction temperature is +130°C.

Calculated limits are based on several performance factors as described in Motorola's Preliminary Design Manual for the MECL 10,000 Macrocell Array. Factors include worst-case delays due to Macro selections, Fan-Out, Metal Lengths, Wire-OR, and Input Follower options. AC measurements are performed on each device to assure process integrity; however, Motorola does not guarantee limits at this time.

FIGURE 4 — SWITCHING WAVEFORM DEFINITION
Propagation Delays

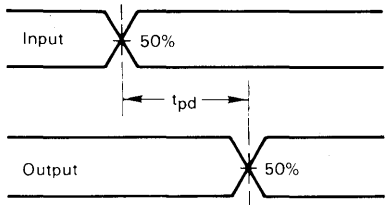


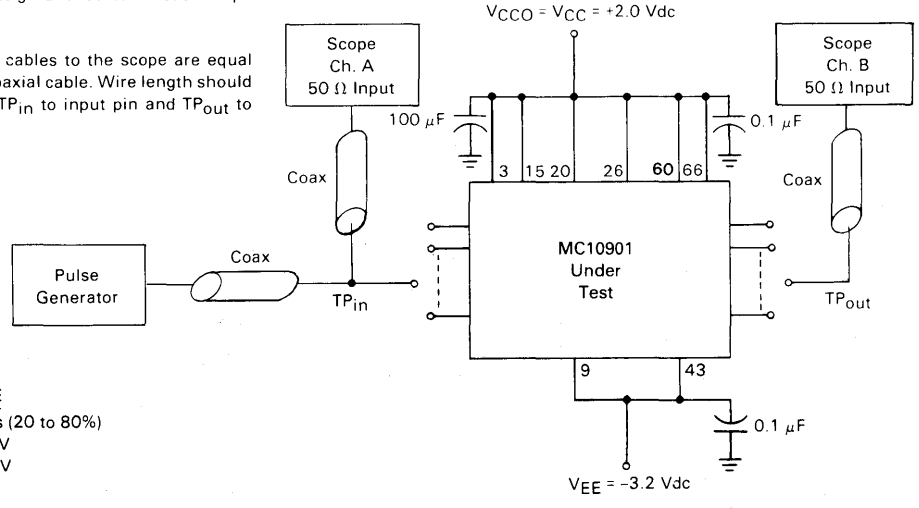
TABLE 5 — PROPAGATION DELAY (Nanoseconds)

Input	Output	0 to 70°C T_A (T_J not to exceed 115°C)	
		Typ	Max
$\overline{X7}$ – $\overline{X0}$, $\overline{Y7}$ – $\overline{Y0}$, $\overline{C1}$, $\overline{C2}$	$\overline{P6}$ – $\overline{P0}$	13.9	19.9
	$\overline{P7}$	13.0	18.6
	$\overline{P14}$ – $\overline{P8}$	17.0	24.3
	$\overline{PS}$	16.3	23.3
$\overline{M7}$ – $\overline{M0}$	$\overline{P6}$ – $\overline{P0}$	7.8	11.2
	$\overline{P7}$	6.9	9.8
	$\overline{P14}$ – $\overline{P8}$	9.3	13.3
	$\overline{PS}$	8.6	12.3
$\overline{K4}$ – $\overline{K0}$	$\overline{P6}$ – $\overline{P0}$	8.2	11.7
	$\overline{P7}$	7.2	10.3
	$\overline{P14}$ – $\overline{P8}$	9.7	13.8
	$\overline{PS}$	8.9	12.7
$\overline{K6}$, $\overline{K5}$	$\overline{P6}$ – $\overline{P0}$	9.4	13.4
	$\overline{P7}$	10.5	15.0
	$\overline{P14}$ – $\overline{P8}$	12.9	18.4
	$\overline{PS}$	12.2	17.4
$\overline{K7}$	$\overline{P7}$	9.9	14.1
	$\overline{P14}$ – $\overline{P8}$	13.9	19.9
	$\overline{PS}$	12.2	18.8
$\overline{C7}$	$\overline{P7}$	10.8	15.4
	$\overline{P14}$ – $\overline{P8}$	14.9	21.2
	$\overline{PS}$	14.1	20.1

FIGURE 5 — SWITCHING TEST CIRCUIT

50-ohm termination to ground located in each scope channel input.

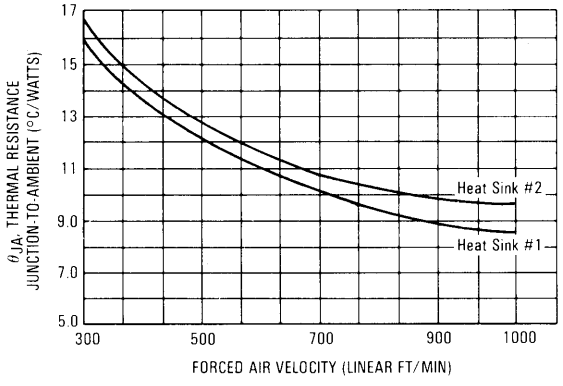
All input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be <1/4 inch from TP_{in} to input pin and TP_{out} to output pin.



INPUT PULSE
$t_r = t_f$ = 1.0 ns (20 to 80%)
V_{OH} = +1.11 V
V_{OL} = + 0.31 V

6

FIGURE 6 — THERMAL CHARACTERISTICS (TYPICAL)



Heat Sink #1 is from THERMALLOY #15832-1, 3 Horizontal Fins, 0.563 inches square, Model No. 2284C.
Heat Sink #2 is from WAKEFIELD #4493, Vertical Fins, 0.5 inches square.
NOTE: $T_J = (\theta_{JA})(P_D) + T_A$ WHERE T_J is the Junction Temperature, T_A is the Ambient Temperature,
$P_D = (I_{EE})(V_{EE}) + (15\ mW)$ (number of 50 Ω outputs).
Still air θJA (with no heat sink) = 35°C/W.

6

MC10902

Advance Information

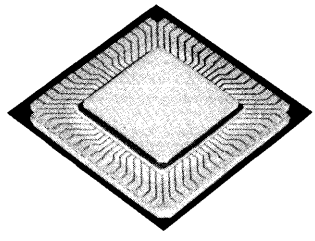
8-BIT BINARY/BCD ALU SLICE

The MC10902 is a high speed ALU building block for digital processors. The circuit operates directly on BCD data in addition to doing normal logic, shift, and binary arithmetic operations. Each part is 8 bits wide and is "sliced" parallel to data flow. The MC10902 easily expands to larger word lengths by connecting circuits in parallel, either with ripple or look-ahead carry.

The MC10902 as illustrated in the logic diagram below contains independently controlled holding latches on all three data inputs. Five function (F) lines select data inputs and logic or arithmetic circuit operation.

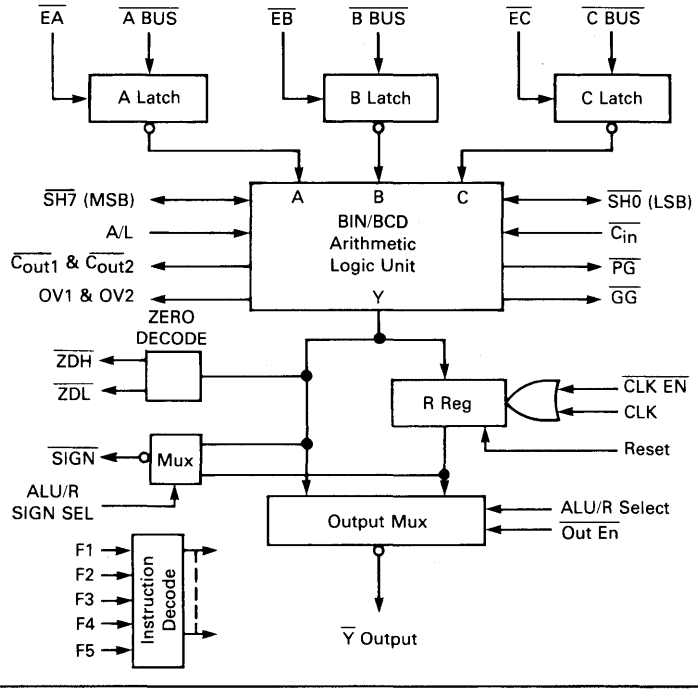
- Member of the M10900 Family utilizing the MECL 10,000 Macrocell Array.
- 34 functions including logic, shift, and both binary and BCD arithmetic.
- Internal 8-bit accumulator with externally available reset, clock, and clock enable.
- Internal look-ahead carry with Propagate and Generate outputs.
- Zero detects for upper and lower 4 bits.
- Select pin for logic or arithmetic shift right.

MECL-LSI
8-BIT BINARY/BCD ALU SLICE



CASE 745
68 Pin, JEDEC Std.
Leadless Package

FIGURE 1 — 8-BIT BINARY/BCD ALU SLICE BLOCK DIAGRAM



PIN ASSIGNMENTS

Pin Name	Number	Description
$\overline{A0}$	46	$\overline{A}$ Input Bus — LSB
$\overline{A1}$	49	$\overline{A}$ Input Bus
$\overline{A2}$	54	$\overline{A}$ Input Bus
$\overline{A3}$	57	$\overline{A}$ Input Bus
$\overline{A4}$	39	$\overline{A}$ Input Bus
$\overline{A5}$	36	$\overline{A}$ Input Bus
$\overline{A6}$	32	$\overline{A}$ Input Bus
$\overline{A7}$	29	$\overline{A}$ Input Bus — MSB
$\overline{B0}$	47	$\overline{B}$ Input Bus — LSB
$\overline{B1}$	52	$\overline{B}$ Input Bus
$\overline{B2}$	55	$\overline{B}$ Input Bus
$\overline{B3}$	59	$\overline{B}$ Input Bus
$\overline{B4}$	38	$\overline{B}$ Input Bus
$\overline{B5}$	35	$\overline{B}$ Input Bus
$\overline{B6}$	31	$\overline{B}$ Input Bus
$\overline{B7}$	28	$\overline{B}$ Input Bus — MSB
$\overline{C0}$	48	$\overline{C}$ Input Bus — LSB
$\overline{C1}$	53	$\overline{C}$ Input Bus
$\overline{C2}$	56	$\overline{C}$ Input Bus
$\overline{C3}$	61	$\overline{C}$ Input Bus
$\overline{C4}$	37	$\overline{C}$ Input Bus
$\overline{C5}$	33	$\overline{C}$ Input Bus
$\overline{C6}$	30	$\overline{C}$ Input Bus
$\overline{C7}$	27	$\overline{C}$ Input Bus — MSB
$\overline{Y0}$	63	$\overline{Y}$ Output Bus — LSB
$\overline{Y1}$	64	$\overline{Y}$ Output Bus
$\overline{Y2}$	67	$\overline{Y}$ Output Bus
$\overline{Y3}$	7	$\overline{Y}$ Output Bus
$\overline{Y4}$	23	$\overline{Y}$ Output Bus
$\overline{Y5}$	21	$\overline{Y}$ Output Bus
$\overline{Y6}$	19	$\overline{Y}$ Output Bus
$\overline{Y7}$	14	$\overline{Y}$ Output Bus — MSB
$\overline{EA}$	51	$\overline{A}$ Latched When $\overline{EA}$ = H
$\overline{EB}$	50	$\overline{B}$ Latched When $\overline{EB}$ = H
$\overline{EC}$	34	$\overline{C}$ Latched When $\overline{EC}$ = H
F1	45	Function Select (See Table 1)
F2	44	Function Select (See Table 1)
F3	41	Function Select (See Table 1)
F4	42	Function Select (See Table 1)
F5	40	Function Select (See Table 1)

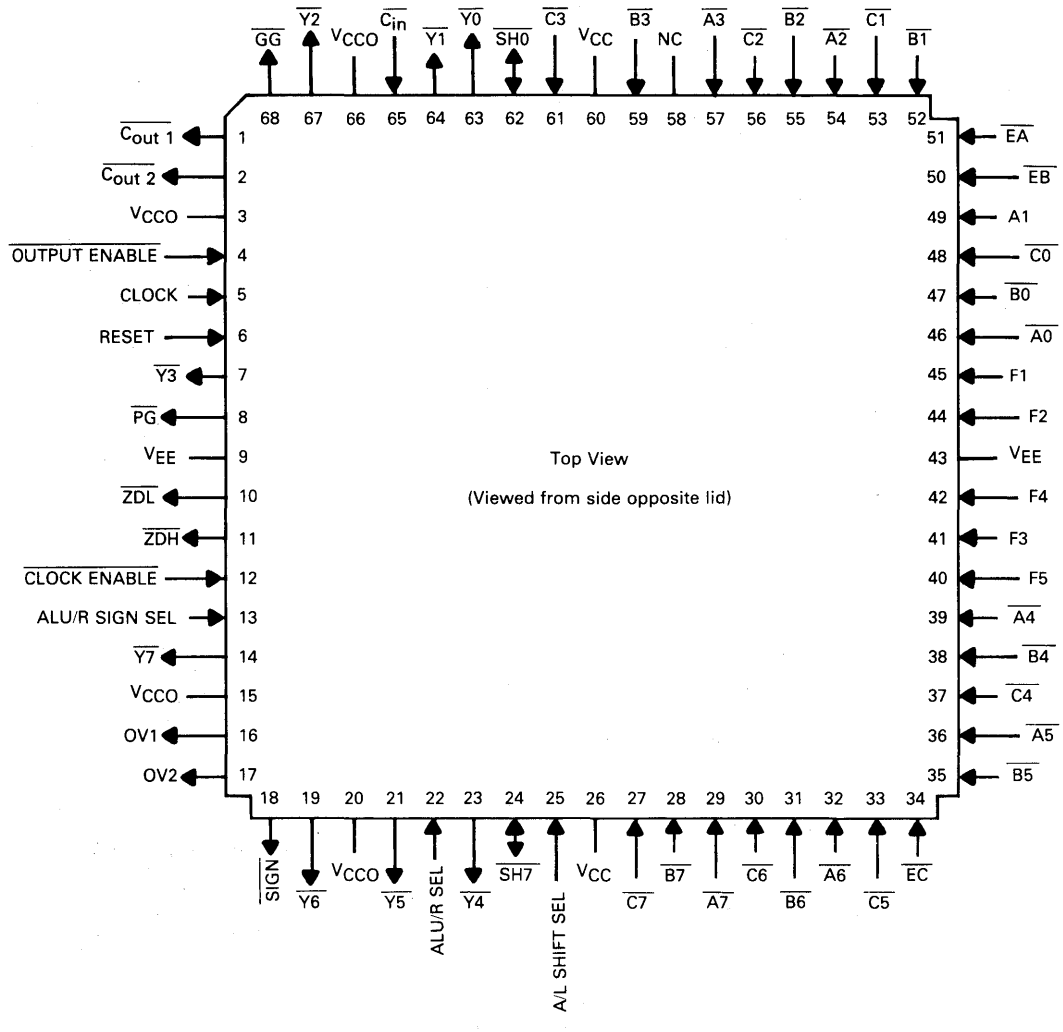
Pin Name	Number	Description
$\overline{C_{out}}$ 1	1	Pins 1 and 2 Tied Together Form $\overline{C_{out}}$ Output
$\overline{C_{out}}$ 2	2	Pins 1 and 2 tied together Form $\overline{C_{out}}$ Output
$\overline{C_{in}}$	65	Carry In
$\overline{PG}$	8	Group Propagate Output
$\overline{GG}$	68	Group Generate Output
OV1	16	Overflow Output for Binary Arithmetic Operations
OV2	17	Overflow Output for Shift Left
ALU/R SEL	22	Selects ALU or R REG for $\overline{Y}$ Outputs
ALU/R SIGN SEL	13	Selects ALU 7 or R 7 for Sign Output
$\overline{SIGN}$	18	$\overline{SIGN}$ Output
$\overline{ZDL}$	10	Zero Detect = L for ALU 0-1-2-3 = L
$\overline{ZDH}$	11	Zero Detect = L for ALU 4-5-6-7 = L
$\overline{OUTPUT\ ENABLE}$	4	$\overline{Y}$ Enabled if L, $\overline{Y}$ = L if Pin 4 = H
RESET	6	Reset R Register When Pin 6 = H
CLOCK	5	Clock R Register on L to H Edge
$\overline{CLOCK\ ENABLE}$	12	Enable Clock When Pin 12 = L
$\overline{SH0}$	62	$\overline{ALU0}$ to $\overline{SH0}$ for Shift Right Output (LSB)
		$\overline{SH0}$ to $\overline{ALU0}$ for Shift Left Input
$\overline{SH7}$	24	$\overline{SH7}$ to $\overline{ALU7}$ for Shift Right (PIN 25 = L)
		$\overline{ALU7}$ to $\overline{SH7}$ for Shift Left Output (MSB)
A/L SHIFT SEL	25	L = Logic Shift Right
		H = Arithmetic Shift Right
V_{EE}	9,43	−5.2 V Supply
V_{CC}	26,60	Ground for Internal Logic
V_{CCO}	3,15,20,66	Ground for Output Drivers
NC	58	Not Used

ABSOLUTE MAXIMUM RATINGS (see Note 1)

Rating	Symbol	Value	Unit
Supply Voltage (V_{CC} = 0)	V_{EE}	−8 to 0	Vdc
Input Voltage (V_{CC} = 0)	V_{in}	0 to V_{EE}	Vdc
Output Source Current — Continuous — Surge	I_o	<30 <100	mAdc
Storage Temperature	T_{stg}	−55 to +150	°C
Junction Temperature	T_J	165	°C

NOTE: 1. Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

FIGURE 2 — INPUT/OUTPUT DIAGRAM



ARCHITECTURAL DESCRIPTION

The MECL 8-bit BCD/Binary ALU Slice is a member of the M10900 family utilizing the MECL 10,000 Macrocell Array. The ALU performs logic, shift, binary arithmetic and BCD arithmetic operations on one or two of three input variables, $\overline{A}$ Bus, $\overline{B}$ Bus, and $\overline{C}$ Bus. Single bit data paths $\overline{C_{in}}$, $\overline{C_{out\ 1}}$, $\overline{C_{out\ 2}}$, $\overline{SH0}$, and $\overline{SH7}$ interconnect MC10902s for longer word lengths. Group propagate and group generate outputs can be used with external look-ahead carry logic for faster system performance.

A $\overline{Y}$ output multiplexer selects output data from either the ALU or R Register outputs. Sign select input selects the ALU or R Register MSB for a special $\overline{SIGN}$ condition code output. Independent selects permit monitoring the ALU sign bit while reading the R Register in a pipelined structure. Other condition code outputs such as zero detect, carry out, and overflow are taken directly off the ALU. Zero Detect is divided into $\overline{ZDL}$ for bits 0 through 3 and $\overline{ZDH}$ for bits 4 through 7 allowing zero detect of BCD digits. The $\overline{C_{out\ 1}}$ and $\overline{C_{out\ 2}}$ must be connected together externally to form $\overline{C_{out}}$.

TABLE 1 — MC10902 ALU LOGIC FUNCTIONS

LOGIC FUNCTIONS								
Function No.	**F5**	**F4**	**F3**	**F2**	**F1**	**A/L**	**ALU Function**	**Y (ALU Output)**
16	H	L	L	L	L	X	OR	$A + B$
18	H	L	L	H	L	X	OR	$\overline{C + B}$
0	L	L	L	L	L	X	NOR	$\overline{A + B}$
2	L	L	L	H	L	X	NOR	$\overline{C + B}$
21	H	L	H	L	H	X	AND	$\overline{A \cdot B}$
5	L	L	H	L	H	X	NAND	$A \cdot B$
7	L	L	H	H	H	X	Logic 1	—
12	L	H	H	L	L	X	Logic 0	—
8	L	H	L	L	L	X	EX OR	$A \oplus B$
10	L	H	L	H	L	X	EX OR	$\overline{C \oplus B}$
11	L	H	L	H	H	X	EX NOR	$\overline{A \oplus B}$
6	L	L	H	H	L	X	Invert	$\overline{C}$
4	L	L	H	L	L	X	Invert	$\overline{A}$
9	L	H	L	L	H	X	Logic	$A + \overline{B}$
14	L	H	H	H	L	X	Logic	$C \cdot \overline{B}$

TABLE 2 — MC10902 ALU ARITHMETIC FUNCTIONS

ARITHMETIC FUNCTIONS								
Function No.	**F5**	**F4**	**F3**	**F2**	**F1**	**A/L**	**ALU Function**	**Y (ALU Output)**
28	H	H	H	L	L	X	Binary Add	A Plus B Plus C_{in}
30	H	H	H	H	L	X	Binary Add	C Plus B Plus C_{in}
29	H	H	H	L	H	X	Binary Sub	A Plus $\overline{B}$ Plus C_{in}
31	H	H	H	H	H	X	Binary Sub	B Plus $\overline{A}$ Plus C_{in}
24	H	H	L	L	L	X	BCD Add*	A Plus B Plus C_{in}
26	H	H	L	H	L	X	BCD Add*	C Plus B Plus C_{in}
25	H	H	L	L	H	X	BCD Sub*	A Plus (9's Complement of B) Plus C_{in}
27	H	H	L	H	H	X	BCD Sub*	B Plus (9's Complement of A) Plus C_{in}
20	H	L	H	L	L	X	Increment	A Plus C_{in}
23	H	L	H	H	H	X	Increment	B Plus C_{in}
22	H	L	H	H	L	X	Increment	$\overline{C}$ Plus C_{in}
15	L	H	H	H	H	X	Complement	$\overline{A}$ Plus C_{in}
13	L	H	H	L	H	X	Complement	$\overline{B}$ Plus C_{in}

*NOTE: For BCD, each four-bit BCD (binary coded decimal) number must have a decimal equivalent of 0 to 9 to be a valid input where A7, A6, A5, A4 is the most significant BCD Digit and A3, A2, A1, A0 is the least significant digit (the B BUS and C BUS inputs are similar).

TABLE 3 — MC10902 ALU SHIFT FUNCTIONS

SHIFT FUNCTIONS								
Function No.	**F5**	**F4**	**F3**	**F2**	**F1**	**A/L**	**ALU Function**	**Y (ALU Output)**
1	L	L	L	L	H	L	Logic Shift Right	A
1	L	L	L	L	H	H	Arithmetic Shift Right	A
3	L	L	L	H	H	L	Logic Shift Right	B
3	L	L	L	H	H	H	Arithmetic Shift Right	B
17	H	L	L	L	H	X	Shift Left	A
19	H	L	L	H	H	X	Shift Left	B

Function Select — F1, F2, F3, F4, and F5

F1 through F5 inputs control the ALU function and select from $\overline{A}$, $\overline{B}$, and $\overline{C}$ Bus inputs. (See Tables 1, 2, and 3.) Two instructions, shift right $\overline{A}$ Bus and shift right $\overline{B}$ Bus, use the A/L SHIFT SELECT input to control the sign bit for arithmetic or logic shifts. Tables 1, 2, and 3 define ALU operation at A, B, C, and Y nodes which are complemented at the package pins.

Data Inputs — $\overline{A0}$–$\overline{A7}$, $\overline{B0}$–$\overline{B7}$, and $\overline{C0}$–$\overline{C7}$

Data enters the MC10902 through three 8-bit data ports. Bit 0 is always the least significant and Bit 7 is the most significant. Each port can be latched independently.

Input Latch Enables — $\overline{EA}$, $\overline{EB}$, and $\overline{EC}$

Each input bus is routed through an 8-bit latch controlled by independent latch enable pins. A low logic level (L) on the enable opens the latch allowing input data to ripple through. A high (H) level latches the circuit holding ALU inputs constant independent of data changes on the bus ports.

Data Outputs — $\overline{Y0}$–$\overline{Y7}$

Data exits the MC10902 through $\overline{Y}$ Bus outputs. As with input data, bit 0 ($\overline{Y0}$) is the least significant and $\overline{Y7}$ the most significant. $\overline{Y}$ output data can be selected from either the ALU or R Register.

Output Mux Controls — ALU/R SEL and $\overline{OUT}$ $\overline{ENABLE}$

Output MUX control is shown in Table 4. $\overline{OUT}$ $\overline{ENABLE}$ forces the $\overline{Y}$ outputs to a MECL low logic level simplifying computer bus architectures.

TABLE 4 — OUTPUT MUX CONTROL

ALU/R SEL	$\overline{OUT\ EN}$	$\overline{Y}$ BUS
L	L	$\overline{R\ REGISTER}$
H	L	$\overline{ALU}$
X	H	OUTPUT LOW (L)

Sign Bit and Control — $\overline{SIGN}$ and ALU/R Sign SEL

A sign bit condition code output displays the most significant bit of the R Register or ALU as selected by the ALU/R SIGN SEL input. A low (L) on the select input gives the R Register MSB and a high (H) selects the ALU MSB.

Note if ALU/R SEL and ALU/R SIGN SEL inputs are connected together, $\overline{SIGN}$ will be the same as $\overline{Y7}$ when the $\overline{Y}$output is enabled ($\overline{OUT\ EN}$ = L).

Carry In — $\overline{C_{in}}$

$\overline{C_{in}}$ is used to interconnect ALUs for word lengths longer than 8 bits. $\overline{C_{in}}$ connects $\overline{C_{out}}$ of the previous ALU for ripple carry or to look-ahead carry logic for look-ahead carry. Carry-in functions only for arithmetic operations and has no effect on logic, see Tables 1, 2, and 3.

Carry Out — $\overline{C_{out\ 1}}$ and $\overline{C_{out\ 2}}$

Carry out, $\overline{C_{out}}$, for the MC10902 is equal to logic $\overline{C_{out\ 1}}$ OR $\overline{C_{out\ 2}}$. IMPORTANT the OR function is implemented externally by connecting pins 1 and 2 together forming a MECL wired OR. Carry out automatically adjusts to binary or BCD arithmetic operations. Carry out may be high or low during ALU logic and shift functions and should be ignored since this is a "don't care" condition.

Group Propagate and Generate — $\overline{PG}$ and $\overline{GG}$

Group propagate and group generate connect to external look-ahead carry logic (MC10179 or equivalent logic) for best performance when several MC10902 circuits operate in parallel. $\overline{PG}$ output goes to a low (L) state when the value of a binary arithmetic calculation is 255 or a BCD calculation is 99 (not including $\overline{C_{in}}$). $\overline{GG}$ goes to a low level when a binary calculation exceeds 255 or a BCD calculation exceeds 99 (not including $\overline{C_{in}}$) and is a high for all other numbers. The $\overline{PG}$ output will be a high level when the value of a binary calculation is less than 255 or a BCD calculation is less than 99 (not including $\overline{C_{in}}$). Propagate and generate may be high or low during ALU logic and shift functions and should be ignored since this is a "don't care" condition.

Overflow — OV1 and OV2

OV1 is the overflow for binary arithmetic operations, while OV2 is the overflow for shift left operations. These two signals can be connected together (wire ORed) so that either condition will cause an overflow condition. In a system, the most significant slice is used to form the overflow function.

1. OV1 is enabled only during binary arithmetic operations (OV1 = L for all non-binary arithmetic operations). OV1 = H means that the sign bit (MSB) is in error due to the result exceeding the maximum positive or negative word value. OV 1 = ($C_{out} \oplus C7$) · (function No. 13, 15, 20, 22, 23, 28-31) where C7 is the carry-in for generating ALU bit Y7.
2. OV2 is enabled only during shift left operations (OV2 = L for all other operations). OV2 = H means the sign bit has changed state due to the shift left operation. OV2 = (SH7 ⊕ Y7) · (function 17, 19)

Zero Detect — $\overline{ZDL}$ and $\overline{ZDH}$

Zero Detects show when the lower ($\overline{ZDL}$) or upper ($\overline{ZDH}$) four bits of the ALU results are all positive logic zero (low L logic state). $\overline{ZDL}$ and $\overline{ZDH}$ can be externally connected together generating an 8-bit $\overline{ZD}$. Zero detect outputs are defined by the following equations:

$$\overline{ZDL} = ALU0 + ALU1 + ALU2 + ALU3$$

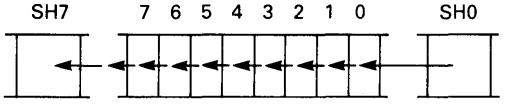
$$\overline{ZDH} = ALU4 + ALU5 + ALU6 + ALU7$$

6

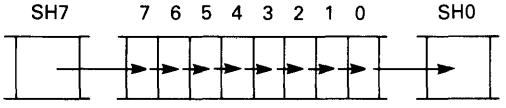
Shift Signals — $\overline{SH0}$, $\overline{SH7}$, and A/L Shift Select

$\overline{SH0}$ and $\overline{SH7}$ are bidirectional single bit data lines. For shift right, $\overline{SH0}$ is an output and $\overline{SH7}$ is an input. For shift left, $\overline{SH0}$ is an input and $\overline{SH7}$ is an output. In addition, shift right may be logic or arithmetic controlled by the A/L SHIFT SELECT as shown below. The $\overline{SH0}$ and $\overline{SH7}$ are "low" for all ALU operations not requiring shift right or shift left.

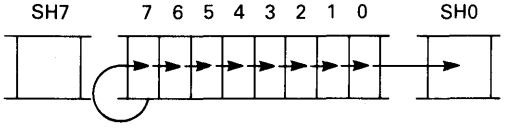
SHIFT LEFT (A/L SEL = DON'T CARE)



LOGIC SHIFT RIGHT (A/L SEL = L)



ARITHMETIC SHIFT RIGHT (A/L SEL = H)



R Register Control — CLOCK, $\overline{\text{CLOCK EN}}$, and RESET

The MC10902 has a built in 8-bit register, R Register (composed of master/slave flip-flops), primarily intended for pipeline system structures. The R Register can also function as an accumulator by connecting the $\overline{Y}$ outputs to one of the three input buses. The respective bus input latch can hold accumulator data, thus freeing the $\overline{Y}$ Bus for ALU output results.

CLOCK and $\overline{\text{CLOCK EN}}$ are equal inputs, logic ORed together as shown on the Page 1 logic diagram. Either input will clock the R Register on a low to high transition if the other input is low (L). Assigning pin 5 as CLOCK, pin 12 can be used for clock enable. A logic low (L) on $\overline{\text{CLOCK EN}}$ enables CLOCK to update R Register with ALU results on each positive going CLOCK transition. A high (H) on $\overline{\text{CLOCK EN}}$ disables the CLOCK. Care should be taken to disable the clock, low to high transition on $\overline{\text{CLOCK EN}}$, while the CLOCK is high. Otherwise $\overline{\text{CLOCK EN}}$ could clock the R REGISTER.

Reset sets the R Register to all bits equal logic low (L). ($\overline{Y}$ bus output = H when R register is selected).

Reset R Register = Reset · (CLOCK + $\overline{\text{CLOCK EN}}$)

Reset can be made to appear independent of clocking signals (asynchronous) by connecting RESET to $\overline{\text{CLOCK EN}}$ forcing both high at the same time. However, a narrow positive going spike (1 to 2 ns wide) on the R Register output can result on the leading edge of Reset. This narrow pulse can also occur if the Reset = H while clocking the R register (CLK switches from L to H while $\overline{\text{CLOCK EN}}$ = L).

Positive versus Negative Logic

System designers use MECL 10,000 in both positive and negative logic formats. Positive logic has MECL VOH (approx. −0.9V) for logic 1 and MECL VOL (approx −1.7 V) for logic 0. Negative logic reverses logic 1 and 0 voltage definitions with VOL being a logic 1. This data sheet is written around positive logic definitions. Tables and descriptions are written in terms of high (H) and low (L) logic levels to simplify translation between formats.

FIGURE 3 — 16-BIT ALU EXAMPLE

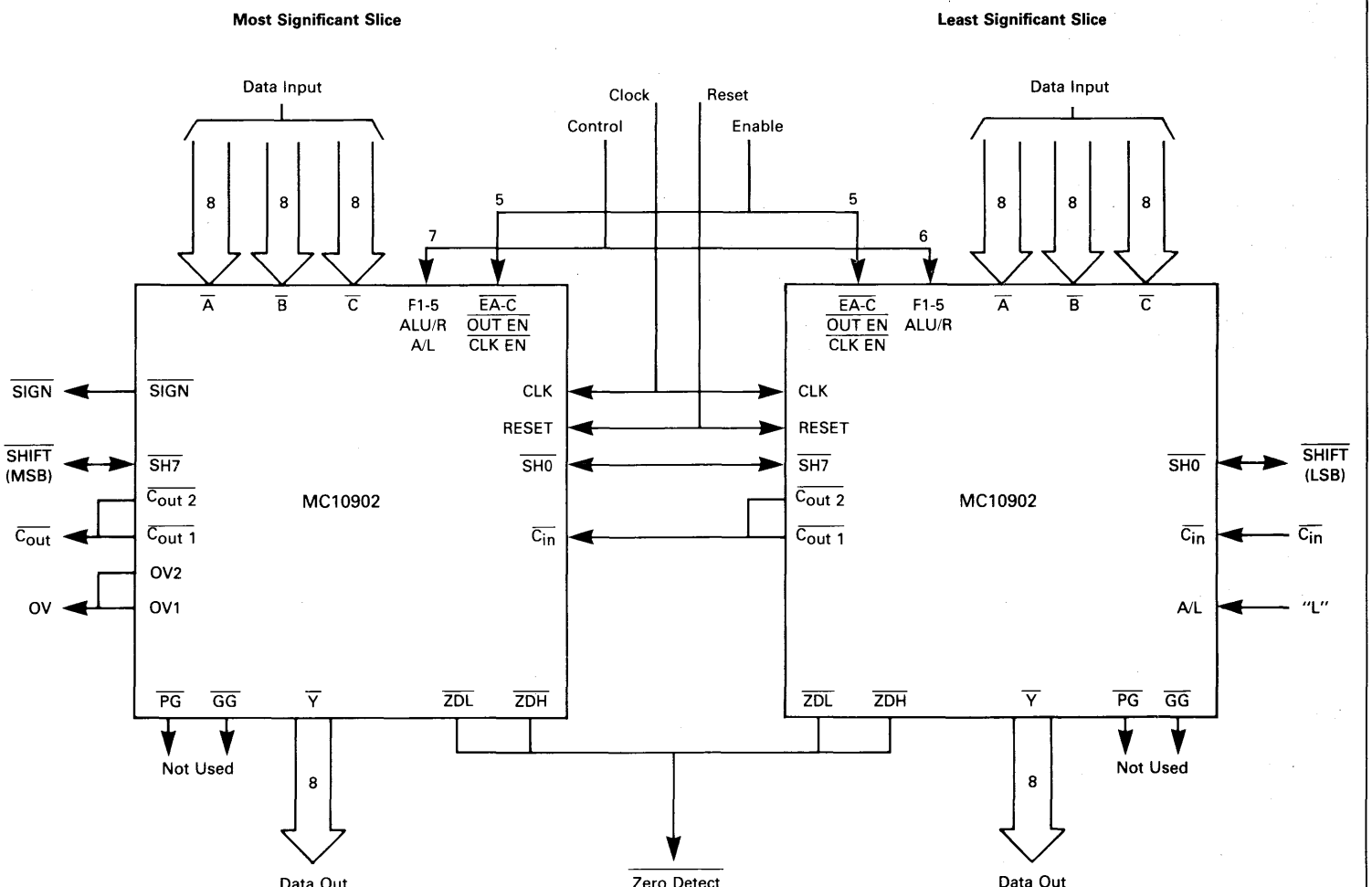


TABLE 5 — RECOMMENDED OPERATING CONDITIONS — MC10902

Parameter	Symbol	Value	Unit
Supply Voltage (V_{CC} = 0 Volts)	V_{EE}	−4.68 to −5.72	Vdc
Operating Temperature (Functional)	T_A	0 to +70	°C
Output Drive	—	50 Ω to −2.0 Vdc	—
Junction Temp	T_J	130 Max	°C

TABLE 6 — ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board with heat sink and transverse air flow greater than 1000 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown for only one input, or for one set of input conditions. Other inputs tested in the same manner.

@ Test Temperature	Test Voltage Values Volts V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
0°C	−0.840	−1.950	−1.145	−1.490	−5.2
+25°C	−0.810	−1.950	−1.105	−1.475	−5.2
−70°C	−0.730	−1.950	−1.050	−1.450	−5.2

Characteristics	Symbol	Pin Under Test	MC10902 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Typ	+25°C Max	+70°C Min	+70°C Max	Unit	Voltage Applied to Pins Listed Below V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	(V_{CCO}) (V_{CC}) Gnd
Power Supply Drain Current	I_{EE}	9,43	—	890	—	712	890	—	890	mAdc	—	—	—	—	9,43	3,15,20 26,60,66
Input Current	I_{inH}	4	—	1750	—	—	1750	—	1750	μ Adc	4	—	—	—		
		40 45,42	—	750	—	—	750	—	750	μ Adc	40	—	—	—		
		24, 44,41, 50,51, 65,34, 12,5, 22,6	—	550	—	—	550	—	550	μ Adc	65	—	—	—		
		*	—	200	—	—	200	—	200	μ Adc	46	—	—	—		
	I_{inL}	*	0.5	—	0.5	—	—	0.5	—	μ Adc	—	46				
Logic "1" Output Voltage	V_{OH}	63	−1.000	−0.840	−0.960	—	−0.810	−0.905	−0.730	Vdc	5,6,13,22 25,65	—	—	—		
Logic "0" Output Voltage	V_{OL}	63	−1.950	−1.665	−1.950	—	−1.650	−1.950	−1.625	Vdc	13,22,25 41,44,45,65	—	—	—		
Logic "1" Threshold Voltage	V_{OHA}	63	−1.02	—	−0.980	—	—	−0.925	—	Vdc	—	—	5,6,13,22, 25,65	—		
Logic "0" Threshold Voltage	V_{OLA}	63		−1.645	—	—	−1.630	—	−1.605	Vdc	—	—	13,22,25,41 44,45,65	—		

*All or All Other Inputs

NOTE: All inputs have input pulldown resistors (~ 68 kΩ) between input and V_{EE}

Switching Characteristics Over Operating Voltage and Temperature Range

Tables 7 and 8 define timing characteristics of the MC10900 over operating voltage and temperature ranges. Worst case Setup and Hold and Propagation Delays are *calculated* for VEE = −5.2 volts ± 10% and a T_J max = 115°C. The maximum recommended operating junction temperature is +130°C.

Calculated limits are based on several performance factors as described in Motorola's Preliminary Design Manual for the MECL 10,000 Macrocell Array. Factors include worst case delays due to Macro selections, Fan-Out, Metal Lengths, Wire-Or, and Input Follower options. AC measurements are performed on each device to assure process integrity; however, Motorola does not guarantee limits at this time.

TABLE 7 — SET UP AND HOLD TIMES (NANOSECONDS) 0 to 70°C T_A (T_J NOT TO EXCEED 115°C)*

Input	Clock (Ref. Edge L To H)	Set up (Min)	Hold (Min)
$\overline{A}$, $\overline{B}$, $\overline{C}$ BUS	$\overline{EA}$, $\overline{EB}$, $\overline{EC}$	1.6	+0.6
A, B, C, BUS	CLK, $\overline{CLK\ EN}$	16.3	−2.0
F1, F2, F3, F4, F5	CLK, $\overline{CLK\ EN}$	17.9	−0.9
$\overline{SH7}$, $\overline{SH0}$, A/L SHIFT SEL	CLK, $\overline{CLK\ EN}$	8.7	−0.8
$\overline{C_{in}}$	CLK, $\overline{CLK\ EN}$	8.9	−0.2
$\overline{EA}$, $\overline{EB}$, $\overline{EC}$ (H→L EDGE)	CLK, $\overline{CLK\ EN}$	17.0	−2.5
$\overline{CLOCK\ EN}$ (H→L EDGE)	CLK	4.4	+0.4

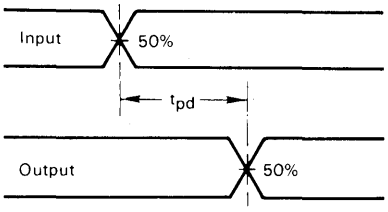
*See Figures 4 and 5 for test definitions and circuit

TABLE 8 — PROPAGATION DELAY (NANOSECONDS) 0 TO 70°C T_A (T_J NOT TO EXCEED 115°C)

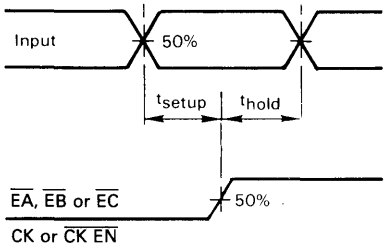
Input	Output	Max
$\overline{A}$, $\overline{B}$, $\overline{C}$ BUS	$\overline{Y}$ OUTPUT, $\overline{ZDH}$, $\overline{ZDL}$, $\overline{SIGN}$	17.9
$\overline{EA}$, $\overline{EB}$, $\overline{EC}$	$\overline{Y}$ OUTPUT, $\overline{ZDH}$, $\overline{ZDL}$, $\overline{SIGN}$	18.7
F1, F2, F3, F4, F5	$\overline{Y}$ OUTPUT, $\overline{ZDH}$, $\overline{ZDL}$, $\overline{SIGN}$	19.6
$\overline{SH7}$, $\overline{SH0}$, A/L SHIFT SELECT	$\overline{Y}$ OUTPUT, $\overline{ZDH}$, $\overline{ZDL}$, $\overline{SIGN}$	10.3
$\overline{C_{in}}$	$\overline{Y}$ OUTPUT, $\overline{ZDH}$, $\overline{ZDL}$, $\overline{SIGN}$	10.5
CLK, $\overline{CLK\ EN}$	$\overline{Y}$ OUTPUT, $\overline{SIGN}$	5.8
ALU/R SEL, ALU/R SIGN SEL	$\overline{Y}$ OUTPUT, $\overline{SIGN}$	4.4
$\overline{RESET}$	$\overline{Y}$ OUTPUT, $\overline{SIGN}$	7.8
$\overline{OUT\ EN}$	$\overline{Y}$ OUPUT, $\overline{SIGN}$	5.4
$\overline{A}$, $\overline{B}$, $\overline{C}$ BUS	$\overline{C_{out\ 1}}$, $\overline{C_{out\ 2}}$, $\overline{PG}$, $\overline{GG}$	11.5
$\overline{EA}$, $\overline{EB}$, $\overline{EC}$	$\overline{C_{out\ 1}}$, $\overline{C_{out\ 2}}$, $\overline{PG}$, $\overline{GG}$	13.0
F1, F2, F3, F4, F5	$\overline{C_{out\ 1}}$, $\overline{C_{out\ 2}}$, $\overline{PG}$, $\overline{GG}$	12.8
$\overline{C_{in}}$	$\overline{C_{out\ 2}}$	4.3
F1, F2, F3, F4, F5	OV1, OV2	17.3
$\overline{A}$, $\overline{B}$, $\overline{C}$ BUS	OV1, OV2	16.2
$\overline{EA}$, $\overline{EB}$, $\overline{EC}$	OV1, OV2	17.5
$\overline{C_{in}}$	OV1	9.5
$\overline{A}$, $\overline{B}$, $\overline{C}$ BUS	$\overline{SH0}$, $\overline{SH7}$	8.6
$\overline{EA}$, $\overline{EB}$, $\overline{EC}$	$\overline{SH0}$, $\overline{SH7}$	9.5
F1, F2, F3, F4, F5	$\overline{SH0}$, $\overline{SH7}$	9.7

FIGURE 4 — SWITCHING WAVEFORMS

Propagation Delays



Setup and Hold



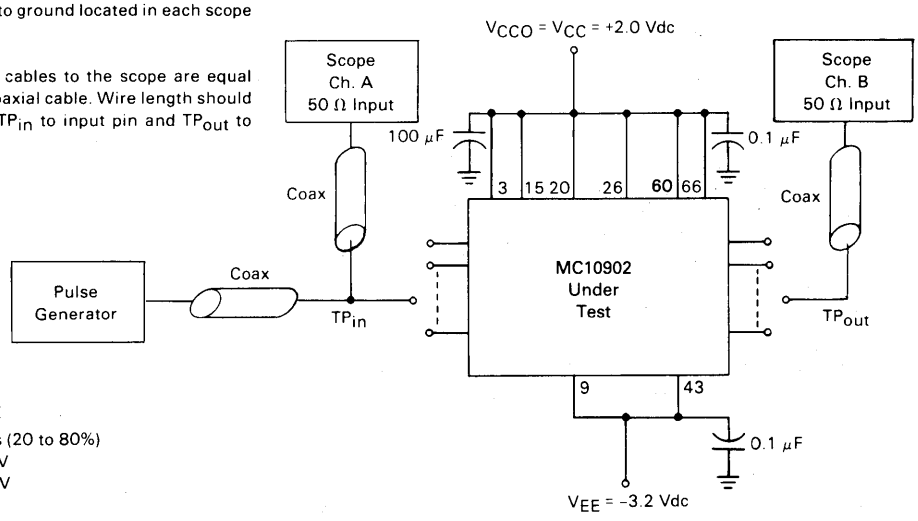
TEST PROCEDURE:
a) Establish setup time with long t_{hold}.
b) Keeping the leading edge of the input constant (t_{setup}) vary the trailing edge of the input to determine t_{hold}.

6

FIGURE 5 — SWITCHING TIME TEST CIRCUIT

50-ohm termination to ground located in each scope channel input.

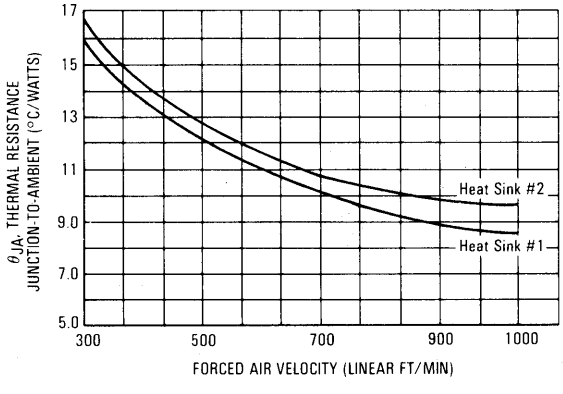
All input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be <1/4 inch from TP_{in} to input pin and TP_{out} to output pin.



INPUT PULSE

$t_r = t_f = 1.0$ ns (20 to 80%)
$V_{OH} = +1.11$ V
$V_{OL} = +0.31$ V

FIGURE 6 — THERMAL CHARACTERISTICS (TYPICAL)



Heat Sink #1 is from THERMALLOY #15832-1, 3 Horizontal Fins, 0.563 inches square, Model No. 2284C.
Heat Sink #2 is from WAKEFIELD #4493, Vertical Fins, 0.5 inches square.
NOTE: $T_J = (\theta_{JA})(P_D) + T_A$ WHERE T_J is the Junction Temperature, T_A is the Ambient Temperature,
$P_D = (I_{EE})(V_{EE}) + (15$ mW) (number of 50 Ω outputs).
Still air θJA (no heat sink) = 35°C/W.

MOTOROLA

MC10904

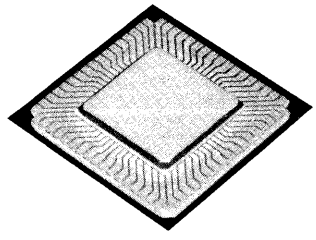
Product Preview

8-BIT MICRO-CODE SEQUENCER

The MC10904 is a high speed, expandable micro-code sequencer slice. This circuit, along with other members of the M10900 family, provides LSI logic building blocks for state-of-the-art computers, controllers, and other uses of high performance digital logic. The MC10904 as diagrammed in Figure 1 contains two main sections, condition input control and micro-code address control. Features include:

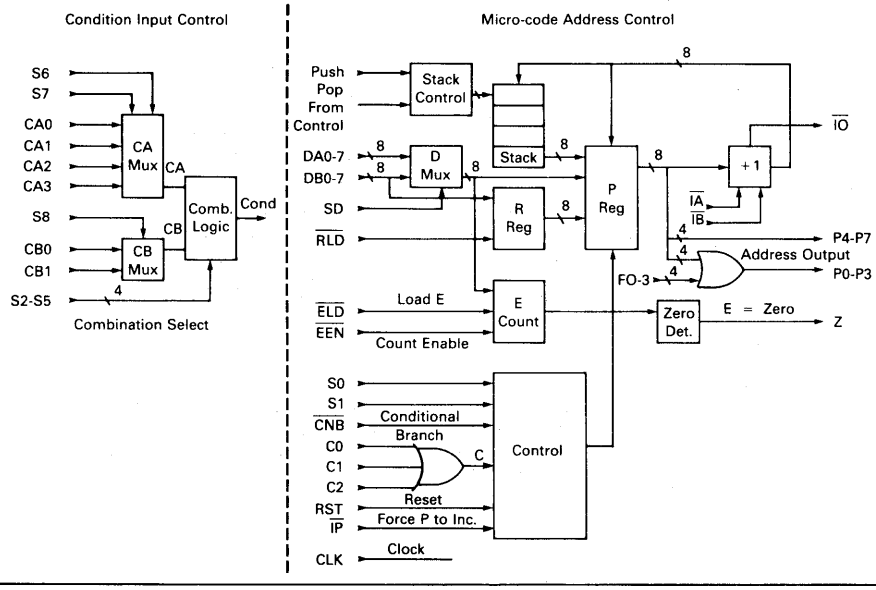
- Member of the M10900 family utilizing the MECL 10,000 Macrocell Array.
- 8-Bit slice, expandable to 24 bits (3 chips) with no extra logic.
- 4 level subroutine stack that can be pushed and popped simultaneously.
- Two direct data inputs for jump and conditional branch destinations.
- A special P counter pin ($\overline{IP}$) simplifies loading RAM writeable macroprogram memory. The input can also be used to hold the system on a microinstruction for diagnostics.
- Multi-way branch on the lowest 4 P output bits allows a 16-way branch.
- Six branch condition inputs can be combined in 14 logic patterns to minimize external branch control logic.
- R register for holding microprogram address information.
- An 8-bit counter for repeating instructions or sequences. Can also be used to count events, conditions, or time.

MECL-LSI
8-BIT MICRO-CODE
SEQUENCER SLICE



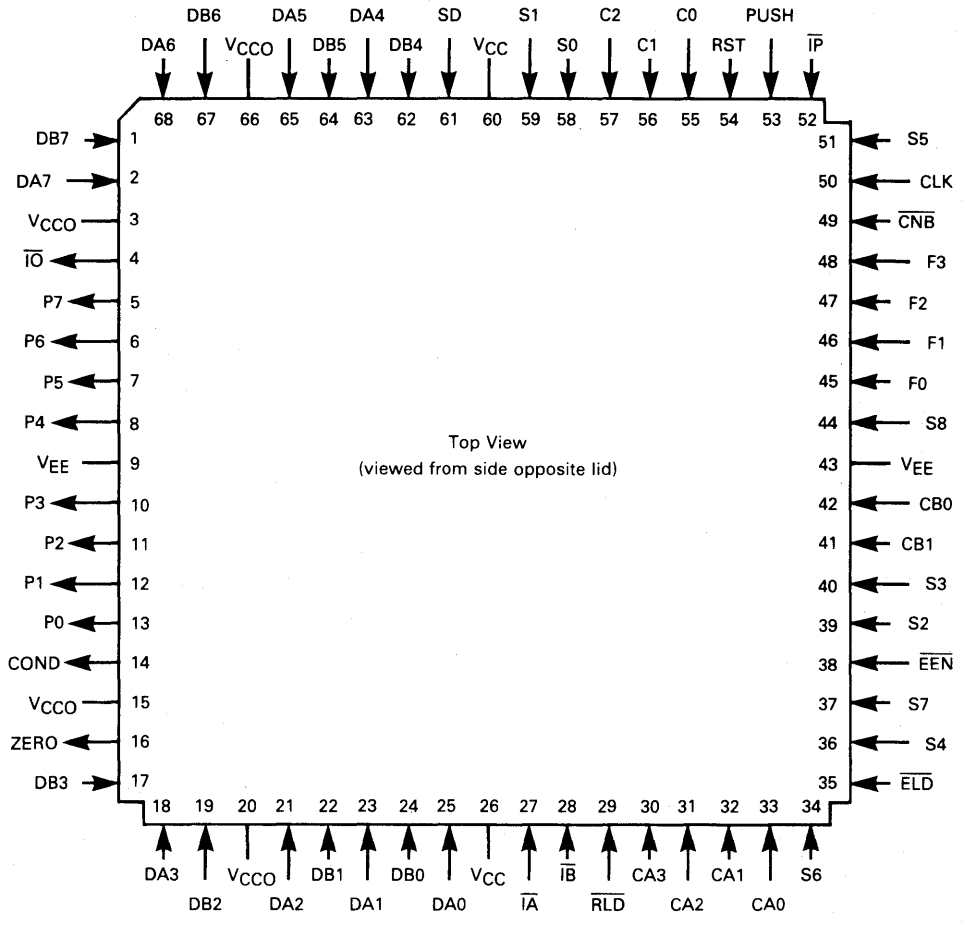
CASE 745
68 Pin, JEDEC Std.
Leadless Package

FIGURE 1 — 8-BIT MICRO-CODE SEQUENCER BLOCK DIAGRAM



6

FIGURE 2 — INPUT/OUTPUT DIAGRAM



ARCHITECTURAL DESCRIPTION

The M10900 family is a line of high performance standard digital LSI products designed around the MECL Macrocell Array. The MC10904 8-bit Micro-code Sequencer circuit controls a microprogram by generating microcode memory addresses, providing a means for sequencing through programs, and making micro-code conditional branch decisions. Each part is 8 bits wide and circuits are easily combined to meet microprogram memory size requirements.

The MC10904 P Register (Figure 1) holds the current micro-code address and supplies address information on outputs P0-P7. Next address is computed from inputs DA0-DA7, inputs DB0-DB7, and several points internal to the circuit including P Register incrementer, 4 deep subroutine stack, and the R Register. Select lines and conditional branch inputs control circuit operation. The 4 bottom P address outputs are gated with force inputs F0-F3, thus providing 16-multiway branch capability.

Each MC10904 handles up to six condition inputs divided into groups of four (CA0-CA3), and two (CB0-CB1). One bit from each group can be used by itself or logically combined with a bit from the other group to determine branch condition status. For example, a single micro-code instruction could incorporate "branch if less than or equal" by having an ALU sign bit on one set of condition inputs and zero detect on the other, then with S2-S5 select "A or B" in the Conditional Combinational Logic. The six condition inputs expand with additional sequencer circuits. Two MC10904s can address 64K micro-code words and provide up to 12 conditional branch inputs.

PIN FUNCTION DESCRIPTION

Data Inputs — DA0-DA7 and DB0-DB7

Two 8-bit ports, DA and DB, are direct inputs for next address information. Bit 0 is the least significant bit and bit 7 the most significant. Either DA or DB may be selected by the D MUX and routed to the P Register. In addition, DB has a direct path to the R Register so that DA can be routed to the P register and DB simultaneously loaded into the R Register for storage. Either DA or DB can be selected to the Event (E) Counter. In some applications the DA inputs could come from an initial address lookup table (or similar function) while DB inputs connect to microcode memory next address field.

Program Address Outputs — P0-P7

P0 through P7 display current micro-code address held in the P Register. The four lowest bits P0 through P3 can be overridden and forced high (positive logic 1) by F inputs. P outputs normally connect directly to microcode memory address inputs.

Multi-Way Branch Inputs — F0-F3

Four input pins F0, F1, F2, and F3 force P0, P1, P2, and P3 respectively high for multi-way branches. Unused F inputs should be held at a low logic level (L).

Incrementer Enable Inputs — $\overline{IA}$ and $\overline{IB}$

Incrementer enable inputs, when both low, enable the P Register incrementer (+ 1 block in Figure 1) to function. If either enable input is high the incrementer is disabled and output equals input. $\overline{IA}$ and $\overline{IB}$ are either connected to a previous stage MC10904 $\overline{IO}$ output or used as a control input to override the incrementer. Unused inputs should be held low.

Incrementer Carry Output — $\overline{IO}$

Carry output indicates that the current count in the P register is maximum (all 1 bits) and the next cycle, if enabled, will roll the P Register to zero. Carry out is actually an anticipation of carry because the carry enable inputs are not used to derive the signal. $\overline{IO}$ connects to either $\overline{IA}$ or $\overline{IB}$ inputs of all MC10904 circuits above it.

Select D Input — SD

SD controls an 8-bit, 2-input multiplexer that selects either DA or DB inputs to an internal 8-bit bus. The bus goes to both the P Register and E counter. (See Table 1.) This bit is normally driven by the microcode memory.

TABLE 1 — SELECT DATA OPERATION

SD	Register/Counter Input
L	DA Input
H	DB Input

LOAD R REGISTER — $\overline{RLD}$

$\overline{RLD}$ enables the R Register to be loaded from the DB inputs on a positive going clock, CLK, input. (See Table 2.)

TABLE 2 — R REGISTER OPERATION

$\overline{RLD}$	R Register
L	Parallel Load
H	Hold Data

Load and Enable E Counter — $\overline{ELD}$ and $\overline{EEN}$

$\overline{ELD}$ enables the E Counter to be parallel loaded from the D MUX output on a positive going clock (CLK) edge. $\overline{EEN}$ enables the E counter to decrement by 1 on each positive going clock edge. (See Table 3.)

TABLE 3 — COUNTER OPERATION

$\overline{ELD}$	$\overline{EEN}$	E Count Output
L	L	Parallel Load
L	H	Parallel Load
H	L	Decrement
H	H	No Change

Note: The E Counter will only decrement to zero, then will hold that value until loaded with a non-zero value (e.g., the counter does not rollover past zero). $\overline{ELD}$ is normally driven by microcode memory while $\overline{EEN}$ is connected as required.

E Counter Zero Detect Output — Z

Zero Detect signifies all E Counter bits are low. (See Table 4.) The counter equals zero state disables the decrement function in Table 3.

TABLE 4 — ZERO DETECT OPERATIONS

Z	E Counter
L	$\overline{Zero}$
H	Zero

Condition Inputs — C0, C1, and C2

The logic OR of C0, C1, and C2, Table 5 is the test point (C) for conditional branch decisions, refer to Table 6. Test node C also affects stack push and pop operations as shown in Tables 7 and 8. The three condition inputs C0, C1, and C2 interconnect to MC10904 condition, COND, outputs insuring multiple parts all test the same branch point. See the condition output description for additional details. Unused C0, C1, or C2 inputs should be held low.

TABLE 5 — CONDITION INPUT OPERATIONS

C0	C1	C2	C (Internal Test Point)
L	L	L	L
H	X	X	H
X	H	X	H
X	X	H	H

Conditional Branch Input — $\overline{CNB}$

$\overline{CNB}$ selects between conditional branch and unconditional jump. A low (L) level on this input enables the MC10904 to test C0, C1, and C2 and determine the next P Register address. A high (H) level on $\overline{CNB}$ overrides the C inputs enabling a direct jump. (See Table 6.) $\overline{CNB}$ also affects stack push and pop operations as shown in Tables 7 and 8.

TABLE 6 — P REGISTER SOURCE CONTROL

S1	S0	$\overline{CNB}$	C*	Next P	Instruction
L	L	X	X	P Incr	Increment
L	H	H	X	D Bus	Direct Jump
L	H	L	H	D Bus	Br. Cond. Met
L	H	L	L	P Incr	Br. Cond. Failed
H	L	H	X	R Reg	Direct Jump
H	L	L	H	R Reg	Br. Cond. Met
H	L	L	L	P Incr	Br. Cond. Failed
H	H	H	X	Stack	Direct Jump/Pop
H	H	L	H	Stack	Br. Cond. Met/Pop
H	H	L	L	P Incr	Br. Cond. Failed

* C = C0 + C1 + C2

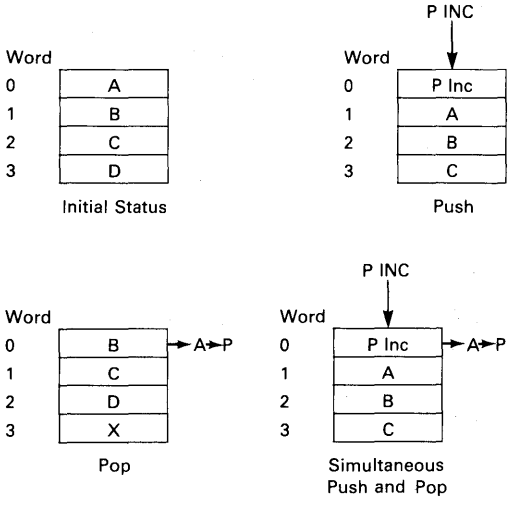
Branch Selection Inputs — S0 and S1

These two inputs are decoded to select a source for the next P Register address. The selection may be modified for conditional branch instructions as shown in Table 6. S0 and S1 also control stack operation as shown in Table 8. These bits are normally driven by microcode memory.

Stack Push Input — Push

When pushed, the incremented P count is written into the top of the stack and all previous stack contents are pushed down by one. There is no check for overflow on a stack push or underflow on stack pop. Simultaneous stack push and pop results when jumping or branching to the stack (Table 6) and asserting a PUSH command (Table 7). The stack is automatically popped on any stack to P Register transfer except simultaneous push and pop and does not require external control. Figure 3 illustrates the various stack operations. Note the simultaneous push/pop saves the previous stack top even though the system jumped to that address.

FIGURE 3 — MC10904 Stack Operation



Tables 7 and 8 define stack push and pop operation. Push is normally driven from microcode memory.

TABLE 7 — STACK PUSH OPERATION

$\overline{CNB}$	C	Push	Stack Push	Instruction
X	X	L	No	No Stack Push
L	H	H	Yes	Push On Cond. Met
H	X	H	Yes	Push Always
L	L	H	No	Push On Cond. Failed

TABLE 8 — STACK POP OPERATION

S1	S0	$\overline{CNB}$	C	Push	Stack Pop	Instruction
L	L	X	X	X	No	Increment P
L	H	X	X	X	No	Select D Bus
H	L	X	X	X	No	Select R Register
H	H	H	X	L	Yes	Jump to Stack
H	H	L	H	L	Yes	Branch to Stack Cond. Met
H	H	L	L	X	No	Branch to Stack Cond. Fail
H	H	H	X	H	No	Simultaneous Push Pop
H	H	L	H	H	No	Simultaneous Push Pop

Condition A Inputs — CA0, CA1, CA2, CA3, S6 and S7

One of four external test conditions CA0–CA3 can be selected by S6 and S7 to an internal node, CA. (See Figure 1.) CA test selection is defined in Table 9.

TABLE 9 — CA CONDITION TEST POINT SELECTION

S6	S7	CA Test Point
L	L	CA0
H	L	CA1
L	H	CA2
H	H	CA3

Condition B Inputs — CB0, CB1, and S8

One of two external test conditions CB0 or CB1 can be selected by S8 to an internal node, CB. CB test selection is defined in Table 10.

TABLE 10 — CB CONDITION TEST POINT SELECTION

S8	CB Test Point
L	CB0
H	CB1

Conditional Branch Combination Logic Select — S2, S3, S4, and S5

S2 through S5 are decoded into 14 different logic selections. (See Table 11.) Final decoded condition selection is presented on the COND output. Table 11 uses CA and CB test points previously defined in tables 9 and 10.

TABLE 11 — CONDITION LOGIC COMBINATION SELECTION

S5	S4	S3	S2	COND
L	L	L	L	L
L	L	L	H	CA
L	L	H	L	CB
L	L	H	H	CA and CB
L	H	L	L	CA or CB
L	H	L	H	CA and $\overline{CB}$
L	H	H	L	CA or $\overline{CB}$
L	H	H	H	L
H	L	L	L	H
H	L	L	H	$\overline{CA}$
H	L	H	L	$\overline{CB}$
H	L	H	H	$\overline{CA}$ or $\overline{CB}$
H	H	L	L	$\overline{CA}$ and $\overline{CB}$
H	H	L	H	$\overline{CA}$ or CB
H	H	H	L	$\overline{CA}$ and CB
H	H	H	H	H

Condition Output — COND

COND output is the result of selecting CA0 through CA3, CB0 or CB1, and logically combining the selections. The COND output of one MC10904 goes to a condition input C0, C1, or C2 of itself and other parallel MC10904 circuits. Three MC10904s would be interconnected by tying COND output of one to all three C0 inputs, COND output of the second to all C1 inputs, and COND output of the third to all C2 inputs.

Increment P Input — $\overline{IP}$

The increment P register input is normally used to provide micro-code addressing at system start up when it is required to load read/write RAM microprogram storage. $\overline{IP}$ overrides all input controls except F0 through F3 inputs and Reset, causing the MC10904 to function in an Increment P Register mode only. A second $\overline{IP}$ function could be to halt system operation by forcing $\overline{IP}$ low and disabling the incrementer with $\overline{IA}$ and $\overline{IB}$ inputs. $\overline{IP}$ operation is shown in Table 12.

TABLE 12 — $\overline{IP}$ FORCED INCREMENT CONTROL

$\overline{IP}$	P Register Operation
L	Increment P
H	Normal

Note that if $\overline{IP}$ is held low and the clock input (CLK) continues running and both $\overline{IA}$ and $\overline{IB}$ are low then the MC10904 will increment the P counter at the clock rate. To load a microcode memory from a slow data source either clock must be slowed or, $\overline{IA}$ or $\overline{IB}$ held high while accessing a new data word.

Reset — RST

Reset overrides all other inputs including $\overline{IP}$ and forces the P Register to all logic low outputs (positive logic 0). Reset is a clocked function and operates on the positive going clock edge. Even though P Register is reset, F0 through F3 inputs can override the four least significant P outputs. Reset would be commonly used at system start up, after loading micro-code, to locate a predefined starting address. Reset also zeros the E counter and sets the microprogram stack to the first location. Reset is normally at a low logic level (L) and is taken high for reset.

Clock — CLK

All registers and counters are activated on a positive going (LOW to HIGH) clock edge.

APPLICATIONS INFORMATION

Two MC10904 circuits, interconnected as shown in Figure 4, generate up to 16-bit micro-code addresses. The right side MC10904 handles the 8 least significant bits and the left side up to 8 most significant bits. Not using all 8 most significant bits adapts the circuit to microprogram memory size.

Parallel address paths DA and DB go to both circuits with least significant address bits going to the right side MC10904. DA and DB inputs normally require the same number of bits as P micro-code address outputs. Control signals are divided into three groups as shown in Figure 4. Common controls go to the same input on both circuits. Common controls handle data transfers and subroutine stack operations, thus insuring both parts perform the same next address function. Each MC10904 also requires separate control inputs, primarily for selecting branch decision test points.

Separate controls on the least significant MC10904 operate the E Counter through $\overline{ELD}$ and $\overline{EEN}$ inputs. The E Counter is limited to 8 bits since there is no provision for carry between circuits. Z output from the E Counter is routed to any CA or CB input on either part (CA0 on the right side MC10904 in the Figure 4 example). The figure only shows multi-way branch F inputs on the least significant stage providing branches to 16 consecutive addresses. Page branches may also be possible with F inputs on the left side MC10904.

The P incrementer is interconnected by tying $\overline{IO}$ of the first circuit to $\overline{IB}$ of the second. Common control $\overline{IA}$ provides for overriding the incrementer, if desired. COND output of the first MC10904 connects to both C0 inputs and the second stage COND to both C1 inputs. This insures both circuits test the same branch condition regardless of CA inputs, CB inputs, or S2 through S8 selections.

Tables 1 through 12 provide for a wide range of next address sequence instructions and various address input sources. Table 13 illustrates input selections for common next address examples. Other variations are possible and may be selected to better fit program flow requirements.

The C column in Table 13 is the logic OR of C0, C1, and C2 as described in Table 5. This is the test point for all conditional branch decisions. Most of the instructions are self explanatory and source selections between DA, DB, and R Register are more for programming example than system architecture. Instruction 9 loads the E Counter to set up a repeat instruction sequence. The repeat is shown in instruction 10 where the microprogram would continue executing the command defined by the R Register address until E Counter equals zero. Selecting $\overline{Z}$ for the test condition is easily accomplished with condition combinational logic (Table 11). Repeating a given subroutine could be accomplished with the following commands: 1) Set E Counter, 2) Jump to Subroutine, 3) Decrement the E Counter once during the subroutine, and 4) Return on Condition from Subroutine. Failure to return would cause a jump to subroutine start.

TABLE 13 — MC10904 SEQUENCE INSTRUCTION EXAMPLES

	SD	$\overline{RLD}$	$\overline{ELD}$	$\overline{EEN}$	S1	S0	$\overline{CNB}$	PUSH	C	INSTRUCTION
1	X	H	H	H	L	L	X	L	X	INCREMENT
2	H	H	H	H	L	H	H	L	X	JUMP TO DB BUS
3	L	L	H	H	L	H	H	L	X	JUMP TO DA BUS, DB BUS TO R REG
4	X	H	H	H	H	L	L	L	C	CONDITIONAL BRANCH TO R REG
5	L	H	H	H	L	H	H	H	X	JUMP TO SUBROUTINE AT DA BUS
6	X	H	H	H	H	H	H	L	X	RETURN FROM SUBROUTINE
7	H	H	H	H	L	H	L	H	C	COND. BRANCH TO SUBROUTINE AT DB
8	X	H	H	H	H	H	L	L	C	COND. RETURN FROM SUBROUTINE
9	L	H	L	H	L	L	X	L	X	INCREMENT, DA TO E COUNTER
10	X	H	H	L	H	L	L	L	$\overline{Z}$	JUMP TO R UNTIL E COUNT = ZERO

FIGURE 4 — 16 BIT MICRO-CODE SEQUENCER EXAMPLE

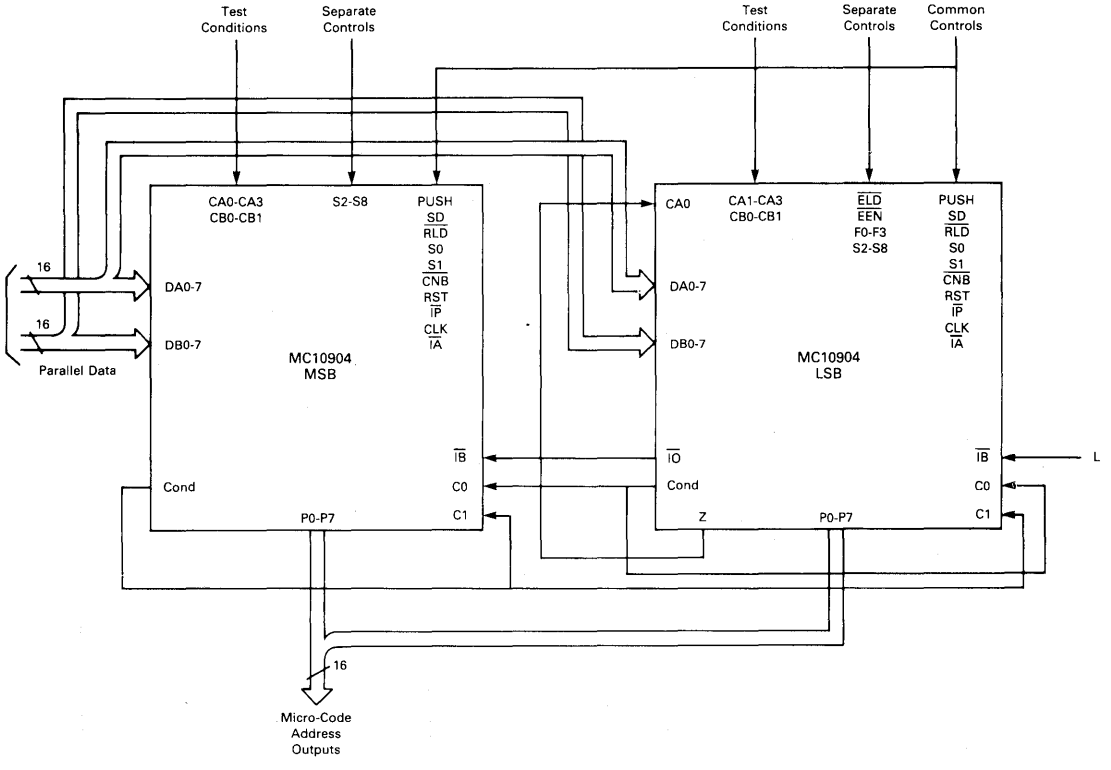


TABLE 14 — RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value	Unit
Supply Voltage (V_{CC} = 0 Volts)	V_{EE}	−4.68 to −5.72	Vdc
Operating Temperature (Functional)	T_A	0 to +70	°C
Output Drive	—	50 Ω to −2.0 Vdc	—
Junction Temperature	T_J	130 max	°C

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table (Table 15), after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 1000 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown for only one input, or for one set of input conditions. Other inputs tested in the same manner.

TABLE 15 — ELECTRICAL CHARACTERISTICS

@ Test Temperature	Test Voltage Values (Volts) V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
0°C	−0.840	−1.95	−1.145	−1.490	−5.2
+25°C	−0.810	−1.95	−1.105	−1.475	−5.2
−70°C	−0.720	−1.95	−1.045	−1.450	−5.2

Characteristics	Symbol	Pin Under Test	MC10904 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Typ	+25°C Max	+70°C Min	+70°C Max	Unit	Voltage Applied to Pins Listed Below V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	(V_{CCO}) (V_{CC}) Gnd
Power Supply Drain Current —	I_{EE}	9, 43	514	855	514	685	855	514	855	mAdc	—	—	—	—	9, 43	3, 15, 20 26, 60, 66
Input Current CLK	I_{inH}	50	—	600	—	—	600	—	600	µAdc	50	—	—	—		
All Others	I_{inL}	49	—	250	—	—	250	—	250		49	—	—	—		
All except NOTE below	I_{inL}	49	0.5	—	0.5	—	—	0.5	—		—	49	—	—		
Logic High Output Voltage	V_{OH}	14	−1.000	−0.840	−0.960	—	−0.810	−0.905	−0.730	Vdc	51	36, 39, 40				
Logic Low Output Voltage	V_{OL}	14	−1.95	−1.665	−1.95	—	−1.650	−1.95	−1.625	Vdc	36, 39, 40	51	—	—		
Logic High Threshold Voltage	V_{OHA}	14	−1.02	—	−0.980	—	—	−0.925	—	Vdc		36, 39, 40	51	—		
Logic Low Threshold Voltage	V_{OLA}	14	—	−1.645	—	—	−1.630	—	−1.605	Vdc	36, 39, 40		—	51		

NOTE: All inputs except pins 1, 2, 17, 18, 19, 67, and 68 have input pulldown resistors (~68 kΩ) between the input and V_{EE}. These 7 inputs, if unused, must be tied to V_{OL} or V_{TT}.

Switching Characteristics Over Operating Voltage and Temperature Range

Tables 16 and 17 define timing characteristics of the MC10904 over operating voltage and temperature ranges. Worst-case Setup and Hold and Propagation Delays are *calculated* for V_{EE} = −5.2 volts ± 10% and a $T_J$max = 115°C. The maximum recommended operating junction temperature is +130°C.

Calculated limits are based on several performance factors as described in Motorola's Preliminary Design Manual for the MECL 10,000 Macrocell Array. Factors include worst case delays due to Macro selections, Fan-Out, Metal Lengths, Wire-OR, and Input Follower options. AC measurements are performed on each device to assure process integrity; however, Motorola does not guarantee limits at this time.

TABLE 16 — SETUP AND HOLD TIMES (NANOSECONDS)
0° to 70°C T_A (T_J not to exceed +115°C)

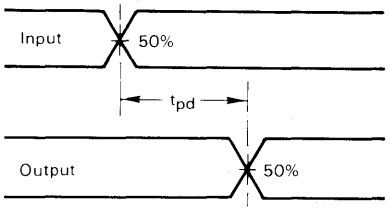
From	To	Setup (Min)	Hold (Min)
DA BUS, DB BUS	CLOCK	1.0	9.0
PUSH, SD, $\overline{RLD}$, $\overline{ELD}$, $\overline{EEN}$	CLOCK	4.0	7.0
$\overline{IA}$, $\overline{IB}$	CLOCK	4.6	2.0
S0, S1, $\overline{CNB}$	CLOCK	2.0	8.0
C0, C1, C2	CLOCK	2.0	8.0
$\overline{IP}$, $\overline{RST}$	CLOCK	2.5	8.0

TABLE 17 — PROPAGATION DELAY (NANOSECONDS)
0° to 70° T_A (T_J not to exceed +115°C)

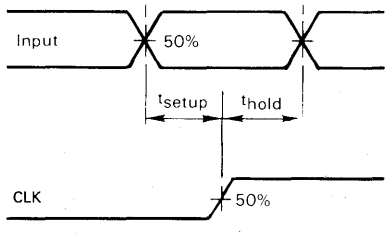
Input	Output	Typ	Max
CLOCK	P4-P7	9.1	14.0
CLOCK	P0-P3	9.1	14.0
CLOCK	$\overline{IO}$	11.1	17.0
CLOCK	Z	15.7	24.0
F0-F3	P0-P3	2.9	4.5
S2-S5	COND	6.5	10.0
S6-S8	COND	7.2	11.0
CA0-3, CB0-1	COND	6.9	10.5

FIGURE 5 — SWITCHING WAVEFORMS

Propagation Delays



Setup and Hold



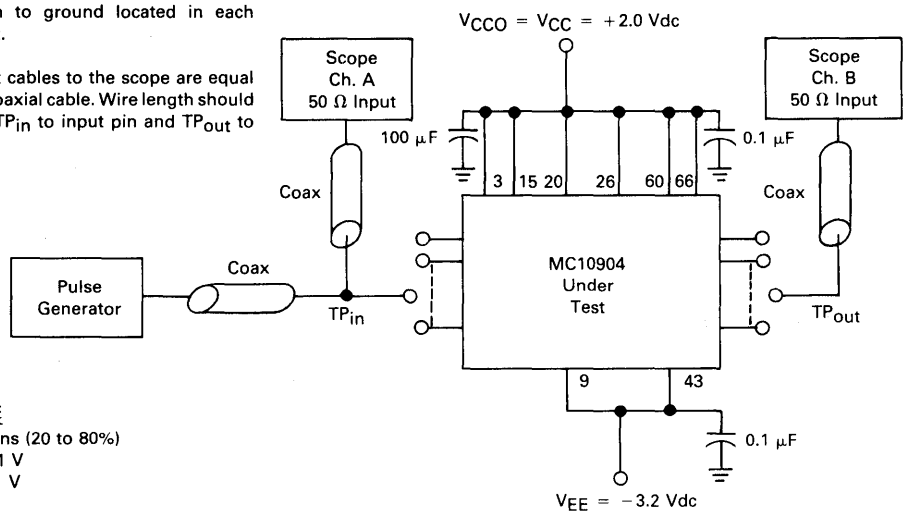
TEST PROCEDURE:
a) Establish setup time with long t_{hold}.
b) Keeping the leading edge of the input constant (t_{setup}) vary the trailing edge of the input to determine t_{hold}.

6

FIGURE 6 — SWITCHING TIME TEST CIRCUIT

50-ohm termination to ground located in each scope channel input.

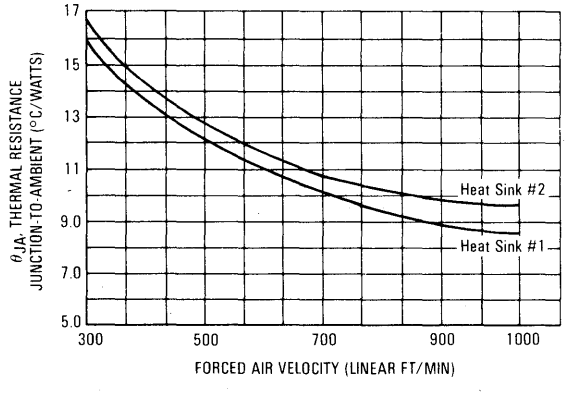
All input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be <1/4 inch from TP_{in} to input pin and TP_{out} to output pin.



INPUT PULSE

$t_r = t_f = 1.0$ ns (20 to 80%)
$V_{OH} = +1.11$ V
$V_{OL} = +0.31$ V

FIGURE 7 — THERMAL CHARACTERISTICS (TYPICAL)



Heat Sink #1 is from THERMALLOY #15832-1, 3 Horizontal Fins, 0.563 inches square. Model No. 2284C.
Heat Sink #2 is from WAKEFIELD #4493, Vertical Fins, 0.5 inches square.
NOTE: $T_J = (\theta_{JA})(P_D) + T_A$ WHERE T_J is the Junction Temperature, T_A is the Ambient Temperature,
$P_D = (I_{EE})(V_{EE}) + (15$ mW) (number of 50 Ω outputs).

6

MOTOROLA

MC10905

Advance Information

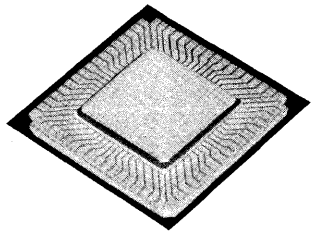
MECL-LSI

16-BIT EXPANDABLE ERROR DETECTION AND CORRECTION UNIT

16-BIT EXPANDABLE ERROR DETECTION AND CORRECTION UNIT

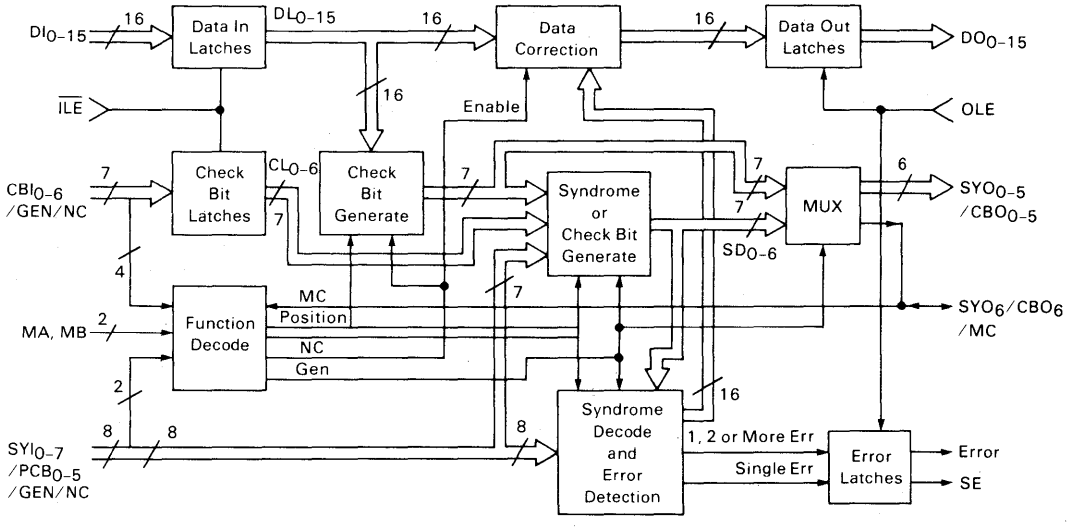
The MC10905 is a high speed 16-bit error detection and correction unit that is easily expandable to handle up to 96 data bits. The unit is designed to improve the reliability of memory systems by detecting and correcting any single bit error while detecting all double bit errors and some multiple bit errors. A high speed pipelined architecture is an important feature providing separate input and output data ports which improves the performance and simplifies the system design.

- High Speed Pipelined Architecture.
- On-Chip Latches for Input Data, Check Bits, Output Data, and Error Flags.
- Separate Input and Output Data Ports.
- Expandable to 96 Bits.
- Full Single Error Correction and Double Error Detection.
- During a Read or Check Mode, Data Correction Can Be Disabled While Checking for Errors.
- Very Fast Error Detect
  - For 16 Bits, 17.2 ns Max.
  - For 32 Bits, 21 ns Max.
  - For 48 through 96 Bits, 28.2 ns Max.
- Very Fast Data Correct
  - For 16 Bits, 19.7 ns Max.
  - For 32 Bits, 28 ns Max.
  - For 48 through 96 Bits, 31.3 ns Max.
- Very Fast Check Bit Generate
  - For 16 Bits, 10.7 ns Max.
  - For 32 Bits, 17 ns Max.
  - For 48 through 96 Bits, 17.8 ns Max.



CASE 745
68 Pin, JEDEC Std.
Leadless Package

BLOCK DIAGRAM — FIGURE 1

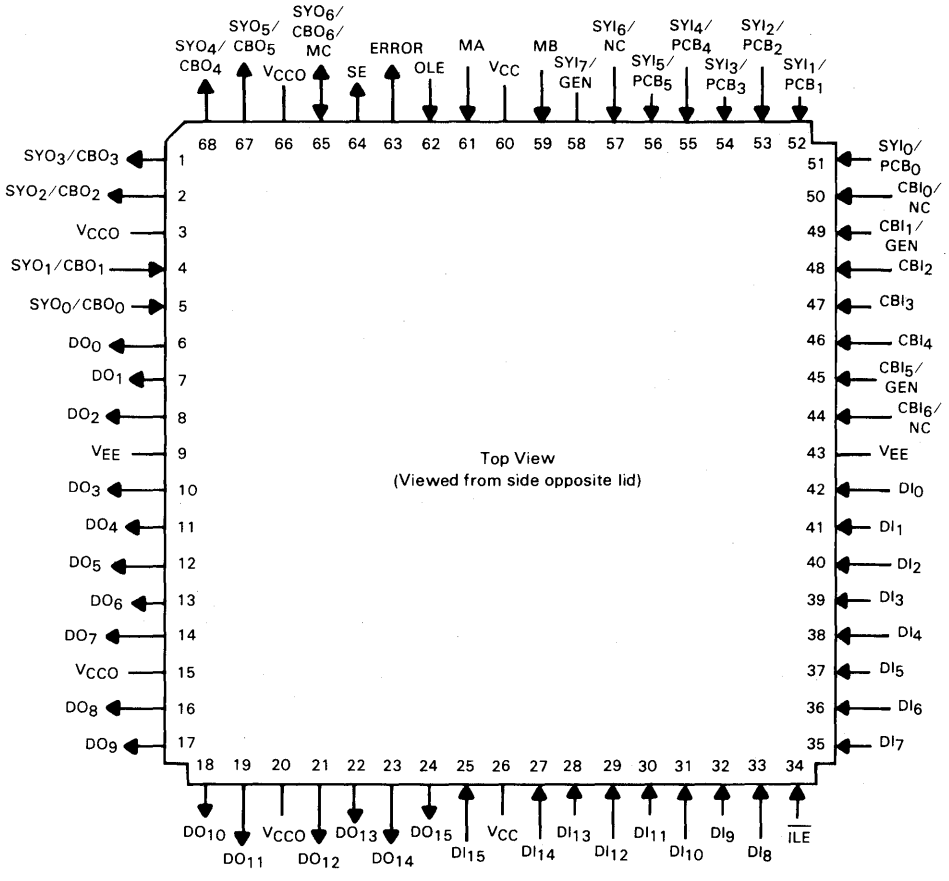


6

Pin Assignments and Definitions (See Figure 2.)

Pin Name	Number	Definition and Description
DI_{0-15}	42-35, 33-27, 25	DATA IN, bits 0 through 15: These 16 data inputs are connected to a data input latch which is then used in error detection and/or correction, and for generating check bits.
CBI_0/NC CBI_1/GEN CBI_2 CBI_3 CBI_4 CBI_5/GEN CBI_6/NC	50 49 48 47 46 45 44	CHECK BITS IN/NO CORRECTION/GENERATE: These input pins can serve one of three functions depending on the selected slice position as described in Table 2. As an example, for slice position 32B, these input pins are all used to input the check bits. For slice position 64A/32A, the first five pins are "don't cares" while pin 45 is GENERATE. Pin 44 is NO CORRECTION. The Check Bits are connected to an input latch which is then used to help generate the syndrome bits used in error detection. (See Table 4). The GENERATE pin when a HIGH selects the generate check bit mode and when a LOW selects the read mode for error checking and/or correction of the input data and check bits. The NO CORRECTION pin, when HIGH during the read mode (GEN = L), disables the data correction while continuing to check for errors. When the pin is LOW during the read mode, the data correction circuitry is enabled. If the NO CORRECTION pin is HIGH when the GENERATE pin is HIGH, the diagnostic write mode is selected. This can be used to check the error detection and correction circuitry of the MC10905.
V_{EE}	9, 43	-5.2 Volt Supply
V_{CC}	26, 60	Ground for Internal Logic
V_{CCO}	3, 15, 20, 66	Ground for Output Drivers
SYI_0/PCB_0 SYI_1/PCB_1 SYI_2/PCB_2 SYI_3/PCB_3 SYI_4/PCB_4 SYI_5/PCB_5 SYI_6/NC SYI_7/GEN	51 52 53 54 55 56 57 58	SYNDROME IN, bits 0-7/PARTIAL CHECK bits 0-5/NO CORRECTION/GENERATE: These input pins perform more than one function depending on the selected slice position (as described in Table 2). The SYI_{0-7} pins are used to input the syndrome bits (for slice positions 64D, 64B/C, and 64A/32A) for decoding the error status and correcting the single data bit errors. (See Tables 6c, d, and e.) The PCB_{0-5} pins are used in the 32-bit data configuration by slice 32B in order to generate the complete check bit and syndrome bit information (See Table 4 and Figure 4.) In the 16-bit slice position, pins 51-56 are don't care conditions. Pin 57 is NC and pin 58 is the GEN signal for slice positions 16 and 32B. The NC and GEN signal definitions are described above.
MA MB SYO_6/CBO_6/MC	61 59 65	SLICE POSITION MODE SELECT: These pins are used to select the slice position as shown in Table 1. Pin 65 is a bidirectional pin that is used as an input (when MA = H and MB = L) for selecting between slice position 16 or 64A/32A. Pin 65 is an output (syndrome or check bit output, bit 6) for slice position 64D, 64 B/C, and 32B.
SYO_0/CBO_0 SYO_1/CBO_1 SYO_2/CBO_2 SYO_3/CBO_3 SYO_4/CBO_4 SYO_5/CBO_5 SYO_6/CBO_6/MC	5 4 2 1 68 67 65	SYNDROME OUTPUT/CHECK BIT OUTPUT: When GEN = L, the syndrome output appears at these pins, and when GEN = H, the generated check bits appear. The truth table for these outputs is shown in Table 4. Note that pin 65 is used as a slice position input (MC) when MA = H and MB = L.
DO_{0-15}	6-8, 10-14, 16-19, 21-24	DATA OUT, bits 0 through 15: These 16 data outputs come from a data out latch. The inputs to the data out latch are the contents of the data input latch as modified by the data correction network. The truth table for DO_{0-15} is shown in Table 5.
ERROR	63	ERROR output: This ERROR flag is the output of a latch. The input to the latch comes from the error detection circuitry. When in the read mode (GEN = L), the ERROR Line is LOW if no errors are detected and it is HIGH if one or more errors are detected.
SE	64	SINGLE ERROR: The SINGLE ERROR flag is the output of a latch with the input of the latch coming from the error detection circuitry. When in the read mode (GEN = L), the SINGLE ERROR output is HIGH if an error has occurred that can be corrected, and the output is low if no error has been detected or if two or more errors are detected. The truth tables for the error outputs are shown in Tables 5 and 6.
$\overline{ILE}$	34	INPUT LATCH ENABLE: This input is used to latch the data at the DI and CBI input pins. When the input is LOW, the latches are enabled with the data at the latch output following the input. When the input is high, the data is latched in the previous state.
OLE	62	OUTPUT LATCH ENABLE: This input is used to control the output latches for DO_{0-15}, SE, and ERROR. When the input is HIGH, the latches are enabled, and if the input is LOW, the information is latched in the previous state. OLE and $\overline{ILE}$ can be tied together for pipelining the data flow.

FIGURE 2 — INPUT/OUTPUT DIAGRAM



ARCHITECTURAL DESCRIPTION

The M10900 family is a line of high performance standard digital LSI products designed around the MECL Macrocell Array. The MC10905 provides an error detection and correction unit (EDCU) between the memory and the CPU that improves system reliability by virtually eliminating system downtime due to memory errors without sacrificing performance. For high speed memory systems it is important that the EDCU be as fast as possible since the delay for detecting errors can add directly to the memory access time.

The dual bus, pipelined architecture (Figure 1) of the MC10905 simplifies system design, reduces the part count, and provides the fastest EDCU on the market. A master-slave data transfer can be accomplished by connecting the latch enables ($\overline{ILE}$ and OLE) together. Error logging can be accomplished by monitoring the syndrome output. Catastrophic memory failures (all 1's or 0's) are also detected. A diagnostic write mode is a special feature which can be used to test the error checking of the MC10905.

In most high performance memory systems, separate MC10905 configurations will be used for writing and reading data to and from memory using separate input and output data buses. Bidirectional data buses slow the performance of high speed memory systems by requiring additional components in the data path such as multiplexors and buffers, and complicating transmission line terminations.

FUNCTIONAL DESCRIPTION

The MC10905 uses a modified Hamming code that allows single error correction with single and double error detection. When writing data to memory, check bits are generated by the MC10905 from selected bits of the data word and stored in memory along with the data word. For a 16-bit wide data word, 6 check bits are required, while 32-bit and 64-bit data words require 7 and 8 check bits respectively. When reading the data from memory, the MC10905 regenerates the check bits and exclusive OR's them with the check bits read from memory producing syndrome bits. If the syndrome bits are all LOW, no errors are detected. If one or more of the syndrome bits are HIGH, an error has been detected. The syndrome bits identify the bit-in-error for single errors, all double errors, and some multiple errors. If a single data bit is in error, the data correction logic inverts this bit (if NC = 0), thus correcting the data word.

SLICE POSITION SELECT — MA, MB, AND MC

The MC10905 can be configured to handle 16-, 32-, 48-, 64-, 76-, 88- and 96-bit data words. Figures 3, 4, 5, and 6 show the different data configurations (48-bit configuration is a subset of the 64-bit configuration). Table 1 shows logic levels that must be applied to the slice position mode inputs (MA, MB, MC) in order to select the chip position for the chosen data configuration. Note that Pin 65 is a bidirectional pin that is used as an input (only when MA = H and MB = L) for selecting between chip positions 16 or 64A/32A. Pin 65 is an output (syndrome or check bit output, bit 6) for chip positions 64D, 64B/C, and 32B.

Some input pins have different signal assignments that are dependent on the selected chip position as shown in Table 2. The GEN (also NC) signal can be 1 of 3 pins depending on the chip position. GEN is pin 45 for slice positions 64D and 64A/32A, pin 58 for positions 16 and 32B, and pin 49 for positions 64B/C. Pins 51–56 are the syndrome bit inputs that are used to decode the error, except for position 32B where these inputs are the partial check bits (PCB_{0-5}) driven by position 32A (Figure 4).

INPUT LATCH ENABLE — $\overline{ILE}$

The Data and Check Bit inputs are connected to latches. A LOW (L) logic level on the $\overline{ILE}$ pin opens the latches allowing data to ripple through. A HIGH (H) level latches the input data and check bits as shown in Table 3.

TABLE 1 — SLICE POSITION SELECTION

Mode Inputs MA Pin 61	MB Pin 59	MC Pin 65	Chip Position
L	L	*	64D — Handles DATA BITS 48–63 in 64-bit configuration
L	H	*	64B/C — Handles DATA BITS 16–31 or 32–47 in 64-bit configuration.
H	L	L	64A/32A — Handles DATA BITS 0–15 in the 64 or 32-bit configuration.
H	L	H	16 — Handles DATA BITS 0–15 in the 16-bit configuration.
H	H	*	32B — Handles DATA BITS 16–31 in the 32-bit configuration.

NOTES:
1. *indicates that Pin 65 is an output (SYO_6/CBO_6) for all slice positions except 64A/32A and 16. The output gate connected to Pin 65 is forced to the "LOW" state when MA = "H" and MB = "L" so that Pin 65 can be used as an input.
2. Inputs requiring a "LOW" state can be left floating (including Pin 65) since an input pull-down resistor (~68 kΩ) is used on all inputs.
3. Chip position 64B/C can also be used to handle data bits 64–75 in a 76-bit data configuration and data bits 76–87 in an 88-bit data configuration. Chip position 64D can also be used to handle data bits 88–95 in a 96-bit configuration.

TABLE 2 — INPUT PIN ASSIGNMENTS AS A FUNCTION OF SLICE POSITION

Slice Position (See Table 1)	Pin Name and Pin Number CBI_0/NC 50	CBI_1/GEN 49	CBI_2 48	CBI_3 47	CBI_4 46	CBI_5/GEN 45	CBI_6/NC 44	SYI_{0-5}/PCB_{0-5} 51-56	SYI_6/NC 57	SYI_7/GEN 58
64D	CBI_0	CBI_1	CBI_2	CBI_3	CBI_4	GEN	NC	SYI_{0-5}	SYI_6	SYI_7
64B/C	NC	GEN	X	X	X	CBI_5	CBI_6	SYI_{0-5}	SYI_6	SYI_7
64A/32A	X	X	X	X	X	GEN	NC	SYI_{0-5}	SYI_6	SYI_7
16	CBI_0	CBI_1	CBI_2	CBI_3	CBI_4	CBI_5	X	X	NC	GEN
32B	CBI_0	CBI_1	CBI_2	CBI_3	CBI_4	CBI_5	CBI_6	PCB_{0-5}	NC	GEN

NOTES:
1. "X" is a don't care condition, Input is not used.
2. For position 32A, Pin 58 must be left open or connected to a V_{OL} voltage.
3. In the generate check-bit mode (GEN = H), the SYI_j inputs are not used for slice positions 64D, 64B/C and 64A/32A. The CBI_j inputs are also not used; however, the input check-bit latches are functional.

TABLE 3 — TRUTH TABLE FOR INTERNAL DATA IN AND CHECK BIT LATCHES

$\overline{ILE}$ (Pin 34)	Internal Latch Outputs DL_{0-15}	CL_{0-6}
L	DI_{0-15}	CBI_{0-6}
H	—	—

NOTES:
1. — denotes NO CHANGE. Outputs are latched.
2. Latches are enabled when $\overline{ILE}$ = "L".

TABLE 4 — SYNDROME OR CHECK BIT OUTPUT AS A FUNCTION OF THE SLICE POSITION AND OPERATING MODE

Operating Mode	Inputs (See Table 2) GEN	NC	(See Table 1) Slice Positions	Syndrome or Check Bit Outputs (Pin 5) SYO_0/CBO_0	(Pin 4) SYO_1/CBO_1	(Pin 2) SYO_2/CBO_2	(Pin 1) SYO_3/CBO_3	(Pin 68) SYO_4/CBO_4	(Pin 67) SYO_5/CBO_5	(Pin 65) SYO_6/CBO_6
Write Mode	H	L	64D	P0	P1	P2	P3	P4	P5A	P6
Generate			64B/C	P0	P1	P2	P3	P4	P5B	P6
Check Bits			64A/32A	P0	$\overline{P1}$	$\overline{P2}$	P3	P4	P5A	L
			16	P0	$\overline{P1}$	$\overline{P2}$	P3	P4	P5A	*
			32B	P0 ⊕ PCB_0	P1 ⊕ PCB_1	P2 ⊕ PCB_2	P3 ⊕ PCB_3	P4 ⊕ PCB_4	P5B ⊕ PCB_5	P6
Diagnostic	H	H	64D	L	L	L	L	L	L	L
Write Mode Initialize Check Bits			64B/C, 64A/32A, 16, 32B	L	H	H	L	L	L	L
Read Mode	L	X	64D	P0 ⊕ CL_0	P1 ⊕ CL_1	P2 ⊕ CL_2	P3 ⊕ CL_3	P4 ⊕ CL_4	P5A	P6
Check Data			64B/C	P0	P1	P2	P3	P4	P5B ⊕ CL_5	P6 ⊕ CL6
and Check Bits			64A/32A	P0	$\overline{P1}$	$\overline{P2}$	P3	P4	P5A	L
and Generate			16	P0 ⊕ CL_0	$\overline{P1}$ ⊕ CL_1	$\overline{P2}$ ⊕ CL_2	P3 ⊕ CL_3	P4 ⊕ CL_4	P5A ⊕ CL_5	*
Syndrome Bits			32B	P0 ⊕ PCB_0 ⊕ CL_0	P1 ⊕ PCB_1 ⊕ CL_1	P2 ⊕ PCB_2 ⊕ CL_2	P3 ⊕ PCB_3 ⊕ CL_3	P4 ⊕ PCB_4 ⊕ CL_4	P5B ⊕ PCB_5 ⊕ CL_5	P6 ⊕ CL_6

NOTES:
1. $PO = DL_0 \oplus DL_1 \oplus DL_2 \oplus DL_4 \oplus DL_6 \oplus DL_8 \oplus DL_{10} \oplus DL_{12}$
   $P1 = DL_0 \oplus DL_1 \oplus DL_3 \oplus DL_5 \oplus DL_7 \oplus DL_9 \oplus DL_{11} \oplus DL_{13}$
   $P2 = DL_0 \oplus DL_2 \oplus DL_3 \oplus DL_4 \oplus DL_5 \oplus DL_8 \oplus DL_9 \oplus DL_{14}$
   $P3 = DL_1 \oplus DL_2 \oplus DL_3 \oplus DL_6 \oplus DL_7 \oplus DL_{10} \oplus DL_{11} \oplus DL_{15}$
   $P4 = DL_4 \oplus DL_5 \oplus DL_6 \oplus DL_7 \oplus DL_{12} \oplus DL_{13} \oplus DL_{14} \oplus DL_{15}$
   $P5A = DL_8 \oplus DL_9 \oplus DL_{10} \oplus DL_{11} \oplus DL_{12} \oplus DL_{13} \oplus DL_{14} \oplus DL_{15}$
   $P5B = DL_0 \oplus DL_1 \oplus DL_2 \oplus DL_3 \oplus DL_4 \oplus DL_5 \oplus DL_6 \oplus DL_7$
   $P6 = P5A \oplus P5B$
   where DL_i is the output of bit i of the DATA IN LATCH.
2. CL_i is the output of bit i of the CHECK BIT LATCH.
3. PCB_{0-5} are the partial check bit inputs (pins 51-56) for slice position 32B (See Table 2 and Figure 4).
4. * indicates that for slice position 16, pin 65 is a slice position mode input (MC) that must be externally connected to an "H" or V_{OH} voltage level (see Table 1).

FIGURE 3 — 16-BIT DATA CONFIGURATION

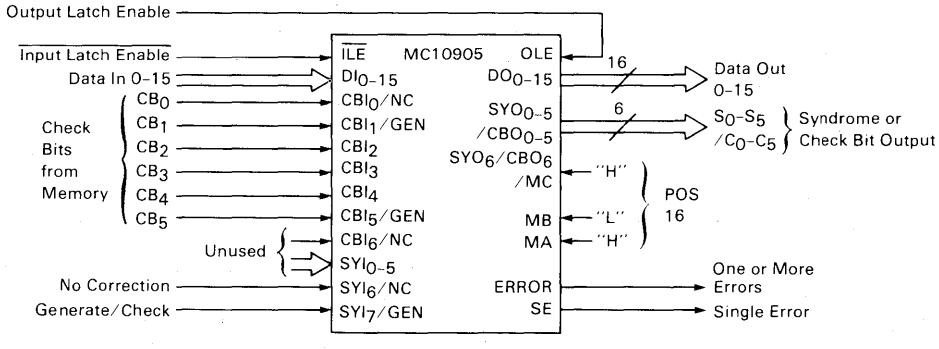
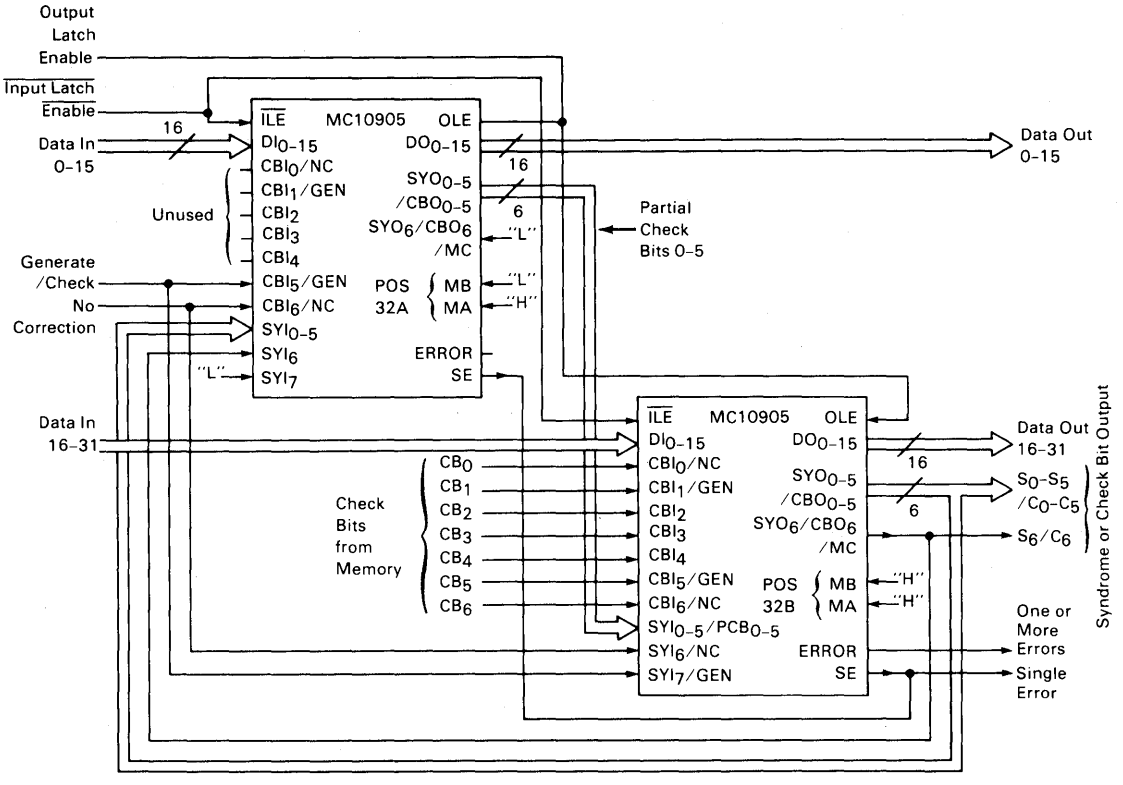


FIGURE 4 — 32-BIT DATA CONFIGURATION



OPERATING MODES — GEN, NC

Four different operating modes can be selected with the GEN and NC inputs which are described in Table 7. Also, tables 4 and 5 show truth tables using the GEN and NC inputs as a function of the slice position.

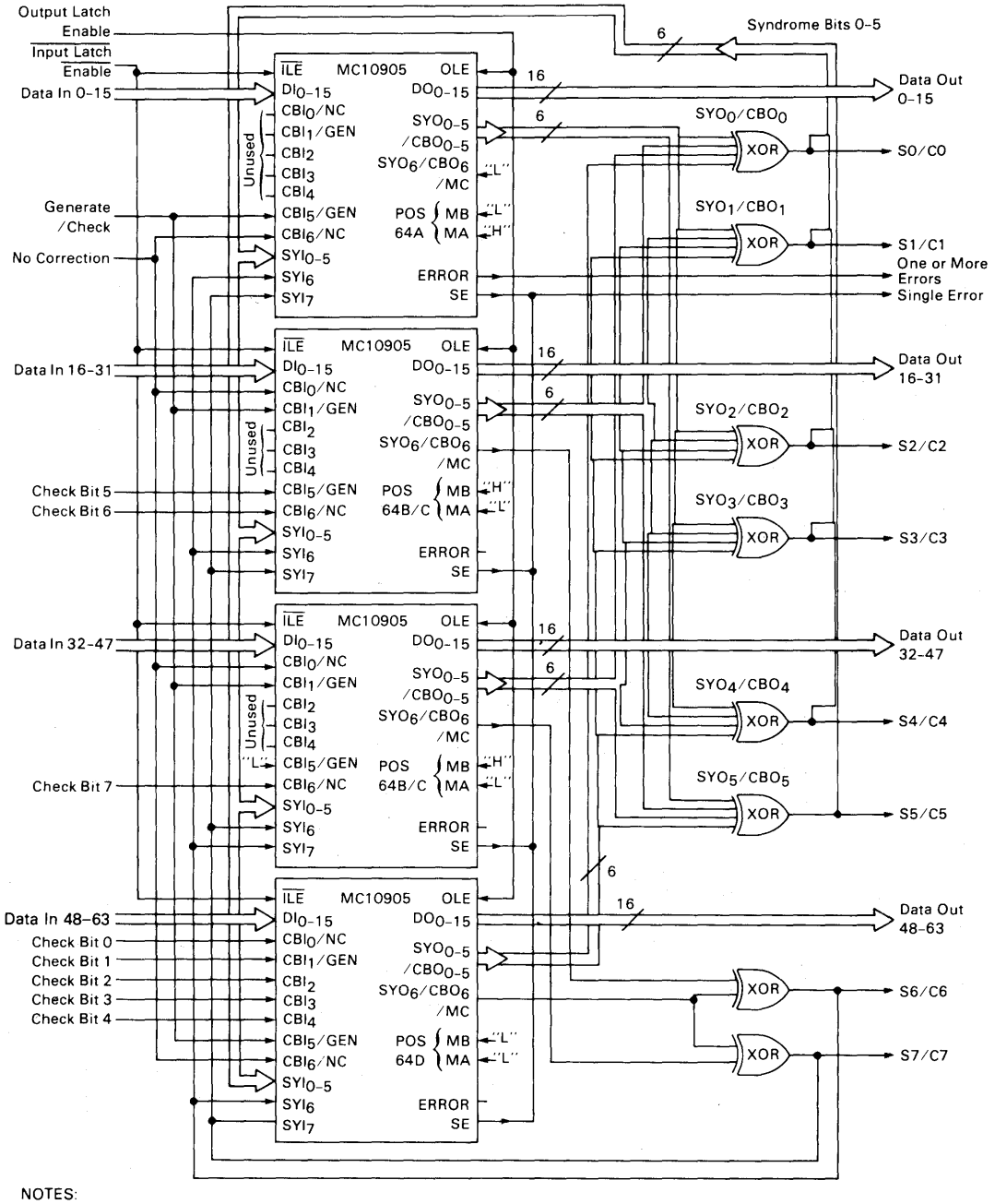
The Read and Correct Mode (GEN = L, NC = L) checks the data and check bits received from memory for errors. If an error occurs, the ERROR flag is activated, and if it is a single bit error, the Single Error flag is also activated and the data is corrected. The syndrome bits are also made available to the designer.

The Read and Check Only Mode (GEN = L, NC = H) also checks the data and check bits from memory for errors. However, if a single bit error occurs, the data is not corrected. With the data correction disabled, the propagation delay from data input to data output is shortened significantly. If the ERROR flag is activated to the CPU, the current cycle could be delayed to correct the data (by making NC = L) if the SE flag is also activated, or a diagnostic routine could be initiated. If a single bit error is detected, the corrected data should be rewritten into the same memory location in order to reduce the chance of getting a double bit error later. A "soft" error that is allowed to remain in memory will increase the probability of getting a double bit error.

The Write Mode (GEN = H, NC = L) generates new check bits from the data word that is to be stored in memory. The generated check bits are stored with the data word in memory. Table 4 shows the equations for generating the check bits. Also, Table 8 shows a chart that defines the check bit generation.

The Diagnostic Write Mode (GEN = H, NC = H) forces the check bit outputs C_0 through C_7 to LHHLLLL (logic output for the all zero-data word) while passing Data-In to the Data-Out pins. In this mode, data patterns are written into memory to cause different types of errors. The MC10905 error detection circuitry can be checked by comparing the data-in and data-out with the syndrome error decode and error flags. Table 9 shows the syndrome bit decoding for the data configurations shown in Figure 3, 4 and 5.

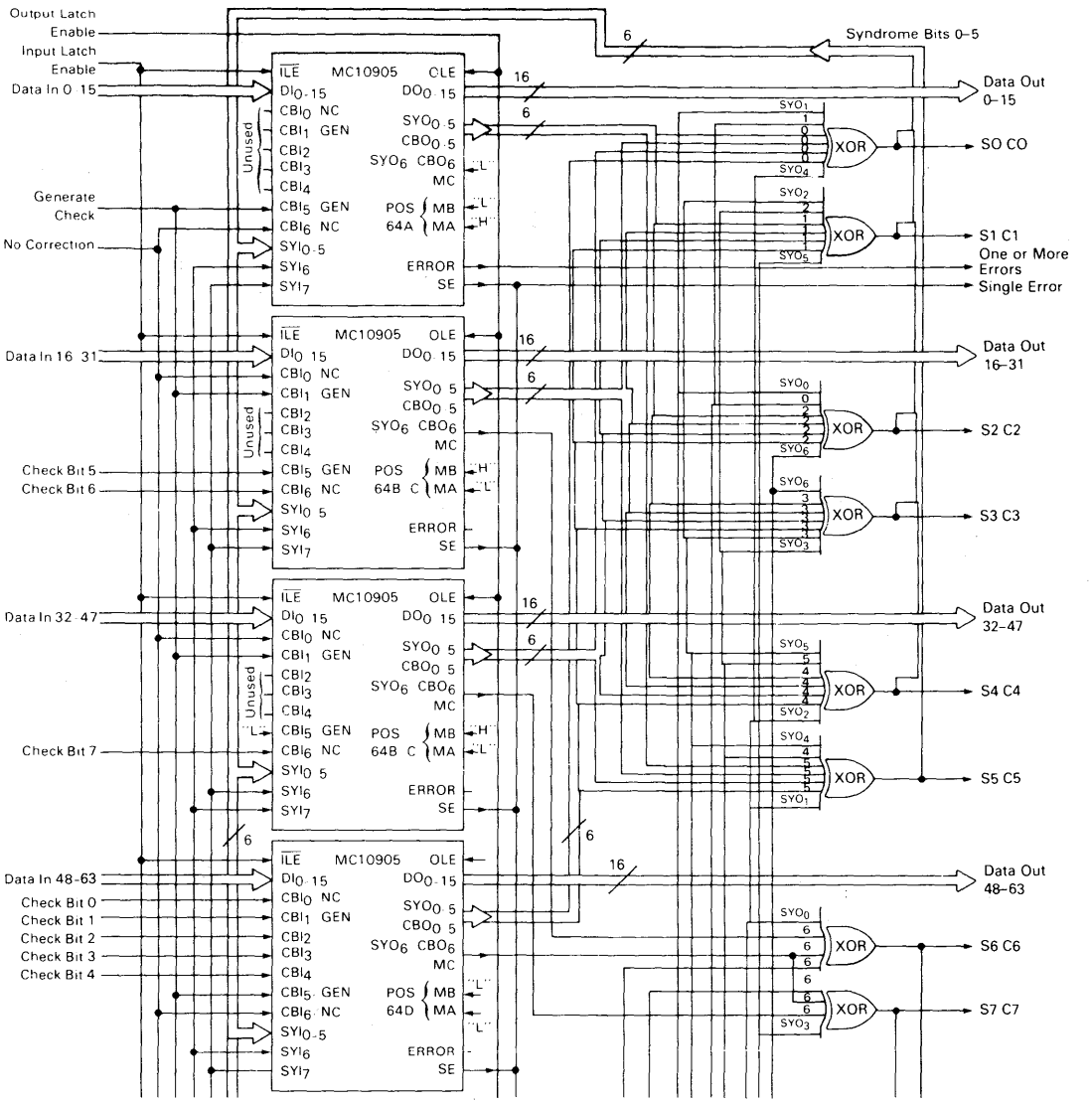
FIGURE 5 — 64-BIT DATA CONFIGURATION



NOTES:

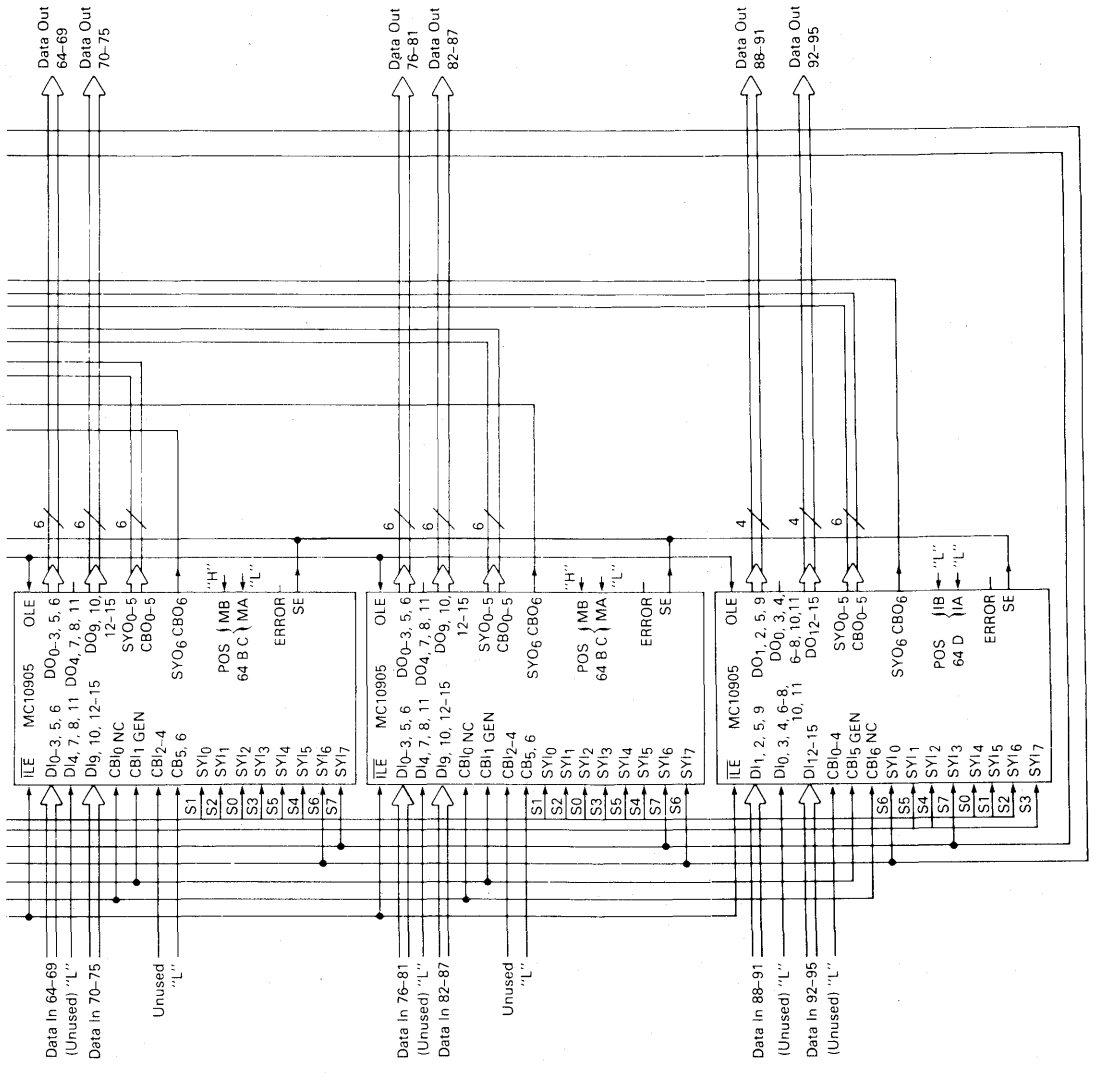
1. For position 64B/C with data bits 32-47, the syndrome output S6 must be connected to the SYI_7 input while the S7 output must be connected to SYI_6.
2. For a 48-bit data configuration, the position 64A is eliminated and the S1 and S2 output gates must be changed from EXCLUSIVE OR to EXCLUSIVE NOR.
3. The ERROR output information is the same on all 4 devices.
4. The SE outputs are connected together (WIRE ORed) to form the SINGLE ERROR output.
5. The MC10163 can be used to provide two 4-input EXCLUSIVE OR gates.

FIGURE 6 — 96-BIT DATA CONFIGURATION



CONTINUED ON NEXT PAGE

FIGURE 6—96-BIT DATA CONFIGURATION (CONTINUED)



NOTES:

1. For a 76-data bit configuration, eliminate the bottom two devices. For an 88-data bit configuration, eliminate the bottom device.
2. The "ERROR" output information is the same on all 7 devices.
3. The "SE" outputs are connected together (wire ORed) to form the "SINGLE ERROR" output.
4. The SYO_{0-6} CBO_{0-6} outputs for the bottom three devices are rotated (see Table 8) to the XOR gates and rotated back into the SYI_{0-7} inputs as labeled.
5. The MC10163 provides two 4-input XOR gates while the MC10H160 provides one 12-input XOR gate.

CONTINUED FROM PREVIOUS PAGE

SYNDROME/CHECK BIT OUTPUTS — SYO_{0-6}/CBO_{0-6}

The logic equations for the syndrome or check bit outputs are shown in Table 4 as a function of the slice position and operating mode. These outputs contain the check bits during write to memory (GEN = H, NC = L). For a real cycle (GEN = L), these outputs contain the syndrome bits used for error identification. Table 8 shows a chart for check bit generation for various data configurations. Note that for data configurations of greater than 32 bits, exclusive OR gates must be used to generate the total syndrome or check bit field as shown in Figures 5 and 6. For the 32-bit data configuration (see Figure 4), the partial check bits generated by one MC10905 (32A) are passed to another MC10905 (32B) for generating the complete syndrome/check bit field without additional hardware.

The code used to generate the check bit patterns is based on the parity of selected data bits. An all LOW syndrome field indicates that no errors have been detected. If an even number of HIGH's occur in the syndrome field, a double error has been detected, while an odd number of HIGH's indicate a single error or multiple error has been detected. Table 9 shows the syndrome bit decoding.

Note that the generated parity (P1 and P2) is inverted on the SYO_1/CBO_1, and SYO_2/CBO_2 outputs for slice positions 16 and 64A/32A. This allows for the detection of catastrophic errors such as all 1's or 0's in the data and check bit field.

OUTPUT LATCH ENABLE — OLE

The internal data and error outputs are connected to latches. A HIGH (H) logic level on the OLE pin opens the latches allowing the information to flow through. A LOW (L) level latches the data and the SE and ERROR outputs as shown in Table 5.

DATA OUTPUT — DO_{0-15}

The unmodified contents of the Data-In latches (DL_{0-15}) are connected to the inputs of the Data-Out latches for all modes except when GEN = L and NC = L (check and correct data mode) as shown in Table 5. If the data is to be corrected (GEN = L and NC = L), the data correction network will invert any single bit error of the Data-In latch before placing it at the input of the Data-Out latch (see Tables 5 and 6).

SINGLE ERROR AND ERROR FLAGS — SE, ERROR

In the write mode (GEN = H), a LOW is forced on the inputs of the error flag latches as shown in Table 5. In the read mode (GEN = L), Table 6 defines the error flags for the various slice positions. The input to the ERROR latch is a LOW only if no errors are detected (data is valid) and it is a HIGH if one or more errors are detected. The input to the Single Error latch is HIGH only if a single bit error has been detected in the Data-In or Check Bit latches.

TABLE 5 — DATA OUT, SE, AND ERROR OUTPUTS AS A FUNCTION OF THE SLICE POSITION AND OPERATING MODE

Operating Mode	INPUTS (See Table 2) OLE	GEN	NC	SYI_{0-7}	(See Note 2) SD_{0-6}	(See Table 1) Slice Position	OUTPUTS DO_{0-15}	SE	ERROR
Output Latched	L	X	X	X	X	X	—	—	—
WRITE Mode	H	H	X	X	X	X	DL_{0-15}	L	L
READ Mode No Data Correction	H	L	H	X	See Table 6a	16	DL_{0-15}	See Table 6a	
				Partial Check Bit Input	See Table 6b	32B	DL_{0-15}	See Table 6b	
				See Table 6c	X	64A/32A	DL_{0-15}	See Table 6c	
				See Table 6d	X	64B/C	DL_{0-15}	See Table 6d	
				See Table 6e	X	64D	DL_{0-15}	See Table 6e	
READ Mode Check and Correct Data	H	L	L	X	See Table 6a	16	See Note 6	See Table 6a	
				Partial Check Bit Input	See Table 6b	32B	See Note 6	See Table 6b	
				See Table 6c	X	64A/32A	See Note 6	See Table 6c	
				See Table 6d	X	64B/C	See Note 6	See Table 6d	
				See Table 6e	X	64D	See Note 6	See Table 6e	

NOTES:
1. X = Input don't care Condition.
2. SD_{0-6} are the internal syndromes which are equal to the syndrome output SYO_{0-6} (see Table 4).
3. Tables 6a-6e describe the outputs in the READ mode as a function of the syndrome bits.
4. — denotes NO CHANGE. Outputs are latched. Outputs are enabled when OLE = "H".
5. DL_{0-15} is the output of the DATA IN latches.
6. If a single data bit error occurs (see tables 6a-6e), the data bit in error will be corrected (by inverting it) while the other 15 bits from DL_{0-15} will appear unchanged at DO_{0-15}.

DATA CONFIGURATIONS

A single MC10905 will handle 16 data bits plus 6 check bits while two MC10905's will handle 32 data bits plus 7 check bits without additional hardware (see Figures 3 and 4). For the 64-bit configuration, four MC10905s are required, plus some additional exclusive OR (XOR) gates as shown in Figure 5. A 48-bit configuration can be generated from Figure 5 by eliminating the MC10905 in position 64A and changing the S1 and S2 output gates from XOR to XNOR (exclusive NOR). The MC10163, MC10107, MC10H107, or MC10H160 can be used to provide the XOR/XNOR functions.

Tables 7, 8 and 9 show the operating modes, the parity tree chart for the check bits, and the syndrome bit decoding, respectively. Table 10 was generated for use in calculating the delays of the important propagation delay paths for multi-chip data configurations. The maximum propagation delays specified in Tables 14 and 15 are used in these calculations.

TABLE 6 — TRUTH TABLES FOR BIT-IN-ERROR, AND THE SE AND ERROR OUTPUTS WHEN IN THE READ OR CHECK MODE (GEN = L)

(a) FOR SLICE POSITION 16

	SD_5	L			H			L			H			L			H			L			H		
	SD_4	L			L			H			H			L			L			H			H		
	SD_3	L			L			L			L			H			H			H			H		
SD_0	SD_1	SD_2	Bit In Error	SE	Error	Bit In Error	SE	Error	Bit In Error	SE	Error	Bit In Error	SE	Error	Bit In Error	SE	Error	Bit In Error	SE	Error	Bit In Error	SE	Error	Bit In Error	SE	Error
L	L	L	*	L	L	CL_5	H	H	CL_4	H	H	—	L	H	CL_3	H	H	—	L	H	—	L	H	DL_{15}	H	H
L	L	H	CL_2	H	H	—	L	H	—	L	H	DL_{14}	H	H	—	L	H	—	L	H	—	L	H	—	L	H
L	H	L	CL_1	H	H	—	L	H	—	L	H	DL_{13}	H	H	—	L	H	DL_{11}	H	H	DL_7	H	H	—	L	H
L	H	H	—	L	H	DL_9	H	H	DL_5	H	H	—	L	H	DL_3	H	H	—	L	H	—	L	H	—	L	H
H	L	L	CL_0	H	H	—	L	H	—	L	H	DL_{12}	H	H	—	L	H	DL_{10}	H	H	DL_6	H	H	—	L	H
H	L	H	—	L	H	DL_8	H	H	DL_4	H	H	—	L	H	DL_2	H	H	—	L	H	—	L	H	—	L	H
H	H	L	—	L	H	—	L	H	—	L	H	—	L	H	DL_1	H	H	—	L	H	—	L	H	—	L	H
H	H	H	DL_0	H	H	—	L	H	—	L	H	—	L	H	—	L	H	—	L	H	—	L	H	—	L	H

NOTES:
1. SD_i is the internal syndrome, bit i, which is equal to the syndrome output bit, SYO_i (see Table 4).
2. — = NO BITS ARE CORRECTED; $DO_{0-15} = DL_{0-15}$
   * = NO ERRORS
3. DL_i = SINGLE BIT ERROR in the DATA-IN LATCH output, bit i. If NC = 0, data bit will be corrected by inverting it.
4. CL_i = SINGLE BIT ERROR in the CHECK BIT LATCH output, bit i.
5. BIT IN ERROR specifies the single bit in error detected by the indicated slice position.
6. Unlisted input SYI combinations in tables 6c, 6d, and 6e perform no data correction, SE = "L", and ERROR = "H".
7. The SE and ERROR output latches (for Table 6) are enabled, OLE = "H".

(b) FOR SLICE POSITION 32b

	SD_6	H			H			H			H			L			L			L			L		
	SD_5	L			L			H			H			L			L			H			H		
	SD_4	L			H			L			H			L			H			L			H		
SD_0	SD_1	SD_2	SD_3	Bit In Error	SE	Error	Bit In Error	SE	Error	Bit In Error	SE	Error	Bit In Error	SE	Error	Bit In Error	SE	Error	Bit In Error	SE	Error	Bit In Error	SE	Error	Bit In Error	SE	Error
L	L	L	L	CL_6	H	H	—	L	H	—	L	H	—	L	H	—	L	H	*	L	L	CL_4	H	H	CL_5	H	H	—	L	H
L	L	L	H	—	L	H	DL_{15}	H	H	—	L	H	—	L	H	CL_3	H	H	—	L	H	—	L	H	—	L	H
L	L	H	L	—	L	H	DL_{14}	H	H	—	L	H	—	L	H	CL_2	H	H	—	L	H	—	L	H	—	L	H
L	L	H	H	—	L	H	—	L	H	—	L	H	—	L	H	—	L	H	—	L	H	—	L	H	—	L	H
L	H	L	L	—	L	H	DL_{13}	H	H	—	L	H	—	L	H	CL_1	H	H	—	L	H	—	L	H	—	L	H
L	H	L	H	DL_{11}	H	H	—	L	H	—	L	H	DL_7	H	H	—	L	H	—	L	H	—	L	H	—	L	H
L	H	H	L	DL_9	H	H	—	L	H	—	L	H	DL_5	H	H	—	L	H	—	L	H	—	L	H	—	L	H
L	H	H	H	—	L	H	—	L	H	DL_3	H	H	—	L	H	—	L	H	—	L	H	—	L	H	—	L	H
H	L	L	L	—	L	H	DL_{12}	H	H	—	L	H	—	L	H	CL_0	H	H	—	L	H	—	L	H	—	L	H
H	L	L	H	DL_{10}	H	H	—	L	H	—	L	H	DL_6	H	H	—	L	H	—	L	H	—	L	H	—	L	H
H	L	H	L	DL_8	H	H	—	L	H	—	L	H	DL_4	H	H	—	L	H	—	L	H	—	L	H	—	L	H
H	L	H	H	—	L	H	—	L	H	DL_2	H	H	—	L	H	—	L	H	—	L	H	—	L	H	—	L	H
H	H	L	L	—	L	H	—	L	H	—	L	H	—	L	H	—	L	H	—	L	H	—	L	H	—	L	H
H	H	L	H	—	L	H	—	L	H	DL_1	H	H	—	L	H	—	L	H	—	L	H	—	L	H	—	L	H
H	H	H	L	—	L	H	—	L	H	DL_0	H	H	—	L	H	—	L	H	—	L	H	—	L	H	—	L	H
H	H	H	H	—	L	H	—	L	H	—	L	H	—	L	H	—	L	H	—	L	H	—	L	H	—	L	H

TABLE 6 — (continued)

(c) FOR SLICE POSITION 64A/32

			SYI_7	L			L			L			L			L			H		
			SYI_6	L			L			L			L			H			L		
			SYI_5	L			L			H			H			L			L		
			SYI_4	L			H			L			H			L			L		
SYI_0	SYI_1	SYI_2	SYI_3	Bit In Error	SE	Error	Bit In Error	SE	Error	Bit In Error	SE	Error	Bit In Error	SE	Error	Bit In Error	SE	Error	Bit In Error	SE	Error	Bit In Error	SE	Error
L	L	L	L	*	L	L	CL_4	H	H	CL_5	H	H	—	L	H	CL_6	H	H	CL_7	H	H
L	L	L	H	CL_3	H	H	—	L	H	—	L	H	DL_{15}	H	H	—	L	H	—	L	H
L	L	H	L	CL_2	H	H	—	L	H	—	L	H	DL_{14}	H	H	—	L	H	—	L	H
L	L	H	H	—	L	H	—	L	H	—	L	H	—	L	H	—	L	H	—	L	H
L	H	L	L	CL_1	H	H	—	L	H	—	L	H	DL_{13}	H	H	—	L	H	—	L	H
L	H	L	H	—	L	H	DL_7	H	H	DL_{11}	H	H	—	L	H	—	L	H	—	L	H
L	H	H	L	—	L	H	DL_5	H	H	DL_9	H	H	—	L	H	—	L	H	—	L	H
L	H	H	H	DL_3	H	H	—	L	H	—	L	H	—	L	H	—	L	H	—	L	H
H	L	L	L	CL_0	H	H	—	L	H	—	L	H	DL_{12}	H	H	—	L	H	—	L	H
H	L	L	H	—	L	H	DL_6	H	H	DL_{10}	H	H	—	L	H	—	L	H	—	L	H
H	L	H	L	—	L	H	DL_4	H	H	DL_8	H	H	—	L	H	—	L	H	—	L	H
H	L	H	H	DL_2	H	H	—	L	H	—	L	H	—	L	H	—	L	H	—	L	H
H	H	L	L	—	L	H	—	L	H	—	L	H	—	L	H	—	L	H	—	L	H
H	H	L	H	DL_1	H	H	—	L	H	—	L	H	—	L	H	—	L	H	—	L	H
H	H	H	L	DL_0	H	H	—	L	H	—	L	H	—	L	H	—	L	H	—	L	H
H	H	H	H	—	L	H	—	L	H	—	L	H	—	L	H	—	L	H	—	L	H

(d) FOR SLICE POSITION 64B/C

			SYI_7	L			L			L			L			L			L			H		
			SYI_6	H			H			H			H			L			L			L		
			SYI_5	L			L			H			H			L			H			L		
			SYI_4	L			H			L			H			L			H			L		
SYI_0	SYI_1	SYI_2	SYI_3	Bit In Error	SE	Error	Bit In Error	SE	Error	Bit In Error	SE	Error	Bit In Error	SE	Error	Bit In Error	SE	Error	Bit In Error	SE	Error	Bit In Error	SE	Error	Bit In Error	SE	Error
L	L	L	L	CL_6	H	H	—	L	H	—	L	H	—	L	H	*	L	L	CL_4	H	H	CL_5	H	H	CL_7	H	H
L	L	L	H	—	L	H	DL_{15}	H	H	—	L	H	—	L	H	CL_3	H	H	—	L	H	—	L	H	—	L	H
L	L	H	L	—	L	H	DL_{14}	H	H	—	L	H	—	L	H	CL_2	H	H	—	L	H	—	L	H	—	L	H
L	L	H	H	—	L	H	—	L	H	—	L	H	—	L	H	—	L	H	—	L	H	—	L	H	—	L	H
L	H	L	L	—	L	H	DL_{13}	H	H	—	L	H	—	L	H	CL_1	H	H	—	L	H	—	L	H	—	L	H
L	H	L	H	DL_{11}	H	H	—	L	H	—	L	H	DL_7	H	H	—	L	H	—	L	H	—	L	H	—	L	H
L	H	H	L	DL_9	H	H	—	L	H	—	L	H	DL_5	H	H	—	L	H	—	L	H	—	L	H	—	L	H
L	H	H	H	—	L	H	—	L	H	DL_3	H	H	—	L	H	—	L	H	—	L	H	—	L	H	—	L	H
H	L	L	L	—	L	H	DL_{12}	H	H	—	L	H	—	L	H	CL_0	H	H	—	L	H	—	L	H	—	L	H
H	L	L	H	DL_{10}	H	H	—	L	H	—	L	H	DL_6	H	H	—	L	H	—	L	H	—	L	H	—	L	H
H	L	H	L	DL_8	H	H	—	L	H	—	L	H	DL_4	H	H	—	L	H	—	L	H	—	L	H	—	L	H
H	L	H	H	—	L	H	—	L	H	DL_2	H	H	—	L	H	—	L	H	—	L	H	—	L	H	—	L	H
H	H	L	L	—	L	H	—	L	H	—	L	H	—	L	H	—	L	H	—	L	H	—	L	H	—	L	H
H	H	L	H	—	L	H	—	L	H	DL_1	H	H	—	L	H	—	L	H	—	L	H	—	L	H	—	L	H
H	H	H	L	—	L	H	—	L	H	DL_0	H	H	—	L	H	—	L	H	—	L	H	—	L	H	—	L	H
H	H	H	H	—	L	H	—	L	H	—	L	H	—	L	H	—	L	H	—	L	H	—	L	H	—	L	H

(e) FOR SLICE POSITION 64D

			SYI_7	H			H			H			H			L			L			L			L			H		
			SYI_6	H			H			H			H			L			L			L			H			L		
			SYI_5	L			L			H			H			L			L			H			L			L		
			SYI_4	L			H			L			H			L			H			L			L			L		
SYI_0	SYI_1	SYI_2	SYI_3	Bit In Error	SE	Error	Bit In Error	SE	Error	Bit In Error	SE	Error	Bit In Error	SE	Error	Bit In Error	SE	Error	Bit In Error	SE	Error	Bit In Error	SE	Error	Bit In Error	SE	Error	Bit In Error	SE	Error
L	L	L	L	–	L	H	–	L	H	–	L	H	–	L	H	*	L	L	CL_4	H	H	CL_5	H	H	CL_6	H	H	CL_7	H	H
L	L	L	H	–	L	H	–	L	H	–	L	H	DL_{15}	H	H	CL_3	H	H	–	L	H	–	L	H	–	L	H	–	L	H
L	L	H	L	–	L	H	–	L	H	–	L	H	DL_{14}	H	H	CL_2	H	H	–	L	H	–	L	H	–	L	H	–	L	H
L	L	H	H	–	L	H	–	L	H	–	L	H	–	L	H	–	L	H	–	L	H	–	L	H	–	L	H	–	L	H
L	H	L	L	–	L	H	–	L	H	–	L	H	DL_{13}	H	H	CL_1	H	H	–	L	H	–	L	H	–	L	H	–	L	H
L	H	L	H	–	L	H	DL_7	H	H	DL_{11}	H	H	–	L	H	–	L	H	–	L	H	–	L	H	–	L	H	–	L	H
L	H	H	L	–	L	H	DL_5	H	H	DL_9	H	H	–	L	H	–	L	H	–	L	H	–	L	H	–	L	H	–	L	H
L	H	H	H	DL_3	H	H	–	L	H	–	L	H	–	L	H	–	L	H	–	L	H	–	L	H	–	L	H	–	L	H
H	L	L	L	–	L	H	–	L	H	–	L	H	DL_{12}	H	H	CL_0	H	H	–	L	H	–	L	H	–	L	H	–	L	H
H	L	L	H	–	L	H	DL_6	H	H	DL_{10}	H	H	–	L	H	–	L	H	–	L	H	–	L	H	–	L	H	–	L	H
H	L	H	L	–	L	H	DL_4	H	H	DL_8	H	H	–	L	H	–	L	H	–	L	H	–	L	H	–	L	H	–	L	H
H	L	H	H	DL_2	H	H	–	L	H	–	L	H	–	L	H	–	L	H	–	L	H	–	L	H	–	L	H	–	L	H
H	H	L	L	–	L	H	–	L	H	–	L	H	–	L	H	–	L	H	–	L	H	–	L	H	–	L	H	–	L	H
H	H	L	H	DL_1	H	H	–	L	H	–	L	H	–	L	H	–	L	H	–	L	H	–	L	H	–	L	H	–	L	H
H	H	H	L	DL_0	H	H	–	L	H	–	L	H	–	L	H	–	L	H	–	L	H	–	L	H	–	L	H	–	L	H
H	H	H	H	–	L	H	–	L	H	–	L	H	–	L	H	–	L	H	–	L	H	–	L	H	–	L	H	–	L	H

TABLE 7 — OPERATING MODE SELECTION FOR 16, 32, 48, AND 64-BIT DATA CONFIGURATIONS

Inputs		
Generate /Check	No Correction	Operating Mode and Description
L	L	READ MODE. Check for errors, generate syndrome bits S0–S7, and correct single data bit errors.
L	H	READ MODE. Check for errors, generate syndrome bits S0–S7, but do not correct single data bit errors.
H	L	WRITE MODE. Generate check bits C0–C7, pass data through, and force inputs to the error latches to the "LOW" state.
H	H	DIAGNOSTIC WRITE MODE. Force the check bits C0 through C7 to a L H H L L L L L respectively, pass data through, and force inputs to the error latches to the "LOW" state.

TABLE 8 — CHECK BIT GENERATION FOR 16, 32, 64, 76, 88 AND 96-BIT DATA CONFIGURATIONS

Check Bits	Parity Operation	Position 16 or 64A/32A — Data In 0–15															Position 32B or 64B/C — Data In 16–31															
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
C_0	XOR	X	X	X	—	X	—	X	—	X	—	X	—	X	—	—	—	X	X	X	—	X	—	X	—	X	—	X	—	X	—	—	—
C_1	XNOR	X	X	—	X	—	X	—	X	—	X	—	X	—	X	—	—	X	X	—	X	—	X	—	X	—	X	—	X	—	X	—	—
C_2	XNOR	X	—	X	X	X	X	—	—	X	X	—	—	—	—	X	—	X	—	X	X	X	X	—	—	X	X	—	—	—	—	X	—
C_3	XOR	—	X	X	X	—	—	X	X	—	—	X	X	—	—	—	X	—	X	X	X	—	—	X	X	—	—	X	X	—	—	—	X
C_4	XOR	—	—	—	—	X	X	X	X	—	—	—	—	X	X	X	X	—	—	—	—	X	X	X	X	—	—	—	—	X	X	X	X
C_5	XOR	—	—	—	—	—	—	—	—	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	—	—	—	—	—	—	—	—
C_6	XOR	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
C_7	XOR	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—

Check Bits	Position 64B/C — Data In 32–47																Position 64D — Data In 48–63															
	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63
C_0	X	X	X	—	X	—	X	—	X	—	X	—	X	—	—	—	X	X	X	—	X	—	X	—	X	—	X	—	X	—	—	—
C_1	X	X	—	X	—	X	—	X	—	X	—	X	—	X	—	—	X	X	—	X	—	X	—	X	—	X	—	X	—	X	—	—
C_2	X	—	X	X	X	X	—	—	X	X	—	—	—	—	X	—	X	—	X	X	X	X	—	—	X	X	—	—	—	—	X	—
C_3	—	X	X	X	—	—	X	X	—	—	X	X	—	—	—	X	—	X	X	X	—	—	X	X	—	—	X	X	—	—	—	X
C_4	—	—	—	—	X	X	X	X	—	—	—	—	X	X	X	X	—	—	—	—	X	X	X	X	—	—	—	—	X	X	X	X
C_5	X	X	X	X	X	X	X	X	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	X	X	X	X	X	X	X	X
C_6	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
C_7	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Check Bits	Position 64B/C — Data In 64–75												Position 64B/C — Data In 76–87											
	64	65	66	67	—	68	69	—	—	70	71	—	72	73	74	75	76	77	78	79	—	80	81	—	—	82	83	—	84	85	86	87
C_0	X	X	—	X	—	X	—	X	—	X	—	X	—	X	—	—	X	X	—	X	—	X	—	X	—	X	—	X	—	X	—	—
C_1	X	—	X	X	X	X	—	—	X	X	—	—	—	—	X	—	X	—	X	X	X	X	—	—	X	X	—	—	—	—	X	—
C_2	X	X	X	—	X	—	X	—	X	—	X	—	X	—	—	—	X	X	X	—	X	—	X	—	X	—	X	—	X	—	—	—
C_3	—	X	X	X	—	—	X	X	—	—	X	X	—	—	—	X	—	X	X	X	—	—	X	X	—	—	X	X	—	—	—	X
C_4	X	X	X	X	X	X	X	X	—	—	—	—	—	—	—	—	X	X	X	X	X	X	X	X	—	—	—	—	—	—	—	—
C_5	—	—	—	—	X	X	X	X	—	—	—	—	X	X	X	X	—	—	—	—	X	X	X	X	—	—	—	—	X	X	X	X
C_6	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
C_7	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Check Bits	Position 64D — Data In 88–95															
	—	88	89	—	—	90	—	—	—	91	—	—	92	93	94	95
C_0	—	—	—	—	X	X	X	X	—	—	—	—	X	X	X	X
C_1	—	—	—	—	—	—	—	—	X	X	X	X	X	X	X	X
C_2	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
C_3	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
C_4	X	—	X	X	X	X	—	—	X	X	—	—	—	—	X	—
C_5	X	X	—	X	—	X	—	X	—	X	—	X	—	X	—	—
C_6	X	X	X	—	X	—	X	—	X	—	X	—	X	—	—	—
C_7	—	X	X	X	—	—	X	X	—	—	X	X	—	—	—	X

NOTES:
1. The check bits are derived by performing the indicated parity operation on the data bits marked with an "X" in each row. XOR = EXCLUSIVE OR, XNOR = EXCLUSIVE NOR. The XNOR is performed internally for check bits outputs CBO_1, and CBO_2 in position and 64A/32A.
2. If C5 is translated by the equation $C5A = C_5 \oplus C_6 \oplus C_7$, then the binary code of C_4, C_{5A}, C_6, and C_7 define each 4-bit data group in a binary sequence, for data configurations of 64 bits or less.

Positive Versus Negative Logic

System designers use MECL 10,000 in both positive and negative logic formats. Positive logic has MECL V_{OH} (approx. −0.9 V) for Logic 1 and MECL V_{OL} (approx. −1.7 V) for Logic 0. Negative logic reverses Logic 1 and 0 voltage definitions with V_{OL} being a Logic 1. This data sheet is written around positive logic definitions. Tables and descriptions are written in terms of high (H) and low (L) logic levels to simplify translation between formats.

TABLE 9 — SYNDROME BIT DECODING FOR 96-BIT DATA

Syndrome Bits				S7	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H
				S6	L	L	L	L	H	H	H	H	L	L	L	L	H	H	H	H
				S5	L	L	H	H	L	L	H	H	L	L	H	H	L	L	H	H
				S4	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H
S0	S1	S2	S3																	
L	L	L	L		*	C_4	C_5	T	C_6	T	T	M	C_7	T	T	M	T	M	M	T
L	L	L	H		C_3	T	T	D_{15}	T	D_{31}	D_{75}	T	T	D_{47}	D_{87}	T	M	T	T	D_{63}
L	L	H	L		C_2	T	T	D_{14}	T	D_{30}	D_{72}	T	T	D_{46}	D_{84}	T	M	T	T	D_{62}
L	L	H	H		T	M	M	T	D_{71}	T	T	D_{69}	D_{83}	T	T	D_{81}	T	D_{89}	D_{88}	T
L	H	L	L		C_1	T	T	D_{13}	T	D_{29}	D_{74}	T	T	D_{45}	D_{86}	T	M	T	T	D_{61}
L	H	L	H		T	D_7	D_{11}	T	D_{27}	T	T	D_{23}	D_{43}	T	T	D_{39}	T	D_{55}	D_{59}	T
L	H	H	L		T	D_5	D_9	T	D_{25}	T	T	D_{21}	D_{41}	T	T	D_{37}	T	D_{53}	D_{57}	T
L	H	H	H		D_3	T	T	D_{91}	T	D_{66}	D_{19}	T	T	D_{78}	D_{35}	T	D_{51}	T	T	M
H	L	L	L		C_0	T	T	D_{12}	T	D_{28}	D_{73}	T	T	D_{44}	D_{85}	T	M	T	T	D_{60}
H	L	L	H		T	D_6	D_{10}	T	D_{26}	T	T	D_{22}	D_{42}	T	T	D_{38}	T	D_{54}	D_{58}	T
H	L	H	L		T	D_4	D_8	T	D_{24}	T	T	D_{20}	D_{40}	T	T	D_{36}	T	D_{52}	D_{56}	T
H	L	H	H		D_2	T	T	D_{90}	T	D_{65}	D_{18}	T	T	D_{77}	D_{34}	T	D_{50}	T	T	M
H	H	L	L		T	M	M	T	D_{70}	T	T	D_{68}	D_{82}	T	T	D_{80}	T	M	M	T
H	H	L	H		D_1	T	T	M	T	D_{67}	D_{17}	T	T	D_{79}	D_{33}	T	D_{49}	T	T	M
H	H	H	L		D_0	T	T	M	T	D_{64}	D_{16}	T	T	D_{76}	D_{32}	T	D_{48}	T	T	M
H	H	H	H		T	D_{94}	D_{93}	T	D_{92}	T	T	M	D_{95}	T	T	M	T	M	M	T

* = No Errors
C_i = Single Bit Error in Check Bit i
D_i = Single Bit Error in Data Bit i
T = Two Errors
M = Multiple Bit Errors (More Than Two)
S_i = Syndrome Bit i Output for 16, 32, 64, and 96 Data Configurations (see Figures 3, 4, 5, and 6)

NOTE:
For data configurations of less than 96 bits, unused data bits in the above table should be replaced with an "M" (for multiple bit error).

TABLE 10 — PROPAGATION DELAY EQUATIONS FOR MULTI-CHIP DATA CONFIGURATIONS

Path	Data Bit Configuration	Propagation Delay Equation
Data In to Check Bit Out (Use Table 14)	32	(DI to CBO, pos. 32A) + (PCB to CBO, pos. 32B) = 10.7 ns + 6.3 ns = 17 ns
	48, 64, 76, 88, 96	(DI to CBO, pos. 64A) + XOR = 10.7 ns + XOR
Data In to Error Detect (Use Table 15)	32	(DI to SYO, pos. 32A) + (SYI to Error, pos. 32B) = 10.7 ns = 10.3 ns = 21 ns
	48, 64, 76, 88, 96	(DI to SYO, pos. 64B/C) + XOR + (SYI to Error, pos. 64A) = 13.2 ns + XOR + 7.9 ns = 21.1 ns + XOR
Data In to Correct Data Out (Use Table 15)	32	(DI to SYO, pos. 32A) + (SYI to SYO, pos. 32B) + (SYI to DO, pos. 32A) = 10.7 ns + 6.3 ns + 11 ns = 28 ns
	48, 64, 76, 88, 96	(DI to SYO, pos. 64B/C) + XOR + (SYI to DO, pos. 64A) = 13.2 ns + XOR + 11 ns = 24.2 ns + XOR
Data In to Single Error (SE) Out (Use Table 15)	32	(DI to SYO, pos. 32A) + (SYI to SYO, pos. 32B) + (SYI to SE, pos. 32A) = 10.7 ns + 6.3 ns + 11.8 ns = 28.8 ns
	48, 64, 76, 88, 96	(DI to SYO, pos. 64B/C) + XOR + (SYI to SE, pos. 64A) = 13.2 ns + XOR + 11.8 ns = 25 ns + XOR

Note* Calculations do not include circuit board wiring delays.

TABLE 11 — ABSOLUTE MAX RATINGS

Rating	Symbol	Value	Unit
Supply Voltage (V_{CC} = 0)	V_{EE}	-7.0 to 0	Vdc
Input Voltage[2] (V_{CC} = 0)	V_{in}	0 to V_{EE}	Vdc
Output Source Current — Continuous — Surge	I_o	<30 <100	mAdc
Storage Temperature	T_{stg}	-55 to +150	°C
Junction Temperature	T_J	165	°C

NOTES:
1. Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.
2. Input voltage limit is V_{CC} to -2.0 volts for bidirectional Pin 65 when used as an input (slice position 16 or 64A/32A).

TABLE 12 — RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value	Unit
Supply Voltage (V_{CC} = 0 Volts)	V_{EE}	-4.68 to -5.72	Vdc
Operating Temperature (Functional)	T_A	0 to +70	°C
Output Drive	—	50 Ω to -2.0 Vdc	—
Max Junction Temp	T_J	130	°C

TABLE 13 — ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board with heatsink and transverse air flow greater than 1000 lfpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only one input, or for one set of input conditions. Other inputs tested in the same manner.

@ Test Temperature	Test Voltage Values (Volts) V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
0°C	-0.840	-1.95	-1.145	-1.490	-5.2
+25°C	-0.810	-1.95	-1.105	-1.475	-5.2
+70°C	-0.730	-1.95	-1.050	-1.450	-5.2

Characteristics	Symbol	Pin Under Test	MC10905 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Typ	+25°C Max	+70°C Min	+70°C Max	Unit	Voltage Applied to Pins Listed Below V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	(V_{CCO}) (V_{CC}) Gnd
Power Supply Drain Current	I_{EE}	9, 43	—	897	—	717	897	—	897	mAdc	—	—	—	—	9.43	3. 15, 20 26, 60, 66
Input Current																
DI_{0-15}	I_{inH}	27	—	200	—	—	200	—	200	μAdc	27	—	—	—		
SYI_6, SYI_7	I_{inH}	57, 58	—	400	—	—	400	—	400	μAdc	57	—	—	—		
OLE, SYI_5	I_{inH}	62, 56	—	350	—	—	350	—	350	μAdc	62	—	—	—		
All Others	I_{inH}	47	—	300	—	—	300	—	300	μAdc	47	—	—	—		
All Except Pin 65	I_{INL}	47	0.5	—	0.5	—	—	0.5	—	μAdc	—	47	—	—		
Logic "H" Output Voltage	V_{OH}	2	-1.000	-0.840	-0.960	—	-0.810	-0.905	-0.730	Vdc	44, 45, 61	—	—	—		
Logic "L" Output Voltage	V_{OL}	2	-1.950	-1.665	-1.950	—	-1.650	-1.950	-1.625	Vdc	44, 45	—	—	—		
Logic "H" Threshold Voltage	V_{OHA}	2	-1.02	—	-0.980	—	—	-0.925	—	Vdc	—	—	44, 45, 61	—		
Logic "L" Threshold Voltage	V_{OLA}	2	—	-1.645	—	—	-1.630	—	-1.605	Vdc	—	—	44, 45	—		

NOTE: All inputs have pulldown resistors (~68 kΩ) between the input and V_{EE} including Pin 65.

Switching Characteristics Over Operating Voltage and Temperature Range

Tables 14–17 define timing characteristics of the MC10905 over operating voltage and temperature ranges. Worst-case Setup and Hold and Propagation Delays are *calculated* for V_{EE} = -5.2 volts ±10% and a T_{Jmax} = 115°C. The maximum recommended operating junction temperature is +130°C.

Calculated limits are based on several performance factors as described in Motorola's Preliminary Design Manual for the MECL 10,000 Macrocell Array. Factors include worst case delays due to Macro selections, Fan-Out, Metal Lengths, Wire-OR, and Input Follower options. AC measurements are performed on each device to assure process integrity.

TABLE 14 — MAXIMUM PROPAGATION DELAY (IN NANOSECONDS) FOR THE WRITE MODE (GEN = H), 0 to 70°C T_A (T_J NOT TO EXCEED 115°C)

To Output / From Input	DO_{0-15}	CBO_{0-6} Position	
		32B	Others
DI_{0-15}	7.6	13.2	10.7
$\overline{ILE}$	10.0	15.6	13.1
PCB_{0-5}		6.3	
NC		21.1	18.7

TABLE 15 — MAXIMUM PROPAGATION DELAY (IN NANOSECONDS) FOR THE READ MODE (GEN = L), 0 to 70°C T_A (T_J Not to Exceed 115°C)

To Output / From Input	DO_{0-15} Position 16 or 32 B Corrected NC = L	16 or 32 B No Correction NC = H	Others	SYO_{0-6} Position 32A/64A	32B	Others	ERROR Position 16 or 32B	Others	SE Position 16 or 32B	Others
SYI_{0-7}	12.9		11.0		6.3		10.3	7.9	13.7	11.8
DI_{0-15}	19.7	7.6	7.6	10.7	13.2		17.2		20.6	
$\overline{ILE}$	22.1	10.0	10.0	13.1	15.6		19.7		23.0	
CBI_{0-6}	14.8				8.2		12.2		15.6	
NC	10.2									

TABLE 16 — MAXIMUM PROPAGATION DELAY (IN NANOSECONDS) FOR GEN, OLE, AND THE SLICE POSITION SELECT INPUTS, 0 TO 70°C T_A (T_J NOT TO EXCEED 115°C)

To Output / From Input		DO_{0-15}	SYO_{0-6}	Error	SE
OLE		6.3		4.5	4.5
GEN (L → H)		12.5	14.5	7.9	7.9
GEN	NC = L	18.4	11.8	15.8	19.2
(H → L)	NC = H	27.4*	19.3	23.7	26.7
MA, MB, MC		40.2	33.6	37.5	41.0

* NC and GEN are both switched simultaneously H → L.

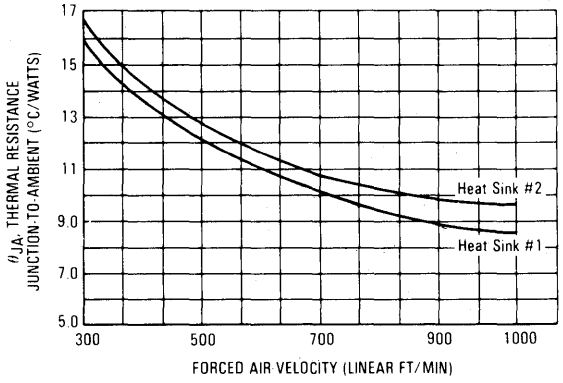
TABLE 17 — SETUP AND HOLD TIMES (IN NANOSECONDS) 0 TO 70°C T_A (T_J NOT TO EXCEED 115°C)

Input	Clock (Ref. Edge)	Conditions	Set Up (Min)	Hold (Min)
DI_{0-15}	$\overline{ILE}$ (L → H)	—	1.5	2.4
CBI_{0-6}	$\overline{ILE}$ (L → H)	—	1.5	2.4
DI_{0-15}	OLE (H → L)	GEN = L, Position - 16 or 32B	20.7	0.9
		All Others	6.3	0.9
$\overline{ILE}$ (H → L)	OLE (H → L)	GEN = L, Position - 16 or 32B	23.1	0
		All Others	8.7	0
SYI_{0-7}	OLE (H → L)	Position - 32B	13.8	-0.5
		Position - Others	11.9	0.2
CBI_{0-6}	OLE (H → L)	Position - 16 or 32B	15.7	-1.0
NC	OLE (H → L)	—	8.9	0.5
GEN (L → H)	OLE (H → L)	—	11.3	0
GEN (H → L)	OLE (H → L)	NC = L	19.3	0
		NC = H	26.8	0
MA, MB, MC	OLE (H → L)	—	41.1	0

TABLE 18 — MINIMUM PULSE WIDTHS (IN NANOSECONDS)

Inputs	PW (Min)
$\overline{ILE}$, OLE	5

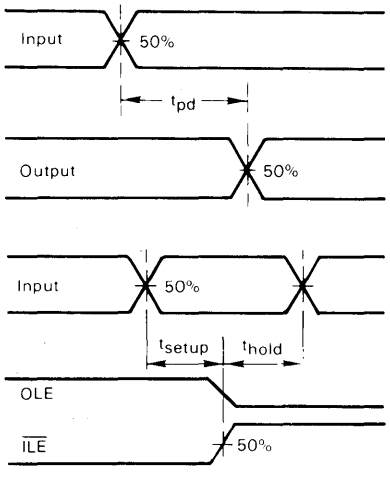
FIGURE 7 — THERMAL CHARACTERISTICS (TYPICAL)



Heat Sink #1 is from THERMALLOY #15832-1, 3 Horizontal Fins, 0.563 inches square, Model No. 2284C.
Heat Sink #2 is from WAKEFIELD #4493, Vertical Fins, 0.5 inches square.
NOTE: $T_J = (\theta_{JA})(P_D) + T_A$ WHERE T_J is the Junction Temperature, T_A is the Ambient Temperature,
$P_D = (I_{EE})(V_{EE}) + (15\ mW)$ (number of 50 Ω outputs).

6

FIGURE 8 — SWITCHING WAFEFORM DEFINITION
Propagation Delays



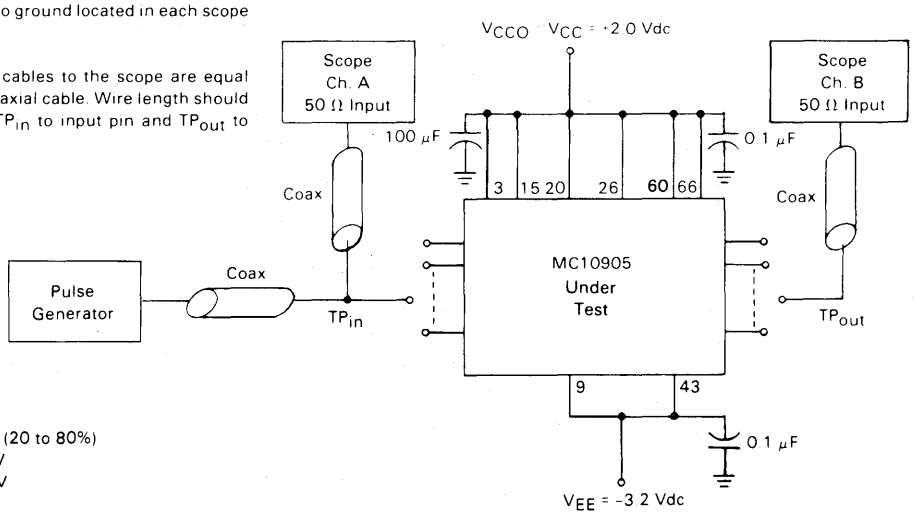
Setup and Hold

TEST PROCEDURE
a) Establish setup time with long t_{hold}
b) Keeping the leading edge of the input constant (t_{setup}) vary the trailing edge of the input to determine t_{hold}

FIGURE 9 — SWITCHING TIME TEST CIRCUIT

50-ohm termination to ground located in each scope channel input.

All input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be ~1 4 inch from TP_{in} to input pin and TP_{out} to output pin.



INPUT PULSE
$t_r = t_f$ = 1.0 ns (20 to 80%)
V_{OH} = +1.11 V
V_{OL} = + 0.31 V

6

MOTOROLA

MCA2500ECL

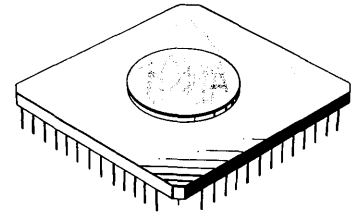
Advance Information

MOSAIC II
MACROCELL
ARRAY

MCA2500ECL MACROCELL ARRAY

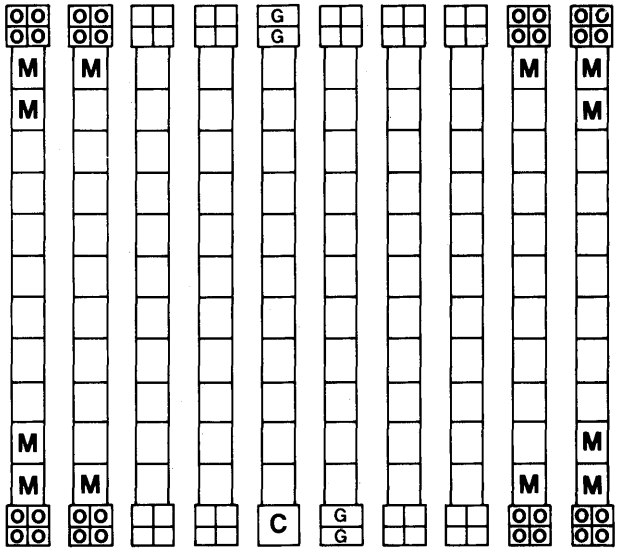
This specification establishes design and performance requirements for the MCA2500ECL, first in a new series of ultra high-performance bipolar arrays. Built with a high density MOSAIC II process, the circuit contains the logic power of over 2500 equivalent subnanosecond gates on one integrated circuit chip. The routing flexibility and macrocell structures are designed to meet the market needs for next generation computer systems.

- Logic Function Specified By User
- Metal Mask Programmable (Three Unique Masks)
- Up to 2800 Equivalent Gates
- Internal Gate Delays — 0.30 ns Typical
- Output Gate Delays — 0.75 ns Typical
- Power Dissipation — 6.5 Watts Typical
- Supported By Complete CAD Development System
- Interfaces with MECL10K/10KH or ECL 100K
- On-Chip System Design Aids



149-Pin
Pin Grid Array Package
CASE 768

FIGURE 1 — MCA2500ECL MACROCELL ARRAY LAYOUT



6

PRODUCT DESCRIPTION

The MCA2500ECL Macrocell Array is a 300 picosecond, 2500 equivalent gate density LSI monolithic integrated circuit designed around the MOSAIC II oxide isolated, walled-base, walled-emitter process. The array is composed of two types of macrocells; M for major cells and O for output cells. Macrocells are similar to ECL integrated circuit packages. A macrocell library provides a selection of fully characterized logic functions, similar to an IC data book. Using the library, a designer can draw schematics for LSI macrocell array circuits similar to drawing printed circuit board schematics. The only restrictions are that designs are limited to logic functions within the library, the number of macrocell positions on the array, and the number of package I/O pins. The MCA2500ECL consists of 178 cells organized as shown in Figure 1. There are 110 major (M) cells, and 68 output (O) cells.

Most of the circuit logic is accomplished using major macrocells. Many of the M macrocell logic functions may be subdivided into half macrocells, such that different type cells can be placed into one M location for more efficient logic utilization. Simple logic functions are further divided into quarter macrocells so that it is possible to mix four different logic circuits within one M location to achieve maximum array utilization. Input signals can go directly to M or O macrocell inputs that are not marked with an asterisk (*). A signal leaving the array must go through an output (O) macrocell.

The MCA2500ECL array uses three layers of metal to accomplish the required routing and power distribution. Each cell location is comprised of uncommitted transistors and resistors, as shown in Figures 2 and 3, which are automatically interconnected with the first layer of metal forming the chosen library macro logic function. Power distribution (fixed-metal) is contained almost entirely on third layer metal and is common to all array designs. Both cell intraconnection and routing of power signals are invisible to the user. The interconnection among macrocell functions and I/O pins are accomplished with a grid of horizontal and vertical routing channels. Vertical channels are positioned between and outside the columns of cell locations, using the first layer of metal. Horizontal channels are second layer metal and capable of routing across macrocells and vertical channels such that placement of a macro on the array never obstructs these routing channels. The three layers of metal are separated by an isolation and can be connected through "VIA's." The use of ECL series-gated techniques yield improved circuit performance and reduces routing channel requirements, thus greatly simplifying the Computer Aided Design interconnection task.

Motorola's MCA-CAD (Macrocell Array — Computer Aided Design) system is the engineering design interface between Motorola and customers developing macrocell circuits (MCA options). Customers can either use terminals at their own geographic location or access CAD software at a Motorola customer CAD design center, in both cases, over phone lines or Data Comm network. The CAD software contains programs to assist in each stage of option design with the addition of several special programs to catch syntactical errors or design violations during the design procedure rather than at test.

The CAD system is common to a variety of MCA products such that designing with one array is only "cosmetically" different than designing with another. Motorola offers a family of array products so that array size, performance, power dissipation, and package can be optimized to match system requirements. Library macrocell functions (macros) are also common to several array types.

Compared with gate arrays, the use of higher component density and more efficiently designed subcircuits (macros) yield a substantial improvement in performance (circuit speed), while a greater utilization of on-chip components reduces potential system costs.

The high packing density of MCA2500ECL arrays offer up to 100-to-1 reduction in system component count when compared with equivalent systems developed using conventional logic (separately packaged SSI/MSI logic functions). System power dissipation is also reduced by as much as 12-to-1. Because a large degree of optimization is possible, the user obtains performance similar to that of a full custom design, and the accelerated turnaround time of a conventional semi-custom array.

6

TABLE 1 — BASIC MCA2500ECL ARRAY FEATURES

1. 178 total cells with 120 Input/Output ports.
2. Up to 2800 equivalent gates if full adders and latches are used in all cells.
3. Up to 2100 equivalent gates if flip-flops and latches are used in all cells.
4. Power Dissipation — 6.5 watts typical.
5. Major cell delays — 0.30 to 0.9 ns typical.
6. Output cell delays — 0.60 to 1.25 ns typical.
7. Up to 38 cells can drive 25 ohm loads (all outputs can drive 50 Ω loads).
8. Edge speed — 1.0 ns typical 20 to 80%.
9. Ambient temperature range (with heat sink and 750 lfpm air) −0°C to 70°C.
10. Θ_{JA} = 3.3 °C/W typical with heatsink and 750 lfpm air flow in 149 pin grid array package.
11. Voltage compensated, V_{EE} = −4.2 Vdc to −4.8 Vdc.
12. Interfaces with MECL 10K/10KH or ECL 100K.

FIGURE 2 — ¼ MAJOR CELL (M) SCHEMATIC
(Repeated 4X per M Cell)

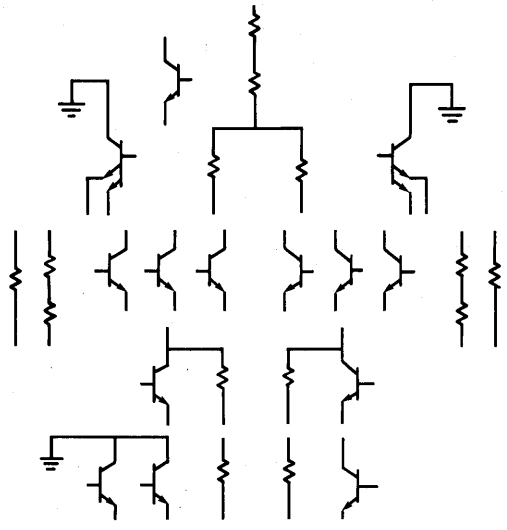
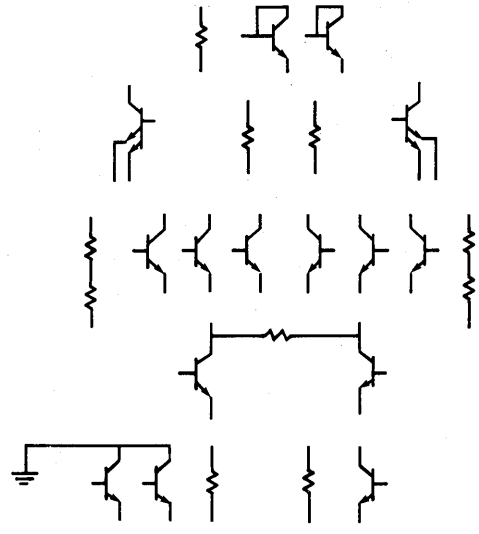


FIGURE 3 — OUTPUT CELL (O) SCHEMATIC



The value of series-gating can be seen by the logic equation for the 4-input exclusive OR gate shown in Figure 4. To implement this function with gates would require eight 4-input AND gates plus one 8-input OR gate. Gates also might be required to form the true and complement of each input.

About 40 connections would be required if gates were used, compared to five connections for the series-gated macro. Each output of the cell has a two-emitter transistor that allows a 1.0 mA or 2.0 mA emitter follower selection for power/speed optimization. This also provides the emitter-dotting capability and at the same time maintains the non-dotted output function through the second emitter.

FIGURE 4 — SCHEMATIC OF 4-INPUT EXCLUSIVE OR GATE
$(Y = \bar{A}BCD + A\bar{B}CD + AB\bar{C}D + ABC\bar{D} + \bar{A}\bar{B}\bar{C}D + \bar{A}\bar{B}C\bar{D} + \bar{A}B\bar{C}\bar{D} + A\bar{B}\bar{C}\bar{D})$

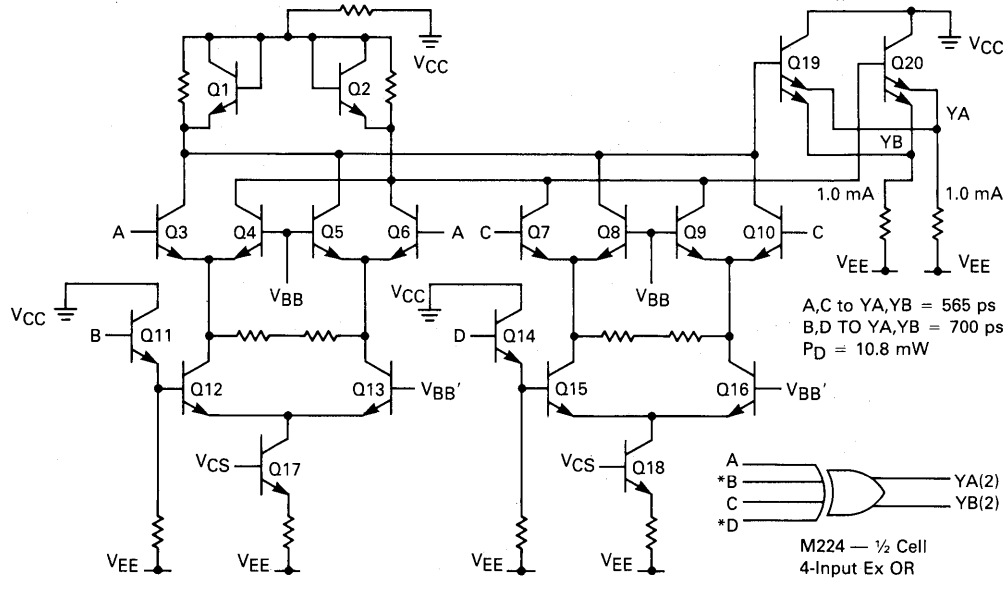
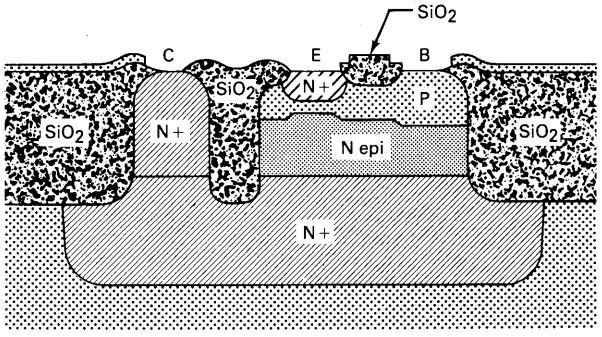


FIGURE 5 — CROSS SECTION of MOSAIC II PROCESS



M. G. Farrell and S. Mastroianni, U.S. Patent 4,199,380, April 22, 1980.

PROCESS DESCRIPTION

The MCA2500ECL has been fabricated by the MOSAIC II (Motorola Oxide-isolated Self-Aligned Implanted Circuits) process utilizing a walled-emitter structure and a three layer metallization system. Usage of a walled-emitter greatly reduces device area and parasitic capacitances associated with the device. A cross-section of the transistor is shown in Figure 5. Collector-to-emitter leakage current has been minimized by using a reverse master mask technique (RMMT). The reverse master mask structures in Figure 5 are the inactive base areas covered by oxide on either side of the emitter. The active base and emitter are both implanted using this oxide for mask edge definition so that both are implanted without an intermediate masking step. Eliminating the intermediate step minimizes the collector-emitter leakage found in conventional walled-emitter structures. Separating the active and inactive base implants also reduces series base resistance without compromising the current gain of the active device. Reduced series base resistance is critical to building small transistors with high performance characteristics. Collector resistance is minimized by use of a thin epi and a deep n^+ collector. Three levels of metallization have been used, two for interconnection wiring and the third for power buses only.

TABLE 2 — MCA1200ECL/MCA2500ECL MACROCELL ARRAY COMPARISON

FEATURE	MCA1200ECL	MCA2500ECL
Interface Levels	MECL10K	10KH/100K/10K
I/O Ports	60	120
Major Cells (M)	48	110
Output Cells (O)	26	68
Interface Cells (I)	32	—
Clock Generator	NO	YES
Minimum Cell Partition	½ Cell	¼ Cell
Diagnostics	YES	Modified LSSD Macro
Basic Gate Delay (Typical)	0.65 ns	0.30 ns
4-Input OR/NOR	1.2 ns Max	0.5 ns Max
D Flip-Flop (Clock)	1.5 ns Max	0.7 ns Max
4-to-1 Multiplexer	1.4 ns Max	0.6 ns Max
Full Adder	2.8 ns Max	1.1 ns Max
Output OR Gate	3.1 ns Max	1.0 ns Max
Power (Typical)	4 Watts	6.5 Watts
Package	68 Leadless	149-Pin Grid Array
Routing Channels:		
Vertical	84	220
Horizontal	104	426
Process	MOSAIC I (2-Layer Metal)	MOSAIC II (3-Layer Metal)
Personalization Layers	3 (2 Metal and 1 VIA)	3 (2 Metal and 1 VIA)

PERFORMANCE COMPARISON

Although the MCA2500ECL array uses many features pioneered with Motorola's MOSAIC I macrocell array family, it is a totally new design representing the latest in high-speed array concepts. The MCA2500ECL array follows Motorola's plan to continually match the latest bipolar processing technology with innovative circuit concepts. Table 2 provides a comparison between Motorola's MOSAIC I technology, MCA1200ECL array introduced in 1979, and the state-of-art MOSAIC II technology MCA2500ECL macrocell array.

In addition to improved performance and greater density, the MCA2500ECL has eliminated the need for simple I Cells by allowing each Major Cell to be partitioned into quarter cells. SSI complexity functions are implemented in quarter cells. In addition, by locating all power buses on third layer metal, a significant increase in the number of routing channels was accomplished while maintaining minimum chip dimensions.

The number of I/O ports has been increased to a full 120 channels with up to 68 outputs.

SPECIAL DESIGN FEATURES

Innovative design features have been incorporated into the MCA2500ECL array to simplify system design and enhance performance.

Clock Pulse Generator Cell (Figure 6)

The on-chip clock generator is capable of producing a narrow, edge-triggered pulse, controlled by Input A. The output signal from the generator is produced by a 10 mA emitter-follower and is capable of driving heavy loads with minimized speed degradation. Use of the generator eliminates the necessity of supplying a narrow clock pulse to the chip. Only a single clock edge needs to be supplied to the chip when the generator is used. The output of the generator can be forced high or low by using control inputs B and C.

Optional Edge Rate Selection

The typical output rise-time (20 to 80%) or fall-time (80 to 20%) is 1.0 ns. For situations where slower edge rates are desirable, such as reducing cross talk or passing signals across board connectors, Motorola offers an optional output edge rate slowdown. Once selected (via (via CAD interface) the typical output rise- or fall-time is increased to 1.5 ns.

These values are specified for the output package pin driving 50 ohms (25 ohms for bus drivers) to −2.0 Volts.

MACROCELL LIBRARY — M CELL and O CELL

Each macrocell M and O cell location contains a number of conventional transistors and resistors that can be interconnected with CAD selected metal patterns to form logic functions. A computer-stored macrocell library contains pre-defined metal patterns for more than 60 different M and O logic functions, all available to the engineer designing an LSI circuit (macrocell array option). Designers have the freedom to select any of the macrocell functions for any M or O cell location. However, an O cell macro cannot be placed in an M cell location and visa versa. Thus, an M cell — a multiplexer, or dual flip-flop, or LSSD type diagnostic cell could be formed in any or all M locations, but not in an O location. The functions available to the designer are similar to those defined in Motorola's MOSAIC I array family, however performance is greatly improved. A list of macrocell functions currently stored in the library is shown in Table 3.

Major Cells (M)

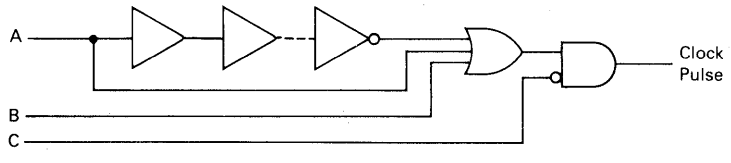
The Major Cells in the array comprise the internal area on the chip and are used for the majority of logic capability. Each Major Cell contains 56 transistors and 56 resistors as shown in Figure 2. These components are connected together on first layer metal to form logic functions with up to four series-gated structures. The macros in the Major Cell Library can use ¼, ½, ¾ or 1 entire major cell. Each macro specifies how much of the cell is needed to implement that particular function.

Worst case propagation delay is specified for V_{EE} = −4.2 Vdc to −4.8 Vdc and a maximum junction temperature of T_J max = 115°C. In general, a lower junction temperature can result in faster propagation delays. Macrocell power dissipation is specified at V_{EE} = −4.5 V.

The worst case setup and hold times are also listed for all flip-flops and latches.

The worst case minimum pulse width (t_{PW}) is specified for the clock inputs of flip-flops and latches to insure proper operation.

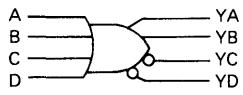
FIGURE 6 — LOGIC SCHEMATIC of CLOCK PULSE GENERATOR



Examples of Major Cell Macros

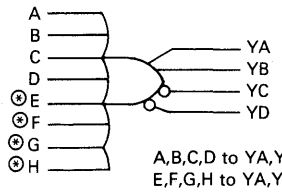
For complete Macrocell Library, consult Motorola's MCA II Design Manual.

M201 — 4-Input OR/NOR
¼ Cell



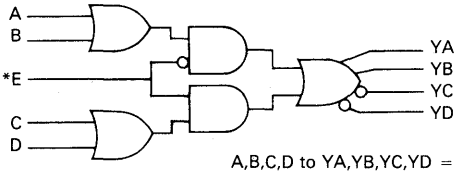
A,B,C,D to YA,YB,YC,YD = 500 ps
P_D = 3.0 mW

M203 — 8-Input OR/NOR
½ Cell



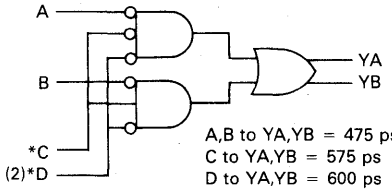
A,B,C,D to YA,YB,YC,YD = 525 ps
E,F,G,H to YA,YB,YC,YD = 600 ps
P_D = 5.4 mW

M254 — 2-to-1 Multiplexer w/Gated Inputs
¼ Cell



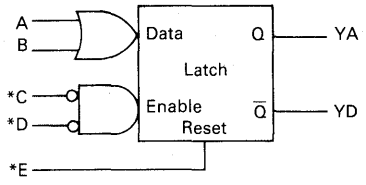
A,B,C,D to YA,YB,YC,YD = 500 ps
E to YA, YB,YC,YD = 575 ps
P_D = 5.4 mW

M253 — 2-to-1 Multiplexer w/Enable
¼ Cell



A,B to YA,YB = 475 ps
C to YA,YB = 575 ps
D to YA,YB = 600 ps
P_D = 5.4 mW

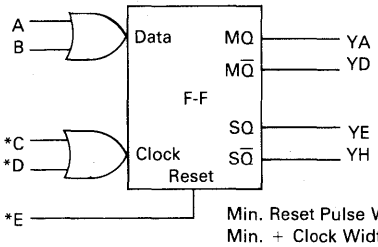
M293 — D Latch
¼ Cell



	YA	YD	C,D ↑ Set	C,D ↑ Hold
A,B	575	575	750	0
Enable	700	700	—	—
Reset	1000	1000	—	—

P_D = 14.4 mW

M291 — D Flip-Flop
½ Cell



Min. Reset Pulse Width = 1250
Min. + Clock Width = 1250
Min. − Clock Width = 1250

	YA	YD	YE	YH	Clock ↑ Set	Clock ↑ Hold
A,B	575	575	—	—	750	0
Clock ↓	700	700	—	—	—	—
Clock ↑	—	—	700	700	—	—
Reset	875	875	1750	1750	—	—

P_D = 26.0 mW

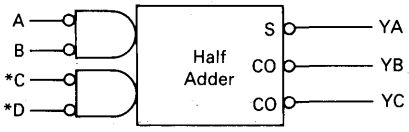
Min. Clock Period = 2500
Max. Toggle Frequency ≈ 400 MHz

(continued)

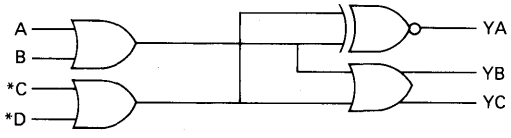
NOTES:
1. Values given for propagation delay, t_{pd}, are max for 1.0 mA output follower current driving a fan-out of 1. Values given for power dissipation, P_D, are typical with unloaded outputs. Output follower current can be selected for either 0.0 or 1.0 mA. Numbers enclosed in parenthesis at the inputs indicate fan-in other than 1.
2. Unmarked upper level inputs and ⊛ inputs can be connected to package pins.
3. *Inputs are connected to an input follower. Numbers enclosed in parenthesis at the output indicate the total number of internal wire OR's.

Examples of Major Cell Macros (continued)

M284 — Half Adder ¼ Cell

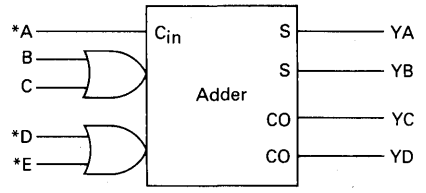


Logic Equivalent

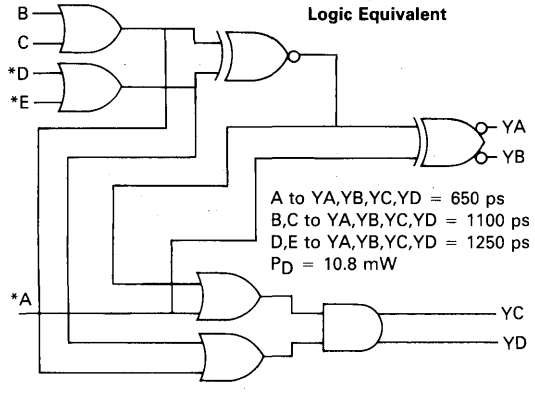


A,B to YA,YB,YC = 450 ps
C,D to YA,YB,YC = 575 ps
P_D = 5.4 mW

M282 — Full Adder ½ Cell

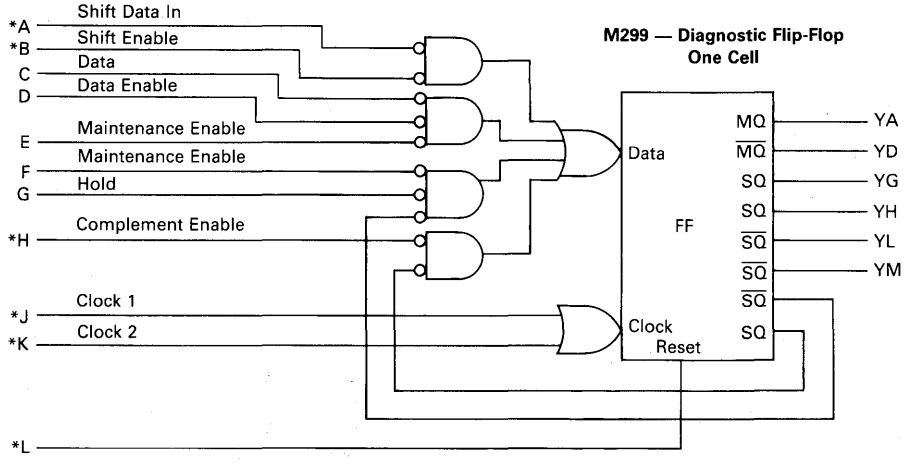


Logic Equivalent



A to YA,YB,YC,YD = 650 ps
B,C to YA,YB,YC,YD = 1100 ps
D,E to YA,YB,YC,YD = 1250 ps
P_D = 10.8 mW

M299 — Diagnostic Flip-Flop One Cell



	YA,YD	YG,YH	YL,YM	CLOCK ↑ Set	CLOCK ↑ Hold
A,B,H	1225	—	—	1400	0
C,D,E,F,G	1125	—	—	1300	0
Clock ↓	700	—	—	—	—
Clock ↑	—	700	700	—	—
Reset	875	1750	1750	—	—

P_D = 41.8 mW

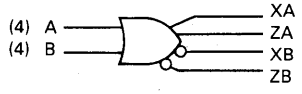
Output Cells (O)

The Output Cells are located at the top and bottom of the array. These macros can use 1 or 2 output cells. The macro library specifies how many output cells are needed for each macro.

The Output Cells are primarily used to provide the interface between internal logic and logic outside the package by supplying 50 ohm and 25 ohm drive capability. These macros also provide extra logic capability with logic functions such as OR-AND, Exclusive OR with enable, 2-to-1 multiplexer with enable, latches and flip-flops. The Output Cell Library provides macros with a similar logic capability to ¼ of a Major Cell.

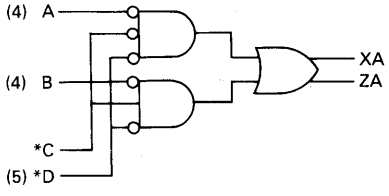
Examples of Output Cell Macros

X201 — 2-Input OR/NOR One Cell



A,B to Outputs = 875 ps
P_D = 16.7 mW

X253 — 2-to-1 Multiplexer w/Enable One Cell

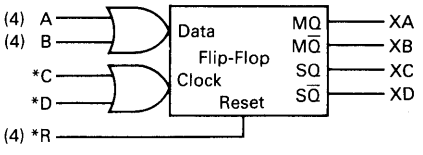


A,B to XA,ZA = 900 ps
C,D to XA,ZA = 1275 ps
P_D = 21.2 mW

X261 — 25 Ω OR/NOR Driver One Cell

A,B to XA+,XB+ = 1900 ps
A,B to XA−,XB− = 1500 ps
P_D = 38.5 mW
V_{OL} Max = −1.95 Vdc at XA and XB Outputs

X291 — Gated Flip-Flop Two Cells

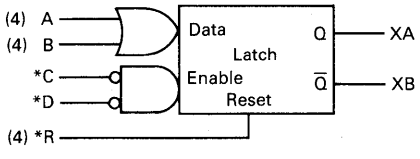


Min. + Clock Width = 2000 ps
Min. − Clock Width = 2000 ps
Min. Reset Pulse Width = 2000 ps

	XA, XB	XC, XD	Clock ↑ Set	Clock ↑ Hold
A,B	925 ps	—	1000 ps	0 ps
Clock ↑	—	1200 ps	—	—
Clock ↓	1150 ps	—	—	—
Reset	1550	3100	—	—

P_D = 56.0 mW

X292 — Gated Latch One Cell



	XA	Clock ↑ Set	Clock ↑ Hold
A,B	950 ps	1000 ps	0 ps
Enable	1300 ps	—	—
Reset	1800	—	—

P_D = 30.2 mW

NOTE: All X outputs come off the collector and must be routed to the large output devices near the bonding pads. All Z outputs have a 1.0 mA emitter follower and may be used for driving internally on the chip.

TABLE 3 — MCA2500ECL MACROCELL LIBRARY

Major Cells	No. of M-Cells
M200 5-Input OR/NOR	¼
M201 4-Input OR/NOR	¼
M202 2-Input OR/NOR	¼
M203 8-Input OR/NOR	½
M204 12-Input OR/NOR	1
M211 2-2 OR/AND	¼
M212 3-2-2-2 OR/AND	½
M213 4-3-3-3 OR/AND	1
M214 2-2-2-2-1-1-1-1 OR/AND	1
M215 2-2-3-3-3 OR/AND	1
M216 4-2-3-2-3 OR/AND	1
M217 5-3-4-2 OR/AND	1
M218 5-4-3-2-1 OR/AND	1
M219 3-3 OR/AND	¼
M221 2-2 OR/EX NOR	¼
M222 Dual 2-2 OR/AND/EX NOR	1
M223 4-Input EX NOR	½
M224 4-Input EX OR	½
M225 2-1-1-2 OR/AND/EX OR	½
M226 2-1-1-2 EX NOR	½
M227 2-1 EX OR/AND/NAND	½
M228 2-1 AND/EX NOR	¼
M231 D Flip-Flop	½
M232 D Flip-Flop w/MUX	¾
M241 D Latch	¼
M242 Dual D Latch	½
M243 D Latch w/MUX	½
M244 Gated 2-Way D Latch	½
M245 Gated 4-Way D Latch	¾
M246 EX NOR D Latch	½
M251 4-to-1 MUX w/Enable (Low)	1
M252 Quad 2-to-1 MUX	1
M253 2-to-1 MUX w/Enable (Low)	¼
M254 2-to-1 MUX w/Gated Inputs	¼
M255 Dual 2-to-1 MUX w/Com. SEL.	½
M256 2-to-1 MUX	½
M258 4-to-1 MUX w/Enable (High)	1
M261 1-of-4 Decode (Low)	½
M263 1-of-4 Decode (High)	1
M281 Full Adder	1
M282 Full Adder	½
M283 2-Bit Look-Ahead-Carry Block	1
M284 Half Adder	¼
M290 D Flip-Flop w/Asyn. Set/Reset	½
M291 D Flip-Flop	½
M292 D Flip-Flop w/MUX	¾
M293 D Latch	¼
M294 D Latch w/MUX	½
M295 Gated 2-Way D Latch	½
M296 EX NOR D Latch	½
M297 Gated 4-Way D Latch	¾
M298 Dual D Latch	½
M299 Diagnostic D Flip-Flop	1
M310 4-4-4-4 AND/OR	1
M311 3-3-3-3 AND/OR	1
M312 3-3-3 AND/OR	½
M313 2-2 OR/AND	¼
M315 2-2-1-1 OR/AND	½
M331 3-2-2 AND/OR	½
M332 Gated OR	½
M333 Gated OR	½
M393 D Latch w/OR Enable Neg. Edge	¼

Output Cells	No. of O-Cells
X201 2-Input OR/NOR	1
X202 4-Input OR/NOR	1
X203 2-2 OR Gates	1
X211 2-2 OR/AND	1
X221 2-2 OR/EX NOR	1
X231 D Flip-Flop	2
X232 D Latch	1
X233 Dual D Latch	2
X291 Gated Flip-Flop	2
X292 D Latch	1
X293 Dual D Latch	2
X251 2-to-1 MUX	1
X252 Dual 2-to-1 MUX	2
X253 2-to-1 MUX w/Enable	1
X261 25 Ohm OR/NOR Driver	1

DEVELOPMENT INTERFACE SYSTEM

To develop an MCA2500ECL circuit, a designer first determines the logic function to be performed by each LSI circuit. Then, using remote terminals, he defines the logic to Motorola's Western Area Computer Center in Arizona. Computer programs simplify circuit design by simulating the design logic function, placing Macrocells within the array, and automatically routing signals between the Macrocells and to the I/O package pins.

Successful implementation of a major array program such as the MCA2500ECL depends on a CAD system that accepts user design information, helps verify design accuracy and converts user data into a format compatible with semiconductor mask-making and test equipment. The Motorola CAD system accomplishes these objectives. Its data input format is easily understood and requires no special computer programming knowledge.

CAD Design Features

The CAD system can handle all design functions associated with semiconductor products, including the selection of first or second layer metal, metal widths and spacing, metal internal to Macrocells and power distribution. Macrocell Array designers use skills common to printed circuit board design, yet, with help from the CAD system, convert the equivalent of a small pc board full of SSI/MSI circuits to a high-performance custom LSI Macrocell Array device.

To help with this process, the Macrocell Array CAD system provides the following design features:

- LOGCAP functional simulation
- Error checking of data input
- Fault grading to identify any untested nodes
- Auto place and route
- AC performance simulation to verify input to output propagation delay or performance of internal paths
- Auto definition of longest delay path between selected input and output points
- CAD data base conversion to electron beam exposure mask generation
- CAD generation of Development/Production test programs
- Customer documentation for every design

Hardware

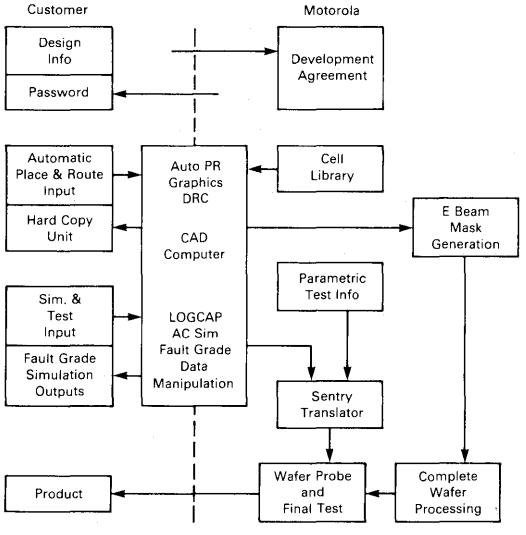
Macrocell array CAD software resides on IBM-compatible computer systems located in Scottsdale, Arizona at the Motorola Western Area Computer Center (WACC). CAD software is available to macrocell array customers on a time-share basis over normal telephone lines or datacomm network at 300 or 1200 baud data rates.

Several pieces of hardware are required at users' locations:

- Tektronix 4112, 4113 or equivalent computer display terminal
- Tektronix 4662 or 4663 interactive digital plotter (Optional)
- 300- or 1200-baud modem
- TTY-compatible keyboard/printer terminal

The appropriate CAD interface hardware is also available through Motorola Regional CAD Design Centers.

FIGURE 8 — MACROCELL ARRAY OPTION DEVELOPMENT FLOW

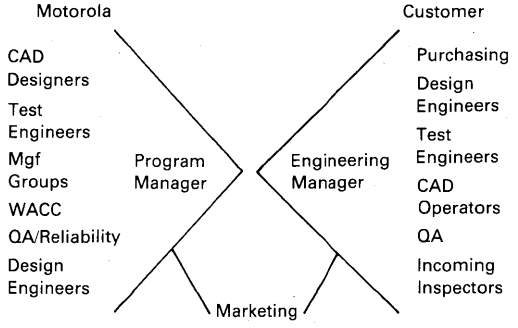


Customer	Motorola
1. Defines the circuit function. 2. Selects the macrocells from the Motorola library. 3. Generates metal interconnect pattern on CAD. 4. Generates the test sequence on CAD.	1. Defines the Macrocell Array. 2. Designs and controls diffusion masks. 3. Develops Macrocell Array. 4. Provides CAD System to help design options. 5. Processes the circuits. 6. Tests the final product.

Program Management

Upon completion of a three-day training course, each customer is assigned a program manager to focus all technical communications during design development. The program manager serves as both engineer and administrator to assure on-time shipment of fully tested prototypes.

FIGURE 9 — MACROCELL ARRAY PROGRAM MANAGER CONCEPT



PACKAGING

The MCA2500ECL macrocell array is offered in the 149-pin grid package as shown in Figure 10.

The package has 120 I/O pins, 6 V_{EE} pins, 6 V_{CC} pins, 16 V_{CCO} pins, and one orientation pin. All contacts are positioned in a uniform rectangular grid on 100 mil centers. Alumina standoffs in each corner of the package provide a 0.050 inch clearance between PC board and package surface. The macrocell array chip is die-attached to the ceramic substrate using a preform to provide excellent thermal coupling between the die and the ceramic. Thermal resistance from junction to case is less than 2°C/W.

In the schematic view of the MCA2500ECL package (Figure 12), separate power and signal metallization layers are provided to minimize lead resistance and inductance. This in turn allows up to 38 outputs to switch simultaneously into 25 ohm loads without creating excessive inductive noise. The die is mounted inverted (away from the PC board) onto a ceramic disk which is in turn brazed to an all alumina substrate. This configuration provides an elevated primary heat conducting surface which is ideally suited to conventional forced air-cooled heat sinks. The central die cavity is square to allow matched lead lengths and voltage drops. Hermiticity is provided with a solder-sealed kovar lid.

HEAT SINKS AND THERMAL CHARACTERISTICS

Worst case propagation delay in the MCA2500ECL is specified for a maximum junction temperature of 115°C. In order to meet this specification, a heat sink and air flow are required. The thermal resistance from junction-

TABLE 4 — ELECTRICAL CHARACTERISTICS

Consistent with industry LSI design requirements, the MCA2500ECL array is voltage-compensated and available in either MECL 10K/10KH temperature tracking or ECL 100K temperature compensation. The array is voltage compensated over a range of V_{EE} values from −4.2 Vdc to −4.8 Vdc.

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Value	Unit
Supply Voltage (V_{CC} = 0)	V_{EE}	−4.2 to −4.8	Vdc
Operating Temperature with Heat Sink and 750 lfpm	T_A	0 to +70	°C
Maximum Junction Temperature (for ac Specifications)	T_J	115	°C
Maximum Clock Input Rise and Fall Times (20 to 80%)	t_r,t_f	10	ns

DC ELECTRICAL CHARACTERISTICS

Input Forcing Voltages	Parameter	MECL 10K/10KH Compatible Spec Limits(1) Ambient Temperature 0°C	25°C	70°C	ECL 100K Compatible Spec Limits(1) Ambient Temperature 0 to 70°C	Unit
V_{IH} Max and V_{IL} Min	V_{OH} Max	−0.840	−0.810	−0.740	−0.880	Vdc
	V_{OH} Min	−1.000	−0.960	−0.900	−1.025	Vdc
	V_{OL} Max	−1.650	−1.650	−1.620	−1.620	Vdc
	V_{OL} Max[2]	−1.950	−1.950	−1.950	−1.950	
	V_{OL} Min	−1.950	−1.950	−1.950	−1.810	Vdc
	V_{OL} Min[2]	−2.020	−2.020	−2.020	−2.020	
V_{IHA} Min and V_{ILA} Max	V_{OHA} Min	−1.020	−0.980	−0.920	−1.035	Vdc
	V_{OLA} Max	−1.630	−1.630	−1.600	−1.610	Vdc
	V_{OLA} Max[2]	−1.950	−1.950	−1.950	−1.950	Vdc
V_{IH} Max	I_{INH} Max[3]	—	—	—	—	μA
Input Voltage Values	V_{IH} Max	−0.840	−0.810	−0.730	−0.880	Vdc
	V_{IL} Min	−1.950	−1.950	−1.950	−1.810	Vdc
	V_{IHA} Min	−1.170	−1.130	−1.070	−1.165	Vdc
	V_{ILA}	−1.480	−1.480	−1.450	−1.475	Vdc

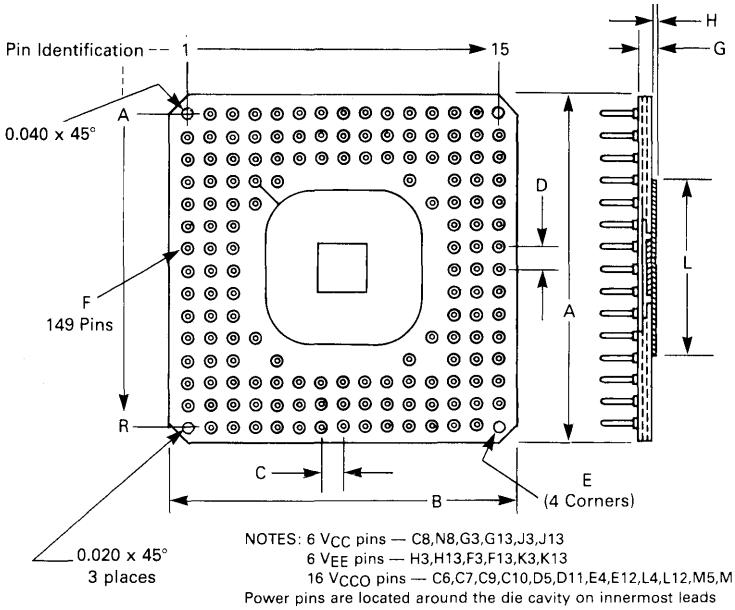
NOTES:
1. DC test limits are specified after thermal equilibrium has been established with the MCA device having an attached heat sink and a transverse air flow of lfpm. V_{EE} = −4.5 V ± 0.3 V. All outputs are loaded with 50 Ω to −2.0 V except the 25 Ω drivers which are loaded with 25 Ω to −2.0 V.
2. These voltage limits are for the driver output of macros with V_{OL} in the cutoff mode.
3. I_{INH} is 50 μA per input fan-in.

to-case is typically 1.2°C/W while the junction-to-ambient thermal is a function of heat sink configuration, mounting technique, and air flow.

Figure 11 shows typical thermal characteristics for the MCA2500ECL using a heat sink designed by Motorola. Selection of an optimum heat sink configuration takes into consideration overall height restrictions, weight, the desirability of omnidirectionality, and the need to obtain reasonably high convection coefficients. In Figure 13, a prototype heat sink was constructed from uncoated 6061 aluminum. For attachment of heat sink to package Aremco 568 Hi-thermal conductivity adhesive was screen printed to approximately 0.0025 inch thickness on both package substrate and heat sink. Pressure was applied to remove air bubbles and ensure proper mating. The adhesive was cured at 200°F (93°C) for 30 minutes.

Care must be taken when selecting a heat sink and attachment procedures to assure mechanical integrity and reliable junction temperatures in any given system.

FIGURE 10 — PACKAGE DIMENSIONS



Dim	Inches	
	Min	Max
A	1.49	1.52
B	1.49	1.52
C	0.100 BSC	
D	0.100 BSC	
E	0.060 ∅ X 0.050 Hi Alumina Standoffs — 4 PL	
F	0.018 ∅ X 0.175 Hi 149 Pins	
G	0.054	0.066
H	0.045	0.050
L	0.620 ∅	0.630 ∅

CASE 768-01

NOTES: 6 V_{CC} pins — C8,N8,G3,G13,J3,J13
6 V_{EE} pins — H3,H13,F3,F13,K3,K13
16 V_{CCO} pins — C6,C7,C9,C10,D5,D11,E4,E12,L4,L12,M5,M11,N6,N7,N9,N10
Power pins are located around the die cavity on innermost leads

FIGURE 11 — THERMAL CHARACTERISTICS (TYPICAL)

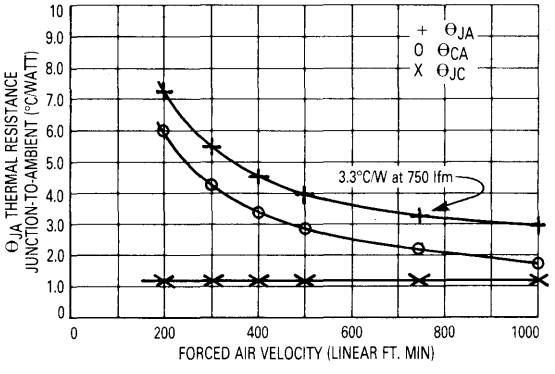


FIGURE 12 — CONSTRUCTION PROFILE

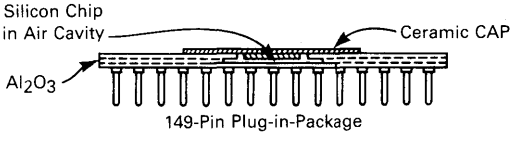
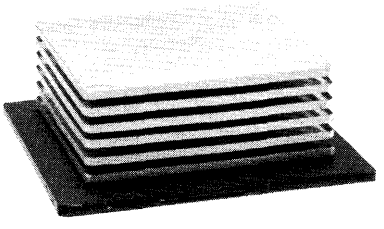
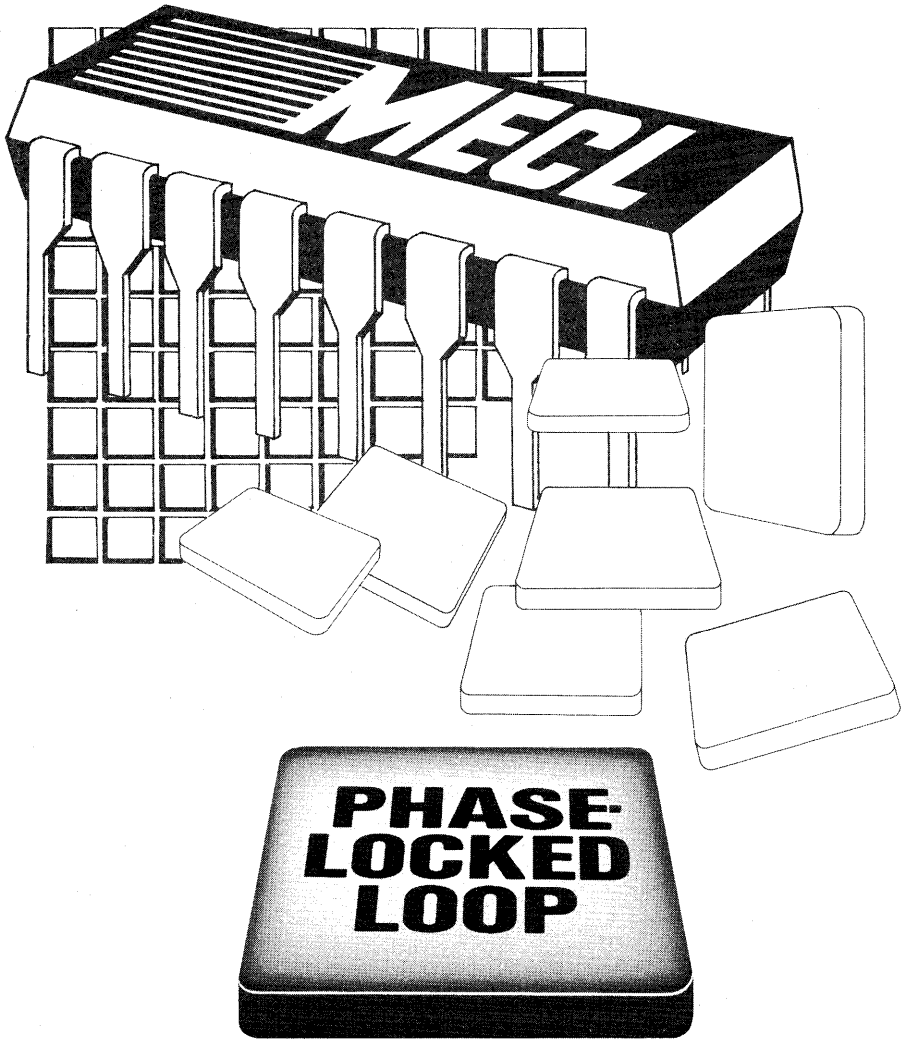


FIGURE 13 — PROTOTYPE HEAT SINK



*Heat Sink — 6 plates 1.25 X 1.25 X 0.04 inches spaced 0.0625 inch apart, mounted on 0.5 inch diameter spindle — omnidirectional.

6


MECL
PHASE-
LOCKED
LOOP

PHASE-LOCKED LOOP INTEGRATED CIRCUITS

Motorola offers the designer an array of devices to perform phase-locked loop functions, such as phase detectors, dividers, and oscillators. These devices include MECL, linear, TTL and CMOS technologies covered both in this data book and in other Motorola literature.

Detailed specification of these devices may be obtained from Motorola sales offices or authorized distributors.

Function	Family	Devices		Case
		-55 to +125°C	0 to +75°C	
Combination Functions				
Frequency Synthesizer	CMOS[2]	—	MC145104	620, 648
Frequency Synthesizer	CMOS	—	MC145106	680, 707
Frequency Synthesizer	CMOS	—	MC145107	620, 648
Frequency Synthesizer	CMOS	—	MC145109	620, 648
Frequency Synthesizer	CMOS	—	MC145112	680, 707
Frequency Synthesizer	CMOS	—	MC145143	620, 648
Frequency Synthesizer	CMOS	—	MC145144	680, 707
Frequency Synthesizer	CMOS	—	MC145145	680, 707
Frequency Synthesizer	CMOS	—	MC145146	729, 738
Frequency Synthesizer	CMOS	—	MC145151	719, 710
Frequency Synthesizer	CMOS	—	MC145152	733, 710
Frequency Synthesizer	CMOS	—	MC145155	680, 707
Frequency Synthesizer	CMOS	—	MC145156	729, 738
Frequency Synthesizer	CMOS	—	MC145157	—
Frequency Synthesizer	CMOS	—	MC145158	—
Frequency Synthesizer	CMOS	—	MC145159	—
Phase Comp/Prog. Counter	CMOS	MC14568BA	MC14568BC	620, 648
Phase Comp/VCO	CMOS	MC14046BA	MC14046BC	620, 648
Phase-Locked Loop	Linear	—	NE565N	646
Oscillators				
Crystal Oscillator	MECL	MC12561	MC12061	620, 648
Voltage-Controlled Oscillator	MECL	MC1648M	MC1648#	632, 646
Voltage-Controlled Multivibrator	MECL	—	MC1658#	620, 648
Dual Voltage-Controlled Multivibrator	TTL	MC4324	MC4024	632, 646, 607
Voltage-Controlled Oscillator	TTL/LS	—	SN74LS724	626
Phase Detectors				
Digital				
Digital Mixer	MECL	—	MC12000	632, 646
Phase-Frequency Detector	MECL	MC12540	MC12040	632, 646
Phase-Frequency Detector	TTL	MC4344	MC4044	632, 646, 607
Analog				
Analog Mixer — Double Balanced	MECL	MC12502	MC12002#	632, 646
Modulator/Demodulator	Linear	MC1594	MC1494	632, 646
Modulator/Demodulator	Linear	MC1595	MC1495	632, 646
Modulator/Demodulator	Linear	MC1596	MC1496	632, 646
Control Functions				
Counter-Control Logic	MECL	MC12514	MC12014	620, 648

Notes:
* To be introduced.
#T_A = -30°C to +85°C.
A = Announced.
[1] Plastic package available for commerical temperature range only.
[2] All CMOS devices are -40°C to +85°C.

7

Function	Family	Devices		Case
		-55 to +125°C	0 to +75°C	
Prescalers/Counters				
UHF Prescaler (÷2)	MECL	—	MC1690#	626, 693
÷4 Counter, 1.0 GHz	MECL	—	MC1697	620
÷4 Counter, 1.0 GHz	MECL	—	MC1699#	620, 648
Two-Modulus ÷5/÷6, 600 MHz Typ	MECL	MC12509	MC12009#	620, 648
Two-Modulus ÷8/÷9, 600 MHz Typ	MECL	MC12511	MC12011#	620, 648
Two-Modulus ÷10/÷11, 600 MHz Typ	MECL	MC12513	MC12013#	620, 648
Two-Modulus ÷32/÷33, 225 MHz	MECL	—	MC12015##	626
Two-Modulus ÷40/÷41, 225 MHz	MECL	—	MC12016##	626
Two-Modulus ÷64/÷65, 225 MHz	MECL	—	MC12017##	626
Low-Power Two-Modulus ÷128/÷129, 520 MHz	MECL	—	MC12018##	626
Low-Power Two-Modulus ÷20/÷21, 225 MHz	MECL	—	MC12019##	626
Low-Power Two-Modulus ÷128/÷129, 1.0 GHz	MECL	—	MC12022##	626
Low-Power ÷64 Prescaler, 225 MHz, 3.2 to 5.5 V_{CC}	MECL	—	MC12023	626
VHF/UHF ÷64/÷256	MECL	—	MC12071	626
Low-Power ÷64 Prescaler, 1.1 GHz	MECL	—	MC12073	626
Low-Power ÷256 Prescaler, 1.1 GHz	MECL	—	MC12074	626
UHF Prescaler (÷2), 750 MHz	MECL	—	MC12090	626
Programmable ÷N Decade[3]	TTL	MC4316	MC4016	620, 648, 650
Programmable ÷N (÷0 - 1, ÷0 - 4)	TTL	MC4317	MC4017	620, 648, 650
Programmable ÷N Hexadecimal[4]	TTL	MC4018	MC4318	620, 648, 650
Programmable ÷N (÷0 - 3, ÷0 - 3)	TTL	MC4319	MC4019	620, 648, 650
Programmable ÷N Decade	TTL/LS	SN54LS716	SN74LS716	620, 648
Programmable ÷N Binary	TTL/LS	SN54LS718	SN74LS718	620, 648

Notes:
#T_A = -30°C to +85°C.
##T_A = -40°C to +85°C.
[3] SN74LS716 is TTL/LS version of MC4016.
[4] SN74LS718 is TTL/LS version of MC4018.

† PLL = Phase-Locked Loop indicates that no external synthesizer would be required to implement Electronic Tuning Systems.
** Temperature to be determined.
TBD = To be determined.

MOTOROLA

MC4316 • MC4016
MC4317 • MC4017
MC4318 • MC4018
MC4319 • MC4019

PROGRAMMABLE MODULO-N COUNTERS

The monolithic devices are programmable, cascadable, modulo-N-counters. The MC4316/4016 can be programmed to divide by any number (N) from 0 thru 9, the MC4318/4018 from 0 thru 15. The MC4317/4017 consists of a modulo 2 counter which can be programmed to divide by 0 or 1 and a modulo 5 counter which can be programmed to divide by any number from 0 to 4. The MC4319/4019 contains two modulo 4 counters which can be programmed to divide by any number from 0 to 3.

The parallel enable ($\overline{PE}$) input enables the parallel data inputs D0 thru D3. All zeros are entered into the counter by applying a logic "0" level to the master reset ($\overline{MR}$) and $\overline{PE}$ inputs. This causes the counter to stop counting (count = 0). All data inputs are independent of the logic level of the Clock.

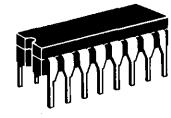
Modulo-N counters are useful in frequency synthesizers, in phase-locked loops, and in other applications where a simple method for frequency division is needed.

All Types:

Input Loading Factor:
Clock, $\overline{PE}$ = 2
D0, D1, D2, D3, Gate = 1
$\overline{MR}$ = 4
Output Loading Factor = 8

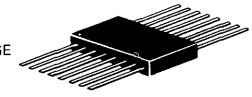
Total Power Dissipation = 250 mW typ/pkg
Propagation Delay Time:
Clock to Q3 = 50 ns typ
Clock to Bus = 35 ns typ

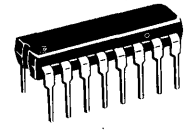
PROGRAMMABLE MODULO-N COUNTERS



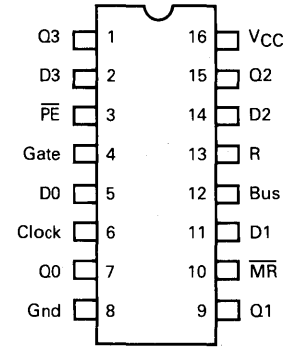
L SUFFIX
CERAMIC PACKAGE
CASE 620

F SUFFIX
CERAMIC PACKAGE
CASE 650





P SUFFIX
PLASTIC PACKAGE
CASE 648



MC4316/4016
MC4318/4018

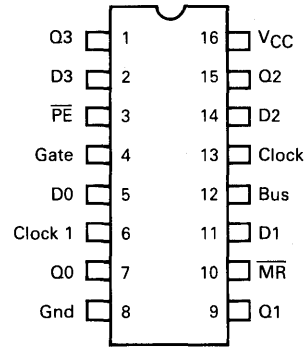
V_{CC} = Pin 16
Gnd = Pin 8

MC4316/4016

COUNT	OUTPUT			
	Q3	Q2	Q1	Q0
9	1	0	0	1
8	1	0	0	0
7	0	1	1	1
6	0	1	1	0
5	0	1	0	1
4	0	1	0	0
3	0	0	1	1
2	0	0	1	0
1	0	0	0	1
0	0	0	0	0

MC4318/4018

COUNT	OUTPUT			
	Q3	Q2	Q1	Q0
15	1	1	1	1
14	1	1	1	0
13	1	1	0	1
12	1	1	0	0
11	1	0	1	1
10	1	0	1	0
9	1	0	0	1
8	1	0	0	0
7	0	1	1	1
6	0	1	1	0
5	0	1	0	1
4	0	1	0	0
3	0	0	1	1
2	0	0	1	0
1	0	0	0	1
0	0	0	0	0



MC4317/4017
MC4319/4019

V_{CC} = Pin 16
Gnd = Pin 8

MC4317/4017

COUNT	OUTPUT
	Q0
1	1
0	0

MC4319/4019

COUNT	OUTPUT	
	Q1	Q0
3	1	1
2	1	0
1	0	1
0	0	0

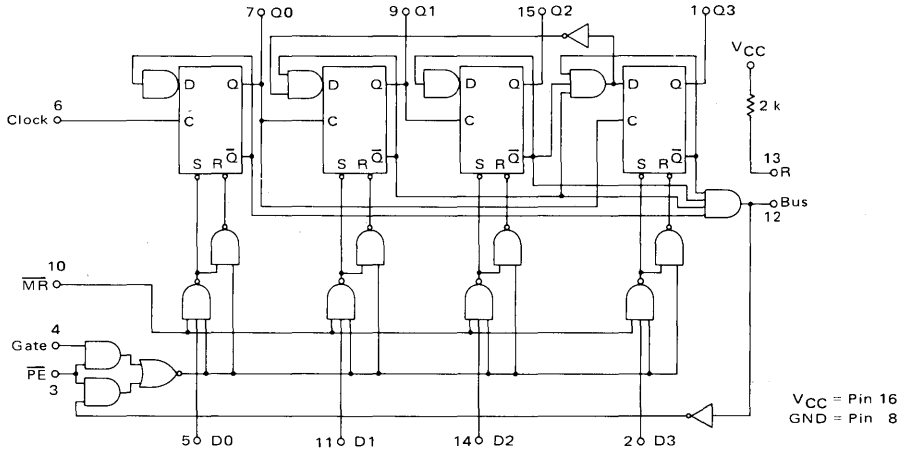
COUNT	OUTPUT		
	Q3	Q2	Q1
4	1	0	0
3	0	1	1
2	0	1	0
1	0	0	1
0	0	0	0

COUNT	OUTPUT	
	Q3	Q2
3	1	1
2	1	0
1	0	1
0	0	0

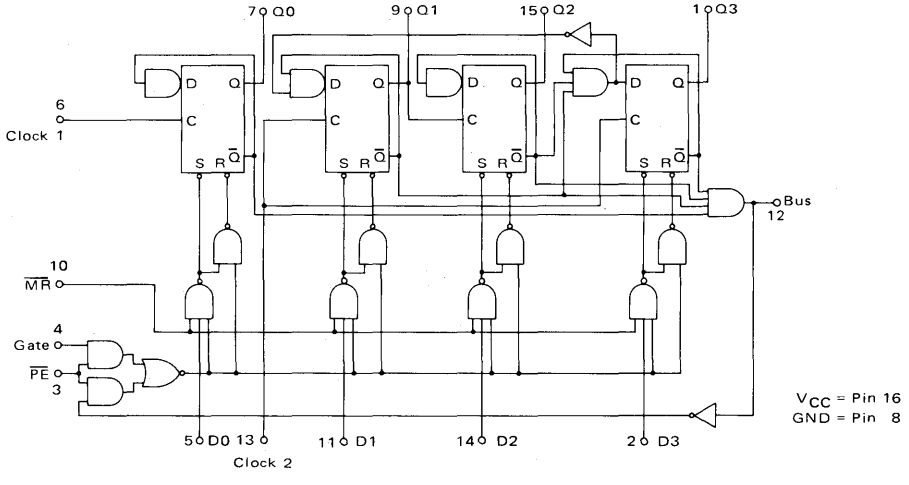
7

LOGIC DIAGRAMS

MC4316/4016

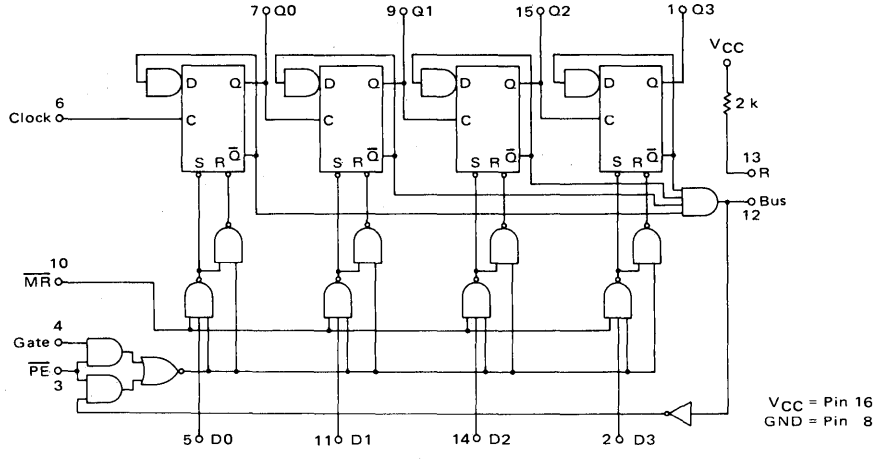


MC4317/4017

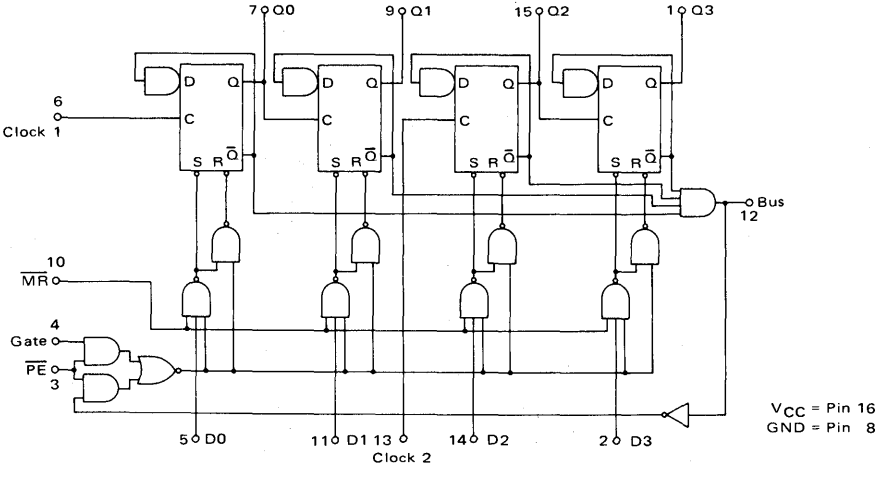


LOGIC DIAGRAMS (continued)

MC4318/4018



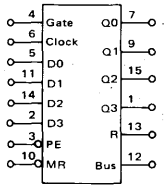
MC4319/4019



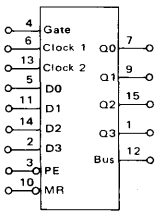
ELECTRICAL CHARACTERISTICS

Tests are shown for one output only.
Others are tested in the same manner.

MC4316/4016
MC4318/4018



MC4317/4017
MC4319/4019

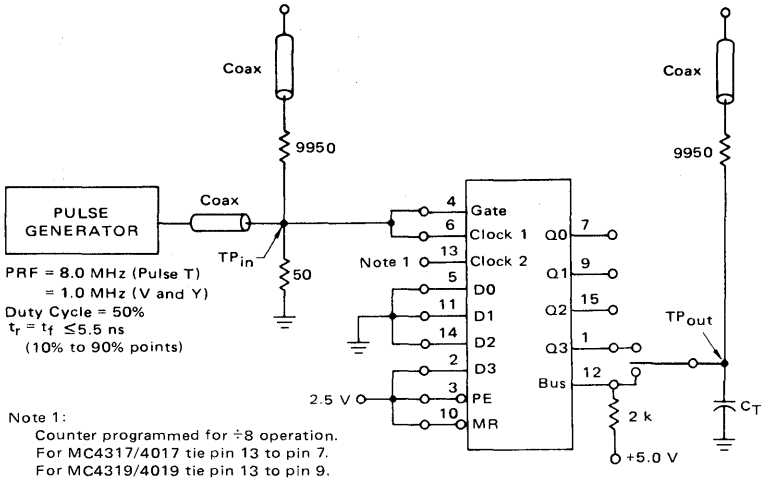


	@ Test Temperature	TEST CURRENT/VOLTAGE VALUES mA I_{OL1}	I_{OL2}	I_{OL3}	I_{OH}	I_{IC}	Volts V_{IL}	V_{IH}	V_{IHH}	V_{ILT}	V_{IHT}	V_{CC}	V_{CCL}	V_{CCH}
MC4316–4019	-55°C	12.8	13.8	9.6	-1.6	–	0.4	2.4	5.5	0.8	2.0	5.0	4.5	5.5
	+25°C	12.8	13.8	9.6	-1.6	-10	0.4	2.4	5.5	0.8	2.0	5.0	4.5	5.5
	+125°C	12.8	13.8	9.6	-1.6	–	0.4	2.4	5.5	0.8	2.0	5.0	4.5	5.5
MC4016–4019	0°C	12.8	13.8	9.6	-1.6	–	0.4	2.5	5.5	0.8	2.0	5.0	4.75	5.25
	+25°C	12.8	13.8	9.6	-1.6	-10	0.4	2.5	5.5	0.8	2.0	5.0	4.75	5.25
	+75°C	12.8	13.8	9.6	-1.6	–	0.4	2.5	5.5	0.8	2.0	5.0	4.75	5.25

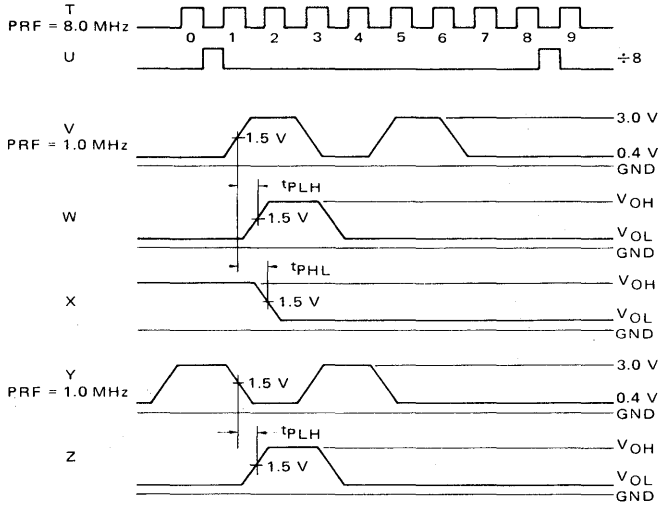
Characteristic	Symbol	Pin Under Test	MC4316–4319 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	MC4016–4019 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL1}	I_{OL2}	I_{OL3}	I_{OH}	I_{IC}	V_{IL}	V_{IH}	V_{IHH}	V_{ILT}	V_{IHT}	V_{CC}	V_{CCL}	V_{CCH}	Gnd
Input																												
Forward Current	I_{IL1}	2	–	-1.6	–	-1.6	–	-1.6	–	-1.6	–	-1.6	–	-1.6	mAdc	–	–	–	–	–	2	10	–	–	–	–	–	16	3,8
		3	–	-3.2	–	-3.2	–	-3.2	–	-3.2	–	-3.2	–	-3.2		–	–	–	–	–	3	4	–	–	–	–	–		8,12
		4	–	-1.6	–	-1.6	–	-1.6	–	-1.6	–	-1.6	–	-1.6		–	–	–	–	–	4	3	–	–	–	–	–		8
		5	–	-1.6	–	-1.6	–	-1.6	–	-1.6	–	-1.6	–	-1.6		–	–	–	–	–	5	10	–	–	–	–	–		3,8
		6	–	-3.2	–	-3.2	–	-3.2	–	-3.2	–	-3.2	–	-3.2		–	–	–	–	–	6	–	–	–	–	–	–		8
		10	–	-6.4	–	-6.4	–	-6.4	–	-6.4	–	-6.4	–	-6.4		–	–	–	–	–	10	2,5,11,14	–	–	–	–	–		3,8
		11	–	-1.6	–	-1.6	–	-1.6	–	-1.6	–	-1.6	–	-1.6		–	–	–	–	–	11	10	–	–	–	–	–		
		14	–	-1.6	–	-1.6	–	-1.6	–	-1.6	–	-1.6	–	-1.6		–	–	–	–	–	14	10	–	–	–	–	–		
	I_{IL2}	2	–	-1.4	–	-1.4	–	-1.4	–	-1.4	–	-1.4	–	-1.4	mAdc	–	–	–	–	–	2	10	–	–	–	–	16		3,8
		3	–	-2.8	–	-2.8	–	-2.8	–	-2.8	–	-2.8	–	-2.8		–	–	–	–	–	3	4	–	–	–	–			8,12
		4	–	-1.4	–	-1.4	–	-1.4	–	-1.4	–	-1.4	–	-1.4		–	–	–	–	–	4	3	–	–	–	–			8
		5	–	-1.4	–	-1.4	–	-1.4	–	-1.4	–	-1.4	–	-1.4		–	–	–	–	–	5	10	–	–	–	–			3,8
		6*	–	-2.8	–	-2.8	–	-2.8	–	-2.8	–	-2.8	–	-2.8		–	–	–	–	–	6	–	–	–	–	–			8
		10	–	-5.6	–	-5.6	–	-5.6	–	-5.6	–	-5.6	–	-5.6		–	–	–	–	–	10	2,5,11,14	–	–	–	–			3,8
		11	–	-1.4	–	-1.4	–	-1.4	–	-1.4	–	-1.4	–	-1.4		–	–	–	–	–	11	10	–	–	–	–			
		14	–	-1.4	–	-1.4	–	-1.4	–	-1.4	–	-1.4	–	-1.4		–	–	–	–	–	14	10	–	–	–	–			
Leakage Current	I_{IH}	2	–	40	–	40	–	40	–	40	–	40	–	40	μAdc	–	–	–	–	–	–	2	–	–	–	–	16		8,10
		3	–	80	–	80	–	80	–	80	–	80	–	80		–	–	–	–	–	–	3	–	–	–	–			4,8
		4	–	40	–	40	–	40	–	40	–	40	–	40		–	–	–	–	–	–	4	–	–	–	–			3,8
		5	–	40	–	40	–	40	–	40	–	40	–	40		–	–	–	–	–	–	5	–	–	–	–			8,10
		6	–	80	–	80	–	80	–	80	–	80	–	80		–	–	–	–	–	–	6	–	–	–	–			8
		10	–	160	–	160	–	160	–	160	–	160	–	160		–	–	–	–	–	–	10	–	–	–	–			2,5,8,11,14
		11	–	40	–	40	–	40	–	40	–	40	–	40		–	–	–	–	–	–	11	–	–	–	–			8,10
		14	–	40	–	40	–	40	–	40	–	40	–	40		–	–	–	–	–	–	14	–	–	–	–			8,10
	I_{IHH}	2	1.0	–	1.0	–	1.0	–	1.0	–	1.0	–	1.0	–	mAdc	–	–	–	–	–	–	–	2	–	–	–	–	16		8,10
		3		–		–		–		–		–		–		–	–	–	–	–	–	–	3	–	–	–	–			4,8
		4		–		–		–		–		–		–		–	–	–	–	–	–	–	4	–	–	–	–			3,8
		5		–		–		–		–		–		–		–	–	–	–	–	–	–	5	–	–	–	–			8,10
		6		–		–		–		–		–		–		–	–	–	–	–	–	–	6	–	–	–	–			8
		10		–		–		–		–		–		–		–	–	–	–	–	–	–	10	–	–	–	–			2,5,8,11,14
		11		–		–		–		–		–		–		–	–	–	–	–	–	–	11	–	–	–	–			8,10
		14		–		–		–		–		–		–		–	–	–	–	–	–	–	14	–	–	–	–			8,10
Clamp Voltage	V_{IC}	2**	–	–	–	-1.5	–	–	–	–	–	-1.5	–	–	Vdc	–	–	–	–	2	–	–	–	–	–	–	16	–	8
Output																												
Output Voltage	V_{OL}	1	–	0.4	–	0.4	–	0.4	–	0.4	–	0.4	–	0.4	Vdc	1	–	–	–	–	–	–	–	2,3,5,11,14	–		16		8
		1	–	0.4	–	0.4	–	0.4	–	0.4	–	0.4	–	0.4		–	1	–	–	–	–	–	–	2,3,5,11,14	–			16	
		12	–	0.5	–	0.5	–	0.5	–	0.5	–	0.5	–	0.5		–	–	12	–	–	–	–	–	3	2,5,11,14		16		
	V_{OH}	1	2.4	–	2.4	–	2.4	–	2.5	–	2.5	–	2.5	–	Vdc	–	–	–	1	–	–	–	–	3	2,5,11,14	–	16		8
Short-Circuit Current	I_{OS}	1	-20	-65	-20	-65	-20	-65	-20	-65	-20	-65	-20	-65	mAdc	–	–	–	–	–	3	2,5,11,14	–	–	–	16	–	–	1,8
		13#	-1.8	-3.8	-1.8	-3.8	-1.8	-3.8	-1.8	-3.8	-1.8	-3.8	-1.8	-3.8	mAdc	–	–	–	–	–	–	–	–	–	–	16	–	–	8,13
Power Requirements (Total Device)																												
Power Supply Drain	I_{CC}	16	–	–	–	65	–	–	–	–	–	65	–	–	mAdc	–	–	–	–	–	–	–	–	–	–	16	–	–	8

*For MC4317/4017 and MC4319/4019 also test pin 13 using the same procedure except V_{IL} applied to pin 13.
**Test all inputs in the same manner.
#Test applies only to MC4316/4016 and MC4318/4018.

SWITCHING TIME TEST CIRCUIT AND VOLTAGE WAVEFORMS



Note 1:
Counter programmed for ÷8 operation.
For MC4317/4017 tie pin 13 to pin 7.
For MC4319/4019 tie pin 13 to pin 9.
(For MC4316/4016 and MC4318/4018, pin 13 is the resistor pin, and left open.)



SWITCHING TIME TEST PROCEDURES (T_A = 25°C)

(Letters shown in test columns refer to waveforms.)

TEST	SYMBOL	INPUT				OUTPUT		LIMITS		
		Clock Pin 6	Gate Pin 4	D0, D1, D2 Pins 5,11,14	D3,$\overline{PE}$, $\overline{MR}$ Pins 2,3,10	Bus Pin 12	Q3 Pin 1	Min	Max	Unit
Toggle Frequency (Check before measuring propagation delay.)	f_{tog}	T	T	Gnd	2.5 V	–	U	8.0	–	MHz
Propagation Delay Clock to Bus	t_{PLH}	V	V	Gnd	2.5 V	W	–	–	65	ns
Propagation Delay Gate to Q3	t_{PLH}	Y	Y	Gnd	2.5 V	–	Z	–	35	ns
Propagation Delay Clock 1 to Q3 MC4316, 17/4016, 17	t_{PHL}	V	V	Gnd	2.5 V	–	X	–	45	ns
MC4318, 19/4018, 19								–	78	ns

7

OPERATING CHARACTERISTICS

MC4316/4016, MC4318/4018

Operation of both counters is essentially the same. The MC4316/4016 has a maximum modulus of ten while the MC4318/4018 is capable of dividing by up to sixteen. Minor differences in the programming procedure will be covered in the discussion of cascaded stages.

Suitable connections for operating a single stage are shown in Figure 1, as well as appropriate waveforms. The desired modulus is applied to the data inputs D0, D1, D2, and D3 in binary (MC4018) or binary coded decimal (MC4016) positive logic format. If a number greater than nine (BCD 1001) is applied to the MC4016, it treats the most significant bit position as a zero; if for example, binary fourteen (1110) were applied to an MC4016, the counter would divide by six. BCD eight is programmed in Figure 1. As $\overline{PE}$ is taken low the states on the parallel inputs are transferred to their respective outputs. Subsequent positive transitions of the input clock will decrement the counter until the all zero state is detected by the bus gate. The resulting positive transition of the bus line is internally inverted and fed back to the preset gating circuitry but does not yet preset the counter since the gateclock input is still high. As the clock returns to the low state the counter is set to the programmed state, taking the bus line low. The net result is one positive pulse on the bus line for every N clock pulses. The output pulse width is approximately equal to one clock pulse high time.

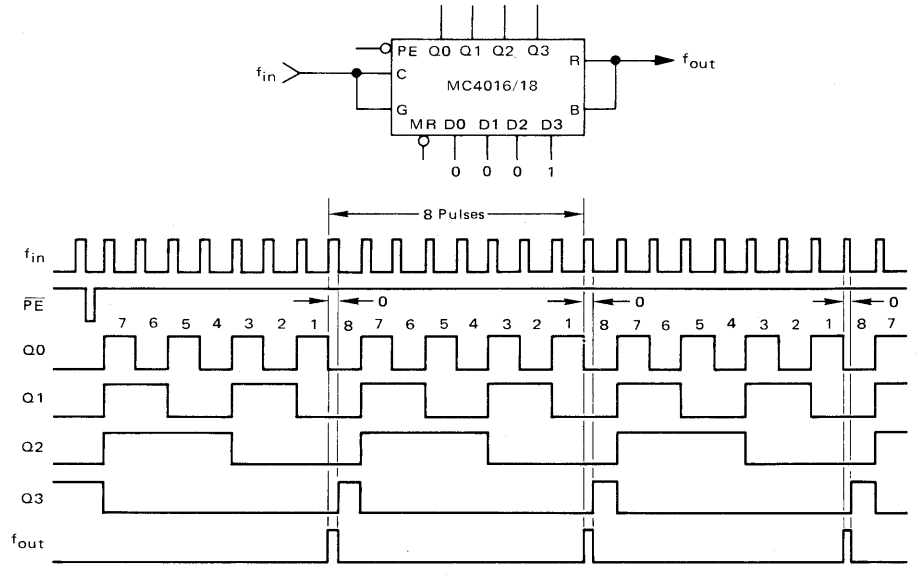
Operation will continue in this fashion until the data on the programmable inputs is changed. Since the preset circuitry is inhibited except when the counter is in the zero state, preset data may be changed while clocking is occurring. If it is necessary to enter a new number before the counter has reached zero this can be done by momentarily taking $\overline{PE}$ low. Countdown will continue from the new number on the next positive clock transition.

The counters can be made to divide by 10 (MC4016) or 16 (MC4018) by inhibiting the preset logic. This may be done by either holding the gate input high or by holding the bus line low.

The normal connections for cascading stages are indicated in Figure 2, with the appropriate waveforms. Note that the gate input of each stage is connected to the clock; all bus outputs are tied to one of the internal pullup resistors, R. The total modulus for cascaded MC4016s is determined from $N_T = N_0 + 10N_1 + 100N_2 + \ldots$; N_T for MC4018s is given by $N_T = N_0 + 16N_1 + 256N_2 + \ldots$ Stated another way, the BCD equivalent of each decimal digit is applied to respective MC4016 stages while the data inputs of the MC4018 stages are treated as part of one long binary number. The difference in programming is illustrated in Figure 2 where $N_T = 245$ is coded for both counter types.

Cascaded operation can be further clarified by referring to the timing diagram of Figure 2. For the MC4016, counting begins with the first positive clock transition after the data has been set in. After the five clock pulses, the least-significant stage has been counted down to zero. The bus line does not go high at this time since the three bus terminals are wire-ORed and the other two stages are not in the zero state. Since no reset occurs, the next positive

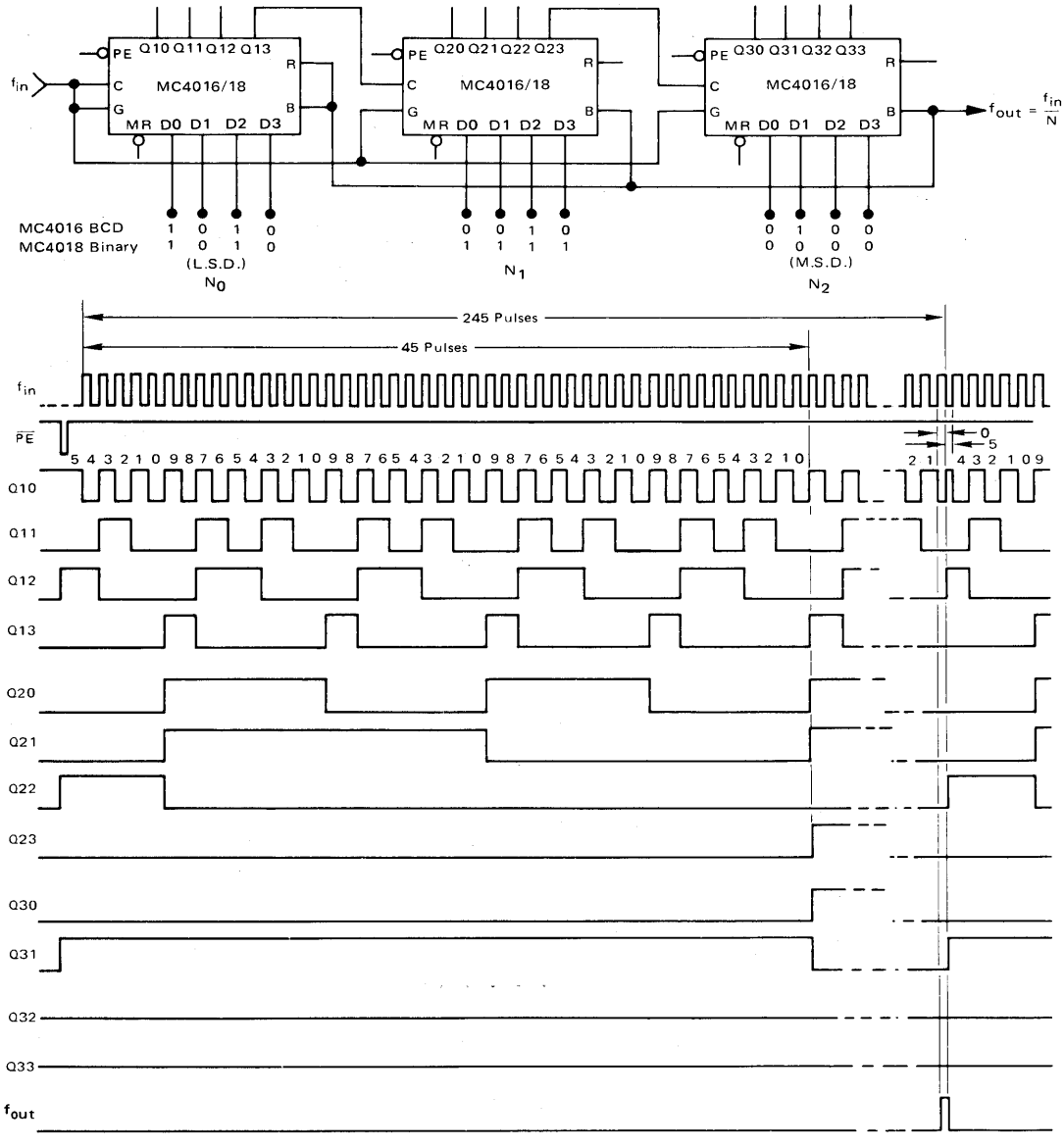
FIGURE 1 — SINGLE-STAGE OPERATION



OPERATING CHARACTERISTICS: MC4316/4016, MC4318/4018

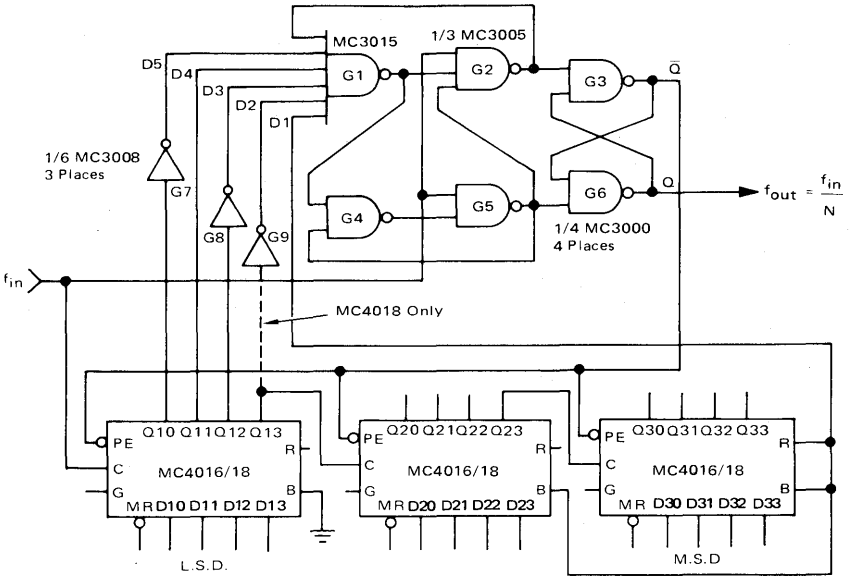
clock edge advances the least significant stage to the nine (1001) state, causing the second stage to be decremented. The process continues in this manner with the least significant stage now dividing by ten. The second stage eventually counts down to zero and also reverts to dividing by ten. Each pulse out of the second stage decrements the third until it reaches zero. At this time the bus line goes high; it remains high until the clock goes low, causing all three stages to be reset to the programmed count again.

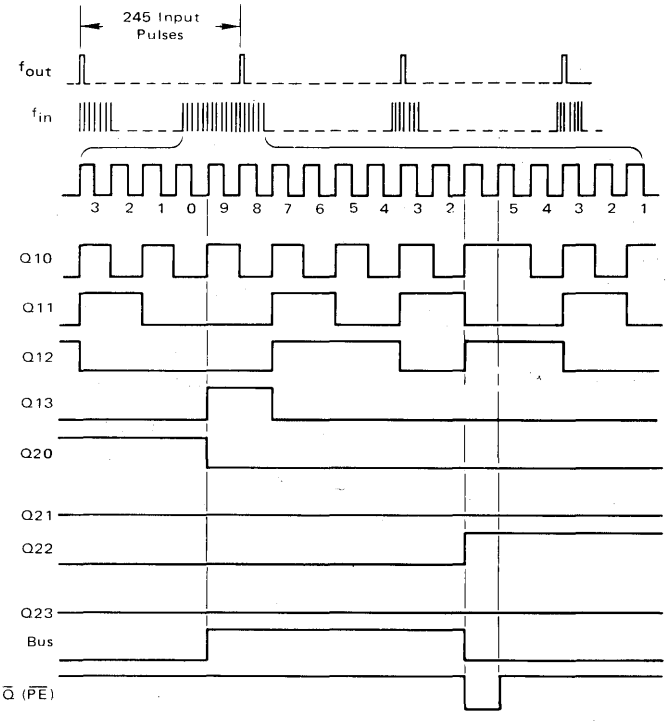
FIGURE 2 — CASCADED OPERATION



OPERATING CHARACTERISTICS: MC4316/4016, MC4318/4018

FIGURE 3 – INCREASING OPERATING RANGE





7

OPERATING CHARACTERISTICS: MC4316/4016, MC4318/4018

Maximum operating frequency of the basic MC4016/4018 counter is limited by the time required for reprogramming at the end of each count down cycle. Operation can be extended to approximately 25 MHz by adding an "early decode" feature as shown in Figure 3. The appropriate connections for three stages are shown; however up to eight stages can be satisfactorily cascaded. Note the following differences between this and the non-extended method: the counter gate inputs are not connected to the input clock; all Parallel Enables are connected to the $\overline{Q}$ output of a type D flip-flop formed by gates G1 through G6; the bus terminal of the least significant stage is grounded; all other bus terminals and one internal resistor, R, are connected together and serve as a data input to the flip-flop. Four additional data inputs are provided for decoding the "two" state of the least significant stage. Circuit operation is illustrated in the waveforms of Figure 3 where the timing for the end of a count-down cycle is shown in expanded form. The counter parallel inputs are assumed to have N = 245 applied. Timing is not shown for the third stage since it has already been counted down to the all zero state. As the next-to-least significant stage reaches zero, the common bus line goes high. Count down of the least significant stage continues until the "two" state is reached. This condition causes the remaining D inputs to the flip-flop to be high. The next-to-last clock pulse of the cycle then triggers the flip-flop Q output high. $\overline{Q}$ simultaneously takes the parallel enable of all stages low, resetting the programmed data to the outputs. The next input pulse clocks Q (f_{out}) back to the zero state since the data inputs to the flip-flop are no longer all high. The positive output pulse is one input clock period in duration. Note that division by N equal to 1 or 2 is not available using this method.

OPERATING CHARACTERISTICS

MC4317/4017, MC4319/4019

The MC4317/4017 consists of a modulo 2 and a modulo 5 programmable counter. The MC4319/4019 contains two modulo 4 programmable counters. Both parts are implemented in the same manner as the MC4316/4016 and MC4318/4018, however in these devices the output of the appropriate flip-flop is disconnected from the input of the next flip-flop. This input is then brought out as the second clock input for the package (see logic diagrams on page 2 of this data sheet). The resistor existing on the MC4316/4016 and MC4318/4018 is eliminated on the MC4317/4017 and MC4319/4019 in order not to exceed 16 pins. Elimination of the resistor causes no problems because only one resistor is required per divider chain and these parts will normally be used with the MC4316/4016 and/or MC4318/4018. In applications where the parts are used alone, an external resistor is connected to the bus output.

To operate the MC4317/4017 as a modulo 2 programmable counter, the modulo 5 programmable counter must be disabled by programming it to zero (D1, D2, and D3 grounded). Likewise, to use the device as a modulo 5 programmable counter the modulo 2 counter must be disabled (D0 grounded). Operation of the MC4319/4019 is similar in that the modulo 4 counter not being used must be disabled by programming it to zero (D0 thru D1 grounded or D2 and D3 grounded).

When cascading packages for large divide ratios, the most significant Q output of the modulo counter being used provides the input for the next package and all bus outputs are tied together. This method of connection is the same as for the MC4316/4016 and MC4318/4018.

The MC4317/4017 and MC4319/4019 can be made to perform the same function as the MC4316/4016 and MC4318/4018, respectively, by externally connecting the last Q output of one counter to the clock input of the other counter and programming inputs in the normal manner.

7

APPLICATIONS INFORMATION

A typical system application for programmable counters is illustrated in the frequency synthesizer shown in Figure 4. There the counter provides a means of digitally selecting some integral multiple of a stable reference frequency. The circuit phase locks the output, f_{VCO}, of a voltage controlled oscillator to a reference frequency, f_{ref}.[1] Circuit operation is such that $f_{VCO} = Nf_{ref}$, where N is the divider ratio of the feedback counter.

In many synthesizer applications the VCO is operated at VHF frequencies too high for direct division by TTL counters. In these cases the VCO output is usually prescaled by using a suitable fixed divide-by-M ECL circuit as shown in Figure 5. For this configuration, $f_{VCO} = NMf_{ref}$, where N is variable (programmable) and M is fixed. Design of the optimum loop filter requires that the input reference frequency be as high as possible where

FIGURE 4 — MTTL PHASE-LOCKED LOOP

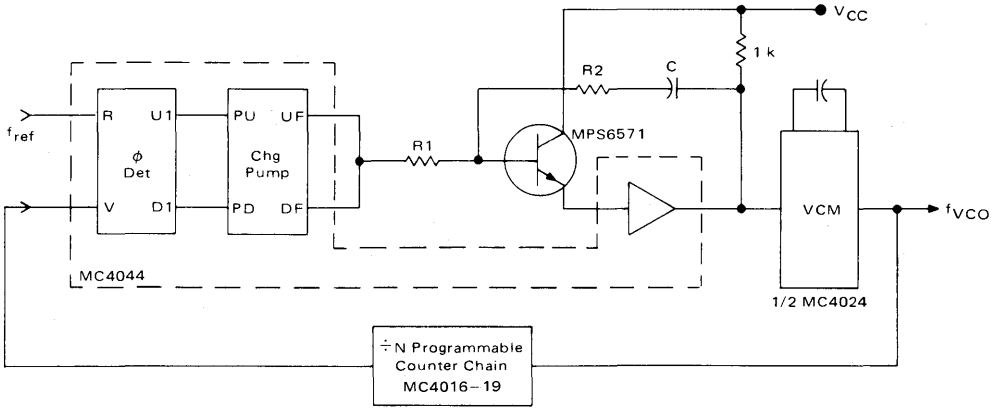
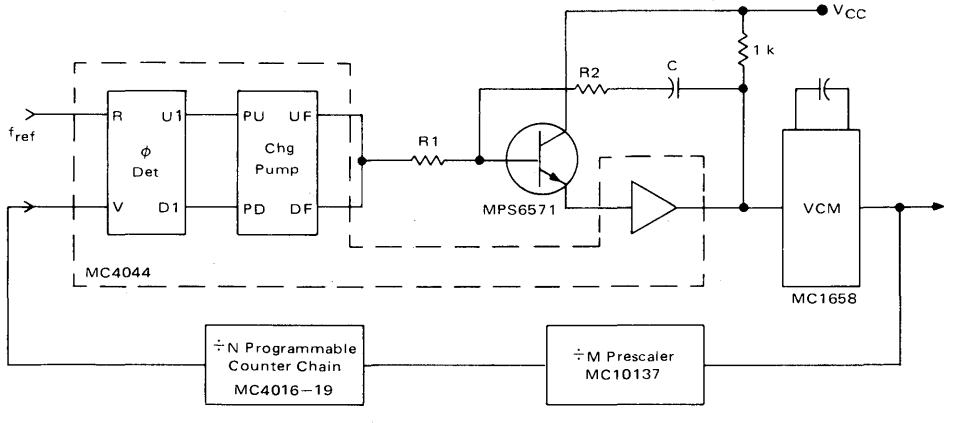


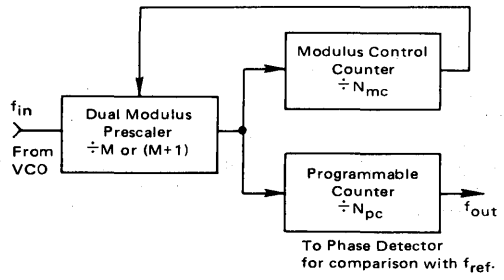
FIGURE 5 — MTTL-MECL PHASE-LOCKED LOOP



1 See Motorola Application Note AN-535 and the MC4344/4044 Data Sheet for detailed explanation of overall circuit operation.

7

FIGURE 6 — FEEDBACK COUNTERS WITH DUAL MODULUS PRESCALER



the upper limit is established by the required channel spacing. Since $f_{VCO} = Nf_{ref}$ in the non-prescaled case, if N is changed by one, the VCO output changes by f_{ref}, or the synthesizer channel spacing is just equal to f_{ref}. When the prescaler is used as in Figure 5, $f_{VCO} = NMf_{ref}$, and a change of one in N results in the VCO changing by Mf_{ref}, i.e., if f_{ref} is set equal to the minimum permissible channel spacing as is desirable, then only every M channels in a given band can be selected. One solution is to set f_{ref} = channel spacing/M but this leads to more stringent loop filter requirements.

An alternate approach that avoids this problem is provided by the counter configuration shown in Figure 6.[2] It too uses a prescaler ahead of a programmable counter, however the modulus of the prescaler is now controlled by a third counter, causing it to alternate between M and M + 1. Operation is best explained by assuming that all three counters have been set for the beginning of a cycle: the prescaler for division by (M + 1), the modulus control counter for division by N_{mc}, and the programmable counter for division by N_{pc}. The prescaler will divide by (M + 1) until the modulus control counter has counted down to zero; at this time, the all zero state is detected and causes the prescaler to divide by M until the programmable counter has also counted down to zero. When this occurs, a cycle is complete and each counter is reset to its original modulus in readiness for the next cycle. For this configuration,

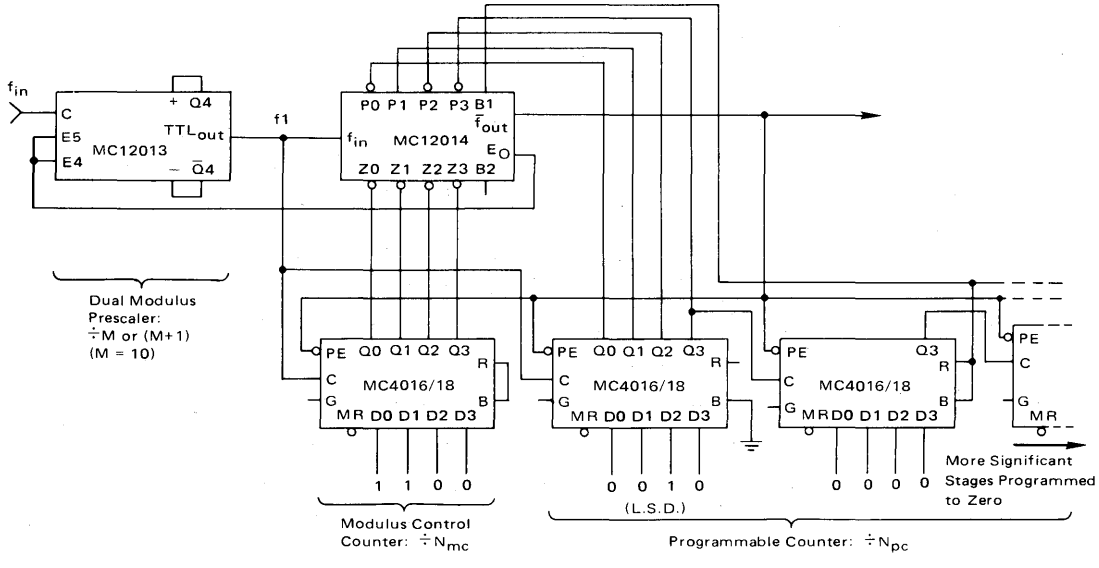
$$f_{out} = \frac{f_{in}}{MN_{pc} + N_{mc}}$$

In terms of the synthesizer application, $f_{VCO} = (MN_{pc} + N_{mc})f_{ref}$ and channels can be selected every f_{ref} by letting N_{pc} and N_{mc} take on suitable integer values, including zero.

A simplified example of this technique is shown in Figure 7. The MC12013 Dual Modulus Prescaler divides by either 10 or 11 when connected as shown in Figure 7. If the E3 and E4 Enable inputs are high at the start of a prescaler cycle, division by 10 results; if the Enable inputs are low at the beginning of the cycle, division by 11 results. The zero detection circuitry of the MC12014 Counter Control Logic is connected to monitor the outputs of the modulus control counter; this provides a suitable enable signal at E0 as the modulus control counter reaches its terminal (zero) count. The remainder of the MC12014 is connected to extend the operating frequency of the programmable counter chain.

A specific example of this technique is shown in Figure 8. There the feedback divider circuitry required for generating frequencies between 144 MHz and 178 MHz with 30 kHz channel spacing is shown.[2]

FIGURE 7 — FREQUENCY DIVISION: $f_O = f_{in}/MN_{pc} + N_{mc}$



2. This application is discussed in greater detail in the MC12014 Counter Control Logic data sheet.

FIGURE 8 – 144 TO 178 MHz FREQUENCY SYNTHESIZER
WITH 30 kHz CHANNEL SPACING

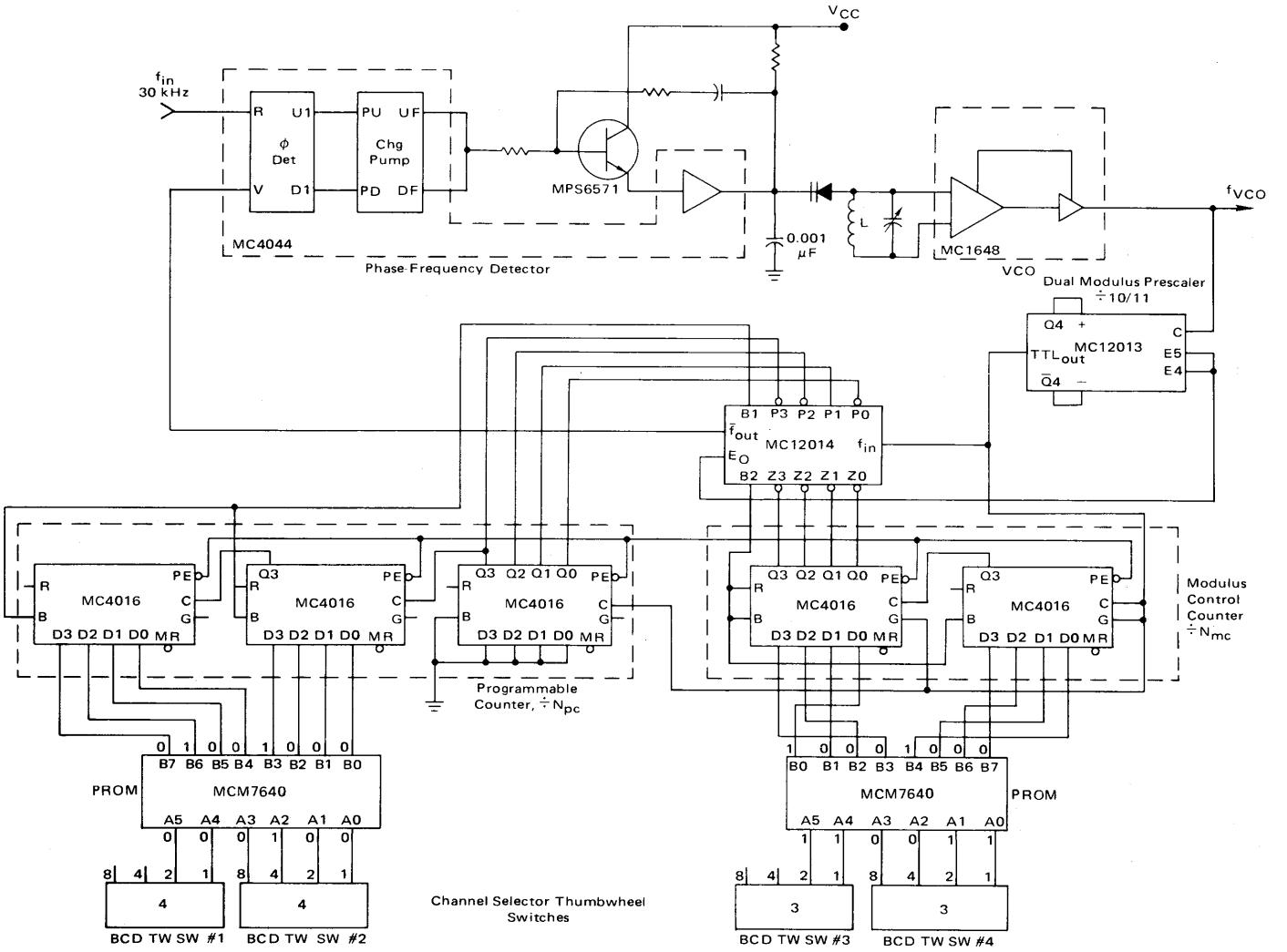
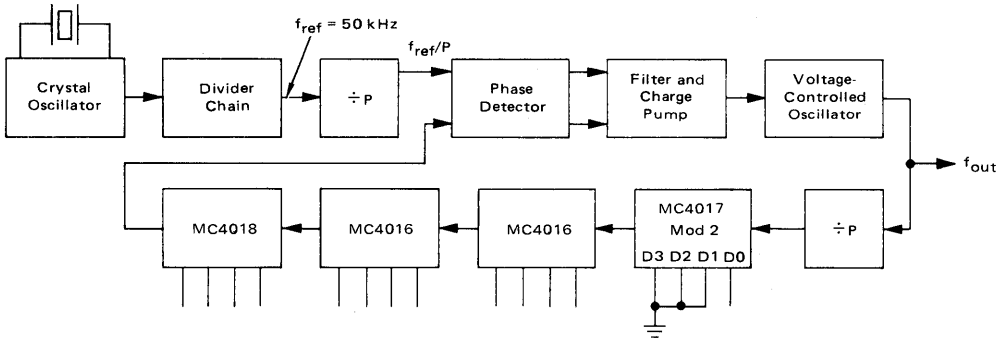


Figure 9 shows a frequency synthesizer system for the aircraft band of 108 to 136 MHz with a channel spacing of 50 kHz. The use of the MC4017 as a modulo 2 programmable counter is shown in Figure 9A, while Figure 9B shows the same system implemented using the MC4016. For a system of this type it is desirable to use direct-reading thumbwheel switches for channel selection. To implement this system with these constraints, it is necessary to calculate the required reference frequency (f_{ref}). Using the equations in Figure 9A, the required reference is 50 kHz and N4 must be programmed to 0 and 1. Figure 9B requires a reference frequency of 10 kHz and N4 must be programmed to only 0 and 5.

For any phase-locked loop system it is desirable to maintain as high a reference frequency as possible while meeting the system requirements. The higher the reference frequency, the higher the number of sampling pulses received by the phase detector per unit time. This results in (1) easier filtering of the control voltage, (2) faster lock-up time, and (3) less noise in the output spectrum. The higher reference frequency is also desirable because the reference frequency appears as sidebands on the output frequency and the farther the sidebands are away from the output the better the system. Another advantage of the higher reference frequency is the smaller divide ratio required in the programmable counter chain. This is advantageous when calculating realizable resistors for the filter. For these reasons, the system using the MC4017 is superior to the one using the MC4016.

FIGURE 9 — 108 TO 136 MHz FREQUENCY SYNTHESIZER WITH 50 kHz CHANNEL SPACING

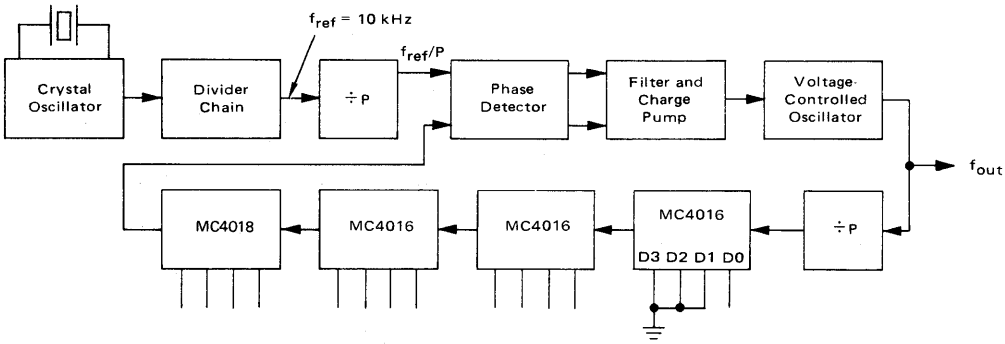
A — Using MC4017



$N = 200N_1 + 20N_2 + 2N_3 + N_4$

f_{out} = 108 to 136 MHz in 50 kHz Steps
= NP (f_{ref}/P)
= Nf_{ref}

B — Using MC4016



$N = 1000N_1 + 100N_2 + 10N_3 + N_4$

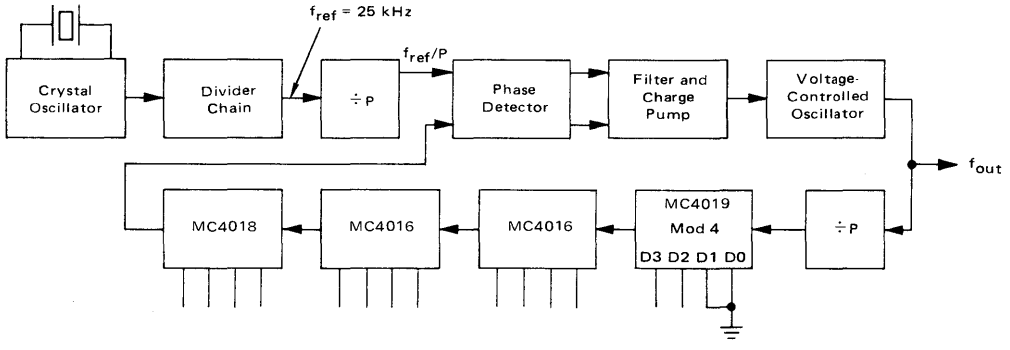
f_{out} = 108 to 136 MHz in 50 kHz Steps
= NP (f_{ref}/P)
= Nf_{ref}

7

Figure 10 shows the implementation of the aircraft band synthesizer with 25 kHz channel spacing (the 25 kHz spacing has been proposed to the FCC). The system is implemented in Figure 10A using the MC4019, and has a reference frequency of 25 kHz. Figure 10B shows the system using an MC4018 as the first counter, and has a reference frequency of 6.25 kHz to obtain the direct programming.

FIGURE 10 — 108 TO 136 MHz FREQUENCY SYNTHESIZER WITH 25 kHz CHANNEL SPACING

A — Using MC4019



10-13
10 MHz Steps
N_1

0-9
1.0 MHz Steps
N_2

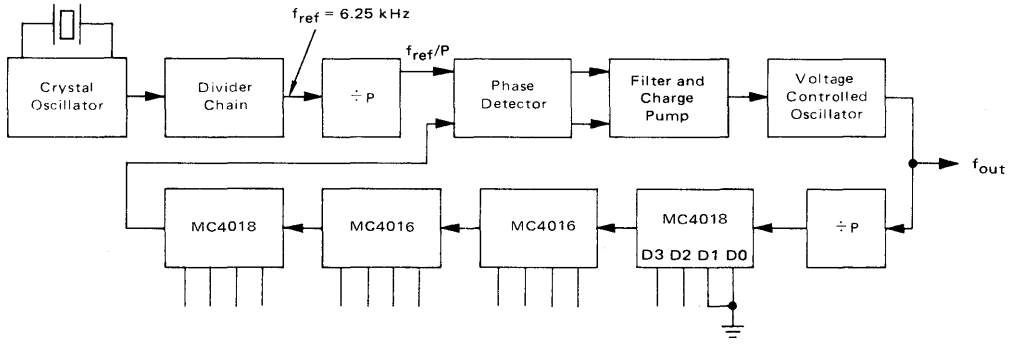
0-9
100 kHz Steps
N_3

0-4
25 kHz Steps
N_4

f_{out} = 108 to 136 MHz in 25 kHz Steps
= NP (f_{ref}/P)
= Nf_{ref}

$N = 400N_1 + 40N_2 + 4N_3 + N_4$

B — Using MC4018



10-13
6.25 MHz Steps
N_1

0-9
625 kHz Steps
N_2

0-9
62.5 kHz Steps
N_3

0,4,8,12
6.25 kHz Steps
N_4

f_{out} = 108 to 136 MHz in 25 kHz Steps
= NP (f_{ref}/P)
= Nf_{ref}

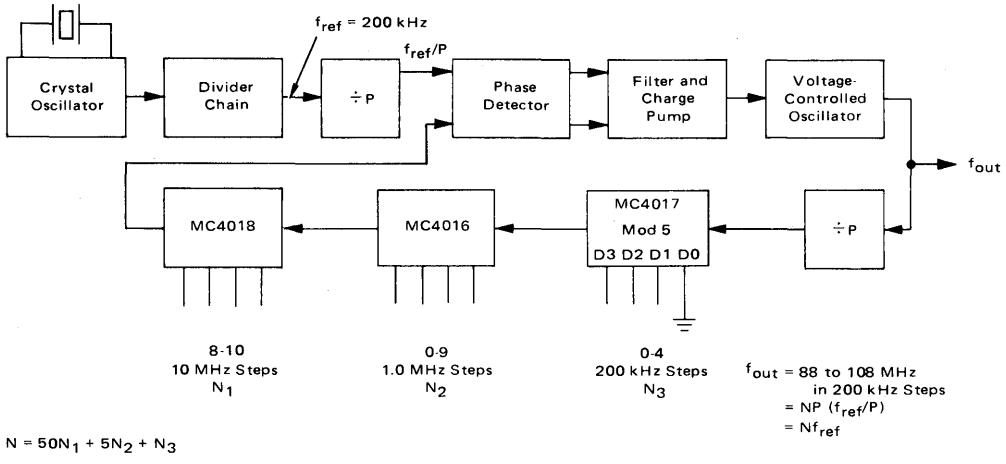
$N = 1600N_1 + 160N_2 + 16N_3 + N_4$

Figures 11A and 11B show the FM band implemented with MC4017 (used as a modulo 5 counter) and MC4016, respectively. The first system has a 200 kHz reference frequency, and the second system has a 100 kHz reference frequency. These systems using the MC4017/19 offer the same advantages over the MC4016/18 as with the aircraft band systems.

These examples illustrate the desirability of the MC4317/4017 for phase-locked loop applications where the channel spacing is 2×10^n Hz when used as a modulo 5 programmable counter, and 5×10^n Hz when used as a modulo 2 programmable counter. The MC4319/4019 is for applications with a channel spacing of 2.5×10^n Hz. The MC4316/4016 covers phase-locked loop applications where the channel spacing is 1×10^n Hz. The MC4318/4018 is used when the most significant digit is between 9 and 15.

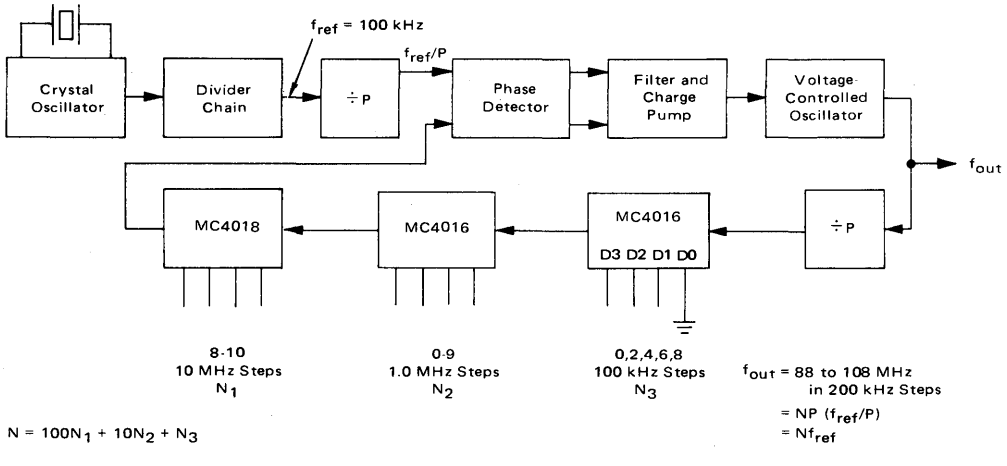
FIGURE 11 — 88 TO 108 MHz FREQUENCY SYNTHESIZER WITH 200 kHz CHANNEL SPACING

A — Using MC4017



$N = 50N_1 + 5N_2 + N_3$

B — Using MC4016



$N = 100N_1 + 10N_2 + N_3$

7

MOTOROLA

MC4324/ MC4024

DUAL VOLTAGE-CONTROLLED MULTIVIBRATOR

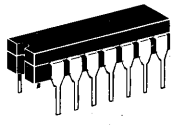
The MC4324/4024 consists of two independent voltage-controlled miltivibrators with output buffers. Variation of the output frequency over a 3.5-to-1 range is guaranteed with an input dc control voltage of 1.0 to 5.0 voltage.

Operating frequency is specified at 25 MHz at 25°C. Operation to 15 MHz is possible over the specified temperature range. For higher frequency requirements, see the MC1648 (200 MHz) or the MC1658 (125 MHz) data sheet.

This device was designed specifically for use in phase-locked loops for digital frequency control. It can also be used in other applications requiring a voltage-controlled frequency, or as a stable fixed frequency oscillator (3.0 MHz to 15 MHz) by replacing the external control capacitor with a series mode crystal.

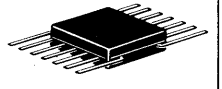
Maximum Operating Frequency = 25 MHz Guaranteed @ 25°C
Power Dissipation = 150 mW typ/pkg
Output Loading Factor = 7

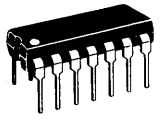
DUAL VOLTAGE-CONTROLLED MULTIVIBRATOR



L SUFFIX
CERAMIC PACKAGE
CASE 632
(TO-116)

F SUFFIX
CERAMIC PACKAGE
CASE 607

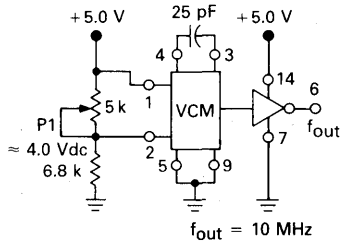




P SUFFIX
PLASTIC PACKAGE
CASE 646
(MC4024 only)

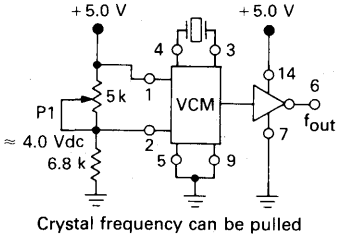
TYPICAL APPLICATIONS

FIGURE 1 — ASTABLE MULTIVIBRATOR



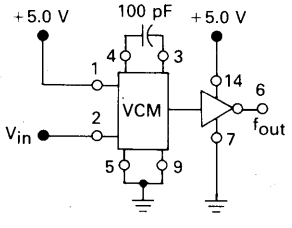
f_{out} = 10 MHz

FIGURE 2 — CRYSTAL CONTROLLED MULTIVIBRATOR



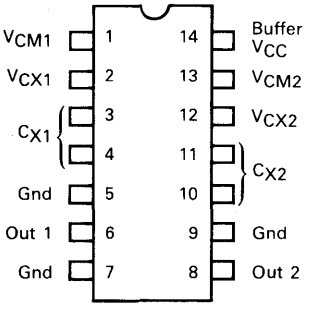
Crystal frequency can be pulled slightly by adjusting P1.

FIGURE 3 — VOLTAGE-CONTROLLED MULTIVIBRATOR



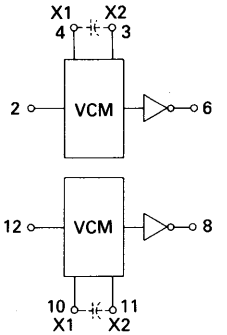
V_{in} = 2.5 V to 5.5 V
f_{out} = 1.0 MHz min, 5.0 MHz max

PIN ASSIGNMENT



7

ELECTRICAL CHARACTERISTICS

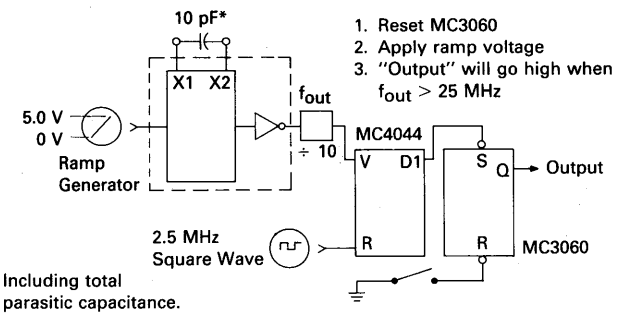


V_{CC}: VCM = 1, 13
Output Buffer = 14
Gnd: VCM = 5, 9
Output Buffer = 7
External Capacitor for
Frequency Range Determination

	@ Test Temperature	TEST CURRENT/VOLTAGE VALUES mA I_{OL1}	I_{OL2}	I_{OH}	Volts V_{IH}	V_{CC}	V_{CCL}	V_{CCH}
MC4324	−55°C	9.8	11.2	−1.6	5.0	5.0	4.5	5.5
	+25°C	9.8	11.2	−1.6	5.0	5.0	4.5	5.5
	+125°C	9.8	11.2	−1.6	5.0	5.0	4.5	5.5
MC4024	0°C	9.8	11.2	−1.6	5.0	5.0	4.75	5.25
	+25°C	9.8	11.2	−1.6	5.0	5.0	4.75	5.25
	+75°C	9.8	11.2	−1.6	5.0	5.0	4.75	5.25

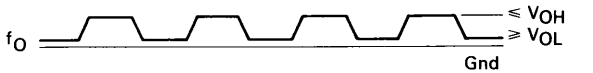
Characteristic	Symbol	Pin Under Test	MC4324 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	MC4024 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL1}	I_{OL2}	I_{OH}	V_{IH}	V_{CC}	V_{CCL}	V_{CCH}	Gnd
Input																							
Forward Current	I_{in}	2	—	100	—	100	—	100	—	100	—	100	—	100	μAdc	—	—	—	2	—	—	14	5,7,9
		12	—	100	—	100	—	100	—	100	—	100	—	100	μAdc	—	—	—	12	—	—	14	5,7,9
Output																							
Output Voltage	V_{OL}	6	—	0.4	—	0.4	—	0.4	—	0.4	—	0.4	—	0.4	Vdc	6	—	—	2	—	1,4,14	—	5,7,9
		8	—	↓	—	↓	—	↓	—	↓	—	↓	—	↓	↓	8	—	—	12	—	10,13,14	—	↓
		6	—	↓	—	↓	—	↓	—	↓	—	↓	—	↓	↓	—	6	—	2	—	—	1,4,14	
		8	—	↓	—	↓	—	↓	—	↓	—	↓	—	↓	↓	—	8	—	12	—	—	10,13,14	
	V_{OH}	6	2.4	—	2.4	—	2.4	—	2.5	—	2.5	—	2.5	—	Vdc	—	—	6	2	—	1,3,14	—	5,7,9
		8	2.4	—	2.4	—	2.4	—	2.5	—	2.5	—	2.5	—	Vdc	—	—	8	12	—	11,13,14	—	5,7,9
Short-Circuit Current	I_{OS}	6	−20	−65	−20	−65	−20	−65	−20	−65	−20	−65	−20	−65	mAdc	—	—	—	2	1,3,14	—	—	5,6,7,9
		8	−20	−65	−20	−65	−20	−65	−20	−65	−20	−65	−20	−65	mAdc	—	—	—	12	11,13,14	—	—	5,7,8,9
Power Requirements (Total Device)																							
Power Supply Drain	I_{CC}	1,3,14	—	—	—	37	—	—	—	—	—	37	—	—	mAdc	—	—	—	2,4,10,12	1,13,14	—	—	5,7,9

FIGURE 4 — AC TEST CIRCUIT AND WAVEFORMS



1. Reset MC3060
2. Apply ramp voltage
3. "Output" will go high when $f_{out} > 25$ MHz

* Including total parasitic capacitance.



(V_{CC} = 5.0 Vdc, T_A = 25°C)

TEST	SYMBOL	CONDITIONS	VALUE Min	VALUE Typ
Maximum Operating Frequency	F_{max}	C_X = 10 pF, V_{in} = 5.0 Vdc Frequency Ratio = 3.5:1	25 MHz	30 MHz
Ratio of Frequency of Oscillation Over Specified Input Voltage Range	$\frac{F_{high}}{F_{low}}$	C_X = 100 pF, V_{in} high = 5.0 Vdc, V_{in} low = 1.0 Vdc	3.5:1.0	4.5:1.0

FIGURE 5 — FREQUENCY-CAPACITANCE PRODUCT

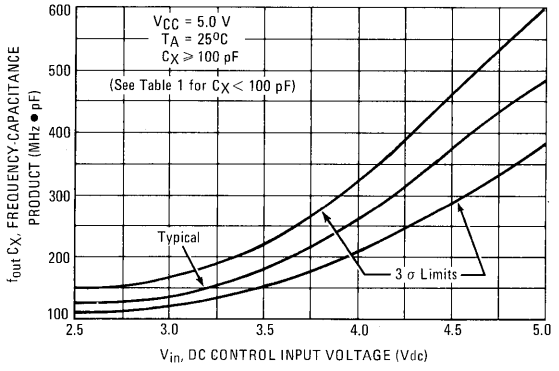


FIGURE 6 — FREQUENCY-VOLTAGE GAIN CHARACTERISTICS

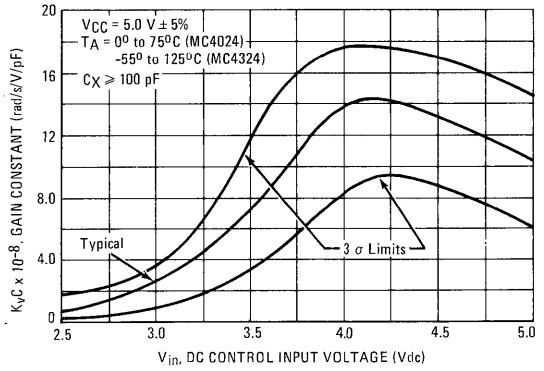


FIGURE 7 — TYPICAL FREQUENCY DEVIATION versus SUPPLY VOLTAGE

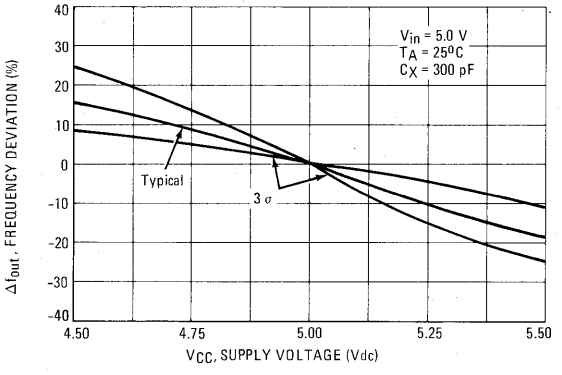


FIGURE 8 — TYPICAL FREQUENCY DEVIATION versus SUPPLY VOLTAGE

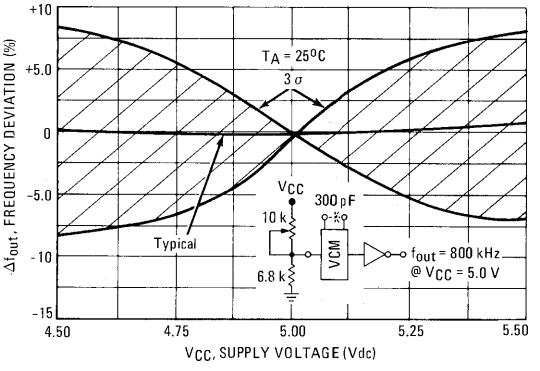


FIGURE 9 — FREQUENCY DEVIATION versus AMBIENT TEMPERATURE

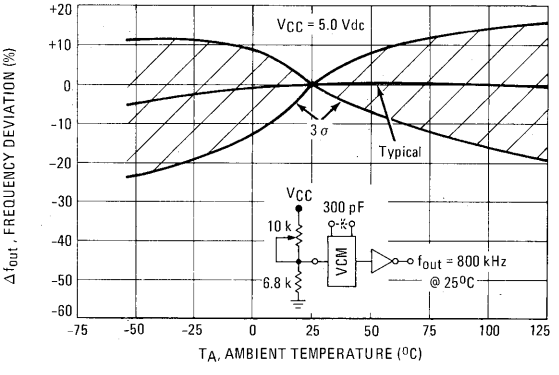
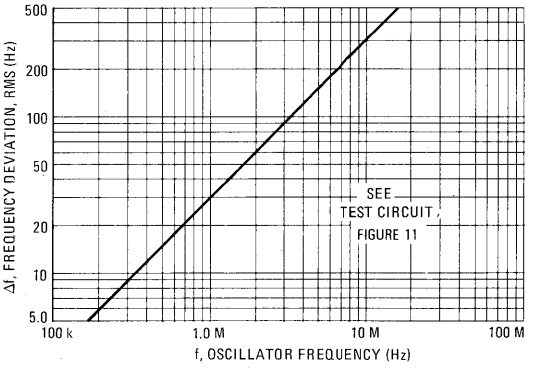
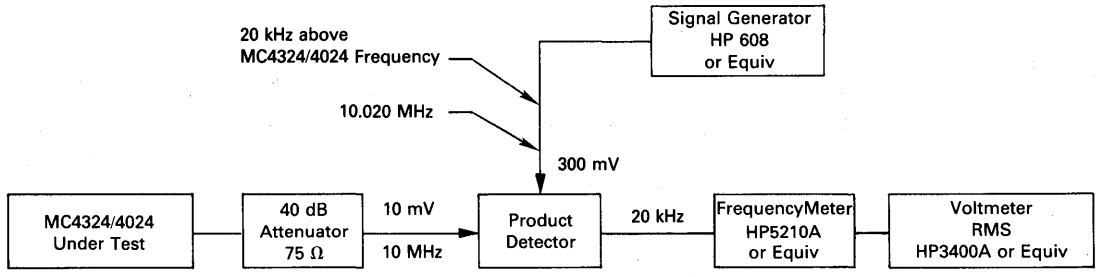


FIGURE 10 — RMS NOISE DEVIATION versus OSCILLATOR FREQUENCY



NOTE: Curves labeled as 3 σ limits denote that 99.7% of the devices tested fell within these limits.

FIGURE 11 — NOISE DEVIATION TEST CIRCUIT



$$\text{Frequency Deviation} = \frac{\text{(HP5210A output voltage) (Full Scale Frequency)}}{\text{1.0 Volt}}$$

NOTE: Frequency deviation values of either the signal generator or power supply should be determined prior to testing.

APPLICATIONS INFORMATION

Suggested Design Practices

Three power supply and three ground connections are provided in this circuit (each multivibrator has separate power supply and ground connections, and the output buffers have common power supply and ground pins). This provides isolation between VCM's and minimizes the effect of output buffer transients on the multivibrators in critical applications. The separation of power supply and ground lines also provides the capability of disabling one VCM by disconnecting its V_{CC} pin. However, all ground lines must always be connected to insure substrate grounding and proper isolation.

General design rules are:

1. Ground pins 5, 7, and 9 for all applications, including those where only one VCM is used.
2. Use capacitors with less than 50 nA leakage at plus and minus 3.0 volts. Capacitance values of 15 pF or greater are acceptable.
3. When operated in the free running mode, the minimum voltage applied to the DC Control input should be 60% of V_{CC} for good stability. The maximum voltage at this input should be V_{CC} + 0.5 volt.
4. When used in a phase-locked loop, the filter design should have a minimum DC Control input voltage of 1.0 volt and a maximum voltage of V_{CC} + 0.5 volt. The maximum restriction may be waived if the output impedance of the driving device is such that it will not source more than 10 mA at a voltage of V_{CC} + 0.5 volt.
5. The power supply for this device should be bypassed with a good quality RF-type capacitor of 500 to 1000 pF. Bypass capacitor lead lengths should be kept as short as possible. For best results, power supply voltage should be maintained as close to +5.0 V as possible. Under no conditions should the design require operation with a power supply voltage outside the range of 5.0 volts ± 10%.

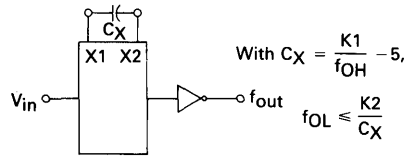
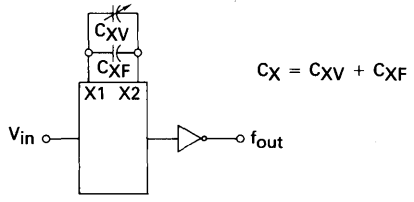
External Control Capacitor (C_X) Determination (See Table 1)

The operating frequency range of this multivibrator is controlled by the value of an external capacitor that is connected between X1 and X2. A tuning ratio of 3.5-to-1 and a maximum frequency of 25 MHz are guaranteed under ideal conditions (V_{CC} = 5.0 volts. T_A = 25°C). Under actual operating conditions, variations in supply voltage, ambient temperature, and internal component tolerances limit the tuning ratio (see Figures 7 thru 12). An improvement in tuning ratio can be achieved by providing a variable tuning capacitor to facilitate initial alignment of the circuit.

Figures 5 through 9 show typical and suggested design limit information for important VCM characteristics. The suggested design limits are based on operation over the specified temperature range with a supply voltage of 5.0 volts ± 5% unless otherwise noted. They include a safety factor of three times the estimated standard deviation.

Figures 5 and 6 provide data for any external control capacitor value greater than 100 pF. With smaller capacitor values, the curves are effectively moved downward. For example, a typical curve of frequency versus control voltage would be very nearly identical to the lower suggested design limit of Figure 5 if a 15 pF capacitor is used. To use Figure 5 divide on the ordinate by the capacitor

TABLE 1 — EXTERNAL CONTROL CAPACITOR VALUE DETERMINATION

CONFIGURATION	T_A	V_{CC}	VALUES OF K				
			K1	K2	K3	K4	K5
 With $C_X = \frac{K1}{f_{OH}} - 5$, $f_{OL} \leq \frac{K2}{C_X}$	25°C ±3°C	5.0 V	385	150	600	110	1.0
		5.0 V ±5%	325	175	680	125	1.14
		5.0 V ±10%	290	190	750	140	1.25
 $C_X = C_{XV} + C_{XF}$	0°C to 75°C	5.0 V	335	165	660	120	1.10
		5.0 V ±5%	280	190	750	140	1.25
		5.0 V ±10%	250	200	840	150	1.40
Choose C_{XF} and C_{XV} such that C_X can be adjusted to: $\frac{K1}{f_{OH}} - 5 \leq C_X \leq \frac{K3}{f_{OH}} - 5$ With $V_{in} = V_{CC} = 5.0$ V, adjust C_X to obtain: $f_{out} = K5\ (f_{OH})$ Then: $f_{OL} \leq \frac{K4}{K1} f_{OH}$	−55°C to 125°C	5.0 V	300	175	690	125	1.15
		5.0 V ±5%	260	200	780	145	1.30
		5.0 V ±10%	230	210	860	155	1.45

Definitions: f_{OH} = Output frequency with $V_{in} = V_{CC}$
f_{OL} = Output frequency with V_{in} = 2.5 V
(Frequencies in MHz, C_X in pF)

value in picofarads to obtain output frequency in megahertz. In Figure 6 the ordinate axis is multiplied by the capacitor value in picofarads to obtain the gain constant (K_V) in radians/second/volt.

Frequency Stability

When the MC4324/4024 is used as a fixed-frequency oscillator (V_{in} constant), the output frequency wll vary slightly because of internal noise. This variation is indicated by Figure 10 for the circuit of Figure 11. These variations are relatively independent (< 10%) of changes in temperature and supply voltage.

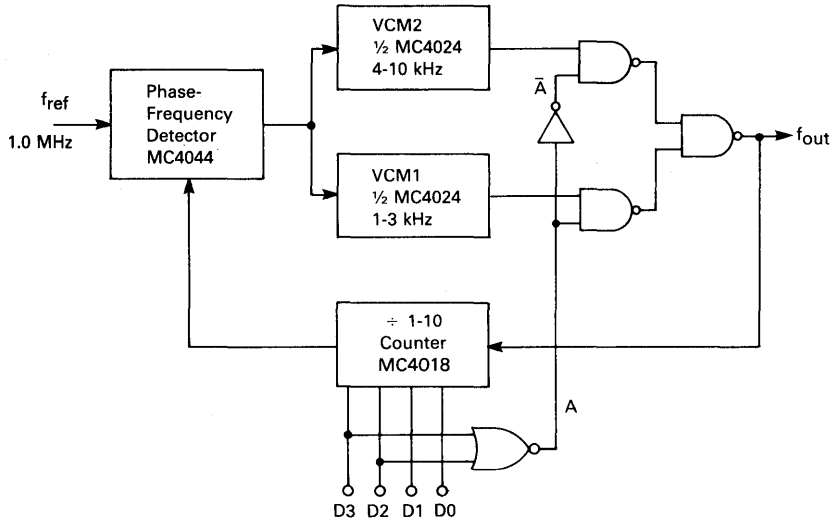
10-to-1 Frequency Synthesizer

A frequency synthesizer covering a 10-to-1 range is shown in Figure 14.Three packages are required to complete the loop: The MC4344/4044 phase-frequency detector, the MC4324/4024 dual voltage-controlled multivibrator, and the MC4318/4018 programmable counter. Two VCM's (one package) are used to obtain the required frequency range. Each VCM is capable of operating over a 3-to-1 range, thus VCM1 is used for the lower portion of the times ten range and VCM2 covers the upper end. The proper divide ratio is set into the programmable counter and the VCM for that frequency is selected by control gates. The other VCM is left to be free running since its output is gated out of the feedback path.

Normally with a single VCM the loop gain would vary over a 10-to-1 range due to the range of the counter ratios. This affects the bandwidth, lockup time, and damping ratio severely. Utilizing two VCM's reduces this change in loop gain rom 10-to-1 to 3-to-1 as a result of the different sensitivities of the two VCM's due to the different frequency ranges. This change of VCM sensitivity (3-to-1) is of such a direction of compensate for loop gain variations due to the programmable counter.

The overall concept of multi-VCM operation can be expanded for ranges greater than 10-to-1. Four VCM's (two packages) could be used to cover a 100-to-1 range.

FIGURE 12 — 10-TO-1 FREQUENCY SYNTHESIZER



÷N	Input D3	D2	D1	D0	A	VCM1 kHz	VCM2 kHz	f_{out} kHz
1	0	0	0	1	1	1	X	1
2	0	0	1	0	1	2	X	2
3	0	0	1	1	1	3	X	3
4	0	1	0	0	0	X	4	4
5	0	1	0	1	0	X	5	5
6	0	1	1	0	0	X	6	6
7	0	1	1	1	0	X	7	7
8	1	0	0	0	0	X	8	8
9	1	0	0	1	0	X	9	9
10	1	0	1	0	0	X	10	10

7

MOTOROLA

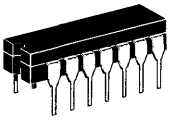
MC4344/ MC4044

PHASE-FREQUENCY DETECTOR

The MC4344/4044 consists of two digital phase detectors, a charge pump, and an amplifier. In combination with a voltage controlled multivibrator (such as the MC4324/4024 or MC1648), it is useful in a broad range of phase-locked loop applications. The circuit accepts TTL waveforms at the R and V inputs and generates an error voltage that is proportional to the frequency and/or phase difference of the input signals. Phase detector #1 is intended for use in systems requiring zero frequency and phase difference at lock. Phase detector #2 is used if quadrature lock is desired. Phase detector #2 can also be used to indicate that the main loop, utilizing phase detector #1, is out of lock.

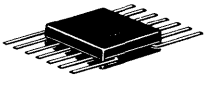
Input Loading Factor: R, V = 3
Output Loading Factor (Pin 8) = 10
Total Power Dissipation = 85 mW typ/pkg
Propagation Delay Time = 9.0 ns typ
(thru phase detector)

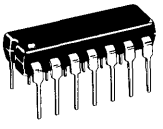
PHASE-FREQUENCY DETECTOR



L SUFFIX
CERAMIC PACKAGE
CASE 632
(TO-116)

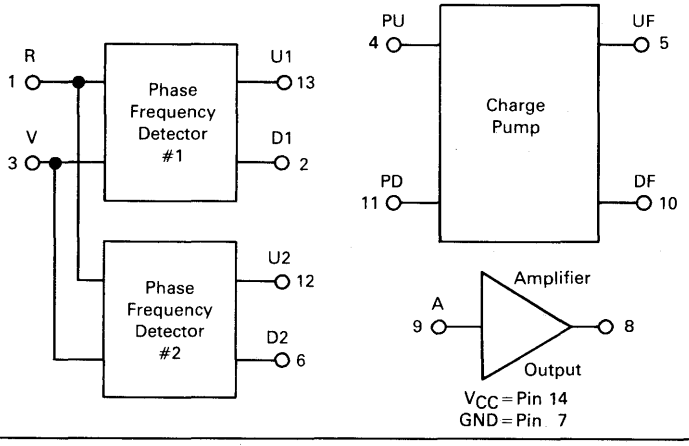
F SUFFIX
CERAMIC PACKAGE
CASE 607



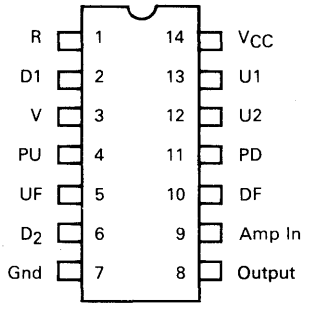


P SUFFIX
PLASTIC PACKAGE
CASE 646
MC4044 only

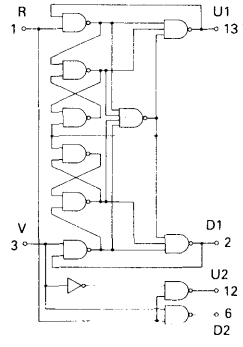
LOGIC DIAGRAM



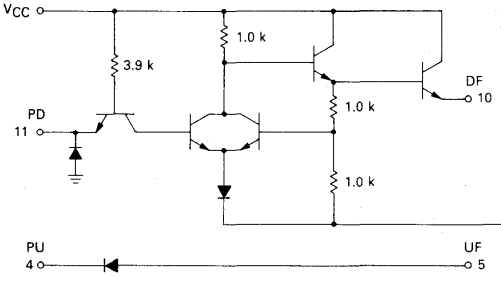
PIN ASSIGNMENT



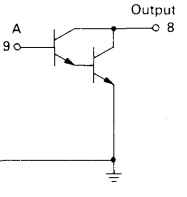
PHASE DETECTOR



CHARGE PUMP

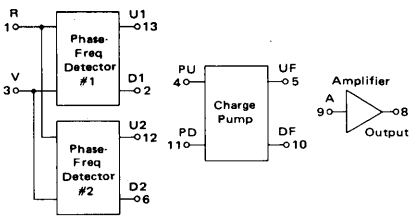


AMPLIFIER



7

ELECTRICAL CHARACTERISTICS



INPUT STATE	INPUT R	INPUT V	OUTPUT U1	OUTPUT D1	OUTPUT U2	OUTPUT D2
1	0	0	X	X	1	1
2	1	0	X	X	0	1
3	1	1	X	X	1	0
4	1	0	X	X	0	1
5	0	0	X	X	1	1
6	1	0	X	X	0	1
7	0	0	0	1	1	1
8	1	0	0	1	0	1
9	0	0	0	1	1	1
10	0	1	0	1	1	1
11	0	0	1	1	1	1
12	0	1	1	1	1	1
13	0	0	1	0	1	1
14	0	1	1	0	1	1
15	0	0	1	0	1	1
16	1	0	1	0	0	1
17	0	0	1	1	1	1

TRUTH TABLE

This is not strictly a functional truth table; i.e., it does not show all possible modes of operation. It is useful for dc testing.

1. X indicates output state unknown.
2. U1 and D1 outputs are sequential; i.e., they must be sequenced in order shown.
3. U2 and D2 outputs are combinational; i.e., they need only inputs shown to obtain outputs.

	@ Test Temperature	TEST CURRENT/VOLTAGE VALUES mA I_{OL}	I_{OH1}	I_{OH2}	I_{in}	I_{IC}	I_A	Volts V_{IL}	V_{IH}	V_{IHH}	V_{ILT}	V_{IHT}	V_{out}	V_{CC}	V_{CCL}	V_{CCH}
MC4344	-55°C	20	-1.6	-1.0	–	–	0.002	0.4	2.4	–	1.1	2.0	1.5	5.0	4.5	5.5
	+25°C	20	-1.6	-1.0	1.0	-10	0.002	0.4	2.4	5.5	1.1	1.8	1.5	5.0	4.5	5.5
	+125°C	20	-1.6	-1.0	–	–	0.002	0.4	2.4	–	0.9	1.8	1.5	5.0	4.5	5.5
MC4044	0°C	20	-1.6	-1.0	–	–	0.002	0.4	2.5	–	1.1	2.0	1.5	5.0	4.75	5.25
	+25°C	20	-1.6	-1.0	1.0	-10	0.002	0.4	2.5	5.5	1.1	1.8	1.5	5.0	4.75	5.25
	+75°C	20	-1.6	-1.0	–	–	0.002	0.4	2.5	–	0.9	1.8	1.5	5.0	4.75	5.25

Characteristic	Symbol	Pin Under Test	MC4344 Test Limits -55°C Min	-55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	MC4044 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH1}	I_{OH2}	I_{in}	I_{IC}	I_A	V_{IL}	V_{IH}	V_{IHH}	V_{ILT}	V_{IHT}	V_{out}	V_{CC}	V_{CCL}	V_{CCH}	Gnd
Input																														
Forward Current	I_{IL}	1	–	-4.8	–	-4.8	–	-4.8	–	-4.8	–	-4.8	–	-4.8	mAdc	–	–	–	–	–	–	1	–	–	–	–	–	–	–	14	7
		3	–	-4.8	–	-4.8	–	-4.8	–	-4.8	–	-4.8	–	-4.8	↓	–	–	–	–	–	–	3	–	–	–	–	–	–	–	↓	↓
		11	–	-1.6	–	-1.6	–	-1.6	–	-1.6	–	-1.6	–	-1.6		–	–	–	–	–	–	11	–	–	–	–	–	–	–		
Leakage Current	I_{IH}	1	–	120	–	120	–	120	–	120	–	120	–	120	μAdc	–	–	–	–	–	–	–	1	–	–	–	–	–	–	14	7
		3	–	120	–	120	–	120	–	120	–	120	–	120	↓	–	–	–	–	–	–	–	3	–	–	–	–	–	–	14	7
		4	–	5.0	–	5.0	–	5.0	–	5.0	–	5.0	–	5.0		–	–	–	–	–	–	–	–	–	–	–	–	–	–	4	5,7
		11	–	40	–	40	–	40	–	40	–	40	–	40		–	–	–	–	–	–	–	11	–	–	–	–	–	–	14	7
	I_{IHH}	1	–	–	–	1.0	–	–	–	–	–	1.0	–	–	mAdc	–	–	–	–	–	–	–	–	1	–	–	–	–	–	14	7
		3	–	–	–	↓	–	–	–	–	–	↓	–	–	↓	–	–	–	–	–	–	–	–	3	–	–	–	–	–	↓	↓
		11	–	–	–		–	–	–	–	–		–	–		–	–	–	–	–	–	–	–	11	–	–	–	–	–		
Clamp Voltage	V_{IC}	1	–	–	–	-1.5	–	–	–	–	–	-1.5	–	–	Vdc	–	–	–	–	1	–	–	–	–	–	–	–	–	14	–	7
		3	–	–	–	-1.5	–	–	–	–	–	-1.5	–	–	Vdc	–	–	–	–	3	–	–	–	–	–	–	–	–	14	–	7
Output (Note 1)																														
Output Voltage	V_{OH}	6	2.4	–	2.4	–	2.4	–	2.5	–	2.5	–	2.5	–	Vdc	–	6	–	–	–	–	–	–	–	1,3	–	–	14	–	7
		12	2.4	–	2.4	–	2.4	–	2.5	–	2.5	–	2.5	–	Vdc	–	12	–	–	–	–	–	–	–	1,3	–	–	14	–	7
	**		–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	3	1	–	14	–	7
	V_{OL}	6	–	0.4	–	0.4	–	0.4	–	0.4	–	0.4	–	0.4	Vdc	6	–	–	–	–	–	–	–	–	–	1,3	–	14	–	7
	V_{OH}	12	2.4	–	2.4	–	2.4	–	2.5	–	2.5	–	2.5	–	Vdc	–	12	–	–	–	–	–	–	–	–	1,3	–	14	–	7
	**		–	–	–	–	–	–	–	–	–	–	–	–	Vdc	–	–	–	–	–	–	–	–	–	3	1	–	14	–	7
	**		–	–	–	–	–	–	–	–	–	–	–	–	Vdc	–	–	–	–	–	–	–	–	–	1,3	–	–	14	–	7
	V_{OH}	6	2.4	–	2.4	–	2.4	–	2.5	–	2.5	–	2.5	–	Vdc	–	6	–	–	–	–	–	–	–	3	1	–	14	–	7
	V_{OL}	12	–	0.4	–	0.4	–	0.4	–	0.4	–	0.4	–	0.4	Vdc	12	–	–	–	–	–	–	–	–	3	1	–	14	–	7
	**		–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	1,3	–	–	14	–	7
	**		–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	3	1	–	14	–	7
	V_{OH}	2	2.4	–	2.4	–	2.4	–	2.5	–	2.5	–	2.5	–	Vdc	–	2	–	–	–	–	–	–	–	1,3	–	–	14	–	7
	V_{OL}	13	–	0.4	–	0.4	–	0.4	–	0.4	–	0.4	–	0.4	Vdc	13	–	–	–	–	–	–	–	–	1,3	–	–	14	–	7
	V_{OH}	2	2.4	–	2.4	–	2.4	–	2.5	–	2.5	–	2.5	–	Vdc	–	2	–	–	–	–	–	–	–	1	3	–	14	–	7
	V_{OL}	13	–	0.4	–	0.4	–	0.4	–	0.4	–	0.4	–	0.4	Vdc	13	–	–	–	–	–	–	–	–	1	3	–	14	–	7
	V_{OH}	2	2.4	–	2.4	–	2.4	–	2.5	–	2.5	–	2.5	–	Vdc	–	2	–	–	–	–	–	–	–	1,3	–	–	14	–	7
		13	2.4	–	2.4	–	2.4	–	2.5	–	2.5	–	2.5	–	Vdc	–	13	–	–	–	–	–	–	–	1	3	–	14	–	7
	V_{OH}	2	2.4	–	2.4	–	2.4	–	2.5	–	2.5	–	2.5	–	Vdc	–	2	–	–	–	–	–	–	–	1,3	–	–	14	–	7
		13	2.4	–	2.4	–	2.4	–	2.5	–	2.5	–	2.5	–	Vdc	–	13	–	–	–	–	–	–	–	1	3	–	14	–	7
	V_{OL}	2	–	0.4	–	0.4	–	0.4	–	0.4	–	0.4	–	0.4	Vdc	2	–	–	–	–	–	–	–	–	1,3	–	–	14	–	7
	V_{OH}	13	2.4	–	2.4	–	2.4	–	2.5	–	2.5	–	2.5	–	Vdc	–	13	–	–	–	–	–	–	–	1,3	–	–	14	–	7
	V_{OL}	2	–	0.4	–	0.4	–	0.4	–	0.4	–	0.4	–	0.4	Vdc	2	–	–	–	–	–	–	–	–	1	3	–	14	–	7
	V_{OH}	13	2.4	–	2.4	–	2.4	–	2.5	–	2.5	–	2.5	–	Vdc	–	13	–	–	–	–	–	–	–	1	3	–	14	–	7
	V_{OL}	2	–	0.4	–	0.4	–	0.4	–	0.4	–	0.4	–	0.4	Vdc	2	–	–	–	–	–	–	–	–	1,3	–	–	14	–	7
	V_{OH}	13	2.4	–	2.4	–	2.4	–	2.5	–	2.5	–	2.5	–	Vdc	–	13	–	–	–	–	–	–	–	1,3	–	–	14	–	7
	V_{OL}	2	–	0.4	–	0.4	–	0.4	–	0.4	–	0.4	–	0.4	Vdc	2	–	–	–	–	–	–	–	–	3	1	–	14	–	7
	V_{OH}	13	2.4	–	2.4	–	2.4	–	2.5	–	2.5	–	2.5	–	Vdc	–	13	–	–	–	–	–	–	–	3	1	–	14	–	7
	V_{OH}	2	2.4	–	2.4	–	2.4	–	2.5	–	2.5	–	2.5	–	Vdc	–	2	–	–	–	–	–	–	–	1,3	–	–	14	–	7
		13	2.4	–	2.4	–	2.4	–	2.5	–	2.5	–	2.5	–	Vdc	–	13	–	–	–	–	–	–	–	1,3	–	–	14	–	7
Short-Circuit Current (Note 1)	I_{OS}	* 2	-20	*-65	-20	-65	-20	-65	-20	-65	-20	-65	-20	-65	mAdc	–	–	–	–	–	–	–	–	–	–	–	14	–	–	2,3,7,1
		6	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓		–	–	–	–	–	–	–	–	–	–	–		–	–	1,3,6,7
		12														–	–	–	–	–	–	–	–	–	–	–		–	–	1,3,7,12
		* 13														–	–	–	–	–	–	–	–	–	–	–		–	–	1,3,7,13
Leakage Current (Note 1)	I_{OLK}	* 2	–	250	–	250	–	250	–	250	–	250	–	250	μAdc	–	–	–	–	–	–	–	–	–	–	–	2,14	–	–	1,3,7
		6	–	↓	–	↓	–	↓	–	↓	–	↓	–	↓	↓	–	–	–	–	–	–	–	–	–	–	–	6,14	–	–	1,3,7
		12	–		–		–		–		–		–			–	–	–	–	–	–	–	–	–	–	–	12,14	–	–	1,3,7
		* 13	–		–		–		–		–		–			–	–	–	–	–	–	–	–	–	–	–	13,14	–	–	1,3,7
Diode Voltage	V_F	5	–	–	0.5		–	–	–	–	0.5		–	–	Vdc	–	–	–	–	5	–	–	–	–	–	–	–	–	–	4,7
Output Voltage	V_{EH}	10	1.5	–	1.5	–	1.5	–	1.5	–	1.5	–	1.5	–	Vdc	–	–	10	–	–	–	–	–	–	11	–	–	14	–	7
Output Current	I_O	8	0.2	–	0.8	–	1.0	–	0.5	–	0.8	–	1.0	–	mAdc	–	–	–	–	9	–	–	–	–	–	–	–	–	8	7
Leakage Current	I_{OLK}	8	–	120	–	120	–	120	–	120	–	120	–	120	μAdc	–	–	–	–	–	–	–	–	–	–	–	–	–,	8	7,9
		10	–	5.0	–	5.0	–	5.0	–	5.0	–	5.0	–	5.0	μAdc	–	–	–	–	–	–	–	11	–	–	–	10	–	14	7
Power Requirements (Total Device) Power Supply Drain	I_{CC}	14	–	40	–	40	–	40	–	40	–	40	–	40	mAdc	–	–	–	–	–	–	–	–	–	–	–	–	14	–	7

Note 1. The output state of Pin 2 or Pin 13 depends upon the sequence that has been applied to the R and V inputs as shown in the Truth Table. In testing output voltage, the outputs of the device are tested by sequencing through the indicated input states according to the Truth Table. Procedures identified by a double asterisk (**) are necessary to change the state of the sequential logic. When testing I_{OS} and I_{OLK} on Pins 2 or 13, a single asterisk (*) indicates that the R and V inputs are sequenced per the Truth Table to input state 11 where the tests are performed. All input, power supply, and ground voltages must be maintained while sequencing and testing unless otherwise noted.

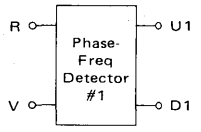
7

APPLICATION

Operation of the MC4344/4044 is best explained by initially considering each section separately. If phase detector #1 is used, loop lockup occurs when both outputs U1 and D1 remain high. This occurs only when all the negative transitions on R, the reference input, and V, the variable or feedback input, coincide. The circuit responds only to transitions, hence phase error is independent of input waveform duty cycle or amplitude variation. Phase detector #1 consists of sequential logic circuitry, therefore operation prior to lockup is determined by initial conditions.

When operation is initiated, by either applying power to the circuit or active input signals to R and V, the circuitry can be in one of several states. Given any particular starting conditions, the flow table of Figure 1 can be used to determine subsequent operation. The flow table indicates the status of U1 and D1 as the R and V inputs are varied. The numbers in the table which are in parentheses are arbitrarily assigned labels that correspond to stable states that can result for each input combination. The numbers without parentheses refer to unstable conditions. Input changes are traced by horizontal movement in the table; after each input change, circuit operation will settle in the numbered state indicated by moving horizontally to the appropriate R-V column. If the number at that location is not in parentheses, move vertically to the number of the same value that is in parentheses. For a given input pair, any one of three stable states can exist. As an example, if R = 1 and V = 0, the circuit will be in one of the stable states (4), (8), or (12).

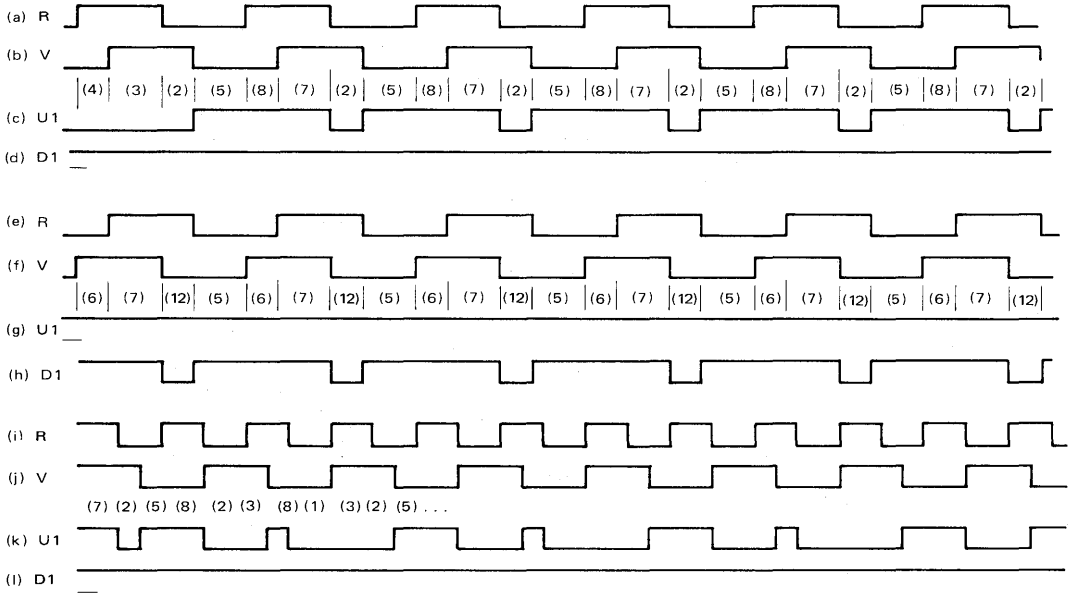
FIGURE 1 — PHASE DETECTOR #1 FLOW TABLE



R-V 0-0	R-V 0-1	R-V 1-1	R-V 1-0	U1	D1
(1)	2	3	(4)	0	1
5	(2)	(3)	8	0	1
(5)	6	7	8	1	1
9	(6)	7	12	1	1
5	2	(7)	12	1	1
1	2	7	(8)	1	1
(9)	(10)	11	12	1	0
5	6	(11)	(12)	1	0

Use of the table in determining circuit operation is illustrated in Figure 2. In the timing diagram, the input to R is the reference frequency; the input to V is the same frequency but lags in phase. Stable state (4) is arbitrarily assumed as the initial condition. From the timing diagram and flow table, when the circuit is in stable state (4), outputs U1 and D1 are "0" an "1" respectively. The next input state is R-V = 1-1; moving horizontally from stable state (4) under R-V = 1-0 to the R-V = 1-1 column, state 3 is indicated. However, this is an unstable condition and the circuit will assume the state indicated by moving vertically in the R-V = 1-1 column to stable state (3). In this

FIGURE 2 — PHASE DETECTOR #1 TIMING DIAGRAM



instance, outputs U1 and D1 remain unchanged. The input states next become R-V = 0-1; moving horizontally to the R-V = 0-1 column, stable state (2) is indicated. At this point there is still no change in U1 or D1. The next input change shifts operation to the R-V = 0-0 column where unstable state 5 is indicated. Moving vertically to stable state (5), the outputs now change state to U1-D1 = 1-1. The next input change, R-V = 1-0, drives the circuitry to stable state (8), with no change in U1 or D1. The next input, R-V = 1-1, leads to stable state (7) with no change in the outputs. The next two input state changes cause U1 to go low between the negative transitions of R and V. As the inputs continue to change, the circuitry moves repeatedly through stable states (2), (5), (8), (7), (2), etc., as shown, and a periodic waveform is obtained on the U1 terminal while D1 remains high.

A similar result is obtained if V is leading with respect to R, except that the periodic waveform now appears on D1 as shown in rows e–h of the timing diagram of Figure 2. In each case, the average value of the resulting waveform is proportional to the phase difference between the two inputs. In a closed loop application, the error signal for controlling the VCO is derived by translating and filtering these waveforms.

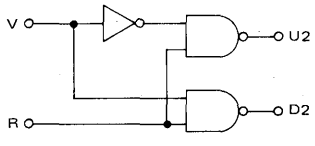
The results obtained when R and V are separated by a fixed frequency difference are indicated in rows i–l of the timing system. For this case, the U1 output goes low when R goes low and stays in that state until a negative transition on V occurs. The resulting waveform is similar to the fixed phase difference case, but now the duty cycle of the U1 waveform varies at a rate proportional to the difference frequency of the two inputs, R and V. It is this characteristic that permits the MC4344/4044 to be used as a frequency discriminator; if the signal on R has been frequency modulated and if the loop bandwidth is selected to pass the deviation frequency but reject R and V, the resulting error voltage applied to the VCO will be the recovered modulation signal.

Phase detector #2 consists only of combinatorial logic, therefore its characteristics can be determined from the simple truth table of Figure 3. Since circuit operation requires that both inputs to the charge pump either be high or have the same duty cycle when lock occurs, using this phase detector leads to a quadrature relationship between R and V. This is illustrated in rows a–d of the timing diagram of Figure 3. Note that any deviation from a fifty percent duty cycle on the inputs would appear as phase error.

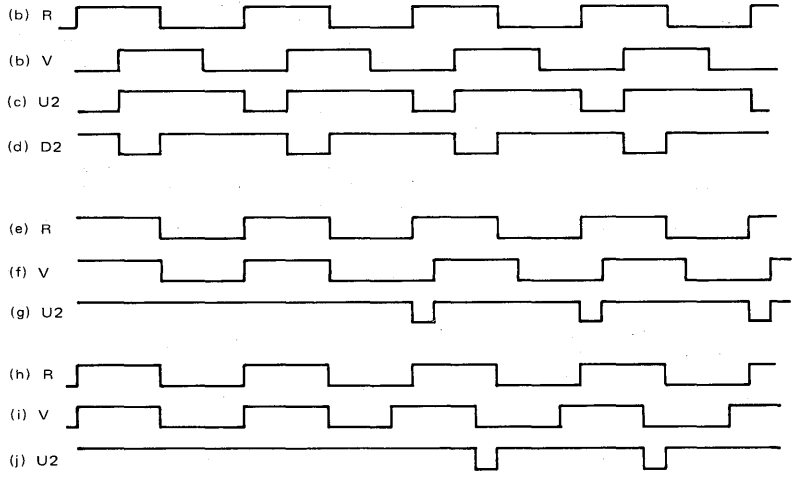
Waveforms showing the operation of phase detector #2 when phase detector #1 is being used in a closed loop are indicated in rows e–j. When the main loop is locked, U2 remains high. If the loop drifts out of lock in either direction a negative pulse whose width is proportional to the amount of drift appears on U2. This can be used to generate a simple loss-of-lock indicator.

Operation of the charge pump is best explained by considering it in conjunction with the Darlington amplifier included in the package (see Figure 4). There will be

FIGURE 3 — PHASE DETECTOR #2 OPERATION



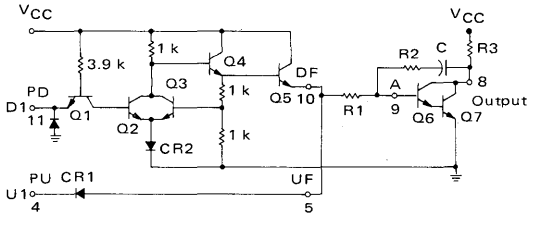
R	V	U2	D2
0	0	1	1
0	1	1	1
1	0	0	1
1	1	1	0



7

a pulsed waveform on either PD or PU, depending on the phase-frequency relationship of R and V. The charge pump serves to invert one of the input waveforms (D1) and translates the voltage levels before they are applied to the loop filter. When PD is low and PU is high, Q1 will be conducting in the normal direction and Q2 will be off. Current will be flowing through Q3 and CR2; the base of Q3 will be two V_{BE} drops above ground or approximately 1.5 volts. Since both of the resistors connected to the base of Q3 are equal, the emitter of Q4 (base of Q5) will be approximately 3.0 volts. For this condition, the emitter of Q5 (DF) will be on V_{BE} below this voltage, or about 2.25 volts. The PU input to the charge pump is high (> 2.4 volts) and CR1 will be reverse biased. Therefore Q5 will be supplying current to Q6. This will tend to lower the voltage at the collector of Q7, resulting in an error signal that lowers the VCO frequency as required by a "pump down" signal.

FIGURE 4 — CHARGE PUMP OPERATION

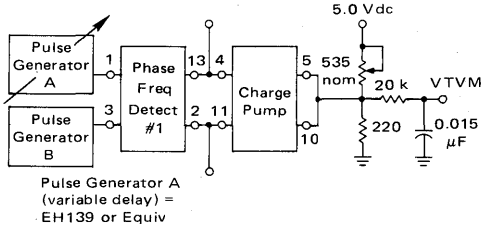


When PU is low and PD is high, CR1 is forward biased and UF will be approximately one V_{BE} above ground (neglecting the $V_{CE(sat)}$ of the driving gate). With PD high, Q1 conducts in the reverse direction, supplying base current for Q2. While Q2 is conducting, Q4 is prevented from supplying base drive to Q5; with Q5 cut off and UF low there is no base current for Q6 and the voltage at the collector of Q7 moves up, resulting in an increase in the VCO operating frequency as required by a "pump up" signal.

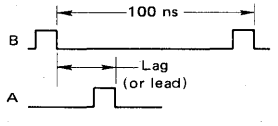
If both inputs to the charge pump are high (zero phase difference), both CR1 and the base-emitter junction of Q5 are reverse biased and there is no tendency for the error voltage to change. The output of the charge pump varies between one V_{BE} and three V_{BE} as the phase difference of R and V varies from minus 2π to plus 2π. If this signal is filtered to remove the high-frequency components, the phase detector transfer function, K_ϕ, of approximately 0.12 volt/radian is obtained (see Figure 5).

The specified gain constant of 0.12 volt/radian may not be obtained if the amplifier/filter combination is improperly designed. As indicated previously, the charge pump delivers pump commands of about 2.25 volts on the positive swings and 0.75 volt on the negative swings for a mean no-pump value of 1.5 volts. If the filter amplifier is biased to threshold "on" at 1.5 volts, then the pump up and down voltages have equal effects. The pump signals are established by V_{BE}s of transistors with milliamperes of current flowing. On the other hand, the transistors included for use as a filter amplifier will have very small currents flowing and will have correspondingly lower V_{BE}s — on the order of 0.6 volt each for a threshold of 1.2 volts. Any displacement of the threshold from 1.5 volts causes an increase in gain in one direction and a reduction in the other. The transistor configuration provided is hence not optimum but does allow for the use of an additional transistor to improve filter response. This addition also results in a non-symmetrical response since the threshold is now approximately 1.8 volts. The effective positive swing is limited to 0.45 volt while the negative swing below threshold can be greater than 1.0 volt. This means that the loop gain when changing from a high frequency to a lower frequency is less than when changing in the opposite direction. For type two loops this tends to increase overshoot when going from low to high and increases damping in the other direction. These problems and the selection of external filter components are intimately related to system requirements and are discussed in detail in the filter design section.

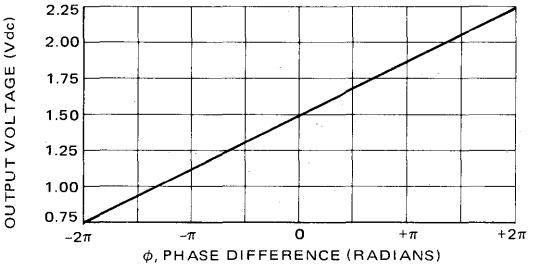
FIGURE 5 — PHASE DETECTOR TEST



Pulse Generator A (variable delay) = EH139 or Equiv



Shown for positive phase angle. Reverse A and B for negative phase angle.



PHASE-LOCKED LOOP COMPONENTS

General

A basic phase-locked loop, when operating properly, will acquire ("lock on") an input signal, track it in frequency, and exhibit a fixed phase relationship relative to the input. In this basic loop, the output frequency will be identical to the input frequency (Figure 6). A fundamental loop consists of a phase detector, amplifier/filter, and voltage-controlled oscillator (Figure 7). It appears and acts like a unity gain feedback loop. The controlled variable is phase; any error between f_{in} and f_{out} is amplified and applied to the VCO in a corrective direction.

FIGURE 6 — BASIC PHASE-LOCKED LOOP FREQUENCY RELATIONSHIP

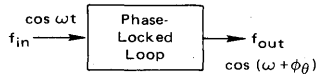
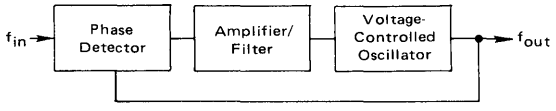


FIGURE 7 — FUNDAMENTAL PHASE-LOCKED LOOP



Simple phase detectors in digital phase-locked loops usually put out a series of pulses. The average value of these pulses is the "gain constant," K_ϕ, of the phase detector — the volts out for a given phase difference, expressed as volts/radian.

The VCO is designed so that its output frequency range is equal to or greater than the required output frequency range of the system. The ratio of change in output frequency to input control voltage is called "gain constant," K_O. If the slope of f_{out} to V_{in} is not linear (i.e., changes greater than 25%) over the expected frequency range, the curve should be piece-wise approximated and the appropriate constant applied for "best" and "worst" case analysis of loop performance.

System dynamics when in lock are determined by the amplifier/filter block. Its gain determines how much phase error exists between f_{in} and f_{out}, and filter characteristics shape the capture range and transient performance. This will be discussed in detail later.

Loop Filter

Fundamental loop characteristics such as capture range, loop bandwidth, capture time, and transient response are controlled primarily by the loop filter. The loop behavior is described by gains in each component block of Figure 8. The output to input ratio reflects a second order low pass filter in frequency response with a static gain of N:

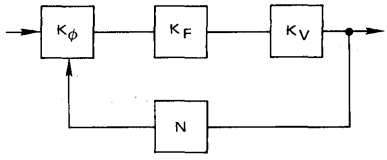
$$\frac{\theta_O(s)}{\theta_i(s)} = \frac{K_\phi K_F K_V}{s + \frac{K_\phi K_F K_V}{N}} \quad (1)$$

where: $K_F = \frac{1 + T_1 s}{T_2 s}$ (2)

$T_1 = R_2C$ and $T_2 = R_1C$ of Figure 4. Therefore,

$$\frac{\theta_O(s)}{\theta_i(s)} = \frac{N(1 + T_1 s)}{\frac{s^2 N T_2}{K_\phi K_V} + T_1 s + 1} \quad (3)$$

FIGURE 8 — GAIN CONSTANTS



K_ϕ = Phase Detector Gain (volts/radian)
K_F = Amplifier/Filter Gain
K_V = VCO Gain (radians/second/volt)
N = Integer Divisor

Both ω_n (loop bandwidth or natural frequency) and ζ (damping factor) are particularly important in the transient response to a step input of phase or frequency (Figure 9), and are defined as:

$$\omega_n = \sqrt{\frac{K_\phi K_V}{N T_2}} \quad (4)$$

$$\zeta = \sqrt{\frac{K_\phi K_V}{N T_2}}\left(\frac{T_1}{2}\right) \quad (5)$$

Using these terms in Equation 3,

$$\frac{\theta_O(s)}{\theta_i(s)} = \frac{N(1 + T_1 s)}{\frac{s^2}{\omega_n^2} + \frac{2\zeta s}{\omega_n} + 1} \quad (6)$$

In a well defined system controlling factors such as ω_n and ζ may be chosen either from a transient basis (time domain response) or steady state frequency plot (roll-off point and peaking versus frequency). Once these two design goals are defined, synthesis of the filter is relatively straight-forward.

Constants K_ϕ, K_V, and N are usually fixed due to other design constraints, leaving T_1 and T_2 as variables to set ω_n and ζ. Since only T_2 appears in Equation 4, it is the easiest to solve for initially.

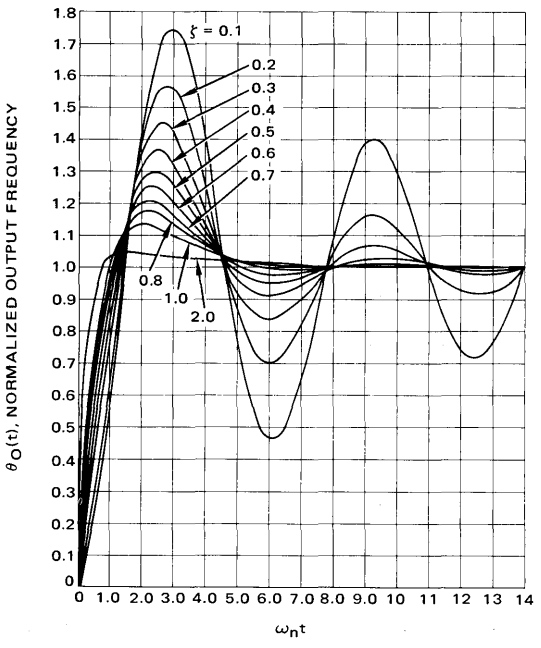
$$T_2 = \frac{K_\phi K_V}{N \omega_n^2} \quad (7)$$

From Equation 5, we find

$$T_1 = \frac{2\zeta}{\omega_n} \quad (8)$$

7

FIGURE 9 — TYPE 2 SECOND ORDER STEP RESPONSE



Using relationships 7 and 8, actual resistor values may be computed:

$$R_1 = \frac{K\phi K_V}{N\omega_n^2 C} \qquad (9)$$

$$R_2 = \frac{2\zeta}{\omega_n C} \qquad (10)$$

Although fundamentally the range of R_1 and R_2 may be from several hundred to several thousand ohms, sideband considerations usually force the value of R_1 to be set first, and then R_2 and C computed.

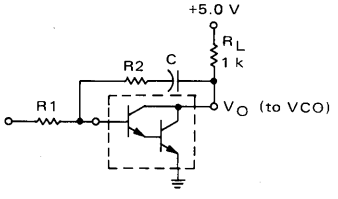
$$C = \frac{K\phi K_V}{N\omega_n^2 R_1} \qquad (11)$$

Calculation of passive components R_2 and C (in synthesizers) is complicated by incomplete information on N, which is variable, and the limits of ω_n and ζ during that variance. Equally important are changes in K_V over the output frequency range. Minimum and maximum values of ω_n and ζ can be computed from Equations 4 and 5 when the appropriate worst case numbers are known for all the factors.

Amplifier/filter gain usually determines how much phase error exists between f_{in} and f_{out}, and the filter characteristic shapes capture range and transient performance. A relatively simple, low gain amplifier may usually be used in the loop since many designs are not constrained so much by phase error as by the need to make f_{in} equal f_{out}. Unnecessarily high gains can cause problems in linear loops when the system is out of lock if the amplifier output swing is not adequately restricted since integrating operational amplifier circuits will latch up in time and effectively open the loop.

The internal amplifier included in the MC4344/4044 may be used effectively if its limits are observed. The circuit configuration shown in Figure 10 illustrates the placement of R_1, R_2, C, and load resistor R_L (1 kΩ). Due to the non-infinite gain of this stage ($A_V \approx 30$) and other non-ideal characteristics, some restraint must be placed on passive component selection. Foremost is a lower limit on the value of R_2 and an upper limit on R_1. Placed in order of priority, the recommendations are as follows: (a) R2 > 50 Ω, (b) R2/R1 ≤ 10, (c) 1 kΩ < R1 < 5 kΩ.

FIGURE 10 — USING MC4344/4044 LOOP AMPLIFIER



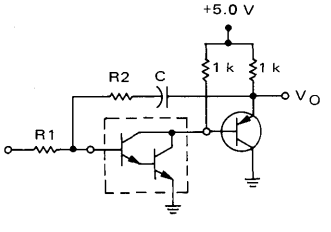
Limit (c) is the most flexible and may be violated with either higher sidebands and phase error ($R_1 > 5$ kΩ) or lower phase detector gain ($R_1 < 1$ kΩ). If limit (b) is exceeded, loop bandwidth will be less than computed and may not have any similarity to the prediction. For an accurate reproduction of calculated loop characteristics one should go to an operational amplifier which has sufficient gain to make limit (b) readily satisfied. Limit (a) is very important because T_1 in Equation 5 is in reality composed of three elements:

$$T_1 = C\left(R_2 - \frac{1}{g_m}\right) \qquad (12)$$

where g_m = transconductance of the common emitter amplifier.

Normally g_m is large and T_1 nearly equals R_2C, but resistance values below 50 Ω can force the phase-compensating "zero" to infinity or worse (into the right half plane) and give an unstable system. The problem can be circumvented to a large degree by buffering the feedback with an emitter follower (Figure 11). Inequality (a) may then be reduced by at least an order of magnitude (R_2 > 5 Ω) keeping in mind that electrolytic capacitors used

FIGURE 11 — AMPLIFIER CAPABLE OF HANDLING LOWER R2



7

as C may approach this value by themselves at the frequency of interest (ω_n).

Larger values of R_1 may be accommodated by either using an operational amplifier with a low bias current ($I_b < 1.0\ \mu A$) as shown in Figure 12 or by buffering the internal Darlington pair with an FET (Figure 13). It is vitally important, however, that the added device be operated at zero V_{GS}. Source resistor R_4 should be adjusted for this condition (which amounts to I_{DSS} current for the FET). This insures that the overall amplifier input threshold remains at the proper potential of approximately two base-emitter drops. Use of an additional emitter follower instead of the FET and R_4 (Figure 14) gives a threshold near the upper limit of the phase detector charge pump, resulting in an extremely unsymmetrical phase detector gain in the pump up versus pump down mode. It is not unusual to note a 5:1 difference in K_ϕ for circuits having the bipolar buffer stage. If the initial design can withstand this variation in loop gain and remain stable, the approach should be considered since there are no critical adjustments as in the FET circuit.

FIGURE 12 — USING AN OPERATIONAL AMPLIFIER TO EXTEND THE VALUE OF R1

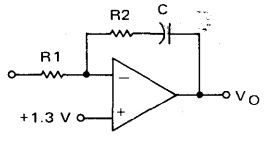


FIGURE 13 — FET BUFFERING TO RAISE AMPLIFIER INPUT IMPEDANCE

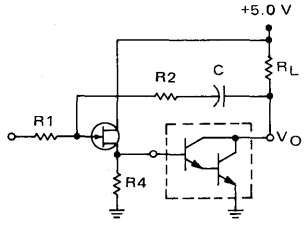
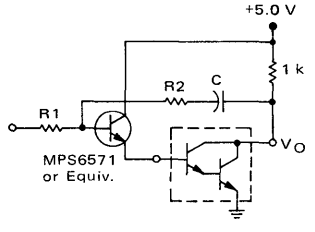


FIGURE 14 — EMITTER FOLLOWER BUFFERING OF AMPLIFIER INPUT



DESIGN PROBLEMS AND THEIR SOLUTIONS

Dynamic Range

A source of trouble for all phase-locked loops, as well as most electronics is simply overload or lack of sufficient dynamic range. One limit is the amplifier output drive to the VCO. Not only must a designer note the outside limits of the dc control voltage necessary to give the output frequency range, he must also account for the worst case of overshoot expected for the system. Relatively large damping factors ($\zeta = 0.5$) can contribute significant amounts of overshoot (30%). To be prepared for the worst case output swing the amplifier should have as much margin to positive and negative limits as the expected swing itself. That is, if a two-volt swing is sufficient to give the desired output frequency excursion, there should be at least a two-volt cushion above and below maximum expected steady-state values on the control line.

This increase in range, in order to be effective, must of course by followed by an equivalent range in the VCO or there is little to be gained. Any loss in loop gain will in general cause a decrease in ζ and a consequent increase in overshoot and ringing. If the loss in gain is caused by saturation or near saturation conditions, the problem tends to accelerate towards a situation where the system settles in not only a slow but oscillator manner as well.

Loss of amplifier gain may not be due entirely to normal system damping considerations. In loops employing digital phase detectors, an additional problem is likely to appear. This is due to amplifier saturation during a step input when there is a maximum phase detector output simultaneous with a large transient overshoot. The phase detector square wave rides on top of the normal transient and may even exceed the amplifier output limits imposed above. Since the input frequency will exceed the R_2C time constant, gain K_F for these annoying pulses will be R_2/R_1. Ordinarily this ratio will be less than 1, but some circumstances dictate a low loop gain commensurate with a fairly high ω_n. For these cases, R_2/R_1 may be higher than 10 and cause pulse-wise saturation of the amplifier. Since the dc control voltage is an average of phase detector pulses, clipping can be translated into a reduction in gain with all the "benefits" already outlined, i.e., poor settling time. An easy remedy to apply in many cases is a simple RC low pass section preceding or together with the integrator-lag section. To make transient suppression independent of amplifier response, the network may be imbedded within the input resistor R_1 (Figure 15) or be implemented by placing a feedback capacitor across R_2 (Figure 16). Besides rounding off and inhibiting pulses, these networks add an additional pole to the loop and may cause further overshoot if the cutoff frequency (ω_c) is too close to ω_n. If at all possible the cutoff point should be five to ten times ω_n. How far ω_c can be placed from ω_n depends on the input frequency relationship to ω_n since f_{in} is, after all, what is being filtered. A side benefit of this simple RC pulse "flattener" is a reduction in f_{in} sidebands around f_{out} for synthe-

sizers with N > 1. However, a series of RC filters is not recommended for either extended pulse suppression or sideband improvement as excess phase will begin to build up at the loop crossover ($\approx \omega_n$) and tend to cause instability. This will be discussed in more detail later.

FIGURE 15 — IMPROVED TRANSIENT SUPPRESSION WITH R1 — C_c

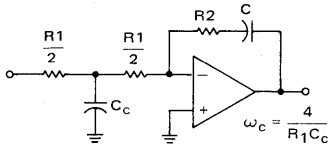
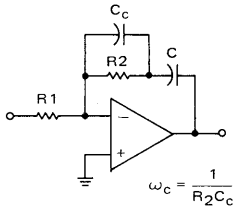


FIGURE 16 — IMPROVED TRANSIENT SUPPRESSION WITH R2 — C_c



Spurious Outputs

Although the major problem in phase-locked loop design is defining loop gain and phase margin under dynamic operating conditions, high-quality synthesizer designs also require special consideration to minimize spurious spectral components — the worst of which is reference-frequency sidebands. Requirements for good sideband suppression often conflict with other performance goals — loop dynamic behavior, suppression of VCO noise, or suppression of other in-loop noise. As a result, most synthesizer designs require compromised specifications. For a given set of components and loop dynamic conditions, reference sidebands should be predicted and checked against design specifications before any hardware is built.

Any steady-state signal on the VCO control will produce sidebands in accordance with normal FM theory. For small spurious deviations on the VCO, relative sideband-to-carrier levels can be predicted by:

$$\frac{\text{sidebands}}{\text{carrier}} \cong \frac{V_{ref} K_V}{2\omega_{ref}} \qquad (13)$$

where V_{ref} = peak voltage value of spurious frequency at the VCO input.

Unwanted control line modulation can come from a variety of sources, but the most likely cause is phase detector pulse components feeding through the loop filter. Although the filter does establish loop dynamic conditions, it leaves something to be desired as a low pass section for reference frequency components.

For the usual case where ω_{ref} is higher than $1/T_2$, the K_F function amounts to a simple resistor ratio:

$$K_F(j\omega)\Big|_{\omega = \omega_{ref}} \cong -\frac{R_2}{R_1} \qquad (14)$$

By substitution of Equations 9 and 10, this signal transfer can be related to loop parameters.

$$K_F(j\omega)\Big|_{\omega = \omega_{ref}} \cong \frac{2\zeta N\omega_n}{K_\phi K_V} = \frac{V_{ref}}{V_\phi} \qquad (15)$$

where V_{ref} = peak value of reference voltage at the VCO input, and

V_ϕ = peak value of reference frequency voltage at the phase detector output.

Sideband levels relative to reference voltage at the phase detector output can be computed by combining Equations 13 and 15:

$$\frac{\text{sideband level}}{f_{out}\text{ level}} = V_\phi \left(\frac{\zeta N\omega_n}{\omega_{ref} K_\phi}\right) \qquad (16)$$

From Equation 16 we find that for a given phase detector, a given value of R_1 (which determines V_ϕ), and given basic system constraints (N, f_{ref}), only ζ and ω_n remain as variables to diminish the sidebands. If there are few limits on ω_n, it may be lowered indefinitely until the desired degree of suppression is obtained. If ω_n is not arbitrary and the sidebands are still objectionable, additional filtering is indicated.

One item worthy of note is the absence of K_V in Equation 16. From Equation 15 it might be concluded that decreasing K_V would be another means for reducing spurious sidebands, but for constant values of ζ and ω_n this is not a free variable. In a given loop, varying K_V will certainly affect sideband voltage, but will also vary ζ and ω_n.

On the other hand, the choice of ω_n may well affect spectral purity near the carrier, although reference sideband levels may be quite acceptable.

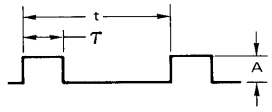
In computing sideband levels, the value of V_ϕ must be determined in relation to other loop components. Residual reference frequency components at the phase detector output are related to the dc error voltage necessary to supply charge pump leakage current and amplifier bias current. From these average voltage figures, spectral components of the reference frequency and its harmonics can be computed using an approximation that the phase detector output consists of square waves τ seconds

wide repeated at t second intervals (Figure 17). A Fourier analysis can be summarized for small ratios of τ/t by:

(1) the average voltage (V_{avg}) is $A(\tau/t)$
(2) the peak reference voltage value (V_ϕ) is twice V_{avg}, and
(3) the second harmonic ($2f_{ref}$) is roughly equal in amplitude to the fundamental.

By knowing the requirements for (1) due to amplifier bias and leakage currents, values for (2) and (3) are uniquely determined.

FIGURE 17 — PHASE DETECTOR OUTPUT



An example of this sideband approximation technique can be illustrated using the parameters specified for the synthesizer design included in the applications information section.

$N_{max} = 30$ $\quad\quad$ $\omega_n = 4500$ rad/s
$K_V = 11.2 \times 10^6$ rad/s/V $\quad\quad$ $R_1 = 2\ k\Omega$
$K_\phi = 0.12$ V/rad $\quad\quad$ $f_{ref} = 100$ kHz
$\zeta = 0.8$

Substituting these numbers into Equation 16:

$$\frac{\text{sideband}}{f_{out}} = V_\phi \frac{(0.8)(30)(4500)}{2\pi(10^5)(0.111)} \quad (17)$$

$$= V_\phi\,(1.55) \quad (18)$$

The result illustrates how much reference feedthrough will affect sideband levels. If 1.0 mV peak of reference appears at the output of the phase detector, the nearest sideband will be down 56.2 dB.

If the amplifier section included in the MC4344/4044 is used, with $R_L = 1\ k\Omega$, some approximations of the value of V_ϕ can be made based on the input bias current and the value of R_1. The phase detector must provide sufficient average voltage to supply the amplifier bias current, I_b, through R_1; when the bias current is about 5.0 μA and R_1 is 2 kΩ, V_{avg} must be 10 mV. From the assumptions earlier concerning the Fourier transform, and with the help of Figure 18, we can see that the phase detector duty cycle will be about 1.7% (A = 0.6 V), giving a fundamental (reference) of 20 mV peak. If this value for V_ϕ is substituted into Equation 18, the resulting sideband ratio represents 30 dB suppression due to this component alone.

In addition to the amplifier bias current, another factor to consider is transistor Q5 reverse leakage current I_L flowing into pin 10 of the MC4344/4044 charge pump. I_L is generally less than 1.0 μA and is no more than 5.0 μA over the temperature range. A typical design value for 25°C is 0.1 μA. Both I_L and amplifier bias current I_B are in a direction to deplenish the charge on filter capacitor C. A second charge pump leakage, I_L', attributed by diode CR1 flows out of pin 5. This current, however, is in a direction to help supply I_B and I_L and thus tends to minimize the discharge of C. Typically I_L' is much less than I_L and, since it is also in a direction to minimize discharge of the filter capacitor, it will be ignored in the following discussion. The total charge removed from C must be replaced by current supplied by the charge pump during the next up-date opportunity. This current flows through R1. To minimize the effects of I_B and I_L a relative small value of R1 should be chosen. A minimum value of 1 kΩ is a good choice.

FIGURE 18 — OUTPUT ERROR CHARACTERISTICS

DUTY CYCLE (%)	PHASE ERROR (Deg)	V_{avg} (mV)	$V_{\phi(peak)}$ (mV)
0.1	0.36	0.6	1.2
0.2	0.72	1.2	2.4
0.3	1.08	1.8	3.6
0.4	1.44	2.4	4.8
0.5	1.80	3.0	6.0
0.6	2.16	3.6	7.2
0.7	2.52	4.2	8.4
0.8	2.88	4.8	9.6
0.9	3.24	5.4	10.8
1.0	3.60	6.0	12.0
2.0	7.2	12.0	24.0
3.0	10.8	18.0	35.9
4.0	14.4	24.0	47.9
5.0	18.0	30.0	59.8
6.0	21.6	36.0	71.6
7.0	25.2	42.0	83.3
8.0	28.8	48.0	95.0
9.0	32.4	54.0	106.6
10.0	36.0	60.0	118.0

After values for C and R_2 have been computed on the basis of loop dynamic properties, the overall sideband to f_{out} ratio computation can be simplified.

Since

$$V_\phi = 2\,V_{avg} \qquad = 2R_1\,(I_b + I_L)\left(\frac{R_2}{R_1}\right)$$
$$V_{avg} = (I_b + I_L)\,R_1$$
$$V_\phi = 2\,(I_b + I_L)\,R_1$$

$$V_{ref} = V_\phi\left(\frac{R_2}{R_1}\right) \qquad = 2R_2\,(I_b + I_L)$$

we find that

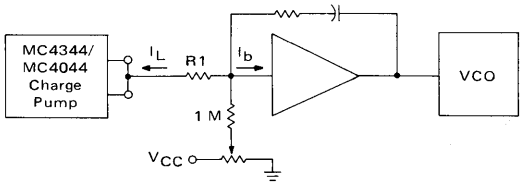
$$\frac{\text{sideband}}{f_{out}} = \frac{V_{ref}K_V}{2\omega_{ref}} \quad (19)$$

$$\frac{\text{sideband}}{f_{out}} = \frac{2R_2(I_b + I_L)K_V}{2\omega_{ref}} \quad (20)$$

Equation 20 indicates that excellent suppression could be achieved if the bias and leakage terms were nulled by current summing at the amplifier input (Figure 19). This has indeed proved to be the case. Experimental results indicate that greater than 60 dB rejection can routinely

be achieved at a constant temperature. However when nulling fairly large values (> 100 nA), the rejection becomes quite sensitive since leakages are inherently a function of temperature. This technique has proved useful in achieving improved system performance when used in conjunction with good circuit practice and reference filtering.

FIGURE 19 — COMPENSATING FOR BIAS AND LEAKAGE CURRENT



Additional Loop Filtering

So far, only the effects of fundamental loop dynamics on resultant sidebands have been considered. If further sideband suppression is required, additional loop filtering is indicated. However, care must be taken in placement of any low pass rolloff with regard to the loop natural frequency (ω_n). On one hand, the "corner" should be well below (lower than) ω_{ref} and yet far removed (above) from ω_n. Although no easy method for placing the roll-off point exists, a rule of thumb that usually works is:

$$\omega_c = 5\omega_n \qquad (21)$$

Reference frequency suppression per pole is the ratio of ω_c to ω_{ref}.

$$SB_{dB} \cong n\ 20 \log_{10} \left(\frac{\omega_c}{\omega_{ref}}\right) \qquad (22)$$

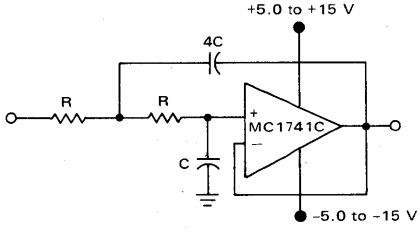
where n is the number of poles in the filter.

Equation 22 gives the additional loop suppression to ω_{ref}; this number should be added to whatever suppression already exists.

For non-critical applications, simple RC networks may suffice, but if more than one section is required, loop dynamics undergo undesirable changes. Loop damping factor decreases, resulting in a high percentage of overshoot and increased ringing since passive RC sections tend to accumulate phase shift more rapidly than signal suppression and part of this excess phase subtracts from the loop phase margin. Less phase margin translates into a lower damping factor and can, in the limit, cause outright oscillation.

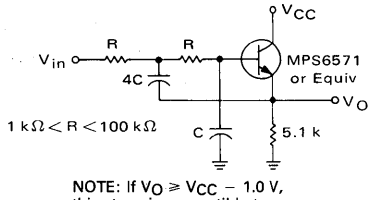
A suitable alternative is an active RC section, Figure 20, compatible with the existing levels and voltages. An active two pole filter (second order section) can realize a more gradual phase shift at frequencies less than the cutoff point and still get nearly equal suppression at frequencies above the cutoff point. Sections designed with a slight amount of peaking ($\zeta \cong 0.5$) show a good compromise between excess phase below cutoff (ω_c), without peaking enough to cause any danger of raising the loop gain for frequencies above ω_n. A fairly non-critical section may simply use an emitter follower as the active device with two resistors and capacitors completing the circuit (Figure 21). This provides a −12 dB/octave (−40 dB/decade) rolloff characteristic above ω_n, though the attenuation may be more accurately determined by Equation 22. If the sideband problem persists, an additional section may be added in series with the first. No more than two sections are recommended since at that time either (1) the constraint between ω_n and ω_{ref} is too close, or (2) reference voltage is modulating the VCO from a source other than the phase detector through the loop amplifier.

FIGURE 20 — OPERATIONAL AMPLIFIER LOW PASS FILTER



1. Choose R
   $1\ k\Omega < R < 1\ M\Omega$
2. $C = \frac{0.5}{\omega_c R}$

FIGURE 21 — EMITTER FOLLOWER LOW PASS FILTER

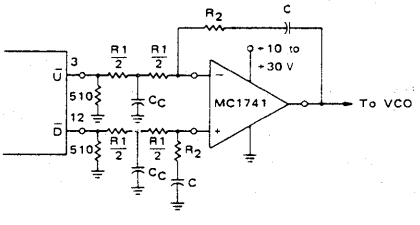


NOTE: If $V_O \geq V_{CC} - 1.0$ V, this stage is susceptible to power supply noise.

Operation without charge pump phase detector #1 of the MC4344/4044 can be implemented quite successfully in many applications without using the charge pump and internal darlington amplifier approach. An operational amplifier filter can be used to process the error information appearing at U1 and D1 (pins 13 and 2) directly (Figure 22).This phase detector/filter approach offers a potentially superior performing system because:

a. Charge pump delay time is eliminated.
b. Charge pump input signed threshold level need not be overcome before error information is obtained. This can result in a substantial improvement in the

FIGURE 22—TYPICAL FILTER AND SUMMING NETWORK



4044's transfer function linearity in the vicinity of zero phase error between the R and V inputs.

c. The filter amplifier ground location can be separated from the phase detector ground.

d. An "optimum" filter amplifier input threshold of approximately two diode drops need not be established.

The filter discussions and relationships developed for integrator-log filter sections can be applied to the system of Figure 22 and the previously derived equations can be used to determine values for R1, R2 and C.

It may be desirable to split each of the R1 resistors and incorporate a capacitor to ground in a manner similar to that shown in Figure 15. This should improve transient suppression and provide integration of the U1 and D1 signals to better enable the operational amplifier to develop corrective error information from very narrow U1 and D1 pulse widths.

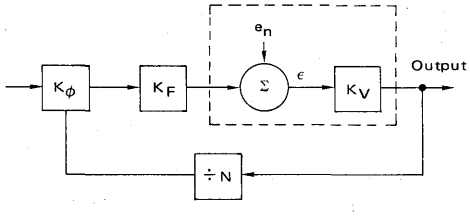
Phase error for the circuit in Figure 22 will result from input offset voltage in the operational amplifier, resistor mismatch and mismatch between the phase detector output states appearing at U1 and D1. Phase error can be trimmed to zero initially by adjusting either the amplifier input offset or one of the R1 resistors.

VCO Noise

Effects of noise within the VCO itself can be evaluated by considering a closed loop situation with an external noise source, e_n, introduced at the VCO (Figure 23). Resultant modulation of the VCO by error voltage, ε, is a second order high pass function:

$$\frac{\varepsilon}{e_n} = \frac{S^2}{S^2 + \frac{ST_1K\phi K_V}{T_2N} + \frac{K\phi K_V}{T_2N}} = \frac{S_2}{S^2 + 2\zeta\omega_n S + \omega_n{}^2} \qquad (23)$$

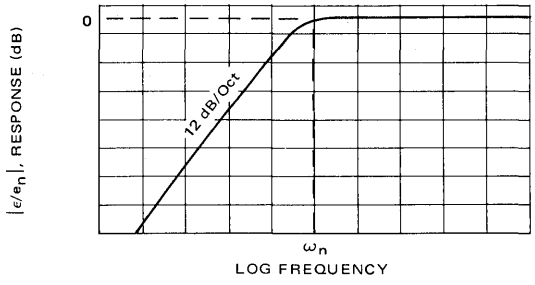
FIGURE 23 — EFFECTS OF VCO NOISE



$$\frac{\epsilon}{e_n} = \frac{S^2}{S^2 + 2\xi\omega_n S + \omega_n{}^2}$$

This function has a slope of 12 dB/octave at frequencies less than ω_n (loop natural frequency), as shown in Figure 24. This means that noise components in the VCO above ω_n will pass unattenuated and those below will have some degree of suppression. Therefore choice of loop natural frequency may well rest on VCO noise quality.

FIGURE 24 — LOOP RESPONSE TO VCO NOISE

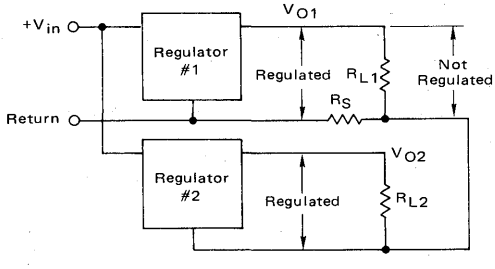


Other Spurious Responses

Spurious components appearing in the output spectrum are seldom due to reference frequency feedthrough alone. Modulation of any kind appearing on the VCO control line will cause spurious sidebands and can come in through the loop amplifier supply, bias circuitry in the control path, a translator, or even the VCO supply itself. Some VCOs have a relatively high sensitivity to power supply variation. This should be investigated and its effects considered. Problems of this nature can be minimized by operating all devices except the phase detector, charge pump, and VCO from a separate and well isolated supply. A common method uses a master supply of about 10 or 12 volts and two regulators to produce voltages for the PLL — one for all the logic (including the phase detector) and the other for all circuitry associated with the VCO control line.

Sideband and noise performance is also a function of good power supply and regulator layout. As mentioned earlier, extreme care should be exercised in isolating the control line voltage to the VCO from influences other than the phase detector. This not only means good voltage regulation but ac bypassing and adherence to good grounding techniques as well. Figure 25 shows two separate regulators and their respective loads. Resistor R_S is a small stray resistance due to a common thin ground return for both R_{L1} and R_{L2}. Any noise in R_{L2} is now reproduced (in a suppressed form) across R_{L1}. Load current from R_{L1} does not affect the voltage across R_{L2}. Even though the regulators may be quite good, they can hold V_O constant only across their outputs, not necessarily across the load (unless remote sensing is used).

FIGURE 25 — LOOP VOLTAGE REGULATION



One solution to the ground-coupled noise problem is to lay out the return path with the most sensitive regulated circuit at the farthest point from power supply entry as shown in Figure 26.

Even for regulated subcircuits, accumulated noise on the ground bus can pose major problems since although the cross currents do not produce a differential load voltage directly, they do produce essentially common mode noise on the regulators. Output differential load noise then is a function of the input regulation specification. By far the best way to sidestep the problem is to connect each subcircuit ground to the power supply entry return line as shown in Figure 27.

FIGURE 26 — REGULATOR LAYOUT

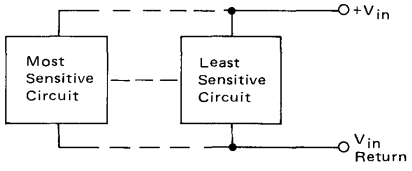
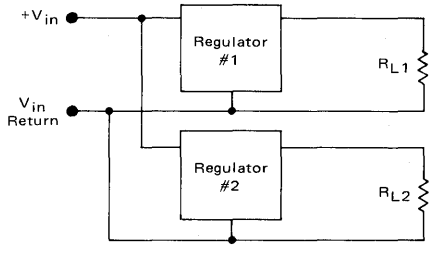


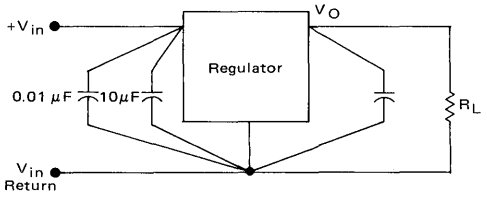
FIGURE 27 — REGULATOR GROUND CONNECTION



In Figures 25 and 27, R_{L1} and R_{L2} represent component groups in the system. The designer must insure that all ground return leads in a specific component group are returned to the common ground. Probably the most overlooked components are bypass capacitors. To minimize sidebands, extreme caution must be taken in the area immediately following the phase detector and through the VCO. A partial schematic of a typical loop amplifier and filter is shown in Figure 28 to illustrate the common grounding technique.

Bypassing in a phase-locked loop must be effective at both high frequencies and low frequencies. One capacitor in the 1.0-to-10 μF range and another between 0.01 and 0.001 μF are usually adequate. These can be effectively utilized both at the immediate circuitry (between supply and common ground) and the regulator if it is some distance away. When used at the regulator, a single electrolytic capacitor on the output and a capacitor pair at the input is most effective (Figure 29). It is important, again, to note that these bypasses go from the input/output pins to as near the regulator ground pin as possible.

FIGURE 29 — SUGGESTED BYPASSING PROCEDURE



APPLICATIONS INFORMATION

Frequency Synthesizers

The basic PLL discussed earlier is actually a special case of frequency synthesis. In that instance, $f_{out} = f_{in}$, although normally a programmable counter in the feedback loop insures the general rule that $f_{out} = Nf_{in}$ (Figure 30). In the synthesizer f_{in} is usually constant (crystal controlled) and f_{out} is changed by varying the programmable divider (÷ N). By stepping N in integer increments, the output frequency is changed by f_{in} per increment. In com-

FIGURE 30 — PHASE-LOCKED LOOP WITH PROGRAMMABLE COUNTER

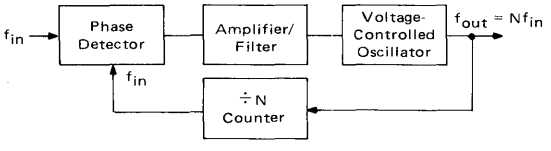
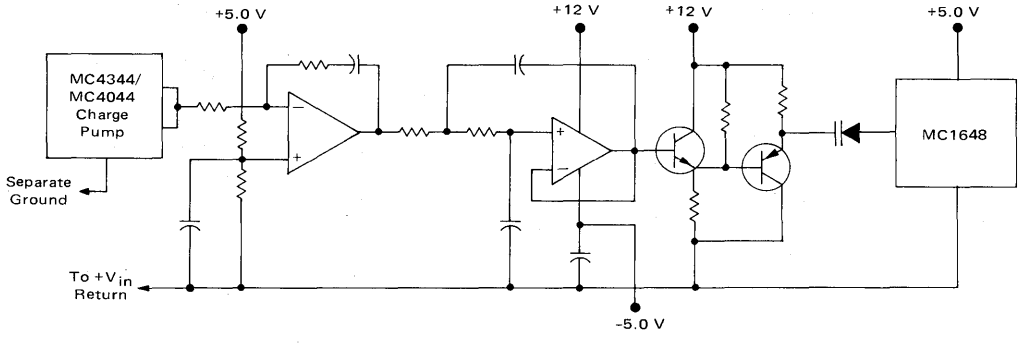


FIGURE 28 — PARTIAL SCHEMATIC OF LOOP AMPLIFIER AND FILTER



munication use, this input frequency is called the "channel spacing" or, in general, it is the reference frequency.

There is essentially no difference in loop dynamic problems between the basic PLL and synthesizers except that synthesizer designers must contend with problems peculiar to loops where N is variable and greater than 1. Also, sidebands or spectral purity usually require special attention. These and other aspects are discussed in greater detail in AN-535. The steps for a suitable synthesis procedure may be summarized as follows:

Synthesis Procedure

1. Choose input frequency. (f_{ref} = channel spacing)
2. Compute the range of digital division:

$$N_{max} = \frac{f_{max}}{f_{ref}}$$

$$N_{min} = \frac{f_{min}}{f_{ref}}$$

3. Compute needed VCO range:

$$(2f_{max} - f_{min}) < f_{VCO} < (2f_{min} - f_{max})$$

4. Choose minimum ζ from transient response plot, Figure 9. A good starting point is $\zeta = 0.5$.
5. Choose ω_n from needed response time (Figure 9):

$$\omega_n = \frac{\omega_n t}{t}$$

6. Compute C:

$$C = \frac{K_\phi K_V}{N_{max}\omega_n^2 R_1}$$

7. Compute R_2:

$$R_2 = \frac{2\zeta_{min}}{\omega_n C}$$

8. Compute ζ_{max}:

$$\zeta_{max} = \zeta_{min}\sqrt{\frac{N_{max}}{N_{min}}}$$

9. Check transient response of ζ_{max} for compatibility with transient specification.
10. Compute expected sidebands:

$$\frac{\text{sideband}}{f_{out}} \cong \frac{(I_b + I_L)R_2K_V}{\omega_{ref}} \qquad \text{(A)}$$

(I_L is about 100 nA at $T_J = 25°C$.)

11. If step 10 yields larger sidebands than are acceptable, add a single pole at the loop amplifier by splitting R_1 and adding C_c as shown in Figure 15:

$$C_c \cong \frac{0.8}{R_1\omega_n}$$

Added sideband suppression (dB) is:

$$dB \cong 20\log_{10}\frac{1}{\sqrt{1 + \frac{\omega_{ref}^2}{25(\omega_n)^2}}} \qquad \text{(B)}$$

12. If step 11 still does not give the desired results, add a second order section at $\omega_c = 5\,\omega_n$ using either the configuration of Figure 20 or 21. The expected improvement is twice that of the single pole in step 11.

$$dB \cong 40\log_{10}\frac{1}{\sqrt{1 + \frac{\omega_{ref}^2}{25(\omega_n)^2}}} \qquad \text{(C)}$$

Total sideband rejection is then the total of $20\log_{10}$(A) + (B) + (C).

Design Example (Figure 31)

Assume the following requirements:
Output frequency, f_{out} = 2.0 MHz to 3.0 MHz
Frequency steps, f_{in} = 100 kHz
Lockup time between channels (to 5%) = 1.0 ms
Overshoot < 20%.
Minimum sideband suppression = −30 dB

From the steps of the synthesis procedure:

1. $f_{ref} = f_{in}$ = 100 kHz
2. $N_{max} = \frac{f_{max}}{f_{ref}} = \frac{3.0\text{ MHz}}{0.1\text{ MHz}} = 30$

   $N_{min} = \frac{f_{min}}{f_{ref}} = \frac{2.0\text{ MHz}}{0.1\text{ MHz}} = 20$
3. VCO range:
   The VCO output frequency range should extend beyond the specified minimum-maximum limits to accommodate the overshoot specification. In this instance f_{out} should be able to cover an additional 20% on either end. End limits on the VCO are:

   $f_{out}max \geq 3.0 + 0.2(1.0) = 3.2$ MHz
   $f_{out}min \leq 2.0 - 0.2(1.0) = 1.8$ MHz

   This VCO range (≈ 1.8:1) is realizable with the MC4324/4024 voltage controlled multivibrator. From Figure 7 of the MC4324/4024 data sheet we find the required tuning capacitor value to be 120 pF and the VCO gain, K_V, typically 11 × 10^6 rad/s/v.
4. From the step response curve of Figure 9, $\zeta = 0.8$ will produce a peak overshoot less than 20%.
5. Referring to Figure 9, overshoot with $\zeta = 0.8$ will settle to within 5% at $\omega_n t = 4.5$. Since the required lock-up time is 1.0 ms,

$$\omega_n = \frac{\omega_n t}{t} = \frac{4.5}{t} = \frac{4.5}{0.001} = (4.5)(10^3)\text{rad/s}$$

7

6. In order to compute C, phase detector gain and R1 must be selected. Phase detector gain, K_ϕ, for the MC4344/4044 is approximately 0.1 volt/radian with $R_1 = 1\ k\Omega$. Therefore,

$$C = \frac{(0.1)(11 \times 10^6)}{(30)(4.5 \times 10^3)2(10^3)} = 1.8\ \mu F$$

7. At this point, R_2 can be computed:

$$R_2 = \frac{2\zeta_{min}}{\omega_n C} = \frac{1.6}{(4.5 \times 10^3)(1.8 \times 10^{-6})} = 200\ \Omega$$

8. $$\zeta_{max} = \zeta_{min}\sqrt{\frac{N_{max}}{N_{min}}} = 0.98$$

9. Figure 9 shows that $\zeta = 0.98$ will meet the settling time requirement.
10. Sidebands may be computed for two cases: (1) with I_L (charge pump leakage current) nominal (100 nA), and (2) with I_L maximum (5.0 μA). A value of 5 μA will also be assumed for the amplifier bias current, i_b.

$$\left.\frac{\text{sideband}}{f_{out}}\right|_{max} = \frac{(10 \times 10^{-6})(200)(11 \times 10^6)}{6.28 \times 10^5} \cong 35 \times 10^{-3}$$

The sideband-to-center frequency ratio nominally will be:

$$\left.\frac{\text{sideband}}{f_{out}}\right|_{nom} = \frac{5.1}{10} \times 35 \times 10^{-3}$$

$$= 20 \log_{10}(17.85 \times 10^{-3}) \cong -35\ dB$$

If desired additional sideband filtering can be obtained as noted in steps 11 and 12.

11. By splitting R_1 and C_C, further attenuation can be gained. The magnitude of C_C is approximately:

$$C_C = \frac{0.8}{R_1\omega_n} = \frac{0.8}{(10^3)(4.5)(10^3)} \cong 0.18\ \mu F$$

Improvement in sidebands will be:

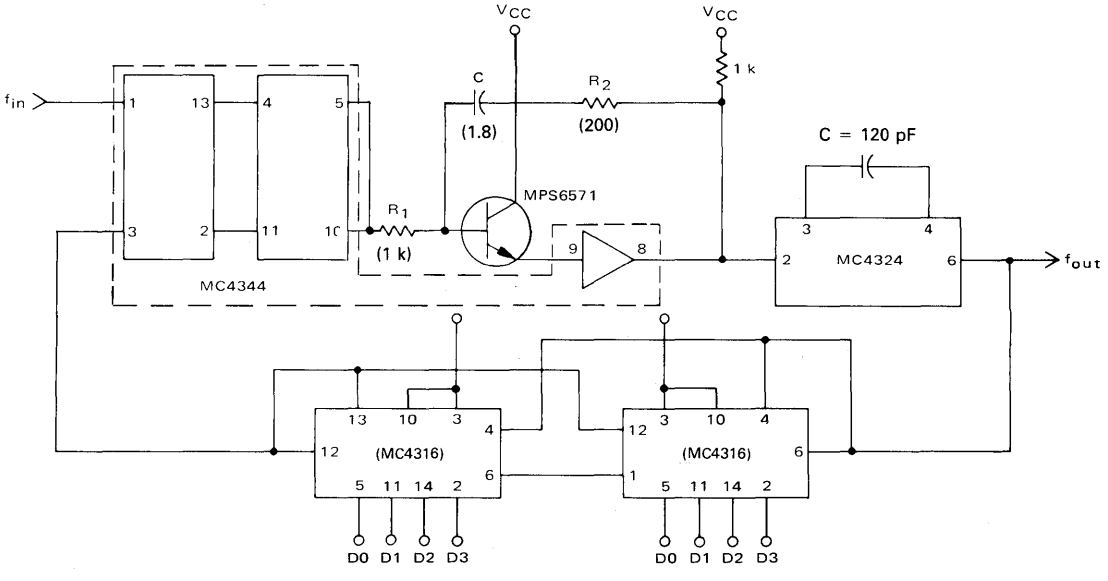
$$20 \log_{10} \frac{1}{\sqrt{1 + \frac{(2\pi \times 10^5)^2}{25(4.5 \times 10^3)^2}}} = -28\ dB$$

Nominal suppression is now −63 dB. Worst-case is 6 dB higher than nominal suppression of −57 dB. This is well within the −30 dB design requirement, step 12 is included for completeness only.

12. Attenuation of a second order filter is double that of the single order filter section described in step 11. The calculations for a second order filter indicate an additional −56 dB of sideband rejection. Figures 20 and 21 show two second order filter configurations. If R is assigned a value of 10 kΩ then C may be calculated.

$$C = \frac{0.1}{\omega_n R} = \frac{0.1}{(4.5 \times 10^3)(10^4)} = 0.0022\ \mu F$$

FIGURE 31 — CIRCUIT DIAGRAM OF TYPE 2 PHASE-LOCKED LOOP



Clock Recovery from Phase-Encoded Data

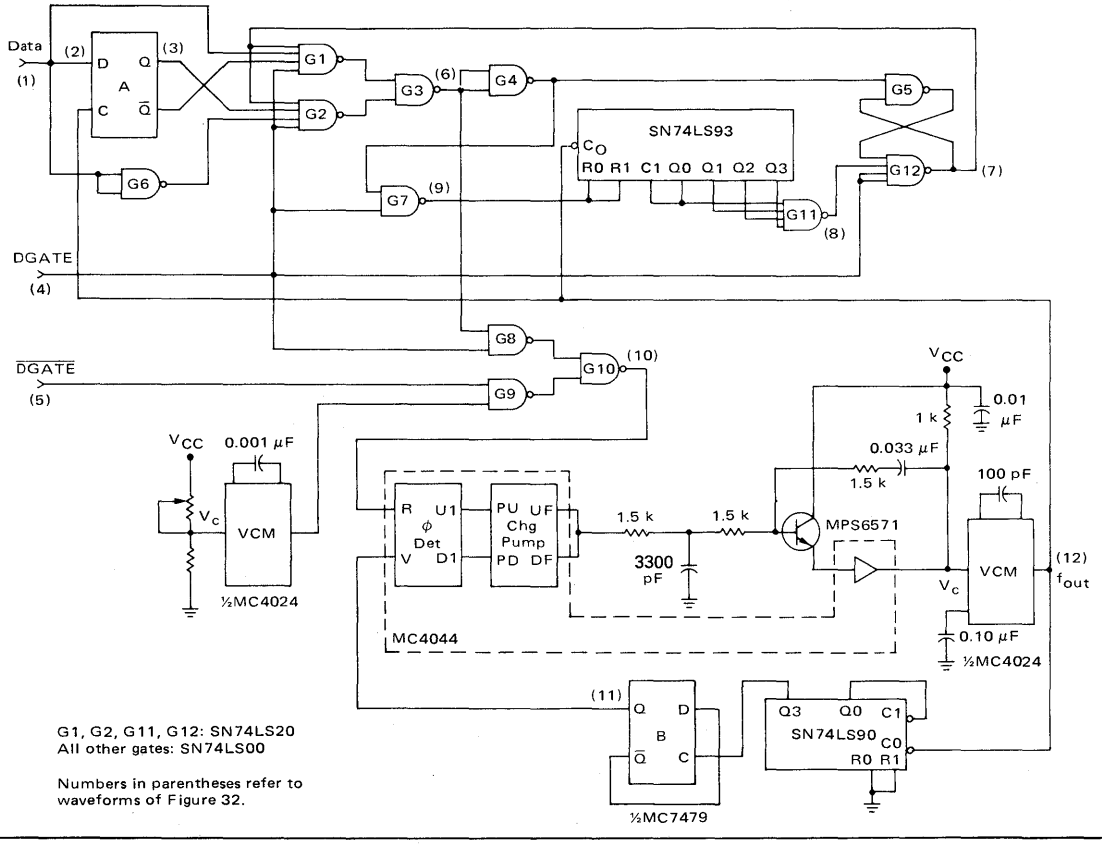
The electro-mechanical system used for recording digital data on magnetic tape often introduces random variations in tape speed and data spacing. Because of this and the encoding technique used, it is usually necessary to regenerate a synchronized clock from the data during this read cycle. One method for doing this is to phase-lock a voltage controlled multivibrator to the data as it is read (Figure 32).

A typical data block using the phase encoded format is shown in row 1 of Figure 33. The standard format calls for recording a preamble of forty "0"s followed by a single "1"; this is followed by from 18 to 2048 characters of data and a postamble consisting of a "1" followed by forty "0"s. The encoding format records a "0" as a transition from low to high in the middle of a data cell. A "1" is indicated by a transition from high to low at the data cell midpoint. When required, phase transitions occur at the end of data cells. If a string of either consecutive "0"s or consecutive "1"s is recorded, the format duplicates the original clock; the clock is easily recovered by straight forward synchronization with a phase-locked loop. In the general case, where the data may appear in any order, the phase-encoded data must be processed to obtain a single pulse during each data cell before it is applied to the phase detector. For example, if the data consisted only of alternating "1"s and "0"s, the phase-encoded format would result in a waveform equal to one-half the original clock frequency. If this were applied directly to the loop, the VCM would of course move down to that frequency. The encoding format insures that there will be a transition in the middle of each data time. If only these transitions are sensed they can be used to regenerate the clock. The schematic diagram of Figure 32 indicates one method of accomplishing this.

The logic circuitry generates a pulse at the midpoint of each data cell which is then applied to the reference input of the phase detector. The loop VCM is designed to operate at some multiple of the basic clock rate. The VCM frequency selected depends on the decoding resolution desired and other system timing requirements. In this example, the VCM operates at twenty-four times the clock rate (Figure 33, Row 12).

Referring to Figure 32 and the timing diagram of Figure 33, the phase-encoded data (Figure 33, Row 1) is combined with a delayed version of itself (output of flip-flop A row 3) to provide a positive pulse out of G3 for every transition of the input signal. Portions of the data block are shown expanded in row 2 of Figure 33. Flip-flop A delays the incoming data of one-half of a VCM clock period. Gates G1, G2 and G3 implement the logic Exclusive OR of waveforms 1 and 3 except when inhibited by DGATE (row 4) or the output of G12 (row 7). DGATE and

FIGURE 32 — CLOCK RECOVERY FROM PHASE-ENCODED DATA



its complement, $\overline{DGATE}$, serve to initialize the circuitry and insure that the first transition of the data block (a phase transition) is ignored. The MC7493 binary counter and the G5-G12 latch generate a suitable signal for gating out G3 pulses caused by phase transitions at the end of a data cell, such as the one shown dashed in row 6.

The initial data pulse from G3 sets G12 low and is combined with DGATE in G7 to reset the counter to its zero state. Subsequent VCM clock pulses now cycle the counter and approximately one-third of the way through the next data cell the counter's full state is decoded by G11, generating a negative transition. This causes G12 to go high, removing the inhibit signal until it is again reset by the next data transition. This pulse also resets the counter, continuing the cycle and generating a positive pulse at the midpoint of each data cell as required.

Acquisition time is reduced if the loop is locked to a frequency approximately the same as the expected data rate during inter-block gaps. In Figure 32, this is achieved by operating the remaining half of the dual VCM at slightly less than the data rate and applying it to the reference input of the phase detector via the G8-G9-G10 data selector. When data appears, DGATE and $\overline{DGATE}$ cause the output of G3 to be selected as the reference input to the loop.

The loop parameters are selected as a compromise between fast acquisition and jitter-free tracking once synchronization is achieved. The resulting filter component values indicated in Figure 32 are suitable for recovering the clock from data recorded at a 120 kHz rate, such as would result in a tape system operating at 75 i.p.s. with a recording density of 1600 b.p.i. Synchronization is achieved by approximately the twenty-fourth bit time of the preamble. The relationship between system requirements and the design procedure is illustrated by the following sample calculation:

Assume a −3.0 dB loop bandwidth much less than the input data rate (≈ 120 kHz), say 10 kHz. Further, assume a damping factor of $\zeta = 0.707$. From the expression for loop bandwidth as a function of damping factor and undamped natural frequency, ω_n, calculate ω_n as:

$$\omega_{-3\ dB} = \omega_n \left(1 + 2\zeta^2 + \sqrt{2 + 4\zeta 2 + 4\zeta 4}\right)^{1/2} \quad (24)$$

or for $\omega_{-3\ dB} = (2\pi)10^4$ rad/s and $\zeta = 0.707$:

$$\omega_n = \frac{(2\pi)10^4}{2.06} = (3.05)10^4 \text{ rad/s}$$

As a rough check on acquisition time, assume that lockup should occur not later than half-way through a 40-bit preample, or for twenty 8.34 μs data periods.

$$\omega_n t = (3.05)10^4(20)(8.34)10^{-6} = 5.1 \quad (26)$$

From Figure 9, the output will be within 2 to 3% of its final value for $\omega_n t \approx 5$ and $\zeta = 0.707$. The filter components are calculated by:

$$\frac{K_\phi K_V}{R_1 CN} = \omega_n^2 \quad (27)$$

and

$$\frac{K_\phi K_V R_2}{R_1 N} = 2\zeta\omega_n \quad (28)$$

where $K_\phi = 0.115$ v/rad
$K_V = (18.2)\ 10^6$ rad/s/volt
$N = 24$ = Feedback divider ratio
$\omega_n = (3.05)\ 10^4$ rad/s
$\zeta = 0.707$

$$\frac{K_\phi K_V}{N} = \frac{(0.115)(18.2)10^6}{24} = (8.72)10^4$$

From Equation 27:

$$R_1 C = \frac{K_\phi K_V}{N\omega_n^2} = \frac{(8.72)10^4}{(3.05)^2 10^8} = (9.34)10^{-5}$$

From Equation 28:

$$\frac{R_2}{R_1} = \frac{2\zeta\omega_n N}{K_\phi K_V} = \frac{2(0.707)(3.05)10^4}{(8.72)10^4} = 0.494 \approx 1/2$$

Let $R_1 = 3.0$ kΩ; then $R_2 = 1.5$ kΩ and

$$C = \frac{(9.34)10^{-5}}{(3.0)10^3} = (3.1)10^{-8}$$

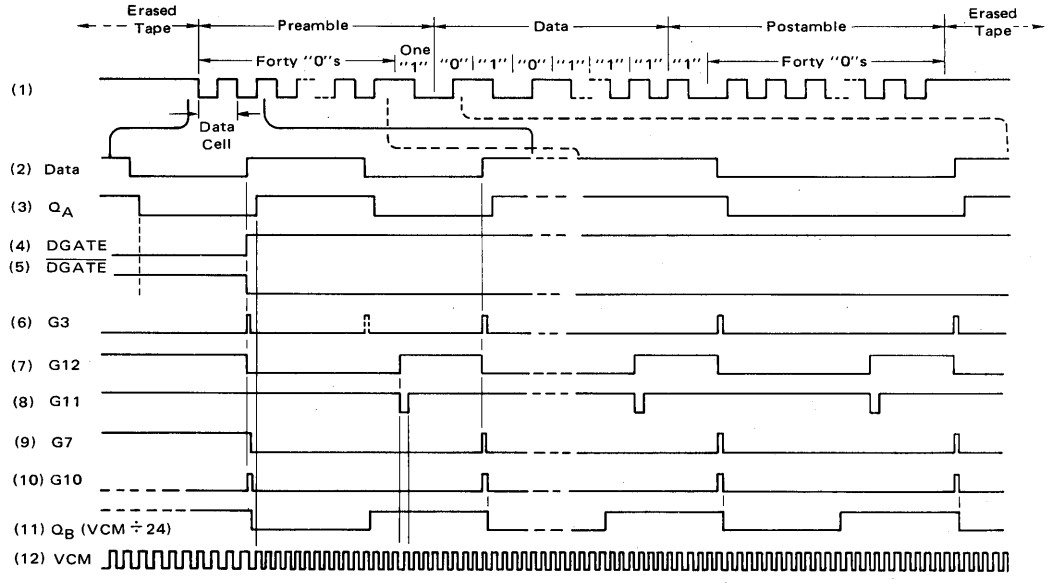
or using a close standard value, use $C = 0.033$ μF. Now add the additional prefiltering by splitting R_1 and selecting a time constant for the additional section so that it is large with respect to R_2C_2.

$$10(1/2 R_1)C_C = R_2 C$$

or

$$C_C = \frac{2R_2 C}{10R_1} = \frac{2(1.5)10^3(3.3)10^{-8}}{10(3.0)10^3} = 3300 \text{ pF}$$

FIGURE 33— TIMING DIAGRAM — CLOCK RECOVERY FROM PHASE-ENCODED DATA



7

MOTOROLA

MC12000

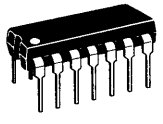
DIGITAL MIXER/TRANSLATOR
(D Flip-Flop w/Translator)

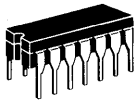
The MC12000 is intended for use as a digital mixer in phase-locked loop frequency synthesizers and other applications where a MECL "D" flip-flop with translators is required. Toggle frequency is typically 250 MHz. TTL to MECL and MECL to TTL translators are provided to facilitate interfacing with MECL or TTL circuits.

The MC12000 is designed to operate from a single power supply of either +5.0 Vdc or −5.2 Vdc.

DIGITAL MIXER/TRANSLATOR

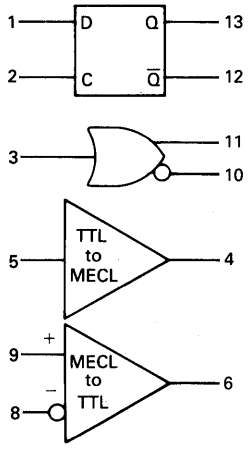
P SUFFIX
PLASTIC PACKAGE
CASE 646





L SUFFIX
CERAMIC PACKAGE
CASE 632

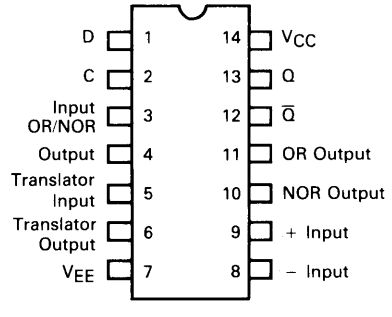
LOGIC DIAGRAM



D	Q_n	Q_{n+1}
0	0	0
0	1	0
1	0	1
1	1	1

V_{CC} = Pin 14
V_{EE} = Pin 7

PIN ASSIGNMENT



7

ELECTRICAL CHARACTERISTICS

Supply Voltage = +5.0 V

@ Test Temperature	TEST VOLTAGE/CURRENT VALUES													
	Volts											mA		
	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{IL}	V_{IH}	V_{IHA}	V_R	V_{IHT}	V_{ILT}	V_{CC}	I_L	I_{OL}	I_{OH}
0°C	+4.25	+3.130	+3.855	+3.49	+0.5	+2.4	+5.0	+4.5	+2.0	+0.8	+5.0	-2.5	16	-0.4
25°C	+4.28	+3.150	+3.895	+3.525	+0.5	+2.4	+5.0	+4.5	+2.0	+0.8	+5.0	-2.5	16	-0.4
75°C	+4.37	+3.170	+3.955	+3.550	+0.5	+2.4	+5.0	+4.5	+2.0	+0.8	+5.0	-2.5	16	-0.4

Characteristic	Symbol	Pin Under Test	MC12000 0°C Min	MC12000 0°C Max	MC12000 +25°C Min	MC12000 +25°C Typ	MC12000 +25°C Max	MC12000 +75°C Min	MC12000 +75°C Max	Unit	TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{IL}	V_{IH}	V_{IHH}	V_R	V_{IHT}	V_{ILT}	V_{CC}	I_L	I_{OL}	I_{OH}	(V_{EE}) Gnd
Power Supply Drain Current	I_E	7	–	–	–	85	117	–	–	mAdc	–	–	–	–	–	–	–	–	–	–	14	–	–	–	7
Input Current	I_{INH1}	1	–	–	–	–	200	–	–	μAdc	1	2	–	–	–	–	–	–	–	–	14	–	–	–	7
		2	–	–	–	–	200	–	–		2	1	–	–	–	–	–	–	–	–		–	–	–	
		3	–	–	–	–	200	–	–		3	–	–	–	–	–	–	–	–	–		–	–	–	
	I_{INH2}	5	–	40	–	–	40	–	40		–	–	–	–	–	–	5	–	–	–		–	–	–	
	I_{INH3}	8	–	–	1.4	–	3.6	–	–	mAdc	9	8	–	–	–	–	–	–	–	–		–	–	–	
		9	–	–	—	–	—	–	–		9	8	–	–	–	–	–	–	–	–		–	–	–	
	I_{INL1}	1	–	–	–	–	2.0	–	–	μAdc	–	–	–	–	–	–	–	–	–	–	14	–	–	–	1,7
	(Leakage	2	–	–	–	–	2.0	–	–		–	–	–	–	–	–	–	–	–	–		–	–	–	2,7
	Current)	3	–	–	–	–	2.0	–	–		–	–	–	–	–	–	–	–	–	–		–	–	–	3,7
	I_{INL2}	5	–	+1.6	–	–	+1.6	–	+1.6	mAdc	–	–	–	–	5	–	–	–	–	–		–	–	–	7
	I_{INL3}	8	–	–	2.0	–	5.0	–	–		8	9	–	–	–	–	–	–	–	–		–	–	–	
	I_{INL4}	9	–	–	0.8	–	2.0	–	–		8	9	–	–	–	–	–	–	–	–		–	–	–	
Logic "1" Output Voltage	V_{OH1}	4	4.000	4.25	4.040	–	4.28	4.100	4.37	Vdc	–	–	–	–	–	5	–	–	–	–	14	4	–	–	7
		10				–					–	3	–	–	–	–	–	–	–	–		10	–	–	
		11				–					3	–	–	–	–	–	–	–	–	–		11	–	–	
		12†				–					–	1	–	–	–	–	–	–	–	–		12	–	–	
		13†				–					1	–	–	–	–	–	–	–	–	–		13	–	–	
	V_{OH2}	6	2.400	–	2.400	–	–	2.400	–	Vdc	9	8	–	–	–	–	–	–	–	–	14	–	–	6	7
Logic "0" Output Voltage	V_{OL1}	4	3.0	3.370	3.05	–	3.380	3.07	3.46	Vdc	–	–	–	–	5	–	–	–	–	–	14	4	–	–	7
		10				–					3	–	–	–	–	–	–	–	–	–		10	–	–	
		11				–					–	3	–	–	–	–	–	–	–	–		11	–	–	
		12†				–					1	–	–	–	–	–	–	–	–	–		12	–	–	
		13†				–					–	1	–	–	–	–	–	–	–	–		13	–	–	
	V_{OL2}	6	–	0.500	–	–	0.500	–	0.500	Vdc	8	9	–	–	–	–	–	–	–	–	14	–	6	–	7
Logic "1" Threshold Voltage	V_{OHA}	4	3.980	–	4.020	–	–	4.080	–	Vdc	–	–	–	–	–	–	–	–	–	5	14	4	–	–	7
		10		–		–	–		–		–	–	–	3	–	–	–	–	–	–		10	–	–	
		11		–		–	–		–		–	–	3	–	–	–	–	–	–	–		11	–	–	
		12†		–		–	–		–		–	–	–	1	–	–	–	–	–	–		12	–	–	
		13†		–		–	–		–		–	–	1	–	–	–	–	–	–	–		13	–	–	
Logic "0" Threshold Voltage	V_{OLA}	4	–	3.390	–	–	3.400	–	3.430	Vdc	–	–	–	–	–	–	–	–	–	5	14	4	–	–	7
		10	–		–	–		–			–	–	3	–	–	–	–	–	–	–		10	–	–	
		11	–		–	–		–			–	–	–	3	–	–	–	–	–	–		11	–	–	
		12†	–		–	–		–			–	–	1	–	–	–	–	–	–	–		12	–	–	
		13†	–		–	–		–			–	–	–	1	–	–	–	–	–	–		13	–	–	
Short Circuit Current	I_{SC}	6	-65	-20	-65	–	-20	-65	-20	mAdc	9	8	–	–	–	–	–	–	–	–	14	–	–	–	6,7

†Output Level to be measured after a clock pulse has been applied to the C input (pin 2) V_{IHmax} / V_{ILmin}

ELECTRICAL CHARACTERISTICS

Supply Voltage = -5.2 V

@ Test Temperature	TEST VOLTAGE/CURRENT VALUES													
	Volts											mA		
	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{IL}	V_{IH}	V_{IHH}	V_R	V_{IHT}	V_{ILT}	V_{EE}	I_L	I_{OL}	I_{OH}
0°C	-0.75	-1.870	-1.145	-1.51	-4.7	-2.8	+0.0	-0.7	-3.2	-4.4	-5.2	-2.5	16	-0.4
25°C	-0.72	-1.850	-1.105	-1.475	-4.7	-2.8	+0.0	-0.7	-3.2	-4.4	-5.2	-2.5	16	-0.4
75°C	-0.63	-1.830	-1.045	-1.450	-4.7	-2.8	+0.0	-0.7	-3.2	-4.4	-5.2	-2.5	16	-0.4

Characteristic	Symbol	Pin Under Test	MC12000 0°C Min	MC12000 0°C Max	MC12000 25°C Min	MC12000 25°C Typ	MC12000 25°C Max	MC12000 +75°C Min	MC12000 +75°C Max	Unit	TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{IL}	V_{IH}	V_{IHH}	V_R	V_{IHT}	V_{ILT}	V_{EE}	I_L	I_{OL}	I_{OL}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	7	–	–	–	90	117	–	–	mAdc	–	–	–	–	–	–	–	–	–	–	7	–	–	–	14
Input Current	I_{INH1}	1	–	–	–	–	200	–	–	µAdc	1	2	–	–	–	–	–	–	–	–	7	–	–	–	14
		2	–	–	–	–	200	–	–		2	1	–	–	–	–	–	–	–	–		–	–	–	
		3	–	–	–	–	200	–	–		3	–	–	–	–	–	–	–	–	–		–	–	–	
	I_{INH2}	5	–	40	–	–	40	–	40		–	–	–	–	–	–	5	–	–	–		–	–	–	
	I_{INH3}	8	–	–	1.4	–	3.6	–	–	mAdc	9	8	–	–	–	–	–	–	–	–		–	–	–	
		9	–	–	–	–	–	–	–		9	8	–	–	–	–	–	–	–	–		–	–	–	
	I_{INL1}	1	–	–	–	–	2.0	–	–	µAdc	–	–	–	–	–	–	–	–	–	–	1,7	–	–	–	14
	(Leakage	2	–	–	–	–	2.0	–	–		–	–	–	–	–	–	–	–	–	–	2,7	–	–	–	
	Current)	3	–	–	–	–	2.0	–	–		–	–	–	–	–	–	–	–	–	–	3,7	–	–	–	
	I_{INL2}	5	–	1.6	–	–	1.6	–	1.6	mAdc	–	–	–	–	5	–	–	–	–	–	7	–	–	–	
	I_{INL3}	8	–	–	2.0	–	5.0	–	–		8	9	–	–	–	–	–	–	–	–		–	–	–	
	I_{INL4}	9	–	–	0.8	–	2.0	–	–		8	9	–	–	–	–	–	–	–	–		–	–	–	
Logic "1" Output Voltage	V_{OH1}	4	-1.000	-0.75	-0.960	–	-0.72	-0.900	-0.63	Vdc	–	–	–	–	–	5	–	–	–	–	7	4	–	–	14
		10				–					–	3	–	–	–	–	–	–	–	–		10	–	–	
		11				–					3	–	–	–	–	–	–	–	–	–		11	–	–	
		12†				–					–	1	–	–	–	–	–	–	–	–		12	–	–	
		13†				–					1	–	–	–	–	–	–	–	–	–		13	–	–	
	V_{OH2}	6	-2.800	–	-2.800	–	–	-2.800	–	Vdc	9	8	–	–	–	–	–	–	–	–	7	–	–	6	14
Logic "0" Output Voltage	V_{OL1}	4	-1.99	-1.635	-1.95	–	-1.620	-1.93	-1.54	Vdc	–	–	–	–	5	–	–	–	–	–	7	4	–	–	14
		10				–					3	–	–	–	–	–	–	–	–	–		10	–	–	
		11				–					–	3	–	–	–	–	–	–	–	–		11	–	–	
		12†				–					1	–	–	–	–	–	–	–	–	–		12	–	–	
		13†				–					–	1	–	–	–	–	–	–	–	–		13	–	–	
	V_{OL2}	6	–	-4.700	–	–	-4.700	–	-4.700	Vdc	8	9	–	–	–	–	–	–	–	–	7	–	6	–	14
Logic "1" Threshold Voltage	V_{OHA}	4	-1.020	–	-0.980	–	–	-0.920	–	Vdc	–	–	–	–	–	–	–	–	5	–	7	4	–	–	14
		10		–		–	–		–		–	–	–	–	–	3	–	–	–	–		10	–	–	
		11		–		–	–		–		–	–	3	–	–	–	–	–	–	–		11	–	–	
		12†		–		–	–		–		–	–	–	–	–	1	–	–	–	–		12	–	–	
		13†		–		–	–		–		–	–	1	–	–	–	–	–	–	–		13	–	–	
Logic "0" Threshold Voltage	V_{OLA}	4	–	-1.615	–	–	-1.600	–	-1.575	Vdc	–	–	–	–	–	–	–	–	–	5	7	4	–	–	14
		10	–		–	–		–			–	–	3	–	–	–	–	–	–	–		10	–	–	
		11	–		–	–		–			–	–	–	3	–	–	–	–	–	–		11	–	–	
		12†	–		–	–		–			–	–	1	–	–	–	–	–	–	–		12	–	–	
		13†	–		–	–		–			–	–	–	1	–	–	–	–	–	–		13	–	–	
Short Circuit Current	I_{SC}	6	-65	-20	-65	–	-20	-65	-20	mAdc	9	8	–	–	–	–	–	–	–	–	6,7	–	–	–	14

†Output Level to be measured after a clock pulse has been applied to the C input (pin 2) V_{IHmax} / V_{ILmin}

AC ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	MC12000 0°C Min	0°C Max	+25°C Min	+25°C Typ	+25°C Max	+75°C Min	+75°C Max	Unit	TEST VOLTAGES/WAVEFORMS APPLIED TO PINS LISTED BELOW: Pulse Gen. 1	Pulse Gen. 2	Pulse Gen. 3	Pulse Out	V_{EE} -3.2 V or -3.0 V	V_{CC} +2.0 V
Propagation Delay (See Figure 4)	t_{2+13+}	2,13	–	–	–	2.4	3.5	–	–	ns	2	1	–	13	7	14
	t_{2+13-}	2,13	–	–	–	2.4	3.5	–	–	ns	2	1	–	13	7	14
	t_{2+12+}	2,12	–	–	–	2.4	3.5	–	–	ns	2	1	–	12	7	14
	t_{2+12-}	2,12	–	–	–	2.4	3.5	–	–	ns	2	1	–	12	7	14
	t_{3+11+}	3,11	–	–	–	1.5	2.5	–	–	ns	3	–	–	11	7	14
	t_{3-11-}	3,11	–	–	–	1.5	2.5	–	–	ns	3	–	–	11	7	14
	t_{3+10-}	3,10	–	–	–	1.5	2.5	–	–	ns	3	–	–	10	7	14
	t_{3-10+}	3,10	–	–	–	1.5	2.5	–	–	ns	3	–	–	10	7	14
	t_{5+4+}	5,4	–	–	–	3	4.5	–	–	ns	–	–	5	4	7	14
	t_{5-4-}	5,4	–	–	–	1.5	2.5	–	–	ns	–	–	5	4	7	14
	t_{9+6+}	9,6	–	–	–	8.0	12.0	–	–	ns	A	–	–	6	7	14
	t_{9-6-}	9,6	–	–	–	5.0	10.0	–	–	ns	A	–	–	6	7	14
Output Rise Time (See Figure 4)	t_{13+}	13	–	–	–	2.8	3.5	–	–	ns	2	1	–	13	7	14
	t_{12+}	12	–	–	–	2.8	↓	–	–	ns	2	1	–	12	7	14
	t_{11+}	11	–	–	–	2.0		–	–	ns	3	–	–	11	7	14
	t_{10+}	10	–	–	–	2.0		–	–	ns	3	–	–	10	7	14
	t_{4+}	4	–	–	–	2.4		–	–	ns	–	–	5	4	7	14
Output Fall Time (See Figure 4)	t_{13-}	13	–	–	–	2.8	3.5	–	–	ns	2	1	–	13	7	14
	t_{12-}	12	–	–	–	2.8	↓	–	–	ns	2	1	–	12	7	14
	t_{11-}	11	–	–	–	2.0		–	–	ns	3	–	–	11	7	14
	t_{10-}	10	–	–	–	2.0		–	–	ns	3	–	–	10	7	14
	t_{4-}	4	–	–	–	2.4		–	–	ns	–	–	5	4	7	14
Setup Time (See Figure 5)	$t_{setup"1"}$	13	–	–	–	0.2	–	–	–	ns	2	1	–	–	7	14
	$t_{setup"0"}$	13	–	–	–	0.7	–	–	–	ns	2	1	–	–	7	14
Hold Time (See Figure 5)	$t_{hold"1"}$	13	–	–	–	0.0	–	–	–	ns	2	1	–	–	7	14
	$t_{hold"0"}$	13	–	–	–	1.0	–	–	–	ns	2	1	–	–	7	14
Toggle Frequency (See Figure 6)	f_{tog}	13	200	–	200	250	–	200	–	MHz	–	–	–	–	7	14

FIGURE 2 — TYPICAL DIGITAL MIXER

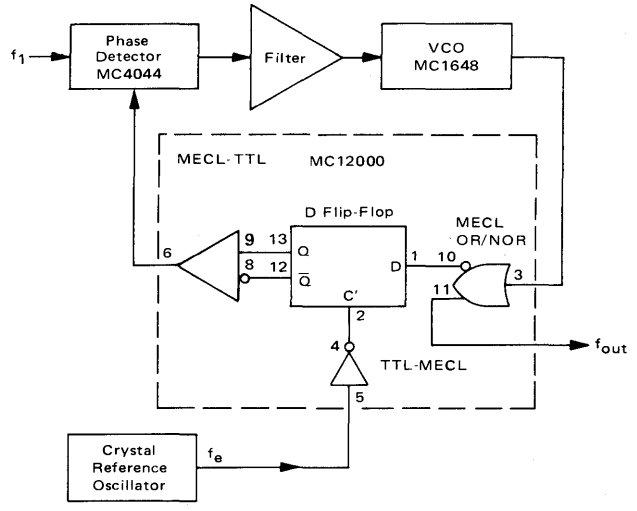


FIGURE 3 — SWITCHING TIME TEST CIRCUIT

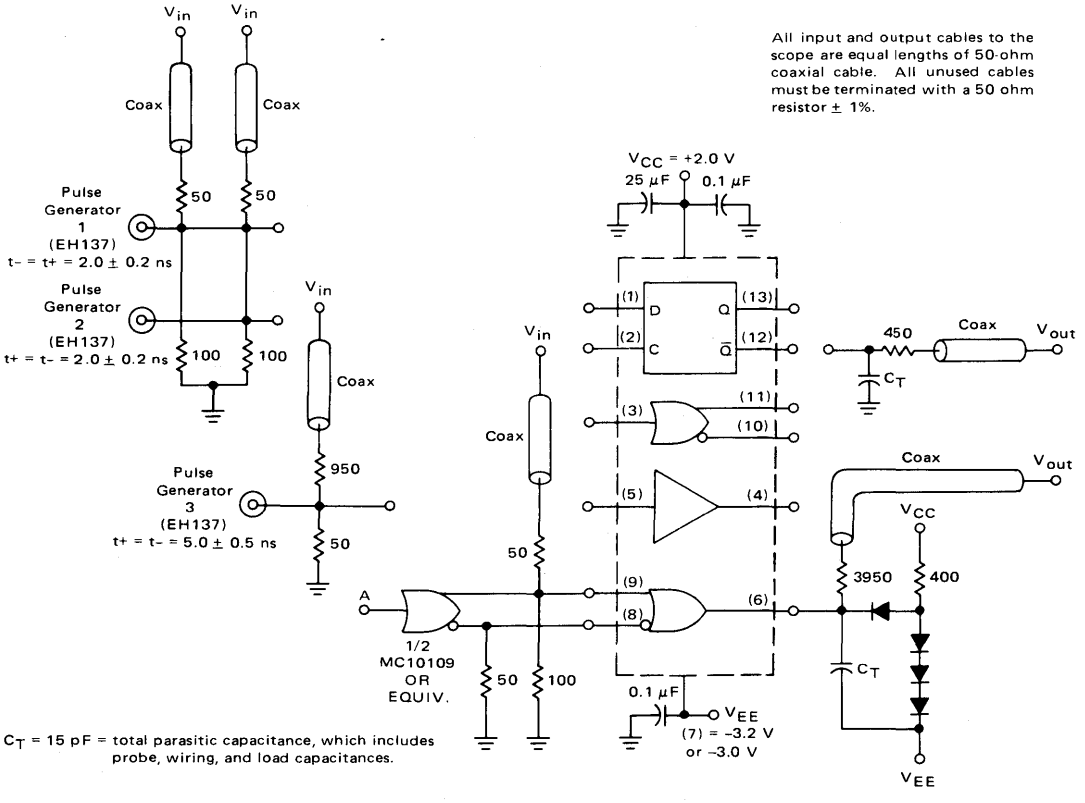
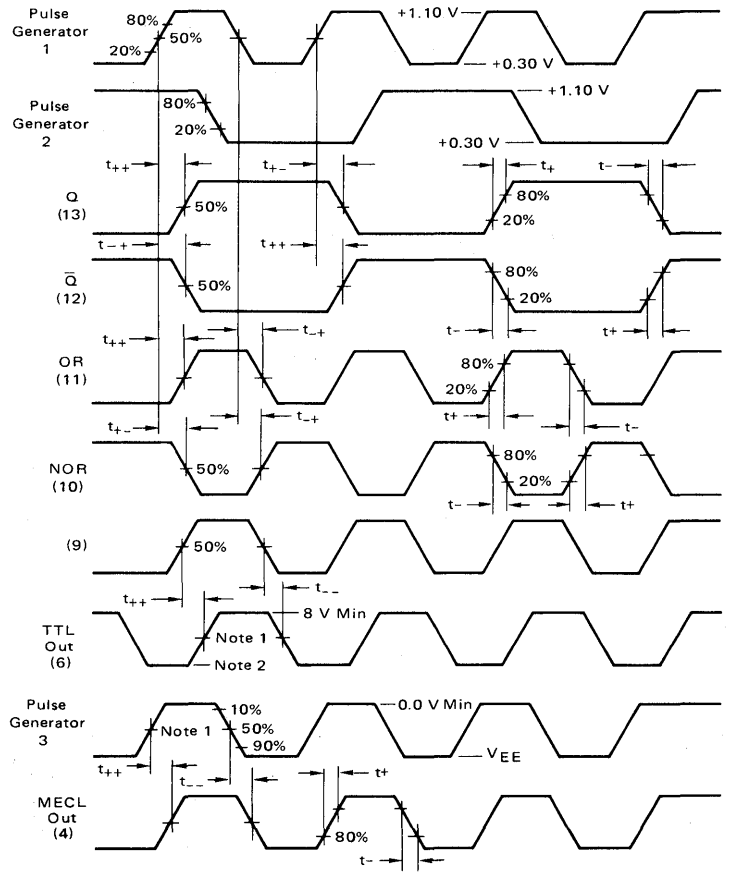


FIGURE 4 — AC TEST VOLTAGE WAVEFORMS



NOTES:
1. V_{EE} + 1.5 V
2. V_{EE} + 0.5 V max

FIGURE 5 — SETUP AND HOLD TIME WAVEFORMS (See Figure 3)

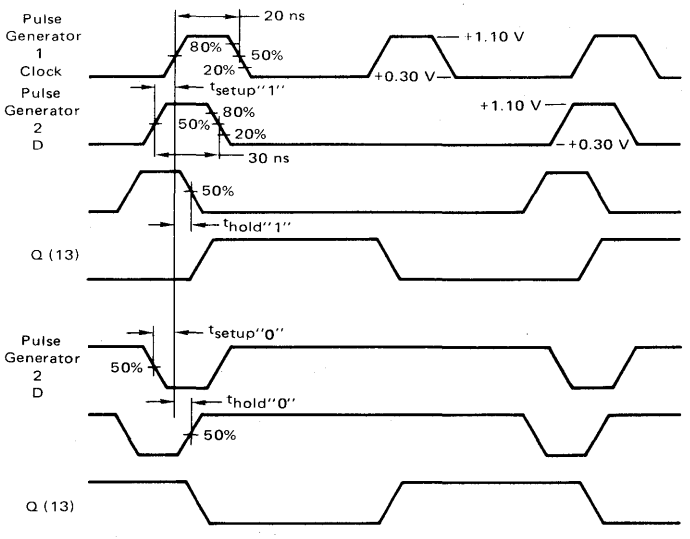
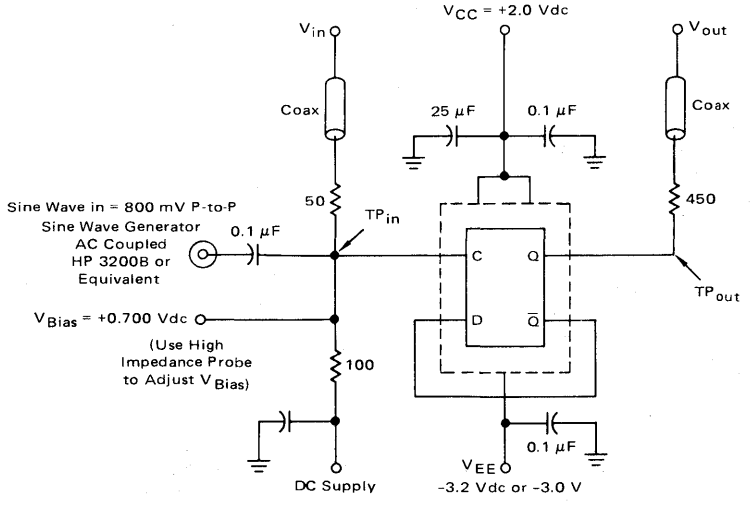


FIGURE 6 — TOGGLE FREQUENCY TEST CIRCUIT



The maximum Toggle Frequency of MC12000 has been exceeded when either:

1. The output Peak-to-Peak voltage swing falls below 600 mV

   or

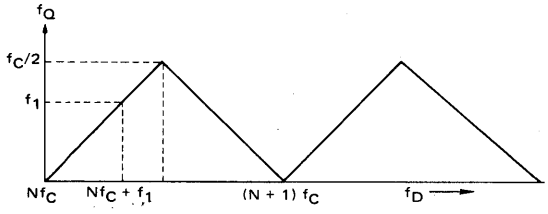
2. The devices cease to Toggle (divide by 2).

MC12000 DIGITAL MIXER

This device is a digital mixer designed to operate with logic levels at its input and output ports. In operation it is an MECL type "D" flip-flop with level translators to and from TTL to accomodate most interfacing demands. Output frequency (f_Q) as a function of "D" and clock inputs is shown in Figure 7. It can be seen that either direct or harmonic mixing may be employed, that is, f_Q may be either the difference between f_D and f_C or the difference between f_D and the Nth harmonic of f_C.

One particular advantage of mixing in phase locked loops (PLL) is that lower frequencies may be generated for use in portions of the circuit where digital processing is done (with divide-by-P network and/or phase detector). Lower frequency operation often reduces overall system cost since a less expensive logic form may be utilized. However use of the mixing technique is not a panacea for all VHF applications and the design of such synthesizer systems must be approached with care.

FIGURE 7



Use of the MC12000 in a non-harmonic PLL is straightforward (Figure 8). Output frequency is the sum of both input quantities ($f_1 + f_C$) as long as f_1 is less than $f_C/2$ (See Figure 7), since f_Q can go no higher than that. Unless VCO output range is restricted somewhat there is a chance also that the loop may operate at the second harmonic of f_C. This problem is minimal in the loop of Figure 8, however, since the output frequency would have to vary more than 2:1.

Mixing is used because the digital phase detector has an upper frequency limit of about 10 MHz and many loops require direct locks at 20 MHz or more. Direct down-mixing does not change any loop characteristics except the sampling rate which restricts loop natural frequency to about $f_C/10$ in practical circuits. Although output frequency may be changed by varying either f_1 or f_C, the clock input is usually crystal controlled since it is of the same magnitude as f_D and more difficult to stabilize.

FIGURE 8

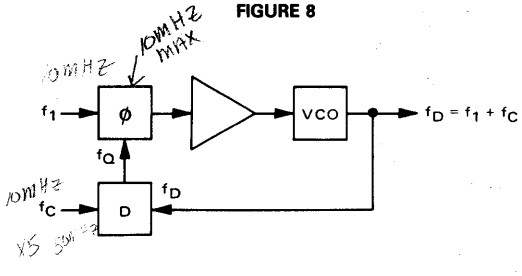
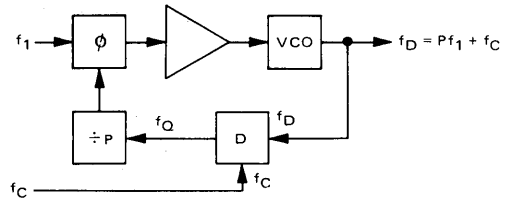


FIGURE 9



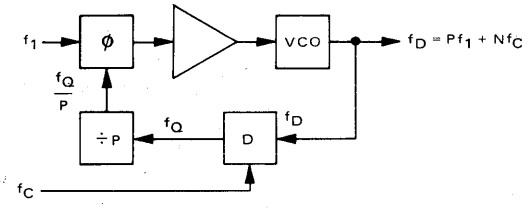
Combining a standard synthesis configuration with the mixer yields a circuit capable of high frequency operation at low cost (Figure 9), if the output frequency range is relatively small ($P_{max} - P_{min}$) $f_1 < f_C/2$. In fact the choice of harmonic or non-harmonic mixing is largely based on the availability of a suitable crystal or other reference source for f_C versus the needed frequency coverage. Considering all the restrictions on f_C, its value (and the maximum harmonic number N) are dictated by the following expressions:

$$N < \frac{f_{D(min)} - f_1}{2\,\Delta f_D} \quad (1)$$

$$N_{fc} = f_{D(min)} - f_1 \quad (2)$$

where Δf_D = change in output frequency.

FIGURE 10



Using Equations (1) and (2) above the minimum value of f_C may be found for the circuit of Figure 10 and still get adequate frequency coverage. In this minimum configuration all necessary output frequencies may be generated by programming the "P" count string. But the divide number might bear no obvious relation to the output frequency such as often happens with non-mixing synthesizers.

DESIGN EXAMPLES

Example #1

Output Frequency: 48-54 MHz
Frequency Increments: 10 kHz
Using Equations (1) and (2), a minimum frequency (f_C) version can be designed:

$$f_1 = \text{increment} = 10\ \text{kHz}$$

$$N < \frac{48\ \text{MHz} - 10\ \text{kHz}}{2\ (54\text{-}48)\ \text{MHz}}$$

$$N < 4$$

Let N = 3

$$Nf_C = 47.99\ \text{MHz}$$

$$f_C = \frac{Nf_C}{N} = \frac{47.99}{3} = 15.99666\ \text{MHz}$$

$$f_C = 15.996666\ \text{MHz}$$

$$P_{min} = 1$$

$$P_{max} = \frac{\Delta f_D}{10\ \text{kHz}} + P_{min} \qquad (3)$$

$$P_{max} = \frac{6\ \text{MHz}}{10\ \text{kHz}} + P_{min}$$

$$P_{max} = 601$$

$$f_{Q(max)} = P_{max}\, f_1 = 6.01\ \text{MHz} \qquad (4)$$

Equation (4) above puts the divider string (divide-by-P) into a medium frequency situation where devices such as the MC4016/4316 may be utilized. Note that the divider number now indicates the channel selected rather than output frequency. That is, at f_D = 48.000 MHz, P = 1; at f_D = 54.000 MHz, P = 601.

If "proper" divide-by-P readings are desired for direct frequency readout a slight circuit modification is necessary. To enable a division at 48.000 MHz the first divide-by-P must be 100 rather than 1, and P_{max} would then be 700 to cover all 6 MHz. Recalculating $f_{Q(max)}$ from Equation 4 we still find that the 7 MHz maximum value allows use of the same components. The next question concerns the allowable range of f_Q in relation to f_C ($f_Q < f_C/2$). Since f_C is nearly 16 MHz, the range of f_Q can be contained. A cosmetic change to the most significant digit switch completes the design. Instead of reading 1 through 7 it must be modified to display 48 through 54.

Example #2

Output Frequency: 144-148 MHz
Frequency Increments: 10 kHz

$$f_1 = \text{increment} = 10\ \text{kHz}$$

$$N < \frac{144.00 - 0.01}{2\ (4)}$$

$$N < 18$$

Let N = 17

$$Nf_C = 144.00 - 0.01\ \text{MHz} = 143.99$$

$$f_C = \frac{Nf_C}{N} = 8.470\ \text{MHz}$$

$$P_{min} = 1$$

$$P_{max} = \frac{4\ \text{MHz}}{10\ \text{kHz}} + 1 = 401$$

$$f_{Q(max)} = P_{max}\, f_1 = 4.01\ \text{MHz}$$

Maximum frequency seen by the divide-by-P chain is still well within the MC4016 rating.

When converting this synthesizer to one that needs frequency directly, a "1" is again added to the most significant digit (MSD). This results in a P_{min} of 100 to P_{max} of 500. In this example, however, $f_{Q(max)}$ is 5 MHz which easily exceeds $f_C/2$. To alleviate this difficulty, the "N" factor must be decreased in order to raise f_C to at least 10 MHz.

$$N < \frac{f_{D(min)} - f_1}{f_C}$$

Let f_C = 10 MHz

$$N < \sim 14.4$$

Let N = 14

$$Nf_C = 143.99\ \text{(from above)}$$

$$f_C = \frac{Nf_C}{N} = \frac{143.99}{14}$$

$$f_C = 10.28540\ \text{MHz} \qquad (5)$$

7

VCO RANGE RESTRICTIONS

As in all harmonically locked PLL's, it is possible for the loop to lock on the wrong harmonic if there is too wide a range in the VCO. This situation is shown in Figure 11 where the possible false lock areas are indicated near the (N − 1) and (N + 1) harmonic points. The problem of VCO restraint however is more than just making sure that output frequency f_D isn't able to go to B or A' (the closest false lock points). Actual operating limits are C and C', symmetrically placed frequencies corresponding to $f_{D(min)}$ about Nf_C and $f_{D(max)}$ about $(Nf+1/2)\ f_C$. If the VCO drops below C while the feedback counter is at P_{min} the phase detector will try to push f_D even lower, toward the stable condition at A (Figure 12). Likewise, at C' (when $P = P_{max}$) the tendency is for the loop to accelerate toward lockup at B' (Figure 13). When C or C' are exceeded the loop will "hang up" and not attain the proper lock.

FIGURE 11

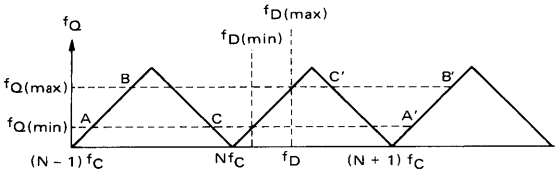


FIGURE 12

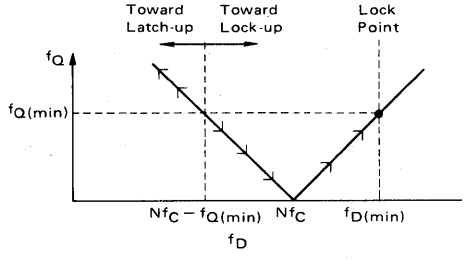
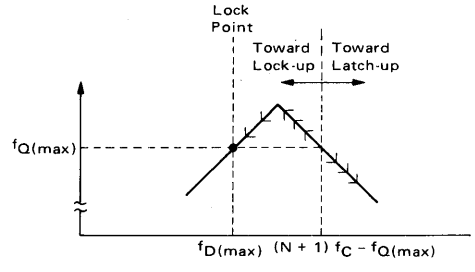
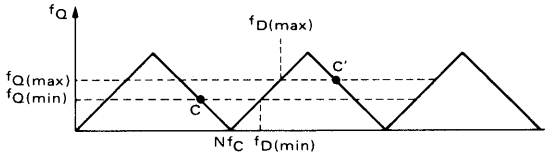


FIGURE 13



The VCO frequency constraints may be quite severe if the minimum f_C formulation is followed and the Nth harmonic is quite high. Where VCO constraint may pose a problem, decrease N below the maximum indicated by Equation (1) until sufficient room is generated by placing the operating range of f_Q on only a small part of the f_D slope (Figure 14). Note that f_C goes up as we approach the more idealized case (Equation 5).

FIGURE 14



The most likely reasons for a "latched up" state in a harmonic loop are turn-on transients and loop overshoot when changing frequency abruptly from one end of the range to the other.

SUMMARY OF SYNTHESIS PROCEDURE

1. Compute harmonic number N

$$N < \frac{f_{D(min)} - f_1}{2\,\Delta f_D}$$

where Δf_D = change in output frequency
f_1 = channel spacing

2. Compute minimum mixing frequency f_C

$$f_C = \frac{f_{D(min)} - f_1}{N}$$

3. Calculate feedback divider's maximum value

$$P_{max} = \frac{\Delta f_D}{f_1} + P_{min}$$

where $P_{min} = 1$ for minimum f_C.

4. Find maximum divide-by-P frequency

$$f_{Q(max)} = \Delta f_D + f_1$$

5. Calculate allowable VCO swing

$$Nf_C - f_1 < f_{VCO} < (N + 1)\,f_C - f_{Q(max)}$$

6. If the above constraints are too tight choose the next lower number for N and repeat steps 2 and 5 until satisfied.

7

SKIP-LOCK TUNING

Harmonic mixing provides an alternate means to frequency synthesis without the feedback divide-by-P network. In this instance the design objective is to provide a large frequency coverage with a set (and relatively wide) channel spacing. The configuration is identical to a single frequency PLL (Figure 15) except it operates in the harmonic mode and tuning is accomplished at the VCO. Output frequency is fixed as being f_1 above all harmonics of f_C. As the VCO is tuned through its range, the loop will acquire and lose signals spaced f_C apart. Since there must be some frequency for the phase detector to operate with, the output frequency cannot be a direct harmonic of f_C. This facet of the circuit often causes users to refer to f_1 as the "offset" frequency.

The value of f_1 is often dictated by output frequency and channel spacing requirements. However the relationship of f_1 to f_C has a large effect on the tunability both up and down the frequency range. If, for example, the loop were locked at point A (Figure 16) and B were the next desired point, then the VCO must be "dragged" from A to A' before lock can be achieved. This frequency adjustment may be quite critical since the frequency difference between A' and B is only $2f_1$. If the VCO is tuned past B the opportunity for lock has been passed.

On the other hand, in going from B to A, the upper end of the VCO control range must only cross A' before the loop acquires frequency A. In either case it's apparent that the loop will not "jump" from one lock point to another and some indication of loop lock should be added. This is normally done by monitoring the VCO dc control line with a pair of comparators and noting when the line reaches its limits.

FIGURE 15

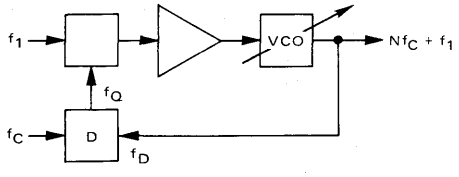
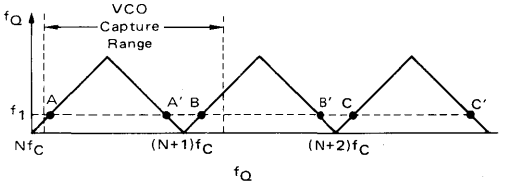


FIGURE 16



MOTOROLA

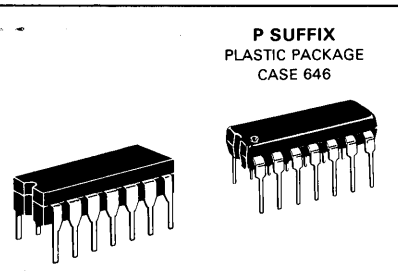
MC12002/ MC12502

ANALOG MIXER

The MC12002/MC12502 is a double balanced analog mixer, including an input amplifier feeding the mixer carrier port and a temperature compensated bias regulator. The input circuits for both the amplifier and mixer are differential amplifier circuits. The on-chip regulator provides all of the required biasing.

This circuit is designed for use as a balanced mixer in high-frequency wide-band circuits. Other typical applications include suppressed carrier and amplitude modulation, synchronous AM detection, FM detection, phase detection, and frequency doubling, at frequencies up to UHF.

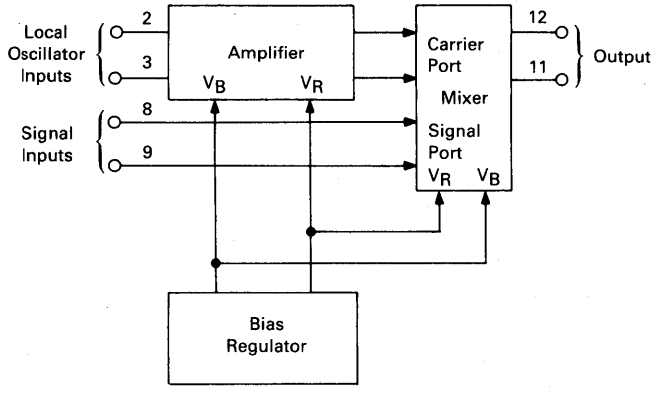
ANALOG MIXER



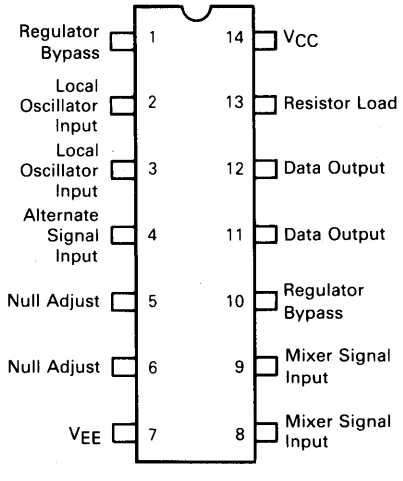
P SUFFIX
PLASTIC PACKAGE
CASE 646

L SUFFIX
CERAMIC PACKAGE
CASE 632-02

LOGIC DIAGRAM



PIN ASSIGNMENT



7

ELECTRICAL CHARACTERISTICS

	TEST VOLTAGE VALUES (Volts)		
	V_{IHmax}	V_{ILmin}	V_{CC}
MC12502	+2.9	+2.0	+5.0
MC12002	+2.9	+2.0	+5.0

Characteristic	Symbol	Pin Under Test	MC12502 Test Limits							MC12002 Test Limits							VOLTAGE APPLIED TO PINS LISTED BELOW			
			−55°C		+25°C		+125°C			−30°C		+25°C		+85°C						
			Min	Max	Min	Max	Min	Max	Unit	Min	Max	Min	Max	Min	Max	Unit	V_{IHmax}	V_{ILmin}	V_{CC}	Gnd
Power Supply Drain	I_{CC}	14	–	–	–	16	–	–	mAdc	–	–	–	16	–	–	mAdc	–	–	11,12,14	5,6,7
Input Current	I_{inH}	2	–	–	–	0.75	–	–	mAdc	–	–	–	0.75	–	–	mAdc	2	–	11,12,14	5,6,7
		3	–	–	–	0.75	–	–	mAdc	–	–	–	0.75	–	–	mAdc	3	–	11,12,14	5,6,7
		8	–	–	–	0.75	–	–	mAdc	–	–	–	0.75	–	–	mAdc	8	–	11,12,14	5,6,7
		9	–	–	–	0.75	–	–	mAdc	–	–	–	0.75	–	–	mAdc	9	–	11,12,14	5,6,7
	I_{inL}	2	–	–	−0.7	–	–	–	mAdc	–	–	−0.7	–	–	–	mAdc	–	2	11,12,14	5,6,7
		3	–	–	−0.7	–	–	–	mAdc	–	–	−0.7	–	–	–	mAdc	–	3	11,12,14	5,6,7
		8	–	–	−0.7	–	–	–	mAdc	–	–	−0.7	–	–	–	mAdc	–	8	11,12,14	5,6,7
		9	–	–	−0.7	–	–	–	mAdc	–	–	−0.7	–	–	–	mAdc	–	9	11,12,14	5,6,7
Output Current	IO_1	11	–	–	0.7	1.3	–	–	mAdc	–	–	0.7	1.3	–	–	mAdc	–	–	11,12,14	7
		12	–	–	0.7	1.3	–	–	mAdc	–	–	0.7	1.3	–	–	mAdc	–	–	11,12,14	7
	IO_2	11	–	–	2.1	3.9	–	–	mAdc	–	–	2.1	3.9	–	–	mAdc	–	–	11,12,14	5,6,7
		12	–	–	2.1	3.9	–	–	mAdc	–	–	2.1	3.9	–	–	mAdc	–	–	11,12,14	5,6,7
	I_{out}	11	–	–	4.2	7.8	–	–	mAdc	–	–	4.2	7.8	–	–	mAdc	2,9	–	11,12,14	5,6
		11	–	–	4.2	7.8	–	–	mAdc	–	–	4.2	7.8	–	–	mAdc	3,8	–	11,12,14	5,6
		12	–	–	4.2	7.8	–	–	mAdc	–	–	4.2	7.8	–	–	mAdc	2,8	–	11,12,14	5,6
		12	–	–	4.2	7.8	–	–	mAdc	–	–	4.2	7.8	–	–	mAdc	3,9	–	11,12,14	5,6
Differential Current	ΔIO_1	11,12	−50	+50	−50	+50	−50	+50	µAdc	−100	+100	−100	+100	−100	+100	µAdc	–	–	11,12,14	7
	ΔIO_2	11,12	−100	+100	−100	+100	−100	+100	µAdc	−200	+200	−200	+200	−200	+200	µAdc	–	–	11,12,14	5,6,7
Bias Voltage	V_{Bias}	1	2.34	2.54	2.32	2.52	2.29	2.49	Vdc	2.33	2.53	2.32	2.52	2.30	2.50	Vdc	–	–	11,12,14	5,6,7
		4	390	590	400	600	420	620	mVdc	390	590	400	600	410	610	mVdc	–	–	11,12,14	5,6,7
		5	275	415	285	425	305	445	mVdc	275	415	285	425	295	435	mVdc	–	–	11,12,14	7
		6	275	415	285	425	305	445	mVdc	275	415	285	425	295	435	mVdc	–	–	11,12,14	7
		10	1.300	1.500	1.185	1.385	1.050	1.250	Vdc	1.260	1.460	1.185	1.385	1.105	1.305	Vdc	–	–	11,12,14	5,6,7
																	Pulse In	Pulse Out	−3.0 V	Gnd	V_{EE}
AC Gain (See Figure 1)	A_V	11	–	–	6.0	–	–	–	V/V	–	–	5.0	–	–	–	V/V	2	11	9	14	7
(Frequency = 100 MHz) *Note		11	–	–	0.33	–	–	–	V/V	–	–	0.28	–	–	–	V/V	8	11	3	14	7

*Note: AC Gain is a function of collector load impedance.

ANALOG MIXER CIRCUIT SCHEMATIC

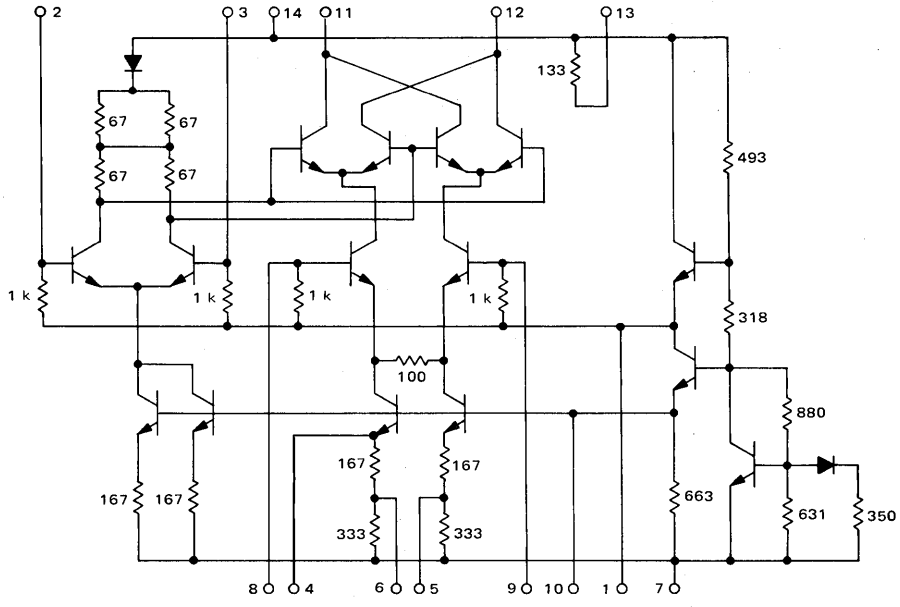
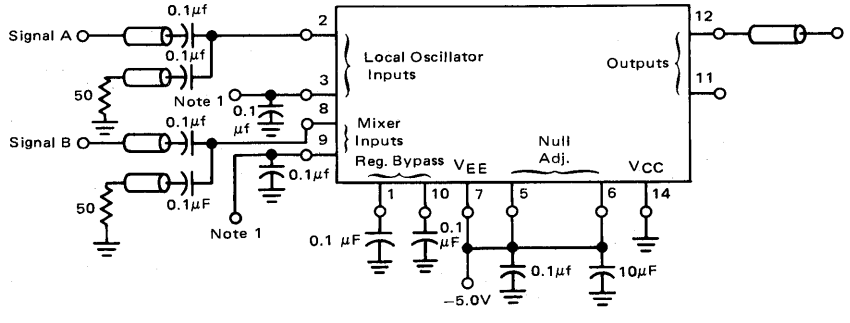


FIGURE 1 — A.C. GAIN TEST



Note 1:
V_{IL} = −3.0 V on pin 3 when pin 8 is under test.
V_{IL} = −3.0 V on pin 9 when pin 2 is under test.

Signal A = 30 mV p-p

Signal B = 300 mV p-p

Freq. = 100 MHz

All input and output cables to the scope are equal lengths of 50-ohm coaxial cable.
The unused output is connected to a 50-ohm resistor to ground.

7

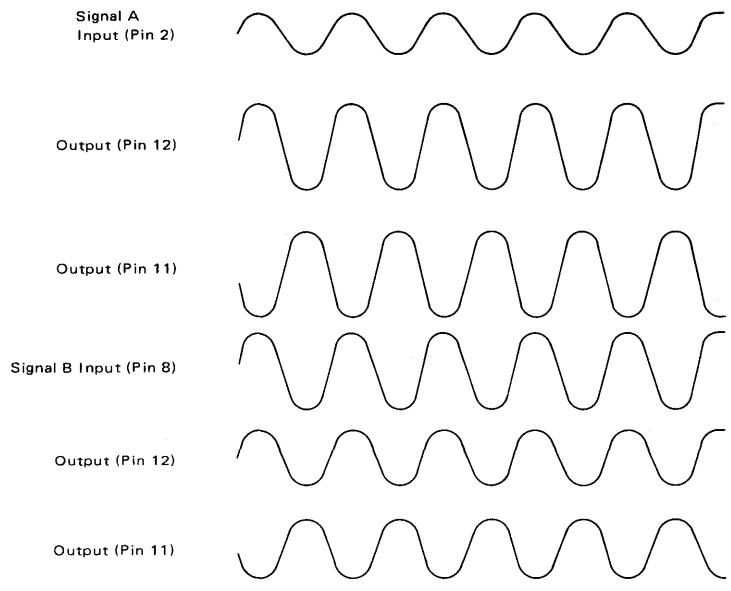
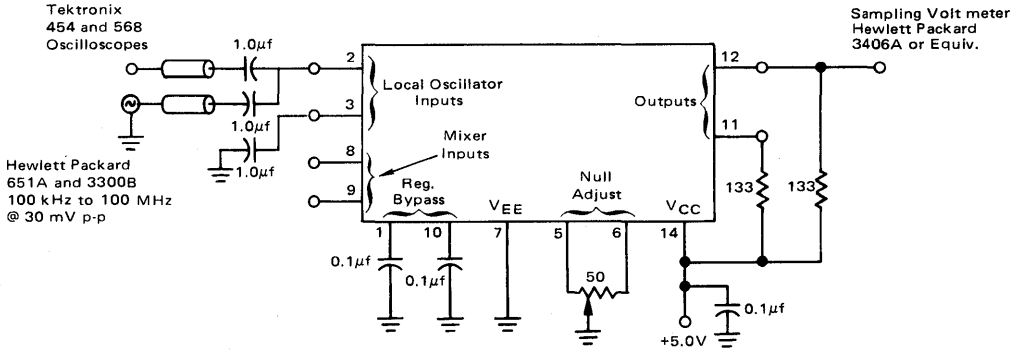


FIGURE 2 — CARRIER FEEDTHROUGH TEST CIRCUITS



Notes:
Test 1—Adjust potentiometer for carrier null at f_c = 100 kHz.
Test 2—Connect pins 5 and 6 to Gnd.

All input and output cables to the scope are equal lengths of 50-ohm coaxial cable.

FIGURE 3 — CARRIER FEEDTHROUGH VERSUS FREQUENCY (Test 1)

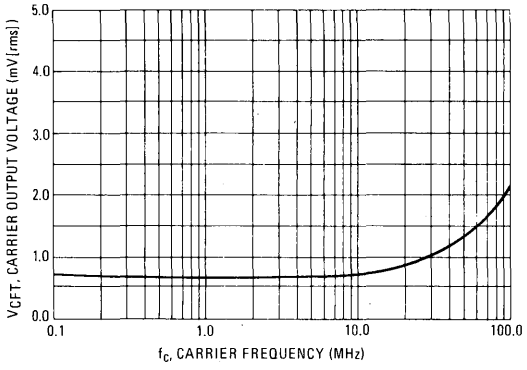


FIGURE 4 — CARRIER FEEDTHROUGH VERSUS FREQUENCY (Test 2)

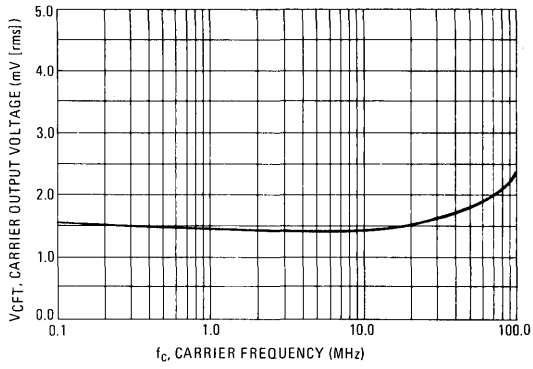
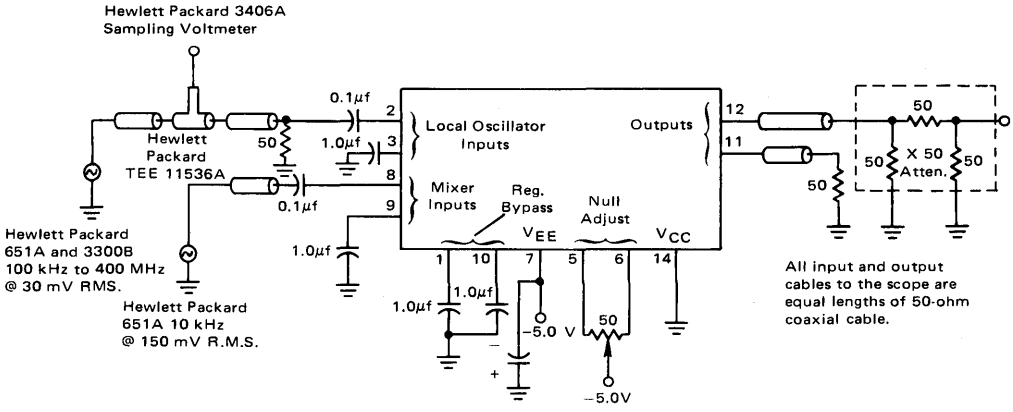


FIGURE 5 — CARRIER SUPPRESSION TEST CIRCUIT



Notes:
Test 1 — Adjust potentiometer for carrier null @ f_c = 100 kHz
Test 2 — Connect pins 5 and 6 to −5.0 volts
Test 3 — Adjust potentiometer for carrier null @ 25°C

FIGURE 6 — CARRIER SUPPRESSION VERSUS FREQUENCY (Test 1)

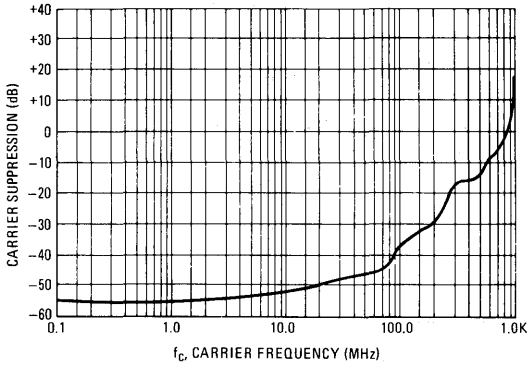
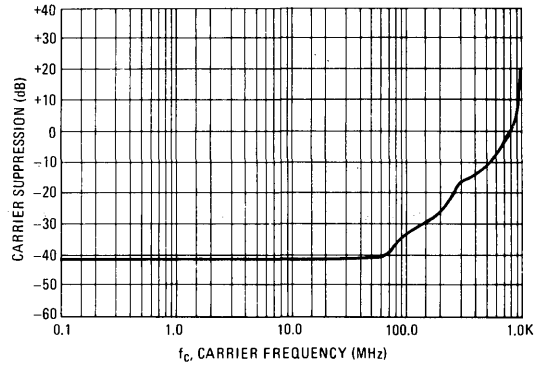


FIGURE 7 — CARRIER SUPPRESSION VERSUS FREQUENCY (Test 2)



7

FIGURE 8 — CARRIER SUPPRESSION VERSUS TEMPERATURE

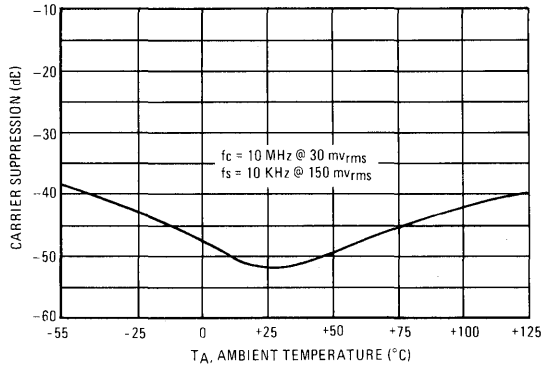
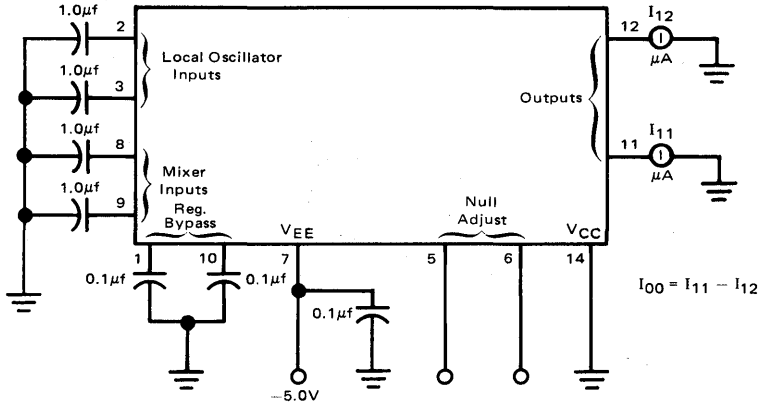


FIGURE 9 — OUTPUT OFFSET CURRENT (I_{00}) VERSUS TEMPERATURE



Notes:
Test 1 — Pins 5 and 6 left open
Test 2 — Pins 5 and 6 are tied to −5.0 volts

FIGURE 10 — OUTPUT OFFSET CURRENT VERSUS TEMPERATURE

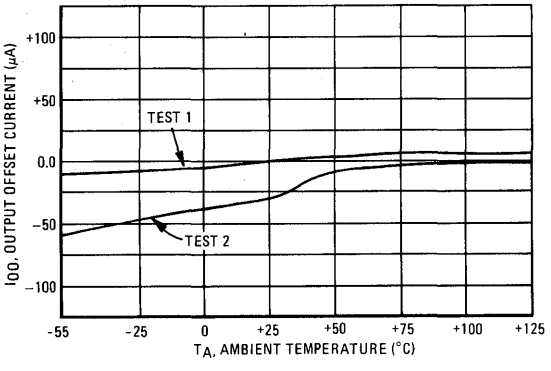
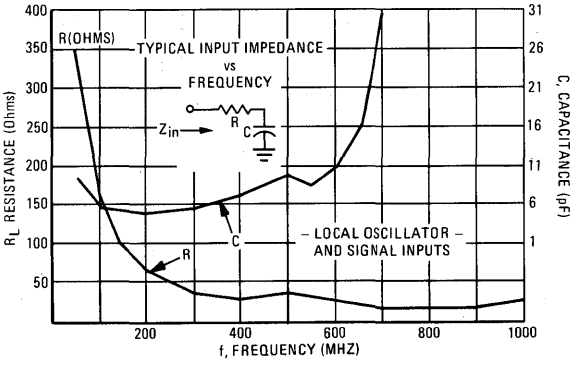


FIGURE 11 — TYPICAL INPUT IMPEDANCE VERSUS FREQUENCY (NO CIRCUIT)



7

MOTOROLA

MC12009 MC12509
MC12011 MC12511
MC12013 MC12513

TWO-MODULUS PRESCALER

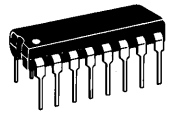
These devices are two-modulus prescalers which will divide by 5 and 6, 8 and 9, and 10 and 11, respectively. A MECL-to-TTL translator is provided to interface directly with the MC12014 Counter Control Logic. In addition, there is a buffered clock input and MECL bias voltage source. Details of operation are on the MC12012 data sheet.

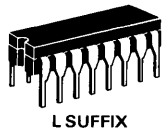
- 600 MHz (Typ) Toggle Frequency
- MC12009 (÷5/6), MC12011 (÷8/9), MC12013 (÷10/11)
- MECL to TTL Translator on Chip
- MECL and TTL Enable Inputs
- +5.0 or −5.2 V Operation*
- Buffered Clock Input — Series Input RC Typ, 20 Ohms and 4 pF
- V_{BB} Reference Voltage
- 310 Milliwatts (Typ)

*When using +5.0 V supply, apply +5.0 V to pin 1 (V_{CCO}), pin 6 (TTL V_{CC}), pin 16 (V_{CC}), and ground pin 8 (V_{EE}). When using −5.2 V supply, ground pin 1 (V_{CCO}), pin 6 (TTL V_{CC}), and pin 16 (V_{CC}) and apply −5.2 V to pin 8 (V_{EE}). If the translator is not required, pin 6 may be left open to conserve dc power drain.

TWO-MODULUS PRESCALER

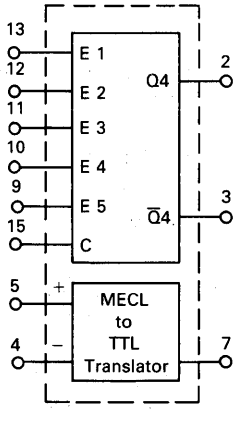
P SUFFIX
PLASTIC PACKAGE
CASE 648





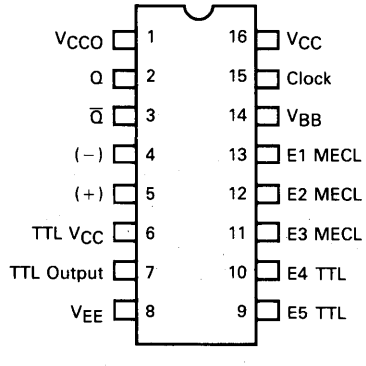
L SUFFIX
CERAMIC PACKAGE
CASE 620

LOGIC DIAGRAM



V_{CCO} = pin 1
V_{CC} = pin 16
V_{EE} = pin 8

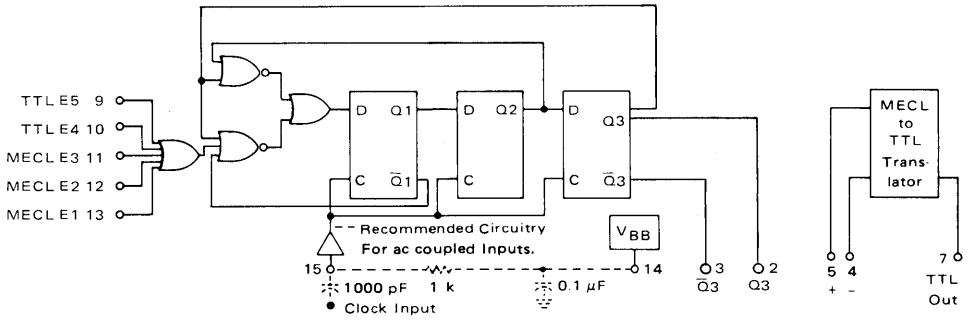
PIN ASSIGNMENT



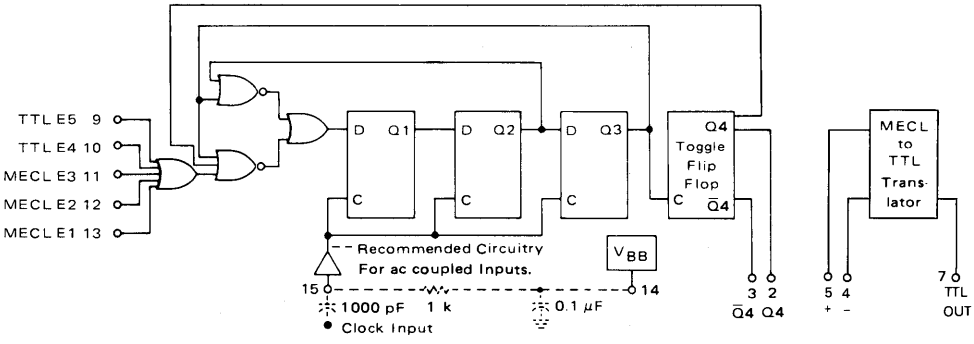
7

LOGIC DIAGRAMS

MC12009

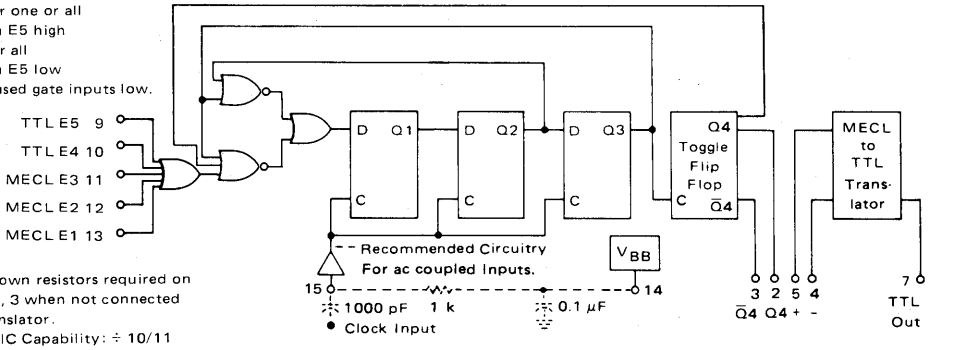


MC12011



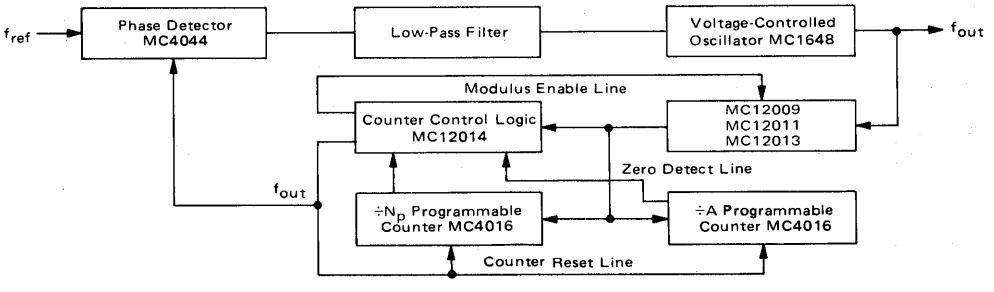
MC12013

÷ 10 for one or all
E1 thru E5 high
÷ 11 for all
E1 thru E5 low
Tie unused gate inputs low.



Pull-down resistors required on Pins 2, 3 when not connected to translator.
Basic IC Capability: ÷ 10/11

FIGURE 2 — TYPICAL FREQUENCY SYNTHESIZER APPLICATION



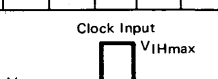
ELECTRICAL CHARACTERISTICS ..... Supply Voltage −5.2 V

These devices are designed to meet the dc specifications shown in the test table after thermal equilibrium has been established. Outputs are terminated through a 50-ohm resistor to −2.0 Vdc.

@Test Temperature	TEST VOLTAGE/CURRENT VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{IH}	V_{IL}	V_{IHT}	V_{ILT}	V_{EE}	(mA) I_L	I_{OL}	I_{OH}
-30°C	-0.890	-1.990	-1.205	-1.500	-2.8	-4.7	-3.2	-4.4	-5.2	-0.25	16	-0.40
+25°C	-0.810	-1.950	-1.105	-1.475	-2.8	-4.7	-3.2	-4.4	-5.2	-0.25	16	-0.40
+85°C	-0.700	-1.925	-1.035	-1.440	-2.8	-4.7	-3.2	-4.4	-5.2	-0.25	16	-0.40

Characteristic	Symbol	Pin Under Test	MC12009, MC12011, MC12013 -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{IH}	V_{IL}	V_{IHT}	V_{ILT}	V_{EE}	I_L	I_{OL}	I_{OH}	Gnd
Power Supply Drain Current	I_{CC1}	8	-88	–	-80	–	–	-80	–	mAdc	–	–		–	–	–	–	–	8	–	–	–	1,16
	I_{CC2}	6	–	5.2	–	–	5.2	–	5.2	mAdc	4	5	–	–	–	–	–	–	8	–	–	–	6
Input Current	I_{INH1}	15	–	375	–	–	250	–	250	μAdc	15	–	–	–	–	–	–	–	8	–	–	–	1,16
		11	–	↓	–	–	↓	–	↓	↓	11	–	–	–	–	–	9,10	–	↓	–	–	–	↓
		12	–		–	–		–			12	–	–	–	–	–	9,10	–		–	–	–	
		13	–		–	–		–			13	–	–	–	–	–	9,10	–		–	–	–	
	I_{INH2}	4	1.7	6.0	2.0	–	6.0	2.0	6.4	mAdc	5	4	–	–	–	–	–	–	8	–	–	–	6
		5	1.7	6.0	2.0	–	6.0	2.0	6.4	mAdc	5	4	–	–	–	–	–	–	8	–	–	–	6
	I_{INH3}	5	0.7	3.0	1.0	–	3.0	1.0	3.6	mAdc	4	5	–	–	–	–	–	–	8	–	–	–	6
	I_{INH4}	9	–	–	100	–	100	–	100	μAdc	–	–	–	–	9	–	–	–	8	–	–	–	1,16
		10	–	–	100	–	100	–	100	μAdc	–	–	–	–	10	–	–	–	8	–	–	–	1,16
Leakage Current	I_{INL1}	15	-10	–	-10	–	–	-10	–	μAdc	–	–	–	–	–	–	–	–	8,15	–	–	–	1,16
		11	↓	–	↓	–	–	↓	–	↓	–	–	–	–	–	–	–	–	8,11	–	–	–	↓
		12		–		–	–		–		–	–	–	–	–	–	–	–	8,12	–	–	–	
		13		–		–	–		–		–	–	–	–	–	–	–	–	8,13	–	–	–	
	I_{INL2}	9	-1.6	–	-1.6	–	–	-1.6	–	mAdc	–	–	–	–	–	9	–	–	8	–	–	–	1,16
		10	-1.6	–	-1.6	–	–	-1.6	–	mAdc		–	–	–	–	10	–	–	8	–	–	–	1,16
Reference Voltage	V_{BB}	14	–	–	-1.360	–	-1.160	–	–	Vdc	–	–	–	–	–	–	–	–	8	14	–	–	1,16
Logic "1" Output Voltage	V_{OH1} ①	2	-1.100	-0.890	-1.000	–	-0.810	-0.930	-0.700	Vdc	–	11,12,13	–	–	–	9,10	–	–	8	–	–	–	1,16
		3	-1.100	-0.890	-1.000	–	-0.810	-0.930	-0.700	Vdc	–	11,12,13	–	–	–	9,10	–	–	8	–	–	–	1,16
	V_{OH2}	7	-2.8	–	-2.6	–	–	-2.4	–	Vdc	5	4	–	–	–	–	–	–	8	–	–	7	6
Logic "0" Output Voltage	V_{OL1} ①	2	-1.990	-1.675	-1.950	–	-1.650	-1.925	-1.615	Vdc	–	11,12,13	–	–	–	9,10	–	–	8	–	–	–	1,16
		3	-1.990	-1.675	-1.950	–	-1.650	-1.925	-1.615	Vdc	–	11,12,13	–	–	–	9,10	–	–	8	–	–	–	1,16
	V_{OL2}	7	–	-4.26	–	–	-4.40	–	-4.48	Vdc	4	5	–	–	–	–	–	–	8	–	7	–	6
Logic "1" Threshold Voltage	V_{OHA} ②	2	-1.120	–	-1.020	–	–	-0.950	–	Vdc	–	–	11,12,13	–	–	–	9,10	–	8	–	–	–	1,16
		3	-1.120	–	-1.020	–	–	-0.950	–	Vdc	–	–	11,12,13	–	–	–	9,10	–	8	–	–	–	1,16
Logic "0" Threshold Voltage	V_{OLA} ③	2	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	–	11,12,13	–	–	–	9,10	8	–	–	–	1,16
		3	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	–	11,12,13	–	–	–	9,10	8	–	–	–	1,16
Short Circuit Current	I_{OS}	7	-65	-20	-65	–	-20	-65	-20	mAdc	5	4	–	–	–	7	–	–	8	–	–	–	6

① Test outputs of the device must be tested by sequencing through the truth table. All input, power supply and ground voltages must be mtaintained between tests. The clock input is the waveform shown.
② In addition to meeting the output levels specified, the device must divide by 5, 8, or 10 during this test. The clock input is the waveform shown.
③ In addition to meeting the output levels specified, the device must divide by 6, 9, or 11 during this test. The clock input is the waveform shown.



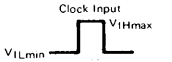
ELECTRICAL CHARACTERISTICS ..... Supply Voltage +5.0 V

These devices are designed to meet the dc specifications shown in the test table after thermal equilibrium has been established. Outputs are terminated through a 50-ohm resistor to +3.0 Vdc.

@ Test Temperature	TEST VOLTAGE/CURRENT VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{IH}	V_{IL}	V_{IHT}	V_{ILT}	V_{CC}	(mA) I_L	I_{OL}	I_{OH}
-55°C	+4.120	+3.040	+3.745	+3.500	+2.4	+0.5	+2.0	+0.8	+5.0	-0.25	16	-0.40
+25°C	+4.220	+3.110	+3.895	+3.525	+2.4	+0.5	+2.0	+0.8	+5.0	-0.25	16	-0.40
+125°C	+4.370	+3.140	+4.000	+3.560	+2.4	+0.5	+2.0	+0.8	+5.0	-0.25	16	-0.40

Characteristic	Symbol	Pin Under Test	MC12509, MC12511, MC12513 -55°C Min	-55°C Max	+25°C Min	+25°C Typ	+25°C Max	+125°C Min	+125°C Max	Unit	TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{IH}	V_{IL}	V_{IHT}	V_{ILT}	V_{CC}	I_L	I_{OL}	I_{OH}	(V_{EE}) Gnd
Power Supply Drain Current	I_{CC1}	8	-88	–	-80	–	–	-80	–	mAdc	–	–	–	–	–	–	–	–	1,16	–	–	–	8
	I_{CC2}	6	–	5.2	–	–	5.2	–	5.2	mAdc	4	5	–	–	–	–	–	–	6	–	–	–	8
Input Current	I_{INH1}	15	–	400	–	–	250	–	250	µAdc	15	–	–	–	–	–	–	–	1,16	–	–	–	8
		11	–	↓	–	–	↓	–	↓	↓	11	–	–	–	–	9,10	–	–	↓	–	–	–	↓
		12	–		–	–		–			12	–	–	–	–	9,10	–	–		–	–	–	
		13	–		–	–		–			13	–	–	–	–	9,10	–	–		–	–	–	
	I_{INH2}	4	1.7	6.0	2.0	–	6.0	2.0	6.4	mAdc	5	4	–	–	–	–	–	–	6	–	–	–	8
		5	1.7	6.0	2.0	–	6.0	2.0	6.4	mAdc	5	4	–	–	–	–	–	–	6	–	–	–	8
	I_{INH3}	5	0.7	3.0	1.0	–	3.0	1.0	3.6	mAdc	4	5	–	–	–	–	–	–	6	–	–	–	8
	I_{INH4}	9	–	100	–	–	100	–	100	µAdc	–	–	–	–	9	–	–	–	1,16	–	–	–	8
		10	–	100	–	–	100	–	100	µAdc	–	–	–	–	10	–	–	–	1,16	–	–	–	8
Leakage Current	I_{INL1}	15	-10	–	-10	–	–	-10	–	µAdc	–	–	–	–	–	–	–	–	1,16	–	–	–	8,15
		11	↓	–	↓	–	–	↓	–	↓	–	–	–	–	–	–	–	–	↓	–	–	–	8,11
		12		–		–	–		–		–	–	–	–	–	–	–	–		–	–	–	8,12
		13		–		–	–		–		–	–	–	–	–	–	–	–		–	–	–	8,13
	I_{INL2}	9	-1.6	–	-1.6	–	–	-1.6	–	mAdc	–	–	–	–	–	9	–	–	1,16	–	–	–	8
		10	-1.6	–	-1.6	–	–	-1.6	–	mAdc	–	–	–	–	–	10	–	–	1,16	–	–	–	8
Reference Voltage	V_{BB}	14	–	–	3.67	–	3.87	–	–	Vdc	–	–	–	–	–	–	–	–	1,16	14	–	–	8
Logic "1" Output Voltage	V_{OH1} ①	2	3.880	4.120	4.030	–	4.220	4.135	4.370	Vdc	–	11,12,13	–	–	–	9,10	–	–	1,16	–	–	–	8
		3	3.880	4.120	4.030	–	4.220	4.135	4.370	Vdc	–	11,12,13	–	–	–	9,10	–	–	1,16	–	–	–	8
	V_{OH2}	7	2.4	–	2.7	–	–	3.0	–	Vdc	5	4	–	–	–	–	–	–	6	–	–	7	8
Logic "0" Output Voltage	V_{OL1} ①	2	3.040	3.405	3.110	–	3.440	3.140	3.515	Vdc	–	11,12,13	–	–	–	9,10	–	–	1,16	–	–	–	8
		3	3.040	3.405	3.110	–	3.440	3.140	3.515	Vdc	–	11,12,13	–	–	–	9,10	–	–	1,16	–	–	–	8
	V_{OL2}	7	–	1.00	–	–	0.80	–	0.66	Vdc	4	5	–	–	–	–	–	–	6	–	7	–	8
Logic "1" Threshold Voltage	V_{OHA} ②	2	3.860	–	4.010	–	–	4.115	–	Vdc	–	–	11,12,13	–	–	–	9,10	–	1,16	–	–	–	8
		3	3.860	–	4.010	–	–	4.115	–	Vdc	–	–	11,12,13	–	–	–	9,10	–	1,16	–	–	–	8
Logic "0" Threshold Voltage	V_{OLA} ③	2	–	3.425	–	–	3.460	–	3.535	Vdc	–	–	–	11,12,13	–	–	–	9,10	1,16	–	–	–	8
		3	–	3.425	–	–	3.460	–	3.535	Vdc	–	–	–	11,12,13	–	–	–	9,10	1,16	–	–	–	8
Short Circuit Current	I_{OS}	7	-65	-20	-65	–	-20	-65	-20	mAdc	5	4	–	–	–	7	–	–	6	–	–	–	8

① Test outputs of the device must be tested by sequencing through the truth table. All input, power supply and ground voltages must be mtaintained between tests. The clock input is the waveform shown.
② In addition to meeting the output levels specified, the device must divide by 5, 8, or 10 during this test. The clock input is the waveform shown.
③ In addition to meeting the output levels specified, the device must divide by 6, 9, or 11 during this test. The clock input is the waveform shown.



ELECTRICAL CHARACTERISTICS ..... Supply Voltage −5.2 V

These devices are designed to meet the dc specifications shown in the test table after thermal equilibrium has been established. Outputs are terminated through a 50-ohm resistor to −2.0 Vdc.

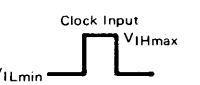
@Test Temperature	TEST VOLTAGE/CURRENT VALUES: Volts V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{IH}	V_{IL}	V_{IHT}	V_{ILT}	V_{EE}	mA I_L	I_{OL}	I_{OH}
-55°C	-0.880	-2.020	-1.255	-1.500	-2.8	-4.7	-3.2	-4.4	-5.2	-0.25	16	-0.40
+25°C	-0.780	-1.950	-1.105	-1.475	-2.8	-4.7	-3.2	-4.4	-5.2	-0.25	16	-0.40
+125°C	-0.630	-1.920	-1.000	-1.400	-2.8	-4.7	-3.2	-4.4	-5.2	-0.25	16	-0.40

Characteristic	Symbol	Pin Under Test	MC12509, MC12511, MC12513 -55°C Min	-55°C Max	+25°C Min	+25°C Typ	+25°C Max	+125°C Min	+125°C Max	Unit	TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{IH}	V_{IL}	V_{IHT}	V_{ILT}	V_{EE}	I_L	I_{OL}	I_{OH}	Gnd
Power Supply Drain Current	I_{CC1}	8	-88	–	-80	–	–	-80	–	mAdc	–	–	–	–	–	–	–	–	8	–	–	–	1,16
	I_{CC2}	6	–	5.2	–	–	5.2	–	5.2	mAdc	4	5	–	–	–	–	–	–	8	–	–	–	6
Input Current	I_{INH1}	15	–	400	–	–	250	–	250	μAdc	15	–	–	–	–	–	–	–	8	–	–	–	1,16
		11	–	↓	–	–	↓	–	↓	↓	11	–	–	–	–	9,10	–	–	↓	–	–	–	↓
		12	–		–	–		–			12	–	–	–	–	9,10	–	–		–	–	–	
		13	–		–	–		–			13	–	–	–	–	9,10	–	–		–	–	–	
	I_{INH2}	4	1.7	6.0	2.0	–	6.0	2.0	6.4	mAdc	5	4	–	–	–	–	–	–	8	–	–	–	6
		5	1.7	6.0	2.0		6.0	2.0	6.4	mAdc	5	4	–	–	–	–	–	–	8	–	–	–	6
	I_{INH3}	5	0.7	3.0	1.0	–	3.0	1.0	3.6	mAdc	4	5	–	–	–	–	–	–	8	–	–	–	6
	I_{INH4}	9	–	100	–	–	100	–	100	μAdc	–	–	–	–	9	–	–	–	8	–	–	–	1,16
		10	–	100	–	–	100	–	100	μAdc	–	–	–	–	10	–	–	–	8	–	–	–	1,16
Leakage Current	I_{INL1}	15	-10	–	-10	–	–	-10	–	μAdc	–	–	–	–	–	–	–	–	8,15	–	–	–	1,16
		11	↓	–	↓	–	–	↓	–	↓	–	–	–	–	–	–	–	–	8,11	–	–	–	↓
		12		–		–	–		–		–	–	–	–	–	–	–	–	8,12	–	–	–	
		13		–		–	–		–		–	–	–	–	–	–	–	–	8,13	–	–	–	
	I_{INL2}	9	-1.6	–	-1.6	–	–	-1.6	–	mAdc	–	–	–	–	–	9	–	–	8	–	–	–	1,16
		10	-1.6	–	-1.6	–	–	-1.6	–	mAdc		–	–	–	–	10	–	–	8	–	–	–	1,16
Reference Voltage	V_{BB}	14	–	–	-1.360	–	-1.160	–	–	Vdc	–	–	–	–	–	–	–	–	8	14	–	–	1,16
Logic "1" Output Voltage	V_{OH1} ①	2	-1.120	-0.880	-0.970	–	-0.780	-0.865	-0.630	Vdc	–	11,12,13	–	–	–	9,10	–	–	8	–	–	–	1,16
		3	-1.120	-0.880	-0.970	–	-0.780	-0.865	-0.630	Vdc	–	11,12,13	–	–	–	9,10	–	–	8	–	–	–	1,16
	V_{OH2}	7	-2.8	–	-2.5	–	–	-2.2	–	Vdc	5	4	–	–	–	–	–	–	8	–	–	7	6
Logic "0" Output Voltage	V_{OL1} ①	2	-2.020	-1.655	-1.950	–	-1.620	-1.920	-1.545	Vdc	–	11,12,13	–	–	–	9,10	–	–	8	–	–	–	1,16
		3	-2.020	-1.655	-1.950	–	-1.620	-1.920	-1.545	Vdc	–	11,12,13	–	–	–	9,10	–	–	8	–	–	–	1,16
	V_{OL2}	7	–	-4.20	–	–	-4.40	–	-4.54	Vdc	4	5	–	–	–	–	–	–	8	–	7	–	6
Logic "1" Threshold Voltage	V_{OHA} ②	2	-1.140	–	-0.990	–	–	-0.885	–	Vdc	–	–	11,12,13	–	–	–	9,10	–	8	–	–	–	1,16
		3	-1.140	–	-0.990	–	–	-0.885	–	Vdc	–	–	11,12,13	–	–	–	9,10	–	8	–	–	–	1,16
Logic "0" Threshold Voltage	V_{OLA} ③	2	–	-1.635	–	–	-1.600	–	-1.525	Vdc	–	–	–	11,12,13	–	–	–	9,10	8	–	–	–	1,16
		3	–	-1.635	–	–	-1.600	–	-1.525	Vdc	–	–	–	11,12,13	–	–	–	9,10	8	–	–	–	1,16
Short Circuit Current	I_{OS}	7	-65	-20	-65	–	-20	-65	-20	mAdc	5	4	–	–	–	7	–	–	8	–	–	–	6

① Test outputs of the device must be tested by sequencing through the truth table. All input, power supply and ground voltages must be mtaintained between tests. The clock input is the waveform shown.

② In addition to meeting the output levels specified, the device must divide by 5, 8, or 10 during this test. The clock input is the waveform shown.

③ In addition to meeting the output levels specified, the device must divide by 6, 9, or 11 during this test. The clock input is the waveform shown.



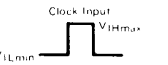
ELECTRICAL CHARACTERISTICS ..... Supply Voltage +5.0 V

These devices are designed to meet the dc specifications shown in the test table after thermal equilibrium has been established. Outputs are terminated through a 50-ohm resistor to +3.0 Vdc.

@ Test Temperature	TEST VOLTAGE/CURRENT VALUES											
	Volts									mA		
	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{IH}	V_{IL}	V_{IHT}	V_{ILT}	V_{CC}	I_L	I_{OL}	I_{OH}
-30°C	+4.110	+3.070	+3.795	+3.500	+2.4	+0.5	+2.0	+0.8	+5.0	-0.25	16	-0.40
+25°C	+4.190	+3.110	+3.895	+3.525	+2.4	+0.5	+2.0	+0.8	+5.0	-0.25	16	-0.40
+85°C	+4.300	+3.135	+3.965	+3.560	+2.4	+0.5	+2.0	+0.8	+5.0	-0.25	16	-0.40

Characteristic	Symbol	Pin Under Test	MC12009, MC12011, MC12013 -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{IH}	V_{IL}	V_{IHT}	V_{ILT}	V_{CC}	I_L	I_{OL}	I_{OH}	(V_{EE}) Gnd
Power Supply Drain Current	I_{CC1}	8	-88	–	-80	–	–	-80	–	mAdc	–	–	–	–	–	–	–	–	1,16	–	–	–	8
	I_{CC2}	6	–	5.2	–	–	5.2	–	5.2	mAdc	4	5	–	–	–	–	–	–	6	–	–	–	8
Input Current	I_{INH1}	15	–	375	–	–	250	–	250	μAdc	15	–	–	–	–	–	–	–	1,16	–	–	–	8
		11	–	↓	–	–	↓	–	↓	↓	11	–	–	–	–	9,10	–	–	↓	–	–	–	↓
		12	–		–	–		–			12	–	–	–	–	9,10	–	–		–	–	–	
		13	–		–	–		–			13	–	–	–	–	9,10	–	–		–	–	–	
	I_{INH2}	4	1.7	6.0	2.0	–	6.0	2.0	6.4	mAdc	5	4	–	–	–	–	–	–	6	–	–	–	8
		5	1.7	6.0	2.0	–	6.0	2.0	6.4	mAdc	5	4	–	–	–	–	–	–	6	–	–	–	8
	I_{INH3}	5	0.7	3.0	1.0	–	3.0	1.0	3.6	mAdc	4	5	–	–	–	–	–	–	6	–	–	–	8
	I_{INH4}	9	–	100	–	–	100	–	100	μAdc	–	–	–	–	9	–	–	–	1,16	–	–	–	8
		10	–	100	–	–	100	–	100	μAdc	–	–	–	–	10	–	–	–	1,16	–	–	–	8
Leakage Current	I_{INL1}	15	-10	–	-10	–	–	-10	–	μAdc	–	–	–	–	–	–	–	–	1,16	–	–	–	8,15
		11	↓	–	↓	–	–	↓	–	↓	–	–	–	–	–	–	–	–	↓	–	–	–	8,11
		12	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	8,12
		13	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	8,13
	I_{INL2}	9	-1.6	–	-1.6	–	–	-1.6	–	mAdc	–	–	–	–	–	9	–	–	1,16	–	–	–	8
		10	-1.6	–	-1.6	–	–	-1.6	–	mAdc	–	–	–	–	–	10	–	–	1,16	–	–	–	8
Reference Voltage	V_{BB}	14	–	–	3.67	–	3.87	–	–	Vdc	–	–	–	–	–	–	–	–	1,16	14	–	–	8
Logic "1" Output Voltage	V_{OH1} ①	2	3.900	4.110	4.000	–	4.190	4.070	4.300	Vdc	–	11,12,13	–	–	–	9,10	–	–	1,16	–	–	–	8
		3	3.900	4.110	4.000	–	4.190	4.070	4.300	Vdc	–	11,12,13	–	–	–	9,10	–	–	1,16	–	–	–	8
	V_{OH2}	7	2.4	–	2.6	–	–	2.8	–	Vdc	5	4	–	–	–	–	–	–	6	–	–	7	8
Logic "0" Output Voltage	V_{OL1} ①	2	3.070	3.385	3.110	–	3.410	3.135	3.445	Vdc	–	11,12,13	–	–	–	9,10	–	–	1,16	–	–	–	8
		3	3.070	3.385	3.110	–	3.410	3.135	3.445	Vdc	–	11,12,13	–	–	–	9,10	–	–	1,16	–	–	–	8
	V_{OL2}	7	–	0.94	–	–	0.80	–	0.72	Vdc	4	5	–	–	–	–	–	–	6	–	7	–	8
Logic "1" Threshold Voltage	V_{OHA} ②	2	3.880	–	3.980	–	–	4.050	–	Vdc	–	–	11,12,13	–	–	–	9,10	–	1,16	–	–	–	8
		3	3.880	–	3.980	–	–	4.050	–	Vdc	–	–	11,12,13	–	–	–	9,10	–	1,16	–	–	–	8
Logic "0" Threshold Voltage	V_{OLA} ③	2	–	3.405	–	–	3.430	–	3.465	Vdc	–	–	–	11,12,13	–	–	–	9,10	1,16	–	–	–	8
		3	–	3.405	–	–	3.430	–	3.465	Vdc	–	–	–	11,12,13	–	–	–	9,10	1,16	–	–	–	8
Short Circuit Current	I_{OS}	7	-65	-20	-65	–	-20	-65	-20	mAdc	5	4	–	–	–	7	–	–	6	–	–	–	8

① Test outputs of the device must be tested by sequencing through the truth table. All input, power supply and ground voltages must be mtaintained between tests. The clock input is the waveform shown.
② In addition to meeting the output levels specified, the device must divide by 5, 8, or 10 during this test. The clock input is the waveform shown.
③ In addition to meeting the output levels specified, the device must divide by 6, 9, or 11 during this test. The clock input is the waveform shown.



SWITCHING CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	MC12009, MC12011, MC12013										TEST VOLTAGES/WAVEFORMS APPLIED TO PINS LISTED BELOW:							
			−30°C			+25°C			+85°C											
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit	Pulse Gen. 1	Pulse Gen. 2	Pulse Gen. 3	V_{IHmin} †	V_{ILmin} †	V_F −3.0 V	V_{EE} −3.0 V	V_{CC} +2.0
Propagation Delay	t_{15+2+}	2	–	–	8.1	–	–	8.1	–	–	8.9	ns	15	–	–	–	11,12,13	9,10	8	1,6,16
(See Figures 3 and 5)	t_{15+2-}	2	–	–	7.5	–	–	7.5	–	–	8.2	↓	15	–	–	–	11,12,13	9,10	8	1,6,16
	t_{5+7+}	7	–	–	8.4	–	–	8.1	–	–	8.9		A	–	–	–	–	–	8	1,6,16
	t_{5-7-}	7	–	–	6.5	–	–	6.5	–	–	7.1		A	–	–	–	–	–	8	1,6,16
Setup Time	t_{setup1}	11	5.0	–	–	5.0	–	–	5.0	–	–	ns	15	*	–	–	*	9,10	8	1,6,16
(See Figures 4 and 5)	t_{setup2}	9	5.0	–	–	5.0	–	–	5.0	–	–	ns	15	–	*	–	11,12,13	*	8	1,6,16
Release Time	t_{rel1}	11	5.0	–	–	5.0	–	–	5.0	–	–	ns	15	*	–	–	*	9,10	8	1,6,16
(See Figures 4 and 5)	t_{rel2}	9	5.0	–	–	5.0	–	–	5.0	–	–	ns	15	–	*	–	11,12,13	*	8	1,6,16
Toggle Frequency (See Figure 6)	f_{max}	2										MHz								
MC12009 : 5/6			440	–	–	480	–	–	440	–	–		–	–	–	11	–	–	8	16
MC12011 : 8/9			500	–	–	550	–	–	500	–	–		–	–	–	11	–	–	8	16
MC12013 : 10/11			500	–	–	550	–	–	500	–	–		–	–	–	11	–	–	8	16

*Test inputs sequentially, with Pulse Generator 2 or 3 as indicated connected to input under test, and the voltage indicated applied to the other input(s) of the same type (i.e., MECL or MTTL).

	−30°C	+25°C	+85°C	
† V_{IHmin}	+1.03	+1.115	+1.20	Vdc
† V_{ILmin}	+0.175	+0.200	+0.235	Vdc

SWITCHING CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	MC12509, MC12511, MC12513										TEST VOLTAGES/WAVEFORMS APPLIED TO PINS LISTED BELOW:							
			−55°C			+25°C			+125°C											
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit	Pulse Gen. 1	Pulse Gen. 2	Pulse Gen. 3	V_{IHmin} †	V_{ILmin} †	V_F −3.0 V	V_{EE} −3.0 V	V_{CC} +2.0
Propagation Delay	t_{15+2+}	2	–	–	8.1	–	–	8.1	–	–	9.4	ns	15	–	–	–	11,12,13	9,10	8	1,6,16
(See Figures 3 and 5)	t_{15+2-}	2	–	–	7.5	–	–	7.5	–	–	8.7	↓	15	–	–	–	11,12,13	9,10	8	1,6,16
	t_{5+7+}	7	–	–	8.4	–	–	8.1	–	–	9.4		A	–	–	–	–	–	8	1,6,16
	t_{5-7-}	7	–	–	6.5	–	–	6.5	–	–	7.6		A	–	–	–	–	–	8	1,6,16
Setup Time	t_{setup1}	11	5.0	–	–	5.0	–	–	5.0	–	–	ns	15	*	–	–	*	9,10	8	1,6,16
(See Figures 4 and 5)	t_{setup2}	9	5.0	–	–	5.0	–	–	5.0	–	–	ns	15	–	*	–	11,12,13	*	8	1,6,16
Release Time	t_{rel1}	11	5.0	–	–	5.0	–	–	5.0	–	–	ns	15	*	–	–	*	9,10	8	1,6,16
(See Figures 4 and 5)	t_{rel2}	9	5.0	–	–	5.0	–	–	5.0	–	–	ns	15	–	*	–	11,12,13	*	8	1,6,16
Toggle Frequency (See Figure 6)	f_{max}	2										MHz								
MC12509÷5/6			420	–	–	480	–	–	420	–	–		–	–	–	11	–	–	8	16
MC12511÷8/9			500	–	–	550	–	–	500	–	–		–	–	–	11	–	–	8	16
MC12513÷10/11			500	–	–	550	–	–	500	–	–		–	–	–	11	–	–	8	16

*Test inputs sequentially, with Pulse Generator 2 or 3 as indicated connected to input under test, and the voltage indicated applied to the other input(s) of the same type (i.e., MECL or MTTL).

	−55°C	+25°C	+125°C	
† V_{IHmin}	+1.02	+1.15	+1.27	Vdc
† V_{ILmin}	+0.165	+0.215	+0.260	Vdc

FIGURE 3 — AC VOLTAGE WAVEFORMS

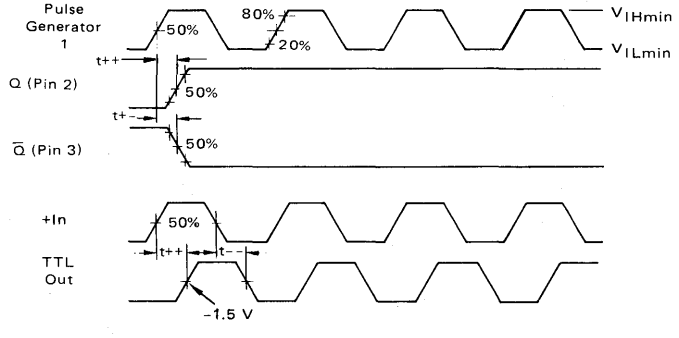


FIGURE 4 — SETUP AND RELEASE TIME WAVEFORMS

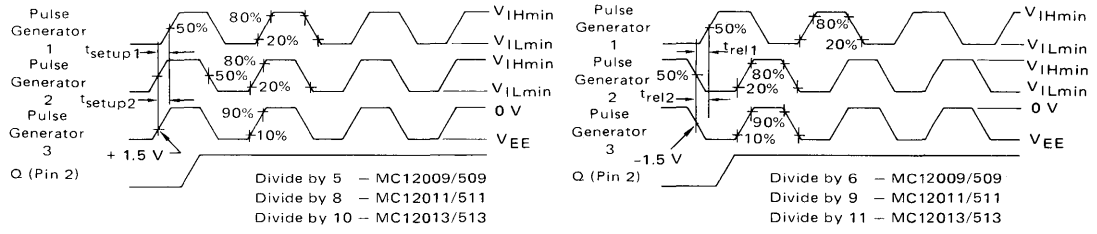
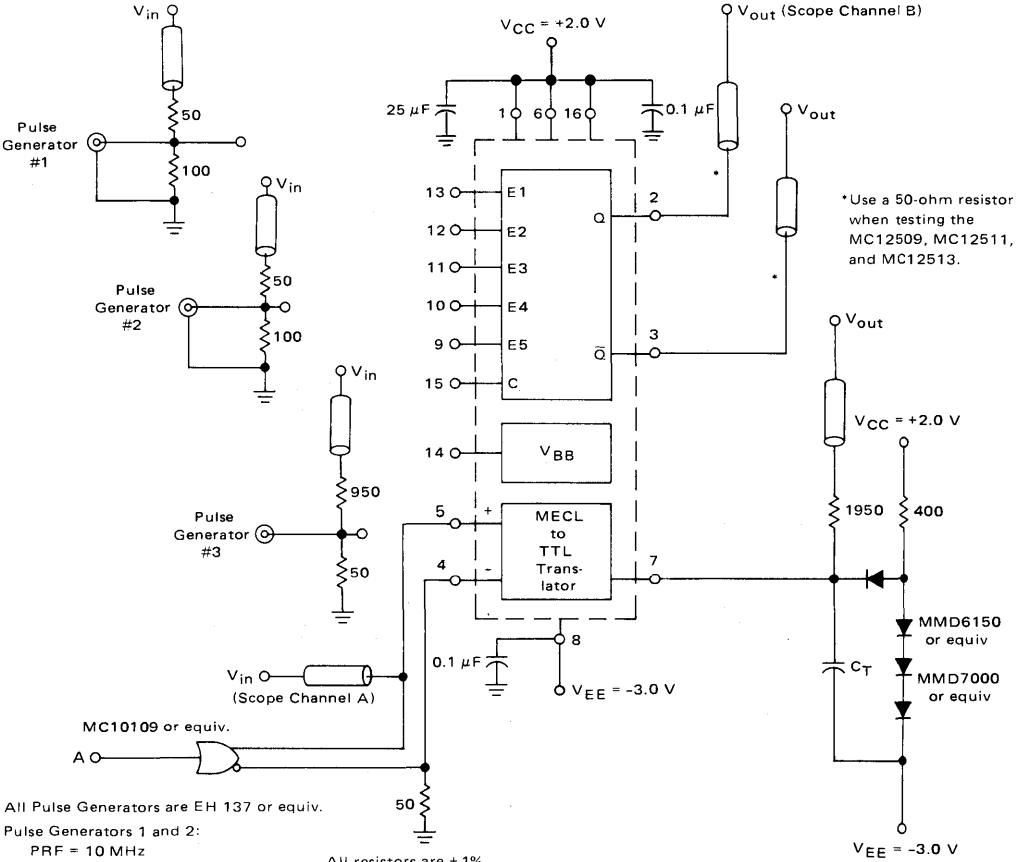


FIGURE 5 — AC TEST CIRCUIT



All Pulse Generators are EH 137 or equiv.

Pulse Generators 1 and 2:
PRF = 10 MHz
PW = 50% Duty Cycle
t+ = t– = 2.0 ± 0.2 ns

Pulse Generator 3:
PRF = 2.0 MHz
PW = 50% Duty Cycle
t+ = t– = 5.0 ± 0.5 ns

All resistors are + 1%.

All input and output cables to the scope are equal lengths of 50-ohm coaxial cable.

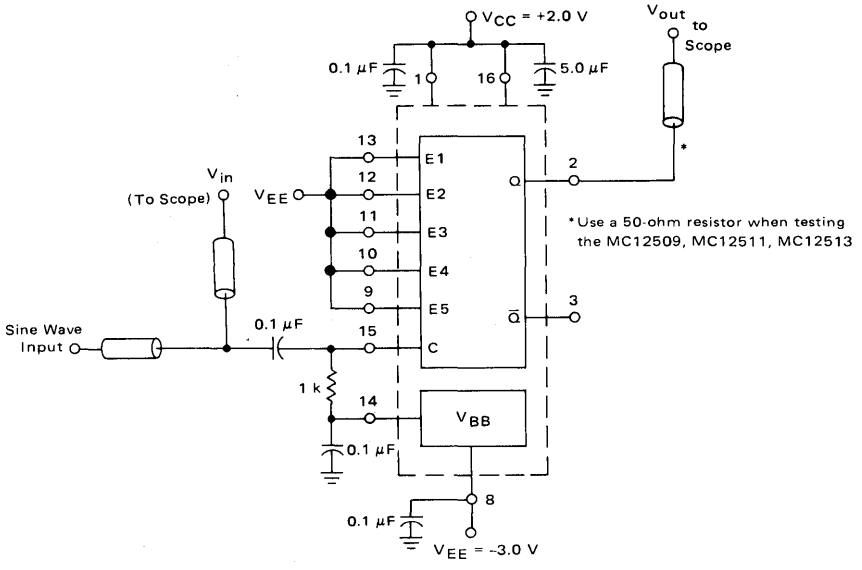
The 1950-ohm resistor at pin 7 and the scope termination impedance constitute a 40:1 attenuator probe.

C_T = 15 pF = total parasitic capacitance which includes probe, wiring, and load capacitance.

Unused output connected to a 50-ohm resistor to ground (MC12009, MC12011, MC12013), 100-ohm resistor to ground (MC12509, MC12511, MC12513).

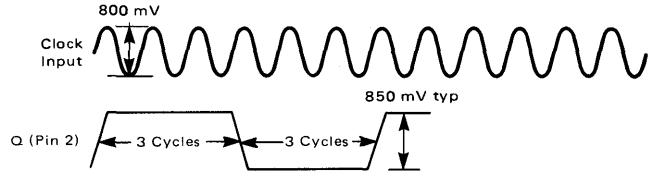
7

FIGURE 6 — MAXIMUM FREQUENCY TEST CIRCUIT

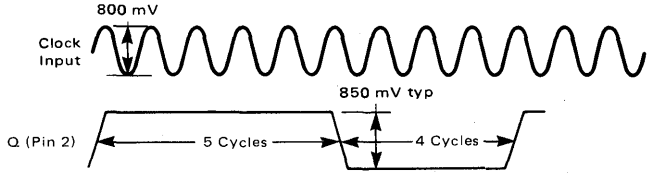


Unused output connected to a 50-ohm resistor to ground (MC12009, MC12011, MC12013), 100-ohm resistor to ground (MC12509, MC12511, MC12513)

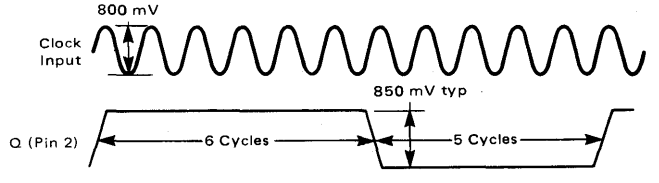
DIVIDE BY 6



DIVIDE BY 9



DIVIDE BY 11



7

FIGURE 7 — STATE DIAGRAM

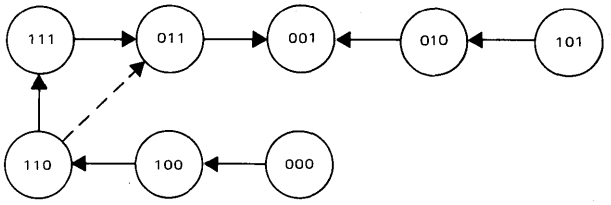
DIVIDE BY 5/6 (MC12009/MC12509)

Q1	Q2	Q3
1	1	1
0	1	1
0	0	1
0	0	0
1	0	0
1	1	0

Enable = 0

Enable = 1

— — — Enable = 1



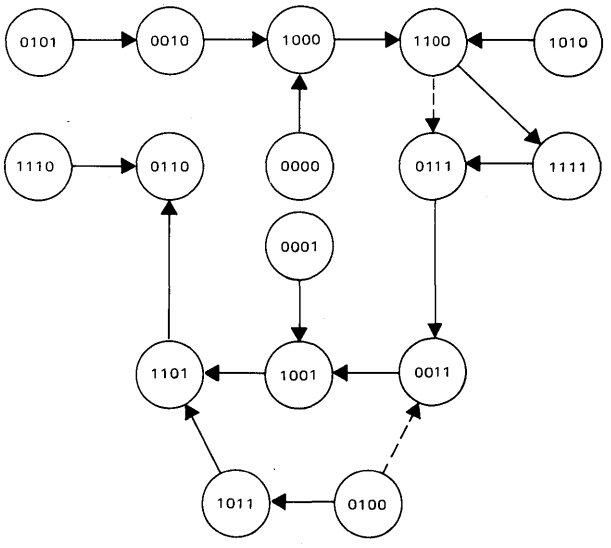
DIVIDE BY 8/9 (MC12011/MC12511)

Q1	Q2	Q3	Q4
1	1	1	1
0	1	1	1
0	0	1	1
1	0	0	1
1	1	0	1
0	1	1	0
0	0	1	0
1	0	0	0
1	1	0	0

Enable = 0

Enable = 1

— — — Enable = 1.



DIVIDE BY 10/11 (MC12013/MC12513)

Q1	Q2	Q3	Q4
1	1	1	1
0	1	1	1
0	0	1	1
0	0	0	1
1	0	0	1
1	1	0	1
0	1	1	0
0	0	1	0
0	0	0	0
1	0	0	0
1	1	0	0

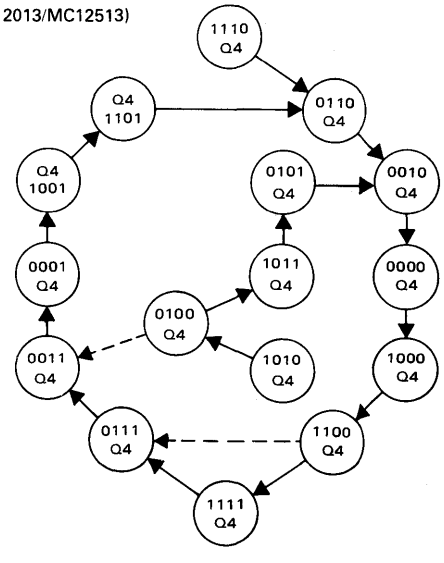
Enable = 0

Enable = 1

NOTES:

— — — Enable = 1.

The State of the Enable is important only for the positive Clock Transition when the counter is in state 1100.



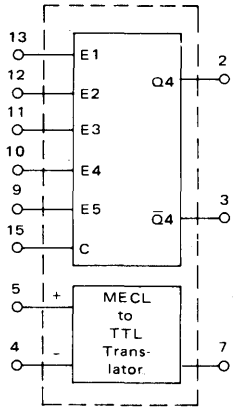
APPLICATIONS INFORMATION

The primary application of these devices is as a high-speed variable modulus prescaler in the divide by N section of a phase-locked loop synthesizer used as the local oscillator of two-way radios. The theory and advantages of variable modulus prescaling, along with typical applications, are covered in detail on the data sheet for the MC12012.

Proper VHF termination techniques should be followed when the clock is separated from the prescaler by any appreciable distance.

In their basic form, these devices will divide by 5/6, 8/9, or 10/11. Division by 5, 8, or 10 occurs when any one or all of the five gate inputs E1 through E5 are high. Division by 6, 9, or 11 occurs when all inputs E1 through E5 are low. (Unconnected TTL inputs are normally high, unconnected MECL inputs are normally low.) With the addition of extra parts, many different division configurations may be obtained (20/21, 40/41, 50/51, 100/101, etc.). A few of the many configurations are shown below, only for the MC12013/MC12513.

FIGURE 8 — DIVIDE BY 10/11 (MC12013/MC12513)

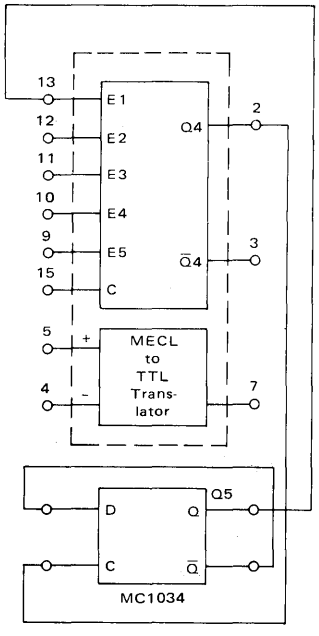


Q1	Q2	Q3	Q4
1	1	1	1
0	1	1	1
0	0	1	1
0	0	0	1
1	0	0	1
1	1	0	1
0	1	1	0
0	0	1	0
0	0	0	0
1	0	0	0
1	1	0	0

Enable = 0

Enable = 1

FIGURE 9 – DIVIDE BY 20/21 (MC12013/MC12513)



COUNT	Q1	Q2	Q3	Q4	Q5
31	1	1	1	1	1
30	0	1	1	1	1
28	0	0	1	1	1
24	0	0	0	1	1
25	1	0	0	1	1
27	1	1	0	1	1
22	0	1	1	0	1
20	0	0	1	0	1
16	0	0	0	0	1
17	1	0	0	0	1
19	1	1	0	0	1
14	0	1	1	1	0
12	0	0	1	1	0
8	0	0	0	1	0
9	1	0	0	1	0
11	1	1	0	1	0
6	0	1	1	0	0
4	0	0	1	0	0
0	0	0	0	0	0
1	1	0	0	0	0
3	1	1	0	0	0

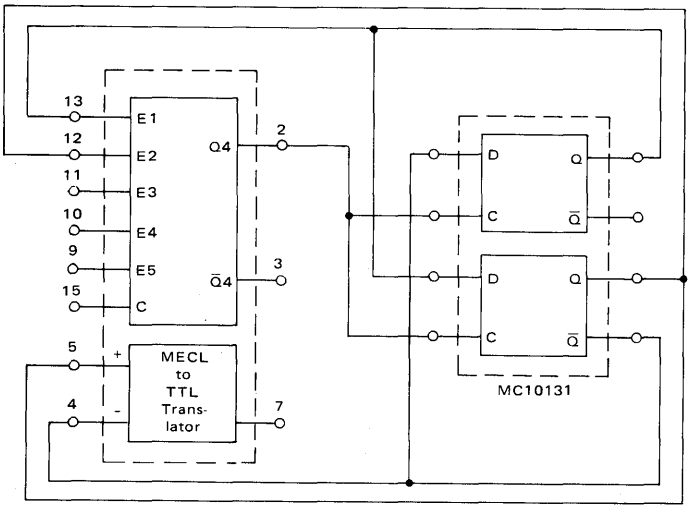
E2 + E3 + E4 + E5 = 1

E2 + E3 + E4 + E5 = 0

To obtain an TTL output, connect pins 5 and 4 to pins 2 and 3 respectively. Termination resistors for the MECL outputs are not shown, but are required except for the flip-flop driving the translator section.

The ÷ 20/21 counter may also be built using an TTL flip-flop by connecting pins 5 and 4 to pins 2 and 3 respectively, and driving the TTL flip-flop with pin 7. MC12013 inputs E4 and E5 are used rather than E1 With E1 + E2 + E3 = 0, operation remains as shown.

FIGURE 10 – DIVIDE BY 40/41 (MC12013/MC12513)



For ÷40: E4 + E5 = 1
For ÷41: E4 +E5 = 0

Termination resistors for MECL outputs are not shown, but are required except for the flip-flop driving the translator section.

7

MOTOROLA

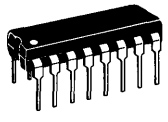
MC12014/ MC12514

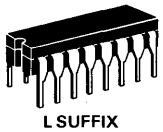
COUNTER CONTROL LOGIC

The MC12014 monolithic counter control logic unit is designed for use with the MC12013 Two-Modulus Prescaler and the MC4016 Programmable Counter to accomplish direct high-frequency programming. The MC12014 consists of a zero detector which controls the modulus of the MC12013, and an early decode function which controls the MC4016. The early decode feature also increases the useful frequency range of the MC4016 from 8.0 MHz to 25 MHz.

COUNTER CONTROL LOGIC

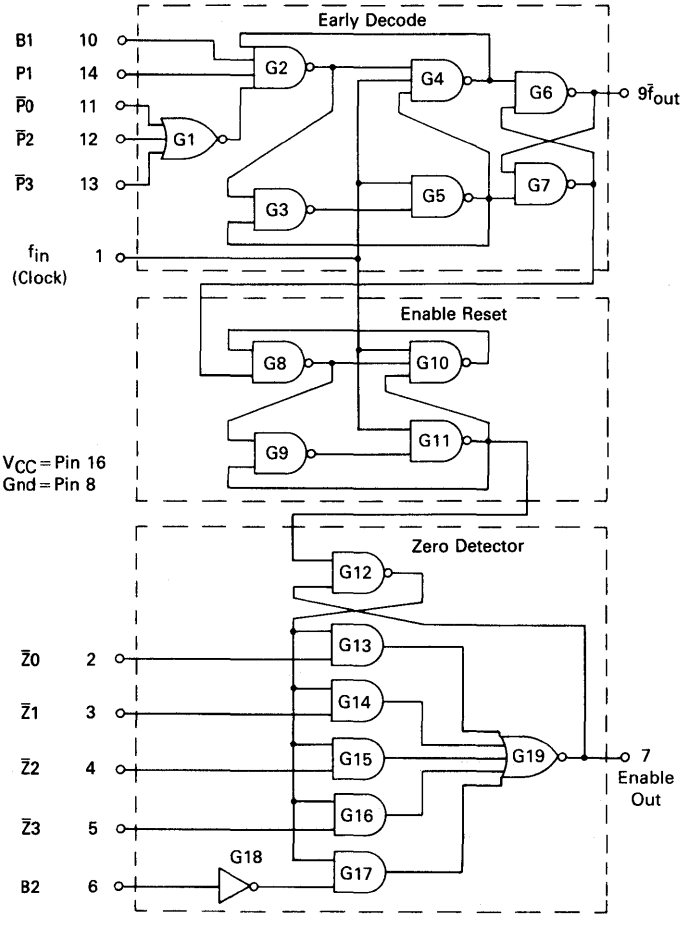
P SUFFIX
PLASTIC PACKAGE
CASE 648



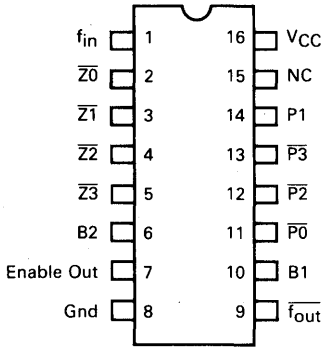


L SUFFIX
CERAMIC PACKAGE
CASE 620

LOGIC DIAGRAM



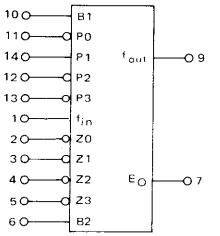
PIN ASSIGNMENT



7

ELECTRICAL CHARACTERISTICS

Test procedures are shown for the f_{in}, $\overline{Z0}$, B1 and P1 inputs. All other inputs are tested in the same manner as the $\overline{Z0}$ input.



Characteristic	Symbol	Pin Under Test	Test Limits 0 to +75°C Min	Max	Unit	TEST CURRENT/VOLTAGE VALUES (All Temperatures) mA I_{OL}	I_{OH}	I_{IC}	Volts V_{IL}	V_{IH}	V_{IHH}	V_{RH}	V_{CC}	V_{CCL}	V_{CCH}	Gnd
						16	-1.6	-10	0.5	2.4	5.5	4.5	5.0	4.75	5.25	
						TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW.										
Input																
Forward Current	I_{IL}	1	–	-6.4	mAdc	–	–	–	1	–	–	–	–	–	16	8,10
		2	–	-1.6	↓	–	–	–	2	–	–	–	–	–	↓	8
		10	–	↓	↓	–	–	–	10	–	–	–	–	–	↓	1,8,11,12,13
		14	–	↓	↓	–	–	–	14	–	–	–	–	–	↓	1,8,11,12,13
Leakage Current	I_{IH}	1	–	160	μAdc	–	–	–	–	1	–	–	–	–	16	8,10
		2	–	40	↓	–	–	–	–	2	–	–	–	–	↓	8
		10	–	↓	↓	–	–	–	–	10	–	–	–	–	↓	1,8,11,12,13
		14	–	↓	↓	–	–	–	–	14	–	–	–	–	↓	1,8,11,12,13
	I_{IHH}	1	–	1.0	mAdc	–	–	–	–	–	1	–	–	–	16	8
		2	–	↓	↓	–	–	–	–	–	2	–	–	–	↓	8
		10	–	↓	↓	–	–	–	–	–	10	–	–	–	↓	1,8,11,12,13
		14	–	↓	↓	–	–	–	–	–	14	–	–	–	↓	1,8,11,12,13
Clamp Voltage	V_{IC}	1	–	-1.2	Vdc	–	–	1	–	–	–	–	–	16	–	8
		2	–	↓	↓	–	–	2	–	–	–	–	–	↓	–	↓
		10	–	↓	↓	–	–	10	–	–	–	–	–	↓	–	↓
		14	–	↓	↓	–	–	14	–	–	–	–	–	↓	–	↓
Output																
Output Voltage	V_{OL}*	7	–	0.5	Vdc	7	–	–	11,12,13	–	–	2,3,4,5,10,11	–	16	–	8
		9	–	0.5	Vdc	9	–	–	11,12,13	–	–	10,14	–	16	–	8
	V_{OH}	7	2.4	–	Vdc	–	7	–	2,3,4,5	–	–	6	–	16	–	8
		9**	2.4	–	Vdc	–	9	–	–	–	–	11,12,13	–	16	–	8
Short-Circuit Current	I_{OS}	7	-20	-65	Vdc	–	–	–	2,3,4,5	–	–	6	16	–	–	7,8
		9**	-20	-65	Vdc	–	–	–	–	–	–	11,12,13	16	–	–	8,9
Power Requirements																
Power Supply Drain	I_{CC}	16	–	35	mAdc	–	–	–	–	–	–	–	16	–	–	1,8

*Output level to be measured after waveform 1 is applied to f_{in}, pin 1.
**Output level to be measured after waveform 2 is applied to f_{in}, pin 1.

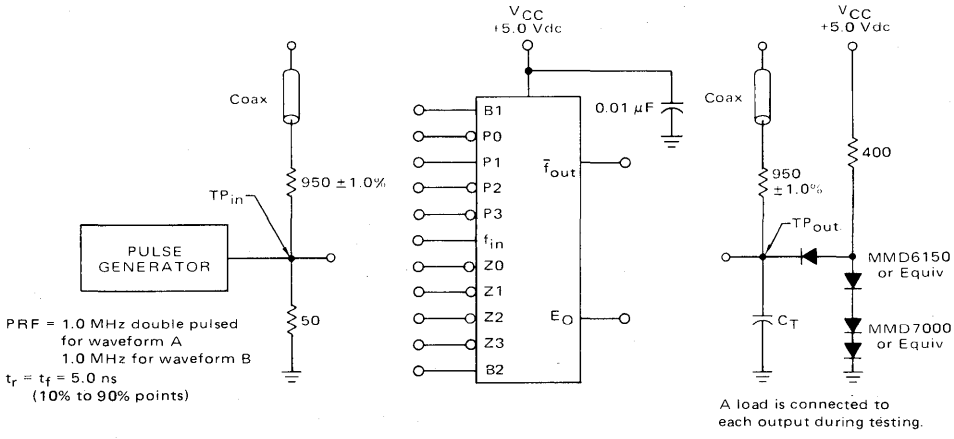
Waveform 1: 

Waveform 2: 

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 Vdc, waveform letters refer to waveforms on next page.)

Characteristic	Symbol	Pin Under Test		Test Limits (ns)							Pulse Gen. 1		Pulse Gen. 2		Pulse Out		Voltage Applied to Pins Listed Below	
				0°C		+25°C			+75°C									
		In	Out	Min	Max	Min	Typ	Max	Min	Max	Wave-form	Pin	Wave-form	Pin	Wave-form	Pin	V_{IL} = 0.5 V	V_{IH} = 2.4 V
Propagation Delay	t_{PLH1}	1	9	7.0	15	7.0	10	15	7.0	17	A	1	J	10	K	9	11,12,13	14
	t_{PHL1}	1	9	7.0	16	7.0	11	16	7.0	18	A	1	J	10	K	9	11,12,13	14
	t_{PLH2}	2	7	5.0	12	5.0	8.5	12	5.0	14	A	1	H	2	L	7	3,4,5,11,12,13	6,10,14
		3	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	3	↓	↓	2,4,5,11,12,13	↓
		4												4			2,3,5,11,12,13	
		5												5			2,3,4,11,12,13	
	t_{PHL2}	1	7	7.0	16	7.0	11	16	7.0	18	A	1	H	2	L	7	3,4,5,11,12,13	6,10,14
	t_{PLH3}	6	7	7.0	16	7.0	11	16	7.0	18	A	1	J	6	L	7	2,3,4,5,11,12,13	10,14
Setup Time	$t_{setup"1"}$	10	–	–	–	–	1.0	2.0	–	–	A	1	B	10	G	9	11,12,13	14
		11	–	–	–	–	7.0	12	–	–				11	F		12,13	10,14
		12	–	–	–	–	↓	↓	–	–				12	↓		11,13	↓
		13	–	–	–	–	↓	↓	–	–				13	↓		11,12	
		14	–	–	–	–	1.0	2.0	–	–	↓	↓	↓	14	G	↓	11,12,13	10
	$t_{setup"0"}$	10	–	–	–	–	4.5	8.0	–	–	A	1	C	10	F	9	11,12,13	14
		11	–	–	–	–	5.0	9.0	–	–				11	G		12,13	10,14
		12	–	–	–	–	↓	↓	–	–				12	↓		11,13	↓
		13	–	–	–	–	↓	↓	–	–				13	↓		11,12	
		14	–	–	–	–	4.5	8.0	–	–	↓	↓	↓	14	F	↓	11,12,13	10
Hold Time	$t_{hold"1"}$	10	–	–	–	–	4.0	8.0	–	–	A	1	D	10	G	9	11,12,13	14
		11	–	–	–	–	5.0	10	–	–				11	F		12,13	10,14
		12	–	–	–	–	↓	↓	–	–				12	↓		11,13	↓
		13	–	–	–	–	↓	↓	–	–				13	↓		11,12	
		14	–	–	–	–	4.0	8.0	–	–	↓	↓	↓	14	G	↓	11,12,13	10
	$t_{hold"0"}$	10	–	–	–	–	1.0	2.0	–	–	A	1	E	10	F	9	11,12,13	14
		11	–	–	–	–	7.5	14	–	–				11	G		12,13	10,14
		12	–	–	–	–	↓	↓	–	–				12	↓		11,13	↓
		13	–	–	–	–	↓	↓	–	–				13	↓		11,12	
		14	–	–	–	–	1.0	2.0	–	–	↓	↓	↓	14	F	↓	11,12,13	10

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

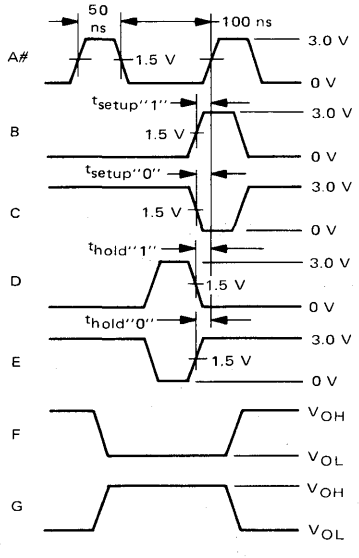


Two pulse generators are required and must be slaved together to provide the waveforms shown.

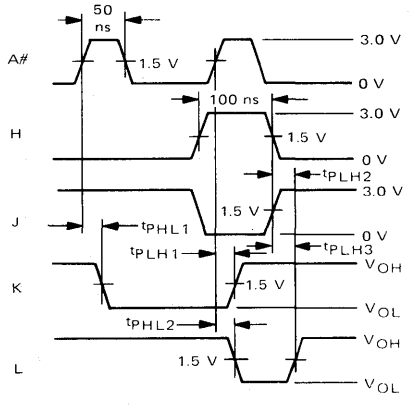
C_T = 15 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

SETUP AND HOLD TIMES



PROPAGATION DELAY TIMES



#Pulse A (f_{in}) used with all tests.

APPLICATIONS INFORMATION

The MC12014 Counter Control Logic incorporates two features for enhancing operation of the MC4016/4018 Programmable Counters.[1] Maximum operating frequency of the counters is limited by the time required for re-programming at the end of each count-down cycle. Operation can be extended to approximately 25 MHz by using the "early decode" feature included in the MC12014. The appropriate connections are shown in Figure 2. Only three counter stages are shown; however, up to eight stages can be satisfactorily cascaded. Note the following differences between this and the non-extended method: the counter gate inputs are not connected to the input clock; all parallel enables are connected to the $\overline{Q}$ output (f_{out}) of a type D flip-flop formed by gates G2 through G7 in the MC12014 package; the bus terminal of the least significant stage is grounded; all other bus terminals and one internal resistor, R, are connected together and serve as a data input, B1, to the flip-flop. Four additional data inputs, $\overline{P}0$ through $\overline{P}3$, serve to decode the "two" state of the least significant counter stage. Circuit operation is illustrated in waveforms of Figure 2, where the timing for the end of a count-down cycle is shown in expanded form. The counter parallel inputs are assumed to have N = 245 programmed. Timing is not shown for the third stage since it has already been counted down to the all zero state. As the next-to-least significant stage reaches zero, the common bus line goes high. Count down of the least significant stage continues until the "two" state is reached, causing the remaining data inputs to the flip-flop to go high. The next-to-last clock pulse of the cycle then triggers the flip-flop $\overline{Q}$ output low. This takes the parallel enables of all three counter stages low, resetting the programmed data to the outputs. The next input pulse clocks $\overline{Q}$ back to the high state since the data inputs to the flip-flop are no longer all high. The resulting negative output pulse at f_{out} is one input clock period in duration. Note that division by N equal to 001 or 002 is not available using this method.

The frequency synthesizer shown in Figure 8 requires that the programmable counters be quickly stopped after reaching their terminal (zero) count. This can be simply accomplished by taking the master reset of all stages low at the appropriate time. The bus output of the counters could be used for this function since a transition there signals the end of a count-down sequence. However, due to the relatively long delay between the last positive clock transition and the bus transition a faster method is required in this application.

The "zero detection" feature of the MC12014 provides a convenient means of implementing a faster method. Gates G12 through G19 form a latch whose output goes high if B2 is high and low logic levels are applied to the Z0 thru Z3 inputs. When once set to a one by appropriate input conditions, the output of G19 remains high until it is reset by the circuit comprised of gates G8 through G11. Note that since the required information is stored, the counter can be allowed to continue cycling.

The G8-G11 circuit monitors the G7 output of the "early decode" type D flip-flop. When the counter stage connected to the $\overline{P}0$ thru $\overline{P}3$ inputs has counted down to its two state the output of G7 goes high; this enables the G8-G11 circuitry and the next positive clock transition causes the output of G11 to go high, resetting the output of G19 to zero.

FIGURE 1 — TYPICAL FREQUENCY SYNTHESIZER APPLICATION

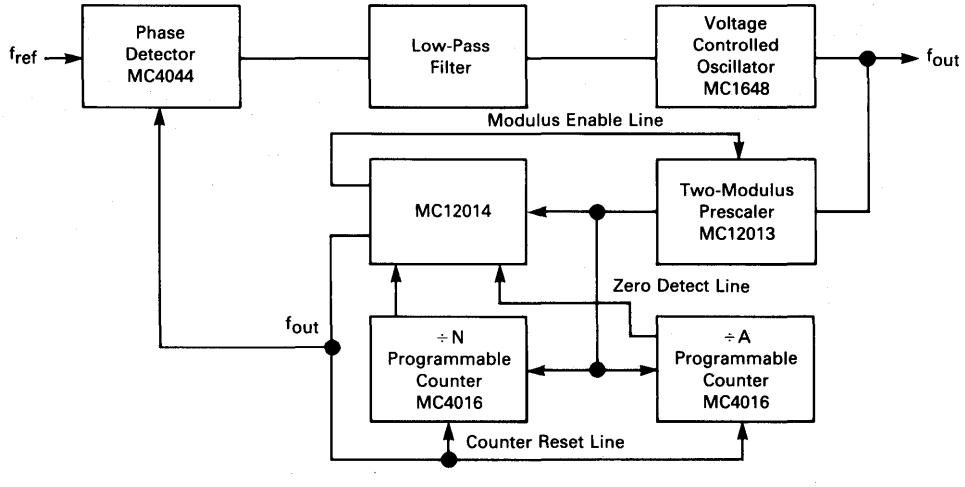
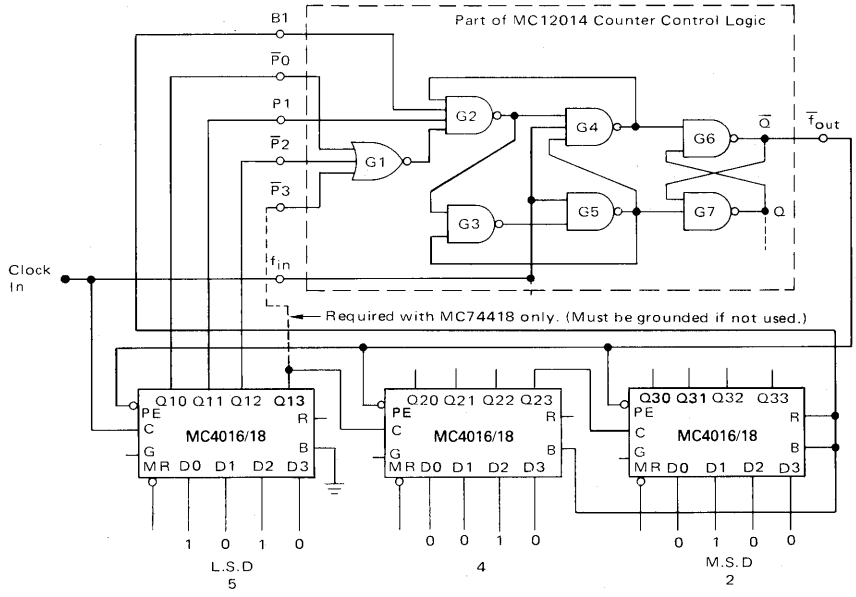
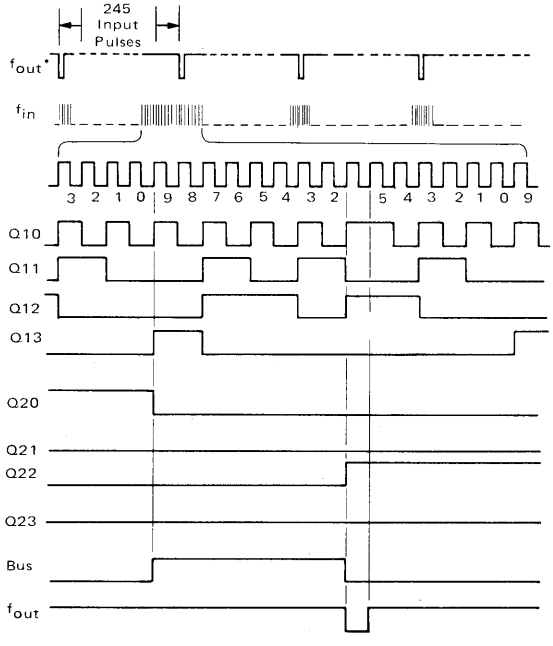


FIGURE 2 — INCREASING THE OPERATING RANGE OF MC74416/74418 PROGRAMMABLE COUNTERS USING MC12014





*Non-expanded version of bottom waveform.

1 See the MC54416/54418 data sheet for additional information.

Operation of the Counter Control Logic can be further clarified by considering a typical system application for programmable counters illustrated in the frequency synthesizer shown in Figure 3. There the counter provides a means of digitally selecting some integral multiple of a stable reference frequency. The circuit phase locks the output, f_{VCO}, of a voltage controlled oscillator to a reference frequency, f_{ref}.[2] Circuit operation is such that $f_{VCO} = Nf_{ref}$, where N is the divider ratio of the feedback counter, permitting frequency selection by means of thumbwheel switches.

In many synthesizer applications the VCO is operated at VHF frequencies too high for direct division by TTL counters. In these cases the VCO output is usually prescaled by using a suitable fixed divide-by-M ECL circuit as shown in Figure 4. For this configuration, $f_{VCO} = NMf_{ref}$, where N is variable (programmable) and M is fixed. Design of the optimum loop filter requires that the input reference frequency be as high as possible where the upper limit is established by the required channel spacing. Since $f_{VCO} = Nf_{ref}$ in the non-prescaled case, if N is changed by one, the VCO output changes by f_{ref}, or the synthesizer channel spacing is just equal to f_{ref}. When the prescaler is used as in Figure 4, $f_{VCO} = NMf_{ref}$, and a change of one in N results in the VCO changing by Mf_{ref}, i.e., if f_{ref} is set equal to the minimum permissible channel spacing as is desirable, then only every M channels in a given band can be selected. One solution is to set f_{ref} = channel spacing/M but this leads to more stringent loop filter requirements.

FIGURE 3 — TTL PHASE-LOCKED LOOP

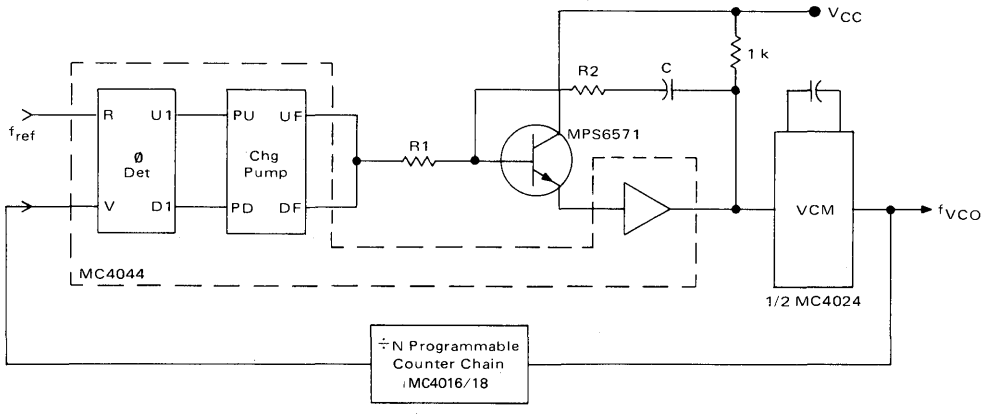
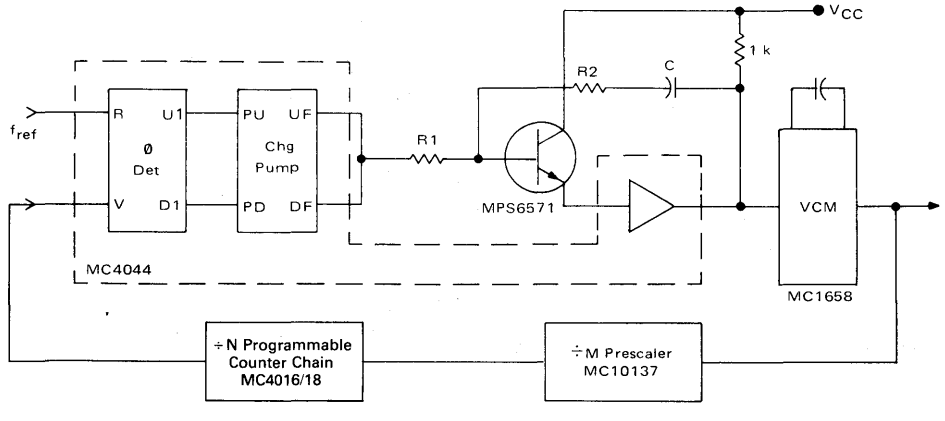


FIGURE 4 — TTL-MECL PHASE-LOCKED LOOP



2 See Motorola Application Notes AN-535, AN-532, and the MC4344/4044 Data Sheet for detailed explanation of over-all circuit operation.

An alternate approach that avoids this problem is provided by the counter configuration shown in Figure 5. It too uses a prescaler ahead of a programmable counter, however the modulus of the prescaler is now controlled by a third counter, causing it to alternate between M and M + 1. Operation is best explained by assuming that all three counters have been set for the beginning of a cycle: the prescaler for division by (M + 1), the modulus control counter for division by N_{mc}, and the programmable counter for division by N_{pc}. The prescaler will divide by (M + 1) until the modulus control counter has counted down to zero; at this time, the all zero state is detected and causes the prescaler to divide by M until the programmable counter has also counted down to zero. When this occurs, a cycle is complete and each counter is reset to its original modulus in readiness for the next cycle.

To determine the relationship between f_{out} and f_{in}, let T_1 be the time required for the modulus control counter to reach its terminal count and let T_2 be the remainder of one cycle. That is, T_2 is the time between terminal count in the modulus control counter and terminal count in the programmable counter. When the modulus control counter reaches zero, N_{mc} pulses will have entered it at a rate given by $f_{in}/(M + 1)$ pulses/second or T_2 is:

$$T_1 = \frac{(M + 1)}{f_{in}} \cdot N_{mc} \qquad (1)$$

At this time, N_{mc} pulses have also entered the programmable counter and it will reach its terminal counter after $(N_{pc} - N_{mc})$ more pulses have entered. The rate of entry is now f_{in}/M pulses/second since the prescaler is now dividing by M. From this T_2 is given by:

$$T_2 = \frac{M}{f_{in}} \cdot (N_{pc} - N_{mc}) \qquad (2)$$

Since $f = \frac{1}{T}$:

$$f_{out} = \frac{1}{T_{total}} = \frac{1}{T_1 + T_2} = \frac{1}{\frac{(M+1)N_{mc}}{f_{in}} + \frac{M(N_{pc} - N_{mc})}{f_{in}}} \qquad (3)$$

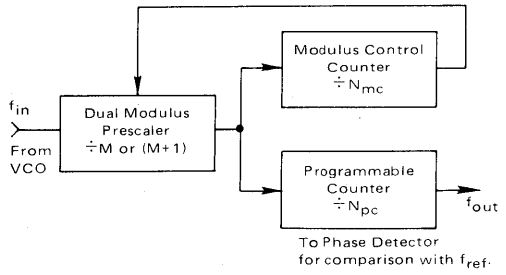
$$f_{out} = \frac{f_{in}}{(M+1)N_{mc} + M(N_{pc} - N_{mc})}$$

$$= \frac{f_{in}}{MN_{mc} + N_{mc} + MN_{pc} - MN_{mc}}$$

$$= \frac{f_{in}}{MN_{pc} + N_{mc}}$$

In terms of the synthesizer application, $f_{VCO} = (MN_{pc} + N_{mc})\, f_{ref}$ and channels can be selected every f_{ref} by letting N_{pc} and N_{mc} take on suitable integer values, including zero.

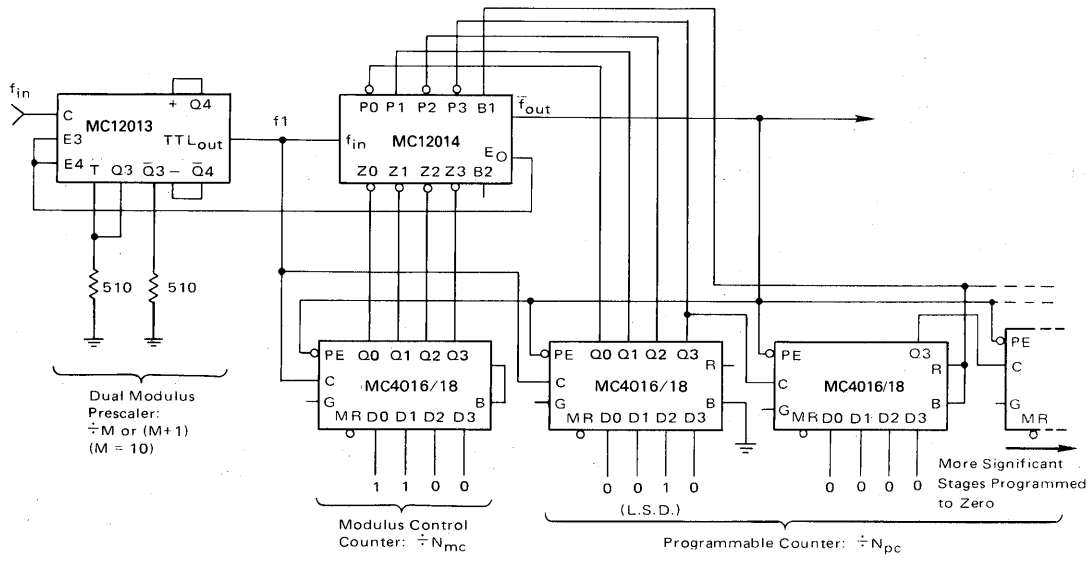
FIGURE 5 — FEEDBACK COUNTERS WITH DUAL MODULUS PRESCALER



A simplified example of this technique is shown in Figure 6. The MC12013 Dual Modulus Prescaler divides by either 10 or 11 when connected as shown in Figure 6. If the E3 and E4 Enable inputs are high at the start of a prescaler cycle, division by 10 results; if the Enable inputs are low at the beginning of the cycle, division by 11 results. The zero detection circuitry of the MC12014 Counter Control Logic is connected to monitor the outputs of the modulus control counter; this provides a suitable enable signal at E0 as the modulus control counter reaches its terminal (zero) count. The remainder of the MC12014 is connected to extend the operating frequency of the programmable counter chain. Appropriate waveforms for division by 43 are shown in Figure 7a.

The beginning of the timing diagram indicates circuit status just prior to the end of a countdown cycle, i.e., the modulus control counter has been counted down to one and the programmable counter is in the two state. The next positive transition from the prescaler (f1 in the timing diagram) then initiates the following sequence of events. Since the two state of the programmable counter enables the early decode circuitry in the MC12014, the positive f1 transition causes f_{out} to go low. Since f_{out} is connected to the Parallel Enables of all the MC4016 counters this low signal will re-program the counters in readiness for another cycle. However, due to the propagation time through the decode circuitry, the programmable and modulus control counters are briefly decremented to one and zero, respectively, before reprogramming occurs. The momentary zero state of the modulus control counter is detected, setting E_O of the MC12014 high, enabling the MC12013 for division by ten during its next cycle. After eleven more f_{in} pulses (E_O went high after the beginning of the prescaler cycle and so doesn't change the modulus until the next prescaler cycle), f1 again goes high, causing f_{out} to return to the one state. This releases the Parallel Enables and simultaneously resets E_O to zero. However, since E_O was high when the current prescaler cycle began, the next positive f1 transition occurs only ten f_{in} pulses later. Subsequent f1 transitions now decrement the MC4016 counters down through another cycle with the prescaler dividing by eleven. From the waveforms, 11 + 10 + 11 + 11 = 43 input pulses occur for each output pulse.

FIGURE 6 — FREQUENCY DIVISION: $f_O = f_{in}/(MN_{pc} + N_{mc})$



Division by 42 is shown in Figure 7b. Operation is similar except that the modulus control counter reaches its terminal count one f1 cycle earlier than before. Since E_O is reset by the trailing edge of the f_{out} pulse, E_O now remains high for two prescaler cycles leading to 10 + 10 + 11 + 11 = 42 input pulses for each output pulse.

Other combinations lead to similar results, however note that N_{pc} must be greater than or equal to N_{mc} for operation as described. If N_{mc} is greater than N_{pc} erroneous results are obtained, however this is not a serious restriction since N_{pc} is greater than N_{mc} in most practical applications.

The synthesizer shown in Figure 8 generates frequencies in the range from 144 to 178 MHz with 30 kHz channel spacing. It uses the dual modulus prescaler approach discussed earlier. General synthesizer design considerations are detailed in the publications listed in footnote 2, hence only the feedback counter is discussed here. Requirements for the feedback divider are determined from:

$$\text{Minimum Divider Ratio} = N_{Tmin} = \frac{144.00\ \text{MHz}}{30\ \text{kHz}} = 4800$$

$$\text{Maximum Divider Ratio} = N_{Tmax} = \frac{177.99\ \text{MHz}}{30\ \text{kHz}} = 5933$$

If the prescaler divides by at least ten, the maximum input frequency to the TTL counters will be 17.799 MHz, allowing use of MC4016 Programmable Counters with the MC12014 frequency extension feature.

7

FIGURE 7a — DIVISION BY 43

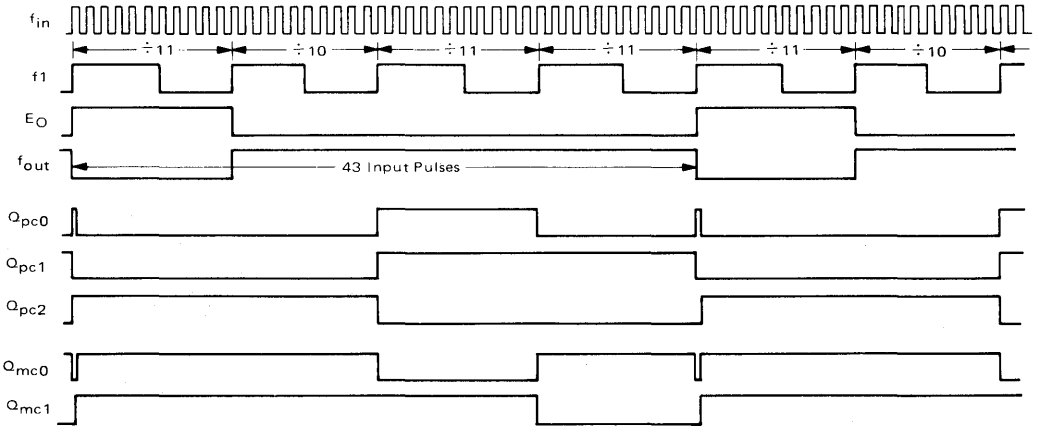
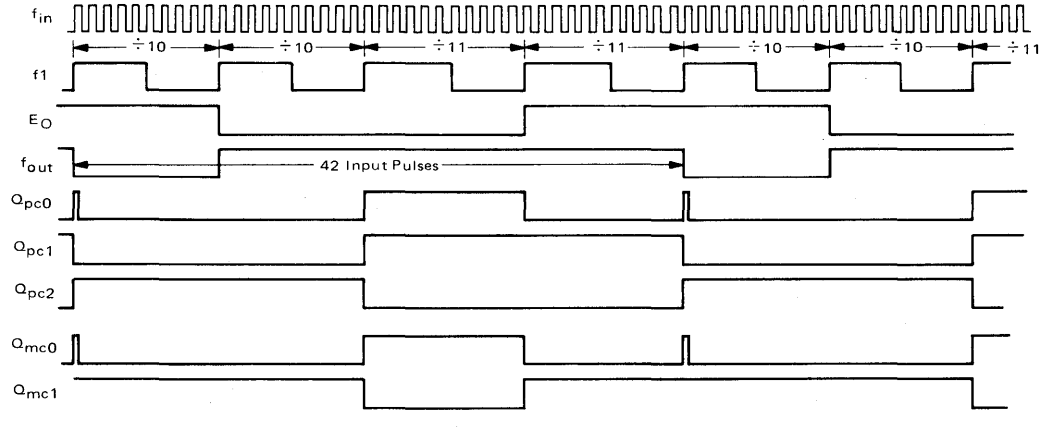


FIGURE 7b — DIVISION BY 42



7

FIGURE 8 — 144 TO 178 MHz FREQUENCY SYNTHESIZER WITH 30 kHz CHANNEL SPACING

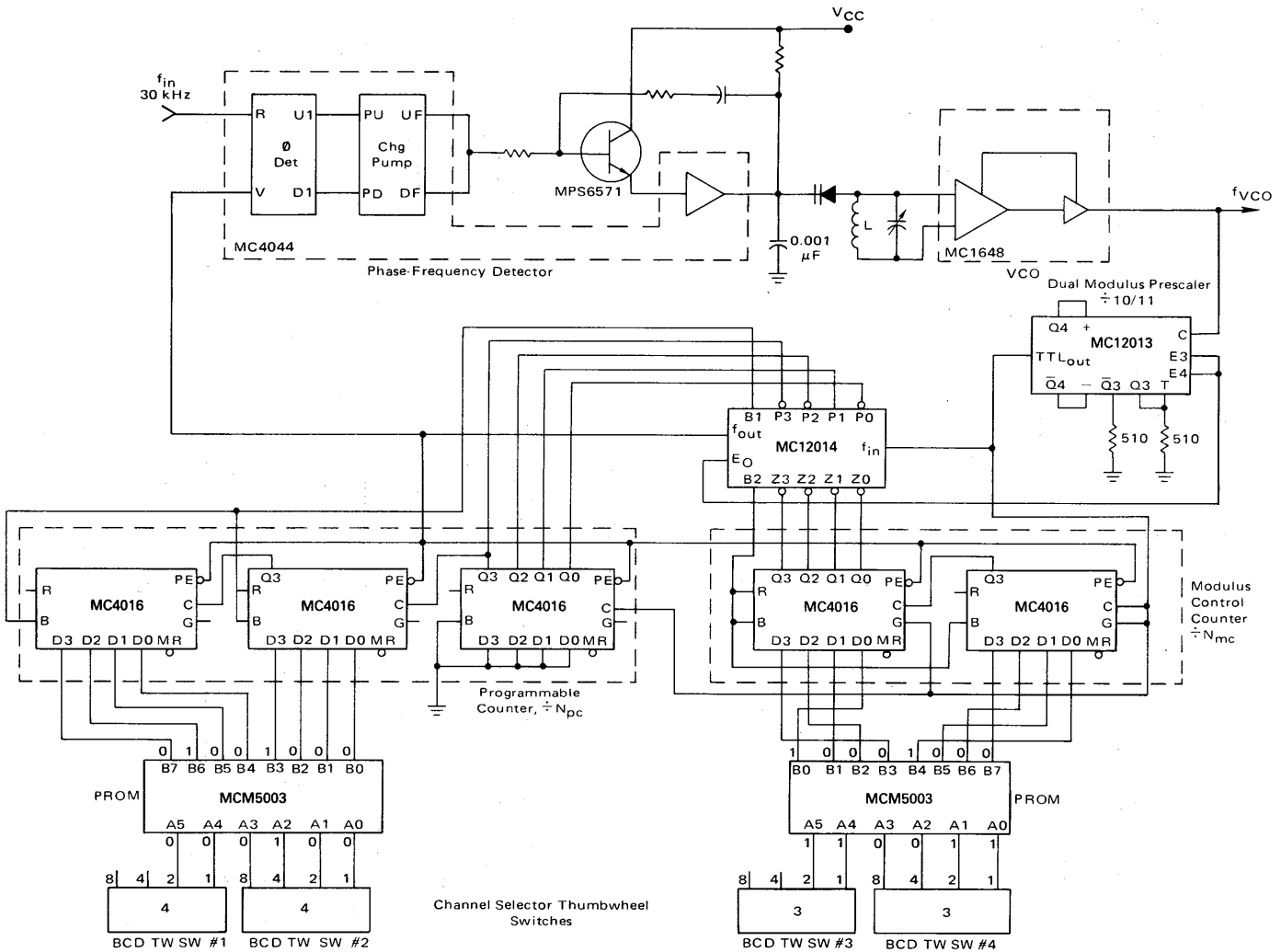


FIGURE 9 — N_{pc} PROM PROGRAMMING

	SW #1	SW #2	SW #1 A5 A4	SW #2 A3 A2 A1 A0	PROM WORD	PROM OUTPUT M.S.B.	PROM OUTPUT L.S.B.	N_{pc}	
(144 MHz)	44		0 1 0 0	0 1 0 0	4	0 1 0 0	1 0 0 0	48	480
	45		0 1 0 0	0 1 0 1	5	0 1 0 0	1 0 0 0	48	
	46		0 1 0 0	0 1 1 0	6	0 1 0 0	1 0 0 0	48	
	47		0 1 0 0	0 1 1 1	7	0 1 0 0	1 0 0 1	49	
	48		0 1 0 0	1 0 0 0	8	0 1 0 0	1 0 0 1	49	
	49		0 1 0 0	1 0 0 1	9	0 1 0 0	1 0 0 1	49	
	50		0 1 0 1	0 0 0 0	16	0 1 0 1	0 0 0 0	50	
	51		0 1 0 1	0 0 0 1	17	0 1 0 1	0 0 0 0	50	
	52		0 1 0 1	0 0 1 0	18	0 1 0 1	0 0 0 0	50	
	53		0 1 0 1	0 0 1 1	19	0 1 0 1	0 0 0 1	51	
	54		0 1 0 1	0 1 0 0	20	0 1 0 1	0 0 0 1	51	
	55		0 1 0 1	0 1 0 1	21	0 1 0 1	0 0 0 1	51	
	56		0 1 0 1	0 1 1 0	22	0 1 0 1	0 0 1 0	52	
	57		0 1 0 1	0 1 1 1	23	0 1 0 1	0 0 1 0	52	
	58		0 1 0 1	1 0 0 0	24	0 1 0 1	0 0 1 0	52	
	59		0 1 0 1	1 0 0 1	25	0 1 0 1	0 0 1 1	53	
	60		0 1 1 0	0 0 0 0	32	0 1 0 1	0 0 1 1	53	
	61		0 1 1 0	0 0 0 1	33	0 1 0 1	0 0 1 1	53	
	62		0 1 1 0	0 0 1 0	34	0 1 0 1	0 1 0 0	54	
	63		0 1 1 0	0 0 1 1	35	0 1 0 1	0 1 0 0	54	
	64		0 1 1 0	0 1 0 0	36	0 1 0 1	0 1 0 0	54	
	65		0 1 1 0	0 1 0 1	37	0 1 0 1	0 1 0 1	55	
	66		0 1 1 0	0 1 1 0	38	0 1 0 1	0 1 0 1	55	
	67		0 1 1 0	0 1 1 1	39	0 1 0 1	0 1 0 1	55	
	68		0 1 1 0	1 0 0 0	40	0 1 0 1	0 1 1 0	56	
	69		0 1 1 0	1 0 0 1	41	0 1 0 1	0 1 1 0	56	
	70		0 1 1 1	0 0 0 0	48	0 1 0 1	0 1 1 0	56	
	71		0 1 1 1	0 0 0 1	49	0 1 0 1	0 1 1 1	57	
	72		0 1 1 1	0 0 1 0	50	0 1 0 1	0 1 1 1	57	
	73		0 1 1 1	0 0 1 1	51	0 1 0 1	0 1 1 1	57	
	74		0 1 1 1	0 1 0 0	52	0 1 0 1	1 0 0 0	58	
	75		0 1 1 1	0 1 0 1	53	0 1 0 1	1 0 0 0	58	
	76		0 1 1 1	0 1 1 0	54	0 1 0 1	1 0 0 0	58	
(177 MHz)	77		0 1 1 1	0 1 1 1	55	0 1 0 1	1 0 0 1	59	590

WORD	BIT 7	6	5	4	3	2	1	0
0	–	–	–	–	–	–	–	–
1	–	–	–	–	–	–	–	–
2	–	–	–	–	–	–	–	–
3	–	–	–	–	–	–	–	–
4	0	1	0	0	1	0	0	0
5	0	1	0	0	1	0	0	0
6	0	1	0	0	1	0	0	0
7	0	1	0	0	1	0	0	1
8	0	1	0	0	1	0	0	1
9	0	1	0	0	1	0	0	1
10	–	–	–	–	–	–	–	–
11	–	–	–	–	–	–	–	–
12	–	–	–	–	–	–	–	–
13	–	–	–	–	–	–	–	–
14	–	–	–	–	–	–	–	–
15	–	–	–	–	–	–	–	–
16	0	1	0	1	0	0	0	0
17	0	1	0	1	0	0	0	0
18	0	1	0	1	0	0	0	0
19	0	1	0	1	0	0	0	1
20	0	1	0	1	0	0	0	1
21	0	1	0	1	0	0	0	1
22	0	1	0	1	0	0	1	0
23	0	1	0	1	0	0	1	0
24	0	1	0	1	0	0	1	0
25	0	1	0	1	0	0	1	1
26	–	–	–	–	–	–	–	–
27	–	–	–	–	–	–	–	–
28	–	–	–	–	–	–	–	–
29	–	–	–	–	–	–	–	–
30	–	–	–	–	–	–	–	–
31	–	–	–	–	–	–	–	–
32	0	1	0	1	0	0	1	1
33	0	1	0	1	0	0	1	1
34	0	1	0	1	0	1	0	0
35	0	1	0	1	0	1	0	0
36	0	1	0	1	0	1	0	0
37	0	1	0	1	0	1	0	1
38	0	1	0	1	0	1	0	1
39	0	1	0	1	0	1	0	1
40	0	1	0	1	0	1	1	0
41	0	1	0	1	0	1	1	0
42	–	–	–	–	–	–	–	–
43	–	–	–	–	–	–	–	–
44	–	–	–	–	–	–	–	–
45	–	–	–	–	–	–	–	–
46	–	–	–	–	–	–	–	–
47	–	–	–	–	–	–	–	–
48	0	1	0	1	0	1	1	0
49	0	1	0	1	0	1	1	1
50	0	1	0	1	0	1	1	1
51	0	1	0	1	0	1	1	1
52	0	1	0	1	1	0	0	0
53	0	1	0	1	1	0	0	0
54	0	1	0	1	1	0	0	0
55	0	1	0	1	1	0	0	1
56	–	–	–	–	–	–	–	–
57	–	–	–	–	–	–	–	–
58	–	–	–	–	–	–	–	–
59	–	–	–	–	–	–	–	–
60	–	–	–	–	–	–	–	–
61	–	–	–	–	–	–	–	–
62	–	–	–	–	–	–	–	–
63	–	–	–	–	–	–	–	–

The required divider range, 4800 to 5933, is obtained in the following manner: the MC12013 Dual Modulus Prescaler is connected in the divide by 10/11 mode; the modulus control counter uses two MC4016 stages with N_{mc} ranging from 00 to 99, establishing the two least significant digits of N_T. The remaining two digits of N_T are obtained from a three stage programmable counter generating N_{pc}. The least significant stage of the N_{pc} counter is fixed programmed to zero. The required programming for all remaining stages is derived from four channel selector BCD thumbwheel switches. The relationship between N_T and the counters is given by $N_T = MN_{pc} + N_{mc}$; for a typical channel, say 144.33 MHz, $N_T = 4811$ requires that $M = 10$, $N_{pc} = 480$, and $N_{mc} = 11$, or $N_T = (10)(480) + 11 = 4811$.

A general problem associated with synthesizer design arises from the fact that there is not always a one-to-one correspondence between the code provided by the channel selector switches and the code required for proper programming of the counters. For instance, in the example above where 144.33 MHz was selected, the channel selector switches are set to 44.33 while the required divider ratio is 4811. There are numerous solutions for a given translation requirement, however the method shown here using read only memories offers a straightforward design method. While field programmable read only memories (PROMs)[3] are shown, they would normally be used only during development; suitable fixed ROMs are more economical in production quantities. The design procedure for the code conversion is illustrated in Figure 9. The required programming for the two most

3 See the MCM5003 data sheet and AN-550 for details of operation; briefly, one of 64 eight-bit output words is selected by a six-bit address applied to the input. The word located at each address can be field programmed by the user.

FIGURE 10 — N_{mc} PROM #1 PROGRAMMING

	SW #3	SW #4	SW #3	SW #4	PROM WORD	PROM OUTPUT		N_{mc}
			A5 A4	A3 A2 A1 A0		M.S.B	L.S.B.	
(144)	.00		0 0 0 0	0 0 0 0	0	0 0 0 0	0 0 0 0	00
	.03		0 0 0 0	0 0 1 1	3	0 0 0 0	0 0 0 1	01
	.06		0 0 0 0	0 1 1 0	6	0 0 0 0	0 0 1 0	02
	.09		0 0 0 0	1 0 0 1	9	0 0 0 0	0 0 1 1	03
	.12		0 0 0 1	0 0 1 0	18	0 0 0 0	0 1 0 0	04
	.15		0 0 0 1	0 1 0 1	21	0 0 0 0	0 1 0 1	05
	.18		0 0 0 1	1 0 0 0	24	0 0 0 0	0 1 1 0	06
	.21		0 0 1 0	0 0 0 1	33	0 0 0 0	0 1 1 1	07
	.24		0 0 1 0	0 1 0 0	36	0 0 0 0	1 0 0 0	08
	.27		0 0 1 0	0 1 1 1	39	0 0 0 0	1 0 0 1	09
	.30		0 0 1 1	0 0 0 0	48	0 0 0 1	0 0 0 0	10
	.33		0 0 1 1	0 0 1 1	51	0 0 0 1	0 0 0 1	11
	.36		0 0 1 1	0 1 1 0	54	0 0 0 1	0 0 1 0	12
	.39		0 0 1 1	1 0 0 1	57	0 0 0 1	0 0 1 1	13
	.42		0 1 0 0	0 0 1 0	2	0 0 0 1	0 1 0 0	14
	.45		0 1 0 0	0 1 0 1	5	0 0 0 1	0 1 0 1	15
	.48		0 1 0 0	1 0 0 0	8	0 0 0 1	0 1 1 0	16
	.51		0 1 0 1	0 0 0 1	17	0 0 0 1	0 1 1 1	17
	.54		0 1 0 1	0 1 0 0	20	0 0 0 1	1 0 0 0	18
	.57		0 1 0 1	0 1 1 1	23	0 0 0 1	1 0 0 1	19
	.60		0 1 1 0	0 0 0 0	32	0 0 1 0	0 0 0 0	20
	.63		0 1 1 0	0 0 1 1	35	0 0 1 0	0 0 0 1	21
	.66		0 1 1 0	0 1 1 0	38	0 0 1 0	0 0 1 0	22
	.69		0 1 1 0	1 0 0 1	41	0 0 1 0	0 0 1 1	23
	.72		0 1 1 1	0 0 1 0	49	0 0 1 0	0 1 0 0	24
	.75		0 1 1 1	0 1 0 1	53	0 0 1 0	0 1 0 1	25
	.78		0 1 1 1	1 0 0 0	56	0 0 1 0	0 1 1 0	26
	.81		1 0 0 0	0 0 0 1	1	0 0 1 0	0 1 1 1	27
	.84		1 0 0 0	0 1 0 0	4	0 0 1 0	1 0 0 0	28
	.87		1 0 0 0	0 1 1 1	7	0 0 1 0	1 0 0 1	29
	.90		1 0 0 1	0 0 0 0	16	0 0 1 1	0 0 0 0	30
	.93		1 0 0 1	0 0 1 1	19	0 0 1 1	0 0 0 1	31
	.96		1 0 0 1	0 1 1 0	22	0 0 1 1	0 0 1 0	32
(144)	.99		1 0 0 1	1 0 0 1	25	0 0 1 1	0 0 1 1	33

Use with frequency ranges:

144.00 – 144.99	162.00 – 162.99
147.00 – 147.99	165.00 – 165.99
150.00 – 150.99	168.00 – 168.99
153.00 – 153.99	171.00 – 171.99
156.00 – 156.99	174.00 – 174.99
159.00 – 159.99	177.00 – 177.99

significant digits of N_{pc} is shown versus the code provided by switches #1 and #2 of the channel selector. If the four outputs of switch #2 and the two least significant outputs of switch #1 are regarded as address bits A0 through A5 for an MCM5003 PROM, a memory location can be associated with each switch setting. The required N_{pc} programming for each switch setting is then set into the appropriate memory location by the user. In Figure 9, the required programming has been transferred into a truth table to be used while programming the PROM. A similar result for the N_{mc} programming is shown in Figure 10. Note that the PROM shown, N_{mc} PROM #1, selects only N_{mc} numbers 00 through 33. This means that the synthesizer as shown in Figure 8 selects only the adjacent channels in a one megahertz slice of the total band. The frequency ranges that can be selected using N_{mc} PROM #1 are summarized in Figure 10. For other ranges, N_{mc} PROM #1 must be replaced by one of two additional PROMs required for generating the remaining N_{mc} numbers. Appropriate truth tables along with the ranges they can be used with are shown in Figures 11 and 12.

	BIT							
WORD	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0
1	0	0	1	0	0	1	1	1
2	0	0	0	1	0	1	0	0
3	0	0	0	0	0	0	0	1
4	0	0	1	0	1	0	0	0
5	0	0	0	1	0	1	0	1
6	0	0	0	0	0	0	1	0
7	0	0	1	0	1	0	0	1
8	0	0	0	1	0	1	1	0
9	0	0	0	0	0	0	1	1
10	–	–	–	–	–	–	–	–
11	–	–	–	–	–	–	–	–
12	–	–	–	–	–	–	–	–
13	–	–	–	–	–	–	–	–
14	–	–	–	–	–	–	–	–
15	–	–	–	–	–	–	–	–
16	0	0	1	1	0	0	0	0
17	0	0	0	1	0	1	1	1
18	0	0	0	0	0	1	0	0
19	0	0	1	1	0	0	0	1
20	0	0	0	1	1	0	0	0
21	0	0	0	0	0	1	0	1
22	0	0	1	1	0	0	1	0
23	0	0	0	1	1	0	0	1
24	0	0	0	0	0	1	1	0
25	0	0	1	1	0	0	1	1
26	–	–	–	–	–	–	–	–
27	–	–	–	–	–	–	–	–
28	–	–	–	–	–	–	–	–
29	–	–	–	–	–	–	–	–
30	–	–	–	–	–	–	–	–
31	–	–	–	–	–	–	–	–
32	0	0	1	0	0	0	0	0
33	0	0	0	0	0	1	1	1
34	–	–	–	–	–	–	–	–
35	0	0	1	0	0	0	0	1
36	0	0	0	0	1	0	0	0
37	–	–	–	–	–	–	–	–
38	0	0	1	0	0	0	1	0
39	0	0	0	0	1	0	0	1
40	–	–	–	–	–	–	–	–
41	0	0	1	0	0	0	1	1
42	–	–	–	–	–	–	–	–
43	–	–	–	–	–	–	–	–
44	–	–	–	–	–	–	–	–
45	–	–	–	–	–	–	–	–
46	–	–	–	–	–	–	–	–
47	–	–	–	–	–	–	–	–
48	0	0	0	1	0	0	0	0
49	0	0	1	0	0	1	0	0
50	–	–	–	–	–	–	–	–
51	0	0	0	1	0	0	0	1
52	–	–	–	–	–	–	–	–
53	0	0	1	0	0	1	0	1
54	0	0	0	1	0	0	1	0
55	–	–	–	–	–	–	–	–
56	0	0	1	0	0	1	1	0
57	0	0	0	1	0	0	1	1
58	–	–	–	–	–	–	–	–
59	–	–	–	–	–	–	–	–
60	–	–	–	–	–	–	–	–
61	–	–	–	–	–	–	–	–
62	–	–	–	–	–	–	–	–
63	–	–	–	–	–	–	–	–

7

FIGURE 11 – N_{mc} PROM #2 TRUTH TABLE

WORD	BIT 7	6	5	4	3	2	1	0
0	0	1	1	0	0	0	0	0
1	0	1	0	0	0	1	1	1
2	0	0	1	1	0	1	0	0
3	0	1	1	0	0	0	0	1
4	0	1	0	0	1	0	0	0
5	0	0	1	1	0	1	0	1
6	0	1	1	0	0	0	1	0
7	0	1	0	0	1	0	0	1
8	0	0	1	1	0	1	1	0
9	0	1	1	0	0	0	1	1
10	–	–	–	–	–	–	–	–
11	–	–	–	–	–	–	–	–
12	–	–	–	–	–	–	–	–
13	–	–	–	–	–	–	–	–
14	–	–	–	–	–	–	–	–
15	–	–	–	–	–	–	–	–
16	0	1	0	1	0	0	0	0
17	0	0	1	1	0	1	1	1
18	0	1	1	0	0	1	0	0
19	0	1	0	1	0	0	0	1
20	0	0	1	1	1	0	0	0
21	0	1	1	0	0	1	0	1
22	0	1	0	1	0	0	1	0
23	0	0	1	1	1	0	0	1
24	0	1	1	0	0	1	1	0
25	0	1	0	1	0	0	1	1
26	–	–	–	–	–	–	–	–
27	–	–	–	–	–	–	–	–
28	–	–	–	–	–	–	–	–
29	–	–	–	–	–	–	–	–
30	–	–	–	–	–	–	–	–
31	–	–	–	–	–	–	–	–
32	0	1	0	0	0	0	0	0
33	–	–	–	–	–	–	–	–
34	0	1	0	1	0	1	0	0
35	0	1	0	0	0	0	0	1
36	–	–	–	–	–	–	–	–
37	0	1	0	1	0	1	0	1
38	0	1	0	0	0	0	1	0
39	–	–	–	–	–	–	–	–
40	0	1	0	1	0	1	1	0
41	0	1	0	0	0	0	1	1
42	–	–	–	–	–	–	–	–
43	–	–	–	–	–	–	–	–
44	–	–	–	–	–	–	–	–
45	–	–	–	–	–	–	–	–
46	–	–	–	–	–	–	–	–
47	–	–	–	–	–	–	–	–
48	–	–	–	–	–	–	–	–
49	0	1	0	1	0	1	1	1
50	0	1	0	0	0	1	0	0
51	–	–	–	–	–	–	–	–
52	0	1	0	1	1	0	0	0
53	0	1	0	0	0	1	0	1
54	–	–	–	–	–	–	–	–
55	0	1	0	1	1	0	0	1
56	0	1	0	0	0	1	1	0
57	–	–	–	–	–	–	–	–
58	–	–	–	–	–	–	–	–
59	–	–	–	–	–	–	–	–
60	–	–	–	–	–	–	–	–
61	–	–	–	–	–	–	–	–
62	–	–	–	–	–	–	–	–
63	–	–	–	–	–	–	–	–

Use with frequency ranges:

145.02 – 145.98
148.02 – 148.98
151.02 – 151.98
154.02 – 154.98
157.02 – 157.98
160.02 – 160.98
163.02 – 163.98
166.02 – 166.98
169.02 – 169.98
172.02 – 172.98
175.02 – 175.98

FIGURE 12 – N_{mc} PROM #3 TRUTH TABLE

WORD	BIT 7	6	5	4	3	2	1	0
0	1	0	0	0	0	0	0	0
1	0	1	1	0	0	1	1	1
2	1	0	0	1	0	1	0	0
3	1	0	0	0	0	0	0	1
4	0	1	1	0	1	0	0	0
5	1	0	0	1	0	1	0	1
6	1	0	0	0	0	0	1	0
7	0	1	1	0	1	0	0	1
8	1	0	0	1	0	1	1	0
9	1	0	0	0	0	0	1	1
10	–	–	–	–	–	–	–	–
11	–	–	–	–	–	–	–	–
12	–	–	–	–	–	–	–	–
13	–	–	–	–	–	–	–	–
14	–	–	–	–	–	–	–	–
15	–	–	–	–	–	–	–	–
16	0	1	1	1	0	0	0	0
17	1	0	0	1	0	1	1	1
18	1	0	0	0	0	1	0	0
19	0	1	1	1	0	0	0	1
20	1	0	0	1	1	0	0	0
21	1	0	0	0	0	1	0	1
22	0	1	1	1	0	0	1	0
23	1	0	0	1	1	0	0	1
24	1	0	0	0	0	1	1	0
25	0	1	1	1	0	0	1	1
26	–	–	–	–	–	–	–	–
27	–	–	–	–	–	–	–	–
28	–	–	–	–	–	–	–	–
29	–	–	–	–	–	–	–	–
30	–	–	–	–	–	–	–	–
31	–	–	–	–	–	–	–	–
32	–	–	–	–	–	–	–	–
33	1	0	0	0	0	1	1	1
34	0	1	1	1	0	1	0	0
35	–	–	–	–	–	–	–	–
36	–	–	–	–	–	–	–	–
37	0	1	1	1	0	1	0	1
38	1	0	0	0	1	0	0	0
39	1	0	0	0	1	0	0	1
40	0	1	1	1	0	1	1	0
41	–	–	–	–	–	–	–	–
42	–	–	–	–	–	–	–	–
43	–	–	–	–	–	–	–	–
44	–	–	–	–	–	–	–	–
45	–	–	–	–	–	–	–	–
46	–	–	–	–	–	–	–	–
47	–	–	–	–	–	–	–	–
48	1	0	0	1	0	0	0	0
49	0	1	1	1	0	1	1	1
50	–	–	–	–	–	–	–	–
51	1	0	0	1	0	0	0	1
52	0	1	1	1	1	0	0	0
53	–	–	–	–	–	–	–	–
54	1	0	0	1	0	0	1	0
55	0	1	1	1	1	0	0	1
56	–	–	–	–	–	–	–	–
57	1	0	0	0	0	0	1	1
58	–	–	–	–	–	–	–	–
59	–	–	–	–	–	–	–	–
60	–	–	–	–	–	–	–	–
61	–	–	–	–	–	–	–	–
62	–	–	–	–	–	–	–	–
63	–	–	–	–	–	–	–	–

Use with frequency ranges:

146.01 – 146.97
149.01 – 149.97
152.01 – 152.97
155.01 – 155.97
158.01 – 158.97
161.01 – 161.97
164.01 – 164.97
167.01 – 167.97
170.01 – 170.97
173.01 – 173.97
176.01 – 176.97

MOTOROLA

MC12015
MC12016
MC12017

Advance Information

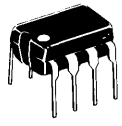
LOW-POWER TWO-MODULUS PRESCALER

The MC12015, MC12016 and MC12017 are two-modulus prescalers which will divide by 32 and 33, 40 and 41, and 64 and 65 respectively. An internal regulator is provided to allow these devices to be used over a wide range of power-supply voltages. Regulated operation is obtained by connecting supply voltages of 4.5 to 5.5 V to both Pin 7 and Pin 8. Unregulated operation is obtained by connecting voltages greater than 5.5 to Pin 8 and leaving Pin 7 open.

- 225 MHz Toggle Frequency
- Low-Power—7.5 mA Max at 6.8 V
- Control Input and Output are Compatible with Standard CMOS
- Connecting Pins 2 and 3 Allows Driving One TTL Load
- Supply Voltage 4.5 V to 9.5 V

MECL PLL COMPONENTS

LOW-POWER
TWO - MODULUS
PRESCALER



P SUFFIX
PLASTIC PACKAGE
CASE 626

MAXIMUM RATINGS

Characteristic	Symbol	Range	Unit
Regulated Voltage, Pin 7	V_{reg}	8.0	Vdc
Power Supply Voltage, Pin 8	V_{CC}	10.0	Vdc
Operating Temperature Range	T_A	-40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +175	°C

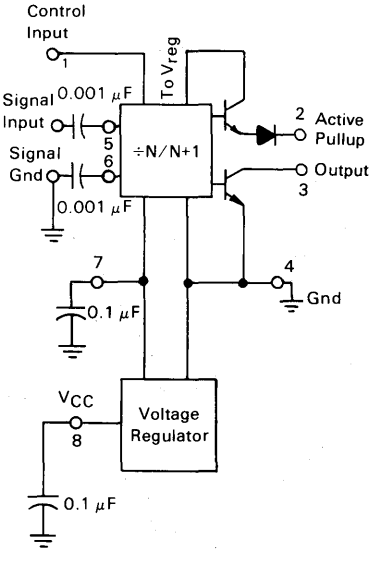
ELECTRICAL CHARACTERISTICS (V_{CC} = 5.5 to 9.5, V_{reg} = 4.5 to 5.5 V, T_A = -40°C to +85°C)

Characteristic	Symbol	Min	Typ	Max	Unit
Toggle Frequency (Sine wave input)	f_{max}	225	—	—	MHz
	f_{min}	—	—	35	MHz
Supply Current	I_{CC}	—	6.0	7.8	mA
Control Input High (÷32, 40 or 64)		2.0	—	—	V
Control Input Low (÷33, 41 or 65)		—	—	0.8	V
Output Voltage High* (I_{source} = 50 μA)	V_{OH}	2.5	—	—	V
Output Voltage Low* (I_{sink} = 2 mA)	V_{OL}	—	—	0.5	V
Input Voltage Sensitivity 35 MHz	V_{in}	400	—	800	mVPP
50-255 MHz		200	—	800	
PLL Response Time (Notes 1 and 2)	t_{PLL}	—	—	t_{out} -70	ns

Notes:
1. t_{PLL} = the period of time the PLL has from the prescaler rising output transition (50%) to the modulus control input edge transition (50%) to ensure proper modulus selection.
2. t_{out} = period of output waveform.

*Pin 2 connected to Pin 3

PRESCALER BLOCK DIAGRAM



7

MOTOROLA

MC12018

Product Preview

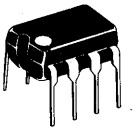
÷128/129 520 MHz
LOW-POWER TWO-MODULUS PRESCALER

The MC12018 is a two-modulus prescaler which divides by 128 and 129. An internal regulator is provided to allow this device to be used over a wide range of power-supply voltages. Regulated operation is obtained by connecting supply voltages of 4.5 to 5.5 V to both Pin 7 and Pin 8. Unregulated operation is obtained by connecting voltages greater than 5.5 to Pin 8 and leaving Pin 7 open.

- 520 MHz Toggle Frequency
- Low-Power — 7.0 mA Typical
- Control Input Is Compatible with Standard CMOS and TTL
- Supply Voltage 4.5 V to 9.5 V
- The Specifications of This Product Preview Are Design Goals Only

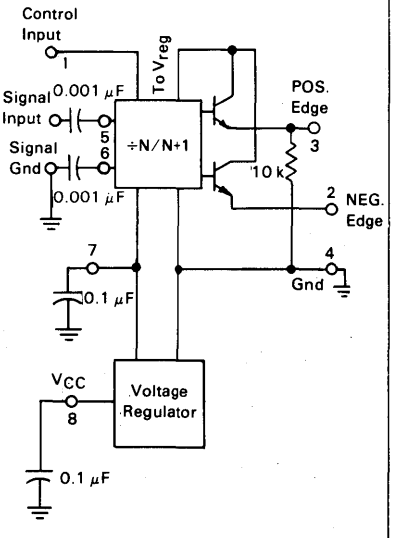
MECL PLL COMPONENTS

÷128/129
LOW-POWER
TWO-MODULUS
PRESCALER



P SUFFIX
PLASTIC PACKAGE
CASE 626

PRESCALER BLOCK DIAGRAM



MAXIMUM RATINGS

Characteristic	Symbol	Range	Unit
Regulated Voltage, Pin 7	V_{reg}	8.0	Vdc
Power Supply Voltage, Pin 8	V_{CC}	10.0	Vdc
Operating Temperature Range	T_A	-40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +175	°C

ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.5 to 9.5, V_{reg} = 4.5 to 5.5 V, T_A = -40°C to +85°C)

Characteristic	Symbol	Min	Typ	Max	Unit
Toggle Frequency (Sine Wave Input)	f_{max}	520	—	—	MHz
Supply Current (Pin 8)	I_{CC}	—	7.0	—	mA
Control Input High (÷ 128)	V_{IH}	2.0	—	—	V
Control Input Low (÷ 129)	V_{IL}	—	—	0.8	V
Differential Output Voltage (I_{sink} = 200 μA)	V_{out}	0.8	1.0	—	V
PLL Response Time (Notes 1 and 2)	t_{PLL}	—	—	t_{out}-35	ns
Input Voltage Sensitivity	V_{in}	200	—	800	mVpp

Notes:
1. t_{PLL} = the period of time the PLL has from the prescaler rising output transition (50%) to the modulus control input edge transition (50%) to ensure proper modulus selection.
2. t_{out} = period of output waveform

MOTOROLA

MC12019

Advance Information

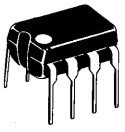
LOW-POWER TWO-MODULUS PRESCALER

The MC12019 is a divide by 20 and 21 two-modulus prescaler. It will divide by 20 when the modulus control input is high and by 21 when the modulus control input is low.

- 225 MHz Toggle Frequency
- Low-Power—7.5 mA Max at 5.5 V
- Control Input Compatible with Standard Motorola CMOS Synthesizers
- Emitter Follower Outputs

MECL PLL COMPONENTS

LOW-POWER TWO - MODULUS PRESCALER ÷20/21



P SUFFIX
PLASTIC PACKAGE
CASE 626

MAXIMUM RATINGS

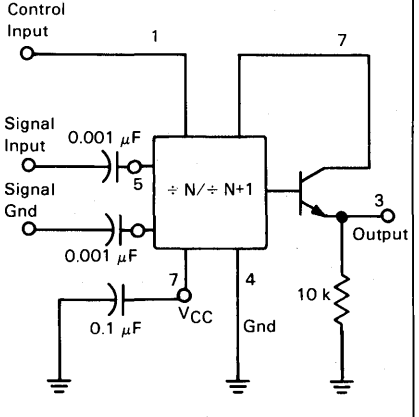
Characteristic	Symbol	Range	Unit
Power Supply Voltage, Pin 7	V_{CC}	8.0	Vdc
Operating Temperature Range	T_A	-40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +175	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 4.5 to 5.5 V, T_A = -40° to +85° C)

Characteristic	Symbol	-40°C		25°C		85°C		Unit
		Min	Max	Min	Max	Min	Max	
Toggle Frequency (Sine wave input)	f_{max} f_{min}	225 —	— 35	225 —	— 35	225 —	— 35	MHz MHz
Supply Current	I_{CC}	—	7.5	—	7.5	—	7.5	mA
Control Input High (÷20)		2.0	—	2.0	—	2.0	—	V
Control Input Low (÷20)		—	0.8	—	0.8	—	0.8	V
Output Voltage Swing	V_{out}	—	600	—	600	—	600	mV_{pp}
Input Voltage Sensitivity 35 MHz 50-255 MHz	V_{in}	 400 200	 800 800	 400 200	 800 800	 400 200	 800 800	
PLL Response Time (Notes 1 and 2)	t_{PLL}	—	t_{out}-70	—	t_{out}-70	—	t_{out}-70	ns

Notes:
1. t_{PLL} = the time the PLL has from the prescaler rising output transition (50%) to the modulus control input edge transition (50%) to ensure proper modulus selection.
2. t_{out} = period of output waveform.

PRESCALER BLOCK DIAGRAM



7

MOTOROLA

MC12022

Product Preview

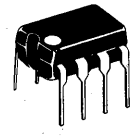
÷128/129 1.0 GHz
LOW-POWER TWO-MODULUS PRESCALER

The MC12022 is a two-modulus prescaler which divides by 128 and 129. An internal regulator is provided to allow this device to be used over a wide range of power-supply voltages. Regulated operation is obtained by connecting supply voltages of 4.5 to 5.5 V to both Pin 7 and Pin 8. Unregulated operation is obtained by connecting voltages greater than 5.5 to Pin 8 and leaving Pin 7 open.

- 1.0 GHz Toggle Frequency
- Low-Power 14 mA Typical
- Control Input Is Compatible with Standard CMOS and TTL
- Supply Voltage 4.5 V to 9.5 V
- Propagation Delay 25 ns Typical
- The Specifications of This Product Preview Are Design Goals Only

MECL PLL COMPONENTS

÷128/129
LOW-POWER
TWO-MODULUS
PRESCALER



P SUFFIX
PLASTIC PACKAGE
CASE 626

MAXIMUM RATINGS

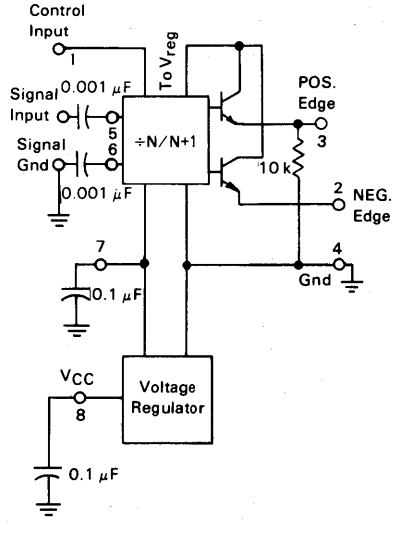
Characteristic	Symbol	Range	Unit
Regulated Voltage, Pin 7	V_{reg}	8.0	Vdc
Power Supply Voltage, Pin 8	V_{CC}	10.0	Vdc
Operating Temperature Range	T_A	-40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +175	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.5 to 9.5, V_{reg} = 4.5 to 5.5 V, T_A = -40°C to +85°C)

Characteristic	Symbol	Min	Typ	Max	Unit
Toggle Frequency (Sine Wave Input)	f_{max}	1.0	—	—	GHz
Supply Current (Pin 8)	I_{CC}	—	14	—	mA
Control Input High (÷ 128)	V_{IH}	2.0	—	—	V
Control Input Low (÷ 129)	V_{IL}	—	—	0.8	V
Differential Output Voltage (I_{sink} = 200 μA)	V_{out}	0.8	1.0	—	V
PLL Response Time (Notes 1 and 2)	t_{PLL}	—	—	t_{out} -50	ns
Input Voltage Sensitivity	V_{in}	200	—	800	mVpp

Notes:
1. t_{PLL} = the period of time the PLL has from the prescaler rising output transition (50%) to the modulus control input edge transition (50%) to ensure proper modulus selection.
2. t_{out} = period of output waveform.

PRESCALER BLOCK DIAGRAM



7

MOTOROLA

MC12023

Advance Information

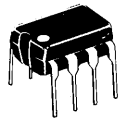
MECL PLL COMPONENTS

LOW-POWER PRESCALER ÷ 64

÷ 64, 225 MHz, LOW-POWER PRESCALER

The MC12023 is a new member of Motorola's PLL family. The MC12023 is a prescaler which will divide by 64. This device may be operated over a wide range of supply voltages (3.2 to 5.5 V). Because of this range of supply voltages the MC12023 is very suitable for hand-held, battery-operated devices.

- 225 MHz Toggle Frequency
- Low-Power — 4.0 mA Maximum at 5.5 V
- Operating Supply Voltage — 3.2 V to 5.5 V
- Connecting Pins 2 and 3 Allows Driving One TTL Load



P SUFFIX
PLASTIC PACKAGE
CASE 626

MAXIMUM RATINGS

Characteristic	Symbol	Range	Unit
Power Supply Voltage	V_{CC}	0 to +7.0	Vdc
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +175	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 3.2 to 5.5 V, T_A = 0°C to +70°C)

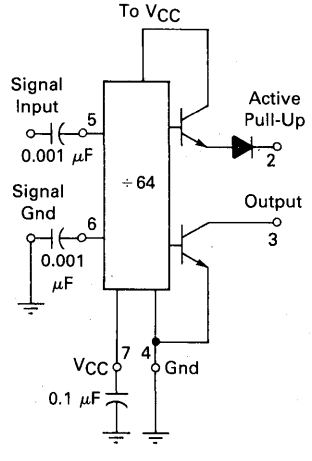
Characteristic	Symbol	Min	Typ	Max	Unit
Toggle Frequency	f_{max}	225	—	—	MHz
(Sine wave input)	f_{min}	—	—	20	MHz
Supply Current	I_{CC}	—	3.5**	4.0	mA
Output Voltage High* (I_{source} = 50 μA, V_{CC} = 3.2 V)	V_{OH}	1.2	1.4	—	V
Output Voltage High* (I_{source} = 50 μA, V_{CC} = 5.0 V)	V_{OH}	3.5	—	—	V
Output Voltage Low* (I_{sink} = 2.0 mA)	V_{OL}	—	—	0.5	V
Input Voltage Sensitivity 35 MHz 50–225 MHz	V_{in}	 400 200	 — —	 800 800	mVpp
AC Input Resistance	R_{in}	—	TBA	—	kΩ
Input Capacitance	C_{in}	—	TBA	—	pF

*Pin 2 connected to Pin 3
**V_{CC} = 4.5 V

TBA — To Be Announced.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

PRESCALER BLOCK DIAGRAM



7

MOTOROLA

MC12040/ MC12540

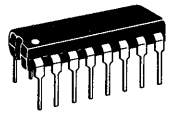
PHASE-FREQUENCY DETECTOR

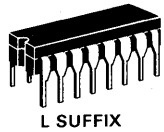
The MC12040 is a phase-frequency detector intended for use in systems requiring zero phase and frequency difference at lock. In combination with a voltage controlled oscillator (such as the MC1648), it is useful in a broad range of phase-locked loop applications. Operation of this device is identical to that of Phase Detector #1 of the MC4044. A discussion of the theory of operation and applications information is given on the MC4344/4044 data sheet.

Operating Frequency = 80 MHz typical

PHASE-FREQUENCY DETECTOR

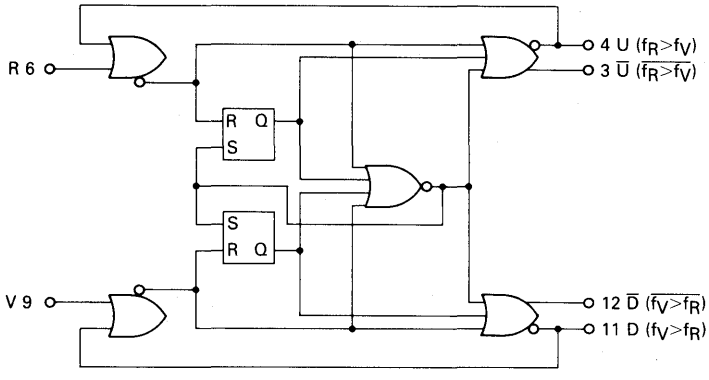
P SUFFIX
PLASTIC PACKAGE
CASE 646





L SUFFIX
CERAMIC PACKAGE
CASE 632-02

LOGIC DIAGRAM



V_{CC1} = Pin 1
V_{CC2} = Pin 14
V_{EE} = Pin 7

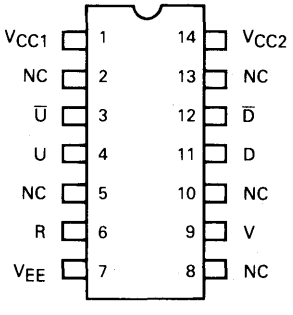
INPUT		OUTPUT			
R	V	U	D	$\overline{U}$	$\overline{D}$
0	0	X	X	X	X
0	1	X	X	X	X
1	1	X	X	X	X
0	1	X	X	X	X
1	1	1	0	0	1
0	1	1	0	0	1
1	1	1	0	0	1
1	0	1	0	0	1
1	1	0	0	1	1
1	0	0	0	1	1
1	1	0	1	1	0
1	0	0	1	1	0
1	1	0	1	1	0
0	1	0	1	1	0
1	1	0	0	1	0

X = Don't Care

TRUTH TABLE

This is not strictly a functional truth table; i.e., it does not cover all possible modes of operation. However it gives a sufficient number of tests to ensure that the device will function properly in all modes of operation.

PIN ASSIGNMENT

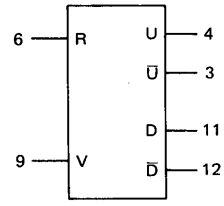


NC — No Connection

7

ELECTRICAL CHARACTERISTICS

The MC12040 has been designed to meet the dc specifications shown in the test table after thermal equilibrium has been established. Outputs are terminated through a 50 ohm resistor to +3.0 V for +5.0 V tests and through a 50 ohm resistor to −2.0 V for −5.2 V tests.



@ Test Temperature	TEST VOLTAGE VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}
0°C	-0.840	-1.870	-1.145	-1.490	-5.2
25°C	-0.810	-1.850	-1.105	-1.475	-5.2
75°C	-0.720	-1.830	-1.045	-1.450	-5.2

Supply Voltage = -5.2V

Characteristic	Symbol	Pin Under Test	MC12040 0°C Min	0°C Max	25°C Min	25°C Max	+75°C Min	+75°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	7	–	–	-120	-60	–	–	mAdc	–	–	–	–	7	1,14
Input Current	I_{INH}	6	–	–	–	350	–	–	µAdc	6	–	–	–	7	1,14
		9	–	–	–	350	–	–	µAdc	9	–	–	–	7	1,14
Logic "1" Output Voltage	V_{OH} ①	3	-1.000	-0.840	-0.960	-0.810	-0.900	-0.720	Vdc	–	–	–	–	7	1,14
		4	↓	↓	↓	↓	↓	↓		–	–	–	–	↓	↓
		11								–	–	–	–		
		12								–	–	–	–		
Logic "0" Output Voltage	V_{OL} ①	3	-1.870	-1.635	-1.850	-1.620	-1.830	-1.595	Vdc	–	–	–	–	7	1,14
		4	↓	↓	↓	↓	↓	↓		–	–	–	–	↓	↓
		11								–	–	–	–		
		12								–	–	–	–		
Logic "1" Threshold Voltage	V_{OHA} ②	3	-1.020	–	-0.980	–	-0.920	–	Vdc	–	–	6,9	–	7	1,14
		4	↓		↓		↓				–			↓	↓
		11								–	–		–		
		12								–	–		–		
Logic "0" Threshold Voltage	V_{OLA} ②	3	–	-1.615	–	-1.600	–	-1.575	Vdc	–	–	9	6	7	1,14
		4		↓		↓		↓			–	6	9	↓	↓
		11								–	–	9	6		
		12								–	–	6	9		

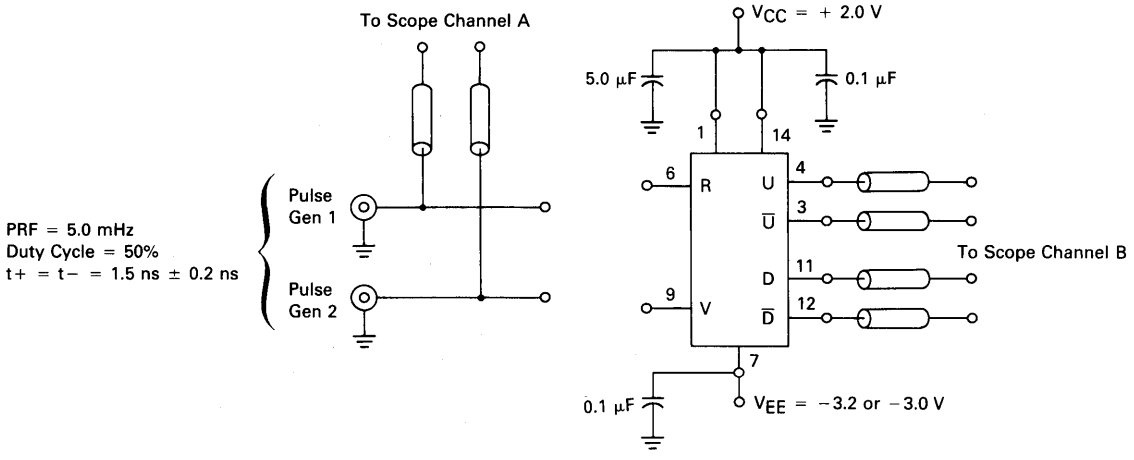
@ Test Temperature	TEST VOLTAGE VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{CC}
0°C	+4.160	+3.130	+3.855	+3.510	+5.0
25°C	+4.190	+3.150	+3.895	+3.525	+5.0
75°C	+4.280	+3.170	+3.955	+3.550	+5.0

Supply Voltage = +5.0V

Characteristic	Symbol	Pin Under Test	MC12040 0°C Min	0°C Max	25°C Min	25°C Max	+75°C Min	+75°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{CC}	(V_{EE}) Gnd
Power Supply Drain Current	I_E	7			-115	-60			mAdc					1,14	7
Input Current	I_{INH}	6				350			µAdc	6	–			1,14	7
		9				350			µAdc	9				1,14	7
Logic "1" Output Voltage	V_{OH} ①	3	4.000	4.160	4.040	4.190	4.100	4.280	Vdc					1,14	7
		4	↓	↓	↓	↓	↓	↓						↓	↓
		11													
		12													
Logic "0" Output Voltage	V_{OL} ①	3	3.190	3.430	3.210	3.440	3.230	3.470	Vdc					1,14	7
		4	↓	↓	↓	↓	↓	↓						↓	↓
		11													
		12													
Logic "1" Threshold Voltage	V_{OHA} ②	3	3.980	–	4.020		4.080		Vdc			6,9		1,14	7
		4	↓		↓		↓							↓	↓
		11													
		12													
Logic "0" Threshold Voltage	V_{OLA} ②	3		3.450		3.460		3.490	Vdc			9	6	1,14	7
		4		↓		↓		↓				6	9	↓	↓
		11										9	6		
		12										6	9		

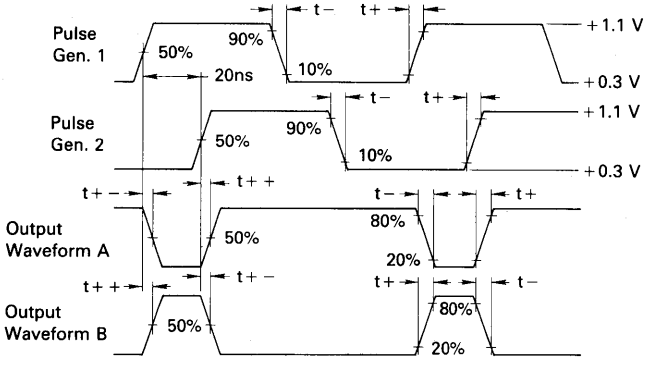
7

AC TESTS



NOTES:

1. All input and output cables to the scope are equal lengths of 50 Ω coaxial cable.
2. Unused input and outputs are connected to a 50 Ω resistor to ground.
3. The device under test must be preconditioned before performing the ac tests. Preconditioning may be accomplished by applying pulse generator 1 for a minimum of two pulses prior to pulse generator 2. The device must be preconditioned again when inputs to pins 6 and 9 are interchanged. The same technique applies.



Characteristic	Symbol	Pin Under Test	Output Waveform	MC12040 0°C Max	MC12040 +25°C Max	MC12040 +75°C Max	MC12540 -55°C Max	MC12540 +25°C Max	MC12540 +125°C Max	Unit	TEST VOLTAGES/WAVEFORMS APPLIED TO PINS LISTED BELOW: Pulse Gen. 1	Pulse Gen. 2	VEE -3.0 or -3.2 V	VCC +2.0 V
Propagation Delay	t_{6+4+}	6,4	B	4.6	4.6	5.6	4.6	4.6	5.0	ns	6	9	7	1,14
	t_{6+12+}	6,12	A	6.0	6.0	7.2	6.0	6.0	6.6		9	6		
	t_{6+3-}	6,3	A	4.5	4.5	5.5	4.5	4.5	4.9		6	9		
	t_{6+11-}	6,11	B	6.4	6.4	7.7	6.4	6.4	7.0		9	6		
	t_{9+11+}	9,11	B	4.6	4.6	5.6	4.6	4.6	5.0		9	6		
	t_{9+3+}	9,3	A	6.0	6.0	7.2	6.0	6.0	6.6		6	9		
	t_{9+12-}	9.12	A	4.5	4.5	5.5	4.5	4.5	4.9		9	6		
	t_{9+4-}	9,4	B	6.4	6.4	7.7	6.4	6.4	7.0		6	9		
Output Rise Time	t_{3+}	3	A	3.4	3.4	3.8	3.4	3.4	3.8	ns	6	9	7	1,14
	t_{4+}	4	B								6	9		
	t_{11+}	11	B								9	6		
	t_{12+}	12	A								9	6		
Output Fall Time	t_{3-}	3	A	3.4	3.4	3.8	3.4	3.4	3.8	ns	6	9	7	1,14
	t_{4-}	4	B								6	9		
	t_{11-}	11	B								9	6		
	t_{12-}	12	A								9	6		

APPLICATIONS INFORMATION

The MC12040 is a logic network designed for use as a phase comparator for MECL-compatible input signals. It determines the "lead" or "lag" phase relationship and the time difference between the leading edges of the waveforms. Since these edges occur only once per cycle, the detector has a range of $\pm 2\pi$ radians.

Operation of the device may be illustrated by assuming two waveforms, R and V (Figure 1), of the same frequency but differing in phase. If the logic had established by past history that R was leading V, the U output of the detector (pin 4) would produce a positive pulse width equal to the phase difference and the D output (pin 11) would simply remain low.

On the other hand, it is also possible that V was leading R (Figure 1), giving rise to a positive pulse on the D output and a constant low level on the U output pin. Both outputs for the sample condition are valid since the determination of lead or lag is dependent on past edge crossing and initial conditions at start-up. A stable phase-locked loop will result from either condition.

Phase error information is contained in the output duty cycle — that is, the ratio of the output pulse width to total period. By integrating or low-pass filtering the outputs of the detector and shifting the level to accommodate ECL swings, usable analog information for the voltage-controlled oscillator can be developed. A circuit useful for this function is shown in Figure 2.

Proper level shifting is accomplished by differentially driving the operational amplifier from the normally high outputs of the phase detector ($\overline{U}$ and $\overline{D}$). Using this technique the quiescent differential voltage to the operational amplifier is zero (assuming matched "1" levels from the phase detector). The $\overline{U}$ and $\overline{D}$ outputs are then used to pass along phase information to the operational amplifier. Phase error summing is accomplished through resistors R1 connected to the inputs of the operational amplifier. Some R-C filtering imbedded within the input network (Figure 2) may be very beneficial since the very narrow correctional pulses of the MC12040 would not normally be integrated by the amplifier. General design guides for calculating R1, R2, and C are included in the MC4044 data sheet. Phase detector gain for this configuration is approximately 0.16 volts/radian.

System phase error stems from input offset voltage in the operational amplifier, mismatching of nominally equal resistors, and mismatching of phase detector "high" states between the outputs used for threshold setting and phase measuring. All these effects are reflected in the gain constant. For example, a 16 mV offset voltage in the amplifier would cause an error of 0.016/0.16 = 0.1 radian or 5.7 degrees of error. Phase error can be trimmed to zero initially by trimming either input offset or one of the threshold resistors (R1 in Figure 2). Phase error over temperature depends on how much the offending parameters drift.

FIGURE 1 — TIMING DIAGRAM

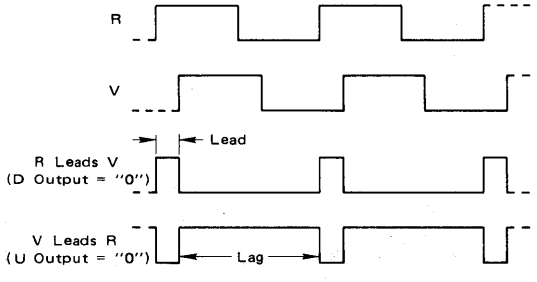
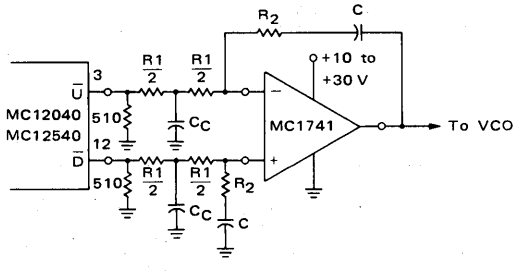


FIGURE 2 — TYPICAL FILTER AND SUMMING NETWORK



MOTOROLA

MC12061 • MC12561

Military

CRYSTAL OSCILLATOR

The MC12061 and MC120561 are designed for use with an external crystal to form a crystal controlled oscillator. In addition to the fundamental series mode crystal, two bypass capacitors are required (plus usual power supply pin bypass capacitors). Translators are provided internally for MECL and TTL outputs.

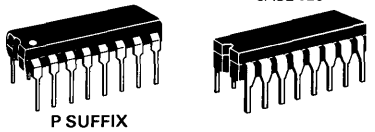
Frequency Range = 2.0 MHz to 20 MHz

Single Supply Operation: + 5.0 Vdc or −5.2 Vdc

Three Outputs Available:

1. Complementary Sine Wave (600 mVp-p typ)
2. Complementary MECL
3. Single Ended TTL

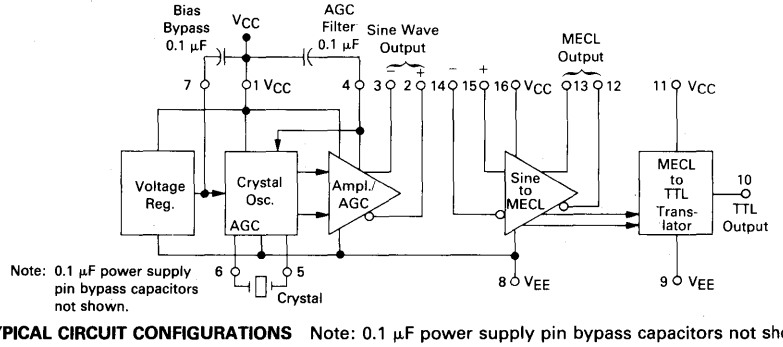
CRYSTAL OSCILLATOR



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

LOGIC DIAGRAM



TYPICAL CIRCUIT CONFIGURATIONS Note: 0.1 µF power supply pin bypass capacitors not shown.

FIGURE 2 — SINE WAVE OUTPUT

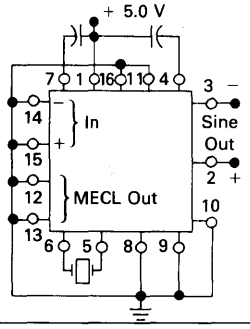


FIGURE 3 — MTTL OUTPUT

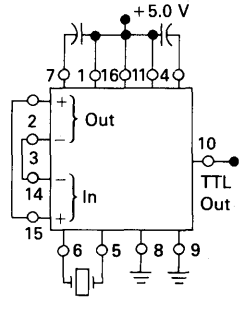


FIGURE 4 — MECL OUTPUT
(+5.0 V Supply)

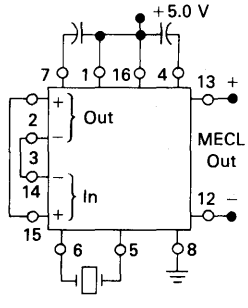
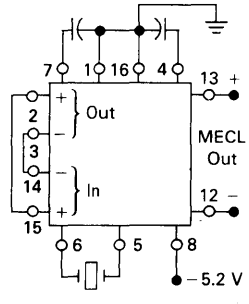


FIGURE 5 — MECL OUTPUT
(−5.2 V Supply)



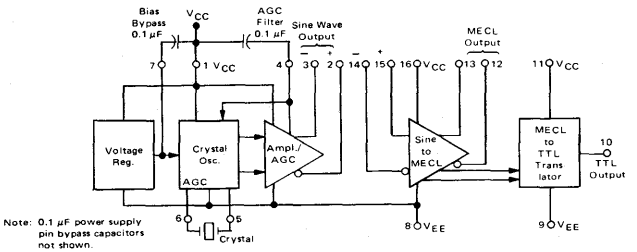
CRYSTAL REQUIREMENTS

Note: Start-up stabilization time is a function of crystal series resistance. The lower the resistance, the faster the circuit stabilizes.

Characteristic	MC12061/12561
Mode of Operation	Fundamental Series Resonance
Frequency Range	2.0 MHz - 20 MHz
Series Resistance, R1	Minimum at Fundamental
Maximum Effective Resistance, $R_{E(max)}$	155 ohms

7

ELECTRICAL CHARACTERISTICS

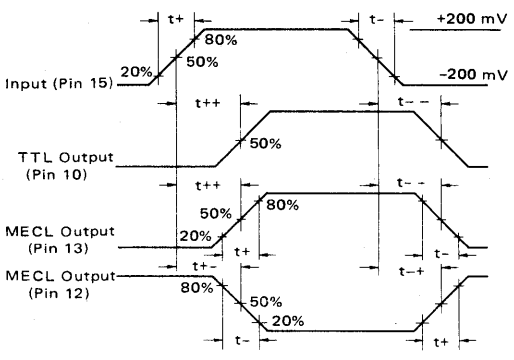


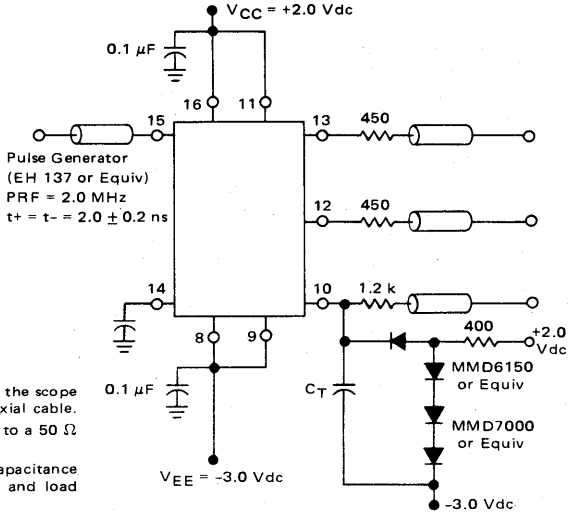
	@ Test Temperature	TEST VOLTAGE/CURRENT VALUES											
		Volts								mA			
		V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{IHT}	V_{CCL}	V_{CC}	V_{CCH}	I_{OL}	I_{OH}	I_L	
MC12561	-55°C	4.07	3.18	3.72	3.49	4.0	4.5	5.0	5.5	16	-0.4	-2.5	
MC12561	+25°C	4.19	3.21	3.90	3.52	4.0	4.5	5.0	5.5	16	-0.4	-2.5	
MC12561	+125°C	4.37	3.25	4.03	3.60	4.0	4.5	5.0	5.5	16	-0.4	-2.5	
MC12061	0°C	4.16	3.19	3.86	3.51	4.0	4.75	5.0	5.25	16	-0.4	-2.5	
MC12061	+25°C	4.19	3.21	3.90	3.52	4.0	4.75	5.0	5.25	16	-0.4	-2.5	
MC12061	+75°C	4.28	3.23	3.96	3.55	4.0	4.75	5.0	5.25	16	-0.4	-2.5	

Characteristic	Symbol	Pin Under Test	MC12561 -55°C Min	MC12561 -55°C Max	MC12561 +25°C Min	MC12561 +25°C Typ	MC12561 +25°C Max	MC12561 +125°C Min	MC12561 +125°C Max	MC12061 0°C Min	MC12061 0°C Max	MC12061 +25°C Min	MC12061 +25°C Typ	MC12061 +25°C Max	MC12061 +75°C Min	MC12061 +75°C Max	Unit	TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{IHT}	V_{CCL}	V_{CC}	V_{CCH}	I_{OL}	I_{OH}	I_L	Gnd
Power Supply Drain Current – MC12061/12561	I_{CC}	1	--	--	18	23	28	--	--	--	--	18	23	28	--	--	mAdc	--	--	--	--	--	--	1	--	--	--	--	8
		11	--	--	--	3.0	4.0	--	--	--	--	--	3.0	4.0	--	--		14	15	--	--	--	--	11,16	--	--	--	--	8,9
		16	--	--	13	16	19	--	--	--	--	13	16	19	--	--		--	--	--	--	--	--	16	--	--	--	--	8
Input Current	I_{INH}	14	--	--	--	--	250	--	--	--	--	--	--	250	--	--	μAdc	14	15	--	--	--	--	16	--	--	--	--	8
		15	--	--	--	--	250	--	--	--	--	--	--	250	--	--	μAdc	15	14	--	--	--	--	16	--	--	--	--	8
	I_{INL}	14	--	--	--	--	1.0	--	--	--	--	--	--	1.0	--	--	μAdc	15	--	--	--	--	--	16	--	--	--	--	8,14
		15	--	--	--	--	1.0	--	--	--	--	--	--	1.0	--	--	μAdc	14	--	--	--	--	--	16	--	--	--	--	8,15
Differential Offset Voltage MC12061/12561	ΔV	4 to 7	--	--	40	--	325	--	--	--	--	40	--	325	--	--	mVdc	--	--	--	--	5,6	--	1	--	--	--	--	8
		2 to 3	--	--	-100	0	+100	--	--	--	--	-200	0	+200	--	--		--	--	--	--	4	--	1	--	--	--	--	8
Output Voltage Level	V_{out}	2	--	--	--	3.5	--	--	--	--	--	--	3.5	--	--	--	Vdc	--	--	--	--	4	--	1	--	--	--	--	8
		3	--	--	--	3.5	--	--	--	--	--	--	3.5	--	--	--	Vdc	--	--	--	--	4	--	1	--	--	--	--	8
Logic "1" Output Voltage	V_{OH1}*	12	3.92	4.07	4.04	--	4.19	4.17	4.37	4.00	4.16	4.04	--	4.19	4.10	4.28	Vdc	14	15	--	--	--	--	16	--	--	--	12	8
		13	3.92	4.07	4.04	--	4.19	4.17	4.37	4.00	4.16	4.04	--	4.19	4.10	4.28	Vdc	15	14	--	--	--	--	16	--	--	--	13	8
	V_{OH2}	10	2.4	--	2.4	--	--	2.4	--	2.4	--	2.4	--	--	2.4	--	Vdc	15	14	--	--	--	11,16	--	--	--	10	--	8,9
Logic "0" Output Voltage	V_{OL1}*	12	2.97	3.39	3.00	--	3.44	3.04	3.50	2.98	3.43	3.00	--	3.44	3.02	3.47	Vdc	15	14	--	--	--	--	16	--	--	--	12	8
		13	2.97	3.39	3.00	--	3.44	3.04	3.50	2.98	3.43	3.00	--	3.44	3.02	3.47	Vdc	14	15	--	--	--	--	16	--	--	--	13	8
	V_{OL2}	10	--	0.5	--	--	0.5	--	0.5	--	0.5	--	--	0.5	--	0.5	Vdc	14	15	--	--	--	11,16	--	--	10	--	--	8,9
		10	--	0.5	--	--	0.5	--	0.5	--	0.5	--	--	0.5	--	0.5	Vdc	14	15	--	--	--	--	--	11,16	10	--	--	8,9
Logic "1" Threshold Voltage	V_{OHA}	12	3.90	--	4.02	--	--	4.15	--	3.98	--	4.02	--	--	4.08	--	Vdc	--	--	14	15	--	--	16	--	--	--	12	8
		13	3.90	--	4.02	--	--	4.15	--	3.98	--	4.02	--	--	4.08	--	Vdc	--	--	15	14	--	--	16	--	--	--	13	8
Logic "0" Threshold Voltage	V_{OLA}	12	--	3.41	--	--	3.46	--	3.52	--	3.45	--	--	3.46	--	3.49	Vdc	--	--	15	14	--	--	16	--	--	--	12	8
		13	--	3.41	--	--	3.46	--	3.52	--	3.45	--	--	3.46	--	3.49	Vdc	--	--	14	15	--	--	16	--	--	--	13	8
Output Short-Circuit Current	I_{OS}	10	20	60	20	--	60	20	60	20	60	20	--	60	20	60	mAdc	15	14	--	--	--	11,16	--	--	--	--	--	8,9,10

*Devices will meet standard MECL logic levels using V_{EE} = -5.2 Vdc and V_{CC} = 0.

FIGURE 6 — AC CHARACTERISTICS — MECL AND TTL OUTPUTS





All input and output cables to the scope are equal lengths of 50 Ω coaxial cable.

Unused outputs are connected to a 50 Ω ±1% resistor to ground.

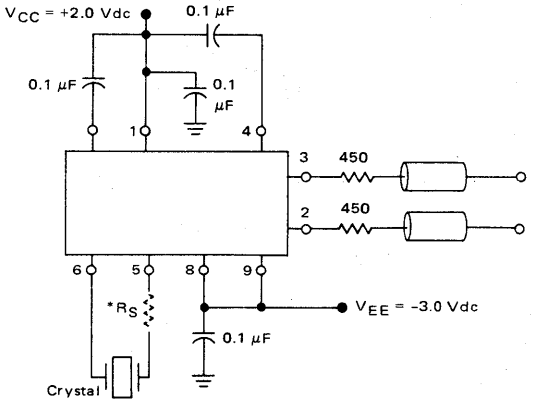
C_T = 15 pF = total parasitic capacitance which includes probe, wiring, and load capacitance.

Characteristic	Symbol	Pin Under Test	MC12561 -55°C Min	MC12561 -55°C Max	MC12561 +25°C Min	MC12561 +25°C Typ	MC12561 +25°C Max	MC12561 +125°C Min	MC12561 +125°C Max	MC12061 0°C Min	MC12061 0°C Max	MC12061 +25°C Min	MC12061 +25°C Typ	MC12061 +25°C Max	MC12061 +75°C Min	MC12061 +75°C Max	Unit	TEST VOLTAGES/WAVEFORMS APPLIED TO PINS LISTED BELOW: Pulse In	Pulse Out	+2.0 Vdc	-3.0 Vdc	Gnd
Propagation Delay	t_{15+10+}	10	–	30	–	17	25	–	30	–	22	–	17	25	–	27	ns	15	10	11,16	8,9	14
	t_{15-10-}	10	–	22	–	12	18	–	22	–	19	–	12	18	–	18			10			
	t_{15+12-}	12	–	5.0	–	4.3	5.5	–	6.0	–	5.2	–	4.3	5.5	–	5.8			12			
	t_{15-12+}	12	–	4.8	–	3.7	5.2	–	5.5	–	5.0	–	3.7	5.2	–	5.2			12			
	t_{15+13+}	13	–	4.6	–	4.0	5.0	–	5.4	–	4.8	–	4.0	5.0	–	5.2			13			
	t_{15-13-}	13	–	5.0	–	4.0	5.0	–	5.2	–	5.0	–	4.0	5.0	–	5.1			13			
Rise Time	t_{12+}	12	–	3.8	–	3.0	4.0	–	5.0	–	4.0	–	3.0	4.0	–	4.4	ns	15	12	11,16	8,9	14
	t_{13+}	13	–	3.8	–	3.0	4.0	–	5.0	–	4.0	–	3.0	4.0	–	4.4	ns	15	13	11,16	8,9	14
Fall Time	t_{12-}	12	–	3.8	–	3.0	4.0	–	4.5	–	4.0	–	3.0	4.0	–	4.0	ns	15	12	11,16	8,9	14
	t_{13-}	13	–	3.8	–	3.0	4.0	–	4.5	–	4.0	–	3.0	4.0	–	4.0	ns	15	13	11,16	8,9	14

FIGURE 7 — AC TEST CIRCUIT — SINE WAVE OUTPUT

Crystal — Reeves Hoffman Series
Mode, Series Resistance
Minimum at Fundamental
MC12061/12561:
f = 10 MHz
R_E = 5 Ω

*R_S is inserted only for test purposes. When used with the above specified crystal, it guarantees oscillation with any crystal which has an equivalent series resistance ≤ 155 Ω for MC12061/12561.



All output cables to the scope are equal lengths of 50 Ω coaxial cable. All unused cables must be terminated with a 50 Ω ±1% resistor to ground.

450 Ω resistor and the scope termination impedance constitute a 10:1 attenuator probe.

OPERATING CHARACTERISTICS

The MC12061/12561 consist of three basic sections: an oscillator with AGC and two translators (Figure 1). Buffered complementary sine wave outputs are available from the oscillator section. The translators convert these sine wave outputs to levels compatible with MECL and/or TTL.

Series mode crystals should be used with the oscillator. If it is necessary or desirable to adjust the crystal frequency, a reactive element can be inserted in series with the crystal — an inductor to lower the frequency or a capacitor to raise it. When such an adjustment is necessary, it is recommended that the crystal be specified slightly lower in frequency and a series trimmer capacitor be added to bring the oscillator back on frequency. As the oscillator frequency is changed from the natural resonance of the crystal, more and more dependence is placed on the external reactance, and temperature drift of the trimming components then affects overall oscillator performance.

The MC12061/12561 are designed to operate from a single supply — either +5.0 Vdc or −5.2 Vdc. Although each translator has separate V_{CC} and V_{EE} supply pins, the circuit is NOT designed to operate from both voltage levels at the same time. The separate V_{EE} pin from the TTL translator helps minimize transient disturbance. If neither translator is being used, all unused pins (9 thru 16) should be connected to V_{EE} (pin 8). With the translators not powered, supply current drain is typically reduced from 42 mA to 23 mA for the MC12061/12561.

Frequency Stability

Output frequency of different oscillator circuits (of a given device type number) will vary somewhat when used with a given test setup, however the variation should be within approximately ±0.001% from unit to unit.

Frequency variations with temperature (independent of the crystal, which is held at 25°C) are small — about −0.08 ppm/°C for MC12061/12561 operating at 8.0 MHz.

Signal Characteristics

The sine wave outputs at either pin 2 or pin 3 will typically range from 800 mVp-p (no load) to 500 mVp-p (120 ohm ac load). Approximately 500 mVp-p can be provided across 50 ohms by slightly increasing the dc current in the output buffer by the addition of an external resistor (680 ohms) from pin 2 or 3 to ground, as shown in Figure 9. Frequency drift is typically less than 0.0003% when going from a high-impedance load (1 megohm, 15 pF) to the 50-ohm load of Figure 9. The dc voltage level at pin 2 or 3 is nominally 3.5 Vdc with V_{CC} = +5.0 Vdc.

Harmonic distortion content in the sine wave outputs is crystal as well as circuit dependent. The largest harmonic (third) will usually be at least 15 dB down from the fundamental. The harmonic content is approximately load independent except that the higher harmonic levels (greater than the fifth) are increased when the MECL translator is being driven.

Typically, the MECL outputs (pins 12 and 13) will drive up to five gates, as defined in Figure 10, and the TTL output (pin 10) will drive up to ten gates, as defined in Figure 11.

Noise Characteristics

Noise level evaluation of the sine wave outputs using the circuit of Figure 12, with operation at 9.0 MHz, indicates the following characteristics:

1. Noise floor (200 kHz from oscillator center frequency) is approximately −122 dB when referenced to a 1.0 Hz bandwidth. Noise floor is not sensitive to load conditions and/or translator operation.
2. Close-in noise (100 Hz from oscillator center frequency) is approximately −88 dB when referenced to a 1.0 Hz bandwidth.

FIGURE 8 — FREQUENCY SHIFT VERSUS TEMPERATURE

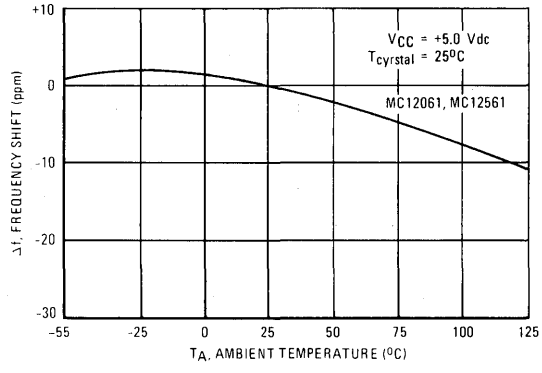
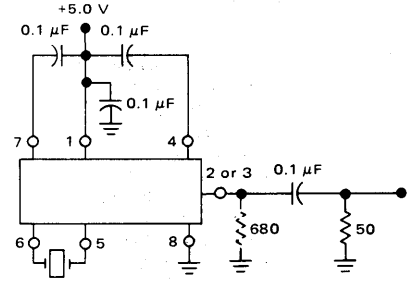


FIGURE 9 — DRIVING LOW-IMPEDANCE LOADS



*See text under signal characteristics.

FIGURE 10 — MECL TRANSLATOR LOAD CAPABILITY

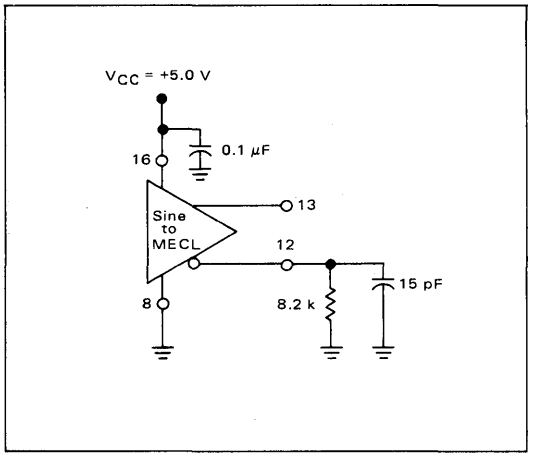


FIGURE 11 — TTL TRANSLATOR LOAD CAPABILITY

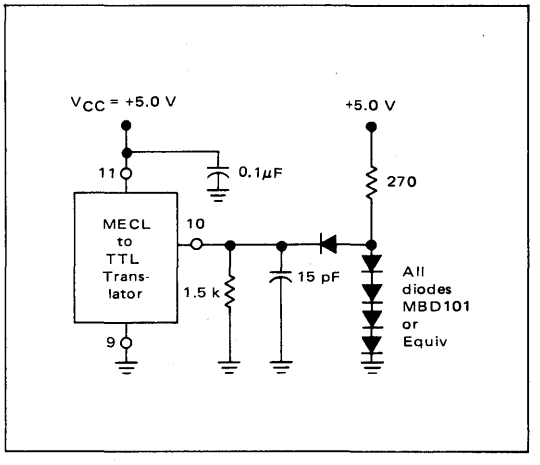
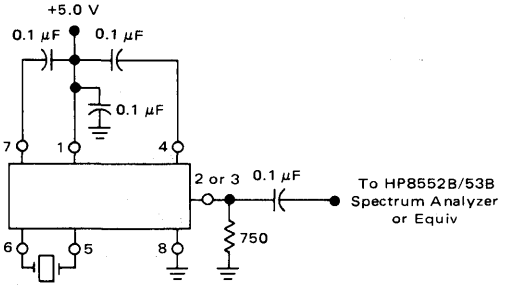


FIGURE 12 — NOISE MEASUREMENT TEST CIRCUIT

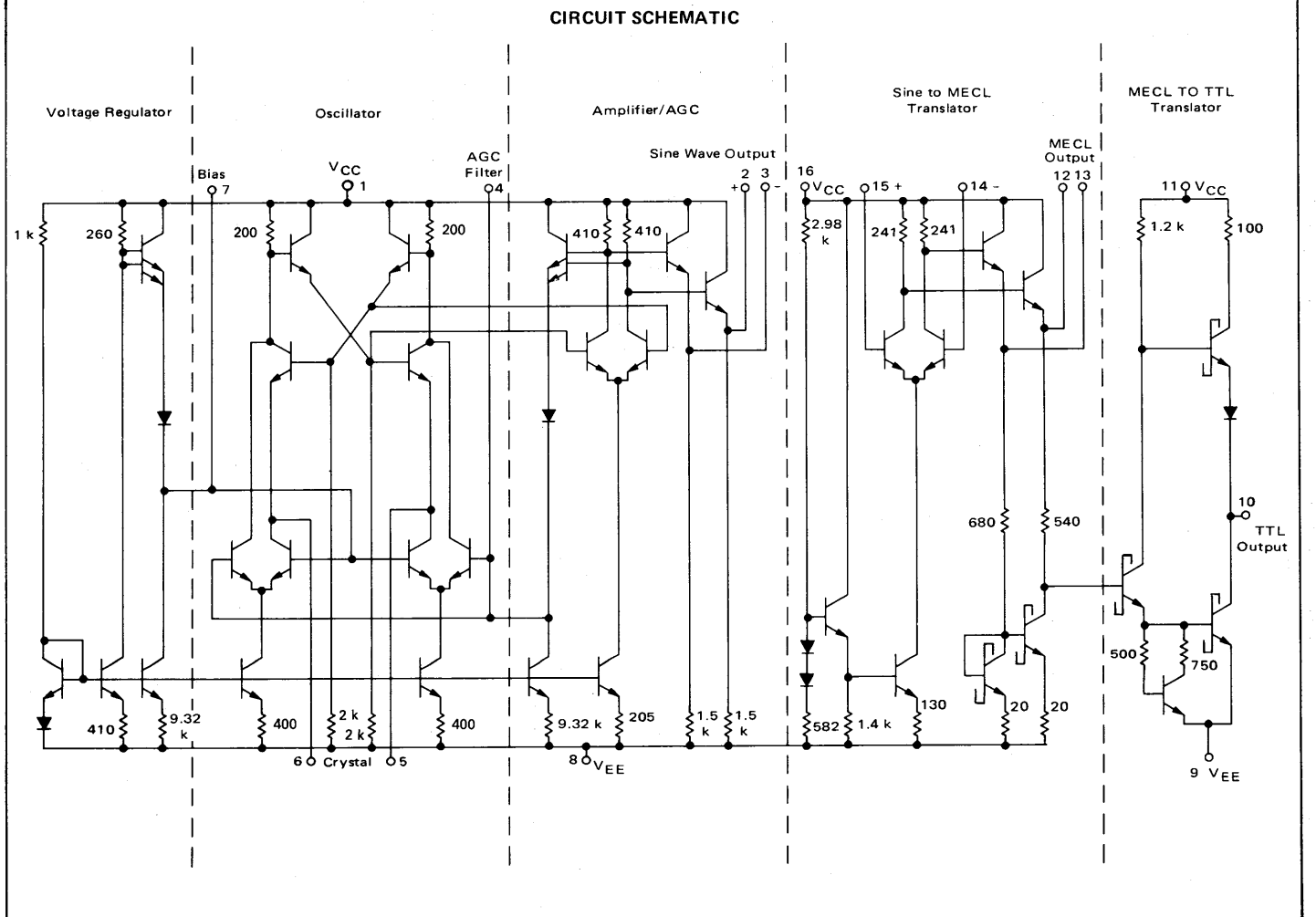


ANALYZER SETTING

Measurement	Sweep	Bandwidth	Video Filter
Noise Floor	50 kHz/div	10 kHz	10 Hz
Close-In Noise	20 kHz/div	10 Hz	10 Hz

7

CIRCUIT SCHEMATIC



MOTOROLA

MC12071

HIGH-SPEED PRESCALER

The MC12071 is a high-speed prescaler designed for use in communications and instrumentation systems. In the UHF mode, it performs division by 256, and divides by 64 in the VHF mode.

A bandswitch mode control line selects the mode of operation between the UHF and VHF input pins.

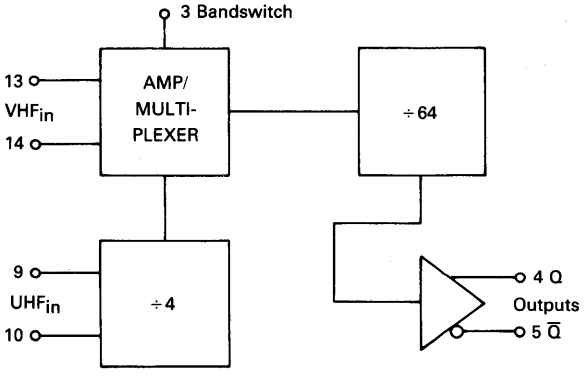
UHF operation is selected by applying a high-level (logical 1) to the bandswitch input. A low-level (logical 0) is applied to the bandswitch input to obtain the VHF mode. An internal amplifier/multiplexer is used to isolate both inputs, amplify the input signal, and improve sensitivity.

Inputs are designed for ac-coupled sine wave signals, but can be dc-coupled if proper bias levels are maintained. Normally used single-ended, the inputs can also be operated with complementary input signals if required.

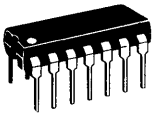
Circuit outputs are complementary emitter-follower type which can drive a 33-pF or equivalent load. Maintaining a balanced load and controlling rise and fall times will reduce harmonic outputs.

- Broadband Operation
- High Sensitivity
- Standard 5 Volt Power Supply
- VHF/UHF — Dual Mode Operation
- Complementary Emitter-Follower Outputs
- Independent VHF and UHF Input Pins

LOGIC DIAGRAM



HIGH-SPEED PRESCALER

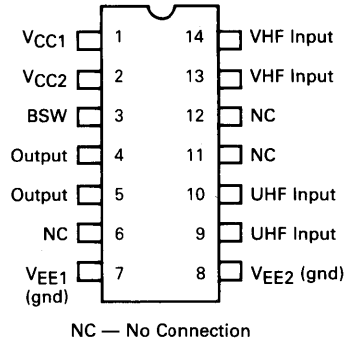


P SUFFIX
PLASTIC PACKAGE
CASE 646

TYPICAL APPLICATIONS

- CATV Converters
- Digital frequency synthesizers for:
  - VHF/UHF receivers
  - Instrumentation
  - Satellite communications
- High-frequency divider for:
  - Frequency counters (UHF)
  - Timers (UHF)
  - High-Speed computers
  - SHF, second IF local-oscillator injection
  - Frequency standards
  - PCM communications
  - Radar ranging systems
  - Satellite communications
- High-frequency up-converters

PIN ASSIGNMENT



NC — No Connection

7

MAXIMUM RATING

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	7.0	Vdc
Operating Power Supply Voltage	V_{CC}	5.0 ± 10%	Vdc
Bandswitch Voltage	V_{BH}	20	Vdc
Input Voltage	V_{in}	0.5	V_{RMS}
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C
Junction Temperature	T_J	150	°C

Ratings above which devjce life may be impaired.

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 0°C to +70°C)

Characteristics	Symbol	Min	Typ	Max	Unit
STATIC					
Supply Current (Pins 1 & 2)	I_{CC}	30	60	90	mA
Bandswitch Voltage, Low	V_{BL}	0	–	0.8	Vdc
High	V_{BH}	2.4	–	20	
Bandswitch current 0 to 0.8 V	I_{BL}	−0.5	–	–	mA
2.4 to 20 V	I_{BH}	–	–	0.5	
Output Voltage, High	V_{OH}		4.2		Vdc
Output Voltage, Low	V_{OL}		3.0		Vdc
DYNAMIC (See Fig. 2)					
UHF Input Sensitivity Range (See note)	UHF_{in}				mV_{RMS}
f_{in} = 450 to 950 MHz, V_{BH}		60	–	*200	
f_{in} = 80 to 450 MHz, V_{BH}		150	–	500	
VHF Input Sensitivity Range (See note)	VHF_{in}	40	–	500	mV_{RMS}
f_{in} = 90 to 275 MHz, V_{BL}					
Output Voltage	V_{out}	0.65	1.2	1.6	Vp-p
Output Rise or Fall Time	t_r, t_f	40	70	110	nS

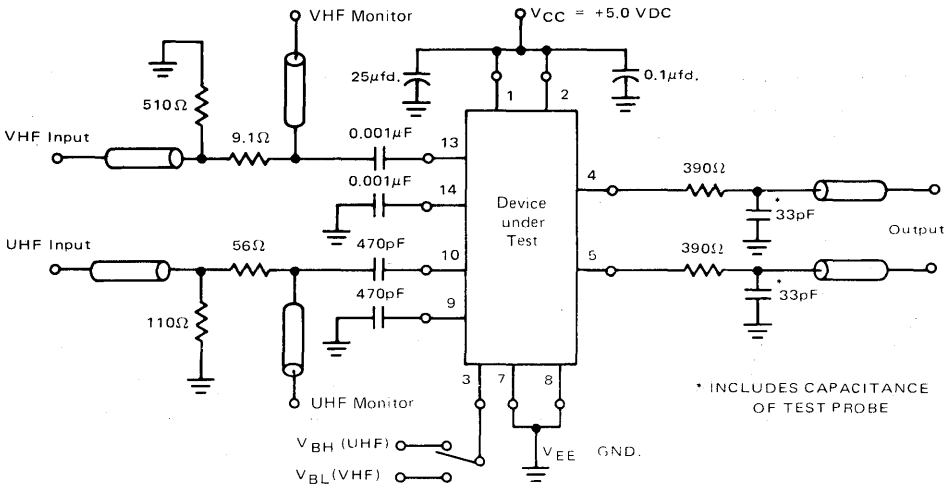
NOTE:

UHF input sensitivity as measured in test fixture shown in Figure 2. Devices may overload if the input signal exceeds the maximum level specified.

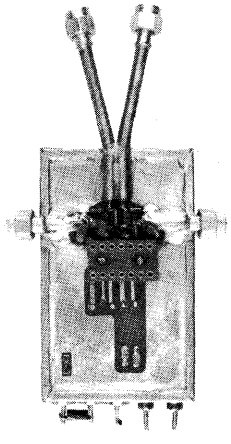
* Overload levels are very layout sensitive and will probably require correlation in customer circuits. Overload levels of 500 mVRMS can easily be attained with various layouts.

7

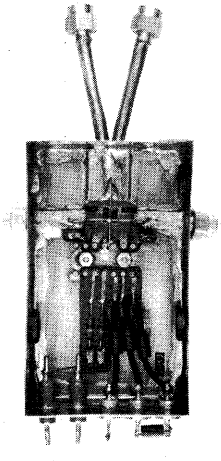
FIGURE 2 — AC TEST CIRCUIT



STANDARD TEST FIXTURE



TOP



BOTTOM

TEST FIXTURE CONSIDERATIONS

Pictured above is our standard MC12071 test fixture. High-frequency construction and design techniques are a must if the operation of the test fixture is to be stable and repeatable. Listed below are some considerations which must be observed to insure proper operation of the test circuit.

- Use a good ground plane with frequent ground connections.
- Use best available high-frequency type socket.
- Maintain a 50Ω environment on inputs except where it is necessary for the signal to pass through a component.
- Use best available high-frequency components and keep lead length to an absolute minimum. (Chip type ceramic capacitors are preferable.)
- Pin bypasses should be placed as close to the device as possible.

Note: Even after implementing the above fixture design and construction techniques some minimal correlation differences may exist due to inherent high-frequency characteristics variations.

7

FIGURE 3 — TYPICAL UHF INPUT SENSITIVITY

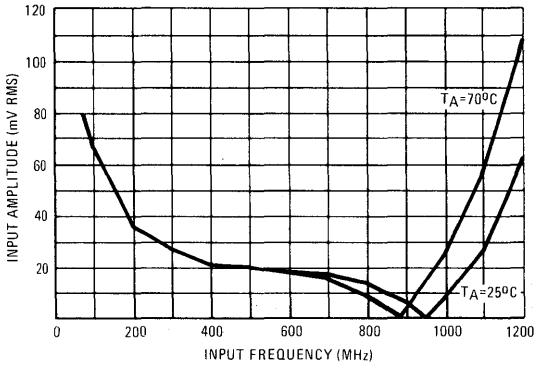


FIGURE 4 — TYPICAL VHF INPUT SENSITIVITY

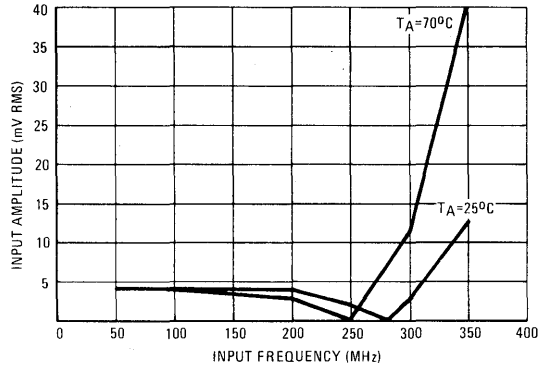
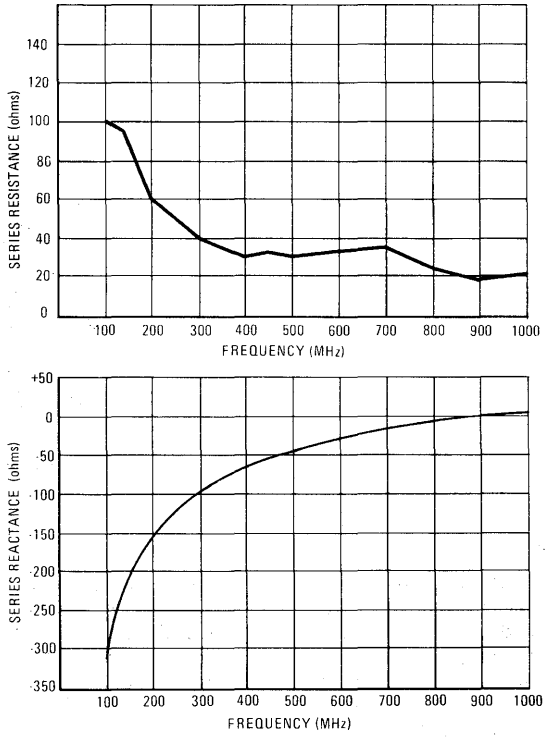


FIGURE 5 — TYPICAL INPUT IMPEDANCE



7

MOTOROLA

MC12073

Product Preview

÷64 LOW-POWER PRESCALER

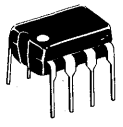
The MC12073 is a new member of Motorola's PLL family. It is a high-speed, low-power prescaler which divides by 64. The MC12073 can be used in all frequency synthesis applications. Typical applications include electronically tuned TV/CATV and communication systems as well as instrumentation.

An internal preamplifier is included in the MC12073. This preamplifier isolates the differential inputs and provides gain for the input signal. The MC12073 is pin compatible with Plessey's SP4632 and has differential outputs.

- 1.1 GHz Toggle Frequency
- Low-Power: 25 mA Typical @ V_{CC} = 5.0 V
- High Input Sensitivity
- 800 mV Minimum Peak-Peak Output Swing
- This Product Preview's Specifications are Design Goals Only

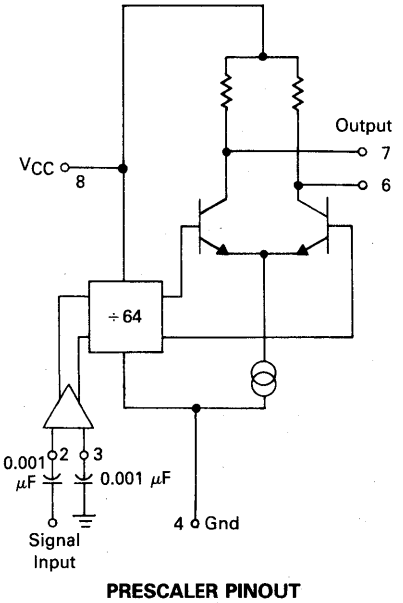
MECL PLL COMPONENTS

LOW-POWER PRESCALER ÷64



P SUFFIX
PLASTIC PACKAGE
CASE 626

PRESCALER BLOCK DIAGRAM



MAXIMUM RATINGS

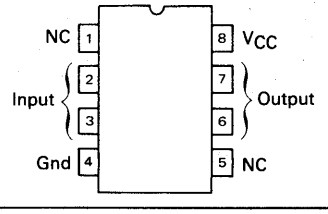
Characteristic	Symbol	Range	Unit
Power Supply Voltage	V_{CC}	7.0	Vdc
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +175	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 4.5 to 5.5 V, T_A = 0°C to +70°C)

Characteristic	Symbol	Min	Typ	Max	Unit
Toggle Frequency (Sine wave input)	f_{max}	1.1	—	—	GHz
Supply Current	I_{CC}	—	25	—	mA
Output Voltage (Load = 10 pF, I_{sink} = 200 μA)	V_{out}	0.8	1.0	—	V_{pp}
Input Voltage Sensitivity	V_{in} Min	—	10	—	mV_{rms}
Input Overload	V_{in} Max	200	—	—	mV_{rms}
AC Input Resistance	R_{in}	—	TBD*	—	kΩ
Input Capacitance	C_{in}	—	TBD*	—	pF

*To be determined.

PRESCALER PINOUT



This document contains information on a new product. Specifications and information herein are subject to change without notice.

MOTOROLA

MC12074

Product Preview

÷256 LOW-POWER PRESCALER

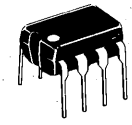
The MC12074 is a new member of Motorola's PLL family. It is a high-speed, low-power prescaler which divides by 256. The MC12074 can be used in all frequency synthesis applications. Typical applications include electronically tuned TV/CATV and communication systems as well as instrumentation.

An internal preamplifier is included in the MC12074. This preamplifier isolates the differential inputs and provides gain for the input signal. The MC12074 is pin compatible with Plessey's SP4653 and has differential outputs.

- 1.1 GHz Toggle Frequency
- Low-Power: 25 mA Typical @ V_{CC} = 5.0 V
- High Input Sensitivity
- 800 mV Minimum Peak-Peak Output Swing
- This Product Preview's Specifications are Design Goals Only

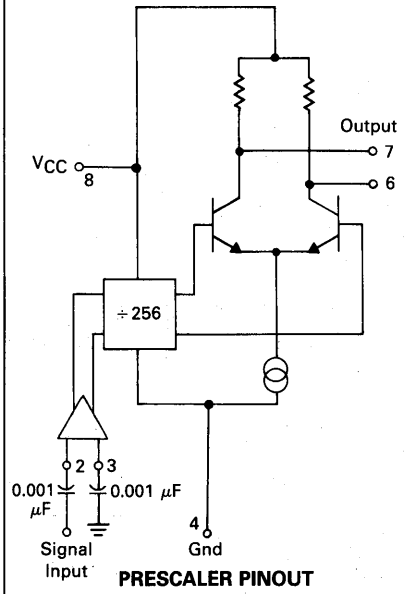
MECL PLL COMPONENTS

LOW-POWER PRESCALER ÷256

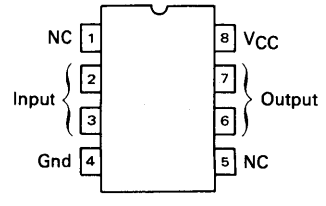


P SUFFIX
PLASTIC PACKAGE
CASE 626

PRESCALER BLOCK DIAGRAM



PRESCALER PINOUT



MAXIMUM RATINGS

Characteristic	Symbol	Range	Unit
Power Supply Voltage	V_{CC}	7.0	Vdc
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +175	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 4.5 to 5.5 V, T_A = 0°C to +70°C)

Characteristic	Symbol	Min	Typ	Max	Unit
Toggle Frequency (Sine wave input)	f_{max}	1.1	—	—	GHz
Supply Current	I_{CC}	—	25	—	mA
Output Voltage (Load = 10 pF, I_{sink} = 200 μA)	V_{out}	0.8	1.0	—	V_{pp}
Input Voltage Sensitivity	V_{in} Min	—	10	—	mV_{rms}
Input Overload	V_{in} Max	200	—	—	mV_{rms}
AC Input Resistance	R_{in}	—	TBD*	—	kΩ
Input Capacitance	C_{in}	—	TBD*	—	pF

*To be determined.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

7

MOTOROLA

MC12090

Advance Information

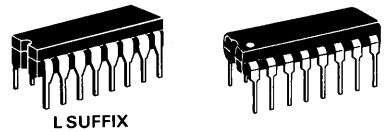
UHF PRESCALER

The MC12090 is a high-speed D master-slave flip-flop capable of toggle rates of over 700 MHz. It was designed primarily for high-speed prescaling applications in communications and instrumentation. This device employs two data inputs, two clock inputs as well as complementary Q and $\overline{Q}$ outputs. There are no SET or RESET inputs.

PLL COMPONENTS

HIGH-SPEED PRESCALER

P SUFFIX
PLASTIC PACKAGE
CASE 648



L SUFFIX
CERAMIC PACKAGE
CASE 620

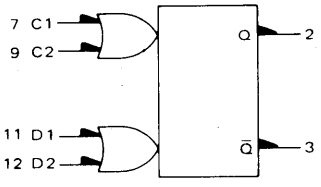
ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	0° Min	0° Max	25° Min	25° Max	75° Min	75° Max	Unit
Power Supply Current	I_E	—	65	—	59	—	65	mA
Input Current High Pin 7, 9 Pin 11, 12	I_{inH}	 — —	 400 435	 — —	 260 280	 — —	 260 280	μA
Input Current Low	I_{inL}	0.5	—	0.5	—	0.3	—	μA
High Output Voltage	V_{OH}	-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
Low Output Voltage	V_{OL}	-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
High Input Voltage	V_{IH}	-1.17	-0.84	-1.13	-0.81	-1.70	-0.735	Vdc
Low Input Voltage	V_{IL}	-1.87	-1.495	-1.85	-1.48	-1.83	-1.45	Vdc

AC PARAMETERS

Characteristic	Symbol	0°C Min	0°C Max	25°C Min	25°C Max	75°C Min	75°C Max	Unit
Toggle Frequency	f_{tog}	700	—	750	—	700	—	MHz
				Typical (25°C)				
Propagation Delay (Clock to Output Pins 7 & 9→2)	t_{pd}			1.3				ns
Setup Time $t_{setup\ H}$ $t_{setup\ L}$	t_s			 0.3 0.3				ns
Hold Time $t_{hold\ H}$ $t_{hold\ L}$	t_h			 0.2 0.3				ns
Rise Time	t_r			0.9				ns
Fall Time	t_f			0.9				ns

LOGIC DIAGRAM



V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

TRUTH TABLE

C	D	Q_{n+1}
L	ϕ	Q_n
H	ϕ	Q_n
⎍	L	L
⎍	H	H

C = C1 + C2 ϕ = Don't Care
D = D1 + D2

7

This document contains information on a new product. Specifications and information herein are subject to change without notice

FIGURE 1 — GUARANTEED RANGE OF OPERATION
(TEMP = 75°C, # DEVICES = FIVE;
V_{CC} = 2.0 V, V_{EE} = -3.2 V, V_{BIAS} = 0.710 V)

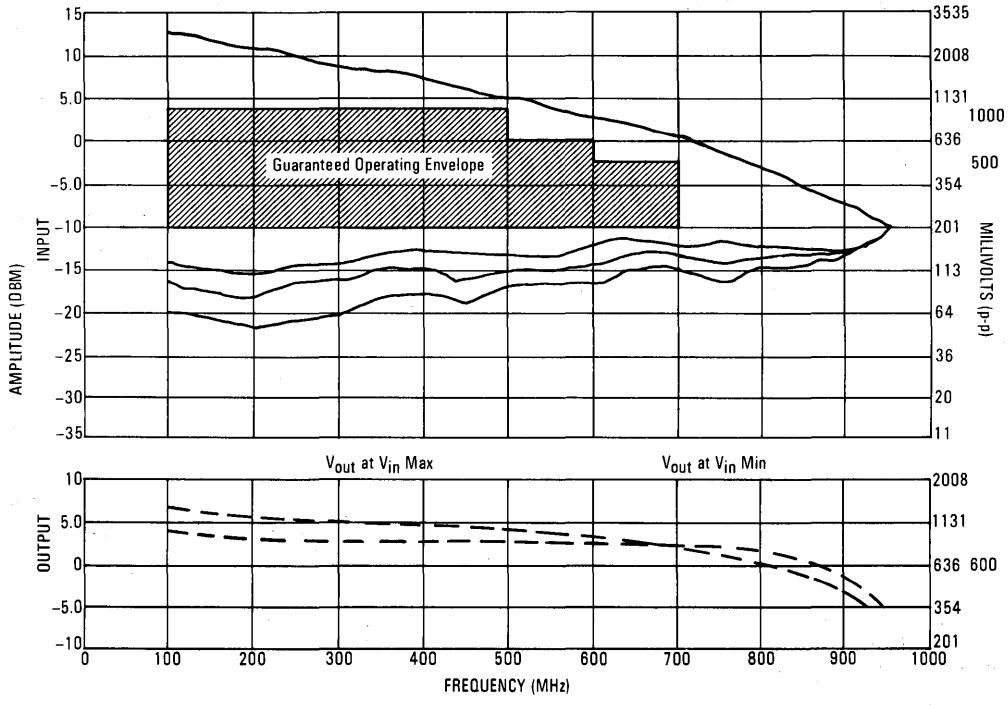
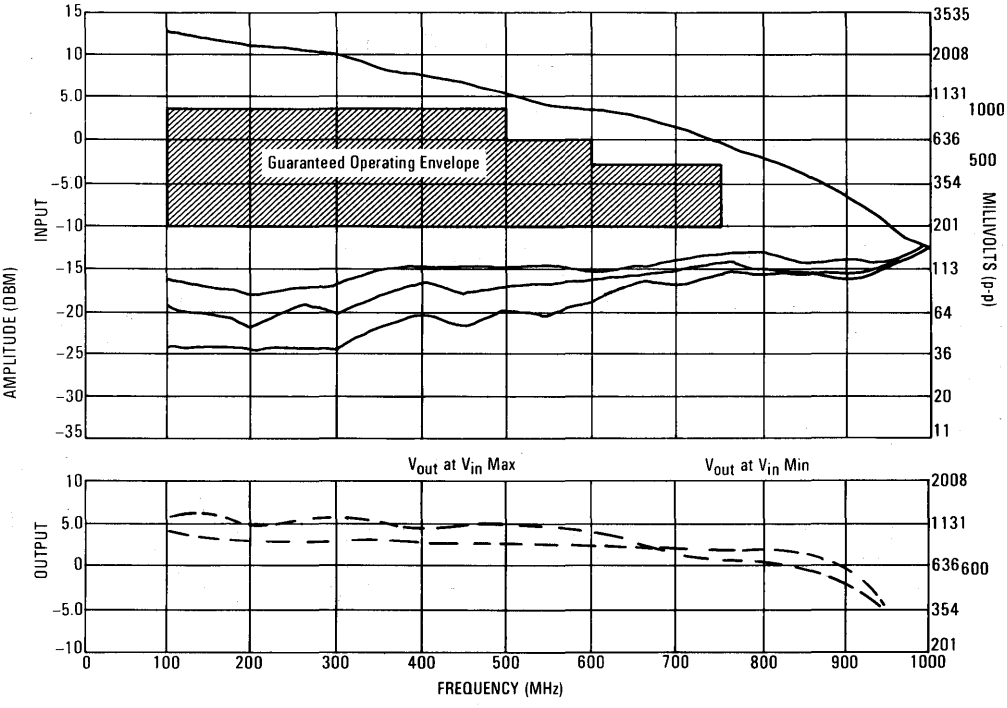


FIGURE 2 — GUARANTEED RANGE OF OPERATION
(TEMP = 25°C, # DEVICES = FIVE;
V_{CC} = 2.0 V, V_{EE} = -3.2 V, V_{BIAS} = 0.710 V)



7


MECL
QUALITY
AND
RELIABILITY

THE "BETTER" PROGRAM

Motorola's reliability enhancement program was developed to provide improved levels of reliability for standard commercial products.

The "BETTER" program is offered on ECL, in dual-in-line ceramic and plastic packages.

Motorola standard commercial integrated circuits are manufactured under stringent in-process controls and quality inspections combined with the industries' finest outgoing quality inspections. The "BETTER" program offers three levels of extra processing, each tailored to meet different user needs at nominal costs.

The program is designed to:

- Reduces incoming electrical inspection
- Eliminate need for independent test labs and associated extra time and costs
- Reduce field failures
- Reduce service calls
- Reduce equipment downtime
- Reduce board and system rework
- Reduce infant mortality
- Save time and money
- Increase end-customer satisfaction

BETTER PROCESSING — STANDARD PRODUCT PLUS:

LEVEL I (Suffix S)

- 100% temperature cycling per MIL-STD-883. Method 1010, ten cycles from −25°C to +150°C.
- 100% functional and dc parametric tests at maximum rated temperature.

LEVEL II (Suffix D)

- 100% burn-in to MIL-STD-883 test conditions — 160 hours at +125°C or 1.0 eV Arrhenius time/temperature equivalent.
- 100% post burn-in functional and dc parametric tests at 25°C (or max rated T_A at Motorola's option). Maximum PDA of 2% (functional) and 5% (DC and functional).

LEVEL III (Suffix DS)

- Combination of Levels I and II above.

"MOTOROLA" AQL GUARANTEES

TEST	CONDITION	AQL[1]		
		LEVEL I	LEVEL II	LEVEL III
HIGH TEMPERATURE FUNCTIONAL	T_A = MAX	0.05	0.05	0.05
DC PARAMETRIC	T_A = 25°C	0.05	0.05	0.05
DC PARAMETRIC	T_A MIN, T_A MAX	0.25	0.25	0.25
AC PARAMETRIC	T_A = 25°C	0.05	0.05	0.05
EXTERNAL VISUAL AND MECHANICAL	MAJOR/MINOR	0.05	0.05	0.05
HERMETICITY (NOT APPLICABLE TO PLASTIC PACKAGES)	GROSS/FINE	0.15	0.15	0.15

1. "AQL" values shown are for reference only—"LTPD" type sampling plans are used that are equal to or tighter than values indicated. Also, the guaranteed electrical and visual/mechanical AQL levels will be progressively tightened. Contact Motorola sales office for latest values.

HOW TO ORDER

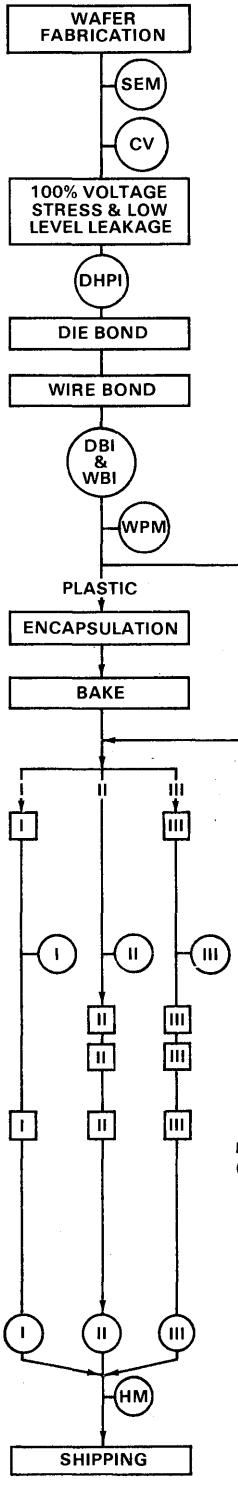
MC10101	P	S
Part Identification	Standard Package Suffix	BETTER PROCESSING LEVEL I = SUFFIX S LEVEL II = SUFFIX D LEVEL III = SUFFIX DS

PART MARKING

The Standard Motorola part number with the corresponding "BETTER" suffix can be ordered from your local authorized Motorola distributor or Motorola sales offices. "BETTER" pricing will be quoted as an adder to standard commercial product price.

8

GENERALIZED "BETTER" PRODUCT FLOW FOR MECL



Scanning Electron Microscope Wafer Process Control Monitor. To control oxide step profiles, contact coverage, and metallization integrity. (Engineering option.)

CV Plot Wafer Process Control Monitor: To control field inversion potential, base inversion — surface channel formation, and to detect any spurious contamination problems. (Engineering option.)

Performed at final wafer probe (or, optionally, at final electrical test) to screen out potential pinhole shorts, interlayer metal shorts, N+ crossunder shorts, diffusion faults, and similar defects that cannot be detected by visual die high-power inspection.

Die High-Power Sample Gate Inspection: Performed by in-process Q.A. to an 5.5% AQL to detect any damage caused by 100% wafer probe or mechanical scribe and break operation, or any scratches, metallization smears, or glass on bonding pads.

Combined Die Bond and Wire Bond Sample Gate Inspection: Performed by in-process Q.A. to 0.65% AQL to detect any misaligned or lifted die, to assure adequate "wetting" for low thermal resistance and high die shear strength, and to detect any improper wire bonds or wire dress, and any wire bonder damage.

Wire Pull Monitor: Performed by in-process Q.A. to maintain process control of bond strength values per MIL-STD-883. Method 2011, Condition D.

Motorola Proprietary Epoxy Molding Compound: Meets or exceeds U.L. flame-retarding level UL94V-1.

Post Encapsulation Bake: Eight hours at 150°C (or six hours at 175°C). Final cure for molding compound; also stresses wire and die bonds and helps eliminate marginal devices.

100% Temperature Cycling: MIL-STD-883, Method 1010, ten cycles −25°C to +150°C. Exercising circuits ten times over a 175°C range stresses the die and wire bonds and generally eliminates any marginal bonds and also screens out some types of wafer defects (pinholes, interlayer metal shorts, marginal step coverage, N+ crossunder shorts) and marginal seals in hermetic packages. This screening is superior to thermal shock screening because it does not introduce latent failures in ceramic packages (microcracks in seals) or in plastic packages (entrapped liquid) that can result from liquid-to-liquid thermal shock.

Hermeticity Monitor: Hermetic packages only — combination fine/gross leak test per modification of MIL-STD-883, Method 1014B. (5×10^{-8} ATM CC/SEC to 1×10^{-4} ATM CC/SEC). Sampled to a 0.25% AQL.

100% Electrical: Functional and dc parametrics at 25°C or max rated T_A (optional).

100% Burn-In: MIL-STD-883, Method 1015, for 160 hours minimum at T_A of 125°C minimum (or equivalent, per Arrhenius equation with 1.0eV activation energy). Test condition depends on device type, but generally condition A or C.

100% Electrical: Level I and III Functional tests at max rated T_A. Level II Functional and all DC parametrics at 25°C or max rated T_A at Motorola's option. Maximum PDA of 2% (Functional) and 5% (DC and Functional).

100% High-Temperature Functional Tests: Devices are tested at maximum rated operating temperatures assuring reliable operation at elevated temperatures and screening out marginally performing devices that could otherwise lower field reliability. Although epoxy molding compounds have essentially eliminated the thermal intermittent failure mode, this screen provides protection from any "maverick" intermittent device being shipped to a customer. This screening is more effective than hot rail "continuity" testing because non-functional devices can often pass a continuity test.

Q.A. Electrical and Mechanical Final Acceptance Tests: Sampled to the AQL levels of Table 1.

Hermeticity Monitor: Hermetic packages only. Combination fine/gross leak test per modification of MIL-STD-883, Method 1014B (5×10^{-8} ATM CC/SEC to 1×10^{-4} ATM CC/SEC). Sampled to a 0.15% AQL.

"RAP"
RELIABILITY AUDIT PROGRAM
for
BIPOLAR DIGITAL
INTEGRATED CIRCUITS

1.0 INTRODUCTION

In January, 1977, Motorola Bipolar Digital Reliability Engineering implemented "RRAP" (Rapid Reliability Assessment Program) to provide rapid assessment of the reliability of newly introduced TTL Low-Power Schottky (LS) devices. This RRAP concept permits rapid feedback of information on any reliability problems to the Product Engineering group so that corrective action can be quickly implemented. The RRAP program is performed by the Reliability Engineering Department on samples submitted by Product, Process, or Package Engineering for obtaining a rapid look at the reliability of new products, processes, or packages. This program has now been extended to standard ALS, TTL, TTL Memories, MDTL, MHTL, MECL III, MECL 10K and 10KH, MECL Memories, Macrocell Arrays, and Phase Lock Loop (PLL) product families. The details of the RRAP program are outlined in Section 2.0.

In March, 1977, an addition was made to the RRAP program for the purpose of auditing the reliability of outgoing product. This audit, called the Reliability Audit Program ("RAP"), is performed weekly by the Quality Assurance Group and reported monthly by Bipolar Digital Reliability Engineering. The details of this "RAP" program are outlined in Section 3.0.

2.0 RAPID RELIABILITY ASSESSMENT PROGRAM (RRAP)

2.1 Hermetic Packaged Devices (50 Units minimum per Evaluation Sample)

a. Electrical I (initial rejects removed from test)
b. Temp Cycling −100 cycles (−65°C/+150°C) per Method 1010C
c. Electrical I (plus Hermeticity per Method 1014 B & C for package evaluations only)
d. "Equivalent" Burn-In for 40 hrs at 145°C per Method 1015 A or C
e. Electrical I

2.2 Plastic Packaged Devices (100 Units minimum per Evaluation Sample)

S/G 1 (30 Units)

a. Electrical I
b. Thermal Shock −200 cycles (−55°C/+125°C −30 Sec. dwell) Method 1011B, modified
c. Electrical I

S/G 2 (40 Units)

a. Electrical I
b. **16 hrs, PTHB; Rated V_{CC} or V_{EE} (15 psig, 100% RH, 121°C) Motorola test method**
c. Electrical I

S/G 3 (30 Units)

a. Electrical I
b. Temp Cycling −100 cycles (−65°C/+150°C). Method 1010C
c. Electrical I
d. "Equivalent" Burn-In (40 hrs @ 145°C) per Method 1015 A or C
e. Electrical I

NOTES:

1. All tests per MIL-STD-883 unless stated otherwise.
2. Electrical I = DC @ 25°C and functional @ 25°C — Go/No/Go
3. 40 hr/145°C burn-in is "equivalent" to 160 hr/125°C burn-in using 1.0 eV activation energy and the Arrhenius equation for determining acceleration factor.
4. 16 hrs of PTHB testing is equivalent to approximately 800 hrs of standard 85°C/85% RH THB testing for $V_{CC} \leqslant 15$ V, based on comparative tests performed by Motorola Reliability Engineering.
5. For each evaluation, the goal is zero failures. Any indicated failure is first verified and then submitted to the Product Analysis Lab for detailed analysis. Results of evaluation, along with analysis of any failure(s), are reviewed promptly with responsible design, product, process and package engineers.

3.0 RELIABILITY AUDIT PROGRAM (RAP)
(per Motorola specification 12 MRM15301A)

3.1 PTHB — 15 psig/121°C/100% RH at rated V_{CC} or V_{EE} for 16 hours — performed on a weekly basis — 0 rejects allowed out of 45 devices. (To be performed on plastic encapsulated devices only.) 48 hour read out also included for reliability engineering information only.

3.2 Temp Cycling — MIL-STD-833, Method 1010, 1000 cycles, Condition C, −65°C/+150°C. Interim readout at 100 cycles (plastic and hermetic packages). Sample pulled on weekly basis — 0 rejects allowed out of 45 devices after 100 cycles; 1 reject allowed out of 45 devices after 1000 cycles.

3.3 Op. Life Test — MIL-STD-883, Method 1005, Condition A (Reverse Bias) or C (Power plus Reverse Bias), T_A = 145°C; readouts at 40 hrs and 250 hrs (plastic and hermetic packages). Sample pulled on weekly basis — 1 reject allowed out of 55 devices at 40 hr readout. No additional rejects allowed at 250 hrs. If no rejects at 40 hrs, 1 reject allowed at 250 hrs.

3.4 Report — Monthly Reliability Engineering computer printout summarizing test results.

NOTES:
1. All standard 25°C dc and functional parameters will be measured Go/No/Go at each readout.
2. Any indicated failure is first verified and then submitted to the Product Analysis Lab for detailed analysis.
3. If both plastic and hermetic packages are available, package type will be alternated weekly. Hermetic packages will include both cerdip CERDIP and LCC types.
4. Device types sampled will be by generic type within each digital I/C product family (MDTL, MECL, TTL-LS, etc.) and will include all major package assembly options (U/S bond, ball bond, etc.) and all assembly locations (Korea, Philippines, Malaysia, etc.).
5. 16 hrs PTHB is equivalent to approximately 800 hrs of 85°C/85% RH THB for $V_{CC} \leqslant$ 15 V.
6. Only moisture related failures (like corrosion) are criteria for failure on PTHB test.
7. 40 hr/145°C Op Life is equivalent to 160 hr/125°C using 1.0 eV in Arrhenius equation.
8. 250 hrs/145°C Op Life is equivalent to 1000 hrs/125°C using 1.0 eV in Arrhenius equation.
9. Special device specifications (48A's) for digital products will reference 12MRM15301A as source of generic data for any customer required monthly audit reports.

STANDARD PROGRAMS

MIL-STD-883 OPERATIONS METHOD	PROCESSING PER 5004/5005	HI-REL JEDEC PROCESSED PROGRAMS		MIL-M-38510 JAN QUALIFIED
SCREEN	CLASS B METHOD	CLASS B	CLASS C	CLASS B
Internal Visual (Precap)	2010 Condition B and 38510	100%	100%	100%
Stabilization Bake	1008 Condition C or Equivalent	100%	100%	100%
Temperature Cycling	1010 Condition C	100%	100%	100%
Constant Acceleration	2001 Condition E (min.) Y_1 Plane	100%	100%	100%
Seal (a) Fine (b) Gross	1014, Condition B 1014, Condition C	100% 100%	100% 100%	100% 100%
Interim Electrical Parameters	Per applicable device specification	Optional[1]		Optional[1]
Burn-in Test	1015 160 Hrs. @ 125° C Min. (4)	100%		100%
Final Electrical Tests (a) Static tests (1) 25°C (subgroup 1, table 1, 5005) (2) Max. and min. rated operating temp. (subgroups 2 and 3, table 1, 5005) (b) Dynamic tests and/or switching tests @ 25°C (subgroup 4 and 9, table 1, 5005) (c) Functional test @ 25°C (subgroup 7, table 1, 5005)	Per applicable device specification	 100% 100%[5] 100% 100%	 100% (2) (2) 100%	 100% 100%[5] 100% 100%
Qualification or Quality Conformance Inspection	5005	Group A[3]	Group A[3]	per 38510[3]
External Visual	2009	100%	100%	100%

1. When specified in the applicable device specification, 100% of the devices shall be tested at Manufacturer's option.
2. Sample at Group A.
3. Full 5005 Conformance testing performed on Jan qualified product. Group A performed on Motorola HI-REL JEDEC processed product with either Generic or group B, C, D testing available.
4. Optional 0.44 eV time-temperature "equivalent" burn-in per Figure 1015-1.
5. AC sample testing at +125°C and −55°C on those types which require subgroup 10 and 11 testing per MIL-M-38510 Slash Sheet Specifications.

JEDEC Processed Product

Screening Levels Available:
Class B & Class C

How to order
JEDEC
Processed Product*

XXXXX/	Y	Y	Y	JC
MOTOROLA DEVICE TYPE (WITHOUT LETTER PREFIX)	CLASS B, OR C (SEE DEVICE CLASS TABLE)	CASE OUTLINE (SEE CASE OUTLINE TABLE)	LEAD FINISH (SEE LEAD FINISH TABLE)	JEDEC DESIGNATOR PER JEDEC PUBLICATION NO. 101

Case Outline Table
Source: MIL-M-38510D Amendment I

Letter	Appendix C Designation	Description
A	F-1	14-lead FP (1/4" x 1/4")
B	F-3	14-lead FP (3/16" x 1/4")
C	D-1	14-lead DIP (1/4" x 3/4")
D	F-2	14-lead FP (1/4" x 3/8")
E	D-2	16-lead DIP (1/4" x 7/8")
F	F-5	16-lead FP (1/4" x 3/8")
G	A-1	8-lead can
H	F-4	10-lead FP (1/4" x 1/4")
I	A-2	10-lead can
J	D-3	24-lead DIP (1/4" x 1 1/4")
K	F-6	24-lead FP (3/8" x 5/8")
L	NONE	NONE
M	A-3	12-lead can
N	NONE	NONE
P	D-4	8-lead DIP (1/4" x 3/8")
Q	D-5	40-lead DIP (9/16" x 2 1/16")
R	D-8	20-lead DIP (1/4" x 1 1/16")
S	F-9	20-lead FP (1/4" x 1/2")
T	NONE	NONE
U	C-2	20 terminal leadless chip carrier
V	D-6	18-lead DIP (0.300" x 1")
W	D-7	22-lead DIP (0.400" x 1.1")
X	Dual-in-line packages not listed above	
Y	Flat packages not listed above	
Z	All other configurations not listed above. Note: When ordering Z Case outline, Motorola case number and/or package classification (TO-3, TO-39, TO-66, etc.) must be referenced.	

Features:

1. Lower cost than JAN-Qualified.
2. Devices manufactured using design and processing guidelines contained in MIL-M-38510 and MIL-STD-883
3. Product supplied with Motorola standard data sheet electricals

Example of JEDEC
Processed Markings

MARKING: 10501/BEBJC

Lead Finish Table
A — Type A or B Per MIL-M-38510 with hot solder dip
B — Type A or B Per MIL-M-38510 with tin plate
C — Type A or B Per MIL-M-38510 with gold plate
X — Any of the above, for ordering purposes only.

*MECL 10500 series is available in JEDEC

MIL-M-38510 JAN-Qualified Product

Screening Levels Available:
Class B & Class C

How to order
MIL-M-38510
JAN-Qualified Product

J	M38510	/XXX	XX	Y	Y	Y
INDICATES A QUALIFIED DEVICE	MILITARY DESIGNATOR	DETAIL SPECIFICATION NUMBER	DEVICE TYPE WITHIN DETAIL SPECIFICATION	CLASS B, OR C (SEE DEVICE CLASS TABLE)	CASE OUTLINE (SEE CASE OUTLINE TABLE)	LEAD FINISH (SEE LEAD FINISH TABLE)

Case Outline Table
Source: MIL-M-38510D Amendment I

Letter	Appendix C Designation	Description
A	F-1	14-lead FP (1/4" x 1/4")
B	F-3	14-lead FP (3/16" x 1/4")
C	D-1	14-lead DIP (1/4" x 3/4")
D	F-2	14-lead FP (1/4" x 3/8")
E	D-2	16-lead DIP (1/4" x 7/8")
F	F-5	16-lead FP (1/4" x 3/8")
G	A-1	8-lead can
H	F-4	10-lead FP (1/4" x 1/4")
I	A-2	10-lead can
J	D-3	24-lead DIP (1/4" x 1 1/4")
K	F-6	24-lead FP (3/8" x 5/8")
L	NONE	NONE
M	A-3	12-lead can
N	NONE	NONE
P	D-4	8-lead DIP (1/4" x 3/8")
Q	D-5	40-lead DIP (9/16" x 2 1/16")
R	D-8	20-lead DIP (1/4" x 1 1/16")
S	F-9	20-lead FP (1/4" x 1/2")
T	NONE	NONE
U	C-2	20 terminal leadless chip carrier
V	D-6	18-lead DIP (0.300" x 1")
W	D-7	22-lead DIP (0.400" x 1.1")
X Y Z	Reserved for use with "special" non-standard case outlines which are specified in the individual detail specifications.	

Features:

1. Manufactured in a government-approved facility.
2. G.S.I. (Government Source Inspection)

Example of MIL-M-38510 JAN-Qualified markings

ORDER: JM38510/00104BCB
MARKING: JM38510/00104BCB

Lead Finish Table
A — Type A or B Per MIL-M-38510 with hot solder dip
B — Type A or B Per MIL-M-38510 with tin plate
C — Type A or B Per MIL-M-38510 with gold plate
X — Any of the above, for ordering purposes only

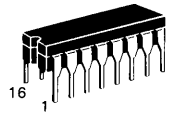
JAN Qualified MECL Devices

Function and MC10500 Equivalent	MIL-M-38510 Device*
Quad OR/NOR Gate (MC10501)	MIL-M-38510/06001
Quad 2-Input NOR Gate (MC10502)	MIL-M-38510/06002
Triple 2-3-2 OR/NOR Gate (MC10505)	MIL-M-38510/06003
Triple 4-3-3 NOR Gate (MC10506)	MIL-M-38510/06004
Triple 2-Input Exclusive OR/Exclusive NOR Gate (MC10507)	MIL-M-38510/06005
Dual 4-5 Input OR/NOR Gate (MC10509)	MIL-M-38510/06006
Quad 2-Input AND (MC10504)	MIL-M-38510/06201
Hex AND (MC10597)	MIL-M-38510/06202
Quad MTTL to MECL Translator (MC10524)	MIL-M-38510/06301
Quad MECL to MTTL Translator (MC10525)	MIL-M-38510/06302
Dual D Flip-Flop (MC10531)	MIL-M-38510/06001
Dual D Flip-Flop (MC10631)	MIL-M-38510/06002
Hex D Flip-Flop (MC10576)	MIL-M-38510/06003
Dual J-K Flip-Flop (MC10535)	MIL-M-38510/06007

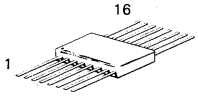
*JAN devices must have complete part number description.

MECL 10K
INTEGRATED CIRCUITS

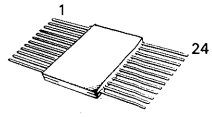
MC10,500/10,600 Series
(-55 to +125°C)



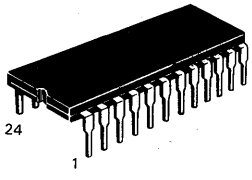
L SUFFIX
CERAMIC PACKAGE
CASE 620



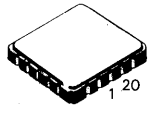
F SUFFIX
CERAMIC PACKAGE
CASE 650



F SUFFIX
CERAMIC PACKAGE
CASE 652



L SUFFIX
CERAMIC PACKAGE
CASE 623



Z SUFFIX
CERAMIC PACKAGE
CASE 756

Function Selection — (-55°C to +125°C)

NOR Gates	
Quad 2-Input Gate Strobe	MC10500
Quad 2-Input Gate	MC10502
Triple 4-3-3 Input Gate	MC10506
Dual 3-Input 3-Output Gate	MC10611
OR Gates	
Quad 2-Input Gate	MC10503
Dual 3-Input 3-Output Gate	MC10610
AND Gates	
Quad 2-Input Gate	MC10504
Hex Gate	MC10597
Complex	
Quad OR/NOR Gate	MC10501
Triple 2-3-2 Input OR/NOR Gate	MC10505
Dual 4-5 Input OR/NOR Gate	MC10509
Dual 3-Input 3-Output OR/NOR Gate	MC10612
Exclusive Triple 2-Input Gate	MC10507
Exclusive Quad 2-Input Gate	MC10513
Complex OR/AND Gate Function	MC10517
Complex OR/AND Gate Function	MC10518
Complex OR/AND Gate Function	MC10519
Complex OR/AND Gate Function	MC10521
Buffers/Inverters	
Hex Inverter/Buffer	MC10595

All devices have standard case 620 or 650.

Function Selection — (-55°C to +125°C)

Function	Device
Line Drivers/Line Receivers	
Triple Line Receiver	MC10514
Quad Line Receiver	MC10515
Triple Line Receiver	MC10516
Triple 4-3-3-Input Bus Driver	MC10523
Triple Line Receiver	MC10616
Dual Transceiver	MC10594
Flip-Flop/Latches	
Dual D Master Slave Flip-Flop	MC10531
Dual J-K Master Slave Flip-Flop	MC10535
Hex D Master Slave Flip-Flop	MC10576
Hex D Common Reset Flip-Flop	MC10586
Dual D Master Slave Flip-Flop	MC10631
Quad Latch	MC10533
Quint Latch	MC10575
Quad/Common Clock Latch	MC10568
Quad/Negative Clock Latch	MC10553
Dual Latch	MC10530
Multiplexer	
Quad 2 Input/Noninverting	MC10558
Dual Multiplexer/Latch	MC10532
Dual Multiplexer/Latch	MC10534
Quad 2-Input/Inverting	MC10559
8-Line	MC10564
Quad 2-Input Multiplexer with Latch	MC10573
Dual 4-1	MC10574

Function	Device
Decoders	
Binary to 1-8 (Low)	MC10561
Binary to 1-8 (High)	MC10562
Dual 4-Line (Low)	MC10571
Dual 4-Line (High)	MC10572
Counters	
Hexadecimal	MC10536
Decade	MC10537
Biquinary	MC10538
Binary Down Counter	MC10554
Binary	MC10578
Arithmetic Functions	
12-Bit Parity Generator	MC10560
Error Detection/Correction	MC10563
8-Input Priority Encoder	MC10565
5-Bit Magnitude Comparator	MC10566
9 + 2 Bit Parity Checker	MC10570
Look Ahead Carry Block	MC10579
Dual 2-Bit Adder/Subtractor	MC10580
4-Bit Arithmetic Function Gen.	MC10581
2-Bit Arithmetic Function Gen.	MC10582
Error Detection/Correction	MC10593
2-Bit Multiplier	MC10687
Translators	
Quad TTL-MECL	MC10524
Quad MECL-TTL	MC10525
Quad MST to MECL	MC10590
Hex MECL-MST	MC10591
Special Function	
4-Bit Shift Register	MC10541

*Contact your Motorola sales office or Motorola distributor for details on availability of special packages.

All devices have standard case 620 or 650.

MC10500/10600 Series

The MC10500/10600 series is a military temperature range (–55°C to +125°C) version of the MC10100/10200 series. Much of the design information contained in the General Information Section of this book is applicable to the MC10500/10600 series. However, specified limits differ over the extended temperature range. The MC10500/10600 series selector guide lists the device and case types available.

Table I defines the forcing functions and associated dc parameters at the operating temperature limits of the MC10500/10600 series. The dc parameters of Table I are specified driving loads of 100 ohms to –2.0 V.

Table I — MC10500/10600 Series Transfer Data for Temperature Variations

Forcing Function	Parameter	–55°C [1]	25°C [1]	125°C [1]	Unit
		MC10500 MC10600	MC10500 MC10600	MC10500 MC10600	
V_{IHmax}	V_{OHmax} V_{OHmin}	–0.880 –1.080	–0.780 –0.930	–0.630 –0.825	Vdc
V_{IHAmin}	V_{OHAmin}	–1.100 –1.255	–0.950 –1.105	–0.845 –1.000	Vdc
V_{ILAmax}	V_{OLAmax}	–1.510 –1.635	–1.475 –1.600	–1.400 –1.525	Vdc
V_{ILmin}	V_{OLmax} V_{OLmin}	–1.655 –1.920	–1.620 –1.850	–1.545 –1.820	Vdc
V_{ILmin}	I_{INLmin}	0.5	0.5	0.3	μA

NOTES: [1] MC10500, MC10600, and series specified driving 100 Ω to –2.0 V.

8