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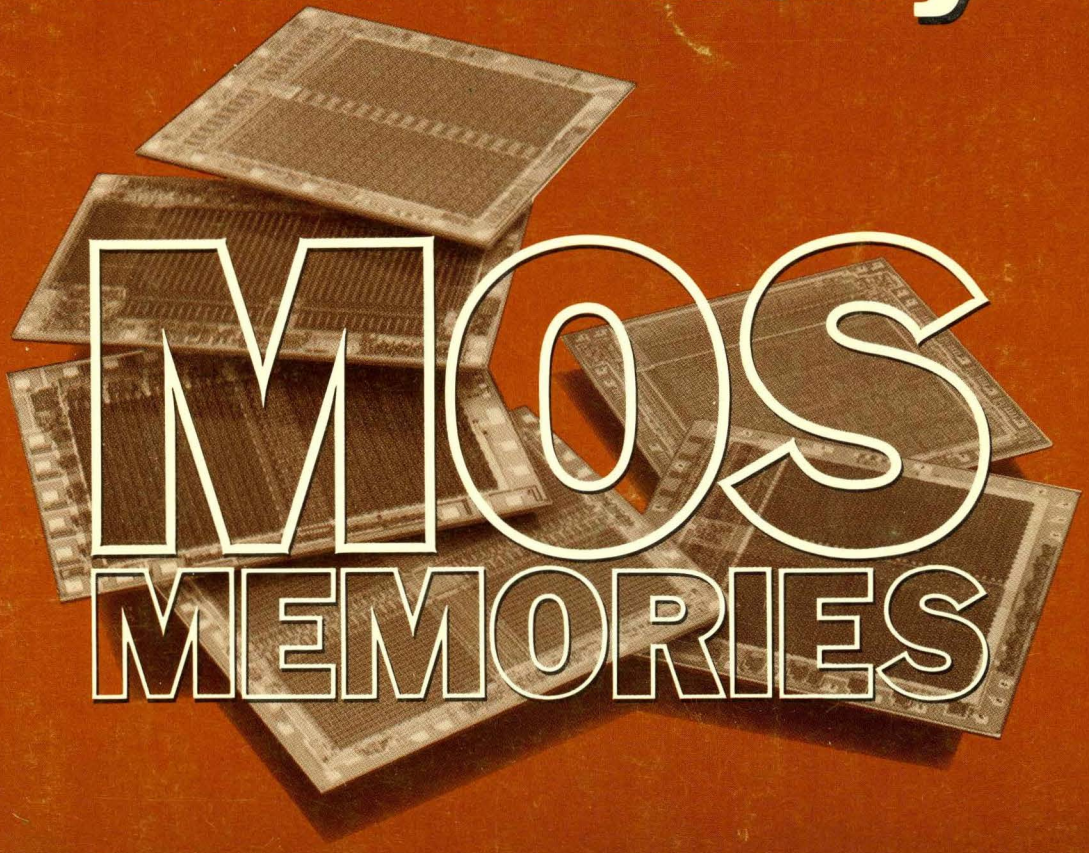

MOS MEMORIES

MOTOROLA Semiconductor Products Inc.

Semiconductor Data Library/MOS MEMORIES Vol. 7 Series A

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Volume 7/Series A

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MOS MEMORIES

This book presents technical data for the broad line of Motorola MOS Memories. Complete specifications for the individual parts are provided in the form of data sheets. Additional sections are provided to include pertinent information on application ideas, reliability concepts and data, and interface components. This book will greatly simplify the task of choosing the best combination of circuits for optimum system architecture.

The information in this book has been carefully checked and is believed to be reliable; however, no responsibility is assumed for inaccuracies. Furthermore, this information does not convey to the purchaser of microelectronic devices any license under the patent right of any manufacturer.

Series A

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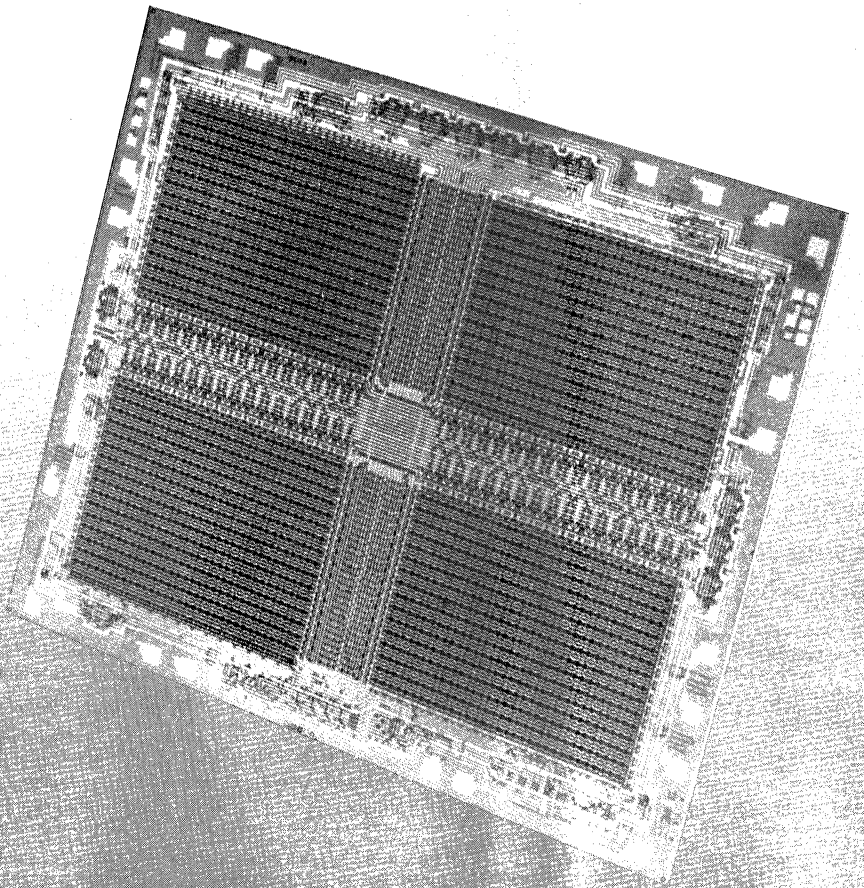

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CHAPTER 1 — GENERAL INFORMATION

INTRODUCTION

Memories are among the most important parts used in digital data-processing systems. Compared with the total system components needed, their share is growing at a faster rate than any other single portion. One of the recent and most promising additions to the memory arsenal is semiconductor memories. Since their appearance in the late 60's, they have had increasing acceptance all over the electronic industry. As a result, the semiconductor memory market is growing at a faster rate than other electronic market segments.

This rapid rate of growth has been characterized by a wide proliferation of memory components. The choice of the correct semiconductor memory for a particular application has become more difficult. The purpose of this data book is to assist the user in his decision-making process by making him familiar with Motorola's large family of MOS Memories and their characteristics.

In order to select the correct memory for his system, the user must be aware of many considerations. Among them are performance, power dissipation, memory density, interface requirements and special applications.

PERFORMANCE

The performance of a memory is widely interpreted to mean the maximum access time or minimum write cycle time guaranteed by the device specifications. Since the speed of a circuit depends on the gain of the devices comprising the circuit, performance is a strong function of technology. In general TTL, ECL and other bipolar memories are the fastest devices, offering both short access times and short write cycle times. An example would be the MCM10144 MECL RAM shown in Figure 1.

The device speeds of MOS memories, although not as fast as bipolar devices, have closed the gap considerably. For example, the 7001 RAM is fabricated with an N-Channel, charge-pump technique, and has an access time considerably less than 100 ns. Figure 2 illustrates the typical access times currently achieved with various memories of the different technologies.

POWER DISSIPATION

MOS technology currently enjoys the position of being the lowest consumer of power, with complementary MOS processes such as the McMOS process consuming the least. This is due to the nature of the insulated gate field effect transistor, as contrasted to bipolar techniques.

For MOS designs, power dissipation is primarily a function of whether the circuit is static or dynamic. A static memory will retain data as long as power is applied since the memory array stores data by means of cross-coupled latches which draw dc power. As a result, the power dissipation for static memories is the same during operation and standby conditions. (Although the 7001 offers static operation, this memory is an exception and has low standby power because of the low charge-pump current and the fact that the 7001 has a clock.)

In contrast, dynamic memories can be designed to use the clock input to drastically reduce power dissipation during standby. The MCM6604 RAM, for example, typically draws less than 1 mA during standby — the current required to maintain one active buffer to sense the low-level clock input. The MCM6605 RAM, which uses a high-level clock, consumes practically no power when the part is not operating. The only current is due to junction leakage and is typically a few microamperes.

Power dissipated during standby is a function of the duty cycle of the active refresh cycles which are required to maintain memory. The memory is stored dynamically on a capacitor comprised of PN junction capacitance, thin-oxide gate capacitance and parasitic capacitance. Because of the leakage at the junction, data storage is temporary and the memory must be refreshed periodically to restore the decaying nodes to full voltage levels. Since memory chips are designed and laid out in arrays, a chip can be refreshed by sequencing through the column addresses. The MCM6605, organized internally as 32 x 128, requires only 32 cycles for a refresh sequence. Assuming one cycle takes 500 ns and the time between refresh is 2 ms, the refresh duty cycle is 1.25%. When the power is added, with 98.75% in standby and 1.25% active, the total is still remarkably low — typically 2.6 mW.

MEMORY DENSITY

One of the distinct advantages of MOS technology is the packing densities achievable. More MOS devices can be packed into a given area than bipolar devices. In addition, MOS processing techniques are more forgiving than bipolar techniques, allowing larger chip sizes. For both reasons, MOS packs more into a chip, requiring far fewer chips per board or per system.

MOS memory density can be further broken down into two parts: density achievable with bits per chip and density achievable with board area per chip. As for the first, dynamic memories allow more bits per chip for a given chip size than static memories. Therefore, dynamic MOS memories are the most cost effective for bulk storage applications.

The densities achievable at the board level depend not only on the bits per chip but on the size of the package as well. Clever circuit design has allowed pin multiplexing and resulted in a 16-pin 4096-bit memory. This package consideration allows the user to put more chips on a given board.

INTERFACING REQUIREMENTS

Since a memory requires certain timing and voltage levels at the pins of the device, interfacing requirements become very important and must be considered in final board density. Static MOS and bipolar memories are the easiest to interface within a system and therefore require the fewest number of interface parts. By contrast, dynamic memories require clocks and refresh circuitry. Additional interface parts are required to provide these functions.

It is not automatically apparent which approach will lead to the smallest board layout. The static MOS and bipolar memories do not have the per part storage capability of the dynamic MOS memories. Therefore, for even a modest board, the additional parts required for dynamic operation may be fewer than the additional parts otherwise required for memory capacity. Each user must determine the tradeoffs for himself.

As another example of spacing and interface tradeoffs, the MCM6604 is packaged in a 16-pin case, which is considerably smaller than the 22-pin case used for the MCM6605. However, the MCM6604 requires more interface parts than the MCM6605 to provide the extra clocks and circuitry required for address multiplexing. Here again, the size of the system will determine whether or not the additional overhead devices will be smaller than the area consumed by the 22-pin MCM6605.

Input and output characteristics must also be considered. For example, CMOS devices operated at high voltage supplies need high level inputs. This will require a level translation from a TTL driver. As for outputs, there is a considerable difference between 3-state outputs, differential outputs and open drain outputs. The first is efficient for wire-ORing the parts on a bus. The second is fast but requires a sense amplifier. The last requires an external resistor.

SPECIAL APPLICATIONS

When a system has special requirements, the choice of memory becomes more limited. For example, high performance (50 ns) requirements can be met only by bipolar memories. Restrictive power requirements may dictate the use of CMOS memories. And microprocessor applications necessitate the use of 3-state output buffering. These considerations may dictate the choice of memory to be used.

One special application which is becoming more important is that of microprocessor-oriented systems. In the past, semiconductor memories have been tailored to meet the requirements of mainframe, bulk storage and have been organized accordingly. In the future, there will be a trend toward by 4, by 8 and by 16 output memories designed to minimize interface requirements in microprocessor applications.

MOS – THE DIFFERENCE

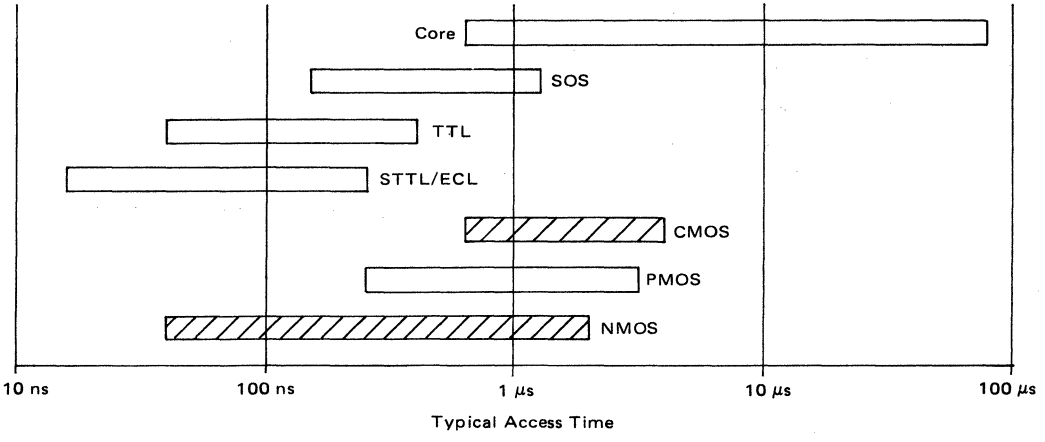
Each technology has its own particular advantages. Bipolar, for example, is fast. However, in almost every other area, MOS has the edge. MOS packing densities are greater, for example, producing physically smaller and cheaper systems. MOS power consumption is generally lower, with McMOS at the one end to provide ultra-low power consumption. MOS is lenient with voltage requirements, with CMOS again providing the least sensitivity and the most noise immunity. And MOS is approaching bipolar even on speed.

One of the greatest advantages of MOS is that its full potential has not yet been reached. Significant advances occur almost daily. And the limit to packing density has not yet been approached. MOS will become more and more dominant and its particular advantage of packing density combined with low power dissipation continues to make inroads into nearly all electronic applications.

FIGURE 1 – COMPARISON OF TYPICAL RANDOM ACCESS MEMORIES WITH DIFFERENT TECHNOLOGIES

Memory	Structure	Organization and Package	Performance		Power Dissipation		Power Supplies (V)	Interface Circuits Required
			Access Time (ns)	Write Cycle Time (ns)	Operating (mW)	Standby (mW)		
MCM6605	N-Channel Dynamic	4096 x 1 22 pin	210	490	335	8.0	+12, +5, -5	TTL inputs 3-state TTL output Refresh circuitry CE clock driver
7001	N-Channel Charge pump	1024 x 1 22 pin	60	180	650	0.5	+15, +8, -3	TTL inputs Differential open drain sense amp Charge pump oscillator CE clock driver
MCM6810	N-Channel Static	128 x 8 24 pin	575	500	350	350	+5	TTL inputs TTL output
MCM10144	ECL Static	256 x 1 16 pin	30	40	520	520	-5.2, -2.0	ECL inputs ECL output (pulldown resistor)
MCM14537	CMOS Static	256 x 1 16 pin	1 μs	1 μs	10	0.023	+15	High level inputs High level 3-state output

FIGURE 2 – TYPICAL ACCESS TIMES FOR MEMORIES WITH DIFFERENT TECHNOLOGIES



MEMORY GLOSSARY

Access Time	Time between application of address and availability of data at the output ("read time").
Address	(Noun) Code that identifies a specific location in a memory. (Verb) Selection of stored information for retrieval from a computer's memory.
ASCII	American Standard Code for Information Interchange (eight bit code).
Associative Memory	Addresses the data actually stored in the memory, not the location (see "CAM").
Bit	Acronym for BInary digiT (can be 0 or 1).
Byte	A grouping of a conveniently small number of adjacent bits that form a sub-unit of information. Through common usage, a byte is usually defined as containing eight bits.
Cache Memory	High-speed, low-capacity memory; similar to "scratch pad memory", but with larger capacity.
CAM	Content Addressable Memory. Retrieves information not by selecting a physical location, but by addressing the content (see "associative memory").
Capacity	Total number of bits that can be stored within a memory. Usually a power of 2 (e.g. $2^{10} = 1024$, called "1K").
CARAM	Acronym for Content Addressable Random Access Memory.
Cell	Basic storage element to memorize one bit of information.
Character Generator	Type of generator which creates letters, numerals, or symbols in desired sequence for any viewing medium. ROMs are commonly programmed to perform this function.
Charge Pump	Device based on a MOS transistor, where a small charge (current) flows from source to substrate when a pump frequency is applied to the gate. Used as a constant current source to replace load devices in some memory cells.
CMOS	Complementary MOS; circuit with both P- and N-Channel FETs on the same MOS wafer.
Cycle Time	Also called read-write cycle time. Measure of how long it takes to obtain information from a memory and then to write back information into the memory.
Driver	Device that can be controlled with normal logic levels, while its output is capable of sinking or sourcing high current (driving heavy capacitive loads).
DRO Memory	Destructive Read-Out memory, in which reading the contents of a storage cell destroys the contents of that location.
Dynamic Memory	Fast memory where the parasitic capacitance of MOS-FET gates within a storage cell is used for temporary storage of information. Due to junction leakage currents this is possible for only a finite time. Prior to the loss of data the information must be refreshed by some electrical methods.
Interface	Circuit to provide compatibility between systems with different logic levels or operating voltages.
LSB	Least Significant Bit; the lowest weighted digit of a binary number.
LSI	Large Scale Integration.
McMOS	Acronym for Motorola Complementary MOS. Trademark.
Mainframe Memory	The main working memory of a data processing system. Has medium storage capacity (up to 128K bytes).
MECL	Acronym for Motorola Emitter Coupled Logic. Trademark.

MOS	Metal Oxide Semiconductor, usually refers to the insulated gate FET.
MSB	Most Significant Bit; the highest weighted digit of a binary number.
MSI	Medium Scale Integration.
MTBF	Mean Time Before Failure.
NDRO Memory	Non Destructive Read-Out Memory, where the read operation does not cause the storage cell to lose the stored information. Most semiconductor memories are of this type.
NMOS	N-Channel Metal Oxide Semiconductor. MOS-FET where negative charge carriers (electrons) are used for operation.
Organization	Indicates how the storage cells are organized within the memory. Expressed in "words by (bits per word)". (e.g., 4096 x 1 = 4096 words of one bit per word; 64 x 4 = 64 words of four bits per word, etc.)
PMOS	P-Channel Metal Oxide Semiconductor. MOS-FET where positive charge carriers (holes) are used for operation.
RAM	Random Access Memory (read/write memory). Stored information is immediately available when addressed, regardless of the previous memory address location.
Random Access	The memory words can be selected in any order; access time is independent of storage cell location.
Read Time	Time between application of read control (and address) and availability of data at the output. More commonly called "access time".
Read/Write Memory	A memory in which the stored data is available at any time and can be changed in normal system operation. Also called a Random Access Memory (RAM).
Refresh Cycle	The time required for the process used to keep data stored in dynamic memory.
Reliability	The measure of a device's ability to function without failure over a period of time.
ROM	Read-Only Memory, permits the reading of predetermined pattern of bits.
SAM	Acronym for Sequential Access Memory. The memory words are selected in a fixed order. See Shift Register.
Scratch Pad Memory	An array of storage elements used where a small amount of data is temporarily stored and must be available promptly when needed. Very high speed.
Shift Register	Digital storage circuit which uses a chain of flip-flops to shift data from one flip-flop to its adjacent flip-flop on each clock pulse. A read/write memory with sequential access ("SAM").
Static Memory	A memory which needs no "refresh cycle" to keep the data stored. Simple operation and less control circuitry, but usually slower than dynamic memories.
Threshold Voltage	The condition at which conduction between source and drain of enhancement mode MOS-FETs is initiated.
Volatility	Stored information is lost in case of power shut-down.
Word	Set of bits, usually 8, 12, 16, 24, 32, etc.; treated as a unit. A word may contain one or more bytes.
Write Time	Time needed to store information safely into the memory, after presence of data input, write control and address.

UNDERSTANDING MOTOROLA'S DEVICE NUMBERING SYSTEM

The device number of Motorola integrated circuit memories gives some information about device function and characteristics. The MCM prefix stands for Motorola integrated Circuit Memories. This is followed by a four or five digit number which denotes a specific memory function and set of characteristics. The suffix contains information on circuit redesign, speed categories, package type, and/or allowed temperature range. The convention differs somewhat between the suffix for a McMOS MC14500 series memory and other MOS memories, as shown in the following examples:

Example 1 — NMOS Memory

MCM6605AL1

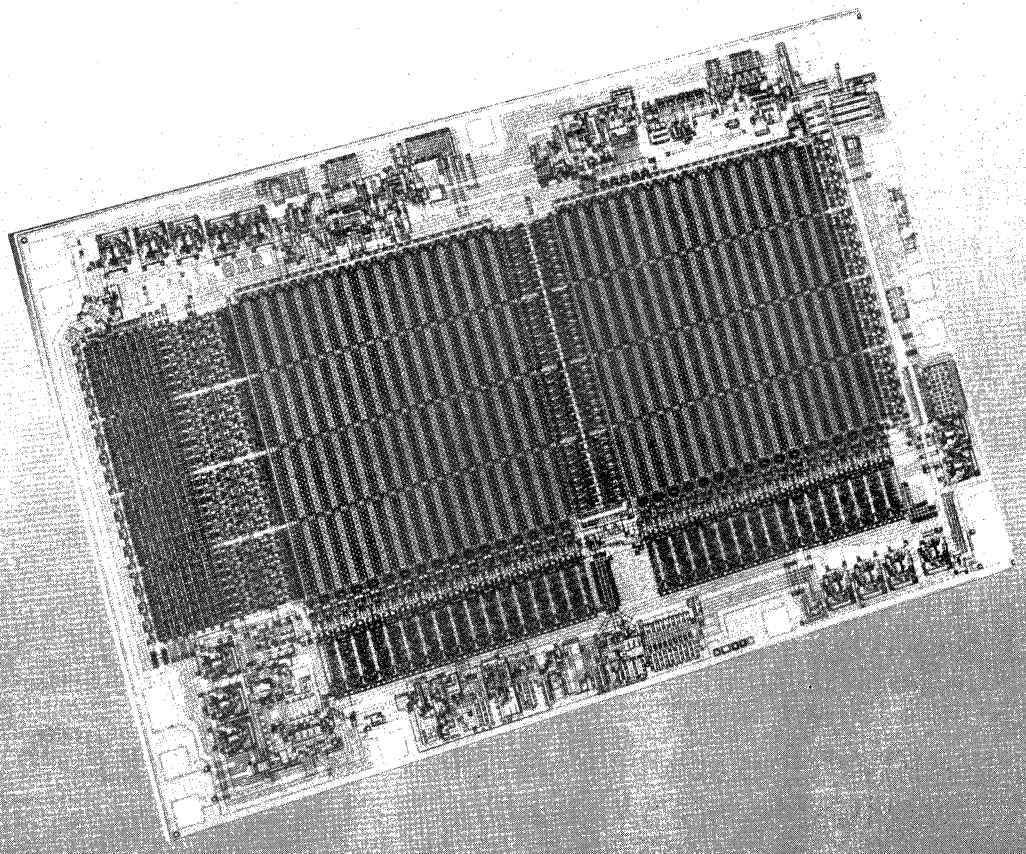
- The 1 indicates the fast version.
- The L indicates a ceramic dual in-line package is used. (A P suffix would indicate plastic.)
- The A indicates that the device is an improved version of the MCM6605.

Example 2 — McMOS MC14500 series Memory

MCM14524AL

- The L, as with NMOS, indicates ceramic dual in-line package. (P would indicate plastic.)
- The A indicates a full temperature range part (–55 to +125°C). A C suffix would indicate limited temperature range (–40 to +85°C).

Random Access Memories (RAM)/Chapter 2



MOS RANDOM ACCESS MEMORIES

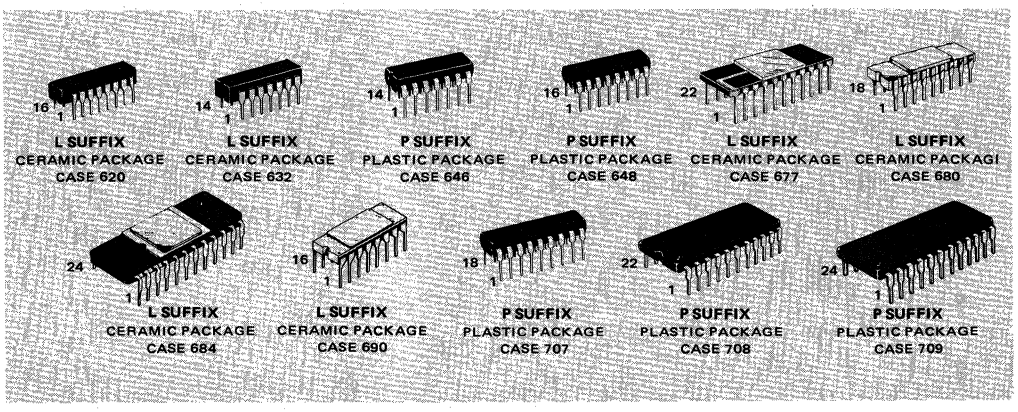
Random Access Memories are useful wherever temporary storage is required. They find application in large mainframe memory systems, minicomputers, and conventional digital control circuits.

RAMs which are specifically intended for use with the M6800 Microcomputer Family are shown in Chapter 4.

2

Device No.	No. of Bits	Description	Organization	Access Time (ns max)	Power Supplies (V)	No. of Pins	Case	Page No.
SILICON GATE NMOS								
MCM2102	1024	Static	1024 x 1	1000	+5	16	620, 648	2-3
MCM2102-1	1024	Static, High Speed	1024 x 1	500	+5	16	620, 648	2-3
MCM2102-2	1024	Static	1024 x 1	650	+5	16	620, 648	2-3
MCM2102A*	1024	Static, Verv High Speed	1024 x 1	350	+5	16	620, 648	2-7
MCM2102A2*	1024	Static, Very High Speed	1024 x 1	250	+5	16	620, 648	2-7
MCM2102A4*	1024	Static, Very High Speed	1024 x 1	450	+5	16	620, 648	2-7
MCM2111A	1024	Static, Common I/O and Output Disable	256 x 4	350	+5	18	680, 707	2-9
MCM2111A2	1024	Static, Common I/O and Output Disable	256 x 4	250	+5	18	680, 707	2-9
MCM2111A4	1024	Static, Common I/O and Output Disable	256 x 4	450	+5	18	680, 707	2-9
MCM2112A	1024	Static, Common I/O	256 x 4	350	+5	16	620, 648	2-13
MCM2112A2	1024	Static, Common I/O	256 x 4	250	+5	16	620, 648	2-13
MCM2112A4	1024	Static, Common I/O	256 x 4	450	+5	16	620, 648	2-13
MCM6604	4096	Dynamic	4096 x 1	350	+12, +5, −5	16	690, 648	2-17
MCM6604-2	4096	Dynamic	4096 x 1	250	+12, +5, −5	16	690, 648	2-17
MCM6604-4	4096	Dynamic	4096 x 1	300	+12, +5, −5	16	690, 648	2-17
MCM6605A	4096	Dynamic	4096 x 1	300	+12, +5, −5	22	677, 708	2-25
MCM6605A1	4096	Dynamic	4096 x 1	150	+12, +5, −5	22	677, 708	2-25
MCM6605A2	4096	Dynamic	4096 x 1	200	+12, +5, −5	22	677, 708	2-25
MCM6616*	16384	Dynamic	16384 x 1	350	+12, +5, −5	16	TBA	2-39
METAL GATE CMOS								
MCM14505A	64	Static, −55 to +125°C	64 x 1	550#	+3 to +18	14	632	2-41
MCM14505C	64	Static, −40 to +85°C	64 x 1	650#	+4.5 to +16	14	632, 646	2-41
MCM14537A	256	Static, −55 to +125°C	256 x 1	4000#	+3 to +18	16	690	2-51
MCM14537C	256	Static, −40 to +85°C	256 x 1	6000#	+4.5 to +16	16	690	2-51
MCM14552A	256	Static, −55 to +125°C	64 x 4	3000#	+3 to +18	24	684	2-59
MCM14552C	256	Static, −40 to +85°C	64 x 4	6000#	+4.5 to +16	24	684, 709	2-59

*To be announced #Measured with V_{DD} = +5 V, T_A = 25°C



MCM2102L/L1/L2
MCM2102P/P1/P2

1024-BIT STATIC RANDOM ACCESS MEMORY

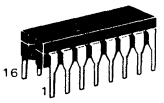
The MCM2102 is a 1024-bit random access memory fabricated with high-density, high-reliability, N-channel, silicon-gate technology. For ease of use, the device operates from a single power supply, is directly compatible with TTL and DTL, and requires no clocks or refreshing because of static operation.

- 1024 Word by 1 Bit Organization
- Access Time = 500 ns (MCM2102L1/P1)
  650 ns (MCM2102L2/P2)
  1000 ns (MCM2102L/P)
- Low Power Dissipation – 150 mW Typical
- Static Operation
- Single +5-Volt Supply
- Direct TTL/DTL Compatibility
- Three-State Output
- Chip Enable for Memory Expansion
- Cost Effective Data Storage

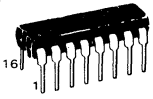
MOS

(N-CHANNEL, SILICON-GATE)

1024-BIT STATIC RANDOM ACCESS MEMORY



L SUFFIX
CERAMIC PACKAGE
CASE 620



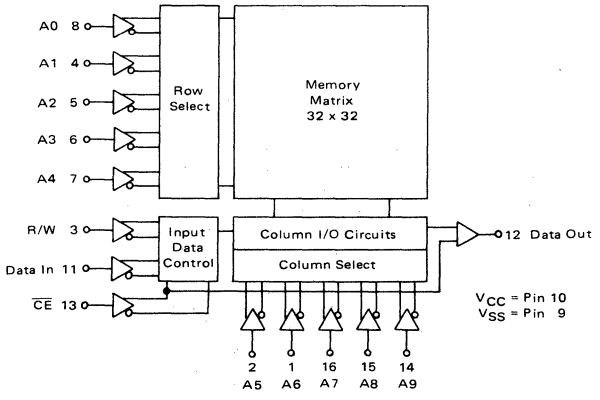
P SUFFIX
PLASTIC PACKAGE
CASE 648

ABSOLUTE MAXIMUM RATINGS[1] (Referenced to V_{SS})

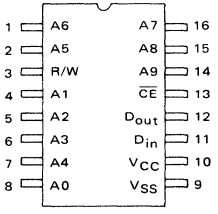
Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.3 to +7.0	Vdc
Input Voltages	V_{in}	-0.3 to +7.0	Vdc
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-55 to +150	°C

Note 1: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

BLOCK DIAGRAM



PIN ASSIGNMENT



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

2

DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted.)

RECOMMENDED DC OPERATING CONDITIONS (Referenced to V_{SS}).

Parameter	Symbol	Min	Nom	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	Vdc
Input Low Voltage	V_{IL}	-0.3	–	0.65	Vdc
Input High Voltage	V_{IH}	2.2	–	5.25	Vdc

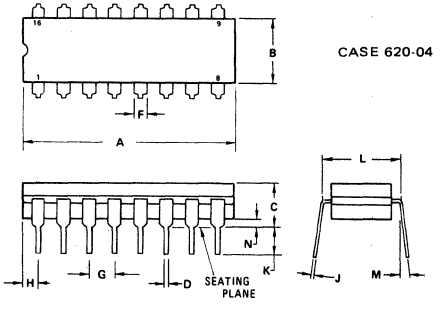
DC CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit
Input Leakage Current (All Inputs; V_{in} = 0 to 5.25 V)	I_{in}	–	–	10	μA
Output Leakage Current (Three-State) ($\overline{CE}$ = 2.2 V, V_{out} = 0.4 to 4 V)	I_{LO}	–	–	10	μA
Output High Voltage (I_{OH} = -100 μA)	V_{OH}	2.4	–	–	Vdc
Output Low Voltage (I_{OL} = 1.9 mA)	V_{OL}	–	–	0.45	Vdc
Power Supply Current (T_A = 0°C, V_{CC} = 5.25 V)	I_{CC}	–	30	70	mA

CAPACITANCE (Periodically sampled rather than 100% tested.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Capacitance (V_{in} = 0 V, f = 1.0 MHz, T_A = 25°C)	C_{in}	–	3.0	5.0	pF
Output Capacitance (V_{out} = 0 V, f = 1.0 MHz, T_A = 25°C)	C_{out}	–	7.0	10	pF

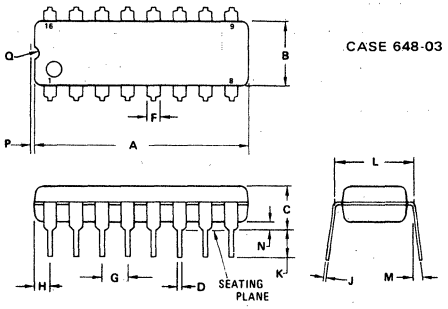
PACKAGE DIMENSIONS



CASE 620-04

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	19.05	19.94	0.750	0.785
B	6.10	7.49	0.240	0.295
C	–	5.08	–	0.200
D	0.38	0.53	0.015	0.021
F	1.40	1.78	0.055	0.070
G	2.54 BSC		0.100 BSC	
H	0.51	1.14	0.020	0.045
J	0.20	0.30	0.008	0.012
K	2.54	–	0.100	–
L	7.49	8.89	0.295	0.350
M	–	15°	–	15°
N	0.51	1.02	0.020	0.040

NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. PKG. INDEX: NOTCH IN LEAD NOTCH IN CERAMIC OR INK DOT.
3. DIM "A" AND "B" DO NOT INCLUDE GLASS RUN-OUT.
4. DIM "L" TO INSIDE OF LEADS (MEASURED 0.51 mm (0.020) BELOW BODY)



CASE 648-03

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	20.70	21.34	0.815	0.840
B	6.10	6.60	0.240	0.260
C	4.06	4.57	0.160	0.180
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.32	1.83	0.052	0.072
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.37	7.87	0.290	0.310
M	–	10°	–	10°
N	0.51	1.02	0.020	0.040
P	0.13	0.38	0.005	0.015
Q	0.51	0.76	0.020	0.030

NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL

AC CHARACTERISTICS

(All timing with $t_r = t_f = 20$ ns; Load = 1 TTL MC7400 Series Gate, $C_L = 100$ pF)

READ CYCLE

Characteristic	Symbol	Min	Max	Unit
Read Cycle Time	$t_{cyc(R)}$			ns
MCM2102L and MCM2102P		1000	–	
MCM2102L1 and MCM2102P1		500	–	
MCM2102L2 and MCM2102P2		650	–	
$\overline{\text{Chip Enable}}$ to Output Delay	t_{CO}			ns
MCM2102L and MCM2102P		–	500	
MCM2102L1 and MCM2102P1		–	350	
MCM2102L2 and MCM2102P2		–	400	
Output Data Valid Time				ns
Data Hold Time from Address	t_{DHA}	50	–	
Data Hold Time from Disable	t_{DHD}	0	–	
Read Access Time	t_{acc}			ns
MCM2102L and MCM2102P		–	1000	
MCM2102L1 and MCM2102P1		–	500	
MCM2102L2 and MCM2102P2		–	650	

WRITE CYCLE

Characteristic	Symbol	Min	Max	Unit
Write Cycle Time	$t_{cyc(W)}$			ns
MCM2102L and MCM2102P		1000	–	
MCM2102L1 and MCM2102P1		500	–	
MCM2102L2 and MCM2102P2		650	–	
Address Setup Time	t_{AS}			ns
MCM2102L and MCM2102P		200	–	
MCM2102L1 and MCM2102P1		150	–	
MCM2102L2 and MCM2102P2		200	–	
$\overline{\text{Chip Enable}}$ Setup Time	t_{CES}			ns
MCM2102L and MCM2102P		900	–	
MCM2102L1 and MCM2102P1		400	–	
MCM2102L2 and MCM2102P2		550	–	
Write Pulse Width	t_W			ns
MCM2102L and MCM2102P		750	–	
MCM2102L1 and MCM2102P1		300	–	
MCM2102L2 and MCM2102P2		400	–	
Write Recover Time	t_{WR}	50	–	ns
Data Setup Time	t_{DS}			ns
MCM2102L and MCM2102P		800	–	
MCM2102L1 and MCM2102P1		330	–	
MCM2102L2 and MCM2102P2		450	–	
Data Hold Time	t_{DH}	100	–	ns

FIGURE 1 – READ CYCLE TIMING*

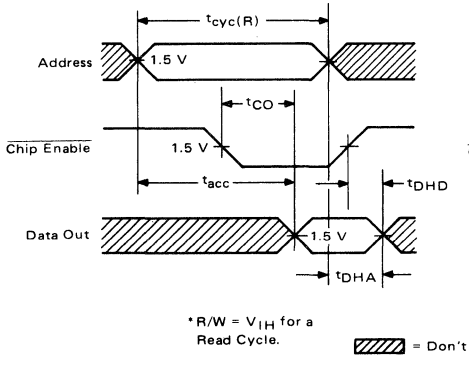
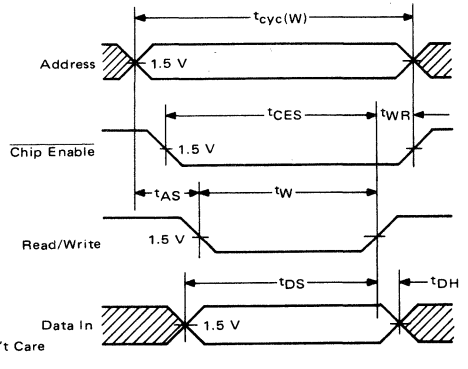


FIGURE 2 – WRITE CYCLE TIMING



2

TYPICAL CHARACTERISTICS CURVES

FIGURE 3 – ACCESS TIME versus V_{CC}

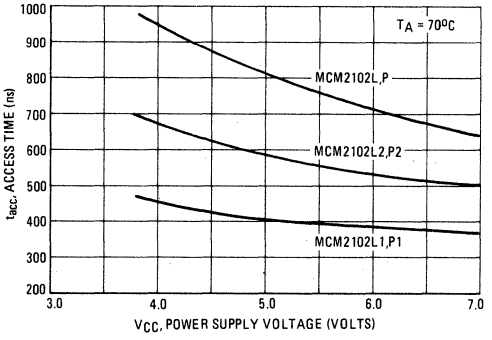


FIGURE 4 – ACCESS TIME versus AMBIENT TEMPERATURE

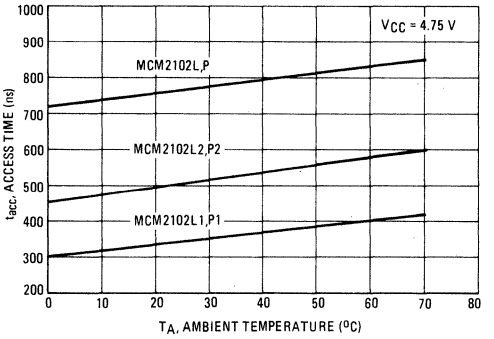


FIGURE 5 – I_{CC} SUPPLY CURRENT versus V_{CC}

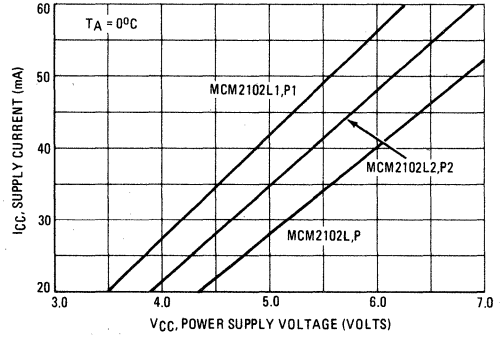
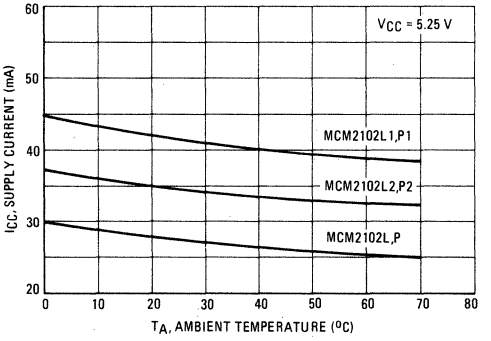


FIGURE 6 – I_{CC} SUPPLY CURRENT versus AMBIENT TEMPERATURE



MCM2102A L/L2/L4
MCM2102A P/P2/P4

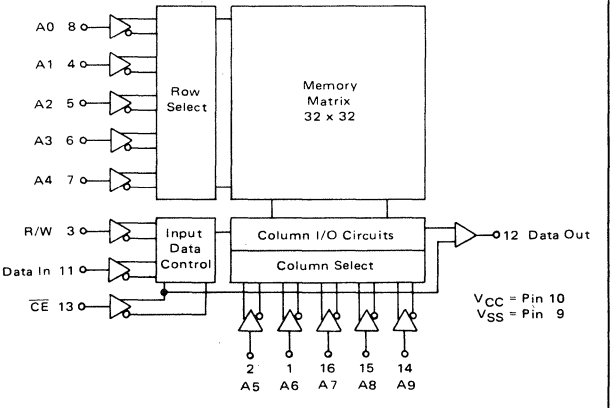
Product Preview

1024-BIT STATIC RANDOM ACCESS MEMORY

The MCM2102A is a 1024-bit random access memory fabricated with high-density, high-reliability, N-channel, silicon-gate, depletion-load technology. For ease of use, the device operates from a single power supply, is directly compatible with TTL and DTL, and requires no clocks or refreshing because of static operation.

- 1024 Word by 1 Bit Organization
- Access Time = 250 ns (L2, P2)
  350 ns (L, P)
  450 ns (L4, P4)
- Low Power Dissipation
- Static Operation
- Single +5-Volt Supply
- Direct TTL/DTL Compatibility
- Three-State Output
- Chip Enable for Memory Expansion
- Cost Effective Data Storage

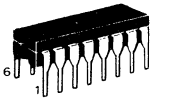
BLOCK DIAGRAM



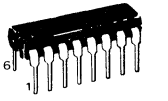
MOS

(N-CHANNEL, SILICON-GATE, DEPLETION LOAD)

1024-BIT STATIC RANDOM ACCESS MEMORY

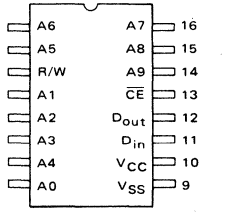


L SUFFIX
CERAMIC PACKAGE
CASE 620



P SUFFIX
PLASTIC PACKAGE
CASE 648

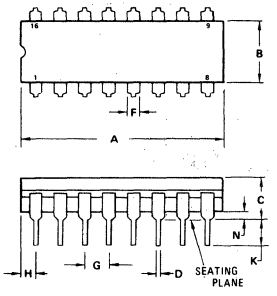
PIN ASSIGNMENT



This is advance information and specifications are subject to change without notice.

2

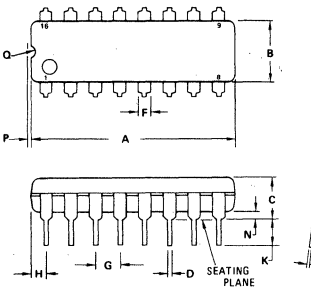
PACKAGE DIMENSIONS



CASE 620-04

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	19.05	19.94	0.750	0.785
B	6.10	7.49	0.240	0.295
C	–	5.08	–	0.200
D	0.38	0.53	0.015	0.021
F	1.40	1.78	0.055	0.070
G	2.54 BSC		0.100 BSC	
H	0.51	1.14	0.020	0.045
J	0.20	0.30	0.008	0.012
K	2.54	–	0.100	–
L	7.49	8.89	0.295	0.350
M	–	15°	–	15°
N	0.51	1.02	0.020	0.040

NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. PKG. INDEX: NOTCH IN LEAD NOTCH IN CERAMIC OR INK DOT.
3. DIM "A" AND "B" DO NOT INCLUDE GLASS RUN-OUT.
4. DIM "L" TO INSIDE OF LEADS (MEASURED 0.51 mm (0.020) BELOW BODY)



CASE 648-03

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	20.70	21.34	0.815	0.840
B	6.10	6.60	0.240	0.260
C	4.06	4.57	0.160	0.180
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.32	1.83	0.052	0.072
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.37	7.87	0.290	0.310
M	–	10°	–	10°
N	0.51	1.02	0.020	0.040
P	0.13	0.38	0.005	0.015
Q	0.51	0.76	0.020	0.030

NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL

MCM2111A L/L2/L4
MCM2111A P/P2/P4

2

Advance Information

256 X 4-BIT STATIC RANDOM ACCESS MEMORY

The MCM2111A is a 256 x 4-bit random access memory fabricated with high-density, high-reliability, N-channel, silicon-gate technology. For ease of use, the device operates from a single power supply, is directly compatible with TTL and DTL, and requires no clocks or refreshing because of static operation.

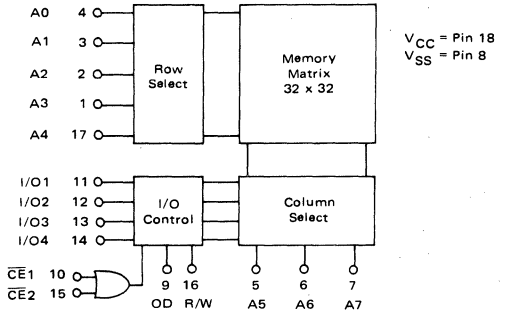
- 1024 Bits Organized as 256 x 4
- Access Time = 250 ns (L2/P2)
  = 350 ns (L/P)
  = 450 ns (L4/P4)
- Static Operation (No Clocks or Refreshing Required)
- Single +5-Volt Supply
- Direct TTL/DTL Compatibility
- Three-State Output
- Output Disable
- Chip Enable for Memory Expansion
- Cost Effective Data Storage

ABSOLUTE MAXIMUM RATINGS[1] (Referenced to V_{SS})

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.3 to +7.0	Vdc
Input Voltages	V_{in}	-0.3 to +7.0	Vdc
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

Note 1: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

BLOCK DIAGRAM



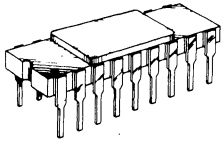
This is advance information and specifications are subject to change without notice.

MOS

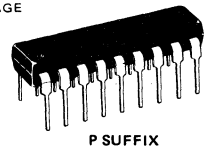
(N-CHANNEL, SILICON-GATE)

256 X 4-BIT STATIC RANDOM ACCESS MEMORY

with Common Data Inputs/Outputs and Output Disable

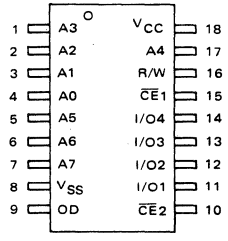


L SUFFIX
CERAMIC PACKAGE
CASE 680



P SUFFIX
PLASTIC PACKAGE
CASE 707

PIN ASSIGNMENT



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted.)

RECOMMENDED DC OPERATING CONDITIONS (Referenced to V_{SS}).

Parameter	Symbol	Min	Nom	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	Vdc
Input Low Voltage	V_{IL}	-0.3	–	0.8	Vdc
Input High Voltage	V_{IH}	2.0	–	5.25	Vdc

DC CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit
Input Leakage Current (All Inputs; V_{in} = 0 to 5.25 V)	I_{in}	–	–	10	μA
I/O Leakage Current (Three-State) ($\overline{CE}$ = 2.0 V, V_{out} = 0.4 to 4 V)	$I_{L\ I/O}$	–	–	10	μA
Output High Voltage (I_{OH} = -150 μA)	V_{OH}	2.4	–	–	Vdc
Output Low Voltage (I_{OL} = 2.1 mA)	V_{OL}	–	–	0.4	Vdc
Power Supply Current (T_A = 0°C, V_{CC} = 5.25 V)	I_{CC}	–	40	70	mA

CAPACITANCE (Periodically sampled rather than 100% tested.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input/Output Capacitance ($V_{I/O}$ = 0 V, f = 1.0 MHz, T_A = 25°C)	$C_{I/O}$	–	8.0	–	pF
Input Capacitance, Other Inputs (V_{in} = 0 V, f = 1.0 MHz, T_A = 25°C)	C_{in}	–	3.0	–	pF

AC CHARACTERISTICS

(All timing with $t_r = t_f$ = 20 ns; Load = 1 TTL MC7400 Series Gate, C_L = 100 pF)

READ CYCLE (Input pulse levels = 0.8 V to 2.0 V)

Characteristic	Symbol	MCM2111AL, P		MCM2111AL2, P2		MCM2111AL4, P4		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	$t_{cyc(R)}$	350	–	250	–	450	–	ns
Access Time	t_{acc}	–	350	–	250	–	450	ns
Chip Enable to Output Delay	t_{CO}	–	180	–	130	–	230	ns
Output Enable to Output Delay	t_{OE}	–	180	–	130	–	230	ns
Data Hold from Address	t_{DHA}	40	–	40	–	40	–	ns
Data Hold From Disable	t_{DHD}	0	80	0	60	0	90	ns
Data Hold from Write	t_{DHW}	0	80	0	60	0	90	ns

WRITE CYCLE (Input pulse levels = 0.8 V to 2.0 V)

Characteristic	Symbol	MCM2111AL,P		MCM2111AL2,P2		MCM2111AL4,P4		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	$t_{cyc(W)}$	350	–	250	–	450	–	ns
Chip Enable Pulse Width	t_{CE}	250	–	180	–	300	–	ns
Address Setup Time	t_{AS}	20	–	20	–	20	–	ns
Address Hold Time	t_{AH}	0	–	0	–	0	–	ns
Address to Write Release	t_{AWR}	350	–	250	–	450	–	ns
Write Pulse Width	t_W	250	–	180	–	300	–	ns
Data Setup Time	t_{DS}	150	–	100	–	190	–	ns
Data Hold Time	t_{DH}	0	–	0	–	0	–	ns

FIGURE 1 – READ CYCLE TIMING

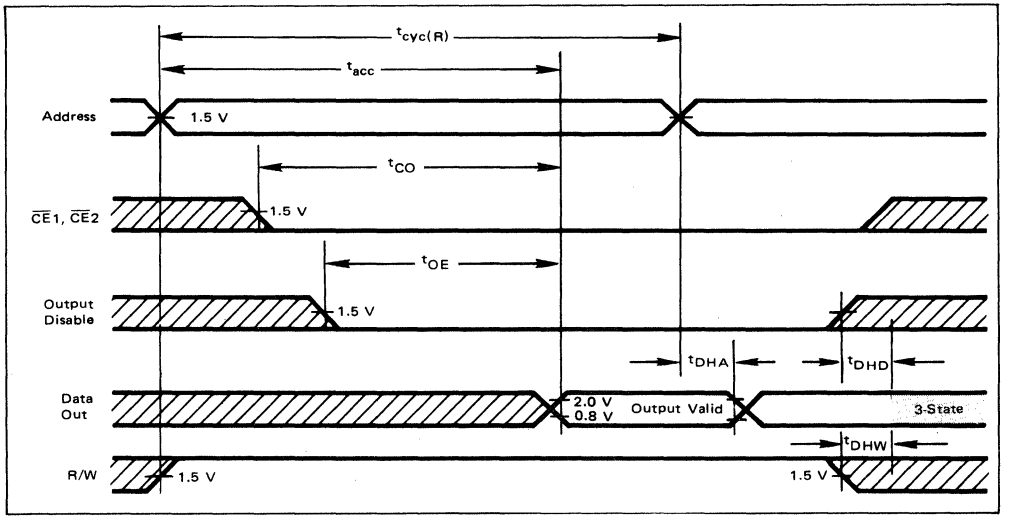
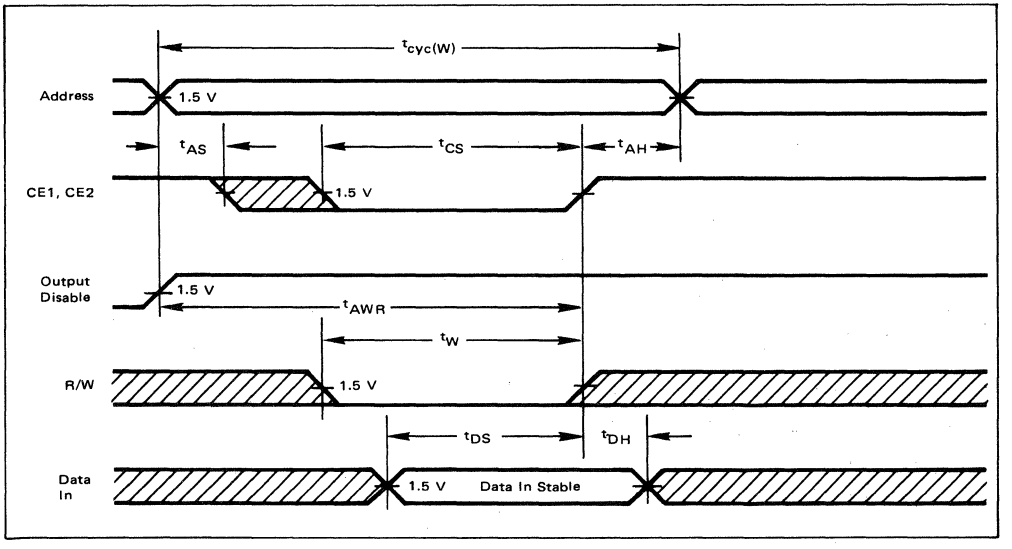


FIGURE 2 – WRITE CYCLE TIMING



= Don't Care

2

CIRCUIT DESCRIPTION

The MCM2111A memory matrix consists of 1024 static storage cells. The matrix is separated into four 256-bit memories operated in parallel to produce 256 4-bit words. A particular word is selected by a 1-of-32 (A0-A4) row address and a 1-of-8 (A5-A7) column address.

The I/O data lines are multiplexed to serve as data inputs during write cycles and as data outputs during read cycles. A read cycle is defined by the overlap of $\overline{CE}1 = \overline{CE}2 = V_{IL}$, OD = V_{IL}, and R/W = V_{IH}. During this time, the I/O ports will act as active outputs. A write cycle occurs at the overlap of $\overline{CE}1 = \overline{CE}2 = V_{IL}$ and R/W = V_{IL}. The I/O ports will be high impedance and data can easily be written in.

When $\overline{CE}1$ or $\overline{CE}2 = V_{IH}$, the chip is disabled; the I/O ports will be high impedance and data presented to these pins will be ignored. This feature of the MCM2111A allows wire-ORing of the part.

READ CYCLE

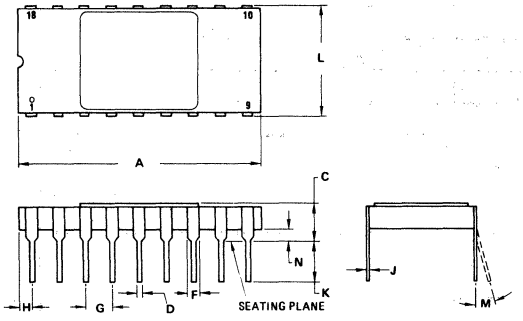
During a read cycle, the MCM2111A will drive the four I/O ports to their correct levels, as defined by the data stored at the address given. A series of successive read cycles may be performed holding $\overline{CE}1$, $\overline{CE}2$, and OD at V_{IL} and R/W at V_{IH}. In this case, the data out is valid t_{acc} nanoseconds after the change in address. Alternatively, the address may be applied with the chip deselected. In this case, valid data will occur t_{CO} nanoseconds after the last $\overline{CE} = V_{IL}$ and t_{OE} nanoseconds after OD = V_{IL}.

WRITE CYCLE

During a series of write cycles, $\overline{CE}1$ and $\overline{CE}2$ may be held at V_{IL}. However, R/W must be strobed according to the timing diagram. The minimum address setup time, t_{AS}, must be observed.

In order to write data into the MCM2111A, the I/O buffers on the chip should be high impedance. OD = V_{IH} may be used for this purpose as shown in the Write Timing Diagram, maintaining the I/O buffers in three-state for the entire cycle. However, OD need not be used and can remain at V_{IL}. In this case, the I/O buffers can become active during the time between $\overline{CE}1 = \overline{CE}2 = V_{IL}$ and R/W = V_{IL} (t_W). The buffers will remain active for t_{DHW} nanoseconds after the R/W = V_{IL} transition. Therefore, the I/O buffers will be in the three-state condition only for a guaranteed $t_W - t_{DS} - (t_{DHW}$ max) nonoseconds before input data must be valid.

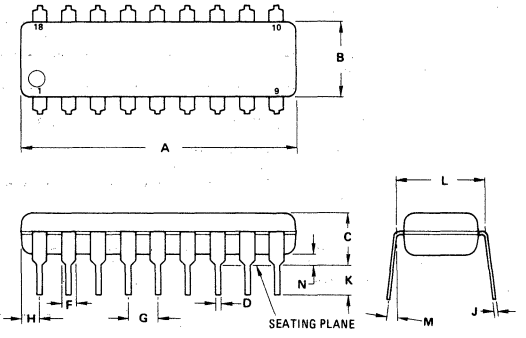
PACKAGE DIMENSIONS



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	22.61	23.11	0.890	0.910
C	3.18	4.27	0.125	0.168
D	0.43	0.58	0.017	0.023
F	0.89	1.14	0.035	0.045
G	2.54 BSC		0.100 BSC	
H	1.14	1.40	0.045	0.055
J	0.20	0.30	0.008	0.012
K	3.18	4.44	0.125	0.175
L	7.47	7.92	0.294	0.312
M	–	10°	–	10°
N	1.02	1.52	0.040	0.060

NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. NOMINAL DIM FROM CENTER OF LEADS PARALLEL TO DIM "L" IS 7.62 mm (0.300").

CASE 680-04



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	22.22	23.24	0.875	0.915
B	6.60	7.11	0.260	0.280
C	4.06	4.57	0.160	0.180
D	0.36	0.51	0.014	0.020
F	1.02	1.52	0.040	0.060
G	2.41	2.67	0.095	0.105
H	1.14	1.40	0.045	0.055
J	0.20	0.30	0.008	0.012
K	3.05	3.56	0.120	0.140
L	7.37	7.87	0.290	0.310
M	0°	10°	0°	10°
N	0.51	1.02	0.020	0.040

CASE 707-01

MCM2112A L/L2/L4
MCM2112A P/P2/P4

Advance Information

256 x 4-BIT STATIC RANDOM ACCESS MEMORY

The MCM2112A is a 256 x 4-bit random access memory fabricated with high-density, high-reliability, N-channel, silicon-gate technology. For ease of use, the device operates from a single power supply, is directly compatible with TTL and DTL, and requires no clocks or refreshing because of static operation.

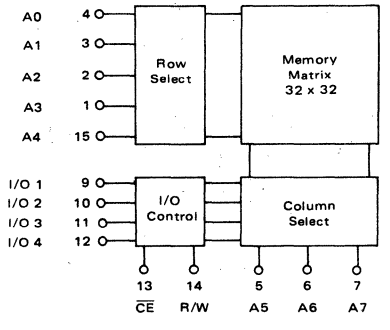
- 1024 Bits Organized as 256 x 4
- Access Time = 250 ns (L2,P2)
  350 ns (L,P)
  450 ns (L4,P4)
- Static Operation (No Clocks or Refreshing Required)
- Single +5-Volt Supply
- Direct TTL/DTL Compatibility
- Three-State Output
- Chip Enable for Memory Expansion
- Cost Effective Data Storage

ABSOLUTE MAXIMUM RATINGS[1] (Referenced to V_{SS})

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.3 to +7.0	Vdc
Input Voltages	V_{in}	-0.3 to +7.0	Vdc
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

Note 1: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

BLOCK DIAGRAM



V_{CC} = Pin 16
V_{SS} = Pin 8

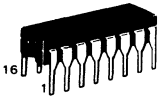
This is advance information and specifications are subject to change without notice.

MOS

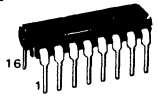
(N-CHANNEL, SILICON-GATE)

256 x 4-BIT STATIC RANDOM ACCESS MEMORY

with Common Data Inputs/Outputs

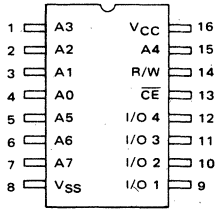


L SUFFIX
CERAMIC PACKAGE
CASE 620



P SUFFIX
PLASTIC PACKAGE
CASE 648

PIN ASSIGNMENT



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

2

DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted.)

RECOMMENDED DC OPERATING CONDITIONS (Referenced to V_{SS}).

Parameter	Symbol	Min	Nom	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	Vdc
Input Low Voltage	V_{IL}	-0.3	–	0.8	Vdc
Input High Voltage	V_{IH}	2.0	–	5.25	Vdc

DC CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit
Input Leakage Current (All Inputs; V_{in} = 0 to 5.25 V)	I_{in}	–	–	10	μA
I/O Leakage Current (Three-State) ($\overline{CE}$ = 2.0 V, V_{out} = 0.4 to 4 V)	$I_{L\ I/O}$	–	–	10	μA
Output High Voltage (I_{OH} = -150 μA)	V_{OH}	2.4	–	–	Vdc
Output Low Voltage (I_{OL} = 2.1 mA)	V_{OL}	–	–	0.4	Vdc
Power Supply Current (T_A = 0°C, V_{CC} = 5.25 V)	I_{CC}	–	40	70	mA

CAPACITANCE (Periodically sampled rather than 100% tested.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input/Output Capacitance ($V_{I/O}$ = 0 V, f = 1.0 MHz, T_A = 25°C)	$C_{I/O}$	–	8.0	–	pF
Input Capacitance, Other Inputs (V_{out} = 0 V, f = 1.0 MHz, T_A = 25°C)	C_{in}	–	3.0	–	pF

AC CHARACTERISTICS

(All timing with $t_r = t_f$ = 20 ns; Load = 1 TTL MC7400 Series Gate, C_L = 100 pF)

READ CYCLE (Input pulse levels = 0.8 V to 2.0 V)

Characteristic	Symbol	MCM2112AL,P		MCM2112AL2,P2		MCM2112AL4,P4		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	$t_{cyc(R)}$	350	–	250	–	450	–	ns
Access Time	t_{acc}	–	350	–	250	–	450	ns
Chip Enable to Output Delay	t_{CO}	–	180	–	130	–	230	ns
Data Hold from Address	t_{DHA}	40	–	40	–	40	–	ns
Data Hold from Disable	t_{DHD}	0	80	0	60	0	90	ns
Data Hold from Write	t_{DHW}	0	80	0	60	0	90	ns

WRITE CYCLE (Input pulse levels = 0.8 V to 2.0 V)

Characteristic	Symbol	MCM2112AL,P		MCM2112AL2,P2		MCM2112AL4,P4		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	$t_{cyc(W)}$	350	–	250	–	450	–	ns
Chip Enable Pulse Width	t_{CE}	250	–	180	–	300	–	ns
Address Setup Time	t_{AS}	20	–	20	–	20	–	ns
Address Hold Time	t_{AH}	0	–	0	–	0	–	ns
Address to Write Release	t_{AWR}	350	–	250	–	450	–	ns
Write Pulse Width	t_W	250	–	180	–	300	–	ns
Data Setup Time	t_{DS}	150	–	100	–	190	–	ns
Data Hold Time	t_{DH}	0	–	0	–	0	–	ns

FIGURE 1 – READ CYCLE TIMING

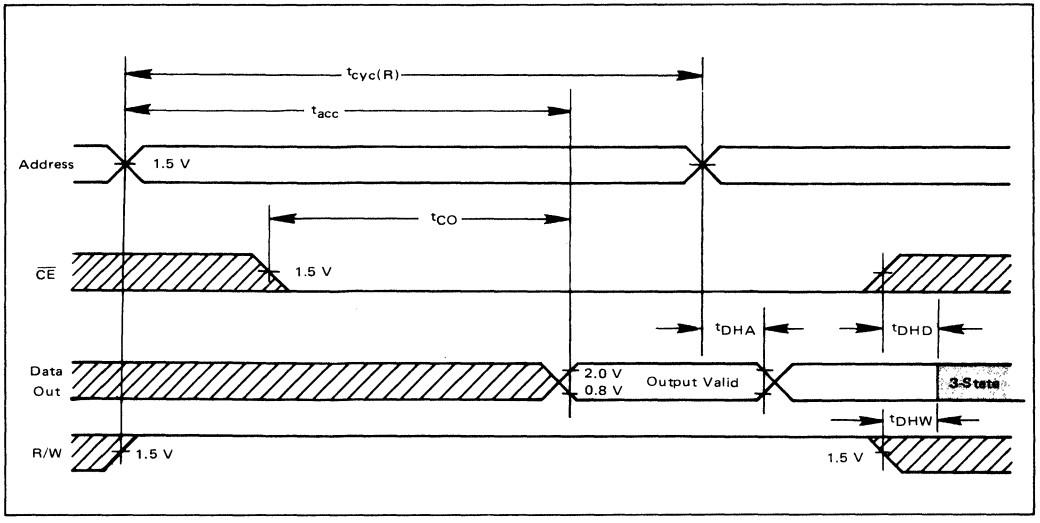
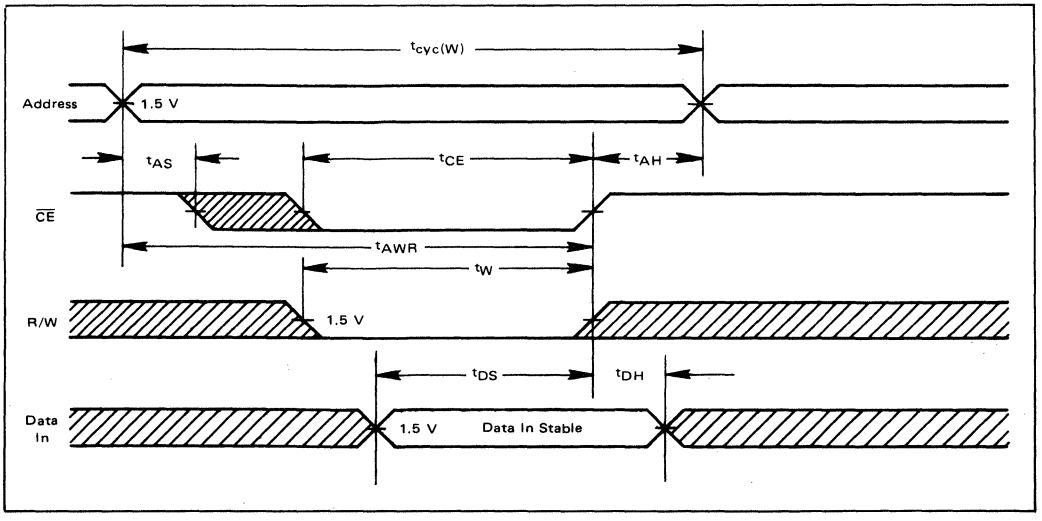


FIGURE 2 – WRITE CYCLE TIMING



= Don't Care

2

CIRCUIT DESCRIPTION

The MCM2112A memory matrix consists of 1024 static storage cells. The matrix is separated into four 256-bit memories operated in parallel to produce 256 4-bit words. A particular word is selected by a 1-of-32 (A0-A4) row address and a 1-of-8 (A5-A7) column address.

The I/O data lines are multiplexed to serve as data inputs during write cycles and as data outputs during read cycles. A read cycle is defined by the overlap of $\overline{CE}$ = V_{IL} and R/W = V_{IH}. During this time, the I/O ports will act as active outputs. A write cycle occurs at the overlap of $\overline{CE}$ = V_{IL} and R/W = V_{IL}. The I/O ports will be high impedance and data can easily be written in.

When $\overline{CE}$ = V_{IH} the chip is disabled; the I/O ports will be high impedance and data presented to these pins will be ignored. This feature of the MCM2112A allows wire-ORing of the part.

READ CYCLE

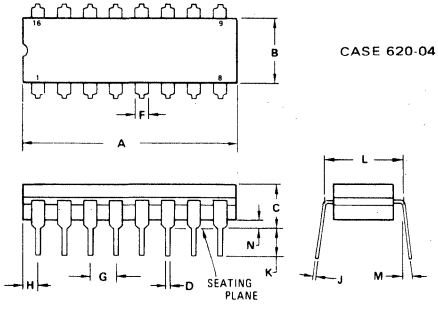
During a read cycle, the MCM2112A will drive the four I/O ports to their correct levels, as defined by the data stored at the address given. A series of successive read cycles may be performed holding $\overline{CE}$ at V_{IL} and R/W at V_{IH}. In this case, the data out is valid t_{acc} nanoseconds after the change in address. Alternatively, the address may be applied with the chip disabled. In this case, valid data will occur t_{CO} nanoseconds after the chip is enabled.

WRITE CYCLE

During a series of write cycles, R/W may be held at V_{IL}. However, $\overline{CE}$ must be strobed according to the timing diagram. The minimum address setup time, t_{AS}, must be observed.

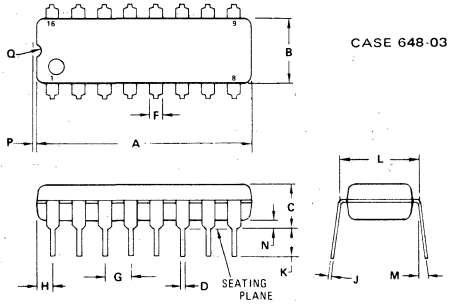
In order to write data into the MCM2112A, the I/O buffers on the chip should be high impedance. This will occur for either R/W = V_{IL} or $\overline{CE}$ = V_{IH}. However, there is a delay from these signals until the high impedance state occurs. The write timing of the MCM2112A guarantees a high impedance state before data in is required to be stable. The minimum time guaranteed is equal to $t_W - t_{DS} - (t_{DHW}max)$.

PACKAGE DIMENSIONS



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	19.05	19.94	0.750	0.785
B	6.10	7.49	0.240	0.295
C	–	5.08	–	0.200
D	0.38	0.53	0.015	0.021
F	1.40	1.78	0.055	0.070
G	2.54 BSC		0.100 BSC	
H	0.51	1.14	0.020	0.045
J	0.20	0.30	0.008	0.012
K	2.54	–	0.100	–
L	7.49	8.89	0.295	0.350
M	–	15^0	–	15^0
N	0.51	1.02	0.020	0.040

NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. PKG. INDEX: NOTCH IN LEAD NOTCH IN CERAMIC OR INK DOT.
3. DIM "A" AND "B" DO NOT INCLUDE GLASS RUN-OUT.
4. DIM "L" TO INSIDE OF LEADS (MEASURED 0.51 mm (0.020) BELOW BODY)



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	20.70	21.34	0.815	0.840
B	6.10	6.60	0.240	0.260
C	4.06	4.57	0.160	0.180
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.32	1.83	0.052	0.072
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.37	7.87	0.290	0.310
M	–	10^0	–	10^0
N	0.51	1.02	0.020	0.040
P	0.13	0.38	0.005	0.015
Q	0.51	0.76	0.020	0.030

NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL

MCM6604L/L2/L4
MCM6604P/P2/P4

2

Advance Information

4096-BIT DYNAMIC RANDOM ACCESS MEMORY

The MCM6604 is a 4096-bit high-speed dynamic Random Access Memory designed for high-performance, low-cost applications in mainframe and buffer memories and peripheral storage. Organized as 4096 one-bit words and fabricated using Motorola's highly reliable N-channel silicon gate technology, this device optimizes speed, power, and density tradeoffs.

By multiplexing row and column address inputs, the MCM6604 requires only six address lines and permits packaging in Motorola's standard 16-pin dual in-line packages. Complete address decoding is done on chip with address latches incorporated.

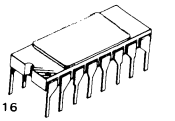
All inputs are TTL compatible, and the output is 3-state TTL compatible. The MCM6604 incorporates a one-transistor cell design and dynamic storage techniques, with each of the 64 row addresses requiring a refresh cycle every 2.0 milliseconds.

- Organized as 4096 Words of 1 Bit
- Maximum Access Time = 250 ns (L2,P2)
  300 ns (L4,P4)
  350 ns (L,P)
- Minimum Read and Write Cycle Time =
  400 ns (L2,P2)
  450 ns (L4,P4)
  500 ns (L,P)
- Low Power Dissipation
  555 mW Maximum (Active)
  24 mW Maximum (Standby)
- TTL Compatible
- 3-State Output
- On-Chip Latches for Address, Chip Select, and Data In
- Power Supply Pins on Package Corners for Optimum Layout
- Standard 16-Pin Package
- Compatible with the Popular 2104/MK4096

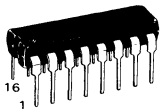
MOS

(N-CHANNEL, SILICON-GATE)

4096-BIT DYNAMIC RANDOM ACCESS MEMORY

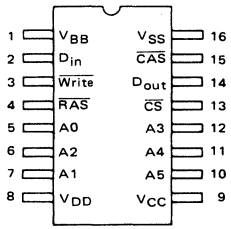


L SUFFIX
CERAMIC PACKAGE
CASE 690



P SUFFIX
PLASTIC PACKAGE
CASE 648

PIN ASSIGNMENT



ABSOLUTE MAXIMUM RATINGS (See Note 1)

Rating	Symbol	Value	Unit
Voltage on Any Pin Relative to V_{BB}	V_{in}, V_{out}	-0.3 to +20	Vdc
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

NOTE 1: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

This is advance information and specifications are subject to change without notice.

2

DC OPERATING CONDITIONS AND CHARACTERISTICS
(Full operating voltage and temperature range unless otherwise noted.)

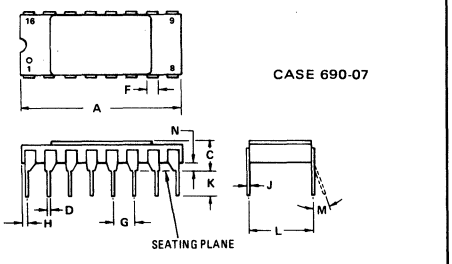
RECOMMENDED OPERATING CONDITIONS (Referenced to V_{SS} = Ground)

Parameter		Symbol	Min	Nom	Max	Unit
Supply Voltage		V_{DD}	11.4	12.0	12.6	Vdc
		V_{CC}	4.5	5.0	5.5	Vdc
		V_{BB}	-4.5	-5.0	-5.5	Vdc
Input High Voltage	An, $\overline{CS}$, D_{in}	V_{IH}	2.4	–	V_{CC}	Vdc
	$\overline{RAS}$, $\overline{CAS}$, Write		3.0	–	V_{CC}	
Input Low Voltage	All Inputs	V_{IL}	-1.0	–	0.8	Vdc

DC CHARACTERISTICS (V_{DD} = 12 V ±5%, V_{CC} = 5.0 V ±10%, V_{BB} = -5.0 V ±10%)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Current, Any Input (V_{in} = 0 to V_{CC})	I_{in}	–	–	10	μA
Output High Voltage (I_O = -3.0 mA)	V_{OH}	2.4	–	–	Vdc
Output Low Voltage (I_O = 2.0 mA)	V_{OL}	–	–	0.4	Vdc
Output Leakage Current (Output Disabled by $\overline{CS}$ Input)	I_{LO}	–	–	10	μA
Average Supply Current, Active Mode ($T_{cyc(W)}$ = min)	I_{DDA}	–	–	44	mA
	I_{CCA}	–	–	100	μA
	I_{BBA}	–	–	100	μA
Supply Current, Standby Mode	I_{DDS}	–	–	2.0	mA
	I_{CCS}	–	–	10	μA
	I_{BBS}	–	–	100	μA

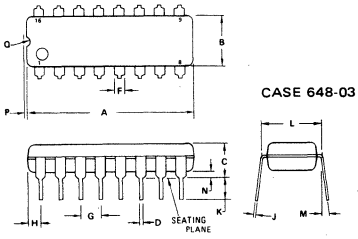
PACKAGE DIMENSIONS



CASE 690-07

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	18.80	19.23	0.740	0.757
C	2.67	3.94	0.105	0.155
D	0.41	0.51	0.016	0.020
F	1.14	1.40	0.045	0.055
G	2.54 BSC		0.100 BSC	
H	0.51	0.71	0.020	0.028
J	0.20	0.31	0.008	0.012
K	3.56	4.83	0.140	0.190
L	7.62 BSC		0.300 BSC	
M	–	10°	–	10°
N	0.64	1.14	0.025	0.045

NOTE
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.



CASE 648-03

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	20.70	21.34	0.815	0.840
B	6.10	6.60	0.240	0.260
C	4.06	4.57	0.160	0.180
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.32	1.83	0.052	0.072
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.37	7.87	0.290	0.310
M	–	10°	–	10°
N	0.51	1.02	0.020	0.040
P	0.13	0.38	0.005	0.015
Q	0.51	0.76	0.020	0.030

NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL

EFFECTIVE CAPACITANCE (Full operating voltage and temperature range, periodically sampled rather than 100% tested.)

Characteristic		Symbol	Max	Unit
Input Capacitance	A_n	$C_{in(EFF)}$	10	pF
	$\overline{RAS}$, $\overline{CAS}$, D_{in}, $\overline{Write}$, $\overline{CS}$		7.0	
Output Capacitance		$C_{out(EFF)}$	8.0	pF

2

AC OPERATING CONDITIONS AND CHARACTERISTICS
(Read, Write, and Read-Modify-Write Cycles)

RECOMMENDED AC OPERATING CONDITIONS (V_{DD} = 12 V ±5%, V_{CC} = 5.0 V ±10%, V_{BB} = –5.0 V ±10%, T_A = 0 to 70°C)

Parameter	Symbol	MCM6604L,P		MCM6604L2,P2		MCM6604L4,P4		Unit
		Min	Max	Min	Max	Min	Max	
Random Read or Write Cycle Time	t_{cyc}	500	–	400	–	450	–	ns
Read-Modify-Write Cycle Time	$t_{cyc(RMW)}$	700	–	540	–	620	–	ns
Row Address Strobe Precharge Time	t_{RP}	150	–	150	–	150	–	ns
Row to Column Strobe Lead Time (Note 1)	t_{RCL}	110	150	70	110	90	130	ns
Column Address Strobe Pulse Width	t_{CPW}	200	–	140	–	170	–	ns
Address Setup Time	t_{AS}	0	–	0	–	0	–	ns
Address Hold Time	t_{AH}	100	–	60	–	80	–	ns
$\overline{RAS}$ Address Release Time	t_{AR}	250	–	170	–	210	–	ns
Read Command Setup Time	t_{RCS}	0	–	0	–	0	–	ns
Read Command Hold Time	t_{RCH}	100	–	60	–	80	–	ns
Read Command Pulse Width	t_{RPW}	300	–	200	–	250	–	ns
Write Command Hold Time (Note 2)	t_{WCH}	150	–	110	–	130	–	ns
Write Command Pulse Width	t_{WP}	200	–	140	–	170	–	ns
Column to Row Strobe Lead Time	t_{CRL}	–50	+50	–40	+40	–45	+45	ns
Write Command to Column Strobe Lead Time	t_{CWL}	200	–	140	–	170	–	ns
Data In Setup Time	t_{DS}	0	–	0	–	0	–	ns
Data In Hold Time	t_{DH}	150	–	110	–	130	–	ns
Refresh Period	t_{REF}	–	2.0	–	2.0	–	2.0	ms
Modify Time	t_{MOD}	0	10	0	10	0	10	µs

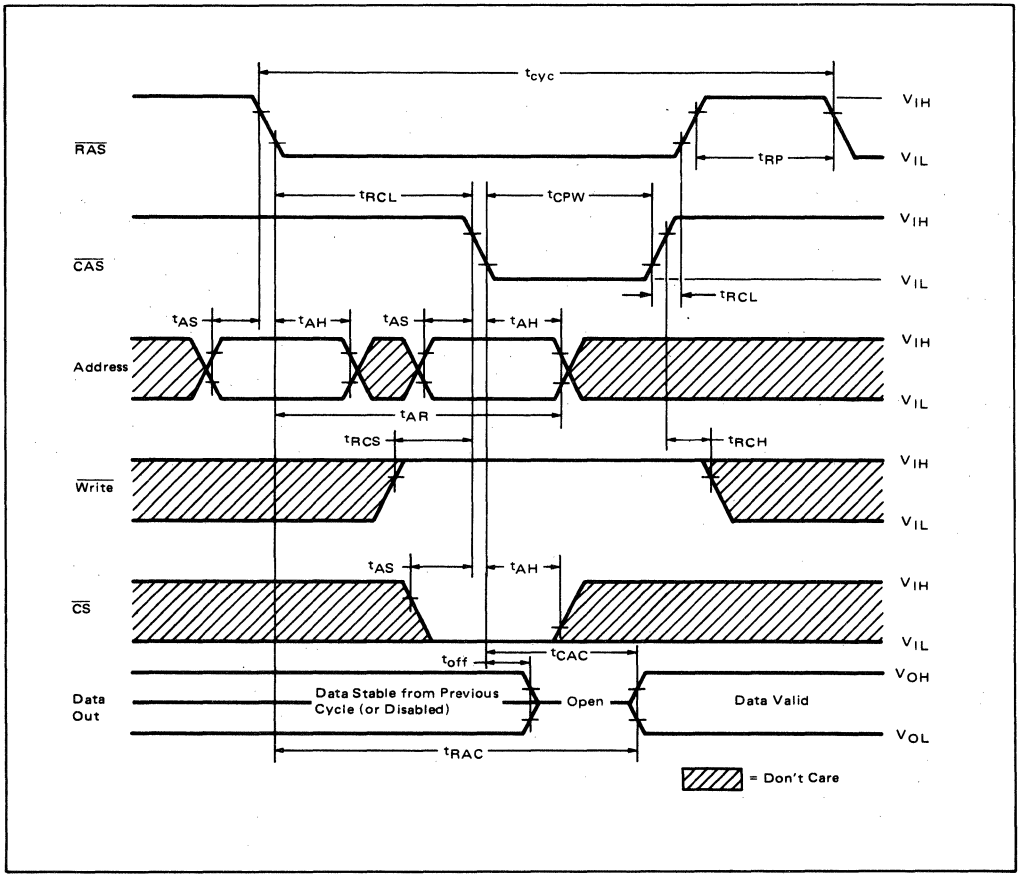
1. If t_{RCL} is greater than the maximum recommended value shown in this table, t_{cyc} and t_{RAC} will increase by the amount that t_{RCL} exceeds the value shown.
2. The Write Command Hold Time is important only when normal random write cycles are being performed. During a read-write or a read-modify-write cycle, the limiting parameter is the Write Command Pulse Width.

AC CHARACTERISTICS ($t_r = t_f$ = 20 ns, Load = 1 MC74H00 Series TTL Gate, $C_{L(EFF)}$ = 50 pF)

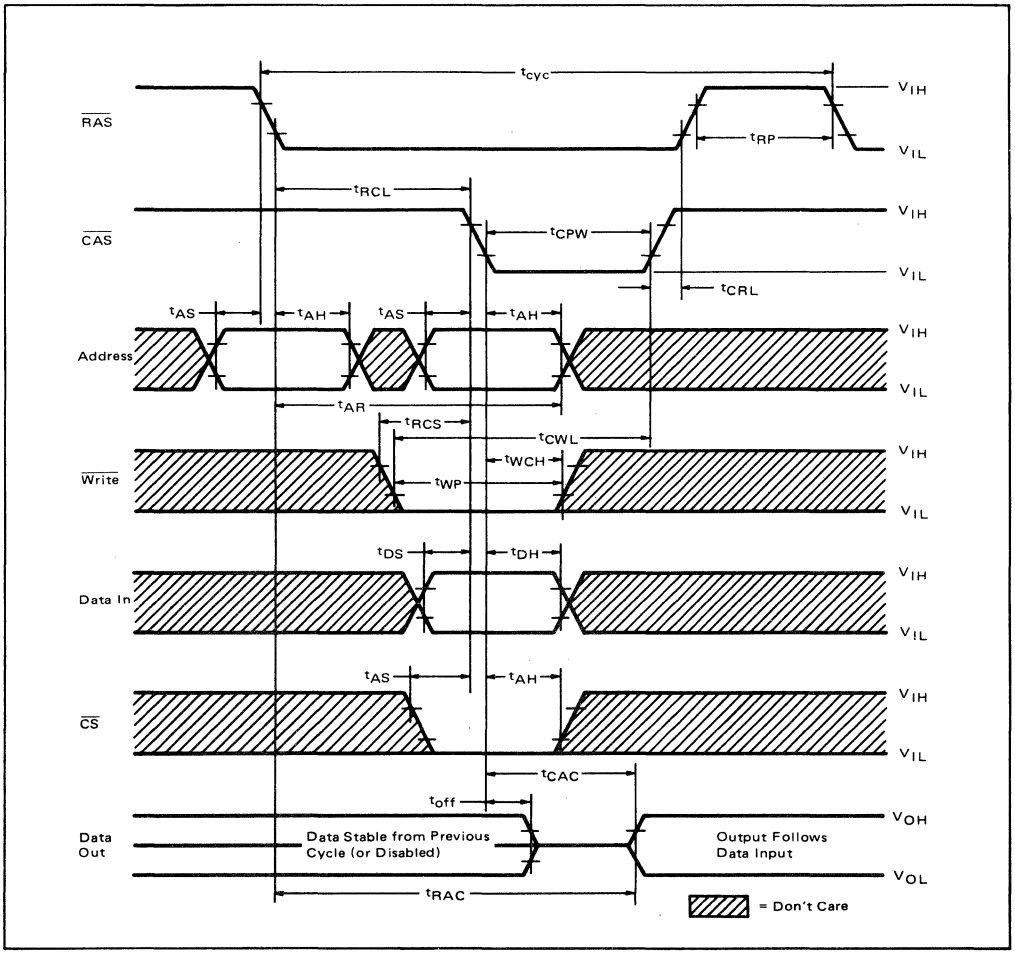
Characteristic	Symbol	MCM6604L,P	MCM6604L2,P2	MCM6604L4,P4	Unit
		Max	Max	Max	
Access Time from Row Address Strobe ($t_{RCL} \leq$ 150 ns for MCM6604L,P) ($t_{RCL} \leq$ 110 ns for MCM6604L2,P2) ($t_{RCL} \leq$ 130 ns for MCM6604L4,P4)	t_{RAC}	350	250	300	ns
Access Time from Column Address Strobe	t_{CAC}	200	150	175	ns
Output Buffer Turn-Off Delay	t_{off}	100	65	85	ns

2

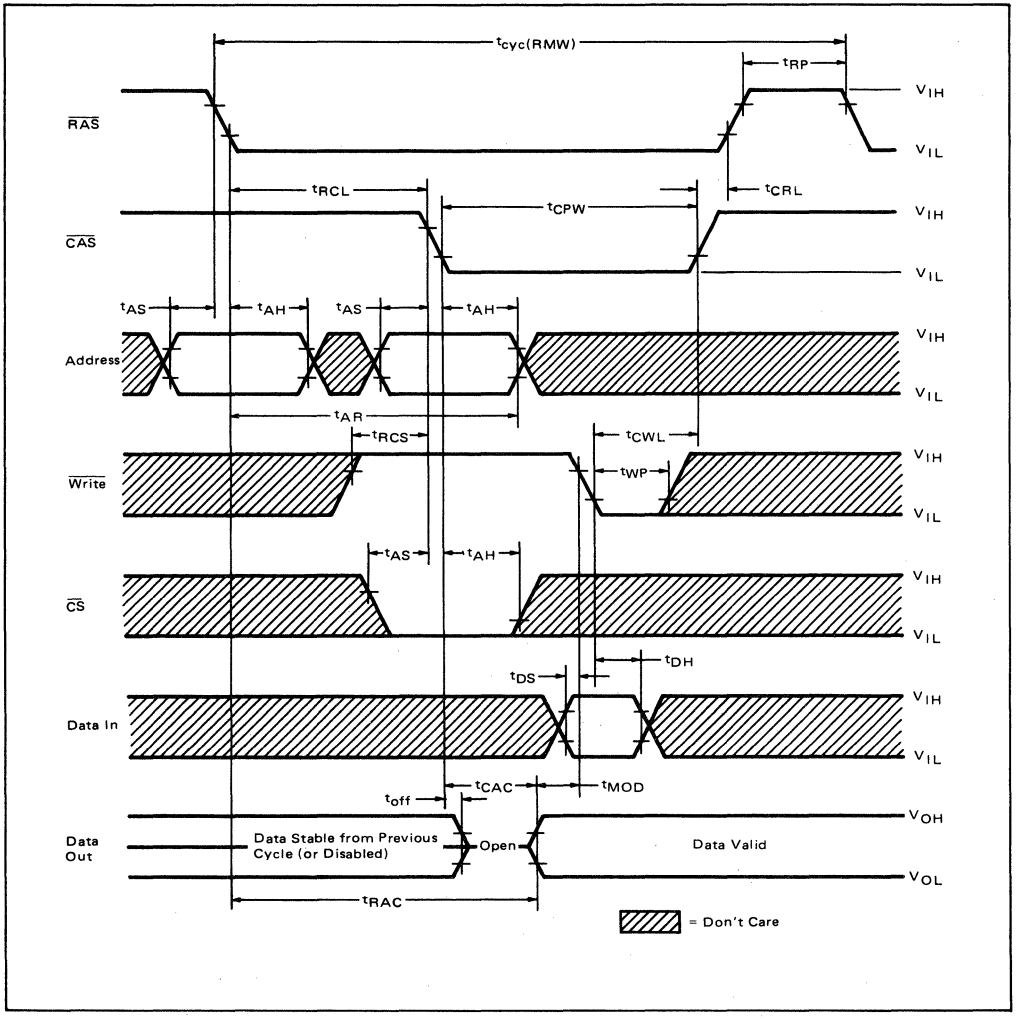
READ CYCLE TIMING



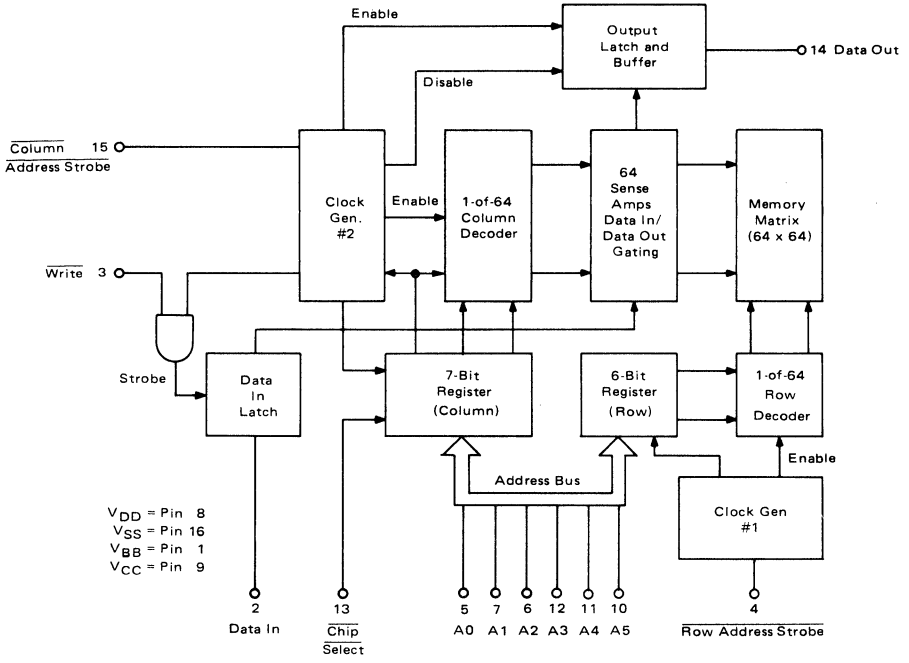
WRITE CYCLE TIMING



READ – MODIFY – WRITE TIMING



BLOCK DIAGRAM



ADDRESSING

The MCM6604 has six address inputs (A0 through A5) that are common to two address registers, one register for the row address and another for the column address. The column register has an additional latch that accommodates the Chip Select ($\overline{CS}$) signal. At the start of a memory cycle, the row address is latched into the address register with the Row Address Strobe ($\overline{RAS}$) signal. Next, the 6-bit column address is placed on the address bus along with the Chip Select signal, and they are latched into the column register with the Column Address Strobe ($\overline{CAS}$). Since the Chip Select signal is latched well into the memory cycle, its decoding time will not increase the memory system access or cycle time.

DATA OUTPUT

In order to simplify the memory system design and reduce the total package count, the MCM6604 contains an input data latch and a buffered output data latch. The state of the output latch and buffer at the end of a memory cycle will depend on the type of memory cycle performed and whether the chip is selected or unselected for that memory cycle.

A chip will be unselected during a memory cycle if:

(1) The chip receives both $\overline{RAS}$ and $\overline{CAS}$ signals, but no Chip Select signal.

(2) The chip receives a $\overline{CAS}$ signal but no $\overline{RAS}$ signal. With this condition, the chip will be unselected regardless of the state of Chip Select input.

If, during a read, write, or read-modify-write cycle, the chip is unselected, the output buffer will be in the high impedance state at the end of the memory cycle. The output buffer will remain in the high impedance state until the chip is selected for a memory cycle.

For a chip to be selected during a memory cycle, it must receive the following signals: $\overline{RAS}$, $\overline{CAS}$, and Chip Select. The state of the output latch and buffer of a selected chip during the following type of memory cycles would be:

(1) Read Cycle – On the negative edge of $\overline{CAS}$, the output buffer will unconditionally go to a high impedance state. It will remain in this state until access time. At this time, the output latch and buffer will assume the logic state of the data read from the selected cell. This output state will be maintained until the chip receives the next $\overline{CAS}$ signal.

(2) Write Cycle – If the $\overline{Write}$ input is switched to a logic 0 before the $\overline{CAS}$ transition, the output latch and buffer will be switched to

the state of the data input at the end of the access time. This logic state will be maintained until the chip receives the next $\overline{CAS}$ signal.

(3) Read-Modify-Write — Same as a read cycle.

DATA INPUT

Data to be written into a selected storage cell of the memory chip is first stored in the on-chip data latch. The gating of this latch is performed with a combination of the $\overline{Write}$ and $\overline{CAS}$ signals. The last of these signals to make a negative transition will strobe the data into the latch. If the $\overline{Write}$ input is switched to a logic 0 at the beginning of a write cycle, the falling edge of $\overline{CAS}$ strobes the data into the latch. The data setup and hold times are then referenced to the negative edge of $\overline{CAS}$.

If a read-modify-write cycle is being performed, the $\overline{Write}$ input would not make its negative transition until after the $\overline{CAS}$ signal was enabled. Thus, the data would not be strobed into the latch until the negative transition of $\overline{Write}$. The data setup and hold times would now be referenced to the negative edge of the $\overline{Write}$ signal. The only other timing constraints for a write-type cycle is that both the $\overline{CAS}$ and $\overline{Write}$ signals remain in the logic 0 state for a sufficient time to accomplish the permanent storage of the data into the selected cell.

INPUT/OUTPUT LEVELS

All of the inputs to the MCM6604 are TTL compatible. The inputs feature high impedance and low capacitance (<10 pF) characteristics which will minimize the driver requirements in a memory system. The three-state data output buffer is TTL compatible and has sufficient current sink capability (2 mA) to drive one high speed TTL load. The output buffer also has a separate V_{CC} pin so that it can be powered from the same supply as the logic being employed.

POWER DISSIPATION

Since the MCM6604 is a dynamic RAM, its power drain will be extremely small during the time the chip is unselected.

The power of the MCM6604 increases when selected and most of this increase is encountered on the address strobe edge. Hence, the power will be a function of the duty cycle.

In a memory system, the $\overline{CAS}$ signal must be supplied to all the memory chips to insure that the outputs of the unselected chips are switched to the high impedance state. Those chips that do not receive an $\overline{RAS}$ signal will not dissipate any power on the $\overline{CAS}$ edge except for that required to turn off the chip outputs. Thus, in order to insure minimum system power, the $\overline{RAS}$ signal should be decoded so that only the chips to be selected receive an $\overline{RAS}$ signal. If the $\overline{RAS}$ signal is decoded, then the chip select input of all the chips can be set to a logic 0 state.

REFRESH

The MCM6604 is refreshed by sequentially cycling through the 64 row addresses every 2 milliseconds or less. It is not necessary to supply the $\overline{CAS}$ to the chip while it is being refreshed. Any read, write, or read-modify-write cycle will refresh a selected row. However, if a write cycle is used to perform a refresh cycle the chip must be unselected.

MCM6605A L/L1/L2
MCM6605A P/P1/P2

4096-BIT DYNAMIC RANDOM ACCESS MEMORY

The MCM6605A is a 4096-bit high-speed dynamic Random Access Memory designed for high-performance, low-cost applications in mainframe and buffer memories and peripheral storage. Organized as 4096 one-bit words, these memories are fabricated using selective oxidation N-channel silicon gate technology to optimize device speed, power and density tradeoffs.

All address and control inputs are TTL compatible except for a single high-level clock (Chip Enable). Complete address decoding is done on chip and address latches are incorporated for ease of use. Refresh of the entire memory can be accomplished by sequentially cycling through addresses A0-A4 (32 cycles) a maximum of every 2.0 milliseconds.

The MCM6605A uses a three-transistor memory cell to simplify internal sense amplifier requirements. Output data is inverted with respect to input data. The outputs are 3-state TTL configuration and require no external sense amplifier. Outputs are in the high impedance (floating) state when either the Chip Enable is in the low state or the $\overline{\text{Chip Select}}$ is in the high state.

- Organized as 4096 Words of 1 Bit

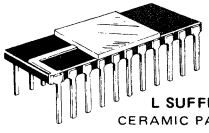
	L1, P1	L2,P2	L, P
• Maximum Access Time =	150 ns	200 ns	300 ns
• Minimum Read Cycle Time =	280 ns	360 ns	470 ns
• Minimum Write Cycle Time =	390 ns	490 ns	590 ns
• Minimum Read Modify Write Cycle Time =	390 ns	490 ns	590 ns

- Low Power Dissipation
  335 mW Typical (Active)
  2.6 mW Typical (Standby with Refresh)
- Easy Refresh – Only 32 Cycles Every 2.0 ms
- TTL Compatible
- 3-State Output
- Address Latches On Chip
- Power Supply Pins on Package Corners for Layout Simplification
- Typical Applications:
  Main Memory
  Buffer Memory
  Peripheral Storage

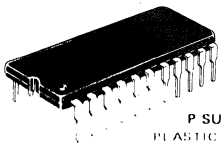
MOS

(N-CHANNEL, SILICON-GATE)

4096-BIT DYNAMIC RANDOM ACCESS MEMORY

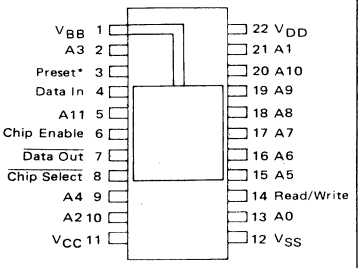


L SUFFIX
CERAMIC PACKAGE
CASE 677



P SUFFIX
PLASTIC PACKAGE
CASE 708

PIN ASSIGNMENT



*See Applications Information

ABSOLUTE MAXIMUM RATINGS (See Note 1)

Rating	Symbol	Value	Unit
Voltage on Any Pin Relative to V_{BB}	V_{in}, V_{out}	-0.3 to +20	Vdc
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

NOTE 1: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted.)

RECOMMENDED DC OPERATING CONDITIONS (Referenced to V_{SS}).

Parameter	Symbol	Min	Nom	Max	Unit
Supply Voltage	V_{DD}	11.4	12	12.6	Vdc
	V_{CC}	4.5	5.0	5.5	Vdc
	V_{SS}	0	0	0	Vdc
	V_{BB}	-5.25	-5.0	-4.75	Vdc
Logic Levels Input High Voltage (A_n, D_{in}, R/W, $\overline{CS}$)	V_{IH}	3.0	–	V_{DD} + 1.0	Vdc
Input Low Voltage (A_n, D_{in}, R/W, $\overline{CS}$)	V_{IL}	-1.0	–	0.8	Vdc
Chip Enable High Voltage	V_{CEH}	V_{DD} -1.0	–	V_{DD} + 1.0	Vdc
Chip Enable Low Voltage	V_{CEL}	-1.0	–	0.8	Vdc

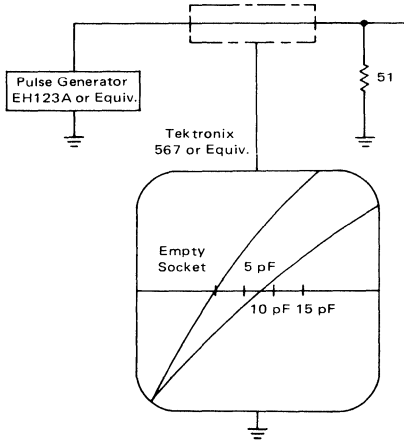
DC CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit
Input Current (A_n, D_{in}, R/W, $\overline{CS}$, Preset) (V_{in} = 0 to V_{DD} + 1.0 V)	I_{in}	–	–	10	μA
Input Chip Enable Current (V_{in} 0 to V_{DD} + 1.0 V)	I_{ICE}	–	–	10	μA
Output High Voltage (I_O = -100 μA)	V_{OH}	2.4	–	V_{CC}	Vdc
Output Low Voltage (I_O = 2.0 mA)	V_{OL}	V_{SS}	–	0.45	Vdc
Output Leakage Current (V_O = 0.45 V to V_{CC}, CE = V_{CEL}, or $\overline{CS}$ = V_{IH})	I_{LO}	–	–	10	μA
Average Supply Current, Active Mode ($T_{cyc(W)}$ = min)	I_{DDA}	–	28	36	mA
	I_{CCA}	–	0.05	1.0	mA
	I_{BBA}	–	–	100	μA
Supply Current, Standby Mode (CE = V_{CEL})	I_{DDS}	–	1.0	20	μA
	I_{CCS}	–	–	10	μA
	I_{BBS}	–	1.0	20	μA

EFFECTIVE CAPACITANCE (Test Circuit of Figure 1, full operating voltage and temperature range, periodically sampled rather than 100% tested.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Capacitance (A_n, D_{in}, R/W, $\overline{CS}$, Preset)	$C_{in(EFF)}$	–	4.0	5.0	pF
Chip Enable Capacitance	$C_{CE(EFF)}$	–	25	30	pF
Output Capacitance	$C_{out(EFF)}$	–	4.0	5.0	pF

FIGURE 1 – MEASUREMENT OF EFFECTIVE CAPACITANCE



Effective capacitance is determined by comparing the rise time of the voltage waveform at a particular pin to that measured with known values of capacitance. Scope calibration points are determined by using the rise times obtained with the empty socket and standard capacitor values as references.

The device under test (DUT) is inserted into the test socket and normal operating power supplies applied. All input pins, except that being measured, are grounded. The effective capacitance of the desired pin can then be read directly from the scope.

Pin	R	Input Pulse	Measurement Level
CE	67 Ω	16 V	12 V
Input/Output	100 Ω	6.0 V	4.0 V

AC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature unless otherwise noted.)

OPERATING MODES

Mode	Control States		Output
	R/W	$\overline{CS}$	
Active (CE = High)			
Read Only	H	L	Valid
Read/Write	H → L	L	Valid
Write Only	L	L	Valid
Read Refresh	H → L	L → H	Valid → Floating
Refresh Only	L	H	Floating
Chip Disable (Unselected)	H	H	Floating
Standby (CE = Low)	X	X	Floating

X = Don't Care

RECOMMENDED AC OPERATING CONDITIONS (Read, Write, and Read Modify Write Cycles)

Parameter		Symbol	Min	Max	Unit
Address Setup Time		t_{AS}	0	–	ns
Address Hold Time		t_{AH}	60	–	ns
CE Pulse Transition Time		t_T	–	100	ns
CE Off Time	MCM6605AL,P/L2,P2	t_{SB}	120	–	ns
	MCM6605AL1,P1		90	–	
Chip Select Delay Time		t_{CSD}	–	70	ns
Chip Select Hold Time		t_{CSH}	0	–	ns
Read Write Delay Time		t_{RWD}	–	70	ns
Read Write Hold Time		t_{RWH}	0	–	ns
Time Between Refresh		t_{REF}	–	2.0	ms

2

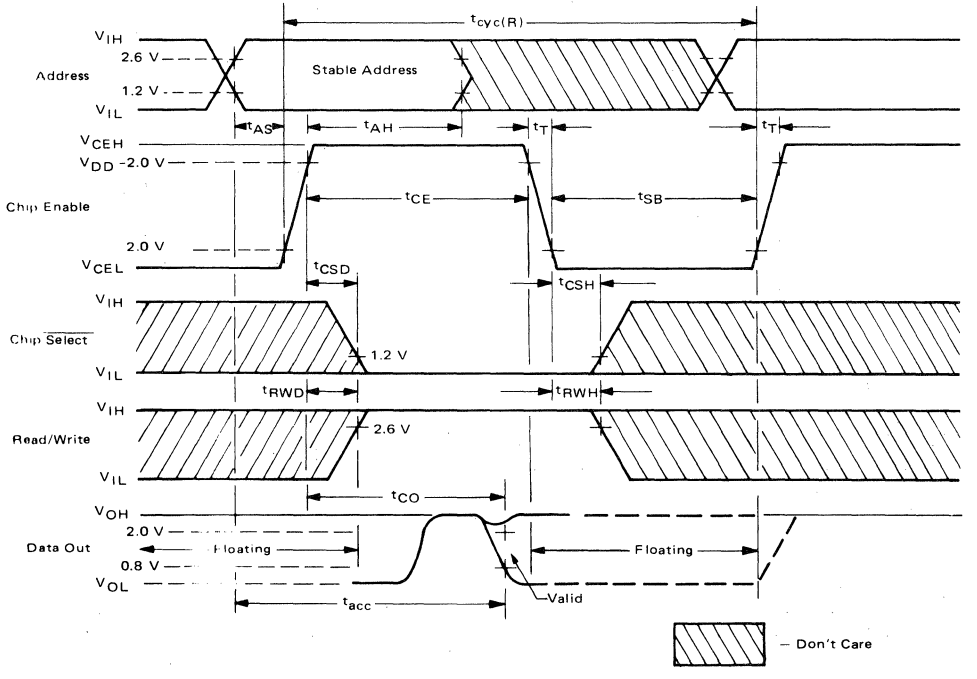
AC CHARACTERISTICS

[All timing with t_T = 20 ns; Load = 1 TTL Gate (MC74H00 Series), C_L = 50 pF (effective)]

READ CYCLE (R/W = V_{IH}, $\overline{CS}$ = V_{IL})

Characteristic	Symbol	MCM6605AL,P		MCM6605AL1,P1		MCM6605AL2,P2		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	$t_{cyc(R)}$	470	–	290	–	360	–	ns
Chip Enable On Time	t_{CE}	310	2000	160	2000	200	2000	ns
Chip Enable to Output Delay	t_{CO}	–	280	–	130	–	180	ns
Read Access Time	t_{acc}	–	300	–	150	–	200	ns

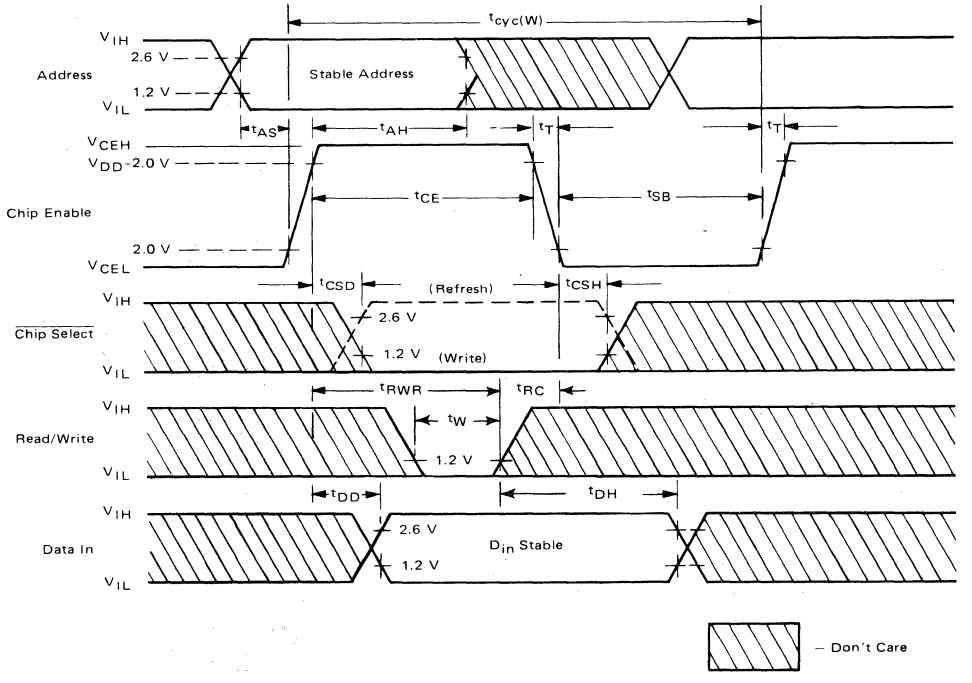
READ CYCLE TIMING



WRITE CYCLE (R/W = V_{IL}, $\overline{CS}$ = V_{IL})
REFRESH CYCLE (R/W = V_{IL}, $\overline{CS}$ = V_{IH})

Characteristic	Symbol	MCM6605AL,P		MCM6605AL1,P1		MCM6605AL2,P2		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	$t_{cyc(W)}$	590	–	390	–	490	–	ns
Chip Enable On Time	t_{CE}	430	2000	260	2000	330	2000	ns
Read-Write Release Time	t_{RWR}	430	2000	260	2000	330	2000	ns
Write Pulse Width	t_W	210	–	140	–	160	–	ns
Read-Write to Chip Enable Separation Time	t_{RC}	0	–	0	–	0	–	ns
Data Delay Time	t_{DD}	–	70	–	70	–	70	ns
Data Hold Time	t_{DH}	50	–	20	–	50	–	ns

WRITE AND REFRESH CYCLE TIMING

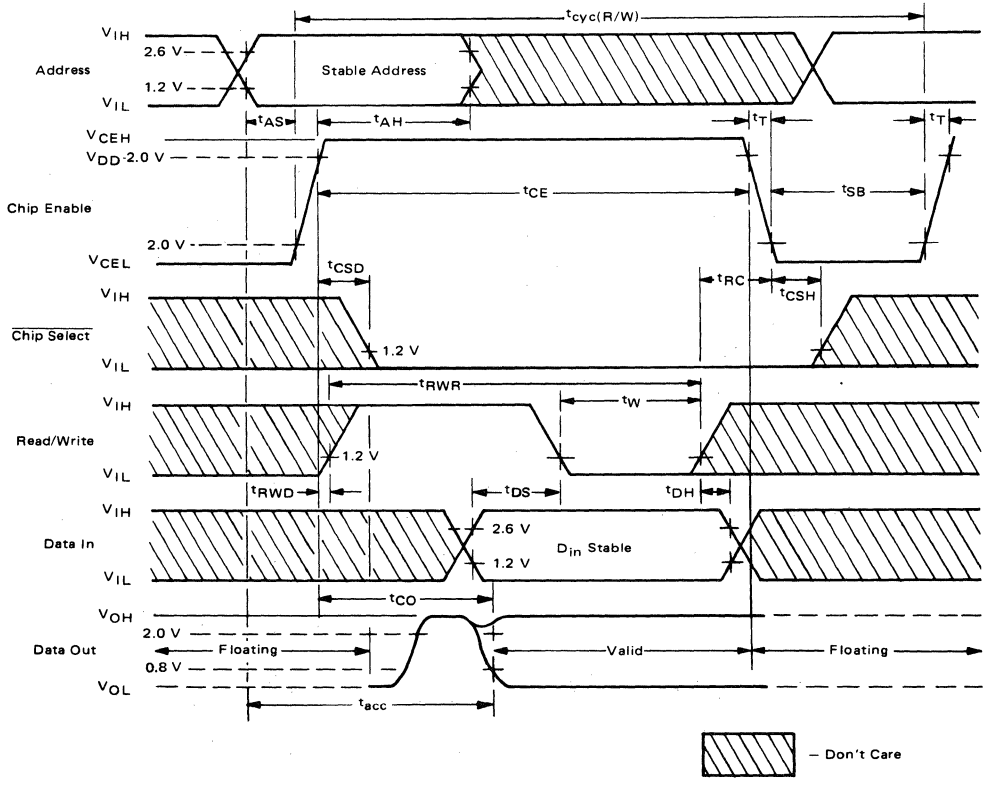


READ-MODIFY-WRITE ($R/\overline{W}$ = $V_{IH} \rightarrow V_{IL}$, $\overline{CS}$ = V_{IL})
READ REFRESH (See Note 1)

Characteristic	Symbol	MCM6605AL,P		MCM6605AL1,P1		MCM6605AL2,P2		Unit
		Min	Max	Min	Max	Min	Max	
Read-Modify-Write Cycle Time	$t_{cyc(R/W)}$	590	–	390	–	490	–	ns
Chip Enable On Time	t_{CE}	430	2000	260	2000	330	2000	ns
Read-Write Release Time	t_{RWR}	430	2000	260	2000	330	2000	ns
Write Pulse Width	t_W	210	–	140	–	160	–	ns
Data Setup Time	t_{DS}	0	–	0	–	0	–	ns
Data Hold Time	t_{DH}	50	–	20	–	50	–	ns
Read-Write to Chip Enable Separation Time	t_{RC}	0	–	0	–	0	–	ns
Chip Enable to Output Delay	t_{CO}	–	280	–	130	–	180	ns
Read Access Time	t_{acc}	–	300	–	150	–	200	ns

Note 1: A read refresh cycle is possible by bringing $\overline{CS}$ high after output data is valid and then bringing R/W low to the write position.

READ MODIFY WRITE TIMING



TYPICAL CHARACTERISTICS CURVES

FIGURE 2 – ACCESS TIME versus V_{DD}

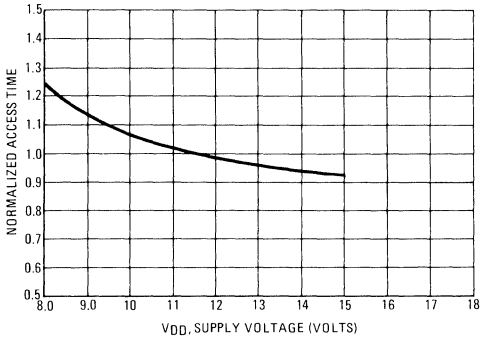


FIGURE 3 – ACCESS TIME versus AMBIENT TEMPERATURE

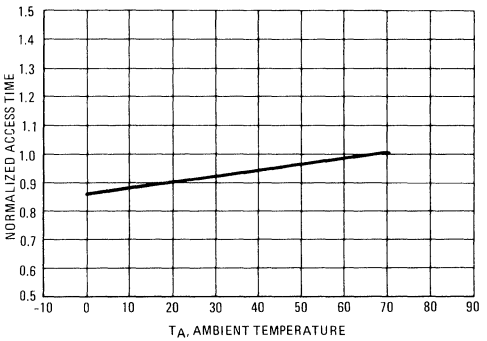


FIGURE 4 – I_{DD} SUPPLY CURRENT versus V_{DD}

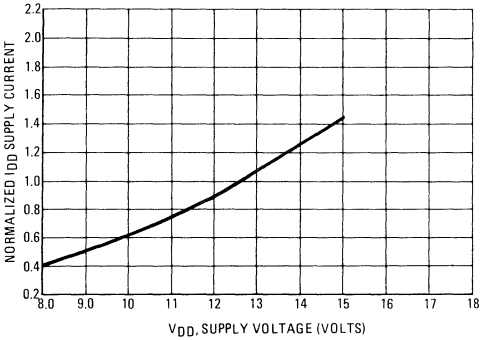


FIGURE 5 – I_{DD} SUPPLY CURRENT versus CYCLE TIME

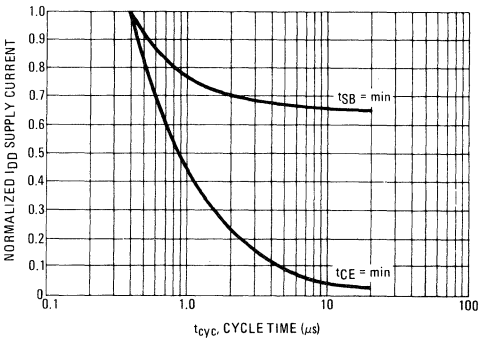


FIGURE 6 – I_{DD} SUPPLY CURRENT versus AMBIENT TEMPERATURE

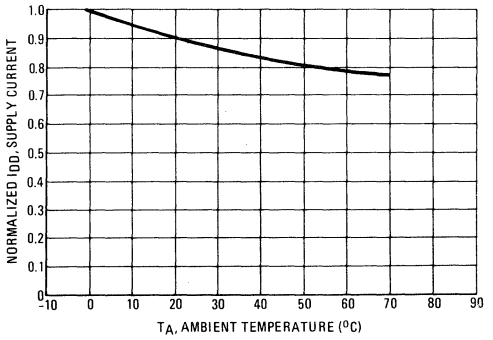
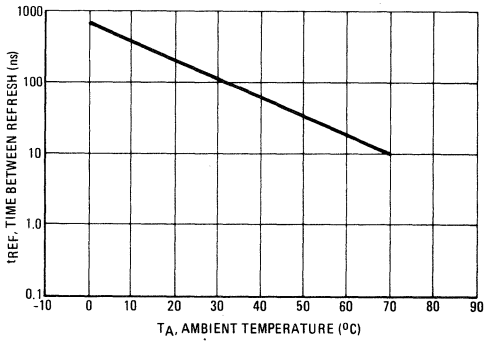


FIGURE 7 – REFRESH TIME versus AMBIENT TEMPERATURE



TYPICAL SUPPLY CURRENT TRANSIENT WAVEFORMS

FIGURE 8 – CHIP ENABLE VOLTAGE

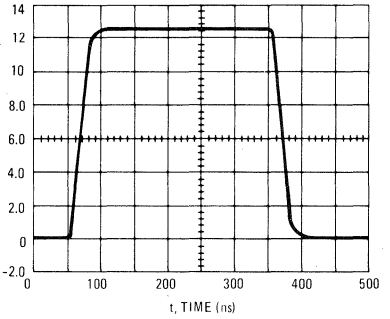


FIGURE 9 – i_{DD} SUPPLY CURRENT

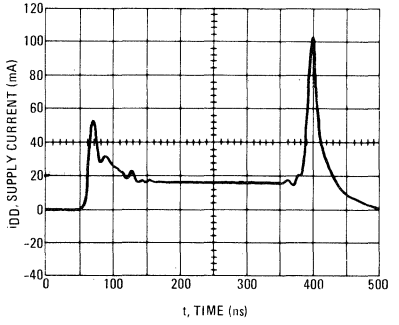


FIGURE 10 – i_{CC} SUPPLY CURRENT

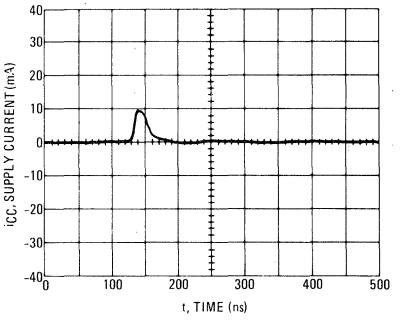


FIGURE 11 – i_{BB} SUPPLY CURRENT

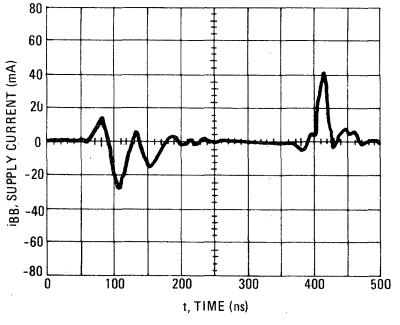
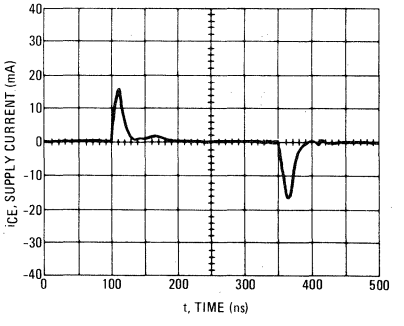
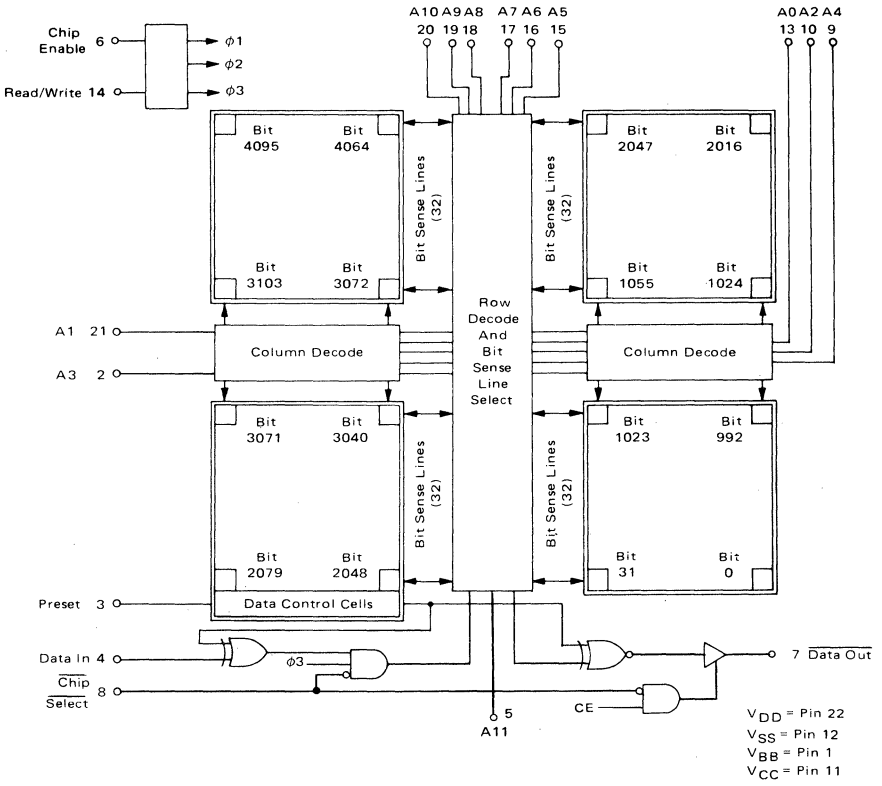


FIGURE 12 – i_{CE} SUPPLY CURRENT



BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

The MCM6605A 4096-bit dynamic RAM uses a three transistor storage cell in an inverting cell configuration. The single high-level clock (Chip Enable) starts an internal three-phase clock generator which controls the read and write functions of the device. The $\phi 1$ signal, which is high when CE is low (standby mode), preconditions the nodes in the dynamic RAM in preparation for a memory cycle. The $\phi 2$ signal, which comes on as CE goes high, is the read control and transfers data from storage onto bit sense lines. The $\phi 3$ signal, which comes after $\phi 2$ only during a write or refresh cycle, transfers data from the bit sense lines back into storage. The $\phi 3$ signal occurs only if the R/W input is low.

To perform a read cycle, CE is brought high to initiate a $\phi 2$ signal and latch the input addresses. The column decoders select one column in each of the four storage quadrants (see the block diagram) and transfers data from storage onto the 128 bit sense lines. The row decoder selects one of these 128 bit sense lines for read and write operations. During the $\phi 2$ signal, the data on this selected bit sense line is Exclusive ORed with the state of the appropriate data control cell to supply the correct output data. After this data is received by the external system, CE may be brought low to the standby position. This assumes that the R/W signal is held high to prevent an internal $\phi 3$ being generated.

To perform a write or refresh operation, CE is brought high and everything is identical to a read operation up until the 128 bit sense lines are charged with the selected columns of stored data. When R/W is brought low (if it is not already there), a $\phi 3$ signal is generated after $\phi 2$ is over. The $\phi 3$ signal takes the data from the 128 bit sense lines and returns it to the 128 storage locations it came from. Because of the design of the memory array, this $\phi 2$-$\phi 3$, read-write operation inverts the data. Therefore, one extra row of memory cells, called data control cells, is used to

keep track of the polarity of stored data in order to be able to correctly recover it. During the write operation, the input data is Exclusive ORed with these control cells before being stored in the array. A refresh cycle does not modify any of the bit sense lines, but simply returns the data (now inverted) into storage.

All timing signals for the MCM6605A are specified around these operations. The following is a brief description of the input pins and relevant timing requirements.

Chip Enable – CE is a single high level clock which initiates all memory cycles. CE can remain low as long as desired for specific applications as long as the 2.0 ms refresh requirements are met.

$\overline{\text{Chip Select}}$ – This signal controls only the I/O buffers. When $\overline{CS}$ is high, the input is disconnected and the output is in the 3-state high-impedance state. A refresh cycle is, therefore, a write cycle with $\overline{CS}$ high. $\overline{CS}$ has no critical timing with respect to any other signal except that there is a finite delay between activation and data out.

Read/Write – When high, R/W inhibits the internal $\phi 3$ signal, thereby keeping the memory from writing. When R/W is low, a $\phi 3$ will occur soon after $\phi 2$ is finished. For a read cycle, R/W should be high within t_{RWD} of CE to insure that a $\phi 3$ does not start. The only timing requirement on the R/W input for writing is a minimum write pulse defined as the overlap of $\overline{CS}$, CE, and R/W. Refresh cycles require that $\overline{CS}$ be high to inhibit the input buffer before a $\phi 3$ occurs. Thus $\overline{CS}$ should be high within t_{CSD} for a refresh cycle, or before R/W goes low for a read-refresh cycle.

Data In – The input data must be valid for a sufficient time to override the data stored on the selected bit sense line. It must remain valid for the "write pulse" defined under Read/Write. Signals on the D_{in} pin are ignored when either $\overline{CS}$ or R/W is high, or CE is low.

Data Out – Output data is inverted from input data and is valid t_{acc} after CE goes high. The data will remain valid as long as CE is high and $\overline{CS}$ remains low. With either CE low or $\overline{CS}$ high, the output is in a high-impedance state. The data output is initially precharged high when CE goes high and is then either discharged to ground or left high depending on the stored data. This precharging followed by valid data occurs regardless of the state of the R/W input, making the write cycle actually a read-write cycle. The output will also try to precharge during a refresh cycle but will be kept at high impedance by the $\overline{CS}$ being high. If $\overline{CS}$ is originally low and is then brought high (within the t_{CSD} specification) the output may start to precharge before being cut off and returned to high impedance.

Addresses – The addresses are latched when CE goes high, and may be removed after an appropriate hold time.

V_{SS} – Circuit ground.

V_{BB} – The reverse bias substrate supply. Forward biasing this supply with respect to V_{SS} will destroy the memory device.

V_{DD} – Positive supply voltage.

V_{CC} – Output buffer supply. This supply goes only to the data output buffer and draws current only when driving an output load high.

Preset – This pin should be tied to ground. During device testing Preset can be used to preset the data control cells to a logic zero. One 200 ns, 12 V pulse will set all 32 cells simultaneously. Preset has no system use; its only purpose is to ensure a good logic level in the control cells after first power up. In system use, this good logic level will come naturally after the first few refresh cycles.

APPLICATIONS INFORMATION

Power Supplies

The MCM6605A is a dynamic RAM which has essentially zero power drain when in the standby (CE low) mode. When operating, the V_{DD} supply may experience transients in the order of 100 mA for a short time (Figure 9). The V_{BB} supply, which has very low dc drain while operating, may see transients of about 40 mA during the edges of CE. Therefore, appropriate bypassing of both supplies is recommended. This bypassing has been simplified by the location of the power supply pins on the corners of the package.

The V_{CC} line supplies only the input leakage of a TTL load on Data Out and should never exceed about 100 μA, presenting little bypassing requirement.

Power dissipation for a system of N chips is much lower than N times the 335 mW typical dissipation for a full speed operating chip. This is because the unselected rows in a memory array card are operating in the standby mode of near zero dissipation. This zero standby power is actually unachievable because of the requirements for refresh. Therefore, power dissipation for an array of N X M chips operating at t_1 cycle time, t_{REF} refresh increment, and maximum CE down time between cycles is:

$$P_D \approx M\left(\frac{490\text{ ns}}{t_1\text{ ns}}\right)335\text{ mW} + (N\text{-}1)\ (M)\left(\frac{15.7}{t_{REF}\ \mu s}\right)335\text{ mW}$$

For a 550-ns-cycle-time, 64 k by 16 system (16 by 16 chip array) with refresh at 2.0 ms, the approximate power dissipation is:

$$P_D \approx 16\left(\frac{490}{550}\right)335 + (15)\ (16)\left(\frac{15.7}{2000}\right)335$$

$$\approx 4775\text{ mW} + 630\text{ mW} = 5.4\text{ W}$$

A similar one megabyte system, eight bytes wide, would have a dissipation of only 24 W. If the low standby power capability were not used, over 600 W would be dissipated.

Refresh

The MCM6605A is refreshed by performing a refresh (or write) cycle on each of the 32 combinations of the least significant address bits (A0-A4) within a 2.0 ms time period. (A5-A11 must remain constant at proper logic levels.) This refresh can be done in a burst mode (32 cycles starting every 2.0 ms) or in a distributed mode where one cycle is done every 62.5 μs.

A refresh abort can be accomplished by treating a refresh cycle as a read-modify-write cycle with $\overline{CS}$ high. This type of cycle can be aborted any time until the R/W signal has been brought low to allow a $\phi 3$ clock to begin.

Non-Volatile Storage

In many digital systems, it is extremely important to retain data during emergencies such as power failure. Unfortunately, however, most random access read/write semiconductor memories such as the MCM6605A are volatile. That is, if power is removed from the semiconductor memory, stored information is lost. Therefore, non-volatility for a specified period of time becomes highly desirable — as a necessity to maintain irreplaceable information or as a convenience to avoid the time consuming and troublesome task of having to reload the memory.

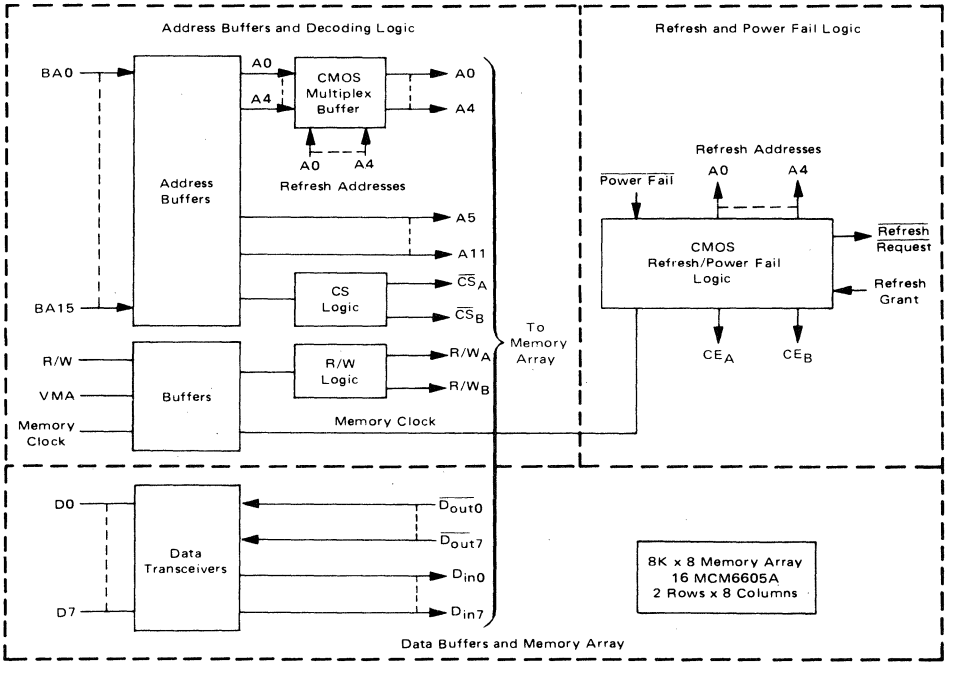
The extremely low standby power dissipation of the MCM6605A makes it ideal for main memory applications requiring battery backup for non-volatility. For example, the MCM6605A can be employed in an 8K byte non-volatile main memory system application for microprocessors. The memory system can be partitioned into three major sections as illustrated in Figure 13. The first section contains the address buffers and the Read/Write and Chip Select decoding logic. The second section consists of the data bus buffering transceivers and the memory array (which consists of 16 MCM6605As) organized into two rows of 4K bytes each.

The third section of the block diagram comprises refresh and control logic for the memory system. This logic interfaces the timing of the refresh handshaking with the microprocessor (MPU) clock circuitry. It handles requests for refresh, the generation of refresh addresses, the synchronization of a $\overline{\text{Power Fail}}$ signal, the multiplexing of the external Memory Clock with the internal clock (used during standby), and the generation of a -5 V supply on the board using a charge-pump method.

The refresh control logic is illustrated in Figure 14. It handles the refreshing of the memory during both operating and standby modes. The timing for this logic is given in Figure 15. Figure 16 gives the memory timing for the standby mode only. Decoding of the memory clock (CE_A and CE_B) and the circuitry to synchronize the $\overline{\text{Power Fail}}$ signal are shown in Figure 17, with the timing given in Figure 18.

The memory device clock (CE_A and CE_B) during standby is created by a monostable multivibrator (MC14528) and buffered from the memory array by three MC14503 buffers in parallel. This clock is multiplexed with the $\overline{\text{Memory Clock}}$ by use of the three-state feature of the

FIGURE 13 – NON-VOLATILE MEMORY SYSTEM BLOCK DIAGRAM



MC14503. The Memory Clock (used during normal operation) is translated to 12 V levels by use of an MC3460 Clock Driver. Decoding of the CE_A and CE_B signals (i.e., clocking only the memory bank addressed) to conserve power is accomplished by the logic within the MC3460.

Since the Power Fail signal will occur asynchronously with both the Memory Clock and the refreshing operation (Refresh Clock), it is necessary to synchronize the Power Fail signal to the rest of the system in order to avoid aborting a memory access cycle or a refresh cycle. An MC14027 dual flip-flop is used as the basic synchronization device. The leading edge of the Refresh Clock triggers a 3 μs monostable multivibrator which is used as a refresh pretrigger. The trailing edge of this pretrigger triggers a 500 ns monostable which creates the CE pulse during standby operation. The 3 μs pretrigger signal is used to set half of the MC14027 flip-flop, the output of which, (B), then inhibits a changeover from the standby to the operating modes (or vice versa). This logic prevents the system from aborting a refresh cycle should the Power Fail signal change states just prior to or during a refresh cycle. The trailing edge of the 500 ns monostable clears the MC14027 flip-flop, enabling the second flip-flop in the package. The state of Power Fail and Power Fail is applied to the K and J inputs of this second flip-flop and is synchronized by clocking with Memory Clock. The outputs of this flip-flop, labeled Bat and Bat, lock the system into the refresh mode and multiplex in the internal clock for standby operation when Bat = "1". The voltage to logic not required for the refresh only mode of operation is removed to conserve power.

By using CMOS for the refresh logic and capacitance drivers, and a low current refresh oscillator, the standby current required for the 8K byte system is extremely small, as noted in Table 1. This low standby current requirement can be easily supplied for several days with standard type +12 V batteries. For more detailed information on this sytem and a large mainframe memory system, see Application Notes AN-732 and AN-740.

FIGURE 14 – REFRESH CONTROL LOGIC

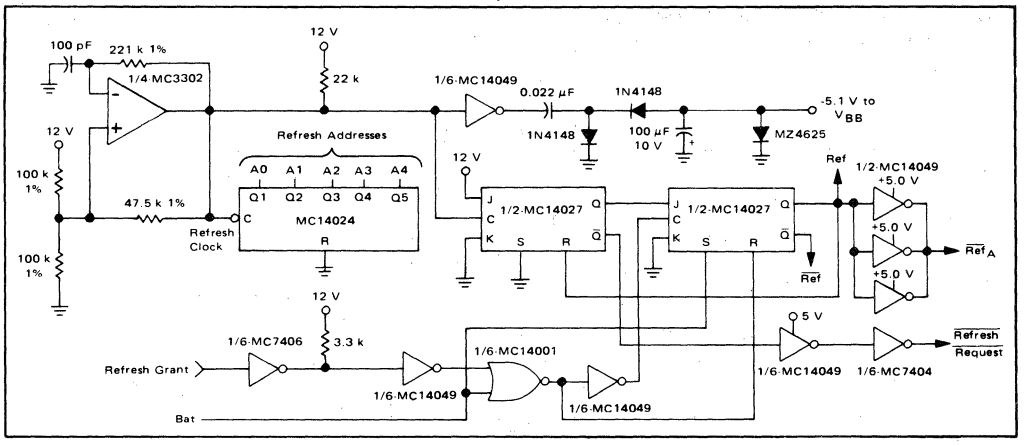


FIGURE 15 – REFRESH TIMING

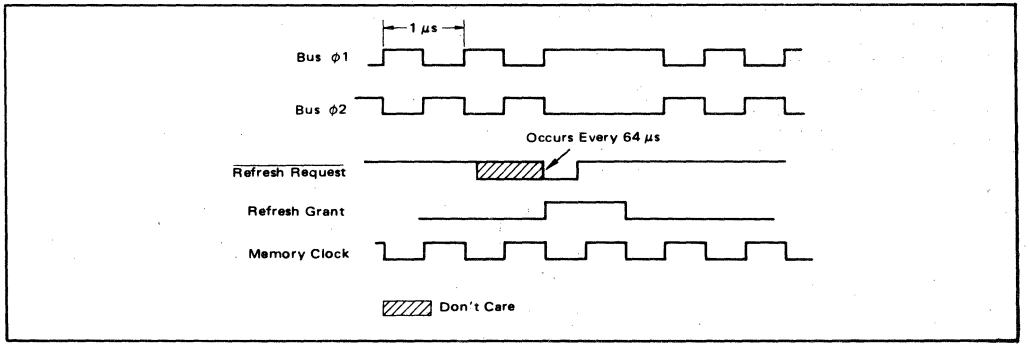


FIGURE 16 – MEMORY TIMING IN STANDBY MODE

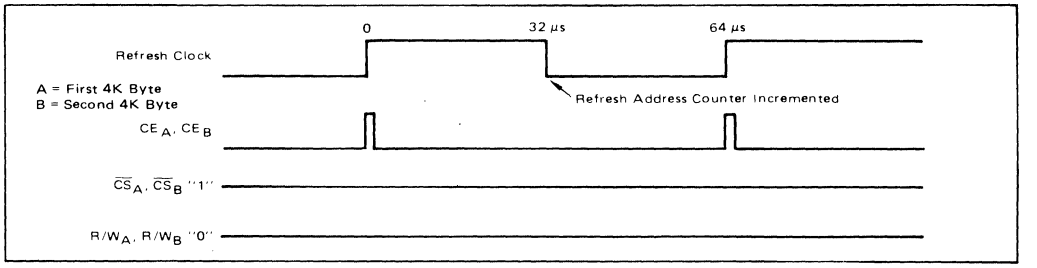


FIGURE 17 – POWER FAIL LOGIC AND CHIP ENABLE DRIVER

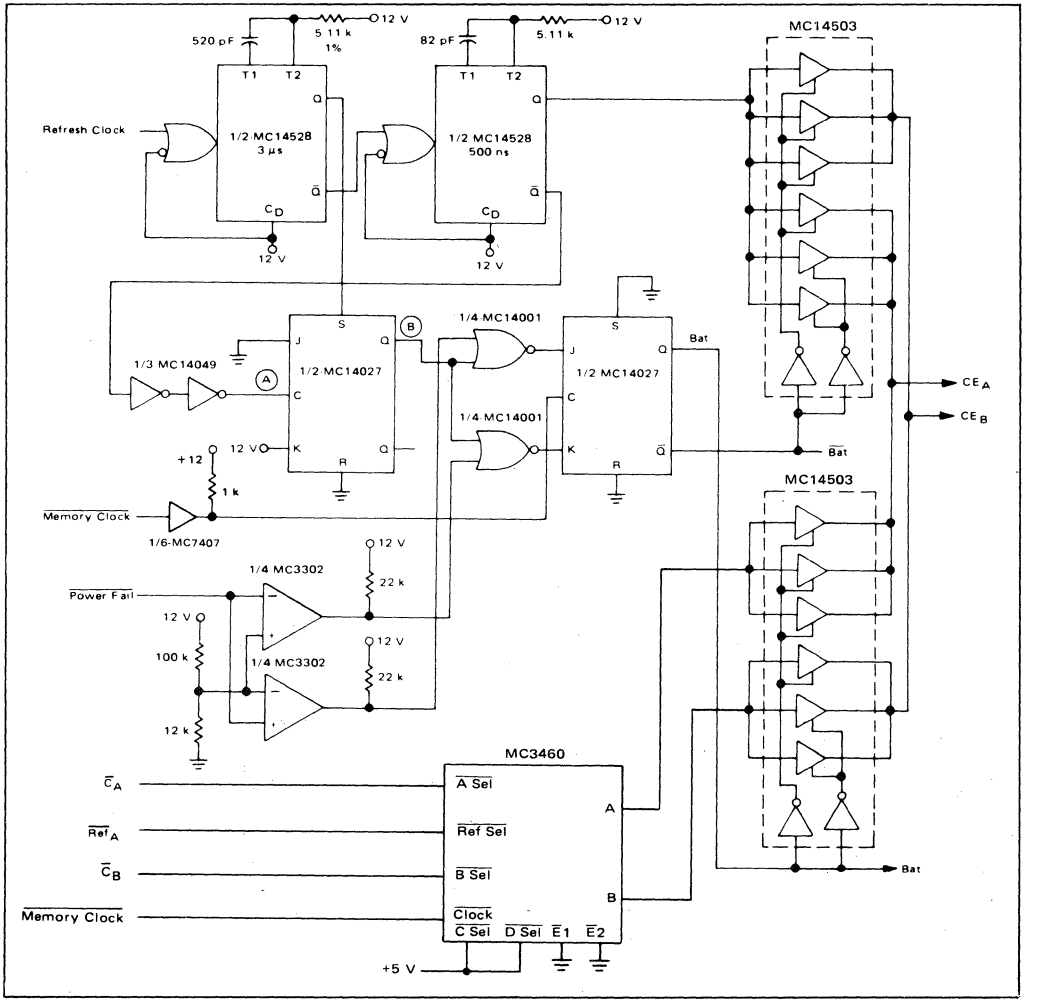


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FIGURE 18 – POWER UP/DOWN SYNCHRONIZATION

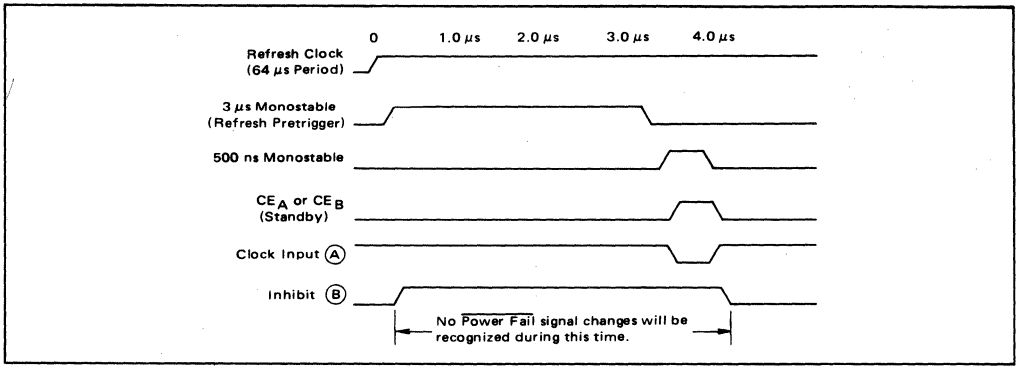
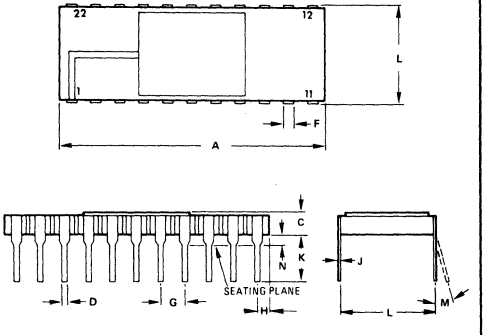


TABLE 1 – STANDBY MODE CURRENT ALLOCATION

Circuit Section	Typical Current
+12 V Current (V_{DD}) for 16 MCM6605A's	5 mA
Charge Pump	3 mA
Comparator	2 mA
Capacitance Drivers	4 mA
Total	14 mA

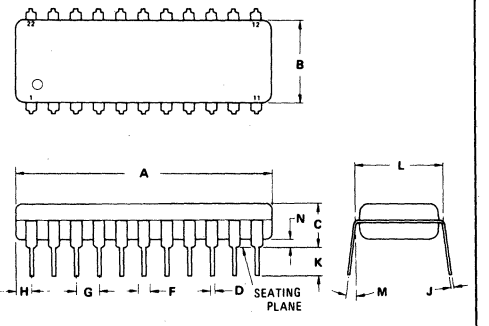
PACKAGE DIMENSIONS



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	27.05	27.94	1.065	1.100
C	2.16	3.68	0.085	0.145
D	0.43	0.58	0.017	0.023
F	1.02 REF		0.040 REF	
G	2.54 BSC		0.100 BSC	
H	0.76	1.78	0.030	0.070
J	0.20	0.30	0.008	0.012
K	3.18	4.45	0.125	0.175
L	9.65	10.67	0.380	0.420
M	–	7°	–	7°
N	0.64	1.27	0.025	0.050

NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.

CERAMIC PACKAGE
CASE 677-03



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	28.83	29.59	1.135	1.165
B	8.64	9.14	0.340	0.360
C	4.57	5.08	0.180	0.200
D	0.36	0.51	0.014	0.020
F	1.02	1.52	0.040	0.060
G	2.41	2.67	0.095	0.105
H	1.78	2.03	0.070	0.080
J	0.20	0.30	0.008	0.012
K	3.05	3.56	0.120	0.140
L	9.65	10.16	0.380	0.400
M	0°	10°	0°	10°
N	0.51	1.02	0.020	0.040

PLASTIC PACKAGE
CASE 708-01

MCM6616L

Product Preview

16,384-BIT DYNAMIC RANDOM ACCESS MEMORY

The MCM6616 is a 16,384-bit high-speed dynamic Random Access Memory designed for high-performance, low-cost applications in mainframe and buffer memories and peripheral storage. Organized as 16,384 one-bit words, this device optimizes speed, power, and density tradeoffs.

By multiplexing row and column address inputs, the MCM6616 requires only seven address lines and permits packaging in Motorola's standard 16-pin dual in-line packages. Complete address decoding is done on chip with address latches incorporated.

All inputs are TTL compatible, and the output is 3-state TTL compatible. The MCM6616 incorporates a one-transistor cell design and dynamic storage techniques, requiring a refresh cycle every 2.0 milliseconds.

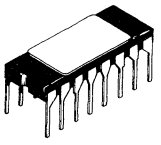
The MCM6616 is a drop-in replacement for the MCM6604, with the CS input of the MCM6604 (pin 13) replaced by an additional address input, A6.

- Organized as 16,384 Words of 1 Bit
- Maximum Access Time = 350 ns
- Minimum Read and Write Cycle Time = 500 ns
- Low Power Dissipation
- TTL Compatible
- 3-State Output
- On-Chip Latches for Address and Data In
- Power Supply Pins on Package Corners for Optimum Layout
- Standard 16-Pin Package
- Drop-In Replacement for MCM6604
- Industry Standard Pinout

MOS

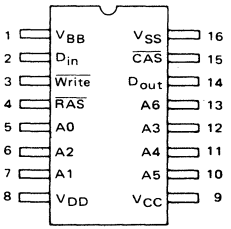
(N-CHANNEL)

16,384-BIT DYNAMIC RANDOM ACCESS MEMORY



CERAMIC PACKAGE

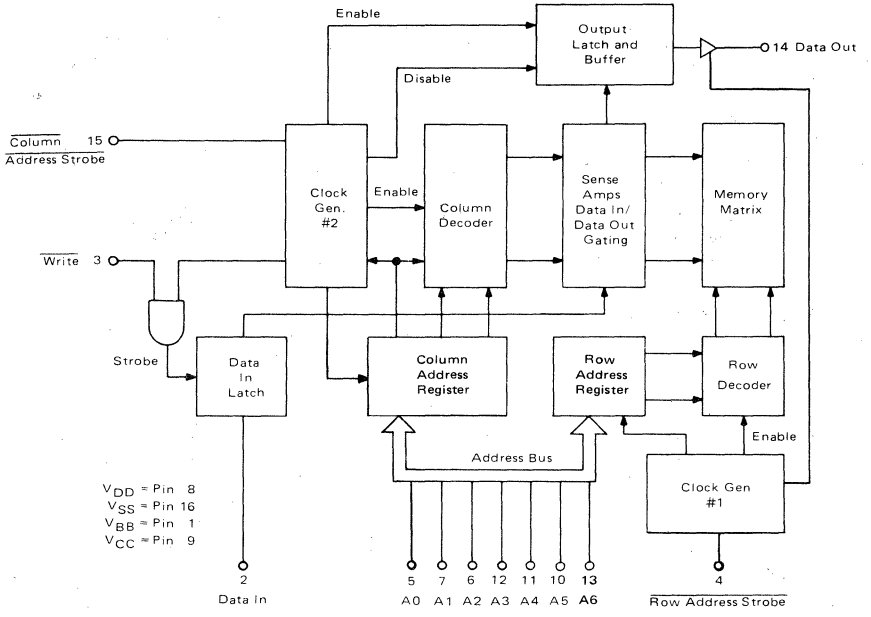
PIN ASSIGNMENT



This is advance information and specifications are subject to change without notice.

2

BLOCK DIAGRAM



MCM14505AL
MCM14505CL
MCM14505CP

McMOS

(LOW-POWER COMPLEMENTARY MOS)

64-BIT (64 x 1) STATIC
RANDOM ACCESS MEMORY

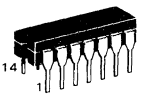
2

64-BIT STATIC RANDOM ACCESS MEMORY

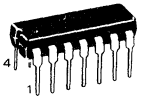
The MCM14505 64-bit random access memory is fully decoded on the chip and organized as 64 one-bit words (64 X 1). Medium speed operation and micropower supply requirements make this device useful for scratch pad or buffer memory applications where power must be conserved or where battery operation is required.

When used with a battery backup, the MCM14505 can be utilized as an alterable read-only memory, allowing the battery to retain information in the memory when the system is powered down, and allowing the battery to charge when power is applied. The micropower requirements of this memory allow quiescent battery operation for great lengths of time without significant discharging.

- Quiescent Power Dissipation = 0.3 μW/package typical at V_{DD} = 10 Vdc
- Noise Immunity = 45% of V_{DD} typical
- Supply Voltage Range = 3.0 Vdc to 18 Vdc (MCM14505AL)
  4.5 Vdc to 16 Vdc (MCM14505CL/CP)
- Single Read/Write Control Line
- Wired-OR Output Capability (3-State Output) for Memory Expansion
- Access Time = 180 ns typical at V_{DD} = 10 Vdc
- Write Cycle Time = 275 ns typical at V_{DD} = 10 Vdc
- Fully Buffered Low Capacitance Inputs



L SUFFIX
CERAMIC PACKAGE
CASE 632



P SUFFIX
PLASTIC PACKAGE
CASE 646

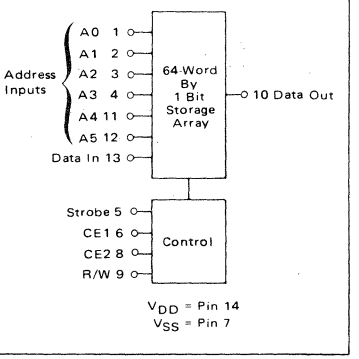
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.i. either V_{SS} or V_{DD})

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 7)

Rating	Symbol	Value	Unit
DC Supply Voltage MCM14505AL MCM14505CL/CP	V_{DD}	+18 to -0.5 +16 to -0.5	Vdc
Input Voltage, All Inputs	V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range MCM14505AL MCM14505CL/CP	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

BLOCK DIAGRAM



2

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{out}	5.0	–	0.01	–	0	0.01	–	0.05	Vdc
		10	–	0.01	–	0	0.01	–	0.05	
		15	–	0.05	–	0	0.05	–	0.25	
"1" Level		5.0	4.99	–	4.99	5.0	–	4.95	–	Vdc
		10	9.99	–	9.99	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.75	–	
Noise Immunity# V	V_{NL}									Vdc
($\triangle V_{out} \leq$ 0.8 Vdc)		5.0	1.5	–	1.5	2.25	–	1.4	–	
($\triangle V_{out} \leq$ 1.0 Vdc)		10	3.0	–	3.0	4.50	–	2.9	–	
($\triangle V_{out} \leq$ 1.5 Vdc)		15	4.5	–	4.5	6.75	–	4.4	–	
($\triangle V_{out} \leq$ 0.8 Vdc)	V_{NH}	5.0	1.4	–	1.5	2.25	–	1.5	–	Vdc
($\triangle V_{out} \leq$ 1.0 Vdc)		10	2.9	–	3.0	4.50	–	3.0	–	
($\triangle V_{out} \leq$ 1.5 Vdc)		15	4.4	–	4.5	6.75	–	4.5	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-0.62	–	-0.50	-1.7	–	-0.35	–	
(V_{OH} = 9.5 Vdc)		10	-0.62	–	-0.50	-0.9	–	-0.35	–	
(V_{OH} = 13.5 Vdc)		15	-1.8	–	-1.5	-3.5	–	-1.1	–	
(V_{OL} = 0.3 Vdc) Sink	I_{OL}	5.0	0.30	–	0.25	0.35	–	0.18	–	mAdc
(V_{OL} = 0.5 Vdc)		10	0.90	–	0.75	1.2	–	0.50	–	
(V_{OL} = 1.5 Vdc)		15	2.2	–	1.7	4.5	–	1.2	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-0.23	–	-0.20	-1.7	–	-0.16	–	
(V_{OH} = 9.5 Vdc)		10	-0.23	–	-0.20	-0.9	–	-0.16	–	
(V_{OH} = 13.5 Vdc)		15	-0.69	–	-0.60	-3.5	–	-0.48	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.20	–	0.15	0.35	–	0.10	–	mAdc
(V_{OL} = 0.5 Vdc)		10	0.60	–	0.50	1.2	–	0.40	–	
(V_{OL} = 1.5 Vdc)		15	0.90	–	0.75	4.5	–	0.60	–	
Input Current	I_{in}	–	–	–	–	0.01	100	–	–	nAdc
Input Capacitance (V_{in} = 0)	C_{in}									pF
Strobe, CE1, D_{in}, A_n		–	–	–	–	4.0	–	–	–	
Read/Write, CE2		–	–	–	–	6.0	–	–	–	
Quiescent Dissipation (AL Device)	P_Q	5.0	–	0.025	–	0.00015	0.025	–	1.5	mW
		10	–	0.10	–	0.0003	0.10	–	6.0	
		15	–	0.30	–	0.001	0.30	–	18	
Quiescent Dissipation (CL/CP Device)	P_Q	5.0	–	0.25	–	0.00015	0.25	–	7.5	mW
		10	–	1.0	–	0.0003	1.0	–	30	
		15	–	3.0	–	0.001	3.0	–	90	
Power Dissipation**†	P_D	5.0	P_D = (6.4 mW/MHz) f + P_Q							mW
		10	P_D = (25.6 mW/MHz) f + P_Q							
		15	P_D = (57.8 mW/MHz) f + P_Q							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
†For dissipation at different external load capacitance (C_L) use the formula:

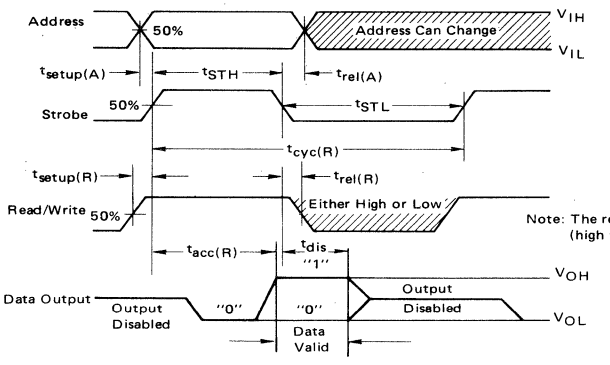
$$P_T(C_L) = P_D + 1 \times 10^{-3} (C_L - 15\ pF)\ V_{DD}{}^2 f$$

where: P_T, P_D in mW (per package), C_L in pF, V_{DD} in Vdc, and f in MHz is input frequency.
**The formula given is for the typical characteristics only.

SWITCHING CHARACTERISTICS (T_A = 25°C, t_r, tf = 20 ns)

Characteristic	Symbol	V_{DD}	Typ All Types	Max AL Device	Max CL/CP Device	Unit
Minimum Strobe Down Time	t_{STL}	5.0	100	400	500	ns
		10	50	100	125	
		15	75	80	95	
Address Setup Time	$t_{setup(A)}$	5.0	-100	200	300	ns
		10	-40	80	120	
		15	-25	60	90	
Data Setup Time	$t_{setup(D)}$	5.0	70	140	200	ns
		10	25	50	75	
		15	20	40	55	
Read Setup Time	$t_{setup(R)}$	5.0	90	180	270	ns
		10	20	40	60	
		15	15	30	45	
Write Setup Time	$t_{setup(W)}$	5.0	80	275	400	ns
		10	25	75	100	
		15	11	55	75	
Address Release Time	$t_{rel(R)}$	5.0	15	50	75	ns
		10	10	15	25	
		15	5.0	10	20	
Data Hold Time	$t_{hold(D)}$	5.0	0	35	50	ns
		10	0	10	15	
		15	0	7.5	10	
Read Release Time	$t_{rel(R)}$	5.0	-90	0	0	ns
		10	-25	0	0	
		15	-10	0	0	
Write Release Time	$t_{rel(W)}$	5.0	5.0	0	0	ns
		10	10	0	0	
		15	30	0	0	
Read Cycle Time	$t_{cyc(R)}$	5.0	500	650	750	ns
		10	200	300	400	
		15	150	225	300	
Write Cycle Time	$t_{cyc(W)}$	5.0	440	600	700	ns
		10	275	400	550	
		15	200	300	415	
Read Access Time (C_L = 15 pF)	$t_{acc(R)}$	5.0	400	550	650	ns
		10	180	270	350	
		15	110	200	260	
Output Disable Delay (10% Output Change into 1.0 kΩ Load)	t_{dis}	5.0	200	400	600	ns
		10	80	160	200	
		15	60	120	150	

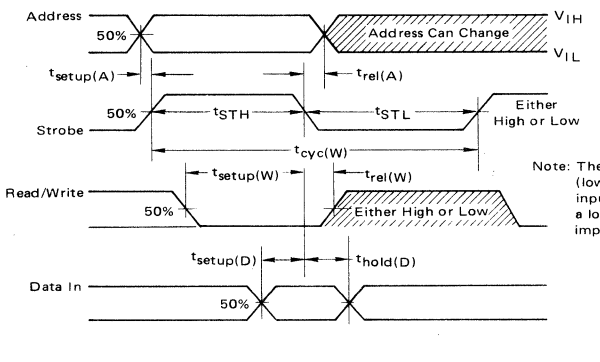
FIGURE 1 – READ CYCLE TIMING DIAGRAM



$t_{STH\ min} = t_{cyc(R)\ max} - t_{STL\ min}$

Note: The read/write input can be maintained at a logical "1" (high voltage) during a read cycle.

FIGURE 2 – WRITE CYCLE TIMING DIAGRAM



$t_{STH\ min} = t_{cyc(W)\ max} - t_{STL\ min}$

Note: The read/write input can be maintained at a logic "0" (low voltage) during a write cycle. If the read/write input is maintained at a logic "0" while the strobe is a logic "1", then the output data will be disabled (high impedance) during the write cycle.

FIGURE 3 – MAXIMUM STROBE PULSE WIDTH versus TEMPERATURE

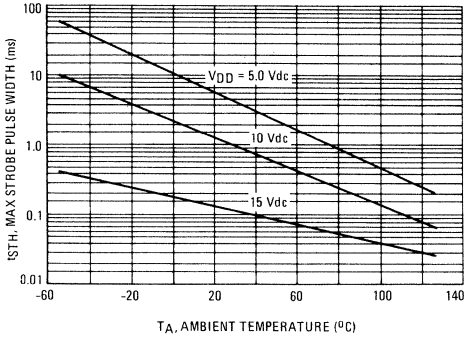


FIGURE 4 – TYPICAL READ ACCESS TIME versus LOAD CAPACITANCE

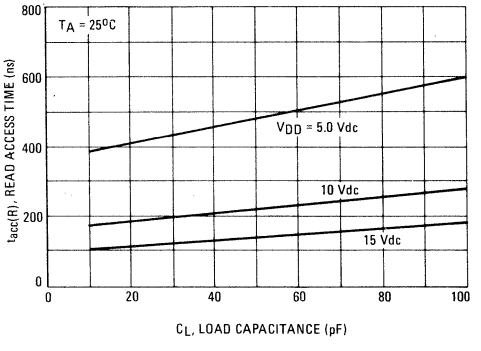
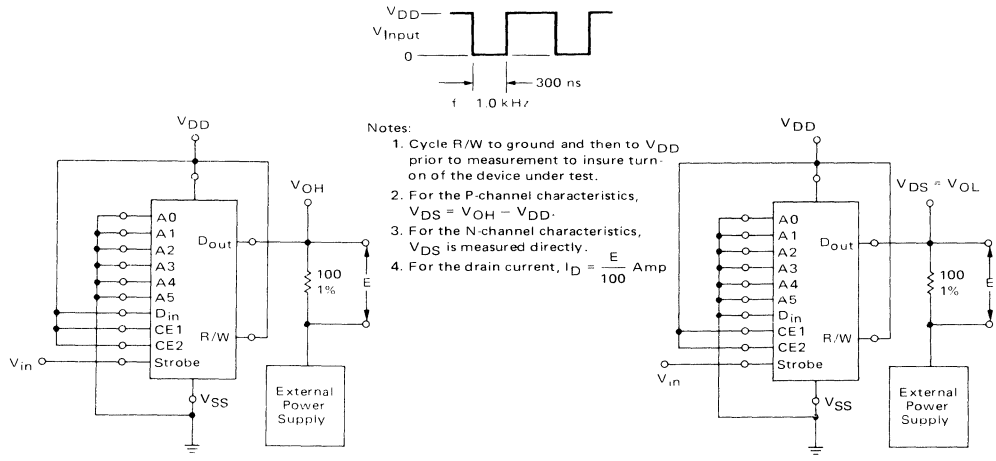
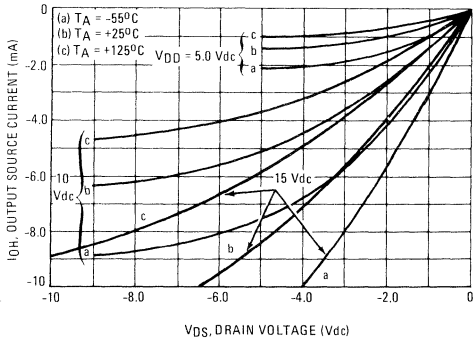


FIGURE 5 – TYPICAL OUTPUT SOURCE CAPABILITY versus TEMPERATURE

FIGURE 6 – TYPICAL OUTPUT SINK CAPABILITY versus TEMPERATURE





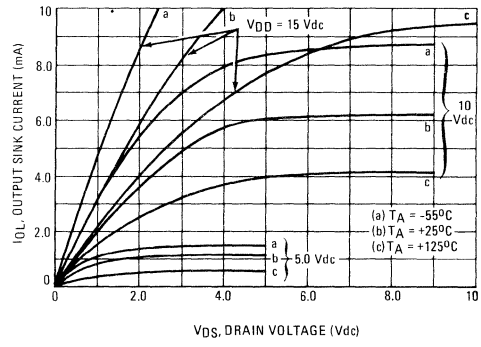
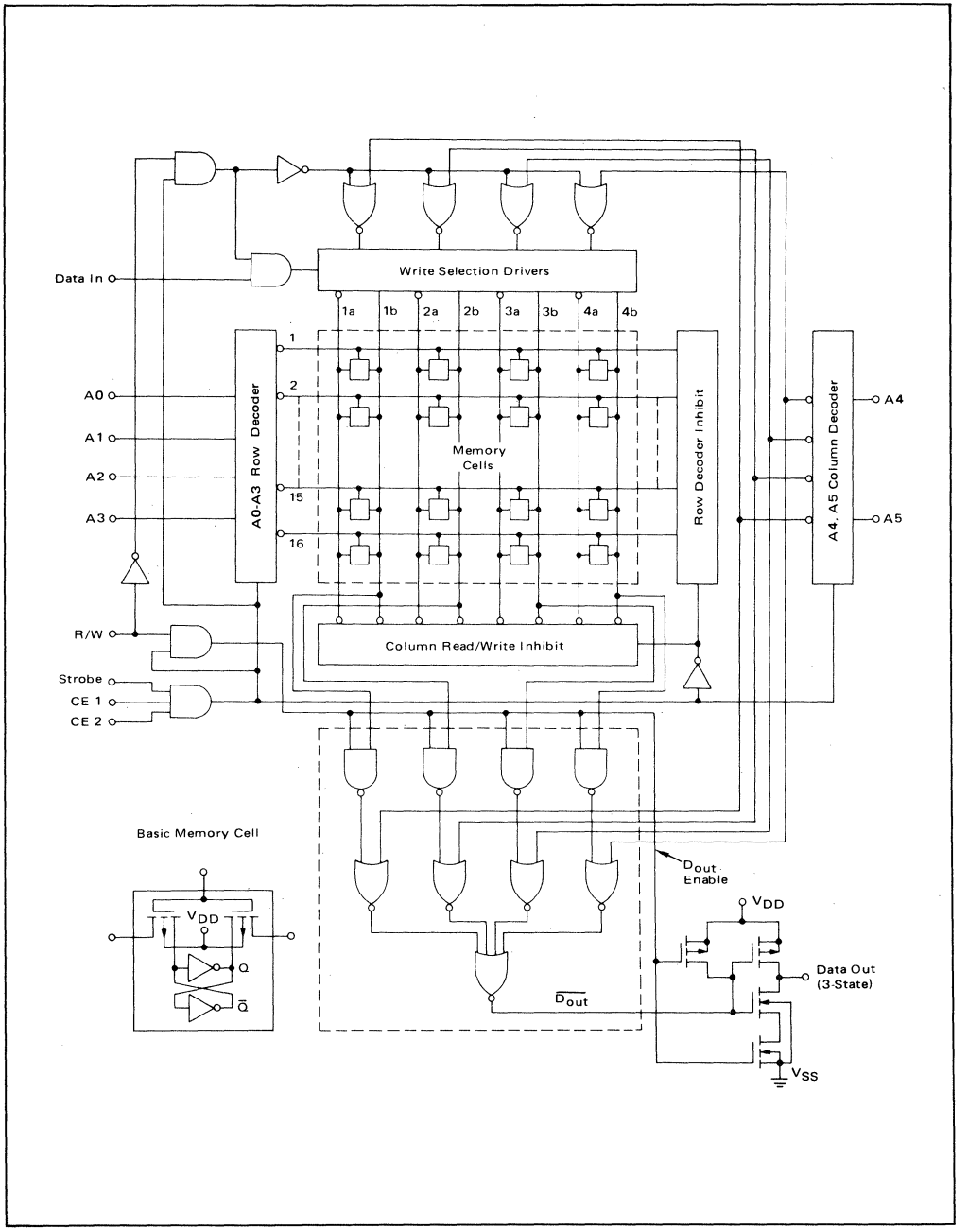


FIGURE 7 – FUNCTIONAL CIRCUIT DIAGRAM



OPERATING CHARACTERISTICS

In considering the operation of the MCM14505 CMOS memory, refer to the functional circuit diagram of Figure 7 and timing diagrams shown in Figures 1 and 2. The basic memory cell is a cross-coupled flip-flop consisting of two inverter gates and two P-channel devices for read/write control. The push-pull cell provides high speed as well as low power.

During a read cycle, when the strobe line is high the write selection drivers are disabled and the data from the selected row is available on columns 1b, 2b, 3b, and 4b. The A4 and A5 address bits are decoded to select output data from one of the four columns. The output data is available on the data output pin only when the strobe and read/write lines are high simultaneously and after the read access time, $t_{acc(R)}$, has occurred (see Figure 1). Note that the output is initially disabled and always goes to the logic "0" state (low voltage) before data is valid. The output is in the high-impedance state (disabled) when the strobe line or the R/W line is in the low state. The memory is strobed for reading or writing only when the strobe, CE1, and CE2 are high simultaneously. The R/W line can be a dc voltage during a read or write cycle and need not be pulsed, as shown in the timing diagrams. For this case the R/W line should be a logic "1" (high) for reading and a logic "0" for writing.

When the strobe line is high, the column read/write inhibit gates and the row decoder inhibit gates are disabled, the selected row is in the low state, and the unselected 15 rows retain their logic "1" level due to the row capacitance that exists when the row decoder inhibit gates are disabled. This capacitive storage mechanism requires a maximum strobe width (see Figure 3) equal to the junction reverse bias RC time constant. When the strobe is returned to a logic "0" the rows are forced to V_{DD} by the row decoder inhibit gates (pullup devices). Similarly the column read/write inhibit gates (pulldown devices) force the column lines to a logic "0" state.

Two column lines are associated with each memory cell in order to write into the cell. The write selection drivers are enabled when the R/W line is a logic "0" and the strobe line is a logic "1". The input data is written into the column selected by the column decoder. For instance, if a "1" is to be written in the memory cell associated with row 1 and column 1, then row 1 would be enabled (logic "0") while column 1b is forced high and column 1a is forced low by the write selection drivers. If a logic "0" is to be written into the cell, then column 1a is forced high and 1b is forced low. The data that is retained in the memory cell is the data that was present on the data input pin at the moment the strobe goes low when R/W is low, or when R/W goes high when the strobe is high.

APPLICATIONS INFORMATION

Figure 8 shows a 256-word by n-bit static RAM memory system The outputs of four MCM14505 devices are tied together to form 256 words by 1 bit. Additional bits are attained by paralleling the inputs in groups of four. Memories of larger words can be attained by decoding the most significant bits of the address and ANDing them with the strobe input.

Fan-in and fan-out of the memory is limited only by speed requirements. The extremely low input and output leakage current (100 nA maximum) keep the output voltage levels from changing significantly as more outputs are tied together. With the output levels independent of fan-out, most of the power supply range is available as logic swing, regardless of the number of units wired together. As a result, high noise immunity is maintained under all conditions.

Power dissipation is 0.1 μW per bit at a 1.0-kHz rate for a 5.0-volt power supply, while the static power dissipation is 2.0 nW per bit. This low power allows non-volatile information storage when the memory is powered by a small standby battery.

Figure 9 shows an optional standby power supply circuit for making a CMOS memory "non-volatile". When the usual power fails, a battery is used to sustain operation or maintain stored information. While normal power supply voltage is present, the battery is trickle-charged through a resistor which sets the charging rate. V_B is the sustaining voltage, and V^+ is the ordinary voltage from a power supply. V_{DD} connects to the power pin on the memory. Low-leakage diodes are recommended to conserve battery power.

The memory system shown in Figure 8 can be interfaced directly with the other devices in the McMOS family. No external components are required.

At the inputs to the CMOS memory, TTL devices can interface directly if an open-collector logic gate such as the MC7407 is used as shown in Figure 10. Driver circuits are not required since the input capacitance is low (4.0 to 6.0 pF). The address, data, and read/write inputs do not need to be fast since they can be changed for the duration when the strobe pulse is low, t_{STL} (see Figures 1 and 2). For high-speed operation, a push-pull driver should be used if more than five strobe inputs must be driven at one time. One circuit of the type shown in Figure 10 can be used for every ten strobe inputs.

Figures 11, 12, and 13 show methods of interfacing the memory output to TTL logic at various memory voltages. If a V_{DD} of 5.0 volts is used for slow-speed, low-power applications, one transistor and one resistor must be used (Figure 11). The MCM14505AL will drive one low-power TTL gate directly.

If a V_{DD} of 10 volts is used, the output of the memory device can fan out to two low-power TTL gates (Figure 12a) or to a discrete transistor (Figure 12b). The discrete transistor circuit provides higher speed and/or high fan-out. A pulldown resistor at the base of the transistor is not needed for fast turn-off because of the push-pull output of the memory. Turn-on time of the transistor is much faster in Figure 12b since the voltage rise is only 0.75 volt. The low output capacitance of the MCM14505 means that several outputs can be wire-ORed without significantly degrading performance. The read access time is increased by only 20 ns typically for 16 outputs tied together when Figure 12b is used.

Five low-power TTL gates can be driven from the memory output if a V_{DD} of 15 volts is used (Figure 13a). Figure 13b shows the interface if a discrete transistor is used. The 1.0 kilohm resistor in the base is required to insure that not more than 10 mA flows through the output as listed in the maximum ratings. If a 2.0 kilohm collector resistor is used (fan-out = 3), the turn-on time of the transistor is only slightly faster than in the circuit shown in Figure 12b due to the lower output impedance when V_{DD} = 15 volts. The voltage at the memory data output has to rise to only 1.3 volts to insure driving a fan-out of three TTL devices.

If a 510-ohm collector resistor is used, 20 TTL loads may be driven. The read access time is increased about 20 ns when four memory outputs are tied together since the output voltage must rise to 3.7 volts before the transistor can sink the full I_{OL} for a fan-out of 20 TTL devices. Almost any NPN transistor with a minimum beta of 15 can be used for the interface shown in Figures 11, 12 and 13.

The high source current from the push-pull output stage of the MCM14505 makes for a simpler interface circuit since a low source current memory requires a differential comparator to achieve high-speed operation.

FIGURE 8 – CMOS 256-WORD BY n-BIT STATIC READ/WRITE MEMORY

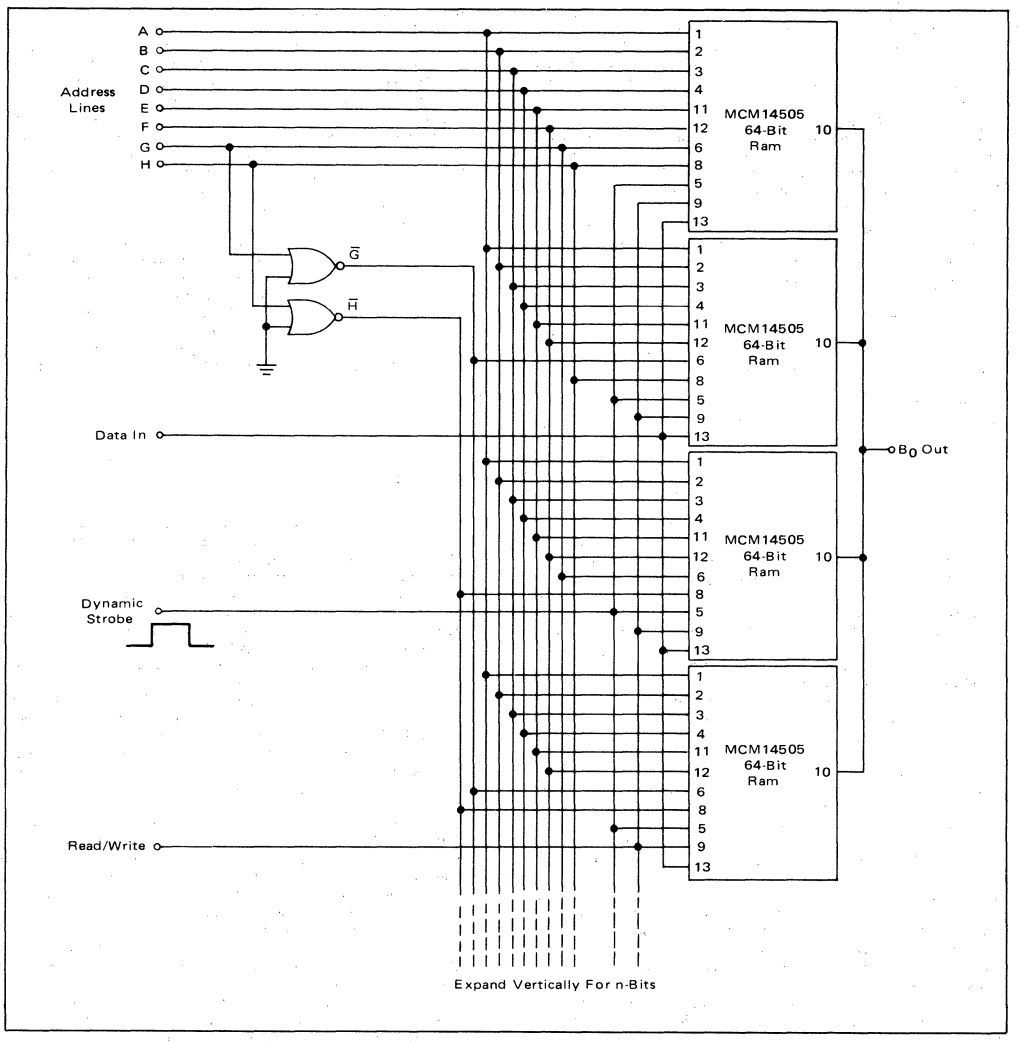


FIGURE 9 – STAND BY BATTERY CIRCUIT

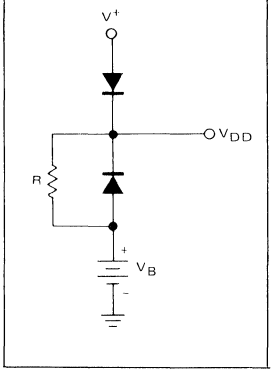


FIGURE 10 – TTL TO CMOS INTERFACE

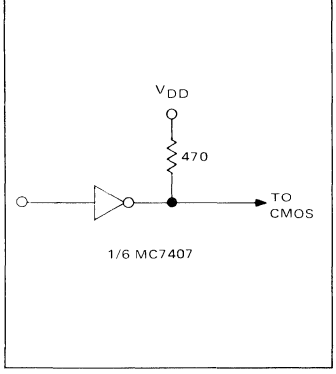


FIGURE 11 – CMOS-TO-TTL INTERFACE FOR V_{DD} = 5.0 V

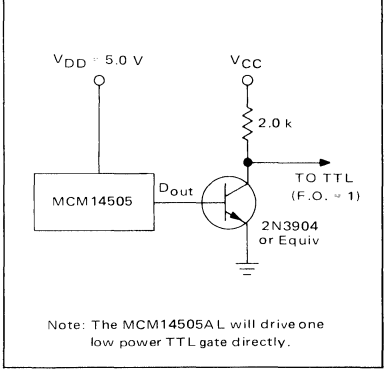


FIGURE 12 – CMOS-TO-TTL INTERFACE FOR V_{DD} = 10 V

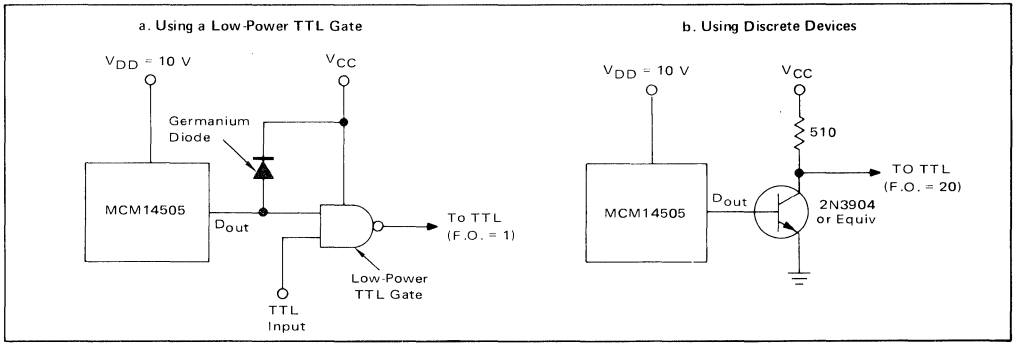
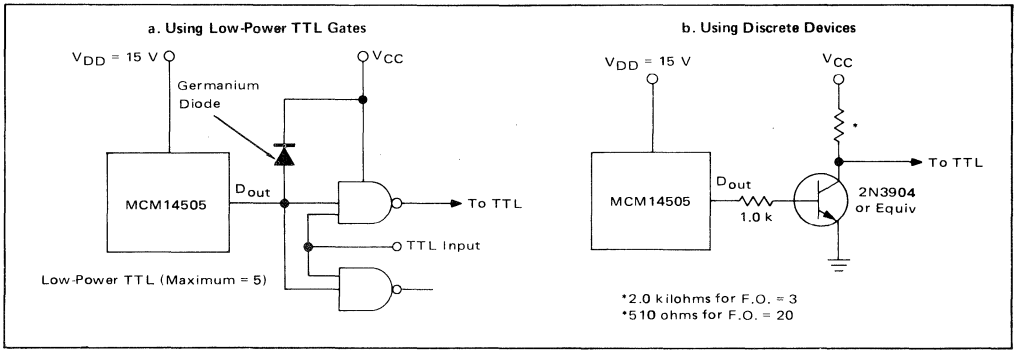


FIGURE 13 – CMOS-TO-TTL INTERFACE FOR V_{DD} = 15 V



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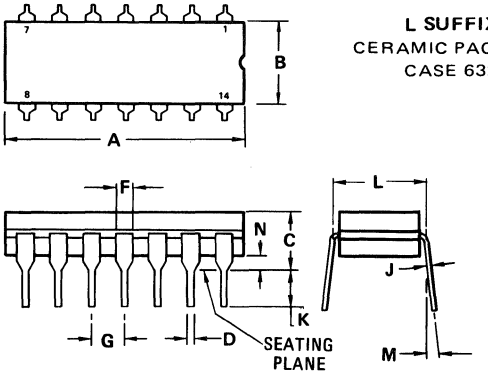
PACKAGE DIMENSIONS



L SUFFIX
CERAMIC PACKAGE
CASE 632

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	16.8	19.9	0.660	0.785
B	5.59	7.11	0.220	0.280
C	–	5.08	–	0.200
D	0.381	0.584	0.015	0.023
F	0.77	1.77	0.030	0.070
G	2.54 BSC		0.100 BSC	
J	0.203	0.381	0.008	0.015
K	2.54	–	0.100	–
L	7.62 BSC		0.300 BSC	
M	–	15°	–	15°
N	0.51	0.76	0.020	0.030
P	–	8.25	–	0.325

All JEDEC dimensions and notes apply.
TO-116
CASE 632-02

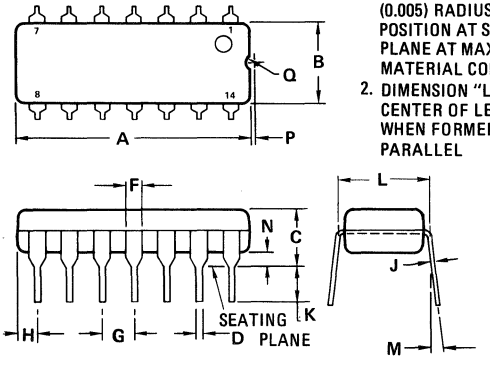
NOTES:
1. DIM "A" AND "B" DO NOT INCLUDE GLASS RUN-OUT.
2. DIM "L" TO INSIDE OF LEADS (MEASURED 0.51 mm (0.020) BELOW BODY)

Devices packaged in Case 632 fall within one of the given sets of dimensions. Further identification is available upon request.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	19.05	19.94	0.750	0.785
B	6.10	7.49	0.240	0.295
C	–	5.08	–	0.200
D	0.38	0.58	0.015	0.023
F	1.40	1.77	0.055	0.070
G	2.54 BSC		0.100 BSC	
H	1.91	2.29	0.075	0.090
J	0.20	0.38	0.008	0.015
K	2.54	4.06	0.100	0.160
L	7.49	8.89	0.295	0.350
M	–	15°	–	15°
N	0.51	1.02	0.020	0.040

CASE 632-04

P SUFFIX
PLASTIC PACKAGE
CASE 646



NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL

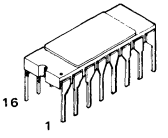
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	18.16	18.80	0.715	0.740
B	6.10	6.60	0.240	0.260
C	4.06	4.57	0.160	0.180
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.32	1.83	0.052	0.072
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.37	7.87	0.290	0.310
M	–	10°	–	10°
N	0.51	1.02	0.020	0.040
P	0.13	0.38	0.005	0.015
Q	0.51	0.76	0.020	0.030

MCM14537AL
MCM14537CL

McMOS

(LOW-POWER COMPLEMENTARY MOS)

256-BIT (256 x 1) STATIC RANDOM ACCESS MEMORY



CERAMIC PACKAGE
CASE 690

256-BIT STATIC RANDOM ACCESS MEMORY

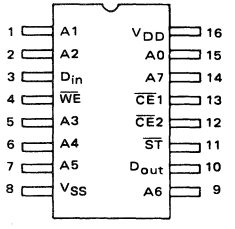
The MCM14537 is a static random access memory (RAM) organized in a 256 x 1-bit pattern and constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. The circuit consists of eight address inputs (A_n), one data input (D_{in}), one write enable input ($\overline{WE}$), one strobe input ($\overline{ST}$), two chip enable inputs ($\overline{CE}_n$), and one data output (D_{out}).

Using both chip enable inputs as extensions of the address inputs, a 10-bit address scheme may be employed. Four MCM14537 devices may be used to comprise a 1024-bit memory without additional address decoding. The $\overline{CE}$ and $\overline{ST}$ inputs are dissimilary designed to enable usage of the memory in a variety of applications. An output latch is provided on the chip for storing the data read or written into memory, making a data-out storage register unnecessary. The CE inputs control the data output for third-state (high output impedance) or active operation which makes the memory very useful in a bus oriented system. When $\overline{CE2}$ is high the chip is fully disabled. When $\overline{CE1}$ is high the output is in the third state but data can be written into the output latch during a read cycle. This enables the use of the memory for fast reading by using the $\overline{CE1}$ input to enable the latch. The memory is also designed so that dc signals can operate the memory with no maximum pulse width required on the $\overline{CE}$ and $\overline{ST}$ lines.

Medium speed operation and micropower operation make the device useful in scratch pad and buffer applications where micropower or battery operation and high noise immunity are required.

- Quiescent Power Dissipation = 2.5 μW/package typical @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typical
- Wired-OR Output Capability (3-state output) for Memory Expansion
- Output Data Latch Eliminates Need for Storage Buffer
- Access Time = 700 ns typical @ V_{DD} = 10 Vdc
- Fully Decoded and Buffered

PIN ASSIGNMENT



MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8)

Rating	Symbol	Value	Unit
DC Supply Voltage MCM14537AL MCM14537CL	V_{DD}	+18 to -0.5 +16 to -0.5	Vdc
Input Voltage, All Inputs	V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature – MCM14537AL Range – MCM14537CL	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{out}	5.0	–	0.01	–	0	0.01	–	0.05	Vdc
		10	–	0.01	–	0	0.01	–	0.05	
		15	–	0.05	–	0	0.05	–	0.25	
"1" Level		5.0	4.99	–	4.99	5.0	–	4.95	–	Vdc
		10	9.99	–	9.99	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.75	–	
Noise Immunity#	V_{NL}									Vdc
($\Delta V_{out} \leq 0.8$ Vdc)		5.0	1.5	–	1.5	2.25	–	1.4	–	
($\Delta V_{out} \leq 1.0$ Vdc)		10	3.0	–	3.0	4.50	–	2.9	–	
($\Delta V_{out} \leq 1.5$ Vdc)		15	4.5	–	4.5	6.75	–	4.4	–	
($\Delta V_{out} \leq 0.8$ Vdc)	V_{NH}	5.0	1.4	–	1.5	2.25	–	1.5	–	Vdc
($\Delta V_{out} \leq 1.0$ Vdc)		10	2.9	–	3.0	4.50	–	3.0	–	
($\Delta V_{out} \leq 1.5$ Vdc)		15	4.4	–	4.5	6.75	–	4.5	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-0.62	–	-0.50	-1.7	–	-0.35	–	
(V_{OH} = 9.5 Vdc)		10	-0.62	–	-0.50	-0.9	–	-0.35	–	
(V_{OH} = 13.5 Vdc)		15	-1.8	–	-1.5	-3.5	–	-1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.50	–	0.40	0.78	–	0.28	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.1	–	0.90	2.0	–	0.65	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	7.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-0.23	–	-0.20	-1.7	–	-0.16	–	
(V_{OH} = 9.5 Vdc)		10	-0.23	–	-0.20	-0.9	–	-0.16	–	
(V_{OH} = 13.5 Vdc)		15	-0.69	–	-0.60	-3.5	–	-0.48	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.23	–	0.20	0.78	–	0.16	–	mAdc
(V_{OL} = 0.5 Vdc)		10	0.60	–	0.50	2.0	–	0.40	–	
(V_{OL} = 1.5 Vdc)		15	1.8	–	1.5	7.8	–	1.2	–	
Input Current	I_{in}	–	–	–	–	10	–	–	–	pAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	–	–	–	pF
Quiescent Dissipation (AL Device)	P_Q	5.0	–	0.5	–	0.0025	0.5	–	9.0	mW
		10	–	2.0	–	0.010	2.0	–	36	
		15	–	6.0	–	0.023	6.0	–	100	
Quiescent Dissipation (CL/CP Device)	P_Q	5.0	–	2.5	–	0.0025	0.5	–	39	mW
		10	–	10	–	0.010	2.0	–	100	
		15	–	30	–	0.023	6.0	–	300	
Power Dissipation**† (Dynamic plus Quiescent) (C_L = 15 pF)	P_D	5.0	$P_D = (6.4\ mW/MHz)\ f + P_Q$							mW
		10	$P_D = (25.6\ mW/MHz + p_Q$							
		15	$P_D = (57.6\ mW/MHz)\ f + P_Q$							

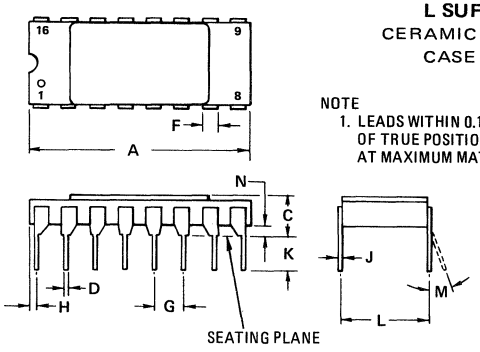
*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
†For dissipation at different external load capacitance (C_L) use the formula:

$$P_T(C_L) = P_D + 1 \times 10^{-3} (C_L - 15\ pF)\ V_{DD}{}^2 f$$

where: P_T, P_D in mW (per package), C_L in pF, V_{DD} in Vdc, and f in MHz is input frequency.
**The formula given is for the typical characteristics only.

PACKAGE DIMENSIONS

L SUFFIX
CERAMIC PACKAGE
CASE 690



NOTE
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	18.80	19.23	0.740	0.757
C	2.67	3.94	0.105	0.155
D	0.41	0.51	0.016	0.020
F	1.14	1.40	0.045	0.055
G	2.54 BSC		0.100 BSC	
H	0.51	0.71	0.020	0.028
J	0.20	0.31	0.008	0.012
K	3.56	4.83	0.140	0.190
L	7.62 BSC		0.300 BSC	
M	–	10°	–	10°
N	0.64	1.14	0.025	0.045

CASE 690-07

SWITCHING CHARACTERISTICS* (T_A = 25°C)

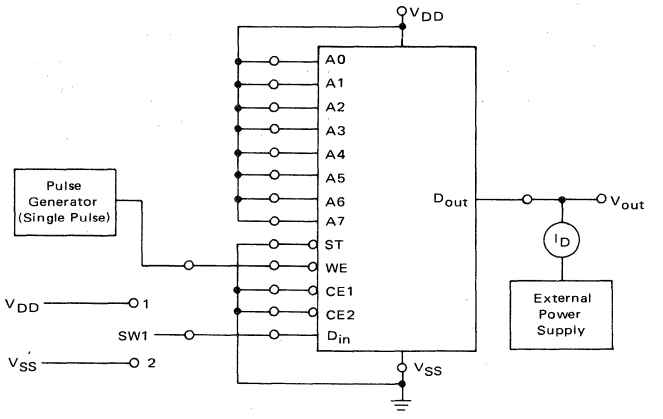
Characteristic	Figure	Symbol	V_{DD}	Min AL Device	Min CL/CP Device	Typ All Types	Max AL Device	Max CL/CP Device	Unit
Output Rise Time (C_L = 15 pF)	3	t_r							ns
t_r = (3.0 ns/pF) C_L + 25 ns			5.0	--	--	70	175	200	
t_r = (1.5 ns/pF) C_L + 12 ns			10	–	–	35	75	100	
t_r = (1.1 ns/pF) C_L + 8.0 ns			15	–	–	25	55	80	
Output Fall Time (C_L = 15 pF)	3	t_f							ns
t_f = (1.5 ns/pF) C_L + 47 ns			5.0	–	–	70	175	200	
t_f = (0.75 ns/pF) C_L + 24 ns			10	–	–	35	75	110	
t_f = (0.55 ns/pF) C_L + 17 ns			15	–	–	25	55	80	
Read Access Time from $\overline{ST}$ or $\overline{CE}2$ (C_L = 15 pF)	4,5	$t_{acc(R)}$							ns
t_{acc} = (1.4 ns/pF) C_L + 2480 ns			5.0	450	400	2500	4000	6000	
t_{acc} = (0.7 nspF) C_L + 690 ns			10	200	150	700	1400	2000	
t_{acc} = (0.5 ns/pF) C_L + 393 ns			15	150	115	400	1050	1500	
Output Enable Delay from $\overline{CE}1$ or $\overline{CE}2$	5,6	$t_{acc(CE_n)}$	5.0	80	70	300	600	900	ns
			10	30	25	100	200	300	
			15	23	20	70	150	225	
Setup Time from A_n to $\overline{ST}$ or $\overline{CE}2$	4,5,6,7	$t_{setup(A)}$	5.0	–	–	600	1200	1800	ns
			10	–	–	200	400	600	
			15	–	–	140	300	450	
Hold Time from A_n to $\overline{ST}$ or $\overline{CE}2$	4,5,6,7	$t_{hold(A)}$	5.0	–	–	200	400	600	ns
			10	–	–	80	160	240	
			15	–	–	55	120	180	
Data Hold Time	7	$t_{hold(D)}$	5.0	–	–	480	960	1400	ns
			10	–	–	160	320	500	
			15	–	–	110	240	375	
Data Setup Time	7	$t_{setup(D)}$	5.0	–	–	1200	2400	3600	ns
			10	–	–	600	1200	1800	
			15	–	–	420	900	1350	
$\overline{Write\ Enable}$ Hold Time	7	$t_{hold(\overline{WE})}$	5.0	–	–	50	100	150	ns
			10	–	–	20	40	60	
			15	–	–	15	30	45	
$\overline{Write\ Enable}$ Setup Time	7	$t_{setup(\overline{WE})}$	5.0	–	–	240	480	720	ns
			10	–	–	80	160	240	
			15	–	–	55	120	180	
$\overline{Write\ Enable}$ to D_{out} Disable**	4	$t_{\overline{WE}}$	5.0	–	–	240	480	720	ns
			10	–	–	80	160	240	
			15	–	–	55	120	180	
$\overline{Strobe}$ or $\overline{CE}2$ Pulse Width When Reading	4,5,6	PW(R)	5.0	–	–	450	900	1350	ns
			10	–	–	150	300	450	
			15	–	–	100	225	340	
$\overline{Strobe}$, $\overline{CE}1$ or $\overline{CE}2$ Pulse Width When Writing	7	PW(W)	5.0	–	–	1200	1800	2400	ns
			10	–	–	600	840	1260	
			15	–	–	420	630	945	
Write Recovery Time,(C_L = 15 pF)	4	$t_{R(W)}$							ns
t_W = (1.4 ns/pF) C_L + 219 ns			5.0	80	70	240	480	720	
t_W = (0.7 ns/pF) C_L + 70 ns			10	30	25	80	160	240	
t_W = (0.5 ns/pF) C_L + 47.5 ns			15	25	20	55	120	180	
$\overline{CE}1$ or $\overline{CE}2$ to D_{out} Disable Delay**	6	$t_{\overline{CE}_n}$	5.0	80	70	300	600	900	ns
			10	30	25	100	200	300	
			15	25	20	70	150	225	
Read Setup Time	4,5	$t_{setup(R)}$	5.0	–	–	-100	-30	0	ns
			10	–	–	-40	-10	0	
			15	–	–	-30	-7.5	0	
Read Hold Time	4,5	$t_{hold(R)}$	5.0	–	–	180	360	540	ns
			10	–	–	60	180	240	
			15	–	–	45	135	180	
Read Cycle Time	4,5	$t_{cyc(R)}$	5.0	–	–	2500	4000	6000	ns
			10	–	–	700	1400	2100	
			15	–	–	500	1050	1575	
Write Cycle Time	7	$t_{cyc(W)}$	5.0	–	–	1400	3400	4800	ns
			10	–	–	700	1400	2100	
			15	–	–	500	1050	1575	

*The formula given is for the typical characteristics only.

**10% output change into a 1.0 kΩ load.

2

FIGURE 1 – TYPICAL OUTPUT SOURCE AND SINK CURRENT CHARACTERISTICS TEST CIRCUIT



Input	Output Source Characteristics	Output Sink Characteristics
$\overline{WE}$	Pulse Once	Pulse Once
D_{in}	SW1 in Position 1	SW1 in Position 2
V_{GS}	$-V_{DD}$	V_{DD}
V_{DS}	$V_{out} - V_{DD}$	V_{out}

FIGURE 2 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORMS

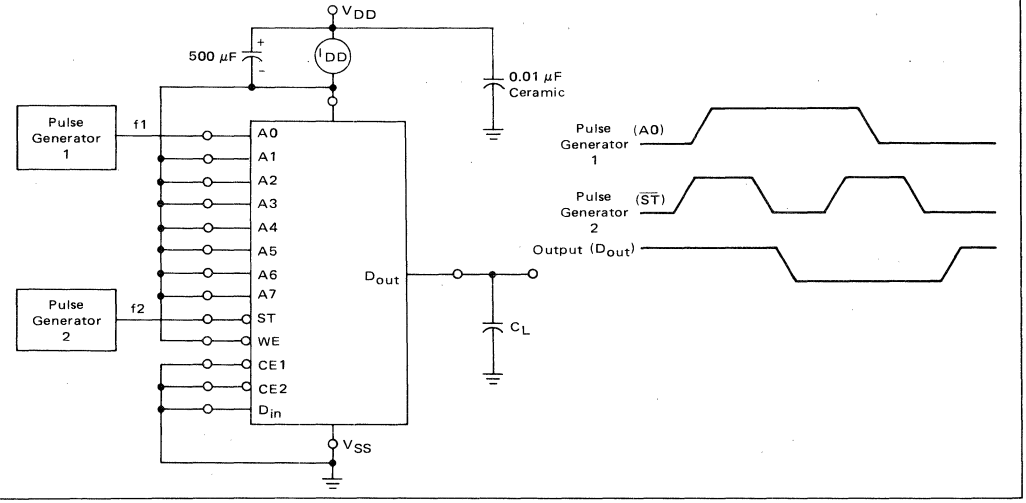


FIGURE 3 – AC TEST CIRCUIT

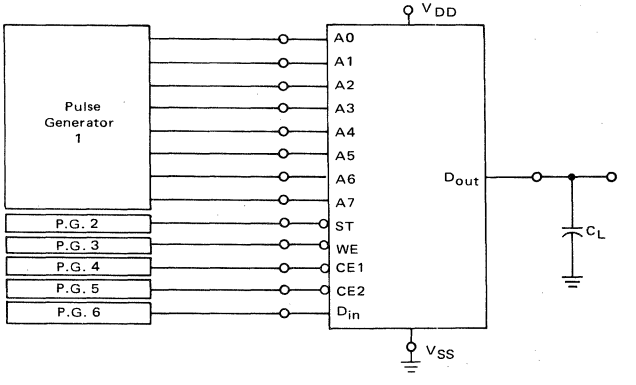
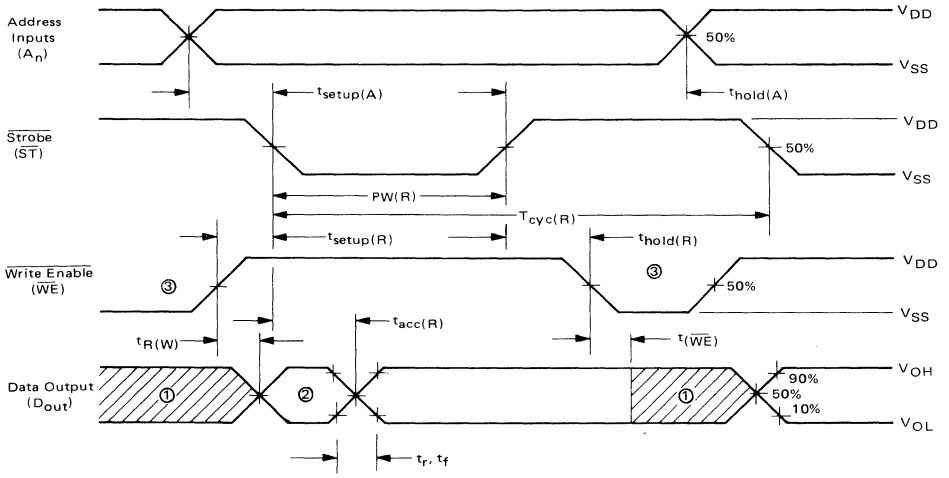
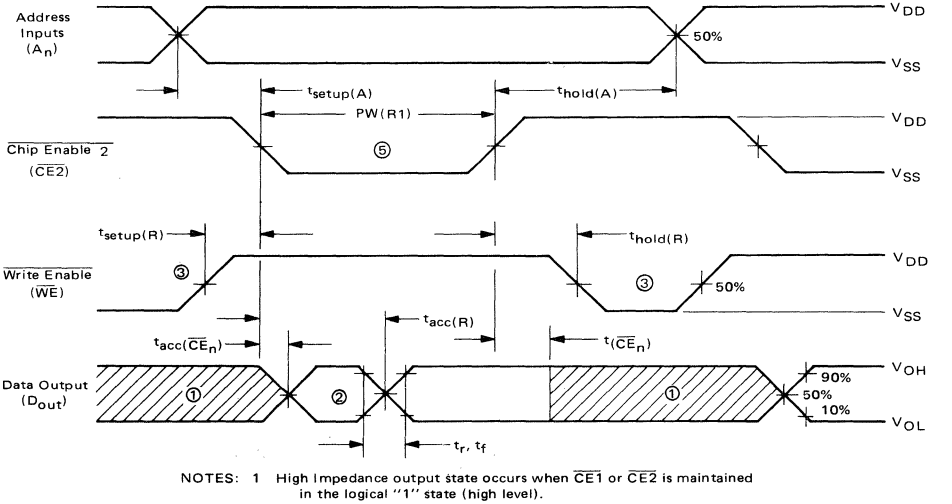


FIGURE 4 – READ CYCLE WAVEFORMS UTILIZING STROBE-TO-ACCESS MEMORY



NOTES:
1. High impedance output state occurs when $\overline{WE}$ is maintained as a logical "0" (low level).
2. The output momentarily displays data from the previous state.
3. For read operation, $\overline{WE}$ may be maintained at a logical "1" (high level) during the complete cycle.
4. $\overline{CE1}$ and $\overline{CE2}$ are maintained at a logical "0" state (low level).
5. All input rise and fall times are 20 ns.

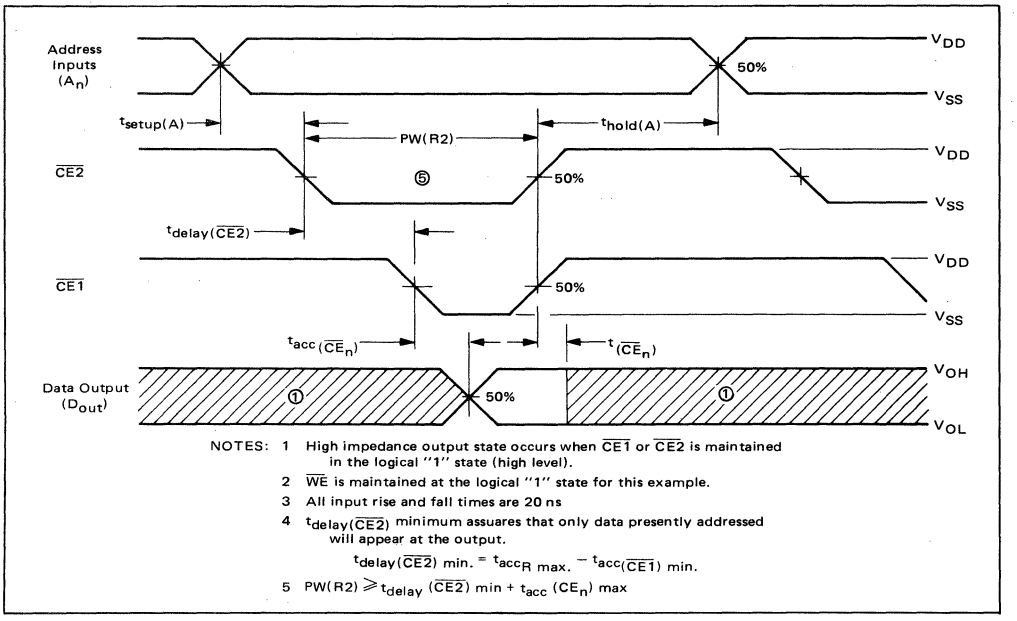
FIGURE 5 – READ CYCLE WAVEFORMS UTILIZING $\overline{CE2}$ FOR ACCESS MEMORY



NOTES:
1. High Impedance output state occurs when $\overline{CE1}$ or $\overline{CE2}$ is maintained in the logical "1" state (high level).
2. The output momentarily displays data from the previous state.
3. For read operation, $\overline{WE}$ may be maintained at a logical "1" (high level) during the complete cycle.
4. All input rise and fall times are 20 ns.
5. PW (R1) $\geqslant t_{acc}$ (R) max

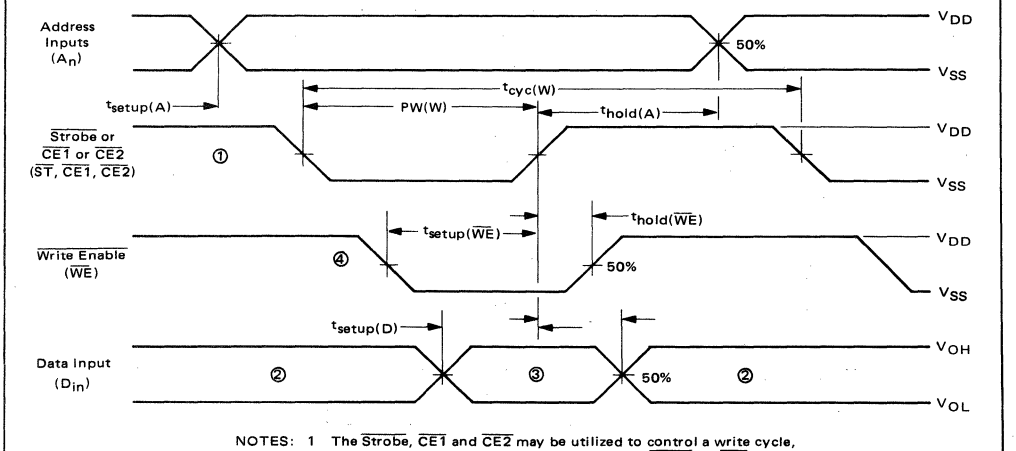
2

FIGURE 6 – READ CYCLE WAVEFORMS UTILIZING $\overline{CE1}$ AND $\overline{CE2}$ TO ACCESS MEMORY



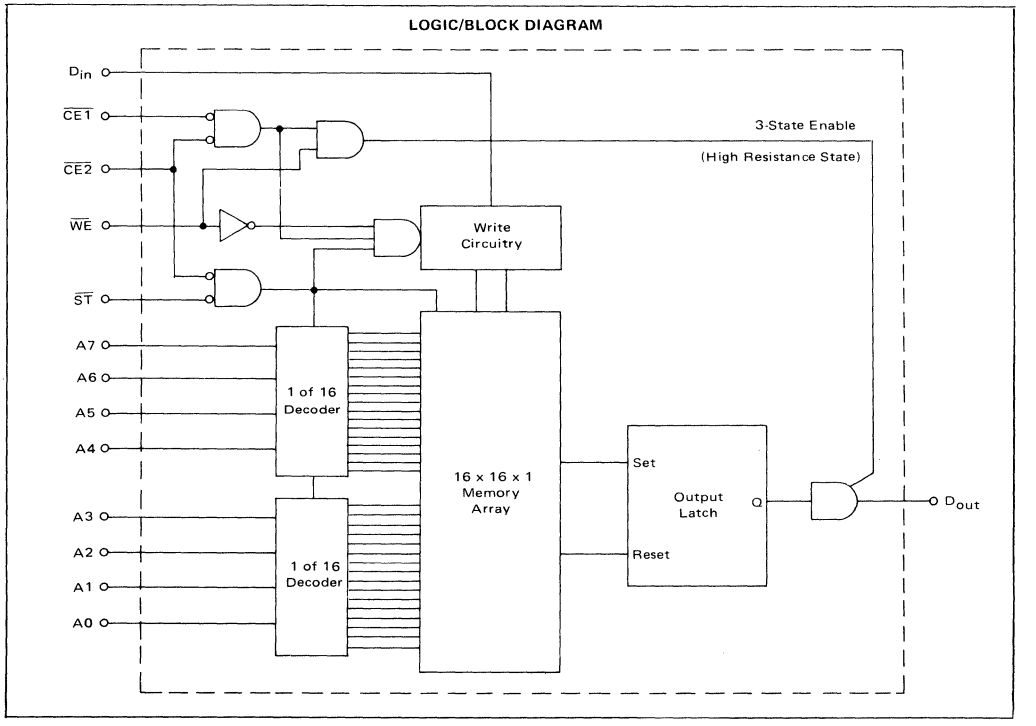
NOTES:
1. High impedance output state occurs when $\overline{CE1}$ or $\overline{CE2}$ is maintained in the logical "1" state (high level).
2. $\overline{WE}$ is maintained at the logical "1" state for this example.
3. All input rise and fall times are 20 ns
4. $t_{delay(\overline{CE2})}$ minimum assuares that only data presently addressed will appear at the output.
   $t_{delay(\overline{CE2})}$ min. = t_{acc_R} max. − $t_{acc(\overline{CE1})}$ min.
5. PW(R2) $\geqslant t_{delay}$ $(\overline{CE2})$ min + t_{acc} (CE_n) max

FIGURE 7 – WRITE CYCLE WAVEFORMS



NOTES:
1. The Strobe, $\overline{CE1}$ and $\overline{CE2}$ may be utilized to control a write cycle, however, during changes of address either Strobe or $\overline{CE2}$ must be in the logical "1" state (high level).
2. Data input logic level is don't care during the indicated intervals.
3. Data input logic level must remain fixed.
4. Write Enable may be maintained as a logical "0" during the write cycle.
5. All input rise and fall times are 20 ns.

LOGIC/BLOCK DIAGRAM

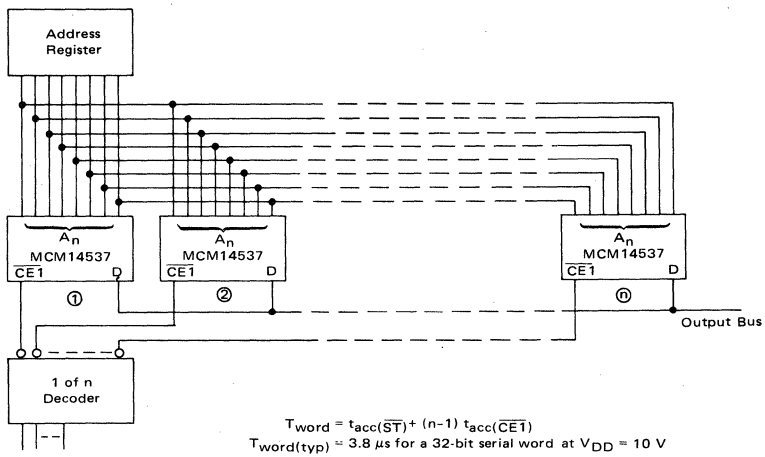


FUNCTION	$\overline{CE1}$	$\overline{CE2}$	$\overline{ST}$	$\overline{WE}$	D_{in}	D_{out}	COMMENTS
Address changing valid	X	X	1	X	X	R/A	D_{out} will be active if $\overline{CE1}$ and $\overline{CE2}$ = "0" and $\overline{WE}$ = "1".
	X	1	X	X	X	R	$\overline{CE2}$ = "1", fully disables internal logic and output.
Address changing not valid	X	0	0	X	X	R/A	Changing address in this mode may result in altered data.
D_{out} disabled in high resistance state	1	X	X	X	X	R	$\overline{CE1}$ = "1" disables write cycle and D_{out}.
	X	1	X	X	X	R	The chip is fully disabled.
	X	X	X	0	X	R	$\overline{WE}$ = "0" enables writing into memory if $\overline{CE1}$, $\overline{CE2}$, and $\overline{ST}$ = "0".
D_{out} enabled in active state	0	0	X	1	X	A	If $\overline{ST}$ = "1", the output stores and reads the previous data from or written into memory.
Read addressed memory location into output latch.	0	0	0	1	X	A	The output reads the present contents that are addressed.
	1	0	0	1	X	R	The addressed location is read into output latch with output in the "R" state.
Disable reading from memory	X	1	X	X	X	R	Address changing can take place in this condition.
	X	X	1	X	X	R/A	
Write into memory	0	0	0	0	A	R	D_{in} is written into memory and into the output latch
Write disabled	1	X	X	X	X	R	$\overline{WE}$ = "1" is a read enable.
	X	1	X	X	X	R	$\overline{WE}$ = "0" is a write enable.
	X	X	1	X	X	R/A	
	X	X	X	1	X	R/A	

R = High resistance state at D_{out}
A = An active level of either V_{SS} or V_{DD}
R/A = An R or A condition depending on the don't care condition
X = Don't care condition (must be in the "1" or "0" state)
1 = A high level at V_{DD}
0 = A low level at V_{SS}

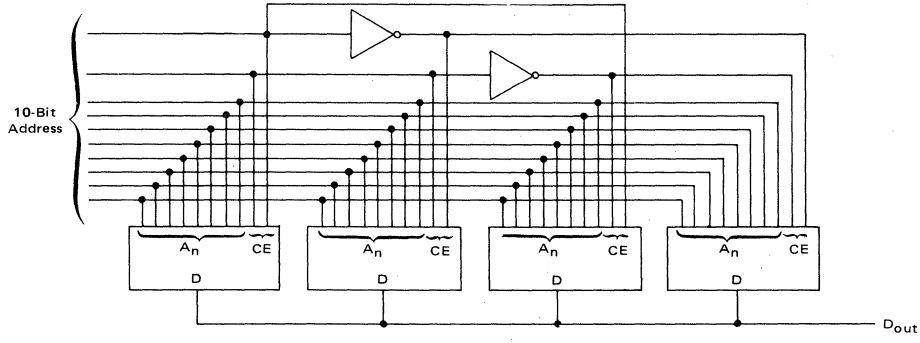
2

TYPICAL APPLICATION FOR SERIAL WORDS UTILIZING BUS TECHNIQUES

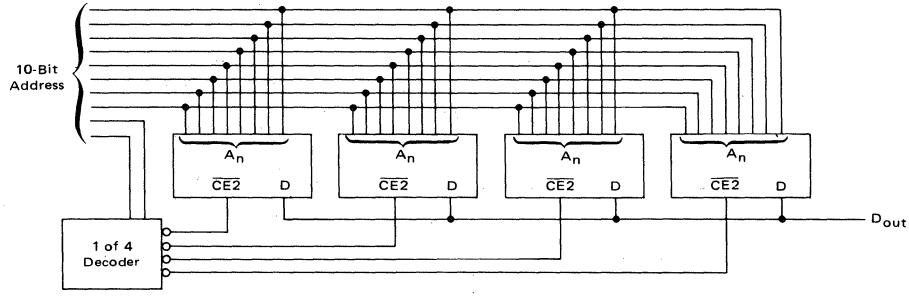


$T_{word} = t_{acc(\overline{ST})} + (n-1)\, t_{acc(\overline{CE1})}$

$T_{word(typ)} \simeq 3.8\ \mu s$ for a 32-bit serial word at $V_{DD} = 10$ V



Typical 1024 x 1 RAM Utilizing Four MCM14537's.



Typical Low Power 1024 x 1 RAM Utilizing Four MCM14537's.

MCM14552AL
MCM14552CL
MCM14552CP

McMOS

(LOW-POWER COMPLEMENTARY MOS)

256-BIT (64 x 4) STATIC RANDOM ACCESS MEMORY

256-BIT STATIC RANDOM ACCESS MEMORY

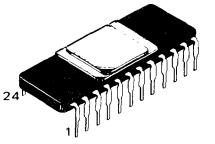
The MCM14552 is a static random access memory (RAM) organized in a 64 x 4 bit pattern. The three chip enable inputs can be used as extensions of the six address inputs, creating 9-bit address scheme. Eight MCM14552 devices may be used to comprise a 2048-bit memory (512 x 4) without additional address decoding.

The mode control (M) is used to change the control logic characteristic of the circuit. For example, with M high, the 3-state input ($\overline{T}$) fully controls the 3-state characteristic of the output. With M low, the output 3-state characteristic is controlled by chip enable inputs ($\overline{CE}$), write enable input ($\overline{WE}$) and $\overline{T}$. The latch enable ($\overline{LE}$) input provides flexibility for holding output data unchanged during write operations as well as increasing the outputting of paired words.

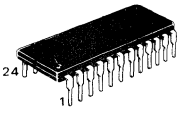
The memory is designed so that dc signals may operate the memory, with no maximum pulse width restrictions.

Medium speed, micropower operation, and control flexibility make the device useful in scratch pad or buffer applications where battery operation or high noise immunity are required.

- Quiescent Power Dissipation = 10 μW/package typical @ V_{DD} = 10 Vdc
- Noise Immunity = 45% of V_{DD} typical
- Wired-OR Output Capability (3-state output) for Memory Expansion
- Output Data Latch Eliminates Need for Storage Buffer
- Access Time = 700 ns typical @ V_{DD} = 10 Vdc
- Fully Decoded and Buffered

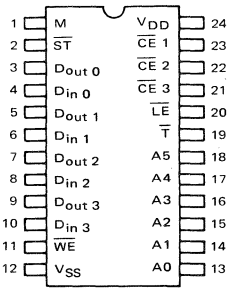


L SUFFIX
CERAMIC PACKAGE
CASE 684



P SUFFIX
PLASTIC PACKAGE
CASE 709

PIN ASSIGNMENT



MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8)

Rating		Symbol	Value	Unit
DC Supply Voltage	MCM14552AL MCM14552CL/CP	V_{DD}	+18 to -0.5 +16 to -0.5	Vdc
Input Voltage, All Inputs		V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Pin		I	10	mAdc
Operating Temperature Range	MCM14552AL MCM14552CL/CP	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range		T_{stg}	-65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}.

2

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{out}	5.0	–	0.01	–	0	0.01	–	0.05	Vdc
		10	–	0.01	–	0	0.01	–	0.05	
		15	–	0.05	–	0	0.05	–	0.25	
"1" Level		5.0	4.99	–	4.99	5.0	–	4.95	–	Vdc
		10	9.99	–	9.99	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.75	–	
Noise Immunity#	V_{NL}									Vdc
($\triangle V_{out} \leq 0.8$ Vdc)		5.0	1.5	–	1.5	2.25	–	1.4	–	
($\triangle V_{out} \leq 1.0$ Vdc)		10	3.0	–	3.0	4.50	–	2.9	–	
($\triangle V_{out} \leq 1.5$ Vdc)		15	4.5	–	4.5	6.75	–	4.4	–	
($\triangle V_{out} \leq 0.8$ Vdc)	V_{NH}	5.0	1.4	–	1.5	2.25	–	1.5	–	Vdc
($\triangle V_{out} \leq 1.0$ Vdc)		10	2.9	–	3.0	4.50	–	3.0	–	
($\triangle V_{out} \leq 1.5$ Vdc)		15	4.4	–	4.5	6.75	–	4.5	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-0.62	–	-0.50	-1.7	–	-0.35	–	
(V_{OH} = 9.5 Vdc)		10	-0.62	–	-0.50	-0.9	–	-0.35	–	
(V_{OH} = 13.5 Vdc)		15	-1.8	–	-1.5	-3.5	–	-1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.50	–	0.40	0.78	–	0.28	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.1	–	0.90	2.0	–	0.65	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	7.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-0.23	–	-0.20	-1.7	–	-0.16	–	
(V_{OH} = 9.5 Vdc)		10	-0.23	–	-0.20	-0.9	–	-0.16	–	
(V_{OH} = 13.5 Vdc)		15	-0.69	–	-0.60	-3.5	–	-0.48	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.23	–	0.20	0.78	–	0.16	–	mAdc
(V_{OL} = 0.5 Vdc)		10	0.60	–	0.50	2.0	–	0.40	–	
(V_{OL} = 1.5 Vdc)		15	1.8	–	1.5	7.8	–	1.2	–	
Input Current	I_{in}	–	–	–	–	10	–	–	–	pAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	–	–	–	pF
Quiescent Dissipation (AL Device)	P_Q	5.0	–	0.5	–	0.005	0.5	–	9.0	mW
		10	–	2.0	–	0.01	2.0	–	36	
		15	–	6.0	–	0.02	6.0	–	108	
Quiescent Dissipation (CL/CP Device)	P_Q	5.0	–	2.5	–	0.005	2.5	–	39	mW
		10	–	10	–	0.01	10	–	100	
		15	–	30	–	0.02	30	–	300	
Power Dissipation**† (Dynamic plus Quiescent) (C_L = 15 pF)	P_D	5.0	P_D = (6.4 mW/MHz) f + P_Q							mW
		10	P_D = (25.6 mW/MHz) f + P_Q							
		15	P_D = (57.6 mW/MHz) f + P_Q							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
†For dissipation at different external load capacitance (C_L) use the formula:

$$P_T(C_L) = P_D + 2 \times 10^{-3} (C_L - 15\text{ pF}) V_{DD}^2 f$$

where: P_T, P_D in mW (per package), C_L in pF, V_{DD} in Vdc, and f in MHz is input frequency.
**The formula given is for the typical characteristics only.

SWITCHING CHARACTERISTICS* (C_L = 15 pF, T_A = 25°C)

Characteristic	Figure	Symbol	V_{DD} Vdc	Typ All Types	Max AL Device	Max CL/CP Device	Unit
Output Rise Time	1	t_r					ns
t_r = (3.0 ns/pF) C_L + 25 ns			5.0	70	175	200	
t_r = (1.5 ns/pF) C_L + 12 ns			10	35	75	110	
t_r = (1.1 ns/pF) C_L + 8 ns			15	25	55	80	
Output Fall Time	1	t_f					ns
t_f = (1.5 ns/pF) C_L + 47 ns			5.0	70	175	200	
t_f = (0.75 ns/pF) C_L + 24 ns			10	35	75	110	
t_f = (0.55 ns/pF) C_L + 17 ns			15	25	55	80	
Read Cycle Time	1,2	$t_{cyc(R)}$	5.0	2000	3000	6000	ns
			10	750	1100	2200	
			15	500	825	1650	
Write Cycle Time	3,4	$t_{cyc(W)}$	5.0	1200	1800	3600	ns
			10	750	1100	2200	
			15	500	825	1650	
Address to $\overline{\text{Strobe}}$ Setup Time	1,3	$t_{setup(A\text{-}\overline{ST})}$	5.0	500	750	1500	ns
			10	150	225	450	
			15	120	170	350	
$\overline{\text{Strobe}}$ to Address Hold Time	1,3	$t_{hold(\overline{ST}\text{-}A)}$	5.0	50	75	150	ns
			10	0	35	100	
			15	0	25	75	
Address to $\overline{\text{Chip Enable}}$ Setup Time	2,4	$t_{setup(A\text{-}\overline{CE})}$	5.0	600	900	1800	ns
			10	200	300	600	
			15	150	225	450	
$\overline{\text{Chip Enable}}$ to Address Hold Time	2,4	$t_{hold(\overline{CE}\text{-}A)}$	5.0	150	225	450	ns
			10	100	150	300	
			15	75	120	225	
$\overline{\text{Strobe}}$ or $\overline{\text{Chip Enable}}$ Pulse Width When Reading	1,2	PW(R)	5.0	450	900	1800	ns
			10	150	225	450	
			15	100	170	350	
$\overline{\text{Strobe}}$ or $\overline{\text{Chip Enable}}$ Pulse Width When Writing	3,4	PW(W)	5.0	1200	1800	3600	ns
			10	600	900	1800	
			15	400	675	1350	
Read Setup Time	1	$t_{setup(R)}$	5.0	-100	30	0	ns
			10	-40	10	0	
			15	-30	7.5	0	
Read Hold Time	1	$t_{hold(R)}$	5.0	180	360	540	ns
			10	60	180	240	
			15	45	140	180	
Data Setup Time	3,4	$t_{setup(D)}$	5.0	600	900	1800	ns
			10	200	300	600	
			15	150	225	450	
Data Hold Time	3,4	$t_{hold(D)}$	5.0	200	300	600	ns
			10	50	75	150	
			15	30	60	120	

*The formula given is for the typical characteristics only.

(continued)

2

SWITCHING CHARACTERISTICS (C_L = 15 pF, T_A = 25°C) (continued)

Characteristic	Figure	Symbol	V_{DD} Vdc	Typ All Types	Max AL Device	Max CL/CP Device	Unit
Write Enable Setup Time	3,4	$t_{setup(\overline{WE})}$	5.0	240	480	720	ns
			10	80	160	240	
			15	55	120	180	
Write Enable Hold Time	3,4	$t_{hold(\overline{WE})}$	5.0	50	100	150	ns
			10	20	40	60	
			15	15	30	45	
Read Access Time from Strobe	1,3	$t_{acc(R\text{-}\overline{ST})}$	5.0	2000	3000	6000	ns
			10	700	1050	2100	
			15	350	800	1600	
Read Access Time from Chip Enable	2	$t_{acc(R\text{-}\overline{CE})}$	5.0	2100	3150	6300	ns
			10	750	1100	2250	
			15	400	825	1700	
Output Enable/Disable Delay from Chip Enable or Write Enable	2,4	$t_{R(\overline{CE})}$, $t_{R(\overline{WE})}$	5.0	400	600	1200	ns
			10	200	400	600	
			15	150	300	450	
Three-State Enable/Disable Output Delay	2	$t_{(\overline{T})}$	5.0	400	600	1200	ns
			10	160	240	480	
			15	120	180	360	
Latch to Output Propagation Delay	1	$t_{\overline{LE}}$	5.0	500	750	1500	ns
			10	200	300	600	
			15	150	225	450	

LOGIC DIAGRAM

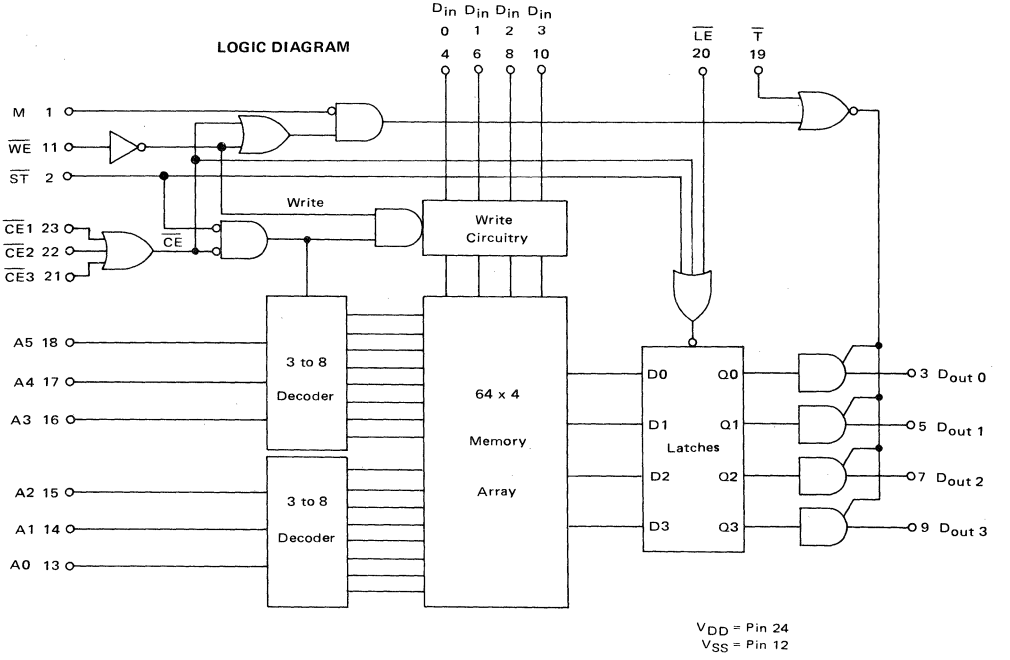
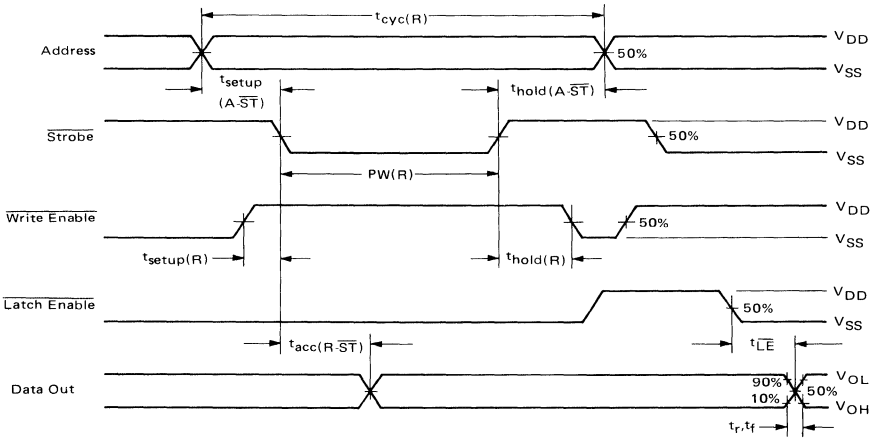
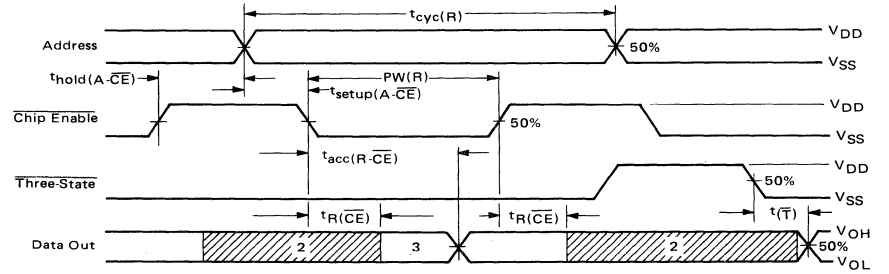


FIGURE 1 – READ CYCLE WAVEFORMS UTILIZING STROBE TO ACCESS MEMORY



Notes: 1 – $\overline{CE}1$, $\overline{CE}2$, $\overline{CE}3$ and $\overline{T}$ are low, M is high.
2 – $\overline{WE}$ may be held high during the complete read cycle.

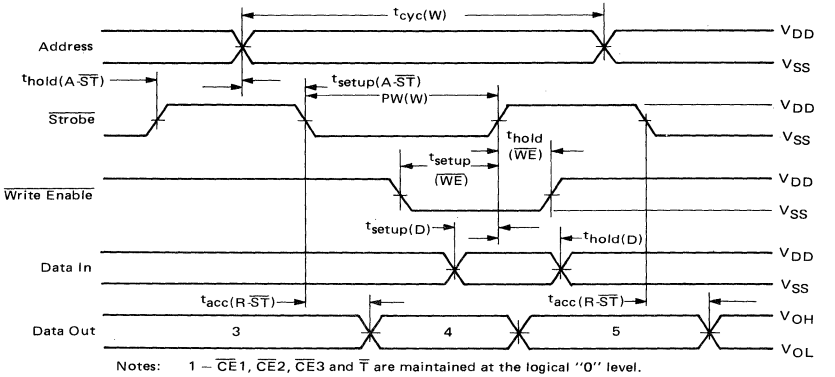
FIGURE 2 – READ CYCLE WAVEFORMS UTILIZING CHIP ENABLE TO ACCESS MEMORY



Notes: 1 – Unused $\overline{CE}$, $\overline{ST}$, M and $\overline{T}$ are low and $\overline{WE}$ is high.
2 – High impedance output state occurs when any $\overline{CE}$ is high and M is low, or when $\overline{T}$ is high.
3 – The output displays data from the previous state.
4 – $PW(R) \geq t_{acc(R-\overline{CE})max}$.

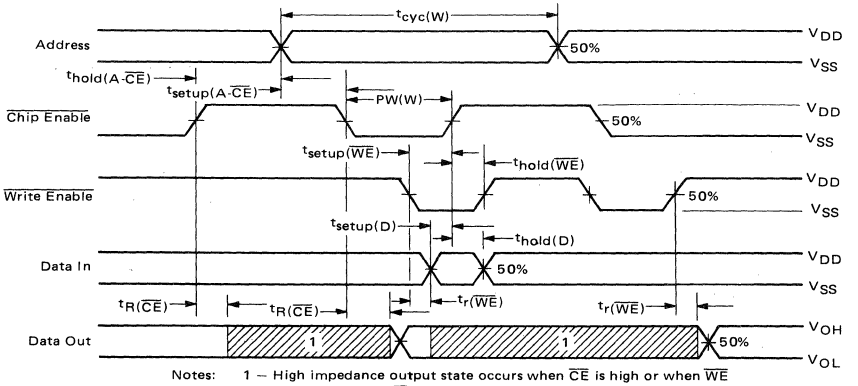
2

FIGURE 3 – WRITE CYCLE WAVEFORMS UTILIZING STROBE



Notes: 1 – $\overline{CE}1$, $\overline{CE}2$, $\overline{CE}3$ and $\overline{T}$ are maintained at the logical "0" level.
2 – M is maintained at the logical "1" level.
3 – The output displays the contents of the previous state.
4 – The output displays the contents of the presently addressed location as in a read modify write cycle.
5 – The output displays the data that was written into addressed location.

FIGURE 4 – WRITE CYCLE WAVEFORM UTILIZING CHIP ENABLE



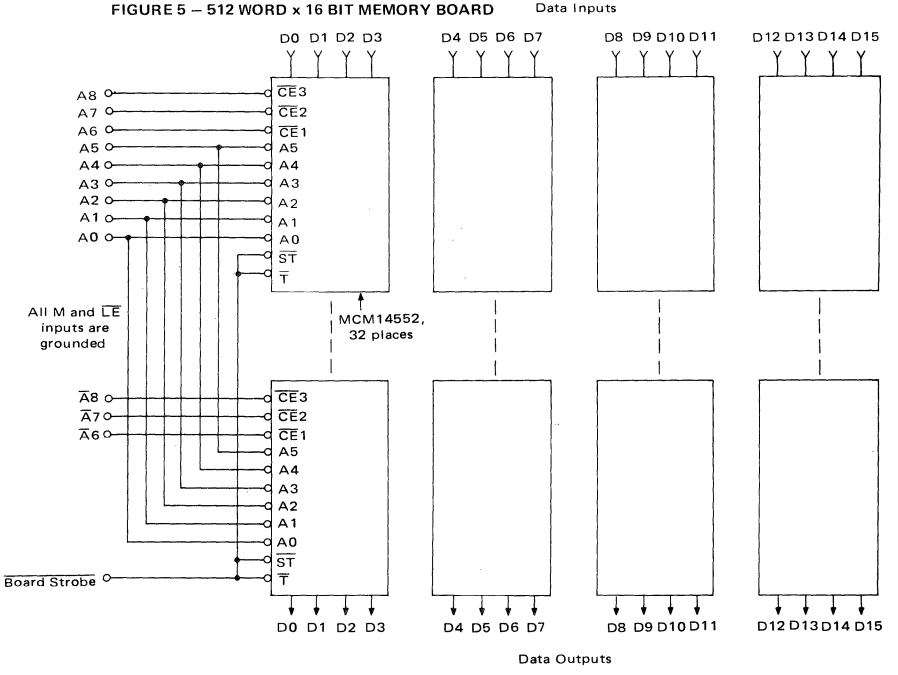
Notes: 1 – High impedance output state occurs when $\overline{CE}$ is high or when $\overline{WE}$ is low, for M and $\overline{T}$ maintained in the low state.
2 – Unused $\overline{CE}$'s, $\overline{ST}$, M and $\overline{T}$ are maintained at the logical "0" level.

TRUTH TABLE

Function	$\overline{CE}$ 1	$\overline{CE}$ 2	$\overline{CE}$ 3	$\overline{T}$	$\overline{LE}$	M	$\overline{ST}$	$\overline{WE}$	D_{in}	D_{out}	Comments
Address Changing Valid	X	X	X	X	X	X	1	X	X	R/A	D_{out} will be active if all $\overline{CE}$ = 0, T = 0 and $\overline{WE}$ = 1 or if M = 1 and $\overline{T}$ = 0
	X	X	1	X	X	X	X	X	X	R/A	
	X	1	X	X	X	X	X	X	X	R/A	
	1	X	X	X	X	X	X	X	X	R/A	
Address Changing Not Valid	0	0	0	X	X	X	0	X	X	R/A	D_{out} will be active if $\overline{T}$ = 0 and $\overline{WE}$ = 1 or if M = 1 and $\overline{T}$ = 0
D_{out} Disabled (in high resistance state)	X	X	1	X	X	0	X	X	X	R	Disables write circuitry
	X	1	X	X	X	0	X	X	X	R	
	1	X	X	X	X	0	X	X	X	R	
	X	X	X	1	X	X	X	X	X	R	$\overline{T}$ = 1 always disables D_{out}
	X	X	X	X	X	0	X	0	X	R	M = 0 and write operation disables D_{out}
D_{out} Enabled (in active state)	0	0	0	0	X	X	X	1	X	A	Read operation, D_{out} active
	X	X	X	0	X	1	X	X	X	A	Read or write, D_{out} active
Read Addressed Memory Location Into Output Latch	0	0	0	X	0	X	0	X	X	R/A	If $\overline{WE}$ = 0, D_{in} = D_{out}
Disable Reading From Memory	X	X	1	X	X	X	X	X	X	R/A	
	X	1	X	X	X	X	X	X	X	R/A	
	1	X	X	X	X	X	X	X	X	R/A	
	X	X	X	X	X	X	1	X	X	R/A	
	X	X	X	X	X	X	X	0	X	R/A	
Write Into Memory	0	0	0	X	X	X	0	0	A	R/A	
Write Disabled	X	X	1	X	X	X	X	X	X	R/A	
	X	1	X	X	X	X	X	X	X	R/A	
	1	X	X	X	X	X	X	X	X	R/A	
	X	X	X	X	X	X	1	X	X	R/A	
	X	X	X	X	X	X	X	1	X	R/A	
Output Latch Enabled	0	0	0	X	0	X	0	X	X	R/A	
Output Latch Disabled	X	X	1	X	X	X	X	X	X	R/A	
	X	1	X	X	X	X	X	X	X	R/A	
	1	X	X	X	X	X	X	X	X	R/A	
	X	X	X	X	1	X	X	X	X	R/A	
	X	X	X	X	X	X	1	X	X	R/A	

R = High resistance state at D_{out}.
A = An active level of either V_{DD} or V_{SS}.
R/A = An R or A condition depending on the don't care condition.
X = Don't care condition (must be in the "1" or "0" state)
1 = A high level at V_{DD}.
0 = A low level at V_{SS}.

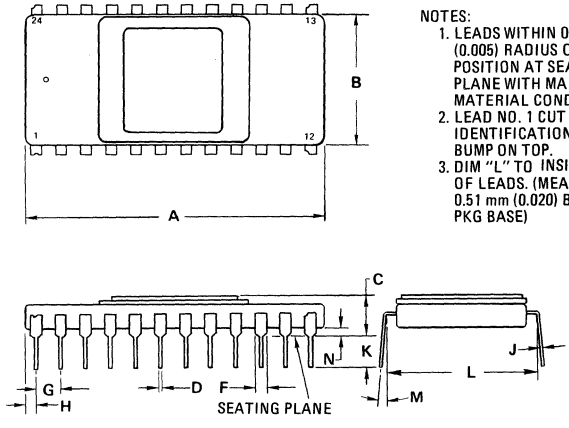
FIGURE 5 – 512 WORD x 16 BIT MEMORY BOARD



2

PACKAGE DIMENSIONS

L SUFFIX
CERAMIC PACKAGE
CASE 684-04

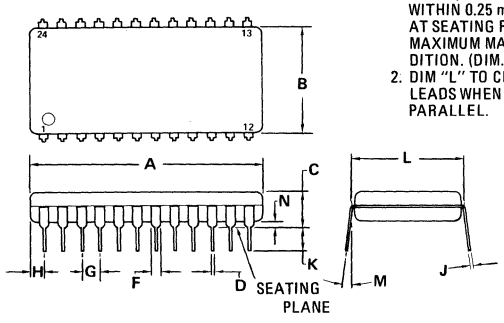


NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE WITH MAXIMUM MATERIAL CONDITION.
2. LEAD NO. 1 CUT FOR IDENTIFICATION, OR BUMP ON TOP.
3. DIM "L" TO INSIDE OF LEADS. (MEASURED 0.51 mm (0.020) BELOW PKG BASE)

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	29.34	30.86	1.155	1.215
B	12.70	14.22	0.500	0.560
C	3.05	3.94	0.120	0.155
D	0.38	0.51	0.015	0.020
F	0.89	1.40	0.035	0.055
G	2.54 BSC		0.100 BSC	
H	0.89	1.40	0.035	0.055
J	0.20	0.30	0.008	0.012
K	2.92	3.68	0.115	0.145
L	14.86	15.87	0.585	0.625
M	–	15^0	–	15^0
N	0.51	1.14	0.020	0.045

CASE 684-04

P SUFFIX
PLASTIC PACKAGE
CASE 709-01

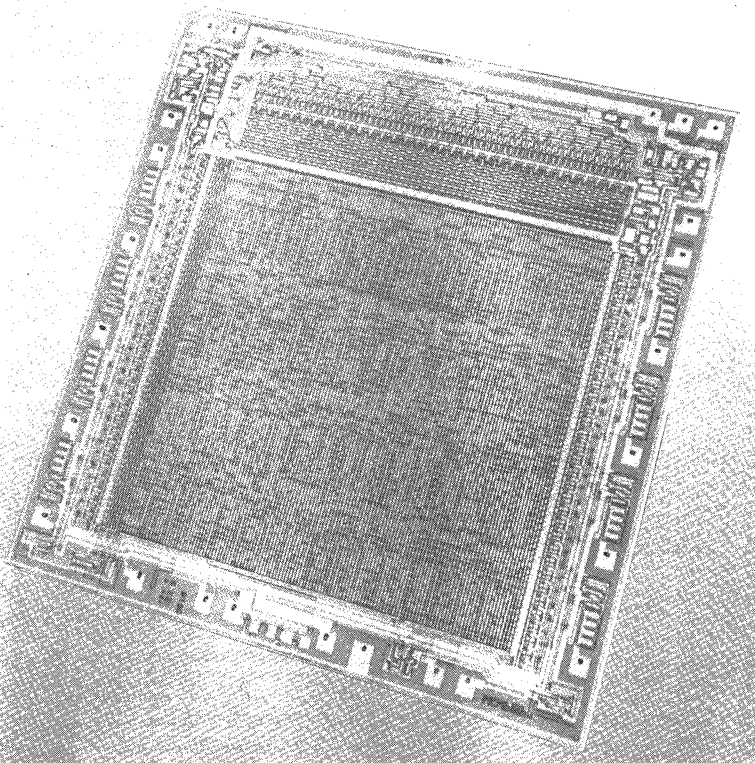


NOTES:
1. LEADS, TRUE POSITIONED WITHIN 0.25 mm (0.010) DIA AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION. (DIM. "D")
2. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	31.37	32.13	1.235	1.265
B	13.72	14.22	0.540	0.560
C	4.57	5.08	0.180	0.200
D	0.36	0.51	0.014	0.020
F	1.02	1.52	0.040	0.060
G	2.41	2.67	0.095	0.105
H	1.78	2.03	0.070	0.080
J	0.20	0.30	0.008	0.012
K	3.05	3.56	0.120	0.140
L	14.73	15.24	0.580	0.600
M	0^0	10^0	0^0	10^0
N	0.51	1.02	0.020	0.040

CASE 709-01

Read Only Memories (ROM)/Chapter 3



3

READ ONLY MEMORIES

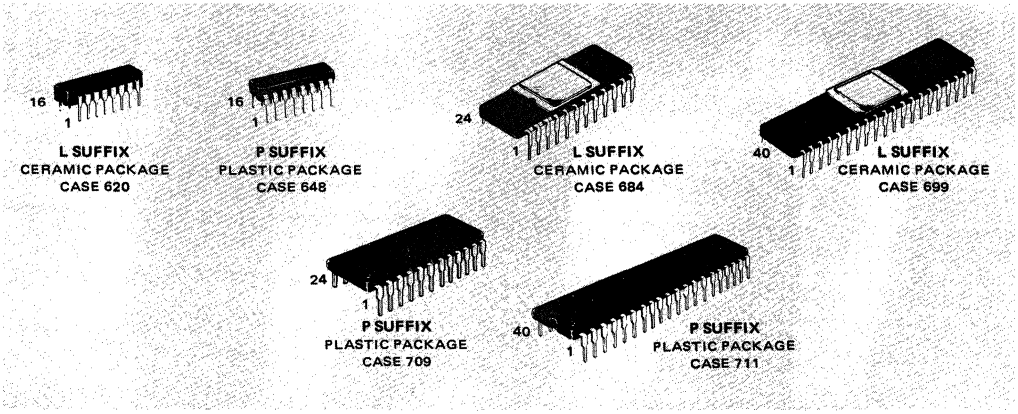
Motorola's Read Only Memories include both pre-programmed memories and mask-programmable memories for custom applications.

The character generators are useful in CRT displays as well as in digital printers. Together with the code converters, which facilitate interface circuitry when going from one character standard to another, they provide a wide choice of devices for data display systems. ROMs are also available to provide the rhythm patterns for electronic organs.

ROMs which are specifically intended for use with the M6800 Microcomputer Family are shown in Chapter 4.

Device No.	No. of Bits	Description	Organization	Access Time (ns max)	Power Supplies (V)	No. of Pins	Case	Page No.
METAL GATE NMOS								
MCM6550*	7168	Mask-Programmable, Static, Rhythm	16 Patterns of 24 or 32 Beats	t_{cyc} = 1 ms	+15, +5, −3	40	699, 711	3-5
MCM6560*	8192	Mask-Programmable, Addressable	1024 x 8 or 2048 x 4	350	+12, +5, −3	24	684, 709	3-13
Pre-Programmed Standard Memories:								
MCM6561		Binary Code Converter	1024 x 8					
MCM6562		Binary Code Converter	1024 x 8					
MCM6570*	8192	Mask-Programmable 9 x 7 Character Generator, Horizontal Scan, Shift Capability	128c x (9 x 7)	500	+12, +5, −3	24	684, 709	3-27
Pre-Programmed Standard Memories:								
MCM6571		ASCII Characters and Greek, Shifted						
MCM6571A		ASCII Characters and Greek, Shifted						
MCM6572		ASCII and Greek, Not Shifted						
MCM6573		Japanese Characters, Not Shifted						
MCM6574		Math Symbols and Pictures, Shifted						
MCM6575		Alphanumeric Control Characters, Shifted						
MCM6576		British Standard Characters, Shifted						
MCM6577		German Standard Characters, Shifted						
MCM6578		French Standard Characters, Shifted						
MCM6579		General European Standard Characters, Shifted						
MCM6580*	8192	Mask-Programmable 7 x 9 Character Generator, Vertical Scan, Shift Capability	128c x (7 x 9)	400	+12, +5, −3	24	684, 709	3-41
Pre-Programmed Standard Memories:								
MCM6581		ASCII Characters and Greek, Shifted						
MCM6583		Japanese Characters, Not Shifted						
MCM6590*	16384	Mask-Programmable, Static	2048 x 8	800	+12, +5, −3	24	684	3-49
Pre-Programmed Standard Memory:								
MCM6591		Universal Code Converter						
METAL GATE CMOS								
MCM14524A*	1024	Mask-Programmable, −55 to +125°C	256 x 4	2650#	+3 to +18	16	620	3-63
MCM14524C*	1024	Mask-Programmable, −40 to +85°C	256 x 4	3975#	+4.5 to +16	16	620, 648	

*Mask-programmable ROMs are manufactured according to a bit-pattern supplied by the customer. A special device number (SCMxxxx) is assigned to each individual pattern. #Measured with V_{DD} = +5 V, T_A = 25°C



MASK PROGRAMMABLE ROM PROCESSING

The programming formats used to customize Motorola's mask-programmable NMOS ROMs are detailed on each data sheet. The formats were generated with both the customer and the automation of mask generation being prime considerations. The use of hexadecimal format on cards and paper tape allows the efficient reduction and transmission of the data to the factory.

Once the data for a custom ROM is received at the factory, the customer's inputs are checked and submitted to our computer aided mask preparation facilities, where work is initiated to generate masks containing the customized pattern information.

This technique also allows Motorola to return to the customer a printout for verification of the formatted data prior to generation of the masks and start of wafer processing. The customer data base is also used to generate the computer test format which allows accurate and complete testing even on prototype samples.

It is with this simplified and automated procedure that Motorola is able to provide both short cycle times and volume production.

MCM6550L
MCM6550P

7168-BIT STATIC ROM RHYTHM GENERATOR

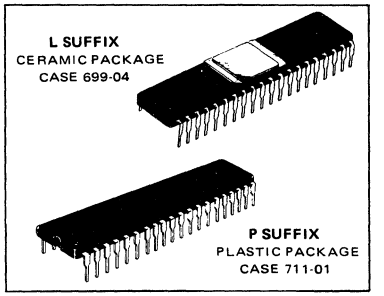
The MCM6550 is a mask-programmable Read Only Memory fabricated with high-performance, N-channel, metal-gate technology. It is designed as a rhythm ROM, with 7168 bits organized as 16 rhythm patterns of either 24 or 32 beats per rhythm, and with 14 outputs. An internal counter counts either 24 or 32 beats according to the input at the 24/32 Select pin. No external counters or one-shots are necessary. The outputs are directly compatible with TTL and DTL.

- 24 or 32 Beats per Rhythm With Counter on Chip
- 16 Rhythms
- 14 Outputs; Any Two May Be Wire-ORed
- On-Chip One-Shot With Capacitance Controlled Pulse Width to Strobe the Outputs
- Second On-Chip One-Shot With Capacitance Controlled Pulse Width to Strobe the Downbeat Output
- Outputs Can Drive Higher Output Voltages Than TTL by Increasing V_{CC} Voltage Above 5 Volts

MOS

(N-CHANNEL, LOW THRESHOLD)

7168-BIT STATIC READ ONLY MEMORY RHYTHM GENERATOR

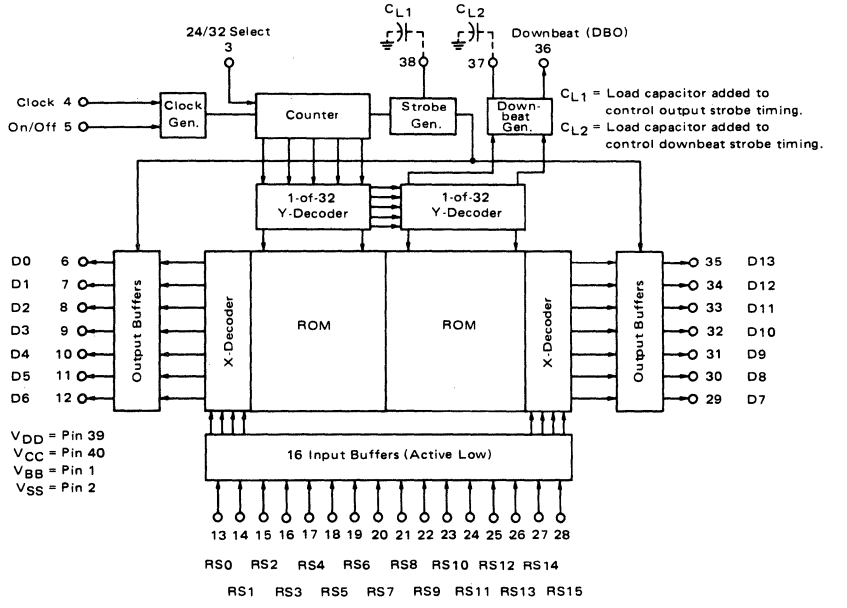


L SUFFIX
CERAMIC PACKAGE
CASE 699-04

P SUFFIX
PLASTIC PACKAGE
CASE 711-01

3

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1] (Referenced to V_{SS})

Rating	Symbol	Value	Unit
Supply Voltages	V_{DD} V_{CC} V_{BB}	-0.3 to +20 -0.3 to +20 -15 to +0.3	Vdc
Input Voltage	V_{in}	-0.3 to +20	Vdc
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-55 to +125	°C

Note 1: This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS
(Full operating voltage and temperature range unless otherwise noted.)

RECOMMENDED DC OPERATING CONDITIONS (Referenced to V_{SS} = Ground)

Parameter	Symbol	Min	Nom	Max	Unit
Supply Voltage	V_{DD}	13	15	17	Vdc
	V_{CC}	4.5	5.0	17	Vdc
	V_{BB}	-3.5	-3.0	-2.5	Vdc
Input High Voltage	V_{IH}	3.0	–	V_{CC}	Vdc
Input Low Voltage	V_{IL}	0	–	0.6	Vdc

DC CHARACTERISTICS (Positive currents flow into the chip, negative currents out.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Leakage Current (V_{IH} = 5.0 Vdc, V_{CC} = 5.0 Vdc)	I_{IH}	–	–	100	μAdc
Input Forward Current (V_{IL} = 0.4 Vdc)	I_{IL}	-800	-330	–	μAdc
Output High Voltage (I_{OH} = -100 μAdc)	V_{OH}	4.0	–	–	Vdc
Output Low Voltage (I_{OL} = 2.0 mAdc)	V_{OL}	–	–	0.4	Vdc
Supply Current	I_{DD}	–	10	20	mAdc
	I_{CC}	–	9.0	20	mAdc
	I_{BB}	-2.0	-1.0	–	mAdc
Power Dissipation	P_D	–	200	500	mW

CAPACITANCE (Periodically Sampled Rather Than 100% tested.)

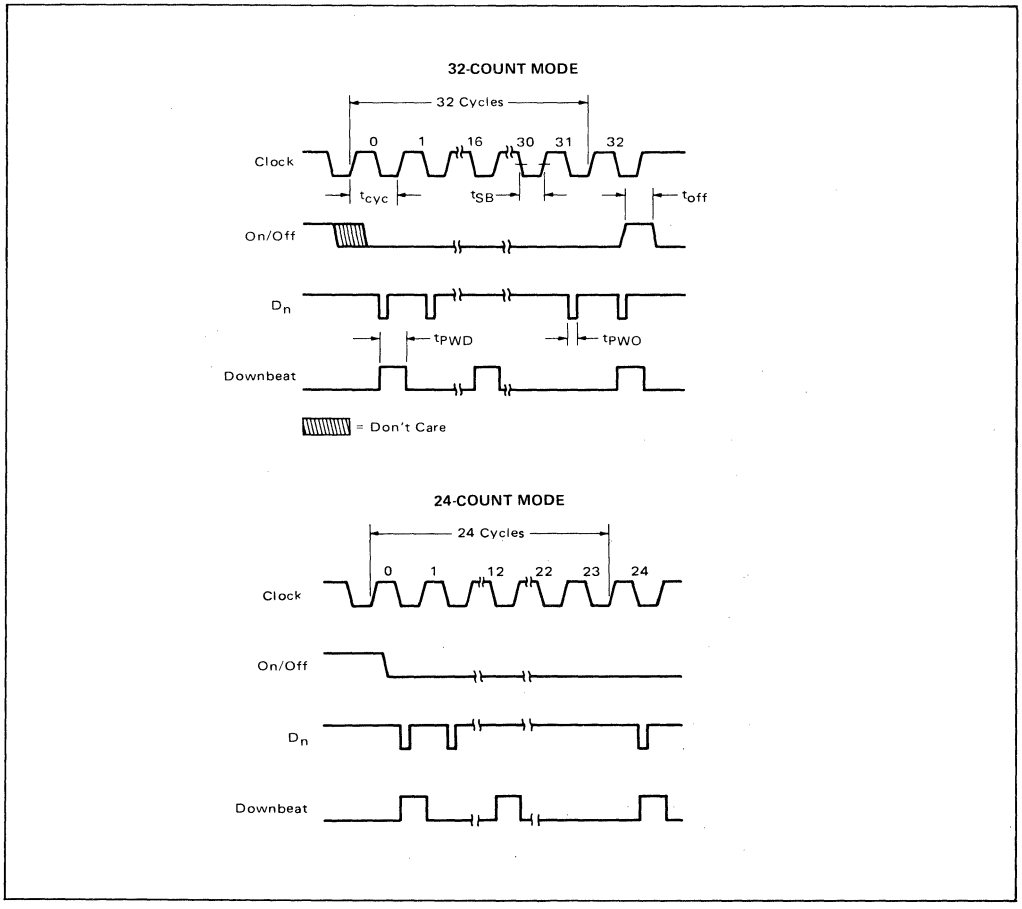
Characteristic	Symbol	Min	Typ	Max	Unit
Input Capacitance (f = 1 MHz)	C_{in}	–	–	10	pF
Output Capacitance (f = 1 MHz)	C_{out}	–	–	12	pF

AC CHARACTERISTICS
(Full operating voltage and temperature unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Cycle Time (Tempo)	t_{cyc}	1.0	–	dc	ms
Clock Down Time	t_{SB}	1.1 (t_{PWO})	–	–	–
Off Time	t_{off}	1.25 (t_{PWD}) – t_{cyc}	–	–	–
Output Pulse Width	t_{PWO}	–	6 C_{L1}/0.1 μF	–	ms
Downbeat Pulse Width	t_{PWD}	–	120 C_{L2}/0.1 μF	–	ms

3

FIGURE 1 – TIMING DIAGRAMS



TYPICAL CHARACTERISTIC CURVES

FIGURE 2 – NORMALIZED PULSE WIDTH versus V_{DD}

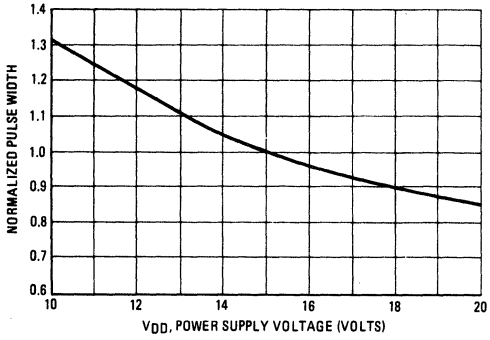


FIGURE 3 – OUTPUT HIGH VOLTAGE versus V_{DD}

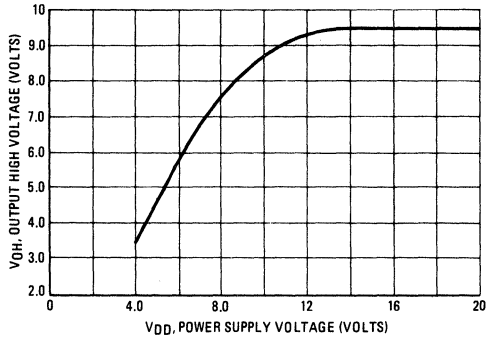


FIGURE 4 – NORMALIZED PULSE WIDTH versus TEMPERATURE

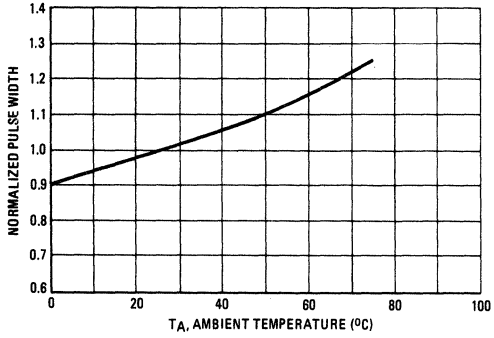


FIGURE 5 – NORMALIZED POWER DISSIPATION versus TEMPERATURE

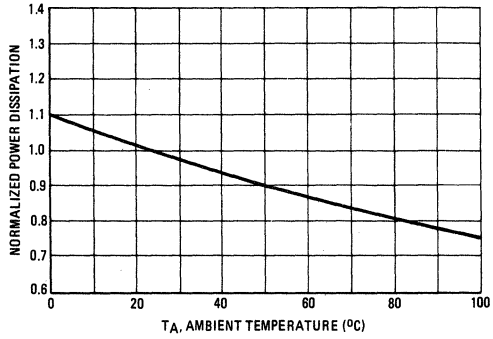
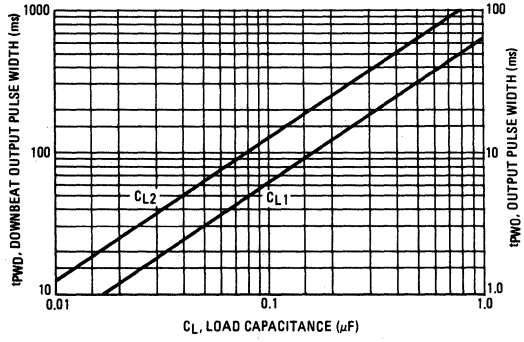


FIGURE 6 – PULSE WIDTHS versus EXTERNAL LOAD CAPACITANCE



MEMORY OPERATION (Using Negative Logic)
Most positive level = 0, most negative level = 1

The MCM6550 has a total of 7168 bits arranged to have 512 bits of information programmed for each of 14 outputs. These 512 bits are further arranged as 16 rhythms with 32 programmed bits per rhythm.

When the memory is ON, one of the Rhythm Select inputs (RS0 thru RS15) is chosen by applying V_{IL} to the appropriate pin. All other RS inputs are normally held at V_{IH}. These inputs are connected to the internal X-decoder, which routes the appropriate rhythm to the output.

The Clock input is used to increment an internal 5-bit counter which in turn is used in the Y-decoder. The two acting together sequence thru the 32 bits per rhythm, repeating the rhythm as long as the RS_n inputs do not change and the memory is ON.

24/32 Select

This input to the MCM6550 selects either 24 or 32 bits per rhythm. This is achieved by modifying the operation of the internal counter. When 32 bits are chosen, the counter counts from 0 to 31 – a total of 32 counts. As long as the clock oscillates and the part is ON, the counter continues counting 0-31, 0-31 and so on. (When the part is OFF, the counter resets to zero.) This counter increments on the rising edge of Clock. To obtain 32-bit operation, the 24/32 Select input is left open and an internal resistor will pull V_{in} to V_{IH}.

In order to obtain the 24-bit operation, set the 24/32 Select input with $V_{in} = V_{IL}$. The internal counter is modified to count from 0 thru 11, then skip to counts 16 thru 27, then back to a 0 thru 11, and so on. The total number of counts 0-11 and 16-27 is 24.

RS_n

The Rhythm Select inputs are used to select the appropriate rhythms. When only one RS input is low, the output of the chip is straightforward. The information comes out as programmed. However, two or more RS inputs may be pulled low at the same time, mixing the information from two or more 32-bit strings. The mixed bits are ORed; i.e., when any one bit is programmed for $V_{out} = V_{OL}$ ("one") the output will be V_{OL}. Only when all bits are programmed for $V_{out} = V_{OH}$ ("zero") will the output be V_{OH}.

D_n

There are 14 outputs on the MCM6550, labeled D0 thru D13. These outputs are normally high (V_{OH}). When a "zero" is read, the output remains high. When a "one" is read, the output goes low at the falling edge of Clock for pulse width t_{PWO}.

Two outputs may be tied together, logically providing an AND function. Only when both outputs are individually programmed high does the common output remain high. As long as either or both of the separate outputs are programmed low, the common output goes low for pulse width t_{PWO} before returning to the normally high state.

An external loading capacitor C_{L1} is connected to Pin 38. This capacitor controls the internal strobe generator which in turn controls the length of t_{PWO}.

Downbeat (DBO)

The Downbeat output is normally low. When the count in the internal counter is either zero or 16, Downbeat goes high for pulse width t_{PWD} at the falling edge of Clock, assuming the chip is ON. If the chip is turned OFF during a Downbeat, the output pulse will nonetheless last the full t_{PWD}. The duration of t_{PWD} is determined by the loading capacitor C_{L2} at Pin 37. Downbeat occurs every 12 cycles in the 24-count mode, and every 16 cycles in the 32-count mode.

CUSTOM PROGRAMMING FOR MCM6550

By the programming of a single photomask, the customer may specify the content of the MCM6550. Encoding of the photomask is done with the aid of a computer to provide quick, efficient implementation of the custom bit pattern while reducing the cost of implementation.

Information for the custom memory content may be sent to Motorola in the following forms, in order of preference:*

1. Hexadecimal coding using IBM Punch Cards
2. Hexadecimal coding using ASCII Paper Tape Punch

Programming the MCM6550 is a straightforward procedure. The desired beats (a beat is defined as $V_{out} = V_{OL}$ for time t_{PWO}) are marked on a coding sheet, such as the one provided for your convenience at the end of this data sheet. (These sheets are not to be submitted to Motorola.) One coding sheet is required for each rhythm.

If a 32 count is used (4/4 timing), all 32 beats are filled in. For a 24 count (3/4 timing), beats 12 thru 15 and 28 thru 31 are left blank. Once this information is completed, the coding is converted to hexadecimal, treating marked-in blocks as "ones" and blanks as "zeros".

When all sheets have been completed, these hex characters are transferred to punch cards starting with Rhythm 0, Beat 0 and ending with Rhythm 15, Beat 31. Even though the 24-count mode does not utilize 8 of the available beats, these beats must be programmed with hex zeros — 16 for beats 12 thru 15 and an additional 16 for beats 28 thru 31.

CARD PUNCH FORMAT

The hexadecimal equivalent (from the coding sheet) should be placed on 80-column punch cards as follows:

Columns	
1- 7	Blank
8	Asterisk(*)
9-72	Hex coding
73-76	Blank
77-78	Card number (starting 01; thru 32)
79-80	Blank

Column 9 on the first card contains the hexadecimal equivalent of 0, 0, D13, D12. Column 10 contains the equivalent of D11 thru D8, column 11 contains D7 thru D4, and column 12 D3 thru D0. These four hex characters program all 14 outputs for Beat 0, Rhythm 0. The next four hex characters program the information for Beat 1, and so on. The first card contains a total of 64 hex characters, equivalent to the data for the first 16 beats of Rhythm 0. The second card programs the remaining 16 beats. The remaining Rhythms are programmed in numeric sequence. At two cards per Rhythm, a total of 32 cards are required.

PAPER TAPE FORMAT

The programming of paper tape is nearly identical to card punch programming. Information is grouped in 32 lines of 64 hex characters, each line terminated with a carriage return and line feed. Note that blanks and card numbers are not included. The hex characters and the lines follow the same sequence as card punch format.

The software program which reads the tape recognizes the first carriage return and line feed as the start of data. Therefore, the customer has the option of using the first characters of the tape for internal identification, terminating with a carriage return and line feed, thereby initiating data entry.

*Note: Motorola can accept magnetic tape and truth table formats. For further information contact your local Motorola sales representative.

The coding format below is given for your convenience in preparing character information for MCM6550 programming. THIS FORMAT IS NOT TO BE USED TO TRANSMIT THE INFORMATION TO MOTOROLA. Refer to the Custom Programming instructions for detailed procedures.

RHYTHM SELECT _____ (0-15)

Beat		Binary Coding													Hex Coding			
		a		b			c				d							
32 Count	24 Count	D 13	D 12	D 11	D 10	D 9	D 8	D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0	a	b	c	d
0	0																		
1	1																		
2	2																		
3	3																		
4	4																		
5	5																		
6	6																		
7	7																		
8	8																		
9	9																		
10	10																		
11	11																		
12	Blank																		
13																			
14																			
15																			
16	12																		
17	13																		
18	14																		
19	15																		
20	16																		
21	17																		
22	18																		
23	19																		
24	20																		
25	21																		
26	22																		
27	23																		
28	Blank																		
29																			
30																			
31																			

BINARY TO HEXADECIMAL CONVERSION

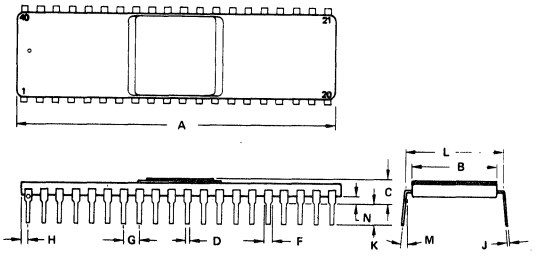
MSB			LSB	
0 D11 D7 D3	0 D10 D6 D2	D13 D9 D5 D1	D12 D8 D4 D0	Hexadecimal Character
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	A
1	0	1	1	B
1	1	0	0	C
1	1	0	1	D
1	1	1	0	E
1	1	1	1	F

$1 = V_{OL}$
$0 = V_{OH}$

3

PACKAGE DIMENSIONS

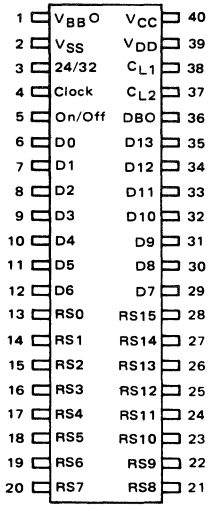
L SUFFIX
CERAMIC PACKAGE
CASE 699-04



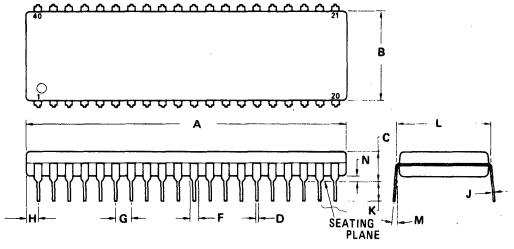
NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE, AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO INSIDE OF LEADS (MEASURED 0.51 mm (0.020) BELOW PACKAGE BASE)

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	50.04	51.05	1.970	2.010
B	13.46	14.22	0.530	0.560
C	3.05	3.94	0.120	0.155
D	0.38	0.51	0.015	0.020
F	0.89	1.40	0.035	0.055
G	2.54 BSC		0.100 BSC	
H	0.89	1.40	0.035	0.055
J	0.20	0.28	0.008	0.011
K	3.05	3.68	0.120	0.145
L	14.86	15.87	0.585	0.625
M	–	15°	–	15°
N	0.51	1.14	0.020	0.045

PIN ASSIGNMENT



P SUFFIX
PLASTIC PACKAGE
CASE 711-01



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	51.82	52.32	2.040	2.060
B	13.72	14.22	0.540	0.560
C	4.57	5.08	0.180	0.200
D	0.36	0.51	0.014	0.020
F	1.02	1.52	0.040	0.060
G	2.41	2.67	0.095	0.105
H	1.65	2.16	0.065	0.085
J	0.20	0.30	0.008	0.012
K	3.68	4.19	0.145	0.165
L	14.99	15.49	0.590	0.610
M	0°	10°	0°	10°
N	0.51	1.02	0.020	0.040

MCM6560
MCM6561
MCM6562

8192-BIT BINARY ADDRESSABLE READ ONLY MEMORIES

The MCM6560 is a mask programmable 8192-bit static Read Only Memory fabricated with N-Channel metal gate technology. A single mask provides memory organization and two programmable Chip Selects. The Chip Select decoding allows up to four MCM6560 devices to be wire-ORed without external decoding.

- Static Operation
- TTL Compatibility
- Compatible with CMOS Operating at 5.0 V
- 3-State Outputs for Wired-OR Capability
- Two Organizations: 1024 x 8 or 2048 x 4
- 350 ns Maximum Access Time
- Standard +5.0 V,+ 12 V and -3.0 V Power Supplies

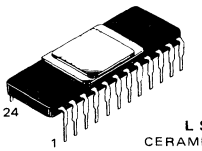
The MCM6561 and MCM6562 are organized as 1024 x 8 bits and pre-programmed with six character conversion codes: ASCII to Selectric, EBCDIC, and a modified 8-bit Hollerith; Selectric to ASCII, EBCDIC to ASCII, and a modified 8-bit Hollerith to ASCII.

Selectric is a registered trademark of IBM.

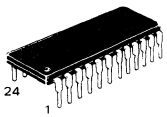
MOS

(N-CHANNEL, LOW THRESHOLD)

8K BINARY ADDRESSABLE READ ONLY MEMORIES



L SUFFIX
CERAMIC PACKAGE
CASE 684



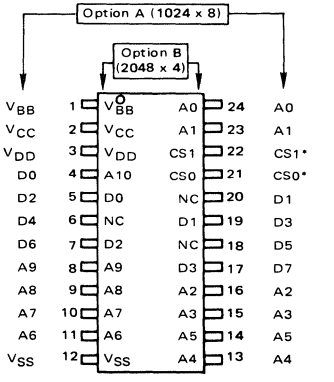
P SUFFIX
PLASTIC PACKAGE
CASE 709

ABSOLUTE MAXIMUM RATINGS[1] (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
Supply Voltages	V_{CC} V_{DD} V_{BB}	-0.3 to +6.0 -0.3 to +15 -10 to +0.3	Vdc
Address/Control Input Voltage	V_{in}	-0.3 to +15	Vdc
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-55 to +125	°C

NOTE 1: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

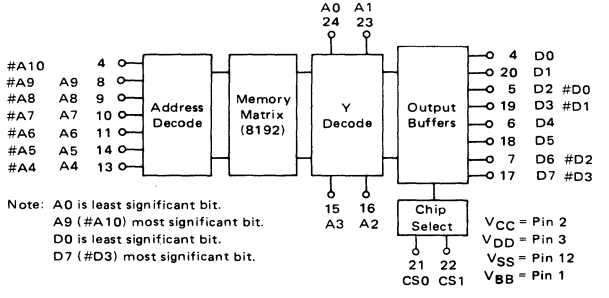
PIN ASSIGNMENT



*MCM6561 and MCM6562 are pre-programmed to be selected with a low input at CS.

BLOCK DIAGRAM

(8-OUTPUT OPTION) #(4-OUTPUT OPTION)



Note: A0 is least significant bit.
A9 (#A10) most significant bit.
D0 is least significant bit.
D7 (#D3) most significant bit.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted.)

RECOMMENDED DC OPERATING CONDITIONS (Referenced to V_{SS}).

Parameter	Symbol	Min	Nom	Max	Unit
Supply Voltage	V_{DD}	10.8	12	13.2	Vdc
	V_{CC}	4.75	5.0	5.25	Vdc
	V_{SS}	0	0	0	Vdc
	V_{BB}	-3.3	-3.0	-2.7	Vdc
Input Logic "1" Voltage (Driven by TTL)	V_{IH}*	3.0	–	V_{CC}	Vdc
(Driven by Other Than TTL)		4.0	–	V_{CC}	Vdc
Input Logic "0" Voltage	V_{IL}	0	–	0.8	Vdc

*A 4.0 V V_{IH} is required at the chip regardless of the type of driver used. However, internal MOS pullup devices on the chip can pull one TTL driver from 3.0 V to 4.0 V, without affecting access time. These pullup devices may not pull non-TTL drivers above 3.0 V.

DC CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit
Input Forward Current (V_{IL} = 0.4 Vdc)	I_{IL}	–	–	-1.6	mAdc
Input Leakage Current (V_{IH} = 5.25 Vdc, V_{CC} = 4.75 Vdc)	I_{IH}	–	–	100	μAdc
Output Leakage Current (High Impedance)	I_{OL}	–	–	10	μAdc
Output Low Voltage (I_{OL} = 1.6 mAdc)	V_{OL}	0	–	0.4	Vdc
Output High Voltage (I_{OH} = -40 μAdc)	V_{OH}	3.0	–	–	Vdc
Power Supply Current	I_{DD}	–	–	25	mAdc
	I_{CC}	–	–	125	mAdc
	I_{BB}	–	–	100	μAdc
Power Dissipation	P_D	–	600	1000	mW

CAPACITANCE (Periodically sampled rather than 100% tested)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Capacitance (f = 1.0 MHz)	C_{in}	–	4.0	7.0	pF
Output Capacitance (f = 1.0 MHz)	C_{out}	–	6.0	10	pF

AC CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted.)

[All timing with t_r,t_f = 20 ns; Load = 1 TTL Gate (MC7400 Series), C_L = 30 pF]

TIMING (Typical values measured at 25°C and nominal supplies)

Characteristic	Symbol	Min	Typ	Max	Unit
Address Access Time (See Figure 1A)	t_{acc}	–	225	350	ns
Output Select Time (See Figure 1B)	t_{OS}	–	100	150	ns
Output Deselect Time (See Figure 1B)	t_{OD}	–	100	150	ns

FIGURE 1 – TIMING DIAGRAMS

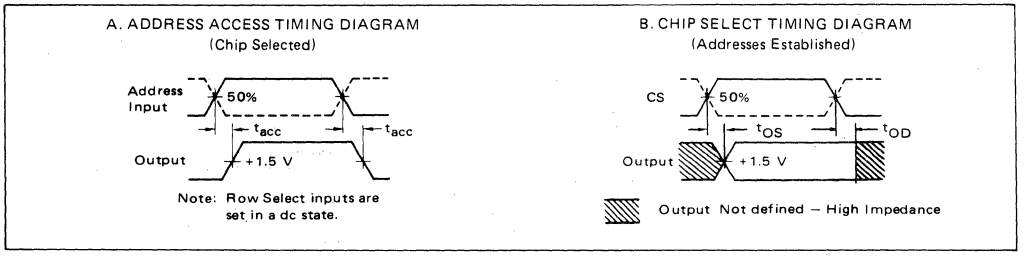


FIGURE 2 – V_{CC} SUPPLY CURRENT versus TEMPERATURE

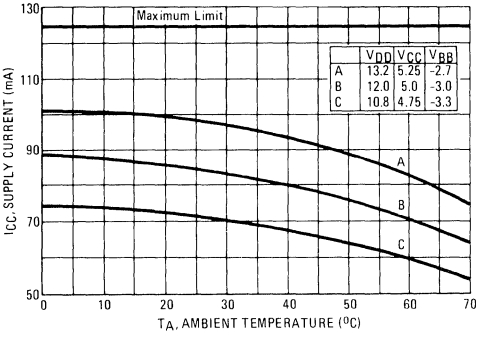


FIGURE 3 – V_{DD} SUPPLY CURRENT versus TEMPERATURE

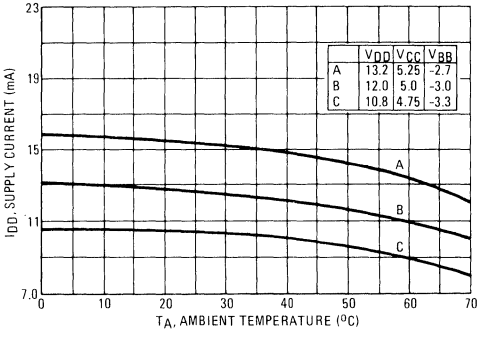


FIGURE 4 – OUTPUT SINK CURRENT versus OUTPUT VOLTAGE

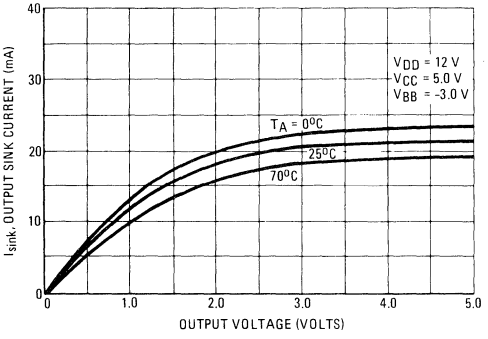


FIGURE 5 – OUTPUT SOURCE CURRENT versus OUTPUT VOLTAGE

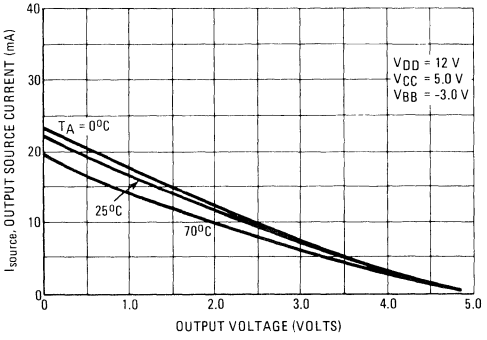


FIGURE 6 – ADDRESS ACCESS TIME versus V_{DD} SUPPLY VOLTAGE

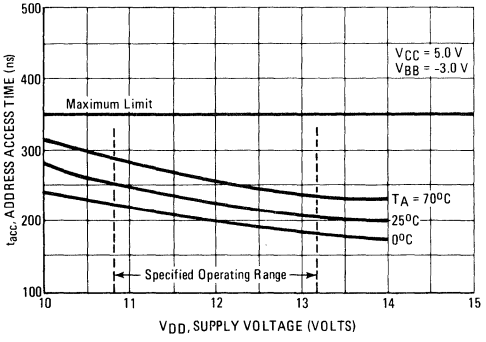
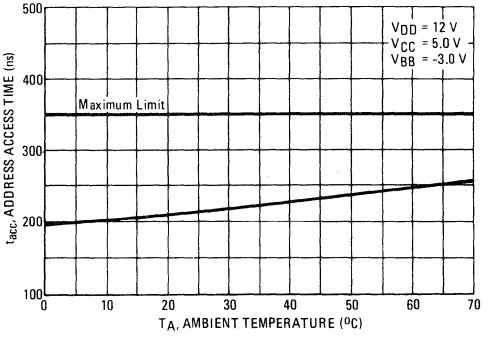


FIGURE 7 – ADDRESS ACCESS TIME versus TEMPERATURE



MEMORY OPERATION (Using Positive Logic)
Most positive level = 1, most negative level = 0

Address

To select any location, apply the appropriate binary code to the Address inputs A0 thru A9 (1024 x 8) or A10 (2048 x 4). The output data will remain valid as long as the Address and Chip Select (CS) inputs remain stable and valid.

Chip Select (CS) Inputs

Each CS input may be programmed for a don't care, logic "1", or logic "0" operation when the custom memory mask is generated. The CS inputs enable the output devices and give valid output data when they are at the programmed logic level. With the CS inputs at a false logic level, the outputs assume a high impedance state. By programming the CS inputs, up to four MCM6560 devices may be operated in parallel without adding external circuitry.

Address Access Time, t_{acc}

The time delay between the latest change in any Address input and the corresponding change on any Output line with all other inputs held stable and the chip selected.

Output Select Time, t_{OS}

The time delay between activation of CS inputs and the appearance of valid data on any Output line with all other inputs held stable.

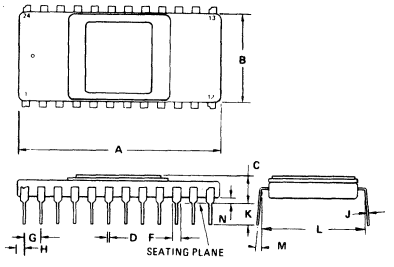
Output

For these devices positive logic levels are assumed. When the outputs are disabled, a high impedance state is present.

3

PACKAGE DIMENSIONS

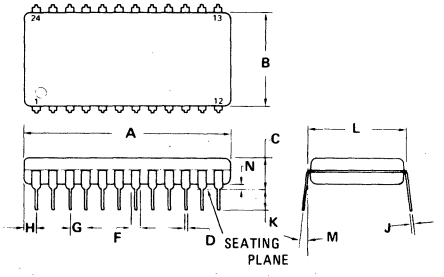
L SUFFIX
CERAMIC PACKAGE
CASE 684-04



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	29.34	30.86	1.155	1.215
B	12.70	14.22	0.500	0.560
C	3.05	3.94	0.120	0.155
D	0.38	0.51	0.015	0.020
F	0.89	1.40	0.035	0.055
G	2.54 BSC		0.100 BSC	
H	0.89	1.40	0.035	0.055
J	0.20	0.30	0.008	0.012
K	2.92	3.68	0.115	0.145
L	14.86	15.87	0.585	0.625
M	–	15°	–	15°
N	0.51	1.14	0.020	0.045

NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE WITH MAXIMUM MATERIAL CONDITION.
2. LEAD NO. 1 CUT FOR IDENTIFICATION, OR BUMP ON TOP.
3. DIM "L" TO INSIDE OF LEADS. (MEASURED 0.51 mm (0.020) BELOW PKG BASE)

P SUFFIX
PLASTIC PACKAGE
CASE 709-01



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	31.37	32.13	1.235	1.265
B	13.72	14.22	0.540	0.560
C	4.57	5.08	0.180	0.200
D	0.36	0.51	0.014	0.020
F	1.02	1.52	0.040	0.060
G	2.41	2.67	0.095	0.105
H	1.78	2.03	0.070	0.080
J	0.20	0.30	0.008	0.012
K	3.05	3.56	0.120	0.140
L	14.73	15.24	0.580	0.600
M	0°	10°	0°	10°
N	0.51	1.02	0.020	0.040

NOTES:
1. LEADS, TRUE POSITIONED WITHIN 0.25 mm (0.010) DIA AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION. (DIM. "D")
2. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.

CUSTOM PROGRAMMING FOR MCM6560

By the programming of a single photomask for the MCM6560, the customer may specify the pin assignment option (1024 x 8 or 2048 x 4), the content of the memory and the method of selecting the outputs.

Information for custom memory content may be sent to Motorola in the following forms, in order of preference:*

1. Hexadecimal coding using IBM Punch Cards (Figures 8 and 11).
2. Hexadecimal coding using ASCII Paper Tape Punch (Figures 9 thru 11).

As Figure 11 indicates, a zero programmed in the memory appears at D_n as V_{OL}. A programmed one appears as V_{OH}.

To specify the pin assignment option and to program the mode of selecting the chip, the information in Figure 12 is required. This information must be in written form and must accompany the punched cards or paper tape. (A copy of Figure 12 may be used for this purpose.) For example, the MCM6561L is pre-programmed to pinout option A and true Chip Select option I.

*Note: Motorola can accept magnetic tape and truth table formats. For further information contact your local Motorola sales representative.

FIGURE 8 – CARD PUNCH FORMAT

Columns	
12 - - 75	Hexadecimal data coding
77 - - 78	Card number (starting 01)
79 - - 80	Total number of cards (32)

Option A (1024 x 8)

Column 12 on the first card contains the hexadecimal equivalent of bits D7 thru D4 of byte 0, while column 13 contains the hexadecimal equivalent of bits D3 thru D0. Columns 14 and 15 contain byte 1, columns 16 and 17 byte 2, and so on.

The first card contains the first 32 bytes. Columns 12 and 13 on the second card will contain byte 32 (the 33rd byte). A total of 32 cards will contain 1024 bytes of 8-bits.

Option B (2048 x 4)

Column 12 on the first card contains the hexadecimal equivalent of byte 0, bits D3 thru D0. Column 13 contains the hexadecimal equivalent of byte 1, column 14 byte 2, and so on.

The first card contains the first 64 bytes. Column 12 on the second card will contain byte 64 (the 65th byte). A total of 32 cards will contain 2048 bytes of 4 bits.

FIGURE 9 – PAPER TAPE FORMAT

Frames	
Leader	Blank Tape
1 to M	Allowed for customer use ($M \leqslant 64$)
M + 1, M + 2	CR; LF (Carriage Return; Line Feed)
M + 3 to M + 66	First line of pattern information (64 hex figures per line)
M + 67, M + 68	CR; LF
M + 69 to M + 2112	Remaining 31 lines of hex figures, each line followed by a Carriage Return and Line Feed

Blank Tape

Frames 1 to M are left to the customer for internal identification, where $M \leqslant 64$. Any combination of alphanumerics may be used. This information is terminated with a Carriage Return and Line Feed, delineating the start of data entry. (Note that the tape cannot begin with a CR and/or LF, or the customer identification will be assumed to be programming data.)

Option A (1024 x 8)

Frame M + 3 contains the hexadecimal equivalent of bits D7 thru D4 of byte 0. Frame M + 4 contains bits D3 thru D0. These two hex figures together program byte 0. Likewise, frames M + 5 and M + 6 program byte 1, while M + 7 and M + 8 program byte 2. Frames M + 3 to M + 66 comprise the first line of the printout and program, in sequence, the first 32 bytes of storage. The line is terminated with a CR and LF.

Option B (2048 x 4)

Frame M + 3 contains the hexadecimal equivalent of byte 0, bits D3 thru D0. Frame M + 4 contains byte 1, frame M + 5 byte 2, and so on. Frames M + 3 to M + 66 sequentially program bytes 0 to 31 (the first 32 bytes). The line is terminated with a CR and LF.

Both Options

The remaining 31 lines of data are punched in sequence using the same format, each line terminated with a CR and LF. The total 32 lines of data contain 32 x 64 or 2048 characters. Since each character programs 4 bits of information, a full 8192 bits are programmed.

As an example, a printout of the punched tape for Figure 13 would read as shown in Figure 10 (a CR and LF is implicit at the end of each line).

FIGURE 10 – PRINTOUT OF PUNCHED TAPE

```
CUSTOMER IDENTIFICATION USING ONLY ALPHANUMERIC CHARACTERS
A0B1B23335B736B8B430FA3912938E847478EEF565E4EB636CE81EE29A0A031B
21ED2EF6277269E16FF38B77998D08006AE7BD66F0BB71ACAFF91E2D140987FF
A07DC0A3A5A6BEAA24A95A2812110584D4D64E55C5444BC3CC481E429C0A1790
3C4D2E5622D2C941CF530CD71D8D8600CA472BC6503AD1AC3F591E5F14090F00
```

FIGURE 11 – BINARY TO HEXADECIMAL CONVERSION

$0 = V_{OL}$
$1 = V_{OH}$

MSB D7	D6	D5	LSB D4	Hexadecimal
D3	D2	D1	D0	Character
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	A
1	0	1	1	B
1	1	0	0	C
1	1	0	1	D
1	1	1	0	E
1	1	1	1	F

FIGURE 12 – FORMAT FOR PROGRAMMING GENERAL OPTIONS

ORGANIZATIONAL DATA
MCM6560 MOS READ ONLY MEMORY

Customer _____

Customer Part No. _____ Rev. _____

Pin-Out Option: ☐ A (1024 x 8)

☐ B (2048 x 4)

True Chip Select options:

	CS1	CS0	
I	0	0	☐
II	0	1	☐
III	1	0	☐
IV	1	1	☐
V	X	1	☐
VI	X	0	☐
VII	X	X	☐

1 is most positive input
0 is most negative input
X is no connection or don't care situation

MCM6561 and MCM6562 CODE CONVERSION

The MCM6561 and MCM6562 binary ROMs are organized as 1024 words of 8 bits. The devices are pre-programmed and contain the code conversions shown to the right. CS0 = CS1 = 0.

ADDRESS (A)		CODES	
From	To	From	To
0	127	Selectric	ASCII
128	255	ASCII	Selectric
256	511	Hollerith	ASCII
512	639	ASCII	Hollerith
640	895	EBCDIC	ASCII
896	1023	ASCII	EBCDIC

Tables 13 through 18 present the coding used in the MCM6561 and MCM6562. The addresses are given both in decimal and hexadecimal form in these figures. The outputs are given in hexadecimal form only. The format is illustrated in the example to the right.

Example:

Address		Output
	A 10 . . . A0	D7 . . . D0
23_{10}	00000010111_2	01100011_2
23_{10}	17_{16}	63_{16}

Table Format

FIGURE 13 – SELECTRIC LINE CODE TO ASCII CODE

Address		Output MCM6561 MCM6562	Address		Output MCM6561 MCM6562	Address		Output MCM6561 MCM6562	Address		Output MCM6561 MCM6562
0	0	A0	32	20	21	64	40	A0	96	60	3C
1	1	B1	33	21	ED	65	41	7D	97	61	4D
2	2	B2	34	22	2E	66	42	C0	98	62	2E
3	3	33	35	23	F6	67	43	A3	99	63	56
4	4	35	36	24	27	68	44	A5	100	64	22
5	5	B7	37	25	72	69	45	A6	101	65	D2
6	6	36	38	26	69	70	46	BE	102	66	C9
7	7	B8	39	27	E1	71	47	AA	103	67	41
8	8	B4	40	28	6F	72	48	24	104	68	CF
9	9	30	41	29	F3	73	49	A9	105	69	53
10	A	FA	42	2A	8B	74	4A	5A	106	6A	0C
11	B	39	43	2B	77	75	4B	28	107	6B	D7
12	C	12	44	2C	99	76	4C	12	108	6C	1D
13	D	93	45	2D	8D	77	4D	11	109	6D	8D
14	E	8E	46	2E	08	78	4E	05	110	6E	88
15	F	84	47	2F	00	79	4F	84	111	6F	00
16	10	74	48	30	6A	80	50	D4	112	70	CA
17	11	78	49	31	E7	81	51	D8	113	71	47
18	12	EE	50	32	BD	82	52	4E	114	72	2B
19	13	F5	51	33	66	83	53	55	115	73	C6
20	14	65	52	34	F0	84	54	C5	116	74	50
21	15	E4	53	35	BB	85	55	44	117	75	3A
22	16	EB	54	36	71	86	56	4B	118	76	D1
23	17	63	55	37	AC	87	57	C3	119	77	AC
24	18	6C	56	38	AF	88	58	CC	120	78	3F
25	19	E8	57	39	F9	89	59	48	121	79	59
26	1A	1E	58	3A	1E	90	5A	1E	122	7A	1E
27	1B	E2	59	3B	2D	91	5B	42	123	7B	5F
28	1C	9A	60	3C	14	92	5C	9C	124	7C	14
29	1D	0A	61	3D	09	93	5D	0A	125	7D	09
30	1E	03	62	3E	87	94	5E	17	126	7E	0F
31	1F	1B	63	3F	FF	95	5F	90	127	7F	00

FIGURE 14 – ASCII TO SELECTRIC LINE CODE

Address		Output MCM6561 MCM6562	Address		Output MCM6561 MCM6562	Address		Output MCM6561 MCM6562	Address		Output MCM6561 MCM6562
128	80	AF	160	A0	00	192	C0	42	224	E0	77
129	81	1B	161	A1	A0	193	C1	E7	225	E1	27
130	82	8B	162	A2	E4	194	C2	DB	226	E2	1B
131	83	1E	163	A3	C3	195	C3	D7	227	E3	17
132	84	0F	164	A4	48	196	C4	55	228	E4	95
133	85	4E	165	A5	44	197	C5	D4	229	E5	14
134	86	BB	166	A6	C5	198	C6	F3	230	E6	33
135	87	BE	167	A7	24	199	C7	71	231	E7	B1
136	88	2E	168	A8	4B	200	C8	59	232	E8	99
137	89	BD	169	A9	C9	201	C9	66	233	E9	A6
138	8A	1D	170	AA	47	202	CA	F0	234	EA	30
139	8B	AA	171	AB	72	203	CB	56	235	EB	96
140	8C	6A	172	AC	B7	204	CC	D8	236	EC	18
141	8D	2D	173	AD	BB	205	CD	E1	237	ED	21
142	8E	8E	174	AE	E2	206	CE	D2	238	EE	12
143	8F	7E	175	AF	B8	207	CF	E8	239	EF	28
144	90	5F	176	B0	09	208	D0	74	240	F0	B4
145	91	4D	177	B1	81	209	D1	F6	241	F1	36
146	92	0C	178	B2	82	210	D2	65	242	F2	A5
147	93	8D	179	B3	03	211	D3	69	243	F3	A9
148	94	3C	180	B4	88	212	D4	50	244	F4	90
149	95	A0	181	B5	84	213	D5	53	245	F5	93
150	96	6F	182	B6	06	214	D6	63	246	F6	A3
151	97	DE	183	B7	05	215	D7	EB	247	F7	2B
152	98	A0	184	B8	87	216	D8	D1	248	F8	11
153	99	AC	185	B9	8B	217	D9	F9	249	F9	39
154	9A	9C	186	BA	F5	218	DA	CA	250	FA	0A
155	9B	9F	187	BB	35	219	DB	41	251	FB	41
156	9C	5C	188	BC	60	220	DC	41	252	FC	41
157	9D	6C	189	BD	B2	221	DD	41	253	FD	41
158	9E	6C	190	BE	C6	222	DE	41	254	FE	41
159	9F	5C	191	BF	78	223	DF	7B	255	FF	3F

FIGURE 15 – MODIFIED 8-BIT HOLLERITH TO ASCII

Address		Output MCM6561	Output MCM6562	Address		Output MCM6561	Output MCM6562	Address		Output MCM6561	Output MCM6562	Address		Output MCM6561	Output MCM6562
256	100	20	20	274	112	16	16	292	124	55	55	310	136	17	17
257	101	31	31	275	113	93	97	293	125	56	56	311	137	1B	1B
258	102	32	32	276	114	94	94	294	126	57	57	312	138	88	90
259	103	33	33	277	115	95	1E	295	127	58	58	313	139	89	91
260	104	34	34	278	116	96	99	296	128	59	59	314	13A	8A	92
261	105	35	35	279	117	04	04	297	129	B9	B9	315	13B	8B	93
262	106	36	36	280	118	98	9A	298	12A	5C	5C	316	13C	8C	94
263	107	37	37	281	119	99	9B	299	12B	2C	2C	317	13D	05	05
264	108	38	38	282	11A	9A	9C	300	12C	25	25	318	13E	06	06
265	109	60	60	283	11B	9B	9D	301	12D	5F	5F	319	13F	07	07
266	10A	3A	3A	284	11C	14	14	302	12E	3E	3E	320	140	2D	2D
267	10B	23	23	285	11D	15	15	303	12F	3F	3F	321	141	4A	4A
268	10C	40	40	286	11E	9E	9E	304	130	5A	5A	322	142	4B	4B
269	10D	27	27	287	11F	1A	1A	305	131	81	8D	323	143	4C	4C
270	10E	3D	3D	288	120	30	30	306	132	82	1C	324	144	4D	4D
271	10F	22	22	289	121	2F	2F	307	133	83	8E	325	145	4E	4E
272	110	39	39	290	122	53	53	308	134	84	8F	326	146	4F	4F
273	111	91	96	291	123	54	54	309	135	0A	0A	327	147	50	50

(continued)

FIGURE 15 – MODIFIED 8-BIT HOLLERITH TO ASCII (continued)

Address		Output		Address		Output		Address		Output		Address		Output	
		MCM6561	MCM6562			MCM6561	MCM6562			MCM6561	MCM6562			MCM6561	MCM6562
328	148	51	51	374	176	B6	B6	420	1A4	64	64	466	1D2	AA	AA
329	149	B1	B1	375	177	B7	B7	421	1A5	65	65	467	1D3	AB	AB
330	14A	5D	21	376	178	B8	B8	422	1A6	66	66	468	1D4	AC	AC
331	14B	24	24	377	179	80	8C	423	1A7	67	67	469	1D5	AD	AD
332	14C	2A	2A	378	17A	F4	F4	424	1A8	68	68	470	1D6	AE	AE
333	14D	29	29	379	17B	F5	F5	425	1A9	C3	C4	471	1D7	AF	AF
334	14E	3B	3B	380	17C	F6	F6	426	1AA	C4	C5	472	1D8	B0	B0
335	14F	5E	5E	381	17D	F7	F7	427	1AB	C5	C6	473	1D9	00	10
336	150	52	52	382	17E	F8	F8	428	1AC	C6	C7	474	1DA	EE	ED
337	151	11	11	383	17F	F9	F9	429	1AD	C7	C8	475	ADB	EF	EE
338	152	12	12	384	180	26	26	430	1AE	C8	C9	476	1DC	F0	EF
339	153	13	13	385	181	41	41	431	1AF	C9	CA	477	1DD	F1	F0
340	154	9D	85	386	182	42	42	432	1B0	69	69	478	1DE	F2	F1
341	155	85	86	387	183	43	43	433	1B1	A0	9F	479	1DF	F3	F2
342	156	08	08	388	184	44	44	434	1B2	A1	A0	480	1E0	BA	BB
343	157	87	87	389	185	45	45	435	1B3	A2	A1	481	1E1	D9	D9
344	158	18	18	390	186	46	46	436	1B4	A3	A2	482	1E2	DA	DA
345	159	19	19	391	187	47	47	437	1B5	A4	A3	483	1E3	DB	DB
346	15A	92	88	392	188	48	48	438	1B6	A5	A4	484	1E4	DC	DC
347	15B	8F	89	393	189	A8	A7	439	1B7	A6	A5	485	1E5	DD	DD
348	15C	1C	8A	394	18A	5B	A8	440	1B8	A7	A6	486	1E6	DE	DE
349	15D	1D	1D	395	18B	2E	2E	441	1B9	10	00	487	1E7	DF	DF
350	15E	1E	8B	396	18C	3C	3C	442	1BA	E8	E7	488	1E8	E0	E0
351	15F	1F	1F	397	18D	28	28	443	1BB	E9	E8	489	1E9	D8	D8
352	160	7D	7D	398	18E	2B	2B	444	1BC	EA	E9	490	1EA	E2	E2
353	161	7E	7E	399	18F	21	7C	445	1BC	EB	EA	491	1EB	E3	E3
354	162	73	73	400	190	49	49	446	1BE	EC	EB	492	1EC	E4	E4
355	163	74	74	401	191	01	01	447	1BF	ED	EC	493	1ED	E5	5D
356	164	75	75	402	192	02	02	448	1C0	7C	BA	494	1EE	E6	E5
357	165	76	76	403	193	03	03	449	1C1	6A	6A	495	1EF	E7	E6
358	166	77	77	404	194	9C	80	450	1C2	6B	6B	496	1F0	E1	E1
359	167	78	78	405	195	09	09	451	1C3	6C	6C	497	1F1	BB	BC
360	168	79	79	406	196	86	81	452	1C4	6D	6D	498	1F2	BC	BD
361	169	D1	D2	407	197	7F	7F	453	1C5	6E	6E	499	1F3	BD	BE
362	16A	D2	D3	408	198	97	82	454	1C6	6F	6F	500	1F4	BE	BF
363	16B	D3	D4	409	199	8D	83	455	1C7	70	70	501	1F5	BF	C0
364	16C	D4	D5	410	19A	8E	84	456	1C8	71	71	502	1F6	C0	C1
365	16D	D5	5B	411	19B	0B	0B	457	1C9	CA	CB	503	1F7	C1	C2
366	16E	D6	D6	412	19C	0C	0C	458	1CA	CB	CC	504	1F8	C2	C3
367	16F	D7	D7	413	19D	0D	0D	459	1CB	CC	CD	505	1F9	90	95
368	170	7A	7A	414	19F	0E	0E	460	1CC	CD	CE	506	1FA	FA	FA
369	171	9F	F3	415	19F	0F	0F	461	1CD	2E	CF	507	1FB	FB	FB
370	172	B2	B2	416	1A0	7B	7B	462	1CE	CF	D0	508	1FC	FC	FC
371	173	B3	B3	417	1A1	61	61	463	1CF	D0	D1	509	1FD	FD	FD
372	174	B4	B4	418	1A2	62	62	464	1D0	72	72	510	1FE	FE	FE
373	175	B5	B5	419	1A3	63	63	465	1D1	A9	A9	511	1FF	FF	FF

FIGURE 16 – ASCII TO MODIFIED 8-BIT HOLLERITH

Address		Output		Address		Output		Address		Output		Address		Output	
		MCM6561	MCM6562			MCM6561	MCM6562			MCM6561	MCM6562			MCM6561	MCM6562
512	200	D9	B9	523	20B	9B	9B	534	216	82	12	545	221	1F	4A
513	201	91	91	524	20C	9C	9C	535	217	C6	36	546	222	0F	0F
514	202	92	92	525	20D	9D	9D	536	218	A8	58	547	223	0B	0B
515	203	93	93	526	20E	9E	9E	537	219	A9	59	548	224	2B	4B
516	204	87	17	527	20F	9F	9F	538	21A	8F	1F	549	225	4C	2C
517	205	CD	3D	528	210	B9	D9	539	21B	C7	37	550	226	10	80
518	206	CE	3E	529	211	A1	51	540	21C	AC	32	551	227	0D	0D
519	207	CF	3F	530	212	A2	52	541	21D	AD	5D	552	228	1D	8D
520	208	A6	56	531	213	A3	53	542	21E	AE	15	553	229	2D	4D
521	209	95	95	532	214	8C	1C	543	21F	AF	5F	554	22A	2C	4C
522	20A	C5	35	533	215	8D	1D	544	220	00	00	555	22B	1E	8E

(continued)

FIGURE 16 – ASCII TO MODIFIED 8-BIT HOLLERITH (continued)

Address		Output		Address		Output		Address		Output		Address		Output	
		MCM6561	MCM6562			MCM6561	MCM6562			MCM6561	MCM6562			MCM6561	MCM6562
556	22C	4B	2B	577	241	11	81	598	256	45	25	619	26B	32	C2
557	22D	20	40	578	242	12	82	599	257	46	26	620	26C	33	C3
558	22E	1B	8B	579	243	13	83	600	258	47	27	621	26D	34	C4
559	22F	41	21	580	244	14	84	601	259	48	28	622	26E	35	C5
560	230	40	20	581	245	15	85	602	25A	C0	30	623	26F	36	C6
561	231	01	01	582	246	16	86	603	25B	1A	60	624	270	37	C7
562	232	02	02	583	247	17	87	604	25C	4A	2A	625	271	38	C8
563	233	03	03	584	248	18	88	605	25D	2A	ED	626	272	B0	D0
564	234	04	04	585	249	90	90	606	25E	2F	4F	627	273	62	62
565	235	05	05	586	24A	21	41	607	25F	4D	2D	628	274	63	63
566	236	06	06	587	24B	22	42	608	260	09	09	629	275	64	64
567	237	07	07	588	24C	23	43	609	261	51	A1	630	276	65	65
568	238	08	08	589	24D	24	44	610	262	52	A2	631	277	66	66
569	239	80	10	590	24E	25	45	611	263	53	A3	632	278	67	67
570	23A	0A	0A	591	24F	26	46	612	264	54	A4	633	279	68	68
571	23B	2E	4E	592	250	27	47	613	265	55	A5	634	27A	E0	70
572	23C	1C	8C	593	251	28	48	614	266	56	A6	635	27B	50	A0
573	23D	0E	0E	594	252	A0	50	615	267	57	A7	636	27C	30	8F
574	23E	4E	2E	595	253	42	22	616	268	58	A8	637	27D	60	60
575	23F	4F	2F	596	254	43	23	617	269	D0	B0	638	27E	61	61
576	240	0C	0C	597	255	44	24	618	26A	31	C1	639	27F	97	97

FIGURE 17 – EBCDIC TO ASCII

Address		Output		Address		Output		Address		Output		Address		Output	
		MCM6561	MCM6562			MCM6561	MCM6562			MCM6561	MCM6562			MCM6561	MCM6562
640	280	00	00	677	2A5	0A	0A	714	2CA	FE	A8	751	2EF	BF	3F
641	281	01	01	678	2A6	17	17	715	2CB	AE	2E	752	2F0	00	BB
642	282	02	02	679	2A7	1B	1B	716	2CC	BC	3C	753	2F1	00	BC
643	283	03	03	680	2A8	00	90	717	2CD	A8	28	754	2F2	00	BD
644	284	00	80	681	2A9	00	91	718	2CE	AB	2B	755	2F3	00	BE
645	285	09	09	682	2AA	00	92	719	2CF	FC	7C	756	2F4	00	BF
646	286	00	81	683	2AB	00	93	720	2D0	A6	26	757	2F5	00	C0
647	287	7F	7F	684	2AC	00	94	721	2D1	00	A9	758	2F6	00	C1
648	288	00	82	685	2AD	05	05	722	2D2	00	AA	759	2F7	00	C2
649	289	00	83	686	2AE	06	06	723	2D3	00	AB	760	2F8	00	C3
650	28A	00	84	687	2AF	07	07	724	2D4	00	AC	761	2F9	00	60
651	28B	0B	0B	688	2B0	00	95	725	2D5	00	AD	762	2FA	BA	3A
652	28C	0C	0C	689	2B1	00	96	726	2D6	00	AE	763	2FB	A3	23
653	28D	0D	0D	690	2B2	16	16	727	2D7	00	AF	764	2FC	C0	40
654	28E	0E	0E	691	2B3	00	97	728	2D8	00	B0	765	2FD	A7	27
655	28F	0F	0F	692	2B4	00	98	729	2D9	00	B1	766	2FE	BD	3D
656	290	10	10	693	2B5	14	1E	730	2DA	A1	21	767	2FF	A2	22
657	291	11	11	694	2B6	00	99	731	2DB	A4	24	768	300	00	C4
658	292	12	12	695	2B7	04	04	732	2DC	AA	2A	769	301	E1	61
659	293	13	13	696	2B8	00	9A	733	2DD	A9	29	770	302	E2	62
660	294	E0	85	697	2B9	00	9B	734	2DE	BB	2B	771	303	E3	63
661	295	DC	86	698	2BA	00	9C	735	2DF	DE	5E	772	304	E4	64
662	296	08	08	699	2BB	00	9D	736	2E0	AD	2D	773	305	E5	65
663	297	00	87	700	2BC	00	14	737	2E1	AF	2F	774	306	E6	66
664	298	18	18	701	2BD	15	15	738	2E2	00	B2	775	307	E7	67
665	299	19	19	702	2BE	00	9E	739	2E3	00	B3	776	308	E8	68
666	29A	00	88	703	2BF	1A	1A	740	2E4	00	B4	777	309	E9	69
667	29B	00	89	704	2C0	A0	20	741	2E5	00	B5	778	30A	00	C5
668	29C	1C	8A	705	2C1	00	9F	742	2E6	00	B6	779	30B	FB	C6
669	29D	1D	1D	706	2C2	00	A0	743	2E7	00	B7	780	30C	00	C7
670	29E	1E	8B	707	2C3	00	A1	744	2F8	00	B8	781	30D	00	C8
671	29F	1F	1F	708	2C4	00	A2	745	2E9	00	B9	782	30E	00	C9
672	2A0	00	8C	709	2C5	00	A3	746	2EA	00	BA	783	30F	00	CA
673	2A1	00	8D	710	2C6	00	A4	747	2EB	AC	2C	784	310	00	CB
674	2A2	00	2C	711	2C7	00	A5	748	2EC	A5	25	785	311	EA	6A
675	2A3	00	8E	712	2C8	00	A6	749	2ED	DF	5F	786	312	EB	6B
676	2A4	00	8F	713	2C9	00	A7	750	2EE	BE	3E	787	313	EC	6C

(continued)

FIGURE 17 – EBCDIC TO ASCII (continued)

Address		Output MCM6561	Output MCM6562	Address		Output MCM6561	Output MCM6562	Address		Output MCM6561	Output MCM6562	Address		Output MCM6561	Output MCM6562
788	314	ED	6D	815	32F	00	D7	842	34A	00	E7	869	365	D6	56
789	315	EE	6E	816	330	00	D8	843	34B	00	E8	870	366	D7	57
790	316	EF	6F	817	331	00	D9	844	34C	00	E9	871	367	D8	58
791	317	F0	70	818	332	00	DA	845	34D	00	EA	872	368	D9	59
792	318	F1	71	819	333	00	DB	846	34E	00	EB	873	369	DA	5A
793	319	F2	72	820	334	00	DC	847	34F	00	EC	874	36A	00	F4
794	31A	00	CC	821	335	00	DD	848	350	00	7D	875	36B	00	F5
795	31B	FD	CD	822	336	00	DE	849	351	CA	4A	876	36C	00	F6
795	31C	00	CE	823	337	00	DF	850	352	CB	4B	877	36D	00	F7
797	31D	00	CF	824	338	00	E0	851	353	CC	4C	878	36E	00	F8
798	31E	00	D0	825	339	00	E1	852	354	CD	4D	879	36F	00	F9
799	31F	00	D1	826	33A	00	E2	853	355	CE	4E	880	370	B0	30
800	320	00	D2	827	33B	00	E3	854	356	CF	4F	881	371	B1	31
801	321	00	7E	828	33C	00	E4	855	357	D0	50	882	372	B2	32
802	322	F3	73	829	33D	DD	5D	856	358	D1	51	883	373	B3	33
803	323	F4	74	830	33E	00	E5	857	359	D2	52	884	374	B4	34
804	324	F5	75	831	33F	00	E6	858	35A	00	ED	885	375	B5	35
805	325	F6	76	832	340	00	7B	859	35B	00	EE	886	376	B6	36
806	326	F7	77	833	341	C1	41	860	35C	00	EF	887	377	B7	37
807	327	F8	78	834	342	C2	42	861	35D	00	F0	888	378	B8	38
808	328	F9	79	835	343	C3	43	862	35E	00	F1	889	379	B9	39
809	329	FA	7A	836	344	C4	44	863	35F	00	F2	890	37A	00	FA
810	32A	00	D3	837	345	C5	45	864	360	00	5C	891	37B	00	FB
811	32B	00	D4	838	346	C6	46	865	361	00	F3	892	37C	00	FC
812	32C	00	D5	839	347	C7	47	866	362	D3	53	893	37D	00	FD
813	32D	DB	5B	840	348	C8	48	867	363	D4	54	894	37E	00	FE
814	32E	00	D6	841	349	C9	49	868	364	D5	55	895	37F	00	FF

FIGURE 18 – ASCII TO EBCDIC

Address		Output MCM6561	Output MCM6562	Address		Output MCM6561	Output MCM6562	Address		Output MCM6561	Output MCM6562	Address		Output MCM6561	Output MCM6562
896	380	00	00	928	3A0	40	40	960	3C0	7C	7C	992	3E0	14	79
897	381	01	01	929	3A1	5A	5A	961	3C1	C1	C1	993	3E1	81	81
898	382	02	02	930	3A2	7F	7F	962	3C2	C2	C2	994	3E2	82	82
899	383	03	03	931	3A3	7B	7B	963	3C3	C3	C3	995	3E3	83	83
900	384	37	37	932	3A4	5B	5B	964	3C4	C4	C4	996	3E4	84	84
901	385	2D	2D	933	3A5	6C	6C	965	3C5	C5	C5	997	3E5	85	85
902	386	2E	2E	934	3A6	50	50	966	3C6	C6	C6	998	3E6	86	86
903	387	2F	2F	935	3A7	7D	7D	967	3C7	C7	C7	999	3E7	87	87
904	388	16	16	936	3A8	4D	4D	968	3C8	C8	C8	1000	3E8	88	88
905	389	05	05	937	3A9	5D	5D	969	3C9	C9	C9	1001	3E9	89	89
906	38A	25	25	938	3AA	5C	5C	970	3CA	D1	D1	1002	3EA	91	91
907	38B	0B	0B	939	3AB	4E	4E	971	3CB	D2	D2	1003	3EB	92	92
908	38C	0C	0C	940	3AC	6B	6B	972	3CC	D3	D3	1004	3EC	93	93
909	38D	0D	0D	941	3AD	60	60	973	3CD	D4	D4	1005	3ED	94	94
910	38E	0E	0E	942	3AE	4B	4B	974	3CE	D5	D5	1006	3EE	95	95
911	38F	0F	0F	943	3AF	61	61	975	3CF	D6	D6	1007	3EF	96	96
912	390	10	10	944	3B0	F0	F0	976	3D0	D7	D7	1008	3F0	97	97
913	391	11	11	945	3B1	F1	F1	977	3D1	D8	D8	1009	3F1	98	98
914	392	12	12	946	3B2	F2	F2	978	3D2	D9	D9	1010	3F2	99	99
915	393	13	13	947	3B3	F3	F3	979	3D3	E2	E2	1011	3F3	A2	A2
916	394	35	35	948	3B4	F4	F4	980	3D4	E3	E3	1012	3F4	A3	A3
917	395	3D	3D	949	3B5	F5	F5	981	3D5	E4	E4	1013	3F5	A4	A4
918	396	32	32	950	3B6	F6	F6	982	3D6	E5	E5	1014	3F6	A5	A5
919	397	26	26	951	3B7	F7	F7	983	3D7	E6	E6	1015	3F7	A6	A6
920	398	18	18	952	3B8	F8	F8	984	3D8	E7	E7	1016	3F8	A7	A7
921	399	19	19	953	3B9	F9	F9	985	3D9	E8	E8	1017	3F9	A8	A8
922	39A	3F	3F	954	3BA	7A	7A	986	3DA	E9	E9	1018	3FA	A9	A9
923	39B	24	27	955	3BB	5E	5E	987	3DB	A9	AD	1019	3FB	8B	C0
924	39C	1C	22	956	3BC	4C	4C	988	3DC	15	E0	1020	3FC	4F	4F
925	39D	1D	1D	957	3BD	7E	7E	989	3DD	BD	BD	1021	3FD	9B	D0
926	39E	1E	35	958	3BE	6E	6E	990	3DE	5F	5F	1022	3FE	4A	A1
927	39F	1F	1F	959	3BF	6F	6F	991	3DF	6D	6D	1023	3FF	07	07

APPLICATIONS INFORMATION

The Selectric code contained in the MCM6561/62 is the IBM Correspondence Selectric Line Code. This code, which is defined by bits B, A, 8, 4, 2, 1, is transmitted over the telephone line by the IBM Selectric Terminal #2741. If the typewriter bail code (R1, R2, R2A, R5, T1, T2) is required, then it is necessary to convert the Selectric code to bail and vice versa as shown in Figures 19 and 20.

The EBCDIC to ASCII code converter requires an inverter gate on address A7 as shown in Figure 21.

To accommodate the full 12-bit Hollerith to ASCII code conversion, the MCM6561/62 requires additional logic to condense the first 7 address bits of the Hollerith code into the 3 least significant address bits of the ROM as given in Figure 22. Figure 23 illustrates how the 8 output bits of the ROM can be converted to the 12-bit Hollerith code by employing a standard decoder (MC4006).

The MCM6560-62 requires three power supplies: -3.0 volts, +5.0 volts, and +12 volts. The memory requires only small currents from the -3.0 volt supply, such that charge pump techniques using +5.0 volts can be used. Figure 24 shows a supply circuit that will generate the required -3.0 volts for V_{BB}.

When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit spikes or "glitches" on their outputs when the ac power is switched on and off. For example, the bench power supply programmed to deliver +12 volts may have large transients below ground when the ac power is switched on and off. If this possibility exists, it is suggested that the user switch the dc side of the power supply or protect the device power pins (+12, +5.0 and -3.0 volt) against reverse biasing with clamp diodes. A hot carrier diode such as the MBD501 is suggested for this purpose.

3

FIGURE 19 – SELECTRIC LINE CODE TO BAIL CODE CONVERSION

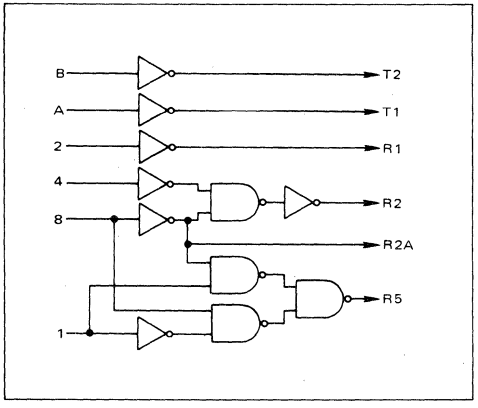


FIGURE 20 – BAIL CODE TO SELECTRIC LINE CODE CONVERSION

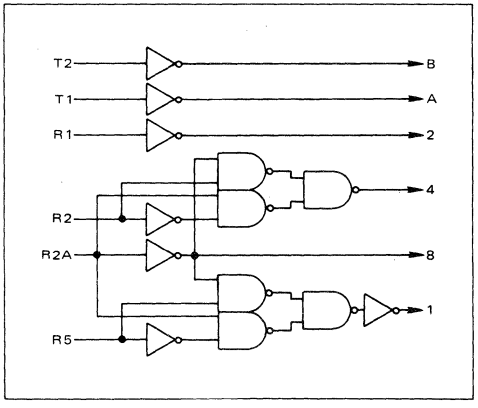


FIGURE 21 – EBCDIC TO ASCII CODE CONVERSION

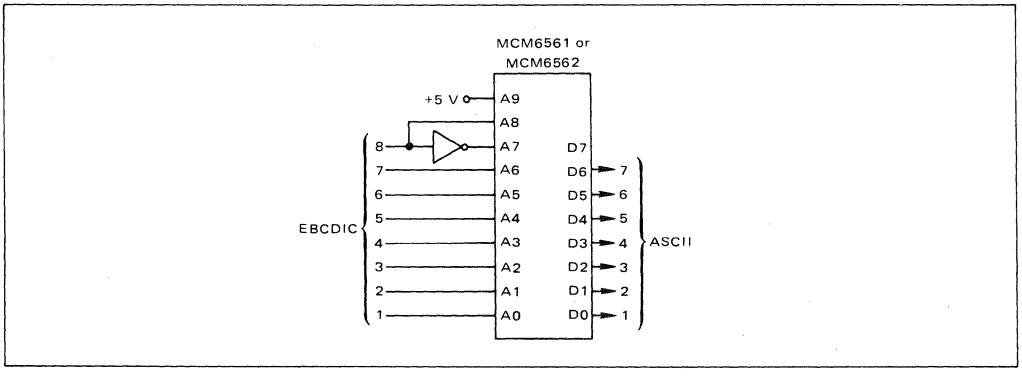


FIGURE 22 – HOLLERITH TO ASCII CODE CONVERSION

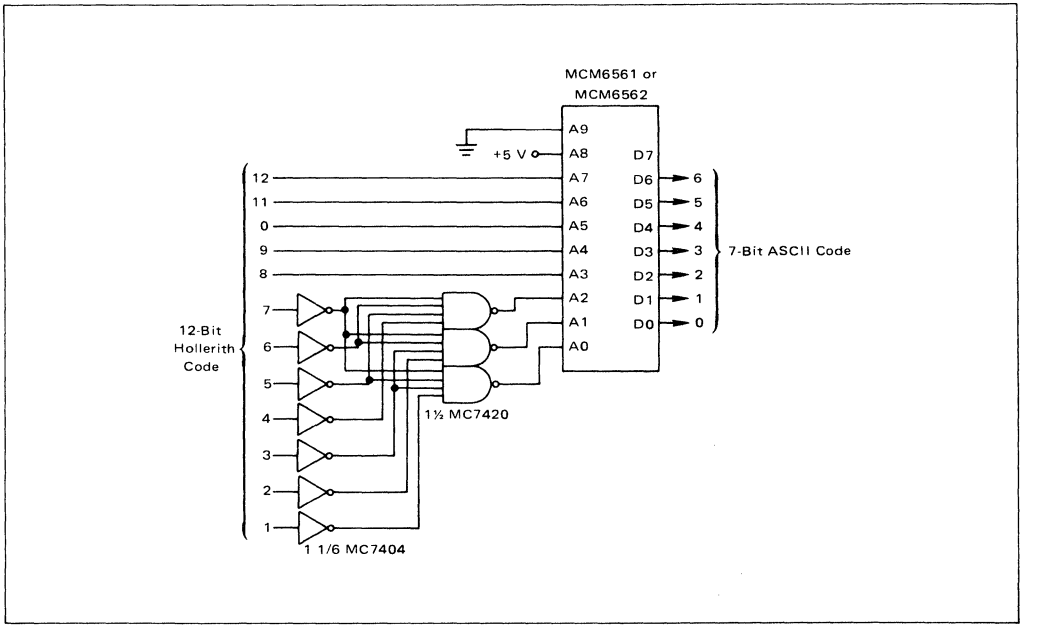


FIGURE 23 – ASCII TO HOLLERITH CODE CONVERSION

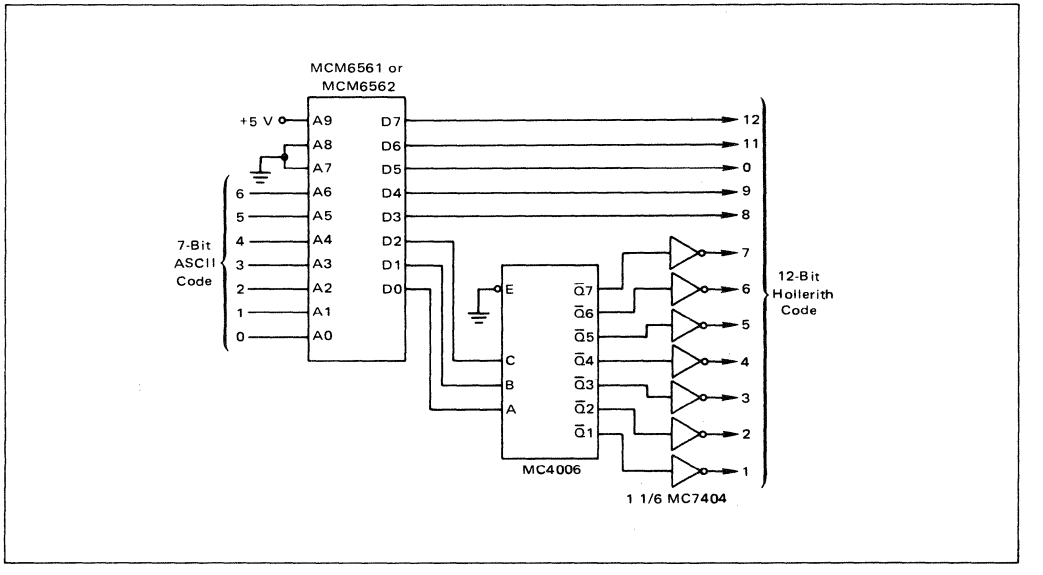
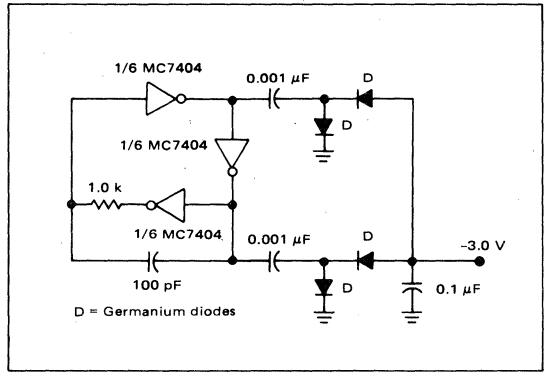


FIGURE 24 – SUBSTRATE BIAS CHARGE PUMP SUPPLY



MCM6570
MCM6571
MCM6571A
MCM6572
thru
MCM6579

8192-BIT READ ONLY MEMORIES
ROW SELECT CHARACTER GENERATORS

The MCM6570 is a mask-programmable 8192-bit horizontal-scan (row select) character generator. It contains 128 characters in a 7 x 9 matrix, and has the capability of shifting certain characters that normally extend below the baseline, such as j, y, g, p, and q. Circuitry is supplied internally to effectively lower the whole matrix for this type of character -- a feature previously requiring external circuitry.

A seven-bit address code is used to select one of the 128 available characters. Each character is defined as a specific combination of logic "1"s and "0"s stored in a 7 x 9 matrix. When a specific four-bit binary row select code is applied, a word of seven parallel bits appears at the output. The rows can be sequentially selected, providing a nine-word sequence of seven parallel bits per word for each character selected by the address inputs. As the row select inputs are sequentially addressed, the devices will automatically place the 7 x 9 character in one of two pre-programmed positions on the 16-row matrix, with the positions defined by the four row select inputs. Rows that are not part of the character are automatically blanked.

The MCM6571, MCM6571A, and MCM6572 thru MCM6579 are pre-programmed versions of the MCM6570. They contain various sets of characters to meet the requirements of diverse applications. The complete patterns of these devices are contained in this data sheet.

- Static Operation
- TTL Compatibility
- CMOS Compatibility (5 V)
- Shifted Character Capability (Except MCM6572, MCM6573)
- Maximum Access Time = 500 ns

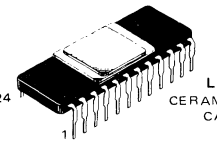
MOS

(N-CHANNEL, LOW THRESHOLD)

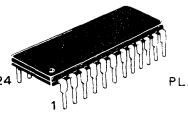
8 K
READ ONLY MEMORIES

HORIZONTAL-SCAN
CHARACTER GENERATORS
WITH SHIFTED CHARACTERS

3



L SUFFIX
CERAMIC PACKAGE
CASE 684



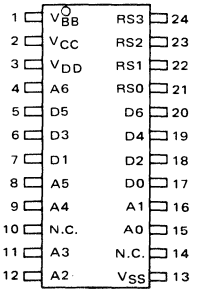
P SUFFIX
PLASTIC PACKAGE
CASE 709

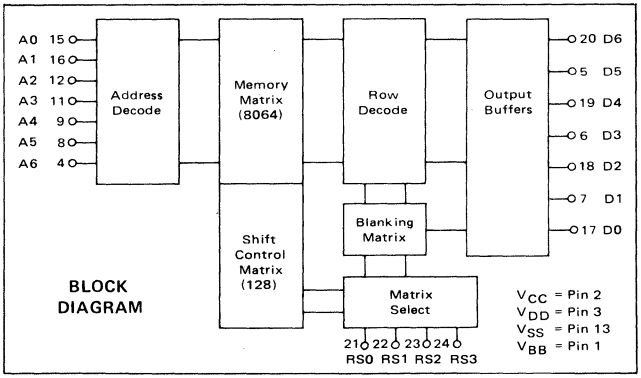
ABSOLUTE MAXIMUM RATINGS (See Note 1, Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
Supply Voltages	V_{CC} V_{DD} V_{BB}	-0.3 to +6.0 -0.3 to +15 -10 to +0.3	Vdc
Data Input Voltage	V_{in}	-0.3 to +15	Vdc
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-55 to +125	°C

NOTE 1: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

PIN ASSIGNMENT





BLOCK DIAGRAM

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted.)

RECOMMENDED DC OPERATING CONDITIONS (Referenced to V_{SS})

Parameter	Symbol	Min	Nom	Max	Unit
Supply Voltage	V_{DD}	10.8	12	13.2	Vdc
	V_{CC}	4.75	5.0	5.25	Vdc
	V_{SS}	0	0	0	Vdc
	V_{BB}	-3.3	-3.0	-2.7	Vdc
Input Logic "1" Voltage (Driven by TTL)	V_{IH}*	3.0	–	V_{CC}	Vdc
(Driven by Other Than TTL)		4.0	–	V_{CC}	Vdc
Input Logic "0" Voltage	V_{IL}	0	–	0.8	Vdc

*A 4.0 V V_{IH} is required at the chip regardless of the type of driver used. However, internal MOS pullup devices on the chip can pull one TTL driver from 3.0 V to 4.0 V, without affecting access time. These pullup devices may not pull non-TTL drivers above 3.0 V.

3

DC CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit
Input Forward Current (V_{IL} = 0.4 Vdc)	I_{IL}	--	–	-1.6	mAdc
Input Leakage Current (V_{IH} = 5.25 Vdc, V_{CC} = 4.75 Vdc)	I_{IH}	–	–	100	μAdc
Output Low Voltage (Blank) (I_{OL} = 1.6 mAdc)	V_{OL}	0	–	0.4	Vdc
Output High Voltage (Dot) (I_{OH} = -40 μAdc)	V_{OH}	3.0	–	–	Vdc
Power Supply Current	I_{DD}	–	–	10	mAdc
	I_{CC}	–	–	125	mAdc
	I_{BB}	–	–	100	μAdc
Power Dissipation	P_D	–	600	800	mW

CAPACITANCE (Periodically sampled rather than 100% tested)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Capacitance (f = 1.0 MHz)	C_{in}	–	4.0	7.0	pF
Output Capacitance (f = 1.0 MHz)	C_{out}	–	4.0	7.0	pF

AC CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted.)

[All timing with t_r,t_f = 20 ns; Load = 1 TTL Gate (MC7400 Series), C_L = 30 pF]

TIMING (Typical values measured at 25°C and nominal supplies)

Characteristic	Symbol	Min	Typ	Max	Unit
Address Access Time (See Figure 1A)	$t_{acc(A)}$	–	350	500	ns
Row Select Access Time (See Figure 1B)	$t_{acc(RS)}$	–	300	500	ns

FIGURE 1 – TIMING DIAGRAMS

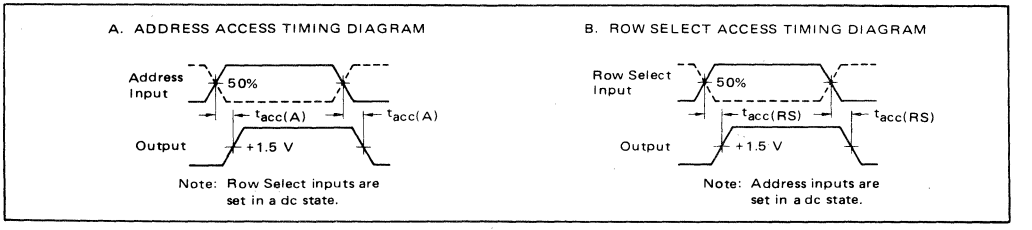


FIGURE 2 – V_{CC} SUPPLY CURRENT versus TEMPERATURE

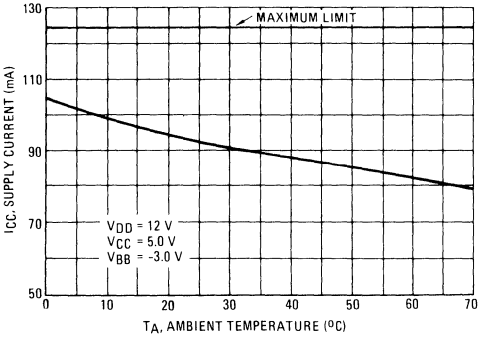


FIGURE 3 – V_{DD} SUPPLY CURRENT versus TEMPERATURE

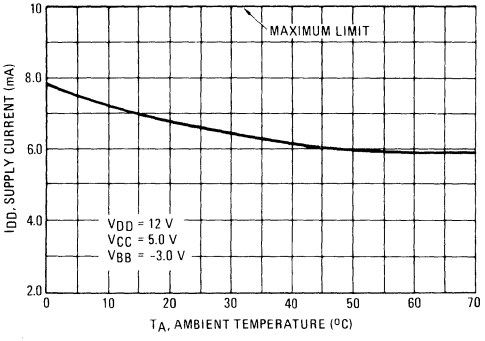


FIGURE 4 – OUTPUT SINK CURRENT versus OUTPUT VOLTAGE

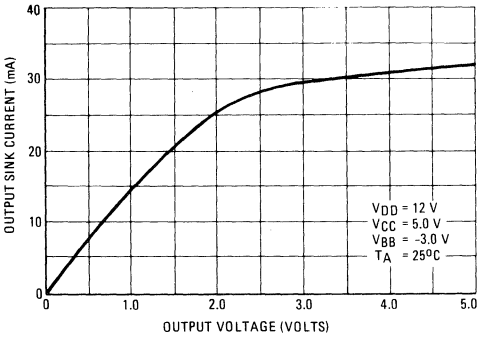


FIGURE 5 – POWER DISSIPATION versus V_{DD} SUPPLY VOLTAGE

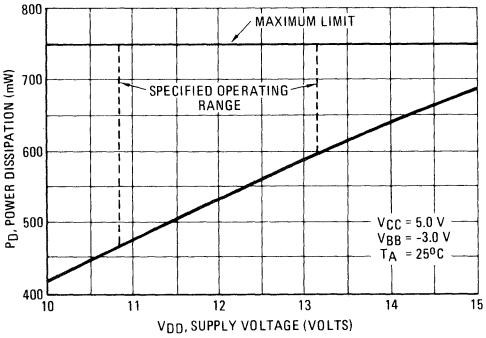


FIGURE 6 – ACCESS TIME versus V_{DD} SUPPLY VOLTAGE

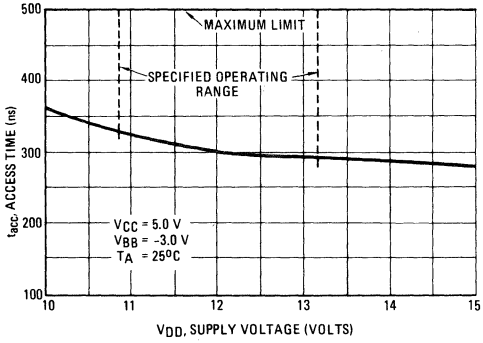
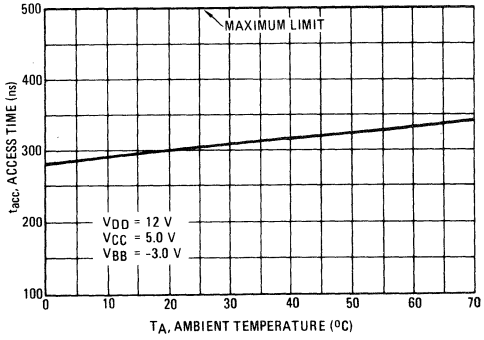


FIGURE 7 – ACCESS TIME versus TEMPERATURE



MEMORY OPERATION (Using Positive Logic)

Most positive level = 1, most negative level = 0

Address

To select one of the 128 characters, apply the appropriate binary code to the Address inputs (A0 thru A6).

Row Select

To select one of the rows of the addressed character to appear at the seven output lines, apply the appropriate binary code to the Row Select inputs (RS1 thru RS4).

Shifted Characters

These devices have the capability of displaying characters that descend below the bottom line (such as lower case letters j, y, g, p, and q). Internal circuitry effectively drops the whole matrix for this type of character. Any character can be programmed to occupy either of the two positions in a 7 x 16 matrix. (Shifted characters are not available on MCM6572 or MCM6573.)

Output

For these devices, an output dot is defined as a logic "1" level, and an output blank is defined as a logic "0" level.

3

DISPLAY FORMAT

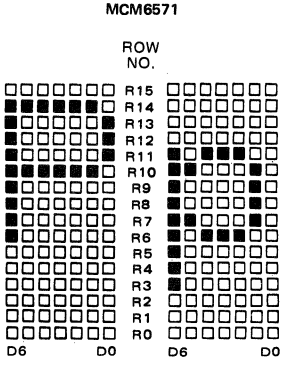
Figure 8 shows the relationship between the logic levels at the row select inputs and the character row at the outputs. The MCM6570 allows the user to locate the basic 7 x 9 font anywhere in the 7 x 16 array. In addition, a shifted font can be placed anywhere in the same 7 x 16 array. For example, the basic MCM6571 font is established in rows R14 thru R6. All other rows are automatically blanked. The shifted font is established in rows R11 thru R3, with all other rows blanked. Thus, while any one character is contained in a 7 x 9 array, the MCM6571 requires a 7 x 12 array on the CRT screen to contain both normal and descending characters. Other uses of the shift option may require as much as the full 7 x 16 array, or as little as the basic 7 x 9 array (when no shifting occurs, as in the MCM6572).

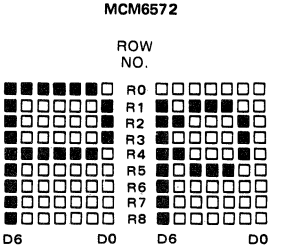
The MCM6570 can be programmed to be scanned either from bottom to top or from top to bottom. This is achieved through the option of assigning row numbers in ascending or descending count, as long as both the basic font and the shifted font are the same. For example, an up counter will scan the MCM6571 from bottom to top, whereas an up counter will scan the MCM6571A from top to bottom (see Figures 14 and 15 for row designation).

FIGURE 8 – ROW SELECT INPUT CODE AND SAMPLE CHARACTERS FOR MCM6571 AND MCM6572

ROW SELECT TRUTH TABLE

RS3	RS2	RS1	RS0	OUTPUT
0	0	0	0	R0
0	0	0	1	R1
0	0	1	0	R2
0	0	1	1	R3
0	1	0	0	R4
0	1	0	1	R5
0	1	1	0	R6
0	1	1	1	R7
1	0	0	0	R8
1	0	0	1	R9
1	0	1	0	R10
1	0	1	1	R11
1	1	0	0	R12
1	1	0	1	R13
1	1	1	0	R14
1	1	1	1	R15





CUSTOM PROGRAMMING FOR MCM6570

By the programming of a single photomask, the customer may specify the content of the MCM6570. Encoding of the photomask is done with the aid of a computer to provide quick, efficient implementation of the custom bit pattern while reducing the cost of implementation.

Information for the custom memory content may be sent to Motorola in the following forms, in order of preference:*

1. Hexadecimal coding using IBM Punch Cards (Figures 10 and 11).
2. Hexadecimal coding using ASCII Paper Tape Punch (Figure 12).

Programming of the MCM6570 can be achieved by using the following sequence:

1. Create the 128 characters in a 7 x 9 font using the format shown in Figure 9. Note that information at output D6 appears in column one, D5 in column two, thru D0 information in column seven. The dots filled in and programmed as a logic "1" will appear at the outputs as V_{OH}; the dots left blank will be at V_{OL}. (Blank formats appear at the end of this data sheet for your convenience; they are not to be submitted to Motorola, however.)

2. Indicate which characters are shifted by filling in the extra square (dot) in the top row, at the left (column S).

3. Convert the characters to hexadecimal coding treating dots as ones and blanks as zeros, and enter this information in the blocks to the right of the character font format. High order bits are at the left, in columns S and D3. For the bottom eight rows, the bit in column S must be zero, so these locations have been omitted. For the top row, the bit in column S will be zero for an unshifted character, and one for a shifted character.

4. Transfer the hexadecimal figures either to punched cards (Figure 10) or to paper tape (Figure 12).

5. Assign row numbers to the unshifted font. These must be nine sequential numbers (values 0 thru 15) assigned consecutively to the rows. The shifted font is similarly placed in any position in the 16 rows.

6. Provide, in writing, the information indicated in Figure 13 (a copy of Figure 13 may be used for this purpose). Submit this information to Motorola together with the punched cards or paper tape.

FIGURE 9 – CHARACTER FORMAT

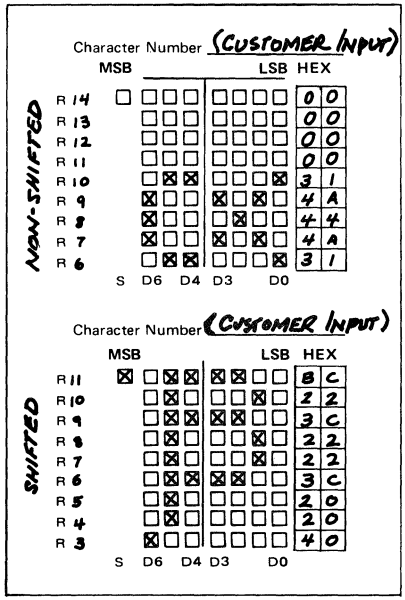


FIGURE 10 – CARD PUNCH FORMAT

Columns	
1 - 10	Blank
11	Asterisk (*)
12 - 29	Hex coding for first character
30	Slash (/)
31 - 48	Hex coding for second character
49	Slash (/)
50 - 67	Hex coding for third character
68	Slash (/)
69 - 76	Blank
77 - 78	Card number (starting 01; thru 43)
79 - 80	Blank

Column 12 on the first card contains the hexadecimal equivalent of column S and D6 thru D4 for the top row of the first character. Column 13 contains D3 thru D0. Columns 14 and 15 contain the information for the next row. The entire first character is coded in columns 12 thru 29. Each card contains the coding for three characters. 43 cards are required to program the entire 128 characters, the last card containing only two characters. The characters must be programmed in sequence from the first character to the last in order to establish proper addressing for the part. As an example, the first nine characters of the MCM6571 are correctly coded and punched in Figure 11.

*Note: Motorola can accept magnetic tape and truth table formats. For further information contact your local Motorola sales representative.

FIGURE 11 – EXAMPLE OF CARD PUNCH FORMAT
(First 9 Characters of MCM6571)

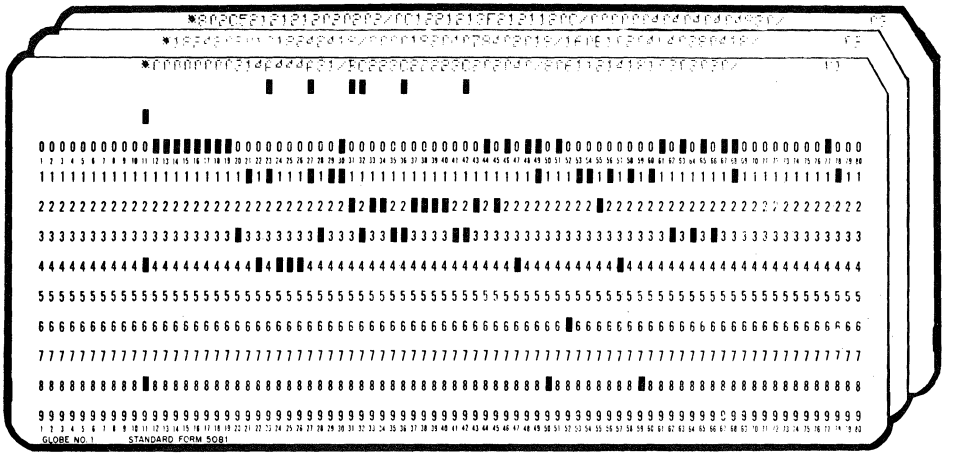


FIGURE 12 – PAPER TAPE FORMAT

Frames	
Leader	Blank Tape
1 to M	Allowed for customer use (M ⩽ 64)
M + 1, M + 2	CR; LF (Carriage Return; Line Feed)
M + 3 to M + 66	First line of pattern information (64 hex figures per line)
M + 67, M + 68	CR; LF
M + 69 to M + 2378	Remaining 35 lines of hex figures, each line followed by a Carriage Return and Line Feed

Blank Tape

Frames 1 to M are left to the customer for internal identification, where M ⩽ 64. Any combination of alpha-numerics may be used. This information is terminated with a Carriage Return and Line Feed, delineating the start of data entry. (Note that the tape cannot begin with a CR and/or LF, or the customer identification will be assumed to be programming data.)

Frame M + 3 contains the hexadecimal equivalent of column S and D6 thru D4 for the top row of the first character. Frame M + 4 contains D3 thru D0. Frames M + 5 and M + 6 program the second row of the first character. Frames M + 3 to M + 66 comprise the first line of the printout. The line is terminated with a CR and LF.

The remaining 35 lines of data are punched in sequence using the same format, each line terminated with a CR and LF. The total 36 lines of data contain 36 x 64 or 2304 hex figures. Since 18 hex figures are required to program each 7 x 9 character, the full 128 (2304 ÷ 18) characters are programmed.

FIGURE 13 – FORMAT FOR ORGANIZATIONAL DATA

ORGANIZATIONAL DATA
MCM6570 MOS READ ONLY MEMORY

Customer _____

Customer Part No. _____ Rev. _____

Row Number for top row of non-shifted font _____

Row Number for bottom row of non-shifted font _____

Row Number for top row of shifted font _____

FIGURE 14 – MCM6571 PATTERN

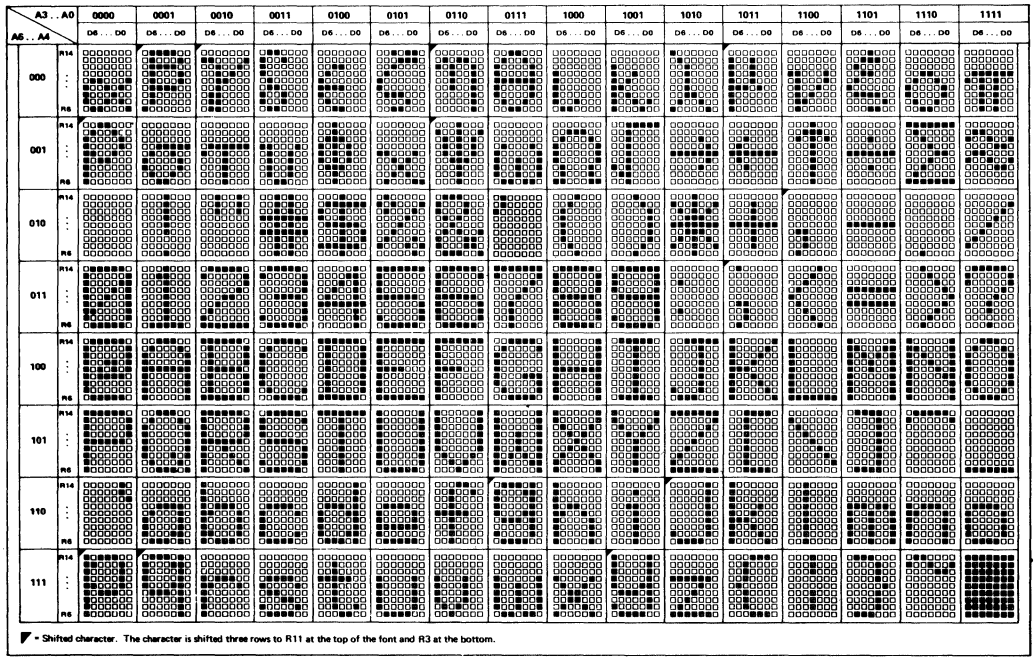


FIGURE 15 – MCM6571A PATTERN

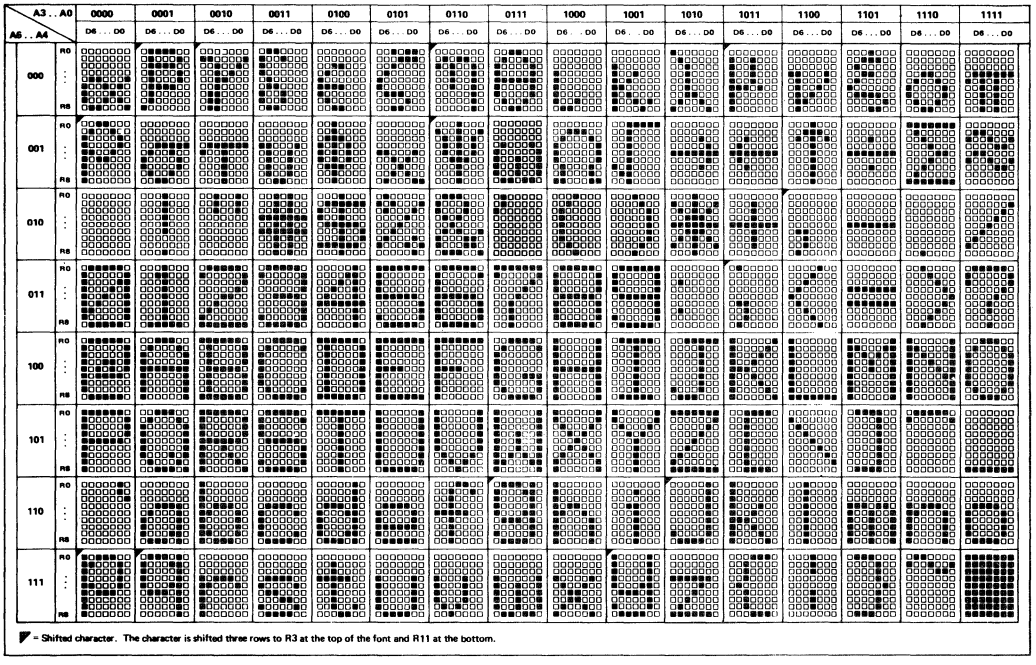
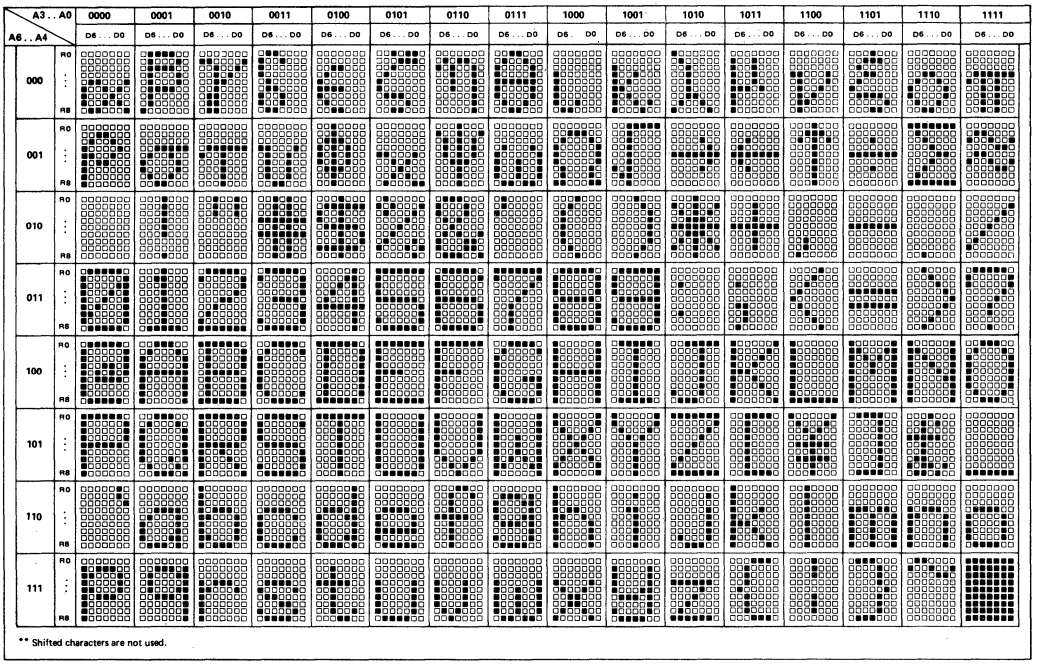
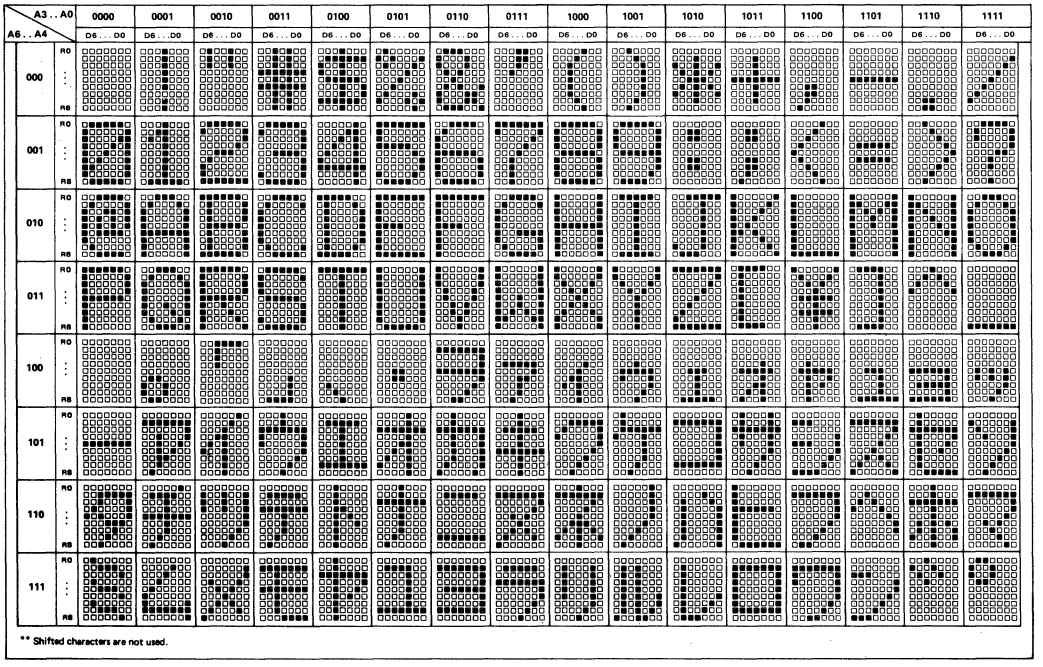


FIGURE 16 – MCM6572 PATTERN**



** Shifted characters are not used.

FIGURE 17 – MCM6573 PATTERN**



** Shifted characters are not used.

FIGURE 18 – MCM6574 PATTERN

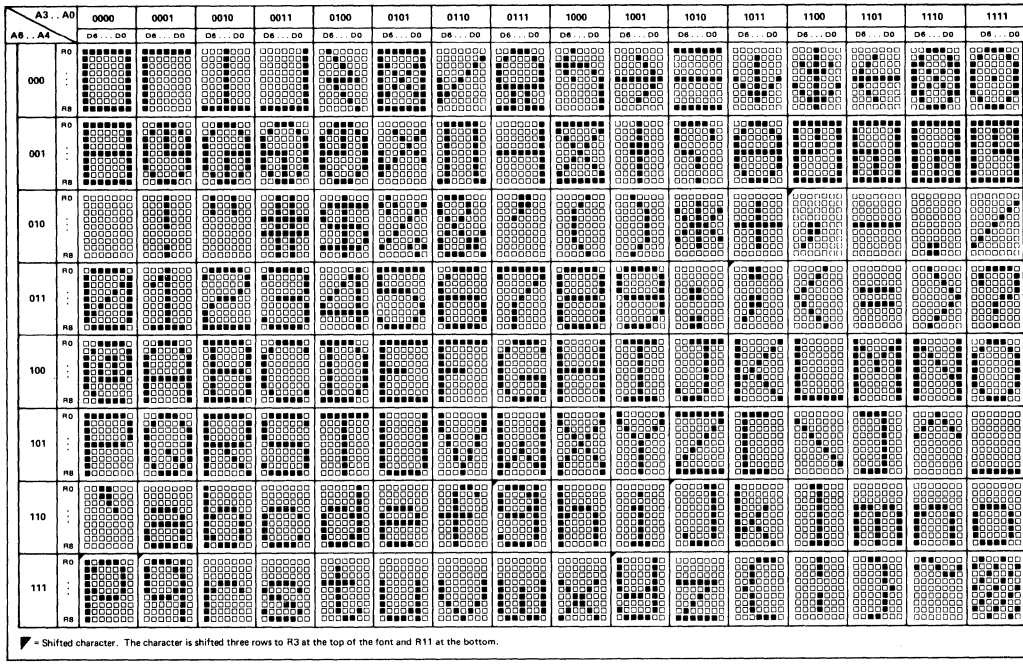


FIGURE 19 – MCM6575 PATTERN

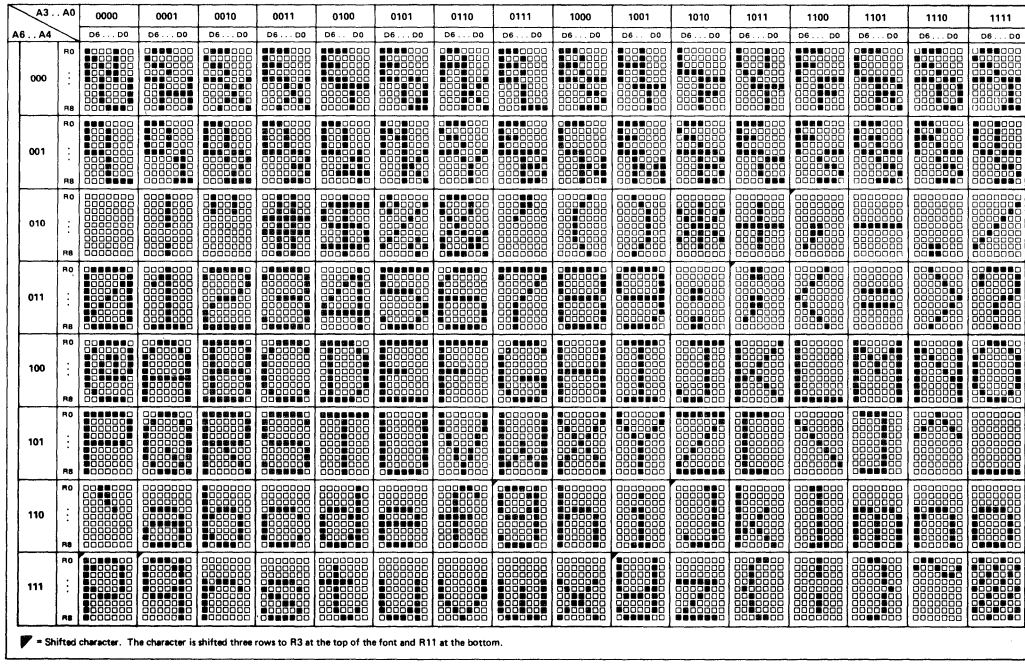


FIGURE 20 – MCM6576 PATTERN

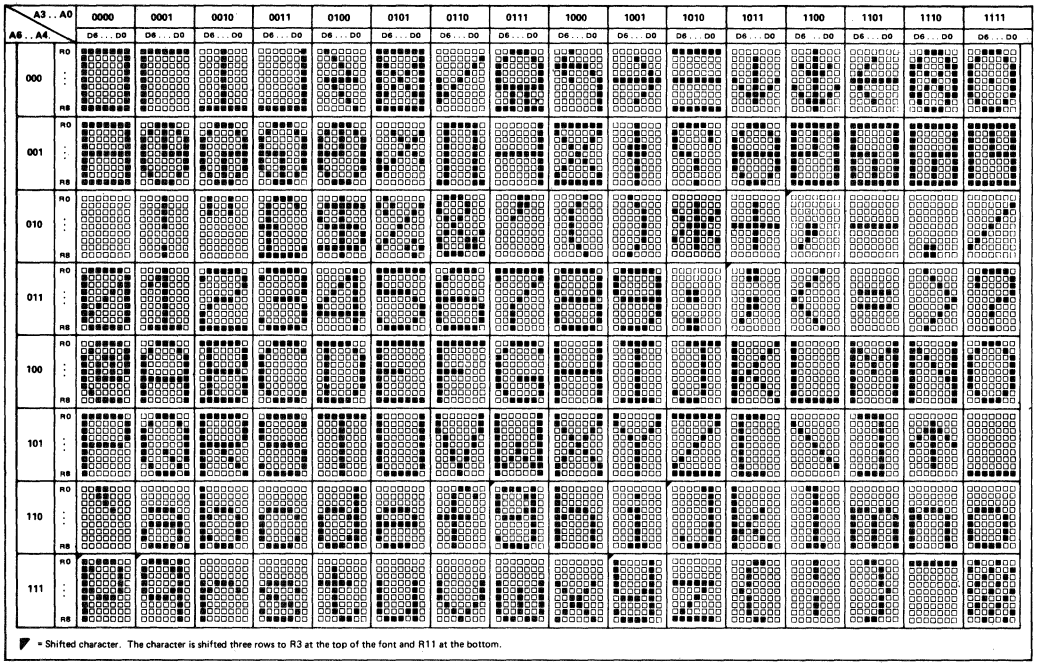


FIGURE 21 – MCM6577 PATTERN

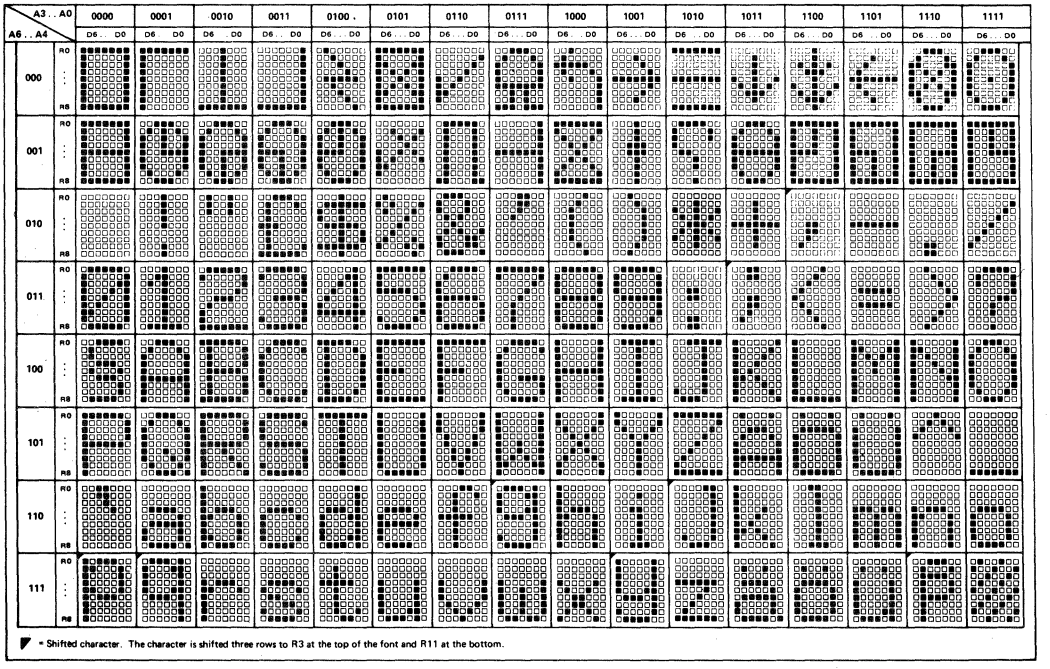
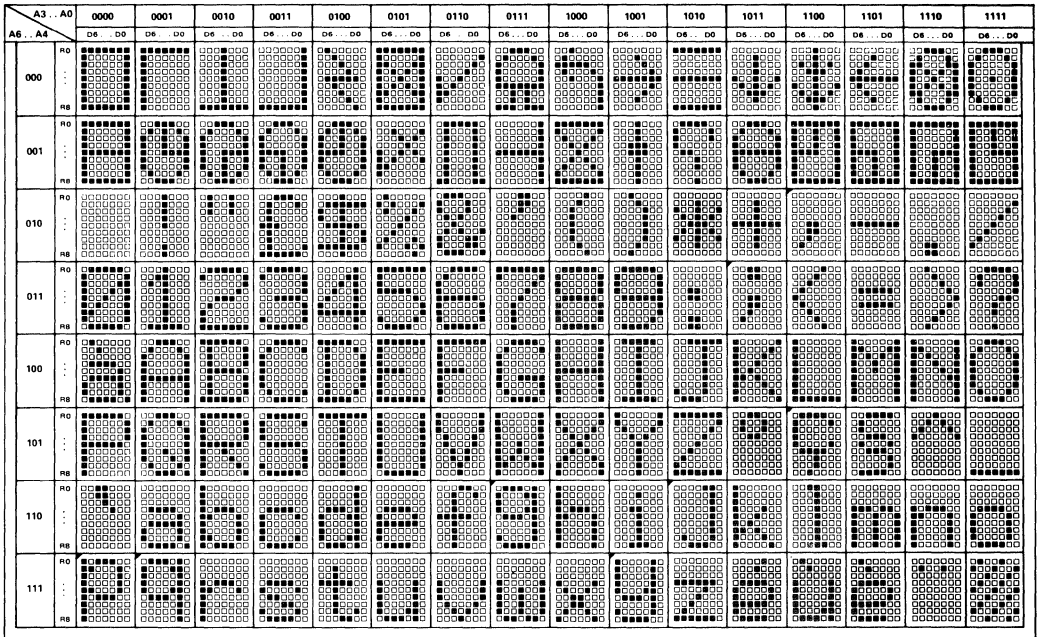
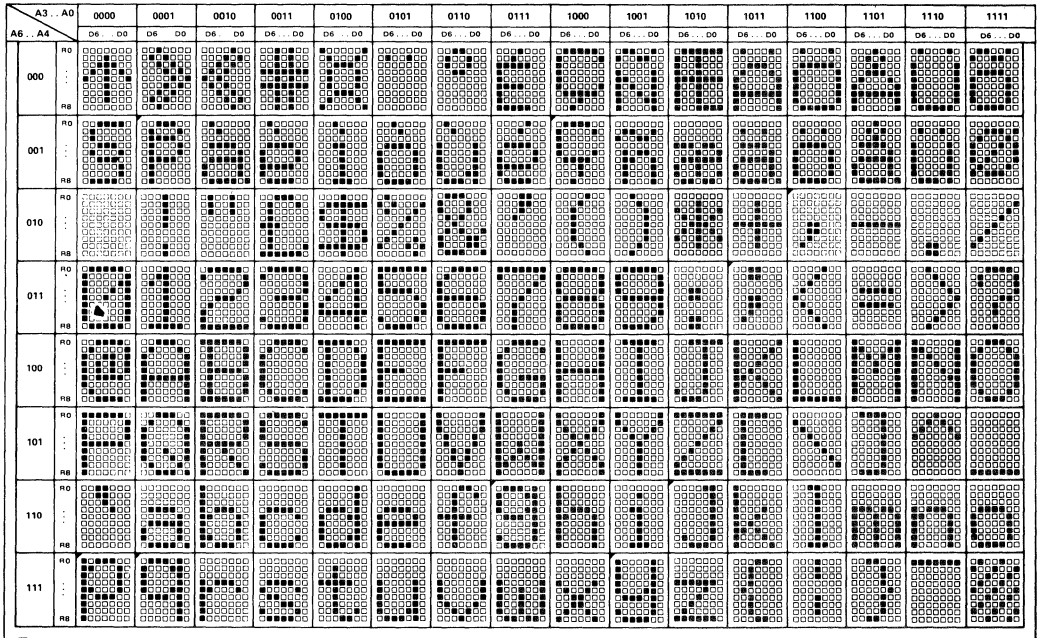


FIGURE 22 – MCM6578 PATTERN



◤ = Shifted character. The character is shifted three rows to R3 at the top of the font and R11 at the bottom.

FIGURE 23 – MCM6579 PATTERN



◤ = Shifted character. The character is shifted three rows to R3 at the top of the font and R11 at the bottom.

APPLICATIONS INFORMATION

One important application for the MCM6570-79 is in CRT display systems (Figure 24). A set of buffer shift registers or random access memories applies a 7-bit character code to the input of the character generator, which then supplies one row of the character according to the count at the four row select inputs. As each row is available, it is put into the TTL MC7495 shift registers. The parallel information in these shift registers is clocked serially out to the Z-axis where it modulates the raster to form the character.

The MCM6570-79 require three power supplies: -3.0 volts, +5.0 volts, and +12 volts. The character generator requires only small currents from the -3.0 volt and +12 volt supplies, such that charge pump techniques using +5.0 volts can be used.

Figure 25 shows a supply circuit that will generate the required -3.0 volts for V_{BB}. The +12-volt supply of Figure 26 will supply the 6.0 mA that is typically required. Increased current capability is possible by modifying the circuits. Use of these small, low-cost supplies makes a single +5.0-volt system possible.

When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit spikes or "glitches" on their outputs when the ac power is switched on and off. For example, the bench power supply programmed to deliver +12 volts may have large transients below ground when the ac power is switched on and off. If this possibility exists, it is suggested that the user switch the dc side of the power supply or protect the device power pins (+12, +5.0, and -3.0 volt) against reverse biasing with clamp diodes. A hot carrier diode such as the MBD501 is suggested for this purpose.

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FIGURE 24 – CRT DISPLAY APPLICATION USING MCM6571

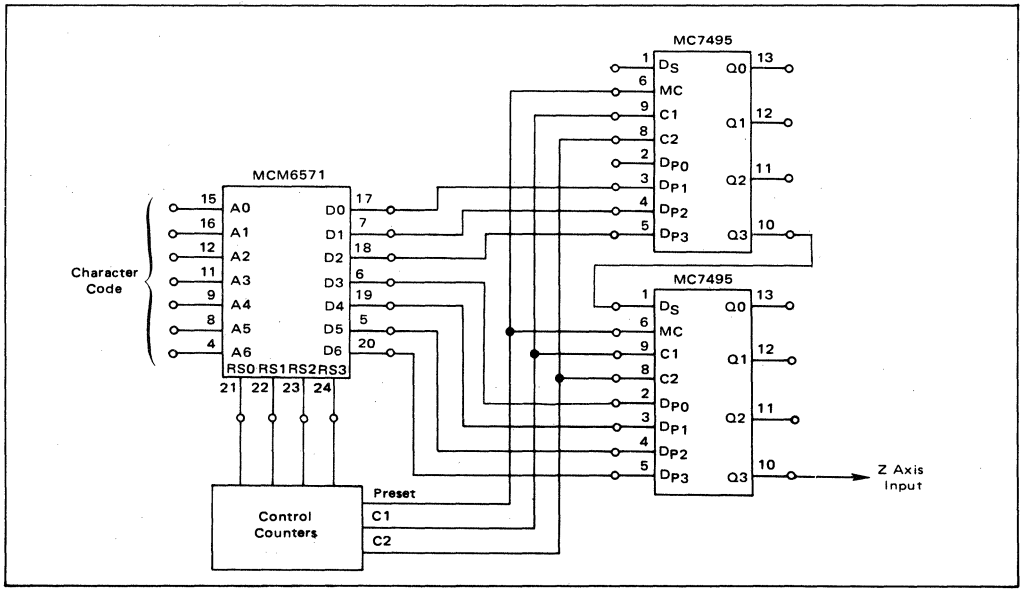


FIGURE 25 – SUBSTRATE BIAS CHARGE PUMP SUPPLY

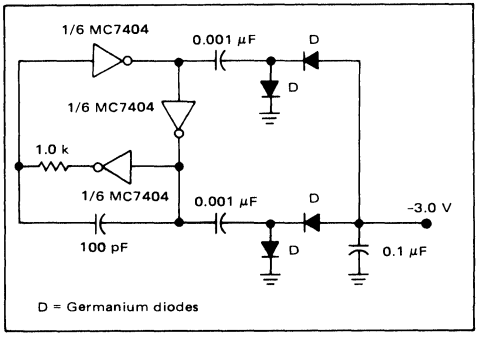
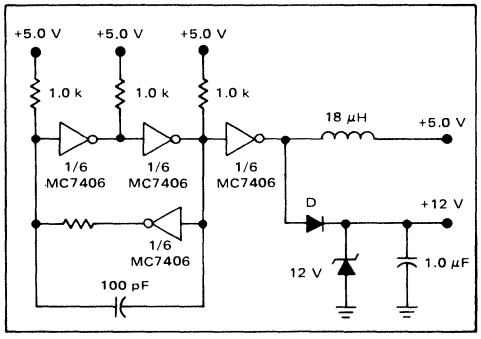


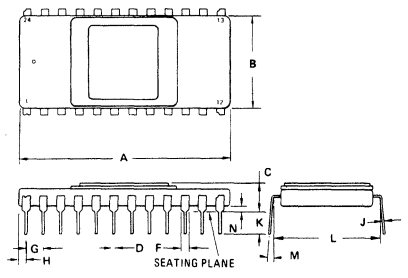
FIGURE 26 – GATE VOLTAGE CHARGE PUMP SUPPLY



3

PACKAGE DIMENSIONS

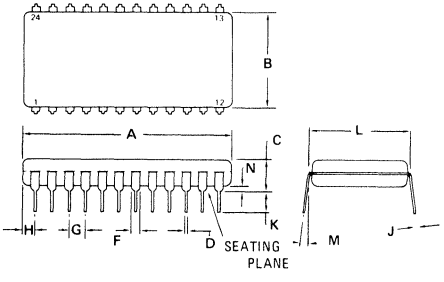
CASE 684-04



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	29.34	30.86	1.155	1.215
B	12.70	14.22	0.500	0.560
C	3.05	3.94	0.120	0.155
D	0.38	0.51	0.015	0.020
F	0.89	1.40	0.035	0.055
G	2.54 BSC		0.100 BSC	
H	0.89	1.40	0.035	0.055
J	0.20	0.30	0.008	0.012
K	2.92	3.68	0.115	0.145
L	14.86	15.87	0.585	0.625
M	–	15^0	–	15^0
N	0.51	1.14	0.020	0.045

NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE WITH MAXIMUM MATERIAL CONDITION.
2. LEAD NO. 1 CUT FOR IDENTIFICATION, OR BUMP ON TOP.
3. DIM "L" TO INSIDE OF LEADS. (MEASURED 0.51 mm (0.020) BELOW PKG BASE)

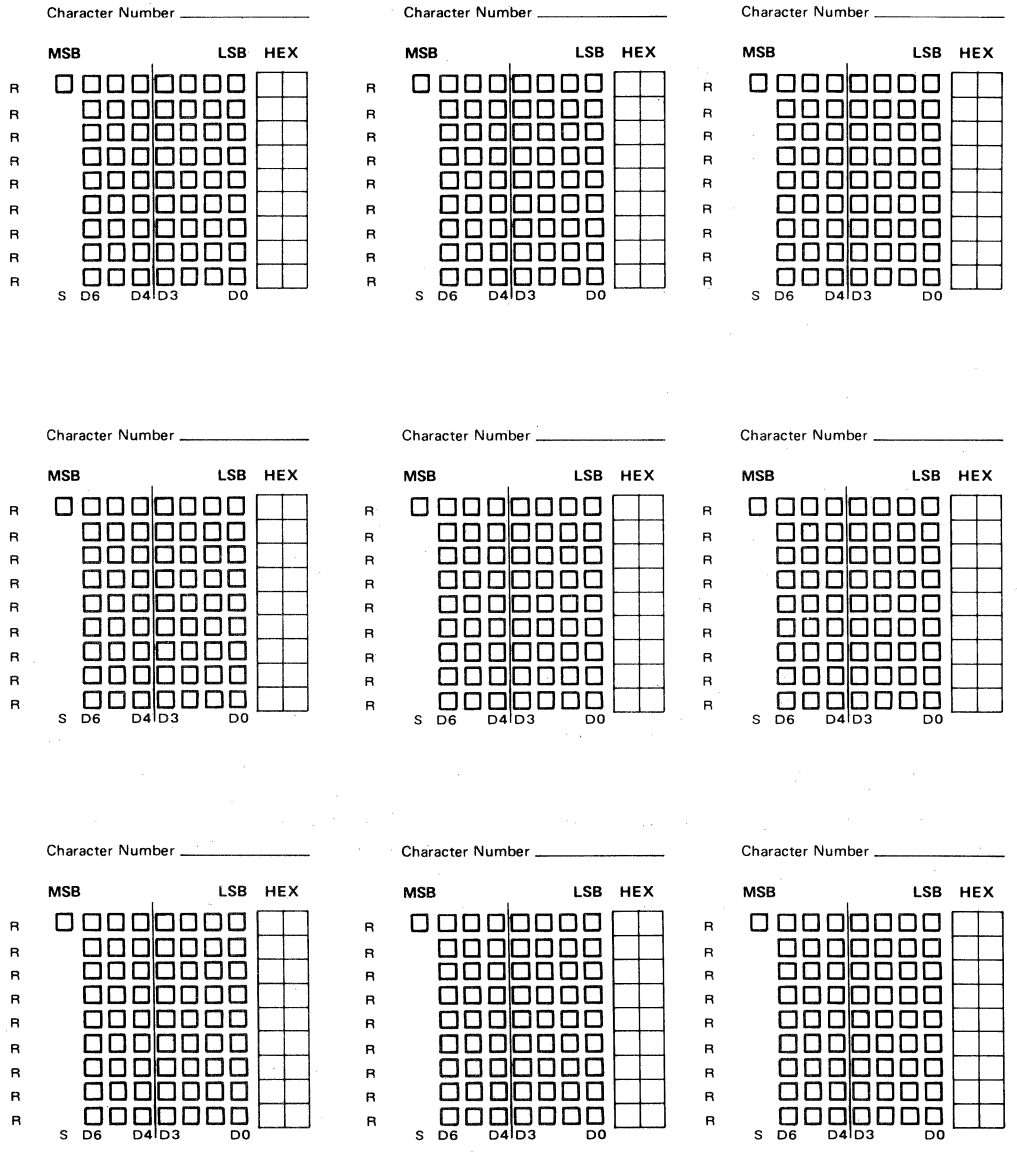
CASE 709-01



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	31.37	32.13	1.235	1.265
B	13.72	14.22	0.540	0.560
C	4.57	5.08	0.180	0.200
D	0.36	0.51	0.014	0.020
F	1.02	1.52	0.040	0.060
G	2.41	2.67	0.095	0.105
H	1.78	2.03	0.070	0.080
J	0.20	0.30	0.008	0.012
K	3.05	3.56	0.120	0.140
L	14.73	15.24	0.580	0.600
M	0^0	10^0	0^0	10^0
N	0.51	1.02	0.020	0.040

NOTES:
1. LEADS, TRUE POSITIONED WITHIN 0.25 mm (0.010) DIA AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION. (DIM. "D")
2. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.

The formats below are given for your convenience in preparing character information for MCM6570 programming. THESE FORMATS ARE NOT TO BE USED TO TRANSMIT THE INFORMATION TO MOTOROLA. Refer to the Custom Programming instructions for detailed procedures.



MCM6580
MCM6581
MCM6583

8192-BIT READ ONLY MEMORIES
COLUMN SELECT CHARACTER GENERATORS

The MCM6580 is a mask-programmable 8192-bit vertical scan (column select) character generator. It contains 128 characters in a 7 x 9 matrix. A Shift Control Command (SCC) bit can be programmed so that a high logic level will appear at the SCC output, in addition to the coding at D0-D8, to indicate to external circuitry that the character is to be shifted.

A seven-bit address code is used to select one of the 128 available characters programmed in the memory. Each character is defined as a specific combination of logic "1"s and "0"s stored in a 7 x 9 matrix. When a specific three-bit binary column select code is applied, a word of nine parallel bits appears at the output. The columns can be sequentially selected, providing a seven-word sequence of nine parallel bits per word for each character selected by the address inputs.

The MCM6581 is a pre-programmed version of the MCM6580, with a modified USASCII code. It contains the upper and lower case English alphabet, lower case Greek alphabet, and various mathematical symbols and punctuation marks. The MCM6583 is also a pre-programmed MCM6580 and contains the upper case English alphabet, Japanese characters, and various mathematical symbols and punctuation marks. The MCM6581 uses the SCC bit for appropriate characters; the MCM6583 holds SCC = "0" for all characters.

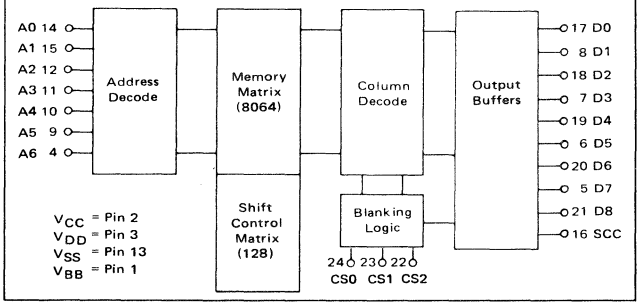
- Static Operation
- TTL Compatibility
- CMOS Compatibility (5 V)
- 128 Characters of 64 Bits (7 x 9) and Shift Control
- Maximum Access Time = 400 ns

ABSOLUTE MAXIMUM RATINGS (See Note 1, Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
Supply Voltages	V_{CC} V_{DD} V_{BB}	-0.3 to +6.0 -0.3 to +15 -10 to +0.3	Vdc
Address/Control Input Voltage	V_{in}	-0.3 to +15	Vdc
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-55 to +125	°C

NOTE 1: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

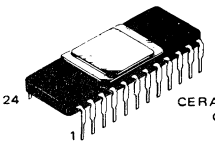
BLOCK DIAGRAM



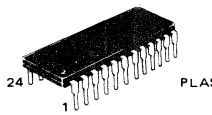
MOS
(N-CHANNEL, LOW THRESHOLD)

8K
READ ONLY MEMORIES

VERTICAL-SCAN CHARACTER GENERATORS

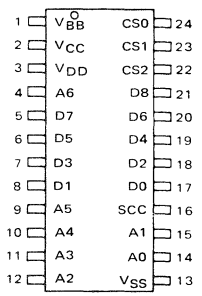


L SUFFIX
CERAMIC PACKAGE
CASE 684



P SUFFIX
PLASTIC PACKAGE
CASE 709

PIN ASSIGNMENT



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted.)

RECOMMENDED DC OPERATING CONDITIONS (Referenced to V_{SS}).

Parameter	Symbol	Min	Nom	Max	Unit
Supply Voltage	V_{DD}	10.8	12	13.2	Vdc
	V_{CC}	4.75	5.0	5.25	Vdc
	V_{SS}	0	0	0	Vdc
	V_{BB}	-3.3	-3.0	-2.7	Vdc
Input Logic "1" Voltage (Driven by TTL)	V_{IH}*	3.0	–	V_{CC}	Vdc
(Driven by Other Than TTL)		4.0	–	V_{CC}	Vdc
Input Logic "0" Voltage	V_{IL}	0	–	0.8	Vdc

*A 4.0 V V_{IH} is required at the chip regardless of the type of driver used. However, internal MOS pullup devices on the chip can pull one TTL driver from 3.0 V to 4.0 V, without affecting access time. These pullup devices may not pull non-TTL drivers above 3.0 V.

DC CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit
Input Forward Current (V_{IL} = 0.4 Vdc)	I_{IL}	–	–	-1.6	mAdc
Input Leakage Current (V_{IH} = 5.25 Vdc, V_{CC} = 4.75 Vdc)	I_{IH}	–	–	100	μAdc
Output Low Voltage (Blank) (I_{OL} = 1.6 mAdc)	V_{OL}	0	–	0.4	Vdc
Output High Voltage (Dot) (I_{OH} = -40 μAdc)	V_{OH}	3.0	–	V_{CC}	Vdc
Power Supply Current	I_{DD}	–	–	30	mAdc
	I_{CC}	–	–	140	mAdc
	I_{BB}	–	–	100	μAdc
Power Dissipation	P_D	–	700	800	mW

CAPACITANCE (Periodically sampled rather than 100% tested)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Capacitance (f = 1.0 MHz)	C_{in}	–	4.0	7.0	pF
Output Capacitance (f = 1.0 MHz)	C_{out}	–	4.0	7.0	pF

AC CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted.)

[All timing with t_r,t_f = 20 ns; Load = 1 TTL Gate (MC7400 Series), C_L = 30 pF]

TIMING (Typical values measured at 25°C and nominal supplies)

Characteristic	Symbol	Min	Typ	Max	Unit
Address Access Time (See Figure 1A)	$t_{acc(A)}$	–	225	400	ns
Column Select Access Time (See Figure 1B)	t_{acc} (CS)	–	225	400	ns

FIGURE 1 – TIMING DIAGRAMS

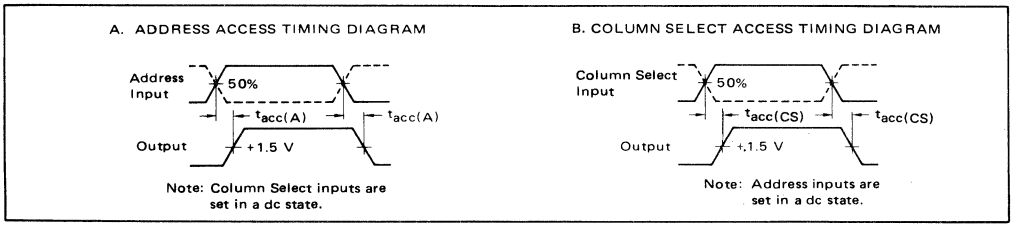


FIGURE 2 – V_{CC} SUPPLY CURRENT versus TEMPERATURE

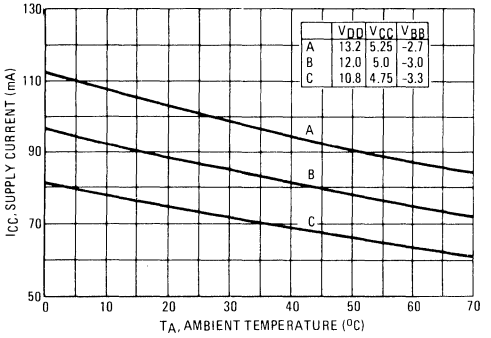


FIGURE 3 – V_{DD} SUPPLY CURRENT versus TEMPERATURE

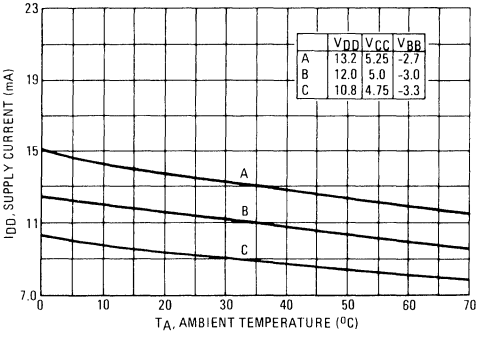


FIGURE 4 – OUTPUT SINK CURRENT versus OUTPUT VOLTAGE

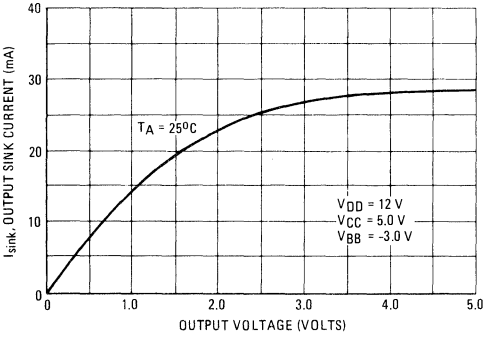


FIGURE 5 – OUTPUT SOURCE CURRENT versus OUTPUT VOLTAGE

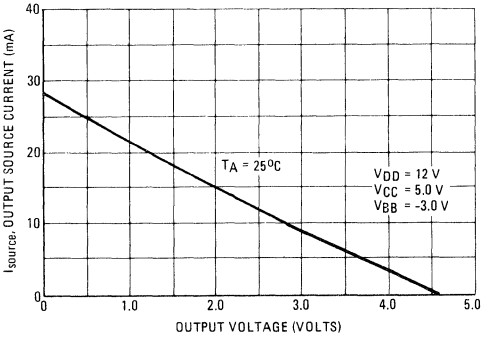


FIGURE 6 – ADDRESS ACCESS TIME versus V_{DD} SUPPLY VOLTAGE

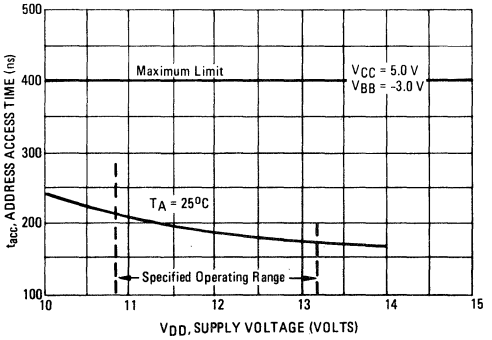
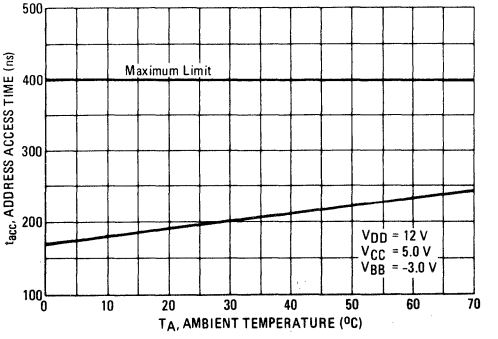


FIGURE 7 – ADDRESS ACCESS TIME versus TEMPERATURE



MEMORY OPERATION (Using Positive Logic)

Most positive level = 1, most negative level = 0

Address

To select one of the 128 characters, apply the appropriate binary code to the Address inputs (A0 thru A6).

Column Select

To select one of the seven columns of the addressed character to appear at the nine output lines, apply the appropriate binary code to the Column Select inputs (CS0 thru CS2). When CS0 = CS1 = CS2 = 0, the outputs are held low.

3

Shift Control Command (SCC)

For characters which are programmed to be shifted, the SCC output goes to a "1" for all columns (C1 thru C7) of the character. The SCC will be at a logic "0" for all non-shifted characters. The MCM6581 uses the SCC for appropriate characters; the MCM6583 has SCC = "0" for all characters.

Address Access Time, $t_{acc(A)}$

The time delay between a change in the Address inputs and a corresponding change at the output lines with all other inputs held stable.

Column Select Access Time, $t_{acc(CS)}$

The time delay between a change in the Column Select inputs and the appearance of valid information at the output lines, with all other inputs held stable.

Output

For these devices, an output dot is defined as a logic "1" level, and an output blank is defined as a logic "0" level.

Device Protection Considerations

When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit spikes or "glitches" on their outputs when the ac power is switched on and off. For example, the bench power supply programmed to deliver +12 volts may have large transients below ground when the ac power is switched on and off. If this possibility exists, it is suggested that the user switch the dc side of the power supply or protect the device power pins (+12, +5.0 and -3.0 volt) against reverse biasing with clamp diodes. A hot carrier diode such as the MBD501 is suggested for this purpose.

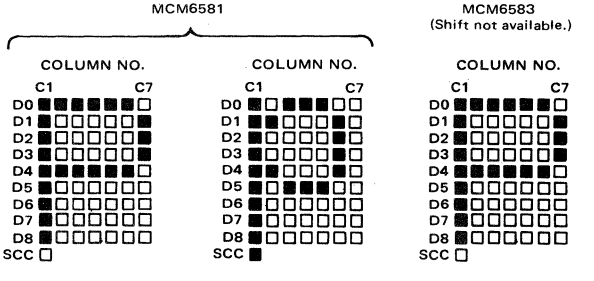
DISPLAY FORMAT

Figure 8 shows the relationship between the logic levels at the Column Select inputs and the corresponding column at the outputs. Note that all outputs are held low (at V_{OL}) when CS0 = CS1 = CS2 = 0. Examples of pre-programmed characters within the MCM6581 and MCM6583 are shown below.

FIGURE 8 – COLUMN SELECT INPUT CODE AND SAMPLE CHARACTERS FOR MCM6581 AND MCM6583

COLUMN SELECT TRUTH TABLE

CS2	CS1	CS0	OUTPUT
0	0	0	0
0	0	1	C1
0	1	0	C2
0	1	1	C3
1	0	0	C4
1	0	1	C5
1	1	0	C6
1	1	1	C7



CUSTOM PROGRAMMING FOR MCM6580

By the programming of a single photomask, the customer may specify the content of the MCM6580. Encoding of the photomask is done with the aid of a computer to provide quick, efficient implementation of the custom bit pattern while reducing the cost of implementation.

Information for the custom memory content may be sent to Motorola in the following forms, in order of preference:*

1. Hexadecimal coding using IBM Punch Cards (Figures 11 and 12).
2. Hexadecimal coding using ASCII Paper Tape Punch (Figure 13).

Programming of the MCM6580 can be achieved by using the following sequence:

1. Create the 128 characters in a 7 x 9 font using the format shown in Figure 9. Note that information at output D0 appears in row one, D1 in row two, thru D8 information in row nine. The dots filled in and programmed as a logic "1" will appear at the outputs as V_{OH}; the dots left blank will be at V_{OL}. (Blank formats appear at the end of this data sheet for your convenience; they are not to be submitted to Motorola, however.)

2. Indicate which characters are shifted by filling in the extra square (dot) at the bottom left (designated as SCC).

3. Convert the characters to hexadecimal coding (Figure 10) treating dots as ones and blanks as zeros. To do this, first rotate the format sheet 90° so that the hex coding squares appear at the left. The hex equivalents of SCC and D8, with the two high order bits both equal zero, are written in the left column of the hex coding table. The hex equivalents of D7 thru D4 are written in the center column, and the hex equivalents of D3 thru D0 in the right column. Note that SCC is programmed only once, in column C1. For columns C2 thru C7, SCC is zero; this makes the three high order bits zero and D8 the only significant factor, with the hex column "0" or "1".

4. Transfer the hex figures either to punched cards (Figure 11) or to paper tape (Figure 13).

5. Submit the programming information to Motorola, together with the Customer's name, Customer's part number, and revision number.

*Note: Motorola can accept magnetic tape and truth table formats. For further information contact your local Motorola sales representative.

3

FIGURE 10 – BINARY TO HEXADECIMAL CONVERSION

MSB 0 D7 D3	0 D6 D2	SCC D5 D1	LSB D8 D4 D0	Hexadecimal Character
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	A
1	0	1	1	B
1	1	0	0	C
1	1	0	1	D
1	1	1	0	E
1	1	1	1	F

0 = V_{OL}
1 = V_{OH}

FIGURE 9 – CHARACTER FORMAT

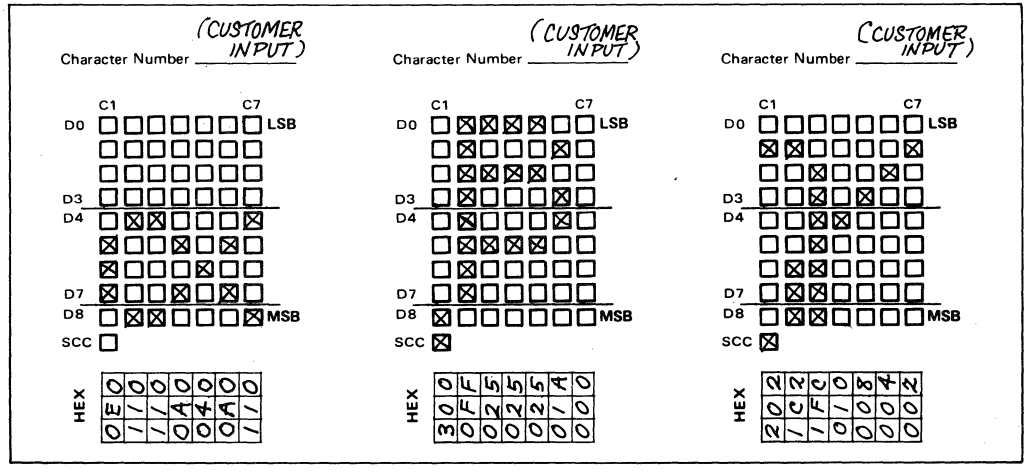


FIGURE 11 – CARD PUNCH FORMAT

Columns	
1 - 10	Blank
11	Asterisk (*)
12 - 32	Hex coding for first character
33	Slash (/)
34 - 54	Hex coding for second character
55	Slash (/)
56 - 76	Blank
77 - 78	Card number (starting 01; thru 64)
79 - 80	Blank

Column 12 on the first card contains the hexadecimal equivalent of SCC and D8 for C1 of the first character. Column 13 contains D7 thru D4, and column 14 contains D3 thru D0. Columns 15 thru 17 contain information for C2 (SCC is programmed only with C1). The entire first character is coded in columns 12 thru 32. Each card contains the coding for two characters. 64 cards are required to program the entire 128 characters. The characters must be programmed in sequence from the first character to the last in order to establish proper addressing for the part. As an example, the first six characters of the MCM6581 are correctly coded and punched in Figure 12.

3

FIGURE 12 – EXAMPLE OF CARD PUNCH FORMAT
(First 6 Characters of MCM6581)

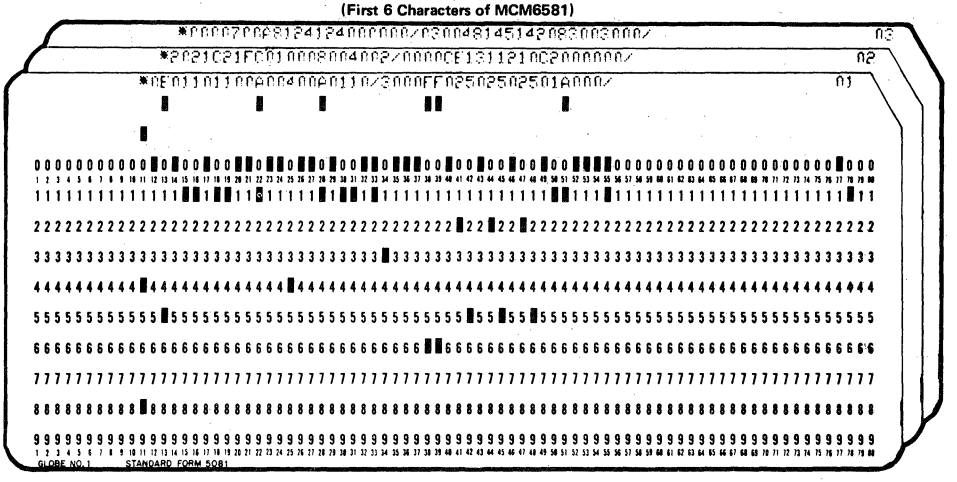


FIGURE 13 – PAPER TAPE FORMAT

Frames	
Leader	Blank Tape
1 to M	Allowed for customer use (M≤64)
M + 1, M + 2	CR; LF (Carriage Return; Line Feed)
M + 3 to M + 65	First line of pattern information (63 hex figures per line – 3 full characters)
M + 66, M + 67	CR; LF
M + 68 to M + 2776	Remaining 42 lines of hex figures, each line followed by a Carriage Return and Line Feed

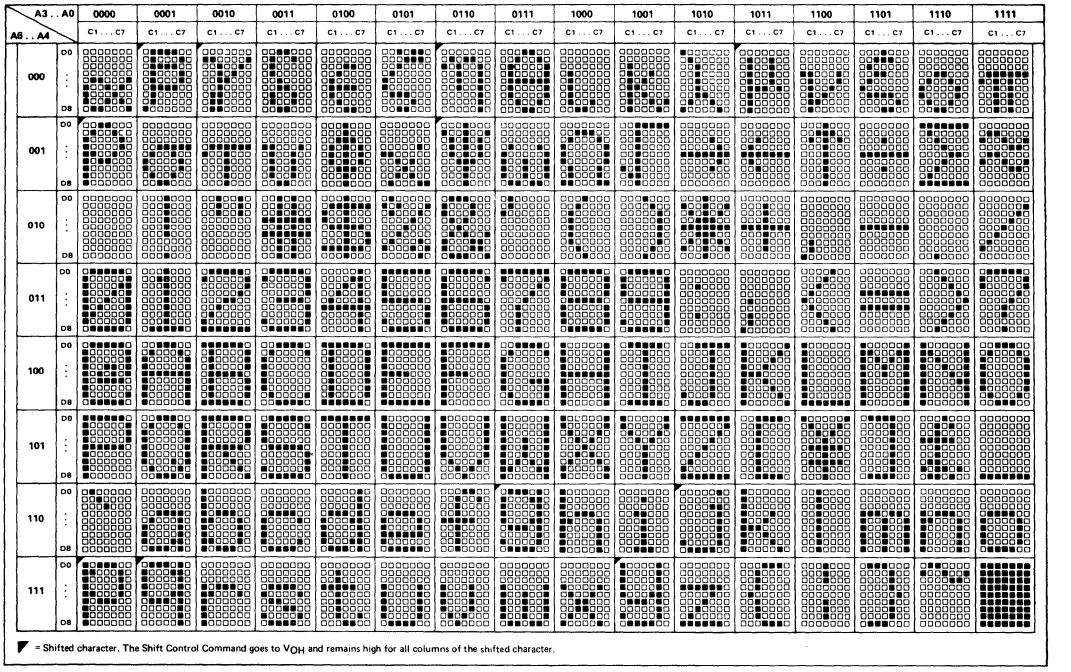
Blank Tape

Frames 1 to M are left to the customer for internal identification, where M ≤ 64. Any combination of alphanumerics may be used. This information is terminated with a Carriage Return and Line Feed, delineating the start of data entry. (Note that the tape cannot begin with a CR and/or LF, or the customer identification will be assumed to be programming data.)

Frame M + 3 contains the hexadecimal equivalent of SCC and D8 for C1 of the first character. Frame M + 4 contains D7 thru D4, and M + 5 contains D3 thru D0. Frames M + 6 thru M + 8 contain information for C2 (SCC is programmed only with C1). Frames M + 8 to M + 65 contain the coding for the first three 7 x 9 characters, since 21 hex figures are required for each character. This is the first line of the printout, and is terminated with a CR and LF.

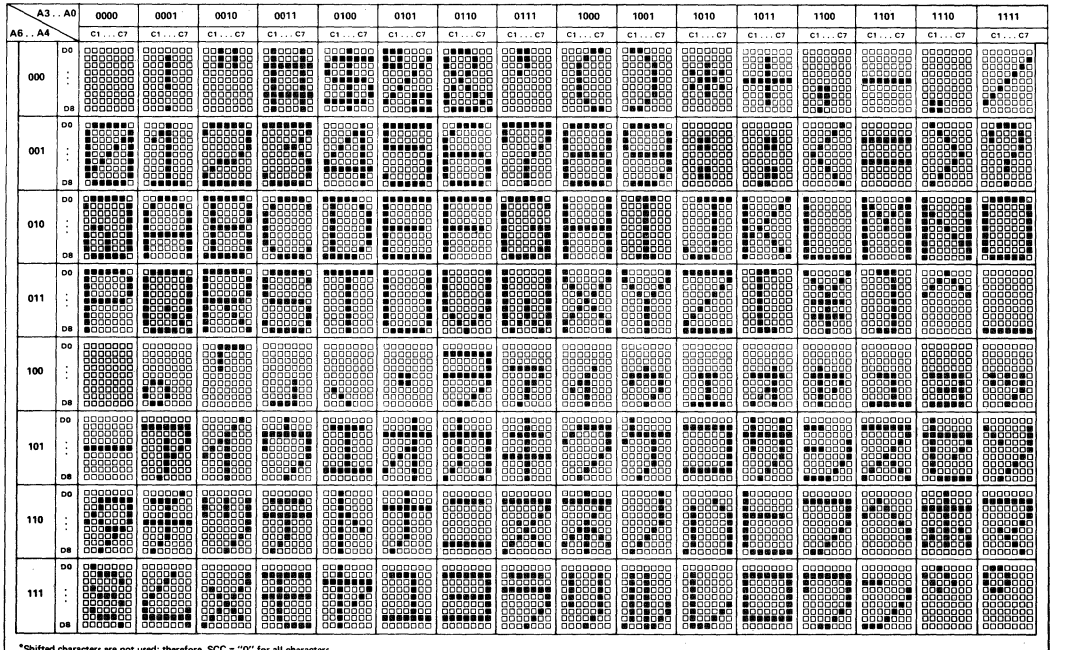
Since three characters are programmed per line, a total of 43 lines are required to program the full 128 characters, with the last line programming only two. The lines are punched in sequence using the format given, with each line terminated with a CR and LF. The last line contains only 42 hex figures to program the last two characters. CR and LF are punched right after the last hex figure, rather than 21 frames later as for the other lines.

FIGURE 14 – MCM6581 PATTERN



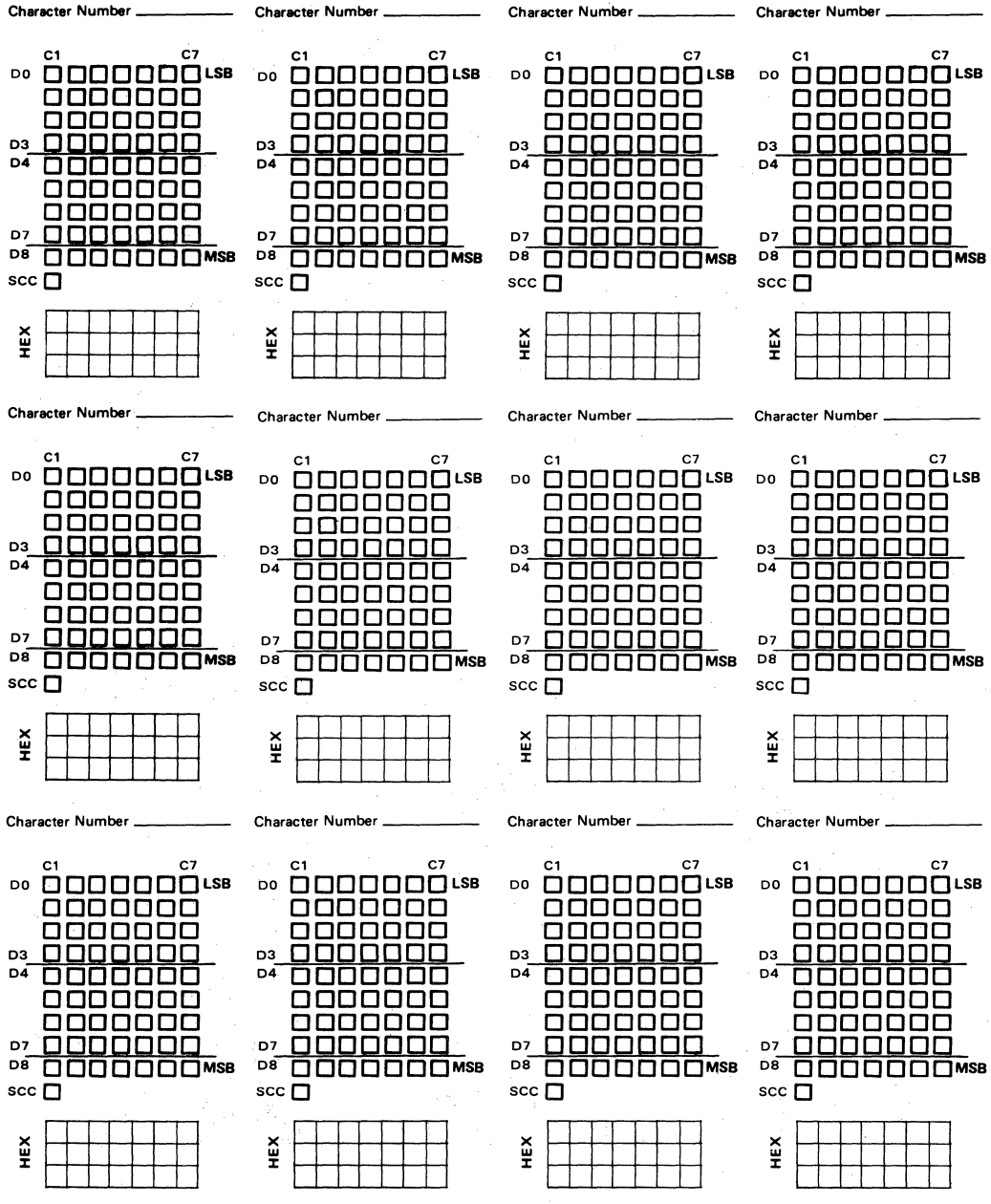
◤ = Shifted character. The Shift Control Command goes to V_{OH} and remains high for all columns of the shifted character.

FIGURE 15 – MCM6583 PATTERN*



*Shifted characters are not used; therefore, SCC = "0" for all characters.

The formats below are given for your convenience in preparing character information for MCM6580 programming. THESE FORMATS ARE NOT TO BE USED TO TRANSMIT THE INFORMATION TO MOTOROLA. Refer to the Custom Programming instructions for detailed procedures.



MCM6590L
MCM6591L

16, 384-BIT READ ONLY MEMORIES

The MCM6590 and MCM6591 static 2048 x 8-bit Read Only Memories are fabricated using N-channel metal gate technology. The MCM6590 is a mask programmable device with a programmable chip select option.

The MCM6591 is a pre-programmed version of the MCM6590 containing six character conversion codes (ASCII to Selectric, EBCDIC, and a modified 8-bit Hollerith; Selectric to ASCII, EBCDIC to ASCII, and a modified Hollerith to ASCII) as well as 128 USASCII characters using mixed character fonts of 5 x 7 and 7 x 7 dot matrices with extra check bits.

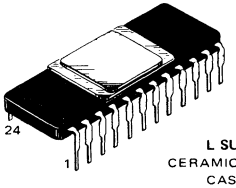
- Static Operation
- TTL Compatibility
- CMOS Compatibility (5 V)
- 3-State Outputs
- 2048 Words by 8-Bit Organization
- 800 ns Maximum Access Time
- Programmable Chip Select
- Wire-OR Capability

Selectric is a registered trademark of IBM.

MOS

(N-CHANNEL, LOW THRESHOLD)

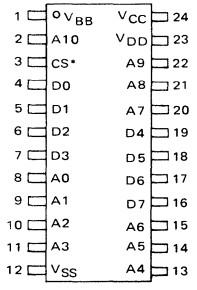
16K
READ ONLY MEMORIES



L SUFFIX
CERAMIC PACKAGE
CASE 684

3

PIN ASSIGNMENT



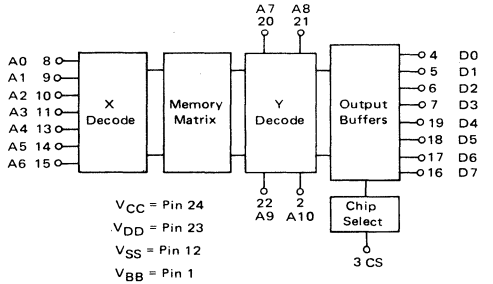
*MCM6591 is pre-programmed to be selected with a low input at CS.

ABSOLUTE MAXIMUM RATINGS[1] (Referenced to V_{SS})

Rating	Symbol	Value	Unit
Supply Voltages	V_{DD} V_{CC} V_{BB}	-0.3 to +15 -0.3 to +6.0 -10 to +0.3	Vdc
Address/Control Input Voltage	V_{in}	-0.3 to +15	Vdc
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-55 to +125	°C

Note 1: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

BLOCK DIAGRAM



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted.)

RECOMMENDED DC OPERATING CONDITIONS (Referenced to V_{SS} = Ground)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{DD}	10.8	12	13.2	Vdc
	V_{CC}	4.75	5.0	5.25	Vdc
	V_{BB}	-3.3	-3.0	-2.7	Vdc
Input High Voltage (A_n, CS)	V_{IH}	3.0	–	V_{CC}	Vdc
Input Low Voltage (A_n, CS)	V_{IL}	-0.3	–	0.8	Vdc

DC CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit
Input Leakage Current (A_n, CS) ($V_{IH} = V_{IL}$min to V_{IH}max)	I_{in}	–	–	10	μAdc
Output Leakage Current (Three-State) (V_{CC} = 5.25 V)	I_{LO}	–	–	10	μAdc
Output High Voltage (I_{OH} = -40 μA)	V_{OH}	3.0	–	V_{CC}	Vdc
Output Low Voltage (I_{OL} = 1.6 mA)	V_{OL}	0	–	0.4	Vdc
Supply Current	I_{DD}	–	–	15	mAdc
(Chip Deselected or Selected)	I_{CC}	–	–	45	mAdc
	I_{BB}	–	–	100	μAdc

CAPACITANCE (Periodically Sampled Rather Than 100% Tested.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Capacitance (f = 1 MHz)	C_{in}	–	6.0	8.0	pF
Output Capacitance (f = 1 MHz)	C_{out}	–	6.0	10	pF

AC CHARACTERISTICS

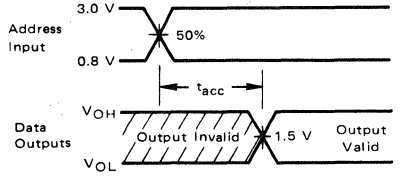
(Full operating voltage and temperature range unless otherwise noted. All timing with $t_r = t_f \leq 20$ ns; Load = 1 TTL Gate (MC7400 Series) biased to draw 1.6 mA; C_L = 30 pF.)

Characteristic	Symbol	Min	Typ*	Max	Unit
Address Access Time	t_{acc}	–	450*	800	ns
Output Select Time	t_{OS}	–	200*	300	ns
Output Deselect Time	t_{OD}	–	200*	300	ns

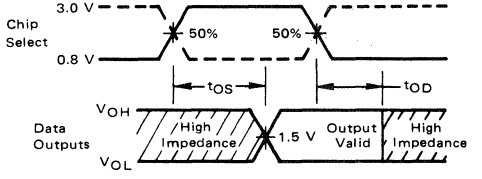
*Typical values measured at 25°C and nominal supply voltages.

FIGURE 1 – TIMING DIAGRAM

A. ADDRESS ACCESS TIMING DIAGRAM (Chip Selected)



B. CHIP SELECT TIMING DIAGRAM (Addresses Established)



TYPICAL CHARACTERISTIC CURVES

FIGURE 2 – ACCESS TIME versus TEMPERATURE

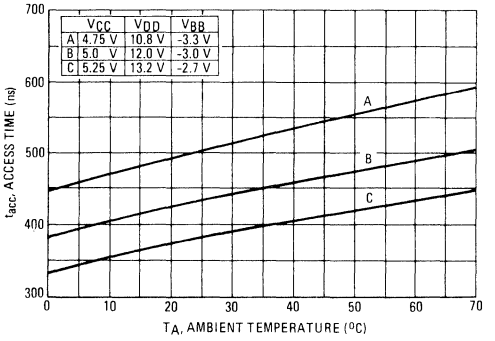


FIGURE 3 – OUTPUT SELECT TIME versus TEMPERATURE

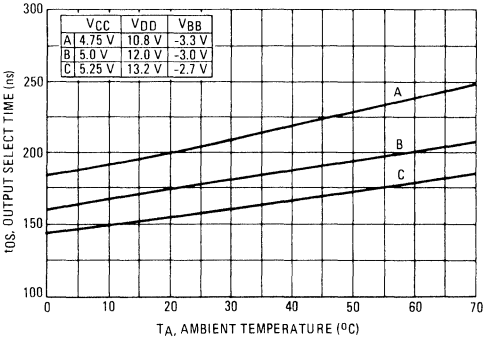


FIGURE 4 – OUTPUT DESELECT TIME versus TEMPERATURE

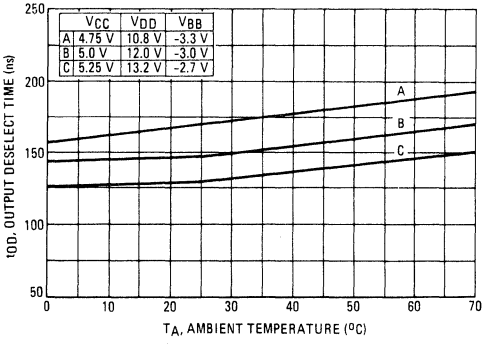


FIGURE 5 – I_{CC} SUPPLY CURRENT versus V_{CC}*

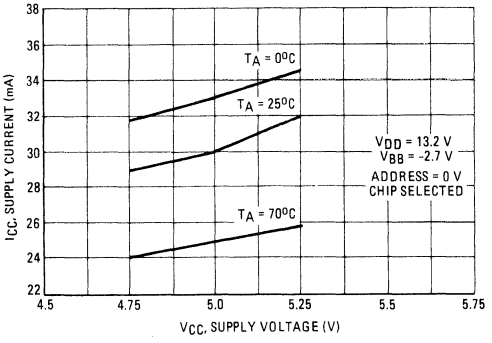


FIGURE 6 – I_{DD} SUPPLY CURRENT versus V_{DD}*

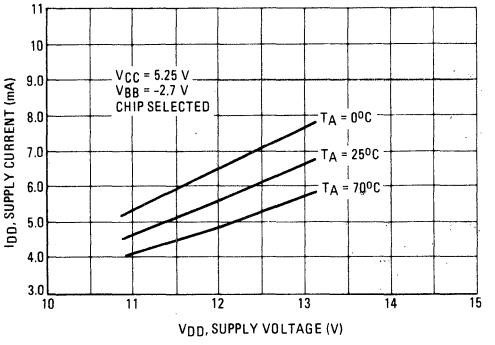
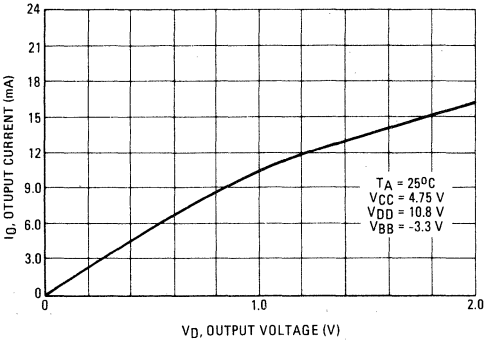


FIGURE 7 – OUTPUT SINK CURRENT versus OUTPUT VOLTAGE



*These curves represent averaged MCM6591 currents over address cycling in the selected mode. More dense patterns can be expected to shift these curves upward, bounded by the maximum dc values stated in the DC Characteristics Table.

CUSTOM PROGRAMMING FOR MCM6590

By the programming of a single photomask for the MCM6590, the customer may specify the content of the memory and the method of selecting the outputs.

Information for custom memory content may be sent to Motorola in the following forms, in order of preference:*

1. Hexadecimal coding using IBM Punch Cards (Figures 8 and 9).
2. Hexadecimal coding using ASCII Paper Tape Punch (Figures 9 and 10).

As Figure 9 indicates, a zero programmed in the memory appears at D_n as V_{OL}. A programmed one appears as V_{OH}.

To program the mode of selecting the chip, the information in Figure 11 is required. This information must be in written form and must accompany the punched cards or paper tape. (A copy of Figure 11 may be used for this purpose.)

*Note: Motorola can accept magnetic tape and truth table formats. For further information contact your local Motorola sales representative.

3

FIGURE 8 – CARD PUNCH FORMAT

Columns	
12 - - 75	Hexadecimal data coding
77 - - 78	Card number (starting 01)
79 - - 80	Total number of cards (64)

Column 12 on the first card contains the hexadecimal equivalent of bits D7 thru D4 of byte 0, while column 13 contains the hexadecimal equivalent of bits D3 thru D0. Columns 14 and 15 contain byte 1, columns 16 and 17 byte 2, and so on.

The first card contains the first 32 bytes. Columns 12 and 13 on the second card will contain byte 32 (the 33rd byte). A total of 64 cards will contain 2048 bytes of 8-bits.

FIGURE 9 – BINARY TO HEXADECIMAL CONVERSION

MSB D7 D3	D6 D2	D5 D1	LSB D4 D0	Hexadecimal Character
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	A
1	0	1	1	B
1	1	0	0	C
1	1	0	1	D
1	1	1	0	E
1	1	1	1	F

$0 = V_{OL}$
$1 = V_{OH}$

FIGURE 10 – PAPER TAPE FORMAT

Frames	
Leader	Blank Tape
1 to M	Allowed for customer use ($M \leqslant 64$)
M + 1, M + 2	CR; LF (Carriage Return; Line Feed)
M + 3 to M + 66	First line of pattern information (64 hex figures per line)
M + 67, M + 68	CR; LF
M + 69 to M + 4426	Remaining 63 lines of hex figures, each line followed by a Carriage Return and Line Feed

Blank Tape

Frames 1 to M are left to the customer for internal identification, where $M \leqslant 64$. Any combination of alphanumerics may be used. This information is terminated with a Carriage Return and Line Feed, delineating the start of data entry. (Note that the tape cannot begin with a CR and/or LF, or the customer identification will be assumed to be programming data.)

Frame M + 3 contains the hexadecimal equivalent of bits D7 thru D4 of byte 0. Frame M + 4 contains bits D3 thru D0. These two hex figures together program byte 0. Likewise, frames M + 5 and M + 6 program byte 1, while M + 7 and M + 8 program byte 2. Frames M + 3 to M + 66 comprise the first line of the printout, and program, in sequence, the first 32 bytes of storage. The line is terminated with a CR and LF.

The remaining 63 lines of data are punched in sequence using the same format, each line terminated with a CR and LF. The total 64 lines of data contain 64 x 64 or 4096 characters. Since each character programs 4 bits of information, a full 16,384 bits are programmed.

As an example, suppose the code conversion in Figure 13 is re-programmed from address 0 to address 127. A printout of the punched tape would read as shown below (a CR and LF is implicit at the end of each line):

```
CUSTOMER IDENTIFICATION USING ONLY ALPHANUMERIC CHARACTERS
A0B1B23335B736B8B430FA3912938E847478EEF565E4EB636CE81EE29A0A031B
21ED2EF6277269E16FF38B77998D08006AE7BD66F0BB71ACAFF91E2D140987FF
A07DC0A3A5A6BEAA24A95A2812110584D4D84E55C5444BC3CC481E429C0A1790
3C4D2E5622D2C941CF530CD71D8D8800CA472BC6503AD1AC3F591E5F14090F00
```

FIGURE 11 – FORMAT FOR PROGRAMMING CHIP SELECT

ORGANIZATIONAL DATA
MCM6590L MOS READ ONLY MEMORY

Customer _____

Customer Part No. _____

Rev. _____

True Chip Select Options:

I. 1 ☐

II. 0 ☐

III. X ☐

1 is most positive input
0 is most negative input
X is a no connection or
don't care situation.

MCM6591 PATTERN INFORMATION

The MCM6591 is pre-programmed as a code converter and character generator, with the Chip Select input active low. When Address A10 is low, the character generator function is selected. When A10 is high, the device provides the code conversion selected by the other address inputs. The table to the right lists the location of the various functions.

ADDRESS		FUNCTION	FIGURE
From	To		
0	1023	Character Generator (A10 = V_{IL})	12
		Code Conversion (A10 = V_{IH}):	
1024	1151	Selectric to ASCII	13
1152	1279	ASCII to Selectric	14
1280	1535	Modified 8-Bit Hollerith to ASCII	15
1536	1663	ASCII to Modified 8-Bit Hollerith	16
1664	1919	EBCDIC to ASCII	17
1920	2047	ASCII to EBCDIC	18

FIGURE 12 – MCM6591 CHARACTER GENERATOR CODE

Addresses 0 to 1023 of the MCM6591 have been programmed with the 128 USASCII characters shown, using mixed 5 x 7 and 7 x 7 fonts with extra check bits. A10 is held low for this function.

■ Usable Character ⧈ Check Bits

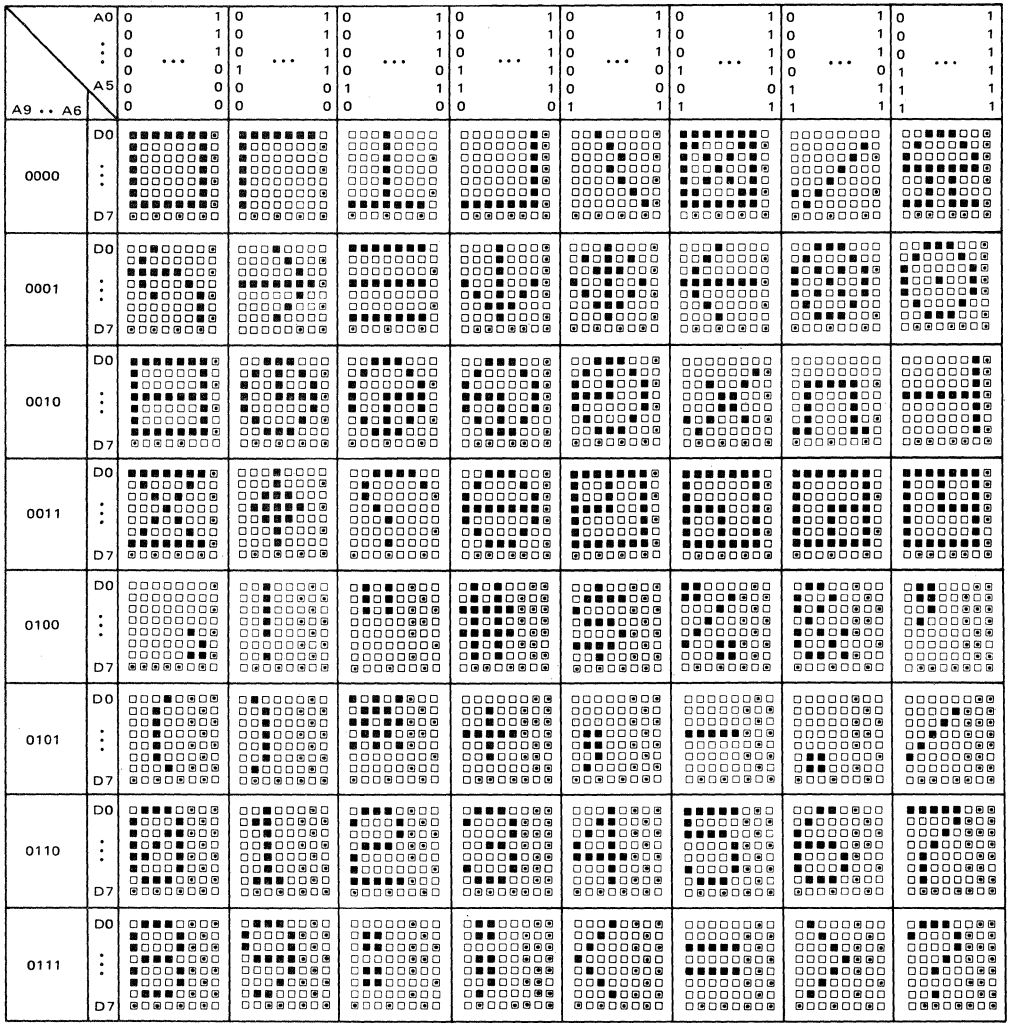
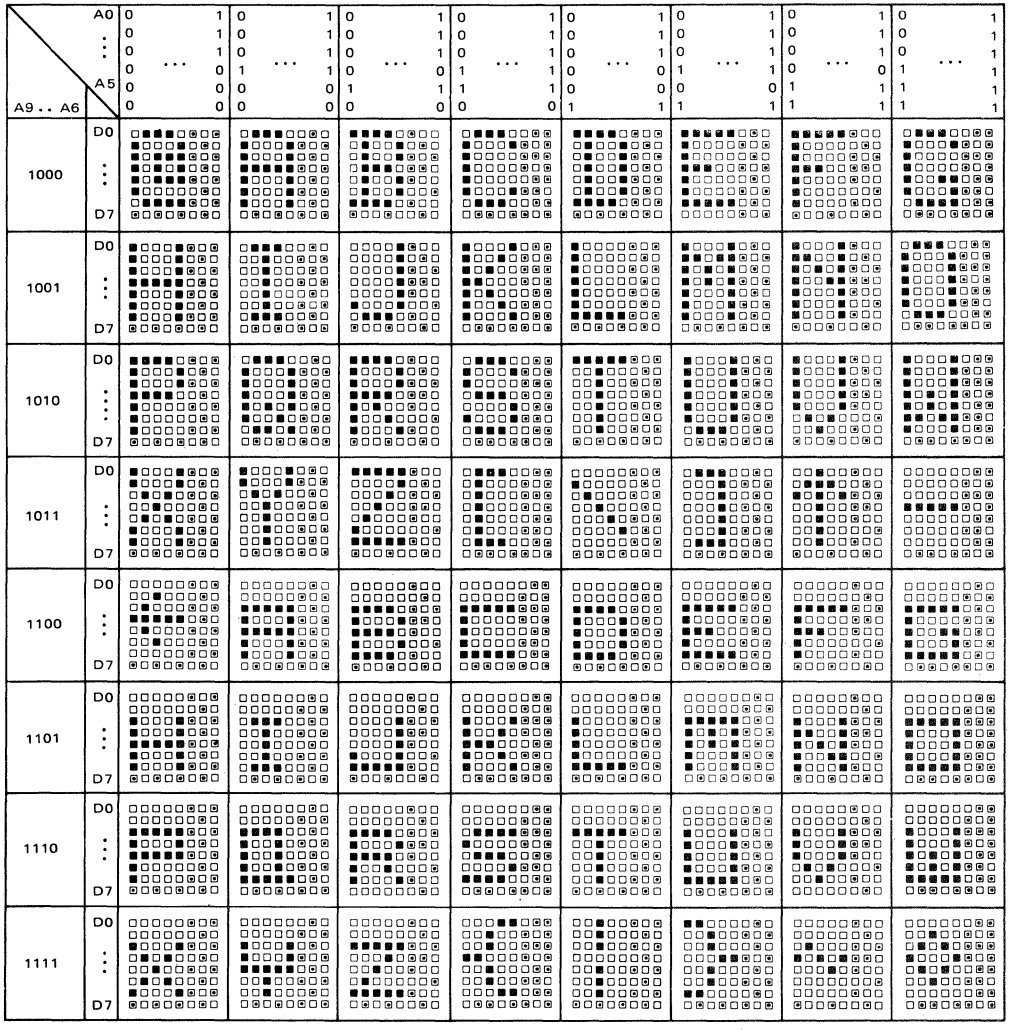


FIGURE 12 – MCM6591 CHARACTER GENERATOR CODE (continued)

■ Usable Character ⊡ Check Bits



MCM 6591 CODE CONVERSION

Tables 13 through 18 present the coding used in the code conversion sections of the MCM6591. A10 is held high for all code conversions.

The addresses are given both in decimal and hexadecimal form in these figures. The outputs are given in hexadecimal form only. The format is illustrated in the following example.

3

Example:

Address		Out
	A10 . . . A0	D7 . . . D0
1047_{10}	10000010111_2	01100011_2
1047_{10}	417_{16}	63_{16}

Table Format

FIGURE 13 – SELECTRIC TO ASCII

Address		Out
1024	400	A0
1025	401	B1
1026	402	B2
1027	403	33
1028	404	35
1029	405	B7
1030	406	36
1031	407	B8
1032	408	B4
1033	409	30
1034	40A	FA
1035	40B	39
1036	40C	12
1037	40D	93
1038	40E	8E
1039	40F	84
1040	410	74
1041	411	78
1042	412	EE
1043	413	F5
1044	414	65
1045	415	E4
1046	416	EB
1047	417	63
1048	418	6C
1049	419	E8
1050	41A	1E
1051	41B	E2
1052	41C	9A
1053	41D	0A
1054	41E	03
1055	41F	1B

Address		Out
1056	420	21
1057	421	ED
1058	422	2E
1059	423	F6
1060	424	27
1061	425	72
1062	426	69
1063	427	E1
1064	428	6F
1065	429	F3
1066	42A	8B
1067	42B	77
1068	42C	99
1069	42D	8D
1070	42E	08
1071	42F	00
1072	430	6A
1073	431	E7
1074	432	BD
1075	433	66
1076	434	F0
1077	435	BB
1078	436	71
1079	437	AC
1080	438	AF
1081	439	F9
1082	43A	1E
1083	43B	2D
1084	43C	14
1085	43D	09
1086	43E	87
1087	43F	FF

Address		Out
1088	440	A0
1089	441	7D
1090	442	C0
1091	443	A3
1092	444	A5
1093	445	A6
1094	446	BE
1095	447	AA
1096	448	24
1097	449	A9
1098	44A	5A
1099	44B	28
1100	44C	12
1101	44D	11
1102	44E	05
1103	44F	84
1104	450	D4
1105	451	D8
1106	452	4E
1107	453	55
1108	454	C5
1109	455	44
1110	456	4B
1111	457	C3
1112	458	CC
1113	459	48
1114	45A	1E
1115	45B	42
1116	45C	9C
1117	45D	0A
1118	45E	17
1119	45F	90

Address		Out
1120	460	3C
1121	461	4D
1122	462	2E
1123	463	56
1124	464	22
1125	465	D2
1126	466	C9
1127	467	41
1128	468	CF
1129	469	53
1130	46A	0C
1131	46B	D7
1132	46C	1D
1133	46D	8D
1134	46E	88
1135	46F	00
1136	470	CA
1137	471	47
1138	472	2B
1139	473	C6
1140	474	50
1141	475	3A
1142	476	D1
1143	477	AC
1144	478	3F
1145	479	59
1146	47A	1E
1147	47B	5F
1148	47C	14
1149	47D	09
1150	47E	0F
1151	47F	00

FIGURE 14 – ASCII TO SELECTRIC

Address		Out
1152	480	AF
1153	481	1B
1154	482	8B
1155	483	1E
1156	484	0F
1157	485	4E
1158	486	BB
1159	487	BE
1160	488	2E
1161	489	BD
1162	48A	1D
1163	48B	AA
1164	48C	6A
1165	48D	2D
1166	48E	8E
1167	48F	7E
1168	490	5F
1169	491	4D
1170	492	0C
1171	493	8D
1172	494	3C
1173	495	A0
1174	496	6F
1175	497	DE
1176	498	A0
1177	499	AC
1178	49A	9C
1179	49B	9F
1180	49C	5C
1181	49D	6C
1182	49E	6C
1183	49F	5C

Address		Out
1184	4A0	00
1185	4A1	A0
1186	4A2	E4
1187	4A3	C3
1188	4A4	48
1189	4A5	44
1190	4A6	C5
1191	4A7	24
1192	4A8	4B
1193	4A9	C9
1194	4AA	47
1195	4AB	72
1196	4AC	B7
1197	4AD	BB
1198	4AE	E2
1199	4AF	B8
1200	4B0	09
1201	4B1	81
1202	4B2	82
1203	4B3	03
1204	4B4	88
1205	4B5	84
1206	4B6	06
1207	4B7	05
1208	4B8	87
1209	4B9	8B
1210	4BA	F5
1211	4BB	35
1212	4BC	60
1213	4BD	B2
1214	4BE	C6
1215	4BF	78

Address		Out
1216	4C0	42
1217	4C1	E7
1218	4C2	DB
1219	4C3	D7
1220	4C4	55
1221	4C5	D4
1222	4C6	F3
1223	4C7	71
1224	4C8	59
1225	4C9	66
1226	4CA	F0
1227	4CB	56
1228	4CC	D8
1229	4CD	E1
1230	4CE	D2
1231	4CF	E8
1232	4D0	74
1233	4D1	F6
1234	4D2	65
1235	4D3	69
1236	4D4	50
1237	4D5	53
1238	4D6	63
1239	4D7	EB
1240	4D8	D1
1241	4D9	F9
1242	4DA	CA
1243	4DB	41
1244	4DC	41
1245	4DD	41
1246	4DE	41
1247	4DF	7B

Address		Out
1248	4E0	77
1249	4E1	27
1250	4E2	1B
1251	4E3	17
1252	4E4	95
1253	4E5	14
1254	4E6	33
1255	4E7	B1
1256	4E8	99
1257	4E9	A6
1258	4EA	30
1259	4EB	96
1260	4EC	18
1261	4ED	21
1262	4EE	12
1263	4EF	28
1264	4F0	B4
1265	4F1	36
1266	4F2	A5
1267	4F3	A9
1268	4F4	90
1269	4F5	93
1270	4F6	A3
1271	4F7	2B
1272	4F8	11
1273	4F9	39
1274	4FA	0A
1275	4FB	41
1276	4FC	41
1277	4FD	41
1278	4FE	41
1279	4FF	3F

FIGURE 15 – MODIFIED 8-BIT HOLLERITH TO ASCII

Address		Out
1280	500	20
1281	501	31
1282	502	32
1283	503	33
1284	504	34
1285	505	35
1286	506	36
1287	507	37
1288	508	38
1289	509	60
1290	50A	3A
1291	50B	23
1292	50C	40
1293	50D	27
1294	50E	3D
1295	50F	22
1296	510	39
1297	511	91

Address		Out
1298	512	16
1299	513	93
1300	514	94
1301	515	95
1302	516	96
1303	517	04
1304	518	98
1305	519	99
1306	51A	9A
1307	51B	9B
1308	51C	14
1309	51D	15
1310	51E	9E
1311	51F	1A
1312	520	30
1313	521	2F
1314	522	53
1315	523	54

Address		Out
1316	524	55
1317	525	56
1318	526	57
1319	527	58
1320	528	59
1321	529	B9
1322	52A	5C
1323	52B	2C
1324	52C	25
1325	52D	5F
1326	52E	3E
1327	52F	3F
1328	530	5A
1329	531	81
1330	532	82
1331	533	83
1332	534	84
1333	535	0A

Address		Out
1334	536	17
1335	537	1B
1336	538	88
1337	539	89
1338	53A	8A
1339	53B	8B
1340	53C	8C
1341	53D	05
1342	53E	06
1343	53F	07
1344	540	2D
1345	541	4A
1346	542	4B
1347	543	4C
1348	544	4D
1349	545	4E
1350	546	4F
1351	547	50

(continued)

FIGURE 15 – MODIFIED 8-BIT HOLLERITH TO ASCII (continued)

Address		Out
1352	548	51
1353	549	B1
1354	54A	5D
1355	54B	24
1356	54C	2A
1357	54D	29
1358	54E	3B
1359	54F	5E
1360	550	52
1361	551	11
1362	552	12
1363	553	13
1364	554	9D
1365	555	85
1366	556	08
1367	557	87
1368	558	18
1369	559	19
1370	55A	92
1371	55B	8F
1372	55C	1C
1373	55D	1D
1374	55E	1E
1375	55F	1F
1376	560	7D
1377	561	7E
1378	562	73
1379	563	74
1380	564	75
1381	565	76
1382	566	77
1383	567	78
1384	568	79
1385	569	D1
1386	56A	D2
1387	56B	D3
1388	56C	D4
1389	56D	D5
1390	56E	D6
1391	56F	D7
1392	570	7A
1393	571	9F
1394	572	B2
1395	573	B3
1396	574	B4
1397	575	B5

Address		Out
1398	576	B6
1399	577	B7
1400	578	B8
1401	579	80
1402	57A	F4
1403	57B	F5
1404	57C	F6
1405	57D	F7
1406	57E	F8
1407	57F	F9
1408	580	26
1409	581	41
1410	582	42
1411	583	43
1412	584	44
1413	585	45
1414	586	46
1415	587	47
1416	588	48
1417	589	A8
1418	58A	5B
1419	58B	2E
1420	58C	3C
1421	58D	28
1422	58E	2B
1423	58F	21
1424	590	49
1425	591	01
1426	592	02
1427	593	03
1428	594	9C
1429	595	09
1430	596	86
1431	597	7F
1432	598	97
1433	599	8D
1434	59A	8E
1435	59B	0B
1436	59C	0C
1437	59D	0D
1438	59F	0E
1439	59F	0F
1440	5A0	7B
1441	5A1	61
1442	5A2	62
1443	5A3	63

Address		Out
1444	5A4	64
1445	5A5	65
1446	5A6	66
1447	5A7	67
1448	5A8	68
1449	5A9	C3
1450	5AA	C4
1451	5AB	C5
1452	5AC	C6
1453	5AD	C7
1454	5AE	C8
1455	5AF	C9
1456	5B0	69
1457	5B1	A0
1458	5B2	A1
1459	5B3	A2
1460	5B4	A3
1461	5B5	A4
1462	5B6	A5
1463	5B7	A6
1464	5B8	A7
1465	5B9	10
1466	5BA	E8
1467	5BB	E9
1468	5BC	EA
1469	5BD	EB
1470	5BE	EC
1471	5BF	ED
1472	5C0	7C
1473	5C1	6A
1474	5C2	6B
1475	5C3	6C
1476	5C4	6D
1477	5C5	6E
1478	5C6	6F
1479	5C7	70
1480	5C8	71
1481	5C9	CA
1482	5CA	CB
1483	5CB	CC
1484	5CC	CD
1485	5CD	2E
1486	5CE	CF
1487	5CF	D0
1488	5D0	72
1489	5D1	A9

Address		Out
1490	5D2	AA
1491	5D3	AB
1492	5D4	AC
1493	5D5	AD
1494	5D6	AE
1495	5D7	AF
1496	5D8	B0
1497	5D9	00
1498	5DA	EE
1499	5DB	EF
1500	5DC	F0
1501	5DD	F1
1502	5DE	F2
1503	5DF	F3
1504	5E0	BA
1505	5E1	D9
1506	5E2	DA
1507	5E3	DB
1508	5E4	DC
1509	5E5	DD
1510	5E6	DE
1511	5E7	DF
1512	5E8	E0
1513	5E9	D8
1514	5EA	E2
1515	5EB	E3
1516	5EC	E4
1517	5ED	E5
1518	5EE	E6
1519	5EF	E7
1520	5F0	E1
1521	5F1	BB
1522	5F2	BC
1523	5F3	BD
1524	5F4	BE
1525	5F5	BF
1526	5F6	C0
1527	5F7	C1
1528	5F8	C2
1529	5F9	90
1530	5FA	FA
1531	5FB	FB
1532	5FC	FC
1533	5FD	FD
1534	5FE	FE
1535	5FF	FF

FIGURE 16 – ASCII TO MODIFIED 8-BIT HOLLERITH

Address		Out
1536	600	D9
1537	601	91
1538	602	92
1539	603	93
1540	604	87
1541	605	CD
1542	606	CE
1543	607	CF
1544	608	A6
1545	609	95
1546	60A	C5

Address		Out
1547	60B	9B
1548	60C	9C
1549	60D	9D
1550	60E	9E
1551	60F	9F
1552	610	B9
1553	611	A1
1554	612	A2
1555	613	A3
1556	614	8C
1557	615	8D

Address		Out
1558	616	82
1559	617	C6
1560	618	A8
1561	619	A9
1562	61A	8F
1563	61B	C7
1564	61C	AC
1565	61D	AD
1566	61E	AE
1567	61F	AF
1568	620	00

Address		Out
1569	621	1F
1570	622	0F
1571	623	0B
1572	624	2B
1573	625	4C
1574	626	10
1575	627	0D
1576	628	1D
1577	629	2D
1578	62A	2C
1579	62B	1E

(continued)

FIGURE 16 – ASCII TO MODIFIED 8-BIT HOLLERITH (continued)

Address		Out
1580	62C	4B
1581	62D	20
1582	62E	1B
1583	62F	41
1584	630	40
1585	631	01
1586	632	02
1587	633	03
1588	634	04
1589	635	05
1590	636	06
1591	637	07
1592	638	08
1593	639	80
1594	63A	0A
1595	63B	2E
1596	63C	1C
1597	63D	0E
1598	63E	4E
1599	63F	4F
1600	640	0C

Address		Out
1601	641	11
1602	642	12
1603	643	13
1604	644	14
1605	645	15
1606	646	16
1607	647	17
1608	648	18
1609	649	90
1610	64A	21
1611	64B	22
1612	64C	23
1613	64D	24
1614	64E	25
1615	64F	26
1616	650	27
1617	651	28
1618	652	A0
1619	653	42
1620	654	43
1621	655	44

Address		Out
1622	656	45
1623	657	46
1624	658	47
1625	659	48
1626	65A	C0
1627	65B	1A
1628	65C	4A
1629	65D	2A
1630	65E	2F
1631	65F	4D
1632	660	09
1633	661	51
1634	662	52
1635	663	53
1636	664	54
1637	665	55
1638	666	56
1639	667	57
1640	668	58
1641	669	D0
1642	66A	31

Address		Out
1643	66B	32
1644	66C	33
1645	66D	34
1646	66E	35
1647	66F	36
1648	670	37
1649	671	38
1650	672	B0
1651	673	62
1652	674	63
1653	675	64
1654	676	65
1655	677	66
1656	678	67
1657	679	68
1658	67A	E0
1659	67B	50
1660	67C	30
1661	67D	60
1662	67E	61
1663	67F	97

FIGURE 17 – EBCDIC TO ASCII

Address		Out
1664	680	00
1665	681	01
1666	682	02
1667	683	03
1668	684	00
1669	685	09
1670	686	00
1671	687	7F
1672	688	00
1673	689	00
1674	68A	00
1675	68B	0B
1676	68C	0C
1677	68D	0D
1678	68E	0E
1679	68F	0F
1680	690	10
1681	691	11
1682	692	12
1683	693	13
1684	694	E0
1685	695	DC
1686	696	08
1687	697	00
1688	698	18
1689	699	19
1690	69A	00
1691	69B	00
1692	69C	1C
1693	69D	1D
1694	69E	1E
1695	69F	1F
1696	6A0	00
1697	6A1	00
1698	6A2	00
1699	6A3	00
1700	6A4	00

Address		Out
1701	6A5	0A
1702	6A6	17
1703	6A7	1B
1704	6A8	00
1705	6A9	00
1706	6AA	00
1707	6AB	00
1708	6AC	00
1709	6AD	05
1710	6AE	06
1711	6AF	07
1712	6B0	00
1713	6B1	00
1714	6B2	16
1715	6B3	00
1716	6B4	00
1717	6B5	14
1718	6B6	00
1719	6B7	04
1720	6B8	00
1721	6B9	00
1722	6BA	00
1723	6BB	00
1724	6BC	00
1725	6BD	15
1726	6BE	00
1727	6BF	1A
1728	6C0	A0
1729	6C1	00
1730	6C2	00
1731	6C3	00
1732	6C4	00
1733	6C5	00
1734	6C6	00
1735	6C7	00
1736	6C8	00
1737	6C9	00

Address		Out
1738	6CA	FE
1739	6CB	AE
1740	6CC	BC
1741	6CD	A8
1742	6CE	AB
1743	6CF	FC
1744	6D0	A6
1645	6D1	00
1746	6D2	00
1747	6D3	00
1748	6D4	00
1749	6D5	00
1750	6D6	00
1751	6D7	00
1752	6D8	00
1753	6D9	00
1754	6DA	A1
1755	6DB	A4
1756	6DC	AA
1757	6DD	A9
1758	6DE	BB
1759	6DF	DE
1760	6E0	AD
1761	6E1	AF
1762	6E2	00
1763	6E3	00
1764	6E4	00
1765	6E5	00
1766	6E6	00
1767	6E7	00
1768	6E8	00
1769	6E9	00
1770	6EA	00
1771	6EB	AC
1772	6EC	A5
1773	6ED	DF
1774	6EE	BE

Address		Out
1775	6EF	BF
1776	6F0	00
1777	6F1	00
1778	6F2	00
1779	6F3	00
1780	6F4	00
1781	6F5	00
1782	6F6	00
1783	6F7	00
1784	6F8	00
1785	6F9	00
1786	6FA	BA
1787	6FB	A3
1788	6FC	C0
1789	6FD	A7
1790	6FE	BD
1791	6FF	A2
1792	700	00
1793	701	E1
1794	702	E2
1795	703	E3
1796	704	E4
1797	705	E5
1798	706	E6
1799	707	E7
1800	708	E8
1801	709	E9
1802	70A	00
1803	70B	FB
1804	70C	00
1805	70D	00
1806	70E	00
1807	70F	00
1808	710	00
1809	711	EA
1810	712	EB
1811	713	EC

(continued)

FIGURE 17 – EBCDIC TO ASCII (continued)

Address		Out
1812	714	ED
1813	715	EE
1814	716	EF
1815	717	F0
1816	718	F1
1817	719	F2
1818	71A	00
1819	71B	FD
1820	71C	00
1821	71D	00
1822	71E	00
1823	71F	00
1824	720	00
1825	721	00
1826	722	F3
1827	723	F4
1828	724	F5
1829	725	F6
1830	726	F7
1831	727	F8
1832	728	F9
1833	729	FA
1834	72A	00
1835	72B	00
1836	72C	00
1837	72D	DB
1838	72E	00

Address		Out
1839	72F	00
1840	730	00
1841	731	00
1842	732	00
1843	733	00
1844	734	00
1845	735	00
1846	736	00
1847	737	00
1848	738	00
1849	739	00
1850	73A	00
1851	73B	00
1852	73C	00
1853	73D	DD
1854	73E	00
1855	73F	00
1856	740	00
1857	741	C1
1858	742	C2
1859	743	C3
1860	744	C4
1861	745	C5
1862	746	C6
1863	747	C7
1864	748	C8
1865	749	C9

Address		Out
1866	74A	00
1867	74B	00
1868	74C	00
1869	74D	00
1870	74E	00
1871	74F	00
1872	750	00
1873	751	CA
1874	752	CB
1875	753	CC
1876	754	CD
1877	755	CE
1878	756	CF
1879	757	D0
1880	758	D1
1881	759	D2
1882	75A	00
1883	75B	00
1884	75C	00
1885	75D	00
1886	75E	00
1887	75F	00
1888	760	00
1889	761	00
1890	762	D3
1891	763	D4
1892	764	D5

Address		Out
1893	765	D6
1894	766	D7
1895	767	D8
1896	768	D9
1897	769	DA
1898	76A	00
1899	76B	00
1900	76C	00
1901	76D	00
1902	76E	00
1903	76F	00
1904	770	B0
1905	771	B1
1906	772	B2
1907	773	B3
1908	774	B4
1909	775	B5
1910	776	B6
1911	777	B7
1912	778	B8
1913	779	B9
1914	77A	0C
1915	77B	00
1916	77C	00
1917	77D	00
1918	77E	00
1919	77F	00

FIGURE 18 – ASCII TO EBCDIC

Address		Out
1920	780	00
1921	781	01
1922	782	02
1923	783	03
1924	784	37
1925	785	2D
1926	786	2E
1927	787	2F
1928	788	16
1929	789	05
1930	78A	25
1931	78B	0B
1932	78C	0C
1933	78D	0D
1934	78E	0E
1935	78F	0F
1936	790	10
1937	791	11
1938	792	12
1939	793	13
1940	794	35
1941	795	3D
1942	796	32
1943	797	26
1944	798	18
1945	799	19
1946	79A	3F
1947	79B	24
1948	79C	1C
1949	79D	1D
1950	79E	1E
1951	79F	1F

Address		Out
1952	7A0	40
1953	7A1	5A
1954	7A2	7F
1955	7A3	7B
1956	7A4	5B
1957	7A5	6C
1958	7A6	50
1959	7A7	7D
1960	7A8	4D
1961	7A9	5D
1962	7AA	5C
1963	7AB	4E
1964	7AC	6B
1965	7AD	60
1966	7AE	4B
1967	7AF	61
1968	7B0	F0
1969	7B1	F1
1970	7B2	F2
1971	7B3	F3
1972	7B4	F4
1973	7B5	F5
1974	7B6	F6
1975	7B7	F7
1976	7B8	F8
1977	7B9	F9
1978	7BA	7A
1979	7BB	5E
1980	7BC	4C
1981	7BD	7E
1982	7BE	6E
1983	7BF	6F

Address		Out
1984	7C0	7C
1985	7C1	C1
1986	7C2	C2
1987	7C3	C3
1988	7C4	C4
1989	7C5	C5
1990	7C6	C6
1991	7C7	C7
1992	7C8	C8
1993	7C9	C9
1994	7CA	D1
1995	7CB	D2
1996	7CC	D3
1997	7CD	D4
1998	7CE	D5
1999	7CF	D6
2000	7D0	D7
2001	7D1	D8
2002	7D2	D9
2003	7D3	E2
2004	7D4	E3
2005	7D5	E4
2006	7D6	E5
2007	7D7	E6
2008	7D8	E7
2009	7D9	E8
2010	7DA	E9
2011	7DB	A9
2012	7DC	15
2013	7DD	BD
2014	7DE	5F
2015	7DF	6D

Address		Out
2016	7E0	14
2017	7E1	81
2018	7E2	82
2019	7E3	83
2020	7E4	84
2021	7E5	85
2022	7E6	86
2023	7E7	87
2024	7E8	88
2025	7E9	89
2026	7EA	91
2027	7EB	92
2028	7EC	93
2029	7ED	94
2030	7EE	95
2031	7EF	96
2032	7F0	97
2033	7F1	98
2034	7F2	99
2035	7F3	A2
2036	7F4	A3
2037	7F5	A4
2038	7F6	A5
2039	7F7	A6
2040	7F8	A7
2041	7F9	A8
2042	7FA	A9
2043	7FB	8B
2044	7FC	4F
2045	7FD	9B
2046	7FE	4A
2047	7FF	07

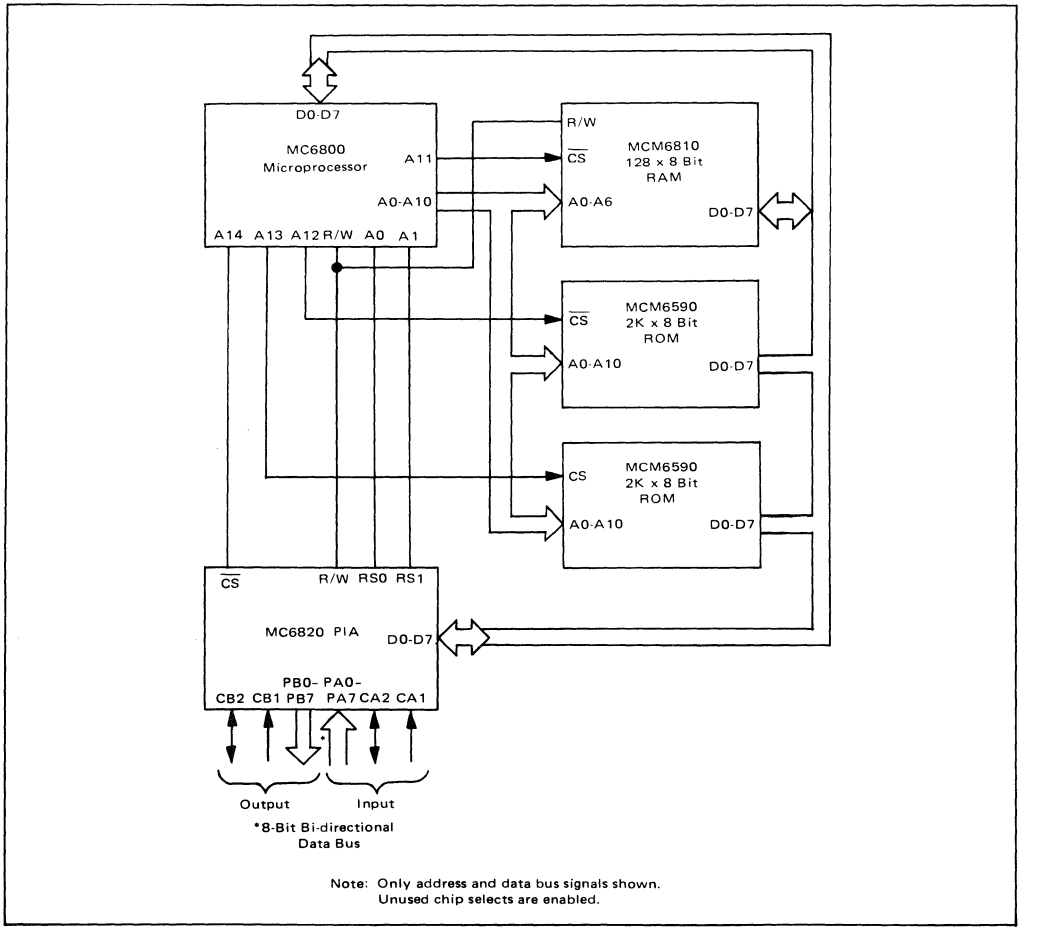
APPLICATIONS INFORMATION

Typical applications for the MCM6590 include microprocessor control storage, CPU microprogramming, code converters, character generators, look-up tables, and random logic replacement.

Figure 19 shows a system controller based on devices from the M6800 Microcomputer Family, and using the MCM6590 to store control programs. Software instructions in the ROMs cause the system to read data from the input lines, perform computations in the RAM, and direct appropriate response by the outputs.

In this minimum system configuration, the need for decoding of the high order address bits is avoided by selecting each device on the address bus with one of the high order address lines (A11-A15). The MCM6590 ROMs are selected by A12 and A13, and the PIA is selected by A14.

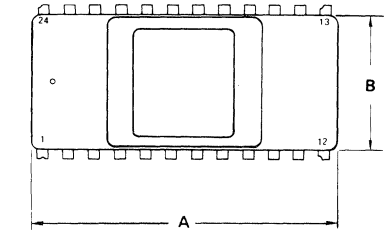
FIGURE 19 – MICROPROCESSOR-BASED SYSTEM CONTROLLER

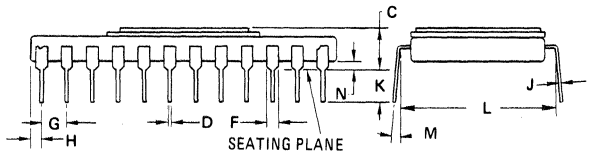


Note: Only address and data bus signals shown.
Unused chip selects are enabled.

3

PACKAGE DIMENSIONS





DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	29.34	30.86	1.155	1.215
B	12.70	14.22	0.500	0.560
C	3.05	3.94	0.120	0.155
D	0.38	0.51	0.015	0.020
F	0.89	1.40	0.035	0.055
G	2.54 BSC		0.100 BSC	
H	0.89	1.40	0.035	0.055
J	0.20	0.30	0.008	0.012
K	2.92	3.68	0.115	0.145
L	14.86	15.87	0.585	0.625
M	–	15^0	–	15^0
N	0.51	1.14	0.020	0.045

NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE WITH MAXIMUM MATERIAL CONDITION.
2. LEAD NO. 1 CUT FOR IDENTIFICATION, OR BUMP ON TOP.
3. DIM "L" TO INSIDE OF LEADS. (MEASURED 0.51 mm (0.020) BELOW PKG BASE)

CASE 684-04

MCM14524AL
MCM14524CL
MCM14524CP

1024-BIT READ ONLY MEMORY

The MCM14524 is a complementary MOS mask programmable Read Only Memory (ROM). This device is ordered as a factory special with its unique pattern specified by the user.

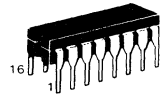
This ROM is organized in a 256 x 4-bit pattern. The contents of a specified address (< A0, A1, A2, A3, A4, A5, A6, A7 >) will appear at the four data outputs (B0, B1, B2, B3) following the negative going edge of the clock. When the clock goes high, the data present at the outputs will be latched. The memory Enable may be taken low asynchronously, forcing the data outputs low and resetting the output latches. This device finds application wherever low power or high noise immunity is a design consideration.

- Diode Protection on All Inputs
- Noise Immunity = 45% of V_{DD} typical
- Quiescent Power Dissipation — 25 nW/package typical @ 5 Vdc
- Single Supply Operation — Either Positive or Negative
- Memory Enable Allows Expansion
- Output Latches Provide a Useful Storage Register

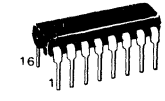
McMOS

(LOW-POWER COMPLEMENTARY MOS)

1024-BIT
(256 x 4)
READ ONLY MEMORY



L SUFFIX
CERAMIC PACKAGE
CASE 620



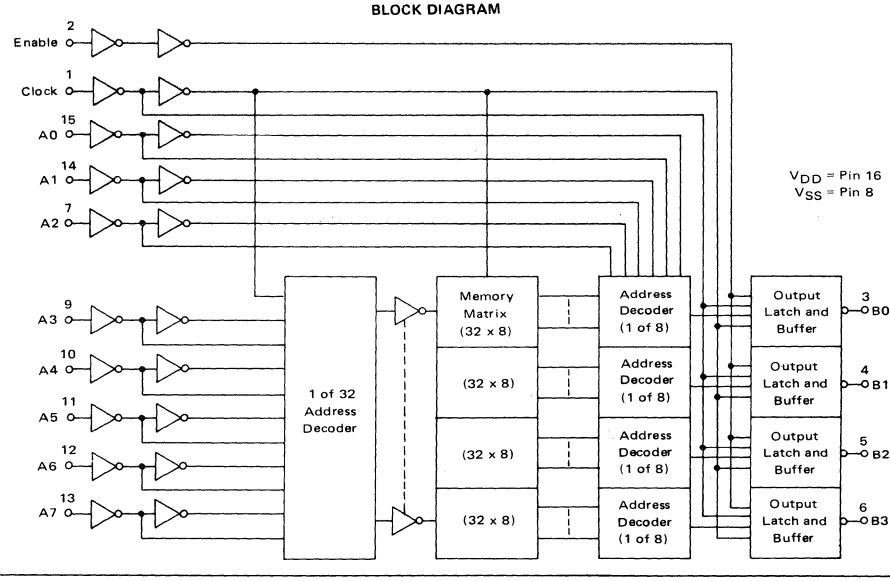
P SUFFIX
PLASTIC PACKAGE
CASE 648

TRUTH TABLE

CLOCK	ENABLE	B0	B1	B2	B3
V_{DD} ⎺_ V_{SS}	1	⟨Address⟩*	⟨Address⟩*	⟨Address⟩*	⟨Address⟩*
V_{SS} _/⎺ V_{DD}	1	OUTPUT DATA LATCHES			
X	0	0	0	0	0

X = Don't Care
*Indicates contents of specified Address will appear at outputs as stated above.

BLOCK DIAGRAM



MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8)

Rating	Symbol	Value	Unit
DC Supply Voltage MCM14524AL MCM14524CL/CP	V_{DD}	+18 to -0.5 +16 to -0.5	Vdc
Input Voltage, All Inputs	V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature — MCM14524AL Range MCM14524CL/CP	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high impedance circuit.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{out}	5.0	–	0.01	–	0	0.01	–	0.05	Vdc
		10	–	0.01	–	0	0.01	–	0.05	
		15	–	0.05	–	0	0.05	–	0.25	
"1" Level		5.0	4.99	–	4.99	5.0	–	4.95	–	Vdc
		10	9.99	–	9.99	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.75	–	
Noise Immunity#	V_{NL}									Vdc
($\Delta V_{out} \leq 0.8$ Vdc)		5.0	1.5	–	1.5	2.25	–	1.4	–	
($\Delta V_{out} \leq 1.0$ Vdc)		10	3.0	–	3.0	4.50	–	2.9	–	
($\Delta V_{out} \leq 1.5$ Vdc)		15	4.5	–	4.5	6.75	–	4.4	–	
($\Delta V_{out} \leq 0.8$ Vdc)	V_{NH}	5.0	1.4	–	1.5	2.25	–	1.5	–	Vdc
($\Delta V_{out} \leq 1.0$ Vdc)		10	2.9	–	3.0	4.50	–	3.0	–	
($\Delta V_{out} \leq 1.5$ Vdc)		15	4.4	–	4.5	6.75	–	4.5	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-0.62	–	-0.50	-1.5	–	-0.35	–	
(V_{OH} = 9.5 Vdc)		10	-0.62	–	-0.50	-0.9	–	-0.35	–	
(V_{OH} = 13.5 Vdc)		15	-1.8	–	-1.5	-3.2	–	-1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.50	–	0.40	0.80	–	0.28	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.1	–	0.90	2.0	–	0.65	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.0	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-0.23	–	-0.20	-1.7	–	-0.16	–	
(V_{OH} = 9.5 Vdc)		10	-0.23	–	-0.20	-0.9	–	-0.16	–	
(V_{OH} = 13.5 Vdc)		15	-0.69	–	-0.60	-3.5	–	-0.48	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.23	–	0.20	0.78	–	0.16	–	mAdc
(V_{OL} = 0.5 Vdc)		10	0.60	–	0.50	2.0	–	0.40	–	
(V_{OL} = 1.5 Vdc)		15	1.8	–	1.5	7.8	–	1.2	–	
Input Current	I_{in}	–	–	–	–	10	–	–	–	pAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	–	–	–	pF
Quiescent Dissipation (AL Device)	P_Q	5.0	–	0.025	–	0.000025	0.025	–	1.5	mW
		10	–	0.10	–	0.00010	0.10	–	6.0	
		15	–	0.30	–	0.00023	0.30	–	18	
Quiescent Dissipation (CL/CP Device)	P_Q	5.0	–	0.25	–	0.000025	0.25	–	3.5	mW
		10	–	1.0	–	0.00010	1.0	–	14	
		15	–	3.0	–	0.00023	3.0	–	42	
Power Dissipation**† (Dynamic plus Quiescent) (C_L = 15 pF)	P_D	5.0	$P_D = (7.0 \text{ mW/MHz}) f + P_Q$							mW
		10	$P_D = (30 \text{ mW/MHz}) f + P_Q$							
		15	$P_D = (75 \text{ mW/MHz}) f + P_Q$							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
†For dissipation at different external load capacitance (C_L) use the formula:

$$P_T(C_L) = P_D + 1 \times 10^{-3} (C_L - 15 \text{ pF}) V_{DD}^2 f$$

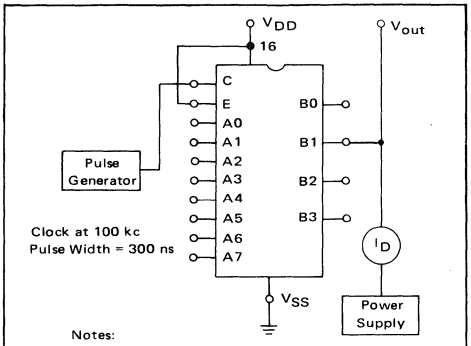
where: P_T, P_D in mW (per package), C_L in pF, V_{DD} in Vdc, and f in MHz is input clock frequency.
**The formula given is for the typical characteristics only.

SWITCHING CHARACTERISTICS (C_L = 15 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min AL Device	Min CL/CP Device	Typ All Type	Max AL Device	Max CL/CP Device	Unit
Clock Read Access Delay Time	t_{accC}							ns
t_{accC} = (1.0 ns/pF) C_L + 1310 ns		5.0	–	–	1325	2650	3975	
t_{accC} = (0.43 ns/pF) C_L + 518 ns		10	–	–	525	1050	1575	
t_{accC} = (0.29 ns/pF) C_L + 351 ns		15	–	–	355	790	1185	
Enable Access Delay Time	t_{accE_n}							ns
t_{accE_n} = (1.14 ns/pF) C_L + 173 ns		5.0	–	–	190	380	570	
t_{accE_n} = (0.57 ns/pF) C_L + 71 ns		10	–	–	80	160	240	
t_{accE_n} = (0.29 ns/pF) C_L + 51 ns		15	–	–	55	120	180	
Output Rise and Fall Time	t_r,t_f							ns
t_r,t_f = (1.7 ns/pF) C_L + 49 ns		5.0	–	–	75	175	200	
t_r,t_f = (1.14 ns/pF) C_L + 18 ns		10	–	–	35	75	110	
t_r,t_f = (0.86 ns/pF) C_L + 12 ns		15	–	–	25	55	85	
Minimum Clock Pulse Width*	PW_{CH}	5.0	–	–	150	300	450	ns
		10	–	–	55	110	165	
		15	–	–	35	85	125	
	PW_{CL}	5.0	–	–	1200	2400	3600	ns
		10	–	–	475	950	1425	
		15	–	–	300	715	1070	
Maximum Low Clock Pulse Width#	PW_{CL}	5.0	5.0	2.0	10	–	–	ms
		10	1.5	0.9	3.0	–	–	
		15	0.15	0.1	0.3	–	–	
Address Setup Time	t_{setupA}	5.0	0	0	0	–	–	ns
		10	0	0	0	–	–	
		15	0	0	0	–	–	
Address Hold Time	t_{holdA}	5.0	0	0	0	–	–	ns
		10	0	0	0	–	–	
		15	0	0	0	–	–	
Minimum Clock to Enable Setup Time	t_{setupC}	5.0	–	–	1425	2850	4275	ns
		10	–	–	575	1150	1725	
		15	–	–	400	865	1295	
Minimum Clock to Enable Hold Time	t_{holdC}	5.0	–	–	0	100	150	ns
		10	–	–	0	50	75	
		15	–	–	0	40	55	

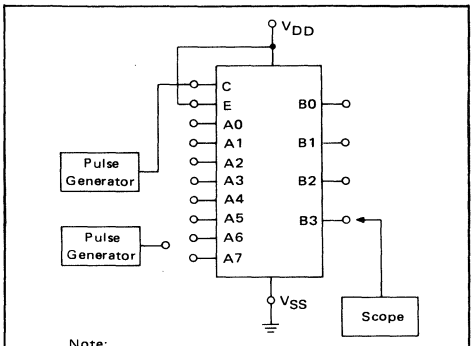
*The clock can remain high indefinitely with the data remaining latched.
#If clock stays low too long, the dynamically stored data will leak off and will have to be recalled.

FIGURE 1 – OUTPUT DRIVE CURRENT TEST CIRCUIT



Notes:
1. Source current, address ROM to obtain a "1" on all four outputs (B0 thru B3).
2. Sink current, address ROM to obtain a "0" on all four outputs (B0 thru B3).

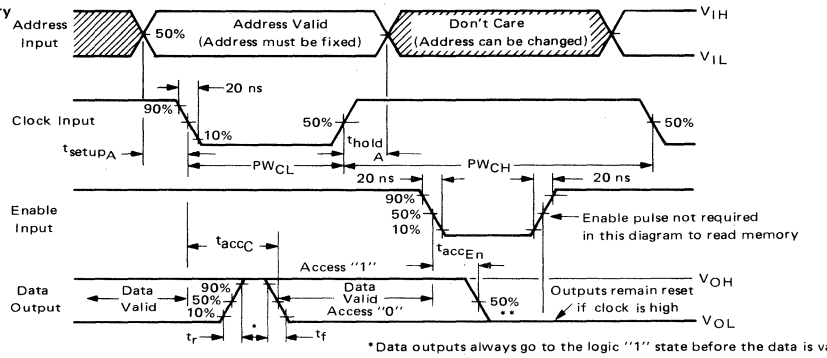
FIGURE 2 – SWITCHING TIME TEST CIRCUIT (Refer to timing diagram)



Note:
Address ROM to obtain level change when clocking any one address line.

MEMORY READ CYCLE TIMING DIAGRAMS

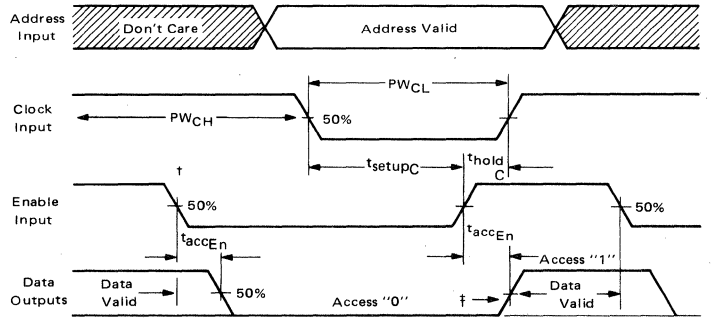
a) Using Clock to Read Memory



*Data outputs always go to the logic "1" state before the data is valid between accessing successive "0's"

**Outputs forced to "0" by Enable.

b) Using the Enable to Read Memory



† In this mode of operation, the negative going edge of Enable should occur on or before the clock negative edge.

‡The data outputs are valid without the logic "1" pulse occurring during the access cycle as shown in a) above.

CUSTOM PROGRAMMING

By the programming of a single photomask for the MCM14524, the customer may specify the content of the memory.

Address Inputs:

Words are numbered 0 through 255 and are addressed using sequential addressing of Address leads A0 through A7 with A0 as the least significant digit.

Logic "0" is defined as a "low" Address input (V_{IL}).
Logic "1" is defined as a "high" Address input (V_{IH}).

WORD \ ADDRESS	A7	A6	A5	A4	A3	A2	A1	A0
Word 0	0	0	0	0	0	0	0	0
Word 1	0	0	0	0	0	0	0	1
Word 2	0	0	0	0	0	0	1	0
Word 3	0	0	0	0	0	0	1	1
. .	.	.	.	.	.	.	.	.
. .	.	.	.	.	.	.	.	.
. .	.	.	.	.	.	.	.	.
Word 255	1	1	1	1	1	1	1	1

Two methods may be used to transmit the custom memory pattern to Motorola.

METHOD A: PUNCHED COMPUTER CARDS

A binary coded decimal equivalent of each desired output may be punched in standard computer cards (four cards are required for all 256 words) in numerical (word number) order. 64 words per card are punched in columns 12 thru 75 using the Binary to Hexadecimal conversion table. Columns 77 and 78 are used to number the cards, which must be in numerical order. Please use characters as shown in the table when punching computer cards.

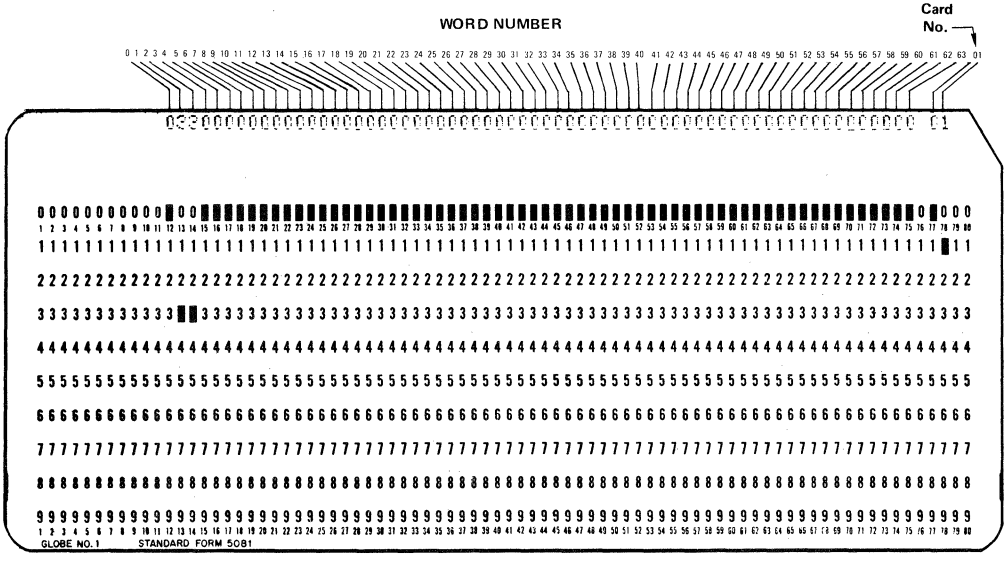
BINARY TO HEXADECIMAL CONVERSION TABLE

BINARY WORD DESIRED	CARD CHARACTER
0 0 0 0	0
0 0 0 1	1
0 0 1 0	2
0 0 1 1	3
0 1 0 0	4
0 1 0 1	5
0 1 1 0	6
0 1 1 1	7
1 0 0 0	8
1 0 0 1	9
1 0 1 0	A
1 0 1 1	B
1 1 0 0	C
1 1 0 1	D
1 1 1 0	E
1 1 1 1	F

ROM SAMPLE WORD PROGRAMMING FOR PUNCHED CARD

WORD NUMBER	ADDRESS INPUTS								SAMPLE WORD OUTPUTS				CARD CHARACTER
	A7	A6	A5	A4	A3	A2	A1	A0	B3	B2	B1	B0	
0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1	0	0	1	1	3
2	0	0	0	0	0	0	1	0	0	0	1	1	3
3	0	0	0	0	0	0	1	1	0	0	0	0	0
.	.	.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.	.	.
255	1	1	1	1	1	1	1	1	1	0	1	0	A

Shown in columns 12 – 15 on card below



METHOD B: TRUTH TABLE

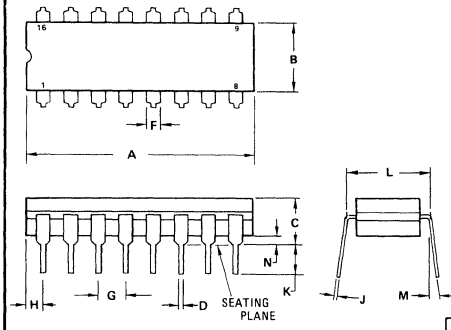
Use of the truth table presents a simple and direct way to input the memory pattern desired to Motorola. When filling out the table please use a "1" for a high, and a "0" for a low.

CUSTOM PROGRAM for the MCM14524 Read Only Memory

	BIT					BIT					BIT					BIT					BIT			
WORD	3	2	1	0	WORD	3	2	1	0	WORD	3	2	1	0	WORD	3	2	1	0	WORD	3	2	1	0
0					51					102					153					204				
1					52					103					154					205				
2					53					104					155					206				
3					54					105					156					207				
4					55					106					157					208				
5					56					107					158					209				
6					57					108					159					210				
7					58					109					160					211				
8					59					110					161					212				
9					60					111					162					213				
10					61					112					163					214				
11					62					113					164					215				
12					63					114					165					216				
13					64					115					166					217				
14					65					116					167					218				
15					66					117					168					219				
16					67					118					169					220				
17					68					119					170					221				
18					69					120					171					222				
19					70					121					172					223				
20					71					122					173					224				
21					72					123					174					225				
22					73					124					175					226				
23					74					125					176					227				
24					75					126					177					228				
25					76					127					178					229				
26					77					128					179					230				
27					78					129					180					231				
28					79					130					181					232				
29					80					131					182					233				
30					81					132					183					234				
31					82					133					184					235				
32					83					134					185					236				
33					84					135					186					237				
34					85					136					187					238				
35					86					137					188					239				
36					87					138					189					240				
37					88					139					190					241				
38					89					140					191					242				
39					90					141					192					243				
40					91					142					193					244				
41					92					143					194					245				
42					93					144					195					246				
43					94					145					196					247				
44					95					146					197					248				
45					96					147					198					249				
46					97					148					199					250				
47					98					149					200					251				
48					99					150					201					252				
49					100					151					202					253				
50					101					152					203					254				
																				255				

PACKAGE DIMENSIONS

L SUFFIX
CERAMIC PACKAGE
CASE 620



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	19.05	19.81	0.750	0.780
B	6.22	6.98	0.245	0.275
C	4.06	5.08	0.160	0.200
D	0.38	0.51	0.015	0.020
F	1.40	1.65	0.055	0.065
G	2.54 BSC		0.100 BSC	
H	0.51	1.14	0.020	0.045
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	7.37	7.87	0.290	0.310
M	–	15^0	–	15^0
N	0.51	1.02	0.020	0.040

CASE 620-02

NOTES:
1 LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION
2 PKG. INDEX: NOTCH IN LEAD
NOTCH IN CERAMIC OR INK DOT
3 DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL

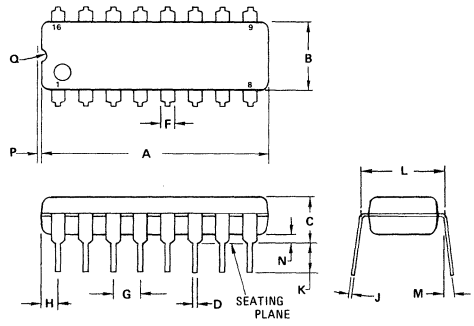
Devices packaged in Case 620 fall within one of the given sets of dimensions. Further identification is available upon request.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	19.05	19.94	0.750	0.785
B	6.10	7.49	0.240	0.295
C	–	5.08	–	0.200
D	0.38	0.53	0.015	0.021
F	1.40	1.78	0.055	0.070
G	2.54 BSC		0.100 BSC	
H	0.51	1.14	0.020	0.045
J	0.20	0.30	0.008	0.012
K	2.54	–	0.100	–
L	7.49	8.89	0.295	0.350
M	–	15^0	–	15^0
N	0.51	1.02	0.020	0.040

CASE 620-04

NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. PKG. INDEX: NOTCH IN LEAD
NOTCH IN CERAMIC OR INK DOT.
3. DIM "A" AND "B" DO NOT INCLUDE GLASS RUN-OUT.
4. DIM "L" TO INSIDE OF LEADS (MEASURED 0.51 mm (0.020) BELOW BODY)

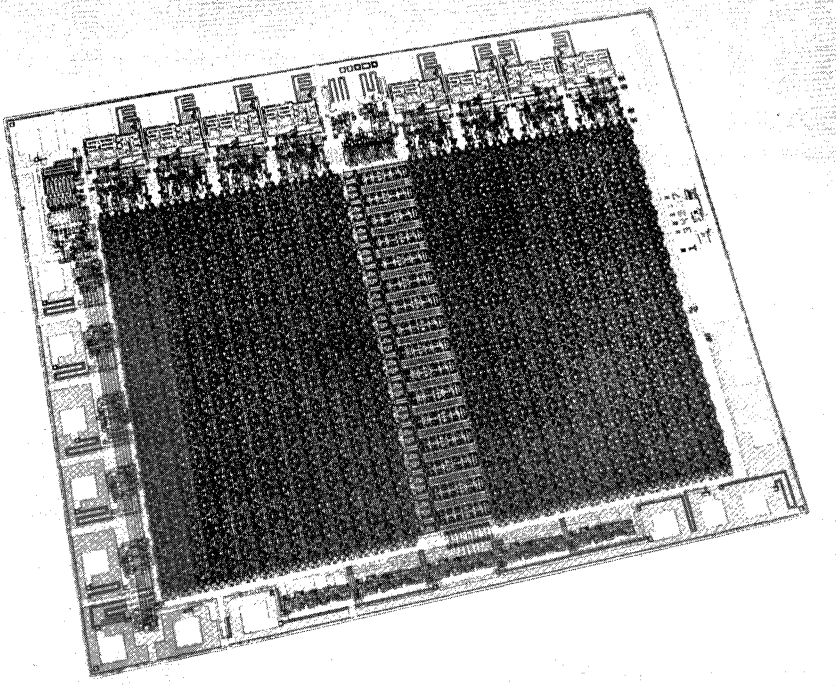
P SUFFIX
PLASTIC PACKAGE
CASE 648



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	20.70	21.34	0.815	0.840
B	6.10	6.60	0.240	0.260
C	4.06	4.57	0.160	0.180
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.32	1.83	0.052	0.072
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.37	7.87	0.290	0.310
M	–	10^0	–	10^0
N	0.51	1.02	0.020	0.040
P	0.13	0.38	0.005	0.015
Q	0.51	0.76	0.020	0.030

CASE 648-03

NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL



M6800 System Memories/Chapter 4

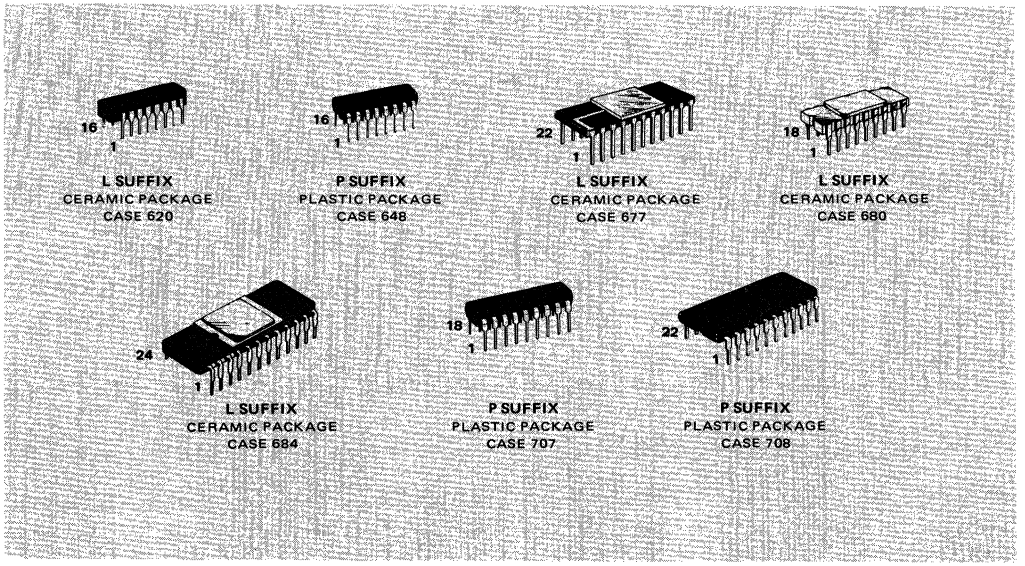
MOS

M6800 SYSTEM MEMORIES

The M6800 family of parts has been designed to set the standard for microcomputer system architecture. Included in this family are a number of Random Access Memories and Read Only Memories to fill the needs of a variety of applications. Both static and dynamic memories are available.

Device No.	No. of Bits	Description	Organization	Access Time (ns max)	Power Supplies (V)	No. of Pins	Case	Page No.
RANDOM ACCESS MEMORIES (Silicon Gate NMOS)								
MCM6810A	1024	Static	128 x 8	500	+5	24	684	4-3
MCM68111A	1024	Static, Common I/O and Output Disable	256 x 4	450	+5	18	680, 707	4-7
MCM68112A	1024	Static, Common I/O	256 x 4	450	+5	16	620, 648	4-11
MCM6815A	4096	Dynamic	4096 x 1	300	+12, +5, −5	22	677, 708	4-15
MCM6815A2	4096	Dynamic	4096 x 1	200	+12, +5, −5	22	677, 708	4-15
READ ONLY MEMORIES (Silicon Gate NMOS unless otherwise noted)								
MCM6830A*	8192	Mask-Programmable	1024 x 8	500	+5	24	684	4-29
MCM68317*#	16384	Mask-Programmable	2048 x 8	500	+5	24	684	4-35
MCM6832*†	16384	Mask-Programmable	2048 x 8	550	+12, +5, −5	24	684	4-37
MCM68708#	8192	Alterable	1024 x 8	500	+12, +5, −5	24	TBA	4-43

*Mask-programmable ROMs are manufactured according to a bit-pattern supplied by the customer. A special device number (SCMxxxx) is assigned to each individual pattern.
#To be announced
†Metal Gate NMOS



MCM6810AL

Advance Information

128 X 8-BIT STATIC RANDOM ACCESS MEMORY

The MCM6810A is a byte-organized memory designed for use in bus-organized systems. It is fabricated with N-channel silicon-gate technology. For ease of use, the device operates from a single power supply, has compatibility with TTL and DTL, and needs no clocks or refreshing because of static operation.

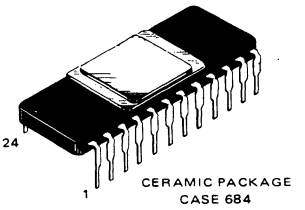
The memory is compatible with the M6800 Microcomputer Family, providing random storage in byte increments. Memory expansion is provided through multiple Chip Select inputs.

- Organized as 128 Bytes of 8 Bits
- Static Operation
- Bi-Directional Three-State Data Input/Output
- Six Chip Select Inputs (Four Active Low, Two Active High)
- Single 5-Volt Power Supply
- TTL Compatible
- Maximum Access Time = 500 ns

MOS

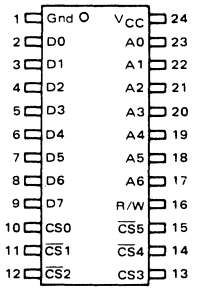
(N-CHANNEL, SILICON-GATE)

128 X 8-BIT STATIC RANDOM ACCESS MEMORY



CERAMIC PACKAGE
CASE 684

PIN ASSIGNMENT

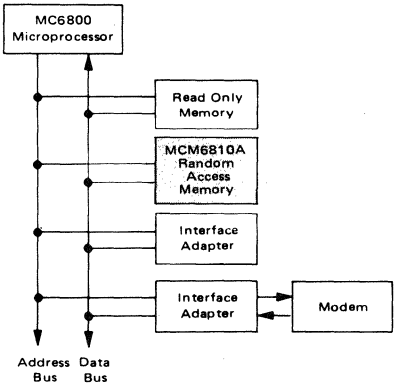


ABSOLUTE MAXIMUM RATINGS (See Note 1)

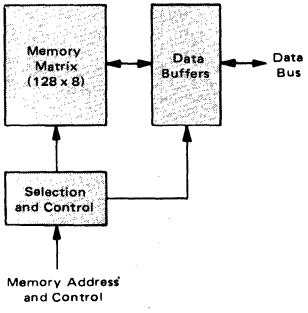
Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.3 to +7.0	Vdc
Input Voltage	V_{in}	-0.3 to +7.0	Vdc
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

NOTE 1: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

M6800 MICROCOMPUTER FAMILY
BLOCK DIAGRAM



MCM6810A RANDOM ACCESS MEMORY
BLOCK DIAGRAM



DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted.)

RECOMMENDED DC OPERATING CONDITIONS

Parameter	Symbol	Min	Nom	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	Vdc
Input High Voltage	V_{IH}	2.0	–	5.25	Vdc
Input Low Voltage	V_{IL}	-0.3	–	0.8	Vdc

DC CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit
Input Current (A_n, R/W, CS_n, $\overline{CS}_n$) (V_{in} = 0 to 5.25 V)	I_{in}	–	–	2.5	μAdc
Output High Voltage (I_{OH} = −205 μA)	V_{OH}	2.4	–	–	Vdc
Output Low Voltage (I_{OL} = 1.6 mA)	V_{OL}	–	–	0.4	Vdc
Output Leakage Current (Three-State) (CS = 0.8 V or $\overline{CS}$ = 2.0 V, V_{out} = 0.4 V to 2.4 V)	I_{LO}	–	–	10	μAdc
Supply Current (V_{CC} = 5.25 V, T_A = 0°C)	I_{CC}	–	–	130	mAdc

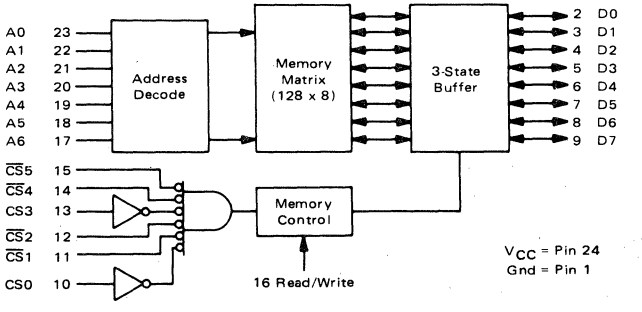
4

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, periodically sampled rather than 100% tested.)

Characteristic	Symbol	Max	Unit
Input Capacitance	C_{in}	7.5	pF
Output Capacitance	C_{out}	12.5	pF

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

BLOCK DIAGRAM



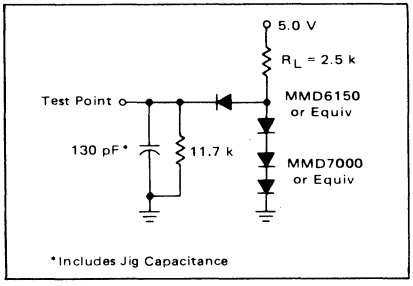
AC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature unless otherwise noted.)

RECOMMENDED AC OPERATING CONDITIONS

Parameter	Symbol	Min	Unit
Address Setup Time	t_{AS}	30	ns
Address Hold Time	t_{AH}	0	ns
Chip Select Pulse Width	t_{CS}	400	ns

FIGURE 1 – AC TEST LOAD

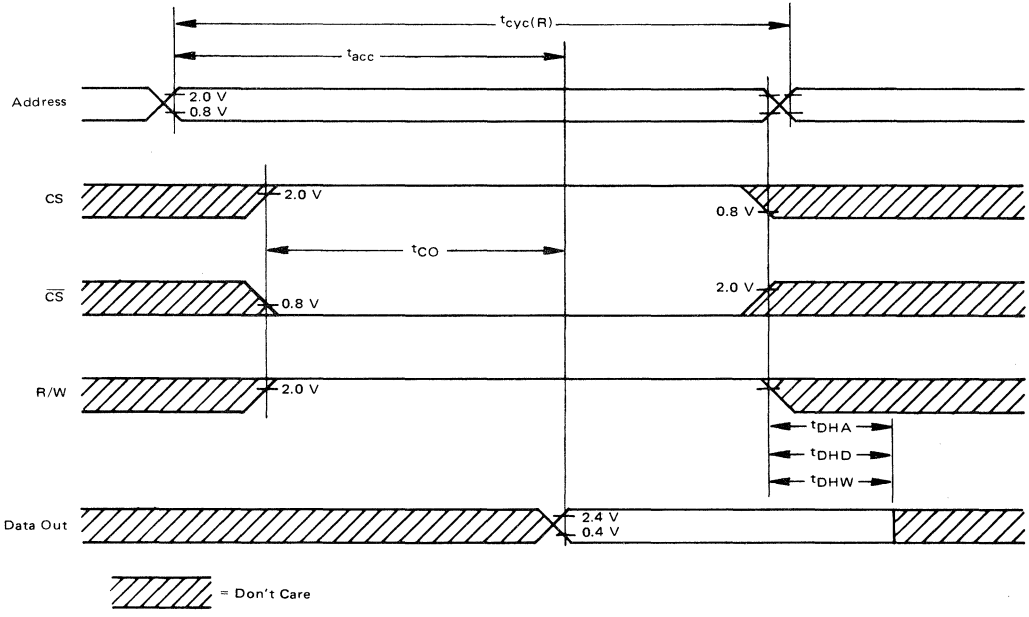


READ CYCLE (All timing with $t_r = t_f = 20$ ns, Load of Figure 1; Input pulse levels = 0.8 V to 2.0 V)

Characteristic	Symbol	Min	Max	Unit
Read Cycle Time	$t_{cyc(R)}$	500	–	ns
Access Time	t_{acc}	–	500	ns
Chip Select to Output Delay	t_{CO}	–	300	ns
Data Hold from Address	t_{DHA}	10	–	ns
Data Hold from Deselection	t_{DHD}	10	150	ns
Data Hold from Write	t_{DHW}	10	–	ns

4

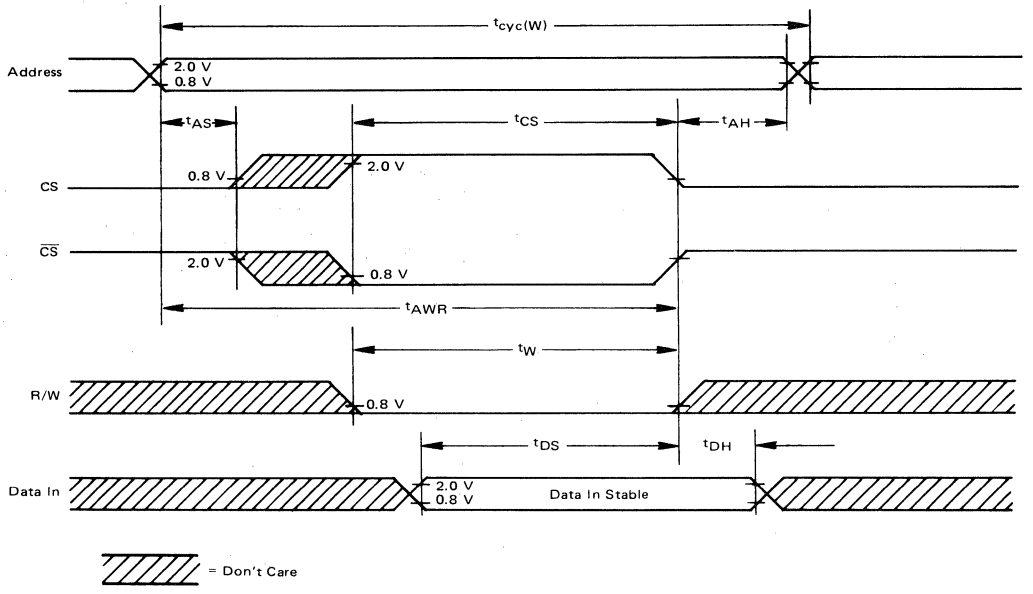
READ CYCLE TIMING



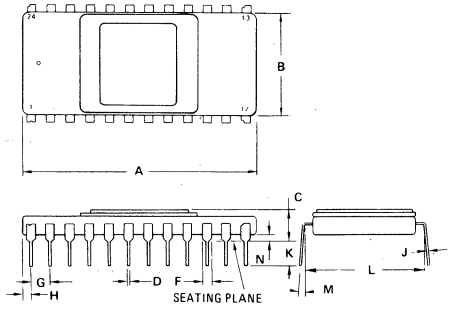
WRITE CYCLE (All timing with $t_r = t_f = 20$ ns, Load of Figure 1; Input pulse levels = 0.8 V to 2.0 V)

Characteristic	Symbol	Min	Max	Unit
Write Cycle Time	$t_{cyc(W)}$	500	–	ns
Write Pulse Width	t_W	400	–	ns
Address to Write Release	t_{AWR}	500	–	ns
Data Setup Time	t_{DS}	225	–	ns
Data Hold Time	t_{DH}	0	–	ns

WRITE CYCLE TIMING



PACKAGE DIMENSIONS



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	29.34	30.86	1.155	1.215
B	12.70	14.22	0.500	0.560
C	3.05	3.94	0.120	0.155
D	0.38	0.51	0.015	0.020
F	0.89	1.40	0.035	0.055
G	2.54 BSC		0.100 BSC	
H	0.89	1.40	0.035	0.055
J	0.20	0.30	0.008	0.012
K	2.92	3.68	0.115	0.145
L	14.86	15.87	0.585	0.625
M	–	15°	–	15°
N	0.51	1.14	0.020	0.045

NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE WITH MAXIMUM MATERIAL CONDITION.
2. LEAD NO. 1 CUT FOR IDENTIFICATION, OR BUMP ON TOP.
3. DIM "L" TO INSIDE OF LEADS. (MEASURED 0.51 mm (0.020) BELOW PKG BASE)

CASE 684-04

MCM68111AL
MCM68111AP

Product Preview

256 x 4-BIT STATIC RANDOM ACCESS MEMORY

The MCM68111A is a 256 x 4-bit static RAM designed for use in bus-organized systems. It is fabricated with high-density, high-reliability, N-channel, silicon-gate, depletion load technology. For ease of use, the device operates from a single power supply, is directly compatible with TTL and DTL, and requires no clocks or refreshing because of static operation.

The memory is compatible with the M6800 Microcomputer Family, providing random storage in 4-bit increments. Memory expansion is provided through two Chip Select inputs.

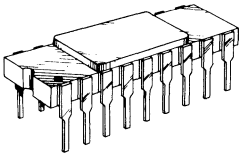
- 1024 Bits Organized as 256 x 4
- Static Operation
- Bi-Directional Three-State Data Input/Output
- Two Chip Select Inputs for Memory Expansion
- Output Disable
- Single 5-Volt Power Supply
- Direct TTL/DTL Compatibility
- Maximum Access Time = 450 ns

MOS

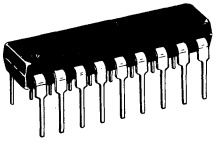
(N-CHANNEL, SILICON-GATE, DEPLETION LOAD)

256 X 4-BIT STATIC RANDOM ACCESS MEMORY

with Common Data Inputs/Outputs and Output Disable



L SUFFIX
CERAMIC PACKAGE
CASE 680



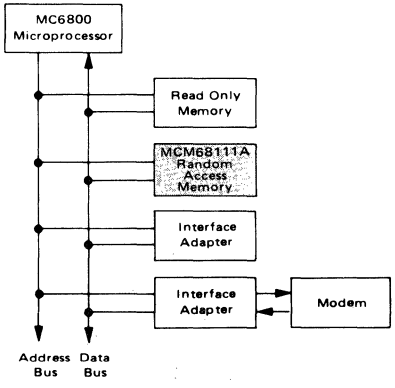
P SUFFIX
PLASTIC PACKAGE
CASE 707

ABSOLUTE MAXIMUM RATINGS (See Note 1; Referenced to V_{SS})

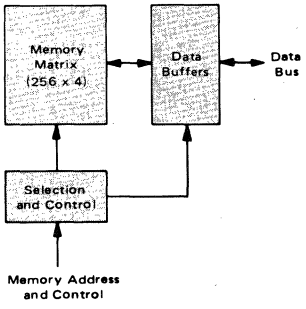
Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.3 to +7.0	Vdc
Input Voltage	V_{in}	-0.3 to +7.0	Vdc
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

NOTE 1: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

M6800 MICROCOMPUTER FAMILY BLOCK DIAGRAM



MCM68111A RANDOM ACCESS MEMORY BLOCK DIAGRAM



This is advance information and specifications are subject to change without notice.

4

DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted.)

RECOMMENDED DC OPERATING CONDITIONS (Referenced to V_{SS}).

Parameter	Symbol	Min	Nom	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	Vdc
Input Low Voltage	V_{IL}	-0.3	–	0.8	Vdc
Input High Voltage	V_{IH}	2.0	–	5.25	Vdc

DC CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to 5.25 V)	I_{in}	–	1.0	2.5	μAdc
Output Leakage Current (Three-State) ($\overline{CS}$ = 2.0 V, V_{out} = 0.4 to 2.4 V)	I_{LO}	–	–	10	μAdc
Output High Voltage (I_{OH} = -205 μA)	V_{OH}	2.4	–	–	Vdc
Output Low Voltage (I_{OL} = 1.6 mA)	V_{OL}	–	–	0.4	Vdc
Power Supply Current (T_A = 0°C, V_{CC} = 5.25 V)	I_{CC}	–	40	70	mAdc

CAPACITANCE (Periodically sampled rather than 100% tested.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input/Output Capacitance ($V_{I/O}$ = 0 V, f = 1.0 MHz, T_A = 25°C)	$C_{I/O}$	–	8.0	12.5	pF
Input Capacitance, Other Inputs (V_{in} = 0 V, f = 1.0 MHz, T_A = 25°C)	C_{in}	–	3.0	7.5	pF

4

AC CHARACTERISTICS

(All timing with $t_r = t_f$ = 20 ns; Load of Figure 1)

READ CYCLE (Input pulse levels = 0.8 V to 2.0 V)

Characteristic	Symbol	Min	Max	Unit
Read Cycle Time	$t_{cyc(R)}$	450	–	ns
Access Time	t_{acc}	–	450	ns
Chip Select to Output Delay	t_{CO}	–	230	ns
Output Enable to Output Delay	t_{OE}	–	230	ns
Data Hold from Address	t_{DHA}	10	–	ns
Data Hold from Disable	t_{DHD}	10	90	ns
Data Hold from Write	t_{DHW}	0	90	ns

WRITE CYCLE (Input pulse levels = 0.8 V to 2.0 V)

Characteristic	Symbol	Min	Max	Unit
Write Cycle Time	$t_{cyc(W)}$	450	–	ns
Chip Select Pulse Width	t_{CS}	300	–	ns
Address Setup Time	t_{AS}	20	–	ns
Address Hold Time	t_{AH}	0	–	ns
Address to Write Release	t_{AWR}	450	–	ns
Write Pulse Width	t_W	300	–	ns
Data Setup Time	t_{DS}	190	–	ns
Data Hold Time	t_{DH}	0	–	ns

FIGURE 1 – AC TEST LOAD

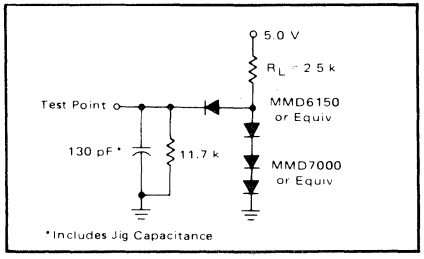


FIGURE 2 – READ CYCLE TIMING

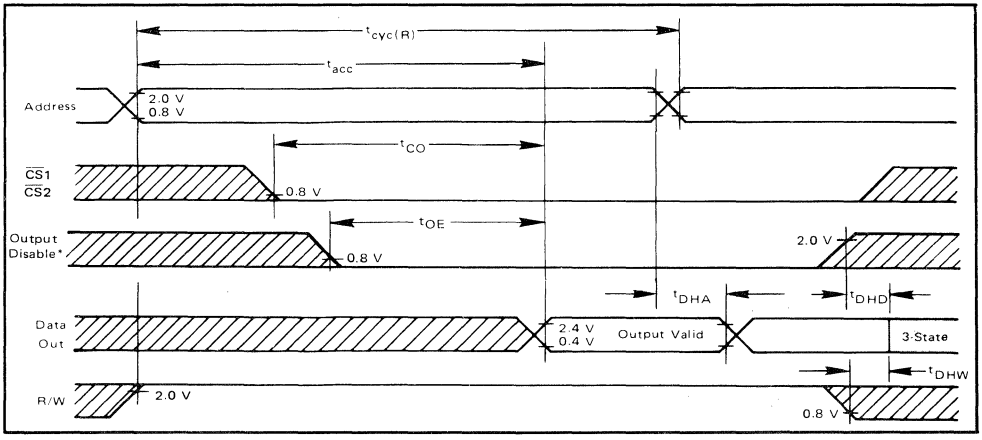
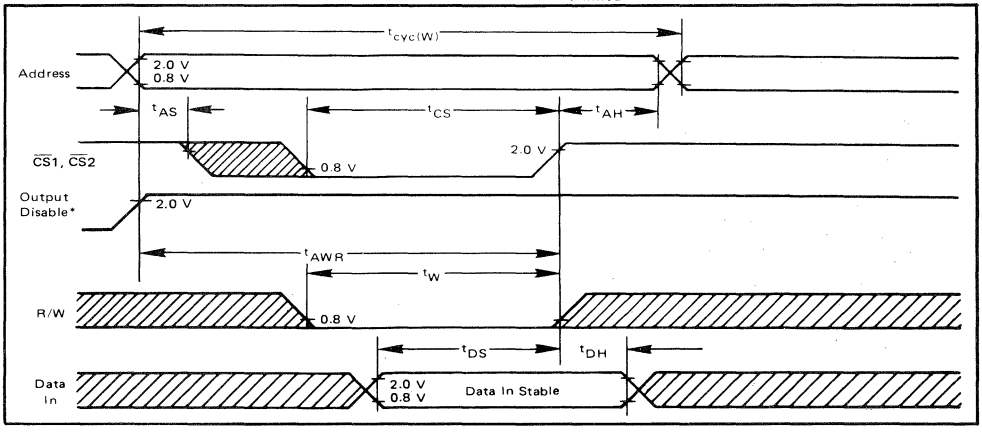


FIGURE 3 – WRITE CYCLE TIMING



= Don't Care

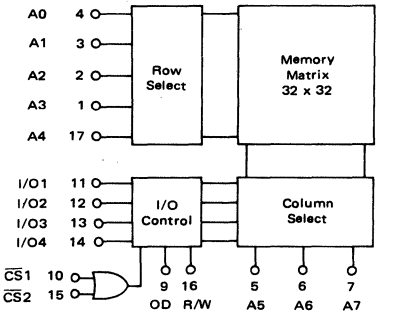
*Output Disable may be hard-wired to V_{SS} and left unused. If this is done, R/W = V_{IL} is used to insure a three-state I/O buffer before valid data input is required for a write cycle. Using the timing shown, 20 ns is allowed between the three-state condition and Data In [$t_W - t_{DS} - (t_{DHW}$ max) = 300 – 190 – 90 = 20 ns]. This time may be extended by widening t_W.

DESCRIPTION OF BUS INTERFACE

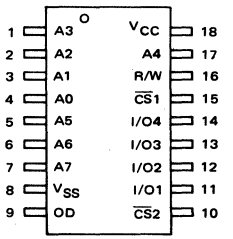
The MCM68111A is compatible with the M6800 bus. The high-impedance address inputs offer low leakage currents and low capacitance. They are readily connected to the address bus. The $\overline{CS}$ inputs, R/W, and Output Disable also offer these advantages.

The MCM68111A uses a three-state I/O buffer, allowing the memory to be connected to the data bus. The I/O buffer will be at a high impedance state when the memory is either deselected ($\overline{CS}$ = V_{IH}), is in the write mode (R/W = V_{IL}), or the output is disabled (OD = V_{IH}). During this time, the I/O ports exhibit low leakage currents and low capacitance. When the memory is selected, outputs enabled, and in the read mode (R/W = V_{IH}), the I/O buffers will actively drive the data bus to its proper levels.

EXPANDED BLOCK DIAGRAM



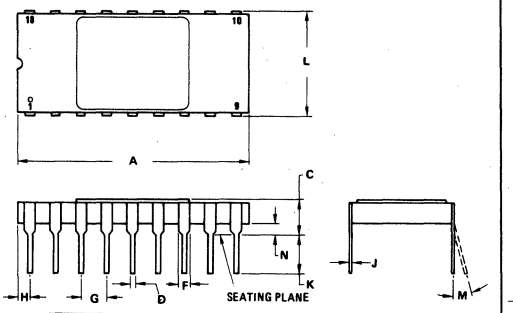
V_{CC} = Pin 18
V_{SS} = Pin 8



PIN ASSIGNMENT

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

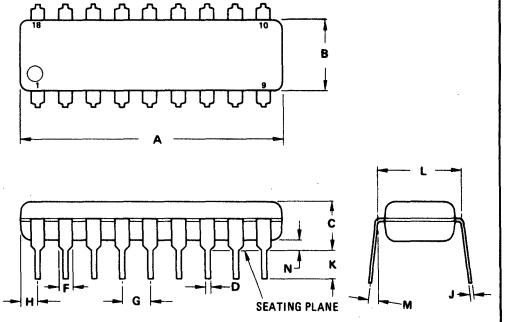
PACKAGE DIMENSIONS



DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	22.61	23.11	0.890	0.910
C	3.18	4.27	0.125	0.168
D	0.43	0.58	0.017	0.023
F	0.89	1.14	0.035	0.045
G	2.54 BSC		0.100 BSC	
H	1.14	1.40	0.045	0.055
J	0.20	0.30	0.008	0.012
K	3.18	4.44	0.125	0.175
L	7.47	7.92	0.294	0.312
M	–	10°	–	10°
N	1.02	1.52	0.040	0.060

NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. NOMINAL DIM FROM CENTER OF LEADS PARALLEL TO DIM "L" IS 7.62 mm (0.300").

CASE 680-04



DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	22.22	23.24	0.875	0.915
B	6.60	7.11	0.260	0.280
C	4.06	4.57	0.160	0.180
D	0.36	0.51	0.014	0.020
F	1.02	1.52	0.040	0.060
G	2.41	2.67	0.095	0.105
H	1.14	1.40	0.045	0.055
J	0.20	0.30	0.008	0.012
K	3.05	3.56	0.120	0.140
L	7.37	7.87	0.290	0.310
M	0°	10°	0°	10°
N	0.51	1.02	0.020	0.040

CASE 707-01

MCM68112AL
MCM68112AP

Product Preview

256 x 4-BIT STATIC RANDOM ACCESS MEMORY

The MCM68112A is a 256 x 4-bit static RAM designed for use in bus-organized systems. It is fabricated with high-density, high-reliability, N-channel, silicon-gate technology. For ease of use, the device operates from a single power supply, is directly compatible with TTL and DTL, and requires no clocks or refreshing because of static operation.

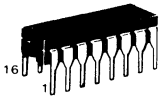
The memory is compatible with the M6800 Microcomputer Family, providing random storage in 4-bit increments. Memory expansion is provided through a Chip Select input.

- 1024 Bits Organized as 256 x 4
- Static Operation
- Bi-Directional Three-State Data Input/Output
- Chip Select Input for Memory Expansion
- Single 5-Volt Power Supply
- Direct TTL/DTL Compatibility
- Maximum Access Time = 450 ns

MOS

(N-CHANNEL, SILICON-GATE)

256 X 4-BIT STATIC RANDOM ACCESS MEMORY



L SUFFIX
CERAMIC PACKAGE
CASE 620

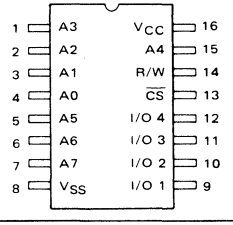
P SUFFIX
PLASTIC PACKAGE
CASE 648

ABSOLUTE MAXIMUM RATINGS (See Note 1; Referenced to V_{SS})

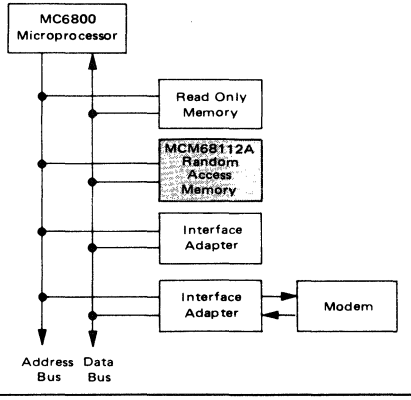
Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.3 to +7.0	Vdc
Input Voltage	V_{in}	-0.3 to +7.0	Vdc
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

NOTE 1: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

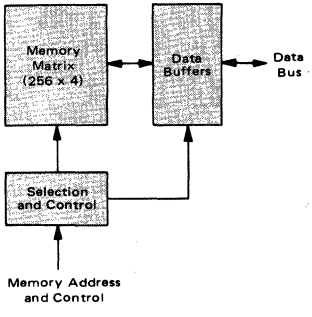
PIN ASSIGNMENT



M6800 MICROCOMPUTER FAMILY BLOCK DIAGRAM



MCM68112A RANDOM ACCESS MEMORY BLOCK DIAGRAM



This is advance information and specifications are subject to change without notice.

DC OPERATING CONDITIONS AND CHARACTERISTICS
(Full operating voltage and temperature range unless otherwise noted.)

RECOMMENDED DC OPERATING CONDITIONS (Referenced to V_{SS}).

Parameter	Symbol	Min	Nom	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	Vdc
Input Low Voltage	V_{IL}	-0.3	–	0.8	Vdc
Input High Voltage	V_{IH}	2.0	–	5.25	Vdc

DC CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit
Input Leakage Current (All Inputs; V_{in} = 0 to 5.25 V)	I_{in}	–	1.0	2.5	μAdc
Output Leakage Current (Three-State) ($\overline{CS}$ = 2.0 V, V_{out} = 0.4 to 2.4 V)	I_{LO}	–	–	10	μAdc
Output High Voltage (I_{OH} = −205 μA)	V_{OH}	2.4	–	–	Vdc
Output Low Voltage (I_{OL} = 1.6 mA)	V_{OL}	–	–	0.4	Vdc
Power Supply Current (T_A = 0°C, V_{CC} = 5.25 V)	I_{CC}	–	40	70	mAdc

CAPACITANCE (Periodically sampled rather than 100% tested.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input/Output Capacitance ($V_{I/O}$ = 0 V, f = 1.0 MHz, T_A = 25°C)	$C_{I/O}$	–	8.0	–	pF
Input Capacitance, Other Inputs (V_{in} = 0.V, f = 1.0 MHz, T_A = 25°C)	C_{in}	–	3.0	–	pF

4

AC CHARACTERISTICS
(All timing with $t_r = t_f$ = 20 ns; Load of Figure 1)

READ CYCLE (Input pulse levels = 0.8 V to 2.0 V)

Characteristic	Symbol	Min	Max	Unit
Read Cycle Time	$t_{cyc(R)}$	450	–	ns
Access Time	t_{acc}	–	450	ns
$\overline{\text{Chip Select}}$ to Output Delay	t_{CO}	–	230	ns
Data Hold from Address	t_{DHA}	10	–	ns
Data Hold from Deselection	t_{DHD}	10	90	ns
Data Hold from Write	t_{DHW}	0	90	ns

WRITE CYCLE (Input pulse levels = 0.8 V to 2.0 V)

Characteristic	Symbol	Min	Max	Unit
Write Cycle Time	$t_{cyc(W)}$	450	–	ns
$\overline{\text{Chip Select}}$ Pulse Width	t_{CS}	300	–	ns
Address Setup Time	t_{AS}	20	–	ns
Address Hold Time	t_{AH}	0	–	ns
Address to Write Release	t_{AWR}	450	–	ns
Write Pulse Width	t_W	300	–	ns
Data Setup Time	t_{DS}	190	–	ns
Data Hold Time	t_{DH}	0	–	ns

FIGURE 1 – AC TEST LOAD

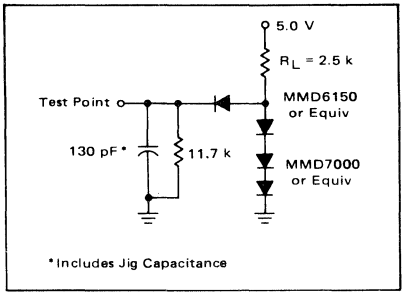


FIGURE 2 – READ CYCLE TIMING

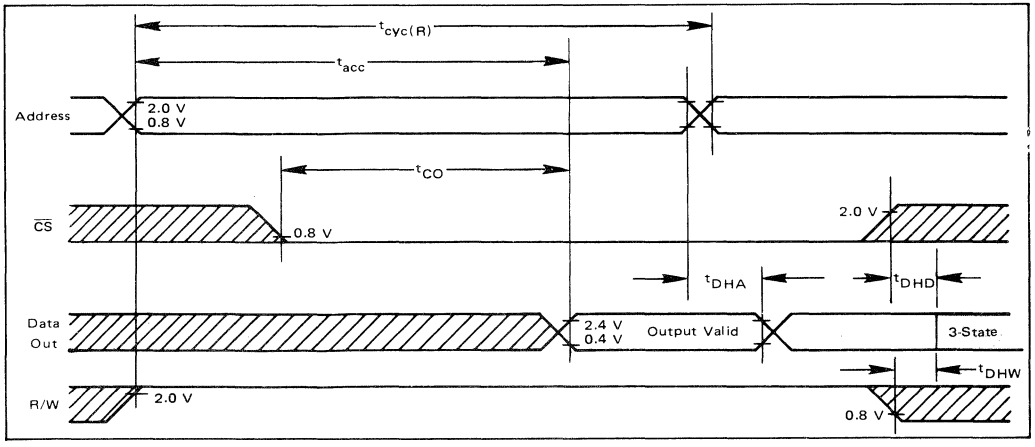
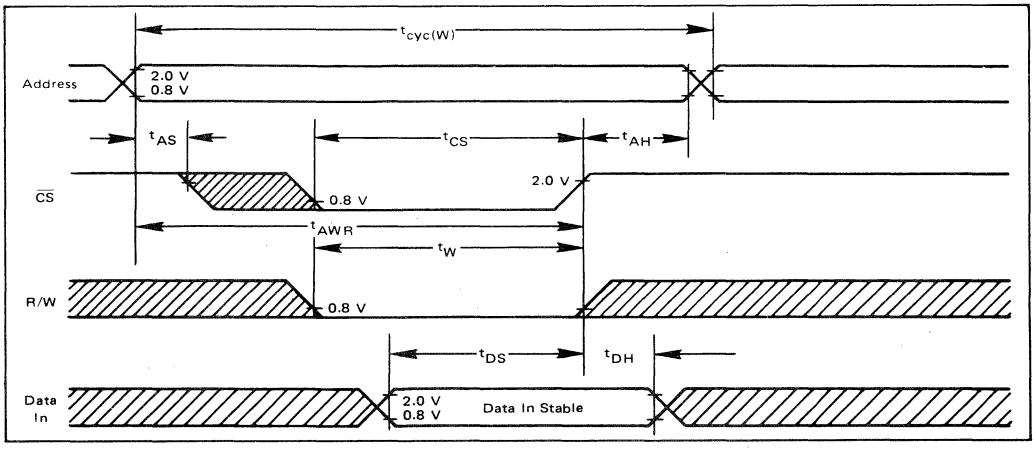


FIGURE 3 – WRITE CYCLE TIMING



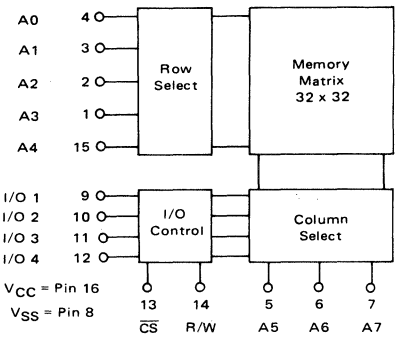
= Don't Care

DESCRIPTION OF BUS INTERFACE

The MCM68112A is compatible with the M6800 bus. The high-impedance address inputs offer low leakage currents and low capacitance. They are readily connected to the address bus. The $\overline{CS}$ and R/W control inputs also offer these advantages.

The MCM68112A uses a three-state I/O buffer, allowing the memory to be connected to the data bus. The I/O buffer will be at a high impedance state when the memory is either deselected ($\overline{CS}$ = V_{IH}) or is in the write mode (R/W = V_{IL}). During this time, the I/O ports exhibit low leakage currents and low capacitance. When the memory is both selected and in the read mode (R/W = V_{IH}), the I/O buffers will actively drive the data bus to its proper levels.

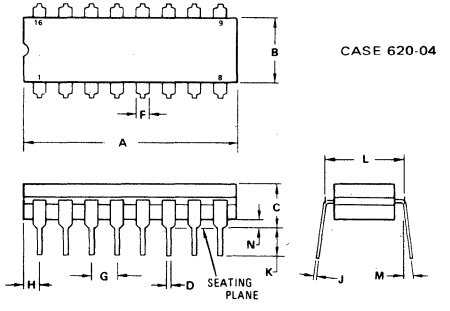
EXPANDED BLOCK DIAGRAM



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

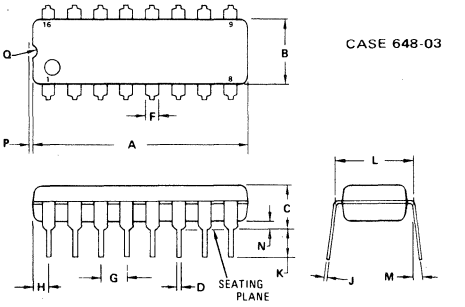
4

PACKAGE DIMENSIONS



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	19.05	19.94	0.750	0.785
B	6.10	7.49	0.240	0.295
C	–	5.08	–	0.200
D	0.38	0.53	0.015	0.021
F	1.40	1.78	0.055	0.070
G	2.54 BSC		0.100 BSC	
H	0.51	1.14	0.020	0.045
J	0.20	0.30	0.008	0.012
K	2.54	–	0.100	–
L	7.49	8.89	0.295	0.350
M	–	15°	–	15°
N	0.51	1.02	0.020	0.040

NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. PKG. INDEX: NOTCH IN LEAD NOTCH IN CERAMIC OR INK DOT.
3. DIM "A" AND "B" DO NOT INCLUDE GLASS RUN-OUT.
4. DIM "L" TO INSIDE OF LEADS (MEASURED 0.51 mm (0.020) BELOW BODY)



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	20.70	21.34	0.815	0.840
B	6.10	6.60	0.240	0.260
C	4.06	4.57	0.160	0.180
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.32	1.83	0.052	0.072
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.37	7.87	0.290	0.310
M	–	10°	–	10°
N	0.51	1.02	0.020	0.040
P	0.13	0.38	0.005	0.015
Q	0.51	0.76	0.020	0.030

NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL

MCM6815A L/L2
MCM6815A P/P2

Advance Information

4096-BIT DYNAMIC RANDOM ACCESS MEMORY

The MCM6815A is a 4096 x 1-bit dynamic RAM designed for use in bus-organized systems. It is fabricated with a high-density, highly-reliable, N-channel, silicon-gate technology. Except for the high-level Chip Enable clock, all inputs are TTL compatible. The output is three-state TTL compatible.

Refresh of the entire memory can be accomplished by sequentially cycling through addresses A0-A4 (32 cycles) a maximum of every 2.0 ms at 70°C ambient temperature. For standby operation, considerable power can be saved by refreshing every 10 ms at 50°C ambient temperature. In addition, widened power supply tolerances are allowed during standby.

The MCM6815A is an ideal Random Access Memory for the M6800 Microcomputer Family, operating well within the timing requirements of the system. Memory expansion is provided for through a Chip Select input.

- Organized as 4096 Words of 1 Bit

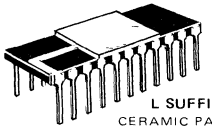
	L2, P2	L, P
• Maximum Access Time =	200 ns	300 ns
• Minimum Read Cycle Time =	360 ns	470 ns
• Minimum Write Cycle Time =	490 ns	590 ns
• Minimum Read-Modify-Write Cycle Time =	490 ns	590 ns

- Low Power Dissipation
  - 335 mW Typical (Active)
  - 550 μW Typical (Standby with Refresh at 50°C)
- Easy Refresh – Only 32 Cycles Every 2.0 ms at 70°C or Every 10 ms During System Standby at 50°C
- TTL Compatible
- 3-State Output
- Address Latches On Chip
- Power Supply Pins on Package Corners for Layout Simplification
- Typical Applications:
  - Main Memory
  - Buffer Memory
  - Peripheral Storage
  - Non-Volatile Memory System

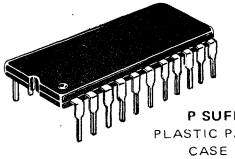
MOS

(N-CHANNEL, SILICON-GATE)

4096-BIT DYNAMIC RANDOM ACCESS MEMORY



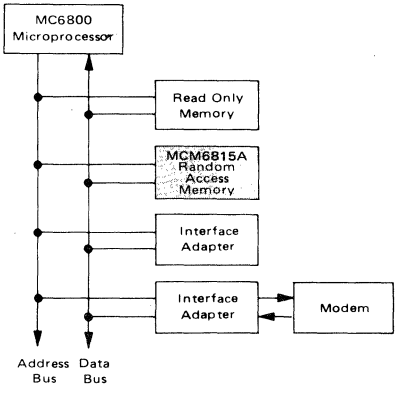
L SUFFIX
CERAMIC PACKAGE
CASE 677



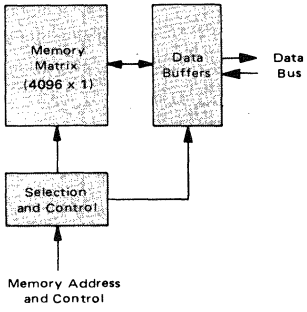
P SUFFIX
PLASTIC PACKAGE
CASE 708

4

M6800 MICROCOMPUTER FAMILY
BLOCK DIAGRAM



MCM6815A RANDOM ACCESS MEMORY
BLOCK DIAGRAM



This is advance information and specifications are subject to change without notice.

ABSOLUTE MAXIMUM RATINGS (See Note 1)

Rating	Symbol	Value	Unit
Voltage on Any Pin Relative to V_{BB}	V_{in}, V_{out}	-0.3 to +20	Vdc
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

NOTE 1: This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted.)

RECOMMENDED DC OPERATING CONDITIONS (Referenced to V_{SS}).

Parameter	Symbol	Min	Nom	Max	Unit
Supply Voltage	V_{DD}	11.4	12	12.6	Vdc
	V_{CC}	4.5	5.0	5.5	Vdc
	V_{SS}	0	0	0	Vdc
	V_{BB}	-5.25	-5.0	-4.75	Vdc
Logic Levels Input High Voltage (A_n, D_{in}, R/W, $\overline{CS}$)	V_{IH}	3.0	–	V_{DD} + 1.0	Vdc
Input Low Voltage (A_n, D_{in}, R/W, $\overline{CS}$)	V_{IL}	-1.0	–	0.8	Vdc
Chip Enable High Voltage	V_{CEH}	V_{DD} -1.0	–	V_{DD} + 1.0	Vdc
Chip Enable Low Voltage	V_{CEL}	-1.0	–	0.8	Vdc

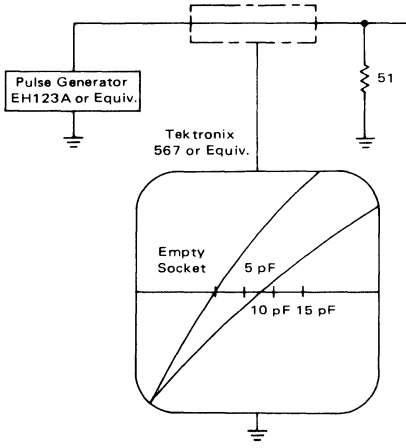
DC CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit
Input Current (A_n, D_{in}, R/W, $\overline{CS}$, Preset) (V_{in} = 0 to V_{DD} + 1.0 V)	I_{in}	–	–	10	μA
Input Chip Enable Current (V_{in} = 0 to V_{DD} + 1.0 V)	I_{ICE}	–	–	10	μA
Output High Voltage (I_O = -100 μA)	V_{OH}	2.4	–	V_{CC}	Vdc
Output Low Voltage (I_O = 2.0 mA)	V_{OL}	V_{SS}	–	0.45	Vdc
Output Leakage Current (V_O = 0.45 V to V_{CC}, CE = V_{CEL}, or $\overline{CS}$ = V_{IH})	I_{LO}	–	–	10	μA
Average Supply Current, Active Mode ($T_{cyc(W)}$ = min)	I_{DDA}	–	28	36	mA
	I_{CCA}	–	0.05	1.0	mA
	I_{BBA}	–	–	100	μA
Supply Current, Standby Mode (CE = V_{CEL})	I_{DDS}	–	1.0	20	μA
	I_{CCS}	–	–	10	μA
	I_{BBS}	–	1.0	20	μA

EFFECTIVE CAPACITANCE (Test Circuit of Figure 1, full operating voltage and temperature range, periodically sampled rather than 100% tested.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Capacitance (A_n, D_{in}, R/W, $\overline{CS}$, Preset)	$C_{in(EFF)}$	–	4.0	5.0	pF
Chip Enable Capacitance	$C_{CE(EFF)}$	–	25	30	pF
Output Capacitance	$C_{out(EFF)}$	–	4.0	5.0	pF

FIGURE 1 – MEASUREMENT OF EFFECTIVE CAPACITANCE



Effective capacitance is determined by comparing the rise time of the voltage waveform at a particular pin to that measured with known values of capacitance. Scope calibration points are determined by using the rise times obtained with the empty socket and standard capacitor values as references.

The device under test (DUT) is inserted into the test socket and normal operating power supplies applied. All input pins, except that being measured, are grounded. The effective capacitance of the desired pin can then be read directly from the scope.

Pin	R	Input Pulse	Measurement Level
CE	67 Ω	16 V	12 V
Input/Output	100 Ω	6.0 V	4.0 V

RECOMMENDED OPERATING CONDITIONS FOR STANDBY WITH REFRESH

(Refresh cycles only, all other parameters unchanged.)

Parameter	Symbol	Min	Nom	Max	Unit
Supply Voltage	V_{DD}	10.8	12.0	13.2	Vdc
	V_{CC}		Not Required		–
	V_{BB}	-5.5	-5.0	-4.5	Vdc
Time Between Refresh (T_A = 50°C)	t_{REF}	–	–	10	ms

AC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature unless otherwise noted.)

OPERATING MODES

Mode	Control States		Output
	R/W	$\overline{CS}$	
Active (CE = High)			
Read Only	H	L	Valid
Read/Write	H → L	L	Valid
Write Only	L	L	Valid
Read Refresh	H → L	L → H	Valid → Floating
Refresh Only	L	H	Floating
Chip Disable (Unselected)	H	H	Floating
Standby (CE = Low)	X	X	Floating

X = Don't Care

RECOMMENDED AC OPERATING CONDITIONS (Read, Write, and Read Modify Write Cycles)

Parameter	Symbol	Min	Max	Unit
Address Setup Time	t_{AS}	0	–	ns
Address Hold Time	t_{AH}	60	–	ns
CE Pulse Transition Time	t_T	–	100	ns
CE Off Time	t_{SB}	120	–	ns
Chip Select Delay Time	t_{CSD}	–	70	ns
Chip Select Hold Time	t_{CSH}	0	–	ns
Read Write Delay Time	t_{RWD}	–	70	ns
Read Write Hold Time	t_{RWH}	0	–	ns
Time Between Refresh	t_{REF}	–	2.0	ms

AC CHARACTERISTICS

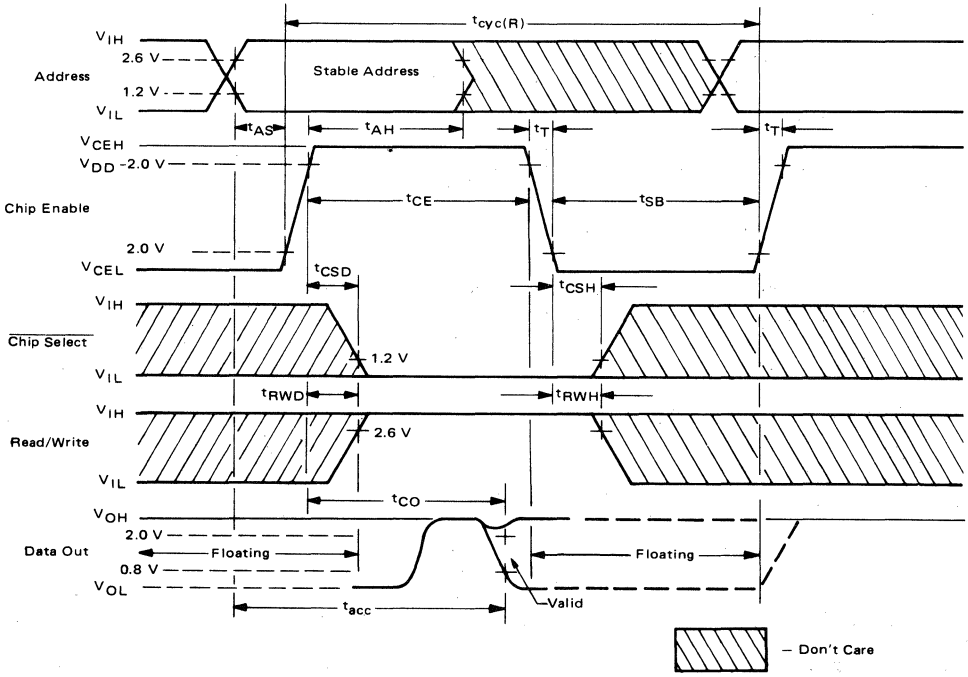
[All timing with t_T = 20 ns; Load = 1 TTL Gate (MC74H00 Series), C_L = 50 pF (effective)]

READ CYCLE (R/W = V_{IH}, $\overline{CS}$ = V_{IL})

Characteristic	Symbol	MCM6815AL,P		MCM6815AL2,P2		Unit
		Min	Max	Min	Max	
Read Cycle Time	$t_{cyc(R)}$	470	–	360	–	ns
Chip Enable On Time	t_{CE}	310	2000	200	2000	ns
Chip Enable to Output Delay	t_{CO}	–	280	–	180	ns
Read Access Time	t_{acc}	–	300	–	200	ns

4

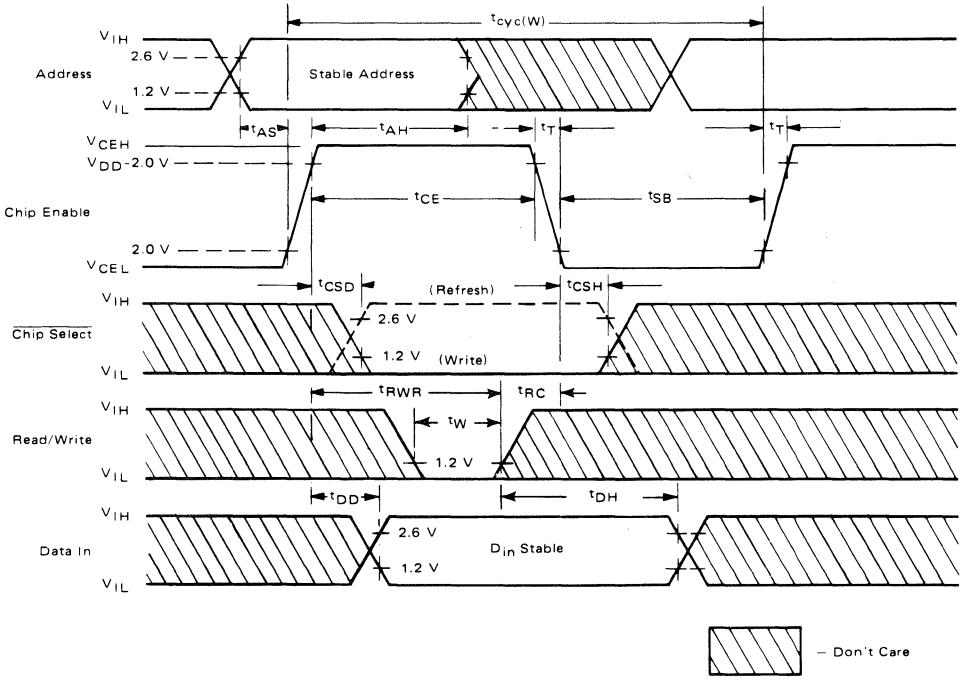
READ CYCLE TIMING



WRITE CYCLE (R/W = V_{IL}, $\overline{CS}$ = V_{IL})
REFRESH CYCLE (R/W = V_{IL}, $\overline{CS}$ = V_{IH})

Characteristic	Symbol	MCM6815AL,P		MCM6815AL2,P2		Unit
		Min	Max	Min	Max	
Write Cycle Time	$t_{cyc(W)}$	590	–	490	–	ns
Chip Enable On Time	t_{CE}	430	2000	330	2000	ns
Read-Write Release Time	t_{RWR}	430	2000	330	2000	ns
Write Pulse Width	t_W	210	–	160	–	ns
Read-Write to Chip Enable Separation Time	t_{RC}	0	–	0	–	ns
Data Delay Time	t_{DD}	–	70	–	70	ns
Data Hold Time	t_{DH}	50	–	50	–	ns

WRITE AND REFRESH CYCLE TIMING

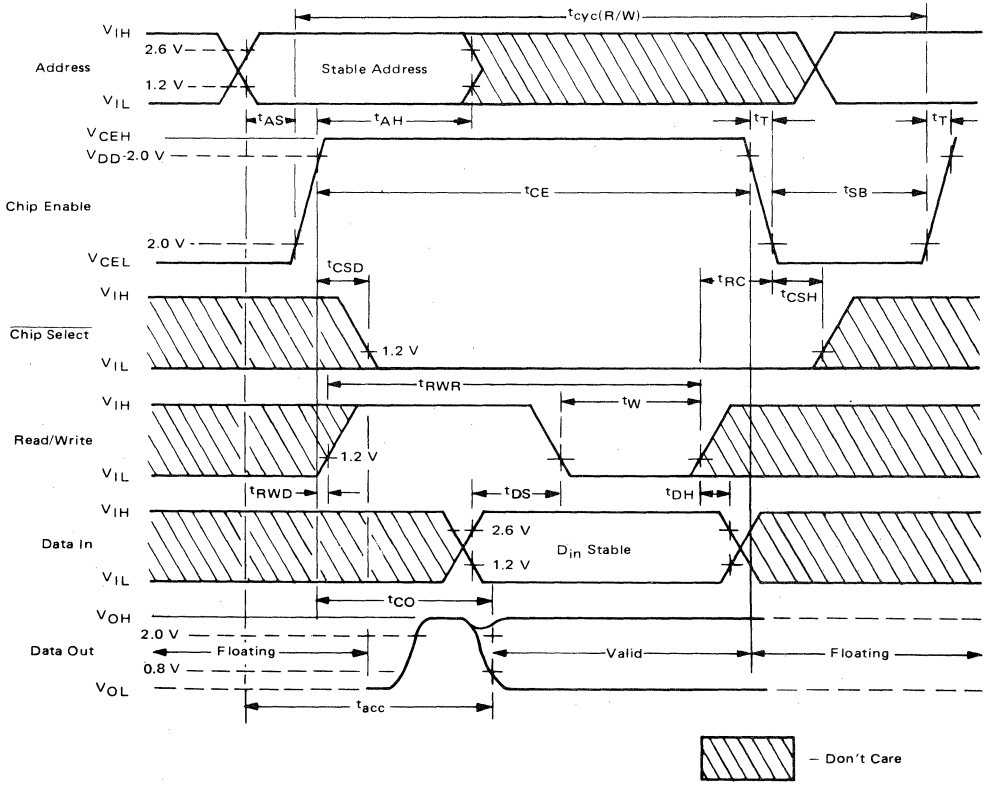


READ-MODIFY-WRITE (R/W = $V_{IH} \rightarrow V_{IL}$, $\overline{CS} = V_{IL}$)
READ REFRESH (See Note 1)

Characteristic	Symbol	MCM6815AL,P Min	MCM6815AL,P Max	MCM6815AL2,P2 Min	MCM6815AL2,P2 Max	Unit
Read-Modify-Write Cycle Time	$t_{cyc(R/W)}$	590	–	490	–	ns
Chip Enable On Time	t_{CE}	430	2000	330	2000	ns
Read-Write Release Time	t_{RWR}	430	2000	330	2000	ns
Write Pulse Width	t_W	210	–	160	–	ns
Data Setup Time	t_{DS}	0	–	0	–	ns
Data Hold Time	t_{DH}	50	–	50	–	ns
Read-Write to Chip Enable Separation Time	t_{RC}	0	–	0	–	ns
Chip Enable to Output Delay	t_{CO}	–	280	–	180	ns
Read Access Time	t_{acc}	–	300	–	200	ns

Note 1: A read refresh cycle is possible by bringing $\overline{CS}$ high after output data is valid and then bringing R/W low to the write position.

READ MODIFY WRITE TIMING



TYPICAL CHARACTERISTICS CURVES

FIGURE 2 – ACCESS TIME versus V_{DD}

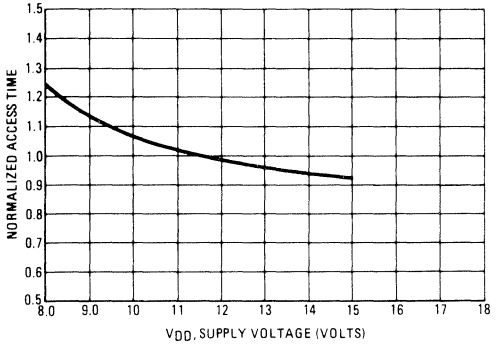


FIGURE 3 – ACCESS TIME versus AMBIENT TEMPERATURE

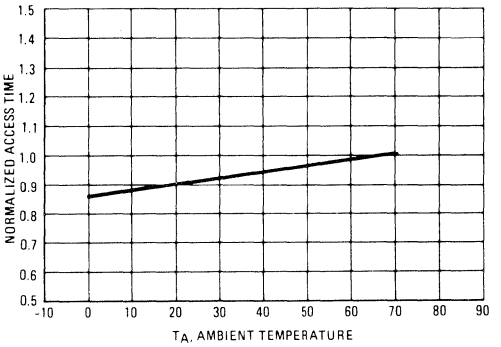


FIGURE 4 – I_{DD} SUPPLY CURRENT versus V_{DD}

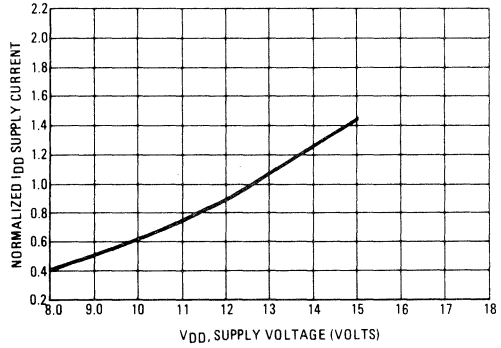


FIGURE 5 – I_{DD} SUPPLY CURRENT versus CYCLE TIME

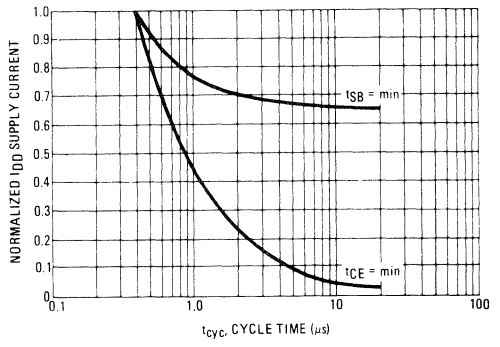


FIGURE 6 – I_{DD} SUPPLY CURRENT versus AMBIENT TEMPERATURE

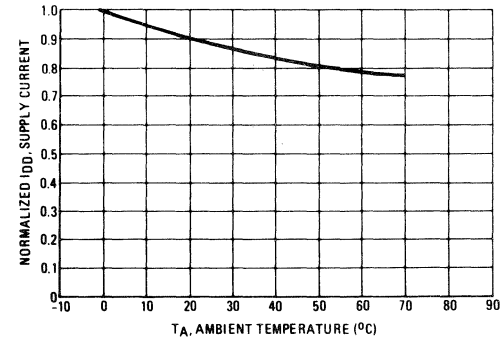
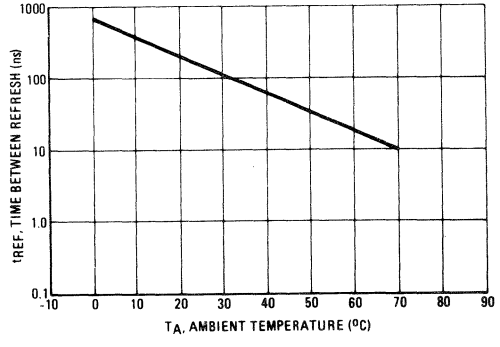


FIGURE 7 – REFRESH TIME versus AMBIENT TEMPERATURE



TYPICAL SUPPLY CURRENT TRANSIENT WAVEFORMS

FIGURE 8 – CHIP ENABLE VOLTAGE

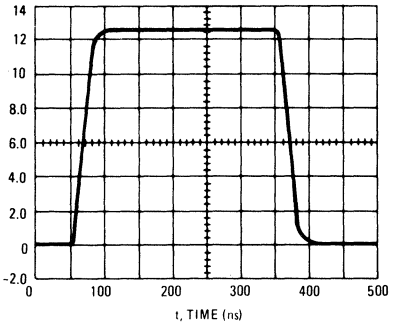


FIGURE 9 – i_{DD} SUPPLY CURRENT

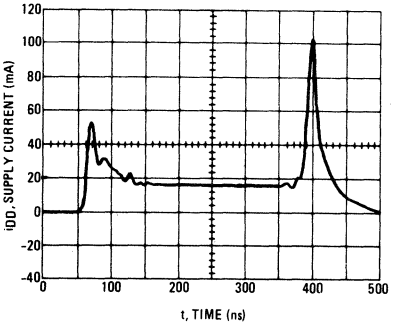


FIGURE 10 – i_{CC} SUPPLY CURRENT

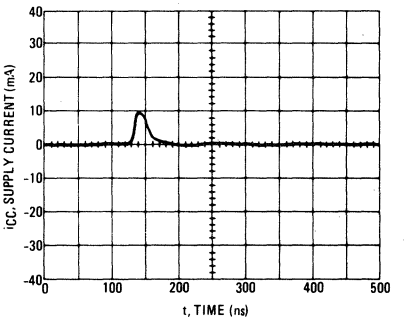


FIGURE 11 – i_{BB} SUPPLY CURRENT

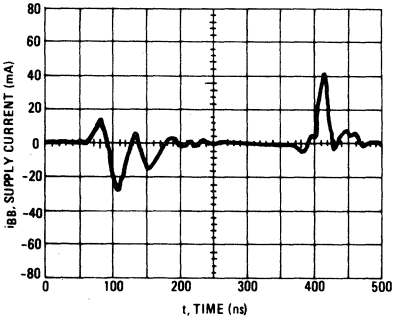
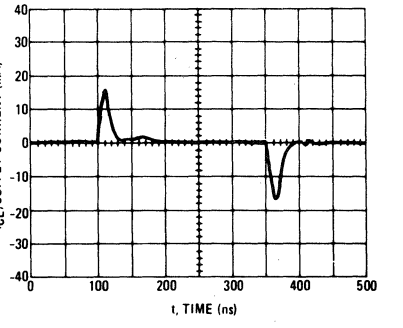
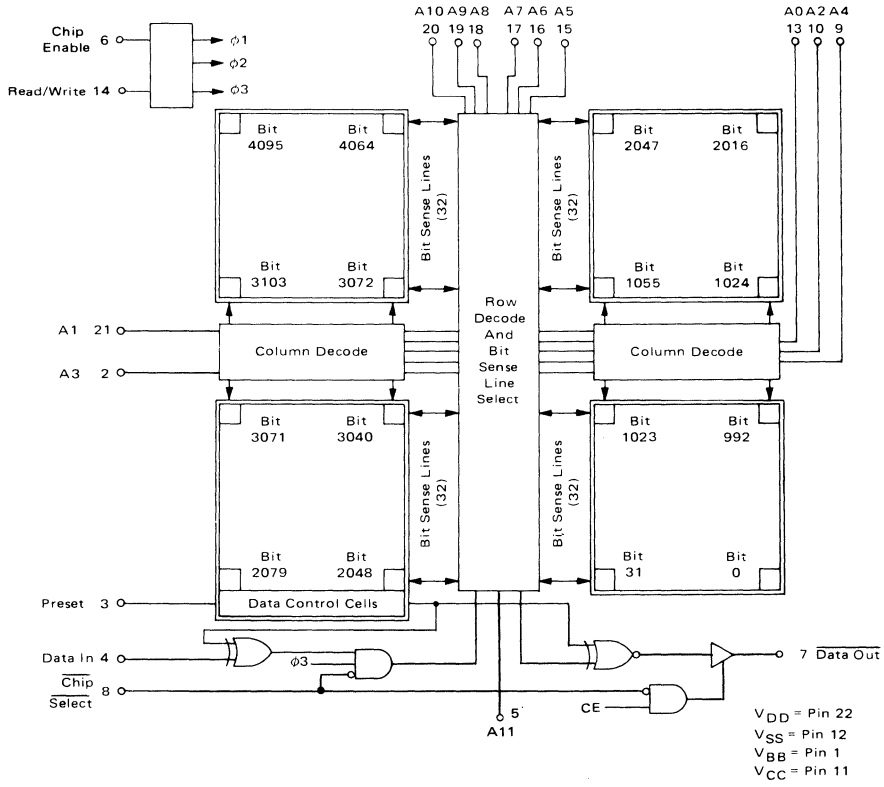


FIGURE 12 – i_{CE} SUPPLY CURRENT



BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

The MCM6815A 4096-bit dynamic RAM uses a three transistor storage cell in an inverting cell configuration. The single high-level clock (Chip Enable) starts an internal three-phase clock generator which controls the read and write functions of the device. The $\phi 1$ signal, which is high when CE is low (standby mode), preconditions the nodes in the dynamic RAM in preparation for a memory cycle. The $\phi 2$ signal, which comes on as CE goes high, is the read control and transfers data from storage onto bit sense lines. The $\phi 3$ signal, which comes after $\phi 2$ only during a write or refresh cycle, transfers data from the bit sense lines back into storage. The $\phi 3$ signal occurs only if the R/W input is low.

To perform a read cycle, CE is brought high to initiate a $\phi 2$ signal and latch the input addresses. The column decoders select one column in each of the four storage quadrants (see the block diagram) and transfers data from storage onto the 128 bit sense lines. The row decoder selects one of these 128 bit sense lines for read and write operations. During the $\phi 2$ signal, the data on this selected bit sense line is Exclusive ORed with the state of the appropriate data control cell to supply the correct output data. After this data is received by the external system, CE may be brought low to the standby position. This assumes that the R/W signal is held high to prevent an internal $\phi 3$ being generated.

To perform a write or refresh operation, CE is brought high and everything is identical to a read operation up until the 128 bit sense lines are charged with the selected columns of stored data. When R/W is brought low (if it is not already there), a $\phi 3$ signal is generated after $\phi 2$ is over. The $\phi 3$ signal takes the data from the 128 bit sense lines and returns it to the 128 storage locations it came from. Because of the design of the memory array, this $\phi 2$-$\phi 3$, read-write operation inverts the data. Therefore, one extra row of memory cells, called data control cells, is used to

keep track of the polarity of stored data in order to be able to correctly recover it. During the write operation, the input data is Exclusive ORed with these control cells before being stored in the array. A refresh cycle does not modify any of the bit sense lines, but simply returns the data (now inverted) into storage.

All timing signals for the MCM6815A are specified around these operations. The following is a brief description of the input pins and relevant timing requirements.

Chip Enable – CE is a single high level clock which initiates all memory cycles. CE can remain low as long as desired for specific applications as long as the 2.0 ms refresh requirements are met.

Chip Select – This signal controls only the I/O buffers. When $\overline{CS}$ is high, the input is disconnected and the output is in the 3-state high-impedance state. A refresh cycle is, therefore, a write cycle with $\overline{CS}$ high. $\overline{CS}$ has no critical timing with respect to any other signal except that there is a finite delay between activation and data out.

Read/Write – When high, R/W inhibits the internal $\phi 3$ signal, thereby keeping the memory from writing. When R/W is low, a $\phi 3$ will occur soon after $\phi 2$ is finished. For a read cycle, R/W should be high within t_{RWD} of CE to insure that a $\phi 3$ does not start. The only timing requirement on the R/W input for writing is a minimum write pulse defined as the overlap of $\overline{CS}$, CE, and R/W. Refresh cycles require that $\overline{CS}$ be high to inhibit the input buffer before a $\phi 3$ occurs. Thus $\overline{CS}$ should be high within t_{CSD} for a refresh cycle, or before R/W goes low for a read-refresh cycle.

Data In – The input data must be valid for a sufficient time to override the data stored on the selected bit sense line. It must remain valid for the "write pulse" defined under Read/Write. Signals on the D_{in} pin are ignored when either $\overline{CS}$ or R/W is high, or CE is low.

Data Out – Output data is inverted from input data and is valid t_{acc} after CE goes high. The data will remain valid as long as CE is high and $\overline{CS}$ remains low. With either CE low or $\overline{CS}$ high, the output is in a high-impedance state. The data output is initially precharged high when CE goes high and is then either discharged to ground or left high depending on the stored data. This precharging followed by valid data occurs regardless of the state of the R/W input, making the write cycle actually a read-write cycle. The output will also try to precharge during a refresh cycle but will be kept at high impedance by the $\overline{CS}$ being high. If $\overline{CS}$ is originally low and is then brought high (within the t_{CSD} specification) the output may start to precharge before being cut off and returned to high impedance.

Addresses – The addresses are latched when CE goes high, and may be removed after an appropriate hold time.

V_{SS} – Circuit ground.

V_{BB} – The reverse bias substrate supply. Forward biasing this supply with respect to V_{SS} will destroy the memory device.

V_{DD} – Positive supply voltage.

V_{CC} – Output buffer supply. This supply goes only to the data output buffer and draws current only when driving an output load high.

Preset – This pin should be tied to ground. During device testing Preset can be used to preset the data control cells to a logic zero. One 200 ns, 12 V pulse will set all 32 cells simultaneously. Preset has no system use; its only purpose is to ensure a good logic level in the control cells after first power up. In system use, this good logic level will come naturally after the first few refresh cycles.

APPLICATIONS INFORMATION

Power Supplies

The MCM6815A is a dynamic RAM which has essentially zero power drain when in the standby (CE low) mode. When operating, the V_{DD} supply may experience transients in the order of 100 mA for a short time (Figure 9). The V_{BB} supply, which has very low dc drain while operating, may see transients of about 40 mA during the edges of CE. Therefore, appropriate bypassing of both supplies is recommended. This bypassing has been simplified by the location of the power supply pins on the corners of the package.

The V_{CC} line supplies only the input leakage of a TTL load on Data Out and should never exceed about 100 μA, presenting little bypassing requirement.

Power dissipation for a system of N chips is much lower than N times the 335 mW typical dissipation for a full speed operating chip. This is because the unselected rows in a memory array card are operating in the standby mode of near zero dissipation. This zero standby power is actually unachievable because of the requirements for refresh. Therefore, power dissipation for an array of N X M chips operating at t_1 cycle time, t_{REF} refresh increment, and maximum CE down time between cycles is:

$$P_D \approx M\left(\frac{490\,ns}{t_1\,ns}\right)335\,mW + (N-1)\,(M)\left(\frac{15.7}{t_{REF}\,\mu s}\right)335\,mW$$

For a 550-ns-cycle-time, 64 k by 16 system (16 by 16 chip array) with refresh at 2.0 ms, the approximate power dissipation is:

$$P_D \approx 16\left(\frac{490}{550}\right)335 + (15)\,(16)\left(\frac{15.7}{2000}\right)335$$

$$\approx 4775\,mW + 630\,mW = 5.4\,W$$

A similar one megabyte system, eight bytes wide, would have a dissipation of only 24 W. If the low standby power capability were not used, over 600 W would be dissipated.

Refresh

The MCM6815A is refreshed by performing a refresh (or write) cycle on each of the 32 combinations of the least significant address bits (A0-A4) within a 2.0 ms time period. (A5-A11 must remain constant at proper logic levels.) This refresh can be done in a burst mode (32 cycles starting every 2.0 ms) or in a distributed mode where one cycle is done every 62.5 μs.

A refresh abort can be accomplished by treating a refresh cycle as a read-modify-write cycle with $\overline{CS}$ high. This type of cycle can be aborted any time until the R/W signal has been brought low to allow a $\phi 3$ clock to begin.

Non-Volatile Storage

In many digital systems, it is extremely important to retain data during emergencies such as power failure. Unfortunately, however, most random access read/write semiconductor memories such as the MCM6815A are volatile. That is, if power is removed from the semiconductor memory, stored information is lost. Therefore, non-volatility for a specified period of time becomes highly desirable – as a necessity to maintain irreplaceable information or as a convenience to avoid the time consuming and troublesome task of having to reload the memory.

The extremely low standby power dissipation of the MCM6815A makes it ideal for main memory applications requiring battery backup for non-volatility. For example, the MCM6815A can be employed in an 8K byte non-volatile main memory system application for microprocessors. The memory system can be partitioned into three major sections as illustrated in Figure 13. The first section contains the address buffers and the Read/Write and Chip Select decoding logic. The second section consists of the data bus buffering transceivers and the memory array (which consists of 16 MCM6815As) organized into two rows of 4K bytes each.

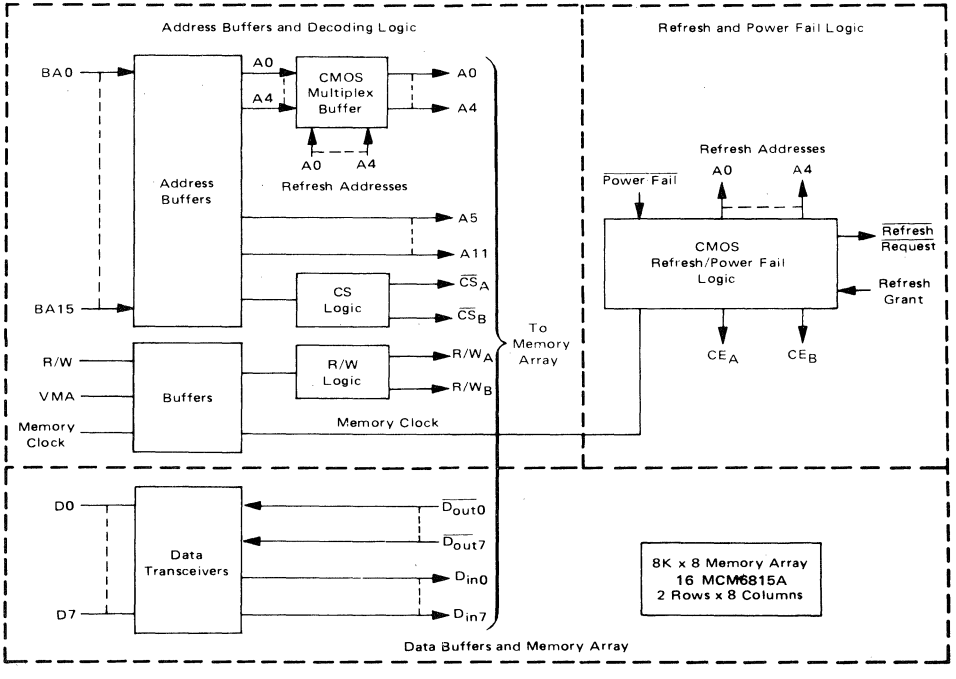
The third section of the block diagram comprises refresh and control logic for the memory system. This logic interfaces the timing of the refresh handshaking with the microprocessor (MPU) clock circuitry. It handles requests for refresh, the generation of refresh addresses, the synchronization of a $\overline{\text{Power Fail}}$ signal, the multiplexing of the external Memory Clock with the internal clock (used during standby), and the generation of a -5 V supply on the board using a charge-pump method.

The refresh control logic is illustrated in Figure 14. It handles the refreshing of the memory during both operating and standby modes. The timing for this logic is given in Figure 15. Figure 16 gives the memory timing for the standby mode only. Decoding of the memory clock (CE_A and CE_B) and the circuitry to synchronize the $\overline{\text{Power Fail}}$ signal are shown in Figure 17, with the timing given in Figure 18.

The memory device clock (CE_A and CE_B) during standby is created by a monostable multivibrator (MC14528) and buffered from the memory array by three MC14503 buffers in parallel. This clock is multiplexed with the $\overline{\text{Memory Clock}}$ by use of the three-state feature of the

4

FIGURE 13 – NON-VOLATILE MEMORY SYSTEM BLOCK DIAGRAM



MC14503. The $\overline{\text{Memory Clock}}$ (used during normal operation) is translated to 12 V levels by use of an MC3460 Clock Driver. Decoding of the CE_A and CE_B signals (i.e., clocking only the memory bank addressed) to conserve power is accomplished by the logic within the MC3460.

Since the $\overline{\text{Power Fail}}$ signal will occur asynchronously with both the $\overline{\text{Memory Clock}}$ and the refreshing operation (Refresh Clock), it is necessary to synchronize the $\overline{\text{Power Fail}}$ signal to the rest of the system in order to avoid aborting a memory access cycle or a refresh cycle. An MC14027 dual flip-flop is used as the basic synchronization device. The leading edge of the Refresh Clock triggers a 3 μs monostable multivibrator which is used as a refresh pretrigger. The trailing edge of this pretrigger triggers a 500 ns monostable which creates the CE pulse during standby operation. The 3 μs pretrigger signal is used to set half of the MC14027 flip-flop, the output of which, Ⓑ, then inhibits a changeover from the standby to the operating modes (or vice versa). This logic prevents the system from aborting a refresh cycle should the $\overline{\text{Power Fail}}$ signal change states just prior to or during a refresh cycle. The trailing edge of the 500 ns monostable clears the MC14027 flip-flop, enabling the second flip-flop in the package. The state of $\overline{\text{Power Fail}}$ and Power Fail is applied to the K and J inputs of this second flip-flop and is synchronized by clocking with $\overline{\text{Memory Clock}}$. The outputs of this flip-flop, labeled Bat and $\overline{\text{Bat}}$, lock the system into the refresh mode and multiplex in the internal clock for standby operation when Bat = "1". The voltage to logic not required for the refresh only mode of operation is removed to conserve power.

By using CMOS for the refresh logic and capacitance drivers, and a low current refresh oscillator, the standby current required for the 8K byte system is extremely small, as noted in Table 1. This low standby current requirement can be easily supplied for several days with standard type +12 V batteries. For more detailed information on this sytem and a large mainframe memory system, see Application Notes AN-732 and AN-740.

FIGURE 14 – REFRESH CONTROL LOGIC

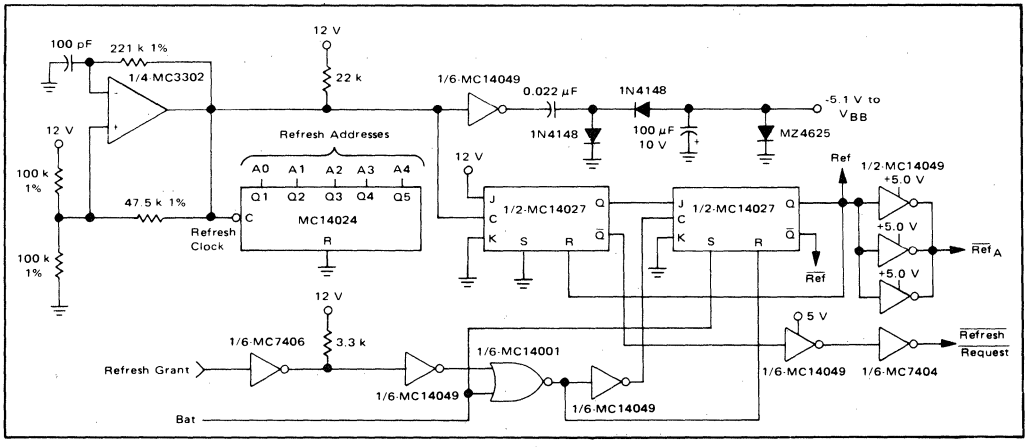


FIGURE 15 – REFRESH TIMING

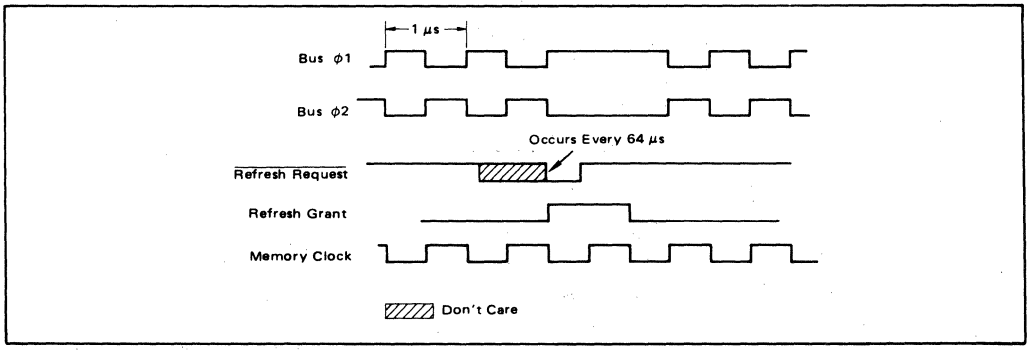


FIGURE 16 – MEMORY TIMING IN STANDBY MODE

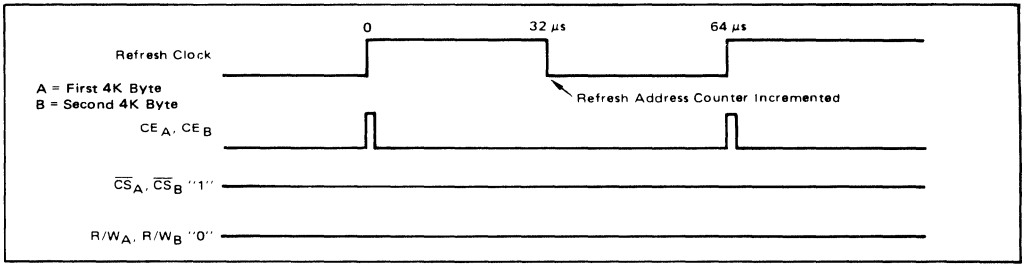


FIGURE 17 – POWER FAIL LOGIC AND CHIP ENABLE DRIVER

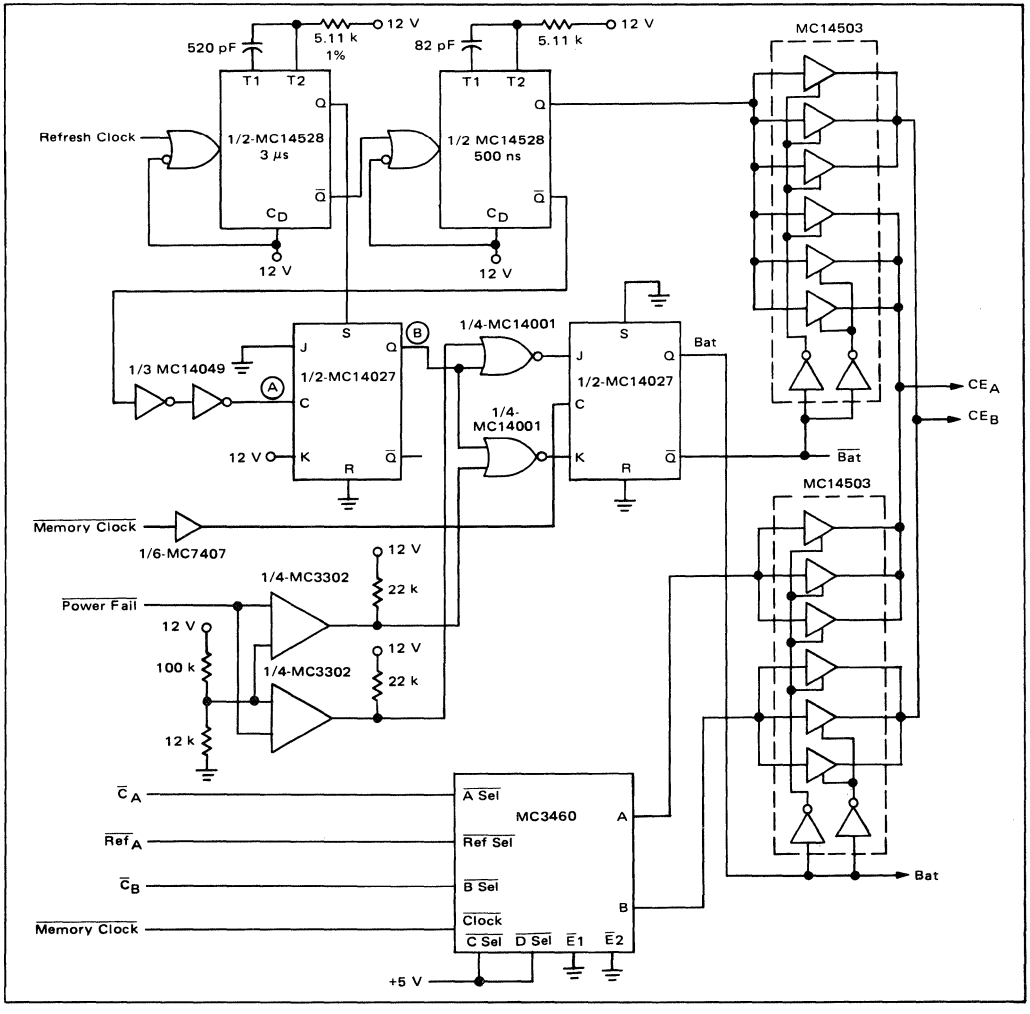


FIGURE 18 – POWER UP/DOWN SYNCHRONIZATION

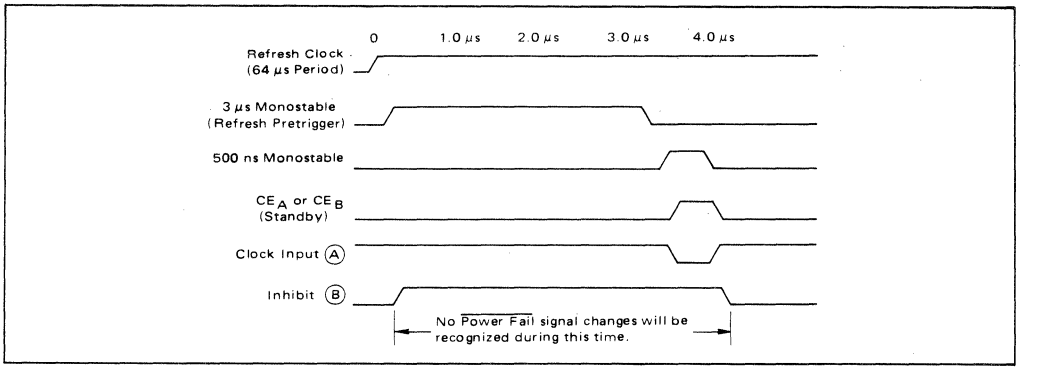
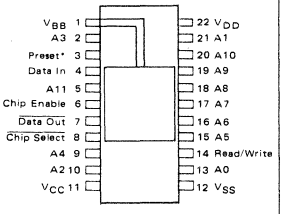


TABLE 1 – STANDBY MODE CURRENT ALLOCATION

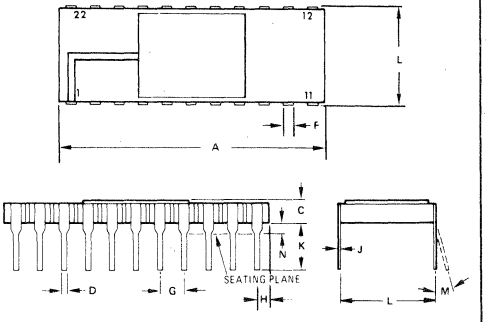
Circuit Section	Typical Current
+12 V Current (V_{DD}) for 16 MCM6815A's	5 mA
Charge Pump	3 mA
Comparator	2 mA
Capacitance Drivers	4 mA
Total	14 mA

PIN ASSIGNMENT



*See Applications Information

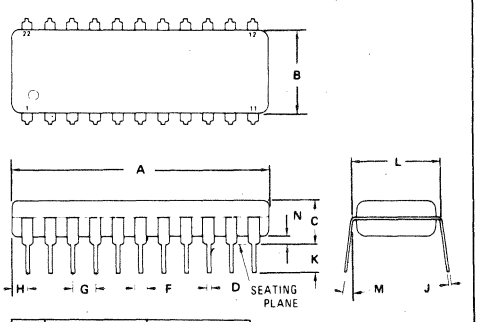
PACKAGE DIMENSIONS



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	27.05	27.94	1.065	1.100
C	2.16	3.68	0.085	0.145
D	0.43	0.58	0.017	0.023
F	1.02 REF		0.040 REF	
G	2.54 BSC		0.100 BSC	
H	0.76	1.78	0.030	0.070
J	0.20	0.30	0.008	0.012
K	3.18	4.45	0.125	0.175
L	9.65	10.67	0.380	0.420
M	–	7°	–	7°
N	0.64	1.27	0.025	0.050

NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.

CERAMIC PACKAGE
CASE 677-03



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	28.83	29.59	1.135	1.165
B	8.64	9.14	0.340	0.360
C	4.57	5.08	0.180	0.200
D	0.36	0.51	0.014	0.020
F	1.02	1.52	0.040	0.060
G	2.41	2.67	0.095	0.105
H	1.78	2.03	0.070	0.080
J	0.20	0.30	0.008	0.012
K	3.05	3.56	0.120	0.140
L	9.65	10.16	0.380	0.400
M	0°	10°	0°	10°
N	0.51	1.02	0.020	0.040

PLASTIC PACKAGE
CASE 708-01

MCM6830AL

Advance Information

1024 X 8-BIT READ ONLY MEMORY

The MCM6830A is a mask-programmable byte-organized memory designed for use in bus-organized systems. It is fabricated with N-channel silicon-gate technology. For ease of use, the device operates from a single power supply, has compatibility with TTL and DTL, and needs no clocks or refreshing because of static operation.

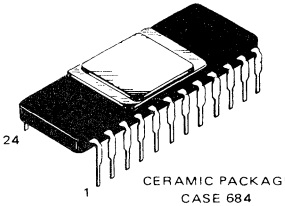
The memory is compatible with the M6800 Microcomputer Family, providing read only storage in byte increments. Memory expansion is provided through multiple Chip Select inputs. The active level of the Chip Select inputs and the memory content are defined by the customer.

- Organized as 1024 Bytes of 8 Bits
- Static Operation
- Three-State Data Output
- Four Chip Select Inputs (Programmable)
- Single 5-Volt Power Supply
- TTL Compatible
- Maximum Access Time = 500 ns

MOS

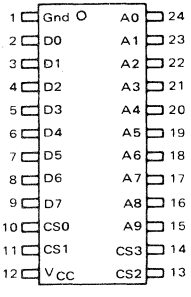
(N-CHANNEL, SILICON-GATE)

1024 X 8-BIT READ ONLY MEMORY



CERAMIC PACKAGE
CASE 684

PIN ASSIGNMENT

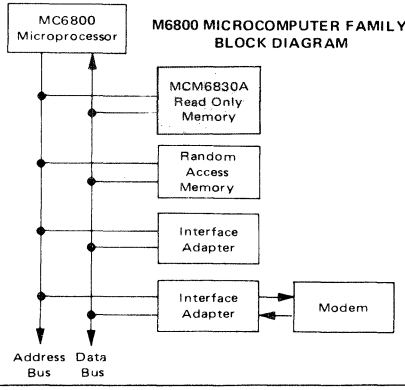


ABSOLUTE MAXIMUM RATINGS (See Note 1)

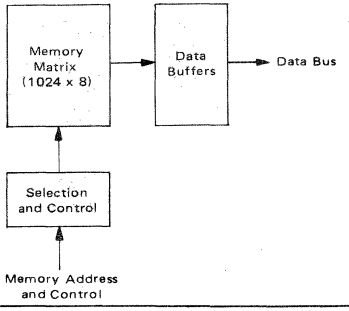
Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.3 to +7.0	Vdc
Input Voltage	V_{in}	-0.3 to +7.0	Vdc
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

NOTE 1: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

M6800 MICROCOMPUTER FAMILY BLOCK DIAGRAM



MCM6830A READ ONLY MEMORY BLOCK DIAGRAM



This is advance information and specifications are subject to change without notice.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted.)

RECOMMENDED DC OPERATING CONDITIONS

Parameter	Symbol	Min	Nom	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	Vdc
Input High Voltage	V_{IH}	2.0	–	5.25	Vdc
Input Low Voltage	V_{IL}	-0.3	–	0.8	Vdc

DC CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit
Input Current (V_{in} = 0 to 5.25 V)	I_{in}	–	–	2.5	μAdc
Output High Voltage (I_{OH} = −205μA)	V_{OH}	2.4	–	–	Vdc
Output Low Voltage (I_{OL} = 1.6 mA)	V_{OL}	–	–	0.4	Vdc
Output Leakage Current (Three-State) (CS = 0.8 V or $\overline{CS}$ = 2.0 V, V_{out} = 0.4 V to 2.4 V)	I_{LO}	–	–	10	μAdc
Supply Current (V_{CC} = 5.25 V, T_A = 0°C)	I_{CC}	–	–	130	mAdc

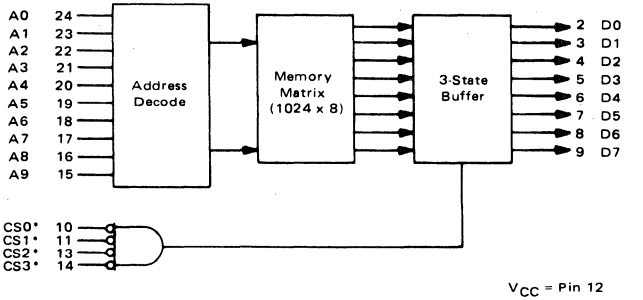
4

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, periodically sampled rather than 100% tested.)

Characteristic	Symbol	Max	Unit
Input Capacitance	C_{in}	7.5	pF
Output Capacitance	C_{out}	12.5	pF

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

BLOCK DIAGRAM



*Active level defined by the customer.

V_{CC} = Pin 12
Gnd = Pin 1

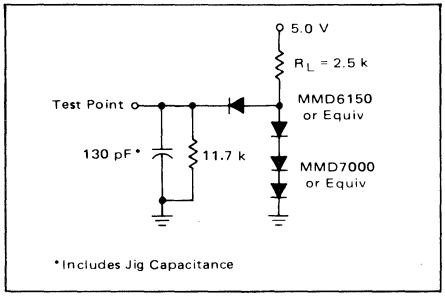
AC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature unless otherwise noted.)

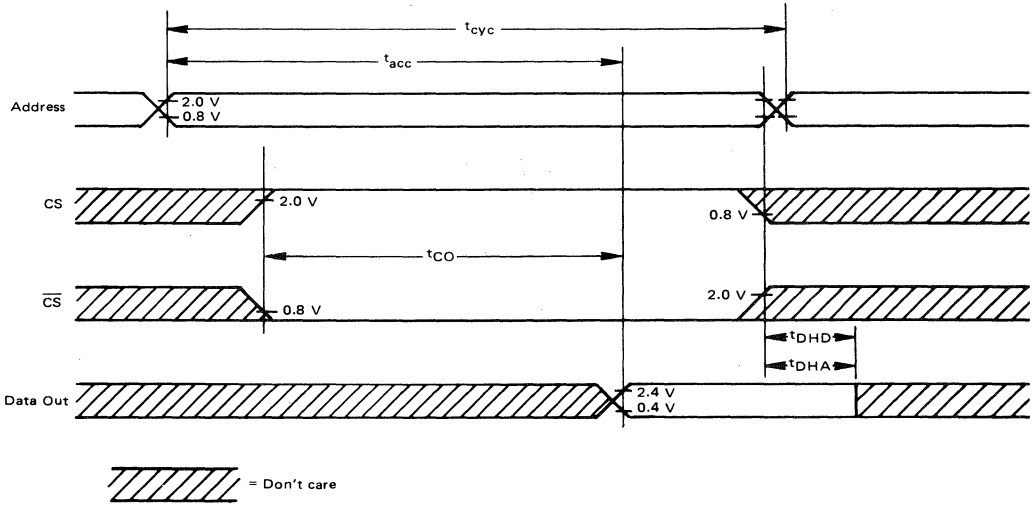
(All timing with $t_r = t_f = 20$ ns, Load of Figure 1)

Characteristic	Symbol	Min	Max	Unit
Cycle Time	t_{cyc}	500	–	ns
Access Time	t_{acc}	–	500	ns
Chip Select to Output Delay	t_{CO}	–	300	ns
Data Hold from Address	t_{DHA}	10	–	ns
Data Hold from Deselection	t_{DHD}	10	150	ns

FIGURE 1 – AC TEST LOAD



TIMING DIAGRAM



CUSTOM PROGRAMMING

By the programming of a single photomask for the MCM6830A, the customer may specify the content of the memory and the method of enabling the outputs.

Information on the general options of the MCM6830A should be submitted on an Organizational Data form such as that shown in Figure 3.

Information for custom memory content may be sent to Motorola in one of two forms (shown in order of preference):

1. Paper tape output of the Motorola M6800 Software.
2. Hexadecimal coding using IBM Punch Cards.

PAPER TAPE

Included in the software packages developed for the M6800 Microcomputer Family is the ability to produce a paper tape output for computerized mask generation. The procedure for generating and verifying a system is shown in Figure 4. The assembler directives are used to control allocation of memory, to assign values for stored data, and for controlling the assembly process. The paper tape must specify the full 1024 bytes.

Note: Motorola can accept magnetic tape and truth table table formats. For further information, contact your local Motorola sales representative.

FIGURE 2 – BINARY TO HEXADECIMAL CONVERSION

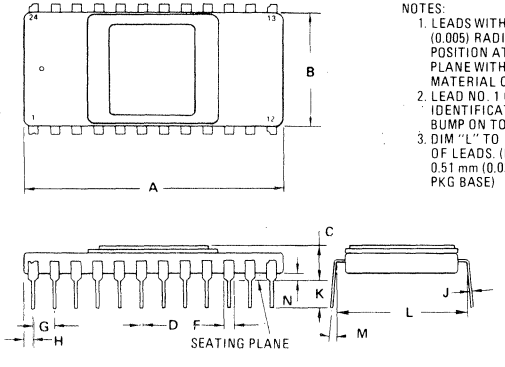
Binary Data				Hexadecimal Character
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	A
1	0	1	1	B
1	1	0	0	C
1	1	0	1	D
1	1	1	0	E
1	1	1	1	F

IBM PUNCH CARDS

The hexadecimal equivalent (from Figure 2) may be placed on 80 column IBM punch cards as follows:

Step	Column	
1	12	Byte "0" Hexadecimal equivalent for outputs D7 thru D4 (D7 = M.S.B.)
2	13	Byte "0" Hexadecimal equivalent for outputs D3 thru D0 (D3 = M.S.B.)
3	14-75	Alternate steps 1 and 2 for consecutive bytes.
4	77-78	Card number (starting 01)
5	79-80	Total number of cards (32)

PACKAGE DIMENSIONS



NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE WITH MAXIMUM MATERIAL CONDITION.
2. LEAD NO. 1 CUT FOR IDENTIFICATION, OR BUMP ON TOP.
3. DIM "L" TO INSIDE OF LEADS. (MEASURED 0.51 mm (0.020) BELOW PKG BASE)

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	29.34	30.86	1.155	1.215
B	12.70	14.22	0.500	0.560
C	3.05	3.94	0.120	0.155
D	0.38	0.51	0.015	0.020
F	0.89	1.40	0.035	0.055
G	2.54 BSC		0.100 BSC	
H	0.89	1.40	0.035	0.055
J	0.20	0.30	0.008	0.012
K	2.92	3.68	0.115	0.145
L	14.86	15.87	0.585	0.625
M	–	15^0	–	15^0
N	0.51	1.14	0.020	0.045

CASE 684-04

FIGURE 3 – FORMAT FOR PROGRAMMING GENERAL OPTIONS

ORGANIZATIONAL DATA
MCM6830A MOS READ ONLY MEMORY

Customer:

Company _____

Part No. _____

Originator _____

Phone No. _____

Motorola Use Only:

Quote: _____

Part No.: _____

Specif. No.: _____

Enable Options:

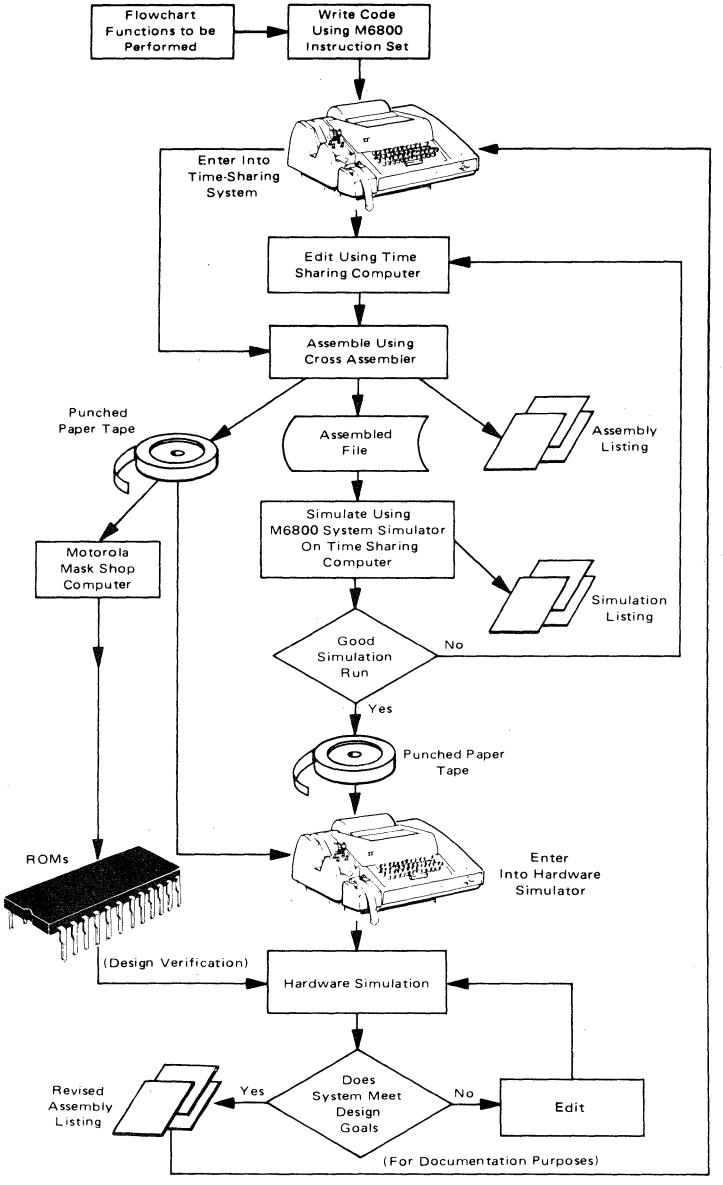
	1	0
CS0	☐	☐
CS1	☐	☐
CS2	☐	☐
CS3	☐	☐

Input Logic Levels:

1 is most positive
0 is most negative

4

FIGURE 4 – SYSTEM DESIGN AND VERIFICATION PROCEDURE



MCM68317L

Product Preview

16,384-BIT READ ONLY MEMORY

The MCM68317 is a 16,384-bit high-speed Read Only Memory designed for high-performance, low-cost applications. Organized as 2048 eight-bit bytes, the device optimizes speed, power, and density trade-offs.

For ease of use, the memory operates from a single +5 volt power supply. No clocks or refreshing are required because of static operation. All inputs are TTL compatible, and the outputs are three-state TTL compatible.

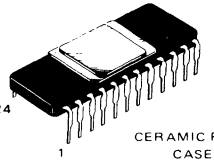
The MCM68317 is a logical extension of the MCM68708, an 8192-bit AROM. An additional address, A10, replaces the V_{DD} power supply at pin 19, and CS2 replaces the Program input at pin 18. V_{BB} is removed, leaving pin 21 with no connection.

- Organized as 2048 Bytes of 8-Bits
- Static Operation
- Single +5 Volt Power Supply
- Access Time = 500 ns
- Low Power Dissipation
- Two Chip Select Inputs Available for Memory Expansion
- TTL Compatible
- Three-State Outputs
- Logical Extension of the MCM68708 AROM

MOS

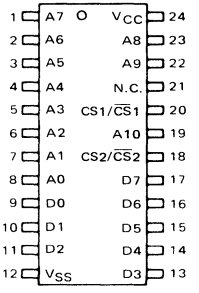
(N-CHANNEL)

2048 X 8-BIT STATIC
READ ONLY MEMORY

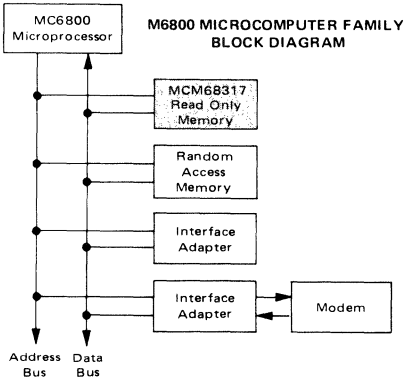


CERAMIC PACKAGE
CASE 684

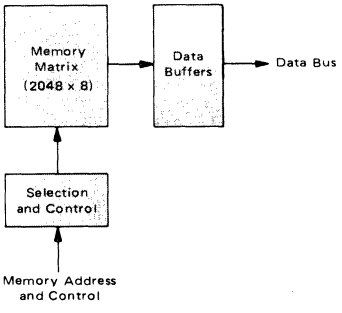
PIN ASSIGNMENT



M6800 MICROCOMPUTER FAMILY
BLOCK DIAGRAM

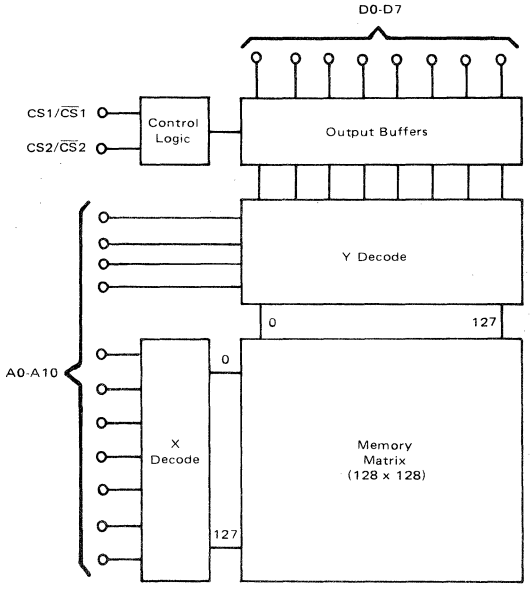


MCM68317 READ ONLY MEMORY
BLOCK DIAGRAM



This is advance information and specifications are subject to change without notice.

BLOCK DIAGRAM



MCM6832L

Advance Information

2048 x 8-BIT READ ONLY MEMORY

The MCM6832 is a mask-programmable byte-organized memory designed for use in bus-organized systems. It is fabricated with N-channel metal-gate technology. For ease of use, the device is compatible with TTL and DTL, and needs no clocks or refreshing because of static operation.

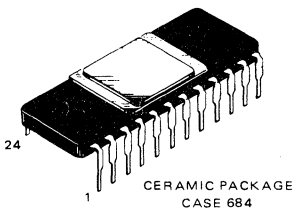
The memory is compatible with the M6800 Microcomputer Family, providing read only storage in byte increments. Memory expansion is provided through a Chip Select input. The active level of the Chip Select input and the memory content are defined by the customer.

- Organized as 2048 Bytes of 8 Bits
- Static Operation
- Three-State Data Output
- Programmable Chip Select
- TTL Compatible
- Maximum Access Time = 550 ns

MOS

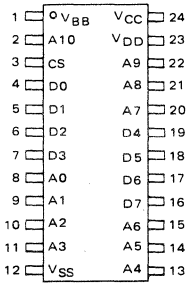
(N-CHANNEL, LOW THRESHOLD)

2048 x 8-BIT READ ONLY MEMORY



CERAMIC PACKAGE
CASE 684

PIN ASSIGNMENT

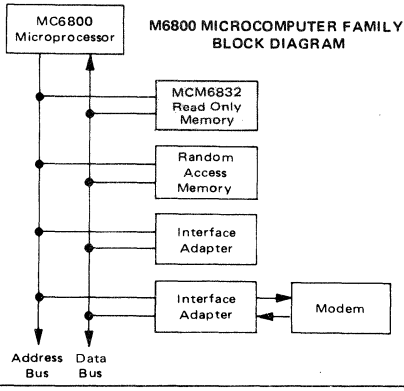


ABSOLUTE MAXIMUM RATINGS[1] (Referenced to V_{SS})

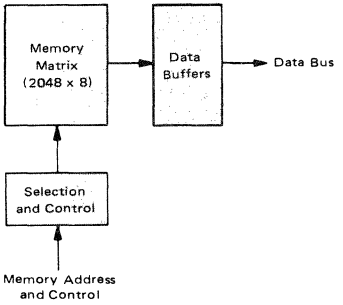
Rating	Symbol	Value	Unit
Supply Voltages	V_{DD} V_{CC} V_{BB}	-0.3 to +15 -0.3 to +6.0 -10 to +0.3	Vdc
Address/Control Input Voltage	V_{in}	-0.3 to +15	Vdc
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-55 to +125	°C

Note 1: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

M6800 MICROCOMPUTER FAMILY BLOCK DIAGRAM



MCM6832 READ ONLY MEMORY BLOCK DIAGRAM



This is advance information and specifications are subject to change without notice.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted.)

RECOMMENDED DC OPERATING CONDITIONS (Referenced to V_{SS} = Ground)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{DD}	11.4	12	12.6	Vdc
	V_{CC}	4.75	5.0	5.25	Vdc
	V_{BB}	-5.25	-5.0	-4.75	Vdc
Input High Voltage (A_n, CS)	V_{IH}	3.0	–	V_{CC}	Vdc
Input Low Voltage (A_n, CS)	V_{IL}	-0.3	–	0.8	Vdc

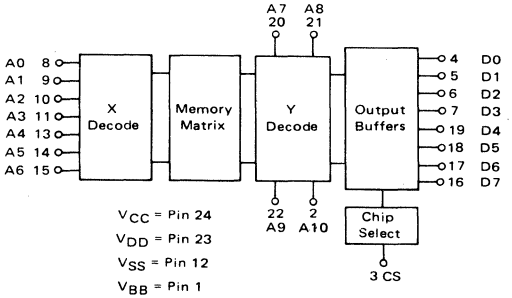
DC CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit
Input Leakage Current (A_n, CS) (V_{in} = 0 to 5.25 V)	I_{in}	–	–	10	μAdc
Output Leakage Current (Three-State) (V_O = 0.4 V to -2.4 V, CS = 0.4 V or $\overline{CS}$ = 2.4 V)	I_{LO}	–	–	10	μAdc
Output High Voltage (I_{OH} = -100 μA)	V_{OH}	3.7	–	V_{CC}	Vdc
Output Low Voltage (I_{OL} = 1.6 mA)	V_{OL}	0	–	0.4	Vdc
Supply Current (Chip Deselected or Selected)	I_{DD}	–	–	25	mAdc
	I_{CC}	–	–	45	mAdc
	I_{BB}	–	–	500	μAdc

CAPACITANCE (Periodically Sampled Rather Than 100% Tested.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Capacitance (f = 1 MHz)	C_{in}	–	5.0	7.5	pF
Output Capacitance (f = 1 MHz)	C_{out}	–	5.0	10	pF

BLOCK DIAGRAM



AC CHARACTERISTICS

(Full operating voltage and temperature unless otherwise noted. All timing with $t_r = t_f \leq 20$ ns; Load = 1 TTL Gate (MC7400 Series) biased to draw 1.6 mA; C_L = 130 pF.)

Characteristic	Symbol	Min	Typ*	Max	Unit
Address Access Time	t_{acc}	–	320*	550	ns
Output Select Time	t_{OS}	–	175*	300	ns
Output Deselect Time	t_{OD}	30	100*	150	ns

*Typical values measured at 25°C and nominal supply voltages.

FIGURE 1 – AC TEST LOAD

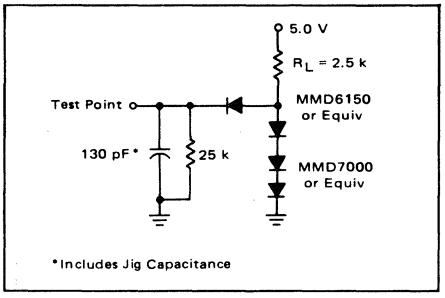
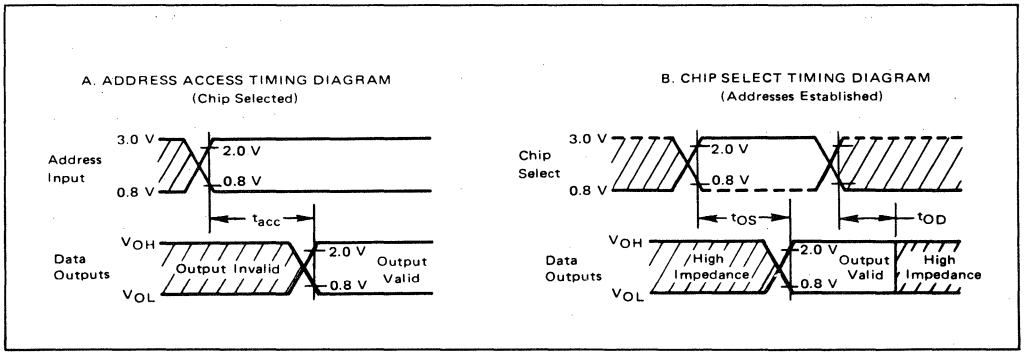


FIGURE 2 – TIMING DIAGRAM



CUSTOM PROGRAMMING

By the programming of a single photomask for the MCM6832, the customer may specify the content of the memory and the method of enabling the outputs.

Information on the general options of the MCM6832 should be submitted on an Organizational Data form such as that shown in Figure 4.

Information for custom memory content may be sent to Motorola in one of two forms (shown in order of preference):

1. Paper tape output of the Motorola M6800 Software.
2. Hexadecimal coding using IBM Punch Cards.

PAPER TAPE

Included in the software packages developed for the M6800 Microcomputer Family is the ability to produce a paper tape output for computerized mask generation. The procedure for generating and verifying a system is shown in Figure 5. The assembler directives are used to control allocation of memory, to assign values for stored data, and for controlling the assembly process. The paper tape must specify the full 2048 bytes.

Note: Motorola can accept magnetic tape and truth table table formats. For further information, contact your local Motorola sales representative.

FIGURE 3 – BINARY TO HEXADECIMAL CONVERSION

MSB D7	D6	D5	LSB D4	Hexadecimal
D3	D2	D1	D0	Character
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	A
1	0	1	1	B
1	1	0	0	C
1	1	0	1	D
1	1	1	0	E
1	1	1	1	F

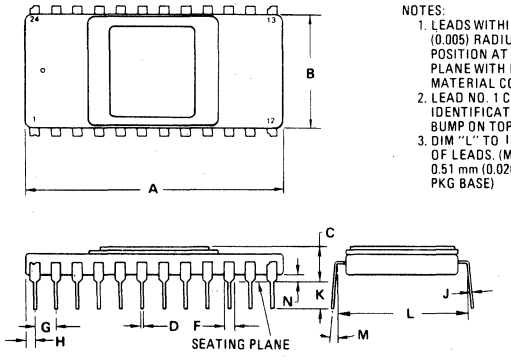
$0 = V_{OL}$
$1 = V_{OH}$

IBM PUNCH CARDS

The hexadecimal equivalent (from Figure 3) may be placed on 80 column IBM punch cards as follows:

Step	Column	
1	12	Byte "0" Hexadecimal equivalent for outputs D7 thru D4 (D7 = M.S.B.)
2	13	Byte "0" Hexadecimal equivalent for outputs D3 thru D0 (D3 = M.S.B.)
3	14-75	Alternate steps 1 and 2 for consecutive bytes.
4	77-78	Card number (starting 01)
5	79-80	Total number of cards (64)

PACKAGE DIMENSIONS



NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE WITH MAXIMUM MATERIAL CONDITION.
2. LEAD NO. 1 CUT FOR IDENTIFICATION, OR BUMP ON TOP.
3. DIM "L" TO INSIDE OF LEADS. (MEASURED 0.51 mm (0.020) BELOW PKG BASE)

DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	29.34	30.86	1.155	1.215
B	12.70	14.22	0.500	0.560
C	3.05	3.94	0.120	0.155
D	0.38	0.51	0.015	0.020
F	0.89	1.40	0.035	0.055
G	2.54 BSC		0.100 BSC	
H	0.89	1.40	0.035	0.055
J	0.20	0.30	0.008	0.012
K	2.92	3.68	0.115	0.145
L	14.86	15.87	0.585	0.625
M	–	15°	–	15°
N	0.51	1.14	0.020	0.045

CASE 684-04

FIGURE 4 – FORMAT FOR PROGRAMMING GENERAL OPTIONS

ORGANIZATIONAL DATA
MCM6832 MOS READ ONLY MEMORY

Customer:

Company _____

Part No. _____

Originator _____

Phone No. _____

Motorola Use Only:

Quote: _____

Part No.: _____

Specif. No.: _____

4

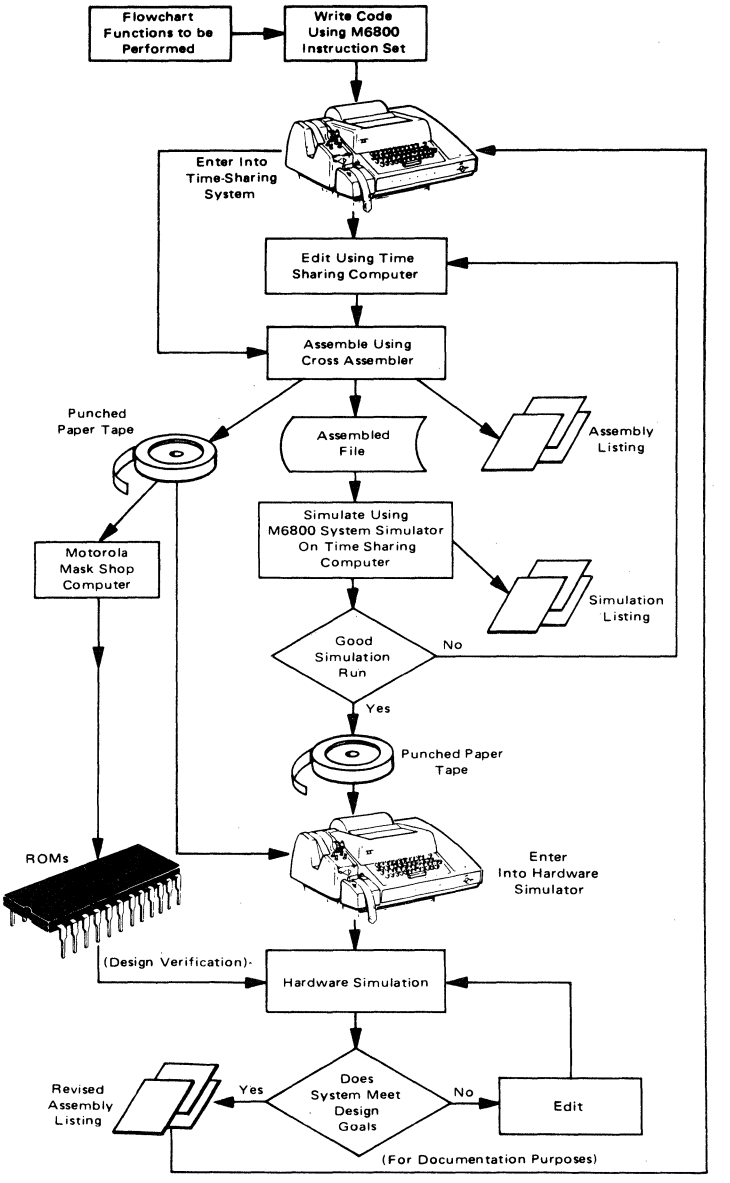
True Chip Select Options:

I. 1 ☐

II. 0 ☐

1 is most positive input
0 is most negative input

FIGURE 5 – SYSTEM DESIGN AND VERIFICATION PROCEDURE



4

MCM68708L

Product Preview

1024 X 8-BIT READ ONLY MEMORY

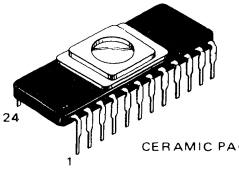
The MCM68708 is an 8192-bit Alterable Read Only Memory designed for system debug usage and similar applications requiring non-volatile memory that must be reprogrammed periodically. The transparent lid on the package allows the memory content to be erased with ultraviolet light. The memory can then be electrically reprogrammed.

- Organized as 1024 Bytes of 8-Bits
- Static Operation
- Standard Power Supplies of +12 V, +5 V, and -5 V.
- Access Time = 500 ns
- Low Power Dissipation
- Chip Select Input for Memory Expansion
- TTL Compatible
- Three-State Outputs
- Compatible with the 2708

MOS

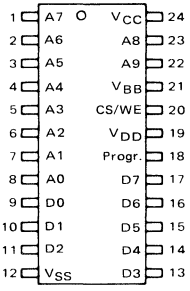
(N-CHANNEL, SILICON-GATE)

1024 X 8-BIT ALTERABLE READ ONLY MEMORY

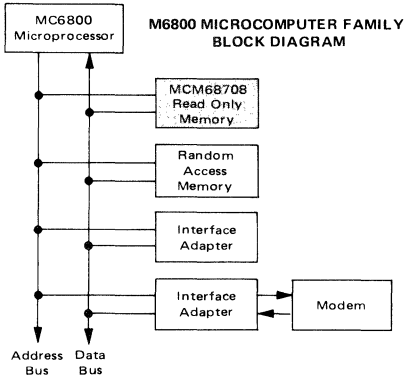


CERAMIC PACKAGE

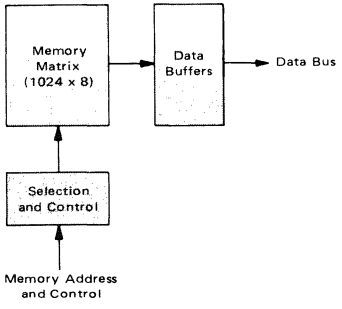
PIN ASSIGNMENT



M6800 MICROCOMPUTER FAMILY BLOCK DIAGRAM

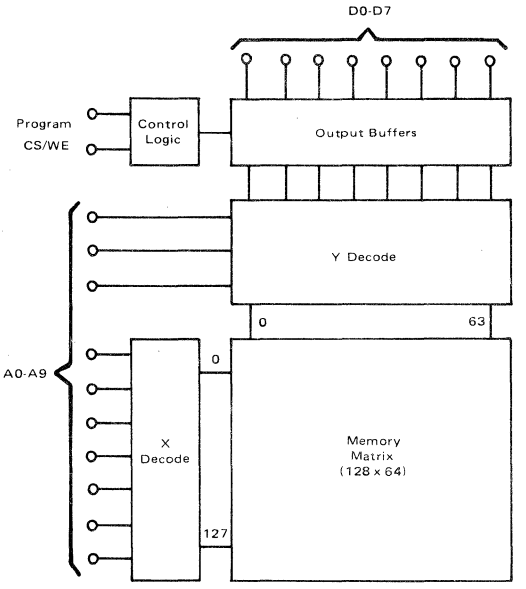


MCM68708 READ ONLY MEMORY BLOCK DIAGRAM

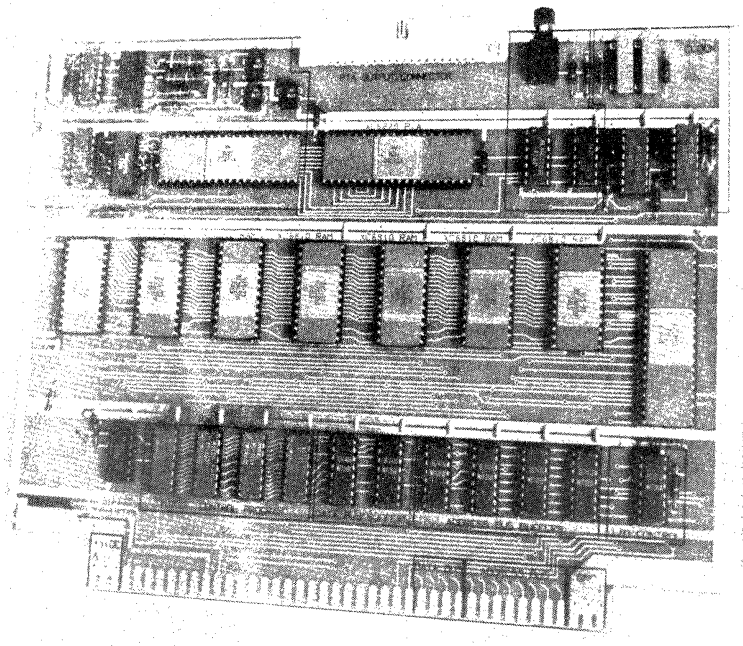


This is advance information and specifications are subject to change without notice.

BLOCK DIAGRAM



4



Application Notes/Chapter 5

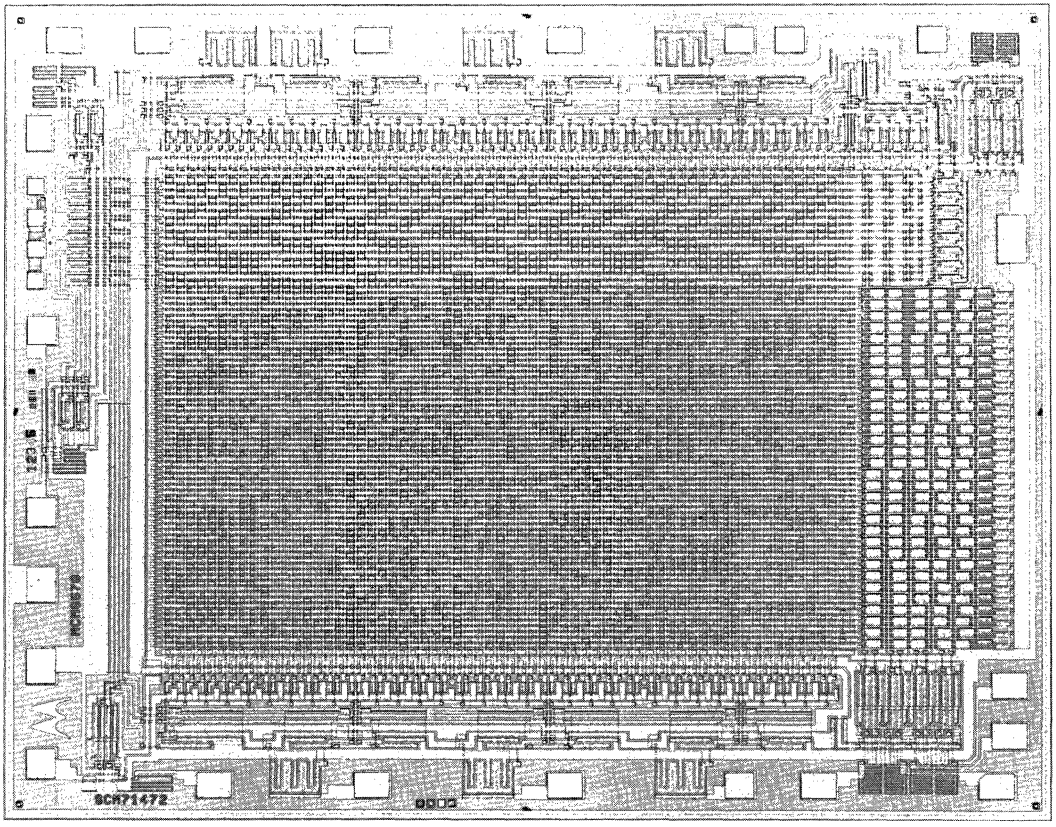
INTRODUCTION

Today's highly developed NMOS technology has produced a wide variety of NMOS memory products that can be utilized in a multitude of digital processing applications. Since the variety of these applications is so broad, it is impractical to cover all of them. However, the application notes in this section do discuss some of the most common storage applications.

For reference purposes, all the available Motorola application notes and their abstracts are tabulated in the Application Information section of the Motorola Semiconductor Data Library Master Index. A copy of the current Application Note Catalog may be obtained by sending your request to:

Technical Information Center
Motorola Semiconductor Products Inc.
P.O. Box 20912
Phoenix, Arizona 85036

A CRT DISPLAY SYSTEM USING NMOS MEMORIES



The emerging NMOS semiconductor technology offers electronic equipment manufacturers improved circuit performance and density. Development of the NMOS process brings a new era of high-density memory technology, and it shows great promise for replacing core and other type memories. For CRT display manufacturers, however, NMOS technology is here today with the introduction of the MCM6571 8K Character Generator and the MC6545 quad 80-bit Shift Register. This paper describes a CRT display system using these devices.

BASIC CRT OPERATION

The basic elements of a display system is the CRT and the circuitry necessary to deflect and modulate the electron beam. The system must be capable of generating graphics and/or alphanumeric characters. The operation of most video display systems is similar to a TV set. The electron gun shoots a beam of electrons toward a screen coated with a light emitting phosphor. Wherever the beam strikes, a dot of light is emitted. The beam is deflected vertically and horizontally by either electrostatic or elec-

tromagnetic fields. The Z-axis grid can switch the electron beam on and off. By modulating the beam with the Z-axis grid, dots and line segments can be formed on the screen.

Due to the fact that the screen phosphor can hold the image for only a short time, the image must be constantly refreshed. The refresh rate is usually between 30 and 60 Hz. Because of the Z-axis modulation and the refresh requirement, two types of components are especially important to an alphanumeric CRT display: a character generator for modulating the Z-axis to form the character, and a storage device to retain the information to be refreshed on the screen.

CHARACTER FORMATION

The most popular type of character formation being used today is the dot matrix method. Figure 1(a) shows the dot matrix which must be generated at every character location to form the image. Any size dot matrix is possible, but 5 x 7 and 7 x 9 are the most popular configurations with the 7 x 9 offering clearer definition. Any character can be formed within the matrix by illuminating the proper dots (see Figure 1(b)).

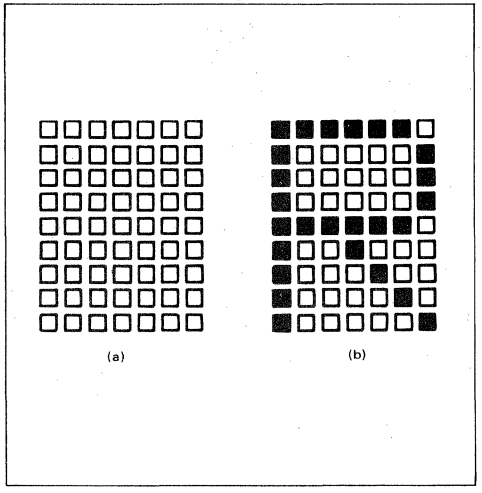


FIGURE 1

Systems using the dot matrix formation will usually generate a raster on the screen of the CRT. If a horizontal AC field is applied to the electron beam, it traces and retraces a line across the screen. If, at the same time, a vertical AC field of a lower frequency is applied and if the beam is shut off during retrace, many lines are generated, and a horizontal raster scan is formed (see Figure 2). Interchanging the frequencies generates a vertical scan. Dot matrices can be formed and separated at every character location by blanking the electronic beam in between matrices. The character location map shown in Figure 9 demonstrates this formation. The numbers indicating column and line location are explained later. As

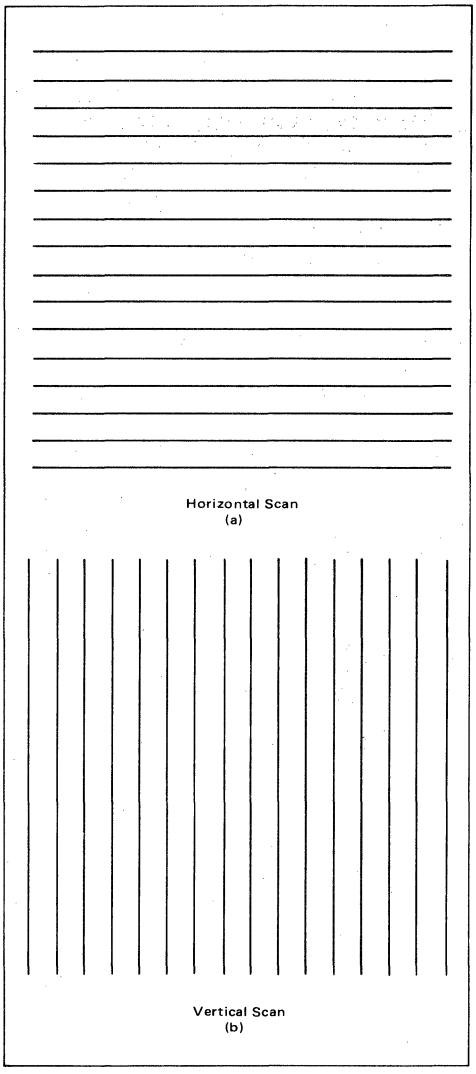


FIGURE 2

mentioned before, a character can be formed in each matrix by illuminating the proper dots.

The device that determines which dots are to be illuminated is called a character generator. Actually, it is a read-only memory containing a dot matrix pre-programmed for each character. Because of pin limitations, the entire dot matrix usually cannot be read out at one time. Instead, characters are read out a row or a column at a time. A row character generator would most efficiently be used with a horizontal scan and a column character generator, with a vertical scan display.

8K-BIT CHARACTER GENERATOR

NMOS technology has produced a new character generator with greater storage capability than the older PMOS devices. The MCM6570 is an 8192 bit, row character generator that can be mask programmed with any desired set of 128 characters. This device can be programmed in Japanese, Hebrew, or any special type of character or symbol format. It generates each character in a 7 x 9 matrix, and it is capable of automatically shifting descenders (such as g, j, p, q, and y). It is directly TTL compatible. This device can also interface directly with other NMOS devices and with Complementary MOS when using a +5 volt power supply.

A 7-bit character code (see Figure 3) is used to select any one of the 128 available characters. The rows can be sequentially selected, providing a nine-word sequence of seven parallel bits per word for each character selected. As the row select inputs are sequentially addressed, the ROM will automatically place the 7 x 9 character in one of two pre-programmed positions on the 16 row matrix (see Figure 6), with the positions defined by the four row select inputs. Maximum access time is 500 ns; however, if a device is programmed with shifted characters, the access time can be reduced to 300 ns.

The MCM6571 is a pre-programmed version of the MCM6570 with a modified USASCII code input. It contains the upper and lower case English alphabet, commonly used lower case Greek letters, numbers 0 to 9 and various mathematical symbols and punctuation marks. In fact any type of specialized symbols can be generated. Figure 6 shows which row of the character matrix is generated for each of the possible row select inputs. When a descending character is selected, rows R14 thru R12 are automatically blanked. The next nine rows form the descending character matrix. Thus, while any one character is contained in a 7 x 9 matrix, a 7 x 12 matrix must be available on the CRT screen to contain both normal and descending characters. The MCM6571 uses a down count to display the rows of the character from top to bottom. The MCM6570 mask-programmable ROM allows a choice of either an up or a down count for this function.

The MCM6570 requires three power supplies: -3, +5, and +12 volts. In systems using only +5 volts, special requirements of -3 and +12 volts can be an inconvenience. Because the device requires only small amounts of current from these supplies, and charge pump techniques using +5 volt supply can be used. A supply shown in Figure 4 will generate the required -3 volts at less than 100μa. In Figure 5, a +12 supply is shown that will provide the 6 ma that typically is required from the 12V source.

STORAGE

As discussed earlier, the image on the CRT must be constantly refreshed; thus, a storage device is required to retain the information. Two types of storage devices can be used in this application: Random Access Memories and shift registers. RAM's offer the cost advantages resulting from high volume use and offer minimum access time when interfacing with a computer. Also, because of the random-access feature, no buffer storage is required. Shift registers are also low-cost devices offering simple editing functions; in particular, insertion operations.

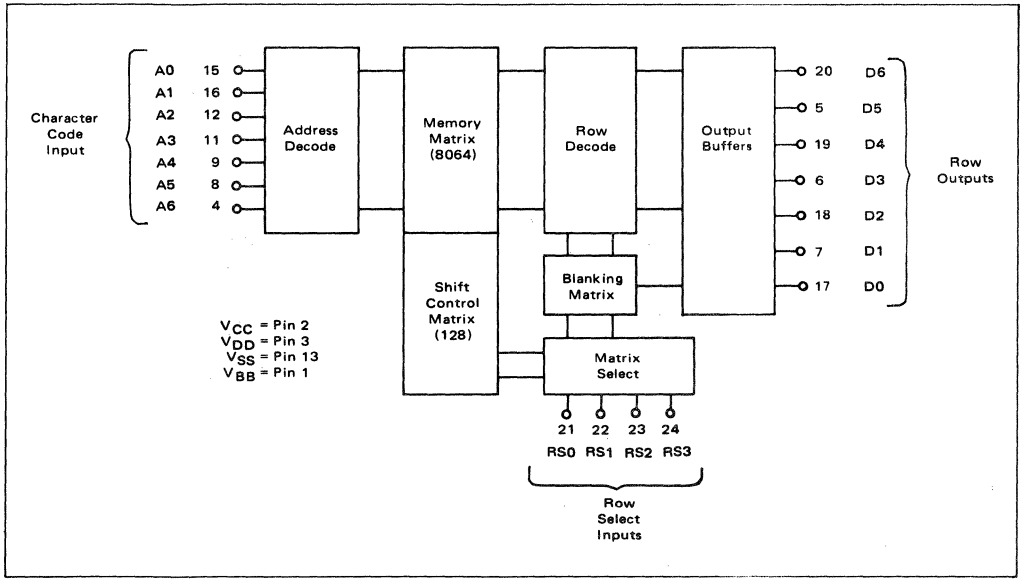


FIGURE 3

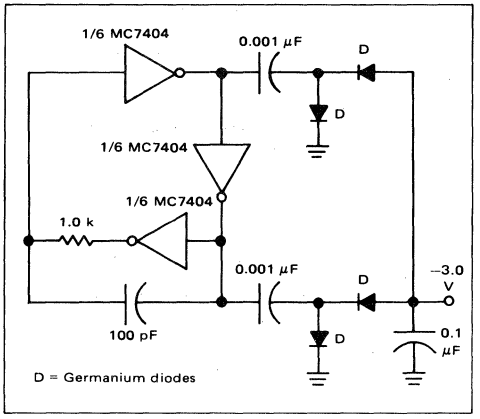


FIGURE 4 – – 3 VOLT POWER SUPPLY

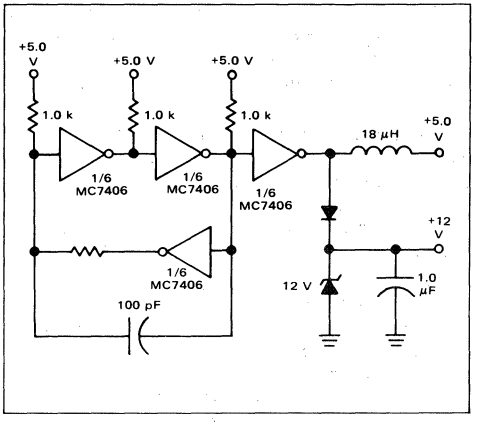


FIGURE 5 – +12 VOLT POWER SUPPLY

ROW SELECT
TRUTH TABLE

RS3	RS2	RS1	RS0	OUTPUT
0	0	0	0	R0
0	0	0	1	R1
0	0	1	0	R2
0	0	1	1	R3
0	1	0	0	R4
0	1	0	1	R5
0	1	1	0	R6
0	1	1	1	R7
1	0	0	0	R8
1	0	0	1	R9
1	0	1	0	R10
1	0	1	1	R11
1	1	0	0	R12
1	1	0	1	R13
1	1	1	0	R14
1	1	1	1	R15

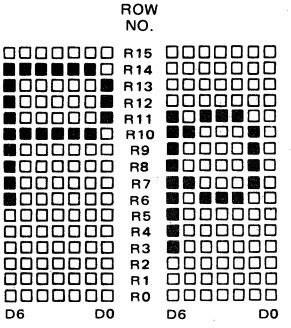


FIGURE 6

The necessity of a buffer register is an unattractive requirement of shift storage. Buffer storage is necessary because of the way the characters are written on the screen (see Figure 7). As the electron beam moves across the screen, each character code is applied in turn to the character generator and the first row of each character is read out. At the end of the row, the electron beam retraces and begins moving across the screen again. The same set of character codes must be presented to the character generator again so that the second row can be written. This procedure must be repeated until all nine rows have been written. With shift register storage, the information for a particular line would not be available after the first row was written, unless the information were shifted all the way around. If the shift register is large, system speed limitations would result. The buffer register can be eliminated, if small shift registers (storage capability of only one or two lines) are used in parallel. An ideal feature of these small shift registers would be 3-state outputs.

An excellent device for this application is the MC6545 Quad 80-bit shift register. It is an NMOS device and thus, is TTL compatible and also it will interface with other NMOS and with CMOS devices. The Quad 80 features internal recirculate logic, and a single clock with frequency capability of D.C. to 5 MHz. The shift register's static storage mode is when the clock logic level is "0".

THE SYSTEM

A CRT display system designed and built using the MCM6571 for character generation and the MC6545 for storage is shown in block form in Figure 8. It can display up to 640 characters (16 lines with 40

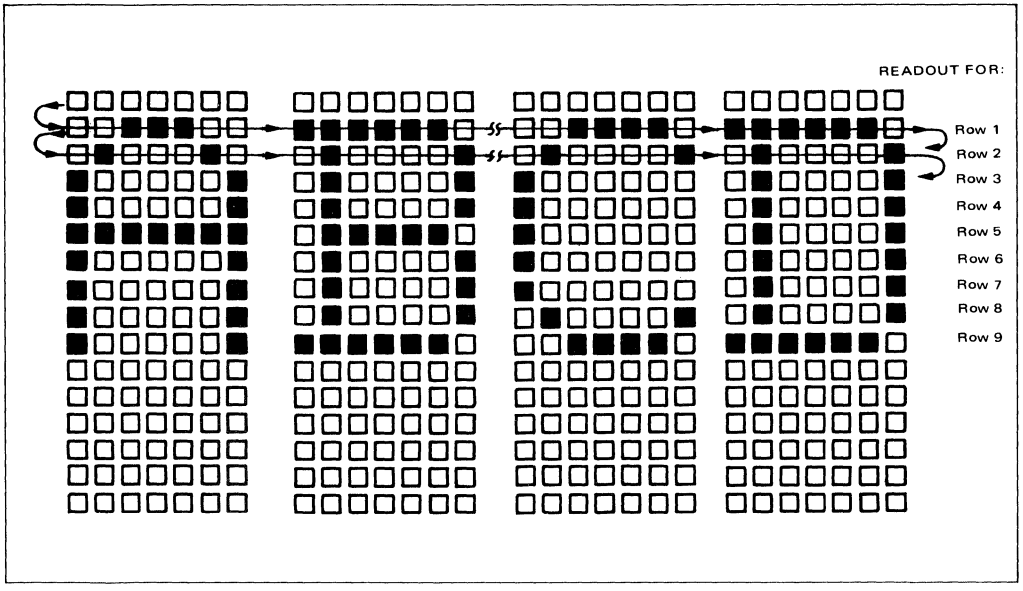


FIGURE 7

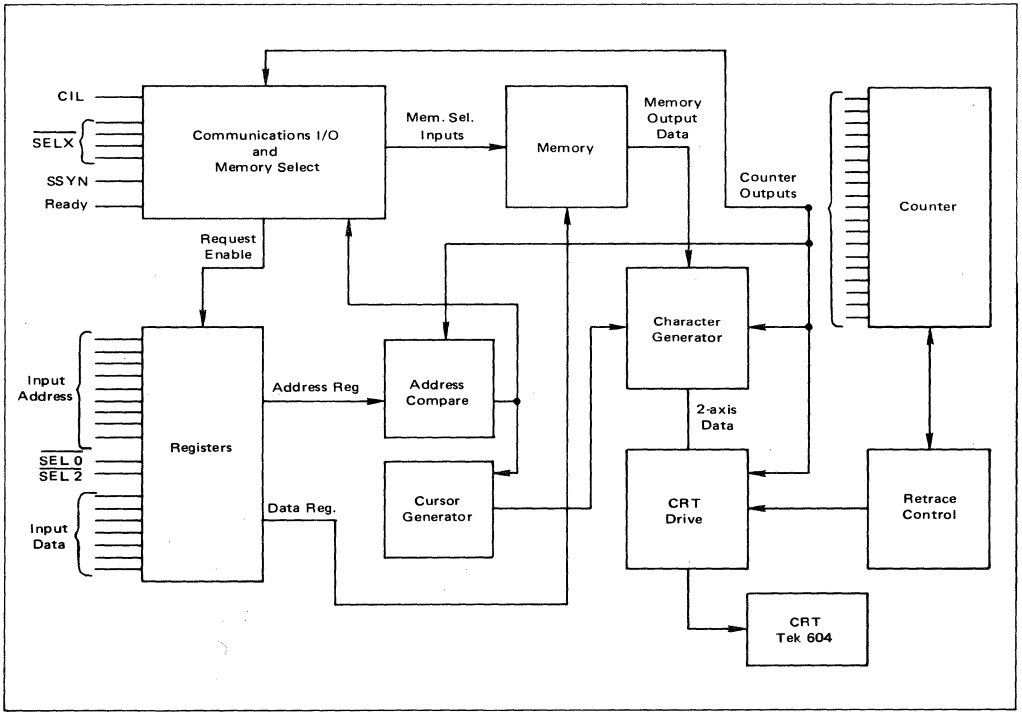


FIGURE 8

characters/line) and has a refresh rate of 60 Hz. The system is built on six circuit boards divided into the following function areas:

1) Counter and Retrace Control
2) Memory
3) Character Generation and CRT Drive
4) Input Address and Data, and Cursor Generation
5) Communications I/O and Memory Select
6) Power Supplies

The CRT display used is a Tektronix 604. It can be mounted in a standard 19" rack and the X, Y, and Z inputs can be driven by +5 and +12 volt supply circuitry. The other circuit blocks are mounted along side the 604. The counter is the central coordinator of the system, and it performs the following functions:

1. Associates a set of data bits in the shift registers with a character location on the screen
2. Signals the retrace control logic at the end of a row for horizontal retrace, and at the end of a frame for vertical retrace.
3. Provides timing signals for;
   a. Serializing the parallel data from the character generator onto the Z-axis.
   b. Initiating a Read or Write cycle requested from the computer.
   c. Erasing the screen.
   d. Entering data in the output data register.
   e. Clocking the shift register.
4. Selects the row of each character being brought out of the character generator.

Retrace control drives the logic for the X and Y amplifier inputs of the display unit and signals the Z-axis to turn off the electron beam during retrace. Memory stores the character code for each character location on the screen (even if it is a blank). Data from the memory drives the character generator which provides the dot matrix, one row at a time. This parallel data is converted and applied serially to the Z-axis. Communications input/output section accepts Read and Write requests from the computer, and enables the address and data bits into the Registers. It disables the recirculate input on the shift register when a write is required. Address Compare checks for equality between the data in the input address register and the counter address. When this equality is detected, one of several things can happen:

a. If the Write Request flip-flop has been set, Address Compare begins a Write cycle.

b. If the Read Request flip-flop has been set, Address Compare enables the data at this location into the Output Data Register.

c. In any case, Address Compare enables the cursor. If no equality is detected during a frame, and if there has been no computer request; the address in the Address Register is illegal and the screen is erased. Figure 9 shows the address map. The Cursor block generates a blinking cursor in row 2 (see Figure 6) of the character location in the Address Register.

COUNTER AND RETRACE CONTROL

A logic diagram of this board is shown in Figure 10. The counter is driven from an oscillator formed from two MC8602 one-shots in a single package. (1). The desirability of this type of oscillator will be discussed later in the memory section. The operating frequency is 5.0 MHz for a refresh rate of precisely 60 Hz. Because the counter is synchronous, the oscillator drives all the devices in the chain.

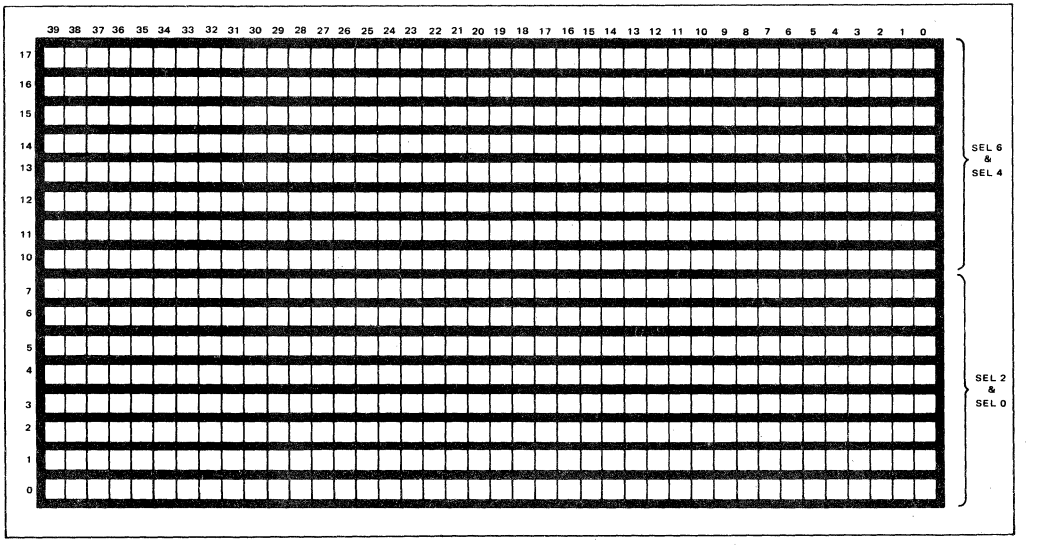


FIGURE 9

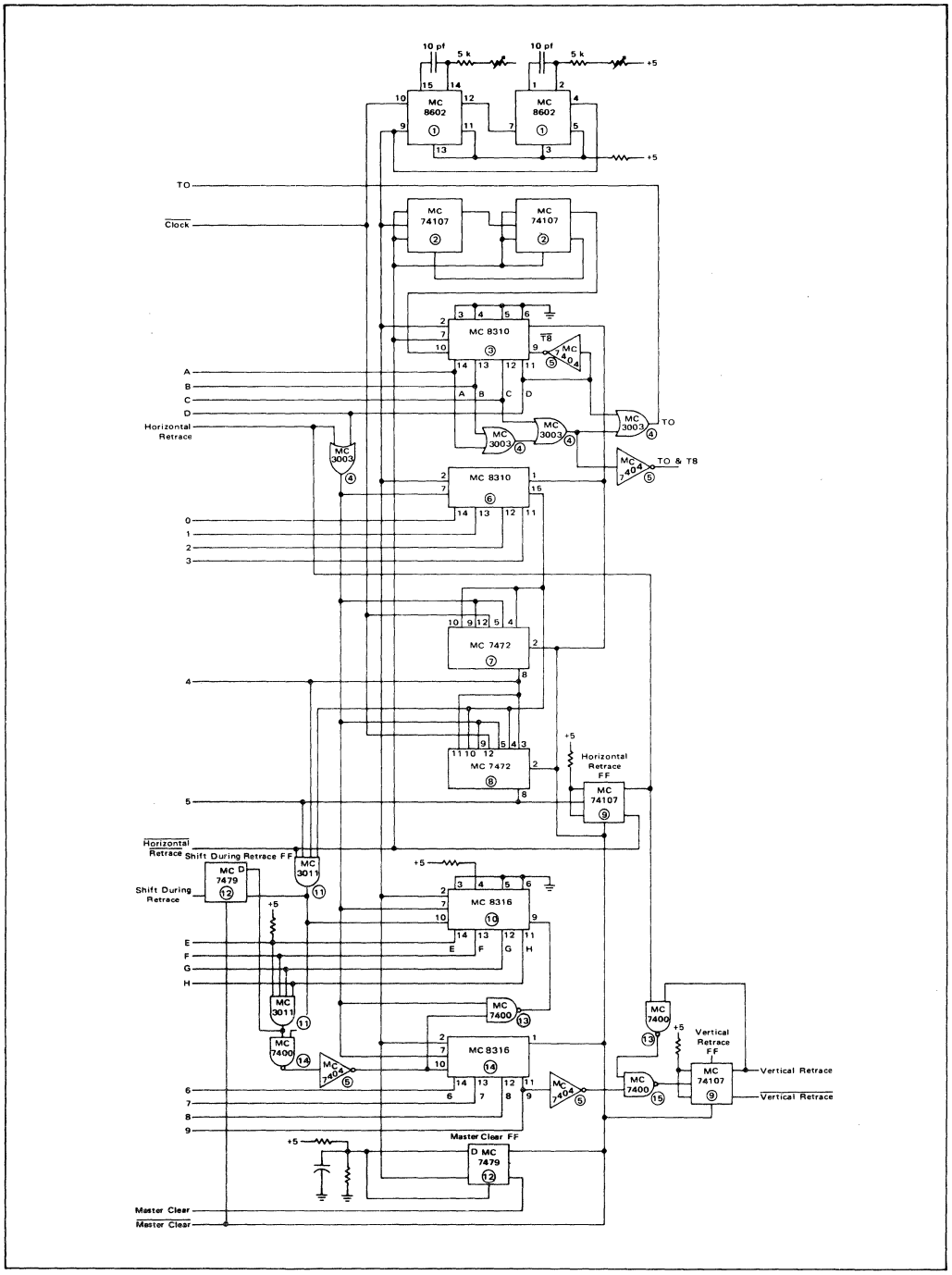

10 pf
5 k
+5
MC 8602
TO
Clock
MC 74107
MC 8310
T8
MC 3003
MC 7404
A
B
C
D
Horizontal Retrace
TO
TO & T8
0
1
2
3
4
5
MC 7472
Horizontal Retrace FF
Horizontal Retrace
Shift During Retrace FF
Shift During Retrace
MC D 7479
MC 8316
E
F
G
H
MC 7400
Vertical Retrace FF
Vertical Retrace
6
7
8
9
Master Clear FF
Master Clear

FIGURE 10

The first stage of the counter is an MC8310 (3) which has been connected to count decimally from 0 to 8. The dot matrix columns 1 through 7 are being written when the count in this register is 1 through 7. During counts 0 and 8, the Z-axis is blanked to form a space between horizontally adjacent characters. (4) and (5) are used to generate the time "T0", "$\overline{T8}$", and "T0 + (or) T8". In addition to the clock input, (3) is enabled by (2) and (9). The function of (2) is to delay the beginning of trace by two clock pulses. The necessity for this delay will be discussed later. Circuit (9) is the horizontal retrace flip-flop which enables this MC8310 (3) during the trace operation and disables it during retrace (see Figure 11). As mentioned earlier in order to write one line of characters the codes must be presented to the character generator once for each row of the dot matrix. In addition, the shift register must be shifted completely around between the beginning of one trace and the start of the next. The shift register is 80-bits long and the number of characters in a line is 40. Thus, the other 40 must be shifted during retrace; as will be explained later, this second set of 40 character codes is for the line following the first set of 40. Since the time for trace is nine times as long as the time for retrace, the second 40 bits must be shifted faster. To obtain this fast shift, (9) disables (3), effectively taking it out of the counter, and enables (6), which is the second stage of the counter, to be driven at the clock frequency. During trace, (6) is driven at the clock frequency divided by 9.

An MC8310 (6), and two MC7472's, (7) and (8), form a 6-bit counter stage to count decimally from 0 to 39. The count in this stage determines the horizontal character position on the screen. During retrace, this stage goes through its full count at the clock frequency and during trace, at the clock frequency divided by 9. At the end of each count the Horizontal Retrace flip-flop, (9), is toggled. Figure 12 shows the necessity of (2). During retrace the character codes are being shifted at a rate of

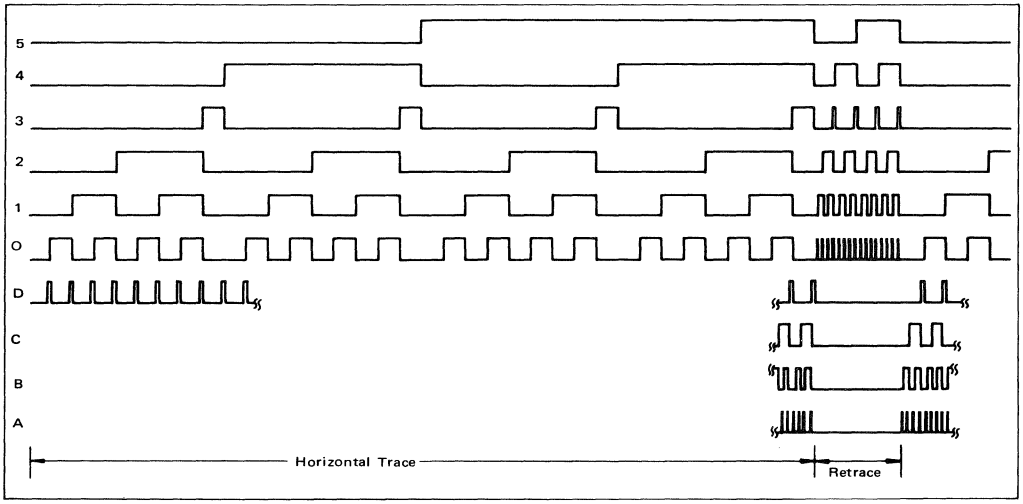


FIGURE 11

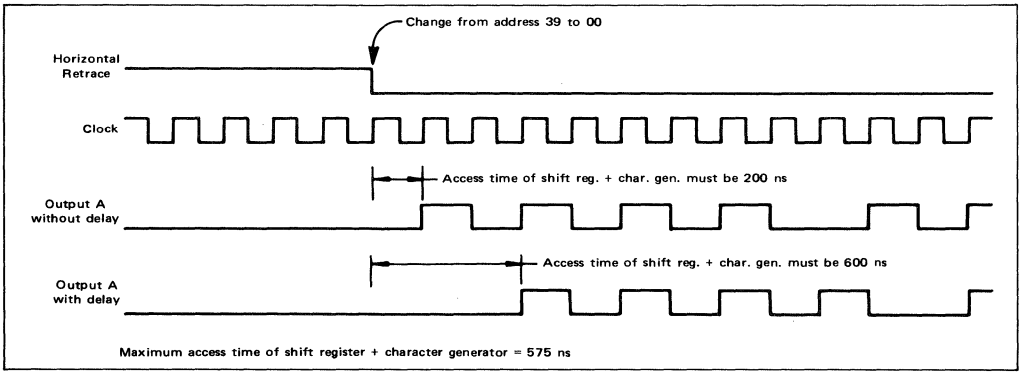


FIGURE 12

5.0 MHz; the maximum access time for the character generator and shift register is 500 + 75 = 575-ns. If there were no delay after the completion of retrace, the output for character location 0 would be required after 200-ns. By inserting a delay of two clock pulses this timing is increased to 600-ns.

The next stage of the counter is an MC8316, (10), a 4-bit counter which counts octally 2 to 16 (see Figure 10). The count in this device determines which dot matrix row is to be read out of the character generator. It is enabled when the count in the previous stage is completed and just before the Horizontal Retrace flip-flop (9) is set. This function is controlled by an MC3011 (11), that also serves as clock for the Shift During Retrace flip-flop, an MC7479 (12). As mentioned before, the data must normally be shifted during retrace. When one line of characters has just been completed and another is to begin, the shift must be inhibited. Thus, the Shift During Retrace flip-flop is clocked as each row is completed. If additional rows in the character line must still be written, the D input will be at logic "0" and the shift will be enabled. If the completion of the row is also the completion of the line (the count in (10) = 16), the D input will be a "1" and the flip-flop set, and this will inhibit Shift During Retrance. An MC3011, (11) decodes the count in (10) and drives the D input of (12).

The outputs of both gates of the MC3011 (11) are "ANDED" to form an enable for the last counter stage, MC8316 (14). It counts octally from 0 to 17. The count in this device determines the vertical character position or character line. At the end of the last count, the vertical retrace flip-flop is set. A vertical retrace takes the same amount of time as a horizontal retrace thus the Vertical Retrace flip-flop is reset by the Horizontal Retrace flip-flop. The Master Clear flip-flop initializes the system when power is first applied.

MEMORY SELECT

The Memory Select section (see Figure 13) forms the Shift Register Clock, and enables the Write and Output Enable inputs of the selected shift registers (MC6545). An MC4038 decodes the 3 highest order bits of the counter to generate an Output Enable. A set of MC3006 logic gates generates a Write Enable for the selected pair of shift registers when a Write cycle is being executed, and an Address Compare indicates that the desired location has been reached.

When the Horizontal Retrace flip-flop is reset, an MC3031 uses output C of the counter to clock data out of the shift registers. When the Horizontal Retrace flip-flop is set, and a Shift During Retrace is required, the counter clock is enabled by the MC3031 to form the Shift Register Clock. The MC3031 output goes to an MC7440 high fan-out driver which in turn drives the clock inputs of all 16 shift registers.

At this point, the desirability of the double one-shot oscillator for the counter clock becomes apparent. The Shift Register Clock is required to be in the high state for at least 90-ns and in the low state for at least-90ns. Since the counter clock runs at 5.0 MHz (200-ns), a duty cycle close to 50% at the shift register clock input is required. The counter clock pulses go through an MC3031 and an MC7440 before reaching the shift register clock input; thus, some skew in the positive and negative propagation times may occur. To compensate for this skew, the pulse widths of the two one-shots can be adjusted as required.

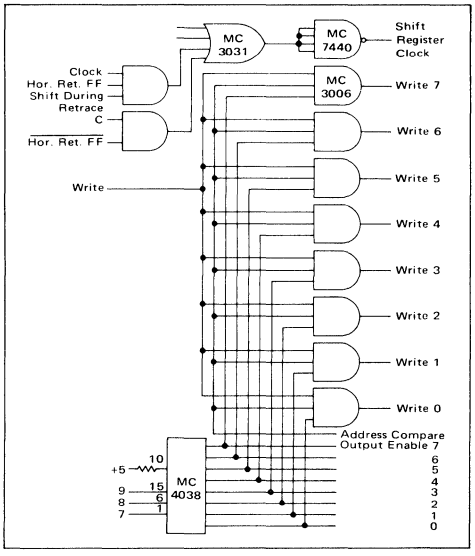


FIGURE 13

MEMORY

The Memory section (see Figure 14) consists of sixteen MC6545 shift registers arranged in pairs and 16 MC8T26 three-state buffers. Each pair holds 80 seven-bit character codes for two lines of display. The MC8T26 buffers are required so that only one pair of shift registers is being accessed at a time.

CHARACTER GENERATION

The output data from the shift registers goes to the Character Generation section (see Figure 15). If the system is in a Read cycle, the data is enabled into the Output Data Register made up of two MC7475's. In any case, the data goes to the character generator as does the row select count from the counter. The specified row for the character is read out of the character generator and stored in the Output Row Register at T0 + T8 time. The Output Row Register is applied to an 8-channel data selector, MC8312. This device selects each row input to be enabled to the single output according to the input count. This is supplied by the three lowest order bits of the counter. Thus, the parallel data is converted to serial data. At T0 and T8 times, the grounded input pin is enabled.

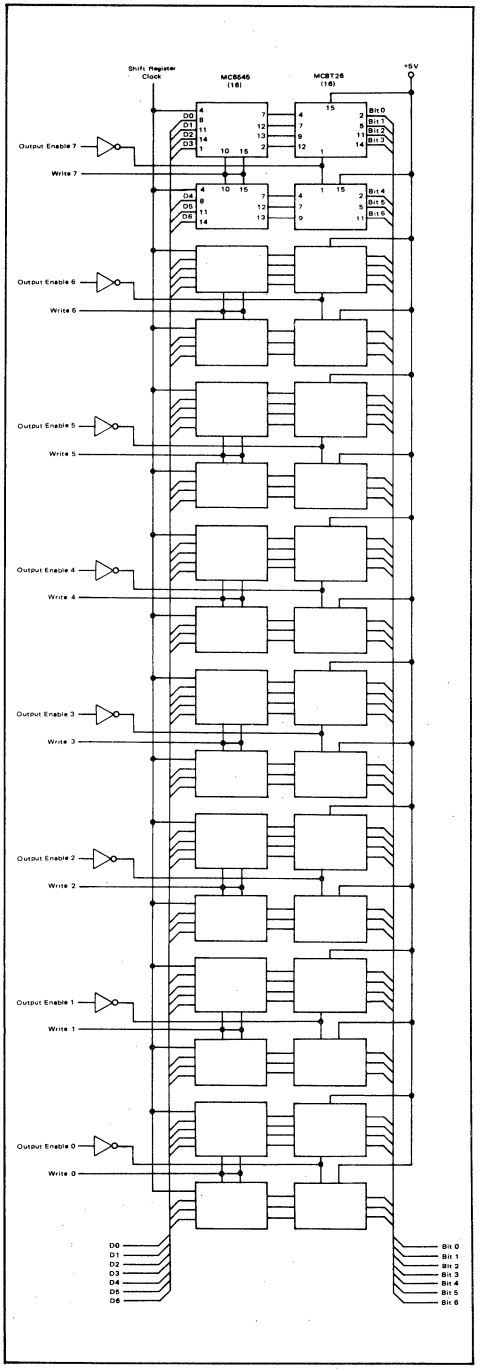


FIGURE 14

The MC8312 also has an enable input which is driven by the cursor generator to be described later.

The output of the MC8312 goes to the Z-axis driver which consists of 3 collector-or'ed MC7417's driving an output transistor. The Z-axis driver output goes to "0" during vertical and horizontal retrace and whenever the data input from the MC8312 is "0".

CRT DRIVE

The output drivers for the X and Y axes are shown in Figure 16. Each is driven by a cross-coupled gate/flip-flop, MC7400, which is, in turn, set and reset by two pulses tapped from the outputs of an MC7442 and MC4007. During retrace, these devices generate a series of timing pulses from the same counter bits that determine horizontal character location. Thus, retrace time can begin a short time after blanking begins, and it can end a short time before blanking ends. This method eliminates any distortion that might result from characters being displayed in the non-linear area of the raster edges.

COMMUNICATION I/O

The read/write logic is designed for use with a 16-bit bus-oriented minicomputer. The display system uses four addresses on the bus. A bus interface card generates four signals, $\overline{\text{SEL0}}$, $\overline{\text{SEL2}}$, $\overline{\text{SEL4}}$, and $\overline{\text{SEL6}}$, to indicate when these four addresses are selected. A control signal, C1L, indicates whether a bus-read or a bus-write cycle is being executed by the external control minicomputer. In order to respond to the minicomputer, the display system must generate two signals: 1) Ready, to indicate whether or not the system is busy doing an operation, and 2) SSYN, to indicate that a bus cycle is complete.

The four possible types of operations have been assigned as follows:

1) A bus write using either $\overline{\text{SEL2}}$ or $\overline{\text{SEL6}}$ is for writing data into the refresh memory. $\overline{\text{SEL2}}$ is for the bottom 8 lines of the display and $\overline{\text{SEL6}}$, the top 8 lines.

2) A bus write using either $\overline{\text{SEL0}}$ or $\overline{\text{SEL4}}$ is for specifying which location is to be read. $\overline{\text{SEL0}}$ indicates the bottom 8 lines of the display and $\overline{\text{SEL4}}$, the top 8 lines.

3) A bus read using either $\overline{\text{SEL2}}$ or $\overline{\text{SEL6}}$ is for determining the status of the Ready signal.

4) A bus read using either $\overline{\text{SEL0}}$ or $\overline{\text{SEL4}}$ is for retrieving the data requested in 2). For these operations, the 16-bit word of the minicomputer is divided into two sections. The seven least significant bits specify the character code, and the remaining nine specify the address.

The communications I/O logic is shown in Figure 17. A write operation is executed in the following manner (see Figure 18(a)):

1) Address and data are applied to the input lines of the CRT display system (Input Address and Data, and Cursor Generation are discussed in a later section). At the same time, C1L input goes to zero which enables the OR gate inputs to the Read and Write Request flip-flops.

2) A minimum of 150-ns later, $\overline{SEL2}$ or $\overline{SEL6}$ goes to zero which sets the Write Request flip-flop. In turn, it sets the SSYN flip-flop. Ready goes to zero, and the input address and data are enabled into the Registers.

3) The SSYN is transmitted back to the minicomputer which waits 75-ns and then changes $\overline{SELX}$ back to a one.

4) The SSYN flip-flop is reset and the SSYN signal goes to a zero.

5) When the Address Compare signal goes to a "1", indicating that the address register and the counter

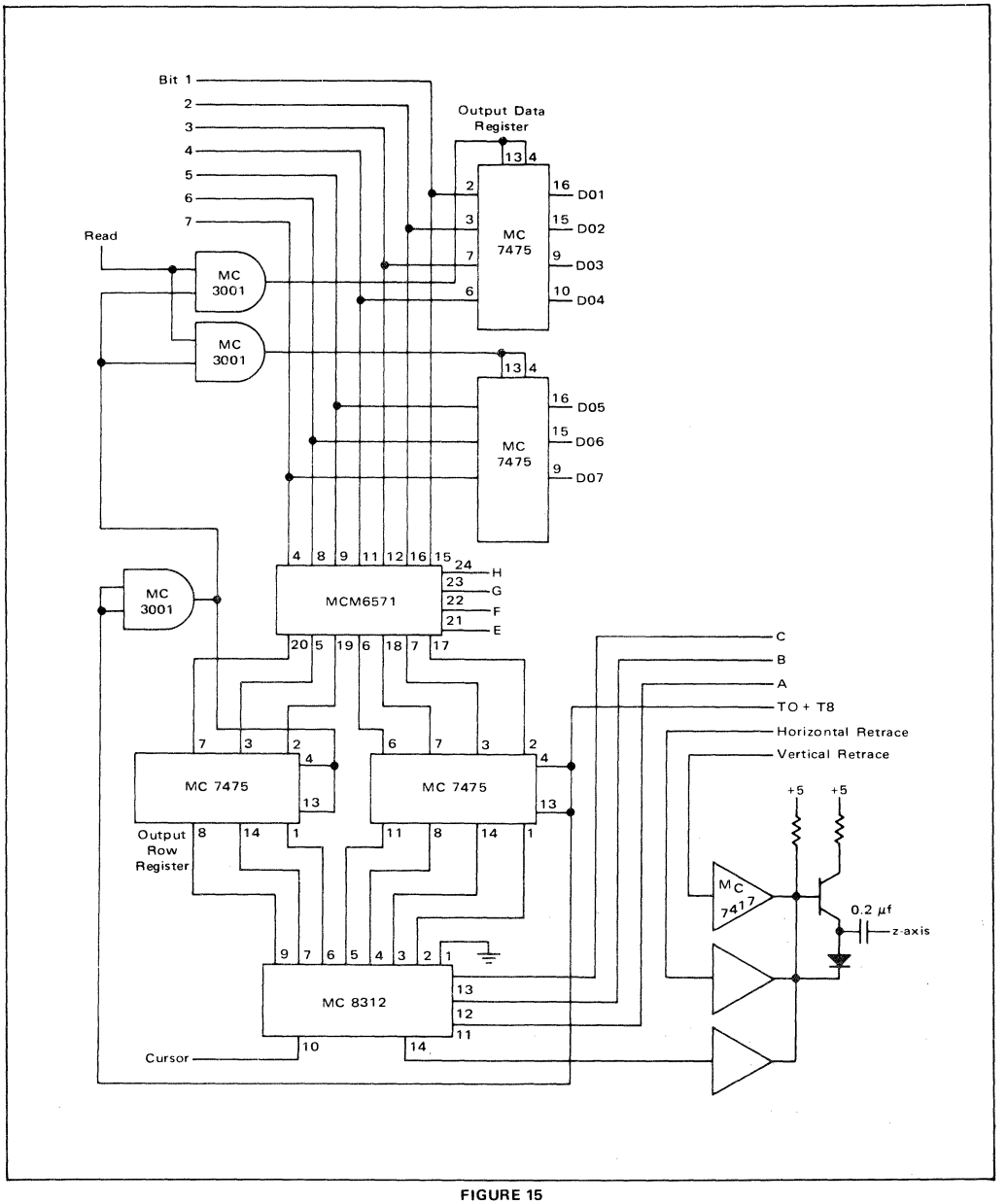


FIGURE 15

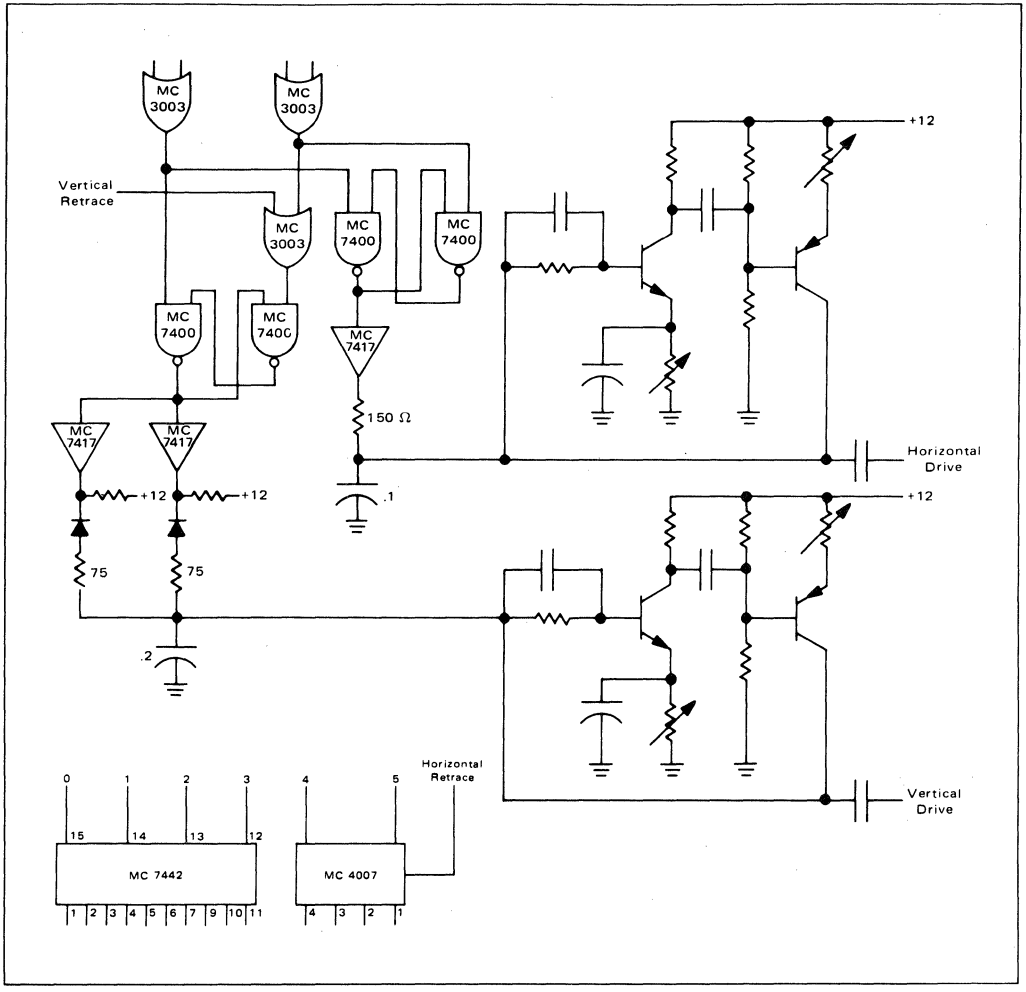


FIGURE 16

contain the same address, the Write Request is clocked into the Write flip-flop. This flip-flop enables the necessary logic to write the new data into memory. The Write flip-flop is set directly when an erase is being executed.

6) At the next T8 to T0 times respectively, the Write Request and Write flip-flops are reset and Ready goes to a "1". The system can now accept a new request.

A read operation (for specifying the location to be read) is done in a similar manner except the $\overline{\text{SEL0}}$ or $\overline{\text{SEL4}}$ are used.

To transfer data from the Output Data Register (see Figure 15) to the minicomputer or to check the status of the CRT system, the following sequence occurs (see Figure 18(b)):

1. C1L goes to a one.
2. A minimum of 150-ns later, one of the $\overline{\text{SELX}}$ signals goes to a zero.
3. The SSYN signal goes to a one for at least 75-ns.
4. The $\overline{\text{SELX}}$ signal returns to a one and SSYN goes to a zero.

INPUT ADDRESS AND DATA

The Address Register consists of two MC4015's and a MC7479 (see Figure 19). The input address is enabled into the register when the Read Request or Write Request flip-flop is set. The input to bit 9 of the Address Register is dependent on the $\overline{\text{SELX}}$ input. If $\overline{\text{SEL0}}$ or $\overline{\text{SEL2}}$ is used, a zero is entered into bit 9 which means the bottom 8 lines of the display will be accessed. If $\overline{\text{SEL4}}$ or $\overline{\text{SEL6}}$ is

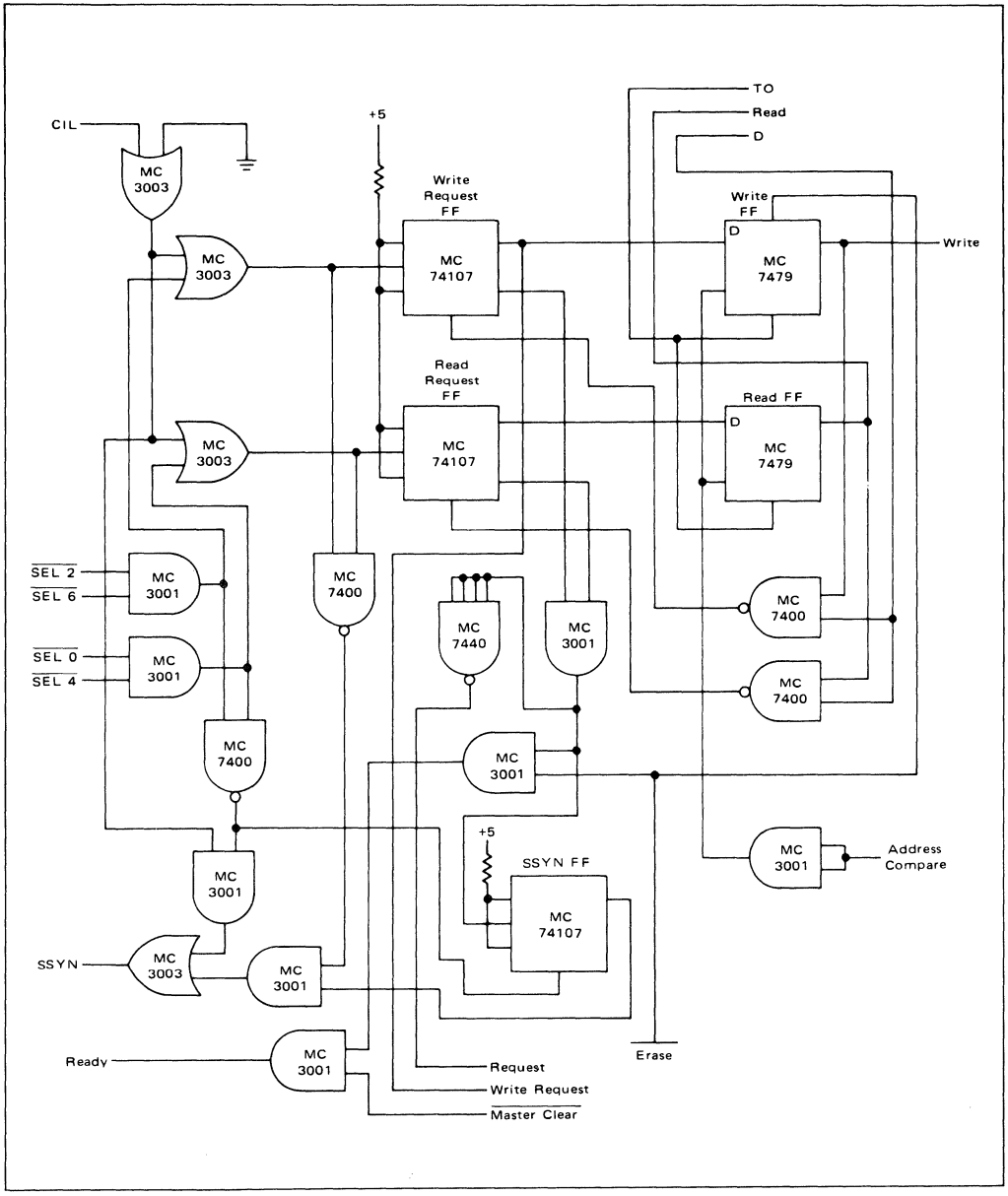


FIGURE 17

used, a one is entered into bit 9 and the top 8 lines will be accessed.

Ten MC8242 exclusive NOR gates are constantly comparing the input and counter addresses. They are open collector output devices; therefore, when they all indicate a compare, the output goes to a "1". The Address Compare flip-flop is set at the first positive edge of the B output of the counter. If a read or a write has been requested, it can be done at this time. Also the Address Compare flip-flop enables the cursor row compare logic and inhibits an Erase.

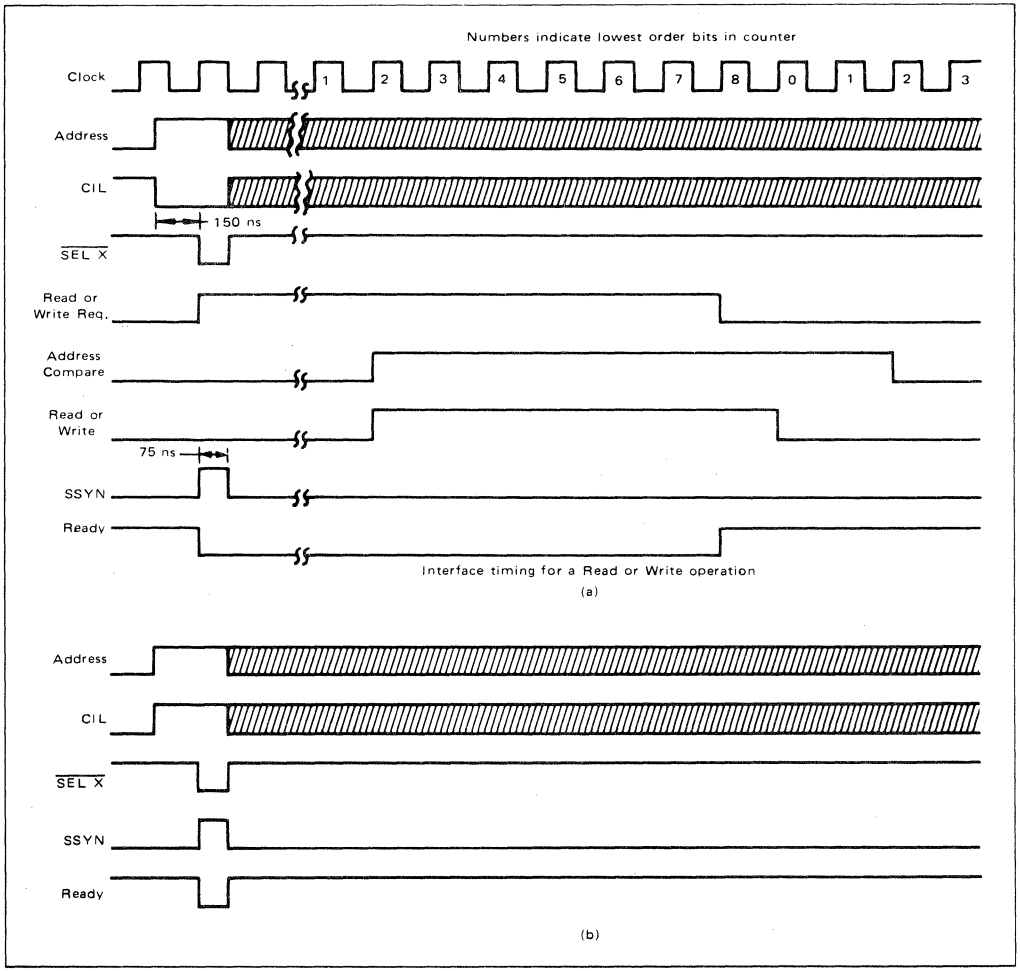


FIGURE 18

When Address Compare or a Read or Write Request goes from "0" to "1", the Erase Inhibit flip-flop is set. After each frame is written, the $\overline{Q}$ side of the Erase Inhibit flip-flop is clocked into the Erase flip-flop. As long as the latter stays reset, nothing happens. An illegal address can be entered into the Address Register however (an illegal address would be when the 4 lowest order bits of the Address Register contain a decimal number between 10 and 16). Since the counter does not duplicate the illegal address, the Address Compare flip-flop and, consequently, the Erase Inhibit flip-flop do not switch. At the end of the frame, then, the Erase flip-flop is set.

Setting the Erase flip-flop forces:

1. The input data to the shift registers to the character code for a blank.
2. The Address and Input Data Registers to all 0's.
3. The Erase Inhibit, Address Compare, and Write flip-flop's set.

This clears the screen of all data and moves the cursor location to address 0.

CURSOR GENERATION

The cursor is written at the location in the Address Register. It is written in row 2 of the dot matrix (see Figure 6). Four MC7405's are collector OR'ed (see Figure 20) to output a "1" each time that row select 2 and address compare exist at the same time. An MC7490 then divides the frequency of this output by five to make the cursor blink. The output of the MC7405's and the MC7490 are "ANDED" and, as mentioned earlier, the signal is used to drive the enable input of the parallel to serial converter for the Z-axis, MC8312.

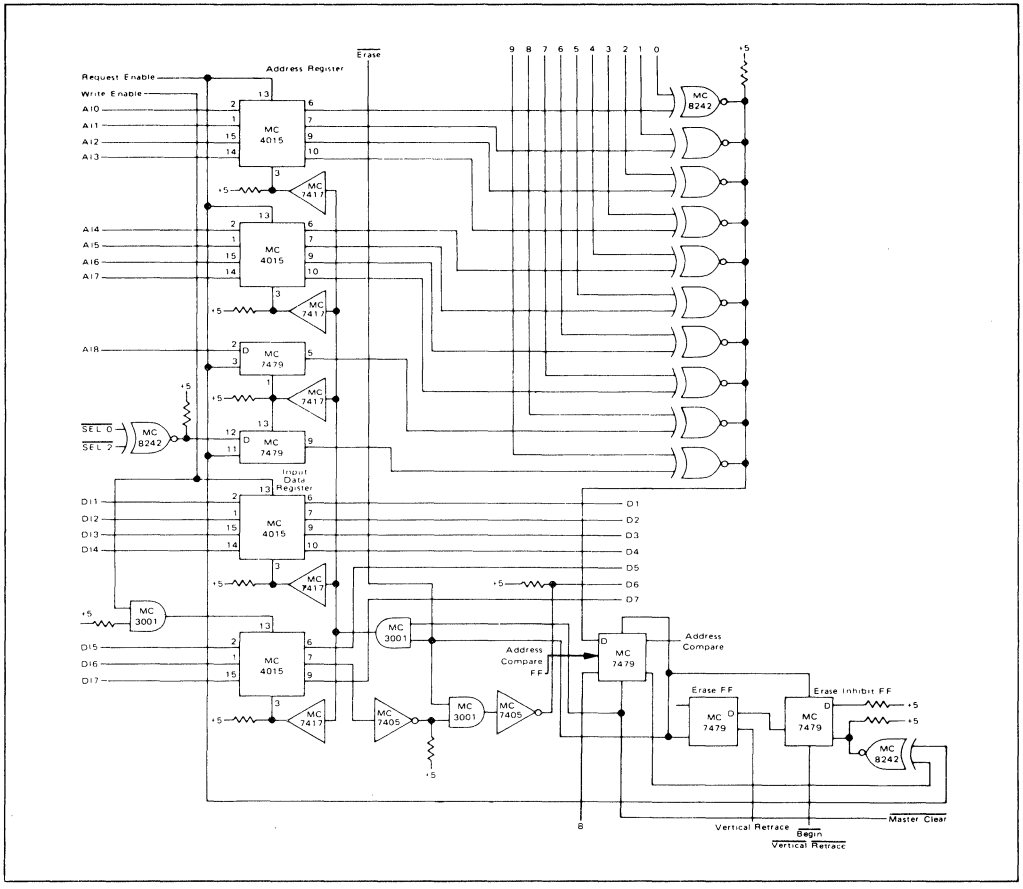


FIGURE 19

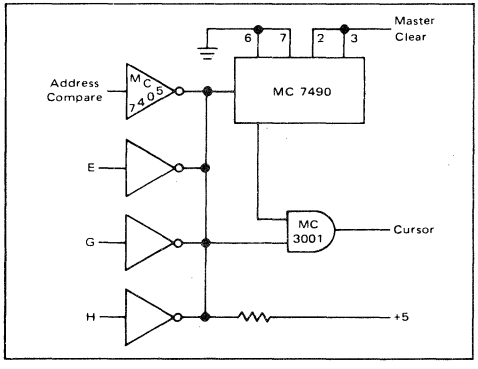


FIGURE 20

CONCLUSION

This system design shows one way of using the new NMOS devices in CRT systems for both storage and character generation. The simplicity of the design is possible because of the TTL compatibility and convenient power requirements of the NMOS parts. The capability of generating 128 characters in a 7 x 9 matrix and automatically shifting descender characters (g, j, p, q, and y) means a substantial reduction in external circuitry. The MC6545 Quad 80-bit Shift Register allows maximum design flexibility with features like a 3-state output, internal recirculate logic, a single clock input, and a frequency range of D.C. of 5 MHz. It will fit into small systems as a main storage device and into large systems as buffer storage. With these devices, NMOS has indeed arrived for the CRT display manufacturers.

A NON-VOLATILE MICROPROCESSOR MEMORY USING 4K N-CHANNEL MOS RAMS

INTRODUCTION

Most read/write semiconductor memories are volatile, i.e., if power is removed from the memory the stored information will be lost. In many cases of power failure, non-volatility for a specific period of time is required either as a necessity (irreplaceable information) or as a convenience (to avoid reloading the memory).

This paper describes the design of an 8192-byte non-volatile memory system using dynamic RAMs and CMOS control logic in order to significantly reduce the power requirement in the standby mode of operation with respect to the normal operating mode.

This system was designed to be an add-on memory for the EXORciser,* a system development tool in the M6800 Microcomputer family.

MEMORY DEVICE DESCRIPTION

The memory device used in this system is the MCM6605A, a 4096-word x 1-bit dynamic Random Access Memory (RAM). The dynamic characteristic of this memory device requires that refreshing of the memory cells be performed at periodic intervals in order to retain the stored data. This device was chosen for the following features: high bit density per chip and correspondingly low price per bit, standby mode with low power dissipation, TTL compatibility of inputs and outputs, and speed characteristics compatible with microprocessors and the EXORciser.

Figure 1 is a functional block diagram of the MCM-6605A. The device uses a three-transistor storage cell in an inverting cell configuration. The single external high-level Chip Enable clock starts an internal three-phase clock generator which controls data handling and routing on the memory chip. The lower 5 address lines (A0 to A4) control the decoding of the 32 columns, and the upper 7 address lines control the decoding of the 128 rows within the memory chip. The Chip Select ($\overline{CS}$) input is used for memory expansion and controls the I/O buffers: when $\overline{CS}$ is low the data input and output are connected to the memory data cells, and when $\overline{CS}$ is high the data input is disconnected and the data output is in the high impedance state. Refreshing is required every 2 ms and is accomplished by performing a write cycle with $\overline{CS}$ high on all 32 columns selected by A0 through A4. The read/write line controls the generation of the internal $\phi 3$ signal which transfers data from the bit sense lines into storage.

All inputs and outputs with the exception of the high-level Chip Enable signal are TTL compatible, and the outputs feature three-state operation to facilitate wired-OR operation. The Chip Enable signal has ground and +12 V logic levels. Power requirements are typically 330 mW per device in the active mode from +12 V, +5 V, and -5 V power supplies, and 2.6 mW in standby with refresh from the +12 V and -5 V power supplies (the +5 V supply powers the output buffers and is not required during standby operation).

Memory timing is outlined in Figure 2 and operates as follows for a read cycle (Figure 2a). The Chip Enable line is brought high after the correct addresses are set up, which starts the internal three-phase clock and latches the addresses into an internal register. Chip Select must be brought low in order to connect the data input and output to the data cells, and the Read/Write line must be brought high to inhibit the $\phi 3$ cycle which writes data into the storage cells. A write cycle (Figure 2b) occurs in exactly the same manner as a read cycle except that the R/W line is placed in the Write mode, which gates the input data onto the bit sense lines, and enables a $\phi 3$ cycle to write into the data cells. A write and a refresh cycle are the same with the exception of Chip Select, which is held high for a refresh cycle and low for a write cycle.

The Read-Modify-Write cycle shown in Figure 2c is a read followed by a write within the same CE cycle. $\overline{CS}$ is brought low shortly after the leading edge of CE and R/W is held high long enough for the Data Out to become valid. The R/W line can then be strobed low for a minimum write time to enter the Data In (which has been placed on the input) into the data cells.

By holding the Chip Select high during refresh, the input data is inhibited from modifying the bit sense lines and the original data is returned to the data cells during $\phi 3$ of the cycle. This refreshing action recharges the storage cells and must be done at least every 2 ms if the memory is to retain the information. The fact that the data is stored on a capacitor in a dynamic memory (rather than the "On" transistor of a static memory) requires that the capacitor be recharged periodically. This capacitive storage produces a low power standby mode of operation where only refreshing takes place, which is the foundation of this low current drain non-volatile memory design. The memory

*Trademark of Motorola Inc.

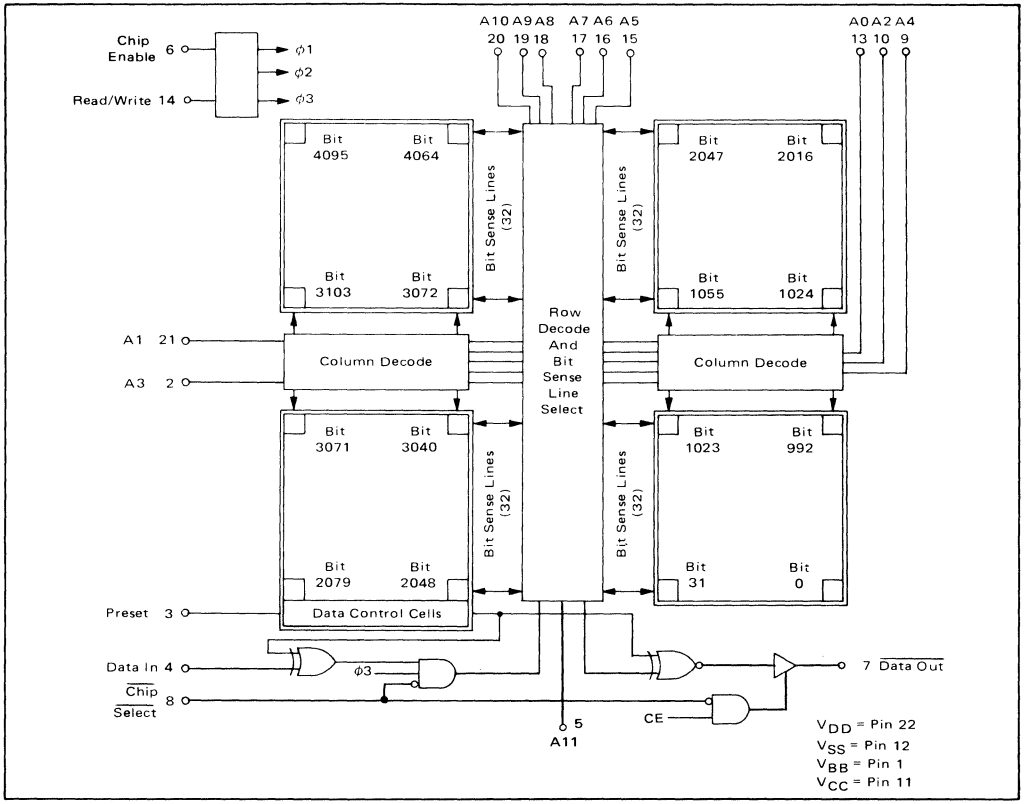


FIGURE 1 — MCM6605A 4K RAM Block Diagram

device typically dissipates 330 mW in the active mode but only 2.6 mW in the standby mode (refreshing only).

MEMORY SYSTEM DESIGN REQUIREMENTS

This memory system was designed with the following major design goals:

First, non-volatility for a period of time in the range of 7 to 10 days from a reasonably sized battery. It is also desirable for the system to operate from one battery voltage during the standby mode to simplify the battery requirements. Second, the memory size was desired to be 8K bytes on a PC card easily expandable upward and addressable in 4K byte blocks. Third, the memory system must be able to interface with the MC6800 microprocessor which has a basic cycle time of 1 μs. Fourth, the memory system controller must handle all refresh requirements in a manner as invisible as possible to microprocessor operation.

MEMORY SYSTEM DESCRIPTION

A block diagram of the memory system is detailed in Figure 3. This block diagram can be split into three main sections as follows. The first section is comprised of the address buffers, Read/Write and Chip Select decoding logic. The second section consists of the data bus buffering and the memory array itself. The memory array consists of sixteen memory devices (4K words x 1-bit) organized into two rows of 4096 bytes each. The third section of the block diagram comprises the refresh and control logic for the memory system. This logic handles the timing of the refresh handshaking with the EXORciser to request a refresh cycle, the generation of the refresh addresses, synchronization of the $\overline{\text{Power Fail}}$ signal, multiplexing of the external Memory Clock with the internal clock (used during standby), and generation of the -5 V supply on the board by a charge pump method.

Figure 4 is a worst case timing diagram of the read and write cycles of the EXORciser and the 4K memory system. The timing is composed of two phases. During phase 1 ($\phi 1$) addresses are set up and during phase 2 ($\phi 2$) data is transferred. Figure 5 is a timing diagram of the memory system in standby showing refresh cycles only. This timing analysis will be referred to in the following discussions of the memory control circuitry.

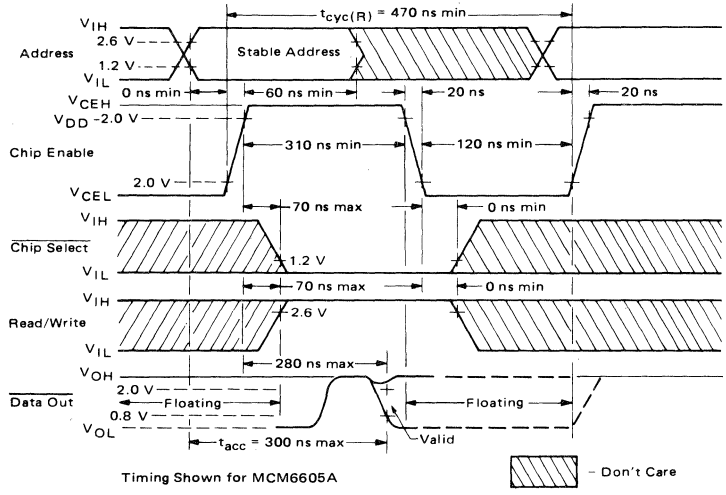


FIGURE 2a – Read Cycle Timing (Minimum Cycle)

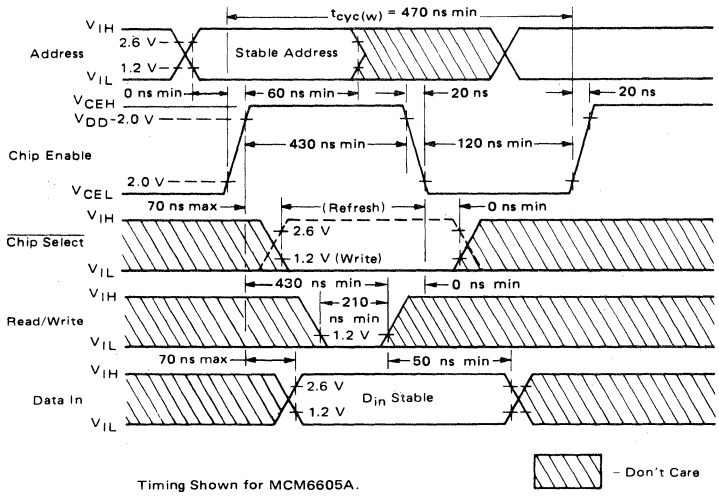


FIGURE 2b – Write and Refresh Cycle Timing (Minimum Cycle)

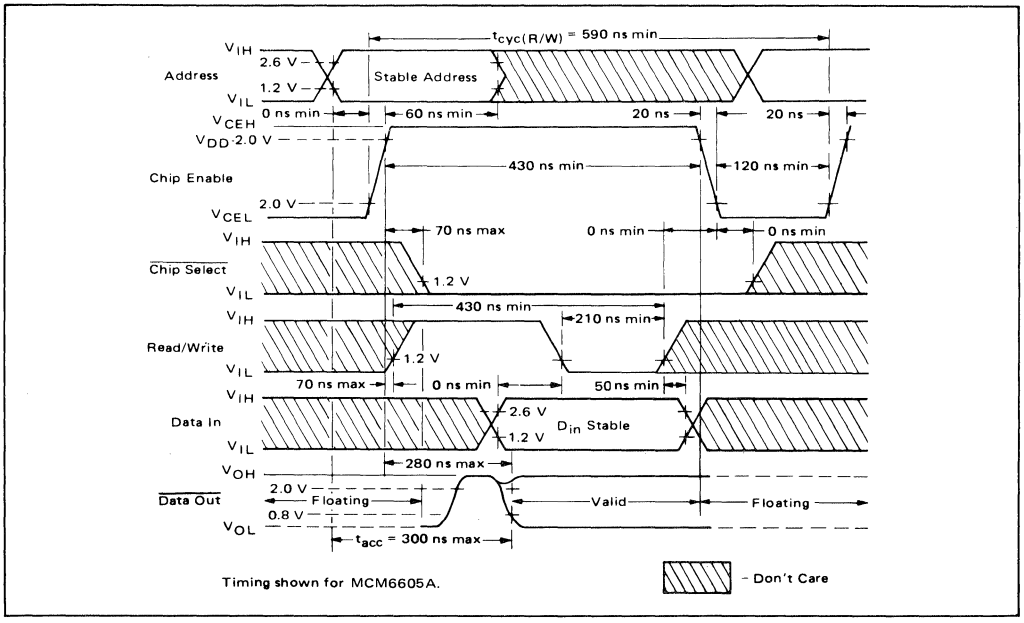


FIGURE 2c – Read-Modify-Write Timing (Minimum Cycle)

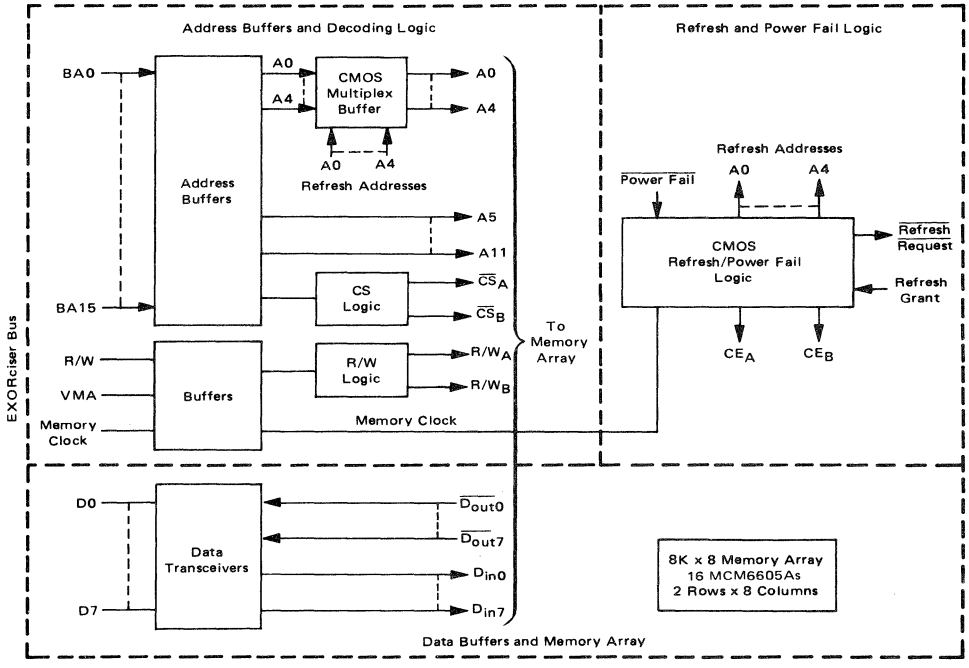


FIGURE 3 – Non-Volatile Memory System Block Diagram

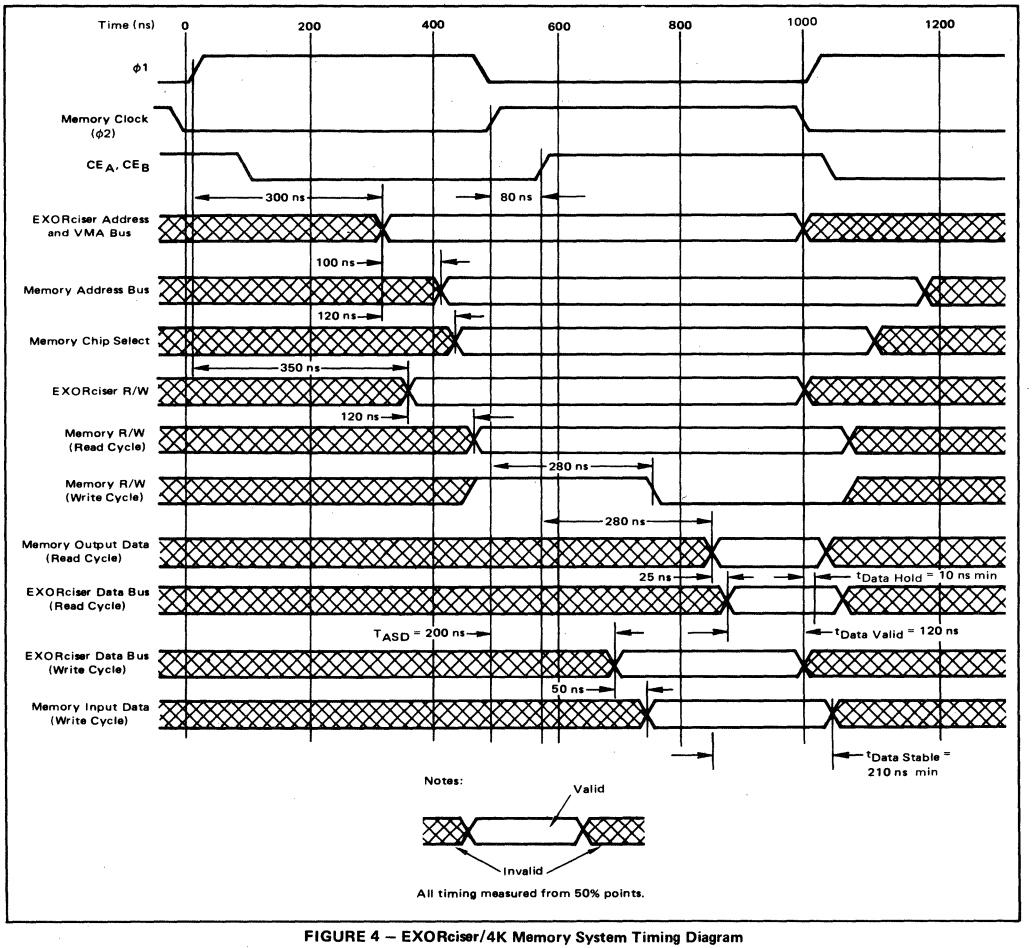


FIGURE 4 – EXORciser/4K Memory System Timing Diagram

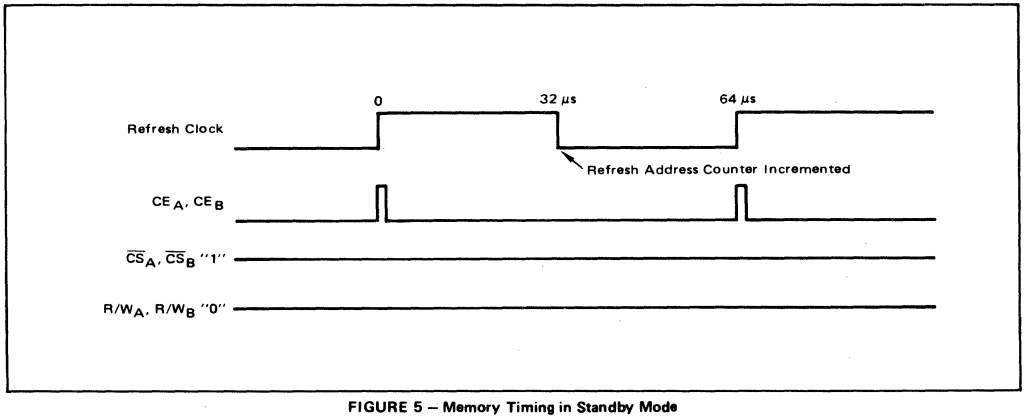


FIGURE 5 – Memory Timing in Standby Mode

ADDRESS BUFFERS AND DECODING

Figure 6 is a logic diagram of the address buffers, decoding logic and refresh address multiplexer. Address and data lines from the EXORciser are buffered from the capacitance of the memory array in order to provide a small load to the bus. This increases the EXORciser flexibility because it can easily be expanded. Since the addresses are valid on the EXORciser bus 300 ns into $\phi 1$, 200 ns is available to set up the address on the memories. The worst case input capacitance on the address lines of the MCM6605A is 5 pF/input. A system of 16 memory devices (8K bytes) presents a total capacitive load on the address lines of only 100 pF (20 pF stray capacitance). Since 200 ns is available to set up the addresses on the memory devices, no high current buffers are required to drive the memories. A0 through A4 must be multiplexed with the refresh addresses so that all 32 columns will be refreshed every 2 ms. Because of the requirement of low current drain in the standby mode, an MC14503* CMOS buffer with a three-state output is used to meet the multiplexing requirement. The buffers have sufficient current drive capability to drive the address line capacitance within 100 ns. An open collector TTL gate is used to translate to +12 V CMOS levels. A0 through A11 are driven with Ground and 12 V logic levels so that +5 V is not required in the standby mode. A5 through A11 are clamped to Ground during a refresh cycle so that they will remain stable.

The high order address lines (A12 through A15) are used to decode one 4K block of memory out of the 16 total possible blocks in the 65K address map. The addresses and their complements are routed through hexadecimal switches to MC7430 NAND gates in order to create a $\overline{CS}$ signal for each 4K byte of memory. By rotating the hexadecimal switches (S3 and S4), all combinations of true and complement addresses can be routed to the NAND gates, thereby selecting one of the sixteen 4K blocks. VMA and $\overline{REF}_A$ are also inputs to these NAND gates: VMA is a Valid Memory Address signal on the bus indicating that the address lines are valid and $\overline{REF}_A$ is a control signal indicating that a refresh cycle is taking place. During a refresh cycle, $\overline{REF}_A$ goes low forcing $\overline{CS}_A$ and $\overline{CS}_B$ high (a refresh cycle for the memory devices is a write cycle with the $\overline{\text{Chip Select}}$ held high). The output of the MC7430 is translated to 12-V CMOS levels with the open collector gates and buffered with the MC14503 three-state buffer. The capacitive loading on each set of three paralleled drivers is 60 pF, allowing $\overline{\text{Chip Select}}$ to be decoded and valid 120 ns after addresses are valid on the data bus. During the standby mode (Bat = "1") the CMOS buffer is disabled allowing the 3.3 k ohm resistors to pull $\overline{CS}_A$ and $\overline{CS}_B$ high for continuous refreshing.

The Read/Write signal is received by an MC8T26** and then decoded in the following manner: A write inhibit feature is provided using switches S1 and S2 for each 4K byte block of memory so that in a ROM simultation application the memory can be protected from extraneous write operations due to programming or operator errors. The Ready-Modify-Write cycle of the MCM6605A is used in this application because it requires a shorter data valid time ($t_{\text{Data Stable}}$) than a normal write cycle (see Figures 2b and 2c). This feature is desirable because the EXORciser places valid data on the bus for the last 300 ns of a Write cycle. In order to delay the write pulse to the memory array until the data is valid on the Data Inputs of the memory array, a write inhibit pulse is combined with the EXORciser R/W signal in the MC7420 NAND gates. This write inhibit pulse is generated by the MC8602 monostable multivibrator triggered from the leading edge of the Memory Clock bus signal. The effect of this added delay can be seen from Figure 4 when comparing the memory array R/W line for a read and a write cycle. Note that for a write cycle, the R/W of the memory array is inhibited from dropping to the Write mode until memory input data is valid.

The refresh control signal ($\overline{REF}_A$) is combined with the output of the MC7420 in an MC7408 AND gate in order to force a write signal on the memory R/W lines while in a refresh cycle. Translation and buffering is accomplished in a similar manner as with the Chip Select signals. When in the standby mode (Bat = "1") the MC14503 buffers are disabled allowing the 3.3 k resistor to establish a zero level on the R/W line of the memory array for continuous refreshing.

DATA BUFFERS AND MEMORY ARRAY

The EXORciser data bus is bidirectional, while the MCM6605A memory has separate data inputs and outputs. The MC8T26 data bus receiver/driver buffers the capacitance of the memory array (very low, about 30 pF per data line) and combines the Data Input and $\overline{\text{Data Output}}$ of the memory array into one bidirectional bus as shown in Figure 7. The $\overline{\text{Data Out}}$ of the memory devices is inverted from the Data In, requiring an extra inverter (MC7404) in the data path when working with a non-inverting bus (i.e., the data is returned to the bus in the same sense it was received).

During a memory write cycle, the data is valid on the data bus 200 ns (T_{ASD}) after the leading edge of the Memory Clock. With a 50 ns delay through the bus translators, the data setup requirement of the memories (210 ns) is easily met (see Figure 4). A memory read cycle requires a data setup time on the data bus of 120 ns. The access time of the memory from the leading edge of the CE signal plus the bus transceiver delay is 305 ns, which is compatible with the setup time required.

REFRESH AND CONTROL LOGIC

The refresh control logic shown in Figure 8 handles the refreshing of the memory during both operating and standby modes. The timing is shown in Figure 9.

The refresh timing is controlled by an astable multivibrator constructed with an MC3302 comparator. This

* MC14503 to be introduced-replacement for MM80C97.
**MC8T26 to be introduced-replacement for N8T26.

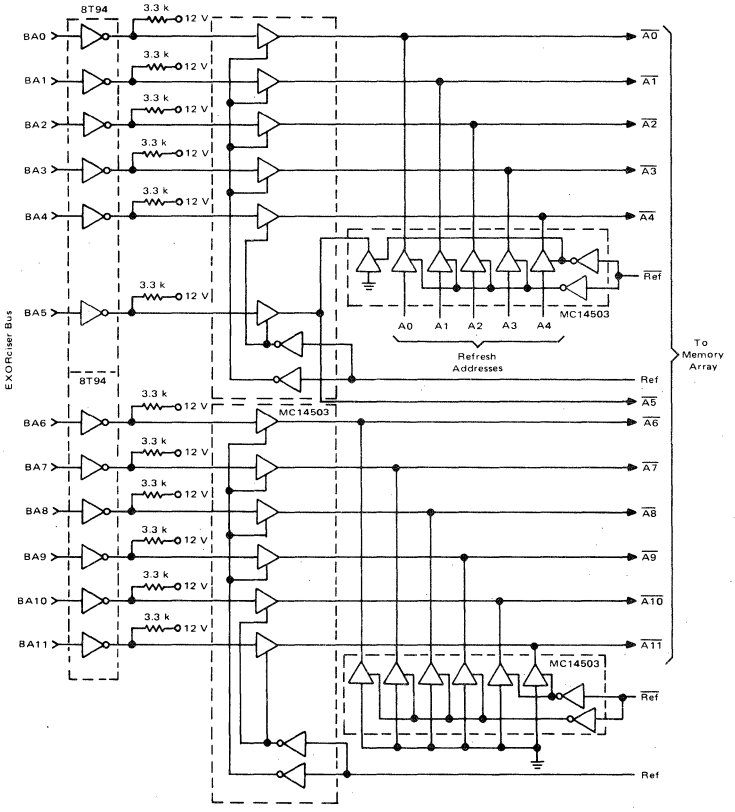


FIGURE 6 – Address Buffers and Decoding Logic

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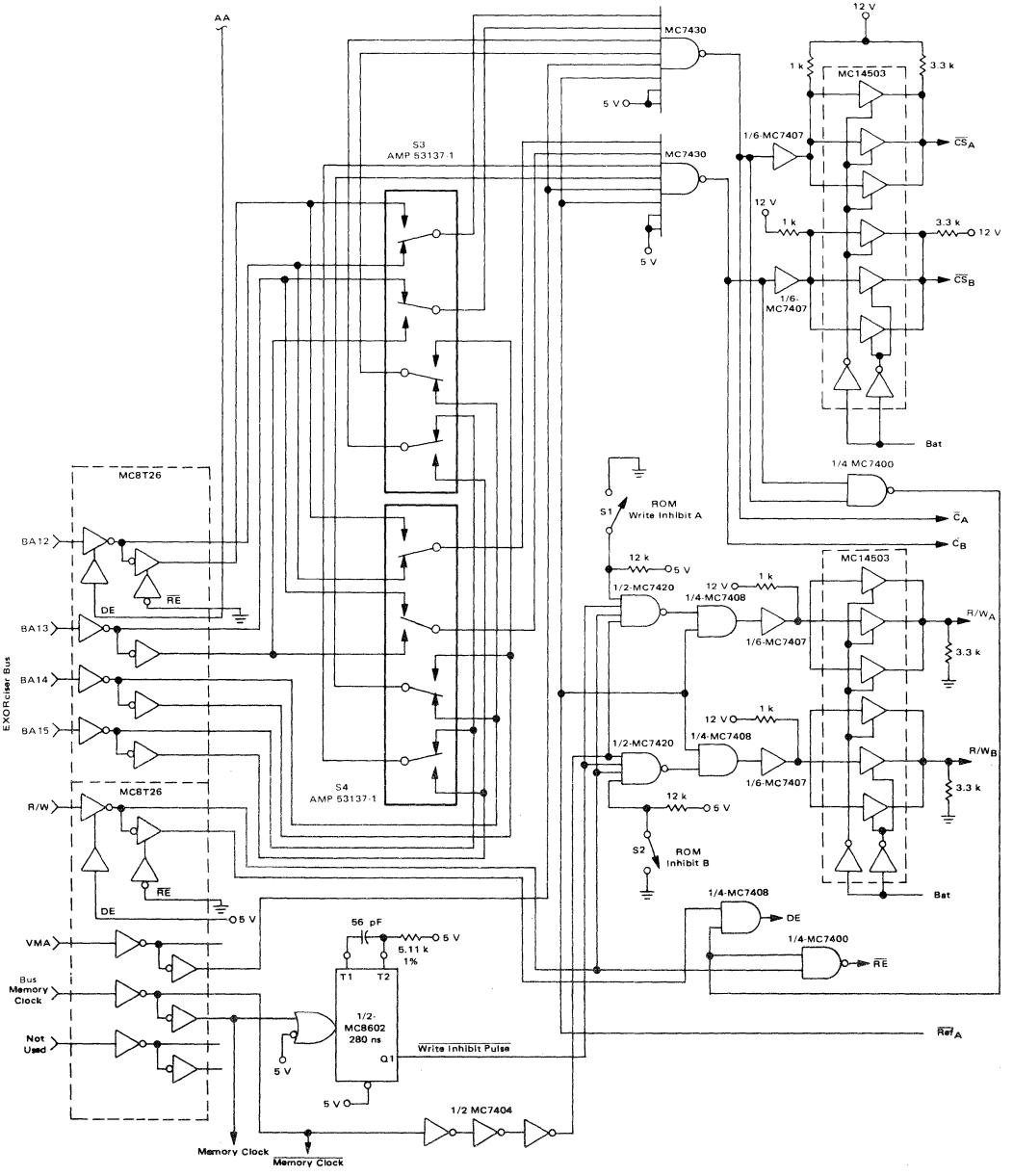

FIGURE 6 – Address Buffers and Decoding Logic
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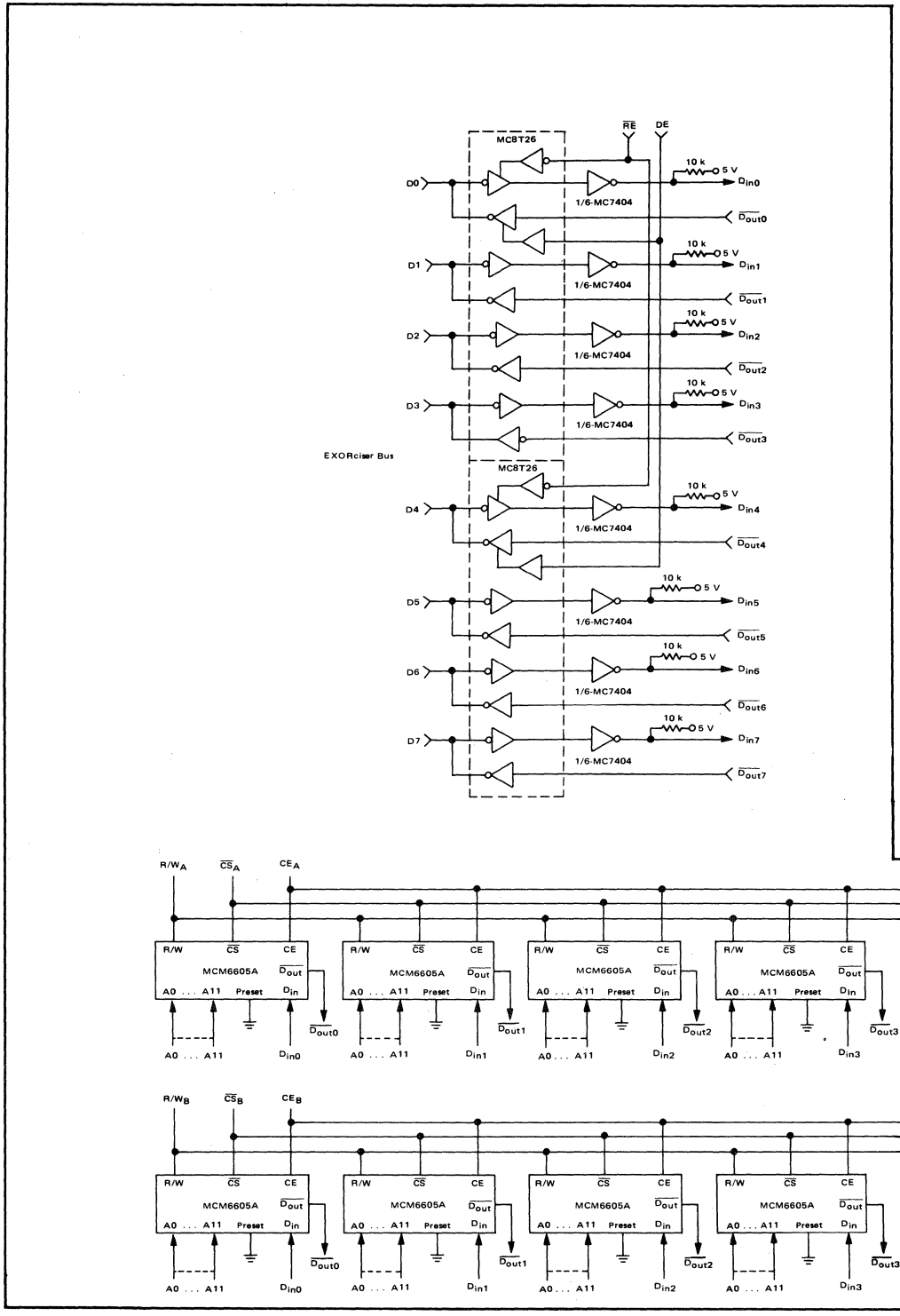


FIGURE 7 – Data Buffers and Memory Array

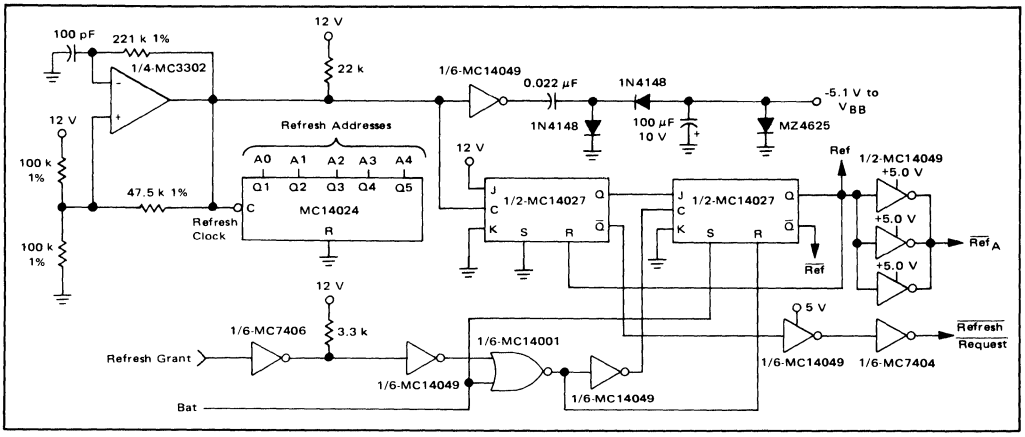


FIGURE 8 – Refresh Control Logic

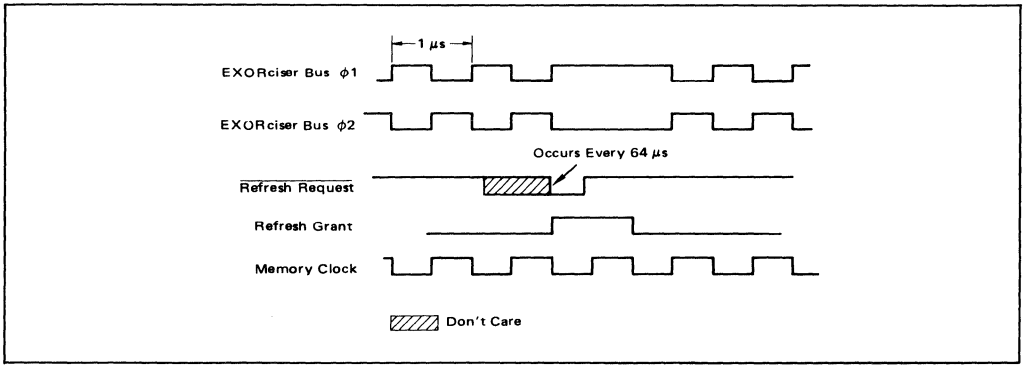
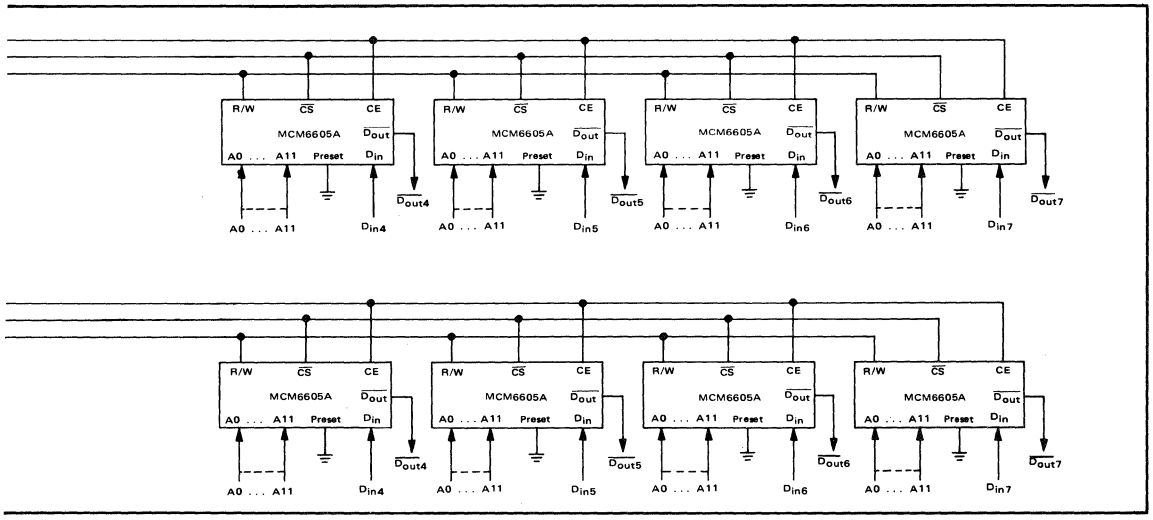


FIGURE 9 – Refresh Timing



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device was chosen for its low current consumption (1.5 mA max) and single supply voltage operation, both important for battery operation. The refresh requirement of 32 refresh cycles every 2 ms is handled by stealing cycles from the processor. This cycle stealing results in a 1.6% slower program execution rate than the basic microprocessor clock frequency. During the refresh cycle, the clocks to the microprocessor are "stretched" during the $\phi 1$ high and the $\phi 2$ low times by 1 μs as shown in Figure 9. During this 1 μs period, the memory executes a refresh cycle. In order to minimize the effects of memory refresh on microprocessor program execution, the 32 refresh cycles are distributed over the 2 ms period, one occuring every 64 μs. Refresh could be done in a burst of 32 cycles every 2 ms but this would cause a larger gap in program execution, which in this case was undesirable.

The MC3302 produces the 64 μs signal shown in Figure 5 to time the refresh requirement, and also is used in the generation of the -5 V supply required by the MCM6605 memory. Since these functions are required in the standby mode, which is powered by the battery, a CMOS buffer is used in a charge pump circuit to minimize current drain from the battery. This charge pump creates -5 V at 3 mA from the 12-V battery to satisfy the bias requirements of the memory devices.

The Refresh Clock is used to increment the address counter (MC14024) and to clock the refresh handshaking logic (MC14027). $\overline{\text{Refresh Request}}$ goes low on the leading edge of the Refresh Clock, thus requesting a refresh cycle. Logic in the clock generation circuitry stretches the high portion of $\phi 1$ and the low portion of $\phi 2$ while sending back a Refresh Grant signal. This stretching of the $\phi 1$ signal delays program execution during this cycle. The leading edge of $\overline{\text{Refresh Grant}}$ starts the refresh cycle and cancels $\overline{\text{Refresh Request}}$. The trailing edge of Refresh Grant returns the refresh logic to the normal state and the memory is ready for a memory access. The trailing edge of the Refresh Clock then increments the refresh address counter in preparation for the next refresh cycle.

Decoding of the memory clock (CE_A and CE_B) and the circuitry to synchronize the $\overline{\text{Power Fail}}$ signal is shown in Figure 10, with the timing given in Figure 11.

The memory device clock (CE_A and CE_B) during standby is created by a monostable multivibrator (MC14528) and buffered from the memory array by three MC14503 buffers in parallel. This clock is multiplexed with the Memory Clock by use of the three-state feature of the MC14503. The Memory Clock (used during normal operation) is translated to 12-V levels by use of MC75451 drivers. Decoding of the CE_A and CE_B signals (i.e., clocking only the memory bank addressed) to conserve power is accomplished by the MC7400 gates in conjunction with the MC75451 drivers.

Since the $\overline{\text{Power Fail}}$ signal will occur asynchronously with both the $\overline{\text{Memory Clock}}$ and the refreshing operation (Refresh Clock), it is necessary to synchronize the $\overline{\text{Power Fail}}$ signal to the rest of the system in order to avoid aborting a memory access cycle or a refresh cycle. An MC14027 dual flip-flop is used as the basic synchronization device. The leading edge of the Refresh Clock triggers a 3 μs monostable multivibrator which is used as a refresh pretrigger. The trailing edge of this pretrigger triggers a 500 ns monostable which creates the CE pulse during standby operation. The 3 μs pretrigger signal is used to direct set half of the MC14027 flip-flop, the output of which, (B), then inhibits a changeover from the standby to the operating modes (or vice versa). This logic prevents the system from aborting a refresh cycle should the $\overline{\text{Power Fail}}$ signal change states just prior to or during a refresh cycle. The trailing edge of the 500 ns monostable clears the MC14027 flip-flop, enabling the second flip-flop in the package. The state of $\overline{\text{Power Fail}}$ and Power Fail is applied to the K and J inputs of this second flip-flop and is synchronized by clocking with $\overline{\text{Memory Clock}}$. The outputs of this flip-flop, labeled Bat and $\overline{\text{Bat}}$, lock the system into the refresh mode and multiplex in the internal clock for standby operation when Bat = "1".

SYSTEM PERFORMANCE

Figure 12 is a photograph of the breadboard of this dynamic memory system. This breadboard was interfaced with an EXORciser system and tested using a comprehensive memory test program written in-house.

Figure 13 is a photograph of waveshapes associated with alternate reads and writes in one 4K bank of the memory system. Included also is the M6800 program used to generate these waveforms. This type of operation produces repetitive signals on the memory board in order to aid troubleshooting. Note the refresh cycle sandwiched in among the read and write cycles, and that the decoding of the CE signals produces no clocks on CE_A (accesses are to bank B), except during refresh.

Figure 14 shows the printed circuit memory array used to interconnect the memories. The addresses are bussed between the 4K memory chips in the horizontal direction. Data lines are bussed in the vertical direction. The MCM6605 4K RAM has power and ground pins on the corners of the package allowing wide, low impedance power and ground interconnects within the memory array. Decoupling capacitors were used as follows within the memory array: +12 V - one 0.1 μF ceramic per package, +5 V - one 0.01 μF ceramic for every three packages, and -5 V - one 0.01 μF ceramic for every three packages. Figure 15 is a photograph showing the ripple on the power supplies caused by accesses to one 4K byte bank of memory as shown in the photograph. The +12 V line supplies the most current to the array and is the one on which the most care in decoupling (wide PC lines and distributed capacitance) should be taken. Placement of the V_{DD} pin on the corner of the package allows the designer the option to do this easily.

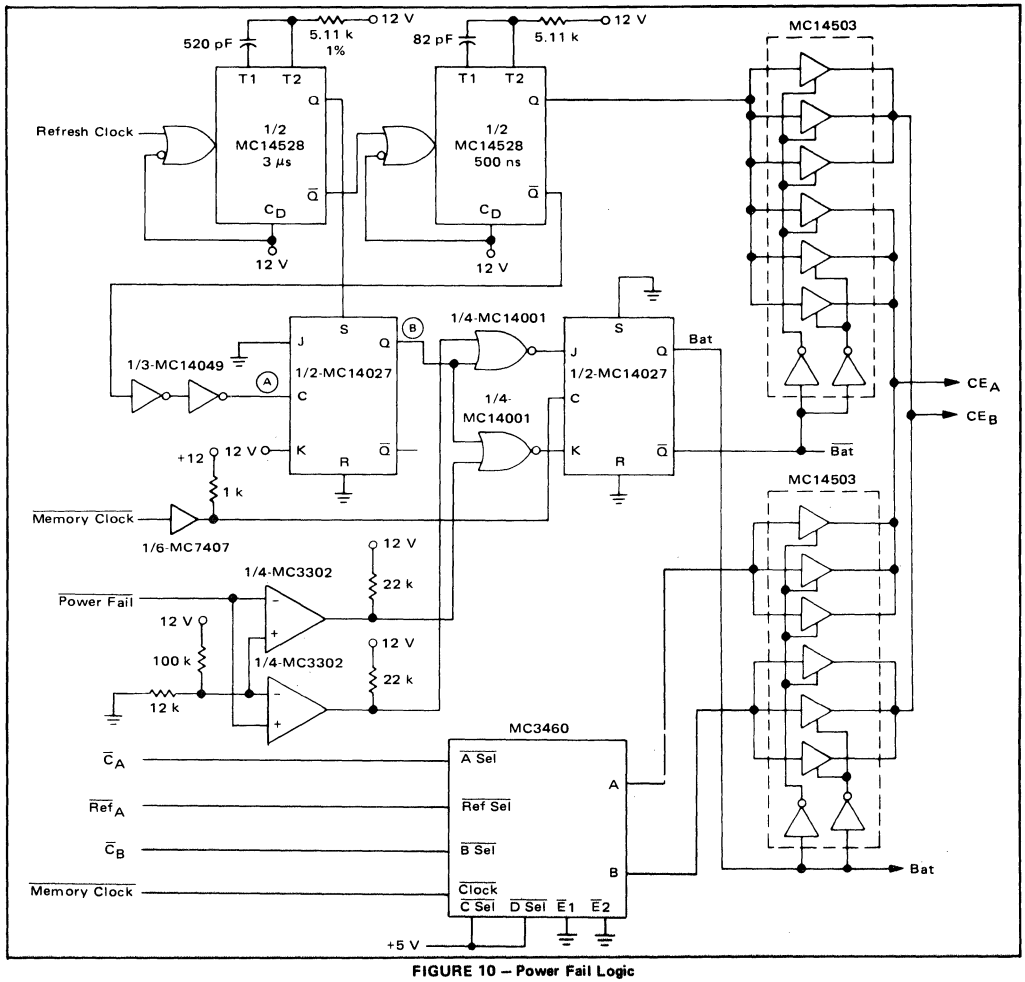


FIGURE 10 – Power Fail Logic

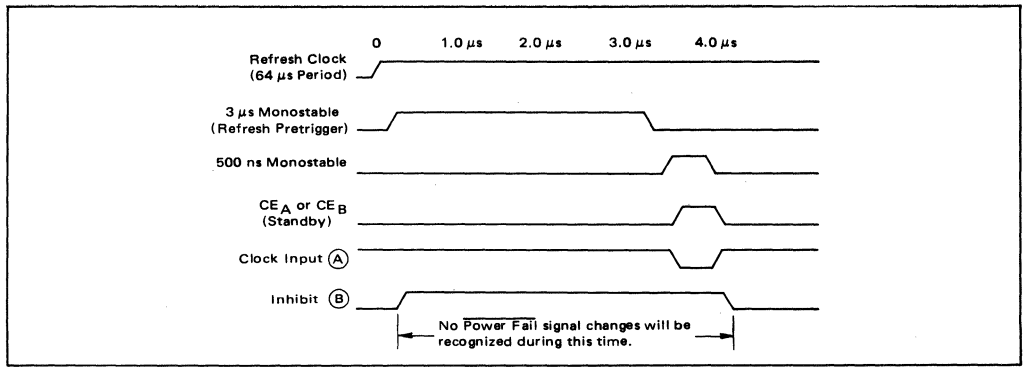


FIGURE 11 – Power Up/Down Synchronization

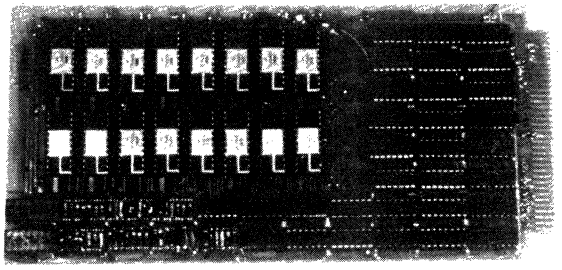
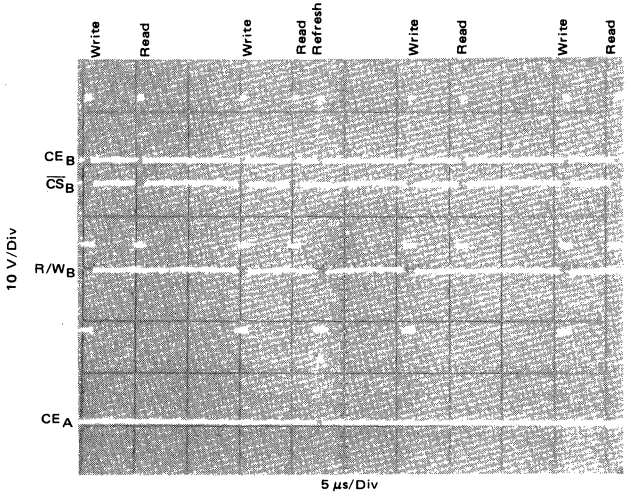


FIGURE 12 – Memory System Breadboard



M6800 Program to Generate Waveforms Shown

Address	Data	Mnemonic	Comment
0000 0001	B6 55	LDA #@55	Load data to be written (55)
0002 0003 0004	B7 30 00	STA A %3000	Store data in address 3000
0005 0006 0007	F6 30 00	LDA B %3000	Read data from address 3000
0008 0009 000A	7E 00 02	JMP %0002	Loop back

FIGURE 13 – Alternate Read and Write Memory Accesses

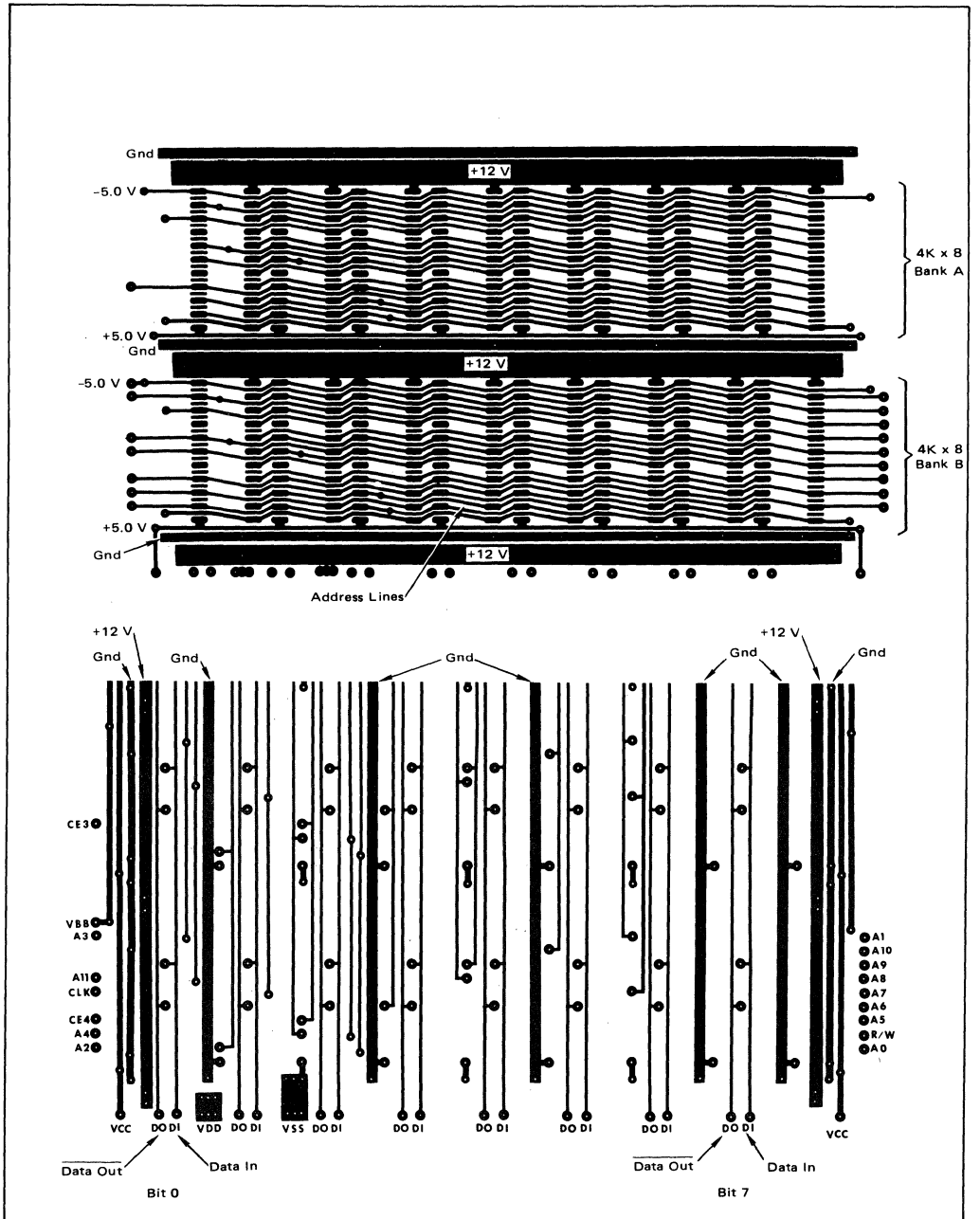


FIGURE 14 – Memory PC Board Array

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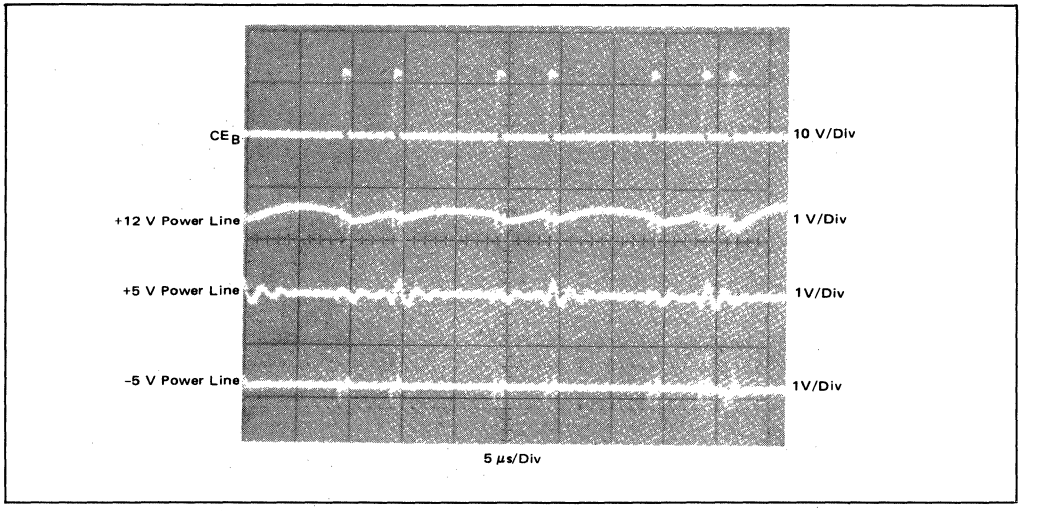

FIGURE 15 – Power Line Ripple

The dc power dissipation of this memory system is shown in Table 1. Of these current drains, the most critical to non-volatile operation is the current requirement in the standby mode in which the current would probably be supplied from a battery. A breakdown of the typical current required from +12 V to maintain the memory in the standby mode is shown in Table 2.

By using CMOS for the refresh logic and capacitance drivers, a dynamic memory, and a low current refresh oscillator, the standby current has been reduced to a level that can be supplied easily by a battery. Table 3 is a brief list of various capacity 12-V batteries that could be used to power a system of this type in the standby mode. Support time runs from one-half to 35 days and can be made as long as desired if sufficient battery capacity is available.

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TABLE 1 – 8K x 8 Non-Volatile Memory System Power Requirements (1-MHz EXORciser Clock Rate)

Mode	Power Supply	Current	
		Typical	Maximum
Operating	+12 V*	100 mA	300 mA
	+5 V	600 mA	860 mA
Standby	+12 V	14 mA	20 mA
	+5 V	No +5 V Supply required	

*Because memory is dynamic, the +12 V current requirement is dependent on rate of memory access.

TABLE 2 – Standby Mode Current Allocation

Circuit Section	Typical Current
+12 V Current (V_{DD})	5 mA
Charge Pump	3 mA
Comparator	2 mA
Capacitance Drivers	4 mA
Total	14 mA

TABLE 3 – Battery Characteristics

Battery	Ampere-Hours	Size (L x W x H)	Weight	Support Time*
Globe GC 12200	20	6.9" x 6.5" x 4.9"	16.75 lbs.	35 days (850 hrs)
Globe GC 1245-1	4.5	6" x 2.5" x 4"	4.5 lbs	8 days (192 hrs)
Globe GC 1215-1	1.5	7" x 1.3" x 2.6"	1.5 lbs	2.6 days (63.75 hrs)
Burgess MP 202	0.6	3.4" x 1.4" x 2.3"	11.6 oz	1.25 days (30 hrs)
Burgess 12.0 V 225 Bh	0.225	3.5" H x 1" Diam.	4.65 oz	0.47 day (11.25 hrs)

*Assumes 20 mA average current drain (14 mA for memory and 6 mA for power fail detection circuitry) and a battery voltage range during discharge from 13 to 11 V.

SUMMARY

This application note has described the design of an 8K byte memory system, based on the MCM6605A 4K x 1 dynamic RAM, to provide non-volatile operation with a minimum of standby current. Tests on the breadboard memory system indicate standby currents typically 14 mA from a 12 V battery. The discussion has shown that a dynamic memory refresh requirement can be handled with minimal control logic. For memory sizes in the area of 8K bytes, the higher bit density of the 4K chip makes the system design cost effective when compared to an equivalent static memory design. In the area of non-volatility, the standby mode inherent in a dynamic memory makes it a "hands down" winner when compared to a static memory design of this size.

THE DESIGN OF AN N-CHANNEL 16K X 16 BIT MEMORY SYSTEM FOR THE PDP-11

INTRODUCTION

When PMOS dynamic random access memories were introduced, they offered, for the first time, memory systems with a cost/performance exceeding that of cores. Although they have been fairly successful in competing with core memories for mainframe applications, there were many shortcomings. For example, some memories required critical overlapping clock pulses which complicated the design and placed an extreme burden on the layout. The logic levels for both input and output were not compatible with standard logic, such as TTL, which meant that translators had to be used. The actual cost of these translators is small compared to the penalty paid for the added complexity of the memory board, additional power, and extended system cycle time. Also additional bypassing is required and the board layout complicated by the ac noise generated from the translators.

With the advent of N-channel and advanced design techniques, a whole new breed of MOS memories has emerged. One such memory is the MCM6605A. The MCM6605A is a 4096-word by 1-bit dynamic memory that does not exhibit any of the undesirable features mentioned earlier. For example: This memory requires only one clock that has no critical overlaps. All inputs and outputs are TTL compatible, and the memory access time is fast (210 ns max). Other features include chip select for easy memory expansion and three-state output. Because of the high density, low power, and high speed of this semiconductor memory, it is ideal for mainframe memory applications.

This paper briefly covers the operation and features of the MCM6605A, and then illustrates the design of a PDP-11 add-on mainframe memory system employing the MCM6605A. The memory system to be described contains 16K words by 16 bits or 32K bytes of semiconductor memory and the associated electronics necessary to control and interface the semiconductor memory to the PDP-11. The whole memory system can be mounted on a single P.C. board because of the small amount of support electronics required and the high density of the MCM6605A memory.

The support electronics can be easily partitioned into three sections or functions: bus interface, refresh timing and control, and memory control and interface. A detailed description is given of the logic and interface devices necessary to perform each of these functions.

The paper is concluded with a summary on the performance of this add-on memory system with the PDP-11 computer.

MCM6605A OPERATION

The MCM6605A is a dynamic random access memory that contains 4096 bits of storage organized into 4096 words by 1 bit. This semiconductor memory, which comes in a standard 22-pin package, see Figure 1, is fabricated with an N-channel silicon gate process to optimize speed, power, and density tradeoffs. By employing the standard three transistor cell arrangement, the internal sense amplifier requirements were simplified.

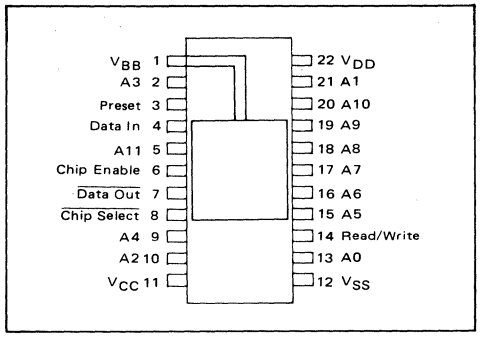

FIGURE 1 – MCM6605A Pin Assignment

In addition to the high speed (210 ns access) and low power (82 μW/bit active and 0.63 μW/bit standby), the MCM6605A has additional features such as TTL-compatible inputs with latch capability on the address inputs, three-state output with chip select control for easy memory expansion in the word direction, only 32 refresh cycles required every 2 ms, and the power supply pins on the corner of the package to simplify power supply distribution and bypassing on the board. One high-voltage clock is required and there is no critical timing or signal overlap.

The net result of these features can provide a big saving in system costs, not only because of the lower cost of the semiconductor memory per bit, but because of the increased packaging density per board, less support electronics, bipolar logic compatibility, reduced power, and lower assembly costs. All of these savings will be apparent in the memory system to be covered in the following sections.

A detailed description of the operation of the MCM6605A is necessary for the design of the memory controller. The 4096 bits of storage are divided equally

into four quadrants as noted in the block diagram given in Figure 2. In addition to the storage, the chip contains input address latches, row and column decoder logic plus additional logic to control the input and output of data to the storage area.

The MCM6605A uses three internal clock signals to control reading from, or writing into, the storage cells. These three clock signals ($\phi1$, $\phi2$, and $\phi3$ shown in Figure 2) are controlled by Chip Enable (CE) and Read/Write (R/W) to perform the various read, write, refresh, or combination cycles possible with the MCM6605. The timing for these cycles is given in Figures 3 and 4.

The $\phi1$ clock is on whenever CE is low (standby position) and precharges the dynamic circuitry of the MCM6605A in preparation for the start of a memory cycle.

Read Cycle

The one high level clock line, CE, is brought high to initiate all cycles. The rising edge of CE turns off the $\phi1$ precharge and initiates the $\phi2$ clock. The $\phi2$ clock does several things in sequence. First, it latches the input addresses into buffers and drives the column decoders. These decoders use addresses A0 to A4 to select one column of 64 storage cells on each side of the chip and transfer the 128 stored data bits onto precharged bit sense lines. The row decoders use A5 to A11 to select one bit of the 128 bit sense lines. This selected bit is exclusive NORed with a data control cell (the purpose of which is explained under write cycle below) and is used to drive an output buffer/latch. The $\phi2$ signal terminates at this time after latching the data into the output buffer. The cycle can be terminated at this point by bringing CE low to standby, allowing $\phi1$ to precharge the memory before the next cycle. During this simple read cycle, R/W must remain high to inhibit writing.

Write Cycle

The write cycle is the same as a read cycle, up until $\phi2$ terminates with 128 bit sense lines holding the two columns of data. When $\phi2$ goes off, a $\phi3$ signal is initiated anytime R/W is in the write position. This $\phi3$ clock transfers the data on the 128 bit sense lines back into the storage array. The line selected by the row decoder (A5 – A11), however, has been overridden by input data. The write cycle is terminated by bringing CE low into standby. The $\phi2$ – $\phi3$ sequence of bringing data from the

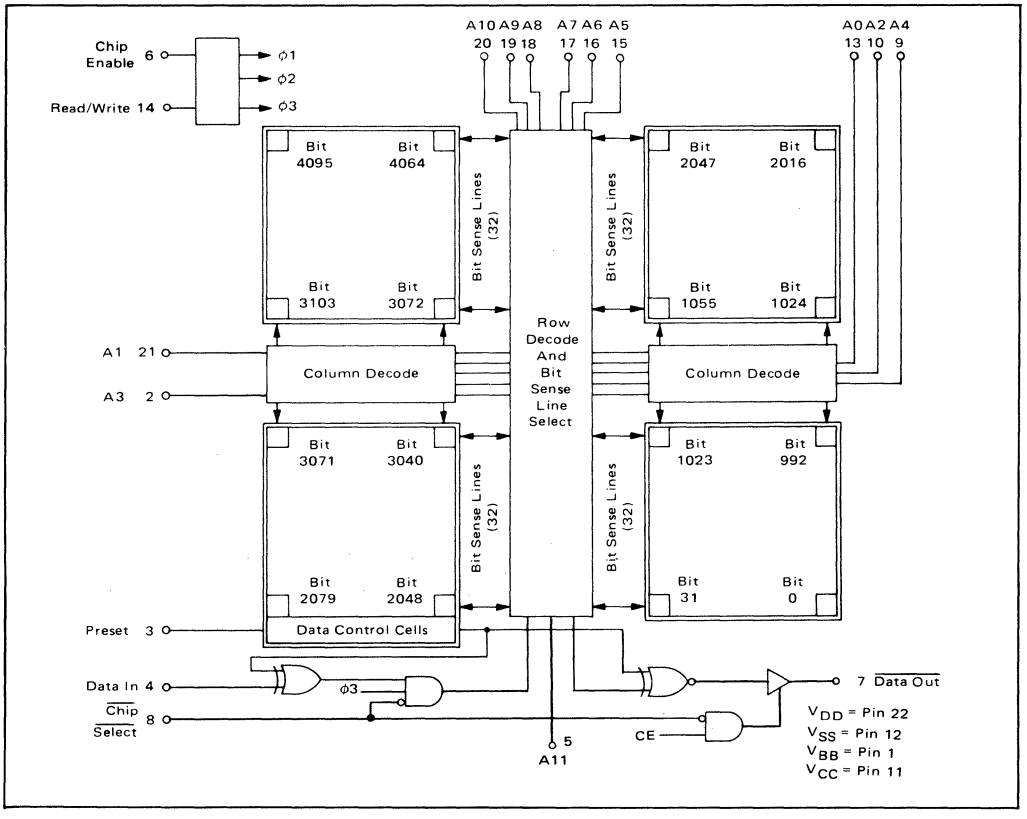

FIGURE 2 – Block Diagram

storage cells onto bit sense lines and then putting the data back into the cells inverts the stored data since the read operation is inverting but the write operation is not. In order to keep track of the polarity of the stored data, a row of data control cells is added to the array and is driven by the same column decoder which drives the storage cells. The data control cells are identical to the storage cells and are inverted each time a write cycle is performed. By performing an exclusive NOR function of both input and output data with the control cell tied to the same column, the relative polarity is always discernable and inversions do not cause loss of data.

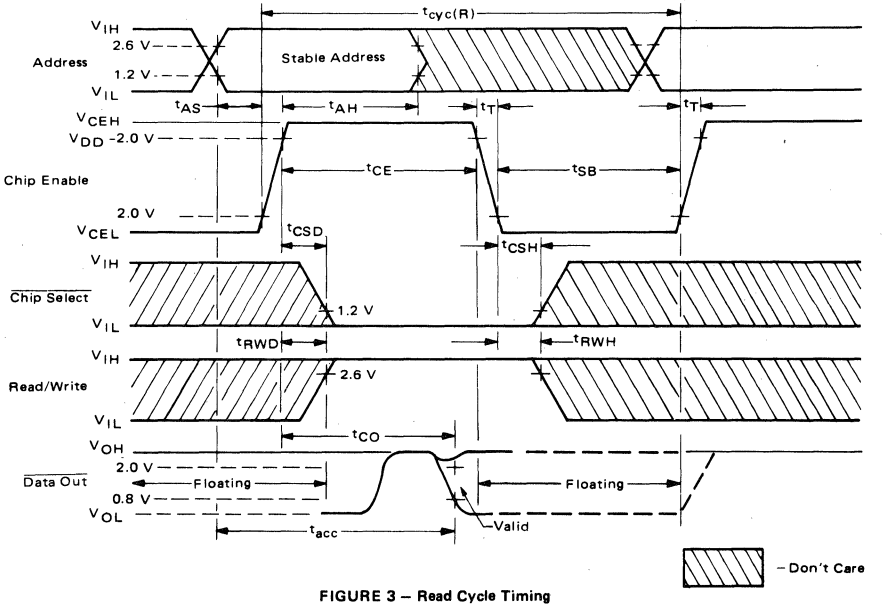

FIGURE 3 – Read Cycle Timing

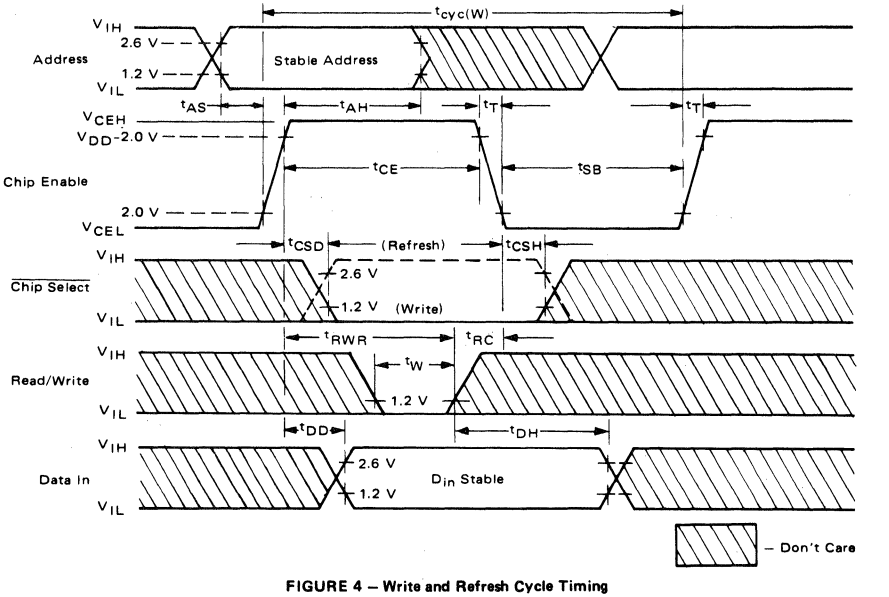

FIGURE 4 – Write and Refresh Cycle Timing

Refresh Cycle

The write operation described above actually refreshes 127 bits in the selected columns while it is writing into one bit. If the Chip Select ($\overline{CS}$) signal is held high to inhibit the input data, then a write cycle would merely refresh all 128 bits. Therefore, one write cycle with $\overline{CS}$ high (now called a refresh cycle) on each of the 32 combinations of A0 through A4 will refresh the entire memory as long as each address combination is used every 2 ms.

When the memory is first powered up, the data control cells may not come up with a valid logic level and several refresh cycles may be required to insure a solid logic level. In system usage, this would cause no difficulty, since data would not normally be immediately written into the memory system. For memory test purposes, a preset input (pin 3) is included to preset these data control cells with a 200 ns pulse. This preset pin should be permanently grounded in systems unless there is some unusual requirement.

Keeping the above memory operation in mind, the first phase of the design will be the PDP-11 interface.

MEMORY SYSTEM

First of all, the memory system can be divided into four distinct functions or sections as illustrated in Figure 5: the memory – CPU interface, refresh address and control, memory timing control, and the memory array.

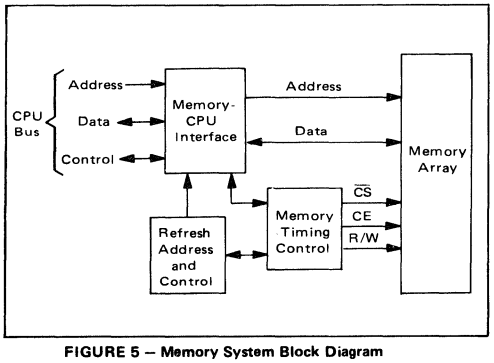

FIGURE 5 – Memory System Block Diagram

1. Memory – CPU Interface

To interface with the PDP-11 computer, the following bus lines are required: 18 address, 16 data, and 4 control. The least significant address bit, $\overline{A}00$, is actually used with the control bits C0 and C1 to determine if a write cycle is to be done on the lower byte (data bits D0 – D7) or upper byte (data bits D8 – D15) as illustrated in Figure 6. The next 12 address bits, $\overline{A}1$ through $\overline{A}12$, go directly to the memories to select one word from 4096 words; see Figure 7. Address bits $\overline{A}13$ and $\overline{A}14$ are used to select one 4K memory block from the 16K words per memory board.

Address bits $\overline{A}15$, $\overline{A}16$ and $\overline{A}17$ permit the main-memory capacity of the PDP-11 to be expanded to 128K words. Thus, only eight 16K memory boards are required

C0	C1	$\overline{A}00$	Condition
X	0	X	Read
0	1	X	Write (0-15)
1	1	0	Write (0-7)
1	1	1	Write (8-15)

X = Don't Care

FIGURE 6 – Memory Control Truth Table (PDP-11)

for the complete main-memory capacity of the PDP-11. The jumper box, illustrated in Figure 7, can be wired to decode address bits $\overline{A}15$, $\overline{A}16$ and $\overline{A}17$ for the selection of only one of the eight memory boards.

The bus lines require special circuits to receive and transmit data so that the transmission-line characteristics of the lines will be maintained. The circuits chosen for this job were the MC3450/MC3452 quad line receivers and the MC4042 quad pre-driver.

The MC3450/MC3452 Bus Receiver

The MC3459 is a quad receiver that features three-state outputs; the MC3452 has open collector outputs. These line receivers were chosen because of the following features:

(1) High input impedance keeps loading of the line to a minimum.
(2) Minimum overdrive to switch receiver is 25 mW, which provides high noise immunity.
(3) The differential input amplifier stage of the receiver can be used to provide either true or complement signals; see Figure 7.
(4) Four receivers per package greatly reduce the total package count.

In order to use the MC3450 or MC3452 as a single-ended line receiver, one input to the differential receiver has to be tied to a reference voltage. For optimum noise immunity, the reference voltage should be set halfway between the minimum high and maximum low voltage specified for the line. Minimum high for this system is 2.5 V and maximum low is 1.4 V. The optimum reference voltage (V_{ref}) for these limits would be 1.95 V. The reference voltage generator is given in Figure 7. The voltage generator is designed to give a constant V_{ref} of 1.95 V regardless of the line receiver current drain. The 1N914 diode is used to track the base-emitter voltage of the 2N3904 with temperature, thus providing relatively constant output voltage over temperature. Note that true and complement signals (A00/$\overline{A}$00) in Figure 7 are easily generated by attaching the V_{ref} voltage to either the non-inverting or inverting inputs respectively.

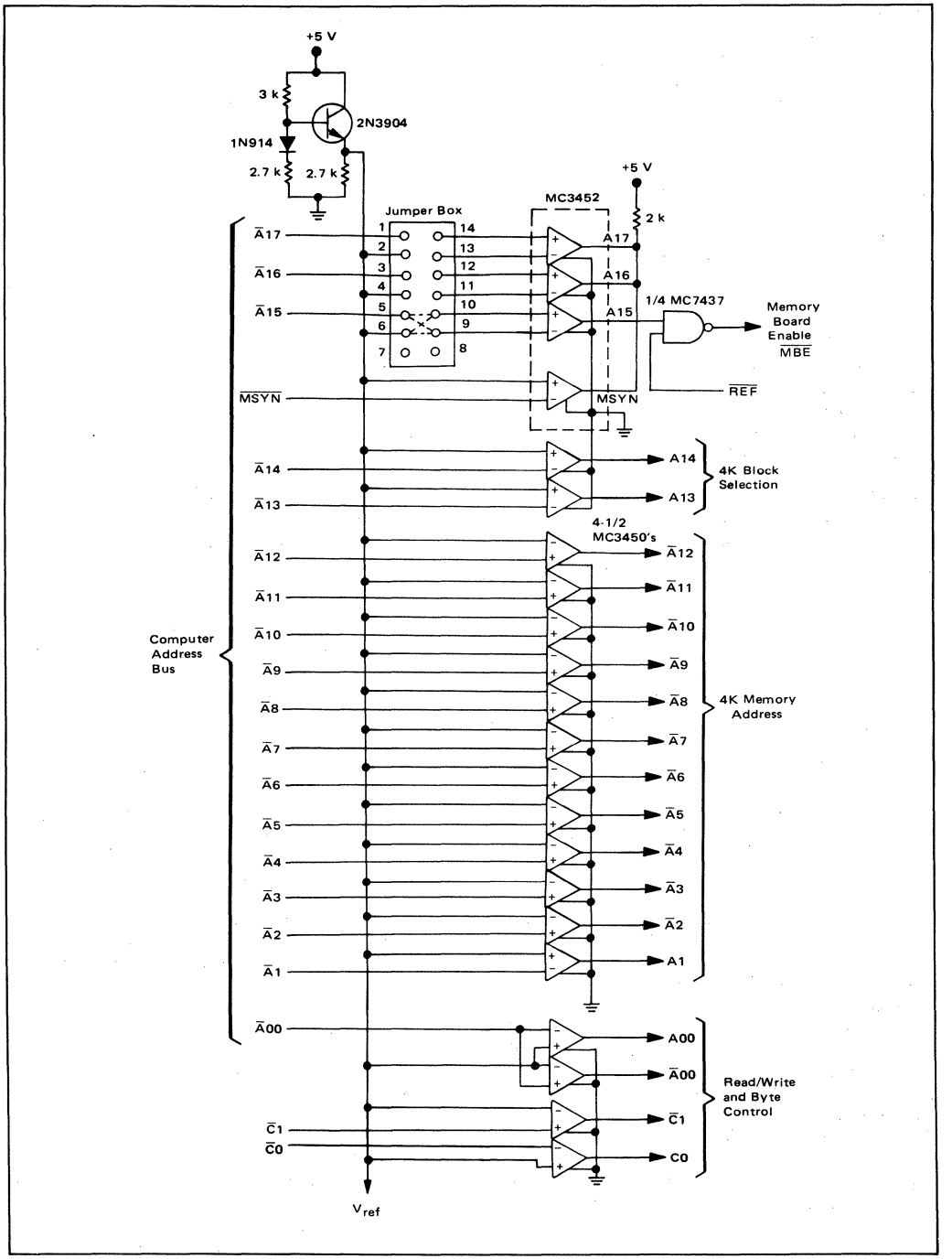

FIGURE 7 – CPU/Memory Address and Control Interfaces

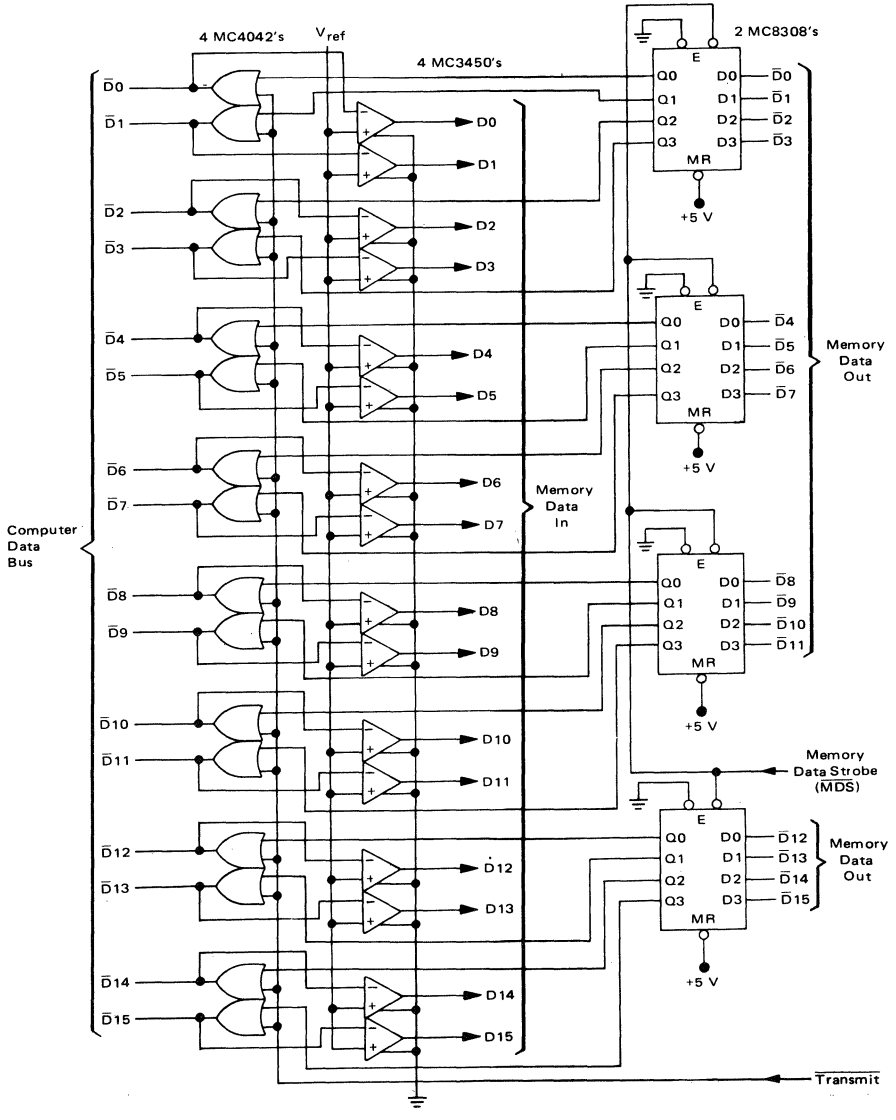

FIGURE 8 – CPU/Memory Data Interface

The MC4042 Bus Driver

The only bus lines for this memory system that require bi-directional transfer are the 16 data lines illustrated in Figure 8. Data transmission on the bus must be done with open collector drivers that are capable of sinking 50 mA with a V_{OL} less than 0.8 V. Also, the driver output must be strobed high when data is not being transmitted. The MC4042 quad pre-driver meets these requirements. The memory data register (MDR) is included in the data interface. The MDR is required to retain valid data on the bus because the memory CE signal is terminated before the system read cycle is complete.

2. Memory Timing Control

Before discussing the design of the memory control section, it might be helpful to review the interaction required between the CPU and memory system for a read or write cycle. The following discussion will use the system timing diagrams shown in Figures 9 and 10 extensively.

System Read Cycle

Figure 9 shows the sequence of events that must occur to successively transfer data from the memory to the CPU. At the start of a read cycle, the CPU sends the address of the storage location it wishes to receive data from, and the

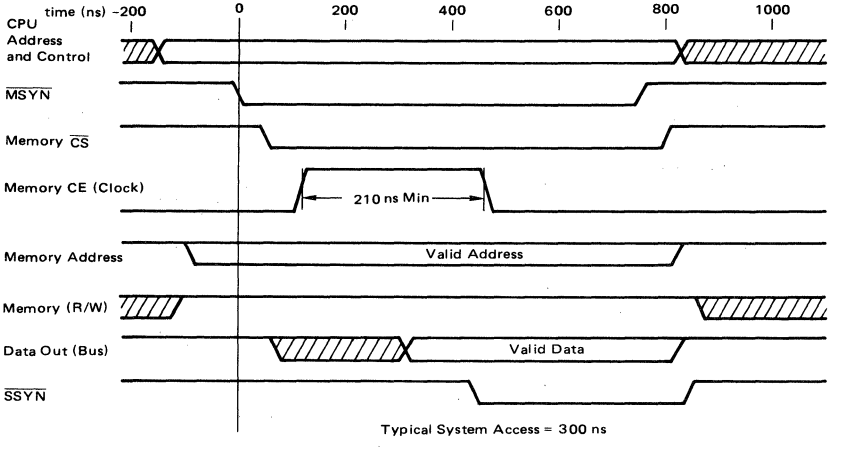

FIGURE 9 – Typical System Read Cycle Time

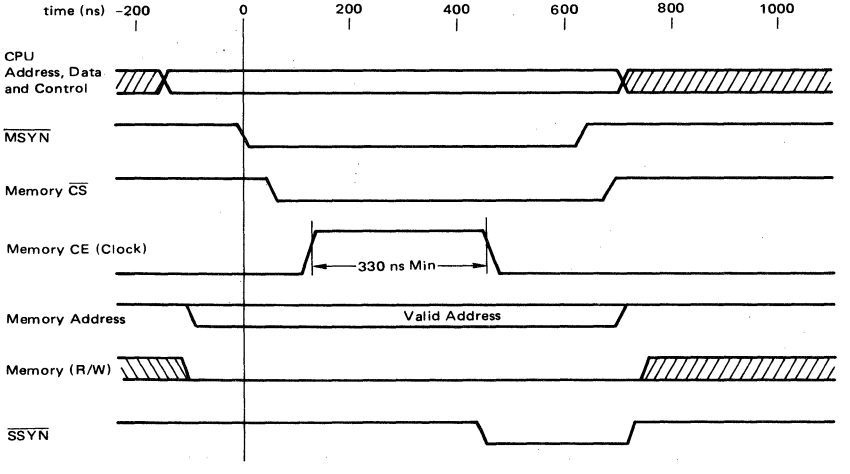

FIGURE 10 – Typical System Write Cycle Time

control lines ($\overline{C0}$, $\overline{C1}$) tell the memory system that the operation to be performed is a read cycle. The logic state of $\overline{C0}$ and $\overline{C1}$ for a read cycle is given in Figure 6. The CPU waits for at least 150 ns to allow for address deskewing and decoding before signaling the start of a read cycle with a master synchronization signal ($\overline{MSYN}$). The remaining signals shown in Figure 9, with the exception of the slave synchronization signal ($\overline{SSYN}$), are the same as those given in Figure 3. When the control board receives $\overline{MSYN}$, the $\overline{CS}$ and CE signals are sent to the memories. At the end of the 210 ns Chip Enable clock, the memory controller must generate $\overline{SSYN}$ to indicate that the data read from the memories is valid. When $\overline{SSYN}$ is sent, the CPU strobes in the data and terminates the cycle by releasing $\overline{MSYN}$.

System Write Cycle

With a write cycle, the data and the address of where the data is to be stored are placed on the bus as indicated in Figure 10. The logic states of $\overline{C0}$, $\overline{C1}$, and $\overline{A00}$ (Figure 6) determine whether the write cycle to be performed is a byte or a word. As with the read cycle, 150 ns is allowed for deskewing and decoding before $\overline{MSYN}$ is sent. The remaining signals given in Figure 10 are the same as those given in Figure 4. When the memory board receives $\overline{MSYN}$, the data, $\overline{CS}$, and CE signals are sent to the memories. At the end of the 330 ns Chip Enable pulse, the memory controller sends $\overline{SSYN}$ to the CPU to signal that the data has been stored. The CPU then terminates the write cycle by releasing $\overline{MSYN}$.

It should be apparent from the preceding discussion that the timing required for either a read or write cycle is extremely simple and that no critical overlapping of signals is required. The complete memory control section is given in Figure 11. Keeping the above memory timing description in mind, the memory control section performs in the following manner.

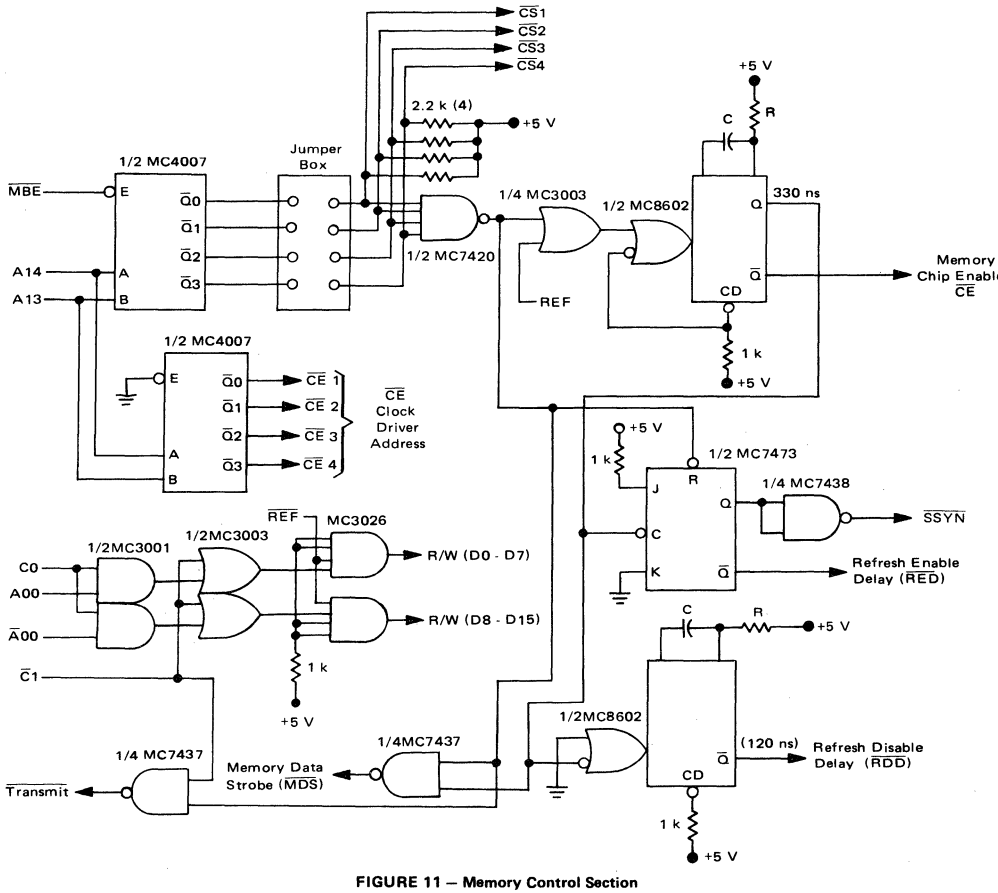

FIGURE 11 – Memory Control Section

Memory Control – Read Mode

Although the CE clock time of the MCM6605A for a read cycle is 120 ns less than that for a write cycle, the CE time for both the read and write cycles was made equal to simplify the memory controller.

For the read cycle, the logic states of control lines C0 and C1 force the read/write buffers into the logic "1" state. A memory board enable ($\overline{MBE}$) signal is generated from the memory – CPU interface circuitry (Figure 7) when the $\overline{MSYN}$ line goes low with the presence of a valid memory board address. The $\overline{MBE}$ signal propagates through the one-of-four demultiplexer (MC4007) and a $\overline{CS}$ signal is sent to the row of memories determined by addresses A13 and A14. The jumper box allows the memory board to be only partially populated for smaller size memory requirements.

The $\overline{CS}$ signal also enables the data bus drivers with $\overline{Transmit}$, and the leading edge of $\overline{CS}$ triggers the MC8602 one-shot which sets the memory CE clock pulse width (330 ns min). To conserve power, the memory CE clock driver is decoded so that only one row of memories will receive a clock pulse (see CE clock address in Figure 11).

On the trailing edge of the CE pulse, the valid data will be strobed into the MDR and the J-K flip-flop is clocked to a logic "1". This enables the $\overline{SSYN}$ line, which tells the CPU that the data on the bus is valid. After the CPU strobes in the valid data, the CPU releases $\overline{MSYN}$ which terminates $\overline{SSYN}$ by resetting the J-K flip-flop. The termination of $\overline{SSYN}$ completes the read cycle.

Note in Figure 11 that the $\overline{Q}$ output of the J-K flip-flop is labeled Refresh Enable Delay ($\overline{RED}$). This output is sent to the refresh control logic to delay the start of a refresh cycle if requested during a CPU cycle (see refresh control). The delay is necessary to insure the minimum t_{SB} time of the memory; see Figures 3 and 4.

Memory Control – Write Mode

The controller performs in the same manner as the read mode with the following exceptions. The control lines force the Read/Write buffers into the write mode and they also disable the $\overline{Transmit}$ signal.

On the trailing edge of the memory CE clock pulse, the $\overline{SSYN}$ line is set low to signal the CPU that the data is stored. The cycle is then terminated with the release of $\overline{MSYN}$ which resets the $\overline{SSYN}$ flip-flop.

Memory Control – Refresh Mode

To perform the refresh cycle, the memory controller is forced into a write mode with a refresh request (REF = logic "1"). The REF signal also enables the refresh address and disables the $\overline{MBE}$ signal (see Figure 7). The $\overline{MBE}$ signal is disabled to prevent the memories from receiving a $\overline{CS}$ signal and the CPU a $\overline{SSYN}$ signal.

The CE clock one-shot is triggered on the leading edge of REF and CE is sent to all of the memories (see section on clock driver). On the trailing edge of CE, a 120 ns one-shot is triggered to delay the start of a CPU cycle that could be requested during a refresh cycle. This signal insures the minimum t_{SB} time of the memory by keeping the $\overline{MBE}$ signal disabled for at least 120 ns after the trailing edge of CE (see refresh control).

3. Refresh Address and Control

In order to insure that data is retained, the whole memory must be completely refreshed every 2 ms as noted earlier. This can be accomplished by insuring that a write cycle is performed on each of the 32 column addresses at least once every 2 ms. There are two ways in which refresh can be performed. One method would be to initiate at the end of a 2 ms period a burst of 32 column refreshes, one refresh cycle followed immediately by another. The second would be to steal one column refresh cycle every 62.4 μs. The latter approach was taken since it would present the least interference to programs being executed by the CPU.

To implement refresh, the following logic is needed: a 16 kHz clock, one 3-input NAND gate, two D latches, a 5-bit ripple counter, and a 5-channel digital multiplexer as illustrated in Figure 12. The 16 kHz can be generated with the MC4024, a voltage controlled multivibrator. The frequency of the MC4024 is adjusted to 16 kHz by setting the voltage on the dc control input with the 5 k ohm variable resistor. The control section is comprised of two flip-flops and the NAND gate. On the positive edge of the 16 kHz clock, a logic "1" propagates through the two flip-flops and REF is switched to a logic "1". Of course, this assumes that no memory cycle is presently being processed ($\overline{MBE}$ input a logic "1"). If a memory cycle is being executed at the time a refresh cycle is requested ($\overline{MBE}$ a logic "0"), then flip-flop #2 will not be set until the end of the memory cycle being executed ($\overline{MBE}$ switched to a logic "1"). When REF is switched to a logic "1", the control logic of Figure 11 is set to perform a write cycle, and the external address coming from the CPU is switched to the refresh address. This gating of the addresses can be accomplished with the quad 2-input multiplexer (MC8322) and the MC7451 as shown in Figure 12. The refresh address is generated with the 5-bit ripple counter comprised of the MC7493 and one-half of an MC7473. The refresh cycle is terminated on the trailing edge of the $\overline{RDD}$ pulse by switching flip-flop #2 (REF) to a logic "0".

These three sections of the memory system are integrated into a single logic schematic shown in Figure 13. For clarity of interconnection between the memory array and the memory control section of the system, the address buffers and clock drivers are also included in the schematic. These devices will be covered in the following discussion of the memory array.

4. Memory Array

The memory array contains sixty-four MCM6605A memories arranged in a matrix of four rows and sixteen columns as noted in Figure 14. The sixteen columns are divided into two groups of eight each with separate read/write control signals. This partitioning scheme provides for

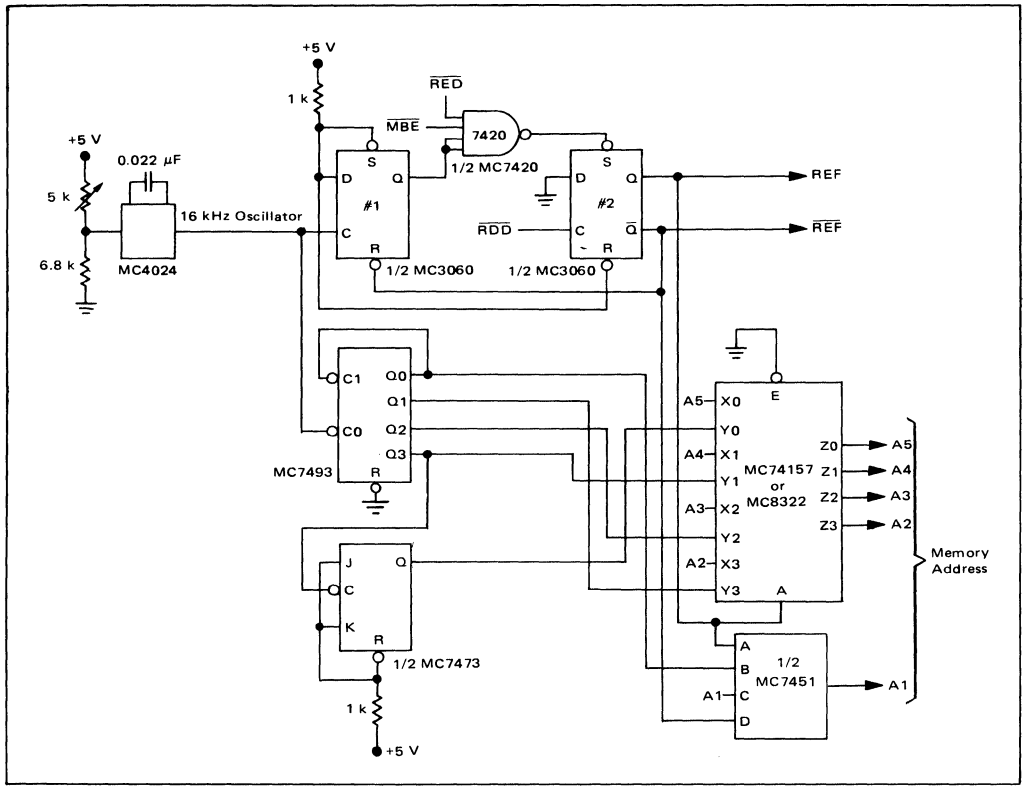

FIGURE 12 – Refresh Address and Refresh Control

a byte as well as a word transfer. Also included in the memory array are address buffers and clock drivers.

The MC3459 Address Line Driver

Although the address inputs of the MCM6605A exhibit low input capacitance (5 pF max), the total parallel input capacitance of these lines in the array can exceed 300 pF. Standard TTL logic gates have insufficient current drive capability to rapidly switch a high capacitive load, therefore, a high speed buffer, such as the MC3459, is required; see Figure 15. The MC3459 has sufficient output current to typically switch a 360 pF load in 20 ns. This fast switching of the lines can cause a considerable amount of overshoot so a 10-ohm series damping resistor is recommended. The output of the MC3459 also has an internal 2.5 k ohm pullup resistor to provide a higher V_{OH} (3.2 V at -640 μA) than standard TTL logic gates. This higher V_{OH} meets the minimum V_{IH} (3.0 V) requirement of the MCM6605.

The MC3460 Clock Driver

The MC3460 quad clock driver, see Figure 16, was employed to meet the high voltage requirements of the memory CE input. The clock driver has internal logic to either select one of the four clock drivers for a normal CPU memory cycle or to select all four drivers at the same time for a refresh cycle. Two enable inputs are also provided for additional memory expansion to 64K words without additional address decoding. Other features of the MC3460 include fast switching (25 ns typical for a 480 pF load), and low dc power for the V_{DD} supply (348 mW max for all four drivers in the logic "0" state).

For the memory array given, each clock driver has to fan out to 16 memory chips. To drive this number of memory chips, an external 6.2 k ohm pullup resistor is required for each driver output to insure a minimum V_{OH} of V_{DD} -1.0 V at a maximum leakage current of 160 μA. A minimum 20 ohm damping resistor is also recommended on the CE lines to reduce overshoot.

The memory system described was laid out on a standard size PDP-11 two-sided PC board as illustrated in Figure 17. A photo of the actual memory board is given in Figure 18.

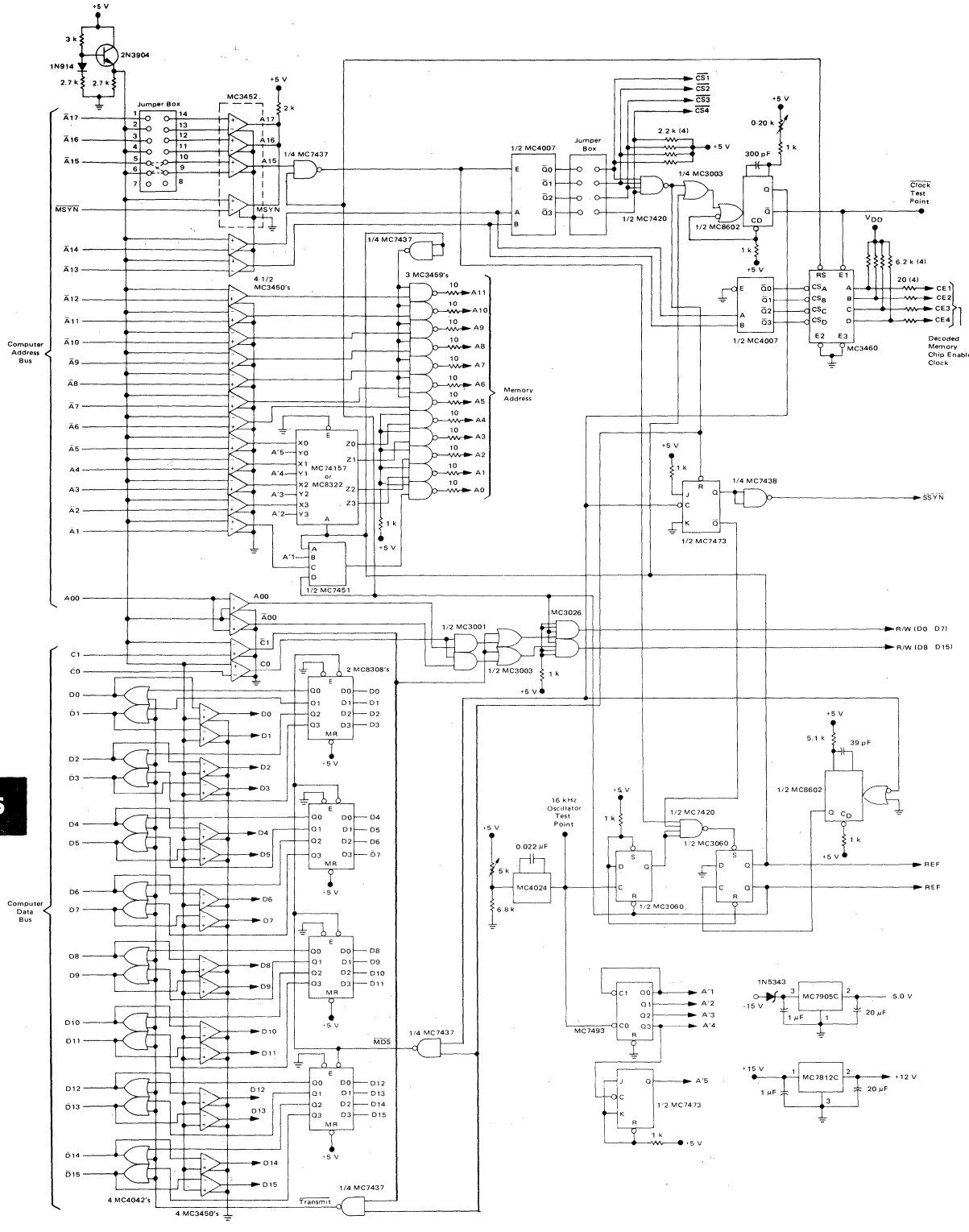

FIGURE 13 – Memory System Schematic

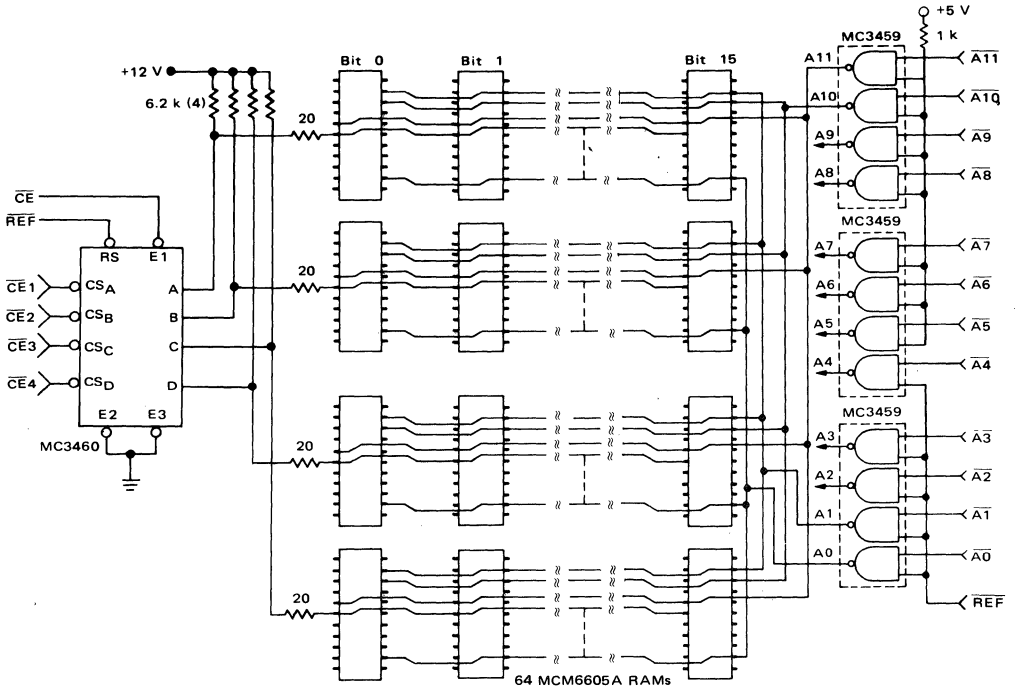

FIGURE 14 – Memory Array

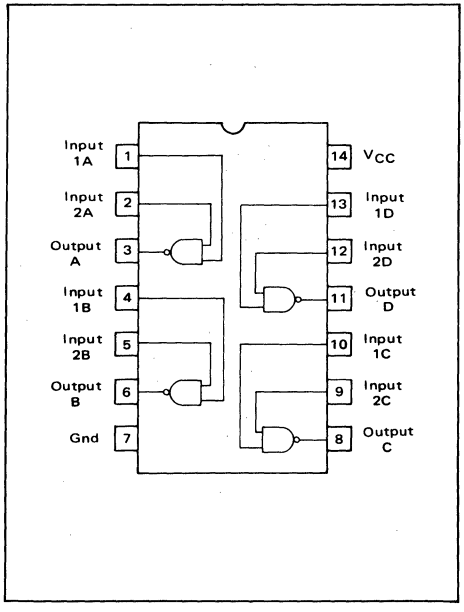

FIGURE 15 – MC3459 Pin Assignment

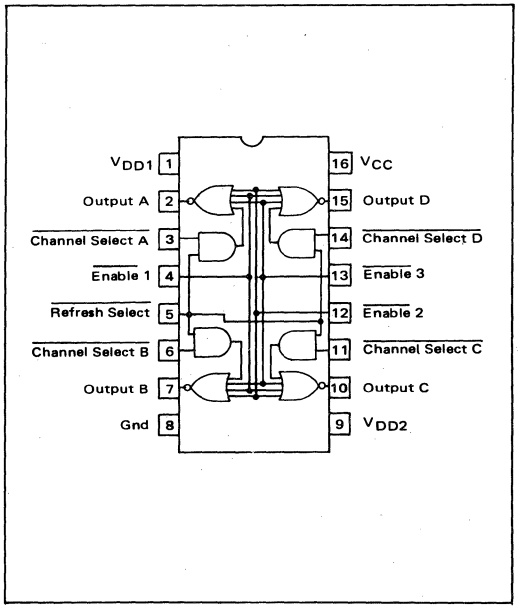

FIGURE 16 – MC3460 Pin Assignment

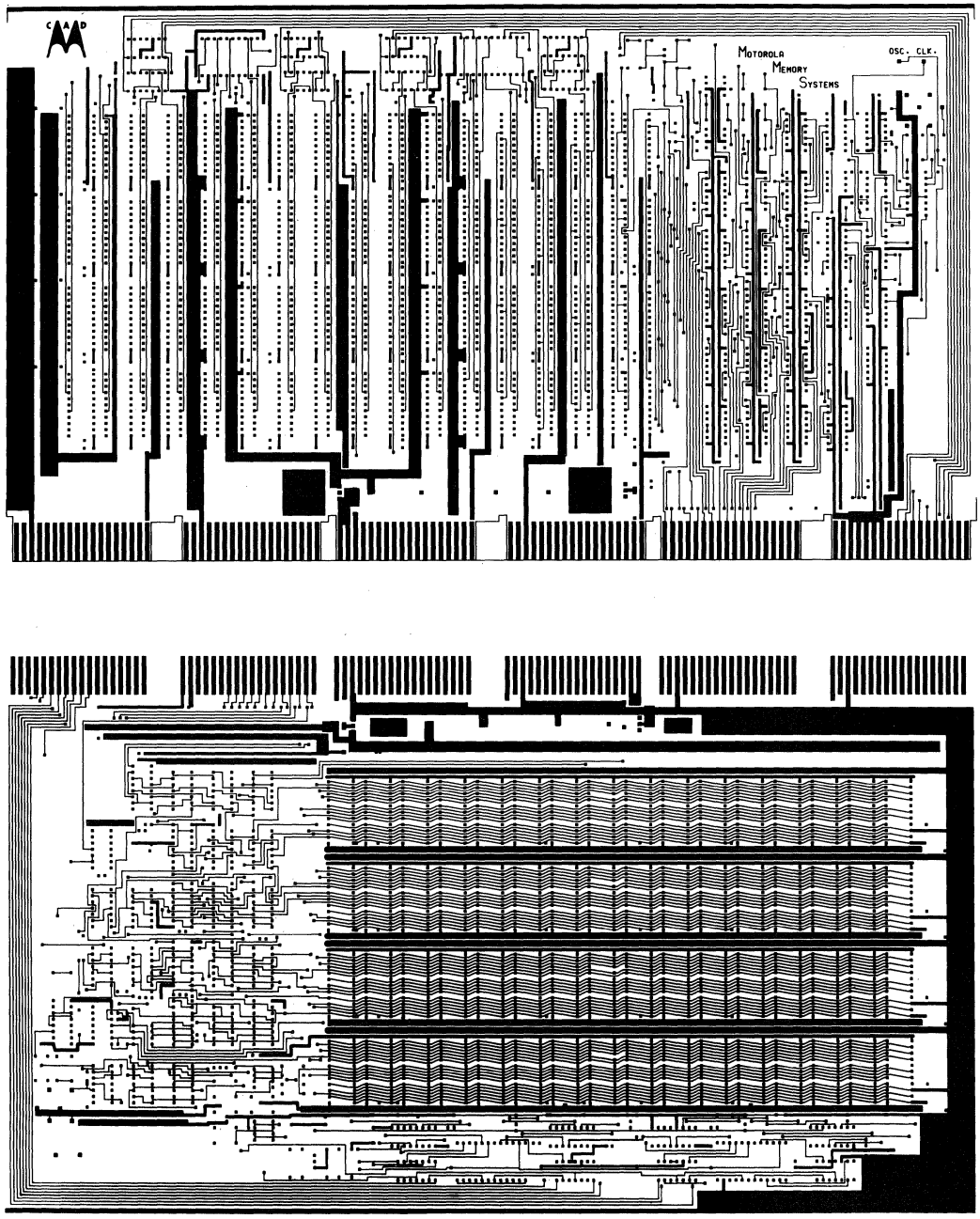

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FIGURE 17 – PC Board Layout of Memory System

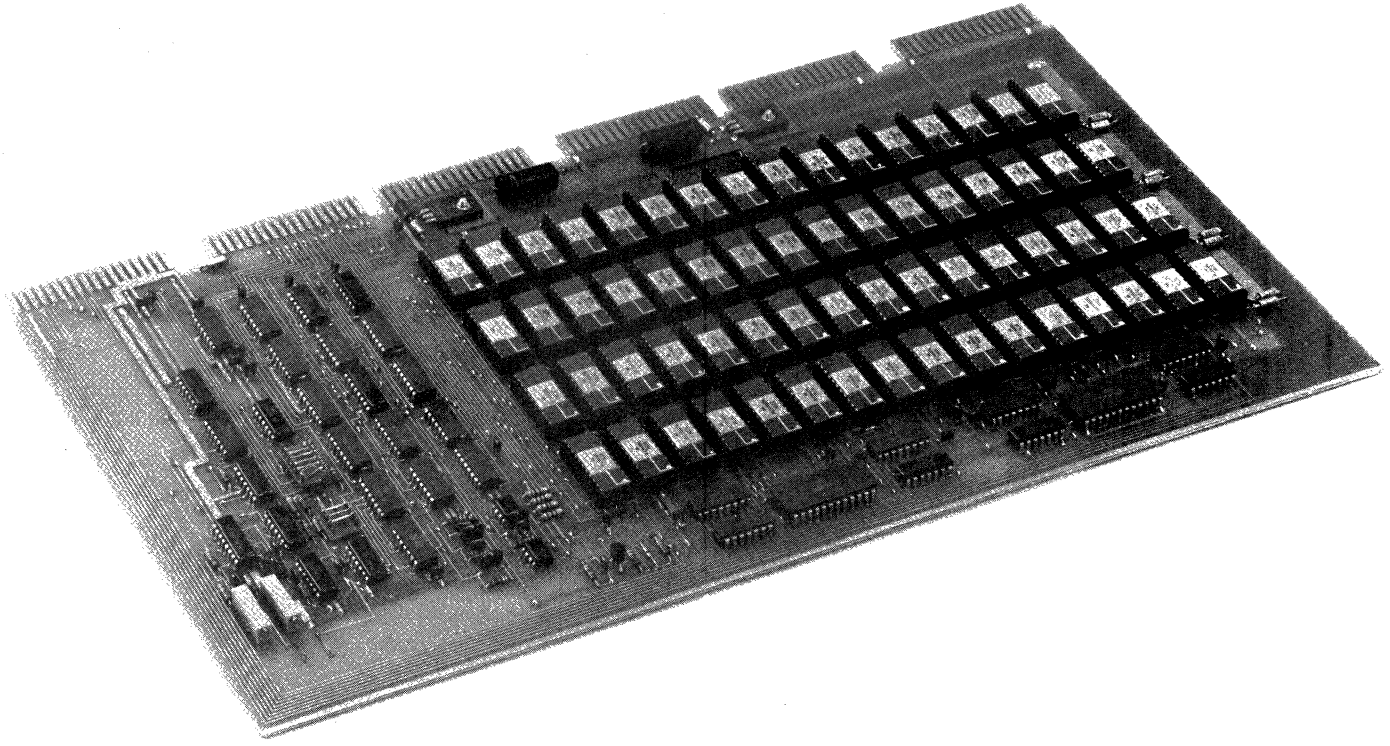


FIGURE 18 – Memory Board

SYSTEM PERFORMANCE

System Access and Cycle Time

The performance of this memory system was measured under program control on the PDP-11 computer. The following cycle times were measured from the 50% point on the leading edge of $\overline{MSYN}$ to the trailing edge of $\overline{SSYN}$ (see Figures 9 and 10).

System Access: 305 ns (from $\overline{MSYN}$ to data valid on the bus)
System Read Cycle: 830 ns
System Write Cycle: 730 ns

A considerable amount of the cycle time is spent by the CPU in acknowledging $\overline{SSYN}$. Some of this wasted time could be used to advantage during a write cycle. That is, the $\overline{SSYN}$ could be sent to the CPU earlier by clocking the $\overline{SSYN}$ latch with a one-shot that has a smaller pulse width than the CE one shot.

System Power Considerations

The MCM6605A is a dynamic RAM that has essentially zero power drain when in the standby mode (CE is a logic "0"). However, when the memory is active, the V_{DD} and V_{BB} supplies have considerable dynamic current transients as noted in Figure 19. To insure that the noise does not exceed 0.35 V on the V_{DD} supply, a low inductance 0.1 μF capacitor is required on the V_{DD} line for every two memory chips. For a 20 ns rise time on the chip enable clock, the bypass capacitors should not be separated more than 1.2 inches. The V_{BB} line requires only one 0.01 μF capacitor for every four memory devices.

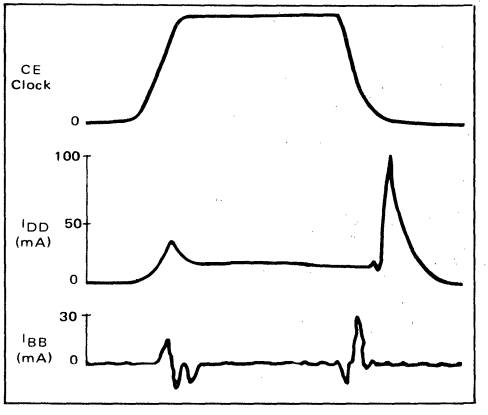


FIGURE 19 – Typical Supply Current Transient Waveforms

The V_{CC} line supplies current only to the output buffer and, therefore, requires only a 0.01 μF bypass for every eight memory chips.

The dc power dissipation of the memory system is given in Table 1. This dc power was measured while running worst-case noise test patterns on the memory systems.

TABLE 1 – Typical Power Requirements for 16K x 16-Bit Memory Board

Power Supply Volts	Standby Power Watts	Active Power Watts
+12 (V_{DD})	0.84	1.10
-5.0 (V_{BB})	0.80	0.80
+5.0 (V_{CC})	4.5	4.75

There are certain data transfers such as direct memory access (DMA) that would greatly increase the V_{DD} power. The following equation can be used to calculate the maximum active V_{DD} power for a DMA type data transfer:

$$P_D = M\left(\frac{MCT}{SCT}\right)(I_{DDA})(V_{DD}) + (N-1)(M) \times \left[\left(\frac{MCT}{T}\right)(I_{DDA})(V_{DD}) + \left(\frac{T-MCT}{T}\right)(I_{DDS})(V_{DD})\right]$$

where: $N = \frac{\text{system word size}}{4096}$

M = number of bits per word
MCT = semiconductor memory cycle time
SCT = system cycle time

$T = \frac{2\text{ ms}}{\text{number of REF cycles}}$

I_{DDA} = active I_{DD} current
I_{DDS} = standby I_{DD} current

Using this equation, the maximum active V_{DD} power for this memory system is 4.46 W. This power figure was determined by using a system cycle time of 830 ns and the following MCM6605A parameters:

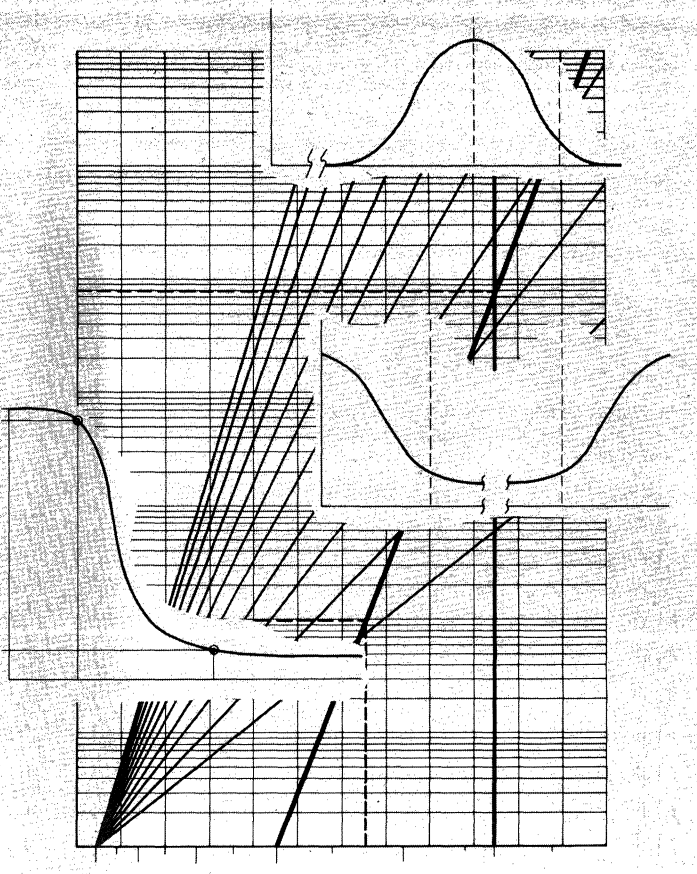
(1) MCT = 490 ns
(2) V_{DD} = 12.6 V
(3) I_{DDA} = 36 mA max
(4) I_{DDS} = 20 μA max
(5) T = 62.5 μs

The calculated power figure does not include the clock driver power. Even with the worst case DMA power figure, the power per bit is extremely favorable compared to other memory systems with comparable performance. In the standby mode with refresh, the average dc power figures taken from Table 1 show a typical 23.4 μW/bit for this system.

SUMMARY

This report has covered the features and operation of the MCM6605A N-channel MOS memory, and the complete design of a PDP-11 memory system employing this device. This design also incorporates some of the newest semiconductor memory interface parts to reduce package count and enhance system performance.

Because of the high density, high speed, and low power of the new 4K RAMs, such as the MCM6605A, they should find rapid and wide acceptance for mainframe memory systems applications such as the one just covered.



Reliability Information/Chapter 6

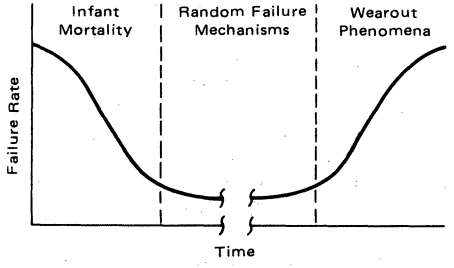
Reliability

Paramount in the mind of every semiconductor user is the question of device performance versus time. After the applicability of a particular device has been established, its effectiveness depends on the length of troublefree service it can offer. The reliability of a device is exactly that — an expression of how well it will serve the customer. The following discussion will attempt to present an overview of Motorola's MOS Reliability efforts.

BASIC CONCEPTS

It is essential to begin with an explanation of the various parameters of reliability. These are probably summarized best in the Bathtub Curve (Figure 1). The reliability performance of a device is characterized by three phases: infant mortality, random failure and wearout. When a device is produced there is often a small distribution of failure mechanisms which will exhibit themselves under relatively moderate stress levels and therefore appear early. This period of early failures, termed infant mortality, can often be reduced significantly through proper manufacturing controls and screening techniques. The most effective period is that in which only occasional random failure mechanisms appear. This typically spans a long period of time with a very low failure rate. The final period is that in which the devices literally wear out due to continuous phenomena which existed at the time of manufacture. Using reasonable design techniques and selectivity in applications, this period can easily be shifted beyond the lifetime required by the user.

FIGURE 1 — THE BATHTUB CURVE



Random Failure

Both the infant mortality and random failure rate regions can be described through the same types of calculations. During this time the probability of having no failures to a specific point in time can be expressed by the equation

$$P_o = e^{-\lambda t}$$

where λ is the failure rate and t is time. Since λ is changing rapidly during infant mortality, the expression does not become useful until the random period, where λ is relatively constant. In this equation λ is failures per unit of time. It is usually expressed in percent failures per thousand hours. Other forms include FIT (Failures In Time = [$\%/10^3$ hrs] x 10^{-4} = 10^{-9} failures per hour) and MTTF (Mean Time To Failure) or MTBF (Mean Time Between Failures), both being equal to $1/\lambda$ and having units of hours.

Since reliability evaluations usually involve only samples of an entire population of devices, the concepts of the Central Limit Theorem apply and λ is calculated using the χ^2 distribution through the equation:

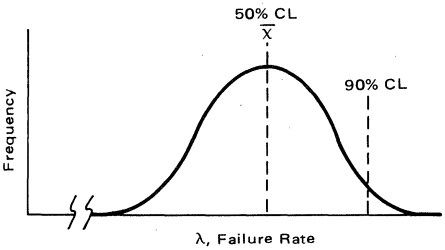
$$\lambda \leqslant \frac{\chi^2\,(\alpha,\ 2r + 2)}{2nt}$$

where $\alpha = \dfrac{100\text{-CL}}{100}$

CL = Confidence Limit in percent
r = Number of rejects
n = Number of devices
t = Duration of test

The confidence limit is the degree of conservatism desired in the calculation. The Central Limit Theorem states that the values of any sample of units out of a large population will produce a normal distribution. A 50% confidence limit is termed the best estimate and is the mean of this distribution. A 90% confidence limit is a very conservative value and results in a higher λ which represents the point at which 90% of the area of the distribution is to the left of that value (Figure 2). The term (2r + 2) is called the degrees of freedom and is an expression of the number of rejects in a form suitable to χ^2 tables.

FIGURE 2 — CONFIDENCE LIMITS AND THE DISTRIBUTION OF SAMPLE FAILURE RATES



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The number of rejects is a critical factor since the definition of rejects often differs between manufacturers. While Motorola uses data sheet limits to determine failures, sometimes rejects are counted only if they are catastrophic. Due to the increasing chance of a test not being representative of the entire population as sample size and test time are decreased, the χ^2 calculation produces surprisingly high values of λ for short test durations even though the true long term failure rate may be quite low. For this reason relatively large amounts of data must be gathered to demonstrate the real long term failure rate. Since this would require years of testing on thousands of devices, methods of accelerated testing have been developed.

Years of semiconductor device testing has shown that temperature will accelerate failures and that this behavior fits the form of the Arrhenius equation:

$$R(t) = R_0(t)e^{-\theta/kT}$$

where $R(t)$ = Reaction rate as a function of time and temperature
R_0 = A constant
t = Time
θ = Activation energy in electon volts
k = Boltzman's constant
T = Temperature in degrees Kelvin

To provide time-temperature equivalents this equation is applied to failure rate calculations in the form

$$t = t_0\, e^{\theta/kT}$$

where
t = time
t_0 = A constant

The Arrhenius equation essentially states that reaction rate increases exponentially with temperature. This produces a straight line when plotted on log-linear paper with a slope expressed by θ. θ may be physically interpreted as the energy threshold of a particular reaction or failure mechanism. The activation energy exhibited by MOS integrated circuits varies from about 0.7 eV for serious contamination problems to about 1.3 eV. Although the relationships do not prohibit devices from having poor failure rates and high activation energies, good performance usually does imply a high θ. Studies by Bell Telephone Laboratories have indicated that an overall θ for semiconductors is 1.0 eV. This value has been accepted by the Rome Air Development Command for time-temperature acceleration in powered burn-in as specified in Method 1015.1 of MIL-STD-883A. Data taken by Motorola on MOS devices has verified this number and it is therefore applied as our standard time-temperature regression for extrapolation of high temperature failure rates to temperatures at which the devices will be used (Figure 3).

To accomplish this, the time in device hours (t1) and temperature (T1) of the test are plotted as point P1. A vertical line is drawn at the temperature of interest (T2) and a line with a 1.0 eV slope is drawn through point P1. Its intersection with the vertical line defines point P2, and determines the number of equivalent device hours (t2). This number may then be used with the χ^2 formula to determine the failure rate at the temperature of interest. Assuming T1 of 125°C at t1 of 10,000 hours, a t2 of 7.8 million hours results at a T2 of 50°C. If one reject results in the 10,000 device hours of testing at 125°C, the failure rate at that temperature will be 20%/1000 hours using a 60% confidence level. One reject at the equivalent 7.8 million device hours at 50°C will result in a 0.026%/1000 hour failure rate, as illustrated in Figure 4.

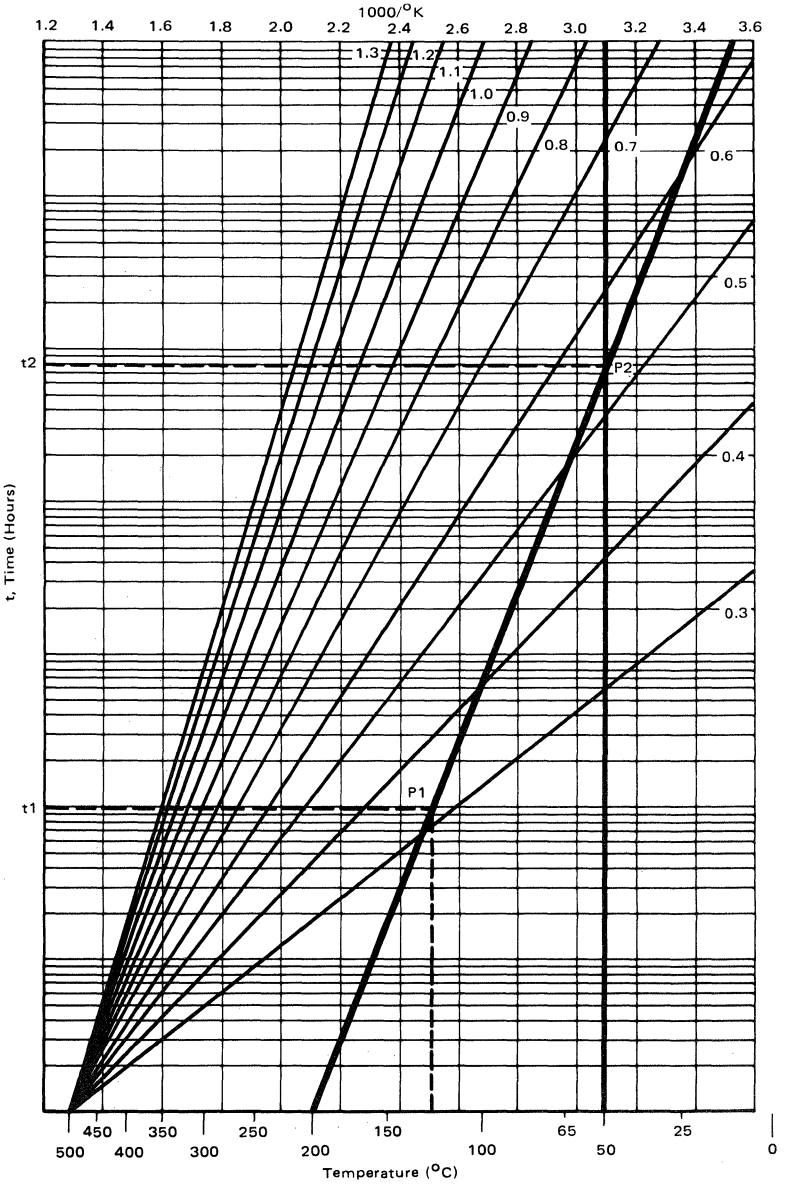
Three parameters determine the failure rate quoted by the manufacturer: the failure rate at the test temperature, the activation energy employed, and the difference between the test temperature and the temperature of the quoted λ. A term often used in this manipulation is the "acceleration factor" which is simply the equivalent device hours at the lower temperature divided by the actual test device hours.

Wearout

Every device will eventually fail, but with reasonable care in design and application the wearout phase can be extended far beyond the lifetime required. During wearout, as in infant mortality, the failure rate is changing rapidly and therefore loses its value. The parameter used to describe performance in this area is "Median Life" and is the point at which 50% of the devices have failed. There are currently only two significant wearout mechanisms: electromigration of circuit metallization and electrolytic corrosion in plastic devices.

Electromigration is the current induced mass transport of metallization due to high temperature and current density. It is strongly affected by the type of metallization as well as the grain structure and surface sealing. It is therefore important that the designer predict the maximum junction temperature of the device, the current on all space limited lines and the process characteristics such as thickness variation, grain size, and step coverage. With these parameters fixed, a median life goal can be selected and the metal width chosen accordingly. Reasonable consideration in the design phase coupled with careful die inspection can therefore eliminate this phenomena as one of practical concern.

FIGURE 3 – NORMALIZED TIME-TEMPERATURE REGRESSIONS FOR VARIOUS ACTIVATION ENERGY VALUES



For increased flexibility in working with a broad range of device hours, the time-temperature regression lines have been normalized to 500°C and the time scale omitted, permitting the user to define the scale based on his own requirements.

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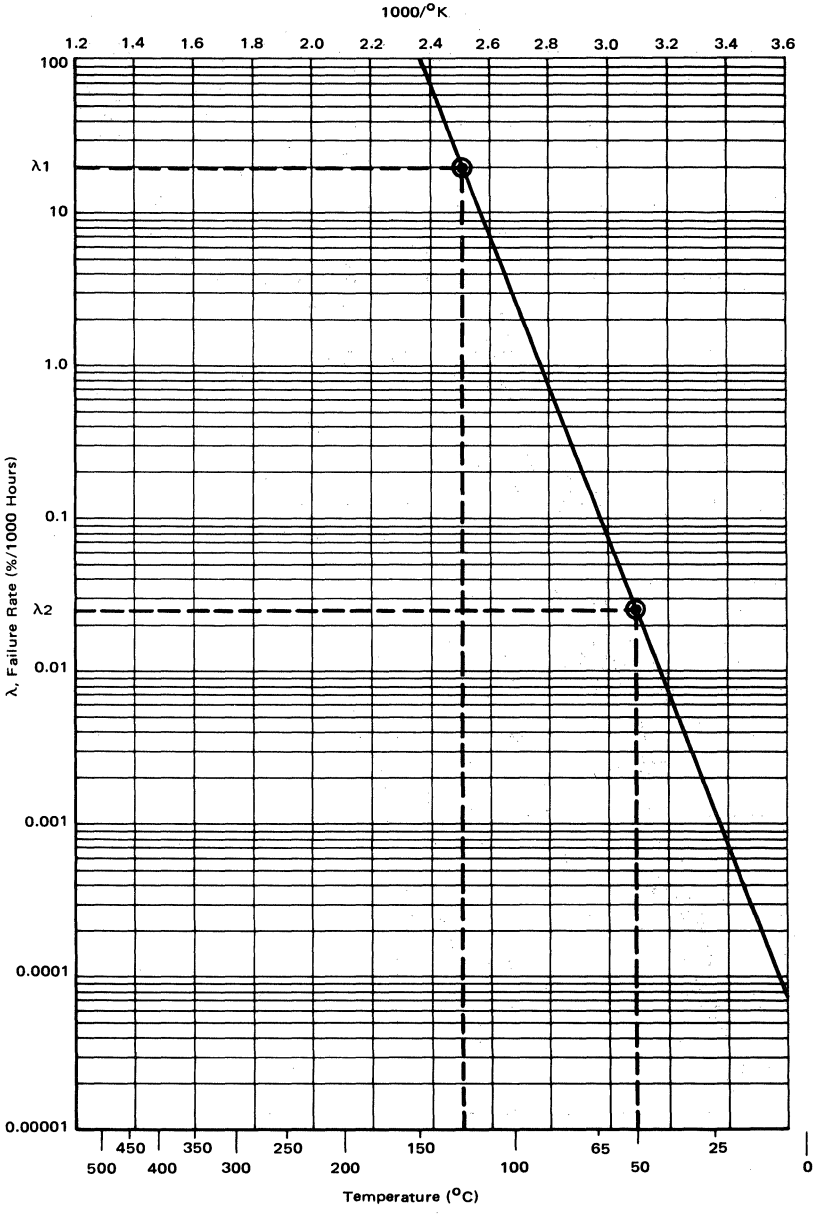
FIGURE 4 – FAILURE RATE



A more pertinent mechanism is the electrolytic corrosion of die metallization by moisture and applied voltage. Although it can occur in hermetic packages which are not properly sealed, hermeticity testing can easily limit it to plastic packaging. In plastic devices there is never enough adhesion between the plastic and the other components to overcome the stresses developed due to differing coefficients of thermal expansion. As a result moisture can enter the device along the interface of the lead frame and the plastic, pass between the surface of the wire and the plastic and reach the surface of the die. If contaminants are present in the water or in the package an electrolyte is created which will corrode the metallization in the presence of an electric field. The median life is determined by many factors such as:

1. Matching of thermal expansion coefficients of the leadframe, wire, die and plastic
2. Purity of the encapsulant
3. Adhesion of the encapsulant
4. Length and width of the leadframe interface
5. Integrity of the final die passivation layer.

Plastic package corrosion is evaluated by exposing the device to extremes of temperature and humidity while under bias. Through consistent bias configurations and control of the environment, temperature-humidity-bias (THB) testing can be an invaluable indicator of performance. Typical test parameters are 85°C and 85% relative humidity. Pressure cooker test and operating tests under tropical conditions are also employed but are more difficult to repeat consistently. The problem with all the tests, however, is the difficulty in relating the results to the environment in which the customer will use the device. To accomplish this a model has been developed which substitutes vapor pressure for temperature in the Arrhenius equation. When available data points are used to adjust the constants, the plot in Figure 5 is the result. Based on several variations of THB conditions and extrapolated performance from burn-in tests, this model provides a good estimate of performance across the range of temperature and humidity environments possible in the customers application.

Sampling Procedures

There are primarily three methods of measuring how well a lot of product meets the quality and reliability requirements of the customer: 100% testing using a Percent Defective Allowable (PDA), sampling based on an Acceptance Quality Limit (AQL), and sampling based on a Lot Tolerance Percent Defective (LTPD). Since 100% testing is time consuming and expensive, sampling procedures are typically employed to assure acceptably low defect levels.

A PDA is simply a reject percentage above which the lot will be rejected. Depending on how the PDA was derived, it may or may not be statistically sound. The availability of theoretically accurate sampling plans in the various military specifications has led to wide use of AQL and LTPD plans. Depending on lot size and sample size, three different probability distributions may be used to derive the sampling plan: the Binomial, the Hypergeometric and the Poisson. The assumptions of a particular sample size (n) and acceptance number (c) and the use of these distributions will generate an Operating Characteristic (OC) Curve as in Figure 6. The AQL is defined at the 95% probability of lot acceptance level while the LTPD is defined at the 10% level. The AQL point describes the Producer's Risk of rejecting good lot (5%) while the LTPD point describes the Consumer's Risk of accepting bad lot (10%) given that the incoming product contains the percent defective p.

FIGURE 5 – VAPOR PRESSURE MODEL

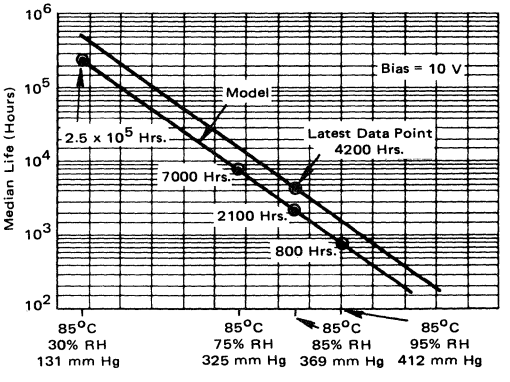
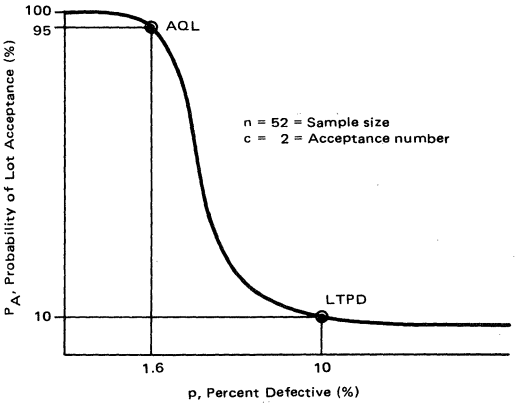


FIGURE 6 – OPERATING CHARACTERISTIC CURVE



It is important to remember that although the concepts of Producer's and Consumer's Risk are utilized to describe AQLs and LTPDs, both are merely indicators of the performance of the original population. Both plans are widely used by manufacturers and users alike. By definition, LTPDs employ fixed sample sizes while AQL plans adjust the sample size according to the lot size. As in the case of failure rate determination, the criteria established to determine rejects and their interpretation are key factors in determining the performance of lots during inspection.

THE SOURCE OF RELIABILITY

One of the most popular sayings about reliability is that it must be "built in", not "tested in". Every manufacturing process exhibits a distribution of quality and reliability. The intent of the saying is that this distribution must be controlled to assure a high mean value, a narrow range and a consistent shape. Through proper design and process control this can be accomplished, thereby reducing the task of screening programs which attempt to eliminate the lower tail of the distribution.

Design

A close interface must be maintained between reliability and design. For this reason a large part of the reliability staff is dedicated to a day by day interface with the device design and modeling groups. Through this mutual effort new techniques are evaluated and proven before they are committed to production. Special test vehicles are generated and experiments performed to verify that the performance of new approaches meets or exceeds the standards of the product line. This effort is not only a beneficial application of reliability but an absolute necessity to provide the rapid product development demanded by the dynamic integrated circuit marketplace.

Processing

In addition to the design interface, reliability engineers work closely with process engineers in both the wafer and assembly areas. As each new process is developed, it is also tested to assure that it presents no hazards to the reliability of the ultimate product. This testing is an extensive qualification program which is performed independently on processes, packages and designs.

New wafer processes are qualified using process control patterns and prototypes of production devices. Each new package is tested using methods based on MIL-STD-883A. Assembly process changes are qualified by employing them in the construction and testing of well characterized products. After these primary level qualifications, wafer processes are generically qualified in new packaging systems to assure process-package compatibility. While assembly oriented qualifications center around the thermal-mechanical sequences of MIL-STD-883A, wafer process qualifications emphasize dynamic high temperature stress testing. (see Figures 7 and 8.)

After testing has proven the performance of the process, it is specified and documented to provide a baseline for process control. Beyond the detailed process control efforts of the process engineering groups, an In-Process Quality Assurance (IPQA) group exists to assure that process control is meeting its objectives. IPQA accomplishes this through surveillance of both the wafer and assembly areas (see Figure 9). There are two major inspection points in the wafer processing areas: CV Plotting and Final Visual. Samples from each wafer lot are stringently tested for voltage shift and inspected for gold backing and visual defects. The three major inspection points in the Assembly Area are Die High Power, Die Bond-Wire Bond and Pre-Cap.

FIGURE 7 – PACKAGE EVALUATION

Test	MIL-STD-883 Test Method	Test Condition
Operating Life	1005	N/A
High Temperature Storage	1008	C
Temperature Cycle	1010	C
Thermal Shock	1011	C
Thermal Resistance	N/A	N/A
Mechanical Shock	2002	B
Constant Acceleration	2001	D
Vibration, Variable Frequency	2007	A
Wire Pull (Hermetic)	2011	D
Temperature-Humidity-Bias (Plastic)	N/A	85°C/85% RH/10V
Moisture Resistance	1004	1
Salt Atmosphere	1009	A
Solderability	2003	260°C
Lead Fatigue	2004	B2
Marking Permanency	2008	B
Physical Dimensions	2008	A

All of these inspection points are known as "Gate Inspections" and are performed on lots of material. Wafers are grouped into lots which generally consist of thirty to fifty wafers while individual devices are grouped into assembly orders consisting of 500 to 2000 devices. Each lot or assembly order is submitted to In-Process Quality Assurance Gate Inspection. If accepted, they are passed to the next operation, while failed material is returned to Production for 100% screening. Only the wafers or devices that meet all established standards are accepted for continued processing.

"Monitor" inspections are performed in the assembly area on each individual machine and operator. The monitors are designed to control the operation, and provide feedback of quality problems to the responsible production supervision. Periodic line audits are used to check for:

1. Documented procedures on each operation
2. Proper usage of specifications
3. Up-to-date calibration of equipment
4. Proper settings on equipment
5. Housekeeping
6. Safety precautions.

Comprehensive training programs are provided for all domestic and off-shore personnel, new plant start-ups, changes in specifications, or process changes. The primary objective is to evaluate the material in process and assure that MOS products meet the levels of reliability and quality which are consistent with the requirements of our customers.

FIGURE 8 – INITIAL EVALUATION OF NEW PRODUCT

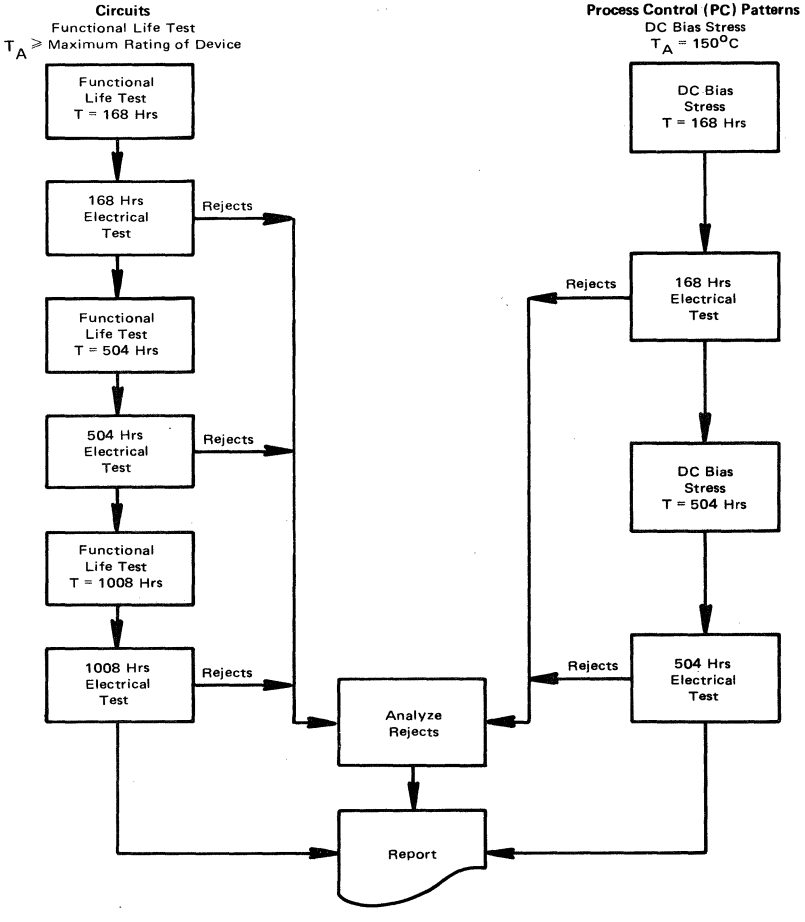
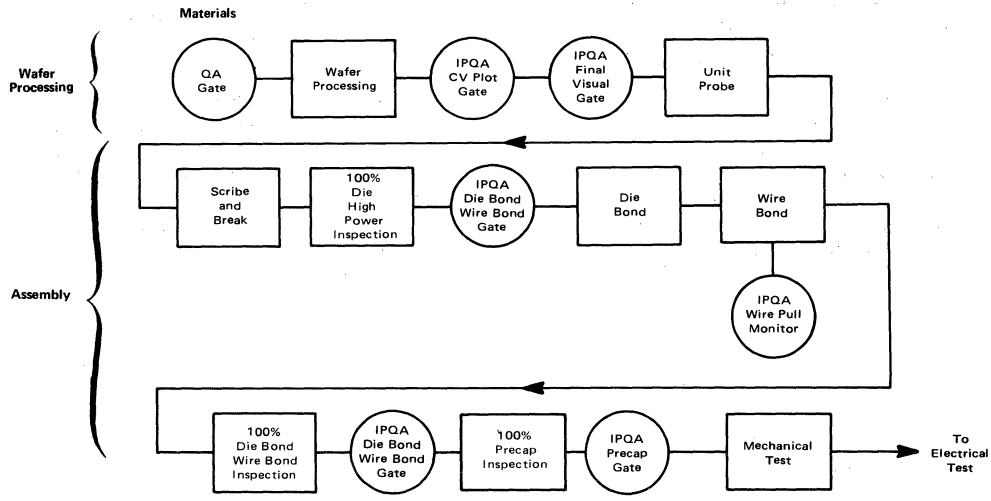


FIGURE 9 – IN-PROCESS QUALITY ASSURANCE FLOW CHART



SCREENING

During the past thirty years that semiconductor products have existed, a wide variety of screening techniques have evolved to eliminate the lower tail of the process distribution discussed previously. These techniques may be categorized in two ways, as illustrated by the two axes of the matrix in Figure 10. The performing agency varies depending on the type and purpose of the test. Most screens utilized by the industry today are based on MIL-STD-883A and are employed by Motorola in the various categories of Figure 10.

Several 100% visual screens are performed during assembly using both stereozoom and metallurgical microscopes. Subsequent sampling is performed by In-Process Quality Assurance as described above. Assembly mechanical tests for hermetic product consist of:

1. Gross leak sampling
2. Temperature cycling
3. Krypton-85 fine leak testing.

Other tests available as adders include stabilization bake and centrifuge. Stabilization bake originated with Mesa transistors which had exposed junctions. The high temperature bake had a significant effect on stabilizing the junction leakage and low current beta. Since integrated circuits have no exposed junctions, Motorola has found no benefit in stabilization bake. The intent of centrifuge is to exert a force on the wire bonds which would detect latent failures. Calculations have shown that even at 30,000 Gs, a higher than normal military requirement, the force on a wire is in the order of 100 mg. This is insignificant compared to a wire pull average of at least 7000 mg. Since each wire bonder is sampled continuously to provide constant control, centrifuge becomes a needless screen. Occasionally die bonds can fail in a centrifuge test, but Motorola controls this factor by employing stringent fillet and wetting criteria in a 100% visual screen enforced by In-Process QA.

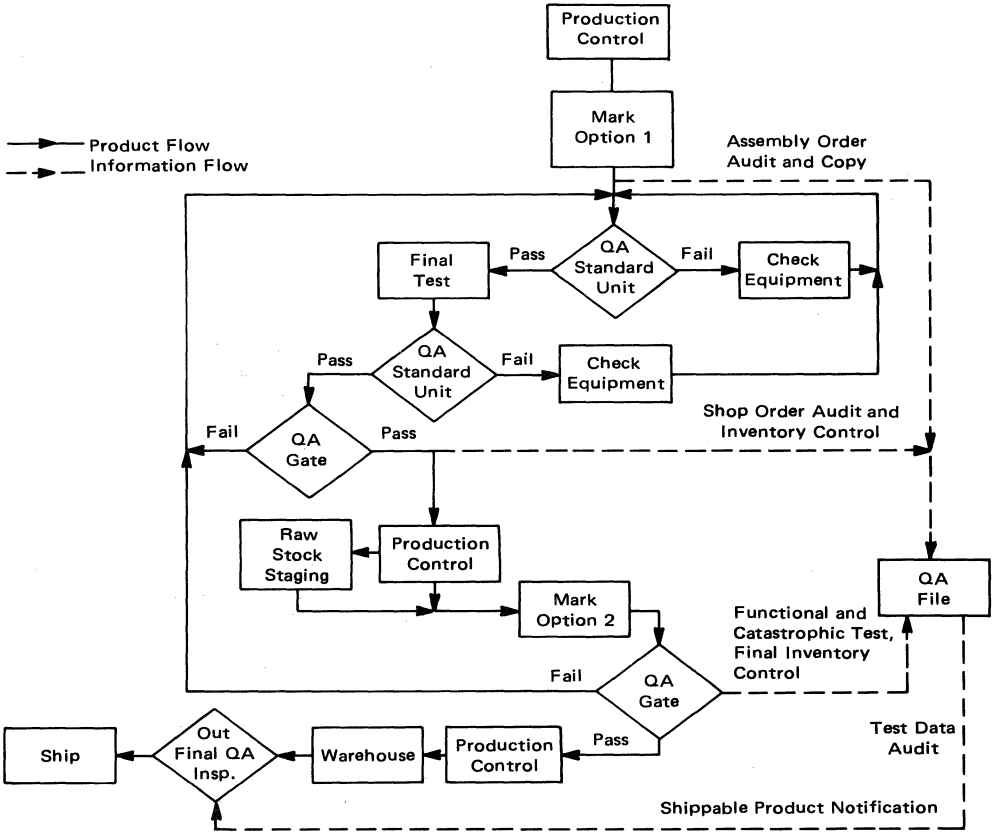
FIGURE 10 – TESTING CATEGORIES

Category	Visual Inspection	Mechanical Testing	Electrical Testing	Environmental Stress
100%	Assembly	Assembly	Final Test	Production Burn-In
Sampling	In-Process QA	In-Process QA Outgoing QA	Outgoing QA	Outgoing QA
Qualification Testing	Reliability Engineering			

Many vendors offer extensive screening programs as an adder. Although some features definitely improve reliability, many are far from cost effective. As in the case of stabilization bake and centrifuge for hermetics, many unnecessary screens are applied to plastic product. Stabilization bake is often touted as a screening procedure for plastics, but this is usually the standard cure cycle through which every plastic device is processed. Temperature cycling and thermal shock are tests commonly employed to test for latent wire bond failures. This was a significant problem when the industry was using aluminum wire on various silicone compounds, and continues to be for those vendors who have not properly balanced the thermal expansion coefficients of the package components. Motorola, like many of the large suppliers, has spent years of research and testing in optimizing its epoxy Novolac plastic package to the extent that temperature intermittence has been virtually eliminated. In addition, recent work by Fitch* has shown that repeated temperature excursions over the military temperature range definitely degrade the THB life of plastic product.

At the end of the assembly process, production final test screens the product with a comprehensive series of dc, functional, and speed oriented electrical tests. These tests are normally more stringent than data sheet requirements and are sampled by Outgoing Quality Assurance. Outgoing QA establishes controls on the equipment, procedures and test programs. Through the use of such monitoring and standard correlation units, this In-Line Quality System (Figure 11) certifies that each unit has been screened to program limits such that all specifications are met or exceeded. Complementing the In-Line systems is a statistical sampling program based on MIL-STD-883A, Method 5005.2. This Group A inspection to Class B levels is detailed in Figure 12.

FIGURE 11 – MOS OUTGOING QUALITY ASSURANCE



*Fitch, William and Carpenter, Marvin: The Effect of Thermal Shock and High Temperature Storage on the Temperature Humidity Bias Life of Plastic Encapsulated TTL Gates, RLC #1239 Motorola Integrated Circuit Reliability Report, Revised February 1975.

FIGURE 12 – GROUP A ELECTRICAL TESTS[1]

Subgroups [2]	Class B LTPD	AQL
Subgroup 1 Static tests at 25°C	5/2	0.78
Subgroup 2 Static tests at maximum rated operating temperature	7/2	1.1
Subgroup 3 Static tests at minimum rated operating temperature	7/2	1.1
Subgroup 4 Dynamic tests at 25°C	5/2	0.78
Subgroup 5 Dynamic tests at maximum rated operating temperature	7/2	1.1
Subgroup 6 Dynamic tests at minimum rated operating temperature	7/2	1.1
Subgroup 7 Functional tests at 25°C	5/2	0.78
Subgroup 8 Functional tests at maximum and minimum rated operating temperatures	10/2	1.6
Subgroup 9 Switching tests at 25°C	7/2	1.1
Subgroup 10 Switching tests at maximum rated operating temperature	10/2	1.6
Subgroup 11 Switching tests at minimum rated operating temperature	10/2	1.6

1 The specific parameters to be included for tests in each subgroup shall be as specified in the applicable procurement document. Where no parameters have been identified in a particular subgroup or test within a subgroup, no Group A testing is required for that subgroup or test to satisfy Group A requirements.

2 A single sample may be used for all subgroup testing.

In addition to these two programs, all MOS product lines are monitored continuously via an MOS Ongoing Reliability Evaluation (MORE) Program for mechanical, environmental and operating life performance. This program evaluates the most recently manufactured product on a scheduled basis with methods derived from MIL-STD-883A (see Figure 13). MORE provides current generic data for process control feedback and, just as important, a "no charge" assurance of compliance to military quality standards for all MOS products.

When necessary, production burn-in is performed on particular device types. Burn-in procedures are always available at competitive adders. Qualification testing by Reliability Engineering has been described, and Motorola's reliability data is presented in the following section.

SYSTEM IMPLEMENTATION

Assessing System Requirements

The reliability needs of each system and application differ significantly, so the various aspects of component performance must be analyzed separately. The two parameters which should be addressed initially are infant mortality and long term random failure rate. Systems with large numbers of components require greater component reliability. Infant mortality should be estimated and used to calculate service costs. This data should be balanced against the cost of a functional burn-in and possibly a board or system burn-in. Long term reliability goals should be established for the system and used to calculate the necessary long term failure rate for the components. Long term failure rates cannot be effectively improved by short burn-ins unless they include infant mortality failures. (Infant mortality is included in Motorola's data.) Infant mortality can be effectively screened by short term accelerated stress testing such as a 24 to 48 hour high temperature functional burn-in. The concepts defined earlier can be used to relate the burn-in to equivalent system hours. Often, customers who are experiencing problems fail to distinquish between infant mortality, long term reliability and wearout. It is imperative that failure patterns be sufficiently investigated and recorded to accomplish this. Buying a Hi Rel device will not solve a problem caused by poor handling or an unforseen overstress in the application.

The system environment should be given careful consideration when choosing between plastic and hermetic packages. Sustained high temperature and humidity will accelerate the corrosion

wearout mechanism in plastic according to the model in Figure 5. Office environments, however, will rarely produce a detectable difference in plastic and hermetic packages. Since the die and wire bonding systems are totally encapsulated in plastic, these packages can often outperform hermetics for both thermal conductivity, and mechanical shock and vibration resistance. The potential for moisture condensation should be evaluated in light of the lead material and finish, whether the package is hermetic or plastic. Unusually moist or contaminated atmospheres can rapidly corrode ferrous metals under bias, regardless of the finish material.

Cost effectiveness is also influenced by the number of defective units received by the customer. For various reasons, a small percentage of product is defective as received. This may be due to handling, correlation, shipping damage or a host of minor difficulties. The percentage of these defects should be less than one percent and any significant levels should be discussed with the vendor immediately.

Comparing Competitors' Data

Every manufacturer has a slightly different method of generating his reliability data. It is therefore difficult for a user inexperienced in reliability calculations to make a valid comparison. Toward this end the concepts introduced earlier will be of great value. The following list should be verified before any conclusions of vendor superiority are drawn.

1. Confidence limit
2. Reject criteria (degradation, data sheet, functional, catastrophic, specific mechanisms)
3. Temperature of test
4. Activation energy
5. Distortion of failure rate due to a low number of device hours
6. Biasing configuration
7. Test monitoring (system failures can produce impressive results due to less stringent stress being applied to the device).

Only if all these factors are considered can a truly objective comparison be made.

FIGURE 13A – PRODUCTION LINE PROCESS EVALUATION
(Independent of package unless otherwise noted)

Test	Condition or Procedure
Subgroup A1 Electrical dc and Functional	All parameters per detail device specification at 25°C ± 5°C. (Go/No go)
Subgroup A2 Electrical dc and Functional	Critical parameters per detail device specification at minimum and maximum rated operating temperature. (Go/No go)
Subgroup A3 Electrical Switching	Critical switching parameters per detail device specification at 25°C ± 5°C. (Go/No go)
Subgroup A4 Electrical Continuity	Plastic package only; all pins at 125°C. (Go/No go)
Subgroup C1 Storage Life	1000 hours at maximum rated storage temperature.
End Points: Electrical	Functional and dc at 25°C ± 5°C; read and record at 168 hours, 500 hours, 1000 hours, and each 1000 hours until termination.
Subgroup C2 Operating Life or Steady State Bias	1000 hours minimum at maximum rated operating temperature. Conditions specified per device type in 12MRB06389A.
End Points: Electrical	Functional and dc at 25°C ± 5°C; read and record at 168 hours, 500 hours, 1000 hours, and each 1000 hours until termination.
Subgroup C3 Accelerated Steady State Life	48 hours minimum at 200°C static. Burn-in circuit per 12MRB06389A (CMOS ceramic only).
End Points: Electrical	Functional and dc parameters at 25°C ± 5°C. Read and record.

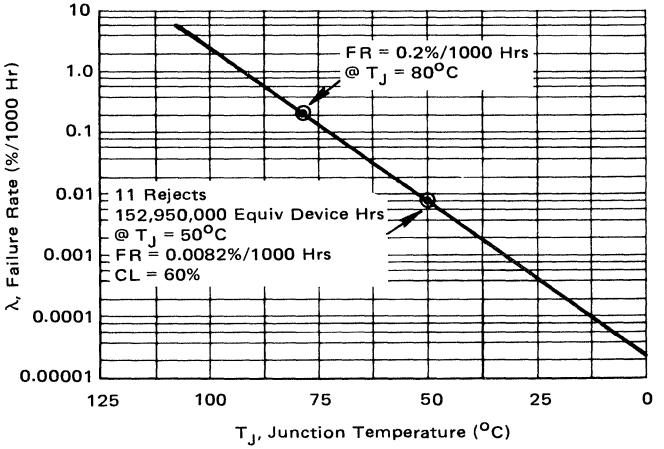
FIGURE 13B – HERMETIC PACKAGE EVALUATION

Test	Method	MIL-STD-883A Condition or Procedure
Subgroup B1		
Solderability	2003.1	Temperature = 260°C maximum. Omit Aging.
Subgroup B2		
Lead Fatigue	2004.1	Condition B2
Subgroup B3		
Seal	1014.1	
a. Fine		Condition B
b. Gross		Condition C2. Omit vacuum of Step 2.
Subgroup B4		
Physical Dimensions	2016	Per case outline drawing
Subgroup B5		
Marking Permanency	2015	Resistance to solvent
Subgroup B6		
Bond Strength	2011.1	Test Condition D
Subgroup C1		
Thermal Shock	1011.1	Condition B (15 cycles)
Temperature Cycle	1010.1	Condition C (30 cycles)
End Points:		
Seal	1014.1	
a. Fine		Condition B
b. Gross		Condition C2. Omit vacuum of Step 2.
Continuity	–	All pins at 25°C ± 5°C
Visual	–	Any crack at 10X magnification
Subgroup C2		
Mechanical Shock	2002.1	Condition B (Y1 axis only)
Vibration, Variable Frequency	2007	Condition A (Y axis only)
Constant Acceleration	2001.1	Condition E (Y1 axis only)
End Points:		
Seal	1014.1	
a. Fine		Condition B
b. Gross		Condition C2. Omit vacuum of Step 2.
Continuity	–	All pins at 25°C ± 5°C
Visual	–	Any crack at 10X magnification
Subgroup C3		
Salt Atmosphere	1009.1	Condition A

FIGURE 13C – PLASTIC PACKAGE EVALUATION

Test	Method	MIL-STD-883A Condition or Procedure
Subgroup B1		
Solderability	2003.1	Temperature = 260°C ± 10°C. Omit Aging.
Subgroup B2		
Lead Fatigue	2004.1	Condition B2
Subgroup B4		
Physical Dimensions	2016	Per case outline drawing
Subgroup B5		
Marking Permanency	2015	Resistance to solvent
Subgroup C1		
Thermal Shock	1011.1	Condition A (15 cycles)
Temperature Cycle	1010.1	Condition A (15 cycles)
End Points:		
Continuity	–	All pins at 125°C ± 5°C
Visual	–	Any crack at 10X magnification
Subgroup C2		
Mechanical Shock	2002.1	Condition B (Y1 axis only)
Vibration, Variable Frequency	2007	Condition A (Y axis only)
Constant Acceleration	2001.1	Condition E (Y1 axis only)
End Points:		
Continuity	–	All pins at 125°C ± 5°C
Visual	–	Any crack at 10X magnification
Subgroup C3		
Salt Atmosphere	1009.1	Condition A
Subgroup C4		
Temperature/Humidity/Bias	–	85°C/85% RH/10 V
End Points:		
DC and Functional	–	25°C Go/No go. Read and record rejects at 168 hours, 500 hours, 1000 hours, 1250 hours, 1500 hours.
Continuity	–	All pins at 125°C

FIGURE 14 – MEMORY FAILURE RATE



Motorola Data

Motorola MOS failure rates are generated by dynamic high temperature stress testing at the maximum ratings of the device, or higher. A 60% confidence level is employed in the standard χ^2 calculation and the Arrhenius model, with a 1.0 eV activation energy, is used to extrapolate the data to typical operating temperatures. 1.0 eV was chosen based on the work done at Bell Telephone Laboratories, its acceptance by the Rome Air Development Command for MIL-STD-883A, and its consistency with our MOS data. Since junction temperature is the most meaningful parameter for reliability data, the failure rate curves are constructed from extrapolations to 80°Cand 50°C T_J (see Figure 14).

Wafer process variations are continuously monitored by classification probe and capacitance voltage testing in the wafer area, and by MORE sampling in Outgoing Quality Assurance. In addition to this, a system of periodic reliability tests is being implemented with Process Control patterns to establish the process distribution and track significant variations. Current tests with 15 V static bias at 150°C for 500 hours produced the plots of threshold stability shown in Figure 15.

In an effort to investigate system reliability of the MCM6605AL, 32K bytes of core in a PDP-11-15 minicomputer were replaced with 64 of the dynamic, N-channel, silicon gate memories. The memory board was then exposed to 70°C in a temperature-controlled environment ($T_J \approx 80°C$) with the following (worst-case) voltage conditions: V_{DD} = 11.4 V, V_{CC} = 4.5 V and V_{BB} = -4.75 V. The system was programmed to monitor the memory board with a comprehensive and sensitive series of patterns. After more than 1300 hours of continuous operation there were no failures. A second test under more stringent refresh conditions has performed for 660 hours with no failures.

An ongoing improvement program has produced impressive results in plastic package temperature-humidity-bias performance. Based on CMOS testing, the Weibull plots of Figure 16 demonstrate this trend. There is a full two fold increase in median life since the data used to generate the vapor pressure model in Figure 5. Although it is not known if a parallel shift of this curve to the latest 85/85 results (ML = 4200 hours) is justified, the extrapolated performance to normal environments is impressive.

FIGURE 15– PROCESS CONTROL PATTERN THRESHOLD STABILITY TESTS

(PC-78, From MCM6605A Wafer; $V_{TO} = 2(V1) - V2$, I1 = 10 μA, I2 = 40 μA)

Fig. 15a — Test Fixture

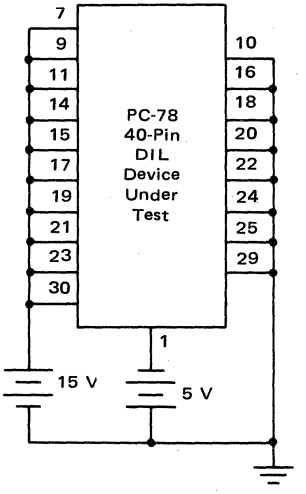


Fig. 15b — Small Device #1

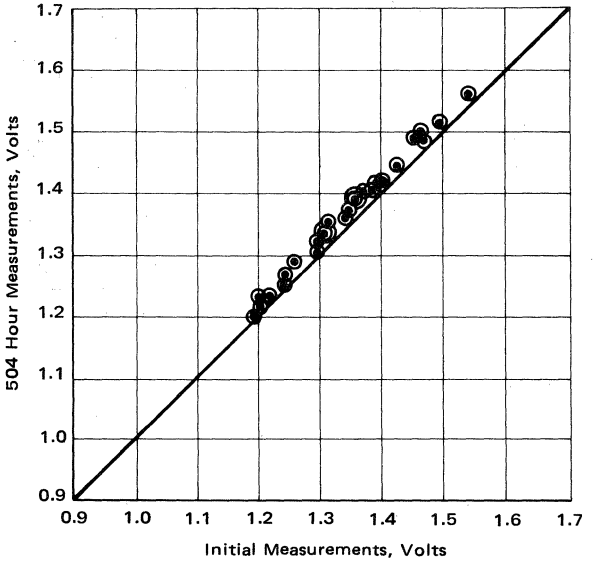


Fig 15c — Small Device #2

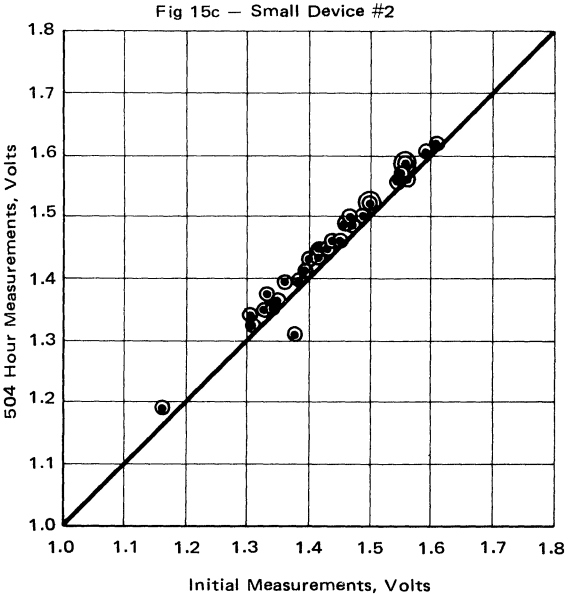


Fig. 15d — Large Device

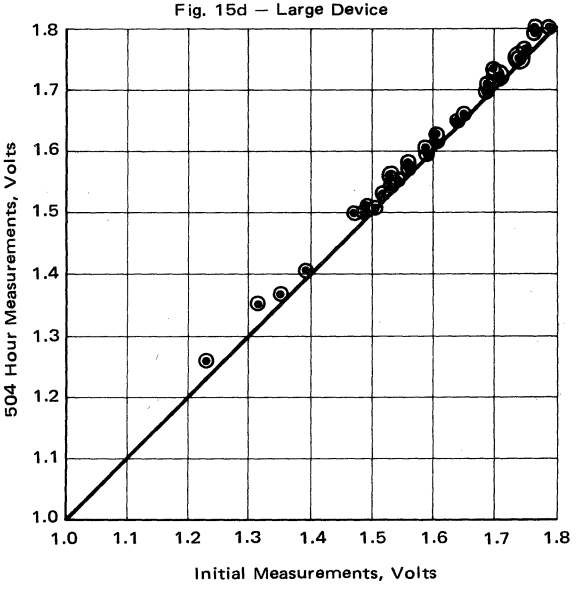
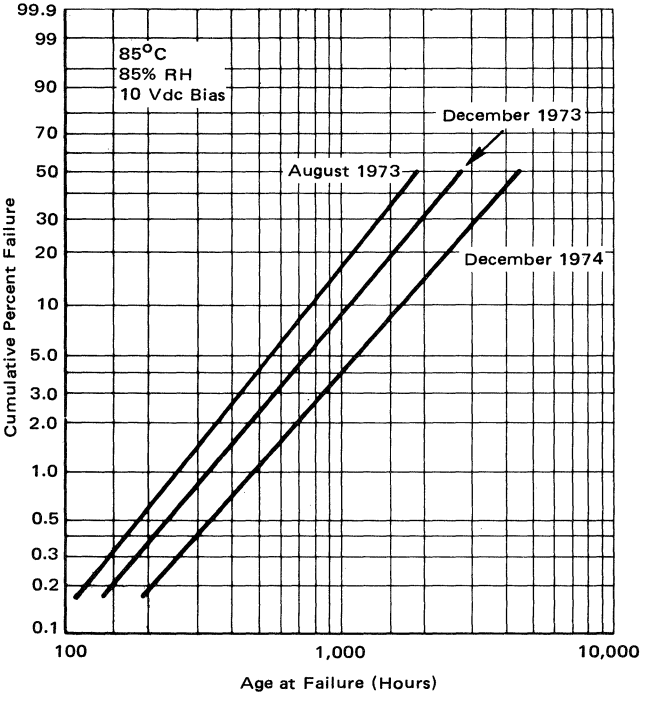


FIGURE 16 – PERFORMANCE HISTORY (TEMPERATURE HUMIDITY BIAS, WEIBULL PROBABILITY)



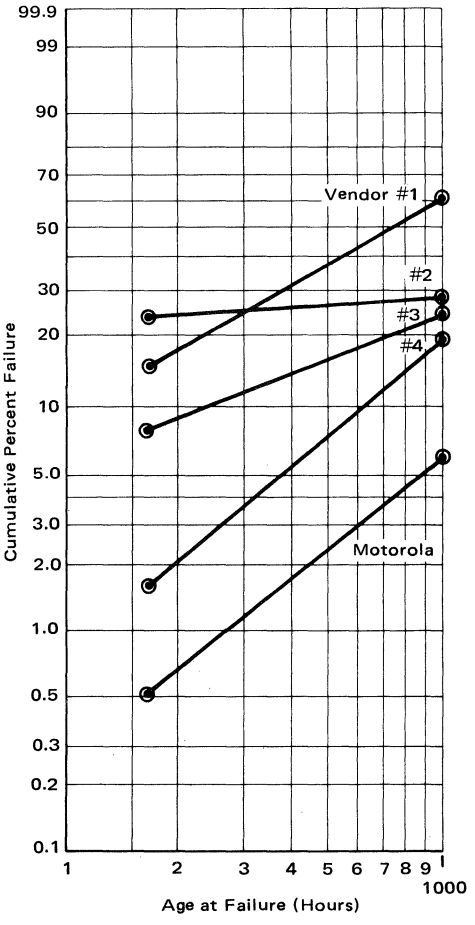
Periodically samples of competitors' product bought from distributors are tested with Motorola methods. To date no other vendor has performed as well as Motorola (see Figure 17). This data was gathered on CMOS product, but is an excellent indicator of the Motorola plastic packaging system. Testing of LSI devices under THB conditions is more difficult since static bias does not stress internal circuitry and cannot be easily related to field use. On the other hand, dynamic bias at even low frequencies is often degraded beyond meaningful levels by board leakage due to condensation. Establishing valid THB models for LSI is an industry wide problem and programs are currently underway at Motorola to bridge the gap between testing and field performance.

Proper evaluation of rejects and feedback to processing can occur only through intensive failure analysis. To support the processing areas, product groups and R & QA, a Product Analysis Laboratory exists. "State-of-the-art" analytical tools are at its disposal including mass spectrometry, Auger, electron microprobe, scanning electron microscopy (with voltage contrast strobe capability) and others too numerous to mention. This capability is complemented by computer tracking systems to evaluate failure patterns and distributions. A simplified example is illustrated in the bar chart of Figure 18.

Detailed information on specific device types is available through individual reliability reports. This series also includes program plans, CMOS and N-Channel generic reports and a plastic packaging report.

FIGURE 17 – VENDOR COMPARISON

A – Temperature Humidity Bias



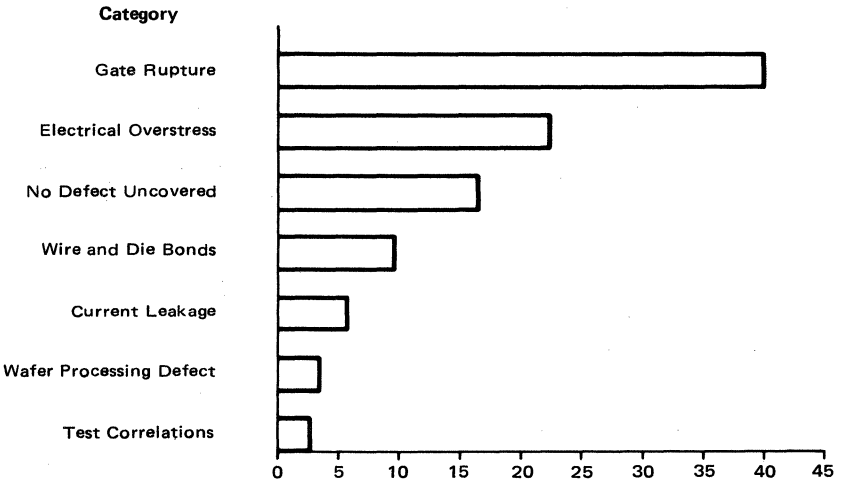
B – Other Testing

Vendor	1000 Hour Burn-In % Failure	Thermal Shock and Temperature Cycling
1	5.7	0
2	44.0	13.3
3	40.0	0
4	12.0	1.8
Motorola	2.3	0

Processing and Handling

No matter how good the reliability data, screening procedures, or incoming inspection, devices are still subject to degradation or destruction by processing and handling. All MOS vendors use input protection devices and most perform well, but there is no device which totally protects the circuit against all conditions. Most users are familiar with good static prevention procedures, but there are few, if any, who could not have prevented a small percentage of in-process failures by a careful review of their assembly lines. Every point at which a MOS device is handled apart from its conductive foam or rail should be evaluated. Conductive work surfaces and wrist straps (making contact with skin) should be tied to ground through a nominal one megohm resistor. Test equipment should be checked to assure grounded sockets during insertion and the absence of voltage spikes. Printed circuit board handling should be consistent with device handling using conductive bags or edge connectors. Conformal coating processes (which can extend the application range of plastic) or cleaning procedures should not be overlooked as possible sources of difficulty. Service personnel should be educated in handling procedures since even when service is completed successfully, valuable failure information can be masked by static damage. With reasonable effort very little static damage can be expected, but considering the higher cost of LSI, a review is always worthwhile.

FIGURE 18 – FAILURE CAUSE



Improper board cleaning procedures can often degrade plastic product performance. High purity flourocarbon systems are preferred to water based systems which can more easily introduce contaminants, particularly in the presence of wetting agents. Cooling the device during the clean or pressurized systems can also enhance the entrance of moisture and contaminants into the package along the lead-plastic interface. Even if contaminants are not present, a thorough bake should be performed to prevent premature introduction of an electrolyte.

CONCLUSION

This discussion has attempted to educate the user with the pertinent concepts of reliability, quality assurance, vendor selection and product use. Motorola's reputation for reliability and customer support has been established by the philosophy of its leadership and is being perpetuated through the efforts of MOS Reliability and Quality Assurance. Customer assistance is always available through sales offices, marketing or R & QA personnel directly.

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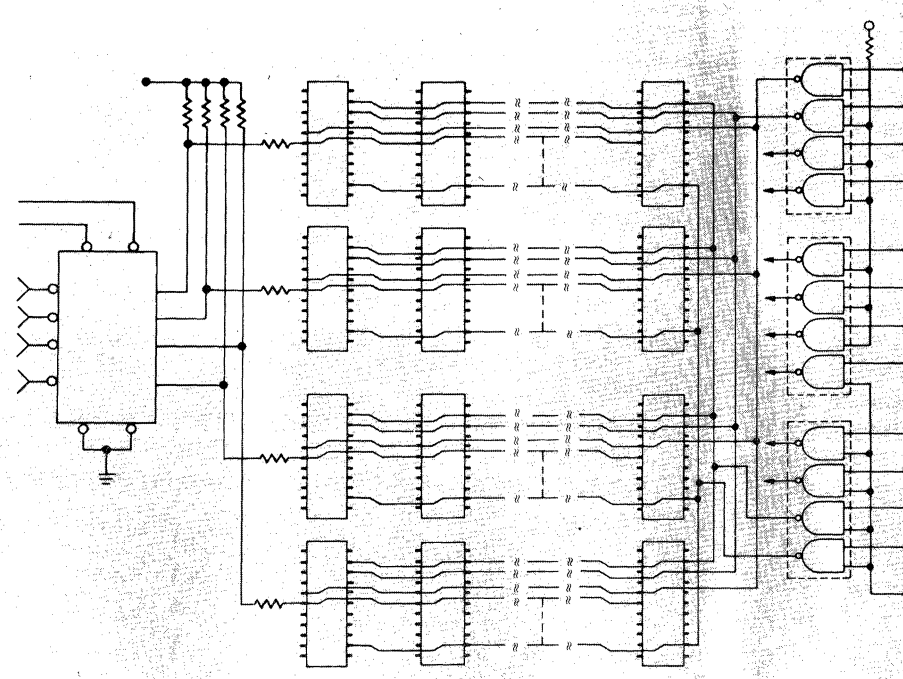


Memory Interface/Chapter 7

INTRODUCTION

Probably nowhere else has semiconductor technology achieved greater complexities and higher circuit densities in practical, real-world products than in today's advanced NMOS memories. These devices permit greater memory capacity per unit volume and lower costs per bit than imaginable only a few years ago.

However, these memory IC's do not function alone. As an approximate rule of thumb, for each three memory packages in a typical system, one package of support interface circuitry is required. Some memory IC's require only low-voltage address and control line drivers and higher-voltage clock drivers. Other types require a sense amplifier in addition to the drivers.

The address and clock drivers are necessary since the inputs to MOS memories appear as highly capacitive loads and substantial peak currents are required to charge or discharge this capacitance rapidly. These currents are generally in excess of that available from standard logic gates.

The output from these MOS memories is generally a low level pulse which requires amplification and buffering to make it compatible with logic systems. The sense amplifier can be constructed of MOS devices and placed on the chip with the memory cells or left to the system engineer to provide bipolar interface circuitry, as is generally the case in the older generation memories or the new higher-speed types.

Motorola continuously studies the advancing memory field, along with new technologies and architectures, to define new drivers and sense amplifiers to meet the coming needs of memory systems.

MC3459

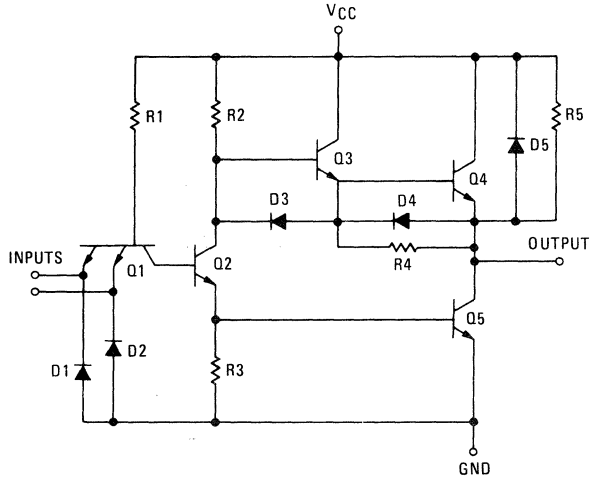
Specifications and Applications Information

QUAD NMOS MEMORY ADDRESS DRIVER

The MC3459 is designed for high-speed driving of the highly capacitive Address select inputs for NMOS Memories. It is also useful in numerous applications requiring a high-current MTTL NAND gate. It is pin-compatible with the popular MC7400 Quad NAND gate.

- Fast Propagation Delay Time – 20 ns Typical with 360 pF Load
- Output Voltages Compatible with NMOS Memories
- Inputs Compatible in MTTL and MDTL Logic Families
- Output Loading Factor – 50

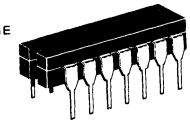
REPRESENTATIVE CIRCUIT SCHEMATIC
(1/4 of Circuit Shown)

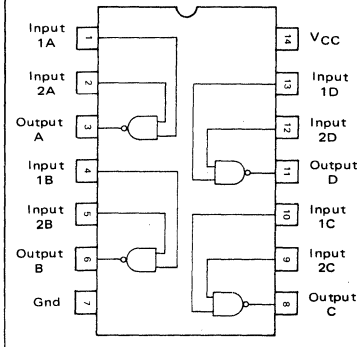


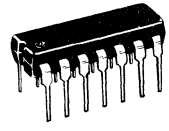
QUAD NMOS ADDRESS LINE DRIVER

SILICON MONOLITHIC INTEGRATED CIRCUIT

L SUFFIX
CERAMIC PACKAGE
CASE 632
TO-116

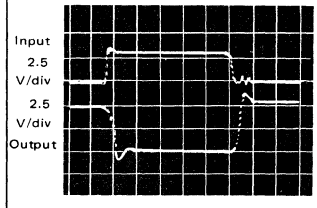






P SUFFIX
PLASTIC PACKAGE
CASE 646

TYPICAL OPERATION



V_{CC} = 5.0 V, T_A = 25°C, 50 ns/div, C_L = 360 pF, R_S = 0 Ω

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	8.5	Vdc
Input Voltage	V_I	5.5	Vdc
Power Dissipation (Package Limitation			
Ceramic Package @ T_A = 25°C	P_D	1000	mW
Derate above T_A = 25°C	$1/R_{\theta JA}$	6.6	mW/°C
Plastic Package @ T_A = 25°C	P_D	830	mW
Derate above T_A = 25°C	$1/R_{\theta JA}$	6.6	mW/°C
Ceramic Package @ T_C = 25°C	P_D	3.0	Watts
Derate above T_C = 25°C	$1/R_{\theta JC}$	20	mW/°C
Plastic Package @ T_C = 25°C	P_D	1.8	Watts
Derate above T_C = 25°C	$1/R_{\theta JC}$	14	mW/°C
Operating Ambient Temperature Range	T_A	0 to 70	°C
Junction Temperature	T_J		°C
Ceramic Package		175	
Plastic Package		150	
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (Unless otherwise noted, 4.75 V ≤ V_{CC} ≤ 5.25 V and 0 ≤ T_A ≤ 70°C)

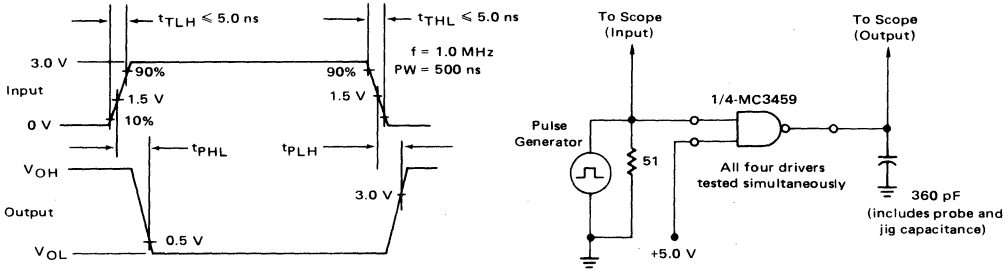
Characteristic	Symbol	Min	Typ(1)	Max	Unit
Input Voltage – High Logic State	V_{IH}	2.0	–	–	V
Input Voltage – Low Logic State	V_{IL}	–	–	0.8	V
Input Current – High Logic State					
(V_{CC} = 5.25 V, V_{IH} = 2.4 V)	I_{IH1}	–	–	80	μA
(V_{CC} = 5.25 V, V_{IH} = 5.5 V)	I_{IH2}	–	–	2.0	mA
Input Current – Low Logic State	I_{IL}	–	–	-3.6	mA
(V_{CC} = 5.25 V, V_{IL} = 0.4 V)					
Input Clamp Voltage	V_{IC}	–	–	-1.5	V
(I_{IC} = -12 mA)					
Output Voltage – High Logic State					V
(V_{CC} = 4.75 V, V_{IL} = 0.8 V, I_{OH} = -640 μA)	V_{OH1}	3.2	–	–	
(V_{CC} = 4.75 V, V_{IL} = 0.8 V, I_{OH} = -2.0 mA)	V_{OH2}	2.4	–	–	
Output Clamp Voltage	V_{OC}	–	5.8	6.75	V
(V_{CC} = 5.25 V, V_{IL} = 0 V, I_{OC} = 5.0 mA)					
Output Voltage – Low Logic State					V
(V_{CC} = 4.75 V, V_{IH} = 2.0 V, I_{OL} = 640 μA)	V_{OL1}	–	–	0.3	
(V_{CC} = 4.75 V, V_{IH} = 2.0 V, I_{OL} = 80 mA)	V_{OL2}	–	–	0.7	
Power Supply Current – Outputs High Logic State	I_{CCH}	–	12	18	mA
(V_{CC} = 5.25 V, V_{IL} = 0 V)					
Power Supply Current – Outputs Low Logic State	I_{CCL}	–	85	122	mA
(V_{CC} = 5.25 V, V_{IH} = 5.0 V)					

SWITCHING CHARACTERISTICS (Unless otherwise noted, V_{CC} = 5.0 V, T_A = 25°C, C_L = 360 pF)

Characteristic	Symbol	Min	Typ	Max	Unit
Propagation Delay Time – High to Low Logic State	t_{PHL}	–	21	32	ns
Propagation Delay Time – Low to High Logic State	t_{PLH}	–	16	26	ns

(1) Typical values measured at T_A = 25°C, V_{CC} = 5.0 V.

FIGURE 1 – TEST CIRCUIT AND WAVEFORMS FOR PROPAGATION DELAY TIMES



TYPICAL PREFORMANCE CURVES

FIGURE 2 – POWER CONSUMPTION versus OPERATING FREQUENCY

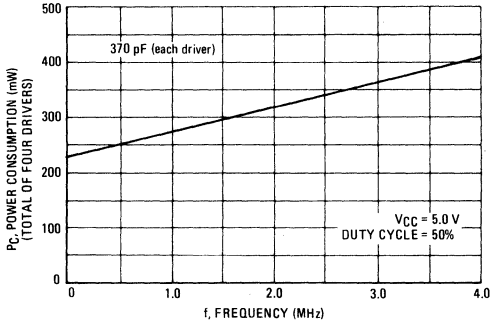


FIGURE 3 – OUTPUT VOLTAGE – HIGH LOGIC STATE versus OUTPUT CURRENT

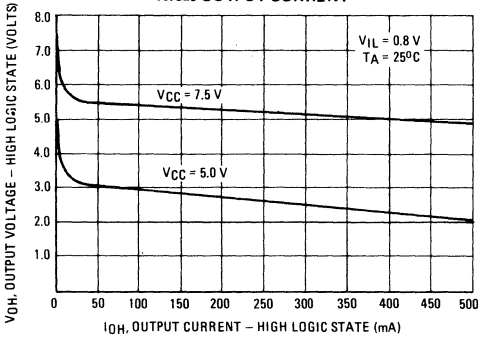


FIGURE 4 – OUTPUT VOLTAGE – HIGH LOGIC STATE versus OUTPUT CURRENT (Expanded Scale)

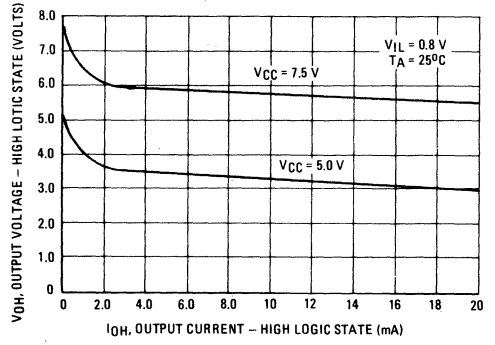
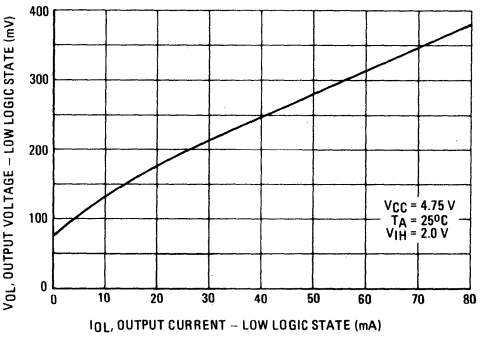


FIGURE 5 – OUTPUT VOLTAGE – LOW LOGIC STATE versus OUTPUT CURRENT



7

APPLICATIONS SUGGESTIONS

A majority of the new N-Channel MOS memories have TTL logic compatible inputs that exhibit extremely low input current and capacitance (typically 5 pF to 10 pF). However, in a typical memory system (Figure 6) where some of the inputs such as Address lines have to be common, the total parallel input capacitance can be over 300 pF. Standard TTL logic gates have insufficient current drive capability to rapidly switch a high capacitive load; a high speed buffer, such as the MC3459, is required.

A considerable amount of noise can be generated during switching due to the high speed and high current drive capability of the MC3459. The high capacitive discharge current during the high to low transition, plus current spikes can result in a considerable amount of noise being generated on the ground lead. Current spikes are due to both the upper and lower output drive transistors being on for a short period of time during switching. This causes a very low impedance path between V_{CC} and ground.

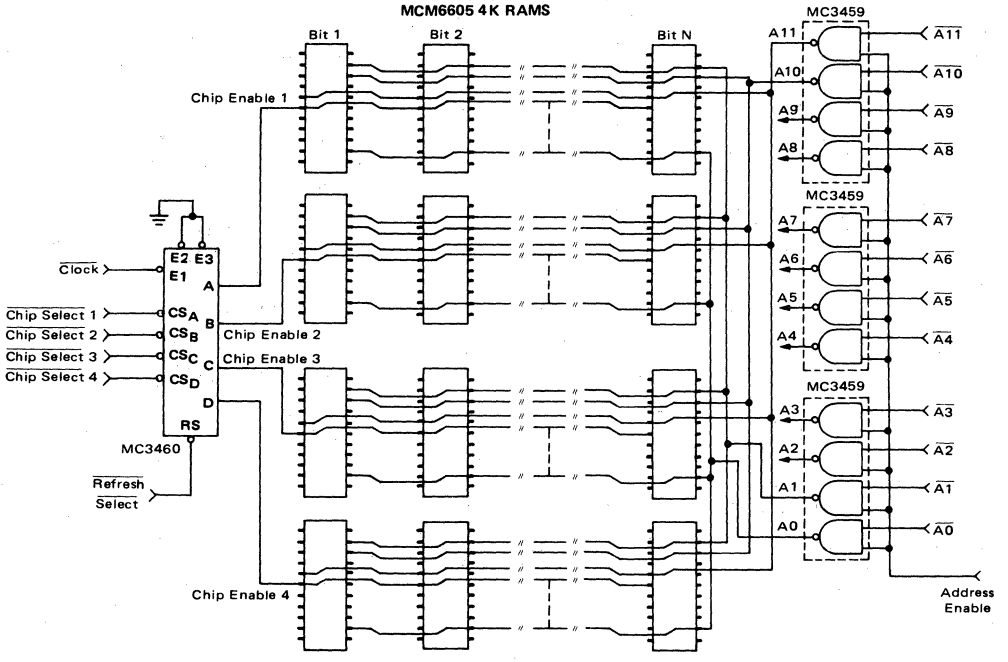
In order to minimize the effects of these currents, the following layout rules should be followed:

1. The V_{CC} supply pin of each package should be bypassed with a low inductance 0.01 μF capacitor. The 0.01 μF capacitor will sustain the high surge currents required during switching.
2. There is a large amount of current out of the ground node during switching – the noise seen at this node will be proportional to the ground impedance. The impedance of the ground bus can be reduced by increasing its width. At least a 50 mil ground width is recommended.

Some of the NMOS memories with TTL logic compatible inputs do not actually meet the TTL logic level requirements in the input high state voltage (V_{IH}). There are N-Channel MOS memories with a V_{IH} minimum ranging from 2.4 V to 4.0 V. The MC3459 can directly interface with those N-Channel memories having a V_{IH} minimum of 3.0 V. The higher driver output levels can be accomplished by adding a pull-up resistor to V_{CC} or by increasing the V_{CC} voltage. There are some N-Channel MOS memories, such as the MCM7001, that have a supply requirement of 7.5 V. The high maximum supply voltage rating of the MC3459 can accommodate a 7.5 V V_{CC} supply without affecting its input TTL logic compatibility. Figure 4 gives the typical V_{OH} versus I_{OH} characteristics for both V_{CC} = 5.0 V and V_{CC} = 7.5 V. An expanded output characteristic curve of Figure 4 is illustrated in Figure 5.

The MC3459 can be used in a variety of applications including, high fan-out buffer (drives 50 standard TTL loads) and low impedance transmission line driver.

FIGURE 6 – TYPICAL APPLICATION
16K X N Memory System Employing
MCM6605 4K RAMS



7

MC3460
MC3466

Specifications and Applications Information

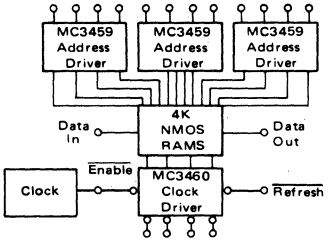
QUAD NMOS MEMORY CLOCK DRIVERS WITH REFRESH SELECT LOGIC

The MC3460 and MC3466 are quad drivers for use with high-level clock lines in NMOS RAM systems. The MC3460 version is specified for 4K memory applications with a V_{DD1} power supply voltages to +13 V. The MC3466 version is specified for mating with the MCM7001A 1K RAM and is guaranteed with a supply voltage V_{DD1} to 18 V. Both versions may be used with the V_{DD2} pin connected to a separate supply > V_{DD1} to increase the high logic state output voltage.

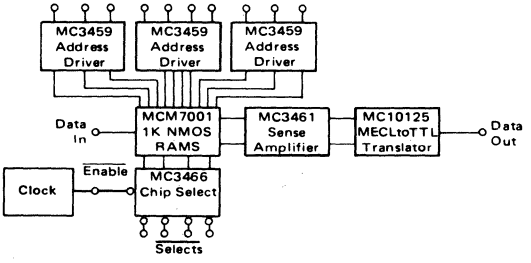
The channel control logic is organized so that all four drivers may be deactivated for STANDBY operation, or single driver may be activated for READ/WRITE operation or all four drivers may be activated for REFRESH operation.

- Control Logic Optimized for Use in MOS RAM Systems
- High Speed Switching
- V_{DD1} and V_{DD2} Variable Over Wide Range of Voltage to 18 and 22 V Respectively (MC3466)
- Output Voltages Compatible with Many Popular MOS RAMs
- MTTL and MDTL Compatible Inputs

TYPICAL APPLICATION WITH 4K NMOS RAM IN TTL SYSTEM (See Figure 17 for Details)

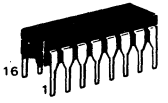


TYPICAL APPLICATION WITH MCM7001 1K RAM AND TTL SYSTEMS (See Figures 22, 23 for Details)



GATE CONTROLLED FOUR CHANNEL MOS CLOCK DRIVERS

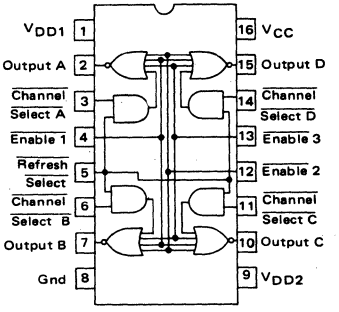
SILICON MONOLITHIC INTEGRATED CIRCUIT



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

PIN CONNECTIONS



TRUTH TABLE

Inputs					Output
Control			Address		
Enable 1	Enable 2	Enable 3	Channel Select	Refresh Select	
H	I	I	I	I	L
I	H	I	I	I	L
I	I	H	I	I	L
I	I	I	H	H	L
L	L	L	L	I	H
L	L	L	I	L	H

H = High Logic State
L = Low Logic State
I = Irrelevant

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MAXIMUM RATINGS (T_A = 25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltages	V_{CC}	+7.0	Vdc
MC3460	V_{DD1}	+14	Vdc
MC3466		+19	
MC3460	V_{DD2}	+18	Vdc
MC3466		+23	
Input Voltage	V_I	+5.5	Vdc
Power Dissipation (Package Limitation)			
Ceramic Package @ T_A = 25°C	P_D	1000	mW
Derate above T_A = 25°C	$1/R_{\theta JA}$	6.6	mW/°C
Plastic Package @ T_A = 25°C	P_D	830	mW
Derate above T_A = 25°C	$1/R_{\theta JA}$	6.6	mW/°C
Ceramic Package @ T_C = 25°C	P_D	3.0	Watts
Derate above T_C = 25°C	$1/R_{\theta JC}$	20	mW/°C
Plastic Package @ T_C = 25°C	P_D	1.8	Watts
Derate above T_C = 25°C	$1/R_{\theta JC}$	14	mW/°C
Operating Ambient Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C
Junction Temperature	T_J		°C
Ceramic Package		175	
Plastic Package		150	

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	MC3460 Min	MC3460 Typ	MC3460 Max	MC3466 Min	MC3466 Typ	MC3466 Max	Unit
Power Supply Voltages	V_{CC}	4.75	5.0	5.25	4.75	5.0	5.25	Vdc
	V_{DD1}	4.75	–	13	4.75	–	18	Vdc
	V_{DD2}	V_{DD1}	–	17	V_{DD1}	–	22	Vdc
(Note 1)	V_{DD2}-V_{DD1}	0	–	10	0	–	10	Vdc
Operating Ambient Temperature Range	T_A	0	–	70	0	–	70	°C

Note 1: Not to Exceed Maximum Recommended Operating Voltages

ELECTRICAL CHARACTERISTICS (Unless otherwise noted, these specifications apply over recommended power supply and temperature ranges. Typical values measured at T_A = 25°C)

Characteristic	Symbol	MC3460 Min	MC3460 Typ	MC3460 Max	MC3466 Min	MC3466 Typ	MC3466 Max	Unit
Output Voltage – High Logic State	V_{OH1}							Vdc
(V_{DD2} = V_{DD1} + 3.0 V, V_{IL} = 0.8 V)								
I_{OH} = -2.0 mA		V_{DD1}-1.0	V_{DD1}-0.8	–	–	–	–	
I_{OH} = -40 mA		–	–	–	V_{DD1}-1.3	V_{DD1}-1.1		
Output Voltage – High Logic State	V_{OH2}							Vdc
(V_{DD2} = V_{DD1}, V_{IL} = 0.8 V)								
(See Applications Section of Data Sheet)								
I_{OH} = -100 μA		V_{DD1}-1.0	V_{DD1}-0.8	–	–	–	–	
I_{OH} = -40 mA		–	–	–	V_{DD1}-2.5	V_{DD1}-1.6	–	
Output Voltage – Low Logic State	V_{OL1}	–	–	0.35	–	–	0.35	Vdc
(V_{IH} = 2.0 V, I_{OL} = +10 mA)								
Output Voltage – Low Logic State	V_{OL2}							Vdc
(V_{IH} = 2.0 V, I_{OL} = 40 mA)								
11 V ≤ V_{DD2} ≤ 17 V		–	–	0.55	–	–	–	
11 V ≤ V_{DD2} ≤ 22 V		–	–	–	–	–	0.55	

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ELECTRICAL CHARACTERISTICS (Unless otherwise noted, these specifications apply over recommended power supply and temperature ranges. Typical values measured at $T_A = 25^oC$)

Characteristic	Symbol	MC3460			MC3466			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Clamp Voltage (V_{IL} = 0 V, I_{OC} = 5.0 mA)	V_{OC}	–	–	V_{DD1}+ 1.0	–	–	V_{DD1}+ 1.0	Vdc
Input Voltage – High Logic State	V_{IH}	2.0	–	–	2.0	–	–	Vdc
Input Voltage – Low Logic State	V_{IL}	–	–	0.8	–	–	0.8	Vdc
Input Clamp Voltage (I_{IC} = -12 mA)	V_{IC}	–	–	-1.5	–	–	-1.5	Vdc
Input Current – High Logic State (V_I = 5.0 V)	I_{IH}							μA
Channel Select Inputs		–	–	20	–	–	20	
Refresh Select and Enable Inputs		–	–	80	–	–	80	
Input Current – Low Logic State (V_{IL} = 0.4 V)	I_{IL}							mA
Channel Select Inputs		–	–	-1.6	–	–	-1.6	
Refresh Select and Enable Inputs		–	–	-6.4	–	–	-6.4	
Power Supply Current – Output – High Logic State	I_{CCH}	–	–	28	–	–	28	mA
(V_{CC} = 5.25 V, V_{IL} = 0V, I_{OH} = 0 mA,	I_{DD1HP}	–	–	0.5	–	–	0.5	
MC3460 V_{DD1} = 13 V, V_{DD2} = 17 V,	I_{DD1HN}	–	–	-6.0	–	–	-6.0	
MC3466 V_{DD1} = 18 V, V_{DD2} = 22 V)	I_{DD2H}	–	–	6.0	–	–	6.0	
Power Supply Current – Output – Low Logic State	I_{CCL}	–	–	48	–	–	48	mA
(V_{CC} = +5.25, V_{IH} = 5.0 V, I_{OL} = 0 mA,	I_{DD1L}	–	–	2.0	–	–	2.0	
MC3460 V_{DD1} = 13 V, V_{DD2} = 17 V,	I_{DD2L}	–	–	23	–	–	30	
MC3466 V_{DD1} = 18 V, V_{DD2} = 22 V)								
Power Supply Current – Output – High Logic State	I_{DD1H}	–	–	0.5	–	–	0.5	mA
(V_{CC} = +5.25 V, V_{IL} = 0 V, I_{OH} = 0 mA,	I_{DD2H}	–	–	0.5	–	–	0.5	
MC3460 V_{DD1} = V_{DD2} = 13 V,								
MC3466 V_{DD1} = V_{DD2} = 18 V)								

SWITCHING CHARACTERISTICS ($T_A = 25^oC$, V_{CC} = 5.0 V; MC3460 : $V_{DD1} = V_{DD2}$ = 12 V, C_L = 480 pF; MC3466 : $V_{DD1} = V_{DD2}$ = 17 V, V_{DD} = 15 V, C_L = 480 pF)

Characteristic	Symbol	MC3460			MC3466			Unit
		Min	Typ	Max	Min	Typ	Max	
Propagation Delay Time – READ/WRITE Mode								ns
Output High to Low Level	t_{DHL1}	–	15	24	–	15	24	
Output Low to High Level	t_{DLH1}	–	15	23	–	15	23	
Transition Time – READ/WRITE Mode								ns
Output High to Low Level	t_{THL1}	–	14	23	–	15	24	
Output Low to High Level	t_{TLH1}	–	14	23	–	15	24	
Propagation Delay Time – REFRESH Mode								ns
Output High to Low Level	t_{DHL2}	–	20	35	–	–	–	
Output Low to High Level	t_{DLH2}	–	16	27	–	–	–	
Transition Time – REFRESH Mode								ns
Output High to Low Level	t_{THL2}	–	20	36	–	–	–	
Output Low to High Level	t_{TLH2}	–	16	27	–	–	–	

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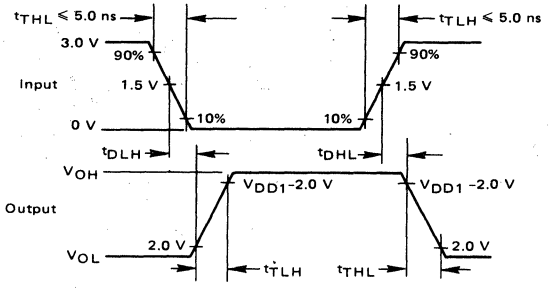
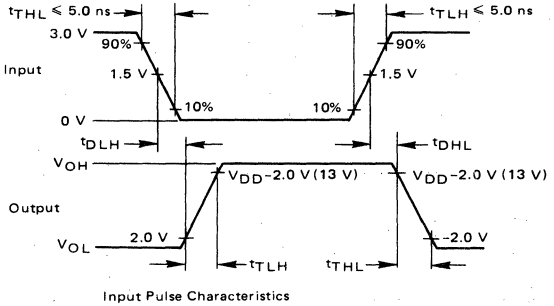
FIGURE 1 – SWITCHING TEST WAVEFORMS – MC3460



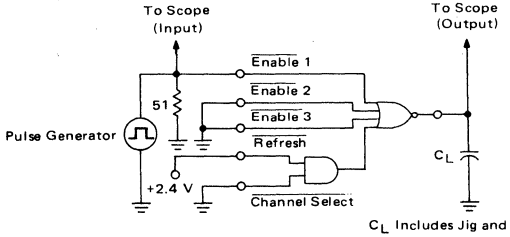
Input Pulse Characteristics
PRR = 1 MHz READ/WRITE Mode
PRR = 100 kHz REFRESH Mode
PW = 500 ns
$t_{TLH} = t_{THL} \leq 5.0$ ns

FIGURE 2 – SWITCHING TEST WAVEFORMS – MC3466



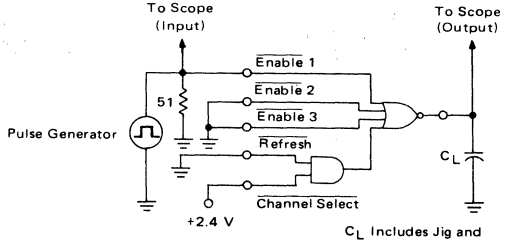
Input Pulse Characteristics
PRR = 1 MHz, READ/WRITE Mode
PW = 500 ns
$t_{TLH} = t_{THL} \leq 5.0$ ns

FIGURE 3 – SWITCHING TEST CIRCUIT FOR READ/WRITE MODE – MC3460



CL Includes Jig and Probe Capacitance

FIGURE 4 – SWITCHING TEST CIRCUIT FOR REFRESH MODE – MC3460



CL Includes Jig and Probe Capacitance

FIGURE 5 – SWITCHING TEST CIRCUIT FOR READ/WRITE MODE – MC3466

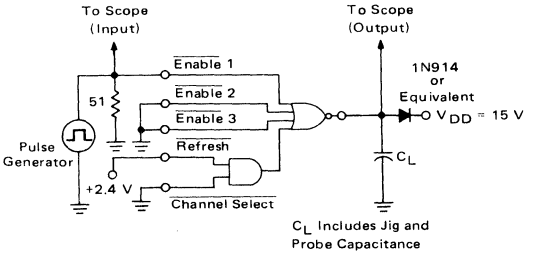
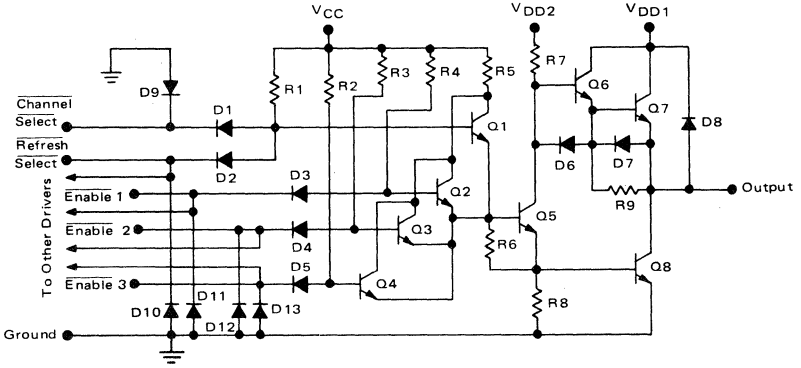


FIGURE 6 – REPRESENTATIVE CIRCUIT SCHEMATIC (1/4 of Circuit Shown)



TYPICAL PERFORMANCE CURVES

FIGURE 7 – DELAY TIMES versus LOAD CAPACITANCE (READ/WRITE MODE)

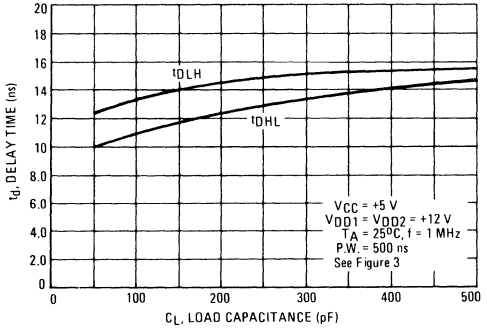
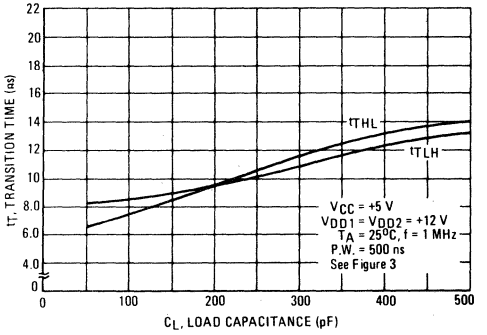


FIGURE 8 – TRANSITION TIMES versus LOAD CAPACITANCE (READ/WRITE MODE)



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TYPICAL PERFORMANCE CURVES

FIGURE 9 – DELAY TIMES versus LOAD CAPACITANCE (REFRESH MODE)

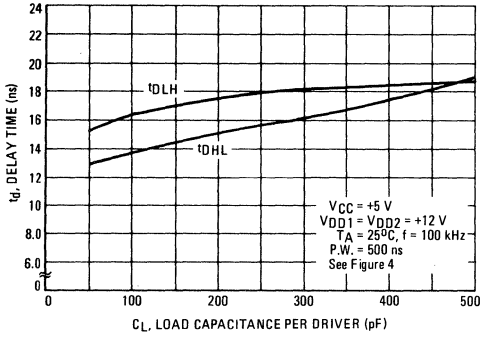


FIGURE 10 – TRANSITION TIMES versus LOAD CAPACITANCE (REFRESH MODE)

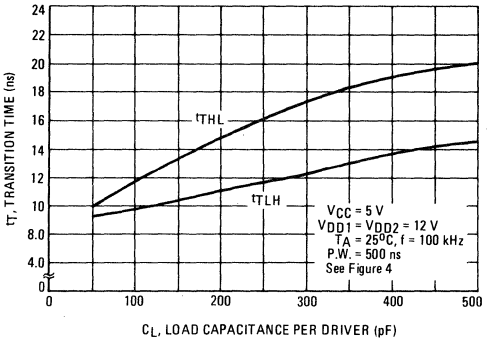


FIGURE 11 – SWITCHING TIMES versus TEMPERATURE (READ/WRITE MODE)

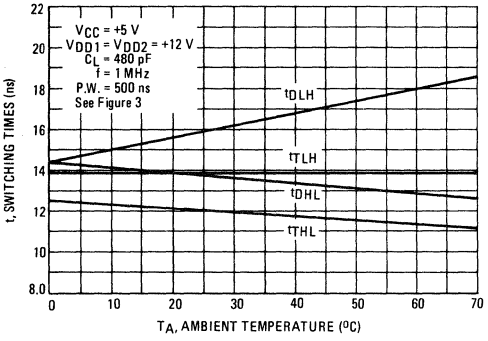


FIGURE 12 – SWITCHING TIMES versus TEMPERATURE (REFRESH MODE)

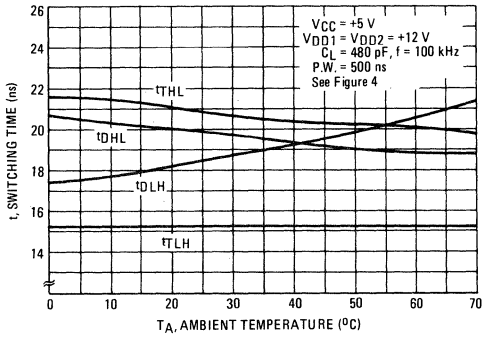


FIGURE 13 – POWER DISSIPATION versus FREQUENCY

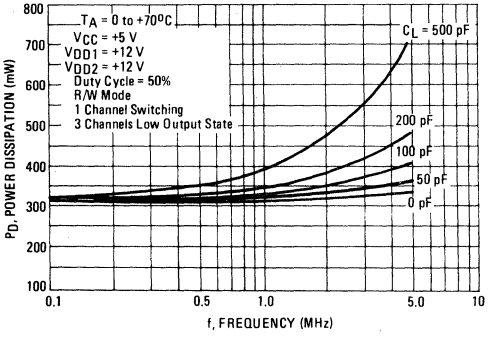
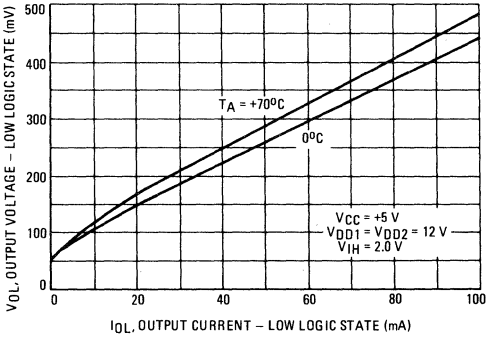


FIGURE 14 – OUTPUT VOLTAGE – LOW LOGIC STATE versus OUTPUT CURRENT



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TYPICAL PERFORMANCE CURVES

FIGURE 15 – OUTPUT VOLTAGE – HIGH LOGIC OUTPUT STATE versus OUTPUT CURRENT

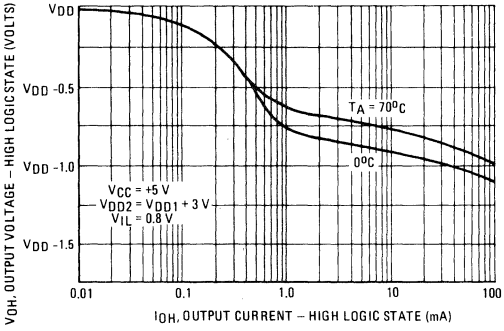


FIGURE 16 – OUTPUT VOLTAGE – HIGH LOGIC STATE versus OUTPUT CURRENT

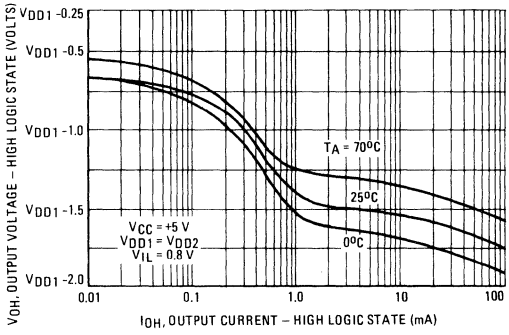
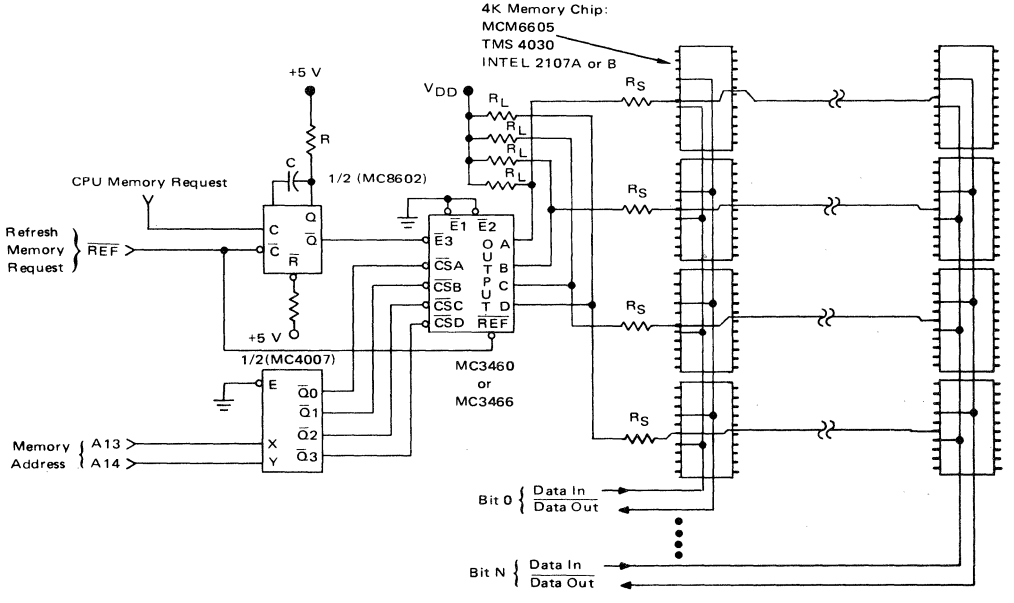


FIGURE 17 – TYPICAL 16K WORD BY N BIT MEMORY ARRAY



APPLICATIONS INFORMATION

The MC3460 and MC3466 are designed specifically for dynamic N-Channel MOS random access memories (RAM's) that require a single high-voltage clock. The unique design and electrical characteristics of these clock drivers will enhance the performance, as well as reduce the cost, of dynamic MOS RAM systems.

Dynamic N-Channel MOS RAM's that require a high voltage clock have extremely low standby power when the clock is in the logic "0" state (Gnd). To take advantage of this low-power mode, the memory system should be partitioned such that only the memory chips of a selected word receive a clock signal (see memory system in Figure 17). However, to reduce the amount of time spent refreshing the memory system, all memory chips of the system should be clocked for each refresh cycle.

The logic necessary to accomplish this desirable system feature has been incorporated in the clock drivers. Note from the block diagram and the truth table (on the front page of this data sheet) that the selection of a clock driver is dependent on the logic state of the $\overline{\text{REFRESH}}$ and $\overline{\text{CHANNEL SELECT}}$ inputs. All four drivers are selected when the $\overline{\text{REFRESH SELECT}}$ input (Pin 5) is at a logic "0" state. However, when the $\overline{\text{REFRESH SELECT}}$ input is at a logic "1" state, only those drivers that have their respective $\overline{\text{CHANNEL SELECT}}$ inputs at a logic "0" state will be selected. The timing and clock driver output pulse width are controlled by a logic "0" signal applied to one of the three $\overline{\text{ENABLE}}$ inputs. The other two $\overline{\text{ENABLE}}$ inputs allow the memory system to be expanded without additional address decoding.

Figure 17 illustrates one possible clock driver configuration that can be employed to drive a 16K word memory system comprised of 4K dynamic MOS RAM's. The MC4007 is a one-of-four decoder that decodes the memory address sent from the CPU. Since the decoder outputs drive the clock driver $\overline{\text{SELECT}}$ inputs, only one of the four clock drivers will be selected. The timing and clock driver output pulse width can be accomplished with a simple one-shot (MC8602). The $\overline{Q}$ output of the MC8602 drives an $\overline{\text{ENABLE}}$ input of the MC3460/MC3466 and the clock pulse width is determined by the RC component values.

For a memory refresh cycle, the $\overline{\text{REFRESH SELECT}}$ input of the MC3460/MC3466 is switched to a logic "0" state which will select all of the clock drivers as noted earlier. On the falling edge of the $\overline{\text{REFRESH SELECT}}$ signal, the one-shot is fired and at the same time all four clock drivers are selected for the refresh cycle since the $\overline{\text{REFRESH SELECT}}$ signal is in the zero state (See Figure 17). At the end of the refresh cycle, the $\overline{\text{REFRESH SELECT}}$ signal is switched to the logic "1" state and the memory system is set to accommodate another CPU memory request. The memory system access time will be enhanced with this scheme because no additional gating is required to accommodate the refresh cycle.

SYSTEM CONSIDERATIONS

Bypass and Layout – A considerable amount of noise can be generated during switching due to the high speed and high current drive capability of these drivers. The high charge or discharge current spikes during transitions can result in a considerable amount of noise being generated on the ground and V_{DD1} leads. These current spikes are primarily due to capacitive load current. However, there is an additional component to the total current spike which is due to both the upper and lower output driver transistors conducting for a short period of time during switching. This causes a low impedance path between the V_{DD1} supply and ground during part of the transition time.

In order to minimize the effects of these surge currents, the following layout rules should be followed:

1. The V_{DD1} supply pin of each package should be bypassed with a low inductance 0.1 μF capacitor. The 0.1 μF capacitor will sustain the high surge currents required during switching.
2. The surge current that flows out of the driver ground pin during switching will generate noise. This noise will be proportional to the ground impedance at the ground pin. To insure minimum ground noise, the ground path to this pin should be as wide as possible. At least a 50 mil to 100 mil ground line is recommended.

Fanout Considerations – In a memory system, the number of memory CHIP ENABLE inputs that can be driven by a single clock driver will depend on the input capacitance and the input leakage current required at a specified minimum logic "1" state (V_{CEH}). Since the memory CHIP ENABLE input capacitance will affect the clock transition times, the total parallel input capacitance should not exceed that value which will cause the clock driver transition times to be slower than those specified for the memory. For a majority of the 4K RAM's, the chip enable input capacitance is less than 40 pF. With a 30 pF loading, each driver of this device can drive up to sixteen 4K memory chips.

Although the input leakage current of each memory CHIP ENABLE is extremely small, the total leakage current of the CHIP ENABLE inputs when paralleled in a memory system can exceed the output current ot the clock driver in the high output state (V_{OH}). With the MC3460/MC3466 there are two methods that can be employed to increase the output current. The MC3460/MC3466 has split high voltage power supplies (V_{DD1} and V_{DD2}) as noted in Figure 18. With $V_{DD1} = V_{DD2}$, the maximum output current, that guarantees a minimum V_{OH} of V_{DD1} -1.0 Volt, is -100 μA. However, the output current can be greatly increased if a voltage greater than V_{DD1} is applied to V_{DD2}. For $V_{DD2} = V_{DD1}$

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+3.0 Volts, I_{OH} can be increased to -2.0 mA for a V_{OH} minimum of V_{DD1} -1.0 Volt. For most 4K RAM's, this current is sufficient to drive to 200 memory chips. However, if a higher voltage is not available for V_{DD2} then the current can be increased by employing a pull-up resistor to V_{DD1}. The following formula can be used to determine what value of pull-up resistor is needed to meet a given fanout requirement.

$$R \leqslant \frac{V_{DD1} - V_{OH(min)}}{I_R} \quad (1)$$

where

$$I_R = N(I_{ICE}) - I_{OH} \quad (2)$$

I_{OH} is the clock driver output current for $V_{OH(min)} \geqslant V_{CEH(min)}$

I_{ICE} is the memory CHIP ENABLE input leakage current specification.

N is the number of CHIP ENABLE inputs to be driven by the clock driver.

For the memory system given in Figure 17, assume that each word has 16 bits. If the MCM6605 4K RAM were employed, then the pull-up resistor value would be calculated in the following manner.

From the MCM6605 Specifications;

$V_{CEH(min)} = V_{DD} - 1.0$ Volt @ $I_{ICE} = 10\ \mu A$.

From the MC3460 Specifications;

For $V_{DD1} = V_{DD2}$ the minimum V_{OH} is V_{DD1} - 1.0 Volt @ an $I_{OH} = 100\ \mu A$

Since the V_{OH} (min) required by the MCM6605 is V_{DD1} -1.0 Volt, equation (1) reduces to:

$$R \leqslant \frac{V_{DD1} - (V_{DD1} - 1.0\ Volt)}{I_R}$$

or

$$R \leqslant \frac{1.0\ Volt}{I_R} \quad (3)$$

From equation (2), since N = 16, I_R = 16 (10 μA) -100 μA = 60 μA. Substituting in this value of I_R into Equation (3) yields the following value for R:

$$R \leqslant \frac{1.0\ Volt}{60\ \mu A} = 16.6\ k$$

Overshoot — The finite inductance of the memory chip ENABLE line can cause the clock driver to overshoot during switching. With fast switching clock drivers, the overshoot can exceed the maximum logic levels specified for the CHIP ENABLE input. To insure that the overshoot voltage does not exceed the maximum CHIP ENABLE input ratings the following two techniques can be employed:

The simplest scheme is to place a damping resistor R_S in series with the clock line, (See Figure 17). The critical value of R_S can be calculated from the formula:

$$R_S \cong 2\sqrt{\frac{L_S}{C_L}} \quad (4)$$

where L_S is the clock line inductance and C_L is the load capacitance.

For most memory systems the value of R_S will range from 10 ohms to 50 ohms.

The series damping resistor will also affect the transition times of the damped output waveform. Thus, the maximum value that may be used for R_S will be determined by the maximum switching times specified for the CHIP ENABLE input. The following equation can be used to determine the maximum value of R_S.

$$t_T\ (max) \leqslant 2.2\ R_S\ C_L \quad (5)$$

In some high performance memory systems the switching times required may be too fast to accomodate the addition of a damping resistor. For these systems the overshoot can be limited by placing clamp diodes at the far end of the CHIP ENABLE line as noted in Figure 19. Fast recovery diodes are required to insure proper clamping on both the leading and trailing edges of the CLOCK pulse.

Power Considerations — Circuit performance and long-term circuit reliability are affected by die temperature. Normally, both are improved by keeping the integrated circuit junction temperatures low. Electrical power dissipated in the integrated circuit is the source of heat. This heat source increases the temperature of the die relative to some reference point, normally the ambient temperature. The temperature increase depends on the amount of power dissipated in the circuit and on the thermal resistance between the heat source and the reference point. The basic formula for converting power dissipation into junction temperature is:

$$T_J = T_A + P_D\ (R_{\theta JC} + R_{\theta CA}) \quad (6)$$

or

$$T_J = T_A + P_D\ (R_{\theta JA}) \quad (7)$$

where

T_J = junction temperature
T_A = ambient temperature
P_D = power dissipation
$R_{\theta JC}$ = thermal resistance, junction to case
$R_{\theta CA}$ = thermal resistance, case to ambient
$R_{\theta JA}$ = thermal resistance, junction to ambient

The power dissipation of the device (P_D) is dependent on the following system requirements: frequency of operation, capacitive loading, output voltage swing, and duty cycle. The power dissipation as a function of capacitive loading and frequency can be obtained from Figure 13. The value found in Figure 13 should not yield a junction temperature, T_J, greater than T_J (max) at the maximum encountered ambient temperature. T_J (max) is specified for the integrated circuit packages in the maximum ratings section of this data sheet.

FIGURE 18 – SIMPLIFIED OUTPUT CONFIGURATION

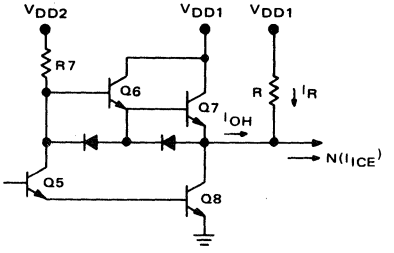
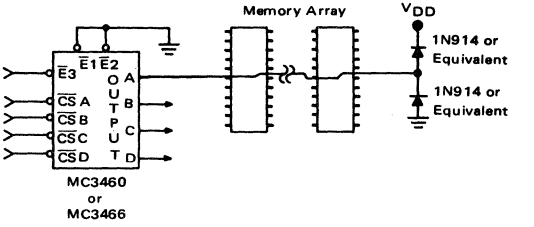


FIGURE 19 – APPLICATION OF CLAMPING DIODES TO LIMIT OVERSHOOT



THE MC3466 IN HIGH PERFORMANCE '7001 SYSTEMS

The MC3466 is specified to meet the more stringent driving requirements of high speed N-channel memories such as the MCM7001A. Figures 20 and 21 show photographs of oscilloscope waveforms for the MC3466 driving up to six MCM7001A memories. The memories were operated with a +15 Volt supply and the MC3466 used a +17 Volt supply tied to V_{DD1} and V_{DD2}. Two clamp diodes were used at the end of the line to clamp the overshoot as noted previously in Figure 19.

With this driver connection, where the V_{DD1} supply is at a higher voltage than the memory V_{DD} supply, the V_{DD1} and V_{DD} supplies should track each other within the following range $3.0\ V \geqslant V_{DD1} - V_{DD} \geqslant 1.5\ V$ to insure the minimum output V_{OH} level and to limit the amount of current the clamp diode has to sink during the clock high state period.

For the MC3466 driving two MCM7001A memories, Figure 20 shows the driver supplying about 250 mA peak current when the CHIP SELECT voltage switches from a "low" to "high", with a transition time of 15 ns (1.5 V to 13.5 V level) and a high to low transition time of only 8 ns. When driving four MCM7001A memories, the peak current reaches about 400 mA with a CHIP SELECT rise time of 22 ns.

Figure 21 shows that for a fanout of 6 memories, the transition time increases to 28 ns. The MC3461 (dual NMOS memory sense amplifier) is used to detect the data of the output memory and translate to MECL 10,000 levels. The use of the MC10125 will translate the MECL levels to TTL levels in only 5 ns. The total delay from the 50% level of the falling clock edge at the MC3466 input to the 50% point at the data output of the MC10125 is only 62 ns when driving two memories and 67 ns for four memories.

Figure 22 shows the logic diagram for building a 32K x 1 memory board with TTL interface and MCM7001A memories using a multiplex approach. Addresses A0 to A9 and the D_{IN} signals go to all the memory devices. The address bits A10 and A11 are used to select 1 of 4 rows (WRITE ENABLE lines) when writing into the memory. The addresses, A12, A13, and A14 are decoded using the MC3466 to drive the CHIP SELECT lines. Only two MC3466's are required. Each driver in the MC3466 drives the CHIP SELECT line connected to four memories. During a read operation, the data from 4 of the 32 memories are latched into the MC3461. Addresses A10 and A11 are used to select which one of the four memories is to be read on the DATA OUT line. This configuration is especially useful in interweaving of fast, large memory systems so that the data can be read out consecutively in one CPU cycle time.

A 4K x 18 memory board is shown in Figure 23 with TTL interface using a more straightforward approach. Only six MC3466's are required to drive the CHIP SELECT lines. The memory can be expanded to 256K words by using two 1-of-8 decoders on the control board and connecting the outputs to the proper BOARD ENABLE.

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FIGURE 20 – CURRENT AND VOLTAGE CHARACTERISTICS FOR THE MC3460 DRIVER DRIVING 2 AND 4 MCM7001A MEMORIES

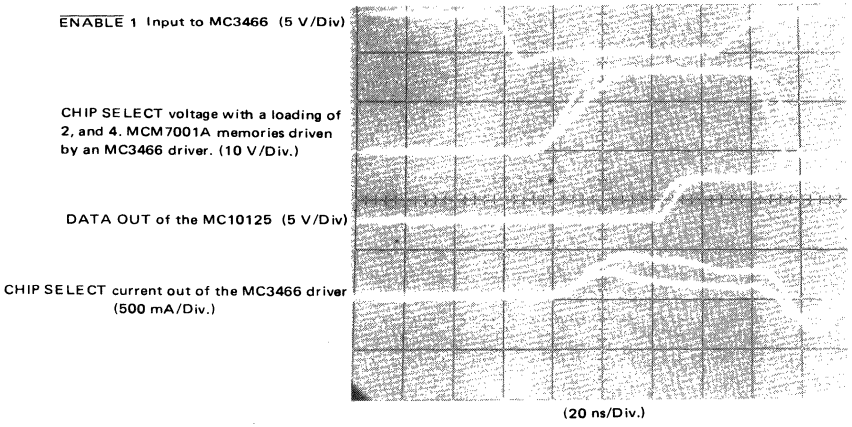


FIGURE 21 – RISE TIME AND ACCESS TIME VARIATIONS FOR AN MC3466 DRIVER DRIVING 1,2,4, AND 6 MCM7001A MEMORIES

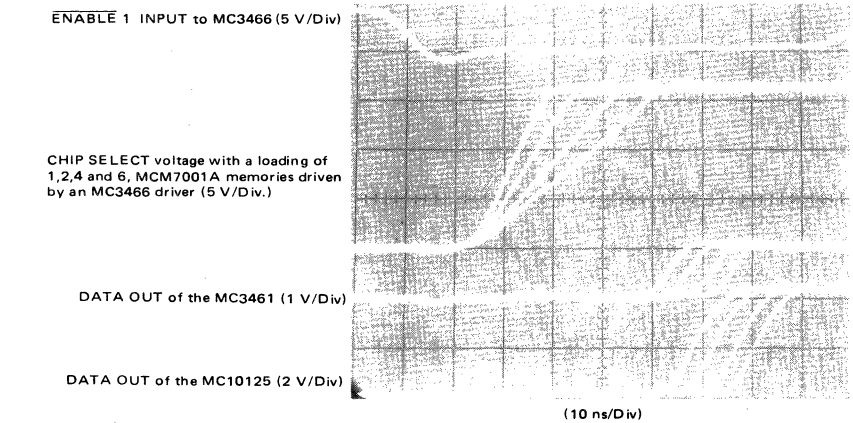
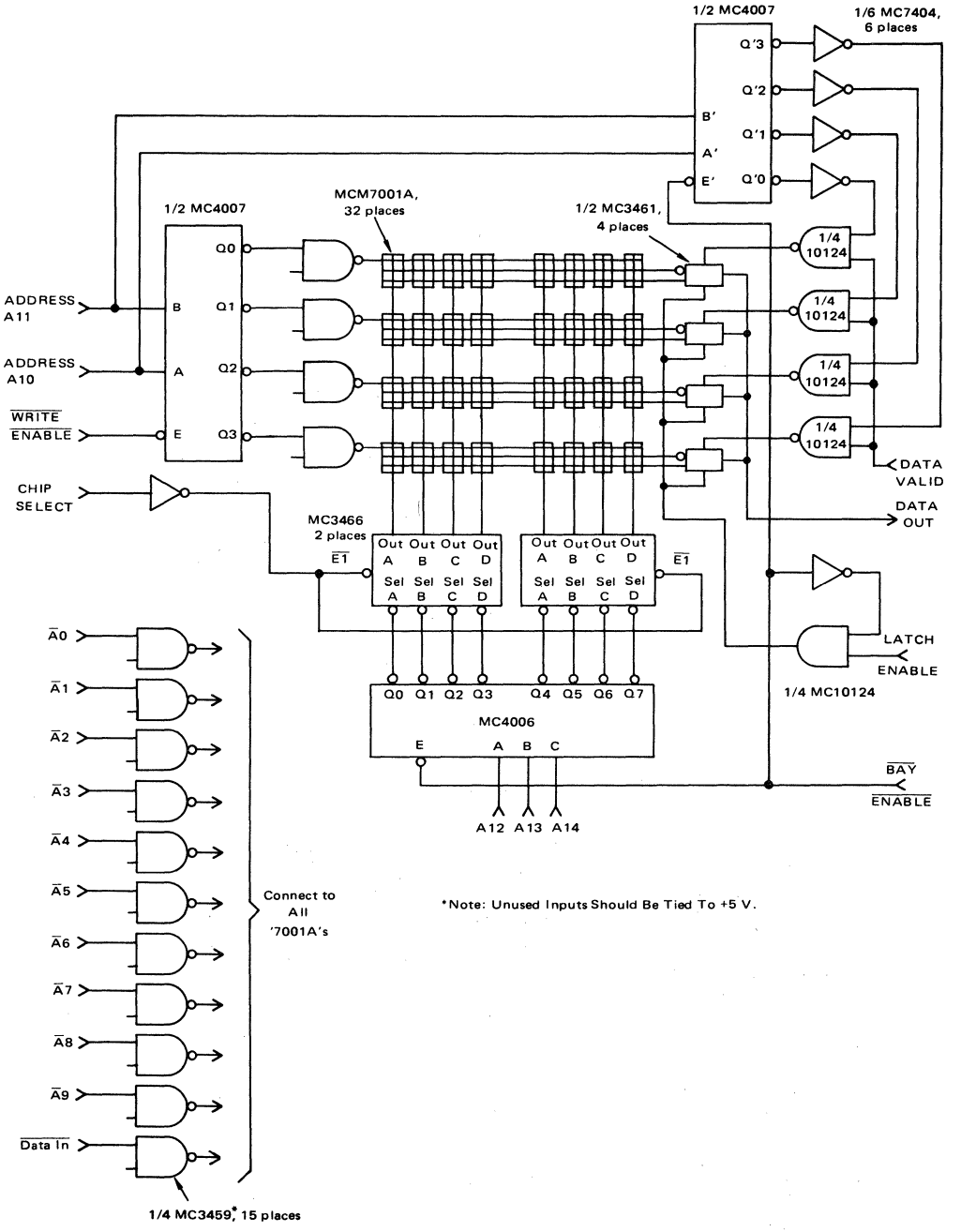


FIGURE 22 – 32K x 1 MEMORY BOARD
(TTL INTERFACE)



*Note: Unused Inputs Should Be Tied To +5 V.

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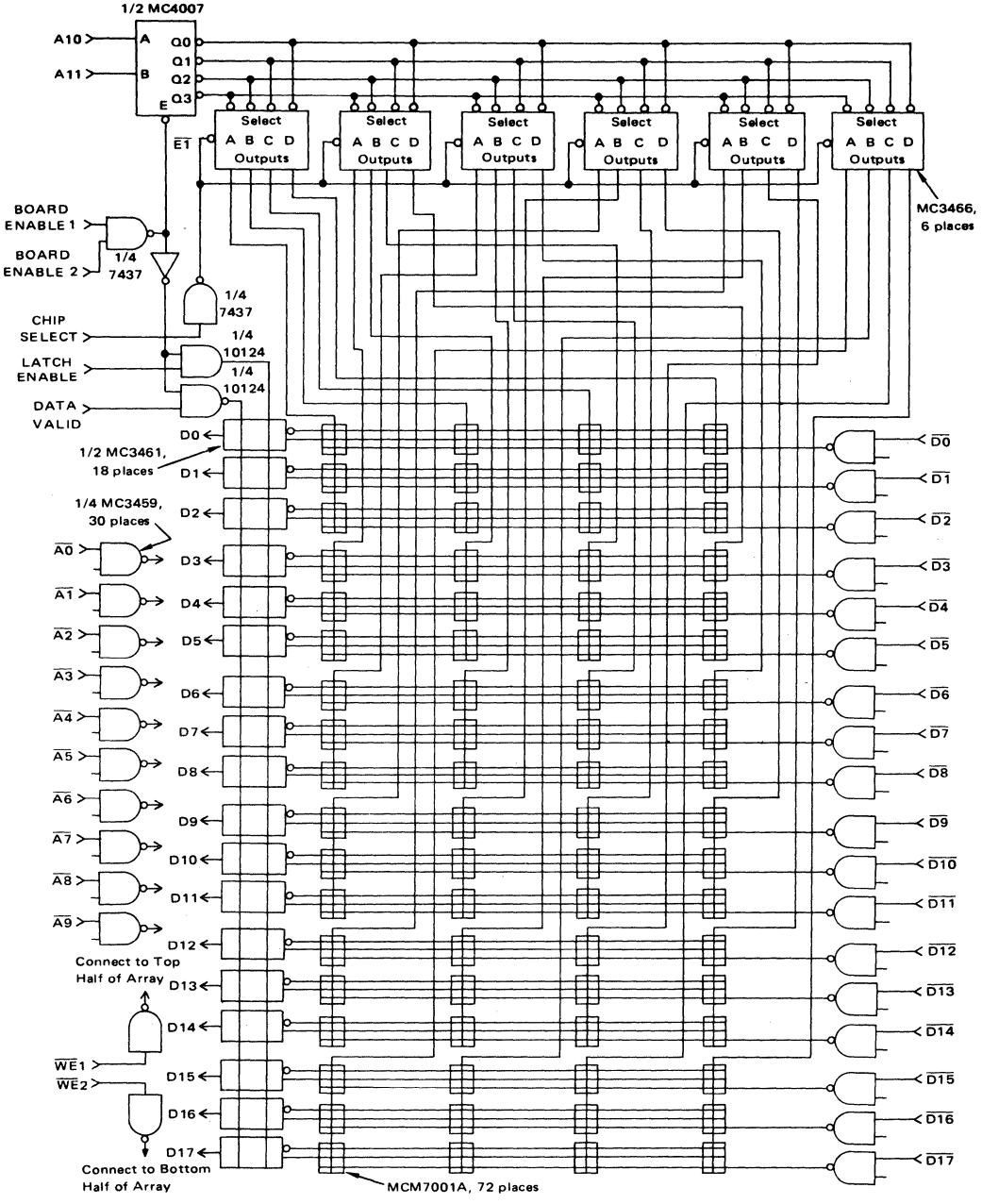
FIGURE 23 – 4K x 18 MEMORY BOARD (TTL INTERFACE)



MC8505P

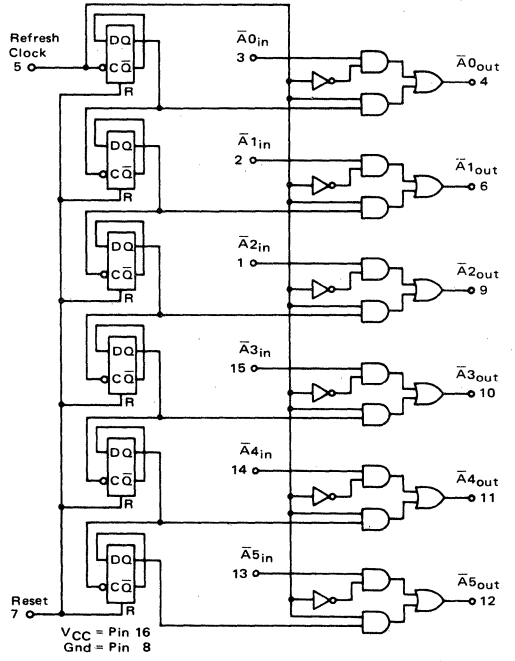
MOS DYNAMIC MEMORY ADDRESS REFRESH LOGIC CIRCUITRY

The MC8505 is a high speed address refresh logic circuit designed for application with MOS dynamic memories. Fabricated using bi-polar integrated circuit technology, this device contains an internal 6-bit counter, counter reset control, and necessary multiplexing circuitry to either propagate memory addresses from the CPU (normal operating mode), or to sequentially cycle through the low order input address lines of dynamic MOS memories (refresh mode).

The MC8505 can be used for 16, 32, or 64 cycle refresh for either 1K or 4K MOS dynamic memories by proper choice of refresh clock frequency and utilization of 4, 5, or 6 output memory address lines. High input impedance and a low propagation delay allow the MC8505 to be tied directly to the CPU address bus with minimal loading and negligible increase in total memory cycle.

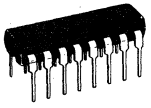
- 16, 32, or 64 Cycle Refresh
- Refresh for 1K or 4K Memories
- Bus Compatible
- Address Delay Time = 60 ns typical
- 5-V Power Supply
- Counter Reset Control

LOGIC DIAGRAM



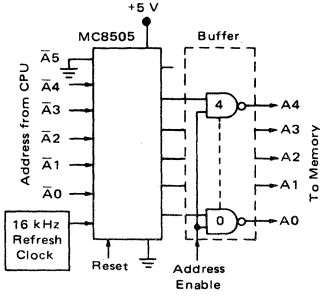
BIPOLAR LSI

MOS DYNAMIC MEMORY ADDRESS REFRESH LOGIC CIRCUIT

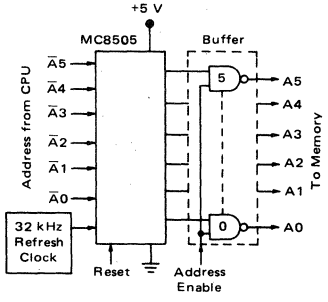


PLASTIC PACKAGE
CASE 648

32-CYCLE REFRESH



64-CYCLE REFRESH



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ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Voltage on Any Pin Relative to Gnd	V_{in},V_{out}	7.0	Vdc
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-55 to +165	°C

DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted.)

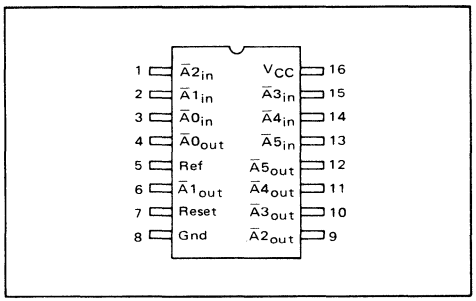
DC OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	4.75	5.25	Vdc
Logic Levels (All Inputs)				Vdc
Input High Threshold Voltage	V_{IHT}	1.4	–	
Input Low Threshold Voltage	V_{ILT}	–	1.0	

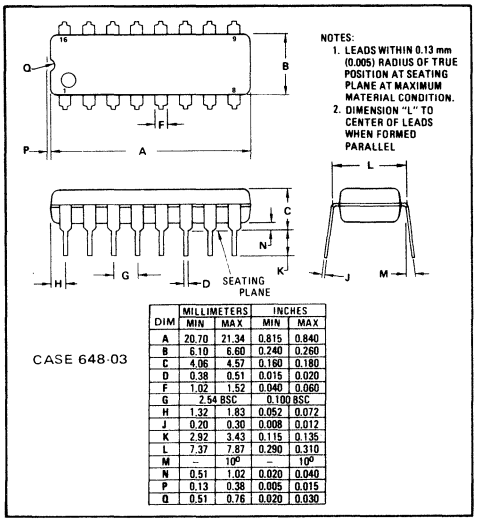
DC ELECTRICAL CHARACTERISTICS

Characteristic		Symbol	Min	Max	Unit
Input High Current					mAdc
(V_{in} = 2.4 Vdc)	Address Inputs	I_{AH}	–	0.24	
	Refresh Clock	I_{CH}	–	1.7	
	Reset	I_{RH}	–	1.5	
Input Low Current					mAdc
(V_{in} = 0)	Address Inputs	I_{AL}	–	-0.2	
	Refresh Clock	I_{CL}	–	-1.4	
	Reset	I_{RL}	–	-1.2	
Output High Voltage (I_O = -300 μAdc)		V_{OH}	2.4	–	Vdc
Output Low Voltage (I_O = 3.2 mAdc)		V_{OL}	–	0.5	Vdc
Power Dissipation (T_A = 25°C)		P_D	–	280	mW
Input Capacitance		C_{in}	–	5.0	pF

PIN ASSIGNMENT



PACKAGE DIMENSIONS



CASE 648-03

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	20.70	21.34	0.815	0.840
B	6.10	6.60	0.240	0.260
C	4.06	4.57	0.160	0.180
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.32	1.83	0.052	0.072
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.37	7.87	0.290	0.310
M	–	10°	–	10°
N	0.51	1.02	0.020	0.040
P	0.13	0.38	0.005	0.015
Q	0.51	0.76	0.020	0.030

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AC OPERATING CONDITIONS AND CHARACTERISTICS

(Load = 1 TTL Gate, C_L = 10 pF, T_A = 25°C)

AC OPERATING CONDITIONS

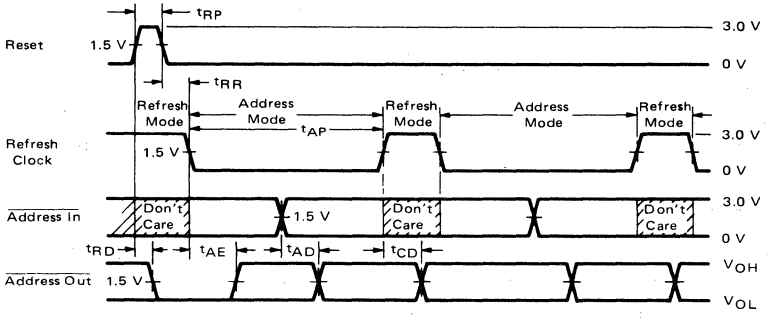
Parameter	Symbol	Min	Unit
Address Mode Pulse Width*	t_{AP}	200	ns
Reset Pulse Width	t_{RP}	100	ns

*Minimum time for burst refresh.

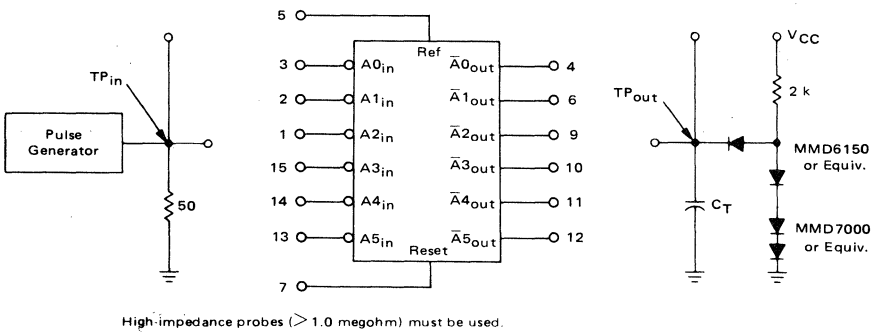
AC ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Typ	Max	Unit
Input-Output Address Delay	t_{AD}	60	80	ns
Address Enable Delay	t_{AE}	70	100	ns
Refresh Address Delay	t_{CD}	120	145	ns
Reset Delay	t_{RD}	100	120	ns
Reset Release Delay	t_{RR}	35	55	ns

TIMING DIAGRAM



SWITCHING TIME TEST CIRCUIT



High-impedance probes (> 1.0 megohm) must be used.
C_T = 10 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

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APPLICATIONS INFORMATION

All dynamic MOS random access memories require a periodic refresh operation to insure that stored data is retained. A refresh operation consists of a specified number of write cycles (some memories require a read cycle) on the least significant address bits of the memory within a given period of time. The number of write or read cycles will vary depending on the memory circuit. Presently available dynamic MOS RAMs require either 16, 32, or 64 write or read cycles within a 2 ms period.

Unfortunately the periodic refresh requirement of dynamic MOS RAMs increases the cost and reduces the overall performance of a memory system. For example, additional logic is required to insure that the memory system is properly refreshed, as indicated in the memory system diagram of Figure 1. The MC8505 was designed to simplify and minimize the logic necessary to perform the refresh operation.

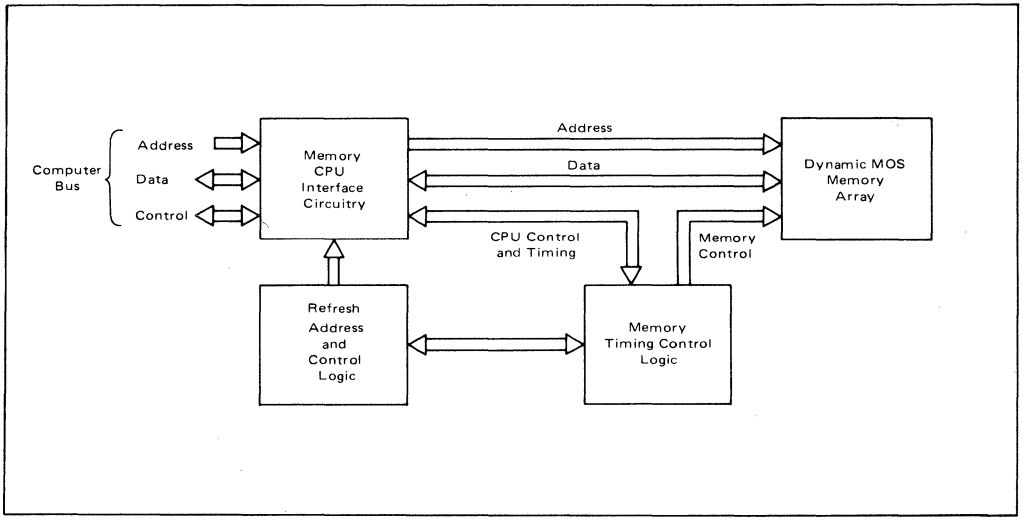
The MC8505 contains a 6-bit binary ripple counter that is used to generate the 64 sequential address states required for the 64-cycle refresh memories. Only four or five bits of the counter are required for those memories having 16 or 32-cycle refresh.

A multiplexer is also included with the counter so that both the counter and the CPU address can be gated to the least significant address bits of the MOS RAM. The refresh clock (see logic diagram) determines which address the multiplexer gates to memory address. When the refresh clock is at a logic "0" (V_{IL}), the bus address inputs are gated to the memory address. The address of the counter is gated to the memory address during a refresh cycle when the refresh clock input is switched to a logic "1" (V_{IH}). After a refresh cycle is complete, the negative-going edge of the refresh clock increments the counter for the next refresh operation.

The high input impedance feature of the MC8505 eliminates the need for high impedance buffers on the CPU address lines, thus reducing CPU interface circuitry. The high input impedance buffers are required to prevent loading of the CPU address bus.

The low power (280 mW max) of the MC8505 is another important feature, especially for memory systems requiring battery backup for non-volatility. The reset input can also be used to save power in a standby mode. One technique to conserve power is to remove all power from the memory board except to the MOS RAMs. The board is then powered up every 2 ms and the proper number of refresh cycles are performed with a high speed clock. By resetting the counter on power up, the most significant bit of the

FIGURE 1 – TYPICAL DYNAMIC MOS MEMORY SYSTEM BLOCK DIAGRAM



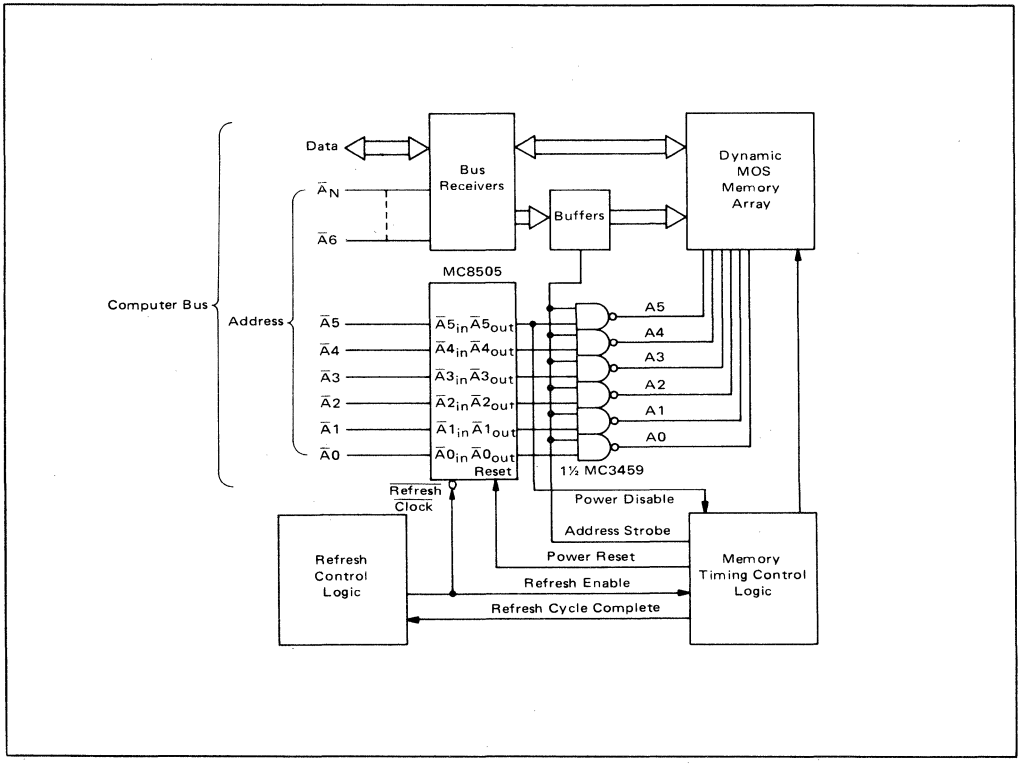
counter can be used to signify refresh is complete so power can be removed until the next refresh period.

Figure 2 illustrates how the MC8505 is employed in the memory system. The least significant address bits of the CPU are connected directly to inputs $\overline{A0}_{in}$ through $\overline{A5}_{in}$ of the MC8505. The refresh control logic generates the proper number of refresh enable signals within each 2 ms period. This refresh enable signal initiates a refresh cycle by switching the counter of the MC8505 to the lower address bits of the memory. At the completion of a refresh cycle, the refresh signal is disabled. On the trailing edge of this signal, the 6-bit counter is incremented and the bus address is once again enabled. High speed address buffers are required (MC3459's) to switch the high capacitive load that is due to paralleling the memory addresses.

Note from the specifications on the refresh clock that the I_{CH} current is 1.7 mA at V_{in} = 2.4 V. To accomodate this high input refresh clock current with standard TTL logic requires a pullup resistor less than 1.8 k ohms to V_{CC}. If high speed TTL is employed, then no pullup resistor is required.

The MC8505 is supplied in a 16-pin package, and replaces at least four MSI and SSI parts. This universal function can be used with all dynamic MOS memories and its simplicity and low cost will further enhance the cost-performance of dynamic MOS memory systems.

FIGURE 2 – MEMORY SYSTEM EMPLOYING THE MC8505



TRIPLE MECL TO
NMOS TRANSLATOR

MC10177

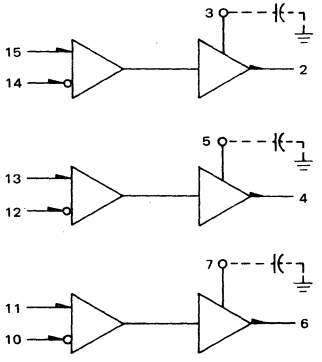
Advance Information

- Max Load: 350 pF
- P_D = 1.0 W typ/pkg @ 5.0 MHz
- Operating Rate: 5.0 MHz typ.
  (all 3 translators in use simultaneously)
- INPUT: MECL 10,000 (differential)
- OUTPUT: NMOS + 0.5 V V_{OLmax}
  + 3.0 V V_{OHmin}*

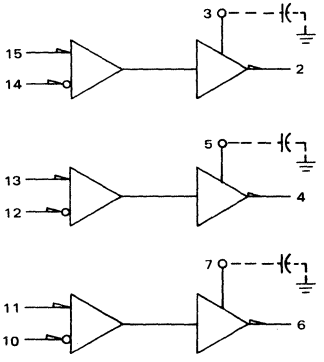
*May be raised by increasing V_{SS}.

The MC10177 consists of three MECL to MOS translators which convert MECL 10,000 logic levels to NMOS levels. It is designed for use in N-channel memory systems as a Read/Write, Data/Address driver. It may also be used as a high fanout (30) MECL to TTL translator, or in other applications requiring the capability to drive high capacitive loads. A separate lead from each of the three translators is brought out of the package. These leads may be connected to V_{SS} or to an external capacitor (0.01 to 0.05 μF to ground), for waveform improvement, and short circuit protection. When connection is made to an external capacitor, V_{SS} line fluctuations due to transient currents are also reduced.

POSITIVE LOGIC



NEGATIVE LOGIC



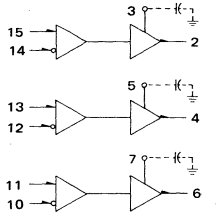
V_{CC} = Gnd = Pins 1,16
V_{EE} = Pin 8 = -5.2 Vdc ±5%
V_{SS} = Pin 9 (+5.0 Vdc or +6.0 Vdc ± 10%)

This is advance information and specifications are subject to change without notice.

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained.

In general test procedures are shown for only one input and one output. The other inputs and outputs are tested in a similar manner.



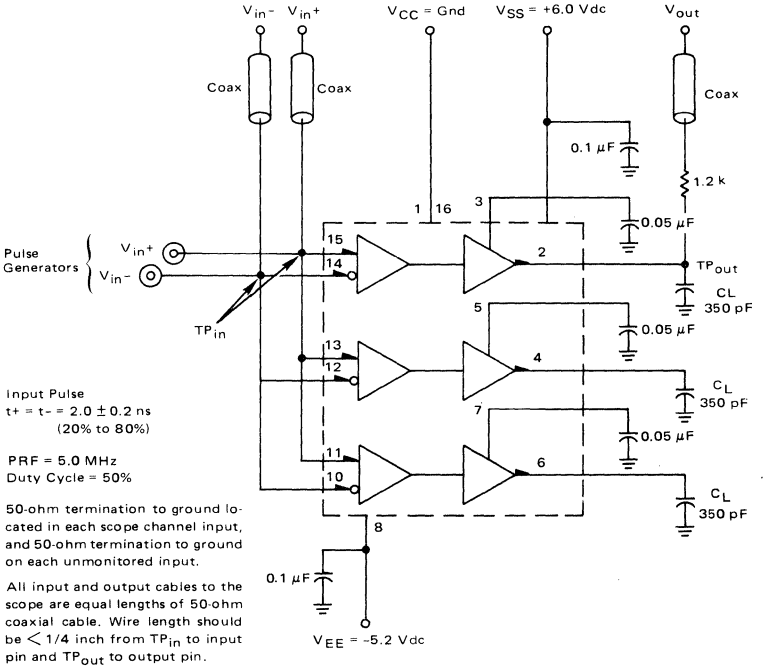
L SUFFIX
CERAMIC PACKAGE
CASE 620

@ Test Temperature	TEST VOLTAGE/CURRENT VALUES: Volts V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	V_{SC}	V_{SS}	mAdc ±1% I_{OL1}	I_{OL2}	I_{OH}	µF ±5% C#
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2	+5.0	+6.0	+1.0	+20	-15	0.05
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2	+5.0	+6.0	+1.0	+20	-15	0.05
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2	+5.0	+6.0	+1.0	+20	-15	0.05

Characteristic	Symbol	Pin Under Test	MC10177L Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	V_{SC}	V_{SS}	I_{OL1}	I_{OL2}	I_{OH}	C#	(V_{CC}) Gnd
Power Supply Drain	I_E	8	–	–	–	–	96	–	–	mAdc	–	–	–	–	8	–	–	–	–	–	–	1,16
Negative	I_{SSO}	9	–	–	–	–	88	–	–	mAdc	–	–	–	–	8	9	–	–	–	–	–	1,16
Positive Output Low	I_{SSL}	9	–	–	–	–	88	–	–	↓	10,12,14	11,13,15	–	–	↓	↓	–	–	–	–	–	↓
Output High	I_{SSH}	9	–	–	–	–	44	–	–	↓	11,13,15	10,12,14	–	–	↓	↓	–	–	–	–	–	↓
Input Current	I_{inH}	10	–	–	–	–	1.0	–	–	µAdc	10	11	–	–	8	9	–	–	–	–	–	1,16
		11	–	–	–	–	↓	–	–	↓	11	10	–	–	↓	↓	–	–	–	–	–	↓
		12	–	–	–	–	↓	–	–	↓	12	13	–	–	↓	↓	–	–	–	–	–	↓
		13	–	–	–	–	↓	–	–	↓	13	12	–	–	↓	↓	–	–	–	–	–	↓
		14	–	–	–	–	↓	–	–	↓	14	15	–	–	↓	↓	–	–	–	–	–	↓
		15	–	–	–	–	↓	–	–	↓	15	14	–	–	↓	↓	–	–	–	–	–	↓
Input Leakage Current	I_{CBO}	11	–	–	-1.0	–	–	–	–	µAdc	10	–	–	–	8,11	9	–	–	–	–	–	1,16
		13	–	–	↓	–	–	–	–	↓	12	–	–	–	8,13	↓	–	–	–	–	–	↓
		15	–	–	↓	–	–	–	–	↓	14	–	–	–	8,15	↓	–	–	–	–	–	↓
Logic "1" Output Voltage	V_{OH}	2	3.0	–	3.0	–	–	3.0	–	Vdc	15	14	–	–	8	9	–	–	–	2	–	1,16
		2	4.0	–	4.0	–	–	4.0	–	Vdc	15	14	–	–	8	–	9	–	–	2	–	1,16
Logic "0" Output Voltage	V_{OL}	2	–	0.5	–	–	0.5	–	0.5	Vdc	14	15	–	–	8	9	–	2	–	–	–	1,16
		2	–	0.6	–	–	0.6	–	0.6	Vdc	14	15	–	–	8	9	–	–	2	–	–	1,16
Logic "1" Threshold Voltage	V_{OHA}	2	3.0	–	3.0	–	–	3.0	–	Vdc	–	14	15	–	8	9	–	–	–	2	–	1,16
		2	4.0	–	4.0	–	–	4.0	–	Vdc	–	14	15	–	8	–	9	–	–	2	–	1,16
Logic "0" Threshold Voltage	V_{OLA}	2	–	0.5	–	–	0.5	–	0.5	Vdc	14	–	–	15	8	9	–	2	–	–	–	1,16
		2	–	0.6	–	–	0.6	–	0.6	Vdc	14	–	–	15	8	9	–	–	2	–	–	1,16
Output Short-Circuit Current	I_{SC}	2	-50	-90	-50	–	-90	-50	-90	mAdc	15	14	–	–	8	9	–	–	–	–	–	1,2,16
											-1.29 V	-1.69 V	Pulse In	Pulse Out	-5.2 V							
Switching Times	t_{15+2+}	2	–	–	–	6.0	–	–	–	ns	14	11,13	15	2	8	9	–	–	–	–	3,5,7	1,16
(350 pF Load)	t_{15-2-}	2	–	–	–	↓	–	–	–	↓	14	↑	15	↑	↓	↓	–	–	–	–	↓	↓
Propagation Delay	t_{14+2-}	2	–	–	–	↓	–	–	–	↓	15	↑	14	↓	↓	↓	–	–	–	–	↓	↓
	t_{14-2+}	2	–	–	–	↓	–	–	–	↓	15	↑	14	↓	↓	↓	–	–	–	–	↓	↓
Rise Time (10% to 90%)	t_{2+}	2	–	–	–	12	–	–	–	↓	14	↑	15	↓	↓	↓	–	–	–	–	↓	↓
Fall Time (10% to 90%)	t_{2-}	2	–	–	–	12	–	–	–	↓	14	↑	15	↓	↓	↓	–	–	–	–	↓	↓
Supply Source Current (@ 5.0 MHz) (350 pF Load)	I_{SS}	9	–	–	–	83	–	–	–	mA	10,12,14	–	11,13,15	–	8	–	9	–	–	–	3,5,7	1,16

#See test circuit.

SWITCHING TIME TEST CIRCUIT



Input Pulse
t+ = t- = 2.0 ± 0.2 ns
(20% to 80%)

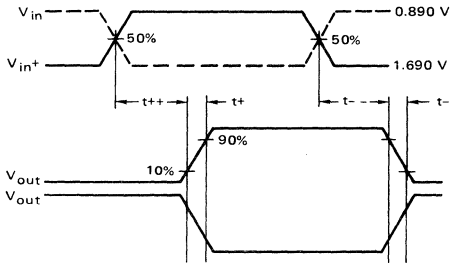
PRF = 5.0 MHz
Duty Cycle = 50%

50-ohm termination to ground located in each scope channel input, and 50-ohm termination to ground on each unmonitored input.

All input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be < 1/4 inch from TP_{in} to input pin and TP_{out} to output pin.

SWITCHING WAVEFORMS @ 25°C

Switching times are measured after the device under test reaches a stabilized temperature (air flow ≥ 500 lfpm)



MC75365

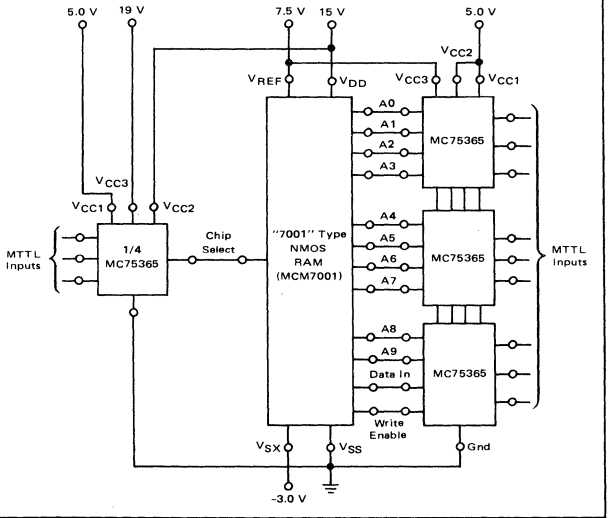
Specifications and Applications Information

QUAD MOS CLOCK DRIVER OR HIGH-VOLTAGE, HIGH-CURRENT NAND DRIVER

The MC75365 is intended for driving the highly capacitive Address, Control and Timing inputs on a variety of MOS RAMs such as the "1103" and "7001" types. It is designed to operate from the MTTL 5.0 V power supply and the V_{SS} and V_{BB} power supplies used with the memories in most applications. Operation is recommended at $V_{CC3} \simeq V_{CC2} + 3$ V, but the part is useable over a wide latitude of supply voltages. V_{CC2} may be tied directly to V_{CC3} in many conditions.

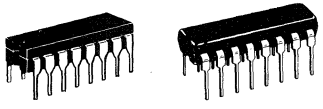
- Pin Compatible with Intel 3207 and Interchangeable with T. I. SN75365
- MTTL and MDTL Compatible, Diode-Clamped Inputs
- Two Common Enable Inputs per Gate Pair
- Low Standby Power Consumption Transient
- Capable of Driving High Capacitive Loads
- Fast Switching Operation

TYPICAL APPLICATION
with "7001" Type 1 K RAM



QUAD MOS CLOCK DRIVER

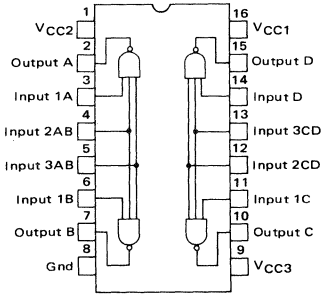
SILICON MONOLITHIC
INTEGRATED CIRCUITS



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

PIN CONNECTIONS



TRUTH TABLE

INPUT			OUTPUT
1	2	3	
H	H	H	L
L	I	I	H
I	L	I	H
I	I	L	H

Where:
H = High Logic State
L = Low Logic State
I = I = Irrelevant

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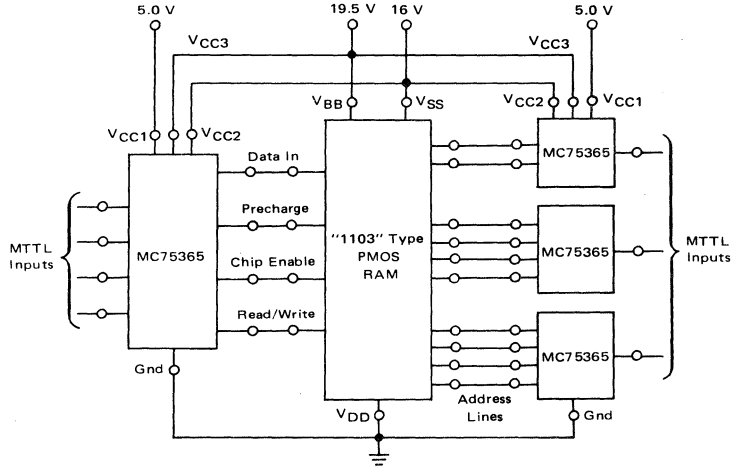
TYPICAL APPLICATION
with "1103" Type 1 K RAM



MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltages	V_{CC1} V_{CC2} V_{CC3}	-0.5 to 7.0 -0.5 to 25 -0.5 to 30	V
Input Voltage	V_I	5.5	V
Input Differential Voltage (see Note 1)	V_{ID}	5.5	V
Power Dissipation (Package Limitation)			
Ceramic Package @ T_A = 25°C	P_D	1000	mW
Derate above T_A = 25°C	$1/R_{\theta JA}$	6.6	mW/°C
Plastic Package @ T_A = 25°C	P_D	830	mW
Derate above T_A = 25°C	$1/R_{\theta JA}$	6.6	mW/°C
Ceramic Package @ T_C = 25°C	P_D	3.0	Watts
Derate above T_C = 25°C	$1/R_{\theta JC}$	20	mW/°C
Plastic Package @ T_C = 25°C	P_D	1.8	Watts
Derate above T_C = 25°C	$1/R_{\theta JC}$	14	mW/°C
Operating Ambient Temperature Range	T_A	0 to 70	°C
Junction Temperature	T_J		°C
Ceramic Package		175	
Plastic Package		150	
Storage Temperature Range	T_{stg}	-65 to +150	°C

Note 1. This is the differential voltage between any two inputs to any single gate.

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Min	Typ	Max	Unit
Power Supply Voltages	V_{CC1}	4.75	5.0	5.25	V
	V_{CC2}	4.75	20	24	
	V_{CC3}	V_{CC2}	24	28	
Difference between V_{CC3} and V_{CC2}	V_{CC3}-V_{CC2}	0	4.0	10	V
Operating Temperature Range	T_A	0	–	70	°C

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ELECTRICAL CHARACTERISTICS (Unless otherwise noted $T_A = 25^oC$, $V_{CC1} = 5.0$ V, $V_{CC2} = 20$ V, $V_{CC3} = 24$ V, $C_L = 200$ pF, $R_D = 24\Omega$, See Figures 1 and 2.)

Characteristic	Symbol	Min	Typ*	Max	Unit
Input Voltage – High Logic State	V_{IH}	2.0	–	–	V
Input Voltage – Low Logic State	V_{IL}	–	–	0.8	V
Input Clamp Voltage ($I_{IC} = -12$ mA)	V_{IC}	–	–	1.5	V
Input Current – Maximum Input Voltage ($V_{IH} = 5.5$ V)	I_{IH1}	–	–	1.0	mA
Input Current – High Logic State	I_{IH2}				μA
(V_{IH} (1) = 2.4 V)		–	–	40	
(V_{IH} (2) or V_{IH} (3) = 2.4 V)		–	–	80	
Input Current – Low Logic State	I_{IL}				mA
(V_{IL} (1) = 0.4 V)		–	-1.0	-1.6	
(V_{IL} (2) or V_{IL} (3) = 0.4 V)		–	-2.0	-3.2	
Output Voltage – High Logic State					V
($V_{CC3} = V_{CC2} + 3.0$ V, $V_{IL} = 0.8$ V, $I_{OH} = -100$ μA)	V_{OH1}	V_{CC2} -0.3	V_{CC2} -0.1	–	
($V_{CC3} = V_{CC2} + 3.0$ V, $V_{IL} = 0.8$ V, $I_{OH} = -10$ mA)	V_{OH2}	V_{CC2} -1.2	V_{CC2} -0.9	–	
($V_{CC3} = V_{CC2}$, $V_{IL} = 0.8$ V, $I_{OH} = -50$ μA)	V_{OH3}	V_{CC2} -1.0	V_{CC2} -0.7	–	
($V_{CC3} = V_{CC2}$, $V_{IL} = 0.8$ V, $I_{OH} = -10$ mA)	V_{OH4}	V_{CC2} -2.3	V_{CC2} -1.8	–	
Output Clamp Voltage ($V_{IL} = 0$ V, $I_{OC} = 20$ mA)	V_{OC}	–	–	V_{CC2} +1.5	V
Output Voltage – Low Logic State					V
($V_{IH} = 2.0$ V, $I_{OL} = 10$ mA)	V_{OL1}	–	0.15	0.3	
($15 \leq V_{CC3} \leq 28$ V, $V_{IH} = 2.0$ V, $I_{OL} = 40$ mA)	V_{OL2}	–	0.25	0.5	
Power Supply Currents – Outputs High Logic State					mA
($V_{CC1} = 5.25$ V, $V_{CC2} = 24$ V, $V_{CC3} = 28$ V,	$I_{CC1(H)}$	–	4.0	8.0	
$V_{IL} = 0$ V, $I_{OH} = 0$ mA)	$I_{CC2(H)}$	–	-2.2	-3.2/+0.25	
	$I_{CC3(H)}$	–	2.2	3.5	
($V_{CC1} = 5.25$ V, $V_{CC2} = 24$ V, $V_{CC3} = 24$ V	$I_{CC2(H)}$	–	–	0.25	
$V_{IL} = 0$ V, $I_{OH} = 0$ mA)	$I_{CC3(H)}$	–	–	0.5	
Power Supply Currents – Output Low Logic State					mA
($V_{CC1} = 5.25$ V, $V_{CC2} = 24$ V, $V_{CC3} = 28$ V	$I_{CC1(L)}$	–	31	47	
$V_{IH} = 5.0$ V, $I_{OL} = 0$ mA)	$I_{CC2(L)}$	–	–	2.5	
	$I_{CC3(L)}$	–	16	25	
Power Supply Currents – Standby Condition					mA
($V_{CC1} = 0$ V, $V_{CC2} = 24$ V, $V_{CC3} = 24$ V	$I_{CC2(S)}$	–	–	0.25	
$V_{IH} = 5.0$ V, $I_{OL} = 0$ mA)	$I_{CC3(S)}$	–	–	0.5	

*Typical Values at 25^oC, $V_{CC1} = 5.0$ V, $V_{CC2} = 20$ V and $V_{CC3} = 24$ V

SWITCHING CHARACTERISTICS (Unless otherwise noted $T_A = 25^oC$, $V_{CC1} = 5.0$ V, $V_{CC2} = 20$ V, $V_{CC3} = 24$ V, $C_L = 200$ pF, $R_D = 24\Omega$, See Figures 1 and 2.)

Characteristic	Symbol	Min	Typ	Max	Unit
Propagation Delay Time, Low to High State Output	t_{PLH}	10	31	48	ns
Propagation Delay Time, High to Low State Output	t_{PHL}	10	30	46	
Delay Time, Low to High State Output	t_{DLH}	–	11	20	ns
Delay Time, High to Low State Output	t_{DHL}	–	10	18	
Transition Time, Low to High State Output	t_{TLH}	–	20	33	ns
Transition Time, High to Low State Output	t_{THL}	–	20	33	

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FIGURE 1 – SWITCHING CHARACTERISTIC TEST CIRCUIT

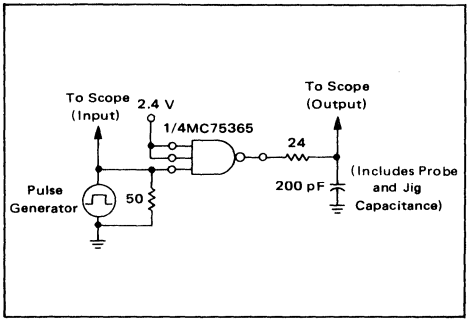
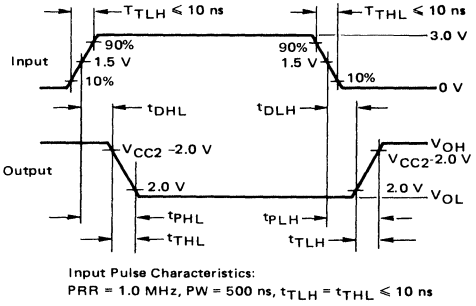


FIGURE 2 – SWITCHING CHARACTERISTICS WAVEFORMS



Input Pulse Characteristics:
PRR = 1.0 MHz, PW = 500 ns, $t_{TLH} = t_{THL} \leq 10$ ns

TYPICAL PERFORMANCE CURVES

FIGURE 3 – OUTPUT VOLTAGE – HIGH LOGIC STATE versus OUTPUT CURRENT

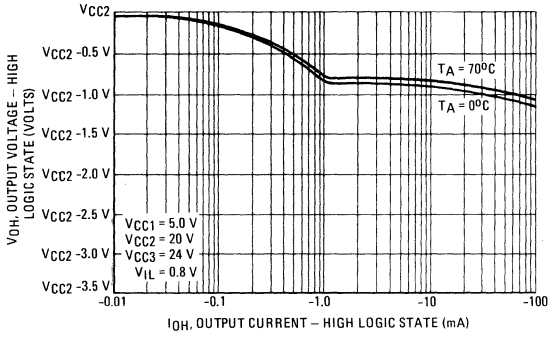


FIGURE 4 – OUTPUT VOLTAGE – HIGH LOGIC STATE versus OUTPUT CURRENT

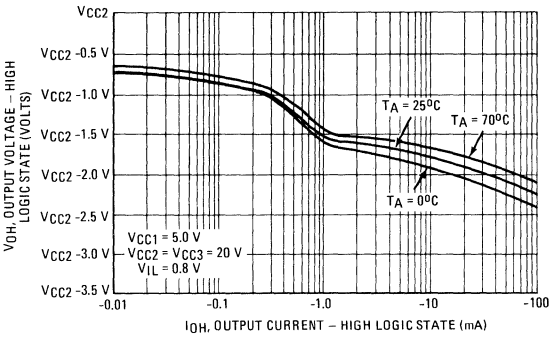


FIGURE 5 – OUTPUT VOLTAGE – LOW LOGIC STATE versus OUTPUT CURRENT

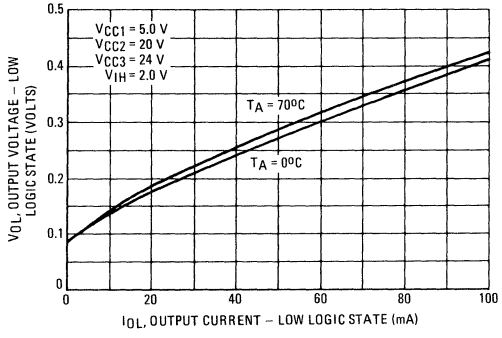
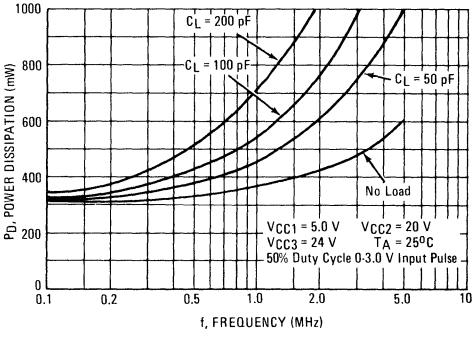


FIGURE 6 – TOTAL POWER DISSIPATION versus FREQUENCY (All Four Drivers)



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TYPICAL PERFORMANCE CURVES

FIGURE 7 – PROPAGATION DELAY TIME – LOW TO HIGH STATE OUTPUT versus AMBIENT TEMPERATURE

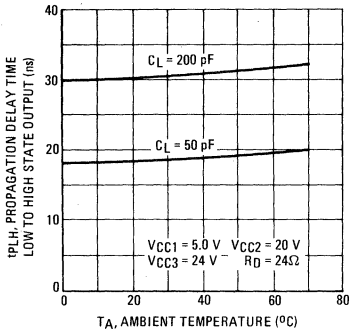


FIGURE 8 – PROPAGATION DELAY TIME – HIGH TO LOW STATE OUTPUT versus AMBIENT TEMPERATURE

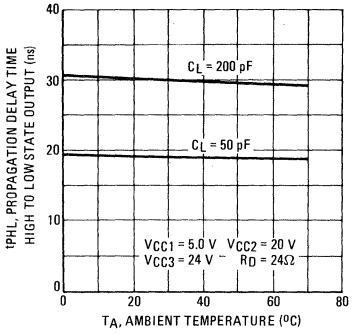


FIGURE 9 – PROPAGATION DELAY TIME – LOW TO HIGH STATE OUTPUT versus V_{CC2} SUPPLY VOLTAGE

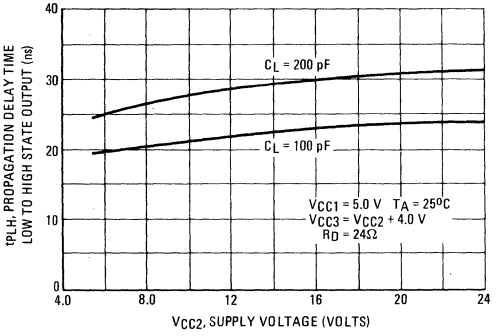


FIGURE 10 – PROPAGATION DELAY TIME – HIGH TO LOW STATE OUTPUT versus V_{CC2} SUPPLY VOLTAGE

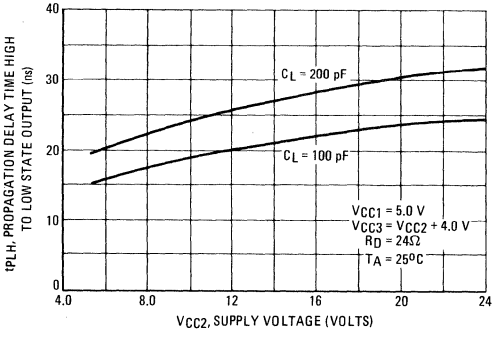


FIGURE 11 – PROPAGATION DELAY TIME – LOW TO HIGH LOGIC STATE versus LOAD CAPACITANCE

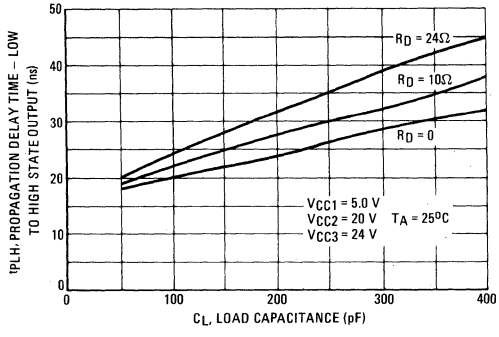
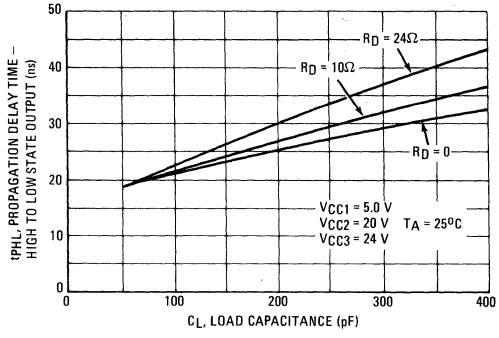


FIGURE 12 – PROPAGATION DELAY TIME – HIGH TO LOW STATE OUTPUT versus LOAD CAPACITANCE



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APPLICATIONS SUGGESTIONS

POWER CONSIDERATIONS

Circuit performance and long-term circuit reliability are affected by die temperature. Normally, both are improved by keeping the integrated circuit junction temperatures low. Electrical power dissipated in the integrated circuit is the source of heat. This heat source increases the temperature of the die relative to some reference point, normally the ambient temperature. The temperature increase depends on the amount of power dissipated in the circuit and on the net thermal resistance between the heat source and the reference point. The basic formula for converting power dissipation into junction temperature is:

$$T_J = T_A + P_D (R_{\theta JC} + R_{\theta CA}) \quad (1)$$

or

$$T_J = T_A + P_D (R_{\theta JA}) \quad (2)$$

where

T_J = junction temperature
T_A = ambient temperature
P_D = power dissipation
$R_{\theta JC}$ = thermal resistance, junction to case
$R_{\theta CA}$ = thermal resistance, case to ambient
$R_{\theta JA}$ = thermal resistance, junction to ambient.

Power Dissipation for the MC75365 MOS Clock Driver:

The power dissipation of the device (P_D) is dependent on the following system requirements: frequency of operation, capacitive loading, output voltage swing, and duty cycle. The variation of power dissipation with frequency and load capacitance for the MC75365 is illustrated in Figure 6. The power dissipation, when substituted into equation (2), should not yield a junction temperature, T_J, greater than T_J(max) at the maximum encountered ambient temperature. T_J(max) is specified for two integrated circuit packages in the maximum ratings section of this data sheet.

With these maximum junction temperature values, the maximum permissible power dissipation at a given ambient temperature may be determined. This can be done with equations (1) and (2) and the maximum thermal resistance values given in Table 1 shown on the following page.

TABLE 1 – THERMAL CHARACTERISTICS OF "L" AND "P" PACKAGES

PACKAGE TYPE (Mounted in Socket)	$R_{\theta JA}$ (°C/W) Still Air		$R_{\theta JC}$ (°C/W) Still Air	
	MAX	TYP	MAX	TYP
"L" (Ceramic Package)	150	100	50	27
"P" (Plastic Package)	150	100	70	40

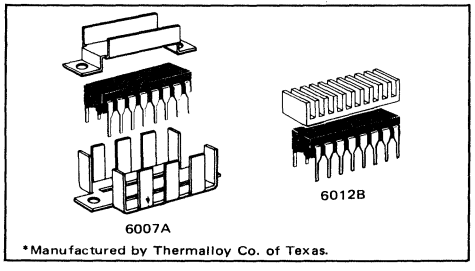
If the power dissipation determined by a given system produces a junction temperature in excess of the recommended maximum rating for a given package type, something must be done to reduce the junction temperature.

There are two methods of lowering the junction temperature without changing the system requirements. First, the ambient temperature may be reduced sufficiently to bring T_J to an acceptable value. Secondly, the $R_{\theta CA}$ term can be reduced. Lowering the $R_{\theta CA}$ term can be accomplished by increasing the surface area of the package with the addition of a heat sink or by blowing air across the package to promote improved heat dissipation.

Heat Sink Considerations:

Heat sinks come in a wide variety of sizes and shapes that will accomodate almost any IC package made. Some of these heat sinks are illustrated in Figure 13.

FIGURE 13 – THERMALLOY* HEAT SINKS



*Manufactured by Thermalloy Co. of Texas.

From Table 1, $R_{\theta JA}$(max) for the ceramic package with no heat sink and in a still air environment is 150°C/W.

For the following example the Thermalloy 6012B type heat sink, or equivalent, is chosen. With this heat sink, the $R_{\theta CA}$ for natural convection from Figure 14 is 44°C/W. From Table 1 $R_{\theta JC}$(max) = 50°C/W for the ceramic package. Therefore, the new $R_{\theta JA}$(max) with the 6012B heat sink added becomes:

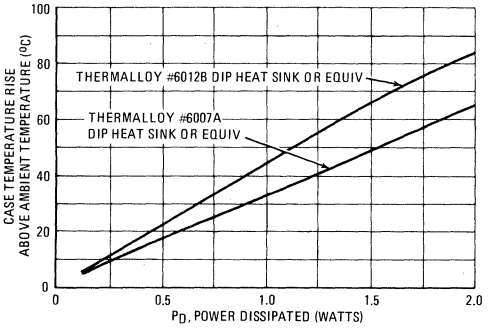
$R_{\theta JA}$(max) = 50°C/W + 44°C/W = 94°C/W.

Thus the addition of the heat sink has reduced $R_{\theta JA}$ (max) from 150°C/W down to 94°C/W. With the heat sink, the maximum power dissipation by equation (2) at T_A = +70°C is:

$$P_D = \frac{175^\circ C - 70^\circ C}{+94^\circ C/W} = 1.11 \text{ watts.}$$

This gives approximately a 60% increase in maximum power dissipation over the power dissipation which is allowable with no heat sink.

FIGURE 14 – CASE TEMPERATURE RISE ABOVE AMBIENT versus POWER DISSIPATED USING NATURAL CONVECTION



Forced Air Considerations:

As illustrated in Figure 15, forced air can be employed to reduce the $R_{\theta JA}$ term. Note, however, that this curve is expressed in terms of typical $R_{\theta JA}$ rather than maximum $R_{\theta JA}$. Maximum $R_{\theta JA}$ can be determined in the following manner:

From Table 1 the following information is known:

(a) $R_{\theta JA}$(typ) = 100°C/W

(b) $R_{\theta JC}$(typ) = 27°C/W

Since:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA} \quad (3)$$

Then:

$$R_{\theta CA} = R_{\theta JA} - R_{\theta JC} \quad (4)$$

Therefore, in still air

$R_{\theta CA}$(typ) = 100°C/W - 27°C/W = 73°C/W

From Curve 1 of Figure 14 at 500 LFPM and equation (4),

$R_{\theta CA}$(typ) = 53°C/W - 27°C/W = 26°C/W.

Thus $R_{\theta CA}$(typ) has changed from 73°C/W (still air) to 26°C/W (500 LFPM), which is a decrease in typical $R_{\theta CA}$ by a ratio of 1:2.8. Since the typical value of $R_{\theta CA}$ was reduced by a ratio of 1:2.8, $R_{\theta CA}$(max) of 100°C/W should also decrease by a ratio of 1:2.8.

This yields an $R_{\theta CA}$(max) at 500 LFPM of 36°C/W. Therefore, from equation (3):

$R_{\theta JA}$(max) = 50°C/W + 36°C/W = 86°C/W.

Therefore the maximum allowable power dissipation at 500 LFPM and T_A = +70°C is from equation (2):

$$P_D = \frac{175^\circ C - 70^\circ C}{86^\circ C/W} = 1.2 \text{ watts.}$$

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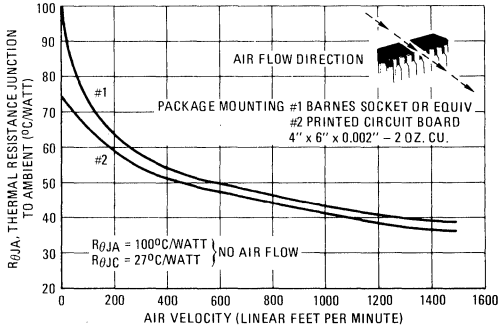
FIGURE 15 – TYPICAL THERMAL RESISTANCE ($R_{\theta JA}$) OF "L" PACKAGE versus AIR VELOCITY



Heat Sink and Forced Air Combined:

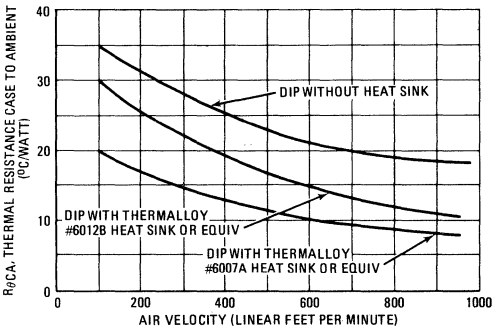
Some heat sink manufacturers provide data and curves of $R_{\theta CA}$ for still air and forced air such as illustrated in Figure 16. For example the 6012B heat sink has an $R_{\theta CA}$ = 17°C/W at 500 LFPM as noted in Figure 15. From equation (3):

Max $R_{\theta JA}$ = 50°C/W + 17°C/W = 67°C/W

From equation (2) at T_A = +70°C

$$P_D = \frac{175^\circ C - 70^\circ C}{67^\circ C/W} = 1.57 \text{ watts.}$$

FIGURE 16 – THERMAL RESISTANCE $R_{\theta CA}$ versus AIR VELOCITY



Note from Table 1 and Figure 15 that if the 16-pin ceramic package is mounted directly to the PC board (2 oz. cu. underneath), that typical $R_{\theta JA}$ is considerably less than for socket mount with still air and no heat sink. The following procedure can be employed to determine the maximum power dissipation for this condition.

Given data from Table 1:

typical $R_{\theta JA}$ = 100°C/W

typical $R_{\theta JC}$ = 27°C/W

From Curve 2 of Figure 15, $R_{\theta JA}$(typ) is 75°C/W for a PC mount and no air flow. Then the typical $R_{\theta CA}$ is 75°C/W – 27°C/W = 48°C/W. From Table 1 the typical value of $R_{\theta CA}$ for socket mount is 100°C/W – 27°C/W = 73°C/W. This shows that the PC board mount results in a decrease in typical $R_{\theta CA}$ by a ratio of 1:1.5 below the typical value of $R_{\theta CA}$ in a socket mount. Therefore, the maximum value of socket mount $R_{\theta CA}$ of 100°C/W should also decrease by a ratio of 1:1.5 when the device is mounted in a PC board. The maximum $R_{\theta CA}$ becomes:

$$R_{\theta CA} = \frac{100^\circ C/W}{1.5} = 66^\circ C/W \text{ for PC board mount}$$

Therefore the maximum $R_{\theta JA}$ for a PC mount is from equation (3).

$R_{\theta JA}$ = 50°C/W + 66°C/W = 116°C/W.

With maximum $R_{\theta JA}$ known, the maximum power dissipation can be found. If T_A = 70°C then from equation (2) the maximum power dissipation may be found to be 905 mW.

In most cases, heat sink manufacturer's publish only $R_{\theta CA}$ socket mount data. Although data for PC mounting is generally not available, this should present no problem. Note in Figure 15 that an air flow greater than 250 LFPM yields a socket mount $R_{\theta JA}$ approximately 6% greater than for a PC mount. Therefore, the socket mount data can be used for a PC mount with a slightly greater safety factor. Also it should be noted that thermal resistance measurements can vary widely. These measurement variations are due to the dependency of $R_{\theta CA}$ of the type environment and measurement techniques employed. For example, $R_{\theta CA}$ would be greater for an integrated circuit mounted on a PC board with little or no ground plane versus one with a substantial ground plane. Therefore, if the maximum calculated junction temperature is on the border line of being too high for a given system application, then thermal resistance measurements should be done on the system to be absolutely certain that the maximum junction temperature is not exceeded.

MC75368
MC75358

Specifications and Applications Information

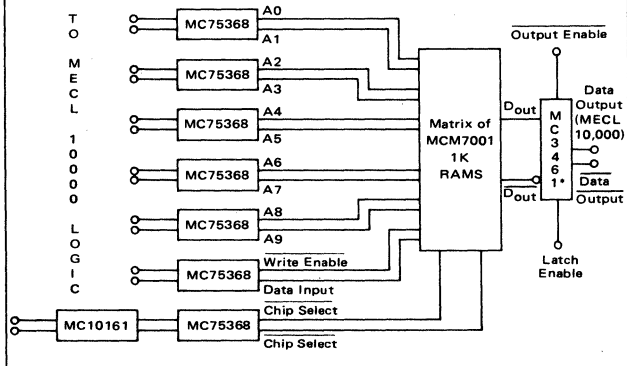
DUAL MECL-to-MOS DRIVERS

The MC75368 and MC75358 are dual MECL-to-MOS driver and interface circuits. The devices accept standard MECL 10,000 and IBM grounded-reference ECL input signals and create high-current and high-voltage output levels suitable for driving MOS circuits. Specifically, they may be used to drive address, control, and timing inputs for several types of MOS RAMs including high-speed MCM7001 1K NMOS RAM. The devices may also be used as MECL-to-MTTL translators.

These two devices differ in that the MC75368 is optimized for higher voltage capability and the MC75358 version is made to operate at somewhat reduced maximum voltages.

- Dual MECL-to-MOS Driver
- Dual MECL-to-MTTL Driver
- Versatile Interface Circuit for Use Between MECL and High-Current, High-Voltage Systems

FIGURE 1 – TYPICAL APPLICATION WITH MCM7001 1K NMOS RAM
(See Figure 8 and 9 for details)

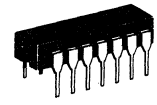


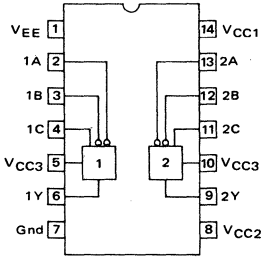
*MC3461 Dual Sense Amplifier to be announced 1st Quarter 1975.

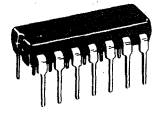
DUAL MECL-to-MOS DRIVERS

SILICON MONOLITHIC INTEGRATED CIRCUITS

L SUFFIX
CERAMIC PACKAGE
CASE 632
TO-116







P SUFFIX
PLASTIC PACKAGE
CASE 646

FUNCTION TABLE

Input Voltage Conditions		Output
Differential	Logic Level	
(More positive of A or B) -C	A B C	Y
($V_{ID} \geq 150$ mV)	L H L H L H H H L	L
(-150 mV $\leq V_{ID} \leq$ 150 mV)	X X X	Indeterminate
($V_{ID} \leq$ -150 mV)	L L H	H

H = high logic level, L = low logic level,
X = irrelevant

MAXIMUM RATINGS (Unless otherwise noted, voltages measured with respect to GND terminals, $T_A = 25^oC$.)

Rating	Symbol	Value	Unit
Power Supply Voltages	V_{CC1}	-0.5 to 7.0	Vdc
MC75368 MC75358	V_{CC2}	-0.5 to 22 -0.5 to 18	Vdc
MC75368 MC75358	V_{CC3}	-0.5 to 30 -0.5 to 24	Vdc
	V_{EE}	-8.0 to 0.5	Vdc
Most Negative of V_{CC1}, V_{CC2}, or V_{CC3} with respect to V_{EE}	–	-0.5	Vdc
Input Voltage	V_I	-8.0 to 0.5	Vdc
Inter-Input Voltage(1)	–	5.5	Vdc
Most negative Input Voltage with respect to V_{EE}	$V_I - V_{EE}$	-5.0	Vdc
Power Dissipation (Package Limitation)			
Ceramic Package @ $T_A = 25^oC$	P_D	1000	mW
Derate above $T_A = 25^oC$	$1/R_{\theta JA}$	6.6	$mW/^oC$
Plastic Package @ $T_A = 25^oC$	P_D	830	mW
Derate above $T_A = 25^oC$	$1/R_{\theta JA}$	6.6	$mW/^oC$
Ceramic Package @ $T_C = 25^oC$	P_D	3.0	Watts
Derate above $T_C = 25^oC$	$1/R_{\theta JC}$	20	$mW/^oC$
Plastic Package @ $T_C = 25^oC$	P_D	1.8	Watts
Derate above $T_C = 25^oC$	$1/R_{\theta JC}$	14	$mW/^oC$
Operating Ambient Temperature Range	T_A	0 to 70	^oC
Storage Temperature Range	T_{stg}	-65 to 150	^oC

(1) With respect to any pair of inputs to either of the input gates.

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	MC75358			MC75368			Unit
		Min	Typ	Max	Min	Typ	Max	
Power Supply Voltages	V_{CC1}	4.75	5.0	5.25	4.75	5.0	5.25	V
	V_{CC2}	4.75	16	18	4.75	20	22	V
	V_{CC3}	V_{CC2}	20	22	V_{CC2}	24	28	V
	$V_{CC3} - V_{CC2}$	0	4.0	10	0	4.0	10	V
	V_{EE}	-4.68	-5.2	-5.72	-4.68	-5.2	-5.72	V
Operating Ambient Temperature Range	T_A	0	–	70	0	–	70	^oC
DEFINITION OF INPUT LOGIC LEVELS								
Input Voltage – High Logic State (Any Input) (1)	V_{IH}	-1.5	–	-0.7	-1.5	–	-0.7	V
Input Voltage – Low Logic State (Any Input) (1)	V_{IL}	V_{EE}	–	V_{IH}-150	V_{EE}	–	V_{IH}-150	mV
Input Differential Voltage – High Logic State (2)	V_{IDH}	150	–	–	150	–	–	mV
Input Differential Voltage – Low Logic State (2)	V_{IDL}	-150	–	–	-150	–	–	mV

(1) The definition of these Logic Levels use Algebraic System of notation.

(2) The input differential voltage is measured from the more positive inverting input (A or B) with respect to the non-inverting input (C) of the same gate.

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ELECTRICAL CHARACTERISTICS (Unless otherwise noted, specifications apply over recommended power supply and temperature ranges. Typical values measured at V_{CC1} = 5.0 V, V_{EE} = -5.2 V, T_A = 25°C and V_{CC2} = 20, V_{CC3} = 24 V for MC75368 and V_{CC2} = 16, V_{CC3} = 20 V for MC75358.

Characteristic	Symbol	MC75358 Min	MC75358 Typ	MC75358 Max	MC75368 Min	MC75368 Typ	MC75368 Max	Unit
Output Voltage — High Logic State								V
(V_{CC3} = V_{CC2} + 3.0 V, V_{IDL} = -150 mV, I_{OH} = -100 μA)	V_{OH1}	V_{CC2} - 0.3	V_{CC2} - 0.1	–	V_{CC2} - 0.3	V_{CC2} - 0.1	–	
(V_{CC3} = V_{CC2} + 3.0 V, V_{IDL} = -150 mV, I_{OH} = -10 mA)	V_{OH2}	V_{CC2} - 1.2	V_{CC2} - 0.9	–	V_{CC2} - 1.2	V_{CC2} - 0.9	–	
(V_{CC3} = V_{CC2}, V_{IDL} = -150 mV, I_{OH} = -50 μA)	V_{OH3}	V_{CC2} - 1.0	V_{CC2} - 0.7	–	V_{CC2} - 1.0	V_{CC2} - 0.7	–	
(V_{CC3} = V_{CC2}, V_{IDL} = -150 mV, I_{OH} = -10 mA)	V_{OH4}	V_{CC2} - 2.3	V_{CC2} - 1.8	–	V_{CC2} - 2.3	V_{CC2} - 1.8	–	
Output Voltage — Low Logic State								V
(V_{IDH} = 150 mV, I_{OL} = 10 mA)	V_{OL1}	–	0.15	0.3	–	0.15	0.3	
(V_{IDH} = 150 mV, I_{OL} = 30 mA)	V_{OL2}							
10 V ≤ V_{CC3} ≤ 22 V		–	0.2	0.4	–	–	–	
10 V ≤ V_{CC2} ≤ 28 V		–	–	–	–	0.2	0.4	
Output Clamp Voltage (V_{IDH} = 500 mV, I_{OC} = 20 mA)	V_{OC}	–	–	V_{CC2}+1.5 V	–	–	V_{CC2}+1.5 V	V
Input Current — High Logic State (V_{EE} = -5.72 V, V_{IL} = -5.72 V, V_{IH} = -0.7 V)	I_{IH}	–	300	800	–	300	800	μA
Input Current — Low Logic State								μA
(V_{IH} = -0.7 V, V_{IL} = -2.0 V)	I_{IL1}	–	–	-10	–	–	-10	
(V_{EE} = -5.72 V, V_{IH} = -0.7 V, V_{IL} = -5.72 V)	I_{IL2}	–	–	-100	–	–	-100	
Power Supply Current — Both Outputs High Logic State (V_{CC} = 5.25 V, V_{EE} = -5.72 V, $V_{IL(A)}$ and (B) = -2.0 V, $V_{IH(C)}$ = -0.7 V, I_{OH} = 0)								
MC75368 — V_{CC2} = 22 V, V_{CC3} = 26 V	$I_{CC1(H)}$	–	21	38	–	21	38	mA
MC75358 — V_{CC2} = 18 V, V_{CC3} = 22 V	$I_{CC2(H)}$	–	-1.1	+0.25 -1.6	–	-1.1	+0.25 -1.6	mA
	$I_{CC3(H)}$	–	0.6	1.0	–	0.6	1.0	mA
	$I_{EE(H)}$	–	-21	-38	–	-21	-38	mA
Power Supply Current — Both Outputs Low Logic State (V_{CC1} = 5.25 V, V_{EE} = -5.72 V, $V_{IH(A)}$ and (B) = -0.7 V, $V_{IL(C)}$ = -2.0 V, I_{OL} = 0)								
MC75368 — V_{CC2} = 22 V, V_{CC3} = 28 V	$I_{CC1(L)}$	–	13	24	–	13	24	mA
MC75358 — V_{CC2} = 18 V, V_{CC3} = 22 V	$I_{CC2(L)}$	–	0.5	1.0	–	0.5	1.0	mA
	$I_{CC3(L)}$	–	3.0	5.7	–	4.0	7.0	mA
	$I_{EE(L)}$	–	-21	-38	–	-21	-38	mA
Power Supply Current — Both Outputs High Logic State (V_{CC1} = 5.25 V, V_{EE} = -5.72 V, $V_{IL(A)}$ and (B) = -2.0 V, $V_{IH(C)}$ = -0.7 V, I_{OL} = 0)								
MC75368 — V_{CC2} = 22 V, V_{CC3} = 22 V	$I_{CC2(H)}$	–	–	0.25	–	–	0.25	mA
MC75358 — V_{CC2} = 18 V V_{CC3} = 18 V	$I_{CC3(H)}$	–	–	0.25	–	–	0.25	mA
Power Supply Current — Stand By Condition (V_{CC1} = 0 V, V_{EE} = 0 V, $V_{IH(A)}$ and (B) = -0.7 V, $V_{IL(C)}$ = -2.0 V, I_{OL} = 0)								
MC75368 — V_{CC2} = 22 V, V_{CC3} = 22 V	$I_{CC2(S)}$	–	–	0.25	–	–	0.25	mA
MC75358 — V_{CC2} = 18 V, V_{CC3} = 18 V	$I_{CC3(S)}$	–	–	0.25	–	–	0.25	mA

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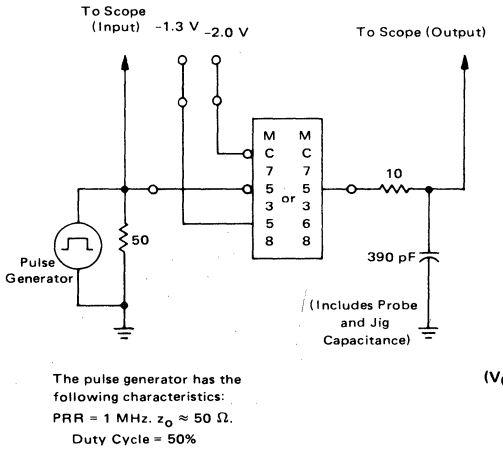
SWITCHING CHARACTERISTICS (Unless otherwise noted, V_{CC1} = 5.0 V, V_{EE} = -5.2 V, T_A = 25°C and V_{CC2} = 20 V for MC75368 and V_{CC2} = 16 V for MC75358)

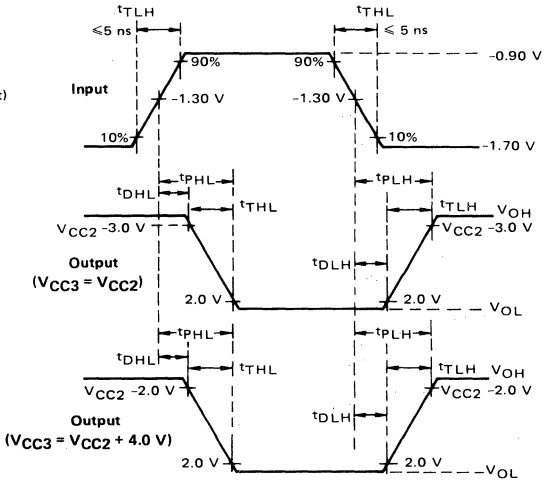
Characteristic	Symbol	MC75358			MC78368			Unit
		Min	Typ	Max	Min	Typ	Max	
Delay Time – Low to High Output Logic Level	t_{DLH}							ns
(V_{CC3} = 24 V)		–	–	–	–	12	24	
(V_{CC3} = 20 V)		–	13	24	–	13	25	
(V_{CC3} = 16 V)		–	14	26	–	–	–	
Delay Time – High to Low Output Logic Level	t_{DHL}							ns
(V_{CC3} = 24 V)		–	–	–	–	13	24	
(V_{CC3} = 20 V)		–	13	24	–	15	26	
(V_{CC3} = 16 V)		–	15	26	–	–	–	
Transition Time, Low-to-High Output Logic Level	t_{TLH}							ns
(V_{CC3} = 24 V)		–	–	–	–	19	30	
(V_{CC3} = 20 V)		–	17	29	–	20	30	
(V_{CC3} = 16 V)		–	18	30	–	–	–	
Transition Time, High-to-Low Output Logic Level	t_{THL}							ns
(V_{CC3} = 24 V)		–	–	–	–	20	33	
(V_{CC3} = 20 V)		–	17	29	–	18	30	
(V_{CC3} = 16 V)		–	16	29	–	–	–	
Propagation Delay Time, Low-to-High Logic Level	t_{PLH}							ns
(V_{CC3} = 24 V)		–	–	–	–	31	54	
(V_{CC3} = 20 V)		–	30	53	–	33	55	
(V_{CC3} = 16 V)		–	32	56	–	–	–	
Propagation Delay Time, High-to-Low Logic Level	t_{PHL}							ns
(V_{CC3} = 24 V)		–	–	–	–	33	57	
(V_{CC3} = 20 V)		–	30	53	–	33	56	
(V_{CC3} = 16 V)		–	31	55	–	–	–	

FIGURE 2 – SWITCHING TIMES TEST CIRCUIT



The pulse generator has the following characteristics:
PRR = 1 MHz. $z_o \approx 50\ \Omega$.
Duty Cycle = 50%

FIGURE 3 – SWITCHING TIMES WAVEFORM

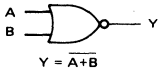


7

APPLICATIONS INFORMATION

MODES OF OPERATION

FIGURE 4 – POSITIVE-NOR GATE

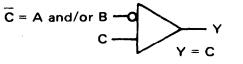


FUNCTION TABLE

CONFIGURATION	INPUTS A	B	C	OUTPUT Y
C at V_{BB}	L	L	V_{BB}	H
	H	X	V_{BB}	L
	X	H	V_{BB}	L

H – High Level, L – Low Level, X – Irrelevant
V_{BB} – Reference Supply voltage for MECL 10,000.

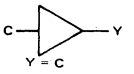
FIGURE 5 – DIFFERENTIAL MECL LINE RECEIVER



FUNCTION TABLE

CONFIGURATION	INPUTS A	B	C	OUTPUT Y
A and B connected together	H	H	L	L
	L	L	H	H
A not used but connected low	L	H	L	L
	L	L	H	H
B not used but connected low	H	L	L	L
	L	L	H	H

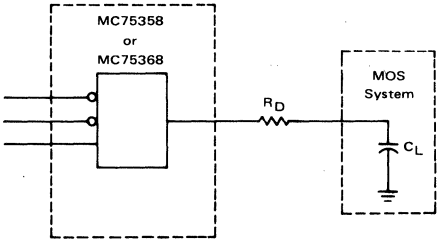
FIGURE 6 – NON-INVERTING GATE



FUNCTION TABLE

CONFIGURATION	INPUTS A	B	C	OUTPUT Y
A and B at V_{BB}	V_{BB}	V_{BB}	L	L
	V_{BB}	V_{BB}	H	H
A at V_{BB}, B connected low	V_{BB}	L	L	L
	V_{BB}	L	H	H
B at V_{BB}, A connected low	L	V_{BB}	L	L
	L	V_{BB}	H	H

FIGURE 7 – USE OF DAMPING RESISTOR TO REDUCE OR ELIMINATE OUTPUT TRANSIENT OVERSHOOT IN CERTAIN MC75358 AND MC75368 APPLICATIONS



Note: $R_D \approx 10\Omega$ to 30Ω (optional)

The MC75368 and MC75358 are identical except that the MC75368 version has been selected for slightly higher voltage capability. The two devices are interchangeable in most applications. Both can operate over a wide range of V_{CC2} and V_{CC3} supply voltages.

The need for four separate power supplies V_{CC1}, V_{CC2}, V_{CC3} and V_{EE} can be avoided in many cases by tying V_{CC2} to V_{CC3}. However, performance advantages can be obtained by connecting either one or both V_{CC3} pins to an additional power supply of higher voltage than V_{CC2}. Both V_{CC3} pins do not have to be held at the same voltage. For MECL-to-TTL level converter applications both V_{CC2} and V_{CC3} are generally connected to a +5.0 V power source.

By providing two out-of-phase (A and B) inputs and one in-phase (C) input, each gate can be used as positive NOR, or as a inverting or non-inverting gate. This flexibility is achieved by connecting an externally supplied MECL 10,000 Series reference supply voltage (V_{BB}) to the appropriate input as shown in Figures 4 thru 6. An unused out-of-phase input should be tied low or connected to the other out-of-phase input of the same gate. The required V_{BB} voltage source may be obtained from MECL 10,000 Series devices such as the MC10115 line receiver, or by connecting the output of a MECL 10,000 gate, like the MC10102, to the respective out-of-phase inputs (as an example connect pins 4 and 5 to 2 of the MC10102 to obtain a V_{BB} reference voltage).

When driven differentially, the MC75368 and MC75358 may be used as a differential MECL line receiver, without the need for the V_{BB} reference voltage.

Undesirable output transient overshoot due to load or wiring inductance and the fast switching speeds of the MC75368 and MC75358 can be eliminated or reduced by adding a small amount of series resistance. The value of this damping resistance is dependent on specific load characteristics and switching speed but typical values lie in the range of 10 to 30 ohms. This is illustrated in Figure 7.

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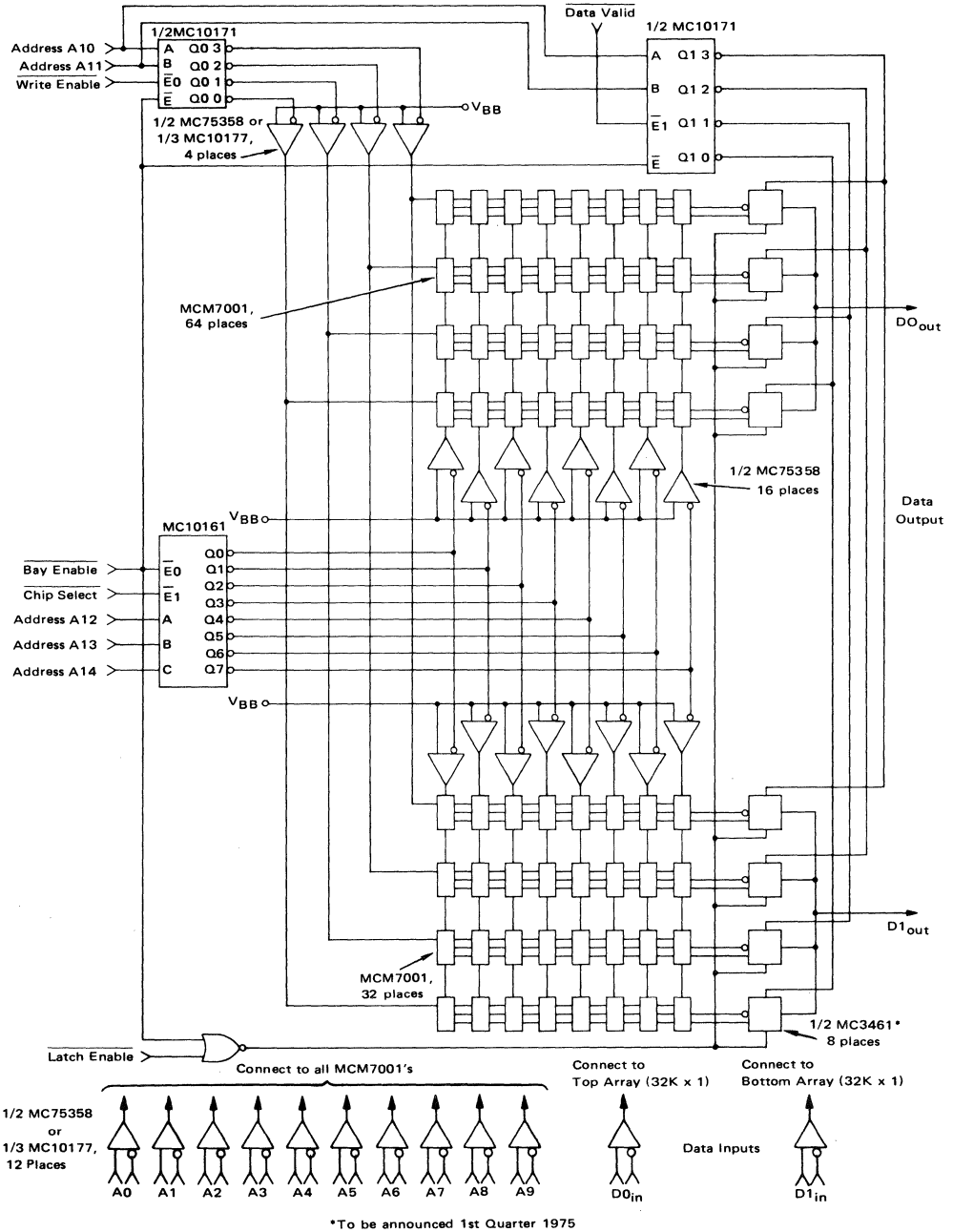
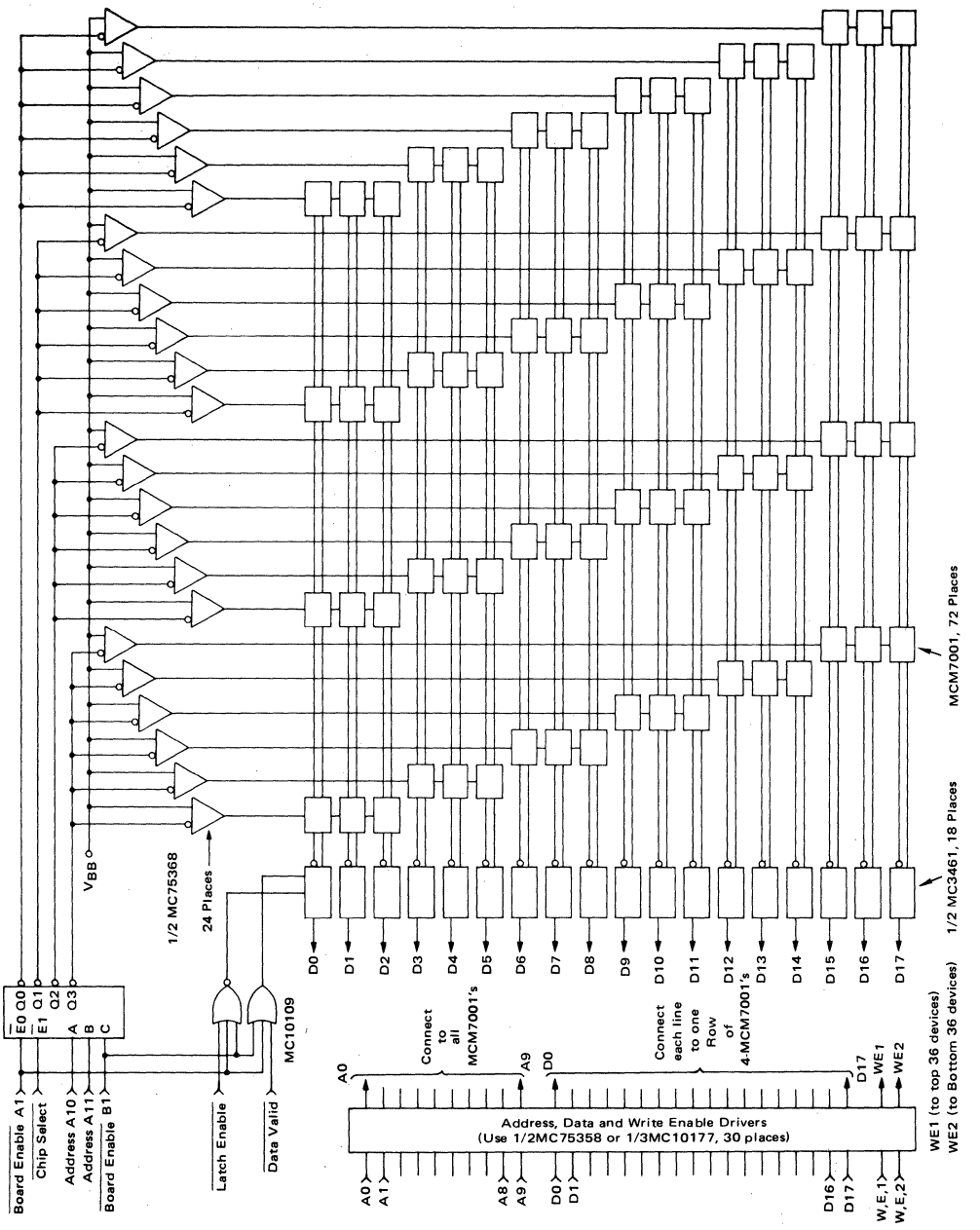
FIGURE 8 – 32K x 2 MEMORY BOARD (MECL SYSTEM)



*To be announced 1st Quarter 1975

FIGURE 9 – 4K x 18 MEMORY BOARD (MECL SYSTEM)



MMH0026
MMH0026C

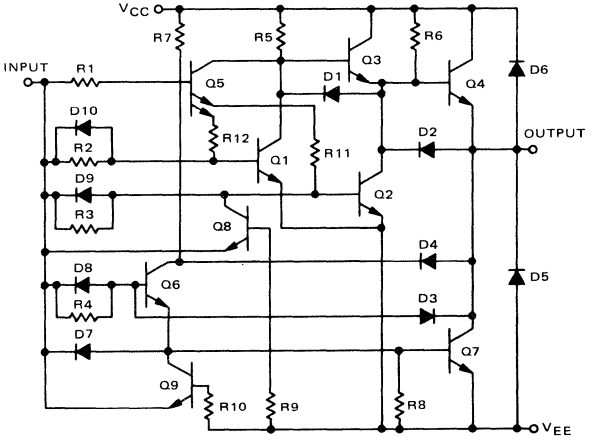
Specifications and Applications Information

DUAL MOS CLOCK DRIVER

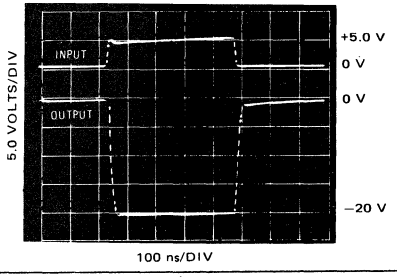
. . . designed for high-speed driving of highly capacitive loads in a MOS system.

- Fast Transition Times – 20 ns with 1000 pF Load
- High Output Swing – 20 Volts
- High Output Current Drive – ±1.5 Amperes
- High Repetition Rate – 5.0 to 10 MHz Depending on Load
- MTTL and MDTL Compatible Inputs
- Low Power Consumption when in MOS "0" State – 2.0 mW
- +5.0-Volt Operation for N-Channel MOS Compatibility

FIGURE 1 – CIRCUIT SCHEMATIC
(1/2 CIRCUIT SHOWN)



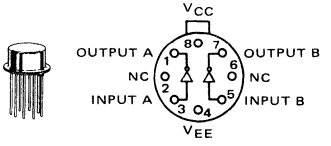
TYPICAL OPERATION
(R_S = 10 Ω, C_L = C_{in} = 1000 pF, f = 1.0 MHz,
PW = 500 ns, V_{CC} = 0 V, V_{EE} = -20 V)



DUAL MOS CLOCK DRIVER

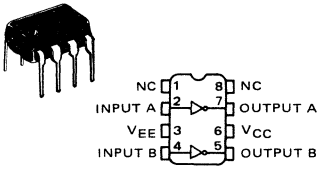
MONOLITHIC SILICON INTEGRATED CIRCUIT

G SUFFIX
METAL PACKAGE
CASE 601



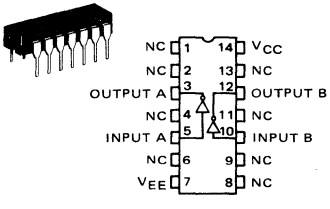
(Top View)

P1 SUFFIX
PLASTIC PACKAGE
CASE 626
(MMH0026C Only)



(Top View)

L SUFFIX
CERAMIC PACKAGE
CASE 632
TO-116



(Top View)

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MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value			Unit
Differential Supply Voltage	$V_{CC}-V_{EE}$	+22			Vdc
Input Current	I_{in}	+100			mA
Input Voltage	V_{in}	V_{EE} + 5.5			Vdc
Peak Output Current	I_{Opk}	±1.5			A
		G Pkg.	L Pkg.	Pl Pkg.	
Power Dissipation and Thermal Characteristics					
T_A = +25°C	P_D	680	1000	830	mW
Thermal Resistance, Junction to Air	θ_{JA}	220	150	150	°C/W
T_C = 25°C	P_D	2.1	3.0	1.8	W
Thermal Resistance, Junction to Case	θ_{JC}	70	50	70	°C/W
Junction Temperature	T_J	+175	+175	+150	°C
Operating Temperature Range	T_A				°C
MMH0026		-55 to +125	-55 to +125	–	
MMH0026C		0 to +85	0 to +85	0 to +85	
Storage Temperature Range	T_{stg}	-65 to +150	-65 to +150	-65 to +150	°C

ELECTRICAL CHARACTERISTICS ($V_{CC}-V_{EE}$ = 10 V to 20 V, C_L = 1000 pF, T_A = -55 to +125°C for MMH0026 and 0 to +85°C for MMH0026C for min and max values; T_A = +25°C for all typical values unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Logic "1" Level Input Voltage $V_O = V_{EE}$ + 1.0 Vdc	V_{IH}	V_{EE} + 2.5	V_{EE} + 1.5	–	Vdc
Logic "1" Level Input Current $V_{in}-V_{EE}$ = 2.5 Vdc, $V_O = V_{EE}$ + 1.0 Vdc	I_{IH}	–	10	15	mA
Logic "0" Level Input Voltage $V_O = V_{CC}$ -1.0 Vdc	V_{IL}	–	V_{EE} + 0.6	V_{EE} + 0.4	Vdc
Logic "0" Level Input Current $V_{in}-V_{EE}$ = 0 Vdc, $V_O = V_{CC}$ -1.0 Vdc	I_{IL}	–	-0.005	-10	μA
Logic "0" Level Output Voltage V_{CC} = +5.0 Vdc, V_{EE} = -12 Vdc, V_{in} = -11.6 Vdc $V_{in}-V_{EE}$ = 0.4 Vdc	V_{OH}	 4.0 V_{CC} -1.0	 4.3 V_{CC} -0.7	 – –	Vdc
Logic "1" Level Output Voltage V_{CC} = +5.0 Vdc, V_{EE} = -12 Vdc, V_{in} = -9.5 Vdc $V_{in}-V_{EE}$ = 2.5 Vdc	V_{OL}	 – –	 -11.5 V_{EE} + 0.5	 -11 V_{EE} + 1.0	Vdc
"On" Supply Current $V_{CC}-V_{EE}$ = 20 Vdc, $V_{in}-V_{EE}$ = 2.5 Vdc	I_{CCL}	–	30	40	mA
"Off" Supply Current $V_{CC}-V_{EE}$ = 20 Vdc, $V_{in}-V_{EE}$ = 0 V	I_{CCH}	–	10	100	μA

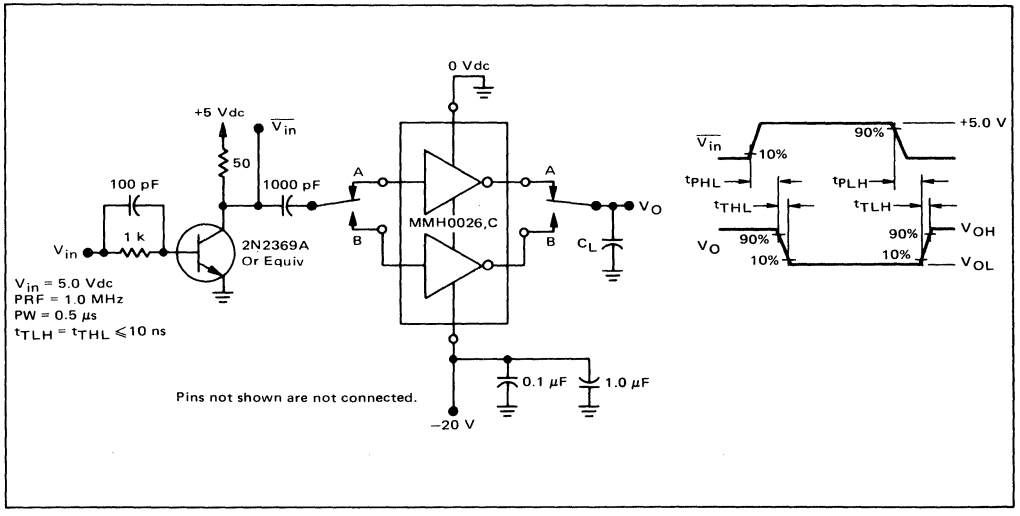
SWITCHING CHARACTERISTICS (See Figure 2.) ($V_{CC}-V_{EE}$ = 10 V to 20 V, C_L = 1000 pF, T_A = -55 to +125°C for MMH0026 and 0 to +85°C for MMH0026C for min and max values; T_A = +25°C for all typical values unless otherwise noted.)

Propagation Time					
High to Low	t_{PHL}	5.0	7.5	12	ns
Low to High	t_{PLH}	5.0	12	15	
Transition Time (High to Low)	t_{THL}				ns
$V_{CC}-V_{EE}$ = 17 Vdc, C_L = 250 pF		–	12	–	
$V_{CC}-V_{EE}$ = 17 Vdc, C_L = 500 pF		–	15	18	
$V_{CC}-V_{EE}$ = 20 Vdc, C_L = 1000 pF		–	20	35	
Transition Time (Low to High)	t_{TLH}				ns
$V_{CC}-V_{EE}$ = 17 Vdc, C_L = 250 pF		–	10	–	
$V_{CC}-V_{EE}$ = 17 Vdc, C_L = 500 pF		–	12	16	
$V_{CC}-V_{EE}$ = 20 Vdc, C_L = 1000 pF		–	17	25	

7

TEST CIRCUIT

FIGURE 2 – AC TEST CIRCUIT AND WAVEFORMS



TYPICAL APPLICATIONS

FIGURE 3 – AC-COUPLED MOS CLOCK DRIVER

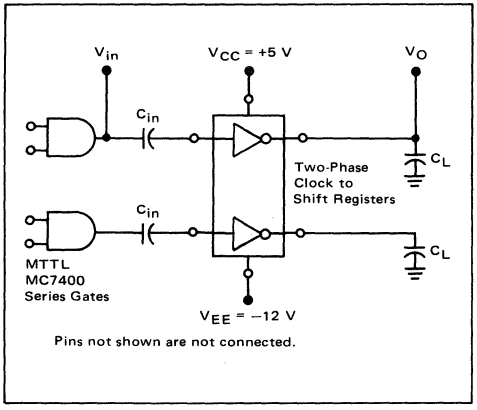
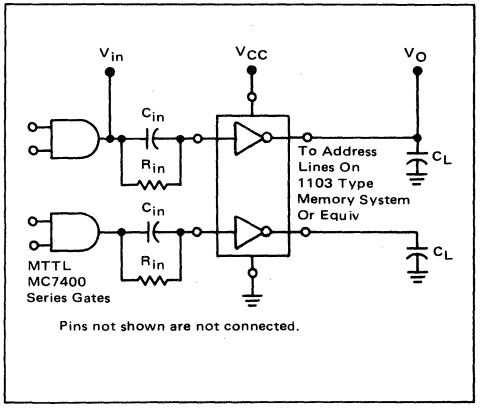


FIGURE 4 – DC-COUPLED RAM MEMORY ADDRESS OR PRECHARGE DRIVER (POSITIVE-SUPPLY ONLY)



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TYPICAL CHARACTERISTICS

(V_{CC} = + 20 V, V_{EE} = 0 V, T_A = +25°C unless otherwise noted.)

FIGURE 5 – INPUT CURRENT versus INPUT VOLTAGE

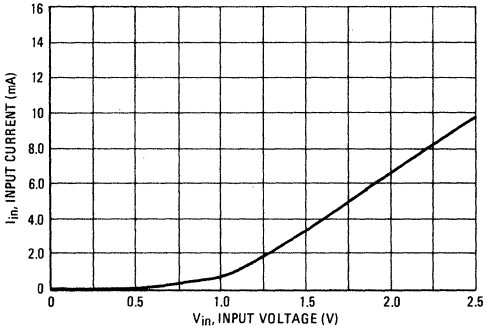


FIGURE 6 – SUPPLY CURRENT versus TEMPERATURE

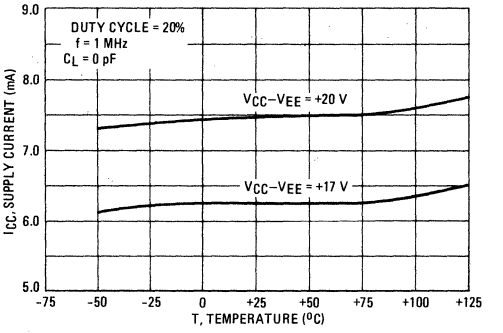


FIGURE 7 – OPTIMUM INPUT CAPACITANCE versus OUTPUT PULSE WIDTH

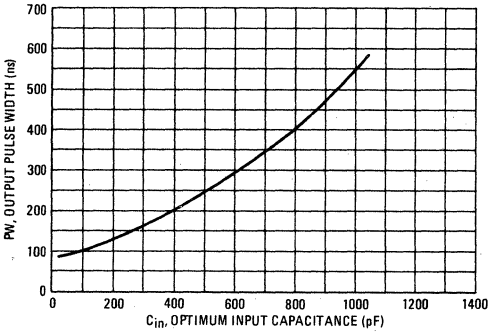


FIGURE 8 – TRANSITION TIMES versus LOAD CAPACITANCE

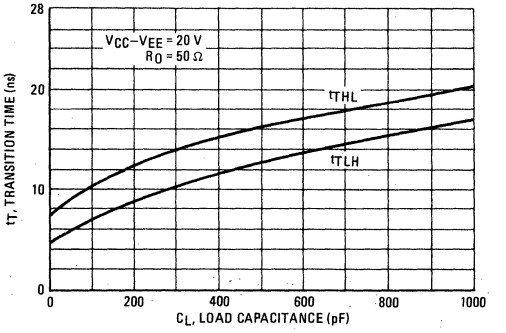


FIGURE 9 – PROPAGATION DELAY TIMES versus TEMPERATURE

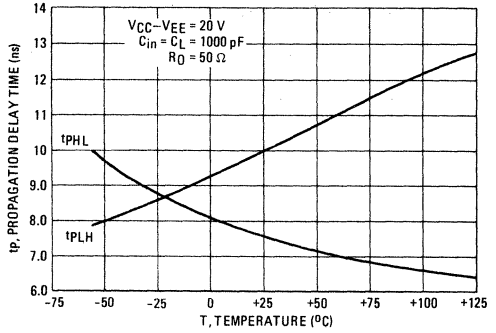
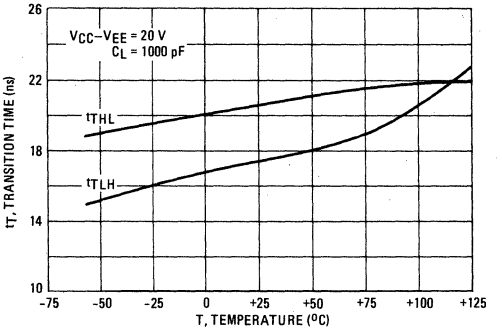


FIGURE 10 – TRANSITION TIMES versus TEMPERATURE



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TYPICAL CHARACTISTICS (continued)

(V_{CC} = + 20 V, V_{EE} = 0 V, T_A = +25°C unless otherwise noted.)

FIGURE 11 – TRANSITION TIME versus TEMPERATURE FOR +5 VOLT DC-COUPLED OPERATION (See Figure 4.)

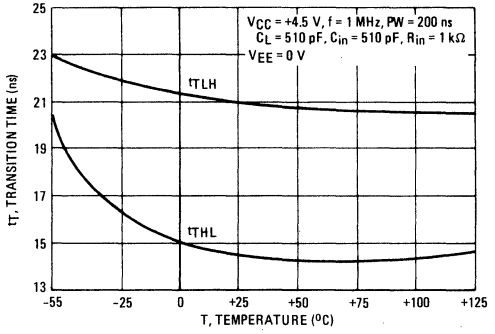


FIGURE 12 – PROPAGATION DELAY TIME versus TEMPERATURE FOR +5 VOLT DC-COUPLED OPERATION (See Figure 4.)

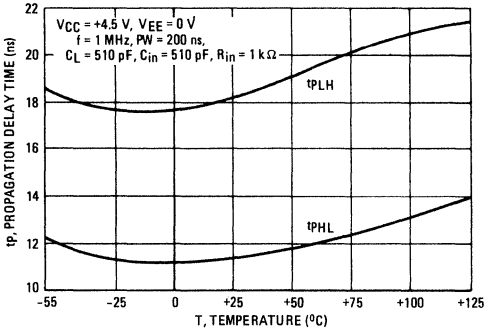


FIGURE 13 – DC-COUPLED SWITCHING RESPONSE versus R_{in} (See Figure 4.)

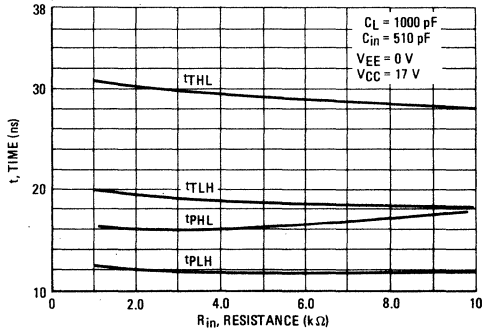


FIGURE 14 – DC-COUPLED SWITCHING versus C_{in} (See Figure 4.)

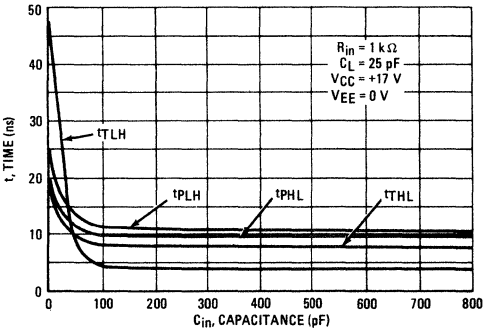


FIGURE 15 – MAXIMUM DC POWER DISSIPATION versus DUTY CYCLE (SINGLE DRIVER)

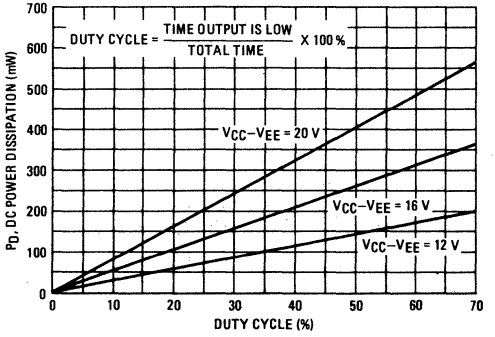
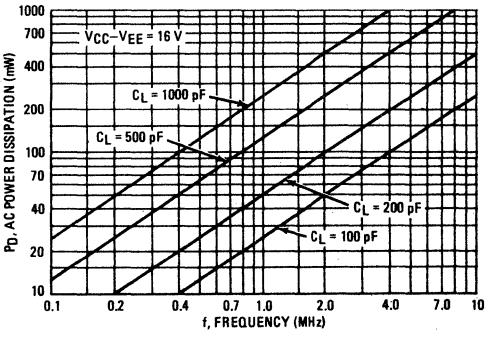


FIGURE 16 – AC POWER DISSIPATION versus FREQUENCY (SINGLE DRIVER)



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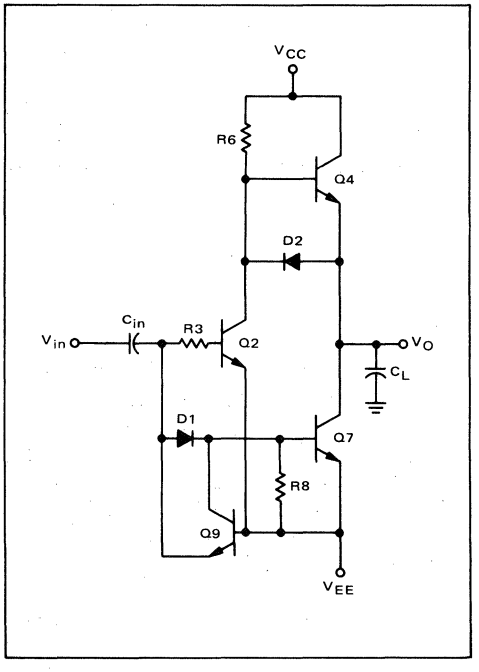
APPLICATIONS INFORMATION

OPERATION OF THE MMH0026

The simplified schematic diagram of MMH0026, shown in Figure 17, is useful in explaining the operation of the device. Figure 17 illustrates that as the input voltage level goes high, diode D1 provides an 0.7-volt "dead zone" thus ensuring that Q2 is turned "on" and Q4 is turned "off" before Q7 is turned "on". This prevents undesirable "current spiking" from the power supply, which would occur if Q7 and Q4 were allowed to be "on" simultaneously for an instant of time. Diode D2 prevents "zenering" of Q4 and provides an initial discharge path for the output capacitive load by way of Q2.

As the input voltage level goes low, the stored charge in Q2 is used advantageously to keep Q2 "on" and Q4 "off" until Q7 is "off". Again undesirable "current spiking" is prevented. Due to the external capacitor, the input side of C_{in} goes negative with respect to V_{EE} causing Q9 to conduct momentarily thus assuring rapid turn "off" of Q7.

FIGURE 17 – SIMPLIFIED SCHEMATIC DIAGRAM (Ref.: Figure 1)



The complete circuit, Figure 1, basically creates Darlington devices of transistors Q7, Q4 and Q2 in the simplified circuit of Figure 17. Note in Figure 1 that when the input goes negative with respect to V_{EE}, diodes D7 through D10 turn "on" assuring faster turn "off" of transistors Q1, Q2, Q6 and Q7. Resistor R6 insures that the output will charge to within one V_{BE} voltage drop of the V_{CC} supply.

SYSTEM CONSIDERATIONS

Overshoot:

In most system applications the output waveform of the MMH0026 will "overshoot" to some degree. However, "overshoot" can be eliminated or reduced by placing a damping resistor in series with the output. The amount of resistance required is given by: $R_S = 2\sqrt{L/C_L}$ where L is the inductance of the line and C_L is the load capacitance. In most cases a series of damping resistor in the range of 10-to-50 ohms will be sufficient. The damping resistor also affects the transition times of the outputs. The speed reduction is given by the formula:

$t_{THL} \approx t_{TLH} = 2.2\ R_S\ C_L$ (R_S is the damping resistor).

Crosstalk:

The MMH0026 is sensitive to crosstalk when the output voltage level is high ($V_O \approx V_{CC}$). With the output in the high voltage level state, Q3 and Q4 are essentially turned "off". Therefore, negative-going crosstalk will pull the output down until Q4 turns "on" sufficiently to pull the output back towards V_{CC}. This problem can be minimized by placing a "bleeding" resistor from the output to ground. The "bleeding" resistor should be of sufficient size so that Q4 conducts only a few milliamperes. Thus, when noise is coupled, Q4 is already "on" and the line is quickly clamped by Q4. Also note that in Figure 1 D6 clamps the output one diode-voltage drop above V_{CC} for positive-going crosstalk.

Power Supply Decoupling:

The decoupling of V_{CC} and V_{EE} is essential in most systems. Sufficient capacitive decoupling is required to supply the peak surge currents during switching. At least a 0.1-μF to 1.0-μF low inductive capacitor should be placed as close to each driver package as the layout will permit.

Input Driving:

For those applications requiring split power supplies ($V_{EE} < GND$), ac coupling, as illustrated in Figure 3, should be employed. Selection of the input capacitor size is determined by the desired output pulse width. Maximum performance is attained when the voltage at

APPLICATIONS INFORMATION (continued)

the input of the MMH0026 discharges to just above the device's threshold voltage (about 1.5 V). Figure 7 shows optimum values for C_{in} versus the desired output pulse width. The value for C_{in} may be roughly predicted by:

$$C_{in} = (2 \times 10^{-3}) (PW_O). \quad (1)$$

For an output pulse width of 500 ns, the optimum value for C_{in} is:

$$C_{in} = (2 \times 10^{-3}) (500 \times 10^{-9}) = 1000 \text{ pF}.$$

If single supply operation is required (V_{EE} = GND), then dc coupling as illustrated in Figure 4 can be employed. For maximum switching performance, a speed-up capacitor should be employed with dc coupling. Figures 13 and 14 show typical switching characteristics for various values of input resistance and capacitance.

POWER CONSIDERATIONS

Circuit performance and long-term circuit reliability are affected by die temperature. Normally, both are improved by keeping the integrated circuit junction temperatures low. Electrical power dissipated in the integrated circuit is the source of heat. This heat source increases the temperature of the die relative to some reference point, normally the ambient temperature. The temperature increase depends on the amount of power dissipated in the circuit and on the net thermal resistance between the heat source and the reference point. The basic formula for converting power dissipation into junction temperature is:

$$T_J = T_A + P_D (\theta_{JC} + \theta_{CA}) \quad (2)$$

or

$$T_J = T_A + P_D (\theta_{JA}) \quad (3)$$

where

T_J = junction temperature
T_A = ambient temperature
P_D = power dissipation
θ_{JC} = thermal resistance, junction to case
θ_{CA} = thermal resistance, case to ambient
θ_{JA} = thermal resistance, junction to ambient.

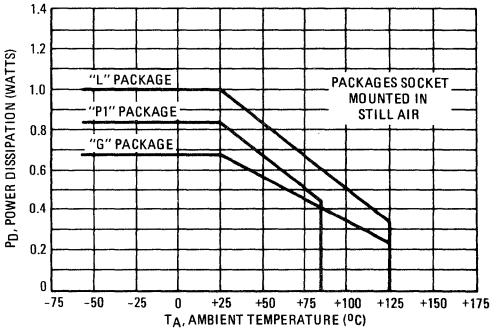
Power Dissipation for the MMH0026 MOS Clock Driver:

The power dissipation of the device (P_D) is dependent on the following system requirements: frequency of operation, capacitive loading, output voltage swing, and duty cycle. This power dissipation, when substituted into equation (3), should not yield a junction temperature, T_J, greater than T_J(max) at the maximum encountered ambient temperature. T_J(max) is specified for three integrated circuit packages in the maximum ratings section of this data sheet.

TABLE 1 – THERMAL CHARACTERISTICS OF "G", "L" AND "P1" PACKAGES

PACKAGE TYPE (Mounted in Socket)	θ_{JA} (°C/W) Still Air		θ_{JC} (°C/W) Still Air	
	MAX	TYP	MAX	TYP
"G" (Metal Package)	220	175	70	40
"L" (Ceramic Package)	150	100	50	27
"P1" (Plastic Package)	150	100	70	40

FIGURE 18 – MAXIMUM POWER DISSIPATION versus AMBIENT TEMPERATURE (As related to package)



With these maximum junction temperature values, the maximum permissible power dissipation at a given ambient temperature may be determined. This can be done with equations (2) or (3) and the maximum thermal resistance values given in Table 1 or alternately, by using the curves plotted in Figure 18. If, however, the power dissipation determined by a given system produces a calculated junction temperature in excess of the recommended maximum rating for a given package type, something must be done to reduce the junction temperature.

There are two methods of lowering the junction temperature without changing the system requirements. First, the ambient temperature may be reduced sufficiently to bring T_J to an acceptable value. Secondly, the θ_{CA} term can be reduced. Lowering the θ_{CA} term can be accomplished by increasing the surface area of the package with the addition of a heat sink or by blowing air across the package to promote improved heat dissipation.

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APPLICATIONS INFORMATION (continued)

The following examples illustrate the thermal considerations necessary to increase the power capability of the MMH0026.

Assume that the ceramic package is to be used at a maximum ambient temperature (T_A) of +70°C. From Table 1: θ_{JA}(max) = 150°C/watt, and from the maximum rating section of the data sheet: T_J(max) = +175°C. Substituting the above values into equation (3) yields a maximum allowable power dissipation of 0.7 watts. Note that this same value may be read from Figure 18. Also note that this power dissipation value is for the device mounted in a socket.

Next, the maximum power consumed for a given system application must be determined. The power dissipation of the MOS clock driver is conveniently divided into dc and ac components. The dc power dissipation is given by:

$$P_{dc} = (V_{CC} - V_{EE}) \times (I_{CCL}) \times (\text{Duty Cycle}) \qquad (4)$$

$$\text{where } I_{CCL} = 40\ \text{mA}\ (\frac{V_{CC} - V_{EE}}{20\ \text{V}}).$$

Note that Figure 15 is a plot of equation (4) for three values of (V_{CC}–V_{EE}). For this example, suppose that the MOS clock driver is to be operated with V_{CC} = +16 V and V_{EE} = GND and with a 50% duty cycle. From equation (4) or Figure 15, the dc power dissipation (per driver) may be found to be 256 mW. If both drivers within the package are used in an identical way, the total dc power is 512 mW. Since the maximum total allowable power dissipation is 700 mW, the maximum ac power that can be dissipated for this example becomes:

$$P_{ac} = 0.7 - 0.512 = 188\ \text{mW}$$

The ac power for each driver is given by:

$$P_{ac} = (V_{CC} - V_{EE})^2 \times f \times C_L \qquad (5)$$

where f = frequency of operation

C_L = load capacitance (including all strays and wiring).

Figure 16 gives the maximum ac power dissipation versus switching frequency for various capacitive loads with V_{CC} = 16 V and V_{EE} = GND. Under the above conditions, and with the aid of Figure 16, the safe operating area beneath Curve A of Figure 19 can be generated.

Since both drivers have a maximum ac power dissipation of 188 mW, the maximum ac power per driver becomes 94 mW. A horizontal line intersecting all the capacitance load lines at the 94 mW level of Figure 16 will yield the maximum frequency of operation for each of the capacitive loads at the specified power level. By using the previous formulas and constants, a new safe operating area can be generated for any output voltage swing and duty cycle desired.

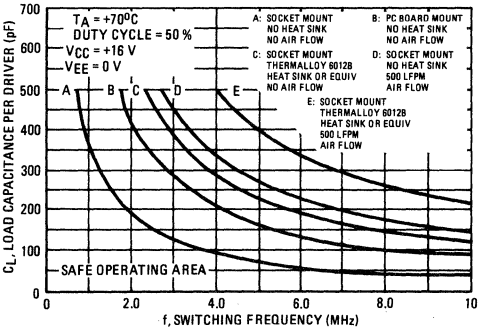
Note from Figure 19, that with highly capacitive loads, the maximum switching frequency is very low. The switching frequency can be increased by varying the following factors:

(a) decrease T_A
(b) decrease the duty cycle
(c) lower package thermal resistance θ_{JA}.

In most cases conditions (a) and (b) are fixed due to system requirements. This leaves only the thermal resistance θ_{JA} that can be varied.

Note from equation (2) that the thermal resistance is comprised of two parts. One is the junction-to-case thermal resistance (θ_{JC}) and the other is the case-to-ambient thermal resistance (θ_{CA}). Since the factor θ_{JC} is a function of the die size and type of bonding employed, it cannot be varied. However, the θ_{CA} term can be changed as previously discussed, see Page 7.

FIGURE 19 – LOAD CAPACITANCE versus FREQUENCY FOR "L" PACKAGE ONLY
(Both drivers used in identical way)



Heat Sink Considerations:

Heat sinks come in a wide variety of sizes and shapes that will accomodate almost any IC package made. Some of these heat sinks are illustrated in Figure 20. In the previous example, with the ceramic package, no heat sink and in a still air environment, θ_{JA}(max) was 150°C/W.

For the following example the Thermalloy 6012B type heat sink, or equivalent, is chosen. With this heat sink, the θ_{CA} for natural convection from Figure 21 is 44°C/W. From Table 1 θ_{JC}(max) = 50°C/W for the ceramic

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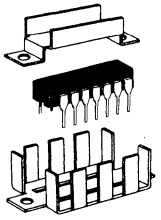
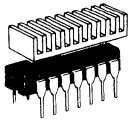
APPLICATIONS INFORMATION (continued)

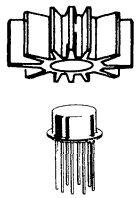
FIGURE 20 – THERMALLOY* HEAT SINKS



6007A



6012B



2230-5

*Manufactured by Thermalloy Co. of Texas.

package. Therefore, the new θ_{JA}(max) with the 6012B heat sink added becomes:

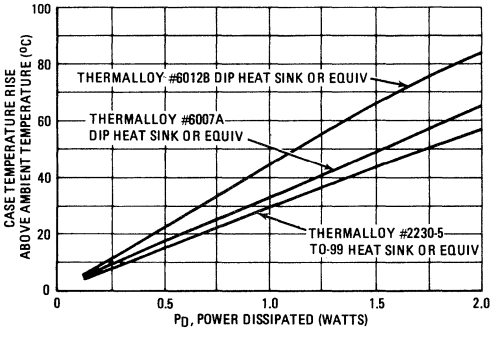
$$\theta_{JA}(max) = 50^{o}C/W + 44^{o}C/W = 94^{o}C/W.$$

Thus the addition of the heat sink has reduced θ_{JA}(max) from 150°C/W down to 94°C/W. With the heat sink, the maximum power dissipation by equation (3) at T_A = +70°C is:

$$P_D = \frac{175^{o}C - 70^{o}C}{94^{o}C/W} = 1.11 \text{ watts.}$$

This gives approximately a 58% increase in maximum power dissipation. The safe operating area under Curve C of Figure 19 can now be generated as before with the aid of Figure 16 and equation (5).

FIGURE 21 – CASE TEMPERATURE RISE ABOVE AMBIENT versus POWER DISSIPATED USING NATURAL CONVECTION



Forced Air Considerations:

As illustrated in Figure 22, forced air can be employed to reduce the θ_{JA} term. Note, however, that this curve is expressed in terms of typical θ_{JA} rather than maximum θ_{JA}. Maximum θ_{JA} can be determined in the following manner:

From Table 1 the following information is known:

(a) θ_{JA}(typ) = 100°C/W
(b) θ_{JC}(typ) = 27°C/W

Since:

$$\theta_{JA} = \theta_{JC} + \theta_{CA} \quad (6)$$

Then:

$$\theta_{CA} = \theta_{JA} - \theta_{JC} \quad (7)$$

Therefore, in still air

$$\theta_{CA}(typ) = 100^{o}C/W - 27^{o}C/W = 73^{o}C/W$$

From Curve 1 of Figure 22 at 500 LFPM and equation (7),

$$\theta_{CA}(typ) = 53^{o}C/W - 27^{o}C/W = 26^{o}C/W.$$

Thus θ_{CA}(typ) has changed from 73°C/W (still air) to 26°C/W (500 LFPM), which is a decrease in typical θ_{CA} by a ratio of 1:2.8. Since the typical value of θ_{CA} was reduced by a ratio of 1:2.8, θ_{CA}(max) of 100°C/W should also decrease by a ratio of 1:2.8.

This yields an θ_{CA}(max) at 500 LFPM of 36°C/W.

Therefore, from equation (6):

$$\theta_{JA}(max) = 50^{o}C/W + 36^{o}C/W = 86^{o}C/W.$$

Therefore the maximum allowable power dissipation at 500 LFPM and T_A = +70°C is from equation (3):

$$P_D = \frac{175^{o}C - 70^{o}C}{+86^{o}C/W} = 1.2 \text{ watts.}$$

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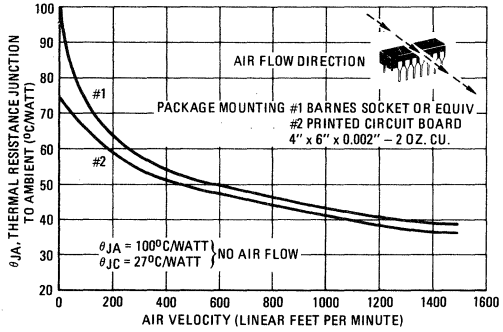
APPLICATIONS INFORMATION (continued)

FIGURE 22 – TYPICAL THERMAL RESISTANCE (θ_{JA}) OF "L" PACKAGE versus AIR VELOCITY



As with the previous examples, the dc power at 50% duty cycle is subtracted from the maximum allowable device dissipation (P_D) to obtain a maximum P_{ac}. The safe operating area under Curve D of Figure 19 can now be generated from Figure 16 and equation (5).

Heat Sink and Forced Air Combined:

Some heat sink manufacturers provide data and curves of θ_{CA} for still air and forced air such as illustrated in Figure 23. For example the 6012B heat sink has an θ_{CA} = 17°C/W at 500 LFPM as noted in Figure 23.

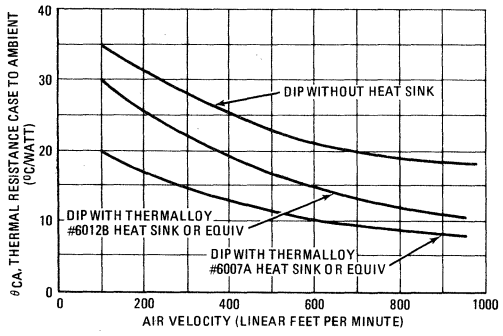
From equation (6):

$$\text{Max } \theta_{JA} = 50°C/W + 17°C/W = 67°C/W$$

From equation (3) at T_A = +70°C

$$P_D = \frac{175°C - 70°C}{67°C/W} \quad 1.57 \text{ watts.}$$

FIGURE 23 – THERMAL RESISTANCE θ_{CA} versus AIR VELOCITY



As before this yields a safe operating area under Curve E in Figure 19.

Note from Table 1 and Figure 22 that if the 14-pin ceramic package is mounted directly to the PC board (2 oz. cu. underneath), that typical θ_{JA} is considerably less than for socket mount with still air and no heat sink. The following procedure can be employed to determine a safe operating area for this condition.

Given data from Table 1:

$$\text{typical } \theta_{JA} = 100°C/W$$
$$\text{typical } \theta_{JC} = 27°C/W$$

From Curve 2 of Figure 22, θ_{JA}(typ) is 75°C/W for a PC mount and no air flow. Then the typical θ_{CA} is 75°C/W – 27°C/W = 48°C/W. From Table 1 the typical value of θ_{CA} for socket mount is 100°C/W – 27°C/W = 73°C/W. This shows that the PC board mount results in a decrease in typical θ_{CA} by a ratio of 1:1.5 below the typical value of θ_{CA} in a socket mount. Therefore, the maximum value of socket mount θ_{CA} of 100°C/W should also decrease by a ratio of 1:1.5 when the device is mounted in a PC board. The maximum θ_{CA} becomes:

$$\theta_{CA} = \frac{100°C/W}{1.5} = 66°C/W \text{ for PC board mount}$$

Therefore the maximum θ_{JA} for a PC mount is from equation (6).

$$\theta_{JA} = 50°C/W + 66°C/W = 116°C/W.$$

With maximum θ_{JA} known, the maximum power dissipation can be found and the safe operating area determined as before. See Curve B in Figure 19.

CONCLUSION

In most cases, heat sink manufacturer's publish only θ_{CA} socket mount data. Although θ_{CA} data for PC mounting is generally not available, this should present no problem. Note in Figure 22 that an air flow greater than 250 LFPM yields a socket mount θ_{JA} approximately 6% greater than for a PC mount. Therefore, the socket mount data can be used for a PC mount with a slightly greater safety factor. Also it should be noted that thermal resistance measurements can vary widely. These measurement variations are due to the dependency of θ_{CA} on the type environment and measurement techniques employed. For example, θ_{CA} would be greater for an integrated circuit mounted on a PC board with little or no ground plane versus one with a substantial ground plane. Therefore, if the maximum calculated junction temperature is on the border line of being too high for a given system application, then thermal resistance measurements should be done on the system to be absolutely certain that the maximum junction temperature is not exceeded.

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1 GENERAL INFORMATION

2 RANDOM ACCESS MEMORIES (RAM)

3 READ ONLY MEMORIES (ROM)

4 M6800 SYSTEM MEMORIES

5 APPLICATION NOTES

6 RELIABILITY INFORMATION

7 MEMORY INTERFACE