Logic: Standard, Special and Programmable

In Brief . . .

This selector guide is a quick reference to Motorola's vast offering of standard logic integrated circuits. In TTL, popular due to its ease of use, low cost, medium–to–high speed operation and good output drive capability, Motorola offers both LS and FAST. Motorola's CMOS portfolio includes MC14000B standard CMOS series devices, High–Speed CMOS consisting of a full line of products that are pinout–compatible with many LSTTL and MC14000B standard CMOS logic devices which offers designers a solution to the long–standing combined barrier — high speed and low power. Motorola's Emitter Coupled Logic (MECL) is a non–saturated form of digital logic which eliminates transistor storage time permitting very high speed operation. Motorola offers five versions of MECL: MECL 10K, MECL 10H, MECL III, and the recently introduced families ECLinPS (ECL in picoseconds) and ECLinPS Lite. Also included are timing solution products such as clock drivers, clock generators and programmable delay chips, high performance and communications products such as VCO's, prescalers, and synthesizers, and a wide variety of translators, low–voltage bus interface and serial data transmission devices. Field programmable logic and in particular, field programmable arrays, have become the solution of choice for logic design implementation in applications where time to market is a critical product development factor. In addition, reconfigurable arrays have been used to enhance Customer product flexibility in ways that no other technology can match.

INTRODUCTION TO MOTOROLA PROGRAMMABLE ARRAYS AND THE MPA DESIGN SYSTEM

Field programmable logic and in particular, field programmable arrays, have become the solution of choice for logic design implementation in applications where time to market is a critical product development factor. In addition, reconfigurable arrays have been used to enhance Customer product flexibility in ways that no other technology can match.

Programmable logic not only vastly reduces the time necessary to implement a static design, but significant product feature benefits can be realized when hardware can be dynamically altered as easily as software.

The reconfigurable Motorola Programmable Array (MPA) and MPA design system maximize application flexibility and minimize time to market by delivering a gate level, push button, programmable logic solution.

Design Capture

Logic system designers have two basic options when selecting a method for capturing their designs. For smaller or very regular designs, schematic capture continues to be a popular design entry vehicle. With the increasing size and complexity of today's designs coupled with decreasing design cycle time requirements, many designers are turning to Hardware Description Languages (HDLs).

The MPA family was designed from the outset to be well suited to both methodologies. The output of logic synthesis compilers maps effortlessly and efficiently onto the MPA architecture. Unlike other FPGA offerings, the MPA poses no significant architectural limitations for which the designer might otherwise have to adjust his schematic design techniques for.

Push Button Design Implementation

The MPA design system minimizes training investment and automatically generates design implementations which meet timing constraints.

The gate level logic and abundant hierarchical routing resources of the MPA device present a rich implementation media for design implementation. MPA design tools understand and optimally utilize the MPA device resources so there are no elaborate rules to learn or design modifications required to begin design capture. Staying focused on end product design rather than implementation tools or device architecture gets the design done faster and, unlike other programmable solutions, without programmable logic device specificity to impede future design migration efforts. The combination of automatic tools and gate level architecture is ideal for traditional schematic driven or high level language based design capture methods. In fact, logic synthesis tools were originally designed for and produce the most efficient results for targeting gate level devices.

A design is analyzed, optimized, transformed into MPA cells, partitioned, placed and routed based on timing constraints for all paths in the design – automatically. A netlist from one of the popular design capture systems or an existing XNF or LPM netlist is imported into the MPA design system. The logic is mapped to a series of MPA cells and the entire resulting netlist is optimized and checked. Based on a simple clock specification, the MPA design system generates timing constraints for all paths in the design. During automatic partitioning, placement and routing path slack time is constantly redistributed insuring only the resources required to meet timing requirements are consumed. Because MPA tools implement the design according to constraints, tool induced design iterations are virtually eliminated. Completed layouts can be transformed into device configurations, as well as annotated simulation netlists. A layout browser is also available.

The MPA design system also includes complete on–line, hypermedia, help covers the device, the design system and the integration kits. Integration kits for Viewlogic, Exemplar, VHDL (1076 and SDF), Verilog (OVI and SDF) and OrCAD are included (contact your vendor for additional kits).All these features add up to a powerful yet extremely easy to use design implementation engine for the MPA product family.

Design Importation

Designs can be captured using schematics, a high level language, or a combination of these entry methods using commercially available design capture and logic synthesis software and the appropriate interface kit. Alternatively, existing designs can be retargeted from other programmable logic devices to the MPA device using commercial logic synthesis tools or the powerful retargetting capabilities provided with MPA design system.

Design importation begins with a netlist and an optional clock specification file. The clock specification file provides a mechanism for the user or design capture tools to document system level timing requirements. In addition, a rich set of attributes can be attached to specific components or nets within the design to specify timing and design pinout constraints.

A retargetting rules file is read and the input netlist is transformed into a series of MPA cells and associated interconnections. Rules files provide a mechanism to perform attribute mapping, cell mapping and macro expansion. By creating custom rule files, the user can extend the importation process from arbitrary sources. The MPA design system comes with rules for it's native library/EDIF. The resulting netlist is optimized to clip unused logic and remove redundant logic. For example: each MPA cell has programmable input inversion capability. All Inverters or non–inverting buffers can be removed from the netlist and replaced with signal sense information attached to each input.

A series of design rule checks are performed to insure design integrity before the layout process begins.

Constraint Generation

Timing constraints, the optimized MPA netlist and static timing analysis is used to generate path slack constraints for all paths in the design. Each unique signal pathway between a register output and a register input throughout the design are enumerated. The total logic and estimated or real wire delays along the path are summed. The time between the active upstream register clock edge and the next active downstream clock edge minus the downstream register setup time is subtracted from the total path delay. This difference is called path slack. If any path in the design has a negative slack value, the implementation will not function at the required clock rate(s).

Path constraints are utilized throughout the layout process to insure that a design implementation which meets timing constraints is automatically generated. If no clock or timing specifications are provided, the MPA design system uses the fastest possible clock based on very small net delay estimates to generate the path constraints. This usually results in the best possible implementation, but may take longer than the time required to generate a satisfactory rather than best possible result.

Contrast this to other programmable logic design tools which only provide manual net constraint annotation or net criticality assignment. In these cases significant effort is necessary to generate constraints and many costly iterations are required to tune these constraints for a given design. If any changes are made to the design, another costly round of iterations is required.

Autolayout

The autolayout process makes use of the hierarchical organization of the MPA device to minimize run time and deliver implementations that meet timing requirements. Designs which have diverse timing requirements are ideally implemented because path slack estimates are refined throughout the autolayout process insuring only the resources required to meet timing requirements are consumed.

The process begins by flattening the design and partitioning it into small component groups of approximately the same size called clusters. A cluster boundary delay estimation is applied to pull the most tightly constrained paths into a minimum number of clusters. The clusters are then assigned to zones talking into account zonal boundary delay cost and relative zone placement delay costs. Other costs like total number of port connections per zone and are also considered. As assignment proceeds, cluster and zone boundary delay costs are added to each path and slack is recomputed.

Next global placement and routing is done. Global routes begin and end on either I/O cells or port cells. Intrazone placement and routing is deferred to a later phase. During global routing all the port cell and I/O cell locations are fixed and the connections between them established. High fanout nets are constructed in a highly regular manner to insure efficient resource utilization. As in partitioning, slack estimates are refined throughout global routing.

Finally the intrazonal placement and routing is done. Cells assigned to a particular zone are placed and routed to other zone cells or zone port cells. Port cells and core cells are constructed to allow port swapping. Core cells can be routed through if necessary. Allowing core cells to act as routing cells allows dynamic adjustment of routing resources within the zone. Dynamic resource adjustment is a powerful design specific adaptation mechanism.

This process produces a layout from which device configurations, delay back annotations, and chipviews can be generated.

Incremental Design Support

When specification changes necessitate design iterations, simply push the button again. Constraints are automatically recalculated and autolayout only reworks those portions of the design which have changed. Full incremental design support means simple design changes to facilitate design verification can be made quickly and easily.

Delay Back Annotation

Designs can be verified through numerous methods. One particularly useful method is the annotation of device and implementation specific delays back into the original simulation environment to improve system or device level simulation accuracy. A MPA device layout can be transformed into an appropriately formatted delay annotation file or annotated netlist quickly and easily. The annotated delay information represents the worst case delays for a given device speed grade.

Chipview

While the MPA design system provides a rich set of reports describing the implementation of a design, a graphical view of the implementation can be indispensable for reviewing overall layout quality. Chipview provides a graphical view of a completed layout. Chipview can be useful during initial design iterations to visually verify I/O pin placements before commencing PCB layout, for example.

Configuration

A layout can be transformed into a device configuration which, when loaded into the appropriate MPA device, produces a physical design realization. Many formatting options are available. The MPA download pod can be used to emulate a serial PROM. Using the pod, device configuration files can be downloaded to a device directly from the PC or workstation development environment.

Integration Kits

The MPA design system can be used with a large number of commercial electronic design automation software. For each supported vendor, an integration kit is provided which facilitates MPA design within that vendors' environment. Many of these kits are available from Motorola and included at no charge on the MPA design system CDROM. Other kits can be acquired directly from the vendor. Refer to the MPA Design System Product List for more information.

Low Cost, Easy Access

MPA Design systems are easy to use, competitively priced and widely available. Copies of MPA design system software supporting up to 8000 gates can be downloaded from the World Wide Web (WWW) at URL:

http://sps.motorola.com/fpga

Complete kits including download pod, evaluation board, MPA device, CDROM and documentation can be ordered from your local authorized Motorola distributor or Motorola sales representative.

Fast, Efficient Design Implentation With Minimal Investment.

That's MPA!

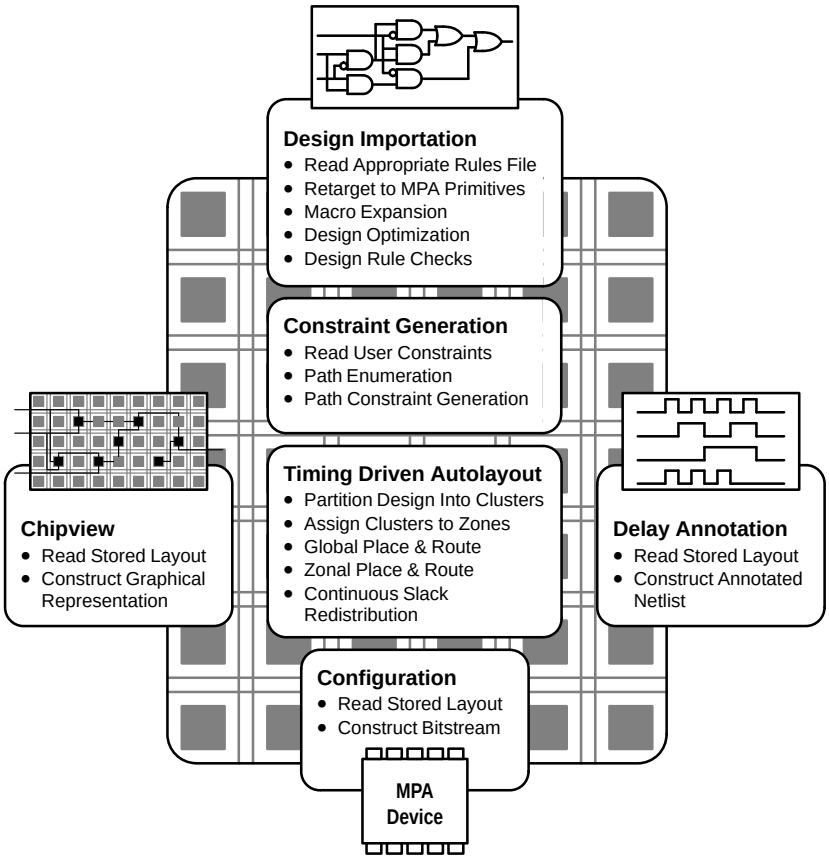
Motorola Programmable Array Design System

DESIGN SYSTEM

The Motorola Programmable Array (MPA) design system is a bridge between a design capture environment and Motorola field programmable arrays. The MPA design system automatically transforms designs into device configurations to realize a design, when loaded into an MPA device. A design is automatically analyzed, optimized, transformed into MPA cells, partitioned, placed and routed based on timing constraints for every path in the design. MPA design tools understand and optimally utilize the MPA device architecture; this eliminates the need to learn a new set of rules and makes these tools ideally suited for use with logic synthesis. Full incremental design support reduces design implementation time and powerful library retargeting capabilities allow you to reuse designs which may have been implemented on less capable devices. The MPA design system operates on existing hardware platforms and supports design capture and simulation tools from more than 10 vendors. All these features plus on–line, hypermedia, help make the MPA design system a powerful, yet extremely easy to use, design implementation engine.

Features

- Push Button Implementation
- Optimal Use of MPA Device Resources
- Optimal Results with Gate Level Design Input
- Library of Common MSI Functions
- Design Flow Manager
- Design Retargeter
- Timing Driven with Integrated Static Timing Analysis
- Layout Delay extraction for post layout simulation
- Layout viewer
- Incremental design support
- On–line, hypermedia, documentation
- Supports all popular design capture and simulation tools
- Lowest cost FPGA development systems.
- Instant access; Downloading via the internet (WWW, ftp).
- Supports multiple speed grades



MPA1000 Programmable Arrays

MPA1016
MPA1036
MPA1064
MPA1100

PROGRAMMABLE ARRAY
3,500 to 22,000 GATES

Motorola Programmable Array (MPA) products are a high density, high performance, low cost, solution for your reconfigurable logic needs. When used with our automatic high performance design tools, MPA delivers custom logic solutions in minutes rather than weeks. And the low cost keeps those solutions competitive throughout the product lifecycle.

The MPA architecture has solved the historical problems associated with fine grain devices without sacrificing re–programmability, reliability, or cost. MPA1000 devices are reprogrammable SRAM based products manufactured on a standard 0.43µ Leff CMOS process with logic capacities from 3,500 to more than 22,000 equivalent FPGA gates. MPA Logic resources hold a single gate or storage element providing a highly efficient, adaptable, design implementation medium. Gate level logic resources, abundant hierarchical interconnection resources and automatic, timing driven, tools work together to quickly provide design implementations that meet timing constraints without sacrificing device utilization.

Staying focused on end product design rather than implementation tools or device architecture gets the design done faster and, unlike other programmable solutions, without programmable logic device specificity to impede future design migration efforts. The combination of automatic tools and gate level architecture is ideal for traditional schematic driven or high level language based design methodologies. In fact, logic synthesis tools were originally designed for and produce the most efficient results when targeting gate level devices.

High MPA1000 register count and controlled clock skew is ideal for designs employing pipelining techniques such as communications. The unique set of MPA1000 I/O programming options make these devices suitable for industrial and computer interfacing circuits.

- Multiple I/O from 80–200 I/O Pins
- Programmable 3V/5V I/O at Any Site
- Multiple Packaging Options
- Fine Grain Structure Is Optimized for Logic Synthesis
- Programmable Output Drive, 4/6mA @ 5.0V and 3.3V
- High Register Count, with 560–2,900 Flip–Flops
- IEEE 1149.1 JTAG Boundary Scan
- Eight Low–Skew (<1ns) Clocks

MPA1000 Family Members

FPGA Gates*	Part No.	Logic Cells	Internal Flip–Flops	I/O Cell Flip–Flops	Avail I/O Pins	Packages	Availability
3500	MPA1016FN MPA1016DD	1600	400	122 160	61 80	84 PLCC 128 PQFP	NOW NOW
8000	MPA1036FN MPA1036DD MPA1036DH MPA1036HI	3600	900	122 160 240 240	61 80 120 120	84 PLCC 128 PQFP 160 PQFP 181 PGA	NOW NOW NOW NOW
14200	MPA1064DH MPA1064DK MPA1064KE MPA1064BG	6400	1600	240 320 320 320	120 160 160 160	160 PQFP 208 PQFP 224 PGA 256 PBGA	NOW NOW NOW 3Q97
22000	MPA1100DK MPA1100HV MPA1100BG	10000	2500	320 400 400	160 200 200	208 PQFP 299 PGA 256 PBGA	NOW NOW 3Q97

* Equivalent to Industry Standards, as supplied by most manufacturers.

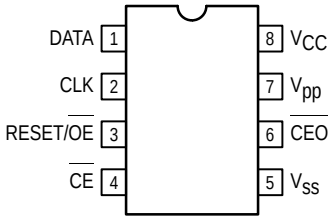
MPA17000 Serial EPROMs

The MPA17128, MPA1765 serial OTP EPROMs provide a compact, low pin count, non–volatile configuration store for MPA1000 devices.

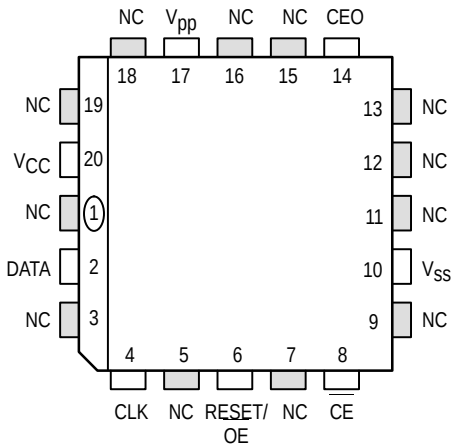
MPA17000 devices can be cascaded for increased memory capacity when needed. They are available in the standard 8–pin plastic DIP (N suffix), 8–pin SOIC (D suffix) and 20–pin PLCC (FN suffix) packages.

- Configuration EPROM for MPA1000 Devices
- Voltage Range — 4.5 to 6.0V
- Maximum Read Current of 10mA
- Standby Current of 10μA, Typical
- Industry Standard Synchronous Serial Interface
- Full Static Operation
- 10MHz Maximum Clock Rate at 5.0V
- Programmable Polarity on Hardware Reset
- Programs With Industry Standard Programmers
- Electrostatic Discharge Protection > 2000 Volts
- 8–Pin PDIP and SOIC; 20–Pin PLCC Packages
- Commercial (0 to +70°C) and Industrial (–40 to +85°C)

8–Lead Pinouts
(Top View)

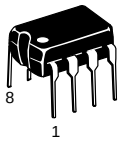


20–Lead Pinout
(Top View)



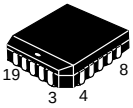
MPA17128
MPA1765

128K, 64K SERIAL EPROM



P SUFFIX
PLASTIC PACKAGE
CASE 626–05

D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751–05



FN SUFFIX
PLCC PACKAGE
CASE 775–02

PIN NAMES

Pins	Function
DATA	Data I/O
CLK	Clock
RESET/OE	Reset Input and Output Enable
CE	Chip Enable Input
VSS	Ground
CEO	Chip Enable Output
VPP	Programming Voltage Supply
VCC	+4.5 to 6.0V Power Supply
NC	Not Connected

Advance Information

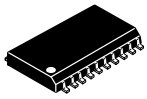
MPA17000 Serial EEPROM

MPA17C256

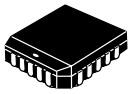
The MPA17C256 is an easy to use and cost effective serial configuration memory ideally suited for use with today's popular SRAM based FPGAs. The MPA17C256 is available in 8–pin PDIP and 20–pin SOIC and PLCC packages, adhering to industry standard pinouts. The device interfaces downstream FPGA(s) with a very simple enable, clock and data interface. The MPA17C256 is reprogrammable with no need for a higher programming "super voltage"; it may even be reprogrammed on board. The MPA17C256 also has user programmable RESET/OE polarity.

- EE Programmable 262,144 x 1 bit Serial Memories Designed to Store Configuration Programs for FPGAs
- Simple Interface to SRAM FPGAs
- Cascadable to Support Additional Configurations or Future Higher Density FPGAs
- Low Power CMOS EEPROM Process
- Programmable Reset Polarity
- Available in Space Efficient 8–Pin PDIP, 20–Pin SOIC and 20–Pin PLCC Packages
- In–System Programmable via 2–Wire Bus

P SUFFIX
8–LEAD PLASTIC PACKAGE
CASE 626–05



DW SUFFIX
20–LEAD PLASTIC SOIC WIDE PACKAGE
CASE 751D–04



FN SUFFIX
20–LEAD PLCC PACKAGE
CASE 775–02

Controlling the MPA17C256 Serial EEPROM

Most connections between the FPGA device and the Serial EEPROM are simple and self–explanatory:

- The DATA output of the MPA17C256 drives DIN of the FPGA devices
- The master FPGA DCLK output drives the CLK input of the MPA17C256
- The CEO output of the first MPA17C256 drives the CE input of the next MPA17C256 in a cascade chain of EEPROMs.
- SER_EN must be connected to V_{CC}
- CE enables the chip and is required to enable the DATA output pin
- RESET/OE is chip reset and is part of the DATA output enable structure

PIN NAMES

Pins	Function
DATA	Data I/O
CLK	Clock
RESET/OE	Reset Input and Output Enable
CE	Chip Enable Input
V_{SS}	Ground
CEO	Chip Enable Output
SER_EN	Programming Enable
V_{CC}	+4.5 to 6.0V Power Supply
NC	Not Connected

This document contains information on a new product. Specifications and information herein are subject to change without notice.

Selection by Function

In order to better serve our customers, we have made some modifications to the Selection by Function portion of the Logic Selector Guide. For easy selection of Logic's newer, more complex functions, as well as standard family functions, refer to the subject index below. Within the Selection by Function tables on the next 27 pages, you will find functions sorted by these broad subjects, and then broken down alphabetically into more precise functions.

Logic Functions

Selection by Function

Description	Tech.	Device(s)		Pins	DIP	SM
AMPLIFIER						
Fiber Optic Post Amplifier	ECL	MC10SX1125	–	16		D
ARITHMETIC OPERATORS						
4–Bit Arithmetic Logic Unit	TTL	MC74F181	–	24	N	DW
	TTL	MC74F381	–	20	N	DW
	TTL	MC74F382	–	20	N	DW
4–Bit Arithmetic Logic Unit/Function Generator	ECL	MC10H181	–	24	P,L, PW, LW	FN
	ECL	MC10181	–	24	P,L	
4–Bit Binary Full Adder With Fast Carry	TTL	MC74F283	–	16	N	D
	TTL	SN54LS83A	SN74LS83A	14	N,J	D
	TTL	SN54LS283	SN74LS283	16	N,J	D
4–Bit Full Adder	CMOS	MC14008B	–	16	P,L	D
9's Complementer	CMOS	MC14561B	–	14	P	D
BCD Rate Multiplier	CMOS	MC14527B	–	16	P	DW
Carry Lookahead Generator	TTL	MC74F182	–	16	N	D
Dual 2–Bit Adder/Subtractor	ECL	MC10H180	–	16	P,L	FN
	ECL	MC10180	–	16	P,L	
Look Ahead Carry Block	ECL	MC10H179	–	16	P,L	FN
NBCD Adder	CMOS	MC14560B	–	16	P,L	D
Triple Serial Adder (Negative Logic)	CMOS	MC14038B	–	16	L	
BOUNCE ELIMINATOR						
Hex Contact Bounce Eliminator	CMOS	MC14490	–	16	P,L	DW
BUFFERS						
1:2 Differential Fanout Buffer	ECL	MC100LVEL11	–	8		D
2:8 Differential Fanout Buffer	ECL	MC100LVE310	MC100E310	28		FN
Dual 1:3 Fanout Buffer	ECL	MC100LVEL13	MC100EL13	20		DW
Expandable Buffer	DTL	MC832	–	14	P,L	
Low Voltage Dual 1:4, 1:5 Differential Fanout Buffer, ECL/PECL Compatible	ECL	MC100LVE210	MC100E210	28		FN
BUFFERS, 3–STATE						
Low–Voltage CMOS 16–Bit Buffer, 3–State, Inverting With 5V Tolerant Inputs and Outputs	CMOS	MC74LCX16240A	–	20		DW,M, DT
Low–Voltage CMOS 16–Bit Buffer, 3–State, Non–Inverting With 5V Tolerant Inputs and Outputs	CMOS	MC74LCX16244	–	20		DW,M, DT
Low–Voltage CMOS Octal Buffer, 3–State, Non–Inverting With 5V Tolerant Inputs and Outputs	CMOS	MC74LCX244	–	20		DW,M, DT
Low–Voltage CMOS Octal Buffer, 3–State, Inverting With 5V Tolerant Inputs and Outputs	CMOS	MC74LCX240	–	20		DW,M, DT
Low–Voltage CMOS Octal Buffer Flow Through Pinout, 3–State, Non–Inverting With 5V Tolerant Inputs and Outputs	CMOS	MC74LCX541	–	20		DW,M, DT
Low–Voltage CMOS Octal Buffer Flow Through Pinout, 3–State, Inverting With 5V Tolerant Inputs and Outputs	CMOS	MC74LCX540	–	20		DW,M, DT
Low–Voltage CMOS Quad Buffer, 3–State, Inverting With 5V Tolerant Inputs and Outputs	CMOS	MC74LCX125	–	20		DW,M, DT
Low–Voltage Quiet CMOS Octal Buffer	CMOS	MC74LVQ541	–	20		D,M, SD,DT
Low–Voltage Quiet CMOS Octal Buffer, 3–State, Non–Inverting	CMOS	MC74LVQ244	–	20		DW,M, SD,DT

Selection by Function

Description	Tech.	Device(s)		Pins	DIP	SM
BUFFERS, 3–STATE						
Low–Voltage Quiet CMOS Octal Buffer, 3–State, Inverting	CMOS	MC74LVQ240	–	20		DW,M, SD,DT
Low–Voltage Quiet CMOS Quad Buffer, 3–State, Non–Inverting	CMOS	MC74LVQ125	–	14		D,M, SD,DT
BUS INTERFACE						
10–Bit Buffer/Line Driver (Inverting), With 3–State Outputs	TTL	MC74F828	–	24	N	DW
10–Bit Buffer/Line Driver (Non–Inverting), With 3–State Outputs	TTL	MC74F827	–	24	N	DW
3–Bit Registered Bus Transceiver, 25Ω Cutoff Outputs	ECL	MC10E336	MC100E336	28		FN
3–Bit Scannable Registered Bus Transceiver	ECL	MC10E337	MC100E337	28		FN
32–Bit to 32/16/8–Bit Dynamic READ/WRITE Bus Sizer	CMOS	MC68150*33	–	68		FN
	CMOS	MC68150*40	–	68		FN
9–Bit Bus Interface, NINV, 3 State Outputs	TTL	MC74F823	–	24	N	DW
Dual Bus Driver/Receiver With 4–to–1 Output Multiplexer (25Ω)	ECL	MC10H332	–	20	P,L	FN
Hex 3–State Inverting Buffer With Common Enables	CMOS	MC54HC366	MC74HC366	16	N,J	
Hex 3–State Inverting Buffer With Separate 2–Bit and 4–Bit Sections	CMOS	MC74HC368	–	16	N	
Hex 3–State Non–Inverting Buffer With Common Enables	CMOS	MC54HC365	MC74HC365	16	N,J	DT
Hex 3–State Non–Inverting Buffer With Separate 2–Bit and 4–Bit Sections	CMOS	MC54HC367	MC74HC367	16	N,J	
Hex Buffer 4/2–Bit/Inverting With 3–State Outputs	TTL	SN54LS368A	SN74LS368A	16	N,J	D
Hex Buffer 4/2–Bit/Non–Inverting With 3–State Outputs	TTL	SN54LS367A	SN74LS367A	16	N,J	D
Hex Buffer Driver, 4+2–Bit, Inverting, With 3–State Outputs	TTL	MC74F368	–	16	N	D
Hex Buffer Gated Enable Inverting With 3–State Outputs	TTL	SN54LS366A	SN74LS366A	16	N,J	D
Hex Buffer Gated Enable Non–Inverting With 3–State Outputs	TTL	SN54LS365A	SN74LS365A	16	N,J	D
Hex Buffer/Driver Gated Enable Inverting, With 3–State Outputs	TTL	MC74F366	–	16	N	D
Hex Buffer/Driver Gated Enable Non–Inverting, With 3–State Outputs	TTL	MC74F365	–	16	N	D
Hex Buffer/Driver, 4+2–Bit, Non–Inverting, With 3–State Outputs	TTL	MC74F367	–	16	N	D
Hex With 3–State Outputs Buffer (Non–Inverting)	CMOS	MC14503B	–	16	P,L	D
Octal 3–State Non–Inverting Bus Transceiver With LSTTL Compatible Inputs	CMOS	MC54HCT245A	MC74HCT245A	20	N,J	DW, SD,DT
Octal Bidirectional Transceiver With 3–State Inputs/Outputs	CMOS	MC74AC245	–	20	N	DW
	CMOS	MC74ACT245	–	20	N	DW
Octal Bidirectional Transceiver With 3–State Outputs	CMOS	MC74AC620	–	20	N	DW
	CMOS	MC74ACT620	–	20	N	DW
	CMOS	MC74AC623	–	20	N	DW
	CMOS	MC74ACT623	–	20	N	DW
	CMOS	MC74AC640	–	20	N	DW
	CMOS	MC74ACT640	–	20	N	DW
	CMOS	MC74AC643	–	20	N	DW
	CMOS	MC74ACT643	–	20	N	DW
	TTL	MC74F245	–	20	N	DW
Octal Bidirectional Transceiver With 8–Bit Parity Generator Checker, With 3–State Outputs	TTL	MC74F657A	–	24	N	DW
	TTL	MC74F657B	–	24	N	DW
Octal Bidirectional Transceiver, With 3–State Inputs/Outputs	TTL	MC74F1245	–	20	N	DW
Octal Buffer With 3–State Outputs (81LS95)	TTL	SN54LS795	SN74LS795	20	N,J	DW
(81LS96)	TTL	SN54LS796	SN74LS796	20	N,J	DW
(81LS97)	TTL	SN54LS797	SN74LS797	20	N,J	DW
(81LS98)	TTL	SN54LS798	SN74LS798	20	N,J	DW

Selection by Function

Description	Tech.	Device(s)		Pins	DIP	SM
BUS INTERFACE						
Octal Buffer/Line Driver With 3–State Outputs	TTL	SN54LS244	SN74LS244	20	N,J	DW
	TTL	MC74F240	–	20	N	DW
	TTL	MC74F241	–	20	N	DW
	TTL	MC74F244	–	20	N	DW
	TTL	SN54LS240	SN74LS240	20	N,J	DW
	TTL	SN54LS241	SN74LS241	20	N,J	DW
	TTL	SN54LS540	SN74LS540	20	N,J	DW
	TTL	SN54LS541	SN74LS541	20	N,J	DW
	CMOS	MC74AC241	–	20	N	DW
	CMOS	MC74AC244	–	20	N	DW
	CMOS	MC74ACT244	–	20	N	DW
	CMOS	MC74AC540	–	20	N	DW
	CMOS	MC74ACT540	–	20	N	DW
	CMOS	MC74AC541	–	20	N	DW
	CMOS	MC74ACT541	–	20	N	DW
	CMOS	MC74AC240	–	20	N	DW
	CMOS	MC74ACT240	–	20	N	DW
	CMOS	MC74ACT241	–	20	N	DW
Octal Bus Transceiver	TTL	SN54LS245	SN74LS245	20	N,J	DW
	TTL	SN54LS623	SN74LS623	20	N,J	DW
Octal Bus Transceiver, With 3–State Outputs	TTL	MC74F623	–	20	N	DW
Octal Bus Transceiver/Inverting With 3–State Outputs	TTL	SN54LS640	SN74LS640	20	N,J	DW
	TTL	MC74F620	–	20	N	DW
	TTL	MC74F640	–	20	N	DW
Octal Bus Transceiver/Non–Inverting With 3–State Outputs	TTL	SN54LS645	SN74LS645	20	N,J	DW
Octal Bus Transceiver/Register With 3–State Outputs Non–Inverting	CMOS	MC74AC652	–	24	N	DW
	CMOS	MC74ACT652	–	24	N	DW
Octal Registered Transceiver Inverting, With 3–State Outputs	TTL	MC74F544	–	24	N	DW
Octal Transceiver/Register With 3–State Outputs Non–Inverting	CMOS	MC74AC646	–	24	N	DW
	CMOS	MC74ACT646	–	24	N	DW
Octal Transceiver/Register With 3–State Outputs Inverting	CMOS	MC74AC648	–	24	N	DW
	CMOS	MC74ACT648	–	24	N	DW
Octal Transceiver/Register, With 3–State Outputs	TTL	MC74F646	–	24	N	DW
Octal With 3–State Non–Inverting Buffer/Line Driver/Line Receiver	CMOS	MC54HC241A	MC74HC241A	20	N,J	DW
Octal With 3–State Non–Inverting Buffer/Line Driver/Line Receiver With LSTTL Compatible Inputs	CMOS	MC54HCT241A	MC74HCT241A	20	N,J	DW
	CMOS	MC54HCT244A	MC74HCT244A	20	N,J	DW, SD,DT
Octal With 3–State Outputs Inverting Buffer/Line Driver/Line Receiver	CMOS	MC54HC240A	MC74HC240A	20	N,J	DW, DT
	CMOS	MC54HC540A	MC74HC540A	20	N,J	DW
Octal With 3–State Outputs Inverting Buffer/Line Driver/Line Receiver With LSTTL Compatible Inputs	CMOS	MC74HCT240A	–	20	N	DW, SD,DT
Octal With 3–State Outputs Inverting Bus Transceiver	CMOS	MC54HC640A	MC74HC640A	20	N,J	DW
Octal With 3–State Outputs Non–Inverting Buffer/Line Driver/Line Receiver	CMOS	MC54HC541A	MC74HC541A	20	N,J	DW
	CMOS	MC74VHC541	–	20		DW, DT,M
Octal With 3–State Outputs Non–Inverting Buffer/Line Driver/Line Receiver With LSTTL Compatible Inputs	CMOS	MC74HCT541A	–	20	N	DW

Selection by Function

Description	Tech.	Device(s)		Pins	DIP	SM
BUS INTERFACE						
Octal With 3–State Outputs Non–Inverting Buffer/Line Driver/Line Receiver	CMOS	MC54HC244A	MC74HC244A	20	N,J	DW, SD,DT
	CMOS	MC74VHC244	–	20		DW, DT,M
Octal With 3–State Outputs Non–Inverting Bus Transceiver	CMOS	MC54HC245A	MC74HC245A	20	N,J	DW
	CMOS	MC74VHC245	–	20		DW DT,M
Octal With 3–State Outputs Non–Inverting Bus Transceiver & D Flip–Flop	CMOS	MC54HC646	MC74HC646	24	N,J	DW
Quad Buffers With 3–State Outputs	TTL	SN54LS125A	SN74LS125A	14	N,J	D
Quad 3–State Non–Inverting Buffers	CMOS	MC74HC125A	–	14	N	D,DT
	CMOS	MC74VHC125	–	14		D, DT,M
	CMOS	MC74HC126A	–	14	N	D,DT
Quad Buffer With 3–State Outputs	CMOS	MC74AC125	–	14	N	D
	CMOS	MC74ACT125	–	14	N	D
	CMOS	MC74AC126	–	14	N	D
	CMOS	MC74ACT126	–	14	N	D
	TTL	MC74F125	–	14	N	D
	TTL	MC74F126	–	14	N	D
	TTL	SN54LS126A	SN74LS126A	14	N,J	D
Quad Bus Driver	ECL	MC10192	–	16	P,L	FN
Quad Bus Driver/Receiver With 2–to–1 Output Multiplexer (25Ω)	ECL	MC10H330	–	24	P,L	FN
Quad Bus Driver/Receiver With Transmit & Receiver Latches (25Ω)	ECL	MC10H334	–	20	P,L	FN
Quad Bus Transceiver/Inverting With 3–State Outputs	TTL	SN54LS242	SN74LS242	14	N,J	D
Quad Bus Transceiver/Non–Inverting With 3–State Outputs	TTL	SN54LS243	SN74LS243	14	N,J	D
Quad Bus Transceivers With 3–State Outputs	TTL	MC74F242	–	14	N	D
	TTL	MC74F243	–	14	N	D
Quad With 3–State Outputs Inverting Bus Transceiver	CMOS	MC74HC242	–	14	N	
Triple 3–Input Bus Driver With Enable (25Ω)	ECL	MC10H423	–	16	P,L	FN
Triple 4–3–3 Input Bus Driver (25Ω)	ECL	MC10H123	–	16	P,L	FN
	ECL	MC10123	–	16	P,L	FN
CBM						
CBM – Carrier Band Modem	SXLG	MC68194	–	52		*FJ
CLOCK DISTRIBUTION CHIPS						
1:4 Clock Distribution Chip	ECL	MC10EL15	MC100EL15	16		D
1:5 Clock Distribution Chip	ECL	MC100LVEL14	MC100EL14	20		DW
1:6 Differential Clock Distribution Chip	ECL	MC10E211	MC100E211	28		FN
Low Voltage 1:12 Clock Distribution Chip	SXLG	MPC948	–	32		FA
	SXLG	MPC948L	–	32		FA
Low Voltage 1:9 Clock Distribution Chip	SXLG	MPC947	–	32		FA
Low Voltage 1:9 ECL/PECL Clock Distribution Chip	ECL	MC100LVE111	–	28		FN
CLOCK DRIVERS						
1:2 Differential Clock Driver	ECL	MC10EL11	MC100EL11	8		D
1:6 PCI Clock Generator/Fanout Buffer	CMOS	MPC903	–	16		D
	CMOS	MPC904	–	16		D
	CMOS	MPC905	–	16		D
1:9 Differential Clock Driver With Low Skew, Enable, Vbb	ECL	MC10E111	MC100E111	28		FN

Selection by Function

Description	Tech.	Device(s)		Pins	DIP	SM
CLOCK DRIVERS						
1:9 Differential ECL/PECL RAMBus Clock Buffer	ECL	MC10E411	–	28		FN
1:9 TTL/TTL Clock Distribution Chip	ECL	MC10H645	–	28		FN
3.3/5.0V Fully Integrated PLL Clock Driver	CMOS	MPC974	–	52		FA
50 MHz Low Skew CMOS PLL Clock Driver With µP Power Down	CMOS	MC88920	–	20		DW
66 MHz Low Skew CMOS PLL Clock Driver With µP Power–Down/Power–Up Feature	CMOS	MC88921	–	20		DW
68030/040 PECL/TTL Clock Driver	ECL	MC10H640	MC100H640	28		FN
	ECL	MC10H642	MC100H642	28		FN
	ECL	MC10H644	MC100H644	20		FN
Clock Driver Quad D–Type Flip–Flop w/ Matched Propagation Delays	TTL	MC74F1803	–	14	N	D
	TTL	MC74F803	–	14	N	D
CMOS PLL Clock Driver Programmable Frequency, Low Skew, High Fan–Out	CMOS	MC88PL117	–	52		FN
Dual 3.3V PLL Clock Generator	CMOS	MPC980	–	52		FA
Dual Supply ECL/TTL 1:8 Clock Driver	ECL	MC10H643	MC100H643	28		FN
High Frequency PLL Clock Generator	ECL	MC12429	–	28		FN
	ECL	MC12430	–	28		FN
	ECL	MC12439	–	28		FN
Low Skew CMOS Clock Driver	CMOS	MC88913	–	14	N	D
Low Skew CMOS Clock Driver With Reset	CMOS	MC88914	–	14	N	D
Low Skew CMOS PLL 68060 Clock Driver	CMOS	MC88LV926	–	20		DW
Low Skew CMOS PLL Clock Driver	CMOS	MC88915*55	–	28		FN
	CMOS	MC88915*70	–	28		FN
Low Skew CMOS PLL Clock Driver With Processor Reset	CMOS	MC88916*70	–	20		DW
	CMOS	MC88916*80	–	20		DW
Low Skew CMOS PLL Clock Driver 160 MHz Version	CMOS	MC88915T*160	–	28		FN
133 MHz Version	CMOS	MC88915T*133	–	28		FN
100 MHz Version	CMOS	MC88915T*100	–	28		FN
70 MHz Version	CMOS	MC88915T*70	–	28		FN
55 MHz Version	CMOS	MC88915T*55	–	28		FN
Low Voltage 1:10 CMOS Clock Driver	CMOS	MPC946	–	32		FA
Low Voltage 1:15 Differential ÷1/2 ECL/PECL Clock Driver	ECL	MC100LVE222	–	52		FA
Low Voltage 1:15 PECL to CMOS Clock Driver	CMOS	MPC949	–	52		FA
Low Voltage 1:9 Differential ECL/HSTL to HSTL Clock Driver	CMOS	MPC911	–	28		FN
Low Voltage PECL PLL Clock Driver	CMOS	MPC992	–	32		FA
Low Voltage PLL Clock Driver	CMOS	MPC930	MPC931	32		FA
	CMOS	MPC950	MPC951	32		FA
	CMOS	MPC956	–	32		FA
	CMOS	MPC970	–	52		FA
	CMOS	MPC972	MPC973	52		FA
	CMOS	MPC990	MPC991	52		FA
Low Voltage Wide Fanout PLL Clock Driver	CMOS	MPC952	–	32		FA
PECL/TTL to TTL 1: 8 Clock Distribution Chip	ECL	MC10H646	MC100H646	28		FN
Single Supply PECL/TTL 1:9 Clock Distribution Chip	ECL	MC10H641	MC100H641	28		FN
÷2, ÷4/6 Clock Generation Chip (3.3V)	ECL	MC100LVEL38	MC100EL38	20		DW
÷2/4, ÷4/6 Clock Generation Chip	ECL	MC100LVEL39	MC100EL39	20		DW
÷2,4,8 Differential Clock Driver	ECL	MC10EL34	MC100EL34	16		D
COAX CABLE DRIVERS						
Fibre Channel Coaxial Cable Driver and Loop Resiliency Circuit	SDX	MC10SX1189	–	16		D
300 MBit/s LED Driver for FDDI and Fibre Channel	SDX	MC10SX1130	–	16		D

Selection by Function

Description	Tech.	Device(s)		Pins	DIP	SM
COMPARATORS						
4–Bit Magnitude Comparator	TTL	MC74F85	–	16	N	D
	CMOS	MC74HC85	–	16	N	DT
	TTL	SN54LS85	SN74LS85	16	N,J	D
	CMOS	MC14585B	–	16	P,L	D
5–Bit Magnitude Comparator	ECL	MC10H166	–	16	P,L	FN
	ECL	MC10166	–	16	P,L	FN
8–Bit Equality Comparator	CMOS	MC54HC688	MC74HC688	20	N,J	DW
8–Bit Identity Comparator	CMOS	MC74ACT521	–	20	N	
	TTL	MC74F521	–	20	N	DW
8–Bit Magnitude Comparator	TTL	SN54LS682	SN74LS682	20	N,J	DW
	TTL	SN54LS684	SN74LS684	20	N,J	DW
	TTL	SN54LS688	SN74LS688	20	N,J	DW
9–Bit Magnitude Comparator	ECL	MC10E166	MC100E166	28		FN
Dual Analog Comparator With Latch	ECL	MC10E1651	–	16,20	L	FN
Dual Analog Comparator With Latch (Hi–Perf MC1651)	ECL	MC10E1652	–	16,20	L	FN
CONVERTERS						
4–Bit Parallel to Serial Converter	ECL	MC10E446	MC100E446	28		FN
4–Bit Serial to Parallel Converter	ECL	MC10E445	MC100E445	28		FN
Dual A/D Converter	ECL	MC1650	–	16	L	
	ECL	MC1651	–	16	L	
COUNTERS						
12–Bit Binary Counter	CMOS	MC14040B	–	16	P,L	D
12–Stage Binary Ripple Counter	CMOS	MC54HC4040A	MC74HC4040A	16	N,J	D,DT
	CMOS	MC74AC4040	–	16	N	D
14–Bit Binary Counter	CMOS	MC14020B	–	16	P,L	D
14–Bit Binary Counter and Oscillator	CMOS	MC14060B	–	16	P,L	D
14–Stage Binary Ripple Counter	CMOS	MC74HC4020A	–	16	N	D,DT
	CMOS	MC74AC4020	–	16	N	D
14–Stage Binary Ripple Counter With Oscillator	CMOS	MC54HC4060	MC74HC4060	16	N,J	DT
	CMOS	MC54HC4060A	MC74HC4060A	16	N,J	D,DT
3–Digit BCD Counter	CMOS	MC14553B	–	16	P	DW
4–Bit BCD Decade Counter, Asynchronous Reset	TTL	SN54LS160A	SN74LS160A	16	N,J	D
	TTL	SN54LS162A	SN74LS162A	16	N,J	D
4–Bit Bidirectional Binary Counter, With 3–State Outputs	TTL	MC74F569	–	20	N	DW
4–Bit Bidirectional Decade Counter, With 3–State Outputs	TTL	MC74F568	–	20	N	DW
4–Bit Binary Counter	TTL	SN54LS93	SN74LS93	14	N,J	D
	TTL	SN54LS293	SN74LS293	14	N,J	D
	ECL	MC10H16	–	16	P,L	FN
4–Bit Binary Counter, Synchronous Presettable	CMOS	MC14161B	–	16	P	D
	CMOS	MC14163B	–	16	P	D
4–Bit Binary Counter, Synchronous Reset	TTL	SN54LS161A	SN74LS161A	16	N,J	D
	TTL	SN54LS163A	SN74LS163A	16	N,J	D
4–Bit Up/Down Counter With 3–State Outputs	TTL	SN54LS569A	SN74LS569A	20	N,J	DW
4–Stage Presettable Ripple Counters	TTL	SN54LS196	SN74LS196	14	N,J	D
	TTL	SN54LS197	SN74LS197	14	N,J	D
4–Stage Synchronous Bidirectional Counter	TTL	MC74F168	–	16	N	D
	TTL	MC74F169	–	16	N	D
5 Cascaded BCD Counters	CMOS	MC14534B	–	24	P,L	DW
6–Bit Universal Counter, (Lookahead Carry)	ECL	MC10E136	MC100E136	28		FN
7–Stage Ripple Counter	CMOS	MC14024B	–	14	P,L	D

Selection by Function

Description	Tech.	Device(s)		Pins	DIP	SM
COUNTERS						
8–Bit Bidirectional Binary Counter	TTL	MC74F269	–	24	N	DW
8–Bit Bidirectional Binary Counter, With 3–State Outputs	TTL	MC74F579	–	20	N	DW
	TTL	MC74F779	–	16	N	D
8–Bit Ripple Counter	ECL	MC10E137	MC100E137	28		FN
8–Bit Synchronous Binary Up Counter	ECL	MC10E016	MC100E016	28		FN
BCD Decade Counter, Synchronous Presettable	TTL	MC74F160A	–	16	N	D
	TTL	MC74F162A	–	16	N	D
BCD Decade Synchronous Bidirectional Counter	TTL	SN54LS168	SN74LS168	16	N,J	D
Bi–Quinary Counter	ECL	MC10138	–	16	P,L	FN
Binary Counter	ECL	MC10154	–	16	P,L	
	ECL	MC10178	–	16	P,L	FN
Binary Counter, Synchronous Presettable, 4–Bit	TTL	MC74F161A	–	16	N	D
	TTL	MC74F163A	–	16	N	D
Counter Control Logic	ECL	MC12014	–	16	P,L	
Decade Counter	TTL	SN54LS90	SN74LS90	14	N,J	D
	TTL	SN54LS290	SN74LS290	14	N,J	D
	CMOS	MC14017B	–	16	P,L	D
	CMOS	MC74HC4017	–	16	N	D
Divide By 12 Counter	TTL	SN54LS92	SN74LS92	14	N,J	D
Dual 4–Stage Binary Counter	TTL	SN54LS393	SN74LS393	16	N,J	D
Dual 4–Stage Binary Ripple Counter	CMOS	MC54HC393	MC74HC393	14	N,J	D
Dual 4–Stage Binary Ripple Counter W ÷2, ÷5 Sections	CMOS	MC54HC390	MC74HC390	16	N,J	D
Dual BCD Up Counter	CMOS	MC14518B	–	16	P,L	DW
Dual Binary Up Counter	CMOS	MC14520B	–	16	P,L	DW
Dual Decade Counter	TTL	SN54LS390	SN74LS390	16	N,J	D
	TTL	SN54LS490	SN74LS490	16	N,J	D
Industrial Time Base Generator	CMOS	MC14566B	–	16	P	D
Modulo 16 Binary Synchronous Bidirectional Counter	TTL	SN54LS169	SN74LS169	16	N,J	D
Octal Counter	CMOS	MC14022B	–	16	P,L	D
Phase Comparator and Programmable Counter	CMOS	MC14568B	–	16	P,L	D
Presettable 4–Bit BCD Down Counter	CMOS	MC14522B	–	16	P	DW
Presettable 4–Bit Binary Down Counter	CMOS	MC14526B	–	16	P,L	DW
Presettable 4–Bit Binary Up/Down Counter	TTL	SN54LS191	SN74LS191	16	N,J	D
	TTL	SN54LS193	SN74LS193	16	N,J	D
Presettable BCD Up/Down Counter	CMOS	MC14510B	–	16	P	D
Presettable BCD/Decade Up/Down Counter	TTL	SN54LS190	SN74LS190	16	N,J	D
	TTL	SN54LS192	SN74LS192	16	N,J	D
Presettable Binary Up/Down Counter	CMOS	MC14516B	–	16	P,L	D
Presettable Binary/BCD Up/Down Counter	CMOS	MC14029B	–	16	P,L	D
Presettable Counter	CMOS	MC54HC160	MC74HC160	16	N,J	D
	CMOS	MC54HC161A	MC74HC161A	16	N,J	D
	CMOS	MC54HCT161A	MC74HCT161A	16	N,J	D
	CMOS	MC54HC162	MC74HC162	16	N,J	D
	CMOS	MC54HC163A	MC74HC163	16	N,J	D
	CMOS	MC54HCT163A	MC74HCT163A	16	N,J	D
Presettable Divide–by–N Counter	CMOS	MC14018B	–	16	P	D
Programmable Dual Binary/BCD Counter	CMOS	MC14569B	–	16	P,L	DW

Selection by Function

Description	Tech.	Device(s)		Pins	DIP	SM
COUNTERS						
Programmable Modulo–N Counters (N=0–9)	ECL	MC4016	–	16	P,L	
	ECL	MC4018	–	16	P,L	
	ECL	MC4316	–	16	P,L	
Synchronous 4–Bit Up/Down Counter	TTL	SN54LS669	SN74LS669	16	N,J	D
Synchronous Presettable Binary Counter	CMOS	MC74AC161	–	16	N	D
	CMOS	MC74ACT161	–	16	N	D
Synchronous Presettable Binary Counter	CMOS	MC74AC163	–	16	N	D
	CMOS	MC74ACT163	–	16	N	D
Synchronous Presettable Binary–Coded–Decimal Decade Counter	CMOS	MC74AC160	–	16	N	D
	CMOS	MC74ACT160	–	16	N	D
	CMOS	MC74AC162	–	16	N	D
	CMOS	MC74ACT162	–	16	N	D
Universal Decade Counter	ECL	MC10137	–	16	P,L	
Universal Hexadecimal Counter	ECL	MC10H136	–	16	P,L	FN
	ECL	MC10136	–	16	P,L	FN
Up/Down Counter With Preset and Ripple Clock	CMOS	MC74AC190	–	16	N	D
DECODER/DEMULTIPLEXERS						
1–of–10 Decoder	CMOS	MC74HC42	–	16	N	D
	TTL	SN54LS42	SN74LS42	16	N,J	D
1–of–10 Decoder/Driver Open–Collector	TTL	SN54LS145	SN74LS145	16	N,J	D
1–of–10 Decoder, With 3–State Outputs	TTL	MC74F537	–	20	N	DW
1–of–16 Decoder/Demultiplexer	CMOS	MC54HC154	MC74HC154	24	N,J	DW
1–of–16 Decoder/Demultiplexer With Address Latch	CMOS	MC74HC4514	–	24	N	DW
1–of–4 Decoder, With 3–State Outputs	TTL	MC74F539	–	20	N	DW
1–of–8 Decoder, With 3–State Outputs	TTL	MC74F538	–	20	N	DW
1–of–8 Decoder/Demultiplexer	CMOS	MC74AC138	–	16	N	D
	CMOS	MC74ACT138	–	16	N	D
	TTL	MC74F138	–	16	N	D
	CMOS	MC54HC138A	MC74HC138A	16	N,J	D
	CMOS	MC74VHC138	–	16		D,DT, M
	CMOS	MC74HCT138A	–	16	N	D,DT
	TTL	SN54LS138	SN74LS138	16	N,J	D
1–of–8 Decoder/Demultiplexer With Address Latch	CMOS	MC74HC137	–	16	N	D
	CMOS	MC74HC237	–	16	N	D
3–Line to 8–Line Decoders/Demultiplexers With Address Latches	TTL	SN54LS137	SN74LS137	16	N,J	D
4–Bit Transparent Latch/4–to–16 Line Decoder (High)	CMOS	MC14514B	–	24	P,L	DW
4–Bit Transparent Latch/4–to–16 Line Decoder (Low)	CMOS	MC14515B	–	24	P,L	DW
8–Bit Addressable Latch/1–of–8 Decoder	CMOS	MC54HC259	MC74HC259	16	N,J	D
BCD–to–Decimal Decoder/Binary–to–Octal Decoder	CMOS	MC14028B	–	16	P,L	D
Binary to 1–4 Decoder (Low)	ECL	MC10171	–	16	P,L	FN
Binary to 1–8 Decoder, (High)	ECL	MC10H162	–	16	P,L	FN
	ECL	MC10162	–	16	P,L	FN
Binary to 1–8 Decoder, (Low)	ECL	MC10H161	–	16	P,L	FN
	ECL	MC10161	–	16	P,L	FN
Dual 1–of–4 Decoder	TTL	SN54LS155	SN74LS155	16	N,J	D
Dual 1–of–4 Decoder Open–Collector	TTL	SN54LS156	SN74LS156	16	N,J	D

Selection by Function

Description	Tech.	Device(s)		Pins	DIP	SM
DECODER/DEMULTIPLEXERS						
Dual 1–of–4 Decoder/Demultiplexer	CMOS	MC74AC139	–	16	N	D
	CMOS	MC74ACT139	–	16	N	D
	TTL	MC74F139	–	16	N	D
Dual 1–of–4 Decoder/Demultiplexer	CMOS	MC54HC139A	MC74HC139A	16	N,J	D
	TTL	SN54LS139	SN74LS139	16	N,J	D
Dual Binary to 1–4 Decoder (High)	ECL	MC10H172	–	16	P,L	FN
	ECL	MC10172	–	16	P,L	FN
Dual Binary to 1–4 Decoder (Low)	ECL	MC10H171	–	16	P,L	FN
Dual Binary to 1–of–4 Decoder (Active High Outputs)	CMOS	MC14555B	–	16	P	D
Dual Binary to 1–of–4 Decoder (Active Low Outputs)	CMOS	MC14556B	–	16	P	D
Low–Voltage CMOS 1–of–8 Decoder/Demultiplexer With 5V Tolerant Inputs and Outputs	CMOS	MC74LCX138	–	16		D,DT
Low–Voltage Quiet CMOS 1–of–8 Decoder/Demultiplexer	CMOS	MC74LVQ138	–	16		D,M, SD,DT
DETECTORS						
Analog Mixer	ECL	MC12002	–	14	P,L	
Phase–Frequency Detector	ECL	MC4044	–	14	P,L	D
	ECL	MC4344	–	14	P,L	
	ECL	MC12040	–	14	P,L	FN
	ECL	MCH12140	MCK12140	8		D
DISPLAY DECODE DRIVERS						
BCD–to–Seven Segment Decoder	TTL	SN54LS48	SN74LS48	16	N,J	D
	CMOS	MC14558B	–	16	P,L	D
BCD–to–Seven Segment Decoder/Driver	TTL	SN54LS47	SN74LS47	16	N,J	D
	TTL	SN54LS247	SN74LS247	16	N,J	D
	TTL	SN54LS248	SN74LS248	16	N,J	D
	TTL	SN54LS249	SN74LS249	16	N,J	D
BCD–to–Seven Segment Latch/Decoder/Display Driver	CMOS	MC74HC4511	–	16	N	D
BCD–to–Seven Segment Latch/Decoder/Driver	CMOS	MC14511B	–	16	P,L	D,DW
BCD–to–Seven Segment Latch/Decoder/Driver for Liquid Crystals	CMOS	MC14543B	–	16	P,L	D
BCD–to–Seven Segment Latch/Decoder/Driver With Ripple Blanking	CMOS	MC14544B	–	18	P,L	
	CMOS	MC14513B	–	18	P	
High Current BCD–to–Seven Segment Decoder/Driver	CMOS	MC14547B	–	16	P,L	DW
DIVIDERS						
÷ 2 Divider	ECL	MC10EL32	MC100EL32	8		D
	ECL	MC100LVEL32	–	8		D
÷ 4 Divider	ECL	MC10EL33	MC100EL33	8		D
	ECL	MC100LVEL33	–	8		D
DRIVER						
Coaxial Cable Driver	ECL	MC10EL89	–	8		D
300MBit/s LED Driver for FDDI and Fibre Channel	ECL	MC10SX1130	–	16		D
EDACs						
Error Detection–Correction Circuit (IBM Code)	ECL	MC10163	–	16	P,L	
Error Detection–Correction Circuit (Motorola Code)	ECL	MC10193	–	16	P,L	
ENCODERS						
10–Line to 4–Line Priority Encoder	TTL	SN54LS147	SN74LS147	16	N,J	D
8–Bit Priority Encoder	CMOS	MC14532B	–	16	P,L	D

Selection by Function

Description	Tech.	Device(s)		Pins	DIP	SM
ENCODERS						
8–Input Priority Encoder	TTL	SN54LS348	SN74LS348	16	N,J	D
	ECL	MC10H165	–	16	P,L	FN
	ECL	MC10165	–	16	P,L	FN
8–Input Priority Encoder (Glitchless)	TTL	SN54LS848	SN74LS848	16	N,J	D
8–Line to 3–Line Priority Encoder	TTL	MC74F148	–	16	N	D
	TTL	SN54LS148	SN74LS148	16	N,J	D
	TTL	SN54LS748	SN74LS748	16	N,J	D
Decimal–to–BCD Encoder	CMOS	MC74HC147	–	16	N	D
ENCODER/DECODERS						
CMI Encoder/Decoder	ECL	MC100SX1230	–	28		FN
EXPANDERS						
Dual 4–Iput Expander	HTL	MC669	–	14	P,L	
Expandable Dual 4–Input Gate (Active Pullup)	HTL	MC660	–	14	P,L	
Expandable Dual 4–Input Gate (Passive Pullup)	HTL	MC661	–	14	P,L	
Expandable Dual 4–Input Line Driver	HTL	MC662	–	14	P,L	
Expandable Dual Power Gate	DTL	MC844	–	14	P,L	
	DTL	MC944	–	14	P,L	
FIELD PROGRAMMABLE GATE ARRAY						
14,200–Gate Programmable Array With Up to 160 User I/Os	CMOS	MPA1064	–	160, 224		DH, KE
22,000–Gate Programmable Array With Up to 200 User I/Os	CMOS	MPA1100	–	229		HV
3,500–Gate Programmable Array With Up to 80 User I/Os	CMOS	MPA1016	–	84, 128		FN, DD
8,000–Gate Programmable Array With Up to 120 User I/Os	CMOS	MPA1036	–	84, 128, 160, 181		FN, DD, DH, HI
FLIP–FLOPS						
3–Bit Differential Flip–Flop	ECL	MC10E431	MC100E431	28		FN
4–Bit D Flip–Flop Individual Clock, Reset Differential Output	ECL	MC10E131	MC100E131	28		FN
4–Bit D Flip–Flop With Enable	TTL	SN54LS379	SN74LS379	16	N,J	D
4–Bit D–Type Register With With 3–State Outputs	TTL	SN54LS173A	SN74LS173A	16	N,J	D
5–Bit Differential Register	ECL	MC10E452	MC100E452	28		FN
6–Bit 2:1 Mux–Register With Common Clock, Asynchronous Master Reset Single Ended	ECL	MC10E167	MC100E167	28		FN
6–Bit D Register With Common Clock, Asynchronous Master Reset, Differential Outputs	ECL	MC10E151	MC100E151	28		FN
6–Bit D Register, With Differential Inputs, (Data & Clock) , VBB, Common Reset	ECL	MC10E451	MC100E451	28		FN
6–Bit Parallel D Register With Enable	CMOS	MC74AC378	–	16	N	D
	CMOS	MC74ACT378	–	16	N	D
9–Bit Hold Register, 700MHz, With Asynchronous Master Reset	ECL	MC10E143	MC100E143	28		FN
Clocked Flip–Flop	DTL	MC845	–	14	P,L	
Clocked Flip–Flop	DTL	MC945	–	14	P,L	
D Flip–Flop With Set & Reset	ECL	MC10EL31	MC100EL31	8		D
Differential Clock D Flip–Flop	ECL	MC10EL51	MC100EL51	8		D
	ECL	MC100LVEL51	–	8		D
Differential Data & Clock D Flip–Flop	ECL	MC10EL52	MC100EL52	8		D
Dual D Flip–Flop	CMOS	MC74AC74	–	14	N	D
	CMOS	MC74ACT74	–	14	N	D
	CMOS	MC14013B	–	14	P,L	D

Selection by Function

Description	Tech.	Device(s)		Pins	DIP	SM
FLIP–FLOPS						
Dual D Flip–Flop With Set and Reset	CMOS	MC54HC74A	MC74HC74A	14	N,J	D,DT
	CMOS	MC74VHC74	–	14		D, DT,M
Dual D Flip–Flop With Set and Reset With LSTTL Compatible Inputs	CMOS	MC74HCT74A	–	14	N	D
Dual D–Type Positive Edge–Triggered Flip–Flop	TTL	MC74F74	–	14	N	D
	TTL	SN54LS74A	SN74LS74A	16	N,J	D
Dual Differential Data and Clock D Flip–Flop With Set and Reset	ECL	MC100LVEL29	MC100EL29	20		DW
Dual J–K Negative Edge–Triggered Flip–Flop	TTL	SN54LS112A	SN74LS112A	16	N,J	D
	TTL	SN54LS113A	SN74LS113A	14	N,J	D
	TTL	SN54LS114A	SN74LS114A	14	N,J	D
Dual J–K Positive Edge–Triggered Flip–Flop	TTL	SN54LS109A	SN74LS109A	16	N,J	D
Dual J–K Flip–Flop	HTL	MC663	–	14	P,L	
	TTL	SN54LS107A	SN74LS107A	14	N,J	D
Dual J–K Flip–Flop (Common Clock and CD Separate SD)	DTL	MC952	–	14	P,L	
Dual J–K Flip–Flop (Separate Clock and SD, No CD)	DTL	MC953	–	14	P,L	
Dual J–K Flip–Flop Negative Edge Trigger	CMOS	MC74AC112	–	16	N	D
	CMOS	MC74ACT112	–	16	N	D
Dual J–K Flip–Flop Negative Edge Trigger	CMOS	MC74AC113	–	14	N	D
	CMOS	MC74ACT113	–	14	N	D
Dual J–K Flip–Flop With Set and Clear	TTL	SN54LS76A	SN74LS76A	16	N,J	D
Dual J–K Flip–Flop With Set and Reset	CMOS	MC74HC112	–	16	N	D,DT
Dual J–K Flip–Flop	CMOS	MC14027B	–	16	P,L	D
Dual J–K Flip–Flop With Reset	CMOS	MC74HC73	–	14	N	D
	CMOS	MC74HC107	–	14	N	D
Dual J–K Flip–Flop With Set and Reset	CMOS	MC74HC76	–	16	N	D
Dual J–K Master–Slave Flip–Flop	ECL	MC10135	–	16	P,L	FN
	ECL	MC10H135	–	16	P,L	FN
Dual J–K Negative Edge–Triggered Flip–Flop	TTL	MC74F112	–	16	N	D
	TTL	SN54LS73A	SN74LS73A	14	N,J	D
Dual J–K Positive Edge–Triggered Flip–Flop With Set & Clear	CMOS	MC74AC109	–	16	N	D
	CMOS	MC74ACT109	–	16	N	D
Dual J–K Flip–Flop With Set and Reset	CMOS	MC74HC109	–	16	N	D
Dual J–K Positive Edge–Triggered Flip–Flop	TTL	MC74F109	–	16	N	D
Dual Type–D Master–Slave Flip–Flop	ECL	MC10131	–	16	P,L	FN
	ECL	MC10H131	–	16	P,L	FN
Hex D Flip–Flop	TTL	SN54LS174	SN74LS174	16	N,J	D
	CMOS	MC14174B	–	16	P,L	D
Hex D Flip–Flop With Enable	TTL	SN54LS378	SN74LS378	16	N,J	D
Hex D Flip–Flop With Master Reset	CMOS	MC74AC174	–	16	N	D
	TTL	MC74F174	–	16	N	D
	CMOS	MC74ACT174	–	16	N	D
Hex D Flip–Flop With Common Clock & Reset	CMOS	MC54HC174A	MC74HC174A	16	N,J	D
	CMOS	MC74HCT174A	–	16	N	D
Hex D Master–Slave Flip–Flop	ECL	MC10H176	–	16	P,L	FN
	ECL	MC10176	–	16	P,L	FN
Hex D Master–Slave Flip–Flop With Reset	ECL	MC10H186	–	16	P,L	FN
	ECL	MC10186	–	16	P,L	FN
High Speed Dual D Master–Slave Flip–Flop	ECL	MC10231	–	16	P,L	FN
J–K Flip–Flop	ECL	MC10EL35	MC100EL35	8		D

Selection by Function

Description	Tech.	Device(s)		Pins	DIP	SM
FLIP–FLOPS						
Low–Voltage CMOS Octal D–Type Flip–Flop With Set and Reset, 3–State, Non–Inverting With 5V Tolerant Inputs	CMOS	MC74LCX74	–	14		D,DT
Low–Voltage CMOS 16–Bit D–Type Flip–Flop, 3–State, Non–Inverting With 5V Tolerant Inputs and Outputs	CMOS	MC74LCX16374	–	20		DW,M, DT
Low–Voltage CMOS Octal D–Type Flip–Flop, 3–State, Non–Inverting With 5V Tolerant Inputs and Outputs	CMOS	MC74LCX374	–	20		DW,M, DT
Low–Voltage CMOS Octal D–Type Flip–Flop Flow Through Pinout, 3–State, Non–Inverting With 5V Tolerant Inputs and Outputs	CMOS	MC74LCX574	–	20		DW,M, DT
Low Voltage D Flip–Flop With Set & Reset	ECL	MC100LVEL31	–	8		D
Low–Voltage Quiet CMOS Octal D–Type Flip–Flop	CMOS	MC74LVQ374	–	20		DW,M, SD,DT
Low–Voltage Quiet CMOS Octal D–Type Flip–Flop Flow Through Pinout	CMOS	MC74LVQ574	–	20		DW,M, SD,DT
Master–Slave Flip–Flop	ECL	MC1670	–	16	L	
Master–Slave R–S Flip–Flop	HTL	MC664	–	14	P,L	
Octal 3–State Inverting D Flip–Flop	CMOS	MC54HC534A	MC74HC534A	20	N,J	DW
Octal 3–State Non–Inverting D Flip–Flop With LSTTL Compatible Inputs	CMOS	MC54HCT374A	MC74HCT374A	20	N,J	DW, SD,DT
Octal D Flip Flop, With 3–State Outputs	TTL	MC74F374	–	20	N	DW
Octal D Flip–Flop	CMOS	MC74AC273	–	20	N	DW
	CMOS	MC74ACT273	–	20	N	DW
Octal D Flip–Flop With 3–State Outputs/Broadside Pinout, F374	TTL	MC74F574	–	20	N	DW
Octal D Flip–Flop With Clear	TTL	SN54LS273	SN74LS273	20	N,J	DW
Octal D Flip–Flop With Clock Enable	CMOS	MC74AC377	–	20	N	DW
	CMOS	MC74ACT377	–	20	N	DW
Octal D Flip–Flop With Common Clock & Reset	CMOS	MC54HC273A	MC74HC273A	20	N,J	DW, DT
Octal D Flip–Flop With Common Clock and Reset With LSTTL Compatible Inputs	CMOS	MC74HCT273A	–	20	N	DW
Octal D Flip–Flop With Enable	TTL	MC74F377	–	20	N	DW
Octal D Flip–Flop With Enable/ Non–Inverting	TTL	SN54LS377	SN74LS377	20	N,J	DW
Octal D Type Flip–Flop With 3–State Outputs	CMOS	MC74AC374	–	20	N	DW
	CMOS	MC74ACT374	–	20	N	DW
	TTL	MC74F534	–	20	N	DW
	TTL	SN54LS374	SN74LS374	20	N,J	DW
	CMOS	MC74AC534	–	20	N	DW
	CMOS	MC74ACT534	–	20	N	DW
Octal D–Type Latch With 3–State Outputs	CMOS	MC74AC564	–	20	N	DW
	CMOS	MC74ACT564	–	20	N	DW
	CMOS	MC74AC574	–	20	N	DW
	CMOS	MC74ACT574	–	20	N	DW
Octal With 3–State Outputs Inverting D Flip–Flop	CMOS	MC74HC564A	–	20	N	DW
Octal With 3–State Outputs Non–Inverting D Flip–Flop	CMOS	MC54HC374A	MC74HC374A	20	N,J	DW, SD,DT
	CMOS	MC74VHC374	–	20		DW, DT,M
	CMOS	MC54HC574A	MC74HC574A	20	N,J	DW
	CMOS	MC74VHC574	–	20		DW, DT,M
Octal With 3–State Outputs Non–Inverting D Flip–Flop With LSTTL Compatible Inputs	CMOS	MC54HCT574A	MC74HCT574A	20	N,J	DW
Quad D Flip–Flop	CMOS	MC74AC175	–	16	N	D
	CMOS	MC74ACT175	–	16	N	D
	TTL	MC74F175	–	16	N	D

Selection by Function

Description	Tech.	Device(s)		Pins	DIP	SM
FLIP–FLOPS						
Quad D Flip–Flop	TTL	SN54LS175	SN74LS175	16	N,J	D
	CMOS	MC14175B	–	16	P,L	D
Quad D Flip–Flop With Common Clock & Reset	CMOS	MC54HC175	MC74HC175	16	N,J	D
	CMOS	MC54HC175A	MC74HC175A	16	N,J	D,SD
Quad D–Type Register With 3–State Outputs	CMOS	MC14076B	–	16	P,L	D
Quad Parallel Register With Enable	TTL	MC74F379	–	16	N	D
Quad With 3–State Outputs D Flip–Flop With Common Clock & Reset	CMOS	MC74HC173	–	16	N	D
Triple D Flip–Flop With Set and Reset	ECL	MC100LVEL30	MC100EL30	20		DW
GATES, AND/NAND						
13–Input NAND Gate	CMOS	MC74HC133	–	16	N	D
	TTL	SN54LS133	SN74LS133	16	N,J	D
8–Input NAND Gate	CMOS	MC74HC30	–	14	N	D
	TTL	SN54LS30	SN74LS30	14	N,J	D
	CMOS	MC14068B	–	14	P	D
Dual 4–Input AND Gate	TTL	MC74F21	–	14	N	D
	TTL	SN54LS21	SN74LS21	14	N,J	D
	CMOS	MC14082B	–	14	P,L	D
Dual 4–Input NAND Buffer	TTL	MC74F40	–	14	N	D
	TTL	SN54LS40	SN74LS40	14	N,J	D
Dual 4–Input NAND Gate	CMOS	MC74AC20	–	14	N	D
	CMOS	MC74ACT20	–	14	N	D
	TTL	MC74F20	–	14	N	D
	CMOS	MC74HC20	–	14	N	D
	TTL	SN54LS20	SN74LS20	14	N,J	D
	TTL	SN54LS22	SN74LS22	14	N,J	D
	CMOS	MC14012B	–	14	P,L	D
Dual 4–Input NAND Gate (Unbuffered)	CMOS	MC14012UB	–	14	P,L	D
Expandable NAND Gate	DTL	MC830	–	14	P,L	
Hex AND Gate	ECL	MC10197	–	16	P,L	FN
Low–Voltage CMOS Quad 2–Input AND Gate, 5V–Tolerant Inputs	CMOS	MC74LCX08	–	14		D,DT
Low–Voltage CMOS Quad 2–Input NAND Gate, 5V–Tolerant Inputs	CMOS	MC74LCX00	–	14		D,DT
Low–Voltage Quiet CMOS Quad 2–Input NAND Gate	CMOS	MC74LVQ00	–	14		D,M, DT,SD
Quad 2–Input AND Gate	CMOS	MC74AC08	–	14	N	D
	CMOS	MC74ACT08	–	14	N	D
	TTL	MC74F08	–	14	N	D
	CMOS	MC54HC08A	MC74HC08A	14	N,J	D,DT
	CMOS	MC74VHC08	–	14		D, DT,M
	TTL	SN54LS08	SN74LS08	14	N,J	D
	TTL	SN54LS09	SN74LS09	14	N,J	D
	ECL	MC10H104	–	16	P,L	FN
	ECL	MC10104	–	16	P,L	FN
	CMOS	MC14081B	–	14	P,L	D
Quad 2–Input AND Gate With LSTTL–Compatible Inputs	CMOS	MC54HCT08A	MC74HCT08A	14	N,J	D
Quad 2–Input NAND Buffer	TTL	MC74F37	–	14	N	D
	TTL	SN54LS26	SN74LS26	14	N,J	D
	TTL	SN54LS37	SN74LS37	14	N,J	D

Selection by Function

Description	Tech.	Device(s)		Pins	DIP	SM
GATES, AND/NAND						
Quad 2–Input NAND Buffer Open–Collector	TTL	MC74F38	–	14	N	D
Quad 2–Input NAND Buffer Open–Collector	TTL	SN54LS38	SN74LS38	14	N,J	D
Quad 2–Input NAND Gate	DTL	MC846	–	14	P,L	
	DTL	MC946	–	14	P,L	
	CMOS	MC74AC00	–	14	N	D
	CMOS	MC74ACT00	–	14	N	D
	TTL	MC74F00	–	14	N	D
	CMOS	MC54HC00A	MC74HC00A	14	N,J	D,DT
	CMOS	MC74VHC00	–	14		D, DT,M
	TTL	SN54LS00	SN74LS00	14	N,J	D
	TTL	SN54LS01	SN74LS01	14	N,J	D
	TTL	SN54LS03	SN74LS03	14	N,J	D
	CMOS	MC14011B	–	14	P,L	D
Quad 2–Input NAND Gate (Unbuffered)	CMOS	MC14011UB	–	14	P,L	D
Quad 2–Input NAND Gate With LSTTL–Compatible Inputs	CMOS	MC54HCT00A	MC74HCT00A	14	N,J	D
Quad 2–Input NAND Gate With Open–Drain Outputs	CMOS	MC74HC03A	–	14	N	D,DT
Triple 3–Input AND Gate	CMOS	MC74AC11	–	14	N	D
	CMOS	MC74ACT11	–	14	N	D
	TTL	MC74F11	–	14	N	D
	CMOS	MC74HC11	–	14	N	D
	TTL	SN54LS11	SN74LS11	14	N,J	D
	TTL	SN54LS15	SN74LS15	14	N,J	D
	CMOS	MC14073B	–	14	P,L	D
Triple 3–Input NAND Gate	CMOS	MC74AC10	–	14	N	D
	CMOS	MC74ACT10	–	14	N	D
	TTL	MC74F10	–	14	N	D
	CMOS	MC74HC10	–	14	N	D
	TTL	SN54LS10	SN74LS10	14	N,J	D
	TTL	SN54LS12	SN74LS12	14	N,J	D
	CMOS	MC14023B	–	14	P,L	D
Triple 3–Input NAND Gate (Unbuffered)	CMOS	MC14023UB	–	14	P,L	D
GATES, COMPLEX						
2–Input AND/NAND Gate	ECL	MC10EL04	MC100EL04	8		D
2–Input Differential AND/NAND Gate	ECL	MC10EL05	MC100EL05	8		D
	ECL	MC100LVEL05	–	8		D
2–Input XOR/NOR Gate	ECL	MC10EL07	MC100EL07	8		D
2–Wide, 2–Input/2–Wide, 3–Input AND–NOR Gate	CMOS	MC74HC51	–	14	N	D
2–Wide, 2–Input/2–Wide, 3–Input AND–OR Gate	CMOS	MC74HC58	–	14	N	D
2–Wide, 4–Input AND/OR Invert Gate	TTL	SN54LS55	SN74LS55	14	N,J	D
3–2–2–3–Input AND/OR Invert Gate	TTL	SN54LS54	SN74LS54	14	N,J	D
4–2–3–2 Input AND–OR–Invert Gate	TTL	MC74F64	–	14	N	D
4–Bit AND/OR Selector	CMOS	MC14519B	–	16	P	D
4–Input OR/NOR Gate	ECL	MC10EL01	MC100EL01	8		D
	ECL	MC100LVEL01	–	8		D
4–Wide 4–3–3–3 Input OR–AND Gate	ECL	MC10H119	–	16	P,L	FN
4–Wide OR–AND/OR–AND–Invert Gate	ECL	MC10H121	–	16	P,L	FN
4–Wide OR–AND/OR–AND–Invert Gate	ECL	MC10121	–	16	P,L	FN

Selection by Function

Description	Tech.	Device(s)		Pins	DIP	SM
GATES, COMPLEX						
8–Input NOR/OR Gate	CMOS	MC74HC4078	–	14	N	D
Dual 2 Wide 2–Input/3–Input AND/OR Invert Gate	TTL	SN54LS51	SN74LS51	14	N,J	D
Dual 2–Wide 2–3–Input OR–AND/OR–AND–Invert Gate	ECL	MC10117	–	16	P,L	FN
	ECL	MC10H117	–	16	P,L	FN
Dual 2–Wide 2–Input, 2–Wide 3–Input AND–OR–Invert Gate	TTL	MC74F51	–	14	N	D
Dual 2–Wide 3–Input OR–AND Gate	ECL	MC10H118	–	16	P,L	FN
Dual 4–5 Input OR/NOR Gate	ECL	MC10H109	–	16	P,L	FN
	ECL	MC10109	–	16	P,L	FN
	ECL	MC10H209	–	16	P,L	FN
Dual 4–Input NAND, 2–Input NOR/OR, 8–Input AND/NAND Gate (Unbuffered)	CMOS	MC14501UB	–	16	P	D
Dual 4–Input OR/NOR Gate	ECL	MC1660	–	16	L	
Dual 5–Input Majority Logic Gate	CMOS	MC14530B	–	16	P	D
Dual Expandable AND OR Invert Gate (Unbuffered)	CMOS	MC14506UB	–	16	L	
Hex NAND/NOR/Invert Gate (Unbuffered)	CMOS	MC14572UB	–	16	P	D
High Speed Dual 3–Input 3–Output OR/NOR Gate	ECL	MC10212	–	16	P	
Quad 4–Input OR/NOR Gate	ECL	MC10E101	MC100E101	28		FN
Quad Differential AND/NAND Gate	ECL	MC10E404	MC100E404	28		FN
Quad OR/NOR Gate	ECL	MC10H101	–	16	P,L	FN
	ECL	MC10101	–	16	P,L	FN
Quint 2–Input AND/NAND Gate	ECL	MC10E104	MC100E104	28		FN
Quint 2–Input XOR/XNOR Gate	ECL	MC10E107	MC100E107	28		FN
Triple 2–3–2 Input OR/NOR Gate	ECL	MC10H105	–	16	P,L	FN
	ECL	MC10105	–	16	P,L	FN
Triple 2–Input Exclusive OR/Exclusive NOR Gate	ECL	MC10H107	–	16	P,L	FN
	ECL	MC10107	–	16	P,L	FN
GATES, EXCLUSIVE OR/EXCLUSIVE NOR						
Low–Voltage CMOS Quad 2–Input Exclusive OR Gate With 5V Tolerant Inputs	CMOS	MC74LCX86	–	14		D,M SD,DT
Quad 2–Input Exclusive NOR Gate	CMOS	MC74AC810	–	14	N	DW
	CMOS	MC74ACT810	–	14	N	DW
	CMOS	MC74HC7266	–	14	N	D
	CMOS	MC74HC7266A	–	14	N	D,DT
	TTL	SN54LS266	SN74LS266	14	N,J	D
Quad Exclusive NOR Gate	CMOS	MC14077B	–	14	P,L	D
Quad 2–Input Exclusive OR Gate	CMOS	MC74AC86	–	14	N	D
	CMOS	MC74ACT86	–	14	N	D
	TTL	MC74F86	–	14	N	D
	CMOS	MC54HC86	MC74HC86	14	N,J	D
	CMOS	MC54HC86A	MC74HC86A	14	N,J	D,DT
	TTL	SN74LS136	–	14	N,J	D
	TTL	SN54LS386	SN74LS386	14	N,J	D
Quad Exclusive OR Gate	TTL	SN54LS86	SN74LS86	14	N,J	D
	ECL	MC10H113	–	16	P,L	FN
	ECL	MC10113	–	16	P,L	FN
	CMOS	MC14070B	–	14	P,L	D
Triple 2–Input Exclusive–OR Gate	ECL	MC1672	–	16	L	

Selection by Function

Description	Tech.	Device(s)		Pins	DIP	SM
GATES, NOR						
8–Input NOR Gate	CMOS	MC14078B	–	14	P	D
Dual 3–Input 3–Output NOR Gate	ECL	MC10111	–	16	P,L	FN
	ECL	MC10H211	–	16	P,L	FN
	ECL	MC10211	–	16	P,L	FN
Dual 4–Input NOR Gate	CMOS	MC74HC4002	–	14	N	D
	CMOS	MC14002B	–	14	P,L	D
Dual 4–Input NOR Gate (Unbuffered)	CMOS	MC14002UB	–	14	P,L	D
Dual 5–Input NOR Gate	TTL	SN54LS260	SN74LS260	14	N,J	D
Low–Voltage CMOS Quad 2–Input NOR Gate, 5V–Tolerant Inputs	CMOS	MC74LCX02	–	14		D,DT
Quad 2–Input NOR Buffer	TTL	SN54LS28	SN74LS28	14	N,J	D
	TTL	SN54LS33	SN74LS33	14	N,J	D
Quad 2–Input NOR Gate	CMOS	MC74AC02	–	14	N	D
	CMOS	MC74ACT02	–	14	N	D
	TTL	MC74F02	–	14	N	D
	CMOS	MC54HC02A	MC74HC02A	14	N,J	D,DT
	CMOS	MC74VHC02	–	14		D, DT,M
	TTL	SN54LS02	SN74LS02	14	N,J	D
	ECL	MC10H102	–	16	P,L	FN
	ECL	MC10102	–	16	P,L	FN
	ECL	MC1662	–	16	L	
	CMOS	MC14001B	–	14	P,L	D
Quad 2–Input NOR Gate (Unbuffered)	CMOS	MC14001UB	–	14	P,L	D
Quad 2–Input NOR Gate With strobe	ECL	MC10H100	–	16	P,L	FN
Triple 3–Input NOR Gate	CMOS	MC54HC27	MC74HC27	14	N,J	D
	TTL	SN54LS27	SN74LS27	14	N,J	D
	CMOS	MC14025B	–	14	P,L	D
Triple 3–Input NOR Gate (Unbuffered)	CMOS	MC14025UB	–	14	P,L	D
Triple 4–3–3 Input NOR Gate	ECL	MC10H106	–	16	P,L	FN
	ECL	MC10106	–	16	P,L	FN
GATES, OR						
Dual 3–Input 3–Output OR Gate	ECL	MC10110	–	16	P,L	FN
	ECL	MC10H210	–	16	P,L	FN
	ECL	MC10210	–	16	P,L	FN
Dual 4–Input OR Gate	CMOS	MC14072B	–	14	P	D
Low–Voltage CMOS Quad 2–Input OR Gate, 5V–Tolerant Inputs	CMOS	MC74LCX32	–	14		D,DT
Low–Voltage Quiet CMOS Quad 2–Input OR Gate, 5V–Tolerant Inputs	CMOS	MC74LVQ32	–	14		D,M SD,DT
Quad 2–Input OR Gate	CMOS	MC74AC32	–	14	N	D
	CMOS	MC74ACT32	–	14	N	D
	TTL	MC74F32	–	14	N	D
	CMOS	MC54HC32A	MC74HC32A	14	N,J	D,DT
	CMOS	MC74VHC32	–	14		D, DT,M
	CMOS	MC54HCT32A	MC74HCT32A	14	N,J	D
	TTL	SN54LS32	SN74LS32	14	N,J	D
	ECL	MC10H103	–	16	P,L	FN
	ECL	MC10103	–	16	P,L	FN
	CMOS	MC14071B	–	14	P,L	D

Selection by Function

Description	Tech.	Device(s)		Pins	DIP	SM
GATES, OR						
Triple 3–Input OR Gate	CMOS	MC74HC4075	–	14	N	D
	CMOS	MC14075B	–	14	P,L	D
INDUSTRIAL CONTROL UNIT						
Industrial Control Unit	CMOS	MC14500B	–	16	P	DW
INVERTERS						
Hex Inverter	DTL	MC836	–	14	P	
	DTL	MC837	–	14	P	
	DTL	MC936	–	14	P,L	
	DTL	MC937	–	14	P,L	
Hex Inverter (Without Input Diodes)	DTL	MC840	–	14	P	
INVERTER/BUFFERS, 2–STATE						
9–Bit Buffer	ECL	MC10E122	MC100E122	28		FN
Driver	ECL	MC10EL12	MC100EL12	8		D
	ECL	MC100LVEL12	–	8		D
Dual Complementary Pair Plus Inverter (Unbuffered)	CMOS	MC14007UB	–	14	P	D
Hex Buffer With Enable	ECL	MC10H188	–	16	P,L	FN
	ECL	MC10188	–	16	P,L	FN
Hex Buffer/Non–Inverting	CMOS	MC14050B	–	16	P,L	D
Hex Inverter	CMOS	MC74AC04	–	14	N	D
	CMOS	MC74ACT04	–	14	N	D
	TTL	MC74F04	–	14	N	D
	CMOS	MC54HC04A	MC74HC04A	14	N,J	D,SD, DT
	CMOS	MC74VHC04	–	14		D, DT,M
	TTL	SN54LS04	SN74LS04	14	N,J	D
	TTL	SN54LS05	SN74LS05	14	N,J	D
Hex Inverter Gate (Unbuffered)	CMOS	MC14069UB	–	14	P,L	D
Hex Inverter With Enable	ECL	MC10H189	–	16	P,L	FN
	ECL	MC10189	–	16	P,L	FN
Hex Inverter With LSTTL Compatible Inputs	CMOS	MC74HCT04A	–	14	N	D,DT
Hex Inverter With open Drain Outputs	CMOS	MC74AC05	–	14	N	D
	CMOS	MC74ACT05	–	14	N	D
Hex Inverter With Strobe (Active Pullup)	HTL	MC677	–	14	P,L	
Hex Inverter With Strobe (Without Output Resistors)	HTL	MC678	–	14	P,L	
Hex Inverter/Buffer	ECL	MC10195	–	16	P,L	FN
	CMOS	MC14049B	–	16	P	D
Hex Inverter/Buffer (Unbuffered)	CMOS	MC14049UB	–	16	P,L	D
Hex Inverting Buffer/Logic–Level Down Converter	CMOS	MC54HC4049	MC74HC4049	16	N,J	D
Hex Non–Inverting Buffer/Logic–Level Down Converter	CMOS	MC54HC4050	MC74HC4050	16	N,J	D
Hex Unbuffered Inverter	CMOS	MC74HCU04	–	14	N	D
	CMOS	MC74HCU04A	–	14	N	D,DT
Low–Voltage CMOS Hex Inverter, With 5V–Tolerant Inputs	CMOS	MC74LCX04	–	14		D,DT
Low–Voltage Quiet CMOS Hex Inverter	CMOS	MC74LVQ04	–	14		D,M, SD,DT
Quad 2–Input Gate (Active Pullup)	HTL	MC672	–	14	P,L	
Quad 2–Input Gate (Passive Pullup)	HTL	MC668	–	14	P,L	
Quad Driver	ECL	MC10E112	MC100E112	28		FN
Strobed Hex Inverter/Buffer	CMOS	MC14502B	–	16	P,L	DW
Triple 3–Input Gate (Active Pullup)	HTL	MC671	–	14	P,L	
Triple 3–Input Gate (Passive Pullup)	HTL	MC670	–	14	P,L	

Selection by Function

Description	Tech.	Device(s)		Pins	DIP	SM
LATCHES						
3–Bit 4:1 Mux–Latch (Integrated E156 & E171)	ECL	MC10E256	MC100E256	28		FN
3–Bit 4:1 Mux–Latch, With Common Enable, Asynchronous Master Reset, Differential Output	ECL	MC10E156	MC100E156	28		FN
4–Bit D Latch	TTL	SN54LS75	SN74LS75	16	N,J	D
	TTL	SN54LS77	SN74LS77	14	N,J	D
	TTL	SN54LS375	SN74LS375	16	N,J	D
5–Bit 2:1 Mux–Latch, With Common Enable, Asynchronous Master Reset Differential Output	ECL	MC10E154	MC100E154	28		FN
6–Bit 2:1 Mux–Latch, With Common Enable, Asynchronous Master Reset Single Ended	ECL	MC10E155	MC100E155	28		FN
6–Bit D Latch	ECL	MC10E150	MC100E150	28		FN
8–Bit Addressable Latch	CMOS	MC74AC259	–	16	N	D
	CMOS	MC74ACT259	–	16	N	D
	TTL	MC74F259	–	16	N	D
	TTL	SN54LS259	SN74LS259	16	N,J	D
	CMOS	MC14099B	–	16	P	DW
	CMOS	MC14599B	–	18	P	
8–Bit Bus Compatible Addressable Latch	CMOS	MC14598B	–	18	P,L	
9–Bit Latch, With Parity	ECL	MC10E175	MC100E175	28		FN
Dual Latch	ECL	MC10H130	–	16	P,L	FN
Dual 2–Bit Transparent Latch	CMOS	MC74HC75	–	16	N	D
Dual 4–Bit Addressable Latch	CMOS	MC74AC256	–	16	N	DW
	CMOS	MC74ACT256	–	16	N	DW
	TTL	MC74F256	–	16	N	D
	TTL	SN54LS256	–	16	N,J	D
Dual 4–Bit Latch	CMOS	MC14508B	–	24	P,L	DW
Dual Latch	ECL	MC10130	–	16	P,L	FN
Low–Voltage CMOS Octal Transparent Latch, 3–State, Non–Inverting With 5V Tolerant Inputs and Outputs	CMOS	MC74LCX373	–	20		DW,M, DT
Low–Voltage CMOS 16–Bit Transparent Latch, 3–State, Non–Inverting With 5V Tolerant Inputs and Outputs	CMOS	MC74LCX16373	–	48		DT
Low–Voltage CMOS Octal Transparent Latch Flow Through Pinout, 3–State, Non–Inverting With 5V Tolerant Inputs and Outputs	CMOS	MC74LCX573	–	20		DW,M, SD,DT
Low–Voltage Quiet CMOS Octal Transparent Latch	CMOS	MC74LVQ373	–	20		DW,M, SD,DT
Low–Voltage Quiet CMOS Octal Transparent Latch Flow Through Pinout	CMOS	MC74LVQ573	–	20		DW,M, SD,DT
Octal 3–State Non–Inverting Transparent Latch With LSTTL Compatible Inputs	CMOS	MC54HCT373A	MC74HCT373A	20	N,J	DW, SD,DT
Octal D Latch With 3–State Outputs	CMOS	MC74AC563	–	20	N	DW
	CMOS	MC74ACT563	–	20	N	DW
	CMOS	MC74AC573	–	20	N	DW
	CMOS	MC74ACT573	–	20	N	DW
Octal Transparent Latch With 3–State Outputs	CMOS	MC74AC373	–	20	N	DW
	CMOS	MC74ACT373	–	20	N	DW
	TTL	SN54LS373	SN74LS373	20	N,J	DW
	TTL	MC74F373	–	20	N	DW
	TTL	MC74F533	–	20	N	DW
	CMOS	MC74AC533	–	20	N	DW
	CMOS	MC74ACT533	–	20	N	DW

Selection by Function

Description	Tech.	Device(s)		Pins	DIP	SM
LATCHES						
Octal With 3–State Outputs Inverting Transparent Latch	CMOS	MC54HC533A	MC74HC533A	20	N,J	DW
	CMOS	MC54HC563A	MC74HC563A	20	N,J	DW,DT
Octal With 3–State Outputs Non–Inverting Transparent Latch	CMOS	MC54HC373A	MC74HC373A	20	N,J	DW, DT,SD
	CMOS	MC74VHC373	–	20		DW, DT,M
	CMOS	MC54HC573A	MC74HC573A	20	N,J	DW
	CMOS	MC74VHC573	–	20		DW, DT,M
Octal With 3–State Outputs Non–Inverting Transparent Latch With LSTTL Compatible Inputs	CMOS	MC74HCT573A	–	20	N	DW
Quad Latch	ECL	MC10133	–	16	P,L	FN
	ECL	MC10153	–	16	P,L	FN
Quad NAND R–S Latch	CMOS	MC14044B	–	16	P	D
Quad NOR R–S Latch	CMOS	MC14043B	–	16	P,L	D
Quad Set/Reset Latch	TTL	SN54LS279	SN74LS279	16	N,J	D
Quad Transparent Latch	CMOS	MC14042B	–	16	P,L	D
Quint Latch	ECL	MC10H175	–	16	P,L	FN
	ECL	MC10175	–	16	P,L	FN
MEMORY SUPPORT						
4–Bit ECL–TTL Load Reducing DRAM Driver	ECL	MC10H660	MC100H660	28		FN
MISCELLANEOUS						
Data Separator	ECL	MC10E197	–	28		FN
MULTIPLEXER/DATA SELECTORS						
1–of–8 Decoder/Demultiplexer	CMOS	MC74AC151	–	16	N	D
	CMOS	MC74ACT151	–	16	N	D
16–Channel Analog Multiplexer/Demultiplexer	CMOS	MC14067B	–	24	P	DW
16:1 Multiplexer	ECL	MC10E164	MC100E164	28		FN
2–Bit 8:1 Multiplexer	ECL	MC10E163	MC100E163	28		FN
2:1 Multiplexer	ECL	MC10EL58	MC100EL58	8		D
3–Bit 4:1 Multiplexer, With Split Select Differential Output	ECL	MC10E171	MC100E171	28		FN
4:1 Differential Multiplexer	ECL	MC10EL57	MC100EL57	16		D
5–Bit 2:1 Multiplexer, With Differential Output	ECL	MC10E158	MC100E158	28		FN
8–Channel Analog Multiplexer/Demultiplexer With Address Latch	CMOS	MC54HC4351	MC74HC4351	20	N,J	DW
8–Channel Analog Multiplexer/Demultiplexer	CMOS	MC54HC4051	MC74HC4051	16	N,J	D, DW ,DT
	CMOS	MC14051B	–	16	P,L	D
8–Channel Data Selector	CMOS	MC14512B	–	16	P,L	D
8–Input Data Selector/Multiplexer	CMOS	MC74HC151	–	16	N	D
8–Input Data Selector/Multiplexer With 3–State Outputs	CMOS	MC54HC251	MC74HC251	16	N,J	D
8–Input Multiplexer	TTL	MC74F151	–	16	N	D
	TTL	SN54LS151	SN74LS151	16	N,J	D
8–Input Multiplexer With 3–State Outputs	TTL	SN54LS251	SN74LS251	16	N,J	D
	TTL	MC74F251	–	16	N	D
	CMOS	MC74AC251	–	16	N	D
	CMOS	MC74ACT251	–	16	N	D
8–Input Data Selector/Multiplexer With Data and Address Latchs and With 3–State Outputs	CMOS	MC54HC354	MC74HC354	20	N,J	DW
8–Line Multiplexer	ECL	MC10H164	–	16	P,L	FN
	ECL	MC10164	–	16	P,L	FN
Analog Multiplexer/Demultiplexer With Injection Current Effect Control, Automotive Customized	CMOS	MC74HC4851A	MC74HC4852A	16	N	D,DW, DT
		MC74HC4853A	–			

Selection by Function

Description	Tech.	Device(s)		Pins	DIP	SM
MULTIPLEXER/DATA SELECTORS						
Dual 4–Channel Analog Data Selector	CMOS	MC14529B	–	16	P	D
Dual 4–Channel Analog Multiplexer/Demultiplexer	CMOS	MC74HC4052	–	16	N	D, DW
	CMOS	MC14052B	–	16	P,L	D
Dual 4–Channel Data Selector/Multiplexer	CMOS	MC14539B	–	16	P	D
Dual 4–Input Data Selector/Multiplexer	CMOS	MC74HC153	–	16	N	D
Dual 4–Input Data Selector/Multiplexer With 3–State Outputs	CMOS	MC74HC253	–	16	N	D
Dual 4–Input Multiplexer	CMOS	MC74AC153	–	16	N	D
	CMOS	MC74ACT153	–	16	N	D
	CMOS	MC74AC352	–	16	N	DW
	CMOS	MC74ACT352	–	16	N	DW
	TTL	MC74F153	–	16	N	D
	TTL	MC74F352	–	16	N	D
	TTL	SN54LS153	SN74LS153	16	N,J	D
	TTL	SN54LS352	SN74LS352	16	N,J	D
Dual 4–Input Multiplexer With 3–State Outputs	CMOS	MC74AC253	–	16	N	DW
	CMOS	MC74ACT253	–	16	N	DW
	CMOS	MC74AC353	–	16	N	D
	CMOS	MC74ACT353	–	16	N	D
	TTL	SN54LS253	SN74LS253	16	N,J	D
	TTL	SN54LS353	SN74LS353	16	N,J	D
	TTL	MC74F253	–	16	N	D
	TTL	MC74F353	–	16	N	D
Dual 4–to–1 Multiplexer	ECL	MC10H174	–	16	P,L	FN
	ECL	MC10174	–	16	P,L	FN
Dual Differential 2:1 Multiplexer (3.3V)	ECL	MC100LVEL56	MC100EL56	20		DW
Dual Multiplexer With Latch	ECL	MC10134	–	16	P,L	FN
Low Voltage 16:1 Multiplexer	ECL	MC100LVE164	–	32		FA
Low–Voltage CMOS Quad 2–Input, Non–Inverting With 5V Tolerant Inputs and Outputs	CMOS	MC74LCX157	–	16		M,D, SD,DT
Quad 2–Input Multiplexer With Latch	ECL	MC10H173	–	16	P,L	FN
Quad 2–Channel Analog Multiplexer/Demultiplexer	CMOS	MC14551B	–	16	P	D
Quad 2–Input Data Selector/Multiplexer	CMOS	MC54HC158	MC74HC158	16	N,J	D
	CMOS	MC74HC158A	–	16	N,J	D,DT
Quad 2–Input Data Selector/Multiplexer With 3–State Outputs	CMOS	MC74HC257	–	16	N	D
Quad 2–Input Data Selectors/Multiplexers	CMOS	MC54HC157A	MC74HC157A	16	N,J	D,DT
	CMOS	MC74VHC157	–	16		D, DT,M
Quad 2–Input Data Selector/Multiplexer With LSTTL Compatible Inputs	CMOS	MC74HCT157A	–	16	N	D
Quad 2–Input Multiplexer	TTL	MC74F157A	–	16	N	D
	TTL	MC74F158A	–	16	N	D
	TTL	SN54LS157	SN74LS157	16	N,J	D
	TTL	SN54LS158	SN74LS158	16	N,J	D
Quad 2–Input Multiplexer (Inverting)	ECL	MC10159	–	16	P,L	FN
Quad 2–Input Multiplexer (Non–Inverting)	ECL	MC10158	–	16	P,L	FN
Quad 2–Input Multiplexer Inverting With 3–State Outputs	CMOS	MC74AC258	–	16	N	DW
	CMOS	MC74ACT258	–	16	N	DW
Quad 2–Input Multiplexer Non–Inverting With 3–State Outputs	CMOS	MC74ACT257	–	16	N	D
	CMOS	MC74AC257	–	16	N	D
Quad 2–Input Multiplexer With 3–State Outputs	TTL	SN54LS257B	SN74LS257B	16	N,J	D
Quad 2–Input Multiplexer With Storage	TTL	SN54LS298	SN74LS298	16	N,J	D

Selection by Function

Description	Tech.	Device(s)		Pins	DIP	SM
MULTIPLEXER/DATA SELECTORS						
Quad 2–Input Multiplexer, Inverting	CMOS	MC74AC158	–	16	N	D
	CMOS	MC74ACT158	–	16	N	D
Quad 2–Input Multiplexer, Inverting Output	ECL	MC10H159	–	16	P,L	FN
Quad 2–Input Multiplexer, Inverting, With 3–State Outputs	TTL	SN54LS258B	SN74LS258B	16	N,J	D
Quad 2–Input Multiplexer, Non–Inverting	CMOS	MC74AC157	–	16	N	D
	CMOS	MC74ACT157	–	16	N	D
Quad 2–Input Multiplexer, Non–Inverting Output	ECL	MC10H158	–	16	P,L	FN
Quad 2–Input Multiplexer, With 3–State Outputs	TTL	MC74F257A	–	16	N	D
	TTL	MC74F258A	–	16	N	D
Quad 2–Input Multiplexer/Latch	ECL	MC10173	–	16	P,L	FN
Quad 2–Port Register	TTL	MC74F398	–	20	N	DW
	TTL	MC74F399	–	16	N	D
	TTL	SN54LS398	SN74LS398	20	N,J	DW
	TTL	SN54LS399	SN74LS399	16	N,J	D
Quad 2:1 Mux, Individual–Select	ECL	MC10E157	MC100E157	28		FN
Quad Analog Switch/Multiplexer	CMOS	MC14016B	–	14	P,L	D
	CMOS	MC14066B	–	14	P,L	D
Quad Analog Switch/Multiplexer/Demultiplexer	CMOS	MC54HC4016	MC74HC4016	14	N,J	D
	CMOS	MC54HC4066	MC74HC4066	14	N,J	D,DT
Quad Analog Switch/Multiplexer/Demultiplexer With Separate Analog/Digital Power Supplies	CMOS	MC74HC4316	–	16	N	D
Triple 2–Channel Analog Multiplexer/Demultiplexer	CMOS	MC54HC4053	MC74HC4053	16	N,J	D, DW
	CMOS	MC14053B	–	16	P,L	D
Triple 2–Channel Analog Multiplexer/Demultiplexer With Address Latch	CMOS	MC54HC4353	MC74HC4353	20	N,J	DW
Triple 2:1 Multiplexer	ECL	MC100EL59	–	20		DW
Triple 2:1 Multiplexer (3.3V)	ECL	MC100LVEL59	–	20		DW
Triple Differential 2:1 Multiplexer	ECL	MC100E457	–	28		FN
	ECL	MC10E457	–	28		FN
MULTIVIBRATORS						
130MHz Voltage Controlled Multivibrator	ECL	MC12101	–	20	P	FN
200 MHz Voltage Controlled Multivibrator	ECL	MC12100	–	20	P	FN
Dual Monostable Multivibrator	HTL	MC667	–	14	P,L	
	CMOS	MC14528B	–	16	P,L	D
Dual Monstable Multivibrators With Schmitt Trigger Inputs	TTL	SN54LS221	SN74LS221	16	N,J	D
Dual Precision Monostable Multivibrator Retriggerable, Resettable)	CMOS	MC54HC4538A	MC74HC4538A	16	N,J	D
Dual Precision Monostable Multivibrator	CMOS	MC14538B	–	16	P,L	D, DW
Dual Voltage–Controlled Multivibrator	ECL	MC4024	–	14	P,L	
Monostable Multivibrator	DTL	MC951	–	14	P,L	
	ECL	MC10198	–	16	P,L	FN
Retriggerable Monostable Multivibrators	TTL	SN54LS122	SN74LS122	14	N,J	D
	TTL	SN54LS123	SN74LS123	14	N,J	D
Voltage Controlled Multivibrator	ECL	MC1658	–	16	P,L	D,FN
OSCILLATORS						
7–Stage Binary Ripple Counter	CMOS	MC74HC4024	–	14	N	D
Crystal Oscillator	ECL	MC12061	–	16	P,L	
Dual Voltage–Controlled Multivibrator	ECL	MC4324	–	14	P,L	
Low Power Voltage Controlled Oscillator	ECL	MC12148	–	8		D,SD

Selection by Function

Description	Tech.	Device(s)		Pins	DIP	SM
OSCILLATORS						
Voltage Controlled Oscillator	ECL	MC1648	–	14	P,L	D,FN
OSCILLATOR/TIMERS						
24–Stage Frequency Divider	CMOS	MC14521B	–	16	P,L	D
Programmable Oscillator Timer	CMOS	MC14541B	–	14	P,L	D
Programmable Timer	CMOS	MC14536B	–	16	P,L	DW
Quad Precision Timer/Driver	CMOS	MC14415	–	16	P,L	DW
PARITY CHECKERS						
12–Bit Parity Generator/Checker	ECL	MC10H160	–	16	P,L	FN
	ECL	MC10160	–	16	P,L	FN
12–Bit Parity Generator/Checker, Register–Shiftable, Diff Output	ECL	MC10E160	MC100E160	28		FN
12–Bit Parity Tree	CMOS	MC14531B	–	16	P	D
9 + 2–Bit Parity Generator–Checker	ECL	MC10170	–	16	P,L	FN
9–Bit Odd/Even Parity Generator/Checker	CMOS	MC74HC280	–	14	N	D
	TTL	SN54LS280	SN74LS280	14	N,J	D
9–Bit Parity Generator/Checker	TTL	MC74F280	–	14	N	D
Error Detection and Correction Circuit	ECL	MC10E193	MC100E193	28		FN
PHASE–LOCKED LOOP						
Phase–Locked Loop	CMOS	MC14046B	–	16	P,L	DW
PRESCALERS						
1.1GHz ÷10/20/40/80 Prescaler	ECL	MC12080	–	8	P	D
1.1GHz ÷126/128, ÷254/256 Low Power Dual Modulus Prescaler	ECL	MC12058	–	8		D,SD
1.1GHz ÷127/128, ÷255/256 Low Power Dual Modulus Prescaler	ECL	MC12038A	–	8	P	D
1.1GHz ÷8/9, ÷16/17 Dual Modulus Prescaler	ECL	MC12026A	–	8	P	D
	ECL	MC12026B	–	8	P	D
1.1GHz ÷2 Low Power Prescaler With Stand–By Mode	ECL	MC12083	–	8	P	D
1.1GHz ÷2/4/8 Low Power Prescaler With Stand–By Mode	ECL	MC12093	–	8	P	D,SD
1.1GHz ÷256 Prescaler	ECL	MC12074	–	8	P	D
1.1GHz ÷32/33, ÷64/65 Dual Modulus Prescaler	ECL	MC12028A	–	8	P	D
1.1GHz ÷32/33, ÷64/65 Dual Modulus Prescaler	ECL	MC12028B	–	8	P	D
1.1GHz ÷64 Prescaler	ECL	MC12073	–	8	P	D
1.1GHz ÷64/65, ÷128/129 Dual Modulus Prescaler	ECL	MC12022A	–	8	P	D
	ECL	MC12022B	–	8	P	D
	ECL	MC12022SLA	–	8	P	D
	ECL	MC12022SLB	–	8	P	D
	ECL	MC12022TSA	–	8	P	D
	ECL	MC12022TSB	–	8	P	D
1.1GHz ÷64/65, ÷128/129 Dual Modulus Prescaler With Stand–By Mode	ECL	MC12036A	–	8	P	D
	ECL	MC12036B	–	8	P	D
1.1GHz ÷64/65, ÷128/129 Low Voltage Dual Modulus Prescaler	ECL	MC12022LVA	–	8	P	D
	ECL	MC12022LVB	–	8	P	D
	ECL	MC12022TVA	–	8	P	D
	ECL	MC12022TVB	–	8	P	D
1.1GHz ÷64/65, ÷128/129 Super Low Power Dual Modulus Prescaler	ECL	MC12052A	–	8		D,SD
1.1GHz ÷64/65, ÷128/129 Super Low Power Dual Modulus Prescaler With Stand–By Mode	ECL	MC12053A	–	8		D,SD
1.3GHz ÷64 Prescaler	ECL	MC12075	–	8	P	D
1.3GHz ÷64/256 Prescaler	ECL	MC12066	–	8		D

Selection by Function

Description	Tech.	Device(s)		Pins	DIP	SM
PRESCALERS						
1.3GHz ÷256 Prescaler	ECL	MC12076	–	8	P	D
	ECL	MC12078	–	8	P	D
2.0GHz ÷32/33, ÷64/65 Dual Modulus Prescaler	ECL	MC12034A	–	8	P	D
	ECL	MC12034B	–	8	P	D
2.0GHz ÷32/33, ÷64/65 Low Voltage Dual Modulus Prescaler	ECL	MC12033A	–	8	P	D
	ECL	MC12033B	–	8	P	D
2.0GHz ÷64/65, ÷128/129 Dual Modulus Prescaler	ECL	MC12032A	–	8	P	D
	ECL	MC12032B	–	8	P	D
2.0GHz ÷64/65, ÷128/129 Low Voltage Dual Modulus Prescaler	ECL	MC12031A	–	8	P	D
	ECL	MC12031B	–	8	P	D
2.0GHz ÷64/65, ÷128/129 Super Low Power Dual Modulus Prescaler	ECL	MC12054A	–	8		D,SD
2.5GHz ÷2, ÷4 Low Power Prescaler With Satnd–By Mode	ECL	MC12095	–	8		D,SD
2.5GHz ÷8192 Prescaler	ECL	MC12098	–	8		D
2.8GHz ÷64/128/256 Prescaler	ECL	MC12079	–	8	P	D
	ECL	MC12089	–	8	P	D
225MHz ÷20/21 Dual Modulus Prescaler	ECL	MC12019	–	8	P,L	D
225MHz ÷32/33 Dual Modulus Prescaler	ECL	MC12015	–	8	P,L	D
225MHz ÷40/41 Dual Modulus Prescaler	ECL	MC12016	–	8	P,L	D
225MHz ÷64 Prescaler	ECL	MC12023	–	8	P	D
225MHz ÷64/65 Dual Modulus Prescaler	ECL	MC12017	–	8	P,L	D
480MHz ÷5/6 Dual Modulus Prescaler	ECL	MC12009	–	16	P,L	
520MHz ÷128/129 Dual Modulus Prescaler	ECL	MC12018	–	8	P,L	D
520MHz ÷64/65 Dual Modulus Prescaler	ECL	MC12025	–	8	P	D
550MHz ÷10/11 Dual Modulus Prescaler	ECL	MC12013	–	16	P,L	
550MHz ÷8/9 Dual Modulus Prescaler	ECL	MC12011	–	16	P,L	
750MHz ÷2 UHF Prescaler	ECL	MC12090	–	16	P,L	
PROGRAMMABLE DELAY CHIPS						
Programmable Delay Chip (Dig 80ps Anal. 1.6 Ps/mv)	ECL	MC10E196	MC100E196	28		FN
Programmable Delay Chip (Digitally Selectable 20ps Res)	ECL	MC10E195	MC100E195	28		FN
RAMs						
1024 X 1–Bit Random Access Memory	ECL	MCM10146	–	16	L	
256 X 1–Bit Random Access Memory	ECL	MCM10152	–	16	L	
RECEIVERS						
Differential Receiver	ECL	MC10EL16	MC100EL16	8		D
	ECL	MC100LVEL16	–	8		D
High Speed Triple Line Receiver	ECL	MC10216	–	16	P,L	FN
Low–Voltage Quad Differential Line Receiver	ECL	MC100LVEL17	MC100EL17	20		DW
Quad Bus Receiver	ECL	MC10129	–	16	L	
Quad Line Receiver	ECL	MC10H115	–	16	P,L	FN
	ECL	MC10115	–	16	P,L	FN
	ECL	MC1692	–	16	L	
Quint Differential Line Receiver	ECL	MC10E116	MC100E116	28		FN
	ECL	MC10E416	MC100E416	28		FN

Selection by Function

Description	Tech.	Device(s)		Pins	DIP	SM
RECEIVERS						
Triple Line Receiver	ECL	MC10H116	–	16	P,L	D,FN
	ECL	MC10114	–	16	P,L	FN
	ECL	MC10116	–	16	P,L	FN
REGISTERS						
4 X 4 Multiport Register	CMOS	MC14580B	–	24	P,L	D
Hex Parallel D Register With Enable	TTL	MC74F378	–	16	N	D
REGISTER FILES						
16 X 4–Bit Register File (RAM)	ECL	MC10H145	–	16	P,L	FN
4 X 4 Register File Open Collector	TTL	SN54LS170	SN74LS170	16	N,J	D
4 X 4 Register File With 3–State Outputs	TTL	SN54LS670	SN74LS670	16	N,J	D
64–Bit Register File (RAM)	ECL	MCM10145	–	16	L	
8 X 2 Multiport Register File (RAM)	ECL	MCM10143	–	24	L	
SCHMITT TRIGGERS						
Dual 4–Input NAND Schmitt Trigger	TTL	MC74F13	–	14	N	D
	TTL	SN54LS13	SN74LS13	14	N,J	D
Dual Schmitt Trigger	CMOS	MC14583B	–	16	P	D
Hex Inverter Schmitt Trigger	CMOS	MC74AC14	–	14	N	D
	CMOS	MC74ACT14	–	14	N	D
	TTL	MC74F14	–	14	N	D
	TTL	SN54LS14	SN74LS14	14	N,J	D
Hex Schmitt Trigger	CMOS	MC14106B	–	14	P,L	D
	CMOS	MC14584B	–	14	P,L	D
Hex Schmitt Trigger Inverter	CMOS	MC54HC14A	MC74HC14A	14	N,J	D,DT
	CMOS	MC74VHC14	–	14		D, DT,M
	CMOS	MC54HCT14A	MC74HCT14A	14	N,J	D
Quad 2–Input NAND Gate With Schmitt Trigger Inputs	CMOS	MC54HC132A	MC74HC132A	14	N,J	D
Quad 2–Input NAND Schmitt Trigger	CMOS	MC74AC132	–	14	N	D
	CMOS	MC74ACT132	–	14	N	D
	TTL	MC74F132	–	14	N	D
	CMOS	MC14093B	–	14	P,L	D
Quad 2–Input Schmitt Trigger NAND Gate	TTL	SN54LS132	SN74LS132	14	N,J	D
SCSI BUS TERMINATORS						
9–Bit Switchable Active SCSI–2 Bus Term (110Ω) with Volt Reg	CMOS	MCCS142237	–	16,20		DW, DT
9–Bit Switchable SCSI Bus Term (220Ω & 330Ω: Passive)	CMOS	MCCS142233	–	20		FN
18–Bit Active SCSI Bus Terminator (*Also Available in 32–Pin QFP Package)	CMOS	MCCS142235	–	24,32		DW, *FA
18–Bit Switchable Active SCSI–2 Bus Term (110Ω) with Volt Reg	CMOS	MCCS142236	–	28		DW
18–Bit Switchable Active SCSI–2 Bus Term (110Ω) with Volt Reg Plus Inverted Disconnect	CMOS	MCCS142238	–	28		DW
9–Bit Switchable Active SCSI Bus Terminator (110Ω) with Volt Reg	CMOS	MCCS142239	–	16		D,DW
SERIAL EPROMs						
Serial EPROM for MPA1016: 8–Pin DIP and SOIC; 20–Pin PLCC	CMOS	MPA1765	–	8,20	N	D,FN
Serial EPROM for MPA1036: 8–Pin DIP and SOIC; 20–Pin PLCC	CMOS	MPA17128	–	8,20	P	D,FN
SHIFT REGISTERS						
1–to–64–Bit Variable Length Shift Register	CMOS	MC14557B	–	16	P,L	DW
128–Bit Static Shift Register	CMOS	MC14562B	–	14	P,L	
18–Bit Static Shift Register	CMOS	MC14006B	–	14	P,L	D
3–Bit Scannable Registered Address Driver, ECL	ECL	MC10E212	MC100E212	28		FN

Selection by Function

Description	Tech.	Device(s)		Pins	DIP	SM
SHIFT REGISTERS						
4–Bit Bidirectional Universal Shift Register	CMOS	MC74AC194	–	16	N	D
	CMOS	MC74ACT194	–	16	N	D
	TTL	MC74F194	–	16	N	D
	CMOS	MC74HC194	–	16	N	
	TTL	SN54LS194A	SN74LS194A	16	N,J	D
4–Bit Shift Register	TTL	MC74F195	–	16	N	D
	TTL	SN54LS95B	SN74LS95B	14	N,J	D
	CMOS	MC14035B	–	16	P,L	D
4–Bit Shift Register With 3–State Outputs	TTL	SN74LS395	–	16	N,J	D
4–Bit Shifter With 3–State	CMOS	MC74AC350	–	16	N	D
	CMOS	MC74ACT350	–	16	N	D
4–Bit Shifter, With 3–State Outputs	TTL	MC74F350	–	16	N	D
4–Bit Universal Shift Register	CMOS	MC74HC195	–	16	N	
	ECL	MC10H141	–	16	P,L	FN
	ECL	MC10141	–	16	P,L	FN
	CMOS	MC14194B	–	16	P,L	D
8–Bit Bidirectional Universal Shift Register With parallel I/O	CMOS	MC74HC299	–	20	N	DW
8–Bit Parallel–to–Serial Shift Register	TTL	SN54LS165	SN74LS165	16	N,J	D
8–Bit Scannable Register	ECL	MC10E241	MC100E241	28		FN
8–Bit Serial In–Serial Out Shift Register	TTL	MC74F164	–	14	N	D
8–Bit Serial or Parallel–Input/Serial–Output Shift Register	CMOS	MC54HC165	MC74HC165	16	N,J	D
8–Bit Serial or Parallel–Input/Serial–Output Shift Register With 3–State Outputs	CMOS	MC54HC589	MC74HC589	16	N,J	D
	CMOS	MC54HC589A	MC74HC589A	16	N,J	D,SDT
8–Bit Serial or Parallel–Input/Serial–Output Shift Register With Input Latch	CMOS	MC54HC597	MC74HC597	16	N,J	D
	CMOS	MC54HC597A	MC74HC597A	16	N,J	D,DT
8–Bit Serial–In/Parallel–Out Shift Register	TTL	SN54LS164	SN74LS164	14	N,J	D
8–Bit Serial–Input/Parallel–Output Shift Register	CMOS	MC54HC164	MC74HC164	14	N,J	D
	CMOS	MC54HC164A	MC74HC164A	14	N,J	D,DT
8–Bit Serial–Input/Serial or Parallel–Output Shift Register With Latched 3–State Outputs	CMOS	MC54HC595A	MC74HC595A	16	N,J	D,DT
	CMOS	MC74VHC595	–	16		D, DT,M
8–Bit Shift Register	ECL	MC10E141	MC100E141	28		FN
	TTL	SN54LS166	SN74LS166	16	N,J	D
8–Bit Shift Registers With Sign Extend	TTL	SN54LS322A	SN74LS322A	20	N,J	DW
8–Bit Shift/Storage Register With 3–State Outputs	TTL	SN54LS299	SN74LS299	20	N,J	DW
	TTL	SN54LS323	SN74LS323	20	N,J	DW
8–Bit Static Shift Register	CMOS	MC14014B	–	16	P,L	D
	CMOS	MC14021B	–	16	P,L	D
8–Input Shift/Storage Register W/Synchronous Reset and Common I/O Pins	TTL	MC74F323	–	20	N	DW
8–Input Universal Shift/Storage Register With Common Parallel I/O Pins: With 3–State Outputs	CMOS	MC74AC299	–	20	N	DW
	CMOS	MC74ACT299	–	20	N	DW
8–Input Universal Shift/Storage Register With Syn Reset/Common Parallel I/O Pins: With 3–State Outputs	CMOS	MC74AC323	–	20	N	DW
	CMOS	MC74ACT323	–	20	N	DW
8–Input Universal Shift/Storage Register, W/Common Parallel I/O Pins	TTL	MC74F299	–	20	N	DW
8–Stage Shift/Store Register With 3–State Outputs	CMOS	MC14094B	–	16	P,L	D
9–Bit Shift Register, 700MHz, With Asynchronous Master Reset	ECL	MC10E142	MC100E142	28		FN
Dual 5–Bit Shift Register	CMOS	MC14015B	–	16	P,L	D

Selection by Function

Description	Tech.	Device(s)		Pins	DIP	SM
SHIFT REGISTERS						
Dual 64–Bit Static Shift Register	CMOS	MC14517B	–	16	P	DW
Successive Approximation Register	CMOS	MC14549B	–	16	P,L	DW
	CMOS	MC14559B	–	16	P,L	DW
Universal 4–Bit Shift Register	TTL	SN54LS195A	SN74LS195A	16	N,J	D
SYNTHESIZERS						
1.1GHz Serial Input Synthesizer With ÷64/65, ÷128/129 Prescaler	ECL	MC12202	–	16,20		D,M, DT
125–1000MHz Frequency Synthesizer With Parallel Programming Interface	ECL	MC12181	–	16		DT
2.0GHz Serial Input Synthesizer With ÷64/65, ÷128/129 Prescaler	ECL	MC12206	–	16,20		D,DT
2.5GHz Serial Input Synthesizer With ÷32/33, ÷64/65 Prescaler	ECL	MC12210	–	16,20		D,DT
2.7GHz Frequency Synthesizer	ECL	MC12179	–	8		D
TRANSCEIVERS						
25Ω Octal Bidirectional Transceiver w/ 3–State Inputs and Outputs	ECL	MC74F2245	–	20		DW,SD
4–Bit Differential ECL Bus/TTL Bus Transceiver	ECL	MC10H680	MC100H680	28		FN
Dual Supply Octal Translating Transceiver	CMOS	MC74LVX4245	–	24		DW,DT
ECL/TTL Inverting Bidirectional Transceivers With Latch (4–Bit)	ECL	MC10804	–	16	L	
ECL/TTL Inverting Bidirectional Transceivers With Latch (5–Bit)	ECL	MC10805	–	20	L	
Hex ECL/TTL Transceiver With Latches	ECL	MC10H681	MC100H681	28		FN
Low–Voltage CMOS 16–Bit Latching Transceiver, 3–State, Non–Inverting With 5V Tolerant Inputs and Outputs	CMOS	MC74LCX16543A	–	56		DT
Low–Voltage CMOS 16–Bit Transceiver, 3–State, Non–Inverting With 5V Tolerant Inputs and Outputs	CMOS	MC74LCX16245	–	48		DT
Low–Voltage CMOS 18–Bit Universal Bus Transceiver, 3–State, Non–Inverting With 5V Tolerant Inputs and Outputs	CMOS	MC74LCX16500	–	56		DT
	CMOS	MC74LCX16501	–	56		DT
Low–Voltage CMOS Octal Registered Transceiver With Dual Output and Clock Enables, With 5V Tolerant Inputs and Outputs	CMOS	MC74LCX2952	–	24		DW, SD,DT
Low–Voltage CMOS Octal Transceiver, 3–State, Non–Inverting With 5V Tolerant Inputs and Outputs	CMOS	MC74LCX245	–	20		M,DW, DT
Low–Voltage Quiet CMOS Octal Transceiver, 3–State, Non–Inverting	CMOS	MC74LVQ245	–	20		M,DW, SD,DT
Low–Voltage CMOS Octal Transceiver/Registered Transceiver With 5V Tolerant Inputs and Outputs	CMOS	MC74LCX646	–	24		DW, SD,DT
Low–Voltage CMOS Octal Transceiver/Registered Transceiver With Dual Enable, With 5V Tolerant Inputs and Outputs	CMOS	MC74LCX652	–	24		DW, DT
Low–Voltage Quiet CMOS Octal Transceiver/Registered Transceiver	CMOS	MC74LVQ646	–	24		DW, SD,DT
Low–Voltage Quiet CMOS Octal Transceiver/Registered Transceiver	CMOS	MC74LVQ652	–	24		DW, SD,DT
Octal Bus Transceiver/Inverting With Open Collector	TTL	SN54LS642	SN74LS642	20	N,J	DW
Octal Bus Transceiver/Non–Inverting With Open Collector	TTL	SN54LS641	SN74LS641	20	N,J	DW
Quad Futurebus Backplane Transceiver, With 3–State Outputs and Open Collector	TTL	MC74F3893A	–	20		FN
TRANSLATORS						
9–Bit ECL/TTL Translator	ECL	MC10H601	MC100H601	28		FN
9–Bit Latch ECL/TTL Translator	ECL	MC10H603	MC100H603	28		FN
9–Bit Latch TTL/ECL Translator	ECL	MC10H602	MC100H602	28		FN
9–Bit TTL/ECL Translator	ECL	MC10H600	MC100H600	28		FN
Differential ECL/TTL Translator	ECL	MC10ELT25	MC100ELT25	8		D
Differential PECL/TTL Translator	ECL	MC10ELT21	MC100ELT21	8		D
Dual Differential PECL/TTL Translator	ECL	MC100ELT23	–	8		D
Dual LVTTL/LVCMOS to Differential PECL Translator	ECL	MC100LVELT22	–	8		D
Dual TTL/Differential PECL Translator	ECL	MC10ELT22	MC100ELT22	8		D

Selection by Function

Description	Tech.	Device(s)		Pins	DIP	SM
TRANSLATORS						
ECL/TTL Translator (Single P.S. @+ 5.0V)	ECL	MC10H350	–	16	P,L	FN
Hex ECL/MST Translator	ECL	MC10191	–	16	P,L	
Hex TTL OR CMOS/CMOS Hex Level Shifter	CMOS	MC14504B	–	16	P,L	D
Quad CMOS/ECL Translator (Single P.S. @+ 5.0V)	ECL	MC10H352	–	20	P,L	FN
Quad MECL/TTL Translator	ECL	MC10H125	–	16	P,L	FN
	ECL	MC10125	–	16	P,L	FN
Quad MST/ECL Translator	ECL	MC10190	–	16	P	
Quad TTL/ECL Translator (ECL Strobe)	ECL	MC10H424	–	16	P,L	FN
Quad TTL/MECL Translator	ECL	MC10124	–	16	P,L	FN
Quad TTL/MECL Translator, With TTL Strobe Input	ECL	MC10H124	–	16	P,L	FN
Quad TTL/NMOS–to–PECL Translator (Single P.S. @+ 5.0V)	ECL	MC10H351	–	20	P,L	FN
Registered Hex ECL/TTL Translator	ECL	MC10H605	MC100H605	28		FN
Registered Hex PECL/TTL Translator	ECL	MC10H607	MC100H607	28		FN
Registered Hex TTL/ECL Translator	ECL	MC10H604	MC100H604	28		FN
Registered Hex TTL/PECL Translator	ECL	MC10H606	MC100H606	28		FN
Triple MECL/NMOS Translator	ECL	MC10177	–	16	L	
Triple ECL to PECL Translator	ECL	MC100LVEL90	MC100EL90	20		DW
Triple PECL to LVPECL Translator	ECL	MC100LVEL92	–	20		DW
Triple PECL to ECL Translator	ECL	MC100LVEL91	–	20		DW
TTL/Differential ECL Translator	ECL	MC10ELT24	MC100ELT24	8		D
TTL/Differential PECL Translator	ECL	MC10ELT20	MC100ELT20	8		D
TTL to Differential PECL/Differential PECL to TTL Translator	ECL	MC10ELT28	MC100ELT28	8		D
VCO						
Phase–Locked–Loop With VCO	CMOS	MC74HC4046A	–	16	N	D
Low Power Voltage Controlled Oscillator Buffer	CMOS	MC12147	–	8		D,SD
Low Power Voltage Controlled Oscillator Buffer	CMOS	MC12149	–	8		D,SD

Device Index

Device Index

Device Index

Device Index

Device Index

Device Index

Device Index

Device Index

Device Index

Device Index

Ordering Information
Device Nomenclatures

LS – Low Power Schottky

SN VV WW XXXX Y

Standard Prefix

Temperature Range
- 74 Series (0 to +70°C)
- 54 Series (–55 to +125°C)

Family
- LS = Low Power Schottky

Function Type

Package Type
- N for Plastic (74 Series Only)
- J for Ceramic
- D for 150 mil Plastic SOIC (74 Series Only)
- DW for 300 mil Plastic SOIC (74 Series Only)

FAST

MC VV W XXXX Y

Motorola Circuit Identifier

Temperature Range
- 74 Series (0 to +70°C)

Family
- F = FAST

Function Type

Package Type
- N for Plastic (74 Series Only)
- D for 150 mil Plastic SOIC (74 Series Only)
- DW for 300 mil Plastic SOIC (74 Series Only)
- SD for Plastic SSOP

MECL 10K, MECL 10H/100H

MC WWW XXX YY

Motorola Circuit Identifier

Temperature Range
- 10 = 10K (–30 to +85°C)
- 10H = 10H (0 to +75°C)
- 100H = 100K Compatible (0 to +85°C)

Function Type

Package Type
- P for Plastic
- L for Ceramic
- FN for PLCC

ECLinPS, ECLinPS Lite

MC WWW XXX YYY ZZ

Motorola Circuit Identifier
- MC = Fully Qualified Circuit
- XC = Non Reliability Qualified

Compatibility Identifier
- 10 = 10H Compatible (0 to +85°C)
- 100 = 100K Compatible (0 to +85°C)

ECLinPS Family Identifier
- E = ECLinPS
- EL = ECLinPS Lite
- ELT = ECLinPS Lite Translator
- LVE = Low Voltage ECLinPS
- LVEL = Low Voltage ECLinPS Lite

Function Type
- YYY = 3–Digits for ECLinPS
- YY= 2–Digits for ECLinPS Lite

Package Type
- FN = PLCC
- D = Plastic SOIC
- L = Ceramic DIP
- P = Plastic DIP

Metal Gate 14000 Series CMOS

MC 14XXX YY ZZ

Motorola Circuit Identifier

Function Type

Identifier (per JEDEC Standard)
- B (or Blank)= Buffered Outputs
- UB = Unbuffered Outputs

Package and Temperature Range
- CL for Ceramic –55 to +125°C
- CP for Plastic –55 to +125°C
- D/DW for Small Outline Package (Plastic) –55 to +125°C
- DT for Plastic TSSOP

High–Speed CMOS

MC VV WWW XXXX Y

Motorola Circuit Identifier

Temperature Range
- 74 Series (–55 to +125°C)
- 54 Series (–55 to +125°C)

High–Speed CMOS Specification Identifier
- HC = Buffered High–Speed CMOS
- HCU = Unbuffered High–Speed CMOS*
- HCT = High–Speed CMOS TTL Compatible

***Not Available On All Devices**

Function Type
- XX(X) Same Function and Pin Configuration as LSTTL
- 4XXX Same Function and Pin Configuration as CMOS 14000
- 7XX(X) Variation of LSTTL or CMOS 14000 Device

Package Type
- N for Plastic (74 Series Only)
- J for Ceramic (54 Series Only)
- D for 150 mil Plastic SOIC (74 Series Only)
- DW for 300 mil Plastic SOIC (74 Series Only)
- SD for Plastic SSOP
- DT for Plastic TSSOP

FACT

MC WWWWW XXX YY

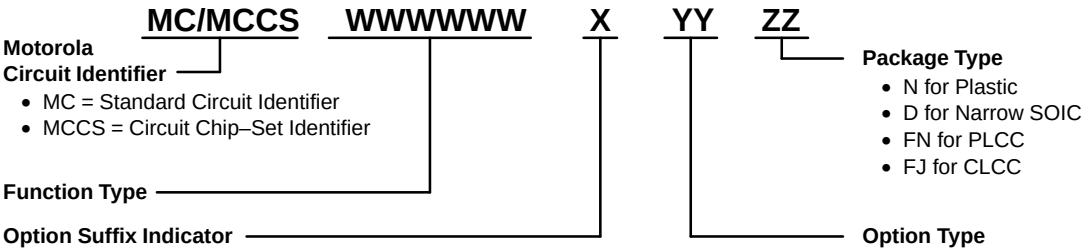
Motorola Circuit Identifier

Temperature Range Family
- 74AC = FACT (–40 to +85°C)
- 74ACT = TTL Compatible (–40 to +85°C)

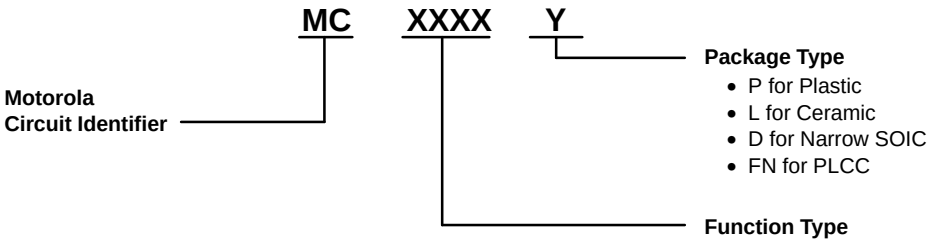
Function Type

Package Type
- N for Plastic
- D for Narrow SOIC
- DW for Wide SOIC
- SD for Plastic SSOP
- DT for Plastic TSSOP

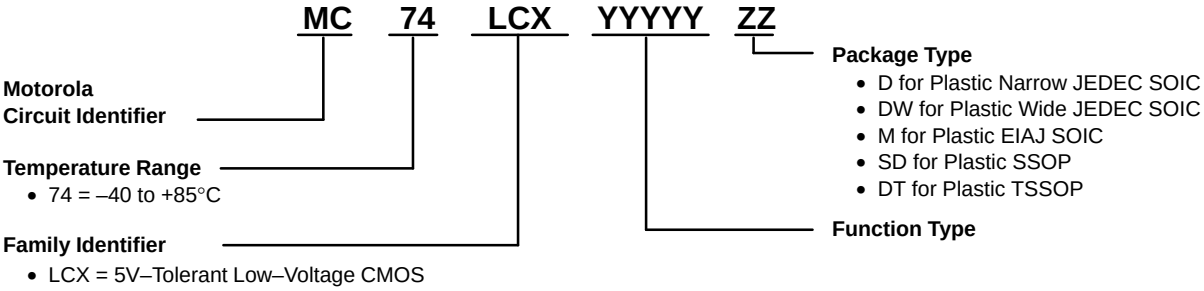
Other Logic Circuits



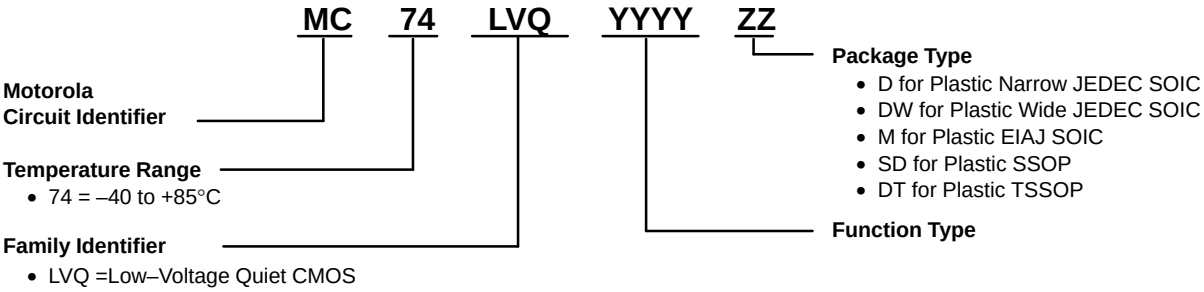
MECL III/HTL/DTL



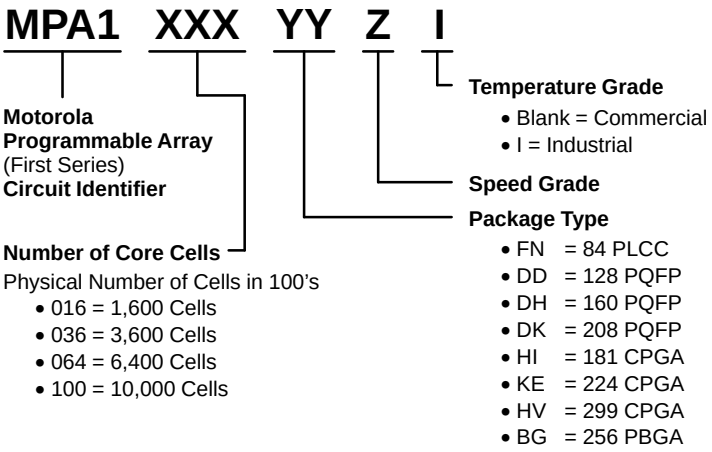
LCX Products



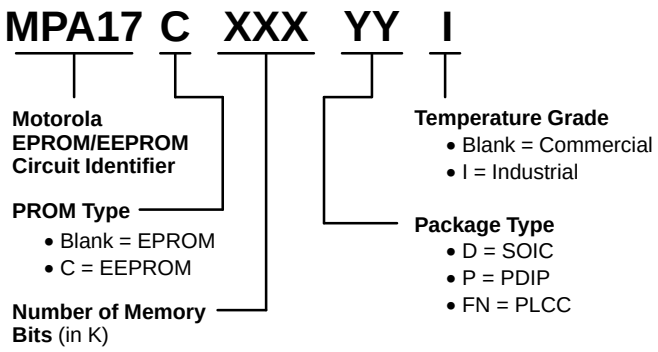
LVQ Products



FPGA Nomenclature



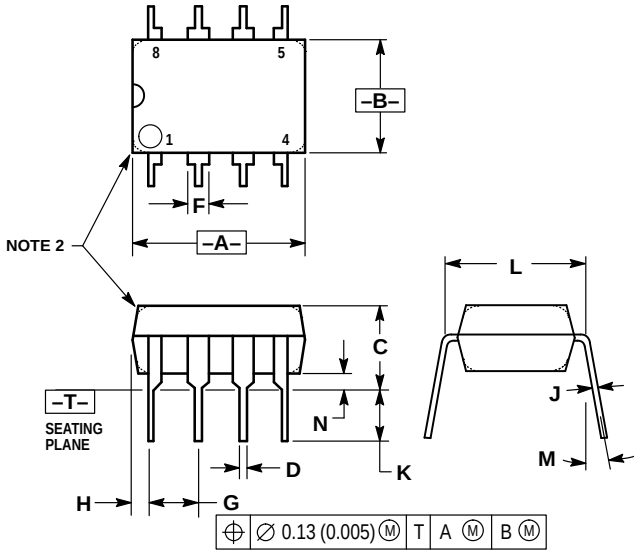
EPROM/EEPROM Nomenclature



Case Outlines

8–Pin Packages

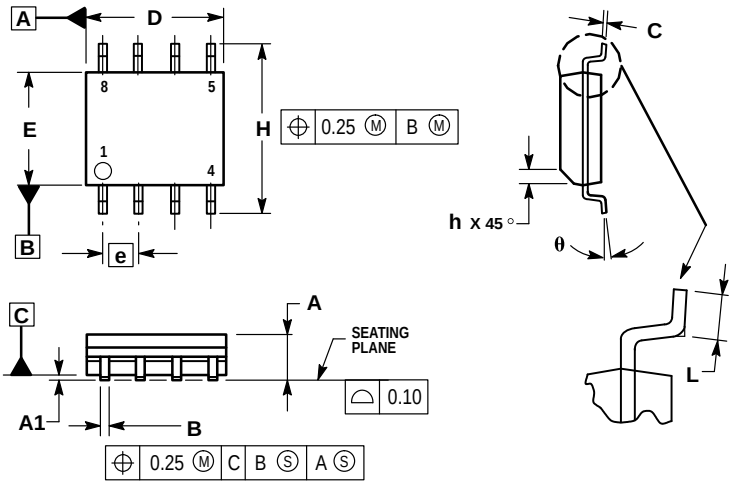
P SUFFIX
PLASTIC DIP PACKAGE
CASE 626–05
ISSUE K



NOTES:
1. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
2. PACKAGE CONTOUR OPTIONAL (ROUND OR SQUARE CORNERS).
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.40	10.16	0.370	0.400
B	6.10	6.60	0.240	0.260
C	3.94	4.45	0.155	0.175
D	0.38	0.51	0.015	0.020
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	0.76	1.27	0.030	0.050
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	—	10°	—	10°
N	0.76	1.01	0.030	0.040

D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751–05
ISSUE S

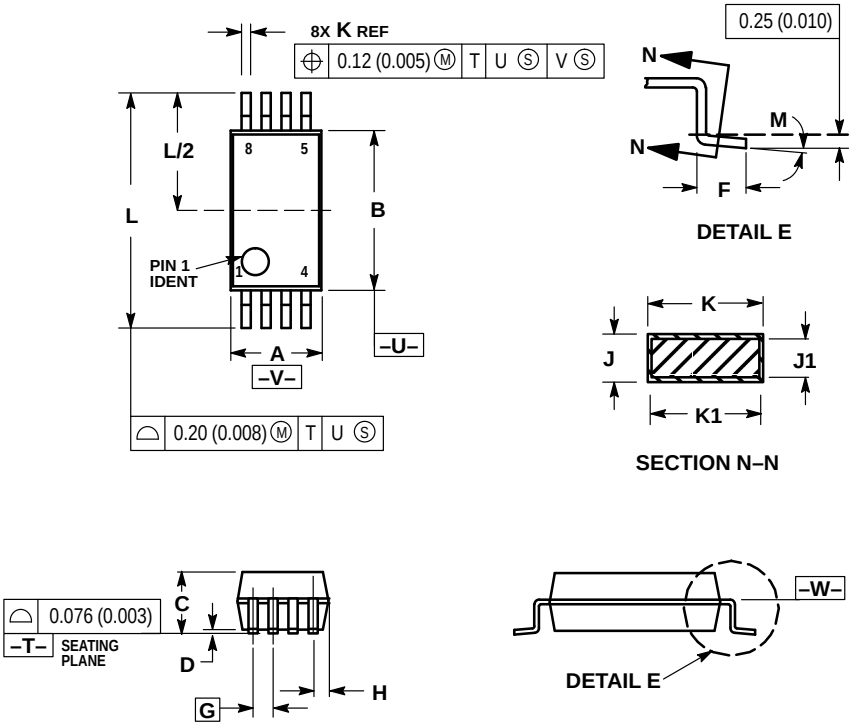


NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS ARE IN MILLIMETERS.
3. DIMENSION D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS	
DIM	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
B	0.35	0.49
C	0.18	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.25
θ	0°	7°

8–Pin Packages

SD SUFFIX
PLASTIC SSOP PACKAGE
CASE 940–03
ISSUE B

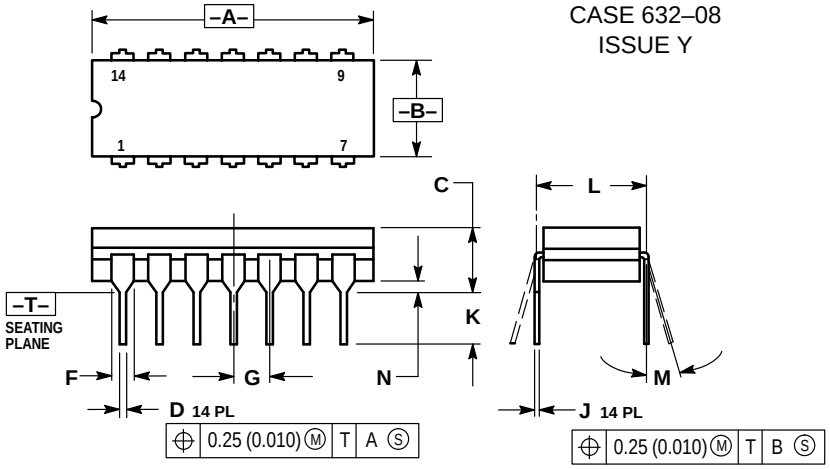


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF K DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR INTRUSION SHALL NOT REDUCE DIMENSION K BY MORE THAN 0.07 (0.002) AT LEAST MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	2.87	3.13	0.113	0.123
B	5.20	5.38	0.205	0.212
C	1.73	1.99	0.068	0.078
D	0.05	0.21	0.002	0.008
F	0.63	0.95	0.024	0.037
G	0.65 BSC		0.026 BSC	
H	0.44	0.60	0.017	0.023
J	0.09	0.20	0.003	0.008
J1	0.09	0.16	0.003	0.006
K	0.25	0.38	0.010	0.015
K1	0.25	0.33	0.010	0.013
L	7.65	7.90	0.301	0.311
M	0 °	8 °	0 °	8 °

14–Pin Packages

L,J SUFFIX
CERAMIC DIP PACKAGE
CASE 632–08
ISSUE Y

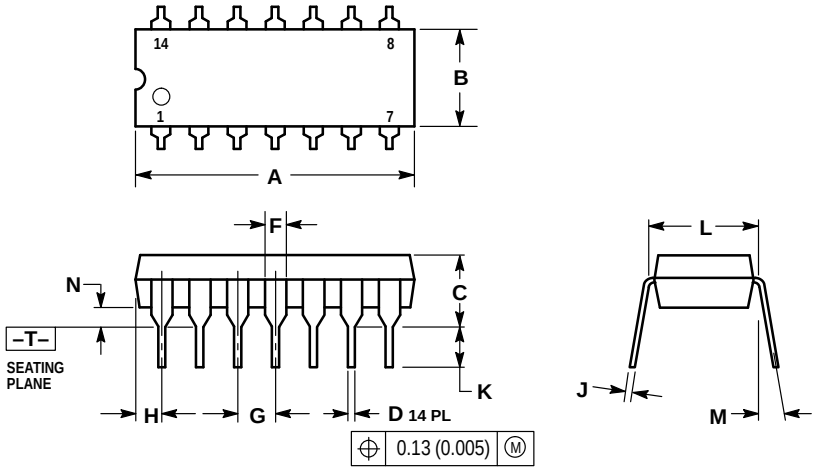


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.750	0.785	19.05	19.94
B	0.245	0.280	6.23	7.11
C	0.155	0.200	3.94	5.08
D	0.015	0.020	0.39	0.50
F	0.055	0.065	1.40	1.65
G	0.100 BSC		2.54 BSC	
J	0.008	0.015	0.21	0.38
K	0.125	0.170	3.18	4.31
L	0.300 BSC		7.62 BSC	
M	0 °	15 °	0 °	15 °
N	0.020	0.040	0.51	1.01

14–Pin Packages

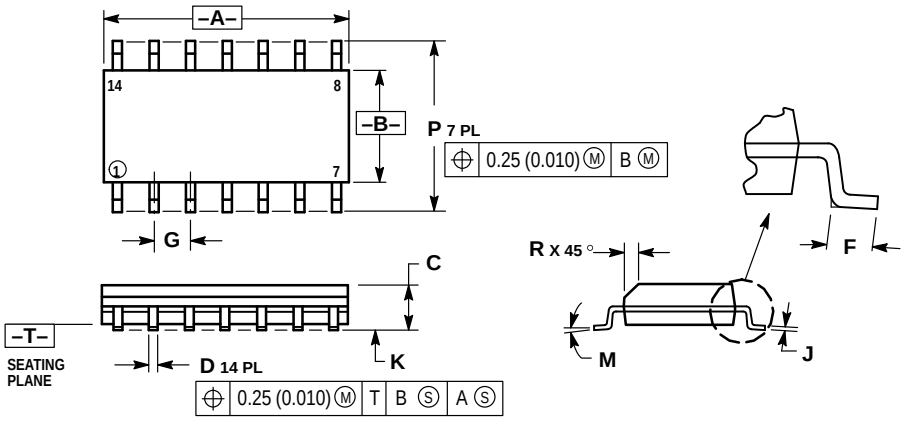
P,N SUFFIX
PLASTIC DIP PACKAGE
CASE 646–06
ISSUE M



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.715	0.770	18.16	18.80
B	0.240	0.260	6.10	6.60
C	0.145	0.185	3.69	4.69
D	0.015	0.021	0.38	0.53
F	0.040	0.070	1.02	1.78
G	0.100 BSC		2.54 BSC	
H	0.052	0.095	1.32	2.41
J	0.008	0.015	0.20	0.38
K	0.115	0.135	2.92	3.43
L	0.290	0.310	7.37	7.87
M	—	10°	—	10°
N	0.015	0.039	0.38	1.01

D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751A–03
ISSUE F

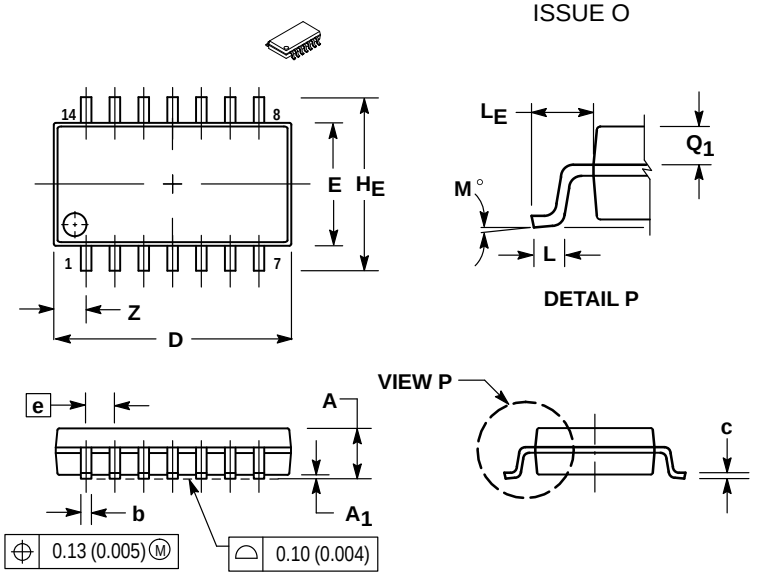


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0 °	7 °	0 °	7 °
P	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

14–Pin Packages

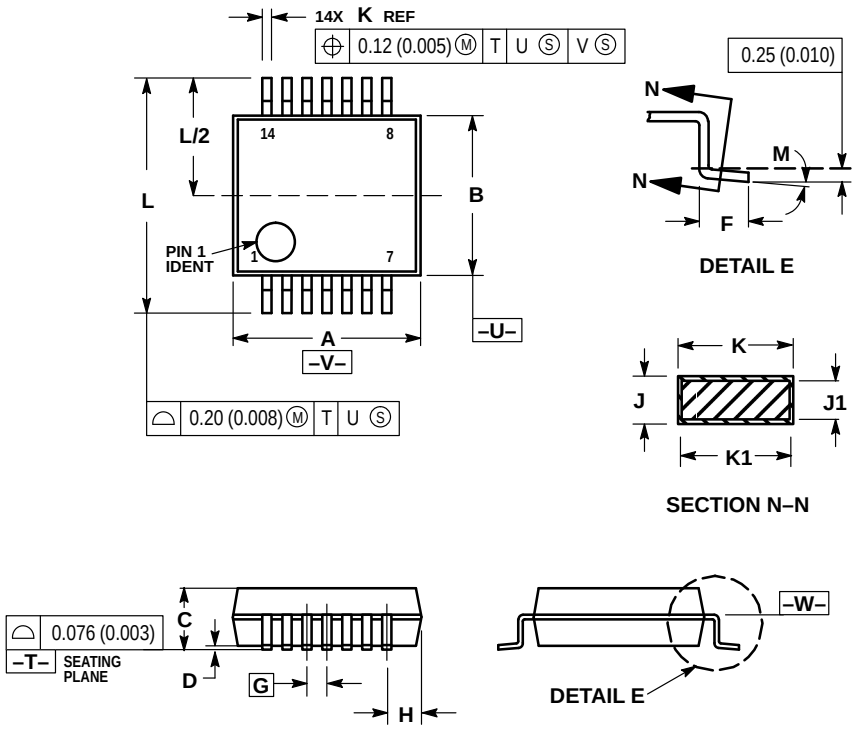
M SUFFIX
PLASTIC SOIC EIAJ PACKAGE
CASE 965–01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	—	2.05	—	0.081
A_1	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.18	0.27	0.007	0.011
D	9.90	10.50	0.390	0.413
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
H_E	7.40	8.20	0.291	0.323
0.50	0.50	0.85	0.020	0.033
L_E	1.10	1.50	0.043	0.059
M	0 °	10 °	0 °	10 °
Q_1	0.70	0.90	0.028	0.035
Z	—	1.42	—	0.056

SD SUFFIX
PLASTIC SSOP PACKAGE
CASE 940A–03
ISSUE B

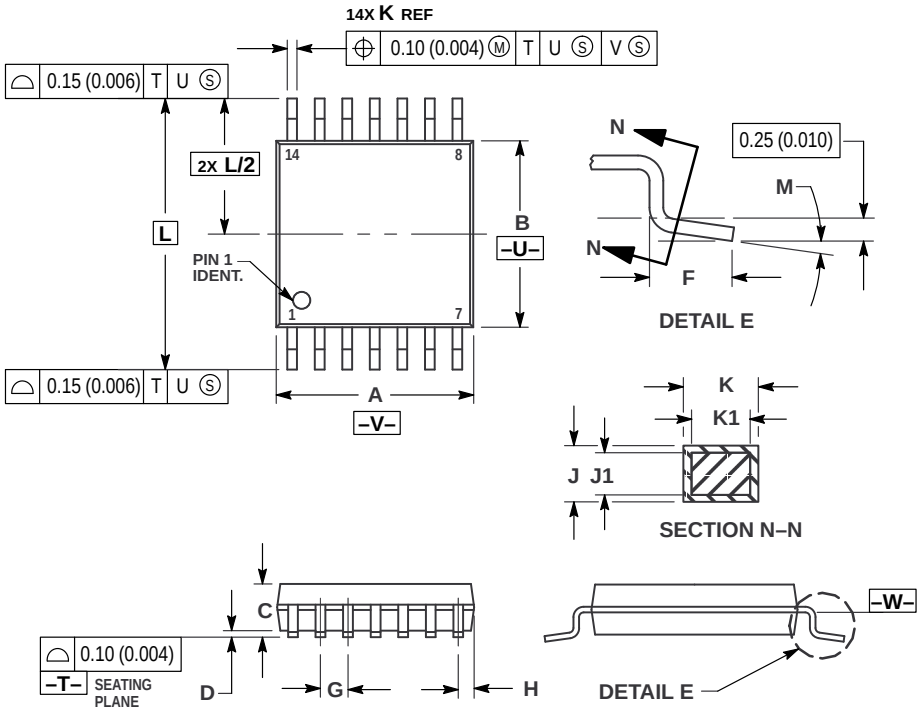


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF K DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR INTRUSION SHALL NOT REDUCE DIMENSION K BY MORE THAN 0.07 (0.002) AT LEAST MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	6.07	6.33	0.238	0.249
B	5.20	5.38	0.205	0.212
C	1.73	1.99	0.068	0.078
D	0.05	0.21	0.002	0.008
F	0.63	0.95	0.024	0.037
G	0.65 BSC		0.026 BSC	
H	1.08	1.22	0.042	0.048
J	0.09	0.20	0.003	0.008
J1	0.09	0.16	0.003	0.006
K	0.25	0.38	0.010	0.015
K1	0.25	0.33	0.010	0.013
L	7.65	7.90	0.301	0.311
M	0 °	8 °	0 °	8 °

14–Pin Packages

DT SUFFIX
PLASTIC TSSOP PACKAGE
CASE 948G–01
ISSUE O

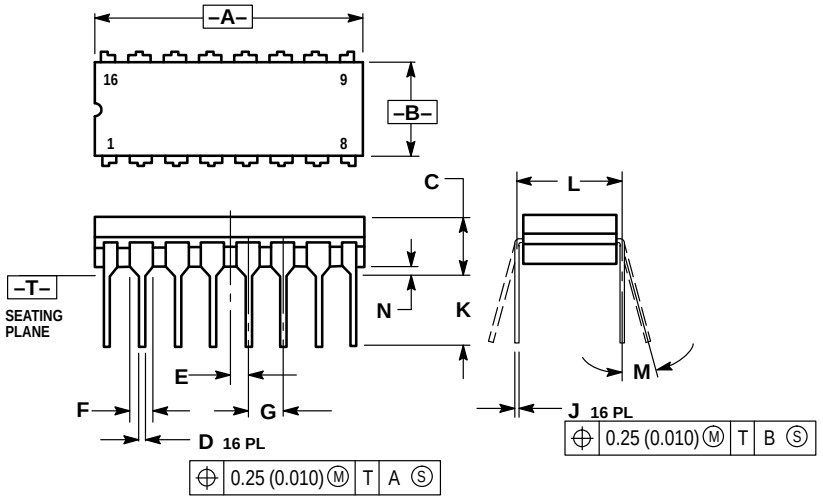


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	—	1.20	—	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

16–Pin Packages

L,J SUFFIX
CERAMIC DIP PACKAGE
CASE 620–10
ISSUE V

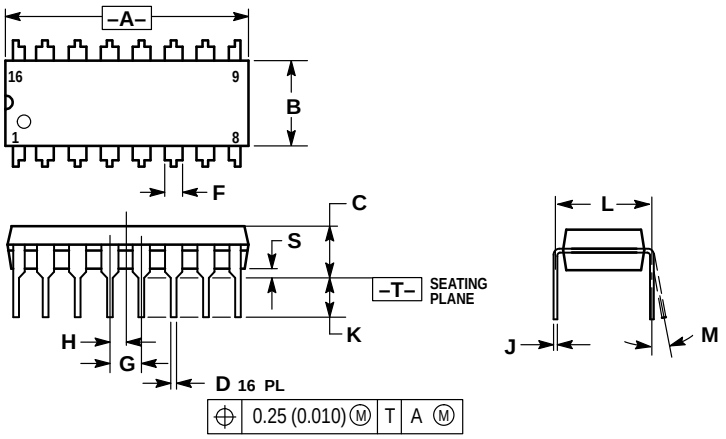


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.750	0.785	19.05	19.93
B	0.240	0.295	6.10	7.49
C	—	0.200	—	5.08
D	0.015	0.020	0.39	0.50
E	0.050 BSC		1.27 BSC	
F	0.055	0.065	1.40	1.65
G	0.100 BSC		2.54 BSC	
H	0.008	0.015	0.21	0.38
K	0.125	0.170	3.18	4.31
L	0.300 BSC		7.62 BSC	
M	0 °	15 °	0 °	15 °
N	0.020	0.040	0.51	1.01

16–Pin Packages

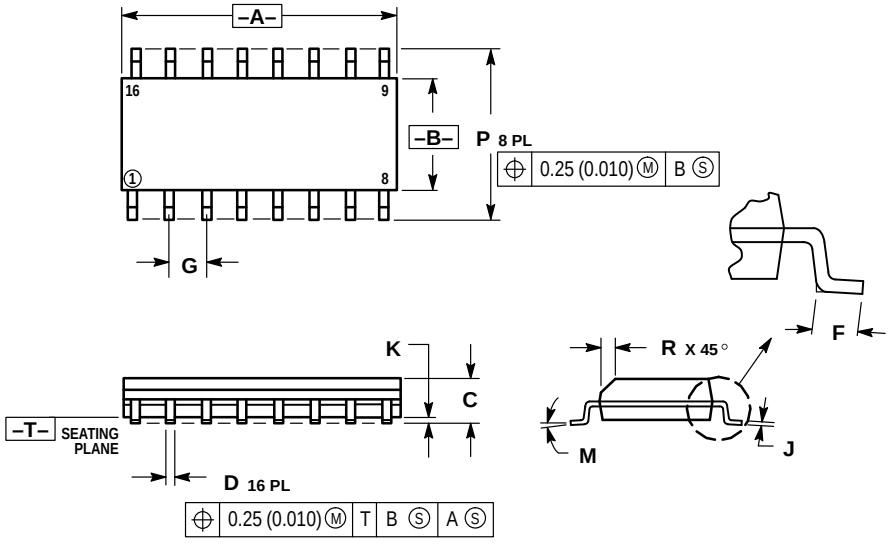
P,N SUFFIX
PLASTIC DIP PACKAGE
CASE 648–08
ISSUE R



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0 °	10 °	0 °	10 °
S	0.020	0.040	0.51	1.01

D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751B–05
ISSUE J

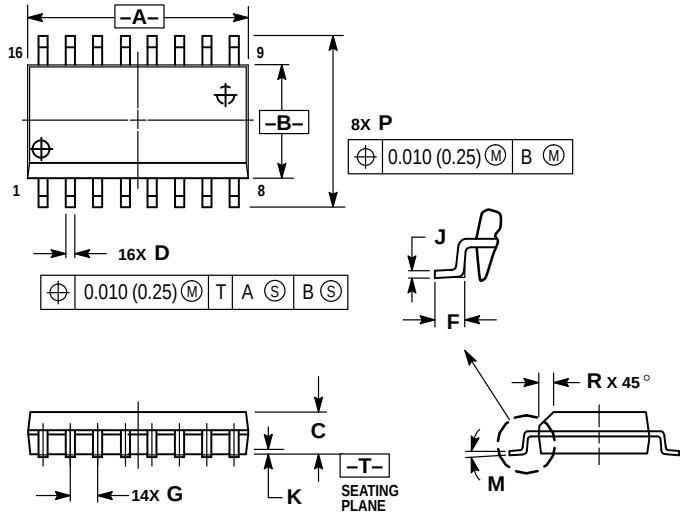


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0 °	7 °	0 °	7 °
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

16–Pin Packages

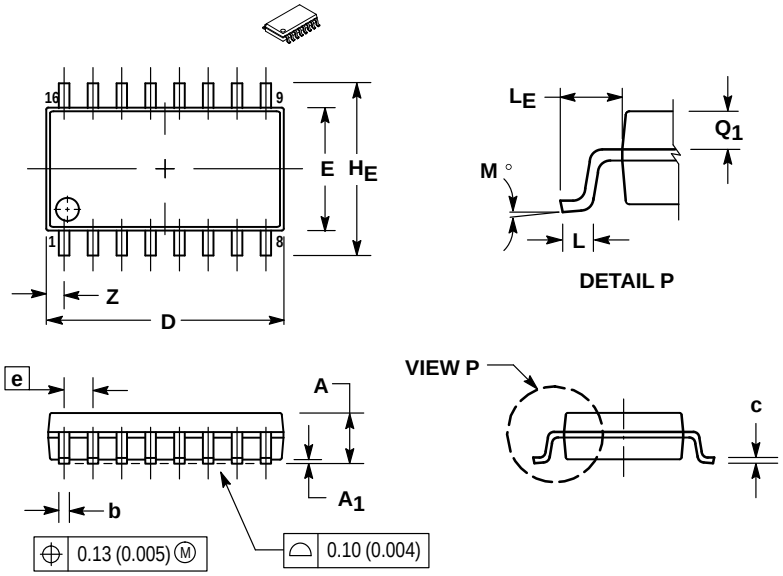
DW SUFFIX
PLASTIC WIDE SOIC PACKAGE
CASE 751G–02
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSIOM D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	10.15	10.45	0.400	0.411
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0 °	7 °	0 °	7 °
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

M SUFFIX
PLASTIC SOIC EIAJ PACKAGE
CASE 966–01
ISSUE O

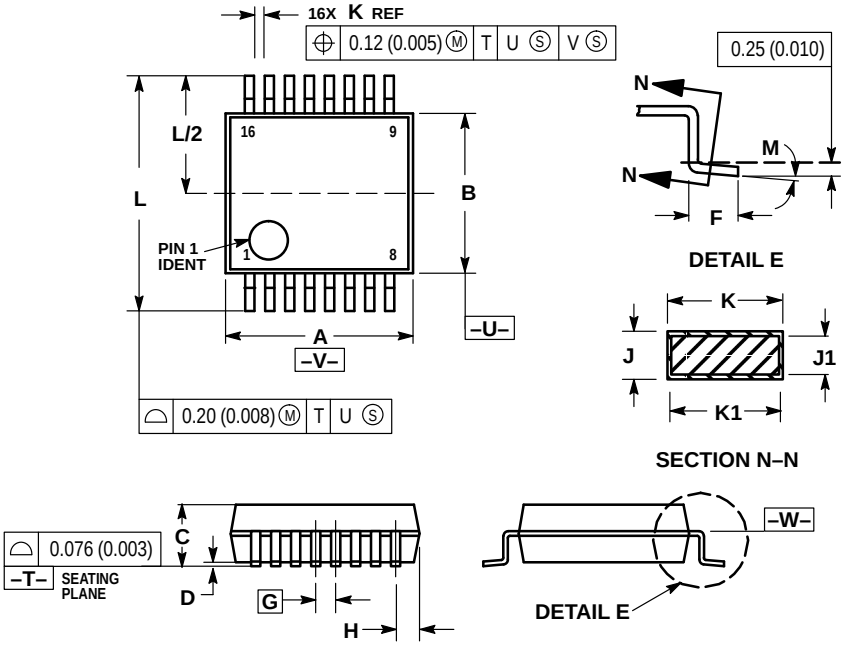


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	—	2.05	—	0.081
A_1	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.18	0.27	0.007	0.011
D	9.90	10.50	0.390	0.413
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
H_E	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
L_E	1.10	1.50	0.043	0.059
M	0 °	10 °	0 °	10 °
Q_1	0.70	0.90	0.028	0.035
Z	—	0.78	—	0.031

16–Pin Packages

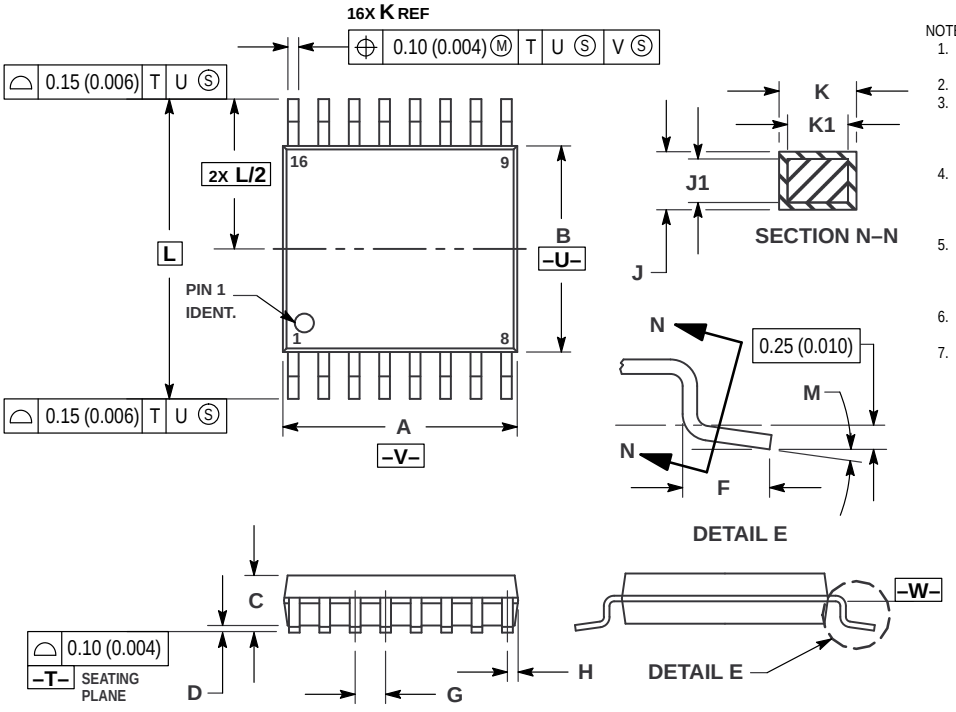
SD SUFFIX
PLASTIC SSOP PACKAGE
CASE 940B–03
ISSUE B



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF K DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR INTRUSION SHALL NOT REDUCE DIMENSION K BY MORE THAN 0.07 (0.002) AT LEAST MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	6.07	6.33	0.238	0.249
B	5.20	5.38	0.205	0.212
C	1.73	1.99	0.068	0.078
D	0.05	0.21	0.002	0.008
F	0.63	0.95	0.024	0.037
G	0.65 BSC		0.026 BSC	
H	0.73	0.90	0.028	0.035
J	0.09	0.20	0.003	0.008
J1	0.09	0.16	0.003	0.006
K	0.25	0.38	0.010	0.015
K1	0.25	0.33	0.010	0.013
L	7.65	7.90	0.301	0.311
M	0 °	8 °	0 °	8 °

DT SUFFIX
PLASTIC TSSOP PACKAGE
CASE 948F–01
ISSUE O

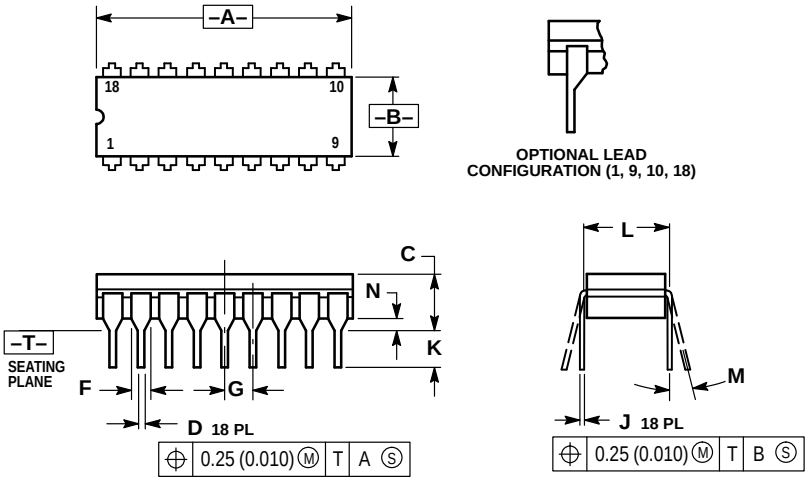


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	—	1.20	—	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

18–Pin Packages

L,J SUFFIX
CERAMIC DIP PACKAGE
CASE 726–04
ISSUE G

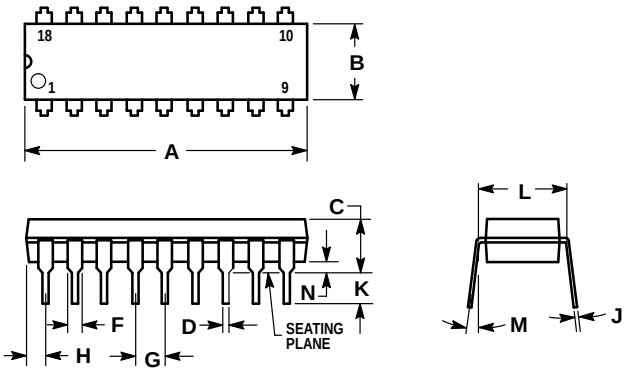


OPTIONAL LEAD CONFIGURATION (1, 9, 10, 18)

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION F FOR FULL LEADS. HALF LEADS OPTIONAL AT LEAD POSITIONS 1, 9, 10, AND 18.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.880	0.910	22.35	23.11
B	0.240	0.295	6.10	7.49
C	—	0.200	—	5.08
D	0.015	0.021	0.38	0.53
F	0.055	0.070	1.40	1.78
G	0.100 BSC		2.54 BSC	
J	0.008	0.012	0.20	0.30
K	0.125	0.170	3.18	4.32
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.02

P,N SUFFIX
PLASTIC DIP PACKAGE
CASE 707–02
ISSUE C

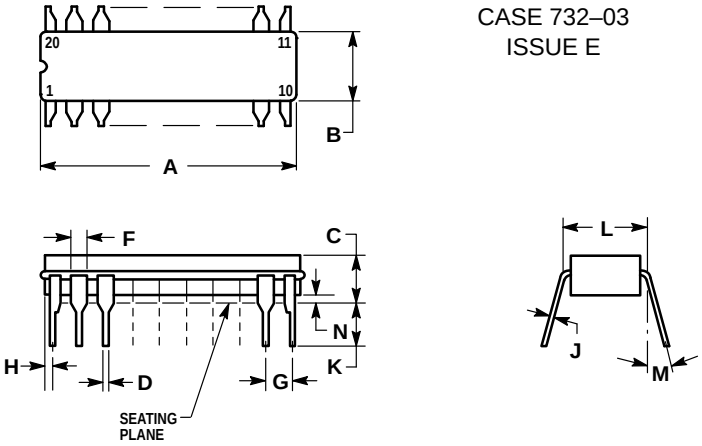


NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	22.22	23.24	0.875	0.915
B	6.10	6.60	0.240	0.260
C	3.56	4.57	0.140	0.180
D	0.36	0.56	0.014	0.022
F	1.27	1.78	0.050	0.070
G	2.54 BSC		0.100 BSC	
H	1.02	1.52	0.040	0.060
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

20–Pin Packages

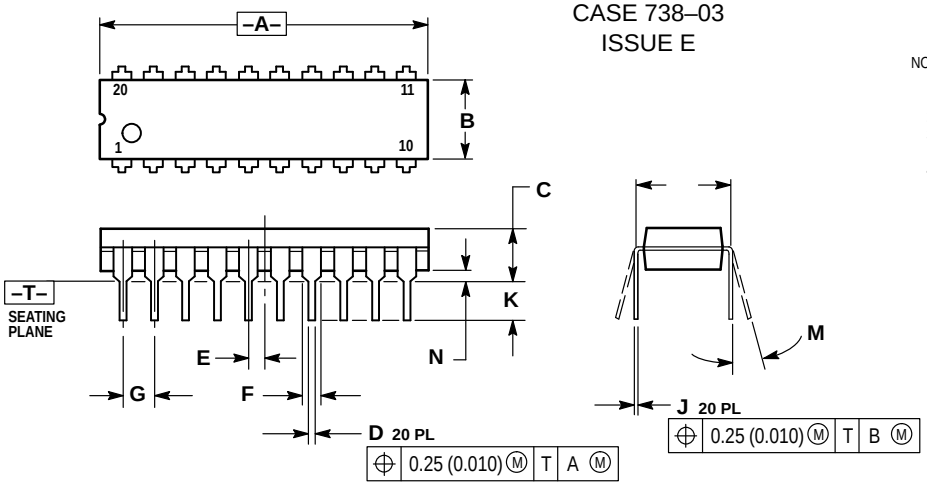
L,J SUFFIX
CERAMIC DIP PACKAGE
CASE 732–03
ISSUE E



NOTES:
1. LEADS WITHIN 0.25 (0.010) DIAMETER, TRUE POSITION AT SEATING PLANE, AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSIONS A AND B INCLUDE MENISCUS.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	23.88	25.15	0.940	0.990
B	6.60	7.49	0.260	0.295
C	3.81	5.08	0.150	0.200
D	0.38	0.56	0.015	0.022
F	1.40	1.65	0.055	0.065
G	2.54 BSC		0.100 BSC	
H	0.51	1.27	0.020	0.050
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.25	1.02	0.010	0.040

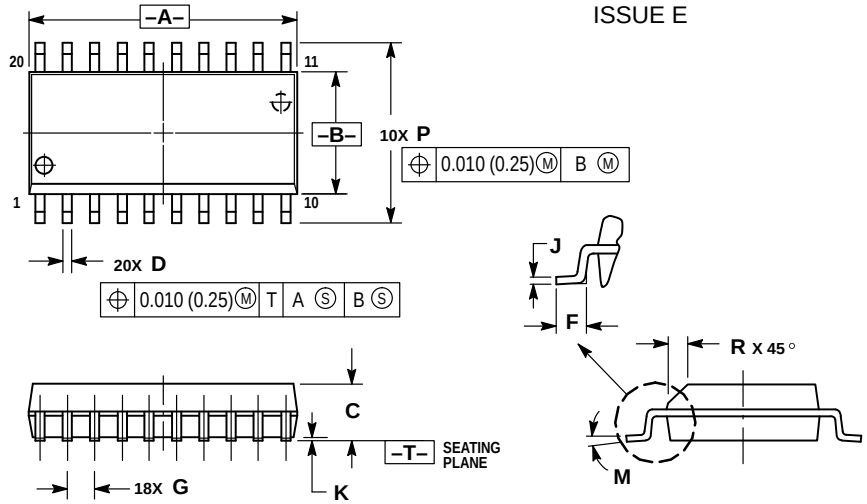
P,N SUFFIX
PLASTICC DIP PACKAGE
CASE 738–03
ISSUE E



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.010	1.070	25.66	27.17
B	0.240	0.260	6.10	6.60
C	0.150	0.180	3.81	4.57
D	0.015	0.022	0.39	0.55
E	0.050 BSC		1.27 BSC	
F	0.050	0.070	1.27	1.77
G	0.100 BSC		2.54 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.140	2.80	3.55
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

DW SUFFIX
PLASTIC WIDE SOIC PACKAGE
CASE 751D–04
ISSUE E

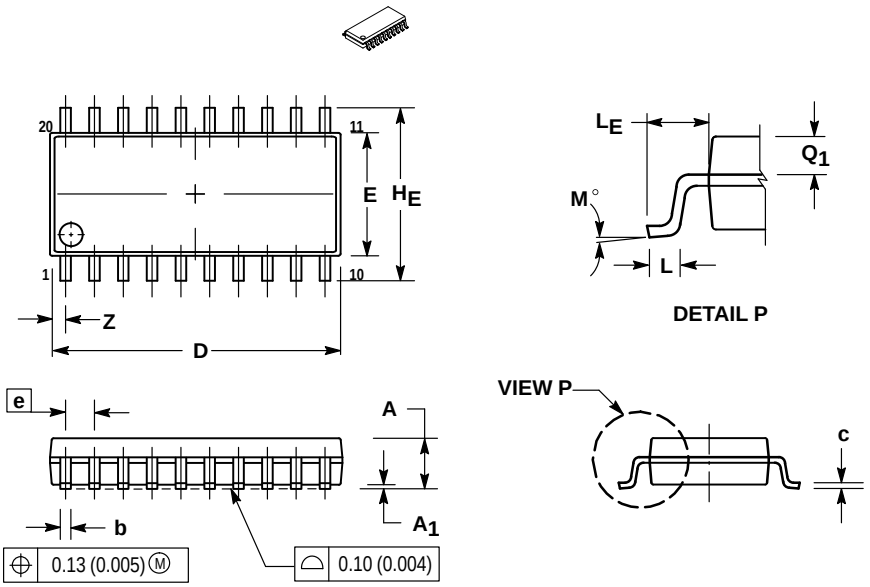


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.150 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	12.65	12.95	0.499	0.510
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

20–Pin Packages

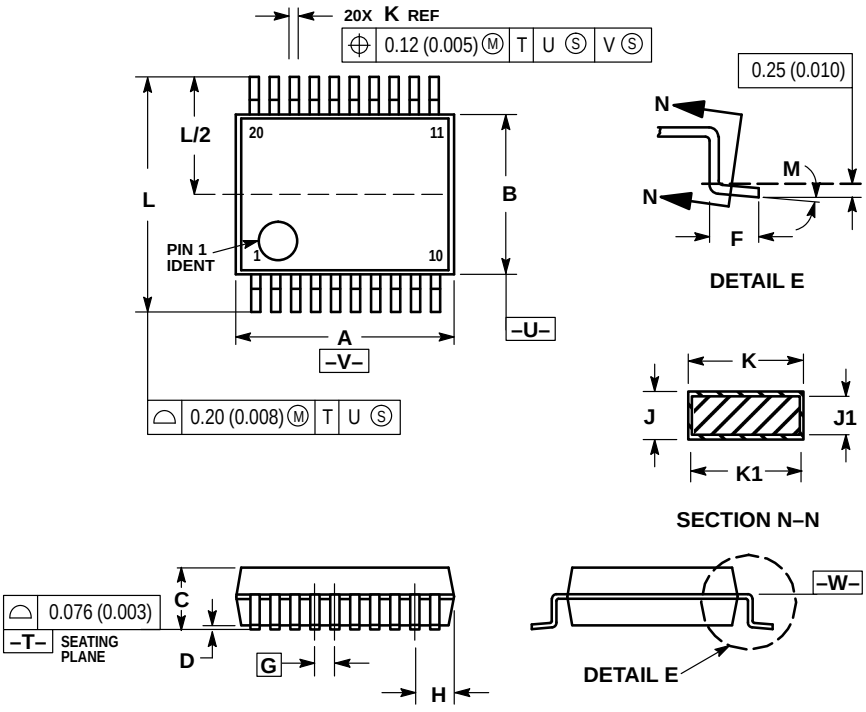
M SUFFIX
PLASTIC SOIC EIAJ PACKAGE
CASE 967–01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	—	2.05	—	0.081
A_1	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.18	0.27	0.007	0.011
D	12.35	12.80	0.486	0.504
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
H_E	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
L_E	1.10	1.50	0.043	0.059
M	0 °	10 °	0 °	10 °
Q_1	0.70	0.90	0.028	0.035
Z	—	0.81	—	0.032

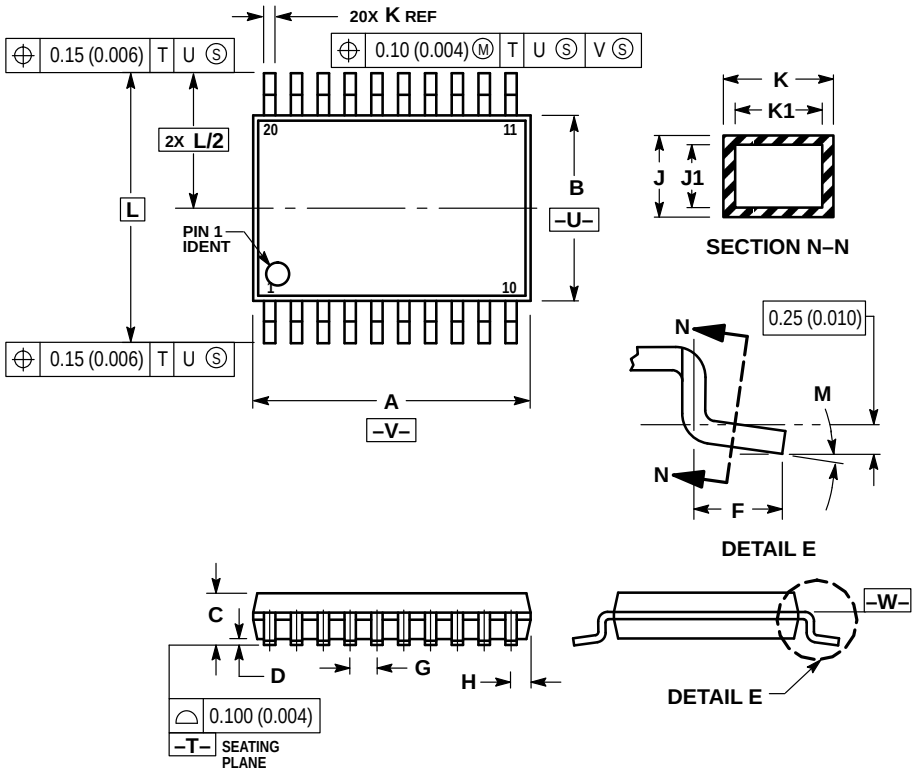
SD SUFFIX
PLASTIC SSOP PACKAGE
CASE 940C–03
ISSUE B



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF K DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR INTRUSION SHALL NOT REDUCE DIMENSION K BY MORE THAN 0.07 (0.002) AT LEAST MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	7.07	7.33	0.278	0.288
B	5.20	5.38	0.205	0.212
C	1.73	1.99	0.068	0.078
D	0.05	0.21	0.002	0.008
F	0.63	0.95	0.024	0.037
G	0.65 BSC		0.026 BSC	
H	0.59	0.75	0.023	0.030
J	0.09	0.20	0.003	0.008
J1	0.09	0.16	0.003	0.006
K	0.25	0.38	0.010	0.015
K1	0.25	0.33	0.010	0.013
L	7.65	7.90	0.301	0.311
M	0 °	8 °	0 °	8 °

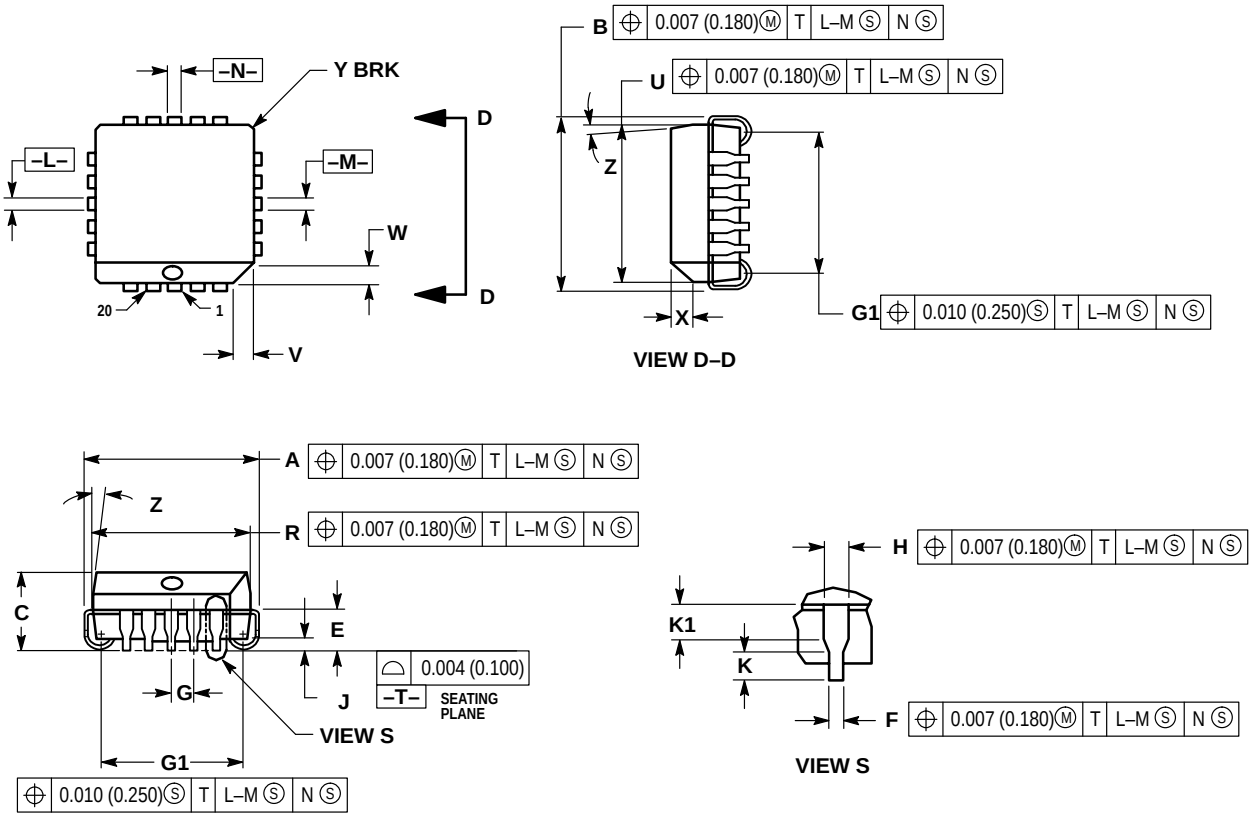
DT SUFFIX
PLASTIC TSSOP PACKAGE
CASE 948E–02
ISSUE A

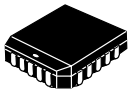


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	6.40	6.60	0.252	0.260
B	4.30	4.50	0.169	0.177
C	—	1.20	—	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

FN SUFFIX
PLASTIC PLCC PACKAGE
CASE 775–02
ISSUE C



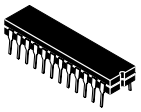


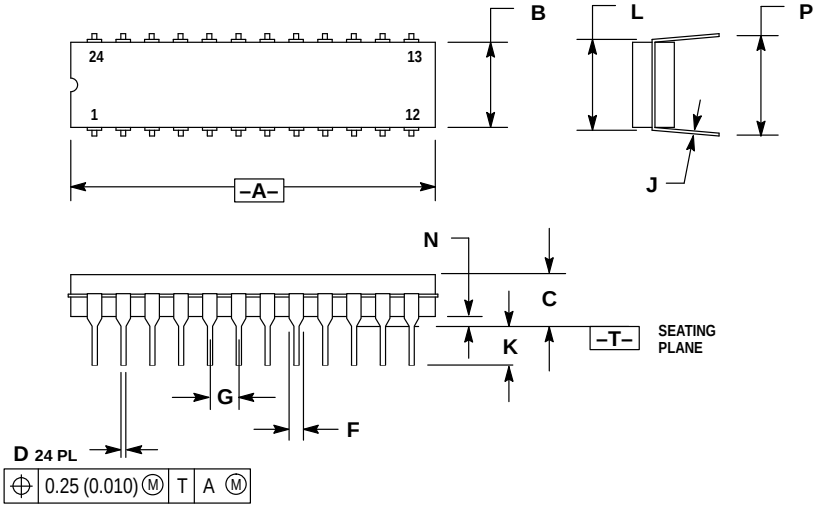
NOTES:
1. DATUMS –L–, –M–, AND –N– DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
2. DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM –T–, SEATING PLANE.
3. DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.
6. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
7. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.385	0.395	9.78	10.03
B	0.385	0.395	9.78	10.03
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	—	0.51	—
K	0.025	—	0.64	—
R	0.350	0.356	8.89	9.04
U	0.350	0.356	8.89	9.04
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	—	0.020	—	0.50
Z	2 °	10 °	2 °	10 °
G1	0.310	0.330	7.88	8.38
K1	0.040	—	1.02	—

24–Pin Packages

J SUFFIX
CERAMIC DIP PACKAGE
CASE 758–02
ISSUE A

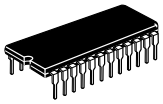


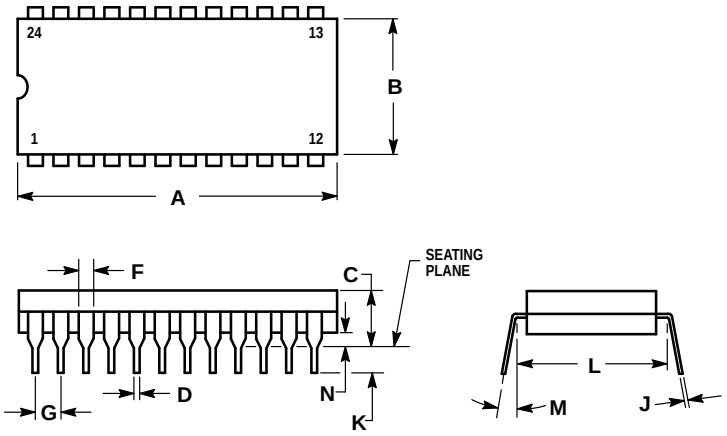


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.240	1.285	31.50	32.64
B	0.285	0.305	7.24	7.75
C	0.160	0.200	4.07	5.08
D	0.015	0.021	0.38	0.53
F	0.045	0.062	1.14	1.57
G	0.100 BSC		2.54 BSC	
J	0.008	0.013	0.20	0.33
K	0.100	0.165	2.54	4.19
L	0.300	0.310	7.62	7.87
N	0.020	0.050	0.51	1.27
P	0.360	0.400	9.14	10.16

L,J,JW SUFFIX
CERAMIC DIP PACKAGE
CASE 623–05
ISSUE M



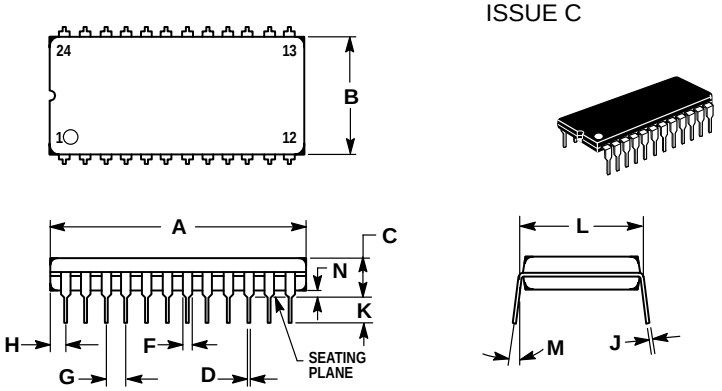


NOTES:
1. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
2. LEADS WITHIN 0.13 (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION (WHEN FORMED PARALLEL).

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	31.24	32.77	1.230	1.290
B	12.70	15.49	0.500	0.610
C	4.06	5.59	0.160	0.220
D	0.41	0.51	0.016	0.020
F	1.27	1.52	0.050	0.060
G	2.54 BSC		0.100 BSC	
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	15.24 BSC		0.600 BSC	
M	0 °	15 °	0 °	15 °
N	0.51	1.27	0.020	0.050

24–Pin Packages

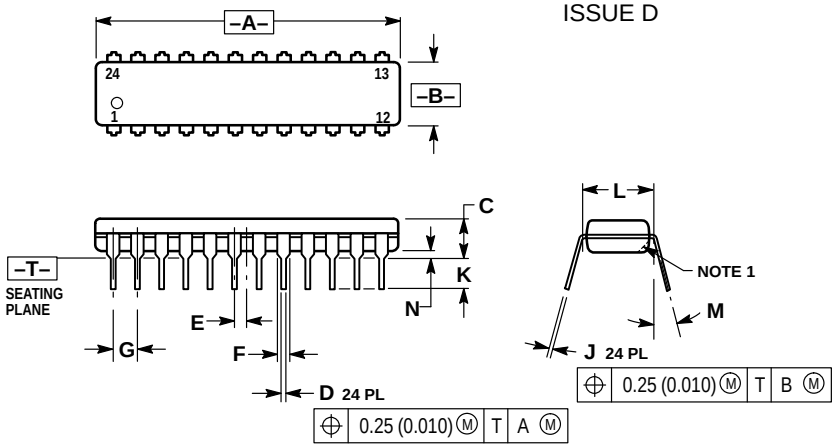
N SUFFIX
PLASTIC DIP PACKAGE
CASE 709–02
ISSUE C



NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	31.37	32.13	1.235	1.265
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.03	0.065	0.080
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24 BSC		0.600 BSC	
M	0 °	15 °	0 °	15 °
N	0.51	1.02	0.020	0.040

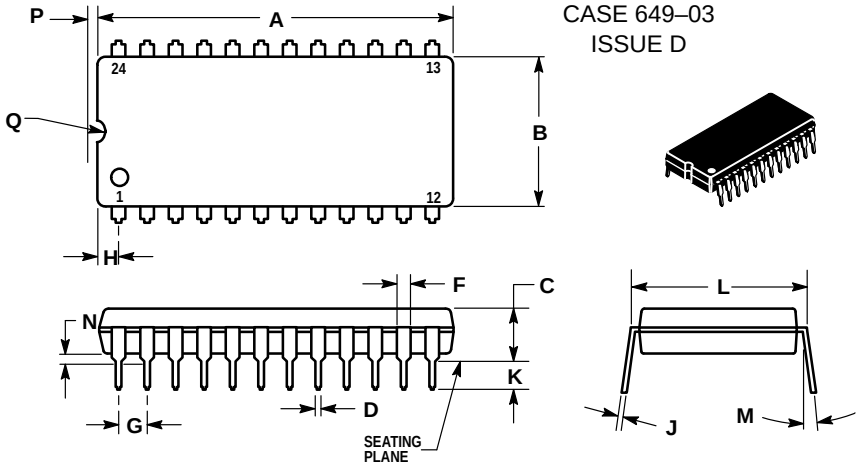
P,N SUFFIX
PLASTIC DIP PACKAGE
CASE 724–03
ISSUE D



NOTES:
1. CHAMFERED CONTOUR OPTIONAL.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
4. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.230	1.265	31.25	32.13
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.020	0.38	0.51
E	0.050 BSC		1.27 BSC	
F	0.040	0.060	1.02	1.52
G	0.100 BSC		2.54 BSC	
J	0.007	0.012	0.18	0.30
K	0.110	0.140	2.80	3.55
L	0.300 BSC		7.62 BSC	
M	0 °	15 °	0 °	15 °
N	0.020	0.040	0.51	1.01

P,N,PW SUFFIX
PLASTIC DIP PACKAGE
CASE 649–03
ISSUE D

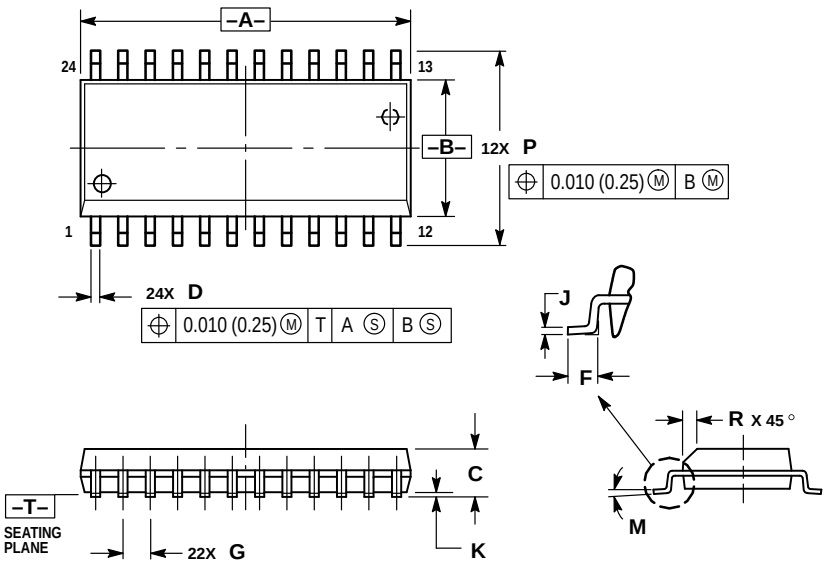


NOTES:
1. LEADS WITHIN 0.13 (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	31.50	32.13	1.240	1.265
B	13.21	13.72	0.520	0.540
C	4.70	5.21	0.185	0.205
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	14.99	15.49	0.590	0.610
M	—	10	—	10 °
N	0.51	1.02	0.020	0.040
P	0.13	0.38	0.005	0.015
Q	0.51	0.76	0.020	0.030

24–Pin Packages

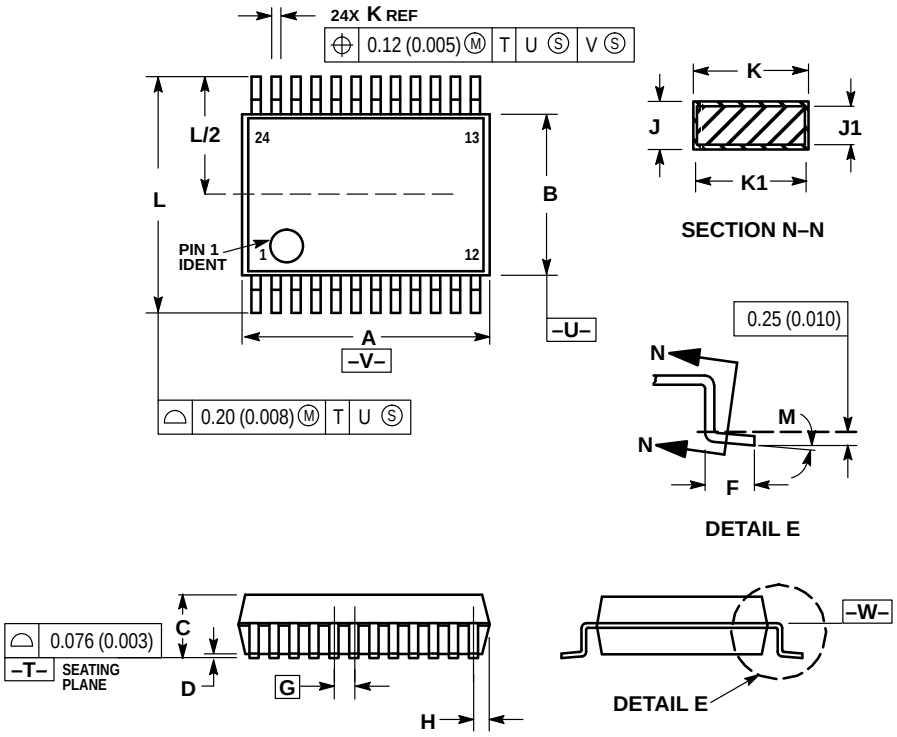
DW SUFFIX
PLASTIC WIDE SOIC PACKAGE
CASE 751E–04
ISSUE E



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	15.25	15.54	0.601	0.612
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.41	0.90	0.016	0.035
G	1.27 BSC		0.050 BSC	
J	0.23	0.32	0.009	0.013
K	0.13	0.29	0.005	0.011
M	0 °	8 °	0 °	8 °
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

SD SUFFIX
PLASTIC SSOP PACKAGE
CASE 940D–03
ISSUE B

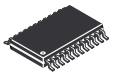


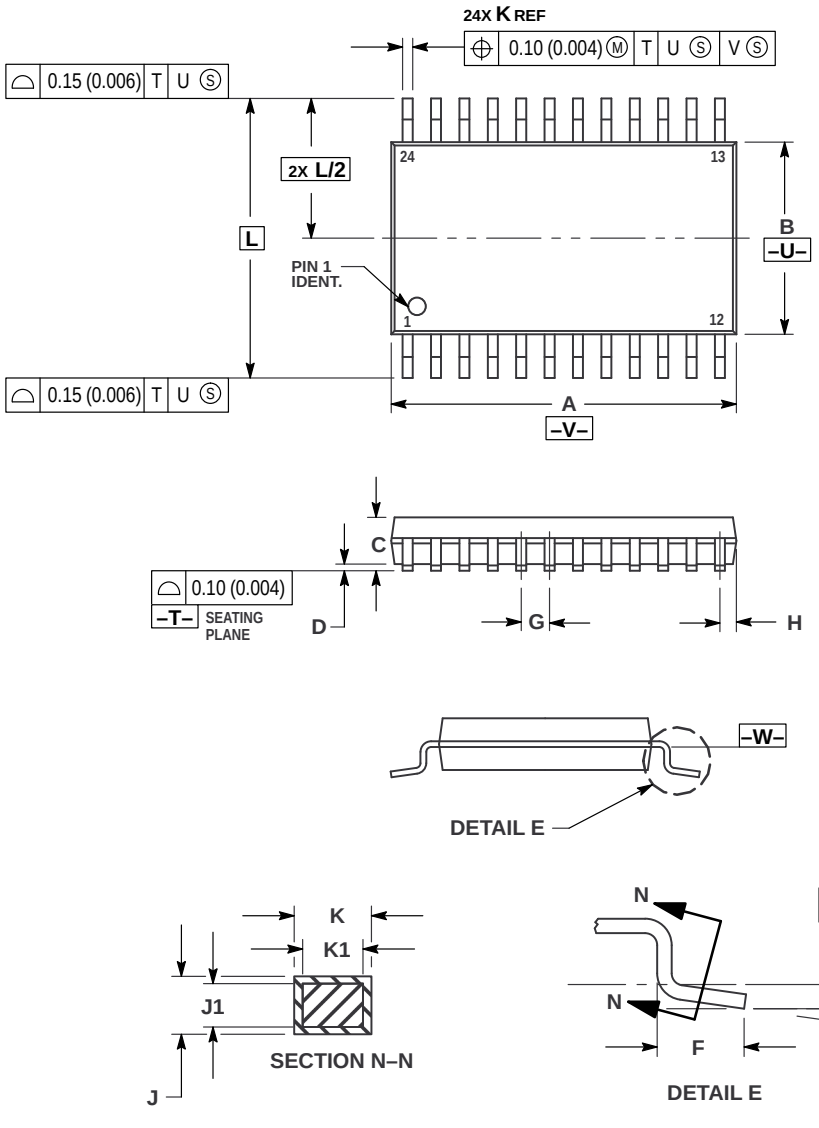
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF K DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR INTRUSION SHALL NOT REDUCE DIMENSION K BY MORE THAN 0.07 (0.002) AT LEAST MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	8.07	8.33	0.317	0.328
B	5.20	5.38	0.205	0.212
C	1.73	1.99	0.068	0.078
D	0.05	0.21	0.002	0.008
F	0.63	0.95	0.024	0.037
G	0.65 BSC		0.026 BSC	
H	0.44	0.60	0.017	0.024
J	0.09	0.20	0.003	0.008
J1	0.09	0.16	0.003	0.006
K	0.25	0.38	0.010	0.015
K1	0.25	0.33	0.010	0.013
L	7.65	7.90	0.301	0.311
M	0 °	8 °	0 °	8 °

24–Pin Packages

DT SUFFIX
PLASTIC TSSOP PACKAGE
CASE 948H–01
ISSUE O



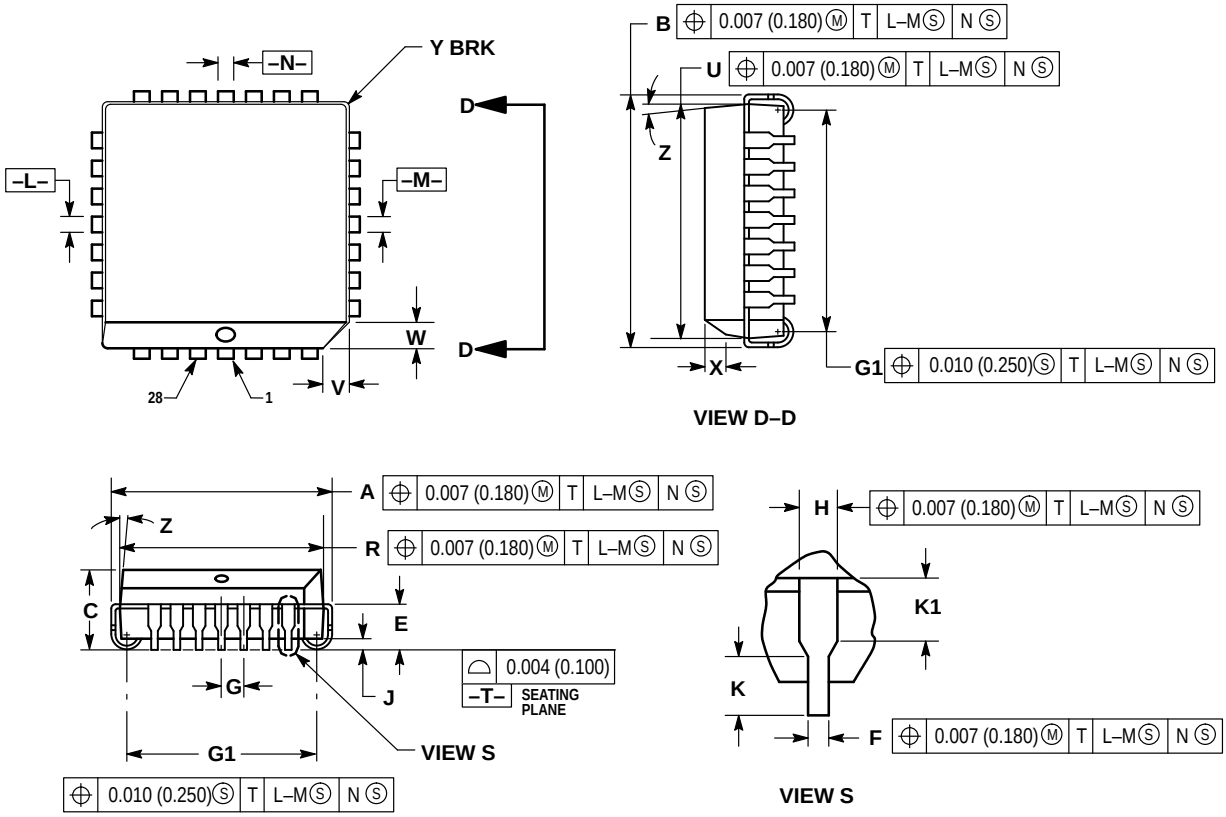


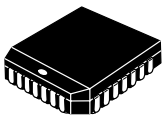
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	7.70	7.90	0.303	0.311
B	4.30	4.50	0.169	0.177
C	—	1.20	—	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

28–Pin Packages

FN SUFFIX
PLASTIC PLCC PACKAGE
CASE 776–02
ISSUE D



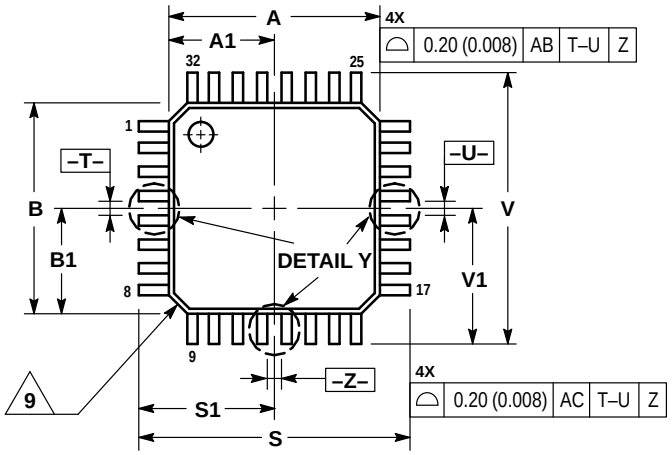


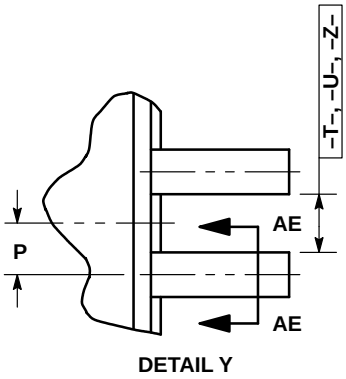
NOTES:
1. DATUMS –L–, –M–, AND –N– DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
2. DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM –T–, SEATING PLANE.
3. DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.
6. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
7. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.485	0.495	12.32	12.57
B	0.485	0.495	12.32	12.57
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	—	0.51	—
K	0.025	—	0.64	—
R	0.450	0.456	11.43	11.58
U	0.450	0.456	11.43	11.58
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	—	0.020	—	0.50
Z	2°	10°	2°	10°
G1	0.410	0.430	10.42	10.92
K1	0.040	—	1.02	—

32–Pin Package

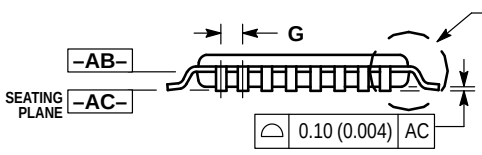
FA SUFFIX
PLASTIC TQFP PACKAGE
CASE 873A–02
ISSUE A

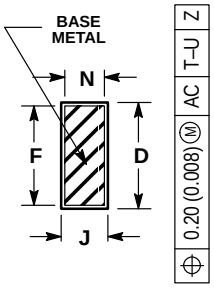




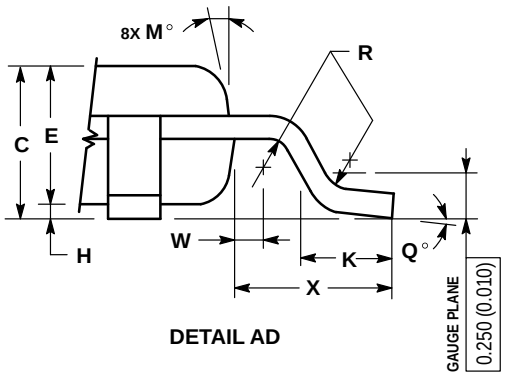
DETAIL Y

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE –AB– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS –T–, –U–, AND –Z– TO BE DETERMINED AT DATUM PLANE –AB–.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE –AC–.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –AB–.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.520 (0.020).
8. MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076 (0.0003).
9. EXACT SHAPE OF EACH CORNER MAY VARY FROM DEPICTION.





SECTION AE–AE

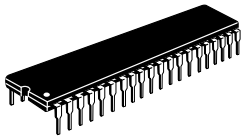


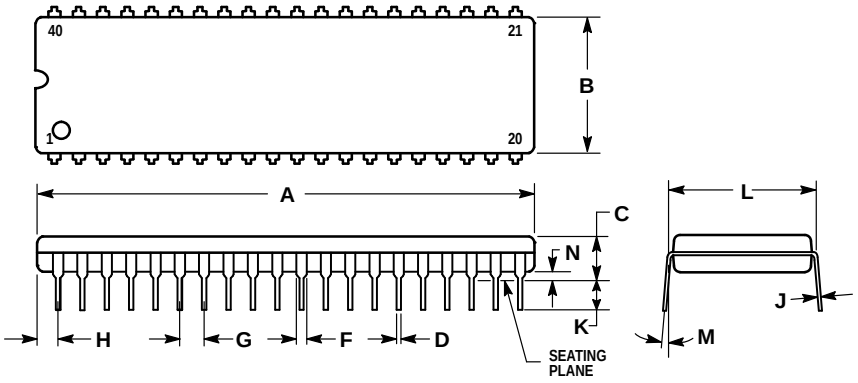
DETAIL AD

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	7.000 BSC		0.276 BSC	
A1	3.500 BSC		0.138 BSC	
B	7.000 BSC		0.276 BSC	
B1	3.500 BSC		0.138 BSC	
C	1.400	1.600	0.055	0.063
D	0.300	0.450	0.012	0.018
E	1.350	1.450	0.053	0.057
F	0.300	0.400	0.012	0.016
G	0.800 BSC		0.031 BSC	
H	0.050	0.150	0.002	0.006
J	0.090	0.200	0.004	0.008
K	0.500	0.700	0.020	0.028
M	12° REF		12° REF	
N	0.090	0.160	0.004	0.006
P	0.400 BSC		0.016 BSC	
Q	1°	5°	1°	5°
R	0.150	0.250	0.006	0.010
S	9.000 BSC		0.354 BSC	
S1	4.500 BSC		0.177 BSC	
V	9.000 BSC		0.354 BSC	
V1	4.500 BSC		0.177 BSC	
W	0.200 REF		0.008 REF	
X	1.000 REF		0.039 REF	

40–Pin Packages

N SUFFIX
PLASTIC DIP PACKAGE
CASE 711–03
ISSUE C



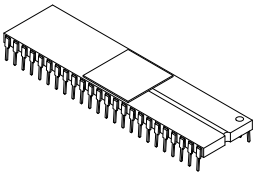


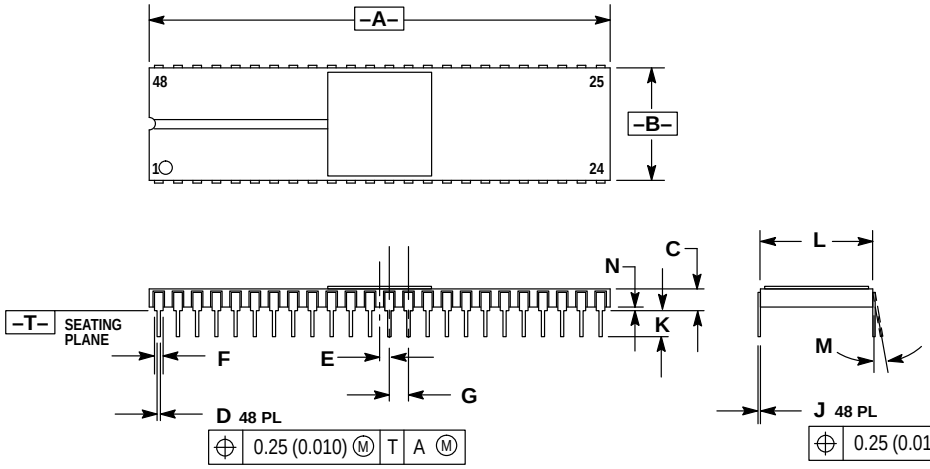
NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	51.69	52.45	2.035	2.065
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24 BSC		0.600 BSC	
M	0 °	15°	0 °	15°
N	0.51	1.02	0.020	0.040

48–Pin Packages

J SUFFIX
CERAMIC DIP PACKAGE
CASE 740–03
ISSUE B



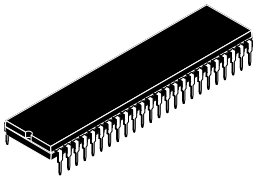


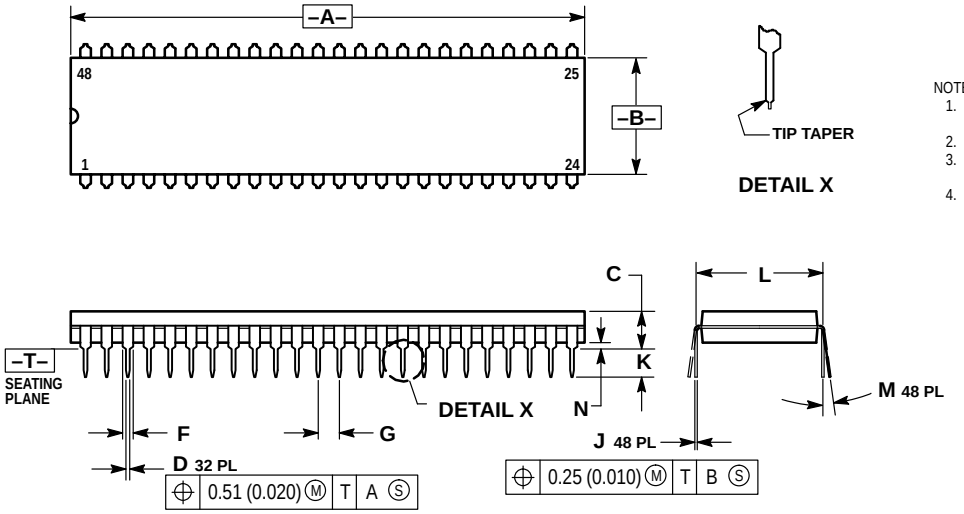
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	2.376	2.424	60.36	61.56
B	0.576	0.604	14.64	15.34
C	0.120	0.127	3.05	4.31
D	0.015	0.021	0.381	0.533
E	0.050 BSC		1.27 BSC	
F	0.030	0.055	0.762	1.397
G	0.100 BSC		2.54 BSC	
J	0.008	0.013	0.204	0.330
K	0.100	0.165	2.54	4.19
L	0.600 BSC		15.24 BSC	
M	0 °	10°	0 °	10°
N	0.040	0.060	1.016	1.524

48–Pin Packages

N SUFFIX
PLASTIC DIP PACKAGE
CASE 767–02
ISSUE B

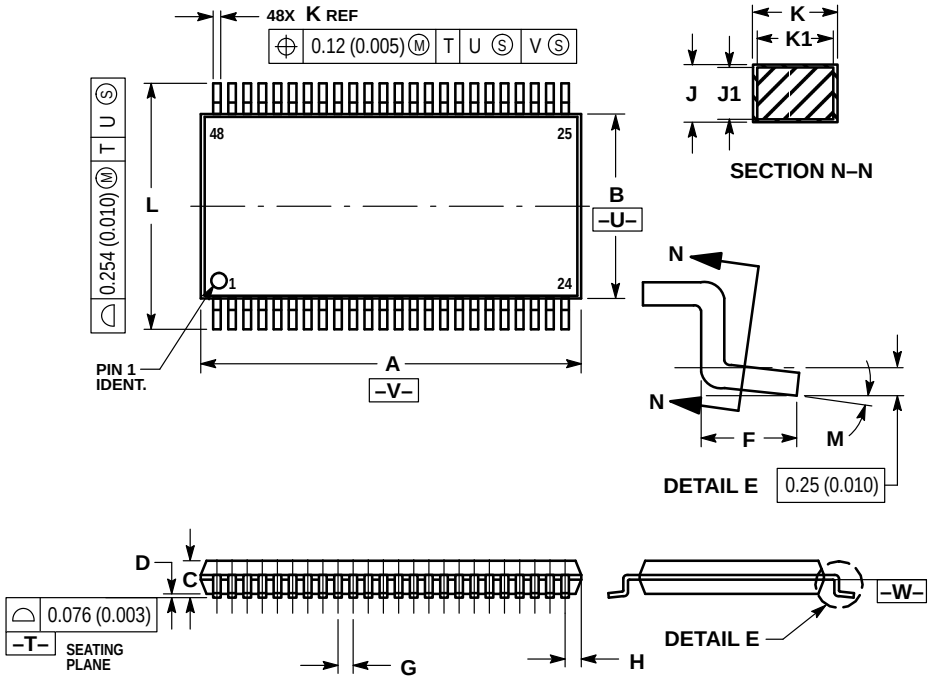




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH. MAXIMUM MOLD FLASH 0.25 (0.010).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	2.415	2.445	61.34	62.10
B	0.540	0.560	13.72	14.22
C	0.155	0.200	3.94	5.08
D	0.014	0.022	0.36	0.55
F	0.040	0.060	1.02	1.52
G	0.100 BSC		2.54 BSC	
H	0.070 BSC		1.79 BSC	
J	0.008	0.015	0.20	0.38
K	0.115	0.150	2.92	3.81
L	0.600 BSC		15.24 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

DT SUFFIX
PLASTIC TSSOP PACKAGE
CASE 1201–01
ISSUE A

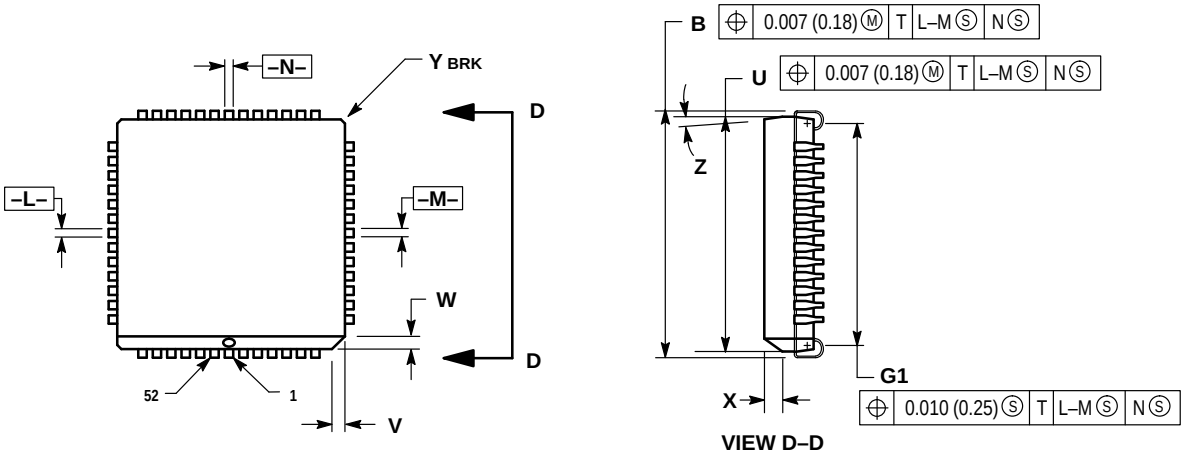


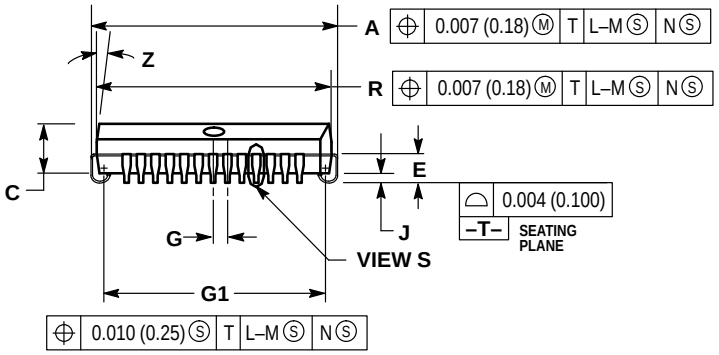
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
6. DIMENSIONS A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

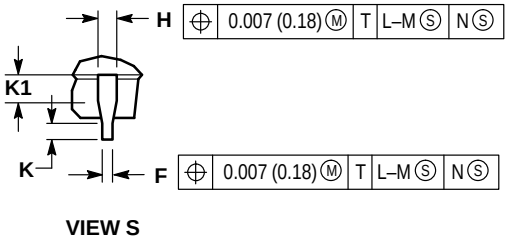
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	12.40	12.60	0.488	0.496
B	6.00	6.20	0.236	0.244
C	—	1.10	—	0.043
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.50 BSC		0.0197 BSC	
H	0.37	—	0.015	—
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.17	0.27	0.007	0.011
K1	0.17	0.23	0.007	0.009
L	7.95	8.25	0.313	0.325
M	0°	8°	0°	8°

52–Pin Packages

FN SUFFIX
PLASTIC PLCC PACKAGE
CASE 778–02
ISSUE C



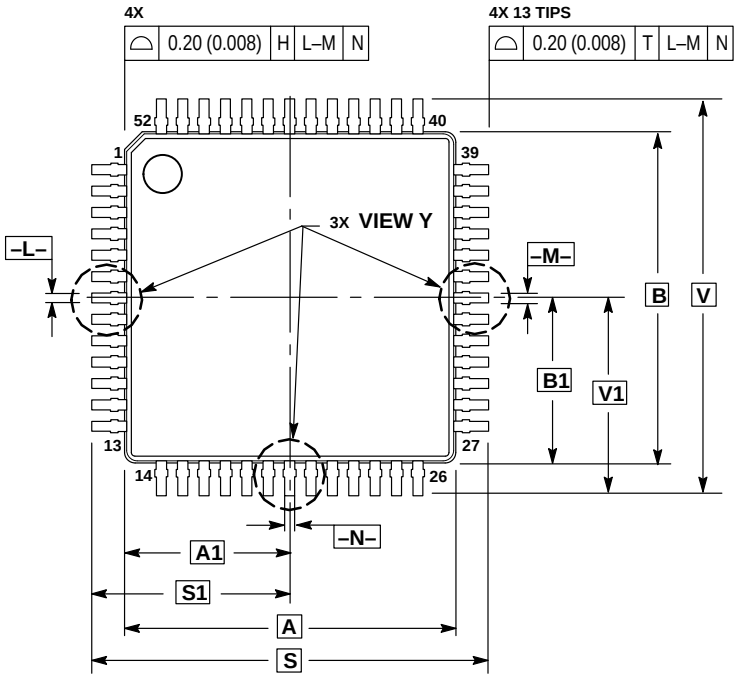


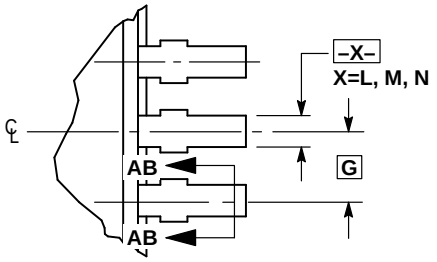


NOTES:
1. DATUMS –L–, –M–, AND –N– DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
2. DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM –T–, SEATING PLANE.
3. DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.
6. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
7. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

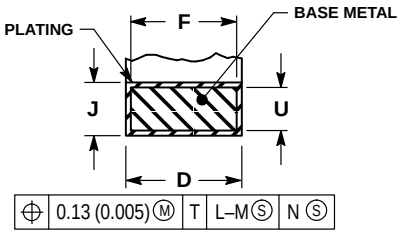
	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.785	0.795	19.94	20.19
B	0.785	0.795	19.94	20.19
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	—	0.51	—
K	0.025	—	0.64	—
R	0.750	0.756	19.05	19.20
U	0.750	0.756	19.05	19.20
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	—	0.020	—	0.50
Z	2°	10°	2°	10°
G1	0.710	0.730	18.04	18.54
K1	0.040	—	1.02	—

FA SUFFIX
PLASTIC TQFP PACKAGE
CASE 848D–03
ISSUE D

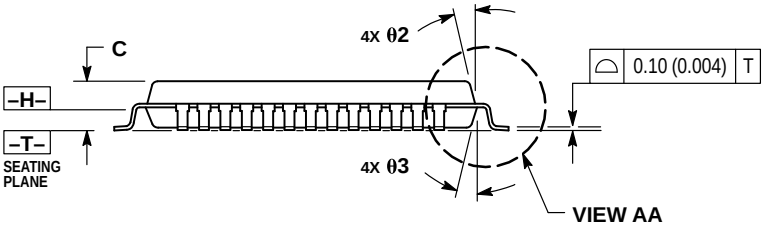




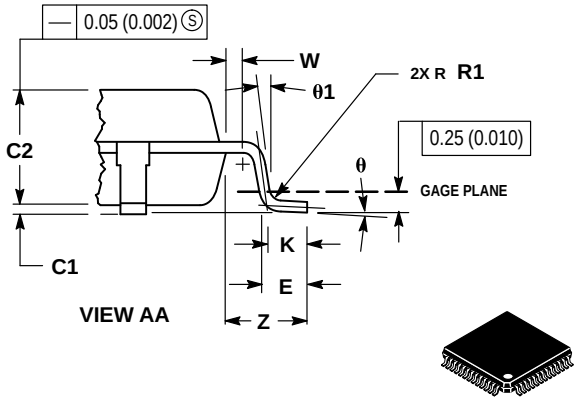
VIEW Y



SECTION AB–AB
ROTATED 90° CLOCKWISE



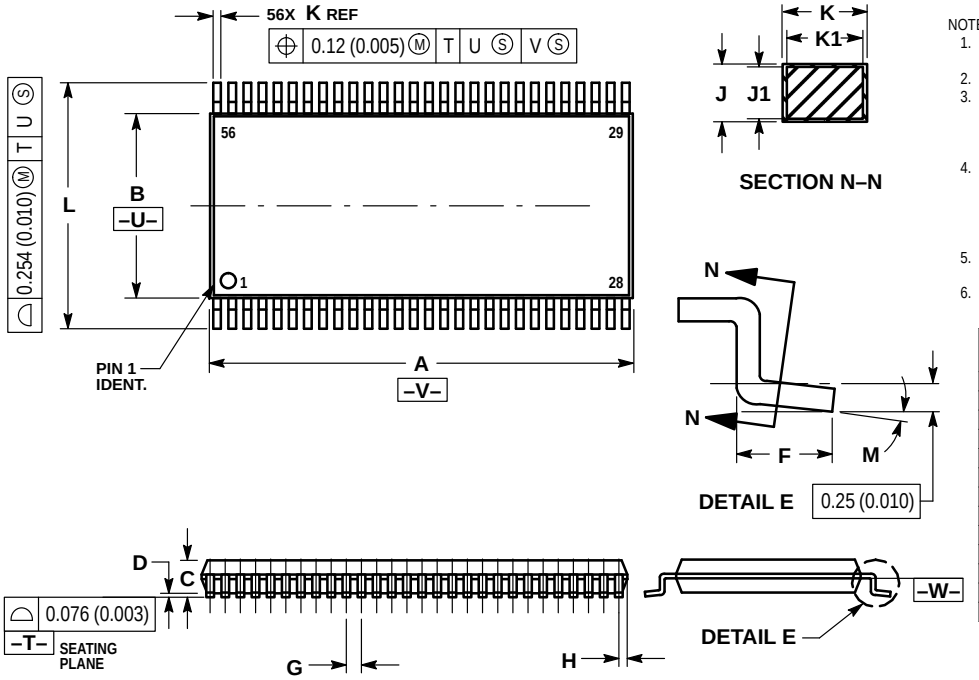
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE –H– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS –L–, –M– AND –N– TO BE DETERMINED AT DATUM PLANE –H–.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE –T–.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.46 (0.018). MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION 0.07 (0.003).



	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	10.00 BSC		0.394 BSC	
A1	5.00 BSC		0.197 BSC	
B	10.00 BSC		0.394 BSC	
B1	5.00 BSC		0.197 BSC	
C	—	1.70	—	0.067
C1	0.05	0.20	0.002	0.008
C2	1.30	1.50	0.051	0.059
D	0.20	0.40	0.008	0.016
E	0.45	0.75	0.018	0.030
F	0.22	0.35	0.009	0.014
G	0.65 BSC		0.026 BSC	
J	0.07	0.20	0.003	0.008
K	0.50 REF		0.020 REF	
R1	0.08	0.20	0.003	0.008
S	12.00 BSC		0.472 BSC	
S1	6.00 BSC		0.236 BSC	
U	0.09	0.16	0.004	0.006
V	12.00 BSC		0.472 BSC	
V1	6.00 BSC		0.236 BSC	
W	0.20 REF		0.008 REF	
Z	1.00 REF		0.039 REF	
θ	0°	7°	0°	7°
θ1	0°	—	0°	—
θ2	12° REF		12° REF	
θ3	12° REF		12° REF	

56–Pin Packages

DT SUFFIX
PLASTIC TSSOP PACKAGE
CASE 1202–01
ISSUE A

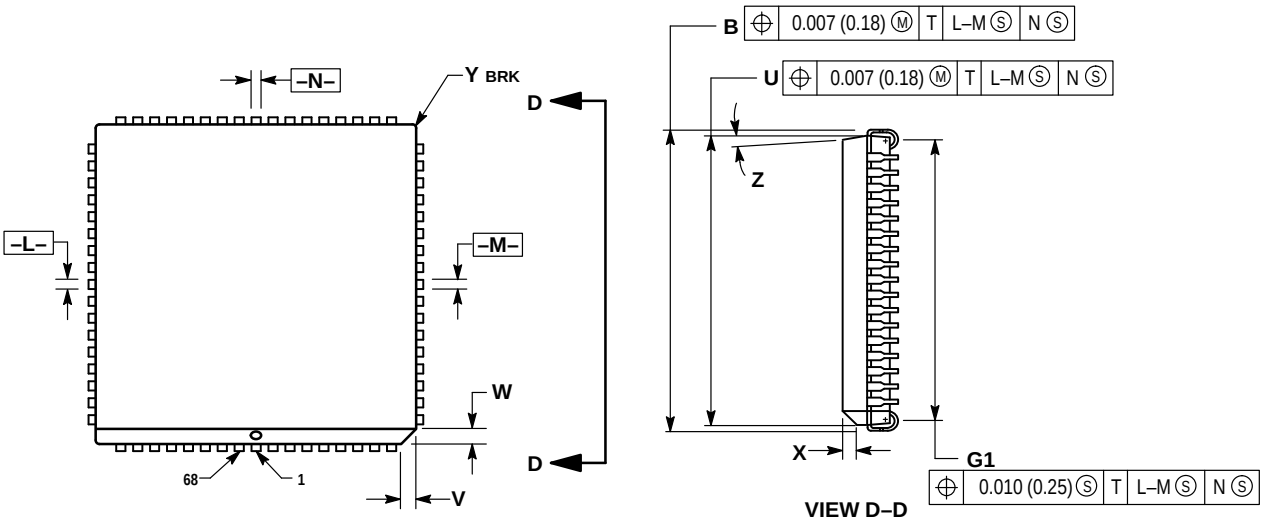


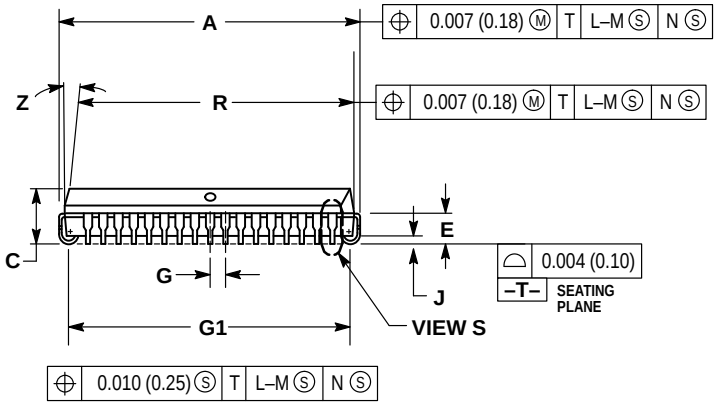
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
6. DIMENSIONS A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

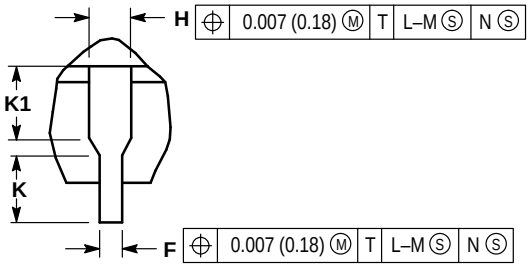
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	13.90	14.10	0.547	0.555
B	6.00	6.20	0.236	0.244
C	—	1.10	—	0.043
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.50 BSC		0.0197 BSC	
H	0.12	—	0.005	—
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.17	0.27	0.007	0.011
K1	0.17	0.23	0.007	0.009
L	7.95	8.25	0.313	0.325
M	0 °	8 °	0 °	8 °

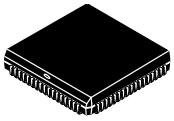
68–Pin Package

FN SUFFIX
PLASTIC PLCC PACKAGE
CASE 779–02
ISSUE C



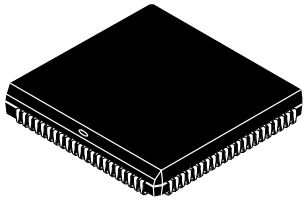




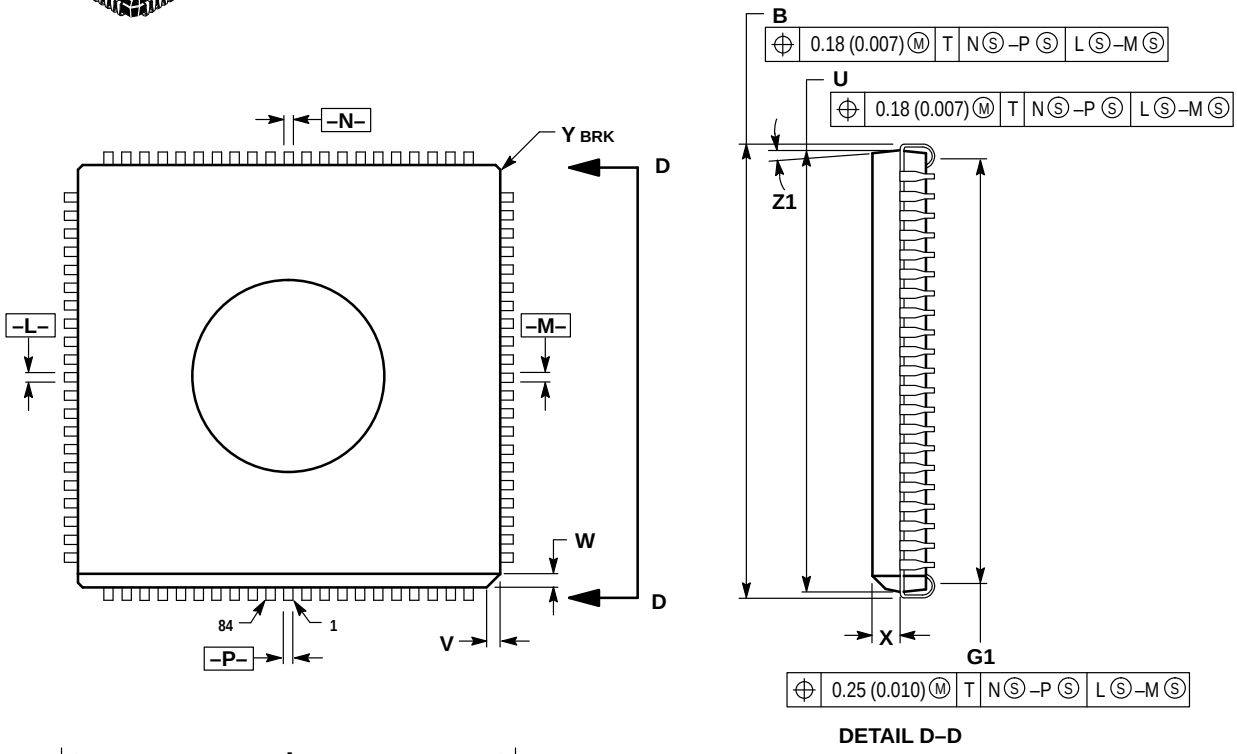


NOTES:
1. DATUMS –L–, –M–, AND –N– DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
2. DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM –T–, SEATING PLANE.
3. DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.
6. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
7. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.985	0.995	25.02	25.27
B	0.985	0.995	25.02	25.27
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	—	0.51	—
K	0.025	—	0.64	—
R	0.950	0.956	24.13	24.28
U	0.950	0.956	24.13	24.28
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	—	0.020	—	0.50
Z	2°	10°	2°	10°
G1	0.910	0.930	23.12	23.62
K1	0.040	—	1.02	—

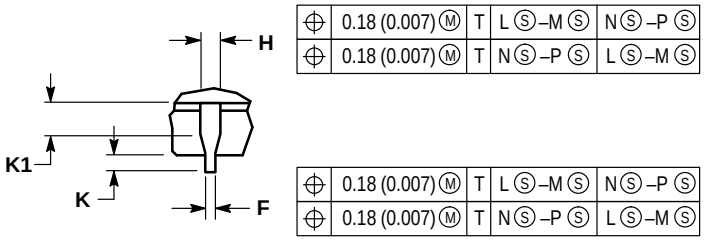


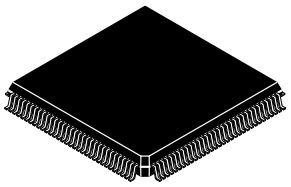
FN SUFFIX
PLASTIC PLCC PACKAGE
CASE 780A–01
ISSUE A



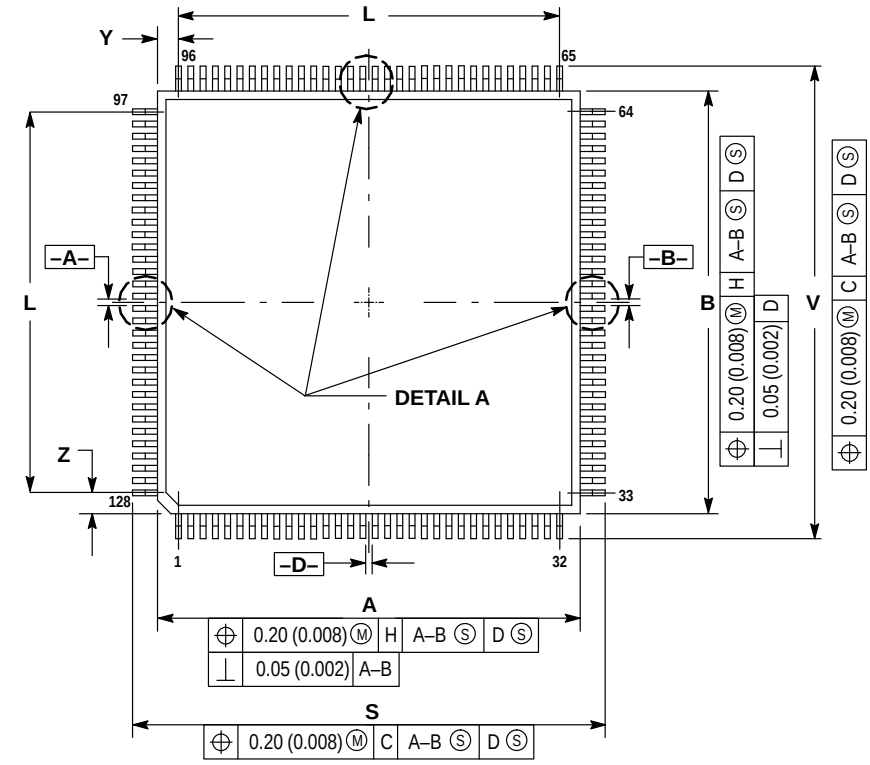
NOTES:
1. DATUMS –L–, –M–, –N–, AND –P– DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PACKAGE BODY AT GLASS PARTING LINE.
2. DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM –T–, SEATING PLANE.
3. DIMENSIONS R AND U DO NOT INCLUDE GLASS PROTRUSION. ALLOWABLE GLASS PROTRUSION IS 0.25 (0.010) PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.

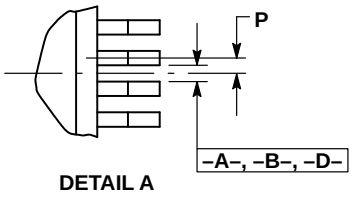
	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.185	1.195	30.10	30.35
B	1.185	1.195	30.10	30.35
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.021	0.33	0.53
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	—	0.51	—
K	0.025	—	0.64	—
R	1.150	1.156	29.21	29.36
U	1.150	1.156	29.21	29.36
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	—	0.020	—	0.50
Z	2°	10°	2°	10°
G1	1.110	1.130	28.20	28.70
K1	0.040	—	1.02	—
Z1	2°	10°	2°	10°



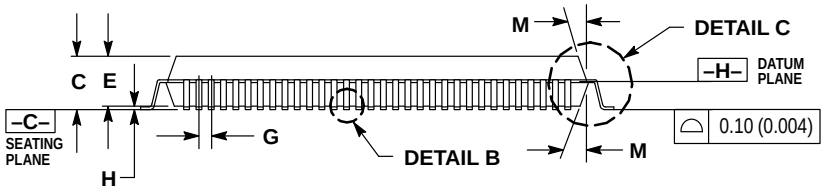


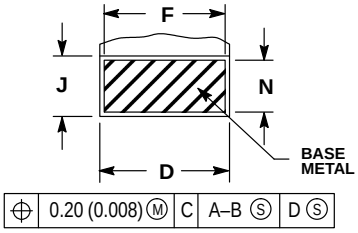
DD SUFFIX
PLASTIC QFP PACKAGE
CASE 862A–02
ISSUE B



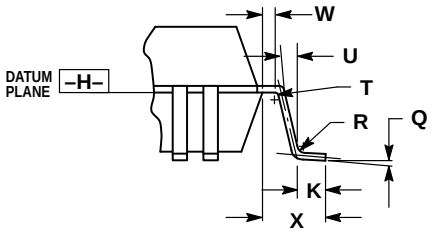


DETAIL A





DETAIL B

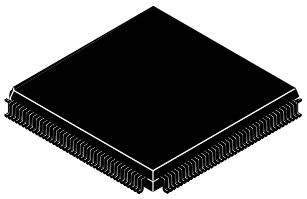


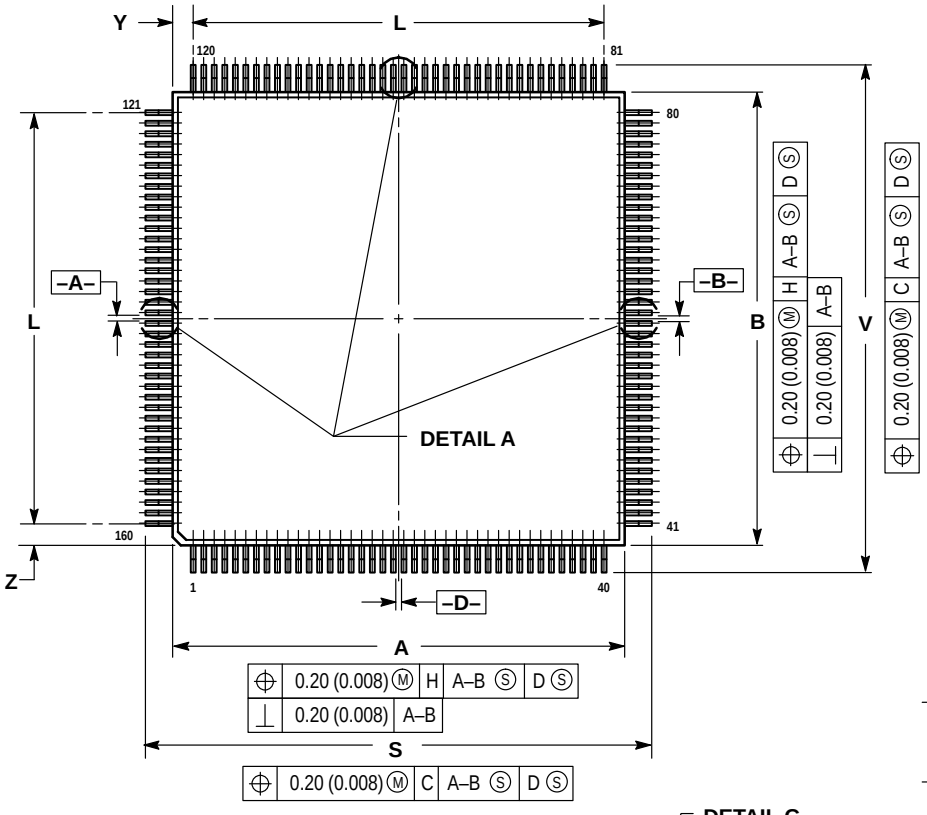
DETAIL C

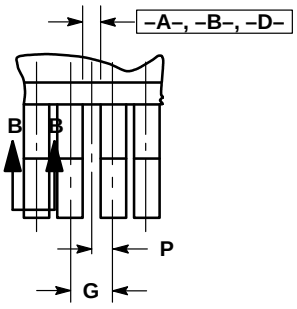
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER
3. DATUM PLANE –H– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS –A–, –B– AND –D–TO BE DETERMINED AT DATUM PLANE –H–.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE –C–.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –H–.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	27.90	28.10	1.098	1.106
B	27.90	28.10	1.098	1.106
C	—	4.07	—	0.160
D	0.30	0.45	0.012	0.018
E	3.17	3.67	0.125	0.144
F	0.30	0.40	0.012	0.016
G	0.80 BSC		0.032 BSC	
H	0.25	0.35	0.010	0.014
J	0.13	0.23	0.005	0.009
K	0.65	0.95	0.026	0.037
L	24.80 REF		0.976 REF	
M	5 °	16 °	5 °	16 °
N	0.13	0.17	0.005	0.007
P	0.40 BSC		0.016 BSC	
Q	0 °	7 °	0 °	7 °
R	0.13	0.30	0.005	0.012
S	30.95	31.45	1.219	1.238
T	0.13	—	0.005	—
U	0 °	—	0 °	—
V	30.95	31.45	1.219	1.238
W	0.40	—	0.016	—
X	1.60 REF		0.063 REF	
Y	1.60 REF		0.063 REF	
Z	1.60 REF		0.063 REF	

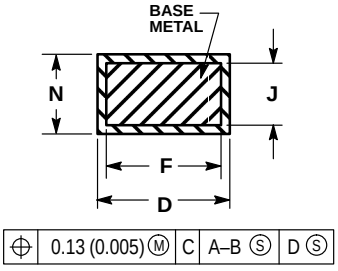
DH SUFFIX
PLASTIC QFP PACKAGE
CASE 864A–03
ISSUE C



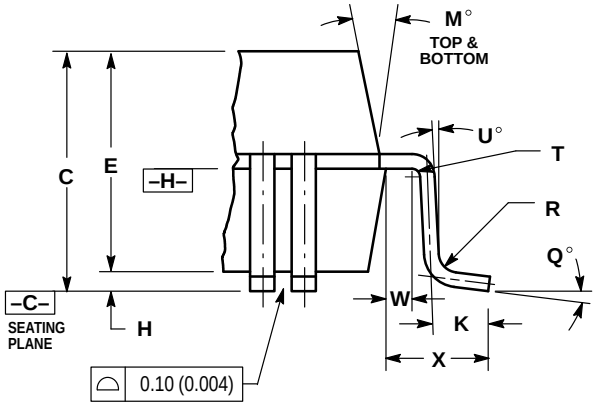




DETAIL A



SECTION B–B

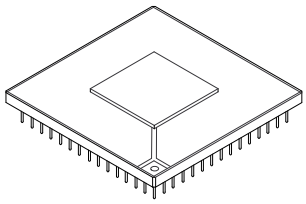


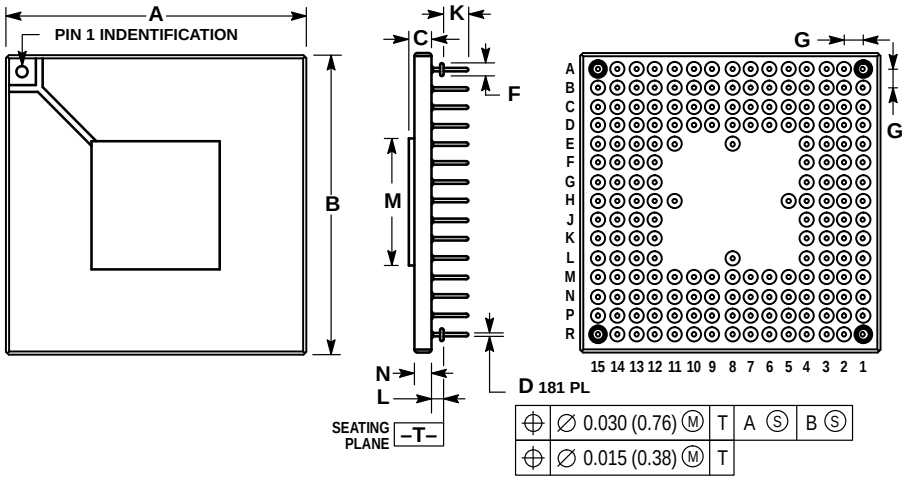
DETAIL C

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE –H– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS –A–, –B– AND –D– TO BE DETERMINED AT DATUM PLANE –H–.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE –C–.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –H–.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	27.90	28.10	1.098	1.106
B	27.90	28.10	1.098	1.106
C	3.35	3.85	0.132	0.152
D	0.22	0.38	0.009	0.015
E	3.20	3.50	0.126	0.138
F	0.22	0.33	0.009	0.013
G	0.65 BSC		0.026 REF	
H	0.25	0.35	0.010	0.014
J	0.11	0.23	0.004	0.009
K	0.70	0.90	0.028	0.035
L	25.35 REF		0.998 REF	
M	5°	16°	5°	16°
N	0.11	0.19	0.004	0.007
P	0.325 BSC		0.013 BSC	
Q	0°	7°	0°	7°
R	0.13	0.30	0.005	0.012
S	31.00	31.40	1.220	1.236
T	0.13	—	0.005	—
U	0°	—	0°	—
V	31.00	31.40	1.220	1.236
W	0.40	—	0.016	—
X	1.60 REF		0.063 REF	
Y	1.33 REF		0.052 REF	
Z	1.33 REF		0.052 REF	

HI SUFFIX
CERAMIC PGA PACKAGE
CASE 768N–01
ISSUE O

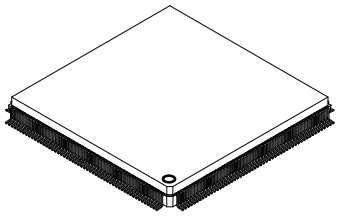


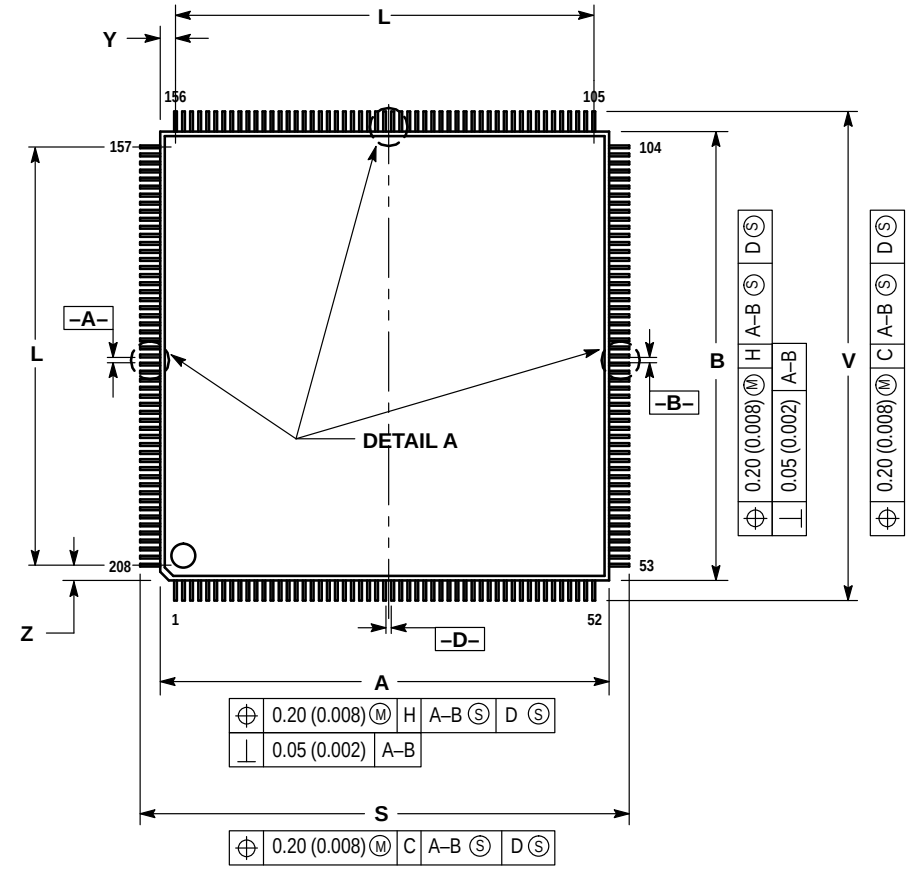


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.555	1.595	39.50	40.51
B	1.555	1.595	39.50	40.51
C	0.102	0.124	2.59	3.15
D	0.016	0.020	0.41	0.51
F	0.040	0.060	1.02	1.52
G	0.100 BSC		2.54 BSC	
K	0.110	0.150	2.79	3.81
L	0.043	0.057	1.09	1.45
M	0.655	0.675	16.64	17.15
N	0.090	0.110	2.29	2.79

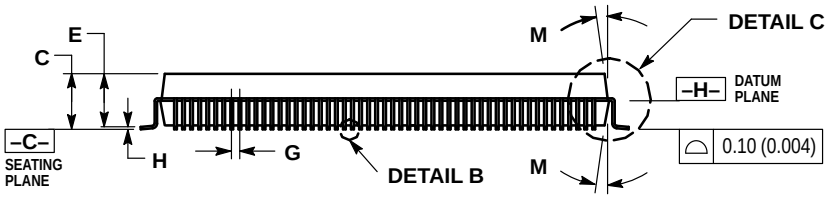
DK SUFFIX
PLASTIC QFP PACKAGE
CASE 872A–01
ISSUE O

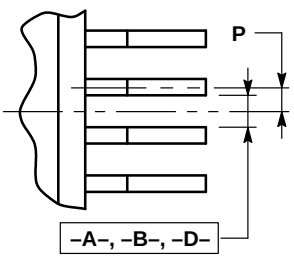




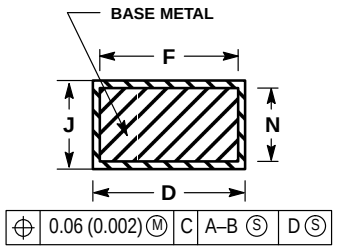
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE –H– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS –A–, –B– AND –D– TO BE DETERMINED AT DATUM PLANE –H–.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE –C–.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –H–.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.38 (0.015).

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	27.90	28.10	1.098	1.106
B	27.90	28.10	1.098	1.106
C	3.45	4.10	0.136	0.161
D	0.14	0.30	0.005	0.012
E	3.20	3.60	1.126	0.142
F	0.14	0.26	0.005	0.010
G	0.50 BSC		0.020 BSC	
H	0.25	0.35	0.010	0.014
J	0.09	0.20	0.003	0.008
K	0.70	0.90	0.027	0.036
L	25.50 REF		1.004 REF	
M	5 °	9 °	5 °	9 °
N	0.09	0.18	0.003	0.007
P	0.25 BSC		0.010 BSC	
Q	0 °	7 °	0 °	7 °
R	0.13	0.30	0.005	0.012
S	31.00	31.40	1.220	1.236
T	0.13	—	0.005	—
U	0 °	—	0 °	—
V	31.00	31.40	1.220	1.236
W	0.40	—	0.016	—
X	1.60 REF		0.063 REF	
Y	1.25 REF		0.049 REF	
Z	1.25 REF		0.049 REF	

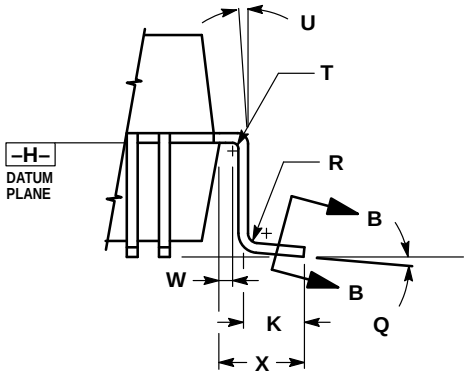




DETAIL A

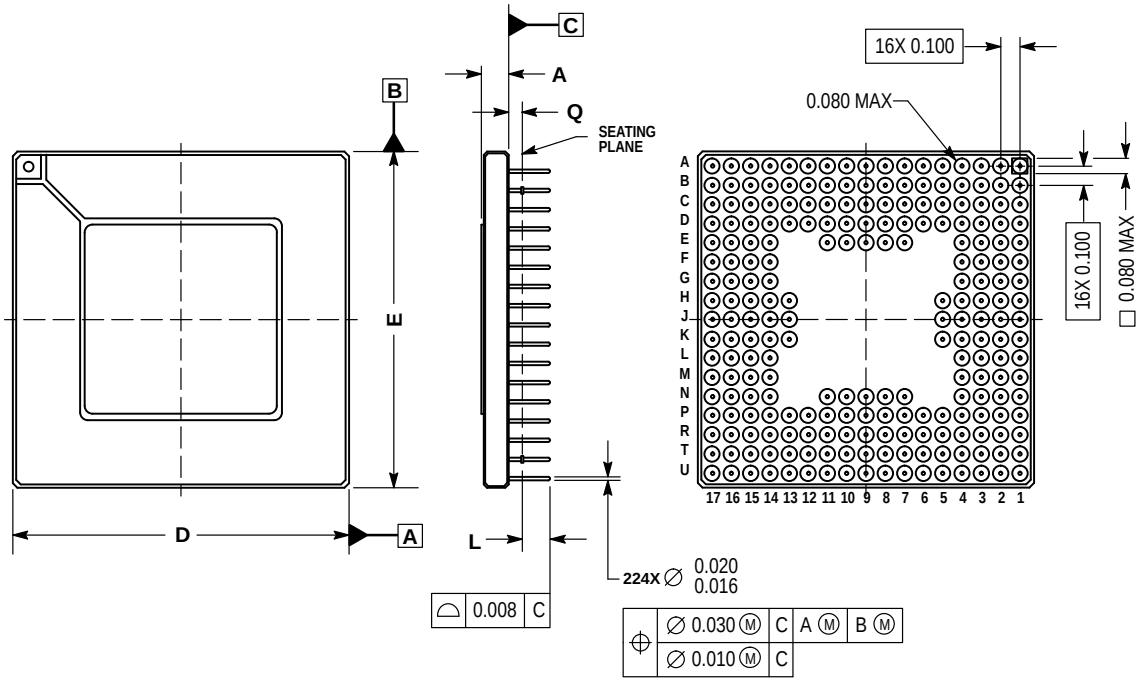


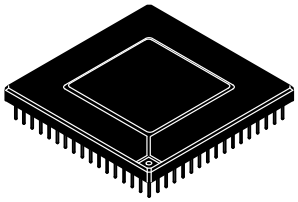
DETAIL B
SECTION B–B
ROTATED 7 ° CCW



DETAIL C

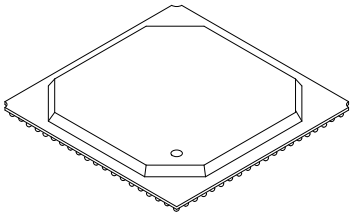
KE SUFFIX
PIN GRID ARRAY PACKAGE
CASE 860F–01
ISSUE O



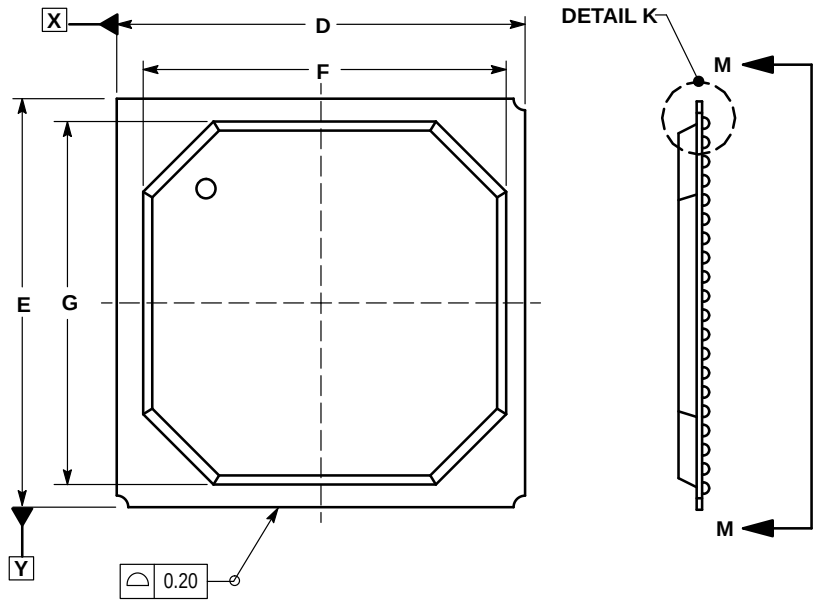


NOTES:
1. DIMENSIONS ARE IN INCHES.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. MINIMUM SPACING BETWEEN CONDUCTORS SHALL BE 0.020.

	INCHES	
DIM	MIN	MAX
A	0.070	0.145
D	1.740	1.780
E	1.740	1.780
L	0.100	0.200
Q	0.045	0.075

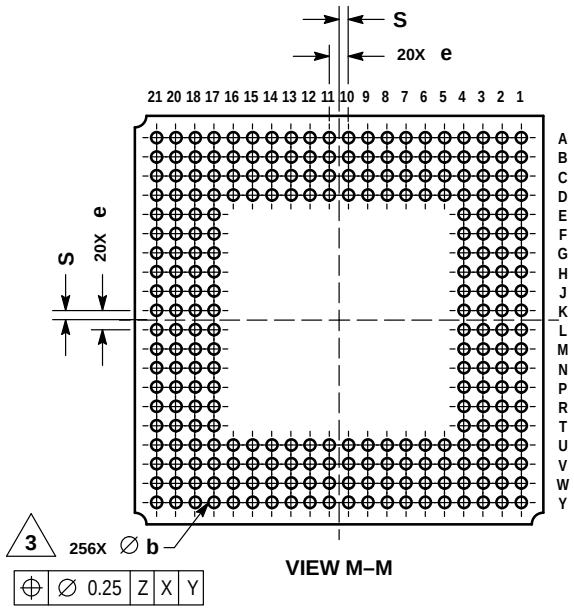


BG SUFFIX
PLASTIC BGA PACKAGE
CASE 1208A–01
ISSUE O

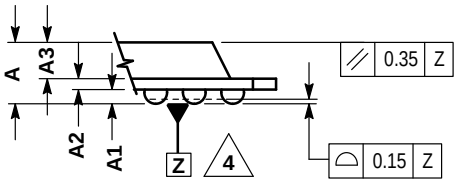


NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO DATUM PLANE Z.
4. DATUM Z (SEATING PLANE) IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

	MILLIMETERS	
DIM	MIN	MAX
A	1.92	2.32
A1	0.50	0.70
A2	0.36 REF	
A3	1.12	1.22
b	0.60	0.90
D	27.00 BSC	
E	27.00 BSC	
F	24.00	24.70
G	24.00	24.70
e	1.27 BSC	
S	0.635 BSC	

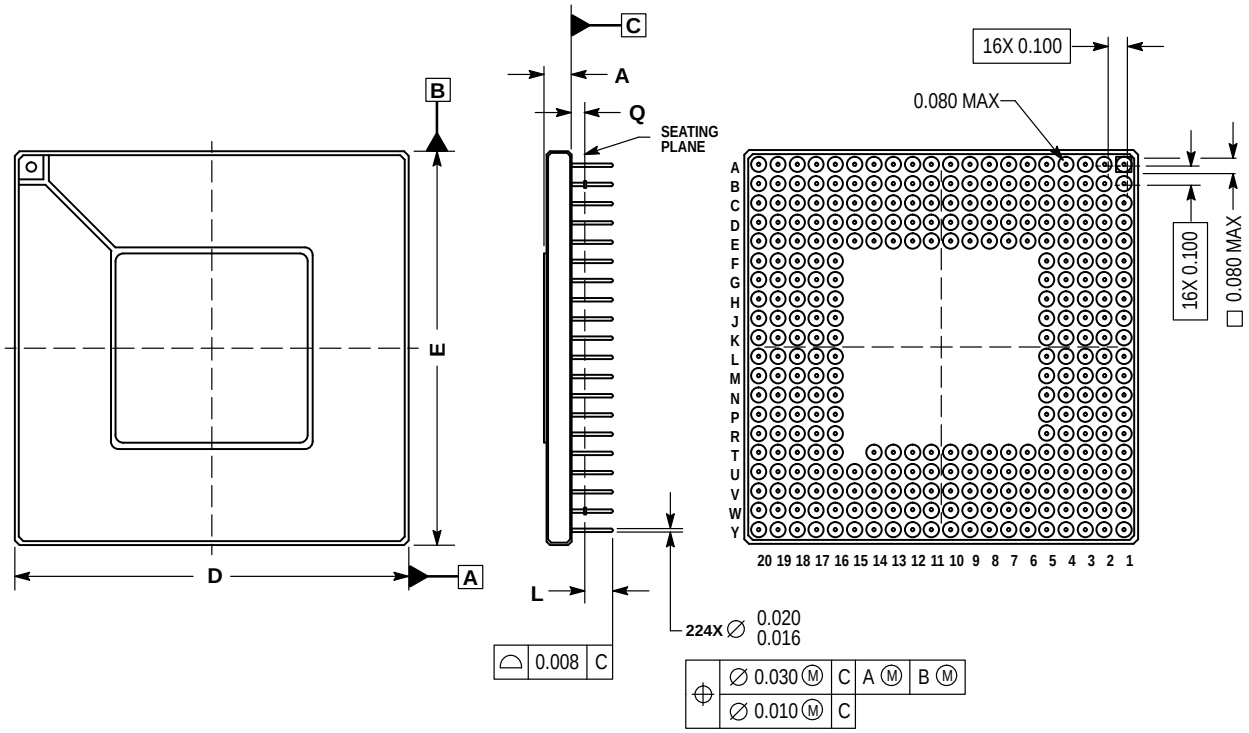


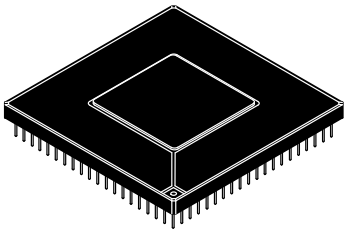
VIEW M–M



DETAIL K
ROTATED 90 ° CLOCKWISE

HV SUFFIX
PIN GRID ARRAY PACKAGE
CASE 861B–01
ISSUE O





NOTES:
1. DIMENSIONS ARE IN INCHES.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. MINIMUM SPACING BETWEEN CONDUCTORS SHALL BE 0.020.

	INCHES	
DIM	MIN	MAX
A	0.070	0.145
D	2.040	2.080
E	2.040	2.080
L	0.100	0.200
Q	0.045	0.075
S	0.050 BSC	

Packaging Information

Surface Mount

Why Surface Mount?

Surface Mount Technology is utilized to offer answers to many problems that have been created in the use of insertion technology.

Limitations have been reached with insertion packages and PC board technology. Surface Mount Technology offers the opportunity to continue to advance the state–of–the–art designs that cannot be accomplished with Insertion Technology.

Surface Mount Packages allow more optimum device performance with the smaller Surface Mount configuration. Internal lead lengths, parasitic capacitance and inductance that placed limitations on chip performance have been reduced.

The lower profile of Surface Mount Packages allows more boards to be utilized in a given amount of space. They are stacked closer together and utilize less total volume than insertion populated PC boards.

Printed circuit costs are lowered with the reduction of the number of board layers required. The elimination or reduction of the number of plated through holes in the board, contributes significantly to lower PC board prices.

Automatic placement equipment is available that can place Surface Mount components at the rate of a few thousand per hour to hundreds of thousands of components per hour.

Surface Mount Technology is cost effective, allowing the manufacturer the opportunity to produce smaller units and/or offer increased functions with the same size product.

Surface Mount assembly does not require the preparation of components that are common on insertion technology lines. Surface Mount components are sent directly to the assembly line, eliminating an intermediate step.

Pin Conversion Tables

Dual–in–Line Package to PLCC Pin Conversion Data

The following table gives the equivalent I/O pinouts of Dual–In–Line Package (DIP) configuration and Plastic Leaded Chip Carrier (PLCC) packages.*

Conversion Tables

8 PIN DIP	1	2	3	4	5	6	7	8
20 PIN PLCC	2	5	7	10	12	15	17	20

14 PIN DIP	1	2	3	4	5	6	7	8	9	10	11	12	13	14
20 PIN PLCC	2	3	4	6	8	9	10	12	13	14	16	18	19	20

16 PIN DIP	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
20 PIN PLCC	2	3	4	5	7	8	9	10	12	13	14	15	17	18	19	20

20 PIN DIP	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
20 PIN PLCC	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20

24 PIN DIP	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
28 PIN PLCC	2	3	4	5	6	7	9	10	11	12	13	14	16	17	18	19	20	21	23	24	25	26	27	28

* The MC1648 has a Non–Standard Conversion Table. For more information, refer to the Motorola MECL Data Book, DL122/D.

Tape and Reel

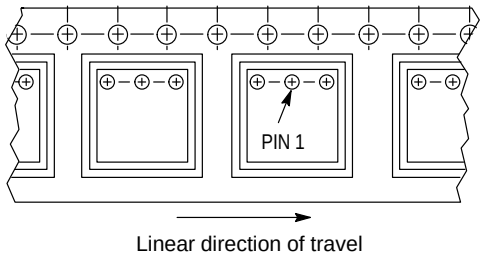
Logic Integrated Circuits

Motorola's tape and reel packaging fully conforms to the latest EIA RS–481A specification. The antistatic embossed tape provides a secure cavity sealed with a peel–back cover tape.

Mechanical Polarization

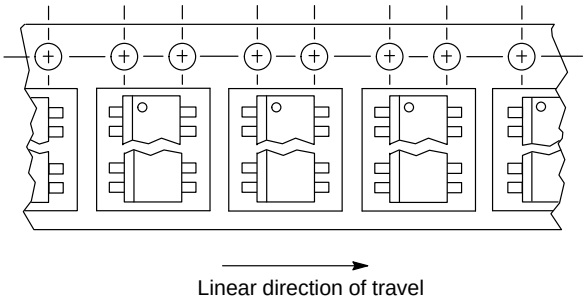
PLCC Devices

Typical



SOIC Devices

Typical



General Information

— Reel Size	13 inch (330 mm) Suffix: R2	— Units/Reel	500 to 5000 (see table)
— Tape Width	12 mm to 24 mm (see table)		

Ordering Information

To order devices which are to be delivered in Tape and Reel, add the suffix R2 to the device number being ordered.

Tape and Reel Data

Device Type	Tape Width (mm)	Device/Reel	Reel Size (inch)	Min Lot Size Per Part No. Tape and Reel
PLCC–20	16	1,000	13	3,000
PLCC–28	24	500	13	500
SO–8	12	2,500	13	5,000
SO–14	16	2,500	13	5,000
SO–16	16	2,500	13	5,000
SO–16 Wide	16	1,000	13	5,000
SO–20 Wide	24	1,000	13	5,000