PIECE-WISE LINEAR ANALYSIS APPLIED TO DESIGN OF INTEGRATED LOGIC CIRCUITS

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Summary

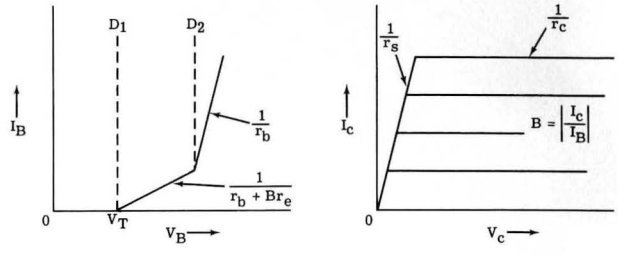
By using a three segment piece-wise linearization of the transistor input and output characteristics, a method has been developed whereby the steady state design of logic circuitry can be optimized analytically. The method has been applied to the design of direct coupled transistor logic (DCTL) and current-mode logic circuitry. The close agreement between the theoretical and experimental data indicates the method should be applicable to most transistor logic circuit design.

Introduction

Reliable optimized design without recourse to unrealistic overdesign factors is the ultimate objective of any circuit design analysis. The specific objective of this study was to predict the interrelationships between the integrated circuit parameters and then optimize the integrated circuitry. Most logic circuits are dependent on certain reliable logic levels being achieved and maintained under worst case conditions of ambient temperature and circuit and device tolerances. These levels are a direct function of the steady state design of the circuits in the system. Although the transient analysis is important, usually any discrepancy between the theoretical and experimental can be overcome by a system speed adjustment; however, an error in the steady state analysis could result in a complete system failure and the only recourse is the complete circuit redesign. In light of this, the importance of analytical steady state design and optimization cannot be over-emphasized. Although worst case design can be accomplished by many methods it is usually an iterative type process using the transistor data sheet and working in terms of the transistor terminals; or else, it employs the basic transistor equations which many times are unwieldly for most circuit analysis,[1, 2, 3, 4]. By use of the piece-wise linearization of the transistor (or diode) characteristics, simple analytical expressions can be developed to optimize the steady state design.

The piece-wise linearization technique leads to a simple model which is in close agreement with experimental data. Figure 1 is a typical I_B - V_B and I_C - V_C characteristic of a 2N834 device. A good approximation to the exponential relations can be made by linearizing the characteristics as shown in Figure 2.

Figure 3 is an equivalent circuit that is compatible with the curves of Figure 2. The breakpoints



V_T = Base emitter threshold voltage

r_b = internal base resistance

r_s = collector saturation resistance

r_c = reverse biased collector resistance

B = Common Emitter Current Gain at edge of saturation

Figure 2. Piece-Wise Linearized Characteristic of the 2N834

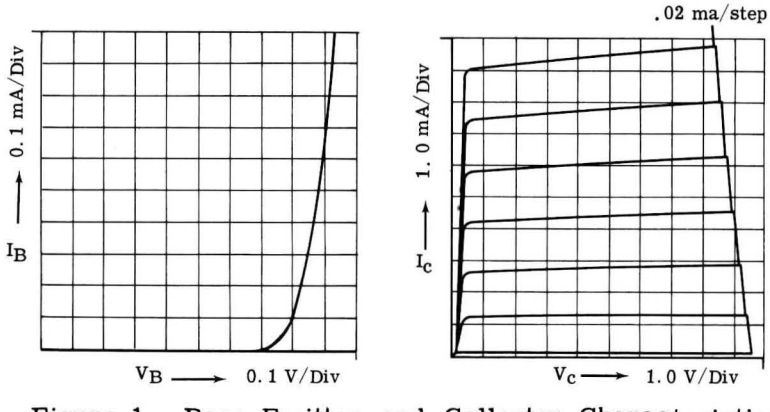


Figure 1. Base-Emitter and Collector Characteristics of a Typical 2N834 Planar Epitaxial Device.

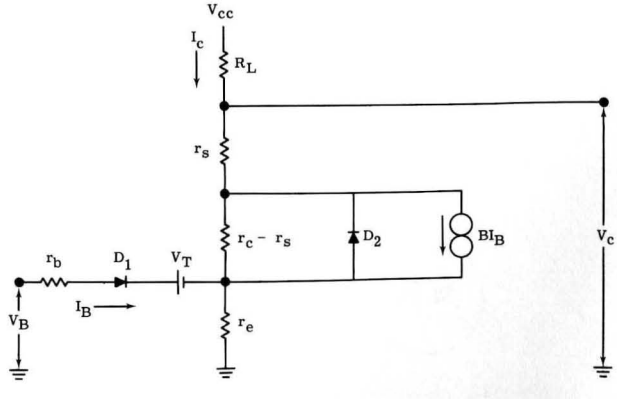


Figure 3. Equivalent Circuit for Piece-Wise Linearized 2N834

of diodes D_1 and D_2, indicated in Figure 2, can be qualitatively explained as follows:

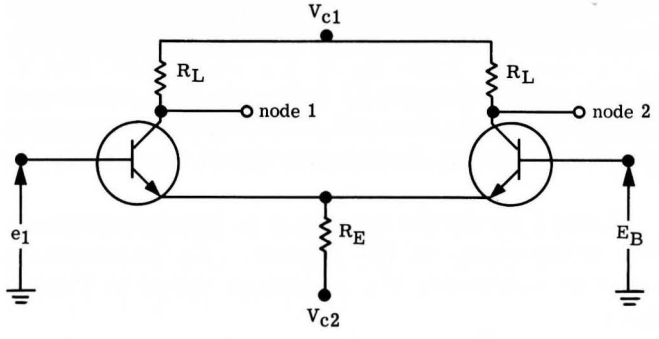
If the diodes are ideal and if the conduction current of the base emitter junction is assumed negligible below a certain threshold voltage V_T (for example 0.7 volts for Silicon, see Figure 1), then the base emitter equivalent at the D_1 breakpoint will be the ideal diode in series with a battery of potential V_T. In the region from D_1 breakpoint to D_2 breakpoint, the normal transistor action takes place. The slope of the V_B - I_B characteristics is $(B + 1)\, r_e + r_b$; however since $r_e = \frac{KT}{qI_E}$ the linear segment from D_1 to D_2 of Figure 2 is a result of averaging I_E. From the D_1 to D_2 breakpoint, the average I_E will simply be the I_E at D_2 breakpoint divided by two. When D_2 breakpoint is reached there is an abrupt change in the terminal impedances and a good first order approximation of the base emitter impedance is r_b and the collector impedance is r_s. Thus Figure 3 follows if the following assumptions are made:

1. $B + 1 \approx B$

2. $r_b >$ parallel combination of re and $(R_L + r_s)$ in the saturation region.

3. Leakage currents are neglected.

The equivalent circuit of Figure 3 will first be applied to a non-saturated current mode circuit to show the degree of accuracy with which the various breakpoints can be predicted; and then, to a DCTL circuit for optimum design.



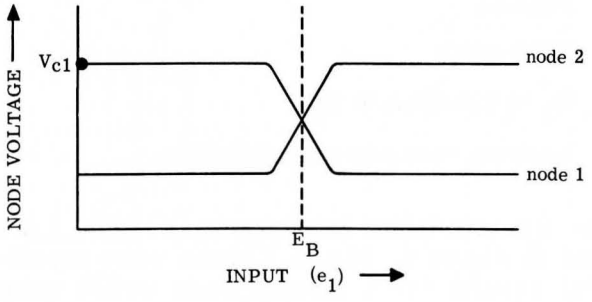


Figure 4. Current Mode Switching Circuit with Typical Voltage Transfer Characteristic

DESIGN OF CURRENT MODE LOGIC CIRCUITS

A typical current mode switching circuit is shown in Figure 4 along with typical voltage transfer characteristics. The piece-wise linearized equivalent circuit of Figure 4 is show in Figure 5.

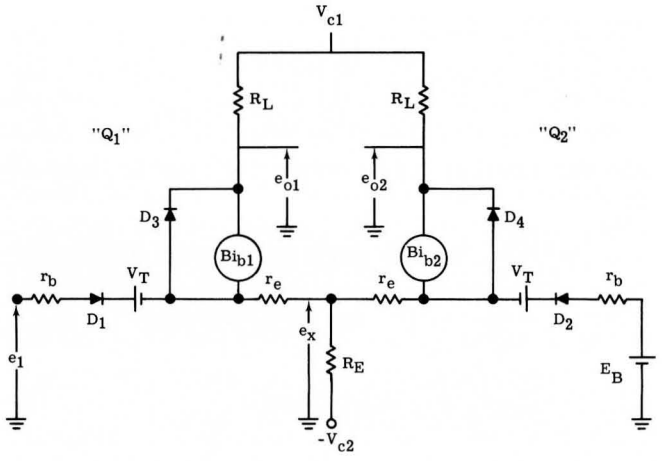


Figure 5. Current Mode Piece-Wise Linearized Equivalent Circuit

With a sufficiently negative input applied at e_1 the input transistor (Q_1) is cut off and the output transistor (Q_2) is conducting. For non-saturating operation through the range of practical inputs, the base current ib_2 must be limited in order to prevent saturation of Q_2 (conduction of diode D_4). This requirement can be found by writing the base and collector loop equations and setting the voltage across D_4 equal to zero.

$$\frac{E_B + Vc_2 - V_t}{rb + (\beta+1)(RE+re)} \leq \frac{V_{c1} + V_t - E_B}{+\beta RL - rb} \qquad (1)$$

The following equations are derived by simple loop equations using Figure 5. With the input voltage e_1 sufficiently negative and meeting the conditions of Equation 1, the conditions of the diodes are: D_1 open, D_2 conducting, D_3 open and D_4 open. As e_1 becomes more positive, the first diode breakpoint occurs in D_1. The input voltage at the D_1 breakpoint is:

$$e_1 = V_T + e_x \quad (ib_1 = 0) \qquad (2)$$

now

$$ex = -\left[\frac{E_B + Vc_2 - V_T}{rb + (\beta+1)(RE+re)}\right]\left[(\beta+1)\,re + rb\right] - V_T + E_B \qquad (3)$$

$$e_1 = -\left[\frac{E_B+Vc_2-V_T}{rb+(\beta+1)\ (RE+re)}\right]\left[(\beta+1)re+rb\right] + E_B \quad (4)$$

The collector current (βib_2) is

$$\beta ib_2 = \frac{\beta\ \ (E_B+Vc_2-V_T)}{rb+(\beta+1)\ \ (RE+re)} \quad (5)$$

and the corresponding output voltages eo_1 and eo_2 are:

$$eo_2 = Vc_1 - \frac{\beta RL(E_B+Vc_2-V_T)}{rb+(\beta+1)\ (RE+re)} \quad (6)$$

$$eo_1 = Vc_1 \quad (7)$$

Equations 3 through 7 define one set of points on the collector-emitter voltage and the input current transfer characteristic of the circuit.

A second breakpoint occurs at D_2 as e_1 becomes increasingly positive. At the point where D_2 ceases to conduct, the voltage e_x is:

$$e_x = -V_T + E_B \quad (8)$$

Thus

$$e_1 = \frac{E_B+Vc_2-V_T}{RE}\left[\frac{rb}{(\beta+1)} + re\right] + E_B \quad (9)$$

the corresponding collector current (βib_1) is

$$\beta ib_1 = \frac{\beta\ \ (E_B+Vc_2-V_T)}{(\beta+1)RE} \quad (10)$$

The resulting output voltages, eo_1 and eo_2 are

$$eo_2 = Vc_1 \quad (11)$$

$$eo_1 = Vc_1 - \frac{\beta RL\left[E_B+Vc_2-V_T\right]}{(\beta+1)\ RE} \quad (12)$$

Equations 8 through 12 define four additional points on the collector-emitter voltage and input current transfer characteristic of the circuit. The remaining breakpoint of interest is where the input transistor Q_1 saturates (at the point where D_3 is on the verge of conduction.) This breakpoint occurs when the input voltage is

$$e_1 = \frac{Vc_1+Vc_2}{\beta RL+(\beta+1)\ (RE+re)}\left[r_b+(B+1)\ (RE+re)\right] + V_T - Vc_2 \quad (13)$$

The collector current at this breakpoint condition is

$$\beta ib_1 = \frac{\beta(Vc_1+Vc_2)}{\beta RL+(\beta+1)\quad (RE+re)} \quad (14)$$

The voltage e_x is

$$e_x = \frac{(\beta+1)RE\quad \left[Vc_1+Vc_2\right]}{\beta RL+(\beta+1)(RE+re)} - Vc_2 \quad (15)$$

and the output voltages eo_1 and eo_2 are

$$eo_2 = Vc_1 \quad (16)$$

$$eo_1 = Vc_1 - \frac{\beta RL(Vc_1+Vc_2)}{\beta RL+(\beta+1)\ (RE+re)} \quad (17)$$

Equations 13 through 17 define the four remaining breakpoints of the collector-emitter and input current transfer characteristics of the circuit.

Table I shows the approximate breakpoint transfer relationship of the circuit. The assumptions used to determine the equations shown in Table I are:

1. $\beta >> 1$
2. RE>>re
3. βRE>>rb
4. Q_1 is identical to Q_2
5. Leakage currents are negligible.

The interconnected breakpoints of Table I are plotted in Figure 6. Figure 7 shows some experimental results for a current mode switch using 2N834's. If one inserts the circuit and device parameters of Figure 7 into the equations of

Table I, the resulting calculated breakpoints are tabulated and shown in Table II.

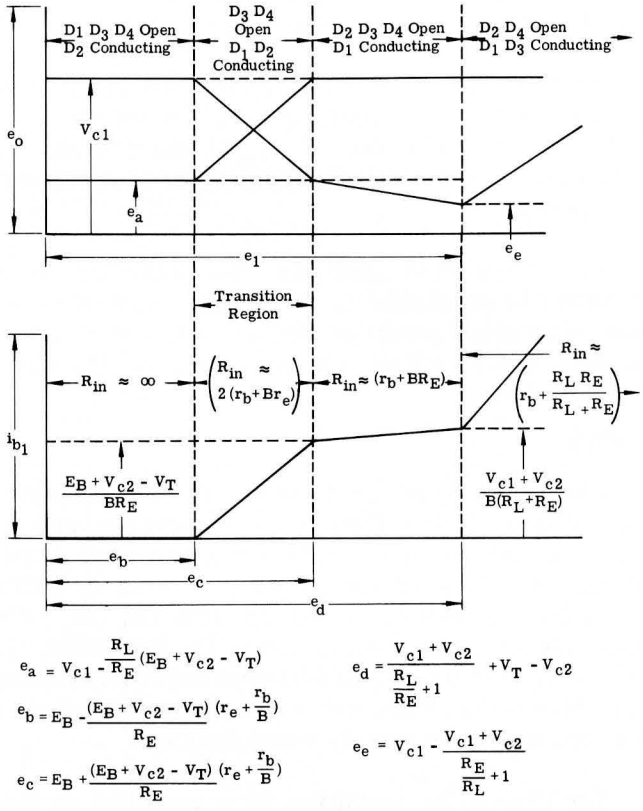


Figure 6. Interconnected Breakpoints for Current Mode Circuit

Table II indicates that good agreement has been obtained between calculated and experimental results. In additions to the experimental results of Figure 7, good agreement was obtained under other circuit conditions not shown here, indicating the piece-wise linear approximations to the non-linear transistor characteristics can be confidently applied to optimization of steady state current mode design.

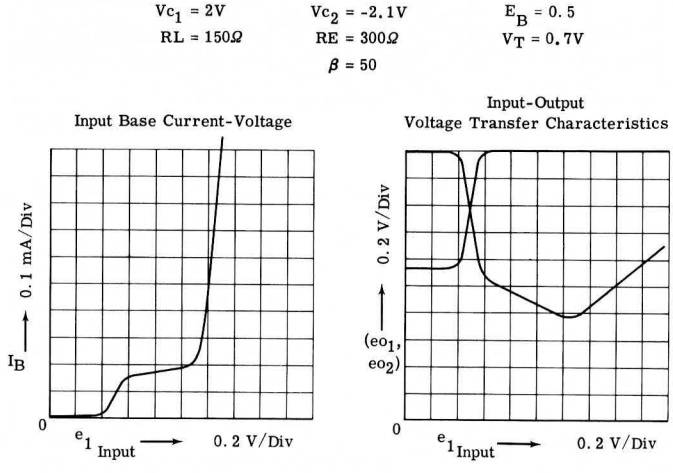


Figure 7. Experimental Curves of the Current Mode Circuit

The preceeding analysis indicates the specific circuit and device parameters critical to the design. From Figure 6 we note that the steady state levels are for practical considerations only a function of power supply and resistor tolerances. A worst case design follows quite easily from Figure 6.

The required conditions for reliable operation are that the maximum translated logical "1" voltage (Vc_1) should not saturate Q_2; the minimum translated logical "1" must be equal to or greater than the maximum transistion voltage; the maximum translated logical "O" voltage must be equal to or less than the minimum transition voltage. These conditions can be fulfilled by the following:

$$V_{Cl_{\substack{\text{Max.}\\\text{Translated}}}} < \left(\frac{V_{C1} + V_{C2}}{\frac{RL}{RE} + 1} + V_T - V_{C2}\right) \text{Min.}$$

$$V_{C1_{\substack{\text{Min.}\\\text{Translated}}}} > \left[\left(\frac{E_B + V_{C2} - V_T}{R_E}\right)\left(r_e + \frac{r_b}{B}\right) + E_B\right] \text{Max.}$$

$$\left[V_{C1} - \frac{R_L}{R_E}\left(E_B + V_{C2} - V_T\right)\right] \text{Max. Translated}$$

$$< \left[-\left(\frac{E_B + V_{C2} - V_T}{R_E}\right)\left(r_e + \frac{r_b}{B}\right) + E_B\right] \text{Min.}$$

The translated outputs are needed for level compatibility. If e_{01}, or e_{02} are connected directly to a base, the levels are not compatible for logic operation; thus, some method of level translation is needed. This level translation can be accomplished by numerous methods and will not be covered here.

For reliable circuit design and good noise immunity, it is desirable to make the transition region as small as possible with respect to the

logic level swing. From Figure 6 the transition width can be calculated and is approximately:

$$\Delta e \approx 2 \frac{(E_B + V_{C2} - V_T)}{R_e} \left(r_e + \frac{r_b}{B} \right) \quad (18)$$

Rewriting 18 in terms of I_e then

$$\Delta e \approx 2I_e \left[\frac{2\,KT}{qI_e} + \frac{r_b}{B} \right] = 104 \text{ mv} + \frac{2I_e r_b}{B} \quad \text{at } 25^\circ C \quad (19)$$

The I_e used to calculate r_e is averaged over the linear transition region, and is approximately

$$\frac{E_B + V_{C2} - V_T}{R_E} \times 1/2$$

Thus, the statement that current mode logic is relatively insensitive to transistor parameters is a valid statement only when the magnitude of logic level is large compared to the transition width. Figure 8 shows e_{out} versus e_{in} for various values of R_L and R_E, where the ratio of R_L/R_E is held constant. Table III is a compilation of the theoretical and experimental results of Figure 8. From Table III we note that for increasing emitter current the r_b/B term of equation 19 can contribute significantly to the transition width. It is interesting to note that the theoretical minimum of the transition region width is approximately 100mv at 25°C and is approached as the current level of the system is decreased.

Since the first term of equation 19 is directly proportioned to temperature, a design could be achieved whereby the $2I_e\ r_b/B$ term could be adjusted to minimize the temperature dependence of equation 19.

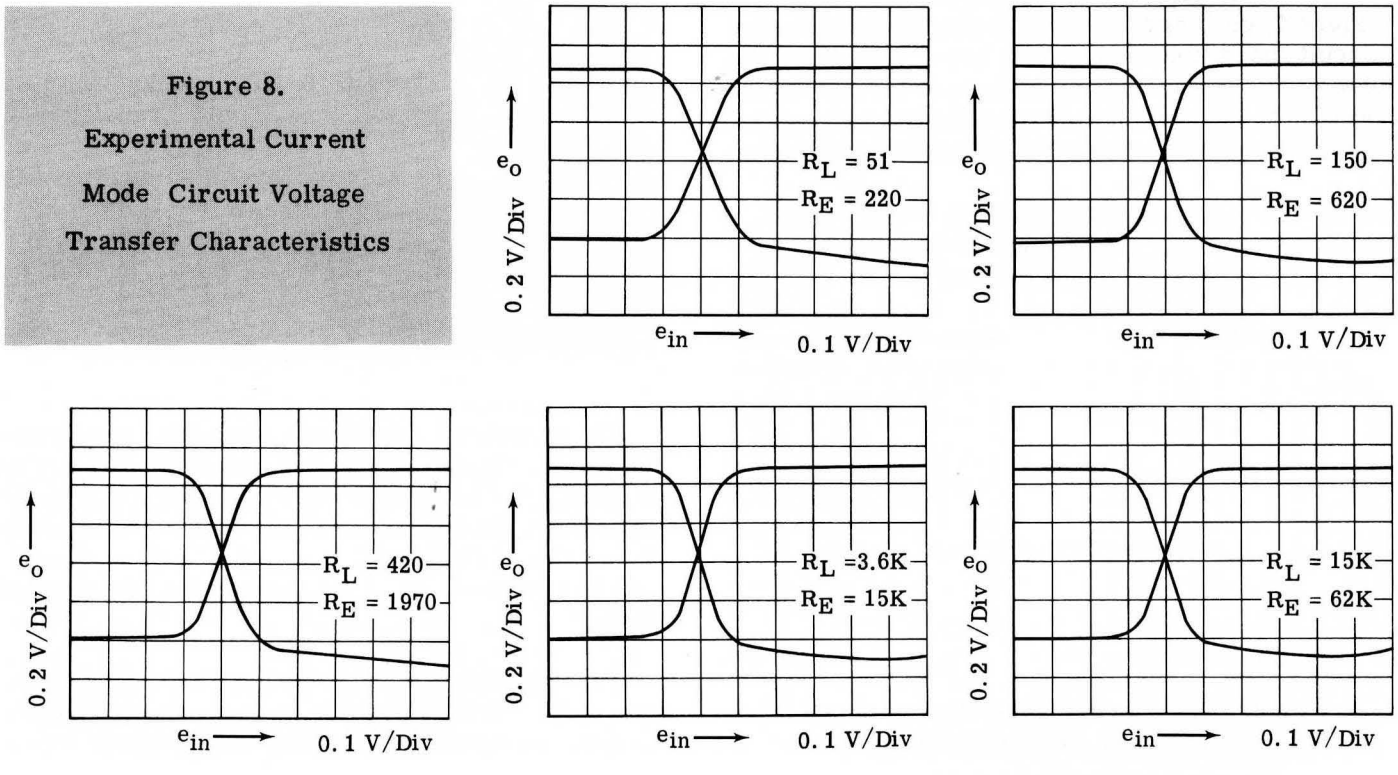
The piece-wise analysis has resulted in a reasonable prediction of breakpoints, clearly shows the interrelationship of device and circuit parameters and it offers a simple approach to worst case design.

DCTL

The DCTL type logic circuit is very sensitive to certain device parameter tolerances and as such is an excellent case for piece-wise linear analysis. One of the major problems of DCTL is achieving sufficient and reliable fan out. The fan out problem arises from the fact that the V_B - I_B characteristics of n parallel transistors are dissimilar; thus, there is an uneven distribution or hogging of current by some devices.

The V_B - I_B variation is a result of normal production spreads and fan in; fan in being more than one collector per load resistor. Figures 9 and 10 illustrate what might be a typical worst case circuit and transistor characteristic.

Figure 8.
Experimental Current
Mode Circuit Voltage
Transfer Characteristics



First a typical approach for solving for a fan out "n" will be outlined; then, the piece-wise linear analysis will be utilized to illustrate the flexibility of this approach.

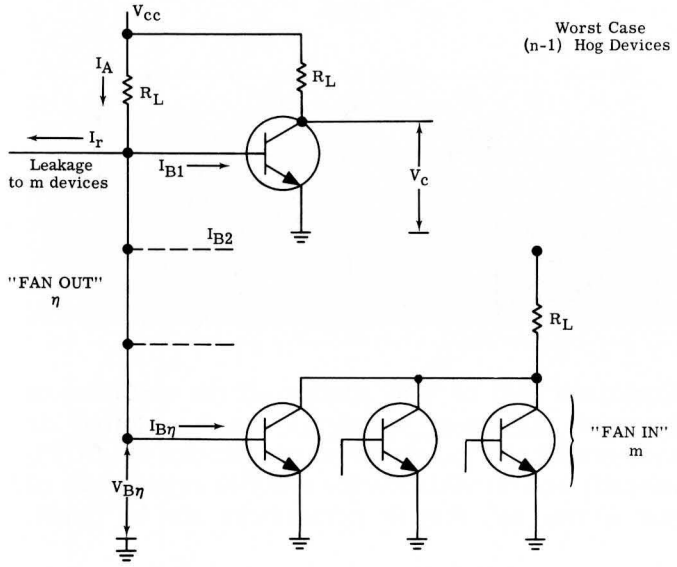


Figure 9. DCTL Worst Case Fan Out Configuration

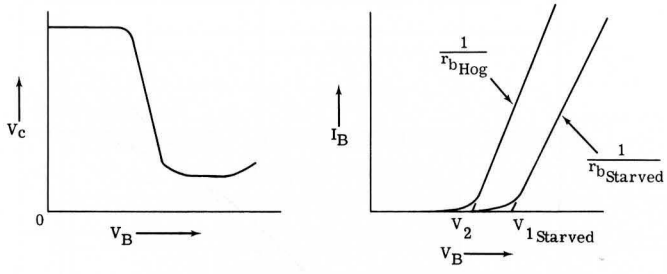


Figure 10. Typical Transistor Characteristics Necessary to Graphically Solve for Fan Out

Writing the node equations for the circuit of Figure 9 we have:

$$\frac{V_{cc} - V_{Bn}}{R_L} = I_{B1} + \sum_{n=2}^{n} I_{Bn} + I_r \qquad (20)$$

where

I_{B1} = base current of starved transistor

$\sum_{n=2}^{n} I_{Bn}$ = base currents of (n-1) hog type transistors

Due to the low leakage currents in silicon devices the I_r component is neglected. To solve equation (20) the relationship of V_{Bn} must be known.

$$V_{Bn} = f(I_{Bn}, V_{cn}) \qquad (21)$$

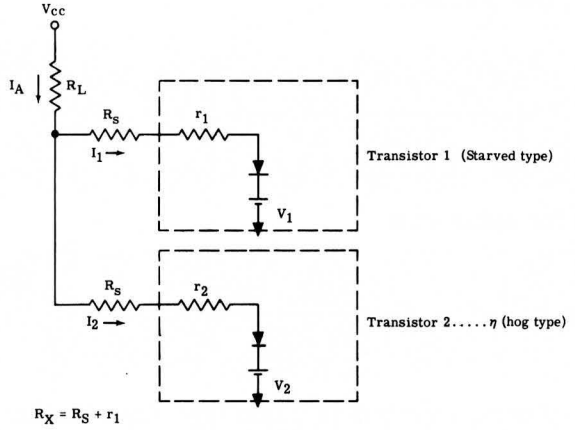
and since $V_{Bn} = V_{B1}$ we have

$$V_{Bn} = V_{B1} = f(I_{B1}, V_{c1}) \qquad (22)$$

This relationship is found graphically from the type curves shown in Figure 10. Knowing the relationship of (22), (20) can be solved for n. The curves necessary for this type approach are not always available; or if they are plotted, the points needed from the curves are not sharply defined. Thus the ΔI_B between hog and starved device could be in considerable error if the slopes are large.

The procedure outlined is time consuming and error-ridden. It does not allow the designer to see the interrelationship between the device and circuit parameters; and worst of all, it is valid only for the devices being investigated.

A more thorough and general analysis can be accomplished by using the piece-wise linear analysis. Applying the piece-wise linear analysis to the circuit of Figure 9 the resulting equivalent circuit is shown in Figure 11. The complete derivation is shown in Appendix A. Figure 11 has been simplified since the V_B - I_B variations due to production spread and fan in have been lumped into V_1 and V_2. If a general expression is desired V_1 and V_2 can be replaced by the proper V_{TS} expressions from Appendix A.



$R_X = R_S + r_1$

r_1 = internal base resistance of starved device

R_S = external padding resistance to minimize hogging

$V_1 = V_{TS} + \Delta V_p$

V_{TS} = saturation threshold voltage

ΔV_p = worst case production spread between V_T's

$V_2 = V_{TSH}$ = saturation threshold voltage for hog type device due to fan in

Figure 11. DCTL Piece-Wise Equivalent Circuit

Writing the node equations for Figure 11, one obtains:

$$I_A = \frac{V_{cc} - I_1 R_x - V_1}{R_L} \tag{23}$$

$$I_2 = \frac{I_1 R_x + V_1 - V_2}{r_2} = \frac{I_1 R_x + \Delta V}{R_x - \Delta r} \tag{24}$$

where

$\Delta V = V_1 - V_2$ (Total variation including production spread between base emitter threshold voltages.)

$\Delta r = r_1 - r_2 =$ (Total variation between hog and starved type base resistances.)

$R_x = R_s + r_1$ (Series padding resistance plus internal base resistance.)

The maximum number of hog type devices is:

$$N = \frac{I_A - I_1}{I_2} \tag{25}$$

and the fan out is $N + 1 = n$

Substituting equation (23) and (24) into equation (25), one obtains:

$$N = \left[\frac{V_{cc} - I_1 (R_x + R_L) - V_1}{I_1 R_x + \Delta V}\right] \frac{R_x - \Delta r}{R_L} \tag{26}$$

And for saturation:

$$I_1 = \frac{V_{cc}}{(R_L + r_{sat})\, B} \tag{27}$$

Substituting equation (27) into (26), one obtains:

$$N = \left\{\frac{V_{cc}\left[\frac{1-(R_x+R_L)}{B(R_L+r_{sat})}\right] - V_1}{\frac{V_{cc} R_x}{B(R_L + r_{sat})} + \Delta V}\right\} \frac{R_x - \Delta r}{R_L} \tag{28}$$

If one rewrites equation (28) in terms of V_{CES} (collector saturation voltage)

$$N = \left[\frac{V_{cc} - (V_{cc} - V_{CES})\frac{(R_x + R_L)}{B R_L} - V_1}{\frac{(V_{cc} - V_{CES})}{B R_L} R_x + \Delta V}\right] \left[\frac{R_x - \Delta r}{R_L}\right] \tag{29}$$

Equations (28) or (29) contain all the variables of interest and these equations can be plotted or mathematically manipulated to optimize the DCTL circuit; and in addition the relative importance of the device and circuit parameters can be found.

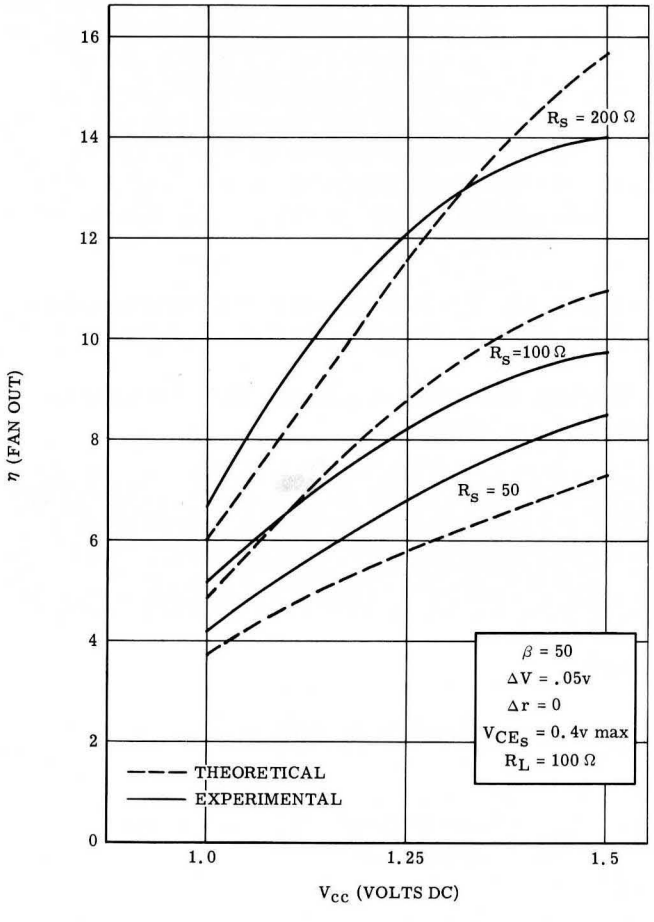


Figure 12. Fan Out versus Collector Supply Voltage

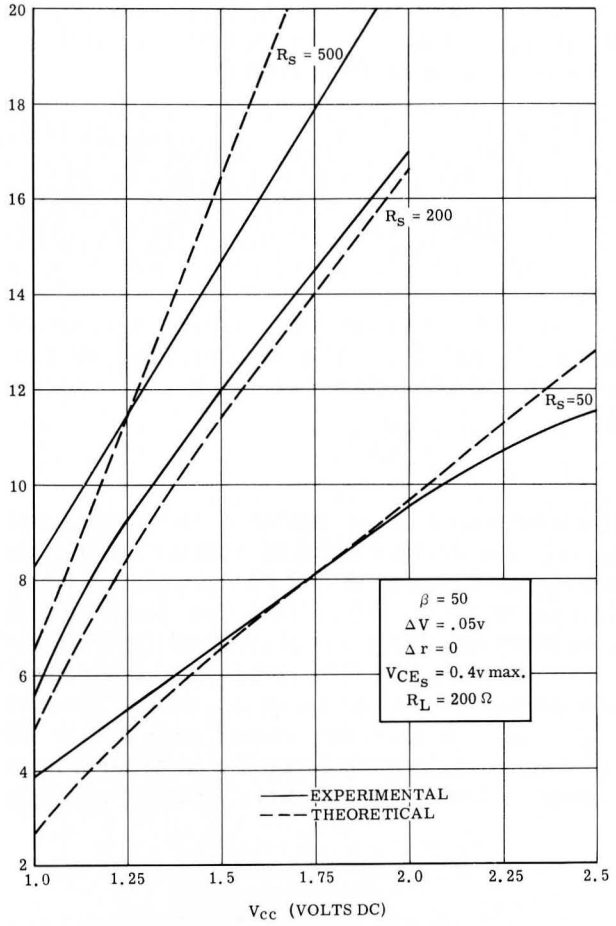


Figure 13. Fan Out versus Collector Supply Voltage

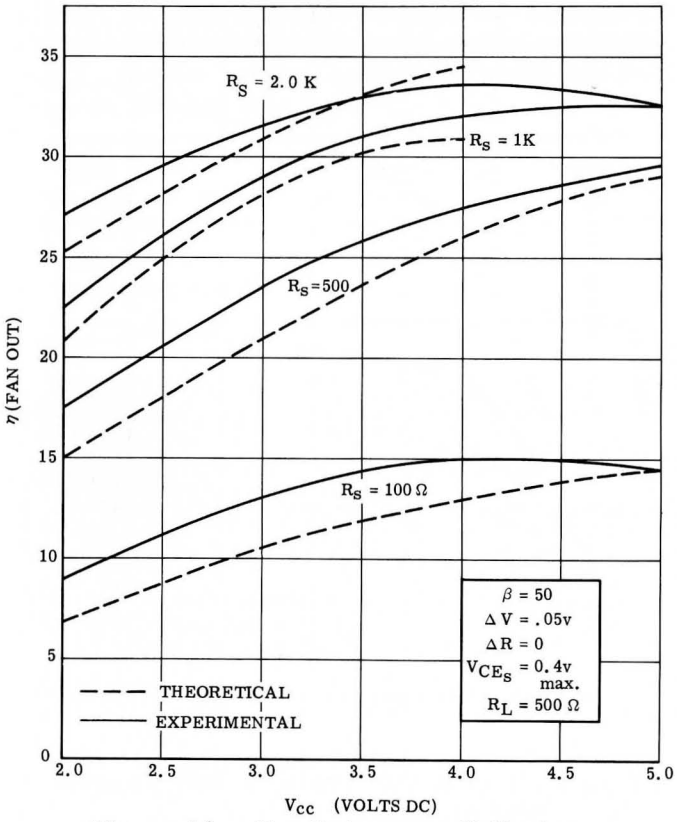


Figure 14. Fan Out versus Collector Supply Voltage

By the use of equation (29), Figures 12, 13 and 14 were plotted. The experimental data were obtained by paralleling (n-1) hog devices (load resistance = 10 R_L) with one starved device (load resistance = R_L). This test set-up simulates ΔV due to production spread (5 R_L) and a fan in of 5 (5 R_L). It should be noted that the fan in contribution to ΔV is more pronounced in high resistivity collector devices such as epitaxial transistors where α inverse is low (usually less than 0.2). If α forward $\approx \alpha$ inverse $\approx$ 1.0 the ΔV due to fan in would be zero, if one neglects the bulk resistances. From a steady state point of view a symmetrical transistor would be optimum for DCTL logic; however the storage time would be adversely affected.

We are now in a position to begin an optimization. If equation (29) is differentiated with respect to R_x/R_L (Appendix B) the resulting maximum occurs at:

$$\frac{R_x}{R_L} \approx \frac{B\ \Delta V}{V_{cc}} \left[\sqrt{\frac{1 + (V_{cc} - V_1)}{\Delta V}} - 1 \right] \qquad (30)$$

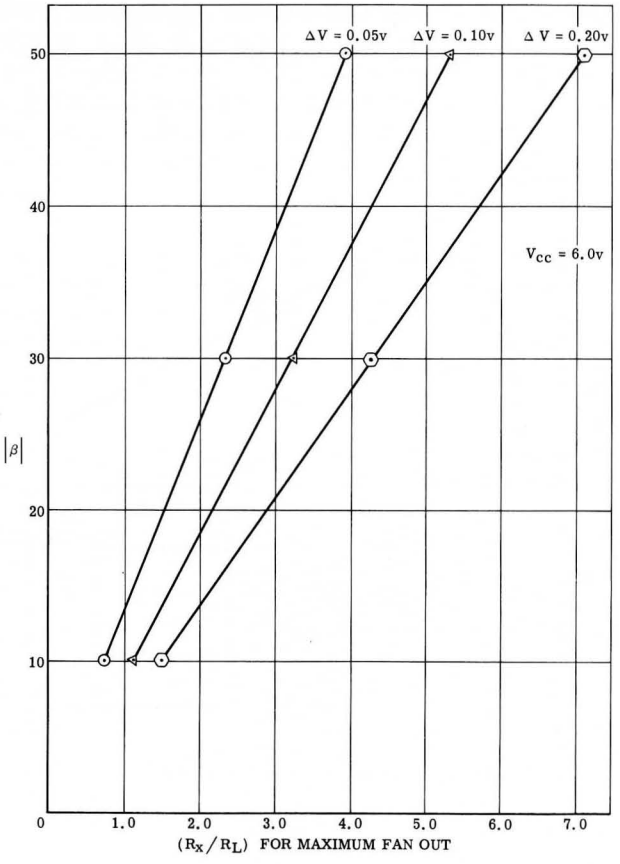


Figure 15. β versus R_X/R_L for Maximum Fan Out

Equation (30) is plotted in Figure 15 for an arbitrary V_{cc}. It is interesting to note that for any combination of the variables a unique value of series padding resistance exists to optimize n.

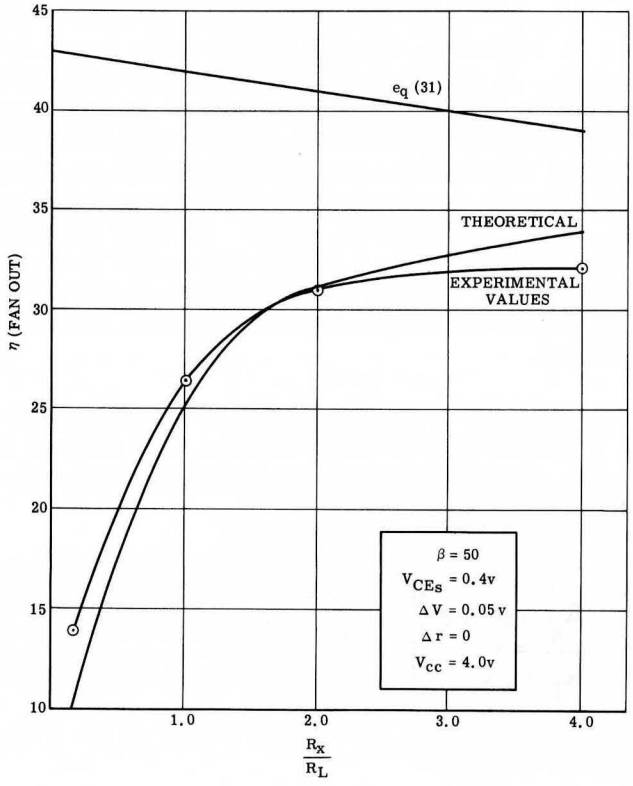


Figure 16. Fan Out versus R_X/R_L for $\beta = 50$

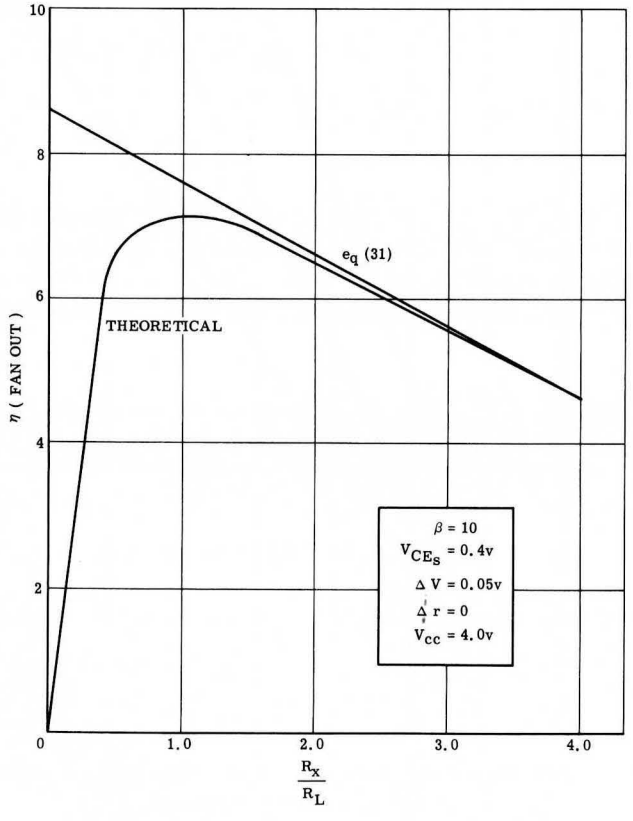


Figure 17. Fan Out versus R_X/R_L for $\beta = 10$

Fan out is plotted in Figures 16 and 17 with experimental data. If we assume n identical devices then equation (29) becomes:

$$n = \left(\frac{V_{cc} - V_1}{V_{cc} - V_{CES}} \right) \quad B - \frac{R_x}{R_L} \tag{31}$$

which is plotted as the theoretical maximum in Figures 16 and 17. The experimental data of Figure 16 substantiates the validity of equation (30).

The piece-wise linear analysis also enables one to clearly see the interrelation between the critical parameters. Figures 18 and 19 were plotted using equations (29) and (30). Here the designer can immediately note the tradeoff involved; for example a device with a $\Delta V = 0.05$ and $B = 10$ is far more desirable for fan out than the device with $\Delta V = 0.15$ and $B = 50$. In fact, the device with $\Delta V = .15$ would require extremely large B's in order to have comparable fan out capability. Solving equation

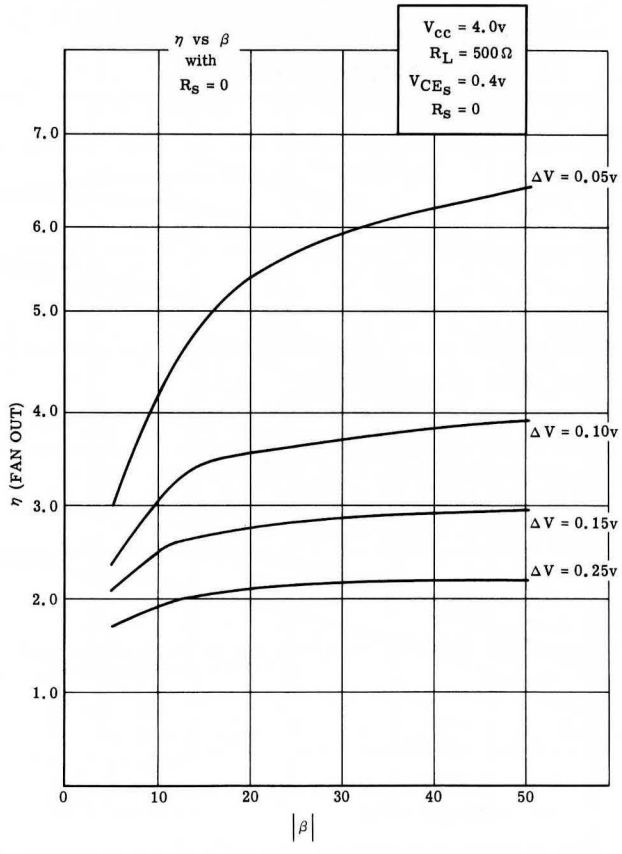


Figure 18. Fan Out versus β with No Series Padding Resistance

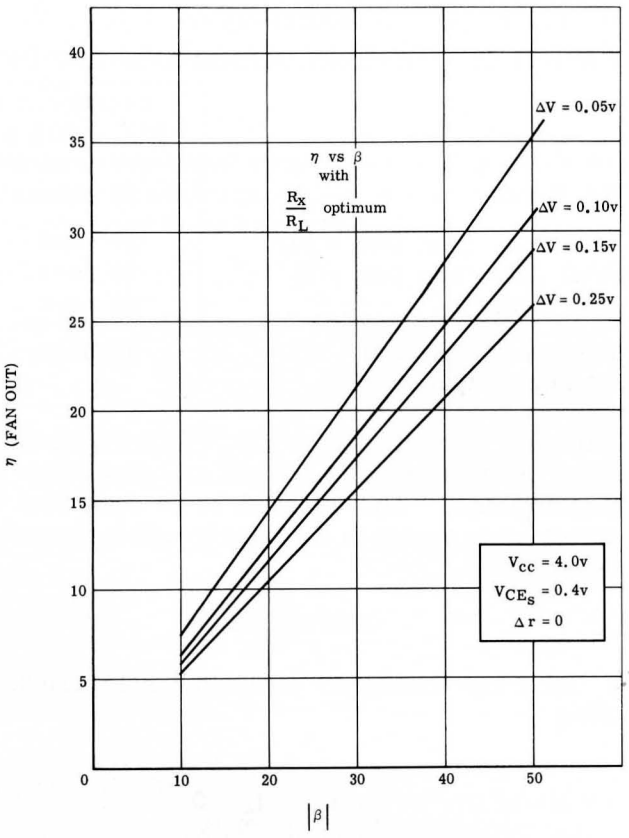


Figure 19. Fan Out versus β with Optimum R_X/R_L

(29) using the R_X/R_L ratio from equation (30), Figure 19 was obtained. Comparing Figures 18 and 19, the improvement in fan out by optimizing R_X/R_L can be noted. Again the tradeoff involved between ΔV and B is apparent.

Other plots could be generated to show the influence of the variables contained in equation (29). For example, the effects of Δr on n were investigated but found to be less significant than those previously discussed.

To show that the steady state design was compatible with transient operation, an eight bit parallel-parallel adder was constructed using the design outlined here.

If speed is of primary concern then it is obvious that R_X should go to zero if storage time is to be minimized, thus some compromise can be made between fan out and speed. For example, noting that the maximum of the Figure 16 curve is somewhat broad, there is not too great a degradation of fan out if the optimum value of R_X is not selected for that particular case. Herein is the advantage of an analysis such as described; it allows the designer to note the tradeoffs involved between the various variables of interest. A family of curves such as Figure 17 could be plotted for various B and V_{CC} values, or the second deviative of equation (29) could be taken with respect to R_X/R_L to indicate the rate of change from the optimum.

The adder had a maximum fan out of 13 and a fan in of 8. Table IV is a partial compilation of transient data observed. The adder unit performed satisfactorily over a temperature range of -50°C to + 100°C.

Conclusions

The piece-wise linear analysis has been used to analyze both saturated and non-saturated logic circuits with considerable experimental data verifying the validity of this approach. General analytical expressions describing the circuits of interest were obtained and used to optimize the design.

With current mode logic the break points were predicted with reasonable accuracy and a note of significant interest is that a theoretical minimum on the transition width is clearly defined by

TABLE I

ORDER DIODE BREAK-POINT	e_1	eo_2	eo_1	e_x	ib_1
D_1	$-\left(\frac{E_B+Vc_2-V_T}{RE}\right)\left(\frac{re+rb}{\beta}\right)+E_B$	$Vc_1-\frac{RL}{RE}\left[E_B+Vc_2-V_T\right]$	Vc_1	$-\left[\frac{E_B+Vc_2-V_T}{RE}\right]\left[\frac{re+rb}{\beta}\right]+E_B-V_T$	0
D_2	$\frac{E_B+Vc_2-V_T}{RE}\left[\frac{re+rb}{\beta}\right]+EB$	Vc_1	$Vc_1-\frac{RL}{RE}\left[E_B+Vc_2-V_T\right]$	$-V_T+E_B$	$\frac{E_B+Vc_2-V_T}{\beta\ RE}$
D_3	$\frac{Vc_1+Vc_2}{\frac{RL}{RE}}+V_T-Vc_2$	Vc_1	$Vc_1-\frac{(Vc_1+Vc_2)}{\frac{RE}{RL}+1}$	$\frac{Vc_1+Vc_2}{\frac{RL}{RE}+1}-Vc_2$	$\frac{Vc_1+Vc_2}{\beta(RL+RE)}$

equation (19). The significance of the transistor parameters are easily noted for worst case design.

The piece-wise linear analysis applied to a saturated DCTL circuit resulted in expressions which described optimum values for the variables of interest. A maximized fan out could not be easily realized by non-analytical methods. The simplicity of the piece-wise linear analysis should make it an excellent tool for the logic circuit designer. It should be obvious that if more accuracy is desired additional segments could be added for a better fit to the transistor characteristics.

The piece-wise linear analysis has:

1. Enabled optimization by analytical means.

2. Clearly described the interrelationships of significant parameters such as B and ΔV.

3. Offered a simple and accurate method for worst case designing.

TABLE II

CALCULATED BREAKPOINT CKT PARAMETERS FOR THE CIRCUIT CONDITIONS OF FIG. 8

Diode Break-Points	e_1 (volts)	e_{o2} (volts)	e_{o1} (volts)	ib_1 (ma)
D_1 Cal.	0.44	1.05	2.0	0
Exp.	0.42	1.1	2.0	0
D_2 Cal.	0.56	2.0	1.05	0.127
Exp.	0.58	2.0	1.1	0.14
D_3 Cal.	1.33	2.0	0.64	0.182
Exp.	1.24	2.0	0.76	0.19

(All experimental data approximately ± 10 percent)

TABLE III

TRANSISTION VOLTAGE DATA FROM FIGURE 8

R_e (ohms)	Δe (volts) (from Fig. 8)	Δe (volts) (calculated) equation (19)
220	.19	.212
620	.15	.143
940	.12	.116
15K	.11	.105
62K	.11	.104

TABLE IV

PARALLEL-PARALLEL ADDER AVERAGE DELAY

	t Average delay (50% - 50% pts)
OR Gate	26 nsec
AND Gate (Fan Out = 13)	27 nsec
AND Gate (Fan Out = 3)	15 nsec
Half Adder	22 nsec
From input to eigth bit sum output	72 nsec

This data was obtained on a DCTL parallel parallel eight bit adder using a HP 185 sampling scope for measurement. The intention is to show that the steady state design is compatible with the transient operation.

APPENDIX A

Using the breakpoint analysis for Figure 3, we have:

$$\text{BP of } D_1 \quad V_B = V_T \quad i_b = 0 \tag{33}$$

$$\text{BP of } D_2 \quad V_{cc} = Bi_b\, m\, R_L + (B+1)\, i_b\, r_e$$

m=fan in on the collector node

$$I_b = \frac{V_{cc}}{BmR_L + (B+1)r_e} \tag{34}$$

$$V_B = \frac{V_{cc}}{BmR_L + (B+1)r_e}\left[r_b + (B+1)r_e\right] + V_T$$

These are the breakpoints of Figure 2, where the assumptions for Figure 2 are:

$B + 1 \approx B$

$r_b >$ parallel combination of r_e and mR_L in the saturation region.

The extrapolation of the $1/r_b$ line to the V_B axis is easily found to be:

$$V_{TS} \approx V_T + \frac{V_{cc} r_e}{mR_L} \tag{35}$$

Where V_{TS} can now be used to represent the saturated case by a two segment linear approximation.

Writing the node equations for Figure 9 and letting the s subscript denote the starved part of the circuit and h the hog part we have:

$$V_{B_s} = \frac{V_{cc}}{B_s R_{L_s}} (r_{b_s} + B_s r_{e_s}) + V_{T_s} \tag{36}$$

$$I_{B_s} = \frac{V_{cc}}{B_s R_{L_s}} \tag{37}$$

$$I_{B_h} = \left[\frac{V_{cc}}{B_s R_{L_s}} (r_{b_s} + B_s r_{e_s}) + V_{T_s} - V_{TS_h} \right] \left[\frac{1}{r_{b_h} + r_{e_h}} \right] \tag{38}$$

$$I_A = \frac{V_{cc} - V_{B_s}}{R_L} = \frac{V_{cc} - \frac{V_{cc}}{B_s R_{L_s}} (r_{b_s} + B_s r_{e_s}) - V_{T_s}}{R_L} \tag{39}$$

Letting $R_L = R_{L_h}$ for worst case

$$N = \frac{I_A - I_{B_s}}{I_{B_h}} = \frac{V_{cc} - \frac{V_{cc}}{B_s R_{L_s}} (r_{b_s} + B_s r_{e_s}) - V_{T_s}}{\frac{V_{cc}}{B_s R_{L_s}} (r_{b_s} + B_s r_{e_s}) + V_{T_s} - V_{TS_h}} \left[\frac{r_{b_h} + r_{e_h}}{R_{L_h}} \right] \tag{40}$$

For the worst case the following conditions would exist:

$$R_{L_h} > R_{L_s}$$

$$r_{b_s} > r_{b_h}$$

$$r_{e_s} > r_{e_h}$$

$$V_{T_s} > V_{T_h}$$

$$B_s > B_h$$

APPENDIX B

from equation (20)

To optimize N with respect to Rx set $\frac{dN}{d\left(\frac{Rx}{R_L}\right)} = 0$

$$N = \frac{\left[V_{cc} - \left(\frac{V_{cc} - V_{CES}}{B} \right) - V_1 \right] R_L - \left(\frac{V_{cc} - V_{CES}}{B} \right) \frac{Rx}{R_L} + \frac{\left(\frac{V_{cc} - V_{CES}}{B} \right) \left(\frac{Rx}{R_L} \right)^2}{\Delta V}}$$

Rewriting in simplified notation,

$$N = \frac{a\left(\frac{Rx}{R_L}\right) - b\left(\frac{Rx}{R_L}\right)^2}{b\left(\frac{Rx}{R_L}\right) + \Delta V} \tag{41}$$

$$\frac{dN}{d\left(\frac{Rx}{R_L}\right)} = \left(\frac{Rx}{R_L}\right)^2 + \frac{2}{b}\frac{\Delta V}{R_L}\frac{Rx}{R_L} - \frac{a}{b^2}\frac{\Delta V}{R_L} = 0 \tag{42}$$

$$\frac{Rx}{R_L} = \frac{\Delta V}{b}\left[\pm\sqrt{1+\frac{a}{\Delta}} - 1\right] \tag{43}$$

$$\frac{Rx}{R_L} = \frac{B\ \Delta V}{(V_{cc}-V_{CES})}\left[\pm\sqrt{1+\left[\frac{V_{cc}(B-1)+V_{CES}-BV_1}{B\ \Delta V}\right]} - 1\right] \tag{44}$$

$$\left(\frac{Rx}{R_L} \approx \frac{B\ \Delta V}{(V_{cc}-V_{CES})}\left[\pm\sqrt{1+\frac{V_{cc}-V_1}{\Delta V}} - 1\right]\right. \tag{45}$$

REFERENCES

1. "Worst Case Design Equations for Transistor Logic Circuits", C. W. Campbell, Jr., May 13, 1959, E.D.

2. "The Transistor NOR Circuit", W. D. Rowe, 1957 IRE WESCON Convention Record, Part 4, pp. 231-245.

3. "Designing a Transistor NOR Circuit For Minimum Power Dissipation", E. L. Cox, Electronic Design, March, 1959, pp. 42-45.

4. "TRADIC Computer Research Program Report", Easley, et al, prepared by Bell Laboratories.

LIST OF SYMBOLS

n = fan out (total number of bases being driven from a single load resistor).

m = fan in (total number of collector per load resistor).

N = n - 1 = (number of hog bases being driven from a single load resistor).

B = D.C. common emitter current gain.

α = D.C. common base current gain.

r_c = reverse biased collector resistance.

r_s = collector saturation resistance.

r_b = internal base resistance.

r_e = instantaneous slope of the $V_B - I_B$ characteristic.

K = Boltzmann constant = 1.38×10^{-23} Joules per degrees Kelvin.

T = temperature in degrees Kelvin.

q = electronic charge = 1.6×10^{-19} Couloumbs.

V_T = the threshold of conduction of the base emitter junction as defined in Figure 2.

V_{TS} = the intercept of the extrapolated $1/r_b$ line with the V_B axis. When dealing with the saturated case this allows the base emitter to be represented by a new two line segment.

BIBLIOGRAPHY

Phillips, A. B.: Transistor Engineering - and Introduction to Integrated Semiconductor Circuits, McGraw-Hill Book Company, New York, July, 1962.

Geller (et al): "A General Junction Transistor Equivalent Circuit For Use In Large Signal Switching Analysis", IRE Transactions of Electronic Computers, December, 1961, pp. 670-679.

Yourke, H.: "Millimicrosecond Transistor Current Switching Circuits", IRE Transactions on Circuit Theory, September, 1957, pp. 236-240.

Beter, R. H., et al: "Surface Barrier Transistor Switching Circuits", 1955 IRE Convention Record, pp. 139-145.

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