MOTOROLA
Semiconductor Products Inc.

AN-848
Application Note

AN EVALUATION SYSTEM FOR HIGH-SPEED A-D AND D-A CONVERTERS

The recent availability of low cost, high-speed monolithic analog-to-digital and digital-to-analog converters have opened new opportunities which until now have been prohibitively expensive or impractical. One of the major areas of application is in digitizing television signals at nearly all phases of the television system.

This application note describes a printed circuit board developed for the purpose of evaluating the converters at the component level, as well as at the system level. A functional description of the components, and the theory involved is included.

INTRODUCTION

With the recent introduction of monolithic Flash (high-speed, parallel operation) analog-to-digital converters, and monolithic high-speed (<20 ns settling time) digital-to-analog converters, the means to digitize and reconstruct (to analog form) high-speed signals without the need for bulky and expensive equipment, is at hand. Included in the range of signals discussed are video speed signals, including composite video. Digitizing video signals provides several advantages to the studio engineer, which include maintaining picture quality, facilitating the manipulation of the picture via microprocessor to obtain special effects, and time base correction capability.

Digitizing an analog signal, and the subsequent reconstruction to analog form, involve many disciplines of mathematics and electronics. A thorough study involves the Nyquist Sampling Theorem, Fourier analysis, and the study of beat frequencies and harmonics. Techniques for handling high-speed signals are necessary, along with the need to maintain high-accuracy and noise-free operation in a noisy environment.

The purpose of this application note is to describe the capabilities and operation of the MC10315 and the MC10317 flash A-D converters, and the MC10318 high-speed D-A converter, as well as their application in an Evaluation Board designed for their use at frequencies which include video rates. The design of the printed circuit board accounts for the need to maintain separate the analog and digital portions of the circuit, as well as proper handling of critical paths. The flexibility of the design permits digitizing signals of any frequency from dc to 5 MHz, at sampling rates up to 15 MHz.

COMPONENT DESCRIPTION

Flash A-D Converter

The MC10315 and MC10317 are 7-bit flash A-D converters, whose operation differ only in the overrange function. In the MC10315, the outputs remain high (Logic "1") when an overrange condition is reached, whereas in the MC10317 the outputs switch to low

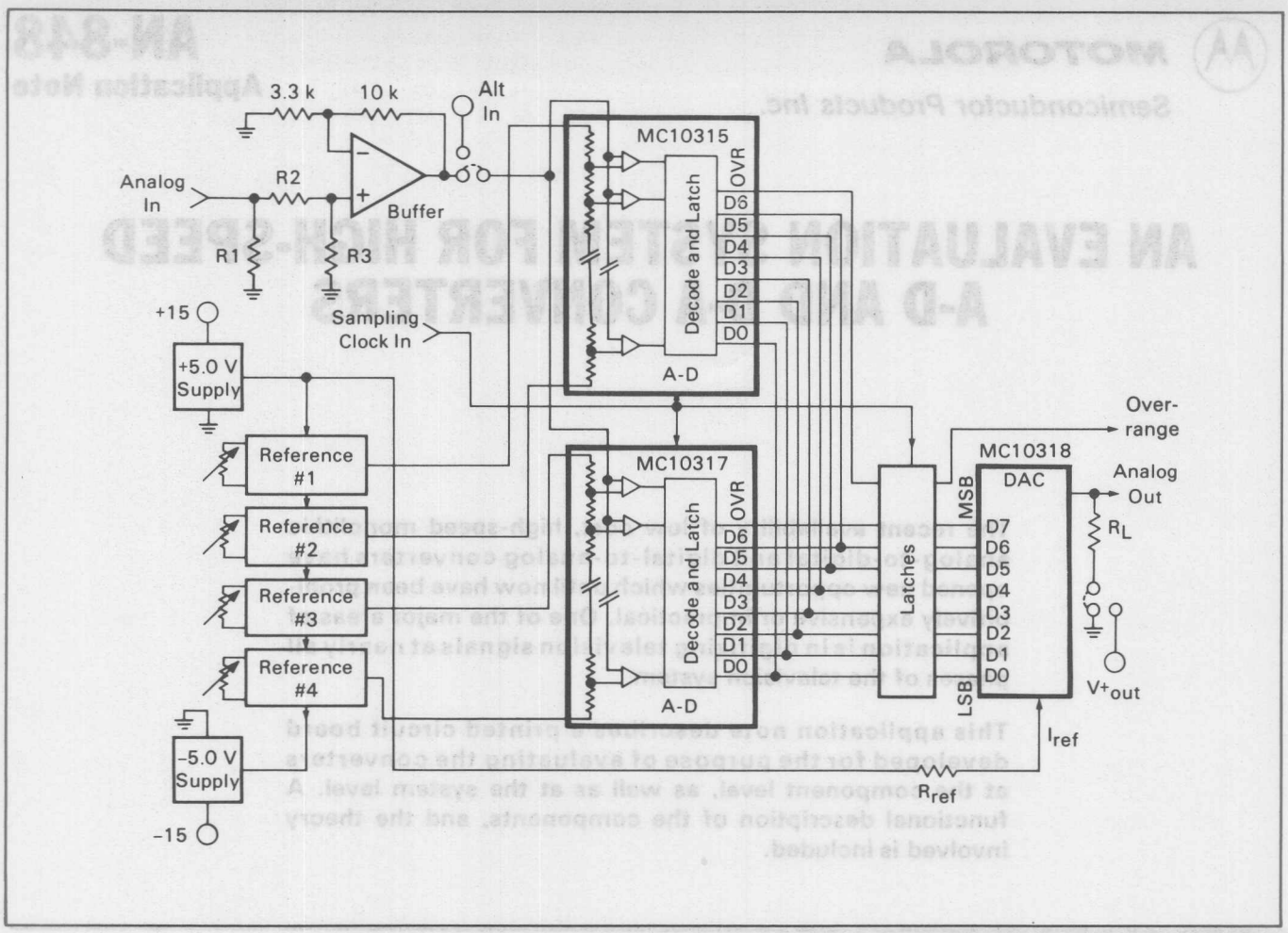


FIGURE 1 — Evaluation System Block Diagram

(Logic "0") on reaching an overrange condition. This difference is necessary in order to be able to parallel two devices into an 8-bit configuration.

The digital output of a flash converter is determined by comparing the analog input to a voltage on a resistor divider reference network. The digital outputs are Logic "0" when the analog input is within 1/2 LSB of the most negative reference voltage (V_{RB}), or less. The outputs are at a logic "1" when the input is within 1-1/2 LSB to 1/2 LSB below the most positive reference voltage (V_{RT}). In between these values are the remaining 126 possible binary codes. When the input exceeds V_{RT} - 1/2 LSB, the overange output is high. The reference span (V_{RT}-V_{RB}) must be less than 2 volts, but preferably greater than 1 volt, within an absolute voltage range of +2 V to -2 V.

The Flash converter requires a clock input. When the clock is high, the 128 input comparators are latched (effectively a sample-and-hold function), allowing the subsequent logic to decode their outputs into a 7-bit binary code. During this time, the output latches are transparent, and the output data is not stable or valid for the first (approximate) 43 ns. When the clock is low the output latches are latched, and the comparators are allowed to resume tracking the input signal. (See Figure 2.) Minimum high time is 44 ns, and minimum low time is 25 ns.

The outputs and clock signal are ECL compatible, the outputs therefore requiring pull-down resistors. The analog input impedance is 5 kΩ minimum in parallel with 70 pF, and the input signal may be bipolar or unipolar.

High-Speed D-A Converter

The MC10318 is a high-speed, 8-bit D-A converter, whose output settles, typically, in 10 ns. The inputs are ECL compatible, and no clock is required. The output (I_O) varies with the digital input in 256 steps from 0 to 51 mA when a reference current of 3.2 mA is supplied to the device. $\overline{I_O}$ is the complementary output, varying in opposite phase to I_O. Both outputs are current sources.

The voltage at either output may fall within the range of +2.5 V to -1.3 V by selection of appropriate load resistor and pullup voltage. Since the output current flows **into** the device, increasing the output current causes the output voltage to swing negative.

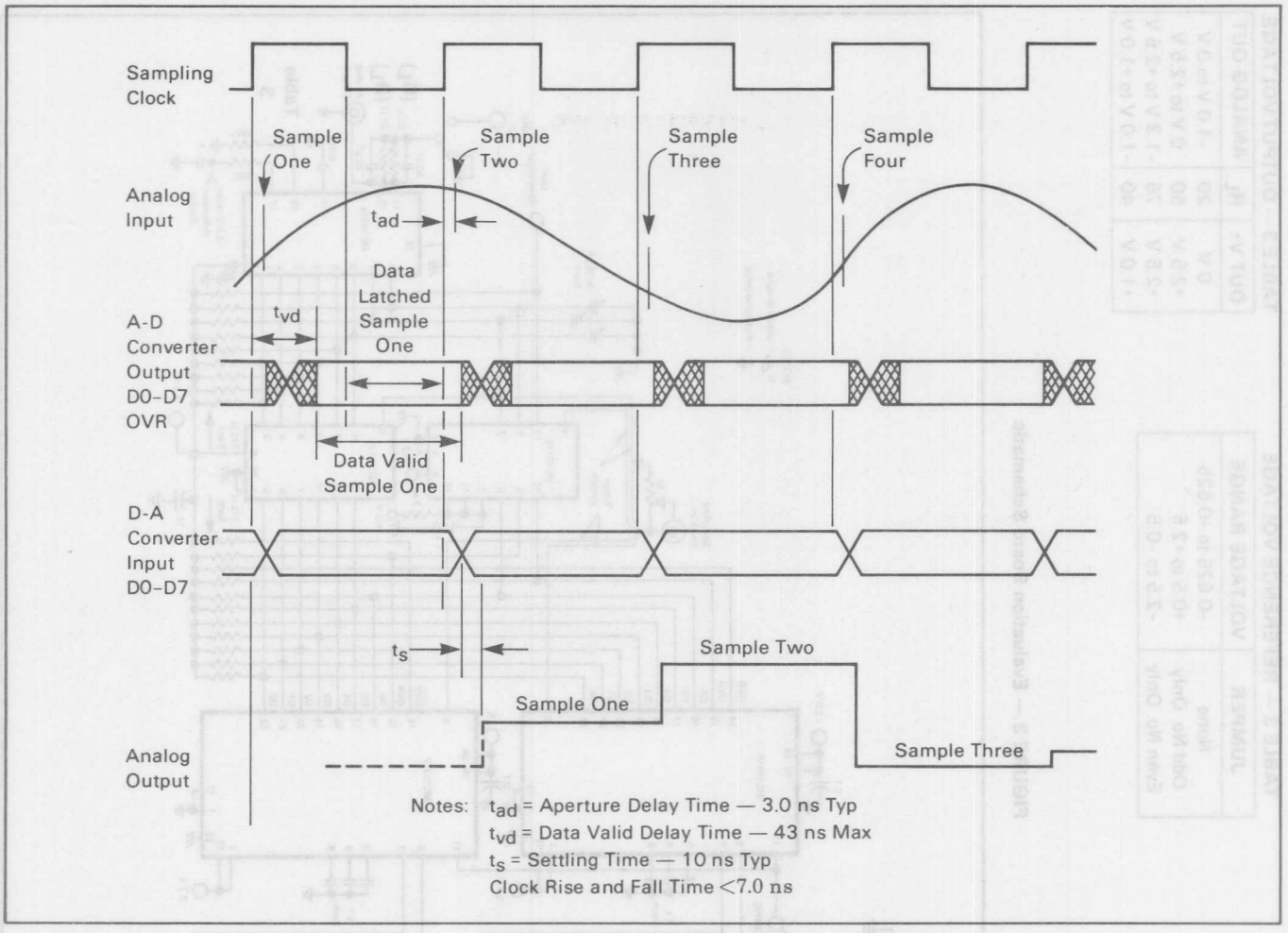


FIGURE 2 — A-D and D-A Conversion Timing

EVALUATION BOARD

Block Diagram

See Figure 1. The board has provisions for the following:

- One MC10315 A-D **and** one MC10317 A-D, to allow digitizing to 8-bit resolution. Either device may be deleted for 7-bit operation;
- One MC10318 D-A;
- Latches to transfer the data from the A-D to the D-A;
- Buffer/amplifier for the analog input signal;
- Adjustable references for the A-D converters;
- Reference current for the D-A converter;
- Various input voltage ranges and input impedances;
- Various output voltage ranges and output impedances.

By installing appropriate components, the board may be configured to produce any of the following functions:

- 8-bit A-D and D-A;
- 7-bit A-D and D-A;
- 8-bit A-D only;
- 7-bit A-D only;
- 8-bit D-A only.

Input Section

The input amplifier permits matching the input impedance to the source impedance, as well as amplifying low-level signals, where that is necessary. Selection of input resistors R1, R2, and R3 should be made from Table 1. Where the signal amplitude does not match exactly with a value in the table, the next higher range should be selected. The A-D references (described later) can then be adjusted to match the signal level.

The amplifier has been configured for stable operation, at a gain of +4, while driving two A-D converters (5 K ‖ 70 pF each). The -3 dB point is approximately 10 MHz.

A dc blocking capacitor is provided at the Analog In input, but may be bypassed by the user in the case of low frequency or dc signals.

The ALT IN connector provides a means of applying the input signal directly to the A-D converters, bypassing the amplifier. If the signal has proper amplitude (1-2 volts p-p for 7-bits, 2-4 volts for 8-bits), and has sufficient drive capability, this input can be used. The jumper adjacent to the connector must be relocated per Figure 13.

TABLE 1 — INPUT SELECTION

P-P V_{IN}	R_{IN} = 50 Ω			R_{IN} = 75 Ω			R_{IN} = 600 Ω			R_{IN} = 1000 Ω		
	R1	R2	R3	R1	R2	R3	R1	R2	R3	R1	R2	R3
1	51	0	∞	75	0	∞	1200	0	1200	1000	0	∞
2	51	1300	1300	100	150	150	1000	750	750	2000	1000	1000
4	51	3000	1000	91	300	100	1200	910	300	2000	1500	510
5	51	3000	750	150	120	30	1000	1200	300	3000	1200	300
10	51	2700	300	100	270	30	750	2700	300	1500	2700	300

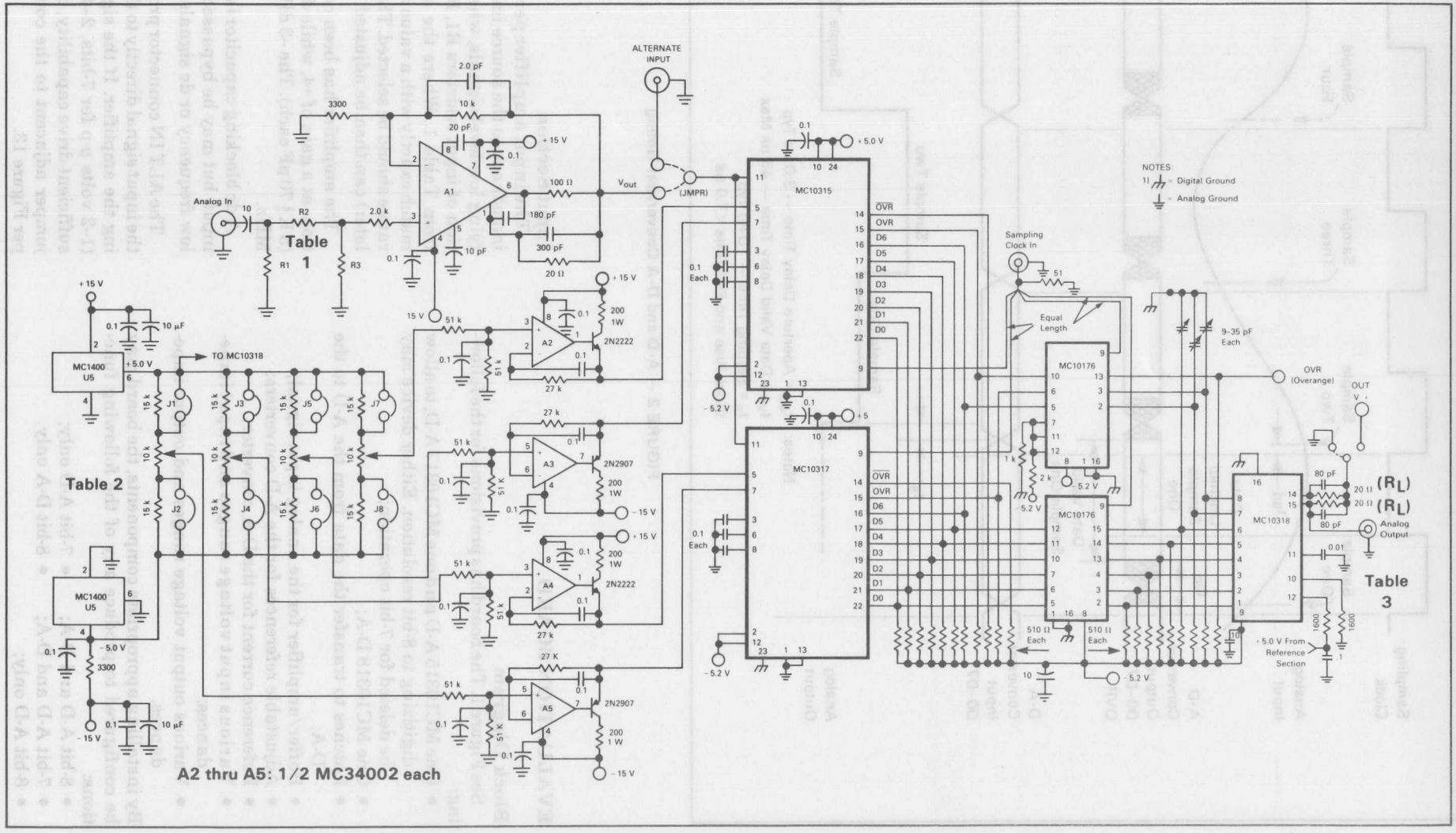
TABLE 2 — REFERENCE VOLTAGE

JUMPER	VOLTAGE RANGE
None	−0.625 to +0.625
Odd No. Only	+0.5 to +2.5
Even No. Only	−2.5 to −0.5

TABLE 3 — OUTPUT VOLTAGE

OUT V+	R_L	ANALOG OUT
0 V	20	−1.0 V to 0 V
+2.5 V	50	0 V to +2.5 V
+2.5 V	76	−1.3 V to +2.5 V
+1.0 V	40	−1.0 V to +1.0 V

FIGURE 3 — Evaluation Board Schematic



Reference Section

This section is designed to provide the reference voltages to the MC10315 and MC10317 A-D converters, and the reference current to the MC10318 D-A converter.

The two MC1400U5 devices provide the precise and stable +5.0 Volts and -5.0 Volts. This 10 Volt difference is spanned by 4 sets of 15 kΩ resistors and 10 kΩ pots. The jumpers across the 15 k resistors allow shifting the available range of adjustment per Table 2. The output of each trimpot goes to a buffer/current driver designed to accommodate the 32 mA current required by the A-D converters' reference ladder. Pin 5 (V_{RT}) or Pin 7 (V_{RB}) of each A-D should be monitored with a high resolution DVM while making adjustments. V_{RB} should **never** be allowed to be more positive than V_{RT}.

The +5.0 Volt supply mentioned above supplies the reference current to the MC10318 D-A converter via a current setting resistor.

Where only one A-D converter is required (7-bit operation), normally the MC10317 will be installed. In this case the upper MC34002 dual op-amp, and appropriate trimpots and resistors may be deleted.

Where only the MC10318 D-A converter is to be installed, only the MC1400U5 supplying the +5.0 Volts is required. The two MC34002's, the trimpots and associated components may be deleted.

A-D Convertion Section

A) 7-Bit Operation

Normally the MC10317 will be installed for 7-bit digitizing, along with the appropriate reference components. The two MC10176 latches are required, along with the pull-down resistors on the outputs of the A-D converter and the latches, and all associated bypass capacitors. The reference voltages (V_{RT} and V_{RB}) are to be adjusted to match the peak-to-peak values of the input signal at Pin 11. The references must be maintained within the range of ±2.0 Volts, with a difference of no greater than 2.0 Volts.

B) 8-Bit Operation

Both the MC10315 and MC10317 are to be installed, along with the four reference circuits, pull-down resistors, bypass capacitors, and the MC10176 latches. The references are to be adjusted such that V_{RT} of the MC10315 is the most positive, V_{RB} of the MC10315 equals V_{RT} of the MC10317, and V_{RB} of the MC10317 is the most negative. All four references must be within the range of ±2.0 Volts, with a differential of no greater than 2.0 Volts across each device. The references may thus be set at +2.0 V to 0 V, 0 V to -2.0 V, +1.0 V to -1.0 V, +2.0 V to -2.0 V, +0.5 V to -1.5 V, etc. Normally the voltage difference (V_{RT}-V_{RB}) is to be the same for each device in order to provide equal differential for each of the 256 digitized steps. Misadjustment of the midpoint of the reference span will result in a discontinuity at the midpoint of the output waveform (see Figure 4).

The outputs of the A-D converters are WIRED-OR to provide the 8-bit binary code. The OVERRANGE of the MC10317 is the MSB of the 8-bit code, while the OVERRANGE of the MC10315 remains an overrange indicator.

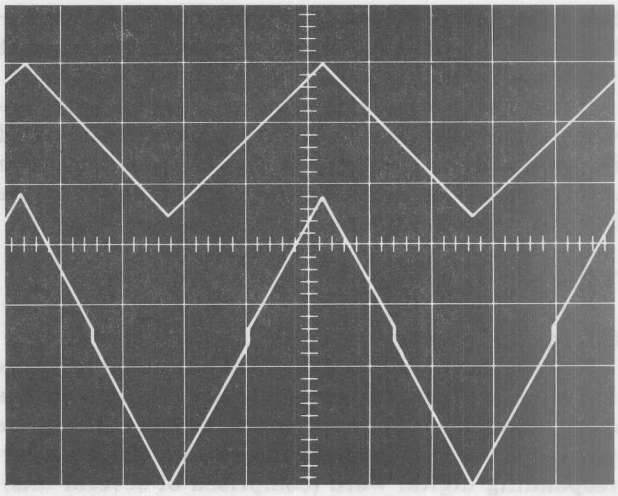


FIGURE 4 — Discontinuity due to misadjustment of A-D references
Upper Trace = Analog Input
Lower Trace = Analog Output

C) Clock Input

The sampling clock signal is to be at ECL levels (V_{IH} = -0.8 V, V_{IL} = -1.8 V) at a frequency determined by the application. The CLK input BNC connector is terminated with 51 ohms, and the traces leading to the 4 devices are (intentionally) equal length.

D) Digital Output

If the MC10318 D-A converter is not to be included, a connector strip is installed in pin positions 1-8 of the MC10318 location to obtain the digital output signals.

D-A Converter Section

The MC10318 D-A converter receives its digital input information from the latches, after the rising edge of each clock signal. (See Figure 2.) The purpose of the latches is to ensure simultaneous transmission of the 8-bits to the MC10318, and to block the outputs of the A-D converters during the time they are invalid.

Even though the 8 bits are received by the MC10318 simultaneously, glitches can still occur on its output due to internal timing differences. Compensation for the timing differences is achieved, in part, by adjustment of the variable capacitors connected to the upper 3 bits. The most noticeable glitches occur at 1/4, 1/2, and 3/4 scale. If the glitches cannot be reduced to a satisfactory level for the application, a sample-and-hold circuit would then be required at the Analog Output.

The complementary current outputs are loaded with 20 ohm resistors each, resulting in an output voltage swing of 0 to -1 Volt (current flows **into** the MC10318). Larger voltage swings can be obtained by changing the load resistors, and applying a pullup voltage to the V+ OUT connector. (See Table 3.) The jumper near

the ANALOG OUT connector must be located as per Figure 13. The output voltage is limited to a range of +2.5 V to -1.3 V.

If only the D-A function is to be evaluated (A-D Converters not installed), a connector strip is installed in pin positions 15-22 of the MC10317 location. The digital input (ECL level) can then be applied to the board at this connector.

THEORY

Sampling Theory

The process of digitizing an analog signal involves the concept of sampling (ideally instantaneously) the signal at various points with respect to time. The value measured at each sample is then converted into a corresponding digital word (comprised of several bits). While the analog signal represents a continuous, unbroken stream of information, the digital words are available only at a fixed, finite rate (the sampling rate) and each word represents a fixed value for a period of time. In order to reconstruct the information contained in the digital words, a number of the words must be "read" (converted to an analog value), and the discrete steps must (in some cases) be "averaged out" (by filtering or other means). See Figures 7 and 8. Obviously the higher the sample rate, compared to the frequency of the analog signal, the more information that will be available in a given period of time. See Figures 5 and 7. The Nyquist Sampling Theorem states that the sampling rate must be equal to or greater than twice the frequency of the highest frequency component of the signal of interest. Sampling at a rate less than the Nyquist limit generally will not permit truthful reproduction of the original analog signal.

The number of bits resolution largely determines the accuracy to which the original analog signal can be reconstructed. In an 8-bit system, there are 256 discrete steps, and therefore each digital code represents a range of 0.39% of the total available signal. As a result, each sampling and digitizing of an analog signal is accompanied by an uncertainty of ±0.195% (±0.39% for a 7-bit system, ±0.097% for a 9-bit system). The uncertainty shows up as a possible error in the amplitude of the reconstructed signal compared to the original signal.

The timing differences between the sampling clock signal and the analog signal causes another type of uncertainty (or error). In the cases where the two signals are not synchronized (the usual mode of operation), the reconstructed analog output will appear to have a phase jitter in an amount equal to the period of the sampling clock. This effect is easiest seen by applying a square wave to the analog input, and observing the jitter at the analog output (see Figure 9). The main effect of the timing uncertainty is the generation of beat frequencies, and harmonics. The greater the difference between the sampling frequency and the signal frequency, the easier it is to contend with the additional unwanted frequencies. But where the sampling rate is a small multiple (2-10) of the signal frequency, the beat frequencies become a very significant part of the output signal (see Figure 6).

In the cases where the sampling rate is locked to the input signal frequency, beat frequencies and harmonics will still be generated, but the timing uncertainty (apparent phase jitter) can be eliminated. For example, a sine wave sampled at exactly twice its frequency will result in a constant amplitude square wave when reconstructed. Recapturing the original sine wave will obviously require filtering at the fundamental frequency. (In the special case where sampling occurs at the zero-crossing point, the output will be a dc signal).

In the processing, or storing of the digital words, prior to reconstruction to analog form, the transmission rates of the words, or bits, becomes a significant factor. If the MC10317 is made to sample at its maximum frequency (≈15 MHz), it will be outputting data at the rate of 15 Megawords per second. If the data is to be transmitted serially, a transmission rate of 105 Megabits per second results (120 Megabits per second for an 8-bit system). A bandwidth of half the bit rate is required, resulting in bandwidth requirements much higher than that for the original analog signal. This fact is one of the major costs to be paid for the benefits of a digital signal.

Digital Video Signals

The highest frequency signal of interest to be digitized in a video signal is the 3.58 MHz sine wave used for the color reference and the subsequent color information. Discussions have been conducted as to whether the signal should be sampled at 3X (10.7 MHz) or at 4X (14.3 MHz). Currently the trend seems to support sampling at 4X, and some manufacturers of VTR's have used 4X to date.

Considerable discussion has been conducted as to the minimum number of bits resolution to which a video signal should be digitized. A general agreement is that 6 bits (64 quantizing levels) is the minimum number of bits which can maintain an acceptable picture. While 7 bits is being considered for many applications, 8 bits digitizing appears to be preferred in order to allow for the cumulative differential phase and gain errors resulting from multiple processing of the digital signals.

As mentioned in the previous section (Sampling Theory), digitizing a signal involves uncertainties, which show up as errors at the output. In video signals, the results are differential phase and gain errors, and a luminance shift. Per reference 1, an ideal 8-bit digitizing system will produce maximum errors of ±4.3% differential gain, ±2.5° differential phase, and ±0.33 IRE unit luminance shift. These figures are based on a 10 IRE signal (20 IRE units p-p) within an available field of 166 IRE units, sampled at 3X. The luminance shift results from digitizing the dc component of the video signal with an uncertainty of ±1/2-LSB, and is independent of the color information. The maximum gain and phase errors occur only under certain sampling conditions, and in fact do not occur simultaneously. When instantaneous gain error is at a maximum, phase error is zero, and vice-versa. Since the sampling signal is asynchronous to the video information, a distribution of each error will result,

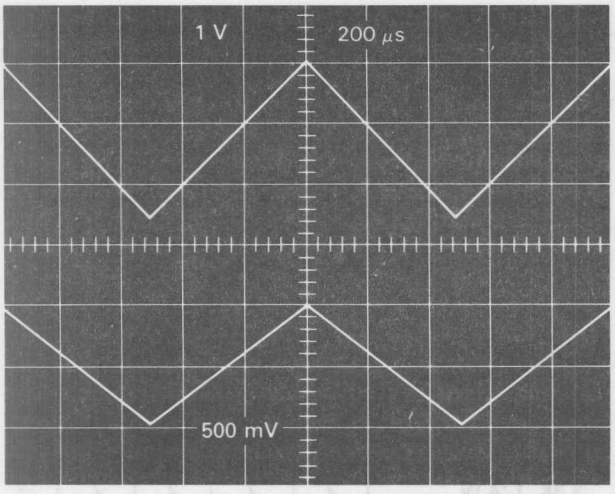


FIGURE 5 — 1.0 kHz Triangle Sampled at 10 MHz

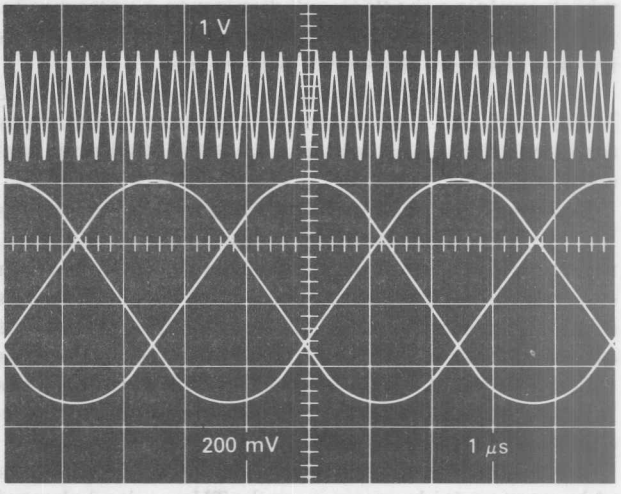


FIGURE 6 — 3.58 MHz Sine Wave Sampled at 10.7 MHz

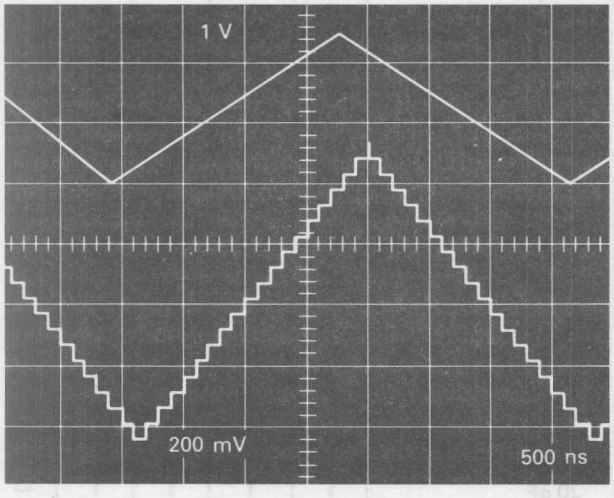


FIGURE 7 — 270 kHz Triangle Sampled at 10 MHz

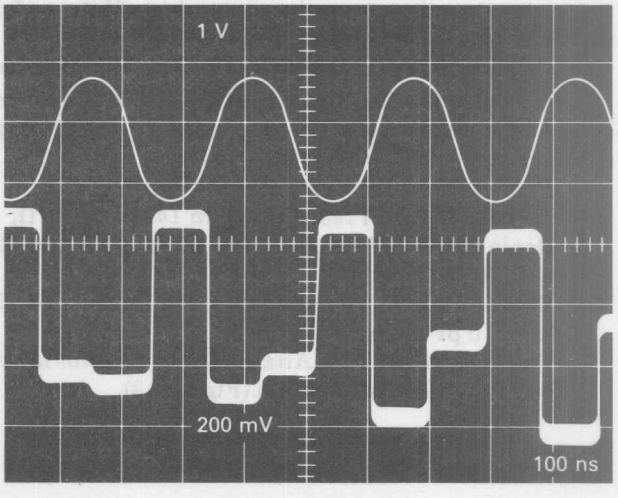


FIGURE 8 — 3.58 MHz Sine Wave Sampled at 10.7 MHz

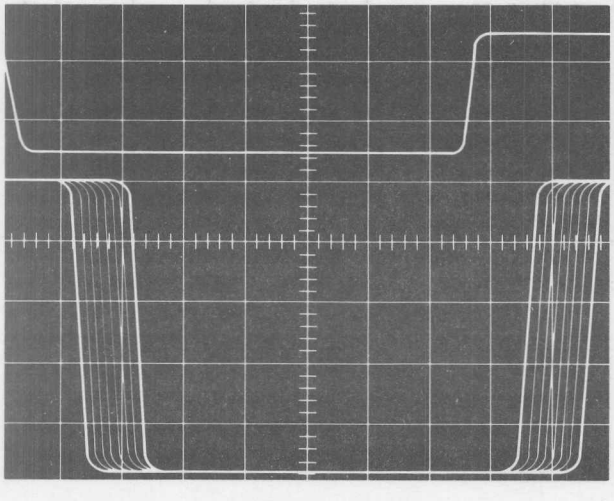


FIGURE 9 — Horizontal Scale = 100 ns/div
Sample Rate = 10 MHz

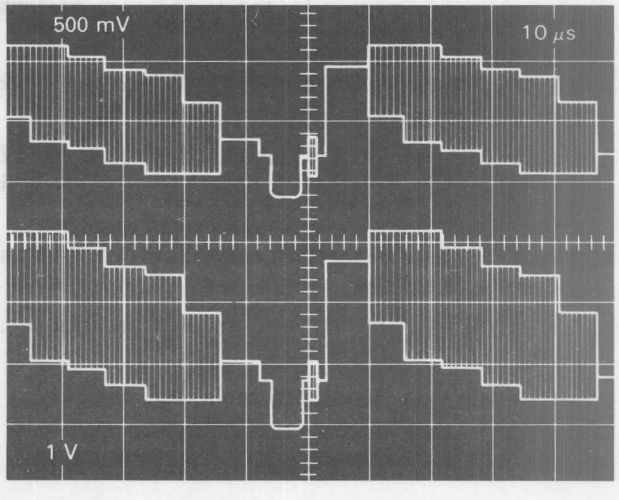


FIGURE 10 — Full Field Color Bars @ 10.7 MHz

Note: Upper Trace = Analog Input, Lower Trace = Analog Output (Each Figure)

which explains the "jittery" display on a vectorscope. Additionally, the errors decrease proportionately as the amplitude of the signal is increased.

If the composite video signal is sampled at 4X (14.3 MHz), then the sync signal will have an uncertainty (or jitter) of ±34.9 ns, which is ±0.055% of a horizontal scan period.

The Evaluation Board described in this article has been tested for differential phase and differential gain, using a standard video test signal (40 IRE subcarrier on a 100 IRE ramp, sampled at 14.3 MHz), with results of ±1% gain error and ±1° phase error. The signal was obtained from a Tektronix 147A video test generator applied to the ALT IN connector. The output (of the MC10318) was configured for 75 ohms output impedance, and applied to a Tektronix 520A Vectorscope.

Tests conducted with the Evaluation Board in a video system (video camera and a TV monitor) showed no visible degradation of picture quality (at 8-bits resolution). The board provides an easy means of testing picture quality at a reduced number of bits, or for conducting any test on a digitized video signal.

See Figure 10 for an example of a video test pattern.

Note: In order for the output of the Evaluation Board to comply with RS-170, make the following changes at the MC10318 DAC:

- Replace the 20 Ω resistor at Pin 15 with 75 Ω;
- Replace the 20 Ω resistor at Pin 14 with 37.5 Ω;
- Replace the 1600 Ω resistors at Pins 10 and 12 with 3000 Ω each;
- Replace the 80 pF capacitors at Pins 14 and 15 with 10 pF each;
- The jumper near the Analog Out connector must be in the Normal position (Figure 13).

REFERENCES

1. Felix, Michael O., *Differential Phase and Gain Measurements in Digitized Video Signals*, SMPTE J., 85: 76-79, Feb. 1976.
2. *The Near-Term Future for Digital Television*, 120th SMPTE Technical Conference, Nov. 1978.
3. *Interconnection Techniques for Motorola's MECL 10,000 Series Emitter Coupled Logic*, AN-556, Motorola, Inc., 1974.
4. *MECL System Design Handbook*, Third Edition, Motorola, Inc., 1980.
5. MC10315L/MC10317L Data Sheet, Motorola, Inc., 1981.
6. MC10318L Data Sheet, Motorola, Inc., 1982.

PARTS LIST

Device	8-Bit A-D and D-A	7-Bit A-D and D-A	8-Bit A-D	7-Bit A-D	8-Bit D-A
Semiconductors					
MC10315	1	—	1	—	—
MC10317	1	1	1	1	—
MC10318	1	1	—	—	1
MC34002	2	1	2	1	—
MC1400U5	2	2	2	2	1
MC10176	2	2	2	2	2
2N2222	2	1	2	—	—
2N2907	2	1	2	—	—
LH0024C	1	1	1	1	—
Resistors					
51K, 1/4 W	8	4	8	4	—
15K, 1/4 W	8	4	8	4	—
3.3K, 1/4 W	2	2	2	2	—
2K, 1/4 W	2	2	2	2	1
10K, 1/4 W	1	1	1	1	—
27K, 1/4 W	4	2	4	2	—
510, 1/4 W	20	17	20	17	16
20, 1/4 W	3	3	1	1	2
1600, 1/4 W	2	2	—	—	2
100, 1/4 W	1	1	1	1	—
51, 1/4 W	1	1	1	1	1
200, 1 W	4	2	4	2	—
1K, 1/4 W	1	1	1	1	1
Trimpots					
10K, 20 Turn (Rectangular)	4	2	4	2	—
Capacitors					
0.1 μF, 50 V	41	26	37	22	7
10 μF, 50 V Tant.	8	8	7	7	3
300 pF	1	1	1	1	—
80 pF	2	2	—	—	2
10 pF	1	1	1	1	—
20 pF	1	1	1	1	—
22 μF, 50 V Tant.	1	1	—	—	1
180 pF	1	1	1	1	—
9-35 pF Trimmer	3	3	—	—	3
0.01 μF, 50 V	1	1	—	—	1
2 pF	1	1	1	1	—
Misc.					
PC Board	1	1	1	1	1
Banana Jacks	8	8	7	6	5
BNC Connector	4	4	3	3	2
8-Pin Connector (SAMTEC TS120GD11)	—	—	1	1	1

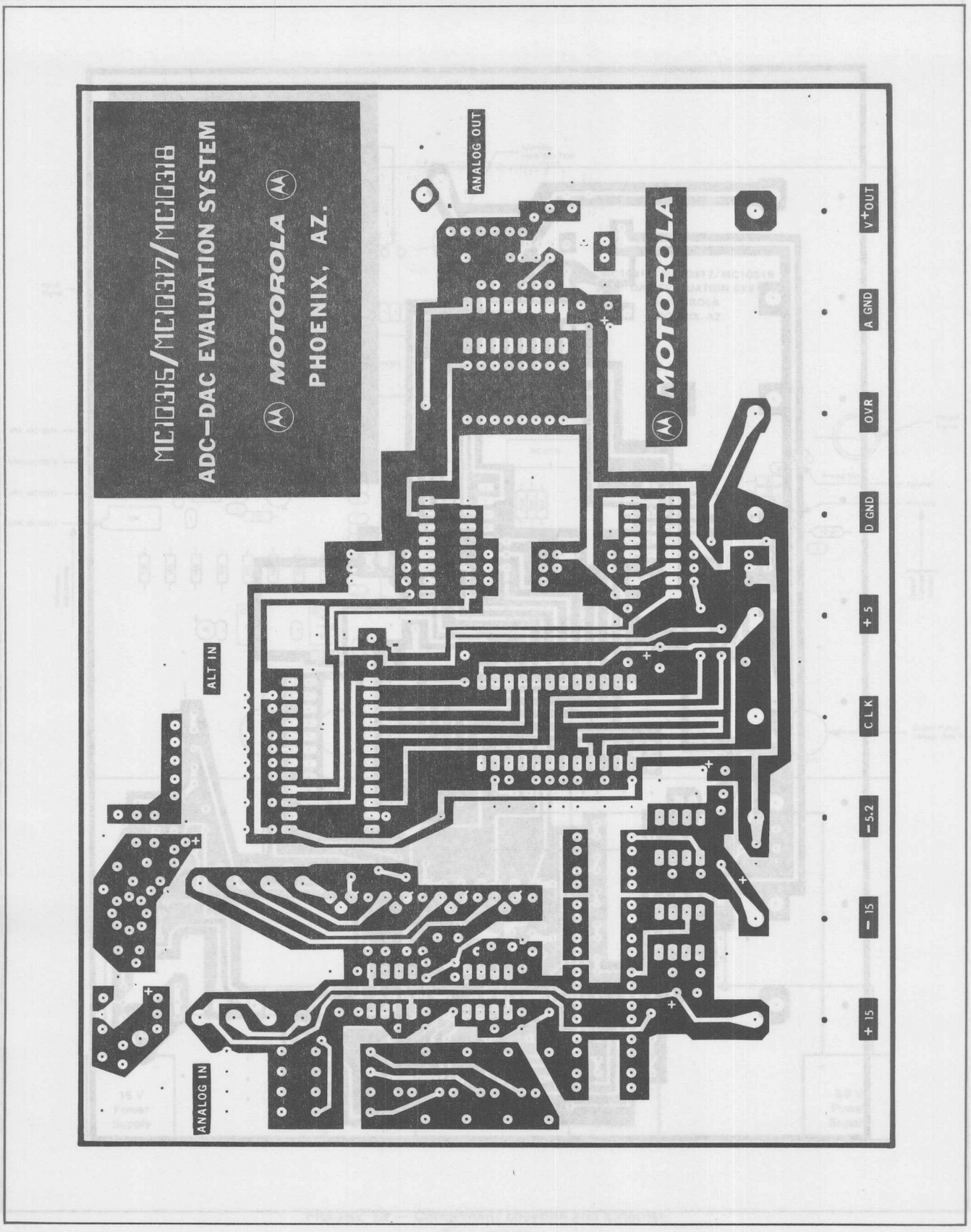
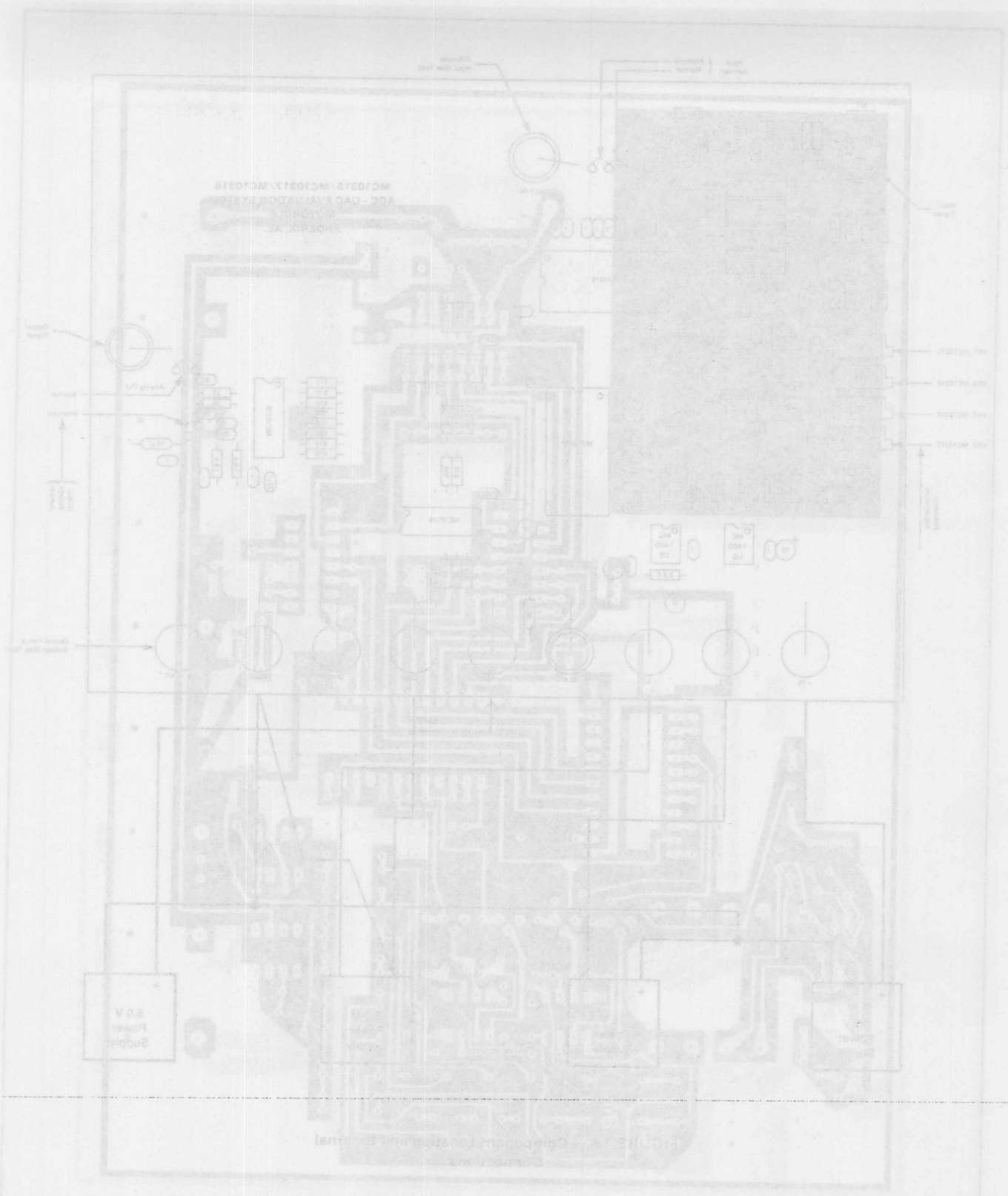


FIGURE 11 — Component Side Artwork (Top)
(Overall Size = 6.0″ × 8.00″)



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