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Application Note

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A LINE OPERATED, REGULATED 5 V/50 A SWITCHING POWER SUPPLY

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This application note describes a regulated 220 V ac to 5 Vdc converter using high voltage switching transistors and Schottky barrier rectifiers. The control functions are all performed by integrated circuits.

MOTOROLA Semiconductor Products Inc.

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INTRODUCTION

Almost all electronic circuits require a dc voltage supply with some degree of stabilization. The voltage is normally obtained by rectifying and filtering an ac voltage. The desired stability is produced by the action of certain regulating circuits.

The most widely used regulator is the series linear regulator which is essentially a controlled voltage divider. The ratio of this divider is controlled such that the output voltage remains at a constant level for all specified changes of input voltage and load current. This type of regulator has outstanding properties as far as load and line regulation, noise and regulation response time are concerned. It is particularly suitable for those applications where linear operational amplifiers have to be supplied and noise can be a problem, or where a very high degree of stability is required. On the other hand, a lot of power is dissipated in these regulators because their efficiency is rarely higher than 50 percent. Higher efficiency, however, at the expense of slower regulation response time and higher noise levels, can be achieved by series switching regulators.

In a series switching regulator, the filtered dc input voltage is chopped by a series switching element, in general, a switching transistor. The resulting rectangular pulse train is filtered by a low pass filter, yielding a smooth dc voltage at the output of the filter. The value of this voltage is determined by the duty-cycle of the chopper and can therefore be stabilized electronically by controlling the duty-cycle, with respect to a reference voltage. This type of regulator offers noise and regulation performances that are always inferior by one order of magnitude to the corresponding linear regulators. They are therefore best suited for supplying less critical loads, like digital circuits. The losses in a series switching regulator are caused mainly by the voltage drops of the saturated switching transistor, the forward voltage drop of the freewheeling diode and the power dissipation during the commutation of the switching transistor. Efficiencies up to 85 percent can be obtained with this system.

Both types of series regulator use a transistor as the controlling element which has not only to withstand the full input voltage but also to carry the full load current. Therefore, both systems usually need a line transformer in order to produce the lowest possible input voltage to the regulator. Transformers operating at 50 or 60 Hz that have to transmit several hundred volt-amperes are heavy and bulky components and frequently prove difficult to place in equipments that have to be compact. The availability of high voltage transistors capable of carrying several amperes collector current have made it possible to design inverter-type switching regulators working directly off the line voltage without an intermediate 60 Hz transformer.

These inverter switching regulators offer noise and regulation performances similar to the series switching types and can replace them in most applications where price is not the ultimate requirement. They can be built to be more compact and light-weight, at the expense of slightly more complicated electronics, than the equivalent series switching units.

Inverter regulators use either two or four switching transistors for chopping the rectified line voltage at ultrasonic frequency (usually between 20 and 50 kHz) before applying it to a compact power transformer designed for operation at this frequency. The transformer, generally a step-down, is followed by a rectifier and a smoothing filter to obtain the dc output. The basic inverter configurations of transistors are the full bridge and its derivatives, the push-pull and the half bridge. A discussion of the properties of the last two circuits is presented in AN737 (ref. 1). The choice between these circuits depends on specific conditions such as magnitude of the line voltage, available switching devices, desired output power, etc. In brief, the full bridge is mainly used for obtaining very high output powers, above 1 kW. For medium and low output powers the half bridge and push-pull are preferred; they require two high power transistors but only two drivers, as compared to four smaller transistors and four drivers for the full bridge. The disadvantage of requiring transistors of higher power is compensated by a simpler driving circuit.

For high line voltages (typically 220 V) the half bridge is preferred to the push-pull because it requires lower voltage transistors. For low line voltages (typically 115 V) the simplicity of the driving circuit of a push-pull inverter makes it generally preferable to the half bridge, although its potential ability to draw destructive dc current through one leg of the output transformer and also sometimes the necessity of having to isolate electrically the transmission of the output voltage magnitude to the control electronics may require extra efforts to find suitable solutions.

In this note a system is described which uses a half bridge Pulse Width Modulated Inverter to generate a 5V/50A output from 220 volts ac lines.* The switching transistors,

*Operation from a 115 V ac line is possible if a full-wave voltage doubler is used.

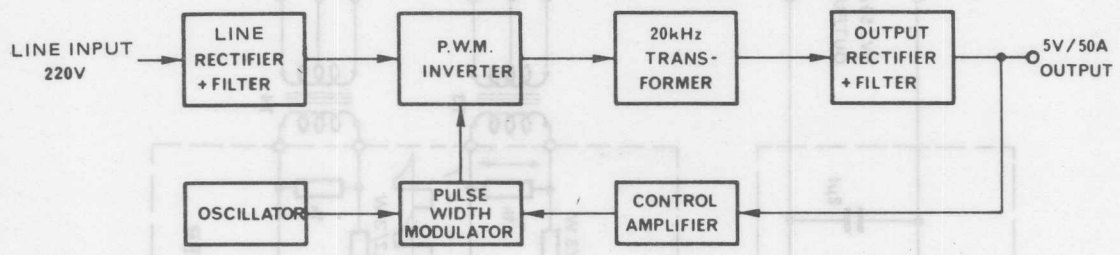


FIGURE 1 – POWER SUPPLY BLOCK DIAGRAM

operated at 20 kHz, are used to produce an ac voltage which is stepped down by a ferrite core transformer to an appropriate value. The secondary voltage of the transformer is rectified and filtered to yield the smoothed 5 Vdc output. Regulation of the output voltage is achieved by controlling the duty cycle of the switching waveforms.

DESCRIPTION OF THE SYSTEM

General

A block diagram of the complete system is shown in Fig. 1. Rectifying and filtering the line voltage yields a 310 Vdc voltage which provides the supply voltage for the dc-dc converter generating the 5 volts output.

The control circuitry consists basically of a Pulse Width Modulator, a clock oscillator and a control amplifier. The control pulses generated by the P.W.M. are at clock frequency and have a duration dictated by the control amplifier.

The input circuit

The input circuit can be seen in detail in figure 2; it consists of a rectifier and a smoothing capacitor. Nominal line voltage is 220 volts, 50–60 Hz. The minimum voltage for a full power output is 190 Vac and the maximum, for the elements selected here, is 260 Vac corresponding to 268 and 367 peak dc volts respectively. The line is rectified by an MDA 806 bridge and filtered by an electrolytic capacitor of 600 μF. This gives a ripple voltage of 15 volts peak-to-peak at full load and at nominal input voltage. The current flowing from the capacitor to the inverter under these conditions is 1.1 amps dc. The current through the rectifier bridge is 2.4 amps rms.

P.W.M. inverter

The half bridge inverter circuit shown in figure 2 consists of capacitor C_1 and C_2, transistors TR_1 and TR_2 and transformer T_1.

The capacitors C_1 and C_2 divide the dc supply voltage approximately to its mid-value (155 Vdc). These capacitors also prevent any net dc voltage being applied to the primary of T_1. Transistors TR_1 and TR_2 are alternately turned ON and OFF, producing across the primary of T_1 the stepped ac waveform indicated in the upper half of figure 3, the same waveform that appears across the switching transistors. The current in one transistor is indicated in the lower half of figure 3. At the beginning and at the end of the conduction period the collector-emitter voltage of each transistor changes ideally by half the inverter dc supply voltage (155 volts). The full dc voltage of 310 volts appears at the transistor collector only after the transistors are completely cut-off and draw no more collector current. The peak switching power which the transistors have to handle is therefore, theoretically, the product $1/2\ V_{CC} \times I_C$.

In practice the switch -off portion of the load line tends to extend up to the point $V_{CC} \cdot I_C$ due to stray inductance in the power transformer. Use of an RC snubber network in parallel with TR_2 is therefore recommended to keep the load line within the Reverse Bias Safe Operating Area of the switching devices. A practical result obtained with such a technique is illustrated in figure 4.

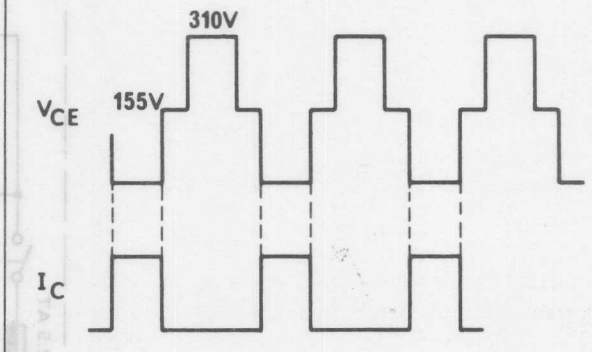


FIGURE 3 – VOLTAGE AND CURRENT WAVEFORMS FOR THE INVERTER TRANSISTORS

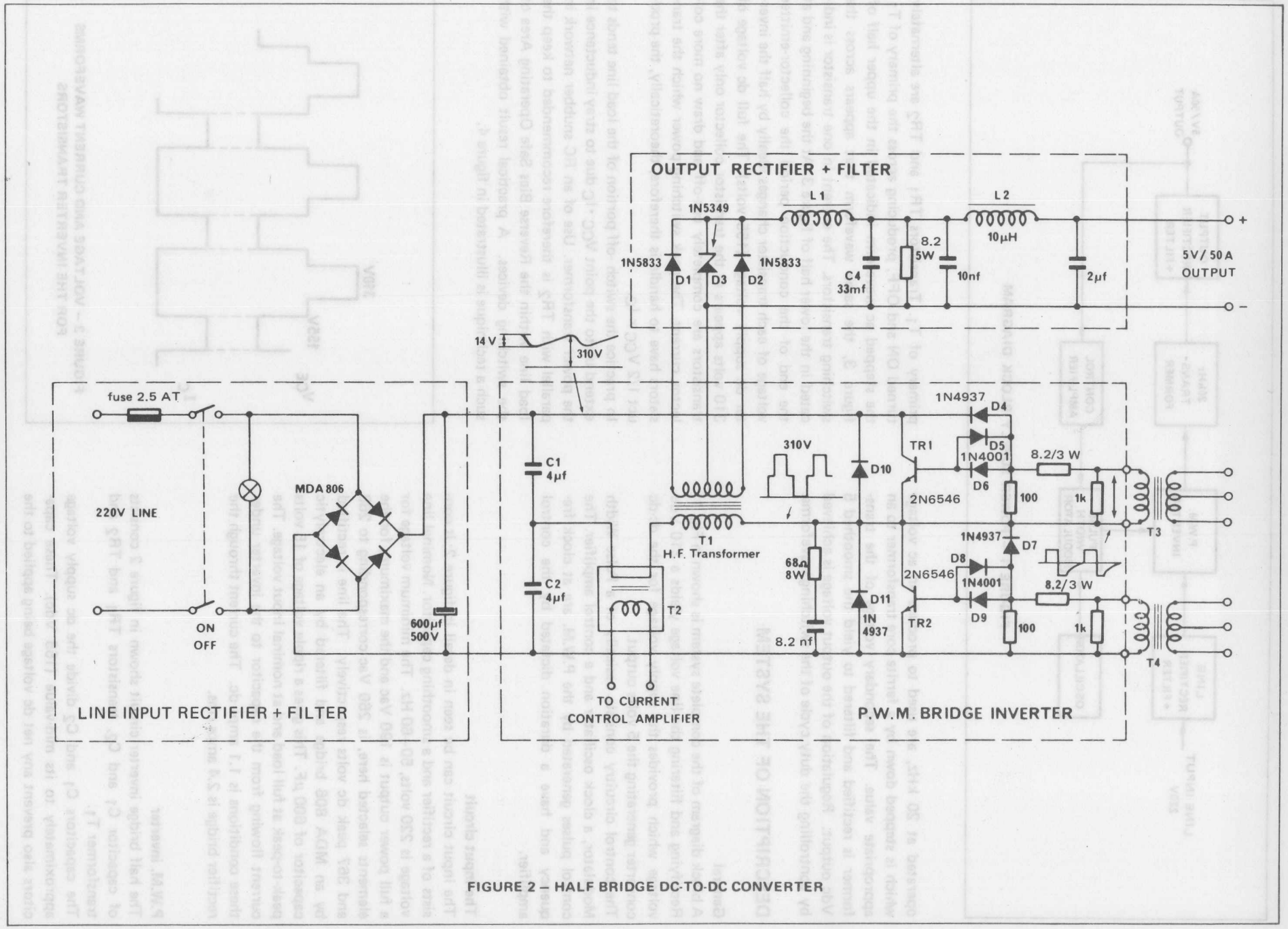
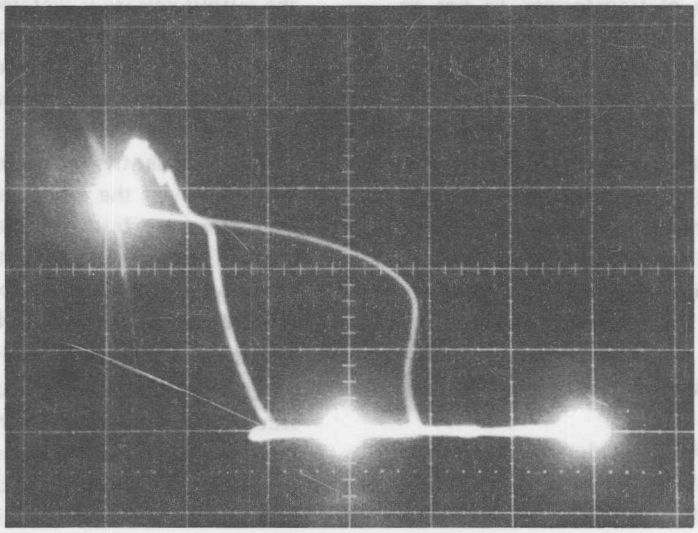


FIGURE 2 – HALF BRIDGE DC-TO-DC CONVERTER



Vertical: 1 A/Div.
Horizontal: 50 V/Div.

FIGURE 4 – LOAD LINE OF THE INVERTER TRANSISTORS AT FULL LOAD

The transistors used in the present design, 2N6546, are fast high voltage devices capable of switching currents of 8 A at 350 volts level. In order to keep the devices switching at high speed throughout the complete range from full output load to no-load, great care has to be taken in the design of the base driving circuits. Here, as illustrated in figure 2, use is made of a diode network for avoiding saturation of the transistors. The diodes D_4 up to D_9 very effectively maintain full switching speed for the transistors with any load. A fast recovery type of diode has to be selected for D_4 and D_7.

The transistor dissipation is about 20 watt for both devices together at full load. The required heatsink should have a thermal resistance of about 2,5°C/watt in order to keep the junction temperature below 120°C for a 50°C ambient temperature.

Special care is needed in the design of the ultrasonic frequency power transformer. The winding technique has to be such as to minimize the leakage inductance in order to avoid large voltage overshoots affecting transistor commutation. An interleaved structure was adopted for the transformer windings as shown in figure 5. The primary winding consists of three windings in parallel, the two halves of the secondary winding are sandwiched between the primary ones.

In addition to proper winding techniques, high frequency wiring rules must be observed in order to minimize RF interference and parasitic oscillation.

The following is the specification for transformer T_1:

Core Philips P 66/56 – 3H1
Np = 33 turns of 0.6 mm dia wire
Ns = 2 turns of 1 x 6 mm flat wire

The current transformer T_2 is used as the detector for the current control loop to limit the output at 50 A. When loaded with 10 kΩ, it provides a signal of about 0.4 V/A.

Construction data for T_2 are as follows:

T_2: Core Telmag HWR 4/5/4, single loop
Np = 1
Ns = 1000 turns of 0.2 mm dia wire

C_1 and C_2 are metallized polyester capacitors with a 20 kHz impedance of approximately 2Ωeach. The ultrasonic frequency ripple across them at full load is about 5 volts pk-pk.

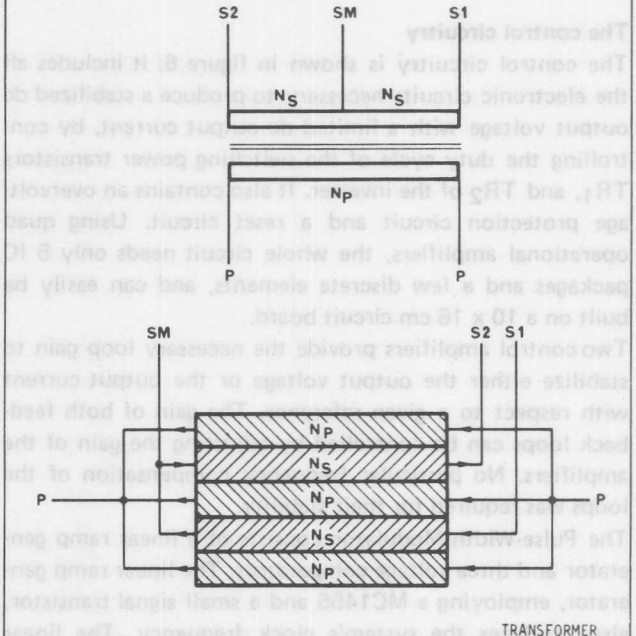


FIGURE 5 – WINDING TECHNIQUES USED FOR THE TRANSFORMER T 1

Output rectifier and filter

The voltage at the secondary of transformer T_1 has an amplitude of approximately 9 volts at nominal input voltage. This voltage is rectified by two 40A/30V Schottky rectifiers which provide a very efficient high current rectification. The thermal power dissipation of these devices at full load is approximately 20 watts each and a heat sink of at least 1.3°C/W is required to keep their junction temperature below 125°C at an ambient temperature of 50°C. Schottky diodes are very sensitive to over-voltages even in the form of short spikes; a simple zener diode D_3 protects them against spikes above $2 \times V_z$ and greatly increases the reliability of the system.

The output filter consists of two LC sections with following data:

L_1 Core Telmag HWR 40/24/4, double loop with a 1.5 mm airgap, 23 windings of copper sheet 55 x 0.4 mm

L_2 1 cm^2 iron core with 4 windings of copper flat wire 6 x 1 mm.

The first filter section has a series resonance frequency of about 400 Hz for greater attenuation of the ripple at the working frequency and above. The 100 Hz ripple is reduced by the regulating circuit itself, by as much as 70 dB. The second filter section attenuates the residual commutating spikes which can pass the first filter section by virtue of the winding capacitance of L_1.

A fixed preload of 8.2Ω maintains a minimum of conduction time in the switching transistors and avoids large shifts in the dc level at the junction of C_1 and C_2. Such shifts would increase the switching power in the switching devices when large loads are suddenly applied.

The control circuitry

The control circuitry is shown in figure 6; it includes all the electronic circuits necessary to produce a stabilized dc output voltage with a limited dc output current, by controlling the duty cycle of the switching power transistors TR_1, and TR_2 of the inverter. It also contains an overvoltage protection circuit and a reset circuit. Using quad operational amplifiers, the whole circuit needs only 5 IC packages and a few discrete elements, and can easily be built on a 10 x 16 cm circuit board.

Two control amplifiers provide the necessary loop gain to stabilize either the output voltage or the output current with respect to a given reference. The gain of both feedback loops can be controlled by adjusting the gain of the amplifiers. No particular frequency compensation of the loops was required for their stability.

The Pulse-Width-Modulator consists of a linear ramp generator and three voltage comparators. The linear ramp generator, employing a MC1455 and a small signal transistor, also produces the system's clock frequency. The linear ramp is separately compared to the outputs of the two control amplifiers and also to a pre-set fixed limiting voltage, by three MC3302. The outputs of these three comparators are connected together in a wired "OR" so that preference is given to the one defining the shorter pulses (i.e. the one defining the lower output voltage). Control of the output voltage is dictated by the voltage loop, up to an output current of approximately 50 A. Above 50 A the current control loop defines the pulse width and causes the output voltage to decrease. The fixed voltage provided by the Limiter defines the maximum length of the pulses and consequently guarantees that in all circumstances (particularly if the input voltage is too low) the switching transistors are both disabled for a few μs at each half cycle. This time, set by potentiometer P_1, is required for the conducting transistor to recover completely before the other transistor is driven ON.

The inverter has to be started with a low duty cycle in order to prevent a large starting pulse (in terms of volt-seconds) from driving the transformer core into saturation and possibly causing high inrush current into the switching transistors. A low duty-cycle start-up network has therefore been foreseen in combination with the Limiter. When the Reset push-button is pressed, capacitor C_5, initially discharged, causes the Limiter comparator to assume control of the duty cycle and to keep it to a very low value. C_5 is then slowly charged-up through R_5 and the duty cycle is progressively increased until control is taken up by the voltage or the current loop.

The phase splitter provides the correct routing of the pulses from the P.W.M. to the power transistors'drivers. It uses one D-flip-flop MC14013 and two gates MC14023. The pulse train can be stopped by the reset circuit; the drivers and the output power transistors are then automatically disabled.

The power transistors' drivers are self-commutating push-pull drivers providing electrically isolated signals to the power transistors by means of the transformers T_3 and T_4. Data for these transformers are as follows:

Core 3H1 18/11

Np = 2 x 60 turns of 0.25 mm dia wire

Ns = 15 turns of 0.5 mm dia wire

While a positive driving pulse is being transmitted to the bases of the power transistors, energy is stored in the core of these transformers. At the end of each pulse this energy is liberated at the secondary of T_3 and T_4 in the form of a negative 5V pulse applied across the emitter-base junction of the power transistors, resulting in fast recovery of the transistor. During development, it was found useful to include a small fuse in series with the transistors' bases to protect the driving circuits in case of accidental transistor failure.

The overvoltage detector compares the output voltage to a reference by means of a programmable unijunction transistor (PUT). If the output voltage exceeds that reference (typically 6 volts) the PUT is triggered and generates a pulse, which, amplified by an MC3302, clocks the reset circuit. An optional thyristor crowbar could easily be added to short the output of the supply so as to avoid damaging the load.

The purpose of the reset circuit, a D-flip-flop MC14013, is to stop the system's clock and disable the output drivers. It is set upon command of the overvoltage detector as well as each time the power supply is switched on, so that it

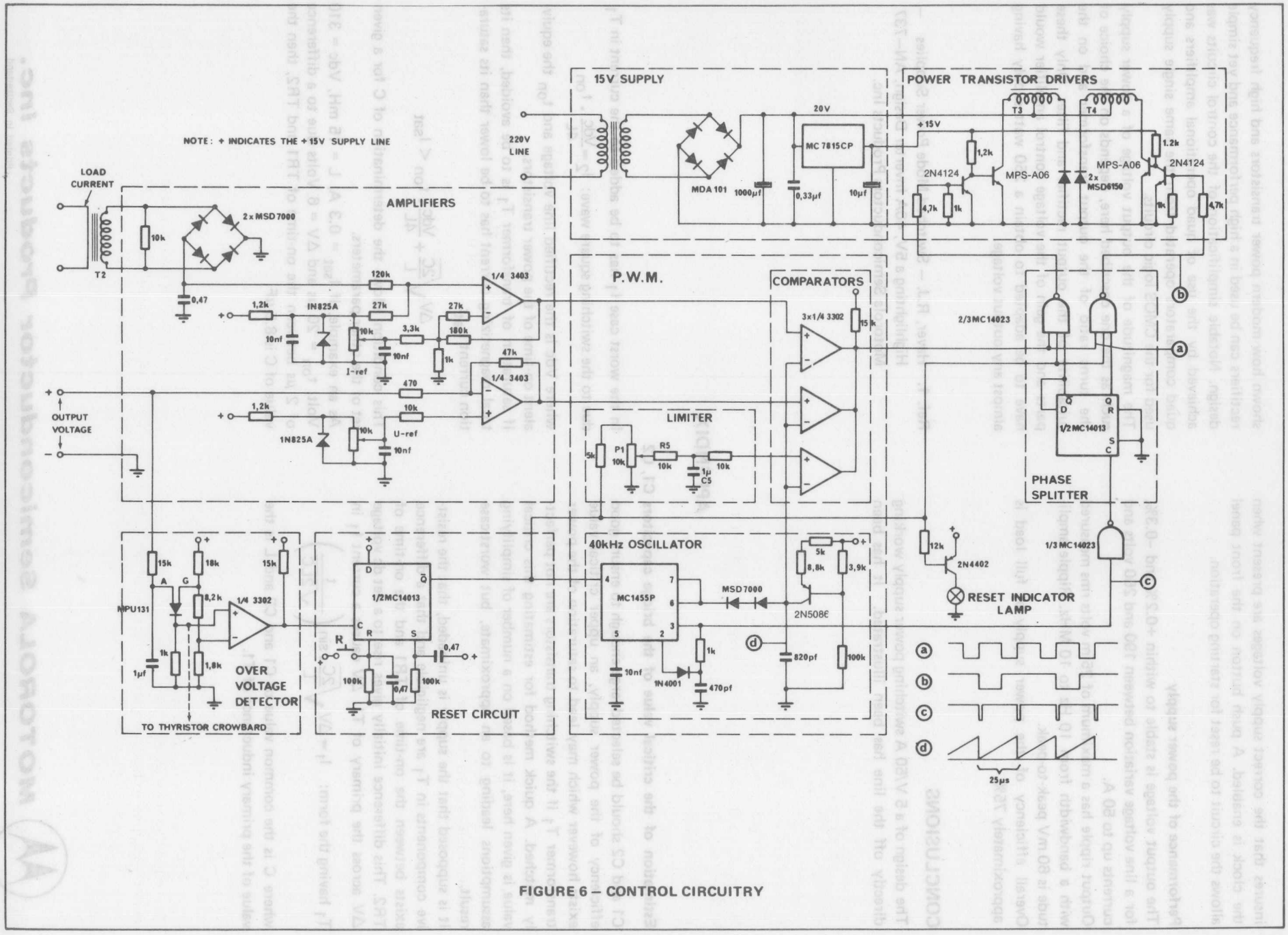


FIGURE 6 – CONTROL CIRCUITRY

insures that the correct supply voltages are present when the clock is enabled. A push button on the front panel allows the circuit to be reset for starting operation.

Performance of the power supply

The output voltage is stable to within +0.2% and −0.3%, for a line voltage variation between 190 and 260 volts and currents up to 50 A.

Output ripple has a maximum of 25 m volts rms measured with a bandwidth from 10 Hz to 10 MHz. Ripple amplitude is 60 mV peak-to-peak.

Overall efficiency of the power supply at full load is approximately 75%.

CONCLUSIONS

The design of a 5 V/50 A switching power supply working directly off the line has been illustrated. It has been shown how modern power transistors and high frequency rectifiers can be used in a high performance and yet simple design. Notable simplification of the control circuits was achieved by the use of quad operational amplifiers and quad comparators operated from the same single supply used for the CMOS logic circuits.

The magnitude of the output voltage of a power supply such as the one described here, depends on the choice of the turns ratio of the output transformer and on the suitability of the output rectifier and filter. Only these parts and the gain of the voltage control amplifier would have to be adapted to obtain a 250 watt supply having almost any output voltage.

Ref. 1. Haver, R.J. – Switched Mode Power Supplies – Highlighting a 5V, 40A Inverter Design, AN–737 Motorola Semiconductors Products Inc.

APPENDIX

Estimation of the critical value of the bridge capacitors C1, C2

C1 and C2 should be selected large enough to ensure good efficiency of the power supply, an upper critical value exists however which may lead to saturation of the power transformer T_1 if the switching transistors are not perfectly matched. A quick method for estimating this critical value is given here, it is based on a number of simplifying assumptions leading to an approximate, but worst-case result.

It is supposed that the supply is unloaded, that the resistive components in T_1 are negligible and that a difference exists between the on-time of TR1 and the on-time of TR2. This difference initially gives rise to a net dc voltage ΔV across the primary of T1. ΔV causes a current I_1 in T_1 having the form: $I_1 = \Delta V \sqrt{\frac{2C}{L}} \cdot \sin\left(\frac{t}{\sqrt{2LC}}\right)$

where C is the common value of C1 and C2 and L is the value of the primary inductance of T1.

In the worst case I_1 has to be added to the current in T_1 due to the switching square wave: $I_2 = \frac{Vdc}{4L} \cdot t_{on}$

where Vdc is the rectified line voltage and t_{on} the equivalent on-time of the power transistors.

If saturation of transformer T_1 is to be avoided, then its total magnetizing current has to be lower than its saturation current I_{sat}:

$$\Delta V \sqrt{\frac{2C}{L}} + \frac{Vdc}{4L} \cdot t_{on} < I_{sat}$$

This condition allows the determination of C for a given set of the other parameters.

As an example, if I_{sat} = 0.3 A, L = 15 mH, Vdc = 310 Volt, t_{on} = 20 μs and ΔV = 6 Volts due to a difference of 2 μs between the on-time of TR1 and TR2, then the value of C is 8.5 μF.

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