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Application Note

A CMOS KEYBOARD DATA ENTRY SYSTEM FOR BUS ORIENTED MEMORY SYSTEMS

Prepared by:
Mike Hadley
Digital Systems Applications

This application note describes a keypad to binary data entry system for use with NMOS or CMOS memories, either in a minicomputer/microprocessor application or as a part of any logic system containing random access memory. Manual data entry using a keypad avoids the use of a binary format, offering increased speed and accuracy of manual direct memory accessing.

MOTOROLA Semiconductor Products Inc.

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INTRODUCTION

Manual loading of data into RAM memory systems is at best a tedious process. The method most commonly used is an array of toggle switches that when on, effect a binary "1" and when off a "0". This method requires operation in binary, an inconvenience as well as a time consuming task. This note describes a data entry system using a 4 x 4 keypad switch array coded in hexadecimal. This in effect allows memory loading in calculator style, with each keystroke coding four binary bits. Any CMOS compatible memory system with external control of an address bus up to sixteen bits and a data bus up to eight bits can make use of this keyboard entry system without modifications.

A typical application is in an M6800 Microprocessor system. When the MPU is in HALT, both the address bus drivers and the data bus drivers are in a 3-state mode. This allows control of both buses with an external device such as the data entry system to be described.

DESIGN AND OPERATION

Several relatively new CMOS devices are presented in this design as shown in Figure 1. The MC14419 is a 4 x 4 keypad to binary encoder with an internal strobe generator. When a key is depressed on the keypad, a row and a column input associated with the key are forced to ground, and the binary representation of the depressed key appears on the four output lines. In this way one keystroke encodes four binary lines. Should two or more keys be depressed simultaneously, the MC14419 outputs will remain zeros, with no internal strobe generated (a strobe will be generated with external logic, however). Since both data entry and addressing must be done using the same keyboard, additional circuitry is required to route these binary coded hexadecimal numbers onto either the address bus or the data bus.

Control of data routing is via four SPST toggle switches, all of which use the MC14490 hex bounce eliminator to insure bounce free logic transitions. This leaves two additional bounce eliminators in the MC14490 package, for use in conjunction with a 2-input AND gate, an inverter, and a 4-input NAND gate to generate a strobe pulse when any one of the sixteen keys on the 4 x 4 keypad is depressed. The output from this configuration is a pulse equal to four periods of the internal clock of the MC14490, and occurs eight clock periods after the depressed switch ceases to bounce. Only one pulse is generated when a key is depressed; bouncing or noise cannot generate additional pulses. An extra inverter-AND gate combination is added to each of the two debouncers used for the Deposit-Address switch and the Deposit-Data switch. The output of the AND gate will produce a "1" whenever the associated switch is toggled from its normally high position to a low (ground) state. The output will bounce with the switch, and then remain high until the debouncer goes low (four clock periods after bouncing ceases). This signal serves to reset the counters immediately before data entry or addressing is to take place, insuring that the first number entered will be the most significant digit (MSD).

As designed, the keyboard will control an eight bit data bus and a sixteen bit address bus. This implies that in addition to controlling data routing to either the address or data bus, control must also determine which of the two 4-bit data positions are to accept data, or which of the four 4-bit address positions are to accept data. This is done with an MC14518 dual 4-bit counter and an MC14555 dual, binary to one-of-four data router. When the counters are enabled with a Deposit Data or a Deposit Address switch, a strobe pulse generated when a key is depressed propagates through the selected decoder to the enable of the most significant counter (for addressing) or latch (for data entry). The trailing edge of the strobe pulse will toggle the selected counter so that the next strobe pulse generated (corresponding to the next number to be entered) will be routed, not to the most significant counter or latch, but to least significant latch (if data) or the third counter (if address). In this manner, if the Deposit Address switch is set, the first number entered will be deposited in the most significant (fourth) counter, the second number entered will be deposited in the third counter, the third number into the second counter, and the fourth number into the first, or least significant counter. The data input system works similarly with the two latches (the single MC14508) whose outputs connect to the data bus.

Since most memory systems are sequential, in that the next data to be used is located at either the next higher or next lower address location, the data routing circuitry was made to automatically increment or decrement the address after entering the least significant (last) 4-bit number. Two toggle switches control this function, the Increment/Decrement switch and the Automatic-Step switch. The Increment/Decrement switch controls the direction of the step. The Auto-Step function enables or disables the automatic step feature. To examine data as it is entered, Auto-Step is disabled, allowing entered data to appear immediately after the least significant data 4-bit

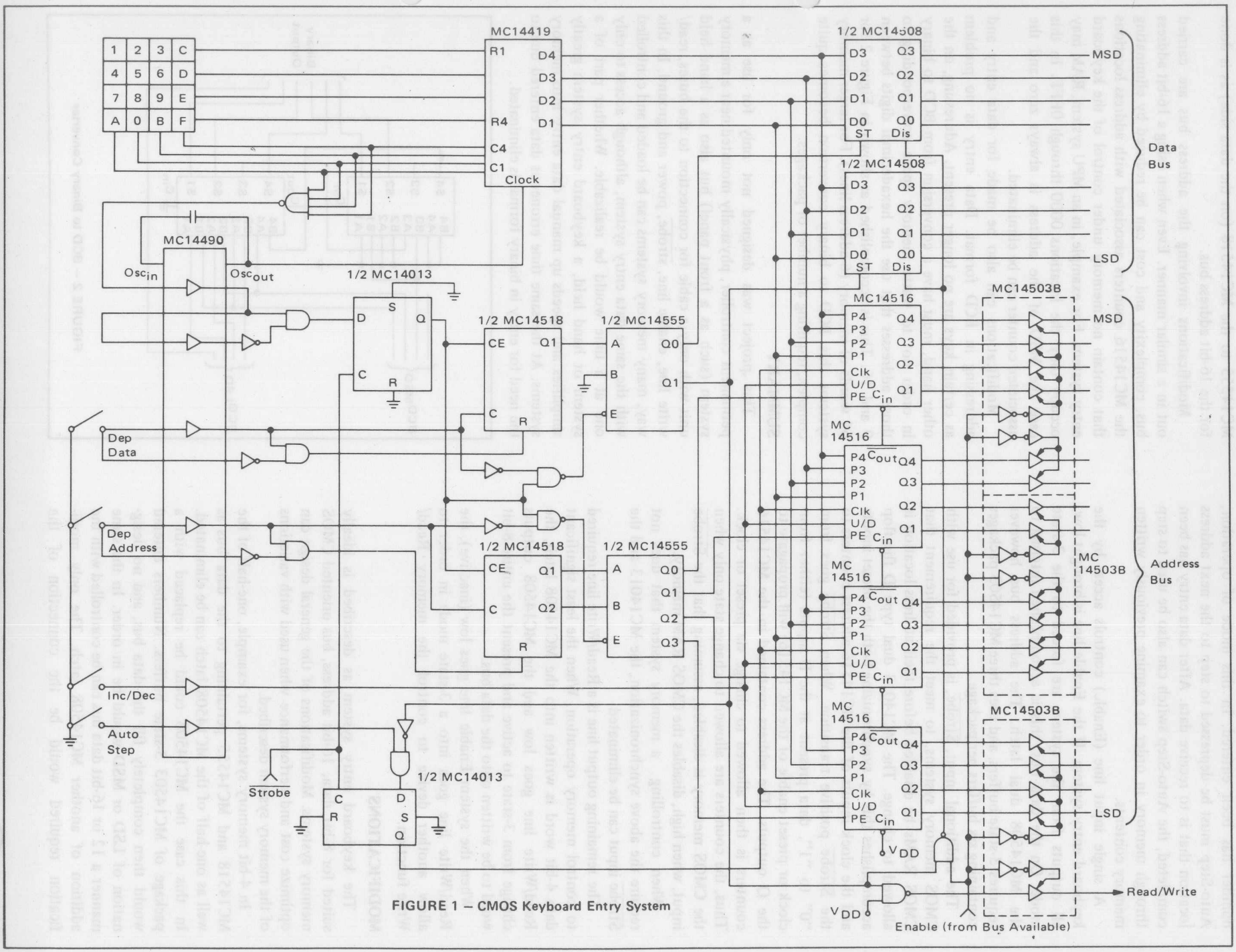

FIGURE 1 – CMOS Keyboard Entry System

number has been entered. In this mode of operation, Auto-Step must be depressed to step to the next address location that is to receive data. After data entry has been completed, the Auto-Step switch can also be used to step through memory in order to examine previously written memory contents.

A single input line (Enable) controls access by the keyboard entry system. If the Enable line is brought low, all outputs from the system are forced to the 3-state mode. On the data bus, this is accomplished internal to the MC14508 dual latch. The address bus however requires 3-state buffers, and uses three MC14503 packages containing six buffers per package.

The additional input, $\overline{\text{Strobe}}$, is provided for use with CMOS memory systems, to meet the requirement that CMOS RAMs be disabled before their address location is allowed to change. The MC14013 dual type D flip-flop accomplishes this by synchronizing both the preset inputs and the clock inputs of the MC14516 address counters to the $\overline{\text{Strobe}}$ positive transition. When $\overline{\text{Strobe}}$ goes from "0" to "1", data present at the D inputs (either from clock or preset enable of the MC14516) will propagate to the Q outputs. The address contained in the MC14516 counters is then allowed to change via preset or clock. Thus, the counters are allowed to change state only when the CMOS memory is disabled, assuming that the $\overline{\text{Strobe}}$ input, when high, disables the CMOS RAM memory.

When controlling a memory system that does not require the above synchronization, the MC14013 and the $\overline{\text{Strobe}}$ input can be eliminated.

The remaining output line is a Read/Write line required to control memory operation. When the least significant data 4-bit word is written into the MC14508 latch, the Read/Write line goes low and the MC14508 outputs change from 3-state to active and present the entire 8-bit word to be written onto the data bus.

When the system Enable line goes low (inactive), the Read/Write line goes into a 3-state mode in order to allow another device to control the memory Read/Write function.

MODIFICATIONS

The keyboard entry system as described is ideally suited for 8-bit data, 16-bit address, bus oriented CMOS memory systems. Modifications of the general design can optimize cost and performance when used with variations of the memory system described.

In 4-bit memory systems, for example, one-half of the MC14518 and MC14555 pertaining to the data bus as well as one-half of the MC14508 latch can be eliminated. In this case the MC14508 could be replaced with a package of MC14503 3-state buffers. Numbers entered would then completely fill the data bus, and no designation of LSD or MSD would be in order. In the same manner a 12 or 16-bit data bus can be controlled with the addition of another MC14508 latch. The only modification required would be the connection of the MC14555 to the MC14518 (on the data side) as is done for the 16-bit address bus.

Modifications involving the address bus are carried out in a similar manner. Even when using a 16-bit address bus, complexity and cost can be reduced by eliminating the MC14516 counters associated with address locations that contain no memory under control of the keyboard entry system. For example, in an MPU system, RAM may occupy only the locations 0000 through 0FFF. In this case the MSD of the address is always zero and the associated counter can be eliminated.

Modifications can also be made for data entry and addressing in BCD format. Data entry is no problem as certain keys are no longer present. Addressing, on the other hand, must have a conversion from BCD to binary in order not to waste memory space corresponding to those addresses that use the hexadecimal digits between 9 and 16. This is accomplished as shown in Figure 2 for 64 words of memory (6 address lines). For larger memory systems this BCD to binary conversion becomes quite complex, requiring a number of packages.

SUMMARY

This project was designed not only for use as a permanent controller, physically mounted near a memory system (such as a front panel) but also as a hand held unit with only a cable for connection to the buses, read/write line, enable line, $\overline{\text{strobe}}$, power and ground. In this way, many memory systems can be loaded and controlled with the same data entry system, although access to only one at a time would be realizable. Whether part of a system or hand held, a keyboard entry system greatly simplifies and speeds up manual data entry into memory systems. At the same time erroneous data entered due to the need for entry in binary format is eliminated.

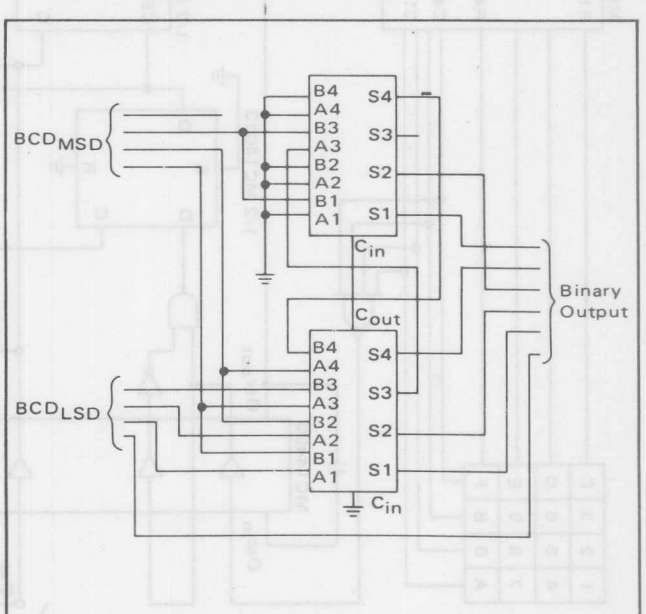

FIGURE 2 – BCD to Binary Converter

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