AN-741
Application Note

INTERFACE CONSIDERATIONS FOR NUMERIC DISPLAY SYSTEMS

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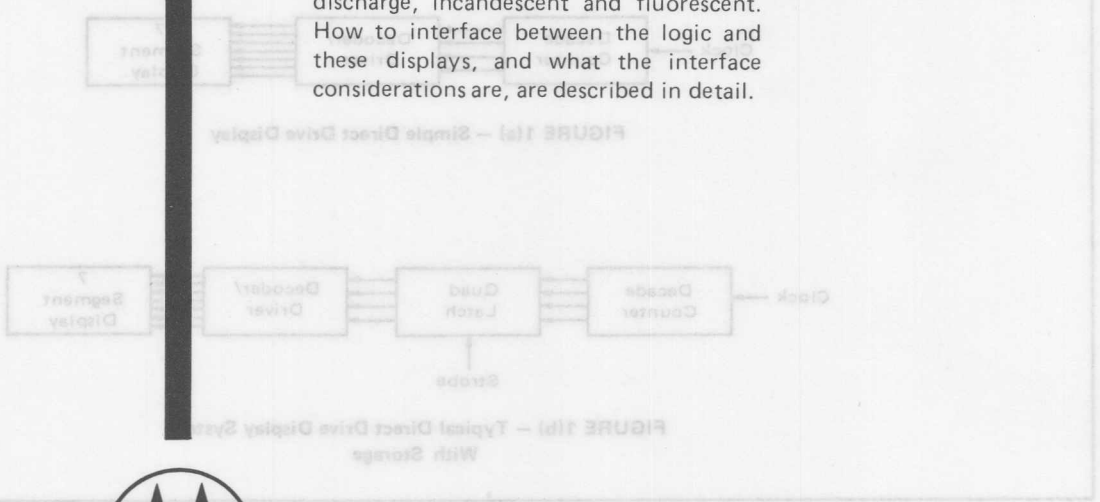
This application note describes several methods of multiplexing multi-digit, seven-segment displays. The logic devices illustrated are primarily CMOS with two examples describing TTL. The displays discussed are liquid crystal, LED, gas discharge, incandescent and fluorescent. How to interface between the logic and these displays, and what the interface considerations are, are described in detail.



MOTOROLA Semiconductor Products Inc.

INTERFACE CONSIDERATIONS FOR NUMERIC DISPLAY SYSTEMS

INTRODUCTION

The advent of MSI digital logic has made feasible the digital display at a reasonable cost with virtually all instrumentation now taking that course. Of the various display technologies, the most popular and commonly used and those with the greatest potential for future growth are liquid crystal displays (LCD), light-emitting diodes (LED), gas discharge, fluorescent and incandescent displays. The choice of which display to be used can often be dictated by the display system constraints – how large of a display is required, how many digits, viewability in lighted environments, viewing angle, what power and supply limitations, what logic families are being used and their ease in interfacing with the display, ability to be multiplexed if so required, whether to multiplex or direct drive, number of interconnections and ultimately, cost trade-offs in the total display system.

Cost considerations are generally the most important factor. Once a display type is determined, the next decision is whether to multiplex (strobe) or direct drive the display in order to reduce costs and/or simplify the design.

The type of logic families to be used and the ability to economically interface with the display must also be decided. Questions such as whether the logic can drive the display directly, and if not, what are the interface considerations, must also be answered.

It is the intent of this application note to give the reader a background on the above mentioned displays and to discuss means of interfacing between the logic devices and the displays. The logic families illustrated are the most current and attractive ones, primarily CMOS, and two examples using TTL are shown. All of the displays described are numeric seven-segment types with examples of 3-1/2 to 16 digit display systems illustrated. Generally, it is more economical to multiplex displays of greater than four digits, therefore, greater emphasis is placed on this approach, with several examples of time-sharing described.

DISPLAY SYSTEMS

The simplest type of display system, shown in Figure 1a, consists of the four lines of BCD information feeding the decoder/driver whose outputs drive the display. This direct drive system does not have information storage capability and thus, the display will read out in real time. Another display system, particularly one that has less than four digits, is shown in Figure 1b. This system contains a decade counter, quad latch, decoder/driver and display, one channel for every digit. This system has storage capability (latches) which allows the counter to recount during the storage time. The decoders discussed throughout this application note are the BCD-to-Seven-Segment Decoders used for driving the popular seven-segment displays (the one-often decoder used for driving the old Nixie ® tube will not be covered).

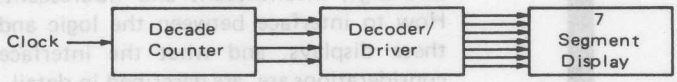


FIGURE 1(a) – Simple Direct Drive Display

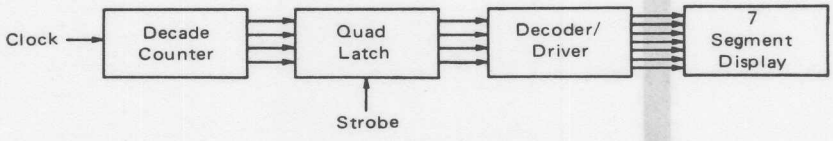


FIGURE 1(b) – Typical Direct Drive Display System With Storage

The most commonly used system for multi-digit displays is the multiplexed (or time-shared or strobed) system as shown in Figure 2. By time-sharing the one decoder/driver, parts count, interconnections and power can be saved. The N stage data register (one stage for each digit) feeds a scanned multiplexer whose sequenced BCD output drives the single seven-segment decoder/driver. Each respective output drives like segments of the display. The digit select elements are sequentially driven by the scan circuit which also synchronously drives the multiplexer. Thus, each display is scanned or strobed in synchronism with the BCD data presented to the decoder at a sufficiently high rate, usually greater than 50 scans/second, to appear as a continuously energized multi-digit display.

LIQUID CRYSTAL DISPLAYS (LCD)

With the advent of the field-effect type Liquid Crystal Display and glass frit hermetic seals, liquid crystal technology, known for many years but dormant in the laboratory, is now a production volume process. Field-effect mode displays have become readily available from various suppliers and are rapidly obsoleting the older dynamic scattering mode displays.

Liquid crystals are fluids that flow like a liquid but which have some of the optical characteristics of solid crystals. They consist of certain organic compounds, generally nematic, whose characteristics change state when placed in an electric field. Thus, images can be created according to predetermined patterns. As no light is emitted or generated, very little power is required to operate liquid crystal displays; thus they are within the drive capability of MOS ICs and are well suited for battery operation. They exhibit excellent readability in direct sunlight but in low ambient light conditions some form of light source either within or external to the display should be used.

There are two basic types of LCDs, dynamic scattering and field-effect. In the dynamic scattering display, the electric field rearranges the normally aligned molecules to scatter the available light. This causes the display to change from a transparent state to an opaque state. A more recent form of liquid crystal, the field-effect, utilizes the twisted nematic mode which effectively has its molecular plane of polarization rotated.

The field-effect LCD consists of two pieces of plate glass separated by a glass spacer/seal with the liquid crystal

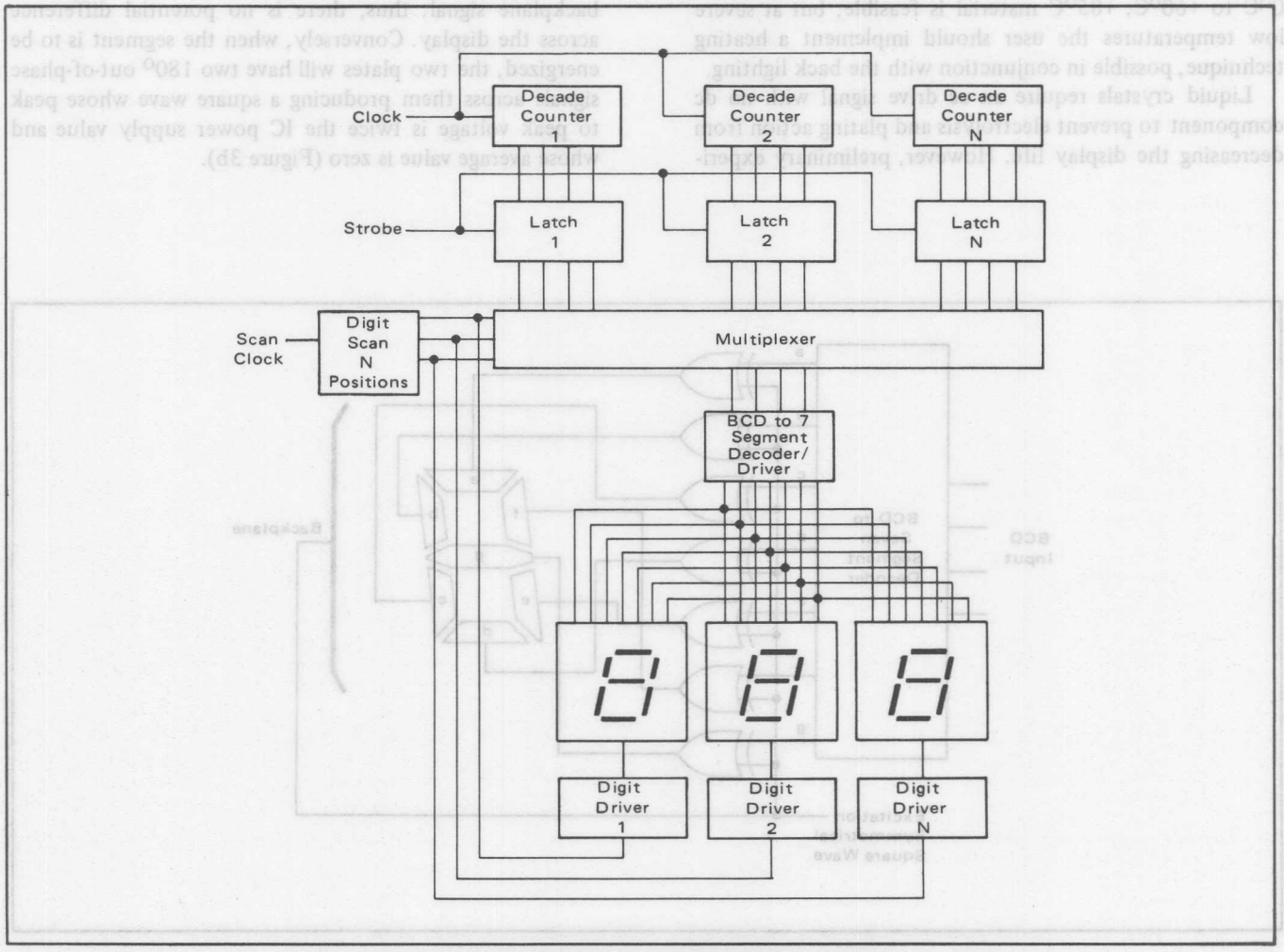


FIGURE 2 – Block Diagram of Multiplexed Display System

material injected in the void between the two plates. A metallization pattern (usually transparent indium oxide) is etched onto the glass and the liquid crystal material under the selected segment is activated when a field is placed on that particular segment. Polarizers are attached to the front and back of the display. Depending on the relative direction of the polarizers, the light striking the lower polarizer will be either reflected or absorbed.

Two types of operation are possible, reflective and transmissive. If a reflective display is desired, reflective material is adhered to the back polarizer. Reflective displays are generally used in applications where ambient light is available. The light enters the front of the display, goes through the front polarizer and the glass, then through the crystal material and back polarizer, reflects off the reflector and back out through the front of the display. It thus uses external light energy and requires virtually no power. In environments where only a small amount of light is available, a back lighted transmissive display is desirable. This display is assembled simply without the reflector material. Backlighting is generally accomplished with a diffused incandescent or fluorescent light source.

Although the state of the art is rapidly advancing, the temperature range of currently available liquid crystal displays is still limited to an operating range typically of $0^{o}C$ to $+60^{o}C$; $+85^{o}C$ material is feasible, but at severe low temperatures the user should implement a heating technique, possible in conjunction with the back lighting.

Liquid crystals require an ac drive signal with no dc component to prevent electrolysis and plating action from decreasing the display life. However, preliminary experimentation has shown that the Motorola passivated field-effect display can tolerate some dc bias on the ac excitation signal without seriously degrading the life of the device. For field-effect displays, this excitation signal may go as low as 2 V peak typically at frequencies of 60 Hz to 10 kHz. The excitation signal for dynamic scattering displays is in the 7 to 30 V peak range at 20 to 400 Hz.

DIRECT DRIVE LCD

Due to the relatively slow turn-on and turn-off times of liquid crystal displays, and the need for ac drive signals, simple multiplexing techniques have not been effective. While schemes have been designed to overcome these limitations, it usually is simpler to direct drive LCDs, with each digit having its own counter, latch, decoder, driver. The preferred method of generating the display ac drive signal is by means of an Exclusive OR gate where one input is the decoder segment signal and the other, the symmetrical square wave (no dc component) excitation signal (Figure 3a).

The excitation signal also feeds the LCD backplane. The output of the Exclusive-OR will therefore be a square wave whose phase is related to the decoder output logic level. When the segment is to be de-energized, the segment drive signal is of the same phase and magnitude as the backplane signal; thus, there is no potential difference across the display. Conversely, when the segment is to be energized, the two plates will have two 180^{o} out-of-phase signals across them producing a square wave whose peak to peak voltage is twice the IC power supply value and whose average value is zero (Figure 3b).

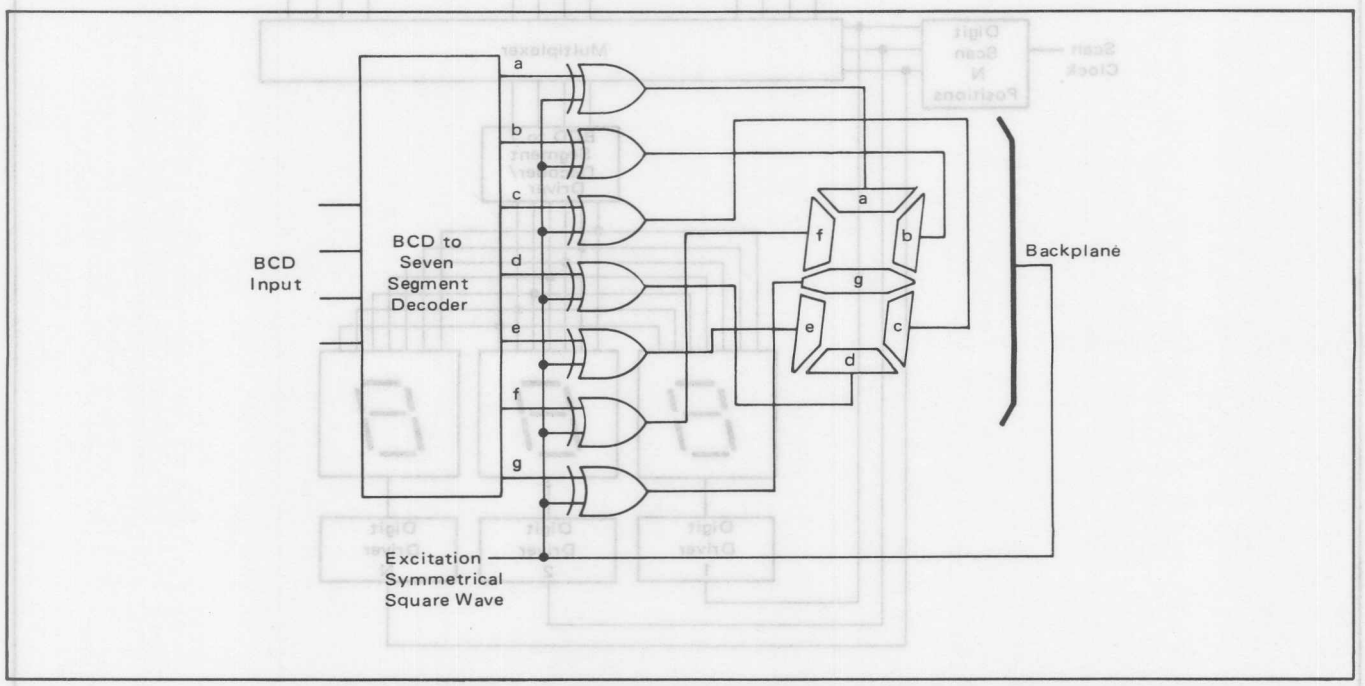


FIGURE 3(a) – Drive Signal for LCD Using Exclusive OR Gates

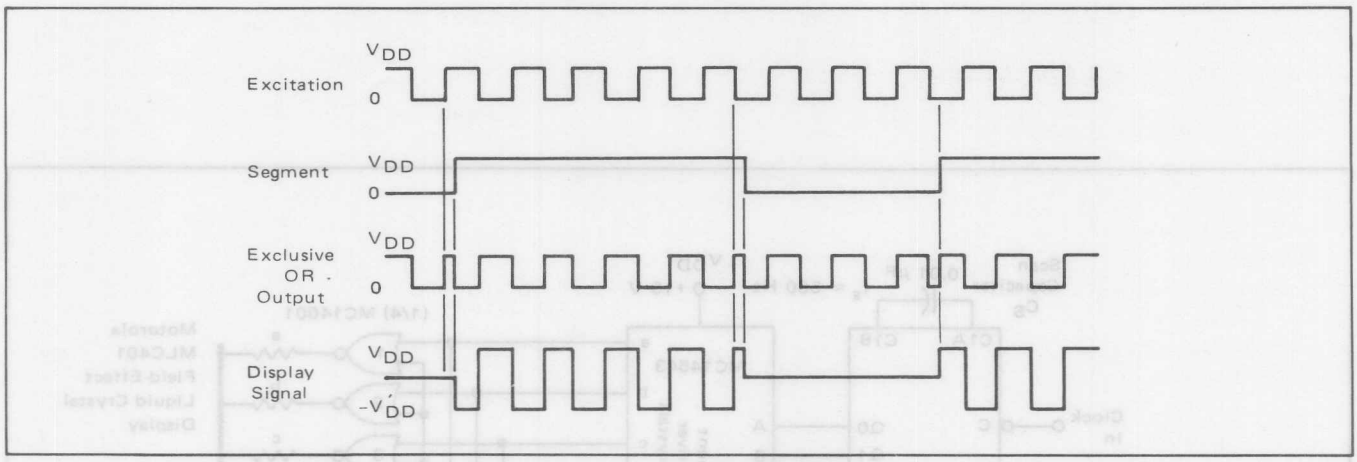


FIGURE 3(b) – LCD Waveforms

CMOS, with its extremely low input power requirements and large power supply operating range, is ideally suited for driving LCDs, particularly for battery operated equipment. In the example of Figure 4, the BCD inputs are generated from the four cascaded up counters (two MC14518 Dual BCD up counters) whose respective outputs feed the MC14543, a decoder designed specifically for driving LCDs. This device contains the required Exclusive OR gates, with the excitation signal applied to the Phase (Ph) input. When a 15 Volt power supply is used, a display excitation voltage of 30 Vp-p is generated, a value compatible with both dynamic scattering and field-effect displays.

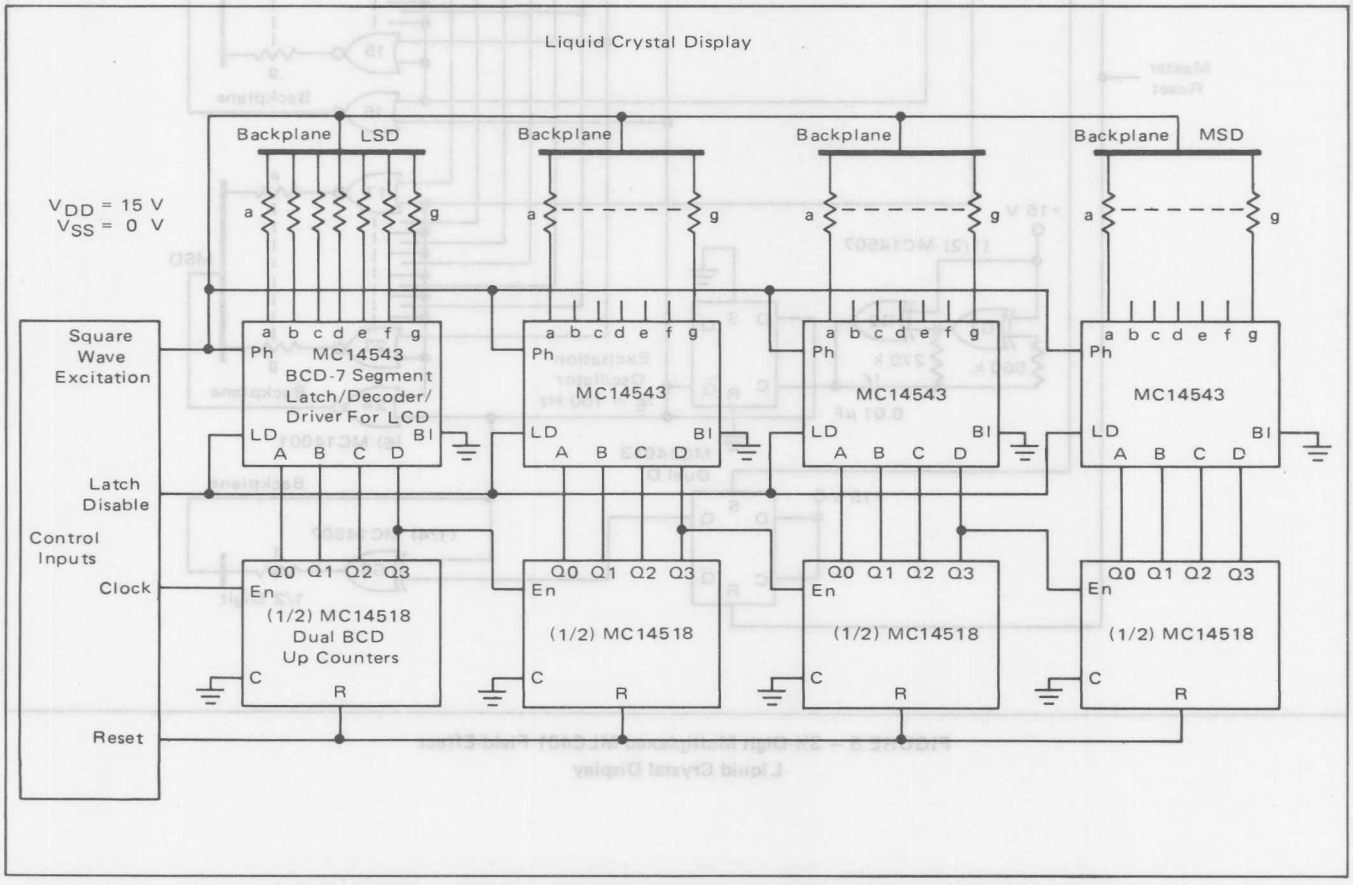


FIGURE 4 – 4-Digit Direct Drive Liquid Crystal Display (LCD)

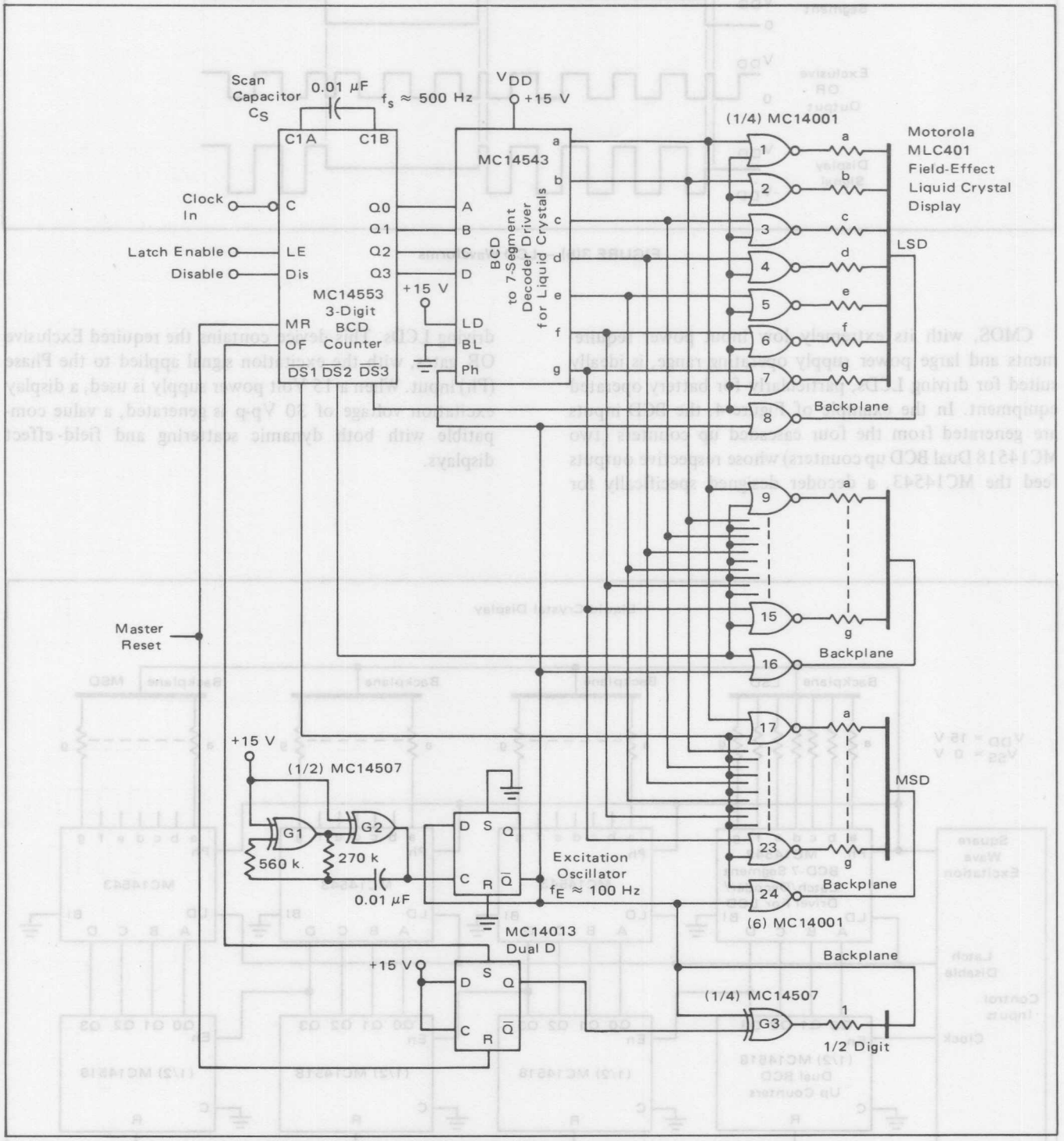


FIGURE 5 – 3½-Digit Multiplexed MLC401 Field-Effect Liquid Crystal Display

MULTIPLEXED FIELD-EFFECT LIQUID CRYSTAL DISPLAY

Experimentation has shown that a LCD will ultimately reach its maximum contrast when it is continually pulsed with a low duty cycle waveform, even when the pulse width is much less than the display turn-on time. This integrating effect is similar to that of a capacitor being charged by a series of pulses. The total time to reach full contrast was in the one hundred to four hundred milliseconds range, well within the requirements for display applications.

Of the two basic types of LCDs, the dynamic scattering and the field-effect, the excitation voltage is less for the latter with a corresponding lower threshold voltage (the voltage level at which the device switches from off to on). When the duty cycle of the excitation voltage is varied, the effective threshold varies inversely. Thus, as the number of multiplexed LCD digits increase (duty cycle decreases), the threshold, and therefore the required power supply, also must increase. For dynamic scattering liquid crystals, the required power supply would be beyond the range of the CMOS ICs, and therefore, the following technique is limited to field-effect LCDs.

The 3-1/2 digit LCD multiplexer described here (Figure 5), which incorporates the MLC401 readout, uses this technique and is a simple, inexpensive variation of the classic multiplexed display system. The three digit BCD counters and respective latches, and the multiplexer and scan circuitry are all contained in one CMOS package, the MC14553 Three-Digit BCD Counter. The time division multiplexed BCD outputs are fed to the inputs of the MC14543 BCD to Seven Segment Latch/Decoder/Driver for Liquid Crystals. For other types of displays (LED, incandescent, etc.), the digits can be strobed by simply scanning the digit drivers. Thus, all common digit segments can be tied to their respective decoder outputs. However, for LCDs, this approach cannot be used since the display will always see a signal across it even when the backplane (digit select) is not strobed. The resultant segment signal is single ended and thus has a deleterious dc component.

When gates are placed in series with the segment lines, the display can readily be strobed. For this example, MC14001 Quad Two Input NOR Gates are used with the control inputs being the negative going digit select pulses from the MC14553 scan circuit. During the non-select time when the scan output is high, the outputs of the NOR gates will be low regardless of the state of the excitation signal and zero voltage will be present across the MLC401 display (Figure 6). During the select low level, the gate outputs will be controlled by the decoder output and excitation signal, and that digit will operate as a direct driven system.

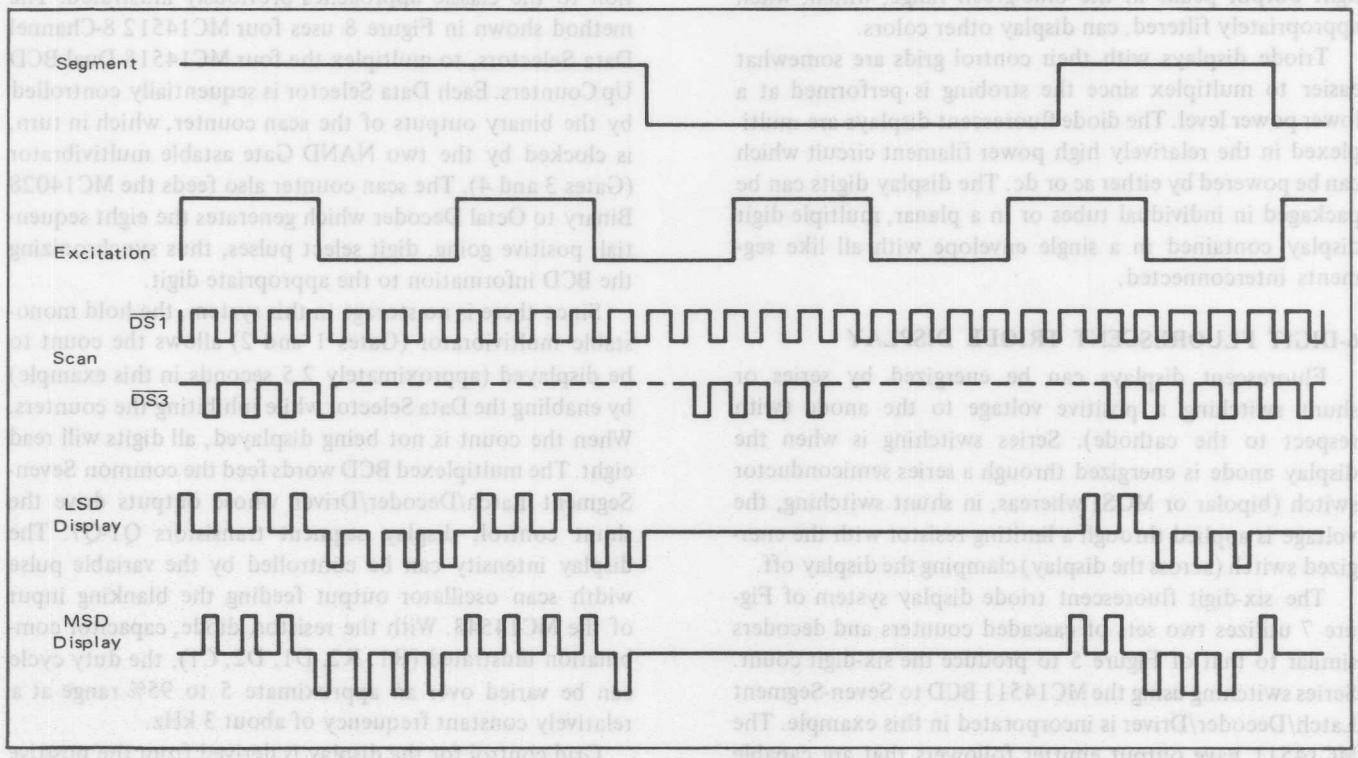


FIGURE 6 – Multiplexed Waveforms for LCDs

The excitation frequency for the field-effect liquid crystal display can vary from 60 Hz to 10 kHz with the 100 Hz used in this example being derived from the two CMOS gate (G1 and G2), toggle flip/flop square wave oscillator. This circuit ensures that the excitation signal will have an exact 50% duty cycle with no dc component. No apparent difference in display presentation was noted when the frequency was varied across the specified range. The scan frequency, using capacitor C_S and the MC14553 internal oscillator, was set for approximately 500 Hz resulting in a display refresh rate of approximately 170 Hz ($\frac{500}{3}$), a frequency well beyond the detectable flicker rate of 30 to 60 Hz. The effective threshold voltage for a three digit scan (33% duty cycle) was approximately 6.5 V. The use of a 15 V power supply ensures that the device is driven well above threshold, the resulting LCD voltage being approximately 30 Vp-p.

FLUORESCENT DISPLAYS

Fluorescent displays, both the diode and triode types, are electrically similar to their vacuum tube counterpart, the exception being that the anodes are coated with a phosphor. When a positive potential is placed across the anode and the directly heated cathode (filament), the electrons impinging on the anode will cause the phosphor to fluoresce and emit light over a broad spectrum. The light output peaks in the blue-green range, which, when appropriately filtered, can display other colors.

Triode displays with their control grids are somewhat easier to multiplex since the strobing is performed at a lower power level. The diode fluorescent displays are multiplexed in the relatively high power filament circuit which can be powered by either ac or dc. The display digits can be packaged in individual tubes or in a planar, multiple digit display contained in a single envelope with all like segments interconnected.

6-DIGIT FLUORESCENT TRIODE DISPLAY

Fluorescent displays can be energized by series or shunt switching a positive voltage to the anode (with respect to the cathode). Series switching is when the display anode is energized through a series semiconductor switch (bipolar or MOS) whereas, in shunt switching, the voltage is applied through a limiting resistor with the energized switch (across the display) clamping the display off.

The six-digit fluorescent triode display system of Figure 7 utilizes two sets of cascaded counters and decoders similar to that of Figure 5 to produce the six-digit count. Series switching using the MC14511 BCD to Seven-Segment Latch/Decoder/Driver is incorporated in this example. The MC14511 have output emitter followers that are capable of sourcing the required anode currents and can thus directly drive the display. The cathodes of the display are set at approximately -18 V derived from the -28 V supply and the 10 V series zener diode D1.

Digit scanning is accomplished by turning on the grid control PNP transistors (Q1-Q3) with the negative going digit select outputs of one MC14533. This switches the grid from the OFF -28 V condition to the ON approximately +15 V value. The zener diode insures that the grid-cathode is back biased in the off mode and satisfies this display's specification of -7 V minimum grid cut-off voltage. When energized, the display will thus have approximately 32 across it ($V_{OH} + |V1| - V_Z = 14 + 28 - 10$). Limiting resistors (R1-R3) are required when interfacing between a 15 V powered CMOS gate and bipolar transistor to prevent the current into the gate from exceeding 10 mA. For high temperature operation, emitter-base resistors are recommended for I_{CBO} considerations. In this example, filament power is supplied by a floating 1.5 Vdc supply referenced to the -18 V cathode, but it can also be powered by a 1.5 Vrms transformer secondary.

Timing for the MC14553 counters are derived from one CMOS IC MC14572 with the Disable pulse obtained from the two inverter, non-symmetrical, astable multivibrator. Diode D2 allows the timing capacitor C1 to charge and discharge through two resistive paths, R7 for the long count duration time and R7 in parallel with R8 for the short, positive going, approximately 100 ms wide Disable pulse. The Latch Enable and Master Reset pulses are obtained from the three, cascaded, half monostable circuits.

8-DIGIT FLUORESCENT TRIODE DISPLAY SYSTEM

There are several ways of multiplexing displays in addition to the classic approaches previously illustrated. The method shown in Figure 8 uses four MC14512 8-Channel Data Selectors, to multiplex the four MC14518 Dual BCD Up Counters. Each Data Selector is sequentially controlled by the binary outputs of the scan counter, which in turn, is clocked by the two NAND Gate astable multivibrator (Gates 3 and 4). The scan counter also feeds the MC14028 Binary to Octal Decoder which generates the eight sequential, positive going, digit select pulses, thus synchronizing the BCD information to the appropriate digit.

Since there is no storage in this system, the hold monostable multivibrator (Gates 1 and 2) allows the count to be displayed (approximately 2.5 seconds in this example) by enabling the Data Selector while inhibiting the counters. When the count is not being displayed, all digits will read eight. The multiplexed BCD words feed the common Seven-Segment Latch/Decoder/Driver whose outputs drive the shunt control, display segment transistors Q1-Q7. The display intensity can be controlled by the variable pulse width scan oscillator output feeding the blanking input of the MC14543. With the resistor, diode, capacitor combination illustrated (R1, R2, D1, D2, C1), the duty cycle can be varied over an approximate 5 to 95% range at a relatively constant frequency of about 3 kHz.

Grid control for the display is derived from the positive going Octal Decoder outputs directly driving the NPN-PNP cascaded transistor pairs (Q9-Q24). The maximum specified grid current of 5 mA is limited by the single, time-shared, emitter resistor R12. The sixteen grid control transistors are in four MPQ6600 quad complementary pair packages. The segments and decimal point anode drive

transistors are in two MPQ2221 quad packages. Using a 36 V supply, the display voltage is approximately 30 V with zener diode D3 ensuring that the grid is appropriately cut-off.

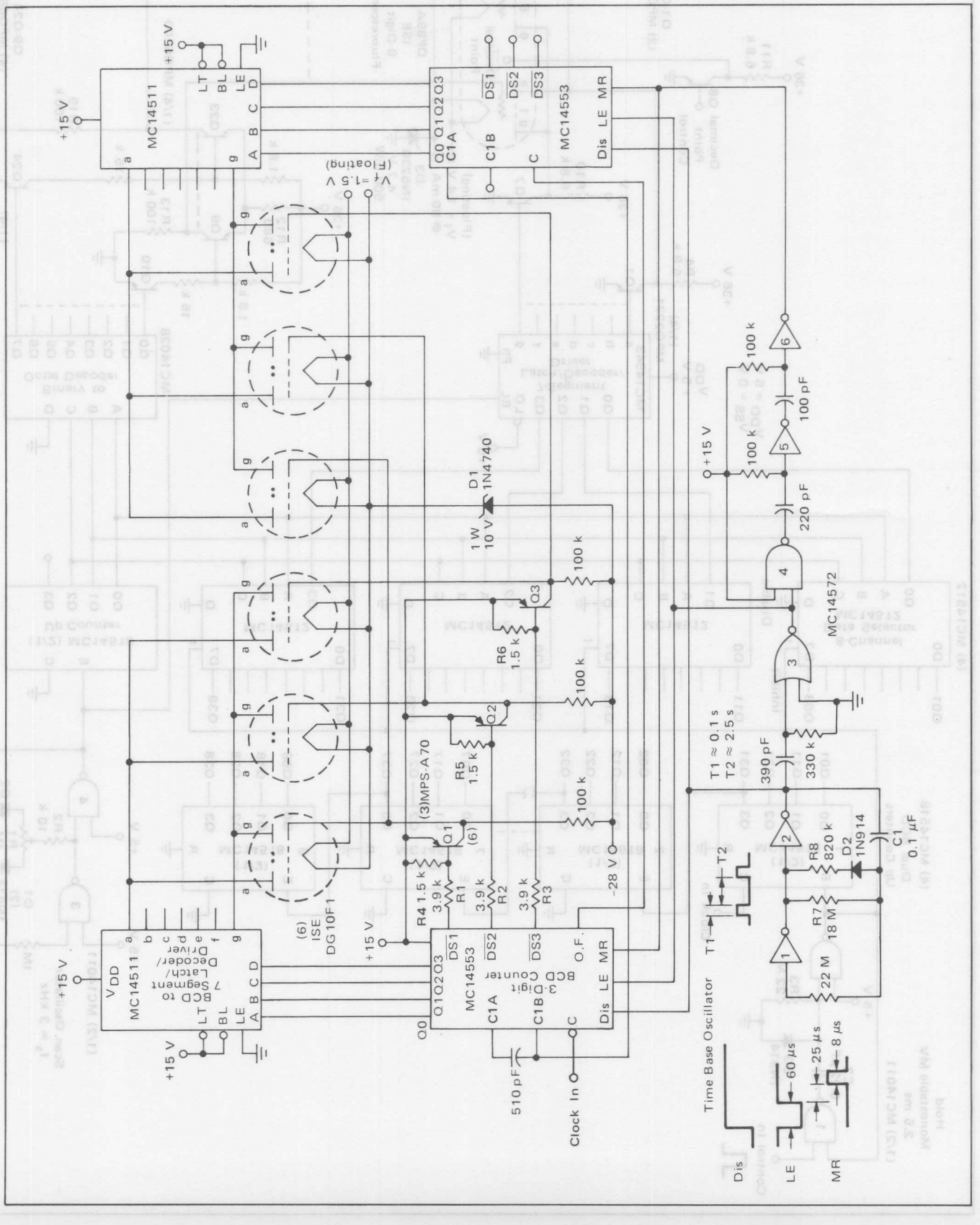
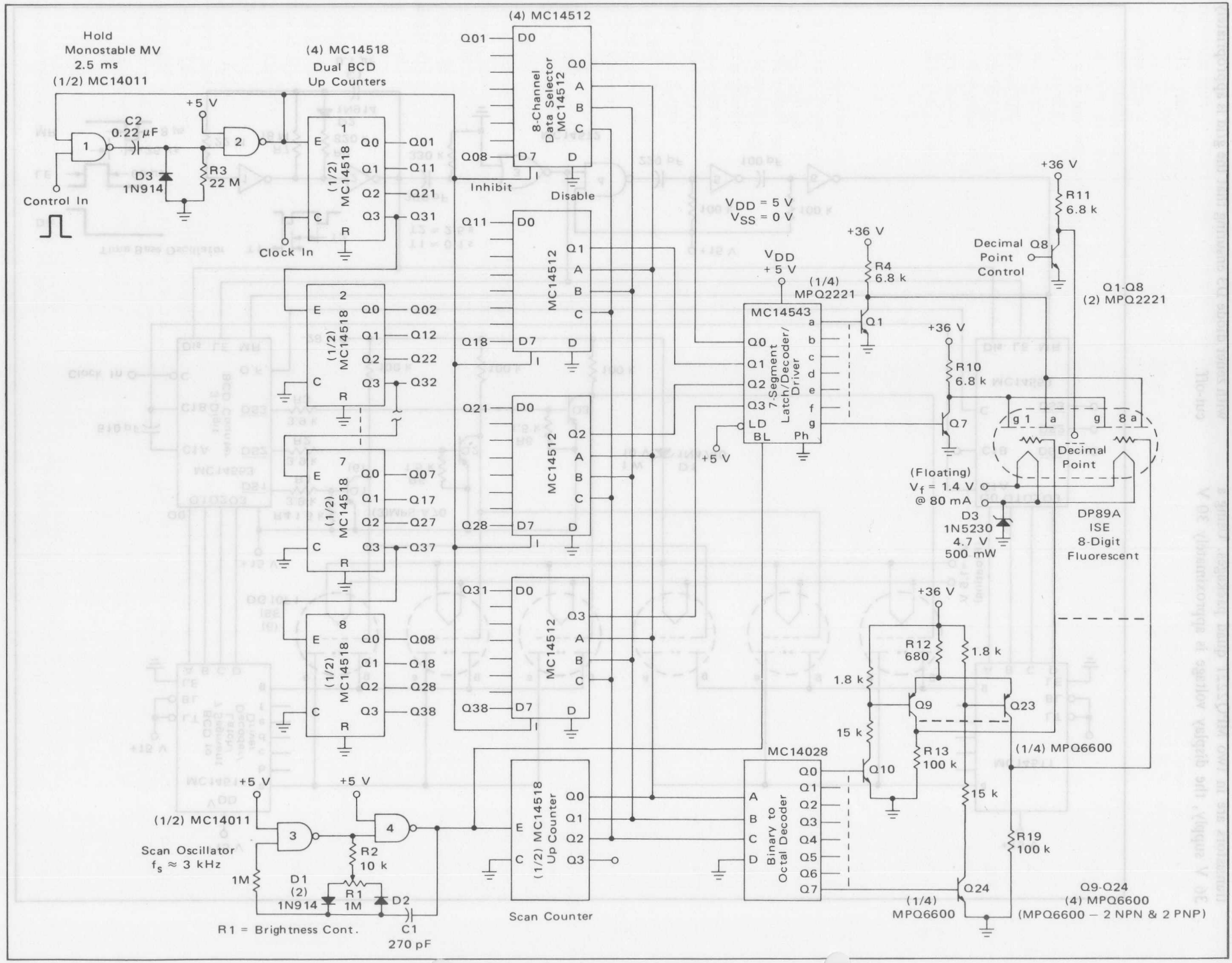


FIGURE 7 – 6-Digit Fluorescent Triode Display



IGURE 8 – 8-Digit Fluorescent Triode Display System

REAL TIME 5-DIGIT FLUORESCENT DIODE DISPLAY

A real time 5 decade counter using only three ICs is described in Figure 9. The key element in this system is the MC14534 which contains a five decade ripple counter with the output time multiplexed by an internal scanner. The scanning rate is controlled by the two inverter (4, 5) astable multivibrator. The multiplexed BCD outputs are fed to the MC14543 Seven-Segment Decoder whose output polarity is controlled by the logic level applied to the Phase input. This feature allows many types of displays to be controlled.

The MC14534 was specifically designed for real time applications where continual updating is required. To allow for display presentation time, the display gate multivibrator (2, 3) generates the non-symmetrical, approximately 2 second gate which is fed to one input of the clock NAND gate (1). The clock pulse is thus inhibited for this 2 second period and the present BCD information in the MC14534 counters is displayed. When the display gate output goes low (approximately 0.5 seconds), the counters are clocked. Since there is no synchronization between the clock input and the display gate for this illustration, the count can possibly be in error by ± one count.

Five digit fluorescent diode displays can readily be interfaced with this system. In this example, shunt switching is employed to control the diode anode segments using the direct coupled NPN transistors (Q1-Q7). Digit selection is accomplished by interrupting the cathode return paths through their respective MPS-U45 Darlington drivers. When the digit select outputs of the MC14534 go high, the drivers saturate, sinking both the display filament current and anode segment current, thus energizing the selected digit. The nominal, direct drive, specified filament voltage and current for the fluorescent diode display is 1.6 V at 45 mA. When scanning 5 digits (20% duty cycle), the multiplexed filament power must be equal to that of the direct driven case.

Expressed mathematically,

$$A_{rms} = A(t_0/T)^{1/2}$$

where

A_{rms} = rms filament voltage = 1.6 V
t_0/T = duty cycle = 0.2 for 5 digits
A = amplitude of multiplexed filament voltage

Solving for A results in

$$A = \frac{1.6}{(0.2)^{1/2}} = 3.6 \text{ V}$$

If this peak voltage were continually applied to a filament due to a malfunction of the scan circuits, the life of the display would be greatly degraded. The display protection circuit, using the remaining inverter of the MC14572 and a voltage doubler input, monitors the Scanner Clock and controls the filament driver transistor Q13. The diodes in series with the filaments (D1-D5) prevent erroneous readings of other digits by conduction through the still hot (due to thermal inertia) filament and the filament supply. The filament voltage is derived from the +5 V logic supply and would be approximately 3.3 V, approximating the desired 3.6 V. ($V_f = V_{CC} - V_{CE(sat)}$ Q13 $- V_D - V_{CE(sat)}$ Q8 = 5.0 -0.2 -0.7 -0.8 ≃ 3.3 V).

At this voltage, the filament current is approximately 90 mA. The MPS-U45 Darlington digit drivers must sink this 90 mA plus an average of 10 mA total segment currents. The worst case, low temperature h_{FE} for the MPS-U45 was approximated to be 2000. A forced h_{FE} of 500 was chosen which thus ensures interfacing with the MC14534. In order to maintain the equivalent light output as in direct drive mode, the supply voltage should be increased. For this 20% duty cycle example, 40 V was used which resulted in an anode voltage and current of approximately 28 V and 1.7 mA respectively when the anode load resistor R1 equals 6.8 k.

LIGHT-EMITTING DIODES – LED

LED displays have taken over an appreciable part of the display business in the last several years primarily due to their high reliability, long life, fast response time, operation from low voltage dc and ready adaptability to miniature displays. LEDs are semiconductor PN junction diodes which produce light due to recombination of holes and electrons when forward biased. The semiconductor material is either gallium arsenide phosphide (GaAsP) or gallium phosphide (GaP) with the former being more prevalent in red display applications. Similar to any junction diode, the voltage drop across the forward biased junction will be relatively constant (approximately 1.6 V for GaAsP) and is generally driven with a constant current source. There are two possible connections when LEDs are used as seven segment displays, common cathode and common anode. Common cathode displays require the drive circuit to supply current (source) to the segments, whereas common anode requires segment drive circuit sink capability. Because of their low voltage and relatively small current requirements, LED displays can be readily interfaced with most families of integrated circuits. When such ICs lack the drive capability, transistors can be easily interfaced between the ICs and the display.

5-DIGIT LED DISPLAY

Typical GaAsP LED currents are in the 5 to 30 mA per segment range, generally varying with the size of the display. The light output and luminous efficiency (light output/unit current) increase with increasing forward current until saturation occurs (100 to 150 mA range). These properties make it advantageous to strobe LEDs so that, for the same average current, with lower duty cycles, the peak current, and thus the light output, will be greater.

An illustration of a 5-digit LED display using the same real time 5 decade counter system as in the previous fluorescent diode example is shown in Figure 10. This display system was designed for a peak forward current of approximately 40 mA (40/5 = 8 mA average). The MC75491 Quad and MC75492 Hex MOS to LED Drivers are ideally suited for this multiplexing application as only

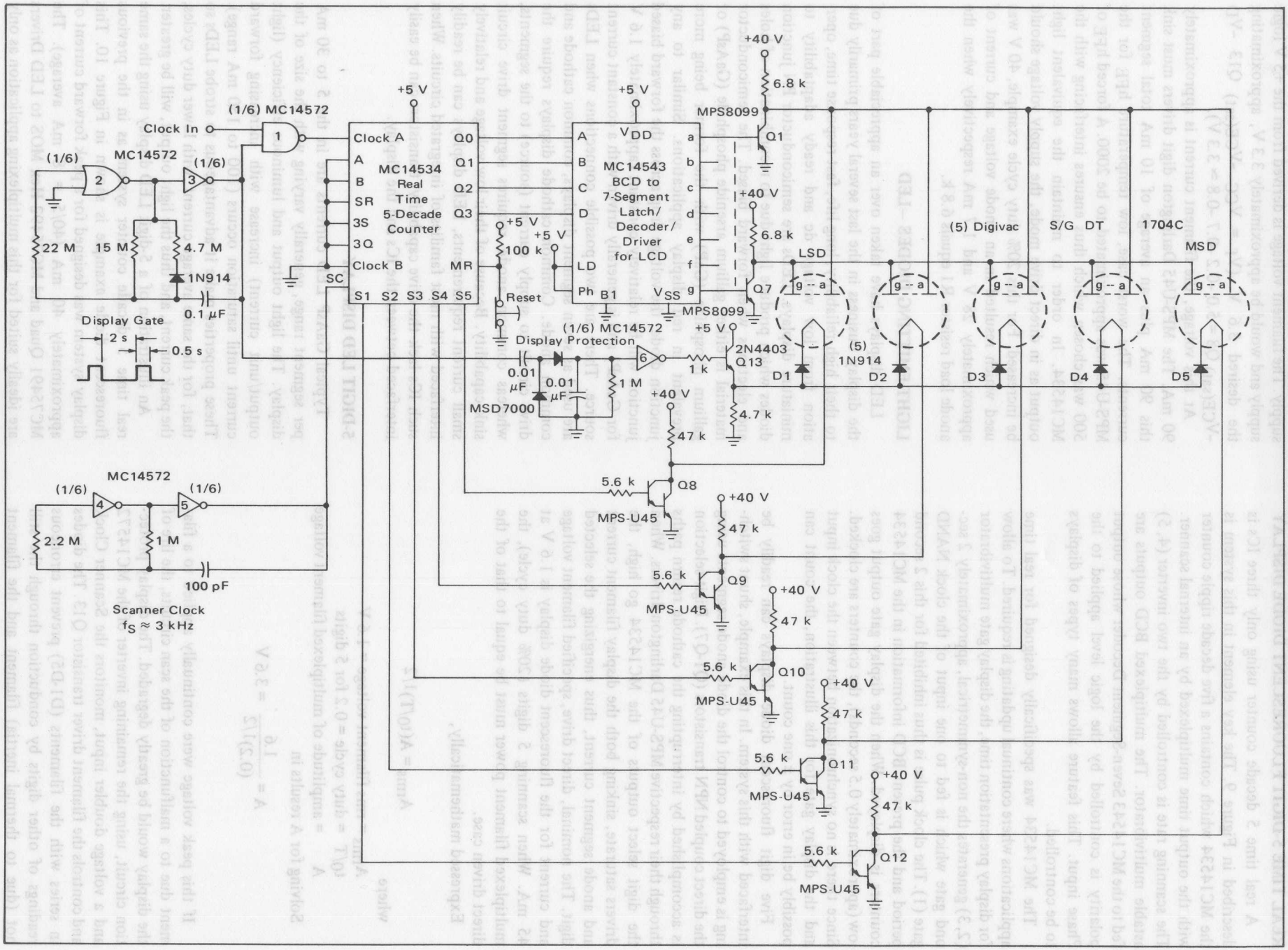


FIGURE 9 – Real Time 5-Digit Fluorescent Diode Display System

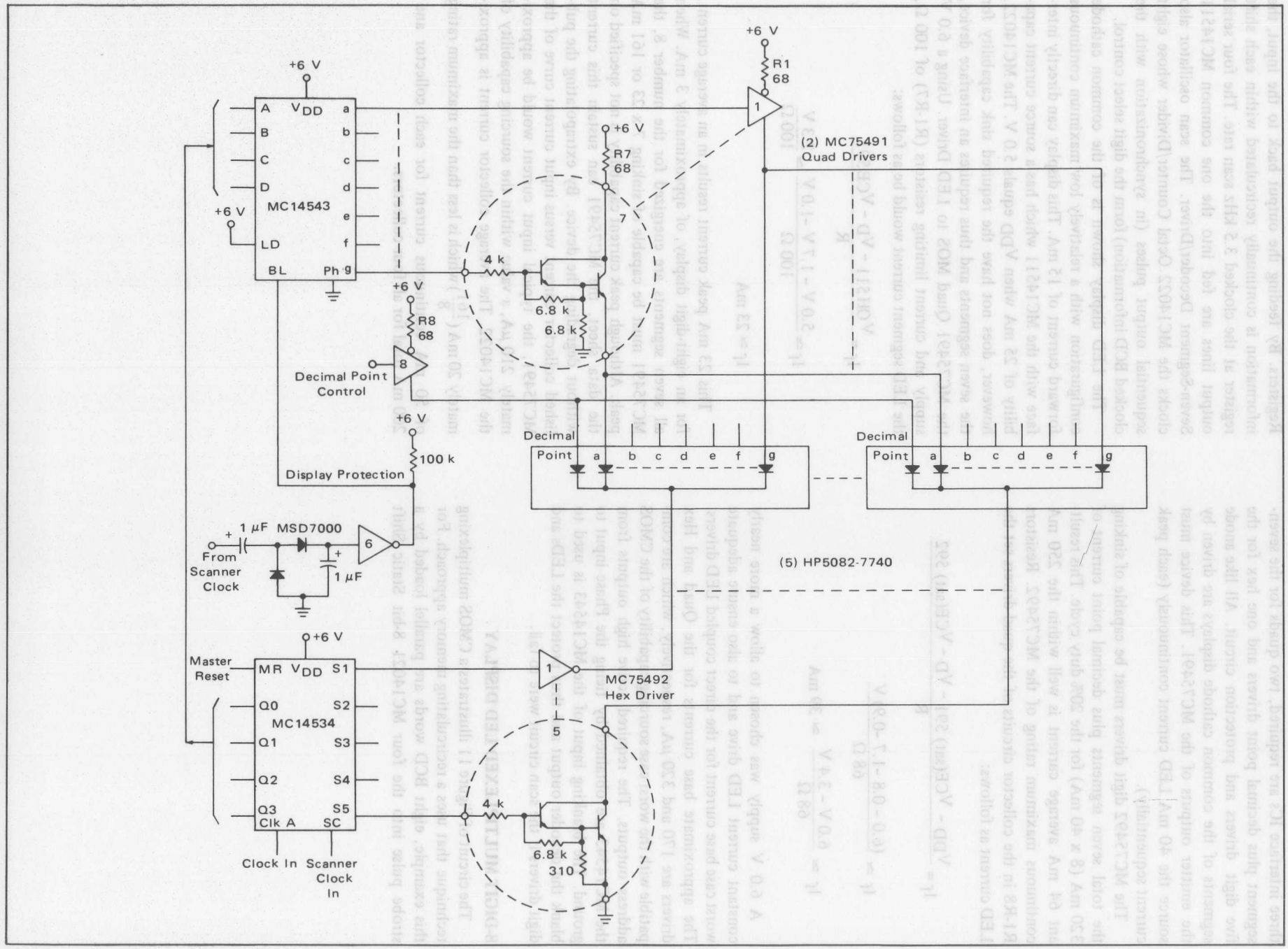


FIGURE 10 – 5-Digit LED Display

three interface ICs are required, two quads for the seven-segment plus decimal point drivers and one hex for the five digit drivers and protection circuit. All like anode segments of the common cathode displays are driven by the emitter outputs of the MC75491. This device must source the 40 mA LED current continuously (each peak current sequentially).

The MC75492 digit drivers must be capable of sinking the total seven segments plus decimal point current of 320 mA (8 x 40 mA) for the 20% duty cycle. This resultant 64 mA average current is well within the 250 mA continuous maximum rating of the MC75492. Resistors R1-R8 in the collector circuits of the quad drivers set the LED current as follows:

$$I_f = \frac{V_{DD} - V_{CE(sat)\ 591} - V_D - V_{CE(sat)\ 592}}{R}$$

$$I_f \simeq \frac{(6.0 - 0.8 - 1.7 - 0.9)\ V}{68\ \Omega}$$

$$I_f \simeq \frac{6.0\ V - 3.4\ V}{68\ \Omega} \simeq 39\ mA$$

A 6.0 V supply was chosen to allow a more nearly constant current LED drive and to also ensure adequate worst case base current for the direct coupled LED drivers. The approximate base currents for the Quad and Hex drivers are 170 and 320 μA, respectively, which are compatible with the worst case sourcing capability of the CMOS address outputs. The required active high outputs from the MC14543 are obtained by tieing the Phase input to ground. The blanking input of the MC14543 is used to blank the decoder output and thus protect the LEDs and digit drivers if the scan circuit were to fail.

8-DIGIT MULTIPLEXED LED DISPLAY

The circuit of Figure 11 illustrates a CMOS multiplexing technique that uses a recirculating memory approach. For this example, eight BCD words are parallel loaded by a strobe pulse into the four MC14021 8-bit Static Shift Registers. By feeding the output back to the input, the information is continually recirculated within each shift register at the clocked 3.5 kHz scan rate. The four serial output lines are fed into the one common MC14511 Seven-Segment Decoder/Driver. The scan oscillator also clocks the MC14022 Octal Counter/Divider whose eight sequential output pulses (in synchronization with the clocked BCD information) form the digit select control.

The LED display shown is of the common cathode configuration with a relatively low maximum continuous forward current of 15 mA. This display can directly interface with the MC14511 which has a source current capability of 25 mA when V_{DD} equals 5.0 V. The MC14022, however, does not have the required sink capability for the seven segments and thus requires an interface device, the MC75491 Quad MOS to LED Driver. Using a 6.0 V supply and current limiting resistors (R1-R7) of 100 Ω, the LED segment current would be as follows:

$$I_f = \frac{V_{OH511} - V_D - V_{CE591}}{R}$$

$$I_f \simeq \frac{5.0\ V - 1.7\ V - 1.0\ V}{100\ \Omega} \simeq \frac{2.3\ V}{100\ \Omega}$$

$$I_f \simeq 23\ mA$$

This 23 mA peak current results in an average current, for an eight-digit display, of approximately 3 mA. When all seven segments are energized for the number 8, the MC75491 must be capable of sinking 7 x 23 or 161 mA peak. Although peak current capability is not specified on the data sheet, the MC75491 can sustain this current without degrading the device. By extrapolating the published collector current versus input current curve of the MC75491, the typical input current would be approximately 210 μA, a value within the sourcing capability of the MC14022. The average collector current is approximately 20 mA ($\frac{161}{8}$) which is less than the maximum rating of 50 mA continuous current for each collector and 200 mA total for all four collectors.

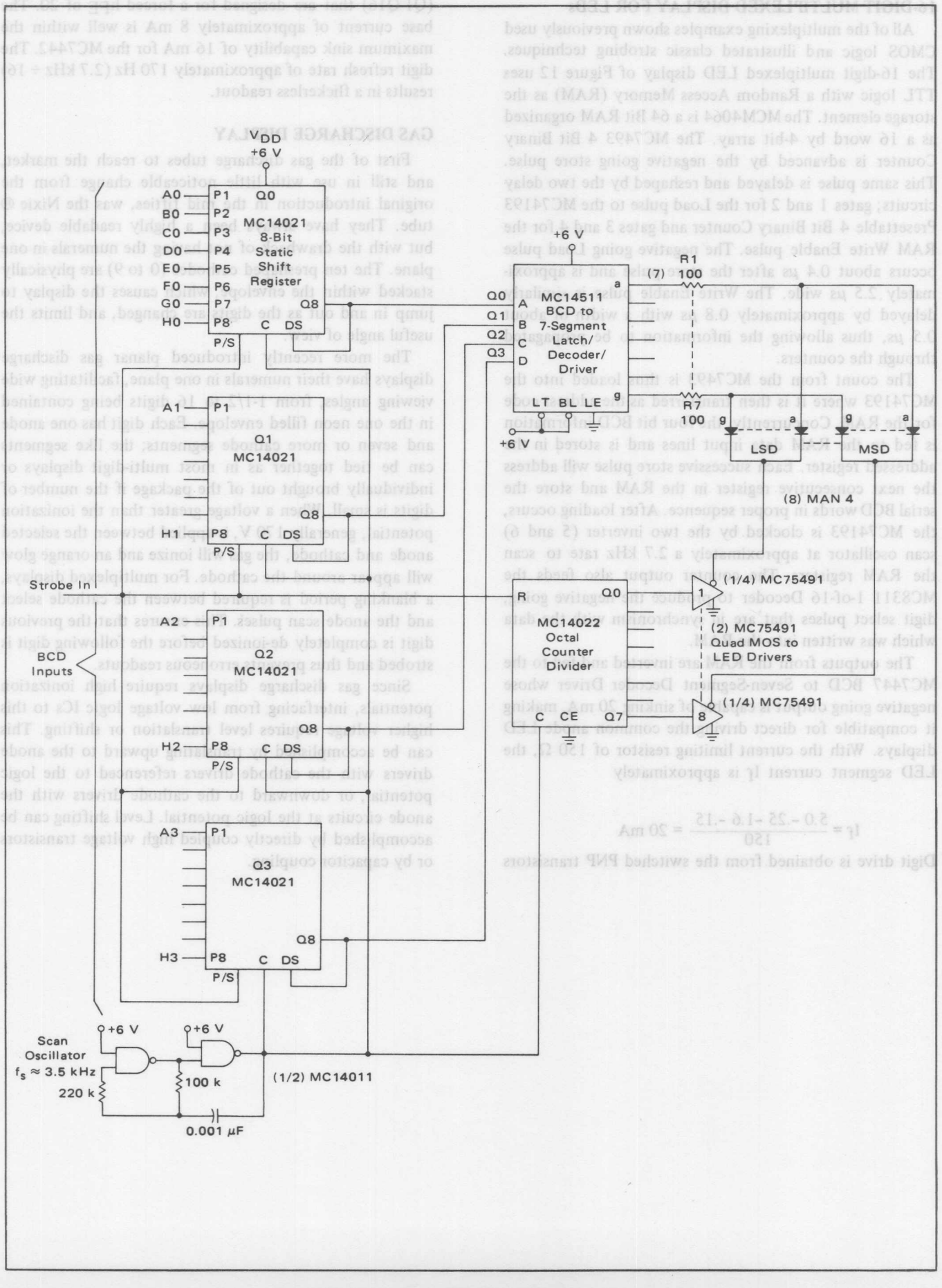


FIGURE 11 – 8-Digit Multiplexed LED Display

16-DIGIT MULTIPLEXED DISPLAY FOR LEDs

All of the multiplexing examples shown previously used CMOS logic and illustrated classic strobing techniques. The 16-digit multiplexed LED display of Figure 12 uses TTL logic with a Random Access Memory (RAM) as the storage element. The MCM4064 is a 64 Bit RAM organized as a 16 word by 4-bit array. The MC7493 4 Bit Binary Counter is advanced by the negative going store pulse. This same pulse is delayed and reshaped by the two delay circuits; gates 1 and 2 for the Load pulse to the MC74193 Presettable 4 Bit Binary Counter and gates 3 and 4 for the RAM Write Enable pulse. The negative going Load pulse occurs about 0.4 μs after the store pulse and is approximately 2.5 μs wide. The Write Enable pulse is similarly delayed by approximately 0.8 μs with a width of about 0.5 μs, thus allowing the information to be propagated through the counters.

The count from the MC7493 is thus loaded into the MC74193 where it is then transferred as the address code for the RAM. Concurrently, the four bit BCD information is fed to the RAM data input lines and is stored in the addressed register. Each successive store pulse will address the next consecutive register in the RAM and store the serial BCD words in proper sequence. After loading occurs, the MC74193 is clocked by the two inverter (5 and 6) scan oscillator at approximately a 2.7 kHz rate to scan the RAM registers. The counter output also feeds the MC8311 1-of-16 Decoder to produce the negative going, digit select pulses that are in synchronism with the data which was written into the RAM.

The outputs from the RAM are inverted and fed to the MC7447 BCD to Seven-Segment Decoder Driver whose negative going output is capable of sinking 20 mA, making it compatible for direct driving the common anode LED displays. With the current limiting resistor of 150 Ω, the LED segment current I_f is approximately

$$I_f = \frac{5.0 - .25 - 1.6 - .15}{150} = 20 \text{ mA}$$

Digit drive is obtained from the switched PNP transistors (Q1-Q16) that are designed for a forced h_{FE} of 20. The base current of approximately 8 mA is well within the maximum sink capability of 16 mA for the MC7442. The digit refresh rate of approximately 170 Hz (2.7 kHz ÷ 16) results in a flickerless readout.

GAS DISCHARGE DISPLAY

First of the gas discharge tubes to reach the market, and still in use with little noticeable change from the original introduction in the mid fifties, was the Nixie ® tube. They have always been a highly readable device, but with the drawback of not having the numerals in one plane. The ten preshaped cathodes (0 to 9) are physically stacked within the envelope, which causes the display to jump in and out as the digits are changed, and limits the useful angle of view.

The more recently introduced planar gas discharge displays have their numerals in one plane, facilitating wide viewing angles, from 1-1/2 to 16 digits being contained in the one neon filled envelope. Each digit has one anode and seven or more cathode segments; the like segments can be tied together as in most multi-digit displays or individually brought out of the package if the number of digits is small. When a voltage greater than the ionization potential, generally 170 V, is applied between the selected anode and cathode, the gas will ionize and an orange glow will appear around the cathode. For multiplexed displays, a blanking period is required between the cathode select and the anode scan pulses. This ensures that the previous digit is completely de-ionized before the following digit is strobed and thus prevents erroneous readouts.

Since gas discharge displays require high ionization potentials, interfacing from low voltage logic ICs to this higher voltage requires level translation or shifting. This can be accomplished by translating upward to the anode drivers with the cathode drivers referenced to the logic potential, or downward to the cathode drivers with the anode circuits at the logic potential. Level shifting can be accomplished by directly coupled high voltage transistors or by capacitor coupling.

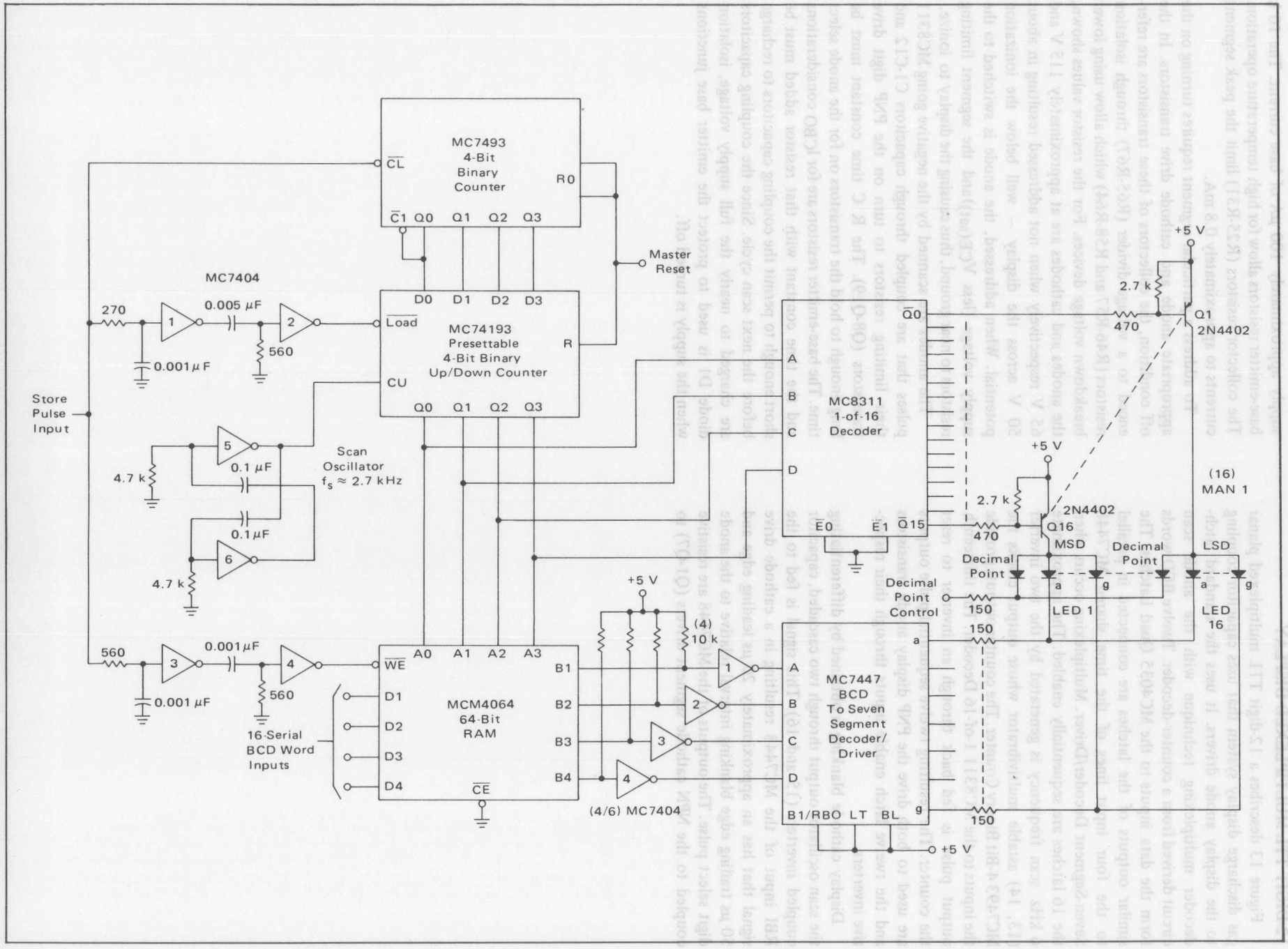


FIGURE 12 – 16-Digit Multiplexed Display for LEDs

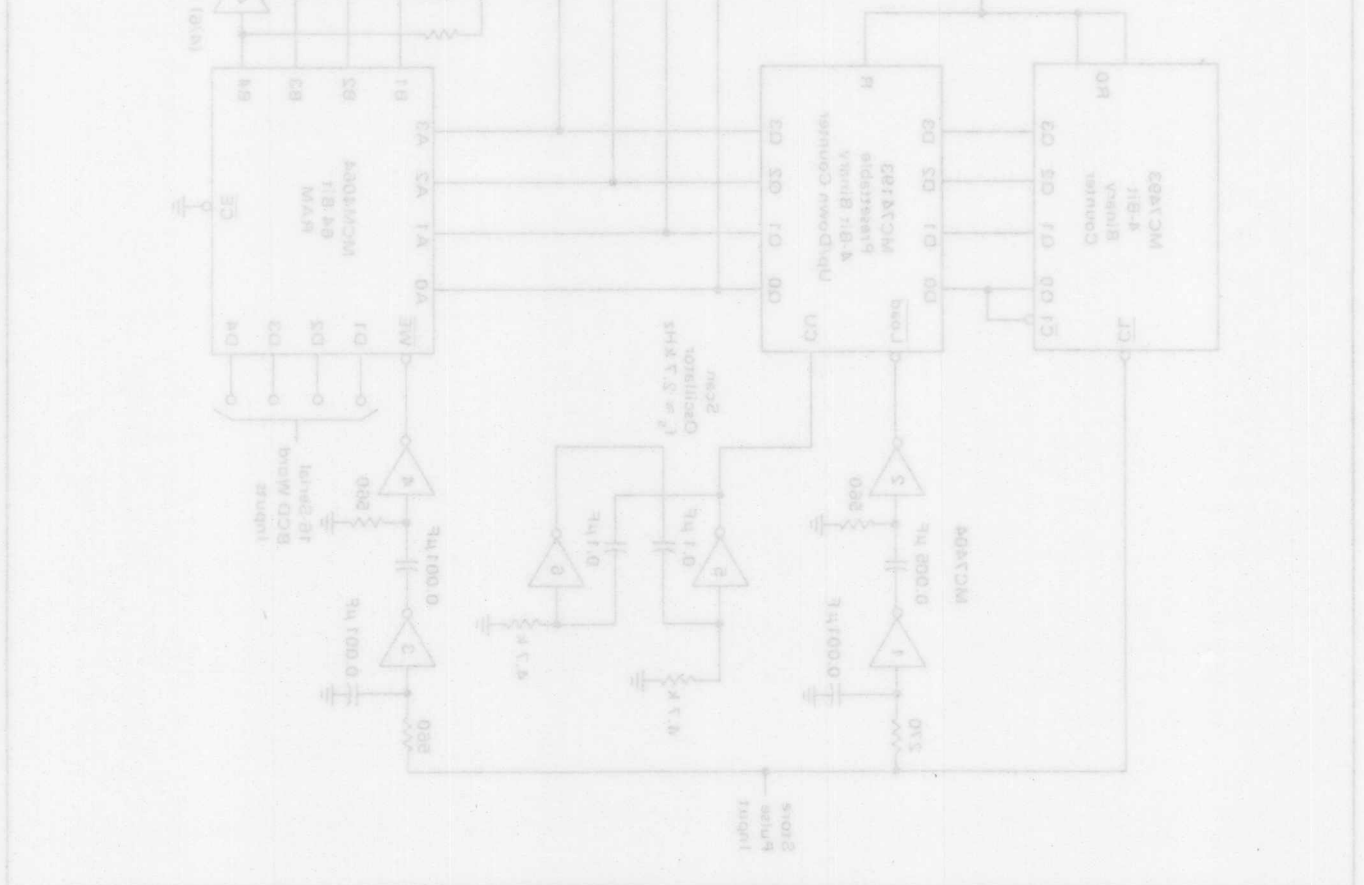
12-DIGIT TTL MULTIPLEXED DISPLAY

Figure 13 describes a 12-digit TTL multiplexed planar gas discharge display system that uses capacitor coupling to the display anode drivers. It uses the standard latch-decoder multiplexing technique with the anode scan circuit derived from a counter-decoder. Twelve BCD words form the data inputs to the MC4035 Quad Latches. The similar outputs of the latches are connected in parallel to the four input lines of the time shared MC7448 Seven-Segment Decoder/Driver. Multiplexing occurs when the 16 latches are sequentially enabled. The approximate 6 kHz scan frequency is generated by the two inverter (13, 14) astable multivibrator whose output clocks the MC7493 4-Bit Binary Counter. The counter outputs provide the inputs to the MC8311 1-of-16 Decoder. The thirteenth output pulse is fed back through an inverter to reset the counter. The resulting twelve sequential pulse outputs are used to both drive the PNP display anode transistors and the twelve latch enable inputs through their respective inverters.

Display cathode blanking is obtained by differentiating the scan oscillator output through two cascaded, capacitor coupled inverters (15 and 16). This signal is fed to the RBI input of the MC7448 resulting in a cathode drive signal that has an approximately 20 μs leading edge and 50 μs trailing edge blanking interval relative to the anode digit select pulse. The outputs of the MC7448 are resistive coupled to the NPN cathode segment drivers (Q1-Q7) to supply approximately 100 μA of base current. The 10 k base-emitter resistors allow for high temperature operation. The collector resistors (R25-R31) limit the peak segment currents to approximately 0.8 mA.

To address a particular segment requires turning on the appropriate anode and cathode drive transistors. In the off condition, the collectors of these transistors are referenced to a voltage divider (R65-R67) through isolation resistors (R46-R57 and R58-R64) which allow using lower breakdown voltage devices. For the resistor values shown, the anodes and cathodes are at approximately 115 V and 65 V respectively when not addressed resulting in about 50 V across the display – well below the ionization potential. When addressed, the anode is switched to the supply voltage (less $V_{CE(sat)}$) and the segment limiting resistors to near ground, thus causing the display to ionize.

The anodes are scanned by the negative going MC8311 pulses that are coupled through capacitors C1-C12 and their limiting resistors to turn on the PNP digit drive transistors (Q8-Q19). The R C time constant must be long enough to hold the transistors on for the anode select time. The base-emitter resistors are for I_{CBO} considerations and the time constant with that resistor added must be short enough to permit the coupling capacitors to recharge before the next scan cycle. Since the coupling capacitors are charged to nearly the full supply voltage, isolation diode D1 is used to protect the emitter base junctions when the supply is turned off.



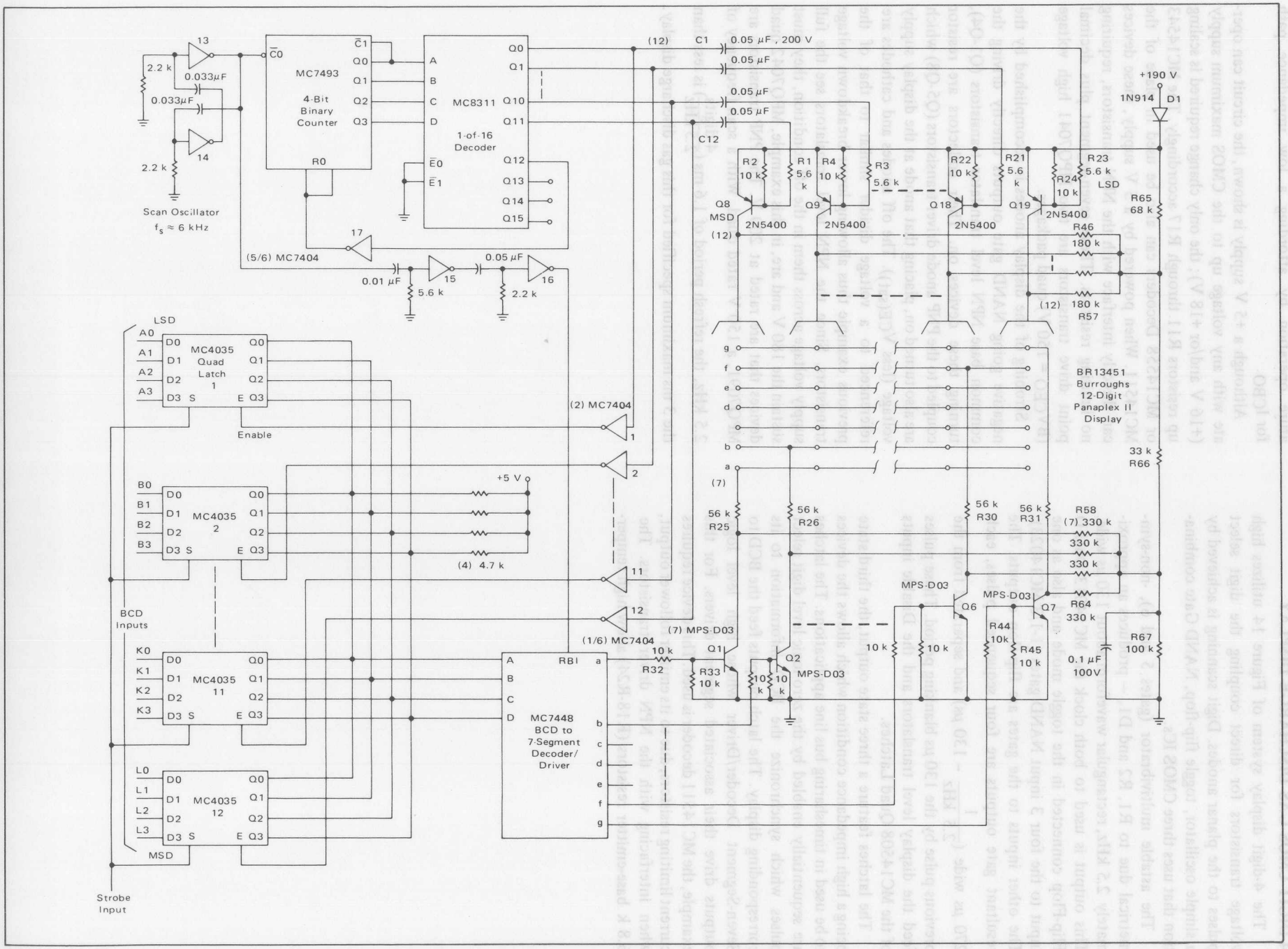


FIGURE 13 – 12-Digit TTL Multiplexed Display Panaplex II

4-DIGIT CMOS GAS DISCHARGE DISPLAY

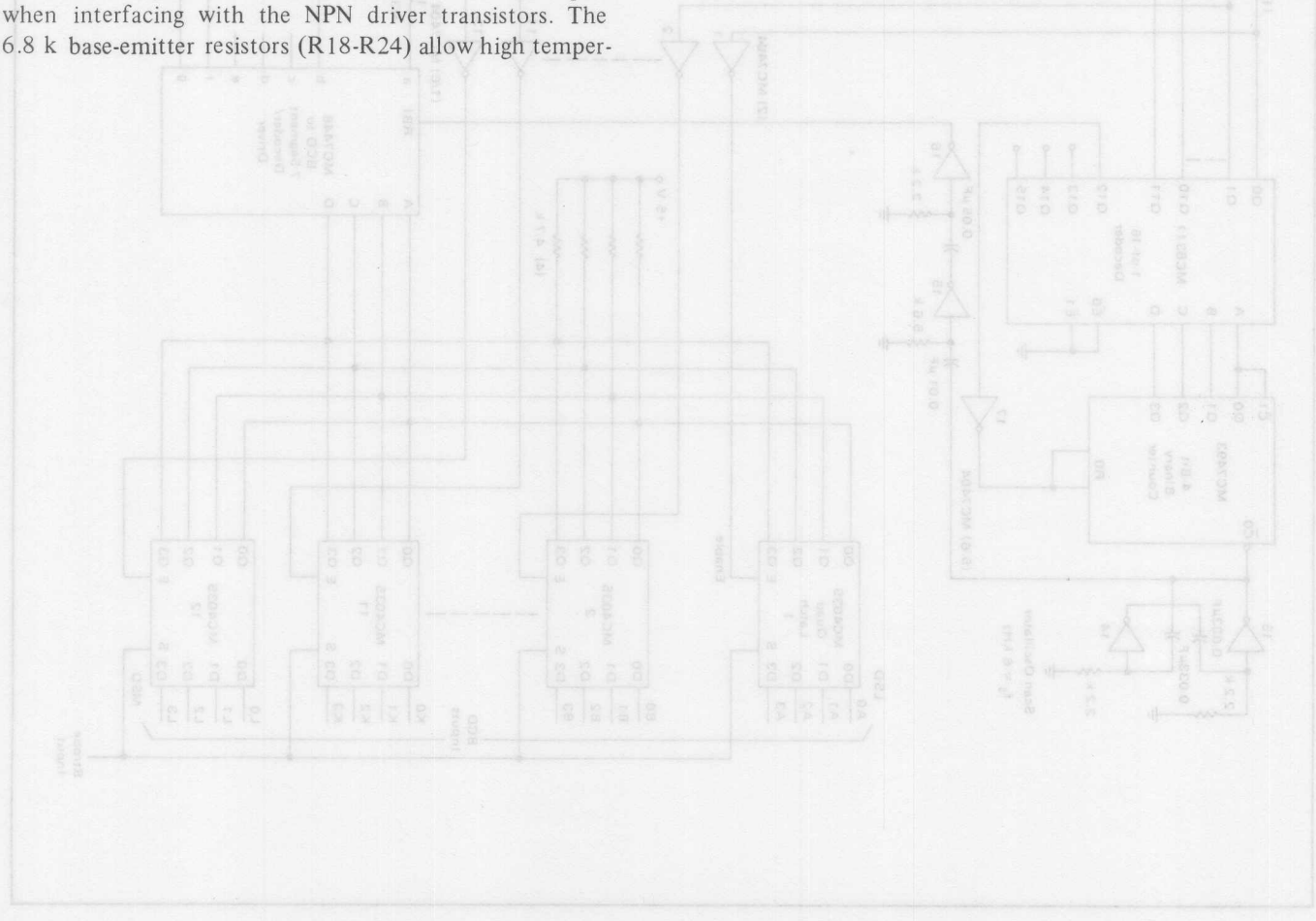
The 4-digit display system of Figure 14 utilizes high voltage transistors for direct coupling the digit select pulses to the planar anodes. Digit scanning is achieved by a simple oscillator, toggle flip-flop, NAND Gate combination that uses three CMOS ICs.

The astable multivibrator (gates 5 and 6), -non-symmetrical due to R1, R2 and D1, – produces an approximately 2.5 kHz, rectangular waveform about 130 μs wide. This output is used to both clock the MC14013 Dual D Flip-Flop connected in the toggle mode and also as one input to the four 3 input NAND gates (1-1/3 MC14023). The other inputs to the gates are flip-flop outputs. The resultant gate outputs are four sequenced pulses, each 270 μs wide ($\frac{1}{2.5\text{ kHz}}$ - 130 μs) and separated from the previous pulse by the 130 μs blanking period. These pulses feed the display level translators and the Disable inputs of the MC14508 Quad Latches.

The latches feature a three state output, the third state being a high impedance condition which allows the devices to be used in timesharing bus line applications. The latches are sequentially enabled by the zero logic level digit select pulses which synchronize the BCD information to its corresponding display. The latch outputs feed the BCD to Seven-Segment Decoder/Driver whose high level logic outputs drive their associated segment drivers. For this example, the MC14511 decoder is used. This device requires current limiting resistors, due to its emitter follower output, when interfacing with the NPN driver transistors. The 6.8 k base-emitter resistors (R18-R24) allow high temperature operation by affording a low impedance path for I_{CBO}.

Although a +5 V supply is shown, the circuit can operate with any voltage up to the CMOS maximum supply (+16 V and/or +18 V); the only change required is scaling up resistors R11 through R17 accordingly. The MC14543 or MC14558 Decoders can also be used in place of the MC14511. When powered by a 5 V supply, these devices can directly interface with the NPN transistors, requiring no limiting resistors. These seven-segment plus decimal point drive transistors are two MPQ7041 high voltage (BV_{CEO} = 150 V) quad packages.

Strobing of the display anodes is accomplished by the negative going NAND gate outputs directly driving the common base NPN level translator transistors (Q1-Q4), turning these devices on. Their collectors are resistor coupled to the PNP anode driver transistors (Q5-Q8) which are also turned on, placing that anode at the display supply voltage (less $V_{CE(sat)}$). The off anodes and cathodes are referenced to a voltage divider similar to that of the previous example thus allowing lower breakdown voltage transistors. Since the NPN level translators see the full supply voltage across them in the off condition, they must sustain the 180 V and are, in this example, MPQ7042 quad devices that are rated at 200 V. The PNP transistors are MPQ7091, a 150 V rated quad. With a scan frequency of 2.5 kHz, the refresh period of 1.6 ms ($\frac{4\text{ digits}}{2.5\text{ kHz}}$) is less than the 3 ms maximum specified for this gas discharge display.



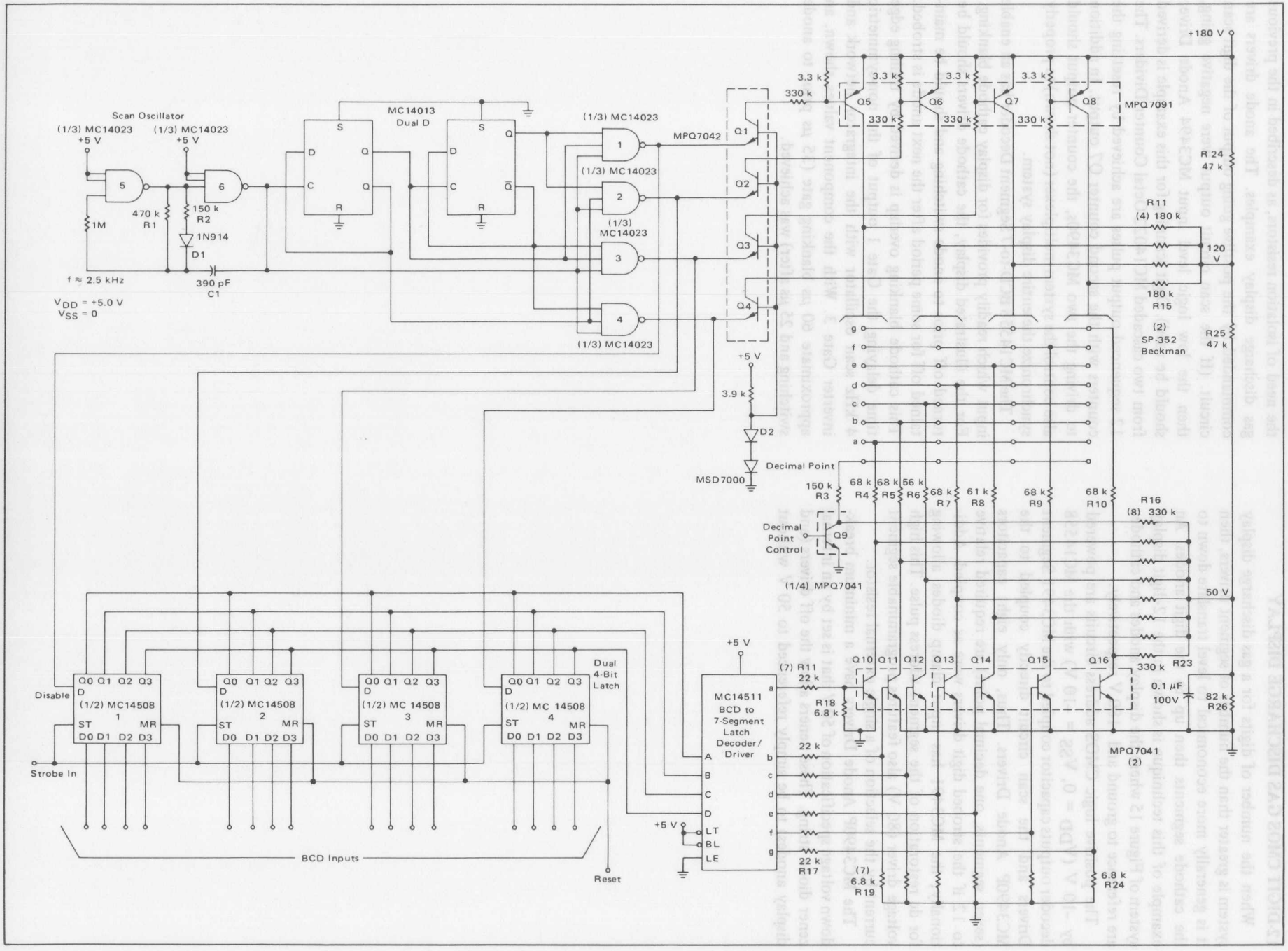


FIGURE 14 – 4-Digit CMOS Gas Discharge Display

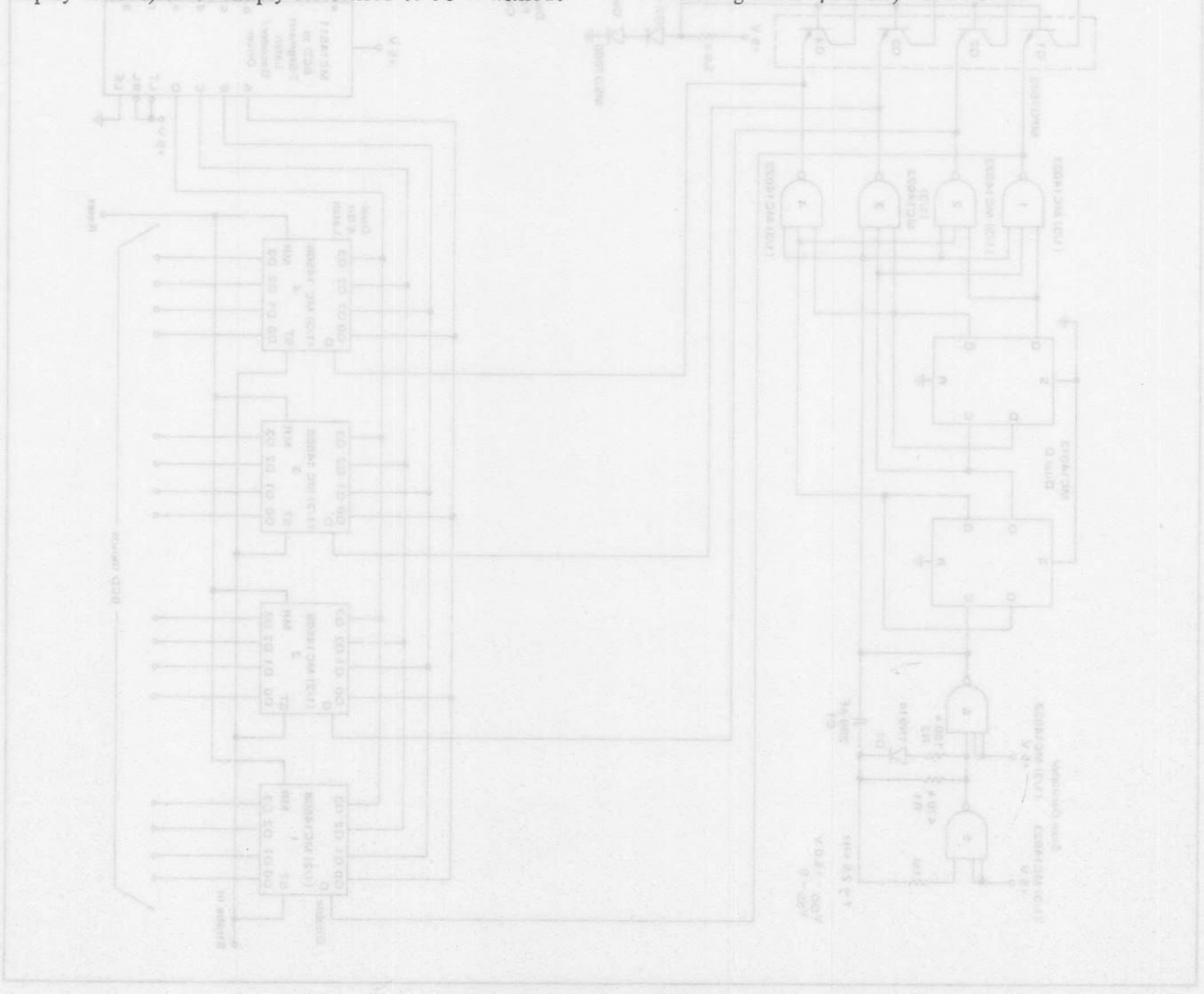
12-DIGIT CMOS GAS DISCHARGE DISPLAY

When the number of digits for a gas discharge display system is greater than the number of segment drivers, then it is generally more economical to level translate down to the cathode segments then up to the digit anodes. An example of this technique is shown in the 12-digit display system of Figure 15 where the display anodes and cathodes are reference to ground and -180 V respectively.

The positive logic CMOS address circuits are powered by -10 V (V_{DD} = 0, V_{SS} = -10 V) with the MC14558 decoder outputs capacitor coupled to the MC3491 Segment Drivers and the scan circuit directly coupled to the MC3490P Anode Drivers. Thus, only eight capacitors (seven segments, one decimal point) are required relative to 12 if the strobed digit drivers were ac coupled. Additionally, the MC3491 has input clamp diodes allowing for dc restoration of the segment address pulse. This high voltage driver (80 V) also features programmable segment current by the selection of a single external resistor.

The MC3490P Anode Drivers have a minimum breakdown voltage specification of 50 V that is set by an internal zener diode string. These zeners allow the off drivers (and display anodes) to be simply referenced to 50 V without the need of isolation resistors, as described in the previous gas discharge display examples. The anode drivers are commanded by the postiive going output of the digit scan circuit. (If the scan circuit output were negative going, then the low logic level input MC3494 Anode Driver should be used). Digit scanning for this example is derived from two cascaded MC14022 Octal Counter/Dividers. The 12 sequenced output pulses are achieved by resetting the counters with the second counter Q7 output. In addition to driving the two MC3490s, the counter output should also control the system multiplexer (not shown) to properly synchronize the entire display system.

The MC14558 BCD-to-7 Segment Decoder has an enable input which readily provides for display cathode blanking. For the illustrated display, the cathode drivers should be turned off prior to anode switching and should be maintained off for some period after the next anode is strobed. This cathode blanking overlap is derived by trailing edge time delaying the Gate 1 output of the non-symmetric 4 kHz scan oscillator with the integrator network and inverter Gate 3. With the component values shown, an approximate 60 μs blanking gate (35 μs prior to anode switching and 25 μs after) was achieved.



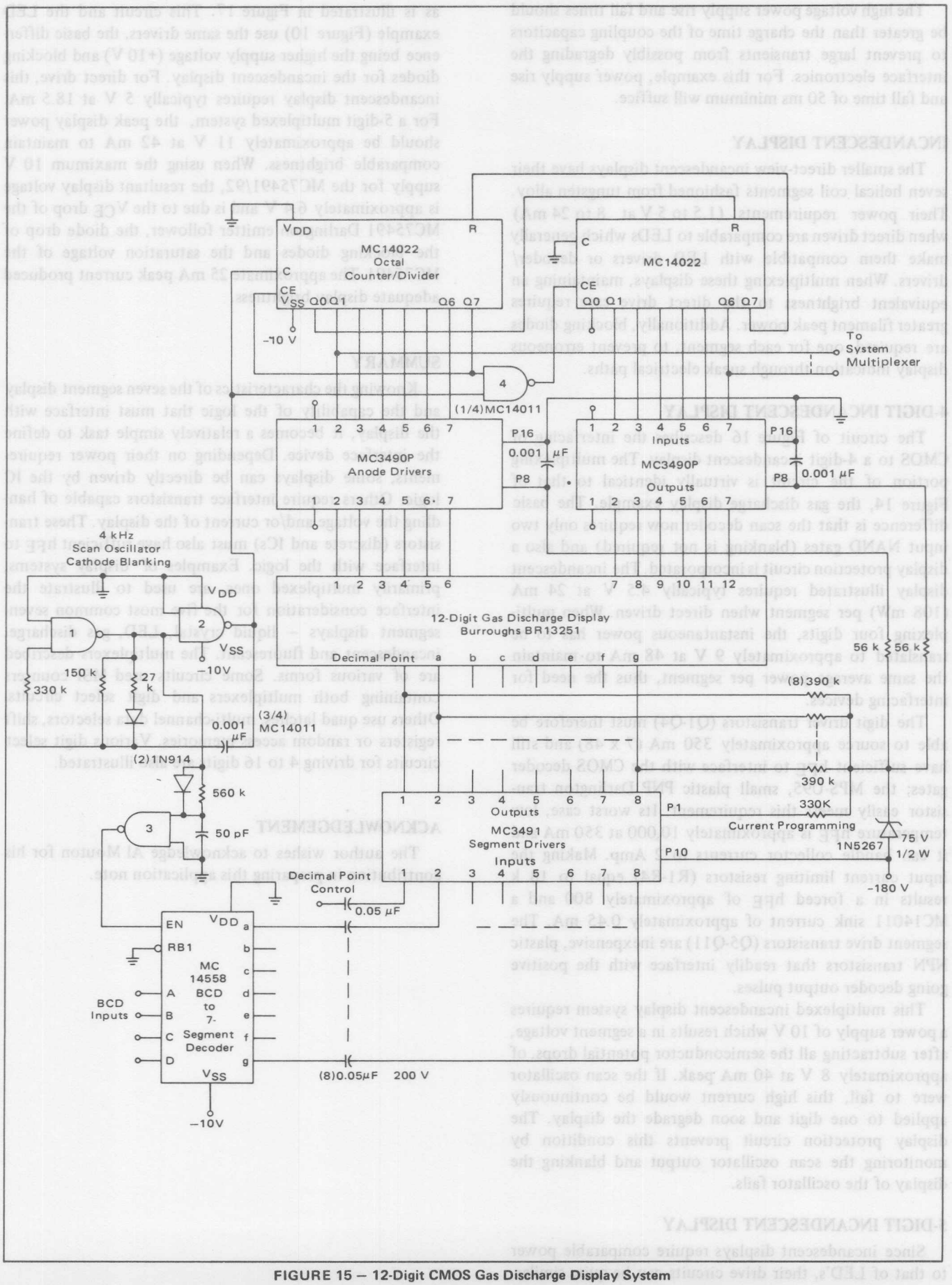


FIGURE 15 – 12-Digit CMOS Gas Discharge Display System

The high voltage power supply rise and fall times should be greater than the charge time of the coupling capacitors to prevent large transients from possibly degrading the interface electronics. For this example, power supply rise and fall time of 50 ms minimum will suffice.

INCANDESCENT DISPLAY

The smaller direct-view incandescent displays have their seven helical coil segments fashioned from tungsten alloy. Their power requirements (1.5 to 5 V at 8 to 24 mA) when direct driven are comparable to LEDs which generally make them compatible with LED drivers or decoder/drivers. When multiplexing these displays, maintaining an equivalent brightness to the direct drive case requires greater filament peak power. Additionally, blocking diodes are required, one for each segment, to prevent erroneous display indication through sneak electrical paths.

4-DIGIT INCANDESCENT DISPLAY

The circuit of Figure 16 describes the interfacing of CMOS to a 4-digit incandescent display. The multiplexing portion of the circuit is virtually identical to that of Figure 14, the gas discharge display example. The basic difference is that the scan decoder now requires only two input NAND gates (blanking is not required) and also a display protection circuit is incorporated. The incandescent display illustrated requires typically 4.5 V at 24 mA (108 mW) per segment when direct driven. When multiplexing four digits, the instantaneous power has to be translated to approximately 9 V at 48 mA to maintain the same average power per segment, thus the need for interfacing devices.

The digit driver transistors (Q1-Q4) must therefore be able to source approximately 350 mA (7 x 48) and still have sufficient h_{FE} to interface with the CMOS decoder gates; the MPS-U95, small plastic PNP Darlington transistor easily meets this requirement. Its worst case, low temperature h_{FE} is approximately 10,000 at 350 mA and it can handle collector currents to 2 Amp. Making the input current limiting resistors (R1-R4) equal to 18 k results in a forced h_{FE} of approximately 800 and a MC14011 sink current of approximately 0.45 mA. The segment drive transistors (Q5-Q11) are inexpensive, plastic NPN transistors that readily interface with the positive going decoder output pulses.

This multiplexed incandescent display system requires a power supply of 10 V which results in a segment voltage, after subtracting all the semiconductor potential drops, of approximately 8 V at 40 mA peak. If the scan oscillator were to fail, this high current would be continuously applied to one digit and soon degrade the display. The display protection circuit prevents this condition by monitoring the scan oscillator output and blanking the display of the oscillator fails.

5-DIGIT INCANDESCENT DISPLAY

Since incandescent displays require comparable power to that of LED's, their drive circuits can be quite similar, as is illustrated in Figure 17. This circuit and the LED example (Figure 10) use the same drivers, the basic difference being the higher supply voltage (+10 V) and blocking diodes for the incandescent display. For direct drive, this incandescent display requires typically 5 V at 18.5 mA. For a 5-digit multiplexed system, the peak display power should be approximately 11 V at 42 mA to maintain comparable brightness. When using the maximum 10 V supply for the MC75491/92, the resultant display voltage is approximately 6.4 V and is due to the V_{CE} drop of the MC75491 Darlington emitter follower, the diode drop of the blocking diodes and the saturation voltage of the MC75491. The approximate 25 mA peak current produced adequate display brightness.

SUMMARY

Knowing the characteristics of the seven segment display and the capability of the logic that must interface with the display, it becomes a relatively simple task to define the interface device. Depending on their power requirements, some displays can be directly driven by the IC logic. Others require interface transistors capable of handling the voltage and/or current of the display. These transistors (discrete and ICs) must also have sufficient h_{FE} to interface with the logic. Examples of display systems, primarily multiplexed ones, are used to illustrate the interface consideration for the five most common seven-segment displays – liquid crystal, LED, gas discharge, incandescent and fluorescent. The multiplexers described are of various forms. Some circuits used MSI counters containing both multiplexers and digit select circuits. Others use quad latches, multi-channel data selectors, shift registers or random access memories. Various digit select circuits for driving 4 to 16 digits are also illustrated.

ACKNOWLEDGEMENT

The author wishes to acknowledge Al Mouton for his contribution in preparing this application note.

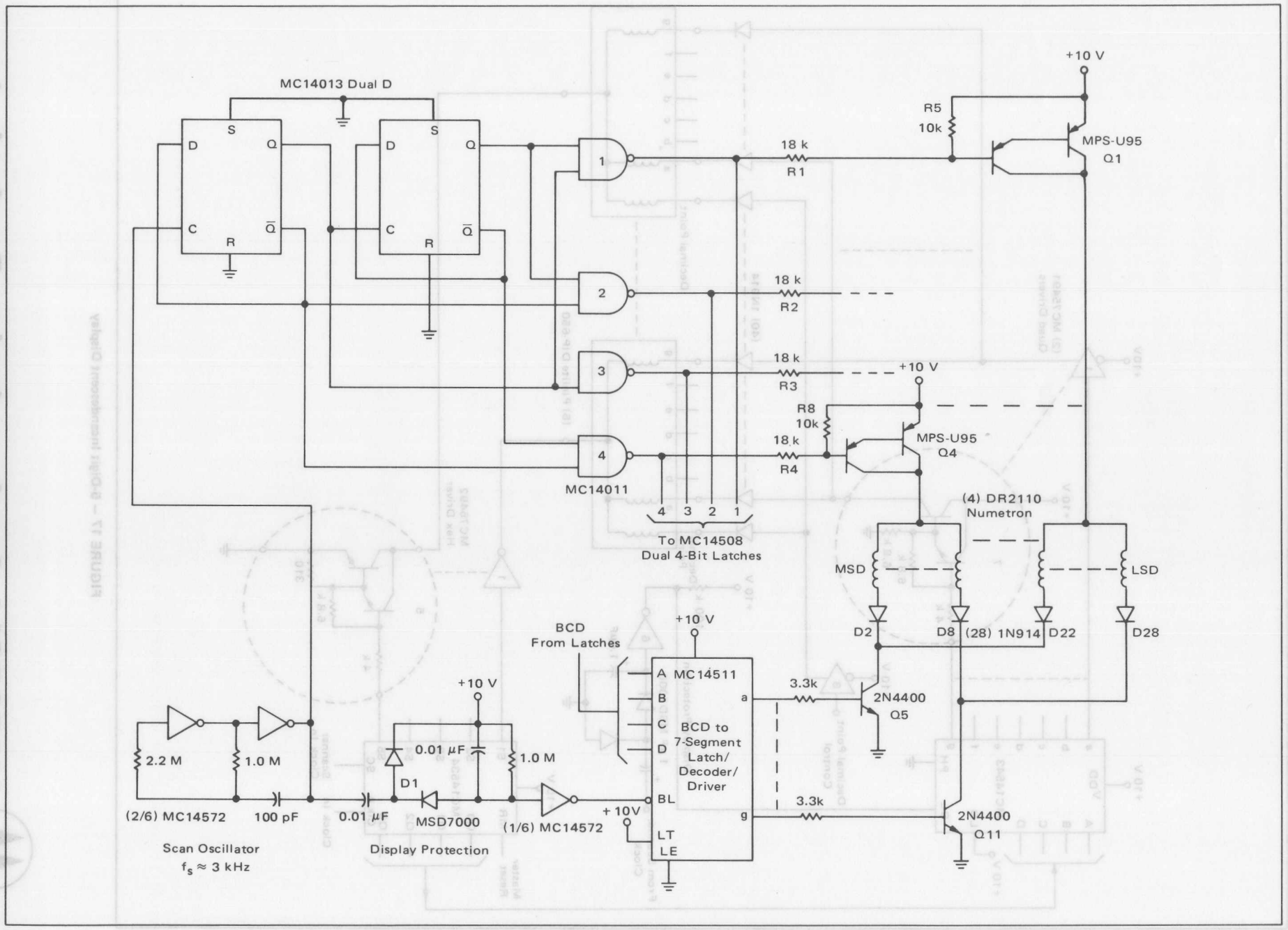


FIGURE 16 – Interfacing CMOS to 4-Digit Incandescent Display

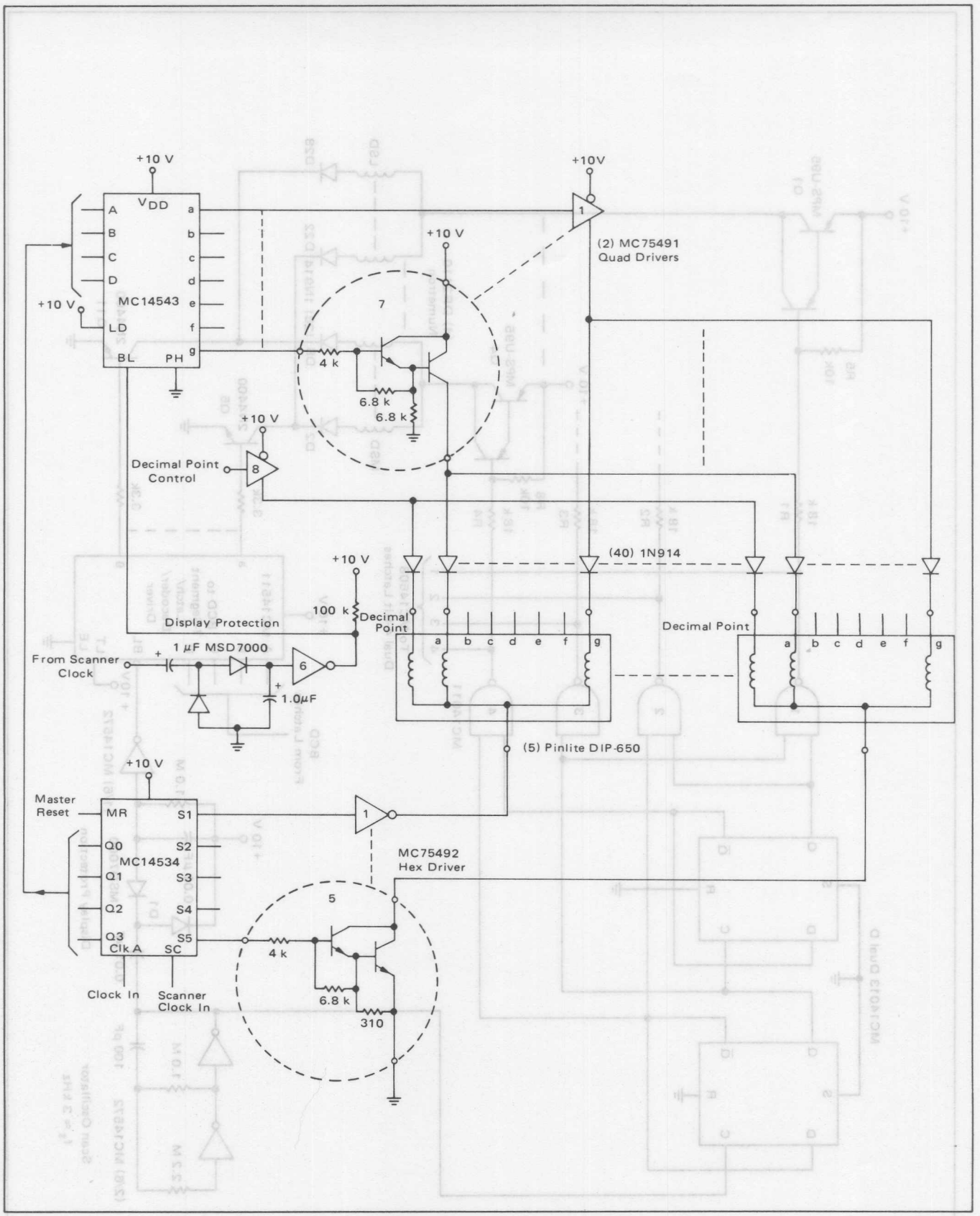


FIGURE 17 – 5-Digit Incandescent Display