AN-733
Application Note

A ROM-DIGITAL APPROACH TO PWM-TYPE SPEED CONTROL OF AC MOTORS

Prepared by:
Thomas Mazur
Technical Information Center

This application note describes a PWM (Pulse Width Modulation) scheme for motor speed control. A state of the art CMOS logic circuit uses a ROM (Read Only Memory) to generate sineweighted pulse trains. The memory organization is such that four pulse trains, with fixed-phase differences between their modulation envelopes, are produced to control single, two or three phase motors. Opto-electronic couplers are used to isolate logic and power stages. The availability of four-phase shifted drive signals and the isolation afforded by optical coupling provides a means of using a single logic stage to control multiple and mixed-type motor installations.

MOTOROLA Semiconductor Products Inc.

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INTRODUCTION

The utilization of ac machines for variable-speed motor drives is increasing. The relatively short lifetimes of the brushes in a dc machine, and their associated maintenance requirements, makes the ac motor an attractive alternative for applications ranging from small machine control to large traction drive schemes.

The speed of an ac induction motor can be controlled by varying the voltage or frequency of the motor's power source. The variable voltage approach is generally used to control shaded pole, permanent split capacitor, wound rotor or universal motors. Variable frequency drives are most often used to power polyphase machines of integral horsepower rating.

Two methods of producing variable-frequency drives include cycloconverters and pulse width modulators (PWM). The cycloconverter synthesizes lower frequency ac by combining the three phases of standard 50/60 Hz power in certain patterns. The PWM inverter operates from a dc source; by switching SCRs or power transistors at certain rates, sine waves of current can be approximated in the motor windings.

The PWM scheme to be described in this Note utilizes state of the art CMOS (complementary metal oxide semiconductor) logic. A stored program contained in a 256 by 4 bit CMOS ROM (Read Only Memory) generates the appropriate sine-weighted pulse trains. The memory programming is such that four pulse trains, with fixed phase differences between their modulation envelopes, are produced to control single, two or three phase ac motors. Optoelectronic couplers are used to interface logic and power stages.

Ordinarily, PWM inverters are used to drive three phase ac motors. While the majority of present day applications may require such machines, the control of single and two phase motors may also be desirable. For example, mills, lathes and other related shop machinery use single, two or three phase motors coupled to gear or pulley transmissions to effect speed control. Elimination of the transmission by means of a variable speed drive can result in a machine with fewer moving parts and lower weight.

The CMOS logic circuit to be described, in conjunction with suitable power stages, can provide variable frequency drive for single, two or three phase motors. The optical couplers, used for interfacing, have a unidirectional signal characteristic; this property minimizes transient feedback from the power stages to the logic stage. In addition, the optical coupler provides an easy means of translating the drive signals from the low voltage logic supply level to the high voltage, bidirectional power switch levels.

SYSTEM OPERATION

ROM Addressing

The control scheme is shown, in block form, in Figure 1. The MCM14524, a 1024 bit, (organized 256 by 4), mask-programmable CMOS memory is used to generate the sine-weighted PWM waveform. In this scheme, the memory outputs form four serial words each 256 bits long. Since $256 = 2^8$, an 8 bit address is required. A 12 bit binary counter, MC14040, and two MC14507 quad exclusive-OR gates form the addressing logic to generate an up-down count pattern; the address cycles from Word 0 (00000000_2) to Word 255 (11111111_2) back to Word 0, and so on. When the address is changing from Word 0 to Word 255, the average value of the ROM output B0 approximates a sine wave from 0^o to 90^o; when the address is changing from Word 255 to Word 0 the average value approximates a sine wave from 90^o to 180^o, as shown in Figure 2.

One output of a simple CMOS R-C oscillator, Clock #1, controls the counter in the address logic. A second output, Clock #2, controls data transfer within the memory. Clock #2 is a delayed version of Clock #1. The delay, of approximately 3 μs, allows the counter to settle to a new state before the data in the memory is transferred to the outputs B0 through B3. The oscillator sets the rate at which the address changes, and consequently, controls the frequency of the drive signals applied to a motor's windings. The drive signal frequency range is from 10 Hz to 100 Hz. In short, the oscillator serves as the RPM control.

ROM Data Steering

To minimize the bit capacity requirements of a memory, only quarter cycle waveform coding need be stored when the desired waveforms are periodic sine-cosine waves. The output data of the memory can then be switched, or steered, through logic gates, to form pulse trains whose composite waveforms have the desired periodicity.

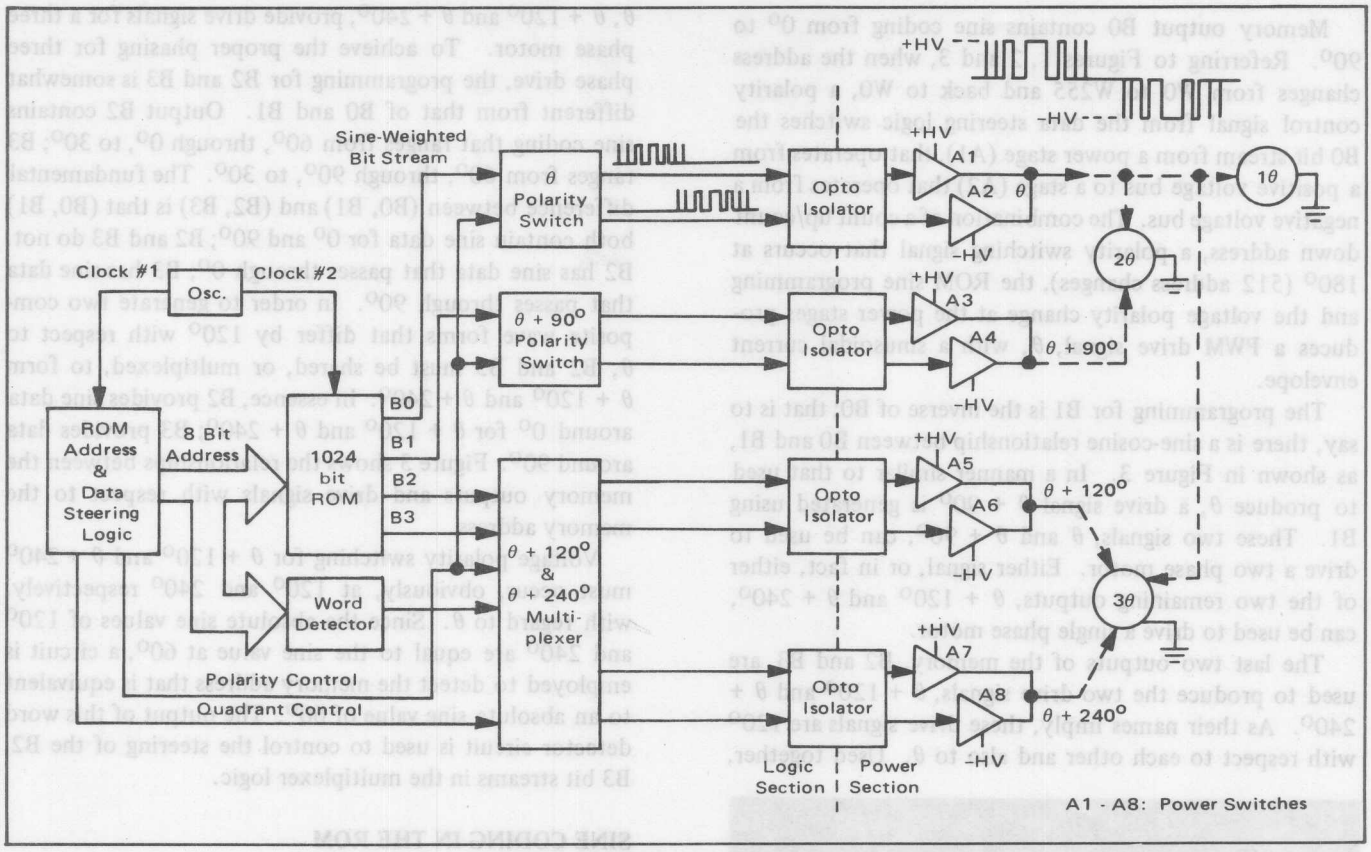


FIGURE 1 – Block Diagram

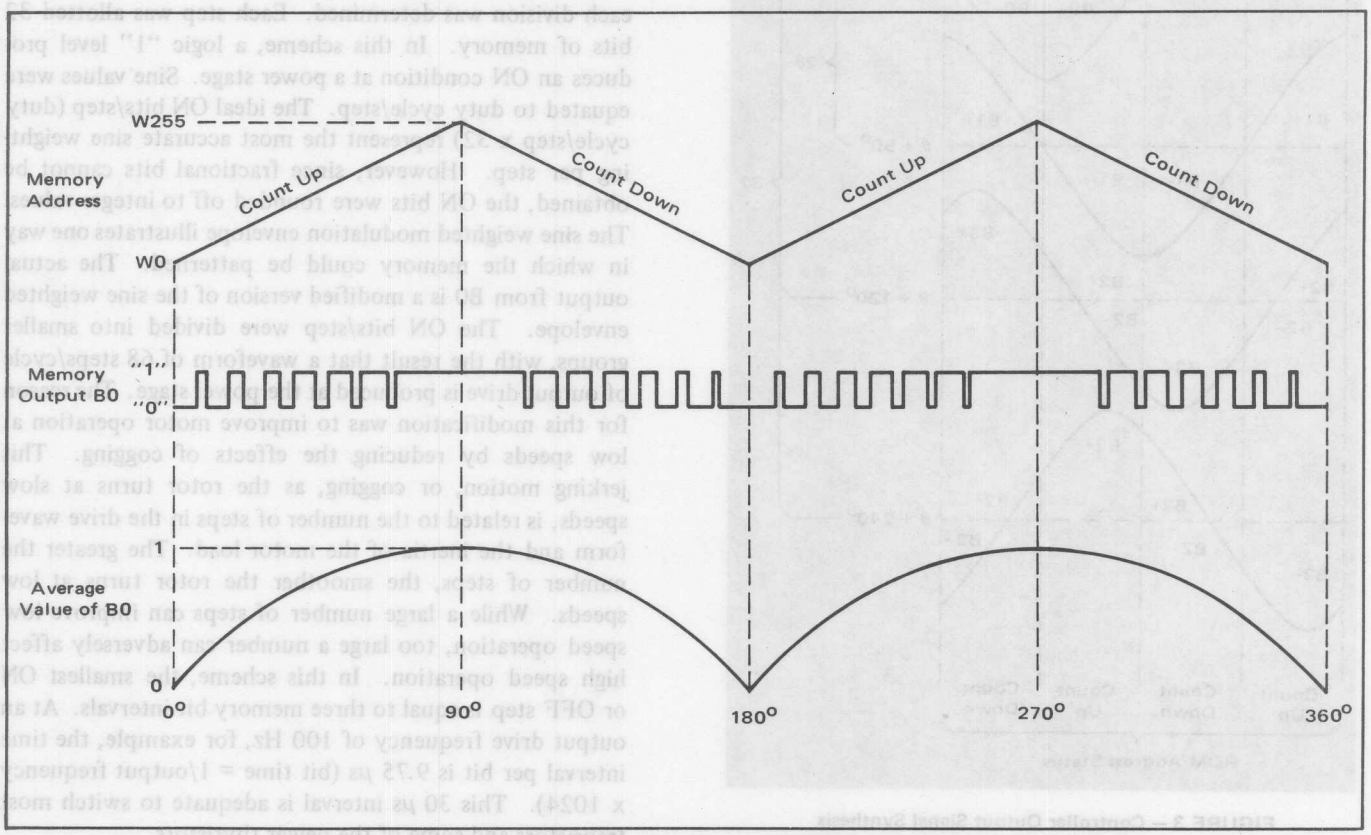


FIGURE 2 – Changes at B0 with Respect to Memory Address

Memory output B0 contains sine coding from 0^o to 90^o. Referring to Figures 1, 2 and 3, when the address changes from W0 to W255 and back to W0, a polarity control signal from the data steering logic switches the B0 bit stream from a power stage (A1), that operates from a positive voltage bus to a stage (A2) that operates from a negative voltage bus. The combination of a count up/count down address, a polarity switching signal that occurs at 180^o (512 address changes), the ROM sine programming and the voltage polarity change at the power stages produces a PWM drive signal, θ, with a sinusoidal current envelope.

The programming for B1 is the inverse of B0; that is to say, there is a sine-cosine relationship between B0 and B1, as shown in Figure 3. In a manner similar to that used to produce θ, a drive signal $\theta + 90^o$ is generated using B1. These two signals, θ and $\theta + 90^o$, can be used to drive a two phase motor. Either signal, or in fact, either of the two remaining outputs, $\theta + 120^o$ and $\theta + 240^o$, can be used to drive a single phase motor.

The last two outputs of the memory, B2 and B3, are used to produce the two drive signals, $\theta + 120^o$ and $\theta + 240^o$. As their names imply, these drive signals are 120^o with respect to each other and also to θ. Used together, θ, $\theta + 120^o$ and $\theta + 240^o$, provide drive signals for a three phase motor. To achieve the proper phasing for three phase drive, the programming for B2 and B3 is somewhat different from that of B0 and B1. Output B2 contains sine coding that ranges from 60^o, through 0^o, to 30^o; B3 ranges from 60^o, through 90^o, to 30^o. The fundamental difference between (B0, B1) and (B2, B3) is that (B0, B1) both contain sine data for 0^o and 90^o; B2 and B3 do not. B2 has sine data that passes through 0^o; B3 has sine data that passes through 90^o. In order to generate two composite wave forms that differ by 120^o with respect to θ, B2 and B3 must be shared, or multiplexed, to form $\theta + 120^o$ and $\theta + 240^o$. In essence, B2 provides sine data around 0^o for $\theta + 120^o$ and $\theta + 240^o$; B3 provides data around 90^o. Figure 3 shows the relationships between the memory outputs and drive signals with respect to the memory address.

Voltage polarity switching for $\theta + 120^o$ and $\theta + 240^o$ must occur, obviously, at 120^o and 240^o respectively, with regard to θ. Since the absolute sine values of 120^o and 240^o are equal to the sine value at 60^o, a circuit is employed to detect the memory address that is equivalent to an absolute sine value of 60^o. The output of this word detector circuit is used to control the steering of the B2, B3 bit streams in the multiplexer logic.

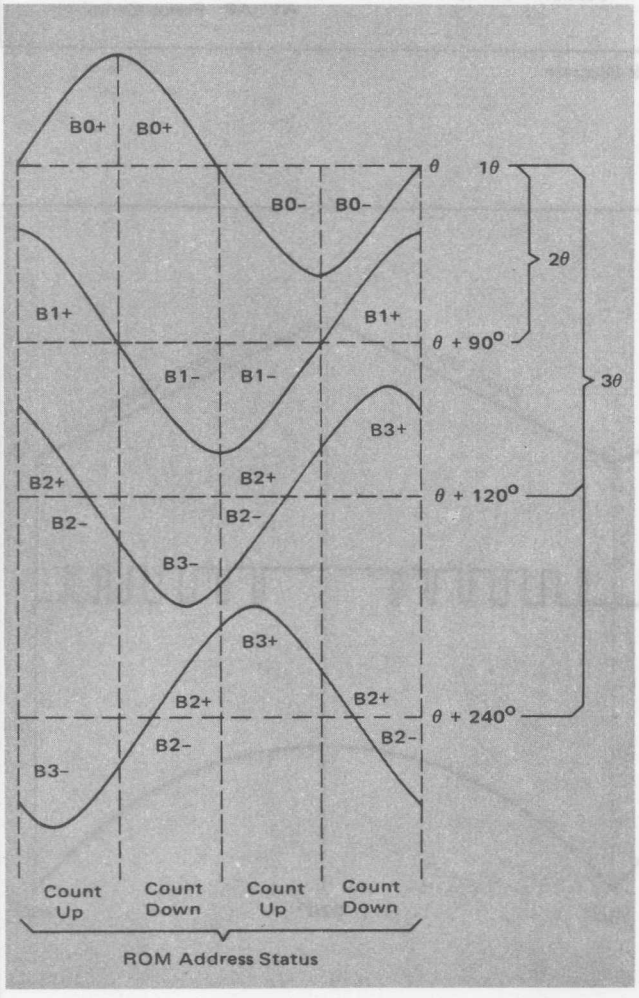


FIGURE 3 – Controller Output Signal Synthesis Idealized Load Current Waveforms

SINE CODING IN THE ROM

Each memory output represents a 90^o segment of a sine modulated envelope. Figure 4 describes the coding for ROM output B0. The first quadrant of a sine wave was divided into eight equal angle steps and the sine value at each division was determined. Each step was allotted 32 bits of memory. In this scheme, a logic "1" level produces an ON condition at a power stage. Sine values were equated to duty cycle/step. The ideal ON bits/step (duty cycle/step x 32) represent the most accurate sine weighting per step. However, since fractional bits cannot be obtained, the ON bits were rounded off to integer values. The sine weighted modulation envelope illustrates one way in which the memory could be patterned. The actual output from B0 is a modified version of the sine weighted envelope. The ON bits/step were divided into smaller groups, with the result that a waveform of 68 steps/cycle of output drive is produced at the power stage. The reason for this modification was to improve motor operation at low speeds by reducing the effects of cogging. This jerking motion, or cogging, as the rotor turns at slow speeds, is related to the number of steps in the drive waveform and the inertia of the motor load. The greater the number of steps, the smoother the rotor turns at low speeds. While a large number of steps can improve low speed operation, too large a number can adversely affect high speed operation. In this scheme, the smallest ON or OFF step is equal to three memory bit intervals. At an output drive frequency of 100 Hz, for example, the time interval per bit is 9.75 μs (bit time = 1/output frequency x 1024). This 30 μs interval is adequate to switch most transistors and some of the newer thyristors.

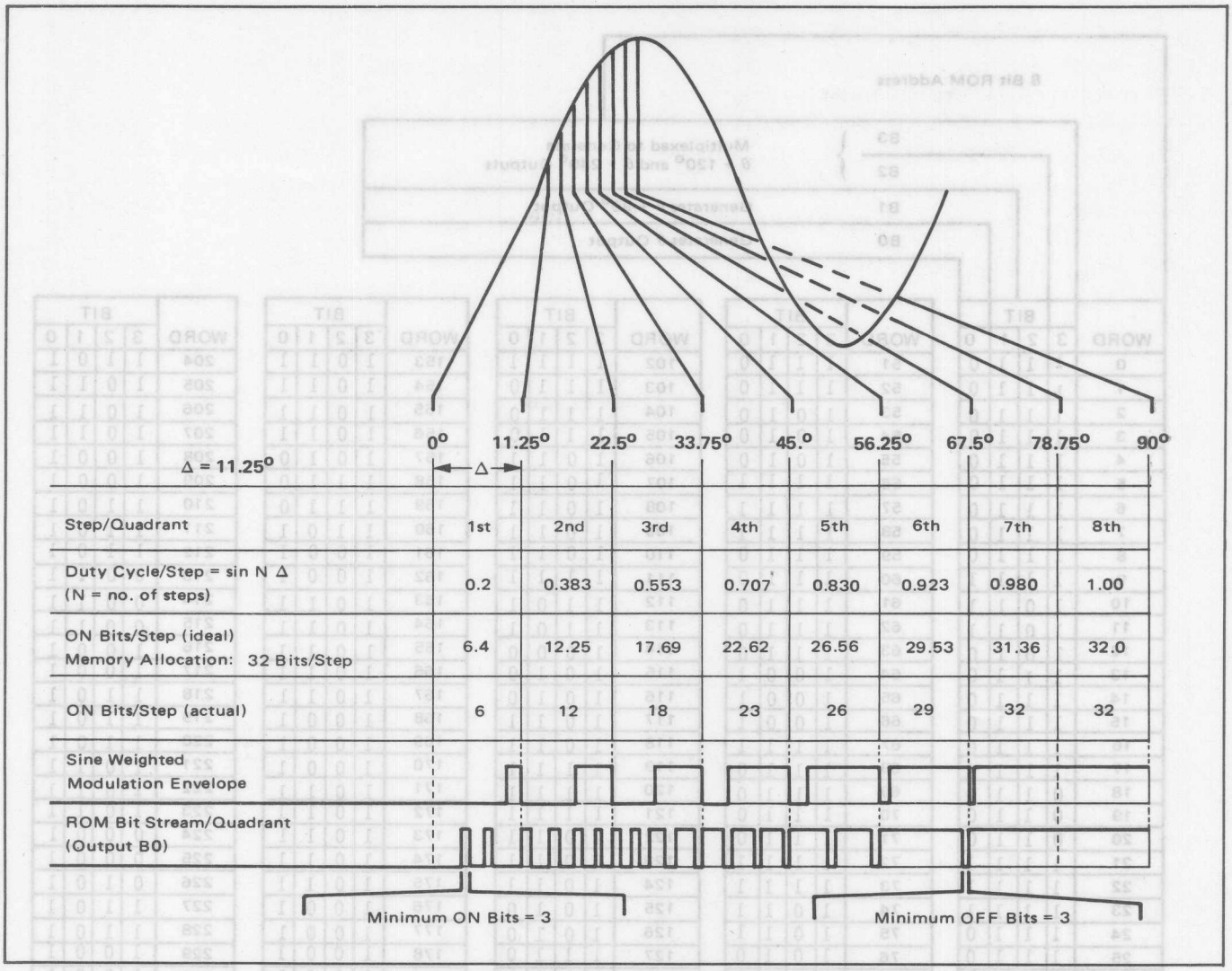


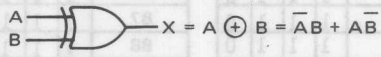
FIGURE 4 – ROM Coding

Memory outputs B1, B2 and B3 have the same ON/OFF bit patterns as B0; they differ only in the way their sine coding is stored with respect to the pattern of B0. Figure 5 shows the program stored in the MCM14524 memory. Examination of the program will show that the pattern of B1, when going from Word 255 to Word 0, is the same as the pattern of B0, when moving from Word 0 to Word 255. Also, the pattern of B2, when starting from Word 170 and going in either direction, is the same as the pattern of B0, when starting from Word 0. Lastly, the pattern of B3, with Word 170 as the starting point, is the same as the pattern of B1, when starting at Word 0.

ROM ADDRESSING AND CONSTRUCTION OF θ AND $\theta + 90^{o}$ OUTPUTS

Refer to Figures 6, 7 and 8. The ROM address inputs A0 through A7 are initiated in the first 8 outputs of the MC14040 12-bit binary up counter, U6. Assume an initial state of logic zero ("0") at all the counter outputs. Clock #1 advances the counter outputs Q1 through Q8 from 00000000_2 to 11111111_2 in 256 clock pulses. At the 257th pulse, Q9 returns to "1". As mentioned earlier in this text, the memory requires an up-down count pattern at the address inputs. This is achieved by combining the outputs of Q1 through Q8 with the output of Q9 in MC14507 Exclusive-OR gates U7 through U14.

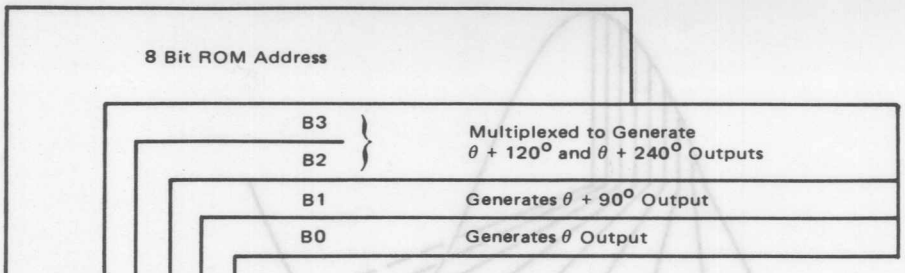
Since the output of the Exclusive-OR is



then a truth table for Q9 ⊕ (Q1 . . . , Q8) would be

(Q1 . . . , Q8)	Q9 = 0	Q9 = 1
0	0	1
1	1	0

Thus it can be seen that when Q9 is at "0", the binary value of Q1 through Q8 remains the same, but when Q9 is "1", the complement of Q1 through Q8 is present at the output of the gates. In the first quadrant, as shown in Figure 2, the sine value of B0 increases from "0" to "1". In the second quadrant, as the address counts down, B0 decreases back to a sine value of "0". This provides one alternation of output θ, via buffer U32. At the beginning



WORD	BIT 3	2	1	0
0	1	1	1	0
1	1	1	1	0
2	1	1	1	0
3	1	1	1	0
4	1	1	1	0
5	1	1	1	0
6	1	1	1	0
7	1	1	1	0
8	1	1	1	0
9	1	1	1	1
10	1	0	1	1
11	1	0	1	1
12	1	0	1	0
13	1	1	1	0
14	1	1	1	0
15	1	1	1	0
16	1	1	1	0
17	1	1	1	0
18	0	1	1	0
19	0	1	1	0
20	0	1	1	0
21	1	1	1	1
22	1	1	1	1
23	1	1	1	1
24	1	1	1	0
25	1	1	1	0
26	1	0	1	0
27	1	0	1	0
28	1	0	1	0
29	1	1	1	0
30	1	1	1	0
31	1	1	1	0
32	1	1	1	1
33	1	1	1	1
34	1	1	1	1
35	1	1	1	0
36	1	1	1	0
37	1	1	1	0
38	1	1	1	0
39	1	1	1	0
40	1	1	1	1
41	1	1	1	1
42	1	0	1	1
43	1	0	1	0
44	1	0	1	0
45	1	1	1	0
46	1	1	1	0
47	1	1	1	0
48	1	1	1	1
49	1	1	1	1
50	1	1	1	1

WORD	BIT 3	2	1	0
51	1	1	1	0
52	1	1	1	0
53	1	0	1	0
54	1	0	1	0
55	1	0	1	0
56	1	1	1	1
57	1	1	1	1
58	1	1	1	1
59	1	1	1	0
60	1	1	1	0
61	1	1	1	0
62	1	1	1	0
63	1	1	1	0
64	1	0	0	1
65	1	0	0	1
66	1	0	0	1
67	1	1	1	1
68	1	1	1	0
69	1	1	1	0
70	1	1	1	0
71	1	1	1	0
72	1	1	1	1
73	1	1	1	1
74	1	0	1	1
75	1	0	1	1
76	1	0	1	0
77	1	1	1	0
78	1	1	1	0
79	1	1	1	0
80	1	1	1	1
81	1	1	1	1
82	1	0	1	1
83	1	0	1	1
84	1	0	1	1
85	1	1	1	0
86	1	1	1	0
87	1	1	1	0
88	1	1	1	1
89	1	1	1	1
90	1	0	1	1
91	1	0	1	1
92	1	0	1	1
93	1	0	1	0
94	1	1	1	0
95	1	1	1	0
96	1	1	0	1
97	1	1	0	1
98	1	0	0	1
99	1	0	1	1
100	1	0	1	1
101	1	0	1	1

WORD	BIT 3	2	1	0
102	1	1	1	1
103	1	1	1	0
104	1	1	1	0
105	1	1	1	0
106	1	0	1	1
107	1	0	1	1
108	1	0	1	1
109	1	0	1	1
110	1	0	1	1
111	1	1	1	1
112	1	1	0	1
113	1	1	0	1
114	1	0	0	0
115	1	0	1	0
116	1	0	1	0
117	1	0	1	1
118	1	0	1	1
119	1	1	1	1
120	1	1	1	1
121	1	1	1	1
122	1	0	1	1
123	1	0	1	1
124	1	0	1	1
125	1	0	1	0
126	1	0	1	0
127	1	1	1	0
128	1	1	0	1
129	1	1	0	1
130	1	0	0	1
131	1	0	1	1
132	1	0	1	1
133	1	0	1	1
134	1	0	1	1
135	1	1	1	1
136	1	1	1	1
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140	1	0	0	1
141	1	0	0	0
142	1	0	1	0
143	1	0	1	0
144	1	0	1	1
145	1	0	1	1
146	1	1	1	1
147	1	1	1	1
148	0	1	1	1
149	0	0	1	1
150	0	0	0	1
151	0	0	0	1
152	1	0	0	1

WORD	BIT 3	2	1	0
153	1	0	1	1
154	1	0	1	1
155	1	0	1	1
156	1	0	1	1
157	1	0	1	0
158	1	1	1	0
159	1	1	1	0
160	1	1	0	1
161	1	0	0	1
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172	1	0	1	1
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181	0	1	1	1
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185	1	0	0	1
186	1	0	0	1
187	1	0	0	1
188	1	0	1	1
189	1	0	1	0
190	1	0	1	0
191	1	1	1	0
192	1	1	0	1
193	1	1	0	1
194	1	0	0	1
195	1	0	0	1
196	1	0	0	1
197	0	0	1	1
198	0	0	1	1
199	0	0	1	1
200	1	0	0	1
201	1	0	0	1
202	1	1	0	1
203	1	1	0	1

WORD	BIT 3	2	1	0
204	1	1	0	1
205	1	0	1	1
206	1	0	1	1
207	1	0	1	1
208	1	0	0	1
209	1	0	0	1
210	1	1	0	1
211	1	1	0	1
212	1	1	0	1
213	0	0	1	1
214	0	0	1	1
215	0	0	1	1
216	1	0	0	1
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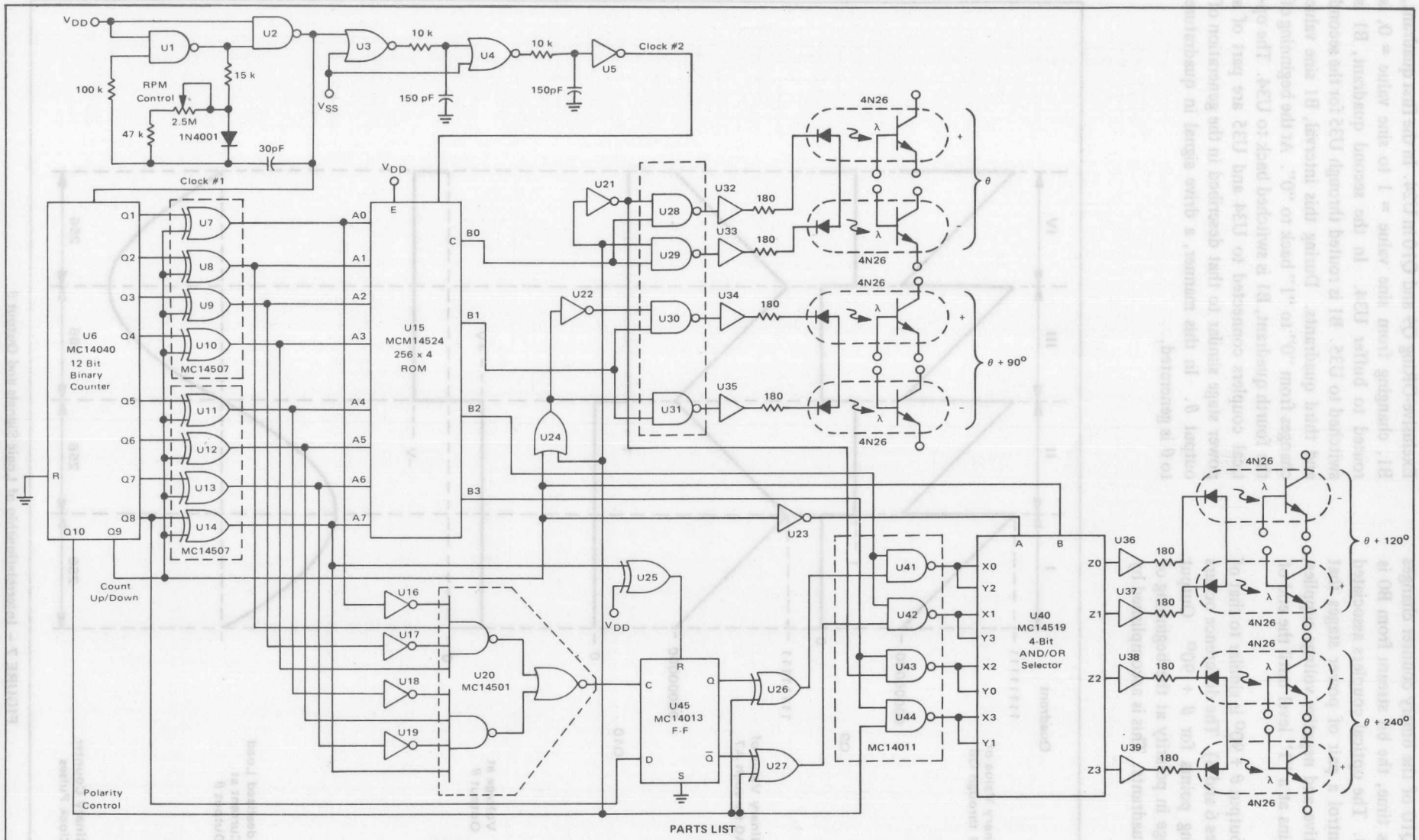
246	0	1	1	1
247	0	0	0	1
248	1	0	0	1
249	1	0	0	1
250	1	1	0	1
251	1	1	0	1
252	1	1	0	1
253	0	1	0	1
254	0	1	0	1
255	0	0	0	1

FIGURE 5 – ROM Programming for 256 x 4 Bit Organization



PARTS LIST

Motorola Part No.	Description	Circuit Identifiers
MC14572	Hex Gate (1 2-Input NAND, 1 2-Input NOR, 4 Inverters)	U1, 3, 16, 17, 18, 19
MC14572	Hex Gate	U2, 4, 5, 21, 22, 23
MC14040	12-Bit Binary Counter	U6
MC14507	Quad Exclusive OR Gate	U7, 8, 9, 10
MC14507	Quad Exclusive OR Gate	U11, 12, 13, 14
MCM14524	1024-Bit ROM	U15
MC14501	8-Input AND Gate	U20
MC14507	Quad Exclusive OR Gate	U24, 25, 26, 27
MC14011	Quad 2-Input NAND Gate	U28, 29, 30, 31
MC14050	Hex Non-Inverting Buffer	U32, 33, 34, 35, 36, 37
MC14050	Hex Non-Inverting Buffer	U38, 39
MC14519	4-Bit AND/OR Selector	U40
MC14011	Quad 2-Input NAND Gate	U41, 42, 43, 44
MC14013	Dual Type D Flip-Flop	U45

FIGURE 6 – Logic Diagram

of the third quadrant, Q10 of the binary counter changes to a "1" level. At this time, the bit stream from B0 is switched to buffer U33. The optical couplers associated with U32 and U33 control a pair of power stages that connect a load to positive and negative voltage supplies, respectively. Q10 remains at a "1" level until the end of the fourth quadrant.

The construction of output $\theta + 90^{o}$ is similar to that of output θ (refer to Figures 6 and 8). The difference occurs in the polarity switching points for $\theta + 90^{o}$ Output $\theta + 90^{o}$ requires a change in polarity at the beginning of the second and fourth quadrants. This is accomplished by Exclusive-ORing Q9 and Q10 in U24. In the first quadrant, B1, changing from sine value = 1 to sine value = 0, is routed to buffer U34. In the second quadrant, B1 is switched to U35. B1 is routed through U35 for the second and third quadrants. During this interval, B1 sine value changes from "0" to "1" back to "0". At the beginning of the fourth quadrant, B1 is switched back to U34. The optical couplers connected to U34 and U35 are part of a power stage similar to that described in the generation of output θ. In this manner, a drive signal in quadrature to θ is generated.

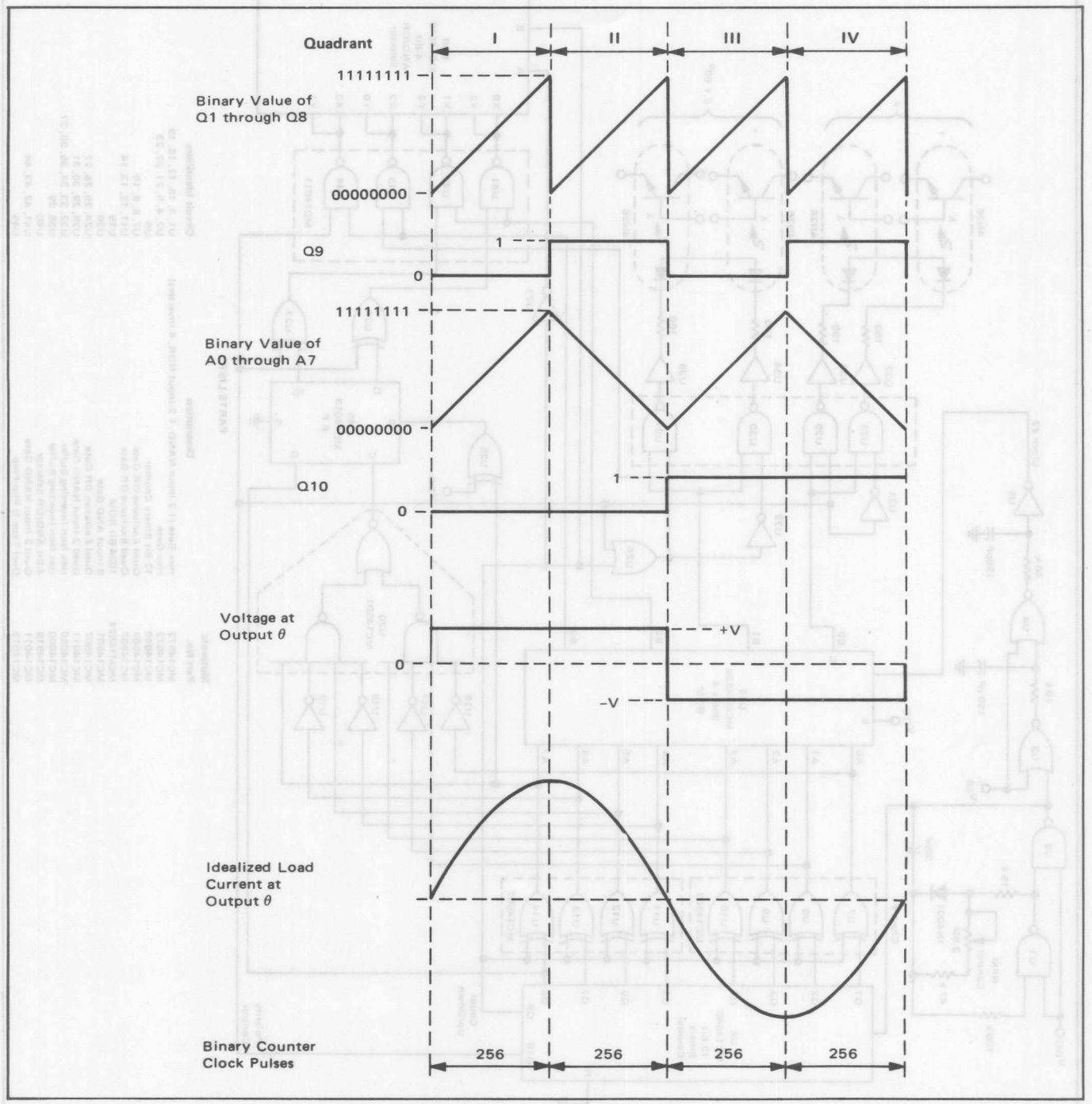


FIGURE 7 – Interrelationship of Logic Signals and Output θ

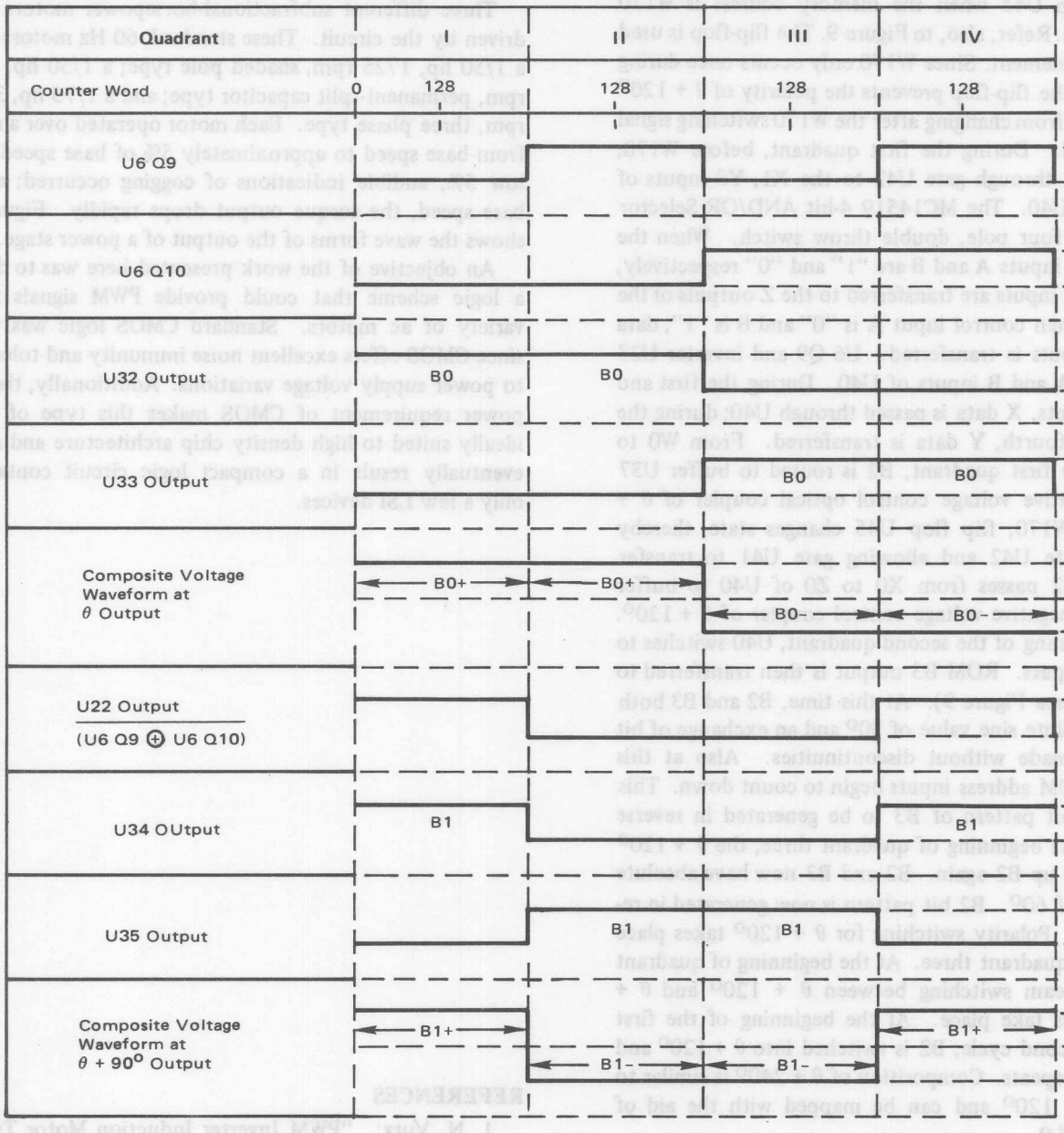


FIGURE 8 – Generation of θ and $\theta + 90^{o}$ Outputs

CONSTRUCTION OF $\theta + 120^{o}$ AND $\theta + 240^{o}$ OUTPUTS

Unlike the θ and $\theta + 90^{o}$ outputs, the $\theta + 120^{o}$ and $\theta + 240^{o}$ outputs require bit stream multiplexing of B2 and B3. As described previously, the "end" point values of B2 and B3 are equivalent to the sines of 60^{o} and 30^{o}. To construct a drive waveform that is displaced 120^{o} from θ, an absolute sine value of 60^{o} is required. When θ has changed from 0^{o} to 90^{o}, a waveform displaced 120^{o} must change to a sine value equivalent to 210^{o}. The absolute sine value of 210^{o} is 30^{o}. For a waveform displaced 240^{o}, the same absolute sine values are required. Both B2 and B3 meet these requirements; however, since $\theta + 120^{o}$ requires a lead angle of 120^{o}, B2 is chosen. Consider that, when θ reaches 60^{o}, $\theta + 120^{o}$ must be at "0" sine value. B2 has a "0" sine value at that time. With output θ as a reference, as shown in Figure 3, output $\theta + 120^{o}$ will be generated, initially, by B2. Output $\theta + 240^{o}$ will begin with B3.

Polarity switching of θ and $\theta + 90^{o}$ occurs every 90^{o} at address W0. Polarity switching of $\theta + 120^{o}$ must occur at 60^{o} and 240^{o}, with respect to θ. In the same regard, switching of $\theta + 240^{o}$ must occur at 120^{o} and 300^{o}. These switching points have absolute sine values equal to 60^{o}.

A switching signal that occurs at 60^{o}, 120^{o}, 240^{o} and 300^{o} can be obtained from the ROM address pattern. Word 170 is equivalent to an angle of 59.75^{o}. This word is used to switch the polarity of $\theta + 120^{o}$ and $\theta + 240^{o}$. A word detector, as shown on Figure 6, consisting of gates

U16 through U20, provides a clock pulse for the D type flip-flop U45 when the memory address is W170 (10101010_2). Refer, also, to Figure 9. The flip-flop is used as a storage element. Since W170 only occurs once during a quadrant, the flip-flop prevents the polarity of $\theta + 120^o$ and $\theta + 240^o$ from changing after the W170 switching signal has occurred. During the first quadrant, before W170, B2 is routed through gate U42 to the X1, Y3 inputs of multiplexer U40. The MC14519 4-bit AND/OR Selector is used as a four pole, double throw switch. When the U40 control inputs A and B are "1" and "0" respectively, data at the X inputs are transferred to the Z outputs of the Selector. When control input A is "0" and B is "1", data at the Y inputs is transferred. U6 Q9 and inverter U23 control the A and B inputs of U40. During the first and third quadrants, X data is passed through U40; during the second and fourth, Y data is transferred. From W0 to W170 of the first quadrant, B2 is routed to buffer U37 and the positive voltage control optical coupler of $\theta + 120^o$. At W170, flip flop U45 changes state, thereby inhibiting gate U42 and allowing gate U41 to transfer B2 data. B2 passes from X0 to Z0 of U40 to buffer U36 to the negative voltage control coupler of $\theta + 120^o$. At the beginning of the second quadrant, U40 switches to its Y data inputs. ROM B3 output is then transferred to buffer U36 (see Figure 9). At this time, B2 and B3 both have an absolute sine value of 30^o and an exchange of bit patterns is made without discontinuities. Also at this time, the ROM address inputs begin to count down. This causes the bit pattern of B3 to be generated in reverse order. At the beginning of quadrant three, the $\theta + 120^o$ output picks up B2 again. B2 and B3 now have absolute sine values of 60^o. B2 bit pattern is now generated in reverse order. Polarity switching for $\theta + 120^o$ takes place at W170 of quadrant three. At the beginning of quadrant four, bit stream switching between $\theta + 120^o$ and $\theta + 240^o$ outputs take place. At the beginning of the first quadrant, second cycle, B2 is switched into $\theta + 120^o$ and the process repeats. Composition of $\theta + 240^o$ is similar to that of $\theta + 120^o$ and can be mapped with the aid of Figures 6 and 9.

OUTPUT POWER STAGES

A transistor power stage is shown in Figure 10. The voltage ratings of the devices make this quasi-complementary configuration suitable for transformerless, 110 Vac line operation. The 4N26 optical couplers have an isolation rating of 1500 V; this allows the power stages to float 1500 V above the logic, should that be necessary. By increasing the drive capability of the logic outputs, by means of emitter followers, etc, the LED's (Light Emitting Diodes) of many couplers can be paralleled at each output. In this manner, extra power stages could be added in different configurations to drive a variety of motors simultaneously.

CONCLUSION

Three different subfractional-horsepower motors were driven by the circuit. These standard, 60 Hz motors were a 1/50 hp, 1725 rpm, shaded pole type; a 1/50 hp, 1725 rpm, permanent-split capacitor type; and a 1/75 hp, 3,300 rpm, three phase type. Each motor operated over a range from base speed to approximately 5% of base speed. Below 5%, audible indications of cogging occurred; above base speed, the torque output drops rapidly. Figure 11 shows the wave forms of the output of a power stage.

An objective of the work presented here was to devise a logic scheme that could provide PWM signals for a variety of ac motors. Standard CMOS logic was used, since CMOS offers excellent noise immunity and tolerance to power supply voltage variations. Additionally, the low power requirement of CMOS makes this type of logic ideally suited to high density chip architecture and could eventually result in a compact logic circuit containing only a few LSI devices.

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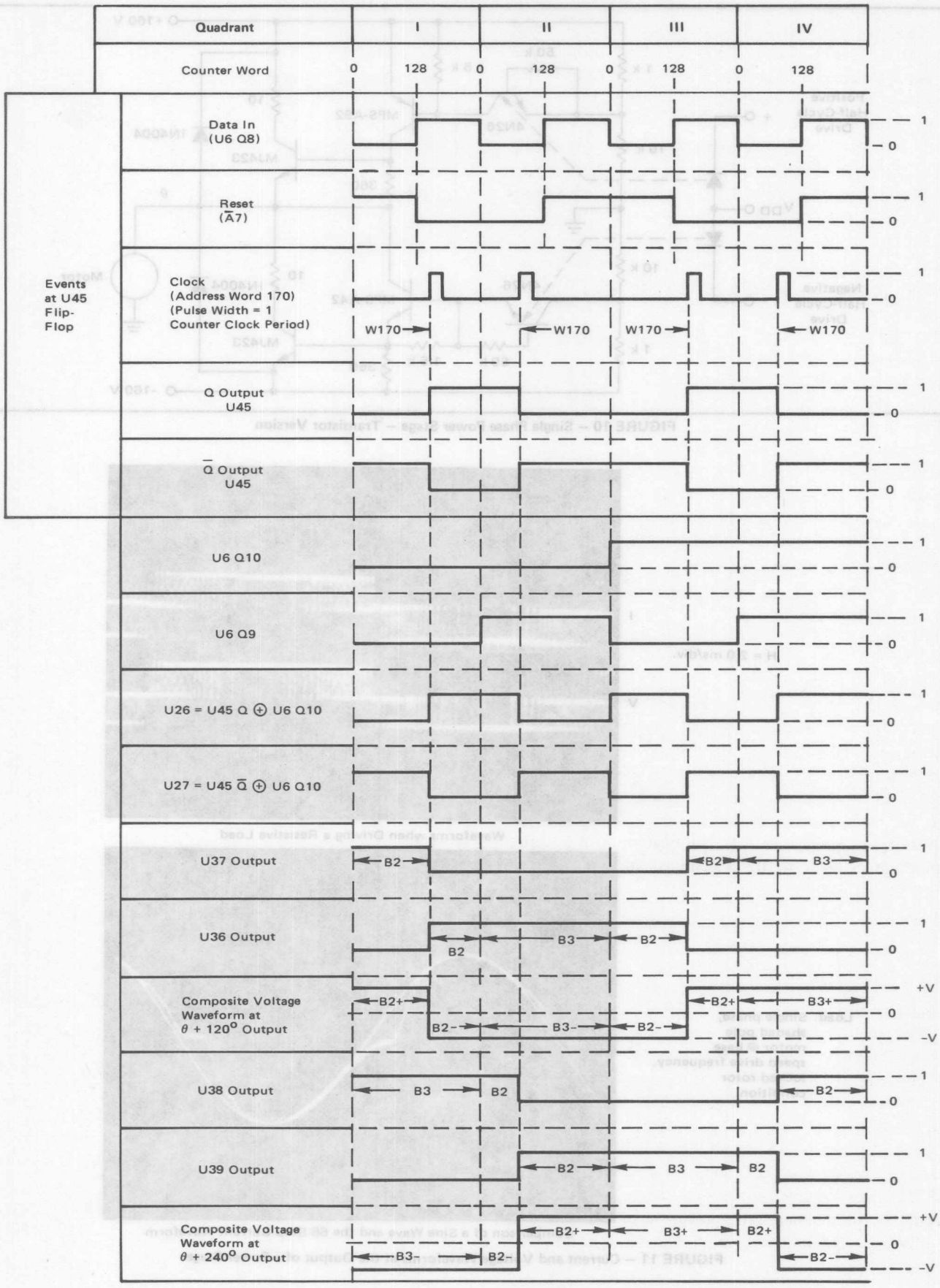


FIGURE 9 – Generation of θ + 120° and θ + 240° Outputs

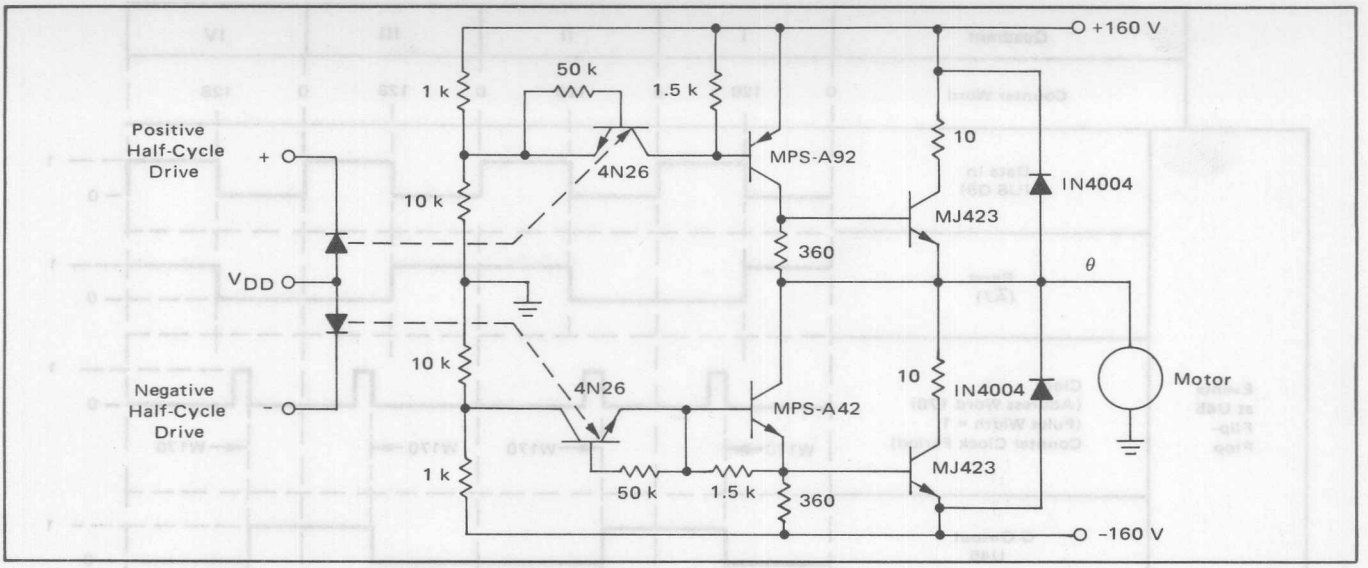
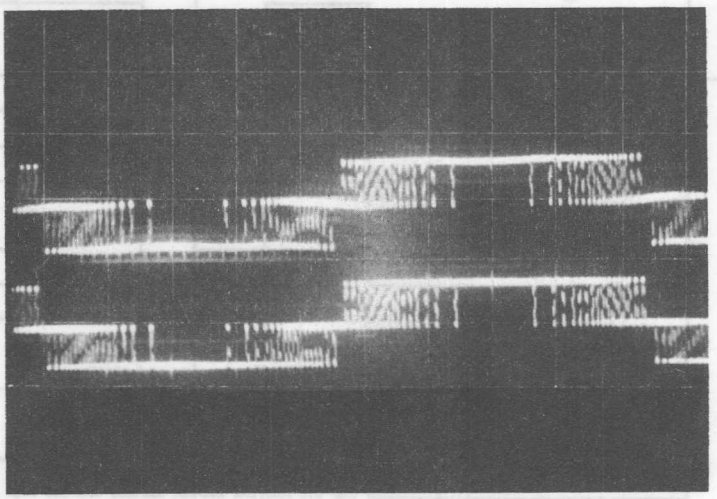
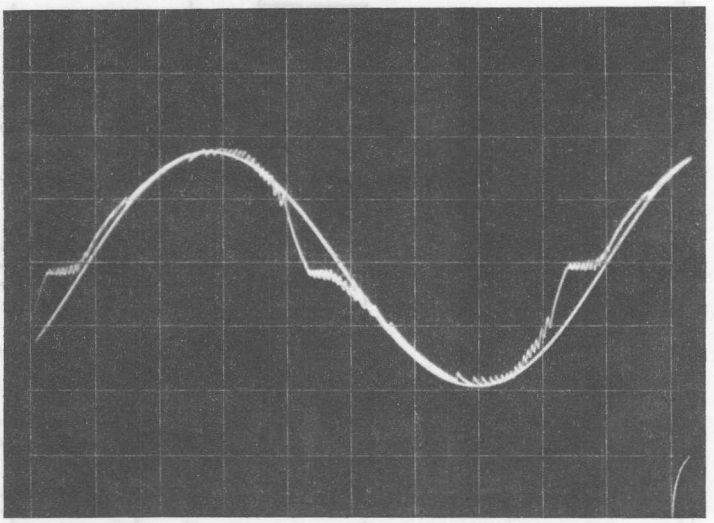


FIGURE 10 – Single Phase Power Stage – Transistor Version



H = 2.0 ms/div.

Waveforms when Driving a Resistive Load



Load: Single phase, shaded pole motor @ base speed drive frequency, locked rotor condition.

Comparison of a Sine Wave and the 68 Step Current Waveform

FIGURE 11 – Current and Voltage Waveforms at the Output of a Power Stage

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