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**MOTOROLA
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APPLICATION NOTE**

AN458

A self-test approach for the MC68HC11A/E

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INTRODUCTION

Since the introduction of the MC6805 family of single chip microcontrollers, it has been traditional for Motorola to provide a small section of ROM on-chip which is programmed at manufacture with self-test software. This software is designed to provide the user, with the aid of a simple Printed Circuit Board, the facility to perform a basic functional test of the chip. This facility can be a useful form of incoming inspection where a VLSI test system is unavailable.

Until now, this facility has not been provided on devices with an expanded mode of operation, due to their ability to address external memory. In this instance it is left to the user to write any test code. This, however, would not allow the user to test the part in the single chip mode, as it may be used in the application.

This application note therefore describes a self-test approach for the MC68HC11 which allows the part to operate in the single chip mode. This is performed by the use of the bootstrap feature of the MC68HC11 which allows user code to be downloaded, via the Serial Communications Interface (SCI), into the RAM of the device and executed. Test routines are also provided for all peripheral functions as well as the on-chip EEPROM. These test modules can also be used as templates for any user-defined test modules.

The description in this application note uses an MC68HC811E2 as the means of downloading the code, but this may also be replaced by a direct download from an IBM or compatible personal computer. If this facility is to be used, a level shift circuit must be used between this circuit and the PC and suitable software must be available for the PC.

HARDWARE DESCRIPTION

The hardware (Figure 1) consists of two parts: the device under test (DUT) and the tester (MC68HC811E2). The DUT is located in a zero insertion force socket with wrap around connections to interconnect all peripheral functions. On the A/D port (PortE) these connections are made by means of resistor ladders in order that the functionality of the A/D may be checked at varying voltages. In addition to this, some ports do not have Input/Output switching capability; an analogue switch (MC14066) is used to isolate these under control of PortB. All communication with the device for download of test code and return of pass/fail data is done via the SCI.

The tester is a second device with 2K of on-chip EEPROM (MC68HC811E2) containing the test routines and control software. This device connects to the SCI of the DUT and has a bank of LEDs for displaying the pass/fail condition and the fail test number.

The devices are isolated from each other with the exception of the SCI and Reset signals and have independent crystal oscillators. This isolation of the devices makes the circuit easily adaptable to direct download from a PC. In this instance the tester device would be omitted.

BOOTSTRAP MODE

The special bootstrap mode of operation is selected at reset by means of the MODA and MODB pins of the MC68HC11 (Table 1). When this mode is selected the reset vector is fetched from a small area of ROM known as the bootstrap ROM. The program in this ROM initialises the on-chip SCI and allows a 256 byte program to be downloaded through the SCI into the on-chip RAM. When the download is complete the program jumps to the start of RAM to execute the user program.

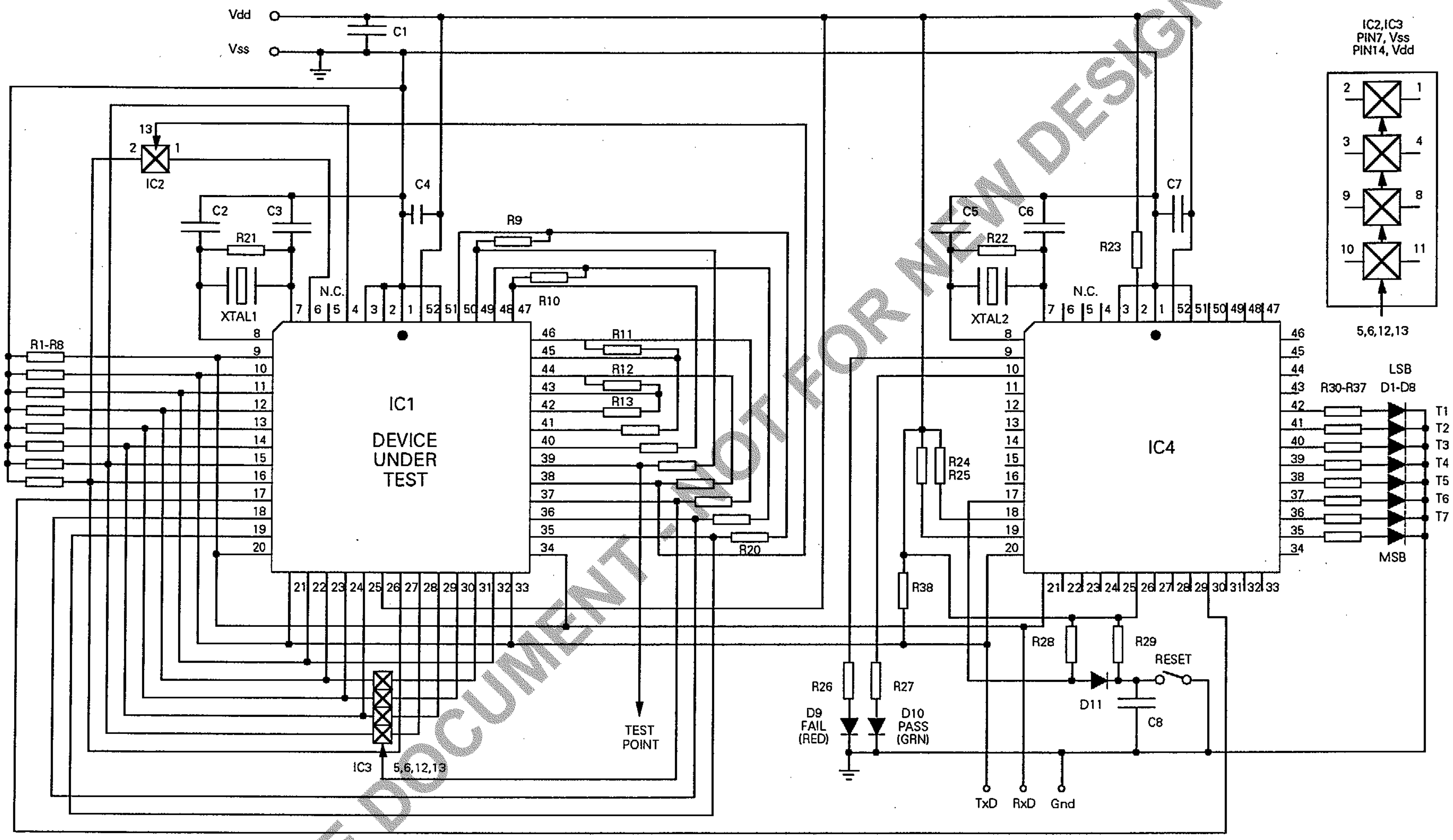

Figure 1. 68HC11 self-test board

PARTS LIST

R1–R8, R29	100K	R26, R27	3K3	C1	1µF, tant	D1–D8	LED, yellow	XTAL1, XTAL2	8MHz
R9-R12	22K	R28	10K	C2, C3	22pF	D9	LED, red		
R13-R20	10K	R29	100K	C4	0.1µF, cer	D10	LED, green	IC1	D.U.T. (52 PLCC ZIF socket)
R21, R22	10M	R30–R37	3K3	C5, C6	22pF	D11	1N914	IC2, IC3	MC14066
R23	4K7	R38	10K	C7, C8	0.1µF, cer			IC4	MC68HC811E2FN
R24, R25	10K	(All resistors 0.25W, 2% tol.)							

Table 1

MODB	MODA	Mode selected
1	0	Single Chip
1	1	Expanded Multiplexed
0	0	Special Bootstrap
0	1	Special Test

Table 2

Address	Vector
00C4	SCI
00C7	SPI
00CA	Pulse Accumulator Input Edge
00CD	Pulse Accumulator Overflow
00D0	Timer Overflow
00D3	Timer Output Compare 5
00D6	Timer Output Compare 4
00D9	Timer Output Compare 3
00DC	Timer Output Compare 2
00DF	Timer Output Compare 1
00E2	Timer Input Capture 3
00E5	Timer Input Capture 2
00E8	Timer Input Capture 1
00EB	Real Time Interrupt
00EE	IRQ
00F1	XIRQ
00F4	SWI
00F7	Illegal Opcode
00FA	COP Fail
00FD	Clock Monitor

The DUT bootloader program initialises its SCI receiver and transmitter to a baud rate defined by E clock/16/16 (7812 baud if E = 2MHz), after which a break character is transmitted. The tester then transmits $FF to establish the baud rate for the rest of the transmission. The 256 bytes of user code are then transmitted and are loaded from address $0000 in RAM. All 256 bytes must be sent; if the user program is shorter, dummy bytes should be used to make up the difference (some versions of the bootstrap routine do not require this but it is more universal to include it). Once all bytes have been received, the bootstrap program jumps to address $0000 and the downloaded (user) program gains control. On completion, the user program can then jump to the start of bootstrap ROM if another program is to be loaded or a loop can be executed. When developing user code it is important to note that many of the device registers will have been changed from their normal reset state by the bootstrap routine. The bootstrap software is available in the MC68HC11 Reference Manual (M68HC11RM/AD) and should be referred to before making assumptions regarding initial conditions.

If interrupt vectors are required to be used by the user program, these must be implemented in RAM. In the bootstrap mode, vectors are fetched from the bootstrap ROM rather than the normal memory location. Each of the bootstrap vectors points to an address in RAM (Table 2) where the user can place a pseudo vector. Each pseudo vector is allocated three bytes in RAM in order that an explicit jump to address might be implemented. In this way the user has full control over the vectors. If any vector is not required by the user, the respective RAM locations may be used for program space.

CONTROL SOFTWARE

The self-test software described in this application note consists of two basic parts; the control software and the test modules. The control software is designed to control the DUT by means of the reset line (connected to PA4) and downloads the appropriate test modules in sequence. Having reset the DUT in bootstrap mode, 256 bytes are downloaded and executed. The result obtained via the SCI then either indicates a pass or fail and the number of the failed test will be displayed. The tester expects a "P" (ASCII $50) for a pass and a "F" (ASCII $46) for a fail. No other response will be considered as an indication of test complete. The tester then forces another reset and begins the download for the next test.

The control software resides in the first 256 bytes of the assembled code ($F800–$F8FF) and each of the test routines is located in 256 byte blocks thereafter. The control software then downloads each 256 byte block in turn as it executes each of the tests.

TEST MODULES

Each one of the test modules is assembled at an absolute address, starting at $XX00 in 256 byte increments. As the tests are downloaded to the DUT, they are of course relocated to address $0000. Care must therefore be taken to use instructions which are relocatable.

The test modules are designed to fit into the 256 bytes of available RAM and each module performs one or more tests. A technique widely used in the software to save space is that of using the stack to pass variables to a subroutine. An example of this is given in Test 1, where PortB is outputting digital data to PortE and the data is variable ($FF,$AA,$55,$00). In this case the data is located in the two bytes immediately following the subroutine call and the port addresses in the next four bytes. From within the subroutine a pull of the stack would ordinarily retrieve the return address but in this case it contains the address of the first byte of data. Manipulation of this address by means of the index registers enables the data to be retrieved as well as the port addresses. In order that the CPU will then correctly return from the subroutine, the initial address pulled must then be incremented by six before pushing back on the stack and executing an RTS. In this way pseudo macros can be created which are very efficient in terms of the amount of code used.

The test modules described in this application note are suitable for use with the following devices but can be easily adapted for use with any of the MC68HC11 family of devices:

MC68HC11A1

MC68HC11A8

MC68HC11E1

MC68HC11E9

MC68HC11A0 (remove test 6 — EEPROM)

MC68HC11E0 (remove test 6 — EEPROM)

TEST 1a: PORTB output -> PORTE input

This is a digital test of Port B, which is output only, and wrapped around to Port E, which is input only. The test uses the pseudo macro approach previously mentioned where the first byte denotes the test data, the second byte denotes which bits to "care" on, the next two bytes are the output port address and the last two are the input port address.

```
i.e.    BSR PORTST
        FCB DATA,MASK
        FDB O/P PORT,I/P PORT
```

In this way, the same test can be performed many times with variable data. In this case the ports are tested for a high state, a low state and alternate highs and lows in both directions (i.e. FF, AA, 55, 00). If the test passes, a pass code ("P" = ASCII $50) is returned to the control MCU and the DUT will loop, toggling PortB 0,1,2 until reset. If the test fails, a fail code ("F" = ASCII $46) is returned and the DUT will loop through the tests. (Refer to "debug" section for more information.)

TEST 1b: Test strobe output (STRB) and pulse accumulator input (PAI)

The MC68HC11 has a special feature known as the handshake I/O subsystem. This subsystem provides a parallel handshake between the Port B output port and the Port C input port. Every time a write is made to Port B, a 2 E cycle pulse is output on the STRB pin.

Another feature of the MC68HC11 timer subsystem is the pulse accumulator. The Port A bit 7 pin (PAI) associated with the pulse accumulator can be configured to act as a clock to the counter or as a gated signal.

Both of these features are tested simultaneously by wrapping the STRB pin back to the PAI pin with the PAI pin configured as a clock input. In this way, any write to Port B will result in one count in the Pulse accumulator. For the purpose of this test, Port B is written to 85 times (Hex $55), after which the pulse accumulator is read and checked for $55.

TEST 2a: PORTC output -> PORT D input

This test checks the bidirectional Port C in the output mode and those pins of Port D which can be configured as inputs. The test is identical in nature to test 1a with the exception of the mask or "care" data. Because PD6,7 are not implemented as digital ports, they are masked. Also, the use of PD0,1 for the SCI communication conflicts with this test. The mask data used is therefore $3C (don't care PB0,1,6,7).

TEST 2b: PORTC output -> PORT A input

This test checks the bidirectional Port C in the output mode and those pins of Port A which can be configured as inputs. The test is identical in nature to test 1a with the exception of the mask or "care" data. Because PA3,4,5,6 cannot be configured as inputs they are masked. Also, the use of PD0,1 for the SCI communication conflicts with this test. The mask data used is therefore $84 (don't care PA0,1,3,4,5,6).

TEST 3a: PORTD output -> PORT C input

This test checks the bidirectional Port D in the output mode and the bidirectional Port C in the input mode. The test is identical in nature to test 1a with the exception of the mask or "care" data. Because PD6,7 are not implemented as output ports, they are masked. Also, the use of PD0,1 for the SCI communication conflicts with this test. The mask data used is therefore $3C (don't care PC0,1,6,7).

TEST 3b: PORTA output -> PORT C input

This test checks the bidirectional Port A in the output mode and the bidirectional Port C in the input mode. The test is identical in nature to test 1a with the exception of the mask or "care" data. Because PA0,1,2 are input only ports, they are masked. The mask data used is therefore $F8 (don't care PC0,1,2).

TEST 4: Test A/D convertor driven from PORT B

The MC68HC11 microcontrollers are equipped with an on-chip analogue-to-digital converter and this test is therefore designed to test the functionality of the converter. In order to keep the test jig as simple as possible, a resistor ladder is used to generate the analogue voltages. Between each Port B pin and the corresponding Port E pin is a serial 10K resistor. In addition, between corresponding bits in the higher and lower nibbles of Port E are 22K resistors (refer to test circuit). The result is that by manipulating the data output by Port B voltages of 100%, 75%, 25% and 0% of Vdd can be applied to each of the analogue inputs. For example, outputting a zero on PB0 and a one on PB4 would result in 25% Vdd on PE0 and 75% Vdd on PE4. One limitation of this test method is that the accuracy of the analogue voltage is dependent on the Port B V_{ol}/V_{oh} and on the accuracy of the resistors. Taking this into account, the test limits are set to plus or minus (2% + 2 bits).

The software uses the same pseudo macro approach used for the port tests with different variables. In this case the first byte is the data to be output on Port B and the second is the data for the A/D control register which determines which channels to convert. The next two bytes are the upper and lower limits of the acceptable digital result from the analogue voltage.

```
i.e.   BSR ADTST
       FCB O/P DATA, CHANNELS, MIN VALUE,
       MAX VALUE
```

By repeating the same test eight times with different variables, all eight channels can therefore be checked at four voltage levels.

TEST 5: Test IRQ, XIRQ

Two external interrupt pins are available on the MC68HC11. These are referred to as IRQ and XIRQ and are connected by the test circuit to PB7 and PB6 respectively.

The test is performed by firstly clearing any interrupts which may be pending. When an interrupt does occur, a flag is set in the interrupt routine. If a spurious interrupt (or stuck low) occurs prior to the valid interrupt (generated from PortB), this will be detected by the setting of this flag. Conversely, when the appropriate Port B pin is pulled low, the test checks that a valid interrupt does occur. This is done by using the flag which is set in the interrupt routine to jump over the instruction which would otherwise force a fail. Both IRQ and XIRQ are tested in the same way. This is one test where it is essential to implement the vectors in RAM, as shown in the software listing.

One point to note is that an interrupt pin stuck low will typically cause the processor to remain permanently in the interrupt routine, thereby hanging up the test. In this case no pass or fail indication would be observed, since control of the DUT can only be recovered by a reset. The only indication would be the illumination of the test number LED.

TEST 6: Test EEPROM

This test checks the 512 bytes of on-chip EEPROM. The test checks for all bits erased ($FF), all bits programmed ($00), checkerboard (alternate ones and zeros) and inverse checkerboard. The topology of the EEPROM array is in rows of 32 bytes so a checkerboard pattern requires that the data alternates from $AA to $55 every 32 bytes.

The test again uses the pseudo macro approach to pass the variable data to the program/verify routine. In this way different data can be loaded into each alternate row of 32 bytes. The programming time for each byte is set by the routine "EEDEL" to 10ms. This 10ms delay makes each pass of 512 bytes take approximately 5 seconds, so the complete test is around 15 seconds.

TEST 7: Test STRA — PORT C input strobe

Part of the handshake I/O subsystem is the input latch facility on Port C. This feature operates by latching any data on Port C into the Port C latch register (as distinct from the Port C data register) on the occurrence of a pulse on the STRA input.

This test therefore configures Port C as an input with data presented to it from Port D which is configured as an output. One exception is PC6 which is configured as an output and is used to drive the STRA input. In this way by writing a "1" to PC6, the edge on the STRA pin will automatically latch the data on all other Port C pins, as presented by Port D. This test is performed three times with the data $00, $FF, $00 to ensure that the latched data is changing state. Only bits PC2–PC5 are "cared", as PD0, PD1 are used for the SCI and PD6, PD7 are not implemented.

USER DEFINED ROUTINES

In addition to the above test routines, any user routine may be downloaded, provided certain criteria are met.

The routine must be 256 bytes long, even if dummy bytes have to be added. If vectors are required, these must be mapped as shown in Table 2 and implemented as a jump instruction. The initial conditions of the device are changed by the bootstrap routine, so no assumptions should be made regarding machine state. The code must be written to be relocatable, as it will be loaded at address $0000 for execution. This precludes the use of JSR instructions, for example, and BSR should be used instead. Also, because the SCI is used to download the software, care must be taken if it is to be incorporated into a user test routine.

TEST RESULTS

After insertion of the DUT, application of power and release of the reset, each test will be executed in sequence and the test number LEDs will display each test in turn. This display will increment rapidly until Test 6 (EEPROM), at which point it will pause for approximately 15 seconds. Successful completion of all tests will then be indicated by a green pass LED and all test number LEDs will be blanked. A failure will be represented by a red fail LED accompanied by the LED for the failing test. If the DUT fails to return a pass or fail indication, this will be represented by the LED for the failing test remaining illuminated but neither the pass nor fail LED will illuminate.

Debug

In the case of a fail, a basic facility is provided on some tests for debug via the test point on PB3. At the beginning of the test sequence, a synchronisation pulse of 98 E clocks (approx. 50µs) is output on PB3. Also, each time a test fails, a fail pulse of 11 E clocks (approx. 5µs) is output on the same pin. By connecting an oscilloscope to the test point and measuring the timing of the fail pulse (or pulses) relative to the sync pulse, it can be determined which sub-test is failing (eg. port stuck high or stuck low). By then observing each bit of the port, the bit at fault can also be isolated. This basic debug approach uses very little code and can effectively isolate the problem bits, but more sophisticated routines can be written by the user provided RAM space allows. This facility is not available for test 6, due to the wearout effect of repeated write/erase cycling of the EEPROM.

APPENDIX – PROGRAM LISTING

```
M68HC11 Absolute Assembler   Version 2.61C:HC11TEST.ASC

A                 ************************************************************** ************
A                 *
A                 *           68HC11 SELFTEST PROGRAM
A                 *
A                 *           WRITTEN BY: PAT JORDAN
A                 *
A                 *        REV 0     15/01/92  ORIGINAL VERSION              PDJ.
A                 *
A                 ************************************************************** ****************
A                 *
A 0000                     INCL      HC11REG.ASC
A                 * MC68HC11 register block addresses
A                 *
A      1000       RB       EQU       $1000
A      1000       PORTA    EQU       RB+$00
A      1002       PIOC     EQU       RB+$02
A      1003       PORTC    EQU       RB+$03
A      1004       PORTB    EQU       RB+$04
A      1005       PORTCL   EQU       RB+$05
A      1007       DDRC     EQU       RB+$07
A      1008       PORTD    EQU       RB+$08
A      1009       DDRD     EQU       RB+$09
A      100A       PORTE    EQU       RB+$0A
A      100B       CFORC    EQU       RB+$0B
A      100C       OC1M     EQU       RB+$0C
A      100D       OC1D     EQU       RB+$0D
A      100E       TCNT     EQU       RB+$0E
A      1010       TIC1     EQU       RB+$10
A      1012       TIC2     EQU       RB+$12
A      1014       TIC3     EQU       RB+$14
A      1016       TOC1     EQU       RB+$16
A      1018       TOC2     EQU       RB+$18
A      101A       TOC3     EQU       RB+$1A
A      101C       TOC4     EQU       RB+$1C
A      101E       TOC5     EQU       RB+$1E
A      1020       TCTL1    EQU       RB+$20
A      1021       TCTL2    EQU       RB+$21
A      1022       TMSK1    EQU       RB+$22
A      1023       TFLG1    EQU       RB+$23
A      1024       TMSK2    EQU       RB+$24
A      1025       TFLG2    EQU       RB+$25
A      1026       PACTL    EQU       RB+$26
A      1027       PACNT    EQU       RB+$27
A      1028       SPCR     EQU       RB+$28
A      1029       SPSR     EQU       RB+$29
A      102A       SPDR     EQU       RB+$2A
A      102B       BAUD     EQU       RB+$2B
A      102C       SCCR1    EQU       RB+$2C
A      102D       SCCR2    EQU       RB+$2D
A      102E       SCSR     EQU       RB+$2E
A      102F       SCDR     EQU       RB+$2F
A      1030       ADCTL    EQU       RB+$30
A      1031       ADR1     EQU       RB+$31
A      1032       ADR2     EQU       RB+$32
A      1033       ADR3     EQU       RB+$33
A      1034       ADR4     EQU       RB+$34
A      1035       BPROT    EQU       RB+$35
A      1039       OPTION   EQU       RB+$39
A      103A       COPRST   EQU       RB+$3A
A      103B       PPROG    EQU       RB+$3B
A      103C       HPRIO    EQU       RB+$3C
A      103D       INIT     EQU       RB+$3D
A      103E       TEST1    EQU       RB+$3E
A      103F       CONFIG   EQU       RB+$3F
A                 *
A                 *
A                 *
A      B600       EEPROM   EQU       $B600
A      B800       EETOP    EQU       $B800
A                 *
```

```
 71 A                    ************************************************************ ***************
 72 A                    *
 73 A       0000                   ORG       $0000
 74 P 0000 0001         TESTNUM    RMB       1
 75 A                    *
 76 A       00F8                   ORG       $00F8
 77 P 00F8 0001         TSTNUM     RMB       1
 78 P 00F9 0001         PASFLG     RMB       1
 79 P 00FA 0001         TEMP       RMB       1
 80 P 00FB 0001         TEMP1      RMB       1
 81 P 00FC 0001         DUMMY      RMB       1
 82 P 00FD 0001         COUNT      RMB       1
 83 A                    *
 84 A                    ************************************************************ ***************
 85 A                              PAGE
 86 A                    ************************************************************ ***************
 87 A                    * T0      INITIALISATION ROUTINE
 88 A                    ************************************************************ ***************
 89 A                    *
 90 A       F800                   ORG       $F800
 91 A F800 8E00FF       RESET      LDS       #$00FF
 92 A F803 86FF                    LDAA      #$FF
 93 A F805 B71007                  STAA      DDRC
 94 A F808 8690                    LDAA      #$90
 95 A F80A B71039                  STAA      OPTION
 96 A F80D 4F                      CLRA
 97 A F80E 5F                      CLRB
 98 A F80F CE0000                  LDX       #$00
 99 A F812 7F1004                  CLR       PORTB
100 A F815 7F1003                  CLR       PORTC
101 A F818 7F1008                  CLR       PORTD
102 A F81B 7F0000                  CLR       TESTNUM
103 A                    ************************************************************ ***************
104 A                    *
105 A                    *
106 A F81E 8601                    LDAA      #$01
107 A F820 B71004                  STAA      PORTB
108 A F823 7C0000                  INC       TESTNUM
109 A F826 CEF900                  LDX       #T1
110 A F829 BDF87E                  JSR       TEST
111 A                    *
112 A F82C 781004                  LSL       PORTB
113 A F82F 7C0000                  INC       TESTNUM
114 A F832 CEFA00                  LDX       #T2
115 A F835 BDF87E                  JSR       TEST
116 A                    *
117 A F838 781004                  LSL       PORTB
118 A F83B 7C0000                  INC       TESTNUM
119 A F83E CEFB00                  LDX       #T3
120 A F841 BDF87E                  JSR       TEST
121 A                    *
122 A F844 781004                  LSL       PORTB
123 A F847 7C0000                  INC       TESTNUM
124 A F84A CEFC00                  LDX       #T4
125 A F84D BDF87E                  JSR       TEST
126 A                    *
127 A F850 781004                  LSL       PORTB
128 A F853 7C0000                  INC       TESTNUM
129 A F856 CEFD00                  LDX       #T5
130 A F859 BDF87E                  JSR       TEST
131 A                    *
132 A F85C 781004                  LSL       PORTB
133 A F85F 7C0000                  INC       TESTNUM
134 A F862 CEFE00                  LDX       #T6
135 A F865 BDF87E                  JSR       TEST
136 A                    *
137 A F868 781004                  LSL       PORTB
138 A F86B 7C0000                  INC       TESTNUM
139 A F86E CEFF00                  LDX       #T7
140 A F871 BDF87E                  JSR       TEST
141 A                    *
142 A F874 8602                    LDAA      #$02
143 A F876 B71003                  STAA      PORTC
144 A F879 7F1004                  CLR       PORTB
145 A F87C 20FE                    BRA       *
146 A                    *
```

```
A                    *************************************************************** ***************
A                    *
A                    *       DOWNLOAD TEST CODE TO DUT
A                    *
A F87E 18CE1000      TEST      LDY       #$1000
A F882 8622                    LDAA      #$22
A F884 B7102B                  STAA      BAUD
A F887 860C                    LDAA      #$0C
A F889 B7102D                  STAA      SCCR2
A F88C 181D0010                BCLR      PORTA-$1000,Y,#$10    ASSERT RESET
A F890 C601                    LDAB      #$01
A F892 BDF8E1                  JSR       PAUSE
A F895 181C0010                BSET      PORTA-$1000,Y,#$10    RELEASE RESET
A F899 C601                    LDAB      #$01
A F89B BDF8E1                  JSR       PAUSE
A                    *
A                    *       START TRANSMISSION
A                    *
A F89E B6102E                  LDAA      SCSR
A F8A1 86FF                    LDAA      #$FF
A F8A3 B7102F                  STAA      SCDR
A F8A6 18CE0101                LDY       #$0101
A F8AA B6102E        STLWT     LDAA      SCSR
A F8AD 8580                    BITA      #$80
A F8AF 27F9                    BEQ       STLWT
A F8B1 B6102F                  LDAA      SCDR
A F8B4 A600                    LDAA      0,X
A F8B6 B7102F                  STAA      SCDR
A F8B9 08                      INX
A F8BA 1809                    DEY
A F8BC 26EC                    BNE       STLWT
A F8BE 8630                    LDAA      #$30
A F8C0 B7102B                  STAA      BAUD
A                    *
A F8C3 B6102E        ANSWER    LDAA      SCSR                  CLEAR FLAG
A F8C6 B6102F                  LDAA      SCDR
A F8C9 181F2E20FB              BRCLR     SCSR-$1000,Y,#$20,*   WAIT FOR TEST DATA
A F8CE B6102F                  LDAA      SCDR
A F8D1 8146                    CMPA      #$46                  CHECK FOR 'F'ail
A F8D3 2705                    BEQ       REJECT
A F8D5 8150                    CMPA      #$50
A F8D7 26EA                    BNE       ANSWER
A F8D9 39                      RTS
A                    *
A F8DA 8601          REJECT    LDAA      #$01
A F8DC B71003                  STAA      PORTC
A F8DF 20FE                    BRA       *
A                    *
A                    *       PAUSE FOR 0.1 SEC * VALUE IN ACC B
A                    *
A F8E1 3C            PAUSE     PSHX
A F8E2 CE2800        PAU02     LDX       #10240
A F8E5 09            PAU01     DEX
A F8E6 26FD                    BNE       PAU01
A F8E8 5A                      DECB
A F8E9 26F7                    BNE       PAU02
A F8EB 38                      PULX
A F8EC 39                      RTS
A                    *
A                    *************************************************************** **************
A                    *     VECTORS
A                    *************************************************************** ***************
A                    *
A      FFD6                    ORG       $FFD6
A FFD6 F800                    FDB       RESET                 SCI
A FFD8 F800                    FDB       RESET                 SPI
A FFDA F800                    FDB       RESET                 PULSE ACC I/P
A FFDC F800                    FDB       RESET                 PULSE ACC OVFL
A FFDE F800                    FDB       RESET                 TIMER OVFL
A FFE0 F800                    FDB       RESET                 O/P COMP 5
A FFE2 F800                    FDB       RESET                 O/P COMP 4
A FFE4 F800                    FDB       RESET                 O/P COMP 3
A FFE6 F800                    FDB       RESET                 O/P COMP 2
A FFE8 F800                    FDB       RESET                 O/P COMP 1
A FFEA F800                    FDB       RESET                 I/P CAPT 3
```

```
222 A FFEC F800              FDB      RESET               I/P CAPT 2
223 A FFEE F800              FDB      RESET               I/P CAPT 1
224 A FFF0 F800              FDB      RESET               REAL TIM INT
225 A FFF2 F800              FDB      RESET               IRQ
226 A FFF4 F800              FDB      RESET               XIRQ
227 A FFF6 F800              FDB      RESET               SWI
228 A FFF8 F800              FDB      RESET               ILLEGAL OPCODE
229 A FFFA F800              FDB      RESET               COP
230 A FFFC F800              FDB      RESET               CLOCK MONITOR
231 A FFFE F800              FDB      RESET               RESET
232 A                ********************************************************* ***********
233 A                        PAGE
234 A                ********************************************************* **************
235 A                *
236 A                *       START OF TEST ROUTINE
237 A                *
238 A 0000                   INCL     T1.SA
239 A                ********************************************************* **************
240 A                * T1a    TEST PORT B TO PORT E IN DIGITAL MODE
241 A                ********************************************************* **************
242 A                *
243 A                *    FORMAT:
244 A                *       BSR     PORTST
245 A                *       FCB     DATA,MASK
246 A                *       FDB     O/P PORT, I/P PORT
247 A                *
248 A      F9F8              ORG      $F9F8
249 A F9F8 0150000000        FCB      $01,$50,$00,$00,$00,$00,$00,$00RESERVED BYTES
       000000
250 A                *
251 A      F900              ORG      $F900
252 A F900 8E00F7    T1      LDS      #$F7                PLACE STACK BELOW RMB
253 A F903 8D6D              BSR      SYNC1
254 A F905 8D7D              BSR      PORTST1             CHECK FOR $FF
255 A F907 FFFF              FCB      $FF,$FF
256 A F909 1004100A          FDB      PORTB,PORTE
257 A                *
258 A F90D 8D75              BSR      PORTST1             CHECK FOR $AA
259 A F90F AAFF              FCB      $AA,$FF
260 A F911 1004100A          FDB      PORTB,PORTE
261 A                *
262 A F915 8D6D              BSR      PORTST1             CHECK FOR $55
263 A F917 55FF              FCB      $55,$FF
264 A F919 1004100A          FDB      PORTB,PORTE
265 A                *
266 A F91D 8D65              BSR      PORTST1             CHECK FOR $00
267 A F91F 00FF              FCB      $00,$FF
268 A F921 1004100A          FDB      PORTB,PORTE
269 A                *
270 A                ********************************************************* ***************
271 A                * T1b    TEST STRB (STROBE) O/P AND PULSE ACCUMULATOR
272 A                ********************************************************* ***************
273 A                *
274 A                *        TEST IS PERFORMED BY LOOPING STRB O/P BACK TO THE PULSE
275 A                *        ACCUMULATOR INPUT. PORT B IS WRITTEN TO AND WRITES ARE
276 A                *        COUNTED.
277 A                *
278 A F925 8640              LDAA     #$40
279 A F927 B71026            STAA     PACTL
280 A F92A 86D0              LDAA     #$D0
281 A F92C 7F1027            CLR      PACNT               CLR THE COUNTER
282 A F92F CE0055            LDX      #$55                SET-UP FOR $55 WRITES TO PORTB
283 A F932 B71004    PACC1   STAA     PORTB               CONFIGURE GATES
284 A F935 09                DEX
285 A F936 26FA              BNE      PACC1               WAIT FOR $55 WRITES
286 A                *
287 A F938 F61027            LDAB     PACNT               READ COUNTER
288 A F93B C155              CMPB     #$55
289 A F93D 2702              BEQ      PACC2               EXIT IF CORRECT
290 A F93F 8D7A              BSR      FAIL1               CLR PASFLG IF FAILED
291 A F941 86C0      PACC2   LDAA     #$C0
292 A F943 B71004            STAA     PORTB               TURN GATES OFF
293 A                *
```

```
A                 ************************************************************* **************
A                 *         FINALLY
A                 *
A                 *         THIS ROUTINE RETURNS THE PASS/FAIL STATUS TO THE MASTER
A                 *
A F946 18FE1000   FINAL1    LDY       $1000
A F94A 7F102C               CLR       SCCR1
A F94D 8630                 LDAA      #$30
A F94F B7102B               STAA      BAUD
A F952 181C2D08             BSET      SCCR2-$1000,Y,#$08    ENABLE TRANSMITTER
A F956 B6102E               LDAA      SCSR                  CLEAR FLAGS
A F959 96F9                 LDAA      PASFLG
A F95B B7102F               STAA      SCDR                  PASS/FAIL BYTE IN TRANSMITTER
A                 *
A F95E 8150                 CMPA      #$50
A F960 269E                 BNE       T1                    LOOP IF YOU FAILED FOR DEBUG
A                 *
A                 ************************************************************* **************
A                 *
A F962 86C0                 LDAA      #$C0                  ALL LEDS OFF
A F964 C6C7                 LDAB      #$C7                  ALL LEDS ON
A F966 F71004     P01       STAB      PORTB
A F969 8D41                 BSR       DELAY1
A F96B B71004               STAA      PORTB
A F96E 8D3C                 BSR       DELAY1
A F970 20D4                 BRA       FINAL1
A                 *
A                 ************************************************************* **************
A                 *        SUBROUTINES
A                 ************************************************************* **************
A                 *
A                 *         SUBROUTINE SYNC
A                 *
A F972 CE1000     SYNC1     LDX       #$1000
A F975 18CE000D             LDY       #$0D
A F979 1C0408               BSET      PORTB-$1000,X,#$08    SYNC PULSE OF 98 E CLOCKS
A F97C 1809       S11       DEY
A F97E 26FC                 BNE       S11
A F980 1D0408               BCLR      PORTB-$1000,X,#$08
A F983 39                   RTS
A                 *
A                 ************************************************************* **************
A                 *
A                 *        SUBROUTINE PORTST
A                 *
A F984 38         PORTST1   PULX
A F985 A600                 LDAA      $0,X                  LOAD ACC A WITH O/P DATA
A F987 1AEE02               LDY       $2,X                  CONFIGURE O/P PORT
A F98A 18A700               STAA      $0,Y
A F98D 1AEE04               LDY       $4,X                  SET-UP I/P PORT ADDRESS
A F990 18A800               EORA      $0,Y                  COMPARE O/P AND I/P
A F993 A401                 ANDA      $1,X                  MASK OUT DONT CARES
A F995 2713                 BEQ       A11                   EXIT IF PASS
A                 *
A                 *         IF FAILED THEN.....
A                 *
A F997 8646                 LDAA      #$46                  ASCII 'F'
A F999 97F9                 STAA      PASFLG
A F99B DFFB                 STX       TEMP1
A F99D CE1000               LDX       #$1000
A F9A0 1C0408               BSET      PORTB-$1000,X,#$08    FAIL PULSE OF 11 E CLOCKS
A F9A3 01                   NOP
A F9A4 01                   NOP
A F9A5 1D0408               BCLR      PORTB-$1000,X,#$08
A F9A8 DEFB                 LDX       TEMP1
A                 *
A F9AA 6E06       A11       JMP       $6,X                  CONTINUE MAIN PROGRAM
A                 *
A                 ************************************************************* **************
A                 *
```

```
364 A                    *        SUBROUTINE DELAY
365 A                    *
366 A F9AC 18CE0001      DELAY1   LDY       #$0001                 SETS THE FLASH RATE
367 A F9B0 CEFFFF        D01      LDX       #$FFFF
368 A F9B3 09            D11      DEX
369 A F9B4 26FD                   BNE       D11
370 A F9B6 1809                   DEY
371 A F9B8 26F6                   BNE       D01
372 A F9BA 39                     RTS
373 A                    *
374 A                    ************************************************************** **************
375 A                    *
376 A                    *       SUBROUTINE FAIL
377 A                    *
378 A F9BB 8646          FAIL1    LDAA      #$46
379 A F9BD 97F9                   STAA      PASFLG
380 A F9BF DFFB                   STX       TEMP1
381 A F9C1 CE1000                 LDX       #$1000
382 A F9C4 1C0408                 BSET      PORTB-$1000,X,#$08    FAIL PULSE OF 11 E CLOCKS
383 A F9C7 01                     NOP
384 A F9C8 01                     NOP
385 A F9C9 1D0408                 BCLR      PORTB-$1000,X,#$08
386 A F9CC DEFB                   LDX       TEMP1
387 A F9CE 39                     RTS
388 A                    *
389 A                    ************************************************************** **************
390 A F9CF                        INCL      T2.SA
391 A                    ************************************************************** **************
392 A                    * T2a    TEST PORTC O/P TO PORTD I/P IN DIGITAL MODE
393 A                    ************************************************************** **************
394 A                    *
395 A                    *    FORMAT:
396 A                    *        BSR      PORTST
397 A                    *        FCB      DATA,MASK
398 A                    *        FDB      O/P PORT, I/P PORT
399 A                    *
400 A      FAF8                   ORG      $FAF8
401 A FAF8 0250000000             FCB      $02,$50,$00,$00,$00,$00,$00,$00RESERVED BYTES
           000000
402 A                    *
403 A      FA00                   ORG      $FA00
404 A FA00 8E00F7        T2       LDS      #$F7                    PLACE STACK BELOW RMB
405 A FA03 2012                   BRA      T21
406 A                    *
407 A FA05 CE1000        SYNC2    LDX      #$1000
408 A FA08 18CE000D               LDY      #$0D
409 A FA0C 1C0408                 BSET     PORTB-$1000,X,#$08     SYNC PULSE OF 98 E CLOCKS
410 A FA0F 1809          S12      DEY
411 A FA11 26FC                   BNE      S12
412 A FA13 1D0408                 BCLR     PORTB-$1000,X,#$08
413 A FA16 39                     RTS
414 A                    *
415 A FA17 86C0          T21      LDAA     #$C0                    CONFIG PORTB TO DRIVE GATES
416 A FA19 B71004                 STAA     PORTB
417 A FA1C 8DE7                   BSR      SYNC2
418 A FA1E 86FC                   LDAA     #$FC                    CONFIGURE PORTC AS O/P
419 A FA20 B71007                 STAA     DDRC
420 A                    *
421 A FA23 8D75                   BSR      PORTST2                 CHECK FOR $FF
422 A FA25 FF3C                   FCB      $FF,$3C
423 A FA27 10031008               FDB      PORTC,PORTD
424 A                    *
425 A FA2B 8D6D                   BSR      PORTST2                 CHECK FOR $AA
426 A FA2D AA3C                   FCB      $AA,$3C
427 A FA2F 10031008               FDB      PORTC,PORTD
428 A                    *
429 A FA33 8D65                   BSR      PORTST2                 CHECK FOR $55
430 A FA35 553C                   FCB      $55,$3C
431 A FA37 10031008               FDB      PORTC,PORTD
432 A                    *
433 A FA3B 8D5D                   BSR      PORTST2                 CHECK FOR $00
434 A FA3D 003C                   FCB      $00,$3C
435 A FA3F 10031008               FDB      PORTC,PORTD
436 A                    *
```

```
A                    **************************************************************** **************
A                    * T2b    TEST PORTC O/P TO PORTA I/P IN DIGITAL MODE
A                    **************************************************************** **************
A                    *
A                    *    FORMAT:
A                    *        BSR       PORTST
A                    *        FCB       DATA,MASK
A                    *        FDB       O/P PORT, I/P PORT
A                    *
A FA43 8D55                    BSR       PORTST2                CHECK FOR $FF
A FA45 FF84                    FCB       $FF,$84
A FA47 10031000                FDB       PORTC,PORTA
A                    *
A FA4B 8D4D                    BSR       PORTST2                CHECK FOR $AA
A FA4D AA84                    FCB       $AA,$84
A FA4F 10031000                FDB       PORTC,PORTA
A                    *
A FA53 8D45                    BSR       PORTST2                CHECK FOR $55
A FA55 5584                    FCB       $55,$84
A FA57 10031000                FDB       PORTC,PORTA
A                    *
A FA5B 8D3D                    BSR       PORTST2                CHECK FOR $00
A FA5D 0084                    FCB       $00,$84
A FA5F 10031000                FDB       PORTC,PORTA
A                    *
A FA63 7F1007                  CLR       DDRC
A                    *
A                    **************************************************************** **************
A                    *         FINALLY
A                    *
A                    *         THIS ROUTINE RETURNS THE PASS/FAIL STATUS TO THE MASTER
A                    *
A FA66 18FE1000      FINAL2    LDY       $1000
A FA6A 7F102C                  CLR       SCCR1
A FA6D 8630                    LDAA      #$30
A FA6F B7102B                  STAA      BAUD
A FA72 181C2D08                BSET      SCCR2-$1000,Y,#$08     ENABLE TRANSMITTER
A FA76 B6102E                  LDAA      SCSR                   CLEAR FLAGS
A FA79 96F9                    LDAA      PASFLG
A FA7B B7102F                  STAA      SCDR                   PASS/FAIL BYTE IN TRANSMITTER
A FA7E 181F2E80FB              BRCLR     SCSR-$1000,Y,#$80,*
A FA83 B7102F                  STAA      SCDR
A                    *
A FA86 8150                    CMPA      #$50
A FA88 268D                    BNE       T21                    LOOP IF YOU FAILED FOR DEBUG
A                    *
A                    **************************************************************** ***************
A                    *
A FA8A 86C0                    LDAA      #$C0                   ALL LEDS OFF
A FA8C C6C7                    LDAB      #$C7                   ALL LEDS ON
A FA8E F71004        P02       STAB      PORTB
A FA91 8D2F                    BSR       DELAY2
A FA93 B71004                  STAA      PORTB
A FA96 8D2A                    BSR       DELAY2
A FA98 20CC                    BRA       FINAL2
A                    *
A                    **************************************************************** **************
A                    *        SUBROUTINES
A                    **************************************************************** **************
A                    *
A                    *        SUBROUTINE PORTST
A                    *
A FA9A 38            PORTST2   PULX
A FA9B A600                    LDAA      $0,X                   LOAD ACC A WITH O/P DATA
A FA9D 1AEE02                  LDY       $2,X                   CONFIGURE O/P PORT
A FAA0 18A700                  STAA      $0,Y
A FAA3 1AEE04                  LDY       $4,X                   SET-UP I/P PORT ADDRESS
A FAA6 18A800                  EORA      $0,Y                   COMPARE O/P AND I/P
A FAA9 A401                    ANDA      $1,X                   MASK OUT DONT CARES
A FAAB 2713                    BEQ       A12                    EXIT IF PASS
A                    *
A                    *         IF FAILED THEN.....
A                    *
A FAAD 8646                    LDAA      #$46                   ASCII 'F'
A FAAF 97F9                    STAA      PASFLG
```

```
A FAB1 DFFB                     STX       TEMP1
A FAB3 CE1000                   LDX       #$1000
A FAB6 1C0408                   BSET      PORTB-$1000,X,#$08    FAIL PULSE OF 11 E CLOCKS
A FAB9 01                       NOP
A FABA 01                       NOP
A FABB 1D0408                   BCLR      PORTB-$1000,X,#$08
A FABE DEFB                     LDX       TEMP1
A                      *
A FAC0 6E06            A12      JMP       $6,X                  CONTINUE MAIN PROGRAM
A                      *
A                      ***************************************************************** **************
A                      *
A                      *        SUBROUTINE DELAY
A                      *
A FAC2 18CE0001        DELAY2   LDY       #$0001                SETS THE FLASH RATE
A FAC6 CEFFFF          D02      LDX       #$FFFF
A FAC9 09              D12      DEX
A FACA 26FD                     BNE       D12
A FACC 1809                     DEY
A FACE 26F6                     BNE       D02
A FAD0 39                       RTS
A                      *
A                      ***************************************************************** **************
A FAD1                          INCL      T3.SA
A                      ***************************************************************** **************
A                      * T3a    TEST PORTD O/P TO PORTC I/P IN DIGITAL MODE
A                      ***************************************************************** **************
A                      *
A                      *    FORMAT:
A                      *        BSR      PORTST
A                      *        FCB      DATA,MASK
A                      *        FDB      O/P PORT, I/P PORT
A                      *
A      FBF8                     ORG       $FBF8
A FBF8 0350000000               FCB       $03,$50,$00,$00,$00,$00,$00,$00RESERVED BYTES
       000000
A                      *
A      FB00                     ORG       $FB00
A FB00 8E00F7          T3       LDS       #$F7                  PLACE STACK BELOW VECTORS AND RMB
A FB03 2012                     BRA       T31
A                      *
A FB05 CE1000          SYNC3    LDX       #$1000
A FB08 18CE000D                 LDY       #$0D
A FB0C 1C0408                   BSET      PORTB-$1000,X,#$08    SYNC PULSE OF 98 E CLOCKS
A FB0F 1809            S13      DEY
A FB11 26FC                     BNE       S13
A FB13 1D0408                   BCLR      PORTB-$1000,X,#$08
A FB16 39                       RTS
A                      *
A FB17 86C0            T31      LDAA      #$C0
A FB19 B71004                   STAA      PORTB                 CONFIGURE PORTB TO DRIVE GATES
A FB1C 8DE7                     BSR       SYNC3
A FB1E 8604                     LDAA      #$04
A FB20 B71028                   STAA      SPCR                  CONFIGURE PORTD IN CMOS MODE
A FB23 86FF                     LDAA      #$FF
A FB25 B71009                   STAA      DDRD                  CONFIGURE PORTD AS O/P
A                      *
A FB28 8D7A                     BSR       PORTST3               CHECK FOR $FF
A FB2A FF3C                     FCB       $FF,$3C
A FB2C 10081003                 FDB       PORTD,PORTC
A                      *
A FB30 8D72                     BSR       PORTST3               CHECK FOR $AA
A FB32 AA3C                     FCB       $AA,$3C
A FB34 10081003                 FDB       PORTD,PORTC
A                      *
A FB38 8D6A                     BSR       PORTST3               CHECK FOR $55
A FB3A 553C                     FCB       $55,$3C
A FB3C 10081003                 FDB       PORTD,PORTC
A                      *
A FB40 8D62                     BSR       PORTST3               CHECK FOR $00
A FB42 003C                     FCB       $00,$3C
A FB44 10081003                 FDB       PORTD,PORTC
A                      *
A FB48 7F1009                   CLR       DDRD
A                      *
```

```
586 A                     *************************************************************** **************
587 A                     * T3b    TEST PORTA O/P TO PORTC I/P IN DIGITAL MODE
588 A                     *************************************************************** **************
589 A                     *
590 A                     *    FORMAT:
591 A                     *        BSR       PORTST
592 A                     *        FCB       DATA,MASK
593 A                     *        FDB       O/P PORT, I/P PORT
594 A                     *
595 A FB4B 86E0                     LDAA      #$E0
596 A FB4D B71004                   STAA      PORTB
597 A FB50 8688                     LDAA      #$88
598 A FB52 B71026                   STAA      PACTL
599 A                     *
600 A FB55 8D4D                     BSR       PORTST3               CHECK FOR $FF
601 A FB57 FFF8                     FCB       $FF,$F8
602 A FB59 10001003                 FDB       PORTA,PORTC
603 A                     *
604 A FB5D 8D45                     BSR       PORTST3               CHECK FOR $AA
605 A FB5F AAF8                     FCB       $AA,$F8
606 A FB61 10001003                 FDB       PORTA,PORTC
607 A                     *
608 A FB65 8D3D                     BSR       PORTST3               CHECK FOR $55
609 A FB67 55F8                     FCB       $55,$F8
610 A FB69 10001003                 FDB       PORTA,PORTC
611 A                     *
612 A FB6D 8D35                     BSR       PORTST3               CHECK FOR $00
613 A FB6F 00F8                     FCB       $00,$F8
614 A FB71 10001003                 FDB       PORTA,PORTC
615 A                     *
616 A FB75 7F1026                   CLR       PACTL
617 A                     *
618 A                     *************************************************************** **************
619 A                     *         FINALLY
620 A                     *
621 A                     *         THIS ROUTINE RETURNS THE PASS/FAIL STATUS TO THE MASTER
622 A                     *
623 A FB78 18FE1000       FINAL3    LDY       $1000
624 A FB7C 7F102C                   CLR       SCCR1
625 A FB7F 8630                     LDAA      #$30
626 A FB81 B7102B                   STAA      BAUD
627 A FB84 181C2D08                 BSET      SCCR2-$1000,Y,#$08    ENABLE TRANSMITTER
628 A FB88 B6102E                   LDAA      SCSR                  CLEAR FLAGS
629 A FB8B 96F9                     LDAA      PASFLG
630 A FB8D B7102F                   STAA      SCDR                  PASS/FAIL BYTE IN TRANSMITTER
631 A                     *
632 A FB90 8150                     CMPA      #$50
633 A FB92 2683                     BNE       T31                   LOOP IF YOU FAILED FOR DEBUG
634 A                     *
635 A                     *************************************************************** **************
636 A                     *
637 A FB94 86C0                     LDAA      #$C0                  ALL LEDS OFF
638 A FB96 C6C7                     LDAB      #$C7                  ALL LEDS ON
639 A FB98 F71004         P04       STAB      PORTB
640 A FB9B 8D2F                     BSR       DELAY3
641 A FB9D B71004                   STAA      PORTB
642 A FBA0 8D2A                     BSR       DELAY3
643 A FBA2 20D4                     BRA       FINAL3
644 A                     *
645 A                     *************************************************************** **************
646 A                     *       SUBROUTINES
647 A                     *************************************************************** **************
648 A                     *
649 A                     *       SUBROUTINE PORTST
650 A                     *
651 A FBA4 38             PORTST3   PULX
652 A FBA5 A600                     LDAA      $0,X                  LOAD ACC A WITH O/P DATA
653 A FBA7 1AEE02                   LDY       $2,X                  CONFIGURE O/P PORT
654 A FBAA 18A700                   STAA      $0,Y
655 A FBAD 1AEE04                   LDY       $4,X                  SET-UP I/P PORT ADDRESS
656 A FBB0 18A800                   EORA      $0,Y                  COMPARE O/P AND I/P
657 A FBB3 A401                     ANDA      $1,X                  MASK OUT DONT CARES
658 A FBB5 2713                     BEQ       A14                   EXIT IF PASS
659 A                     *
```

```
660 A                    *         IF FAILED THEN.....
661 A                    *
662 A FBB7 8646                    LDAA     #$46                ASCII 'F'
663 A FBB9 97F9                    STAA     PASFLG
664 A FBBB DFFB                    STX      TEMP1
665 A FBBD CE1000                  LDX      #$1000
666 A FBC0 1C0408                  BSET     PORTB-$1000,X,#$08  FAIL PULSE OF 11 E CLOCKS
667 A FBC3 01                      NOP
668 A FBC4 01                      NOP
669 A FBC5 1D0408                  BCLR     PORTB-$1000,X,#$08
670 A FBC8 DEFB                    LDX      TEMP1
671 A                    *
672 A FBCA 6E06          A14       JMP      $6,X                CONTINUE MAIN PROGRAM
673 A                    *
674 A                    ****************************************************************** **************
675 A                    *
676 A                    *         SUBROUTINE DELAY
677 A                    *
678 A FBCC 18CE0001      DELAY3    LDY      #$0001              SETS THE FLASH RATE
679 A FBD0 CEFFFF        D03       LDX      #$FFFF
680 A FBD3 09            D13       DEX
681 A FBD4 26FD                    BNE      D13
682 A FBD6 1809                    DEY
683 A FBD8 26F6                    BNE      D03
684 A FBDA 39                      RTS
685 A                    *
686 A                    ****************************************************************** **************
687 A FBDB                         INCL     T4.SA
688 A                    ****************************************************************** ***************
689 A                    * T4   TEST A/D DRIVEN FROM PORT B
690 A                    ****************************************************************** ***************
691 A                    *
692 A       0000         ZMIN      EQU      $00                 0%       2%+2BIT ACCURACY
693 A       0008         ZMAX      EQU      $08
694 A       00FF         FSMAX     EQU      $FF                 100%
695 A       00F8         FSMIN     EQU      $F8
696 A       00CA         HIMAX     EQU      $CA                 75%
697 A       00B9         HIMIN     EQU      $B9
698 A       0048         LOMAX     EQU      $48                 25%
699 A       0037         LOMIN     EQU      $37
700 A                    *
701 A                    *    FORMAT:
702 A                    *         BSR      ADTST
703 A                    *         FCB      O/P DATA, CHANNELS, MINVAL, MAXVAL
704 A                    *
705 A       FCF8                   ORG      $FCF8
706 A FCF8 0450000000              FCB      $04,$50,$00,$00,$00,$00,$00,$00RESERVED BYTES
        000000
707 A                    *
708 A       FC00                   ORG      $FC00
709 A FC00 8E00F7        T4        LDS      #$F7                PLACE STACK BELOW VECTORS AND RMB
710 A FC03 8690                    LDAA     #$90
711 A FC05 B71039                  STAA     OPTION              TURN A/D ON
712 A                    *
713 A FC08 8D69                    BSR      ADTST
714 A FC0A 00100008                FCB      $00,$10,ZMIN,ZMAX
715 A                    *
716 A FC0E 8D63                    BSR      ADTST
717 A FC10 00140008                FCB      $00,$14,ZMIN,ZMAX
718 A                    *
719 A FC14 8D5D                    BSR      ADTST
720 A FC16 FF10F8FF                FCB      $FF,$10,FSMIN,FSMAX
721 A                    *
722 A FC1A 8D57                    BSR      ADTST
723 A FC1C FF14F8FF                FCB      $FF,$14,FSMIN,FSMAX
724 A                    *
725 A FC20 8D51                    BSR      ADTST
726 A FC22 0F10B9CA                FCB      $0F,$10,HIMIN,HIMAX
727 A                    *
728 A FC26 8D4B                    BSR      ADTST
729 A FC28 0F143748                FCB      $0F,$14,LOMIN,LOMAX
730 A                    *
731 A FC2C 8D45                    BSR      ADTST
732 A FC2E F0103748                FCB      $F0,$10,LOMIN,LOMAX
733 A                    *
```

```
734 A FC32 8D3F                 BSR      ADTST
735 A FC34 F014B9CA             FCB      $F0,$14,HIMIN,HIMAX
736 A                  *
737 A                  *************************************************************** **************
738 A                  *        FINALLY
739 A                  *
740 A                  *        THIS ROUTINE RETURNS THE PASS/FAIL STATUS TO THE MASTER
741 A                  *
742 A FC38 18FE1000    FINAL4   LDY      $1000
743 A FC3C 7F102C               CLR      SCCR1
744 A FC3F 8630                 LDAA     #$30
745 A FC41 B7102B               STAA     BAUD
746 A FC44 181C2D08             BSET     SCCR2-$1000,Y,#$08    ENABLE TRANSMITTER
747 A FC48 B6102E               LDAA     SCSR                  CLEAR FLAGS
748 A FC4B 96F9                 LDAA     PASFLG
749 A FC4D B7102F               STAA     SCDR                  PASS/FAIL BYTE IN TRANSMITTER
750 A                  *
751 A FC50 8150                 CMPA     #$50
752 A FC52 26AC                 BNE      T4                    LOOP IF YOU FAILED FOR DEBUG
753 A                  *
754 A                  *************************************************************** **************
755 A                  *
756 A FC54 86C0                 LDAA     #$C0                  ALL LEDS OFF
757 A FC56 C6C7                 LDAB     #$C7                  ALL LEDS ON
758 A FC58 F71004               STAB     PORTB
759 A FC5B 8D07                 BSR      DELAY4
760 A FC5D B71004               STAA     PORTB
761 A FC60 8D02                 BSR      DELAY4
762 A FC62 20D4                 BRA      FINAL4
763 A                  *
764 A                  *************************************************************** **************
765 A                  *      SUBROUTINES
766 A                  *************************************************************** **************
767 A                  *
768 A                  *        SUBROUTINE DELAY
769 A                  *
770 A FC64 18CE0001    DELAY4   LDY      #$0001                SETS THE FLASH RATE
771 A FC68 CEFFFF      D04      LDX      #$FFFF
772 A FC6B 09          D14      DEX
773 A FC6C 26FD                 BNE      D14
774 A FC6E 1809                 DEY
775 A FC70 26F6                 BNE      D04
776 A FC72 39                   RTS
777 A                  *
778 A                  *************************************************************** **************
779 A                  *
780 A                  *      SUBROUTINE ADTST
781 A                  *
782 A FC73 38          ADTST    PULX                           FIND INDEX FOR VARIABLES
783 A FC74 A600                 LDAA     $0,X                  LOAD DRIVE DATA IN PORT B
784 A FC76 B71004               STAA     PORTB
785 A FC79 18CE0010             LDY      #$10                  PAUSE FOR VOLTAGE STABALISATION
786 A FC7D 1809        ADP      DEY
787 A FC7F 26FC                 BNE      ADP
788 A                  *
789 A FC81 A601                 LDAA     $1,X                  CONFIG ADCTL FOR CHANNEL SELECT
790 A FC83 B71030               STAA     ADCTL
791 A FC86 A602                 LDAA     $2,X                  LOAD ACC A WITH MIN LIMIT
792 A FC88 E603                 LDAB     $3,X                  LOAD ACC B WITH MAX LIMIT
793 A FC8A 18CE1031             LDY      #ADR1                 LOAD Y REG WITH FIRST RESULT REG ADDRESS
794 A FC8E 3C                   PSHX
795 A FC8F CE1000               LDX      #$1000
796 A FC92 1F3080FC             BRCLR    ADCTL-$1000,X,#$80,*  WAIT FOR CONV. COMPLETE
797 A                  *
798 A FC96 18A100      AD0      CMPA     $0,Y                  COMPARE RESULT WITH MIN AND MAX
799 A FC99 2304                 BLS      AD1                   BRANCH IF MIN(ACCA) < RESULT
800 A FC9B 8646                 LDAA     #$46
801 A FC9D 97F9                 STAA     PASFLG                'F' IN PASFLG IF FAILED
802 A FC9F 18E100      AD1      CMPB     $0,Y
803 A FCA2 2404                 BHS      AD2                   BRANCH IF MAX(ACCB) > RESULT
804 A FCA4 8646                 LDAA     #$46
805 A FCA6 97F9                 STAA     PASFLG                'F' IN PASFLG IF FAILED
806 A FCA8 188C1034    AD2      CPY      #ADR4                 CHECK ALL FOUR RESULT REGISTERS
807 A FCAC 2704                 BEQ      AD3
808 A FCAE 1808                 INY
```

```
A FCB0 20E4                BRA     AD0
A FCB2 38         AD3      PULX
A FCB3 6E04                JMP     $4,X                 CONTINUE MAIN PROGRAM
A                 *
A                 ************************************************************** ***************
A FCB5                     INCL    T5.SA
A                 ************************************************************** **************
A                 * T5     TEST IRQ, XIRQ
A                 ************************************************************** **************
A                 *    THIS TEST IS PERFORMED BY CLEARING ALL PENDING INTERRUPTS
A                 *    AND THEN PULLING THE APPROPRIATE PORT B PIN LOW TO GENERATE
A                 *    THE INTERRUPT. IF THE INTERRUPT OCCURS CORRECTLY THE
A                 *    PROGRAM WILL JUMP OVER THE INSTRUCTION WHICH FORCES A FAIL.
A                 *
A      00B8                ORG     $B8
P 00B8 0001       TSTNUM5  RMB     1
P 00B9 0001       PASFLG5  RMB     1
P 00BA 0001       IRQVAL   RMB     1
P 00BB 0001       IRQBAD   RMB     1
P 00BC 0001       XIRVAL   RMB     1
P 00BD 0001       XIRBAD   RMB     1
P 00BE 0001       TEMP15   RMB     1
A                 *
A      FD00                ORG     $FD00
A FD00 8E00B7     T5       LDS     #$B7                 PLACE STACK BELOW VECTORS AND RMB
A FD03 86C0                LDAA    #$C0
A FD05 B71004              STAA    PORTB                HOLD IRQ/XIRQ HIGH
A FD08 8D70                BSR     DELAY5
A                 *
A                 *        IRQ TEST
A                 *
A FD0A CE1000              LDX     #$1000
A                 *        CLR PENDING INTERRUPTS BY EXECUTING DUMMY INTERRUPT AFTER
A                 *        THE CLI AND CHECKING THE IRQVAL FLAG IN THE IRQ ROUTINE
A FD0D 0E                  CLI                          CLEAR THE MASK
A FD0E 14BAFF              BSET    IRQVAL,#$FF          ENABLE VALID INTERRUPTS
A FD11 13BBFF02            BRCLR   IRQBAD,#$FF,I1       CHECK FOR IRQ STUCK LOW
A FD15 8D4F                BSR     FAIL5                FORCES A FAIL IF IRQ IS LOW
A FD17 1D0480     I1       BCLR    PORTB-$1000,X,#$80   GENERATE VALID INT (PB7)
A FD1A 01                  NOP                          WAIT FOR IT !
A FD1B 12BBFF02            BRSET   IRQBAD,#$FF,I2
A FD1F 8D45                BSR     FAIL5                JUMP THIS IF INTERRUPT OCCURS
A FD21 01         I2       NOP
A                 *
A                 *        XIRQ TEST
A                 *
A FD22 07                  TPA                          CHANGE THE X BIT IN THE CC TO
A FD23 84BF                ANDA    #$BF                 ENABLE XIRQ INTERRUPTS.
A FD25 06                  TAP
A                 *        CLR PENDING INTERRUPTS
A FD26 14BCFF              BSET    XIRVAL,#$FF          ENABLE VALID INTERRUPT
A FD29 13BDFF02            BRCLR   XIRBAD,#$FF,XI1      CHECK IF XIRQ IS STUCK LOW
A FD2D 8D37                BSR     FAIL5                FORCE A FAIL IF LOW
A FD2F 1D0440     XI1      BCLR    PORTB-$1000,X,#$40   GENERATE VALID XIRQ (PB6)
A FD32 01                  NOP                          WAIT FOR IT !
A FD33 12BDFF02            BRSET   XIRBAD,#$FF,XI2
A FD37 8D2D                BSR     FAIL5                SKIP THIS IF XIRQ OCCURS
A FD39 01         XI2      NOP
A                 *
A                 *
A                 ************************************************************** **************
A                 *        FINALLY
A                 *
A                 *        THIS ROUTINE RETURNS THE PASS/FAIL STATUS TO THE MASTER
A                 *
A FD3A 18FE1000   FINAL5   LDY     $1000
A FD3E 7F102C              CLR     SCCR1
A FD41 8630                LDAA    #$30
A FD43 B7102B              STAA    BAUD
A FD46 181C2D08            BSET    SCCR2-$1000,Y,#$08   ENABLE TRANSMITTER
A FD4A B6102E              LDAA    SCSR                 CLEAR FLAGS
A FD4D 96B9                LDAA    PASFLG5
A FD4F B7102F              STAA    SCDR                 PASS/FAIL BYTE IN TRANSMITTER
A                 *
```

```
883 A FD52 8150                CMPA     #$50
884 A FD54 26E4                BNE      FINAL5              LOOP IF YOU FAILED
885 A                    *
886 A                    *************************************************************** **************
887 A                    *
888 A FD56 86C0                LDAA     #$C0                ALL LEDS OFF
889 A FD58 C6C7                LDAB     #$C7                ALL LEDS ON
890 A FD5A F71004        P05   STAB     PORTB
891 A FD5D 8D1B                BSR      DELAY5
892 A FD5F B71004              STAA     PORTB
893 A FD62 8D16                BSR      DELAY5
894 A FD64 20D4                BRA      FINAL5
895 A                    *
896 A                    *************************************************************** **************
897 A                    *     SUBROUTINES
898 A                    *************************************************************** **************
899 A                    *
900 A                    *         SUBROUTINE FAIL
901 A                    *
902 A FD66 8646          FAIL5     LDAA     #$46
903 A FD68 97B9                    STAA     PASFLG5             LOAD 'F' IN PASFLG
904 A FD6A DFBE                    STX      TEMP15
905 A FD6C CE1000                  LDX      #$1000
906 A FD6F 1C0408                  BSET     PORTB-$1000,X,#$08  FAIL PULSE OF 11 E CLOCKS
907 A FD72 01                      NOP
908 A FD73 01                      NOP
909 A FD74 1D0408                  BCLR     PORTB-$1000,X,#$08
910 A FD77 DEBE                    LDX      TEMP15
911 A FD79 39                      RTS
912 A                    *
913 A                    *************************************************************** **************
914 A                    *
915 A                    *         SUBROUTINE DELAY
916 A                    *
917 A FD7A 18CE0001      DELAY5    LDY      #$0001              SETS THE FLASH RATE
918 A FD7E CEFFFF        D05       LDX      #$FFFF
919 A FD81 09            D15       DEX
920 A FD82 26FD                    BNE      D15
921 A FD84 1809                    DEY
922 A FD86 26F6                    BNE      D05
923 A FD88 39                      RTS
924 A                    *
925 A                    *************************************************************** **************
926 A                    *     INTERUPT ROUTINES
927 A                    *************************************************************** **************
928 A                    *
929 A                    *         IRQ ROUTINE
930 A                    *
931 A FD89 12BAFF04      IRQ       BRSET    IRQVAL,#$FF,IR1     CHECK IF INT IS VALID
932 A FD8D 14BAFF                  BSET     IRQVAL,#$FF         SET FLAG SO NEXT INT IS VALID
933 A FD90 3B                      RTI
934 A FD91 1C0480        IR1       BSET     PORTB-$1000,X,#$80  SET PORTB7 HIGH AGAIN
935 A FD94 14BBFF                  BSET     IRQBAD,#$FF
936 A FD97 1830                    TSY                          LOAD STACK POINTER INTO Y
937 A FD99 181C0010                BSET     $0,Y,#$10           SET INT MASK WHILE STILL ON..
938 A FD9D 3B                      RTI                          ..THE STACK AND RETURN.
939 A                    *
940 A                    *************************************************************** **************
941 A                    *
942 A                    *         XIRQ ROUTINE
943 A                    *
944 A FD9E 12BCFF04      XIRQ      BRSET    XIRVAL,#$FF,XIR1    CHECK IF INT IS VALID
945 A FDA2 14BCFF                  BSET     XIRVAL,#$FF         SET FLAG SO NEXT INT IS VALID
946 A FDA5 3B                      RTI
947 A FDA6 1C0440        XIR1      BSET     PORTB-$1000,X,#$40  SET PB6 HIGH AGAIN
948 A FDA9 14BDFF                  BSET     XIRBAD,#$FF
949 A FDAC 3B                      RTI
950 A                    *
951 A                    *************************************************************** **************
952 A                    *
953 A      FDB8                    ORG      $FDB8
954 A FDB8 0550000000              FCB      $05,$50,$00,$00,$00,$00,$00,$00RESERVED BYTES
           000000
955 A                    *
956 A      FDC4                    ORG      $FDC4
```

```
 957 A FDC4 7E0000             JMP      $0000              SCI
 958 A FDC7 7E0000             JMP      $0000              SPI
 959 A FDCA 7E0000             JMP      $0000              PULSE ACC I/P
 960 A FDCD 7E0000             JMP      $0000              PULSE ACC OVFL
 961 A FDD0 7E0000             JMP      $0000              TIMER OVFL
 962 A FDD3 7E0000             JMP      $0000              O/P COMP 5
 963 A FDD6 7E0000             JMP      $0000              O/P COMP 4
 964 A FDD9 7E0000             JMP      $0000              O/P COMP 3
 965 A FDDC 7E0000             JMP      $0000              O/P COMP 2
 966 A FDDF 7E0000             JMP      $0000              O/P COMP 1
 967 A FDE2 7E0000             JMP      $0000              I/P CAPT 3
 968 A FDE5 7E0000             JMP      $0000              I/P CAPT 2
 969 A FDE8 7E0000             JMP      $0000              I/P CAPT 1
 970 A FDEB 7E0000             JMP      $0000              REAL TIM INT
 971 A FDEE 7E0089             JMP      IRQ-$FD00          IRQ
 972 A FDF1 7E009E             JMP      XIRQ-$FD00         XIRQ
 973 A FDF4 7E0000             JMP      $0000              SWI
 974 A FDF7 7E0000             JMP      $0000              ILLEGAL OPCODE
 975 A FDFA 7E0000             JMP      $0000              COP
 976 A FDFD 7E0000             JMP      $0000              CLOCK MONITOR
 977 A                   *
 978 A                   ****************************************************************************
 979 A FE00                    INCL     T6.SA
 980 A                   *******************************************************************************
 981 A                   * T6     TEST EEPROM
 982 A                   *********************************************************************************
 983 A                   *   THIS TEST PROGRAMS THE 512 BYTES OF INTERNAL EEPROM AND
 984 A                   *   CHECKS FOR ERASURE ($FF), CHECKERBOARD AND $00. THE PROGRAMMING
 985 A                   *   TIME IS SET BY SUBROUTINE 'EEDEL' TO 10MS SO EACH PROGRAMMING
 986 A                   *   CYCLE OF 512 BYTES TAKES APPROX 5 SECONDS (15 SEC TOTAL).
 987 A                   *
 988 A                   *       FORMAT:
 989 A                   *       BSR      EEPROG
 990 A                   *       FCB      $XX,$YY           $XX - DATA FOR FIRST 32 BYTES
 991 A                   *                                 $YY - DATA FOR NEXT  32 BYTES
 992 A                   *
 993 A      00FA         TSTNUM6  EQU     $FA
 994 A      00FB         PASFLG6  EQU     $FB
 995 A      00FC         TEMP6    EQU     $FC
 996 A      00FD         TEMP16   EQU     $FD
 997 A      00FE         DUMMY6   EQU     $FE
 998 A      00FF         COUNT6   EQU     $FF
 999 A                   *
1000 A      FEFA                  ORG     $FEFA
1001 A FEFA 0600000000            FCB     $06,$00,$00,$00,$00,$00RESERVED BYTES
            00
1002 A                   *
1003 A      FE00                  ORG     $FE00
1004 A FE00 8E00F9       T6       LDS     #$F9               PLACE STACK BELOW VECTORS AND RMB
1005 A FE03 7F1035                CLR     BPROT
1006 A FE06 8650                  LDAA    #$50
1007 A FE08 97FB                  STAA    PASFLG6            INITIALISE PASS FLAG
1008 A FE0A 86C0                  LDAA    #$C0
1009 A FE0C B71004                STAA    PORTB              BLANK LED'S
1010 A                   *
1011 A FE0F 8D2C                  BSR     BULKE              BULK ERASE THE EEPROM
1012 A FE11 8D6C                  BSR     EEPROG             PROGRAM WITH CHECKERBOARD
1013 A FE13 AA55                  FCB     $AA,$55
1014 A                   *
1015 A FE15 8D26                  BSR     BULKE              BULK ERASE
1016 A FE17 8D66                  BSR     EEPROG             INVERSE CHECKERBOARD
1017 A FE19 55AA                  FCB     $55,$AA
1018 A                   *
1019 A FE1B 8D20                  BSR     BULKE              BULK ERASE
1020 A FE1D 8D60                  BSR     EEPROG             PROGRAM ALL ZERO'S
1021 A FE1F 0000                  FCB     $00,$00
1022 A                   *
1023 A FE21 8D1A                  BSR     BULKE              ERASE AGAIN BEFORE FINISHED
1024 A                   *
```

```
                  ************************************************************* **************
                  *         FINALLY
                  *
                  *         THIS ROUTINE RETURNS THE PASS/FAIL STATUS TO THE MASTER
                  *
FE23 18FE1000     FINAL6    LDY       $1000
FE27 7F102C                 CLR       SCCR1
FE2A 8630                   LDAA      #$30
FE2C B7102B                 STAA      BAUD
FE2F 181C2D08               BSET      SCCR2-$1000,Y,#$08    ENABLE TRANSMITTER
FE33 B6102E                 LDAA      SCSR                  CLEAR FLAGS
FE36 96FB                   LDAA      PASFLG6
FE38 B7102F                 STAA      SCDR                  PASS/FAIL BYTE IN TRANSMITTER
FE3B 20E6                   BRA       FINAL6
                  *
                  ************************************************************* **************
                  *        SUBROUTINES
                  ************************************************************* **************
                  *
                  *        SUBROUTINE BULK ERASE
                  *
FE3D 18CE0006     BULKE     LDY       #$0006
FE41 18FF103A               STY       PPROG-1
FE45 7FB600                 CLR       EEPROM
FE48 18CE0007               LDY       #$0007
FE4C 18FF103A               STY       PPROG-1
FE50 8D18                   BSR       EEDEL
                  *
FE52 18CE0006               LDY       #$0006
FE56 18FF103A               STY       PPROG-1
FE5A 7F103B                 CLR       PPROG
                  *
FE5D CEB600       VERFE     LDX       #EEPROM
FE60 86FF                   LDAA      #$FF
FE62 8D78         V1        BSR       EEV
FE64 8CB800                 CPX       #EETOP
FE67 26F9                   BNE       V1
FE69 39                     RTS
                  *
                  ************************************************************* **************
                  *
                  *        SUBROUTINE EEPROM PROGRAM DELAY
                  *
FE6A 18CE0B29     EEDEL     LDY       #$0B29                10MS PROGRAMMING DELAY
FE6E 1809         EED1      DEY
FE70 26FC                   BNE       EED1
FE72 18CE1000               LDY       #$1000
FE76 181C0401               BSET      PORTB-$1000,Y,#$01
FE7A 181D0401               BCLR      PORTB-$1000,Y,#$01
FE7E 39                     RTS
                  *
                  ************************************************************* **************
                  *
                  *        SUBROUTINE EEPROM PROG/VERF
                  *
FE7F 38           EEPROG    PULX
FE80 A600                   LDAA      $0,X
FE82 E601                   LDAB      $1,X
FE84 08                     INX
FE85 08                     INX
FE86 3C                     PSHX
FE87 7F103B                 CLR       PPROG
FE8A CEB600                 LDX       #EEPROM
FE8D 18CE0002               LDY       #$0002
FE91 18FF103A               STY       PPROG-1
                  *
FE95 8D23         EE1       BSR       EEP                   PROG FIRST 32 BYTES
FE97 97FD                   STAA      TEMP16
FE99 17                     TBA
FE9A 8D1E                   BSR       EEP                   PROG NEXT 32 BYTES
FE9C 16                     TAB
FE9D 96FD                   LDAA      TEMP16
                  *
FE9F 8CB800                 CPX       #EETOP
FEA2 26F1                   BNE       EE1                   REPEAT FOR ALL 256 BYTES
```

```
1100 A FEA4 7F103B                CLR     PPROG
1101 A                     *
1102 A FEA7 CEB600   EEVERF       LDX     #EEPROM              VERIFY DATA IS CORRECT
1103 A                     *
1104 A FEAA 8D30     EE3          BSR     EEV                  VERIFY FIRST 32 BYTES
1105 A FEAC 97FD                  STAA    TEMP16
1106 A FEAE 17                    TBA
1107 A FEAF 8D2B                  BSR     EEV                  VERIFY NEXT 32 BYTES
1108 A FEB1 16                    TAB
1109 A FEB2 96FD                  LDAA    TEMP16
1110 A                     *
1111 A FEB4 8CB800                CPX     #EETOP
1112 A FEB7 26F1                  BNE     EE3                  REPEAT FOR ALL 256 BYTES
1113 A FEB9 39                    RTS
1114 A                     *
1115 A                     ************************************************************ ***********
1116 A                     *
1117 A                     *        SUBROUTINE EEPROM PROGRAM
1118 A                     *
1119 A FEBA 18CE0020 EEP          LDY     #$20                 PROG 32 BYTES FROM ACCA
1120 A FEBE 18DFFE                STY     COUNT6-1
1121 A FEC1 A700     EE2          STAA    $0,X
1122 A FEC3 18CE0003              LDY     #$0003
1123 A FEC7 18FF103A              STY     PPROG-1
1124 A FECB 8D9D                  BSR     EEDEL
1125 A                     *
1126 A FECD 18CE0002              LDY     #$0002
1127 A FED1 18FF103A              STY     PPROG-1
1128 A FED5 08                    INX
1129 A FED6 7A00FF                DEC     COUNT6
1130 A FED9 26E6                  BNE     EE2
1131 A FEDB 39                    RTS
1132 A                     *
1133 A                     ************************************************************ ************
1134 A                     *
1135 A                     *        SUBROUTINE EEPROM VERIFY
1136 A                     *
1137 A FEDC 18CE0020 EEV          LDY     #$20                 VERIFY 32 BYTES
1138 A FEE0 A100     EEV1         CMPA    $0,X
1139 A FEE2 2704                  BEQ     EEV2
1140 A FEE4 8646                  LDAA    #$46
1141 A FEE6 97FB                  STAA    PASFLG6
1142 A FEE8 08       EEV2         INX
1143 A FEE9 1809                  DEY
1144 A FEEB 26F3                  BNE     EEV1
1145 A FEED 39                    RTS
1146 A                     *
1147 A                     ************************************************************ **************
1148 A
1149 A FEEE                       INCL    T7.SA
1150 A                     ************************************************************ **************
1151 A                     * T7       TEST STRA - PORTCL I/P STROBE
1152 A                     ************************************************************ **************
1153 A                     *
1154 A                     *          PORTC IS CONFIGURED AS AN I/P EXCEPT FOR PORTC6 WHICH IS
1155 A                     *          USED TO DRIVE THE STRA I/P. ONLY BITS 2-5 ARE CARED.
1156 A                     *
1157 A                     *     FORMAT:
1158 A                     *          BSR     PORTST
1159 A                     *          FCB     DATA, MASK
1160 A                     *          FDB     O/P PORT,I/P PORT
1161 A                     *
1162 A                     *
1163 A      00B8                      ORG     $B8
1164 P 00B8 0001     TSTNUM7      RMB     1
1165 P 00B9 0001     PASFLG7      RMB     1
1166 P 00BA 0001     TEMP7        RMB     1
1167 P 00BB 0001     TEMP17       RMB     1
1168 A                     *
1169 A      FFB8                      ORG     $FFB8
1170 A FFB8 0750000000                FCB     $07,$50,$00,$00,$00,$00,$00,$00RESERVED BYTES
            000000
1171 A                     *
```

```
A      FF00                   ORG      $FF00
A FF00 8E00B7      T7         LDS      #$B7                 PLACE STACK BELOW VECTORS AND RMB
A FF03 8D6D                   BSR      DELAY7
A                  *
A FF05 7F1008                 CLR      PORTD
A FF08 8604                   LDAA     #$04                 CONFIGURE PORTD IN CMOS MODE
A FF0A B71028                 STAA     SPCR
A FF0D 8640                   LDAA     #$40                 CONFIG PORTC6 ONLY AS O/P
A FF0F B71007                 STAA     DDRC
A FF12 86FF                   LDAA     #$FF                 CONFIG PORTD AS O/P
A FF14 B71009                 STAA     DDRD
A                  *
A FF17 8D68                   BSR      PORTST7              CHECK FOR $00
A FF19 403C                   FCB      $40,$3C
A FF1B 10031005               FDB      PORTC,PORTCL
A FF1F 7F1003                 CLR      PORTC
A FF22 86FF                   LDAA     #$FF
A FF24 B71008                 STAA     PORTD
A                  *
A FF27 8D58                   BSR      PORTST7              CHECK FOR $FF
A FF29 FF3C                   FCB      $FF,$3C
A FF2B 10031005               FDB      PORTC,PORTCL
A FF2F 7F1003                 CLR      PORTC
A FF32 7F1008                 CLR      PORTD
A                  *
A FF35 8D4A                   BSR      PORTST7              CHECK FOR $00
A FF37 403C                   FCB      $40,$3C
A FF39 10031005               FDB      PORTC,PORTCL
A FF3D 7F1003                 CLR      PORTC
A FF40 7F1007                 CLR      DDRC
A FF43 7F1009                 CLR      DDRD
A                  *
A                  *
A                  ************************************************************ **************
A                  *          FINALLY
A                  *
A                  *          THIS ROUTINE RETURNS THE PASS/FAIL STATUS TO THE MASTER
A                  *
A FF46 18FE1000    FINAL7     LDY      $1000
A FF4A 7F102C                 CLR      SCCR1
A FF4D 8630                   LDAA     #$30
A FF4F B7102B                 STAA     BAUD
A FF52 181C2D08               BSET     SCCR2-$1000,Y,#$08   ENABLE TRANSMITTER
A FF56 B6102E                 LDAA     SCSR                 CLEAR FLAGS
A FF59 96B9                   LDAA     PASFLG7
A FF5B B7102F                 STAA     SCDR                 PASS/FAIL BYTE IN TRANSMITTER
A                  *
A FF5E 8150                   CMPA     #$50
A FF60 269E                   BNE      T7                   LOOP IF YOU FAILED FOR DEBUG
A                  *
A                  ************************************************************ ***************
A                  *
A FF62 86C0                   LDAA     #$C0                 ALL LEDS OFF
A FF64 C6C7                   LDAB     #$C7                 ALL LEDS ON
A FF66 F71004      P07        STAB     PORTB
A FF69 8D07                   BSR      DELAY7
A FF6B B71004                 STAA     PORTB
A FF6E 8D02                   BSR      DELAY7
A FF70 20D4                   BRA      FINAL7
A                  *
A                  ************************************************************ **************
A                  *        SUBROUTINES
A                  ************************************************************ **************
A                  *
A                  *          SUBROUTINE DELAY
A                  *
A FF72 18CE0001    DELAY7     LDY      #$0001               SETS THE FLASH RATE
A FF76 CEFFFF      D07        LDX      #$FFFF
A FF79 09          D17        DEX
A FF7A 26FD                   BNE      D17
A FF7C 1809                   DEY
A FF7E 26F6                   BNE      D07
A FF80 39                     RTS
A                  *
A                  ************************************************************ **************
```

```
1247 A                   *
1248 A                   *        SUBROUTINE PORTST
1249 A                   *
1250 A FF81 38           PORTST7    PULX
1251 A FF82 A600                    LDAA      $0,X                    LOAD ACC A WITH O/P DATA
1252 A FF84 1AEE02                  LDY       $2,X                    CONFIGURE O/P PORT
1253 A FF87 18A700                  STAA      $0,Y
1254 A FF8A 1AEE04                  LDY       $4,X                    SET-UP I/P PORT ADDRESS
1255 A FF8D 18A800                  EORA      $0,Y                    COMPARE O/P AND I/P
1256 A FF90 A401                    ANDA      $1,X                    MASK OUT DONT CARES
1257 A FF92 2713                    BEQ       A17                     EXIT IF PASS
1258 A                   *
1259 A                   *          IF FAILED THEN.....
1260 A                   *
1261 A FF94 8646                    LDAA      #$46                    ASCII 'F'
1262 A FF96 97B9                    STAA      PASFLG7
1263 A FF98 DFBB                    STX       TEMP17
1264 A FF9A CE1000                  LDX       #$1000
1265 A FF9D 1C0408                  BSET      PORTB-$1000,X,#$08      FAIL PULSE OF 11 E CLOCKS
1266 A FFA0 01                      NOP
1267 A FFA1 01                      NOP
1268 A FFA2 1D0408                  BCLR      PORTB-$1000,X,#$08
1269 A FFA5 DEBB                    LDX       TEMP17
1270 A                   *
1271 A FFA7 6E06         A17        JMP       $6,X                    CONTINUE MAIN PROGRAM
1272 A                   *
1273 A                   ************************************************************ **************
1274 A                   *
1275 A                   ************************************************************ **************
1276 A                              END

SYMBOL TABLE:  Total Entries=  178

A11                 F9AA     P07                  FF66
A12                 FAC0     PACC1                F932
A14                 FBCA     PACC2                F941
A17                 FFA7     PACNT                1027
AD0                 FC96     PACTL                1026
AD1                 FC9F     PASFLG               00F9
AD2                 FCA8     PASFLG5              00B9
AD3                 FCB2     PASFLG6              00FB
ADCTL               1030     PASFLG7              00B9
ADP                 FC7D     PAU01                F8E5
ADR1                1031     PAU02                F8E2
ADR2                1032     PAUSE                F8E1
ADR3                1033     PIOC                 1002
ADR4                1034     PORTA                1000
ADTST               FC73     PORTB                1004
ANSWER              F8C3     PORTC                1003
BAUD                102B     PORTCL               1005
BPROT               1035     PORTD                1008
BULKE               FE3D     PORTE                100A
CFORC               100B     PORTST1              F984
CONFIG              103F     PORTST2              FA9A
COPRST              103A     PORTST3              FBA4
COUNT               00FD     PORTST7              FF81
COUNT6              00FF     PPROG                103B
D01                 F9B0     RB                   1000
D02                 FAC6     REJECT               F8DA
D03                 FBD0     RESET                F800
D04                 FC68     S11                  F97C
D05                 FD7E     S12                  FA0F
D07                 FF76     S13                  FB0F
D11                 F9B3     SCCR1                102C
D12                 FAC9     SCCR2                102D
D13                 FBD3     SCDR                 102F
D14                 FC6B     SCSR                 102E
D15                 FD81     SPCR                 1028
D17                 FF79     SPDR                 102A
DDRC                1007     SPSR                 1029
DDRD                1009     STLWT                F8AA
DELAY1              F9AC     SYNC1                F972
DELAY2              FAC2     SYNC2                FA05
DELAY3              FBCC     SYNC3                FB05
DELAY4              FC64     T1                   F900
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DELAY5              FD7A     T2                   FA00
DELAY7              FF72     T21                  FA17
DUMMY               00FC     T3                   FB00
DUMMY6              00FE     T31                  FB17
EE1                 FE95     T4                   FC00
EE2                 FEC1     T5                   FD00
EE3                 FEAA     T6                   FE00
EED1                FE6E     T7                   FF00
EEDEL               FE6A     TCNT                 100E
EEP                 FEBA     TCTL1                1020
EEPROG              FE7F     TCTL2                1021
EEPROM              B600     TEMP                 00FA
EETOP               B800     TEMP1                00FB
EEV                 FEDC     TEMP15               00BE
EEV1                FEE0     TEMP16               00FD
EEV2                FEE8     TEMP17               00BB
EEVERF              FEA7     TEMP6                00FC
FAIL1               F9BB     TEMP7                00BA
FAIL5               FD66     TEST                 F87E
FINAL1              F946     TEST1                103E
FINAL2              FA66     TESTNUM              0000
FINAL3              FB78     TFLG1                1023
FINAL4              FC38     TFLG2                1025
FINAL5              FD3A     TIC1                 1010
FINAL6              FE23     TIC2                 1012
FINAL7              FF46     TIC3                 1014
FSMAX               00FF     TMSK1                1022
FSMIN               00F8     TMSK2                1024
HIMAX               00CA     TOC1                 1016
HIMIN               00B9     TOC2                 1018
HPRIO               103C     TOC3                 101A
I1                  FD17     TOC4                 101C
I2                  FD21     TOC5                 101E
INIT                103D     TSTNUM               00F8
IR1                 FD91     TSTNUM5              00B8
IRQ                 FD89     TSTNUM6              00FA
IRQBAD              00BB     TSTNUM7              00B8
IRQVAL              00BA     V1                   FE62
LOMAX               0048     VERFE                FE5D
LOMIN               0037     XI1                  FD2F
OC1D                100D     XI2                  FD39
OC1M                100C     XIR1                 FDA6
OPTION              1039     XIRBAD               00BD
P01                 F966     XIRQ                 FD9E
P02                 FA8E     XIRVAL               00BC
P04                 FB98     ZMAX                 0008
P05                 FD5A     ZMIN                 0000

Total errors: 0
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Printed in Great Britain by Tavistock Press (Bedford) Ltd. 3500 5/92 PO.2559