GETTING MORE VALUE OUT OF AN INTEGRATED OPERATIONAL AMPLIFIER DATA SHEET

Prepared by
Karl Huehne
Applications Engineering

The operational amplifier has become a basic building block in present day solid state electronic systems. The purpose of this application note is to provide a better understanding of the open loop characteristics of the amplifier and their significance to overall circuit operation. Also each parameter is defined and reviewed with respect to closed loop considerations. The importance of loop gain stability and bandwidth is discussed at length. Input offset voltage and current and resultant drift effects in the circuit are also reviewed with respect to closed loop operation.

MOTOROLA *Semiconductor Products Inc.*

GETTING MORE VALUE OUT OF AN INTEGRATED OPERATIONAL AMPLIFIER DATA SHEET

INTRODUCTION

Integrated circuit development previously concentrated upon digital devices that were more tolerant of monolithic limitations and more easily standardized for volume production than their linear counterparts. Improved process controls, better resultant yields and resourceful design techniques have now produced linear devices capable of matching or exceeding the conventional component designs. One such linear device, the operational amplifier, has become a "standard" or "universal" building block compatible with numerous circuit and system applications and the present integrated circuit technology.

The designation, "operational amplifier" was originally adopted for a series of high performance dc amplifiers used in analog computers. These amplifiers were used to perform mathematical operations applicable to analog computation such as summation, scaling, subtraction, integrating, etc. The application of operational amplifiers is so widely diversified now that this original terminology is inappropriate. In many electronic systems, the operational amplifier is used as a basic building block for phase shifting, filtering, signal conditioning, multiplexing, detecting, etc. And in many non-linear applications such as comparators, oscillators and multivibrators, the operational amplifier has proven competent.

The purpose of this application note is to provide the circuit designer with a better understanding of the basic operational amplifier open loop parameters and their significance to overall circuit operation. In this manner, maximum use can be made of the amplifiers with a minimum of design difficulties. Methodically, each operational amplifier characteristic appearing on a sample data sheet will be reviewed. First the parameter will be defined, and then the significance of the parameter and parameter magnitude upon overall closed loop operation of the amplifier will be discussed in detail. Liberal use will be made of all supplementary information contained on the data sheet in order to convey a maximum of information.

PARAMETERS

The data sheet used for the review and discussion of the operational amplifier parameters is that used for characterization of the Motorola MC1539 and MC1439 operational amplifiers. The absolute maximum ratings and schematic diagram of these devices are shown in Figure 1. It will suffice to say that if the maximum ratings of the device are exceeded, possible device damage could ensue and abnormal circuit operation observed.

Figure 2 contains the itemized parameter specifications that when used appropriately with supplementary informa-

tion will permit the designer to determine applicability and validity of his design equations to the overall design.

A short discussion on each of the more important parameters used to specify the performance of an operating amplifier will now follow.

OPEN LOOP VOLTAGE GAIN (A_{Vol}) is defined as the ratio of a change in output voltage to a change in voltage at the input terminals. Ideally, this parameter should be infinitely high since the primary function is to amplify and, in general, the higher the gain, the better the gain accuracy. However, there are practical limits to gain magnitude and also levels where an increase in magnitude buys little in the way of increased performance with respect to the price paid. The true significance of open loop gain is many times misapplied in amplifier operation where in reality open loop gain determines closed loop accuracy limits rather than the ultimate accuracy. Loop gain is really the primary determinent in amplifier closed loop operations. Referring to Figure 3, which contains a somewhat ideal operational amplifier, the closed loop gain of the circuit is

$$\frac{e_O}{e_S} = - \frac{A_{Vol} \left(\dfrac{R2}{R1 + R2} \right)}{1 + A_{Vol} \left(\dfrac{R1}{R1 + R2} \right)} . \qquad (1)$$

The form of Equation 1 is quite similar to the standard equation derived in basic feedback theory that reads

$$\frac{e_O}{e_S} = \frac{A_{Vol}}{1 + A_{Vol}\beta} . \qquad (2)$$

The exception being that the open loop gain in the numerator of Equation 1 is attenuated. This occurs because in the derivation of Equation 2 the assumption was made that forward signal transmission through the feedback element was negligible. The denominators of the Equations 1 and 2 are identical since the fraction of the output voltage feedback to the amplifier summing point is

$$\beta = \frac{R1}{R1 + R2}. \qquad (3)$$

The denominator product of Equation 1:

$\left(-A_{Vol} \dfrac{R1}{R1 + R2} \right)$ and Equation 2: $(-A_{Vol}\beta)$

is defined as the loop gain measured if the connection between the output of the amplifier and its load or feedback

resistor were broken and a signal inserted. The resultant signal measured at the amplifier open loop output terminal is therefore

$$\text{loop gain} = A_{vol} \frac{R1}{R1 + R2}. \qquad (4)$$

The significance of this parameter will manifest itself repeatedly in the ensuing discussions.

If the amplifier of Figure 3 exhibited infinite open loop gain, Equation 1 reduces to

$$\frac{e_O}{e_S} = -\frac{R2}{R1} \qquad (5)$$

the ratio of two passive elements, which is the ideal closed loop gain of an operational amplifier connected in this mode of operation. The error in closed loop gain of an amplifier then may be represented as

$$\%\epsilon_{CL} = \frac{\left.\dfrac{e_O}{e_S}\right|_{ideal} - \left.\dfrac{e_O}{e_S}\right|_{actual}}{\left.\dfrac{e_O}{e_S}\right|_{ideal}} \times 100 \qquad (6)$$

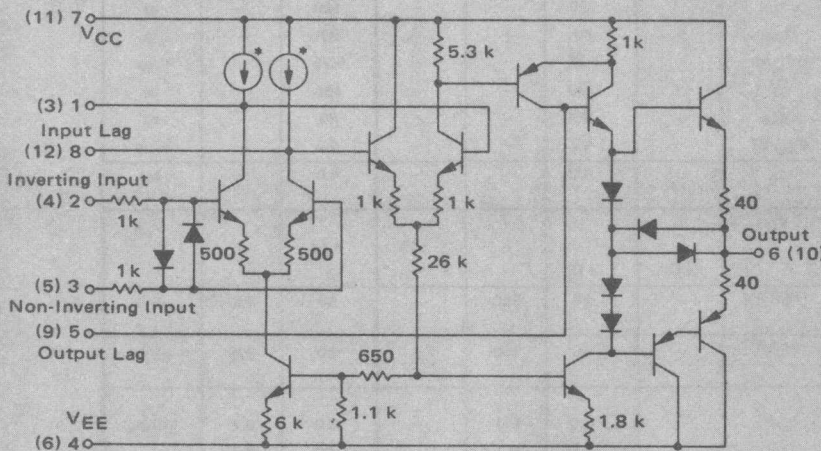which after insertion of Equations 1 and 5 reduces to

$$\%\epsilon_{CL} = \frac{100}{1 + A_{vol} \dfrac{R1}{R1 + R2}}. \qquad (7)$$

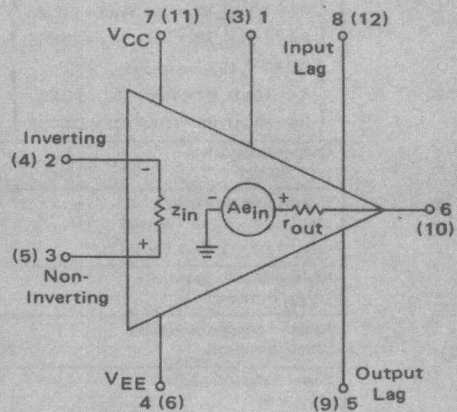The closed loop gain error is, therefore, a direct function

MAXIMUM RATINGS ($T_A = +25^{\circ}C$ unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	+18	Vdc
	V_{EE}	–18	Vdc
Differential Input Signal	V_{ID}	$\pm [V_{CC} + |V_{EE}|]$	Vdc
Common-Mode Input Swing	V_{ICR}	$+V_{CC}, -|V_{EE}|$	Vdc
Load Current	I_L	15	mA
Output Short Circuit Duration	t_S	Continuous	
Power Dissipation (Package Limitation)	P_D		
Metal Can		680	mW
Derate above $T_A = +25^{\circ}C$		4.6	mW/$^{\circ}$C
Ceramic Dual In-Line Package		750	mW
Derate above $T_A = +25^{\circ}C$		6.0	mW/$^{\circ}$C
Plastic Dual In-Line Package		625	mW
Derate above $T_A = +25^{\circ}C$		5.0	mW/$^{\circ}$C
Operating Temperature Range MC1539	T_A	–55 to +125	$^{\circ}$C
MC1439		0 to +75	
Storage Temperature Range	T_{stg}		$^{\circ}$C
Metal and Ceramic Packages		–65 to +150	
Plastic Package		–55 to +125	

CIRCUIT SCHEMATIC

EQUIVALENT CIRCUIT

Pin numbers adjacent to terminals apply to 8-pin package, numbers in parenthesis apply to 14-pin packages.
Pin 7 is electrically connected to the substrate and V_{EE} for Case 605 (plastic package) only.
*Patent pending.

FIGURE 1 — MC1539, MC1439 Data Sheet

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 Vdc, V_{EE} = –15 Vdc, T_A = +25°C unless otherwise noted)

Characteristic	Symbol*	MC1539			MC1439			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Bias Current	I_{IB}							µA
(T_A = +25°C)		–	0.20	0.50	–	0.20	1.0	
(T_A = T_{low} ①)		–	0.23	0.70	–	0.23	1.5	
Input Offset Current	$|I_{IO}|$							nA
(T_A = T_{low})		–	–	75	–	–	150	
(T_A = +25°C)		–	20	60	–	20	100	
(T_A = T_{high} ①)		–	–	75	–	–	150	
Input Offset Voltage	$|V_{IO}|$							mV
(T_A = +25°C)		–	1.0	3.0	–	2.0	7.5	
(T_A = T_{low}, T_{high})		–	–	4.0	–	–	–	
Average Temperature Coefficient of Input Offset Voltage (T_A = T_{low} to T_{high})	$|TC_{VIO}|$							µV/°C
(R_S = 50 Ω)		–	3.0	–	–	3.0	–	
($R_S \leq$ 10 kΩ)		–	5.0	–	–	5.0	–	
Input Impedance (f = 20 Hz)	z_{in}	150	300	–	100	300	–	kΩ
Input Common-Mode Voltage Swing	V_{ICR}	±11	±12	–	±11	±12	–	V_{pk}
Equivalent Input Noise Voltage (R_S = 10 kΩ, Noise Bandwidth = 1.0 Hz, f = 1.0 kHz)	$V_{N(in)}$	–	30	–	–	30	–	nV/(Hz)½
Common-Mode Rejection Ratio (f = 1.0 kHz)	CMRR	80	110	–	80	110	–	dB
Open-Loop Voltage Gain (V_O = ±10 V, R_L = 10 kΩ, R_5 = ∞) (T_A = +25°C to T_{high})	A_{vol}	50,000	120,000	–	15,000	100,000	–	–
(T_A = T_{low})		25,000	100,000	–	15,000	100,000	–	
Power Bandwidth (A_v = 1, THD $\leq$ 5%, V_O = 20 Vp-p)	PBW							kHz
(R_L = 2.0 kΩ)		–	–	–	10	50	–	
(R_L = 1.0 kΩ)		20	50	–	–	–	–	
Step Response								
Gain = 1000, no overshoot,	t_f	–	130	–	–	130	–	ns
R1 = 1.0 kΩ, R2 = 1.0 MΩ, R3 = 1.0 kΩ,	t_{pd}	–	190	–	–	190	–	ns
R4 = 30 kΩ, R5 = 10 kΩ, C1 = 1000 pF	dV_O/dt ②	–	6.0	–	–	6.0	–	V/µs
Gain = 1000, 15% overshoot,	t_f	–	80	–	–	80	–	ns
R1 = 1.0 kΩ, R2 = 1.0 MΩ, R3 = 1.0 kΩ,	t_{pd}	–	100	–	–	100	–	ns
R4 = 0, R5 = 10 kΩ, C1 = 10 pF	dV_O/dt	–	14	–	–	14	–	V/µs
Gain = 100, no overshoot,	t_f	–	60	–	–	60	–	ns
R1 = 1.0 kΩ, R2 = 100 kΩ, R3 = 1.0 kΩ,	t_{pd}	–	100	–	–	100	–	ns
R4 = 10 kΩ, R5 = 10 kΩ, C1 = 2200 pF	dV_O/dt	–	34	–	–	34	–	V/µs
Gain = 10, 15% overshoot,	t_f	–	120	–	–	120	–	ns
R1 = 1.0 kΩ, R2 = 10 kΩ, R3 = 1.0 kΩ,	t_{pd}	–	80	–	–	80	–	ns
R4 = 1.0 kΩ, R5 = 10 kΩ, C1 = 2200 pF	dV_O/dt	–	6.25	–	–	6.25	–	V/µs
Gain = 1, 15% overshoot,	t_f	–	160	–	–	160	–	ns
R1 = 10 kΩ, R2 = 10 kΩ, R3 = 5.0 kΩ,	t_{pd}	–	80	–	–	80	–	ns
R4 = 390 Ω, R5 = 10 kΩ, C1 = 2200 pF	dV_O/dt	–	4.2	–	–	4.2	–	V/µs
Output Impedance (f = 20 Hz)	z_o	–	4.0	–	–	4.0	–	kΩ
Output Voltage Swing	V_O							V_{pk}
(R_L = 2.0 kΩ, f = 1.0 kHz)		–	–	–	±10	±13	–	
(R_L = 1.0 kΩ, f = 1.0 kHz)		±10	±13	–	–	–	–	
Positive Supply Sensitivity (V_{EE} constant)	PSRR +	–	50	150	–	50	200	µV/V
Negative Supply Sensitivity (V_{CC} constant)	PSRR –	–	50	150	–	50	200	µV/V
Power Supply Current (V_O = 0)	I_D+	–	3.0	5.0	–	3.0	6.7	mAdc
	I_D-	–	3.0	5.0	–	3.0	6.7	

① T_{low} = 0°C for MC1439 T_{high} = +75°C for MC1439   ② dV_O/dt = Slew Rate
    = –55°C for MC1539   +125°C for MC1539
*Symbols conform to JEDEC Bulletin No. 1 where applicable.
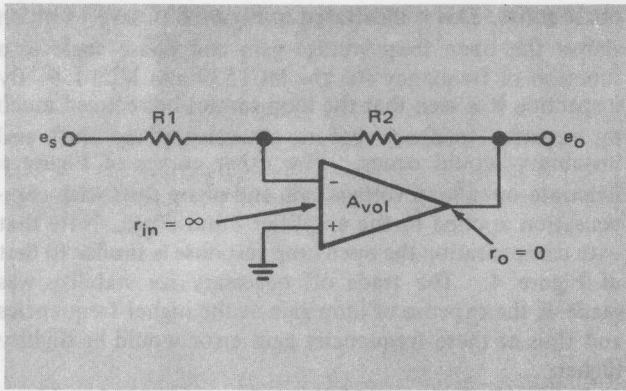
FIGURE 2 – MC1539, MC1439 Data Sheet

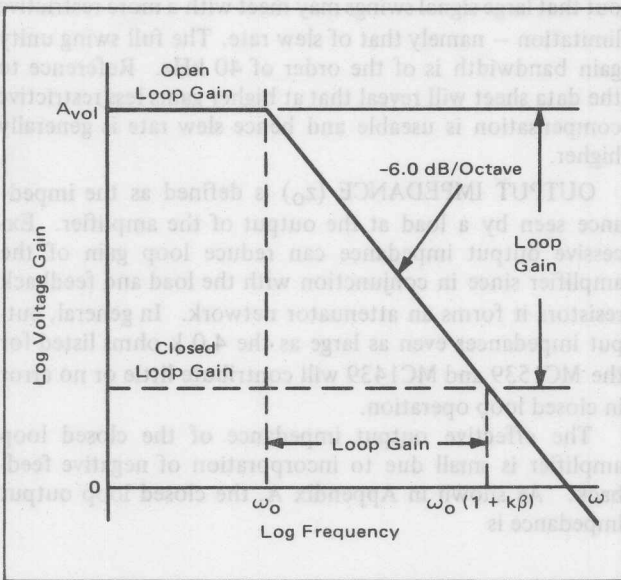**FIGURE 3 — Idealized Operational Amplifier**

FIGURE 4 — Optimum Open Loop Frequency Response

of loop gain $\left(A_{vol} \dfrac{R1}{R1 + R2} \right)$ rather than solely open loop gain. Open loop gain is the limiting factor in closed loop gain error; loop gain establishes the accuracy.

As represented in Equation 7, the gain error is not in itself too significant if resistor trimming is used to compensate for the gain error. A more important feature of the loop gain is its resultant effect upon the closed loop gain as variations in open loop gain due to device parameter spreads, temperature, etc. are encountered. Differentiation of Equation 1 with respect to open loop gain yields

$$\triangle \left(\frac{e_o}{e_s} \right) = \frac{\Delta A_{vol}}{A_{vol}} \; \frac{\left(\frac{e_o}{e_s} \right)}{1 + A_{vol} \; \dfrac{R1}{R1 + R2}} \tag{8}$$

which shows that any variation in open loop gain will be attenuated by the loop gain of the amplifier. Therein lies one of the basic benefits of feedback amplifier applications. The application of negative feedback improves closed loop gain stability.

OPEN LOOP BANDWIDTH (BW_{OL}) is defined as the frequency where the high frequency gain is 3.0 dB less than the gain at a low frequency.

This particular parameter more than any other is probably responsible for a large majority of operational amplifier design problems. Many applications are designed without allowing for closed loop gain error accrued due to a lower loop gain at the frequency of interest or problems are encountered with amplifier stability due to inadequate or marginal frequency compensation.

A desirable operational amplifier would have an open loop frequency response as shown in Figure 4. It is readily apparent that loop gain is frequency dependent and at higher frequencies gain error and gain stability will not be as good as encountered at lower frequencies.

The desirability of a –6.0 dB/octave slope for the amplifier to establish a stable amplifier instead of an oscillator need not be emphasized. In Figure 4 the amplifier response can be represented as

$$A_{vol} (\omega) = \frac{A_{vol}}{1 + j \; \dfrac{\omega}{\omega_O}} \tag{9}$$

where ω_O is the open loop bandwidth of the amplifier. Inserting Equation 9 into Equation 1 yields

$$\frac{e_o}{e_s} (\omega) = - \frac{A_{vol} \; \dfrac{R2}{R1 + R2}}{1 + A_{vol} \; \dfrac{R1}{R1 + R2} + j \; \dfrac{\omega}{\omega_O}} \tag{10}$$

which is the closed loop response of the amplifier. Equation 10 is indicative of several other important benefits in feedback amplifiers. First, it can be seen by inspection that the 3.0 dB point or closed loop bandwidth occurs when the real and imaginary terms of the denominator are equal, thus

$$\omega_{CL} = \left(1 + A_{vol} \; \frac{R1}{R1 + R2} \right) \omega_O. \tag{11}$$

Here again the loop gain is encountered. The closed loop bandwidth is extended by a factor of loop gain over the open loop bandwidth. Reflection will justify this action. Since the open loop gain is reduced by a factor equal to the loop gain, and the open loop bandwidth is increased by a factor equal to open loop gain, a gain-bandwidth trade-off has ensured for a constant gain-bandwidth circuit. Second, this particular amplifier will be unconditionally stable with a response as presented in Figure 4. From Equation 1 or 2 it is apparent that instability will occur in a closed loop amplifier when the loop gain crosses unity with 180° phase shift such that it becomes numerically –1 and causes an infinite gain due to denominator cancellation. An infinite gain is tantamount to oscillation. From Equation 10 it can be seen that the phase shift cannot exceed 90° and thus the amplifier is unconditionally stable.

In a high gain, multi-stage operational amplifier, the concept of a single lag network (pole) as illustrated in Figure 4 is unrealistic since each stage will contribute
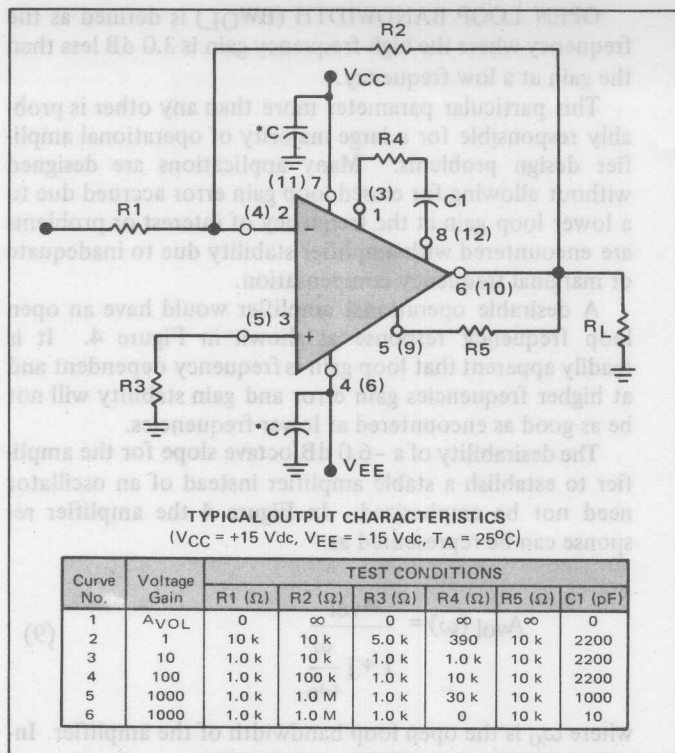
TYPICAL OUTPUT CHARACTERISTICS
(V_{CC} = +15 Vdc, V_{EE} = –15 Vdc, T_A = 25°C)

Curve No.	Voltage Gain	TEST CONDITIONS					
		R1 (Ω)	R2 (Ω)	R3 (Ω)	R4 (Ω)	R5 (Ω)	C1 (pF)
1	A_{VOL}	0	∞	0	∞	∞	0
2	1	10 k	10 k	5.0 k	390	10 k	2200
3	10	1.0 k	10 k	1.0 k	1.0 k	10 k	2200
4	100	1.0 k	100 k	1.0 k	10 k	10 k	2200
5	1000	1.0 k	1.0 M	1.0 k	30 k	10 k	1000
6	1000	1.0 k	1.0 M	1.0 k	0	10 k	10

FIGURE 5 — Test Circuit Used to Obtain Curves in Figure 6 and Figure 12
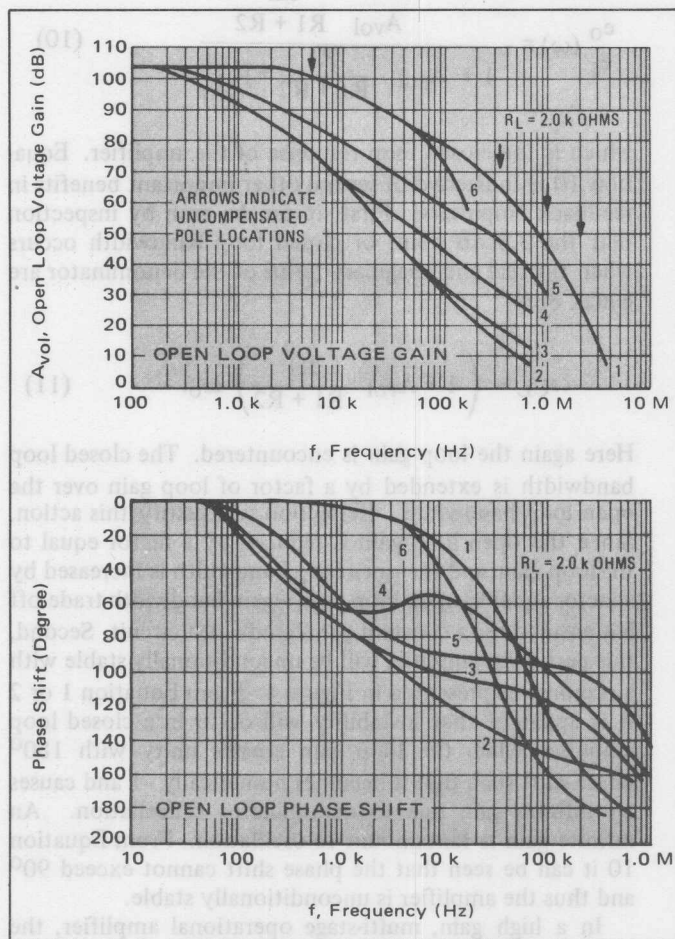
FIGURE 6 — Open Loop Voltage Gain and Phase Angle versus Frequency

phase shifts. This is illustrated in Figure 6 (Curve 1) which shows the open loop voltage gain and phase angle as a function of frequency for the MC1539 and MC1439. By inspection it is seen that the loop cannot be reduced much by negative feedback before excessive phase shift and instability would occur. The other curves of Figure 6 illustrate open loop voltage gain and phase shift with compensation applied to the amplifier input stage. Note that with compensation the open loop response is similar to that of Figure 4. The trade off necessary for stability was made at the expense of loop gain at the higher frequencies and thus at these frequencies gain error would be slighlty higher.

Figures 7, 8, 9, and 10 show the resultant closed loop response. It should be emphasized that these curves illustrate typical small signal characteristics. Figure 11 points out that large signal swings may meet with a more restrictive limitation — namely that of slew rate. The full swing unity gain bandwidth is of the order of 40 kHz. Reference to the data sheet will reveal that at higher gains less restrictive compensation is useable and hence slew rate is generally higher.

OUTPUT IMPEDANCE (z_O) is defined as the impedance seen by a load at the output of the amplifier. Excessive output impedance can reduce loop gain of the amplifier since in conjunction with the load and feedback resistors it forms an attenuator network. In general, output impedances even as large as the 4.0 k ohms listed for the MC1539 and MC1439 will contribute little or no error in closed loop operation.

The effective output impedance of the closed loop amplifier is small due to incorporation of negative feedback. As shown in Appendix A, the closed loop output impedance is

$$z_{O\,CL} = \frac{z_O}{1 + A_{vol}\left(\dfrac{R1}{R1 + R2}\right)} \quad (12)$$

and is reduced by the amount of loop gain. One final consideration is that as indicated by Equation 12, output impedance will increase as a function of frequency because loop gain decreases.

It is, of course, erroneous to model the output resistance of an op amp as a discrete resistor for a large signal model, as it is certainly possible to obtain several milliamperes of current from the MC1539.

INPUT IMPEDANCE (z_{in}) is defined as the impedance seen by a source looking into one input of the amplifier with the other input grounded. The primary effect of input impedance is to reduce amplifier loop gain and consequently alter gain accuracy and stability. If in Equation 1 a finite input impedance is included

$$\frac{e_o}{e_s} = -\frac{A_{vol}\dfrac{R2'}{R1 + R2'}}{1 + A_{vol}\dfrac{R1'}{R1' + R2}} \quad (13)$$
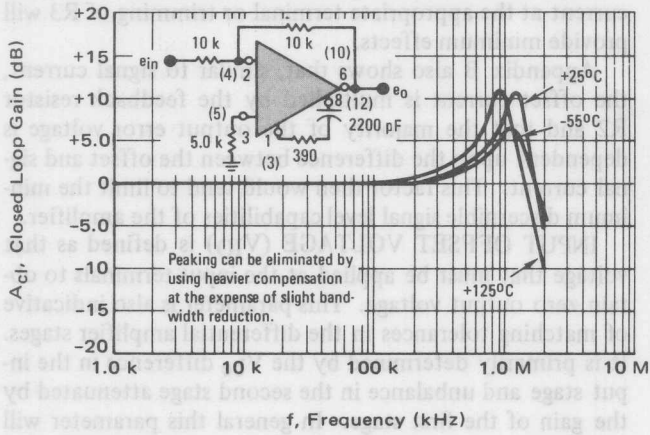
where

FIGURE 7 — $A_{cl} = 1$ Response versus Temperature

Peaking can be eliminated by using heavier compensation at the expense of slight bandwidth reduction.

FIGURE 8 — $A_{cl} = 10$ Response versus Temperature

FIGURE 9 — $A_{cl} = 100$ Response versus Temperature

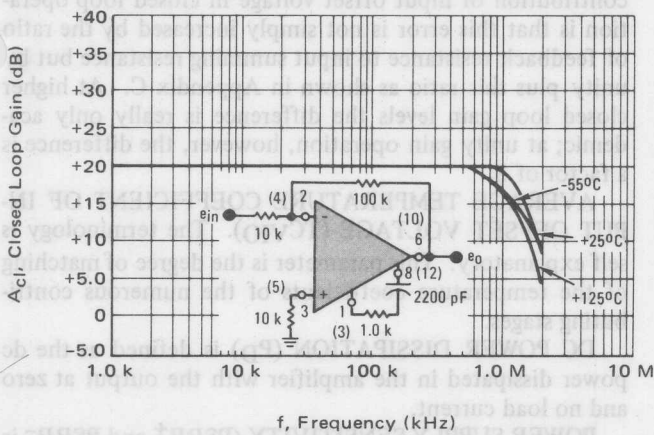**FIGURE 10 — $A_{cl} = 1000$ Response versus Temperature**

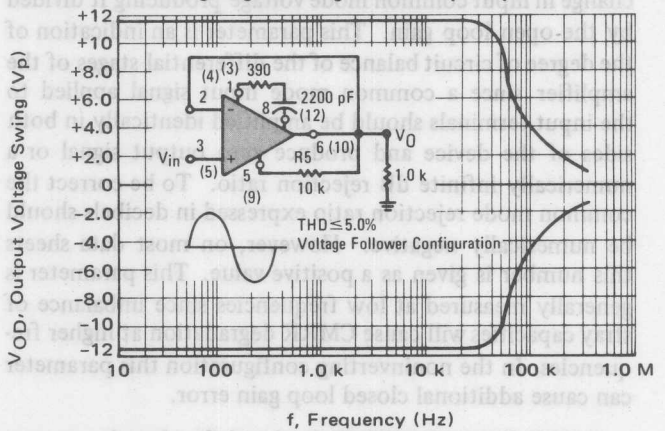**FIGURE 11 — Power Bandwidth (Large Signal Swing versus Frequency)**

THD ≤ 5.0%
Voltage Follower Configuration
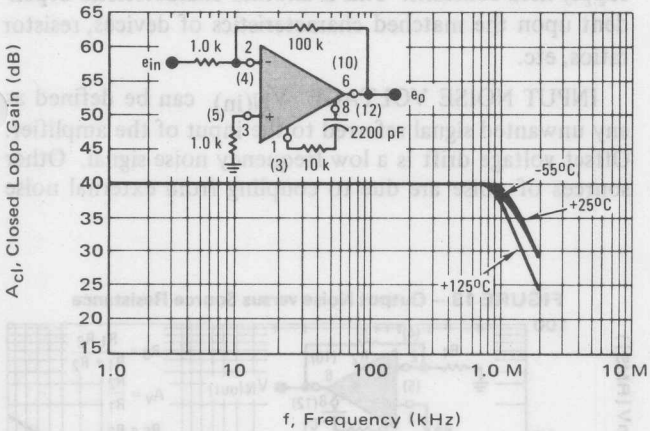
FIGURE 12 — Large Signal Swing versus Frequency

$R_L = 1.0$ k OHM
≤ 5% THD
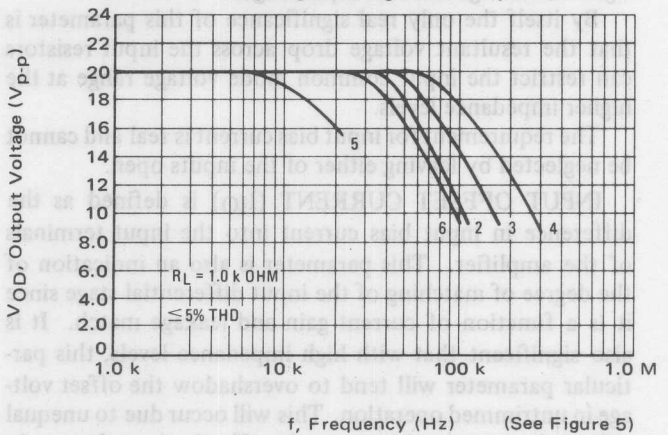
$$R2' = \frac{R2 \ z_{in}}{R2 + z_{in}} \qquad (14)$$

$$R1' = \frac{R1 \ z_{in}}{R1 + z_{in}} \qquad (15)$$

It must be noted that the data sheet specification refers to small-signal input impedance where "small" is < 200 mVp-p.

A look at the schematic reveals that a large differential input signal will cause the clamping diodes to be turned on and reduce the input impedance to something slightly greater than 2.0 k ohms.

OUTPUT VOLTAGE SWING (V_{OD}) is defined as the peak output voltage swing referred to zero that can be obtained without clipping. A symmetrical voltage swing is generally implied. As mentioned previously, output

impedance, load current, and frequency limit this particular characteristic of the amplifier.

Figure 12 shows the maximum output voltage swing available from the devices as a function of frequency and compensation technique.

INPUT COMMON MODE VOLTAGE SWING (V_{ICR}) is defined as the maximum peak input voltage that can be applied to either input terminal of the device without causing abnormal operation. This particular parameter is most prominent when using the amplifier in the non-inverting mode or as an inverting integrator where excessive signal levels or transients are encountered.

The positive limit of this characteristic is dependent upon the collector voltage of the input stage of the amplifier while the negative limit is generally limited by the base voltage of the constant current source of the first stage.

COMMON MODE REJECTION RATIO (CMRR) is defined as the ratio of the change in output voltage to the change in input common mode voltage producing it divided by the open loop gain. This parameter is an indication of the degree of circuit balance of the differential stages of the amplifier since a common mode input signal applied to the input terminals should be amplified identically in both sides of the device and produce zero output signal or a numerically infinite dB rejection ratio. To be correct the common mode rejection ratio expressed in decibels should be numerically negative. However, on most data sheets this number is given as a positive value. This parameter is generally measured at low frequencies since unbalance of stray capacities will cause CMRR degradation at higher frequencies. In the noninverting configuration this parameter can cause additional closed loop gain error.

INPUT BIAS CURRENT (I_{IB}) is defined as the average value of the two input bias currents of the differential input stage. This parameter is simply a function of the large signal current gain of the input stage.

By itself the only real significance of this parameter is that the resultant voltage drop across the input resistors can restrict the input common mode voltage range at the higher impedance levels.

The requirement for input bias current is real and cannot be neglected by leaving either of the inputs open.

INPUT OFFSET CURRENT (I_{IO}) is defined as the difference in input bias current into the input terminals of the amplifier. This parameter is also an indication of the degree of matching of the input differential stage since it is a function of current gain and leakage match. It is also significant that with high impedance levels, this particular parameter will tend to overshadow the offset voltage in untrimmed operation. This will occur due to unequal voltage drops appearing across the effective impedance. As shown in Appendix B, to obtain minimum offset voltage drops due to offset currents, a resistor equal in magnitude to the parallel equivalent of the input and summing resistor should be inserted in the non-inverting input.

$$R3 = \frac{R1\ R2}{R1 + R2} \qquad (16)$$

This condition will not necessarily produce zero resultant offset but will tend to minimize offset voltage for equal

currents and unequal impedances. Injection of an offset current at the appropriate terminal or trimming of R3 will provide minimum effects.

Appendix B also shows that, similar to signal current, the offset current is multiplied by the feedback resistor R2 and that the majority of the output error voltage is dependent upon the difference between the offset and signal current. This factor then would tend to limit the minimum discernible signal level capabilities of the amplifier.

INPUT OFFSET VOLTAGE (V_{IO}) is defined as that voltage that must be applied at the input terminals to obtain zero output voltage. This parameter is also indicative of matching tolerances in the differential amplifier stages. It is primarily determined by the V_{be} difference in the input stage and unbalance in the second stage attenuated by the gain of the first stage. In general this parameter will be the major source of offset voltage error in low impedance circuits.

A factor not always considered when determining the contribution of input offset voltage in closed loop operation is that this error is not simply increased by the ratio of feedback resistance to input summing resistance but by unity plus this ratio as shown in Appendix C. At higher closed loop gain levels the difference is really only academic; at unity gain operation, however, the difference is a factor of 2.

AVERAGE TEMPERATURE COEFFICIENT OF INPUT OFFSET VOLTAGE (TC_{VIO}). The terminology is self explanatory. This parameter is the degree of matching of the temperature coefficients of the numerous contributing stages.

DC POWER DISSIPATION (P_D) is defined as the dc power dissipated in the amplifier with the output at zero and no load current.

POWER SUPPLY SENSITIVITY ($PSRR^+$ and $PSRR^-$ is defined as the ratio of change in input offset voltage to the change in supply voltage producing it with the remaining supply held constant. This is another characteristic dependent upon the matched characteristics of devices, resistor ratios, etc.

INPUT NOISE VOLTAGE $V_{N(in)}$ can be defined as any unwanted signal referred to the input of the amplifier. Offset voltage drift is a low frequency noise signal. Other sources of noise are due to coupling from external noise

FIGURE 13 – Output Noise versus Source Resistance

8
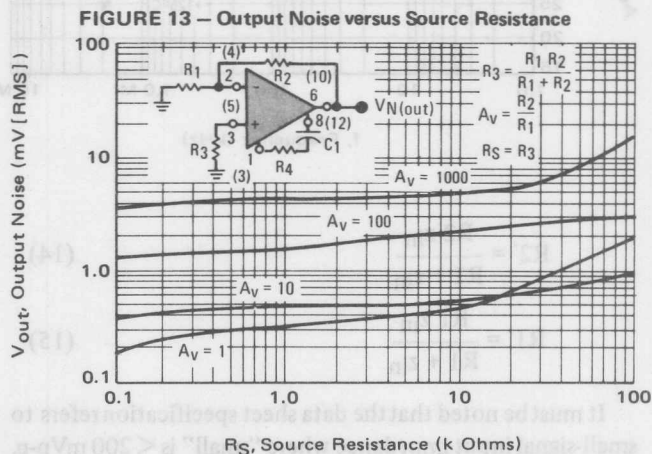
sources and the thermal noise generated in a resistor or conductor. These noise voltages are treated simply as if they were drift voltages discussed above.

Figure 13 illustrates typical wideband output noise as measured for various configurations of the MC1539.

SUMMARY AND CONCLUSIONS

The various pertinent open loop parameters of operational amplifiers have been defined and reviewed with respect to their significance in closed loop operation. One point that manifested itself was the importance of loop gain in the ultimate closed loop circuit operation.

Loop gain determines gain accuracy, gain stability, closed loop bandwidth and effective output impedance in actual operation. The point was also made that input drift errors must be considered individually depending upon whether it is offset current or offset voltage drift. Ready reference was made to supplementary parameter characteristics in order to clarify points and give a better device understanding. The application of the principles discussed in this paper should permit usage of the operational amplifier in any of the numerous circuit configurations available while still maintaining maximum design efficiency.

APPENDIX A. EFFECTIVE CLOSED LOOP OUTPUT IMPEDANCE

Let the open loop input impedance of the amplifier in Figure A1 be infinite. The following nodal equations can then be written

$$I = i_0 + i_2 \tag{17}$$

$$i_0 = \frac{E - (-A_{vol}\epsilon)}{R_0} \tag{18}$$

$$i_2 = \frac{E}{R1 + R2} \tag{19}$$

$$\epsilon = E \frac{R1}{R1 + R2} \tag{20}$$

Combining and solving yields for output conductance

$$Y_0 = \frac{I}{E} = \frac{1}{R_0} \left(1 + A_{vol} \frac{R1}{R1 + R2} \right) + \frac{1}{R1 + R2} \tag{21}$$

where the open loop output conductance is increased by a factor equal to loop gain; or conversely, the output resistance is reduced by a factor equal to loop gain in the closed loop configuration
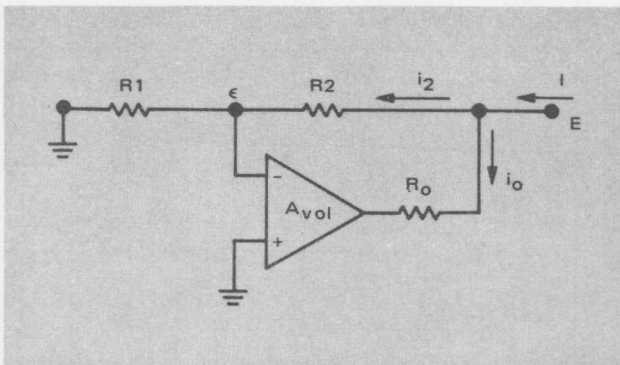
APPENDIX B. INPUT OFFSET CURRENT CONSIDERATIONS

Writing the nodal equations for the amplifier in Figure B1 yields

$$e_0 = A_{vol} (V - \epsilon) \tag{22}$$

$$V = -i_2 R3 \tag{23}$$

$$\epsilon = -i_x R1 \tag{24}$$

$$i_x = i_1 - i_4 \tag{25}$$

$$i_4 = \frac{e_0 - \epsilon}{R2} \tag{26}$$

Solving for the output voltage

$$e_0 = i_1 R2 - i_2 R3 \left(1 + \frac{R2}{R1} \right) \tag{27}$$

For zero output voltage

$$i_1 R2 = i_2 R3 \left(1 + \frac{R2}{R1} \right) \tag{28}$$

or

$$i_1 \frac{R1 R2}{R1 + R2} = i_2 R3 \tag{29}$$
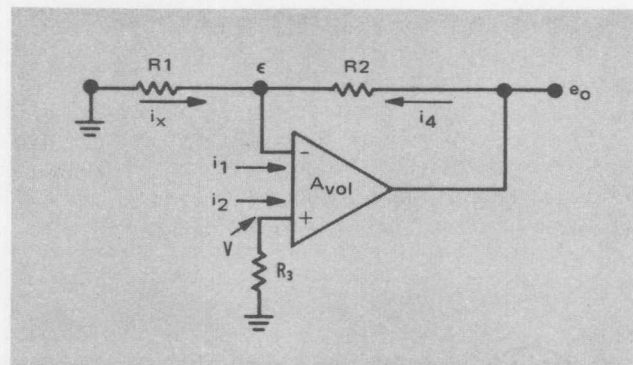

FIGURE A1 – Closed Loop Impedance is Infinite

FIGURE B1 – Input Offset Currents

if $i_1 = i_2$

$$R3 = \frac{R1\,R2}{R1 + R2}. \tag{30}$$

Thus the magnitude of R3 should be equal to the parallel combination of the inverting input and feedback resistors

to realize minimum offset current effects.

If Equation 30 is inserted into Equation 27

$$e_0 = (i_1 - i_2)\,R2 \tag{31}$$

which states that the input offset current is multiplied by the feedback resistance at the output.

APPENDIX C. INPUT OFFSET VOLTAGE CONSIDERATIONS

The amplifier in Figure C1 contains two offset voltages, e_{os}, generated in the input of the first amplifier stage, and V, generated in the input of the second amplifier stage. The latter being included mainly for academic reasons. The nodal equations are

$$e_0 = A_{VO2}\left[V - A_{vo1}\left(\epsilon \pm \epsilon_{os} \right) \right] \tag{32}$$

$$\epsilon = e_0\,\frac{R1}{R1 + R1} \tag{33}$$

Combining and solving gives

$$e_0 = \left(1 + \frac{R2}{R1}\right)\left[e_{os} \pm \frac{V}{A_{vo1}} \right]. \tag{34}$$

Where it was assumed the loop gain $\gg 1$.

Equation 34 indicates two important considerations with respect to offset voltage error in closed loop operation. First, the offset voltage of the second stage is attenuated by the gain of the first stage as occurs with noise voltage

generation. Thus with adequate gain in the first stage, the second stage offset can be isolated and the amplifier only dependent upon first stage offset. The second consideration is that the resultant offset voltage is multiplied by unity plus the ideal gain as given by the resistance ratios. This consideration has more than a little significance at the lower closed loop gains. For unity gain, the effective offset is doubled.
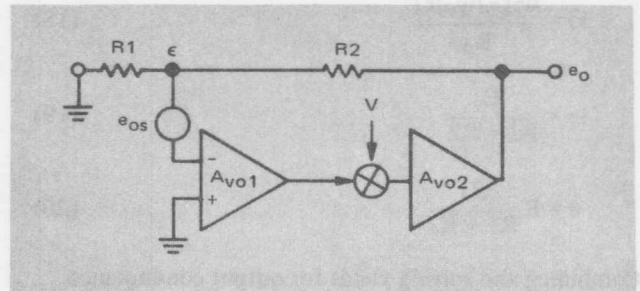

FIGURE C1 – Input Offset Voltage