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"SEMICONDUCTOR CONSIDERATION FOR DC POWER SUPPLY VOLTAGE PROTECTOR CIRCUITS"

MOTOROLA Semiconductors

SEMICONDUCTOR CONSIDERATION FOR DC POWER SUPPLY OVER-UNDER VOLTAGE PROTECTOR CIRCUITS „

Abstract

This paper addresses the requirements for the semiconductor sensing circuitry and SCR crowbar devices used in DC poser supply OVER-UNDER VOLTAGE PROTECTION schemes.

Introduction

It is uncommon now to find several hundred dollars worth of microprocessors and memory chips powered from a single low DC supply.

If this supply on the board does'nt have overvoltage or undervoltage protection, potentially large sums of money can literally go up in smoke due to component failure or, for instance, a tool accidentally dropped across the supply buses of different voltages during testing or repair of the system.

Since a couple of years, computer and industrial manufacturers agree to put additional small investment in OVP*, OUVP* circuitry to prevent disasters.

MOTOROLA choose the "crowbar" sensing circuit technology". This system senses the overvoltage condition, and quickly "crowbar" or short circuit the supply, forcing the supply into current limiting or opening the fuse or circuit breaker. Before to detail this technology, 3 questions should be considered:

1°) **Why OVP?:** Evidently for saving money and increasing the reliability of the system.

2°) **Where OVP?:**
- — Everywhere over/under voltage is a problem
- — Everywhere, power supply system is used
- — Everywhere switchmode system is designed

3°) **How OVP?:** There are several types of sense circuits presently being used in OVP applications. They can be classified into three types:
a) ZENER
b) DISCRETE
c) MC1723 (voltage regulator in OVP configuration).

OVP* (Over Voltage Protector), OUVP* (Over, Under Voltage Protector).

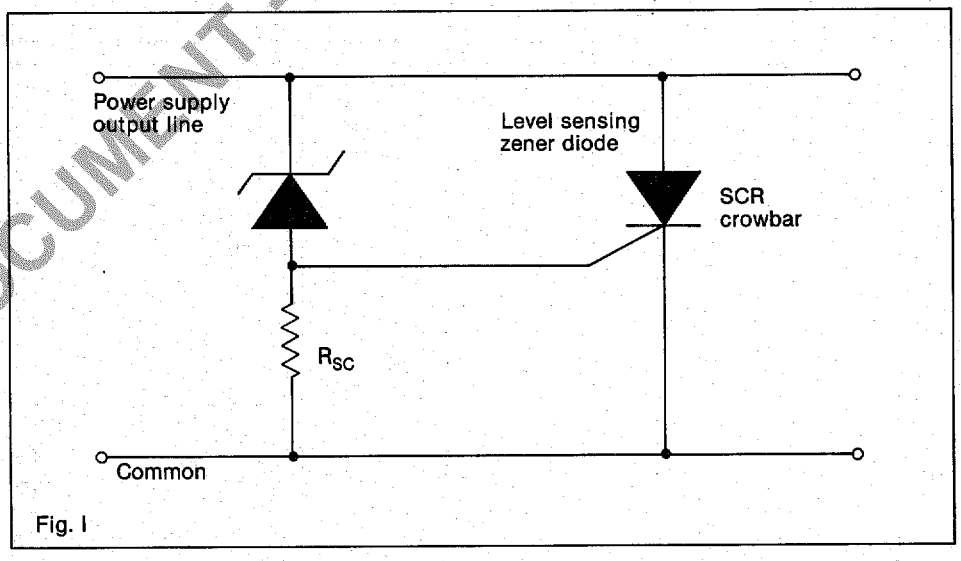

Fig. I

a) The zener sense circuit

The simplest way to protect against overvoltage is to use a zener diode to sense the output voltage (Fig. I). When the zener goes into avalanche, it triggers the SCR.

There are problems with this kind of protection:

1°) No threshold adjustment, except by selecting different zener diodes

2°) Inability to ignore momentary transients

3°) Poor SCR reliability caused by inadequate trigger-current rise time when slowly varying voltage is sensed.

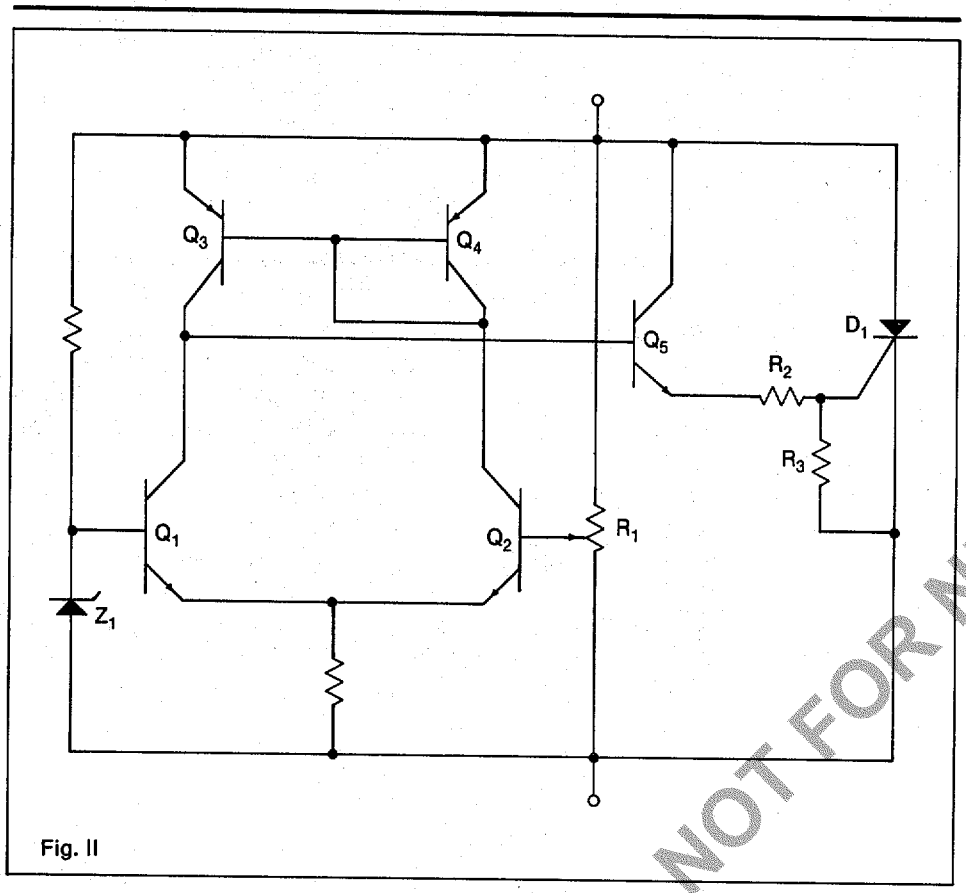

Fig. II

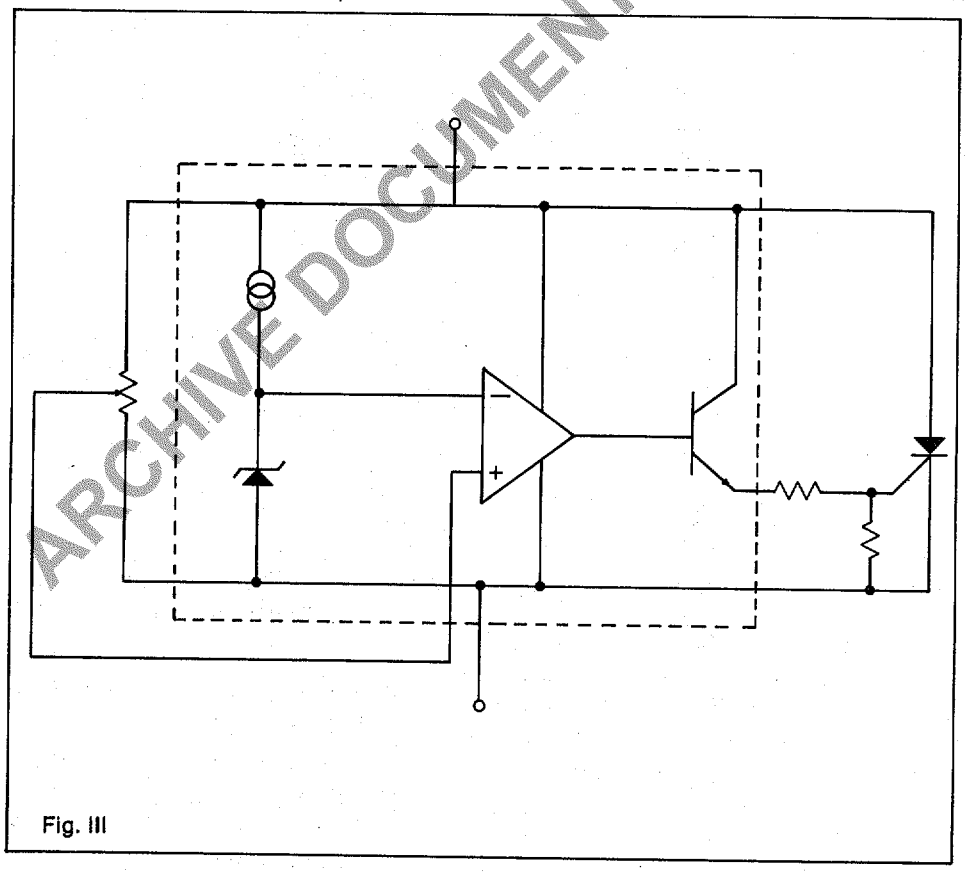

Fig. III

b) The discrete sense circuit

A technique which can provi adequate gate drive and an a justable, low temperature coef cient trip point is shown in Fig. II

This circuit includes the Zen reference voltage (Z_1), the co parator section (Q_1, Q_2), bandg circuit (Q_3, Q_4), potentiometer (R_1 trip point, output section (Q_5, R_2, R D_1).

While overcoming the problem of the Zener sense circuit, thi technique brings also many disad vantages:

1°) This technique requires man components (12 here)

2°) Cost is very high

3°) This method is not particular noise immune and often suffe from nuisance tripping.

c) The MC1723 sense circuit

A simpler approach is to fire th SCR crowbar with an MC172 voltage regulator.

A considerable reduction in com ponent count is done (see Fig. II The main disadvantages are:

1°) No noise immunity

2°) The minimum input voltage range is 9.5 V, so you're restricted to use it for highe voltages or to supplement it by feeding in an auxiliary suppl voltage.

The SCR choose

The use of the SCR crowbar overvoltage protection circuits in DC power supplies has been, for many years, a popular method of providing protection to the load from accidental overvoltage stresses. This technique and its proper implementation have become increasingly important in light of the recent advances in LSI made by the semiconductor industry.

Referring to Fig. IV, V, it can be seen that the crowbar SCR, when activated, is subject to a large current surge from the output capacitance, C_{out}. This surge current is illustrated in Fig. VI and can cause SCR failure or degradation by any one of three mechanisms: di/dt, absolute peak surge, or I^2t. The interrelationship of these failure methods and the breadth of the application make specification of the SCR by the semiconductor manufacturer difficult and expensive. Therefore, the designer must empirically determine the SCR and circuit elements which result in reliable and effective OVP operation. However, an understanding of the factors which influence the SCR's di/dt and surge capabilities simplifies this task.

1. di/dt

As the gate region of the SCR is driven on, its area of conduction takes a finite amount of time to grow, starting as a very small region and gradually spreading. Since the anode current flows through this turned-on gate region, very high current densities can occur in the gate region if high anode currents appear quickly (di/dt). This can result in immediate destruction of the SCR or gradual degradation of its forward blocking voltage capabilities—depending on the severity of the occasion.

C_{out} consists of the power supply output caps, the load's decoupling caps, and in the case of Fig. IV, the supply's input filter caps.

The value of di/dt that an SCR can safely handle is influenced by its construction and the characteristics of the gate drive signal. A center-gate-fire SCR has more di/dt capability than a corner-gate-fire type and heavily overdriving (3 to 5 times I_{GT}) the SCR gate with a fast (< 1 µs) rise time signal will maximize its di/dt capability. A typical maximum number in phase control SCRs of less than 50 Arms rating might be 200 A/µs, assuming a gate current of five times I_{GT} and < 1 µs rise time. If having done this, a di/dt problem is seen to still exist, the designer can also decrease the di/dt of the current waveform by adding inductance in series with the SCR, as shown in Fig. VII. Of course, this reduces the circuit's ability to rapidly reduce the dc bus voltage and a tradeoff must be made between speedy voltage reduction and di/dt.

2. Surge Current

If the peak current and/or the duration of the surge is excessive, immediate destruction due to device overheating will result. The surge capability of the SCR is directly proportional to its die area. If the surge current cannot be reduced (by adding series resistance—see Fig. VII) to a safe level which is consistent with the system's requirements for speedy bus voltage reduction, the designer must use a higher current SCR. This may result in the average current capability of the SCR exceeding the steady state current requirements imposed by the dc power supply.

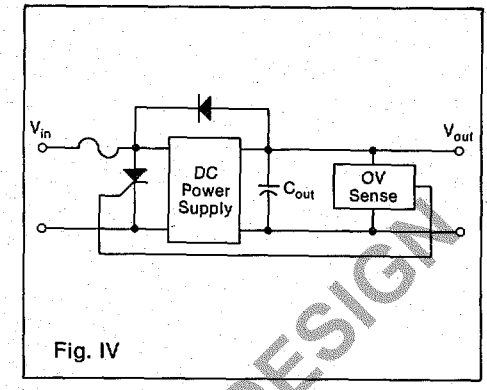

Fig. IV

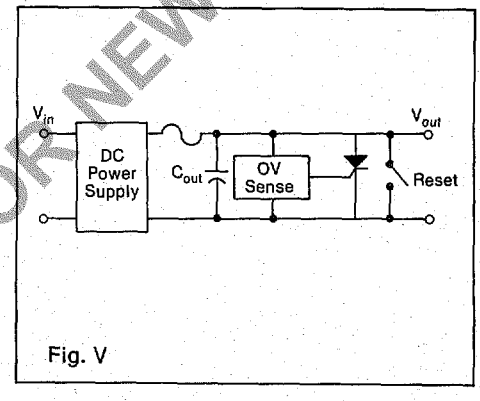

Fig. V

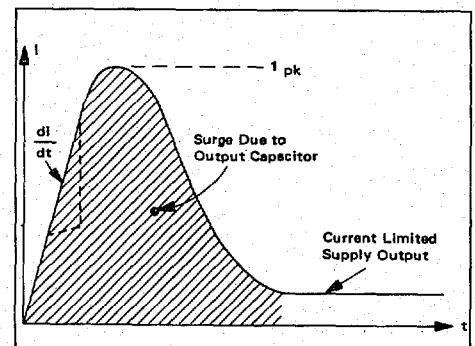

Fig. VI

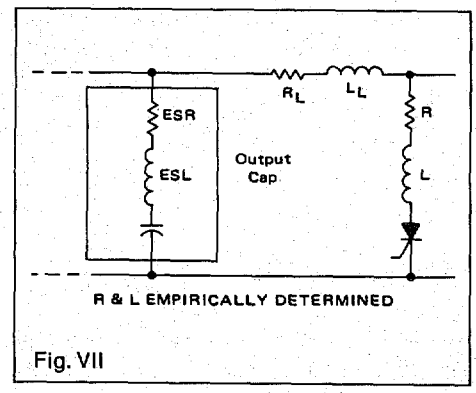

Fig. VII

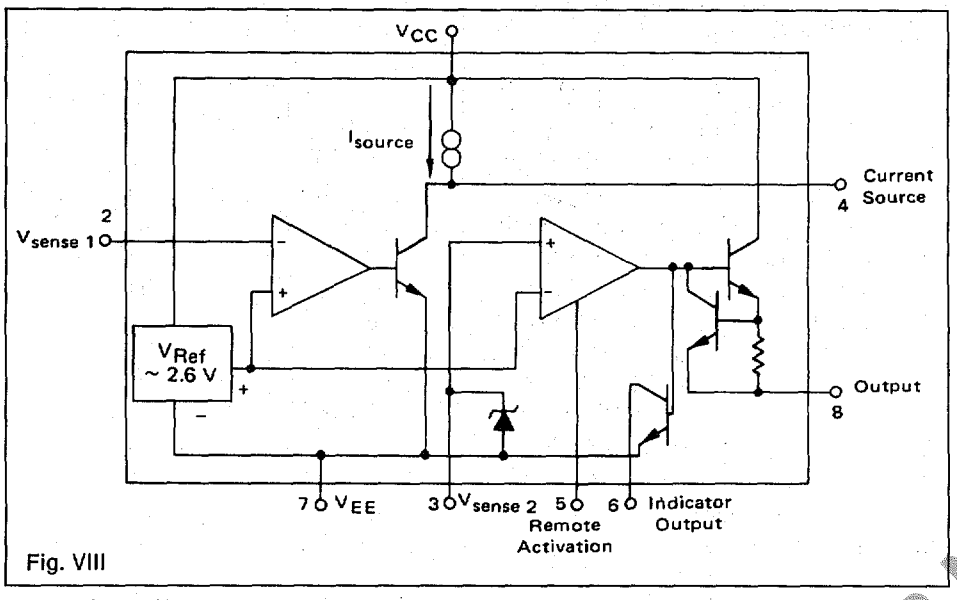

Fig. VIII

Overvoltage protector: the MC3423

To fill the need for a low cost, low complexity method or implementing crowbar overvoltage protection which does not suffer the disadvantages of previous techniques, and IC has been developed by Motorola in 1979. **THE MC3423** and its military temperature range version **THE MC3523**.

This circuit was designed to provide output currents of up to 300 mA with a 400 mA/µs rise time in order to maximize the di/dt capabilities of the crowbar SCR. In addition, its main features include:

1) Operation off 4.5 V to 36 V supply voltages
2) Adjustable, low temperature coefficient trip point
3) Adjustable minimum overvoltage duration before actuation (0.5 µS to 1 mS) to reduce nuisance tripping in noisy environments
4) Remote activation input
5) Activation indication output
6) Output short circuit protected for $V_{CC} \leq 10$ V

1°) The Block Diagram

— The block diagram of the MC3423 is shown in Fig. VIII. It consists of a stable 2.6 V reference, two comparators and a high current output.

— This output, together with the indication output transistor, is activated either by a voltage greater than 2.6 V on pin 3 or by a TTL/5 V C_{mos} high logic level on the remote activation input, pin 5.

— The first comparator is designed to initiate a stable time delay and the second one activates both a crowbar firing current and a low level indication signal.

2°) The Basic Circuit

— The basic circuit configuration of the OVP is shown in Fig. IX. In this circuit, the voltage sensing inputs of both the internal amplifiers are tied together for sensing the overvoltage condition. The shortest possible propagation delay is thus obtained.

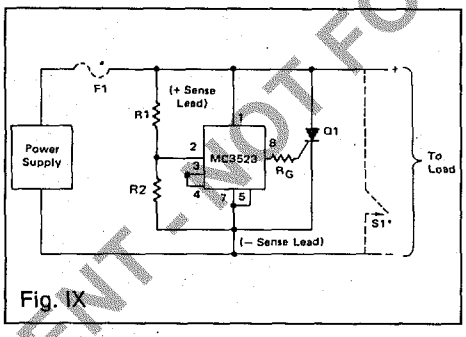

Fig. IX

The threshold on trip voltage at which the MC3423 will trigger and supply gate drive to the crowb SCR, Q_1, is determined by the selection of R_1 and R_2. Their values can be determined by the equation (1):

$$Vtrip = V_{REF}\left(1+\frac{R1}{R2}\right) \simeq 2.6\,V\left(1+\frac{R1}{R2}\right) \quad (1)$$

$R2 \leq K\Omega$ for minimum drift

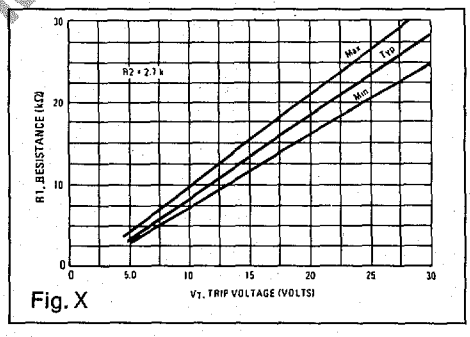

Fig. X

The graph Fig. X shows (with R_2 = 2.7 KΩ) the value (min, typ, max) of R_1 versus trip voltage.

The switch S_1, shown in Fig. IX, may be used to reset the SCR crowbar. Otherwise, the power supply, accross which the SCR is connected, must be shut down to reset the crowbar. If a non current-limited supply is used, a fuse or circuit breaker, F_1, should be used to protect the SCR and/or the load.

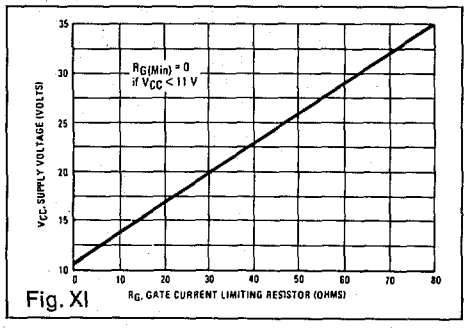

Fig. XI

The minimum value of the gate current limiting resistor, R_G, is given in Fig. XI. Using this value of R_G the SCR Q1 will receive the greatest gate current possible without damaging the MC3423. If lower output currents are required, R_G can be increased in value.

The programmation

a) **Low Voltage < 36 V**

In many instances, the MC3423 will be used in a noise environment. To present false tripping of the OVP circuit by noise which would not normally harm the load, the MC3423 has a programmable delay feature. To implement this feature, the circuit configuration of figure XII is used. In this configuration, a capacitor is connected from pin 3 to V_{EE}. The value of this capacitor determines the minimum duration of the overvoltage condition which is necessary to trip the OVP. The value of C can be found from Figure XIII. The circuit operates in the following manner: when V_{CC} rises above the trip point set by R_1 and R_2, an internal current source (pin 4) begins charging the capacitor, C, connected to pin 3. If the overvoltage condition disappears before this occurs, the capacitor is discharged at rate ≅ 10 times faster than the charging rate, resetting the timing feature until the next overvoltage condition occurs.

Occasionally, it is desired that immediate crowbarring of the supply occurs when a high overvoltage condition occurs, while retaining the false tripping immunity of Figure XII.

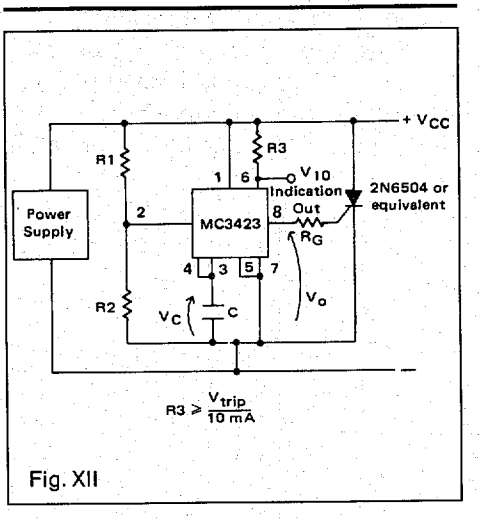

Fig. XII

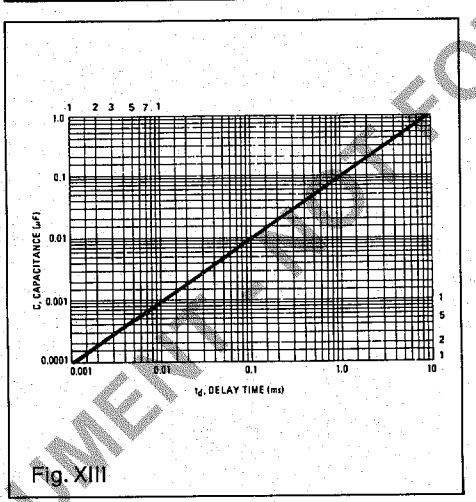

Fig. XIII

Following the choose of the SCR (Q1) the protection can be done up to 800 V

VS ≤ 50 V: 2N6504 or equivalent
VS ≤ 100 V: 2N6505 or equivalent
VS ≤ 200 V: 2N6506 or equivalent
VS ≤ 400 V: 2N6507 or equivalent
VS ≤ 600 V: 2N6508 or equivalent
VS ≤ 800 V: 2N6509 or equivalent

On this configuration (Fig. XIV) the typical propagation delay is 1.0 μS. If faster operation is desired, pin 3 may be connected to pin 2 with pin 4 left floating. This will result in decreasing the propagation delay to approximately 0.5 μS at the expense of a slightly increased T_C for the trip voltage value.

b) **High Voltage 36 V < V < 800 V**

Fig. XIV is a typical application for voltage protection over 36 V, using a Zener diode 1N4740 (10 V) and a 10 μF (15 V) capacitor at the positive sense lead.

The value of R_S can be calculated with the following formula (2)

$$Rs = \frac{(VS - 10)}{25} K\Omega \quad (2)$$

The V trip is given by the formula (1).

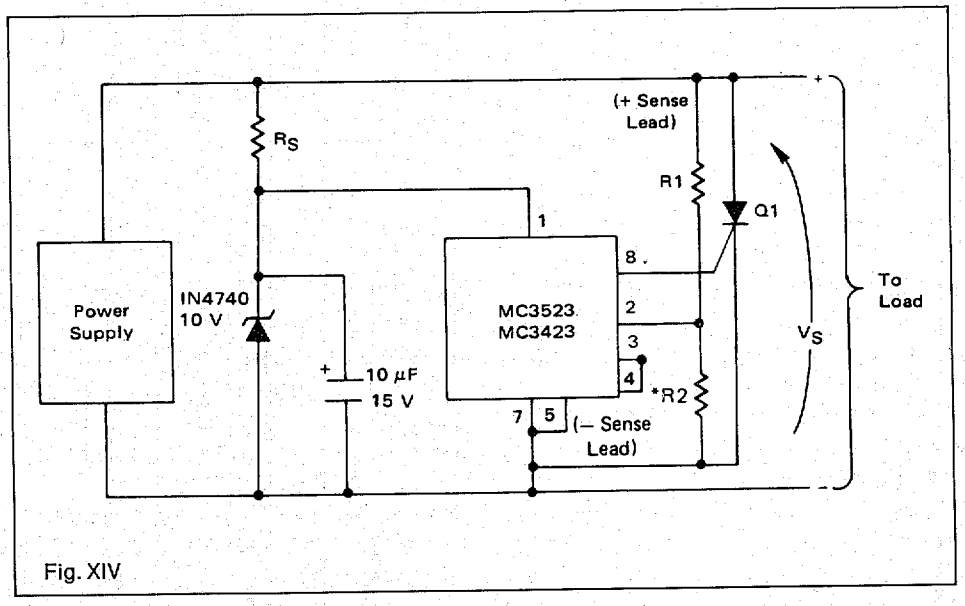

Fig. XIV

The additional features

1) Activation Indication Output

An additional output for use as an indication of OVP activation is provided by the MC3423/3523. This output is an open collector transistor which saturates when the OVP is activated. It will remain in a saturated state until the SCR crowbar pulls the supply voltage, V_{CC}, below 4.5 V as in Figures XII and XV. This output can be used to clock an edge triggered flip-flop whose output inhibits or shuts down the power supply when the OVP trips. This reduces or eliminates the heat-sinking requirements for the crowbar SCR.

Using Fig. XIII (C value) and Fig. XV, td is equal to:

$$td = \frac{Vref}{I_{source}} \times C \simeq (12.10^3) \cdot C \quad (3)$$

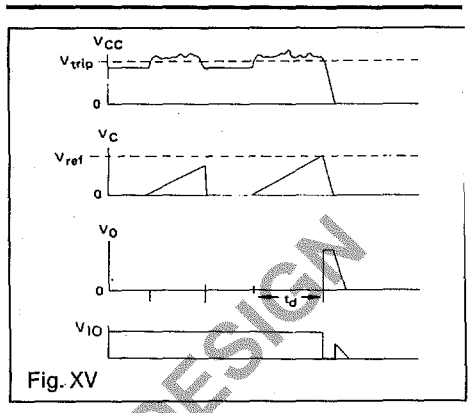

Fig. XV

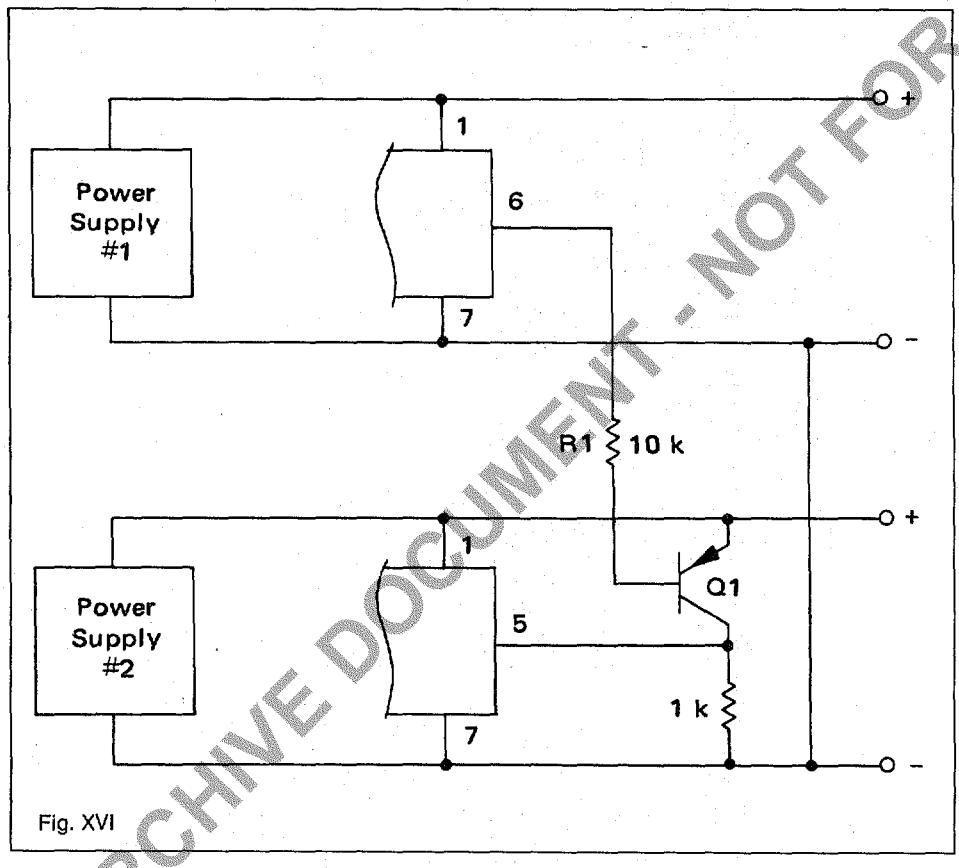

Fig. XVI

2) Remote Activation Input

Another feature of the MC3423/3523 is its remote activation input, pin 5. If the voltage on this CMOS/TTL compatible input is held below 0.8 V, the MC3423/3523 operates normally. However, if it is raised to a voltage above 2.0 V, the OVP output is activated independent of whether or not an overvoltage condition is present. It should be noted that pin 5 has an internal pull-up current source. This feature can be used to accomplish an orderly and sequenced shut-down of system power supplies during a system fault condition. In addition the activation indication output of one MC3423/3523 can be used to activate another MC3423/3523 if a single transistor inverter is used to interface the former's indication output to the latter's remote activation input, as shown in Fig. XVI. In this circuit, the indication output (pin 6) of the MC3423 on power supply 1 is used to activate the MC3423 associated with power supply 2. Q1 is any small PNP with adequate voltage rating.

Note that both supplies have their negative output leads tied together (i.e., both are positive supplies). If their positive leads are common (two negative supplies) the emitter of Q1 would be moved to the positive lead of supply 1 and R1 would therefore have to be resized to deliver the appropriate drive to Q1.

3) A Word about Fuse Protector

Referring back to Fig. IV and V it will be seen that a fuse is necessary if the power supply to be protected is not output current limited. This fuse is not meant to prevent SCR failure but rather to prevent a fire!

In order to protect the SCR, the fuse would have to possess an I^2t rating less than that of the SCR and yet have a high enough continuous current rating to survice normal supply output currents.

In addition, it must be capable of successfully cleaning the high short circuit currents from the supply. Such a fuse as this is quite expensive, and may not even be available.

What about over and under voltage protection

Two types of circuits have been developed: The MC3424 and the MC3425 with their military temperature range series MC3524 and MC3525. Like the MC3423 these circuits were primarily intended for use as a voltage protection circuit. Basically the MC3424 and MC3425 use also the "crowbar sensing circuit technology" and the block diagrams (Fig. XVII and XVIII) seems to the MC3423.

If we look at Fig. XVII (MC3424) we can see two channels of uncommitted differential inputs with a common mode range from ground (V_{EE}) to $V_{CC}+$, for maximum flexibility. This circuit have an externally programmable hysterisis. However, the output is very stable (T_C < .01%/°C), due mainly to its band gap reference voltage circuit: 2.5 V at 10 mA

- The two independent drive outputs are able of sourcing 300 mA at a slew rate of 200 to 400-mA/µS.

— The two indicators are capable of sinking 300 mA.

— The enable input (CMOS, TTL, DTL compatible) control of either channel 2 or both channels depending on channel 1 input conditions.

— Each channel can be operated closed loop with gain or unity gain, stabilized at the delay pin.

If we look at Fig. XVIII (MC3425) we see a low cost OUVP version: 8 pins dual in line instead of 14 pins for the MC3424.

MC3424/MC3524 EQUIVALENT CIRCUIT

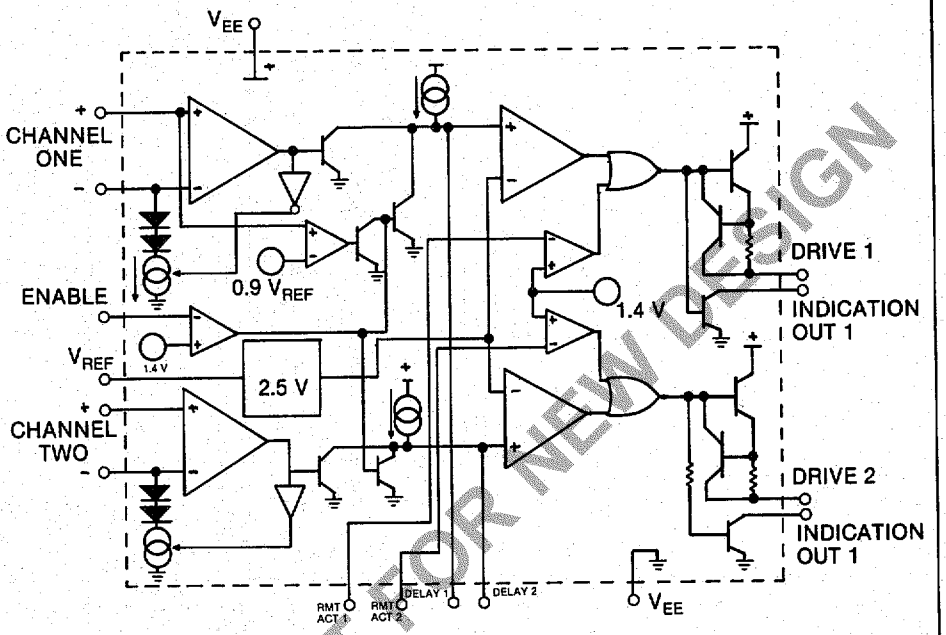

Fig. XVII

MC3425 MC3525

EQUIVALENT CIRCUIT

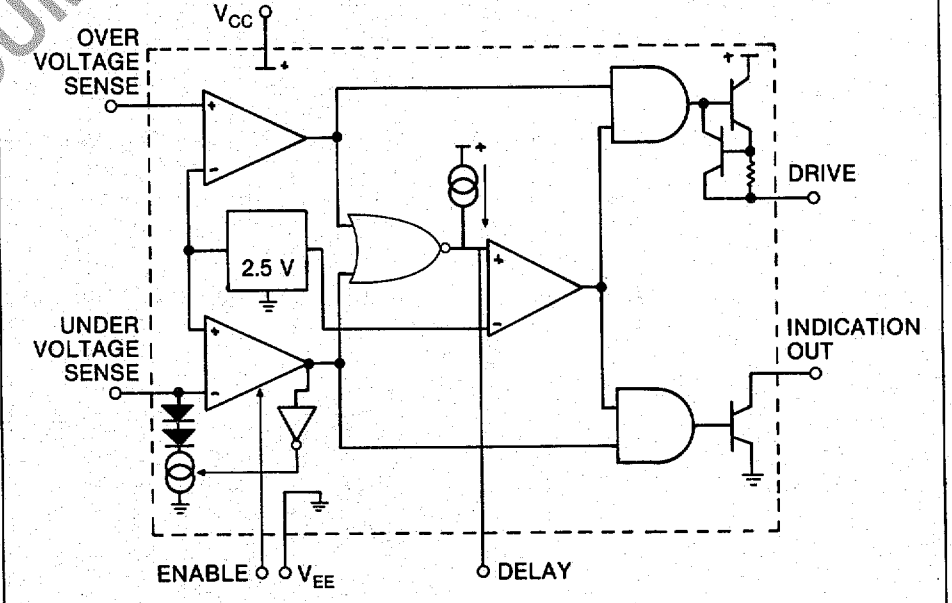

Fig. XVIII

MC3425 TYPICAL APPLICATION

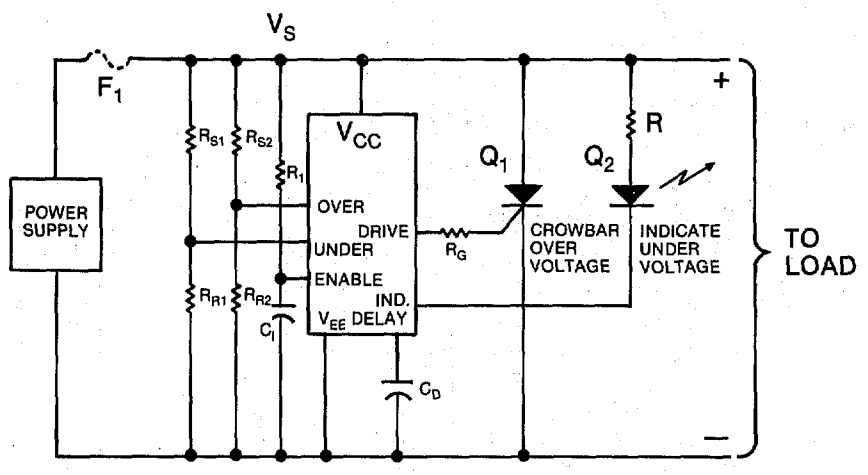

Fig. XIX

A typical application is shown Fig. XIX. Following the trip voltage required the value of resistors R and R_B will be selected following the formula [(see formula (1)]

$$V_{trip} = V_{REF}\left(1+\frac{RS}{RB}\right) = 2.6\ V\left(1+\frac{RS}{RB}\right)$$

To prevent a minimum drift of the circuit R_B value should be around 10 Kα and

$$R_E = \frac{T}{C_E L_n\left(\frac{VS}{VS - VE}\right)}$$

$$CD = \frac{Is\ Td}{V_{REF}} = \frac{200\ \mu A\ Td}{2.5\ V}$$

Conclusion

The use of a crowbar to protect sensitive loads from power supply overvoltage is quite common and, at the first glance, the design of these crowbars seems like a straight forward relatively simple task:

— How much overvoltage and for how long (energy) can the load take this overvoltage?

— Will the crowbar responds too slowly and thus no protect the load or too fast resulting in false, nuisance triggering?

— How much energy can the crowbar thyristor (SCR) take and will it survive until the fuse opens on the circuit breaker opens?

— Can the fuse adequately differentiate between normal current levels, including surge currents, and crowbar short circuit conditions?

All the users are involved about these problems; it is the attemps of this article to answer these questions...

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