Depletion-mode devices hike speed of MOS random access memory

Ion implantation process yields 1,024-bit by one-word array that has submicrosecond read cycle time and TTL compatibility, but requires no clock and isn't troubled by carrier injection problems

by Vernon McKenny, Mostek Corp., *Carrollton, Texas*

☐ Combining depletion-mode and low-threshold enhancement-mode devices, produced on a single chip by ion implantation, yields a high-speed, random access memory that requires no clock and overcomes the carrier injection problem that plagues dynamic MOS units. It also interfaces directly with transistor-transistor logic and fits into a 16-pin package instead of the usual 18-pin unit.

Depletion-mode transistors are used in the decoding, driving, and sense amplifier circuits for better speed-power products than enhancement-mode devices alone can provide. They also help speed up circuit operation by allowing wide voltage swings that decrease series resistances for fast capacitor charging. That's how the new 1,024-word by one-bit memory, designated the MK4006P, achieves read access and read cycle times of less than 400 nanoseconds, and a write cycle time below 650 ns.

The depletion-mode transistors also account for the elimination of precharging, along with the clock usually required to control the precharging that's commonly used to increase speed. With depletion-mode transistors as loads, necessary speed is attained without any need for precharging, resulting in one less pin on the package. Another is saved by eliminating a bias supply that's normally needed to prevent MOS transistors from injecting currents that discharge storage capacitors (see "Injection rejection" p. 84).

A depletion device's behavior when used as a load for an enhancement device in an inverter circuit is shown in Fig. 1. The depletion-mode device's gate (Fig. 1a) is tied to its source so that $V_{GS} = 0$, and the device is always on (since V_{GS} is less than the pinch-off voltage, 5 volts).

Thus, because of its characteristic curve, it acts as a constant current device; current, I_1, is approximately equal to $(W/L)_1 (V_p)^2$ where V_p is pinch-off voltage, a constant. Also shown are an inverter with an enhancement-mode device as a load (Fig. 1b) and an inverter with a resistive load (Fig. 1c).

The drain-source characteristics shown in Fig. 1d illustrate the V-I curve for the inverter transistor, Q_2, as one curve, since all inverter devices are the same. However, load lines for the three cases are different. As the load voltage decreases (V_{out} approaches V_{DD}), the resistive and enhancement loads provide decreasing charging current for the output load capacitance. For the resistor load, I_1 is $(V_{DD} - V_{out})/R_L$; for the enhancement mode load, I_1 is approximately $(W/L)_1 (V_{DD} - V_T - V_{out})^2$.

However, the charging current from the depletion load remains essentially constant until V_{out} is quite close to V_{DD}. This extra charging current will charge the load capacitance faster than the resistive and enhancement loads. Thus, since all three loads have been adjusted to have the same quiescent point, the depletion load offers the highest speed (Fig. 1e) for the same power dissipation. The resistive load is next fastest, while the enhancement load is slowest. Approximate transfer curves for the circuits (Fig. 1f) show the depletion load's sharpest transition.

The depletion load inverter can be represented as a pair of constant current sources (Fig. 2). If I_1 is made greater than I_2 either by giving depletion-mode transistor Q_1 a greater channel width-to-length ratio W/L, or by decreasing the drive, V_{in}, to Q_2, then V_{out} will approximate V_{DD} when the load capacitance charges. This is apparent from the current-source analogy: since I_1 is the larger, it controls charging and brings the output up to V_{DD}. This situation approximates that of a high-gain amplifier—a small change in V_{in} produces a large swing at the output. But if I_2 is greater than I_1, then V_{out} will charge toward V_{SS}.

For large-signal inputs, V_{in} is made positive enough so that Q_2, the inverter transistor, is strongly cut off; thus, $I_2 = 0$. In this case, the switching time of the negative-going edge of V_{out} is completely determined by I_1—it alone acts to charge the capacitor. The positive-going switching time is determined by $I_2 - I_1$. These times are expressed as the product of the voltage change, $V_{DD} - V_{SS}$, and the capacitance, divided by the charging current:

$$\Delta t\,(+) = \frac{(V_{DD} - V_{SS})\,C_L}{I_2 - I_1}$$

$$\Delta t\,(-) = \frac{(V_{DD} - V_{SS})\,C_L}{I_1 - I_2};\ (I_2 \cong 0)$$

Thus, to make the switching times equal, the device geometry ratio, $(W/L)_2/(W/L)_1$, must be adjusted so that $I_2 = 2I_1$.

Depletion-mode device advantages are even more apparent when three types of high-speed, high-ampli-

tude drivers are compared. These are a saturated inverter, a bootstrap inverter, and the depletion inverter.

The saturated inverter (Fig. 3a) has a poor speed-power product; most negative level is $V_{DD} - V_T$.

The bootstrap (Fig. 3b), finding greater popularity in MOS circuits, has a better speed-power figure of merit. An added advantage: it can attain V_{DD} at its output for a short time. However, normal diode leakage eventually will cause the bootstrapped node to drop to $V_{DD} - 2V_T$. But there's a way around this: a low-power MOS device can be placed in parallel with the bootstrapped load; V_{out} falls only to $V_{DD} - V_T$.

Depletion inverters offer an even better speed-power product than bootstrap inverters. They also attain V_{DD} as the most negative level and remain at that level indefinitely. This is particularly useful on an address line or in a TTL-compatible output buffer on a memory, where maximum negative amplitude must be maintained.

In the new RAM, depletion-mode devices provide faster switching inverters and gates in the row and column decoders, drivers, and buffers. Another useful feature is higher gain in the sense amplifiers. However, depletion-mode devices are not used in individual memory cells—those circuits primarily perform charge-steering junctions.

The storage matrix of the new RAM is organized (see block diagram, Fig. 4) into 32 rows and columns, or 1,024 cells. Basically, the row address decoder and driver signals combine with the read and write signals to enable the selected row for the read and write condition; the column decoder then uses these signals to control the flow of data into and out of the memory. Because of charge leakage, data must be refreshed every 2 milliseconds.

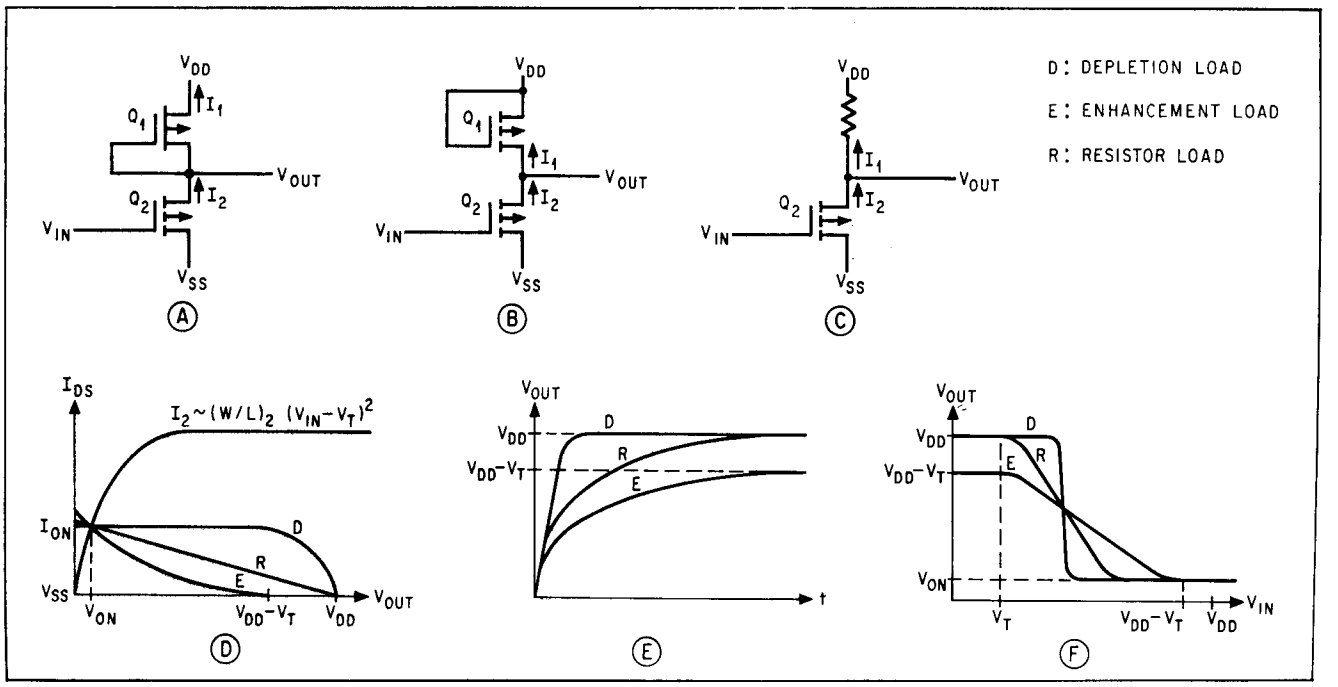
In a typical read-modify-write cycle, the row and column addresses are applied first. With a READ signal on the READ-WRITE line, the row decoder output, R_n, and the READ signal are combined to activate R_n READ for a selected row. All 32 cells in the selected row transfer their data to the sense amplifier inputs at each column's edge. The column decoder output connects the selected column's sense amplifier to the output through D_{out} SELECT. The reading operation is completed; time involved is the read access time.

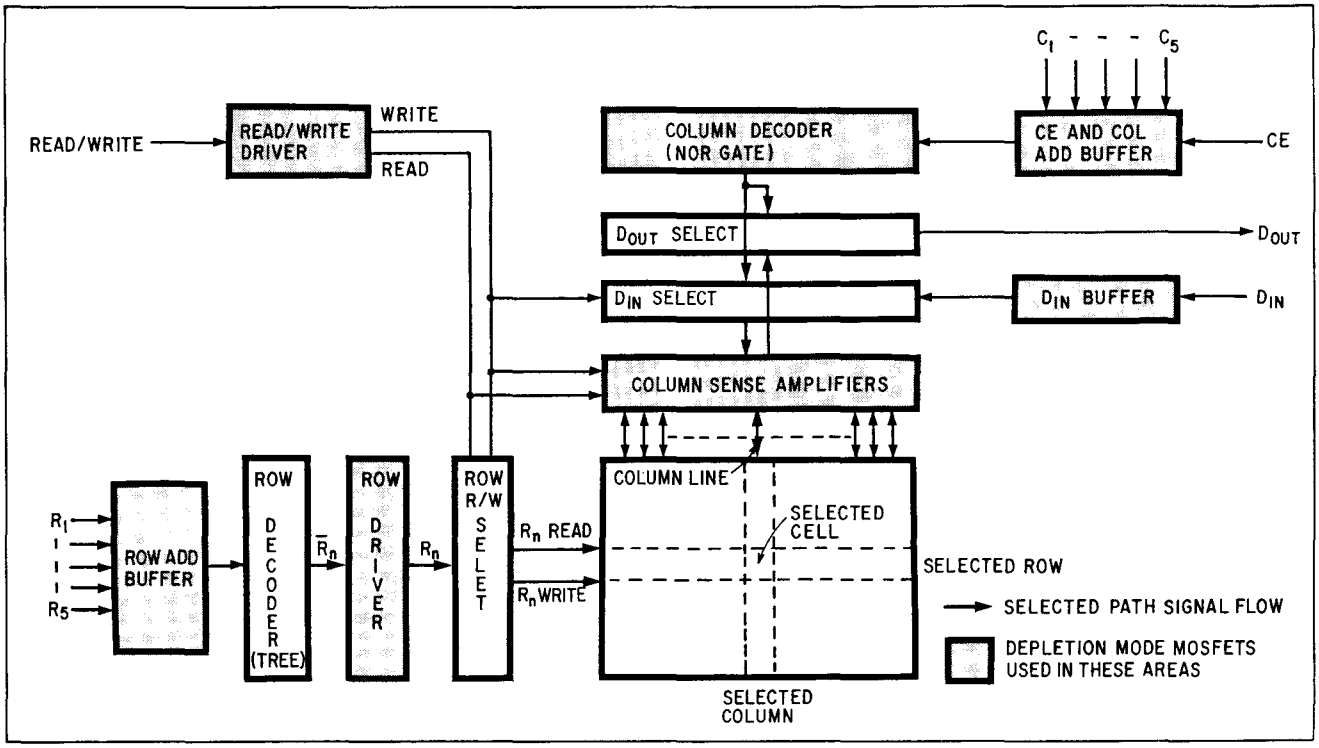
New data is fed in through D_{in}. The WRITE signal now is applied at the READ-WRITE input. Data from the previous read condition of the read-write-modify cycle unselected by the column decoder is returned to each cell's storage nodes; the new input data is combined with the column decoder output and applied to a sense amplifier to be written into a cell.

Operation of an individual cell is shown in Fig. 5. The memory chip requires only +5-V and −15-V supplies. The +5 V is for compatibility with TTL and DTL logic levels; the +5-V supply line serves as the return signal path, since there is no system ground connection to the chip. The +5 V substrate voltage is considered chip ground; −15 V thus becomes −20 V with respect to substrate ground.

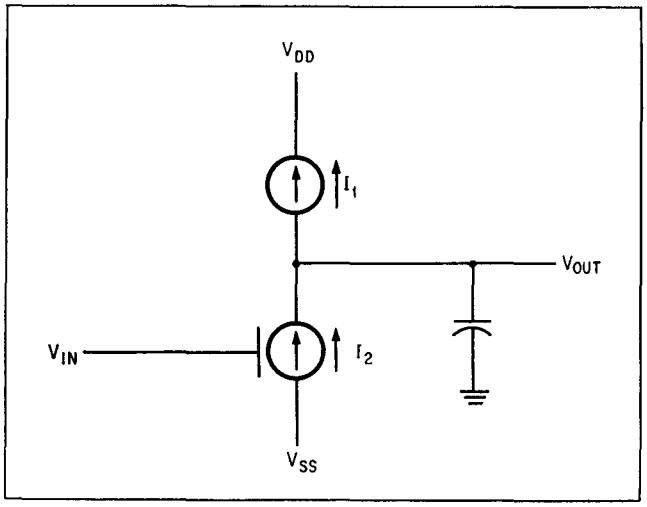
Note that the difference in voltage supplies for the DTL or TTL and the MOS chip also results in a difference in logic levels. A TTL or DTL logic 0 (0 V) results in an MOS 0 of +5 V; a TTL or DTL 1 (+5 V) results in an MOS 1 of −15 V. Thus, DTL and TTL use positive logic (logic 1 higher in level than logic 0) while

1. Depletion-mode load. Of three typical inverter circuits—depletion load, A, enhancement-mode MOS load, B, and resistor load, C—depletion type is fastest because it operates at constant current for greater range of voltages, as in D. Load current helps change output load capacitance faster, E, and transfer characteristic, F, shows sharper transition for depletion-mode circuit.





4. Full memory. Shaded blocks indicate sections of RAM that use depletion-mode devices. Paths shown in color indicate signal flow for selected row and column.



2. Equivalent. Operation of depletion-mode inverter circuit is equivalent to two constant current sources, where larger of the two currents determines rate at which an output capacitor charges up.

the MOS chip uses negative logic (logic 1 lower in level than logic 0). All logic diagrams shown are in terms of negative logic: for example, a NOR gate is equivalent to a positive-logic NAND gate.

At the storage node, A in Fig. 5, the capacitance, shown dashed in color, is the total capacitance to substrate at that point, not an actual physical capacitor. The same is true for the capacitor shown at node B at the input of the sense amplifier, which temporarily stores information during the write cycle.

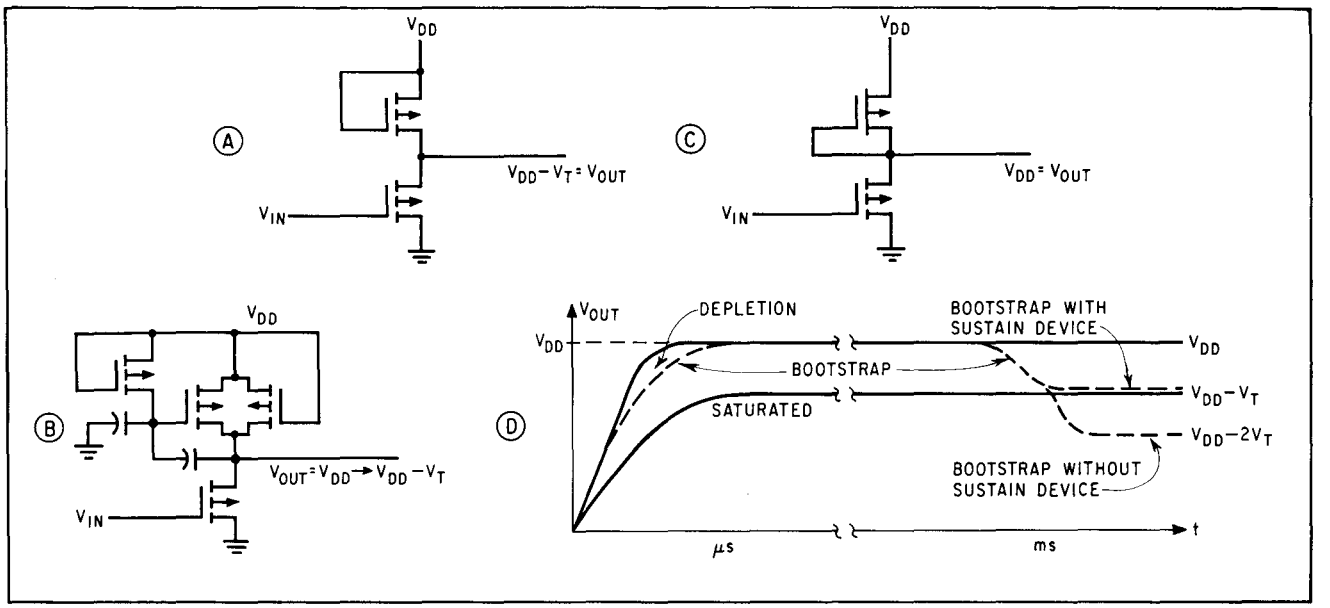
The storage capacitor holds a negative charge for a positive logic 1 entered at the data input, D_{in}. With a positive logic 0, there is no charge on the capacitor. To understand how the charge gets to the capacitor, consider a read cycle and then a write cycle.

In a read cycle, suppose R_n, R_n READ, R_n WRITE, C_m, and WRITE are at V_{SS} (0 V) and READ is at V_{DD}, —20V. When the row address is applied, R_n and R_n READ go negative to about —14 V, which is $V_{DD} - V_T'$ where V_T' includes threshold voltage of the enhancement-mode device (—1.5 V), body effect, and the effect of limited charging time.

Body effect, inherent in all MOS structures, takes into account the increase in threshold voltage caused by the bias voltage, V_{BS}, applied between source and bulk material. If $V_{BS} = 0$ V, then the threshold voltage is the normally specified value, —1.5 V in the MK4006P. But if V_{BS} has a finite value, the gate voltage must be increased beyond this nominal threshold if conduction is to occur. The increase in threshold voltage is approximately proportional to the square root of V_{BS}. In this case, the bias between bulk and source creates a 2-V increase in threshold voltage. Thus, $V_{DD} - V_T'$ is reduced from —18.5 V to about —16.5 V. Because the time for charging the capacitance is limited, this voltage is further reduced to —14 V.

R_n READ turns on Q_1, connecting storage-node transistor Q_3 to the column line so that the charge on the storage capacitor is read out.

If there is no charge on the capacitor, Q_3 does not turn on and the column line simply charges through transistor Q_6 to —14 V. Since the READ pulse also turns on Q_9, the sense amplifier input node B thus is connected to the column line so that the voltage



3. Widest swing. Depletion-mode inverter circuit, C, attains V_{DD} as most negative output level, while bootstrap circuit, B, and enhancement-mode inverter, A, do not offer as wide a range on a dc basis. Depletion-mode circuit also has best speed-power product.

change on the column line can be read out.

If the storage capacitor were charged to a negative voltage, Q_3 would be turned on; the column line then would discharge toward ground, to about −10 V ($V_{DD} - V_T' - 4$ V, where 4 V is dropped across Q_6).

Depletion mode transistors provide high gain to the sense amplifier and decrease drive requirements on the storage cell. The sense amplifier is designed with a built-in offset voltage of about −12 V—a value exactly between −10 V and −14 V, the two possible final values of the column line. The sense amplifier's gain is adjusted so that its input need change by only 0.5 V to drive the output to −14 V or 0 V.

This property allows the small devices in the storage cell to drive the high-capacitance column line over a maximum swing of only ±2.5 V instead of the 10- to 15-V swing common in other memories. To achieve a further increase in speed, column line capacitance is reduced by the −12 V bias (the usual 0-V bias produces p-n junction capacitances about three times higher). The two effects—reduced capacitance and reduced voltage swing—improve column line response time by a factor of 10 or more compared with conventional circuits.

The memory can be operated in a continuous READ mode by holding the READ-WRITE line at logical 1 (0 V), while providing the CHIP ENABLE signal. Within typically 300 ns after the address change, all switching has occurred, and thus output data becomes valid.

Data readout is nondestructive, and can continue until the storage capacitor's charge starts to degrade through p-n junction leakage. Under worst-case voltage conditions and at elevated temperatures, the data will remain on the storage capacitor for at least 2 ms. Therefore, data must be refreshed every 2 ms. Since the refreshing is accomplished for an entire row at a

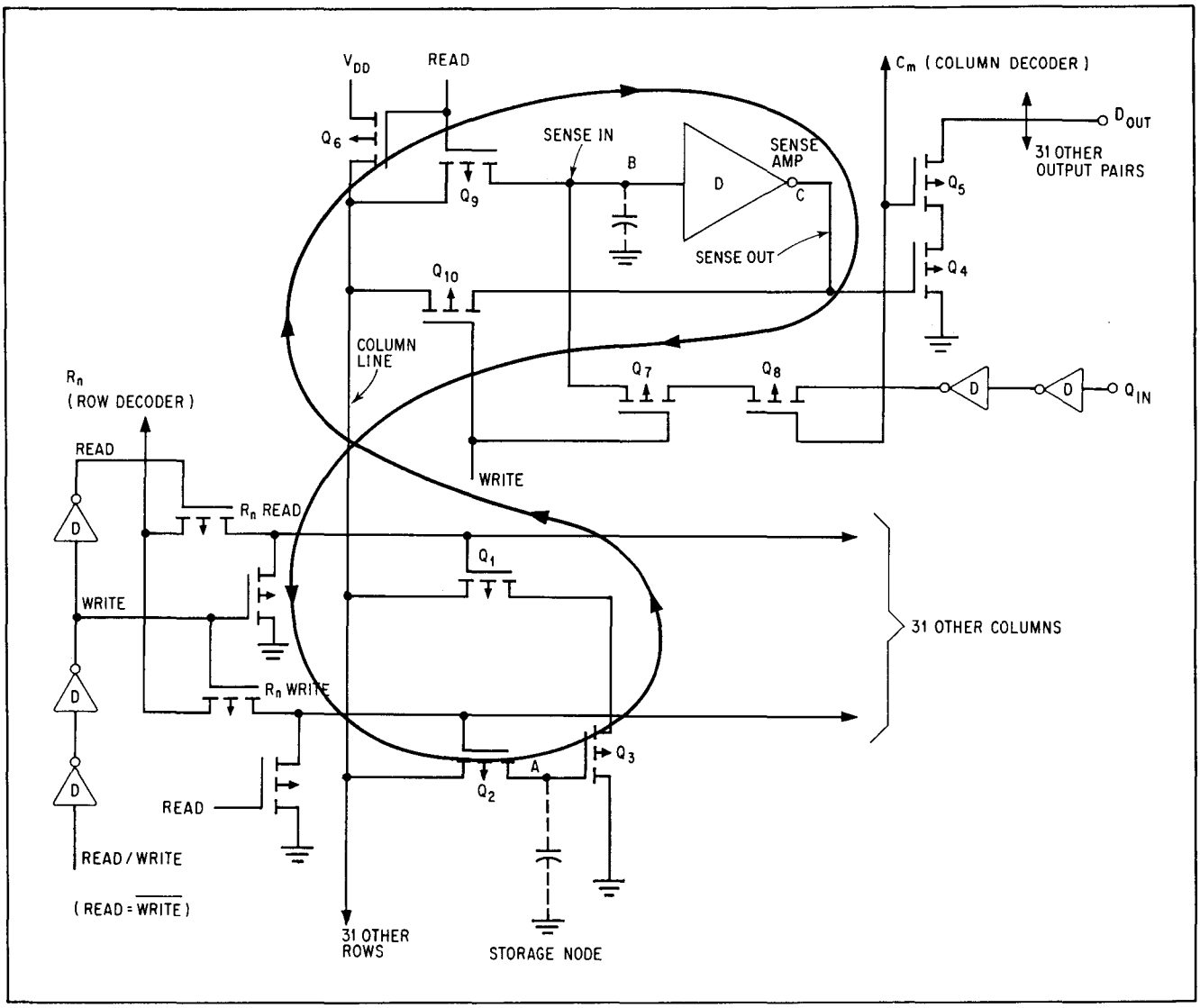
Depletion modes and ion implants

MOS circuits generally use enhancement-mode transistors, in which no conduction between drain and source takes place with zero gate-to-source voltage. Such devices are commonly fabricated on an n-type substrate and operate with a negative gate voltage to form a p-type channel between the diffused p-type drain and source regions. To form a conductive channel, the applied negative voltage must exceed a certain threshold, ranging from about −1.5 volts for low-threshold devices up to −4 or −5 v.

In the depletion mode device, however, a conductive channel is formed when $V_{GS} = 0$. To turn off a p-channel device, the gate-source voltage must be increased to about +5 v, the pinch-off voltage, which corresponds to the threshold voltage. To form a p-channel depletion-mode transistor, light p-type doping of the channel is required. Proper doping has been difficult to achieve chemically because the oxide grown after the doping process tended to absorb impurities at the high temperatures required for oxide growth. However, with ion implantation, the oxide already is in place when the dopant ions are implanted.

In the MK4006P 1,024 x 1 RAM, two ion implant steps are used with the p-type dopant, boron. The first one lowers the enhancement-mode thresholds from −4 v to a nominal −1.5 v, and the second implant produces the depletion-mode transistors.

In the future, ion implantation also could be used to manufacture precisely controlled complementary MOS circuits as well as n-channel devices free of unwanted, parasitic, depletion-mode devices, while at the same time producing depletion-mode devices in the desired locations. Such combinations could produce RAMs as large as 2,000 to 8,000 bits on a single chip with access times less than 100 nanoseconds.



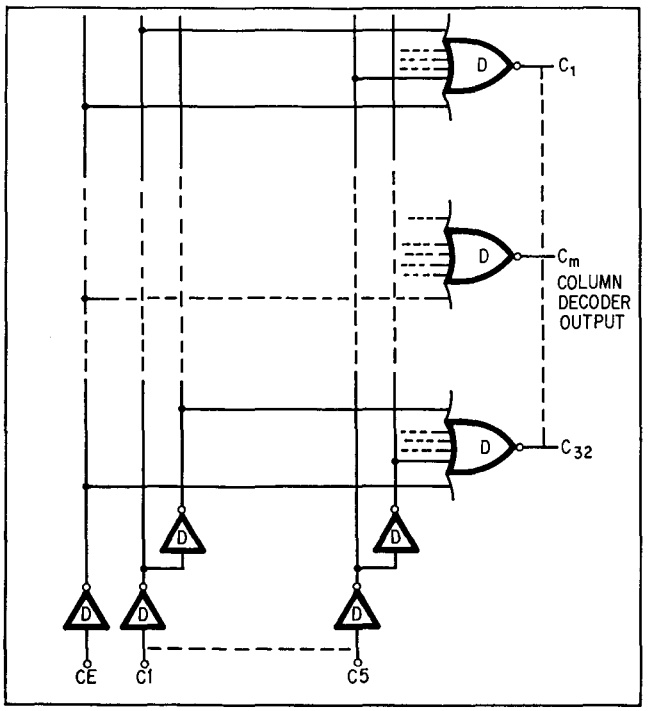
5. Single cell. Information entered at D_{in} is stored at node A. In refresh mode, data at A travels in figure-eight path from A to column line to node B, through sense amplifier, and back to the column line to refresh A through Q_2. Circuits with depletion-mode devices are designated D.

Injection rejection

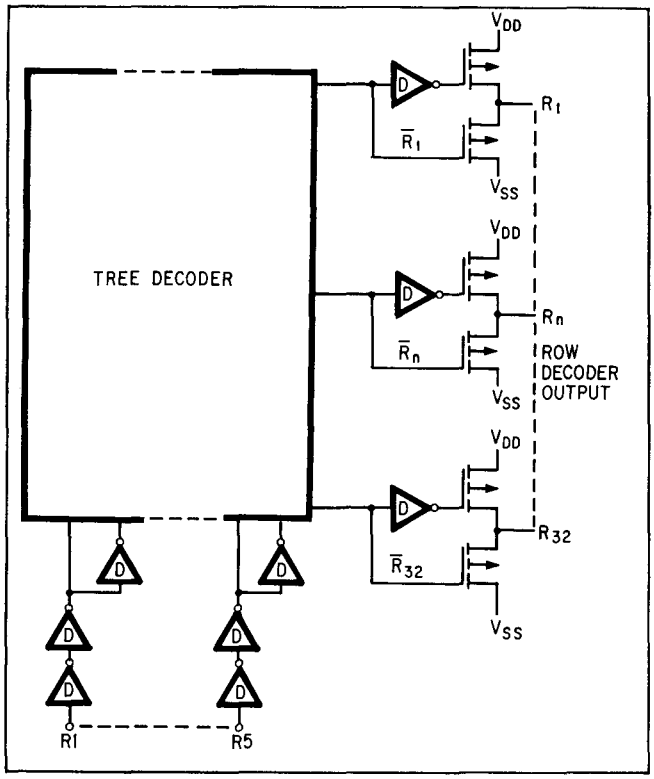
The carrier injection problem in some conventional MOS arrays tends to discharge storage capacitors resulting in lost data. Injection occurs because an MOS device can behave like a parasitic pnp lateral bipolar transistor when one p-diffusion region acts as an emitter and a nearby p area acts as the collector. If the "collector" area is connected to a storage node, injected current can reduce the charge and destroy the stored information. Since capacitances used for storage purposes amount to only a fraction of a picofarad, only a small amount of injected current can disrupt operation with the extra charge.

Generally, two types of signals can cause a p-diffusion to go positive with respect to its surrounding n material and begin injecting carriers. Ringing or spikes from an input line can forward bias the junction, but this effect can be isolated and remedied with appropriate external filters. More difficult to deal with is a pulse internally coupled to the p area by the capacitance between the gate and the drain or source pad. The usual remedy is application of an extra bias that maintains the substrate positive with respect to the drain and source p diffusions. However, this requires an extra pin on the package.

The MK4006P RAM avoids the problem with a careful design of the capacitance overlap area at the storage nodes. Also helping out is close control of the rise and fall times at the storage nodes. Because it doesn't use the extra bias, the RAM can do with one less pin per package. Another is eliminated by doing away with a clock, so that the RAM can fit into a standard 16-pin package instead of an 18-pin unit.



6. Column decoder. Depletion-load inverters drive depletion-mode NOR gates. Decoder uses 32 six-input NOR gates. Selected column is driven by one gate (the only one that provides an output at V_{DD}). D indicates circuits with depletion-mode devices.



7. Row decoder. Tree decoder drives 32 depletion-load inverters and push-pull buffers. Selected row is driven to V_{DD}—V_T'. D indicates circuits with depletion-mode devices.

time, a total of 32 REFRESH cycles are required to completely refresh all the bits on the chip. Column address is ignored during the REFRESH cycle.

To refresh the cell of Fig. 5, information at the storage node first is transferred to the sense amplifier output as in the read cycle. The READ-WRITE input then is changed to a WRITE condition. This causes the READ line to discharge to 0 V and the WRITE line to charge to —20 V. The column load resistor, Q_6, then is turned off and node B at the sense amplifier input is isolated from the column line. Q_{10} connects the column line to the sense amplifier output. The data that had been on the column line is stored on the capacitance at node B. R_n READ goes to 0 V and R_n WRITE goes to —14 V, turning Q_1 off and Q_2 on. The storage capacitor therefore is connected back to the column line and receives the information stored at the output of the sense amplifier. If the storage node was previously at 0 V, it stays at 0 V. If it had been at a negative voltage, it will be restored to —11 V (V_{DD} — 2 V_T'). At this point, the READ-WRITE input is changed back to the READ condition; the row address is changed, and REFRESH for the new row proceeds.

Although all the nodes in a row are refreshed simultaneously, the WRITE mode operates on only one node at a time. During the WRITE cycle, all the cells in the selected row are automatically refreshed except the one selected for a new data input.

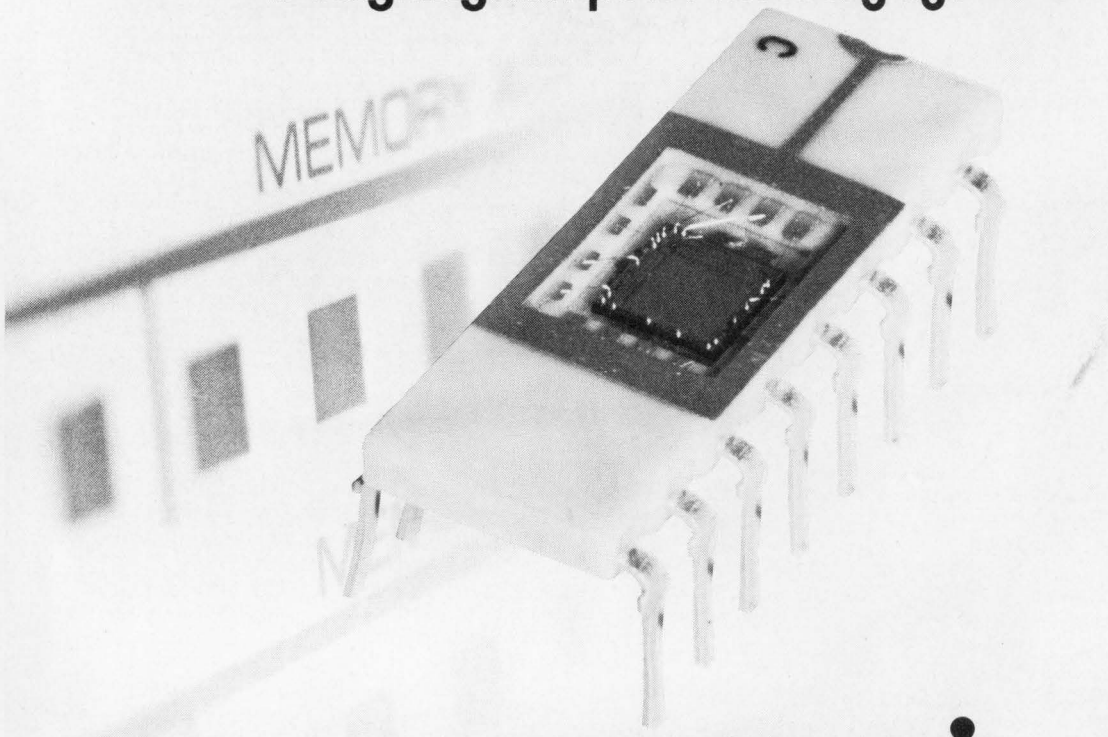
For this cell, the C_m line, instead of being at 0 V as in all the other columns, is put at —20 V by the column address decoder. Hence, the input data buffer, through transistors Q_7 and Q_8, can overpower the information stored on node B. The sense amplifier receives this new input and delivers it back to the storage cell through a process similar to REFRESH.

Depletion-load NOR gates are used in the column decoder (Fig. 6). Each of the 32 six-input gates drives a column line and carries input from various combinations of true and complement data for the five-column address inputs. The sixth gate's input is the complement of the CHIP ENABLE external input.

In the circuit (Fig. 6), if CE is at a positive logic 1 (0 V), the NOR gate produces 0 V at its output regardless of the address information. All column decoder outputs are clamped at 0 V and the chip is disabled. To enable the chip, the CE input is changed to —5 V, positive logic 0, and one of the 32 six-input NOR gates will have an input of all six lines at 0 V. This gate will turn on its column line, C_m, to —20 V.

Depletion-load gates also speed up row decoding, where signals have a longer delay path to their output than the column decoding signals. The individual row-decoder stages must have less delay and switching times than the corresponding column decoder units. The TTL level input signals first are amplified and then used to generate five pairs of address signals which feed the tree decoder. This device has 32 output lines feeding buffers, which in turn feed the 32 row address lines (R_n). Each buffer consists of a depletion mode inverter driving an enhancement push-pull. □

Designing computer memory systems?



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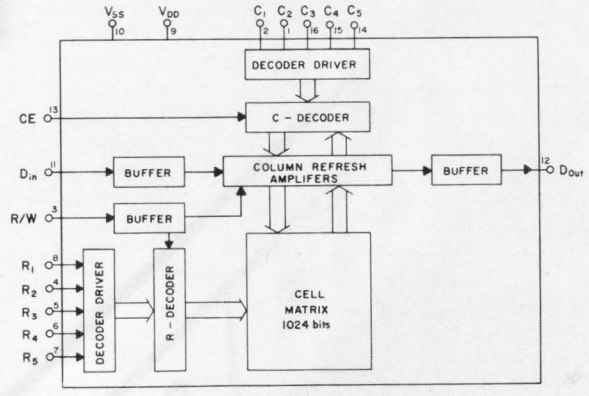
MK 4006 P FUNCTIONAL DIAGRAM



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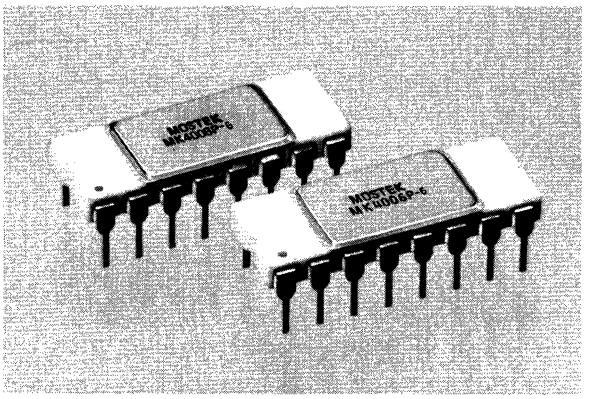
- ☐ Standby power: under 50 mW
- ☐ 16-pin standard CDIP
- ☐ Supply voltage: +5V and −12V



DESCRIPTION

This is a family of MOS dynamic 1024x1 random-access memories having identical functional characteristics, differing only in speed. Access time in the MK 4006 P-6 is less than 400 ns; in the MK 4008 P-6 less than 500.

Full address decoding is provided internally. Information is read out non-destructively (NDRO) and has the same polarity as the input data.

TTL/DTL compatibility at all inputs allows economical use in small systems by eliminating the need for special interface circuitry. Large main-memory applications also benefit from the low drive-voltage swings as well as the packing density afforded by the standard 16-pin dual-in-line packaging and low standby power.

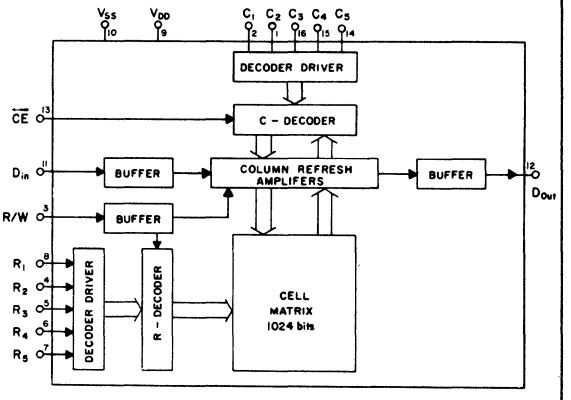
The internal memory element of this RAM is a capacitance, and refreshing must be periodically initiated (see TIMING). However, all internal decoding and sensing is static, so that precharging or clocking normally associated with dynamic memories is not required. From the user's viewpoint, memory control and addressing are essentially those of a static device.

Noise suppression measures normally employed in DTL or TTL systems are sufficient. High voltage input swings and high peak-current line drivers are unnecessary for driving memory inputs, and the memory itself does not exhibit large supply current transients.

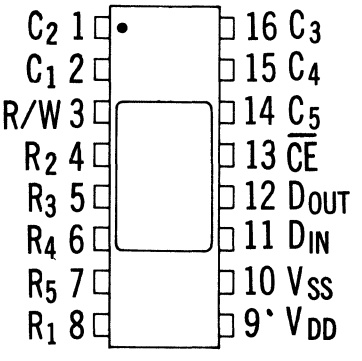
Data output is single-ended to minimize propagation delay. Output current is sourced from V_{SS} (+5V), and easily sensed using readily available components. A logic 1 at the output terminal appears as a 5,000 Ohm resistor (MK 4006) to +5V; a logic 0 as an open circuit.

The performance of this RAM is made possible by Mostek's ion-implantation process. In addition to offering low threshold voltages for TTL/DTL compatibility and utilizing conventional P-channel processing, ion-implantation allows both enhancement (normally OFF) and depletion (normally ON) MOS transistors to be fabricated on the same chip. By replacing conventional MOS load resistors with constant-current depletion transistors, operational speeds and functional density are increased.

FUNCTIONAL DIAGRAM



PIN CONNECTIONS



ABSOLUTE MAXIMUM RATINGS

Voltage on any pin relative to V_{SS} ..... +0.3 to −20V

Operating Temperature ..... 0°C to +70°C

Storage Temperature Range ..... −55°C to +150°C

RECOMMENDED DC OPERATING CONDITIONS

(0° C $\leq T_A \leq$ 70°C)

	PARAMETER	MK 4006P-6 MIN	MK 4006P-6 MAX	MK 4008P-6 MIN	MK 4008P-6 MAX	UNITS	NOTES
V_{SS}	Supply Voltage		+4.75		+5.25	V	
V_{DD}	Supply Voltage		−11.4		−12.6	V	
V_{IL}	Input Voltage, Logic 0				+0.8	V	
V_{IH}	Input Voltage, Logic 1		$V_{SS}-1$		V_{SS}	V	
V_{SB}	Standby Supply Voltage (Fig. 4)		$V_{SS}-4$		$V_{SS}-6$	V	Note 1

Random Access Memories

RECOMMENDED AC OPERATING CONDITIONS[2]

(0° C $\leq T_A \leq$ 70°C)

	PARAMETER	MK 4006P-6 MIN	MK 4006P-6 MAX	MK 4008P-6 MIN	MK 4008P-6 MAX	UNITS	NOTES
t_{RC}	Read Cycle Time (Fig. 1)	400		500		ns	
t_{WC}	Write Cycle Time (Fig. 2)	650				ns	t_{WP}=250 ns
				900		ns	t_{WP}=400 ns
t_{WP}	Write Pulse Width (Fig. 2)	250				ns	t_{AW}=400 ns
				400		ns	t_{AW}=500 ns
t_{AW}	Address-to-Write Delay (Fig. 2)	400				ns	t_{WP}=250 ns
				500		ns	t_{WP}=400 ns
t_{DLD}	Data-to-Write Lead Time (Fig. 2)	300				ns	t_{WP}=250 ns
				400		ns	t_{WP}=400 ns
t_{RDLY}	Refresh Time (Fig. 3)		2		2	ms	See Note 3.
t_{CDPD}	Chip-Disable-to-Power-Down Delay (Fig. 4)	200		200		ns	See Note 1 See Note 4

DC ELECTRICAL CHARACTERISTICS

(V_{SS} = +5V ± 5%; V_{DD} = −12V ± 5%; 0°C $\leq T_A \leq$ 70°C unless otherwise noted)

	PARAMETER	MK 4006P-6 MIN	MK 4006P-6 MAX	MK 4008P-6 MIN	MK 4008P-6 MAX	UNITS	NOTES
I_{SS}, I_{DD}	Supply Current: At T_A=0°C		32		32	mA	Output
	At T_A=70°C		27		27	mA	Open
P_{SDBY}	Power Dissipation, Standby		50		50	mW	$V_{SS}-V_{DD}$ = 5V; Note 1
I_{IH}	Input Current, Logic 1. Any Input	−5	+5	−5	+5	μA	$V_I=V_{SS}-1V$
I_{IL}	Input Current, Logic 0, Any Input	−5	+5	−5	+5	μA	V_I=0.8V
I_{OH}	Output Current, Logic 1	1.0		0.8		mA	Note 5
I_{OL}	Output Current, Logic 0		5		5	μA	

AC ELECTRICAL CHARACTERISTICS

($V_{SS} = +5V \pm 5\%$; $V_{DD} = -12V \pm 5\%$; $0°C \leq T_A \leq 70°C$ unless otherwise noted)

	PARAMETER	MK 4006P-6 MIN	MK 4006P-6 MAX	MK 4008P-6 MIN	MK 4008P-6 MAX	UNITS	NOTES
t_{ACCESS}	Read Access Time (Fig. 1 & 1-A)		400		500	ns	Note 2
t_{CE}	Chip Enable Time (Fig. 1A & 5)		350		450	ns	Note 2
t_{CD}	Chip Disable Time (Fig. 1A & 5)		350		450	ns	
C_I	Input Capacitance, Any Input		5.0		5.0	pF	$T_A=25°C$; $V_I=V_{SS}$; f=1MHz
C_O	Output Capacitance		10		10	pF	$T_A=25°C$; $V_O=V_{SS}-5V$; f=1MHz
C_{DD}	V_{DD} Capacitance		75		75	pF	$T_A = 25°C$; Note 6

NOTES:

(1) Applies to MK 4006-6 and MK 4008-6 only.

(2) Measurement Criteria: Input voltage swing, all inputs: 0.8V to $V_{SS} - 1$
Input rise and fall times: 20 ns
Measurement point on input signals: +1.5V above ground
Measurement point on output signal: +60 mV above ground, using a load circuit of a 200 ohm resistor in parallel with a 100 pF capacitance connected to ground.

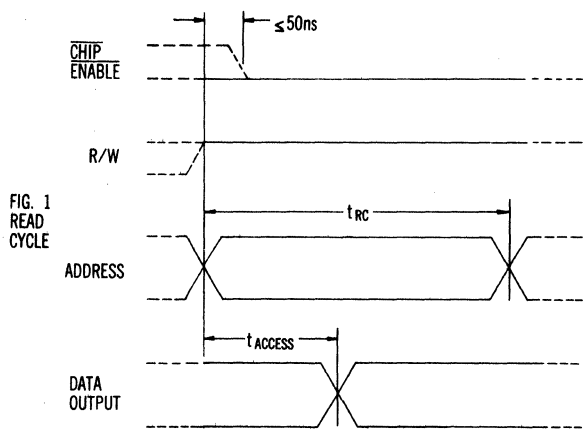
(3) t_{RDLY} is the time between refresh cycles for a given row address.

(4) The rise time of V_{DD} must not be faster than 20 ns.

(5) Steady-state values. (Refer to Fig. 1A for clarification)

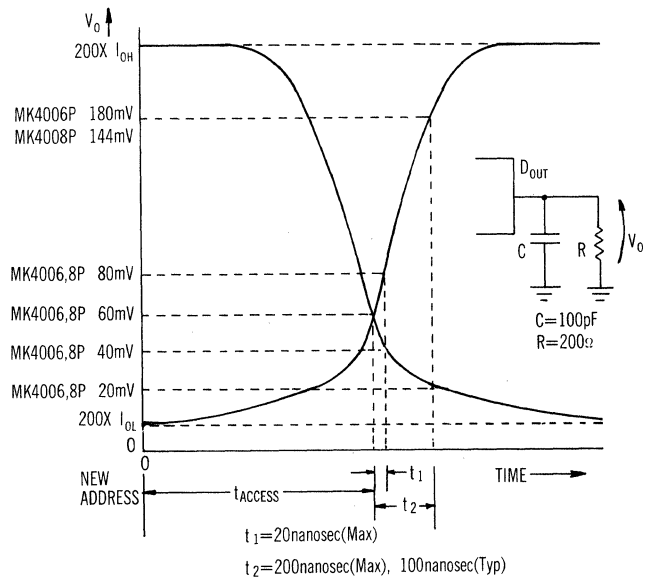
(6) Average capacitance of the V_{DD} terminal relative to the V_{SS} terminal. Measured by switching the V_{DD} terminal from OV to —12V with an applied $V_{SS} = 5V$. Peak I_{DD} is observed and the circuit replaced by a capacitance which yields the same peak current as the circuit under test.

TIMING (Note 2)



READING (Fig. 1)

Reading is accomplished with the Read/Write input held high. Data output directly follows the application of an address. As long as the address is unchanged and the chip enabled, data output will remain valid until the next refresh cycle. Input addresses can be changed as soon as output data is accessed. Any address can be applied repetitively without degrading stored data, providing that the refresh period of 2 ms is observed.



ACCESS TIME (Fig. 1-A)

Figure 1-A illustrates the measurement of access time after application of new address for the MK 4006 P and the MK 4008 P.

AC ELECTRICAL CHARACTERISTICS

($V_{SS} = +5V \pm 5\%$; $V_{DD} = -12V \pm 5\%$; $0°C \leq T_A \leq 70°C$ unless otherwise noted)

	PARAMETER	MK 4006P-6 MIN	MK 4006P-6 MAX	MK 4008P-6 MIN	MK 4008P-6 MAX	UNITS	NOTES
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C_O	Output Capacitance		10		10	pF	$T_A=25°C$; $V_O=V_{SS}-5V$; f=1MHz
C_{DD}	V_{DD} Capacitance		75		75	pF	$T_A = 25°C$; Note 6

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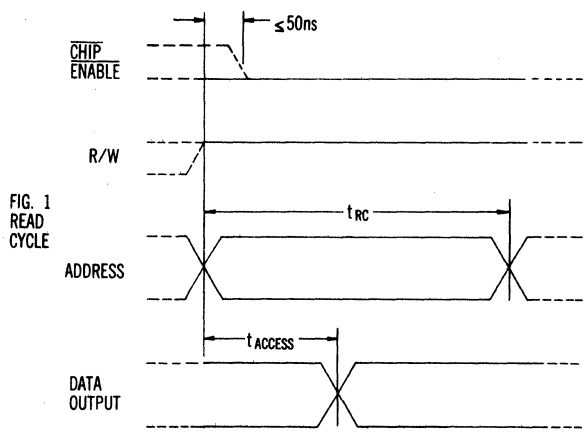
TIMING (Note 2)



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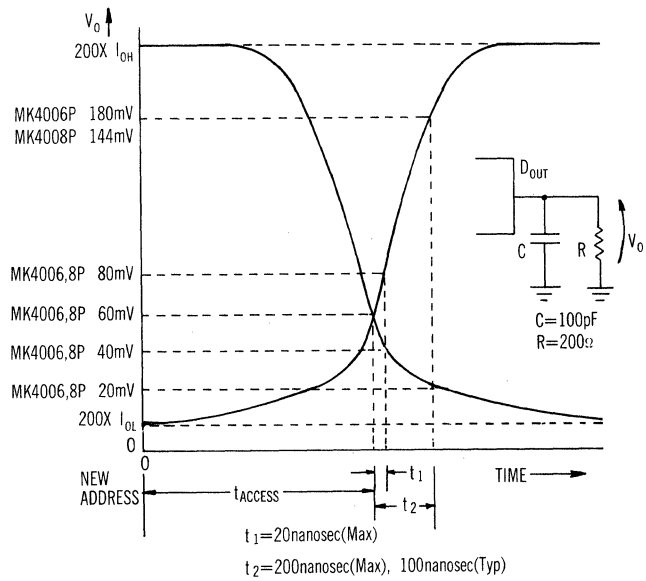


ACCESS TIME (Fig. 1-A)

Figure 1-A illustrates the measurement of access time after application of new address for the MK 4006 P and the MK 4008 P.

TIMING
(Note 2)

CHIP ENABLING (Fig. 5)

The negative-going $\overline{CE}$ enables the chip, and output data becomes valid within t_{CE} time. Return of the $\overline{CE}$ input to logic 1 disables the chip; data out remains for t_{CD} time.

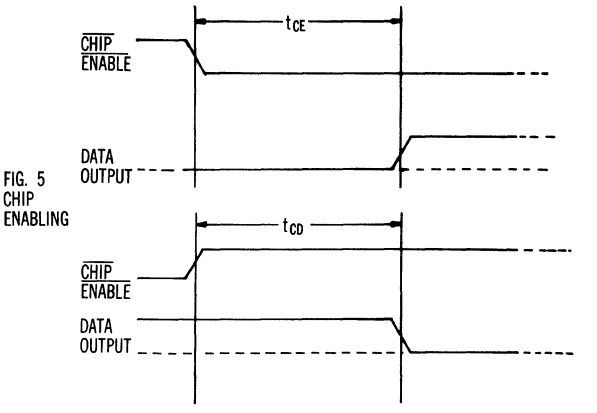


FIG. 5 CHIP ENABLING

TESTING CONSIDERATIONS

For a complete discussion of testing this memory, see Mostek's Applications Note AN-103.

The functional diagram (Fig. 6) indicates signal flow for selected row and column.

A simplified listing of functional tests is shown in Table 1. (high = Logic 1; low = Logic 0)

Tests are performed in an address sequence which requires the maximum number of changes in the row and column decoders between addresses. Addressing Rows 0 through 31 is accomplished by using the binary equivalent of the row address. The internal organization of the memory matrix requires the logic shown in Fig. 7 for column addresses; this logic provides the necessary conversion from inary equivalent to column address.

Fig. 6

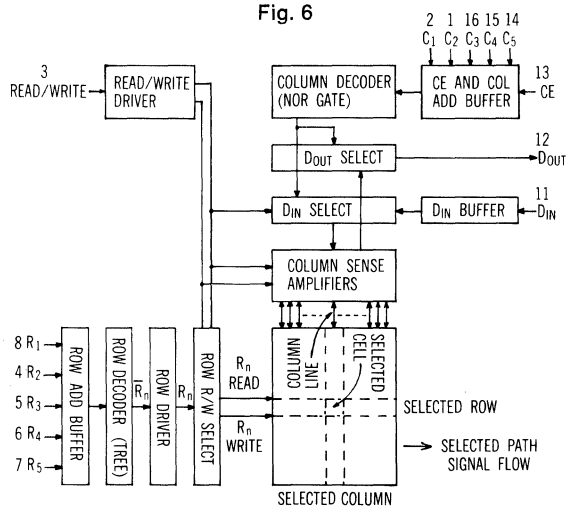


Fig. 7

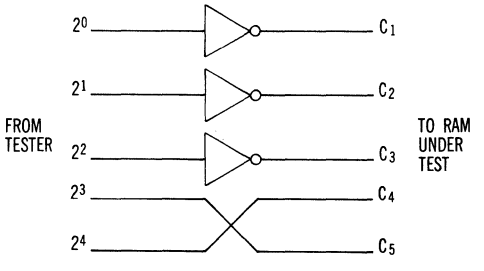
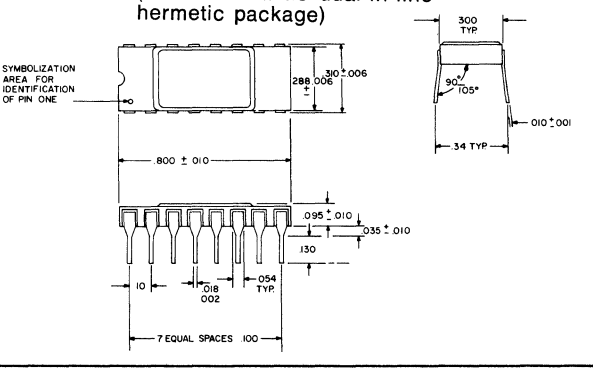


TABLE 1: FUNCTIONAL TESTS (SIMPLIFIED)

TEST DESC.	TEST SEQ.	OPER.	CHIP ENABLE	DATA INPUT	COMPARE DATA
Bit & Decoder Test[1]	First	Write	E	Parity	
	Next	Read	E		Parity
Column Shorts & No Write During Disable	First	Write	E	V-Bar	
	Next	Write	D	$\overline{\text{V-Bar}}$	
	Next	Read	E		V-Bar
Row Shorts, No Read During Disable, & Max. Power	First	Write	E	H-Bar	
	Next	Read	D	1	0
	Next	Read	E	0	H-Bar
Access Time, Refresh, Write Cycle, & Standby[1]	First	Write, Write	E	V-Bar, $\overline{\text{V-Bar}}$	
	Next	Delay	D	0	
	Next	Read	E		$\overline{\text{V-Bar}}$
Disturb Test	First	Write Row of 1's	E	1	
	Next	Write Adj. Row with 0's	E	0	
	Next	Continue Writing Same Row for Max. Refresh Delay	E	0	
	Next	Read original Row of 1's	E		1

1. Test performed as shown and repeated with complementary data.

PACKAGE (16-lead ceramic dual-in-line hermetic package)



ORDERING INFORMATION

MK 4006 P-6 1024x1 RAM/w/400 ns access time with power down
MK 4008 P-6 1024x1 RAM/w/500 ns access time with power down

APPLICATION

SENSE AMPLIFIERS FOR MK 4006/4008 RAM's

Since the interface circuitry used to convert memory signals to system logic levels strongly influences system access times, this circuitry should always be designed to meet the speed and cost requirements of the particular application.

Fig. 1-A (See "Timing") is shown to assist in the design of such amplifiers. This figure shows output voltage (across a specified load) vs. time from application of new address with several points indicated where specified voltage levels are referenced to specific times. Although all the various access times vs. output current levels cannot be shown, a few guidelines are given for interpolation between the specified points.

In Fig. 1-A, the two points at t_{access} + 20 nsec give the minimum "1" level and the maximum "0" level for this particular time (80 mV and 40 mV respectively). At t_{access} + 200 nsec, voltage levels are specified for the 90% and 10% points of the minimum "1" and maximum "0" levels.

INTERPOLATION

These interpolation guidelines are selected to give the designer a high level of confidence in his sense amplifier design.

From O to 1: This portion of the access curve can be estimated by two linear portions: (1) from the 60 mV to the 80 mV level; and (2) from the 80 mV level to 180/144 mV level.

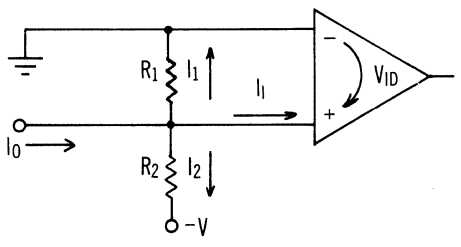
From 1 to O: This portion of the access curve can be estimated by a semi-logarithmic plot decreasing 20 mV for each decade or 10 nsec of time added to t_{access}, with the end points being 60 mV at 2 nsec and 20 mV at 200 nsec.

EXAMPLE: Let us consider how this data can be used in a sense amplifier design utilizing the 75107/108 Dual-Line-Receiver-and-Driver.

The manufacturer's data sheet for this circuit shows us that at strobe time, three conditions of the line receiver can exist: (1) the input voltage differential can be more positive than 25 mV, resulting in a logic 1 at the output (Input differential voltage is referenced to the inverting terminal); (2) the input differential can be more negative than 25 mV, resulting in a logic O at the output; (3) the input differential is less than 25 mV (absolute value), which will result in an output of an undetermined state. In other words, the line receiver has a 50 mV "window" centered around zero, and a signal must fall outside this window to provide reliable information at the output.

The standard configuration for using the 75107/108 as a sense amp is shown in Fig. 8 with the voltage and current conventions used in this analysis.

FIG. 8: Illustrating use of 75107/108 Line Receivers as sense amplifiers for the MK 4006/4008 P.



From the worst-case access at the *chip* level, one can use the interpolation technique described above to determine maximum "O" current level [I_{OLC}(MAX)] and the minimum "1" current level [I_{OH}(MIN)].

However, to use a worst-case approach to this design, in addition to the chip's characteristics, one must include in the "O" level current the effect of leakage from all outputs that are wired together. Also the input currents required by the 75107/108 (75 mA and 10 mA) must be included. Let us call this I_{OLT}(MAX):

$$I_{OLT}(MAX) = I_{OLC}(MAX) + (N\text{-}1)\ (5\ \mu A) \quad [1]$$

where N = number of outputs wired together

Using the maximum zero level at the line receiver input ($V_{ID} \leq -25mV = V_{ID}^{-}$), the following equation is derived:

$$I_{OLT}(MAX) = I_1 - I_2 + I_{IL}(MIN)$$

and $I_{IL}(MIN) = O\ \mu A$ [2]

therefore:

$$I_{OLT}(MAX) = \frac{V_{ID}^{-}}{R1} + \frac{V + V_{ID}^{-}}{R2} \quad [3]$$

Using the minimum "1" level at the line receiver input ($V_{ID} \geq +25\ mV = V_{ID}^{+}$), the equation becomes

$$I_{OH}(MIN) = I_1 - I_2 + I_{IH}(MAX) \quad [4]$$

and $I_{IH}(MAX) = 75\ \mu A$

$$I_{OH}(MIN) = \frac{V_{ID}^{+}}{R1} + \frac{V + V_{ID}^{+}}{R2} + 75\ \mu A \quad [5]$$

Solving these equations ([3] and [5]) simultaneously yields R1 and R2.

As an example, assume a memory system with 4 outputs wired-ORed to a sense amplifier, requiring a chip access time of 460 nsec. Then the associated current and resistor values are:

$I_{OLT}(MAX) = 152.3\ \mu A + 3\ (5\ \mu A) = 167.3\ \mu A$

$I_{OH}(MIN) = 511.12\ \mu A$

Therefore:

$R1 = 190\ \Omega$

$R2 = 16.5\ K\Omega$

Sense amplifiers vary from the very fast, low-threshold types to the slower, high-threshold kind. The ideal choice will depend on the application. Fig. 1-A and the guidelines in this note are intended to help the designer tailor his sense amplifier design to meet the speed and cost requirements of his particular application.

It should also be noted that a portion of the output current from the memory chip is used to charge the capacitance on the data output. If the output impedance differs greatly from the specified load, this current must also be calculated.