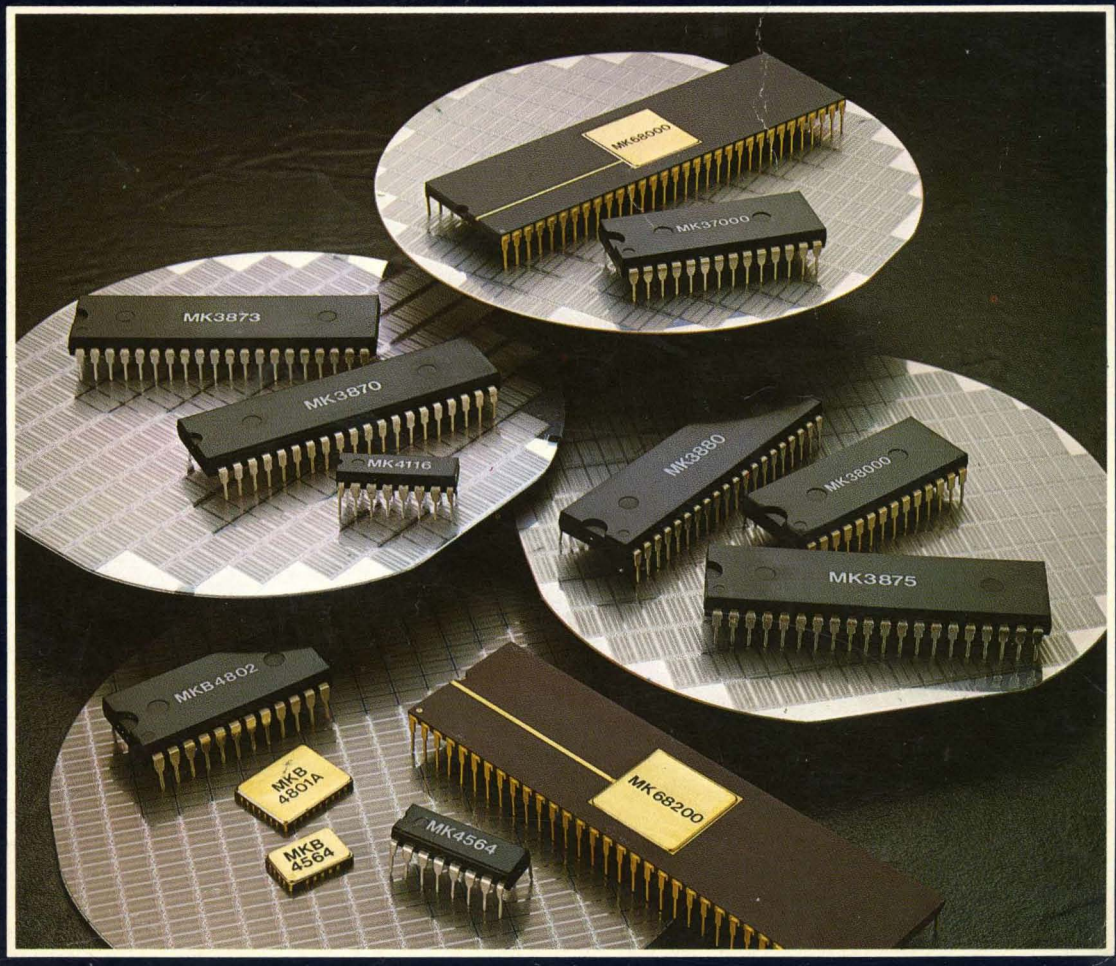
MOSTEK 1982/1983

MICROELECTRONIC DATA BOOK



1982/1983
MICROELECTRONIC
DATA BOOK

PRINTED IN USA May 1982

1982/1983 MICROELECTRONIC DATA BOOK

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XIII. Microprocessor and Support Devices

XIV. Industrial Hi-Rel Products

TELECOMMUNICATIONS

Information on the following Mostek telecomunications circuits is contained in the 1982 Telecommunications Data Book which is available separately.

Integrated Tone Dialers
MK5087 Integrated Tone Dialer
MK5089 Integrated Tone Dialer
MK5087/89 Electronic Drive Application Brief
MK5091 Integrated Tone Dialer
MK5092 Integrated Tone Dialer
MK5094 Integrated Tone Dialer
MK5380 Integrated Tone Dialer
MK5382 Integrated Tone Dialer with Redial
Integrated Dialer Comparison - Tone II vs Tone III Application Brief
Loop Simulator Application Brief

Integrated Pulse Dialers with Redial
MK50981 Integrated Pulse Dialer with Redial
MK50982 Integrated Pulse Dialer with Redial
MK50991 Integrated Pulse Dialer with Redial
MK50992 Integrated Pulse Dialer with Redial
Current Sources Application Brief
Pulse Dialer Comparison Application Brief

Repertory Dialers
MK5170 Repertory Dialer
MK5175 Ten-Number Repertory Dialer

Integrated Tone Decoders
MK5102-5 Integrated Tone Receiver
MK5102-5 DTMF Decoder Application Note
MK5102/S3525A DTMF Receiver System Application Brief
MK5103-5 Integrated Tone Decoder
DTMF Receiver System Application Brief

Active Speech Networks
MK5242 Active Speech Network

CODECs
MK5116 μ-255 Law Companding CODEC
MK5151 μ-255 Law Companding CODEC
MK5156 A-Law Companding CODEC
MK5316 Companding CODEC with Filters
Integrated PCM CODEC Technology Update

Transmit/Receive Filter
MK5912-3 PCM Transmit/Receive Filter
CODEC/Filter Demo Board Application Brief

INDUSTRIAL PRODUCTS

Information on the following Mostek industrial circuits is contained in the 1981 Industrial Products Data Book which is available separately.

Frequency Generator
MK50240/1/2 Top-Octave Frequency Generator

Digital Alarm Clock
*MK50250 Series MOS Digital Alarm Clock

Counter/Display Decoders
MK5002/5/7 Four-Digit Counter/Display Decoder
MK5002/7 Application Note
MK50395/6/7 Six-Decade Counter/Display Decoder
MK50395/6/7 Application Note
MK50398/9 Six-Decade Counter/Display Decoder

Counter/Time-Base Circuit
MK5009 Counter Time-Base Circuit
MK5009 Application Note

μP-Compatible A/D Converters/Analog Multiplexers
MK5168-1 μP-Compatible A/D Converter
MK50808 Eight-Bit A/D Converter/8-Channel Analog Multiplexer
MK50816 Eight-Bit A/D Converter/16-Channel Analog Multiplexer
A/D Converter Demo System Application Brief

*Not Recommended For New Design

1982/1983 MICROELECTRONIC DATA BOOK

Mostek - Technology For Today And Tomorrow

II

TECHNOLOGY

From its beginning, Mostek has been an innovator. From the developments of the 1K dynamic RAM and the single-chip calculator in 1970 to the current 64K dynamic RAM, Mostek technological breakthroughs have proved the benefits and cost-effectiveness of metal oxide semiconductors. Today, Mostek represents one of the industry's most productive bases of MOS/LSI technology, including Direct-Step-on-Wafer processing and laser implemented redundant circuitry.

The addition of the Microelectronics Research Center in Colorado Springs adds a new dimension to Mostek circuit design capabilities. Using the latest computer-aided design techniques, center engineers will be keeping ahead of the future with new technologies and processes.

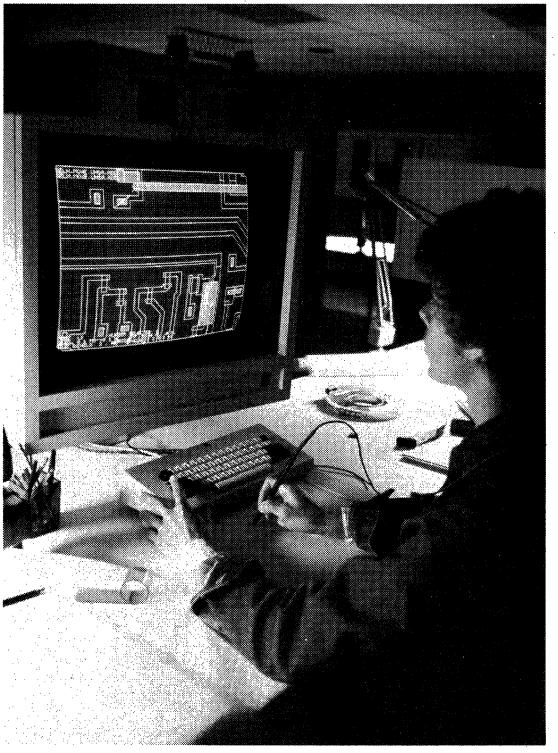
QUALITY

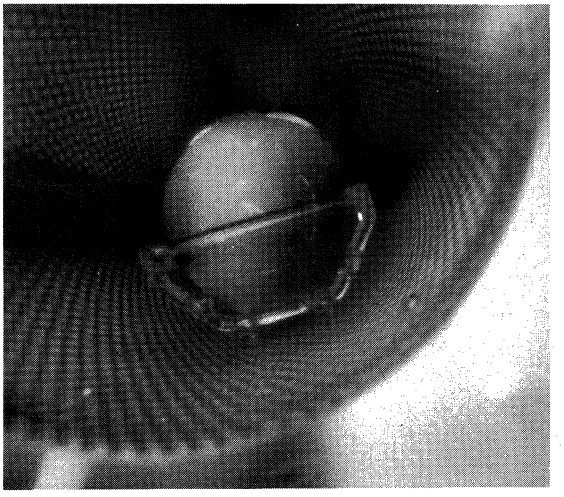
The worth of a product is measured by how well it is designed, manufactured and tested and by how well it works in your system.

In design, production and testing, the Mostek goal is meeting specifications the first time on every product. This goal requires a collective discipline from the company as well as individual efforts. Discipline, coupled with very personal pride, has enabled Mostek to build in quality at every level of production.

PRODUCTION CAPABILITY

The commitment to increasing production capability has made Mostek the world's largest manufacturer of dynamic RAMs. We entered the telecommunications market in 1974 with a tone dialer, and have shipped millions of telecom circuits since then. Millions of our MK3870 single-chip microcomputers are in use throughout the world. Recent construction in Dallas, Ireland and Colorado Springs has added some 50 percent to the Mostek manufacturing capacity.





THE PRODUCTS

Telecommunications Products

Mostek is the leading supplier of tone dialers, pulse dialers, and CODEC devices. As each new generation of telecommunications systems emerges, Mostek is ready with new generation components, including PCM filters, tone decoders, repertory dialers, new integrated tone dialers, and pulse dialers.

These products, many of them using CMOS technology, represent the most modern advancements in telecommunications component design.

Industrial Products

Mostek's line of Industrial Products offers a high degree of versatility per device. This family of components includes various microprocessor-compatible A/D converters, a counter/time-base circuit for the division of clock signals, and combined counter/display decoders. As a result of the low parts count involved, an economical alternative to discrete logic systems is provided.

Memory Products

Through innovations in both circuit design, wafer processing and production, Mostek has become the industry's leading supplier of dynamic RAMs.

Examples of Mostek leadership are families of x1 and x8 high performance static RAMs and our extremely successful 64K ROMs with more codes processed than any other mask-ROM in the industry. Another performance and density milestone is our 256K ROM, the MK38000. In MOS Dynamic RAMs, Mostek led the way as the world's leading supplier of 16K devices.

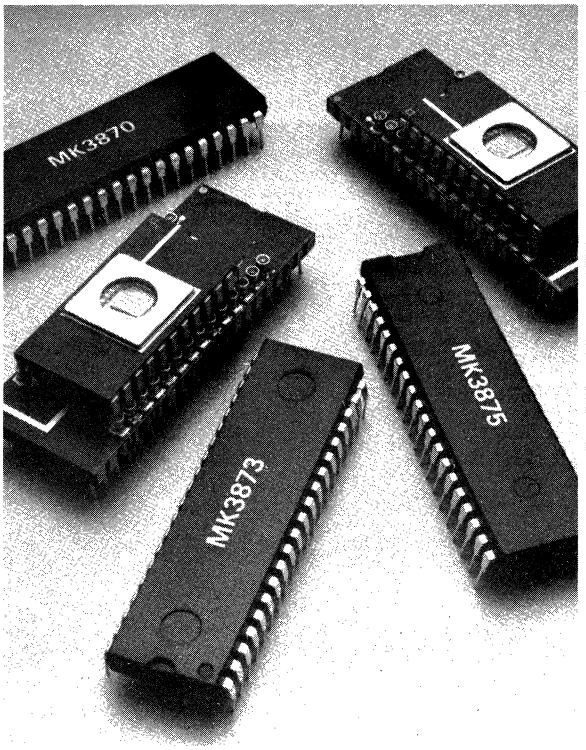
Our MK4564 64K dynamic RAM uses advanced circuit techniques and design to enhance manufacturability to satisfy the demands of a huge marketplace.

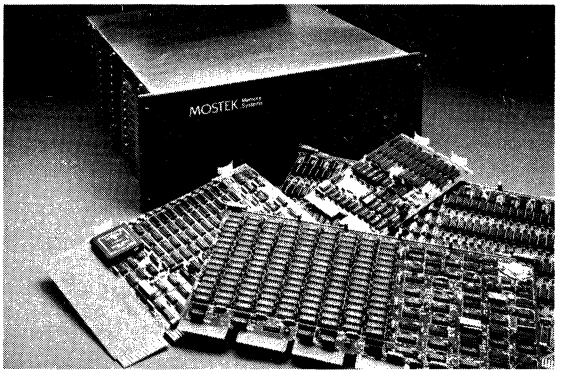
Microcomputer Components

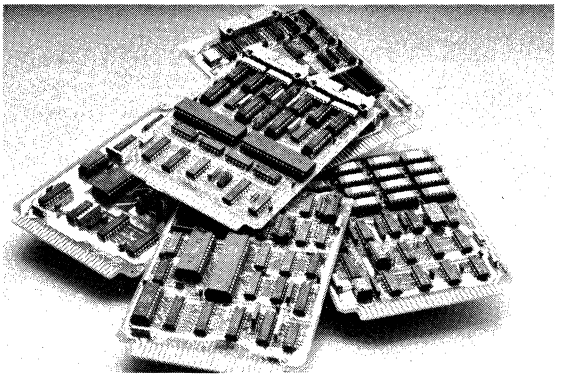
Mostek's microcomputer components cover the entire spectrum of microcomputer applications.

Our MK68000 16-bit microprocessor is designed for high-performance, memory-intensive systems.

Our Z80 is today's industry-standard 8-bit microprocessor. The Mostek 3870 family of single-chip microcomputers offers upgrade options in ROM, RAM, and I/O—all in the same socket. The MK38P70 EPROM piggyback microcomputer emulates the entire family and is ideal for low-volume applications.







Development systems include the RADIUS™ remote development station that lets you use your host minicomputer to develop the applications software. The program is then downloaded into the RADIUS which then lets you perform real-time in-circuit emulation and debug. The Mostek Matrix™ Development System is a stand-alone hardware and software debug and integration system.

Microcomputer Systems

Mostek is the world's leading manufacturer of Z80-based STD BUS system components. A new line of microsystems utilizing the VME BUS and based on the MK68000 will be available soon.

Computer systems include our Matrix line which utilize STD BUS cards to let you custom-design your own system.

Military Products

An extension of the high quality in fabrication and design inherent in Mostek's product line allows many of our ICs to be made available screened to MIL-STD-883. In addition, select parts are qualified to the rigors of MIL-M-38510 and are processed on our QPL certified lines.

The MKB product line begins with the complete Memory Products offering, and extends into microprocessors and gate arrays. Leadless Chip Carrier packaging and prepared customer SCDs address the particular needs of the military community.

Memory Systems

Taking full advantage of our leadership in memory components technology, Mostek Memory Systems offers a broad line of products, all with the performance and reliability to match our industry-standard circuits. Mostek Memory Systems offers add-in memory boards for popular DEC, Data General, and Perkin-Elmer minicomputers.

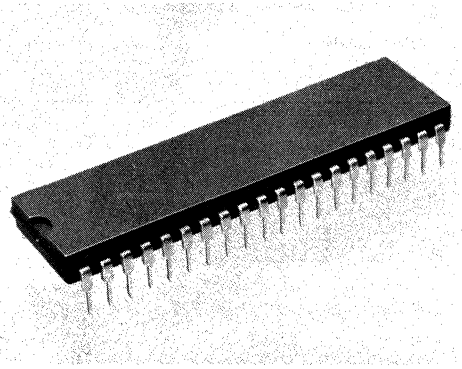
Mostek also offers special purpose and custom memory boards for special applications.

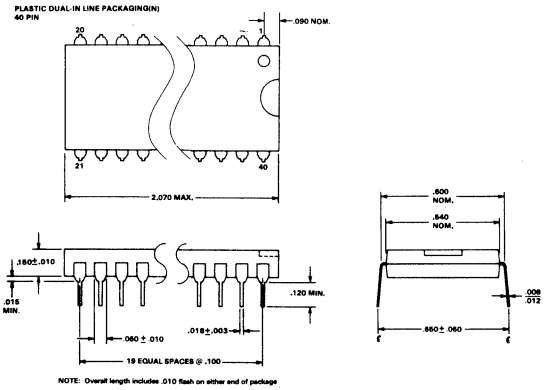
Gate Arrays

Utilizing the technology developed by United Technologies Microelectronic Research Center, Mostek plans to market custom gate array circuits in the second half of 1982.

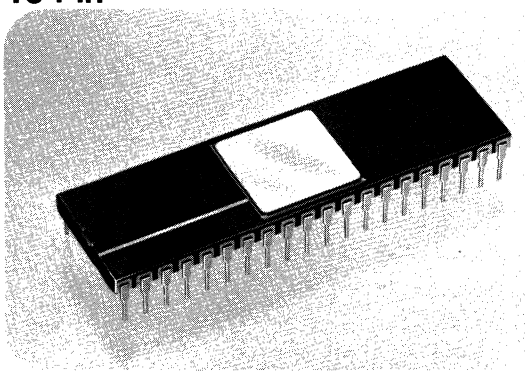
Package Descriptions

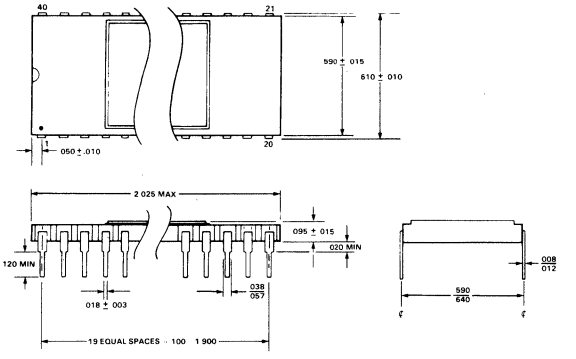
Plastic Dual-In-Line Package (N)
40 Pin



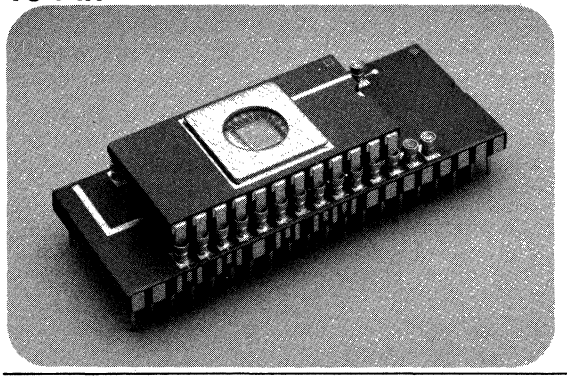


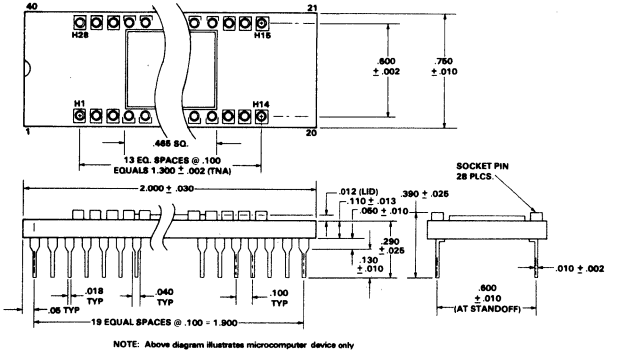
Ceramic Dual-In-Line Package (P)
40 Pin



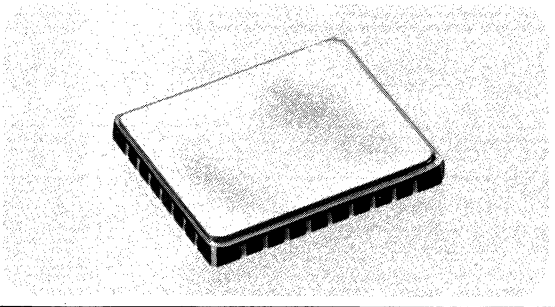


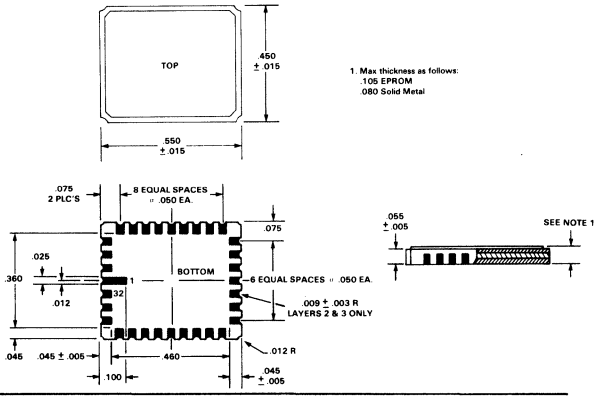
P-PROM Package (R)
40 Pin



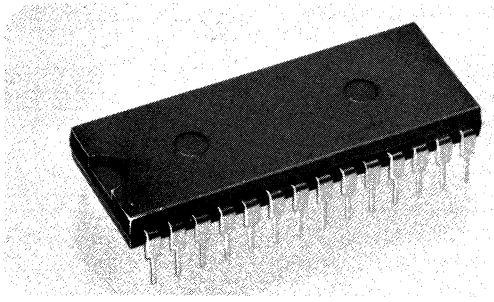


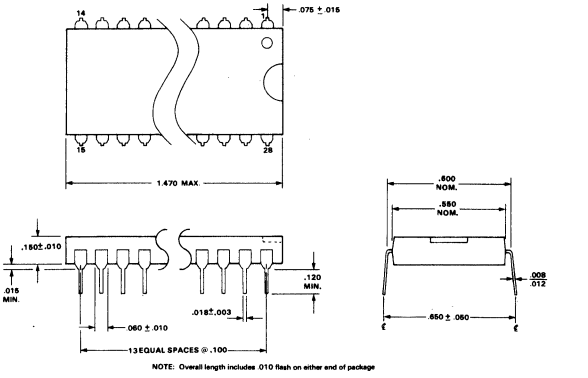
Leadless Hermetic Chip Carrier (E)
32 Pin (Proposed JEDEC Type E)



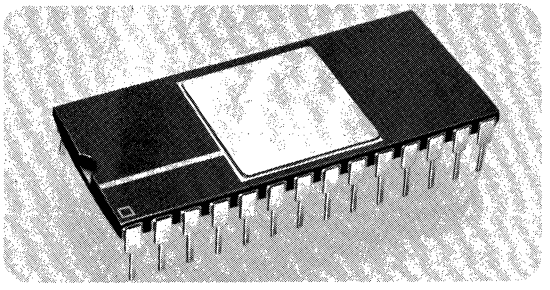


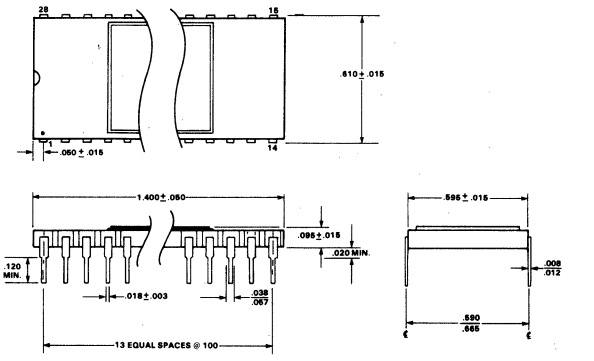
Plastic Dual-In-Line Package (N)
28 Pin



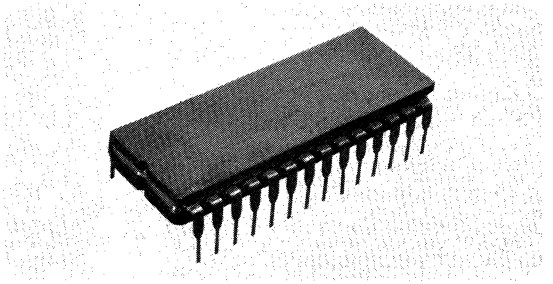


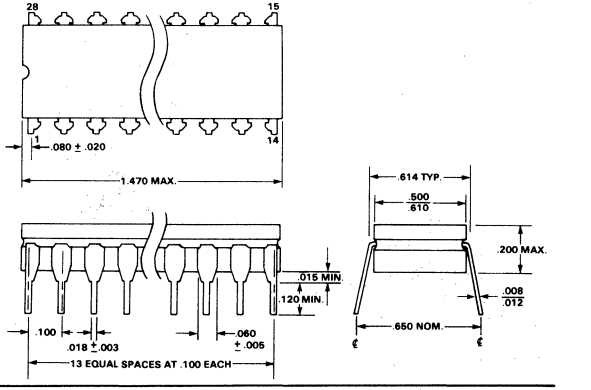
Ceramic Dual-In-Line Package (P)
28 Pin



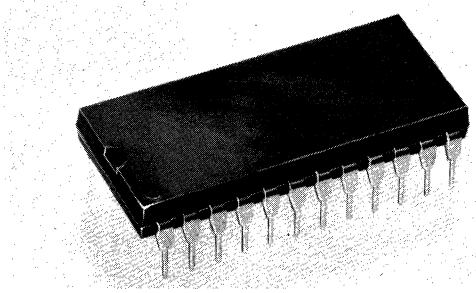


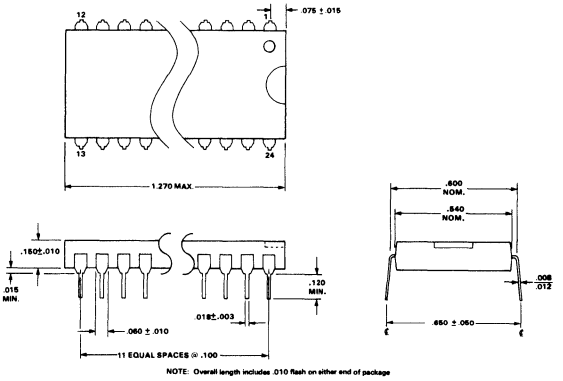
Cerdip Hermetic Package (J)
28 Pin



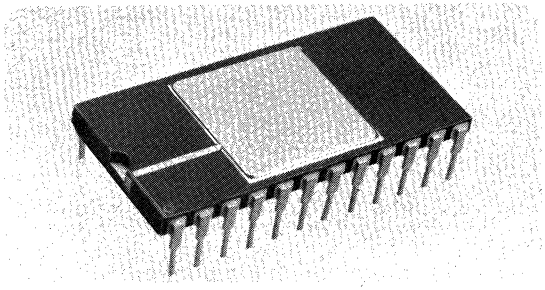


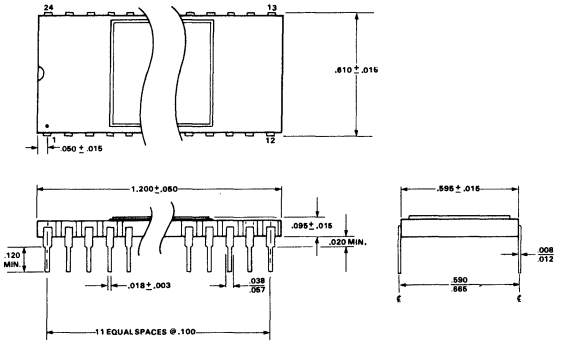
Plastic Dual-In-Line Package (N)
24 Pin



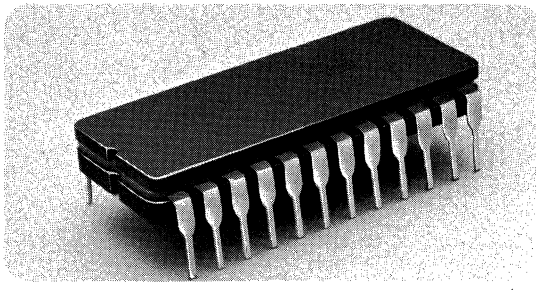


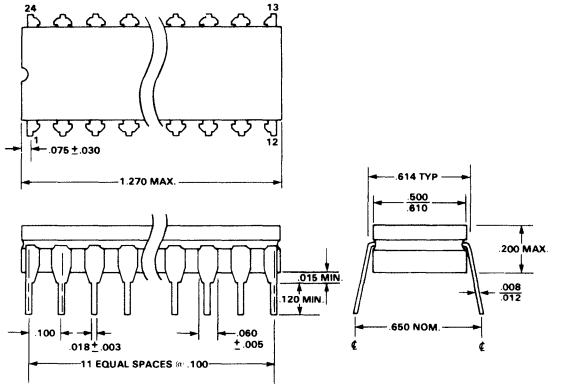
Ceramic Dual-In-Line Package (P)
24 Pin





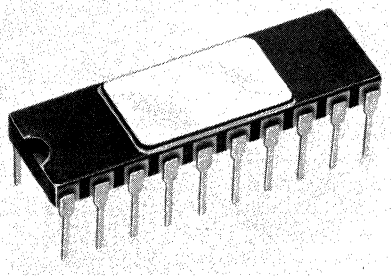
Cerdip Hermetic Package (J)
24 Pin

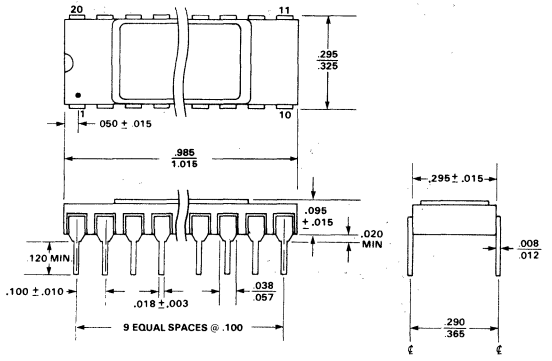




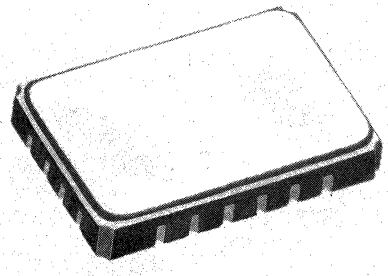
II

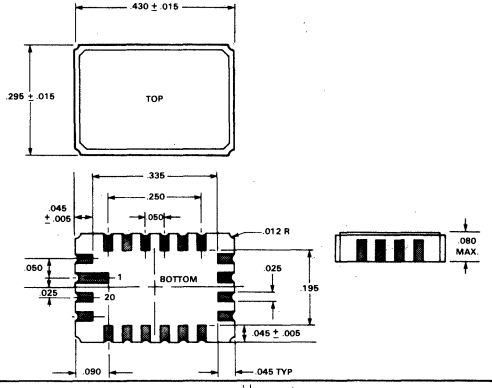
Ceramic Dual-In-Line Package (P)
20 Pin



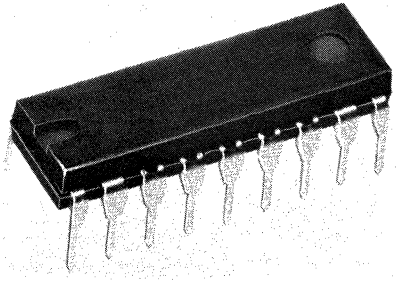


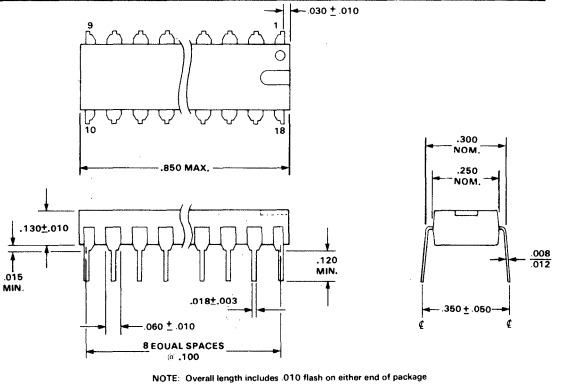
Leadless Hermetic Chip Carrier (E)
20 Pin





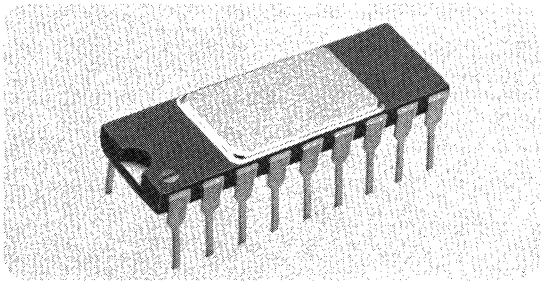
Plastic Dual-In-Line Package (N)
18 Pin

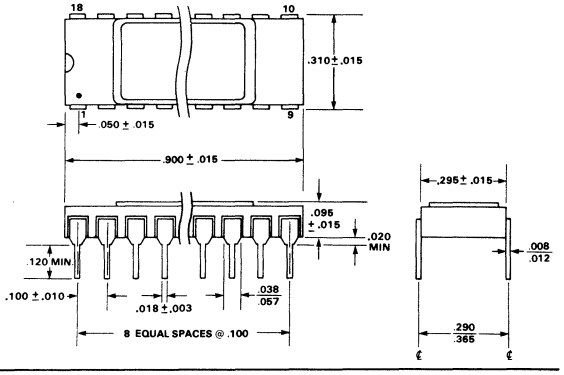




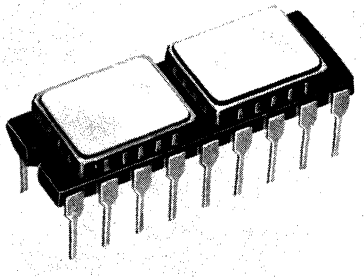
NOTE: Overall length includes .010 flash on either end of package

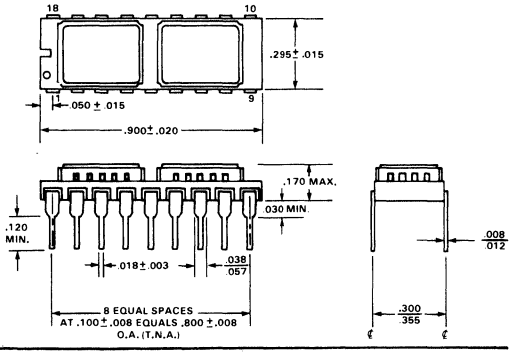
Ceramic Dual-In-Line Package (P)
18 Pin



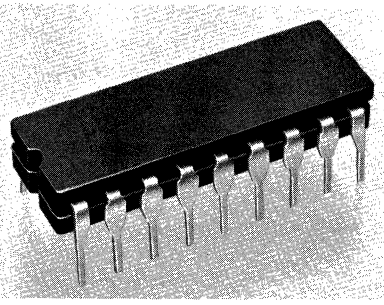


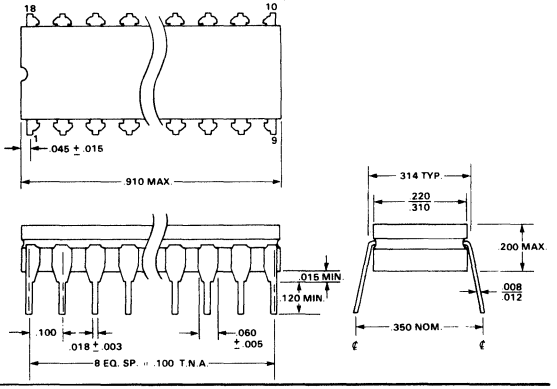
Dual-In-Line Double Density Ceramic Package (D)
18 Pin



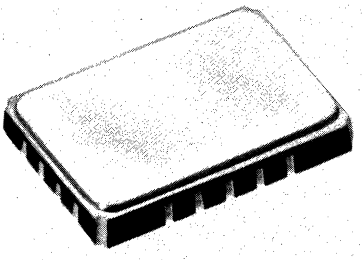


Cerdip Hermetic Package (J)
18 Pin





Leadless Hermetic Chip Carrier (E)
18 Pin (Proposed JEDEC Type F)



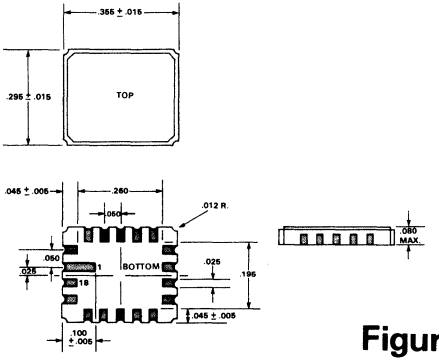
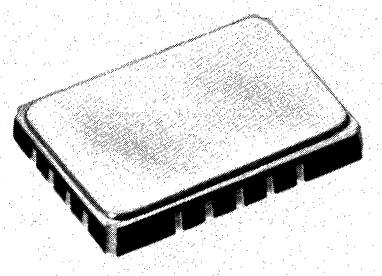


Figure A

Leadless Hermetic Chip Carrier (E)
18 Pin (Proposed JEDEC Type F)



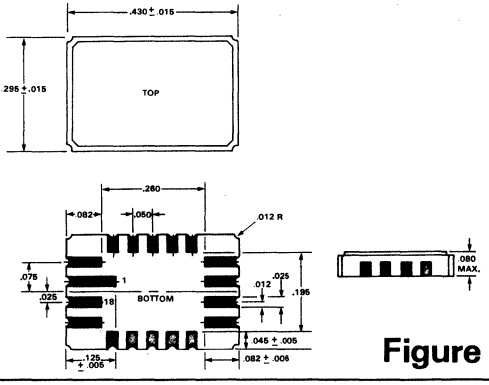
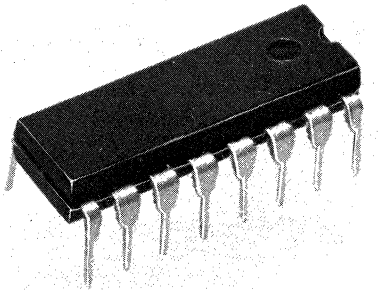
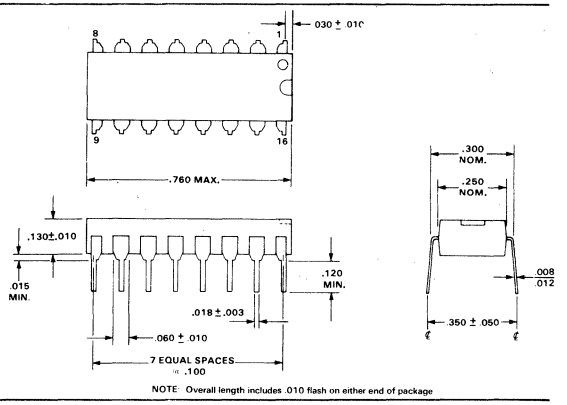


Figure B

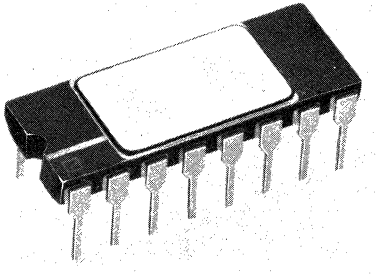
Plastic Dual-In-Line Package (N)
16 Pin

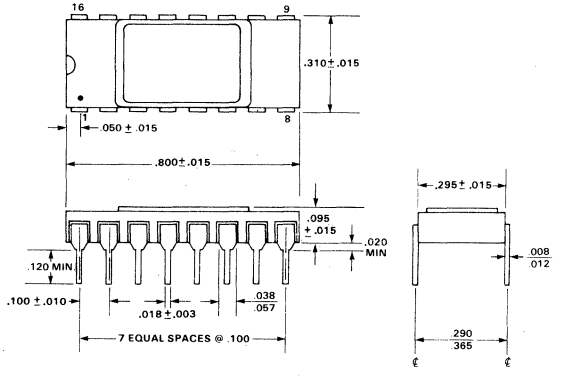




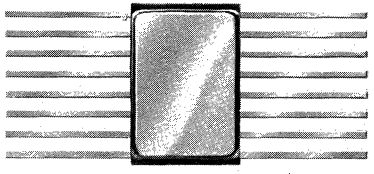
NOTE Overall length includes .010 flash on either end of package

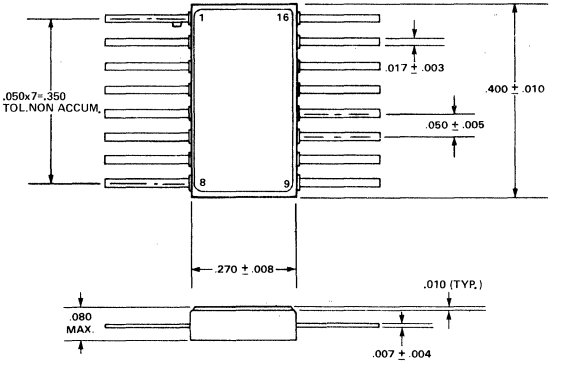
Ceramic Dual-In-Line Package (P)
16 Pin



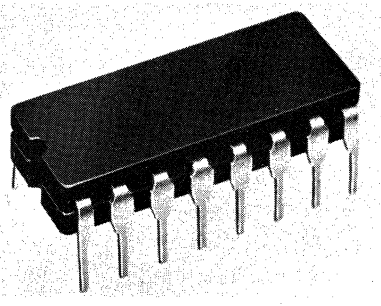


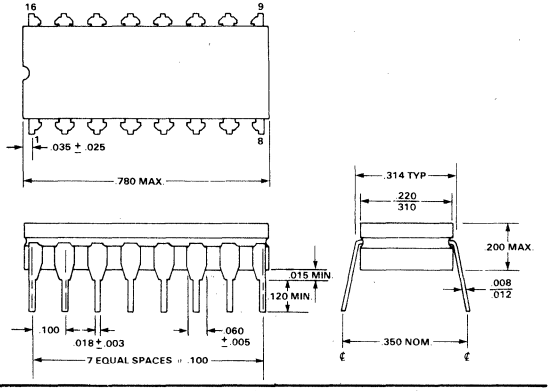
Ceramic Flat Package (F)
16 Pin



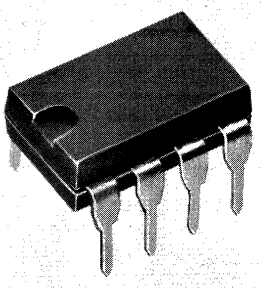


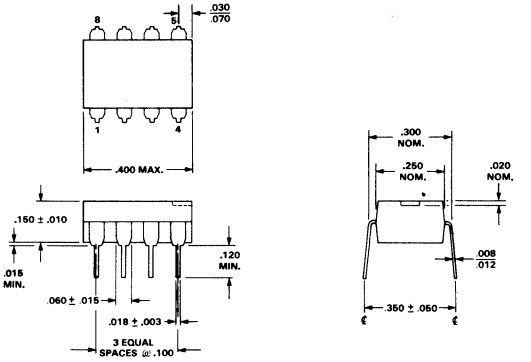
Cerdip Hermetic Package (J)
16 Pin





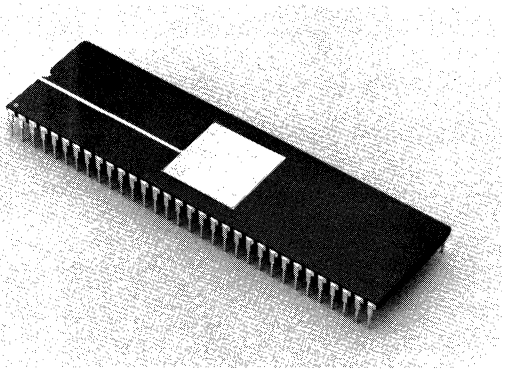
Plastic Dual-In-Line Package (N)
8 Pin

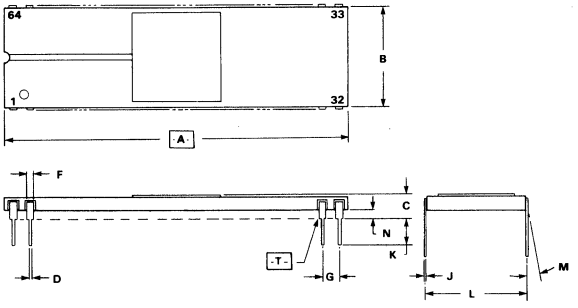




NOTE: Overall length includes .010 flash on either end of package

68000 Family
Ceramic Dual-In-Line Package (P)
64 Pin



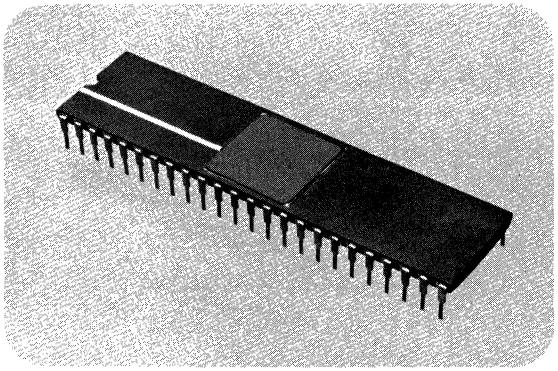


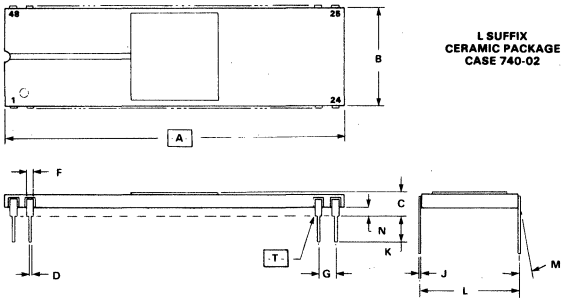
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	80.52	82.04	3.170	3.240
B	22.25	22.96	0.900	0.920
C	3.05	4.32	0.120	0.170
D	0.38	0.53	0.015	0.021
F	0.76	1.40	0.030	0.057
G	2.54 BSC		0.100 BSC	
J	0.20	0.33	0.008	0.013
K	2.54	4.19	0.100	0.165
L	22.61	23.11	0.890	0.910
M	–	10°	–	10°
N	1.02	1.52	0.020	0.060

Case 746.01

NOTES:
1. Dimension -A- is datum.
2. Positional tolerance for leads:
   ⌖ 0.25 (0.010) Ⓜ T A Ⓜ
3. -T- is seating plane.
4. Dimension "L" to center of leads when formed parallel.
5. Dimensioning and tolerancing per ANSI Y14.5, 1973.

Ceramic Dual-In-Line Package (P)
48 Pin





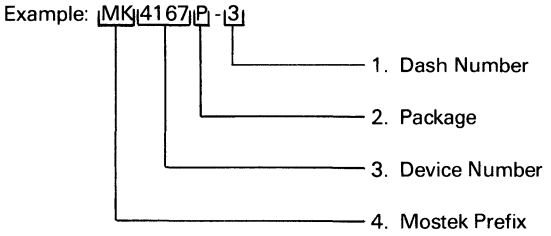
L SUFFIX
CERAMIC PACKAGE
CASE 740-02

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	60.35	61.57	2.376	2.424
B	14.63	15.34	0.576	0.604
C	3.05	4.32	0.120	0.160
D	0.381	0.533	0.015	0.021
F	0.762	1.397	0.030	0.055
G	2.54 BSC		0.100 BSC	
J	0.203	0.330	0.008	0.013
K	2.54	4.19	0.100	0.165
L	14.99	15.65	0.590	0.616
M	0°	10°	0°	10°
N	1.016	1.524	0.040	0.060

NOTES:
1. DIMENSION -A- IS DATUM.
2. POSITIONAL TOLERANCE FOR LEADS:
   Ø 0.25 (0.010) T AM
3. -T- IS SEATING PLANE.
4. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

ORDERING INFORMATION

Factory orders for parts described in this book should include a four-part number as explained below:



1. Dash Number

   One or two numerical characters defining specific device performance characteristics and operating temperature range.

2. Package

   P - Gold side-brazed ceramic DIP
   J - CER-DIP
   N - Epoxy DIP (Plastic)
   K - Tin side-brazed ceramic DIP
   T - Ceramic DIP with transparent lid
   E - Ceramic leadless chip carrier
   D - Dual density RAM-PAC
   F - Flat pack

3. Device number

   1XXX or 1XXXX - Shift Register, ROM
   2XXX or 2XXXX - ROM, EPROM
   3XXX or 3XXXX - ROM, EPROM
   38XX - Microcomputer Components
   4XXX or 4XXXX - RAM
   5XXX or 5XXXX - Counters, Telecommunication and Industrial
   7XXX or 7XXXX - Microcomputer Systems

4. Mostek Prefix

   MK - Standard Prefix

   MKB - Military Hi-Rel screening to MIL-STD-883 Class B for extended temperature range operation.

   MKI - Industrial Hi-Rel screening for -40°C to +85°C operation.

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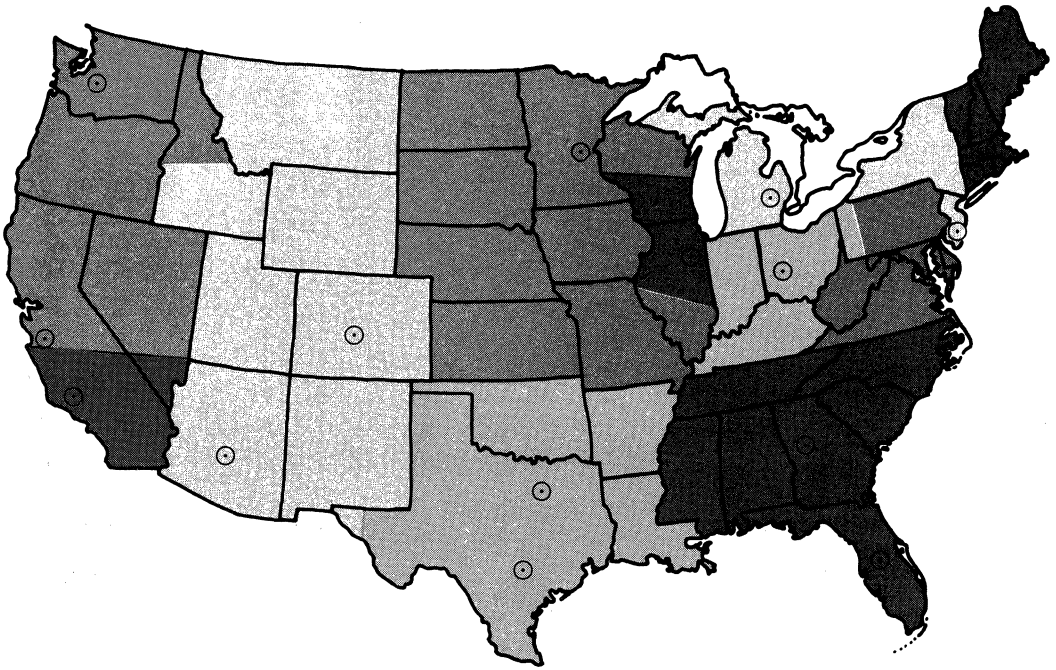

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1982/1983 MICROELECTRONIC DATA BOOK

MOSTEK®

MEMORY COMPONENTS

64K-Bit Read-Only Memory

MK36000(P/J/N) Series

III

FEATURES

- ☐ MK36000 8K x 8 Organization— "Edge Activated" * operation ($\overline{CE}$)
- ☐ Access Time/Cycle Time

P/N	Access	Cycle
MK36000-4	250 ns	375 ns
MK36000-5	300 ns	450 ns

- ☐ Single +5V ± 10% Power Supply
- ☐ Standard 24 pin DIP
- ☐ Low Power Dissipation - 220mW Max Active
- ☐ Low Standby Power Dissipation - 45mW Max, ($\overline{CE}$ High)
- ☐ On chip latches for addresses
- ☐ Inputs and three-state outputs - TTL compatible
- ☐ Outputs drive 2 TTL loads and 100pF
- ☐ MKB version screened to MIL-STD-883

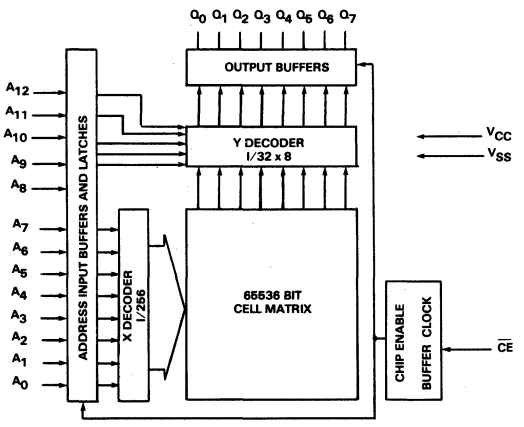
DESCRIPTION

The MK36000 is a N-channel silicon gate MOS Read Only Memory, organized as 8192 words by 8 bits. As a state-of-the-art device, the MK36000 incorporates advanced circuit techniques designed to provide maximum circuit density and reliability with the highest possible performance, while maintaining low power dissipation and wide operating margins.

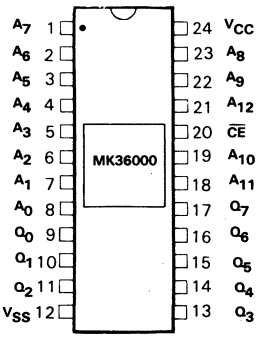
Use of a static storage cell with clocked control periphery allows the circuit to be put into an automatic low power standby mode. This is accomplished by maintaining the chip enable ($\overline{CE}$) input at a TTL high level. In this mode, power dissipation is reduced to typically 45mW, as compared to unclocked devices which draw full power continuously. In system operation, a device is selected by the $\overline{CE}$ input, while all others are in a low power mode, reducing the overall system power. Lower power means reduced power supply cost, less heat to dissipate and an increase in device and system reliability.

The edge activated chip enable also means greater system flexibility and an increase in system speed.

FUNCTIONAL DIAGRAM (MK36000)



PIN CONNECTIONS



PIN NAMES

A_0-A_{12}	Address	V_{SS}	GND
O_0-O_7	Outputs	$\overline{CE}$	Chip Enable
V_{CC}	+5V		

* Trademark of Mostek Corporation

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Terminal Relative to V_{SS} ..... -1.0 V to +7 V
Operating Temperature T_A (Ambient) ..... 0°C to +70°C
Storage Temperature - Ceramic (Ambient) ..... -65°C to +150°C
Storage Temperature - Plastic (Ambient) ..... -55°C to +125°C
Power Dissipation ..... 1 Watt

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS[6]

($0°C \leq T_A \leq +70°C$)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Power Supply Voltage	4.5	5.0	5.5	V	6
V_{IL}	Input Logic 0 Voltage	-1.0		0.8	V	
V_{IH}	Input Logic 1 Voltage	2.0		V_{CC}	V	

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ±10%) ($0°C \leq T_A \leq +70°C$) [6]

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
I_{CC1}	V_{CC} Power Supply Current (Active)			40	mA	1
I_{CC2}	V_{CC} Power Supply Current (Standby)			8	mA	7
$I_{I(L)}$	Input Leakage Current	-10		10	μA	2
$I_{O(L)}$	Output Leakage Current	-10		10	μA	3
V_{OL}	Output Logic "0" Voltage @ I_{OUT} = 3.3 mA			0.4	V	
V_{OH}	Output Logic "1" Voltage @ I_{OUT} = -220 μA	2.4			V	

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ±10%) ($0°C \leq T_A \leq +70°C$)[6]

SYM	PARAMETER	-4		-5		UNITS	NOTES
		MIN	MAX	MIN	MAX		
t_C	Cycle Time	375		450		ns	4
t_{CE}	$\overline{CE}$ Pulse Width	250	10000	300	10000	ns	4
t_{AC}	$\overline{CE}$ Access Time		250		300	ns	4
t_{OFF}	Output Turn Off Delay		60		75	ns	4
t_{AH}	Address Hold Time Referenced to $\overline{CE}$	60		75		ns	
t_{AS}	Address Setup Time Referenced to $\overline{CE}$	0		0		ns	
t_p	$\overline{CE}$ Precharge Time	125		150		ns	

NOTES:

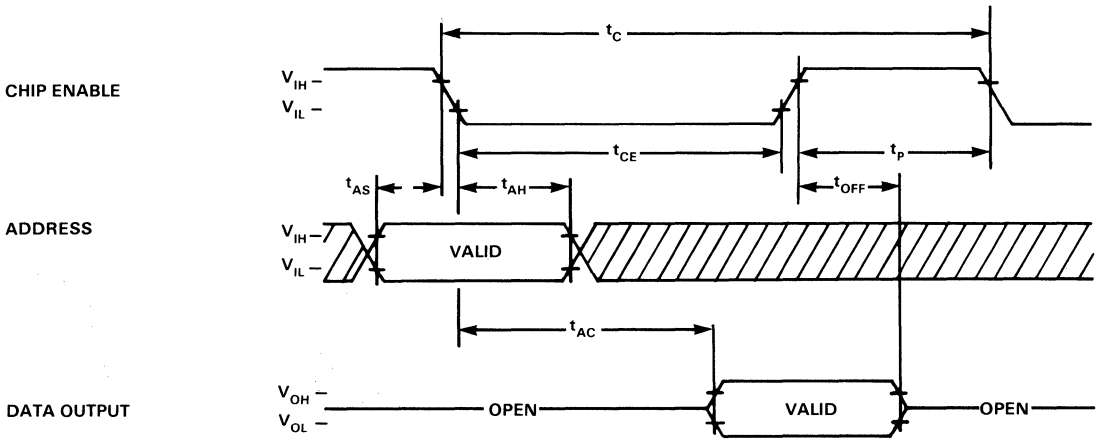
1. Current is proportional to cycle rate. I_{CC1} is measured at the specified minimum cycle time. Data Outputs open.
2. V_{IN} = 0 V to 5.5 V (V_{CC} = 5 V)
3. Device unselected; V_{OUT} = 0 V to 5.5 V
4. Measured with 2 TTL loads and 100 pF, transition times = 20 ns
5. Capacitance measured with Boonton Meter or effective capacitance calculated from the equation: $C = \frac{\Delta Q}{\Delta V}$ with ΔV = 3 volts
6. A minimum 2 ms time delay is required after the application of V_{CC} (+5) before proper device operation is achieved. $\overline{CE}$ must be at V_{IH} for this time period.
7. $\overline{CE}$ high.

CAPACITANCE

($0°C \leq T_A \leq 70°C$)

SYM	PARAMETER	TYP	MAX	UNITS	NOTES
C_I	Input Capacitance	5	8	pF	5
C_O	Output Capacitance	7	15	pF	5

TIMING DIAGRAM



DESCRIPTION (Continued)

The MK36000 features onboard address latches controlled by the $\overline{CE}$ input. Once the address hold time specification has been met, new address data can be applied in anticipation of the next cycle. Outputs can be wire 'OR'ed together, and a specific device can be selected by utilizing the $\overline{CE}$ input with no bus conflict on the outputs. The $\overline{CE}$ input allows the fastest access times yet available in 5 volt only ROM's and imposes no loss in system operating flexibility over an unclocked device.

Other system oriented features include fully TTL compatible inputs and outputs. The three state outputs, controlled by the $\overline{CE}$ input, will drive a minimum of 2 standard TTL loads. The MK36000 operates from a single +5 volt power supply with a wide ±10% tolerance, providing the widest operating margins available. The MK36000 is packaged in the industry standard 24 pin DIP.

Any application requiring a high performance, high bit density ROM can be satisfied by the MK36000 ROM. This device is ideally suited for 8 bit microprocessor systems such as those which utilize the Z80. It can offer significant cost advantages over PROM.

OPERATION

The MK36000 is controlled by the chip enable ($\overline{CE}$) input. A negative going edge at the $\overline{CE}$ input will activate the device as well as strobe and latch the inputs into the on-chip address registers. At access time the outputs will become active and contain the data read from the selected location. The outputs will remain latched and active until $\overline{CE}$ is returned to the inactive state.

MOSTEK®

64K-BIT MOS READ-ONLY MEMORY

MK37000(P/J/N) Series

III

FEATURES

- ☐ Organization: 8K x 8 Bit ROM - JEDEC Pinout
- ☐ Pin compatible with Mostek's BYTEWYDE™ Memory Family
- ☐ Access Time/Cycle Time

P/N	ACCESS	CYCLE
MK37000-5	300 ns	450 ns
MK37000-4	250 ns	375 ns

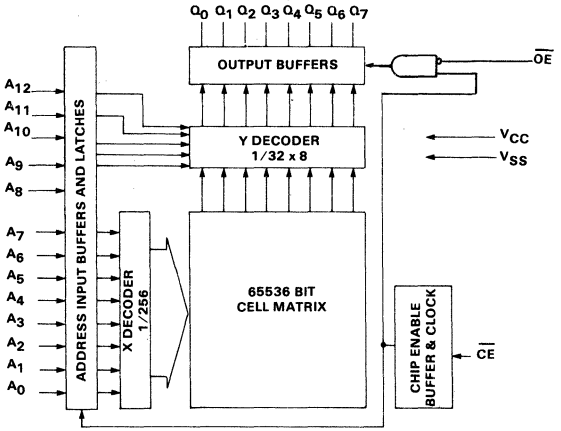
- ☐ Mask ROM replacement for 2764 EPROM
- ☐ No Connections allow easy upgrade to future generation higher density ROMs
- ☐ Low power dissipation: 220mW max active, 45mW max standby
- ☐ $\overline{CE}$ and $\overline{OE}$ functions facilitate Bus control
- ☐ MKB version screened to MIL-STD-883

DESCRIPTION

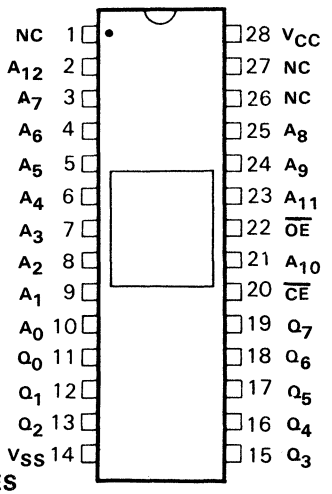
The MK37000 is a N-channel silicon gate MOS Read Only Memory, organized as 8192 words by 8 bits. As a state-of-the-art device, the MK37000 incorporates advanced circuit techniques designed to provide maximum circuit density and reliability with the highest possible performance, while maintaining low power dissipation and wide operating margins. The MK37000 is to be used as a pin/function compatible mask programmable alternative to the 2764 8K x 8 bit EPROM. As a member of the Mostek BYTEWYDE Memory Family, the MK37000 brings to the memory market a new era of ROM, PROM and EPROM compatibility previously unavailable.

Use of clocked control periphery and a standard static ROM cell makes the MK37000 the lowest power 64K ROM available. Active power is a mere 220mW while standby ($\overline{CE}$ high) is only 45mW. To provide greater system flexibility an output enable ($\overline{OE}$) function has been added using one of the extra pins available on the

FUNCTIONAL DIAGRAM (MK37000)



PIN CONNECTIONS



TRUTH TABLE

$\overline{CE}$	$\overline{OE}$	MODE	OUTPUTS	POWER
V_{IH}	X	Deselect	High-Z	Standby
V_{IL}	V_{IH}	Inhibit	High-Z	Active
V_{IL}	V_{IL}	Read	D_{OUT}	Active

X = Don't Care

PIN NAMES

A0 - A12-Address	NC - No Connection
$\overline{CE}$ - Chip Enable	$\overline{OE}$ - Output Enable
Q_0 - Q_7 - Outputs	V_{CC} - +5V supply
	V_{SS} - Ground

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Terminal Relative to V_{SS} ..... -1.0V to +7V
Operating Temperature T_A (Ambient) ..... 0°C to +70°C
Storage Temperature—Ceramic (Ambient) ..... -65°C to +150°C
Storage Temperature—Plastic (Ambient) ..... -55°C to +125°C
Power Dissipation ..... 1 Watt

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS[6]

($0°C \leq T_A \leq +70°C$)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Power Supply Voltage	4.5	5.0	5.5	V	
V_{IL}	Input Logic 0 Voltage	-1.0		0.8	V	
V_{IH}	Input Logic 1 Voltage	2.0		V_{CC}	V	

DC ELECTRICAL CHARACTERISTICS [6]

($V_{CC} = 5V \pm 10\%$) ($0°C \leq T_A \leq +70°C$)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
I_{CC1}	V_{CC} Power Supply Current (Active)			40	mA	1
I_{CC2}	V_{CC} Power Supply Current (Standby)			8	mA	7
$I_{I(L)}$	Input Leakage Current	-10		10	μA	2
$I_{O(L)}$	Output Leakage Current	-10		10	μA	3
V_{OL}	Output Logic "0" Voltage @ $I_{OUT} = 3.3mA$			0.4	V	
V_{OH}	Output Logic "1" Voltage @ $I_{OUT} = -220\mu A$	2.4			V	

AC ELECTRICAL CHARACTERISTICS[6]

($V_{CC} = 5V \pm 10\%$) ($0°C \leq T_A \leq +70°C$)

		-4		-5			
SYM	PARAMETER	MIN	MAX	MIN	MAX	UNITS	NOTES
t_{RC}	Read Cycle Time	375		450		ns	4
t_{CE}	$\overline{CE}$ Pulse Width	250	10,000	300	10,000	ns	4
t_{CEA}	$\overline{CE}$ Access Time		250		300	ns	4
t_{CEZ}	Chip Enable Data Off Time		60		75	ns	
t_{AH}	Address Hold Time Referenced to $\overline{CE}$	60		75		ns	
t_{AS}	Address Setup Time Referenced to $\overline{CE}$	0		0		ns	
t_P	$\overline{CE}$ Precharge Time	125		150		ns	
t_{OEA}	Output Enable Access Time		80		100	ns	
t_{OEZ}	Output Enable Data Off Time		60		75	ns	

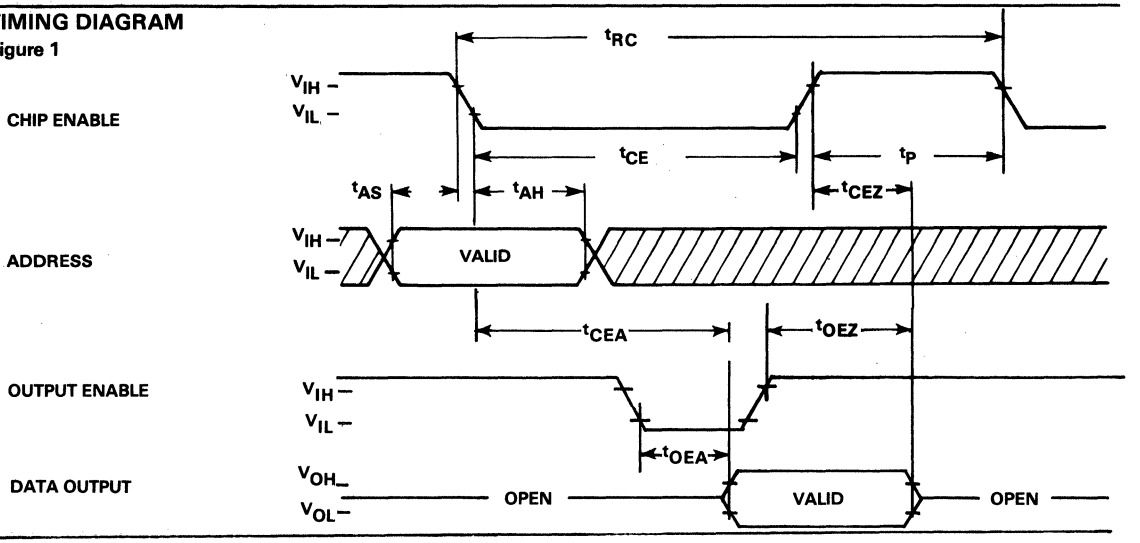
CAPACITANCE

($0°C \leq T_A \leq 70°C$)

SYM	PARAMETER	TYP	MAX	UNITS	NOTES
C_I	Input Capacitance	5	8	pF	5
C_O	Output Capacitance	7	15	pF	5

TIMING DIAGRAM

Figure 1



NOTES:

1. Current is proportional to cycle rate. I_{CC1} is measured at the specified minimum cycle time. Data Outputs open.
2. V_{IN} = 0V to 5.5V
3. Device unselected; V_{OUT} = 0V to 5.5V
4. Measured with 2 TTL loads and 100pF, transition times = 20ns
5. Capacitance measured with Boonton Meter or effective capacitance calculated from the equation:
   $C = \frac{\Delta Q}{\Delta V}$ with ΔV = 3 volts
6. A minimum 2ms time delay is required after the application of V_{CC} (+5) before proper device operation is achieved. $\overline{CE}$ must be at V_{IH} for this time period.
7. $\overline{CE}$ high

DESCRIPTION (Continued)

28 pin DIP. This function matches that found on all of the new BYTEWYDE family of memories available from Mostek.

The use of clocked $\overline{CE}$ mode of operation provides an automatic power down mode of operation. The MK37000 features on chip address latches controlled by the $\overline{CE}$ input. Once address hold time is met, new address data can be provided to the device in anticipation of a subsequent cycle. It is not necessary to maintain the address up to access time to access valid data. The output enable function controls only the outputs and is not latched by $\overline{CE}$. The $\overline{CE}$ input can be used for device selection and the $\overline{OE}$ input used to avoid bus conflicts so that outputs can be 'OR'ed together when using multiple devices.

Other system oriented features include fully TTL compatible inputs and outputs. The three state outputs, controlled by the $\overline{OE}$ input, will drive a minimum of 2 standard TTL loads. The MK37000 operates from a single +5 volt power supply with a wide ± 10% tolerance, providing the widest operating margins available. The MK37000 is packaged in the industry standard 28 pin DIP. Pin 1 and 26 are not connected to allow easy upward compatibility with next generation higher density ROM which will use these pins for addresses. Pin 27 is not connected in order to maintain compatibility with RAMs which use this pin as a write enable ($\overline{WE}$) control function.

Any application requiring a high performance, high bit density ROM can be satisfied by the MK37000. This device is ideally suited for 8 bit microprocessor systems such as those which utilize the MK3880. It can offer significant cost advantages over PROM.

OPERATION

The MK37000 is controlled by the chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) inputs. A negative going edge at the $\overline{CE}$ input will activate the device and latch the addresses into the on chip address registers. The output buffers, under the control of $\overline{OE}$, will become active in $\overline{CE}$ access

time (t_{CEA}) if the output enable access time (t_{OEA}) requirement is met. The on chip address register allows addresses to be changed after the specified hold time (t_{AH}) in preparation for the next cycle. The outputs will remain valid and active until either $\overline{CE}$ or $\overline{OE}$ is returned to the inactive state. After chip deselect time (t_{CEZ}) the output buffers will go to a high impedance state. The $\overline{CE}$ input must remain inactive (high) between subsequent cycles for time t_P to allow for precharging the nodes of the internal circuitry.

MK37000 ROM CODE DATA INPUT PROCEDURE

The preferred method of supplying code data to Mostek is in the form of programmed EPROMs (see table). In addition to the programmed set, Mostek requires an additional set of blank EPROMs for supplying customer code verification. When multiple EPROMs are required to describe the ROM they shall be designated in ascending address space with the numbers 1, 2, 3, etc. As an example, EPROM #1 would start with address space 0000 and go to 07FF for a 2K x 8 device. EPROM #2 would then start at address space 0800 and so on. A total of (4) 2K x 8 devices would be required to totally describe the address space of the 8K x 8 MK37000.

A paper printout and verification approval letter will accompany each verification EPROM set returned to the customer. Approval is considered to be excepted when the signed verification letter is returned to Mostek. The original set of EPROMs will be retained by Mostek for the duration of the prototyping process.

Acceptable EPROMs for Code Data

Table 1

EPROM	# REQUIRED
2716/2516	4
2732	2
2764	1

MOSTEK®

256K-BIT MOS READ-ONLY MEMORY

MK38000(P/N)-25

III

FEATURES

- □ Organized 32K x 8
- □ Pin compatible with Mostek's BYTEWYDE™ Memory Family
- □ Access Time = Cycle Time
- □ Static Operation
- □ Automatic Power Down
- □ $\overline{CE}$ and $\overline{OE}$ functions facilitate bus control
- □ Pin 27 no connection permits interchange with static RAM ($\overline{WE}$)
- □ High performance

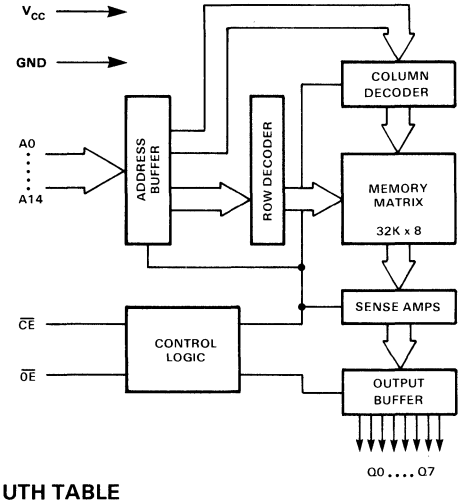
Part No.	Access Time	Cycle Time
MK38000-25	250 ns	250 ns

DESCRIPTION

The MK38000 is a N-channel silicon gate MOS Read Only Memory, organized as 32,768 words by 8 bits. As a state-of-the-art device, the MK38000 incorporates advanced circuit techniques designed to provide maximum circuit density and reliability with the highest possible performance, while maintaining low power dissipation and wide operating margins.

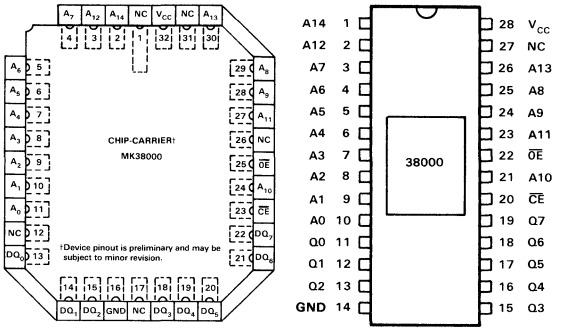
FUNCTIONAL DIAGRAM (MK38000)

Figure 1



PIN CONNECTIONS

Figure 2



TRUTH TABLE

$\overline{CE}$	$\overline{OE}$	MODE	OUTPUTS	POWER
H	X	Deselect	High-Z	Standby
L	H	Inhibit	High-Z	Active
L	L	Read	D_{OUT}	Active

PIN NAMES

A0-A14	Address	$\overline{OE}$	Output Enable
$\overline{CE}$	Chip Enable	V_{CC}	+5 V
NC	No Connection	GND	Ground
		Q0-Q7	Data Outputs

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Terminal Relative to GND ..... -1.0 V to +7 V
Operating Temperature T_A (Ambient) ..... 0°C to +70°C
Storage Temperature—Ceramic (Ambient) ..... -65°C to +150°C
Storage Temperature—Plastic (Ambient) ..... -55°C to +125°C
Power Dissipation ..... 1 Watt

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS[1,6]

($0°C \leq T_A \leq +70°C$)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Power Supply Voltage	4.75	5.0	5.25	V	
V_{IL}	Input Logic 0 Voltage	-1.0		0.8	V	8
V_{IH}	Input Logic 1 Voltage	2.0		V_{CC}	V	

DC ELECTRICAL CHARACTERISTICS[1,6]

(V_{CC} = 5 V ± 5%) ($0°C \leq T_A \leq +70°C$)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
I_{CC1}	V_{CC} Power Supply Current (Active)		75	100	mA	5
I_{CC2}	V_{CC} Power Supply Current (Standby)		35	50	mA	7
$I_{I(L)}$	Input Leakage Current	-10	0.1	10	μA	3
$I_{O(L)}$	Output Leakage Current	-10	0.1	10	μA	2
V_{OL}	Output Logic "0" Voltage @ I_{OUT} = 4 mA			0.4	V	
V_{OH}	Output Logic "1" Voltage @ I_{OUT} = -1 mA	2.4			V	

AC ELECTRICAL CHARACTERISTICS[1,4,6,9,10]

(V_{CC} = 5 V ± 5%) ($0°C \leq T_A \leq +70°C$)

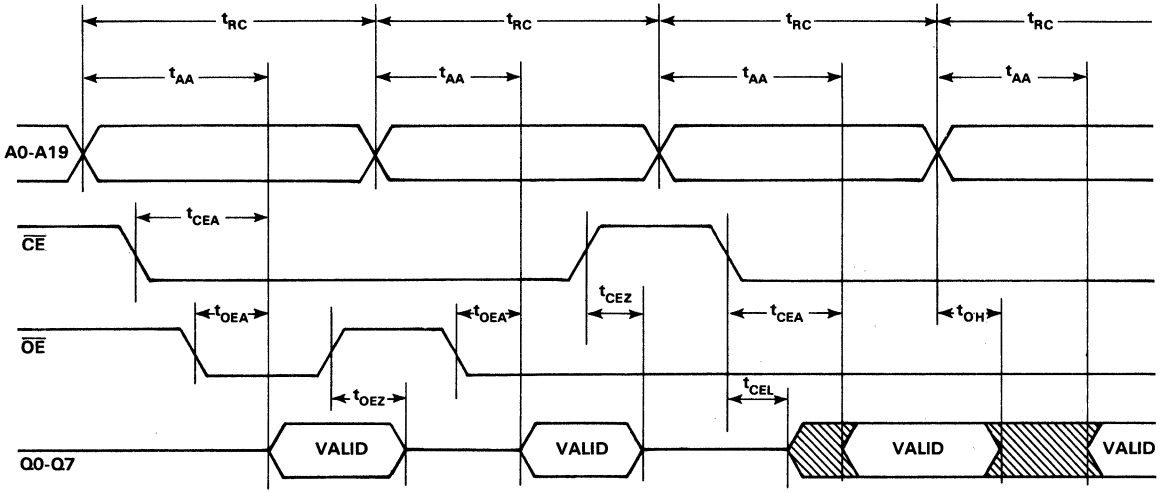
SYM	PARAMETER	-25		UNITS	NOTES
		MIN	MAX		
t_{RC}	Read Cycle Time	250		ns	
t_{AA}	Address Access Time		250	ns	
t_{CEA}	CE Access Time		250	ns	
t_{CEZ}	Chip Enable Data Off Time		40	ns	
t_{CEL}	Chip Enable to Data Bus Active	5		ns	
t_{OEA}	Output Enable Access Time		50	ns	
t_{OEZ}	Output Enable Data Off Time		40	ns	
t_{OH}	Output Hold from Address Change	5		ns	

CAPACITANCE
($0°C \leq T_A \leq 70°C$)

SYM	PARAMETER	TYP	MAX	UNITS	NOTES
C_I	Input Capacitance	5		pF	
C_O	Output Capacitance	7		pF	5

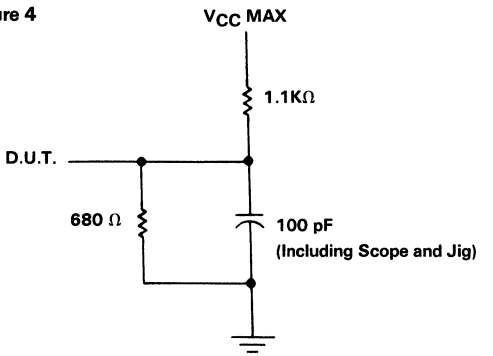
III

TIMING DIAGRAM
Figure 3



NOTES:
1. All voltages referenced to GND.
2. Measured with $0.4\ V \leq V_O \leq 5.0\ V$ outputs deselected and $V_{CC} = 5\ V$.
3. $V_{IN} = 0\ V$ to $5.25\ V$.
4. Input and output timing reference levels are at 1.5 V for inputs and .8 and 2.0 for outputs.
5. Measured with outputs open.
6. A minimum of 2 ms time delay is required after the application of V_{CC} (+5) before proper device operation is achieved. $\overline{CE}$ must be at V_{IH} for this time period.
7. $\overline{CE}$ high.
8. Negative undershoots to a minimum of −1.5 V are allowed with a maximum of 10 ns pulse width.
9. Measured with a load as shown in Figure 4.
10. A.C. measurements assume transition time = 5 ns levels GND to 3 V.

OUTPUT LOAD
Figure 4



DESCRIPTION (continued)

As a member of the Mostek BYTEWYDE Memory Family, the MK38000 allows compatibility between RAM, ROM, and EPROM. The MK38000 can be used as a pin/function density upgrade to the MK37000 8K x 8 bit ROM.

The output enable function controls only the outputs. The $\overline{CE}$ input can be used for device selection and the $\overline{OE}$ input used to avoid bus conflicts so that outputs can be 'OR'ed together when using multiplexed or bi-directional busses.

Other system oriented features include fully TTL compatible inputs and outputs. The three state outputs, controlled by the $\overline{OE}$ input, will drive a minimum of 2 standard TTL loads. The MK38000 operates from a single +5 volt power supply. It is packaged in the industry standard 28 pin DIP. Pin 27 is not connected in order to maintain compatiblity with RAMs which use this pin as a write enable ($\overline{WE}$) control function.

Any application requiring a high performance high bit density ROM can be satisfied by the MK38000. This device is ideally suited for 8 bit microprocessor systems such as those which can utilize the MK3880. It can offer significant cost advantages over PROM.

OPERATION

The MK38000 is controlled by the chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) inputs. A low level at the $\overline{CE}$ input powers up the memory for an active cycle. The output buffers, under the control of $\overline{OE}$, will become active in $\overline{CE}$ access time (t_{CEA}) if the output enable access time (t_{OEA}) requirement is met.

By maintaining valid address, the outputs will remain valid and active until either $\overline{CE}$ or $\overline{OE}$ is returned to the high state or until an address is changed. After chip deselect time (t_{CEZ}) or output enable deselect time (t_{OEZ}), the output buffers will go to a high impedance state.

MK38000 ROM CODE DATA INPUT PROCEDURE

The preferred method of supplying code data to Mostek is in the form of programmed EPROMs (see table). In addition to the programmed set, Mostek requires an additional set of blank EPROMs for supplying customer code verification. When multiple EPROMs are required to describe the ROM, they shall be designated in ascending address space with the numbers 1, 2, 3, etc. As an example, EPROM #1 would start with address space 0000 and go to 1FFF for an 8K x 8 device. EPROM #2 would then start at address space 2000 and so on. A total of four 8K x 8 devices would be required to totally describe the address space of the 32K x 8 MK38000.

A paper printout and verification approval letter will accompany each verification EPROM set returned to the customer. Approval is considered to be accepted when the signed verification letter is returned to Mostek. The original set of EPROMs will be retained by Mostek for the duration of the prototyping process.

ACCEPTABLE EPROMs FOR CODE DATA

Table 1

EPROM	# REQUIRED
2732	8
2764	4

Guidelines for Submitting and Verifying Customer ROM Patterns

ROM PROGRAMMING GUIDE

It has always been Mostek's policy to service its customers ROM needs in the most efficient way possible. In continuing with this effort, Mostek has revised its ROM procedure to better facilitate the market we serve. This new ROM programming guide and information form will insure that all pertinent information is received with the purchase order. This will reduce the unnecessary delavs which develop when sufficient information is not available.

DESCRIPTION OF ROM FORM

The first part of the ROM programming form is concerned with providing all necessary customer information to Mostek. This will simplify any correspondence which may be necessary to complete the order in question.

The ROM generic type simply indicates the ROM series the customer wishes to purchase. This includes the following Mostek series.

MK34000 Series
MK36000 Series
MK37000 Series
MK38000 Series

PACKAGE TYPE

The package type must be included on both the ROM form and the purchase order to prevent parts being produced in the wrong package. Currently, all prototypes and any follow-on quantities built in Dallas will be ceramic. Remember: P = Ceramic, N = Plastic, J = Cerdip.

CUSTOMER NUMBERS

In the event the customer assigns a part number to the Mostek ROM selected, this number should be entered on the ROM form. This number will simplify any communication which may be necessary between the customer and Mostek.

SPECIAL BRANDING

Special branding of Mostek ROMs is possible if the instructions are indicated on the ROM programming form. But due to space and printing limitations, any special branding desired must be limited to 12 characters on one line.

CUSTOMER SPECIFICATIONS

If the customer desires different specifications for the ROM selected than appears on the appropriate Mostek data sheet; it is imperative that these specification changes be well documented and sent to Mostek as early as possible. This is important because any specification change must be reviewed and accepted by Mostek before the ROM order can be processed.

ROM DATA

Mostek will accept a number of media and formats for the inputting of programming data. This flexibility will make it easy for a customer to have his ROM order processed as quickly as possible. The following table shows the media that can be most easily processed by Mostek. When filling out the ROM programming form, check the appropriate block under pattern media.

PATTERN MEDIA

ROMs/PROMs: On Mostek's ROMs of 16K bit and larger density, PROMs of the 2716, 2732, or 2764 type or pin compatible ROMs may be submitted for the ROM contents. They must, however, be accompanied by the information required for the Mostek ROM type in written form. Each PROM or ROM submitted must also be clearly marked so that no question arises as to its starting memory location. (See ROM Programming Form on last page).

VERIFICATION MEDIA

For pattern verification, Mostek will supply a printout and reprogrammed PROMs or magnetic tape.

To insure rapid turnaround of data verification information, acceptable media should be used as outlined in the table. If another method is desired, contact Mostek so that all arrangements can be made and an accurate schedule can be generated. Quick turnaround of verification information cannot be guaranteed in cases where new software has to be developed. Remember, when filling out the ROM programming form, check the appropriate block under verification media.

HOW THE PROGRAM WORKS

Mostek's ROM program is designed for maximum safety with two verification steps that limit the liability of both the

customer and Mostek. However, if circumstances dictate, Mostek is flexible enough to vary its procedures to better serve its customers.

PATTERN VERIFICATION

Upon receipt of the ROM programming information form and the ROM input data, Mostek engineering will re-generate the pattern data for customer verification. At this point the only customer liability is a nominal data charge in the event of a pattern change. Following customer verification, Mostek begins prototype production. Customer is now liable for mask charge and minimum order quantity work in process.

The verification step can be waived so that prototype production begins immediately upon receipt of the input data. The time savings is the time for Mostek engineering to generate verification plus the time necessary for the customer to receive and verify the data. This savings is usually less than two weeks. If data verification is waived, the customer is liable for the mask charge plus the minimum order quantity work-in-process material.

PROTOTYPE VERIFICATION

The second verification step in Mostek's ROM program is that of prototype verification. The prototype quantity is usually 25 parts which are considered part of the order quantity for billing purposes. After the customer has verified the prototype, in writing, as being correct, Mostek will proceed with the production of the total remaining order.

The prototype verification step can also be waived and Mostek will immediately begin production instead of prototyping. The time savings gained from waiving prototype verification is usually 5-6 weeks. If prototype verification is waived, the customer is liable for the mask charge plus all work-in-process material. If only prototype verification is waived Mostek guaranties ROM data to agree with data verified by customer.

WAIVERS OF VERIFICATION

Arrangements must be worked out with Mostek prior to committing deliveries based on verification waivers. If an order is accepted by Mostek waiving pattern verification, the quoted cycle time begins upon receipt of the input data and only a small quantity of parts will be produced as prototypes. If Mostek accepts an order waiving prototype verification, the quoted cycle time will begin upon notification of pattern verification and placement of order.

GENERAL INFORMATION

Production capacity cannot be reserved without written verification in house and a purchase order. Therefore any quotes for delivery will be subject to change until a purchase order is obtained.

Limited quantities of parts are usually available from the Mostek Dallas assembly facility shortly after prototype shipments, but prior to standard follow on production. These units will require an expedite adder in addition to the standard price.

The appropriate Mostek price sheet contains information on order minimums and price adders.

ACCEPTABLE MEDIA

Table 1

MK Type	ROM	PROM	Magnetic Tape
MK34000P/N/J	X	X	X
MK36000P/N/J	X	X	X
MK37000P/N/J	X	X	X
MK38000P/N/J	X	X	X

READ ONLY MEMORIES

Table 2

Device	Organization	Logic	Number Bits	Access	Supply Voltages		Power Dis (mW) Max	Package		BYTEWYDE Pinout
					V_{CC}	V_{SS}		Type	Pins	
MK34000	2048x8	Static	16384	350 ns	+5	0	330	P/N/J	24	Yes
MK36000	8192x8	Dynamic	65536	200 ns	+5	0	220	P/N/J	24	No
MK37000	8192x8	Dynamic	65536	200 ns	+5	0	220	P/N/J	28	Yes
MK38000	32768x8	Static	262144	150 ns	+5	0	495	P/N/J	28	Yes

III

ROM CROSS REFERENCE

Table 3

Mostek	AMD	NEC	Motorola	AMI	GI	Synertek	National	Signetics	Toshiba	SMC
MK34000	AM9218	μPD2316E	MCM68316E	S6831B	RO-3-9316	SY2316B	MM52116	2616	TMM334P	2316E
MK36000		μPD2364	MCM68364	S4264	RO-3-9364	SY2364	MM52164	2664A		36000
MK37000	AM9265								TMM2364P	
MK38000									TMM 23256	

ROM PROGRAMMING FORM

Customer Name _____

Address _____

City _____ State _____ Zip _____

Phone ( ) _____ Extension _____

Customer Contact _____ Title _____

Mostek Rep or Dist _____

ROM Generic Type _____	Customer Part #	Brand
(Including Pkg, Speed)	_____	_____
☐ Standard data sheet part	_____	_____
☐ Customer Spec # _____	_____	_____
Date customer spec sent	_____	_____
to Mostek _____	_____	_____
Spec review complete ☐ Yes	_____	_____

Pattern Media	Verification Media
☐ PROM type _____	☐ PROM type _____
☐ Pin Compatible ROMs - Note 1	☐ Pin Compatible ROMs - Note 1
☐ Magnetic Tape - Note 1	☐ Magnetic Tape - Note 1
☐ Other - Note 1	☐ Other - Note 1 (Note 1-Requires Factory Coordination)

Date Pattern Data Sent to Mostek _____

Does Customer Require Prototypes	Yes _____	No _____
Pattern Verification Required by Customer	Yes _____	Waived _____
Prototype Verification Required by Customer	Yes _____	Waived _____
Pattern Verification To Be Sent To	Rep _____	Customer _____

Customer signature approving waivers _____

Customer Order Number _____ Date _____

Order Quantity and Price _____

Delivery Requested/Committed Prototypes _____ Production _____

Form Completed By _____ Date _____

1982/1983 MICROELECTRONIC DATA BOOK

MOSTEK®

4096x1-BIT DYNAMIC RAM

MK4027(J/N)-2/3

FEATURES

- ☐ Industry standard 16-pin DIP (MK 4096) configuration
- ☐ 120ns access time, 320ns cycle (MK4027-1)
  150ns access time, 320ns cycle (MK4027-2)
  200ns access time, 375ns cycle (MK4027-3)
- ☐ ±10% tolerance on all supplies (+12V, ±5V)
- ☐ ECL compatible on V_{BB} power supply (−5.7V)
- ☐ Low Power: 462mW active (max)
  27mW standby (max)
- ☐ Improved performance with "gated $\overline{CAS}$", "$\overline{RAS}$ only" refresh and page mode capability
- ☐ All inputs are low capacitance and TTL compatible
- ☐ Input latches for addresses, chip select and data in
- ☐ Three-state TTL compatible output
- ☐ Output data latched and valid into next cycle
- ☐ MKB version screened to MIL-STD-883

IV

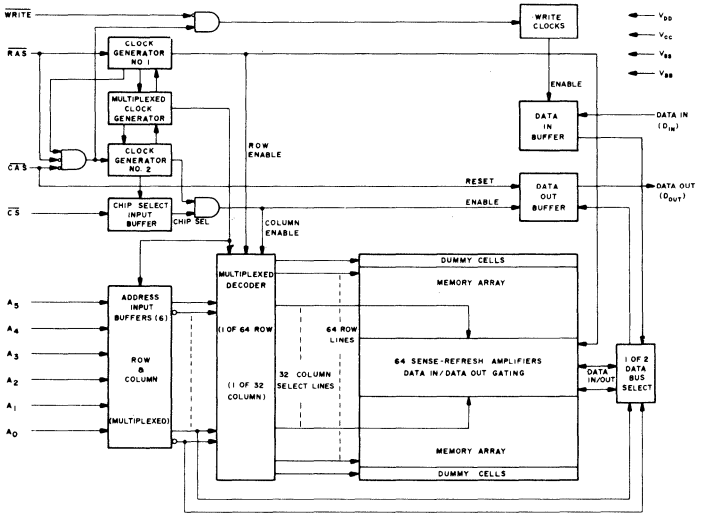
DESCRIPTION

The MK 4027 is a 4096 word by 1 bit MOS random access memory circuit fabricated with MOSTEK's N-channel silicon gate process. This process allows the MK 4027 to be a high performance state-of-the-art memory circuit that is manufacturable in high volume. The MK 4027 employs a single transistor storage cell utilizing a dynamic storage technique and dynamic control circuitry to achieve optimum performance with low power dissipation.

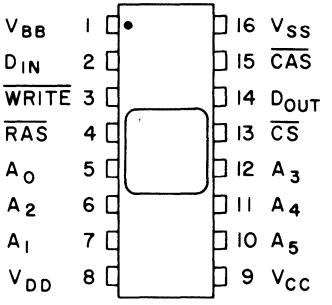
A unique multiplexing and latching technique for the address inputs permits the MK 4027 to be packaged in a standard 16-pin DIP on 0.3 in. centers. This package size provides high system-bit densities and is compatible with widely available automated testing and insertion equipment.

System oriented features include direct interfacing capability with TTL, only 6 very low capacitance address lines to drive, on-chip address and data registers which eliminates the need for interface registers, input logic levels selected to optimize noise immunity, and two chip select methods to allow the user to determine the appropriate speed/power characteristics of his memory system. The MK 4027 also incorporates several flexible operating modes. In addition to the usual read and write cycles, read-modify write, page-mode, and $\overline{RAS}$-only refresh cycles are available with the MK 4027. Page-mode timing is very useful in systems requiring Direct Memory Access (DMA) operation.

FUNCTIONAL DIAGRAM



PIN CONNECTIONS



PIN NAMES

A_0-A_5	ADDRESS INPUTS
$\overline{CAS}$	COLUMN ADDRESS STROBE
$\overline{CS}$	CHIP SELECT
D_{IN}	DATA IN
D_{OUT}	DATA OUT
$\overline{RAS}$	ROW ADDRESS STROBE
$\overline{WRITE}$	READ/WRITE INPUT
V_{BB}	POWER (−5V)
V_{CC}	POWER (+5V)
V_{DD}	POWER (+ 12V)
V_{SS}	GROUND

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to V_{BB} ..... −0.5V to +20V
Voltage on V_{DD}, V_{CC} relative to V_{SS} ..... −1.0V to +15V
$V_{BB}-V_{SS}$ ($V_{DD}-V_{SS} > 0$) 0V
Operating temperature, T_A (Ambient) ..... 0°C to + 70°C
Storage temperature (Ambient)(Ceramic) ..... −65°C to + 150°C
Storage temperature (Ambient)(Plastic) ..... −55°C to + 125°C
Short circuit output current 50mA
Power dissipation ..... 1 Watt

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS [4]

($0°C \leq T_A \leq 70°C$) [1]

	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{DD}	Supply Voltage	10.8	12.0	13.2	volts	2
V_{CC}	Supply Voltage	4.5V	5.0	5.5	volts	2,3
V_{SS}	Supply Voltage	0	0	0	volts	2
V_{BB}	Supply Voltage	−4.5	−5.0	−5.7	volts	2
V_{IHC}	Logic 1 Voltage, $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	2.4		7.0	volts	2
V_{IH}	Logic 1 Voltage, all inputs except $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	2.2		7.0	volts	2
V_{IL}	Logic 0 Voltage, all inputs	−1.0		.8	volts	2

DC ELECTRICAL CHARACTERISTICS [4]

($0°C \leq T_A \leq 70°C$)[1] (V_{DD} = 12.0V ± 10%; V_{CC} = 5.0V ± 10%; V_{SS} = 0V; $-5.7V \leq V_{BB} \leq -4.5V$)

	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
I_{DD1}	Average V_{DD} Power Supply Current			35	mA	5
I_{DD2}	Standby V_{DD} Power Supply Current			2	mA	8
I_{DD3}	Average V_{DD} Power Supply Current during "$\overline{RAS}$ only" cycles			25	mA	
I_{CC}	V_{CC} Power Supply Current				mA	6
I_{BB}	Average V_{BB} Power Supply Current			150	μA	
$I_{I(L)}$	Input Leakage Current (any input)			10	μA	7
$I_{O(L)}$	Output Leakage Current			10	μA	8,9
V_{OH}	Output Logic 1 Voltage @ I_{OUT} = −5mA	2.4			volts	
V_{OL}	Output Logic 0 Voltage @ I_{OUT} = 3.2mA			0.4	volts	

NOTES

1. T_A is specified for operation at frequencies to $t_{RC} \geq t_{RC}$ (min). Operation at higher cycle rates with reduced ambient temperatures and higher power dissipation is permissible provided that all AC parameters are met. See figure 2 for derating curve.
2. All voltages referenced to V_{SS}.
3. Output voltage will swing from V_{SS} to V_{CC} when enabled, with no output load. For purposes of maintaining data in standby mode, V_{CC} may be reduced to V_{SS} without affecting refresh operations or data retention. However, the V_{OH} (min) specification is not guaranteed in this mode.
4. Several cycles are required after power-up before proper device operation is achieved. Any 8 cycles which perform refresh are adequate for this purpose.
5. Current is proportional to cycle rate, I_{DD1} (max) is measured at the cycle rate specified by t_{RC} (min). See figure 1 for I_{DD1} limits at other cycle rates.
6. I_{CC} depends on output loading. During readout of high level data V_{CC} is connected through a low impedance (135Ω typ) to Data Out. At all other times I_{CC} consists of leakage currents only.
7. All device pins at 0 volts except V_{BB} which is at −5 volts and the pin under test which is at +10 volts.
8. Output is disabled (high-impedance) and $\overline{RAS}$ and $\overline{CAS}$ are both at a logic 1. Transient stabilization is required prior to measurement of this parameter.
9. $0V \leq V_{OUT} \leq +10V$.
10. Effective capacitance is calculated from the equation:

    $C = \frac{\Delta Q}{\Delta V}$ with ΔV = 3 volts.
11. A.C. measurements assume t_T = 5ns.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS(4, 11, 17)

($0°C \leq T_A \leq 70°C$)[1] (V_{DD} = 12.0V ± 10%, V_{CC} = 5.0V ± 10%, V_{SS} = 0V, −5.7V ≤ V_{BB} ≤ −4.5V)

	PARAMETER	MK4027-2		MK4027-3		UNITS	NOTES
		MIN	MAX	MIN	MAX		
t_{RC}	Random read or write cycle time	320		375		ns	12
t_{RWC}	Read write cycle time	320		375		ns	12
t_{RMW}	Read modify write cycle time	320		405		ns	12
t_{PC}	Page mode cycle time	170		225		ns	12
t_{RAC}	Access time from row address strobe		150		200	ns	13, 15
t_{CAC}	Access time from column address strobe		100		135	ns	14, 15
t_{OFF}	Output buffer turn-off delay		40		50	ns	
t_{RP}	Row address strobe precharge time	100		120		ns	
t_{RAS}	Row address strobe pulse width	150	10,000	200	10,000	ns	
t_{RSH}	Row address strobe hold time	100		135		ns	
t_{CAS}	Column address strobe pulse width	100		135		ns	
t_{CSH}	Column address strobe hold time	150		200		ns	
t_{RCD}	Row to column strobe delay	20	50	25	65	ns	16
t_{ASR}	Row address set-up time	0		0		ns	
t_{RAH}	Row address hold time	20		25		ns	
t_{ASC}	Column address set-up time	−10		−10		ns	
t_{CAH}	Column address hold time	45		55		ns	
t_{AR}	Column address hold time referenced to $\overline{RAS}$	95		120		ns	
t_{CSC}	Chip select set-up time	−10		−10		ns	
t_{CH}	Chip select hold time	45		55		ns	
t_{CHR}	Chip select hold time referenced to $\overline{RAS}$	95		120		ns	
t_T	Transition time (rise and fall)	3	35	3	50	ns	17
t_{RCS}	Read command set-up time	0		0		ns	
t_{RCH}	Read command hold time	0		0		ns	
t_{WCH}	Write command hold time	45		55		ns	
t_{WCR}	Write command hold time referenced to $\overline{RAS}$	95		120		ns	
t_{WP}	Write command pulse width	45		55		ns	
t_{RWL}	Write command to row strobe lead time	50		70		ns	
t_{CWL}	Write command to column strobe lead time	50		70		ns	
t_{DS}	Data in set-up time	0		0		ns	18
t_{DH}	Data in hold time	45		55		ns	18
t_{DHR}	Data in hold time referenced to $\overline{RAS}$	95		120		ns	
t_{CRP}	Column to row strobe precharge time	0		0		ns	
t_{CP}	Column precharge time	60		80		ns	
t_{RFSH}	Refresh period		2		2	ms	
t_{WCS}	Write command set-up time	0		0		ns	19
t_{CWD}	$\overline{CAS}$ to $\overline{WRITE}$ delay	60		80		ns	19
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ delay	110		145		ns	19
t_{DOH}	Data out hold time	10		10		μs	

Notes Continued

12. The specifications for t_{RC} (min) and t_{RWC} (min) are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \leq T_A \leq 70°C$) is assured. See figure 2 for derating curve.

13. Assumes that $t_{RCD} \leq t_{RCD}$ (max).

14. Assumes that $t_{RCD} \geq t_{RCD}$ (max).

15. Measured with a load circuit equivalent to 2 TTL loads and 100pF

16. Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.

17. V_{IHC} (min) or V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IHC} or V_{IH} and V_{IL}.

18. These parameters are referenced to $\overline{CAS}$ leading edge in random write cycles and to $\overline{WRITE}$ leading edge in delayed write or read-modify-write cycles.

19. t_{WCS}, t_{CWD}, and t_{RWD} are restrictive operating parameters in a read/write or read/modify/write cycle only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and Data Out will contain the data written into the selected cell. If $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min), the cycle is a read-write cycle and Data Out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of Data Out (at access time) is indeterminate.

AC ELECTRICAL CHARACTERISTICS

($0°C \leq T_A \leq 70°C$) ($V_{DD} = 12.0V \pm 10\%$; $V_{SS} = 0V$; $-5.7V \leq V_{BB} \leq -4.5V$)

	PARAMETER	TYP	MAX	UNITS	NOTES
C_{I1}	Input Capacitance (A_0-A_5), D_{IN}, $\overline{CS}$	4	5	pF	10
C_{I2}	Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	8	10	pF	10
C_O	Output Capacitance (D_{OUT})	5	7	pF	8,10

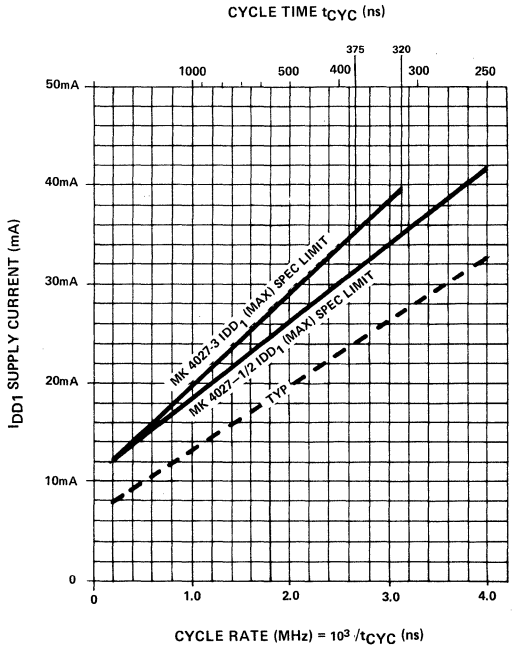


Figure 1. Maximum I_{DD1} versus cycle rate for device operation at extended frequencies.

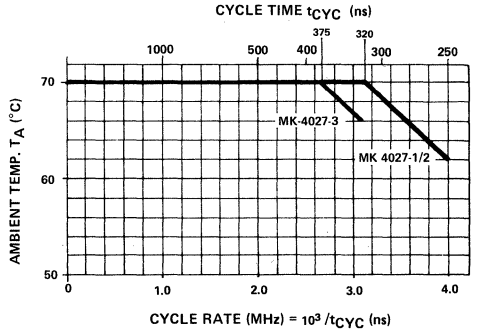
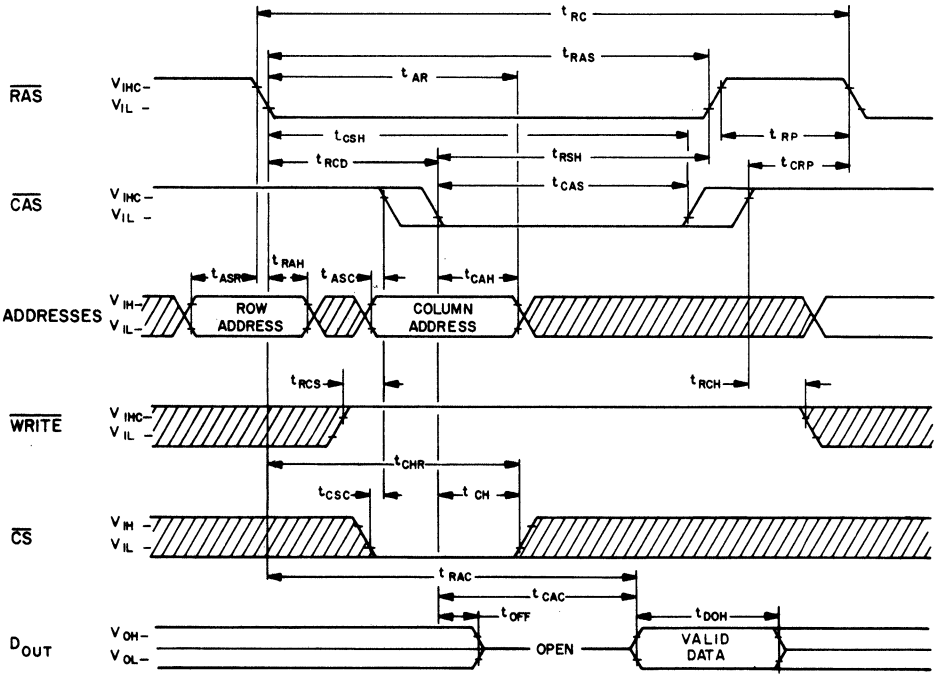


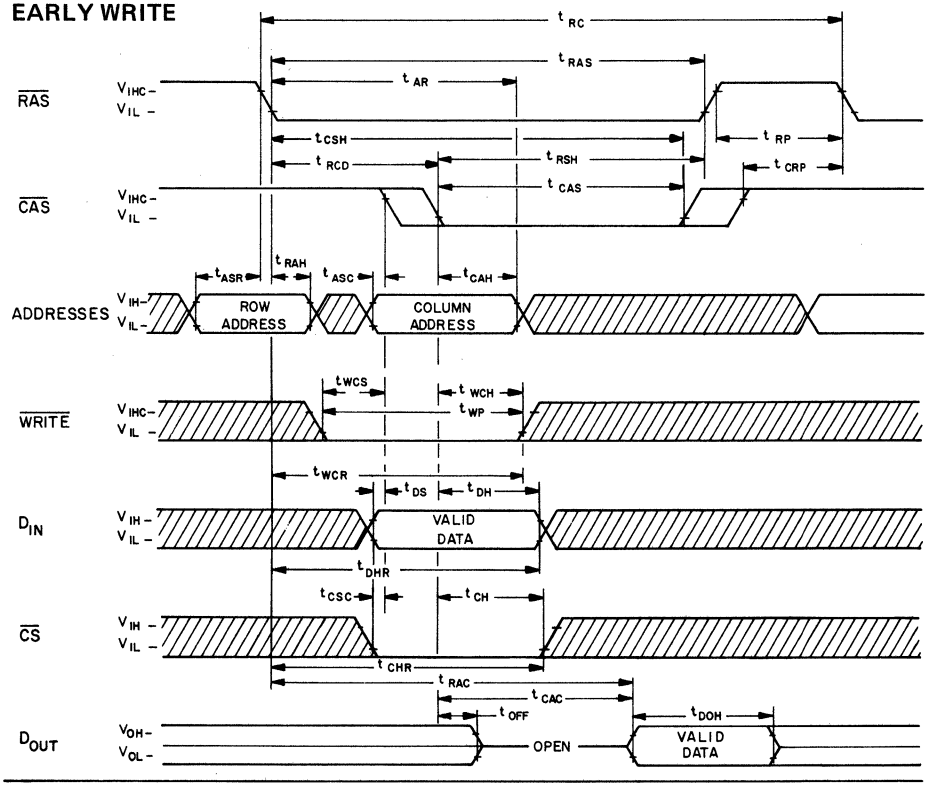
Figure 2. Maximum ambient temperature versus cycle rate for extended frequency operation.

READ CYCLE

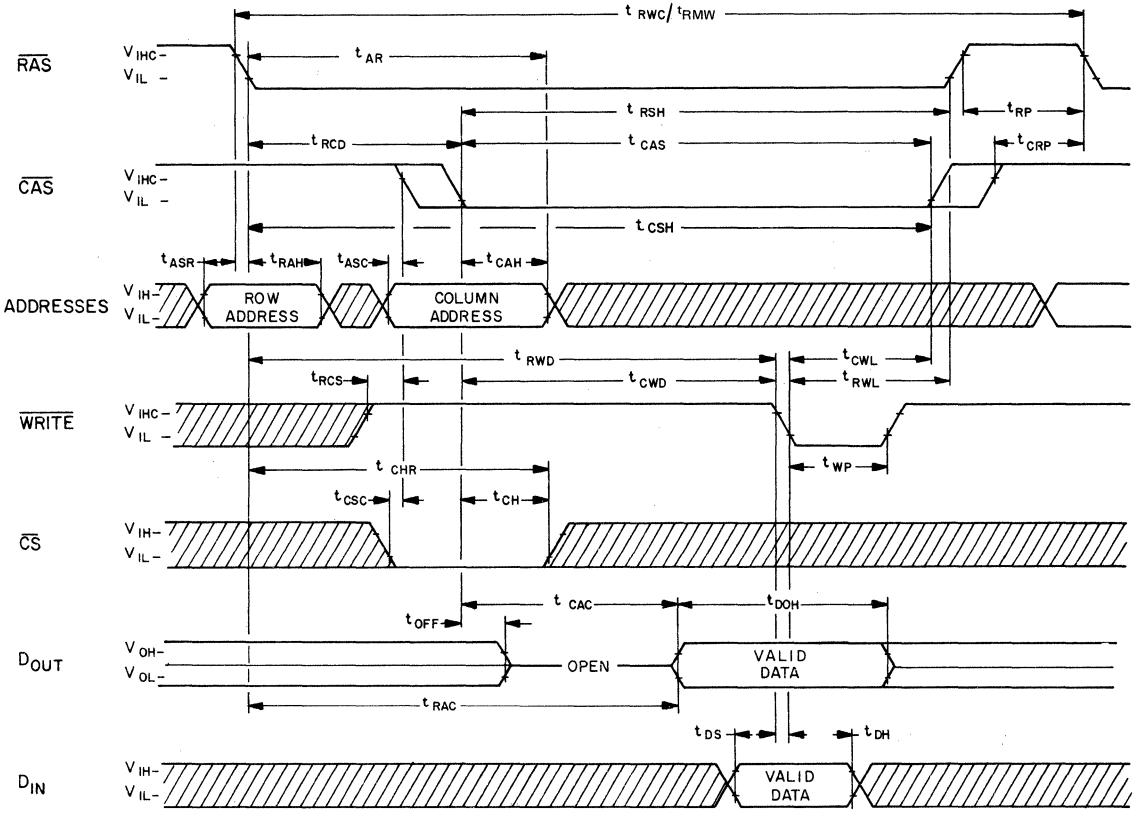


IV

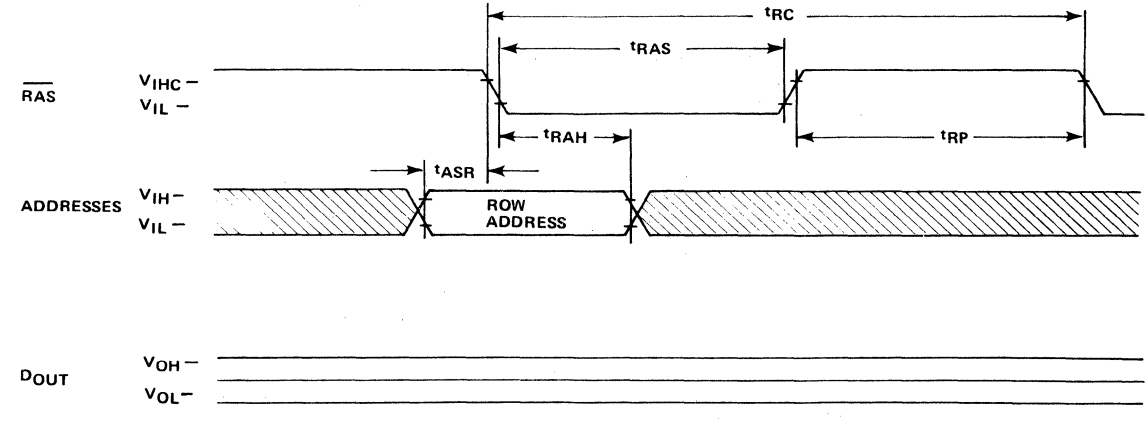
EARLY WRITE



READ-WRITE / READ-MODIFY-WRITE CYCLE

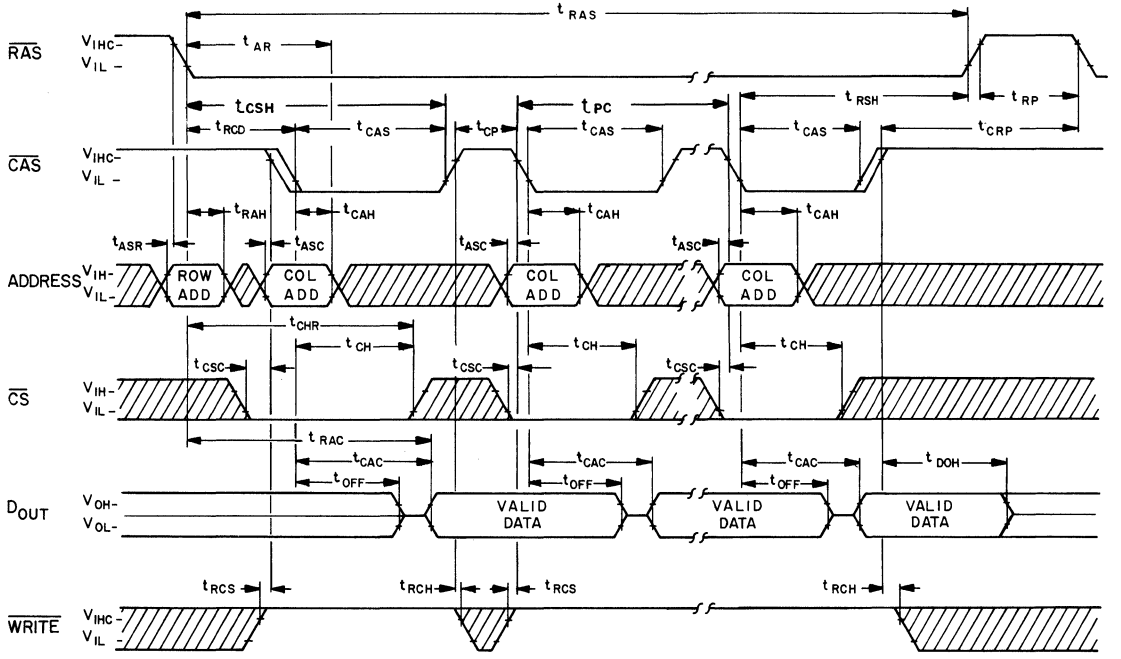


"RAS ONLY" REFRESH CYCLE

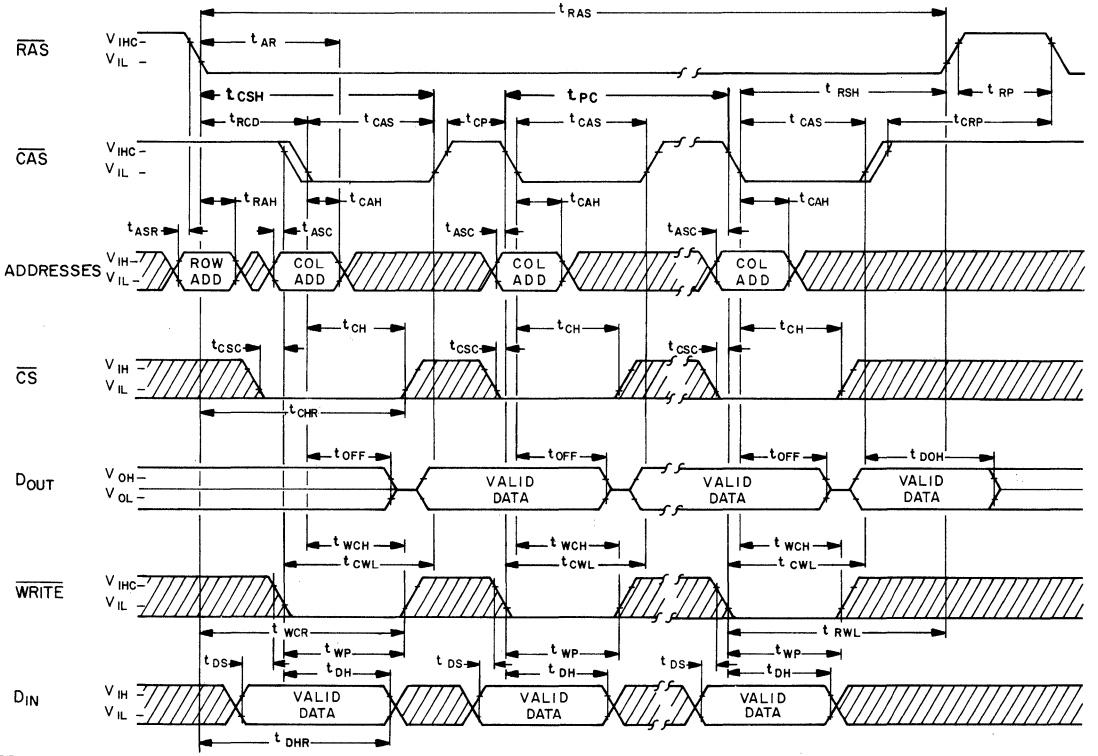


NOTE: D_{OUT} remains unchanged from previous cycle.

PAGE MODE READ CYCLE



PAGE MODE WRITE CYCLE



ADDRESSING

The 12 address bits required to decode1 of the 4096 cell locations within the MK 4027 are multiplexed onto the 6 address inputs and latched into the on-chip address latches by externally applying two negative going TTL level clocks. The first clock, the Row Address Strobe ($\overline{RAS}$), latches the 6 row address bits into the chip. The second clock, the Column Address Strobe ($\overline{CAS}$), subsequently latches the 6 column address bits plus Chip Select ($\overline{CS}$) into the chip. The internal circuitry of the MK 4027 is designed to allow the column information to be externally applied to the chip before it is actually required. Because of this, the hold time requirements for the input signals associated with the Column Address Strobe are also referenced to $\overline{RAS}$. However, this gated $\overline{CAS}$ feature allows the system designer to compensate for timing skews that may be encountered in the multiplexing operation. Since the Chip Select signal is not required until $\overline{CAS}$ time, which is well into the memory cycle,its decoding time does not add to system access or cycle time.

DATA INPUT/OUTPUT

Data to be written into a selected cell is latched into an on-chip register by a combination of $\overline{WRITE}$ and $\overline{CAS}$ while $\overline{RAS}$ is active. The later of the signals ($\overline{WRITE}$ or $\overline{CAS}$) to make its negative transition is the strobe for the Data In register. This permits several options in the write cycle timing. In a write cycle, if the $\overline{WRITE}$ input is brought low prior to $\overline{CAS}$, the Data In is strobed by $\overline{CAS}$, and the set-up and hold times are referenced to $\overline{CAS}$. If the data input is not available at $\overline{CAS}$ time or if it is desired that the cycle be a read-write cycle, the $\overline{WRITE}$ signal must be delayed until after $\overline{CAS}$. In this "delayed write cycle" the data input set-up and hold times are referenced to the negative edge of $\overline{WRITE}$ rather than to $\overline{CAS}$. (To illustrate this feature, Data In is referenced to $\overline{WRITE}$ in the timing diagram depicting the read-write and page mode write cycles while the "early write" cycle diagram shows Data In referenced to $\overline{CAS}$.) Note that if the chip is unselected ($\overline{CS}$ high at $\overline{CAS}$ time) $\overline{WRITE}$ commands are not executed and, consequently, data stored in the memory is unaffected.

Data is retrieved from the memory in a read cycle by maintaining $\overline{WRITE}$ in the inactive or high state throughout the portion of the memory cycle in which $\overline{CAS}$ is active. Data read from the selected cell will be available at the output within the specified access time.

DATA OUTPUT LATCH

Any change in the condition of the Data Out Latch is initiated by the $\overline{CAS}$ signal. The output buffer is not affected by memory (refresh) cycles in which only the $\overline{RAS}$ signal is applied to the MK 4027. Whenever $\overline{CAS}$ makes a negative transition, the output will go unconditionally open-circuited, independent of the state of any other input to the chip. If the cycle in progress is a read,read-modify-write, or a delayed write cycle and the chip is selected, then the output latch and buffer will again go active and at access time will contain the data read from the selected cell. This output data is the same polarity (not inverted) as the input data. If the cycle in progress is a write cycle ($\overline{WRITE}$ active low before $\overline{CAS}$ goes low) and the chip is selected, then at access time the output latch and buffer will contain the input data. Once having gone active, the output will remain valid until the MK 4027 receives the next $\overline{CAS}$ negative edge. Intervening refresh cycles in which a $\overline{RAS}$ is received (but no $\overline{CAS}$) will not cause valid data to be affected. Conversely, the output will assume the open-circuit state during any cycle in which the MK 4027 receives a $\overline{CAS}$ but no $\overline{RAS}$ signal (regardless of the state of any other inputs). The output will also assume the open circuit state in normal cycles (in which both $\overline{RAS}$ and $\overline{CAS}$ signals occur) if the chip is unselected.

The three-state data output buffer presents the data output pin with a low impedance to V_{CC} for a logic 1 and a low impedance to V_{SS} for a logic 0. The output resistance to V_{CC} (logic 1 state) is 420 Ω maximum and 135 Ω typically. The output resistance to V_{SS} (logic 0 state) is 125Ω maximum and 35 Ω typically. The separate V_{CC} pin allows the output buffer to be powered from the supply voltage of the logic to which the chip is interfaced. During battery standby operation, the V_{CC} pin may have power removed without affecting the MK 4027 refresh operation. This allows all system logic except the $\overline{RAS}$ timing circuitry and the refresh address logic to be turned off during battery standby to conserve power.

REFRESH

Refresh of the dynamic cell matrix is accomplished by performing a memory cycle at each of the 64 row addresses within each 2 millisecond time interval. Any cycle in which a $\overline{RAS}$ signal occurs, accomplishes a refresh operation. A read cycle will refresh the selected row, regardless of the state of the Chip Select ($\overline{CS}$) input. A write or read-modify-write cycle also refreshes the selected row, but the chip should be unselected to prevent writing data into the selected cell. If, during a refresh cycle, the MK 4027 receives a $\overline{RAS}$ signal but no $\overline{CAS}$ signal, the state of the output will not be affected. However, if "$\overline{RAS}$-only" refresh cycles (where $\overline{RAS}$ is the only signal applied to the chip) are continued for extended periods, the output buffer may eventually lose proper data and go open-circuit. The output buffer will regain activity with the first cycle in which a $\overline{CAS}$ signal is applied to the chip.

POWER DISSIPATION/STANDBY MODE

Most of the circuitry used in the MK 4027 is dynamic and most of the power drawn is the result of an address strobe edge. Because the power is not drawn during the whole time the strobe is active, the dynamic power is a function of operating frequency rather than active duty cycle. Typically, the power is 170mW at 1 μsec cycle rate for the MK 4027 with a worse case power of less than 470mW at 320nsec cycle time. To minimize the overall system power, the Row Address Strobe ($\overline{RAS}$) should be decoded and supplied to only the selected chips. The $\overline{CAS}$ must be supplied to all chips (to turn off the unselected output). Those chips that did not receive a $\overline{RAS}$, however, will not dissipate any power on the $\overline{CAS}$ edges, except for that required to turn off the outputs. If the $\overline{RAS}$ signal is decoded and supplied only to the selected chips, then the Chip Select ($\overline{CS}$) input of all chips can be at a logic 0. The chips that receive a $\overline{CAS}$ but no $\overline{RAS}$ will be unselected (output open-circuited) regardless of the Chip Select input. For refresh cycles, however, either the $\overline{CS}$ input of all chips must be high or the $\overline{CAS}$ input must be held high to prevent several "wire-OR'd" outputs from turning on with opposing force. Note that the MK 4027 will dissipate considerably less power when the refresh operation is accomplished with a "$\overline{RAS}$-only" cycle as opposed to a normal $\overline{RAS}/\overline{CAS}$ memory cycle.

PAGE MODE OPERATION

The "Page Mode" feature of the MK 4027 allows for successive memory operations at multiple column locations of the same row address with increased speed without an increase in power. This is done by strobing the row address into the chip and keeping the $\overline{RAS}$ signal at a logic 0 throughout all successive memory cycles in which the row address is common. This "page mode" of operation will not dissipate the power associated with the negative going edge of $\overline{RAS}$. Also, the time required for strobing in a new row address is eliminated, thereby decreasing the access and cycle times. The chip select input ($\overline{CS}$) is operative in page mode cycles just as in normal cycles. It is not necessary that the chip be selected during the first operation in a sequence of page cycles. Likewise, the $\overline{CS}$ input can be used to select or disable any cycle(s) in a series of page cycles. This feature allows the page boundary to be extended beyond the 64 column locations in a single chip. The page boundary can be extended by applying $\overline{RAS}$ to multiple 4K memory blocks and decoding $\overline{CS}$ to select the proper block.

POWER UP

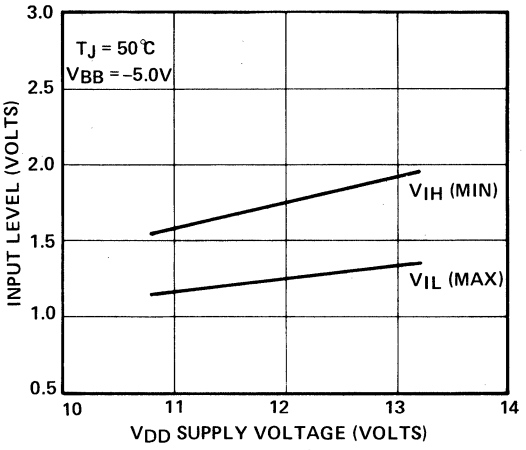
The MK 4027 requires no particular power supply sequencing so long as the Absolute Maximum Rating Conditions are observed. However, in order to insure compliance with the Absolute Maximum Ratings, MOSTEK recommends sequencing of power supplies such that V_{BB} is applied first and removed last. V_{BB} should never be more positive than V_{SS} when power is applied to V_{DD}.

Under system failure conditions in which one or more supplies exceed the specified limits significant additional margin against catastrophic device failure may be achieved by forcing $\overline{RAS}$ and Data Out to the inactive state.

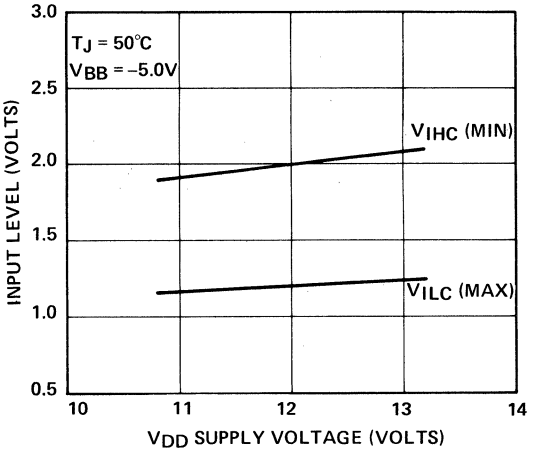
After power is applied to the device, the MK 4027 requires several cycles before proper device operation is achieved. Any 8 cycles which perform refresh are adequate for this purpose.

TYPICAL DEVICE CHARACTERISTICS

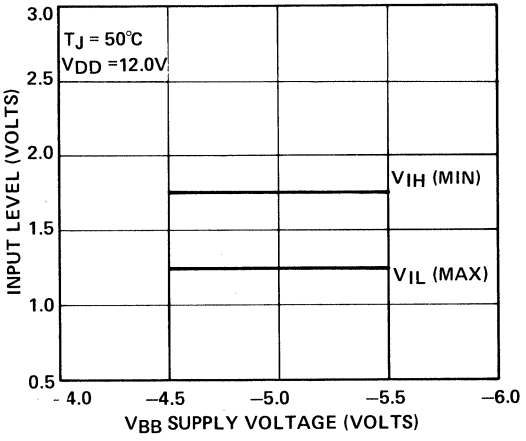
TYPICAL ADDRESS AND DATA INPUT LEVELS vs. V_{DD}



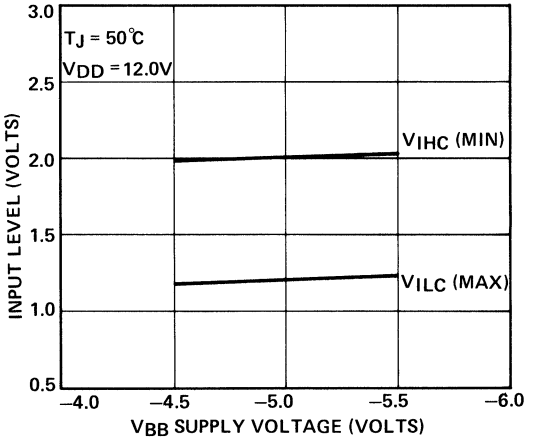
TYPICAL CLOCK INPUT LEVELS vs. V_{DD}



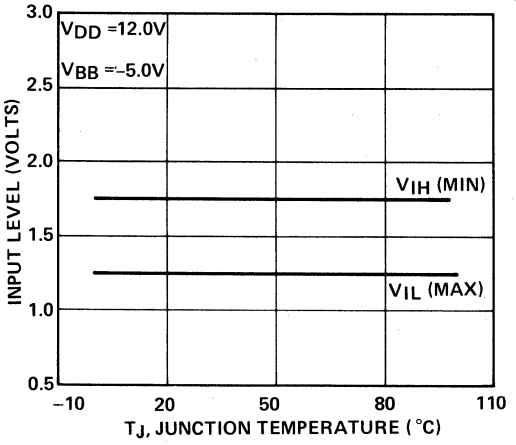
TYPICAL ADDRESS AND DATA INPUT LEVELS vs. V_{BB}



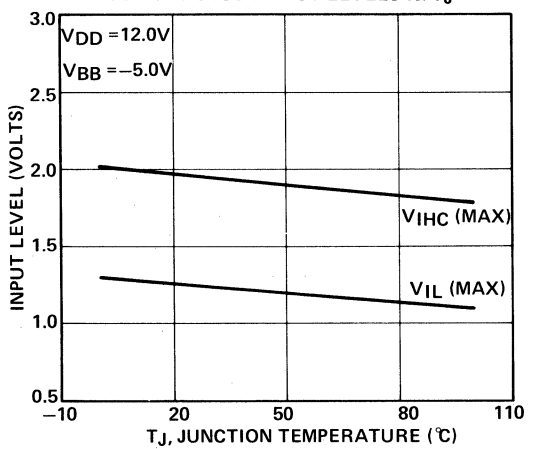
TYPICAL CLOCK INPUT LEVELS vs. V_{BB}



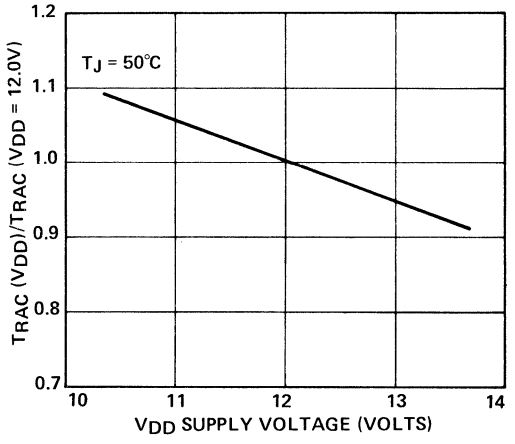
TYPICAL ADDRESS AND DATA INPUT LEVELS vs. T_J



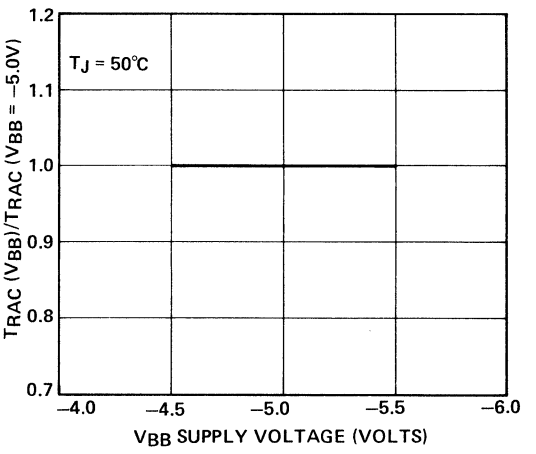
TYPICAL CLOCK INPUT LEVELS vs. T_J



TYPICAL ACCESS TIME (NORMALIZED) vs. V_{DD}

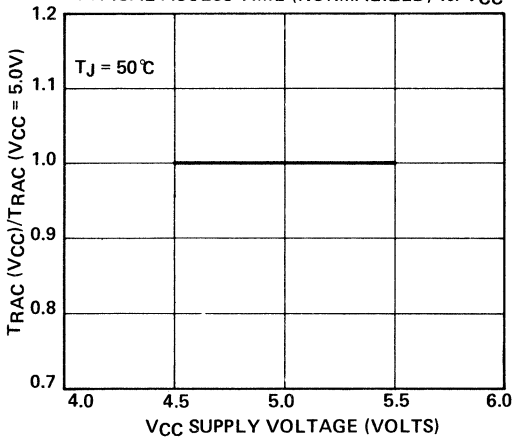


TYPICAL ACCESS TIME (NORMALIZED) vs. V_{BB}

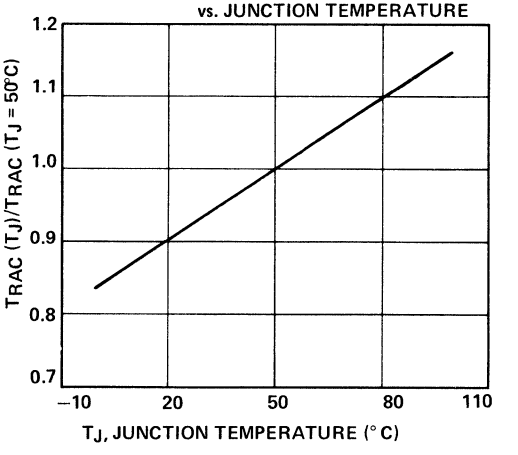


IV

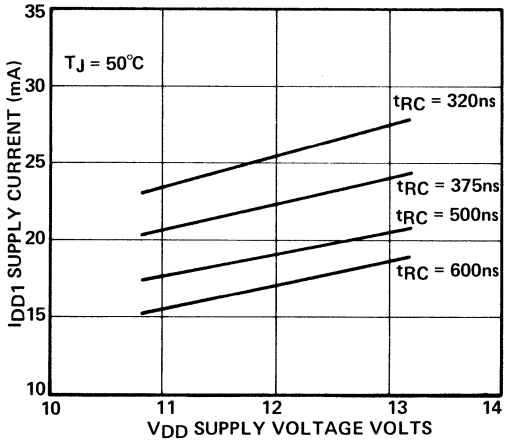
TYPICAL ACCESS TIME (NORMALIZED) vs. V_{CC}



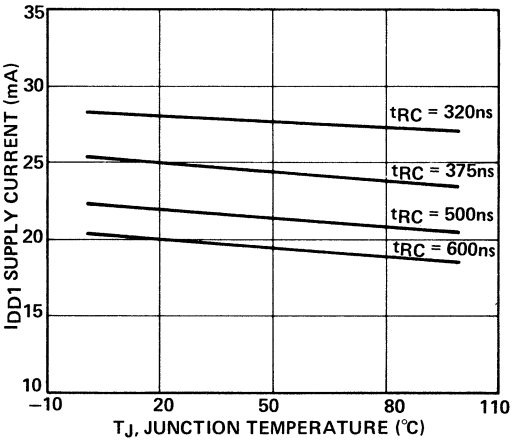
TYPICAL ACCESS TIME (NORMALIZED) vs. JUNCTION TEMPERATURE



TYPICAL I_{DD1} vs. V_{DD}



TYPICAL I_{DD1} vs. JUNCTION TEMPERATURE



MOSTEK®

4096 x 1-BIT DYNAMIC RAM

MK4027(J/N)-4

FEATURES

- ☐ Industry standard 16-pin DIP (MK 4096) configuration
- ☐ 250ns access time, 380ns cycle
- ☐ ±10% tolerance on all supplies (+12V, ±5V)
- ☐ ECL compatible on V_{BB} power supply (−5.7V)
- ☐ Low Power: 462mW active (max)
  27mW standby (max)
- ☐ Improved performance with "gated $\overline{CAS}$", "$\overline{RAS}$ only" refresh and page mode capability
- ☐ All inputs are low capacitance and TTL compatible
- ☐ Input latches for addresses, chip select and data in
- ☐ Three-state TTL compatible output
- ☐ Output data latched and valid into next cycle
- ☐ MKB version screened to MIL-STD-883

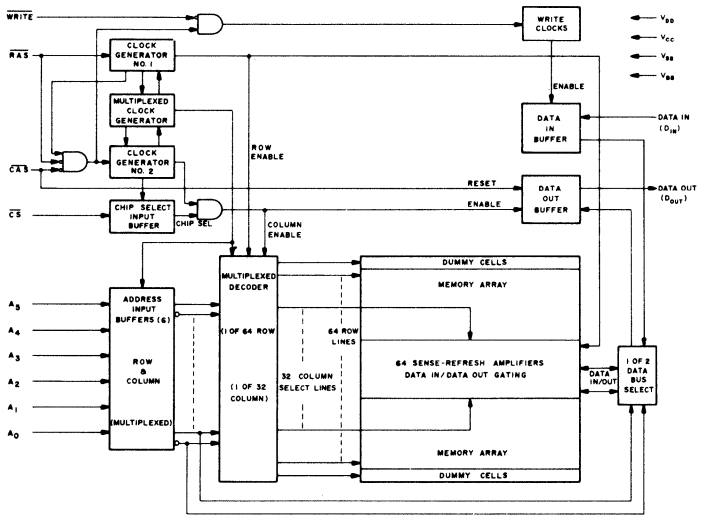
DESCRIPTION

The MK 4027 is a 4096 word by 1 bit MOS random access memory circuit fabricated with MOSTEK's N-channel silicon gate process. This process allows the MK 4027 to be a high performance state-of-the-art memory circuit that is manufacturable in high volume. The MK 4027 employs a single transistor storage cell utilizing a dynamic storage technique and dynamic control circuitry to achieve optimum performance with low power dissipation.

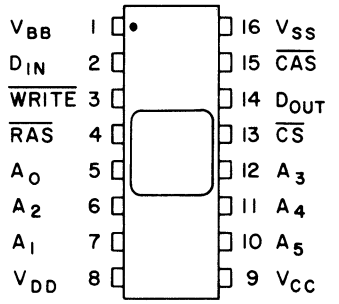
A unique multiplexing and latching technique for the address inputs permits the MK 4027 to be packaged in a standard 16-pin DIP on 0.3 in. centers. This package size provides high system-bit densities and is compatible with widely available automated testing and insertion equipment.

System oriented features include direct interfacing capability with TTL, only 6 very low capacitance address lines to drive, on-chip address and data registers which eliminates the need for interface registers, input logic levels selected to optimize noise immunity, and two chip select methods to allow the user to determine the appropriate speed/power characteristics of his memory system. The MK 4027 also incorporates several flexible operating modes. In addition to the usual read and write cycles, read-modify write, page-mode, and $\overline{RAS}$-only refresh cycles are available with the MK 4027. Page-mode timing is very useful in systems requiring Direct Memory Access (DMA) operation.

FUNCTIONAL DIAGRAM



PIN CONNECTIONS



PIN NAMES

A_0-A_5	ADDRESS INPUTS
$\overline{CAS}$	COLUMN ADDRESS STROBE
$\overline{CS}$	CHIP SELECT
D_{IN}	DATA IN
D_{OUT}	DATA OUT
$\overline{RAS}$	ROW ADDRESS STROBE
$\overline{WRITE}$	READ/WRITE INPUT
V_{BB}	POWER (−5V)
V_{CC}	POWER (+5V)
V_{DD}	POWER (+ 12V)
V_{SS}	GROUND

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to V_{BB} ..... −0.5V to +20V
Voltage on V_{DD}, V_{CC} relative to V_{SS} ..... −1.0V to +15V
$V_{BB}-V_{SS}$ ($V_{DD}-V_{SS} > 0$) 0V
Operating temperature, T_A (Ambient) ..... 0°C to + 70°C
Storage temperature (Ambient)(Ceramic) ..... −65°C to + 150°C
Storage temperature (Ambient)(Plastic) ..... −55°C to + 125°C
Short Circuit Output Current 50mA
Power dissipation ..... 1 Watt

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS [4]

($0°C \leq T_A \leq 70°C$) [1]

	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{DD}	Supply Voltage	10.8	12.0	13.2	volts	2
V_{CC}	Supply Voltage	4.5V	5.0	5.5	volts	2,3
V_{SS}	Supply Voltage	0	0	0	volts	2
V_{BB}	Supply Voltage	−4.5	−5.0	−5.7	volts	2
V_{IHC}	Logic 1 Voltage, $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	2.4		7.0	volts	2
V_{IH}	Logic 1 Voltage, all inputs except $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	2.2		7.0	volts	2
V_{IL}	Logic 0 Voltage, all inputs	−1.0		.8	volts	2

DC ELECTRICAL CHARACTERISTICS [4]

($0°C \leq T_A \leq 70°C$)[1] (V_{DD} = 12.0V ± 10%; V_{CC} = 5.0V ± 10%; V_{SS} = 0V; $-5.7V \leq V_{BB} \leq -4.5V$)

	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
I_{DD1}	Average V_{DD} Power Supply Current			35	mA	5
I_{DD2}	Standby V_{DD} Power Supply Current			2	mA	8
I_{DD3}	Average V_{DD} Power Supply Current during "$\overline{RAS}$ only" cycles			25	mA	
I_{CC}	V_{CC} Power Supply Current				mA	6
I_{BB}	Average V_{BB} Power Supply Current			150	μA	
$I_{I(L)}$	Input Leakage Current (any input)			10	μA	7
$I_{O(L)}$	Output Leakage Current			10	μA	8,9
V_{OH}	Output Logic 1 Voltage @ I_{OUT} = −5mA	2.4			volts	
V_{OL}	Output Logic 0 Voltage @ I_{OUT} = 3.2mA			0.4	volts	

NOTES

1. T_A is specified for operation at frequencies to $t_{RC} \geq t_{RC}$ (min).
2. All voltages referenced to V_{SS}.
3. Output voltage will swing from V_{SS} to V_{CC} when enabled, with no output load. For purposes of maintaining data in standby mode, V_{CC} may be reduced to V_{SS} without affecting refresh operations or data retention. However, the V_{OH} (min) specification is not guaranteed in this mode.
4. Several cycles are required after power-up before proper device operation is achieved. Any 8 cycles which perform refresh are adequate for this purpose.
5. Current is proportional to cycle rate, I_{DD1} (max) is measured at the cycle rate specified by t_{RC} (min). See figure 1 for I_{DD1} limits at other cycle rates.
6. I_{CC} depends on output loading. During readout of high level data V_{CC} is connected through a low impedance (135Ω typ) to Data Out. At all other times I_{CC} consists of leakage currents only.
7. All device pins at 0 volts except V_{BB} which is at −5 volts and the pin under test which is at +10 volts.
8. Output is disabled (high-impedance) and $\overline{RAS}$ and $\overline{CAS}$ are both at a logic 1. Transient stabilization is required prior to measurement of this parameter.
9. $0V \leq V_{OUT} \leq +10V$.
10. Effective capacitance is calculated from the equation:

$$C = \frac{\Delta Q}{\Delta V} \text{ with } \Delta V = 3 \text{ volts.}$$

11. A.C. measurements assume t_T = 5ns.
12. The specifications for tRC (min) and tRWC (min) are used only to indicate cycle time at which proper operation over the full temperature range ($0° \leq TA \leq 70°C$) is assured.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS(4, 11, 17)

($0°C \leq T_A \leq 70°C$)[1] (V_{DD} = 12.0V ± 10%, V_{CC} = 5.0V ± 10%, V_{SS} = 0V, $-5.7V \leq V_{BB} \leq -4.5V$)

	PARAMETER	MK4027-4 MIN	MK4027-4 MAX	UNITS	NOTES
t_{RC}	Random read or write cycle time	380		ns	12
t_{RWC}	Read write cycle time	395		ns	12
t_{RMW}	Read modify write cycle time	470		ns	12
t_{PC}	Page mode cycle time	285		ns	12
t_{RAC}	Access time from row address strobe		250	ns	13,15
t_{CAC}	Access time from column address strobe		165	ns	14,15
t_{OFF}	Output buffer turn-off delay	0	60	ns	
t_{RP}	Row address strobe precharge time	120		ns	
t_{RAS}	Row address strobe pulse width	250	10,000	ns	
t_{RSH}	Row address strobe hold time	165		ns	
t_{CAS}	Column address strobe pulse width	165		ns	
t_{CSH}	Column address strobe hold time	250		ns	
t_{RCD}	Row to column strobe delay	35	85	ns	16
t_{ASR}	Row address set-up time	0		ns	
t_{RAH}	Row address hold time	35		ns	
t_{ASC}	Column address set-up time	-10		ns	
t_{CAH}	Column address hold time	75		ns	
t_{AR}	Column address hold time referenced to $\overline{RAS}$	160		ns	
t_{CSC}	Chip select set-up time	-10		ns	
t_{CH}	Chip select hold time	75		ns	
t_{CHR}	Chip select hold time referenced to $\overline{RAS}$	160		ns	
t_T	Transition time (rise and fall)	3	50	ns	17
t_{RCS}	Read command set-up time	0		ns	
t_{RCH}	Read command hold time	0		ns	
t_{WCH}	Write command hold time	75		ns	
t_{WCR}	Write command hold time referenced to $\overline{RAS}$	160		ns	
t_{WP}	Write command pulse width	75		ns	
t_{RWL}	Write command to row strobe lead time	85		ns	
t_{CWL}	Write command to column strobe lead time	85		ns	
t_{DS}	Data in set-up time	0		ns	18
t_{DH}	Data in hold time	75		ns	18
t_{DHR}	Data in hold time referenced to $\overline{RAS}$	160		ns	
t_{CRP}	Column to row strobe precharge time	0		ns	
t_{CP}	Column precharge time	110		ns	
t_{RFSH}	Refresh period		2	ms	
t_{WCS}	Write command set-up time	0		ns	19
t_{CWD}	$\overline{CAS}$ to $\overline{WRITE}$ delay	90		ns	19
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ delay	175		ns	19
t_{DOH}	Date out hold time	10		μs	

Notes Continued

13. Assumes that $t_{RCD} \leq t_{RCD}$ (ma.).

14. Assumes that $t_{RCD} \geq t_{RCD}$ (max).

15. Measured with a load circuit equivalent to 2 TTL loads and 100pF

16. Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.

17. V_{IHC} (min) or V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IHC} or V_{IH} and V_{IL}.

18. These parameters are referenced to $\overline{CAS}$ leading edge in random write cycles and to $\overline{WRITE}$ leading edge in delayed write or read-modify-write cycles.

19. t_{WCS}, t_{CWD}, and t_{RWD} are restrictive operating parameters in a read/write or read/modify/write cycle only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and Data Out will contain the data written into the selected cell. If $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min), the cycle is a read-write cycle and Data Out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of Data Out (at access time) is indeterminate.

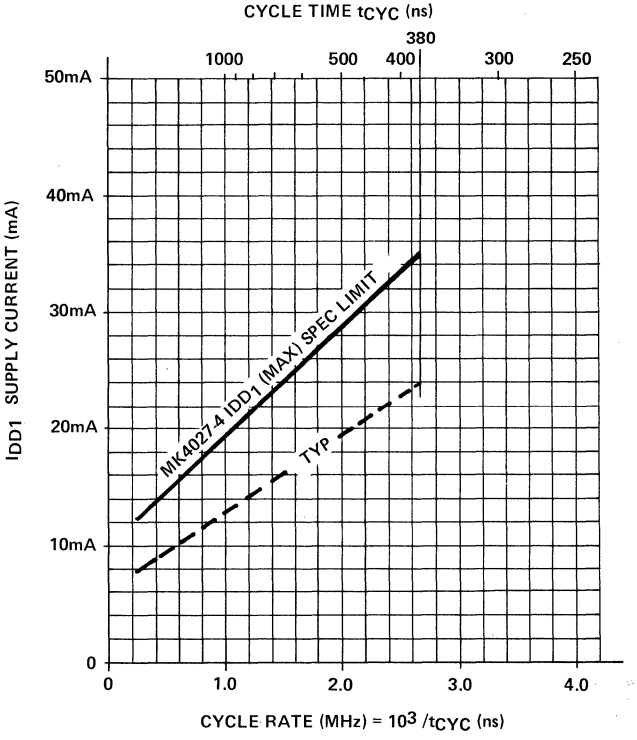
AC ELECTRICAL CHARACTERISTICS

(0°C ≤ T_A ≤ 70°C) (V_{DD} = 12.0V ± 10%; V_{SS} = 0V; −5.7V ≤ V_{BB} ≤ −4.5V)

	PARAMETER	TYP	MAX	UNITS	NOTES
C_{I1}	Input Capacitance (A_0-A_5), D_{IN}, $\overline{CS}$	4	5	pF	10
C_{I2}	Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	8	10	pF	10
C_O	Output Capacitance (D_{OUT})	5	7	pF	8,10

MAXIMUM I_{DD1} vs. CYCLE RATE FOR DEVICE OPERATION AT EXTENDED FREQUENCIES

Figure 1



SUPPLEMENT - To be used in conjunction with MK4027(J/N)-1/2/3 data sheet.

MOSTEK®

16,384 X 1-BIT DYNAMIC RAM

MK4116(J/N/E)-2/3

IV

FEATURES

- ☐ Recognized industry standard 16-pin configuration from MOSTEK
- ☐ 150ns access time, 320ns cycle (MK 4116-2) 200ns access time, 375ns cycle (MK 4116-3)
- ☐ ± 10% tolerance on all power supplies (+12V, ±5V)
- ☐ Low power: 462mW active, 20mW standby (max)
- ☐ Output data controlled by $\overline{CAS}$ and unlatched at end of cycle to allow two dimensional chip selection and extended page boundary
- ☐ Common I/O capability using "early write" operation
- ☐ Read-Modify-Write, $\overline{RAS}$-only refresh, and Page-mode capability
- ☐ All inputs TTL compatible,low capacitance, and protected against static charge
- ☐ 128 refresh cycles
- ☐ ECL compatible on VBB power supply (-5.7V)
- ☐ MKB version screened to MIL-STD-883
- ☐ JAN version available to MIL-M-38510/240

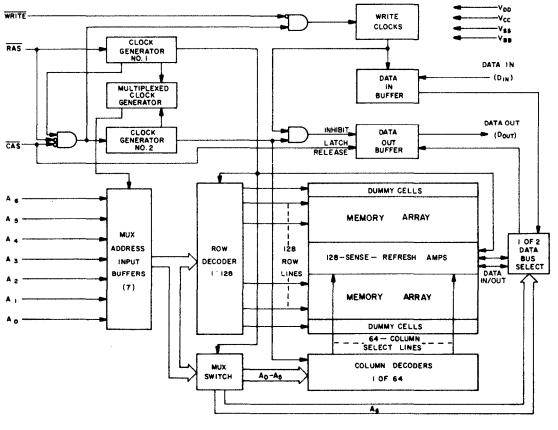
DESCRIPTION

The MK 4116 is a new generation MOS dynamic random access memory circuit organized as 16,384 words by 1 bit. As a state-of-the-art MOS memory device, the MK 4116 (16K RAM) incorporates advanced circuit techniques designed to provide wide operating margins, both internally and to the system user, while achieving performance levels in speed and power previously seen only in MOSTEK's high performance MK 4027 (4K RAM).

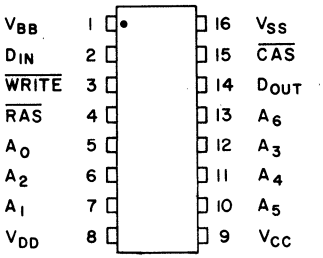
The technology used to fabricate the MK 4116 is MOSTEK's double-poly, N-channel silicon gate, POLY II™ process. This process, coupled with the use of a single transistor dynamic storage cell, provides the maximum possible circuit density and reliability, while maintaining high performance capability. The use of dynamic circuitry throughout, including sense amplifiers, assures that power dissipation is minimized without any sacrifice in speed or operating margin. These factors combine to make the MK 4116 a truly superior RAM product.

Multiplexed address inputs (a feature pioneered by MOSTEK for its 4K RAMS) permits the MK 4116 to be packaged in a standard 16-pin DIP. This recognized industry standard package configuration, while compatible with widely available automated testing and insertion equipment, provides highest possible system bit densities and simplifies system upgrade from 4K to 16K RAMs for new generation applications. Non-critical clock timing requirements allow use of the multiplexing technique while maintaining high performance.

FUNCTIONAL DIAGRAM



PIN CONNECTIONS



PIN NAMES

A_0-A_6	ADDRESS INPUTS	$\overline{WRITE}$	READ/WRITE INPUT
$\overline{CAS}$	COLUMN ADDRESS STROBE	V_{BB}	POWER (−5V)
		V_{CC}	POWER (+5V)
D_{IN}	DATA IN	V_{DD}	POWER (+12V)
D_{OUT}	DATA OUT	V_{SS}	GROUND
$\overline{RAS}$	ROW ADDRESS STROBE		

Available per MIL-STD-883 B. Mostek is qualified per JM-38150 Class B.

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to V_{BB} ..... −0.5V to +20V
Voltage on V_{DD}, V_{CC} supplies relative to V_{SS} ..... −1.0V to +15.0V
V_{BB}−V_{SS} (V_{DD}−V_{SS}>0V) 0V
Operating temperature, T_A (Ambient) ..... 0°C to + 70°C
Storage temperature (Ambient) Ceramic ..... −55°C to + 150°C
Storage temperature, (Ambient) Plastic ..... −55°C to +125°C
Short circuit output current 50mA
Power dissipation ..... 1 Watt

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS[6]

($0°C \leq T_A \leq 70°C$)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{DD} V_{CC} V_{SS} V_{BB}	10.8 4.5 0 −4.5	12.0 5.0 0 −5.0	13.2 5.5 0 −5.7	Volts Volts Volts Volts	2 2,3 2 2
Input High (Logic 1) Voltage, $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	V_{IHC}	2.4	–	7.0	Volts	2
Input High (Logic 1) Voltage, all inputs except $\overline{RAS}$, $\overline{CAS}$ $\overline{WRITE}$	V_{IH}	2.2	–	7.0	Volts	2
Input Low (Logic 0) Voltage, all inputs	V_{IL}	−1.0	–	.8	Volts	2

DC ELECTRICAL CHARACTERISTICS

($0°C \leq T_A \leq 70°C$) (V_{DD} = 12.0V ± 10%; V_{CC} = 5.0V ±10%; −5.7V ≤ V_{BB} ≤ −4.5V; V_{SS} = 0V)

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
OPERATING CURRENT Average power supply operating current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = t_{RC} Min	I_{DD1} I_{CC1} I_{BB1}		35 200	mA µA	4 5
STANDBY CURRENT Power supply standby current ($\overline{RAS}$ = V_{IHC}, D_{OUT} = High Impedance)	I_{DD2} I_{CC2} I_{BB2}	 −10 	1.5 10 100	mA µA µA	
REFRESH CURRENT Average power supply current, refresh mode ($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IHC}; t_{RC} = t_{RC} Min	I_{DD3} I_{CC3} I_{BB3}	 −10 	25 10 200	mA µA µA	4
PAGE MODE CURRENT Average power supply current, page-mode operation ($\overline{RAS}$ =V_{IL}, $\overline{CAS}$ cycling; t_{PC} = t_{PC} Min	I_{DD4} I_{CC4} I_{BB4}		27 200	mA µA	4 5
INPUT LEAKAGE Input leakage current, any input (V_{BB} = −5V, 0V ≤ V_{IN} ≤ +7.0V, all other pins not under test = 0 volts)	$I_{I(L)}$	−10	10	µA	
OUTPUT LEAKAGE Output leakage current (D_{OUT} is disabled, 0V ≤ V_{OUT} ≤ +5.5V)	$I_{O(L)}$	−10	10	µA	
OUTPUT LEVELS Output high (Logic 1) voltage (I_{OUT} = −5mA) Output low (Logic 0) voltage (I_{OUT} = 4.2 mA)	V_{OH} V_{OL}	2.4 	 0.4	Volts Volts	3

NOTES:

1. T_A is specified here for operation at frequencies to $t_{RC} \geq t_{RC}$ (min). Operation at higher cycle rates with reduced ambient temperatures and higher power dissipation is permissible, however, provided AC operating parameters are met. See figure 1 for derating curve.
2. All voltages referenced to V_{SS}.
3. Output voltage will swing from V_{SS} to V_{CC} when activated with no current loading. For purposes of maintaining data in standby mode, V_{CC} may be reduced to V_{SS} without affecting refresh operations or data retention. However, the V_{OH} (min) specification is not guaranteed in this mode.
4. I_{DD1}, I_{DD3}, and I_{DD4} depend on cycle rate. See figures 2,3, and 4 for I_{DD} limits at other cycle rates.
5. I_{CC1} and I_{CC4} depend upon output loading. During readout of high level data V_{CC} is connected through a low impedance (135Ω typ) to data out. At all other times I_{CC} consists of leakage currents only.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (6,7,8)

($0°C \leq T_A \leq 70°C$)[1] (V_{DD} = 12.0V ± 10%; V_{CC} = 5.0V ±10%, V_{SS} = 0V, V_{BB} = -5.7V ≤ VBB ≤ -4.5V)

PARAMETER	SYMBOL	MK 4116-2		MK 4116-3		UNITS	NOTES
		MIN	MAX	MIN	MAX		
Random read or write cycle time	t_{RC}	320		375		ns	9
Read-write cycle time	t_{RWC}	320		375		ns	9
Read modify write cycle time	t_{RMW}	320		405		ns	9
Page mode cycle time	t_{PC}	170		225		ns	9
Access time from $\overline{RAS}$	t_{RAC}		150		200	ns	10,12
Access time from $\overline{CAS}$	t_{CAC}		100		135	ns	11,12
Output buffer turn-off delay	t_{OFF}	0	40	0	50	ns	13
Transition time (rise and fall)	t_T	3	35	3	50	ns	8
$\overline{RAS}$ precharge time	t_{RP}	100		120		ns	
$\overline{RAS}$ pulse width	t_{RAS}	150	10,000	200	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	100		135		ns	
$\overline{CAS}$ hold time	tCSH	150		200		ns	
$\overline{CAS}$ pulse width	t_{CAS}	100	10,000	135	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	50	25	65	ns	14
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	−20		−20		ns	
Row Address set-up time	t_{ASR}	0		0		ns	
Row Address hold time	t_{RAH}	20		25		ns	
Column Address set-up time	t_{ASC}	−10		−10		ns	
Column Address hold time	t_{CAH}	45		55		ns	
Column Address hold time referenced to $\overline{RAS}$	t_{AR}	95		120		ns	
Read command set-up time	t_{RCS}	0		0		ns	
Read command hold time	t_{RCH}	0		0		ns	
Write command hold time	t_{WCH}	45		55		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	95		120		ns	
Write command pulse width	t_{WP}	45		55		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	50		70		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	50		70		ns	
Data-in set-up time	t_{DS}	0		0		ns	15
Data-in hold time	t_{DH}	45		55		ns	15
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	95		120		ns	
$\overline{CAS}$ precharge time (for page-mode cycle only)	t_{CP}	60		80		ns	
Refresh period	t_{REF}		2		2	ms	
$\overline{WRITE}$ command set-up time	t_{WCS}	-20		-20		ns	16
$\overline{CAS}$ to $\overline{WRITE}$ delay	t_{CWD}	60		80		ns	16
$\overline{RAS}$ to $\overline{WRITE}$ delay	t_{RWD}	110		145		ns	16

NOTES (Continued)

6. Several cycles are required after power-up before proper device operation is achieved. Any 8 cycles which perform refresh are adequate for this purpose.
7. AC measurements assume tT = 5ns.
8. VIHC (min) or VIH (min) and VIL (max) are reference levels for measuring timing of input signals. Also transition times are measured between VIHC or VIH and VIL.
9. The specifications for tRC (min) tRMW (min) and tRWC (min) are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \leq TA \leq 70°C$) is assured
10. Assumes that $tRCD \leq tRCD$ (Max). If tRCD is greater than the maximum recommended value shown in this table, tRAC will increase by the amount that tRCD exceeds the value shown.
11. Assumes that tRCD (max).
12. Measured with a load equivalent to 2 TTL loads and 100pF.
13. tOFF (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
14. Operation within the tRCD (max) limit insures that tRAC (max) can be met. tRCD (max) is specified as a reference point only if tRCD is greater than the specified tRCD (max) limit, then access time is controlled exclusively by tCAC.
15. These parameters are referenced to CAS leading edge in early write cycles and to WRITE leading edge in delayed write or read-modify-write cycles.
16. tWCS, tCWD and tRWD are restrictive operating parameters in read write and read modify write cycles only. If $tWCS \geq tWCS$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; If $tCWD \geq tCWD$ (min) and $tRWD \geq tRWD$ (min), the cycle is a read-write cycle and the data out will contain data read from the selected cell; If neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.
17. Effective capacitance calculated from the equation $C = 1\frac{\Delta t}{\Delta V}$ with ΔV = 3 volts and power supplies at nominal levels.
18. $\overline{CAS}$ = VIHC to disable DOUT.

AC ELECTRICAL CHARACTERISTICS

(0°C ≤ T_A ≤ 70°C) (V_{DD} = 12.0V ± 10%; V_{SS} = 0V; V_{BB} = **-5.7V ≤ VBB ≤ -4.5V**)

PARAMETER	SYMBOL	TYP	MAX	UNITS	NOTES
Input Capacitance (A_0–A_6), D_{IN}	C_{I1}	4	5	pF	17
Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	C_{I2}	8	10	pF	17
Output Capacitance (D_{OUT})	C_O	5	7	pF	17,18

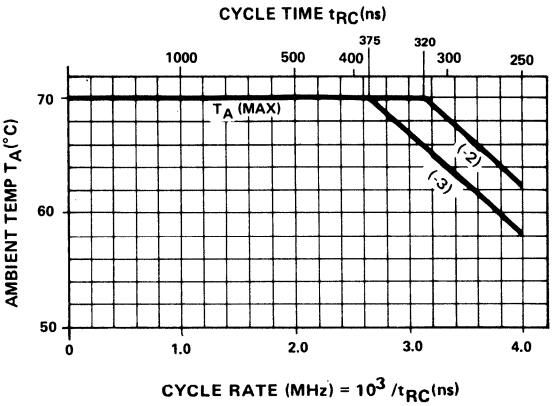


Fig. 1 Maximum ambient temperature versus cycle rate for extended frequency operation. T_A (max) for operation at cycling rates greater than 2.66 MHz (t_{CYC} < 375ns) is determined by T_A (max)° C = 70– 9.0 x (cycle rate MHz –2.66) for -3. T_A (max) °C = 70 – 9.0 x cycle rate MHz –3.125MHz) for -2 only.

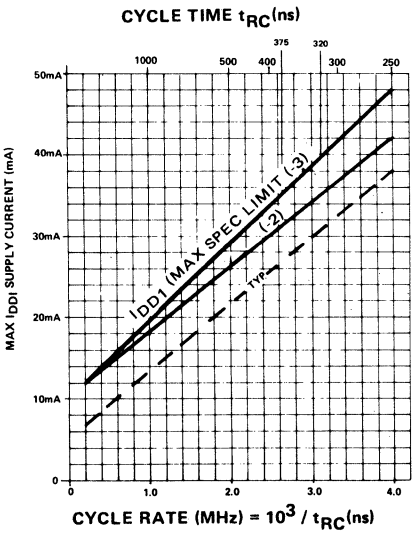


Fig. 2 Maximum I_{DD1} versus cycle rate for device operation at extended frequencies. I_{DD1} (max) curve is defined by the equation:

I_{DD1} (max) mA = 10 + 9.4 x cycle rate [MHz] for -3
I_{DD1} (max) mA = 10 + 8.0 x cycle rate [MHz] for -2

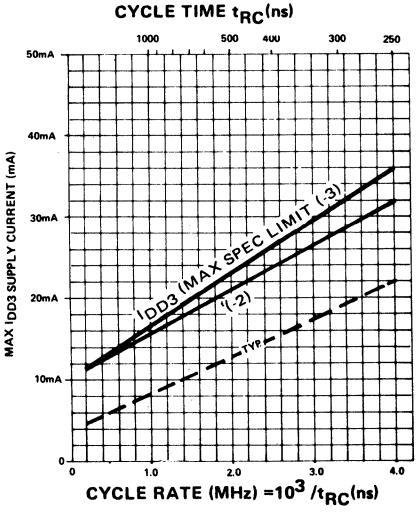


Fig. 3 Maximum I_{DD3} versus cycle rate for device operation at extended frequencies. I_{DD3} (max) curve is defined by the equation:

I_{DD3}(max) mA = 10 + 6.5 x cycle rate [MHz] for -3
I_{DD3}(max) mA = 10 + 5.5 x cycle rate [MHz] for -2

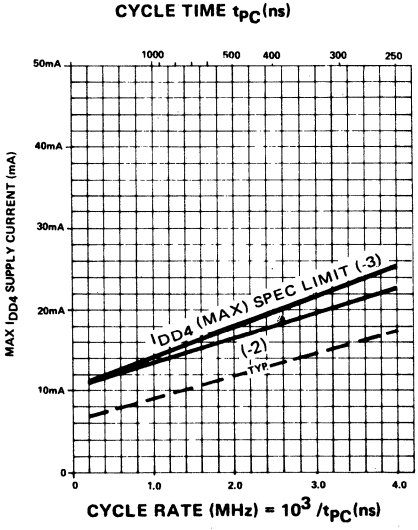
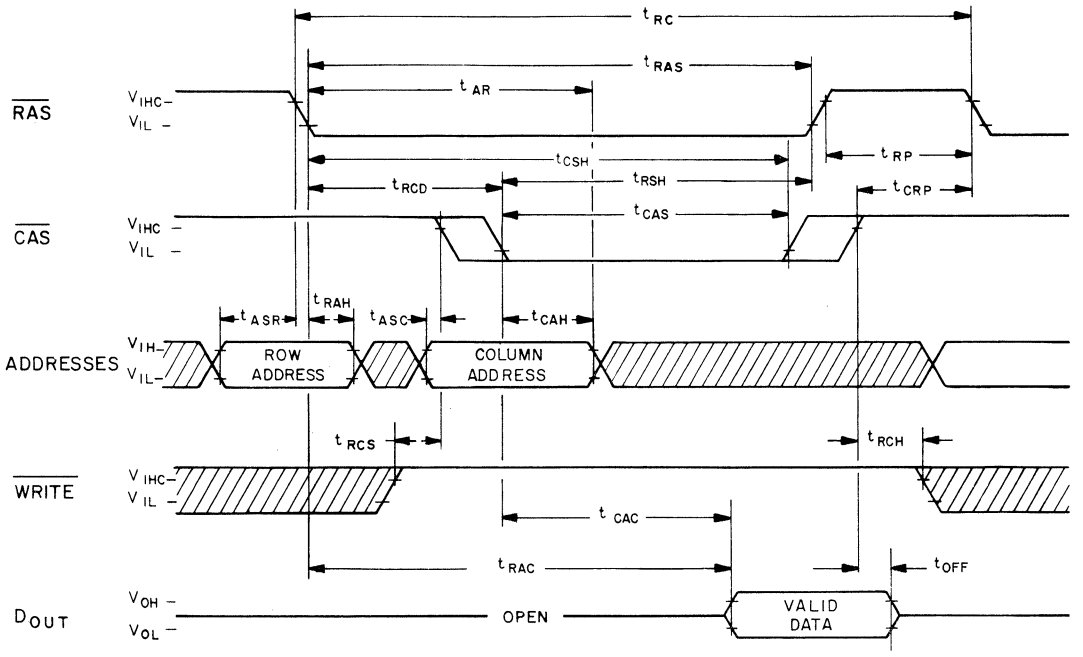


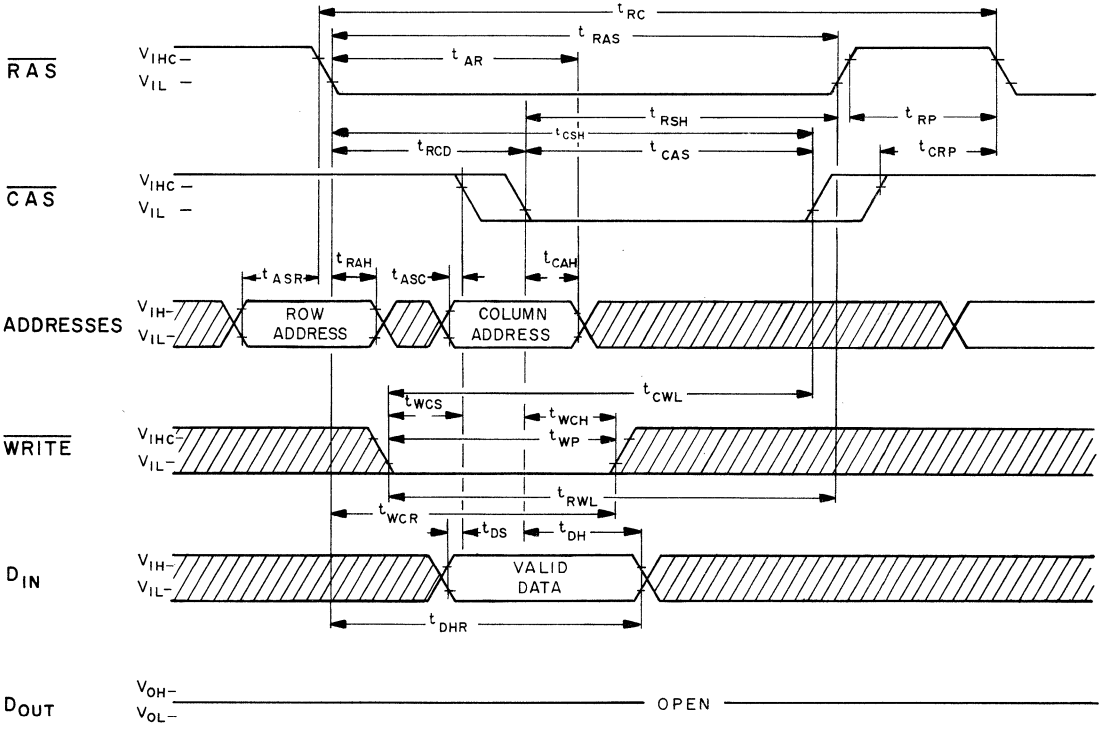
Fig. 4 Maximum I_{DD4} versus cycle rate for device operation in page mode. I_{DD4} (max) curve is defined by the equation:

I_{DD4} (max) mA = 10 + 3.75 x cycle rate [MHz] for -3
I_{DD4} (max) mA = 10 + 3.2 x cycle rate [MHz] for -2

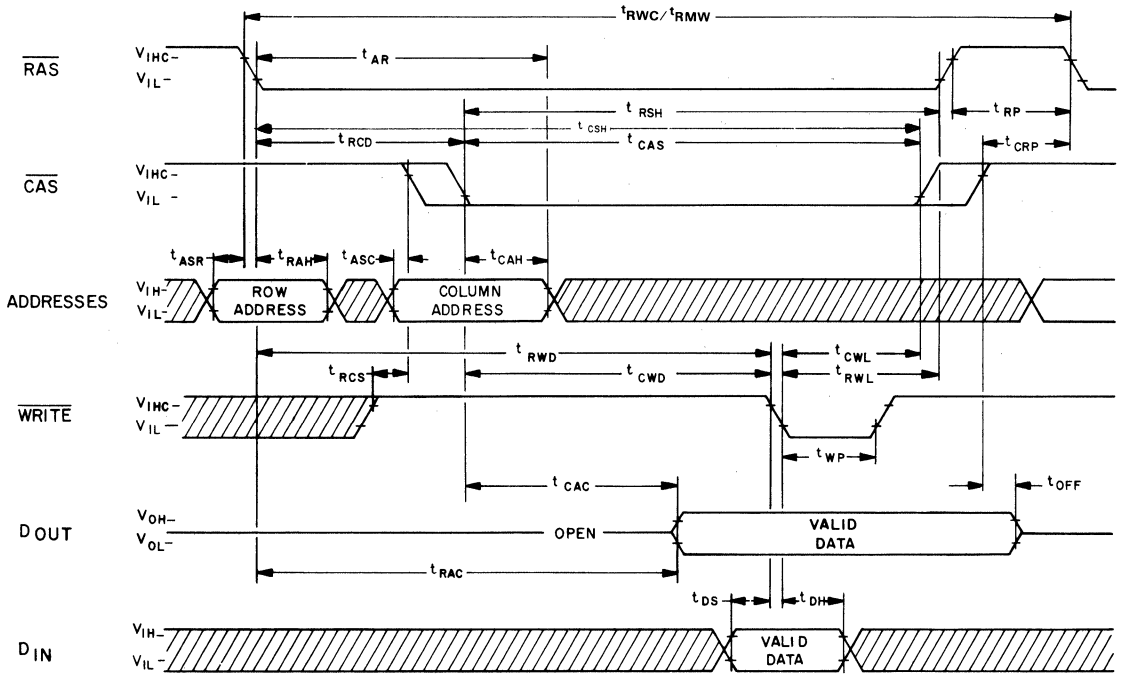
READ CYCLE



WRITE CYCLE (EARLY WRITE)

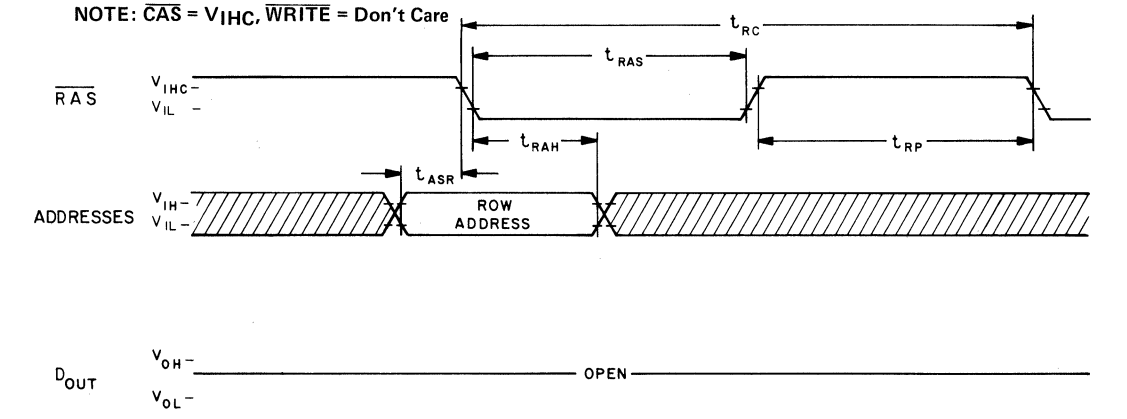


READ–WRITE/READ–MODIFY–WRITE CYCLE

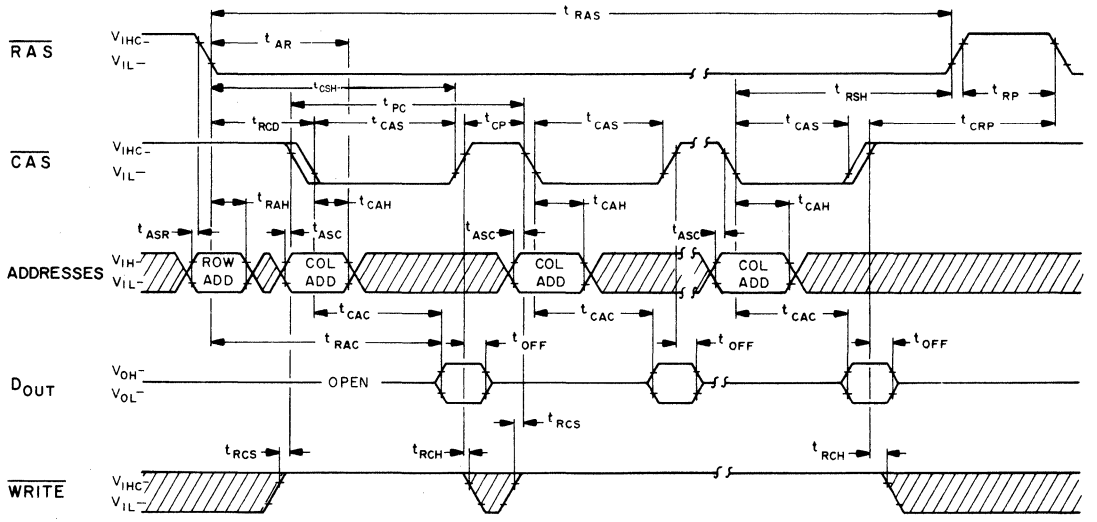


"RAS–ONLY" REFRESH CYCLE

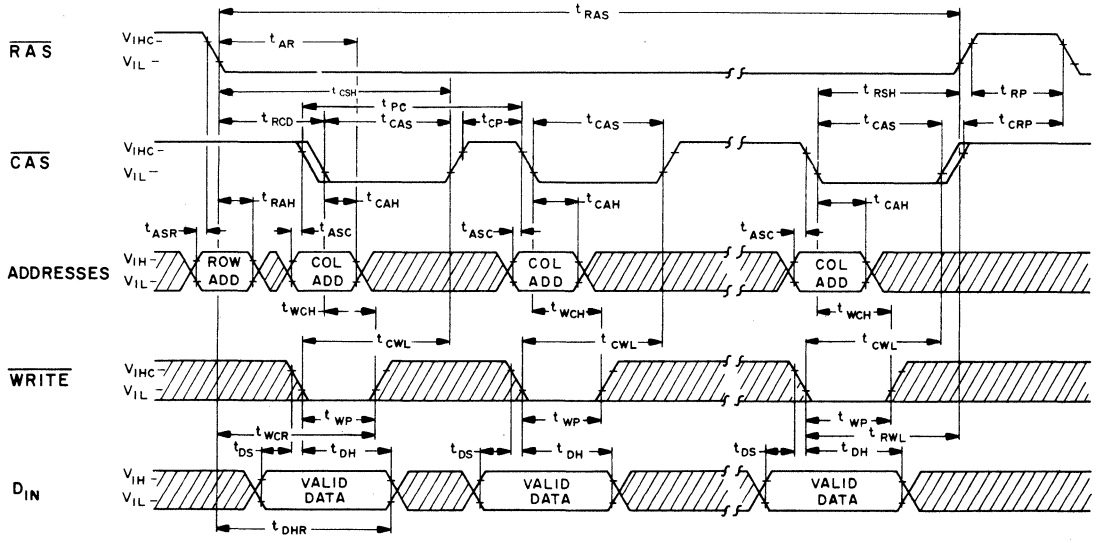
NOTE: CAS = V_{IHC}, WRITE = Don't Care



PAGE MODE READ CYCLE



PAGE MODE WRITE CYCLE



IV

DESCRIPTION (continued)

System oriented features include ± 10% tolerance on all power supplies, direct interfacing capability with high performance logic families such as Schottky TTL, maximum input noise immunity to minimize "false triggering" of the inputs (a common cause of soft errors), on-chip address and data registers which eliminate the need for interface registers, and two chip select methods to allow the user to determine the appropriate speed/power characteristics of his memory system. The MK 4116 also incorporates several flexible timing/operating modes. In addition to the usual read, write, and read-modify-write cycles, the MK 4116 is capable of delayed write cycles, page-mode operation and $\overline{RAS}$-only refresh. Proper control of the clock inputs($\overline{RAS}$, $\overline{CAS}$ and $\overline{WRITE}$) allows common I/O capability, two dimensional chip selection, and extended page boundaries (when operating in page mode).

ADDRESSING

The 14 address bits required to decode 1 of the 16,384 cell locations within the MK 4116 are multiplexed onto the 7 address inputs and latched into the on-chip address latches by externally applying two negative going TTL-level clocks. The first clock, the Row Address Strobe ($\overline{RAS}$), latches the 7 row address bits into the chip. The second clock, the Column Address Strobe ($\overline{CAS}$), subsequently latches the 7 column address bits into the chip. Each of these signals, $\overline{RAS}$ and $\overline{CAS}$, triggers a sequence of events which are controlled by different delayed internal clocks. The two clock chains are linked together logically in such a way that the address multiplexing operation is done outside of the critical path timing sequence for read data access. The later events in the $\overline{CAS}$ clock sequence are inhibited until the occurence of a delayed signal derived from the $\overline{RAS}$ clock chain. This "gated $\overline{CAS}$" feature allows the $\overline{CAS}$ clock to be externally activated as soon as the Row Address Hold Time specification (t_{RAH}) has been satisfied and the address inputs have been changed from Row address to Column address information.

Note that $\overline{CAS}$ can be activated at any time after t_{RAH} and it will have no effect on the worst case data access time (t_{RAC}) up to the point in time when the delayed row clock no longer inhibits the remaining sequence of column clocks. Two timing endpoints result from the internal gating of $\overline{CAS}$ which are called t_{RCD} (min) and t_{RCD} (max). No data storage or reading errors will result if $\overline{CAS}$ is applied to the MK 4116 at a point in time beyond the t_{RCD} (max) limit. However, access time will then be determined exclusively by the access time from $\overline{CAS}$ (t_{CAC}) rather than from $\overline{RAS}$ (t_{RAC}), and access time from $\overline{RAS}$ will be lengthened by the amount that t_{RCD} exceeds the t_{RCD} (max) limit.

DATA INPUT/OUTPUT

Data to be written into a selected cell is latched into an on-chip register by a combination of $\overline{WRITE}$ and $\overline{CAS}$ while $\overline{RAS}$ is active. The later of the signals ($\overline{WRITE}$ or $\overline{CAS}$) to make its negative transition is the strobe for the Data In (D_{IN}) register. This permits several options in the write cycle timing. In a write cycle, if the $\overline{WRITE}$ input is brought low (active) prior to $\overline{CAS}$, the D_{IN} is strobed by $\overline{CAS}$, and the set-up and hold times are referenced to $\overline{CAS}$. If the input data is not available at $\overline{CAS}$ time or if it is desired that the cycle be a read-write cycle, the $\overline{WRITE}$ signal will be delayed until after $\overline{CAS}$ has made its negative transition. In this "delayed write cycle" the data input set-up and hold times are referenced to the negative edge of $\overline{WRITE}$ rather than $\overline{CAS}$. (To illustrate this feature, D_{IN} is referenced to $\overline{WRITE}$ in the timing diagrams depicting the read-write and page-mode write cycles while the "early write" cycle diagram shows D_{IN} referenced to $\overline{CAS}$).

Data is retrieved from the memory in a read cycle by maintaining $\overline{WRITE}$ in the inactive or high state throughout the portion of the memory cycle in which $\overline{CAS}$ is active (low). Data read from the selected cell will be available at the output within the specified access time.

DATA OUTPUT CONTROL

The normal condition of the Data Output (D_{OUT}) of the MK 4116 is the high impedance (open-circuit) state. That is to say, anytime $\overline{CAS}$ is at a high level, the D_{OUT} pin will be floating. The only time the output will turn on and contain either a logic 0 or logic 1 is at access time during a read cycle. D_{OUT} will remain valid from access time until $\overline{CAS}$ is taken back to the inactive (high level) condition.

If the memory cycle in progress is a read, read-modify write, or a delayed write cycle, then the data output will go from the high impedance state to the active condition, and at access time will contain the data read from the selected cell. This output data is the same polarity (not inverted) as the input data. Once having gone active, the output will remain valid until $\overline{CAS}$ is taken to the precharge (logic 1) state, whether or not $\overline{RAS}$ goes into precharge.

If the cycle in progress is an "early-write" cycle ($\overline{WRITE}$ active before $\overline{CAS}$ goes active), then the output pin will maintain the high impedance state throughout the entire cycle. Note that with this type of output configuration, the user is given full control of the D_{OUT} pin simply by controlling the placement of $\overline{WRITE}$ command during a write cycle, and the pulse width of the Column Address Strobe during read operations. Note also that even though data is not latched at the output, data can remain valid from access time until the beginning of a subsequent cycle without paying any penalty in overall memory cycle time (stretching the cycle).

This type of output operation results in some very significant system implications.

Common I/O Operation – If all write operations are handled in the "early write" mode, then D_{IN} can be connected directly to D_{OUT} for a common I/O data bus.

Data Output Control – D_{OUT} will remain valid during a read cycle from t_{CAC} until $\overline{CAS}$ goes back to a high level (precharge), allowing data to be valid from one cycle up until a new memory cycle begins with no penalty in cycle time. This also makes the $\overline{RAS}/\overline{CAS}$ clock timing relationship very flexible.

Two Methods of Chip Selection – Since D_{OUT}

is not latched, $\overline{CAS}$ is not required to turn off the outputs of unselected memory devices in a matrix. This means that both $\overline{CAS}$ and/or $\overline{RAS}$ can be decoded for chip selection. If both $\overline{RAS}$ and $\overline{CAS}$ are decoded, then a two dimensional (X,Y) chip select array can be realized.

Extended Page Boundary – Page-mode operation allows for successive memory cycles at multiple column locations of the same row address. By decoding $\overline{CAS}$ as a page cycle select signal, the page boundary can be extended beyond the 128 column locations in a single chip. (See page-mode operation).

OUTPUT INTERFACE CHARACTERISTICS

The three state data output buffer presents the data output pin with a low impedance to V_{CC} for a logic 1 and a low impedance to V_{SS} for a logic 0. The effective resistance to V_{CC} (logic 1 state) is 420 Ω maximum and 135Ω typically. The resistance to V_{SS} (logic 0 state) is 95 Ω maximum and 35 Ω typically. The separate V_{CC} pin allows the output buffer to be powered from the supply voltage of the logic to which the chip is interfaced. During battery standby operation, the V_{CC} pin may have power removed without affecting the MK 4116 refresh operation. This allows all system logic except the $\overline{RAS}$ timing circuitry and the refresh address logic to be turned off during battery standby to conserve power.

PAGE MODE OPERATION

The "Page Mode" feature of the MK 4116 allows for successive memory operations at multiple column locations of the same row address with increased speed without an increase in power. This is done by strobing the row address into the chip and maintaining the $\overline{RAS}$ signal at a logic 0 throughout all successive memory cycles in which the row address is common. This "page-mode" of operation will not dissipate the power associated with the negative going edge of $\overline{RAS}$. Also, the time required for strobing in a new row address is eliminated, thereby decreasing the access and cycle times.

The page boundary of a single MK 4116 is limited to the 128 column locations determined by all combinations of the 7 column address bits. However, in system applications which utilize more than 16,384 data words, (more than one 16K memory block), the page boundary can be extended by using $\overline{CAS}$ rather than $\overline{RAS}$ as the chip select signal. $\overline{RAS}$ is applied to all devices to latch the row address into each device and then $\overline{CAS}$ is decoded and serves as a page cycle select signal. Only those devices which receive both $\overline{RAS}$ and $\overline{CAS}$ signals will execute a read or write cycle.

REFRESH

Refresh of the dynamic cell matrix is accomplished by performing a memory cycle at each of the 128 row addresses within each 2 millisecond time interval. Although any normal memory cycle will perform the refresh operation, this function is most easily accomplished with "$\overline{RAS}$-only" cycles. $\overline{RAS}$-only refresh results in a substantial reduction in operating power. This reduction in power is reflected in the I_{DD3} specification.

POWER CONSIDERATIONS

Most of the circuitry used in the MK 4116 is dynamic and most of the power drawn is the result of an address strobe edge. Consequently, the dynamic power is primarily a function of operating frequency rather than active duty cycle (refer to the MK 4116 current waveforms in figure 5). This current characteristic of the MK 4116 precludes inadvertent burn out of the device in the event that the clock inputs become shorted to ground due to system malfunction.

Although no particular power supply noise restriction exists other than the supply voltages remain within the specified tolerance limits, adequate decoupling should be provided to suppress high frequency noise resulting from the transient current of the device. This insures optimum system performance and reliability. Bulk capacitance requirements are minimal since the MK 4116 draws very little steady state (DC) current.

In system applications requiring lower power dissipation, the operating frequency (cycle rate) of the MK 4116 can be reduced and the (guaranteed maximum) average power dissipation of the device will be lowered in accordance with the I_{DD1} (max) spec limit curve illustrated in figure 2. NOTE: The MK 4116 family is guaranteed to have a maximum I_{DD1} requirement of 35mA @ 375ns cycle (320ns cycle for the -2) with an ambient temperature range from 0° to 70°C. A lower operating frequency, for example 1 microsecond cycle, results in a reduced maximum Idd1 requirement of under 20mA with an ambient temperature range from 0° to 70°C.

It is possible the MK4116 family (-2 and 3 speed selections for example) at frequencies higher than specified, provided all AC operating parameters are met. Operation at shorter cycle times (<tRC min) results in higher power dissipation and, therefore, a reduction in ambient temperature is required. Refer to Figure 1 for derating curve.

NOTE: Additional power supply tolerance has been included on the VBB supply to allow direct interface capability with both -5V systems -5.2V ECL systems.

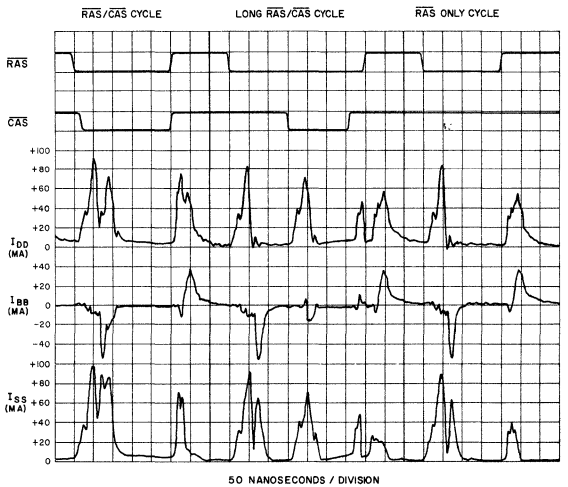


Fig. 5 Typical Current Waveforms

Although $\overline{RAS}$ and/or $\overline{CAS}$ can be decoded and used as a chip select signal for the MK 4116, overall system power is minimized if the Row Address Strobe ($\overline{RAS}$) is used for this purpose. All unselected devices (those which do not receive a $\overline{RAS}$) will remain in a low power (standby) mode regardless of the state of $\overline{CAS}$.

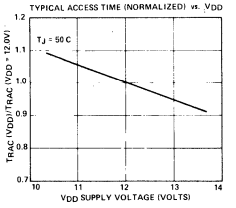
POWER UP

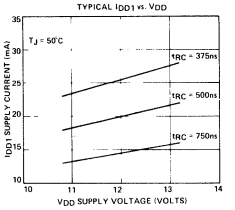
The MK 4116 requires no particular power supply sequencing so long as the Absolute Maximum Rating Conditions are observed. However, in order to insure compliance with the Absolute Maximum Ratings, MOSTEK recommends sequencing of power supplies such that V_{BB} is applied first and removed last. V_{BB} should never be more positive than V_{SS} when power is applied to V_{DD}.

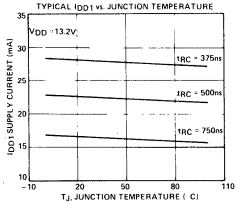
Under system failure conditions in which one or more supplies exceed the specified limits significant additional margin against catastrophic device failure may be achieved by forcing $\overline{RAS}$ and $\overline{CAS}$ to the inactive state (high level).

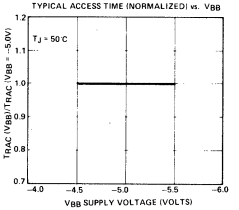
After power is applied to the device, the MK 4116 requires several cycles before proper device operation is achieved. Any 8 cycles which perform refresh are adequate for this purpose.

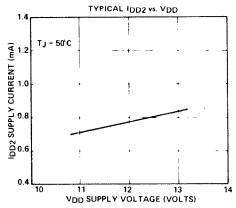
TYPICAL CHARACTERISTICS

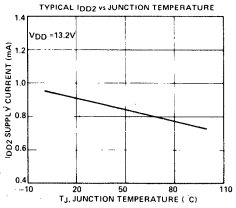


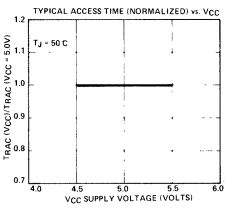


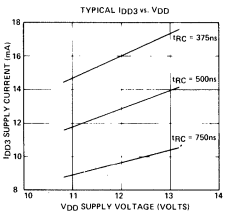


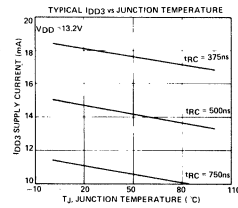


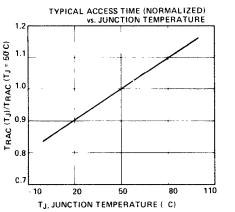


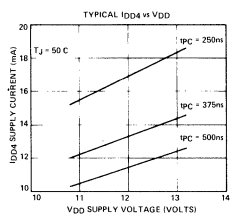


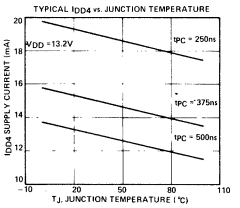


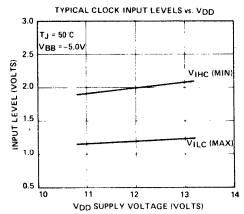


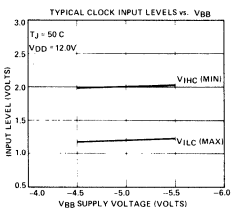


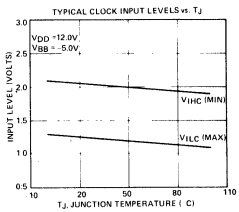


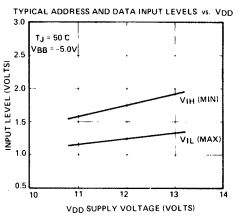


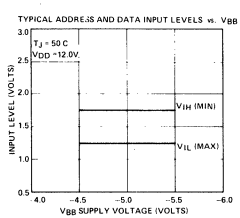


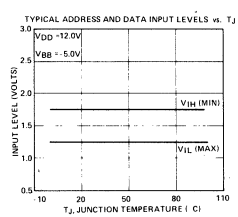












MOSTEK®

16,384 x 1-BIT DYNAMIC RAM

MK4116(J/N/E)-4

FEATURES

- ☐ Recognized industry standard 16-pin configuration from MOSTEK
- ☐ 250ns access time, 410ns cycle
- ☐ ± 10% tolerance on all power supplies (+12V, ±5V)
- ☐ Low power: 462mW active, 20mW standby (max)
- ☐ Output data controlled by $\overline{CAS}$ and unlatched at end of cycle to allow two dimensional chip selection and extended page boundary
- ☐ Common I/O capability using "early write" operation
- ☐ Read-Modify-Write, $\overline{RAS}$-only refresh, and Page-mode capability
- ☐ All inputs TTL compatible,low capacitance, and protected against static charge
- ☐ **128 refresh cycles (2 msec refresh interval)**
- ☐ ECL compatible on V_{BB} power supply (-5.7V)
- ☐ MKB version screened to MIL-STD-883
- ☐ JAN version available to MIL-M-38510/240

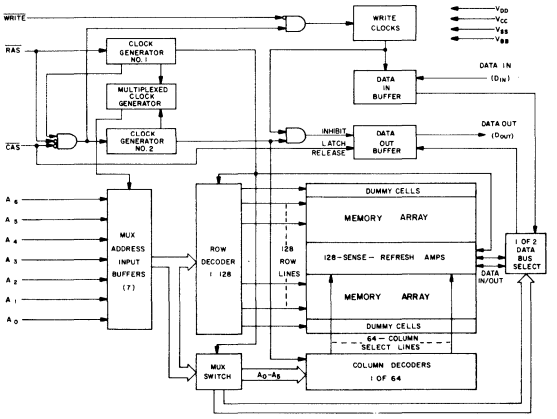
DESCRIPTION

The MK 4116 is a new generation MOS dynamic random access memory circuit organized as 16,384 words by 1 bit. As a state-of-the-art MOS memory device, the MK 4116 (16K RAM) incorporates advanced circuit techniques designed to provide wide operating margins, both internally and to the system user, while achieving performance levels in speed and power previously seen only in MOSTEK's high performance MK 4027 (4K RAM).

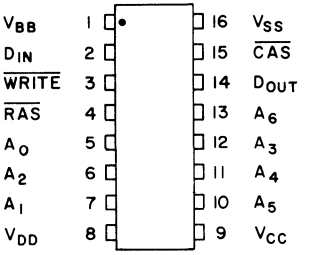
The technology used to fabricate the MK 4116 is MOSTEK's double-poly, N-channel silicon gate, POLY II™ process. This process, coupled with the use of a single transistor dynamic storage cell, provides the maximum possible circuit density and reliability, while maintaining high performance capability. The use of dynamic circuitry throughout, including sense amplifiers, assures that power dissipation is minimized without any sacrifice in speed or operating margin. These factors combine to make the MK 4116 a truly superior RAM product.

Multiplexed address inputs (a feature pioneered by MOSTEK for its 4K RAMS) permits the MK 4116 to be packaged in a standard 16-pin DIP. This recognized industry standard package configuration, while compatible with widely available automated testing and insertion equipment, provides highest possible system bit densities and simplifies system upgrade from 4K to 16K RAMs for new generation applications. Non-critical clock timing requirements allow use of the multiplexing technique while maintaining high performance.

FUNCTIONAL DIAGRAM



PIN CONNECTIONS



PIN FUNCTIONS

A_0-A_6	Address Inputs	$\overline{WRITE}$	Read/Write Input
$\overline{CAS}$	Column Address Strobe	V_{BB}	Power (-5V)
		V_{CC}	Power (+5V)
D_{IN}	Data In	V_{DD}	Power (+12V)
D_{OUT}	Data Out	V_{SS}	Ground
$\overline{RAS}$	Row Address Strobe		

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to V_{BB} ..... −0.5V to +20V
Voltage on V_{DD}, V_{CC} supplies relative to V_{SS} ..... −1.0V to +15.0V
$V_{BB}-V_{SS}$ ($V_{DD}-V_{SS}>0V$) 0V
Operating temperature, T_A (Ambient) ..... 0°C to + 70°C
Storage temperature (Ambient) (Ceramic) ..... -65°C to + 150°C
Storage temperature (Ambient) (Plastic) ..... -55°C to + 125°C
Short circuit output current 50mA
Power dissipation ..... 1 Watt

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS
($0°C \leq T_A \leq 70°C$)[1]

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{DD} V_{CC} V_{SS} V_{BB}	10.8 4.5 0 −4.5	12.0 5.0 0 −5.0	13.2 5.5 0 −5.7	Volts Volts Volts Volts	1 1,2 1 1
Input High (Logic 1) Voltage, $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	V_{IHC}	2.4	–	7.0	Volts	1
Input High (Logic 1) Voltage, all inputs except $\overline{RAS}$, $\overline{CAS}$ $\overline{WRITE}$	V_{IH}	2.2	–	7.0	Volts	1
Input Low (Logic 0) Voltage, all inputs	V_{IL}	−1.0	–	.8	Volts	1

DC ELECTRICAL CHARACTERISTICS
($0°C \leq T_A \leq 70°C$)[1] (V_{DD} = 12.0V ±10%; V_{CC} = 5.0V ±10%; -5.7V ≤ V_{BB} ≤ -4.5; V_{SS} =0V)

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
OPERATING CURRENT Average power supply operating current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = 410ns)	I_{DD1} I_{CC1} I_{BB1}		35 200	mA µA	3 4
STANDBY CURRENT Power supply standby current ($\overline{RAS}$ = V_{IHC}, D_{OUT} = High Impedance)	I_{DD2} I_{CC2} I_{BB2}	 −10 	1.5 10 	mA µA µA	
REFRESH CURRENT Average power supply current, refresh mode ($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IHC}; t_{RC} = 410ns)	I_{DD3} I_{CC3} I_{BB3}	 −10 	27 10 	mA µA µA	3
PAGE MODE CURRENT Average power supply current, page-mode operation ($\overline{RAS}$ =V_{IL},$\overline{CAS}$ cycling; t_{PC} = 275ns)	I_{DD4} I_{CC4} I_{BB4}		27 	mA µA	3 4
INPUT LEAKAGE Input leakage current, any input (V_{BB} = −5V, 0V ≤ V_{IN} ≤ +7.0V, all other pins not under test = 0 volts)	$I_{I(L)}$	−10	10	µA	
OUTPUT LEAKAGE Output leakage current (D_{OUT} is disabled, 0V ≤ V_{OUT} ≤ +5.5V)	$I_{O(L)}$	−10	10	µA	
OUTPUT LEVELS Output high (Logic 1) voltage (I_{OUT} = −5mA) Output low (Logic 0) voltage (I_{OUT} = 4.2 mA)	V_{OH} V_{OL}	2.4 	 0.4	Volts Volts	3

NOTES:

1. All voltages referenced to V_{SS}.
2. Output voltage will swing from V_{SS} to V_{CC} when activated with no current loading. For purposes of maintaining data in standby mode, V_{CC} may be reduced to V_{SS} without affecting refresh operations or data retention. However, the V_{OH} (min) specification is not guaranteed in this mode.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (5,6,7)

($0°C \leq T_A \leq 70°C$) V_{DD} = 12.0V ±10%; V_{CC} = 5.0V ±10%; V_{SS} = 0V, -5.7V ≤ V_{BB} ≤ -4.5V)

PARAMETER	SYMBOL	MK4116-4 MIN	MK4116-4 MAX	UNITS	NOTES
Random read or write cycle time	t_{RC}	410		ns	
Read-write cycle time	t_{RWC}	425		ns	
Read Modify Write	t_{RMW}	500		ns	
Page mode cycle time	t_{PC}	275		ns	
Access time from $\overline{RAS}$	t_{RAC}		250	ns	8,10
Access time from $\overline{CAS}$	t_{CAC}		165	ns	9,10
Output buffer turn-off delay	t_{OFF}	0	60	ns	11
Transition time (rise and fall)	t_T	3	50	ns	7
$\overline{RAS}$ precharge time	t_{RP}	150		ns	
$\overline{RAS}$ pulse width	t_{RAS}	250	10000	ns	
$\overline{RAS}$ hold time	t_{RSH}	165		ns	
$\overline{CAS}$ pulse width	t_{CAS}	165	10000	ns	
$\overline{CAS}$ hold time	t_{CSH}	250		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	35	85	ns	12
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	−20		ns	
Row Address set-up time	t_{ASR}	0		ns	
Row Address hold time	t_{RAH}	35		ns	
Column Address set-up time	t_{ASC}	−10		ns	
Column Address hold time	t_{CAH}	75		ns	
Column Address hold time referenced to $\overline{RAS}$	t_{AR}	160		ns	
Read command set-up time	t_{RCS}	0		ns	
Read command hold time	t_{RCH}	0		ns	
Write command hold time	t_{WCH}	75		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	160		ns	
Write command pulse width	t_{WP}	75		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	85		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	85		ns	
Data-in set-up time	t_{DS}	0		ns	13
Data-in hold time	t_{DH}	75		ns	13
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	160		ns	
$\overline{CAS}$ precharge time (for page-mode cycle only)	t_{CP}	100		ns	
Refresh period	t_{REF}		2	ms	
$\overline{WRITE}$ command set-up time	t_{WCS}	−20		ns	14
$\overline{CAS}$ to $\overline{WRITE}$ delay	t_{CWD}	90		ns	14
$\overline{RAS}$ to $\overline{WRITE}$ delay	t_{RWD}	175		ns	14

3. I_{DD1}, I_{DD3}, and I_{DD4} depend on cycle rate. The maximum specified current values are for t_{RC}=410ns and t_{PC}=275ns. I_{DD} limit at other cycle rates are determined by the following equations:

   I_{DD1} (max) [MA] = 10+10.25 x cycle rate [MHz]
   I_{DD3} (max) [MA] = 10+7 x cycle rate [MHz]
   I_{DD4} (max) [MA] = 10 + 4.7 x cycle rate [MHz]

4. I_{CC1} and I_{CC4} depend upon output loading. During readout of high level data V_{CC} is connected through a low impedance (135 typ) to data out. At all other times I_{CC} consists of leakage currents only.

5. Several cycles are required after power-up before proper device operation is achieved. Any 8 cycles which perform refresh are adequate for this purpose.

6. AC measurements assume t_T=5ns.

7. V_{IHC} (min) or V_{IH}((min) and V_{IL}(max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IHC} or V_{IH} and V_{IL}.

8. Assumes that $t_{RCD} \leq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.

9. Assumes that $t_{RCD} \geq t_{RCD}$ (max).

10. Measured with a load equivalent to 2 TTL loads and 100pF.

11. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

12. Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.

13. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in delayed write or read-modify-write cycles.

14. t_{WCS}, t_{CWD} and t_{RWD} are restrictive operating parameters in read write and read modify write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; If $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min), the cycle is a read-write cycle and the data out will contain data read from the selected cell; If neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.

15. Effective capacitance calculated from the equation $C = I \frac{\Delta t}{\Delta v}$ with Δv = 3 volts and power supplies at nominal levels.

16. $\overline{CAS}$ = V_{IHC} to disable D_{OUT}.

AC ELECTRICAL CHARACTERISTICS
($0°C \leq T_A \leq 70°C$) (V_{DD} = 12.0V ±10%; V_{SS} = 0V, -5.7V ≤ V_{BB} ≤ -4.5V)

PARAMETER	SYMBOL	TYP	MAX	UNITS	NOTES
Input Capacitance (A_0–A_6), D_{IN}	C_{I1}	4	5	pF	17
Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	C_{I2}	8	10	pF	17
Output Capacitance (D_{OUT})	C_O	5	7	pF	17,18

DESCRIPTION (continued)

System oriented features include ± 10% tolerance on all power supplies, direct interfacing capability with high performance logic families such as Schottky TTL, maximum input noise immunity to minimize "false triggering" of the inputs (a common cause of soft errors), on-chip address and data registers which eliminate the need for interface registers, and two chip select methods to allow the user to determine the appropriate speed/power characteristics of his memory system. The MK 4116 also incorporates several flexible timing/operating modes. In addition to the usual read, write, and read-modify-write cycles, the MK 4116 is capable of delayed write cycles, page-mode operation and $\overline{RAS}$-only refresh. Proper control of the clock inputs($\overline{RAS}$, $\overline{CAS}$ and $\overline{WRITE}$) allows common I/O capability, two dimensional chip selection, and extended page boundaries (when operating in page mode).

SUPPLEMENTAL DATA SHEET TO BE USED IN CONJUNCTION WITH MOSTEK MK4116(J/N/E)-2/3 DATA SHEET.

PRELIMINARY

MOSTEK®

MEMORY COMPONENTS

16,384 x 1-Bit Dynamic RAM
MK4516(N/J)-10/12/15

IV

FEATURES

- Recognized industry standard 16-pin configuration from Mostek
- Single +5 V (± 10%) supply operation
- On chip substrate bias generator for optimum performance
- Active power 193 mW maximum
  Standby power 20 mW maximum (MK4516-10)
  Standby power 17 mW maximum (MK4516-12/15)
- 100 ns access time, 235 ns cycle time (MK4516-10)
  120 ns access time, 270 ns cycle time (MK4516-12)
  150 ns access time, 320 ns cycle time (MK4516-15)
- Common I/O capability using "early write"
- Read, Write, Read-Write, Read-Modify-Write and Page-Mode capability
- All inputs TTL compatible, low capacitance, and protected against static charge
- Scaled POLY 5 technology
- Pin compatible with the MK4564 (64K RAM)
- 128 refresh cycles (2 msec)

DESCRIPTION

The MK4516 is a single +5 V power supply version of the industry standard MK4116, 16,384 x 1 bit dynamic RAM.

The high performance features of the MK4516 are achieved by state-of-the-art circuit design techniques as well as utilization of Mostek's "Scaled POLY 5" process technology. Features include access times starting where the current generation 16K RAMs leave off, TTL compatability, and +5 V only operation.

The MK4516 is capable of a variety of operations including READ, WRITE, READ-WRITE, READ-MODIFY-WRITE, PAGE MODE, and REFRESH.

The MK4516 is designed to be compatible with the JEDEC standards for the 16K x 1 dynamic RAM. The MK4516 is intended to extend the life cycle of the 16K RAM, as well as create new applications due to its superior performance. The compatability with the MK4564 will also permit a common board design to service both the MK4516 and MK4564 (64K RAM) designs. The MK4516 will therefore permit a smoother transition to the 64K RAM as the industry standard MK4027 did for the MK4116.

The user requiring only a small memory size need no longer pay the three power supply penalty for achieving the economics of using dynamic RAM over static RAM when using this new generation device.

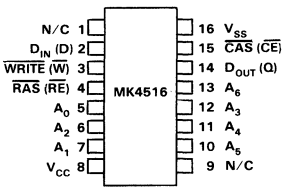
PIN FUNCTIONS

A_0-A_6	Address Inputs	$\overline{RAS}$ ($\overline{RE}$)	Row Address Strobe
$\overline{CAS}$ ($\overline{CE}$)	Col. Address Strobe	$\overline{WRITE}$ ($\overline{W}$)	Read/Write Input
D_{IN} (D)	Data In	N/C	Not connected
D_{OUT} (Q)	Data Out	V_{CC}	Power (+5V)
		V_{SS}	GND

PIN OUT

Figure 1

DUAL-IN-LINE PACKAGE



Available soon in MIL-STD-883 Class B (MKB4516)

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -1.0 V to +7.0 V
Operating Temperature, T_A (Ambient) ..... 0°C to +70°C
Storage Temperature (Ceramic) ..... -65°C to +150°C
Storage Temperature (Plastic) ..... -55°C to +125°C
Power Dissipation ..... 1 Watt
Short Circuit Output Current ..... 50 mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High (Logic 1) Voltage, All Inputs	2.4	—	V_{CC}+1	V	2
V_{IL}	Input Low (Logic 0) Voltage, All Inputs	-2.0	—	.8	V	2,19

DC ELECTRICAL CHARACTERISTICS

(0°C ≤ T_A ≤ 70°C) (V_{CC} = 5.0 V ± 10%)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC1}	OPERATING CURRENT Average power supply operating current ($\overline{RAS}$, $\overline{CAS}$ cycling, t_{RC} = t_{RC} min.)		35	mA	3
I_{CC2}	STANDBY CURRENT Power supply standby current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH}, D_{OUT} = High Impedance)		3	mA	
			3.5	mA	21
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average power supply current, refresh mode ($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}; t_{RC} = t_{RC} min.)		30	mA	3
I_{CC4}	PAGE MODE CURRENT Average power supply current, page mode operation ($\overline{RAS}$ = V_{IL}, t_{RAS} = t_{RAS} max., $\overline{CAS}$ cycling; t_{PC} = t_{PC} min.)		32	mA	3,20
$I_{I(L)}$	INPUT LEAKAGE Input leakage current, any input (0 V ≤ V_{IN} ≤ +5.5 V, all other pins not under test = 0 volts)	-10	10	μA	
$I_{O(L)}$	OUTPUT LEAKAGE Output leakage current (D_{OUT} is disabled, 0 V ≤ V_{OUT} ≤ +5.5 V)	-10	10	μA	
	OUTPUT LEVELS				
V_{OH}	Output High (Logic 1) voltage (I_{OUT} = -5 mA)	2.4		V	
V_{OL}	Output Low (Logic 0) voltage (I_{OUT} = 4.2 mA		0.4	V	

AC ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS [4,5,6,16]

($0°C \leq T_A \leq 70°C$), $V_{CC} = 5.0\ V \pm 10\%$

SYMBOL			MK4516-10		MK4516-12		MK4516-15			
STD	ALT	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
t_{RELREL}	t_{RC}	Random read or write cycle time	235		270		320		ns	7,8
t_{RELREL} (RMW)	t_{RMW}	Read-modify-write cycle time	285		320		410		ns	7,8
t_{RELREL} (PC)	t_{PC}	Page mode cycle time	125		145		190		ns	7,8,20
t_{RELQV}	t_{RAC}	Access time from $\overline{RAS}$		100		120		150	ns	8,9
t_{CELQV}	t_{CAC}	Access time from $\overline{CAS}$		55		65		80	ns	8,10
t_{CEHQZ}	t_{OFF}	Output buffer turn-off delay	0	45	0	50	0	60	ns	11
t_T	t_T	Transition time (rise and fall)	3	50	3	50	3	50	ns	6,16
t_{REHREL}	t_{RP}	$\overline{RAS}$ precharge time	110		120		135		ns	
t_{RELREH}	t_{RAS}	$\overline{RAS}$ pulse width	115	10^4	140	10^4	175	10^4	ns	
t_{CELREH}	t_{RSH}	$\overline{RAS}$ hold time	70		85		105		ns	
t_{RELCEH}	t_{CSH}	$\overline{CAS}$ hold time	100		120		165		ns	
t_{CELCEH}	t_{CAS}	$\overline{CAS}$ pulse width	55	10^4	65	10^4	95	10^4	ns	
t_{RELCEL}	t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ delay time	25	45	25	55	25	70	ns	12
t_{REHWX}	t_{RRH}	Read command hold time referenced to $\overline{RAS}$	0		0		0		ns	13
t_{AVREL}	t_{ASR}	Row Address set-up time	0		0		0		ns	
t_{RELAX}	t_{RAH}	Row Address hold time	15		15		15		ns	
t_{AVCEL}	t_{ASC}	Column Address set-up time	0		0		0		ns	
t_{CELAX}	t_{CAH}	Column Address hold time	15		15		20		ns	
$t_{RELA(C)X}$	t_{AR}	Column Address hold time referenced to $\overline{RAS}$	60		70		90		ns	
t_{WHCEL}	t_{RCS}	Read command set-up time	0		0		0		ns	
t_{CEHWX}	t_{RCH}	Read command hold time referenced to $\overline{CAS}$	0		0		0		ns	13
t_{CELWX}	t_{WCH}	Write command hold time	25		30		45		ns	
t_{RELWX}	t_{WCR}	Write command hold time referenced to $\overline{RAS}$	70		85		115		ns	
t_{WLWH}	t_{WP}	Write command pulse width	25		30		50		ns	
t_{WLREH}	t_{RWL}	Write command to $\overline{RAS}$ lead time	60		65		110		ns	
t_{WLCEH}	t_{CWL}	Write command to $\overline{CAS}$ lead time	45		50		100		ns	

IV

AC ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS (Continued)

SYMBOL			MK4516-10		MK4516-12		MK4516-15			
STD	ALT	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
t_{DVCEL}	t_{DS}	Data-in set-up time	0		0		0		ns	14
t_{CELDX}	t_{DH}	Data-in hold time	25		30		45		ns	14
t_{RELDX}	t_{DHR}	Data-in hold time referenced to $\overline{RAS}$	70		85		115		ns	
t_{CEHCEL} (PC)	t_{CP}	$\overline{CAS}$ precharge time (for page mode cycle only)	60		70		85		ns	20
t_{RVRV}	t_{REF}	Refresh period		2		2		2	ms	
t_{WLCEL}	t_{WCS}	WRITE command set-up time	0		0		0		ns	15
t_{CELWL}	t_{CWD}	$\overline{CAS}$ to $\overline{WRITE}$ delay	55		65		80		ns	15
t_{RELWL}	t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ delay	100		120		150		ns	15
t_{CEHREL}	t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ precharge time	0		0		0		ns	

CAPACITANCE

($0°C \leq T_A \leq 70°C$) (V_{CC} = 5.0 V ± 10%)

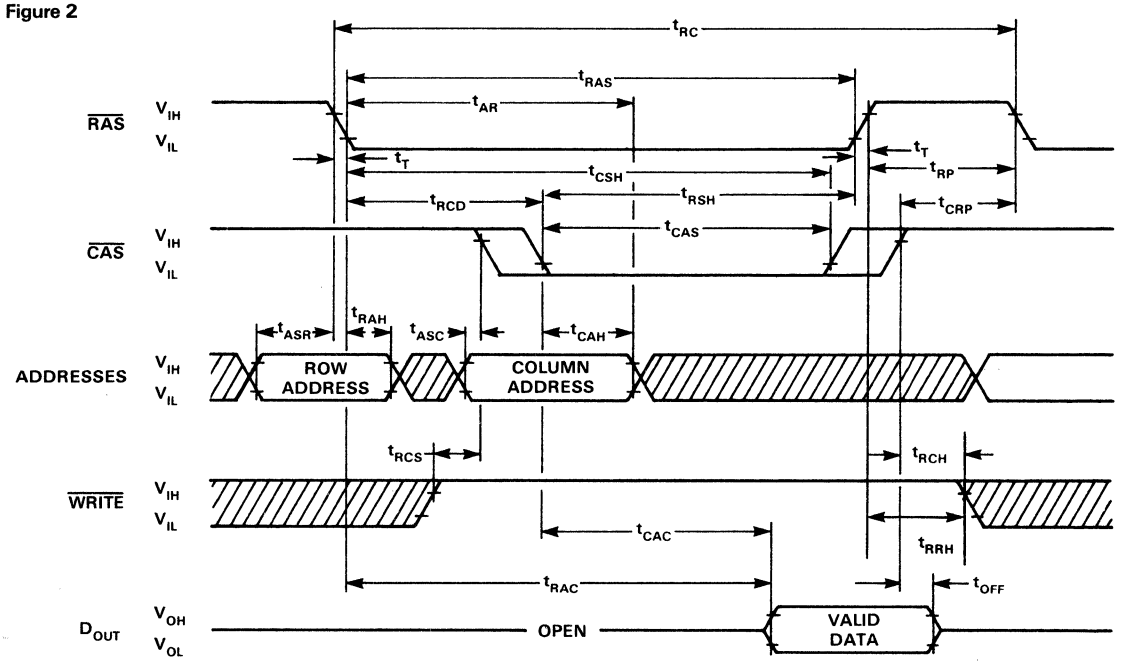
SYMBOL	PARAMETER	TYP	MAX	UNITS	NOTES
C_{I1}	Input (A_0-A_6), D_{IN}	4	5	pF	17
C_{I2}	Input $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	8	10	pF	17
C_O	Output (D_{OUT})	5	7	pF	17,18

NOTES:

1. No user connection to Pin 1 (Leadless Chip Carrier only). This pin must be left floating.
2. All voltages referenced to V_{SS}.
3. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open.
4. An initial pause of 500 μs is required after power-up followed by any 8 $\overline{RAS}$ start-up cycles before proper device operation is achieved. $\overline{RAS}$ may be cycled during the initial pause. If $\overline{RAS}$ inactive interval exceeds 2ms, the device must be re-initialized by a minimum of 8 $\overline{RAS}$ start-up cycle.
5. AC characteristics assume t_T = 5 ns
6. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
7. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \leq T_A \leq 70°C$) is assured.
8. Load = 2 TTL loads and 100 pF.
9. Assumes that $t_{RCD} \leq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
10. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
11. t_{OFF} max defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
12. Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
13. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
14. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in delayed write or read-modify-write.
15. t_{WCS}, t_{CWD}, and t_{RWD} are restrictive operating parameters in READ/WRITE and READ/MODIFY/WRITE cycles only. If $t_{WCS} \geq t_{WCS}$ (min) the cycle is an EARLY WRITE cycle and the data output will remain open circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min) the cycle is a READ/WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met the condition of the data out (at access time and until $\overline{CAS}$ goes back to V_{IH}) is indeterminate.
16. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
17. Effective capacitance calculated from the equation $c = I \frac{\Delta T}{\Delta V}$ with ΔV = 3 volts and power supply at nominal level.
18. $\overline{CAS}$ = V_{IH} to disable D_{OUT}.
19. Includes the dc level and all instantaneous signal excursions.
20. Page Mode operation is not guaranteed on the standard MK4516. This function is available on request.
21. Applies to MK4516-10 only.

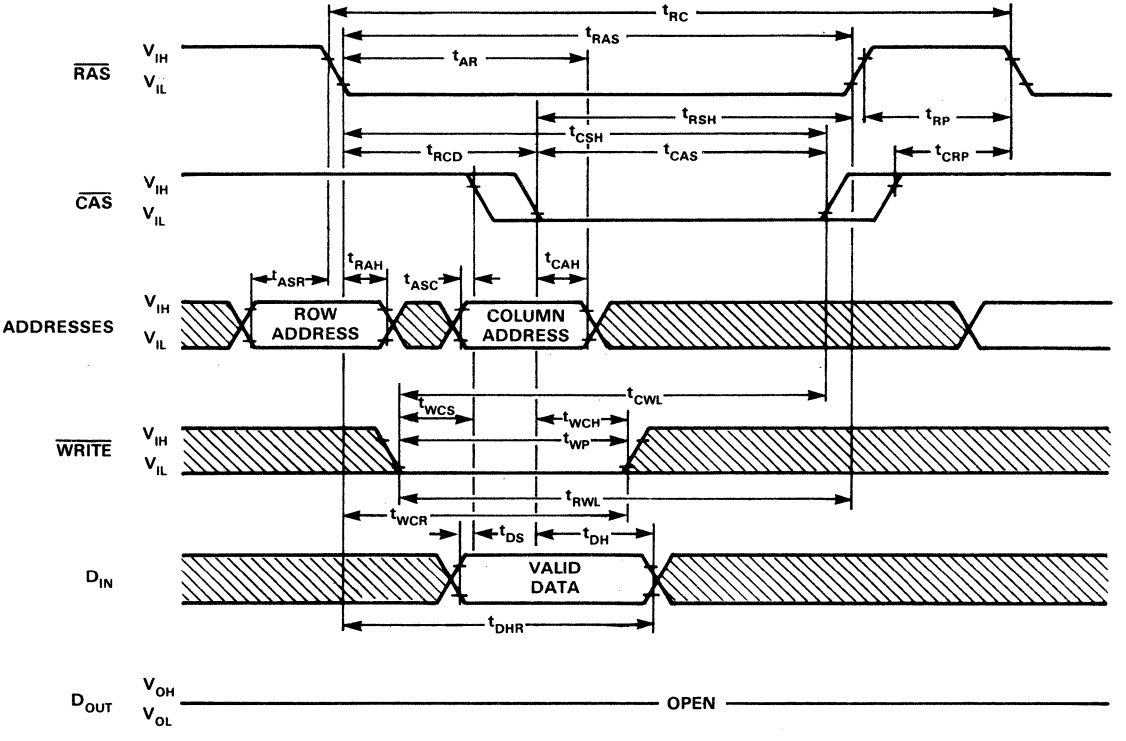
READ CYCLE

Figure 2



WRITE CYCLE (EARLY WRITE)

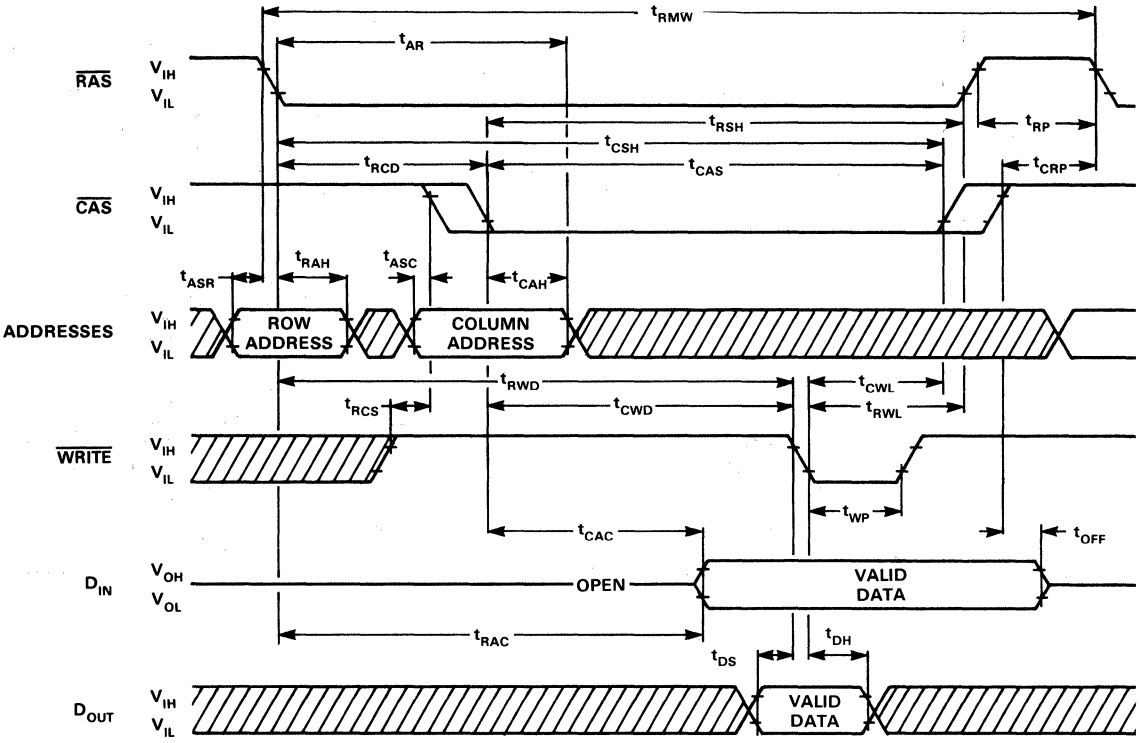
Figure 3



IV

READ-WRITE/READ-MODIFY-WRITE CYCLE

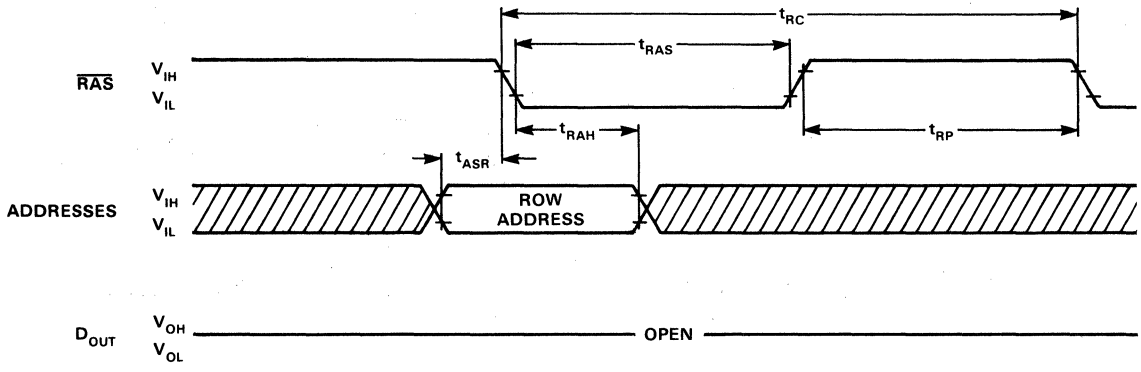
Figure 4



"$\overline{RAS}$-ONLY" REFRESH CYCLE

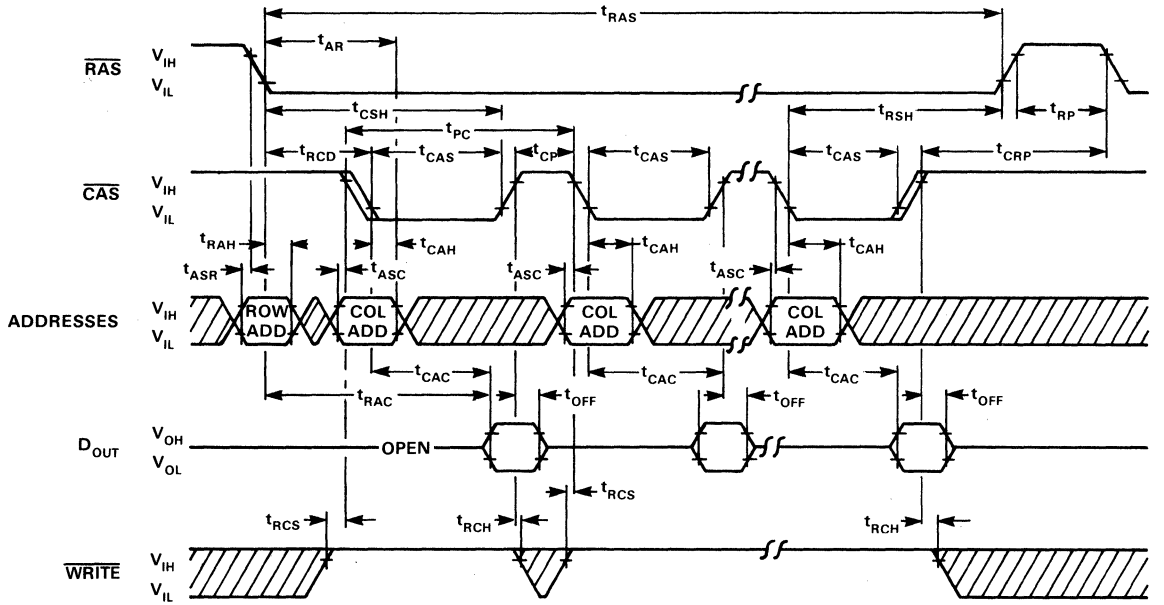
NOTE: $\overline{CAS}$ = V_{IH}, $\overline{WRITE}$ = DON'T CARE

Figure 5



PAGE MODE READ CYCLE (20)

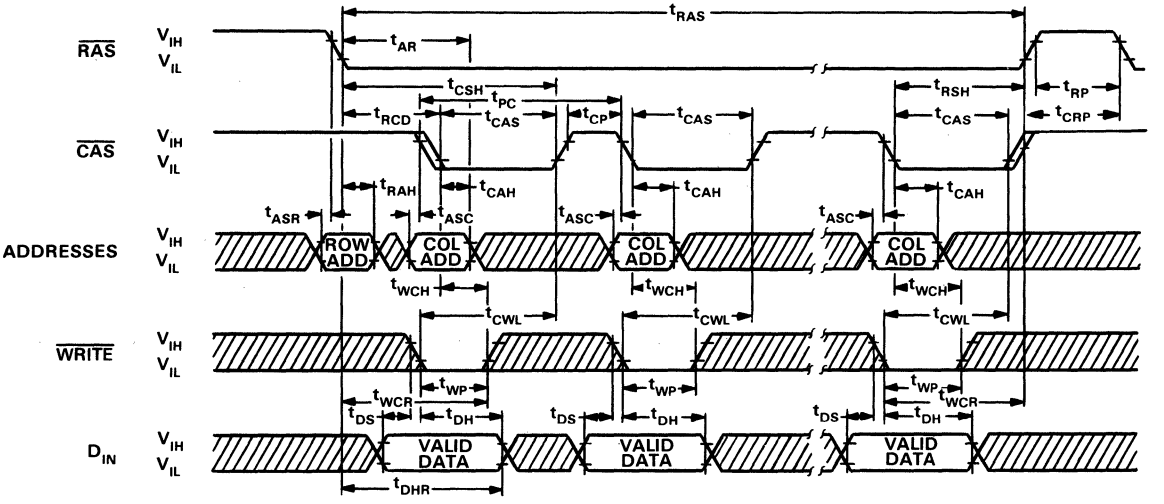
Figure 6



IV

PAGE MODE WRITE CYCLE (20)

Figure 7



OPERATION

The 14 address bits required to decode 1 of the 16,384 cell locations within the MK4516 are multiplexed onto the 7 address inputs and latched into the on-chip address latches by externally applying two negative going TTL-level clocks. The first clock, Row Address Strobe ($\overline{RAS}$), latches the 7 row addresses into the chip. The high-to-low transition of the second clock, Column Address Strobe ($\overline{CAS}$), subsequently latches the 7 column addresses into the chip. Each of these signals, $\overline{RAS}$ and $\overline{CAS}$, triggers a sequence of events which are controlled by different delayed internal clocks. The two clock chains are linked together logically in such a way that the address multiplexing operation is done outside of the critical timing path for read data access. The later events in the $\overline{CAS}$ clock sequence are inhibited until the occurrence of a delayed signal derived from the $\overline{RAS}$ clock chain. This "gated $\overline{CAS}$" feature allows the $\overline{CAS}$ clock to be externally activated as soon as the Row Address Hold specification (t_{RAH}) has been satisfied and the address inputs have been changed from Row address to Column address information.

The "gated $\overline{CAS}$" feature permits $\overline{CAS}$ to be activated at any time after t_{RAH} and it will have no effect on the worst case data access time (t_{RAC}) up to the point in time when the delayed row clock no longer inhibits the remaining sequence of column clocks. Two timing endpoints result from the internal gating of $\overline{CAS}$ which are called t_{RCD} (min) and t_{RCD} (max). No data storage or reading errors will result if $\overline{CAS}$ is applied to the MK4516 at a point in time beyond the t_{RCD} (max) limit. However, access time will then be determined exclusively by the access time from $\overline{CAS}$ (t_{CAC}) rather than from $\overline{RAS}$ (t_{RAC}), and $\overline{RAS}$ access time will be lengthened by the amount that t_{RCD} exceeds the t_{RCD} (max) limit.

Data Input/Output

Data to be written into a selected cell is latched into an on-chip register by a combination of $\overline{WRITE}$ and $\overline{CAS}$ while $\overline{RAS}$ is active. The latter of $\overline{WRITE}$ or $\overline{CAS}$ to make its negative transition is the strobe for the Data In (D_{IN}) register. This permits several options in the write cycle timing. In a write cycle, if the $\overline{WRITE}$ input is brought low (active) prior to $\overline{CAS}$ being brought low (active), the D_{IN} is strobed by $\overline{CAS}$, and the Input Data set-up and hold times are referenced to $\overline{CAS}$. If the input data is not available at $\overline{CAS}$ time (late write) or if it is desired that the cycle be a read-write or read-modify-write cycle the $\overline{WRITE}$ signal should be delayed until after $\overline{CAS}$ has made its negative transition. In this "delayed write cycle" the data input set-up and hold times are referenced to the negative edge of $\overline{WRITE}$ rather than $\overline{CAS}$.

Data is retrieved from the memory in a read cycle by maintaining $\overline{WRITE}$ in the inactive or high state throughout the portion of the memory cycle in which both the $\overline{RAS}$ and $\overline{CAS}$ are low (active). Data read from the selected cell is available at the output port within the specified access time. The output data is the same polarity (not inverted) as the input data.

Data Output Control

The normal condition of the Data Output (D_{OUT}) of the MK4516 is the high impedance (open-circuit) state; anytime $\overline{CAS}$ is high (inactive) the D_{OUT} pin will be floating. Once the output data port has gone active, it will remain valid until $\overline{CAS}$ is taken to the precharge (inactive high) state.

Refresh

Refresh of the dynamic cell matrix is accomplished by performing a memory cycle at all 128 combinations of the seven row address bits within each 2 ms interval. Although any normal memory cycle will perform the required refreshing, this function is most easily accomplished with "$\overline{RAS}$-only" cycles.

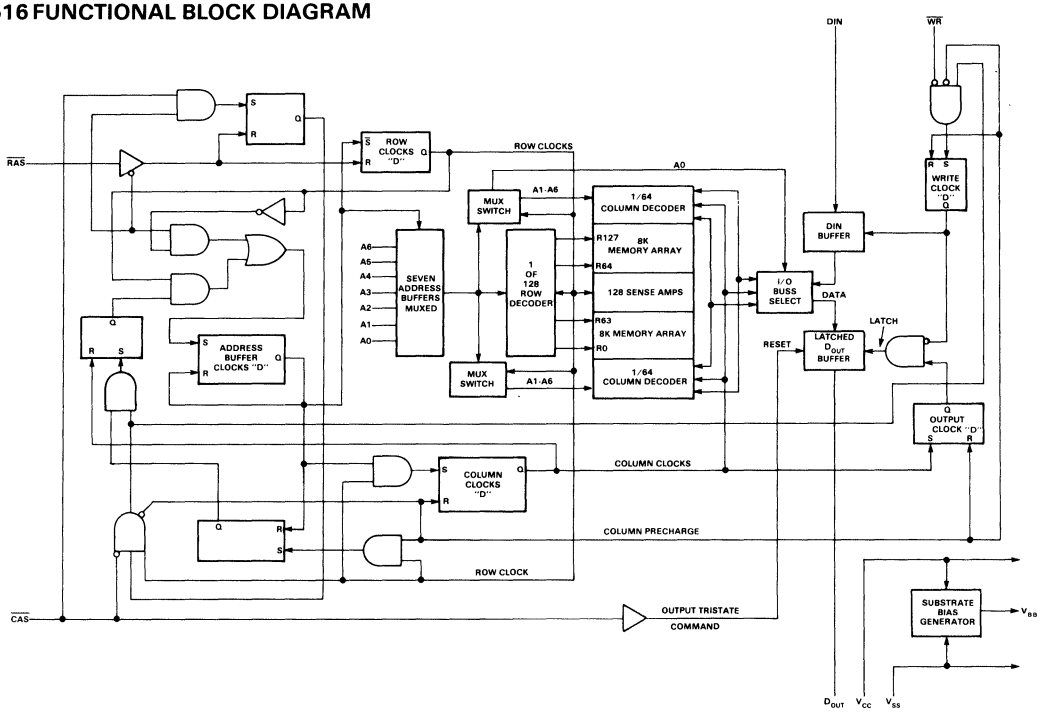
Page Mode Operation *

The Page Mode feature of the MK4516 allows for successive memory operations at multiple column locations within the same row address. This is done by strobing the row address into the chip and maintaining the $\overline{RAS}$ signal low (active) throughout all successive memory cycles in which the row address is common. The first access within a page mode operation will be available at t_{RAC} or t_{CAC} time, whichever is the limiting parameter. However, all successive accesses within the page mode operation will be available at t_{CAC} time (referenced to $\overline{CAS}$). With the MK4516, this results in as much as a 55% improvement in access times! Effective memory cycle times are also reduced when using page mode.

The page mode boundary of a single MK4516 is limited to the 128 column locations determined by all combinations of the seven column address bits. Operations within the page boundary need not be sequentially addressed and any combination of read-write and read-modify-write cycle are permitted within the page mode operation.

* see footnote 20

MK4516 FUNCTIONAL BLOCK DIAGRAM



IV

PRELIMINARY

MOSTEK®

131,072 x 1-BIT DYNAMIC RAM

MK4528(D)-15/20/25

FEATURES

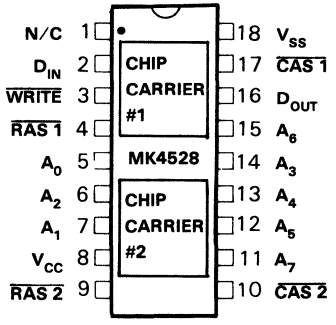
- Utilizes two standard MK4564 devices in an 18-pin package configuration
- Single +5V (± 10%) supply operation
- On chip substrate bias generator for optimum performance
- Active power 320mW (Single MK4564 active) Standby power 44mW
- 150ns access time, 260ns cycle time (MK4564-15) 200ns access time, 345ns cycle time (MK4564-20) 250ns access time, 425ns cycle time (MK4564-25)
- Common I/O capability using "early write"
- Separate $\overline{RAS}$, $\overline{CAS}$ Clocks
- Read, Write, Read-Write, Read-Modify-Write and Page-Mode capability
- All inputs TTL compatible, low capacitance, and are protected against static charge
- Scaled POLY 5 technology
- Pin compatible with the MK4332 (32K RAM)
- 128 refresh cycles (2 msec) for each MK4564 device in the dual density configuration (address A_7 is not used for refresh).
- Extended D_{OUT} hold using CAS control (Hidden Refresh).

DESCRIPTION

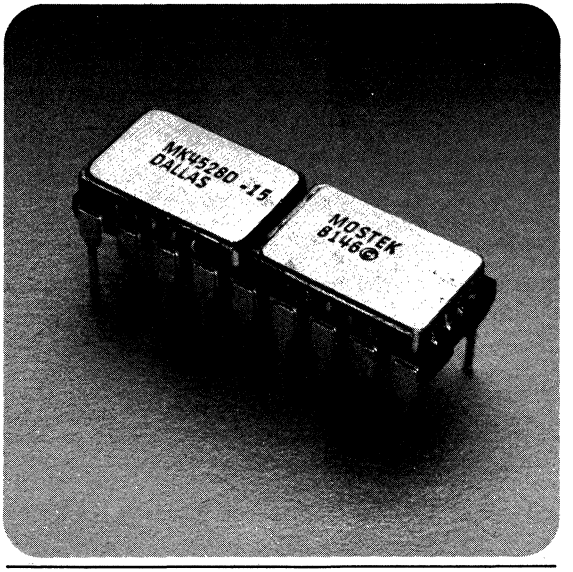
The MK4528 sets a new milestone in the state of the art of package technology to give you dual density now before the next generation of MOS RAMs are available. This device is made up of two 64K (MK4564) 5 volt only RAMs and it is organized as 131,072 words by 1 bit. The upper 16 pins are identical to the industry standard 64K Dual-In Line Package, allowing either device to be installed in the 18 pin position.

The MK4528's high performance features and wide operating margins, both internally and to the system user, are achieved by state-of-the-art circuit design techniques as well as utilization of Mostek's "Scaled POLY 5" process technology.

PIN CONNECTIONS



DEVICE PROFILE



PIN FUNCTION

A_0A_7	Address Inputs	$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe	$\overline{WRITE}$	Read/Write Input
D_{IN}	Data In	V_{CC}	Power (+ 5 V)
D_{OUT}	Data Out	N/C	No Connections
V_{SS}	GND		

Also Available in MIL-STD-883 Class B (MKB)

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0 V to +7.0 V
Operating Temperature, T_A (Ambient) ..... 0°C to +70C
Storage Temperature (Ceramic) ..... -65°C to +150°C
Power Dissipation ..... 1 Watt
Short Circuit Output Current ..... 50 mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	1
V_{IH}	Input High (Logic 1) Voltage, All Inputs	2.4	—	V_{CC}+1	V	1
V_{IL}	Input Low (Logic 0) Voltage, All Inputs	-2.0	—	.8	V	1,18

DC ELECTRICAL CHARACTERISTICS

(0°C ≤ T_A ≤ 70°C) (V_{CC} = 5.0 V ± 10%)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC1}	OPERATING CURRENT Average power supply operating current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = t_{RC} min.)		58	mA	2
I_{CC2}	STANDBY CURRENT Power suply standby current (RAS = V_{IH}, D_{OUT} = High Ipedance)		8	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average power supply current, refresh mode ($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}; t_{RC} = t_{RC} min.)		49	mA	2
I_{CC4}	PAGE MODE CURRENT Average power supply current, page mode operation ($\overline{RAS}$ = V_{IL}, t_{RAS} = t_{RAS} max., $\overline{CAS}$ cycling; t_{PC} = t_{PC} min.)		39	mA	2
$i_{I(L)}$	INPUT LEAKAGE Input leakage current, any input (0V ≤ V_{IN} ≤ V_{CC}), all other pins not under test = 0 volts	-20	20	μA	
$I_{O(L)}$	OUTPUT LEAKAGE Output leakage current (D_{OUT} is disabled, 0V ≤ V_{OUT} ≤ V_{CC})	-20	20	μA	
V_{OH} V_{OL}	OUTPUT LEVELS Output High (Logic 1) voltage (I_{OUT} = -5 mA) Output Low (Logic 0) voltage (I_{OUT} = 4.2 mA)	2.4	 0.4	V V	

NOTES:

1. All voltages referenced to V_{SS}.
2. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open. Only one MK4564 is active.
3. An initial pause of 500 μs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved. Note that $\overline{RAS}$ may be cycled during the initial pause.
4. AC characteristics assume t_T = 5 ns.
5. V_{IH} min. and V_{IL} max. are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
7. Load = 2 TTL loads and 50 pF.
8. Assumes that $t_{RCD} \leq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
9. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
10. t_{OFF} max defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
11. Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
12. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
13. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in delayed write or read-modify-write cycles.
14. t_{WCS}, t_{CWD}, and t_{RWD} are restrictive operating parameters in READ/WRITE and READ/MODIFY/WRITE cycles only. If $t_{WCS} \geq t_{WCS}$ (min) the cycle is an EARLY WRITE cycle and the data output will remain open circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min) the cycle is a READ/WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met the condition of the data out (at access time and until $\overline{CAS}$ goes back to V_{IH}) is indeterminate.
15. In addition to meeting the transition rate specification, all input signals must transmit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
16. Effective capacitance calculated from the equation $C = I \frac{\Delta t}{\Delta V}$ with ΔV = 3 volts and power supply at nominal level.
17. $\overline{CAS}$ = V_{IH} to disable D_{OUT}.
18. Includes the DC level and all instantaneous signal excursions.
19. $\overline{WRITE}$ = don't care. Data out depends on the state of $\overline{CAS}$. If $\overline{CAS}$ = V_{IH}, data output is high impedance. If $\overline{CAS}$ = V_{IL}, the data output will contain data from the last valid read cycle.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(3,4,5,15) (0°C ≤ T_A ≤ 70°C), V_{CC} = 5.0V ± 10%

SYMBOL			MK4528-15		MK4528-20		MK4528-25			
STD	ALT	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
t_{RELREL}	t_{RC}	Random read or write cycle time	260		345		425		ns	6,7
t_{RELREL} (RMW)	t_{RMW}	Read modify write cycle time	310		405		490		ns	6,7
t_{RELREL} (PC)	t_{PC}	Page mode cycle time	155		200		240		ns	6,7
t_{RELQV}	t_{RAC}	Access time from $\overline{RAS}$		150		200		250	ns	7,8
t_{CELQV}	t_{CAC}	Access time from $\overline{CAS}$		85		115		145	ns	7,9
t_{CEHQZ}	t_{OFF}	Output buffer turn-off delay	0	40	0	50	0	60	ns	10
t_T	t_T	Transition time (rise and fall)	3	50	3	50	3	50	ns	5,15
t_{REHREL}	t_{RP}	$\overline{RAS}$ precharge time	100		135		165		ns	
t_{RELREH}	t_{RAS}	$\overline{RAS}$ pulse width	150	10,000	200	10,000	250	10,000	ns	
t_{CELREH}	t_{RSH}	$\overline{RAS}$ hold time	85		115		145		ns	
t_{RELCEH}	t_{CSH}	$\overline{CAS}$ hold time	150		200		250		ns	
t_{CELCEH}	t_{CAS}	$\overline{CAS}$ pulse width	85	10,000	115	10,000	145	10,000	ns	
t_{RELCEL}	t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ delay time	30	65	35	85	45	105	ns	11
t_{REHWX}	t_{RRH}	Read command hold time referenced to $\overline{RAS}$	20		25		30		ns	12
t_{AVREL}	t_{ASR}	Row address set-up time	0		0		0		ns	
t_{RELAX}	t_{RAH}	Row address hold time	20		25		30		ns	
t_{AVCEL}	t_{ASC}	Column address set-up time	0		0		0		ns	
t_{CELAX}	t_{CAH}	Column address hold time	30		40		50		ns	
$t_{RELA(C)X}$	t_{AR}	Column address hold time referenced to $\overline{RAS}$	100		130		160		ns	

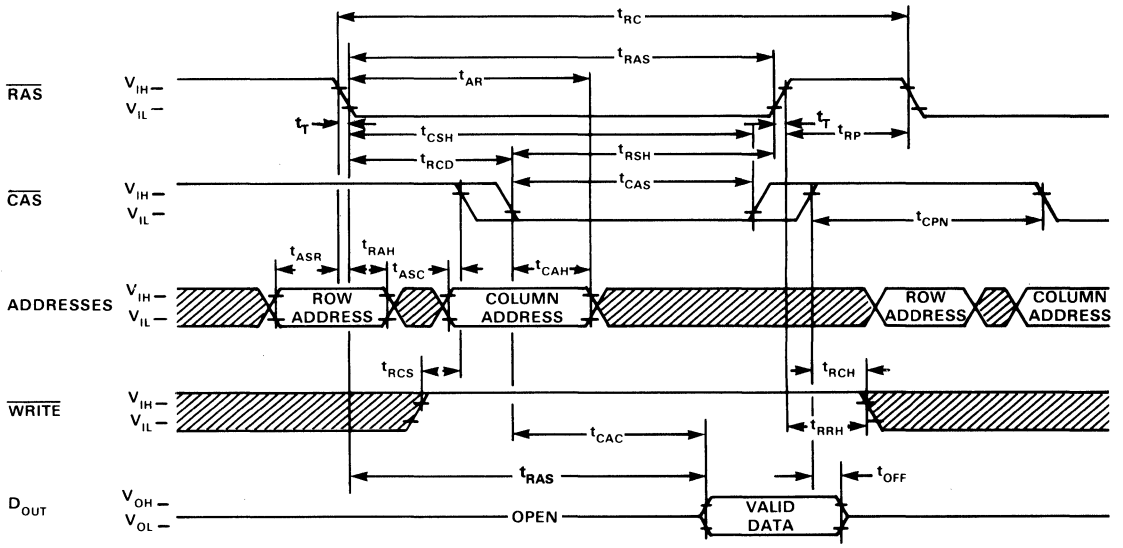
ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Continued)
(3,4,5,15) ($0°C \leq T_A \leq 70°C$), $V_{CC} = 5.0V \pm 10\%$

SYMBOL			MK4528-15		MK4528-20		MK4528-25			
STD	ALT	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
t_{WHCEL}	t_{RCS}	Read command set-up time	0		0		0		ns	
t_{CEHWX}	t_{RCH}	Read command hold time referenced to $\overline{CAS}$	0		0		0		ns	12
t_{CELWX}	t_{WCH}	Write command hold time	45		55		70		ns	
t_{RELWX}	t_{WCR}	Write command hold time referenced to $\overline{RAS}$	115		150		185		ns	
t_{WLWH}	t_{WP}	Write command pulse width	35		45		55		ns	
t_{WLREH}	t_{RWL}	Write command to $\overline{RAS}$ lead time	45		55		65		ns	
t_{WLCEH}	t_{CWL}	Write command to $\overline{CAS}$ lead time	45		55		65		ns	
t_{DVCEL}	t_{DS}	Data-in set-up time	0		0		0		ns	13
t_{CELDX}	t_{DH}	Data-in hold time	45		55		70		ns	13
t_{RELDX}	t_{DHR}	Data-in hold time referenced to $\overline{RAS}$	115		150		190		ns	
t_{CEHCEL} (PC)	t_{CP}	$\overline{CAS}$ precharge time (for page-mode cycle only)	60		75		85		ns	
t_{RVRV}	t_{REF}	Refresh Period		2		2		2	ms	
t_{WLCEL}	t_{WCS}	$\overline{WRITE}$ command set-up time	-10		-10		-10		ns	14
t_{CELWL}	t_{CWD}	$\overline{CAS}$ to $\overline{WRITE}$ delay	55		80		100		ns	14
t_{RELWL}	t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ delay	120		165		205		ns	14
t_{CEHCEL}	t_{CPN}	$\overline{CAS}$ precharge time	30		35		45		ns	

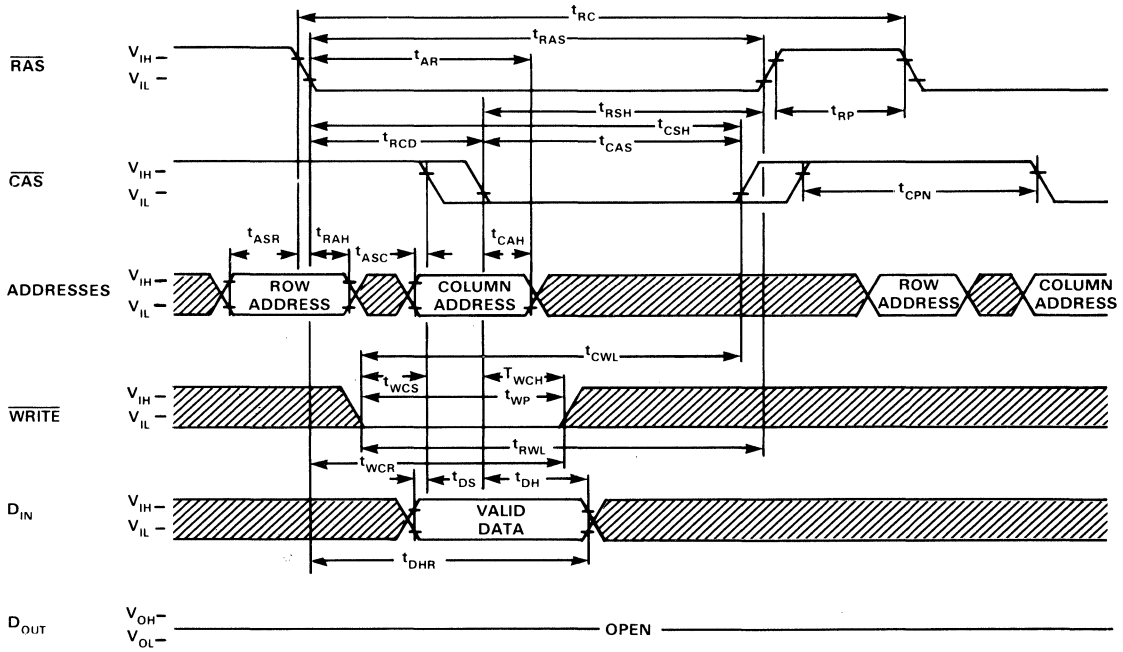
AC ELECTRICAL CHARACTERISTICS
($0°C \leq T_A \leq 70°C$) ($V_{CC} = 5.0V \pm 10\%$)

SYM	PARAMETER	MAX	UNITS	NOTES
C_{I1}	Input Capacitance (A_0 - A_7), D_{IN}	10	pF	16
C_{I2}	Input Capacitance RAS, CAS	10	pF	16
C_{I3}	Input Capacitance $\overline{WRITE}$	20	pF	16
C_O	Output Capacitance (D_{OUT})	14	pF	16,17

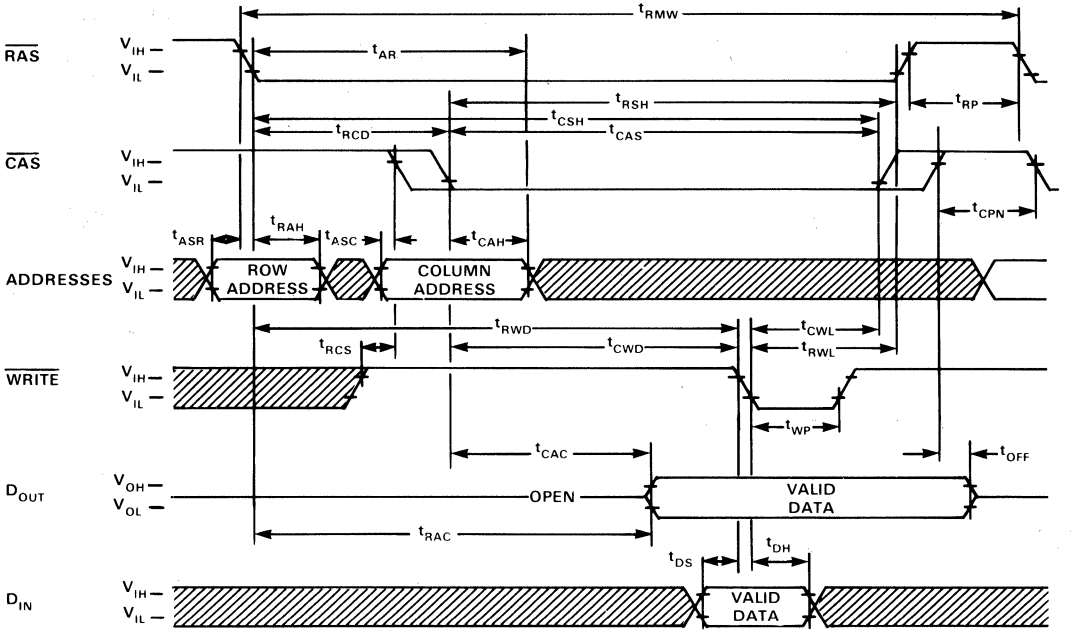
READ CYCLE



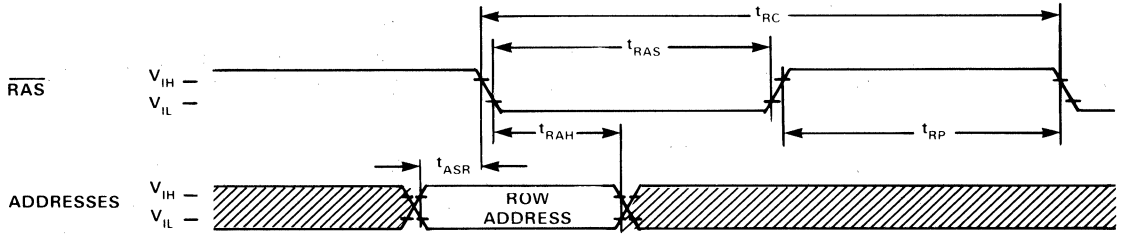
WRITE CYCLE (EARLY WRITE)



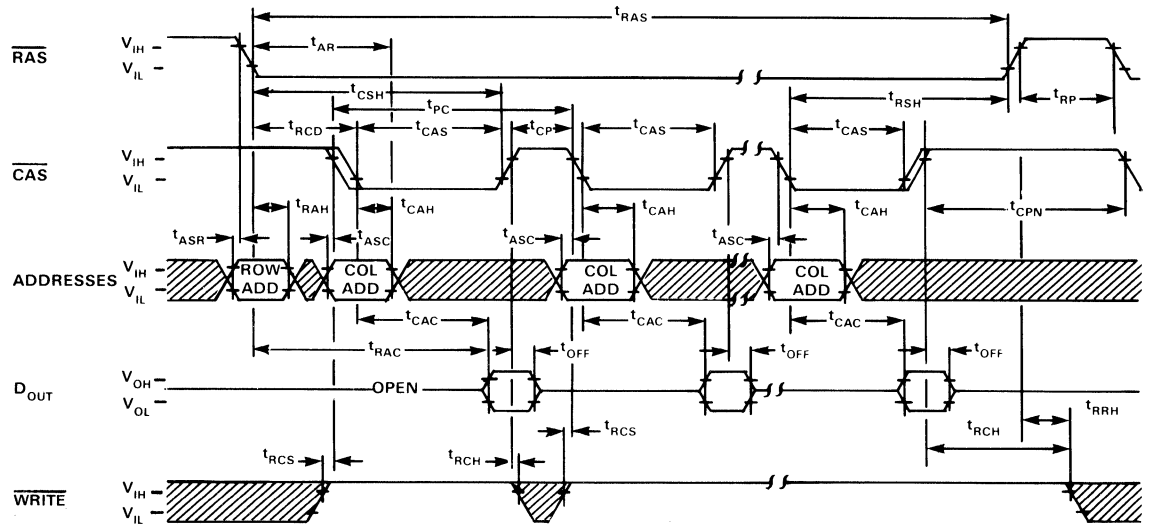
READ-WRITE/READ-MODIFY-WRITE CYCLE



"RAS-ONLY" REFRESH CYCLE

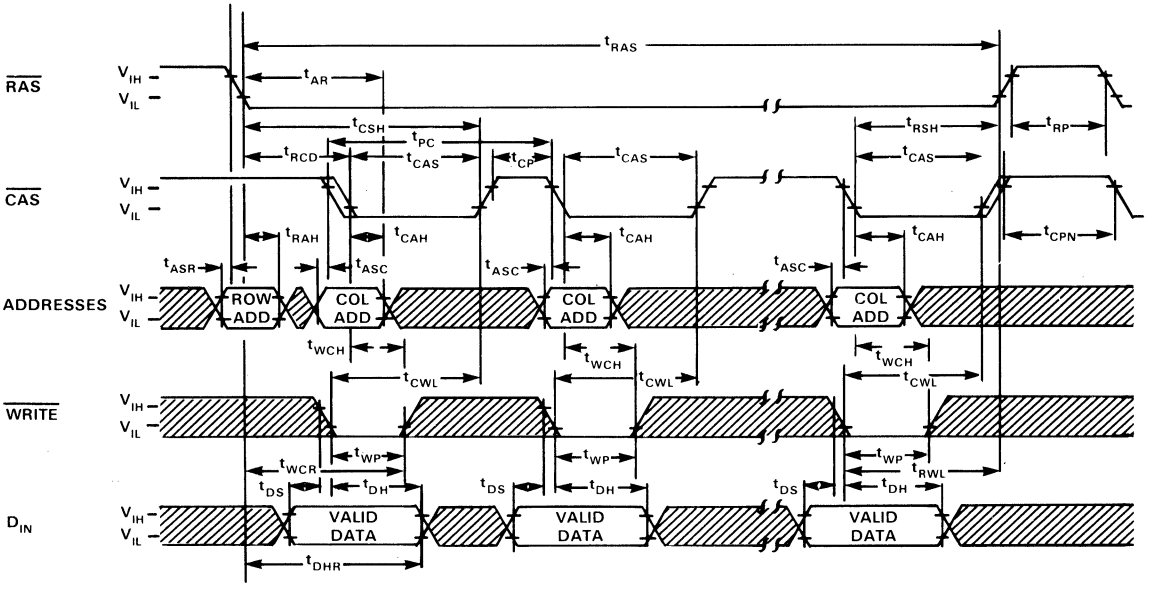


PAGE MODE READ CYCLE



IV

PAGE MODE WRITE CYCLE



OPERATION

The MK4528 consists of two 64K (MK4564) dynamic RAMs connected by a substrate in a 131,072 x 1 configuration.The eight address bits required to decode 1 of the 65,536 cell locations within each MK4564 are multiplexed onto the eight address inputs and latched into the on-chip address latches by externally applying two negative going TTL-level clocks. The first clock, Row Address Strobe ($\overline{RAS}$), latches the eight row addresses into the cip. The high-to-low transition of the second clock, Column Address Strobe ($\overline{CAS}$), subsequently latches the eight column addresses into the chip. Each of these signals, $\overline{RAS}$ and $\overline{CAS}$, triggers a sequence of events which are controlled by different delayed internal clocks. The two clock chains are linked together logically in such a way that the address multiplexing operation is done outside of the critical timing path for read data access. The later events in the $\overline{CAS}$ clock sequence are inhibited until the occurrence of a delayed signal derived from the $\overline{RAS}$ clock chain. This "gated $\overline{CAS}$" feature allows the $\overline{CAS}$ clock to be externally activated as soon as the Row Address Hold specification (t_{RAH}) has been satisfied and the address inputs have been changed from Row address to Column address information.

The "gated $\overline{CAS}$" feature permits $\overline{CAS}$ to be activated at any time after t_{RAH} and it will have no effect on the worst case data access time (t_{RAC}) up to the point in time when the delayed row clock no longer inhibits the remaining sequence of column clocks. Two timing endpoints result from the internal gating of $\overline{CAS}$ which are called t_{RCD} (min) and t_{RCD} (max). No data storage or reading errors will result if $\overline{CAS}$ is applied to the MK4564 at a point in time beyond the t_{RCD} (max) limit. However, access time will then be determined exclusively by the access time from $\overline{CAS}$ (t_{CAC}) rather than from $\overline{RAS}$ (t_{RAC}), and $\overline{RAS}$ access time will be lengthened by the amount that t_{RCD} exceeds the t_{RCD} (max) limit.

DATA INPUT/OUTPUT

Data to be written into a selected cell is latched into an on-chip register by a combination of $\overline{WRITE}$ and $\overline{CAS}$ while $\overline{RAS}$ is active. The latter of $\overline{WRITE}$ or $\overline{CAS}$ to make its negative transition is the strobe for the Data In (D_{IN}) register. This permits several options in the write cycle timing. In a write cycle, if the $\overline{WRITE}$ input is brought low (active) prior to $\overline{CAS}$ being brought low (active), the D_{IN} is strobed by $\overline{CAS}$, and the Input Data set-up and hold times are referenced to $\overline{CAS}$. If the input data is not available at $\overline{CAS}$ time (late write) or if it is desired that the cycle be a read-write or read-modify-write cycle the $\overline{WRITE}$ signal should be delayed until after $\overline{CAS}$ has made its negative transition. In this "delayed write cycle" the data input set-up and hold times are referenced to the negative edge of $\overline{WRITE}$ rather than $\overline{CAS}$.

Data is retrieved from the memory in a read cycle by maintaining $\overline{WRITE}$ in the inactive or high state throughout the portion of the memory cycle in which both the $\overline{RAS}$ and $\overline{CAS}$ are low (active). Data read from the selected cell is available at the output port within the specified access time. The output data is the same polarity (not inverted) as the input data.

DATA OUTPUT CONTROL

The normal condition of the Data Output (D_{OUT}) of the MK4564 is the high impedance (open-circuit) state; anytime $\overline{CAS}$ is high (inactive) the D_{OUT} pin will be floating. Once the output data port has gone active, it will remain valid until $\overline{CAS}$ is taken to the precharge (inactive high) state.

PAGE MODE OPERATION

The Page Mode feature of the MK4564 allows for successive memory operations at multiple column locations within the same row address. This is done by strobing the row address into the chip and maintaining the $\overline{RAS}$ signal low (active) throughout all successive memory cycles in which the row address is common. The first access within a page mode operation will be available at t_{RAC} or t_{CAC} time, whichever is the limiting parameter. However, all successive accesses within the page mode operation will be available at t_{CAC} time (referenced to $\overline{CAS}$). With the MK4564 this results in approximately a 57% improvement in access times. Effective memory cycle times are also reduced when using page mode.

The page mode boundary of a single MK4564 is limited to the 256 column locations determined by all combinations of the eight column address bits. Operations within the page boundary need not be sequentially addressed and any combination of read, write, and read-modify-write cycles is permitted within the page mode operation.

REFRESH

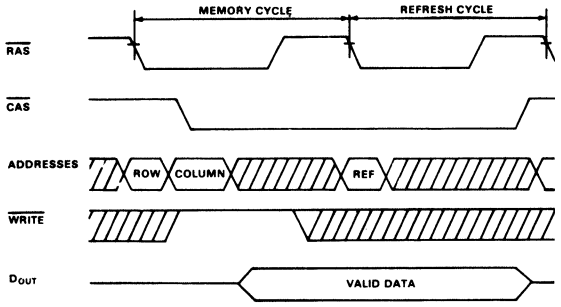
Refresh of the dynamic cell matrix is accomplished by performing a memory cycle at each of the 128 row addresses within each 2 ms interval. Although any normal memory cycle will perform the required refreshing, this function is most easily accomplished with "$\overline{RAS}$-only" cycles.

The $\overline{RAS}$-only refresh cycle requires that a 7 bit refresh address (A0-A6) be valid at the device address inputs when $\overline{RAS}$ goes low (active). The state of the output data port during a $\overline{RAS}$-only refresh is controlled by $\overline{CAS}$. If $\overline{CAS}$ is high (inactive) during the entire time that $\overline{RAS}$ is asserted, the output will remain in the high impedance state. If $\overline{CAS}$ is low (active) the entire time the $\overline{RAS}$ is asserted, the output port will remain in the same state that it was prior to the issuance of the $\overline{RAS}$ signal. If $\overline{CAS}$ makes a low-to-high transition during the $\overline{RAS}$-only refresh cycle, the output data buffer will assume the high impedance state. However, the $\overline{CAS}$ may not make a high to low transition during the $\overline{RAS}$-only refresh cycle since the device interprets this as a normal $\overline{RAS}/\overline{CAS}$ (read or write) type cycle.

HIDDEN REFRESH

A $\overline{RAS}$-only refresh cycle may take place while maintaining valid output data by extending the $\overline{CAS}$ active time from a previous memory read cycle. This feature is referred to as a hidden refresh. (See figure below.)

HIDDEN REFRESH CYCLE (SEE NOTE 19)



MOSTEK®

32,768 x 1-BIT DYNAMIC RAM

MK4332(D)-3

IV

FEATURES

- ☐ Utilizes two industry standard MK 4116 devices in an 18-pin package configuration
- ☐ 200ns access time, 375ns cycle (MK 4116-3)
- ☐ Separate $\overline{RAS}$, $\overline{CAS}$ Clocks
- ☐ ± 10% tolerance on all power supplies (+12V,±5V)
- ☐ Low power: 482mW active, 40mW standby (max)
- ☐ Output data controlled by $\overline{CAS}$ and unlatched at end of cycle to allow two dimensional chip selection and extended page boundary
- ☐ Common I/O capability using "early write" operation
- ☐ Read-Modify-Write, $\overline{RAS}$-only refresh, and Page-mode capability
- ☐ All inputs TTL compatible,low capacitance, and protected against static charge
- ☐ 128 refresh cycles for each MK 4116 device in the dual density configuration
- ☐ Pin compatible to MK 4116 and MK 4164

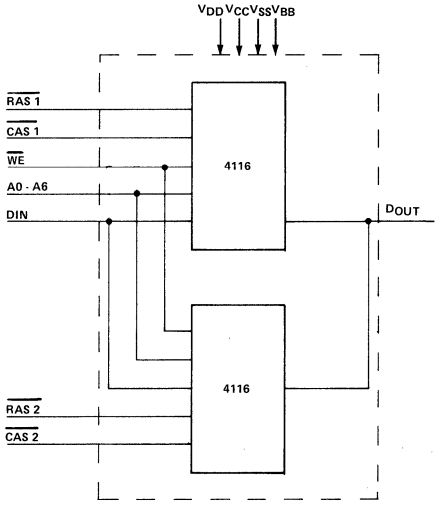
DESCRIPTION

The MK 4332 is a new generation MOS dynamic random access memory circuit organized as 32,768 words by 1 bit. As a state-of-the-art MOS memory device, the MK4332 (32K RAM) incorporates advanced circuit techniques designed to provide wide operating margins, both internally and to the system user

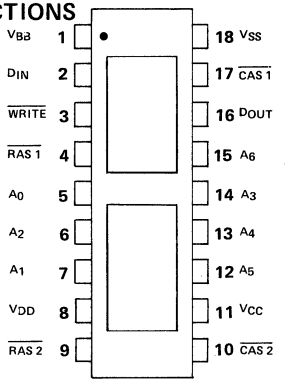
The technology used to fabricate the MK 4332 is MOSTEK's double-poly, N-channel silicon gate, POLY II™ process. This process, coupled with the use of a single transistor dynamic storage cell, provides the maximum possible circuit density and reliability, while maintaining high performance capability. The use of dynamic circuitry throughout, including sense amplifiers, assures that power dissipation is minimized without any sacrifice in speed or operating margin. These factors combine to make the MK 4332 a truly superior RAM product.

Multiplexed address inputs (a feature pioneered by MOSTEK for its 4K RAMS) permits the MK 4332 to be packaged in a standard 18-pin DIP. This standard package configuration, is compatible with widely available automated testing and insertion equipment, and it provides the highest possible system bit densities and simplifies system upgrade from 16K to 64K RAMs for new generation applications. Non-critical clock timing requirements allow use of the multiplexing technique while maintaining high performance.

FUNCTIONAL DIAGRAM



PIN CONNECTIONS



PIN NAMES

A_0-A_6	ADDRESS INPUTS
$\overline{CAS}$	COLUMN ADDRESS STROBE
D_{IN}	DATA IN
D_{OUT}	DATA OUT
$\overline{RAS}$	ROW ADDRESS STROBE
$\overline{WRITE}$	READ/WRITE INPUT
V_{BB}	POWER (−5V)
V_{CC}	POWER (+5V)
V_{DD}	POWER (+12V)
V_{SS}	GROUND

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to V_{BB} ..... −0.5V to +20V
Voltage on V_{DD}, V_{CC} supplies relative to V_{SS} ..... −1.0V to +15.0V
$V_{BB}-V_{SS}$ ($V_{DD}-V_{SS}>0V$) 0V
Operating temperature, T_A (Ambient) ..... 0°C to + 70°C
Storage temperature (Ambient) ..... −65°C to + 150°C
Short circuit output current 50mA
Power dissipation ..... 1 Watt

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS[6]

($0°C \leq T_A \leq 70°C$)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{DD} V_{CC} V_{SS} V_{BB}	10.8 4.5 0 −4.5	12.0 5.0 0 −5.0	13.2 5.5 0 −5.7	Volts Volts Volts Volts	2 2,3 2 2
Input High (Logic 1) Voltage, $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	V_{IHC}	2.4	–	7.0	Volts	2
Input High (Logic 1) Voltage, all inputs except $\overline{RAS}$, $\overline{CAS}$ $\overline{WRITE}$	V_{IH}	2.2	–	7.0	Volts	2
Input Low (Logic 0) Voltage, all inputs	V_{IL}	−1.0	–	.8	Volts	2

DC ELECTRICAL CHARACTERISTICS

($0°C \leq T_A \leq 70°C$) (V_{DD} = 12.0V ±10%; V_{CC} = 5.0V ±10%; −5.7V ≤ V_{BB} ≤ −4.5V; V_{SS} = 0V)

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
OPERATING CURRENT Average power supply operating current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = t_{RC} Min)	I_{DD1} I_{CC1} I_{BB1}		36.5 300	mA µA	4,19 5 19
STANDBY CURRENT Power supply standby current ($\overline{RAS}$ = V_{IHC}, D_{OUT} = High Impedance)	I_{DD2} I_{CC2} I_{BB2}	 −20 	3.0 20 200	mA µA µA	
REFRESH CURRENT Average power supply current, refresh mode ($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IHC}; t_{RC} = t_{RC} Min)	I_{DD3} I_{CC3} I_{BB3}	 −20 	26.5 20 300	mA µA µA	4, 19 19
PAGE MODE CURRENT Average power supply current, page-mode operation ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling; t_{PC} = t_{PC} Min)	I_{DD4} I_{CC4} I_{BB4}		28.5 300	mA µA	4,19 5 19
INPUT LEAKAGE Input leakage current, any input (V_{BB} = −5V, 0V ≤ V_{IN} ≤ +7.0V, all other pins not under test = 0 volts)	$I_{I(L)}$	−20	20	µA	
OUTPUT LEAKAGE Output leakage current (D_{OUT} is disabled, 0V ≤ V_{OUT} ≤ +5.5V)	$I_{O(L)}$	−20	20	µA	
OUTPUT LEVELS Output high (Logic 1) voltage (I_{OUT} = −5mA) Output low (Logic 0) voltage (I_{OUT} = 4.2 mA)	V_{OH} V_{OL}	2.4 	 0.4	Volts Volts	3

NOTES:

1. T_A is specified here for operation at frequencies to $t_{RC} \geq t_{RC}$ (min). Operation at higher cycle rates with reduced ambient temperatures and higher power dissipation is permissible, however, provided AC operating parameters are met. See figure 1 for derating curve.
2. All voltages referenced to V_{SS}.
3. Output voltage will swing from V_{SS} to V_{CC} when activated with no current loading. For purposes of maintaining data in standby mode, V_{CC} may be reduced to V_{SS} without affecting refresh operations or data retention. However, the V_{OH} (min) specification is not guaranteed in this mode.
4. I_{DD1}, I_{DD3}, and I_{DD4} depend on cycle rate. See figures 2,3, and 4 for I_{DD} limits at other cycle rates.
5. I_{CC1} and I_{CC4} depend upon output loading. During readout of high level data V_{CC} is connected through a low impedance (135 Ω typ) to data out. At all other times I_{CC} consists of leakage currents only.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (6,7,8)

($0\,°C \leq T_A \leq 70°C$)[1] (V_{DD} = 12.0V ±10%; V_{CC} = 5.0V ±10%, V_{SS} = 0V, -5.7V≤ V_{BB} ≤ -4.5V)

PARAMETER	SYMBOL	MK 4332 MIN	MK 4332 MAX	UNITS	NOTES
Random read or write cycle time	t_{RC}	375		ns	9
Read-write cycle time	t_{RWC}	375		ns	9
Read modify write cycle time	t_{RMW}	405		ns	9
Page mode cycle time	t_{PC}	225		ns	9
Access time from $\overline{RAS}$	t_{RAC}		200	ns	10,12
Access time from $\overline{CAS}$	t_{CAC}		135	ns	11,12
Output buffer turn-off delay	t_{OFF}	0	50	ns	13
Transition time (rise and fall)	t_T	3	50	ns	8
$\overline{RAS}$ precharge time	t_{RP}	120		ns	
$\overline{RAS}$ pulse width	t_{RAS}	200	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	135		ns	
$\overline{CAS}$ hold time	t_{CSH}	200		ns	
$\overline{CAS}$ pulse width	t_{CAS}	135	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	25	65	ns	14
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	–20		ns	
Row Address set-up time	t_{ASR}	0		ns	
Row Address hold time	t_{RAH}	25		ns	
Column Address set-up time	t_{ASC}	–10		ns	
Column Address hold time	t_{CAH}	55		ns	
Column Address hold time referenced to $\overline{RAS}$	t_{AR}	120		ns	
Read command set-up time	t_{RCS}	0		ns	
Read command hold time	t_{RCH}	0		ns	
Write command hold time	t_{WCH}	55		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	120		ns	
Write command pulse width	t_{WP}	55		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	70		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	70		ns	
Data-in set-up time	t_{DS}	0		ns	15
Data-in hold time	t_{DH}	55		ns	15
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	120		ns	
$\overline{CAS}$ precharge time (for page-mode cycle only)	t_{CP}	80		ns	
Refresh period	t_{REF}		2	ms	
$\overline{WRITE}$ command set-up time	t_{WCS}	–20		ns	16
$\overline{CAS}$ to $\overline{WRITE}$ delay	t_{CWD}	80		ns	16
$\overline{RAS}$ to $\overline{WRITE}$ delay	t_{RWD}	145		ns	16

NOTES (Continued)

6. Several cycles are required after power-up before proper device operation is achieved. Any 8 cycles which perform refresh are adequate for this purpose.
7. AC measurements assume t_T = 5ns.
8. V_{IHC} (min) or V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IHC} or V_{IH} and V_{IL}.
9. The specifications for t_{RC} (min) t_{RMW} (min) and t_{RWC} (min) are used only to indicate cycle time at which proper operation over the full temperature range ($0\,°C \leq T_A \leq 70°C$) is assured.
10. Assumes that $t_{RCD} \leq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
11. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
12. Measured with a load equivalent to 2 TTL loads and 100pF.
13. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
14. Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
15. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in delayed write or read-modify-write cycles.
16. t_{WCS}, t_{CWD} and t_{RWD} are restrictive operating parameters in read write and read modify write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; If $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min), the cycle is a read-write cycle and the data out will contain data read from the selected cell; If neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.
17. Effective capacitance calculated from the equation $C = \frac{I\Delta t}{\Delta V}$ with ΔV = 3 volts and power supplies at nominal levels.
18. $\overline{CAS}$ = V_{IHC} to disable D_{OUT}.
19. One 16K RAM is active while the other is in standby mode.

AC ELECTRICAL CHARACTERISTICS

(0°C ≤ T_A ≤ 70°C) (V_{DD} = 12.0V ± 10%; V_{SS} = 0V; −5.7V ≤ V_{BB} ≤ −4.5V)

PARAMETER	SYMBOL	TYP	MAX	UNITS	NOTES
Input Capacitance (A_0–A_6), D_{IN}	C_{I1}	8	10	pF	17
Input Capacitance $\overline{RAS}$, $\overline{CAS}$,	C_{I2}	8	10	pF	17
Output Capacitance (D_{OUT})	C_O	10	14	pF	17, 18
Input Capacitance $\overline{WRITE}$	C_{I3}	16	20	pF	17

AC Characteristics and Timing Diagrams of MK4116-3.

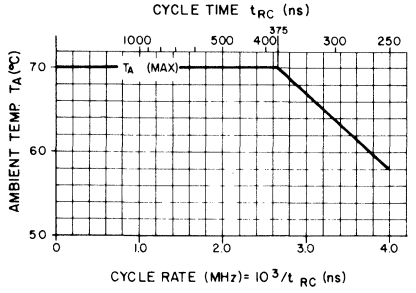


Fig. 1 Maximum ambient temperature versus cycle rate for extended frequency operation. T_A (max) for operation at cycling rates greater than 2.66 MHz (t_{CYC}<375ns) is determined by T_A (max)° C = 70–9.0 x (cycle rate MHz −2.66) for -3.

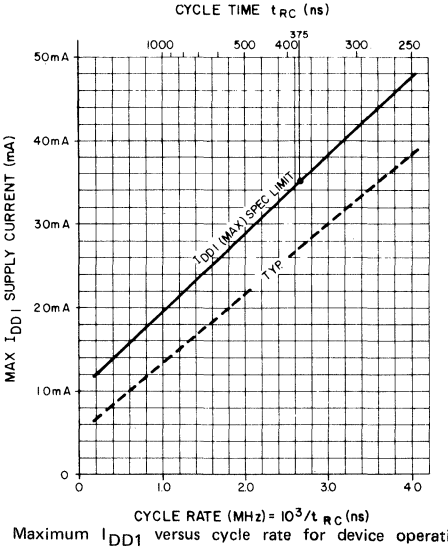


Fig. 2 Maximum I_{DD1} versus cycle rate for device operation at extended frequencies. I_{DD1} (max) curve is defined by the equation:

I_{DD1} (max) mA = 10 + 9.4 x cycle rate [MHz] for -3

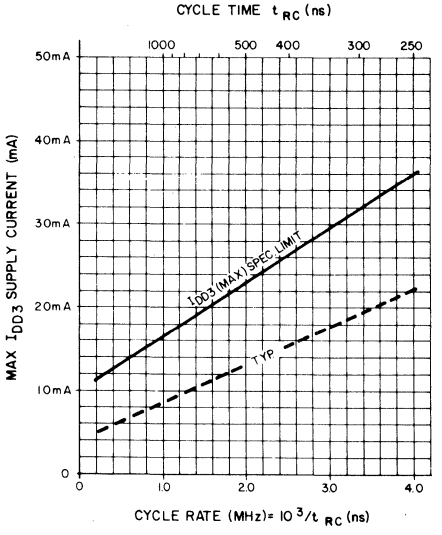


Fig. 3 Maximum I_{DD3} versus cycle rate for device operation at extended frequencies. I_{DD3} (max) curve is defined by the equation:

I_{DD3}(max) mA = 10 + 6.5 x cycle rate [MHz] for -3

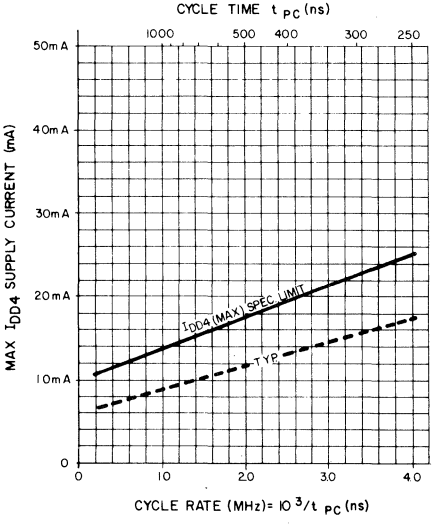
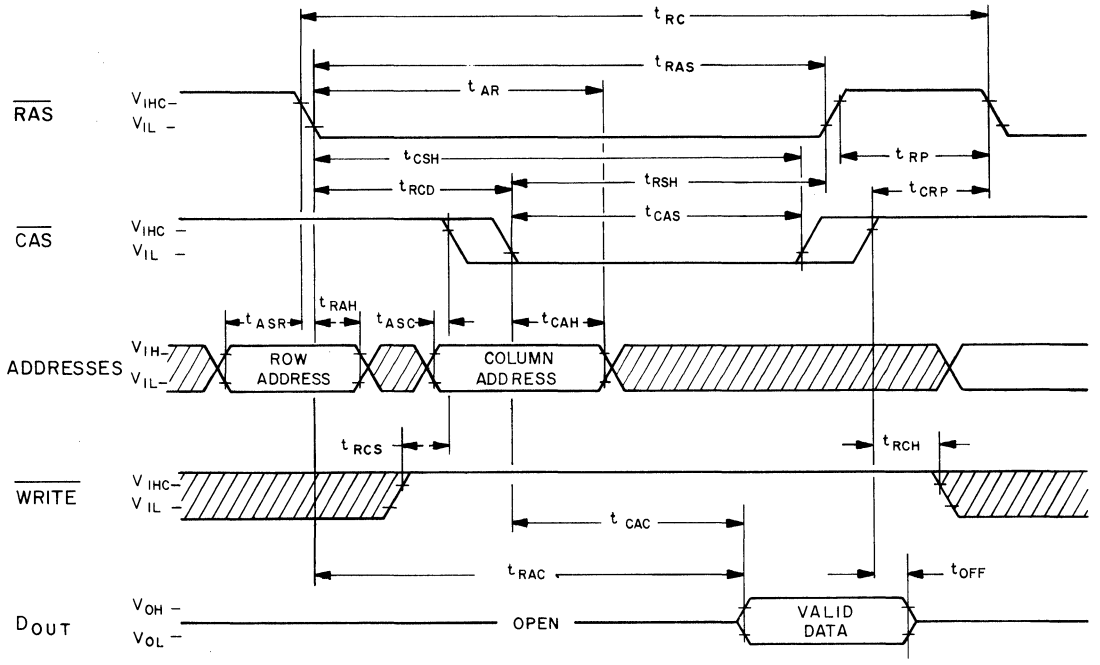


Fig. 4 Maximum I_{DD4} versus cycle rate for device operation in page mode. I_{DD4} (max) curve is defined by the equation:

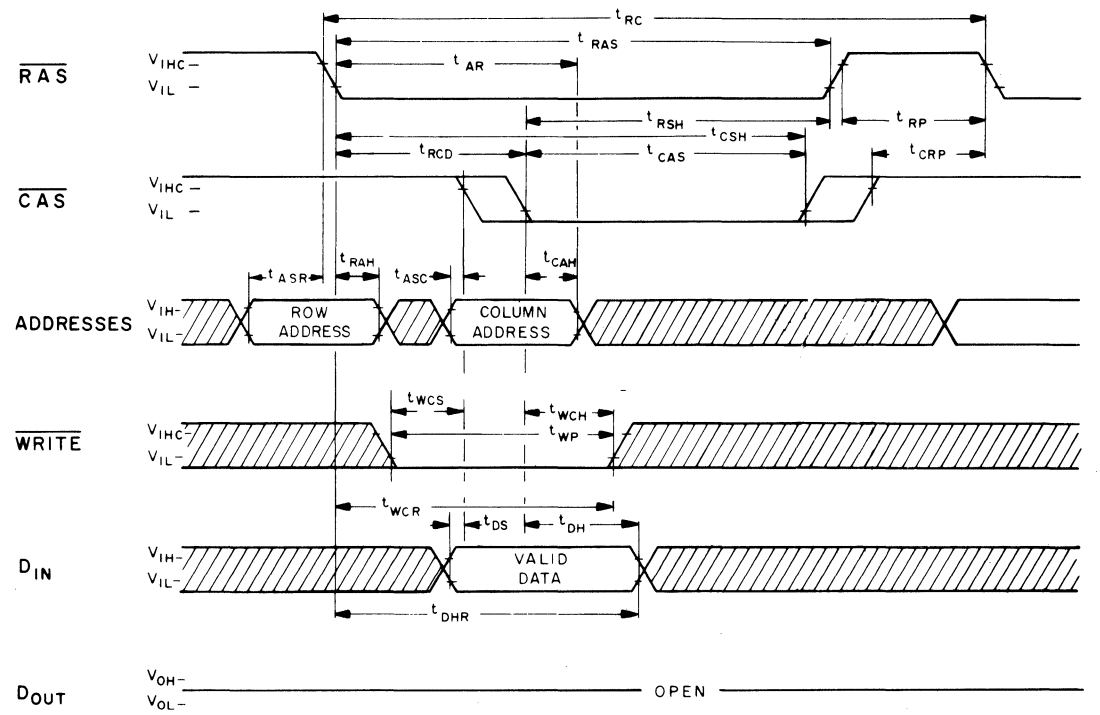
I_{DD4} (max) mA = 10 + 3.75 x cycle rate [MHz] for -3

READ CYCLE

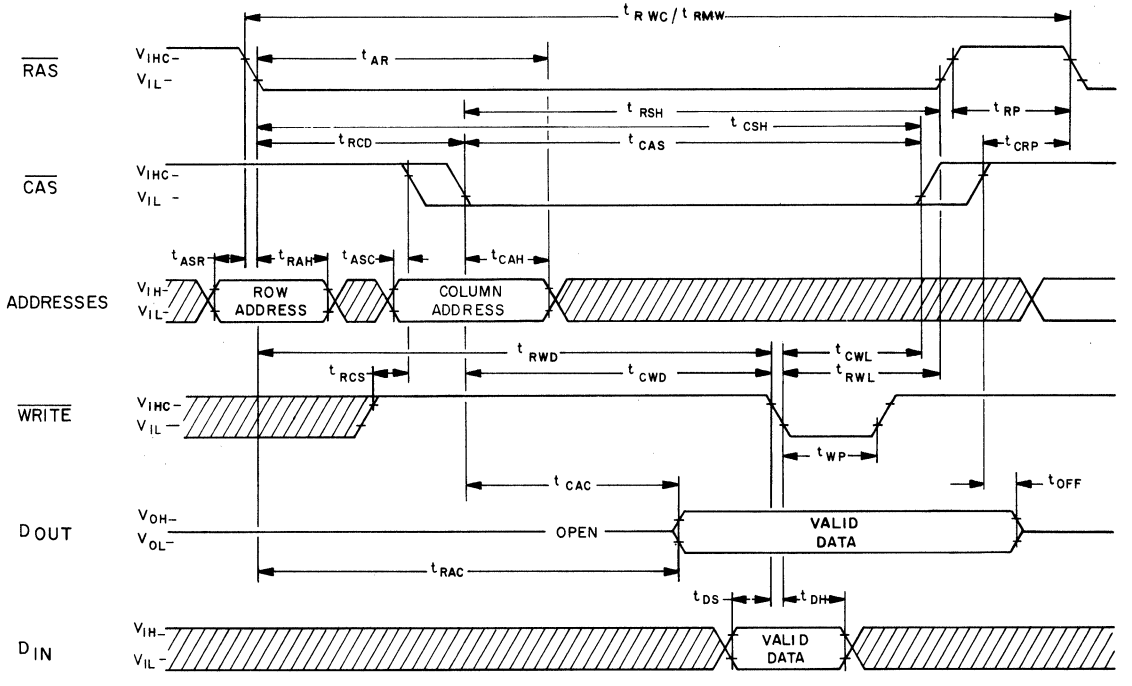


IV

WRITE CYCLE (EARLY WRITE)

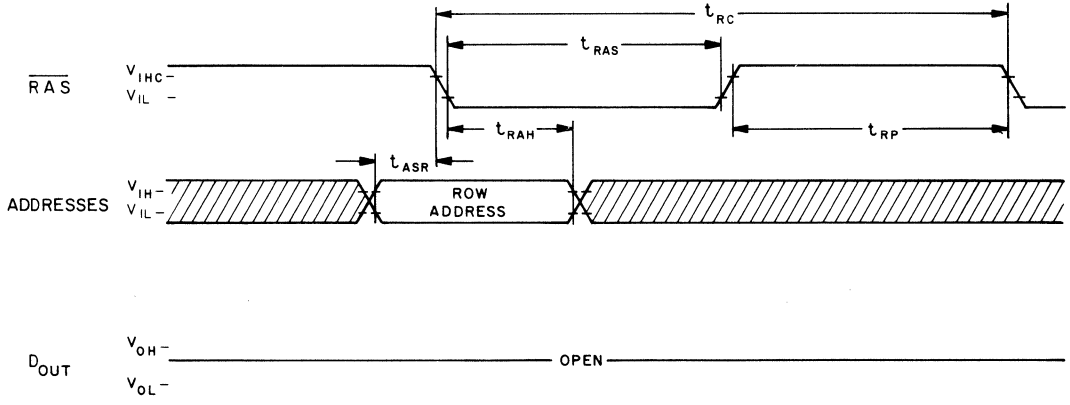


READ–WRITE/READ–MODIFY–WRITE CYCLE

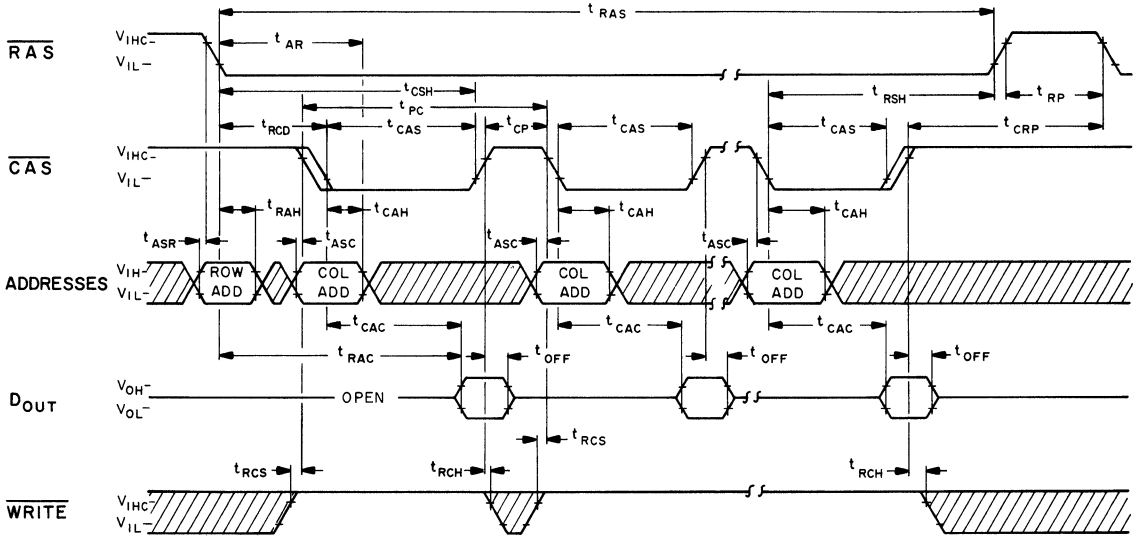


"RAS–ONLY" REFRESH CYCLE

NOTE: $\overline{CAS}$ = V_{IHC}, $\overline{WRITE}$ = Don't Care

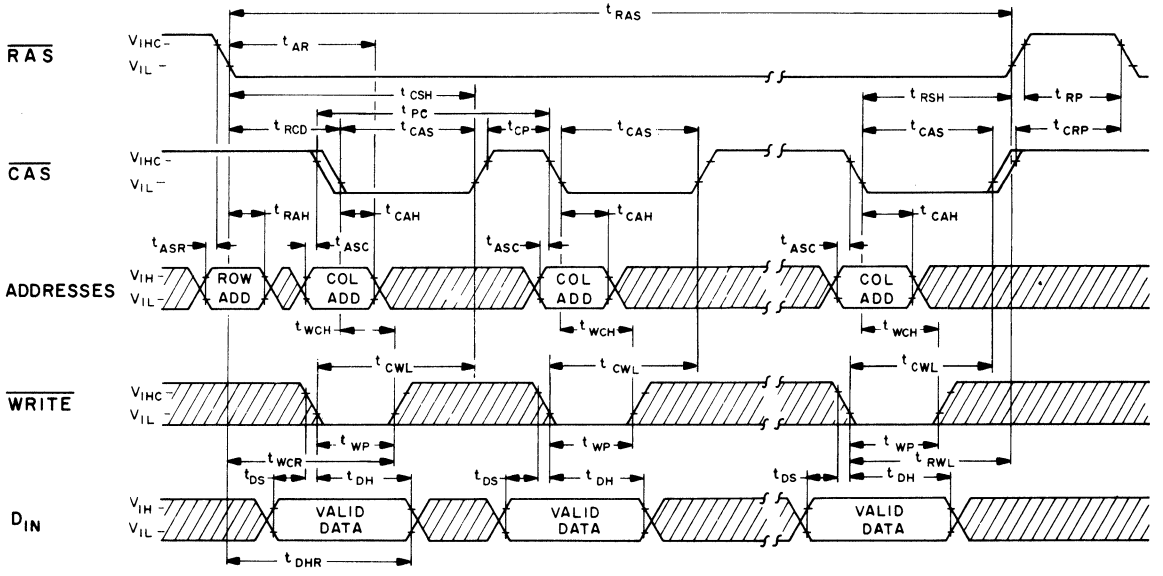


PAGE MODE READ CYCLE



IV

PAGE MODE WRITE CYCLE



DESCRIPTION (continued)

System oriented features include ± 10% tolerance on all power supplies, direct interfacing capability with high performance logic families such as Schottky TTL, maximum input noise immunity to minimize "false triggering" of the inputs (a common cause of soft errors), on-chip address and data registers which eliminate the need for interface registers, and two chip select methods. The MK 4332 also incorporates several flexible timing/operating modes. In addition to the usual read, write, and read-modify-write cycles, the MK 4332 is capable of delayed write cycles, page-mode operation and RAS-only refresh. Proper control of the clock inputs($\overline{RAS}$, $\overline{CAS}$ and $\overline{WRITE}$) allows common I/O capability, two dimensional chip selection, and extended page boundaries (when operating in page mode).

ADDRESSING

User access of a unique memory location is accomplished by multiplexing 14 address bits onto 7 address inputs and by proper control of the $\overline{RAS}$ and $\overline{CAS}$ clocks in a manner identical to operation of the MK 4116 in a memory array board. The 14 address bits required to decode 1 of the 16,384 cell locations within each MK 4116 are multiplexed onto the 7 address inputs and latched into the on-chip address latches by externally applying two negative going TTL-level clocks. The first clock, the Row Address Strobe ($\overline{RAS}$), latches the 7 row address bits into the chip. The second clock, the Column Address Strobe ($\overline{CAS}$), subsequently latches the 7 column address bits into the chip. Each of these signals, $\overline{RAS}$ and $\overline{CAS}$, triggers a sequence of events which are controlled by different delayed internal clocks. The two clock chains are linked together logically in such a way that the address multiplexing operation is done outside of the critical path timing sequence for read data access. The later events in the $\overline{CAS}$ clock sequence are inhibited until the occurence of a delayed signal derived from the $\overline{RAS}$ clock chain. This "gated $\overline{CAS}$" feature allows the $\overline{CAS}$ clock to be externally activated as soon as the Row Address Hold Time specification (t_{RAH}) has been satisfied and the address inputs have been changed from Row address to Column address information.

Note that $\overline{CAS}$ can be activated at any time after t_{RAH} and it will have no effect on the worst case data access time (t_{RAC}) up to the point in time when the delayed row clock no longer inhibits the remaining sequence of column clocks. Two timing endpoints result from the internal gating of $\overline{CAS}$ which are called t_{RCD} (min) and t_{RCD} (max). No data storage or reading errors will result if $\overline{CAS}$ is applied to the MK 4332 at a point in time beyond the t_{RCD} (max) limit. However, access time will then be determined exclusively by the access time from $\overline{CAS}$ (t_{CAC}) rather than from $\overline{RAS}$ (t_{RAC}), and access time from $\overline{RAS}$ will be lengthened by the amount that t_{RCD} exceeds the t_{RCD} (max) limit.

DATA INPUT/OUTPUT

Data to be written into a selected cell is latched into an on-chip register by a combination of $\overline{WRITE}$ and $\overline{CAS}$ while $\overline{RAS}$ is active. The later of the signals ($\overline{WRITE}$ or $\overline{CAS}$) to make its negative transition is the strobe for the Data In (D_{IN}) register. This permits several options in the write cycle timing. In a write cycle, if the $\overline{WRITE}$ input is brought low (active) prior to $\overline{CAS}$, the D_{IN} is strobed by $\overline{CAS}$, and the set-up and hold times are referenced to $\overline{CAS}$. If the input data is not available at $\overline{CAS}$ time or if it is desired that the cycle be a read-write cycle, the $\overline{WRITE}$ signal will be delayed until after $\overline{CAS}$ has made its negative transition. In this "delayed write cycle" the data input set-up and hold times are referenced to the negative edge of $\overline{WRITE}$ rather than $\overline{CAS}$. (To illustrate this feature, D_{IN} is referenced to $\overline{WRITE}$ in the timing diagrams depicting the read-write and page-mode write cycles while the "early write" cycle diagram shows D_{IN} referenced to $\overline{CAS}$).

Data is retrieved from the memory in a read cycle by maintaining $\overline{WRITE}$ in the inactive or high state throughout the portion of the memory cycle in which $\overline{CAS}$ is active (low). Data read from the selected cell will be available at the output within the specified access time.

DATA OUTPUT CONTROL

The normal condition of the Data Output (D_{OUT}) of the MK 4332 is the high impedance (open-circuit) state. That is to say, anytime $\overline{CAS}$ is at a high level, the D_{OUT} pin will be floating. The only time the output will turn on and contain either a logic 0 or logic 1 is at access time during a read cycle. D_{OUT} will remain valid from access time until $\overline{CAS}$ is taken back to the inactive (high level) condition.

Since the outputs to both 16K devices are tied together, care must be taken with the timing relationships of the two devices. Both devices cannot be activated at the same time as a data output conflict can occur.

If the memory cycle in progress is a read, read-modify write, or a delayed write cycle, then the data output will go from the high impedance state to the active condition, and at access time will contain the data read from the selected cell. This output data is the same polarity (not inverted) as the input data. Once having gone active, the output will remain valid until $\overline{CAS}$ is taken to the precharge (logic 1) state, whether or not $\overline{RAS}$ goes into precharge.

If the cycle in progress is an "early-write" cycle ($\overline{WRITE}$ active before $\overline{CAS}$ goes active), then the output pin will maintain the high impedance state throughout the entire cycle. Note that with this type of output configuration, the user is given full control of the D_{OUT} pin simply by controlling the placement of $\overline{WRITE}$ command during a write cycle, and the pulse width of the Column Address Strobe during read operations. Note also that even though data is not latched at the output, data can remain valid from access time until the beginning of a subsequent cycle without paying any penalty in overall memory cycle time (stretching the cycle).

This type of output operation results in some very significant system implications.

Common I/O Operation – If all write operations are handled in the "early write" mode, then D_{IN} can be connected directly to D_{OUT} for a common I/O data bus.

Data Output Control – D_{OUT} will remain valid during a read cycle from t_{CAC} until $\overline{CAS}$ goes back to a high level (precharge), allowing data to be valid from one cycle up until a new memory cycle begins

with no penalty in cycle time. This also makes the $\overline{RAS}/\overline{CAS}$ clock timing relationship very flexible.

Two Methods of Chip Selection – Since D_{OUT} is not latched, $\overline{CAS}$ is not required to turn off the outputs of unselected memory devices in a matrix. This means that both $\overline{CAS}$ and/or $\overline{RAS}$ can be decoded for chip selection. If both $\overline{RAS}$ and $\overline{CAS}$ are decoded, then a two dimensional (X,Y) chip select array can be realized.

Extended Page Boundary – Page-mode operation allows for successive memory cycles at multiple column locations of the same row address. By decoding $\overline{CAS}$ as a page cycle select signal, the page boundary can be extended beyond the 128 column locations in a single chip. (See page-mode operation).

OUTPUT INTERFACE CHARACTERISTICS

The three state data output buffer presents the data output pin with a low impedance to V_{CC} for a logic 1 and a low impedance to V_{SS} for a logic 0. The effective resistance to V_{CC} (logic 1 state) is 420 Ω maximum and 135Ω typically. The resistance to V_{SS} (logic 0 state) is 95 Ω maximum and 35 Ω typically. The separate V_{CC} pin allows the output buffer to be powered from the supply voltage of the logic to which the chip is interfaced. During battery standby operation, the V_{CC} pin may have power removed without affecting the MK 4332 refresh operation. This allows all system logic except the $\overline{RAS}$ timing circuitry and the refresh address logic to be turned off during battery standby to conserve power.

PAGE MODE OPERATION

The "Page Mode" feature of the MK 4332 allows for successive memory operations at multiple column locations of the same row address with increased speed without an increase in power. This is done by strobing the row address into the chip and maintaining the $\overline{RAS}$ signal at a logic 0 throughout all successive memory cycles in which the row address is common. This "page-mode" of operation will not dissipate the power associated with the negative going edge of $\overline{RAS}$. Also, the time required for strobing in a new row address is eliminated, thereby decreasing the access and cycle times.

The page boundary of a single MK 4116 is limited to the 128 column locations determined by all combinations of the 7 column address bits. However, the page boundary of the MK4332 can be extended by using $\overline{CAS}$ rather than $\overline{RAS}$ as the chip select signal. $\overline{RAS}$ is applied to all devices to latch the row address into each device and then $\overline{CAS}$ is decoded and serves as a page cycle select signal. Only those devices which receive both $\overline{RAS}$ and $\overline{CAS}$ signals will execute a read or write cycle.

REFRESH

Refresh of the MK4116 is accomplished by performing a memory cycle at each of the 128 row addresses within each 2 millisecond time interval. Each MK4116 in the MK4332 Assembly must receive all 128 refresh cycles within the 2ms time interval in order to completely refresh all 32,768 memory cells.

Although any normal memory cycle will perform the refresh operation, this function is most easily accomplished with "$\overline{RAS}$-only" cycles. $\overline{RAS}$-only refresh resuls in a substantial reduction in operating power. This reduction in power is reflected in the I_{DD3} specification.

POWER CONSIDERATIONS

Most of the circuitry used in the MK 4332 is dynamic and most of the power drawn is the result of an address strobe edge. Consequently, the dynamic power is primarily a function of operating frequency rather than active duty cycle (refer to the MK 4116 current waveforms in figure 5). This current characteristic of the MK 4332 precludes inadvertent burn out of the device in the event that the clock inputs become shorted to ground due to system malfunction.

Although no particular power supply noise restriction exists other than the supply voltages remain within the specified tolerance limits, adequate decoupling should be provided to suppress high frequency noise resulting from the transient current of the device. This insures optimum system performance and reliability. Bulk capacitance requirements are minimal since the MK 4332 draws very little steady state (DC) current.

In system applications requiring lower power dissipation, the operating frequency (cycle rate) of the MK 4332 can be reduced and the (guaranteed maximum) average power dissipation of the device will be lowered in accordance with the I_{DD1} (max) spec limit curve illustrated in figure 2. NOTE: The MK 4332 family is guaranteed to have a maximum I_{DD1} requirement of 36.5mA @ 375ns cycle with an ambient temperature range from 0° to 70°C. A lower operating frequency, for example 1 microsecond cycle, results in a reduced maximum I_{DD1} requirement of under 20mA with an ambient temperature range from 0° to 70°C.

NOTE: Additional power supply tolerance has been included on the V_{BB} supply to allow direct interface capability with both –5V systems –5.2V ECL systems.

Fig. 5 Typical Current Waveforms for the MK 4116

Although $\overline{RAS}$ and/or $\overline{CAS}$ can be decoded and used as a chip select signal for the MK 4116, overall system power is minimized if the Row Address Strobe ($\overline{RAS}$) is used for this purpose. All unselected devices (those which do not receive a $\overline{RAS}$) will remain in a low power (standby) mode regardless of the state of $\overline{CAS}$.

POWER UP

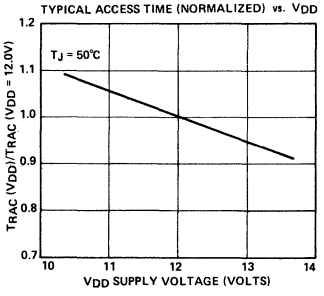
The MK 4332 requires no particular power supply sequencing so long as the Absolute Maximum Rating Conditions are observed. However, in order to insure compliance with the Absolute Maximum Ratings, MOSTEK recommends sequencing of power supplies such that V_{BB} is applied first and removed last. V_{BB} should never be more positive than V_{SS} when power is applied to V_{DD}.

Under system failure conditions in which one or more supplies exceed the specified limits significant additional margin against catastrophic device failure may be achieved by forcing $\overline{RAS}$ and $\overline{CAS}$ to the inactive state (high level).

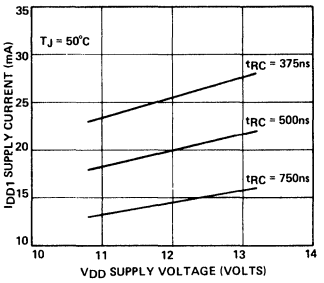
After power is applied to the device, the MK 4332 requires several cycles before proper device operation is achieved. Any 8 cycles which perform refresh are adequate for this purpose. Each MK 4116 device must receive the 8 initialization cycles.

TYPICAL CHARACTERISTICS OF THE MK 4116

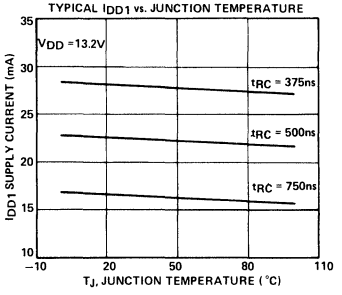
TYPICAL ACCESS TIME (NORMALIZED) vs. V_{DD}



TYPICAL I_{DD1} vs. V_{DD}

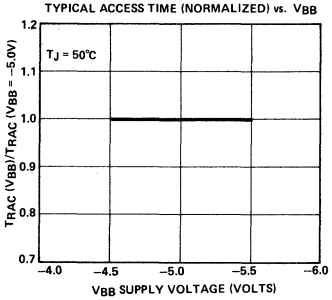


TYPICAL I_{DD1} vs. JUNCTION TEMPERATURE

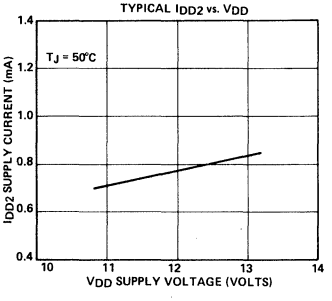


IV

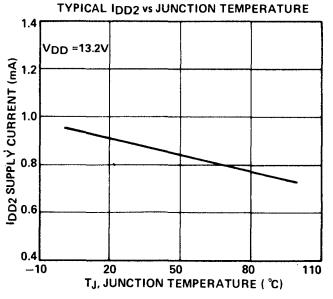
TYPICAL ACCESS TIME (NORMALIZED) vs. V_{BB}



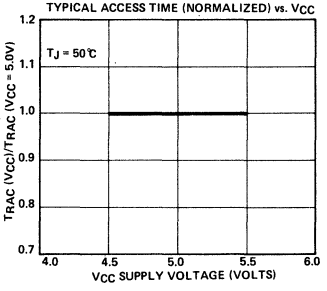
TYPICAL I_{DD2} vs. V_{DD}



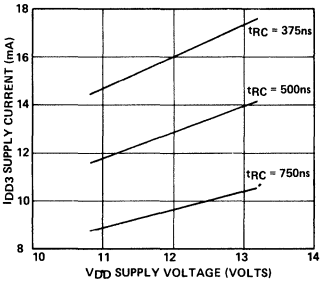
TYPICAL I_{DD2} vs JUNCTION TEMPERATURE



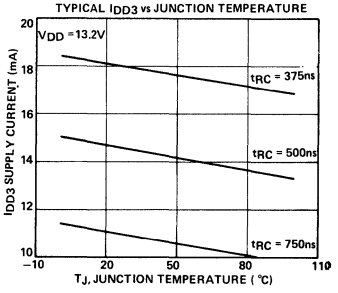
TYPICAL ACCESS TIME (NORMALIZED) vs. V_{CC}



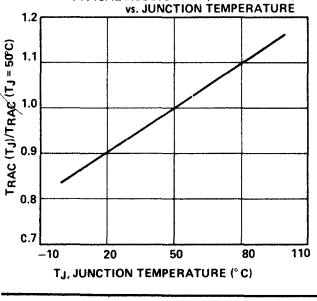
TYPICAL I_{DD3} vs. V_{DD}



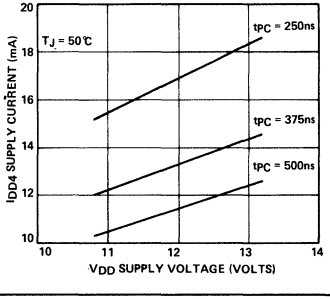
TYPICAL I_{DD3} vs JUNCTION TEMPERATURE



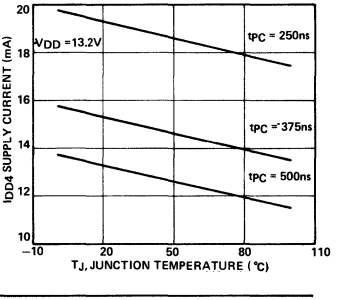
TYPICAL ACCESS TIME (NORMALIZED) vs. JUNCTION TEMPERATURE



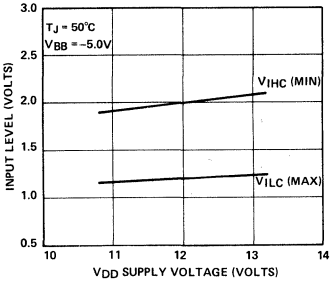
TYPICAL I_{DD4} vs VDD



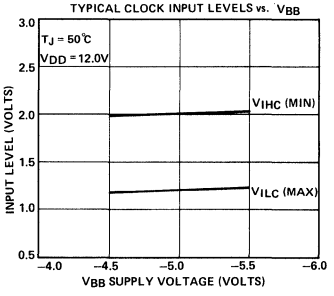
TYPICAL I_{DD4} vs. JUNCTION TEMPERATURE



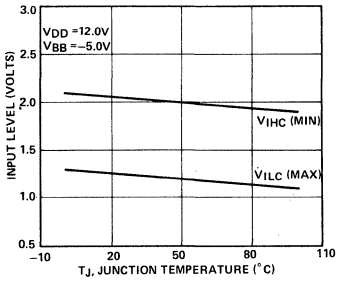
TYPICAL CLOCK INPUT LEVELS vs. V_{DD}



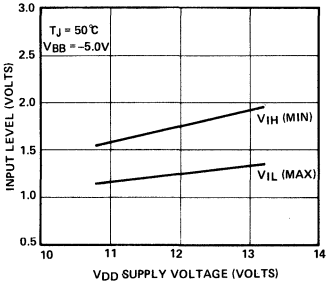
TYPICAL CLOCK INPUT LEVELS vs. V_{BB}



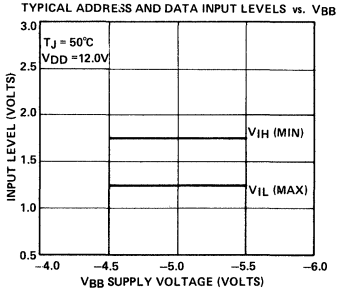
TYPICAL CLOCK INPUT LEVELS vs. T_J



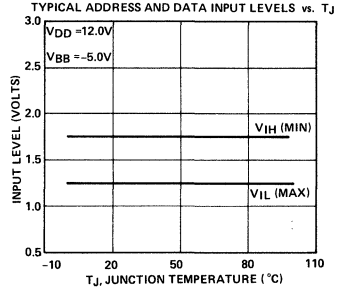
TYPICAL ADDRESS AND DATA INPUT LEVELS vs. V_{DD}



TYPICAL ADDRESS AND DATA INPUT LEVELS vs. V_{BB}



TYPICAL ADDRESS AND DATA INPUT LEVELS vs. T_J



PRELIMINARY

MOSTEK®

MEMORY COMPONENTS

65,536 x 1-Bit Dynamic RAM

MK4564(P/N/J)-15/20/25

IV

FEATURES

- Recognized industry standard 16-pin configuration from Mostek
- Single +5V (± 10%) supply operation
- On chip substrate bias generator for optimum performance
- Low power: 300 mW active, max
  22 mW standby, max
- 150 ns access time, 260 ns cycle time (MK4564-15)
  200 ns access time, 345 ns cycle time (MK4564-20)
  250 ns access time, 425 ns cycle time (MK4564-25)
- Extended D_{OUT} hold using $\overline{CAS}$ control (Hidden Refresh)
- Common I/O capability using "early write"
- Read, Write, Read-Write, Read-Modify-Write and Page-Mode capability
- All inputs TTL compatible, low capacitance, and protected against static charge
- Scaled POLY 5™ technology
- 128 refresh cycles (2 msec)
  Pin 9 is not needed for refresh
- MKB version screened to MIL-STD-883

DESCRIPTION

The MK4564 is the new generation dynamic RAM. Organized 65,536 words by 1 bit, it is the successor to the industry standard MK4116. The MK4564 utilizes Mostek's Scaled POLY 5 process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user. The use of dynamic circuitry throughout, including the 512 sense amplifiers, assures that power dissipation is minimized without any sacrifice in speed or internal and external operating margins. Refresh characteristics have been chosen to maximize yield (low cost to user) while maintaining compatibility between dynamic RAM generations.

Multiplexed address inputs (a feature dating back to the industry standard MK4096, 1973) permit the MK4564 to be packaged in a standard 16-pin DIP with only 15 pins required for basic functionality. The MK4564 is designed to be compatible with the JEDEC standards for the 64K x 1 dynamic RAM.

The output of the MK4564 can be held valid up to 10 μsec by holding $\overline{CAS}$ active low. This is quite useful since refresh cycles can be performed while holding data valid from a previous cycle. This feature is referred to as Hidden Refresh.

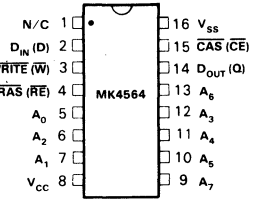
The 64K RAM from Mostek is the culmination of several years of circuit and process development, proven in predecessor products.

PIN FUNCTIONS

A_0-A_7	Address Inputs	$\overline{RAS}$ ($\overline{RE}$)	Row Address Strobe
$\overline{CAS}$ ($\overline{CE}$)	Column Address Strobe	$\overline{WRITE}$ ($\overline{W}$)	Read/ Write Input
D_{IN} (D)	Data In	V_{CC}	Power (5V)
D_{OUT} (Q)	Data Out	V_{SS}	GND
		N/C	Not Connected

PIN OUT

DUAL-IN-LINE PACKAGE



Available soon in MIL-STD-883 Class B (MKB).

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0 V to +7.0 V
Operating Temperature, T_A (Ambient) ..... 0°C to +70C
Storage Temperature (Ceramic) ..... -65°C to +150°C
Storage Temperature (Plastic) ..... -55°C to +125°C
Power Dissipation ..... 1 Watt
Short Circuit Output Current ..... 50 mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

($0°C \leq T_A \leq 70°C$)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	1
V_{IH}	Input High (Logic 1) Voltage, All Inputs	2.4	—	V_{CC}+1	V	1
V_{IL}	Input Low (Logic 0) Voltage, All Inputs	-2.0	—	.8	V	1,18

DC ELECTRICAL CHARACTERISTICS

($0°C \leq T_A \leq 70°C$) (V_{CC} = 5.0 V ± 10%)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC1}	OPERATING CURRENT Average power supply operating current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = t_{RC} min.)		54.0	mA	2
I_{CC2}	STANDBY CURRENT Power supply standby current ($\overline{RAS}$ = V_{IH}, D_{OUT} = High Impedance)		4	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average power supply current, refresh mode ($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}; t_{RC} = t_{RC} min.)		45	mA	2
I_{CC4}	PAGE MODE CURRENT Average power supply current, page mode operation ($\overline{RAS}$ = V_{IL}, t_{RAS} = t_{RAS} max., $\overline{CAS}$ cycling; t_{PC} = t_{PC} min.)		35	mA	2
$I_{I(L)}$	INPUT LEAKAGE Input leakage current, any input ($0 V \leq V_{IN} \leq V_{CC}$), all other pins not under test = 0 V	-10	10	µA	
$I_{O(L)}$	OUTPUT LEAKAGE Output leakage current (D_{OUT} is disabled, $0 V \leq V_{OUT} \leq V_{CC}$)	-10	10	µA	
V_{OH} V_{OL}	OUTPUT LEVELS Output High (Logic 1) voltage (I_{OUT} = -5 mA) Output Low (Logic 0) voltage (I_{OUT} = 4.2 mA)	2.4	 0.4	V V	

NOTES:

1. All voltages referenced to V_{SS}.
2. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open.
3. An initial pause of 500 μs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved. Note that $\overline{RAS}$ may be cycled during the initial pause.
4. AC characteristics assume t_T = 5 ns.
5. V_{IH} min. and V_{IL} max. are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C $\leq T_A \leq$ 70°C) is assured.
7. Load = 2 TTL loads and 50 pF.
8. Assumes that $t_{RCD} \leq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
9. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
10. t_{OFF} max defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
11. Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
12. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
13. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in delayed write or read-modify-write cycles.
14. t_{WCS}, t_{CWD}, and t_{RWD} are restrictive operating parameters in READ/WRITE and READ/MODIFY/WRITE cycles only. If $t_{WCS} \geq t_{WCS}$ (min) the cycle is an EARLY WRITE cycle and the data output will remain open circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min) the cycle is a READ/WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met the condition of the data out (at access time and until $\overline{CAS}$ goes back to V_{IH}) is indeterminate.
15. In addition to meeting the transition rate specification, all input signals must transmit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
16. Effective capacitance calculated from the equation $C = I \frac{\Delta t}{\Delta V}$ with ΔV = 3 volts and power supply at nominal level.
17. $\overline{CAS}$ = V_{IH} to disable D_{OUT}.
18. Includes the DC level and all instantaneous signal excursions.
19. $\overline{WRITE}$ = don't care. Data out depends on the state of $\overline{CAS}$. If $\overline{CAS}$ = V_{IH}, data output is high impedance. If $\overline{CAS}$ = V_{IL}, the data output will contain data from the last valid read cycle.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(3,4,5,15) (0°C $\leq T_A \leq$ 70°C), V_{CC} = 5.0 V ± 10%

SYMBOL			MK4564-15		MK4564-20		MK4564-25			
STD	ALT	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
t_{RELREL}	t_{RC}	Random read or write cycle time	260		345		425		ns	6,7
t_{RELREL} (RMW)	t_{RMW}	Read-modify-write cycle time	310		405		490		ns	6,7
t_{RELREL} (PC)	t_{PC}	Page mode cycle time	155		200		240		ns	6,7
t_{RELQV}	t_{RAC}	Access time from $\overline{RAS}$		150		200		250	ns	7,8
t_{CELQV}	t_{CAC}	Access time from $\overline{CAS}$		85		115		145	ns	7,9
t_{CEHQZ}	t_{OFF}	Output buffer turn-off delay	0	40	0	50	0	60	ns	10
t_T	t_T	Transition time (rise and fall)	3	50	3	50	3	50	ns	5,15
t_{REHREL}	t_{RP}	$\overline{RAS}$ precharge time	100		135		165		ns	
t_{RELREH}	t_{RAS}	$\overline{RAS}$ pulse width	150	10,000	200	10,000	250	10,000	ns	
t_{CELREH}	t_{RSH}	$\overline{RAS}$ hold time	85		115		145		ns	
t_{RELCEH}	t_{CSH}	$\overline{CAS}$ hold time	150		200		250		ns	
t_{CELCEH}	t_{CAS}	$\overline{CAS}$ pulse width	85	10,000	115	10,000	145	10,000	ns	
t_{RELCEL}	t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ delay time	30	65	35	85	45	105	ns	11
t_{REHWX}	t_{RRH}	Read command hold time referenced to $\overline{RAS}$	20		25		30		ns	12
t_{AVREL}	t_{ASR}	Row address set-up time	0		0		0		ns	
t_{RELAX}	t_{RAH}	Row address hold time	20		25		30		ns	
t_{AVCEL}	t_{ASC}	Column address set-up time	0		0		0		ns	
t_{CELAX}	t_{CAH}	Column address hold time	30		40		50		ns	
$t_{RELA((}$	t_{AR}	Column address hold time referenced to $\overline{RAS}$	100		130		160		ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Continued)

(3,4,5,15) ($0° \leq T_A \leq 70°C$), V_{CC} = 5.0 V ± 10%

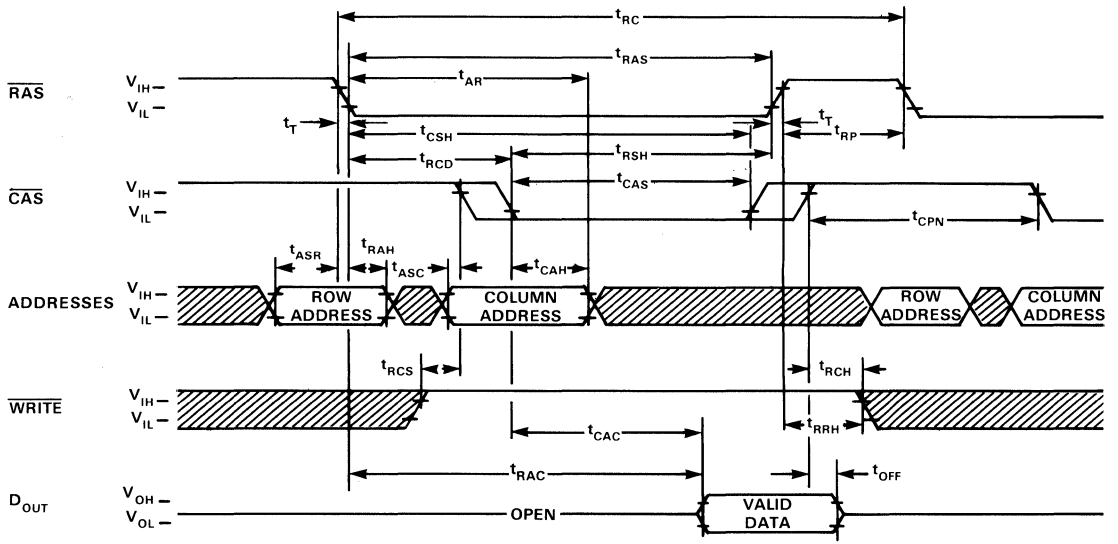
SYMBOL			MK4564-15		MK4564-20		MK4564-25			
STD	ALT	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
t_{WHCEL}	t_{RCS}	Read command set-up time	0		0		0		ns	
t_{CEHWX}	t_{RCH}	Read command hold time referenced to $\overline{CAS}$	0		0		0		ns	12
t_{CELWX}	t_{WCH}	Write command hold time	45		55		70		ns	
t_{RELWX}	t_{WCR}	Write command hold time referenced to $\overline{RAS}$	115		150		185		ns	
t_{WLWH}	t_{WP}	Write command pulse width	35		45		55		ns	
t_{WLREH}	t_{RWL}	Write command to $\overline{RAS}$ lead time	45		55		65		ns	
t_{WLCEH}	t_{CWL}	Write command to $\overline{CAS}$ lead time	45		55		65		ns	
t_{DVCEL}	t_{DS}	Data-in set-up time	0		0		0		ns	13
t_{CELDX}	t_{DH}	Data-in hold time	45		55		70		ns	13
t_{RELDX}	t_{DHR}	Data-in hold time referenced to $\overline{RAS}$	115		150		190		ns	
t_{CEHCEL} (PC)	t_{CP}	$\overline{CAS}$ precharge time (for page-mode cycle only)	60		75		85		ns	
t_{RVRV}	t_{REF}	Refresh Period		2		2		2	ms	
t_{WLCEL}	t_{WCS}	$\overline{WRITE}$ command set-up time	-10		-10		-10		ns	14
t_{CELWL}	t_{CWD}	$\overline{CAS}$ to $\overline{WRITE}$ delay	55		80		100		ns	14
t_{RELWL}	t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ delay	120		165		205		ns	14
t_{CEHCEL}	t_{CPN}	$\overline{CAS}$ precharge time	30		35		45		ns	

AC ELECTRICAL CHARACTERISTICS

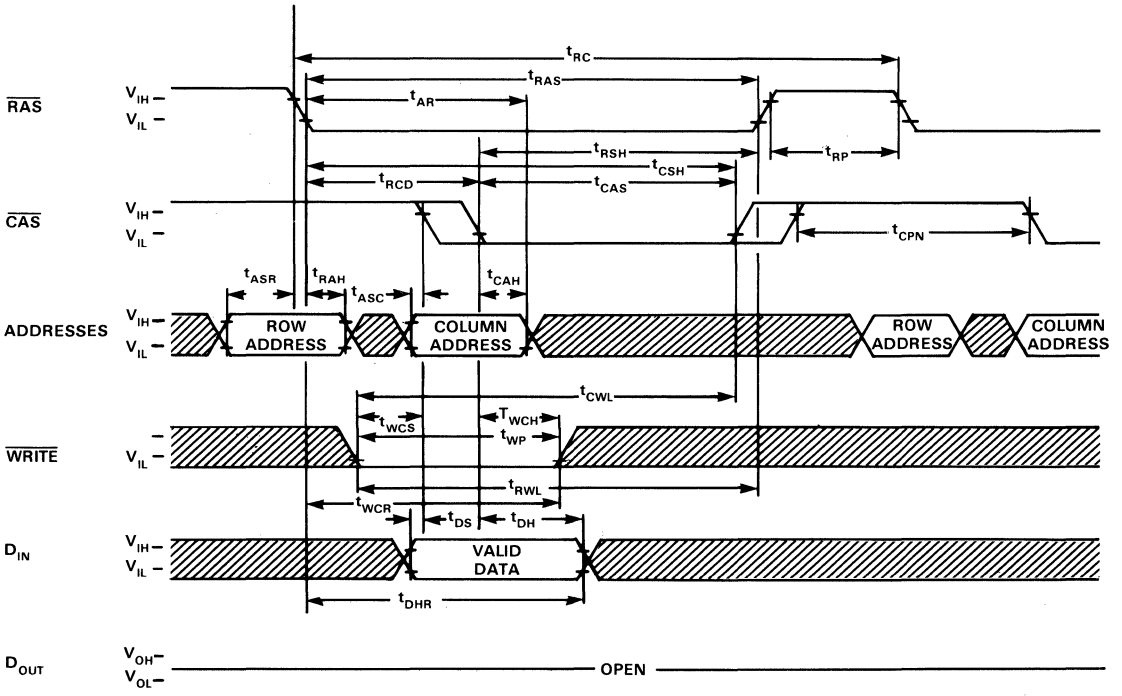
($0° \leq T_A \leq 70°C$), V_{CC} = 5.0 V ± 10%

SYM	PARAMETER	MAX	UNITS	NOTES
C_{I1}	Input Capacitance (A_0 - A_7), D_{IN}	5	pF	16
C_{I2}	Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	10	pF	16
C_O	Output Capacitance (D_{OUT})	7	pF	16,17

READ CYCLE

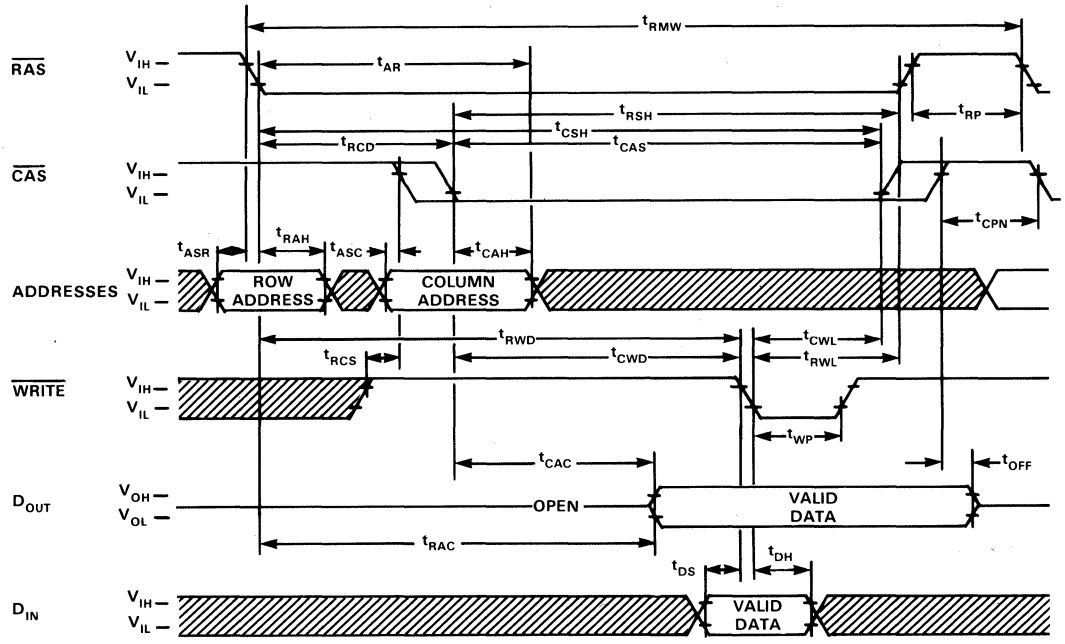


WRITE CYCLE (EARLY WRITE)

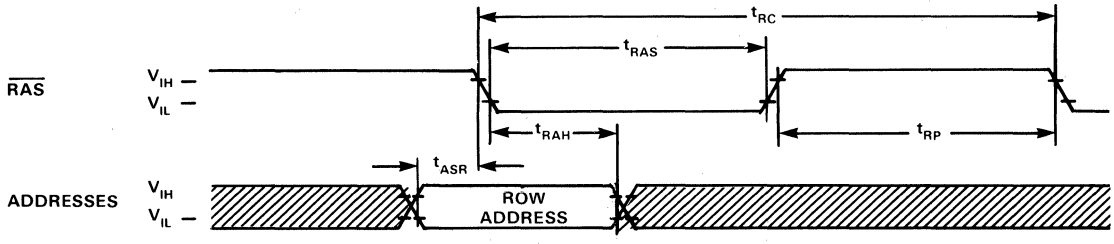


IV

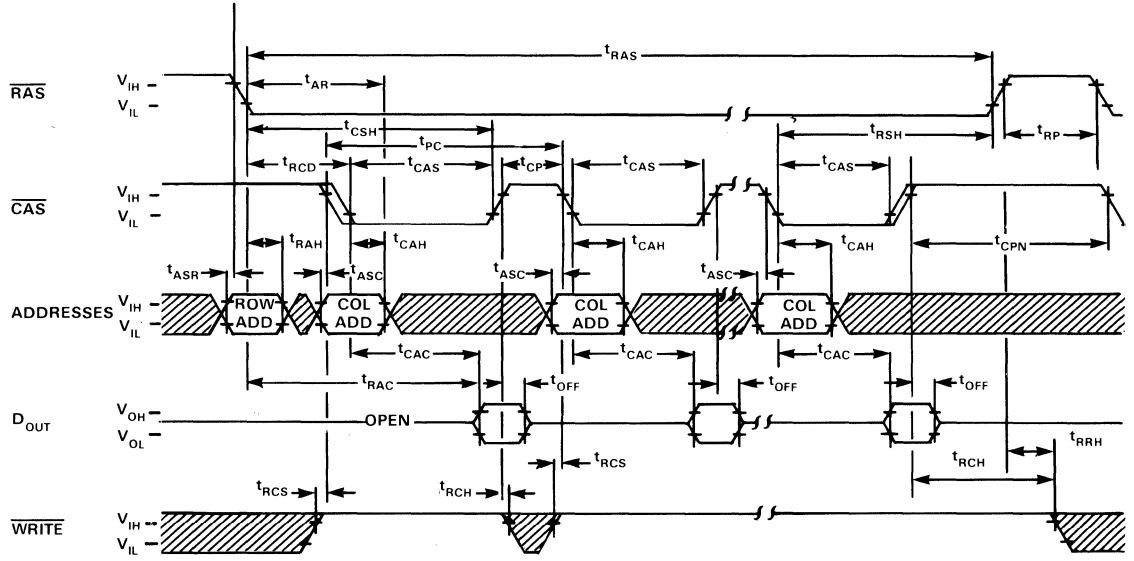
READ-WRITE/READ-MODIFY-WRITE CYCLE



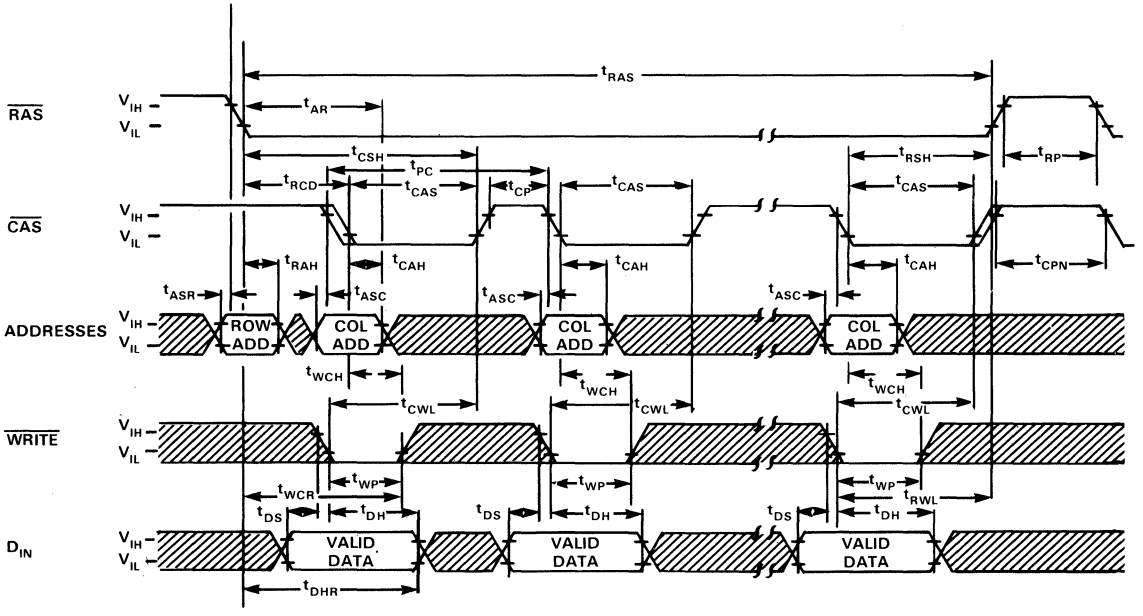
"RAS-ONLY" REFRESH CYCLE



PAGE MODE READ CYCLE



PAGE MODE WRITE CYCLE



OPERATION

The eight address bits required to decode 1 of the 65,536 cell locations within the MK4564 are multiplexed onto the eight address inputs and latched into the on-chip address latches by externally applying two negative going TTL-level clocks. The first clock, Row Address Strobe ($\overline{RAS}$), latches the eight row addresses into the chip. The high-to-low transition of the second clock, Column Address Strobe ($\overline{CAS}$), subsequently latches the eight column addresses into the chip. Each of these signals, $\overline{RAS}$ and $\overline{CAS}$, triggers a sequence of events which are controlled by different delayed internal clocks. The two clock chains are linked together logically in such a way that the address multiplexing operation is done outside of the critical timing path for read data access. The later events in the $\overline{CAS}$ clock sequence are inhibited until the occurrence of a delayed signal derived from the $\overline{RAS}$ clock chain. This "gated $\overline{CAS}$" feature allows the $\overline{CAS}$ clock to be externally activated as soon as the Row Address Hold specification (t_{RAH}) has been satisfied and the address inputs have been changed from Row address to Column address information.

The "gated $\overline{CAS}$" feature permits $\overline{CAS}$ to be activated at any time after t_{RAH} and it will have no effect on the worst case data access time (t_{RAC}) up to the point in time when the delayed row clock no longer inhibits the remaining sequence of column clocks. Two timing endpoints result from the internal gating of $\overline{CAS}$ which are called t_{RCD} (min) and t_{RCD} (max). No data storage or reading errors will result if $\overline{CAS}$ is applied to the MK4564 at a point in time beyond the t_{RCD} (max) limit. However, access time will then be determined exclusively by the access time from $\overline{CAS}$ (t_{CAC}) rather than from $\overline{RAS}$ (t_{RAC}), and $\overline{RAS}$ access time will be lengthened by the amount that t_{RCD} exceeds the t_{RCD} (max) limit.

DATA INPUT/OUTPUT

Data to be written into a selected cell is latched into an on-chip register by a combination of $\overline{WRITE}$ and $\overline{CAS}$ while $\overline{RAS}$ is active. The latter of $\overline{WRITE}$ or $\overline{CAS}$ to make its negative transition is the strobe for the Data In (D_{IN}) register. This permits several options in the write cycle timing. In a write cycle, if the $\overline{WRITE}$ input is brought low (active) prior to $\overline{CAS}$ being brought low (active), the D_{IN} is strobed by $\overline{CAS}$, and the Input Data set-up and hold times are referenced to $\overline{CAS}$. If the input data is not available at $\overline{CAS}$ time (late write) or if it is desired that the cycle be a read-write or read-modify-write cycle the $\overline{WRITE}$ signal should be delayed until after $\overline{CAS}$ has made its negative transition. In this "delayed write cycle" the data input set-up and hold times are referenced to the negative edge of $\overline{WRITE}$ rather than $\overline{CAS}$.

Data is retrieved from the memory in a read cycle by maintaining $\overline{WRITE}$ in the inactive or high state throughout the portion of the memory cycle in which both the $\overline{RAS}$ and $\overline{CAS}$ are low (active). Data read from the selected cell is available at the output port within the specified access time. The output data is the same polarity (not inverted) as the input data.

DATA OUTPUT CONTROL

The normal condition of the Data Output (D_{OUT}) of the MK4564 is the high impedance (open-circuit) state; anytime $\overline{CAS}$ is high (inactive) the D_{OUT} pin will be floating. Once the output data port has gone active, it will remain valid until $\overline{CAS}$ is taken to the precharge (inactive high) state.

PAGE MODE OPERATION

The Page Mode feature of the MK4564 allows for successive memory operations at multiple column locations within the same row address. This is done by strobing the row address into the chip and maintaining the $\overline{RAS}$ signal low (active) throughout all successive memory cycles in which the row address is common. The first access within a page mode operation will be available at t_{RAC} or t_{CAC} time, whichever is the limiting parameter. However, all successive accesses within the page mode operation will be available at t_{CAC} time (referenced to $\overline{CAS}$). With the MK4564 this results in approximately a 45% improvement in access times. Effective memory cycle times are also reduced when using page mode.

The page mode boundary of a single MK4564 is limited to the 256 column locations determined by all combinations of the eight column address bits. Operations within the page boundary need not be sequentially addressed and any combination of read, write, and read-modify-write cycles is permitted within the page mode operation.

REFRESH

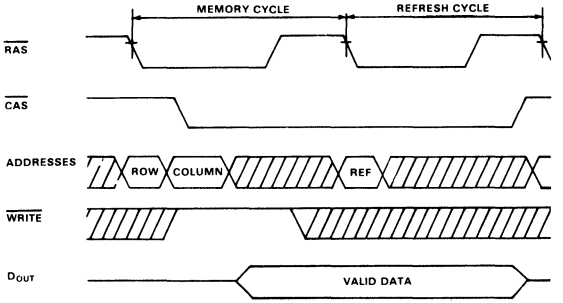
Refresh of the dynamic cell matrix is accomplished by performing a memory cycle at each of the 128 row addresses within each 2ms interval. Although any normal memory cycle will perform the required refreshing, this function is most easily accomplished with "$\overline{RAS}$-only" cycles.

The $\overline{RAS}$-only refresh cycle requires that a 7 bit refresh address (A0-A6) be valid at the device address inputs when $\overline{RAS}$ goes low (active). The state of the output data port during a $\overline{RAS}$-only refresh is controlled by $\overline{CAS}$. If $\overline{CAS}$ is high (inactive) during the entire time that $\overline{RAS}$ is asserted, the output will remain in the high impedance state. If $\overline{CAS}$ is low (active) the entire time that $\overline{RAS}$ is asserted, the output port will remain in the same state that it was prior to the issuance of the $\overline{RAS}$ signal. If $\overline{CAS}$ makes a low-to-high transition during the $\overline{RAS}$-only refresh cycle, the output data buffer will assume the high impedance state. However, $\overline{CAS}$ may not make a high to low transition during the $\overline{RAS}$-only refresh cycle since the device interprets this as a normal $\overline{RAS}/\overline{CAS}$ (read or write) type cycle.

HIDDEN REFRESH

A $\overline{RAS}$-only refresh cycle may take place while maintaining valid output data by extending the $\overline{CAS}$ active time from a previous memory read cycle. This feature is referred to as a hidden refresh. (See figure below.)

HIDDEN REFRESH CYCLE (SEE NOTE 19)



1982/1983 MICROELECTRONIC DATA BOOK

MOSTEK®

4096 x1-BIT STATIC RAM

MK4104(J/N/E) Series

FEATURES

- ☐ Combination static storage cells and dynamic control circuitry for truly high performance

PART NUMBER	ACCESS TIME	CYCLE TIME
MK4104-3/-33	200ns	310ns
MK4104-4/-34	250ns	385ns
MK4104-5/-35	300ns	460ns
MK4104-6	350ns	535ns

- ☐ Low Active Power Dissipation: 150mW (Max)
- ☐ Battery backup mode (3V/10mW on -33, -34 and -35)
- ☐ Standby Power Dissipation less than 28 mW (at V_{CC} = 5.5V)
- ☐ Single +5V Power Supply (± 10% tolerance)
- ☐ Fully TTL Compatible
  Fanout: 2 — Standard TTL
  2 — Schottky TTL
  12 — Low Power Schottky TTL
- ☐ Standard 18-pin DIP
- ☐ MKB version screened to MIL-STD-883

V

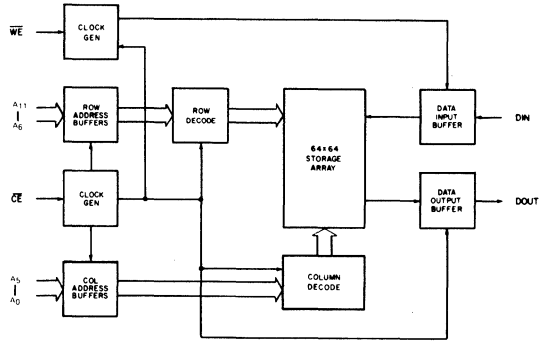
DESCRIPTION

The MOSTEK MK 4104 is a high performance static random access memory organized as 4096 one bit words. The MK 4104 combines the best characteristics of static and dynamic memory techniques to achieve a TTL compatible, 5 volt only, high performance, low power memory device. It utilizes advanced circuit design concepts and an innovative state-of-the-art N-channel silicon gate process specially tailored to provide static data storage with the performance (speed and power) of dynamic RAMs. Since the storage cell is static the device may be stopped indefinitely with the $\overline{CE}$ clock in the off (Logic 1) state.

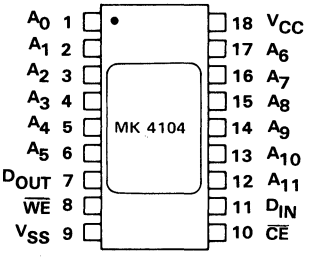
All input levels, including write enable ($\overline{WE}$) and chip enable ($\overline{CE}$) are TTL compatible with a one level of 2.2 volts and a zero level of 0.8 volts. This gives the system designer for a logic "1" state, at least 200mV of noise margin when driven by standard TTL and a minimum of 500mV when used with high performance Schottky TTL. These margins are wider than on most TTL compatible MOS memories available. The push-pull output (no pull-up resistor required) delivers a one level of 2.4V minimum and a zero level of .4 volts maximum. The output has a fanout of 2 standard TTL loads or 12 low power Schottky loads.

The RAM employs an innovative static cell which occupies a mere 2.75 square mils (½ the area of previous cells) and dissipates power levels comparable

FUNCTIONAL DIAGRAM



PIN CONNECTIONS



PIN NAMES

A_0-A_{11}	Address Inputs	V_{SS}	Ground
$\overline{CE}$	Chip Enable	V_{CC}	Power (+5V)
D_{IN}	Data Input	$\overline{WE}$	Write Enable
D_{OUT}	Data Output		

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to V_{SS} . . . . . −1.0V to +7.0V
Operating Temperature T_A (Ambient) . . . . . 0° C to + 70° C
Storage Temperature (Ambient) (Ceramic) . . . . . −65° C to +150° C
Storage Temperature (Ambient) (Plastic) . . . . . −55° C to +125° C
Power Dissipation . . . . . 1 Watt
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS[6]

(0° C ≤ T_A ≤ + 70° C)

	PARAMETER	MK4104 Series			UNITS	NOTES
		MIN	TYP	MAX		
V_{CC}	Supply Voltage	4.5	5.0	5.5	Volts	1
V_{SS}	Supply Voltage	0	0	0	Volts	1
V_{IH}	Logic "1" Voltage All Inputs	2.2		7.0	Volts	1
V_{IL}	Logic "0" Voltage All Inputs	-1.0		.8	Volts	1

DC ELECTRICAL CHARACTERISTICS[1]

(0° C ≤ T_A ≤ + 70° C) (V_{CC} = 5.0 volts ± 10%)

	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC1}	Average V_{CC} Power Supply Current		27	mA	2
I_{CC2}	Standby V_{CC} Power Supply Current		5	mA	3
I_{IL}	Input Leakage Current (Any Input)	−10	10	μA	4
I_{OL}	Output Leakage Current	−10	10	μA	3, 5
V_{OH}	Output Logic "1" Voltage I_{OUT}=−500μA	2.4		Volts	
V_{OL}	Output Logic "0" Voltage I_{OUT}= 5mA		0.4	Volts	

AC ELECTRICAL CHARACTERISTICS[1]

(0° C ≤ T_A ≤ + 70° C) (V_{CC} = + 5.0 volts ± 10%)

	PARAMETER	TYP	MAX	NOTES
C_I	Input Capacitance	4pF	6pF	14
C_O	Output Capacitance	6pF	7pF	14

NOTES:

1. All voltages referenced to V_{SS}.
2. I_{CC1} is related to precharge and cycle times. Guaranteed maximum values for I_{CC1} may be calculated by:
   I_{CC1} [ma] = $(5t_p + 15(t_C - t_p) + 4720) \div t_C$
   where t_p and t_C are expressed in nanoseconds. Equation is referenced to the -3 device, other devices derate to the same curve. Data outputs open.
3. Output is disabled (open circuit), $\overline{CE}$ is at logic 1.
4. All device pins at 0 volts except pin under test at 0 ≤ V_{IN} ≤ 5.5 volts. (V_{CC} = 5V)
5. 0V ≤ V_{OUT} ≤ + 5.5V . (V_{CC} = 5V)
6. During power up, $\overline{CE}$ and $\overline{WE}$ must be at V_{IH} for minimum of 2ms after V_{CC} reaches 4.5V, before a valid memory cycle can be accomplished.
7. Measured with load circuit equivalent to 2 TTL loads and CL = 100 pF.
8. If $\overline{WE}$ follows $\overline{CE}$ by more than t_{WS} then data out may not remain open circuited.
9. Determined by user. Total cycle time cannot exceed t_{CE} max.
10. Data-in set-up time is referenced to the later of the two falling clock edges $\overline{CE}$ or $\overline{WE}$.
11. AC measurements assume t_T = 5ns. Timing points are taken at .8V and 2.0V on inputs and .8V and 2.0V on the output. Transition times are also taken between these levels.
12. $t_C = t_{CE} + t_p + 2t_T$.
13. The true level of the output in the open circuit condition will be determined totally by output load conditions. The output is guaranteed to be open circuit within t_{OFF}.
14. Effective capacitance calculated from the equation $C = I\frac{\Delta t}{\Delta V}$ with Δ V equal to 3V and V_{CC} nominal.
15. $t_{RMW} = t_{AC} + t_{WPL} + t_p + 3t_T + t_{MOD}$

AC ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS[6,11]

($0°C \leq T_A \leq +70°C$) (V_{CC} = + 5.0 volts ± 10%)[1]

SYMBOL	PARAMETER	MK4104-3/33 MIN	MK4104-3/33 MAX	MK4104-4/34 MIN	MK4104-4/34 MAX	MK4104-5/35 MIN	MK4104-5/35 MAX	MK4104-6 MIN	MK4104-6 MAX	UNITS	NOTES
t_C	Read or Write Cycle Time	310		385		460		535		ns	12
t_{AC}	Random Access		200		250		300		350		7
t_{CE}	Chip Enable Pulse Width	200	10,000	250	10,000	300	10,000	350	10,000		
t_P	Chip Enable Precharge Time	100		125		150		175			
t_{AH}	Address Hold Time	110		135		165		190			
t_{AS}	Address Set-Up Time	0		0		0		0			
t_{OFF}	Output Buffer Turn-Off Delay	0	50	0	65	0	75	0	100		13
t_{RS}	Read Command Set-Up Time	0		0		0		0			8
t_{WS}	Write Enable Set-Up Time	-20		-20		-20		-20			8
t_{DHC}	Data Input Hold Time Referenced to $\overline{CE}$	170		210		250		285			
t_{DHW}	Data Input Hold Time Referenced to $\overline{WE}$	70		90		105		125			
t_{WW}	Write Enabled Pulse Width	60		75		90		105			
t_{MOD}	Modify Time	0	10,000	0	10,000	0	10,000	0	10,000		9
t_{WPL}	$\overline{WE}$ to $\overline{CE}$ Precharge Lead Time	70		85		105		120			
t_{DS}	Data Input Set-Up Time	0		0		0		0			10
t_{WH}	Write Enable Hold Time	150		185		225		260			
t_T	Transition Time	5	50	5	50	5	50	5	50		
t_{RMW}	Read-Modify-Write Cycle Time	385		475		570		660			16

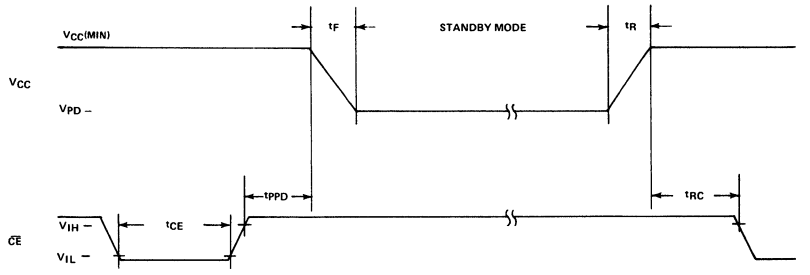
V

STANDBY CHARACTERISTICS

(T_A = 0°C to 70°C)

SYMBOL	PARAMETER	MK4104-33 MIN	MK4104-33 MAX	MK4104-34 MIN	MK4104-34 MAX	MK4104-35 MIN	MK4104-35 MAX	UNITS
V_{PD}	V_{CC} In Standby	3.0		3.0		3.0		Volts
I_{PD}	Standby Current		3.3		3.3		3.3	mA
t_F	Power Supply Fall Time	100		100		100		µsec
t_R	Power Supply Rise Time	100		100		100		µsec
t_{CE}	Chip Enable Pulse Width	200		250		300		µsec
t_{PPD}	Chip Enable Precharge To Power Down Time	100		125		150		nsec
V_{IH}	Min CE High "I" Level	2.2		2.2		2.2		Volts
t_{RC}	Standby Recovery Time	500		500		500		µsec

POWER DOWN WAVEFORM



DESCRIPTION (Cont'd)

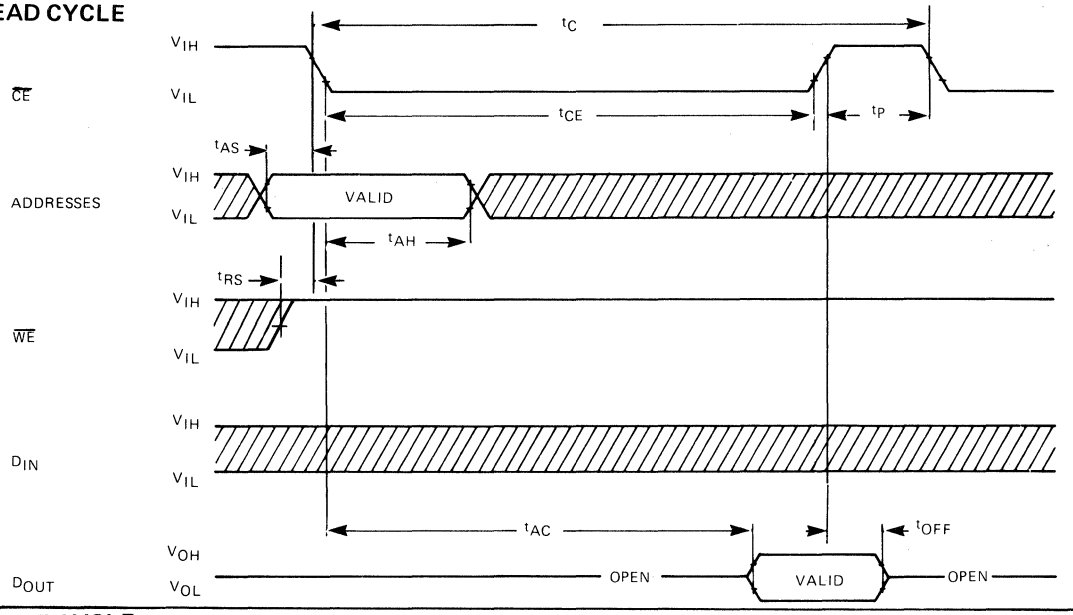
to CMOS. The static cell eliminates the need for refresh cycles and associated hardware thus allowing easy system implementation.

Power supply requirements of +5V ± 10% tolerance combined with TTL compatability on all I/0 pins permits easy integration into large memory configurations. The single supply reduces capacitor count and permits denser packaging on printed circuit boards. The 5V only supply requirement and TTL compatible I/0 makes this part an ideal choice for next generation +5V only microprocessors such as MOSTEK's MK3880 (Z80). The early write mode ($\overline{WE}$ active prior to $\overline{CE}$) permits common I/0 operation, needed for Z80 interfacing, without external circuitry.

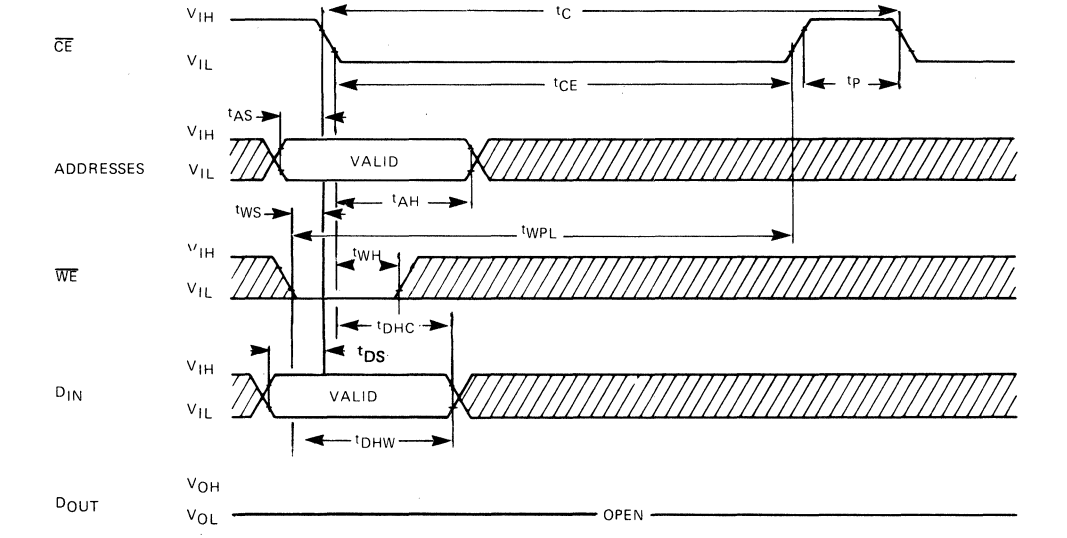
The MK4104-3X series has the added capability of retaining data in a reduced power mode. V_{CC} maybe lowered to 3V with a guaranteed power dissipation of only 10mW maximum. This makes the MK4104 ideal for those applications requiring data retention at the lowest possible power as in battery operation.

Reliability is greatly enhanced by the low power dissipation which causes a maximum junction rise of only at 8°C at 1.86 Megahertz operation. The MK 4104 was designed for the system designer and user who require the highest performance available along with MOSTEK's proven reliability.

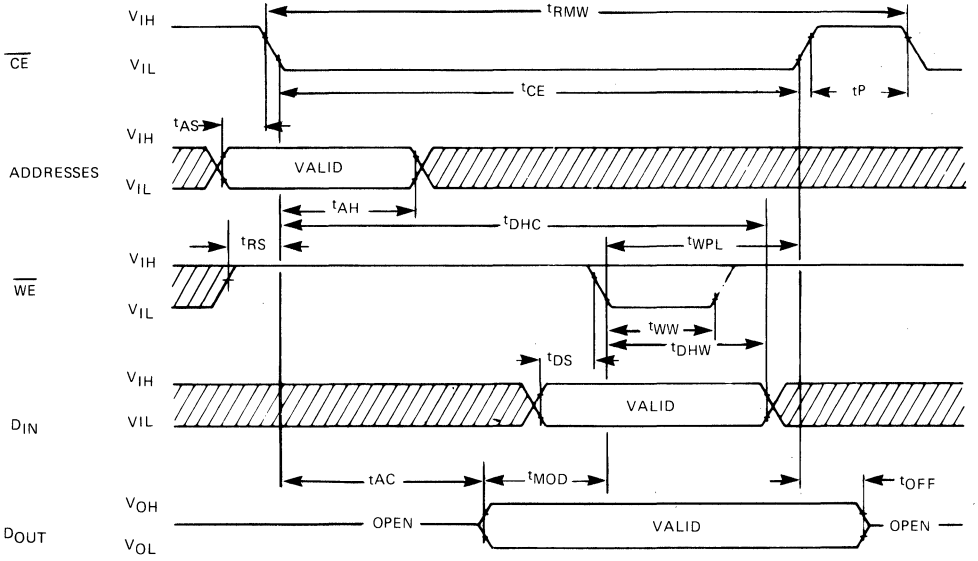
READ CYCLE



WRITE CYCLE



READ-MODIFY-WRITE CYCLE



OPERATION

READ CYCLE

The circuit offers one bit of the possible 4096 by decoding the 12 address bits presented at the inputs. The address bits are strobed into the chip by the negative-going edge of the Chip Enable ($\overline{CE}$) clock. A read cycle is accomplished by holding the 'write enable' ($\overline{WE}$) input at a high level (V_{IH}) while clocking the $\overline{CE}$ input to a low level (V_{IL}). At access time (t_{AC}) valid data will appear at the output. The output is unlatched by a positive transition of $\overline{CE}$ and therefore will be open circuited (high impedance state) from the previous cycle to access time and will go open again at the end of the present cycle when $\overline{CE}$ goes high.

Once the address hold time has been satisfied, the addresses may be changed for the next cycle.

WRITE CYCLE

Data that is to be written into a selected cell is strobed into the chip on the later occurring negative edge of $\overline{CE}$ or $\overline{WE}$. If the negative transition of $\overline{WE}$ occurs prior to the leading edge of $\overline{CE}$ as in an "early" write cycle then the $\overline{CE}$ input serves as the strobe for data-in. If $\overline{CE}$ leading edge occurs prior to the leading edge of $\overline{WE}$ as in a read-modify-write cycle then data-in is strobed by the $\overline{WE}$ input. Due to the internal timing generator, two independent timing parameters must be satisfied for DI hold time, these are, t_{DHW} and t_{DHC}. For a R/W or RMW cycle t_{DHC} is automatically satisfied making t_{DHW} the more restrictive parameter. For a write only cycle either parameter can be more restrictive depending on the position of $\overline{WE}$ relative to $\overline{CE}$. In any event both parameters must be satisfied.

In an early' write cycle the output will remain in an open or high impedance state. In a read-modify write operation the output will go active through the modify and write period until $\overline{CE}$ goes to precharge. If the cycle is such that $\overline{WE}$ goes active after $\overline{CE}$ but before valid data appears on the output (prior to t_{AC}) then the output may not remain open. However, if data-in is valid on the leading edge of $\overline{WE}$, and $\overline{WE}$ occurs prior to the positive transition of $\overline{CE}$ by the minimum lead time t_{WPL}, then valid data will be written into the selected cell. The Data in hold time parameters t_{DHW} and t_{DHC} must be satisfied.

READ-MODIFY-WRITE CYCLE

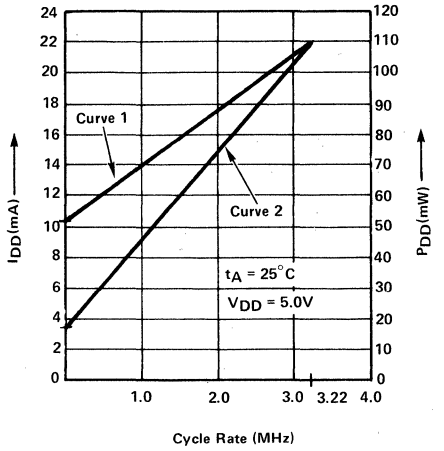
The read-modify-write (RMW) cycle is no more than an extension of the read and write cycles. Data is read at access time, modified during a period determined by the user and the same or new data written between $\overline{WE}$ active (low) and the rising edge of $\overline{CE}$ (t_{WPL}). Data out will remain valid until the rising edge of $\overline{CE}$. A minimum RMW cycle time can be approximated by the following equation (t_{RMW} = RMW cycle time and t_P = $\overline{CE}$ precharge time).

$$t_{RMW} = t_{AC} + t_{MOD} + t_{WPL} + t_P + 3t_T$$

POWER DOWN MODE

In power down data may be retained indefinitely by maintaining V_{CC} at +3V. However, prior to V_{CC} going below V_{CC} minimum ($\leq$4.5V) $\overline{CE}$ must be taken high (V_{IH} = 2.2V) and held for a minimum time period t_{PPD} and maintained at V_{IH} for the entire standby period. After power is returned to V_{CC} min or above, $\overline{CE}$ must be held high for a minimum of t_{RC} in order that the device may operate properly. See power down waveforms herein. Any active cycle in progress prior to power down must be completed so that t_{CE} min is not violated.

OPERATING POWER VS CYCLE TIME



Characterization data plot of frequency vs power dissipation for a typical MK4104 device.

Curve 1 - Clock on time (low level) is bottom scale minus 100 NSEC

Curve 2 - Clock off time (high level) is bottom scale minus 200 NSEC

MOSTEK

MEMORY COMPONENTS

1K x 8-Bit Static RAM

MK4118A/MK4801A(P/J/N) Series

FEATURES

- ☐ Static operation
- ☐ Organization: 1K x 8 bit RAM JEDEC pinout
- ☐ High performance
- ☐ Pin compatible with Mostek's BYTEWYDE™ memory family
- ☐ 24/28 pin ROM/PROM compatible pin configuration
- ☐ $\overline{CE}$ and $\overline{OE}$ functions facilitate bus control
- ☐ MKB version screened to MIL-STD-883

Part No.	Access Time	R/W Cycle Time
MK4118A-1	120 nsec	120 nsec
MK4118A-2	150 nsec	150 nsec
MK4118A-3	200 nsec	200 nsec
MK4118A-4	250 nsec	250 nsec

V

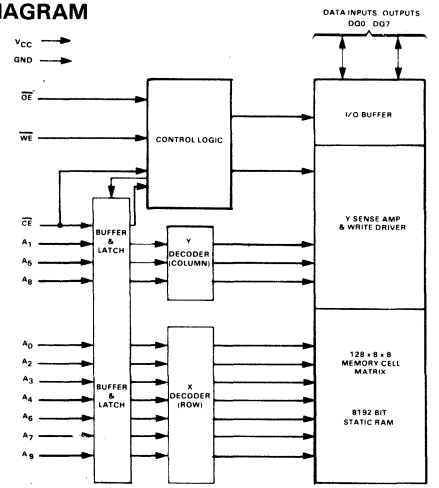
DESCRIPTION

The MK4118A uses Mostek's advanced circuit design techniques to package 8,192 bits of static RAM on a single chip. Static operation is achieved with high performance and low power dissipation by utilizing Address Activated™ circuit design techniques.

The MK4118A excels in high speed memory applications where the organization requires relatively shallow depth with a wide word format. The MK4118A presents to the user a high density cost effective N-MOS memory with the performance characteristics necessary for today's microprocessor applications.

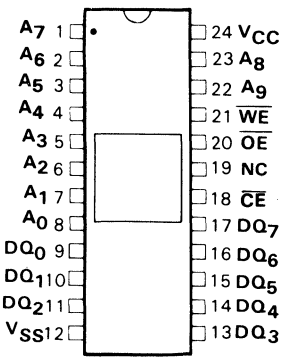
BLOCK DIAGRAM

Figure 1



PIN CONNECTIONS

Figure 2



TRUTH TABLE

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	DQ
V_{IH}	X	X	Deselect	High Z
V_{IL}	X	V_{IL}	Write	D_{IN}
V_{IL}	V_{IL}	V_{IH}	Read	D_{OUT}
V_{IL}	V_{IH}	V_{IH}	Read	High Z

X = Don't Care

PIN NAMES

A_0-A_9	Address Inputs	$\overline{WE}$	Write Enable
$\overline{CE}$	Chip Enable	$\overline{OE}$	Output Enable
V_{SS}	Ground	NC	No Connection
V_{CC}	Power (+5V)	DQ_0-DQ_7	Data In/Data Out

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to V_{SS} ..... -.5 V to +7.0 V
Operating Temperature T_A (Ambient) ..... 0°C to +70°C
Storage Temperature (Ambient)(Ceramic) ..... -65°C to +150°C
Storage Temperature (Ambient)(Plastic) ..... -55°C to +125°C
Power Dissipation ..... 1 Watt
Output Current ..... 20 mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS[7]

($0°C \leq T_A \leq +70°C$)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.75	5.0	5.25	V	1
V_{SS}	Supply Voltage	0	0	0	V	1
V_{IH}	Logic "1" Voltage All Inputs	2.2		7.0	V	1
V_{IL}	Logic "0" Voltage All Inputs	-0.3		.8	V	1, 9

DC ELECTRICAL CHARACTERISTICS[1,7]

($0°C \leq T_A \leq +70°C$) (V_{CC} = 5.0 V ± 5%)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
I_{CC1}	Average V_{CC} Power Supply Current		50	80	mA	8
I_{IL}	Input Leakage Current (Any Input)	-10		10	μA	2
I_{OL}	Output Leakage Current	-10		10	μA	2
V_{OH}	Output Logic "1" Voltage I_{OUT} = 1 mA	2.4			V	
V_{OL}	Output Logic "0" Voltage I_{OUT} = 4 mA			0.4	V	

CAPACITANCE[1,7]

($0°C \leq T_A \leq +70°C$) (V_{CC} = +5.0 V ± 5%)

SYM	PARAMETER	TYP	MAX	NOTES
C_I	All pins (except D/Q)	4 pF	6 pF	
$C_{D/Q}$	D/Q pins	10 pF	12 pF	6

AC ELECTRICAL CHARACTERISTICS [3,4]

($0°C \leq T_A \leq 70°$) ($V_{CC} = 5.0\ V \pm 5\%$)

		-1		-2		-3		-4			
SYM	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
t_{RC}	Read Cycle Time	120		150		200		250		ns	
t_{AA}	Address Access Time		120		150		200		250	ns	5
t_{CEA}	Chip Enable Access Time		60		75		100		125	ns	5
t_{CEZ}	Chip Enable Data Off Time	5	30	5	35	5	40	5	45	ns	
t_{OEA}	Output Enable Access Time		60		75		100		125	ns	5
t_{OEZ}	Output Enable Data Off Time	5	30	5	35	5	40	5	45	ns	
t_{AZ}	Address Data Off Time	10		10		10		10		ns	
t_{WC}	Write Cycle Time	120		150		200		250		ns	
t_{AS}	Address Setup Time	0		0		0		0		ns	see text
t_{AH}	Address Hold Time	40		50		65		80		ns	see text
t_{DSW}	Data To Write Setup Time	10		10		15		20		ns	
t_{DHW}	Data From Write Hold Time	10		10		10		10		ns	
t_{WD}	Write Pulse Duration	45		50		60		70		ns	see text
t_{WEZ}	Write Enable Data Off Time	5	30	5	35	5	40	5	45	ns	
t_{WPL}	Write Pulse Lead Time	75		90		130		170		ns	

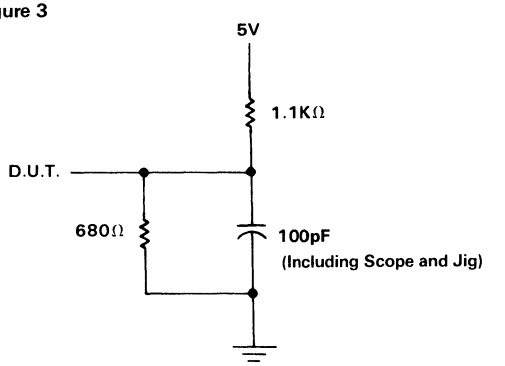
V

NOTES:

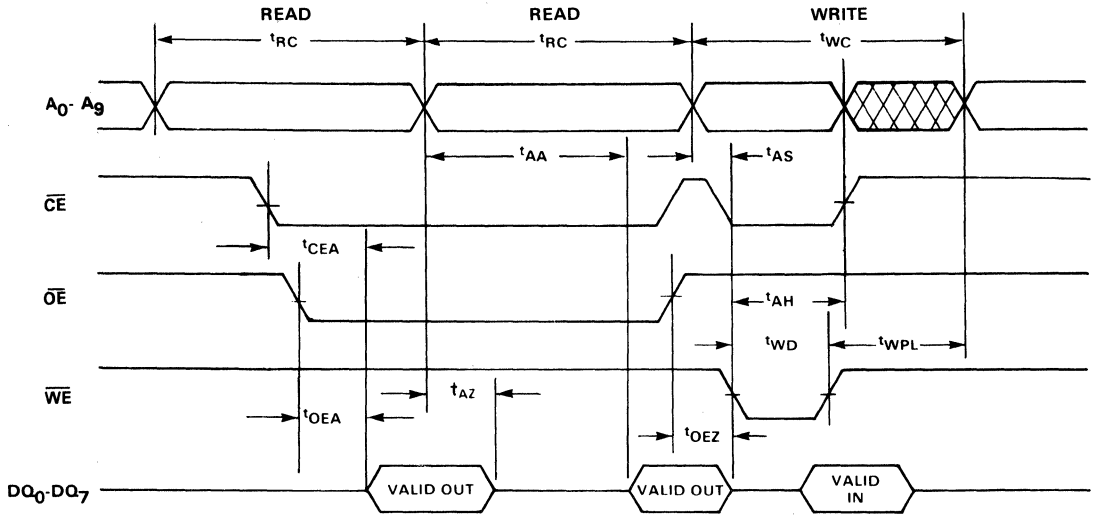
1. All voltages referenced to V_{SS}
2. Measured with $.4 \leq V_I \leq 5.0$ V, outputs deselected and $V_{CC} = 5$ V
3. AC measurements assume Transition Time = 5 ns, levels V_{SS} to 3.0 V
4. Input and output timing reference levels are at 1.5 V
5. Measured with a load as shown in Figure 3.
6. Output buffer is deselected.
7. A minimum of 2ms time delay is required after application of V_{CC} (+5 V) before proper device operation can be achieved.
8. I_{CC} measured with outputs open.
9. Negative undershoots to a minimum of -1.5 V are allowed with a maximum of 50 ns pulse width.

OUTPUT LOAD

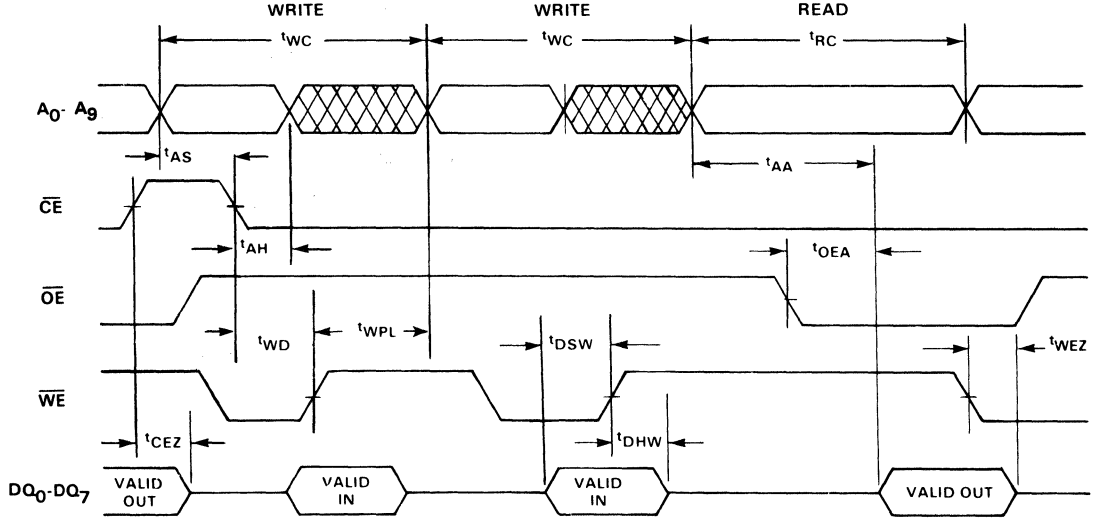
Figure 3



TIMING DIAGRAM
Figure 4



TIMING DIAGRAM
Figure 5



The MK4118A features a fast $\overline{CE}$ (50% of Address Access) function to permit memory expansion without impacting system access time. A fast $\overline{OE}$ (50% of access time) is included to permit data interleaving for enhanced system performance.

The MK4118A is pin compatible with Mostek's BYTEWYDE™ memory family of RAMs, ROMs and EPROMs. Mostek also offers a higher performance version of the MK4118A designated the MK4801A.

OPERATION

Read Mode

The MK4118A is in the READ MODE whenever the Write Enable Control input ($\overline{WE}$) is in the high state.

In the READ mode of operation, the MK4118A provides a fast address ripple-through access of data from 8 of 8192 locations in the static storage array. Thus, the unique address specified by the 10 Address Inputs (An) define which 1 of 1024 bytes of data is to be accessed.

A transition on any of the 10 address inputs will disable the 8 Data Output Drivers after t_{AZ}. Valid Data will be available to the 8 Data Output Drivers within t_{AA} after the last address input signal is stable, providing that the $\overline{CE}$ and $\overline{OE}$ access times are satisfied. If $\overline{CE}$ or $\overline{OE}$ access times are not met, data access will be measured from the limiting parameter (t_{CEA} or t_{OEA}) rather than the address. The state of the 8 data I/O signals is controlled by the Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) control signals.

Write Mode

The MK4118A is in the Write Mode whenever the Write Enable ($\overline{WE}$) and Chip Enable ($\overline{CE}$) control inputs are in the low state.

The WRITE cycle is initiated by the $\overline{WE}$ pulse going low provided that $\overline{CE}$ is also low. The leading edge of the $\overline{WE}$ pulse is used to latch the status of the address bus.

NOTE: In a write cycle the latter occurring edge of either $\overline{WE}$ or $\overline{CE}$ will determine the start of the write cycle. Therefore, t_{AS}, t_{WD} and t_{AH} are referenced to the latter occurring edge of $\overline{CE}$ or $\overline{WE}$. Addresses are latched at this time. All write cycles whether initiated by $\overline{CE}$ or $\overline{WE}$ must be terminated by the rising edge of $\overline{WE}$. If the output bus has been enabled ($\overline{CE}$ and $\overline{OE}$ low) then $\overline{WE}$ will cause the output to go to the high Z state in t_{WEZ}.

Data In must be valid t_{DSW} prior to the low to high transition of $\overline{WE}$. The Data In lines must remain stable for t_{DHW} after $\overline{WE}$ goes inactive. The write control of the MK4118A disables the data out buffers during the write cycle; however, $\overline{OE}$ should be used to disable the data out buffers to prevent bus contention between the input data and data that would be output upon completion of the write cycle.

1K x 8-Bit Static RAM

MK4801A(P/J/N) Series

FEATURES

- ☐ Static operation
- ☐ Organization: 1K x 8 bit RAM JEDEC pinout
- ☐ Pin compatible with Mostek's BYTEWYDE™ memory family
- ☐ 24/28 pin ROM/PROM compatible pin configuration
- ☐ High performance
- ☐ $\overline{CE}$ and $\overline{OE}$ functions facilitate bus control

Part No.	Access Time	R/W Cycle Time
MK4801A-55	55 nsec	55/65 nsec
MK4801A-70	70 nsec	70/80 nsec
MK4801A-90	90 nsec	90/100 nsec

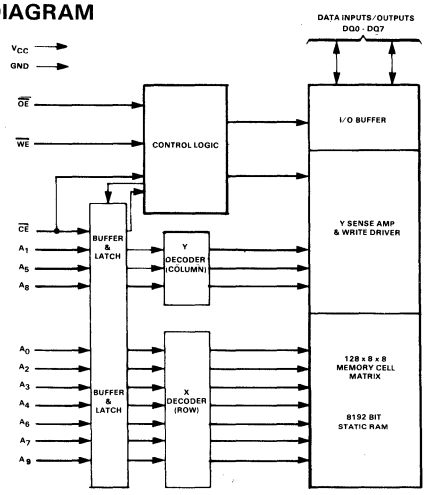
DESCRIPTION

The MK4801A uses Mostek's Scaled POLY 5™ process and advanced circuit design techniques to package 8,192 bits of static RAM on a single chip. Static operation is achieved with high performance and low power dissipation by utilizing Address Activated™ circuit design techniques.

The MK4801A excels in high speed memory applications where the organization requires relatively shallow depth with a wide word format. The MK4801A presents the user a high density cost effective alternative to bipolar and previous generation N-MOS fast memory.

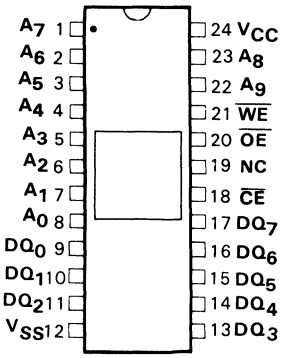
BLOCK DIAGRAM

Figure 1



PIN CONNECTIONS

Figure 2



TRUTH TABLE

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	DQ
V_{IH}	X	X	Deselect	High Z
V_{IL}	X	V_{IL}	Write	D_{IN}
V_{IL}	V_{IL}	V_{IH}	Read	D_{OUT}
V_{IL}	V_{IH}	V_{IH}	Read	High Z

X = Don't Care

PIN NAMES

A_0-A_9	Address Inputs	$\overline{WE}$	Write Enable
$\overline{CE}$	Chip Enable	$\overline{OE}$	Output Enable
V_{SS}	Ground	NC	No Connection
V_{CC}	Power (+5V)	DQ_0-DQ_7	Data In/ Data Out

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to V_{SS} ..... -.5V to + 7.0V
Operating Temperature T_A (Ambient) ..... 0°C to +70°C
Storage Temperature (Ambient)(Ceramic) ..... -65°C to +150°C
Storage Temperature (Ambient)(Plastic) ..... -55°C to +125°C
Power Dissipation ..... 1 Watt
Output Current 20mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS[7]

(0°C ≤ T_A ≤ +70°C)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.75	5.0	5.25	V	1
V_{SS}	Supply Voltage	0	0	0	V	1
V_{IH}	Logic "1" Voltage All Inputs	2.2		7.0	V	1
V_{IL}	Logic "0" Voltage All Inputs	-2.0		.8	V	1,9

DC ELECTRICAL CHARACTERISTICS[1,7]

(0°C ≤ T_A ≤ +70°C) (V_{CC} = 5.0 V ± 5%)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
I_{CC1}	Average V_{CC} Power Supply Current		60	125	mA	8
I_{IL}	Input Leakage Current (Any Input)	-10		10	μA	2
I_{OL}	Output Leakage Current	-10		10	μA	2
V_{OH}	Output Logic "1" Voltage I_{OUT} = 1 mA	2.4			V	
V_{OL}	Output Logic "0" Voltage I_{OUT} = 4 mA			0.4	V	

CAPACITANCE[1,7]

(0°C ≤ T_A ≤ +70°C) (V_{CC} = +5.0 V ± 5%)

SYM	PARAMETER	TYP	MAX	NOTES
C_I	All pins (except D/Q)	4 pF	6 pF	
$C_{D/Q}$	D/Q pins	10 pF	12 pF	6

AC ELECTRICAL CHARACTERISTICS [3,4]

($0°C \leq T_A \leq 70°$) (V_{CC} = 5.0 V ± 5%)

		MK4801A-55		MK4801A-70		MK4801A-90			
SYM	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
t_{RC}	Read Cycle Time	55		70		90		ns	
t_{AA}	Address Access Time		55		70		90	ns	5
t_{CEA}	Chip Enable Access Time		25		35		45	ns	5
t_{CEZ}	Chip Enable Data Off Time	5	15	5	20	5	30	ns	
t_{OEA}	Output Enable Access Time		25		35		45	ns	5
t_{OEZ}	Output Enable Data Off Time	5	15	5	20	5	30	ns	
t_{AZ}	Address Data Off Time	10		10		10		ns	
t_{WC}	Write Cycle Time	65		80		100		ns	
t_{AS}	Address Setup Time	0		0		0		ns	see text
t_{AH}	Address Hold Time	15		20		30		ns	see text
t_{DSW}	Data To Write Setup Time	5		5		5		ns	
t_{DHW}	Data From Write Hold Time	10		10		10		ns	
t_{WD}	Write Pulse Duration	25		30		40		ns	see text
t_{WEZ}	Write Enable Data Off Time	5	10	5	15	5	25	ns	
t_{WPL}	Write Pulse Lead Time	40		50		60		ns	

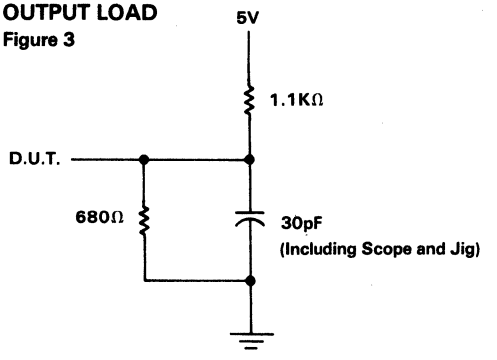
V

NOTES:

1. All voltages referenced to V_{SS}.
2. Measured with $.4 \leq V_I \leq 5.0$ V, outputs deselected and V_{CC} = 5 V.
3. AC measurements assume Transition Time = 5 ns, levels V_{SS} to 3.0 V.
4. Input and output timing reference levels are at 1.5 V.
5. Measured with a load as shown in Figure 3.
6. Output buffer is deselected.
7. A minimum of 2 ms time delay is required after application of V_{CC} (+5 V) before proper device operation can be achieved.
8. I_{CC} measured with outputs open.
9. Negative undershoots to a minimum of -1.5 V are allowed with a maximum of 50 ns pulse width.

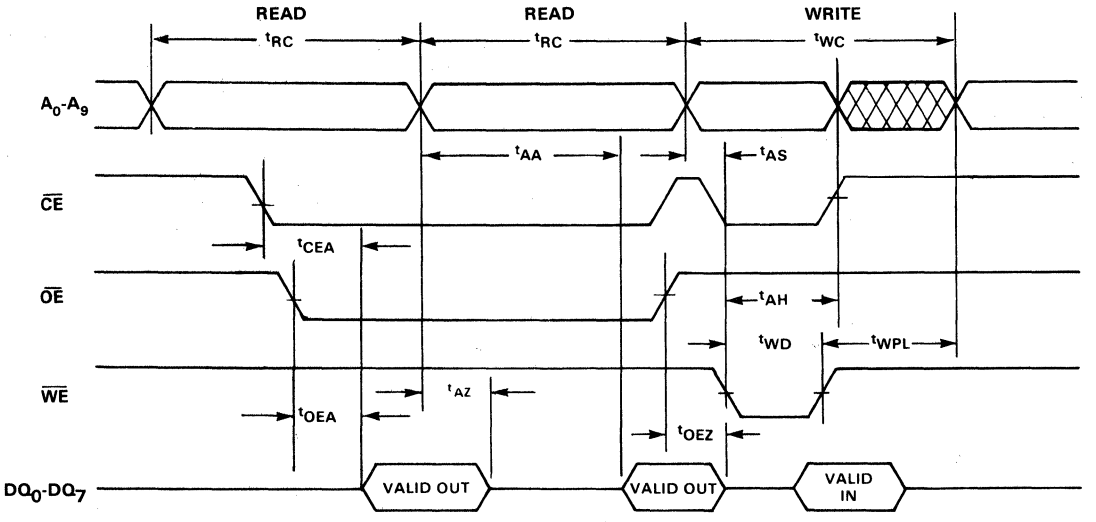
OUTPUT LOAD

Figure 3



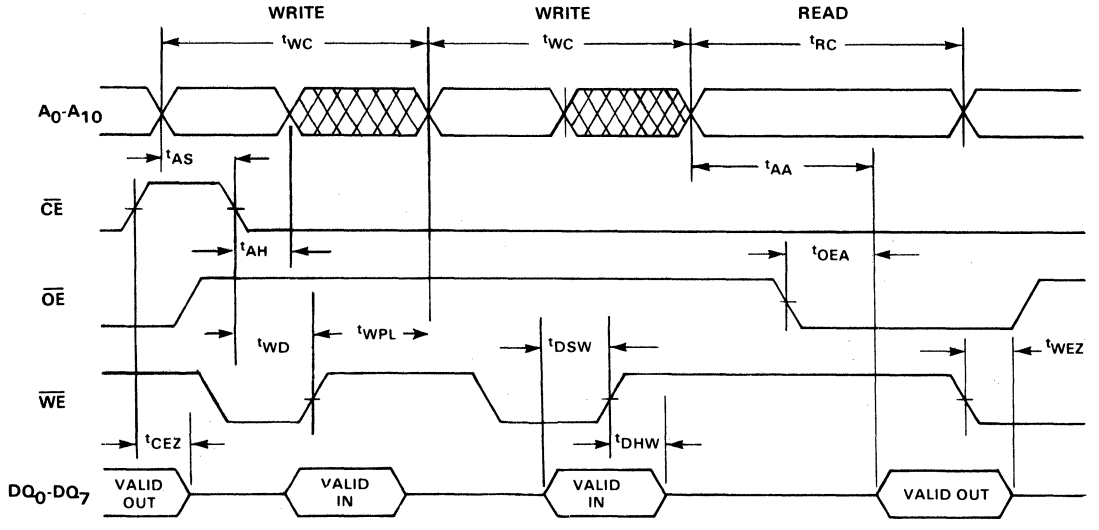
TIMING DIAGRAM

Figure 4



TIMING DIAGRAM

Figure 5



The MK4801A features a fast $\overline{CE}$ (50% of Address Access) function to permit memory expansion without impacting system access time. A fast $\overline{OE}$ (50% of access time) is included to permit data interleaving for enhanced system performance.

The MK4801A is pin compatible with Mostek's BYTEWYDE™ memory family of RAMs, ROMs and EPROMs.

OPERATION

Read Mode

The MK4801A is in the READ MODE whenever the Write Enable Control input ($\overline{WE}$) is in the high state.

In the READ mode of operation, the MK4801A provides a fast address ripple-through access of data from 8 of 8192 locations in the static storage array. Thus, the unique address specified by the 10 Address Inputs (An) define which 1 of 1024 bytes of data is to be accessed.

A transition on any of the 10 address inputs will disable the 8 Data Output Drivers after t_{AZ}. Valid Data will be available to the 8 Data Output Drivers within t_{AA} after the last address input signal is stable, providing that the $\overline{CE}$ and $\overline{OE}$ access times are satisfied. If $\overline{CE}$ or $\overline{OE}$ access times are not met, data access will be measured from the limiting parameter (t_{CEA} or t_{OEA}) rather than the address. The state of the 8 data I/O signals is controlled by the Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) control signals.

Write Mode

The MK4801A is in the Write Mode whenever the Write Enable ($\overline{WE}$) and Chip Enable ($\overline{CE}$) control inputs are in the low state.

The WRITE cycle is initiated by the $\overline{WE}$ pulse going low provided that $\overline{CE}$ is also low. The leading edge of the $\overline{WE}$ pulse is used to latch the status of the address bus.

NOTE: In a write cycle the latter occurring edge of either $\overline{WE}$ or $\overline{CE}$ will determine the start of the write cycle. Therefore, t_{AS}, t_{WD} and t_{AH} are referenced to the latter occurring edge of $\overline{CE}$ or $\overline{WE}$. Addresses are latched at this time. All write cycles whether initiated by $\overline{CE}$ or $\overline{WE}$ must be terminated by the rising edge of $\overline{WE}$. If the output bus has been enabled ($\overline{CE}$ and $\overline{OE}$ low) then $\overline{WE}$ will cause the output to go to the high Z state in t_{WEZ}.

Data In must be valid t_{DSW} prior to the low to high transition of $\overline{WE}$. The Data In lines must remain stable for t_{DHW} after $\overline{WE}$ goes inactive. The write control of the MK4801A disables the data out buffers during the write cycle; however $\overline{OE}$ should be used to disable the data out buffers to prevent bus contention between the input data and data that would be output upon completion of the write cycle.

1982/1983 MICROELECTRONIC DATA BOOK

PRELIMINARY

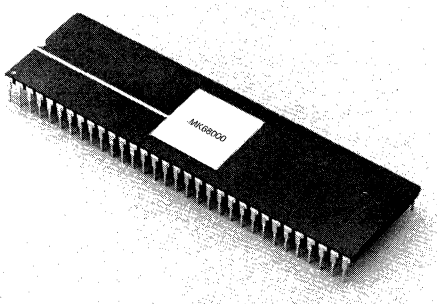
MOSTEK

MICROCOMPUTER COMPONENTS

16-Bit Microprocessor

MK68000

Advances in semiconductor technology have provided the capability to place on a single silicon chip a microprocessor at least an order of magnitude higher in performance and circuit complexity than has been previously available. The MK68000 is the first of a family of such VLSI microprocessors from Mostek. It combines state-of-the-art technology and advanced circuit design techniques with computer sciences to achieve an architecturally advanced 16-bit microprocessor.

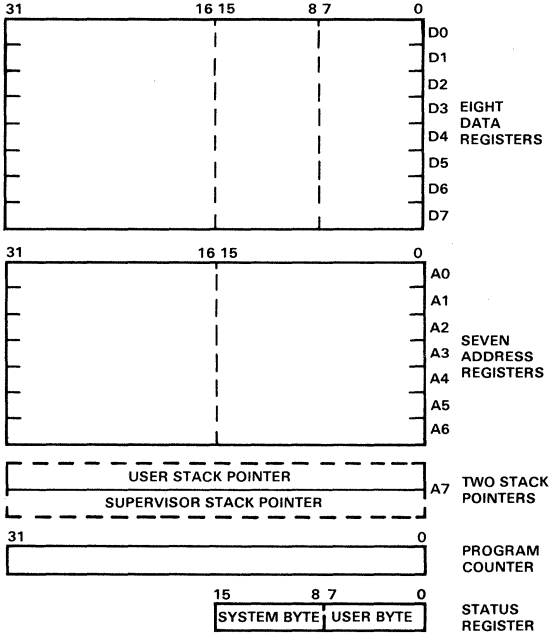


The resources available to the MK68000 user consist of the following:

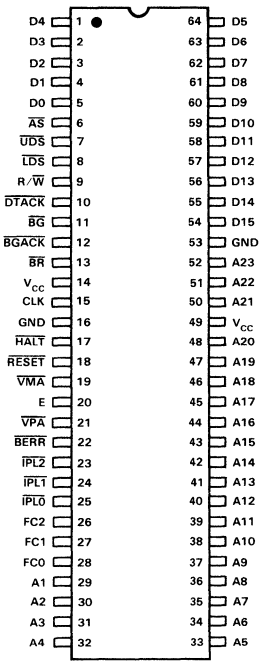
- 32-Bit Data and Address Registers
- 16 Megabyte Direct Addressing Range
- 56 Powerful Instruction Types
- Operations on Five Main Data Types
- Memory Mapped I/O
- 14 Addressing Modes

VI

PROGRAMMING MODEL



PIN ASSIGNMENT



This is advance information and specifications are subject to change without notice.

As shown in the programming model, the MK68000 offers seventeen 32-bit registers in addition to the 32-bit program counter and a 16-bit status register. The first eight registers (D0-D7) are used as data registers for byte (8-bit), word (16-bit), and long word (32-bit) data operations. The second set of seven registers (A0-A6) and the system stack pointer may be used as software stack pointers and base address registers. In addition, these registers may be used for word and long word address operations. All 17 registers may be used as index registers.

A 23-bit address bus provides a memory addressing range of greater than 16 megabytes. This large range of addressing capability, coupled with a memory management unit, allows large, modular programs to be developed and operated without resorting to cumbersome and time consuming software bookkeeping and paging techniques.

The status register contains the interrupt mask (eight levels available) as well as the condition codes; extend (X), negative (N), zero (Z), overflow (V), and carry (C). Additional status bits indicate that the processor is in a trace (T) mode and/or in a supervisor (S) state.

Five basic data types are supported. These data types are:

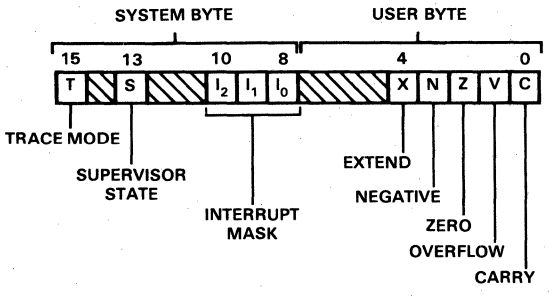
- Bits
- BCD Digits (4-bits)
- Bytes (8-bits)
- Word (16-bits)
- Long Words (32-bits)

In addition, operations on other data types such as memory addresses, status word data, etc., are provided for in the instruction set.

The 14 addressing modes, shown in Table 1, include six basic types:

- Register Direct
- Register Indirect
- Absolute
- Immediate
- Program Counter Relative
- Implied

STATUS REGISTER



Included in the register indirect addressing modes is the capability to do postincrementing, predecrementing, offsetting and indexing. Program counter relative mode can also be modified via indexing and offsetting.

The MK68000 instruction set is shown in Table 2. Some additional instructions are variations, or subsets, of these and they appear in Table 3. Special emphasis has been given to the instruction set's support of structured high-level languages to facilitate ease of programming. Each instruction, with few exceptions, operates on bytes, words, and long words and most instructions can use any of the 14 addressing modes. Combining instruction types, data types, and addressing modes, over 1000 useful instructions are provided. These instructions include signed and unsigned multiply and divide, "quick" arithmetic operations, BCD arithmetic and expanded operations (through traps).

DATA ADDRESSING MODES

Table 1

Mode	Generation
Register Direct Addressing	
Data Register Direct	EA = Dn
Address Register Direct	EA = An
Absolute Data Addressing	
Absolute Short	EA = (Next Word)
Absolute Long	EA = (Next Two Words)
Program Counter Relative Addressing	
Relative with Offset	EA = (PC) + d_{16}
Relative with Index and Offset	EA = (PC) + (Xn) + d_8
Register Indirect Addressing	
Register Indirect	EA = (An)
Postincrement Register Indirect	EA = (An), An ← An + N
Predecrement Register Indirect	An ← An – N, EA = (An)
Register Indirect with Offset	EA = (An) + d_{16}
Indexed Register Indirect with Offset	EA = (An) + (Xn) + d_8
Immediate Data Addressing	
Immediate	DATA = Next Word(s)
Quick Immediate	Inherent Data
Implied Addressing	
Implied Register	EA = SR, USP, SP, PC

NOTES:

EA = Effective Address
An = Address Register
Dn = Data Register
Xn = Address or Data Register used as Index Register
SR = Status Register
PC = Program Counter
( ) = Contents of
d_8 = Eight-bit Offset (displacement)
d_{16} = Sixteen-bit Offset (displacement)
N = 1 for Byte, 2 for Words and 4 for Long Words
← = Replaces

INSTRUCTION SET

Table 2

Mnemonic	Description	Mnemonic	Description	Mnemonic	Description
ABCD	Add Decimal with Extend	EOR	Exclusive Or	PEA	Push Effective Address
ADD	Add	EXG	Exchange Registers	RESET	Reset External Devices
AND	Logical And	EXT	Sign Extend	ROL	Rotate Left without Extend
ASL	Arithmetic Shift Left	JMP	Jump	ROR	Rotate Right without Extend
ASR	Arithmetic Shift Right	JSR	Jump to Subroutine	ROXL	Rotate Left with Extend
B_{CC}	Branch Conditionally	LEA	Load Effective Address	ROXR	Rotate Right with Extend
BCHG	Bit Test and Change	LINK	Link Stack	RTE	Return from Exception
BCLR	Bit Test and Clear	LSL	Logical Shift Left	RTR	Return and Restore
BRA	Branch Always	LSR	Logical Shift Right	RTS	Return from Subroutine
BSET	Bit Test and Set	MOVE	Move	SBCD	Subtract Decimal with Extend
BSR	Branch to Subroutine	MOVEM	Move Multiple Registers	S_{CC}	Set Conditional
BTST	Bit Test	MOVEP	Move Peripheral Data	STOP	Stop
CHK	Check Register Against Bounds	MULS	Signed Multiply	SUB	Subtract
CLR	Clear Operand	MULU	Unsigned Multiply	SWAP	Swap Data Register Halves
CMP	Compare	NBCD	Negate Decimal with Extend	TAS	Test and Set Operand
DB_{CC}	Test Condition, Decrement and Branch	NEG	Negate	TRAP	Trap
DIVS	Signed Divide	NOP	No Operation	TRAPV	Trap on Overflow
DIVU	Unsigned Divide	NOT	One's Complement	TST	Test
		OR	Logical Or	UNLK	Unlink

VI

VARIATIONS OF INSTRUCTION TYPES

Table 3

Instruction Type	Variation	Description	Instruction Type	Variation	Description
ADD	**ADD**	Add	**MOVE**	**MOVE**	MOVE
	ADDA	Add Address		MOVEA	Move Address
	ADDQ	Add Quick		MOVEQ	Move Quick
	ADDI	Add Immediate		MOVE from SR	Move from Status Register
	ADDX	Add with Extend		MOVE to SR	Move to Status Register
AND	**AND**	Logical And		MOVE to CCR	Move to Condition Codes
	ANDI	And Immediate		MOVE USP	Move User Stack Pointer
CMP	**CMP**	Compare	**NEG**	**NEG**	Negate
	CMPA	Compare Address		NEGX	Negate with Extend
	CMPM	Compare Memory	**OR**	**OR**	Logical Or
	CMPI	Compare Immediate		ORI	Or Immediate
EOR	**EOR**	Exclusive Or	**SUB**	**SUB**	Subtract
	EORI	Exclusive Or Immediate		SUBA	Subtract Address
				SUBI	Subtract Immediate
				SUBQ	Subtract Quick
				SUBX	Subtract with Extend

DATA ORGANIZATION AND ADDRESSING CAPABILITIES

The following paragraphs describe the data organization and addressing capabilities of the MK68000.

OPERAND SIZE

Operand sizes are defined as follows: a byte equals 8 bits, a word equals 16 bits, and a long word equals 32 bits. The operand size for each instruction is either explicitly encoded in the instruction or implicitly defined by the instruction operation. All explicit instructions support byte, word or long word operands. Implicit instructions support some subset of all three sizes.

DATA ORGANIZATION IN REGISTERS

The eight data registers support data operands of 1, 8, 16, or

32 bits. The seven address registers together with the active stack pointer support address operands of 32 bits.

DATA REGISTERS. Each data register is 32 bits wide. Byte operands occupy the low order 8 bits, word operands the low order 16 bits, and long word operands the entire 32 bits. The least significant bit is addressed as bit zero; the most significant bit is addressed as bit 31.

When a data register is used as either a source or destination operand, only the appropriate low-order portion is changed; the remaining high-order portion is neither used nor changed.

ADDRESS REGISTERS. Each address register and the stack pointer is 32 bits wide and holds a full 32 bit address. Address registers do not support byte sized operands. Therefore, when an address register is used as a source operand, either the low order word or the entire long word operand is used depending upon the operation size. When an address register is used as the destination operand, the entire register is affected regardless of the operation size. If the operation size is word, any other operands are sign extended to 32 bits before the operation is performed.

DATA ORGANIZATION IN MEMORY

Bytes are individually addressable with the high order byte having an even address the same as the word, as shown in Figure 1. The low order byte has an odd address that is one count higher than the word address. Instructions and multibyte data are accessed only on word (even byte) boundaries. If a long word datum is located at address n (n even), then the second word of that datum is located at address n + 2.

The data types supported by the MK68000 are: bit data, integer data of 8, 16, or 32 bits, 32-bit addresses and binary coded decimal data. Each of these data types is put in memory, as shown in Figure 2.

ADDRESSING

Instructions for the MK68000 contain two kinds of information: the type of function to be performed, and the location of the operand(s) on which to perform that function. The methods used to locate (address) the operand(s) are explained in the following paragraphs.

Instructions specify an operand location in one of three ways:

Register Specification - the number of the register is given in the register field of the instruction.
Effective Address - use of the different effective address modes.
Implicit Reference - the definition of certain instructions implies the use of specific registers.

INSTRUCTION FORMAT

Instructions are from one to five words in length, as shown in Figure 3. The length of the instruction and the operation to be performed is specified by the first word of the instruction which is called the operation word. The remaining words further specify the operands. These words are either immediate operands or extensions to the effective address mode specified in the operation word.

PROGRAM/DATA REFERENCES

The MK68000 separates memory references into two classes: program references, and data references. Program references, as the name implies, are references to that section of memory that contains the program being executed. Data references refer to that section of memory that contains data. Generally, operand reads are from the data space. All operand writes are to the data space.

REGISTER SPECIFICATION

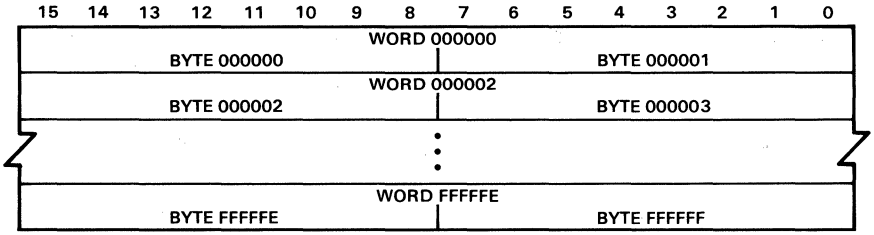
The register field within an instruction specifies the register to be used. Other fields within the instruction specify whether the register selected is an address or data register and how the register is to be used.

EFFECTIVE ADDRESS

Most instructions specify the location of an operand by using the effective address field in the operation word. For example, Figure 4 shows the general format of the single effective address instruction operation word. The effective address is composed of two 3-bit fields: the mode field, and the register field. The value in the mode field selects the

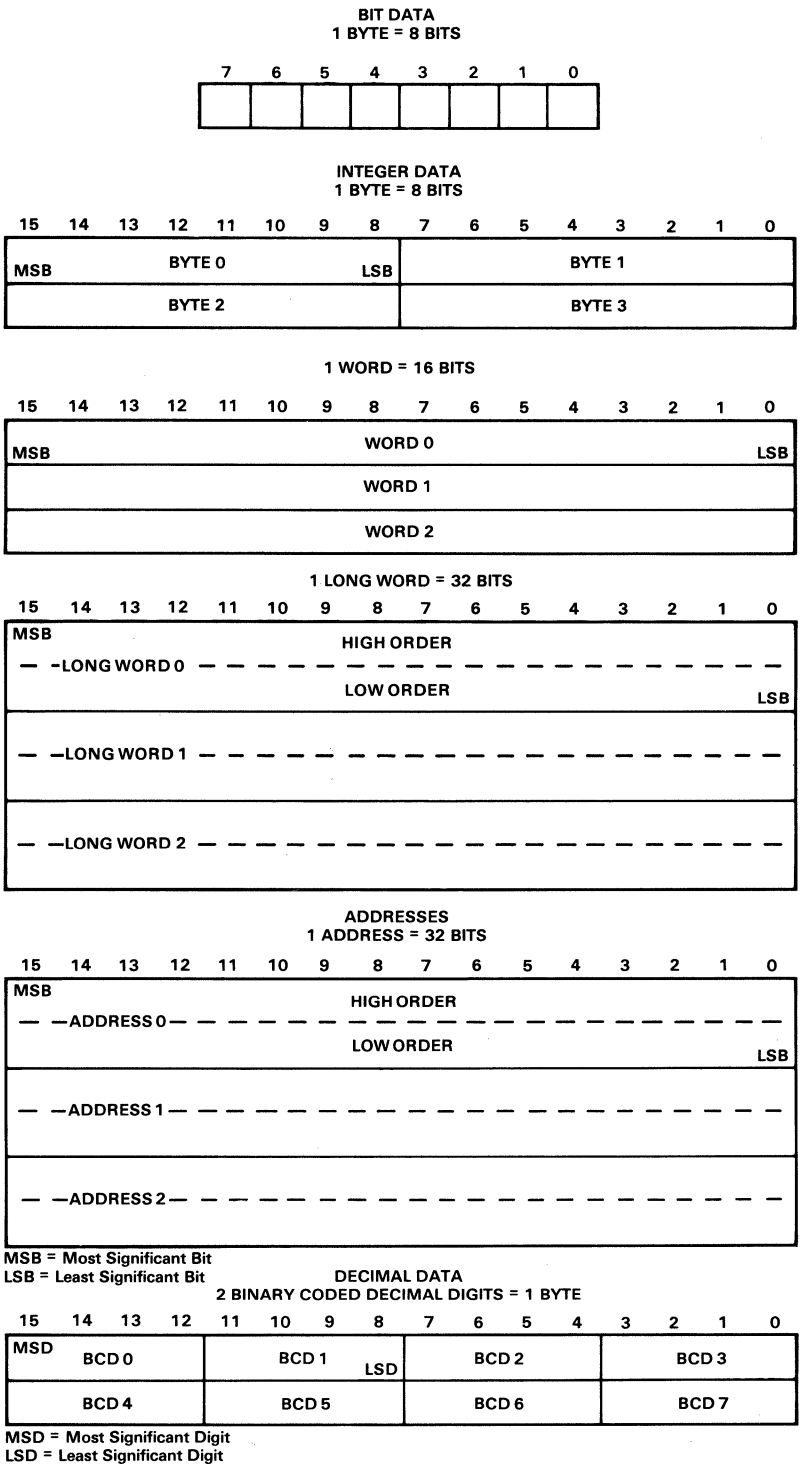
WORD ORGANIZATION IN MEMORY

Figure 1



DATA ORGANIZATION IN MEMORY

Figure 2



different address modes. The register field contains the number of a register.

The effective address field may require additional information to fully specify the operand. This additional information, called the effective address extension, is contained in the following word or words and is considered part of the instruction, as shown in Figure 3. The effective address modes are grouped into three categories: register direct, memory addressing, and special.

REGISTER DIRECT MODES

These effective addressing modes specify that the operand is in one of the 16 multifunction registers.

Data Register Direct. The operand is in the data register specified by the effective address register field.

Address Register Direct. The operand is in the address register specified by the effective address register field.

MEMORY ADDRESS MODES

These effective addressing modes specify that the operand is in memory and provide the specific address of the operand.

Address Register Indirect. The address of the operand is in the address register specified by the register field. The reference is classified as a data reference with the exception of the jump and jump to subroutine instructions.

Address Register Indirect With Postincrement. The address of the operand is in the address register specified by the register field. After the operand address is used, it is incremented by one, two, or four depending upon whether the size of the operand is byte, word, or long word. If the address register is the stack pointer and the operand size is byte, the address is incremented by two rather than one to keep the stack pointer on a word boundary. The reference is classified as a data reference.

Address Register Indirect With Predecrement. The address of the operand is in the address register specified by the register field. Before the operand address is used, it is decremented by one, two, or four depending upon whether the operand size is byte, word, or long word. If the address register is the stack pointer and the operand size is byte, the address is decremented by two rather than one to keep the stack pointer on a word boundary. The reference is classified as a data reference.

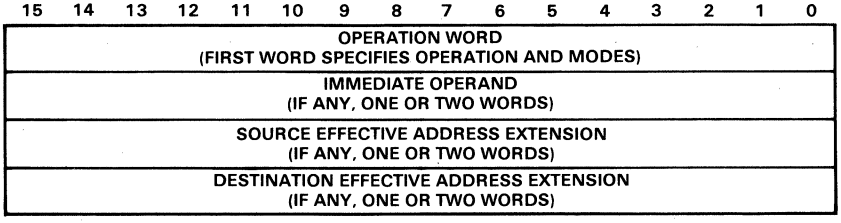
Address Register Indirect With Displacement. This address mode requires one word of extension. The address of the operand is the sum of the address in the address register and the sign-extended 16-bit displacement integer in the extension word. The reference is classified as a data reference with the exception of the jump and jump to subroutine instructions.

Address Register Indirect With Index. This address mode requires one word of extension. The address of the operand is the sum of the address in the address register, the sign-extended displacement integer in the low order eight bits of the extension word, and the contents of the index register. The reference is classified as a data reference with the exception of the jump and jump to subroutine instructions.

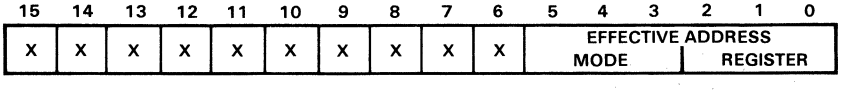
SPECIAL ADDRESS MODES

The special address modes use the effective address

INSTRUCTION FORMAT
Figure 3



SINGLE-EFFECTIVE-ADDRESS INSTRUCTION OPERATION WORD GENERAL FORMAT
Figure 4



register field to specify the special addressing mode instead of a register number.

Absolute Short Address. This address mode requires one word of extension. The address of the operand is the extension word. The 16-bit address is sign extended before it is used. The reference is classified as a data reference with the exception of the jump and jump to subroutine instructions.

Absolute Long Address. This address mode requires two words of extension. The address of the operand is developed by the concatenation of the extension words. The high-order part of the address is the first extension word; the low-order part of the address is the second extension word. The reference is classified as a data reference with the exception of the jump and jump to subroutine instructions.

Program Counter With Displacement. This address mode requires one word of extension. The address of the operand is the sum of the address in the program counter and the sign-extended 16-bit displacement integer in the extension word. The value in the program counter is the address of the extension word. The reference is classified as a program reference.

Program Counter With Index. This address mode requires one word of extension. The address is the sum of the address in the program counter, the sign-extended displacement integer in the lower eight bits of the extension word, and the contents of the index register. The value in the program counter is the address of the extension word. This reference is classified as a program reference.

Immediate Data. This address mode requires either one or two words of extension depending on the size of the operation.

Byte operation - operand is low order byte of extension word
Word operation - operand is extension word
Long word operation - operand is in the two extension words, high-order 16 bits are in the first extension word, low-order 16 bits are in the second extension word.

EFFECTIVE ADDRESS ENCODING SUMMARY

Table 4

Addressing Mode	Mode	Register
Data Register Direct	000	register number
Address Register Direct	001	register number
Address Register Indirect	010	register number
Address Register Indirect with Postincrement	011	register number
Address Register Indirect with Predecrement	100	register number
Address Register Indirect with Displacement	101	register number
Address Register Indirect with Index	110	register number
Absolute Short	111	000
Absolute Long	111	001
Program Counter with Displacement	111	010
Program Counter with Index	111	011
Immediate or Status Register	111	100

IMPLICIT INSTRUCTION REFERENCE SUMMARY

Table 5

Instruction	Implied Register(s)
Branch Conditional (B_{CC}), Branch Always (BRA)	PC
Branch to Subroutine (BSR)	PC, SP
Check Register against Bounds (CHK)	SSP, SR
Test Condition, Decrement and Branch (DB_{CC})	PC
Signed Divide (DIVS)	SSP, SR
Unsigned Divide (DIVU)	SSP, SR
Jump (JMP)	PC
Jump to Subroutine (JSR)	PC, SP
Link and Allocate (LINK)	SP
Move Condition Codes (MOVE CCR)	SR
Move Status Register (MOVE SR)	SR
Move User Stack Pointer (MOVE USP)	USP
Push Effective Address (PEA)	SP
Return from Exception (RTE)	PC, SP, SR
Return and Restore Condition Codes (RTR)	PC, SP, SR
Return from Subroutine (RTS)	PC, SP
Trap (TRAP)	SSP, SR
Trap on Overflow (TRAPV)	SSP, SR
Unlink (UNLK)	SP

Condition Codes or Status Register. A selected set of instructions may reference the status register by means of the effective address field. These are:

ANDI to CCR
ANDI to SR
EORI to CCR
EORI to SR
ORI to CCR
ORI to SR

EFFECTIVE ADDRESS ENCODING SUMMARY

Table 4 is a summary of the effective addressing modes discussed in the previous paragraphs.

IMPLICIT REFERENCE

Some instructions make implicit reference to the program counter (PC), the system stack pointer (SP), the supervisor stack pointer (SSP), the user stack pointer (USP), or the status register (SR). Table 5 provides a list of these instructions and the registers implied.

SYSTEM STACK

The system stack is used implicitly by many instructions; user stacks and queues may be created and maintained through the addressing modes. Address register seven (A7) is the system stack pointer (SP). The system stack pointer is either the supervisor stack pointer (SSP) or the user stack pointer (USP), depending on the state of the S-bit in the status register. If the S-bit indicates supervisor state, SSP is the active system stack pointer, and the USP cannot be referenced as an address register. If the S-bit indicates user state, the USP is the active system stack pointer, and the SSP cannot be referenced. Each system stack fills from high memory to low memory.

INSTRUCTION SET SUMMARY

The following paragraphs contain an overview of the form and structure of the MK68000 instruction set. The instructions form a set of tools that include all the machine functions to perform the following operations:

Data Movement
Integer Arithmetic
Logical
Shift and Rotate
Bit Manipulation
Binary Coded Decimal
Program Control
System Control

The complete range of instruction capabilities combined with the flexible addressing modes described previously provide a very flexible base for program development.

DATA MOVEMENT OPERATIONS

The basic method of data acquisition (transfer and storage) is provided by the move (MOVE) instruction. The move instruction and the effective addressing modes allow both address and data manipulation. Data move instructions allow byte, word, and long word operands to be transferred from memory to memory, memory to register, register to memory, and register to register. Address move instructions allow word and long word operand transfers and ensure that only legal address manipulations are executed. In addition to the general move instruction there are several special data movement instructions: move multiple registers (MOVEM), move peripheral data (MOVEP), exchange registers (EXG), load effective address (LEA), push effective address (PEA), link stack (LINK), unlink stack (UNLK), and move quick (MOVEQ). Table 6 is a summary of the data movement operations.

DATA MOVEMENT OPERATIONS

Table 6

Instruction	Operand Size	Operation
EXG	32	Rx ↔ Ry
LEA	32	EA → An
LINK	-	An → SP @ - SP → An SP + d → SP
MOVE	8, 16, 32	(EA)s → EAd
MOVEM	16, 32	(EA) → An, Dn An, Dn → EA
MOVEP	16, 32	(EA) → Dn Dn → EA
MOVEQ	8	#xxx → Dn
PEA	32	EA → SP @ -
SWAP	32	Dn[31:16]↔Dn[15:0]
UNLK	-	An → Sp SP @ + → An

NOTES:

s = source
d = destination
[ ] = bit numbers
@ - = indirect with predecrement
@ + = indirect with postincrement

INTEGER ARITHMETIC OPERATIONS

The arithmetic operations include the four basic operations of add (ADD), subtract (SUB), multiply (MUL), and divide (DIV) as well as arithmetic compare (CMP), clear (CLR), and negate (NEG). The add and subtract instructions are available for both address and data operations, with data operations accepting all operand sizes. Address operations are limited to legal address size operands (16 or 32 bits). Data, address, and memory compare operations are also available. The clear and negate instructions may be used on all sizes of data operands.

The multiply and divide operations are available for signed and unsigned operands using word multiply to produce a long word product, and a long word dividend with word divisor to produce a word quotient with a word remainder.

Multiprecision and mixed size arithmetic can be accomplished using a set of extended instructions. These instructions are: add extended (ADDX), subtract extended (SUBX), sign extend (EXT), and negate binary with extend (NEGX).

A test operand (TST) instruction that will set the condition codes as a result of a compare of the operand with zero is also available. Test and set (TAS) is a synchronization instruction useful in multiprocessor systems. Table 7 is a summary of the integer arithmetic operations.

INTEGER ARITHMETIC OPERATIONS

Table 7

Instruction	Operand Size	Operation
ADD	8, 16, 32 16, 32	Dn + (EA) → Dn (EA) + Dn → EA (EA) + #xxx → EA An + (EA) → An
ADDX	8, 16, 32 16, 32	Dx + Dy + X → Dx Ax@ - Ay@ - + X → Ax@
CLR	8, 16, 32	0 → EA
CMP	8, 16, 32 16, 32	Dn - (EA) (EA) - #xxx Ax@ + - Ay@ + An - (EA)
DIVS	32 ÷ 16	Dn/(EA) → Dn
DIVU	32 ÷ 16	Dn/(EA) → Dn
EXT	8 → 16 16 → 32	$(Dn)_8 \rightarrow Dn_{16}$ $(Dn)_{16} \rightarrow Dn_{32}$
MULS	16* 16 → 32	Dn* (EA) → Dn
MULU	16* 16 → 32	Dn* (EA) → Dn
NEG	8, 16, 32	0 - (EA) → EA
NEGX	8, 16, 32	0 - (EA) - X - EA
SUB	8, 16, 32 16, 32	Dn - (EA) → Dn (EA) - Dn → EA (EA) - #xxx → EA An - (EA) → An
SUBX	8, 16, 32	Dx - Dy - X → Dx Ax@ - - Ay@ - - X → Ax@
TAS	8	(EA) - 0, 1 → EA[7]
TST	8, 16, 32	(EA) - 0

NOTE: [ ] = bit number

LOGICAL OPERATIONS

Logical operation instructions AND, OR, EOR, and NOT are available for all sizes of integer data operands. A similar set of immediate instructions (ANDI, ORI, and EORI) provides these logical operations with all sizes of immediate data. Table 8 is a summary of the logical operations.

LOGICAL OPERATIONS

Table 8

Instruction	Operand Size	Operation
AND	8, 16, 32	Dn∧(EA) → Dn (EA)∧Dn → EA (EA)∧#xxx → EA
OR	8, 16, 32	Dn v (EA) → Dn (EA) v Dn → EA (EA) v #xxx → EA
EOR	8, 16, 32	(EA) ⊕ Dy → EA (EA) ⊕ #xxx → EA
NOT	8, 16, 32	~ (EA) → EA

NOTE: ~ = invert

SHIFT AND ROTATE OPERATIONS

Shift operations in both directions are provided by the arithmetic instructions ASR and ASL and logical shift instructions LSR and LSL. The rotate instructions (with and without extend) available are ROXR, ROXL, ROR, and ROL. All shift and rotate operations can be performed in either registers or memory. Register shifts and rotates support all operand sizes and allow a shift count specified in the instruction of one to eight bits, or 0 to 63 specified in a data register.

Memory shifts and rotates are for word operands only and allow only single-bit shifts or rotates.

Table 9 is a summary of the shift and rotate operations.

BIT MANIPULATION OPERATIONS

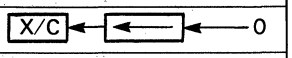
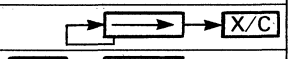
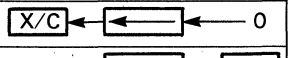
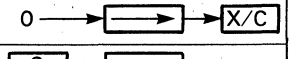
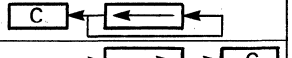
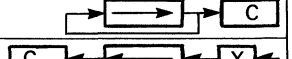
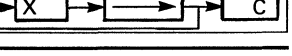
Bit manipulation operations are accomplished using the following instructions: bit test (BTST), bit test and set (BSET), bit test and clear (BCLR), and bit test and change (BCHG). Table 10 is a summary of the bit manipulation operations. (Bit 2 of the status register is Z.)

BINARY CODED DECIMAL OPERATIONS

Multiprecision arithmetic operations on binary coded decimal numbers are accompolished using the following instructions: add decimal with extend (ABCD), subtract decimal with extend (SBCD), and negate decimal with extend (NBCD). Table 11 is a summary of the binary coded decimal operations.

SHIFT AND ROTATE OPERATIONS

Table 9

Instruction	Operand Size	Operation
ASL	8, 16, 32	
ASR	8, 16, 32	
LSL	8, 16, 32	
LSR	8, 16, 32	
ROL	8, 16, 32	
ROR	8, 16, 32	
ROXL	8, 16, 32	
ROXR	8, 16, 32	

BIT MANIPULATION OPERATIONS

Table 10

Instruction	Operand Size	Operation
BTST	8, 32	~ bit of (EA) → Z
BSET	8, 32	~ bit of (EA) → Z 1 → bit of EA
BCLR	8, 32	~ bit of (EA) → Z 0 → bit of EA
BCHG	8, 32	~ bit of (EA) → Z ~ bit of (EA) → bit of EA

BINARY CODED DECIMAL OPERATIONS

Table 11

Instruction	Operand Size	Operation
ABCD	8	$Dx_{10}+Dy_{10}+X \rightarrow Dx$ Ax@ - 10+Ay@ - 10+X → Ax@
SBCD	8	$Dx_{10} - Dy_{10} - X \rightarrow Dx$ Ax@ - 10 - Ay@ - 10 - X → Ax@
NBCD	8	$0 - (EA)_{10} - X \rightarrow EA$

PROGRAM CONTROL OPERATIONS

Program control operations are accomplished using a series of conditional and unconditional branch instructions and return instructions. These instructions are summarized in Table 12.

The conditional instructions provide setting and branching for the following conditions:

CC - carry clear	LS - low or same
CS - carry set	LT - less than
EQ - equal	MI - minus
F - never true	NE - not equal
GE - greater or equal	PL - plus
GT - greater than	T - always true
HI - high	VC - no overflow
LE - less or equal	VS - overflow

PROGRAM CONTROL OPERATIONS

Table 12

Instruction	Operation
Conditional	
B_{CC}	Branch conditionally (14 conditions) 8- and 16-bit displacement
DB_{CC}	Test condition, decrement, and branch 16-bit displacement
S_{CC}	Set byte conditionally (16 conditions)
Unconditional	
BRA	Branch always 8- and 16-bit displacement
BSR	Branch to subroutine 8- and 16-bit displacement
JMP	Jump
JSR	Jump to subroutine
Returns	
RTR	Return and restore condition codes
RTS	Return from subroutine

SYSTEM CONTROL OPERATIONS

System control operations are accomplished by using privileged instructions, trap generating instructions, and instructions that use or modify the status register. These instructions are summarized in Table 13.

SIGNAL AND BUS OPERATION DESCRIPTION

The following paragraphs contain a brief description of the input and output signals. A discussion of bus operation during the various machine cycles and operations is also given.

SIGNAL DESCRIPTION

The input and output signals can be functionally organized into the groups shown in Figure 5. The following paragraphs provide a brief description of the signals and also a reference (if applicable) to other paragraphs that contain more detail about the function being performed.

ADDRESS BUS (A1 THROUGH A23). This 23-bit, unidirectional, three-state bus is capable of addressing 8 megawords of data. It provides the address for bus operation during all cycles except interrupt cycles. During interrupt cycles, address lines A1, A2, and A3 provide

information about what level interrupt is being serviced while address lines A4 through A23 are all set to a logic high.

DATA BUS (D0 THROUGH D15). This 16-bit bidirectional, three-state bus is the general purpose data path. It can transfer and accept data in either word or byte length. During an interrupt acknowledge cycle, the external device supplies the vector number on data lines D0-D7.

ASYNCHRONOUS BUS CONTROL. Asynchronous data transfers are handled using the following control signals: address strobe, read/write, upper and lower data strobes, and data transfer acknowledge. These signals are explained in the following paragraphs.

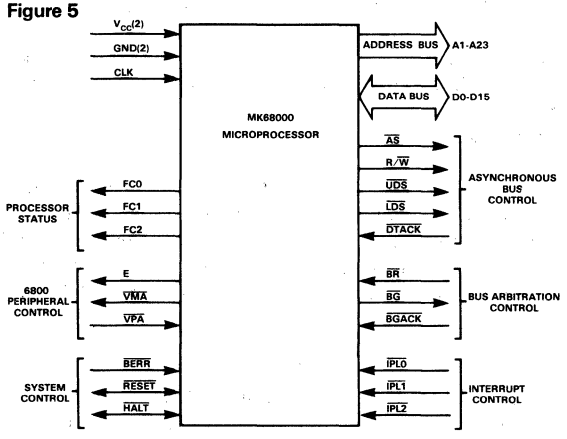
SYSTEM CONTROL OPERATIONS

Table 13

Instruction	Operation
Privileged	
RESET	Reset external devices
RTE	Return from exception
STOP	Stop program execution
ORI to SR	Logical OR to status register
MOVE USP	Move user stack pointer
ANDI to SR	Logical AND to status register
EORI to SR	Logical EOR to status register
MOVE EA to SR	Load new status register
Trap Generating	
TRAP	Trap
TRAPV	Trap on overflow
CHK	Check register against bounds
Status Register	
ANDI to CCR	Logical AND to condition codes
EORI to CCR	Logical EOR to condition codes
MOVE EA to CCR	Load new condition codes
ORI to CCR	Logical OR to condition codes
MOVE SR to EA	Store status register

INPUT AND OUTPUT SIGNALS

Figure 5



Address Strobe ($\overline{AS}$). This signal indicates that there is a valid address on the address bus.

Read/Write (R/$\overline{W}$). This signal defines the data bus transfer as a read or write cycle. The R/$\overline{W}$ signal also works in conjunction with the upper and lower data strobes as explained in the following paragraph.

Upper And Lower Data Strobes ($\overline{UDS}$, $\overline{LDS}$). These signals control the data on the data bus, as shown in Table 14. When the R/$\overline{W}$ line is high, the processor will read from the data bus as indicated. When the R/$\overline{W}$ line is low, the processor will write to the data bus as shown.

DATA STROBE CONTROL OF DATA BUS

Table 14

$\overline{UDS}$	$\overline{LDS}$	R/$\overline{W}$	D8-D15	D0-D7
High	High	-	No valid data	No valid data
Low	Low	High	Valid data bits 8-15	Valid data bits 0-7
High	Low	High	No valid data	Valid data bits 0-7
Low	High	High	Valid data bits 8-15	No valid data
Low	Low	Low	Valid data bits 8-15	Valid data bits 0-7
High	Low	Low	Valid data bits 0-7*	Valid data bits 0-7
Low	High	Low	Valid data bits 8-15	Valid data bits 8-15*

*These conditions are a result of current implementation and may not appear on future devices.

Data Transfer Acknowledge ($\overline{DTACK}$). This input indicates that the data transfer is completed. When the processor recognizes $\overline{DTACK}$ during a read cycle, data is latched and the bus cycle terminated. When $\overline{DTACK}$ is recognized during a write cycle, the bus cycle is terminated.

An active transition of data transfer acknowledge, $\overline{DTACK}$, indicates the termination of a data transfer on the bus.

If the system must run at a maximum rate determined by RAM access times, the relationship between the times at which $\overline{DTACK}$ and DATA are sampled are important.

All control and data lines are sampled during the MK68000's clock high time. The clock is internally buffered, which results in some slight differences in the sampling and recognition of various signals. The $\overline{DTACK}$ signal, like other

VI

control signals, is internally synchronized to allow for valid operation in an asynchronous system. If the required setup time (#47) is met during S4, $\overline{DTACK}$ will be recognized during S5 and S6, and data will be captured during S6. The data must meet the required setup time (#27).

If an asynchronous control signal does not meet the required setup time, it is possible that it may not be recognized during that cycle. Because of this, asynchronous systems must not allow $\overline{DTACK}$ to precede data by more than parameter #31.

Asserting $\overline{DTACK}$ (or $\overline{BERR}$) on the rising edge of a clock (such as S4) after the assertion of address strobe will allow an MK68000 system to run at its maximum bus rate. If setup times #27 and #47 are guaranteed, #31 may be ignored.

BUS ARBITRATION CONTROL. These three signals form a bus arbitration circuit to determine which device will be the bus master device.

Bus Request ($\overline{BR}$). This input is write ORed with all other devices that could be bus masters. This input indicates to the processor that some other device desires to become the bus master.

Bus Grant ($\overline{BG}$). This output indicates to all other potential bus master devices that the processor will release bus control at the end of the current bus cycle.

Bus Grant Acknowledge ($\overline{BGACK}$). This input indicates that some other device has become the bus master. This signal cannot be asserted until the following four conditions are met:

1. a bus grant has been received
2. address strobe is inactive which indicates that the microprocessor is not using the bus
3. data transfer acknowledge is inactive which indicates that either memory or the peripherals are not using the bus
4. bus grant acknowledge is inactive which indicates that no other device is still claiming bus mastership

INTERRUPT CONTROL ($\overline{IPL0}$, $\overline{IPL1}$, $\overline{IPL2}$). These input pins indicate the encoded priority level of the device requesting an interrupt. Level seven is the highest priority while level zero indicates that no interrupts are requested. The least significant bit is given in $\overline{IPL0}$ and the most significant bit is contained in $\overline{IPL2}$.

SYSTEM CONTROL. The system control inputs are used to either reset or halt the processor and to indicate to the processor that bus errors have occurred. The three system control inputs are explained in the following paragraphs.

Bus Error ($\overline{BERR}$). This input informs the processor that there is a problem with the cycle currently being executed. Problems may be a result of:

1. nonresponding devices
2. interrupt vector number acquisition failure
3. illegal access request as determined by a memory management unit
4. other application dependent errors.

The bus error signal interacts with the halt signal to determine if exception processing should be performed or the current bus cycle should be retried.

Refer to BUS ERROR AND HALT OPERATION paragraph for additional information about the interaction of the bus error and halt signals.

Reset ($\overline{RESET}$). This bidirectional signal line acts to reset (initiate a system initialization sequence) the processor in response to an external reset signal. An internally generated reset (result of RESET instruction) causes all external devices to be reset and the internal state of the processor is not affected. A total system reset (processor and external devices) is the result of external halt and reset signals applied at the same time. Refer to RESET OPERATION paragraph for additional information about reset operation.

Halt ($\overline{HALT}$). When this bidirectional line is driven by an external device, it will cause the processor to stop at the completion of the current bus cycle. When the processor has been halted using this input, all control signals are inactive and all three-state lines are put in their high-impedance state. Refer to BUS ERROR AND HALT OPERATION paragraph for additional information about the interaction between the halt and bus error signals.

When the processor has stopped executing instructions, such as in a double bus fault condition, the halt line is driven by the processor to indicate to external devices that the processor has stopped.

6800 PERIPHERAL CONTROL. These control signals are used to allow the interfacing of synchronous 6800 peripheral devices with the asynchronous MK68000. These signals are explained in the following paragraphs.

Enable (E). This signal is the standard enable signal common to all 6800 type peripheral devices. The period for this output is ten MK68000 clock periods (six clocks low; four clocks high).

Valid Peripheral Address ($\overline{VPA}$). This input indicates that the device or region addressed is a 6800 family device and that data transfer should be synchronized with the enable (E) signal. This input also indicates that the processor should use automatic vectoring for an interrupt. Refer to INTERFACE WITH 6800 PERIPHERALS.

Valid Memory Address ($\overline{VMA}$). This output is used to indicate to 6800 peripheral devices that there is a valid address on the address bus and the processor is

FUNCTION CODE OUTPUTS

Table 15

FC2	FC1	FC0	Cycle Type
Low	Low	Low	(Undefined, Reserved)
Low	Low	High	User Data
Low	High	Low	User Program
Low	High	High	(Undefined, Reserved)
High	Low	Low	(Undefined, Reserved)
High	Low	High	Supervisor Data
High	High	Low	Supervisor Program
High	High	High	Interrupt Acknowledge

synchronized to enable. This signal only responds to a valid peripheral address ($\overline{VPA}$) input which indicates that the peripheral is a 6800 family device.

PROCESSOR STATUS (FC0, FC1, FC2). These function code outputs indicate the state (user or supervisor) and the cycle type currently being executed, as shown in Table 15. The information indicated by the function code outputs is valid whenever address strobe ($\overline{AS}$) is active.

CLOCK (CLK). The clock input is a TTL compatible signal that is internally buffered for development of the internal clocks needed by the processor. The clock input shall be a constant frequency.

SIGNAL SUMMARY. Table 16 is a summary of all the signals discussed in the previous paragraphs.

SIGNAL SUMMARY

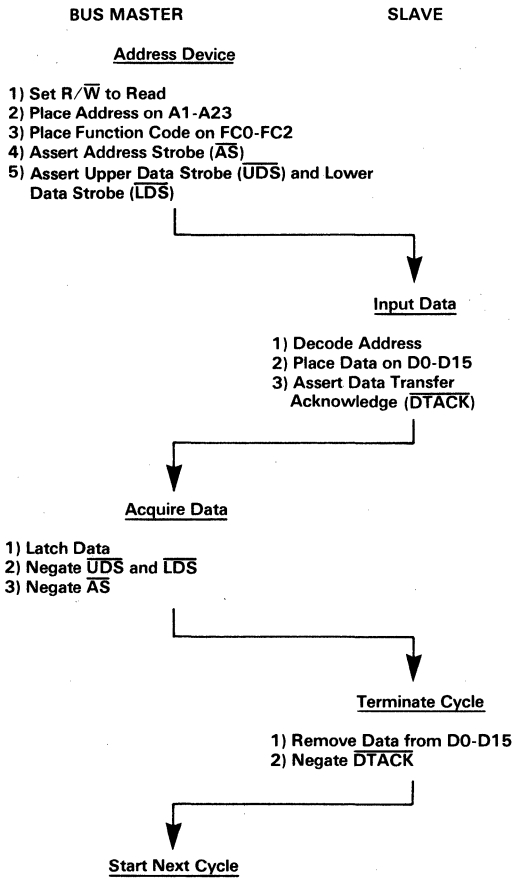
Table 16

Signal Name	Mnemonic	Input/Output	Active State	Three State
Address Bus	A1-A23	output	high	yes
Data Bus	D0-D15	input/output	high	yes
Address Strobe	$\overline{AS}$	output	low	yes
Read/Write	R/$\overline{W}$	output	read-high write-low	yes
Upper and Lower Data Strobes	$\overline{UDS}$, $\overline{LDS}$	output	low	yes
Data Transfer Acknowledge	$\overline{DTACK}$	input	low	no
Bus Request	$\overline{BR}$	input	low	no
Bus Grant	$\overline{BG}$	output	low	no
Bus Grant Acknowledge	$\overline{BGACK}$	input	low	no
Interrupt Priority Level	$\overline{IPL0}$, $\overline{IPL1}$, $\overline{IPL2}$	input	low	no
Bus Error	$\overline{BERR}$	input	low	no
Reset	$\overline{RESET}$	input/output	low	no*
Halt	$\overline{HALT}$	input/output	low	no*
Enable	E	output	high	no
Valid Memory Address	$\overline{VMA}$	output	low	yes
Valid Peripheral Address	$\overline{VPA}$	input	low	no
Function Code Output	FC0, FC1, FC2	output	high	yes
Clock	CLK	input	high	no
Power Input	V_{CC}	input	—	—
Ground	GND	input	—	—

* open drain

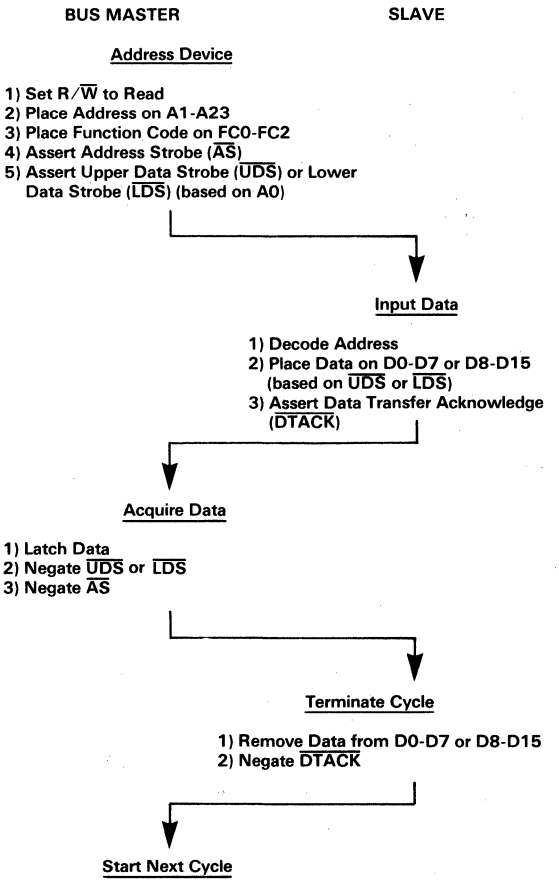
WORD READ CYCLE FLOW CHART

Figure 6



BYTE READ CYCLE FLOW CHART

Figure 7



BUS OPERATION

The following paragraphs explain control signal and bus operation during data transfer operations, bus arbitration, bus error and halt conditions, and reset operation.

DATA TRANSFER OPERATIONS. Transfer of data between devices involves the following leads:

- Address Bus A1 through A23
- Data Bus D0 through D15
- Control Signals

The address and data buses are separate parallel buses used to transfer data using an asynchronous bus structure. In all cycles, the bus master assumes responsibility for deskewing all signals it issues at both the start and end of a cycle. In addition, the bus master is responsible for deskewing the acknowledge and data signals from the slave device.

The following paragraphs explain the read, write, and read-modify-write cycles. The indivisible read-modify-write cycle is the method used by the MK68000 for interlocked multiprocessor communications.

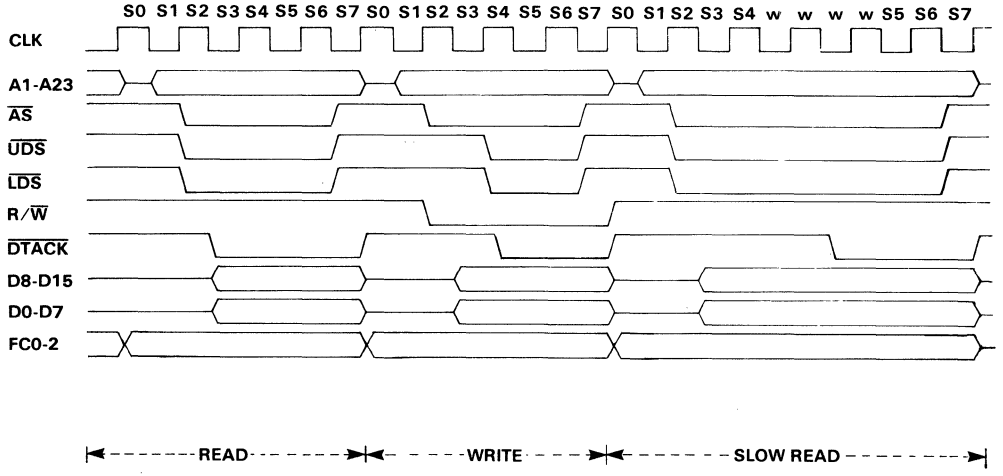
NOTE

The terms assertion and negation will be used extensively. This is done to avoid confusion when dealing with a mixture of "active-low" and "active-high" signals. The term assert or assertion is used to indicate that a signal is active or true independent of whether that voltage is low or high. The term negate or negation is used to indicate that a signal is inactive or false.

Read Cycle. During a read cycle, the processor receives data from memory or a peripheral device. The processor reads bytes of data in all cases. If the instruction specifies a word (or double word) operation, the processor reads both bytes. When the instruction specifies byte operation, the processor uses an internal A0 bit to determine which byte to read and then issues the data strobe required for that byte. For byte operations, when the A0 bit equals zero, the upper data strobe is issued. When the A0 bit equals one, the lower

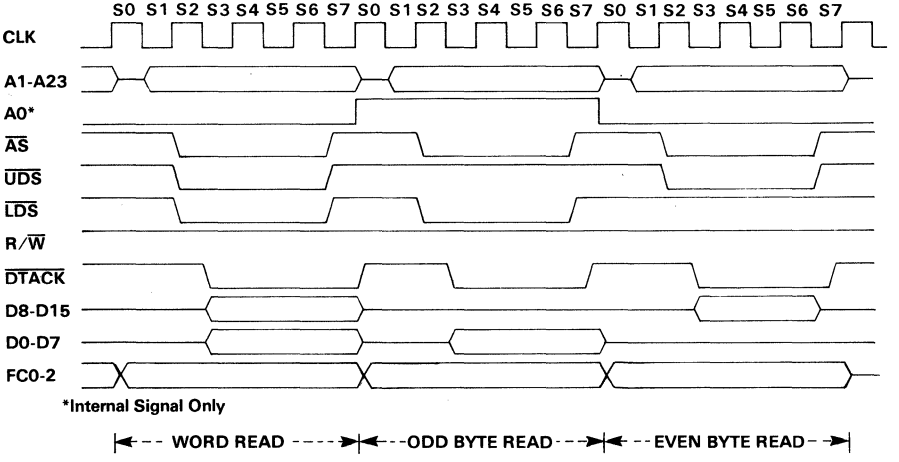
READ AND WRITE CYCLE TIMING DIAGRAM

Figure 8



WORD AND BYTE READ CYCLE TIMING DIAGRAM

Figure 9



data strobe is issued. When the data is received, the processor correctly positions it internally.

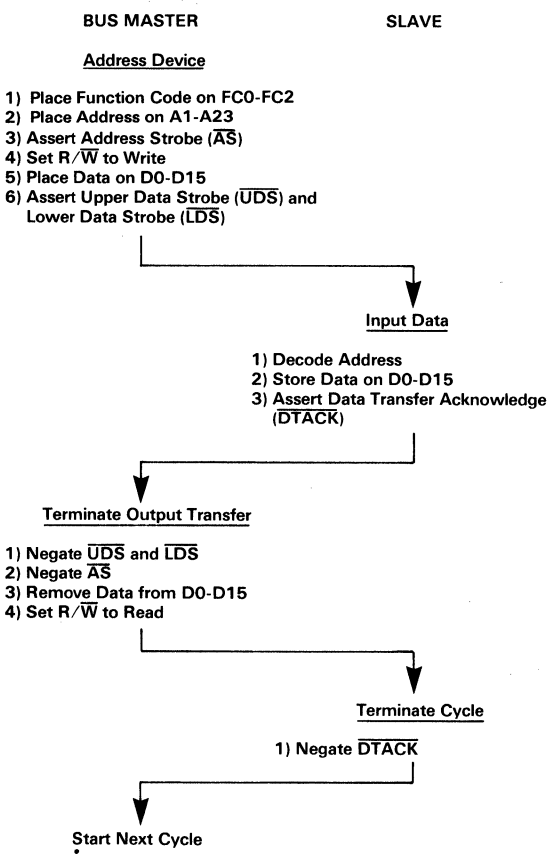
A word read cycle flow chart is given in Figure 6. A byte read cycle flow chart is given in Figure 7. Read cycle timing is given in Figure 8 and Figure 9 details word and byte read cycle operation.

Write Cycle. During a write cycle, the processor sends data to memory or a peripheral device. The processor writes bytes of data in all cases. If the instruction specifies a word operation, the processor writes both bytes. When the instruction specifies a byte operation, the processor uses an internal A0 bit to determine which byte to write and then issues the data strobe required for that byte. For byte operations, when the A0 bit equals zero, the upper data strobe is issued. When the A0 bit equals one, the lower data strobe is issued. A word write cycle flow chart is given in Figure 10. A byte write cycle flow chart is given in Figure 11. Write cycle timing is given in Figure 8 and Figure 12 details word and byte write cycle operation.

Read-Modify-Write Cycle. The read-modify-write cycle performs a read, modifies the data in the arithmetic-logic unit, and writes the data back to the same address. In the MK68000 this cycle is indivisible in that the address strobe is asserted throughout the entire cycle. The test and set (TAS) instruction uses this cycle to provide meaningful communication between processors in a multiple processor environment. This instruction is the only instruction that uses the read-modify-write cycles and since the test and set instruction only operates on bytes, all read-modify-write

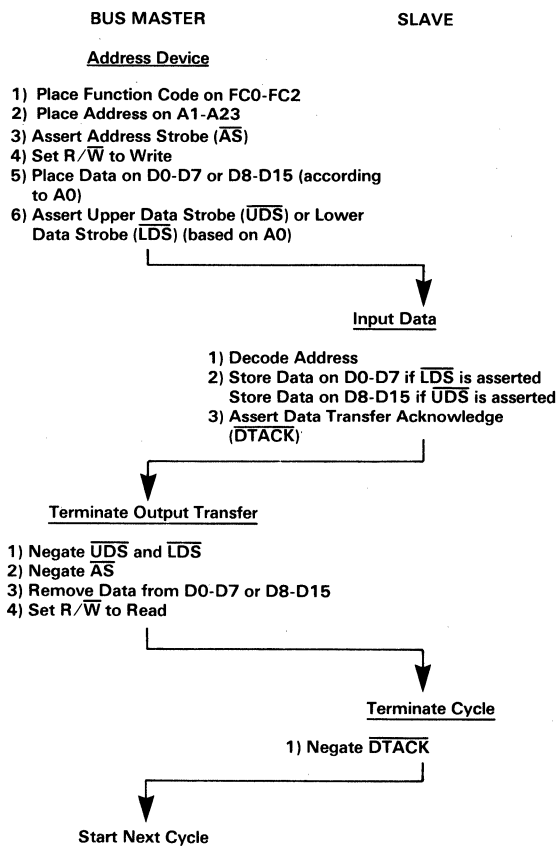
WORD WRITE CYCLE FLOW CHART

Figure 10



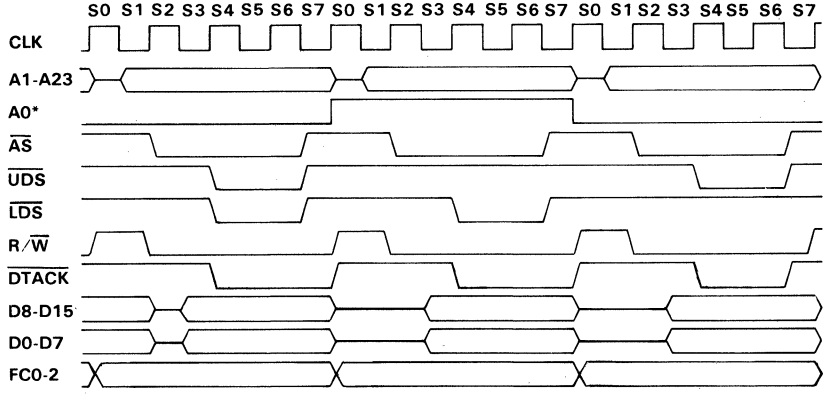
BYTE WRITE CYCLE FLOW CHART

Figure 11



WORD AND BYTE WRITE CYCLE TIMING DIAGRAM

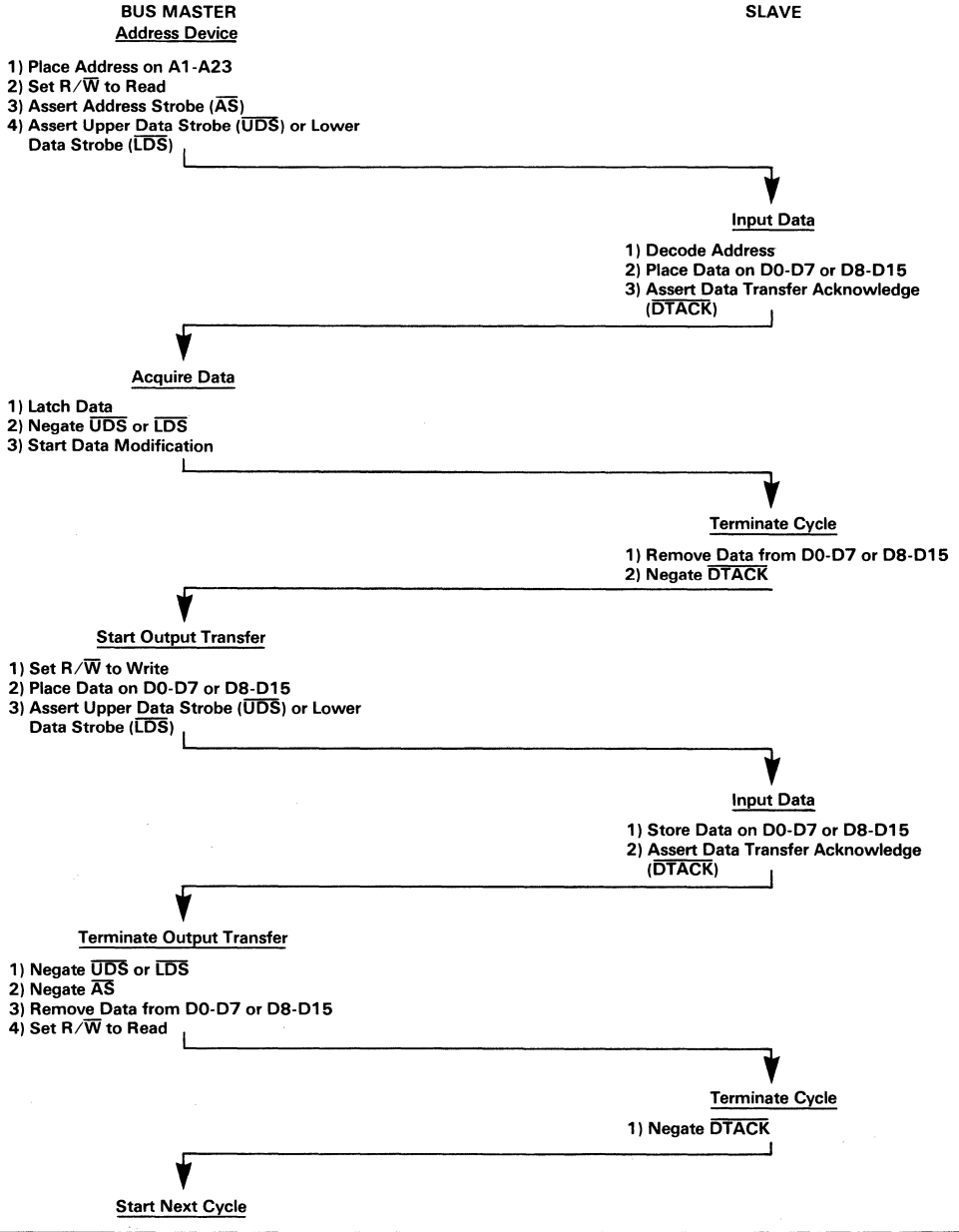
Figure 12



*Internal Signal Only

READ-MODIFY-WRITE CYCLE FLOW CHART

Figure 13



cycles are byte operations. A read-modify-write cycle flow chart is given in Figure 13 and a timing diagram is given in Figure 14.

BUS ARBITRATION. Bus arbitration is a technique used by master-type devices to request, be granted, and acknowledge bus mastership. In its simplest form, it consists of:

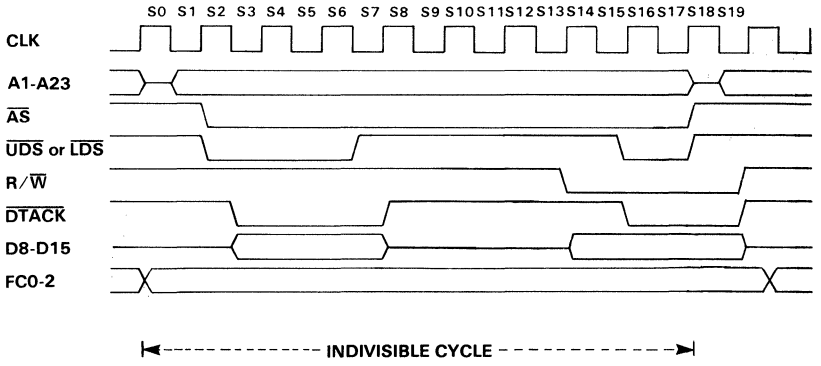
1. Asserting a bus mastership request.
2. Receiving a grant that the bus is available at the end of the current cycle.
3. Acknowledging that mastership has been assumed.

Figure 15 is a flow chart showing the detail involved in a request from a single device. Figure 16 is a timing diagram for the same operations. This technique allows processing of bus requests during data transfer cycles.

The timing diagram shows that the bus request is negated

READ—MODIFY-WRITE CYCLE TIMING DIAGRAM

Figure 14



at the time that an acknowledge is asserted. This type of operation would be true for a system consisting of the processor and one device capable of bus mastership. In systems having a number of devices capable of bus mastership, the bus request line from each device is wire ORed to the processor. In this system, it is easy to see that there could be more than one bus request being made. The timing diagram shows that the bus grant signal is negated a few clock cycles after the transition of the acknowledge (BGACK) signal.

However, if the bus requests are still pending, the processor will assert another bus grant within a few clock cycles after it was negated. This additional assertion of bus grant allows external arbitration circuitry to select the next bus master before the current bus master has completed its requirements. The following paragraphs provide additional information about the three steps in the arbitration process.

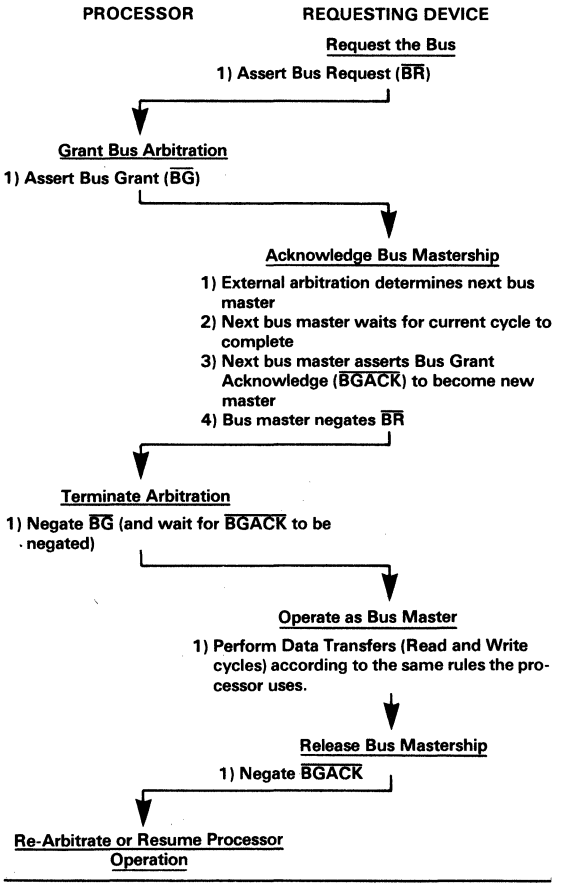
Requesting the Bus. External devices capable of becoming bus masters request the bus by asserting the bus request (BR) signal. This is a wire ORed signal (although it need not be constructed from open collector devices) that indicates to the processor that some external device requires control of the external bus. The processor is effectively at a lower bus priority level than the external device and will relinquish the bus after it has completed the last bus cycle it has started.

When no acknowledge is received before the bus request signal goes inactive, the processor will continue processing when it detects that the bus request is inactive. This allows ordinary processing to continue if the arbitration circuitry responded to noise inadvertently.

Receiving the Bus Grant. The processor asserts bus grant (BG) as soon as possible. Normally this is immediately after internal synchronization. The only exception to this occurs when the processor has made an internal decision to execute the next bus cycle but has not progressed far enough into the cycle to have asserted the address strobe (AS) signal. In this case, bus grant will not be asserted until one clock after address strobe is asserted to indicate to external devices that a bus cycle is being executed.

BUS ARBITRATION CYCLE FLOW-CHART

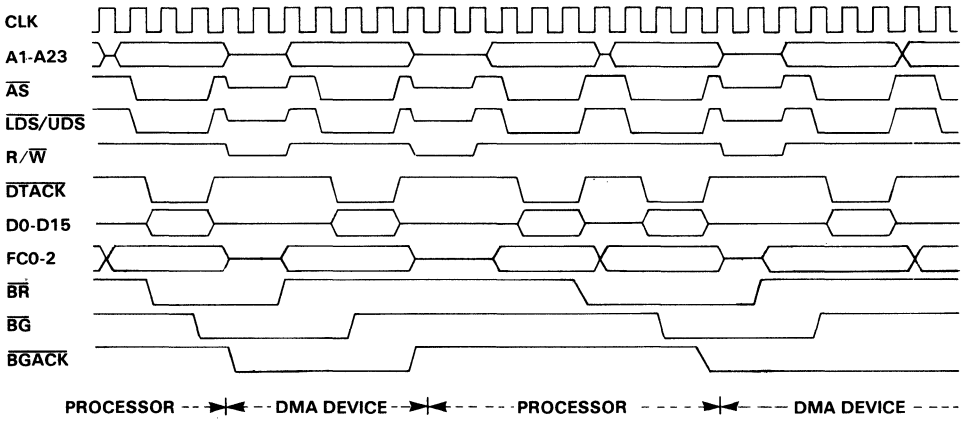
Figure 15



The bus grant signal may be routed through a daisy-chained network or through a specific priority-encoded network. The processor is not affected by the external method of arbitration as long as the protocol is obeyed.

Acknowledgement of Mastership. Upon receiving a bus

BUS ARBITRATION CYCLE TIMING DIAGRAM
Figure 16



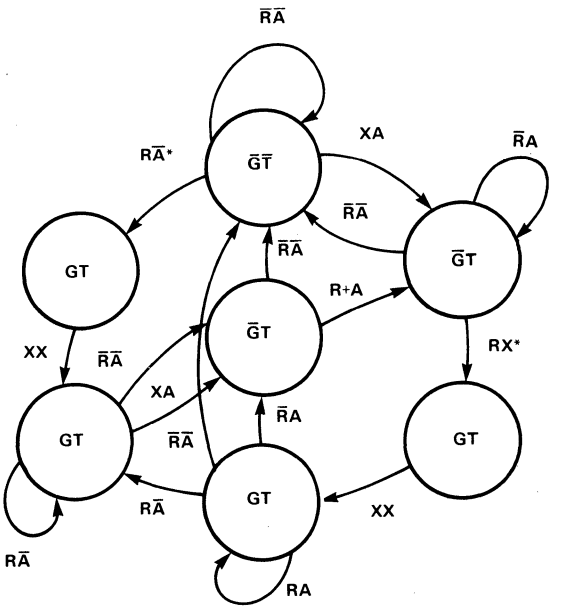
grant, the requesting device waits until address strobe, data transfer acknowledge, and bus grant acknowledge are negated before issuing its own BGACK. The negation of the address strobe indicates that the previous master has completed its cycle, the negation of bus grant acknowledge indicates that the previous master has released the bus. (While address strobe is asserted no device is allowed to "break into" a cycle.) The negation of data transfer acknowledge indicates the previous slave has terminated its connection to the previous master. Note that in some applications data transfer acknowledge might not enter into this function. General purpose devices would then be connected such that they were only dependent on address strobe. When bus grant acknowledge is issued the device is bus master until it negates bus grant acknowledge. Bus grant acknowledge should not be negated until after the bus cycle(s) is (are) completed. Bus mastership is terminated at the negation of bus grant acknowledge.

The bus request from the granted device should be dropped when bus grant acknowledge is asserted. If bus request is still asserted after bus grant acknowledge is negated, the processor performs another arbitration sequence and issues another bus grant. Note that the processor does not perform any external bus cycles before it re-asserts bus grant.

BUS ARBITRATION CONTROL. The bus arbitration control unit in the MK68000 is implemented with a finite state machine. A state diagram of this machine is shown in Figure 17. All asynchronous signals to the MK68000 are synchronized before being used internally. This synchronization is accomplished in a maximum of one cycle of the system clock, assuming that the asynchronous input setup time (#47) has been met. The input signal is sampled on the falling edge of the clock and is valid internally after the next falling edge.

As shown in Figure 17, input signals labeled R and A are internally synchronized on the bus request and bus grant

STATE DIAGRAM OF MK68000 BUS ARBITRATION UNIT
Figure 17



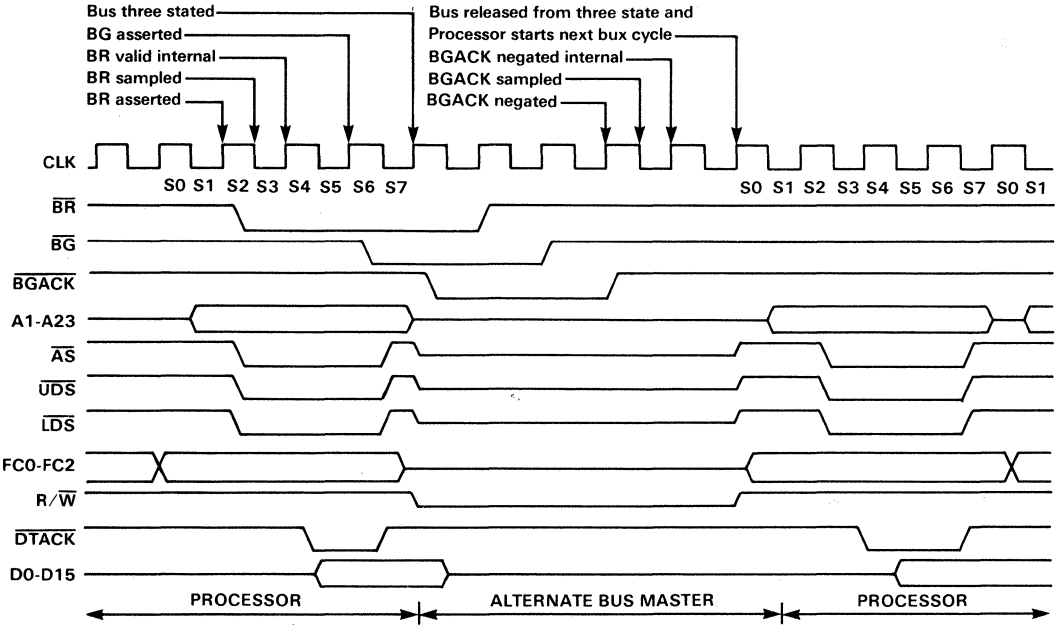
R = Bus Request Internal
A = Bus Grant Acknowledge Internal
G = Bus Grant
T = Three-state Control to Bus Control Logic
X = Don't Care

*State machine will not change state if bus is in S0. Refer to BUS ARBITRATION CONTROL for additional information.

acknowledge pins respectively. The bus grant output is labeled G and the internal three-state control signal T. If T is true, the address, data, and control buses are placed in a high-impedance state when AS is negated. All signals are shown in positive logic (active high) regardless of their true active voltage level.

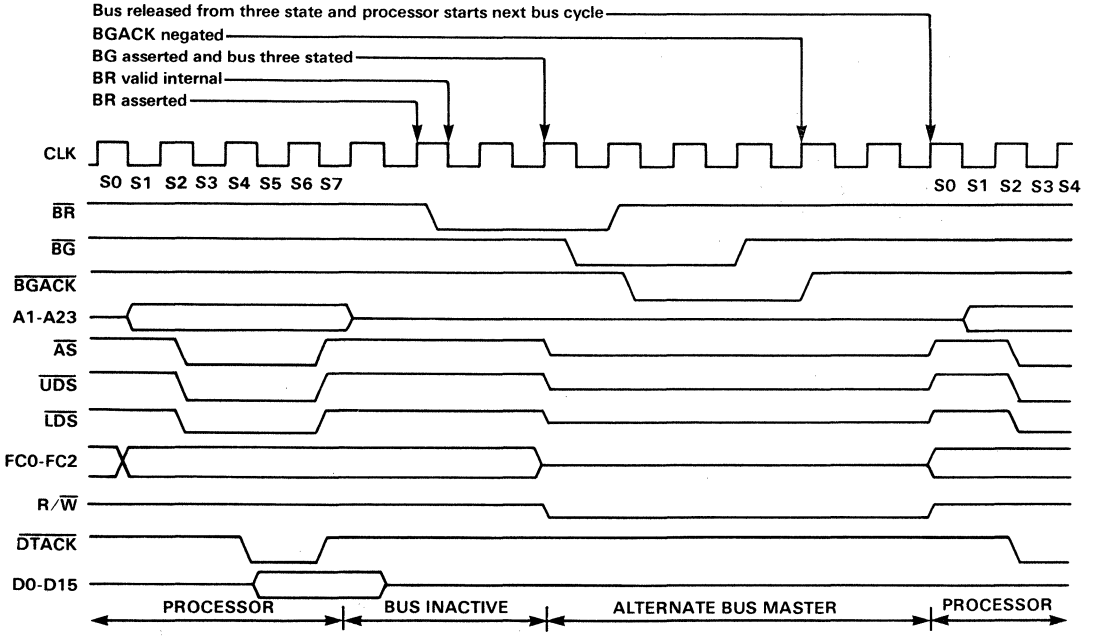
BUS ARBITRATION DURING PROCESSOR BUS CYCLE

Figure 18



BUS ARBITRATION WITH BUS INACTIVE

Figure 19



State changes (valid outputs) occur on the next rising edge after the internal signal is valid.

A timing diagram of the bus arbitration sequence during a processor bus cycle is shown in Figure 18. The bus arbitration sequence while the bus is inactive (i.e., executing internal operations such as a multiply instruction) is shown in Figure 19.

If a bus request is made at a time when the MPU has already begun a bus cycle but $\overline{AS}$ has not been asserted (bus state S0), $\overline{BG}$ will not be asserted on the next rising edge. Instead, $\overline{BG}$ will be delayed until the second rising edge following its internal assertion.

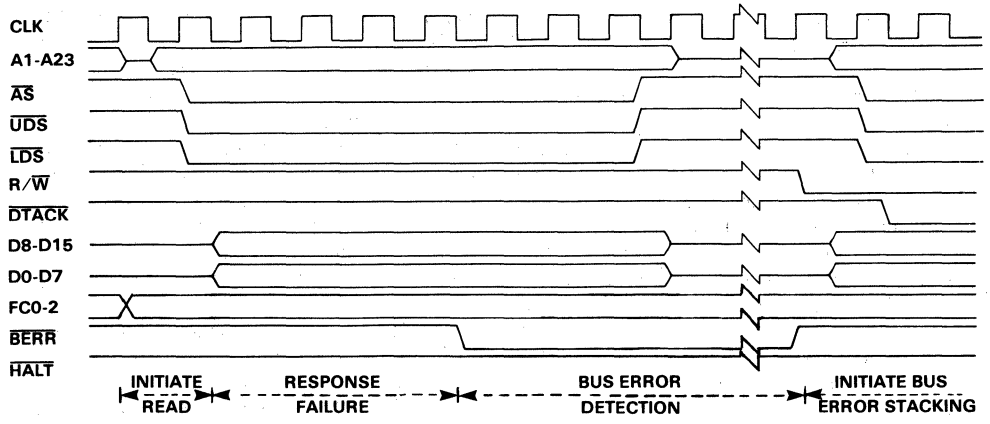
BUS ERROR AND HALT OPERATION. In a bus architecture that requires a handshake from an external device, the possibility exists that the handshake might not occur. Since different systems will require a different maximum response time, a bus error input is provided. External circuitry must be used to determine the duration between address strobe and data transfer acknowledge before issuing a bus error signal. When a bus error signal is received, the processor has two options: initiate a bus error exception sequence or try running the bus cycle again.

Exception Sequence. When the bus error signal is asserted, the current bus cycle is terminated. If $\overline{BERR}$ is asserted before the falling edge of S4, $\overline{AS}$ will be negated in S7 in either a read or write cycle. As long as $\overline{BERR}$ remains asserted, the data and address buses will be in the high-impedance state. When the $\overline{BERR}$ is negated, the processor will begin stacking for exception processing. The bus error exception sequence is entered when the processor receives a bus error signal and the halt pin is inactive. Figure 20 is a timing diagram for the exception sequence. The sequence is composed of the following elements:

1. Stacking the program counter and status register

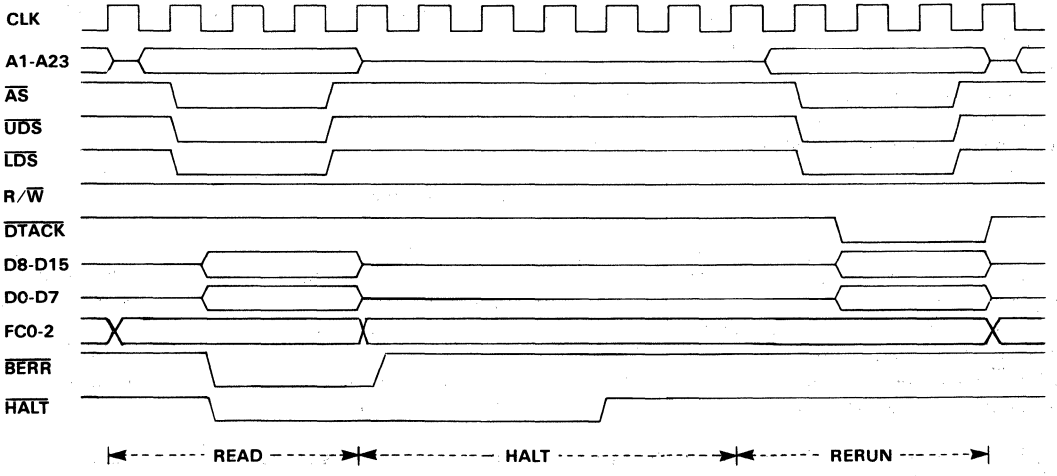
BUS ERROR TIMING DIAGRAM

Figure 20



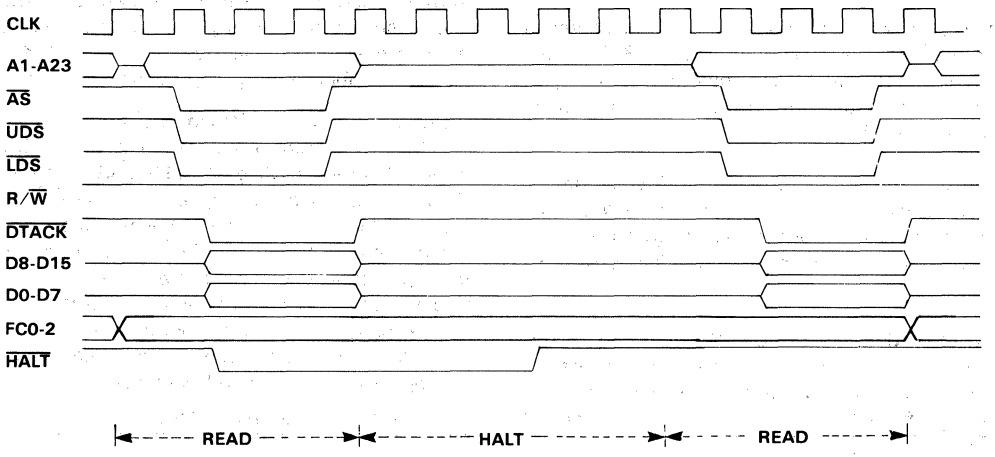
RE-RUN BUS CYCLE TIMING INFORMATION

Figure 21



HALT SIGNAL TIMING CHARACTERISTICS

Figure 22



2. Stacking the error information
3. Reading the bus error vector table entry
4. Executing the bus error handler routine

The stacking of the program counter and the status register is the same as if an interrupt had occurred. Several additional items are stacked when a bus error occurs. These items are used to determine the nature of the error and correct it, if possible. The bus error vector is vector number two located at address $000008. The processor loads the new program counter from this location. A software bus error handler routine is then executed by the processor. Refer to EXCEPTION PROCESSING for additional information.

Re-Running the Bus Cycle. When the processor receives a bus error signal and the halt pin is being driven by an external device, the processor enters the re-run sequence. Figure 21 is a timing diagram for re-running the bus cycle.

The processor completes the bus cycle, then puts the address and data lines in the high-impedance state. The processor remains "halted," and will not run another bus cycle until the halt signal is removed by external logic. Then the processor will re-run the previous bus cycle using the same address, the same function codes, the same data (for a write operation), and the same controls. The bus error signal should be removed at least one clock cycle before the halt signal is removed.

NOTE

The processor will not re-run a read-modify-write cycle. This restriction is made to guarantee that the entire cycle runs correctly and that the write operation of a Test-and-Set operation is performed without ever releasing $\overline{AS}$. If $\overline{BERR}$ and $\overline{HALT}$ are asserted during a read-modify-write bus cycle, a bus error operation results.

Halt Operation with No Bus Error. The halt input signal to the MK68000 performs a Halt/Run/Single-Step function. The halt and run modes are somewhat self explanatory in that when the halt signal is constantly active the processor "halts" (does nothing) and when the halt signal is constantly inactive the processor "runs" (does something).

The single-step mode is derived from correctly timed transitions on the halt signal input. It forces the processor to execute a single bus cycle by entering the "run" mode until the processor starts a bus cycle then changing to the "halt" mode. Thus, the single-step mode allows the user to proceed through (and therefore debug) processor operations one bus cycle at a time.

Figure 22 details the timing required for correct single-step operations. Some care must be exercised to avoid harmful interactions between the bus error signal and the halt pin when using the single cycle mode as a debugging tool. This is also true of interactions between the halt and reset lines, since these can reset the machine.

When the processor completes a bus cycle after recognizing that the halt signal is active, most three-state signals are put in the high-impedance state. These include:

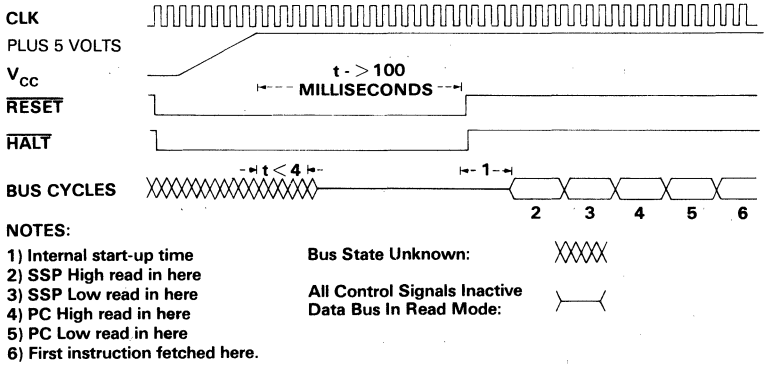
1. address lines
2. data lines

This is required for correct performance of the re-run bus cycle operation.

Note that when the processor honors a request to halt, the function codes are put in the high-impedance state (their buffer characteristics are the same as the address buffers). While the processor is honoring the halt request, bus arbitration performs as usual. That is, halting has no effect on bus arbitration. It is the bus arbitration function that removes the control signals from the bus.

The halt function and the hardware trace capability allow the hardware debugger to trace single bus cycles or single

RESET OPERATION TIMING DIAGRAM
Figure 23



instructions at a time. These processor capabilities, along with a software debugging package, give total debugging flexibility.

Double Bus Faults. When a bus error exception occurs, the processor will attempt to stack several words containing information about the state of the machine. If a bus error exception occurs during the stacking operation, there have been two bus errors in a row. This is commonly referred to as a double bus fault. When a double bus fault occurs, the processor will halt. Once a bus error exception has occurred, any bus error exception occurring before the execution of the next instruction constitutes a double bus fault.

Note that a bus cycle which is re-run does not constitute a bus error exception, and does not contribute to a double bus fault. Note also that this means that as long as the external hardware requests it, the processor will continue to re-run the same bus cycle.

The bus error pin also has an effect on processor operation after the processor receives an external reset input. The processor reads the vector table after a reset to determine the address to start program execution. If a bus error occurs while reading the vector table (or at any time before the first instruction is executed), the processor reacts as if a double bus fault has occurred and it halts. Only an external reset will start a halted processor.

RESET OPERATION. The reset signal is a bidirectional signal that allows either the processor or an external signal to reset the system. Figure 23 is a timing diagram for reset operations. Both the halt and the reset lines must be applied to ensure total reset of the processor.

When the reset and halt lines are driven by an external device, it is recognized as an entire system reset, including the processor. The processor responds by reading the reset vector table entry (vector number zero, address $000000) and loads it into the supervisor stack pointer (SSP). Vector table entry number one at address $000004 is read next and loaded into the program counter. The processor initializes the status register to an interrupt level of seven. No other registers are affected by the reset sequence.

When a RESET sequence is executed, the processor drives the reset pin for 124 clock pulses. In this case, the processor is trying to reset the rest of the system. Therefore, there is no effect on the internal state of the processor. All of the processor's internal registers and the status register are unaffected by the execution of a RESET instruction. All external devices connected to the reset line should be reset at the completion of the RESET instruction.

Asserting the reset and halt pins for 10 clock cycles will cause a processor reset, except when V_{CC} is initially applied to the processor. In this case, an external reset must be applied to the reset pin for 100 milliseconds.

THE RELATIONSHIP OF $\overline{\text{DTACK}}$, $\overline{\text{BERR}}$, AND $\overline{\text{HALT}}$

In order to control termination of a bus cycle for a re-run or a bus error condition properly, $\overline{\text{DTACK}}$, $\overline{\text{BERR}}$, and $\overline{\text{HALT}}$ should be asserted and negated on the rising edge of the MK68000 clock. This will assure that when two signals are asserted simultaneously, the required setup time (#47) for both of them will be met during the same bus state.

This, or some equivalent precaution, should be designed external to the MK68000. Parameter #48 is intended to ensure this operation in a totally asynchronous system, and may be ignored if the above conditions are met.

The preferred bus cycle terminations may be summarized as follows (case numbers refer to Table 17):

Normal Termination: $\overline{\text{DTACK}}$ occurs first (case 1).
Halt Termination: $\overline{\text{HALT}}$ is asserted at same time, or precedes $\overline{\text{DTACK}}$ (no $\overline{\text{BERR}}$) cases 2 and 3.
Bus Error Termination: $\overline{\text{BERR}}$ is asserted in lieu of, at same time, or preceding $\overline{\text{DTACK}}$ (case 4); $\overline{\text{BERR}}$ negated at same time, or after $\overline{\text{DTACK}}$.
Re-Run Termination: $\overline{\text{HALT}}$ and $\overline{\text{BERR}}$ asserted at the

DTACK, BERR, HALT ASSERTION RESULTS
Table 17

Case No.	Control Signal	Asserted on Rising Edge of State N	Asserted on Rising Edge of State N+2	Result
1	DTACK BERR HALT	A NA NA	S X X	Normal cycle terminate and continue.
2	DTACK BERR HALT	A NA A	S X S	Normal cycle terminate and halt. Continue when HALT removed.
3	DTACK BERR HALT	NA NA A	A NA S	Normal cycle terminate and halt. Continue when HALT removed.
4	DTACK BERR HALT	X A NA	X S NA	Terminate and take bus error trap.
5	DTACK BERR HALT	X A A	X S S	Terminate and re-run.
6	DTACK BERR HALT	NA NA A	X A S	Terminate and re-run when HALT removed.

Legend:
N — the number of the current even bus state (e.g., S4, S6, etc.)
A — signal is asserted in this bus state
NA — signal is not asserted in this state
X — don't care
S — signal was asserted in previous state and remains asserted in this state

BERR AND HALT NEGATION RESULTS
Table 18

Conditions of Termination in Table A	Control Signal	Negated on Rising Edge of State N		Negated on Rising Edge of State N+2	Results — Next Cycle
Bus Error	BERR HALT	• •	or or	• •	Takes bus error trap.
Re-run	BERR HALT	• •	or	•	Illegal sequence, usually traps to vector number 0.
Re-run	BERR HALT	•		 •	Re-runs the bus cycle.
Normal	BERR HALT	• •	 or	 •	May lengthen next cycle.
Normal	BERR HALT	 •	 or	• none	If next cycle is started it will be terminated as a bus error.

same time, or before $\overline{DTACK}$ (cases 5 and 6); $\overline{HALT}$ must be negated at least 1 cycle after $\overline{BERR}$.

Table 17 details the resulting bus cycle termination under various combinations of control signal sequences. The negation of these same control signals under several conditions is shown in Table 18 ($\overline{DTACK}$ is assumed to be negated normally in all cases; for best results, both $\overline{DTACK}$ and $\overline{BERR}$ should be negated when address strobe is negated.)

Example A: A system uses a watch-dog timer to terminate accesses to un-populated address space. The timer asserts $\overline{DTACK}$ and $\overline{BERR}$ simultaneously after time-out. (case 4)

Example B: A system uses error detection on RAM contents. Designer may (a) delay $\overline{DTACK}$ until data verified, and return $\overline{BERR}$ and $\overline{HALT}$ simultaneously to re-run error cycle (case 5), or if valid, return $\overline{DTACK}$; (b) delay $\overline{DTACK}$ until data verified, and return $\overline{BERR}$ at same time as $\overline{DTACK}$ if data in error (case 4); (c) return $\overline{DTACK}$ prior to data verification, as described in previous section. If data invalid, $\overline{BERR}$ is asserted (case 1) in next cycle. Error-handling software must know how to recover error cycle.

PROCESSING STATES

The MK68000 is always in one of three processing states: normal, exception, or halted. The normal processing state is that associated with instruction execution; the memory references are to fetch instructions and operands, and to store results. A special case of the normal state is the stopped state which the processor enters when a STOP instruction is executed. In this state, no further memory references are made.

The exception processing state is associated with interrupts, trap instructions, tracing and other exceptional conditions. The exception may be internally generated by an instruction or by an unusual condition arising during the execution of an instruction. Externally, exception processing can be forced by an interrupt, by a bus error, or by a reset. Exception processing is designed to provide an efficient context switch so that the processor may handle unusual conditions.

The halted processing state is an indication of catastrophic hardware failure. For example, if during the exception processing of a bus error another bus error occurs, the processor assumes that the system is unusable and halts. Only an external reset can restart a halted processor. Note that a processor in the stopped state is not in the halted state, nor vice versa.

PRIVILEGE STATES

The processor operates in one of two states of privilege: the "user" state or the "supervisor" state. The privilege state determines which operations are legal, is used by the external memory management device to control and translate accesses, and is used to choose between the supervisor stack pointer and the user stack pointer in instruction references.

The privilege state is a mechanism for providing security in a computer system. Programs should access only their own code and data areas, and ought to be restricted from accessing information which they do not need and must not modify.

The privilege mechanism provides security by allowing most programs to execute in user state. In this state, the accesses are controlled, and the effects on other parts of the system are limited. The operating system executes in the supervisor state, has access to all resources, and performs the overhead tasks for the user state programs.

SUPERVISOR STATE. The supervisor state is the higher state of privilege. For instruction execution, the supervisor state is determined by the S-bit of the status register; if the S-bit is asserted (high), the processor is in the supervisor state. All instructions can be executed in the supervisor state. The bus cycles generated by instructions executed in the supervisor state are classified as supervisor references. While the processor is in the supervisor privilege state, those instructions which use either the system stack pointer implicity or address register seven explicitly access the supervisor stack pointer.

All exception processing is done in the supervisor state, regardless of the setting of the S-bit. The bus cycles generated during exception processing are classified as supervisor references. All stacking operations during exception processing use the supervisor stack pointer.

USER STATE. The user state is the lower state of privilege. For instruction execution, the user state is determined by the S-bit of the status register; if the S-bit is negated (low), the processor is executing instructions in the user state.

Most instructions execute the same in user state as in the supervisor state. However, some instructions which have important system effects are made privileged. User programs are not permitted to execute the STOP instruction, or the RESET instruction. To ensure that a user program cannot enter the supervisor state except in a controlled manner, the instructions which modify the whole status register are privileged. To aid in debugging programs which are to be used as operating systems, the move to user stack pointer (MOVE USP) and move from user stack pointer (MOVE from USP) instructions are also privileged.

The bus cycles generated by an instruction executed in user state are classified as user state references. This allows an external memory management device to translate the address and to control access to protected portions of the address space. While the processor is in the user privilege state, those instructions which use either the system stack pointer implicity, or address register seven explicitly, access the user stack pointer.

PRIVILEGE STATE CHANGES. Once the processor is in the user state and executing instructions, only exception processing can change the privilege state. During exception processing, the current setting of the S-bit of the status register is saved and the S-bit is asserted, putting the processing in the supervisor state. Therefore, when instruction execution resumes at the address specified to process the exception, the processor is in the supervisor privilege state.

REFERENCE CLASSIFICATION. When the processor makes a reference, it classifies the kind of reference being made, using the encoding on the three function code output lines. This allows external translation of addresses, control of access, and differentiation of special processor states, such as interrupt acknowledge. Table 19 lists the classification of references.

REFERENCE CLASSIFICATION
Table 19

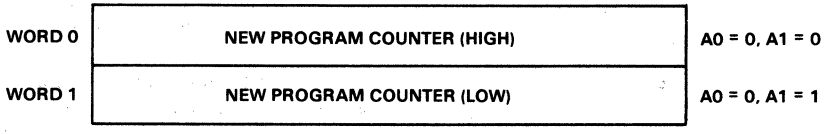
Function Code Output			
FC2	FC1	FC0	Reference Class
0	0	0	(Unassigned)
0	0	1	User Data
0	1	0	User Program
0	1	1	(Unassigned)
1	0	0	(Unassigned)
1	0	1	Supervisor Data
1	1	0	Supervisor Program
1	1	1	Interrupt Acknowledge

EXCEPTION PROCESSING

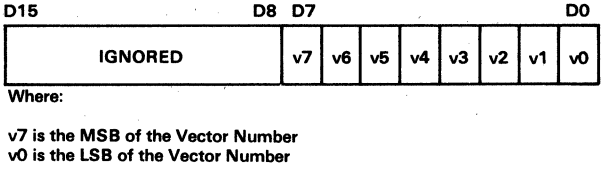
Before discussing the details of interrupts, traps, and tracing, a general description of exception processing is in order. The processing of an exception occurs in four steps, with variations for different exception causes. During the first step, a temporary copy of the status register is made, and the status register is set for exception processing. In the second step the exception vector is determined, and the third step is the saving of the current processor context. In the fourth step a new context is obtained, and the processor switches to instruction processing.

EXCEPTION VECTORS. Exception vectors are memory locations from which the processor fetches the address of a routine which will handle that exception. All exception vectors are two words in length (Figure 24), except for the reset vector, which is four words. All exception vectors lie in the supervisor data space, except for the reset vector which is in the supervisor program space. A vector number is an eight-bit number which, when multiplied by four, gives the address of an exception vector. Vector numbers are generated internally or externally, depending on the cause of the exception. In the case of interrupts, during the interrupt acknowledge bus cycle, a peripheral provides an 8-bit vector number (Figure 25) to the processor on data bus lines D0 through D7. The processor translates the vector number into a full 24-bit address, as shown in Figure 26. The memory layout for exception vectors is given in Table 20.

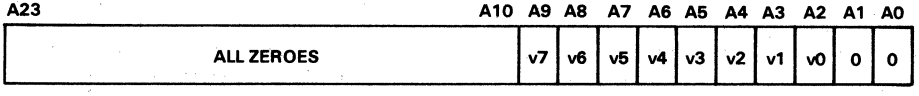
EXCEPTION VECTOR FORMAT
Figure 24



PERIPHERAL VECTOR NUMBER FORMAT
Figure 25



ADDRESS TRANSLATED FROM 8-BIT VECTOR NUMBER
Figure 26



EXCEPTION VECTOR ASSIGNMENT

Table 20

Vector Number(s)	Address			Assignment
	Dec	Hex	Space	
0	0	000	SP	Reset Initial SSP
—	4	004	SP	Reset Initial PC
2	8	008	SD	Bus Error
3	12	00C	SD	Address Error
4	16	010	SD	Illegal Instruction
5	20	014	SD	Zero Divide
6	24	018	SD	CHK Instruction
7	28	01C	SD	TRAPV Instruction
8	32	020	SD	Privilege Violation
9	36	024	SD	Trace
10	40	028	SD	Line 1010 Emulator
11	44	02C	SD	Line 1111 Emulator
12*	48	030	SD	(Unassigned, reserved)
13*	52	034	SD	(Unassigned, reserved)
14*	56	038	SD	(Unassigned, reserved)
15	60	03C	SD	Uninitialized Interrupt Vector
16-23*	64	04C	SD	(Unassigned, reserved)
	95	05F		—
24	96	060	SD	Spurious Interrupt
25	100	064	SD	Level 1 Interrupt Autovector
26	104	068	SD	Level 2 Interrupt Autovector
27	108	06C	SD	Level 3 Interrupt Autovector
28	112	070	SD	Level 4 Interrupt Autovector
29	116	074	SD	Level 5 Interrupt Autovector
30	120	078	SD	Level 6 Interrupt Autovector
31	124	07C	SD	Level 7 Interrupt Autovector
32-47	128	080	SD	TRAP Instruction Vectors
	191	0BF		—
48-63*	192	0C0	SD	(Unassigned, reserved)
	255	0FF		—
64-255	256	100	SD	User Interrupt Vectors
	1023	3FF		—

*Vector numbers 12, 13, 14, 16 through 23 and 48 through 63 are reserved for future enhancements by Mostek. No user peripheral devices should be assigned these numbers.

As shown in Table 20, the memory layout is 512 words long (1024 bytes). It starts at address 0 and proceeds through address 1023. This provides 255 unique vectors; some of these are reserved for TRAPS and other system functions. Of the 255, these are 192 reserved for user interrupt vectors. However, there is no protection on the first 64 entries, so user interrupt vectors may overlap at the discretion of the systems designer.

KINDS OF EXCEPTIONS. Exceptions can be generated by either internal or external causes. The externally generated exceptions are the interrupts and the bus error and reset requests. The interrupts are requests from peripheral devices for processor action while the bus error and reset inputs are used for access control and processor restart. The internally generated exceptions come from instructions, or from address errors or tracing. The trap (TRAP), trap on overflow (TRAPV), check register against bounds (CHK) and divide (DIV) instructions all can generate exceptions as part of their instruction execution. In addition, illegal instructions, word fetches from odd addresses and privilege violations cause exceptions. Tracing behaves like a very high priority, internally generated interrupt after each instruction execution.

EXCEPTION PROCESSING SEQUENCE. Exception processing occurs in four identifiable steps. In the first step, an internal copy is made of the status register. After the copy is made, the S-bit is asserted, putting the processor into the supervisor privilege state. Also, the T-bit is negated which will allow the exception handler to execute unhindered by tracing. For the reset and interrupt exceptions, the interrupt priority mask is also updated.

In the second step, the vector number of the exception is determined. For interrupts, the vector number is obtained by a processor fetch, classified as an interrupt acknowledge. For all other exceptions, internal logic provides the vector number. This vector number is then used to generate the address of the exception vector.

The third step is to save the current processor status, except for the reset exception. The current program counter value and the saved copy of the status register are stacked using the supervisor stack pointer. The program counter value stacked usually points to the next unexecuted instruction, however for bus error and address error, the value stacked for the program counter is unpredictable, and may be incremented from the address of the instruction which caused the error. Additional information defining the current context is stacked for the bus error and address error exceptions.

The last step is the same for all exceptions. The new program counter value is fetched from the exception vector. The processor then resumes instruction execution. The instruction at the address given in the exception vector is fetched, and normal instruction decoding and execution is started.

MULTIPLE EXCEPTIONS. These paragraphs describe the processing which occurs when multiple exceptions arise simultaneously. Exceptions can be grouped according to their occurrence and priority. The Group 0 exceptions are reset, bus error, and address error. These exceptions cause the instruction currently being executed to be aborted, and the exception processing to commence at the next minor cycle of the processor. The Group 1 exceptions are trace and interrupt, as well as the privilege violations and illegal instructions. These exceptions allow the current instruction to execute to completion, but preempt the execution of the next instruction by forcing exception processing to occur (privilege violations and illegal instructions are detected when they are the next instruction to be executed). The Group 2 exceptions occur as part of the normal processing of instructions. The TRAP, TRAPV, CHK, and zero divide exceptions are in this group. For these exceptions, the normal execution of an instruction may lead to exception processing.

Group 0 exceptions have highest priority, while Group 2 exceptions have lowest priority. Within Group 0, reset has highest priority, followed by bus error and then address error. Within Group 1, trace has priority over external interrupts, which in turn takes priority over illegal instruction and privilege violation. Since only one instruction can be executed at a time, there is no priority relation within Group 2.

The priority relation between two exceptions determines which is taken, or taken first, if the conditions for both arise simultaneously. Therefore, if a bus error occurs during a TRAP instruction, the bus error takes precedence, and the TRAP instruction processing is aborted. In another example, if an interrupt request occurs during the execution of an instruction while the T-bit is asserted, the trace exception has priority, and is processed first. Before instruction processing resumes, however, the interrupt exception is also processed, and instruction processing commences finally in the interrupt handler routine. A summary of exception grouping and priority is given in Table 21.

EXCEPTION GROUPING AND PRIORITY
Table 21

Group	Exception	Processing
0	Reset Bus Error Address Error	Exception processing begins within two clock cycles
1	Trace Interrupt Illegal Privilege	Exception processing begins before the next instruction
2	TRAP, TRAPV, CHK, Zero Divide	Exception processing is started by normal instruction execution

EXCEPTION PROCESSING DETAILED DISCUSSION

Exceptions have a number of sources, and each exception has processing which is peculiar to it. The following paragraphs detail the sources of exceptions, how each arises, and how each is processed.

RESET. The reset input provides the highest exception level. The processing of the reset signal is designed for system initiation, and recovery from catastrophic failure. Any processing in progress at the time of the reset is aborted and cannot be recovered. The processor is forced into the supervisor state, and the trace state is forced off. The processor interrupt priority mask is set at level seven. The vector number is internally generated to reference the reset exception vector at location 0 in the supervisor program space. Because no assumptions can be made about the validity of register contents, in particular the supervisor stack pointer, neither the program counter nor the status register is saved. The address contained in the first two words of the reset exception vector is fetched as the initial supervisor stack pointer, and the address in the last two words of the reset exception vector is fetched as the initial program counter. Finally, instruction execution is started at the address in the program counter. The power-up/restart code should be pointed to by the initial program counter.

The RESET instruction does not cause loading of the reset vector, but does assert the reset line to reset external devices. This allows the software to reset the system to a known state and then continue processing with the next instruction.

INTERRUPTS. Seven levels of interrupt priorities are provided. Devices may be chained externally within interrupt priority levels, allowing an unlimited number of peripheral devices to interrupt the processor. Interrupt priority levels are numbered from one to seven, level seven being the highest priorty. The status register contains a three-bit mask which indicates the current processor priority, and interrupts are inhibited for all priority levels less than or equal to the current processor priority.

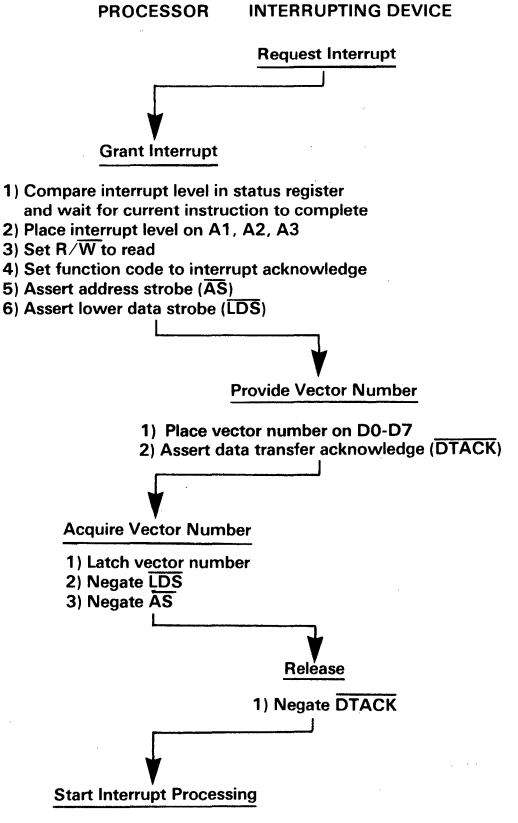
An interrupt request is made to the processor by encoding the interrupt request level on the interrupt request lines; a zero indicates no interrupt request. Interrupt requests arriving at the processor do not force immediate exception processing, but are made pending. Pending interrupts are detected between instruction executions. If the priority of the pending interrupt is lower than or equal to the current processor priority, execution continues with the next instruction and the interrupt exception processing is postponed. (The recognition of level seven is slightly different, as explained in a following paragraph.)

If the priority of the pending interrupt is greater than the current processor priority, the exception processing sequence is started. First a copy of the status register is saved, and the privilege state is set to supervisor, tracing is suppressed, and the processor priority level is set to the level of the interrupt being acknowledged. The processor fetches the vector number from the interrupting device, classifying the reference as an interrupt acknowledge and displaying the level number of the interrupt being acknowledged on the address bus. If external logic requests an automatic vectoring, the processor internally generates a vector number which is determined by the interrupt level number. If external logic indicates a bus error, the interrupt is taken to be spurious, and the generated vector number references the spurious interrupt vector. The processor then proceeds with the usual exception processing, saving the program counter and status register on the supervisor stack. The saved value of the program counter is the address of the instruction which would have been executed had the interrupt not been present. The content of the interrupt vector whose vector number was previously obtained is fetched and loaded into the program counter, and normal instruction execution commences in the interrupt handling routine. A flow chart for the interrupt acknowledge sequence is given in Figure 27; a timing diagram is given in Figure 28.

Priority level seven is a special case. Level seven interrupts

INTERRUPT ACKNOWLEDGE SEQUENCE FLOW CHART

Figure 27



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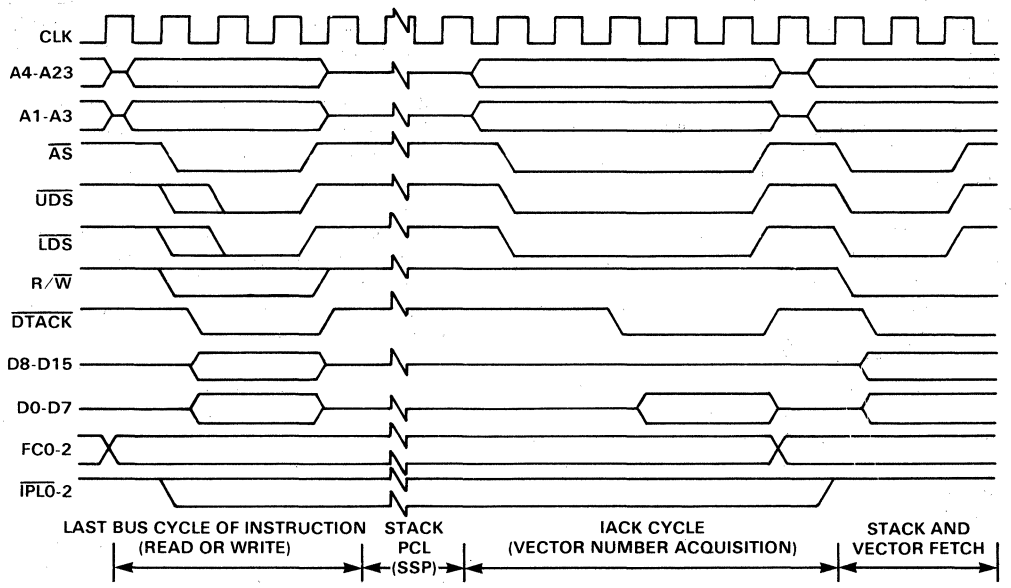
INTERRUPT ACKNOWLEDGE SEQUENCE TIMING DIAGRAM

Figure 28



cannot be inhibited by the interrupt priority mask, thus providing a "non-maskable interrupt" capability. An interrupt is generated each time the interrupt request level changes from some lower level to level seven. Note that a level seven interrupt may still be caused by the level comparison if the request level is a seven and the processor priority is set to a lower level by an instruction.

UNINITIALIZED INTERRUPT. An interrupting device asserts $\overline{VPA}$ or provides an interrupt vector during an interrupt acknowledge cycle to the MK68000. If the vector register has not been initialized, the responding MK68000 Family peripheral will provide vector 15, the uninitialized interrupt vector. This provides a uniform way to recover from a programming error.

SPURIOUS INTERRUPT. If during the interrupt acknowledge cycle no device responds by asserting $\overline{DTACK}$ or $\overline{VPA}$, the bus error line should be asserted to terminate the vector acquisition. The processor separates the processing of this error from bus error by fetching the spurious interrupt vector instead of the bus error vector. The processor then proceeds with the usual exception processing.

INSTRUCTION TRAPS. Traps are exceptions caused by instructions. They arise either from processor recognition of abnormal conditions during instruction execution, or from use of instructions whose normal behavior is trapping.

Some instructions are used specifically to generate traps. The TRAP instruction always forces an exception, and is useful for implementing system calls for user programs. The TRAPV and CHK instructions force an exception if the user program detects a runtime error, which may be an arithmetic overflow or a subscript out of bounds.

The signed divide (DIVS) and unsigned divide (DIVU) instructions will force an exception if a division operation is attempted with a divisor of zero.

ILLEGAL AND UNIMPLEMENTED INSTRUCTIONS. Illegal instruction is the term used to refer to any of the word bit patterns which are not the bit pattern of the first word of a legal instruction. During instruction execution, if such an instruction is fetched, an illegal instruction exception occurs.

Word patterns with bits 15 through 12 equaling 1010 or 1111 are distinguished as unimplemented instructions and separate exception vectors are given to these patterns to permit efficient emulation. This facility allows the operating system to detect program errors, or to emulate unimplemented instructions in software.

PRIVILEGE VIOLATIONS. In order to provide system security, various instructions are privileged. An attempt to execute one of the privileged instructions while in the user state will cause an exception. The privileged instructions are:

STOP	AND (word) Immediate to SR
RESET	EOR (word) Immediate to SR
RTE	OR (word) Immediate to SR
MOVE to SR	MOVE USP

TRACING. To aid in program development, the MK68000 includes a facility to allow instruction by instruction tracing. In the trace state, after each instruction is executed an exception is forced, allowing a debugging program to monitor the execution of the program under test.

The trace facility uses the T-bit in the supervisor portion of the status register. If the T-bit is negated (off), tracing is disabled, and instruction execution proceeds from instruction to instruction as normal. If the T-bit is asserted (on) at the beginning of the execution of an instruction, a trace exception will be generated after the execution of that instruction is completed. If the instruction is not executed, either because an interrupt is taken, or the instruction is illegal or privileged, the trace exception does not occur. The trace exception also does not occur if the instruction is aborted by a reset, bus error, or address error exception. If the instruction is indeed executed and an interrupt is pending on completion, the trace exception is processed before the interrupt exception. If, during the execution of the instruction, an exception is forced by that instruction, the forced exception is processed before the trace exception.

As an extreme illustration of the above rules, consider the arrival of an interrupt during the execution of a TRAP instruction while tracing is enabled. First the trap exception is processed, then the trace exception, and finally the interrupt exception. Instruction execution resumes in the interrupt handler routine.

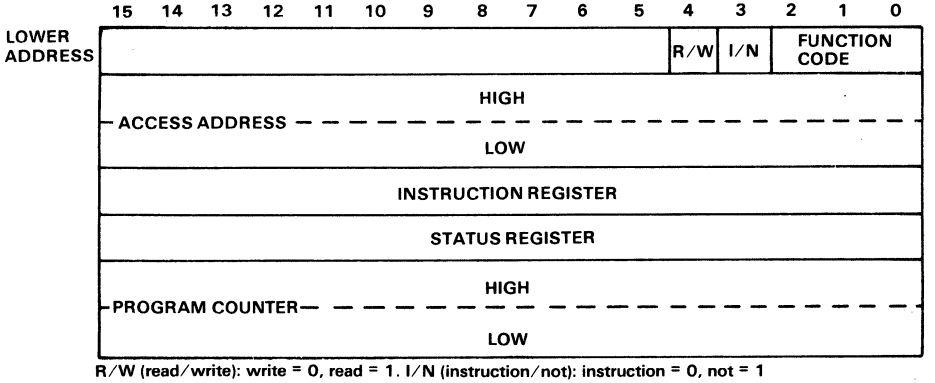
BUS ERROR. Bus error exceptions occur when the external logic requests that a bus error be processed by an exception. The current bus cycle which the processor is making is then aborted. Whether the processor was doing instruction or exception processing, that processing is terminated, and the processor immediately begins exception processing.

Exception processing for bus error follows the usual sequence of steps. The status register is copied, the supervisor state is entered, and the trace state is turned off. The vector number is generated to refer to the bus error vector. Since the processor was not between instructions when the bus error exception request was made, the context of the processor is more detailed. To save more of this context, additional information is saved on the supervisor stack. The program counter and the copy of the status register are of course saved. The value saved for the program counter is advanced by some amount, two to ten bytes beyond the address of the first word of the instruction which made the reference causing the bus error. If the bus error occurred during the fetch of the next instruction, the saved program counter has a value in the vicinity of the current instruction, even if the current instruction is a branch, a jump, or a return instruction. Besides the usual information, the processor saves its internal copy of the first word of the instruction being processed and the address which was being accessed by the aborted bus cycle. Specific information about the access is also saved whether it was a read or a write, whether the processor was processing an instruction or not, and the classification displayed on the function code outputs when the bus error occurred. The processor is processing an instruction if it is in the normal state or processing a Group 2 exception; the processor is not processing an instruction if it is processing a Group 0 or a Group 1 exception. Figure 29 illustrates how this information is organized on the supervisor stack. Although this information is not sufficient in general to effect full recovery from the bus error, it does allow software diagnosis. Finally, the processor commences instruction processing at the address contained in the vector. It is the responsibility of the error handler routine to clean up the stack and determine where to continue execution.

If a bus error occurs during the exception processing for a bus error, address error, or reset, the processor is halted, and all processing ceases. This simplifies the detection of catastrophic system failure, since the processor removes itself from the system rather than destroy all memory contents. Only the RESET pin can restart a halted processor.

ADDRESS ERROR. Address error exceptions occur when the processor attempts to access a word or a long word operand or an instruction at an odd address. The effect is much like an internally generated bus error, so that the bus cycle is aborted, and the processor ceases whatever processing it is currently doing and begins exception processing. After exception processing commences, the

SUPERVISOR STACK ORDER
Figure 29



R/W (read/write): write = 0, read = 1. I/N (instruction/not): instruction = 0, not = 1

sequence is the same as that for bus error including the information that is stacked, except that the vector number refers to the address error vector instead. Likewise, if an address error occurs during the exception processing for a bus error, address error, or reset, the processor is halted.

INTERFACE WITH 6800 PERIPHERALS

To interface the synchronous 6800 peripherals with the asynchronous MK68000, the processor modifies its bus cycle to meet the 6800 cycle requirements whenever a 6800 device address is detected. This is possible since both processors use memory mapped I/O. Figure 30 is a flow chart of the interface operation between the processor and 6800 devices.

DATA TRANSFER OPERATION

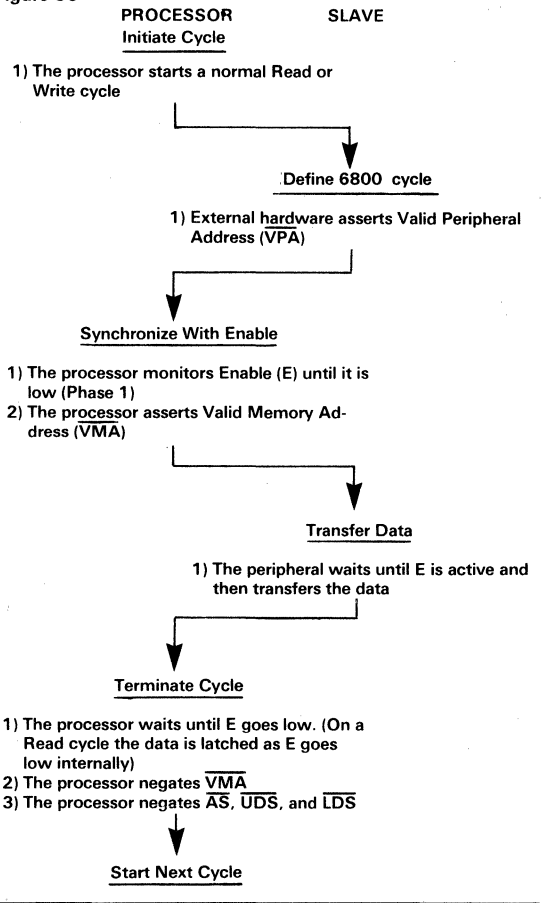
Three signals on the processor provide the 6800 interface. They are: enable (E), valid memory address ($\overline{VMA}$), and valid peripheral address ($\overline{VPA}$). Enable corresponds to the E or Φ2 signal in existing 6800 systems. It is the bus clock used by the frequency clock that is one tenth of the incoming MK68000 clock frequency. The timing of E allows 1 MHz peripherals to be used with an 8 MHz MK68000. Enable has a 60/40 duty cycle; that is, it is low for six input clocks and high for four input clocks. This duty cycle allows the processor to do successive $\overline{VPA}$ accesses on successive E pulses.

6800 cycle timing is given in Figure 31. At state zero (S0) in the cycle, the address bus and function codes are in the high-impedance state. One half clock later, in state 1, the address bus and function code outputs are released from the high-impedance state.

During state 2, the address strobe ($\overline{AS}$) is asserted to

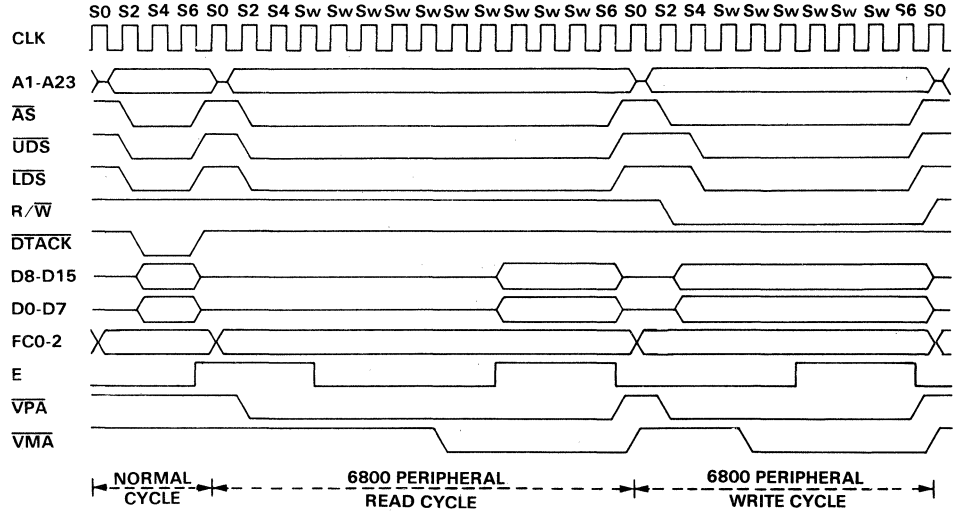
6800 INTERFACING FLOW CHART

Figure 30



6800 CYCLE OPERATION

Figure 31



indicate that there is a valid address on the address bus. If the bus cycle is a read cycle, the upper and/or lower data strobes are also asserted in state 2. If the bus cycle is a write cycle, the read/write (R/$\overline{W}$) signal is switched to low (write) during state 2. One half clock later, in state 3, the write data is placed on the data bus, and in state 4 the data strobes are issued to indicate valid data on the data bus.

The processor now inserts wait states until it recognizes the assertion of $\overline{VPA}$. The $\overline{VPA}$ input signals the processor that the address on the bus is the address of a 6800 device (or an area reserved for 6800 devices) and that the bus should conform to the Φ2 transfer characteristics of the 6800 bus. Valid peripheral address is derived by decoding the address bus, conditioned by address strobe.

After the recognition of $\overline{VPA}$, the processor assures that the Enable (E) is low, by waiting if necessary, and subsequently asserts $\overline{VMA}$. Valid memory address is then used as part of the chip select equation of the peripheral. This ensures that the 6800 peripherals are selected and deselected at the correct time. The peripheral now runs its cycle during the high portion of the E signal.

During a read cycle, the processor latches the peripheral data in state 6. For all cycles, the processor negates the address and data strobes one half clock cycle later in state 7 and the Enable signal goes low at this time. Another half clock later, the address bus is put in the high-impedance state. During a write cycle, the data bus is put in the high-impedance state and the read/write signal is switched high at this time. The peripheral logic must remove $\overline{VPA}$ within one clock after address strobe is negated. $\overline{DTACK}$ should not be asserted while $\overline{VPA}$ is asserted.

Figure 32 shows the timing required by 6800 peripherals, the timing specified for the 6800, and the corresponding timing for the MK68000. Notice that the MK68000 $\overline{VMA}$ is active low, contrasted with the active high 6800 VMA. This allows the processor to put its buses in the high-impedance state on DMA requests without inadvertently selecting peripherals.

INTERRUPT INTERFACE OPERATION

During an interrupt acknowledge cycle while the processor is fetching the vector, if $\overline{VPA}$ is asserted, the MK68000 will assert $\overline{VMA}$ and complete a normal 6800 read cycle as shown in Figure 33. The processor will then use an internally generated vector that is a function of the interrupt being serviced. This process is known as autovectoring. The seven autovectors are vector numbers 25 through 31 (decimal).

This operates in the same fashion (but is not restricted to) the 6800 interrupt sequence. The basic difference is that there are six normal interrupt vectors and one NMI type vector. As with both the 6800 and the MK68000's normal vectored interrupt, the interrupt service routine can be located anywhere in the address space. This is due to the fact that while the vector numbers are fixed, the contents of the vector table entries are assigned by the user.

Since $\overline{VMA}$ is asserted during autovectoring, the 6800 peripheral address decoding should prevent unintended accesses.

INSTRUCTION SET

The following paragraphs provide information about the addressing categories and instruction set of the MK68000.

ADDRESSING CATEGORIES

Effective address modes may be categorized by the ways in which they may be used. The following classifications will be used in the instruction definitions.

Data	If an effective address mode may be used to refer to data operands, it is considered a data addressing effective address mode.
Memory	If an effective address mode may be used to refer to memory operands, it is considered a memory addressing effective address mode.
Alterable	If an effective address mode may be used to refer to alterable (writeable) operands, it is considered an alterable addressing effective address mode.
Control	If an effective address mode may be used to refer to memory operands without an associated size, it is considered a control addressing effective address mode.

Table 22 shows the various categories to which each of the effective address modes belong. Table 23 is the instruction set summary.

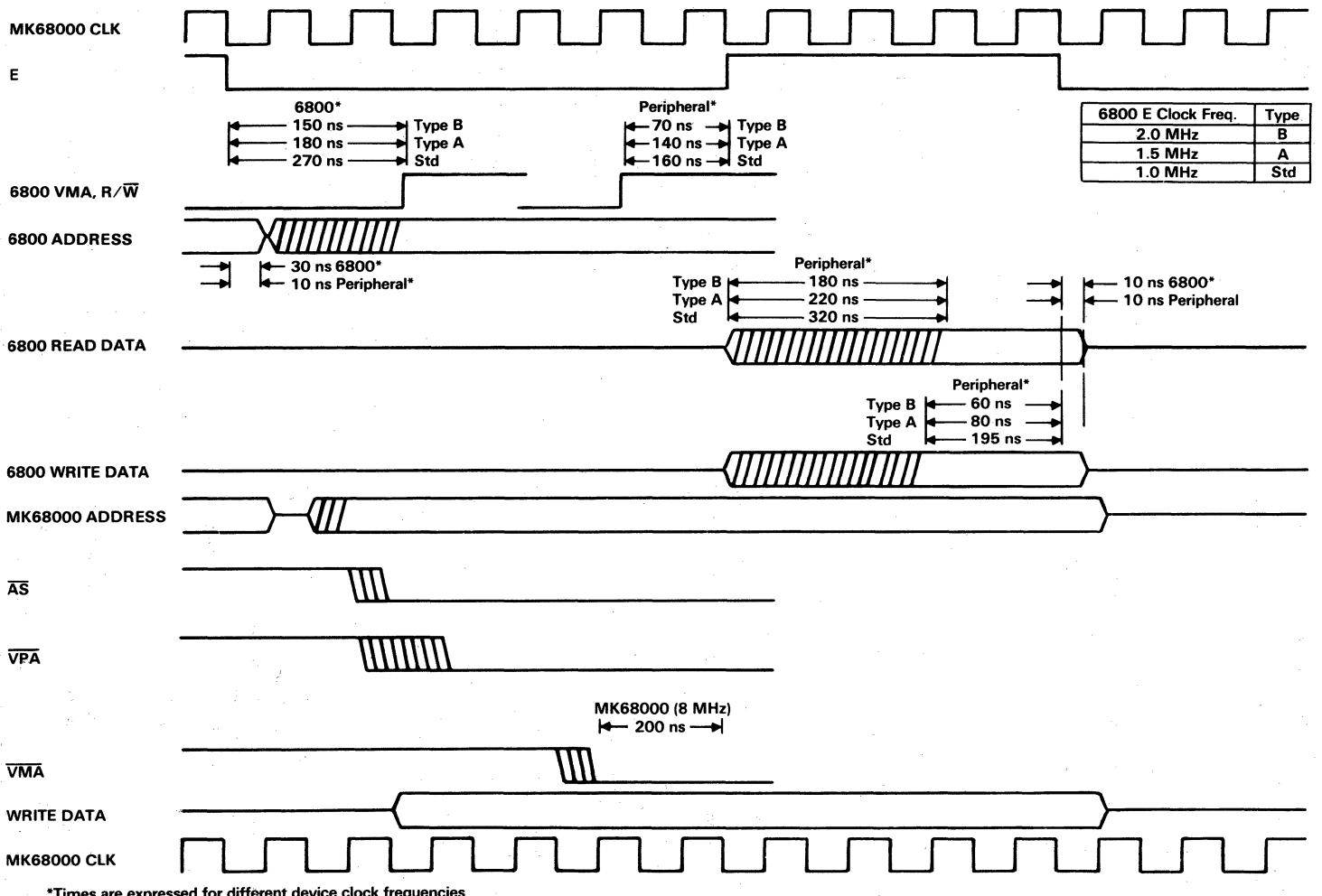
The status register addressing mode is not permitted unless it is explicitly mentioned as a legal addressing mode.

These categories may be combined, so that additional, more restrictive, classifications may be defined. For example, the instruction descriptions use such classifications as alterable memory or data alterable. The former refers to those addressing modes which are both alterable and memory addresses, and the latter refers to addressing modes which are both data and alterable.

INSTRUCTION PRE-FETCH

The MK68000 uses a 2-word tightly-coupled instruction prefetch mechanism to enhance performance. This mechanism is described in terms of the microcode operations involved. If the execution of an instruction is defined to begin when the microroutine for that instruction is entered, some features of the prefetch mechanism can be described.

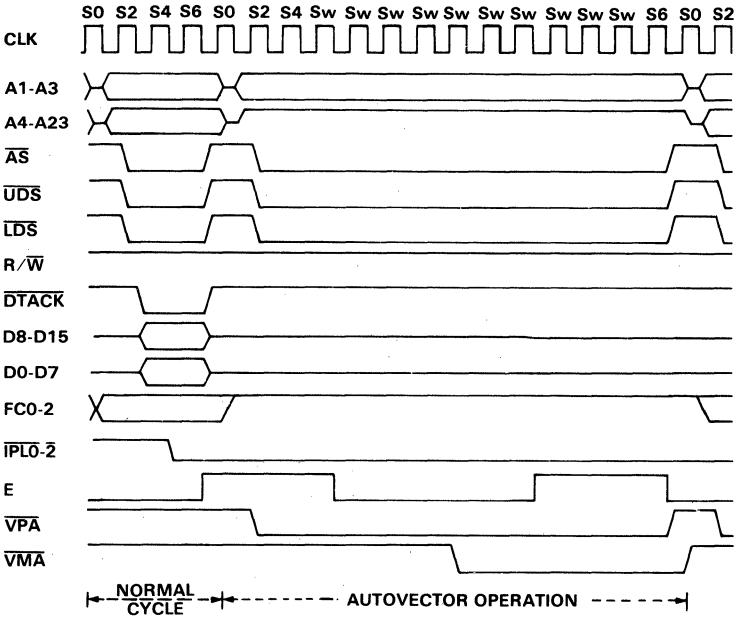
1) When execution of an instruction begins, the operation word and the word following have already been



*Times are expressed for different device clock frequencies

AUTOVECTOR OPERATION TIMING DIAGRAM

Figure 33



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EFFECTIVE ADDRESSING MODE CATEGORIES

Table 22

Effective Address Modes	Mode	Register	Data	Addressing Categories		
				Memory	Control	Alterable
Dn	000	register number	X	–	–	X
An	001	register number	–	–	–	X
An@	010	register number	X	X	X	X
An@+	011	register number	X	X	–	X
An@-	100	register number	X	X	–	X
An@(d)	101	register number	X	X	X	X
An@(d, ix)	110	register number	X	X	X	X
xxx.W	111	000	X	X	X	X
xxx.L	111	001	X	X	X	X
PC@(d)	111	010	X	X	X	–
PC@(d, ix)	111	011	X	X	X	–
#xxx	111	100	X	X	–	–

INSTRUCTION SET

Table 23

Mnemonic	Description	Operation	Condition Codes				
			X	N	Z	V	C
ABCD	Add Decimal with Extend	$(Destination)_{10}+(Source)_{10} \rightarrow Destination$	*	U	*	U	*
ADD	Add Binary	(Destination)+(Source) → Destination	*	*	*	*	*

* affected 0 cleared U defined – unaffected 1 set [ ] = bit number

INSTRUCTION SET (CONTINUED)

Table 23

Mnemonic	Description	Operation	Condition Codes				
			X	N	Z	V	C
ADDA	Add Address	(Destination)+(Source) → Destination	–	–	–	–	–
ADDI	Add Immediate	(Destination)+Immediate Data → Destination	*	*	*	*	*
ADDQ	Add Quick	(Destination)+Immediate Data → Destination	*	*	*	*	*
ADDX	Add Extended	(Destination)+(Source)+ X → Destination	*	*	*	*	*
AND	AND Logical	(Destination) Λ (Source) → Destination	–	*	*	0	0
ANDI	AND Immediate	(Destination) Λ Immediate Data → Destination	–	*	*	0	0
ASL, ASR	Arithmetic Shift	(Destination) Shifted by <count> → Destination	*	*	*	*	*
B_{CC}	Branch Conditionally	If $_{CC}$ then PC+d → PC	–	–	–	–	–
BCHG	Test a Bit and Change	~(<bit number>) OF Destination → Z ~(<bit number>) OF Destination → <bit number> OF Destination	–	–	*	–	–
BCLR	Test a Bit and Clear	~(<bit number>) OF Destination → Z 0 → <bit number> → OF Destination	–	–	*	–	–
BRA	Branch Always	PC + d → PC	–	–	–	–	–
BSET	Test a Bit and Set	~(<bit number>) OF Destination → Z 1 → <bit number> OF Destination	–	–	*	–	–
BSR	Branch to Subroutine	PC → SP@ –; PC+d → PC	–	–	–	–	–
BTST	Test a Bit	~(<bit number>) OF Destination → Z	–	–	*	–	–
CHK	Check Register against Bounds	If Dn <0 or Dn> (<ea>) then TRAP	–	*	U	U	U
CLR	Clear an Operand	0 → Destination	–	0	1	0	0
CMP	Compare	(Destination) – (Source)	–	*	*	*	*
CMPA	Compare Address	(Destination) – (Source)	–	*	*	*	*
CMPI	Compare Immediate	(Destination) – Immediate Data	–	*	*	*	*
CMPM	Compare Memory	(Destination) – (Source)	–	*	*	*	*
DB_{CC}	Test Condition, Decrement and Branch	If ~ $_{CC}$ then Dn – 1 → Dn; if Dn ≠ – 1 then PC + d → PC	–	–	–	–	–
DIVS	Signed Divide	(Destination)/(Source) → Destination	–	*	*	*	0
DIVU	Unsigned Divide	(Destination)/(Source) → Destination	–	*	*	*	0
EOR	Exclusive OR Logical	(Destination) ⊕ (Source) → Destination	–	*	*	0	0
EORI	Exclusive OR Immediate	(Destination) ⊕ Immediate Data → Destination	–	*	*	0	0
EXG	Exchange Register	Rx ⟷ Ry	–	–	–	–	–
EXT	Sign Extend	(Destination) Sign-extended → Destination	–	*	*	0	0
JMP	Jump	Destination → PC	–	–	–	–	–

* affected 0 cleared U defined – unaffected 1 set [ ] = bit number

INSTRUCTION SET (CONTINUED)

Table 23

Mnemonic	Description	Operation	Condition Codes				
			X	N	Z	V	C
JSR	Jump to Subroutine	PC → SP@ –; Destination → PC	–	–	–	–	–
LEA	Load Effective Address	Destination → An	–	–	–	–	–
LINK	Link and Allocate	An → SP@ –; SP → An; SP + d → SP	–	–	–	–	–
LSL, LSR	Logical Shift	(Destination) Shifted by <count> → Destination	*	*	*	0	*
MOVE	Move Data from Source to Destination	(Source) → Destination	–	*	*	0	0
MOVE to CCR	Move to Condition Code	(Source) → CCR	*	*	*	*	*
MOVE to SR	Move to the Status Register	(Source) → SR	*	*	*	*	*
MOVE from SR	Move from the Status Register	SR → Destination	–	–	–	–	–
MOVE USP	Move User Stack Pointer	USP → An, An → USP	–	–	–	–	–
MOVEA	Move Address	(Source) → Destination	–	–	–	–	–
MOVEM	Move Multiple Registers	Registers → Destination (Source) → Registers	–	–	–	–	–
MOVEP	Move Peripheral Data	(Source) → Destination	–	–	–	–	–
MOVEQ	Move Quick	Immediate Data → Destination	–	*	*	0	0
MULS	Signed Multiply	(Destination)* (Source) → Destination	–	*	*	0	0
MULU	Unsigned Multiply	(Destination)* (Source) → Destination	–	*	*	0	0
NBCD	Negate Decimal with Extend	$0 - (\text{Destination})_{10} - X \rightarrow$ Destination	*	U	*	U	*
NEG	Negate	0 – (Destination) → Destination	*	*	*	*	*
NEGX	Negate with Extend	0 – (Destination) – X → Destination	*	*	*	*	*
NOP	No Operation	–	–	–	–	–	–
NOT	Logical Complement	~ (Destination) → Destination	–	*	*	0	0
OR	Inclusive OR Logical	(Destination) v (Source) → Destination	–	*	*	0	0
ORI	Inclusive OR Immediate	(Destination) v Immediate Data → Destination	–	*	*	0	0
PEA	Push Effective Address	Destination → SP@ –	–	–	–	–	–
RESET	Reset External Devices	–	–	–	–	–	–
ROL, ROR	Rotate (Without Extend)	(Destination) Rotated by <count> → Destination	–	*	*	0	*
ROXL, ROXR	Rotate with Extend	(Destination) Rotated by <count> → Destination	*	*	*	0	*
RTE	Return from Exception	SP@ – → SR, SP@ + → PC	*	*	*	*	*
RTR	Return and Restore Condition Codes	SP@ + → CC; SP@ + → PC	*	*	*	*	*
RTS	Return from Subroutine	SP@ + → PC	–	–	–	–	–

* affected 0 cleared U defined – unaffected 1 set [ ] = bit number

Table 23

Mnemonic	Description	Operation	Condition Codes				
			X	N	Z	V	C
SBCD	Subtract Decimal with Extend	$(Destination)_{10} - (Source)_{10} - X \rightarrow Destination$	*	U	*	U	*
S_{CC}	Set According to Condition	If $_{CC}$ then 1's→ Destination else 0's→ Destination	–	–	–	–	–
STOP	Load Status Register and Stop	Immediate Data → SR; STOP	*	*	*	*	*
SUB	Subtract Binary	(Destination) - (Source) → Destination	*	*	*	*	*
SUBA	Subtract Address	(Destination) - (Source) → Destination	–	–	–	–	–
SUBI	Subtract Immediate	(Destination) - Immediate Data → Destination	*	*	*	*	*
SUBQ	Subtract Quick	(Destination) - Immediate Data → Destination	*	*	*	*	*
SUBX	Subtract with Extend	(Destination) - (Source) - X → Destination	*	*	*	*	*
SWAP	Swap Register Halves	Register [31:16] ↔ Register [15:0]	–	*	*	0	0
TAS	Test and Set an Operand	(Destination) Tested → CC; 1 → [7] OF Destination	–	*	*	0	0
TRAP	Trap	PC → SSP@ –; SR → SSP@ –; (Vector) → PC	–	–	–	–	–
TRAPV	Trap on Overflow	If V then TRAP	–	–	–	–	–
TST	Test an Operand	(Destination) Tested → CC	–	*	*	0	0
UNLK	Unlink	An → SP; SP@ + → An	–	–	–	–	–

* affected 0 cleared U defined – unaffected 1 set [ ] = bit number

fetched. The operation word is in the instruction decoder.

2) In the case of multi-word instructions, as each additional word of the instruction is used internally, a fetch is made to the instruction stream to replace it.
3) The last fetch from the instruction stream is made when the operation word is discarded and decoding is started on the next instruction.
4) If the instruction is a single-word instruction causing a branch, the second word is not used. But because this word is fetched by the preceding instruction, it is impossible to avoid this superfluous fetch. In the case of an interrupt or trace exception, both words are not used.
5) The program counter usually points to the last word fetched from the instruction stream.

INSTRUCTION EXECUTION TIMES

The following paragraphs contain listings of the instruction execution times in terms of external clock (CLK) periods. In this timing data, it is assumed that the memory cycle time is 4 clock periods. Any wait states caused by a longer memory cycle must be added to the total instruction time. The number of bus read and write cycles for each instruction is also included with the timing data. This data is enclosed in parenthesis following the execution periods and is shown as: (r/w) where r is the number of read cycles and w is the number of write cycles.

NOTE

The number of periods includes instruction fetch and all applicable operand fetches and stores.

EFFECTIVE ADDRESS OPERAND CALCULATION TIMING

Table 24 lists the number of clock periods required to compute an instruction's effective address. It includes fetching of any extension words, the address computation, and fetching of the memory operand. The number of bus read and write cycles is shown in parenthesis as (r/w). Note there are no write cycles involved in processing the effective address.

MOVE INSTRUCTION CLOCK PERIODS

Tables 25 and 26 indicate the number of clock periods for the move instruction. This data includes instruction fetch, operand reads, and operand writes. The number of bus read and write cycles is shown in parenthesis as: (r/w).

STANDARD INSTRUCTION CLOCK PERIODS

The number of clock periods shown in Table 27 indicates the time required to perform the operations, store the results, and read the next instruction. The number of bus read and write cycles is shown in parenthesis as: (r/w). The number of clock periods plus the number of read and write cycles must be added to those of the effective address calculation where indicated.

In Table 27, the headings have the following meanings. An = address register operand, Dn = data register operand, ea = an operand specified by an effective address, and M = memory effective address operand.

IMMEDIATE INSTRUCTION CLOCK PERIODS

The number of clock periods shown in Table 28 includes the time to fetch immediate operands, perform the operations, store the results, and read the next operation. The number of bus read and write cycles is shown in parenthesis as: (r/w). The number of clock periods plus the number of read

EFFECTIVE ADDRESS CALCULATION TIMING

Table 24

	Addressing Mode	Byte, Word	Long
	Register		
Dn	Data Register Direct	0(0/0)	0(0/0)
An	Address Register Direct	0(0/0)	0(0/0)
	Memory		
An@	Address Register Indirect	4(1/0)	8(2/0)
An@+	Address Register Indirect with Postincrement	4(1/0)	8(2/0)
An@ –	Address Register Indirect with Predecrement	6(1/0)	10(2/0)
An@(d)	Address Register Indirect with Displacement	8(2/0)	12(3/0)
An@ (d, ix)*	Address Register Indirect with Index	10(2/0)	14(3/0)
xxx.W	Absolute Short	8(2/0)	12(3/0)
xxx.L	Absolute Long	12(3/0)	16(4/0)
PC@ (d)	Program Counter with Displacement	8(2/0)	12(3/0)
PC@ (d, ix)*	Program Counter with Index	10(2/0)	14(3/0)
#xxx	Immediate	4(1/0)	8(2/0)

*The size of the index register (ix) does not affect execution time.

MOVE BYTE AND WORD INSTRUCTION CLOCK PERIODS

Table 25

Source	Destination								
	Dn	An	An@	An@+	An@–	An@(d)	An@(d,ix)*	xxx.W	xxx.L
Dn	4(1/0)	4(1/0)	8(1/1)	8(1/1)	8(1/1)	12(2/1)	14(2/1)	12(2/1)	16(3/1)
An	4(1/0)	4(1/0)	8(1/1)	8(1/1)	8(1/1)	12(2/1)	14(2/1)	12(2/1)	16(3/1)
An@	8(2/0)	8(2/0)	12(2/1)	12(2/1)	12(2/1)	16(3/1)	18(3/1)	16(3/1)	20(4/1)
An@+	8(2/0)	8(2/0)	12(2/1)	12(2/1)	12(2/1)	16(3/1)	18(3/1)	16(3/1)	20(4/1)
An@–	10(2/0)	10(2/0)	14(2/1)	14(2/1)	14(2/1)	18(3/1)	20(3/1)	18(3/1)	22(4/1)
An@(d)	12(3/0)	12(3/0)	16(3/1)	16(3/1)	16(3/1)	20(4/1)	22(4/1)	20(4/1)	24(5/1)
An@(d, ix)*	14(3/0)	14(3/0)	18(3/1)	18(3/1)	18(3/1)	22(4/1)	24(4/1)	22(4/1)	26(5/1)
xxx.W	12(3/0)	12(3/0)	16(3/1)	16(3/1)	16(3/1)	20(4/1)	22(4/1)	20(4/1)	24(5/1)
xxx.L	16(4/0)	16(4/0)	20(4/1)	20(4/1)	20(4/1)	24(5/1)	26(5/1)	24(5/1)	28(6/1)
PC@(d)	12(3/0)	12(3/0)	16(3/1)	16(3/1)	16(3/1)	20(4/1)	22(4/1)	20(4/1)	24(5/1)
PC@(d, ix)*	14(3/0)	14(3/0)	18(3/1)	18(3/1)	18(3/1)	22(4/1)	24(4/1)	22(4/1)	26(5/1)
#xxx	8(2/0)	8(2/0)	12(2/1)	12(2/1)	12(2/1)	16(3/1)	18(3/1)	16(3/1)	20(4/1)

*The size of the index register (ix) does not affect execution time.

MOVE LONG INSTRUCTION CLOCK PERIODS

Table 26

Source	Destination								
	Dn	**An**	**An@**	**An@+**	**An@-**	**An@(d)**	**An@(d,ix)***	**xxx.W**	**xxx.L**
Dn	4(1/0)	4(1/0)	12(1/2)	12(1/2)	14(1/2)	16(2/2)	18(2/2)	16(2/2)	20(3/2)
An	4(1/0)	4(1/0)	12(1/2)	12(1/2)	14(1/2)	16(2/2)	18(2/2)	16(2/2)	20(3/2)
An@	12(3/0)	12(3/0)	20(3/2)	20(3/2)	20(3/2)	24(4/2)	26(4/2)	24(4/2)	28(5/2)
An@+	12(3/0)	12(3/0)	20(3/2)	20(3/2)	20(3/2)	24(4/6)	26(4/2)	24(4/2)	28(5/2)
An@-	14(3/0)	14(3/0)	22(3/2)	22(3/2)	22(3/2)	26(4/2)	28(4/2)	26(4/2)	30(5/2)
An@(d)	16(4/0)	16(4/0)	24(4/2)	24(4/2)	24(4/2)	28(5/2)	30(5/2)	28(5/2)	32(6/2)
An@(d, ix)*	18(4/0)	18(4/0)	26(4/2)	26(4/2)	26(4/2)	30(5/2)	32(5/2)	30(5/2)	34(6/2)
xxx.W	16(4/0)	16(4/0)	24(4/2)	24(4/2)	24(4/2)	28(5/2)	30(5/2)	28(5/2)	32(6/2)
xxx.L	20(5/0)	20(5/0)	28(5/2)	28(5/2)	28(5/2)	32(6/2)	34(6/2)	32(6/2)	36(7/2)
PC@(d)	16(4/0)	16(4/0)	24(4/2)	24(4/2)	24(4/2)	28(5/2)	30(5/2)	28(5/2)	32(5/2)
PC@(d, ix)*	18(4/0)	18(4/0)	26(4/2)	26(4/2)	26(4/2)	30(5/2)	32(5/2)	30(5/2)	34(6/2)
#xxx	12(3/0)	12(3/0)	20(3/2)	20(3/2)	20(3/2)	24(4/2)	26(4/2)	24(4/2)	28(5/2)

*The size of the index register (ix) does not affect execution time.

STANDARD INSTRUCTION CLOCK PERIODS

Table 27

Instruction	Size	op <ea>, An	op <ea>, Dn	op Dn, <M>
ADD	Byte, Word	8(1/0) +	4(1/0) +	8(1/1) +
	Long	6(1/0) +**	6(1/0) +**	12(1/2) +
AND	Byte, Word	-	4(1/0) +	8(1/1)+
	Long	-	6(1/0) +**	12(1/2)+
CMP	Byte, Word	6(1/0)+	4(1/0) +	-
	Long	6(1/0) +	6(1/0) +	-
DIVS	-	-	158(1/0) +*	-
DIVU	-	-	140(1/0) +*	-
EOR	Byte, Word	-	4(1/0)***	8(1/1)+
	Long	-	8(1/0)***	12(1/2) +
MULS	-	-	70(1/0) +*	-
MULU	-	-	70(1/0) +*	-
OR	Byte, Word	-	4(1/0) +	8(1/1) +
	Long	-	6(1/0) +**	12(1/2) +
SUB	Byte, Word	8(1/0) +	4(1/0) +	8(1/1) +
	Long	6(1/0) +**	6(1/0) +**	12(1/2) +

+ add effective address calculation time
* indicates maximum value
** total of 8 clock periods for instruction if the effective address is register direct
*** only available effective address mode is data register direct

and write cycles must be added to those of the effective address calculation where indicated.

In Table 28, the headings have the following meanings: # = immediate operand, Dn = data register operand, M = memory operand, and An = address register operand.

SINGLE OPERAND INSTRUCTION CLOCK PERIODS

Table 29 indicates the number of clock periods for the single

IMMEDIATE INSTRUCTION CLOCK PERIODS

Table 28

Instruction	Size	op #, Dn	op #, M	op #, An
ADDI	Byte, Word	8(2/0)	12(2/1) +	–
	Long	16(3/0)	20(3/2) +	–
ADDQ	Byte, Word	4(1/0)	8(1/1) +	8(1/0)*
	Long	8(1/0)	12(1/2) +	8(1/0)
ANDI	Byte, Word	8(2/0)	12(2/1) +	–
	Long	16(3/0)	20(3/1) +	–
CMPI	Byte, Word	8(2/0)	8(2/0) +	8(2/0)
	Long	14(3/0)	12(3/0) +	14(3/0)
EORI	Byte, Word	8(2/0)	12(2/1) +	–
	Long	16(3/0)	20(3/2) +	–
MOVEQ	Long	4(1/0)	–	–
ORI	Byte, Word	8(2/0)	12(2/1) +	–
	Long	16(3/0)	20(3/2) +	–
SUBI	Byte, Word	8(2/0)	12(2/1) +	–
	Long	16(3/0)	20(3/2) +	–
SUBQ	Byte, Word	4(1/0)	8(1/1) +	8(1/0)*
	Long	8(1/0)	12(1/2) +	8(1/0)

+ add effective address calculation time
*word only

SINGLE OPERAND INSTRUCTION CLOCK PERIODS

Table 29

Instruction	Size	Register	Memory
CLR	Byte, Word	4(1/0)	8(1/1) +
	Long	6(1/0)	12(1/2) +
NBCD	Byte	6(1/0)	8(1/1) +
NEG	Byte, Word	4(1/0)	8(1/1) +
	Long	6(1/0)	12(1/2) +
NEGX	Byte, Word	4(1/0)	8(1/1) +
	Long	6(1/0)	12(1/2) +
NOT	Byte, Word	4(1/0)	8(1/1) +
	Long	6(1/0)	12(1/2) +
S_{CC}	Byte, False	4(1/0)	8(1/1) +
	Byte, True	6(1/0)	8(1/1) +
TAS	Byte	4(1/0)	10(1/1) +
TST	Byte, Word	4(1/0)	4(1/0)
	Long	4(1/0)	4(1/0) +

+ add effective address calculation time

SHIFT/ROTATE INSTRUCTION CLOCK PERIODS

Table 30

Instruction	Size	Register	Memory
ASR, ASL	Byte, Word	6 + 2n(1/0)	8(1/1) +
	Long	8 + 2n(1/0)	–
LSR, LSL	Byte, Word	6 + 2n(1/0)	8(1/1) +
	Long	8 + 2n(1/0)	–
ROR, ROL	Byte, Word	6 + 2n(1/0)	8(1/1) +
	Long	8 + 2n(1/0)	–
ROXR, ROXL	Byte, Word	6 + 2n(1/0)	8(1/1) +
	Long	8 + 2n(1/0)	–

BIT MANIPULATION INSTRUCTION CLOCK PERIODS

Table 31

Instruction	Size	Dynamic		Static	
		Register	Memory	Register	Memory
BCHG	Byte	–	8(1/1)+	–	12(2/1)+
	Long	8(1/0)*	–	12(2/0)*	–
BCLR	Byte	–	8(1/1)+	–	12(2/1)+
	Long	10(1/0)*	–	14(2/0)*	–
BSET	Byte	–	8(1/1)+	–	12(2/1)+
	Long	8(1/0)*	–	12(2/0)*	–
BTST	Byte	–	4(1/0)+	–	8(2/0)+
	Long	6(1/0)	–	10(2/0)	–

+ add effective address calculation time
* indicates maximum value

CONDITIONAL INSTRUCTION CLOCK PERIODS

Table 32

Instruction	Displacement	Trap or Branch Taken	Trap or Branch Not Taken
B_{CC}	Byte	10(2/0)	8(1/0)
	Word	10(2/0)	12(2/0)
BRA	Byte	10(2/0)	–
	Word	10(2/0)	–
BSR	Byte	18(2/2)	–
	Word	18(2/2)	–
DB_{CC}	CC true	–	12(2/0)
	CC false	10(2/0)	14(3/0)
CHK	–	40(5/3)+ *	8(1/0)+
TRAP	–	34(4/3)	–
TRAPV	–	34(5/3)	4(1/0)

+ add effective address calculation time
* indicates maximum value

JMP, JSR, LEA, PEA, MOVEM INSTRUCTION CLOCK PERIODS
Table 33

Instr	Size	An@	An@+	An@-	An@(d)	An@(d, ix)*	xxx.W	xxx.L	PC@(d)	PC@(d, ix)*
JMP	-	8(2/0)	-	-	10(2/0)	14(3/0)	10(2/0)	12(3/0)	10(2/0)	14(3/0)
JSR	-	16(2/2)	-	-	18(2/2)	22(2/2)	18(2/2)	20(3/2)	18(2/2)	22(2/2)
LEA	-	4(1/0)	-	-	8(2/0)	12(2/0)	8(2/0)	12(3/0)	8(2/0)	12(2/0)
PEA	-	12(1/2)	-	-	16(2/2)	20(2/2)	16(2/2)	20(3/2)	16(2/2)	20(2/2)
MOVEM	Word	12 + 4n (3 + n/0)	12 + 4n (3 + n/0)	- -	16 + 4n (4 + n/0)	18 + 4n (4 + n/0)	16 + 4n (4 + n/0)	20 + 4n (5 + n/0)	16 + 4n (4 + n/0)	18 + 4n (4 + n/0)
M→R	Long	12 + 8n (3 + 2n/0)	12 + 8n (3 + 2n/0)	- -	16 + 8n (4 + 2n/0)	18 + 8n (4 + 2n/0)	16 + 8n (4 + 2n/0)	20 + 8n (5 + 2n/0)	16 + 8n (4 + 2n/0)	18 + 8n (4 + 2n/0)
MOVEM	Word	8 + 5n (2/n)	- -	8 + 5n (2/n)	12 + 5n (3/n)	14 + 5n (3/n)	12 + 5n (3/n)	16 + 5n (4/n)	- -	- -
R→M	Long	8 + 10n (2/2n)	- -	8 + 10n (2/2n)	12 + 10n (3/2n)	14 + 10n (3/2n)	12 + 10n (3/2n)	16 + 10n (4/2n)	- -	- -

n is the number of registers to move
* is the size of the index register (ix) does not affect the instruction's execution time

operand instructions. The number of bus read and write cycles is shown in parenthesis as: (r/w). The number of clock periods plus the number of read and write cycles must be added to those of the effective address calculation where indicated.

SHIFT/ROTATE INSTRUCTION CLOCK PERIODS

Table 30 indicates the number of clock periods for the shift and rotate instructions. The number of bus read and write cycles is shown in parenthesis as: (r/w). The number of clock periods plus the number of read and write cycles must be added to those of the effective address calculation where indicated.

BIT MANIPULATION INSTRUCTION CLOCK PERIODS

Table 31 indicates the number of clock periods required for the bit manipulation instructions. The number of bus read and write cycles is shown in parenthesis as: (r/w). The number of clock periods plus the number of read and write cycles must be added to those of the effective address calculation where indicated.

CONDITIONAL INSTRUCTION CLOCK PERIODS

Table 32 indicates the number of clock periods required for the conditional instructions. The number of bus read and write cycles is indicated in parenthesis as: (r/w). The number of clock periods plus the number of read and write cycles must be added to those of the effective address calculation where indicated.

JMP, JSR, LEA, PEA, MOVEM INSTRUCTION CLOCK PERIODS

Table 33 indicates the number of clock periods required for the jump, jump to subroutine, load effective address, push effective address, and move multiple registers instructions. The number of bus read and write cycles is shown in parenthesis as: (r/w).

MULTI-PRECISION INSTRUCTION CLOCK PERIODS

Table 34 indicates the number of clock periods for the multi-precision instructions. The number of clock periods includes the time to fetch both operands, perform the operations, store the results, and read the next instructions. The number of read and write cycles is shown in parenthesis as: (r/w).

In Table 34, the headings have the following meanings: Dn = data register operand and M = memory operand.

MULTI-PRECISION INSTRUCTION CLOCK PERIODS
Table 34

Instruction	Size	op Dn, Dn	op M, M
ADDX	Byte, Word	4(1/0)	18(3/1)
	Long	8(1/0)	30(5/2)
CMPM	Byte, Word	-	12(3/0)
	Long	-	20(5/0)
SUBX	Byte, Word	4(1/0)	18(3/1)
	Long	8(1/0)	30(5/2)
ABCD	Byte	6(1/0)	18(3/1)
SBCD	Byte	6(1/0)	18(3/1)

MISCELLANEOUS INSTRUCTION CLOCK PERIODS
Table 35

Instruction	Size	Register	Memory	Register Memory	Memory Register
MOVE from SR	–	6(1/0)	8(1/1)+	–	–
MOVE to CCR	–	12(2/0)	12(2/0)+	–	–
MOVE to SR	–	12(2/0)	12(2/0)+	–	–
MOVEP	Word	–	–	18(2/2)	16(4/0)
	Long	–	–	24(2/4)	24(6/0)
EXG	–	6(1/0)	–	–	–
EXT	Word	4(1/0)	–	–	–
	Long	4(1/0)	–	–	–
LINK	–	16(2/2)	–	–	–
MOVE from USP	–	4(1/0)	–	–	–
MOVE to USP	–	4(1/0)	–	–	–
NOP	–	4(1/0)	–	–	–
RESET	–	132(1/0)	–	–	–
RTE	–	20(5/0)	–	–	–
RTR	–	20(5/0)	–	–	–
RTS	–	16(4/0)	–	–	–
STOP	–	4(0/0)	–	–	–
SWAP	–	4(1/0)	–	–	–
UNLK	–	12(3/0)	–	–	–

+ add effective address calculation time

MISCELLANEOUS INSTRUCTION CLOCK PERIODS

Table 35 indicates the number of clock periods for the following miscellaneous instructions. The number of bus read and write cycles is shown in parenthesis as: (r/w). The number of clock periods plus the number of read and write cycles must be added to those of the effective address calculation where indicated.

EXCEPTION PROCESSING CLOCK PERIODS

Table 36 indicates the number of clock periods for exception processing. The number of clock periods includes the time for all stacking, the vector fetch, and the fetch of the first instruction of the handler routine. The number of bus read and write cycles is shown in parenthesis as: (r/w).

EXCEPTION PROCESSING CLOCK PERIODS
Table 36

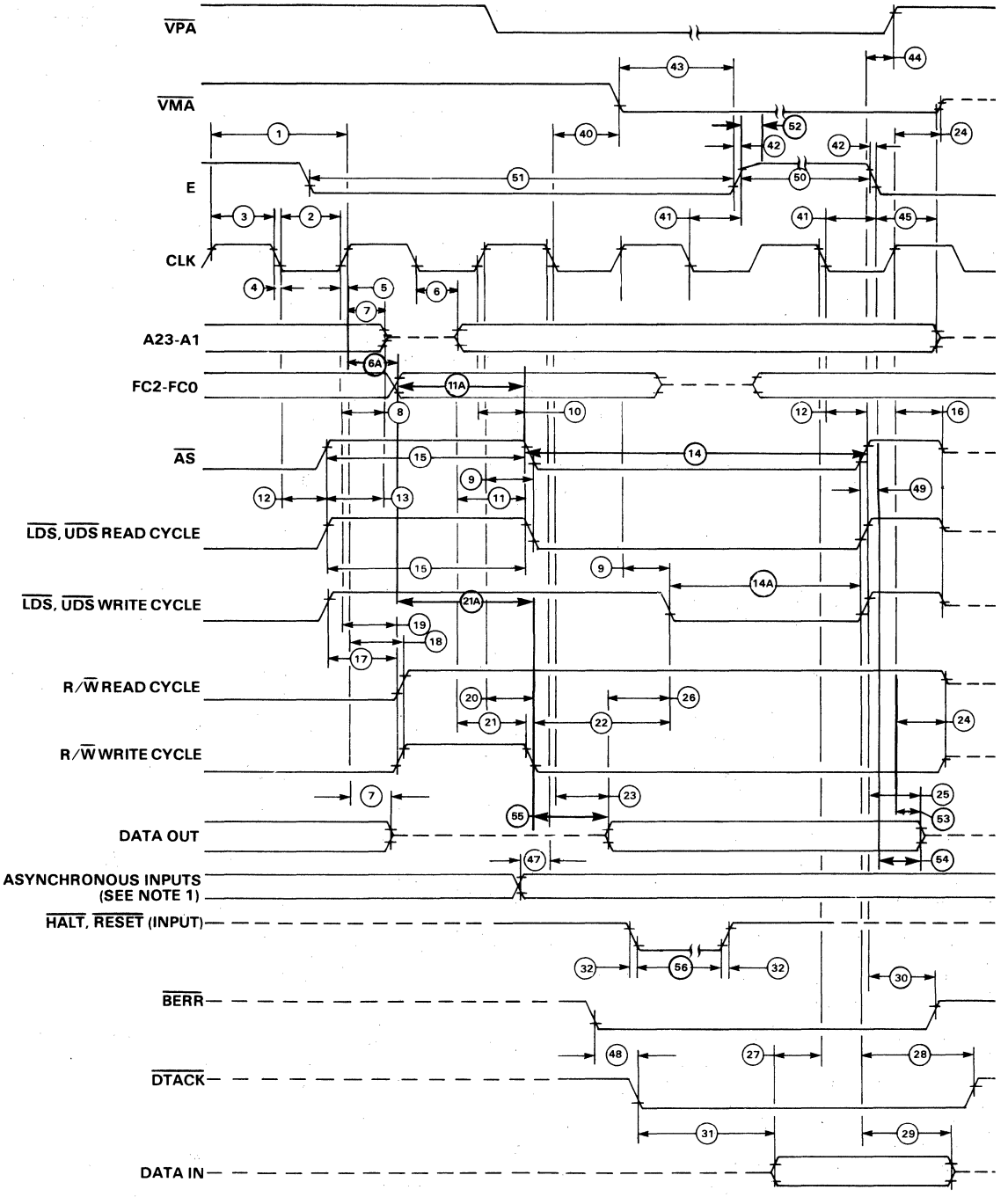
Exception	Periods
Address Error	50(4/7)
Bus Error	50(4/7)
Interrupt	44(5/3)*
Illegal Instruction	34(4/3)
Privileged Instruction	34(4/3)
Trace	34(4/3)

*The interrupt acknowledge bus cycle is assumed to take four external clock periods

AC ELECTRICAL WAVEFORMS

Figure 34

These waveforms should only be referenced in regard to the edge-to-edge measurement of the timing specifications. They are not intended as a functional description of the input and output signals. Refer to other functional descriptions and their related diagrams for device operation.



NOTE 1: Setup time for the asynchronous inputs BERR, BGACK, BR, DTACK, IPL0-IPL2, and VPA guarantees their recognition at the next falling edge of the clock.

NOTE 2: Waveform measurements for all inputs and outputs are specified at: logic high = 2.0 volts, logic low = 0.8 volts.

VI

AC ELECTRICAL SPECIFICATIONS

(V_{CC} = 5.0 Vdc ± 5%; V_{SS} = 0 Vdc; T_A = 0°C to 70°C, Figure 31)

No.	Characteristic	Symbol	4 MHz		6 MHz		8 MHz		10 MHz		Unit
			MK68000-4		MK68000-6		MK68000-8		MK68000-10		
			Min	Max	Min	Max	Min	Max	Min	Max	
1	Clock Period	t_{cyc}	250	500	167	500	125	500	100	500	ns
2	Clock Width Low	t_{CL}	115	250	75	250	55	250	45	250	ns
3	Clock Width High	t_{CH}	115	250	75	250	55	250	45	250	ns
4	Clock Fall Time	t_{Cf}	–	10	–	10	–	10	–	10	ns
5	Clock Rise Time	t_{Cr}	–	10	–	10	–	10	–	10	ns
6	Clock Low to Address	t_{CLAV}	–	90	–	80	–	70	–	55	ns
6A	Clock High to FC Valid	t_{CHFCV}	–	90	–	80	–	70	–	60	ns
7	Clock High to Address/Data High Impedance (maximum)	t_{CHAZx}	–	120	–	100	–	80	–	70	ns
8	Clock High to Address/FC Invalid (minimum)	t_{CHAZn}	0	–	0	–	0	–	0	–	ns
9[1]	Clock High to $\overline{AS}$, $\overline{DS}$ Low (maximum)	t_{CHSLx}	–	80	–	70	–	60	–	55	ns
10	Clock High to $\overline{AS}$, $\overline{DS}$ Low (minimum)	t_{CHSLn}	0	–	0	–	0	–	0	–	ns
11[2]	Address to $\overline{AS}$, $\overline{DS}$ (read) Low/$\overline{AS}$ Write	t_{AVSL}	55	–	35	–	30	–	20	–	ns
11A[2]	FC valid to $\overline{AS}$, $\overline{DS}$ (read) Low/$\overline{AS}$ Write	t_{FCVSL}	80	–	70	–	60	–	50	–	μs
12[1]	Clock Low to $\overline{AS}$, $\overline{DS}$ High	t_{CLSH}	–	90	–	80	–	70	–	55	ns
13[2]	$\overline{AS}$, $\overline{DS}$ High to Address/FC Invalid	t_{SHAZ}	60	–	40	–	30	–	20	–	ns
14[2]	$\overline{AS}$, $\overline{DS}$ Width Low (read)/ $\overline{AS}$ Write	t_{SL}	535	–	337	–	240	–	195	–	ns
14A[2]	$\overline{DS}$ Width Low (Write)	–	285	–	170	–	115	–	95	–	ns
15[2]	$\overline{AS}$, $\overline{DS}$ Width High	t_{SH}	285	–	180	–	150	–	105	–	ns
16	Clock High to $\overline{AS}$, $\overline{DS}$ High Impedance	t_{CHSZ}	–	120	–	100	–	80	–	70	ns
17[2]	DS High to R/$\overline{W}$ High	t_{SHRH}	60	–	50	–	40	–	20	–	ns
18[1]	Clock High to R/$\overline{W}$ High (maximum)	t_{CHRHx}	–	90	–	80	–	70	–	60	ns
19	Clock High to R/$\overline{W}$ High (minimum)	t_{CHRHn}	0	–	0	–	0	–	0	–	ns
20[1]	Clock High to R/$\overline{W}$ Low	t_{CHRL}	–	90	–	80	–	70	–	60	ns
21[2]	Address/Valid to R/$\overline{W}$ Low	t_{AVRL}	45	–	25	–	20	–	0	–	ns
21A[2]	FC Valid to R/$\overline{W}$ Low	t_{FCVRL}	80	–	70	–	60	–	50	–	ns

AC ELECTRICAL SPECIFICATIONS (Continued)
(V_{CC} = 5.0 Vdc ± 5%; V_{SS} = 0 Vdc; T_A = 0°C to 70°C, Figure 31)

No.	Characteristic	Symbol	4 MHz		6 MHz		8 MHz		10 MHz		Unit
			MK68000-4		MK68000-6		MK68000-8		MK68000-10		
			Min	Max	Min	Max	Min	Max	Min	Max	
22[2]	R/$\overline{W}$ Low to $\overline{DS}$ Low (write)	t_{RLSL}	200	–	140	–	80	–	50	–	ns
23	Clock Low to Data Out Valid	t_{CLDO}	–	90	–	80	–	70	–	55	ns
24	Clock High to R/$\overline{W}$, $\overline{VMA}$ High Impedance	t_{CHRZ}	–	120	–	100	–	80	–	70	ns
25[2]	$\overline{DS}$ High to Data Out Invalid	t_{SHDO}	60	–	40	–	30	–	20	–	ns
26[2]	Data Out Valid to $\overline{DS}$ Low (write)	t_{DOSL}	55	–	35	–	30	–	20	–	ns
27[5]	Data In to Clock Low (set up time)	t_{DICL}	30	–	25	–	15	–	15	–	ns
28[2]	$\overline{DS}$ High to $\overline{DTACK}$ High	t_{SHDAH}	0	240	0	160	0	120	0	90	ns
29	$\overline{DS}$ High to Data Invalid (hold time)	t_{SHDI}	0	–	0	–	0	–	0	–	ns
30	$\overline{AS}$, $\overline{DS}$ High to $\overline{BERR}$ High	t_{SHBEH}	0	–	0	–	0	–	0	–	ns
31[2,5]	$\overline{DTACK}$ Low to Data In (setup time)	t_{DALDI}	–	180	–	120	–	90	–	65	ns
32	$\overline{HALT}$ and $\overline{RESET}$ Input Transition Time	t_{RHrf}	0	200	0	200	0	200	0	200	ns
33	Clock High to $\overline{BG}$ Low	t_{CHGL}	–	90	–	80	–	70	–	60	ns
34	Clock High to $\overline{BG}$ High	t_{CHGH}	–	90	–	80	–	70	–	60	ns
35	$\overline{BR}$ Low to $\overline{BG}$ Low	t_{BRLGL}	1.5	3.0	1.5	3.0	1.5	3.0	1.5	3.0	clk. per.
36	$\overline{BR}$ High to $\overline{BG}$ High	t_{BRHGH}	1.5	3.0	1.5	3.0	1.5	3.0	1.5	3.0	clk. per.
37	$\overline{BGACK}$ Low to $\overline{BG}$ High	t_{GALGH}	1.5	3.0	1.5	3.0	1.5	3.0	1.5	3.0	clk. per.
38	$\overline{BG}$ Low to Bus High Impedance (with $\overline{AS}$ high)	t_{GLZ}	–	120	–	100	–	80	–	70	ns
39	$\overline{BG}$ Width High	t_{GH}	1.5	–	1.5	–	1.5	–	1.5	–	clk. per.
40	Clock Low to $\overline{VMA}$ Low	t_{CLVML}	–	90	–	80	–	70	–	70	ns
41	Clock Low to E Transition	t_{CLE}	–	100	–	85	–	70	–	55	ns
42	E Output Rise and Fall Time	t_{Erf}	–	25	–	25	–	25	–	25	ns
43	$\overline{VMA}$ Low to E High	t_{VMLEH}	325	–	240	–	200	–	150	–	ns
44	$\overline{AS}$, $\overline{DS}$ High to $\overline{VPA}$ High	t_{SHVPH}	0	240	0	160	0	120	0	90	ns
45	E Low to Address/$\overline{VMA}$/FC Invalid	t_{ELAI}	55	–	35	–	30	–	10	–	ns
46	$\overline{BGACK}$ Width	t_{BGL}	1.5	–	1.5	–	1.5	–	1.5	–	clk. per.
47	Asynchronous Input Setup Time	t_{ASI}	30	–	25	–	20	–	20	–	ns
48	$\overline{BERR}$ Low to $\overline{DTACK}$ Low	t_{BELDAL}	50	–	50	–	50	–	50	–	ns
49	E Low to $\overline{AS}$, $\overline{DS}$ Invalid	t_{ELSI}	–80	–	–80	–	–80	–	–80	–	ns

VI

AC ELECTRICAL SPECIFICATIONS (Continued)

(V_{CC} = 5.0 Vdc ± 5%; V_{SS} = 0 Vdc; T_A = 0°C to 70°C, Figure 31)

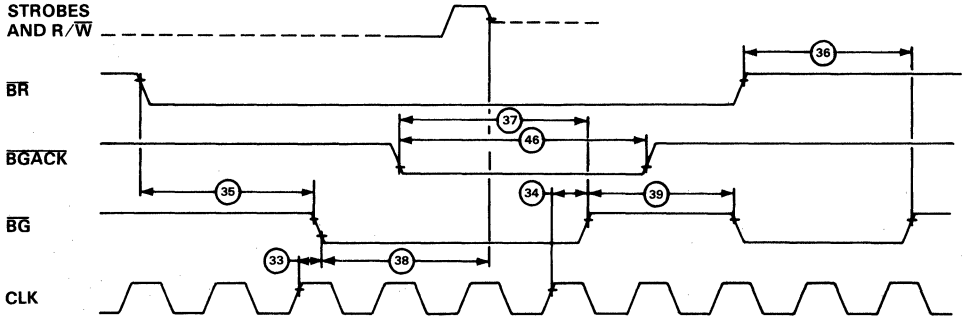
No.	Characteristic	Symbol	4 MHz MK68000-4		6 MHz MK68000-6		8 MHz MK68000-8		10 MHz MK68000-10		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
50	E Width High	t_{EH}	900	–	600	–	450	–	350	–	ns
51	E Width Low	t_{EL}	1400	–	900	–	700	–	550	–	ns
52	E Extended Rise Time	t_{CIEHX}	80	–	80	–	80	–	80	–	ns
53	Data Hold from Clock High	t_{CHDO}	0	–	0	–	0	–	0	–	ns
54	Data Hold from E Low (Write)	t_{ELDOZ}	60	–	40	–	30	–	20	–	ns
55	R/$\overline{W}$ to Data bus Impedance change	t_{RLDO}	55	–	35	–	30	–	20	–	ns
56	Halt/$\overline{RESET}$ Pulse Width (Note 4)	t_{HRPW}	10	–	10	–	10	–	10	–	clk. per.

NOTES:

1. For a loading capacitance of less than or equal to 50 picofarads, subtract 5 nanoseconds from the values given in these columns.
2. Actual value depends on actual clock period.
3. If #47 is satisfied for both $\overline{DTACK}$ and $\overline{BERR}$, #48 may be 0 ns.
4. After V_{CC} has been applied for 100 ms.
5. If the asynchronous setup time (#47) requirements are satisfied, the $\overline{DTACK}$ low-to-data setup time (#31) requirement can be ignored. The data must only satisfy the data-in to clock-low setup time (#27) for the following cycle.

AC ELECTRICAL WAVEFORMS - BUS ARBITRATION

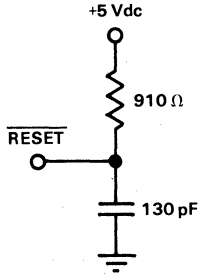
Figure 35



These waveforms should only be referenced in regard to the edge-to-edge measurement of the timing specifications. They are not intended as a functional description of the input and output signals. Refer to other functional descriptions and their related diagrams for device operation.

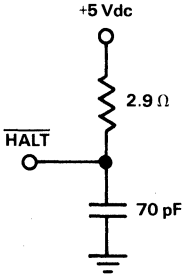
RESET TEST LOAD

Figure 36



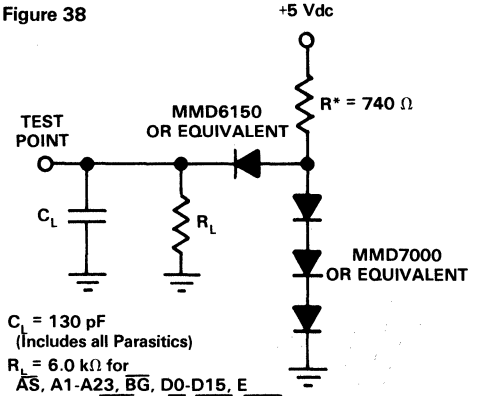
HALT TEST LOAD

Figure 37



TEST LOADS

Figure 38



C_L = 130 pF (Includes all Parasitics)

R_L = 6.0 kΩ for $\overline{AS}$, A1-A23, $\overline{BG}$, D0-D15, E FC0-FC2, $\overline{LDS}$, R/$\overline{W}$, $\overline{UDS}$, $\overline{VMA}$

*R = 1.22 kΩ for A1-A23, $\overline{BG}$, E, FC0-FC2

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0 Vdc ± 5%; V_{SS} = 0 Vdc; T_A = 0°C to 70°C, Figures 33, 34, 35)

Characteristic		Symbol	Min	Max	Unit
Input High Voltage		V_{IH}	2.0	V_{CC}	Vdc
Input Low Voltage		V_{IL}	V_{SS} - 0.3	0.8	Vdc
Input Leakage Current @ 5.25 V	$\overline{BERR}$, $\overline{BGACK}$, $\overline{BR}$, $\overline{VPA}$, $\overline{DTACK}$, $\overline{CLOCK}$, $\overline{IPL0}$-$\overline{IPL2}$	I_{in}	–	2.5	μAdc
	$\overline{HALT}$, $\overline{RESET}$		–	20	
Three-State (Off State) Input Current @ 2.4 V/0.4 V	$\overline{AS}$, A1-A23, D0-D15, FC0-FC2, $\overline{LDS}$, R/$\overline{W}$, $\overline{UDS}$, $\overline{VMA}$	I_{TSI}	–	20	μAdc
Output High Voltage (I_{OH} = –400 μAdc)	$\overline{AS}$, A1-A23, BG, D0-D15, E, FC0-FC2, $\overline{LDS}$, R/$\overline{W}$, $\overline{UDS}$, $\overline{VMA}$	V_{OH}	2.4	–	Vdc
	E*		V_{CC}–0.75		
Output Low Voltage					
(I_{OL} = 1.6mA)	$\overline{HALT}$		–	0.5	
(I_{OL} = 3.2mA)	A1-A23, $\overline{BG}$, E, FC0-FC2		–	0.5	
(I_{OL} = 5.0mA)	$\overline{RESET}$	V_{OL}	–	0.5	Vdc
(I_{OL} = 5.3mA)	E, $\overline{AS}$, D0-D15, $\overline{LDS}$, R/W, $\overline{UDS}$, $\overline{VMA}$		–	0.5	
Power Dissipation (Clock Frequency = 8 MHz)		P_D	–	1.5 W	W
Capacitance (Package Type Dependent) (V_{in} = 0 Vdc; T_A = 25°C; Frequency = 1 MHz)		C_{in}	–	10.0	pF

*with external pullup register of 470 Ω

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	–0.3 to + 7.0	Vdc
Input Voltage	V_{in}	–0.3 to + 7.0	Vdc
Operating Temperature	T_A	0 to 70	°C
Storage Temperature	T_{stg}	–55 to 150	°C

VI

MK68000 ORDERING INFORMATION

PART NO.	PACKAGE TYPE	MAX. CLOCK FREQUENCY	TEMPERATURE RANGE
MK68000P-4	Ceramic	4.0 MHz	0° to 70°C
MK68000P-6	Ceramic	6.0 MHz	
MK68000P-8	Ceramic	8.0 MHz	
MK68000P-10	Ceramic	10.0 MHz	

MOSTEK®

MICROCOMPUTER COMPONENTS

16-Bit Single-Chip Microcomputer

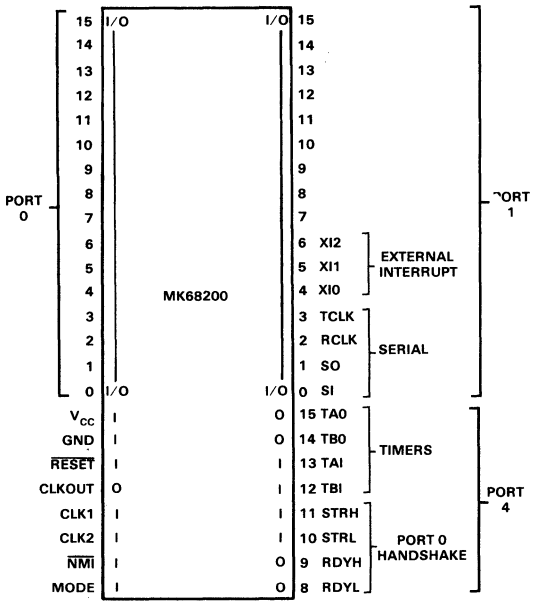
MK68200

FEATURES

- 16-bit high performance single-chip microcomputer
- 14 address and data registers
  - Eight 16-bit or sixteen 8-bit data registers
  - Six 16-bit address registers
- Advanced 16-bit instruction set
  - Bit, byte, and word operands
  - 9 Addressing modes
  - Byte and word BCD arithmetic
- High performance (6 MHz clock)
  - 500 ns register-to-register move or add
  - 3.5 μs 16x16 multiply
  - 4.0 μs 32/16 divide
- 4K byte ROM (2K x 16)
- 256 byte RAM (128 x 16)
- Three 16-bit timers
  - Interval modes
  - Event modes
  - One-shot modes
  - Pulse and period measurement modes
  - Two input and two output pins
- Serial channel
  - Double buffered receive and transmit
  - Asynchronous to 250 Kbps
  - Synchronous to 1 Mbps
  - Address wake-up recognition and generation
  - Internal/external Baud rate generation
- Parallel I/O
  - Up to 40 pins
  - Direction programmable by bit
  - 8- or 16-bit ports with handshaking
- Interrupt controller
  - 16 independent vectors
  - 8 external interrupt sources
  - 1 non-maskable interrupt
  - Individual interrupt masking
- Optional external bus
  - 16-bit multiplexed address/data bus
  - Mask-programmable control bus options
  - MK68000-compatible bus
  - General-purpose bus
  - Automatic bus request/grant arbitration
- 6 MHz clock
  - Crystal or external TTL clock
- Single +5 volt power supply
- 48 pin DIP

MK68200 LOGICAL PIN OUT

Figure 1



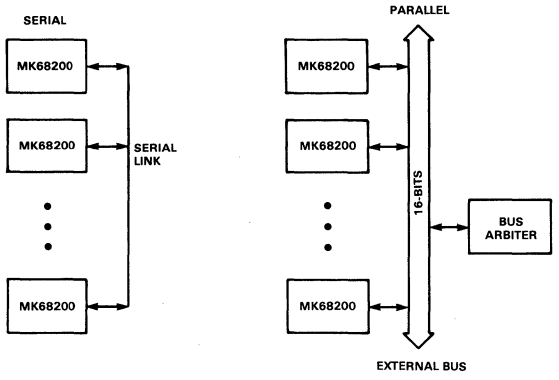
INTRODUCTION

The MK68200 is the first of a new family of high-performance 16-bit single-chip microcomputers from Mostek. Implemented in Scaled Poly-5 NMOS, it combines a modern, comprehensive instruction set architecture with extensive, flexible I/O capabilities. 4K Bytes of on-chip ROM and 256 Bytes of on-chip RAM are provided within a full 64K Byte Address Space, allowing for expansion in future family members. In addition, the on-chip I/O capabilities will change and grow to meet the needs of the marketplace.

The MK68200 is designed to serve the needs of microcomputer applications requiring high performance and low cost, such as industrial control and instrumentation. High speed mathematical ability, rapid I/O addressing and interrupt response, and powerful bit manipulation instructions provide the necessary tools for these applications. Also, where multiple processors or distributed intelligence is required, several MK68200 processors may be interconnected by either a single serial channel or a shared parallel bus as illustrated in Figure 2. The on-chip resources such as ROM, RAM, and I/O are accessed within each MK68200 without affecting the utilization of the shared bus so that only external communications compete for bus bandwidth.

DISTRIBUTED PROCESSING

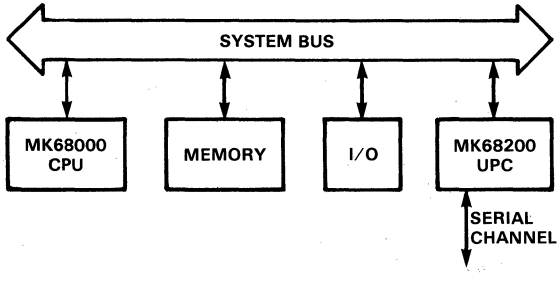
Figure 2



In addition, the MK68200 can be used as a very cost-effective peripheral controller in MK68000 systems. Here, the MK68200's instruction set similarity and direct bus compatibility with the MK68000 make it an ideal choice to perform many intelligent I/O functions in the system. For instance, since the MK68200 includes both a serial channel and an external bus capable of performing DMA transfers, it can be programmed to act as a Serial DMA Controller, as shown in Figure 3.

SERIAL DMA CONTROLLER

Figure 3



PROCESSOR ARCHITECTURE

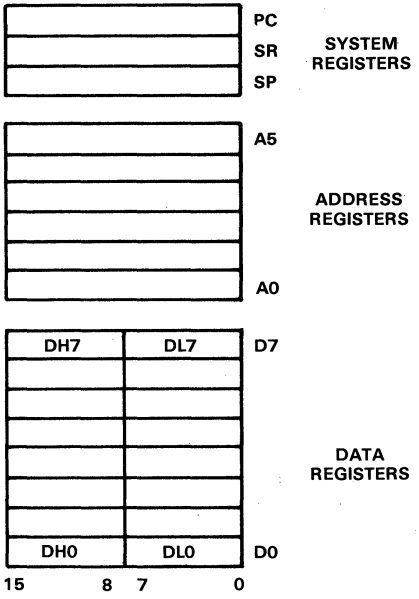
The MK68200 microcomputer contains an advanced processor architecture, combining the best properties of both 8- and 16-bit processors, since most instructions operate on either byte or word operands.

REGISTERS

The MK68200 register set includes 3 system registers, 6 address registers, and 8 data registers. The three 16-bit system registers, as shown in Figure 4, include a Program Counter, Status Register, and Stack Pointer. The 6 address registers may be used either for 16-bit data or for memory addressing. The eight 16-bit data registers are used for data and may also be referenced as sixteen 8-bit registers, providing great flexibility in register allocation.

REGISTER SET

Figure 4

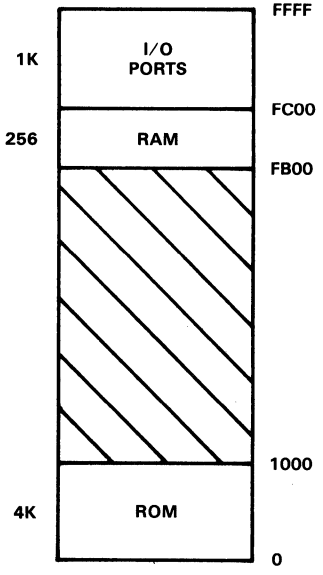


ADDRESSING

The MK68200 directly addresses a 64K byte memory space, which is organized as 32K 16-bit words. The memory is byte-addressable, but most transfers occur 16 bits at a time for increased performance over 8-bit microcomputers. All Input/Output is memory-mapped, and the on-chip I/O is situated in the top 1K bytes of the address space, as depicted in Figure 5.

ADDRESS SPACE

Figure 5



Nine addressing modes provide ease of access to data in the MK68200, as depicted in Table 1. The four Register Indirect forms utilize the address registers and the stack pointer and support many common data structures such as arrays, stacks, queues, and linked lists. I/O Port addressing is a short form address for the first 16 words of the I/O port space and allows most instructions to access the most often referenced I/O data in just one word. Many microcomputer applications are I/O intensive, and short, fast addressing of I/O has a significant impact on performance.

ADDRESSING MODES

Table 1

Register
Register Indirect
Register Indirect with Post-increment
Register Indirect with Pre-decrement
Register Indirect with Displacement
Program Counter Relative
Memory Absolute
Immediate
I/O Port

INSTRUCTIONS

The MK68200 instruction set has been designed with regularity and ease of programming in mind. In addition, instructions have been encoded to minimize code space, a feature which is especially important in single-chip microcomputers. Small code space is related to execution speed, and most instructions execute in either 3 or 6 clock periods. (A clock period is equal to 167 ns with a 6 MHz clock.) See Table 2.

INSTRUCTION EXECUTION TIMES

Table 2

Instruction Type	Clock Periods	Execution Time with 6 MHz clock (μs)
Move Register-to-register	3	0.5
Add Register-to-register (binary or BCD)	3	0.5
Move Memory-to-register	6	1.0
Add Register-to-memory	9	1.5
Multiply (16x16)	21	3.5
Divide (32/16)	23	3.84
Move Multiple (save or restore all registers)	55	9.2

In addition to operations on bytes and words, the MK68200 has rapid bit manipulation instructions which can operate on both registers and memory. The bit to be affected may be an immediate operand of the instruction or may be dynamically specified in a register. Operations available include bit set, clear, test, change, and exchange; and all bit operations always perform a bit test as well. Since each instruction is indivisible, this provides the necessary test-and-set function for the implementation of semaphores.

The MOVE group of instructions has the most extensive capabilities. A wide variety of combinations of addressing modes are supported, including memory-to-memory transfers. A special Move Multiple is included to save and restore a specified portion of the registers rapidly.

In total, the MK68200 instruction set provides a programming environment similar to the MK68000 which has been optimized for the needs of the single-chip microcomputer marketplace. A summary of the instruction set is provided in Table 3.

INPUT/OUTPUT ARCHITECTURE

The I/O capabilities of the MK68200 are extensive, encompassing timers, a serial channel, parallel I/O, and an interrupt controller. All of these devices are accessible to the programmer as ports within the top 1K bytes of the address space, and the most commonly accessed ports may be accessed with the short Port Addressing mode.

In total, 40 pins out of the 48 are used for I/O, and the functions they perform are highly programmable by the user. In particular, many pins can perform multiple functions and the programmer selects which ones are to be

INSTRUCTION SET SUMMARY

Table 3

INST	DESCRIPTION	INST	DESCRIPTION
ADD	Add	HALT	Halt
ADD.B	Add Byte	JMPA	Jump Absolute
ADDC	Add with Carry	JMPR	Jump Relative
ADDC.B	Add with Carry Byte	LIBA	Load Indexed Byte Address
AND	Logical And	LIWA	Load Indexed Word Address
AND.B	Logical And Byte	LSR	Logical Shift Right
ASL	Arithmetic Shift Left	LSR.B	Logical Shift Right Byte
ASL.B	Arithmetic Shift Left Byte	MOVE	Move
ASR	Arithmetic Shift Right	MOVE.B	Move Byte
ASR.B	Arithmetic Shift Right Byte	MOVEM	Move Multiple Registers
BCHG	Bit Test and Change	MOVEM.B	Move Multiple Registers Byte
BCLR	Bit Test and Clear	MULS	Multiply Signed
BEXG	Bit Test and Exchange	MULU	Multiply Unsigned
BSET	Bit Test and Set	NEG	Negate
BTST	Bit Test	NEG.B	Negate Byte
CALLA	Call Absolute	NEGC	Negate with Carry
CALLR	Call Relative	NEGC.B	Negate with Carry Byte
CLR	Clear	NOP	No Operation
CLR.B	Clear Byte	NOT	One's Complement
CMP	Compare	NOT.B	One's Complement Byte
CMP.B	Compare Byte	OR	Logical Or
DADD	Decimal Add	OR.B	Logical Or Byte
DADD.B	Decimal Add Byte	POP	Pop
DADDC	Decimal Add with Carry	POPM	Pop Multiple Registers
DADDC.B	Decimal Add with Carry Byte	PUSH	Push
DI	Disable Interrupts	PUSHM	Push Multiple Registers
DIVU	Divide Unsigned	RET	Return from Subroutine
DJNZ	Decrement Count and Jump if Non-zero	RETI	Return from Interrupt
		ROL	Rotate Left
DJNZ.B	Decrement Count Byte and Jump if Non-zero	ROL.B	Rotate Left Byte
		ROLC	Rotate Left through Carry
DNEG	Decimal Negate	ROLC.B	Rotate Left through Carry Byte
DNEG.B	Decimal Negate Byte	ROR	Rotate Right
DNEGC	Decimal Negate with Carry	ROR.B	Rotate Right Byte
DNEGC.B	Decimal Negate with Carry Byte	RORC	Rotate Right through Carry
DSUB	Decimal Subtract	RORC.B	Rotate Right through Carry Byte
DSUB.B	Decimal Subtract Byte	SUB	Subtract
DSUBC	Decimal Subtract with Carry	SUB.B	Subtract Byte
DSUBC.B	Decimal Subtract with Carry Byte	SUBC	Subtract with Carry
EI	Enable Interrupts	SUBC.B	Subtract with Carry Byte
EOR	Exclusive Or	TEST	Test
EOR.B	Exclusive Or Byte	TEST.B	Test Byte
EXG	Exchange	TESTN	Test Not
EXG.B	Exchange Byte	TESTN.B	Test Not Byte
EXT	Extend Sign		

used. For example, TAI may be used as an input for Timer A, an interrupt source, or a general input pin, and the interrupt source may be selected simultaneously with either of the other functions. Refer to the Logical Pin Out, Figure 1.

TIMERS

There are 3 full 16-bit timers on-chip. The first two (A and B) provide a variety of functions while the third (C) may be used either as an interval timer or a baud rate generator for the serial channel. Most significant timer events, such as a count match or a timer input signal transition can generate interrupts to the processor. Timers A and B also each have associated input and output pins.

TIMER MODES

Table 4

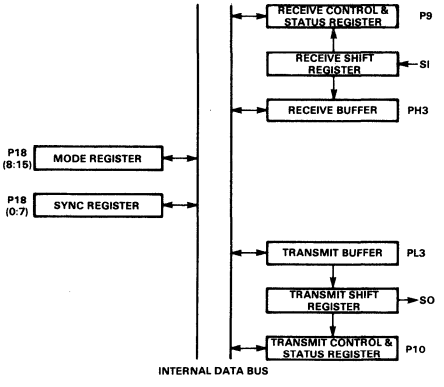
Timer	Modes
A	Interval
A	Event
A	Pulse Width and Period Measurement
B	Interval
B	Retriggerable One-shot
B	Non-retriggerable One-shot
C	Interval
C	Baud Rate Generation

SERIAL CHANNEL

The Serial Channel on the MK68200, as shown in Figure 6, is a full-duplex USART with double buffering on both transmit and receive. Word length, parity, stop bits, and modes are fully programmable. The asynchronous mode supports bit rates up to 250 Kbps, and the byte synchronous mode operates up to 1 Mbps. Either internal or external clocks may be used.

SERIAL CHANNEL

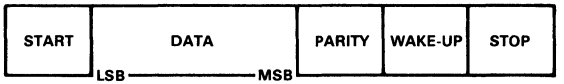
Figure 6



In addition to the typical USART functions, the serial channel can transmit and receive several special wake-up modes by appending a Wake-up bit to each data word, as illustrated in Figure 7.

SERIAL FRAME WITH WAKE-UP

Figure 7



This Wake-up bit is used to differentiate normal data words and special address words. The receiver can be programmed to receive only address words or only address words with a specific data value. In this way, the processor can be interrupted only when it receives its particular address and can then change mode to receive the following data words. Wake-up capability is especially useful when several MK68200 microcomputers are interconnected on one serial link.

PARALLEL I/O

Two 16-bit ports, P0 and P1, may be used for parallel I/O. If individual bits are desired, each of the 32 bits may be separately defined as input or output. Bits may be grouped to provide the exact data widths desired. Port 0 has the additional capability of operating under the control of external handshaking signals. 8- or 16-bit sections of P0 may be individually controlled as input, output, or bidirectional I/O. Two pairs of Ready and Strobe signals provide the necessary control.

INTERRUPT CONTROLLER

The MK68200 interrupt controller provides rapid service of up to 16 interrupt sources, each with a unique internal vector. The lowest 16 words of the address space contain the starting addresses of the service routines of each potential interrupt source, as shown in Figure 8.

Interrupt sources are prioritized in the order shown, with Reset having highest priority. A single non-maskable interrupt (NMI) is provided. All of the other sources share an interrupt enable bit in the processor status register. This bit is automatically cleared whenever an interrupt is acknowledged. Also, each of these sources has a corresponding individual enable bit. This feature allows selective enabling of particular interrupts, including the ability to choose any priority scheme desired with only minimal software overhead. In fact, 15 levels of nested priority may be programmed.

EXTERNAL BUS

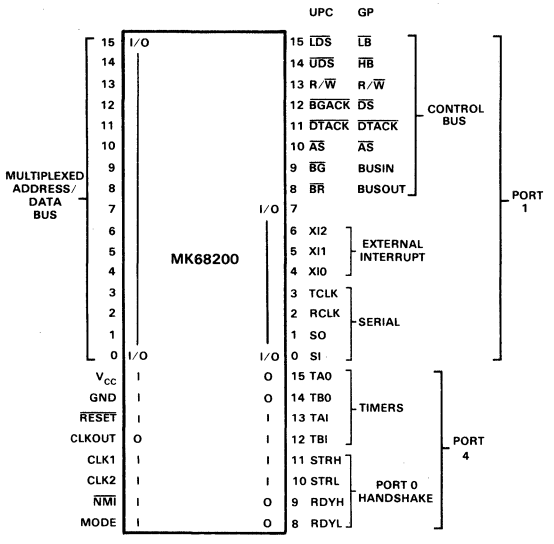
When it is necessary to expand beyond the on-chip complement of RAM, ROM, or I/O, or when DMA access to external memory space is desired, the MK68200 may be placed in an external bus mode. The selection of single-chip

INTERRUPT SOURCES
Figure 8

NAME	MNEMONIC	VECTOR LOCATION	
Reset	RESET	0000	LEVEL 2
Non-Maskable Interrupt	NMI	0002	
Spare	S	0004	LEVEL 1
External Interrupt 2	XI2	0006	
Strobe 'L'	STRL	0008	
Timer 'A' Output Interrupt	TAOI	000A	
Timer 'A' Input	TAI	000C	
Strobe 'H'	STRH	000E	
Receive Special Condition Interrupt	RSCI	0010	
Receive Normal Interrupt	RNI	0012	
External Interrupt 1	XI1	0014	
Timer 'B' Output Interrupt	TBOI	0016	
Timer 'B' Input	TBI	0018	
External Interrupt 0	XI0	001A	
Transmit Interrupt	XMTI	001C	
Timer C Interrupt	TCI	001E	

I/O or external bus is accomplished by the Mode pin at Reset time. Port 0 and a portion of Port 1 are reconfigured to provide the necessary bus functions. Figure 9 illustrates the external bus logical pin out.

EXTERNAL BUS LOGICAL PIN OUT
Figure 9



Port 0 becomes the 16-bit multiplexed Address/Data bus, and half of Port 1 becomes the Control bus. Two different Control busses are available as a mask-option: a Universal Peripheral Controller (UPC) bus which generates MK68000-compatible control signals and a General Purpose (GP) bus which provides control signals which can be used to interface to a wide variety of existing busses.

UPC CONTROL BUS

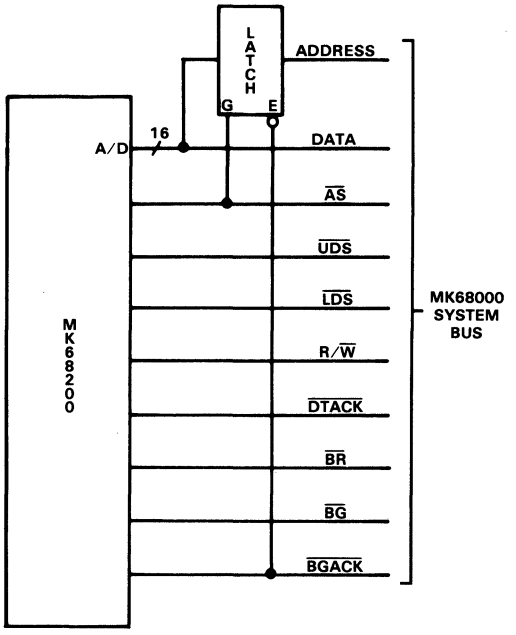
The UPC Control bus is easily connected to an MK68000 system bus with the simple addition of an external address latch, as shown in Figures 3 and 10. With the UPC Control bus, the MK68200 always acts as a bus requester in a system with the MK68000 typically as a bus master. Once the UPC has gained mastership of the system bus, it may proceed to perform DMA transfers or to communicate with other I/O devices in the system.

GP CONTROL BUS

The GP Control bus is provided to allow connection to non-MK68000 systems and to support systems of multiple MK68200 microcomputers better. The control signals have been designed to be able to generate the appropriate control signals of many available bus systems, with only a small amount of external logic. For the multiple microcomputer case, the GP bus provides BUSIN and BUSOUT, two signals which are used for bus arbitration. At Reset time, these two pins are configured so that the MK68200 may act as either a bus requester or the bus granter. When several microcomputers are connected together on a shared GP

UPC BUS INTERFACE

Figure 10



bus, only a simple bus arbiter is required in external logic. If exactly two processors are used, no external logic is needed.

BUS OPERATION

As mentioned previously, the selection of single-chip I/O pins or an external bus is made with the Mode pin. The Mode pin is also used to determine the portion of the address space which is placed on the external bus. In all cases, the on-chip I/O Ports and on-chip RAM are retained. However, the on-chip ROM may be either kept or removed from the address space. Keeping the ROM allows the designer primarily to access internal resources with occasional external references. This mode allows the maximum amount of concurrent processing in multi-processor configurations. As long as references remain on-chip, the external bus will be tri-stated and unaffected by the processor. The bus request/grant logic within the MK68200 monitors each memory reference in order to detect external bus addresses. Whenever such a reference is about to occur, the logic automatically holds the processor in an internal wait state as it proceeds to obtain mastership of the bus. As soon as the bus is obtained, the processor is allowed to continue the reference. This procedure is invisible to the running program. If the next reference is also an external address, the bus is retained.

VI

I/O PORT SUMMARY

Table 5

PORT	FUNCTION
0	16 External I/O pins
1	16 External I/O pins (including Interrupt, Serial, and Bus Control)
2	(reserved)
3	Serial Transmit (Low byte) and Receive (High byte) Buffers
4	8 External I/O pins (Timer Control and Port 0 Handshake Control)
5	(reserved)
6	(reserved)
7	Interrupt Latches
8	Interrupt Enable Register
9	Serial I/O Receive Control and Status Register
10	Serial I/O Transmit Control and Status Register
11	Timer B Latch
12	Timer A, Low Latch
13	Timer A, High Latch
14	Timer Control, Interrupt Edge Select
15	Port 0 Handshake Mode bits, Bus Lock, Bus Segment bits
16	Port 0 Direction Control (DDR0)
17	Port 1 Direction Control (DDR1)
18	Serial I/O Mode and Sync Registers
19	Timer C Latch

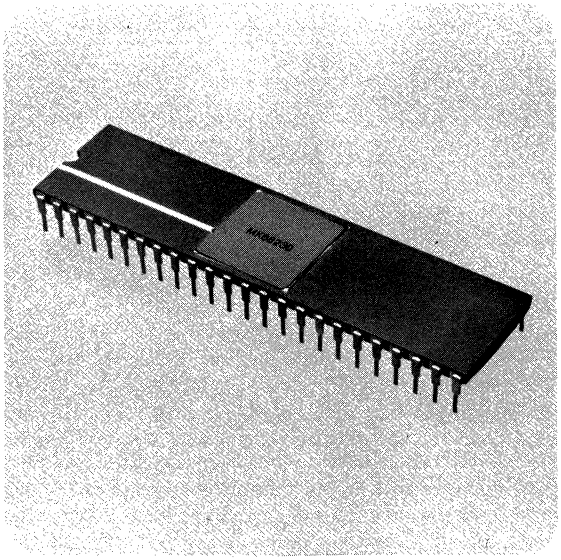
PRELIMINARY

PARALLEL INTERFACE/TIMER (PI/T)
MK68230P8/MK68230P10

MK68230 PARALLEL INTERFACE/TIMER

The MK68230 Parallel Interface/Timer provides versatile double buffered parallel interfaces and an operating system oriented timer to MK68000 systems. The parallel interfaces operate in unidirectional or bidirectional modes, either 8 or 16 bits wide. In the unidirectional modes, an associated data direction register determines whether the port pins are inputs or outputs. In the bidirectional modes the data direction registers are ignored and the direction is determined dynamically by the state of four handshake pins. These programmable handshake pins provide an interface flexible enough for connection to a wide variety of low, medium, or high speed peripherals or other computer systems. The PI/T ports allow use of vectored or autovectored interrupts, and also provide a DMA Request pin for connection to the MK68450 Direct Memory Access Controller or a similar circuit. The PI/T timer contains a 24-bit wide counter and a 5-bit prescaler. The timer may be clocked by the system clock (PI/T CLK pin) or by an external clock (TIN pin), and a 5-bit prescaler can be used. It can generate periodic interrupts, a square wave, or a single interrupt after a programmed time period. Also it can be used for elapsed time measurement or as a device watchdog.

- MK68000 Bus Compatible
- Port Modes Include:
  Bit I/O
  Unidirectional 8-Bit and 16-Bit
  Bidirectional 8-Bit and 16-Bit
- Selectable Handshaking Options
- 24-Bit Programmable Timer
- Software Programmable Timer Modes
- Contains Interrupt Vector Generation Logic
- Separate Port and Timer Interrupt Service Requests
- Registers are Read/Write and Directly Addressable
- Registers are Addressed for MOVEP (Move Peripheral) and DMAC Compatibility



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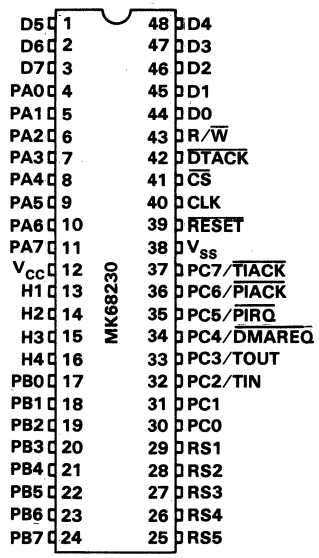
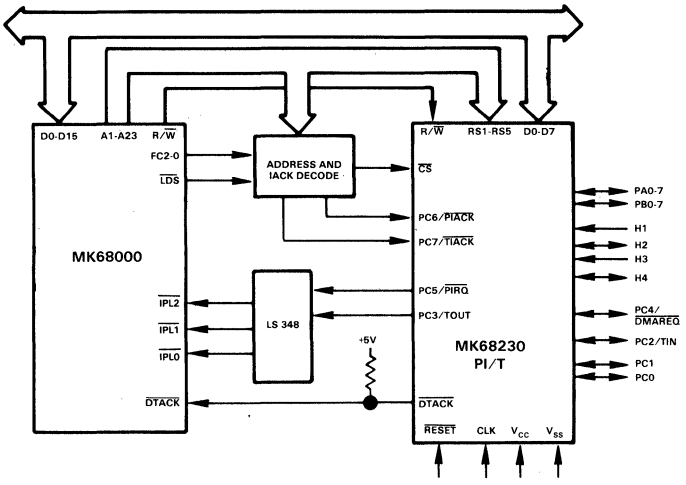
PIN ASSIGNMENT



PI/T SYSTEM BLOCK DIAGRAM

Figure 1



GENERAL DESCRIPTION

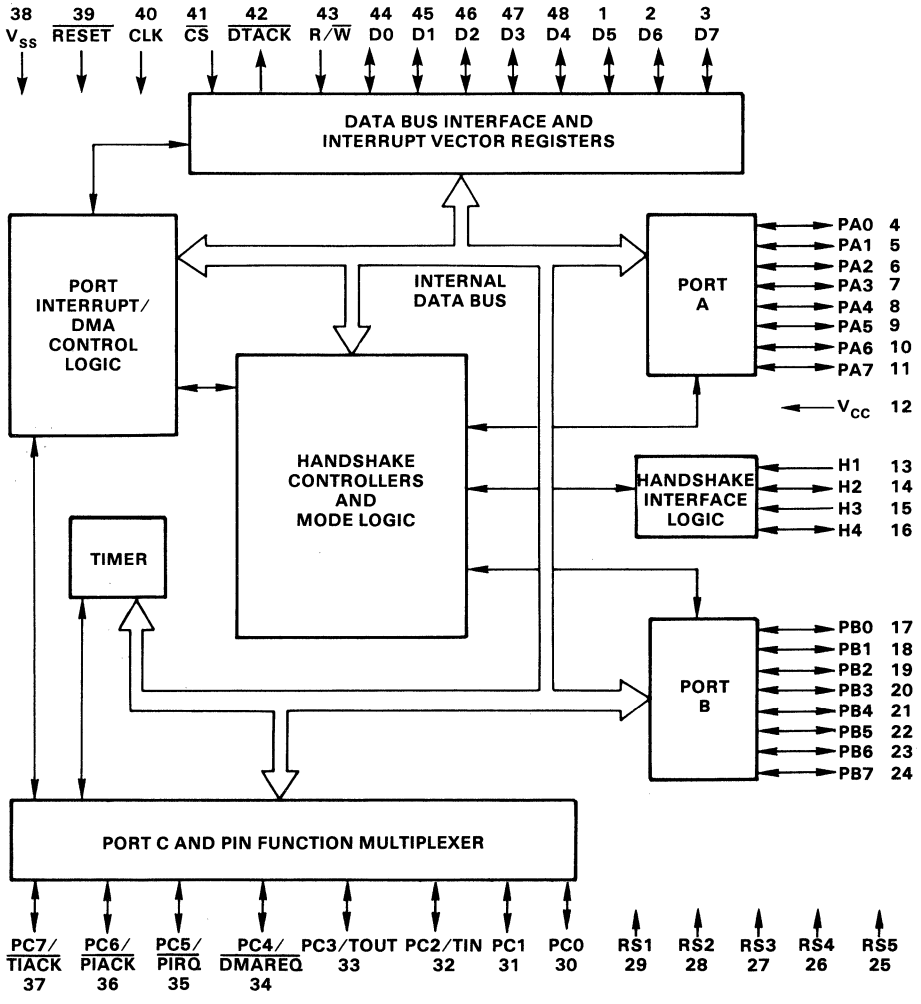
The PI/T consists of two logically independent sections: the ports and the timer. The port section consists of Port A (PA0-7), Port B (PB0-7), four handshake pins (H1, H2, H3, and H4), two general I/O pins, and six dual-function pins. The dual-function pins can individually operate as a third port (Port C) or an alternate function related to either Ports A and B, or the timer. The four programmable handshake pins, depending on the mode, can control data transfer to and from the ports, or can be used as interrupt generating inputs, or I/O pins.

The timer consists of a 24-bit counter, optionally clocked by a 5-bit prescaler. Three pins provide complete timer I/O: PC2/TIN, PC3/TOUT, and PC7/$\overline{\text{TIACK}}$. Of course, only the ones needed for the given configuration perform the timer function, while the others remain Port C I/O.

The system bus interface provides for asynchronous transfer of data from the PI/T to a bus master over the data bus (D0-D7). Data transfer acknowledge ($\overline{\text{DTACK}}$), register selects (RS1-RS5), chip select, the read/write line (R/$\overline{\text{W}}$), and Port Interrupt Acknowledge ($\overline{\text{PIACK}}$) or Timer Interrupt Acknowledge ($\overline{\text{TIACK}}$) control data transfer between the PI/T and the MK68000.

MK68230 BLOCK DIAGRAM

Figure 2



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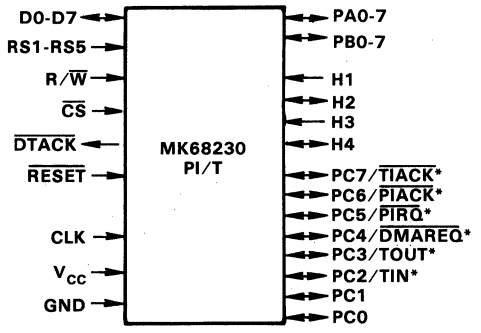
PI/T PIN DESCRIPTION

Throughout the data sheet, signals are presented using the terms active and inactive or asserted and negated independent of whether the signal is active in the high-voltage state or low-voltage state. (The active state of each logic pin is given below.) Active low signals are denoted by a superscript bar. R/$\overline{W}$ indicates a 'write' is active low and a 'read' active high.

LOGICAL PIN ASSIGNMENT

Figure 3



*Individually Programmable Dual-Function Pin

D0-D7 — Bidirectional Data Bus. The data bus pins D0-D7 form an 8-bit bidirectional data bus to/from the MK68000 or other bus master. These pins are active high.

RS1-RS5 — Register Selects. RS1-RS5 are active high high-impedance inputs that determine which of the 25 possible registers is being addressed. They are provided by the MK68000 or other bus master.

R/$\overline{W}$ — Read/Write Input. R/$\overline{W}$ is the high-impedance Read/Write signal from the MK68000 or bus master, indicating whether the current bus cycle is a read (high) or write (low) cycle.

$\overline{CS}$ — Chip Select Input. $\overline{CS}$ is a high-impedance input that selects the PI/T registers for the current bus cycle. Address strobe and the data strobe (upper or lower) of the bus master, along with the appropriate address bits, must be included in the chip select equation. A low level corresponds to an asserted chip select.

$\overline{DTACK}$ — Data Transfer Acknowledge Output. $\overline{DTACK}$ is an active low output that signals the completion of the bus cycle. During read or interrupt acknowledge cycles, $\overline{DTACK}$ is asserted by the MK68230 after data has been provided on the data bus; during write cycles it is asserted after data has been accepted at the data bus. Data transfer acknowledge is compatible with the MK68000 and with other Mostek bus masters such as the MK68450 DMA controller. A holding resistor is required to maintain $\overline{DTACK}$ high between bus cycles.

$\overline{RESET}$ — Reset Input. $\overline{RESET}$ is a high-impedance input used to initialize all PI/T functions. All control and data direction registers are cleared and most internal operations are disabled by the assertion of $\overline{RESET}$ (low).

CLK — Clock Input. The clock pin is a high-impedance TTL-compatible signal with the same specifications as the MK68000. The PI/T contains dynamic logic throughout, and hence this clock must not be gated off at any time. It is not necessary that this clock maintain any particular phase relationship with the MK68000 clock. It may be connected to an independent frequency source (faster or slower) as long as all bus specifications are met.

PA0-PA7 and PB0-PB7 — Port A and Port B. Ports A and B are 8-bit ports that may be concatenated to form a 16-bit port in certain modes. The ports may be controlled in conjunction with the handshake pins H1-H4. For stabilization during system power-up, Ports A and B have internal pullup resistors to V_{CC}. All port pins are active high.

H1-H4 — Handshake pins (I/O depending on the Mode and Submode). Handshake pins H1-H4 are multi-purpose pins that (depending on the operational mode) may provide an interlocked handshake, a pulsed handshake, an interrupt input (independent of data transfers), or simple I/O pins. For stabilization during system power-up, H2 and H4 have internal pullup resistors to V_{CC}. Their sense (active high or low) may be programmed in the Port General Control Register bits 3-0. Independent of the mode, the instantaneous level of the handshake pins can be read from the Port Status Register.

Port C — (PC0-PC7/Alternate function). This port can be used as eight general purpose I/O pins (PC0-PC7) or any combination of six special function pins and two general purpose I/O pins (PC0-PC1). (Each dual function pin can be standard I/O or a special function independent of the other port C pins.) The dual function pins are defined in the following paragraphs. When used as a port C pin, these pins are active high. They may be individually programmed as inputs or outputs by the Port C Data Direction Register.

The alternate functions (TIN, TOUT, and $\overline{TIACK}$) are timer I/O pins. TIN may be used as a rising-edge triggered external clock input or an external run/halt control pin (the timer is in the run state if run/halt is high and in the halt state if run/halt is low). TOUT may provide an active low timer interrupt request output or a general-purpose square-wave output, initially high. $\overline{TIACK}$ is an active low high-impedance input used for timer interrupt acknowledge.

Port A and B functions have an independent pair of active low interrupt request ($\overline{PIRQ}$) and interrupt acknowledge ($\overline{PIACK}$) pins.

The $\overline{DMAREQ}$ (Direct Memory Access Request) pin provides an active low Direct Memory Access Controller

(DMAC) request pulse of 3 clock cycles, completely compatible with the MK68450 DMAC.

REGISTER MODEL

A register model that includes the corresponding Register Selects is shown in Table 1.

REGISTER MODEL

Table 1

Register Select Bits 5	4	3	2	1	7	6	5	4	3	2	1	0	
0	0	0	0	0	Port Mode Control		H34 Enable	H12 Enable	H4 Sense	H3 Sense	H2 Sense	H1 Sense	Port General Control Register
0	0	0	0	1	*	SVCRQ Select		Interrupt PFS		Port Interrupt Priority Control			Port Service Request Register
0	0	0	1	0	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Port A Data Direction Register
0	0	0	1	1	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Port B Data Direction Register
0	0	1	0	0	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Port C Data Direction Register
0	0	1	0	1	Interrupt Vector Number						*	*	Port Interrupt Vector Register
0	0	1	1	0	Port A Submode		H2 Control			H2 Int Enable	H1 SVCRQ Enable	H1 Stat Ctrl.	Port A Control Register
0	0	1	1	1	Port B Submode		H4 Control			H4 Int Enable	H3 SVCRQ Enable	H3 Stat Ctrl.	Port B Control Register
0	1	0	0	0	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Port A Data Register
0	1	0	0	1	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Port B Data Register
0	1	0	1	0	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Port A Alternate Register
0	1	0	1	1	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Port B Alternate Register
0	1	1	0	0	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Port C Data Register
0	1	1	0	1	H4 Level	H3 Level	H2 Level	H1 Level	H4S	H3S	H2S	H1S	Port Status Register
0	1	1	1	0	*	*	*	*	*	*	*	*	(null)
0	1	1	1	1	*	*	*	*	*	*	*	*	(null)
1	0	0	0	0	TOUT/$\overline{\text{TIACK}}$ Control			Z D Ctrl.	*	Clock Control		Timer Enable	Timer Control Register
1	0	0	0	1	Bit 7	Bit 6	Bit 5	Bit 4	kBit 3	Bit 2	Bit 1	Bit 0	Timer Interrupt Vector Register
1	0	0	1	0	*	*	*	*	*	*	*	*	(null)
1	0	0	1	1	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16	Counter Preload Register (High)
1	0	1	0	0	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	(Mid)
1	0	1	0	1	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	(Low)
1	0	1	1	0	*	*	*	*	*	*	*	*	(null)
1	0	1	1	1	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16	Count Register (High)
1	1	0	0	0	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	(Mid)
1	1	0	0	1	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	(Low)
1	1	0	1	0	*	*	*	*	*	*	*	ZDS	Timer Status Register
1	1	0	1	1	*	*	*	*	*	*	*	*	(null)
1	1	1	0	0	*	*	*	*	*	*	*	*	(null)
1	1	1	0	1	*	*	*	*	*	*	*	*	(null)
1	1	1	1	0	*	*	*	*	*	*	*	*	(null)
1	1	1	1	1	*	*	*	*	*	*	*	*	(null)

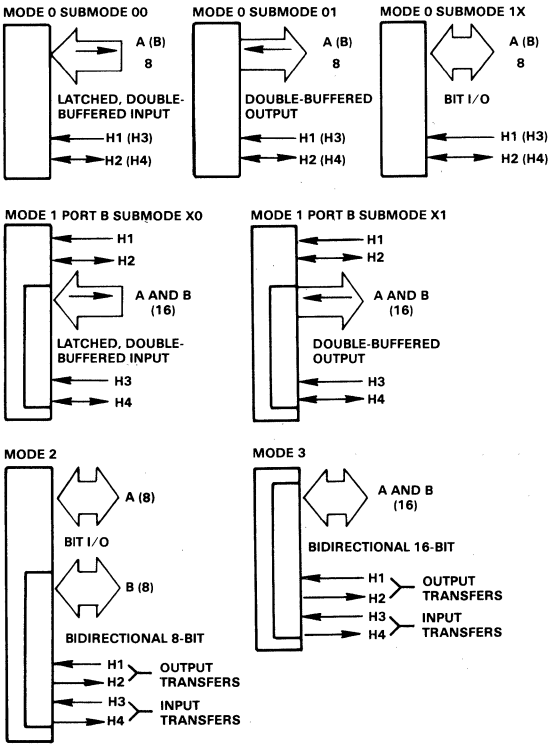
*Unused, read as zero.

PORT CONTROL STRUCTURE

The primary focus of most applications will be on Ports A and B, the handshake pins, the port interrupt pins, and the DMA request pin. They are controlled in the following way: the Port General Control Register contains a 2-bit field that specifies a set of four operation modes. These govern the overall operation of the ports and determine their interrelationships. Some modes require additional information from each port's control register to further define its operation. In each port control register, there is a 2-bit submode field that serves this purpose. Each port mode/submode combination specifies a set of programmable characteristics that fully defines the behavior of that port and two of the handshake pins. This structure is summarized in Table 2 and Figure 4.

PORT MODE LAYOUT

Figure 4



PORT MODE CONTROL SUMMARY

Table 2

Mode 0 (Unidirectional 8-Bit Mode)
- Port A
  - Submode 00 — Double-Buffered Input
    - H1 — Latches input data
    - H2 — Status/interrupt generating input, general-purpose output, or operation with H1 in the interlocked or pulsed input handshake protocols
  - Submode 01 — Double-Buffered Output
    - H1 — Indicates data received by peripheral
    - H2 — Status/interrupt generating input, general-purpose output, or operation with H1 in the interlocked or pulsed input handshake protocols
  - Submode 1X — Bit I/O
    - H1 — Status/interrupt generating input
    - H2 — Status/interrupt generating input or general-purpose output
- Port B, H3 and H4 — Identical to Port A, H1 and H2

Mode 1 (Unidirectional 16-Bit Mode)
- Port A — Double-Buffered Data (Most significant)
  - Submode XX (not used)
    - H1 — Status/interrupt generating input
    - H2 — Status/interrupt generating input or general-purpose output
- Port B — Double-Buffered Data (Least significant)
  - Submode X0 — Unidirectional 16-Bit Input
    - H3 — Latches input data
    - H4 — Status/interrupt generating input, general-purpose output, or operation with H3 in the interlocked or pulsed input handshake protocols
  - Submode X1 — Unidirectional 16-Bit Output
    - H3 — Indicates data received by peripheral
    - H4 — Status/interrupt generating input, general-purpose output, or operation with H3 in the interlocked or pulsed input handshake protocols

Mode 2 (Bidirectional 8-Bit Mode)
- Port A — Bit I/O (with no handshaking pins)
  - Submode XX (not used)
- Port B — Bidirectional 8-Bit Data (Double-Buffered)
  - Submode XX (not used)
    - H1 — Indicates output data received by peripheral
    - H2 — Operation with H1 in the interlocked or pulsed output handshake protocols
    - H3 — Latches input data
    - H4 — Operation with H3 in the interlocked or pulsed input handshake protocols

Mode 3 (Bidirectional 16-Bit Mode)
- Port A — Double-Buffered Data (Most significant)
  - Submode XX (not used)
- Port B — Double-Buffered Data (Least significant)
  - Submode XX (not used)
- H1 — Indicates output data received by peripheral
- H2 — Operation with H1 in the interlocked or pulsed output handshake protocols
- H3 — Latches input data
- H4 — Operation with H3 in the interlocked or pulsed input handshake protocols

PORT GENERAL INFORMATION AND CONVENTIONS

The following paragraphs introduce concepts that are generally applicable to the PI/T ports independent of the chosen mode and submode. For this reason, no particular port or handshake pins are mentioned; the notation H1 (H3) indicates that, depending on the chosen mode and submode, the statement given may be true for either the H1 or H3 handshake pin.

UNIDIRECTIONAL VS BIDIRECTIONAL — Figure 4 shows the configuration of Ports A and B and each of the handshake pins in each port mode and submode. In Modes 0 and 1, a data direction register is associated with each of the ports. These registers contain one bit for each port pin to determine whether that pin is an input or an output. Modes 0 and 1 are, thus, called unidirectional modes because each pin assumes a constant direction, changeable only by a reset condition or a programming change. These modes allow double-buffered data transfers in one direction. This direction, determined by the mode and submode definition, is known as the primary direction. Data transfers in the primary direction are controlled by the handshake pins. Data transfers not in the primary direction are generally unrelated, and single or unbuffered data paths exist.

In Modes 2 and 3 there is no concept of primary direction as in Modes 0 and 1. Except for Port A in Mode 2 (Bit I/O), the data direction registers have no effect. These modes are bidirectional, in that the direction of each transfer (always 8 or 16 bits, double-buffered) is determined dynamically by the state of the handshake pins. Thus, for example, data may be transferred out of the ports, followed very shortly by a transfer into the same port pins. Transfers to and from the ports are independent and may occur in any sequence. Since the instantaneous direction is always determined by the external system, a small amount of arbitration logic may be required.

CONTROL OF DOUBLE-BUFFERED DATA PATHS — Generally speaking, the PI/T is a double-buffered device. In the primary direction, double-buffering allows orderly transfers by using the handshake pins in any of several programmable protocols. (When Bit I/O is used, double-buffering is not available and the handshake pins are used as outputs or status/interrupt inputs.)

Use of double-buffering is most beneficial in situations where a peripheral device and the computer system are capable of transferring data at roughly the same speed. Double-buffering allows the fetch operation of the data transmitter to be overlapped with the store operation of the data receiver. Thus, throughput measured in bytes or words-per-second may be greatly enhanced. If there is a large mismatch in transfer capability between the computer and the peripheral, little or no benefit is obtained. In these cases there is no penalty in using double-buffering.

DOUBLE-BUFFERED INPUT TRANSFERS — In all modes, the PI/T supports double-buffered input transfers. Data that meets the port setup and hold times is latched on the asserted edge of H1(H3). H1(H3) is edge-sensitive, and may assume any duty-cycle as long as both high and low minimum times are observed. The PI/T contains a Port Status Register whose H1S(H3S) status bit is set anytime any input data is present in the double-buffered latches that have not been read by the bus master. The action of H2(H4) is programmable; it may indicate whether there is room for more data in the PI/T latches or it may serve other purposes. The following options are available, depending on the mode.

1. H2(H4) may be an edge-sensitive input that is independent of H1(H3) and the transfer of port data. On the asserted edge of H2(H4), the H2S(H4S) status bit is set. It is cleared by the direct method (refer to Direct Method of Resetting Status), the $\overline{\text{RESET}}$ pin being asserted, or when the H12 Enable (H34 Enable) bit of the Port General Control Register is 0.

2. H2(H4) may be a general purpose output pin that is always negated. The H2S(H4S) status bit is always 0.

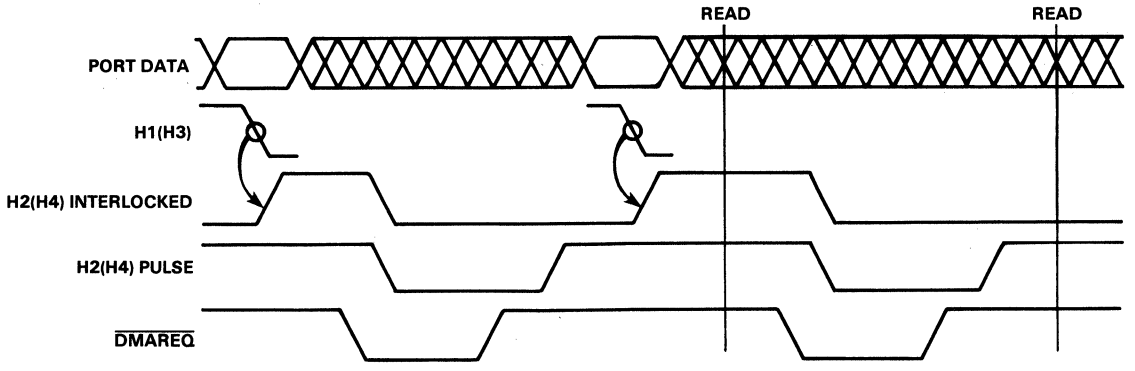
3. H2(H4) may be a general purpose output pin that is always asserted. The H2S(H4S) status bit is always 0.

4. H2(H4) may be an output pin in the interlocked input handshake protocol. It is asserted when the port input latches are ready to accept new data. It is negated asynchronously following the asserted edge of the H1(H3) input. As soon as the input latches become ready, H2(H4) is again asserted. When the input double-buffered latches are full, H2(H4) remains negated until data is removed. Thus, anytime the H2(H4) output is asserted, new input data may be entered by asserting H1(H3). At other times transitions on H1(H3) are ignored. The H2S(H4S) status bit is always 0. When H12 Enable (H34 Enable) is 0, H2(H4) is held negated.

5. H2(H4) may be an output pin in the pulsed input handshake protocol. It is asserted exactly as in the interlocked input protocol, but never remains asserted longer than 4 clock cycles. Typically, a four clock cycle pulse is generated. But in the case that a subsequent H1(H3) asserted edge occurs before termination of the pulse, H2(H4) is negated asynchronously. Thus, anytime after the leading edge of the H2(H4) pulse, new data may be entered in the PI/T double-buffered input latches. The H2S(H4S) status bit is always 0. When H12 Enable (H34 Enable) is 0, H2(H4) is held negated.

A sample timing diagram is shown in Figure 5. The H2(H4) interlocked and pulsed input handshake protocols are shown. The $\overline{\text{DMAREQ}}$ pin is also shown assuming it is enabled. All handshake pin sense bits are assumed to be 0 (refer to Port General Control Register); thus, the pins are in the low state when asserted. Due to the great similarity between modes, this timing diagram is applicable to all double-buffered input transfers.

DOUBLE-BUFFERED INPUT TRANSFERS
Figure 5



DOUBLE-BUFFERED OUTPUT TRANSFERS — The PI/T supports double-buffered output transfers in all modes. Data, written by the bus master to the PI/T, is stored in the port's output latch. The peripheral accepts the data by asserting H1(H3), which causes the next data to be moved to the port's output latch as soon as it is available. The function of H2(H4) is programmable; it may indicate whether new data has been moved to the output latch or it may serve other purposes. The H1S(H3S) status bit may be programmed for two interpretations. Normally the status bit is a 1 when there is at least one latch in the double-buffered data path that can accept new data. After writing one byte/word of data to the ports, an interrupt service routine could check this bit to determine if it could store another byte/word, thus, filling both latches. When the bus master is finished, it is often useful to be able to check whether all of the data has been transferred to the peripheral. The H1S(H3S) Status Control bit of the Port A and B Control Registers provides this flexibility. The programmable options of the H2(H4) pin are given below, depending on the mode.

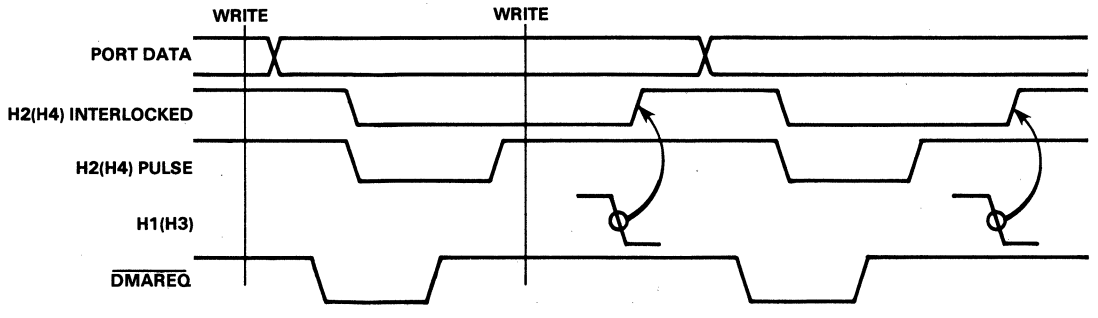
1. H2(H4) may be an edge-sensitive input pin independent of H1(H3) and the transfer of port data. On the asserted edge of H2(H4), the H2S(H4S) status bit is set. It is reset by the direct method (refer to Direct Method of Resetting Status), the $\overline{\text{RESET}}$ pin being asserted, or when the H12 Enable (H34 Enable) bit of the Port General Control Register is 0.

2. H2(H4) may be a general-purpose output pin that is always negated. The H2S(H4S) status bit is always 0.

3. H2(H4) may be a general-purpose output pin that is always asserted. The H2S(H4S) status bit is always 0.

4. H2(H4) may be an output pin in the interlocked output handshake protocol. H2(H4) is asserted two clock cycles after data is transferred to the double-buffered output latches. The data remains stable and H2(H4) remains asserted until the next asserted edge of the H1(H3) input. At that time, H2(H4) is asynchronously negated. As soon as the next data is available, it is transferred to the output latches. When H2(H4) is negated, asserted transitions on H1(H3) have no effect on the data paths. As is explained later, however, in Modes 2 and 3 they do control the three-state output buffers of the bidirectional port(s). The H2S(H4S) status bit is always 0. When H12 Enable (H34 Enable) is 0, H2(H4) is held negated.

DOUBLE-BUFFERED OUTPUT TRANSFERS
Figure 6



5. H2(H4) may be an output pin in the pulsed output handshake protocol. It is asserted exactly as in the interlocked output protocol above, but never remains asserted longer than four clock cycles. Typically, a four clock pulse is generated. But in the case that a subsequent H1(H3) asserted edge occurs before termination of the pulse, H2(H4) is negated asynchronously shortening the pulse. The H2S(H4S) status bit is always 0. When H12 Enable (H34 Enable) is 0, H2(H4) is held negated.

A sample timing diagram is shown in Figure 6. The H2(H4) interlocked and pulsed output handshake protocols are shown. The $\overline{\text{DMAREQ}}$ pin is also shown assuming it is enabled. All handshake pin sense bits are assumed to be 0; thus, the pins are in the low state when asserted. Due to the great similarity between modes, this timing diagram is applicable to all double-buffered output transfer.

REQUESTING BUS MASTER SERVICE — The PI/T has several means of indicating a need for service by a bus master. First, the processor may poll the Port Status Register. It contains a status bit for each handshake pin, plus a level bit that always reflects the instantaneous state of that handshake pin. A status bit is 1 when the PI/T needs servicing, i.e., generally when the bus master needs to read or write data to the ports, or when a handshake pin used as a simple status input has been asserted. The interpretation of these bits is dependent on the chosen mode and submode.

Second, the PI/T may be placed in the processor's interrupt structure. As mentioned previously, the PI/T contains Port A and B Control Registers that configure the handshake pins. Other bits in these registers enable an interrupt associated with each handshake pin. This interrupt is made available through the PC5/$\overline{\text{PIRQ}}$ pin, if the $\overline{\text{PIRQ}}$ function is selected. Three additional conditions are required for $\overline{\text{PIRQ}}$ to be asserted: (1) the handshake pin status bit is set, (2) the corresponding interrupt (service request) enable bit is set, and (3) DMA requests are not associated with that data transfer (H1 and H3 only). The conditions from each of the four handshake pins and corresponding status bits are ORed to determine $\overline{\text{PIRQ}}$.

The third method of requesting service is via the PC4/$\overline{\text{DMAREQ}}$ pin. This pin can be associated with double-buffered transfers in each mode. If it is used as a DMA controller request, it can initiate requests to keep the PI/T's input/output double-buffering empty/full as much as possible. It will not overrun the DMA controller. The pin is compatible with the MK68450 Direct Memory Access Controller (DMAC).

VECTORED, PRIORITIZED PORT INTERRUPTS - Use of MK68000-compatible vectored interrupts with the PI/T requires the $\overline{\text{PIRQ}}$ and $\overline{\text{PIACK}}$ pins. When $\overline{\text{PIACK}}$ is asserted, the PI/T places an 8-bit vector on the data pins D0-D7. Under normal conditions, this vector corresponds to the highest priority, enabled, active port interrupt source with which the $\overline{\text{DMAREQ}}$ pin is not currently associated. The most-significant six bits are provided by the Port Interrupt Vector Register (PIVR), with the lower two bits supplied by prioritization logic according to conditions present when $\overline{\text{PIACK}}$ is asserted. It is important to note that the only affect on the PI/T caused by interrupt acknowledge cycles is that the vector is placed on the data bus. Specifically, no registers, data, status, or other internal states of the PI/T are affected by the cycle.

Several conditions may be present when the $\overline{\text{PIACK}}$ input is asserted to the PI/T. These conditions affect the PI/T's response and the termination of the bus cycle. If the PI/T has no interrupt function selected, or is not asserting $\overline{\text{PIRQ}}$, the PI/T will make no response to $\overline{\text{PIACK}}$ ($\overline{\text{DTACK}}$ will not be asserted). If the PI/T is asserting $\overline{\text{PIRQ}}$ when $\overline{\text{PIACK}}$ is received, the PI/T will output the contents of the Port Interrupt Vector Register and the prioritization bits. If the PIVR has not been initialized, $0F will be read from this register. These conditions are summarized in Table 3.

RESPONSE TO PORT INTERRUPT ACKNOWLEDGE
Table 3

Conditions	$\overline{\text{PIRQ}}$ negated OR interrupt request function not selected	$\overline{\text{PIRQ}}$ asserted
PIVR has not been initialized since $\overline{\text{RESET}}$	No response from PI/T. No $\overline{\text{DTACK}}$.	PI/T provides $0F, the Uninitialized Vector.*
PIVR has been initialized since $\overline{\text{RESET}}$	No response from PI/T. No $\overline{\text{DTACK}}$.	PI/T provides PIVR contents with prioritization bits.

*The uninitialized vector is the value returned from an interrupt vector register before it has been initialized.

The vector table entries for the PI/T appear as a contiguous block of four vector numbers whose common upper six bits are programmed in the PIVR. The following table pairs each interrupt source with the 2-bit value provided by the prioritization logic, when interrupt acknowledge is asserted.

H1 source — 00
H2 source — 01
H3 source — 10
H4 source — 11

AUTOVECTORED PORT INTERRUPTS — Autovectored interrupts use only the $\overline{\text{PIRQ}}$ pin. The operation of the PI/T with vectored and autovectored interrupts is identical except that no vectors are supplied and the PC6/$\overline{\text{PIACK}}$ pin can be used as a Port C pin.

DIRECT METHOD OF RESETTING STATUS - In certain modes one or more handshake pins can be used as edge-sensitive inputs for the sole purpose of setting bits in the Port Status Register. These bits consist of simple flip-flops. They are set (to 1) by the occurrence of the asserted edge of the handshake pin input. Resetting a handshake status bit can be done by writing an 8-bit mask to the Port Status Register. This is called the direct method of resetting. To reset a status bit that is resettable by the direct method, the mask must contain a 1 in the bit position of the Port Status Register corresponding to the desired bit. Other positions must contain 0's. For status bits that are not resettable by the direct method in the chosen mode, the data written to the port status register has no effect. For status bits that are resettable by the direct method in the chosen mode, a 0 in the mask has no effect.

HANDSHAKE PIN SENSE CONTROL — The PI/T contains exclusive-OR gates to control the sense of each of the handshake pins, whether used as inputs or outputs. Four bits in the Port General Control Register may be programmed to determine whether the pins are asserted in the low or high voltage state. As with other control registers, these bits are reset to 0 when the $\overline{\text{RESET}}$ pin is asserted, defaulting the asserted level to be low.

ENABLING PORTS A AND B - Certain functions involved with double-buffered data transfers, the handshake pins, and the status bits, may be disabled by the external system or by the programmer during initialization. The Port General Control Register contains two bits, H12 Enable and H34 Enable, which control these functions. These bits are cleared when the $\overline{\text{RESET}}$ pin is asserted, and the functions are disabled. The functions are the following:

1. Independent of other actions by the bus master or peripheral (via the handshake pins), the PI/T's disabled handshake controller is held to the "empty" state, i.e., no data is present in the double-buffered data path.

2. When any handshake pin is used to set a simple status flip-flop, unrelated to double-buffered transfers, these flip-flops are held reset to 0. (See Table 2.)

3. When H2(H4) is used in an interlocked or pulsed handshake with H1(H3), H2(H4) is held negated, regardless of the chosen mode, submode, and primary direction. Thus, for double-buffered input transfers, the programmer may signal a peripheral when the PI/T is ready to begin transfers by setting the associated handshake enable bit to 1.

THE PORT A AND B ALTERNATE REGISTERS — In addition to the Port A and B Data Registers, the PI/T contains Port A and B Alternate Registers. These registers are read-only, and simply provide the instantaneous level of each port pin. They have no effect on the operation of the handshake pins, double-buffered transfers, status bits, or any other aspect of the PI/T, and they are mode/submode independent.

PORT MODES

This section contains information that distinguishes the various port modes and submodes. General characteristics, common to all modes, have been defined previously.

MODE 0 — UNIDIRECTIONAL 8-BIT MODE

In Mode 0, Ports A and B operate independently. Each may be configured in any of its three possible submodes:

Submode 00 — Double-Buffered Input
Submode 01 — Double-Buffered Output
Submode 1X — Bit I/O

Handshake pins H1 and H2 are associated with Port A and configured by programming the Port A Control Register. (The H12 Enable bit of the Port General Control Register enables Port A transfers.) Handshake pins H3 and H4 are associated with Port B and configured by programming the Port B Control Register. (The H34 Enable bit of the Port General Control Register enables Port B transfers.) The Port A and B Data Direction Registers operate in all three submodes. Along with the submode, they affect the data read and written at the associated data register according to Table 4. They also enable the output buffer associated with each port pin. The $\overline{\text{DMAREQ}}$ pin may be associated with either (not both) Port A or Port B, but does not function if the Bit I/O submode is programmed for the chosen port.

MODE 0 PORT DATA PATHS

Table 4

Mode	Read Port A/B Data Register		Write Port A/B Data Register	
	DDR=0	DDR=1	DDR=X	
0 Submode 00	FIL, D.B.	FOL Note 3	FOL, S.B.	Note 1
0 Submode 01	Pin	FOL Note 3	IOL/FOL, D.B.	Note 2
0 Submode 1X	Pin	FOL Note 3	FOL, S.B.	Note 1

Abbreviations:
IOL — Initial Output Latch
FOL — Final Output Latch
FIL — Final Input Latch
S.B. — Single Buffered
D.B. — Double Buffered
DDR — Data Direction Register

Note 1: Data is latched in the output data registers (final output latch) and will be single buffered at the pin if the DDR is 1. The output buffers will be turned off if the DDR is 0.

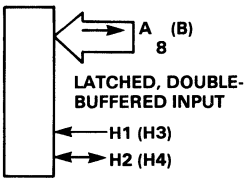
Note 2: Data is latched in the double-buffered output data registers. The data in the final output latch will appear on the port pin if the DDR is a 1.

Note 3: The output drivers that connect the final output latch to the pins are turned on.

VI

PORT A OR B SUBMODE 00 (8-BIT DOUBLE-BUFFERED INPUT) —

MODE 0 SUBMODE 00



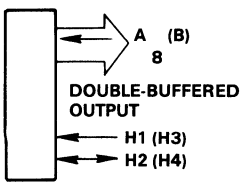
In Mode 0, double-buffered input transfers of up to 8-bits are available by programming Submode 00 in the desired port's control register. The operation of H2 and H4 may be selected by programming the Port A and Port B Control Registers, respectively. All five double-buffered input handshake options, previously mentioned in the Port General Information and Conventions section, are available.

For pins used as outputs, the data path consists of a single latch driving the output buffer. Data written to the port's data register does not affect the operation of any handshake pin, status bit, or any other aspect of the PI/T. Output pins may be used independently of the input transfer. However, read bus cycles to the data register do remove data from the port. Therefore, care should be taken to avoid processor instructions that perform unwanted read cycles.

Refer to PARALLEL PORTS Double-Buffered Input Transfers for a sample timing diagram (Figure 5).

PORT A OR B SUBMODE 01 (8-BIT DOUBLE-BUFFERED OUTPUT) —

MODE 0 SUBMODE 01

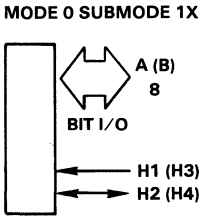


In Mode 0, double-buffered output transfers of up to 8 bits are available by programming submode 01 in the desired port's control register. The operation of H2 and H4 may be selected by programming the Port A and Port B Control Registers, respectively. All five double-buffered output handshake options, previously mentioned in the Port General Information and Conventions section, are available.

For pins used as inputs, data written to the associated data register is double-buffered and passed to the initial or final output latch, as usual, but the output buffer is disabled.

Refer to PARALLEL PORTS Double-Buffered Output Transfers for a sample timing diagram (Figure 6).

PORT A OR B SUBMODE 1X (BIT I/O) —



In Mode 0, simple Bit I/O is available by programming Submode 1X in the desired port's control register. This submode is intended for applications in which several independent devices must be controlled or monitored. Data written to the associated data register is single-buffered. If the data direction register bit for that pin is a 1 (output), the output buffer is enabled. If it is 0 (input), data written is still latched, but is not available at the pin. Data read from the data register is the instantaneous value of the pin or what was written to the data register, depending on the contents of the data direction register. H1(H3) is an edge-sensitive status input pin only and it controls no data-related function. The H1S(H3S) status bit is set following the asserted edge of the input waveform. It is reset by the direct method, the $\overline{\text{RESET}}$ pin being asserted, or when the H12 Enable (H34 Enable) bit is 0.

H2(H4) can be programmed as a simple status input (identical to H1(H3), or as an asserted or negated output. The interlocked or pulsed handshake configurations are not available.

MODE 1 — UNIDIRECTIONAL 16-BIT MODE

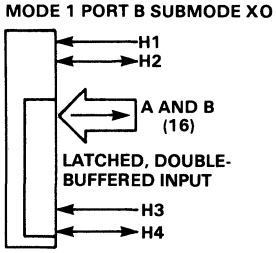
In Mode 1, Ports A and B are concatenated to form a single 16-bit port. The Port B Submode field controls the configuration of both ports. The possible submodes are:

Port B Submode X0 — Double-Buffered Input
Port B Submode X1 — Double-Buffered Output

Handshake pins H3 and H4, configured by programming the Port B Control Register, are associated with the 16-bit double-buffered transfer. These 16-bit transfers are enabled by the H34 Enable bit of the Port General Control Register. Handshake pins H1 and H2 may be used as simple status inputs not related to the 16-bit data transfer or H2 may be an output. Enabling of the H1 and H2 handshake pins is done by the H12 Enable bit of the Port General Control Register. The Port A and B Data Direction Registers operate in each submode. Along with the submode, they affect the data read and written at the data register according to Table 5. They also enable the output buffer associated with each port pin. The $\overline{\text{DMAREQ}}$ pin may be associated only with H3.

Mode 1 can provide convenient, high-speed 16-bit transfers. The Port A and B data registers are addressed for compatibility with the MK68000 Move Peripheral (MOVEP) instruction and with the MK68450 DMAC. To take advantage of this, Port A should contain the most-significant byte of data and always be read or written by the bus master first. The interlocked and pulsed handshake protocols are keyed to accesses to the Port B Data Register in Mode 1. if it is accessed last, the 16-bit double-buffered transfers proceed smoothly.

PORT B SUBMODE X0 (16-BIT DOUBLE-BUFFERED INPUT) —



In Mode 1 Port B Submode X0, double-buffered input transfers of up to 16 bits may be obtained. The level of all 16 pins is asynchronously latched with the asserted edge of H3. The processor may check H3S status bit to determine if new data is present. The $\overline{\text{DMAREQ}}$ pin may be used to signal a DMA controller to empty the input buffers. Regardless of the bus master, Port A data should be read first. (Actually, Port A data need not be read at all.) Port B data should be read last. The operation of the internal handshake controller, the H3S bit, and $\overline{\text{DMAREQ}}$ are keyed to the reading of the Port B data register. (The MK68450 DMAC can be programmed to perform the exact transfers needed for compatibility with the PI/T.) H4 may be programmed for all five of the handshake options mentioned in the Port General Information and Conventions section.

For pins used as outputs, the data path consists of a single latch driving the output buffer. Data written to the port's data register does not affect the operation of any handshake pin, status bit, or any other aspect of the PI/T. Thus, output pins may be used independently of the input transfer. However, read bus cycles to the Port B Data Register do remove data, so care should be taken to avoid unwanted read cycles.

Refer to PARALLEL PORTS Double-Buffered Input Transfers for a sample timing diagram (Figure 5).

In Mode 1 Port B Submode X1, double-buffered output transfers of up to 16 bits may be obtained. Data is written by the bus master (processor or DMA controller) in two bytes.

MODE 1 PORT DATA PATHS

Table 5

Mode	Read Port A/B Register		Write Port A/B Register	
	DDR=0	DDR = 1	DDR=0	DDR=1
1, Port B Submode X0	FIL, D.B.	FOL Note 3	FOL, S.B. Note 2	FOL, S.B. Note 2
1, Port B Submode X1	Pin	FOL Note 3	IOL/FOL, D.B., Note 1	IOL/FOL, D.B., Note 1

Note 1: Data written to Port A goes to a temporary latch. When the Port B data register is later written, Port A data is transferred to IOL/FOL.

Note 2: Data is latched in the output data registers (final output latch) and will be single buffered at the pin if the DDR is 1. The output buffers will be turned off if the DDR is 0.

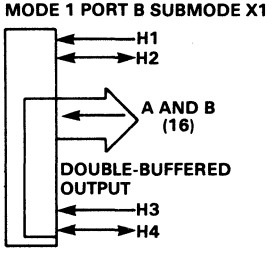
Note 3: The output drivers that connect the final output latch to the pins are turned on.

Abbreviations:

IOL — Initial Output Latch
FOL — Final Output Latch
FIL — Final Input Latch
S.B. — Single Buffered
D.B. — Double Buffered
DDR — Data Direction Register

VI

PORT B SUBMODE X1 (16-BIT DOUBLE-BUFFERED OUTPUT) —

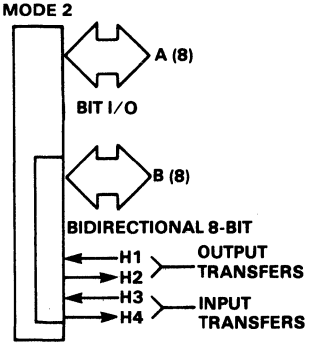


The first byte (most-significant) is written to the Port A Data Register. It is stored in a temporary latch until the next byte is written to the Port B Data Register. Then all 16 bits are transferred to the final output latches of Ports A and B. Both options for interpretation of the H3S status bit, mentioned in Port General Information and Comments section, are available and apply to the 16-bit port as a whole. The $\overline{\text{DMAREQ}}$ pin may be used to signal a DMA controller to transfer another word to the port output latches. (The MK68450 DMAC can be programmed to perform the exact transfers needed for compatibility with the PI/T.) H4 may be programmed for all five of the handshake options mentioned in the Port General Information and Comments section.

For pins used as inputs, data written to either data register is double-buffered and passed to the initial or final output latch, as usual, but the output buffer is disabled.

Refer to PARALLEL PORTS Double-Buffered Input/Output Transfer for a sample timing diagram (Figure 6).

MODE 2 — BIDIRECTIONAL 8-BIT MODE



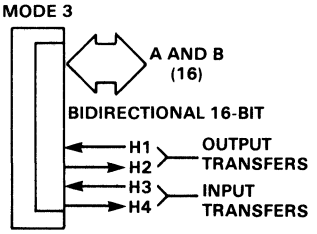
In Mode 2, Port A is used for simple bit I/O with no associated handshake pins. Port B is used for bidirectional 8-bit double-buffered transfers. H1 and H2, enabled by the H12 Enable bit in the Port General Control Register, control

output transfers, while H3 and H4, enabled by the Port General Control Register bit H34 Enable, control input transfers. The instantaneous direction of the data is determined by the H1 handshake pin. The Port B Data Direction Register is not used. The Port A and Port B submode fields do not affect PI/T operation in Mode 2.

DOUBLE-BUFFERED I/O (PORT B) - The only aspect of bidirectional double-buffered transfers that differs from the unidirectional modes lies in controlling the Port B output buffers. They are controlled by the level of H1. When H1 is negated, the Port B output buffers (all 8) are enabled and the pins drive the bidirectional bus. Generally, H1 is negated in response to an asserted H2, which indicates that new output data is present in the double-buffered latches. Following acceptance of the data, the peripheral asserts H1, disabling the Port B output buffers. Other than controlling the output buffer, H1 is edge-sensitive as in other modes. Input transfers proceed identically to the double-buffered input protocol described in the Port General Information and Conventions Section. In Mode 2, only the interlocked and pulsed handshake pin options are available on H2 and H4. The $\overline{\text{DMAREQ}}$ pin may be associated with either input transfers (H3) or output transfers (H1), but not both. Refer to Table 6 for a summary of the Port B Data Register responses in Mode 2.

BIT I/O (PORT A) — Mode 2, Port A performs simple bit I/O with no associated handshake pins. This configuration is intended for applications in which several independent devices must be controlled or monitored. Data written to the Port A data register is single-buffered. If the Port A Data Direction Register bit for that pin is 1 (output), the output buffer is enabled. If it is 0, data written is still latched but not available at the pin. Data read from the data register is either the instantaneous value of the pin or what was written to the data register, depending on the contents of the Port A Data Direction Register. This is summarized in Table 7.

MODE 3 —BIDIRECTIONAL 16-BIT DOUBLE-BUFFERED I/O



In Mode 3, Ports A and B are used for bidirectional 16-bit double-buffered transfers. H1 and H2 control output transfers, while H3 and H4 control input transfers. (H1 and H2 are enabled by the H12 Enable bit while H3 and H4 are enabled by the H34 Enable bit of the Port General Control Register.) The instantaneous direction of the data is determined by the H1 handshake pin, and thus, the data direction registers are not used. The Port A and Port B submode fields do not affect PI/T operation in Mode 3.

The only aspect of bidirectional double-buffered transfers that differs from the unidirectional modes lies in controlling the Port A and B output buffers. They are controlled by the level of H1. When H1 is negated, the output buffers (all 16) are enabled and the pins drive the bidirectional bus. Generally, H1 is negated in response to an asserted H2, which indicates that new output data is present in the the double-buffered latches. Following acceptance of the data, the peripheral asserts H1, disabling the output buffers. Other than controlling the output buffers, H1 is edge-sensitive as in other modes. Input transfers proceed

MODE 2 PORT B DATA PATHS

Table 6

Mode	Read Port B Data Register	Write Port B Data Register
2	FIL, D. B.	IOL/FOL, D. B.
Abbreviations: IOL - Initial Output Latch FOL - Final Output Latch FIL - Final Input Latch	D.B. - Double Buffered	

MODE 2 PORT A DATA PATHS

Table 7

Mode	Read Port A Data Register		Write Port A Data Register	
	DDR=0	DDR= 1	DDR=0	DDR=1
2	PIN	FOL	FOL	FOL, S.B.

Abbreviations:
S.B. — Single Buffered
FOL — Final Output Latch
DDR — Data Direction Register

identically to the double-buffered input protocol described in the Port General Information and Conventions section. Port A and B data is latched with the asserted edge of H3. In Mode 3, only the interlocked and pulsed handshake pin options are available to H2 and H4. The $\overline{\text{DMAREQ}}$ pin may be associated with either input transfers (H3) or output transfers (H1), but not both. H2 indicates when new data is available in the Port B (and implicitly Port A) output latches, but unless the buffer is enabled by H1, the data is not driving the pins.

Mode 3 can provide convenient high-speed 16-bit transfers. The Port A and B Data Registers are addressed for compatibility with the MK68000's Move Peripheral (MOVEP) instruction and with the MK68450 DMAC. To take advantage of this, Port A should contain the most-significant data and always be read or written by the bus master first. The interlocked and pulsed handshake protocols are keyed to accesses to the Port B Data Register in Mode 3. If it is accessed last, the 16-bit double-buffered transfer proceeds smoothly. Refer to Table 8 for a summary of the Port A and B data paths in Mode 3.

DMA REQUEST OPERATION

The Direct Memory Access Request ($\overline{\text{DMAREQ}}$) pulse (when enabled) is associated with output or input transfers to keep the initial and final output latches full or initial and final input latches empty, respectively. Figures 7 and 8 show all the possible paths in generating DMA requests.

$\overline{\text{DMAREQ}}$ is generated on the bus side of the MK68230 by the synchronized* Chip Select. If the conditions of Figures 7 and 8 are met, an access of the bus (assertion of $\overline{\text{CS}}$) will cause $\overline{\text{DMAREQ}}$ to be asserted 3 PI/T clocks (plus the delay time from the clock edge) after $\overline{\text{CS}}$ is synchronized.* $\overline{\text{DMAREQ}}$ remains asserted 3 clock cycles (plus the delay time from the clock edge) and is then negated.

The $\overline{\text{DMAREQ}}$ pulse associated with a peripheral or port side of the PI/T is caused by the synchronized* H1(H3) input. If the conditions of Figures 7 and 8 are met, a port access (assertion of the H1(H3) input) will cause $\overline{\text{DMAREQ}}$ to be asserted 2.5 PI/T clock cycles (plus the delay time from clock edge) after H1(H3) is synchronized.* $\overline{\text{DMAREQ}}$ remains asserted 3 clock cycles (plus the delay time from the clock edge) and is then negated.

MODE 3 PORT A AND B DATA PATHS

Table 8

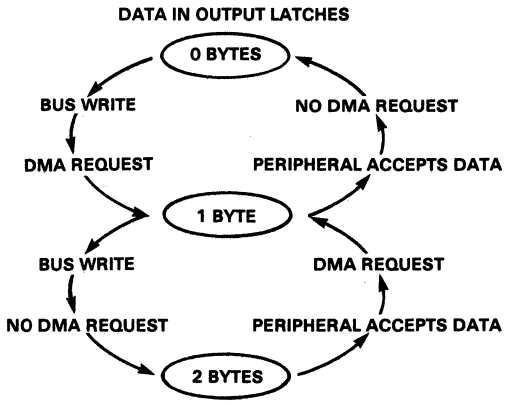
Mode	Read Port A and B Data Register	Write Port A and B Data Register
3	FIL, D.B.	IOL/FOL, D.B., Note 1

Note 1: Data written to Port A goes to a temporary latch. When the Port B data register is later written, Port A data is transferred to IOL/FOL.

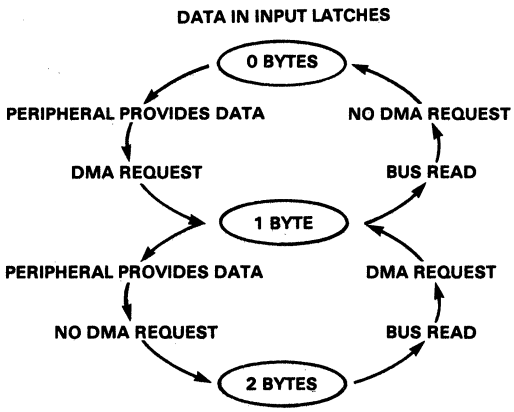
Abbreviations:
IOL — Initial Output Latch
FOL — Final Output Latch
FIL — Final Input Latch
S.B. — Single Buffered
D.B. — Double Buffered

*Synchronized means that the input signal has been seen by the PI/T on the appropriate edge of the clock (rising edge for H1(H3) and falling edge for $\overline{\text{CS}}$). (Refer to the BUS INTERFACE CONNECTION section for the exception concerning $\overline{\text{CS}}$.) If a bus access (assertion of $\overline{\text{CS}}$) and a port access (assertion of H1(H3) occur at the same time, $\overline{\text{CS}}$ will be recognized without any delay. H1(H3) will be recognized one clock cycle later.

$\overline{\text{DMAREQ}}$ ASSOCIATED WITH OUTPUT TRANSFERS
Figure 7



$\overline{\text{DMAREQ}}$ ASSOCIATED WITH INPUT TRANSFERS
Figure 8



TIMER

The MK68230 timer can provide several facilities needed by MK68000 operating systems. It can generate periodic interrupts, a square wave, or a single interrupt after a programmed time period. Also, it can be used for elapsed time measurement or as a device watchdog. This section describes the programmable options available, capabilities, and restrictions that apply to the timer.

The PI/T timer contains a 24-bit synchronous down counter that is loaded from three 8-bit Counter Preload Registers. The 24-bit counter may be clocked by the output of a 5-bit (divide-by-32) prescaler or by an external timer input TIN. If the prescaler is used, it may be clocked by the system clock (CLK pin) or by the TIN external input. The counter signals the occurrence of an event primarily through zero detection. (A zero is when the counter of the 24-bit timer is equal to zero.) This sets the zero detect status (ZDS) bit in the Timer Status Register. It may be checked by the processor or may be used to generate a timer interrupt. The ZDS bit is reset by writing a 1 to the Timer Status Register in that bit position.

The general operation of the timer is flexible and easily programmable. The timer is fully configured and controlled by programming the 8-bit Timer Control Register. It controls: (1) the choice between the Port C operation and the timer operation of three timer pins, (2) whether the counter is loaded from the Counter Preload Register or rolls over when zero detect is reached, (3) the clock input, (4) whether the prescaler is used, and (5) whether the timer is enabled.

RUN/HALT DEFINITION

The overall operation of the timer is described in terms of the run or halt states. The control of the current state is determined by programming the Timer Control Register. When in the halt state, all of the following occur:

1. The prior contents of the counter are not altered and are reliably readable via the Count Registers.
2. The prescaler is forced to $1F whether or not it is used.
3. The ZDS status bit is forced to 0, regardless of the possible zero contents of the 24-bit counter.

The run state is characterized by:

1. The counter is clocked by the source programmed in the Timer Control Register.
2. The counter is not reliably readable.
3. The prescaler is allowed to decrement if programmed for use.
4. The ZDS status bit is set when the 24-bit counter transitions from $000001 to $000000.

TIMER RULES

This section provides a set of rules that allow easy application of the timer.

1. Refer to the Run/Halt Definition above.
2. When the RESET pin is asserted, all bits of the Timer Control Register go to 0, configuring the dual function pins as Port C inputs.

3. The contents of the Counter Preload Registers and counter are not affected by the $\overline{\text{RESET}}$ pin.
4. The Count Registers provide a direct read data path from each portion of the 24-bit counter, but data written to their addresses is ignored. (This results in a normal bus cycle.) These registers are readable at any time, but their contents are never latched. Unreliable data may be read when the timer is in the run state.
5. The Counter Preload Registers are readable and writable at any time and this occurs independently of any timer operation. No protection mechanisms are provided against ill-timed writes.
6. The input frequency to the 24-bit counter from the TIN pin or prescaler output must be between 0 and the input frequency at CLK pin divided by 32, regardless of the configuration chosen.
7. For configurations in which the prescaler is used (with the CLK pin or TIN pin as in input), the contents of the Counter Preload Register (CPR) is transferred to the counter the first time that the prescaler passes from $00 to $1F (rolls over) after entering the run state. Thereafter, the counter decrements or is loaded from the Counter Preload Register when the prescaler rolls over.
8. For configurations in which the prescaler is not used, the contents of the Counter Preload Registers are transferred to the counter on the first asserted edge of the TIN input after entering the run state. On subsequent asserted edges the counter decrements or is loaded from the Counter Preload Registers.
9. The lowest value allowed in the Counter Preload Register for use with the counter is $000001.

TIMER INTERRUPT ACKNOWLEDGE CYCLES

Several conditions may be present when the timer interrupt acknowledge pin ($\overline{\text{TIACK}}$) is asserted. These conditions affect the PI/T's response and the termination of the bus cycle. (See Table 9.)

RESPONSE TO TIMER INTERRUPT ACKNOWLEDGE
Table 9

PC3/TOUT Function	Response to Asserted $\overline{\text{TIACK}}$
PC3 — Port C Pin	No response. No $\overline{\text{DTACK}}$.
TOUT — Square Wave	No response. No $\overline{\text{DTACK}}$.
TOUT — Negated Timer Interrupt Request	No response, No $\overline{\text{DTACK}}$.
TOUT — Asserted Timer Interrupt Request	Timer Interrupt Vector Contents. $\overline{\text{DTACK}}$ Asserted.

PROGRAMMER'S MODEL

The internal accessible register organization is represented in Table 10. Address space within the address map is reserved for future expansion. Throughout the PI/T data sheet the following conventions are maintained:

1. A read from a reserved location in the map results in a read from the "null register." The null register returns all zeros for data and results in a normal bus cycle. A write to one of these locations results in a normal bus cycle but no write occurs.
2. Unused bits of a defined register are denoted by "*" and are read as zeroes.
3. Bits that are unused in the chosen mode/submode but are used in others, are denoted by "X", and are readable and writeable. Their content, however, is ignored in the chosen mode/submode.
4. All registers are addressable as 8-bit quantities. To facilitate operation with the MOVEP instruction and the DMAC, addresses are ordered such that certain sets of registers may also be accessed as words (2 bytes) or long words (4 bytes).

PORT GENERAL CONTROL REGISTER (PGCR) —

7	6	5	4	3	2	1	0
Port Mode Control		H34 Enable	H12 Enable	H4 Sense	H3 Sense	H2 Sense	H1 Sense

The Port General Control Register controls many of the functions that are common to the overall operation of the ports. The PGCR is composed of three major fields: bits 7 and 6 define the operational mode of Ports A and B and affect operation of the handshake pins and status bits; bits 5 and 4 allow a software controlled disabling of particular hardware associated with the handshake pins of each port; and bits 3-0 define the sense of the handshake pins. The PGCR is always readable and writeable.

All bits are reset to 0 when the RESET pin is asserted.

The Port Mode Control field should be altered only when the H12 Enable and H34 Enable bits are 0. Except when Mode 0 is desired, the Port General Control register must be written once to establish the mode, and again to enable the respective operation(s).

PGCR

7	6	Port Mode Control
0	0	Mode 0 (Unidirectional 8-Bit Mode)
0	1	Mode 1 (Unidirectional 16-Bit Mode)
1	0	Mode 2 (Bidirectional 8-Bit Mode)
1	1	Mode 3 (Bidirectional 16-Bit Mode)

PGCR

5	H34 Enable
0	Disabled
1	Enabled

PI/T REGISTER ADDRESSING ASSIGNMENTS

Table 10

Register	Register Select Bits					Accessible	Affected by Reset	Affected by Read Cycle
	5	4	3	2	1			
Port General Control Register (PGCR)	0	0	0	0	0	R W	Yes	No
Port Service Request Register (PSRR)	0	0	0	0	1	R W	Yes	No
Port A Data Direction Register (PADDR)	0	0	0	1	0	R W	Yes	No
Port B Data Direction Register (PBDDR)	0	0	0	1	1	R W	Yes	No
Port C Data Direction Register (PCDDR)	0	0	1	0	0	R W	Yes	No
Port Interrupt Vector Register (PIVR)	0	0	1	0	1	R W	Yes	No
Port A Control Register (PACR)	0	0	1	1	0	R W	Yes	No
Port B Control Register (PBCR)	0	0	1	1	1	R W	Yes	No
Port A Data Register (PADR)	0	1	0	0	0	R W	No	**
Port B Data Register (PBDR)	0	1	0	0	1	R W	No	**
Port A Alternate Register (PAAR)	0	1	0	1	0	R	No	No
Port B Alternate Register (PBAR)	0	1	0	1	1	R	No	No
Port C Data Register (PCDR)	0	1	1	0	0	R W	No	No
Port Status Register (PSR)	0	1	1	0	1	R W*	Yes	No
Timer Control Register (TCR)	1	0	0	0	0	R W	Yes	No
Timer Interrupt Vector Register (TIVR)	1	0	0	0	1	R W	Yes	No
Counter Preload Register High (CPRH)	1	0	0	1	1	R W	No	No
Counter Preload Register Middle (CPRM)	1	0	1	0	0	R W	No	No
Counter Preload Register Low (CPRL)	1	0	1	0	1	R W	No	No
Count Register High (CNTRH)	1	0	1	1	1	R	No	No
Count Register Middle (CNTRM)	1	1	0	0	0	R	No	No
Count Register Low (CNTRL)	1	1	0	0	1	R	No	No
Timer Status Register (TSR)	1	1	0	1	0	R W*	Yes	No

* A write to this register may perform a special status resetting operation.

** Mode dependent.

R = Read

W = Write

PGCR

4	H12 Enable
0	Disabled
1	Enabled

PGCR

3-0	Handshake Pin Sense
0	The associated pin is at the high-voltage level when negated and at the low-voltage level when asserted.
1	The associated pin is at the low-voltage level when negated and at the high-voltage level when asserted.

Port Service Request Register (PSRR)

7	6	5	4	3	2	1	0
*	SVCRQ Select		Interrupt PFS		Port Interrupt Priority Control		

The Port Service Request Register controls other functions that are common to the overall operation to the ports. It is composed of four major fields: bit 7 is unused and is always read as 0; bits 6 and 5 define whether interrupt or DMA requests are generated from activity on the H1 and H3 handshake pins; bits 4 and 3 determine whether two dual function pins operate as Port C or port interrupt request/acknowledge pins; and bits 2, 1, and 0 control the priority among all port interrupt sources. Since bits 2, 1, and 0 affect interrupt operation, it is recommended that they be changed only when the affected interrupt(s) is (are) disabled or known to remain inactive. The PSRR is always readable and writable.

All bits are reset to 0 when the $\overline{\text{RESET}}$ pin is asserted.

PSRR

6	5	SVCRQ Select
0	X	The PC4/$\overline{\text{DMAREQ}}$ pin carries the PC4 function; DMA is not used.
1	0	The PC4/$\overline{\text{DMAREQ}}$ pin carries the $\overline{\text{DMAREQ}}$ function and is associated with double-buffered transfers controlled by H1. H1 is removed from the PI/T's interrupt structure, and thus, does not cause interrupt requests to be generated. To obtain $\overline{\text{DMAREQ}}$ pulses, Port A Control Register bit 1 (H1 SVCRQ Enable) must be a 1.
1	1	The PC4/$\overline{\text{DMAREQ}}$ pin carries the $\overline{\text{DMAREQ}}$ function and is associated with double-buffered transfers controlled by H3. H3 is removed from the PI/T's interrupt structure, and thus, does not cause interrupt requests to be generated. To obtain $\overline{\text{DMAREQ}}$ pulses, Port B Control Register bit 1 (H3 SVCRQ Enable) must be 1.

PSRR

4	3	Interrupt Pin Function Select
0	0	The PC5/$\overline{\text{PIRQ}}$ pin carries the PC5 function. The PC6/$\overline{\text{PIACK}}$ pin carries the PC6 function.
0	1	The PC5/$\overline{\text{PIRQ}}$ pin carries the $\overline{\text{PIRQ}}$ function. The PC6/$\overline{\text{PIACK}}$ pin carries the PC6 function.
1	0	The PC5/$\overline{\text{PIRQ}}$ pin carries the PC5 function. The PC6/$\overline{\text{PIACK}}$ pin carries the $\overline{\text{PIACK}}$ function.
1	1	The PC5/$\overline{\text{PIRQ}}$ pin carries the $\overline{\text{PIRQ}}$ function. The PC6/$\overline{\text{PIACK}}$ pin carries the $\overline{\text{PIACK}}$ function.

Bits 2, 1, and 0 determine port interrupt priority. The priority is shown in descending order left to right.

PSRR Port Interrupt Priority Control

2 1 0	Highest ..... Lowest			
0 0 0	H1S	H2S	H3S	H4S
0 0 1	H2S	H1S	H3S	H4S
0 1 0	H1S	H2S	H4S	H3S
0 1 1	H2S	H1S	H4S	H3S
1 0 0	H3S	H4S	H1S	H2S
1 0 1	H3S	H4S	H2S	H1S
1 1 0	H4S	H3S	H1S	H2S
1 1 1	H4S	H3S	H2S	H1S

PORT A DATA DIRECTION REGISTER (PADDR)—The Port A Data Direction Register determines the direction and buffering characteristics of each of the Port A pins. One bit in the PADDR is assigned to each pin. A 0 indicates that the pin is used as an input, while a 1 indicates it is used as an output. The PADDR is always readable and writeable. This register is ignored in Mode 3.

All bits are reset to the 0 (input) state when the $\overline{\text{RESET}}$ pin is asserted.

PORT B DATA DIRECTION REGISTER (PBDDR)—The PBDDR is identical to the PADDR for the Port B pins and the Port B Data Register, except that this register is ignored in Modes 2 and 3.

PORT C DATA DIRECTION REGISTER (PCDDR)—The Port C Data Direction Register specifies whether each dual-function pin that is chosen for Port C operation is an input (0) or an output (1) pin. The PCDDR, along with bits that determine the respective pin's function, also specify the exact hardware to be accessed at the Port C Data Register address. (See the Port C Data Register description for more details.) The PCDDR is an 8-bit register that is readable and writeable at all times. Its operation is independent of the chosen PI/T mode.

These bits are cleared to 0 when the $\overline{\text{RESET}}$ pin is asserted.

PORT INTERRUPT VECTOR REGISTER (PIVR)—

7	6	5	4	3	2	1	0
Interrupt Vector Number						*	*

The Port Interrupt Vector Register contains the upper order six bits of the four port interrupt vectors. The contents of this register may be read two ways: by an ordinary read cycle, or

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by a port interrupt acknowledge bus cycle. The exact data read depends on how the cycle was initiated and other factors. Behavior during a port interrupt acknowledge cycle is summarized above in Table 3.

From a normal read cycle (CS), there is never a consequence to reading this register. Following negation of the $\overline{\text{RESET}}$ pin, but prior to writing to the PIVR, a $0F will be read. After writing to the register, the upper 6 bits may be read and the lower 2 bits are forced to 0. No prioritization computation is performed.

PORT A CONTROL REGISTER (PACR) —

7	6	5	4	3	2	1	0
Port A Submode		H2 Control			H2 Int. Enable	H1 SVCRQ Enable	H1 Stat. Ctrl.

The Port A Control Register, in conjunction with the programmed mode and the Port B submode, control the operation of Port A and the handshake pins H1 and H2. The Port A Control Register contains five fields: bits 7 and 6 specify the Port A submode; bits 5, 4, and 3 control the operation of the H2 handshake pin and H2S status bit; bit 2 determines whether an interrupt will be generated when the H2S status bit goes to 1; bit 1 determines whether a service request (interrupt request or DMA request) will occur; bit 0 controls the operation of the H1S status bit. The PACR is always readable and writeable.

All bits are cleared to 0 when the $\overline{\text{RESET}}$ pin is asserted.

When the Port A submode field is relevant in a mode/submode definition, it must not be altered unless the H12 Enable bit in the Port General Control Register is 0. (See Table 2.)

The operation of H1 and H2 and their related status bits is given below, for each of the modes specified by Port General Control Register bits 7 and 6. This description is organized such that for each mode/submode all programmable options of each pin and status bit are given.

Bits 2 and 1 carry the same meaning in each mode/submode, and thus are specified only once.

PACR

2	H2 Interrupt Enable
0	The H2 interrupt is disabled.
1	The H2 interrupt is enabled.

PACR

1	H1 SVCRQ Enable
0	The H1 interrupt and DMA request are disabled.
1	The H1 interrupt and DMA request are enabled.

PACR MODE 0 PORT A SUBMODE 00

PACR

5 4 3	H2 Control
0 X X	Input pin — status only.
1 0 0	Output pin — always negated.
1 0 1	Output pin — always asserted.
1 1 0	Output pin — interlocked input handshake protocol.
1 1 1	Output pin — pulsed input handshake protocol.

PACR

0	H1 Status Control
X	Not Used

PACR MODE 0 PORT A SUBMODE 01

PACR

5 4 3	H2 Control
0 X X	Input pin — status only.
1 0 0	Output pin — always negated.
1 0 1	Output pin — always asserted.
1 1 0	Output pin — interlocked output handshake protocol.
1 1 1	Output pin — pulsed output handshake protocol.

PACR

0	H1 Status Control
0	The H1S status bit is 1 when either the Port A initial or final output latch can accept new data. It is 0 when both latches are full and cannot accept new data.
1	The H1S status bit is 1 when both of the Port A output latches are empty. It is 0 when at least one latch is full.

PACR MODE 0 PORT A SUBMODE 1X

PCR

5 4 3	H2 Control
0 X X	Input pin — status only.
1 X 0	Output pin — always negated.
1 X 1	Output pin — always asserted.

PACR

0	H1 Status Control
X	Not used.

PACR MODE 1 PORT A SUBMODE XX PORT B SUBMODE X0

PACR

5 4 3	H2 Control
0 X X	Input pin — status only.
1 X 0	Output pin — always negated.
1 X 1	Output pin — always asserted.

PACR

0	H1 Status Control
X	Not used.

PACR MODE 1 PORT A SUBMODE XX PORT B SUBMODE X1

PACR

5	4	3	H2 Control
0	X	X	Input pin — status only.
1	X	0	Output pin — always negated.
1	X	1	Output pin — always asserted.

PACR

0	H1 Status Control
X	Not used.

PACR MODE 2

PACR

5	4	3	H2 Control
X	X	0	Output pin — interlocked output handshake protocol.
X	X	1	Output pin — pulsed output handshake protocol.

PACR

0	H1 Status Control
0	The H1S status bit is 1 when either the Port B initial or final output latch can accept new data. It is 0 when both latches are full and cannot accept new data.
1	The H1S status bit is 1 when both of the Port B output latches are empty. It is 0 when at least one latch is full.

PACR MODE 3

PACR

5	4	3	H2 Control
X	X	0	Output pin — interlocked output handshake protocol.
X	X	1	Output pin — pulsed output handshake protocol.

PACR

0	H1 Status Control
0	The H1S status bit is 1 when either the initial or final output latch of Port A and B can accept new data. It is 0 when both latches are full and cannot accept new data.
1	The H1S status bit is 1 when both the initial and final output latches of Ports A and B are empty. It is 0 when either the initial or final latch of Ports A and B is full.

PORT B CONTROL REGISTER (PBCR) —

7	6	5	4	3	2	1	0
Port B Submode		H4 Control			H4 Int. Enable	H3 SVCRQ Enable	H3 Stat. Ctrl.

The Port B Control Register specifies the operation of Port B and the handshake pins H3 and H4. The Port B control register contains five fields: bits 7 and 6 specify the Port B submode; bits 5, 4, and 3 control the operation of the H4 handshake pin and H4S status bit; bit 2 determines whether an interrupt will be generated when the H4S status bit goes to 1; bit 1 determines whether a service request (interrupt request or DMA request) will occur; bit 0 controls the operation of the H3S status bit. The PACR is always readable and writeable. There is never a consequence to reading the register.

All bits are cleared to 0 when the $\overline{\text{RESET}}$ pin is asserted.

When the Port B submode field is relevant in a mode/submode definition, it must not be altered unless the H34 Enable bit in the Port General Control Register is 0. (See Table 2.)

The operation of H3 and H4 and their related status bits is given below, for each of the modes specified by Port General Control Register bits 7 and 6. This description is organized such that for each mode/submode all programmable options of each pin and status bit are given.

Bits 2 and 1 carry the same meaning in each mode/submode, and thus are specified only once.

PBCR

2	H4 Interrupt Enable
0	The H4 interrupt is disabled.
1	The H4 interrupt is enabled.

PBCR

1	H3 SVCRQ Enable
0	The H3 interrupt and DMA request are disabled.
1	The H3 interrupt and DMA request are enabled.

PBCR MODE 0 PORT B SUBMODE 00

PBCR

5	4	3	H4 Control
0	X	X	Input pin — status only.
1	0	0	Output pin — always negated.
1	0	1	Output pin — always asserted.
1	1	0	Output pin — interlocked input handshake protocol.
1	1	1	Output pin — pulsed input handshake protocol.

PBCR

0	H3 Status Control
X	Not used.

PBCR MODE 0 PORT B SUBMODE 01

PBCR

5	4	3	H4 Control
0	X	X	Input pin — status only.
1	0	0	Output pin — always negated.
1	0	1	Output pin — always asserted.
1	1	0	Output pin — interlocked output handshake protocol.
1	1	1	Output pin — pulsed output handshake protocol.

PBCR

0	H3 Status Control
0	The H3S status bit is 1 when either the Port B initial or final output latch can accept new data. It is 0 when both latches are full and cannot accept new data.
1	The H3S status bit is 1 when both of the Port B output latches are empty. It is 0 when at least one latch is full.

PBCR MODE 0 PORT B SUBMODE 1X

PBCR

5 4 3	H4 Control
0 X X	Input pin — status only.
1 X 0	Output pin — always negated.
1 X 1	Output pin — always asserted.

PBCR

0	H3 Status Control
X	Not used.

PBCR MODE 1 PORT B SUBMODE X0

PBCR

5 4 3	H4 Control
0 X X	Input pin — status only.
1 0 0	Output pin — always negated.
1 0 1	Output pin — always asserted.
1 1 0	Output pin — interlocked input handshake protocol.
1 1 1	Output pin — pulsed input handshake protocol.

PBCR

0	H3 Status Control
X	Not used.

PBCR MODE 1 PORT B SUBMODE X1

PBCR

5 4 3	H4 Control
0 X X	Input pin — status only.
1 0 0	Output pin — always negated.
1 0 1	Output pin — always asserted.
1 1 0	Output pin — interlocked input handshake protocol.
1 1 1	Output pin — pulsed input handshake protocol.

PBCR

0	H3 Status Control
0	The H3S status bit is 1 when either the initial or final output latch of Port A and B can accept new data. It is 0 when both latches are full and cannot accept new data.
1	The H3S status bit is 1 when both the initial and final output latches of Ports A and B are empty. It is 0 when neither the initial nor final latch of Ports A and B is full.

PBCR MODE 2

PBCR

5 4 3	H4 Control
X X 0	Output pin — interlocked input handshake protocol.
X X 1	Output pin — pulsed input handshake protocol.

PBCR

0	H3 Status Control
X	Not used.

PBCR MODE 3

PBCR

5 4 3	H4 Control
X X 0	Output pin — interlocked input handshake protocol.
X X 1	Output pin — pulsed input handshake protocol.

PBCR

0	H3 Status Control
X	Not used.

Port A Data Register (PADR) — The Port A Data Register is an address for moving data to and from the Port A pins. The Port A Data Direction Register determines whether each pin is an input (0) or an output (1), and is used in configuring the actual data paths. This is mode dependent and is described with the modes above.

This register is readable and writeable at all times. Depending on the chosen mode/submode, reading or writing may affect the double-buffered handshake mechanism. The Port A Data Register is not affected by the assertion of the $\overline{\text{RESET}}$ pin.

Port B Data Register (PBDR) — The Port B Data Register is an address for moving data to and from the Port B pins. The Port B Data Direction Register determines whether each pin is an input (0) or an output (1), and is used in configuring the actual data paths. This is mode dependent and is described with the modes, above.

This register is readable and writeable at all times. Depending on the chosen mode/submode, reading or writing may affect the double-buffered handshake mechanism. The Port B Data Register is not affected by the assertion of the $\overline{\text{RESET}}$ pin.

Port A Alternate Register (PAAR) — The Port A Alternate Register is an alternate address for reading the Port A pins. It is a read-only address and no other PI/T condition is affected. In all modes the instantaneous pin level is read and no input latching is performed except at the data bus interface (see Bus Interface Connection). Writes to this address are answered with $\overline{\text{DTACK}}$, but the data is ignored.

Port B Alternate Register (PBAR) — The Port B Alternate Register is an alternate address for reading the Port B pins. It is a read-only address and no other PI/T condition is affected. In all modes the instantaneous pin level is read and no input latching is performed except at the data bus interface (see Bus Interface Connection). Writes to this address are answered with $\overline{DTACK}$, but the data is ignored.

Port C Data Register (PCDR) — The Port C Data Register is an address for moving data to and from each of the eight Port C/alternate-function pins. The exact hardware accessed is determined by the type of bus cycle (read or write) and individual conditions affecting each pin. These conditions are (1) whether the pin is used for the Port C or alternate function, and (2) whether the Port C Data Direction Register indicates the input or output direction. The Port C Data Register is single buffered for output pins and not buffered for input pins. These conditions are summarized in Table 11.

The Port C Data Register is not affected by the assertion of the $\overline{RESET}$ pin.

The operation of the PCDR is independent of the chosen PI/T mode.

PCDR HARDWARE ACCESSES

Table 11

Read Port C Data Register			
Port C Function PCDDR = 0	**Port C Function PCDDR = 1**	**Alternate function PCDDR = 0**	**Alternate function PCDDR = 1**
pin	Port C output register	pin	Port C output register
Write Port C Data Register			
Port C Function PCDDR = 0	**Port C Function PCDDR = 1**	**Alternate function PCDDR = 0**	**Alternate function PCDDR = 1**
Port C output register, buffer disabled	Port C output register, buffer enabled	Port C output register	Port C output register

Note that two additional useful benefits result from this structure. First, it is possible to directly read the state of a dual-function pin while used for the non-Port C function. Second, it is possible to generate program controlled transitions on alternate-function pins by switching back to the Port C function, and writing to the PCDR.

This register is readable and writable at all times.

The Port Status Register contains information about handshake pin activity. Bits 7-4 show the instantaneous level of the respective handshake pin, and is independent of the handshake pin sense bits in the Port General Control Register. Bits 3-0 are the respective status bits referred to throughout this data sheet. Their interpretation depends on the programmed mode/submode of the PI/T. For Bits 3-0 a 1 is the active or asserted state.

Port Status Register (PSR)

7	6	5	4	3	2	1	0
H4 Level	H3 Level	H2 Level	H1 Level	H4S	H3S	H2S	H1S

The Timer Control Register (TCR) determines all operations of the timer. Bits 7-5 configure the PC3/TOUT and PC7/$\overline{TIACK}$ pins for Port C, square wave, vectored interrupt, or autovectored interrupt operation; bit 4 specifies whether the counter receives data from the Counter Preload Register or continues counting when zero detect is reached; bit 3 is unused and is read as 0; bits 2 and 1 configure the path from the CLK and TIN pins to the counter controller; bit 0 enables the timer. This register is readable and writeable at all times.

All bits are cleared to 0 when the $\overline{RESET}$ pin is asserted.

Timer Control Register (TCR)

7	6	5	4	3	2	1	0
TOUT/$\overline{TIACK}$ Control			Z.D. Ctrl.	*	Clock Control		Timer Enable

TCR 7 6 5 — TOUT/$\overline{TIACK}$ Control

- 0 0 X The dual-function pins PC3/TOUT and PC7/$\overline{TIACK}$ carry the Port C function.
- 0 1 X The dual-function pin PC3/TOUT carries the TOUT function. In the run state it is used as a square wave output and is toggled on zero detect. The TOUT pin is high while in the halt state. The dual-function pin PC7/$\overline{TIACK}$ carries the PC7 function.
- 1 0 0 The dual-function pin PC3/TOUT carries the TOUT function. In the run or halt state it is used as a timer interrupt request output. The timer interrupt is disabled; thus, the pin is always three-stated. The dual-function pin PC7/$\overline{TIACK}$ carries the $\overline{TIACK}$ function; however, since interrupt request is negated, the PI/T produces no response, i.e., no data or $\overline{DTACK}$, to an asserted $\overline{TIACK}$. Refer to Timer Interrupt Cycle section for details. This combination and the 101 state below support vectored timer interrupts.
- 1 0 1 The dual-function pin PC3/TOUT carries the TOUT function and is used as a timer interrupt request output. The timer interrupt is enabled; thus, the pin is low when the timer ZDS status bit is 1. The dual function pin PC7/$\overline{TIACK}$ carries the $\overline{TIACK}$ function and is used as a timer interrupt acknowledge input. Refer to the Timer Interrupt Acknowledge Cycle section for details. This combination and the 100 state above support vectored timer interrupts.

1 1 0 The dual-function pin PC3/TOUT carries the TOUT function. In the run or halt state it is used as a timer interrupt request output. The timer interrupt is disabled; thus, the pin is always three-stated. The dual-function pin PC7/$\overline{\text{TIACK}}$ carries the PC7 function.

1 1 1 The dual-function pin PC3/TOUT carries the TOUT function and is used as a timer interrupt request output. The timer interrupt is enabled; thus, the pin is low when the timer ZDS status bit is 1. The dual-function pin PC7/$\overline{\text{TIACK}}$ carries the PC7 function and autovectored interrupts are supported.

TCR

4	**Zero Detect Control**
0	The counter is loaded from the Counter Preload Register on the first clock to the 24-bit counter after zero detect, and resumes counting.
1	The counter rolls over on zero detect, then continues counting.

Bit 3 is unused and is always read as 0.

TCR

2 1	**Clock Control**
0 0	The PC2/TIN input pin carries the Port C function and the CLK pin and prescaler are used. The prescaler is decremented on the falling transition of the CLK pin; the 24-bit counter is decremented or loaded from the Counter Preload Registers when the prescaler rolls over from $00 to $1F. The Timer Enable bit determines whether the timer is in the run or halt state.
0 1	The PC2/TIN pin serves as a timer input and the CLK pin and prescaler are used. The prescaler is decremented on the the falling transition of the CLK pin; the 24-bit counter is decremented or loaded from the Counter Preload Registers when the prescaler rolls over from $00 to $1F. The timer is in the run state when the Timer Enable bit is 1 and the TIN pin is high; otherwise the timer is in the halt state.
1 0	The PC2/TIN pin serves as a timer input and the prescaler is used. The prescaler is decremented following the rising transition of the TIN pin after syncing with the internal clock. The 24-bit counter is decremented or loaded from the counter preload registers when the prescaler rolls over from $00 to $1F. The Timer Enable bit determines whether the timer is in the run or halt state.
1 1	The PC2/TIN pin serves as a timer input and the prescaler is unused. The 24-bit counter is decremented or loaded from the Counter Preload Registers following the rising edge of the TIN pin after syncing with the internal clock. The Timer Enable bit determines whether the timer is in the run or halt state.

TCR

0	**Timer Enable**
0	Disabled.
1	Enabled.

Timer Interrupt Vector Register (TIVR) — The timer interrupt vector register contains the 8-bit vector supplied when the timer interrupt acknowledge pin $\overline{\text{TIACK}}$ is asserted. The register is readable and writeable at all times, and the same value is always obtained from a normal read cycle and a timer interrupt acknowledge bus cycle ($\overline{\text{TIACK}}$). When the $\overline{\text{RESET}}$ pin is asserted the value of $0F is automatically loaded into the register. Refer to Timer Interrupt Acknowledge Cycle section for more details.

Counter Preload Register H, M, L (CPRH-L)

7	6	5	4	3	2	1	0	
Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16	CPRH
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	CPRM
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	CPRL

The Counter Preload Registers are a group of three 8-bit registers used for storing data to be transferred to the counter. Each of the registers is individually addressable, or the group may be accessed with the MOVEP .L or the MOVEP.W instructions. The address one less than the address of CPRH is the null register, and is reserved so that zeros are read in the upper 8 bits of the destination data register when a MOVEP.L is used. Data written to this address is ignored.

The registers are readable and writeable at all times. A read cycle proceeds independently of any transfer to the counter, which may be occurring simultaneously.

To insure proper operation of the PI/T Timer, a value of $000000 may not be stored in the Counter Preload Registers for use with the counter.

The $\overline{\text{RESET}}$ pin does not affect the contents of these registers.

Count Register H, M, L (CNTRH-L) —

7	6	5	4	3	2	1	0	
Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16	CNTRH
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	CNTRM
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	CNTRL

The count registers are a group of three 8-bit addresses at which the counter can be read. The contents of the counter are not latched during a read bus cycle; thus, the data read at these addresses is not guaranteed if the timer is in the

run state. (Bits 2, 1, and 0 of the Timer Control Register specify the state.) Write operations to these addresses result in a normal bus cycle but the data is ignored.

Each of the registers is individually addressable, or the group may be accessed with the MOVEP.L or the MOVEP.W instructions. The address one less than the address of CNTRH is the null register, and is reserved so that zeros are read in the upper 8 bits of the destination data register when a MOVEP.L is used. Data written to this address is ignored.

Timer Status Register (TSR)

7	6	5	4	3	2	1	0
*	*	*	*	*	*	*	ZDS

The Timer Status Register contains one bit from which the zero detect status can be determined. The ZDS status bit (bit 0) is an edge-sensitive flip-flop that is set to 1 when the 24-bit counter decrements from $000001 to $000000. The ZDS status bit is cleared to 0 following the direct clear operation (similar to that of the ports), or when the timer is halted. Note also that when the RESET pin is asserted the timer is disabled, and thus enters the halt state.

This register is always readable without consequence. A write access performs a direct clear operation if bit 0 in the written data is 1. Following that, the ZDS bit is 0.

This register is constructed with a reset dominant S-R flip-flop so that all clearing conditions prevail over the possible zero detect condition.

Bits 7-1 are unused and are read as 0.

TIMER APPLICATIONS SUMMARY

This section outlines programming of the Timer Control Register for several typical examples.

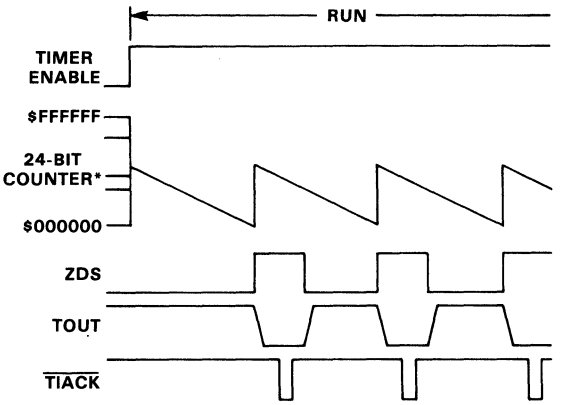
Periodic Interrupt Generator

7	6	5	4	3	2	1	0
TOUT/$\overline{\text{TIACK}}$ Control			Z.D. Ctrl.	*	Clock Control		Timer Enable
1	X	1	0	0	00 or 1X		changed

In this configuration the timer generates a periodic interrupt. The TOUT pin is connected to the system's interrupt request circuitry and the $\overline{\text{TIACK}}$ pin may be used as an interrupt acknowledge input to the timer. The TIN pin may be used as a clock input.

The processor loads the Counter Preload Registers and Timer Control Register, and then enables the timer. When the 24-bit counter passes from $000001 to $000000 the ZDS status bit is set and the TOUT (interrupt request) pin is asserted. At the next clock to the 24-bit counter it is again loaded with the contents of the CPR's, and thereafter decrements. In normal operation, the processor must direct clear the status bit to negate the interrupt request (see Figure 9).

PERIODIC INTERRUPT GENERATOR
Figure 9



*Analog representation of counter value

Square Wave Generator

7	6	5	4	3	2	1	0
TOUT/$\overline{\text{TIACK}}$ Control			Z. D. Ctrl.	*	Clock Control		Timer Enable
0	1	X	0	0	00 or 1X		changed

In this configuration the timer produces a square wave at the TOUT pin. The TOUT pin is connected to the user's circuitry and the $\overline{\text{TIACK}}$ pin is not used. The TIN pin may be used as a clock input.

The processor loads the Counter Preload Registers and Timer Control Register, and then enables the timer. When the 24-bit counter passes from $000001 to $000000 the ZDS status bit is set and the TOUT (square wave output) pin is toggled. At the next clock to the 24-bit counter it is again loaded with the contents of the CPRs, and thereafter decrements. In this application there is no need for the processor to direct clear the ZDS status bit; however, it is possible for the processor to sync itself with the square wave by clearing the ZDS status bit, then polling it. The processor may also read the TOUT level at the Port C address.

Note that the PC3/TOUT pin functions as PC3 following the negation of $\overline{\text{RESET}}$. If used in the square wave configuration a pullup resistor may be required to keep a known level prior

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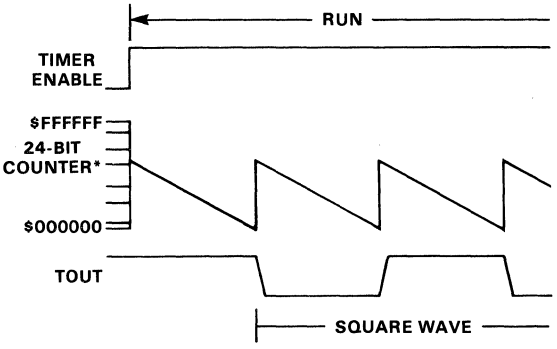
to programming. Prior to enabling the timer, TOUT is high (see Figure 10).

SQUARE WAVE GENERATOR

Figure 10



*Analog representation of counter value.

Interrupt After Timeout

7	6	5	4	3	2	1	0
TOUT/$\overline{\text{TIACK}}$ Control			Z.D. Ctrl.	*	Clock Control		Timer Enable
1	X	1	1	0	00 or 1X		changed

In this configuration the timer generates an interrupt after a programmed time period has expired. The TOUT pin is connected to the system's interrupt request circuitry and the $\overline{\text{TIACK}}$ pin may be an interrupt acknowledge input to the timer. The TIN pin may be used as a clock input.

This configuration is similar to the periodic interrupt generator except that the Zero Detect Control bit is set. This forces the counter roll over after Zero Detect is reached, rather than reloading from the CPRs. When the processor takes the interrupt it can halt the timer and read the counter. This allows the processor to measure the delay time from Zero Detect (interrupt request) to entering the service routine. Accurate knowledge of the interrupt latency may be useful in some applications (see Figure 11).

ELAPSED TIME MEASUREMENT

Elapsed time measurement takes several forms; two are described below.

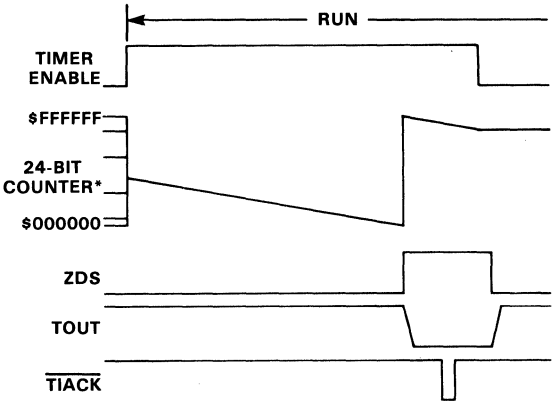
System Clock

7	6	5	4	3	2	1	0
TOUT/$\overline{\text{TIACK}}$ Control			Z. D. Ctrl.	*	Clock Control		Timer Enable
0	0	X	1	0	0	0	changed

This configuration allows time interval measurement by software. No timer pins are used.

SINGLE INTERRUPT AFTER TIMEOUT

Figure 11



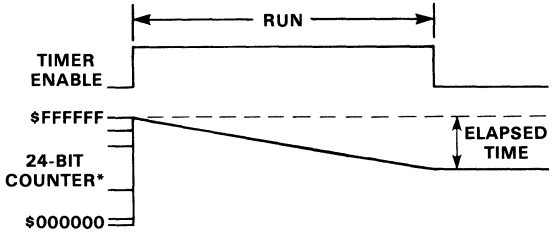
*Analog representation of counter value.

The processor loads the Counter Preload Registers (generally with all 1s) and Timer Control Register, and then enables the timer. The counter decrements until the ending event takes place. When it is desired to read the time interval, the processor must halt the timer, then read the counter.

For applications in which the interval could have exceeded that programmable in this timer, interrupts can be counted to provide the equivalent of additional timer bits. At the end, the timer can be halted and read (see Figure 12).

ELAPSED TIME MEASUREMENT

Figure 12



*Analog representation of counter value.

External Clock

7	6	5	4	3	2	1	0
TOUT/$\overline{\text{TIACK}}$ Control			Z. D. Ctrl.	*	Clock Control		Timer Enable
0	0	X	1	0	1	X	changed

This configuration allows measurement (counting) of the number of input pulses occurring in an interval in which the counter is enabled. The TIN input pin provides the input pulses. Generally the TOUT and $\overline{\text{TIACK}}$ pins are not used.

This configuration is identical to the Elasped Time Measurement/System Clock configuration except that the TIN pin is used to provide the input frequency. It can be connected to a simple oscillator, and the same methods could be used. Alternately, it could be gated off and on externally and the number of cycles occurring while in the run state can be counted. However, minimum pulse width high and low specifications must be met.

Device Watchdog

7	6	5	4	3	2	1	0
TOUT/$\overline{\text{TIACK}}$ Control			Z. D. Ctrl.	*	Clock Control		Timer Enable
1	X	1	1	0	0	1	changed

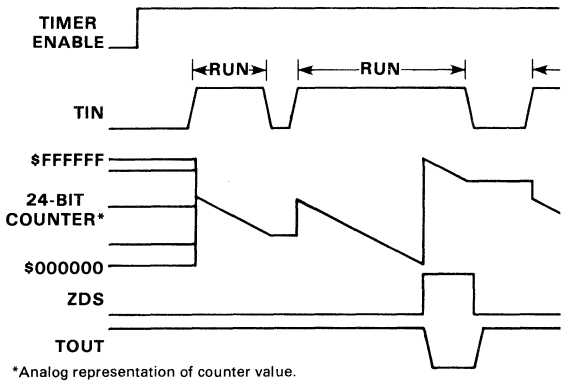
This configuration provides the watchdog function needed in many systems. The TIN pin is the timer input whose period at the high (1) level is to be checked. Once allowed by the processor, the TIN input pin controls the run/halt mode. The TOUT pin is connected to external circuitry requiring notification when the TIN pin has been asserted longer than the programmed time. The $\overline{\text{TIACK}}$ pin (interrupt acknowledge) is only needed if the TOUT pin is connected to interrupt circuitry.

The processor loads the Counter Preload Register and Timer Control Register, and then enables the timer. When the TIN input is asserted (1, high) the timer transfers the contents of the Counter Preload Register to the counter and begins counting. If the TIN input is negated before Zero Detect is reached, the TOUT output and the ZDS status bit remain negated. If Zero Detect is reached while the TIN input is still asserted the ZDS status bit is set and the TOUT output is asserted. (The counter rolls over and keeps on counting.)

In either case, when the TIN input is negated the ZDS status bit is 0, the TOUT output is negated, the counting stops, and the prescaler is forced to all 1s (see Figure 13).

DEVICE WATCHDOG

Figure 13



*Analog representation of counter value.

BUS INTERFACE CONNECTION

The PI/T has an asynchronous bus interface, primarily designed for use with the MK68000 microprocessor. With care, however, it can be connected to synchronous microprocessor buses. This section completely describes the PI/T's bus interface, and is intended for the asynchronous bus designer unless otherwise mentioned.

In an asynchronous system the PI/T CLK may operate at a significantly different frequency, either higher or lower, than the bus master and other system components, as long as all bus specifications are met. The MK68230 CLK pin has the same specifications as the MK68000 CLK, and must not be gated off at any time.

The following signals generate normal read and write cycles to the PI/T: $\overline{\text{CS}}$ (Chip Select), R/$\overline{\text{W}}$ (Read/Write), RS1-RS5 (five Register Select bits), D0-D7 (the 8-bit bidirectional data bus), and $\overline{\text{DTACK}}$ (Data Transfer Acknowledge). To generate interrupt acknowledge cycles PC6/$\overline{\text{PIACK}}$ or PC7/$\overline{\text{TIACK}}$ is used instead of $\overline{\text{CS}}$, and the Register Select pins are ignored. No combination of the following pins may be asserted simultaneously: $\overline{\text{CS}}$, $\overline{\text{PIACK}}$, or $\overline{\text{TIACK}}$.

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READ CYCLES VIA CHIP SELECT

This catagory includes all register reads, except port or timer interrupt acknowledge cycles. When $\overline{\text{CS}}$ is asserted, the Register Select and R/$\overline{\text{W}}$ inputs are latched internally. They must meet small setup and hold time requirements with respect to the asserted edge of $\overline{\text{CS}}$. (See the AC ELECTRICAL CHARACTERISTICS table.) The PI/T is not protected against aborted (shortened) bus cycles generated by an Address Error or Bus Error exception in which it is addressed.

Certain operations triggered by normal read (or write) bus cycles are not complete within the time allotted to the bus cycle. One example is transfers to/from the double-buffered latches that occur as a result of the bus cycle. If the bus master's CLK is significantly faster than the PI/T's the possibility exists that, following the bus cycle, $\overline{\text{CS}}$ can be negated then re-asserted before completion of these internal operations. In this situation the PI/T does not recognize the re-assertion of CS until these operations are complete. Only at that time does it begin the internal sequencing necessary to react to the asserted $\overline{\text{CS}}$. Since $\overline{\text{CS}}$ also controls the $\overline{\text{DTACK}}$ response, this "bus cycle recovery time" can be related to the CLK edge on which $\overline{\text{DTACK}}$ is asserted for that cycle. The PI/T will recognize the subsequent assertion of CS three (3) CLK periods after the CLK edge on which $\overline{\text{DTACK}}$ was previously asserted.

The Register Select and R/$\overline{\text{W}}$ inputs pass through an internal latch that is transparent when the PI/T can recognize a new $\overline{\text{CS}}$ pulse (see above paragraph). Since the internal data bus of the PI/T is continuously enabled for read transfers, the read access time (to the data bus buffers)

begins when the Register Selects are stabilized internally. Also, when the PI/T is ready to begin a new bus cycle, the assertion of $\overline{CS}$ enables the data bus buffers within a short propagation delay. This does not contribute to the overall read access time unless $\overline{CS}$ is asserted significantly after the Register Select and R/$\overline{W}$ inputs are stabilized (as may occur with synchronous bus microprocessors).

In addition to Chip Select's previously mentioned duties, it controls the assertion of $\overline{DTACK}$ and latching of read data at the data bus interface. Except for controlling input latches and enabling the data bus buffers, all of these functions occur only after $\overline{CS}$ has been recognized internally and synchronized with the internal clock. Chip Select is recognized on the falling edge of the CLK if the setup time has been met, and $\overline{DTACK}$ is then asserted (low) on the next falling edge of the CLK. Read data is latched at the PI/T's data bus interface at the same time $\overline{DTACK}$ is asserted. It is stable as long as Chip Select remains asserted independent of other external conditions.

From the above discussion it is clear that if the $\overline{CS}$ setup time prior to the falling edge of the CLK is met, the PI/T can consistently respond to a new read or write bus cycle every four (4) CLK cycles. This fact is especially useful in designing the PI/T's clock in synchronous bus systems not using $\overline{DTACK}$. (An extra CLK period is required in interrupt acknowledge cycles; see Read Cycles via Interrupt Acknowledge.)

In asynchronous bus systems in which the PI/T's CLK differs from that of the bus master, generally there is no way to guarantee that the $\overline{CS}$ setup time with respect to the PI/T CLK is met. Thus, the only way to determine that the PI/T recognized the assertion of $\overline{CS}$ is to wait for the assertion of $\overline{DTACK}$. In this situation, all latched bus inputs to the PI/T must be held stable until $\overline{DTACK}$ is asserted. These include Register Select, R/$\overline{W}$, and write data inputs (see below).

System specifications impose a maximum delay from the trailing (negated) edge of Chip Select to the negated edge of $\overline{DTACK}$. As system speeds increase this becomes more difficult to meet with a simple pullup resistor tied to the $\overline{DTACK}$ line. Therefore, the PI/T provides an internal active pullup device to reduce the rise time, and a level-sensitive circuit that later turns this device off. $\overline{DTACK}$ is negated asynchronously as fast as possible following the rising edge of Chip Select, then three-stated to avoid interference with the next bus cycle.

The system designer must take care that $\overline{DTACK}$ is negated and three-stated quickly enough after each bus cycle to avoid interference with the next one. With the MK68000 this necessitates a relatively fast external path from the data strobe to $\overline{CS}$ going negated.

WRITE CYCLES

In many ways write cycles are similar to normal read cycles (see above). On write cycles, data at the D0-D7 pins must meet the same setup specifications as the Register Select and R/$\overline{W}$ lines. Like these signals, write data is latched on the asserted edge of $\overline{CS}$, and must meet small setup and hold time requirements with respect to that edge. The same bus cycle recovery conditions exist as for normal read cycles. No other differences exist.

READ CYCLES VIA INTERRUPT ACKNOWLEDGE

Special internal operations take place on PI/T interrupt acknowledge cycles. The Port Interrupt Vector Register or the Timer Interrupt Vector Register is implicitly addressed by the assertion of PC6/$\overline{PIACK}$ or PC7/$\overline{TIACK}$, respectively. The signals are first synchronized with the falling edge of the CLK. One clock period after they are recognized the data bus buffers are enabled and the vector is driven onto the bus. $\overline{DTACK}$ is asserted after another clock period to allow the vector some setup time prior to $\overline{DTACK}$. $\overline{DTACK}$ is negated, then three-stated as with the normal read or write cycle, when $\overline{PIACK}$ or $\overline{TIACK}$ is negated.

POWER CONSIDERATIONS

The average chip-junction temperature, T_J, in °C can be obtained from:

$$T_J = T_A + (P_D \bullet \theta_{JA}) \quad (1)$$

Where:

$T_A \equiv$ Ambient Temperature, °C
$\theta_{JA} \equiv$ Package Thermal Resistance, Junction-to-Ambient, °C/W
$P_D \equiv P_{INT} + P_{PORT}$
$P_{INT} \equiv I_{CC} \times V_{CC}$, Watts — Chip Internal Power
$P_{PORT} \equiv$ Port Power Dissipation, Watts — User Determined

For most applications $P_{PORT} \ll P_{INT}$ and can be neglected. P_{PORT} may become significant if the device is configured to drive Darlington bases or sink LED loads.

An approximate relationship between P_D and T_J (if P_{PORT} is neglected) is:

$$P_D = K \div (T_J + 273°C) \quad (2)$$

Solving equations 1 and 2 for K gives:

$$K = P_D \bullet (T_A + 273°C) + \theta_{JA} \bullet P_D 2 \quad (3)$$

Where K is a constant pertaining to the particular part. K can be determined from equation 3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.

VI

MAXIMUM RATINGS

CHARACTERISTICS	SYM	VALUE	UNIT
Supply Voltage	V_{CC}	-0.3 to + 7.0	V
Input Voltage	V_{in}	-0.3 to + 7.0	V
Operating Temperature Range	T_A	0 to 70	°C
Storage Temperature	T_{stg}	-55 to + 150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{CC}).

THERMAL CHARACTERISTICS

CHARACTERISTICS	SYM	VALUE	RATING
Thermal Resistance Ceramic	θ_{JA}	50	°C/W

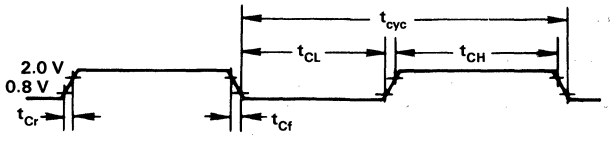
DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 Vdc ± 5%, T_A = 0 to 70°C unless otherwise noted)

CHARACTERISTICS		SYM	MIN	MAX	UNIT
Input High Voltage	All Inputs	V_{IH}	V_{SS} = 2.0	V_{CC}	V
Input Low Voltage	All Inputs	V_{IL}	V_{SS} — 0.3	V_{SS} = 0.8	V
Input Leakage Current (V_{in} = 0 to 5.25 V) H1, H3, R/$\overline{W}$, $\overline{RESET}$, CLK, RS1-RS5, $\overline{CS}$		I_{in}	—	10.0	μA
Three-State (Off State) Input Current (V_{in} = 0.4 to 2.4)	$\overline{DTACK}$, PC0-PC7, D0-D7,		—	20	μA
	H2, H4, PA0-PA7, PB0-PB7	I_{TSI}	-0.1	-1.0	mA
Output High Voltage (I_{Load} = -400 μA, V_{CC} = min)	$\overline{DTACK}$, D0-D7				
(I_{Load} = -150 μA, V_{CC} = min)	H2, H4, PB0-PB7, PA0-PA7	V_{OH}	V_{SS} = 2.4	—	V
(I_{Load} = -100 μA, V_{CC} = min)	PC0-PC7				
Output Low Voltage (I_{Load} = 8.8 mA, V_{CC} = min)	PC3/TOUT, PC5/$\overline{PIRQ}$				
(I_{Load} = 5.3 mA, V_{CC} = min)	D0-D7, $\overline{DTACK}$	V_{OL}	—	0.5	V
(I_{Load} = 2.4 mA, V_{CC} = min)	PA0-PA7, PB0-PB7, H2, H4, PC0-PC2, PC4, PC6, PC7				
Internal Power Dissipation (Measured at T_A = 0°C)		P_{INT}	—	500	mW
Input Capacitance (V_{in} = 0, T_A = 25°C, F = 1 MHz)		C_{in}	—	15	pF

CLOCK TIMING (See Figure 14)

CHARACTERISTIC	SYM	8 MHz MK68230P8		10 MHz MK68230P10		UNIT
		MIN	MAX	MIN	MAX	
Frequency of Operation	f	2.0	8.0	2.0	10.0	MHz
Cycle Time	t_{cyc}	125	500	100	500	ns
Clock Pulse Width	t_{CL}	55	250	45	250	ns
	t_{CH}	55	250	45	250	
Clock Rise and Fall Times	t_{Cr}	—	10	—	10	ns
	t_{Cf}	—	10	—	10	

INPUT CLOCK WAVEFORM
Figure 14



AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 Vdc ± 5%, V_{SS} = 0 Vdc, T_A = 0°C to 70°C)

NUM	CHARACTERISTIC	8 MHz MK68230P8		10 MHz MK68230P10		UNIT
		MIN	MAX	MIN	MAX	
1	R/$\overline{W}$, RS1-RS5 Valid to $\overline{CS}$ Low (Setup Time)	0	—	0	—	ns
2(10)	$\overline{CS}$ Low to R/$\overline{W}$ and RS1-RS5 Invalid (Hold Time)	100	—	65	—	ns
3(1)	$\overline{CS}$ Low to CLK Low (Setup Time)	30	—	20	—	ns
4(2)	$\overline{CS}$ Low to data Out Valid (Delay)	—	75	—	60	ns
5	RS1-RS5 Valid to Data Out Valid (Delay), R/$\overline{W}$ Valid	—	140	—	100	ns
6	CLK Low to $\overline{DTACK}$ Low (Read/Write Cycle) (Delay)	0	70	0	60	ns
7(3)	DTACK Low to $\overline{CS}$ High (Hold Time)	0	—	0	—	ns
8	$\overline{CS}$ or $\overline{PIACK}$ or $\overline{TIACK}$ High to Data Out Invalid (Hold Time)	0	—	0	—	ns
9	$\overline{CS}$ of $\overline{PIACK}$ or $\overline{TIACK}$ High to D0-D7 High-Impedance (Delay)	—	50	—	45	ns
10	$\overline{CS}$ or $\overline{PIACK}$ or $\overline{TIACK}$ High to DTACK High (Delay)	—	50	—	30	ns
11	$\overline{CS}$ or $\overline{PIACK}$ or $\overline{TIACK}$ High to $\overline{DTACK}$ High Impedance (Delay)	—	100	—	55	ns
12	Data In Valid to $\overline{CS}$ Low (Setup Time)	0	—	0	—	ns
13	$\overline{CS}$ Low to Data In Invalid (Hold Time)	100	—	65	—	ns
14	Input Data Valid to H1(H3) Asserted (Setup Time)	100	—	60	—	ns
15	H1(H3) Asserted to Input Data Invalid (Hold Time)	20	—	20	—	ns
16	Handshake Input H1(H4) Pulse Width Asserted	40	—	40	—	ns
17	Handshake Input (H1-H4) Pulse Width Negated	40	—	40	—	ns
18	H1(H3) Asserted to H2(H4) Negated (Delay)	—	150	—	120	ns
19	CLK Low to H2(H4) Asserted (Delay)	—	100	—	100	ns
20(4)	H2(H4) Asserted to H1(H3) Asserted	0	—	0	—	ns
21(5)	CLK Low to H2(H4) Pulse Negated (Delay)	—	125	—	125	ns
22(9, 11)	Synchronized H1(H3) to CLK Low on which $\overline{DMAREQ}$ is Asserted (See Figures 7 and 8)	2.5	3.5	2.5	3.5	CLK Per
23	CLK Low $\overline{DMAREQ}$ is Asserted to CLK Low on which $\overline{DMAREQ}$ is Negated	3	3	3	3	CLK Per
24	CLK Low to Output Data Valid (Delay) (Modes 0, 1)	—	150	—	120	ns
25(9, 11)	Synchronized H1(H3) to Output Data Invalid (Modes 0, 1)	1.5	2.5	1.5	2.5	CLK Per
26	H1 Negated to Output Data Valid (Modes 2, 3)	—	70	—	50	ns
27	H1 Asserted to Output Data High Impedance (Modes 2, 3)	0	70	0	70	ns

AC ELECTRICAL CHARACTERISTICS (Continued) (V_{CC} = 5.0 Vdc ± 5%, V_{SS} = 0 Vdc, T_A = 0°C to 70°C)

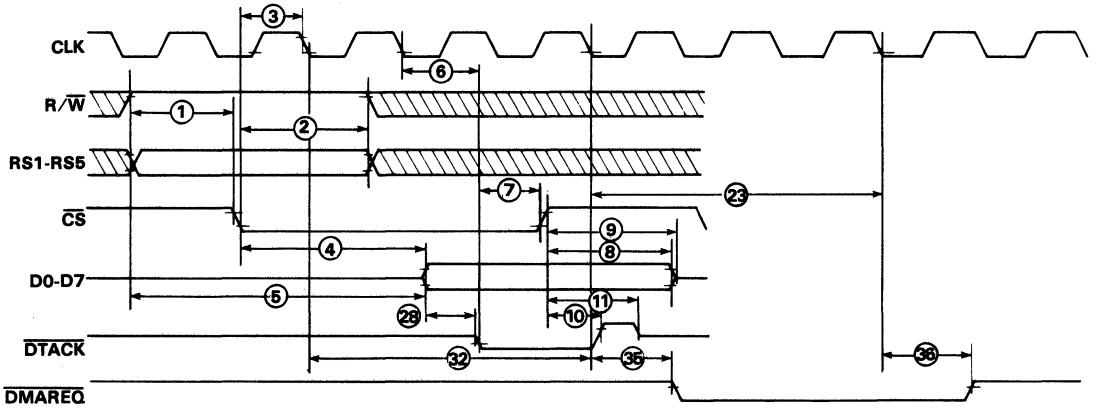
NUM	CHARACTERISTIC	8 MHz MK68230P8 MIN	8 MHz MK68230P8 MAX	10 MHz MK68230P10 MIN	10 MHz MK68230P10 MAX	UNIT
28	Read Data Valid to $\overline{DTACK}$ Low (Setup Time)	0	—	0	—	ns
29	CLK Low to Data Output Valid (Interrupt Acknowledge Cycle)	—	120	—	100	ns
30(7)	H1(H3) Asserted to CLK High (Setup Time)	50	—	40	—	ns
31	$\overline{PIACK}$ or $\overline{TIACK}$ Low to CLK Low (Setup Time)	50	—	40	—	ns
32(11)	Synchronized $\overline{CS}$ to CLK Low on which DMAREQ is Asserted (See Figures 7 and 8)	3	3	3	3	CLK Per
33(9,11)	Synchronized H1(H3) to CLK Low on which H2(H4) is Asserted	3.5	4.5	3.5	4.5	CLK Per
34	CLK Low to $\overline{DTACK}$ Low (Interrupt Acknowledge Cycle (Delay))	—	75	—	75	ns
35	CLK Low to $\overline{DMAREQ}$ Low (Delay)	0	120	0	100	ns
36	CLK Low to $\overline{DMAREQ}$ High (Delay)	0	120	0	100	ns
—	CLK Low to $\overline{PIRQ}$ Low or High Impedance	—	250	—	225	ns
— (8)	TIN Frequency (External Clock) — Prescaler Used	0	1	0	1	Fclk(Hz)(6)
—	TIN Frequency (External Clock) —Prescaler Not used	0	1/32	0	1/32	Fclk(Hz)(6)
—	TIN Pulse Width High or Low (External Clock)	55	—	45	—	ns
—	TIN Pulse Width Low (Run/Halt Control)	1	—	1	—	CLK
—	CLK Low to TOUT High, Low, or High Impedance	0	250	0	225	ns
—	$\overline{CS}$, $\overline{PIACK}$, or $\overline{TIACK}$ High to $\overline{CS}$, $\overline{PIACK}$, or $\overline{TIACK}$ Low	50	—	30	—	ns
37 (11)	Synchronized $\overline{CS}$ to CLK Low on which $\overline{PIRQ}$ is asserted	3	3	3	3	CLK
38(9,11)	Synchronized H1 (H3) to CLK Low on which $\overline{PIRQ}$ is asserted or High Impedance	2.5	3.5	2.5	3.5	CLK

NOTES:

1. This specification only applies if the PI/T had completed all operations initiated by the previous bus cycle when $\overline{CS}$ was asserted. Following a normal read or write bus cycle, all operations are complete within three CLKs after the falling edge of the CLK pin on whict $\overline{DTACK}$ was asserted. If $\overline{CS}$ is asserted prior to completion of these operations, the new bus cycle, and hence, $\overline{DTACK}$ is postponed.
   If all operations of the previous bus cycle were complete when $\overline{CS}$ was asserted, this specification is made only to insure that $\overline{DTACK}$ is asserted with respect to the falling edge of the CLK pin as shown in the timing diagram, not to guarantee operation of the part. If the $\overline{CS}$ setup time is violated, $\overline{DTACK}$ may be asserted as shown, or may be asserted one clock cycle later.
2. Assuming the RS1-RS5 to Data Valid time has also expired.
3. This specification imposes a lower bound on $\overline{CS}$ low time, guaranteeing that $\overline{CS}$ will be low for at least 1 CLK period.
4. This specification assures recognition of the asserted edge of H1(H3).
5. This specification applies only when a pulsed handshake option is chosen and the pulse is not shortened due to an early asserted edge of H1(H3).
6. CLK refers to the actual frequency of the CLK pin, not the maximum allowable CLK frequency.
7. If the setup time on the rising edge of the clock is violated, H1(H3) may not be recognized until the next rising of the clock.
8. This limit applies to the frequency of the signal at TIN compared to the frequency of the CLK signal during each clock cycle. If any period of the waveform at TIN is smaller than the period of the CLK signal at that instant, then it is likely that the timer circuit will completely ignore one cycle of the TIN signal.
   If these two signals are derived from different sources they will have different instantaneous frequency variations. In this case the frequency applied to the TIN pin must be distinctly less than the frequency at the CLK pin to avoid lost cycles of the TIN signal. With signals derived from different crystal oscillators applied to the TIN and CLK pins with fast rise and fall times, the TIN frequency can approach 80 to 90% of the frequency of the CLK signal without a loss of a cycle of the TIN signal.
   If these two signals are derived from the same frequency source then the frequency of the signal applied to TIN can be 100% of the frequency at the CLK pin. They may be generated by different buffers from the same signal or one may be an inverted version of the other. The TIN signal may be generated by an 'AND' function of the clock and a control signal.
9. The maximum value is caused by a peripheral access (H1(H3) asserted) and bus access ($\overline{CS}$ asserted) occurring at the same time.
10. See BUS INTERFACE CONNECTION section for exception.
11. Synchronized means that the input signal has been seen by the PI/T on the appropriate edge of the clock (rising edge for H1(H3) and falling edge for $\overline{CS}$). (Refer to the BUS INTERFACE CONNECTION section for the exception concerning $\overline{CS}$.)

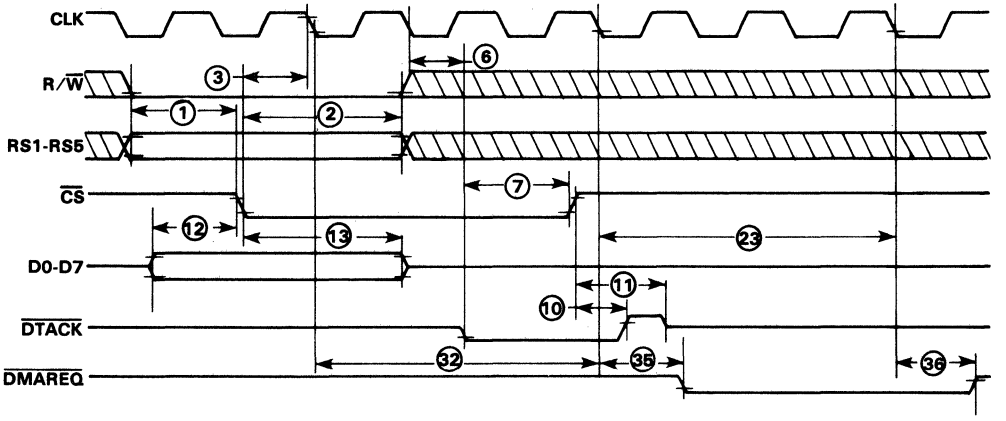
BUS READ CYCLE TIMING

Figure 15



BUS WRITE CYCLE TIMING

Figure 16

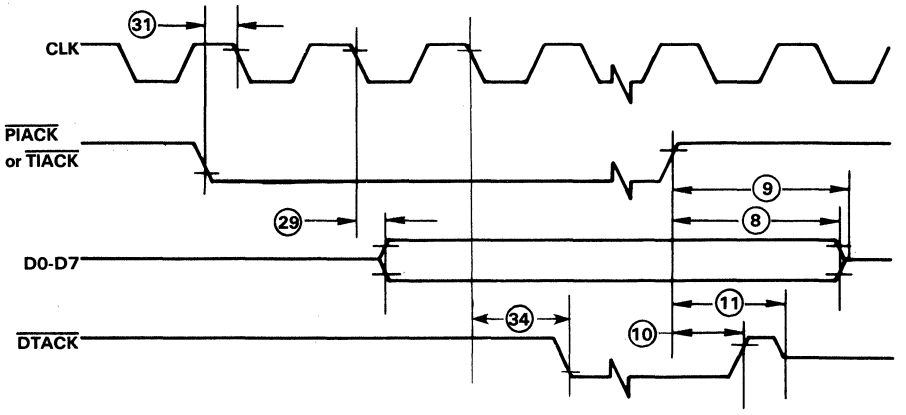


Note: Timing measurements are referenced to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts, unless otherwise noted.

VI

INTERRUPT ACKNOWLEDGE FUNCTIONAL TIMING DIAGRAM

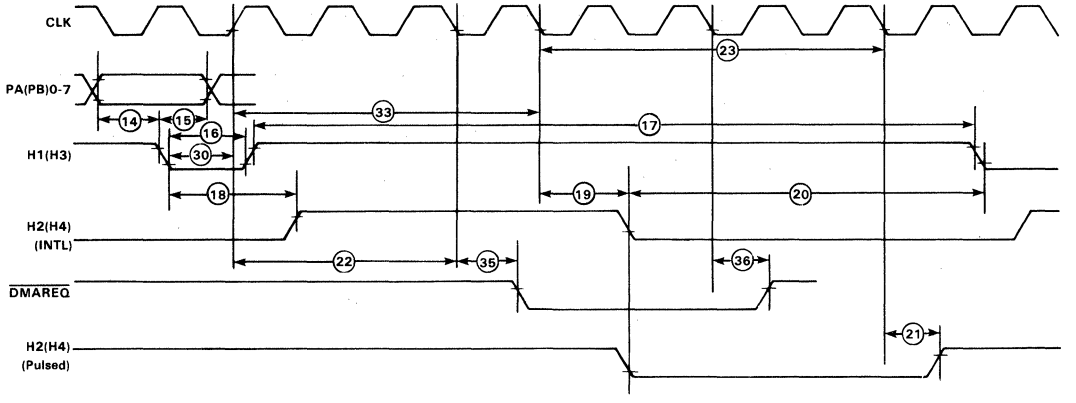
Figure 17



Note: Timing measurements are referenced to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts, unless otherwise noted.

PERIPHERAL INTERFACE INPUT TIMING

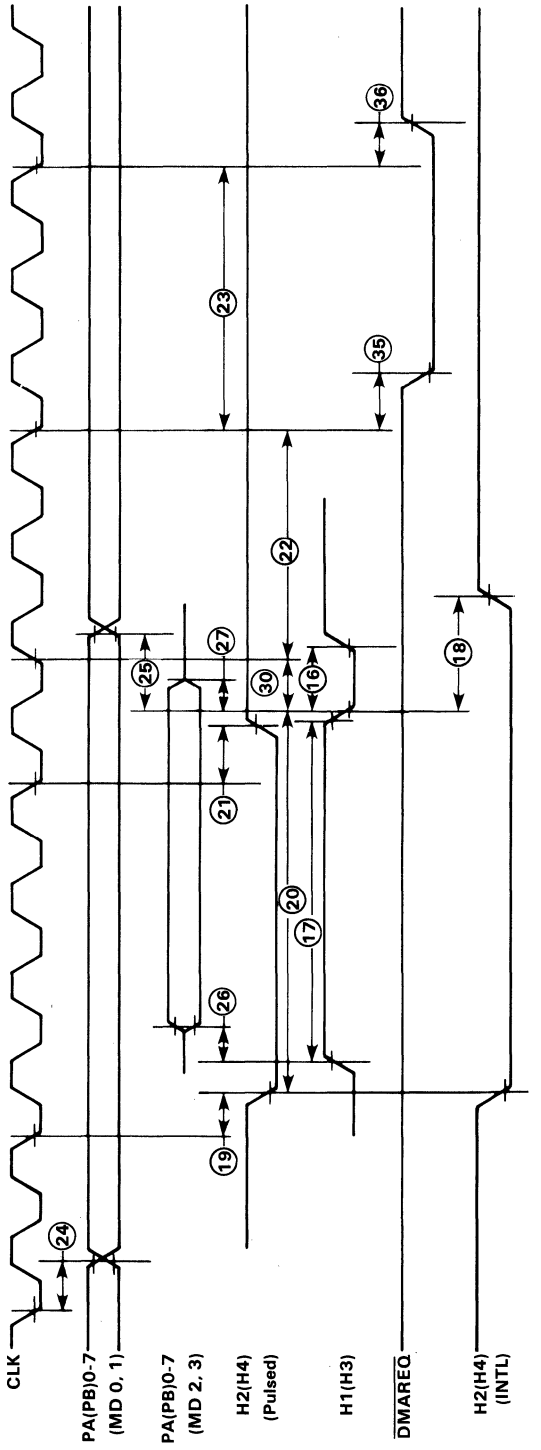
Figure 18



Note: Timing diagram shows H1, H2, H3, and H4 asserted low.

PERIPHERAL INTERFACE OUTPUT TIMING

Figure 19



NOTE: Timing diagram shows H1, H2, H3, and H4 asserted low.

MK68230 ORDERING INFORMATION

PART NO.	PACKAGE TYPE	MAX. CLOCK FREQUENCY	TEMPERATURE RANGE
MK68230P-8	Ceramic	8.0 MHz	0° to 70°C
MK68230P-10	Ceramic	10.0 MHz	

MOSTEK®

68000 MICROCOMPUTER PERIPHERALS

Serial Input Output

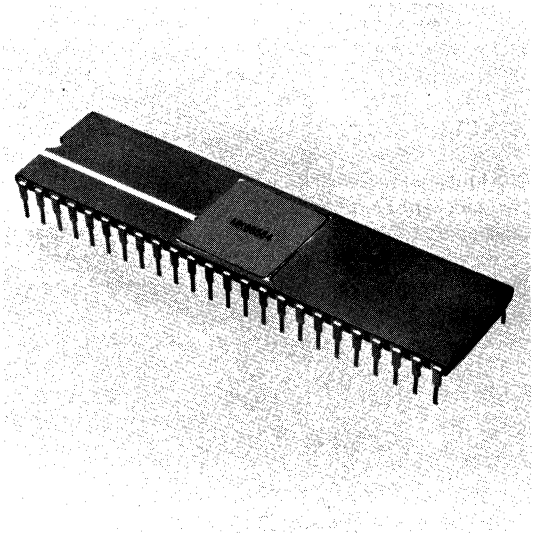
MK68564

FEATURES

- ☐ Self-test capability
- ☐ Directly addressable registers (all control registers are read/write)
- ☐ Two independent full-duplex channels
- ☐ Data rate in synchronous or asynchronous modes
  - 0-1 M bits/second with 5.0 MHz system clock rate
- ☐ Receiver data registers quadruply buffered, transmitter double buffered
- ☐ Asynchronous features:
  - 5, 6, 7, or 8 bits/character
  - 1, 1½, or 2 stop bits
  - Even, odd or no parity
  - x1, x16, x32, and x64 clock modes
  - Break generation and detection
  - Parity, overrun and framing error detection
- ☐ Byte synchronous features:
  - Internal or external character synchronization
  - One or two sync characters in separate registers
  - Automatic sync character insertion
  - CRC generation and checking
- ☐ Bit synchronous features:
  - Abort sequence generation and detection
  - Automatic zero insertion and deletion
  - Automatic flag insertion between messages
  - Address field recognition
  - I-field residue handling
  - Valid receive messages protected from overrun
  - CRC generation and checking
  - Separate modem control inputs and outputs for both channels
  - CRC-16 or CRC-CCITT block check
- ☐ Daisy-Chain Priority interrupt logic provides automatic interrupt vectoring without external logic
- ☐ Modem status can be monitored
- ☐ N-channel silicon-gate depletion-load technology
- ☐ 48 pin DIP

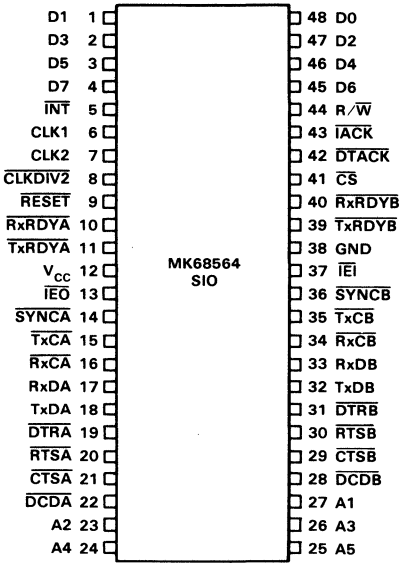
MK68564

Figure 1



PIN DESCRIPTION

Figure 2



VI

- Single 5 V power supply
- Single-phase TTL clock or XTAL CLK
- All inputs and outputs TTL compatible

INTRODUCTION

The MK68564 SIO (Serial Input Output) is a dual-channel, multi-function peripheral circuit designed to satisfy a wide variety of serial data communications requirements in microcomputer systems. It is one of a series of peripherals that will directly support the MK68000. The MK68564 is capable of handling asynchronous and synchronous byte-oriented protocols, such as IBM Bisync, and synchronous bit-oriented protocols, such as HDLC and IBM SDLC. The SIO is fabricated in N-channel silicon gate depletion load MOS technology, and it is packaged in a 48 pin DIP.

FUNCTIONAL CAPABILITIES

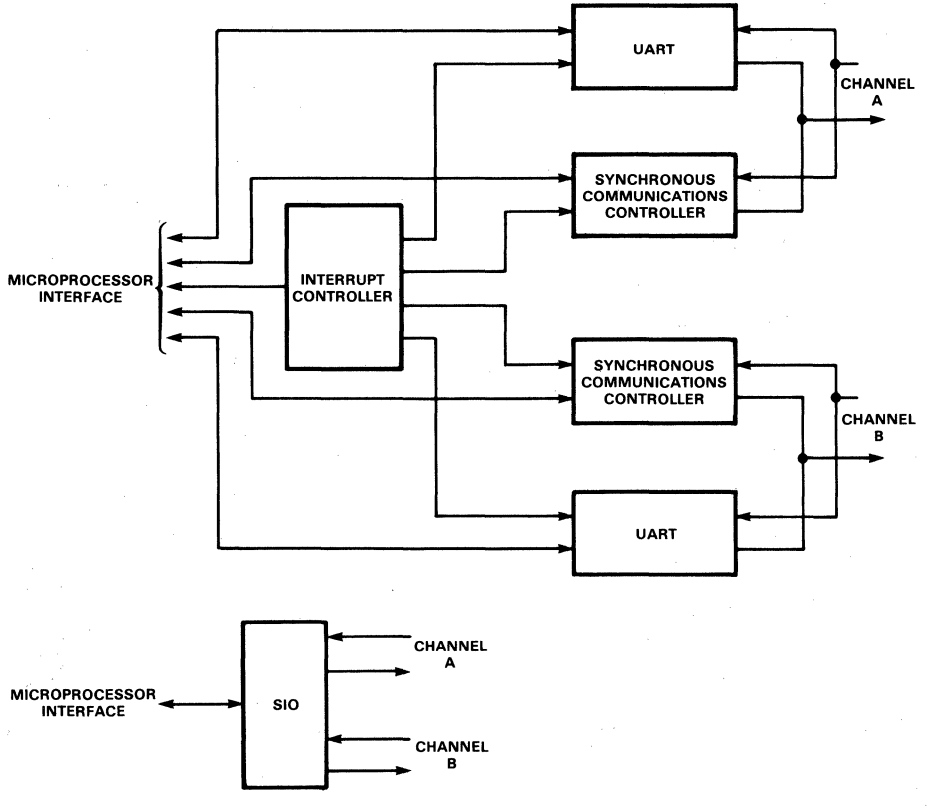
The functional capabilities of the SIO can be described from two different points of view. As a data communications device, the SIO transmits and receives serial data in a wide variety of data-communication protocols. As an MK68000 family peripheral, it interacts with the MK68000 CPU and other peripheral circuits, sharing the data, address and control buses, as well as being a part of the MK68000 interrupt structure. As a peripheral to other microprocessors, the SIO offers valuable features such as non-vectored interrupts, polling and simple handshake capability.

Figure 3 illustrates the conventional devices that the SIO replaces.

SIO PIN DESCRIPTION

D0-D7 — System Data Bus (Bidirectional, Tri-state, Active High). The data pins are driven out when R/$\overline{W}$ is high and $\overline{CS}$ is asserted. Valid data is input to the SIO when R/$\overline{W}$ is low and $\overline{CS}$ is asserted. The data bus is latched on the falling edge of $\overline{CS}$ during a write cycle. The interrupt vector is driven out when $\overline{IACK}$ is asserted, when $\overline{IEI}$ is asserted and the SIO is generating an interrupt.

CONVENTIONAL DEVICES REPLACED BY THE SIO
Figure 3



A1-A5 — Address Bus (Inputs, Active High). The five-bit address bus determines one of the 32 possible internal SIO register addresses. This bus is latched on-chip by the falling edge of $\overline{CS}$. At present there are only 21 internal registers implemented on the SIO.

$\overline{CS}$ — Chip Select (Input, Active low). $\overline{CS}$ is used both to select the SIO and to provide the necessary internal timing to the SIO. $\overline{CS}$ is a combination of address decode for the chip and either upper or lower data strobe from the MK68000. R/$\overline{W}$, address bus (A1-A5), and input data bus (D0-D7) are latched on-chip on the falling edge of $\overline{CS}$. In addition, $\overline{CS}$ must not be asserted on an interrupt acknowledge cycle.

R/$\overline{W}$ — Read/Write (Input). R/$\overline{W}$ is the signal from the bus master indicating whether the current bus cycle is a Read (High) or Write (Low) cycle. R/$\overline{W}$ is latched by the SIO on the falling edge of $\overline{CS}$.

$\overline{DTACK}$ — Data Transfer Acknowledge (Output, Active Low, Tri-State). $\overline{DTACK}$ is an active low output sent by the SIO to terminate the current bus cycle. $\overline{DTACK}$ is asserted when valid data is available on the data bus during a read or $\overline{IACK}$ cycle, or after data has been accepted during a write cycle. $\overline{DTACK}$ is negated following negation of $\overline{CS}$ or $\overline{IACK}$. When $\overline{DTACK}$ is negated, the output is driven momentarily high before entering the tri-state mode. $\overline{DTACK}$ will remain tri-stated until the next $\overline{CS}$ or $\overline{IACK}$ cycle.

$\overline{INT}$ — Interrupt Request (Output, Open Drain, Active Low). $\overline{INT}$ is asserted when the SIO is requesting an interrupt. $\overline{INT}$ is negated during an $\overline{IACK}$ cycle or by clearing the pending interrupt(s) with software.

$\overline{IACK}$ — Interrupt Acknowledge (Input, Active Low). The SIO will begin an interrupt acknowledge cycle when $\overline{IACK}$ is asserted if $\overline{IEI}$ is low and the SIO is requesting an interrupt ($\overline{INT}$ pin driven low by the SIO).

$\overline{IEI}$ — Interrupt Enable In (Input, Active Low). When $\overline{IEI}$ is asserted, the SIO can respond to an interrupt acknowledge ($\overline{IACK}$) signal.

$\overline{IEO}$ — Interrupt Enable Out (Output, Active Low). $\overline{IEO}$ will be asserted only when $\overline{IEI}$ and $\overline{IACK}$ are asserted and the SIO is not requesting an interrupt.

$\overline{RESET}$ — (Input, Active Low). A low level disables both receivers and transmitters, forces TxDA and TxDB marking, forces the modem controls high and disables all interrupts. The control registers must be rewritten after the SIO is reset and before data is transmitted or received.

CLK1, CLK2 — Clock In (Input) (Output, Special). CLK1 and CLK2 can be connected to an external crystal time base or CLK1 alone may be used to input a TTL compatible square wave signal to provide internal timing for the SIO.

$\overline{CLKDIV2}$ — Clock Divide by 2 (Input, Active Low, Internal Pull Down). If $\overline{CLKDIV2}$ is left open or driven low, the external clock is divided by 2. This mode must be used for a crystal time base. If $\overline{CLKDIV2}$ is driven high, no division of the external clock takes place.

V_{CC} — 5 volts (±5%)

GND — Ground

$\overline{RxRDYA}$, $\overline{TxRDYA}$, $\overline{RxRDYB}$, $\overline{TxRDYB}$ — (Outputs, Active Low, Tri-State) When enabled, these outputs reflect the inverted state of the receive character available status bit (RxRDY) and the transmit buffer empty status bit (TxRDY). When disabled, the outputs are tri-stated. These outputs may be used for DMA control.

$\overline{CTSA}$, $\overline{CTSB}$ — Clear to Send (Inputs Active Low). When programmed as Auto Enables, a low on these inputs enables the respective transmitter. If not programmed as Auto Enables, these inputs may be programmed as general purpose inputs. Both inputs are Schmitt-trigger buffered to accommodate slow resetting inputs. The SIO detects pulses on these inputs and interrupts the CPU if external/status interrupts are enabled on both logic level transitions. The Schmitt trigger inputs do not guarantee a specified noise level margin.

$\overline{DCDA}$, $\overline{DCDB}$ — Data Carrier Detect (Inputs, Active Low). These signals are similar to the CTS inputs, except they can be used as receiver enables.

VI

$\overline{RxDA}$, $\overline{RxDB}$ Receive Data (Inputs, Active High).

TxDA, TxDB Transmit Data (Outputs, Active High).

$\overline{RxCA}$, $\overline{RxCB}$ Receiver Clocks (Inputs). The Receive Clocks may be 1, 16, 32 or 64 times the data rate in asynchronous modes. Receive data is sampled on the rising edge of $\overline{RxC}$.

$\overline{TxCA}$, $\overline{TxCB}$ Transmitter Clocks (Inputs). In asynchronous modes, the Transmitter clocks may be 1, 16, 32 or 64 times the data rate. The multiplier for the transmitter and the receiver must be the same. Both the $\overline{TxC}$ and $\overline{RxC}$ inputs are Schmitt trigger buffered for relaxed rise and fall time requirements (no noise margin is specified). TxD changes on the falling edge of $\overline{TxC}$.

$\overline{RTSA}$, $\overline{RTSB}$ Request to Send (Outputs, Active Low). When the RTS bit is set, the RTS output goes low. When the RTS bit is reset in the Asynchronous mode, the output goes high after the transmitter is empty. In Synchronous modes, the $\overline{RTS}$ pin strictly follows the inverted state of the RTS bit. Both pins can be used as general purpose outputs.

$\overline{DTRA}$, $\overline{DTRB}$ Data Terminal Ready (Outputs, Active Low). These outputs follow the inverted state programmed into the DTR bit. They can be used as general purpose outputs.

$\overline{SYNCA}$, $\overline{SYNCB}$ Synchronization (Inputs/Outputs Active Low). These pins can act either as inputs or outputs. In the Asynchronous Receive mode, they are inputs similar to $\overline{CTS}$ and $\overline{DCD}$. In this mode, the transitions on these lines affect the state of the Sync/Hunt status bits. In the External Sync mode, these lines also act as inputs. When external synchronization is achieved, $\overline{SYNC}$ must be driven low on the second rising edge of $\overline{RxC}$ after the rising edge of $\overline{RxC}$ on which the bit of the sync character was received. In other words, after the sync pattern is detected, the external logic must wait for two full Receive Clock cycles to activate the $\overline{SYNC}$ input. Once $\overline{SYNC}$ is forced low, it is wise to keep it low until the CPU informs the external sync logic that synchronization has been lost or a new message is about to start. Character assembly begins on the rising edge of $\overline{RxC}$ that immediately precedes the falling edge of $\overline{SYNC}$ in the External Sync mode. In the Internal Synchronization mode (Monosync and Bisync), these pins act as outputs that are asserted during the part of the receive clock ($\overline{RxC}$) cycle in which sync characters are recognized. The sync condition is not latched, so these outputs are asserted each time a sync pattern is recognized regardless of character boundaries.

I/O CAPABILITIES

The SIO offers the choice of Polling, Interrupt (vectored or non-vectored) and DMA Transfer modes to transfer data, status and control information to and from the CPU.

POLLING

The polled mode avoids interrupts. Two status registers, ST0 and ST1, are updated at appropriate times for each function being performed (for example, CRC error status valid at the end of the message).

While in its Polling sequence, the CPU examines the contents of the status registers for each channel; the status bits serve as an acknowledge to the poll inquiry. The two ST0 bits D0 and D2 indicate that a receive or transmit data transfer is needed. The status also indicates error or other special status conditions. The special receive condition status contained in ST1 does not have to be read in the Polling sequence until the Receive Character Available status in ST0 is valid.

INTERRUPTS

The SIO offers an elaborate interrupt scheme to provide fast interrupt response in real-time applications. The interrupt vector points to an interrupt service routine in the memory. To service operations in both channels and to eliminate the necessity of writing a status analysis routine, the SIO can modify the interrupt vector so it points directly to one of eight interrupt service routines. This is done under program control by setting the program bit called "Status Affects Vector". When this bit is set, the interrupt vector is modified according to the assigned priority of the various interrupting conditions.

Transmit interrupts, Receive interrupts and External/Status interrupts are the sources of interrupts. Each interrupt source is enabled under program control with Channel A having a higher priority than Channel B, and with Receiver, Transmitter and External/Status interrupts prioritized in that order within each channel. When the Transmit interrupt is enabled, the CPU is interrupted after the transmit buffer becomes empty. (This implies that the transmitter must have a data character written into it so it can become empty). When enabled, the receiver can interrupt the CPU in one of three ways:

Interrupt on first receive character
Interrupt on all receive characters
Interrupt on a Special Receive condition

Interrupt On First Character is typically used with the DMA Transfer mode. Interrupt On All Receive Characters has the option of modifying the interrupt vector in the event of a parity error. The Special Receive Condition interrupt can occur on a character or message basis (End of Frame interrupt in SDLC, for example). The Special Receive condition can cause an interrupt only if the Interrupt On First Receive Character or Interrupt On All Receive Characters mode is selected. In Interrupt On First Receive Character, an interrupt can occur from Special Receive conditions (except Parity Error) after the first receive character interrupt (example: Receive Overrun interrupt).

The main function of the External/Status interrupt is to monitor the signal transitions of the $\overline{CTS}$, $\overline{DCD}$ and $\overline{SYNC}$ pins; however, an External/Status interrupt is also caused by a Transmit Underrun condition or by the detection of a Break (Asynchronous mode) or Abort (SDLC mode) sequence in the data stream. The interrupt caused by the Break/Abort sequence has a special feature that allows the SIO to interrupt when the Break/Abort sequence is detected or terminated. The feature facilitates the proper termination of the current message, correct initialization of the next message, and the accurate timing of the Break/Abort condition in external logic.

DMA TRANSFER

The SIO provides 4 outputs that can be used for DMA control (2 per channel). Each output has a separate enable bit in the control registers. The outputs will be in a tri-state condition after RESET. The $\overline{RxRDY}$ output is associated with the receiver. When enabled, $\overline{RxRDY}$ will go low each time the receive buffer has data available. It will be driven high after each read from the receiver data buffer. $\overline{TxRDY}$ is associated with the transmit data buffer. If enabled, $\overline{TxRDY}$ will go low each time the data buffer contents are transferred to the transmit shift register. When the transmit data buffer is reloaded, $\overline{TxRDY}$ will be driven high.

DATA COMMUNICATIONS CAPABILITIES

The SIO provides two independent full duplex channels. Each channel can be programmed to operate in either asynchronous or synchronous communication modes.

ASYNCHRONOUS MODES

Transmission and reception can be done independently on each channel with five to eight bits per character, plus optional even or odd parity. The transmitters can supply one, one and a half or two stop bits per character and can provide a break output at any time. The receiver break detection logic interrupts the CPU both at the start and end of a received break. Reception is protected from spikes by a transient spike rejection mechanism that checks the signal one half bit time after a low level is detected on the receive data input (RxDA or RxDB). If the low does not persist—as in the case of a transient—the character assembly process is not started.

Framing errors and overrun errors are detected and buffered together with the character on which they occurred. Vectored interrupts allow fast servicing of error conditions using dedicated routines. Furthermore, a built-in checking process avoids interpreting a framing error as a new start bit; a framing error results in the addition of one half bit time to the point at which the search for the next start bit is begun.

The SIO does not require symmetric transmit and receive clock signals—a feature that allows it to be used with many other clock sources. The transmitter and receiver can handle data at a rate of 1, 1/16, 1/32 or 1/64 of the clock rate supplied to the receive and transmit clock inputs. In asynchronous modes, the SYNC pin may be programmed as an input.

SYNCHRONOUS MODES

The SIO supports both byte-oriented and bit-oriented synchronous communication. Synchronous byte-oriented protocols can be handled in several modes that allow character synchronization with an 8-bit sync character (Monosync), any 16-bit sync pattern (Bisync) or with an external sync signal. Leading sync characters can be removed without interrupting the CPU.

CRC checking for synchronous byte-oriented modes is delayed by one character time so the CPU may disable CRC checking on specific characters. This permits implementation of protocols such as IBM Bisync. Both CRC-16 ($X^{16} + X^{15} + X^2 + 1$) and CCITT ($X^{16} + X^{12} + X^6 + 1$) error checking polynomials are supported. In all non-SDLC modes, the CRC generator is initialized to 0's; in SDLC modes, it is initialized to 1's. The SIO can be used for interfacing to peripherals such as hard-sectored floppy disks, but it cannot generate or check CRC for IBM-compatible soft-sectored disks. The SIO also provides a feature that automatically transmits CRC data when no other data is available for transmission. This allows very high-speed transmissions under DMA control with no need for CPU intervention at the end of a message. When there is no data or CRC to send in synchronous modes, the transmitter inserts 8- or 16-bit sync characters regardless of the programmed character length.

The SIO supports synchronous bit-oriented protocols such as SDLC and HDLC by performing automatic flag sending, zero insertion and CRC generation. A special command can be used to abort a frame in transmission. At the end of a message the SIO automatically transmits the CRC and trailing flag when the transmit buffer becomes empty. If a transmit underrun occurs in the middle of a message, an external/status interrupt warns the CPU of this status change so that an abort may be issued. One to eight bits per

character can be sent, which allows reception of a message with no prior information about the character structure in the information field of a frame.

The receiver automatically synchronizes on the leading flag of a frame in SDLC or HDLC, and provides a synchronization signal on the SYNC pin; an interrupt can also be programmed. The receiver can be programmed to search for frames addressed by a single byte to only a specified user-selected address or to a global address. In this mode, frames that do not match either the user-selected or global address are ignored. The number of address bytes can be extended under software control. For receiving data, an interrupt on the first received character or on every character can be selected. The receiver automatically deletes all zeroes inserted by the transmitter during character assembly. It also calculates and automatically checks the CRC to validate frame transmission. At the end of transmission, the status of a received frame is available in the status registers.

The SIO can be conveniently used under DMA control to provide high-speed reception or transmission. In reception, for example, the SIO can interrupt the CPU when the first character of a message is received. The CPU then enables the DMA to transfer the message to memory. The SIO then issues an end-of-frame interrupt and the CPU can check the status of the received message. Thus, the CPU is freed for other service while the message is being received.

SIO INTERFACE DESCRIPTION

The SIO is designed for simple and efficient interface to a MK68000 CPU system. All data transfers between the SIO and the CPU are asynchronous to the system clock. The SIO system timing is derived from the chip select input ($\overline{CS}$) during normal read and write sequences and from the interrupt acknowledge input ($\overline{IACK}$) during an exception processing sequence. Chip select is a function of address decode and (normally) lower data strobe ($\overline{LDS}$). Interrupt acknowledge ($\overline{IACK}$) is a function of the interrupt level on address lines A1, A2, & A3, an interrupt acknowledge function code (FC0 - FC2) and lower data strobe ($\overline{LDS}$). NOTE: $\overline{CS}$ and $\overline{IACK}$ can never be asserted at the same time.

READ SEQUENCE

The SIO will begin a read cycle (see Figure 4) if on the falling edge of $\overline{CS}$ the read-write (R/$\overline{W}$) pin is high. The SIO will respond by decoding the address bus (A1-A5) for the register selected, by placing the contents of the register on the data bus pins (D0-D7), and by driving the data transfer acknowledge ($\overline{DTACK}$) pin low. If the register selected is not implemented on the SIO, the data bus pins will be driven high and then $\overline{DTACK}$ will be asserted. When the CPU has acquired the data, the $\overline{CS}$ signal is driven high, at which time the SIO will drive $\overline{DTACK}$ high, then tri-state $\overline{DTACK}$ and D0-D7.

WRITE SEQUENCE

The SIO will begin a write cycle (see Figure 4) if on the falling edge of $\overline{CS}$ the R/$\overline{W}$ pin is low. The SIO will respond by latching the data bus, by decoding the address bus for the register selected, by loading the register with the contents of the data bus, and by driving $\overline{DTACK}$ low. When the CPU has finished the cycle, the $\overline{CS}$ signal is driven high. At this time, the SIO will drive $\overline{DTACK}$ high, then tri-state DTACK. If the register selected is not implemented on the SIO, the normal write sequence will proceed but the data bus contents will not be stored.

INTERRUPT SEQUENCE

The SIO is designed to operate as an independent interrupting peripheral or, if interconnected with other components, an interrupt priority daisy chain is formed.

INDEPENDENT OPERATION

Independent operation requires that the $\overline{IEI}$ pin be tied low. The SIO starts the interrupt sequence by driving the Interrupt Request ($\overline{INT}$) pin low. The CPU responds to the interrupt by driving the SIO $\overline{IACK}$ pin low (see Figure 5). The highest priority interrupt request in the SIO, at the time $\overline{IACK}$ goes low, places its vector on the data bus pins. The interrupt request is then cleared. The SIO releases the $\overline{INT}$ pin and drives $\overline{DTACK}$ low. When the CPU has acquired the vector, the $\overline{IACK}$ signal is driven high. The SIO responds by driving $\overline{DTACK}$ to a high level then tri-stating $\overline{DTACK}$ and the data bus (D0-D7). If more than one interrupt request is pending at the start of an interrupt acknowledge sequence, the SIO will drive the Interrupt Request ($\overline{INT}$) pin low following the completion of the interrupt acknowledge cycle. This sequence will continue until all pending interrupts are cleared. If the SIO is not requesting an interrupt when the $\overline{IACK}$ pin goes low, the SIO will not respond to $\overline{IACK}$, and the data bus and $\overline{DTACK}$ will remain tri-stated.

DAISY CHAIN OPERATION

The Interrupt Priority Daisy Chain is formed by connecting the Interrupt Enable Out ($\overline{IEO}$) pin of a higher priority device to the Interrupt Enable In ($\overline{IEI}$) pin of the next lower priority device. The highest priority device in the chain should have its $\overline{IEI}$ pin tied low. The interrupt sequence described under independent operation is still valid with these exceptions: the vector will not be placed on the data bus pins nor will the $\overline{DTACK}$ pin be driven low until the $\overline{IEI}$ pin is low. If the SIO is not requesting an interrupt at the start of an Interrupt Acknowledge Sequence, the SIO $\overline{IEO}$ pin will follow the $\overline{IEI}$ pin.

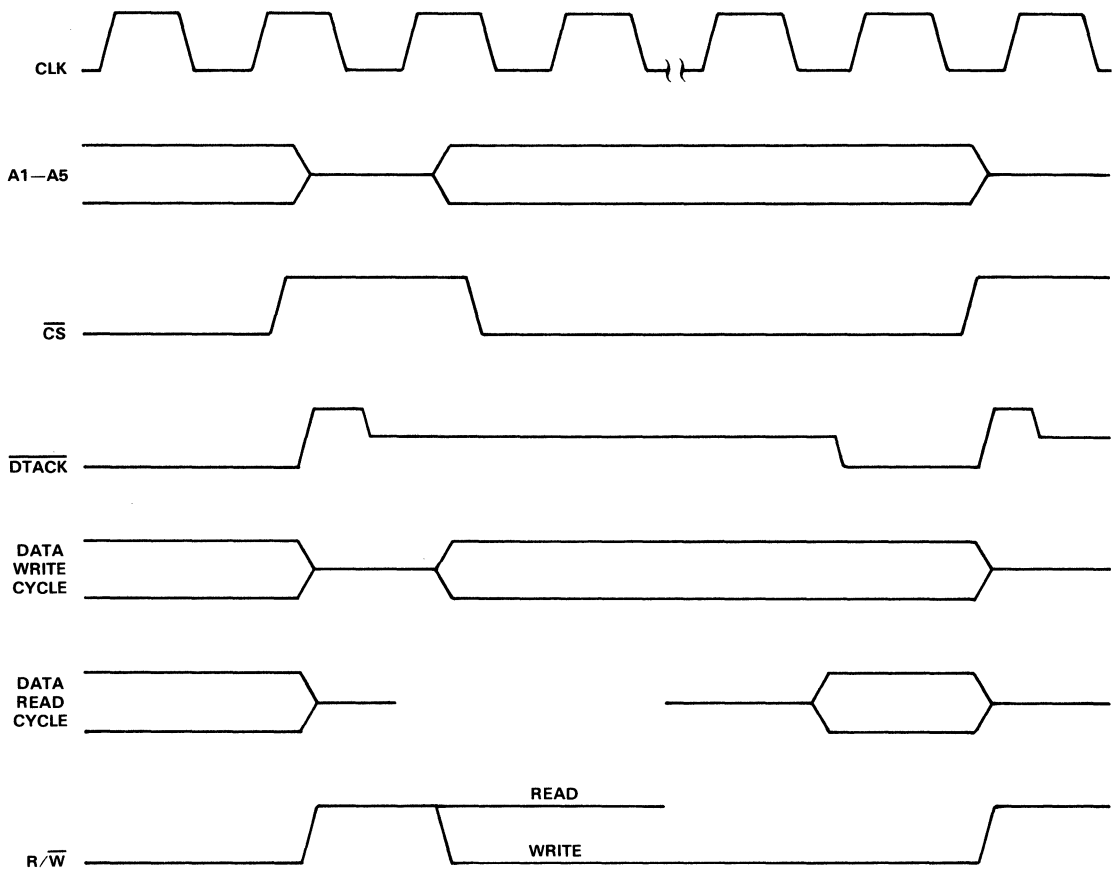
SELF-TEST

When the loop bit is set the receiver shift clock ($\overline{RxC}$) pin and

the receiver data input (RxD) pin are electrically disconnected from the internal logic. The Transmit Data Output (TxD) is connected to the internal receiver data logic and the Transmit Shift Clock ($\overline{TxC}$) pin is connected to the internal receiver shift clock logic. All other features of the SIO are unaffected.

SIO READ AND WRITE TIMING DIAGRAM

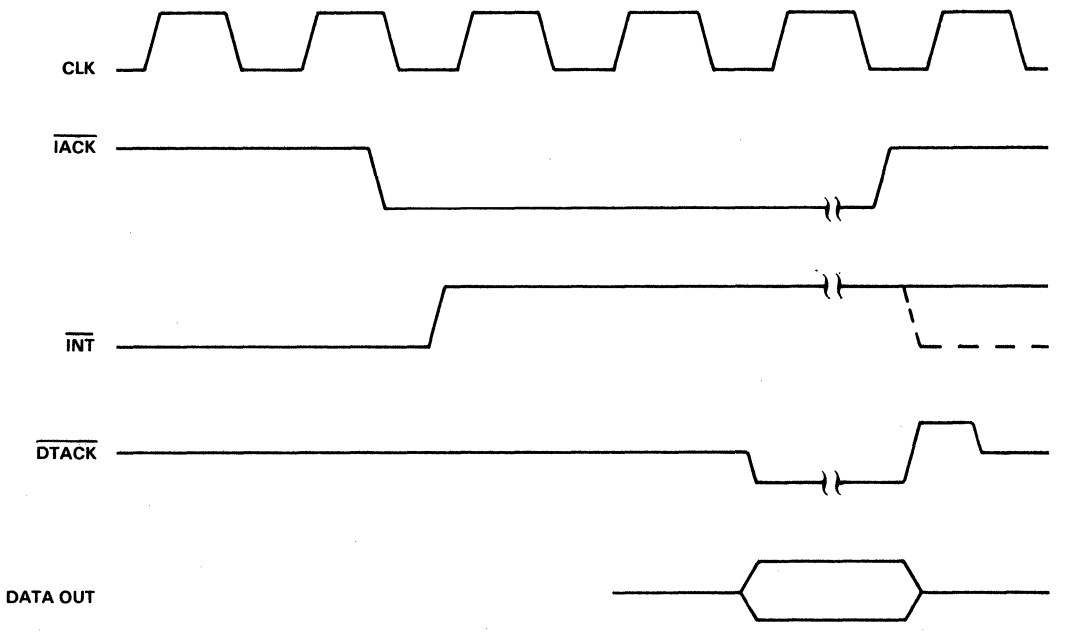
Figure 4



VI

SIO INTERRUPT TIMING DIAGRAM

Figure 5



ADVANCE INFORMATION

MOSTEK®

68000 MICROCOMPUTER PERIPHERALS

Multi-Function Peripheral

MK68901

FEATURES

- ☐ Four timers with individually programmable prescaling
  - Two multimode timers
    - Delay mode
    - Pulse width measurement mode
    - Event counter mode
  - Two delay mode timers
- ☐ 16 source interrupt controller
  - 8 internal sources
  - 8 external sources
  - Individual source enable
  - Individual source masking
  - Programmable interrupt service modes
    - Polling
    - Vector generation
      - Optional In-service status
- ☐ 8 input/output pins
  - Individually programmable direction
  - Individual interrupt source capability
    - Programmable edge selection
- ☐ Single channel USART
  - Full duplex
  - Asynchronous to 62.5 kbps
  - Byte synchronous to 1 Mbps
  - Internal/external baud rate generation
  - DMA handshake signals
  - Modem control
- ☐ MK68000 BUS compatible
- ☐ 48 Pin dip

INTRODUCTION

The MK68901 MFP (Multi-Function Peripheral) is a combination of many of the necessary peripheral functions in a microprocessor system. Included are:

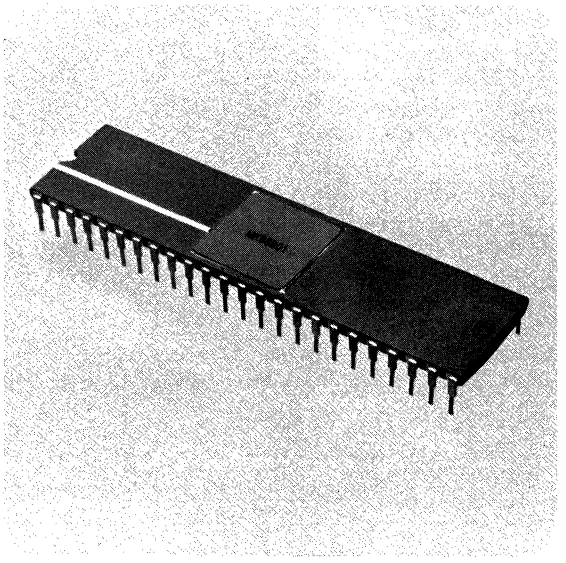
Four timers

Interrupt controller for 16 sources

Eight parallel I/O lines

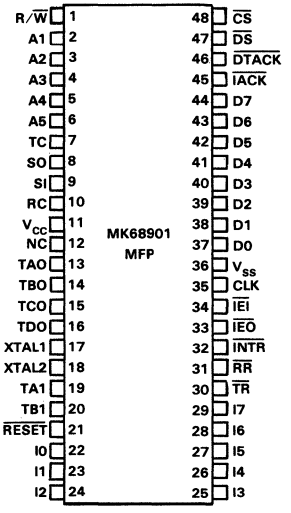
Single channel USART

MK68901
Figure 1



DEVICE PINOUT

Figure 2



The use of the MFP in a system can significantly reduce chip count, thereby reducing system cost. The MFP is completely MK68000 bus compatible, and 24 directly addressable internal registers provide the necessary control and status interface to the programmer.

The MFP is an enhancement of the MK3801 STI, a Z80 family peripheral.

PIN DESCRIPTION

Vss: Ground

Vcc: +5 volts (± 5%)

$\overline{CS}$: Chip Select (Input, Active Low). Used to activate the MK68901 MFP for accesses to the registers.

$\overline{DS}$: Data Strobe (Input, Active Low). Used as part of the chip select and interrupt acknowledge functions.

R/$\overline{W}$: Read/Write (Input, Active High for read, Active Low for write).

$\overline{DTACK}$: Data Transfer Acknowledge (Output, Active Low). Used to signal the CPU that data is ready, or that data has been accepted by the MK68901 MFP.

A1-A5: Address Inputs. Used to address one of the internal registers during a read or write operation.

D0-D7: Data Bus (Bi-Directional). Used to receive data from or transmit data to one of the internal registers during a read or write operation. Also used to pass a vector during interrupt acknowledge.

$\overline{RESET}$: Device Reset (Input, Active Low). When activated, all internal registers (except for timer, USART Data registers, and transmit status register) will be cleared. All timers will be stopped. The USART receiver and transmitter will be disabled. All interrupt channels will be disabled and all pending interrupts will be cleared. The General Purpose I/O and Interrupt lines will be placed in the tri-state input mode. All timer outputs will be forced to the low (logic "0") state.

I0-I7: General Purpose I/O and Interrupt lines. These lines may be used as I/O lines and/or interrupt inputs. When used as interrupt inputs, their active edge is programmable. A data direction register is used to define which lines are to be Hi-Z inputs and which lines are to be push-pull TTL compatible outputs.

$\overline{INTR}$: Interrupt Request (Output, Active Low, open drain). Used to communicate an interrupt request from the MK68901 to the CPU.

$\overline{IACK}$: Interrupt Acknowledge. (Input, Active Low). Used to signal the MK68901 that the CPU is a knowledging its interrupt. $\overline{CS}$ and $\overline{IACK}$ are mutually exclusive.

$\overline{IEI}$: Interrupt Enable In (Input, Active Low). Used to signal the MK68901 that no higher priority device is requesting interrupt service.

$\overline{IEO}$: Interrupt Enable Out (Output, Active Low). Used to signal lower priority peripherals that neither the MK68901 nor another higher priority peripheral is requesting interrupt service.

SO: Serial Output. The output of the USART transmitter.

SI: Serial Input. The input to the USART receiver.

RC: Receiver Clock (Input). Controls the serial bit rate of the USART receiver.

TC: Transmitter Clock (Input). Controls the serial bit rate of the USART transmitter.

$\overline{RR}$: Receiver Ready (Output, Active Low). DMA output for receiver.

$\overline{TR}$: Transmitter Ready (Output, Active Low). DMA output for transmitter.

TAO, TBO, TCO, TDO: Timer Outputs. Each of the four timers has an output which can produce a square wave. The output will change states each timer cycle; thus one full period of the timer out signal is equal to two timer cycles. TAO or TBO can be reset (logic "0") by a write to TACR, or TBCR, respectively.

XTAL1, XTAL2: Timer Clock inputs. A crystal can be connected between XTAL1 and XTAL2, or XTAL1 can be driven with a TTL level clock. All chip accesses are independent of the timer clock.

TAI, TBI: Timer A, B inputs. Used when running the timers in the event count or the pulse width measurement mode. The interrupt channels associated with I4 and I3 are used for TAI and TBI, respectively. Thus, when running a timer in one of these two modes, I4 or I3 can be used for I/O only.

REGISTER MAP

Figure 3

ADDRESS	ABBREVIATION	REGISTER NAME
0	GPIP	GENERAL PURPOSE I/O
1	AER	ACTIVE EDGE REGISTER
2	DDR	DATA DIRECTION REGISTER
3	IERA	INTERRUPT ENABLE REGISTER A
4	IERB	INETRRUPT ENABLE REGISTER B
5	IPRA	INTERRUPT PENDING REGISTER A
6	IPRB	INTERRUPT PENDING REGISTER B
7	ISRA	INTERRUPT IN-SERVICE REGISTER A
8	ISRB	INTERRUPT IN-SERVICE REGISTER B
9	IMRA	INTERRUPT MASK REGISTER A
A	IMRB	INTERRUPT MASK REGISTER B
B	VR	VECTOR REGISTER
C	TACR	TIMER A CONTROL REGISTER
D	TBCR	TIMER B CONTROL REGISTER
E	TCDCR	TIMERS C AND D CONTROL REGISTERS
F	TADR	TIMER A DATA REGISTER
10	TBDR	TIMER B DATA REGISTER
11	TCDR	TIMER C DATA REGISTER
12	TDDR	TIMER D DATA REGISTER
13	SCR	SYNC CHARACTER REGISTER
14	UCR	USART CONTROL REGISTER
15	RSR	RECEIVER STATUS REGISTER
16	TSR	TRANSMITTER STATUS REGISTER
17	UDR	USART DATA REGISTER

CLK: Clock input. Used to control accessing of the MK68901 MFP.

INTERRUPT CONTROLLER

Each individual function in the MK68901 is provided with a unique interrupt vector that is presented to the system during the interrupt acknowledge cycle. The interrupt vector returned during the interrupt acknowledge cycle is shown in Figure 4, while the vector register is shown in Figure 5.

There are 16 vector addresses generated internally by the MK68901, one for each of the 16 interrupt channels.

INTERRUPT CONTROL REGISTERS

The Interrupt Control Registers provide control of interrupt processing for all I/O facilities of the MK68901. These registers allow the programmer to enable or disable any or all of the 16 interrupts, provide masking for any interrupts, and provide access to the pending and in-service status of the interrupts. Optional End-of-Interrupt modes are available under software control. All the interrupts are prioritized as shown in Figure 6.

INTERRUPT OPERATION

The Interrupt Enable Registers enable or disable the setting of an interrupt in the Interrupt Pending Registers. A '0' in a bit of the Interrupt Enable Registers disables the interrupt for the associated channel while a '1' enables the interrupt. Once an interrupt is enabled, the occurrence of an interrupting condition on that channel will cause the corresponding bit in the Interrupt Pending Register to be set which indicates that an interrupt is pending in the MK68901. Pending interrupts are presented to the CPU in order of priority unless they have been masked off. Masking is done by clearing the bit in the Interrupt Mask Register corresponding to the channel whose interrupt is to be masked. The channel's interrupt will remain pending until the mask bit for that channel is set, at which time the interrupt for that channel will be processed in order of priority.

When an interrupt vector is generated for a pending interrupt and passed to the CPU, the bit in the Interrupt Pending Register associated with the channel generating the interrupt will be cleared. At this time, no history of the interrupt remains in the MK68901.

In order to retain historical evidence of an interrupt being serviced by the CPU, the In-Service Register may be enabled by setting the S-bit in the Vector Register. If the In-Service Register is enabled, the bit of the In-Service Register corresponding to the interrupting channel will be set when the interrupt vector is passed to the CPU. At the same time, the Interrupt Pending bit will be cleared since the interrupt is now in service. The in-service bit can be cleared by writing a zero into it.

The daisy chaining capability (by using the $\overline{IEI}$ and $\overline{IEO}$ signals) would allow a designer to configure many MK68901 MFP's in the chain. It also allows for the freedom of putting more interrupt sources at one interrupt level. The MK68901 can handle up to eight external interrupts. The individual enabling, masking, edge selection, and vectoring capability allow the MFP to be an intelligent multiplexor for MK68000 systems.

TIMERS

There are four timers on the MK68901 MFP. Two of the timers (Timer A and Timer B) are full function timers which perform the basic delay function and can also perform event counting, pulse width measurement, and waveform generation functions. The other two timers (Timer C and Timer D) are delay timers only. One or both of these timers can be used to supply the baud rate clocks for the USART.

All timers are prescaler/counter timers with a common independent clock input (XTAL1, XTAL2), and are not required to be operated from the system clock. In addition, all timers have a time-out output function that toggles each time the timer times out.

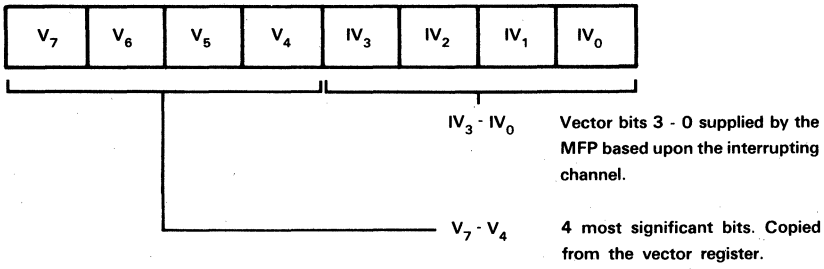
TIMER CONTROL REGISTERS

The 4 timers (A, B, C, and D) are programmed via 3 control registers and 4 timer data registers. Timers A and B are controlled by the control registers TACR and TBCR respectively (See Figure 7) and by the timer data registers TADR and TBDR. Timer C and D are controlled by the control registers TCDCR (See Figure 8) and two timer data registers TCDR and TDDR. Bits in the control registers allow the selection of operational mode, prescale, and control, while the data registers are used to read the timer or write into the time constant register. Timer A and B input pins, TAI and TBI, are used for the event and pulse width modes for timers A and B.

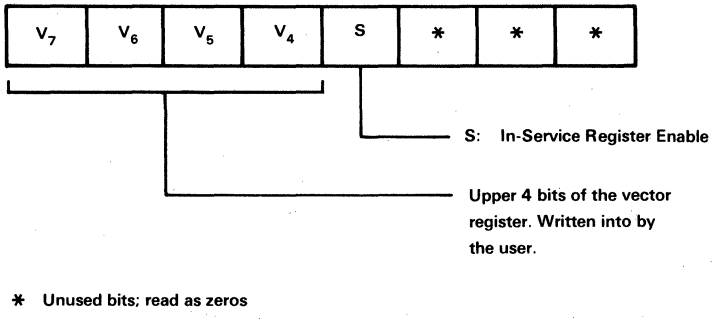
USART

Serial Communication is provided by the USART, which is capable of either asynchronous or synchronous operation. Variable word length and start/stop bit configurations are available under software control for asynchronous operation. For synchronous operation, a Sync Word is provided to establish synchronization during receive operations. The Sync Word will also be repeatedly transmitted when no other data is available for

INTERRUPT VECTOR
Figure 4



VECTOR REGISTER
Figure 5



INTERRUPT PRIORITIES

Figure 6

PRIORITY	CHANNEL	DESCRIPTION
HIGHEST	1111	General Purpose Interrupt 7(I7)
	1110	General Purpose Interrupt 6(I6)
	1101	Timer A
	1100	Receive Buffer Full
	1011	Receive Error
	1010	Transmit Buffer Empty
	1001	Transmit Error
	1000	Timer B
	0111	General Purpose Interrupt 5(I5)
	0110	General Purpose Interrupt 4(I4)
	0101	Timer C
	0100	Timer D
	0011	General Purpose Interrupt 3(I3)
	0010	General Purpose Interrupt 2(I2)
	0001	General Purpose Interrupt 1(I1)
LOWEST	0000	General Purpose Interrupt 0(I0)

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TIMERS A AND B CONTROL REGISTERS

Figure 7

*	*	*	TIMER A RESET	AC_3	AC_2	AC_1	AC_0	TACR
*	*	*	TIMER B RESET	BC_3	BC_2	BC_1	BC_0	TBCR

C_3	C_2	C_1	C_0	
0	0	0	0	Timer Stopped
0	0	0	1	Delay Mode, ÷4 Prescale
0	0	1	0	Delay Mode, ÷10 Prescale
0	0	1	1	Delay Mode, ÷16 Prescale
0	1	0	0	Delay Mode. ÷50 Prescale
0	1	0	1	Delay Mode, ÷64 Prescale
0	1	1	0	Delay Mode, ÷100 Prescale
0	1	1	1	Delay Mode, ÷200 Prescale
1	0	0	0	Event Count Mode
1	0	0	1	Pulse Width Mode, ÷4 Prescale
1	0	1	0	Pulse Width Mode, ÷10 Prescale
1	0	1	1	Pulse Width Mode, ÷16 Prescale
1	1	0	0	Pulse Width Mode, ÷50 Prescale
1	1	0	1	Pulse Width Mode, ÷64 Prescale
1	1	1	0	Pulse Width Mode, ÷100 Prescale
1	1	1	1	Pulse Width Mode, ÷200 Prescale

* Unused bits; read as zeros.

transmission. Moreover, the MK68901 allows stripping of all Sync Words received in synchronous operation. The handshake control lines $\overline{RR}$ (Receiver Ready) and $\overline{TR}$ (Transmitter Ready)allow DMA operation. Separate receive and transmit clocks are available, and separate receive and transmit status and data bytes allow independent operation of the transmit and receive sections.

USART CONTROL REGISTERS

The USART is provided with 3 control/status registers and a data register. The programmer may specify operational parameters for the USART via the Control Register, as shown in Figure 9. Status of both the Receiver and Transmitter sections is accessed by means of the 2 Status

TIMERS C AND D CONTROL REGISTER

Figure 8

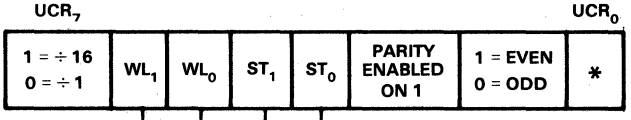
*	CC_2	CC_1	CC_0	*	DC_2	DC_1	DC_0

C_2	C_1	C_0	
0	0	0	Timer Stopped
0	0	1	Delay Mode, ÷4 Prescale
0	1	0	Delay Mode, ÷10 Prescale
0	1	1	Delay Mode, ÷16 Prescale
1	0	0	Delay Mode, ÷50 Prescale
1	0	1	Delay Mode, ÷64 Prescale
1	1	0	Delay Mode, ÷100 Prescale
1	1	1	Delay Mode, ÷200 Prescale

* Unused bits; read as zeros.

USART CONTROL REGISTER (UCR) Port C

Figure 9



Start/Stop bit control (format control)

ST_1	ST_0	Start Bits	Stop Bits	Formats
0	0	0	0	Sync
0	1	1	1	Async
*1	0	1	1½	Async
1	1	1	2	Async

*Note: ÷ 16 only

Word Length Control

WL_1	WL_0	Word Length
0	0	8 bits
0	1	7 bits
1	0	6 bits
1	1	5 bits

* Unused bits; read as zeros

RECEIVER STATUS REGISTER (RSR) Port '15'

Figure 10

RSR_7							RSR_0
BUFFER FULL	OVERRUN ERROR	PARITY ERROR	FRAME ERROR	FOUND/SEARCH OR BREAK DETECT	MATCH/CHARACTER IN PROGRESS	SYNC STRIP ENABLE	RECEIVER ENABLE

TRANSMITTER STATUS REGISTER (TSR) Port '16'

TSR_7							TSR_0
BUFFER EMPTY	UNDERRUN ERROR	AUTO TURNAROUND	END OF TRANSMISSION	BREAK	HIGH	LOW	TRANSMITTER ENABLE

H	L	Serial Output State
0	0	Hi-Z
0	1	Low ("0")
1	0	High
1	1	Loop[1]

[1] Connects transmitter output to receiver input. In loopback mode, transmitter goes high when disabled. Also connects clocks when TC given priority.

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USART DATA REGISTER (UDR) Port '17'

Figure 11

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

GENERAL PURPOSE I/O CONTROL REGISTERS

Figure 12

ACTIVE EDGE CONTROL REGISTER (AER) Port 1

1 = RISING
0 = FALLING

GPIP 7	GPIP 6	GPIP 5	GPIP 4	GPIP 3	GPIP 2	GPIP 1	GPIP 0

DATA DIRECTION REGISTER (DDR) Port 2

1 = OUTPUT
0 = INPUT

GPIP 7	GPIP 6	GPIP 5	GPIP 4	GPIP 3	GPIP 2	GPIP 1	GPIP 0

GENERAL PURPOSE I/O DATA REGISTER (GPIP) Port 0

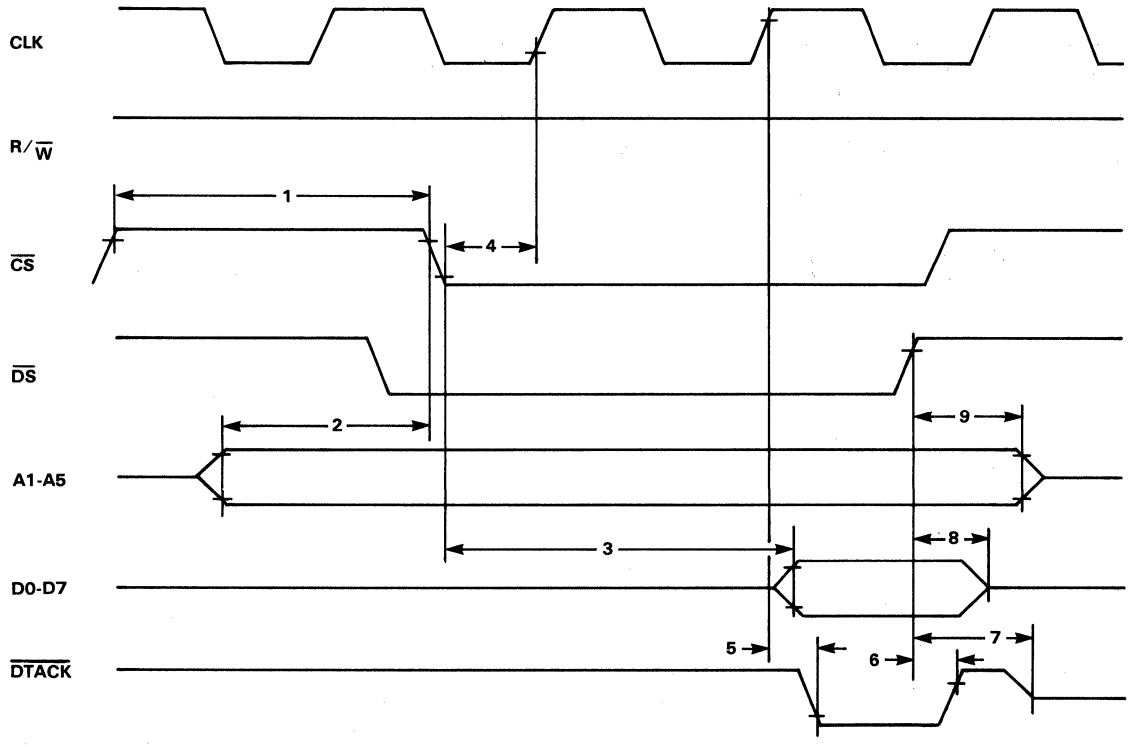
GPIP 7	GPIP 6	GPIP 5	GPIP 4	GPIP 3	GPIP 2	GPIP 1 (TR)	GPIP 0 (RR)

Registers, as shown in Figure 10. Data written to the Data Register is passed to the transmitter, while reading the data register will access data received by the USART. The USART Data Register form is illustrated in Figure 11.

ERROR CONDITIONS

Error conditions in the USART are determined by monitoring the Receive Status register (Port '15') and the Transmitter Status Register (Port '16'). These error conditions are only valid for each word boundary and are not latched. When executing block transfers of data, it is necessary to save any errors so that they can be checked at the end of a block. In order to save any error conditions during data transfer, the MFP interrupt controller may be used by enabling error interrupts (Port 4), for the desired channel (Receive error or Transmit error) and by masking these bits off (Port A). Once the transfer is complete, the Interrupt Pending Register (Port 6) can be polled to determine the presence of a pending error interrupt, and therefore an error.

READ CYCLE
Figure 13



NOTES:

1. $\overline{CS}$ High time between reads
2. Address setup for READ cycle
3. Data valid from $\overline{CS}$ if $\overline{CS}$ setup to CLK met
4. $\overline{CS}$ setup to CLK
5. $\overline{DTACK}$ delay from rising edge of CLK
6. $\overline{DS}$ or $\overline{CS}$ high to $\overline{DTACK}$ high
7. $\overline{DS}$ high to $\overline{DTACK}$ high impedance
8. $\overline{DS}$ high to Data Bus high impedance
9. Address hold time for READ cycle

GENERAL PURPOSE I/O - INTERRUPT PORT

The General Purpose I/O - Interrupt Port provides eight I/O lines that may be operated either as inputs or outputs under software control. In addition, each line may generate an interrupt on either a positive going edge or a negative going edge of the input signal.

GENERAL PURPOSE I/O CONTROL REGISTERS

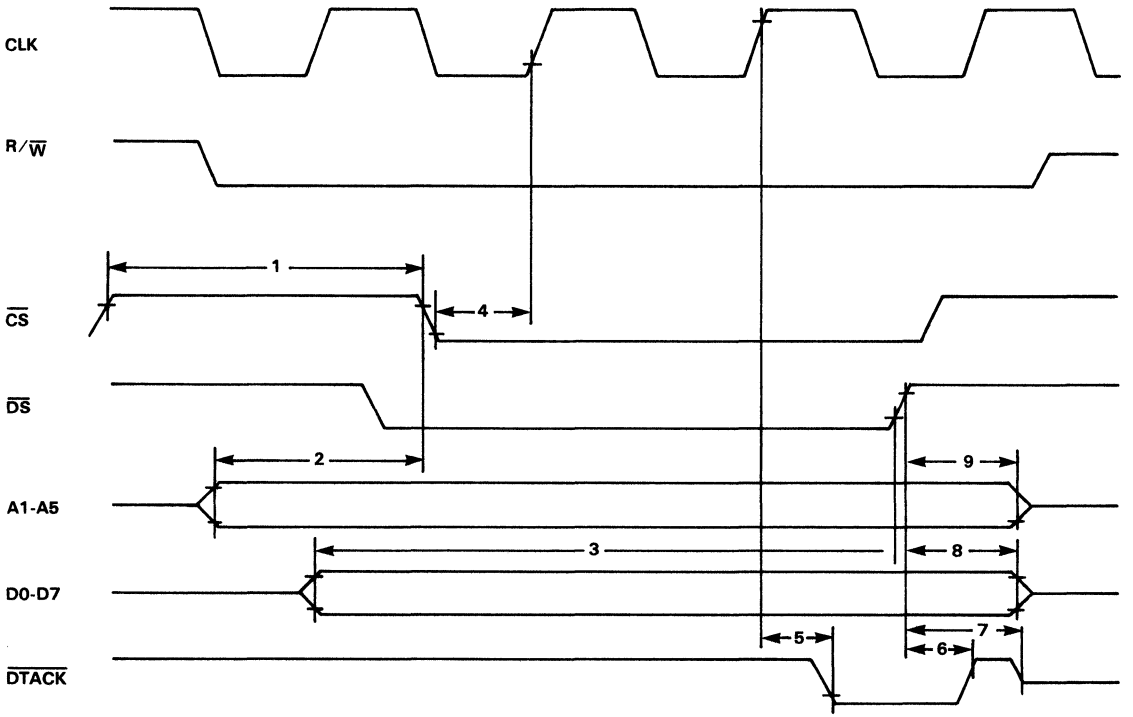
The General Purpose I/O and Interrupt Port has 3 associated registers. One allows the programmer to specify the Active Edge for each bit that will trigger the interrupt associated with that bit. The other register specifies the Data Direction (input and output) associated with each bit. The third register is the actual data I/O register used to input or output data to the port. The General Purpose I/O Control and Data Registers are illustrated in Figure 12.

REGISTER ACCESS

All register accesses are dependent on CLK. To read a register (See Figure 13), $\overline{CS}$ and $\overline{DS}$ must be asserted, and R/$\overline{W}$ must be high. The internal read control signal is essentially the combination of $\overline{CS}$, $\overline{DS}$, and R/$\overline{W}$. Thus the read operation will begin when $\overline{CS}$ and $\overline{DS}$ go active and end when either $\overline{CS}$ or $\overline{DS}$ goes inactive. The address bus must be stable prior to the start of the operation and must remain

WRITE CYCLE

Figure 14



NOTES:

1. $\overline{CS}$ High time between writes
2. Address setup time for write cycle
3. Data setup prior to end of write cycle
4. $\overline{CS}$ setup to rising edge of CLK
5. $\overline{DTACK}$ delay from rising edge of CLK
6. $\overline{DS}$ high to $\overline{DTACK}$ high
7. $\overline{DS}$ high to $\overline{DTACK}$ high impedance
8. Data hold time
9. Address hold time

stable until the end of the operation. Unless a read operation, or interrupt acknowledge cycle, is in progress, the data bus (D0-D7) will remain in the tri-state condition.

To write a register (See Figure 14), $\overline{CS}$ and $\overline{DS}$ must be asserted and R/$\overline{W}$ must be low. The MK68901 will respond by sampling the data bus and decoding the address bus for the register selected. After the MK68901 asserts $\overline{DTACK}$, the CPU negates $\overline{DS}$. At this time, the MFP latches the data bus and writes the contents into the appropriate register. Also, when $\overline{DS}$ is negated, the MFP rescinds $\overline{DTACK}$.

MOSTEK®

MICROCOMPUTER COMPONENTS

Local Area Network Controller For Ethernet

MK68590

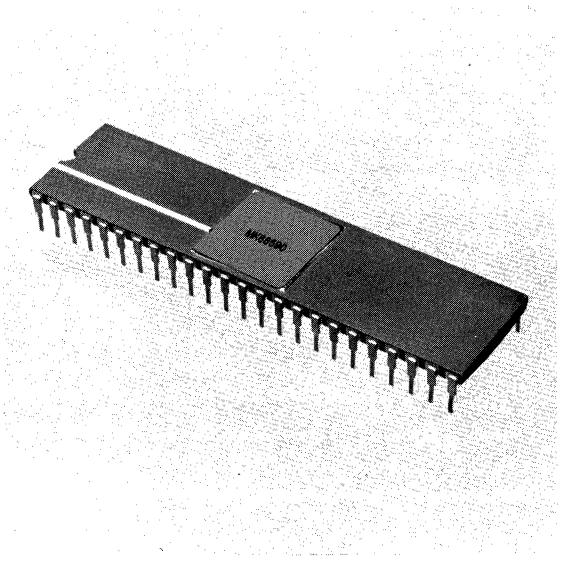
FEATURES

- ☐ 100% compatible Ethernet serial port
- ☐ Data packets moved by block transfers over a processor bus (on-board DMA controller-24 bit linear address space)
- ☐ Buffer management
- ☐ Packet framing
- ☐ Preamble and CRC insertion
- ☐ Preamble stripping and CRC checking
- ☐ General 16 bit microprocessor bus interface compatible with popular processors (68000, 8086, Z8000, LSI-11)
- ☐ Cable fault detection
- ☐ Multicast logical address filtration
- ☐ Collision handling and retry
- ☐ Scaled N-channel MOS VLSI technology
- ☐ 48 pin DIP
- ☐ Single 5 volt power supply
- ☐ Single phase TTL level clock
- ☐ All inputs and outputs TTL compatible
- ☐ Completely compatible with companion Serial Interface Adapter (SIA) chip.

INTRODUCTION

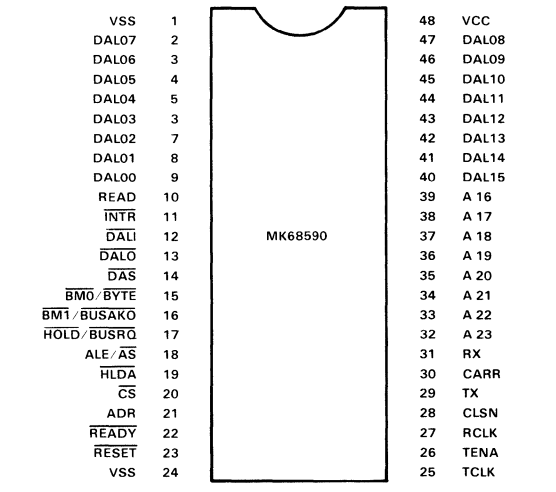
The MK68590-LANCE (Local Area Network Controller for Ethernet) is a 48 pin VLSI device designed to simplify greatly the interfacing of a microcomputer or a minicomputer to an Ethernet Local Area Network. This chip is intended to operate in a local environment that includes a closely coupled memory and microprocessor. The LANCE uses scaled N-channel MOS technology and is compatible with several microprocessors.

MK68590
Figure 1



LANCE PIN DESCRIPTION

Figure 2



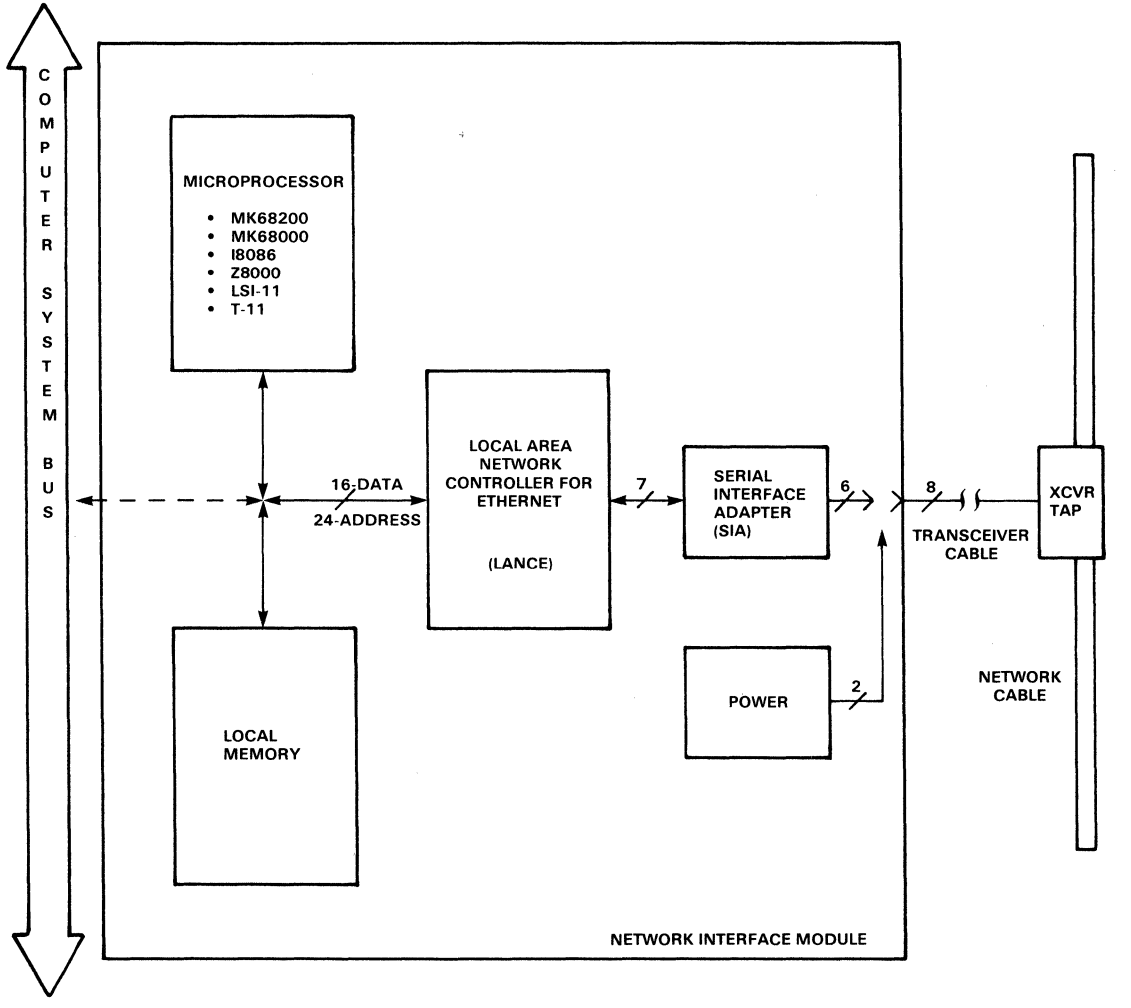
FUNCTIONAL CAPABILITIES

The Local Area Network Controller for Ethernet (LANCE) interfaces to a microprocessor bus characterized by time multiplexed address and data lines. Typically, data transfers are 16 bits wide but byte transfers occur if the buffer memory address boundaries are odd. The address bus is 24 bits wide.

The Ethernet packet format consists of a 64 bit preamble, a 48 bit destination address, a 48 bit source address, a 16 bit type field, and from a 46 to 1500 byte data field terminated with a 32-bit CRC. The variable widths of the packets accommodate both short status, command and terminal traffic packets, and long data packets to printers and disks (1024 byte disk sectors for example). Packets are spaced a minimum of 9.6 μsec apart to allow one node time enough to receive back to back packets.

The LANCE is intended to operate in a minimal configuration that requires close coupling between local memory and a processor. The local memory provides packet buffering for the chip and serves as a communication link between the chip and the processor. During initialization, the control processor loads into LANCE the starting address of the initialization block plus the operating mode of the chip via two control registers. It is only during this initial phase that the host processor talks directly to LANCE. All further communications are handled via a DMA machine under microword control contained within the LANCE. Figure 3 is a block diagram of the LANCE and SIA device used to create an Ethernet interface for a computer system.

ETHERNET LOCAL AREA NETWORK SYSTEM BLOCK DIAGRAM
Figure 3



PIN DESCRIPTION

DAL00-DAL15 DATA/ADDRESS BUS (INPUT/OUTPUT TRI-STATE) The time multiplexed Address/Data bus. These lines will be driven as a Bus Master and as a Bus Slave.

A16-A23 HIGH ORDER ADDRESS BUS (OUTPUT TRI-STATE) The additional address bits necessary to extend the DAL lines to produce a 24 bit address. These lines will be driven as a Bus Master only.

READ (INPUT/OUTPUT TRI-STATE) Indicates the type of operation to be performed in the current bus cycle. This signal will be driven by the LANCE when it is a bus master.

LANCE as a Bus Slave:

High - Data is placed on the DAL by the chip

Low - Data is taken off the DAL by the chip

LANCE as a Bus Master:

High - Data is taken off the DAL by the chip

Low - Data is placed on the DAL by the chip

$\overline{BM0}$, $\overline{BM1}$ or BYTE, $\overline{BUSAKO}$ BYTE MASK (INPUT/OUTPUT) Pins 15 and 16 are programmable through bit (00) of CSR3 (known as BCON). Asserting $\overline{RESET}$ clears CSR3.

If BCON = 0

I/O PIN 16 = $\overline{BM\ 1}$ (OUTPUT TRI-STATE)

I/O PIN 15 = $\overline{BM\ 0}$ (OUTPUT TRI-STATE)

BM0, BM1 Byte Mask. Indicates the byte(s) of a bus transaction to be read or written. The BM lines are ignored as a Bus Slave and assume word transfers only. The LANCE drives the BM lines only as a Bus Master. Byte selection is done as outlined in the following table:

$\overline{BM\ 1}$	$\overline{BM\ 0}$	
LOW	LOW	Whole Word
LOW	HIGH	Upper byte
HIGH	LOW	Lower byte
HIGH	HIGH	None

If BCON = 1

I/O PIN 16 = $\overline{BUSAKO}$ (OUTPUT)

I/O PIN 15 = BYTE (OUTPUT TRI-STATE)

BYTE An alternate byte selection line. Byte selection is done using the BYTE line and DAL (00) line, latched during the address portion of the bus transaction. BYTE is ignored as a Bus Slave as is $\overline{BM0}$, $\overline{BM1}$. There are two modes of ordering bytes depending on bit (02) of CSR 3, (known as BSWP). This programmable ordering of upper and lower bytes when using BYTE and DAL (00) as selection signals is required to make the ordering compatible with the various 16 bit microprocessors.

BSWP = 0		BSWP = 1		
LOW	LOW	LOW	LOW	Whole Word
LOW	HIGH	LOW	HIGH	Illegal Condition
HIGH	HIGH	HIGH	LOW	Upper Byte
HIGH	LOW	HIGH	HIGH	Lower Byte

$\overline{BUSAKO}$ The DMA daisy chain output

$\overline{CS}$ CHIP SELECT (INPUT). Indicates, when asserted, that the LANCE is the slave device of the data transfer. $\overline{CS}$ must be valid throughout the data portion of the bus cycle.

ADR REGISTER ADDRESS PORT SELECT (INPUT). Indicates, when $\overline{CS}$ is asserted, which of the two register ports is selected. ADR must be valid throughout the data portion of the bus cycle.

ADR

LOW Register Data Port.

HIGH Register Address Port.

ALE/$\overline{AS}$ ADDRESS LATCH ENABLE (OUTPUT TRI-STATE). Used to demultiplex the DAL lines and define the address portion of the bus cycle. This I/O pin is programmable through bit (01) of CSR3. As ALE, the signal transitions from a HIGH to a LOW during the address portion of the bus transaction and remains LOW during the entire data portion of the transaction. As $\overline{AS}$, the signal pulses LOW during the address

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portion of the bus transaction. The LANCE drives the ALE/$\overline{AS}$ line only as a Bus Master

CSR3 (01) ACON = 0

I/O PIN 31 = ALE

CSR3 (01) ACON = 1

I/O PIN 31 = $\overline{AS}$

$\overline{DAS}$ — DATA STROBE (INPUT/OUTPUT TRI-STATE). Defines the data portion of the bus transaction. $\overline{DAS}$ is driven only as a Bus Master.

$\overline{DALO}$ — DATA/ADDRESS LINE OUT (OUTPUT TRI-STATE). An external bus transceiver control line. $\overline{DALO}$ is asserted when the LANCE drives the DAL lines as a Bus Master.

$\overline{DALI}$ — DATA/ADDRESS LINE OUT (OUTPUT TRI-STATE). An external bus transceiver control line. $\overline{DALI}$ is asserted when the LANCE reads from the DAL lines as a Bus Master.

$\overline{HOLD}/\overline{BUSRQ}$ — BUS HOLD REQUEST (OUTPUT OPEN DRAIN). Asserted by the LANCE when it requires access to memory. $\overline{HOLD}$ is held LOW for the entire ensuing bus transaction. This bit is programmable through bit (00) of CSR3. Bit (00) of CSR3 is cleared when $\overline{RESET}$ is asserted.

CSR3 (00) BCON = 0
I/O PIN 17 = $\overline{HOLD}$ (OUTPUT OPEN DRAIN)
CSR3 (00) BCON = 1
I/O PIN 17 = $\overline{BUSRQ}$ (OUTPUT OPEN DRAIN)
$\overline{BUSRQ}$ will be asserted only if I/O PIN 17 is high prior to assertion.

$\overline{HLDA}$ — BUS HOLD ACKNOWLEDGE (INPUT). A response to $\overline{HOLD}$ indicating that the LANCE is the Bus Master. $\overline{HLDA}$ stops its response when $\overline{HOLD}$ ends its assertion.

$\overline{INTR}$ — INTERRUPT (OUTPUT OPEN DRAIN). An attention signal that indicates, when enabled, that one or more of the following events have occurred: a message reception or transmission has completed or an error has occurred during the transaction; the initialization procedure has completed, or a memory error has been encountered. $\overline{INTR}$ is enabled by programming register (CSR0).

RX — RECEIVE (INPUT). Receive Input Bit Stream.

TX — TRANSMIT (OUTPUT). Transmit Output Bit Stream.

TENA — TRANSMIT ENABLE (OUTPUT). Transmit Output Bit Stream Enable. A level asserted with the transmit output bit stream, TX, to enable the external transmit logic.

RCLK — RECEIVE CLOCK (INPUT). Normally a 10 MHz square wave synchronized to the Receive data and only present while receiving an input bit stream.

CLSN — COLLISION (INPUT). A logical input that indicates that a collision is occurring on the channel.

CARR — CARRIER (INPUT). A logical input that indicates that the presence of a carrier on the channel.

TLCK — TRANSMIT CLOCK (INPUT). Normally a freerunning 10 MHz clock.

$\overline{READY}$ — (INPUT/OUTPUT TRI-STATE). When the LANCE is a bus master, $\overline{READY}$ is an asynchronous acknowledgement from external memory that it will complete the data transfer. As a bus slave, the chip asserts $\overline{READY}$ when it has put data on the bus, or is about to take data off the bus. $\overline{READY}$ is a response to $\overline{DAS}$. $\overline{READY}$ negates after $\overline{DAS}$ negates.

$\overline{RESET}$ — (INPUT). Bus reset signal. Causes the LANCE to cease operation and enter an idle state.

VCC — Power supply pin. +5 VDC ±5%

VSS — Ground. 0 VDC

FUNCTIONAL DESCRIPTION

SERIAL DATA HANDLING

The basic operation of the chip set to provide the Ethernet interface is as follows. In the transmit mode (since there is only one transmission path, Ethernet is a half duplex system), the LANCE reads data from a transmit buffer by using Direct Memory Access (DMA) and appends the preamble, sync pattern (two ones after alternating ones and zeros in the preamble), and calculates and appends the complement of the 32-bit CRC. In the receive mode, the destination address, source address, type, data, and CRC fields are transferred to memory via DMA cycles. The CRC is calculated as the data and transmitted CRC is received. At the end of the packet, if this calculated CRC does not agree with a constant, an error bit is set and an interrupt is generated to the microprocessor. In the receive mode, packets will be accepted by the LANCE under four modes of operation. The first mode is a full comparison of the 48 bit destination address in the packet with the node address that was programmed into the LANCE during an initialization cycle. There are two types of logical address. One is a group type mask where the 48 bit address in the packet is put through a hash filter in order to map the 48 bit physical addresses into 1 of 64 logical groups. This mode can be useful if sending packets to all of one type of a device simultaneously or the network. (i.e. send a packet to all file servers or all printer servers). The second logical address is a multicast address where all nodes on the network receive the packet. The last receive mode of operation is the so called "promiscuous mode" in which a node will accept all packets on the coax regardless of their destination address.

COLLISION DETECTION AND IMPLEMENTATION

The Ethernet CSMA/CD network access algorithm is implemented completely within the LANCE. In addition to listening for a clear coax before transmitting, Ethernet handles collisions in a predetermined way. Should two transmitters attempt to seize the coax at the same time, they will collide, and the data on the coax will be garbled. During a transmission, the LANCE monitors the CLSN (collision) pin. This signal is generated by the transceiver when data on the coax gets garbled. A normal collision occurs while the preamble is being transmitted. The LANCE will continue to transmit the preamble then "jams" the network for a predetermined amount of time. This jamming ensures that all nodes have recognized the collision. The transmitting nodes then delay a random amount of time according to the "truncated binary backoff" algorithm specified in the Ethernet specification in order that the colliding nodes do not repeatedly try to access the network at the same time. Up to 16 attempts to access the network are made by the LANCE before it will report back an error due to excessive collisions.

Extensive error reporting is provided by the LANCE through a microprocessor interrupt and error bits in a status register. The following are the significant error conditions: CRC error on received data; transmitter on longer than was needed to send the data; missed packet error (meaning a packet on the coax was missed because there were no empty buffers in memory), and memory error, in which the memory did not respond (handshake) to a memory cycle request.

BUFFER MANAGEMENT

A key feature of the LANCE and its on board DMA channel is the flexibility and speed of communication between the LANCE and the host microprocessor through common memory locations. The basic organization of the buffer management is a circular queue of tasks in memory called descriptor rings, as shown in Figure 4. There are separate descriptor rings to describe transmit and receive operations. Up to 128 tasks may be queued up on a descriptor ring awaiting execution by the LANCE. Each entry in a descriptor ring holds a pointer to a data memory buffer and an entry for the length of the data buffer. Data buffers can be chained or cascaded in order to handle a long packet in multiple data buffer areas. The LANCE searches the descriptor rings in a "look ahead manner" to determine the next empty buffer in order to chain buffers together or to handle back to back packets. As each buffer is filled, an "own" bit is reset, signaling the host processor to empty this buffer.

MICROPROCESSOR INTERFACE

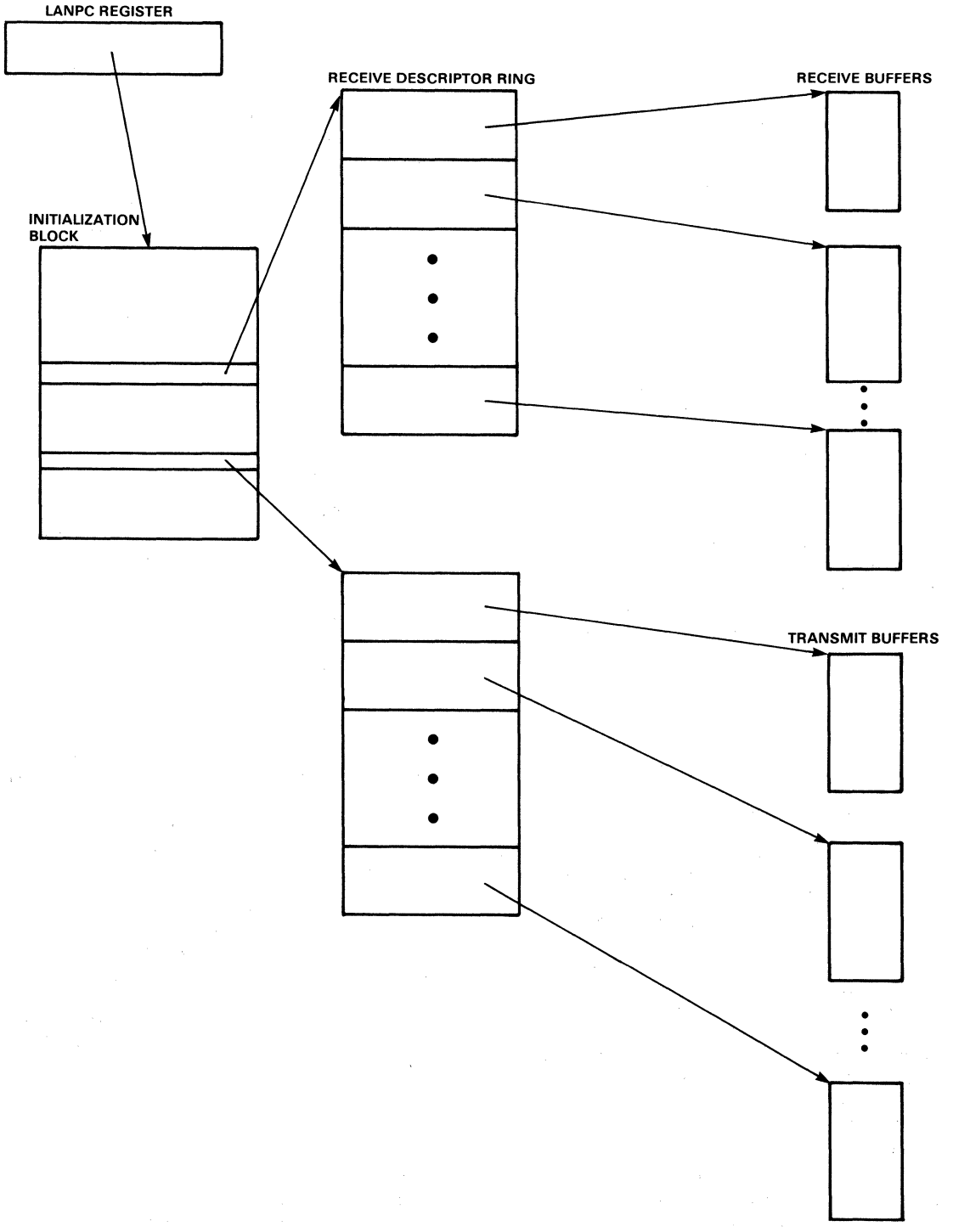
The parallel interface of the LANCE has been designed to be "friendly" or easy to interface to a variety of popular 16-bit microprocessors. These microprocessors include the following: 68000, Z8000, 8086, LSI-11, T-11, and MK68200. (The MK68200 is a 16-bit single chip microcomputer under development at Mostek with an architecture modeled after the 68000). The LANCE has a wide 24-bit linear address space when it is in the Bus Master Mode, allowing it to DMA directly into the entire address space of the above microprocessors. No segmentation or paging methods are used within the LANCE, and as such the addressing is closest to that used by the 68000 but is compatible with the others. When the LANCE is a bus master, a programmable mode of operation allows byte addressing either by employing a Byte/Word control signal, much like that used on the 8086 or the Z8000, or by using an Upper Data Strobe/Lower Data Strobe much like that used on the 68000, LSI-11 and MK68200 microprocessors. A programmable polarity on the Address Strobe signal eliminates the need for external logic. The LANCE interfaces with both multiplexed and demultiplexed data busses and features control signals for address/data bus transceivers,

Interrupts to the microprocessor are generated by the LANCE upon completion of its initialization routine, the reception of a packet, the transmission of a packet, transmitter timeout error, a missed packet, and memory error.

The cause of the interrupt is ascertained by reading CSR0. Bit (06) of CSR0, INEA, enables or disables interrupts to the microprocessor. In a polling mode, BIT (07) of CSR0 is sampled to determine when an interrupt causing condition occurred.

LANCE MEMORY MANAGEMENT

Figure 4



LANCE INTERFACE DESCRIPTION

All data transfers from the LANCE in the Bus Master mode are timed by ALE, $\overline{DAS}$ and $\overline{READY}$. The automatic adjustment of the LANCE cycle by the $\overline{READY}$ signal allows synchronization with variable cycle time memory due either to memory refresh or to dual port access. Bus cycles are a minimum of 600 nsec in length and can be increased in 100 nsec increments.

READ SEQUENCE

At the beginning of a read cycle, valid addresses are placed on DAL00-DAL15 and A16-A21. The BYTE Mask signals ($\overline{BM0}$ and $\overline{BM1}$) become valid at the beginning of this cycle as does READ, indicating the type of cycle. The trailing edge of ALE or $\overline{AS}$ is used to strobe in the addresses A0-A15 into the external latches. Approximately a hundred nanoseconds later, DAL00-DAL15 go into a tristate mode. There is a fifty nanosecond delay to allow for transceiver turnaround, then $\overline{DAS}$ falls low to signal the beginning of the data portion of the cycle. At this point in the cycle, the LANCE stalls waiting for the memory device to assert $\overline{READY}$. Upon assertion of $\overline{READY}$, $\overline{DAS}$ makes a transition from a zero to a one, latching memory data. ($\overline{DAS}$ is low for a minimum of 200 nsec).

The bus transceiver controls, $\overline{DALI}$ and $\overline{DALO}$, are used to control the bus transceivers. $\overline{DALI}$ signals to strobe data toward the LANCE and $\overline{DALO}$ signals to strobe data or addresses away from the LANCE. During a read cycle, $\overline{DALO}$ goes inactive before $\overline{DALI}$ goes active to avoid the "spiking" of the bus transceivers.

WRITE SEQUENCE

The write cycle begins exactly like a read cycle with the READ line remaining inactive. After ALE or $\overline{AS}$ pulse, the DAL00-DAL15 change from addresses to data. $\overline{DAS}$ goes active when the DAL00-DAL15 lines are stable. This data will remain valid on the bus until the memory device asserts $\overline{READY}$. At this point $\overline{DAS}$ goes inactive latching data into the memory device. Data is held for seventy five nanoseconds after the deassertion of $\overline{DAS}$.

LANCE INTERFACE DESCRIPTION — BUS SLAVE MODE

The LANCE enters the Bus Slave Mode whenever $\overline{CS}$ becomes active. This mode must be entered whenever writing or reading the four status control registers (CSR0, CSR1, CSR2, and CSR3) and the register address pointer (RAP). RAP and CSR0 may be read or written to at any time, but the LANCE must be stopped for CSR1, CSR2, and CSR3 to be written to.

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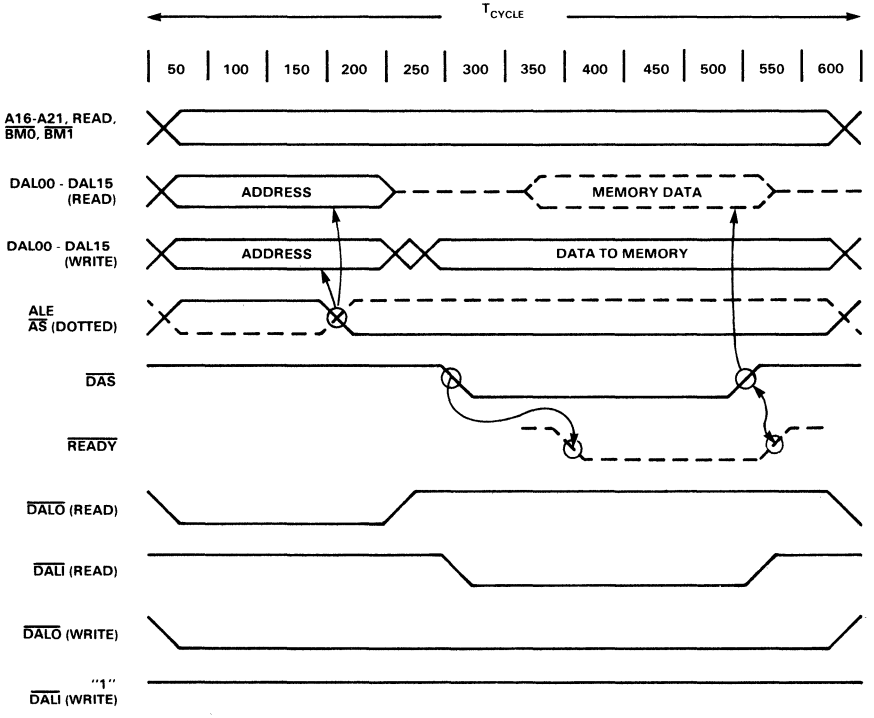
BUS MASTER TIMING

Figure 5



ADVANCE INFORMATION

MOSTEK®

MICROCOMPUTER COMPONENTS

Serial Interface Adapter

MK3891

FEATURES

- 100% compatible with companion LANCE chip and Ethernet specification
- Manchester data encoding
- Manchester data decoding with a Phase Lock Loop (PLL)
- Receive Squelch circuitry
- Collision Squelch circuitry
- Differential TRANSMIT transceiver cable drivers
- TTL compatible input to 20 MHz oscillator eliminates need for a separate crystal for SIA (ie. share uP's crystal).
- Bipolar VLSI technology
- Single 5 volt power supply
- 20 MHz crystal oscillator which generates 10 MHz LANCE clock inputs
- All LANCE signals TTL compatible
- All transceiver signals compatible with Ethernet specifications

VI

INTRODUCTION

The MK3891-SIA (Serial Interface Adapter) is a VLSI device designed to simplify greatly the interfacing of a microcomputer or minicomputer to an Ethernet Local Area Network. The SIA is a companion device to the LANCE (Local Area Network Controller for Ethernet) Ethernet Protocol Controller. The SIA and LANCE chips are intended to operate in an environment that includes a closely coupled memory and microprocessor. The SIA is compatible with the transceiver input specifications detailed in the September 30, 1980 (Rev. 1.0) specification entitled "The Ethernet - A Local Area Network - Data Link Layer and Physical Layer Specification".

FUNCTIONAL CAPABILITIES

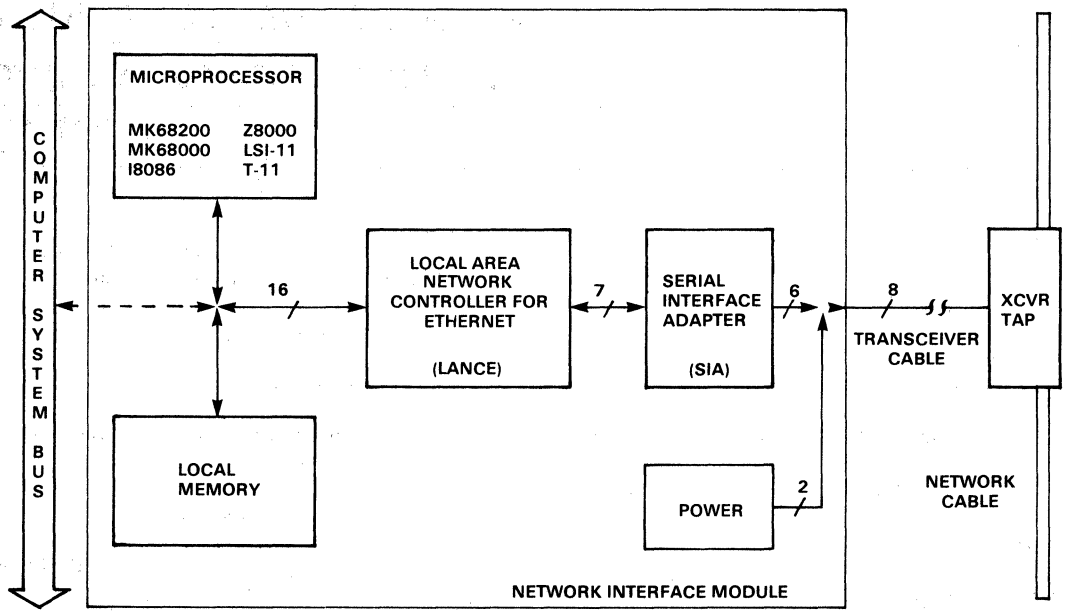
The Serial Interface Adapter (SIA) interfaces the LANCE Ethernet protocol controller with a standard Ethernet Transceiver cable as specified in the Ethernet Specification. Seven interface signals between the LANCE and the SIA chips can be wired pin to pin, while the six transceiver cable signals can be connected directly to the 15 pin D Transceiver connector. This relationship is described in Figure 1.

Figure 2 details a block diagram of the SIA. The Crystal Oscillator is controlled by a 20 MHz external crystal or can accept a 20 MHz TTL signal. A 10 MHz symmetric signal is created to drive the Manchester Encoder and to provide a TRANSMIT CLOCK for the LANCE. The Manchester Encoder takes the TRANSMIT DATA and TRANSMIT ENABLE signals from the LANCE and creates the Manchester encoded differential signals TRANSMIT + and TRANSMIT – to drive the Transceiver interface.

A collision on the Ethernet cable will be sensed by the Transceiver, and it will create the differential signals COLLISION PRESENCE + and COLLISION PRESENCE – which are received and signal conditioned to produce a TTL signal COLLISION for the LANCE. Likewise when data is on the Ethernet coax, the Transceiver will create the differential signals RECEIVE + and RECEIVE –. These inputs to the SIA are decoded by the PLL phase locked loop which synchronizes to the Ethernet Preamble and recovers clock and data from the Manchester Encoded cable signals. These two signals are supplied to the LANCE as TTL signals RECEIVE DATA and RECEIVE CLOCK. In addition, the SIA creates the signal CARRIER PRESENT while it is receiving data from the cable to indicate to the LANCE that receive data and clock are valid and available.

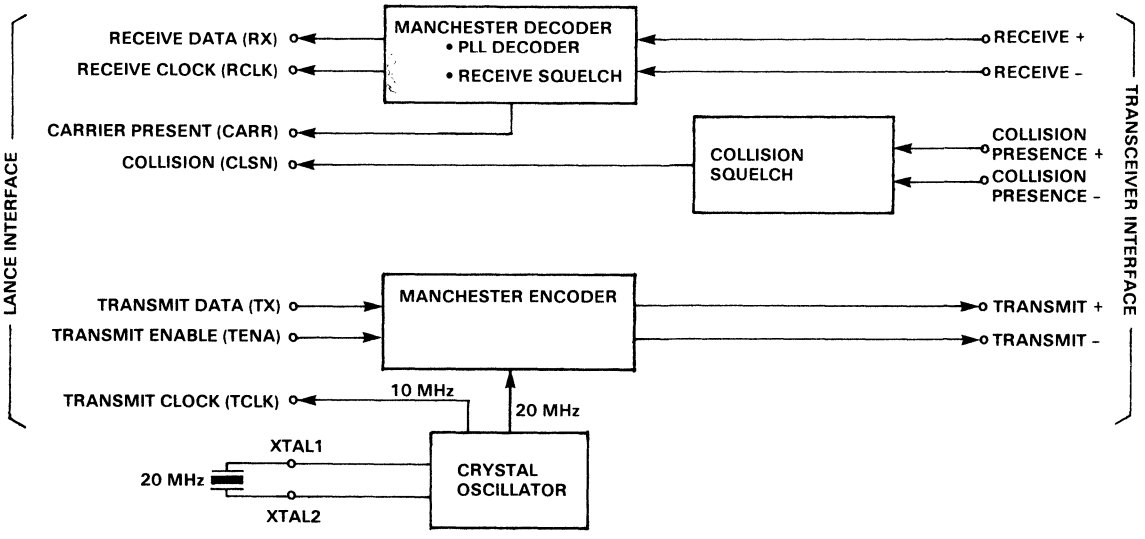
ETHERNET LOCAL AREA NETWORK SYSTEM BLOCK DIAGRAM

Figure 1



SERIAL INTERFACE ADAPTER (SIA) BLOCK DIAGRAM

Figure 2



VI

1982/1983 MICROELECTRONIC DATA BOOK

MOSTEK®

Z80 MICROCOMPUTER

Central Processing Unit

MK3880

FEATURES

- The Z80 is fully software compatible with the 8080A CPU. The 78 instructions of the 8080A are a subset of the Z80's 158 instructions.
- The extensive instruction set includes relative and indexed addressing, block searches and block transfers, word, byte, and bit data operations.
- The architecture provides duplicate sets of general purpose Flag and Index registers to allow background/foreground programming and easier single level interrupt processing and to facilitate array and table processing.
- On chip Dynamic memory refresh counter
- Single +5 V supply
- Single phase system clock
- Vectored interrupt handling system. This system allows for a Daisy Chain arrangement of a priority interrupt scheme with little if any additional hardware.

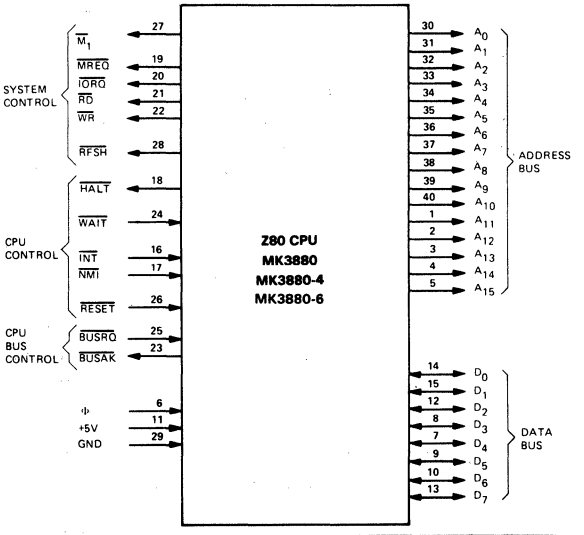
INTRODUCTION

The Mostek Z80 family of components is a significant advancement in the state-of-the-art of microcomputers. These components can be configured with any type of standard semiconductor memory to generate computer systems with an extremely wide range of capabilities. For example, as few as two LSI circuits and three standard TTL MSI packages can be combined to form a simple controller. With additional memory and I/O devices, a computer can be constructed with capabilities that only a minicomputer could previously deliver. This wide range of computational power allows standard modules to be constructed by a user that can satisfy the requirements of an extremely wide range of applications.

The Z80 Central Processing Unit is the heart of the Z80 family. It provides arithmetic and bus control to operate with the bussed peripheral controllers such as the Parallel I/O, Serial I/O, Counter/Timer, and Direct Memory Access Circuits. The Z80-CPU utilizes N channel silicon gate depletion load technology and is packaged in a 40 pin DIP.

Z80 PIN CONFIGURATION

Figure 1



Z80-CPU PIN DESCRIPTION

The Z80-CPU is packaged in an industry-standard 40 pin Dual In-Line Package. The I/O pins are shown in Figure 1, and the function of each is described below.

A_0-A_{15} (Address Bus)

Tri-state output, active high. A_0-A_{15} constitute a 16-bit address bus. The address bus provides the address for memory (up to 64K bytes), data exchanges, and for I/O device data exchanges. I/O addressing uses the 8 lower address bits to allow the user to select up to 256 input or 256 output ports directly. A_0 is the least significant address bit. During refresh time, the lower 7 bits contain a valid refresh address.

D_0-D_7 (Data Bus)

Tri-state input/output, active high. D_0-D_7 constitute an 8-bit bidirectional data bus. The data bus is used for data exchanges with memory and I/O devices.

VII

$\overline{M_1}$ (Machine Cycle one)

Output, active low, $\overline{M_1}$ indicates that the current machine cycle is the OP code fetch cycle of an instruction execution. Note that during execution of 2-byte op-codes, $\overline{M_1}$ is generated as each op code byte is fetched. These two byte op-codes always begin with CBH, DDH, EDH, or FDH. $\overline{M_1}$ also occurs with $\overline{IORQ}$ to indicate an interrupt acknowledge cycle.

$\overline{MREQ}$ (Memory Request)

Tri-state output, active low. The memory request signal indicates that the address bus holds a valid address for a memory read or memory write operation.

$\overline{IORQ}$ (Input/Output Request)

Tri-state output, active low. The $\overline{IORQ}$ signal indicates that the lower half of the address bus holds a valid I/O address for an I/O read or write operation. An $\overline{IORQ}$ signal is also generated with an $\overline{M_1}$ signal when an interrupt is being acknowledged to indicate that an interrupt response vector can be placed on the data bus. Interrupt Acknowledge operations occur during $\overline{M_1}$ time while I/O operations never occur during $\overline{M_1}$ time.

$\overline{RD}$ (Memory Read)

Tri-state output, active low. $\overline{RD}$ indicates that the CPU wants to read data from memory or an I/O device. The addressed I/O device or memory should use this signal to gate data onto the CPU data bus.

$\overline{WR}$ (Memory Write)

Tri-state output, active low. $\overline{WR}$ indicates that the CPU data bus holds valid data to be stored in the addressed memory or I/O device.

$\overline{RFSH}$ (Refresh)

Output, active low. $\overline{RFSH}$ indicates that the lower 7 bits of the address bus contain a refresh address for dynamic memories and current $\overline{MREQ}$ signal should be used to do a refresh read to all dynamic memories. A_7 is a logic zero and the upper 8 bits of the Address Bus contain the I Register.

$\overline{HALT}$ (Halt state)

Output, active low. $\overline{HALT}$ indicates that the CPU has executed a $\overline{HALT}$ software instruction and is awaiting either a non maskable or a maskable interrupt (with the mask enabled) before operation can resume. While halted, the CPU executes NOP's to maintain memory refresh activity.

$\overline{WAIT}$* (Wait)

Output, active low. $\overline{WAIT}$ indicates to the Z80-CPU that the addressed memory or I/O devices are not ready for a data transfer. The CPU continues to enter wait states for as long as this signal is active. This signal allows memory or I/O devices of any speed to be synchronized to the CPU.

$\overline{INT}$ (Interrupt Request)

Input, active low. The Interrupt Request signal is generated by I/O devices. A request will be honored at the end of the current instruction if the internal software controlled interrupt enable flip-flop (IFF) is enabled and if the $\overline{BUSRQ}$ signal is not active. When the CPU accepts the interrupt, an acknowledge signal ($\overline{IORQ}$ during M_1 time) is sent out at the beginning of the next instruction cycle. The CPU can respond to an interrupt in three different modes that are described in detail in section 8 of the Technical Manual, which is included in section IV of this data book.

$\overline{NMI}$

Input, negative edge triggered. The non maskable interrupt request line has a higher priority than $\overline{INT}$ and is always recognized at the end of the current instruction, independent of the status of the interrupt enable flip-flop. $\overline{NMI}$ automatically forces the Z80-CPU to restart to location 0066_H. The program counter is automatically saved in the external stack so that the user can return to the program that was interrupted. Note that continuous WAIT cycles can prevent the current instruction from ending, and that a $\overline{BUSRQ}$ will override an $\overline{NMI}$.

RESET

Input, active low. $\overline{RESET}$ forces the program counter to zero and initializes the CPU. The CPU initialization will:

1) Disable the interrupt enable flip-flop
2) Set Register I = 00H
3) Set Register R = 00H
4) Set Interrupt Mode 0

During reset time, the address bus and data bus go to a high impedance state and all control output signals go to the inactive state. No refresh occurs.

$\overline{BUSRQ}$ (Bus Request)

Input, active low. The bus request signal is used to request the CPU address bus, data bus and tri-state output control signals to go to a high impedance state so that other devices can control buses to a high impedance state as soon as

the current CPU machine cycle is terminated.

$\overline{\text{BUSAK}}$* Output, active low. Bus acknowledge is used to indicate to the requesting device that the CPU address bus, data bus and tri-state control bus signals have been set to their high impedance state and the external device can now control these signals.

Φ Single phase system clock.

*While the Z80-CPU is in either a $\overline{\text{WAIT}}$ state or a Bus Acknowledge condition, Dynamic Memory Refresh will not occur.

For further details on this device, please consult the MK3880 Z80 CPU Technical Manual, included in Section IV.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... Specified Operating Range
Storage Temperature ..... -65°C to +150°C
Voltage on Any Pin with Respect to Ground ..... -0.3 V to +7V
Power Dissipation ..... 1.5 W

All ac parameters assume a load capacitance of 50 pF max.

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = 5 V ± 5% unless otherwise specified

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
V_{ILC}	Clock Input Low Voltage	-0.3		0.8	V	
V_{IHC}	Clock Input High Voltage	V_{CC}-.6		V_{CC}+.3	V	
V_{IL}	Input Low Voltage	-0.3		0.8	V	
V_{IH}	Input High Voltage	2.0		V_{CC}	V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 1.8 mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = -250 μA
I_{CC}	Power Supply Current			150*	mA	
I_{LI}	Input Leakage Current			±10	μA	V_{IN} = 0 to V_{CC}
I_{LO}	Tri-State Output Leakage Current in Float			±10	μA	V_{OUT} = 0.4 V to V_{CC}

*200 mA for -4, -10 or -20 devices

CAPACITANCE

T_A = 25°C, f = 1 MHz unmeasured pins returned to ground

SYMBOL	PARAMETER	MAX	UNIT
CΦ	Clock Capacitance	35	pF
C_{IN}	Input Capacitance	5	pF
C_{OUT}	Output Capacitance	10	pF

AC CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = +5 V ± 5%, Unless Otherwise Noted

SIGNAL	SYMBOL	PARAMETER	3880 MIN (ns)	3880 MAX (ns)	3880-4 MIN (ns)	3880-4 MAX (ns)	3880-6 MIN (ns)	3880-6 MAX (ns)
Φ	t_c	Clock Period	400	[12]	250	[12]	165	[12]
	$t_{w(\Phi H)}$	Clock Pulse Width, Clock High	180	(D)	110	(D)	65	(D)
	$t_{w(\Phi L)}$	Clock Pulse Width, Clock Low	180	2000	110	2000	65	2000
	$t_{r,f}$	Clock Rise and Fall Time		30		30		20
A_{0-15}	$t_{D(AD)}$	Address Output Delay		145		110		90
	$t_{F(AD)}$	Delay to Float		110		90		80
	t_{acm}	Address Stable Prior to $\overline{MREQ}$ (Memory Cycle)	[1]		[13]		[24]	
	t_{aci}	Address Stable Prior to $\overline{IORQ}$, $\overline{RD}$ or $\overline{WR}$ (I/O Cycle)	[2]		[14]		[25]	
	t_{ca}	Address Stable From $\overline{RD}$, $\overline{WR}$, $\overline{IORQ}$ or $\overline{MREQ}$	[3]		[15]		[26]	
	t_{caf}	Address Stable From $\overline{RD}$ or $\overline{WR}$ During Float	[4]		[16]		[27]	
D_{0-7}	$t_{D(D)}$	Data Output Delay		230		150		130
	$t_{F(D)}$	Delay to Float During Write Cycle		90		90		80
	$t_{S\Phi(D)}$	Data Setup Time to Rising Edge of Clock During M1 Cycle	50		35		30	
	$t_{S\overline{\Phi}(D)}$	Data Setup Time to Falling Edge at Clock During M2 to M5	60		50		40	
	t_{dcm}	Data Stable Prior to $\overline{WR}$ (Memory Cycle)	[5]		[17]		[28]	
	t_{dci}	Data Stable Prior to $\overline{WR}$ (I/O Cycle)	[6]		[18]		[29]	
	t_{cdf}	Data Stable from $\overline{WR}$	[7]		[19]		[30]	
	t_H	Input Hold Time	0		0		0	
$\overline{MREQ}$	$t_{DL\overline{\Phi}(MR)}$	$\overline{MREQ}$ Delay From Falling Edge of Clock, $\overline{MREQ}$ Low	20	100	20	85	20	70
	$t_{DH\Phi(MR)}$	$\overline{MREQ}$ Delay From Rising Edge of Clock, $\overline{MREQ}$ High		100		85		70
	$t_{DH\overline{\Phi}(MR)}$	$\overline{MREQ}$ Delay From Falling Edge of Clock, $\overline{MREQ}$ High		100		85		70
	$t_{w(\overline{MRL})}$	Pulse Width, $\overline{MREQ}$ Low	[8]		[20]		[20]	
	$t_{w(\overline{MRH})}$	Pulse Width, $\overline{MREQ}$ High	[9]		[21]		[21]	
$\overline{IORQ}$	$t_{DL\Phi(IR)}$	$\overline{IORQ}$ Delay From Rising Edge of Clock, $\overline{IORQ}$ Low		90		75		65
	$t_{DL\overline{\Phi}(IR)}$	$\overline{IORQ}$ Delay From Falling Edge of Clock, $\overline{IORQ}$ Low		110		85		70
	$t_{DH\Phi(IR)}$	$\overline{IORQ}$ Delay From Rising Edge of Clock, $\overline{IORQ}$ High		100		85		70
	$t_{DH\overline{\Phi}(IR)}$	$\overline{IORQ}$ Delay From Falling Edge of Clock $\overline{IORQ}$ High		110		85		70
$\overline{RD}$	$t_{DL\Phi(RD)}$	$\overline{RD}$ Delay From Rising Edge of Clock, $\overline{RD}$ Low		100		85		70
	$t_{DL\overline{\Phi}(RD)}$	$\overline{RD}$ Delay From Falling Edge of Clock, $\overline{RD}$ Low		130		95		80
	$t_{DH\Phi(RD)}$	$\overline{RD}$ Delay From Rising Edge of Clock, $\overline{RD}$ High	15	100	15	85	15	70
	$t_{DH\overline{\Phi}(BD)}$	$\overline{RD}$ Delay From Falling Edge of Clock, $\overline{RD}$ High		110		85		70
$\overline{WR}$	$t_{DL\Phi(WR)}$	$\overline{WR}$ Delay From Rising Edge of Clock, $\overline{WR}$ Low		80		65		60
	$t_{DL\overline{\Phi}(WR)}$	$\overline{WR}$ Delay From Falling Edge of Clock, $\overline{WR}$ Low		90		80		70
	$t_{DH\overline{\Phi}(WR)}$	$\overline{WR}$ Delay From Falling Edge of Clock, $\overline{WR}$ High		100		80		70
	$t_{w(\overline{WRL})}$	Pulse Width, $\overline{WR}$ Low	[10]		[22]		[22]	

NOTES:

A. Data should be enabled onto the CPU data bus when RD is active. During interrupt acknowledge data should be enabled when $\overline{M1}$ and $\overline{IORQ}$ are both active.

B. The $\overline{RESET}$ signal must be active for a minimum of 3 clock cycles. [Cont'd. on next page].

SIGNAL	SYMBOL	PARAMETER	3880 MIN (ns)	3880 MAX (ns)	3880-4 MIN (ns)	3880-4 MAX (ns)	3880-6 MIN (ns)	3880-6 MAX (ns)
$\overline{M1}$	$t_{DL(M1)}$	$\overline{M1}$ Delay From Rising Edge of Clock M1 Low		130		100		80
	$t_{DH(M1)}$	$\overline{M1}$ Delay From Rising Edge of Clock M1 High		130		100		80
$\overline{RFSH}$	$t_{DL(RF)}$	$\overline{RFSH}$ Delay From Rising Edge of Clock, $\overline{RFSH}$ Low		180		130		110
	$t_{DH(RF)}$	$\overline{RFSH}$ Delay From Rising Edge of Clock, $\overline{RFSH}$ High		150		120		100
$\overline{WAIT}$	$t_{S(WT)}$	$\overline{WAIT}$ Setup Time to Falling Edge of Clock	70		70		60	
$\overline{HALT}$	$t_{D(HT)}$	$\overline{HALT}$ Delay Time From Falling Edge of Clock		300		300		260
$\overline{INT}$	$t_{s(IT)}$	$\overline{INT}$ Setup Time to Rising Edge of Clock	80		80		70	
$\overline{NMI}$	$t_{w(NMI)}$	Pulse Width, $\overline{NMI}$ Low	80		80		70	
$\overline{BUSRQ}$	$t_{S(BQ)}$	$\overline{BUSRQ}$ Setup Time to Rising Edge of Clock	80		50		50	
$\overline{BUSAK}$	$t_{DL(BA)}$	$\overline{BUSAK}$ Delay From Rising Edge of Clock, $\overline{BUSAK}$ Low		120		100		90
	$t_{DH(BA)}$	$\overline{BUSAK}$ Delay From Falling Edge of Clock, $\overline{BUSAK}$ High		110		100		90
$\overline{RESET}$	$t_{S(RS)}$	$\overline{RESET}$ Setup Time to Rising Edge of Clock	90		60		60	
	$t_{F(C)}$	Delay to/from Float ($\overline{MREQ}$, $\overline{IORQ}$, $\overline{RD}$ and $\overline{WR}$)		100		80		70
	t_{mr}	$\overline{M1}$ Stable Prior to $\overline{IORQ}$ (Interrupt Ack.)	[11]		[23]		[31]	

[1] $t_{ACM} = t_w(\Phi H) + t_f - 75$

[2] $t_{aci} = t_c - 80$

[3] $t_{CA} = t_w(\Phi L) + t_r - 40$

[4] $t_{caf} = t_w(\Phi L) + t_r - 60$

[5] $t_{dcm} = t_C - 210$

[6] $t_{dci} = t_w(\Phi L) + t_r - 210$

[7] $t_{cdf} = t_w(\Phi L) + t_r - 80$

[8] $t_w(MRL) = t_c - 40$

[9] $t_w(MRH) = t_w(\Phi H) + t_f - 30$

[10] $t_w(WR) = t_c - 40$

[11] $t_{mr} = 2\,t_c + t_w(\Phi H) + t_f - 80$

[12] $t_c = t_w(\Phi H) + t_w(\Phi L) + t_r + t_f$

[13] $t_{acm} = t_w(\phi H) + t_f - 65$

[14] $t_{aci} = t_c - 70$

[15] $t_{ca} = t_w(\Phi L) + t_r - 50$

[16] $t_{caf} = t_w(\Phi L) + t_r - 45$

[17] $t_{dcm} = t_c - 170$

[18] $t_{dci} = t_w(\Phi L) + t_r - 170$

[19] $t_{cdf} = t_w(\Phi L) + t_r - 70$

[20] $t_w(\overline{MRL}) = t_c - 30$

[21] $t_w(\overline{MRH}) = t_w(\Phi H) + t_f - 20$

[22] $t_w(\overline{WR}) = t_c - 30$

[23] $t_{mr} = 2t_c + t_w(\Phi H) + t_f - 65$

[24] $t_{ACM} = t_w(\Phi H) + t_f - 50$

[25] $t_{aci} = t_c - 55$

[26] $t_{CA} = t_w(\Phi L) + t_r - 50$

[27] $t_{caf} = t_w(\Phi L) + t_r - 45$

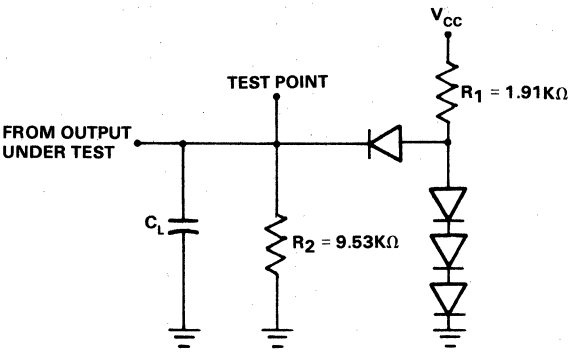
[28] $t_{dcm} = t_C - 140$

[29] $t_{dci} = t_w(\Phi L) + t_r - 140$

[30] $t_{cdf} = t_w(\Phi L) + t_r - 55$

[31] $t_{mr} = 2t_c + t_w(\Phi H) + t_f - 50$

LOAD CIRCUIT FOR OUTPUT



NOTES (Cont'd.)

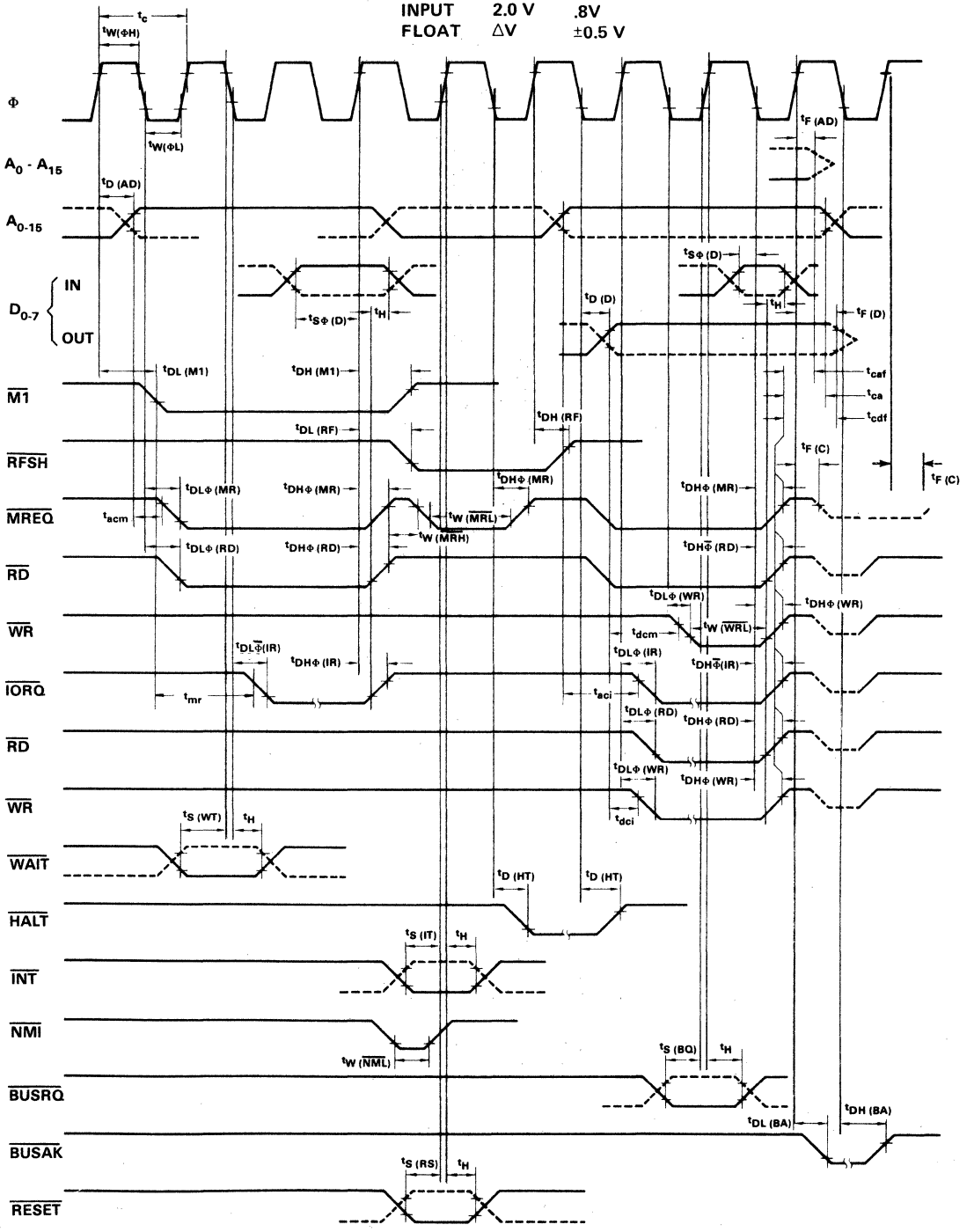
C. Output Delay vs. Load Capacitance
$T_A = 70°C$ $V_{CC} = 5\ V \pm 5\%$
Add 10 nsec delay for each 50 pF increase in load up to a maximum of 200 pF for the data bus and 100 pF for address and control lines.

D. Although static by design, testing guarantees t_w (ΦH) of 200 μsec maximum.

A.C. TIMING DIAGRAM

Timing measurements are made at the following voltages, unless otherwise specified:

	"1"	"0"
CLOCK	V_{CC}−.6	.8V
OUTPUT	2.0 V	.8V
INPUT	2.0 V	.8V
FLOAT	ΔV	±0.5 V



VII

ORDERING INFORMATION

PART NO.	PACKAGE TYPE	MAX CLOCK FREQUENCY	TEMPERATURE RANGE
MK3880N Z80-CPU	Plastic	2.5 MHz	0° to + 70°C
MK3880P Z80-CPU	Ceramic	2.5 MHz	
MK3880N-4 Z80-CPU	Plastic	4.0 MHz	
MK3880P-4 Z80-CPU	Ceramic	4.0 MHz	
MK3880P-10 Z80-CPU	Ceramic	2.5 MHz	–40°C to +85°C

MOSTEK®

Z80 MICROCOMPUTER

Parallel I/O Controller

MK3881

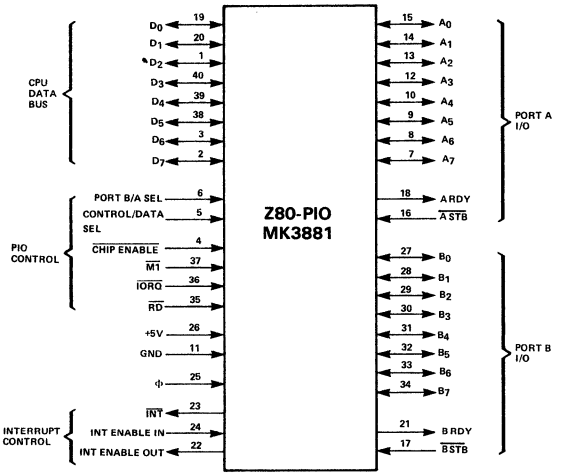
FEATURES

- Two independent 8 bit bidirectional peripheral interface ports with 'handshake' data transfer control
- Interrupt driven 'handshake' for fast response
- Any one of four distinct modes of operation may be selected for a port, including:
  - Byte output
  - Byte input
  - Byte bidirectional bus (Available on Port A only)
  - Bit control mode

  All with interrupt controlled handshake
- Daisy chain priority interrupt logic included to provide for automatic interrupt vectoring without external logic
- Eight outputs are capable of driving Darlington transistors
- All inputs and outputs fully TTL compatible
- Single 5 volt supply and single phase clock required.

PIO PIN CONFIGURATION

Figure 1



INTRODUCTION

The Z80 Parallel I/O Circuit is a programmable, two port device which provides a TTL compatible interface between peripheral devices and the Z80-CPU. The CPU can configure the Z80-PIO to interface with a wide range of peripheral devices with no other external logic required. Typical peripheral devices that are fully compatible with the Z80-PIO include most keyboard, paper tape readers and punches, printers, PROM programmers, etc. The Z80-PIO utilizes N channel silicon gate depletion load technology and is packaged in a 40 pin DIP.

One of the unique features of the Z80-PIO that separates it from other interface controllers is that all data transfer between the peripheral device and the CPU is accomplished under total interrupt control. The interrupt logic of the PIO permits full usage of the efficient interrupt capabilities of the Z80-CPU during I/O transfers. All logic necessary to implement a fully nested interrupt structure is included in the PIO so that additional circuits are not required. Another unique feature of the PIO is that it can be programmed to interrupt the CPU on the occurrence of specified status conditions in the peripheral device. For example, the PIO can be programmed to interrupt if any specified peripheral alarm conditions should occur. This interrupt capability reduces the amount of time that the processor must spend in polling peripheral status.

PIN DESCRIPTION

A diagram of the Z80-PIO pin configuration is shown in Figure 1. This section describes the function of each pin.

D_7-D_0 — Z80-CPU Data Bus (bidirectional, tristate)
This bus is used to transfer all data and commands between the Z80-CPU and the Z80-PIO. D_0 is the least significant bit of the bus.

B/$\overline{A}$ Sel — Port B or A Select (input, active high)
This pin defines which port will be accessed during a data transfer between the Z80-CPU and the Z80-PIO. A low level on this pin selects Port A while a high level selects Port B. Often Address Bit A_0 from the CPU will be used for this selection function.

C/$\overline{D}$ Sel — Control or Data Select (input, active high)
This pin defines the type of data transfer to be performed between the CPU and the PIO. A

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high level on this pin during a CPU write to the PIO causes the Z80 data bus to be interpreted as a command for the port selected by the B/A Select line. A low level on this pin means that the Z80 data bus is being used to transfer data between the CPU and the PIO. Often Address bit A_1 from the CPU will be used for this function.

$\overline{CE}$ Chip Enable (input, active low)
A low level on this pin enables the PIO to accept command or data inputs from the CPU during a write cycle or to transmit data to the CPU during a read cycle. This signal is generally a decode of four I/O port numbers that encompass port A and B, data and Control.

Φ System Clock (input)
The Z80-PIO uses the standard Z80 system clock to synchronize certain signals internally. This is a single phase clock.

$\overline{M1}$ Machine Cycle One Signal from CPU (input, active low)
This signal from the CPU is used as a sync pulse to control several internal PIO operations. When $\overline{M1}$ is active and the $\overline{RD}$ signal is active, the Z80-CPU is fetching an instruction from memory. Conversely, when $\overline{M1}$ is active and $\overline{IORQ}$ is active, the CPU is acknowledging an interrupt. In addition, the $\overline{M1}$ signal has two other functions within the Z80-PIO.

1. $\overline{M1}$ synchronizes the PIO interrupt logic.
2. When $\overline{M1}$ occurs without an active $\overline{RD}$ or $\overline{IORQ}$ signal, the PIO logic enters a reset state.

$\overline{IORQ}$ Input/Output Request from Z80-CPU (input, active low)
The $\overline{IORQ}$ signal is used in conjunction with the B/A Select, C/D Select, $\overline{CE}$, and $\overline{RD}$ signals to transfer commands and data between the Z80-CPU and the Z80-PIO. When $\overline{CE}$, $\overline{RD}$ and $\overline{IORQ}$ are active, the port addressed by B/A will transfer data to the CPU (a read operation). Conversely, when $\overline{CE}$ and $\overline{IORQ}$ are active but $\overline{RD}$ is not active, then the port addressed by B/A will be written into from the CPU with either data or control information as specified by the C/D Select signal. Also, if $\overline{IORQ}$ and $\overline{M1}$ are active simultaneously, the CPU is acknowledging an interrupt and the interrupting port will automatically place its interrupt vector on the CPU data bus if it is the highest device requesting an interrupt.

$\overline{RD}$ Read Cycle Status from the Z80-CPU (input, active low)
If $\overline{RD}$ is active a MEMORY READ or I/O READ operation is in progress. The $\overline{RD}$ signal is used with B/A Select, C/D Select, $\overline{CE}$ and $\overline{IORQ}$ signals to transfer data from the Z80-PIO to the Z80-CPU.

IEI Interrupt Enable In (input, active high)
This signal is used to form a priority interrupt daisy chain when more than one interrupt driven device is being used. A high level on this pin indicates that no other devices of higher priority are being serviced by a CPU interrupt service routine.

IEO Interrupt Enable Out (output, active high)
The IEO signal is the other signal required to form a daisy chain priority scheme. It is high only if IEI is high and the CPU is not servicing an interrupt from this PIO. Thus this signal blocks lower priority devices from interrupting while a higher priority device is being serviced by its CPU interrupt service routine.

$\overline{INT}$ Interrupt Request (output, open drain, active low)
When INT is active the Z80-PIO is requesting an interrupt from the Z80-CPU.

A_0-A_7 Port A Bus (bidirectional, tri-state)
This 8 bit bus is used to transfer data and/or status or control information between Port A of the Z80-PIO and a peripheral device. A_0 is the least significant bit of the Port A data bus.

$\overline{A\ STB}$ Port A Strobe Pulse from peripheral Device (input, active low)
The meaning of this signal depends on the mode of operation selected for Port A as follows:

1) Output mode: The positive edge of this strobe is issued by the peripheral to acknowledge the receipt of data made available by the PIO.

2) Input mode: The strobe is issued by the peripheral to load data from the peripheral into the Port A input register. Data is loaded into the PIO when this signal is active.

3) Bidirectional mode: When this signal is active, data from the Port A output register is gated onto Port A bidirectional data bus. The positive edge of the strobe acknowledges the receipt of the data.

4) Control mode: The strobe is inhibited internally.

A RDY — Register A Ready (output, active high)
The meaning of this signal depends on the mode of operation selected for Port A as follows:

1) Output mode: This signal goes active to indicate that the Port A output register has been loaded and the peripheral data bus is stable and ready for transfer to the peripheral device.

2) Input mode: This signal is active when the Port A input register is empty and is ready to accept data from the peripheral device.

3) Bidirectional mode: This signal is active when data is available in Port A output register for transfer to the peripheral device. In this mode data is not placed on the Port A data bus unless $\overline{\text{A STB}}$ is active.

4) Control mode: This signal is disabled and forced to a low state.

B_0 - B_7 — Port B (bidirectional, tristate)
This 8 bit bus is used to transfer data and/or status or control information between Port B of the PIO and a peripheral device. The Port B data bus is capable of supplying 1.5 ma@ 1.5 V to drive Darlington transistors. B_0 is the least significant bit of the bus.

$\overline{\text{B STB}}$ — Port B Strobe Pulse from Peripheral Device (input, active low)
The meaning of this signal is similar to that of $\overline{\text{A STB}}$ with the following exception:

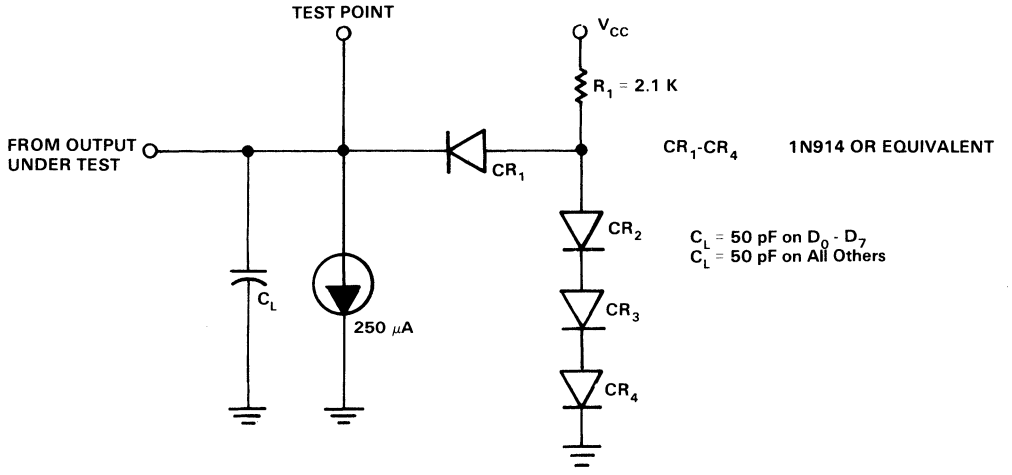
In the Port A bidirectional mode this signal strobes data from the peripheral device into the Port A input register.

B RDY — Register B Ready (output, active high)
The meaning of this signal is similar to that of A Ready with the following exception:

In the Port A bidirectional mode this signal is high when the Port A input register is empty and ready to accept data from the peripheral device.

OUTPUT LOAD CIRCUIT

Figure 2



For further details on this device, please consult the PIO MK3881 Technical Manual, included in Section IV.

ELECTRICAL SPECIFICATIONS

MK3881

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... Specified operating range
Storage Temperature ..... -65°C to +150°C
Voltage On Any Pin With Respect To Ground ..... -0.3 V to +7 V
Power Dissipation ..... .6 W

All ac parameters assume a load capacitance of 100 pF max. Timing references between two output signals assume a load difference of 50 pF max.

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = 5 V ± 5% unless otherwise specified

SYMBOL	PARAMETER	MIN	MAX	UNIT	TEST CONDITION
V_{ILC}	Clock Input Low Voltage	-0.3	0.80	V	
V_{IHC}	Clock Input High Voltage	V_{CC} -.6	V_{CC} +.3	V	
V_{IL}	Input Low Voltage	-0.3	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC}	V	
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 2.0 mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = -250 μA
I_{CC}	Power Supply Current		70*	mA	
I_{LI}	Input Leakage Current		±10	μA	V_{IN} = 0 to V_{CC}
I_{LOH}	Tri-State Output Leakage Current in Float		10	μA	V_{OUT} = 2.4 to V_{CC}
I_{LOL}	Tri-State Output Leakage Current in Float		-10	μA	V_{OUT} = 0.4 V
I_{LD}	Data Bus Leakage Current in Input Mode		±10	μA	$0 \leq V_{IN} \leq V_{CC}$
I_{OHD}	Darlington Drive Current	-1.5		mA	V_{OH} = 1.5 V Port B Only

*150 mA for -4, -10, and -20 devices.

CAPACITANCE

T_A = 25°C, f = 1 MHz

SYMBOL	PARAMETER	MAX	UNIT	TEST CONDITION
C_Φ	Clock Capacitance	10	pF	Unmeasured Pins
C_{IN}	Input Capacitance	5	pF	Returned to Ground
C_{OUT}	Output Capacitance	10	pF	

A.C. CHARACTERISTICS MK3881, MK3881-10, MK3881-20, Z80-PIO

T_A = 0°C to 70°C, V_{CC} = +5 V ± 5%, unless otherwise noted

SIGNAL	SYMBOL	PARAMETER	3881		3881-4		UNIT
			MIN	MAX	MIN	MAX	
Φ	t_c	Clock Period	400	[1]	250	[1]	nsec
	$t_{W(\Phi H)}$	Clock Pulse Width, Clock High	170	2000	105	2000	nsec
	$t_{W(\Phi L)}$	Clock Pulse Width, Clock Low	170	2000	105	2000	nsec
	t_r, t_f	Clock Rise and Fall Times		30		30	nsec
	t_h	Any Hold Time for Specified Set-Up Time	0		0		nsec
C/D SEL $\overline{CE}$ ETC.	$t_{S\Phi(CS)}$	Control Signal Set-up Time to Rising Edge of Φ During Read or Write Cycle	50		50		nsec
D_0 - D_7	$t_{DR(D)}$	Data Output Delay from Falling Edge of RD		430		380	nsec
	$t_{S\Phi(D)}$	Data Set-up Time to Rising Edge of Φ During Write or $\overline{M1}$ Cycle	50		50		nsec
	$t_{DI(D)}$	Data Output Delay from Falling Edge of $\overline{IORQ}$ During $\overline{INTA}$ Cycle		340		250	nsec
	$t_{F(D)}$	Delay to Floating Bus (Output Buffer Disable Time)		160		110	nsec
IEI	$t_{S(IEI)}$	IEI Set-Up Time to Falling Edge of $\overline{IORQ}$ During $\overline{INTA}$ cycle	140		140		nsec
IEO	$t_{DH(IO)}$	IEO Delay Time from Rising Edge of IEI		210		160	nsec
	$t_{DL(IO)}$	IEO Delay Time from Falling Edge of IEI		190		130	nsec
	$t_{DM(IO)}$	IEO Delay from Falling Edge of M1 (Interrupt Occurring Just Prior to M1) See Note A.		300		190	nsec
$\overline{IORQ}$	$t_{S\Phi(IR)}$	$\overline{IORQ}$ Set-Up Time to Rising Edge of Φ During Read or Write Cycle	250		115		nsec
$\overline{M1}$	$t_{S\Phi(M1)}$	$\overline{M1}$ Set-Up Time to Rising Edge of Φ During $\overline{INTA}$ or $\overline{M1}$ Cycle. See Note B.	210		90		nsec
$\overline{RD}$	$t_{S\Phi(RD)}$	$\overline{RD}$ Set-Up Time to Rising Edge of Φ During Read or $\overline{M1}$ Cycle	240		115		nsec
A_0 - A_7 B_0 - B_7	$t_{S(PD)}$	Port Data Set-Up Time to Rising Edge of $\overline{STROBE}$ (Mode 1)	260		230		nsec
	$t_{DS(PD)}$	Port Data Output Delay from Falling Edge of $\overline{STROBE}$ (Mode 2)		230		210	nsec
	$t_{F(PD)}$	Delay to Floating Port Data Bus from Rising Edge of $\overline{STROBE}$ (Mode 2)		200		180	nsec
	$t_{DI(PD)}$	Port Data Stable from Rising Edge of $\overline{IORQ}$ During $\overline{WR}$ Cycle (Mode 0)		200		180	nsec
$\overline{ASTB}$ $\overline{BSTB}$	$t_{W(ST)}$	Pulse Width, $\overline{STROBE}$	150 [4]		150 [4]		nsec nsec
$\overline{INT}$	$t_{D(IT)}$	$\overline{INT}$ Delay Time from Rising Edge of $\overline{STROBE}$		490		440	nsec
	$t_{D(IT3)}$	$\overline{INT}$ Delay Time from Data Match During Mode 3 Operation		420		380	nsec
ARDY	$t_{DH(RY)}$	Ready Response Time from Rising Edge of $\overline{IORQ}$		t_c+460		t_c+410	nsec
BRDY	$t_{DL(RY)}$	Ready Response Time from Rising Edge of $\overline{STROBE}$		t_c+ 400		t_c+ 360	nsec

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A. $2.5\,t_c > (N-2)t_{DL(IO)} + t_{DM(IO)} + t_{S(IEI)}$ + TTL Buffer Delay, if any.

B. $\overline{M1}$ must be active for a minimum of 2 clock periods to reset the PIO.

[1] $t_c = t_{W(\Phi H)} + t_{W(\Phi L)} + t_r + t_f$

[2] Increase $t_{DR(D)}$ by 10 nsec for each 50 pF increase in loading up to 200 pF max.

[3] Increase $t_{DI(D)}$ by 10 nsec for each 50 pF increase in loading up to 200 pF max.

[4] For Mode 2: $t_{W(ST)} > t_{S(PD)}$

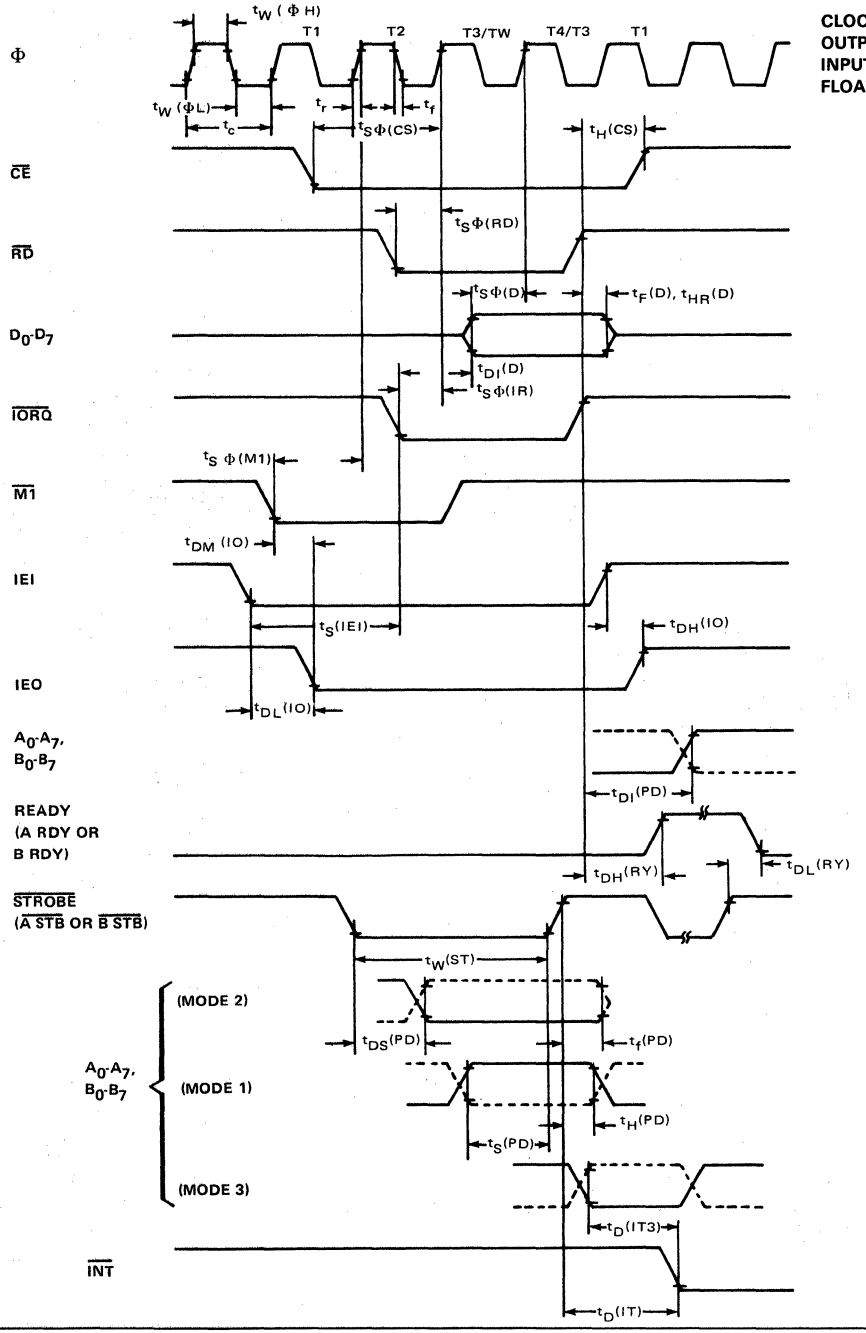
[5] Increase these values by 2 nsec for each 10 pF increase in loading up to 100 pF max.

TIMING DIAGRAM

Figure 3

Timing measurements are made at the following voltages, unless otherwise specified:

	"1"		"0"
CLOCK	4.2 V		0.8 V
OUTPUT	2.0 V		0.8 V
INPUT	2.0 V		0.8 V
FLOAT	Δ V	=	0.5 V



ORDERING INFORMATION

PART NO.	DESIGNATOR	PACKAGE TYPE	MAX CLOCK FREQUENCY	TEMPERATURE RANGE
MK3881N	Z80-PIO	Plastic	2.5 MHz	
MK3881P	Z80-PIO	Ceramic	2.5 MHz	
MK3881N-4	Z80A-PIO	Plastic	4.0 MHz	0° to 70°C
MK3881P-4	Z80A-PIO	Ceramic	4.0 MHz	
MK3881P-10	Z80-PIO	Ceramic	4.0 MHz	-40° to +85°C

Counter Timer Circuit
MK3882

FEATURES

- All inputs and outputs fully TTL compatible
- Each channel may be selected to operate in either Counter Mode or Timer Mode
- Used in either mode, a CPU-readable Down Counter indicates number of counts-to-go until zero
- A Time Constant Register can automatically reload the Down Counter at Count Zero in Counter and Timer Mode
- Selectable positive or negative trigger initiates time operation in Timer Mode. The same input is monitored for event counts in Counter Mode.
- Three channels have Zero Count/Timeout outputs capable of driving Darlington transistors
- Interrupts may be programmed to occur on the zero count condition in any channel
- Daisy chain priority interrupt logic included to provide for automatic interrupt vectoring without external logic

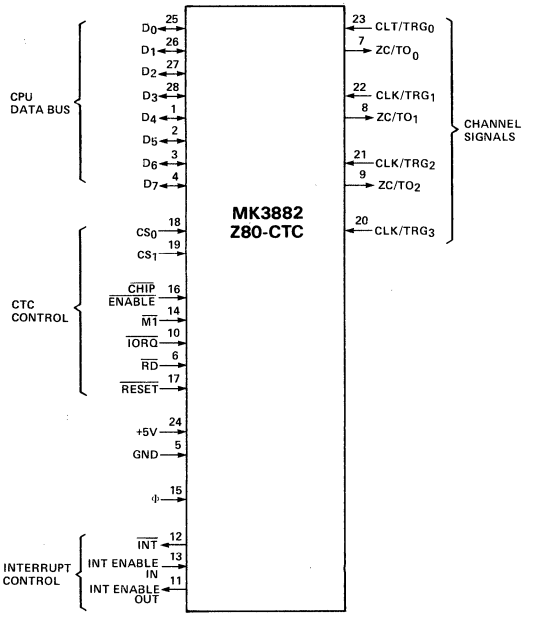
INTRODUCTION

The Z80-Counter Timer Circuit (CTC) is a programmable component with four independent channels that provide counting and timing functions for microcomputer systems based on the Z80-CPU. The CPU can configure the CTC channels to operate under various modes and conditions as required to interface with a wide range of devices. In most applications, little or no external logic is required. The Z80-CTC utilizes N-channel silicon gate depletion load technology and is packaged in a 28-pin DIP. The Z80-CTC requires only a single 5 volt supply and a one-phase 5 volt clock.

CTC PIN DESCRIPTION

A diagram of the Z80-CTC pin configuration is shown in Figure 1. This section describes the function of each pin.

Z80-CTC PIN CONFIGURATION
Figure 1



D_7-D_0 Z80-CPU Data Bus (bidirectional, tristate)
This bus is used to transfer all data and command words between the Z80-CPU and the Z80-CTC. There are 8 bits on this bus, of which D_0 is the least significant.

CS1-CS0 Channel Select (input, active high)
These pins form a 2-bit binary address code for selecting one of the four independent CTC channels for an I/O Write or Read (See truth table below.)

	CS1	CS0
Ch0	0	0
Ch1	0	1
Ch2	1	0
Ch3	1	1

$\overline{CE}$ Chip Enable (input, active low)
A low level on this pin enables the CTC to accept control words, Interrupt Vectors, or time constant data words from the Z80 Data

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Bus during an I/O Write cycle, or to transmit the contents of the Down Counter to the CPU during an I/O Read cycle. In most applications this signal is decoded from the 8 least significant bits of the address bus for any of the four I/O port addresses that are mapped to the four Counter/Timer Channels.

Clock (Φ) — System Clock (input)
This single-phase clock is used by the CTC to synchronize certain signals internally.

$\overline{M1}$ — Machine Cycle One Signal from CPU (input, active low)
When $\overline{M1}$ is active and the $\overline{RD}$ signal is active, the CPU is fetching an instruction from memory. When $\overline{M1}$ is active and $\overline{IORQ}$ is active, the CPU is acknowledging an interrupt, alerting the CTC to place an Interrupt Vector on the Z80 Data Bus if it has daisy chain priority and one of its channels has requested an interrupt.

$\overline{IORQ}$ — Input/Output Request from CPU (input, active low)
The $\overline{IORQ}$ signal is used in conjunction with the $\overline{CE}$ and $\overline{RD}$ signals to transfer data and Channel Control Words between the Z80-CPU and the CTC. During a CTC Write Cycle, $\overline{IORQ}$ and $\overline{CE}$ must be true and $\overline{RD}$ false. The CTC does not receive a specific write signal, instead generating its own internally from the inverse of a valid $\overline{RD}$ signal. In a CTC Read Cycle, $\overline{IORQ}$, $\overline{CE}$ and $\overline{RD}$ must be active to place the contents of the Down Counter on the Z80 Data Bus. If $\overline{IORQ}$ and $\overline{M1}$ are both true, the CPU is acknowledging an interrupt request, and the highest-priority interrupting channel will place its Interrupt Vector on the Z80 Data Bus.

$\overline{RD}$ — Read Cycle Status from the CPU (input, active low)
The $\overline{RD}$ signal is used in conjunction with the $\overline{IORQ}$ and $\overline{CE}$ signals to transfer data and Channel Control Words between the Z80-CPU and the CTC. During a CTC Write Cycle, $\overline{IORQ}$ and $\overline{CE}$ must be true and $\overline{RD}$ false. The CTC does not receive a specific write signal, instead generating its own internally from the inverse of a valid $\overline{RD}$ signal. In a CTC Read Cycle, $\overline{IORQ}$, $\overline{CE}$ and $\overline{RD}$ must be active to place the contents of the Down Counter on the Z80 Data Bus.

IEI — Interrupt Enable In (input, active high)
This signal is used to help form a system-wide interrupt daisy chain which establishes priorities when more than one peripheral device in the system has interrupting capability. A high level on this pin indicates that no other interrupting devices of higher priority are being serviced by the Z80-CPU.

IEO — Interrupt Enable Out (output, active high)
The IEO signal, in conjunction with IEI, is used to form a system-wide interrupt priority daisy chain. IEO is high only if IEI is high and the CPU is not servicing an interrupt from any CTC channel. Thus this signal blocks lower priority devices from interrupting while a higher priority device is being serviced by the CPU.

$\overline{INT}$ — Interrupt Request (output, open drain, active low)
This signal goes true when any CTC channel which has been programmed to enable interrupts has a zero-count condition in its Down Counter.

$\overline{RESET}$ — Reset (input, active low)
This signal stops all channels from counting and resets channel interrupt enable bits in all control registers, thereby disabling CTC-generated interrupts. The ZC/TO and $\overline{INT}$ outputs go to their inactive states, IEO reflects IEI, and the CTC's data bus output drivers go to the high impedance state.

CLK/TRG3-CLK/TRG0 — External Clock/Timer Trigger (input, user-selectable active high or low)
There are four CLK/TRG pins, corresponding to the four independent CTC channels. In the Counter Mode, every active edge on this pin decrements the Down Counter. In the Timer Mode, an active edge on this pin initiates the timing function. The user may select the active edge to be either rising or falling.

ZC/TO2—ZC/TO0 — Zero Count/Timeout (output, active high)
There are three ZC/TO pins, corresponding to CTC channels 2 through 0. (Due to package pin limitations channel 3 has no ZC/TO pin.) In either Counter Mode or Timer Mode, when the Down Counter decrements to zero an active high going pulse appears at this pin.

For further details on this device, please consult the CTC MK3882 Technical Manual, included in Section IV.

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... Specified operating range
Storage Temperature ..... -65°C to +150°C
Voltage On Any Pin With Respect To Ground ..... -0.3 V to +7 V
Power Dissipation ..... 0.8 W

All ac parameters assume a load capacitance of 100 pF max. Timing references between two output signals assume a load difference of 50 pF max.

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = 5 V ± 5% unless otherwise specified

SYMBOL	PARAMETER	MIN	MAX	UNIT	TEST CONDITION
V_{ILC}	Clock Input Low Voltage	-0.3	0.80	V	
V_{IHC}	Clock Input High Voltage (1)	V_{CC} -.6	V_{CC} +.3	V	
V_{IL}	Input Low Voltage	-0.3	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC}	V	
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 2 mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = -250 μA
I_{CC}	Power Supply Current		120	mA	T_C = 400 nsec**
I_{LI}	Input Leakage Current		±10	μA	V_{IN} = 0 to V_{CC}
I_{LOH}	Tri-State Output Leakage Current in Float		10	μA	V_{OUT} = 2.4 to V_{CC}
I_{LOL}	Tri-State Output Leakage Current in Float		-10	μA	V_{OUT} = 0.4 V
I_{OHD}	Darlington Drive Current	-1.5		mA	V_{OH} = 1.5 V

**T_C = 250 nsec for MK3882-4

CAPACITANCE

T_A = 25°C, f = 1 MHz

SYMBOL	PARAMETER	MAX	UNIT	TEST CONDITION
C_Φ	Clock Capacitance	20	pF	Unmeasured Pins
C_{IN}	Input Capacitance	5	pF	Returned to Ground
C_{OUT}	Output Capacitance	10	pF	

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A.C. CHARACTERISTICS MK3882, MK3882-10, Z80-CTC

T_A = 0°C to 70°C, V_{CC} = +5 V ± 5%, unless otherwise noted

SIGNAL	SYMBOL	PARAMETER	38823882-4 MIN	38823882-4 MAX	MIN	MAX	UNIT	COMMENTS
Φ	t_C	Clock Period	400	(1)	250	(1)	ns	
	t_W (ΦH)	Clock Pulse Width, Clock High	170	2000	105	2000	ns	
	t_W(ΦL)	Clock Pulse Width, Clock Low	170	2000	105	2000		
	t_r, t_f	Clock Rise and Fall Times		30		30	ns	
	t_H	Any Hold Time for Specified Setup Time	0		0		ns	
CS, $\overline{CE}$, etc.	t_SΦ(CS)	Control Signal Setup Time to Rising Edge of Φ During Read or Write Cycle	160		145		ns	
	t_DΦ(D)	Data Output Delay from Rising Edge of Φ During Read Cycle		240		200	ns	(2)
	t_SΦ(D)	Data Setup Time to Rising Edge of Φ During Write or M1 Cycle	60		50		ns	
D_0 - D_7	t_{DI}(D)	Data Output Delay from Falling Edge of $\overline{IORQ}$ During INTA Cycle		340		160	ns	(2)
	t_F(D)	Delay to Floating Bus (Output Buffer Disable Time)		230		110	ns	
IEI	t_S(IEI)	IEI Setup Time to Falling Edge of $\overline{IORQ}$ During INTA Cycle	200		140		ns	
	t_{DH}(IO)	IEO Delay Time from Rising Edge of IEI		220		160	ns	(3)
	t_{DL}(IO)	IEO Delay Time from Falling Edge of IEI		190		130	ns	(3)
IEO	t_{DM}(IO)	IEO Delay from Falling Edge of $\overline{M1}$ (Interrupt Occurring just Prior to $\overline{M1}$)		300		190	ns	(3)
$\overline{IORQ}$	t_SΦ(IR)	$\overline{IORQ}$ Setup Time to Rising Edge of Φ During Read or Write Cycle	250		115		ns	
$\overline{M1}$	t_SΦ(M1)	$\overline{M1}$ Setup Time to Rising Edge of Φ During INTA or $\overline{M1}$ Cycle	210		90		ns	
$\overline{RD}$	t_SΦ(RD)	$\overline{RD}$ Setup Time to Rising Edge of Φ During Read or $\overline{M1}$ Cycle	240		115		ns	
$\overline{INT}$	t_DΦ(IT)	$\overline{INT}$ Delay from Rising Edge of Φ		t_C(Φ) + 200		t_C(Φ) + 140		(7)
	t_C(CK)	Clock Period	2t_C(Φ)		2t_C(Φ)			(5)
	t_r, t_f	Clock and Trigger Rise and Fall Times		50		50	ns	
	t_S(CK)	Clock Setup Time to Rising Edge of Φ for Immediate Count	210		130		ns	(5)
	t_S(TR)	Trigger Setup Time to Rising Edge of Φ for Enabling of Prescaler on Following Rising Edge of Φ	210		130		ns	(6)
CLK/ TRG_{0-3}	t_W(CTH)	Clock and Trigger High Pulse Width	200		120		ns	(7)
	t_W(CTL)	Clock and Trigger Low Pulse Width	200		120		ns	(7)

A.C. CHARACTERISTICS MK3882, MK3882-10, Z80-CTC (Cont'd)

T_A = 0°C to 70°C, V_{CC} = +5 V ± 5%, unless otherwise noted

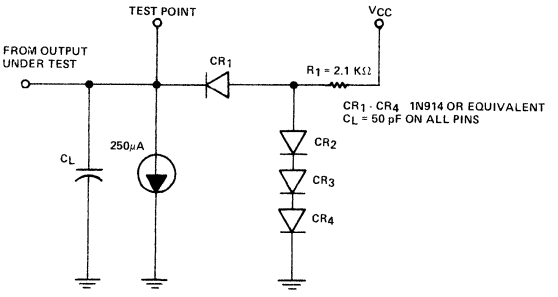
SIGNAL	SYMBOL	PARAMETER	3882 MIN	3882 MAX	3882-4 MIN	3882-4 MAX	UNIT	COMMENTS
	$t_{DH}(ZC)$	ZC/TO Delay Time from Rising Edge of Φ, ZC/TO High		190		120	ns	(7)
ZC/ TO_{0-2}	$t_{DL}(ZC)$	ZC/TO Delay Time from Falling Edge of Φ, ZC/TO Low		190		120	ns	(7)

NOTES:

1. $t_C = t_W(\Phi H) + t_W(\Phi L) + t_r + t_f$.
2. Increase delay by 10 nsec for each 50 pF increase in loading 200 pF maximum for data lines and 100 pF for control lines.
3. Increase delay by 2 nsec for each 10 pF increase in loading, 100 pF maximum.
4. $\overline{\text{RESET}}$ must be active for a minimum of 3 clock cycles.
5. Counter mode
6. Timer mode
7. Counter and Timer mode

OUTPUT LOAD CIRCUIT

Figure 2



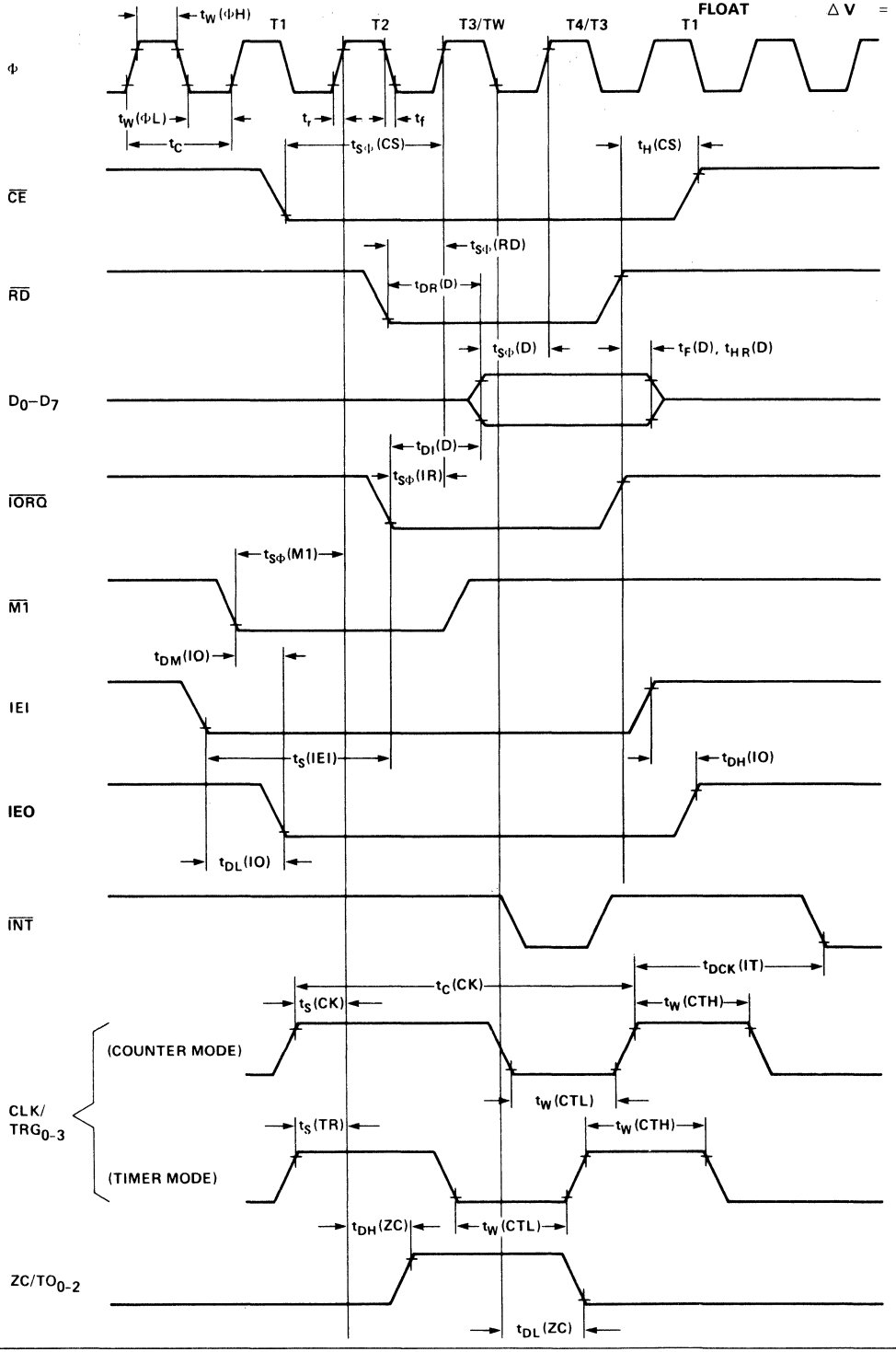
VII

TIMING DIAGRAM

Figure 3

Timing measurements are made at the following voltages, unless otherwise specified:

	"1"		"0"
CLOCK	4.2 V		0.8 V
OUTPUT	2.0 V		0.8 V
INPUT	2.0 V		0.8 V
FLOAT	Δ V	=	0.5 V



ORDERING INFORMATION

PART NO.	DESIGNATOR	PACKAGE TYPE	MAX CLOCK FREQUENCY	TEMPERATURE RANGE
MK3882N	Z80-CTC	Plastic	2.5 MHz	0° to 70°C
MK3882P	Z80-CTC	Ceramic	2.5 MHz	
MK3882N-4	Z80A-CTC	Plastic	4.0 MHz	
MK3882P-4	Z80A-CTC	Ceramic	4.0 MHz	
MK3882P-10	Z80-CTC	Ceramic	4.0 MHz	–40° to +85°C

Direct Memory Access Controller MK3883

FEATURES

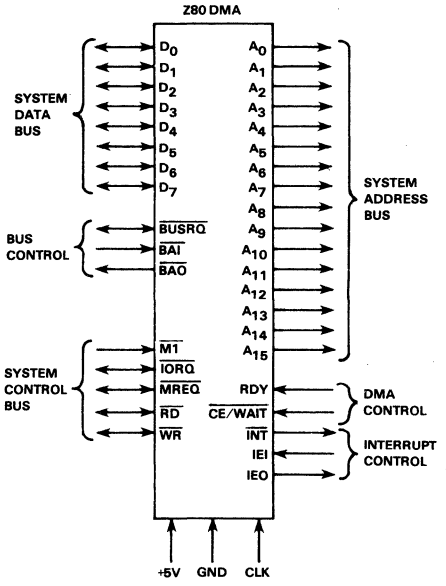
- Transfers, searches and search/transfers in byte-at-a-time, burst or continuous modes. Cycle length and edge timing can be programmed to match the speed of any port.
- Dual port addresses (source and destination) generated for memory-to-I/O, memory-to-memory, or I/O-to-I/O operations. Addresses may be fixed or automatically incremented/decremented.
- Next-operation loading without disturbing current operations via buffered starting-address registers. An entire previous sequence can be repeated automatically.
- Extensive programmability of functions. CPU can read complete channel status.
- Standard Z80 Family bus-request and prioritized interrupt-request daisy chains implemented without external logic. Sophisticated, internally modifiable interrupt vectoring.
- Direct interfacing to system buses without external logic.

GENERAL DESCRIPTION

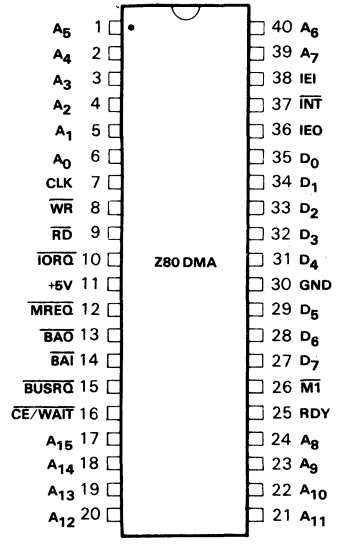
The MK3883 Z80 DMA (Direct Memory Access) is a powerful and versatile device for controlling and processing transfers of data. Its basic function of managing CPU-independent transfers between two ports is augmented by an array of features that optimize transfer speed and control with little or no external logic in systems using an 8- or 16-bit data bus and a 16-bit address bus.

VII

PIN FUNCTIONS
Figure 1



PIN ASSIGNMENTS
Figure 2



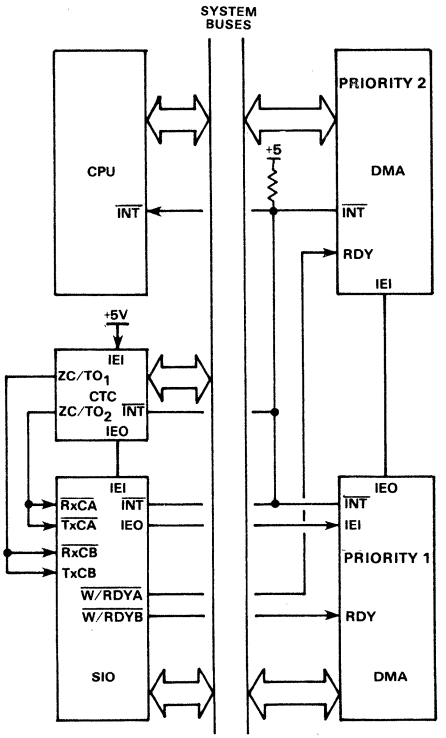
Transfers can be done between any two ports (source and destination), including memory-to-I/O, memory-to-memory, and I/O-to-I/O. Dual port addresses are automatically generated for each transaction and may be either fixed or incrementing/decrementing. In addition, bit-maskable byte searches can be performed either concurrently with transfers or as an operation in itself.

The MK3883 Z80 DMA contains direct interfacing to and independent control of system buses, as well as sophisticated bus and interrupt controls. Many programmable features, including variable cycle timing and auto-restart minimize CPU software overhead. They are especially useful in adapting this special-purpose transfer processor to a broad variety of memory, I/O and CPU environments.

The MK3883 Z80 DMA is an n-channel silicon-gate depletion-load device packaged in a 40-pin plastic, or ceramic DIP. It uses a single +5V power supply and the standard Z80 Family single-phase clock.

Z80 ENVIRONMENT WITH MULTIPLE DMA CONTROLLERS

Figure 3



FUNCTIONAL DESCRIPTION

Classes of Operation

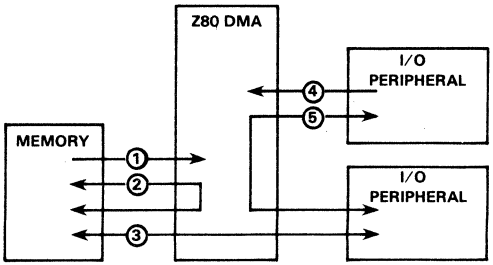
The MK3883 Z80 DMA has three basic classes of operation:

- Transfers of data between two ports (memory or I/O peripheral)
- Searches for a particular 8-bit maskable byte at a single port in memory or an I/O peripheral
- Combined transfers with simultaneous search between two ports

Figure 4 illustrates the basic functions served by these classes of operation.

BASIC FUNCTIONS OF THE Z80 DMA

Figure 4



1. Search memory
2. Transfer memory-to-memory (optional search)
3. Transfer memory-to-I/O (optional search)
4. Search I/O
5. Transfer I/O-to-I/O (optional search)

During a transfer, the DMA assumes control of the system control, address, and data buses. Data is read from one addressable port and written to the other addressable port, byte by byte. The ports may be programmed to be either system main memory or peripheral I/O devices. Thus, a block of data may be written from one peripheral to another, from one area of main memory to another, or from a peripheral to main memory and vice versa.

During a search-only operation, data is read from the source port and compared byte by byte with the DMA-internal register containing a programmable match byte. This match byte may optionally be masked so that only certain bits within the match byte are compared. Search rates up to 1.25M bytes per second can be obtained with the 2.5MHz MK3883 Z80 DMA or 2M bytes per second with the 4MHz MK3883-4 Z80 DMA.

In combined searches and transfers, data is transferred between two ports while simultaneously searching for a bit-maskable byte match.

Data transfers or searches can be programmed to stop or interrupt under various conditions. In addition, CPU-readable status bits can be programmed to reflect the condition.

Modes of Operation

The MK3883 Z80 DMA can be programmed to operate in one of three transfer and/or search modes:

- Byte-at-a-time: data operations are performed one byte at a time. Between each byte operation the system buses are released to the CPU. The buses are requested again for each succeeding byte operation.
- Burst: data operations continue until a port's Ready line to the DMA goes inactive. The DMA then stops and releases the system buses after completing its current byte operation.
- Continuous: data operations continue until the end of the programmed block of data is reached before the system buses are released. If a port's Ready line goes inactive before this occurs, the DMA simply pauses until the Ready line comes active again.

In all modes, once a byte of data is read into the DMA, the operation on the byte will be completed in an orderly fashion, regardless of the state of other signals (including a port's Ready line).

Due to the DMA's high-speed buffered method of reading data, operations on one byte are not completed until the next byte is read in. Consequently, total transfer or search block lengths must be two or more bytes, and those block lengths programmed into the DMA must be one byte less than the desired block length (count is N-1 where N is the block length).

Commands and Status

The Z80 DMA has several writeable control registers and readable status registers available to the CPU. Control bytes can be written to the DMA while the DMA is enabled or disabled, but the act of writing a control byte to the DMA disables the DMA until it is again enabled by a specific command. Status bytes can also be read at any time, but writing the Read Status command or the Read Mask command disables the DMA.

Control bytes to the DMA include those which effect immediate command actions such as enable, disable, reset, load starting-address buffers, continue, clear counters, clear status bits and the like. In addition, many mode-setting control bytes can be written, including mode and class of operation, port configuration, starting addresses, block length, address counting rule, match and match-mask byte, interrupt conditions, interrupt vector, status-affects-vector condition, pulse counting, auto restart, Ready-line and Wait-line rules, and read mask.

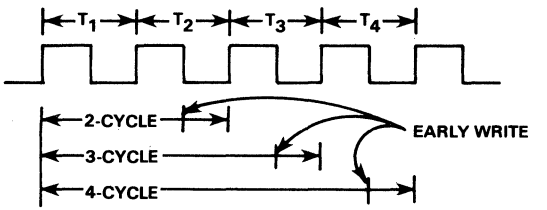
Readable status registers include a general status byte reflecting Ready-line, end-of-block, byte-match and interrupt conditions, as well as Dual-byte registers for the current byte count, Port A address and Port B address.

Variable Cycle

The Z80 DMA has the unique feature of programmable operation-cycle length. This is valuable in tailoring the DMA to the particular requirements of other system components (fast or slow) and maximizes the data-transfer rate. It also eliminates external logic for signal conditioning.

There are two aspects to the variable cycle feature. First, the entire read and write cycles (periods) associated with the source and destination ports can be independently programmed as 2, 3 or 4 T-cycles long (more if Wait cycles are used), thereby increasing or decreasing the speed with which all DMA signals change (Figure 5).

VARIABLE CYCLE LENGTH
Figure 5



Second, the four signals in each port specifically associated with transfers of data (I/O Request, Memory Request, Read and Write) can each have its active trailing edge terminated one-half T-cycle early. This adds a further dimension of flexibility and speed, allowing such things as shorter-than-normal Read or Write signals that go inactive before data starts to change.

Address Generation

Two 16-bit addresses are generated by the Z80 DMA for every transfer or search operation, one address for the source Port A and another for the destination Port B. Each address can be either variable or fixed. Variable addresses can increment or decrement from the programmed starting address. The fixed-address capability eliminates the need for separate enabling wires to I/O ports.

Port addresses are multiplexed onto the system address bus, depending on whether the DMA is reading the source port or writing to the destination port. Two readable address counters (2-bytes each) keep the current address of each port.

Auto Restart

The starting addresses of either port can be reloaded automatically at the end of a block. This option is selected by the Auto Restart control bit. The byte counter is cleared when the addresses are reloaded.

The Auto Restart feature relieves the CPU of software overhead for repetitive operations such as CRT refresh and many others. Moreover, the CPU can write different starting addresses into buffer registers during transfers causing the Auto Restart to begin at a new location.

Interrupts

The MK3883 Z80 DMA can be programmed to interrupt the CPU on four conditions:

- Interrupt on Ready (before requesting bus)
- Interrupt on Match
- Interrupt on End of Block
- Interrupt on Match at End of Block

Any of these interrupts cause an interrupt-pending status bit to be set, and each of them can optionally alter the DMA's interrupt vector. Due to the buffered constraint mentioned under "Modes of Operation," interrupts on Match at End of Block are caused by matches to the byte just prior to the last byte in the block.

The DMA shares the Z80 family's elaborate interrupt scheme, which provides fast interrupt service in real-time applications. In a Z80 CPU environment, the DMA passes its internally modifiable 8-bit interrupt vector to the CPU, which adds an additional eight bits to form the memory address of the interrupt-routine table. This table contains the address of the beginning of the interrupt routine itself.

In this process, CPU control is transferred directly to the interrupt routine, so that the next instruction executed after an interrupt acknowledge is the first instruction of the interrupt routine itself.

Pulse Generation

External devices can keep track of how many bytes have been transferred by using the DMA's pulse output, which provides a signal at 256-byte intervals. The interval sequence may be offset at the beginning by 1 to 255 bytes.

The interrupt line outputs the pulse signal in a manner that prevents misinterpretation by the CPU as an interrupt request, since it only appears when the Bus Request and Bus Acknowledge lines are both active.

PIN DESCRIPTIONS

A_0-A_{15}. System Address Bus (output, 3-state). Addresses generated by the DMA are sent to both source and destination ports (main memory or I/O peripherals) on these lines.

$\overline{BAI}$. Bus Acknowledge In (input, active Low). Signals that the system buses have been released for DMA control. In multiple-DMA configurations, the $\overline{BAI}$ pin of the highest priority DMA is normally connected to the Bus Acknowledge pin of the CPU. Lower-priority DMAs have their $\overline{BAI}$ connected to the $\overline{BAO}$ of a higher-priority DMA.

$\overline{BAO}$. Bus Acknowledge Out (output, active Low). In a multiple-DMA configuration, this pin signals that no other higher-priority DMA has requested the system busses. $\overline{BAI}$ and $\overline{BAO}$ form a daisy chain for multiple-DMA priority resolution over bus control.

$\overline{BUSRQ}$. Bus Request (bidirectional, active Low, open drain). As an output, it sends requests for control of the system address bus, data bus and control bus to the CPU. As an input when multiple DMAs are strung together in a priority daisy chain via $\overline{BAI}$ and $\overline{BAO}$, it senses when another DMA has requested the buses and causes this DMA to refrain from bus requesting until the other DMA is finished. Because it is a bidirectional pin, there cannot be any buffers between this DMA and any other DMA. It can, however, have a unidirectional into the CPU. A pull-up resistor is connected to this pin.

$\overline{CE}$/$\overline{WAIT}$. Chip Enable and Wait (input, active Low). Normally this functions only as a $\overline{CE}$ line, but it can also be programmed to serve a $\overline{WAIT}$ function. As a $\overline{CE}$ line from the CPU, it becomes active when $\overline{WR}$ and $\overline{IORQ}$ are active and the I/O port address on the system address bus is the DMA's address, thereby allowing a transfer of control or command bytes from the CPU to the DMA. As a $\overline{WAIT}$ line from memory or I/O devices, after the DMA has received a bus-request acknowledge from the CPU, it causes wait states to be inserted in the DMA's operation cycles thereby slowing the DMA to a speed that matches the memory or I/O device.

CLK. System clock (input). Standard Z80 single-phase clock at 2.5MHz (MK3883) or 4.0MHz (MK3883-4). For slower system clocks, a TTL gate with a large pullup resistor may be adequate to meet the timing and voltage level specification. For higher-speed systems, use a clock driver with an active pullup to meet the V_{IH} specification and risetime requirements.

D_0-D_7. System Data Bus (bidirectional, 3-state). Commands from the CPU, DMA status, and data from memory or I/O peripherals are transferred on these lines.

IEI. Interrupt Enable In (input, active High). This is used with IEO to form a priority daisy chain when there is more than one interrupt-driven device. A High on this line indicates that no other device of higher priority is being serviced by a CPU interrupt service routine.

IEO. Interrupt Enable Out (output, active High). IEO is High only if IEI is High and the CPU is not servicing an interrupt from this DMA. Thus, this signal blocks lower-priority devices from interrupting while a higher-priority device is being serviced by its CPU interrupt service routine.

$\overline{INT}$. Interrupt Request (output, active Low, open drain). This requests a CPU interrupt. The CPU acknowledges the interrupt by pulling its $\overline{IORQ}$ output Low during an $\overline{M1}$ cycle. It is typically connected to the $\overline{INT}$ pin of the CPU with a pullup resistor and tied to all other $\overline{INT}$ pins in the system.

$\overline{IORQ}$. Input/Output Request (bidirectional, active Low, 3-state). As an input, this indicates that the lower half of the address bus holds a valid I/O port address for transfer of control or status bytes from or to the CPU, respectively; this DMA is the addressed port if its $\overline{CE}$ pin and its $\overline{WR}$ or $\overline{RD}$ pins are simultaneously active. As an output, after the DMA has taken control of the system busses, it indicates that the lower half of the address bus holds a valid port address for another I/O device involved in a DMA transfer of data. When $\overline{IORQ}$ and $\overline{M1}$ are both active simultaneously, an interrupt acknowledge is indicated.

$\overline{M1}$. Machine Cycle One (input, active Low). Indicates that the current CPU machine cycle is an instruction fetch. It is used by the DMA to decode the return-from-interrupt instruction (RETI) (ED-4D) sent by the CPU. During two-byte instruction fetches, $\overline{M1}$ is active as each opcode byte is fetched. An interrupt acknowledge is indicated when both $\overline{M1}$ and $\overline{IORQ}$ are active.

$\overline{MREQ}$. Memory Request (bidirectional, active Low, 3-state). This indicates that the address bus holds a valid address for a memory read or write operation. As an input, it indicates that control or status information from or to memory is to be transferred to the DMA, if the DMA's $\overline{CE}$ and $\overline{WR}$ or $\overline{RD}$ lines are simultaneously active. As an output, after the DMA has taken control of the system buses, it indicates a DMA transfer request from or to memory.

$\overline{RD}$. Read (bidirectional, active Low, 3-state). As an input, this indicates that the CPU wants to read status bytes from the DMA's read registers. As an output, after the DMA has taken control of the system buses, it indicates a DMA-controlled read from a memory or I/O port address.

$\overline{WR}$. Write (bidirectional, active Low, 3-state). As an input, this indicates that the CPU wants to write control or command bytes to the DMA write registers. As an output, after the DMA has taken control of the system busses, it indicates a DMA-controlled write to a memory or I/O port address.

RDY. Ready (input, programmable active Low or High). This is monitored by the DMA to determine when a peripheral device associated with a DMA port is ready for a read or write operation. Depending on the mode of DMA operation (byte, burst or continuous), the RDY line indirectly controls DMA activity by causing the $\overline{BUSRQ}$ line to go Low or High.

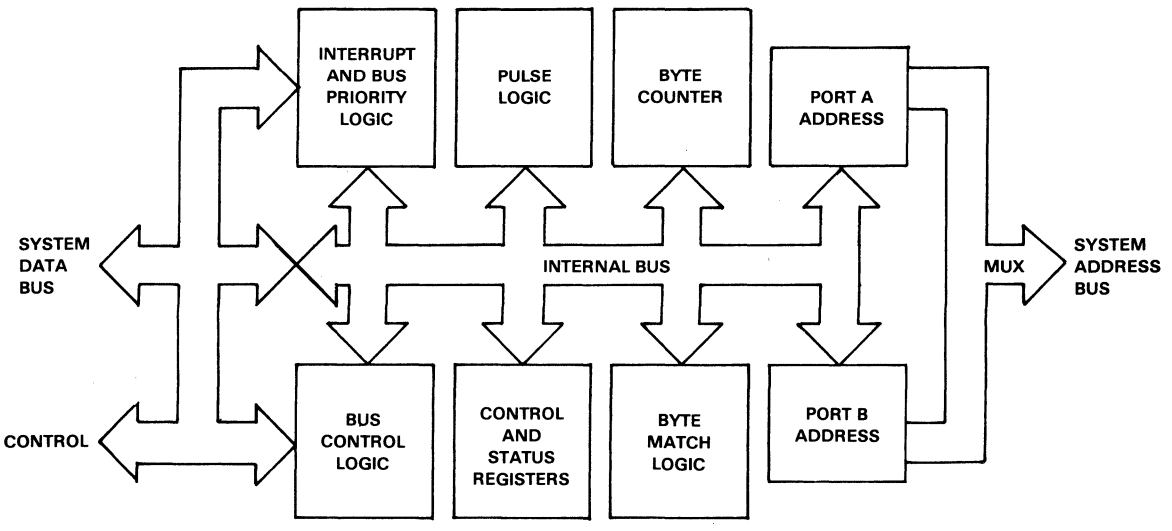
INTERNAL STRUCTURE

The internal structure of the MK3883 Z80 DMA includes driver and receiver circuitry for interfacing with an 8-bit system data bus, a 16-bit system address bus, and system control lines (Figure 6). In a Z80 CPU environment, the DMA can be tied directly to the analogous pins on the CPU (Figure 7) with no additional buffering, except for the $\overline{CE}/\overline{WAIT}$ line.

The DMA's internal data bus interfaces with the system data bus and services all internal logic and registers. Addresses generated from this logic for Ports A and B (source and destination) of the DMA's single transfer channel are multiplexed onto the system address bus.

VII

BLOCK DIAGRAM
Figure 6



Specialized logic circuits in the DMA are dedicated to the various functions of external bus interfacing, internal bus control, byte matching, byte counting, periodic pulse generation, CPU interrupts, bus requests, and address generation. A set of twenty-one writeable control registers and seven readable status registers provide the means by which the CPU governs and monitors the activities of these logic circuits. All registers are eight bits wide, with double-byte information stored in adjacent registers. The two starting-address registers (two bytes each) for Ports A and B are buffered.

The 21 writeable control registers are organized into seven base-register groups, most of which have multiple registers. The base registers in each writeable group contain both control/command bits and pointer bits that can be set to address other registers within the group. The seven readable status registers have no analogous second-level registers.

The registers are designated as follows, according to their base-register groups:

WR0-WR6 - Write Register groups 0 through 6 (7 base registers plus 14 associated registers)

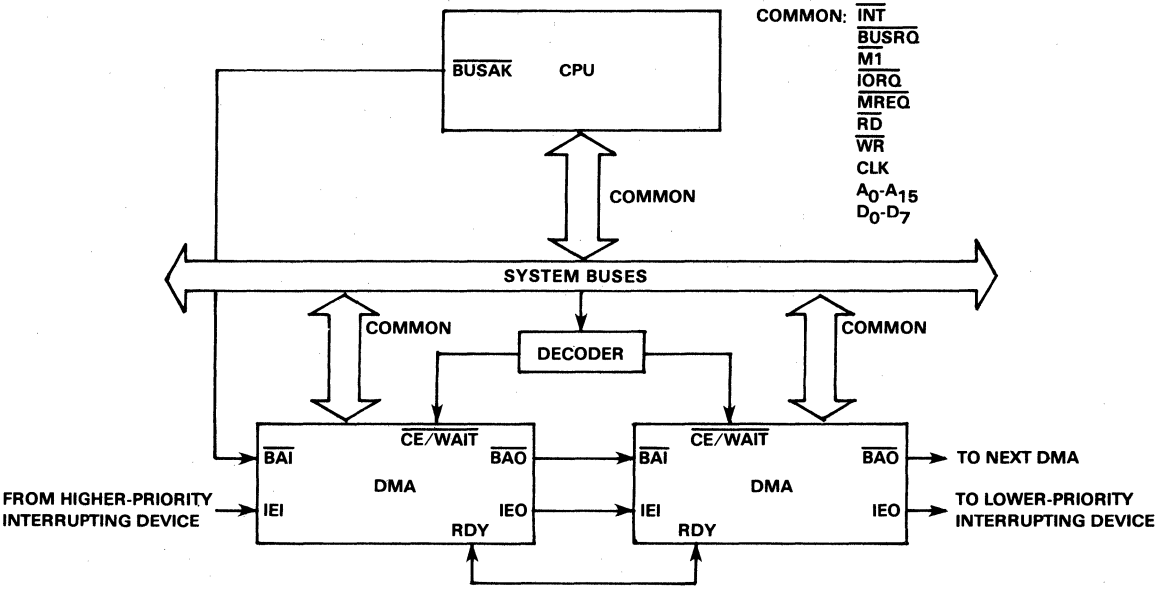
RR0-RR6 - Read Registers 0 through 6

Writing to a register within a write-register group involves first writing to the base register, with the appropriate pointer bits set, then writing to one or more of the other registers within the group. All seven of the readable status registers are accessed sequentially according to a programmable mask contained in one of the writeable registers. The section entitled "Programming" explains this in more detail.

A pipelining scheme is used for reading data in. The programmed block length is the number of bytes compared to the byte counter, which increments at the end of each cycle. In searches, data byte comparisons with the match byte are made during the read cycle of the next byte. Matches are, therefore, discovered only after the next byte is read in.

In multiple-DMA configurations, interrupt-request daisy chains are prioritized by the order in which their IEI and IEO lines are connected. The system bus, however, may not be pre-empted. Any DMA that gains access to the system buses keeps them until it is finished.

MULTIPLE-DMA INTERCONNECTION TO THE Z80 CPU
Figure 7



WRITE REGISTERS

WR0	Base register byte Port A starting address (low byte) Port A starting address (high byte) Block length (low byte) Block length (high byte)
WR1	Base register byte Port A variable-timing byte
WR2	Base register byte Port B variable-timing byte
WR3	Base register byte Mask byte Match byte
WR4	Base register byte Port B starting address (low byte) Port B starting address (high byte) Interrupt control byte Pulse control byte Interrupt vector
WR5	Base register byte
WR6	Base register byte Read mask

READ REGISTERS

RR0	Status byte
RR1	Byte counter (low byte)
RR2	Byte counter (high byte)
RR3	Port A address counter (low byte)
RR4	Port A address counter (high byte)
RR5	Port B address counter (low byte)
RR6	Port B address counter (high byte)

PROGRAMMING

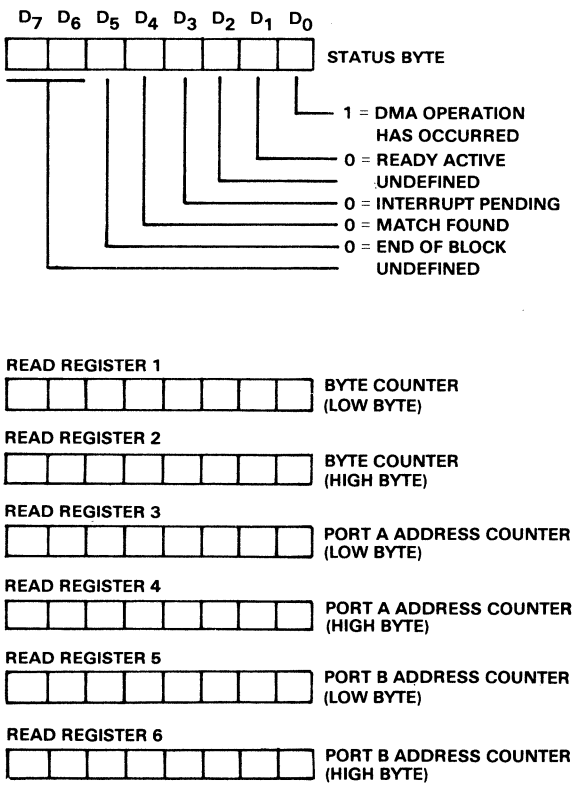
The Z80 DMA has two programmable fundamental states: (1) an enabled state, in which it can gain control of the system buses and direct the transfer of data between ports, and (2) a disabled state, in which it can initiate neither bus requests or data transfers. When the DMA is powered up or reset by any means, it is automatically placed into the disabled state. Program commands can be written to it by the CPU in either state, but this automatically puts the DMA in the disabled state, which is maintained until an enabled command is issued by the CPU. The CPU must program the DMA in advance of any data search or transfer by addressing it as an I/O port and sending a sequence of control bytes using an Output instruction (such as OTIR for the Z80 CPU).

Writing

Control or command bytes are written into one or more of the Write Register groups (WR0-WR6) by first writing to the base register byte in that group. All groups have base registers and most groups have additional associated registers. The associated registers in a group are sequentially accessed by first writing a byte to the base register containing register-group identification and pointer bits (1's) to one or more of that base register's associated registers.

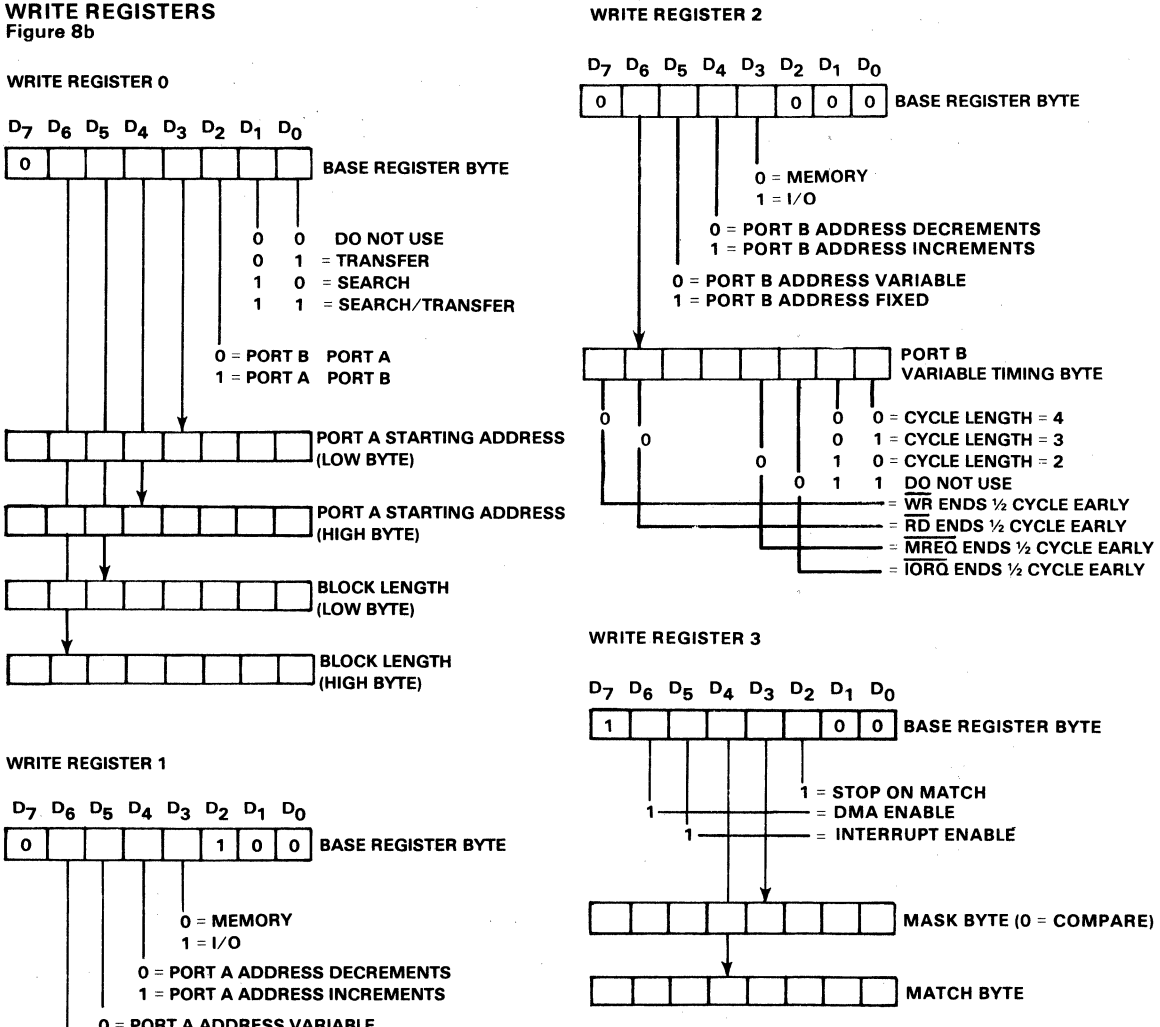
READ REGISTERS

Figure 8a.



This is illustrated in Figure 8. In this figure, the sequence in which associated registers within a group can be written to is shown by the vertical position of the associated registers. For example, if a byte written to the DMA contains the bits that identify WR0 (bits D0, D1 and D7), and also contains 1's in the bit positions that point to the associated "Port A Starting Address (low byte)" and "Port A Starting Address (high byte)" then the next two bytes written to the DMA will be stored in these two registers, in that order.

WRITE REGISTERS
Figure 8b



Reading

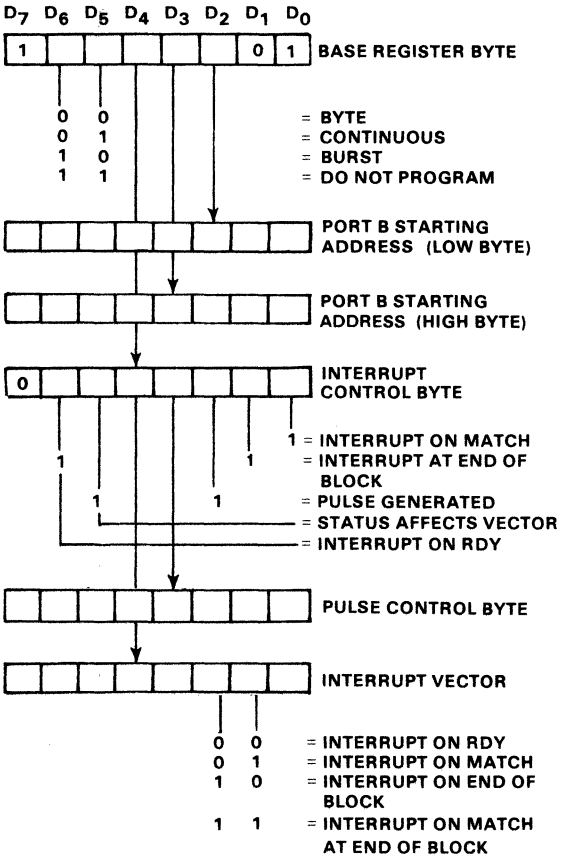
The Read Registers (RR0-RR6) are read by the CPU by addressing the DMA as an I/O port using an Input instruction (such as INIR for the Z80 CPU). The readable bytes contain DMA status, byte-counter values, and port addresses since the last DMA reset. The registers are always read in a fixed sequence beginning with RR0 and ending with RR6. However, the register read in this sequence is determined by programming the Read Mask in WR6. The sequence of reading is initialized by writing an Initiate Read Sequence or Set Read Status command to WR6. After a Reset DMA, the sequence must be initialized with the Initiate Read Sequence command or a Read Status command. The sequence of reading all registers that are not excluded by the Read Mask register must be completed before a new Initiate Read Sequence or Read Status command.

Fixed-Address Programming

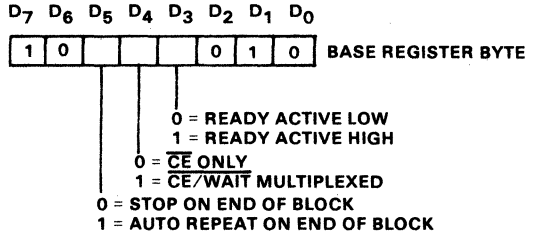
A special circumstance arises when programming a destination port to have a fixed address. The load command in WR6 only loads a fixed address to a port selected as the source, not to a port selected as the destination. Therefore, a fixed destination address must be loaded by temporarily declaring it a fixed-source

WRITE REGISTERS
Figure 8b

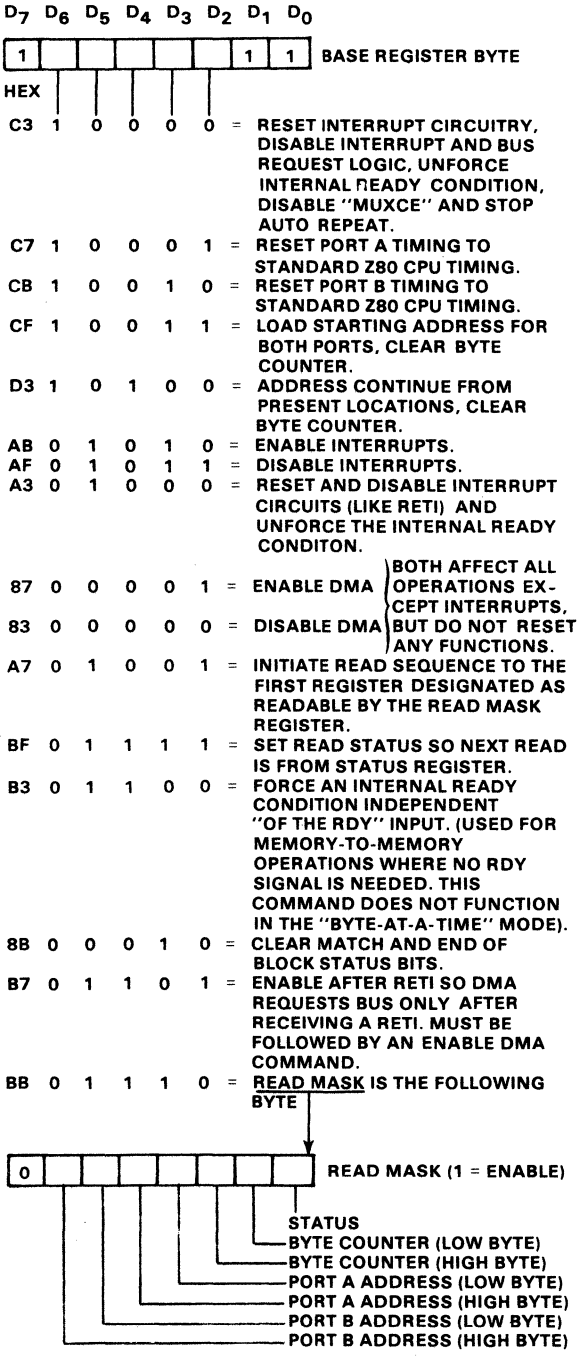
WRITE REGISTER 4



WRITE REGISTER 5



WRITE REGISTER 6



VII

SAMPLE DMA PROGRAM

Figure 9

COMMENTS	D_7	D_8	D_5	D_4	D_3	D_2	D_1	D_0	HEX
WR0 sets DMA to receive block length, Port A starting address and temporarily sets Port B as source.	0	1 Block Length Upper Follows	1 Block Length Lower Follows	1 Port A Upper Address Follows	1 Port A Lower Address Follows	0 B→A Temporary for Loading B Address	0	1 Transfer, No Search	79
Port A address (lower)	0	1	0	1	0	0	0	0	50
Port A address (upper)	0	0	0	1	0	0	0	0	10
Block length (lower)	0	0	0	0	0	0	0	0	00
Block length (upper)	0	0	0	1	0	0	0	0	10
WR1 defines Port A as peripheral with fixed address.	0	0 No Timing Follows	0 Address Changes	1 Address Increments	0 Port is Memory	1 This is Port A	0	0	14
WR2 defines Port B as peripheral with fixed address.	0	0 No Timing Follows	1 Fixed Address	0	1 Port is I/O	0 This is Port B	0	0	28
WR4 sets mode to Burst, sets DMA to expect Port B address.	1	1 Burst Mode	0	0 No Interrupt Control Byte Follows	0 No Upper Address	1 Port B Lower Address Follows	0	1	C5
Port B address (lower)	0	0	0	0	0	1	0	1	05
WR5 sets Ready active High	1	0	0 No Auto Restart	0 No Wait States	1 RDY Active High	0	1	0	8A
WR6 loads both Port addresses and resets block counter.*	1	1	0	0 Load	1	1	1	1	CF
WR0 sets Port A as source.*	0	0	0 No Address of Block Length Bytes	0	0	1 A→B	0 Transfer, No Search	1	05
WR6 reloads Port addresses and resets block counter	1	1	0	0 Load	1	1	1	1	CF
WR6 enables DMA to start operation.	1	0	0	0 Enable DMA	0	1	1	1	87

NOTE: The actual number of bytes transferred is one more than specified by the block length.
*These commands are necessary only in the case of a fixed destination address.

address and subsequently declaring the true source as such, thereby implicitly making the other a destination.

The following example illustrates the steps in this procedure, assuming that transfers are to occur from a variable-address source (Port A) to a fixed-address destination (Port B):

1. Temporarily declare Port B as source in WR0.
2. Load Port B address in WR6.
3. Declare Port A as source in WR0.
4. Load Port A address in WR6.
5. Enable DMA in WR6.

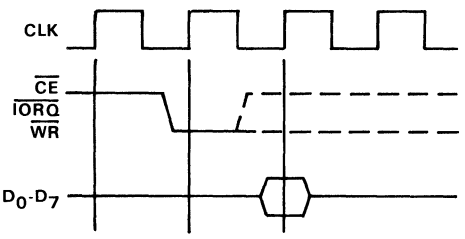
Figure 9 illustrates a program to transfer data from memory (Port A) to a peripheral device (Port B). In this example, the Port A memory starting address is 1050_H and the Port B peripheral fixed address is 05_H. Note that the data flow is 1001_H bytes—one more than specified by the block length. The table of DMA commands may be stored in consecutive memory locations and transferred to the DMA with an output instruction such as the Z80 CPU's OTIR instruction.

INACTIVE STATE TIMING (DMA as CPU Peripheral)

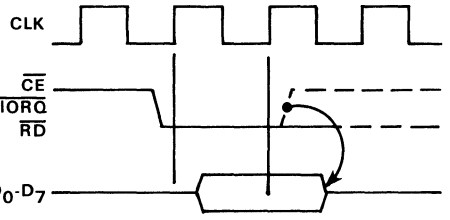
In its inactive state, the DMA is addressed by the CPU as an I/O peripheral for write and read (control and status) operations. Write timing is illustrated in Figure 10.

Reading of the DMA's status byte, byte counter or port address counters is illustrated in Figure 11. These operations require less than three T-cycles. The $\overline{CE}$, $\overline{IORQ}$ and $\overline{RD}$ lines are made active over two rising edges of CLK, and data appears on the bus approximately one T-cycle after they become active.

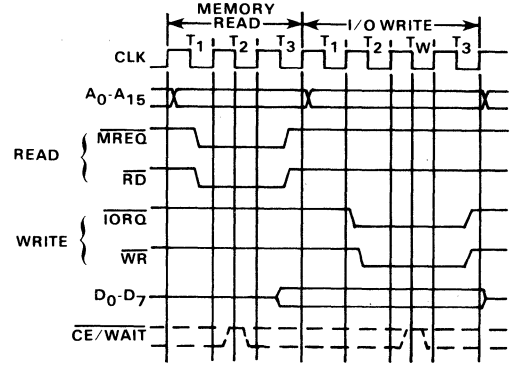
CPU-TO-DMA WRITE CYCLE
Figure 10



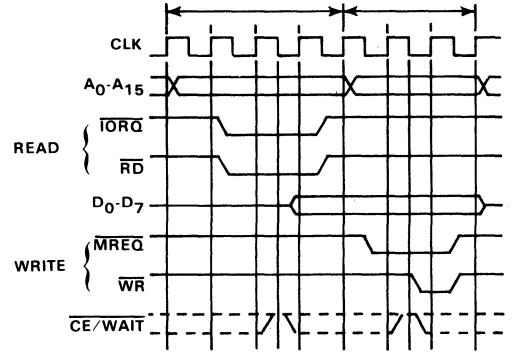
CPU-TO-DMA READ CYCLE
Figure 11



MEMORY-TO-I/O TRANSFER
Figure 12



I/O-TO-MEMORY TRANSFER
Figure 13



ACTIVE STATE TIMING (DMA as Bus Controller)

The DMA is active when it takes control of the system bus and begins transferring data.

Default Read and Write Cycles

By default, and after reset the DMA's timing of read and write operations is exactly the same as the Z80 CPU's timing of read and write cycles for memory and I/O peripherals, with one exception: during a read cycle, data is latched on the falling edge of T_3 and held on the data bus across the boundary between read and write cycles, through the end of the following write cycle.

Figure 12 illustrates the timing for memory-to-I/O port transfers and Figure 13 illustrates I/O-to-memory transfers. Memory-to-memory and I/O-to-I/O transfer timings are simply permutations of these diagrams.

The default timing uses three T-cycles for memory transactions and four T-cycles for I/O transactions, which include one automatically inserted wait cycle between T_2 and T_3. If the $\overline{CE/WAIT}$ line is programmed to act as WAIT line during the DMA's active state, it is sampled on the falling edge of T_2 for memory transactions and the falling edge of T_W for I/O transactions. If $\overline{CE/WAIT}$ is low during this time another T-cycle is added, during which the $\overline{CE/WAIT}$ line will again be sampled. The duration of transactions can thus be indefinitely extended.

Variable Cycle and Edge Timing

The Z80 DMA's default operation-cycle length for the source (read) port and destination (write) port can be independently programmed. This variable-cycle feature allows read or write cycles consisting of two, three or four T-cycles (more if Wait cycles are inserted), thereby increasing or decreasing the speed of all signals generated by the DMA. In addition, the trailing edges of the $\overline{IORQ}$, $\overline{MREQ}$, $\overline{RD}$ and $\overline{WR}$ signals can be independently terminated one-half cycle early. Figure 14 illustrates this.

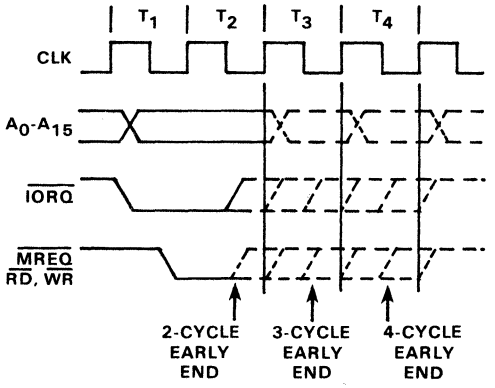
In the variable-cycle mode, unlike default timing, $\overline{IORQ}$ comes active one-half cycle before $\overline{MREQ}$, $\overline{RD}$ and $\overline{WR}$. $\overline{CE/WAIT}$ can be used to extend only the 3 or 4 T-cycle variable cycles. It is sampled at the falling edge of T_2 for 3- or 4-cycle memory cycles, and at the falling edge of T_3 for 4-cycle I/O cycles.

During transfers, data is latched on the clock edge causing the rising edge of $\overline{RD}$ and held until the end of the write cycle.

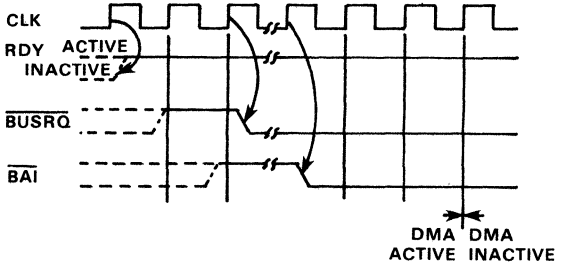
Bus Requests

Figure 15 illustrates the bus request and acceptance timing. The RDY line, which may be programmed active

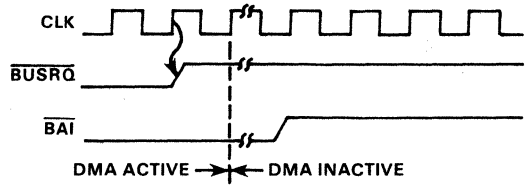
VARIABLE-CYCLE AND EDGE TIMING
Figure 14



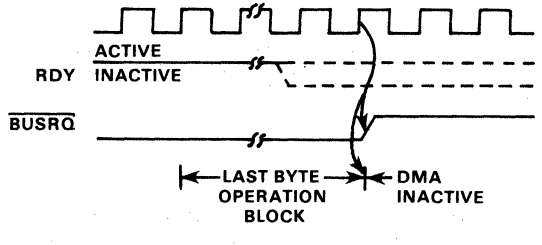
BUS REQUEST AND ACCEPTANCE
Figure 15



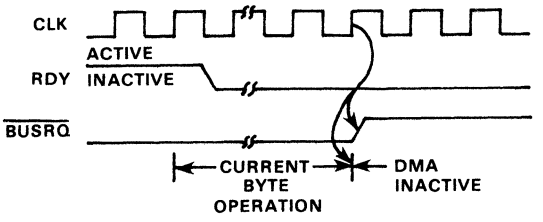
BUS RELEASE (BYTE-AT-A-TIME MODE)
Figure 16



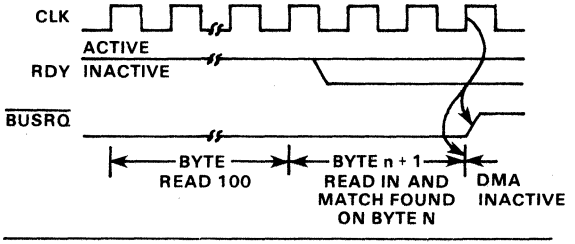
BUS RELEASE (CONTINUOUS MODE)
Figure 17



BUS RELEASE WHEN NOT READY (BURST MODE)
Figure 18



BUS RELEASE ON MATCH (BURST AND CONTINUOUS MODES)
Figure 19



High or Low, is sampled on every rising edge of CLK. If it is found to be active, and the bus is not in use by any other device, the following rising edge of CLK drives $\overline{BUSRQ}$ low. After receiving $\overline{BUSRQ}$, the CPU acknowledges on the $\overline{BAI}$ input either directly or through a multiple-DMA daisy chain. When a low is detected on $\overline{BAI}$ for two consecutive rising edges of CLK, the DMA will begin transferring data on the next rising edge of CLK.

Bus Release Byte-at-a-Time

In Byte-at-a-Time mode, $\overline{BUSRQ}$ is brought high on the rising edge of CLK prior to the end of each read cycle (search-only) or write cycle (transfer and transfer/search) as illustrated in Figure 16. This is done regardless of the state of RDY. There is no possibility of confusion when a Z80 CPU is used since the CPU cannot begin an operation until the following T-cycle. Most other CPUs are not bothered by this either, although note should be taken of it. The next bus request for the next byte will come after both $\overline{BUSRQ}$ and $\overline{BAI}$ have returned high.

Bus Release at End of Block

In Burst and Continuous modes, an end of block causes $\overline{BUSRQ}$ to go High usually on the same rising edge of CLK in which the DMA completes the transfer of the data block (Figure 17). The last byte in the block is transferred even if RDY goes inactive before completion of the last byte transfer.

Bus Release on Not Ready

In Burst Mode, when RDY goes inactive it causes $\overline{BUSRQ}$ to go High on the next rising edge of CLK after the completion of its current byte operation (Figure 18). The action on $\overline{BUSRQ}$ is thus somewhat delayed from action on the RDY line. The DMA always completes its current byte operation in an orderly fashion before releasing the bus.

By contrast, $\overline{BUSRQ}$ is not released in Continuous mode when RDY goes inactive. Instead, the DMA idles after completing the current byte operation, awaiting an active RDY again.

Bus Release on Match

If the DMA is programmed to stop on match in Burst or Continuous modes, a match causes $\overline{BUSRQ}$ to go inactive on the rising edge of CLK after the next byte following the match (Figure 19). Due to the pipelining scheme, matches are determined while the next byte is being read. Matches at End-of-Block are, therefore, actually matches to the byte immediately preceding the last byte in the block.

The RDY line can go inactive after the matching operation begins without affecting this bus-release timing.

Interrupts

Timings for interrupt acknowledge and return from interrupt are the same as timings for these in other Z80 peripherals.

Interrupt on RDY (interrupt before requesting bus) does not directly affect the $\overline{BUSRQ}$ line. Instead, the interrupt service routine must handle this by issuing the following commands to WR6:

1. Enable after Return From Interrupt (RETI) Command —Hex B7
2. Enable DMA—Hex 87
3. A RETI instruction that resets the IUS latch in the Z80 DMA

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Operating Ambient Temperature Under Bias ..... As Specified Under "Ordering Information"
Storage Temperature ..... -65°C to +150°C
Voltage on any pin with respect to ground ..... -0.3V to +7V
Power Dissipation 1.5W

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

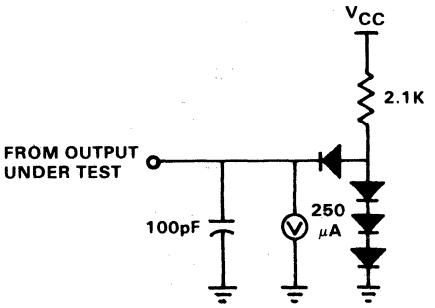
STANDARD TEST CONDITIONS

The characteristics below apply for the following standard test conditions, unless otherwise noted. All voltages are referenced to GND. Positive current flows into the referenced pin. Standard conditions are as follows:

- $+4.75 \leq V_{CC} \leq +5.25V$
- GND = 0V
- $0°C \leq T_A \leq +70°C$

All AC parameters assume a load capacitance of 100pF max. Timing references between two output signals assume a load difference of 50pF max.

Figure 20



DC CHARACTERISTICS

SYM	PARAMETER	MIN	MAX	UNIT	TEST CONDITION
V_{ILC}	Clock Input Low Voltage	-0.3	0.80	V	
V_{IHC}	Clock Input High Voltage	V_{CC}-.6	5.5	V	
V_{IL}	Input Low Voltage	-0.3	0.8	V	

DC CHARACTERISTICS

SYM	PARAMETER	MIN	MAX	UNIT	TEST CONDITION
V_{IH}	Input High Voltage	2.0	5.5	V	
V_{OL}	Output Low Voltage		0.4	V	I_{OL}=3.2mA for $\overline{BUSRQ}$ I_{OL}=2.0mA for all others
V_{OH}	Output High Voltage	2.4		V	I_{OH}=250μA
I_{CC}	Power Supply Current MK3883 MK3883-4		 150 200	 mA mA	
I_{LI}	Input Leakage Current		$\pm$ 10	μA	V_{IN} = 0 to V_{CC}
I_{LOH}	Tri-State Output Leakage Current in Float		10	μA	V_{OUT}=2.4 to V_{CC}
I_{LOL}	Tri-State Output Leakage Current in Float		-10	μA	V_{OUT}=0.4V
I_{LD}	Data Bus Leakage Current in Input Mode		$\pm$ 10	μA	$0 \leq V_{IN} \leq V_{CC}$

V_{CC} = 5V $\pm$ 5% unless otherwise specified, over specified temperature range.

CAPACITANCE

SYM	PARAMETER	MIN	MAX	UNIT	TEST CONDITION
C	Clock Capacitance		35	pF	Unmeasured Pins
C_{IN}	Input Capacitance		10	pF	Returned to Ground
C_{OUT}	Output Capacitance		10	pF	

f = 1MHz, over specified temperature range

INACTIVE STATE AC CHARACTERISTICS

(See Figure 21)

NO	SYM	PARAMETER	MK3883		MK3883-4		UNIT
			MIN	MAX	MIN	MAX	
1	TcC	Clock Cycle Time	400	4000	250	4000	ns
2	TwCh	Clock Width (High)	170	2000	105	2000	ns
3	TwCl	Clock Width (Low)	170	2000	105	2000	ns
4	TrC	Clock Rise Time		30		30	ns
5	TfC	Clock Fall Time		30		30	ns
6	Th	Hold Time for Any Specified Setup Time	0		0		ns
7	TsC(Cr)	$\overline{IORQ}$, $\overline{WR}$, $\overline{CE}$ $\downarrow$ to Clock $\uparrow$ Setup	280		145		ns
8	TdDO(RDf)	$\overline{RD}$ to Data Output Delay		500		380	ns
9	TsWM(Cr)	Data In to Clock $\uparrow$ Setup ($\overline{WR}$ or $\overline{M1}$)	50		50		ns
10	TdCf(DO)	$\overline{IORQ}\downarrow$ to Data Out Delay (INTA Cycle)		340		160	ns

INACTIVE STATE AC CHARACTERISTICS (Continued)

NO	SYM	PARAMETER	MK3883		MK3883-4		UNIT
			MIN	MAX	MIN	MAX	
11	TdRD(Dz)	$\overline{RD}\uparrow$ to Data Float Delay (output buffer disable)		160		110	ns
12	TsIEI(IORQ)	IEI $\downarrow$ to $\overline{IORQ}\downarrow$ Setup (INTA Cycle)	140		140		ns
13	TdIEOr(IEIr)	IEI $\uparrow$ to IEO $\uparrow$ Delay		210		160	ns
14	TdIEOf(IEIf)	IEI $\downarrow$ to IEO $\downarrow$ Delay		190		130	ns
15	TdM1(IEO)	$\overline{M1}\downarrow$ to IEO$\downarrow$ Delay (interrupt just prior to $\overline{M1}\downarrow$)		300		190	ns
16	TsM1f(Cr)	$\overline{M1}\downarrow$ to Clock $\uparrow$ Setup	210		90		ns
17	TsM1r(Cf)	$\overline{M1}\uparrow$ to Clock $\downarrow$ Setup	20		0		ns
18	TsRD(C)	$\overline{RD}\downarrow$ to Clock $\uparrow$ Setup ($\overline{M1}$ Cycle)	240		115		ns
19	TdI(INT)	Interrupt Cause to $\overline{INT}\downarrow$ Delay ($\overline{INT}$ generated only when DMA is inactive)		500		500	ns
20	TdBAIr (BAOr)	$\overline{BAI}\uparrow$ to $\overline{BAO}\uparrow$ Delay		200		150	ns
21	TdBAIf (BAOf)	$\overline{BAI}\downarrow$ to $\overline{BAO}\downarrow$ Delay		200		150	ns
22	TsRDY(Cr)	RDY Active to Clock $\uparrow$ Setup	150		100		ns

VII

ACTIVE STATE AC CHARACTERISTICS
(See Figure 22)

NO	SYM	PARAMETER	MK3883		MK3883-4	
			MIN(ns)	MAX(ns)	MIN(ns)	MAX(ns)
1	TcC	Clock Cycle Time	400		250	
2	TwCh	Clock Width (High)	180	2000	110	2000
3	TwCl	Clock Width (Low)	180	2000	110	2000
4	TrC	Clock Rise Time		30		30
5	TfC	Clock Fall Time		30		30
6	TdA	Address Output Delay		145		110
7	TdC(Az)	Clock $\uparrow$ to Address Float Delay		110		90
8	TsA(MREQ)	Address to $\overline{MREQ}\downarrow$ Setup (Memory Cycle)	(2)+(5)-75		(2)+(5)-75	
9	TsA(IRW)	Address Stable to $\overline{IORQ}$, $\overline{RD}$, $\overline{WR}\downarrow$ Setup (I/O Cycle)	(1)-80		(1)-70	
*10	TdRW(A)	$\overline{RD}$, $\overline{WR}\uparrow$ to Addr. Stable Delay	(3)+(4)-40		(3)+(4)-50	
*11	TdRW(Az)	$\overline{RD}$, $\overline{WR}\uparrow$ to Addr. Float	(3)+(4)-60		(3)+(4)-45	
12	TdCf(DO)	Clock $\downarrow$ to Data Out Delay		230		150

ACTIVE STATE AC CHARACTERISTICS

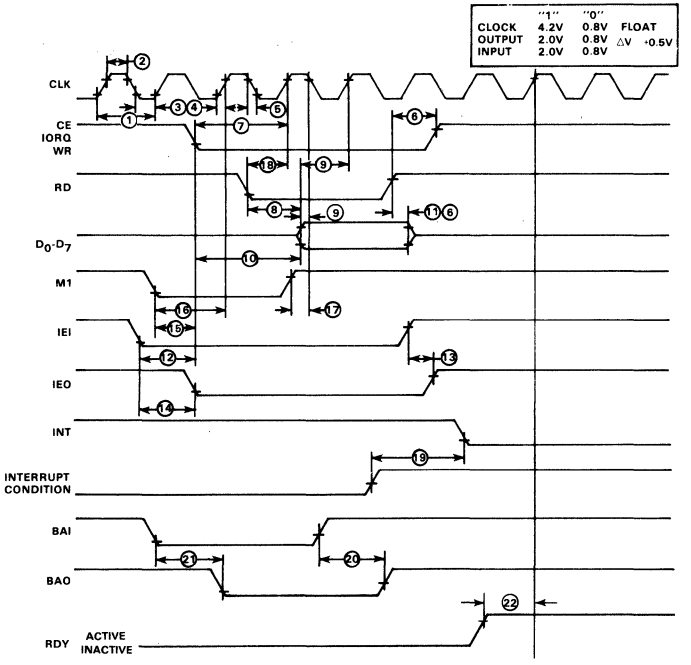
NO	SYM	PARAMETER	MK3883		MK3883-4	
			MIN(ns)	MAX(ns)	MIN(ns)	MAX(ns)
*13	TdCr(Dz)	Clock↑ to Data Float Delay (Write Cycle)		90		90
14	TsDI(Cr)	Data In to Clock↑ Setup (Read cycle when rising edge ends read)	50		35	
15	TsDI(Cf)	Data In to Clock↓ Setup (Read cycle when falling edge ends read)	60		50	
*16	TsDO(WfM)	Data Out to $\overline{WR}$↓ Setup (Memory Cycle)	(1)-210		(1)-170	
17	TsDO(WfI)	Data Out to $\overline{WR}$↓ Setup (I/O cycle)	100		100	
*18	TdWr(DO)	$\overline{WR}$↑ to Data Out Delay	(3)+(4)-80		(3)+(4)-70	
19	Th	Hold Time for Any Specified Setup Time	0		0	
*20	TdCr(Mf)	Clock↑ to $\overline{MREQ}$↓ Delay		100		85
21	TdCf(Mf)	Clock↓ to $\overline{MREQ}$↓ Delay		100		85
22	TdCr(Mr)	Clock↑ to $\overline{MREQ}$↑ Delay		100		85
23	TdCf(Mr)	Clock↓ to $\overline{MREQ}$↑ Delay		100		85
24	TwM1	$\overline{MREQ}$ Low Pulse Width	(1)-40		(1)-30	
*25	TwMh	$\overline{MREQ}$ High Pulse Width	(2)+(5)-30		(2)+(5)-20	
26	TdCr(If)	Clock↑ to $\overline{IORQ}$↓ Delay		90		75
27	TdCf(If)	Clock↓ to $\overline{IORQ}$↓ Delay		110		85
28	TdCr(Ir)	Clock↑ to $\overline{IORQ}$↑ Delay		100		85
*29	TdCf(Ir)	Clock↓ to $\overline{IORQ}$↑ Delay		110		85
30	TdCr(Rf)	Clock↑ to $\overline{RD}$↓ Delay		100		85
31	TdCf(Rf)	Clock↓ to $\overline{RD}$↓ Delay		130		95
32	TdCr(Rr)	Clock↑ to $\overline{RD}$↑ Delay		100		85
33	TdCf(Rr)	Clock↓ to $\overline{RD}$↑ Delay		110		85
34	TdCr(Wf)	Clock↑ to $\overline{WR}$↓ Delay		80		65
35	TdCf(Wf)	Clock↓ to $\overline{WR}$↓ Delay		90		80
*36	TdCr(Wr)	Clock↑ to $\overline{WR}$↑ Delay		100		80
37	TdCf(Wr)	Clock↓ to $\overline{WR}$↑ Delay		100		80
38	TwWI	$\overline{WR}$ Low Pulse Width	(1)-40		(1)-30	
39	TsWA(Cf)	$\overline{WAIT}$ to Clock↓ Setup	70		70	
40	TdCr(B)	Clock↑ to $\overline{BUSRQ}$ Delay		100		100
41	TdCr(Iz)	Clock↑ to $\overline{IORQ}$, $\overline{MREQ}$, $\overline{RD}$, $\overline{WR}$ Float Delay		100		80

NOTES:

1. Numbers in parentheses are other parameter-numbers in this table; their values should be substituted in equations.
2. All equations imply DMA default (standard) timing.
3. Data must be enabled onto data bus when RD is active.
4. Asterisk(*) before parameter number means the parameter is not illustrated in the AC Timing Diagrams.

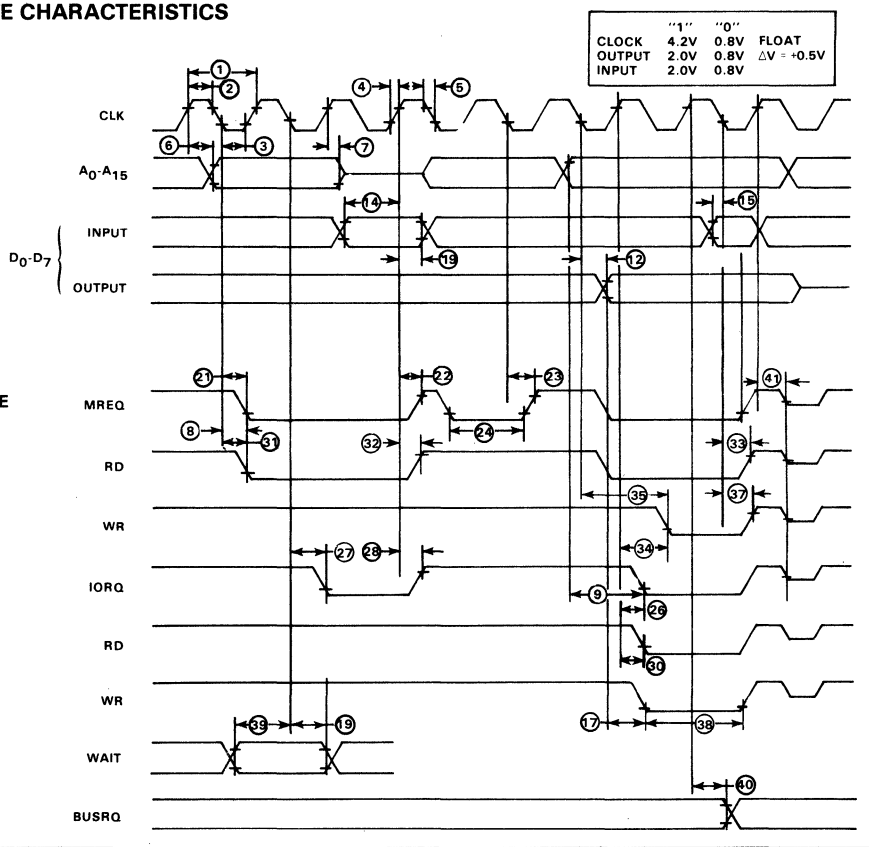
INACTIVE STATE CHARACTERISTICS

Figure 21



ACTIVE STATE CHARACTERISTICS

Figure 22



ORDERING INFORMATION

PART NO.	PACKAGE TYPE	MAX CLOCK FREQUENCY	TEMPERATURE RANGE
MK3883N MK3883P	Z80-DMA Plastic Z80-DMA Ceramic	2.5 MHz 2.5 MHz	0°C to +70°C 0°C to +70°C
MK3883N-10 MK3883P-10	Z80-DMA Plastic Z80-DMA Ceramic	2.5 MHz 2.5 MHz	–40°C to +85°C –40°C to +85°C
MK3883N-4 MK3883P-4	Z80A-DMA Plastic Z80A-DMA Ceramic	4 MHz 4 MHz	0°C to +70°C 0°C to +70°C

Serial Input/Output Controller MK3884

FEATURES

- Two independent full-duplex channels, with separate control and status lines for modems or other devices.
- Data rates of 0 to 500K bits/second in the x1 clock mode with a 2.5MHz clock (MK3884 Z80 SIO), or 0 to 800K bits/second with a 4.0MHz clock (MK3884-4 Z80 SIO).
- Asynchronous protocols: everything necessary for complete messages in 5, 6, 7 or 8 bits/character. Includes variable stop bits and several clock-rate multipliers; break generation and detection; parity; overrun and framing error detection.
- Synchronous protocols: everything necessary for complete bit- or byte-oriented messages in 5, 6, 7 or 8 bits/character, including IBM Bisync, SDLC, HDLC, CCITT-X.25 and others. Automatic CRC generation/-checking, sync character and zero insertion/-deletion, abort generation/detection and flag insertion.
- Receiver data registers quadruply buffered, transmitter registers doubly buffered.
- Highly sophisticated and flexible daisy-chain interrupt vectoring for interrupts without external logic.

DESCRIPTION

The MK3884 Z80 SIO Serial Input/Output Controller is a dual-channel data communication interface with extraordinary versatility and capability. Its basic functions as a serial-to-parallel, parallel-to-serial converter/controller can be programmed by a CPU for a broad range of serial communication applications.

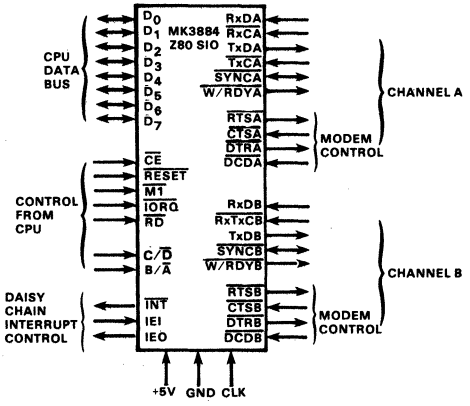
The device supports all common asynchronous and synchronous protocols, byte- or bit-oriented, and performs all of the functions traditionally done by UARTs, USARTs and synchronous communication controllers combined, plus additional functions traditionally performed by the CPU. Moreover, it does this on two fully-independent channels, with an exceptionally sophisticated interrupt structure that allows very fast transfers.

Full interfacing is provided for CPU or DMA control. In addition to data communication, the circuit can handle virtually all types of serial I/O with fast (or slow) peripheral devices. While designed primarily as a member of the Z80 family, its versatility makes it well suited to many other CPUs.

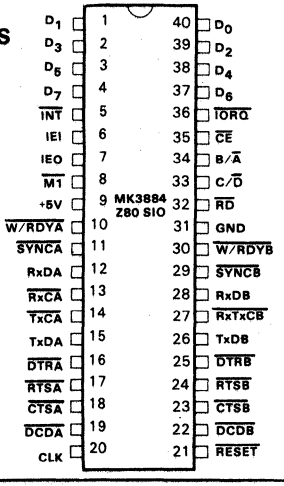
The Z80 SIO is an n-channel silicon-gate depletion-load device packaged in a 40-pin plastic, or ceramic DIP. It uses a single +5V power supply and the standard Z80 family single-phase clock.

VII

MK3884 Z80 SIO PIN FUNCTIONS
Figure 1



MK3884 Z80 SIO PIN ASSIGNMENTS
Figure 2



PIN DESCRIPTIONS

Figures 1 through 6 illustrate the three pin configurations (bonding options) available in the SIO. The constraints of a 40-pin package make it impossible to bring out the Receive Clock ($\overline{RxC}$), Transmit Clock ($\overline{TxC}$), Data Terminal Ready ($\overline{DTR}$) and Sync ($\overline{SYNC}$) signals for both channels. Therefore, either Channel B lacks a signal or two signals are bonded together in the three bonding options offered:

- MK3887 Z80 SIO lacks $\overline{SYNCB}$
- MK3885 Z80 SIO lacks $\overline{DTRB}$
- MK3884 Z80 SIO has all four signals, but $\overline{TxCB}$ and $\overline{RxCB}$ are bonded together

The pin descriptions are as follows:

B/$\overline{A}$. Channel A Or B Select (input, High selects Channel B). This input defines which channel is accessed during a data transfer between the CPU and the SIO. Address bit A_0 from the CPU is often used for the selection function.

C/$\overline{D}$. Control Or Data Select (input, High selects Control). This input defines the type of information transfer performed between the CPU and the SIO. A High at this input during a CPU write to the SIO causes the information on the data bus to be interpreted as a command for the channel selected by B/$\overline{A}$. A Low at C/$\overline{D}$ means that the information on the data bus is data. Address bit A_1 is often used for this function.

$\overline{CE}$. Chip Enable (Input, active Low). A Low level at this input enables the SIO to accept command or data input from the CPU during a write cycle, or to transmit data to the CPU during a read cycle.

CLK. System Clock (input). The SIO uses the standard Z80 System Clock to synchronize internal signals. This is a single-phase clock.

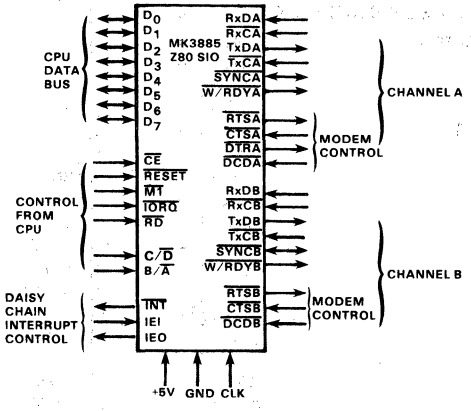
$\overline{CTSA}$, $\overline{CTSB}$. Clear To Send (inputs, active Low). When programmed as Auto Enables, a Low on these inputs enables the respective transmitter. If not programmed as Auto Enables, these inputs may be programmed as general-purpose inputs. Both inputs are Schmitt-trigger buffered to accommodate slow-risetime signals. The SIO detects pulses on these inputs and interrupts the CPU on both logic level transitions. The Schmitt-trigger buffering does not guarantee a specified noise-level margin.

D_0-D_7. System Data Bus (bidirectional, 3-state). The system data bus transfers data and commands between the CPU and the Z80 SIO. D_0 is the least significant bit.

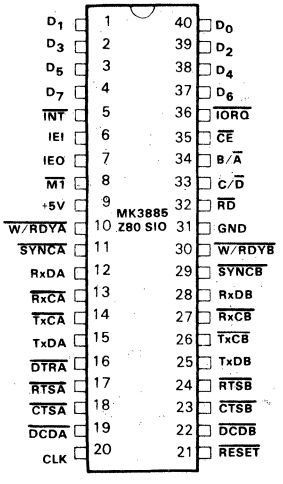
$\overline{DCDA}$, $\overline{DCDB}$. Data Carrier Detect (inputs, active Low). These pins function as receiver enables if the SIO is programmed for Auto Enables; otherwise they may be used as general-purpose input pins. Both pins are Schmitt-trigger buffered to accommodate slow-risetime signals. The SIO detects pulses on these pins and interrupts the CPU on both logic level transitions. Schmitt-trigger buffering does not guarantee a specific noise-level margin.

$\overline{DTRA}$, $\overline{DTRB}$. Data Terminal Ready (outputs, active Low). These outputs follow the state programmed into Z80 SIO. They can also be programmed as general-purpose outputs.
In the MK3885 bonding option, $\overline{DTRB}$ is omitted.

MK3885 Z80 SIO PIN FUNCTIONS
Figure 3



MK3885 Z80 SIO PIN ASSIGNMENTS
Figure 4



IEI. Interrupt Enable In (input, active High). This signal is used with IEO to form a priority daisy chain when there is more than one interrupt-driven device. A High on this line indicates that no other device of higher priority is being serviced by a CPU interrupt service routine.

IEO. Interrupt Enable Out (output, active High). IEO is High only if IEI is High and the CPU is not servicing an interrupt from this SIO. Thus, this signal blocks lower priority devices from interrupting while a higher priority device is being serviced by its CPU interrupt service routine.

$\overline{\text{INT}}$. Interrupt Request (output, open drain, active Low). When the SIO is requesting an interrupt, it pulls $\overline{\text{INT}}$ Low.

$\overline{\text{IORQ}}$. Input/Output Request (input from CPU, active Low). $\overline{\text{IORQ}}$ is used in conjunction with B/$\overline{\text{A}}$, C/$\overline{\text{D}}$, $\overline{\text{CE}}$ and $\overline{\text{RD}}$ to transfer commands and data between the CPU and the SIO. When $\overline{\text{CE}}$, $\overline{\text{RD}}$ and $\overline{\text{IORQ}}$ are all active, the channel selected by B/$\overline{\text{A}}$ transfers data to the CPU (a read operation). When $\overline{\text{CE}}$ and $\overline{\text{IORQ}}$ are active, but $\overline{\text{RD}}$ is inactive, the channel selected by B/$\overline{\text{A}}$ is written to by the CPU with either data or control information as specified by C/$\overline{\text{D}}$. As mentioned previously, if $\overline{\text{IORQ}}$ and $\overline{\text{M1}}$ are active simultaneously, the CPU is acknowledging an interrupt and the SIO automatically places its interrupt vector on the CPU data bus if it is the highest priority device requesting an interrupt.

$\overline{\text{M1}}$. Machine Cycle (input from Z80 CPU, active Low). When $\overline{\text{M1}}$ is active and $\overline{\text{RD}}$ is also active, the Z80 CPU is fetching an instruction from memory; when $\overline{\text{M1}}$ is active while $\overline{\text{IORQ}}$ is active, the SIO accepts $\overline{\text{M1}}$ and $\overline{\text{IORQ}}$ as an interrupt acknowledge if the SIO is the highest priority device that has interrupted the Z80 CPU.

$\overline{\text{RxCA}}$, $\overline{\text{RxCB}}$. Receiver Clocks (inputs). Receive data is sampled on the rising edge of $\overline{\text{RxC}}$. The Receive Clocks may be 1, 16, 32 or 64 times the data rate in asynchronous modes. These clocks may be driven by the Z80 CTC Counter Timer Circuit for programmable baud rate generation. Both inputs are Schmitt-trigger buffered (no noise level margin is specified).

In the MK3884 bonding option, $\overline{\text{RxCB}}$ is bonded together with $\overline{\text{TxCB}}$.

$\overline{\text{RD}}$. Read Cycle Status (input from CPU, active Low). If $\overline{\text{RD}}$ is active, a memory or I/O read operation is in progress. $\overline{\text{RD}}$ is used with B/$\overline{\text{A}}$, $\overline{\text{CE}}$ and $\overline{\text{IORQ}}$ to transfer data from the SIO to the CPU.

RxDA, RxDB. Receive Data (inputs, active High). Serial data at TTL levels.

$\overline{\text{RESET}}$. Reset (input, active Low). A Low $\overline{\text{RESET}}$ disables both receivers and transmitters, forces TxDA and TxDB marking, forces the modem controls High and disables all interrupts. The control registers must be rewritten after the SIO is reset and before data is transmitted or received.

$\overline{\text{RTSA}}$, $\overline{\text{RTSB}}$. Request To Send (outputs, active Low). When the RTS bit in Write Register 5 (Figure 14) is set, the $\overline{\text{RTS}}$ output goes Low. When the $\overline{\text{RTS}}$ bit is reset in the Asynchronous mode, the output goes High after the transmitter is empty. In Synchronous modes, the $\overline{\text{RTS}}$ pin strictly follows the state of the RTS bit. Both pins can be used as general-purpose outputs.

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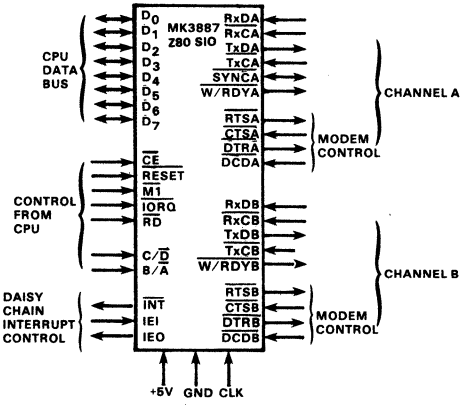
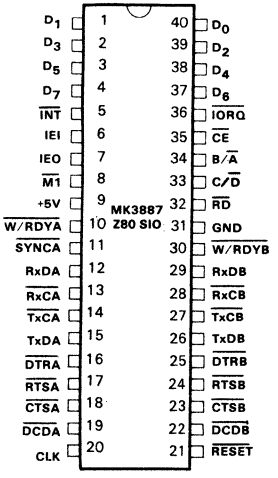
MK3887 Z80 SIO PIN FUNCTIONS
Figure 5



MK3887 Z80 SIO PIN ASSIGNMENTS
Figure 6



SYNCA, SYNCB. Synchronization (inputs/outputs, active Low). These pins can act either as inputs or outputs. In the asynchronous receive mode, they are inputs similar to CTS and DCD. In this mode, the transitions on these lines affect the state of the Sync/-Hunt status bit in Read Register 0 (Figure 13), but have no other function. In the External Sync mode, these lines also act as inputs. When external synchronization is achieved, SYNC must be driven Low on the second rising edge of RxC after that rising edge of RxC on which the last bit of the sync character was received. In other words, after the sync pattern is detected, the external logic must wait for two full Receive Clock cycles to activate the SYNC input. Once SYNC is forced Low, it should be kept Low until the CPU informs the external synchronization detect logic that synchronization has been lost or a new message is about to start. Character assembly begins on the rising edge of RxC that immediately precedes the falling edge of SYNC in the External Sync mode.

In the internal synchronization mode (Monosync and Bisync), these pins act as outputs that are active during the part of the receive clock (RxC) cycle in which sync characters are recognized. The sync condition is not latched, so these outputs are active each time a sync pattern is recognized, regardless of character boundaries.

In the MK3887 bonding option, SYNCB is omitted.

TxCA, TxCB. Transmitter Clocks (inputs). TxD changes from the falling edge of TxC. In asynchronous modes, the Transmitter Clocks may be 1, 16, 32 or 64 times the data rate; however, the clock multiplier for the transmitter and the receiver must be the same. The Transmit Clock inputs are Schmitt-trigger buffered for relaxed rise- and fall-time requirements (no noise level margin is specified). Transmitter Clocks may be driven by the Z80 CTC Counter Timer Circuit for programmable baud rate generation.
In the MK3884 bonding option, TxCB is bonded together with RxCB.

TxDA, TxDB. Transmit Data (outputs, active High). Serial data at TTL levels.

W/RDYA, W/RDYB. Wait/Ready A, Wait/Ready B (outputs, open drain, when programmed for Wait function; driven High and Low when programmed for Ready function). These dual-purpose outputs may be programmed as Ready lines for a DMA controller or as Wait lines that synchronize the CPU to the SIO data rate. The reset state is open drain.

FUNCTIONAL CAPABILITIES

The functional capabilities of the Z80 SIO can be described from two different points of view: as a data communications device, it transmits and receives serial data in a wide variety of data-communication protocols; as a Z80 family peripheral, it interacts with the Z80 CPU and other peripheral circuits, sharing the data, address and control buses, as well as being a part of the Z80 interrupt structure. As a peripheral to other microprocessors, the SIO offers valuable features such as non-vectored interrupts, polling and simple handshake capability.

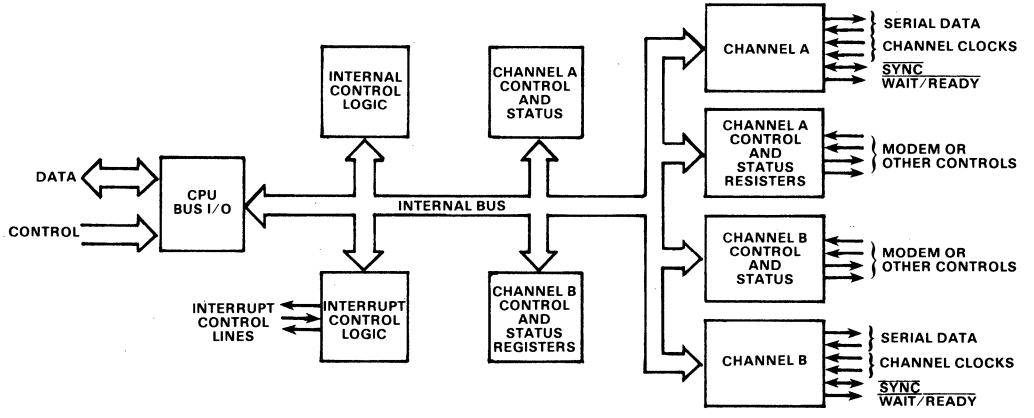
Figure 8 illustrates the conventional devices that the SIO replaces.

The first part of the following discussion covers SIO data-communication capabilities; the second part describes interactions between the CPU and the SIO.

DATA COMMUNICATION CAPABILITIES

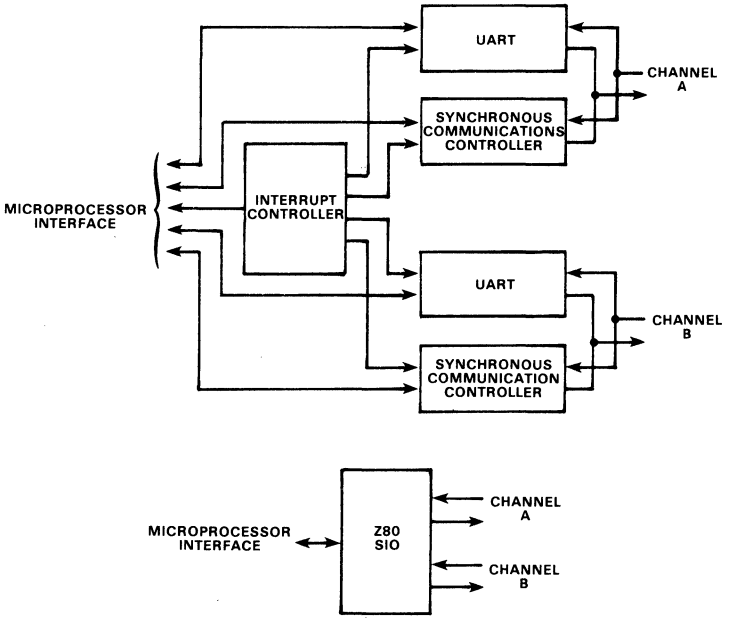
The SIO provides two independent full-duplex channels that can be programmed for use in any common asynchronous or synchronous data-communication

BLOCK DIAGRAM
Figure 7



CONVENTIONAL DEVICES REPLACED BY THE Z80 SIO

Figure 8



protocol. Figure 9 illustrates some of these protocols. The following is a short description of them. A more detailed explanation of these modes can be found in the MK3884 Z80 SIO Technical Manual.

Asynchronous Modes. Transmission and reception can be done independently on each channel with five to eight bits per character, plus optional even or odd parity. The transmitters can supply one, one-and-a-half or two stop bits per character and can provide a break output at any time. The receiver break-detection logic interrupts the CPU both at the start and end of a received break. Reception is protected from spikes by a transient spike-rejection mechanism that checks the signal one-half a bit time after a Low level is detected on the receive data input (RxDA or RxDB in Figure 5). If the Low does not persist—as in the case of a transient—the character assembly process is not started.

Framing errors and overrun errors are detected and buffered together with the partial character on which they occurred. Vectored interrupts allow fast servicing of error conditions using dedicated routines. Furthermore, a built-in checking process avoids interpreting a framing error as a new start bit: a framing error results in the addition of one-half a bit time to the point at which the search for the next start bit is begun.

The SIO does not require symmetric transmit and receive clock signals—a feature that allows it to be used with MK3882 Z80 CTC or many other clock sources. The transmitter and receiver can handle data at a rate of 1, 1/16, 1/32 or 1/64 of the clock rate supplied to the receive and transmit clock inputs. In asynchronous modes, the SYNC pin may be programmed as an input that can be used for functions such as monitoring a ring indicator.

Synchronous Modes. The SIO supports both byte-oriented and bit-oriented synchronous communication. Synchronous byte-oriented protocols can be handled in several modes that allow character synchronization with an 8-bit sync character (Monosync), any 16-bit sync pattern (Bisync) or with an external sync signal. Leading sync characters can be removed without interrupting the CPU.

Five-, six- or seven-bit sync characters are detected with 8- or 16-bit patterns in the SIO by overlapping the larger pattern across multiple in-coming sync characters, as shown in Figure 10.

CRC checking for synchronous byte-oriented modes is delayed by one character time so the CPU may disable CRC checking on specific characters. This permits implementation of protocols such as IBM Bisync.
Both CRC-16 ($X^{16} + X^{15} + X^2 + 1$) and CCITT ($X^{16} + X^{12} + X^5 + 1$) error checking polynomials are supported. In all non-SDLC modes, the CRC generator is initialized to 0's; in SDLC modes, it is initialized to 1's. The SIO can be used for interfacing to peripherals such as hard-sectored floppy disk, but it cannot generate or check CRC for IBM-compatible soft-sectored disks. The SIO also provides a feature that automatically transmits CRC data when no other data is available for transmission. This allows very high-speed transmissions under

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DMA control with no need for CPU intervention at the end of a message. When there is no data or CRC to send in synchronous modes, the transmitter inserts 8- or 16-bit sync characters regardless of the programmed character length.

The SIO supports synchronous bit-oriented protocols such as SDLC and HDLC by performing automatic flag sending, zero insertion and CRC generation. A special command can be used to abort a frame in transmission. At the end of a message the SIO automatically transmits the CRC and trailing flag when the transmit buffer becomes empty. If a transmit underrun occurs in the middle of a message, an external/status interrupt warns the CPU of this status change so that an abort may be issued. One to eight bits per character can be sent, which allows reception of a message with no prior information about the character structure in the information field of a frame.

The receiver automatically synchronizes on the leading flag of a frame in SDLC or HDLC, and provides a synchronization signal on the SYNC pin; an interrupt can also be programmed. The receiver can be programmed to search for frames addressed by a single byte to only a specified user-selected address or to a global broadcast address. In this mode, frames that do not match either the user-selected or broadcast address are ignored. The number of address bytes can be extended under software control. For transmitting data, an interrupt on the first received character or on every character can be selected. The receiver automatically deletes all zeroes inserted by the transmitter during character assembly. It also calculates and automatically checks the CRC to validate frame transmission. At the end of transmission, the status of a received frame is available in the status registers.

The SIO can be conveniently used under DMA control to provide high-speed reception or transmission. In reception, for example, the SIO can interrupt the CPU when the first character of a message is received. The CPU then enables the DMA to transfer the message to memory. The SIO then issues an end-of-frame interrupt and the CPU can check the status of the received message. Thus, the CPU is freed for other service while the message is being received.

I/O INTERFACE CAPABILITIES

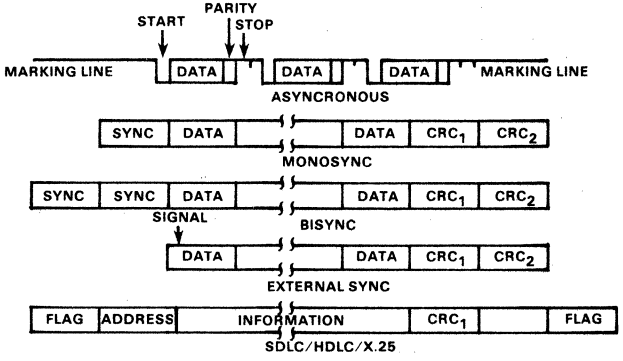
The SIO offers the choice of polling, interrupt (vectored or non-vectored) and block-transfer modes to transfer data, status and control information to and from the CPU. The block-transfer mode can also be implemented under DMA control.

Polling. Two status registers are updated at appropriate times for each function being performed (for example, CRC error-status valid at the end of a message). When the CPU is operated in a polling fashion, one of the SIO's two status registers is used to indicate whether the SIO has some data or needs some data. Depending on the contents of this register, the CPU will either write data, read data, or just go on. Two bits in the register indicate that a data transfer is needed. In addition, error and other conditions are indicated. The second status register (special receive conditions) does not have to be read in a polling sequence, until a character has been received. All interrupt modes are disabled when operating the device in a polled environment.

Interrupts. The SIO has an elaborate interrupt scheme to provide fast interrupt service in real-time applications. A control register and a status register in Channel B contain the interrupt vector. When programmed to do

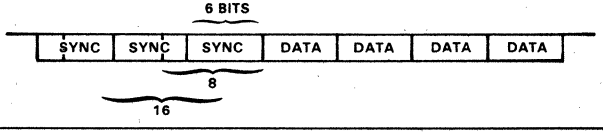
Z80 SIO PROTOCOLS

Figure 9



VARIABLE LENGTH SYNC CHARACTERS

Figure 10



so, the SIO can modify three bits of the interrupt vector in the status register so that it points directly to one of eight interrupt service routines in memory, thereby servicing conditions in both channels and eliminating most of the needs for a status-analysis routine.

Transmit interrupts, receive interrupts and external/-status interrupts are the main sources of interrupts. Each interrupt source is enabled under program control, with Channel A having a higher priority than Channel B, and with receive, transmit and external/status interrupts prioritized in that order within each channel. When the transmit interrupt is enabled, the CPU is interrupted by the transmit buffer becoming empty. (This implies that the transmitter must have had a data character written into it so it can become empty.) The receiver can interrupt the CPU in one of two ways:

- Interrupt on first received character
- Interrupt on all received characters

Interrupt-on-first-received-character is typically used with the block-transfer mode. Interrupt-on-all-received-characters has the option of modifying the interrupt vector in the event of a parity error. Both of these interrupt modes will also interrupt under special receive conditions on a character or message basis (end-of-frame interrupt in SDLC, for example). This means that the special-receive condition can cause an interrupt only if the interrupt-on-first-received--character or interrupt-on-all-received-characters mode is selected. In interrupt-on-first-received-character, an interrupt can occur from special-receive conditions (except parity error) after the first-received-character interrupt (example: receive-overrun interrupt).

The main function of the external/status interrupt is to monitor the signal transitions of the Clear To Send ($\overline{CTS}$), Data Carrier Detect ($\overline{DCD}$) and Synchronization ($\overline{SYNC}$) pins (Figures 1 through 6). In addition, an external/status interrupt is also caused by a CRC-sending condition or by the detection of a break sequence (asynchronous mode) or abort sequence (SDLC mode) in the data stream. The interrupt caused by the break/abort sequence allows the SIO to interrupt when the break/abort sequence is detected or terminated. This feature facilitates the proper termination of the current message, correct initialization of the next message, and the accurate timing of the break/-abort condition in external logic.

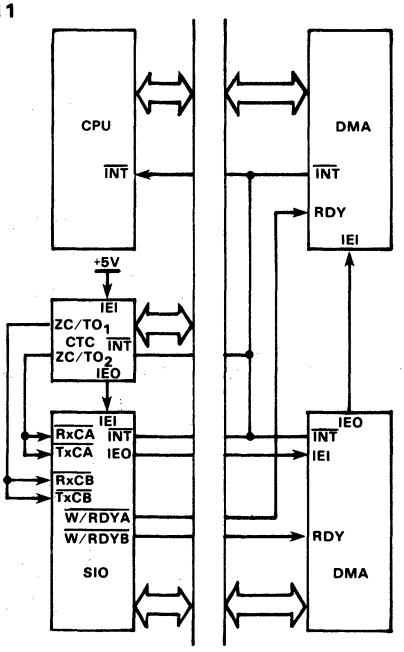
In a Z80 CPU environment (Figure 11), SIO interrupt vectoring is "automatic": the SIO passes its internally-modifiable 8-bit interrupt vector to the CPU, which adds an additional 8 bits from its interrupt-vector (I) register to form the memory address of the interrupt-routine table. This table contains the address of the beginning of the interrupt routine itself. The process entails an indirect transfer of CPU control to the interrupt routine, so that the next instruction executed after an interrupt acknowledge by the CPU is the first instruction of the interrupt routine itself.

CPU/DMA Block Transfer. The SIO's block-transfer mode accommodates both CPU block transfers and DMA controllers (Z80 DMA or other designs). The block-transfer mode uses the Wait/Ready output signal, which is selected with three bits in an internal control register. The Wait/Ready output signal can be programmed $\overline{WAIT}$ line in the CPU block-transfer mode or as a READY line in the DMA block-transfer mode.

To a DMA controller, the SIO $\overline{READY}$ output indicates that the SIO is ready to transfer data to or from memory. To the CPU, the $\overline{WAIT}$ output indicates that the SIO is not ready to transfer data, thereby requesting the CPU to extend the I/O cycle.

TYPICAL Z80 ENVIRONMENT

Figure 11



ARCHITECTURE

DESCRIPTION

The internal structure of the device includes a Z80 CPU interface, internal control and interrupt logic, and two full-duplex channels. Each channel contains its own set of control and status (write and read) registers, and control and status logic that provides the interface to modems or other external devices.

The registers for each channel are designated as follows:

WR0-WR7 — Write Registers 0 through 7
RR0-RR2 — Read Registers 0 through 2

The register group includes five 8-bit control registers,

two sync-character registers and two status registers. The interrupt vector is written into an additional 8-bit register (Write Register 2) in Channel B that may be read through another 8-bit register (Read Register 2) in Channel B. The bit assignment and functional grouping of each register is configured to simplify and organize the programming process. Table 1 lists the functions assigned to each read or write register.

Read Register Functions	
RR0	Transmit/Receive buffer status, interrupt status and external status
RR1	Special Receive Condition status
RR2	Modified interrupt vector (Channel B only)

Write Register Functions	
WR0	Register pointers, CRC initialize, initialization commands for the various modes, etc.
WR1	Transmit/Receive interrupt and data transfer mode definition.
WR2	Interrupt vector (Channel B only)
WR3	Receive parameters and control
WR4	Transmit/Receive miscellaneous parameters and modes
WR5	Transmit parameters and controls
WR6	Sync character or SDLC address field
WR7	Sync character or SDLC flag

The logic for both channels provides formats, synchronization and validation for data transferred to and from the channel interface. The modem control inputs, Clear To Send ($\overline{CTS}$) and Data Carrier Detect ($\overline{DCD}$), are monitored by the external control and status logic under program control. All external control-and-status-logic signals are general-purpose in nature and can be used for functions other than modem control.

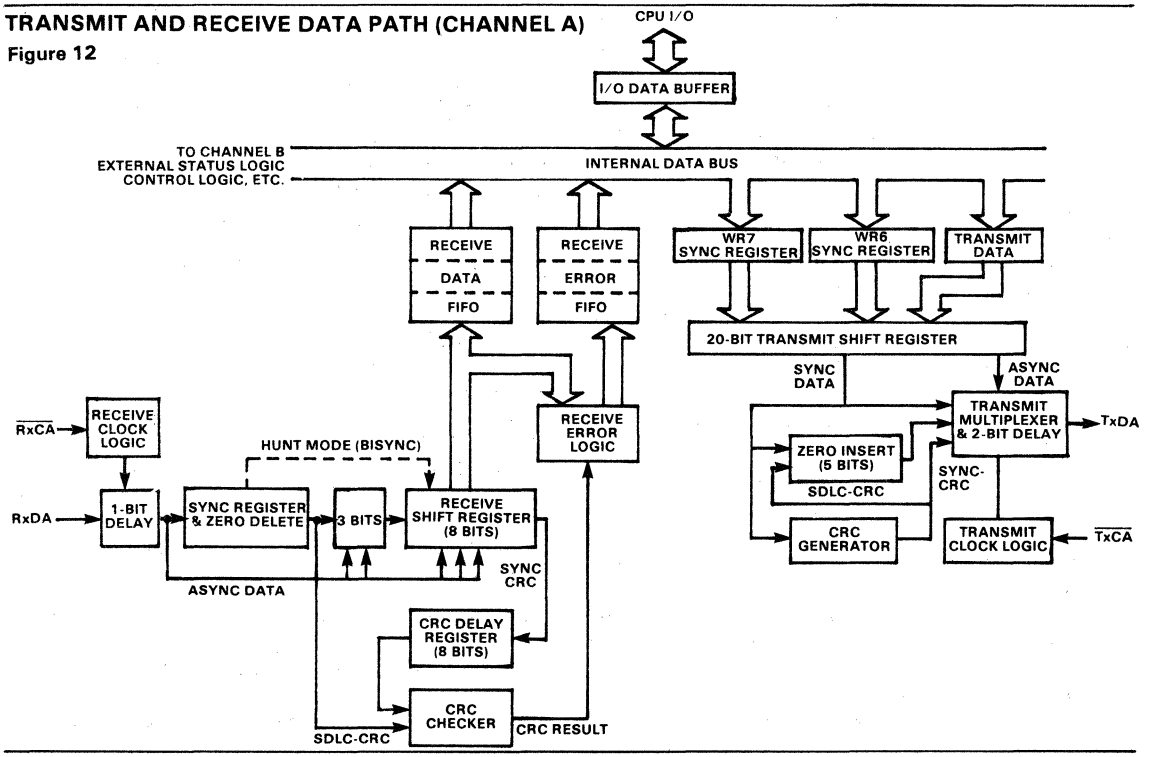
Data Path. The transmit and receive data path illustrated for Channel A in Figure 12 is identical for both channels. The receiver has three 8-bit buffer registers in a FIFO arrangement, in addition to the 8-bit receive shift register. This scheme creates additional time for the CPU to service an interrupt at the beginning of a block of high-speed data. Incoming data is routed through one of several paths (data or CRC) depending on the selected mode and—in asynchronous modes—the character length.

The transmitter has an 8-bit transmit data buffer register that is loaded from the internal data bus, and a 20-bit transmit shift register that can be loaded from the sync-character buffers or from the transmit data register. Depending on the operational mode, outgoing data is routed through one of four main paths before it is transmitted from the Transmit Data output (TxD).

The system program first issues a series of commands that initialize the basic mode of operation and then other commands that qualify conditions within the selected

TRANSMIT AND RECEIVE DATA PATH (CHANNEL A)

Figure 12



mode. For example, the asynchronous mode, character length, clock rate, number of stop bits, even or odd parity might be set first; then the interrupt mode; and finally, receiver or transmitter enable.

Both channels contain registers that must be programmed via the system program prior to operation. The channel-select input (B/$\overline{A}$) and the control/data input (C/$\overline{D}$) are the command-structure addressing controls, and are normally controlled by the CPU address bus. Figures 15 and 16 illustrate the timing relationships for programming the write registers and transferring data and status.

Read Registers. The SIO contains three read registers for Channel B and two read registers for Channel A (RR0-RR2 in Figure 13) that can be read to obtain the status information; RR2 contains the internally--modifiable interrupt vector and is only in the Channel B register set. The status information includes error conditions, interrupt vector and standard communications-interface signals.

To read the contents of a selected read register other than RR0, the system program must first write the pointer byte to WR0 in exactly the same way as a write register operation. Then, by executing a read instruction, the contents of the addressed read register can be read by the CPU.

The status bits of RR0 and RR1 are carefully grouped to simplify status monitoring. For example, when the interrupt vector indicates that a Special Receive Condition interrupt has occured, all the appropriate error bits can be read from a single register (RR1).

Write Registers. The SIO contains eight write registers for Channel B and seven write registers for Channel A (WR0-WR7 in Figure 14) that are programmed separately to configure the functional personality of the channels; WR2 contains the interrupt vector for both channels and is only in the Channel B register set. With the exception of WR0, programming the write registers requires two bytes. The first byte is to WR0 and contains three bits (D_0-D_2) that point to the selected register; the second byte is the actual control word that is written into the register to configure the SIO.

WR0 is a special case in that all of the basic commands can be written to it with a single byte. Reset (internal or external) initializes the pointer bits D_0-D_2 to point to WR0. This implies that a channel reset must always point to WR0.

The SIO must have the same clock as the CPU (same phase and frequency relationship, not necessarily the same driver).

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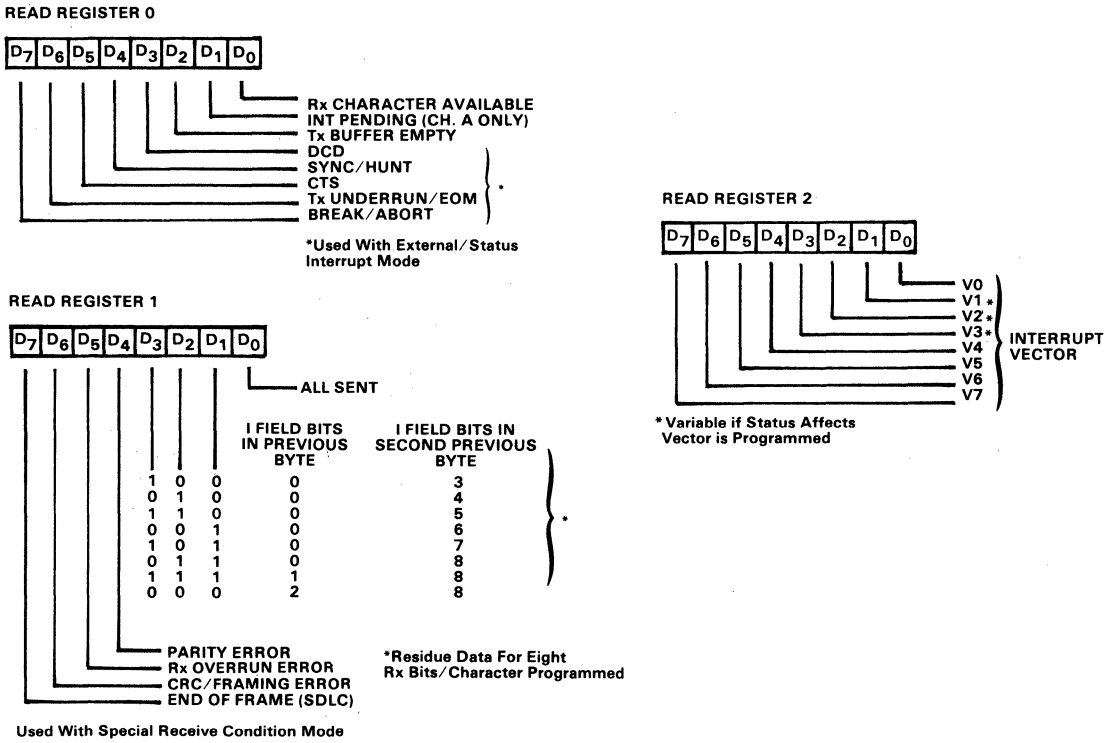
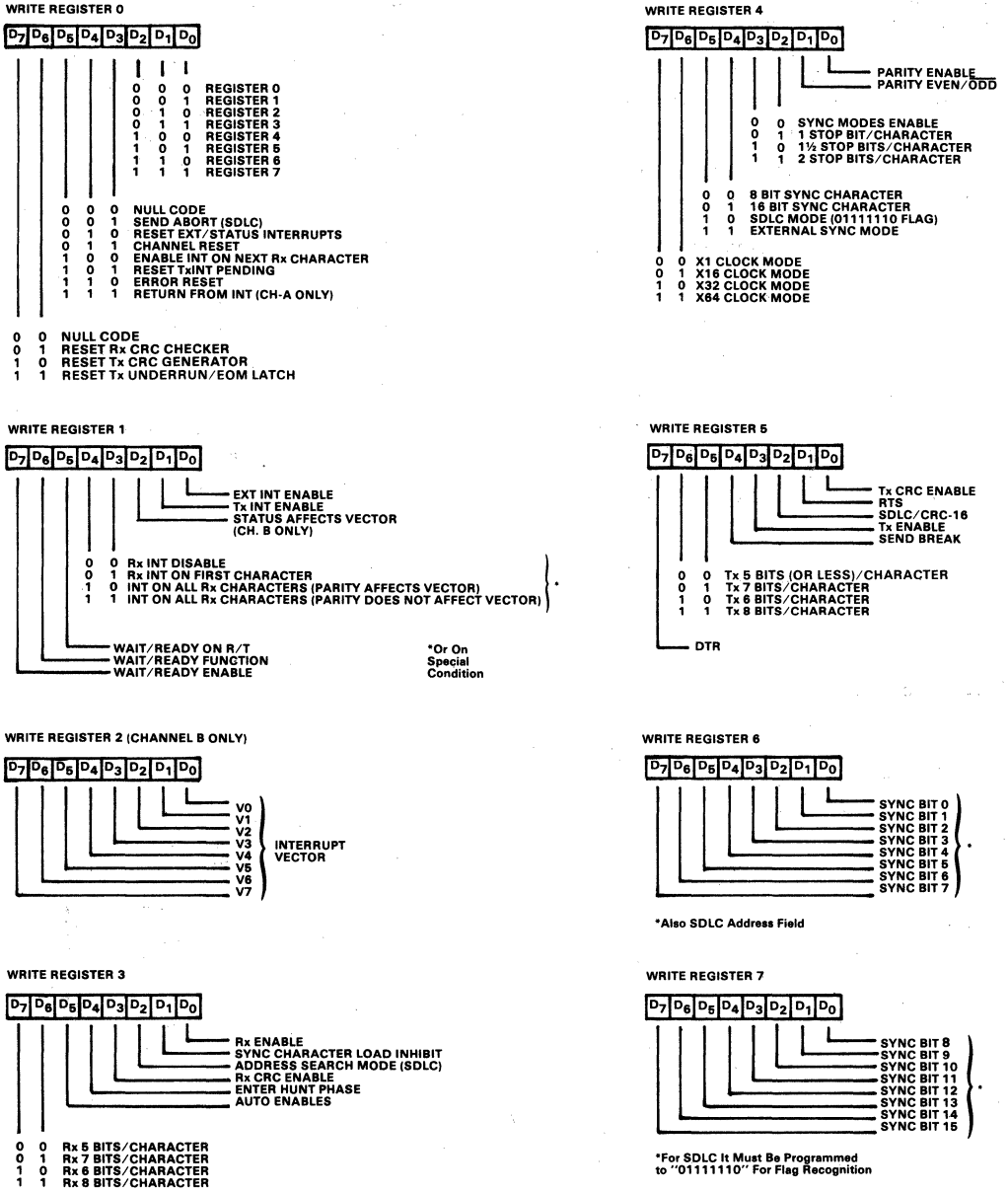
READ REGISTER BIT FUNCTIONS

Figure 13



WRITE REGISTER BIT FUNCTIONS

Figure 14



Read Cycle. The timing signals generated by a Z80 CPU input instruction to read a data or status byte from the SIO are illustrated in Figure 15.

Write Cycle. Figure 16 illustrates the timing and data signals generated by a Z80 CPU output instruction to write a data or control byte into the SIO.

Interrupt-Acknowledge Cycle. After receiving an interrupt-request signal from an SIO ($\overline{INT}$ pulled Low), the Z80 CPU sends an interrupt-acknowledge sequence ($\overline{M1}$ Low, and $\overline{IORQ}$ Low a few cycles later) as in Figure 17. The SIO contains an internal daisy-chained interrupt structure for prioritizing nested interrupts for the various functions of its two channels, and this structure can be used within an external user-defined daisy chain that prioritizes several peripheral circuits.

The IEI of the highest-priority device is terminated High. A device that has an interrupt pending or under service forces its IEO Low. For devices with no interrupt pending or under service, IEO = IEI.

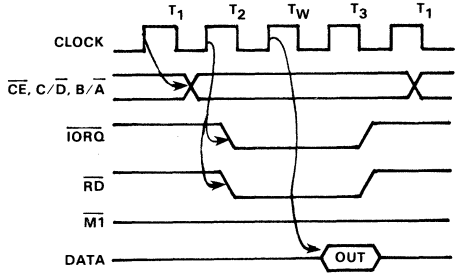
To insure stable conditions in the daisy chain, all interrupt status signals are prevented from changing while M1 is Low. When IORQ is Low, the highest priority interrupt requestor (the one with IEI High) places its interrupt vector on the data bus and sets its internal interrupt-under-service latch.

Return From Interrupt Cycle. Figure 18 illustrates the return from interrupt cycle. Normally, the Z80 CPU issues a RETI (return from interrupt) instruction at the end of an interrupt service routine. RETI is a 2-byte opcode (ED-4D) that resets the interrupt-under-service latch in the SIO to terminate the interrupt that has just been processed. This is accomplished by manipulating the daisy chain in the following way.

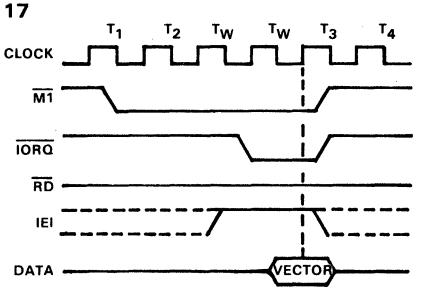
The normal daisy-chain operation can be used to detect a pending interrupt; however, it cannot distinguish between an interrupt under service and a pending unacknowledged interrupt of a higher priority. Whenever "ED" is decoded, the daisy chain is modified by forcing High the IEO of any interrupt that has not yet been acknowledged. Thus the daisy chain identifies the device presently under service as the only one with an IEI High and an IEO Low. If the next opcode byte is "4D", the interrupt-under-service latch is reset.

The ripple time of the interrupt daisy chain (both the High-to-Low and the Low-to-High transitions) limits the number of devices that can be placed in the daisy chain. Ripple time can be improved with carry-look-ahead, or by extending the interrupt-acknowledge cycle. For further information about techniques for increasing the number of daisy-chained devices, refer to the MK3880 Z80 CPU Product Specification.

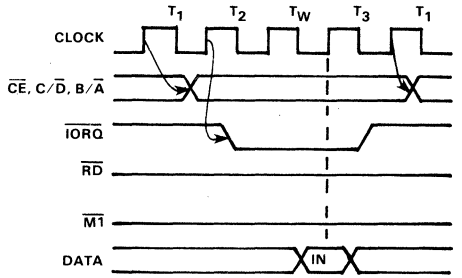
READ CYCLE
Figure 15



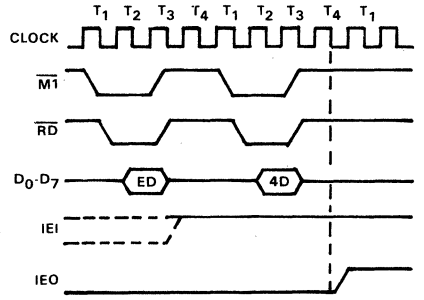
INTERRUPT ACKNOWLEDGE CYCLE
Figure 17



WRITE CYCLE
Figure 16



RETURN FROM INTERRUPT CYCLE
Figure 18



ABSOLUTE MAXIMUM RATINGS

Voltages on all inputs and outputs with respect to GND .....-0.3V to +7.0V
Operating Ambient Temperature.....As Specified in Ordering Information
Storage Temperature .....-65°C to +150°C

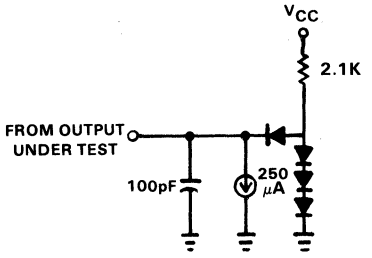
Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at an condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods ma affect device reliability.

STANDARD TEST CONDITIONS

The characteristics below apply for the following standard test conditions, unless otherwise noted. All voltages are referenced to GND. Positive current flows into the referenced pin. Standard conditions are as follows:

- $+4.75V \leq V_{CC} \leq +5.25V$
- GND = 0V
- T_A as specified in Ordering Information

All AC parameters assume a load capacitance of 100 pF max. Timing references between two output signals assume a load difference of 50 pF max.



DC CHARACTERISTICS

SYM	PARAMETER	MIN	MAX	UNIT	TEST CONDITION
V_{ILC}	Clock Input Low Voltage	-0.3	+0.80	V	
V_{IHC}	Clock Input High Voltage	V_{CC} -0.6	+5.5	V	
V_{IL}	Input Low Voltage	-0.3	+0.8	V	
V_{IH}	Input High Voltage	+2.0	+5.5	V	
V_{OL}	Output Low Voltage		+0.4	V	I_{OL} = 2.0mA
V_{OH}	Output High Voltage	+2.4		V	I_{OH} = -250 µA
I_{LI}	Input Leakage Current	-10	±10	µA	$0 < V_{IN} < V_{CC}$
I_Z	3-State Output/Data Bus Input Leakage Current	-10	+10	µA	$0 < V_{IN} < V_{CC}$
$I_{L(SY)}$	$\overline{SYNC}$ Pin Leakage Current	-40	+10	µA	$0 < V_{IN} < V_{CC}$
I_{CC}	Power Supply Current		100	mA	

Overall specified temperature and voltage range.

CAPACITANCE

SYM	PARAMETER	MIN	MAX	UNIT	TEST CONDITION
C	Clock Capacitance		40	pF	Unmeasured pins returned to ground
C_{IN}	Input Capacitance		10	pF	
C_{OUT}	Output Capacitance		10	pF	

Over specified temperature range; f = 1MHz

AC ELECTRICAL CHARACTERISTICS

See Figure 19

NUMBER	SYM	PARAMETER	MK3884		MK3884-4		UNIT
			MIN	MAX	MIN	MAX	
1	TcC	Clock Cycle Time	400	4000	250	4000	ns
2	TwCh	Clock Width (High)	170	2000	105	2000	ns
3	TfC	Clock Fall Time		30		30	ns
4	TrC	Clock Rise Time		30		30	ns
5	TwCl	Clock Width (Low)	170	2000	105	2000	ns
6	TsAD(C)	$\overline{CE}$, C/$\overline{D}$, B/$\overline{A}$ to Clock ↑ Setup Time	160		145		ns
7	TsCS(C)	$\overline{IORQ}$, $\overline{RD}$ to Clock ↑ Setup Time	240		115		ns
8	TdC(DO)	Clock ↑ to Data Out Delay		240		220	ns
9	TsDI(C)	Data In to Clock ↑ Setup (Write or M1 Cycle)	50		50		ns
10	TdRD(DOz	$\overline{RD}$ ↑ to Data Out Float Delay		230		110	ns
11	TdIO(DOI)	$\overline{IORQ}$ ↓ to Data Out Delay ($\overline{INTA}$ Cycle)		340		160	ns
12	TsM1(C)	$\overline{M1}$ to Clock ↑ Setup Time	210		90		ns
13	TsIEI(IO)	IEI to $\overline{IORQ}$ ↓ Setup Time ($\overline{INTA}$ Cycle)	200		140		ns
14	TdM1(IEO)	$\overline{M1}$ ↓ to IEO ↓ Delay (interrupt before $\overline{M1}$)		300		190	ns
15	TdIEI(IEOr)	IEI ↑ to IEO ↑ Delay (after ED decode)		150		100	ns
16	TdIEI(IEOf)	IEI ↓ to IEO ↓ Delay		150		100	ns
17	TdC(INT)	Clock ↑ to $\overline{INT}$ ↓ Delay		200		200	ns
18	TdIO (W/RWf)	$\overline{IORQ}$ ↓ or $\overline{CE}$ ↓ to $\overline{W/RDY}$ ↓ Delay (Wait Mode)		300		210	ns
19	TdC (W/RR)	Clock ↑ to $\overline{W/RDY}$ ↓ Delay (Ready Mode)		120		120	ns
20	TdC (W/RWz)	Clock ↓ to $\overline{W/RDY}$ Float Delay (Wait Mode)		150		130	ns
21	Th	Any unspecified Hold when Setup is specified	0		0		ns

NOTE: Timings are referenced from minimum V_{IH} or maximum V_{IL} for inputs and from minimum V_{OH} or maximum V_{OL} for outputs.

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AC ELECTRICAL CHARACTERISTICS (continued)

See Figure 20

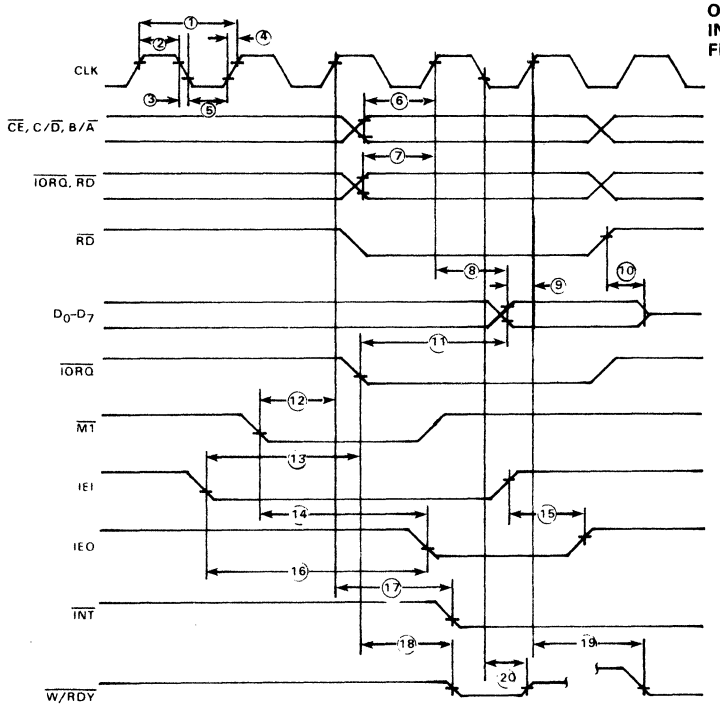
NUMBER	SYM	PARAMETER	MK3884		MK3884-4		UNIT
			MIN	MAX	MIN	MAX	
1	TwPh	Pulse Width (High)	200		200		ns
2	TwPl	Pulse Width (Low)	200		200		ns
3	TcTxC	$\overline{TxC}$ Cycle Time	400	∞	400	∞	ns
4	TwTxCl	$\overline{TxC}$ Width (Low)	180	∞	180	∞	ns
5	TwTxCh	$\overline{TxC}$ Width (High)	180	∞	180	∞	ns
6	TdTxC(TxD)	$\overline{TxC}$ ↓ to TxD Delay (x1 Mode)		400		300	ns
7	TdTxC (W/RRf)	$\overline{TxC}$ ↓ to $\overline{W/RDY}$ ↓ Delay (Ready Mode)	5	9	5	9	Clk Periods*
8	TdTxC(INT)	$\overline{TxC}$ ↓ to $\overline{INT}$ ↓ Delay	5	9	5	9	Clk Periods*
9	TcRxC	$\overline{RxC}$ Cycle Time	400	∞	400	∞	ns
10	TwRxCl	$\overline{RxC}$ Width (Low)	180	∞	180	∞	ns
11	TwRxCh	$\overline{RxC}$ Width (High)	180	∞	180	∞	ns
12	TsRxD(RxC)	RxD to $\overline{RxC}$ ↑ Setup Time (x1 Mode)	0		0		ns
13	ThRxD(RxC)	$\overline{RxC}$ ↑ to RxD Hold time (x1 Mode)	140		140		ns
14	TdRxC (W/RRf)	$\overline{RxC}$ ↑ to $\overline{W/RDY}$ ↓ Delay (Ready Mode)	10	13	10	13	Clk Periods*
15	TdRxC(INT)	$\overline{RxC}$ ↑ to $\overline{INT}$ ↓ Delay	10	13	10	13	Clk Periods*
16	TdTxC(INT)	$\overline{TxC}$ ↓ to $\overline{INT}$ ↓ Delay	5	9	5	9	Clk Periods*
17	TdRxC (SYNC)	$\overline{RxC}$ ↑ to $\overline{SYNC}$ ↓ Delay (Output Modes)	4	7	4	7	Clk Periods*
18	TsSYNC (RxC)	$\overline{SYNC}$ ↓ to $\overline{RxC}$ ↑ Setup (External Sync Modes)	-100		-100		ns

In all modes, the System Clock rate must be at least five times the maximum data rate.
RESET must be active a minimum of one complete Clock Cycle.
*System Clock

AC ELECTRICAL CHARACTERISTICS

Figure 19

	"1"	"0"
CLOCK	V_{CC}-0.6	0.8 V
OUTPUT	2.0 V	0.8 V
INPUT	2.0 V	0.8 V
FLOAT	Δ V	±0.5 V



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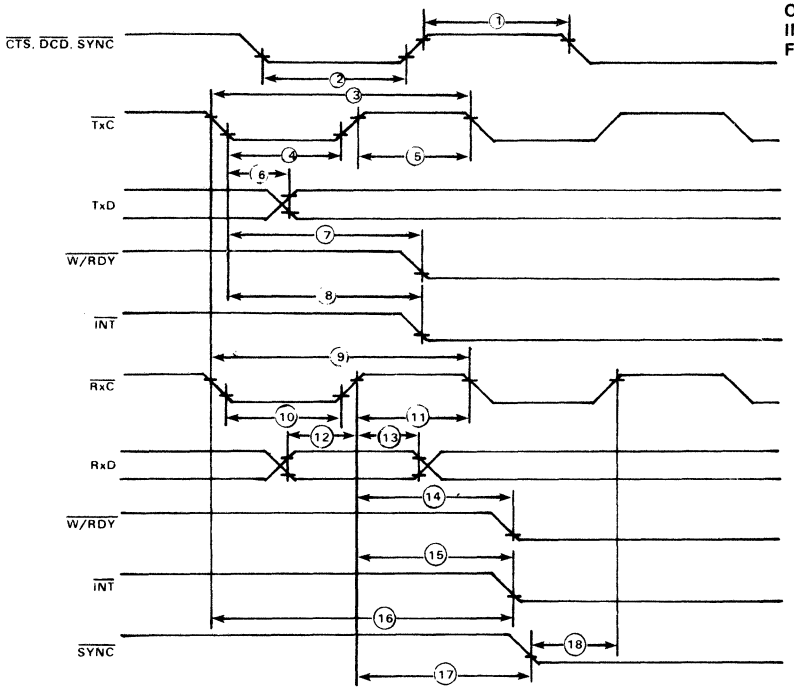
AC ELECTRICAL CHARACTERISTICS

Figure 20

	"1"	"0"
CLOCK	V_{CC}-0.6	0.8 V
OUTPUT	2.0 V	0.8 V
INPUT	2.0 V	0.8 V
FLOAT	Δ V	±0.5 V



ORDERING INFORMATION

PART NO.	PACKAGE TYPE	MAX CLOCK FREQUENCY	TEMPERATURE RANGE
MK3884N Z80-SIO	Plastic	2.5MHz	0°C to +70°C
MK3884P Z80-SIO	Ceramic	2.5MHz	0°C to +70°C
MK3884N-10 Z80-SIO	Plastic	2.5MHz	-40°C to +85°C
MK3884P-10 Z80-SIO	Ceramic	2.5MHz	-40°C to +85°C
MK3884N-4 Z80A-SIO	Plastic	4MHz	0°C to +70°C
MK3884P-4 Z80A-SIO	Ceramic	4MHz	0°C to +70°C
MK3885N Z80-SIO	Plastic	2.5MHz	0°C to +70°C
MK3885P Z80-SIO	Ceramic	2.5MHz	0°C to +70°C
MK3885N-10 Z80-SIO	Plastic	2.5MHz	-40°C to +85°C
MK3885P-10 Z80-SIO	Ceramic	2.5MHz	-40°C to +85°C
MK3885N-4 Z80A-SIO	Plastic	4MHz	0°C to +70°C
MK3885P-4 Z80A-SIO	Ceramic	4MHz	0°C to +70°C
MK3887N Z80-SIO	Plastic	2.5MHz	0°C to +70°C
MK3887P Z80-SIO	Ceramic	2.5MHz	0°C to +70°C
MK3887N-10 Z80-SIO	Plastic	2.5MHz	-40°C to +85°C
MK3887P-10 Z80-SIO	Ceramic	2.5MHz	-40°C to +85°C
MK3887N-4 Z80A-SIO	Plastic	4MHz	0°C to +70°C
MK3887P-4 Z80-SIO	Ceramic	4MHz	0°C to +70°C

NOTE: Refer to the section on pin descriptions for explanation of the differences between the MK3884, MK3885, and MK3887.

Serial Input/Output Controller
MK3884/5/7/SIO/9

FEATURES

- ☐ One full-duplex channel, with separate control and status lines for modems or other devices
- ☐ Data rates of 0 to 500K bits/second in the x1 clock mode with a 2.5 MHz clock (MK3884/5/7 Z80 SIO/9), or 0 to 800K bits/second with a 4.0 MHz clock (MK3884/5/7-4 Z80 SIO/9)
- ☐ Asynchronous protocols: everything necessary for complete messages in 5, 6, 7 or 8 bits/character. Includes variable stop bits and several clock-rate multipliers; break generation and detection; parity; overrun and framing error detection.
- ☐ Synchronous protocols: everything necessary for complete bit- or byte-oriented messages in 5, 6, 7 or 8 bits/character, including IBM Bisync, SDLC, HDLC, CCITT-X.25 and others. Automatic CRC generation/-checking, sync character and zero insertion/deletion, abort generation/detection and flag insertion.
- ☐ Receiver data registers quadruply buffered, transmitter registers doubly buffered.
- ☐ Highly sophisticated and flexible daisy-chain interrupt vectoring for interrupts without external logic.

DESCRIPTION

The MK3884/5/7 Z80 SIO/9 Serial Input/Output Controller is a single channel data communication interface with extraordinary versatility and capability. Its basic functions as a serial-to-parallel, parallel-to-serial converter/controller can be programmed by a CPU for a broad range of serial communication applications. Functionally, this device is identical to the MK3884 Z80 SIO, except that it operates in one channel only (Channel A).

The device supports all common asynchronous and synchronous protocols, byte- or bit-oriented, and performs all of the functions traditionally done by UARTs, USARTs and synchronous communication controllers combined, plus additional functions traditionally performed by the CPU. Moreover, it does this on one fully-independent channel, with an exceptionally sophisticated interrupt structure that allows very fast transfers.

Full interfacing is provided for CPU or DMA control. In addition to data communication, the circuit can handle virtually all types of serial I/O with fast (or slow) peripheral devices. While designed primarily as a member of the Z80 family, its versatility makes it well suited to many other CPUs.

The Z80 SIO/9 is an n-channel silicon-gate depletion-load device packaged in a 40-pin plastic, or ceramic DIP. It uses a

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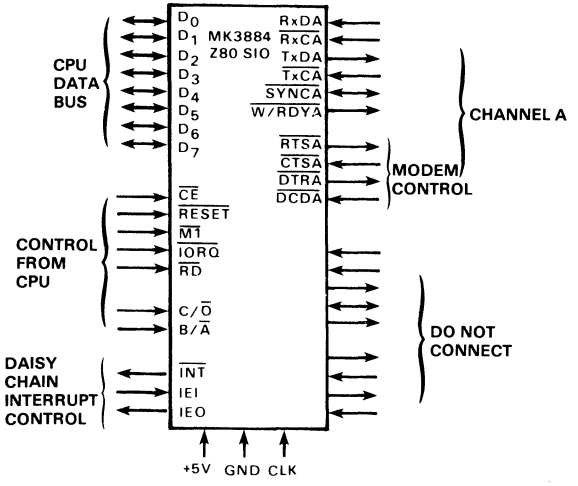
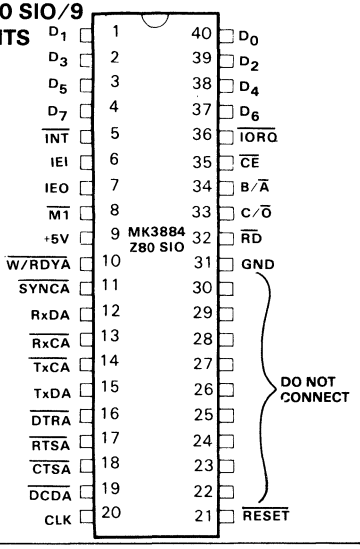
MK3884/5/7 Z80 SIO/9 PIN FUNCTIONS
Figure 1

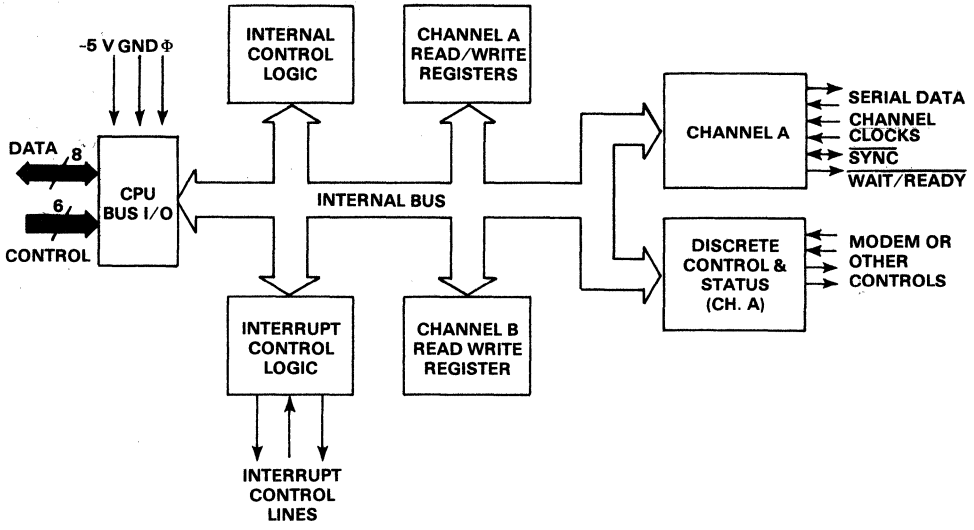


MK3884/5/7 Z80 SIO/9 PIN ASSIGNMENTS
Figure 2



Z80-SIO/9 BLOCK DIAGRAM

Figure 3



single +5V power supply and the standard Z80 family single-phase clock.

Refer to the MK3884/5/7 SIO Data Sheet and the MK3884/5/7 SIO Technical Manual for detailed functional and electrical descriptions. All functional and electrical descriptions in these publications are applicable to the SIO/9, except that Channel B cannot be used for data input or output and that pins 22 through 30 must not be connected.

Write Register 2 (Interrupt Vector) and the Status Affects Vector bit in Write Register 1 are, however, still programmed by selecting Channel B with the B/A input. All other bits in Write Register 1 or Channel B must be programmed to 0.

ORDERING INFORMATION

PART NO.	ZILOG DESIGNATOR	PACKAGE TYPE	MAX CLOCK FREQUENCY	TEMPERATURE RANGE
MK3884N SIO/9	Z80 SIO/9	Plastic	2.5 MHz	0°C to +70°C
MK3884P SIO/9	Z80-SIO/9	Ceramic	2.5 MHz	0°C to +70°C
MK3884N-4 SIO/9	Z80A-SIO/9	Plastic	4 MHz	0°C to +70°C
MK3884P-4 SIO/9	Z80A-SIO/9	Ceramic	4 MHz	0°C to +70°C
MK3885N SIO/9	Z80-SIO/9	Plastic	2.5 MHz	0°C to +70°C
MK3885P SIO/9	Z80-SIO/9	Ceramic	2.5 MHz	0°C to +70°C
MK3885N-4 SIO/9	Z80A-SIO/9	Plastic	4 MHz	0°C to +70°C
MK3885P-4 SIO/9	Z80A-SIO/9	Ceramic	4 MHz	0°C to +70°C
MK3887N SIO/9	Z80-SIO/9	Plastic	2.5 MHz	0°C to +70°C
MK3887P SIO/9	Z80-SIO/9	Ceramic	2.5 MHz	0°C to +70°C
MK3887N-4 SIO/9	Z80A-SIO/9	Plastic	4 MHz	0°C to +70°C
MK3887P-4 SIO/9	Z80A-SIO/9	Ceramic	4 MHz	0°C to +70°C

NOTE: Refer to the section on pin descriptions for explanation of the differences between the MK3884, MK3885, and MK3887 SIO/9.

MOSTEK®

Z80 MICROCOMPUTER COMPONENTS

Dual Asynchronous Receiver/Transmitter

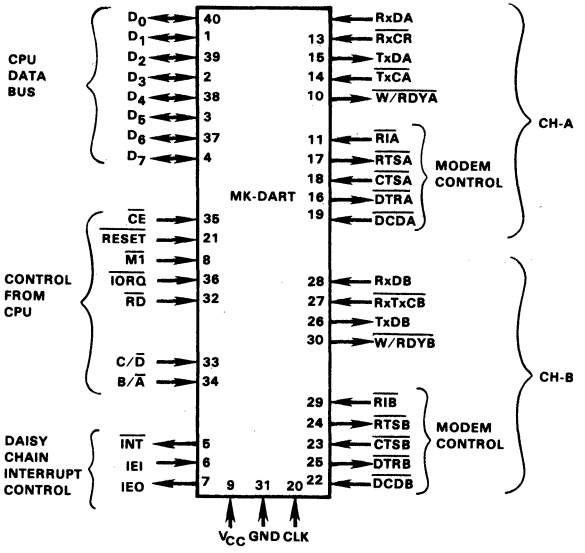
MK DART

FEATURES

- Two independent full-duplex channels with separate modem controls. Modem status can be monitored
- Receiver data registers are quadruply buffered; the transmitter is doubly buffered
- Interrupt features include a programmable interrupt vector, a "status affects vector" mode for fast interrupt processing, and the standard Z80 peripheral daisy-chain interrupt structure that provides automatic interrupt vectoring with no external logic
- In X1 clock mode, data rates are 0 to 500K bits/second with a 2.5 MHz clock, or 0 to 800K bits/second with a 4.0 MHz clock
- Programmable options include 1, 1½ or 2 stop bits; even, odd or no parity; and X1, X16, X32 and X64 clock modes
- Break generation and detection as well as parity-, overrun- and framing-error detection are available

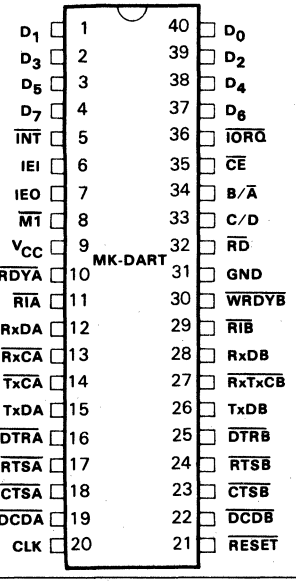
MK DART PIN FUNCTIONS

Figure 1



PIN ASSIGNMENTS

Figure 2



DESCRIPTION

The MK DART (Dual-Channel Asynchronous Receiver/Transmitter) is a dual-channel multi-function peripheral component that satisfies a wide variety of asynchronous serial data communications requirements in microcomputer systems. The MK DART is used as a serial-to-parallel, parallel-to-serial converter/controller in asynchronous applications. In addition, the device also provides modem controls for both channels. In applications where modem controls are not needed, these lines can be used for general-purpose I/O.

Mostek also offers the MK3884 Z80 SIO, a more versatile device that provides synchronous (Bisync, HDLC and SDLC) as well as asynchronous operation.

The MK DART is fabricated with n-channel silicon-gate depletion-load technology, and is packaged in a 40-pin plastic or ceramic DIP.

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PIN DESCRIPTIONS

B/$\overline{A}$. Channel A Or B Select (input, High selects Channel B). This input defines which channel is accessed during a data transfer between the CPU and the MK DART.

C/$\overline{D}$. Control Or Data Select (input, High selects Control). This input specifies the type of information (control or data) transferred on the data bus between the CPU and the MK DART.

$\overline{CE}$. Chip Enable (input, active Low). A Low at this input enables the MK DART to accept command or data input from the CPU during a write cycle, or to transmit data to the CPU during a read cycle.

CLK. System Clock (input). The MK DART uses the standard Z80 single-phase system clock to synchronize internal signals.

$\overline{CTSA}$, $\overline{CTSB}$. Clear To Send (inputs, active Low). When programmed as Auto Enables, a Low on these inputs enables the respective transmitter. If not programmed as Auto Enables, these inputs may be programmed as general-purpose inputs. Both inputs are Schmitt-trigger buffered to accommodate slow-risetime signals.

D_0-D_7. System Data Bus (bidirectional, 3-state) transfers data and commands between the CPU and the MK DART.

$\overline{DCDA}$, $\overline{DCDB}$. Data Carrier Detect (inputs, active Low). These pins function as receiver enables if the MK DART is programmed for Auto Enables; otherwise they may be used as general-purpose input pins. Both pins are Schmitt-trigger buffered.

$\overline{DTRA}$, $\overline{DTRB}$. Data Terminal Ready (outputs, active Low). These outputs follow the state programmed into the DTR bit. They can also be programmed as general-purpose outputs.

IEI. Interrupt Enable In (input, active High) is used with IEO to form a priority daisy chain when there is more than one interrupt-driven device. A High on this line indicates that no other device of higher priority is being serviced by a CPU interrupt service routine.

IEO. Interrupt Enable Out (output, active High). IEO is High only if IEI is High and the CPU is not servicing an interrupt from this MK DART. Thus, this signal blocks low priority devices from interrupting while a higher priority device is being serviced by its CPU interrupt service routine.

$\overline{INT}$. Interrupt Request (output, open drain, active Low). When the MK DART is requesting an interrupt, it pulls INT Low.

$\overline{M1}$. Machine Cycle One (input from Z80 CPU, active Low). When $\overline{M1}$ and $\overline{RD}$ are both active, the Z80 CPU is fetching an instruction from memory. When $\overline{M1}$ is active while $\overline{IORQ}$ is active, the MK DART accepts $\overline{M1}$ and $\overline{IORQ}$ as an interrupt acknowledge of the MK DART is the highest priority device that has interrupted the Z80 CPU.

$\overline{IORQ}$. Input/Output Request (input from CPU, active Low). $\overline{IORQ}$ is used in conjunction with B/$\overline{A}$, C/$\overline{D}$, $\overline{CE}$ and $\overline{RD}$ to transfer commands and data between the CPU and the MK DART. When $\overline{CE}$, $\overline{RD}$ and $\overline{IORQ}$ are all active, the channel selected by B/$\overline{A}$ transfers data to the CPU (a read operation). When $\overline{CE}$ and $\overline{IORQ}$ are active, but $\overline{RD}$ is inactive, the channel selected by B/$\overline{A}$ is written to by the CPU with either data or control information as specified by C/$\overline{D}$.

$\overline{RxCA}$, $\overline{RxCB}$. Receiver Clocks (inputs). Receive data is sampled on the rising edge of RxC. The Receive Clocks may be 1, 16, 32, or 64 times the data rate.

$\overline{RD}$. Read Cycle Status. (input from CPU, active Low). If $\overline{RD}$ is active, a memory or I/O read operation is in progress.

RxDA, RxDB. Receive Data (inputs, active High).

$\overline{RESET}$. Reset (input, active Low). Disables both receivers and transmitters, forces TxDA and TxDB marking, forces the modem controls High, and disables all interrupts.

$\overline{RIA}$, $\overline{RIB}$. Ring Indicator (inputs, active Low). These inputs are similar to $\overline{CTS}$ and $\overline{DCD}$. The MK DART detects both logic level transitions and interrupts the CPU. When not used in switched-line applications, these inputs can be used as general-purpose inputs.

$\overline{RTSA}$, $\overline{RTSB}$. Request to Send (outputs, active Low). When the RTS bit is set, the RTS output goes Low. When the RTS bit is reset, the output goes High after the transmitter empties.

$\overline{TxCA}$, $\overline{TxCB}$. Transmitter Clocks (inputs). TxD changes on the falling edge of TxC. The Transmitter Clocks may be 1, 16, 32, or 64 times the data rate; however, the clock multiplier for the transmitter and the receiver must be the same. The Transmit Clock inputs are Schmitt-trigger buffered for relaxed rise and fall time requirements (no noise level margin is specified). Both the Receiver and Transmitter Clocks may be driven by the MK3882 Counter Timer Circuit for programmable baud rate generation.

TxDA, TxDB. Transmit Data (outputs, active High).

$\overline{W/RDYA}$, $\overline{W/RDYB}$. Wait/Ready (outputs, open drain when programmed for Wait function, driven High and Low when programmed for Ready function). These dual-purpose outputs may be programmed as Ready lines for a DMA controller or as Wait lines that synchronize the CPU to the MK DART data rate. The reset state is open drain.

The functional capabilities of the MK DART can be described from two different points of view: as a data communications device, it transmits and receives serial data, and meets the requirements of asynchronous data communications protocols; as a Z80 family peripheral, it

interacts with the Z80 CPU and other Z80 peripheral circuits, and shares the data, address, and control buses, as well as being a part of the Z80 interrupt structure. As a peripheral to other microprocessors, the MK DART offers valuable features such as non-vectored interrupts, polling, and simple handshake capability.

The first part of the following functional description introduces MK DART data communications capabilities; the second part describes the interaction between the CPU and the MK DART.

COMMUNICATIONS CAPABILITIES

The MK DART provides two independent full-duplex channels for use as an asynchronous receiver/transmitter. The MK DART offers transmission and reception of five to eight bits per character, plus optional even or odd parity. The transmitter can supply one, one and a half, or two stop bits per character and can provide a break output at any time. The receiver break detection logic interrupts the CPU both at the start and end of a received break. Reception is protected from spikes by a transient spike rejection mechanism that checks the signal at one-half a bit time after a Low level is detected on the Receive Data input. If the Low does not persist—as in the case of a transient—the character assembly process is not started.

Framing errors and overrun errors are detected and buffered together with the character on which they occurred. Vectored interrupts allow fast servicing of interrupting conditions using dedicated routines. Furthermore, a built-in checking process avoids interpreting a framing error as a new start bit: a framing error results in the addition of one-half a bit time to the point at which the search for the next start bit is begun.

The MK DART does not require symmetric Transmit and Receive Clock signals—a feature that allows it to be used with a MK3882 or any other clock source. The transmitter and receiver can handle data at a rate of 1, 1/16, 1/32, or 1/64 of the clock rate supplied to the Receive and Transmit Clock inputs. When using Channel B, the bit rates for transmit and receive operations must be the same because RxC and TxC are bonded together (RxTxCB).

I/O INTERFACE CAPABILITIES

The MK DART offers the choice of Polling, Interrupt (vectored or non-vectored), and Block Transfer modes to transfer data, status, and control information to and from the CPU. The Block Transfer mode can be implemented under CPU or DMA control.

POLLING

There are no interrupts in the Polled mode. Status registers RR0 and RR1 are updated at appropriate times for each function being performed. All the interrupt modes of the MK DART must be disabled to operate the device in a polled environment.

While in its Polling sequence, the CPU examines the status contained in RR0 for each channel; the RR0 status bits serve as an acknowledge to the Poll inquiry. The two RR0 status bits D_0 and D_2 indicate that a data transfer is needed. The status also indicates Error or other special status conditions (see "MK DART Programming"). The Special Receive Condition status contained in RR1 does not have to be read in a Polling sequence because the status bits in RR1 are accompanied by a Receive Character Available status in RR0.

INTERRUPTS

The MK DART offers an elaborate interrupt scheme that provides fast interrupt response in real-time applications. As a member of the Z80 family, the MK DART can be daisy-chained along with other Z80 peripherals for peripheral interrupt-priority resolution. In addition, the

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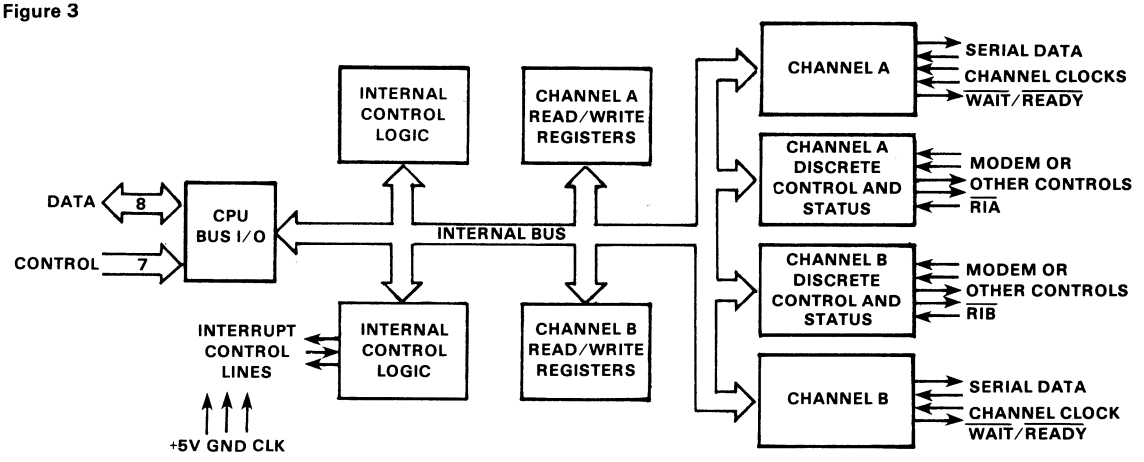
BLOCK DIAGRAM

Figure 3



internal interrupts of the MK DART are nested to prioritize the various interrupts generated by Channels A and B. Channel B registers, WR2 and RR2, contain the interrupt vector that points to an interrupt service routine in the memory. To eliminate the necessity of writing a status analysis routine, the MK DART can modify the interrupt vector in RR2 so it points directly to one of eight interrupt service routines. This is done under program control by setting a program bit (WR1, D_2) in Channel B, called "Status Affects Vector." When this bit is set, the interrupt vector in RR2 is modified according to the assigned priority of the various interrupting conditions.

Transmit interrupts, Receive interrupts and External/Status interrupts are the main sources of interrupts. Each interrupt source is enabled under program control with Channel A having a higher priority than Channel B, and with Receiver, Transmit, and External/Status interrupts prioritized in that order within each channel. When the Transmit interrupt is enabled, the CPU is interrupted by the transmit buffer. (This implies that the transmitter must have had a data character written into it so it can become empty.) When enabled, the receiver can interrupt the CPU in one of three ways:

- Interrupt on the first received character
- Interrupt on all received characters
- Interrupt on a Special Receive condition

Interrupt On the First Character is typically used with the Block Transfer mode. Interrupt On All Received Characters can optionally modify the interrupt vector in the event of a parity error. The Special Receive Condition interrupt can occur on a character basis. The Special Receive condition can cause an interrupt only if the Interrupt On First Received Character or Interrupt On All Received Characters' mode is selected. In Interrupt On the First Received Character, an interrupt can occur from Special Receive conditions (except Parity Error) after the first receive character interrupt (example: Receive Overrun interrupt).

The main function of the External/Status interrupt is to monitor the signal transitions of the $\overline{CTS}$, $\overline{DCD}$ and $\overline{RI}$ pins; however, an External/Status interrupt is also caused by the detection of a Break sequence in the data stream. The interrupt caused by the Break sequence has a special feature that allows the MK DART to interrupt when the Break sequence is detected or terminated. This feature facilitates the proper termination of the current message, correct initialization of the next message, and the accurate timing of the Break condition.

CPU, DMA BLOCK TRANSFER

The MK DART provides a Block Transfer to accommodate CPU block transfer functions and DMA block transfers (Z80 DMA or other designs). The Block Transfer mode uses the $\overline{W/RDY}$ output in conjunction with the Wait/Ready bits of Write Register 1. The $\overline{W/RDY}$ output can be defined under software control as a Wait line in the CPU Block Transfer mode or as a Ready line in the DMA Block Transfer mode. To a DMA controller, the MK DART Ready output indicates that the MK DART is ready to transfer data to or from memory. To the CPU, the Wait output indicates that the MK DART is not ready to transfer data, thereby requesting the CPU to extend the I/O cycle.

INTERNAL ARCHITECTURE

The device internal structure includes a Z80 CPU interface, internal control and interrupt logic, and two full-duplex channels. Each channel contains read and write registers, and discrete control and status logic that provides the interface to modems or other external devices.

The read and write register group includes five 8-bit control registers and two status registers. The interrupt vector is written into an additional 8-bit register (Write Register 2) in Channel B that may be read through Read Register 2 in Channel B. The registers for both channels are designated as follows:

WR0-WR5 - Write Registers 0 through 5
RR0-RR2 - Read Registers 0 through 2

The bit assignment and functional grouping of each register are configured to simplify and organize the programming process.

The logic for both channels provides formats, bit synchronization, and validation for data transferred to and from the channel interface. The modem control inputs Clear to Send ($\overline{CTS}$), Data Carrier Detect ($\overline{DCD}$) and Ring Indicator ($\overline{RI}$) are monitored by the control logic under program control. All the modem control signals are general purpose in nature and can be used for functions other than modem control.

For automatic interrupt vectoring, the interrupt control logic determines which channel and which device within the channel has the highest priority. Priority is fixed with Channel A assigned a higher priority than Channel B; Receive, Transmit and External/Status interrupts are prioritized in that order within each channel.

DATA PATH

The transmit and receive data path illustrated for Channel A in Figure 4 is identical for both channels. The receiver has three 8-bit buffer registers in a FIFO arrangement in addition to the 8-bit receive shift register. This scheme creates additional time for the CPU to service a Receive Character Available interrupt in a high-speed data transfer.

The transmitter has an 8-bit transmit data register that is loaded from the internal data bus, and a 9-bit transmit shift register that is loaded from the transmit data register.

READ CYCLE

The timing signals generated by a Z80 CPU input instruction to read a Data or Status byte from the MK-DART are illustrated in Figure 5.

WRITE CYCLE

Figure 6 illustrates the timing and data signals generated by a Z80 CPU output instruction to write a Data or Control byte into the MK DART.

INTERRUPT ACKNOWLEDGE CYCLE

After receiving an Interrupt Request signal ($\overline{INT}$ pulled Low), the Z80 CPU sends an Interrupt Acknowledge signal ($\overline{M1}$ and $\overline{IORQ}$ both Low). The daisy-chained interrupt circuits determine the highest priority interrupt requestor. The IEI of the highest priority peripheral is terminated High. For any peripheral that has no interrupt pending or under service, IEO = IEI. Any peripheral that does have an interrupt pending or under service forces its IEO Low.

To ensure stable conditions in the daisy chain, all interrupt status signals are prevented from changing while $\overline{M1}$ is Low. When $\overline{IORQ}$ is Low coincidental with $\overline{M1}$ Low, the highest priority interrupt requestor (the one with IEI High) places its interrupt vector on the data bus and sets its internal interrupt-under-service latch.

Refer to the Z80 SIO Technical Manual for additional details on the interrupt daisy chain and interrupt nesting.

RETURN FROM INTERRUPT CYCLE

Normally, the Z80 CPU issues a RETI (RETurn from Interrupt) instruction at the end of an interrupt service routine. RETI is a 2-byte opcode (ED-4D) that resets the interrupt-under-service latch to terminate the interrupt that has just been processed.

When used with other CPUs, the MK DART allows the user to return from the interrupt cycle with a special command called "Return From Interrupt" in Write Register 0 of Channel A. This command is interpreted by the MK DART in exactly the same way it would interpret an RETI command on the data bus.

MK DART PROGRAMMING

To program the MK DART, the system program first issues a series of commands that initialize the basic mode and then other commands that qualify conditions within the selected mode. For example, the character length, clock rate, number of stop bits, even or odd parity are first set, then the interrupt mode and, finally, receiver or transmitter enable.

Both channels contain command registers that must be programmed via the system program prior to operation. The Channel Select input (B/$\overline{A}$) and the Control/Data input (C/$\overline{D}$) are the command structure addressing controls, and are normally controlled by the CPU address bus.

WRITE REGISTERS

The MK DART contains six registers (WR0-WR5) in each channel that are programmed separately by the system program to configure the functional personality of the channels (Figure 4). With the exception of WR0, programming the write registers requires two bytes. The first byte contains three bits (D_0-D_2) that point to the selected register; the second byte is the actual control word that is written into the register to configure the MK DART.

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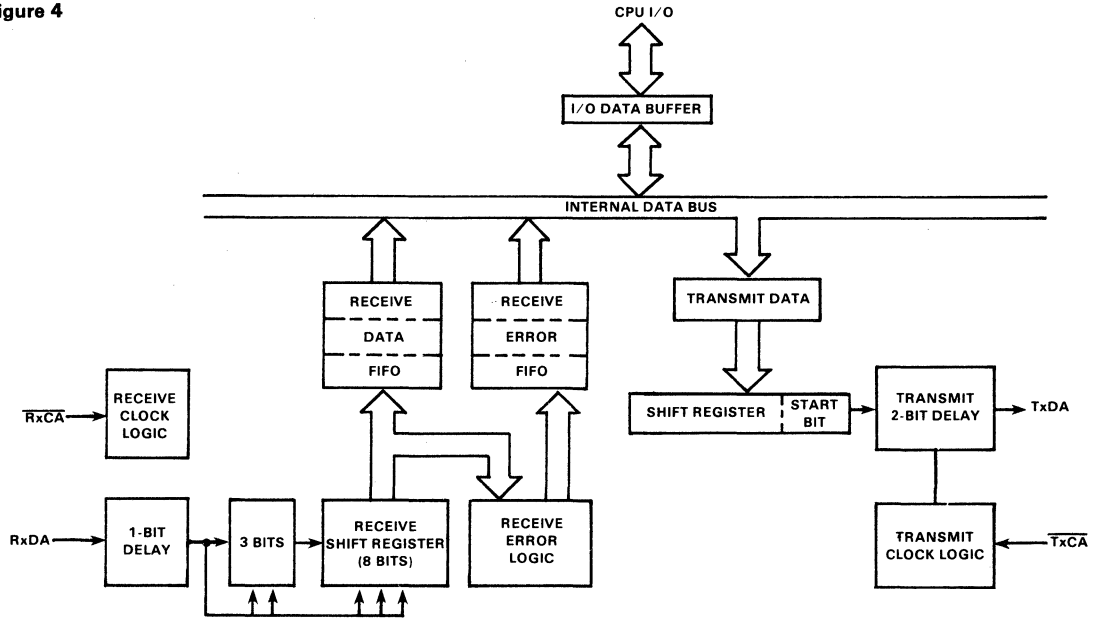
DATA PATH

Figure 4



WR0 is a special case in that all the basic commands (CMD_0-CMD_2) can be accessed with a single byte. Reset (internal or external) initializes the pointer bits D_0-D_2 to point to WR0. This means that a register cannot be pointed to in the same operation as a channel reset.

READ REGISTERS

The MK DART contains three registers (RR0-RR2) that can be read to obtain the status information for each channel (except for RR2, which applies to Channel B only). The status information includes error conditions, interrupt vector, and standard communications-interface signals.

To read the contents of a selected read register other than RR0, the system program must first write the pointer byte to WR0 in exactly the same way as a write register operation. Then, by executing an input instruction, the contents of the addressed read register can be read by the CPU.

The status bits of RR0 and RR1 are carefully grouped to simplify status monitoring. For example, when the interrupt vector indicates that a Special Receive Condition interrupt has occurred, all the appropriate error bits can be read from a single register (RR1).

WRITE REGISTER FUNCTIONS

Table 1

WR0	Register pointers, initialization commands for the various modes, etc.
WR1	Transmit/Receive interrupt and data transfer mode definition.
WR2	Interrupt vector (Channel B only)
WR3	Receive parameters and control
WR4	Transmit/Receive miscellaneous parameters and modes
WR5	Transmit parameters and controls

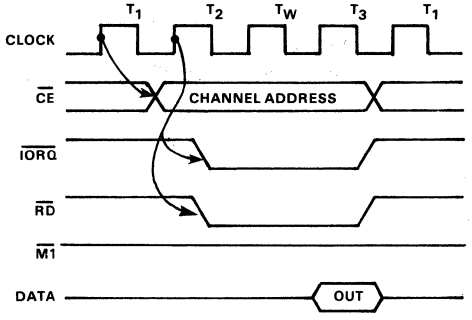
READ REGISTER FUNCTIONS

Table 2

RR0	Transmit/Receive buffer status, interrupt status and external status
RR1	Special Receive Condition status
RR2	Modified interrupt vector (Channel B only)

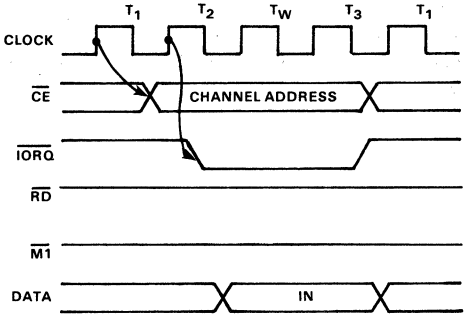
READ CYCLE

Figure 5



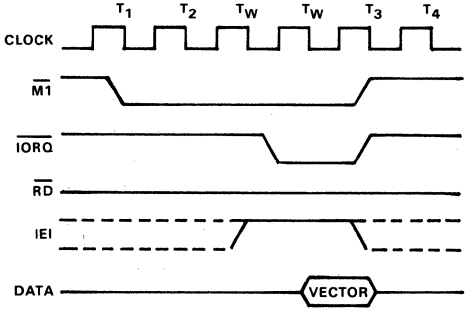
WRITE CYCLE

Figure 6



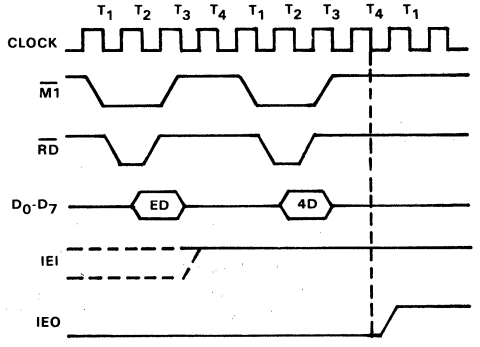
INTERRUPT ACKNOWLEDGE CYCLE

Figure 7



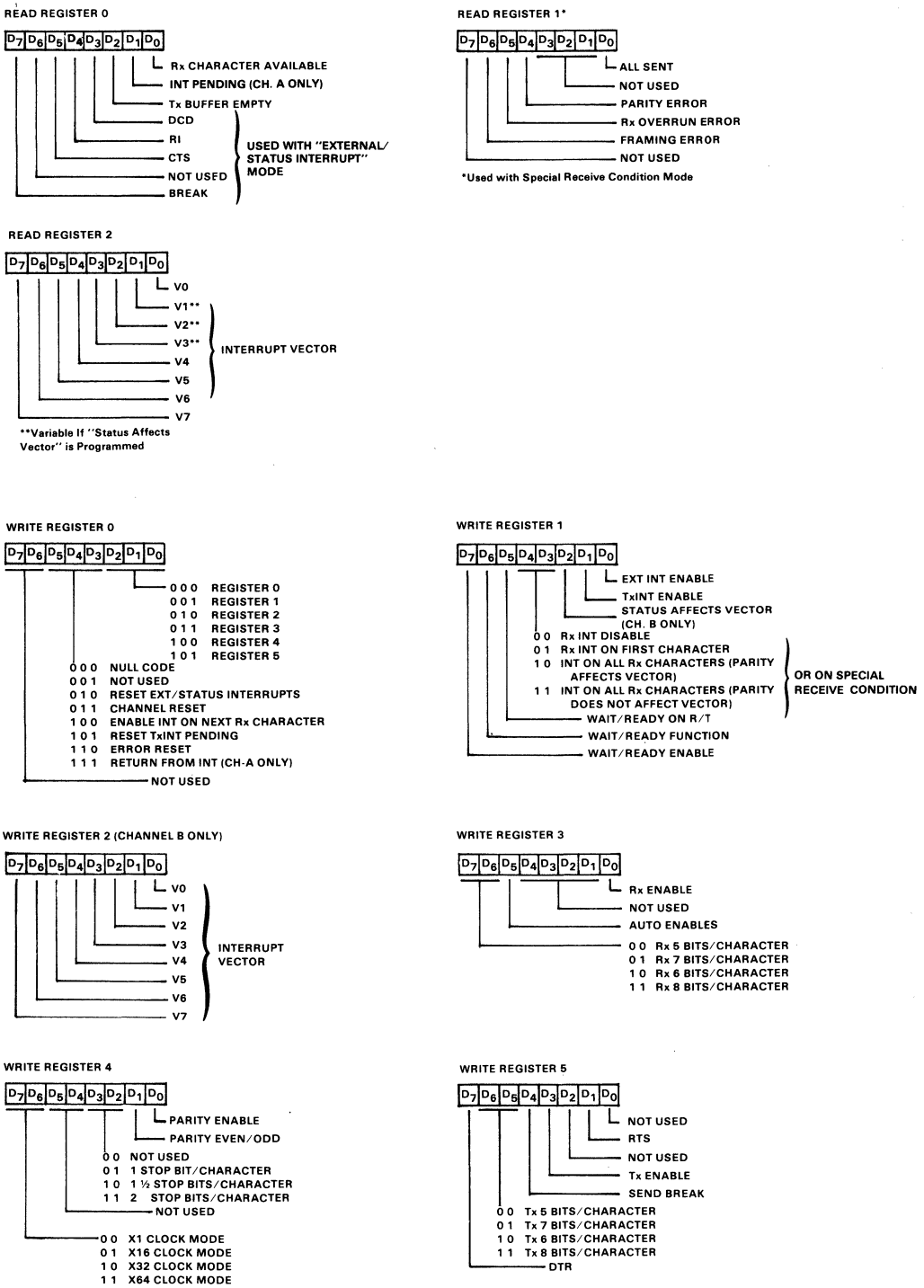
RETURN FROM INTERRUPT CYCLE

Figure 8



MK-DART READ AND WRITE REGISTERS

Figure 9



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ABSOLUTE MAXIMUM RATINGS

Voltages on all inputs and outputs with respect to GND ..... -0.3 V to +7.0 V
Operating Ambient Temperature ..... As Specified in Ordering Information
Storage Temperature ..... -65°C to +150°C
Power Dissipation ..... 1.5 W

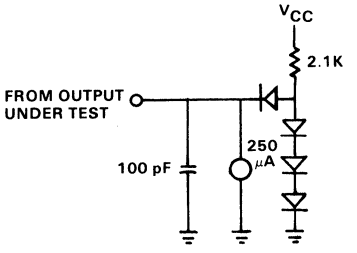
Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

STANDARD TEST CONDITIONS

The characteristics below apply for the following standard test conditions, unless otherwise noted. All voltages are referenced to GND. Positive current flows into the referenced pin. Standard conditions are as follows:

- $+4.75V \leq V_{CC} \leq +5.25V$
- GND = 0V
- T_A as specified in Ordering Information

All AC parameters assume a load capacitance of 100pF max. Timing references between two output signals assume a load difference of 50pF max.



DC CHARACTERISTICS

SYM	PARAMETER	MIN	MAX	UNIT	TEST CONDITION
V_{ILC}	Clock Input Low Voltage	-0.3	+0.80	V	
V_{IHC}	Clock Input High Voltage	V_{CC}-0.6	+5.5	V	
V_{IL}	Input Low Voltage	-0.3	+0.8	V	
V_{IH}	Input High Voltage	+2.0	+5.5	V	
V_{OL}	Output Low Voltage		+0.4	V	I_{OL} = 2.0 mA
V_{OH}	Output High Voltage	+2.4		V	I_{OH} = -250μA
I_L	Input/3-State Output Leakage Current	-10	+10	μA	0.4 < V < 2.4 V
$I_{L(RI)}$	RI Pin Leakage Current	-40	+10	μA	0.4 < V < 2.4 V
I_{CC}	Power Supply Current		100	mA	

CAPACITANCE

SYM	PARAMETER	MIN	MAX	UNIT	TEST CONDITION
C	Clock Capacitance		40	pF	Unmeasured
C_{IN}	Input Capacitance		10	pF	pins returned
C_{OUT}	Output Capacitance		10	pF	to ground

Over specified temperature range; f = 1 MHz

AC CHARACTERISTICS
See Figure 8.1

NO	SYM	PARAMETER	MK DART		MK DART-4		UNIT
			MIN	MAX	MIN	MAX	
1	TcC	Clock Cycle Time	400	4000	250	4000	ns
2	TwCh	Clock Width (High)	170	2000	105	2000	ns
3	TfC	Clock Fall Time		30		30	ns
4	TrC	Clock Rise Time		30		30	ns
5	TwCl	Clock Width (Low)	170	2000	105	2000	ns
6	TsAD(C)	$\overline{CE}$, C/$\overline{D}$, B/$\overline{A}$ to Clock ↑ Setup Time	160		145		ns
7	TsCS(C)	$\overline{IORQ}$, $\overline{RD}$ to Clock ↑ Setup Time	240		115		ns
8	TdC(DO)	Clock ↑ to Data Out Delay		240		220	ns
9	TsDI(C)	Data In to Clock ↑ Setup Time	50		50		ns
10	TdRD(DOz)	$\overline{RD}$ ↑ to Data Out Float Delay		230		110	ns
11	TdIO(DOI)	$\overline{IORQ}$ ↓ to Data Out Delay (INTA Cycle)		340		160	ns
12	TsM1(C)	$\overline{M1}$ ↓ to Clock ↑ Setup Time	210		90		ns
13	TsIEI(IO)	IEI to $\overline{IORQ}$ ↓ Setup Time (INTA Cycle)	200		140		ns
14	TdM1(IEO)	$\overline{M1}$ ↓ to IEO ↓ Delay (Interrupt immediately preceeding $\overline{M1}$)		300		190	ns
15	TdIEI(IEOr)	IEI ↑ to IEO ↑ Delay (after ED decode)		150		100	ns
16	TdIEI(IEOf)	IEI ↓ to IEO ↓ Delay		150		100	ns
17	TdC(INT)	Clock ↑ to $\overline{INT}$ ↓ Delay		200		200	ns
18	TdIO (W/RWf)	$\overline{IORQ}$ ↓ or $\overline{CE}$ ↓ to $\overline{W/RDY}$ ↓ Delay (Wait Mode)		300		210	ns
19	TdC(W/RR)	Clock ↑ to $\overline{W/RDY}$ ↓ Delay (Ready Mode)		120		120	ns
20	TdC (W/RWz)	Clock ↓ to $\overline{W/RDY}$ Float Delay (Wait Mode)		150		130	ns

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AC CHARACTERISTICS
See Figure 8.2

NO	SYM	PARAMETER	MK DART		MK DART-4		UNIT
			MIN	MAX	MIN	MAX	
1	TwPh	Pulse Width (High)	200		200		ns
2	TwPl	Pulse Width (Low)	200		200		ns
3	TcTxC	$\overline{TxC}$ Cycle Time	400	∞	400	∞	ns
4	TwTxCl	$\overline{TxC}$ Width (Low)	180	∞	180	∞	ns
5	TwTxCh	$\overline{TxC}$ Width (High)	180	∞	180	∞	ns
6	TdTxC(TxD)	$\overline{TxC}$ ↓ to TxD Delay		400		300	ns
7	TdTxC (W/RRf)	$\overline{TxC}$ ↓ to $\overline{W/RDY}$ ↓ Delay	5	9	5	9	Clk Periods
8	TdTxC(INT)	$\overline{TxC}$ ↓ to $\overline{INT}$ ↓ Delay	5	9	5	9	Clk Periods
9	TcRxC	$\overline{RxC}$ Cycle Time	400	∞	400	∞	ns
10	TwRxCl	$\overline{RxC}$ Width (Low)	180	∞	180	∞	ns
11	TwRxCh	$\overline{RxC}$ Width (High)	180	∞	180	∞	ns
12	TsRxD(RxC)	RxD to $\overline{RxC}$ ↑ Setup Time (X1 Mode)	0		0		ns
13	ThRxD(RxC)	RxD Hold Time (xl Mode)	140		140		ns
14	TdRxC (W/RRf)	$\overline{RxC}$ ↑ to $\overline{W/RDY}$ ↓ Delay (Ready Mode)	10	13	10	13	Clk Periods
15	TdRxC(INT)	$\overline{RxC}$ ↑ to $\overline{INT}$ ↓ Delay	10	13	10	13	Clk Periods

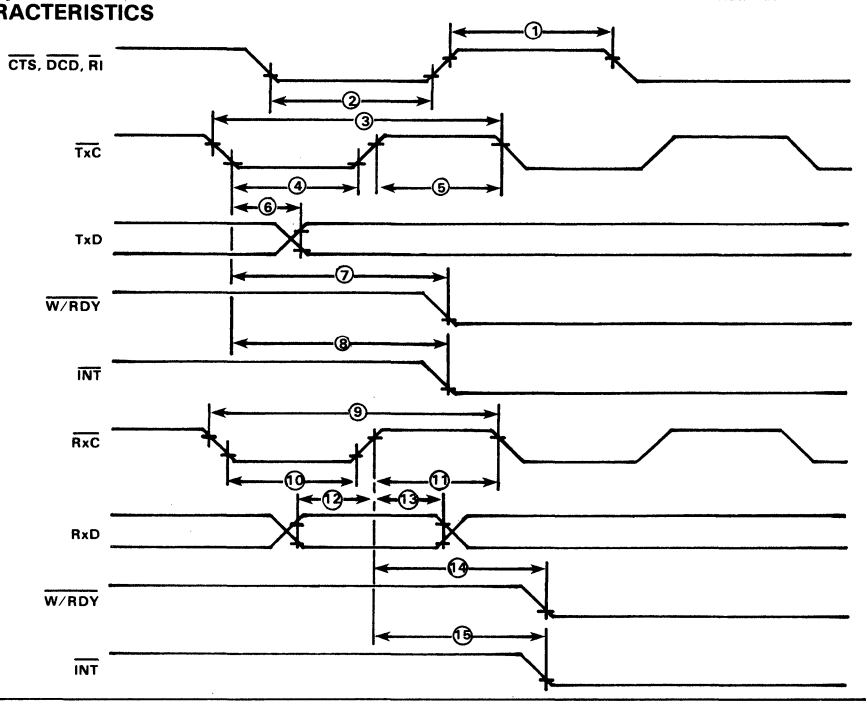
In all modes, the Clock rate must be at least five times the maximum data rate.
RESET must be active a minimum of one complete Clock Cycle.

ORDERING INFORMATION

PART NUMBER	MAXIMUM CLOCK RATE	TEMPERATURE RANGE	PACKAGE
MK DART N	2.5 MHz	0°C to 70°C	Plastic
MK DART P	2.5 MHz	0°C to 70°C	Ceramic
MK DART N-4	4.0 MHz	0°C to 70°C	Plastic
MK DART P-4	4.0 MHz	0°C to 70°C	Ceramic

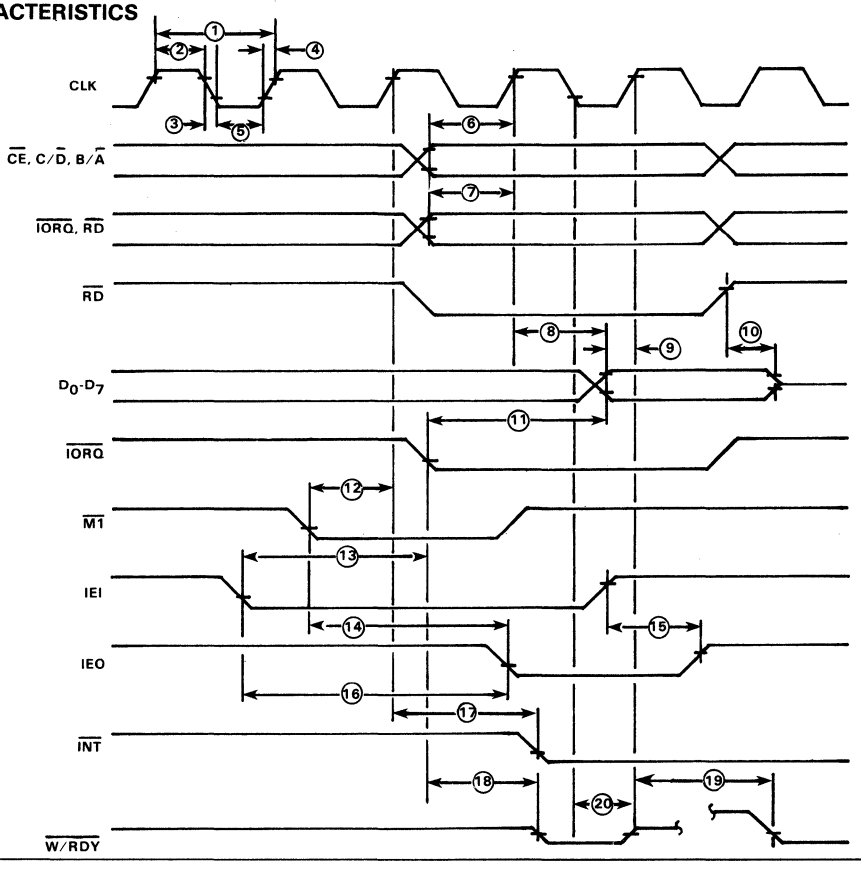
ELECTRICAL CHARACTERISTICS

Figure 10



ELECTRICAL CHARACTERISTICS

Figure 11



VII

PRELIMINARY

MOSTEK®

Z80 MICROCOMPUTER PERIPHERALS

Serial Timer Interrupt Controller

MK3801

FEATURES

- Full duplex USART with programmable DMA control signals
- Two binary delay timers
- Two full feature timers with
  - Delay to interrupt mode
  - Pulse width measurement mode
  - Event counter mode
- Eight general purpose lines with
  - Full bi-directional I/O capability
  - Edge triggered interrupts on either edge
- Full control of each interrupt channel
  - Enable/disable
  - Maskable
  - Automatic end-of-interrupt mode
  - Software end-of-interrupt mode
- 2.5, 4 MHz, and 6 MHz versions available

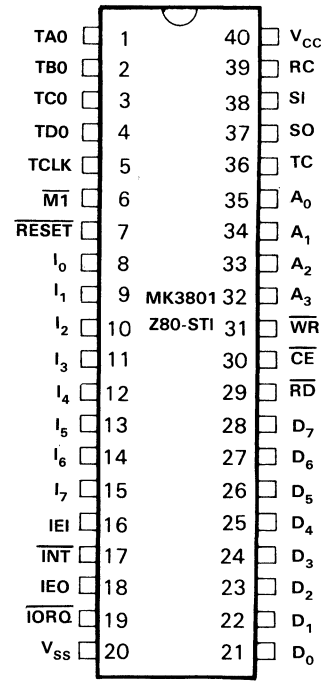
INTRODUCTION

The MK3801 Z80 STI (Serial Timer Interrupt) is a multifunctional peripheral device for use in Z80 microprocessor based systems. It is designed to optimize current systems by reducing chip count and system costs. By providing a USART, four timers (two binary and two full function), and eight bi-directional I/O lines with individually programmable interrupts, the MK3801 can make substantial improvement to any Z80 based system.

Control and operation of the MK3801 are provided by 24 internal registers accessible by the Z80 bus. Sixteen of these registers are directly addressable and accessible; eight are indirectly addressable. Two of the four timers provide full service features, while the other two provide delay timer features only. Serial Communication is provided by the USART, which is capable of either asynchronous or synchronous operation, optional sync word recognition and stripping, and programmable DMA control handshake lines. Eight bi-directional I/O lines provide parallel I/O capability and individually programmable interrupt capability. The interrupt structure of the device is fully programmable for all interrupts, provides for interrupt vector generation, conforms to the Z80 daisy chain interrupt priority scheme, and supports automatic end of interrupt functions for the Z80.

DEVICE PINOUT

Figure 1



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SIGNAL NAME	DESCRIPTION
V_{SS}	Ground
V_{CC}	+5 volts (± 5 percent)
$\overline{CE}$	Chip Enable (Input, active low)
$\overline{RD}$	Read Enable (Input, active low)
$\overline{WR}$	Write Enable (Input, active low)
A_0-A_3	Address Inputs. Used to address one of the internal registers during a read or write operation
D_0-D_7	Data Bus (bi-directional)
$\overline{RESET}$	Device Reset (Input, active low). When activated, all internal registers (except for Timer or USART Data registers) will be cleared, all timers stopped, USART turned off, all interruptsdisabled and all pending interrupts cleared, and all I/O lines placed in tri-state input mode.
I_0-I_7	General purpose I/O and interrupt lines
$\overline{INT}$	Interrupt Request (Output, active low, open drain)
$\overline{IORQ}$	Input/Output Request from Z80-CPU (input, active low). The IORQ signal is used in conjunction with M1 to signal the MK3801 that the CPU is acknowledging its interrupt.
IEI	Interrupt Enable In, active High
IEO	Interrupt Enable Out, active High
SO	Serial Output
SI	Serial Input
RC	Receiver Clock Input
TC	Transmit Clock Input
TAO-TDO	Timer Outputs
TCLK	Timer Clock Input
$\overline{M1}$	Z80 Machine Cycle One (Input, active low)

PIN DESCRIPTION

Figure 1 illustrates the pinout of the MK3801. The functions of these individual pins are described above.

INTERNAL ORGANIZATION

Figure 2 illustrates the MK3801 internal organization, which supports the full set of timing, communications, parallel I/O, and interrupt processing functions available in the device.

CPU BUS I/O

The CPU BUS I/O provides the means of communications between the system and the MK3801. Data, Status, and Control Registers in the MK3801 are accessed by the bus in order to establish device parameters, assert control, and transfer status and data between the system and the MK3801.

Each register in the MK3801 is addressed over the address bus in conjunction with Chip Enable ($\overline{CE}$), while data is transferred over the eight bit Data bus under control of Read ($\overline{RD}$) and Write ($\overline{WR}$) signals.

REGISTER ACCESSES

All register accesses are independent of any system clock. To read a register, both $\overline{CE}$ and $\overline{RD}$ must be active. The internal read control signal is essentially the combination of both $\overline{CE}$ and $\overline{RD}$ active; thus the read operation will begin when the later of these two signals goes active and will end when the first signal goes inactive. The address bus must be stable prior to the start of the operation and must remain stable until the end of the operation. Unless a read operation or an interrupt acknowledge cycle is in progress, the data bus (D_0-D_7) will remain in the tri-state condition.

To write a register, both $\overline{CE}$ and $\overline{WR}$ must be active. The address must be stable prior to the start of the operation and must remain stable until the end of the operation. The data must be stable prior to the end of the operation and must remain stable until the end of the operation. The data presented on the bus will be latched into the register shortly after either $\overline{WR}$ or $\overline{CE}$ goes inactive.

INTERNAL REGISTERS

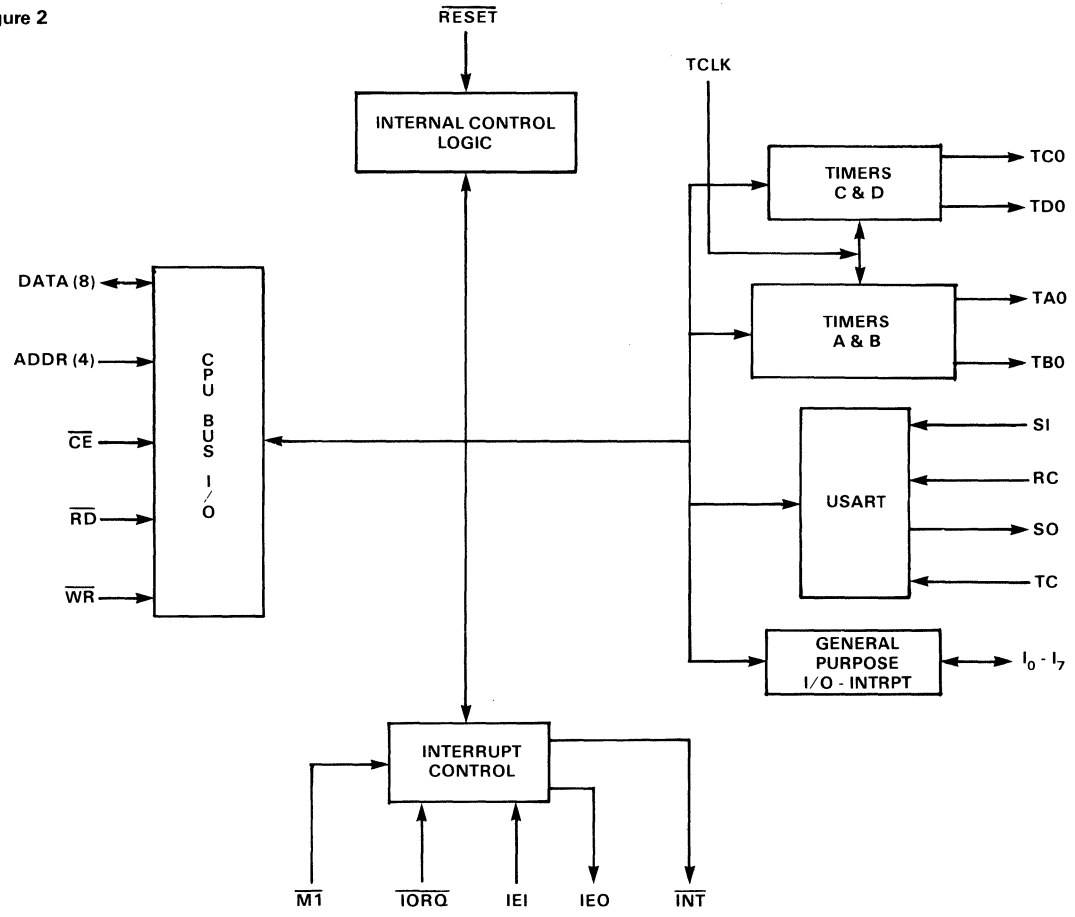
There are 24 internal registers used to control the operation of the STI. Sixteen of these registers are directly addressable and accessible. Eight registers are indirectly addressable via the Pointer/Vector Register and accessible via the Indirect Data Register.

DIRECTLY ADDRESSABLE REGISTERS

The Directly Addressable Registers are accessed by placing the address of the desired register on the address lines (A_0-A_3) during a write or read cycle. Figure 3 lists the Directly Addressable Registers.

INTERNAL ORGANIZATION

Figure 2



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DIRECTLY ACCESSIBLE REGISTERS

Figure 3

ADDRESS	ABBREVIATION	REGISTER NAME
0	IDR	Indirect Data Register
1	GPIP	General Purpose I/O-Interrupt
2	IPRB	Interrupt Pending Register B
3	IPRA	Interrupt Pending Register A
4	ISRB	Interrupt in-Service Register B
5	ISRA	Interrupt in-Service Register A
6	IMRB	Interrupt Mask Register B
7	IMRA	Interrupt Mask Register A
8	PVR	Pointer/Vector Register
9	TABCR	Timers A and B Control Register

DIRECTLY ACCESSIBLE REGISTERS (Continued)
Figure 3

ADDRESS	ABBREVIATION	REGISTER NAME
A	TBDR	Timer B Data Register
B	TADR	Timer A Data Register
C	UCR	USART Control Register
D	RSR	Receiver Status Register
E	TSR	Transmitter Status Register
F	UDR	USART Data Register

INDIRECTLY ADDRESSABLE REGISTERS
Figure 4

INDIRECT ADDRESS	ABBREVIATION	REGISTER NAME
0	SCR	Sync Character Register
1	TDDR	Timer D Data Register
2	TCDR	Timer C Data Register
3	AER	Active Edge Register
4	IERB	Interrupt Enable Register B
5	IERA	Interrupt Enable Register A
6	DDR	Data Direction Register
7	TCDCR	Timers C and D Control Register

INDIRECTLY ADDRESSABLE REGISTERS

Indirectly Addressable Registers are addressed by placing the indirect address in bits IA0-IA2 of the Pointer/Vector Register, as defined in Figure 5. Data may be written to or read from the register indicated by these Indirect Register Address bits by a write or read access of the Indirect Data Register (selected when A_0-A_3 are all zero). The indirect address bits of the Pointer/Vector Register will remain unchanged after an indirect access. Repeated accesses of the Indirect Data Register will access the same indirect register as long as the indirect address in the Pointer/Vector Register remains unchanged. The Indirectly Addressable Registers are listed in Figure 4.

INTERRUPT VECTOR DEFINITION

Each individual function in the MK3801 is provided with a unique interrupt vector that is presented to the system during the interrupt acknowledge cycle. The interrupt vector returned during interrupt acknowledge is formed as shown in Figure 6. There are 16 vector addresses generated internally by the MK3801, one for each of the 16 interrupt channels. The three most significant bits of these vector addresses correspond to the three most significant bits of the Pointer/Vector Register shown in Figure 5. The least significant bit of each vector address is always 0, thus producing even vector addresses. The remaining 4 bits (IV_1 through IV_4) identify each of the 16 interrupt channels individually. The lowest priority channel responds with 0000 for IV_4-IV_1 respectively. The next higher priority channel responds with 0001, and so on in binary order, with the highest priority channel responding with 1111. Figure 7 lists each of the 16 interrupt channels in order of descending priority.

INTERRUPT CONTROL REGISTERS

The Interrupt Control Registers provide control of interrupt processing for all I/O facilities of the MK3801. These registers allow the programmer to enable or disable any or all of the 16 interrupts, provide masking for any interrupts, and access to the pending or in-service status of the interrupts. Optional End-of-Interrupt modes are available under software control. The format of each of the Interrupt Control Registers is presented in Figure 8.

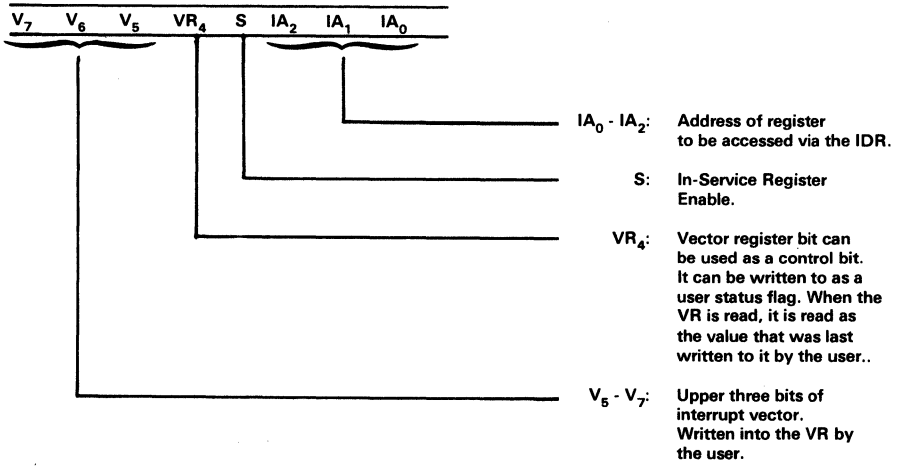
INTERRUPT OPERATION

The Interrupt Enable Registers enable or disable the setting of an interrupt in the Interrupt Pending Registers. A 0 in a bit of the Interrupt Enable Registers disables the interrupt for the associated channel while a 1 enables the interrupt.

Once an interrupt is enabled, the occurrence of an interrupting condition on that channel will cause the

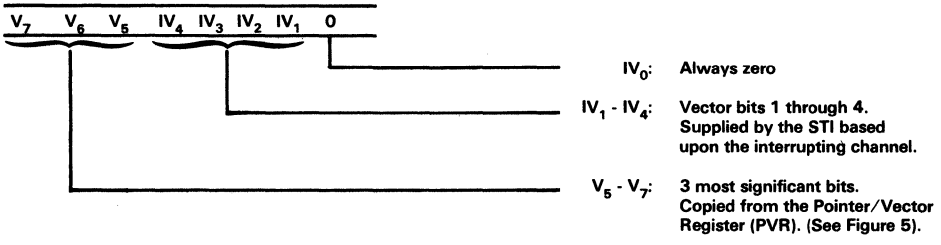
POINTER/VECTOR REGISTER (PVR) Port 08

Figure 5



INTERRUPT VECTOR

Figure 6



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corresponding bit in the Interrupt Pending Register to be set. This indicates that an interrupt is pending in the MK3801.

Pending interrupts are presented to the Z80 CPU in order of priority (see Figure 1) unless they have been masked off. This is done by clearing the bit in the Interrupt Mask Register corresponding to the channel whose interrupt is to be masked. The channel's interrupt will remain pending until the mask bit for that channel is set, at which time the interrupt for that channel will be processsed in order of priority.

When an interrupt vector is generated for a pending interrupt and passed to the Z80 CPU, the bit in the Interrupt Pending Register, associated with the channel generating the interrupt, will be cleared. At this time, no history of the interrupt remains in the MK3801.

In order to retain historical evidence of an interrupt being serviced by the Z80, the In-Service Register may be enabled by setting the S-bit in the Pointer/Vector Register (see Figure 5). If the In-Service Register is enabled, the bit of the In-Service Register corresponding to the interrupting channel will be set when the interrupt vector is passed to the Z80. At the same time, the Interrupt Pending bit will be cleared since the interrupt is now in service. The In-Service bit will be cleared on execution of a Return-from-Interrupt (H'ED4D') instruction. The In-Service Registers are directly addressable, and the In-Service bit for any interrupt may be cleared by writing to the In-Service Register if the Return-from-Interrupt instruction is not used.

INTERRUPT CONTROL REGISTER DEFINITIONS

Figure 7

There are sixteen interrupt channels on the STI arranged in the following priority:

PRIORITY	CHANNEL	DESCRIPTION	ALTERNATE USAGE
HIGHEST	1111	General Purpose Interrupt 7 (I_7)	
	1110	General Purpose Interrupt 6 (I_6)	
	1101	Timer A	
	1100	Receive Buffer Full	
	1011	Receive Error	
	1010	Transmit Buffer Empty	
	1001	Transmit Error	
	1000	Timer B	
	0111	General Purpose Interrupt 5 (I_5)	
	0110	General Purpose Interrupt 4 (I_4)	TA (PW-Event)
	0101	Timer C	
	0100	Timer D	
	0011	General Purpose Interrupt 3 (I_3)	TB (PW-Event)
	0010	General Purpose Interrupt 2 (I_2)	
	0001	General Purpose Interrupt 1 (I_1)	DMA (TR)TX
LOWEST	0000	General Purpose Interrupt 0 (I_0)	DMA (RR)REC

INTERRUPT CONTROL REGISTERS

Figure 8

INTERRUPT ENABLE REGISTERS

ADDRESS		7	6	5	4	3	2	1	0
Indirect Port 5	A (IERA)	GPIP 7	GPIP 6	TIMER A	RCV Buffer Full	RCV Error	XMIT Buffer Empty	XMIT Error	TIMER B
Indirect Port 4	B (IERB)	GPIP 5	GPIP 4	TIMER C	TIMER D	GPIP 3	GPIP 2	GPIP 1	GPIP 0

INTERRUPT MASK REGISTERS

		7	6	5	4	3	2	1	0
Port 7	A (IMRA)	GPIP 7	GPIP 6	TIMER A	RCV Buffer Full	RCV Error	XMIT Buffer Empty	XMIT Error	TIMER B
Port 6	B (IMRB)	GPIP 5	GPIP 4	TIMER C	TIMER D	GPIP 3	GPIP 2	GPIP 1	GPIP 0

1 = UNMASKED, 0 = MASKED

INTERRUPT PENDING REGISTERS

		7	6	5	4	3	2	1	0
Port 3	A (IPRA)	GPIP 7	GPIP 6	TIMER A	RCV Buffer Full	RCV Error	XMIT Buffer Empty	XMIT Error	TIMER B
Port 2	B (IPRB)	GPIP 5	GPIP 4	TIMER C	TIMER D	GPIP 3	GPIP 2	GPIP 1	GPIP 0

WRITING 0 = CLEAR
WRITING 1 = UNCHANGED

INTERRUPT CONTROL REGISTERS (Continued)

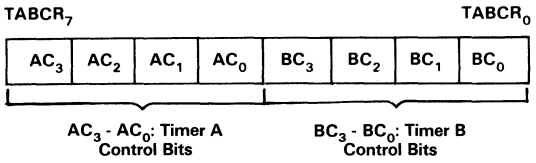
Figure 8

INTERRUPT SERVICE REGISTERS

ADDRESS		7	6	5	4	3	2	1	0
Port 5	A (ISRA)	GPIP 7	GPIP 6	TIMER A	RCV Buffer Full	RCV Error	XMIT Buffer Empty	XMIT Error	TIMER B
Port 4	B (ISRB)	GPIP 5	GPIP 4	TIMER C	TIMER D	GPIP 3	GPIP 2	GPIP 1	GPIP 0

TIMER A and B CONTROL REGISTER (TABCR) Port 9

Figure 9

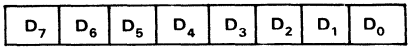


The four control bits are used to select the timer mode and prescale value, as follows:

CONTROL BIT DEFINITION

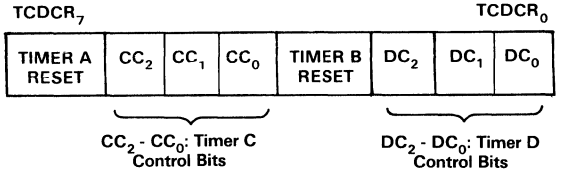
C_3	C_2	C_1	C_0	
0	0	0	0	Timer Stopped
0	0	0	1	Delay Mode, ÷4 Prescale
0	0	1	0	Delay Mode, ÷10 Prescale
0	0	1	1	Delay Mode, ÷16 Prescale
0	1	0	0	Delay Mode, ÷50 Prescale
0	1	0	1	Delay Mode, ÷64 Prescale
0	1	1	0	Delay Mode, ÷100 Prescale
0	1	1	1	Delay Mode, ÷200 Prescale
1	0	0	0	Event Count Mode
1	0	0	1	Pulse Width Mode, ÷4 Prescale
1	0	1	0	Pulse Width Mode, ÷10 Prescale
1	0	1	1	Pulse Width Mode, ÷16 Prescale
1	1	0	0	Pulse Width Mode, ÷50 Prescale
1	1	0	1	Pulse Width Mode, ÷64 Prescale
1	1	1	0	Pulse Width Mode, ÷100 Prescale
1	1	1	1	Pulse Width Mode, ÷200 Prescale

TIMER A DATA REGISTER AND TIMER B DATA REGISTER (TADR, TBDR) Port B & Port A



TIMER C and D CONTROL REGISTER (TCDCR) Indirect Port 7

Figure 10

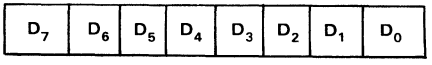


Three control bits are used to control each timer, as defined below:

CONTROL BIT DEFINITION

C_2	C_1	C_0	
0	0	0	Timer Stopped
0	0	1	Delay Mode, ÷4 Prescale
0	1	0	Delay Mode, ÷10 Prescale
0	1	1	Delay Mode, ÷16 Prescale
1	0	0	Delay Mode, ÷50 Prescale
1	0	1	Delay Mode, ÷64 Prescale
1	1	0	Delay Mode, ÷100 Prescale
1	1	1	Delay Mode, ÷200 Prescale

TIMER C DATA REGISTER and TIMER D DATA REGISTER (TCDR, TDDR) Indirect, Port 2 and Indirect Port 1



TIMERS

Four timers are available on the MK3801. Two provide full service features including delay timer operation, event counter operation, pulse width measurement operation, and pulse generation. The two other timers provide delay timer features only, and may be used for baud rate generators for use with the USART.

All timers are prescaler/counter timers, with a common independent clock input, and are not required to be operated from the system clock. In addition, all timers have a time-out output function that toggles each time the timer times out.

TIMER CONTROL REGISTERS

The 4 timers (A,B,C, and D) are programmed via 2 control registers and 4 timer data registers. Timers A and B are controlled by a single register (TABCR) and two timer data registers (TADR,TBDR). Timers C and D are controlled by a second control register (TCDCR) and two timer data

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registers (TCDR, TDDR). Bits in the control registers allow the selection of operational mode, prescale, and control, while the data registers are used to read the timer or write the time constant register. General Purpose I/O Interrupt pins 3 (TB) and 4 (TA) are used for timer B and A inputs in event and pulse width modes. Figure 9 illustrates the Control and Data Register for timers A and B, while Figure 10 illustrates the Control and Data registers for timers C and D.

USART

Serial Communication is provided by the USART, which is capable of either asynchronous or synchronous operation. Variable word width and start/stop bit configurations are available under software control for asynchronous operation. For synchronous operation, a Sync Word is provided to establish synchronization during receive operations. The Sync Word will also be repeatedly transmitted when no other data is available for transmission. Operational modes exist to allow stripping of all Sync Words received in synchronous operation, and to allow the operation of DMA control handshake lines by the USART through General Purpose I/O Port lines 0 and 1. Separate receive and transmit clocks are available, and separate receive and transmit status and data bytes allow independent operation of the transmit and receive sections.

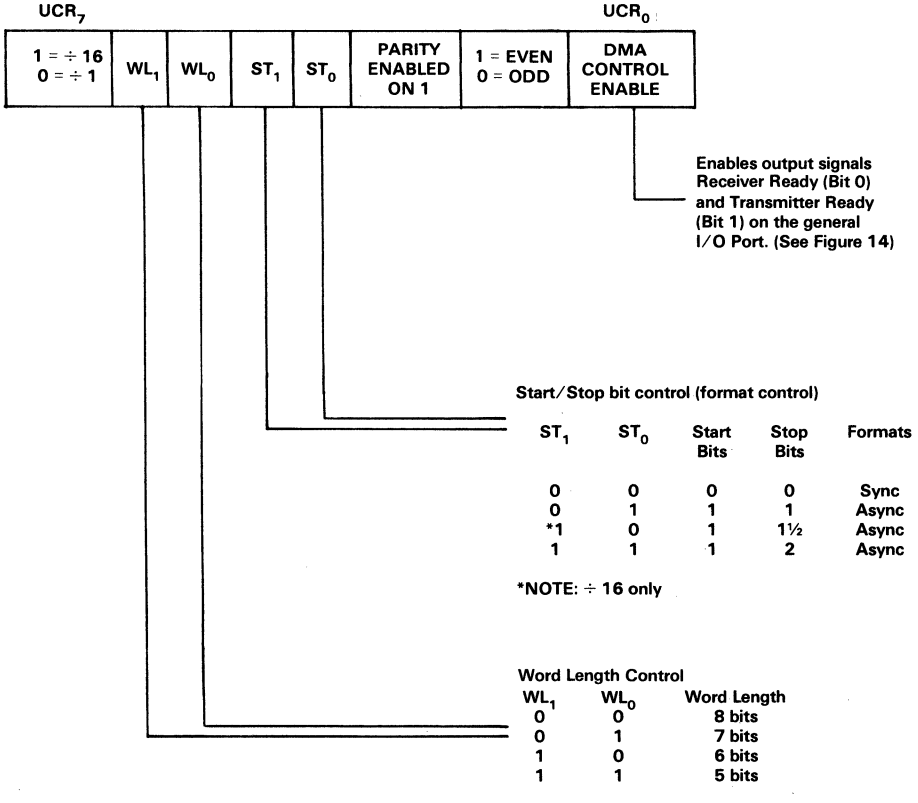
USART CONTROL REGISTERS

The USART is provided with 3 control/status registers and a data register. The programmer may specify operational parameters for the USART via the Control Register, as shown in Figure 11. Status of both the Receiver and Transmitter sections is accessed by means of the 2 Status Registers, as shown in Figure 12. Data written to the Data Register is passed to the transmitter, while reading the data register will access data received by the USART. The USART Data Register form is illustrated in Figure 13.

ERROR CONDITIONS

Error conditions in the USART are determined by monitoring the Receive Status Register (Port D) and the Transmitter Status Register (Port E). These error conditions are only valid for each word boundary and are not latched. When executing block transfers of data, it is necessary to save any errors so that they can be checked at the end of a block. In order to save error conditions during data transfer, the STI interrupt controller may be used by enabling error

USART CONTROL REGISTER (UCR) Port C
Figure 11



RECEIVER STATUS REGISTER (RSR) Port D

Figure 12

RSR_7							RSR_0
BUFFER FULL	OVERRUN ERROR	PARITY ERROR	FRAME ERROR	FOUND/$\overline{\text{SEARCH}}$ OR BREAK DETECT	MATCH/CHARACTER IN PROGRESS	SYNC STRIP ENABLE	RECEIVER ENABLE

TRANSMITTER STATUS REGISTER (TSR) Port E

TSR_7							TSR_0
BUFFER EMPTY	UNDERRUN ERROR	AUTO TURNAROUND	END OF TRANSMISSION	BREAK	HIGH	LOW	TRANSMITTER ENABLE

H	L	Serial Output State
0	0	Hi-Z
0	1	Low ("0")
1	0	High
1	1	Loop*

*Connects transmitter output to receiver input. In loopback mode, transmitter goes high when disabled. Also connects clocks with TC given priority.

USART DATA REGISTER (UDR) Port F

Figure 13

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

GENERAL PURPOSE I/O CONTROL REGISTERS

Figure 14

ACTIVE EDGE CONTROL REGISTER (AER) Indirect Port 3

1 = RISING
0 = FALLING

GPIP 7	GPIP 6	GPIP 5	GPIP 4	GPIP 3	GPIP 2	GPIP 1	GPIP 0

DATA DIRECTION REGISTER (DDR) Indirect Port 6

1 = OUTPUT
0 = INPUT

GPIP 7	GPIP 6	GPIP 5	GPIP 4	GPIP 3	GPIP 2	GPIP 1	GPIP 0

GENERAL PURPOSE I/O DATA REGISTER (GPIP) Port 1

GPIP 7	GPIP 6	GPIP 5	GPIP 4	GPIP 3	GPIP 2	GPIP 1 (TR)	GPIP 0 (RR)
			TIMER A INPUT	TIMER B INPUT			

interrupts (Port 5, Indirect) for the desired channel (Receive error or Transmit error) and by masking these bits off (Port 7). Once the transfer is complete, the Interrupt Pending Register (Port 3) can be polled to determine the presence of a pending error interrupt, and therefore an error.

GENERAL PURPOSE I/O - INTERRUPT PORT

The General Purpose I/O - Interrupt Port provides eight I/O lines that may be operated either as inputs or outputs under software control. In addition, each line may generate an interrupt on either a positive going edge or a negative going edge of the input signal.

Two of the lines in this port provide auxiliary input functions for the timers in the pulse width measurement mode and the event counter mode. Two others serve as auxiliary output lines for the USART, one indicating the Receive Buffer Full condition (RR) and the other indicating the Transmitter Buffer Empty condition (TR). These may be used as handshake signals for a DMA controller or other external control circuitry.

GENERAL PURPOSE I/O CONTROL REGISTERS

The General Purpose I/O and Interrupt Port has 2 control registers. One allows the programmer to specify the Active Edge for each bit that will trigger the interrupt associated with that bit. The other register specifies the Data Direction (input and output) associated with each bit. The third register is the actual data I/O register used to input or output data to the port. When the USART is programmed to use DMA signals, this overrides the GPIP data and the DDR. The General Purpose I/O Control and Data Registers are illustrated in Figure 14.

MK3801 ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias ..... -25°C to + 100°C
Storage Temperature ..... -65°C to + 150°C
Voltage on Any Pin with Respect to Ground ..... -.3 V to + 7 V
Power Dissipation ..... 1.5 W

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = +5 V ± 5% unless otherwise specified.

SYM	PARAMETER	MIN	MAX	UNIT	TEST CONDITION
V_{IH}	Input High Voltage	2.0	V_{CC} + .3	V	
V_{IL}	Input Low Voltage	-0.3	0.8	V	
V_{OH}	Output High Voltage	2.4		V	I_{OH} = -120 μA
V_{OL}	Output Low voltage		0.4	V	I_{OL} = 2.0 mA
I_{LL}	Power Supply Current		180	mA	Outputs Open
I_{LI}	Input Leakage Current		±10	μA	V_{IN} = 0 to V_{CC}
I_{LOH}	Tri-State Output Leakage Current in Float		10	μA	V_{OUT}=2.4 to V_{CC}
I_{LOL}	Tri-State Output Leakage Current in Float		-10	μA	V_{OUT} = 0.4 V

All voltages are referenced to ground.

CAPACITANCE

T_A = 25°C, f = 1 MHz unmeasured pins returned to ground.

SYM	PARAMETER	MAX	UNIT	TEST CONDITION
C_{IN}	Input Capacitance	10	pf	Unmeasured pins returned to ground
C_{OUT}	Tri-state Output Capacitance	10	pf	

A.C. CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = +5 V ± 5% unless otherwise noted.

SIGNAL	SYMBOL	PARAMETER	MK3801-0		MK3801-4		MK3801-6		UNIT	CONDITION
			MIN	MAX	MIN	MAX	MIN	MAX		
A_0-A_3	T_{SAR} & T_{SAW}	Address setup time prior to falling edge of $\overline{CEWR}$ or $\overline{CERD}$	80		30		15		ns	
	T_{HAR} & T_{HAW}	Address hold time after rising edge of $\overline{CEWR}$ or $\overline{CERD}$	0		0		0		ns	
$\overline{CEWR}$	T_{WL}	$\overline{CEWR}$ pulse width low (write cycle)	360		205		175		ns	Note 1
	T_{WW}	$\overline{CEWR}$ high time between write cycles	580		400		300		ns	Note 1
	T_{WRD}	$\overline{CEWR}$ high to $\overline{CERD}$ low	580		400		300		ns	
$\overline{CERD}$	T_{RDL}	$\overline{CERD}$ pulse width low (read cycle)	400		250		215		ns	Note 1
	T_{RR}	$\overline{CERD}$ high time between read cycles	300		200		190		ns	
	T_{M1RD}	Rising $\overline{M1RD}$ to falling $\overline{M1RD}$	225		165		95		ns	
	T_{RDW}	$\overline{CERD}$ high to $\overline{CEWR}$ low	125		100		75			
$\overline{M1}$	T_{SM1}	$\overline{M1}$ setup time prior to falling $\overline{IORQ}$ during interrupt acknowledge	800		500		350		ns	
$\overline{IORQ}$	T_{IOL}	$\overline{IORQ}$ low time	300		185		170		ns	
IEI	T_{SIEI}	Setup to falling $\overline{IORQ}$ during interrupt acknowledge	140		80		65		ns	
	T_{SRD}	Setup prior to end of 4D read on RETI	100		50		40		ns	
D_0-D_7	T_{SDM1}	Data valid prior to rising $\overline{RD}$ ($\overline{M1}$ cycle)	65		50		45		ns	Load 100 pf + 1 TTL load
	T_{HDM1}	Data hold time after rising $\overline{RD}$ ($\overline{M1}$ cycle)	0		0		0		ns	
	T_{DRD}	Data output delay from $\overline{CERD}$		400		250		215	ns	
	T_{SDW}	Data setup time to rising edge of $\overline{CEWR}$	350		280		175		ns	
	T_{HDW}	Data hold time from rising edge of $\overline{CEWR}$	0		0		0		ns	
	T_{DDI}	Data output delay from falling $\overline{IORQ}$ during interrupt acknowledge		300		185		170	ns	

NOTE 1: One wait state must be inserted when used as a 6 MHz memory mapped device.

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A.C. CHARACTERISTICS (Continued)

SIGNAL	SYMBOL	PARAMETER	MK3801-0		MK3801-4		MK3801-6		UNIT	CONDITION
			MIN	MAX	MIN	MAX	MIN	MAX		
	T_{DHVZ}	Data hold time following $\overline{M1}$ $\overline{IORQ}$ during interrupt acknowledge cycle.	0		0		0		ns	
	T_{DDZ}	Delay to float		150		100		80	ns	
I_0-I_7	T_{IPW}	Minimum active pulse width	200		100		90		ns	
	T_{ICY}	Minimum time between active edges	200		100		90		ns	
	T_{DIW}	Data valid from rising $\overline{CEWR}$		600		500		400	ns	Load 100 pf + 1 TTL
RR	T_{DRR}	Delay from rising RC		360		240		195	ns	1 TTL
TR	T_{DTR}	Delay from rising TC		450		295		240	ns	
TA0-TD0	T_{DTW}	Timer output low from rising edge of $\overline{CEWR}$ (A & B) (Reset T_{OUT})		600		500		400	ns	Load 100 pf +
	T_{DTI}	T_{OUT} valid from Internal timeout		2 t_{CLK} +400		2 t_{CLK} +300		2 t_{CLK} +250	ns	1 TTL load
TCLK	$T_{t_{CLKL}}$	Low time	130		95		75		ns	
	$T_{t_{CLKH}}$	High time	130		95		75		ns	
	$T_{t_{CKC}}$	Cycle time	300	2500	200	2500	165	2500	ns	
$\overline{RESET}$	T_{RSL}	Low time for part reset	3		2		1.6		μs	
IEO	T_{DIEOH}	IEO delay from rising edge of IEI		200		130		100	ns	Load 100 pf +
	T_{DIEOL}	IEO delay from falling edge of IEI		200		130		100	ns	1 TTL load
	T_{DIEOM}	IEO delay from falling edge of $\overline{M1}$ (interrupt occurring just prior to $\overline{M1}$)		270		190		110	ns	
	T_{DIEOA}	Delay to rising IEO from rising $\overline{IORQ}$ during interrupt acknowledge		1000		800		600	ns	
	T_{DIEOR}	Delay to rising IEO from rising edge of RD during ED fetch of RETI		500		400		300	ns	
$\overline{INT}$	T_{DIX}	Delay to falling $\overline{INT}$ from external interrupt active transition		550		380		300	ns	Open drain load 100 pf + 2.1 K resistor

A.C. CHARACTERISTICS (Continued)

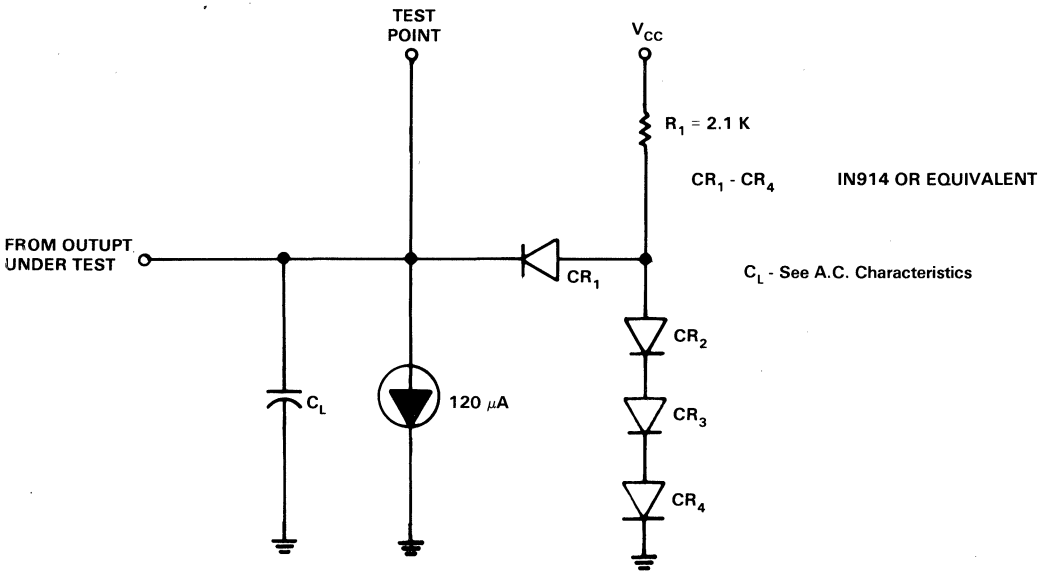
SIGNAL	SYMBOL	PARAMETER	MK3801-0		MK3801-4		MK3801-6		UNIT	CONDITION
			MIN	MAX	MIN	MAX	MIN	MAX		
	T_{DII}	Delay to falling $\overline{INT}$ from internal interrupt transition		360		280		250	ns	
	T_{DTI}	Transmitter Internal interrupt transition delay from rising or falling edge of TC		560		390		360	ns	
	T_{DRI}	Receiver buffer full internal interrupt transition delay from rising edge of RC		400		300		270	ns	
	T_{DREI}	Receiver error internal interrupt transition delay from falling edge of RC		550		430		400	ns	
SI	T_{SSI}	Serial in set up time to rising edge of RC (Divide by one only)	80		80		55		ns	
	T_{HSI}	Data hold time from rising edge of RC (Divide by one only)	400		350		300		ns	
SO	T_{DSO}	Data valid from falling edge of TC		420		390		345	ns	100 pf + 1 TTL load
TC	T_{TCL}	Low time	650		500		400		ns	
	T_{TCH}	High time	650		500		400		ns	
	T_{TCCY}	Cycle time	1.5		1.05		.85		μs	
RC	T_{RCL}	Low time	650		500		400		ns	
	T_{RCH}	High time	650		500		400		ns	
	T_{RCCY}	Cycle time	1.5		1.05		.85		μs	

NOTE: All A.C. measurements are referenced to V_{IL} max., V_{IH} min., V_{OL} (0.8 V), or V_{OH} (2.0 V).

VII

OUTPUT LOAD CIRCUIT

Figure 15



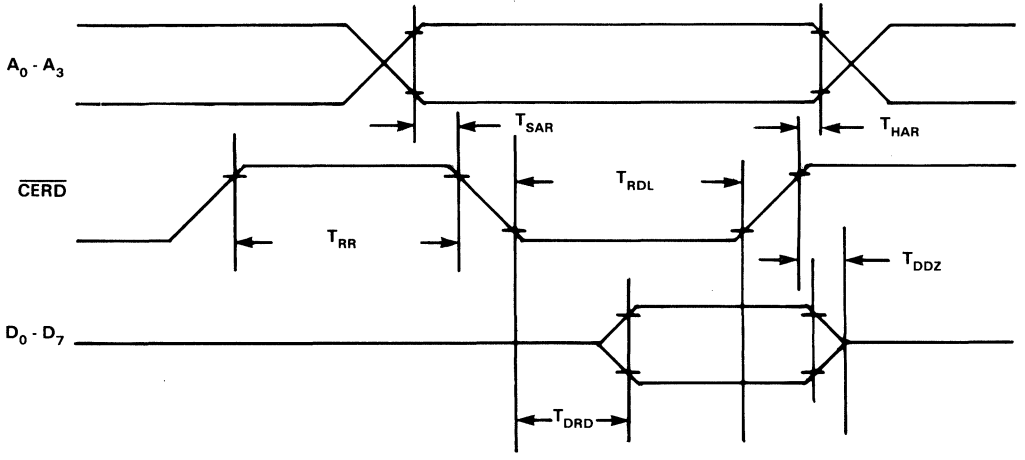
TIMING DIAGRAMS

Figure 16

Timing measurements are made at the following voltages, unless otherwise specified:

	"1"	"0"
OUTPUT	2.0 V	0.8 V
INPUT	2.0 V	0.8 V
FLOAT	△ V =	0.5 V

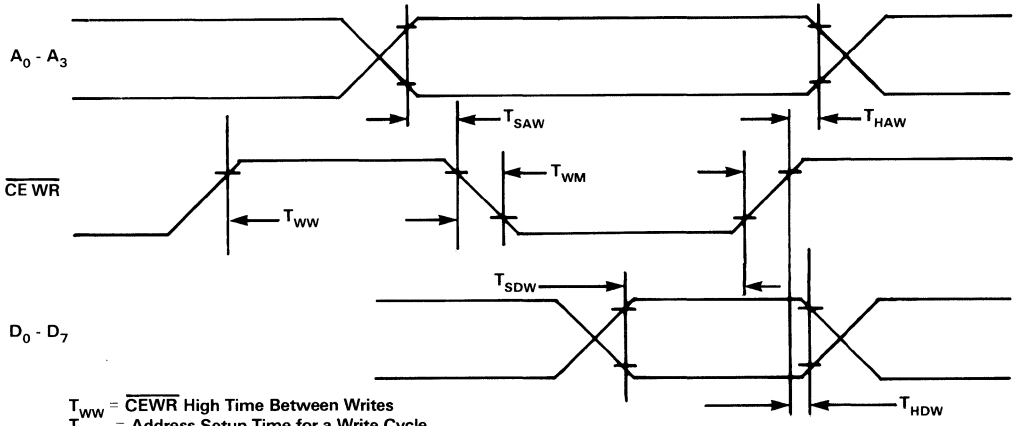
READ CYCLE



T_{SAR} = Address Setup Time for a Read Cycle
T_{DRD} = Data Output Delay from $\overline{CERD}$
T_{DDZ} = Time to Tri-State Following a Read Cycle
T_{HAR} = Required Address Hold Time Following a Read Cycle

WRITE CYCLE

Figure 17

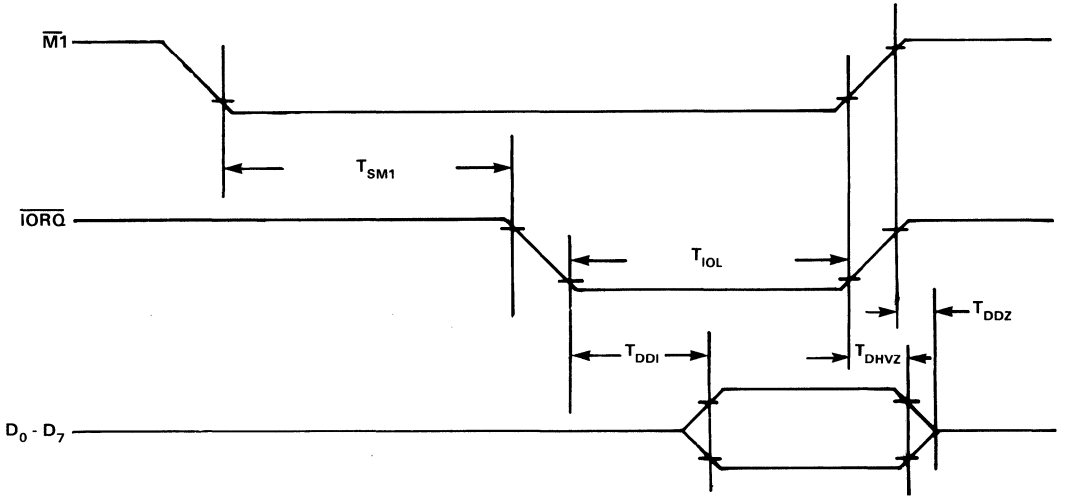


T_{WW} = $\overline{CEWR}$ High Time Between Writes
T_{SAW} = Address Setup Time for a Write Cycle
T_{SDW} = Data Setup Time Prior to the End of a Write Cycle
T_{HDW} = Required Data Hold Time Following a Write Cycle
T_{HAW} = Required Address Hold Time Following a Write Cycle
T_{WM} = $\overline{CEWR}$ pulse width low

VII

INTERRUPT ACKNOWLEDGE CYCLE

Figure 18



T_{IOL} = $\overline{IORQ}$ Pulse Width Low
T_{SMI} = $\overline{M1}$ Setup Time prior to $\overline{IORQ}$ For an Acknowledge cycle
T_{DDI} = Access Time for Vector
T_{DDZ} = Time to Tri-State Following a Vector
T_{DHVZ} = Data hold time following $\overline{M1}$ $\overline{IORQ}$ during interrupt acknowledge cycle

TIMER A.C. CHARACTERISTICS

Definitions:

Error = Indicated Time Value - Actual Time Value

tpsc = t_{CLK} x Prescale Value

Internal Timer Mode

Single Interval Error (free running) (Note 2) ..... ± 100 ns
Cumulative Internal Error 0
Error Between Two Timer Reads ..... ± (tpsc + 4 t_{CLK})
Start Timer to Stop Timer Error ..... 2 t_{CLK} + 100 ns to –(tpsc + 6t_{CLK} + 100 ns)
Start Timer to Read Timer Error ..... 0 to –(tpsc + 6 t_{CLK} + 400 ns)
Start Timer to Interrupt Request Error (Note 3) ..... –2 t_{CLK} to –(4t_{CLK} +800 ns)

Pulse Width Measurement Mode

Measurement Accuracy (Note 1) ..... 2 t_{CLK} to –(tpsc + 4t_{CLK})
Minimum Pulse Width ..... 4t_{CLK}

Event Counter Mode

Minimum Active Time of I_3, I_4 ..... 4t_{CLK}
Minimum Inactive Time of I_3, I_4 ..... 4t_{CLK}

NOTES:
1. Error may be cumulative if repetitively performed.
2. Error with respect to T_{OUT} or INT if note 3 is true.
3. Assuming it is possible for the timer to make an interrupt request immediately.

ORDERING INFORMATION

PART NO.	DESIGNATOR	PACKAGE TYPE	MAX CLOCK FREQUENCY	TEMPERATURE RANGE
MK3801N-0	Z80-STI	Plastic	2.5 MHz	0 to 70°C
MK3801N-4	Z80-STI	Plastic	4.0 MHz	0 to 70°C
MK3801N-6	Z80-STI	Plastic	6.0 MHz	0 to 70°C

1982/1983 MICROELECTRONIC DATA BOOK

3870 FAMILY
SELECTION GUIDE

	MEMORY			I/O		PKG.	ADDRESS RANGE		MISC.	
ROM DEVICES	ROM x 8	SCRATCHPAD RAM x 8	EXECUTABLE RAM x 8	PARALLEL I/O LINES	SERIAL I/O	PACKAGE SIZE	ADDRESS REGISTERS SIZE	USABLE ADDRESS RANGE (Note 1)	STANDBY RAM OPTION	OTHER
2870/10	1K	64	0	20	No	28	12 bits	1K	No	
3870/10	1K	64	0	32	No	40	12 Bits	1K	No	
3870/20	2K	64	0	32	No	40	11 Bits 12 Bits	2K	No	(Note 2)
38C70/20	2K	64	0	32	No	40	16 Bits	2K	Halt Mode	CMOS
3870/30	3K	64	0	32	No	40	12 Bits	3K	No	
3870/40	4K	64	0	32	No	40	12 Bits	4K	No	
3870/42	4032	64	64	32	No	40	12 Bits	4K	No	
3873/22	2K	64	64	29	Yes	40	12 Bits	2K + 64	No	Baud rate generator
3875/42	4032	64	64	30	No	40	12 Bits	4K	Yes	
P-PROM DEVICES										Address external Memory (EPROM) through socket on top of 40 pin package
97300	0	64	64	29	Yes	40	12 Bits	4K	No	(38P73)
97310	0	64	64	29	Yes	40	12 Bits	4K	No	(38P73)
97400	0	64	64	32	No	40	12 Bits	4K	No	(38P70)
97403	0	64	64	30	No	40	12 Bits	4K	Yes	(38P75)
97410	0	64	64	32	No	40	12 Bits	4K	No	(38P70)
97500	0	64	64	32	No	40	16 Bits	8K +64	No	(38P70)
97501	0	64	64	32	No	40	16 Bits	8K +64	No	(38P70)
97502	0	64	64	32	No	40	16 Bits	64K	No	(38P70)

NOTES:

1. Usable address range is the amount of memory that can effectively be addressed. This may be less than the full range of the address registers either because the amount of on-chip memory is less than the possible address range or, in the case of P-PROM devices, all address bits are not externally available.
2. The original 3870 device (3870/20) has 11 bit address registers. A version is now available with 12 bit address registers.

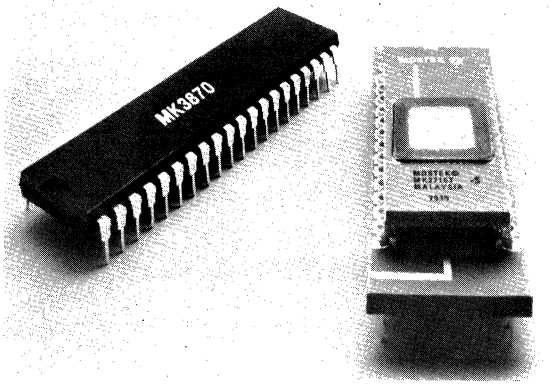
MK3870 and MK38P70

MK3870 FEATURES

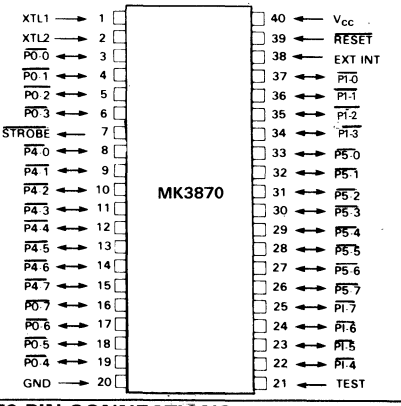
- ☐ Available with 1K, 2K, 3K, or 4K bytes of mask programmable ROM memory
- ☐ 64 bytes scratchpad RAM
- ☐ Available with 64 bytes executable RAM
- ☐ 32 bits (4 ports) TTL compatible I/O
- ☐ Programmable binary timer
  Interval timer mode
  Pulse width measurement mode
  Event counter mode
- ☐ External interrupt input
- ☐ Crystal, LC, RC, or external time base options
- ☐ Low power (275 mW typ.)
- ☐ Single +5 volt supply

MK38P70 FEATURES

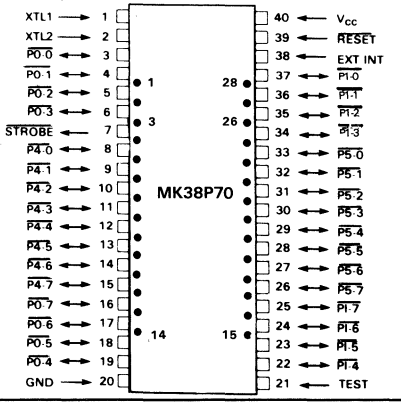
- ☐ EPROM version of MK3870
- ☐ Piggyback PROM (P-PROM)™ package
- ☐ Accepts 24 pin or 28 pin EPROM memories
- ☐ Identical pinout as MK3870
- ☐ In-Socket emulation of MK3870



MK3870 PIN CONNECTIONS



MK38P70 PIN CONNECTIONS



GENERAL DESCRIPTION

The MK3870 is a complete 8-bit microcomputer on a single MOS integrated circuit. The MK3870 can execute a set of more than 70 instructions, and is completely software compatible with the rest of the devices in the 3870 family. The MK3870 features 1-4K bytes of ROM and optional additional executable RAM depending on the specific part type designated by a slash number suffix. The MK3870 also features 64 bytes of scratchpad RAM, a programmable binary timer, and 32 bits of I/O.

The programmable binary timer operates by itself in the interval timer mode or in conjunction with the external interrupt input in the pulse width measurement and the

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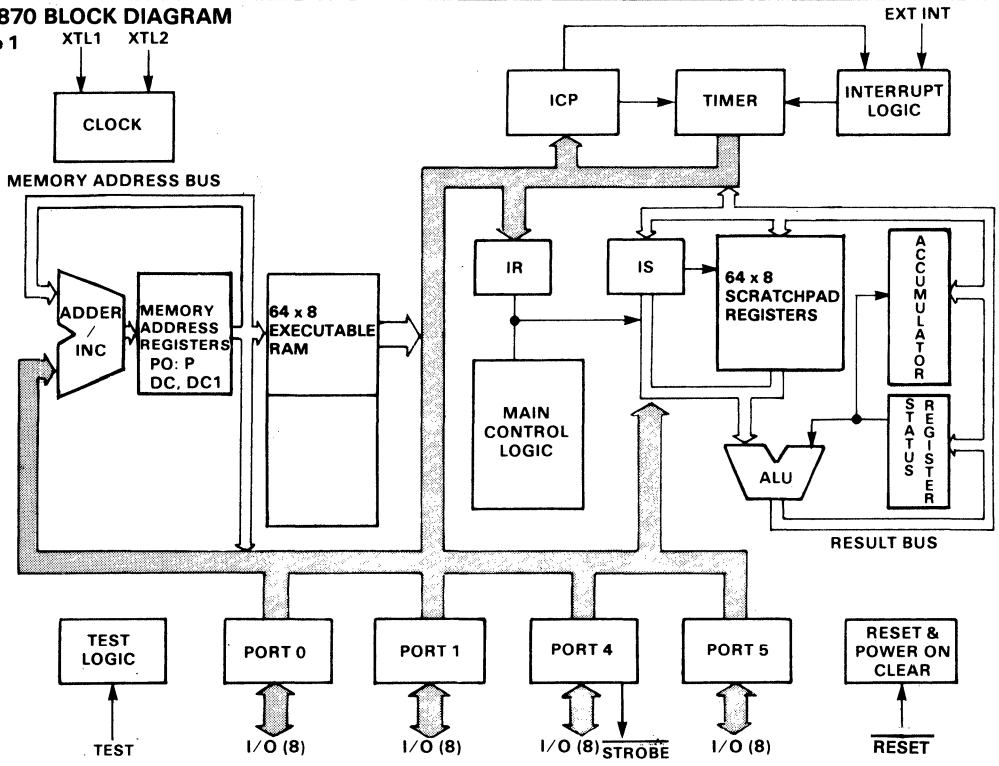
MK3870 BLOCK DIAGRAM

Figure 1



event counter modes of operation. Two sources of vectored, prioritized interrupt are provided with the binary timer and the external interrupt input. The user has the option of specifying one of four clock sources for the MK3870 and MK38P70: Crystal, LC, RC, or external clock. In addition, the user can specify either a ±10% power supply tolerance or a ±5% power supply tolerance.

The MK38P70 microcomputer is the PROM based version of the MK3870. It is called the piggyback PROM (P-PROM)™ because of its packaging concept. This concept allows a standard 24-pin or 28 pin EPROM to be mounted directly on top of the microcomputer itself. The EPROM can be removed and reprogrammed as required with a standard PROM programmer. The MK38P70 retains exactly the same pinout and architectural features as other members of the 3870 family. The MK38P70 is discussed in more detail in a later section.

PIN NAME	DESCRIPTION	TYPE
$\overline{P0\text{-}0}$ -- $\overline{P0\text{-}7}$	I/O Port 0	Bidirectional
$\overline{P1\text{-}0}$ -- $\overline{P1\text{-}7}$	I/O Port 1	Bidirectional
$\overline{P4\text{-}0}$ -- $\overline{P4\text{-}7}$	I/O Port 4	Bidirectional
$\overline{P5\text{-}0}$ -- $\overline{P5\text{-}7}$	I/O Port 5	Bidirectional
$\overline{STROBE}$	Ready Strobe	Output
EXT INT	External Interrupt	Input
$\overline{RESET}$	External Reset	Input
TEST	Test Line	Input
XTL 1, XTL 2	Time Base	Input
V_{CC}, GND	Power Supply Lines	Input

FUNCTIONAL PIN DESCRIPTION

$\overline{P0\text{-}0}$-- $\overline{P0\text{-}7}$, $\overline{P1\text{-}0}$--$\overline{P1\text{-}7}$, $\overline{P4\text{-}0}$--$\overline{P4\text{-}7}$, and $\overline{P5\text{-}0}$--$\overline{P5\text{-}7}$ are 32 lines which can be individually used as either TTL compatible inputs or as latched outputs.

$\overline{STROBE}$ is a ready strobe associated with I/O Port 4. This pin, which is normally high, provides a single low pulse after valid data is present on the $\overline{P4\text{-}0}$--$\overline{P4\text{-}7}$ pins during an output instruction.

$\overline{RESET}$ may be used to externally reset the MK3870. When pulled low the MK3870 will reset. When then allowed to go high the MK3870 will begin program execution at program location H '000'.

EXT INT is the external interrupt input. Its active state is software programmable. This input is also used in conjunction with the timer for pulse width measurement and event counting.

XTL 1 and XTL 2 are the time base inputs to which a crystal, LC network, RC network, or an external single-phase clock may be connected. The time base network must be specified when ordering a mask ROM MK3870. The MK38P70 will operate with any of the four configurations.

TEST is an input, used only in testing the MK3870. For normal circuit function this pin may be left unconnected, but

it is recommended that TEST be grounded.

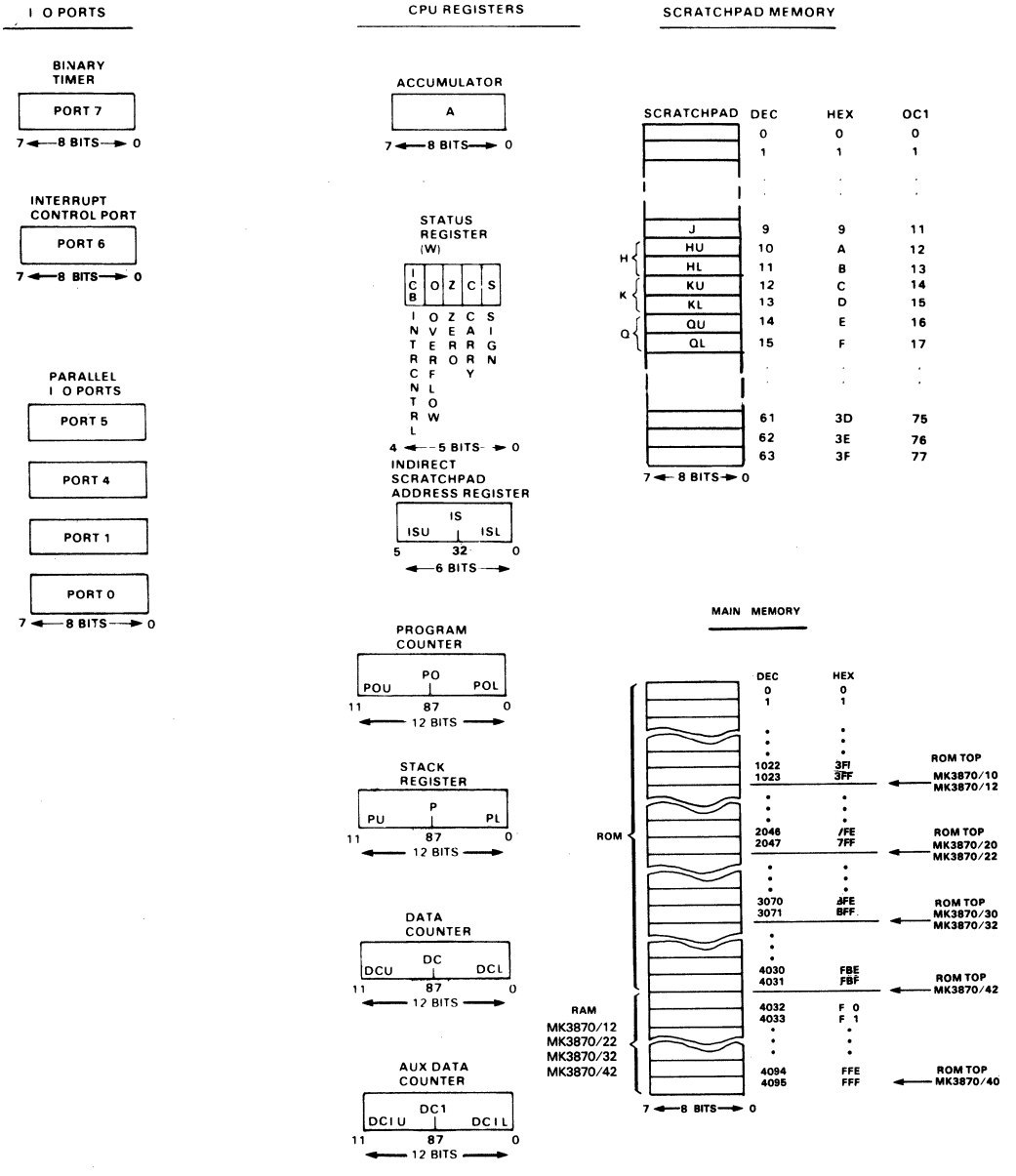
V_{CC} is the power supply input (single +5v).

MK3870 ARCHITECTURE

The basic functional elements of the MK3870 are shown in Figure 1. A programming model is shown in Figure 2. The architecture is common to all members of the 3870 family. All 3870 devices are instruction set compatible and differ only in amount and type of ROM, RAM, and I/O. The unique features of the MK3870 are discussed in the following sections. The user is referred to the 3870 Family Technical Manual for a thorough discussion of the architecture, instruction set, and other features which are common to all 3870 family devices.

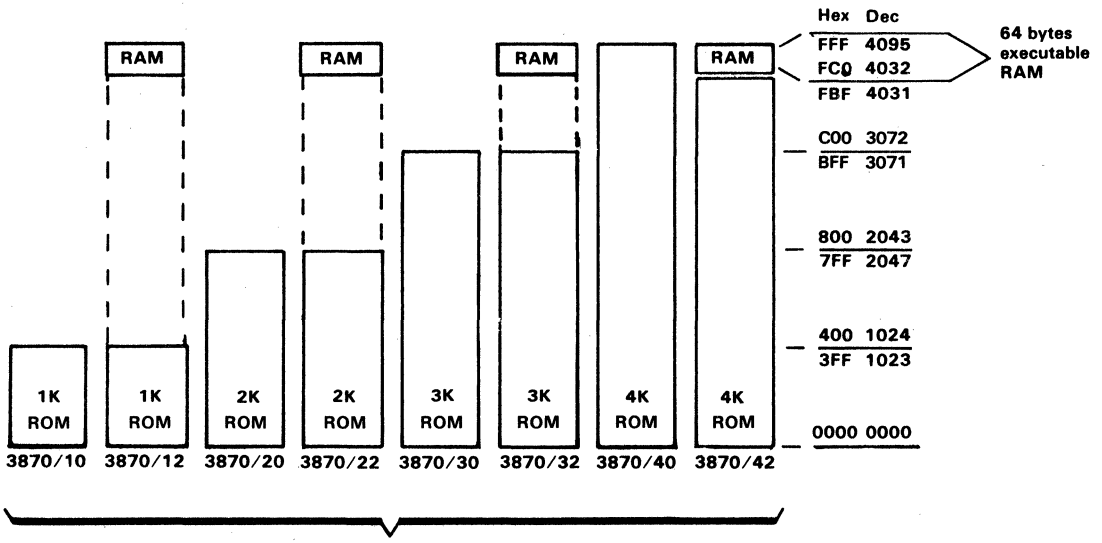
MK3870 PROGRAMMABLE REGISTERS, PORTS, AND MEMORY MAP

Figure 2



VIII

MK3870 MAIN MEMORY
SIZES AND TYPES BY SLASH NUMBERS
Figure 3



All devices contain 64 bytes of scratchpad RAM.

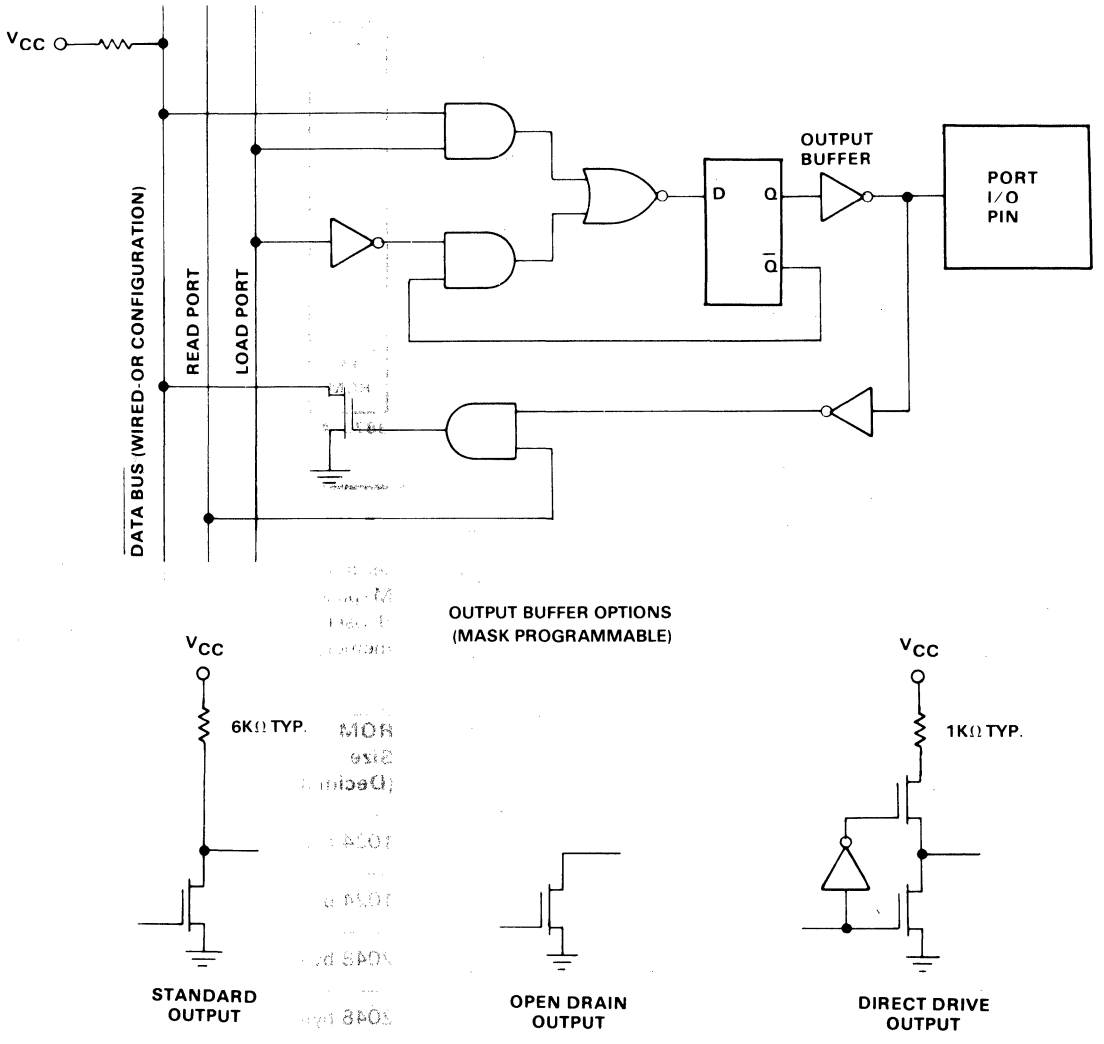
NOTE: Data derived from addressing any locations other than those within a part's specified ROM space or RAM space (if any) are not tested nor are the data guaranteed. Users should refrain from entering this area of the memory map.

Device	Scratchpad RAM Size (Decimal)	Address Register Size (P0, P, DC, DC1)	ROM Size (Decimal)	Executable RAM Size
MK3870/10	64 bytes	12 bits	1024 bytes	0 bytes
MK3870/12	64 bytes	12 bits	1024 bytes	64 bytes
MK3870/20*	64 bytes	12 bits	2048 bytes	0 bytes
MK3870/22	64 bytes	12 bits	2048 bytes	64 bytes
MK3870/30	64 bytes	12 bits	3072 bytes	0 bytes
MK3870/32	64 bytes	12 bits	3072 bytes	64 bytes
MK3870/40	64 bytes	12 bits	4096 bytes	0 bytes
MK3870/42	64 bytes	12 bits	4032 bytes	64 bytes

*The MK3870/20 is equivalent to the original 3870 device in memory size; however, the original 3870 had an 11-bit Address Register. The original 3870 with 11-bit Address Register is available where required. Consult the section describing ROM Code Ordering Information for additional information.

I/O PIN CONCEPTUAL DIAGRAM WITH OUTPUT BUFFER OPTIONS

Figure 4



Ports 0 and 1 are Standard Output type only.

Ports 4 and 5 may both be any of the three output options (mask programmable bit by bit)

The $\overline{\text{STROBE}}$ output is always configured similar to a Direct Drive Output except that it is capable of driving 3 TTL loads.

$\overline{\text{RESET}}$ and EXT INT may have standard 6KΩ (typical) pull-up or may have no pull-up (mask programmable).

$\overline{\text{RESET}}$ and EXT INT do not have internal pull up on the MK38P70.

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MK3870 MAIN MEMORY

There are four address registers used to access main memory. These are the Program Counter (PO), the Stack Register (P), the Data Counter (DC), and the Auxiliary Data Counter (DC1). The Program Counter is used to address instructions or immediate operands. The Stack Register is used to save the contents of the Program Counter during an interrupt or subroutine call. Thus, the Stack Register contains the return address at which processing is to resume upon completion of the subroutine or interrupt routine. The Data Counter is used to address data tables. This register is auto-incrementing. Of the two data counters, only Data Counter (DC), can access the ROM. However, the XDC instruction allows the Data Counter and Auxiliary Data Counter to be exchanged.

The graph in Figure 3 shows the amounts of ROM and executable RAM for every available slash number in the MK3870 pin configuration.

EXECUTABLE RAM

The upper bytes of the address space in some of the MK3870 devices are RAM memory. As with the ROM memory, the RAM may be addressed by the PO and the DC address registers. The executable RAM may be addressed by all MK3870 instructions which address Main Memory. Additionally, the MK3870 may execute an instruction sequence which resides in the executable RAM. Note this cannot be done with the scratchpad RAM memory, which is the reason the term "executable RAM" is given to this additional memory.

I/O PORTS

The MK3870 provides four, 8 bit bidirectional Input/Output ports. These are ports 0, 1, 4, 5. In addition, the Interrupt Control Port is addressed as Port 6 and the binary timer is addressed as Port 7. The programming of Ports 6 and 7 and the bidirectional I/O pin are covered in the 3870 Family Technical Manual. The schematic of an I/O pin and available output drive options are shown in Figure 4.

An output ready strobe is associated with Port 4. This flag may be used to signal a peripheral device that the MK3870 has just completed an output of new data to Port 4. The strobe provides a single low pulse shortly after the output operation is completely finished, so either edge may be used to signal the peripheral. $\overline{\text{STROBE}}$ may also be used as an input strobe to Port 4 after completing the input operation.

MK38P70 GENERAL DESCRIPTION

The MK38P70 is the EPROM version of the MK3870. It retains an identical pinout with the MK3870, which is documented in the section of this data sheet entitled "FUNCTIONAL PIN DESCRIPTION". The MK38P70 is housed in two packages which incorporate a 28-pin socket located directly on top of the package. A number of standard EPROMs may be plugged into this socket.

The MK38P70 can act as an emulator for the purpose of verification of user code prior to the ordering of mask ROM MK3870 devices. Thus, the MK38P70 eliminates the need for emulator board products. In addition, several MK38P70s can be used in prototype systems in order to test design concepts in field service before committing to high-volume production with mask ROM MK3870s. The compact size of the MK38P70/EPROM combination allows the packaging of such prototype systems to be the same as that used in production. Finally, in low-volume applications, the MK38P70 can be used as the actual production device.

Most of the material which has been presented for the MK3870 in this document applies to the MK38P70. This includes the description of the pin configuration, architecture, programming model, and I/O ports. Additional information is presented in the following sections.

MK38P70 MAIN MEMORY

There are two basic versions of the MK38P70. These are the 97400 series and the 97500 series. The 97400 series parts have twelve bit address capability thus a total 4K memory map like the MK3870 ROM devices. The 97500 series has 16 bit address capability.

As can be seen from Figure 6, both the 97400 series and the 97500 series contain on-chip RAM in the upper portion of their memory maps and no on-chip ROM. Instead of on-chip ROM, address and data lines are brought out to the 28 pin socket located directly on top of the 40 pin package so that external memory devices (principally EPROMs) are addressed.

By using an external EPROM, the 38P70 may be used to emulate the 3870 ROM devices. The 97400 series can directly emulate the following devices.

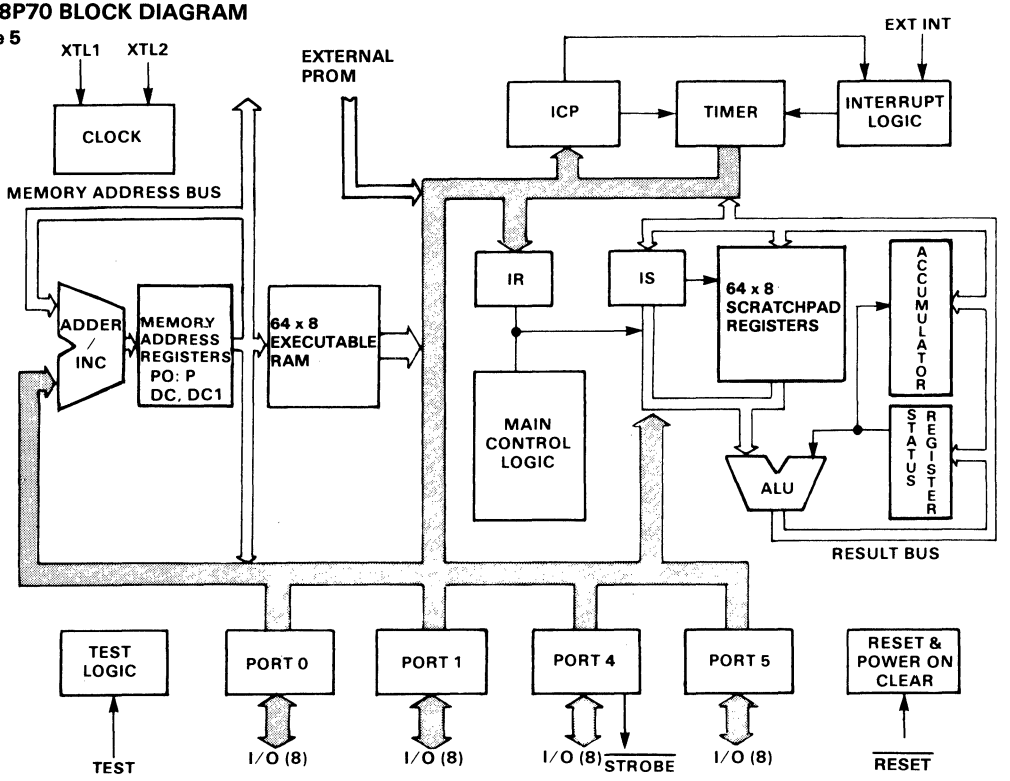
MK3870/10
MK3870/20
MK3870/22
MK3870/30
MK3870/42

The MK3807/40 cannot be emulated exactly by the 97400 series because the 97400 devices have the 64 bytes of RAM in the upper memory map while the 3870/40 provides ROM memory in this address space.

Besides the difference in the size of the address registers, 97500 series can also emulate many of the 3870 ROM devices. This difference in address capability should not cause any functional difference as long as normal programming practice is used. That is, as long as address roll-over or automatic truncation is not used. One such usage would be an end around branch (branching forward

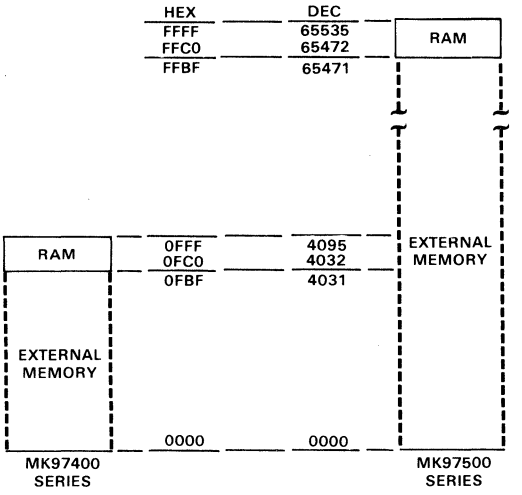
MK38P70 BLOCK DIAGRAM

Figure 5



MK38P70 MAIN MEMORY MAP

Figure 6



MK38P70 TYPE	SCRATCHPAD RAM SIZE (DECIMAL)	ADDRESS REGISTER SIZE	EXTERNALLY ADDRESSABLE MEMORY SIZE	INTERNAL EXECUTABLE RAM SIZE
97400 Series	64 bytes	12 bits	4032 bytes	64 bytes
97500 Series	64 bytes	16 bits	65472 bytes	64 bytes

MK38P70 devices have no internal ROM memory.

at upper memory to get to lower memory). Another case would be in using automatic truncation of data loaded into the 12 bit address registers on the ROM devices. For example, to access some particular location (03FF hex for example) via the data counter, one could load that address into DC using the DCI instruction. The instruction

DCI '73FF'

would cause 3FF to be loaded into the DC of the 3870 ROM device because the upper bits of the DC (bits 12-15) do not exist. If that instruction was followed by the LM instruction, the data stored at location 3FF would be obtained. The 97500 series devices would not truncate the 73FF address to 3FF. As previously stated, this type of programming is generally not done and thus the 97500 devices can be used to emulate the following devices directly.

MK3870/10
MK3870/20
MK3870/30
MK3870/40

The 97500 series can also be used to emulate the remainder of the 3870 devices as long as one accounts for the difference in the location of the RAM memory. In the 97500 devices, RAM is located at FFC0 through FFFF. While in 3870 devices this RAM (when it exists) is located at 0FC0 through 0FFF. When this minor difference is accounted for, the 97500 series will also emulate the following devices.

MK3870/22
MK3870/42

MK38P70 EPROM SOCKET

A 28 pin socket is located on top of the 40 pin package. When 24 pin memories are used, they are inserted so that pin 1 of the memory device is plugged into pin 3 of the socket (the 24 pin memory is lower justified in the 28 pin socket).

A 24 pin top socket was used so that the same package could be used for all 38P70 devices but could accommodate both 24 pin and 28 pin. Due to pin-out differences between various common memory devices, several different versions of the MK38P70 are provided with differing signals connected to particular pins on the 28 pin socket. Figure 7 shows the various options available.

MK38P70 I/O PORTS

For custom 3870 ROM codes, the user is given a bit by bit selection of I/O options on I/O ports 4 and 5. Additionally, the user has the option of selecting whether or not either $\overline{\text{RESET}}$ or EXT INT has an internal pull-up resistor. This flexibility allows about 172 million possible variations in I/O port and $\overline{\text{RESET}}$ and EXT INT configurations. Obviously, it is not practical to offer this variety in an "off the shelf" product like the 38P70. Thus a few variations are offered which still give some flexibility to the designer. The available I/O options are also shown in Figure 7.

28 PIN SOCKET SIGNALS

The 40 package pins are the identical signals that are provided with the MK3870 ROM devices. In addition to these 40 inputs and outputs, various other signals are implemented on the 38P70 die which are available for connection to the top socket. Depending upon the particular version, some subset of these signals are connected to the 28 pin socket. These signals are described below.

A_0 - A_{11} (97400 Series)
A_0 - A_{15} (97500 Series)

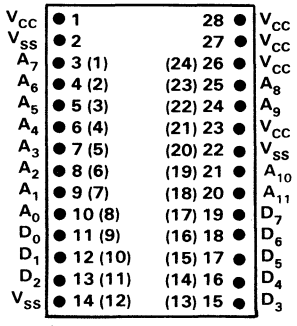
These are the address buses. They are always outputs and a new address will appear on this bus during each machine cycle. Normally this is the address of op-codes or operands, but there are machine cycles wherein no op-code or operand is required by the CPU. During these cycles, an address is still provided but the data that may be read from that address is not used.

D_0 - D_7 (97400 and 97500 Series)

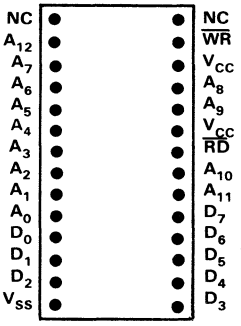
This is the bi-directional data bus for the external memory. Normally these lines are high impedance inputs. During op-code or operand reads, they receive data from the external memory and conduct it onto the internal 38P70 data bus. During those cycles wherein the operation is strictly internal to the 38P70, they remain hi-z inputs. Data may be presented to the 38P70 by an external memory device but it is not conducted onto the internal data bus. This includes machine cycles wherein op-codes or operands are read from the internal executable RAM. During the operand write machine cycle that occurs in the ST (store) instruction, they become push-pull outputs to conduct data to be written out to the external memory. However, if data is written to the internal executable RAM, this transaction is strictly internal and thus the data bus lines remain in their hi-z state. It, therefore, depends upon the address as to whether this bus becomes an active output bus or remains high impedance. If the address of the operand is not within the internal executable RAM space when a ST instruction is executed, D_0 - D_7 will become active outputs at the appropriate time, or else they will remain in the hi-z state. The 97400 devices do not provide a RD (read) control signal, nor is this signal provided on all versions of the 97500 series. Thus if a ST is executed with the operand address being that of external memory, that memory may access data and drive it onto D_0 - D_7 while the 38P70 is also driving data onto D_0 -D_7 and a bus conflict will result. This condition should be avoided; thus the user should note whether or not his external memory will drive D_0 - D_7 in this event. If it will drive D_0 - D_7, an ST with that operand address should be avoided. In general, one would not normally execute a write to a memory location where there is ROM or EPROM memory instead of RAM. However, some 3870 users have

DEVICE	PORT 4 I/O TYPE	PORT 5 I/O TYPE	SUPPORTS THESE MEMORY DEVICES	TOP 28 PIN SOCKET WIRING VERSION
MK97400	TTL	TTL	2716, 2516, 2532, 2758 MK34000 ROM	A
MK97410	Open Drain	Open Drain	2716, 2516, 2532, 2758 MK34000 ROM	A
MK97500	TTL	Open Drain	2716, 2516, 2532, 2758 MK34000 ROM	B
MK97501	TTL	Open Drain	2764, 2732, MK37000 ROM MK34000 ROM	C
MK97503	TTL	Open Drain	Use connector from 28 pin socket to memory bus	D

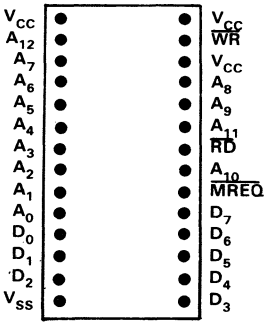
MK38P70 VERSIONS
Figure 7



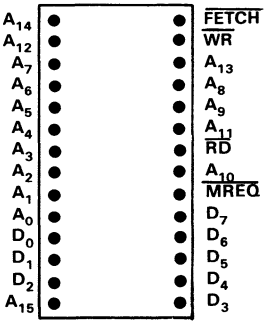
VERSION A



VERSION B



VERSION C



VERSION D

found the ST instruction useful even in devices like the 3870/20 which have no executable RAM. In this case it causes the data counter to increment (to perhaps totalize some event) but otherwise does nothing as one cannot write the internal ROM. No internal conflicts will occur if one attempts to write a 3870 ROM location. Most 97500 versions place a $\overline{RD}$ (read, active low) signal on the top socket pin which matches the $\overline{OE}$ (output enable, active low) input on most memories. Since $\overline{RD}$ will remain high during an operand write, the external memory would not have its data outputs enabled and no conflict will occur.

$\overline{MREQ}$ (97500 Series Only)

This is an active low output which occurs during each machine cycle. It goes high at the start of each cycle then goes low for the remainder of the cycle.

$\overline{RD}$ (97500 Series Only)

This is the active low read output which goes high at the start of each cycle then goes low if data (op-codes or operands) are to be read from external memory. During cycles wherein a strictly internal operation occurs, $\overline{RD}$ will remain high. It will also remain high during an operand write cycle.

$\overline{WR}$ (97500 Series Only)

This is the active low write control output. It is normally high but will go low then return high during an operand write if the address is not that of internal executable RAM.

$\overline{FETCH}$ (97500 Series Only)

This is the active low fetch status signal which signals that an op-code fetch occurred during that cycle. It is generated for use of the 97500 as a development system component.

It will go low during all op-code fetches whether from internal or external memory.

38P70 EXTERNAL MEMORY TIMING

The following Figures show the relative waveforms for the signals used to interface with external memory. The timing parameters are labeled. Their values are given in the A.C. Characteristics section of the Electrical Specifications.

97400 SERIES TIMING
Read Cycle
Figure 8

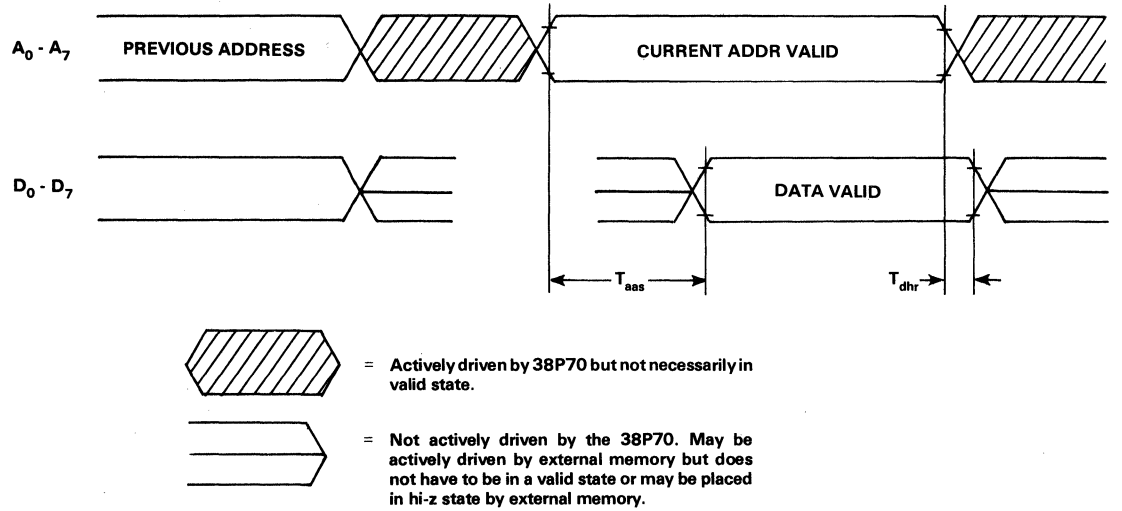
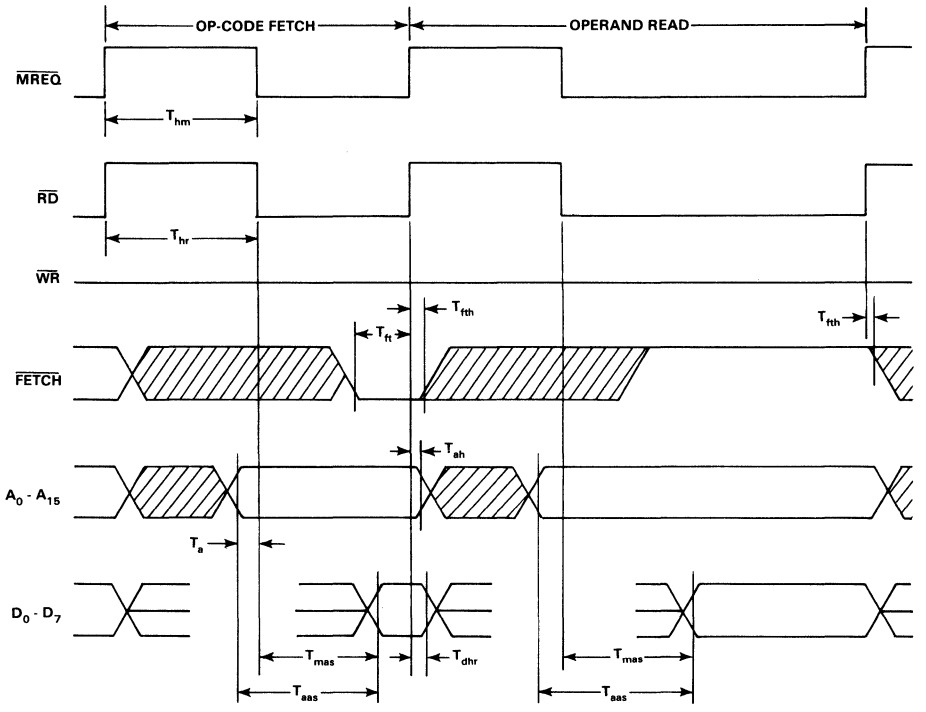


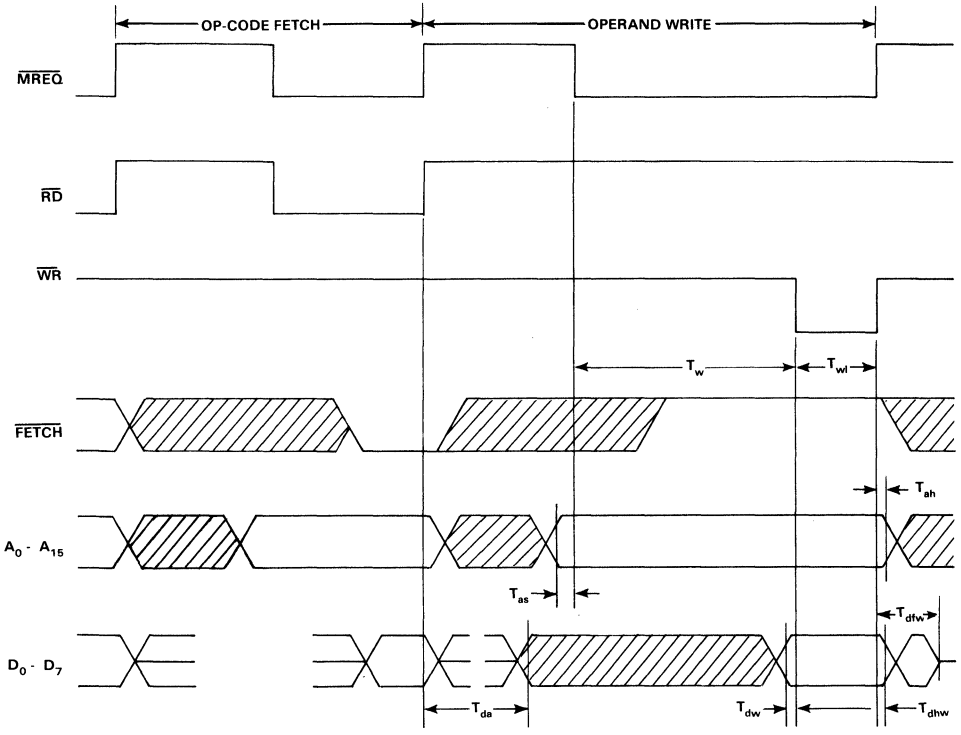
Figure 9



A. OP-CODE AND OPERAND READ FROM EXTERNAL MEMORY

VIII

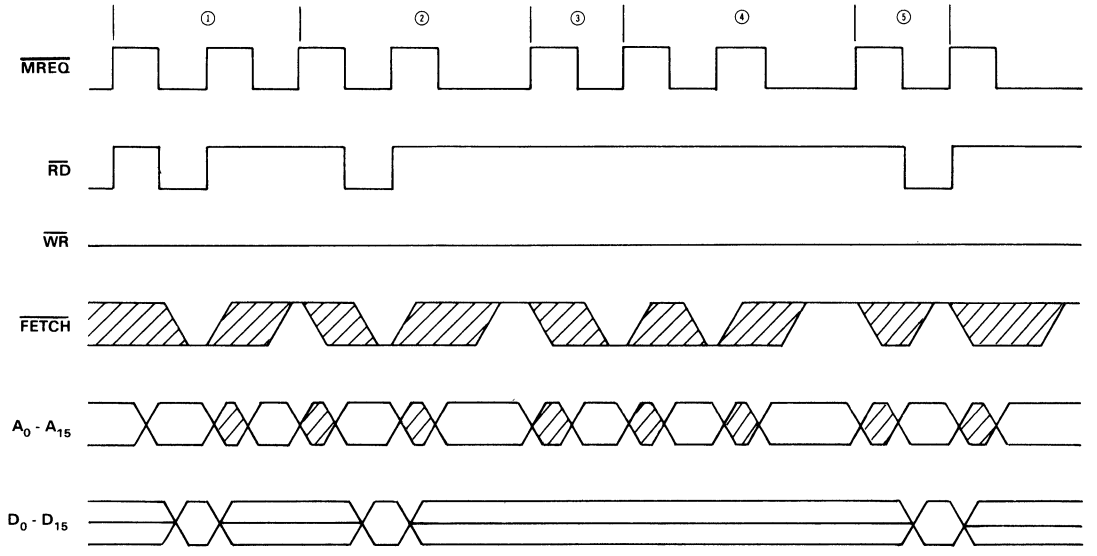
Figure 9



B. OPERAND WRITE TO EXTERNAL MEMORY

97500 SERIES TIMING (Continued)

Figure 9



C. EXAMPLES OF VARIOUS CYCLES

① Op-code fetch from external memory followed by an internal cycle (short cycle).
② Op-code fetch from external memory followed by an internal cycle (long cycle) such as an operand read or write internal executable RAM.
③ Op-code fetch from internal executable RAM.
④ Op-code fetch from internal executable RAM followed by a internal cycle (long cycle) such as an operand read or write of internal executable RAM.
⑤ First cycle of an interrupt acknowledge. Had an interrupt not occurred, this would have been an op-code fetch. If it would have been an external op-code fetch, $\overline{RD}$ will still go low but $\overline{FETCH}$ will not indicate a fetch cycle. Externally this would appear to be an operand read except that it occurs in a short cycle and all real operand reads occur in a long cycle.

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3870 TIME BASE OPTIONS

The 3870 contains an on-chip oscillator circuit which provides an internal clock. The frequency of the oscillator circuit is set from the external time base network. The time base for the 3870 may originate from one of four sources:

1) Crystal
2) LC Network
3) RC Network
4) External Clock

The type of network which is to be used with the mask ROM MK3870 must be specified at the time when mask ROM devices are ordered. However, the MK38P70 may operate with any of the four configurations so that it may emulate any configuration used with a mask ROM device.

The specifications for the four configurations are given in the following text. There is an internal 26 pF capacitor between XTL 1 and GND and an internal 26 pF capacitor between XTL 2 and GND. Thus, external capacitors are not necessarily required. In all external clock modes the external time base frequently is divided by two to form the internal PHI clock.

CRYSTAL SELECTION

The use of a crystal as the time base is highly recommended as the frequency stability and reproduction from system to system is unsurpassed. The 3870 has an internal divide by two to allow the use of inexpensive and widely available TV Color Burst Crystals (3.58 MHz). Figure 11 lists the required crystal parameters for use with the 3870. The Crystal Mode time base configuration is shown in Figure 10.

Through careful buffering of the XTL1 pin it may be possible to amplify this waveform and distribute it to other devices. However, Mostek recommends that a separate active device (such as a 7400 series TTL gate) be used to oscillate the crystal and that the waveform from that oscillator be buffered and supplied to all devices, including the 3870, if a single crystal is to provide the time base for more than just a single 3870.

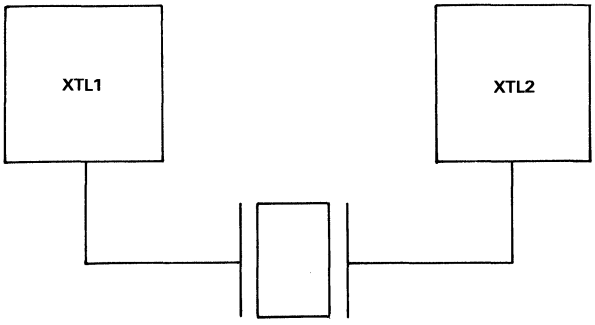
While a ceramic resonator may work with the 3870 crystal oscillator, it was designed specifically to support the use of this component. Thus, Mostek does not support the use of a ceramic resonator either through proper testing, parametric specification, or applications support.

LC NETWORK

The LC time base configuration can be used to provide a less expensive time base for the 3870 than can be provided with a crystal. However, the LC configuration is much less accurate than is the crystal configuration. The LC time base configuration is shown in Figure 12. Also shown in the figure are the specified parameters for the LC components, along with the formula for calculating the resulting time base frequency. The minimum value of the inductor which is required for proper operation of the LC time base network is 0.1 millihenries. The inductor must have a Q factor which is no less than 40. The value of C is derived from C external, the internal capacitance of the 3870, C_{XTL}, and the stray

CRYSTAL MODE CONNECTION

Figure 10



AT - CUT

CRYSTAL PARAMETERS

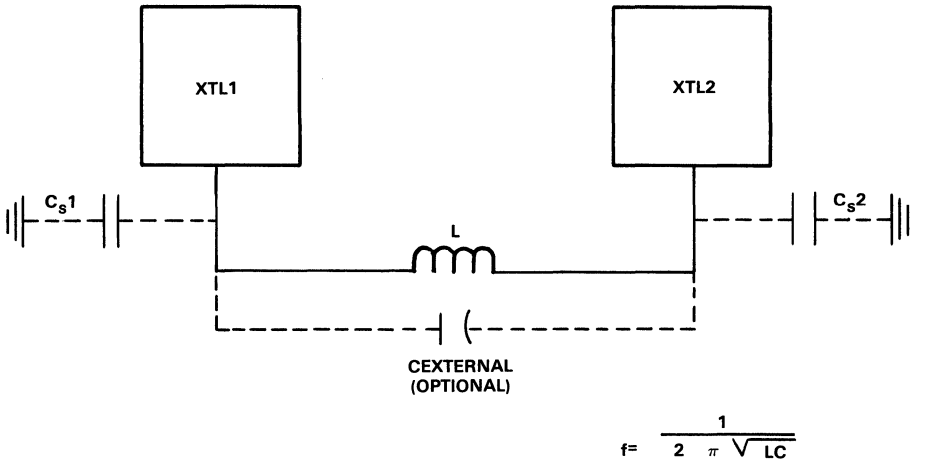
Figure 11

a) Parallel resonance, fundamental mode AT-Cut
b) Shunt capacitance (C_0) = 7 pf max.
c) Series resistance (R_S) = See table
d) Holder = See table below.

Frequency	Series Resistance	Holder
f = 2-2.7 MHz	Rs = 300 ohms max	HC-6 HC-33
f = 2.8-4 MHz	Rs = 150 ohms max	HC-6 HC-18* HC-25* HC-33

*This holder may not be available at frequencies near the lower end of this range.

LC MODE CONNECTION
Figure 12



capacitances, C_{S1} and C_{S2}. C_{XTL} is the capacitance looking into the internal two port network at XTL1 and XTL2. C_{XTL} is listed under the "Capacitance" section of the Electrical Specifications. C_{S1} and C_{S2} are stray capacitances from XTL1 to ground and from XTL2 to ground, respectively. C external should also include the stray shunt capacitance across the inductor. This is typically in the 3 to 5 pf range and significant error can result if it is not included in the frequency calculation.

Variation in time base frequency with the LC network can arise from one of four sources: 1) Variation in the value of the inductor. 2) Variation in the value of the external capacitor. 3) Variation in the value of the internal capacitance of the 3870 at XTL1 and XTL2 and 4) Variation in the amount of stray capacitance which exists in the circuit. Therefore, the actual frequency which is generated by the LC circuit is within a range of possible frequencies, where the range of frequencies is determined by the worst case variation in circuit parameters. The designer must select component values such that the range of possible frequencies with the LC mode does not go outside of the specified operating frequency range for the 3870.

RC CLOCK CONFIGURATION

The time base for the 3870 may be provided from an RC network tied to the XTL2 pin, when XTL1 is grounded. A schematic picturing the RC clock configuration is shown in Figure 13. The RC time base configuration is intended to provide an inexpensive time base source for applications in which timing is not critical. Some users have elected to tune each unit using a variable resistor or external capacitor thus reducing the variation in frequency. However, for increased time base accuracy, Mostek recommends the use of the Crystal or LC time base configuration. Figure 14 illustrates a curve which gives the resulting operating frequency for a particular RC value. The x-axis represents the product of the value of the resistor times the value of the capacitor. Note that three curves are actually shown. The curve in the middle represents the nominal frequency obtained for a given value of RC. A maximum curve and a minimum curve for different types of 3870 devices are also shown in the diagram.

The designer must select the RC product such that a frequency of less than 2 MHz is not possible, taking into account the maximum possible RC product and using the minimum curve shown in Figure 14 below. Also, the RC product must not allow a frequency of more than 4 MHz, taking into account the minimum possible R and C and using the Maximum curve shown below. Temperature induced variations in the external components should be considered in calculating the RC product.

Frequency variation from unit to unit owing to switching speed and level at constant temperature and V_{CC} = + or – 5 percent.

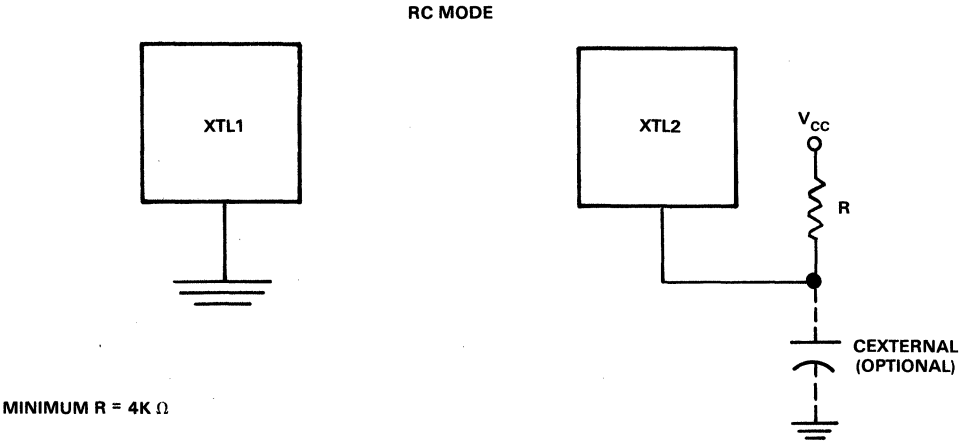
Frequency variation due to V_{CC} with all other parameters constant with respect to +5V = +7 percent to –4 percent on all devices.

Frequency variation due to temperature with respect to 25 C (all other parameters constant) is as follows:

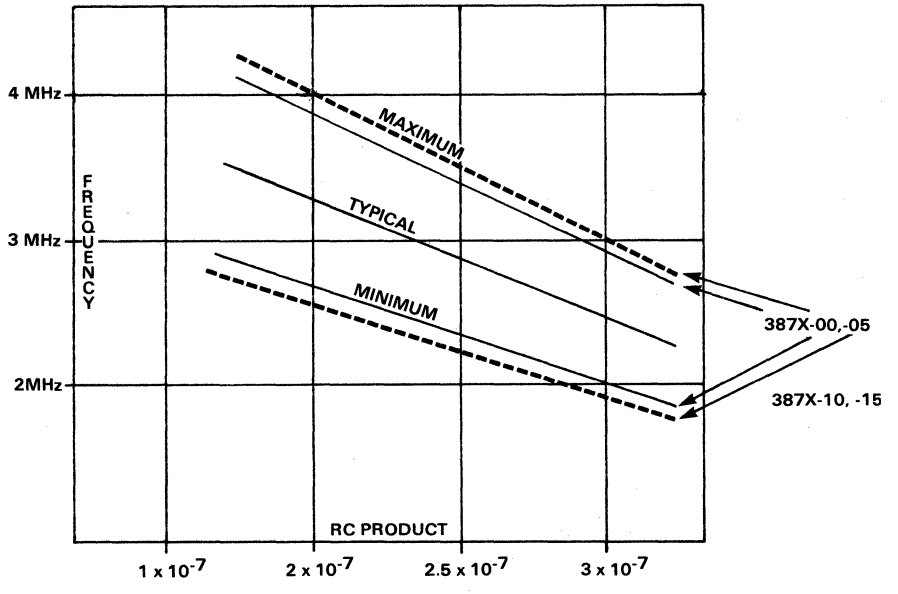
PART #	VARIATION
387X-00, -05	+6 percent to – 9 percent
387X-10, -15	+9 percent to –12 percent

VIII

RC MODE CONNECTION
Figure 13



FREQUENCY VS. RC
Figure 14



Variations in frequency due to variations in RC components may be calculated as follows:

Maximum RC = (R max) (C external max + C_{XTL} max)

Minimum RC = (R min) (C external min + C_{XTL} min)

Typical RC = (R typ) (C external typ + $\frac{\{C_{XTL} \text{ max} + C_{XTL} \text{ min}\}}{2}$)

Positive Freq. Variation = $\frac{\text{RC typical - RC minimum}}{\text{RC typical}}$

Negative Freq. Variation due to RC Components = $\frac{\text{RC maximum - RC typical}}{\text{RC typical}}$

Total frequency variation due to all factors:

387X-00, -05
= +18 percent plus positive frequency variation due to RC components

387X-10, -15
= +21 percent plus positive frequency variation due to RC components

= -18 percent minus negative frequency variation due to RC components

= -21 percent minus negative frequency variation due to RC components

Total frequency variation due to V_{CC} and temperature of a unit tuned to frequency at +5V V_{CC}, 25 C

387X-00, -05
= + 13 percent

387X-10, -15
= + 16 percent

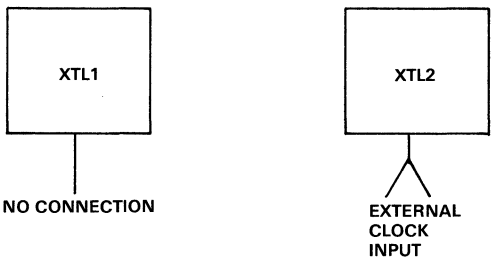
EXTERNAL CLOCK CONFIGURATION

The connection for the external clock time base configuration is shown in Figure 15. Refer to the DC Characteristics section for proper input levels and current requirements.

Refer to the Capacitance section of the appropriate 3870 Family device data sheet for input capacitance.

EXTERNAL MODE CONNECTION

Figure 15



VIII

OPERATING VOLTAGES AND TEMPERATURES

Dash Number Suffix	Operating Voltage V_{CC}	Operating Temprature T_A
— 00	+5V ± 10%	0°C - 70°C
— 05	+5V ± 5%	0°C - 70°C
— 10	+5V ± 10%	-40°C - +85°C
— 15	+5V ± 5%	-40°C - +85°C

See Ordering Information for explanation of part numbers.

ABSOLUTE MAXIMUM RATINGS*

	-00, -05	-10, -15
Temperature Under Bias	-20°C to +85°C	-50°C to +100°C
Storage Temperature	-65°C to +150°C	-65°C to +150°C
Voltage on any Pin With Respect to Ground (Except open drain pins and TEST)	-1.0V to +7V	-1.0V to +7V
Voltage on TEST with Respect to Ground	-1.0V to +9V	-1.0V to +9V
Voltage on Open Drain Pins With Respect to Ground	-1.0V to +13.5V	-1.0V to +13.5V
Power Dissipation	1.5W	1.5W
Power Dissipation by any one I/O pin	60mW	60mW
Power Dissipation by all I/O pins	600mW	600mW

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

AC CHARACTERISTICS

T_A, V_{CC} within specified operating range.
I/O power dissipation ≤ 100mW (Note 2)

SIGNAL	SYM	PARAMETER	-00,-05 MIN	-00,-05 MAX	-10,-15 MIN	-10,-15 MAX	UNIT	NOTES
XTL1 XTL2	t_O	Time Base Period, all clock modes	250	500	250	500	ns	4MHz-2MHz
	$t_{ex(H)}$	External clock pulse width high	90	400	100	390	ns	
	$t_{ex(L)}$	External clock pulse width low	100	400	110	390	ns	
Φ	t_Φ	Internal Φ clock	$2t_O$		$2t_O$			
WRITE	t_W	Internal WRITE Clock period	4tΦ 6tΦ		4tΦ 6tΦ			Short Cycle Long Cycle
I/O	$t_{dI/O}$	Output delay from internal WRITE clock	0	1000	0	1200	ns	50pF plus one TTL load
	$t_{sI/O}$	Input setup time to internal WRITE clock	1000		1200		ns	
$\overline{STROBE}$	$t_{I/O-s}$	Output valid to $\overline{STROBE}$ delay	3tΦ -1000	3tΦ +250	3tΦ -1200	3tΦ +300	ns	I/O load = 50pF + 1 TTL load
	t_{sL}	$\overline{STROBE}$ low time	8tΦ -250	12tΦ +250	8tΦ -300	12tΦ +300	ns	$\overline{STROBE}$ load= 50pF + 3TTL loads
$\overline{RESET}$	t_{RH}	$\overline{RESET}$ hold time, low	6tΦ +750		6tΦ +1000		ns	
	t_{RPOC}	$\overline{RESET}$ hold time, low for power clear	power supply rise time +0.1		power supply rise time +.1		ms	
EXT INT	t_{EH}	EXT INT hold time in active and inactive state	6tΦ +750		6tΦ +1000		ns	To trigger interrupt
			2tΦ		2tΦ		ns	To trigger timer

AC CHARACTERISTICS FOR MK38P70 Signals brought to top 28 pin socket.
T_A, V_{CC} within specified operating range.
I/O Power Dissipation ≤ 100 mW (Note 2)
97400 Series (See Note 3)

SYMBOL	PARAMETER	-00, -05		-10, -15		UNIT	CONDITION
		MIN	MAX	MIN	MAX		
t_{aas}	External memory required access time from A_0-A_{11} stable	3tΦ -850		3tΦ -850		ns	C_L A_0-A_{11} = 50 pF

97500 Series (See Note 3)

SIGNAL	SYMBOL	PARAMETER	-00, -05		-10, -15		UNITS	CONDITION
			MIN	MAX	MIN	MAX		
$\overline{MREQ}$	T_{hm}	$\overline{MREQ}$ high time	2tΦ -100		2tΦ -100		ns	Load = 50 pF + 1 TTL load
$\overline{RD}$	T_{hr}	$\overline{RD}$ high time	2tΦ -100		2tΦ -100		ns	Load = 50 pF + 1 TTL load
$\overline{WR}$	T_w	$\overline{WR}$ low from $\overline{MREQ}$ low	3tΦ -200	3tΦ +100	3tΦ -200	3tΦ +100	ns	Load = 50 pF + 1 TTL load
	T_{wl}	$\overline{WR}$ low time	tΦ -100	tΦ +100	tΦ -100	tΦ +100	ns	
$\overline{FETCH}$	T_{ft}	$\overline{FETCH}$ stable prior to rising $\overline{MREQ}$	650	650	650	650	ns	Load = 50 pF + 1 TTL Load
	T_{fh}	$\overline{FETCH}$ hold time after $\overline{MREQ}$ high	20		20		ns	Load = 20 pF
A_0 - A_{15}	T_a	Address stable prior to $\overline{RD}$ or $\overline{MREQ}$ falling	tΦ -400		tΦ -400		ns	Load = 50 pF + 1 TTL load
	T_{ah}	Address hold time after $\overline{MREQ}$, $\overline{RD}$, or $\overline{WR}$ high	15		15		ns	Load = 20 pF
D_0 - D_7	T_{aas}	External memory required access time from	3tΦ -850		3tΦ -850		ns	
	T_{mas}	External memory required access time from $\overline{MREQ}$ or $\overline{RD}$ low	2tΦ -450		2tΦ -450		ns	
	T_{dhr}	Required data hold time after $\overline{MREQ}$ rising	0		0		ns	
	T_{da}	Data bus active after $\overline{MREQ}$ or $\overline{RD}$ high	tΦ		tΦ			
	T_{dw}	Data stable prior to $\overline{WR}$ falling	5tΦ -2250		5tΦ -2250		ns	Load = 50 pF + 1 TTL load
	T_{dhr}	Data hold after $\overline{WR}$ high	15		15		ns	Load = 20 pF
	T_{dfw}	Data bus delay to float after $\overline{MREQ}$ rising		200		200	ns	

VIII

CAPACITANCE
T_A = 25°C
All Part Numbers

SYM	PARAMETER	MIN	MAX	UNIT	NOTES
C_{IN}	Input capacitance		10	pF	unmeasured pins grounded
C_{XTL}	Input capacitance; XTL1, XTL2	23.5	29.5	pF	

DC CHARACTERISTICS
T_A, V_{CC} within specified operating range
I/O power dissipation ≤ 100 mW (Note 2)

SYMBOL	PARAMETER	-00, -05		-10, -15		UNIT	DEVICE
		MIN	MAX	MIN	MAX		
I_{CC}	Average Power Supply Current		85		110	mA	MK3870/10 Outputs Open
			94		125	mA	MK3870/12 Outputs Open
			85		110	mA	MK3870/20 Outputs Open
			94		125	mA	MK3870/22 Outputs Open
			100		130	mA	MK3870/30 Outputs Open
			100		130	mA	MK3870/32 Outputs Open
			100		130	mA	MK3870/40 Outputs Open
			100		130	mA	MK3870/42 Outputs Open
			125		150	mA	MK38P70/X2 No EPROM, Outputs Open

DC CHARACTERISTICS (cont.)

SYMBOL	PARAMETER	-00, -05		-10, -15		UNIT	DEVICE
		MIN	MAX	MIN	MAX		
P_D	Power Dissipation		400		525	mW	MK3870/10 Outputs Open
			440		575	mW	MK3870/12 Outputs Open
			400		525	mW	MK3870/20 Outputs Open
			440		575	mW	MK3870/22 Outputs Open
			475		620	mW	MK3870/30 Outputs Open
			475		620	mW	MK3870/32 Outputs Open
			475		620	mW	MK3870/40 Outputs Open
			475		620	mW	MK3870/42 Outputs Open
			600		750	mW	MK38P70/X2 No EPROM, Outputs Open

VIII

DC CHARACTERISTICS (cont.)

T_A, V_{CC} within specified operating range, I/O power dissipation ≤ 100mW (Note 2)

SYM	PARAMETER	-00,-05		-10,-15		UNIT	CONDITIONS
		MIN	MAX	MIN	MAX		
V_{IHEX}	External Clock input high level	2.4	5.8	2.4	5.8	V	
V_{ILEX}	External Clock input low level	-.3	.6	-.3	.6	V	
I_{IHEX}	External Clock input high current		100		130	μA	$V_{IHEX}=V_{CC}$
I_{ILEX}	External Clock input low current		-100		-130	μA	$V_{ILEX}=V_{SS}$
$V_{IHI/O}$	Input high level, I/O pins	2.0	5.8	2.0	5.8	V	Standard pull-up
		2.0	13.2	2.0	13.2	V	Open drain (1)
V_{IHR}	Input high level, $\overline{RESET}$	2.0	5.8	2.2	5.8	V	Standard pull-up
		2.0	13.2	2.2	13.2	V	No Pull-up
V_{IHEI}	Input high level, EXT INT	2.0	5.8	2.2	5.8	V	Standard pull-up
		2.0	13.2	2.2	13.2	V	No Pull-up
V_{IL}	Input low level	-.3	.8	-.3	.7	V	(1)
I_{IL}	Input low current, all pins with standard pull-up resistor		-1.6		-1.9	mA	$V_{IN}=0.4V$
I_L	Input leakage current, open drain pins, and inputs with no pull-up resistor		+10 -5		+18 -8	μA μA	$V_{IN}=13.2V$ $V_{IN}=0.0V$
I_{OH}	Output high current pins with standard pull-up resistor	-100 -30		-89 -25		μA μA	$V_{OH}=2.4V$ $V_{OH}=3.9V$
I_{OHDD}	Output high current, direct drive pins	-100 -1.5	 -8.5	-80 -1.3	 -11	μA mA mA	$V_{OH}=2.4V$ $V_{OH}=1.5V$ $V_{OH}=0.7V$
I_{OHS}	$\overline{STROBE}$ Output High current	-300		-270		μA	V_{OH} = 2.4V
I_{OL}	Output low current	1.8		1.65		mA	$V_{OL}=0.4V$
I_{OLS}	$\overline{STROBE}$ Output Low current	5.0		4.5		mA	$V_{OL}=0.4V$

DC CHARACTERISTICS FOR MK38P70

Signals brought to top 25 pin socket
T_A, V_{CC} within specified range
I/O Power Dissipation ≤ 100 mW (Note 2)

97400, 97500 Series

SYMBOL	PARAMETER	-00, -05 MIN	-00, -05 MAX	-10, -15 MIN	-10, -15 MAX	UNIT	CONDITION
V_{IH}	Input high level (D_0 - D_7)	2.0	V_{CC} +.3	2.1	V_{CC} +.3	V	D_0 - D_7 in Hi-z input mode
V_{IL}	Input low level (D_0 - D_7)	V_{SS} -.3	.8	V_{SS} -.3	.7	V	
I_L	Input Leakage (D_0 - D_7)		±10		±15	μA	
V_{OH}	Output high level (all outputs and D_0-D_7 in output mode)	2.4		2.4		V	
V_{OL}	Output low level (all outputs and D_0-D_7 in output mode)		.4		.4	V	
I_{OH}	Output source current (all outputs and D_0-D_7 in output mode)	-100		-90		μA	V_{OH} = 2.4 V
I_{OL}	Output sink current (all outputs and D_0-D_7 in output mode)	1.8		1.65		mA	V_{OL} = .4 V
R_{CC}	Package resistance from device pin 40 to top socket V_{CC} pin(s)					Ω	Pin 28, 27, or 26 when V_{CC}
						Ω	Pin 1 if V_{CC}
						Ω	Pin 23 if V_{CC}
R_{SS}	Package resistance from device pin 20 to top socket V_{SS} pin(s)					Ω	Pin 14 when V_{SS}
						Ω	Pin 2 or 22 when V_{SS}
I_{CC}	Supply current available from top socket V_{CC} pin(s)		-185		-185	mA	Σl pin 28 27, 26 when V_{CC}
			-20		-20	mA	Pin 1 if V_{CC}
			-10		-10	mA	Pin 23 if V_{CC}
I_{SS}	Supply current available from top socket V_{SS} pin(s)		190		190	mA	Pin 14 if V_{SS}
			2		2	mA	Pin 2 if V_{SS}
			2		2	mA	Pin 22 if V_{SS}

NOTES:

1. $\overline{\text{RESET}}$ and EXT INT have internal Schmit triggers giving minimum .2 V hysteresis.
2. Power dissipation for I/O pins is calcualted by $\Sigma(V_{CC} - V_{IL})(|I_{IL}|) = \Sigma(V_{CC}-V_{OH})(|I_{OH}|) = \Sigma(V_{OH})(I_{OL})$
3. AC timing for external memory signals on 38P70 are measured from either the .8 or 2.0 volt points as applicable. High means at or above 2.0 volts. Low means at or below .8 volts. Stable means high or low as appropriate. Rising means signal is no longer below .8 volts. Falling means signal is no longer above 2.0 volts. Hold times on outputs assume full rated load on reference signal and 20 pf load on specified signal. For 97400 series, only applicable specification is Taas as no other signals are available to reference to other than A_0-A_{11}.

TIMER AC CHARACTERISTICS

Definitions:
Error = Indicated time value - actual time value

tpsc = tΦ x Prescale Value

Interval Timer Mode:

Single interval error, free running (Note 3) ..... ±6tΦ
Cumulative interval error, free running (Note 3) 0

Error between two Timer reads (Note 2) ..... ± (tpsc + tΦ)
Start Timer to stop Timer error (Notes 1, 4) ..... + tΦ to - (tpsc + tΦ)
Start Timer to read Timer error (Notes 1, 2) ..... -5tΦ to - (tpsc + 7tΦ)
Start Timer to interrupt request error (Notes 1, 3) ..... -2tΦ to -8tΦ
Load Timer to stop Timer error (Note 1) ..... + tΦ to - (tpsc + 2tΦ)
Load Timer to read Timer error (Notes 1, 2) ..... -5t ± to - (tpsc + 8t ±)
Load Timer to interrupt request error (Notes 1, 3) ..... -2tΦ to -9tΦ

Pulse Width Measurement Mode:

Measurement accuracy (Note 4) ..... + tΦ to -(tpsc + 2tΦ)
Minimum pulse width of EXT INT pin 2tΦ

Event Counter Mode:

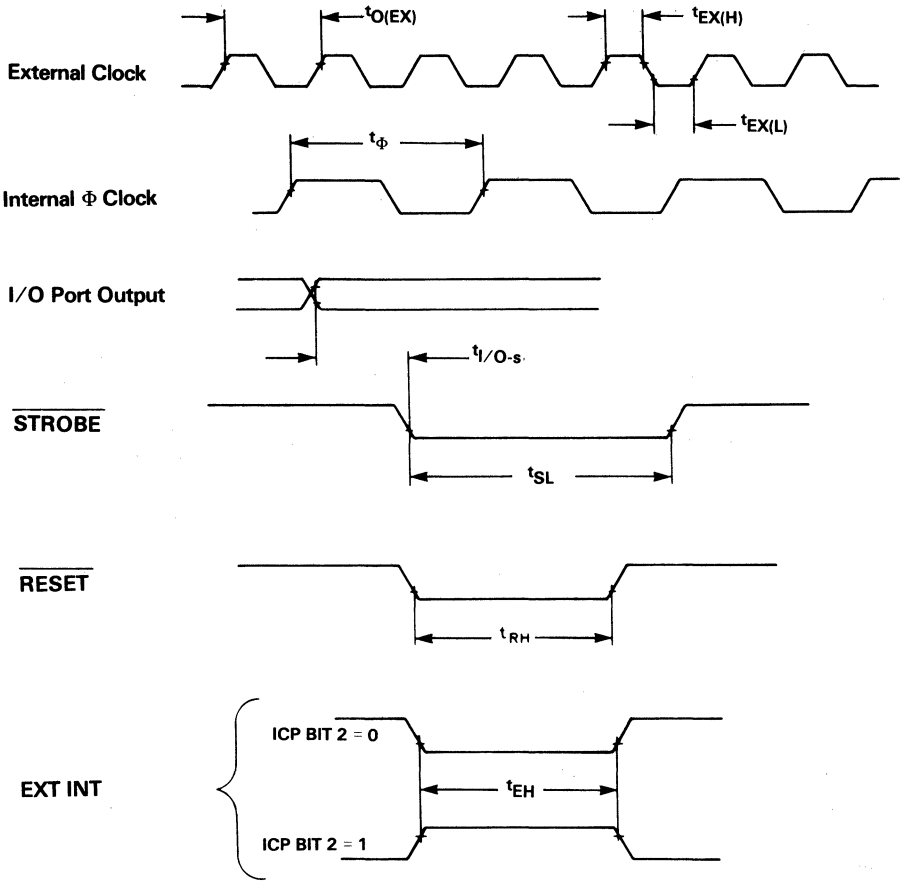
Minimum active time of EXT INT pin 2tΦ
Minimum inactive time of EXT INT pin 2tΦ

Notes:

1. All times which entail loading, starting, or stopping the Timer are referenced from the end of the last machine cycle of the OUT or OUTS instruction.
2. All times which entail reading the Timer are referenced from the end of the last machine cycle of the IN or INS instruction.
3. All times which entail the generation of an interrupt request are referenced from the start of the machine cycle in which the appropriate interrupt request latch is set. Additional time may elapse if the interrupt request occurs during a privileged or multicycle instruction.
4. Error may be cumulative if operation is repetitively performed.

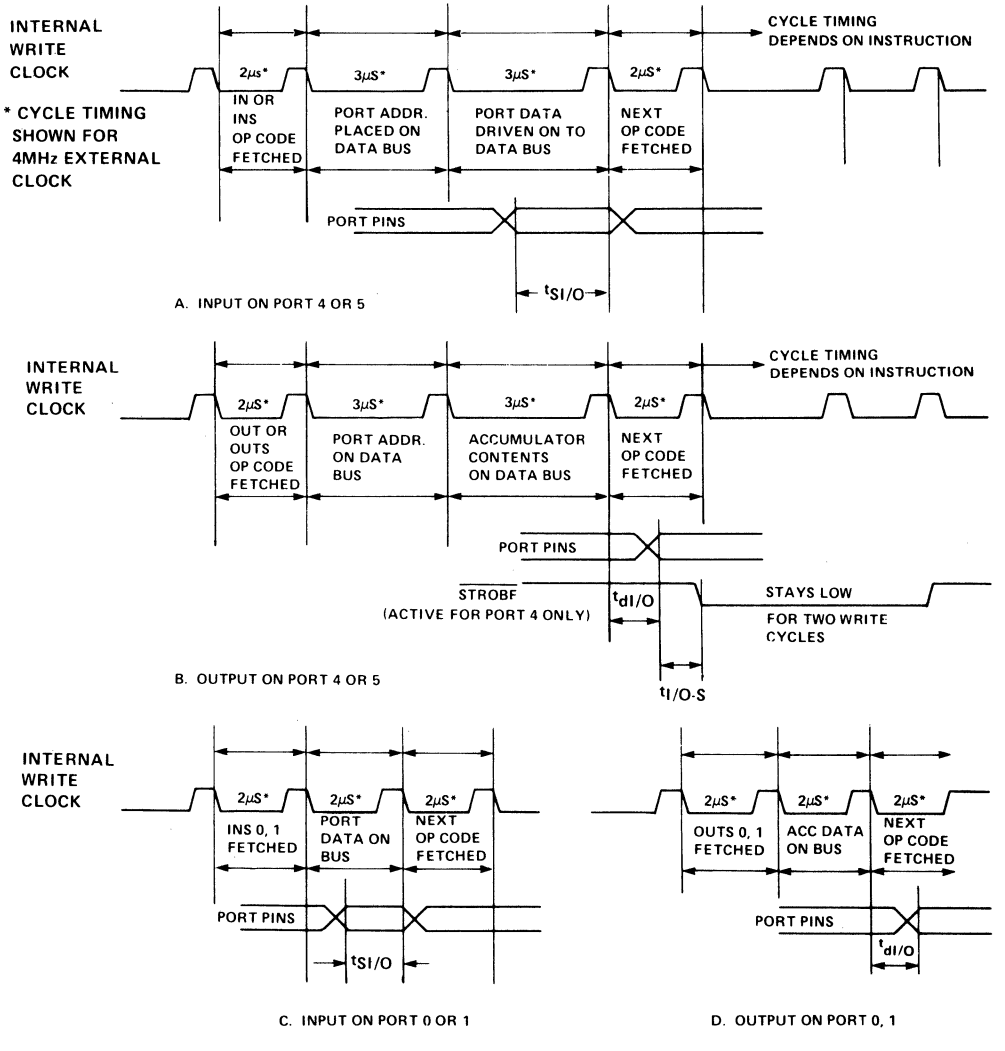
AC TIMING DIAGRAM

Figure 16



Note: All AC measurements are referenced to V_{IL} max., V_{IH} min., V_{OL} (.8v), or V_{OH} (2.0v).

INPUT/OUTPUT AC TIMING
Figure 17

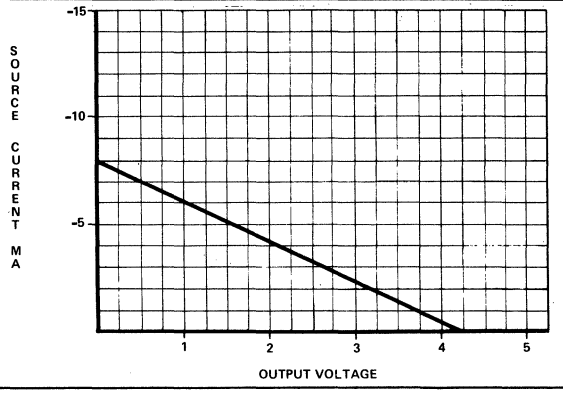


VIII

STROBE SOURCE CAPABILITY

(TYPICAL AT V_{CC} = 5 V, T_A = 25°C)

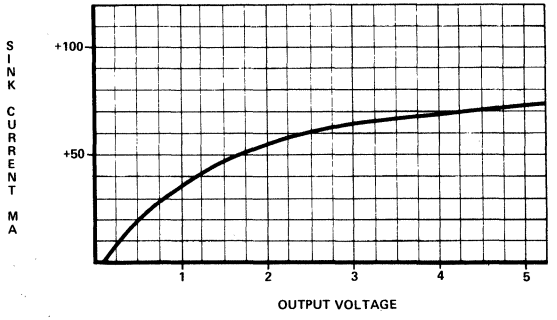
Figure 18



STROBE SINK CAPABILITY

(TYPICAL AT V_{CC} = 5 V, T_A = 25°C)

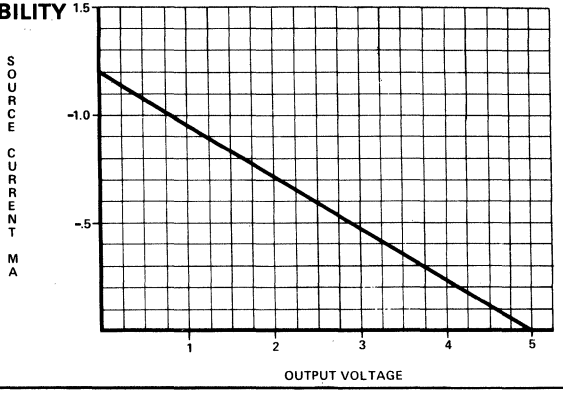
Figure 19



STANDARD I/O PORT SOURCE CAPABILITY

(TYPICAL AT V_{CC} = 5 V, T_A = 25°C)

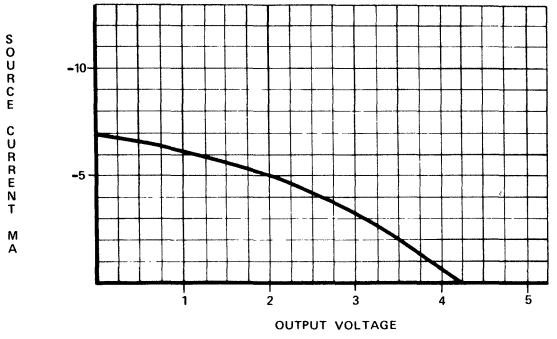
Figure 20



DIRECT DRIVE I/O PORT SOURCE CAPABILITY

(TYPICAL AT V_{CC} = 5 V, T_A = 25°C)

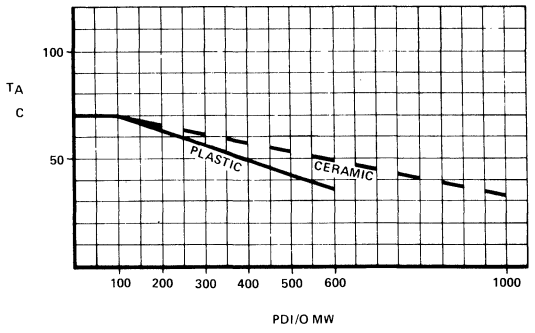
Figure 21



I/O PORT SINK CAPABILITY

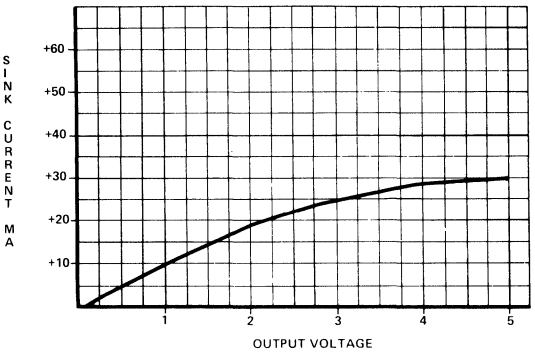
(TYPICAL AT V_{CC} = 5 V, T_A = 25°C)

Figure 22



MAXIMUM OPERATING TEMPERATURE VS. I/O POWER DISSIPATION

Figure 23



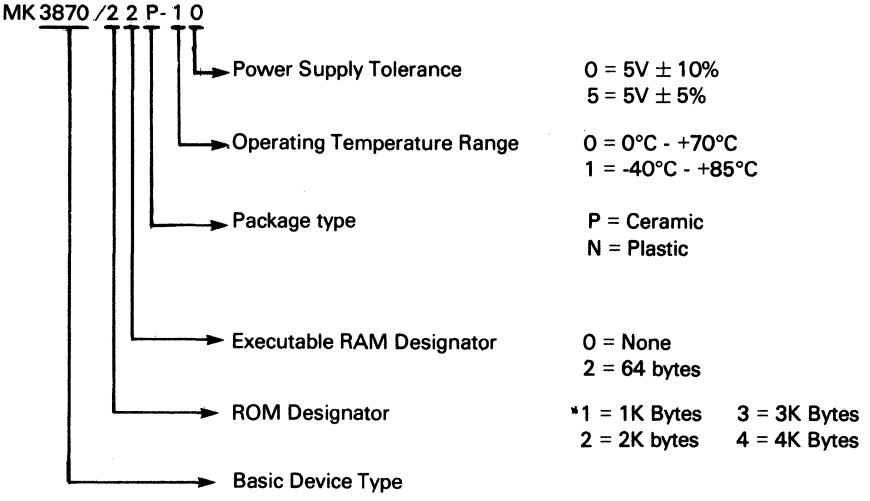
VIII

ORDERING INFORMATION

There are two types of part numbers for the 3870 family of devices. The generic part number describes the basic device type, the amount of ROM and Executable RAM, the desired package type, temperature range, and power supply tolerance. For each customer specific code, additional information defining I/O options and oscillator options will be combined with the information described in the generic part number to define a customer/code specific device order number. Note: the specific device order number will be used to differentiate between the MK3870/20 with 12-bit Address Registers and the original 3870 with 11-bit Address Register, as mentioned in an earlier section.

GENERIC PART NUMBER

An example of the generic part number is shown below.

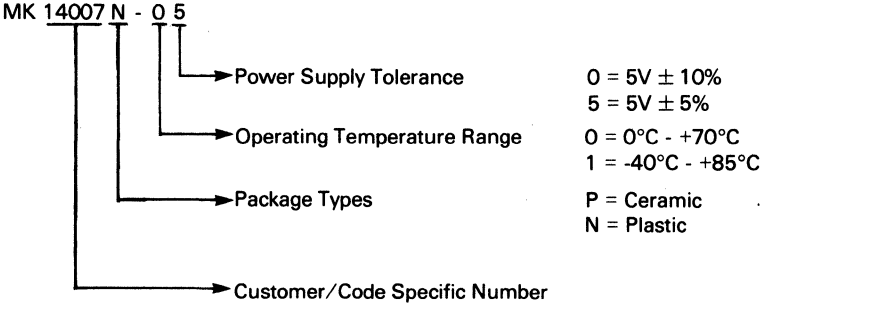


An example of the generic part number for the EPROM device is shown below.

MK38P70/02 R-05

DEVICE ORDER NUMBER

An example of the device order number is shown below.



The Customer/Code specific number defines the ROM bit pattern, I/O configuration, oscillator type, and generic part type to be used to satisfy the requirements of a particular customer purchase order. For further information on the ordering of mask ROM devices, the customer should refer to the 3870 Family Technical Manual.

PRELIMINARY

MOSTEK®

MICROCOMPUTER COMPONENTS

3870 Single Chip Micro Family

MK2870

MK2870 FEATURES

- 28 pin version of the industry standard MK3870 single chip microcomputer
- Available with 1K or 2K bytes of mask programmable ROM memory
- 64 bytes scratchpad RAM
- Available with additional 64 bytes executable RAM
- 20 bits TTL compatible I/O
- Programmable binary timer
  Interval timer mode
  Pulse width measurement mode
  Event counter mode
- External interrupt input
- Crystal, LC, RC, or external time base options
- Low power (275 mW typ.)
- Single +5 volt supply

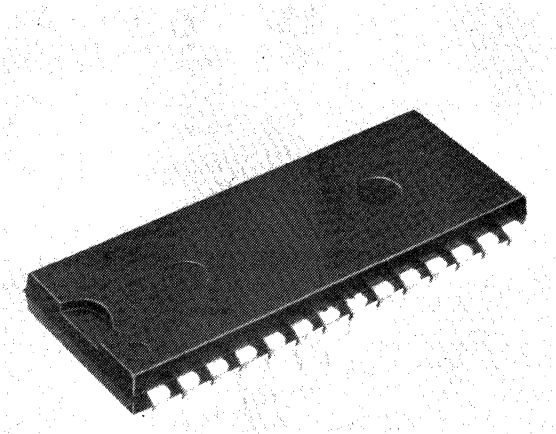
GENERAL DESCRIPTION

The MK2870 is the 28 pin version of the industry standard Mostek MK3870 single chip microcomputer. It is offered as a low cost device which can be used in those applications that do not require the entire I/O capability of the 40 pin MK3870. The compact 28 pin package makes the MK2870 ideally suited for applications where PC board space is a premium.

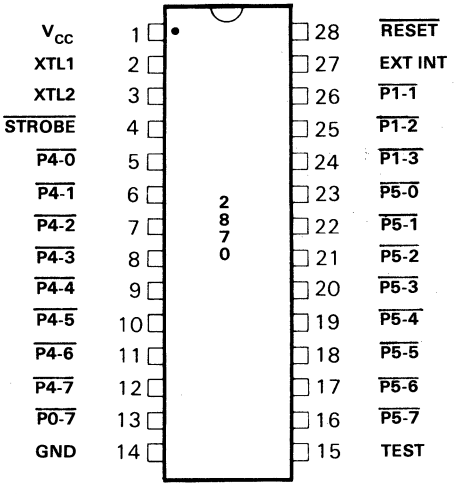
The MK2870 can execute more than 70 instructions, and is completely software compatible with the rest of the devices in the 3870 family. The MK2870 features 1K or 2K bytes of ROM and optional additional executable RAM depending on the specific part type designated by a slash number suffix. The MK2870 also features 64 bytes of scratchpad RAM, a programmable binary timer, and 20 bits of I/O.

The programmable binary timer operates by itself in the interval timer mode or in conjunction with the external interrupt input in the pulse width measurement and the event counter modes of operation. Two sources of vectored, prioritized interrupt are provided with the binary timer and

MK2870
Figure 1



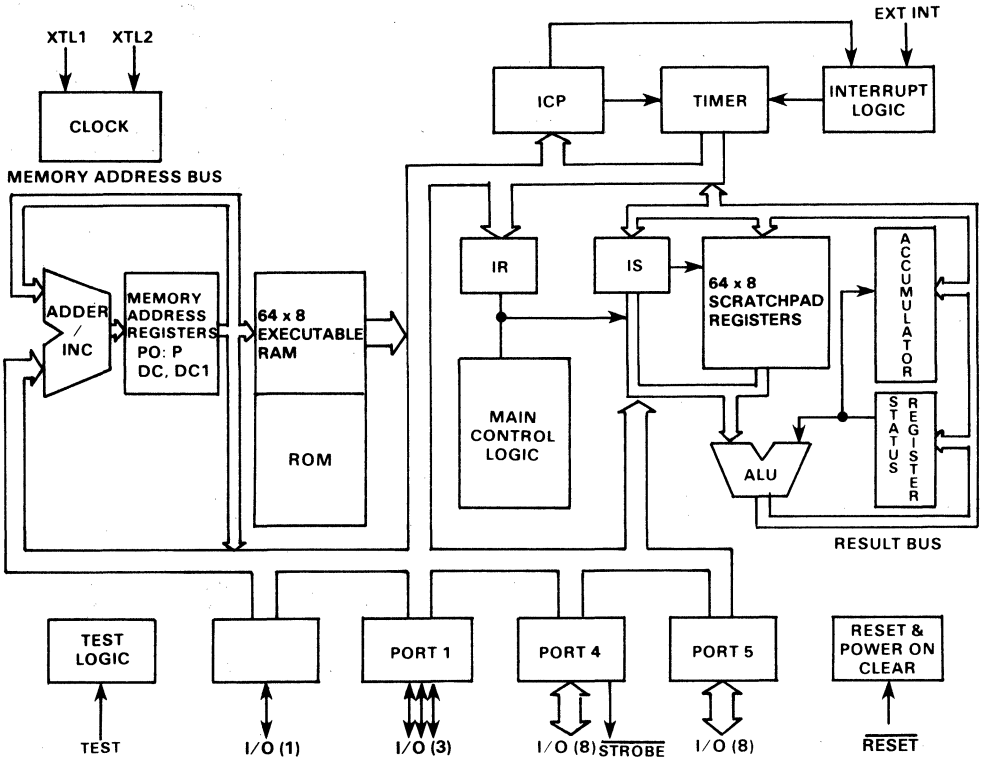
MK2870 PIN CONNECTIONS
Figure 2



VIII

MK2870 BLOCK DIAGRAM

Figure 3



the external interrupt input. The user has the option of specifying one of four clock sources for the MK2870: Crystal, LC, RC, or external clock. In addition, the user can specify either a ±10% power supply tolerance or a ±5% power supply tolerance.

PIN NAME	DESCRIPTION	TYPE
$\overline{P0\text{-}7}$	I/O Port 0 Bit 7	Bidirectional
$\overline{P1\text{-}1}$ -- $\overline{P1\text{-}3}$	I/O Port 1 Bits 1-3	Bidirectional
$\overline{P4\text{-}0}$ -- $\overline{P4\text{-}7}$	I/O Port 4	Bidirectional
$\overline{P5\text{-}0}$ -- $\overline{P5\text{-}7}$	I/O Port 5	Bidirectional
$\overline{STROBE}$	Ready Strobe	Output
EXT INT	External Interrupt	Input
$\overline{RESET}$	External Reset	Input
TEST	Test Line	Input
XTL 1, XTL 2	Time Base	Input
V_{CC}, GND	Power Supply Lines	Input

FUNCTIONAL PIN DESCRIPTION

$\overline{P0\text{-}7}$, $\overline{P1\text{-}1}$--$\overline{P1\text{-}3}$, $\overline{P4\text{-}0}$--$\overline{P4\text{-}7}$, and $\overline{P5\text{-}0}$--$\overline{P5\text{-}7}$ are 20 lines which can be individually used as either TTL compatible inputs or as latched outputs.

$\overline{STROBE}$ is a ready strobe associated with I/O Port 4. This pin, which is normally high, provides a single low pulse after valid data is present on the $\overline{P4\text{-}0}$--$\overline{P4\text{-}7}$ pins during an output instruction.

$\overline{RESET}$ may be used to externally reset the MK2870. When pulled low the MK2870 will reset. When then allowed to go high the MK2870 will begin program execution at program location H '000'.

EXT INT is the external interrupt input. Its active state is software programmable. This input is also used in conjunction with the timer for pulse width measurement and event counting.

XTL 1 and XTL 2 are the time base inputs to which a crystal, LC network, RC network, or an external single-phase clock may be connected. The time base network must be specified when ordering a mask ROM MK2870.

TEST is an input, used only in testing the MK2870. For normal circuit functionality this pin may be left unconnected, but it is recommended that TEST be grounded.

V_{CC} is the power supply input (single +5 V).

MK2870 ARCHITECTURE

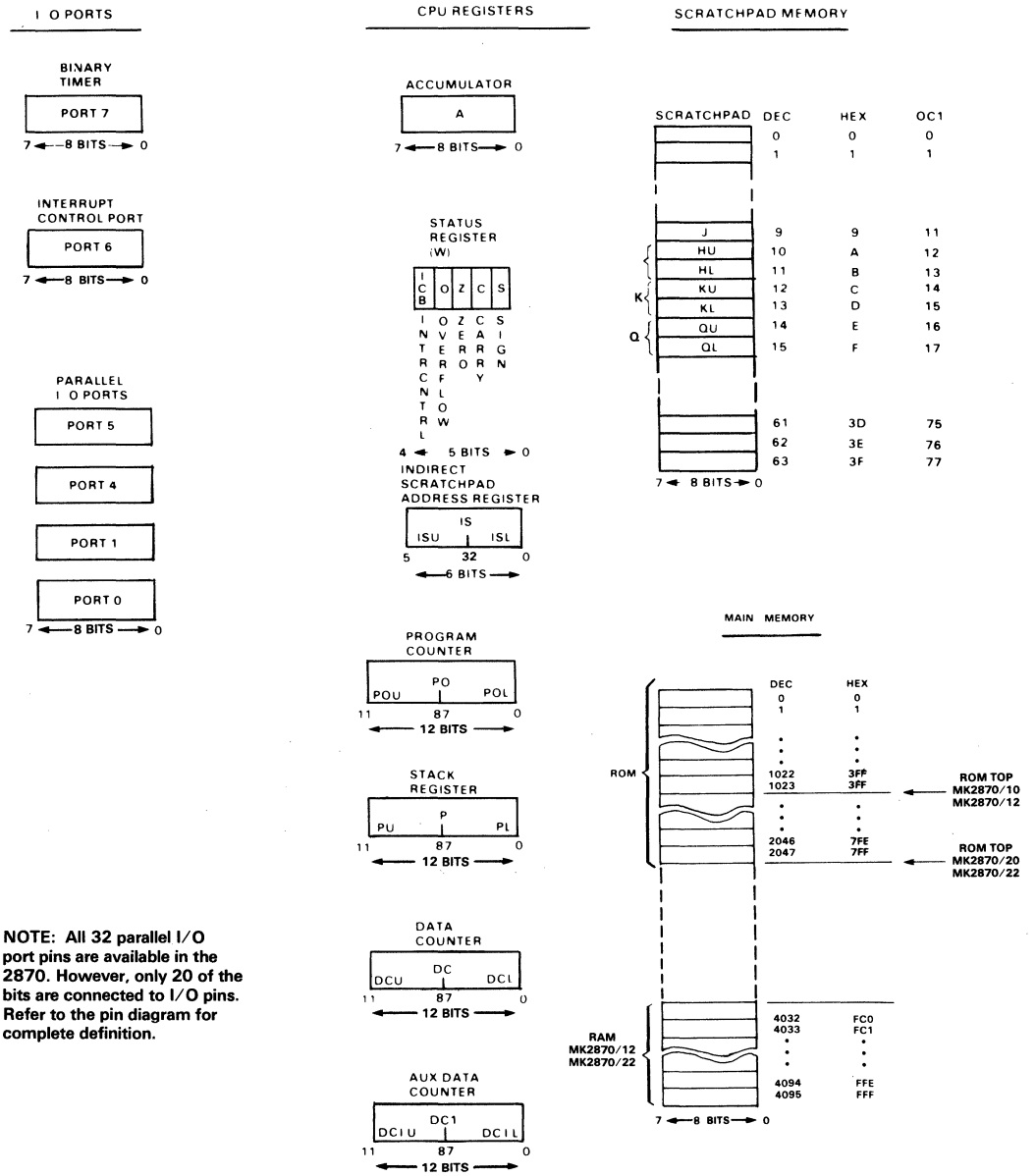
The basic functional elements of the MK2870 are shown in Figure 3. A programming model is shown in Figure 4. The architecture is common to all members of the 2870 family. All 2870 devices are instruction set compatible and differ only in amount and type of ROM and RAM. The unique features of the MK2870 are discussed in the following sections. The user is referred to the 3870 Family Technical Manual for a thorough discussion of the architecture, instruction set, and other features which are common to all 2870 family devices.

MK2870 MAIN MEMORY

There are four address registers used to access main memory. These are the Program Counter (PO), the Stack Register (P), the Data Counter (DC), and the Auxiliary Data Counter (DC1). The Program Counter is used to address instructions or immediate operands. The Stack Register is

MK2870 PROGRAMMABLE REGISTERS, PORTS, AND MEMORY MAP

Figure 4

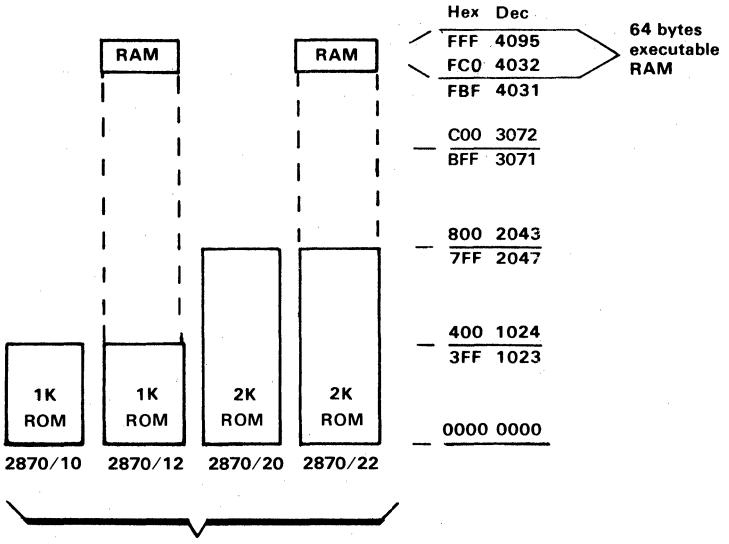


NOTE: All 32 parallel I/O port pins are available in the 2870. However, only 20 of the bits are connected to I/O pins. Refer to the pin diagram for complete definition.

VIII

MK2870 MAIN MEMORY SIZES AND TYPES BY SLASH NUMBERS

Figure 5



All devices contain 64 bytes of scratchpad RAM.

NOTE:

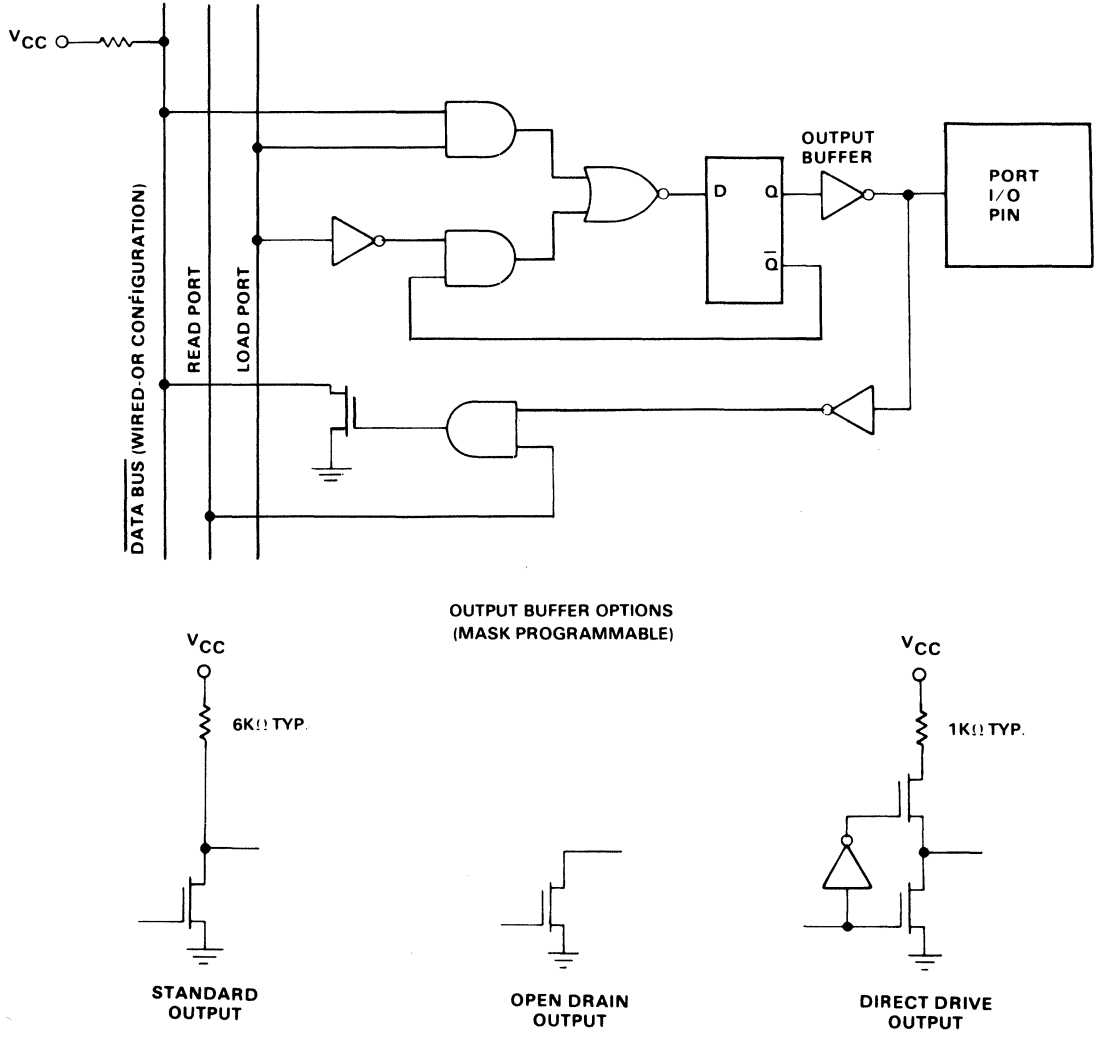
Data derived from addressing any locations other than those within a part's specified ROM space or RAM space (if any) is not tested nor is it guaranteed. Users should refrain from entering this area of the memory map.

Device	Scratchpad RAM Size (Decimal)	Address Register Size (P0, P, DC, DC1)	ROM Size (Decimal)	Executable RAM Size (Decimal)
MK2870/10	64 bytes	12 bits	1024 bytes	0 bytes
MK2870/12	64 bytes	12 bits	1024 bytes	64 bytes
MK2870/20	64 bytes	12 bits	2048 bytes	0 bytes
MK2870/22	64 bytes	12 bits	2048 bytes	64 bytes

NOTE: The Address Register Size for the 2870/20 is 11 bits. It will be changed to 12 bits at a later date.

I/O PIN CONCEPTUAL DIAGRAM WITH OUTPUT BUFFER OPTIONS

Figure 6



Ports 0 and 1 are Standard Output type only.

Ports 4 and 5 may both be any of the three output options (mask programmable bit by bit)

The $\overline{\text{STROBE}}$ output is always configured similar to a Direct Drive Output except that it is capable of driving 3 TTL loads.

$\overline{\text{RESET}}$ and EXT INT may have standard 6K Ω (typical) pull-up or may have no pull-up (mask programmable).

When Direct Drive option is selected, it should be used as an Output only (not as an input).

used to save the contents of the Program Counter during an interrupt or subroutine call. Thus, the Stack Register contains the return address at which processing is to resume upon completion of the subroutine or interrupt routine. The Data Counter is used to address data tables. This register is auto-incrementing. Of the two data counters, only Data Counter (DC), can access the ROM. However, the SDC instruction allows the Data Counter and Auxiliary Data Counter to be exchanged.

The graph in Figure 5 shows the amounts of ROM and executable RAM for every available slash number in the MK2870 pin configuration.

EXECUTABLE RAM

The upper bytes of the address space in some of the MK2870 devices is RAM memory. As with the ROM memory, the RAM may be addressed by the PO and the DC address registers. The executable RAM may be addressed by all MK2870 instructions which address Main Memory. Additionally, the MK2870 may execute an instruction sequence which resides in the executable RAM. Note this cannot be done with the scratchpad RAM memory, which is the reason the term "executable RAM" is given to this additional memory.

I/O PORTS

The MK2870 provides four, 8 bit bidirectional Input/Output ports. These are ports 0, 1, 4, 5. However, only 20 of the bits are connected to I/O pins. The remaining bits are storage elements. In addition, the Interrupt Control Port is addressed as Port 6 and the binary timer is addressed as Port 7. The programming of Ports 6 and 7 and the bidirectional I/O pin are covered in the 3870 Family Technical Manual. The schematic of an I/O pin and available output drive options are shown in Figure 6.

An output ready strobe is associated with Port 4. This flag may be used to signal a peripheral device that the MK2870 has just completed an output of new data to Port 4. The strobe provides a single low pulse shortly after the output operation is completely finished, so either edge may be used to signal the peripheral. $\overline{\text{STROBE}}$ may also be used as an input strobe to Port 4 after completing the input operation.

To use a port pin as an input, the large transistor which pulls the pin to V_{SS} must be turned off. This is accomplished by writing a '0' to that bit of the port. This applies to Ports 0, 1, 4, and 5 only.

2870 TIME BASE OPTIONS

The 2870 contains an on-chip oscillator circuit which provides an internal clock. The frequency of the oscillator circuit is set from the external time base network. The time base for the 2870 may originate from one of four sources:

1) Crystal
2) LC Network
3) RC Network
4) External Clock

The type of network which is to be used with the mask ROM MK2870 must be specified at the time when mask ROM devices are ordered.

The specifications for the four configurations are given in the following text. There is an internal capacitor between XTL 1 and GND and an internal capacitor between XTL 2 and GND. Thus, external capacitors are not necessarily required. In all clock modes the external time base frequency is divided by two to form the internal PHI clock.

CRYSTAL SELECTION

The use of a crystal as the time base is highly recommended as the frequency stability and reproducability from system to system is unsurpassed. The 2870 has an internal divide by two to allow the use of inexpensive and widely available TV Color Burst Crystals (3.58 MHz). Figure 8 lists the required crystal parameters for use with the 2870. The Crystal Mode time base configuration is shown in Figure 7.

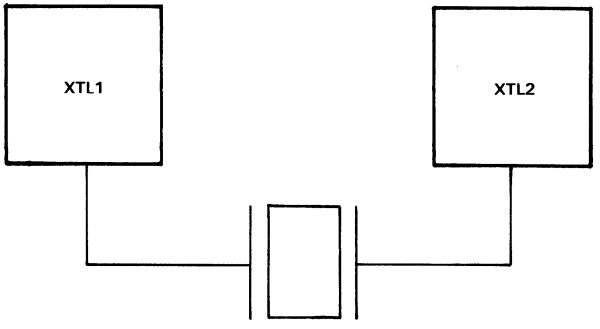
Through careful buffering of the XTL 1 pin it may be possible to amplify this waveform and distribute it to other devices. However, Mostek recommends that a separate active device (such as a 7400 series TTL gate) be used to oscillate the crystal and the waveform from that oscillator be buffered and supplied to all devices, including the 2870, in the event that a single crystal is to provide the time base for more than just a single 2870.

While a ceramic resonator may work with the 2870 crystal oscillator, it was not designed specifically to support the use of this component. Thus, Mostek does not support the use of a ceramic resonator either through proper testing, parametric specification, or applications support.

LC NETWORK

The LC time base configuration can be used to provide a less expensive time base for the 2870 than can be provided with a crystal. However, the LC configuration is much less accurate than is the crystal configuration. The LC time base configuration is shown in Figure 9. Also shown in the figure are the specified parameters for the LC components, along with the formula for calculating the resulting time base frequency. The minimum value of the inductor which is required for proper operation of the LC time base network is 0.1 millihenries. The inductor must be a Q factor which is no less than 40. The value of C is derived from C external, the internal capacitance of the 2870 C_{XTL}, and the stray capacitances, C_{S1} and C_{S2}. C_{XTL} is the capacitance looking into the internal two port network at XTL 1 and XTL 2. C_{XTL} is listed under the "Capacitance" section of the Electrical Specifications. C_{S1} and C_{S2} are stray capacitances from XTL 1 to ground and from XTL 2 to ground, respectively. C

CRYSTAL MODE CONNECTION
Figure 7



AT - CUT

NOTE: Lead lengths from the crystal to the 2870 pins should be kept reasonably short to reduce stray capacitance load.

CRYSTAL PARAMETERS
Figure 8

a) Parallel resonance, fundamental mode AT-Cut
b) Shunt capacitance (C_0) = 7 pf max.
c) Series resistance (R_s) = See table
d) Holder = See table below.

Frequency	Series Resistance	Holder
f = 2-2.7 MHz	Rs = 300 ohms max	HC-6 HC-33
f = 2.8-4 MHz	Rs = 150 ohms max	HC-6 HC-18* HC-25* HC-33

*This holder may not be available at frequencies near the lower end of this range.

external should also include the stray shunt capacitance across the inductor. This is typically in the 3 to 5 pf range and significant error can result if it is not included in the frequency calculation.

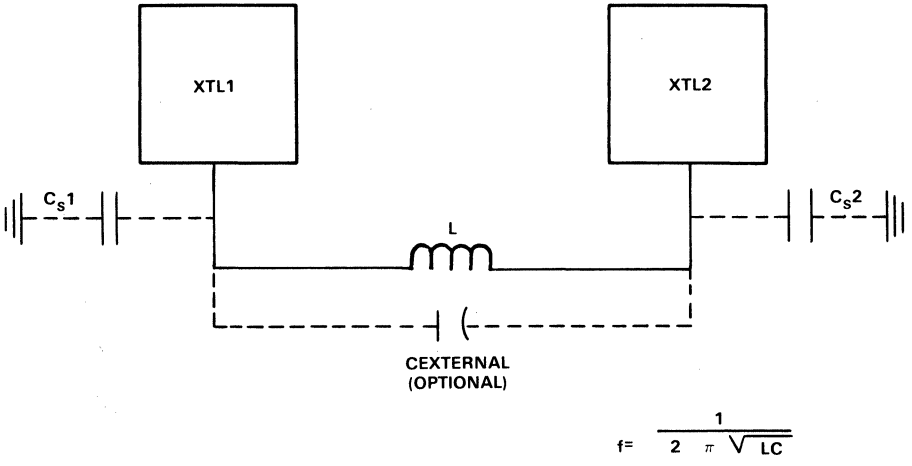
Variation in time base frequency with the LC network can arise from one of four sources: 1) Variation in the value of the inductor. 2) Variation in the value of the external capacitor. 3) Variation in the value of the internal capacitance of the 2870 at XTL 1 and XTL 2 and 4) Variation in the amount of stray capacitance which exists in the circuit. Therefore, the actual frequency which is generated by the LC circuit is within a range of possible frequencies, where the range of frequencies is determined by the worst case variation in circuit parameters. The designer must select component values such that the range of possible frequencies with the LC mode does not go outside of the specified operating frequency range for the 2870.

RC CLOCK CONFIGURATION

The time base for the 2870 may be provided from an RC network tied to the XTL 2 pin, when XTL 1 is grounded. A schematic picturing the RC clock configuration is shown in Figure 10. The RC time base configuration is intended to provide an inexpensive time base source for applications in which timing is not critical. Some users have elected to tune each unit using a variable resistor or external capacitor thus reducing the variation in frequency. However, for increased time base accuracy Mostek recommends the use of the Crystal or LC time base configuration. Figure 11 illustrates a curve which gives the resulting operating frequency for a particular RC value. The x-axis represents the product of the value of the resistor times the value of the capacitor. Note that three curves are actually shown. The curve in the middle represents the nominal frequency obtained for a given value of RC. A maximum curve and a minimum curve

LC MODE CONNECTION

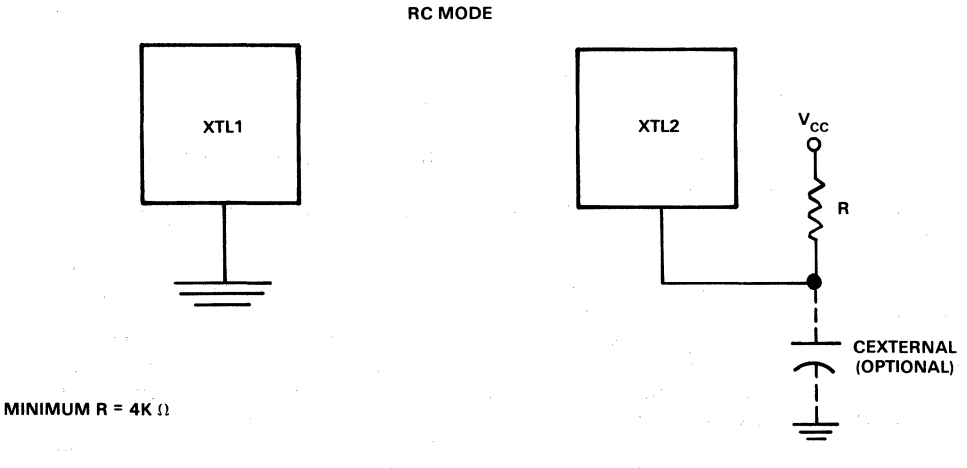
Figure 8



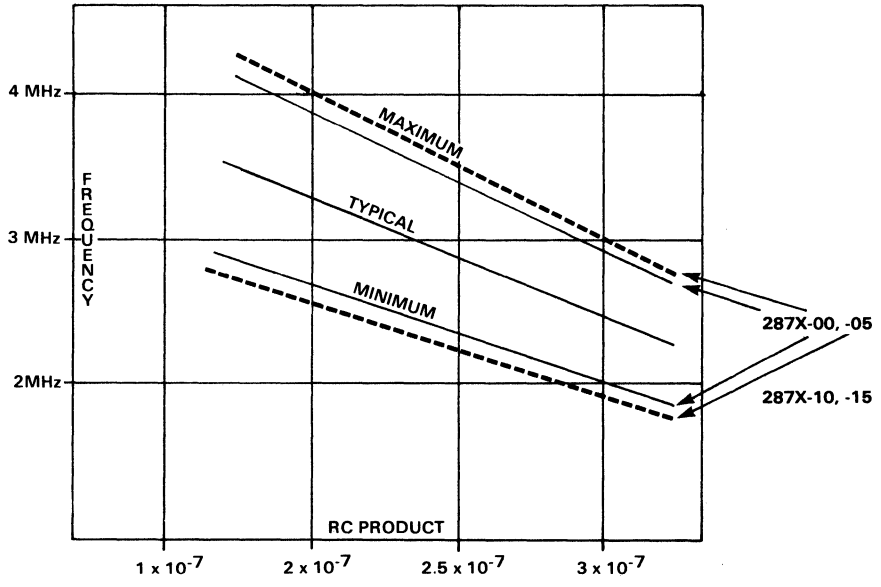
NOTE: The LC options uses the same mask option as the crystal option.

RC MODE CONNECTION

Figure 10



FREQUENCY VS. RC
Figure 11



for different types of 2870 devices are also shown in the diagram.

The designer must select the RC product such that a frequency of less than 2 MHz is not possible taking into account the maximum possible RC product and using the minimum curve shown in Figure 11. Also, the RC product must not allow a frequency of more than 4 MHz taking into account the minimum possible R and C and using the Maximum curve shown below. Temperature induced variations in the external components should be considered in calculating the RC Product.

Frequency variation from unit to unit due to switching speed and level at constant temperature and V_{CC} = + or -5 percent.

Frequency variation due to V_{CC} with all other parameters constant with respect to +5 V = +7 percent to -4 percent on all devices.

Frequency variation due to temperature with respect to 25 C (all other parameters constant) is as follows:

PART #	VARIATION
287X-00, -05	+6 percent to - 9 percent
287X-10, -15	+9 percent to -12 percent

Variations in frequency due to variations in RC components may be calculated as follows:

Maximum RC = (R max) (C external max + C_{XTL} max)

Minimum RC = (R min) (C external min + C_{XTL} min)

Typical RC = (R typ) (C external typ + $\frac{\{C_{XTL} \text{ max} + C_{XTL} \text{ min}\})}{2}$

Positive Freq. Variation = $\frac{\text{RC typical - RC minimum}}{\text{RC typical}}$

Netative Freq. Variation = $\frac{\text{RC maximum - RC typical}}{\text{RC typical}}$
due to RC Components

Total frequency variation due to all factors:

287X-00, -05	287X-10, -15
+18 percent plus positive frequency variation due to RC components	= +21 percent plus positive frequency variation due to RC components
= -18 percent minus negative frequency variation due to RC components	= -21 percent minus negative frequency variation due to RC components

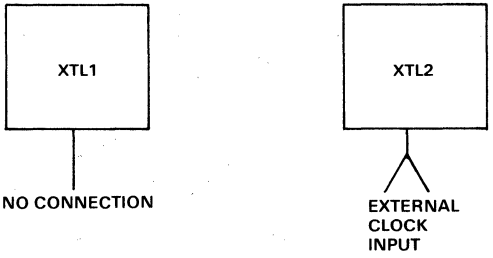
Total frequency variation due to V_{CC} and temperature of a unit tuned to frequency at +5 V V_{CC}, 25 C

287X-00, -05	287X-10, -15
= + 13 percent	= +16 percent

VIII

EXTERNAL MODE CONNECTION

Figure 12



EXTERNAL CLOCK CONFIGURATION

The connection for the external clock time base configuration is shown in Figure 12. Refer to the DC Characteristics section for proper input levels and current requirements.

Refer to the Capacitance section of the appropriate 2870 Family device data sheet for input capacitance.

OPERATING VOLTAGES AND TEMPERATURES

Dash Number Suffix	Operating Voltage V_{CC}	Operating Temperature T_A
— 00	+5 V ±10%	0°C - 70°C
— 05	+5 V ± 5%	0°C - 70°C
— 10	+5 V ± 10%	-40°C - +85°C
— 15	+5 V ± 5%	-40°C - +85°C

See Ordering Information for explanation of part numbers.

ABSOLUTE MAXIMUM RATINGS*

	-00, -05	-10, -15
Temperature Under Bias	-20°C to +85°C	-50°C to +100°C
Storage Temperature	-65°C to +150°C	-65°C to +150°C
Voltage on any Pin With Respect to Ground (Except open drain pins and TEST)	-1.0 V to +7 V	-1.0 V to + 7 C
Voltage on TEST with Respect to Ground	-1.0 V to +9 V	-1.0 V to +9 V
Voltage on Open Drain Pins With Respect to Ground	-1.0 V to +13.5 V	-1.0 V to +13.5 V
Power Dissipation	1.5 W	1.5 W
Power Dissipation by any one I/O pin	60 mW	60 mW
Power Dissipation by all I/O pins	600 mW	600 mW

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

AC CHARACTERISTICS

T_A, V_{CC} within specified operating range.
I/O power dissipation ≤ 100 mW (Note 2)

SIGNAL	SYM	PARAMETER	-00, -05 MIN	-00, -05 MAX	-10, -15 MIN	-10, -15 MAX	UNIT	NOTES
XTL 1 XTL 2	t_o $t_{ex(H)}$ $t_{ex(L)}$	Time Base Period, all clock modes External clock pulse width high External clock pulse width low	250 90 100	500 400 400	250 100 110	500 390 390	ns ns ns	4 MHz - 2 MHz
Φ	t_Φ	Internal Φ clock	$2t_o$		$2t_o$			
WRITE	t_w	Internal WRITE Clock period	4tΦ 6tΦ		4tΦ 6tΦ			Short Cycle Long Cycle
I/O	$t_{dI/O}$	Output delay from internal WRITE clock	0	1000	0	1200	ns	50 pF plus one TTL load
	$t_{sI/O}$	Input setup time to internal WRITE clock	1000		1200		ns	
$\overline{STROBE}$	$t_{I/O-s}$	Output valid to $\overline{STROBE}$ delay	3tΦ -1000	3tΦ +250	3tΦ -1200	3tΦ +300	ns	I/O load = 50 pF + 1 TTL load
	t_{sL}	$\overline{STROBE}$ low time	8tΦ -250	12tΦ +250	8tΦ -300	12tΦ +300	ns	$\overline{STROBE}$ load = 50 pF + 3TTL loads
$\overline{RESET}$	t_{RH}	$\overline{RESET}$ hold time, low	6tΦ +750		6tΦ +1000		ns	
	t_{RPOC}	$\overline{RESET}$ hold time, low for power clear	power supply rise time + 0.1		power supply rise time + .15		ms	
EXT INT	t_{EH}	EXT INT hold time in active and inactive state	6tΦ +750		6tΦ +1000		ns	To trigger interrupt
			2tΦ		2tΦ		ns	To trigger timer

VIII

DC CHARACTERISTICS

T_A, V_{CC} within specified operating range
I/O power dissipation ≤ 100 mW (Note 2)

SYMBOL	PARAMETER	-00, -05		-10, -15		UNIT	DEVICE
		MIN	MAX	MIN	MAX		
I_{CC}	Average Power Supply Current		85		110	mA	MK2870/10 Outputs Open
			94		125	mA	MK2870/12 Outputs Open
			85		110	mA	MK2870/20 Outputs Open
			94		125	mA	MK2870/22 Outputs Open
P_D	Power Dissipation		400		525	mW	MK2870/10 Outputs Open
			440		575	mW	MK2870/12 Outputs Open
			400		525	mW	MK2870/20 Outputs Open
			440		575	mW	MK2870/22 Outputs Open
V_{IHEX}	External Clock input high level	2.4	5.8	2.4	5.8	V	
V_{ILEX}	External Clock input low level	-.3	.6	-.3	.6	V	
I_{IHEX}	External Clock input high current		100		130	μA	$V_{IHEX}=V_{CC}$
I_{ILEX}	External Clock input low current		-100		-130	μA	$V_{ILEX}=V_{SS}$
$V_{IHI/O}$	Input high level, I/O pins	2.0	5.8	2.0	5.8	V	Standard pull-up
		2.0	13.2	2.0	13.2	V	Open drain (1)
V_{IHR}	Input high level, $\overline{\text{RESET}}$	2.0	5.8	2.2	5.8	V	Standard pull-up
		2.0	13.2	2.2	13.2	V	No Pull-up
V_{IHEI}	Input high level, EXT INT	2.0	5.8	2.2	5.8	V	Standard pull-up
		2.0	13.2	2.2	13.2	V	No Pull-up
V_{IL}	Input low level	-.3	.8	-.3	.7	V	(1)
I_{IL}	Input low current, all pins with standard pull-up resistor		-1.6		-1.9	mA	V_{IN} = 0.4 V
I_L	Input leakage current, open drain pins, and inputs with no pull-up resistor		+10 -5		+18 -8	μA μA	V_{OH} = 13.2 V V_{IN} = 0.0 V
I_{OH}	Output high current pins with standard pull-up resistor	-100		-89		μA	V_{OH} = 2.4 V
		-30		-25		μA	V_{OH} = 3.9 V

DC CHARACTERISTICS (cont.)

T_A, V_{CC} within specified operating range, I/O power dissipation ≥ 100 mW (Note 2)

SYM	PARAMETER	-00, -05 MIN	-00, -05 MAX	-10, -15 MIN	-10, -15 MAX	UNIT	CONDITIONS
I_{OHDD}	Output high current, direct drive pins	-100 -1.5	 -8.5	-80 -1.3	 -11	μA mA mA	V_{OH} = 2.4 V V_{OH} = 1.5 V V_{OH} = 0.7 V
I_{OHS}	$\overline{\text{STROBE}}$ Output High current	-300		-270		μA	V_{OH} = 2.4 V
I_{OL}	Output low current	1.8		1.65		mA	V_{OL} = 0.4 V
I_{OLS}	$\overline{\text{STROBE}}$ Output Low current	5.0		4.5		mA	V_{OL} = 0.4 V

TIMER AC CHARACTERISTICS

Definitions:
Error = Indicated time value - actual time value

tpsc = tΦ x Prescale Value

Interval Timer Mode:

Single interval error, free running (Note 3) ..... ±6tΦ
Cumulative interval error, free running (Note 3) 0
Error between two Timer reads (Note 2) ..... ±(tpsc + tΦ)
Start Timer to stop Timer error (Notes 1, 4) ..... +tΦ to - (tpsc + tΦ)
Start Timer to read Timer error (Notes 1, 2) ..... -5t Φ to - (tpsc + 7tΦ)
Start Timer to interrupt request error (Notes 1, 3) ..... -2tΦ to -8 tΦ
Load Timer to stop Timer error (Note 1) ..... + tΦ to - (tpsc + 2tΦ)
Load Timer to read Timer error (Notes 1, 2) ..... -5tΦ ± to - (tpsc + 8tΦ)
Load Timer to interrupt request error (Notes 1, 3) ..... -2tΦ to -9tΦ

Pulse Width Measurement Mode:

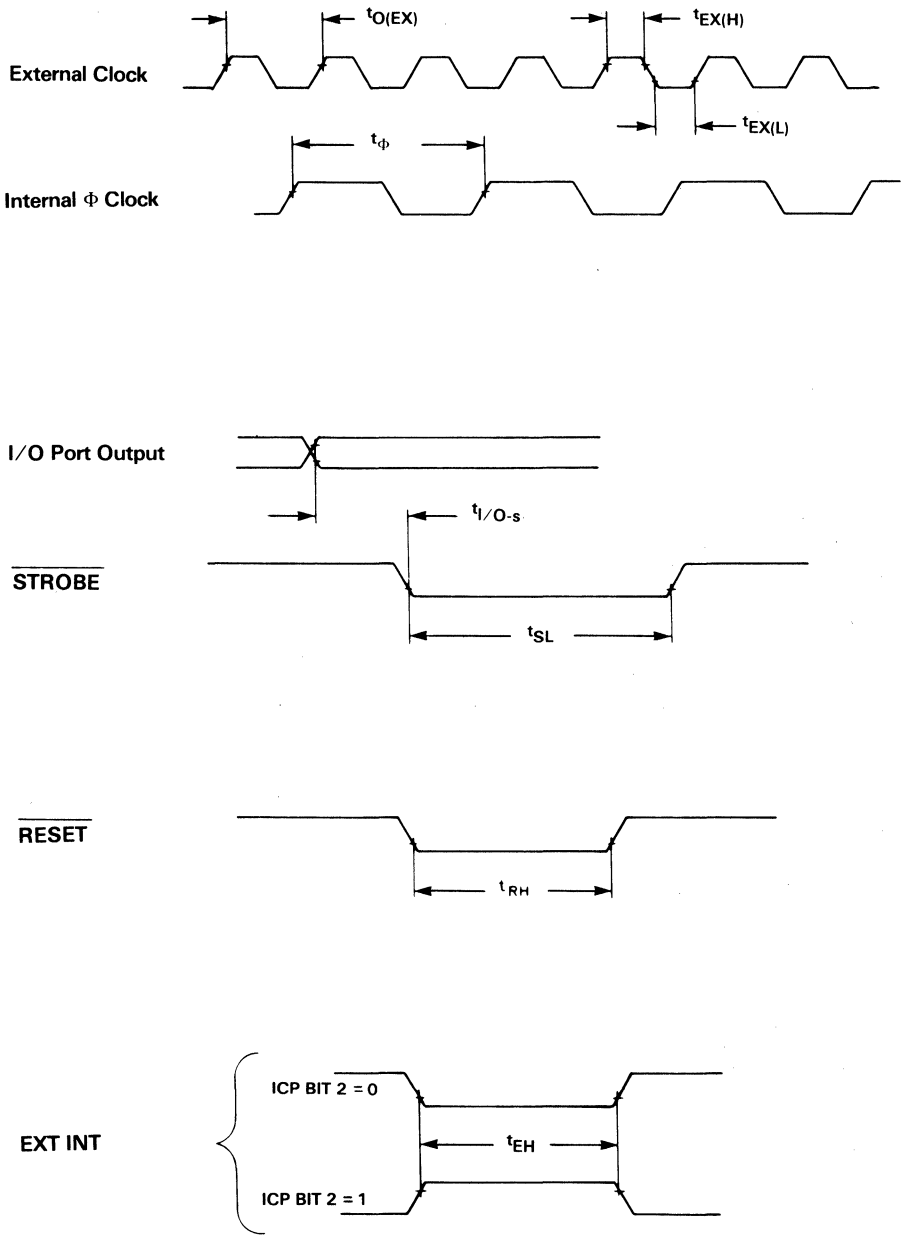
Measurement accuracy (Note 4) ..... + tΦ to - (tpsc + 2tΦ)
Minimum pulse width of EXT INT pin 2tΦ

Event Counter Mode:

Minimum active time of EXT INT pin 2tΦ
Minimum inactive time of EXT INT pin 2tΦ

NOTES:
1. All times which entail loading, starting, or stopping the Timer are referenced from the end of the last machine cycle of the OUT or OUTS instruction.
2. All times which entail reading the Timer are referenced from the end of the last machine cycle of the IN or INS instruction.
3. All times which entail the generation of an interrupt request are referenced from the start of the machine cycle in which the appropriate interrupt request latch is set. Additional time may elapse if the interrupt request occurs during a privileged or multicycle instruction.
4. Error may be cumulative if operation is repetitively performed.

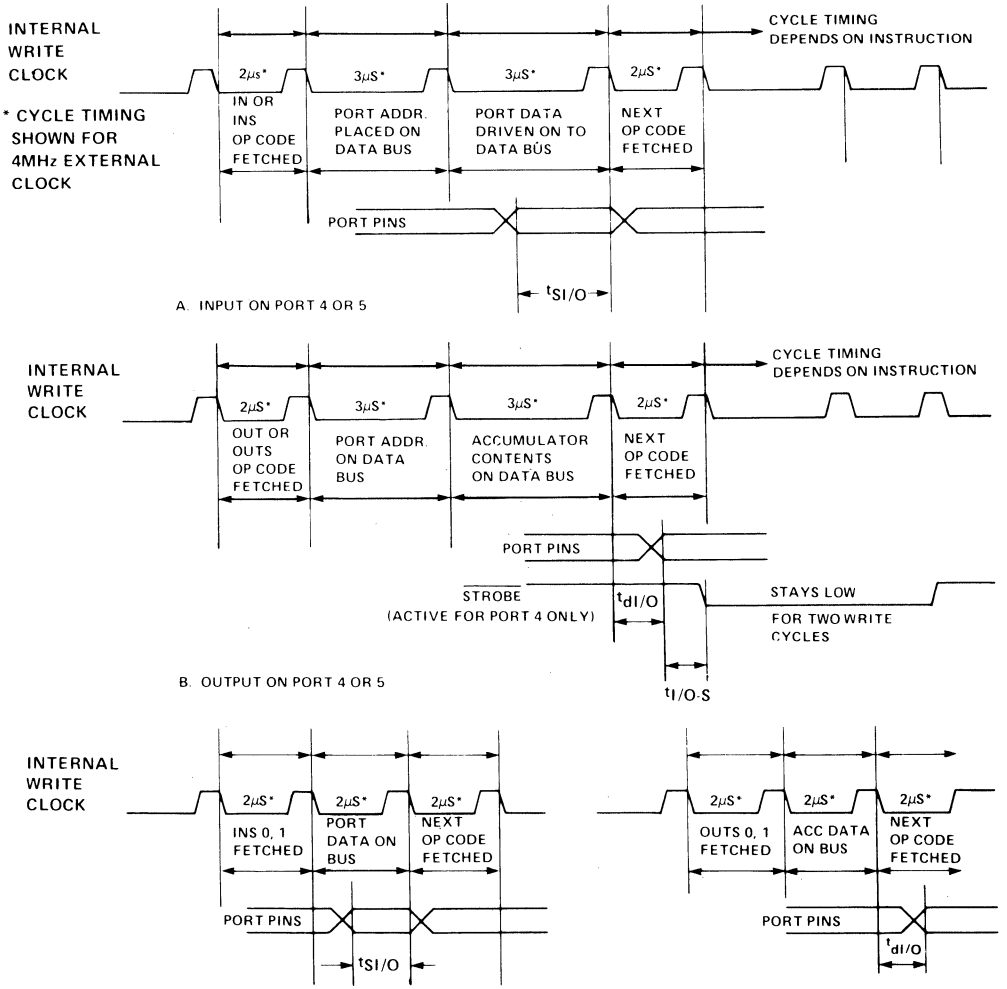
AC TIMING DIAGRAM
Figure 13



Note: All AC measurements are referenced to V_{IL} max., V_{IH} min., V_{OL} (.8v), or V_{OH} (2.0v).

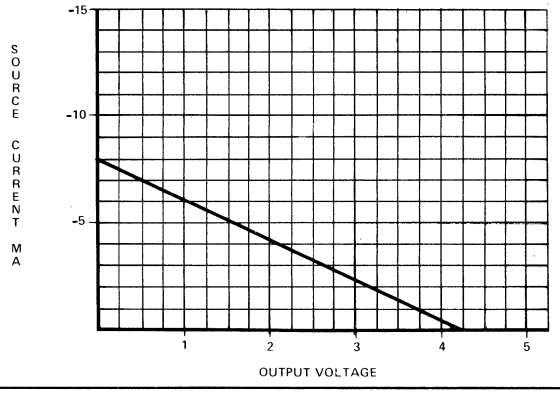
INPUT/OUTPUT AC TIMING

Figure 14

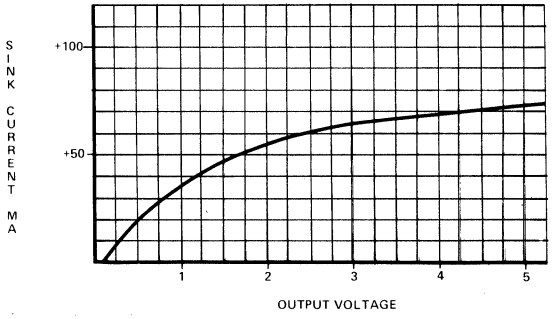


VIII

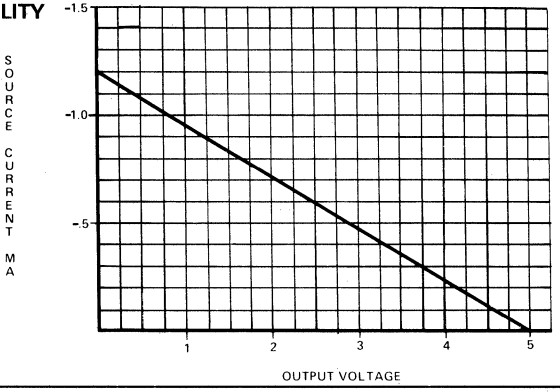
STROBE SOURCE CAPABILITY
(TYPICAL AT V_{CC} = 5 V, T_A = 25°C)
Figure 15



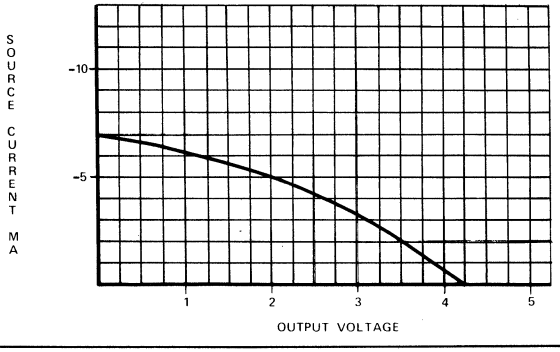
STROBE SINK CAPABILITY
(TYPICAL AT V_{CC} = 5 V, T_A = 25°C)
Figure 16



STANDARD I/O PORT SOURCE CAPABILITY
(TYPICAL AT V_{CC} = 5 V, T_A = 25°C)
Figure 17



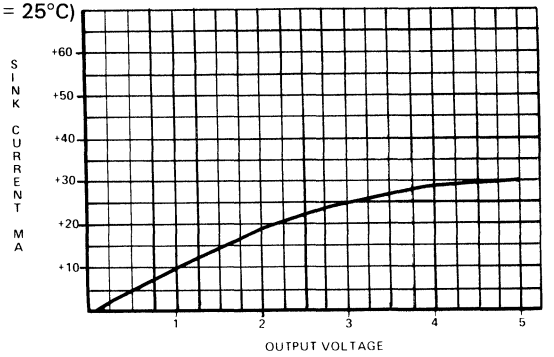
DIRECT DRIVE I/O PORT SOURCE CAPABILITY
(TYPICAL AT V_{CC} = 5 V, T_A = 25°C)
Figure 18



I/O PORT SINK CAPABILITY

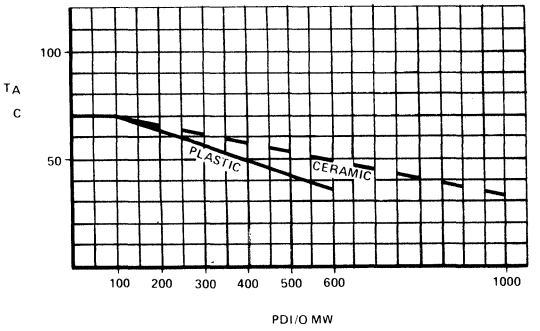
(TYPICAL AT V_{CC} = 5 V, T_{A}, = 25°C)

Figure 19



MAXIMUM OPERATING TEMPERATURE VS. I/O POWER DISSIPATION

Figure 20



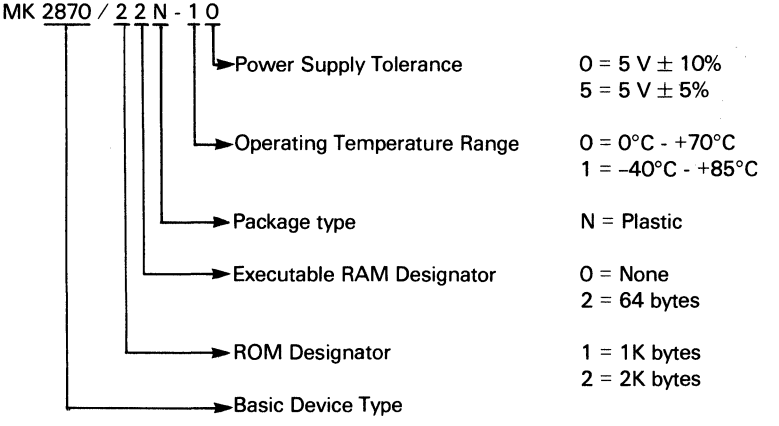
VIII

ORDERING INFORMATION

There are two types of part numbers for the 2870 family of devices. The generic part number describes the basic device type, the amount of ROM and Executable RAM, the desired package type, temperature range, and power supply tolerance. For each customer specific code, additional information defining I/O options and oscillator options will be combined with the information described in the generic part number to define a customer/code specific device order number.

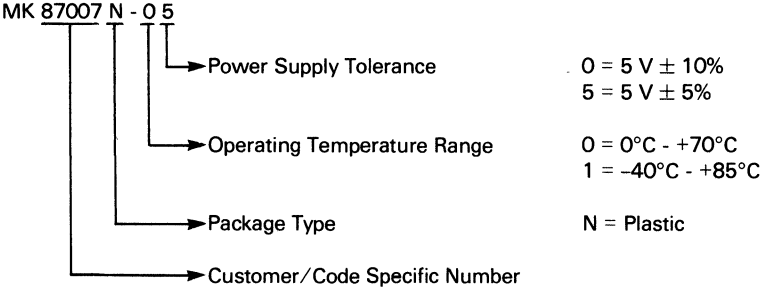
GENERIC PART NUMBER

An example of the generic part number is shown below.



DEVICE ORDER NUMBER

An example of the device order number is shown below.



The Customer/Code specific number defines the ROM bit pattern, I/O configuration, oscillator type, and generic part type to be used to satisfy the requirements of a particular customer purchase order. For further information on the ordering of mask ROM devices, the customer should refer to the 3870 Family Technical Manual.

PRELIMINARY

MOSTEK®

3870 SINGLE CHIP MICRO FAMILY

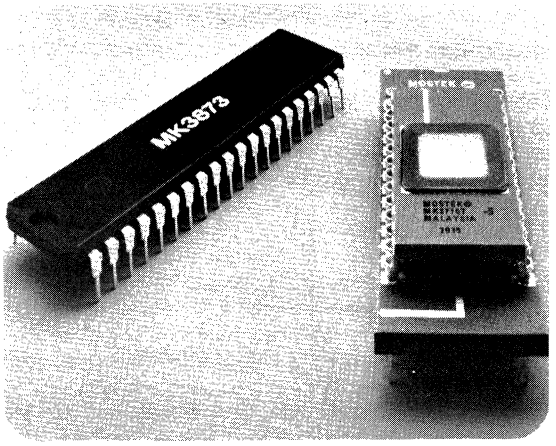
MK3873 and MK38P73

MK3873 FEATURES

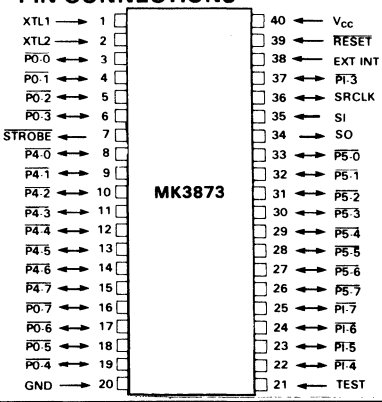
- ☐ Available with 1K or 2K byte mask programmable ROM
- ☐ Software compatible with 3870 instruction set
- ☐ 64 byte scratchpad RAM
- ☐ Available with 64 byte Executable RAM
- ☐ 29 bits (4 ports) TTL compatible parallel I/O
- ☐ Serial Input/Output port
  - External or Internal Serial Port Clock
  - Transmit and Receive registers double buffered
  - Internal Baud rate generator
  - Synchronous or Asynchronous serial I/O
  - Data rates to 9600 bits per second (ASYNC)
  - I/O pins dedicated as SERIAL IN, SERIAL OUT, and SERIAL CLOCK
  - Variable duty cycle waveform generation
- ☐ Vectored interrupts
- ☐ Programmable binary timer
  - Internal timer mode
  - Pulse width measurement mode
  - Event counter mode
- ☐ External Interrupt
- ☐ Crystal, LC, RC or external time base options available
- ☐ Low power (325 mW typ.)
- ☐ Single +5V power supply
- ☐ Pinout compatible with the 3870 Family members

MK38P73 FEATURES

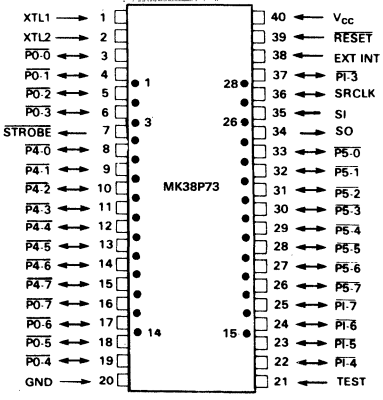
- ☐ EPROM version of MK3873
- ☐ Piggyback PROM (P-PROM)™ package
- ☐ Accepts 24 pin or 28 pin EPROM memories
- ☐ Identical pinout as MK3873
- ☐ In-Socket emulation of MK3873



MK3873 PIN CONNECTIONS



MK38P73 PIN CONNECTIONS



VIII

GENERAL DESCRIPTION

The MK3873 single chip microcomputer introduces a major addition to the 3870 microcomputer family, a serial input/output port. This serial port is capable of either synchronous or asynchronous serial data transfers. The heart of the serial port is a 16-bit Shift Register that is double-buffered on transmit and receive. The Shift Register clock source can be either the internal baud rate generator or an external clock. An end-of-word vectored interrupt is generated in either transmit or receive mode so that the CPU overhead is only at the word rate and not at the serial bit rate. This serial channel can be used to provide a low-cost data channel for communicating between 3873 microcomputers or between a 3873 and another host computer. The serial port is also very flexible so that it could be used for other purposes such as an interface to external serial logic or serial memory devices.

The MK3873 retains commonality with the 3870 family of single chip microcomputers. It has up to 2048 bytes of mask ROM for program storage, and 64 bytes of scratchpad random-access memory. Certain versions also include up to 64 bytes of Executable RAM. Also, the 3870's sophisticated programmable binary timer is included and provides for system flexibility by operating in 3 different modes. The MK3873 has a large number of parallel I/O lines available to the user. Twenty nine pins of the MK3873 are dedicated to parallel I/O. In addition, three pins are dedicated to the serial I/O port. These pins provide input, output, and clock for the serial port. The serial clock pin can be driven externally or programmed to provide a 50% duty cycle TTL compatible serial clock. No additional CPU instructions are necessary for use with the serial port. Thus, the MK3873 is instruction set compatible with the rest of the 3870 family.

The MK38P73 microcomputer is the PROM based version of the MK3873 single-chip microcomputer. The MK38P73 is called the Piggyback PROM (P-PROM)™ microcomputer because of a new packaging concept. This concept allows a 24 or 28 pin EPROM to be mounted directly on top of the microcomputer itself. The EPROM can then be removed and reprogrammed as required with a standard PROM programmer. The MK38P73 retains exactly the same pinout and architectural features as other members of the MK3873 Family. The MK38P73 is discussed in more detail in a later section of this document.

FUNCTIONAL PIN DESCRIPTION

$\overline{P0\text{-}0}$ - $\overline{P07}$, $\overline{P1\text{-}3}$ - $\overline{P1\text{-}7}$, $\overline{P4\text{-}0}$ - $\overline{P4\text{-}7}$, $\overline{P5\text{-}0}$ - $\overline{P5\text{-}7}$ are 29 bidirectional I/O lines which can either be used as TTL compatible inputs or latch outputs.

SI - SERIAL IN is a TTL compatible Schmitt Trigger input pin for either serial synchronous or asynchronous data.

SO - SERIAL OUT is an output line for either serial synchronous or asynchronous data.

SRCLK is the clock for the serial port operations. It can be configured by software to be an input or output depending upon whether an internal baud rate or external clock is desired. It has a Schmitt trigger input and can be used to drive up to 3 TTL loads.

$\overline{STROBE}$ is a ready strobe associated with I/O Port 4. This pin which is normally high provides a single low pulse after valid data is present on the $\overline{P4\text{-}0}$ - $\overline{P4\text{-}7}$ pins during an output instruction. $\overline{STROBE}$ can be used to drive up to 3 TTL loads.

$\overline{RESET}$ may be used to externally reset the MK3873. When pulled low the MK3873 will reset. When allowed to go high the MK3873 will begin program execution at program location H'000'.

PIN NAME	DESCRIPTION	TYPE
$\overline{P0\text{-}0}$, $\overline{P0\text{-}7}$	I/O Port 0	Bidirectional
$\overline{P1\text{-}3}$ - $\overline{P1\text{-}7}$	I/O Port 1	Bidirectional
$\overline{P4\text{-}0}$ - $\overline{P4\text{-}7}$	I/O Port 4	Bidirectional
$\overline{P5\text{-}0}$ - $\overline{P5\text{-}7}$	I/O Port 5	Bidirectional
$\overline{STROBE}$	Ready Strobe	Output
EXT INT	External Interrupt	Input
$\overline{RESET}$	External Reset	Input
SI	Serial Input	Input
SO	Serial Output	Output
SRCLK	Serial Clock	Bidirectional
TEST	Test Line	Input
XTL 1, XTL 2	Time Base	Input
V_{CC}, GND	Power Supply Lines	Input

EXT INT is the external interrupt input. Its active state is software programmable as described in the 3870 Family Technical Manual. This input is also used in conjunction with the timer for pulse width measurement and event counting.

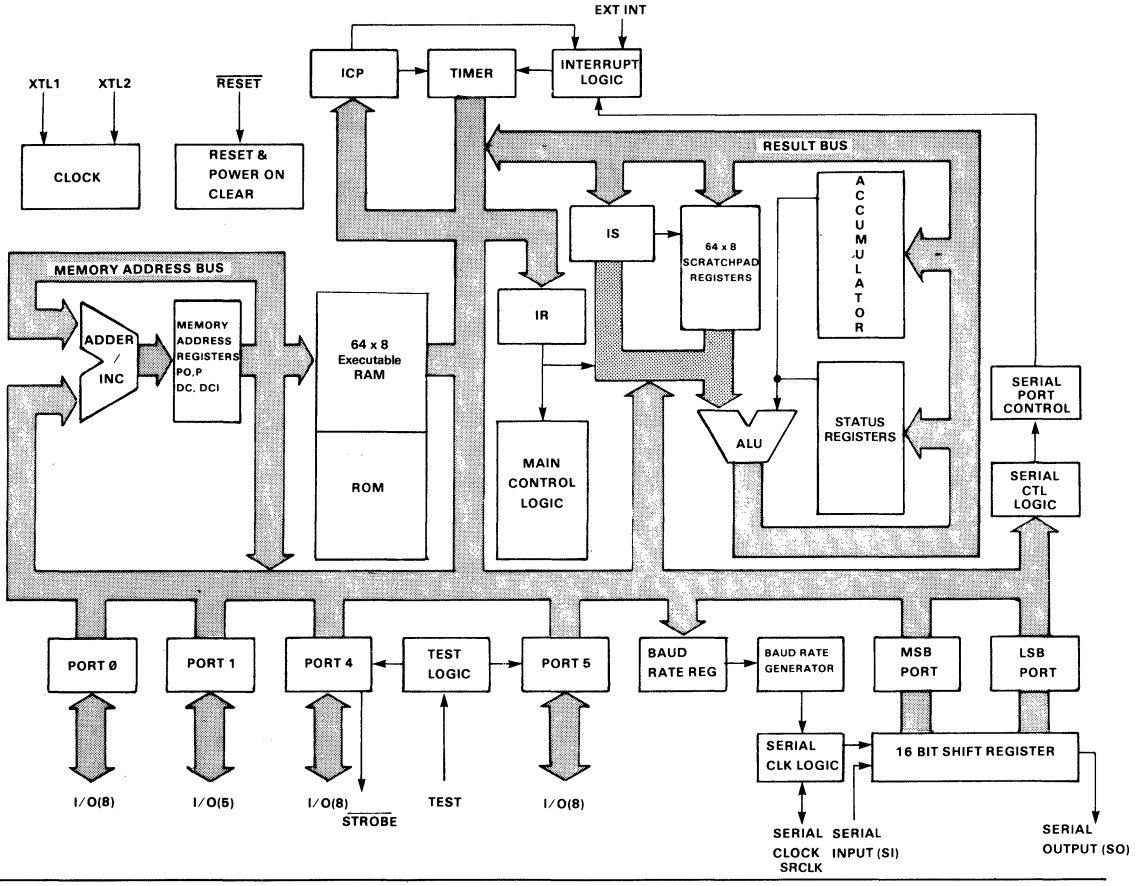
XTL 1 and XTL 2 are the time base inputs (2 MHz to 4 MHz) to which a crystal, LC network, RC network, or an external single-phase clock may be connected. The time base mode must be specified when submitting an order for a mask ROM MK3873. The MK38P73 will operate with any of the four configurations.

MK3873 ARCHITECTURE

The architecture of the MK3873 is identical to that of the rest of the devices in the 3870 family, with the exception of the serial port logic. The serial port logic is shown in the block diagram of the MK3873 (Figure 1). Addressing of the serial port logic is accomplished through I/O instructions. Operation and programming of the serial port is thoroughly discusssed below. A programming-model of the MK3873 is shown in Figure 2. For a more complete discussion of the 3870 family architecture, the user is referred to the 3870 Family Technical Manual.

MK3873 BLOCK DIAGRAM

Figure 1



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MAIN MEMORY

The main memory section on the MK3873 consists of a combination of ROM and executable RAM.

There are four registers associated with the main memory section. These are the Program Counter (PO), the Stack Register (P), the Data Counter (DC), and the Auxiliary Data Counter (DC1). The Program Counter is used to address instructions during program execution. P is used to save the contents of PO during an interrupt or subroutine call. Thus, P contains the return address at which processing is to resume upon completion of the subroutine or the interrupt routine. The Data Counter (DC) is used to address data tables. This register is auto-incrementing. Of the two data counters, only DC can access memory directly. However, the XDC instruction allows DC and DC1 to be exchanged.

The length of the PO, P, DC, and DC1 registers for all MK3873 devices is listed in the table shown in Figure 3. The graph and table in Figure 3 also shows the amounts of ROM and executable RAM for the different members of the MK3873 family.

EXECUTABLE RAM

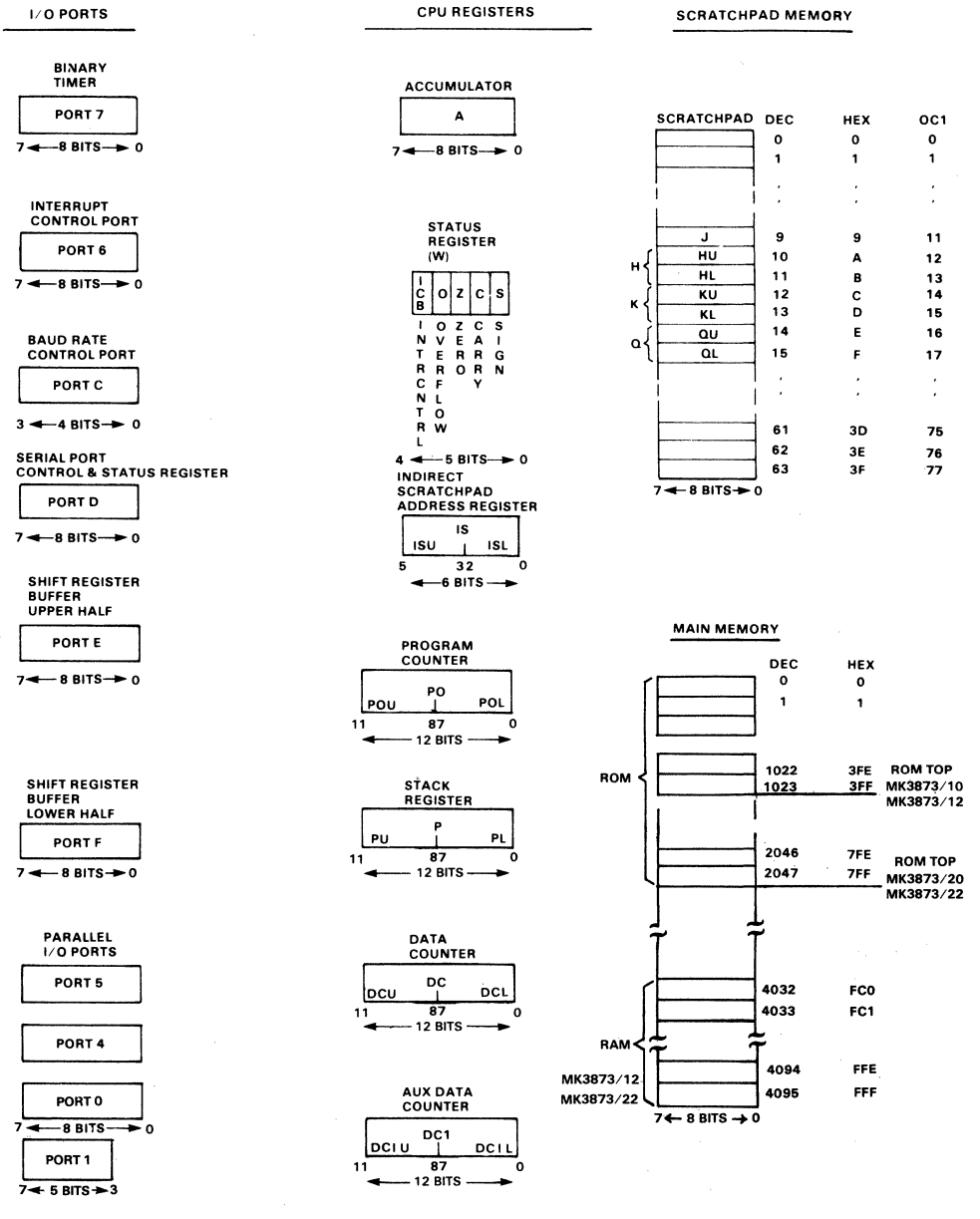
The upper bytes of the total address space in certain MK3873 devices is RAM memory. As with the ROM memory the RAM may be addressed by the PO and DC address registers. The executable RAM may be accessed by all 3870 instructions which address main memory indirectly through the Data Counter (DC) register. Additionally, the MK3873 may execute an instruction sequence which resides in the Executable RAM. Note that this cannot be done with the scratchpad RAM memory, which is the reason the term "Executable RAM" is given to this additional memory.

I/O PORTS

On the MK3873, 29 lines are provided for bidirectional, parallel I/O. These lines are addressable as four parallel I/O ports at locations 0, 1, 4, and 5. Note that Ports 0, 4, and 5 are 8 bits wide, while Port 1 contains only 5 bits of I/O in bit positions 3, 4, 5, 6, and 7. Bits 0-2 on Port 1 are not available for use as I/O port pins or as storage elements. The remaining three pins are used to provide the serial I/O

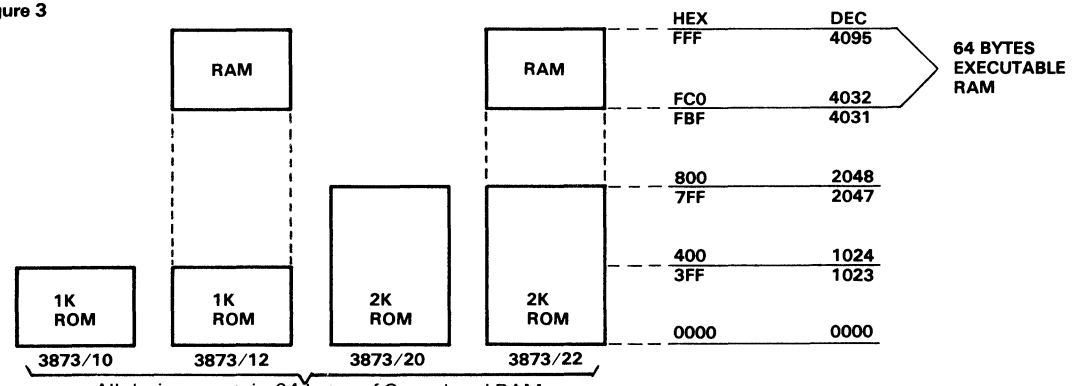
MK3873 PROGRAMMABLE REGISTERS, PORTS, AND MEMORY MAP

Figure 2



MK3873 MAIN MEMORY SIZES AND TYPES

Figure 3



All devices contain 64 bytes of Scratchpad RAM

Data derived from addressing any locations other than within the specified ROM and RAM space is not tested nor is it guaranteed. Users should refrain from entering this area of the memory map.

Device	Scratchpad RAM Size (Decimal)	Address Register Size P0, P, DC, DC1	ROM Size (Decimal)	Executable RAM Size
MK3873/10	64 bytes	12 bits	1024 bytes	0 bytes
MK3873/12*	64 bytes	12 bits	1024 bytes	64 bytes
MK3873/20	64 bytes	12 bits	2048 bytes	0 bytes
MK3873/22*	64 bytes	12 bits	2048 bytes	64 bytes

*The 3873/12 and 3873/22 will be available as future products.

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function. A conceptual schematic of a bidirectional I/O port pin and available output drive options are shown in Figure 4.

As in all other 3870 family devices, an output ready strobe is associated with Port 4. This flag may be used to signal a peripheral device that the 3873 has just completed an output of new data to port 4. The strobe provides a single low pulse shortly after the output operation is completely finished, so either edge may be used to signal the peripheral. STROBE may also be used as an input strobe by doing a dummy output of H '00' to port 4 after completing the input operation.

SERIAL I/O OPERATION

The Serial Input/Output Port consists of a serial Shift Register, baud rate generator and control logic as shown in Figure 1. Together these elements provide the MK3873 with a half duplex asynchronous, or a full duplex synchronous, variable bit length serial port. Data is shifted into or out of the shift register at a rate determined by the internal baud rate generator or external clock. An end-of-word interrupt is generated in transmit or receive mode so that the CPU overhead is only at the word rate and not the serial bit rate.

SHIFT CLOCK

The internal clock is used to clock data transfers into and out of the 16 bit Shift Register. It is also used as an input to an internal counter which keeps track of the number of bits which have been shifted into or out of the Shift Register. Input data is sampled on the SERIAL INPUT, (SI), line on the rising edge of the SHIFT clock and is clocked into the most significant bit of the shift register. Output data is gated to the SERIAL OUTPUT line on the falling edge of the internal SHIFT clock.

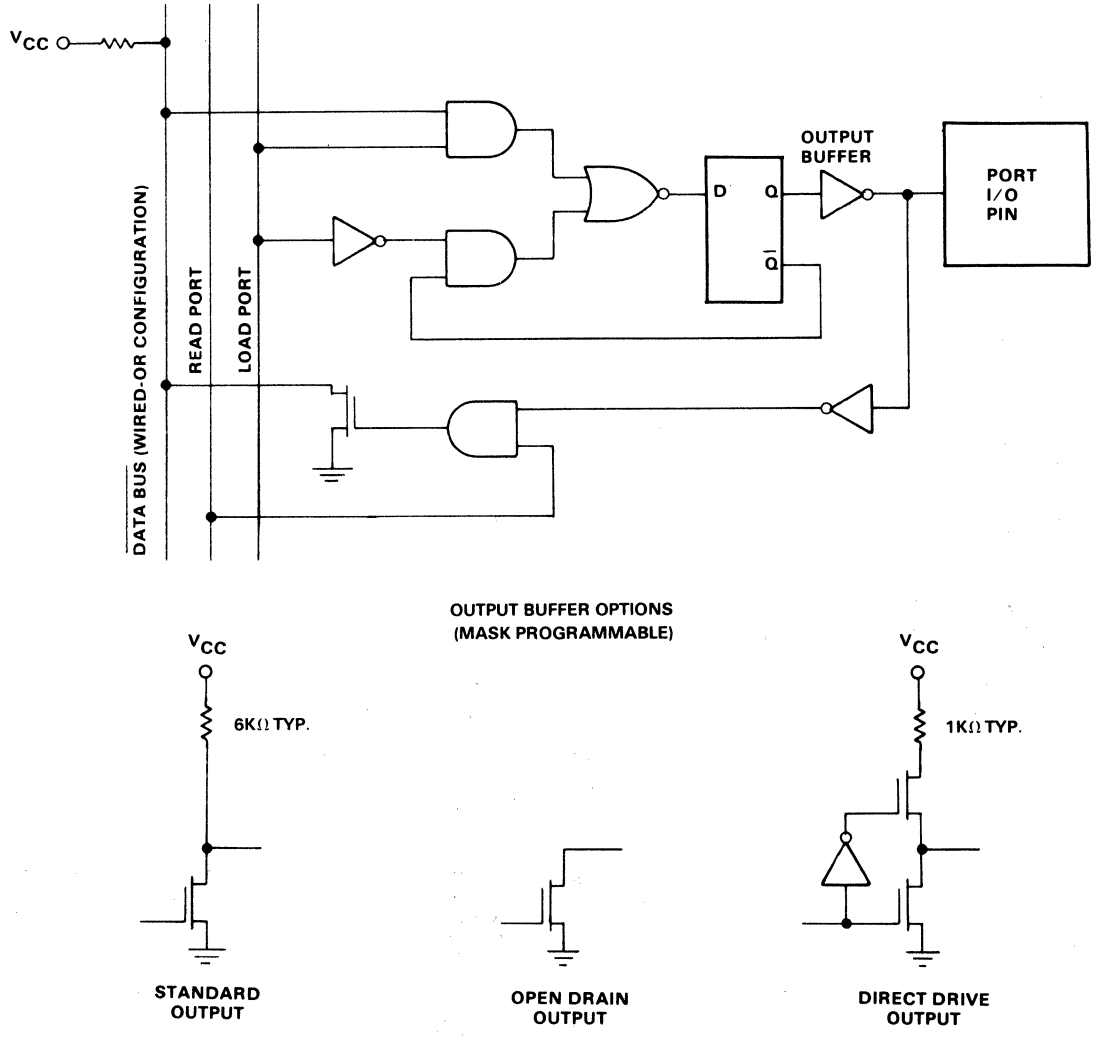
The clock is derived from the SRCLK pulse. The SRCLK pulse may be generated from the internal baud rate generator, or it may be programmed as an input. The internal SHIFT clock operates at the same frequency as the SRCLK pulse when the Sync mode is selected, and at a rate which is divided by 16 (÷16) from the SRCLK pulse when the Async mode is selected.

SHIFT REGISTER

The Serial Port Shift Register is a 16-bit serial to parallel, parallel to serial shift register. This register is addressed and double-buffered by ports E and F as shown in Figure 5A.

I/O PIN CONCEPTUAL DIAGRAM WITH OUTPUT BUFFER OPTIONS

Figure 4



Ports 0 and 1 are Standard Output type only.

Ports 4 and 5 may both be any of the three output options (mask programmable bit by bit)

The $\overline{\text{STROBE}}$ output is always configured similar to a Direct Drive Output except that it is capable of driving 3 TTL loads.

$\overline{\text{RESET}}$ and EXT INT may have standard 6KΩ (typical) pull-up or may have no pull-up (mask programmable). These two inputs have Schmitt trigger inputs with a minimum of 0.2 volts of hysteresis.

Serial In is a Schmitt trigger input with a minimum of 0.2V hysterisis.

Serial Out (SO) is the Standard Output type.

SRCLK output is capable of driving 3 TTL loads.

$\overline{\text{RESET}}$ and EXT INT do not have internal pull up on the MK38P73.

PORT D SERIAL PORT CONTROL REGISTER

The Serial Port Control register is write only and is addressed as Port D. The bit assignment is pictured in Figure 5C. The function of each bit is described below.

N2, N1, N0 - WORD LENGTH SELECT

These bits select one of the eight possible word lengths which are available with the MK3873 serial port. The serial port will shift the programmed number of bits through the Shift Register. If the Transmit mode is selected, data will be shifted out of the least significant bit (SR0) of the Shift Register to the Serial Out line (SO) while data is simultaneosly sampled at the Serial Input (SI) line and shifted into the most significant bit (SR15) of the Shift Register. When the Receive mode is selected, data will be sampled at SI and shifted in, but the SO line will be disabled such that it remains in a marking condition (Logic "1"). After the programmed number of bits have been shifted, the serial port logic will generate an end-of-word condition. This end-of-word condition will cause an interrupt if the serial port INTERRUPT ENABLE bit has been set.

It should be noted that the word values have been chosen so that the MK3873 can be programmed to send and receive a wide variety of asynchronous serial codes with various combinations of start and stop bits. Shown in Figure 6 is a table which gives the word length for various asynchronous data formats.

Values which would be programmed into the MK3873 Serial Port Register for Baudot, ASCII, and 8 bit binary codes in an asynchronous word format are shown in the table of Figure 6. Shown in the table are word length values for various combinations of data bits, start and stop bits, and parity. It can be seen that the MK3873 serial port can accommodate many different word lengths of asynchronous or synchronous data.

SERIAL PORT REGISTERS

Figure 5A

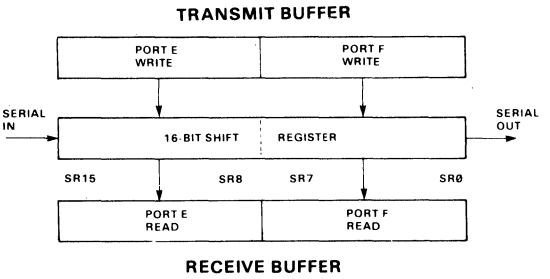


Figure 5B

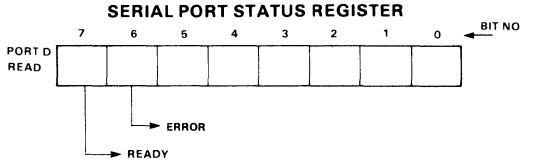
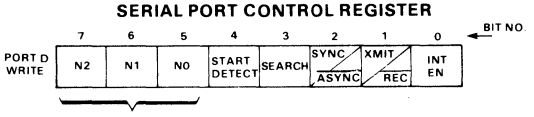


Figure 5C



WORD LENGTH SELECT

N2	N1	N0	WORD LENGTH
0	0	0	4 Bits
0	0	1	7 Bits
0	1	0	8 Bits
0	1	1	9 Bits
1	0	0	10 Bits
1	0	1	11 Bits
1	1	0	12 Bits
1	1	1	16 Bits

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ASYNCHRONOUS WORD LENGTHS

Figure 6

DATA WORD	# OF BITS	START BITS	STOP BITS	PARITY	WORD LENGTH (BITS)
BAUDOT	5	1	1	No	7
	5	1	2	No	8
	5	1	1	Yes	8
	5	1	2	Yes	9
ASCI I	7	1	1	No	9
	7	1	2	No	10
	7	1	1	Yes	10
	7	1	2	Yes	11
8 Bit Binary	8	1	1	No	10
	8	1	2	No	11
	8	1	1	Yes	11
	8	1	2	Yes	12

START DETECT

When the START DETECT bit is enabled the serial port will not shift data through the Shift Register until a valid start bit is detected at the SI input pin. The Start Detect mode is operative only when the Async mode has been selected by programming bit 2 of the Serial Port Control Register to a logic "0". By selecting the Async mode, the internal SHIFT clock frequency is divided by 16 from the clock frequency at the SRCLK pin. (Recall that SRCLK can be an input or an output depending on whether the internal baud rate generator or the external clock is selected). When the START DETECT bit is set, the serial port logic looks for a low level on the SI input on a SRCLK pulse edge. Until this low level occurs, the internal SHIFT clock is held low, and no data is shifted through the shift register. Once the level is sensed, the SI input will be sampled on every SRCLK pulse for seven clock periods. If the logic level remains at zero on the SI input for each of the seven clock periods, the serial port logic will begin shifting data into the Shift Register on the eighth SRCLK pulse. Data will be shifted in at the ÷16 or SHIFT clock rate until the number of bits have been shifted in. Once the programmed number of bits have been shifted, the start detect circuitry will be rearmed and will begin searching for the next high-to-low level on SI. This operation is pictured in the example shown in Figure 7.

When the START DETECT bit is disabled, data is continuously shifted through the Shift Register. An end-of-word condition will be generated each time the programmed number of bits has been shifted into or out of the Shift Register. A serial port interrupt will be generated when the end-of-word condition occurs, if it has been enabled.

SEARCH

The SEARCH bit is enabled by programming it to a logic "1". When enabled, the SEARCH bit causes the serial port logic to generate an interrupt at every bit time if the serial port interrupt has been enabled. This interrupt will occur regardless of whether or not the Transmit or Receive mode has been selected and whether or not the Synchronous or Asynchronous mode has been selected. The Search mode is usually used for recognition of a sync character in synchronous serial data transmission. The MK3873 serial port does not automatically detect sync characters.

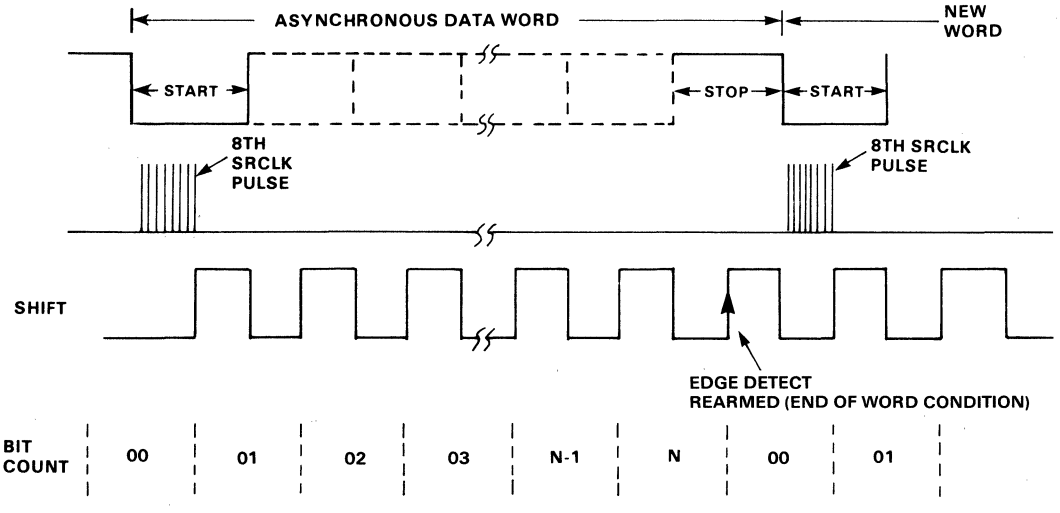
SYNC/ASYNC

The SYNC/$\overline{\text{ASYNC}}$ bit is used to select either the Synchronous mode of operation or the Asynchronous mode of operation. In the Synchronous mode of operation, data is shifted through the Shift Register at a rate which is ÷1 the rate of SRCLK. When the Synchronous mode is selected, the start bit detect circuitry cannot be enabled, even if the START DETECT bit is programmed to a "1". In the Asynchronous mode (SYNC/$\overline{\text{ASYNC}}$ = 0), the internal SHIFT clock operates at a rate which is ÷16 the rate of SRCLK.

XMIT/$\overline{\text{REC}}$

The XMIT/$\overline{\text{REC}}$ bit is used to select either the Transmit or Receive modes of operation. When programmed to a "1" XMIT is selected and the serial port will shift data on the SO line as well as shift data into the SI input. Transmitted data will be enabled on the SO output on the falling edge of the internal SHIFT clock. When the Receive mode is selected (by programming XMIT/$\overline{\text{REC}}$ = 0), data will be clocked into the Shift Register on the rising edge of SHIFT, as it is when the

MK3873 SERIAL PORT START BIT DETECTION
Figure 7



where N is the word length value selected by programming bits N2-N0 in the serial port control register

Transmit mode is enabled, but data will be disabled from being shifted out on Serial Out. Serial Out will be held at a marking, or logic "1", condition.

SERIAL PORT INTERRUPT ENABLE

By programming this bit to a "1", the serial port interrupt will be enabled. A serial port interrupt may then occur when an end-of-word condition is generated. Program control will be vectored to one of two locations upon a serial port interrupt, depending on the way the XMIT/$\overline{\text{REC}}$ bit has been programmed. If the Transmit mode has been selected by programming XMIT/$\overline{\text{REC}}$ bit to a "1", then program control will be vectored to location E0 (Hex). For the Receive mode (XMIT/$\overline{\text{REC}}$ = 0), program control will be vectored to 60 (Hex) when the serial port interrupt occurs. With the addition of the Serial Port Interrupt, the MK3873 has three sources of interrupt. If these three interrupts were to occur simultaneously, priority between them would be such that they would be serviced in the following order:

1) Serial Port
2) Timer
3) External Interrupt

STATUS REGISTER

Reading port D of the MK3873 by performing an Input or Input Short (IN or INS) instruction will load the contents of the Serial Port Status Register into the Accumulator. The two bits which make up the Status Register are shown in Figure 5B. The operation of these two bits is described below:

READY - The meaning of the READY flag depends on whether the Transmit or Receive mode is selected. When the Transmit mode has been selected, the READY flag is set when a Transmit Buffer empty condition occurs. This means that any previous data which may have been loaded into the Transmit Buffer register pair has been transferred into the Shift Register. Loading either byte of the Transmit Buffer will clear the READY flag until the time that the Transmit Buffer register pair is loaded into the Shift Register during an end-of-word condition

In the Receive mode (XMIT/$\overline{\text{REC}}$ = 0), the READY flag is used to indicate a Receive Buffer full condition. This means that a word of the programmed length has been shifted in and has been loaded into the receive buffer register pair. Reading one of the ports E or F which make up the receive buffer register pair will clear the READY flag. The READY flag will remain a 0 until the next word is completely shifted in and loaded into the receive buffer.

It should be noted that writing to the Serial Port Control Register has no effect on the state of the READY flag.

ERROR is like the READY flag; the meaning of ERROR depends on the programming of the XMIT/REC bit in the Serial Port Control Register. When the Transmit mode has been selected ERROR is used to indicate a transmitter underflow condition.

A transmitter underflow condition can occur as follows: Assume that the Transmit mode is selected. Suppose that a word is loaded into the Transmit Buffer register. The serial port logic will load the contents of the Transmit Buffer into the Shift Register and will begin to shift the word out on the SO pin. When the contents of the Transmit Buffer are loaded into the Shift Register, the serial port logic will signal the Transmit Buffer empty condition by setting the READY flag to a "1". When the word in the Shift Register is completely shifted out, an end-of-word condition will be generated. The serial port logic will then check to see if new data has been loaded into the Transmit Buffer. If it has not, the ERROR flag will be set, indicating that the serial port logic has run out of data to send. The ERROR flag can be used to signal an error condition to the firmware, or it can be used to signal that all data has been cleared out of the Shift Register for the purposes of line turnaround.

The ERROR flag which, in this case, represents a transmitter underflow condition, is reset by reading the Status Register.

When the Receive mode is programmed, ERROR is used to signal that the Receive Buffer has overflowed. This overflow condition can occur as follows: Suppose that a serial word is shifted in, generating an end-of-word condition. The serial port logic will load the contents of the Shift Register into the Receive Buffer, and will set the READY flag to a "1" to indicate that the Receive Buffer is full. When the next word being received is completely shifted in, generating the next end-of-word condition, the serial port logic will check to see if the Receive Buffer has been read by examining the state of the READY flag. If the READY flag = 0, then the previous word has already been read from the Receive Buffer by the software, and the serial port logic will load the current word into the Receive Buffer and will again set the READY flag. If the READY flag = 1, then the previous word has not been read from the Receive Buffer. The serial port logic will load the new word into the Receive Buffer, destroying the previous word. This action is signalled by the serial port logic setting the ERROR to a "1" signalling a receive buffer overflow condition. In this case, reading the status register also clears the ERROR flag.

BAUD RATE CONTROL REGISTER

Port C is designated as the Baud Rate Control register. Four bits, 0-3, are used to select nine different internal Baud rates or an external clock. When an internal Baud rate is programmed, the SRCLK output is generated at a frequency which is divided from the MK3873's time base frequency. The SRCLK frequency can be calculated by dividing the time base frequency by the divide factor shown in Figure 8 for the bit pattern which is programmed into bits C3-C0. Also shown in Figure 7 is the programming of bits C3-C0 to obtain a set of standard Baud rates when a 3.6864 MHz crystal is used as a time base.

BAUD RATE CONTROL PORT
PORT C WRITE ONLY
Figure 8

PORT C WRITE 7 6 5 4	3	2	1	0	Bit No.	SRCLK Divide Factor	Shift Clock Rate @ 3.6864 MHz time base SYNC	ASYNC
X X X X	C3	C2	C1	C0				
	1	0	1	1		÷24	153.6 kbs	9600 bps
	1	0	1	0		÷48	76.8 kbs	4800 bps
	1	0	0	1		÷96	38.4 kbs	2400 bps
	1	0	0	0		÷192	19.2 kbs	1200 bps
	0	1	1	1		÷384	9600 bps	600 bps
	0	1	1	0		÷768	4800 bps	300 bps
	0	1	0	1		÷1536	2400 bps	150 bps
	0	1	0	0		÷2096	1758.8 bps	110 bps
	0	0	1	1		÷3072	1200 bps	75 bps
	0	0	0	0		External Clock Mode		

When any of the internal Baud rates are selected, pin 36 becomes an output port pin. This pin is capable of driving three standard TTL inputs and provides a square wave output from the frequency selected in port C. The SYNC/$\overline{\text{ASYNC}}$ bit in the Serial I/O Control register has no effect on the output clock rate. The output will always be ÷1 directly from the Baud rate generator.

If all zeros are loaded into this port, the External Clock mode is selected. Pin 36 becomes an input. Any TTL compatible square wave input can be used to generate the clock for the serial port.

TRANSMIT AND RECEIVE BUFFERS

The Receive Buffer registers are two eight bit registers which are addressed as ports E and F (Hex) and are read only. The Receive Buffer registers may be read at any time. The Transmit Buffer registers are also two 8-bit registers which are write only and addressed as ports E and F (Hex).

In the Receive mode, the contents of the 16 bit Shift Register are transferred to the Receive Buffer Register pair when a complete word has been shifted in. Bits SR15-SR8 of the Shift Register are loaded into bits 7-0 of port E while bits SR7-SR0 are loaded into bits 7-0 of Port F.

When entering the Transmit mode, the first data transfer from the Transmit Buffer to the 16 bit Shift Register won't occur until a 1 word time delay after entering Transmit Mode.

In the Receive mode, no transfers between the Transmit Buffer and the 16 bit Shift Register can occur.

The serial port does not automatically right justify incoming data, nor does it insert or strip start and stop bits from an asynchronous data word. Therefore, it is usually necessary to right justify incoming data read from the Receive Buffer registers in software through shift instructions, as well as strip start and stop bits if an asynchronous data format is being used. Likewise, in transmitting an asynchronous data word, it is usually necessary to insert start and stop bits in software into the 16 bit word which is to be loaded in two halves into the Transmit Buffer register.

RESET

The reset circuit on the MK3873 is used to initialize the device to a known condition either during the course of program execution or on a power on condition. This section discusses the effect of $\overline{\text{RESET}}$ on the serial port logic. A more complete description of $\overline{\text{RESET}}$ may be found in the 3870 Family Technical Manual.

Upon reset, both the serial port control register (port D) and the Baud Rate Control register (port C) are loaded with zeroes. This action sets the serial port control logic in the following state:

N2, N1, N0 (word length) = 4 bits
START DETECT disabled
SEARCH disabled
Asynchronous Receive mode
Serial port interrupt disabled
External Clock mode (SRCLK = 1).
READY and ERROR are reset
Ports E and F are undefined

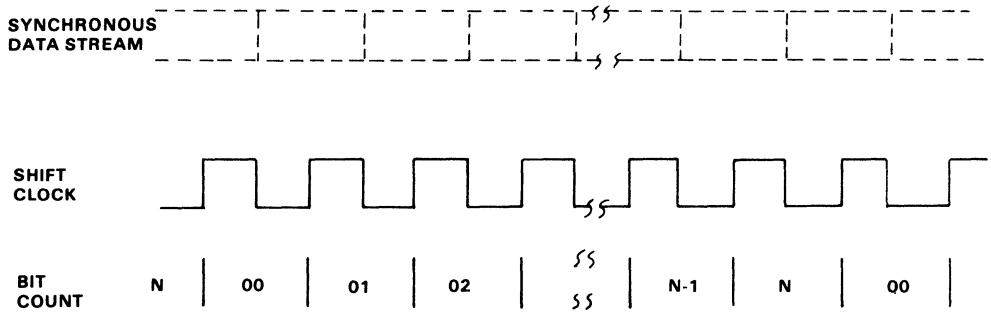
After the first control word is written to the Serial Port Control Register which selects an internal clock mode, the SRCLK will become an output and will remain high for one-half of a clock period as programmed into port C. It will then go low and produce a clock output waveform with the selected frequency.

ASYNCHRONOUS RECEIVE OPERATION

Figure 7 illustrates the timing for an example using the serial port in the Asynchronous mode. When operating in this mode, the Serial Port Control Register should be programmed for receive (XMIT/$\overline{\text{REC}}$ = 0) and the START DETECT bit should be enabled. Also, the Async mode should be selected, which allows the start detect circuitry to operate and sets the internal SHIFT clock at a rate which is divided by 16 (÷16) from the SRCLK rate. Upon selecting the Async mode and the START DETECT bit, the internal SHIFT clock is held low until a low level occurs on the SI pin. After a valid edge has been detected (see the START DETECT bit operation section), the SHIFT clock will go high and data will be shifted in at the middle of each bit time. When the programmed number of bits has been shifted in, an end-of-word condition is generated and a serial port receive interrupt will occur if it has been enabled.

After the falling edge of SHIFT following the end-of-word interrupt, the start detect circuitry will be enabled in preparation for the next word. Thus, if a start bit is present immediately following the time when the start detect circuitry is enabled, SHIFT Clock will again go high approximately on bit-time after the rising edge of SHIFT which clocked in the last bit of the preceding word and caused the end-of-word interrupt. In other words, SHIFT can go high again on

SYNCHRONOUS TRANSMIT OR RECEIVE TIMING
Figure 9



the eighth SRCLK pulse as soon as the start detect circuitry is rearmed.

The Shift Register must be read before the next end-of-word condition; otherwise, a receiver overrun error will occur. For a 9600 bps data rate, this would require reading the Receive Buffer within N x 104 μs from the time that the end-of-word condition is generated, where N is the number of bits in the data word.

The example in Figure 7 shows the timing required for asynchronous data reception from a device such as a teletype. Within this data stream are start, data and stop bits. A typical format requires 1 start bit, 8 data bits and 2 stop bits for a total of 11 bits. All of these bits will be residing in the 16 bit Shift Register when the end-of-word interrupt is generated. It is, therefore, necessary to strip the start and stop bits from the data.

SYNCHRONOUS RECEIVE OPERATION

For synchronous operation, the START DETECT bit should not be enabled and the XMIT/$\overline{\text{REC}}$ bit should be programmed to a zero. Also the Sync mode should be enabled so that the internal SHIFT clock is divided by 1, or is equivalent to, SRCLK. Once a control word is written to port D specifying START DETECT = 0, Receive mode, and Sync mode, then the Serial Port will continuously shift data into the MSB of the upper half of the Shift Register at the SRCLK rate and will generate an end-of-word condition when the programmed number of bits have been shifted in.

An illustration of synchronous receive timing is shown in Figure 9. This diagram is a synchronous receive sequence for a word which is N bits in length, where N corresponds to the number of bits which have been programmed into the Serial Port Control Register. Note the relationship of SHIFT clock, the synchronous data stream, and the bit count. Since the START DETECT bit is not enabled, the serial port logic will continuously shift data in and generate end-of-word conditions at regular intervals. When the end-of-word condition occurs, a serial port receive interrupt occurs if it has been enabled, and the contents of the Shift Register will be loaded into the Receive Buffer. The serial port logic will set the READY flag in the Serial Port Status Register, indicating that the receive buffer is full. Since the serial port is double-buffered on receive, the program has entire word time to read the Receive Buffer. At 9600 bps, this corresponds to a word time of N x 104μs, where N is the number of bits in a word.

Note that if a new control word is written to port D during the time that a serial word is shifted in, the bit count will be reset.

When using the Synchronous Receive mode on the MK3873, it is usually necessary to establish word synchronization in the data stream. The SEARCH bit, when enabled, causes the serial port logic to interrupt on each rising edge of SHIFT so that the data stream can be examined on a bit by bit basis. When the last bit of a sync word is found, the Search mode can be disabled and the serial port logic will shift in data and interrupt at the word rate.

ASYNCHRONOUS TRANSMIT OPERATION

The Asynchronous Transmit mode of operation is initiated by setting the XMIT/$\overline{\text{REC}}$ bit to a "1", and by programming the SYNC/$\overline{\text{ASYNC}}$ bit to a "0". Also, there must be an SRCLK pulse by selecting an internal or external source for SRCLK by programming port C. Upon setting XMIT/$\overline{\text{REC}}$ to a "1", there will be a 1 word length delay prior to the actual transfer of the first word from the Transmit Buffer to the 16 bit Shift Register. Serial data will then be shifted to the right on each rising edge of the internal SHIFT clock, and each new bit in the data stream will be enabled onto the SERIAL OUTPUT pin (SO) at the time of the falling edge of the

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internal SHIFT clock.

As mentioned, one word time delay is generated between the time that the Transmit mode is initiated by programming XMIT/$\overline{REC}$ = 1 and the time that the contents of the Transmit Buffer are transferred into the Shift Register. This word time delay is generated internally to the MK3873 by counting the number of SHIFT clock pulses which correspond to the number of bits programmed into the word length select section of the Serial Port Control Register (N2, N1, N0). Therefore, the word time delay is equivalent to the time it takes to shift a complete serial data word out of the Shift Register. The same word time delay will result if data had been loaded prior to programming the XMIT/$\overline{REC}$ bit to a "1". As mentioned in the "START DETECT" bit description, the internal SHIFT clock is disabled when this bit is programmed to a "1". Since the serial port logic counts SHIFT clock pulses to generate the word time delay, the Transmit Buffer contents will never be transferred to the Shift Register and shifted out when the START DETECT bit is enabled. Also, the Transmit Buffer contents cannot be loaded into the Shift Register when XMIT/$\overline{REC}$ bit = 0.

When the initial serial data word has been transferred into the Shift Register, the READY flag is set in the Serial Port Status Register, which is used to indicate that the Transmit Buffer is empty. A transmit interrupt will be generated if the INTERRUPT ENABLE bit has been set in the Serial Port Control Register, and program control will be vectored to location E0 (hex). When operating the serial port in a polled environment with the serial port interrupt disabled, the READY bit can be used as a flag which indicates that new data may be loaded into the Transmit Buffer. In an interrupt driven software configuration, new data may be loaded into the Transmit Buffer at the beginning of the serial port interrupt service routine.

During the operation of the Transmit Mode, the SERIAL INPUT pin (SI) is sampled and shifted into the Shift Register. However, since the START DETECT bit must be disabled during a transmit sequence, there is no way of establishing bit synchronization on any incoming serial data. Therefore, in the Asynchronous mode, the serial port can only be used in a half-duplex configuration.

After a block of data has been sent, it is sometimes useful for the program to know when the last serial word has been shifted out of the shift register. This is especially useful when operating the MK3873 with a bidirectional half-duplex transmission line. Once the block of serial data has been completely shifted out of the port, then it is usually desirable to reverse the direction of the line so that data may be received.

One way of determining when the last word has been shifted out of the Shift Register is through the use of the ERROR status bit in the Serial Port Status Register. The sequence would take place as follows: the program loads the Transmit Buffer with the last serial data word which is to be sent out either when the "READY" bit is set or during a transmit interrupt service routine. Loading the Transmit Buffer clears the READY flag. At the next end-of-word condition, the last serial data word is transferred from the Transmit Buffer into the Shift Register, which sets the READY flag once again. At this point the program will not load any more data into the Transmit Buffer and the READY flag will remain set. When the last word is completely shifted out of the Shift Register, the serial port logic will check to see if any new data has been loaded into the Transmit Buffer register pair. When it determines that there are no new data in the Transmit Buffer, the serial port logic will set the ERROR bit in the serial port status register and will return the SERIAL OUTPUT pin (SO) to a making condition (logic "1"). The SERIAL OUTPUT pin (SO) is always returned to a marking condition on transmitter underflow when the ASYNC mode is selected. Since the ERROR bit is set when the last serial data word has completely been sent out, it can be used as a signal to indicate the end of transmission and that the direction of the transmission line may be set for receive.

SYNCHRONOUS TRANSMIT OPERATION

The Synchronous Transmit mode of operation is selected by programming bit 2 (XMIT/$\overline{REC}$) of the Serial Port Control register to a "1" and setting the SYNC/$\overline{ASYNC}$ bit to a "1".

Figure 9 illustrates serial output timing relationships in the Synchronous mode. Data are shifted to the right on each rising edge of the internal SHIFT clock. Output data are not enabled to the SERIAL OUTPUT pin (SO) until the falling edge of the SHIFT clock. In a 16 bit data word, SR0, the least significant bit of the Shift Register is shifted out first, and SR15, the most significant bit of the Shift Register, is shifted out last. While the Shift Register contents are being output on a bit by bit basis, data are simultaneously shifted in to the Shift Register through the SI pin.

As discussed in the "ASYNCHRONOUS TRANSMIT OPERATION" section, a word time delay is generated between the time that data is written to the Transmit Buffer and the time that the contents of the Transmit Buffer are loaded into the Shift Register once the XMIT/$\overline{REC}$ bit has been programmed to a one (1).

Another way of loading the initial data word into the Transmit Buffer requires that the word synchronization be achieved through recognition of a received sync character. Recall that in the Transmit mode, data are sampled at SI and shifted into the Shift Register at the same time that data are shifted out through SO. Upon power up or reset, a control word may be written to Port D which specifies Transmit and Synchronous modes. Word synchronization can then be achieved through the use of the SEARCH bit as described in the section which covers Synchronous Receive mode. Once word synchronization is achieved, the SEARCH bit is disabled and the serial port shifts in data and generates an end-of-word condition at the word rate.

Each time the end of word condition is reached, receive data

is transferred from the shift register into the Receive Buffer. At the same time, data is transferred from the Transmit Buffer into the Shift Register.

Therefore, in the Synchronous Transmit mode, the serial port may be used in a full duplex mode if word synchronization is established. At each end of word condition, output data is transferred to the Shift Register from the Transmit Buffer. At the same time, an incoming data word is transferred from the Shift register to the Receive Buffer register pair. In this case, the End-of-Word transmit routine would be used for sending data by loading the Transmit Buffer register, and for receiving data by reading the Receive Buffer register. Note that once word synchronization is established, an amount of time which is equal to one word time is available following the end-of-word interrupt for loading data into the Transmit Buffer.

The serial port operates differently in the Transmit mode for Synchronous operation that it does for Asynchronous operation. In the Asynchronous mode, after a word has been shifted out, the SO line is returned to a marking condition if no new data have been loaded into the Transmit Buffer.

In the Synchronous mode, after a word has been shifted out, the contents of the Transmit Buffer are loaded into the Shift Register regardless of whether or not new data were loaded into the Transmit Buffer. If new data were not loaded since the last time the transmit buffer was read, the ERROR flag is set and signals a transmitter underflow condition. This feature of always reloading the Shift Register with the contents of the Transmit Buffer when an end-of-word condition occurs allows a sync word to be continuously generated without CPU intervention when the transmitter is idle. This feature also allows for a variable duty cycle, variable frequency waveforms to be generated on the Serial Output line.

MK38P73 GENERAL DESCRIPTION

The MK38P73 is the EPROM version of the MK3873. It retains an identical pinout with the MK3873. The MK38P73 is housed in the "R" package which incorporates a 28 pin socket located directly on top of the package.

The MK38P73 can act as an emulator for the purpose of verification of user code prior to the ordering of mask ROM MK3870 devices. Thus, the MK38P73 eliminates the need for emulator board products. In addition, several MK38P73s can be used in prototype systems in order to test design concepts in field service before committing to high-volume production with mask ROM MK3873s. The compact size of the MK38P73/EPROM combination allows the packaging of such prototype systems to be the same as that used in production.

Finally, in low-volume applications, the MK38P73 can be used as the actual production device.

Most of the material which has been presented for the MK3873 applies to the MK38P73. The MK38P73 has the same architecture and pinout as the MK3873. Additional information is presented in the following sections.

MK38P73 MAIN MEMORY

As can be seen from the block diagram in Figure 10, the MK38P73 contains no on-chip ROM. The memory address and data lines are brought out to the 28 pin socket located directly on top of the 40 pin package. The MK38P73 will address up to 4096 bytes of external EPROM memory.

There is one memory version of the MK38P73, and it is designated as the MK38P73/02. The MK38P73/02 contains 64 bytes of on-chip executable RAM. The MK38P73/02 can emulate the following mask ROM MK3873 devices:

MK3873/10
MK3873/12
MK3873/20
MK3873/22

Addressing of main memory on the MK38P73 is accomplished in the same way as it is for the MK3873. See Figure 12 for Main Memory addresses and for address register size in the MK38P73.

MK38P73 EPROM SOCKET

A 28 pin EPROM socket is located on top of the MK38P73 "R" package. The socket and compatible EPROM memories are shown in Figure 11. When 24 pin memories are used in the 28 pin socket, they should be inserted so that pin 1 of the memory device is plugged into pin 3 of the socket. (The memory should be lower justified in the 28 pin socket.)

The 28-pin socket has been provided to allow use of both 24-pin and 28-pin memory devices. Minor pin-out differences in the memory devices must be accommodated by providing different versions of the MK38P73.

Initially, the MK38P73 that is compatible with the MK2716 is available. The MK38P73 designed to accommodate the 28-pin memory devices will be available at a later date.

MK38P73 I/O PORTS

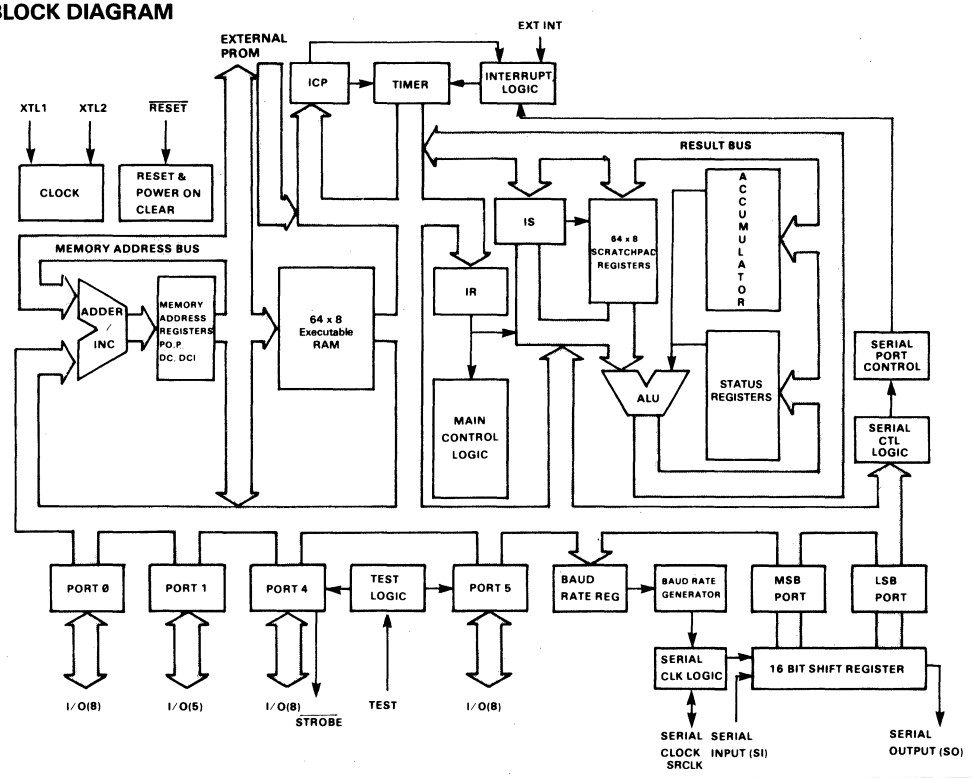
The MK38P73 is offered with open drain type output buffers on Ports 4 and 5. This open drain version is provided so that user-selected open drain port pins on the mask ROM MK38P73 can be emulated prior to ordering those mask ROM parts. Figure 11 lists the part ordering number for an MK38P73/02.

MEMORY ACCESS TIMING

A timing diagram depicting the memory access timing of the MK38P73 is shown in Figure 13. The Φ clock signal is

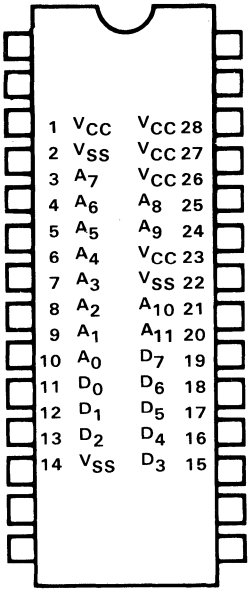
MK38P73 BLOCK DIAGRAM

Figure 10



MK38P73 "R" PACKAGE PINOUT

Figure 11



MK97310 (Open Drain)
Compatible Memories
2758
MK2716
2516 2532

derived internally in the MK38P73 by dividing the time base frequency by two and is used to establish all timing frequencies. The WRITE signal is another internal signal to the MK38P73 which corresponds to a machine cycle during which time a memory access may be performed. Each machine cycle is either 4 Φ clock periods or 6 Φ clock periods long. These machine cycles are termed short cycles and long cycles respectively. The worst case memory cycle is the short cycle, during which time an op code fetch is performed. This is the cycle which is pictured in the timing diagram. After a delay from the falling edge of the WRITE clock, the address lines A_{11} - A_0 become stable. Data must be valid at the data out lines of the PROM for a setup time prior to the next falling edge of the WRITE pulse. The total access time available for the MK38P73 is shown as t_{aas}, or the time from when address is stable to when data must be valid on the data bus lines.

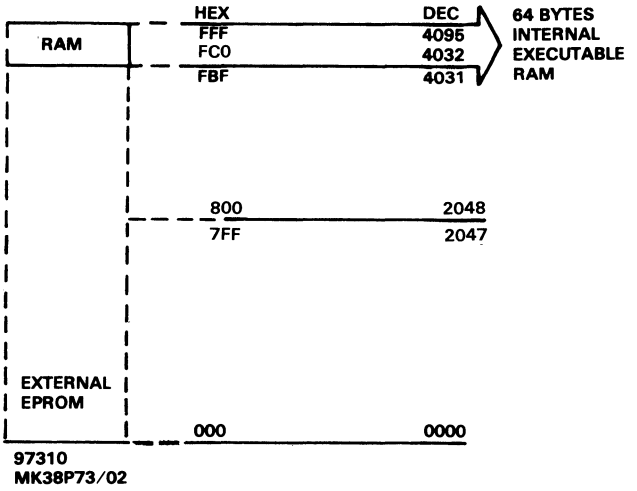
An equation for calculating available memory access time and some calculated access times based on the listed time base frequencies is also shown in Figure 13.

3873 TIME BASE OPTIONS

The 3873 contains an on-chip oscillator circuit which provides an internal clock. The frequency of the oscillator circuit is set from the external time base network. The time

MK38P73 MAIN MEMORY MAP

Figure 12



Device	Scratchpad RAM Size (Decimal)	Address Register Size P0, P, DC, DC1)	ROM Size (Decimal)	Executable RAM Size
MK38P73/02 97310	64 bytes	12 bits	0 bytes	64 bytes

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base for the 3873 may originate from one of four sources:

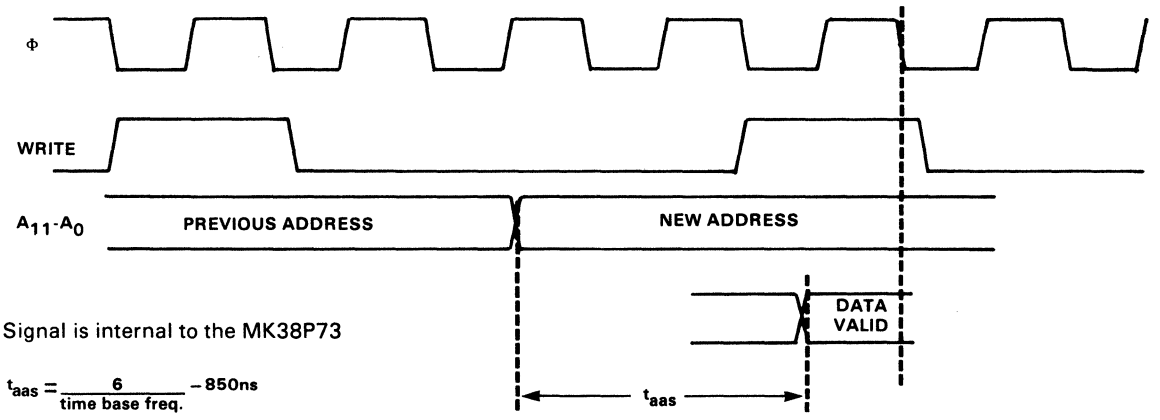
1) Crystal
2) LC Network
3) RC Network
4) External Clock

The type of network which is to be used with the mask ROM MK3873 must be specified at the time when mask ROM devices are ordered. However, the MK38P73 may operate with any of the four configurations so that it may emulate any configuration used with a mask ROM device.

The specifications for the four configurations are given in the following text. There is an internal 26pF capacitor between XTL 1 and GND and an internal 26pF capacitor between XTL 2 and GND. Thus, external capacitors are not necessarily required. In all external clock modes the external time base frequently is divided by two to form the internal PHI clock.

MEMORY ACCESS SHORT CYCLE OP CODE FETCH MK38P73

Figure 13



Signal is internal to the MK38P73

$$t_{aas} = \frac{6}{\text{time base freq.}} - 850ns$$

(FROM ADDRESS STABLE)

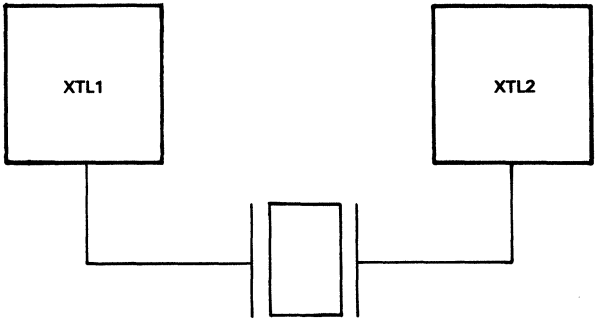
	4MHz	3.58MHz	3MHz	2.5MHz	2MHz
ACCESS TIME	650ns	825ns	1.15μs	1.55μs	2.15μs

CRYSTAL SELECTION

The use of a crystal as the time base is highly recommended as the frequency stability and reproductiveness from system to system is unsurpassed. The 3873 has an internal divide by two to allow the user of inexpensive and widely available TV Color Burst Crystals (3.58MHz). Figure 15 lists the required crystal parameters for use with the 3873. The Crystal Mode time base configuration is shown in Figure 14.

CRYSTAL MODE CONNECTION

Figure 14



CRYSTAL PARAMETERS
Figure 15

a) Parallel resonsnace, fundamental mode AT-Cut
b) Shunt capacitance (C_0) = 7 pf max.
c) Series resistance (R_S) = See table
d) Holder = See table below.

Frequency	Series Resistance	Holder
f = 2-2.7 MHz	Rs = 300 ohms max	HC-6 HC-33
f = 2.8-4 MHz	Rs = 150 ohms max	HC-6 HC-18* HC-25* HC-33

*This holder may not be available at frequencies near the lower end of this range.

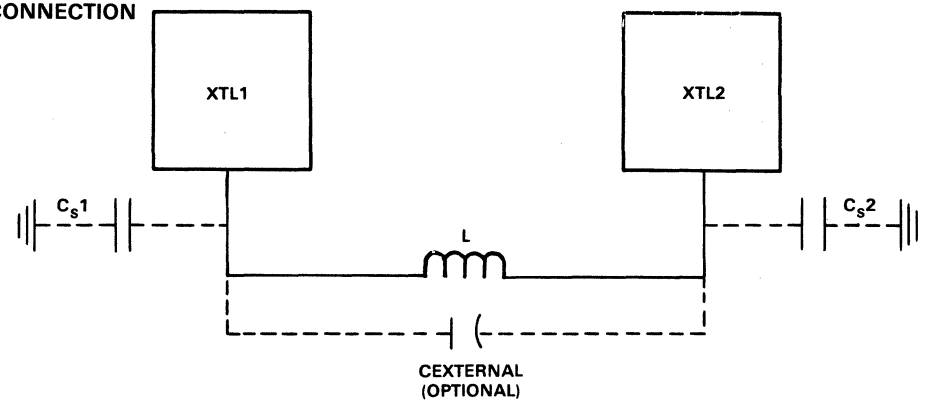
Through careful buffering of the XTL1 pin it may be possible to amplify this waveform and distribute it to other devices. However, Mostek recommends that a separate active device (such as a 7400 series TTL gate) be used to oscillate the crystal and that the waveform from that oscillator be buffered and supplied to all devices, including the 3873, in the event that a single crystal is to provide the time base for more than just a single 3873.

While a ceramic resonator may work with the 3873 crystal oscillator, it was designed specifically to support the use of this component. Thus, Mostek does not support the use of a ceramic resonator either through proper testing, parametric specification, or applications support.

LC NETWORK

The LC time base configuration can be used to provide a less expensive time base for the 3873 than can be provided with a crystal. However, the LC configuration is much less accurate than is the crystal configuration. The LC time base configuration is shown in Figure 16. Also shown in the figure are the specified parameters for the LC components, along with the formula for calculating the resulting time base frequency. The minimum value of the inductor which is required for proper operation of the LC time base network is 0.1 millihenries. The inductor must have a Q factor which is no less than 40. The value of C is derived from C external, the internal capacitance of the 3873, C_{XTL}, and the stray capacitances, C_{S1} and C_{S2}. C_{XTL} is the capacitance looking into the internal two port network at XTL1 and XTL2. C_{XTL} is listed under the "Capacitance" section of the Electrical Specifications. C_{S1} and C_{S2} are stray capacitances from XTL1 to ground and from XTL2 to ground, respectively. C external should also include the stray shunt capacitance across the inductor. This is typically in the 3 to 5 pf range, and significant error can result if it is not included in the frequency calculation.

LC MODE CONNECTION
Figure 16



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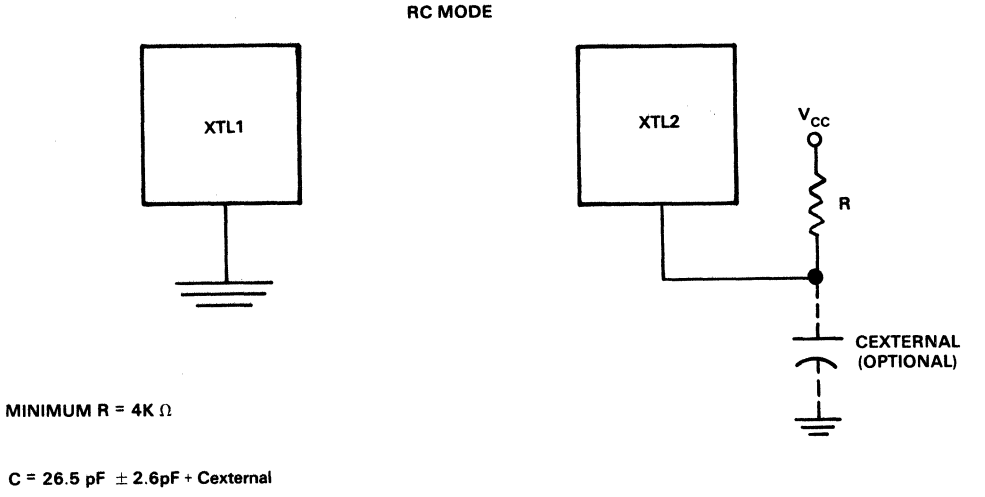
Variation in time base frequency with the LC network can arise from one of four sources: 1) Variation in the value of the inductor. 2) Variation in the value of the external capacitor. 3) Variation in the value of the internal capacitance of the 3873 at XTL1 and XTL2, and 4) Variation in the amount of stray capacitance which exists in the circuit. Therefore, the actual frequency which is generated by the LC circuit is within a range of possible frequencies, where the range of frequencies is determined by the worst case variation in circuit parameters. The designer must select component values such that the range of possible frequencies with the LC mode does not go outside of the specified operating frequency range for the 3873.

RC CLOCK CONFIGURATION

The time base for the 3873 may be provided from an RC network tied to the XTL2 pin, when XTL1 is grounded. A schematic picturing the RC clock configuration is shown in Figure 17. The RC time base configuration is intended to provide an inexpensive time base source for applications in which timing is not critical. Some users have elected to tune each unit using a variable resistor or external capacitor, thus reducing the variation in frequency. However, for increased time base accuracy, Mostek recommends the use of the Crystal or LC time base configuration. Figure 18 illustrates a curve which gives the resulting operating frequency for a particular RC value. The x-axis represents the product of the value of the resistor times the value of the capacitor. Note that three curves are actually shown. The curve in the middle represents the nominal frequency obtained for a given value of RC. A maximum curve and a minimum curve for different types of 3873 devices are also shown in the diagram.

RC MODE CONNECTION
Figure 17



The designer must select the RC product such that a frequency of less than 2 MHz is not possible, taking into account the maximum possible RC product and using the minimum curve shown in Figure 18. Also, the RC product must not allow a frequency of more than 4 MHz, taking into account the minimum possible R and C and using the Maximum curve shown. Temperature induced variations in the external components should be considered in calculating the RC product.

Frequency variation from unit to unit due to switching speed and level at constant temperature and V_{CC} = + or - 5 percent.

Frequency variation due to V_{CC} with all other parameters constant with respect to +5V = +7 percent to -4 percent on all devices.

Frequency variation due to temperature with respect to 25 C (all other parameters constant) is as follows:

PART #	VARIATION
387X-00, -05	+6 percent to - 9 percent
387X-10, -15	+9 percent to -12 percent

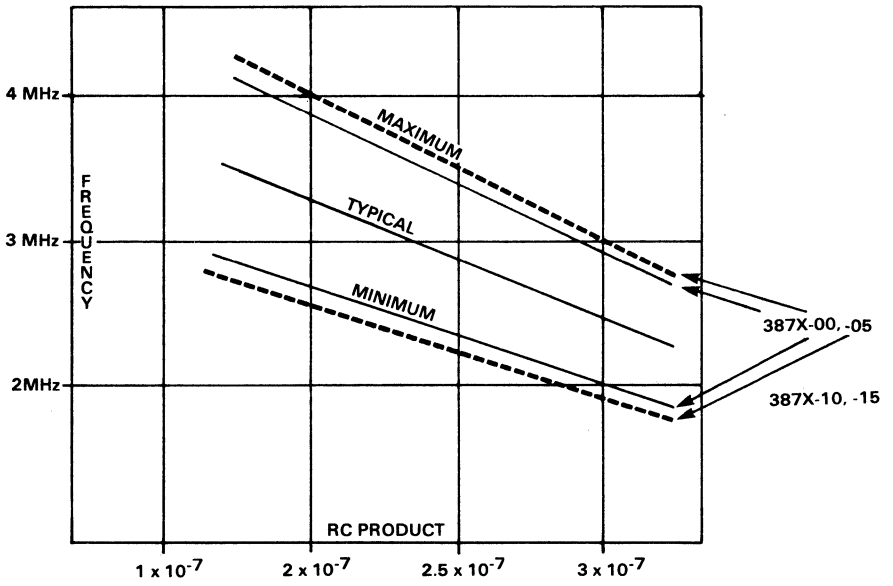
Variations in frequency due to variations in RC components may be calculated as follows:

Maximum RC = (R max) (C external max + C_{XTL} max)

Minimum RC = (R min) (C external min + C_{XTL} min)

$$\text{Typical RC} = (\text{R typ})\left(\text{C external typ} + \frac{\{C_{XTL}\ \text{max} + C_{XTL}\ \text{min}\}}{2}\right)$$

FREQUENCY VS. RC
Figure 18



Positive Freq. Variation = RC typical - RC minimum / RC typical

Negative Freq. Variation = RC maximum - RC typical / RC typical
due to RC Components

Total frequency variation due to all factors:

387X-00, -05
= +18 percent plus positive frequency variation due to RC components

= -18 percent minus negative frequency variation due to RC components

387X-10, -15
= +21 percent plus positive frequency variation due to RC components

= -21 percent minus negative frequency variation due to RC components

Total frequency variation due to V_{CC} and temperature of a unit tuned to frequency at +5V V_{CC}, 25 C

387X-00, -05
= + 13 percent

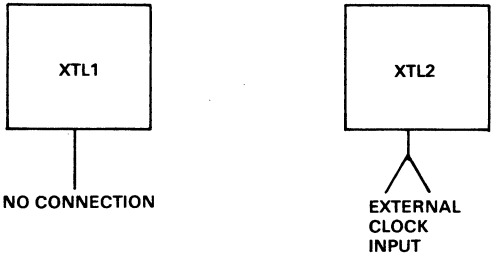
387X-10, -15
= + 16 percent

EXTERNAL CLOCK CONFIGURATION

The connection for the external clock time base configuration is shown in Figure 19. Refer to the DC Characteristics section for proper input levels and current requirements.

Refer to the Capacitance section of the appropriate 3873 Family device data sheet for input capacitance.

EXTERNAL MODE CONNECTION
Figure 19



OPERATING VOLTAGES AND TEMPERATURES

Dash Number Suffix	Operating Voltage V_{CC}	Operating Temperature T_A
—00	+5V ± 10%	0°C - 70°C
—05	+5V ± 5%	0°C - 70°C
—10	+5V ± 10%	-40°C - +85°C
—15	+5V ± 5%	-40°C - +85°C

ABSOLUTE MAXIMUM RATINGS*

	-00,-05	-10,-15
Temperature Under Bias	-20°C to +85°C	-50°C to +100°C
Storage Temperature	-65°C to +150°C	-65°C to +150°C
Voltage on any Pin With Respect to Ground (Except open drain pins and TEST)	-1.0V to +7V	-1.0V to +7V
Voltage on TEST with Respect to Ground	-1.0V to +9V	-1.0V to +9V
Voltage on Open Drain Pins With Respect to Ground	-1.0V to +13.5V	-1.0V to + 13.5V
Power Dissipation	1.5W	1.5W
Power Dissipation by any one I/O pin[2]	60mW	60mW
Power Dissipation by all I/O pins[2]	600mW	600mW

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

AC CHARACTERISTICS

T_A, V_{CC} within specified operating range.
I/O Power Dissipation ≤ 100mW (Note 2)

SIGNAL	SYM	PARAMETER	-00,-05 MIN	-00,-05 MAX	-10,-15 MIN	-10,-15 MAX	UNIT	NOTES
XTL1 XTL2	t_0	Time Base Period, all clock modes	250	500	250	500	ns	4MHz-2MHz
	$t_{ex(H)}$	External clock pulse width high	90	400	100	390	ns	
	$t_{ex(L)}$	External clock pulse width low	100	400	110	390	ns	
Φ	t_Φ	Internal Φ clock	$2t_0$		$2t_0$			
WRITE	t_W	Internal WRITE Clock period	4tΦ 6tΦ		4tΦ 6tΦ			Short Cycle Long Cycle
I/O	$t_{dI/O}$	Output delay from internal WRITE clock	0	1000	0	1200	ns	50pF plus one TTL load
	$t_{sI/O}$	Input setup time to internal WRITE clock	1000		1200		ns	
$\overline{STROBE}$	$t_{I/O-s}$	Output valid to $\overline{STROBE}$ delay	3tΦ -1000	3tΦ +250	3tΦ -1200	3tΦ +300	ns	I/O load = 50pF + 1 TTL load
	t_{sL}	$\overline{STROBE}$ low time	8tΦ -250	12tΦ +250	8tΦ -300	12tΦ +300	ns	$\overline{STROBE}$ load = 50pF+3TTL loads
$\overline{RESET}$	t_{RH}	$\overline{RESET}$ hold time, low	6tΦ +750		6tΦ +1000		ns	
	t_{RPOC}	$\overline{RESET}$ hold time, low for power clear	power supply rise time +0.1		power supply rise time +0.15		ms	
EXT INT	t_{EH}	EXT INT hold time in active and inactive state	6tΦ +750		6tΦ +1000		ns	To trigger interrupt
			2tΦ		2tΦ		ns	To trigger timer

CAPACITANCE
T_A = 25°C
All Part Numbers

SYM	PARAMETER	MIN	MAX	UNIT	NOTES
C_{IN}	Input capacitance; I/O, $\overline{RESET}$, EXT INT, TEST		10	pF	unmeasured pins grounded
C_{XTL}	Input capacitance; XTL1, XTL2	23.5	29.5	pF	

AC CHARACTERISTICS FOR SERIAL I/O PINS
T_A, V_{CC} within specified operating range.
I/O Power Dissipation ≤ 100mW (Note 2)

			-00, -05		-10, -15			
SIGNAL	SYM	PARAMETER	MIN	MAX	MIN	MAX	UNIT	CONDITIONS
SRCLK	$t_{C(SRCLK)}$	Serial Clock Period in External Clock Mode Async	3.25	∞	3.25	∞	μs	
		Sync	4.0	∞	4.0	∞	μs	
	$t_{W(SRCLKH)}$	Serial Clock Pulse Width, High. External Clock Mode	1.3	∞	1.3	∞	μs	
	$t_{W(SRCLKL)}$	Serial Clock Pulse Width, Low. External Clock Mode	1.3	∞	1.3	∞	μs	
	$t_{r(SRCLK)}$	Serial Clock Rise Time Internal Clock Mode		60		100	ns	0.8V –2.0V C_L = 100pf
	$t_{f(SRCLK)}$	Serial Clock Fall Time Internal Clock Mode		30		50	ns	2.4V –0.4V C_L = 100pf
SI	$t_{S(SI)}$	Setup Time To Rising Edge of SRCLK (SYNC Mode)	0		0		ns	
	$t_{H(SI)}$	Hold Time From Rising Edge of SRCLK (SYNC Mode)	2		2		μs	
SO	$t_{D(SO)}$	Data Output Delay From Falling Edge of SRCLK (SYNC Mode)		1190		1190	ns	

AC CHARACTERISTICS FOR MK38P73

(Signals brought out at socket)
T_A, V_{CC} within specified operating range.
I/O Power Dissipation ≤ 100mW (Note 2)

SYMBOL	PARAMETER	-00, -05		-10, -15		UNIT	CONDITION
		MIN	MAX	MIN	MAX		
t_{aas}*	Access time from Address A_{11}-A_{01} stable until data must be valid at D_7-D_0	650		650		ns	Φ = 2.0MHz

*See Table in Figure 13.

DC CHARACTERISTICS

T_A, V_{CC} within specified operating range
I/O Power Dissipation ≤ 100mW (Note 2)

SYM	PARAMETER	-00,-05		-10,-15		UNIT	DEVICE
		MIN	MAX	MIN	MAX		
I_{CC}	Average Power Supply Current		93.5		121	mA	MK3873/10 Outputs Open
			103		138	mA	MK3873/12 Outputs Open
			93.5		121	mA	MK3873/20 Outputs Open
			103		138	mA	MK3873/22 Outputs Open
			138		165	mA	MK38P73/02 No EPROM, Outputs Open
P_D	Power Dissipation		440		570	mW	MK3873/10 Outputs Open
			485		645	mW	MK3873/12 Outputs Open
			440		570	mW	MK3873/20 Outputs Open
			485		645	mW	MK3873/22 Outputs Open
			646		775	mW	MK38P73/02 No EPROM, Outputs Open

DC CHARACTERISTICS

T_A, V_{CC} within specified operating range
I/O Power Dissipation ≤ 100mW (Note 2)

SYM	PARAMETER	-00,-05		-10,-15		UNIT	CONDITIONS
		MIN	MAX	MIN	MAX		
V_{IHEX}	External Clock input high level	2.4	5.8	2.4	5.8	V	
V_{ILEX}	External Clock input low level	-.3	.6	-.3	.6	V	
I_{IHEX}	External Clock input high current		100		130	μA	$V_{IHEX}=V_{CC}$
I_{ILEX}	External Clock input low current		-100		-130	μA	$V_{ILEX}=V_{SS}$
$V_{IHI/O}$	I/O input high level	2.0	5.8	2.0	5.8	V	standard pull-up (1)
		2.0	13.2	2.0	13.2	V	open drain (1)
V_{IHR}	Input high level, $\overline{RESET}$	2.0	5.8	2.2	5.8	V	standard pull-up (1)
		2.0	13.2	2.2	13.2	V	No pull-up
V_{IHEI}	Input high level, EXT INT	2.0	5.8	2.2	5.8	V	standard pull-up (1)
		2.0	13.2	2.2	13.2	V	No pull-up
V_{IL}	I/O ports, $\overline{RESET}$[1], EXT INT[1] input low level	-.3	.8	-.3	0.7	V	(1)
I_{IL}	Input low current, standard pull-up pins		-1.6		-1.9	mA	$V_{IN}=0.4V$
I_L	Input leakage current, open drain pins $\overline{RESET}$ and EXT INT inputs With no pull-up resistor		+10 -5		+18 -8	μA μA	$V_{IN}=13.2V$ $V_{IN}=0.0V$
I_{OH}	Output high current, standard	-100		-89		μA	$V_{OH}=2.4V$
	pull-up pins	-30		-25		μA	$V_{OH}=3.9V$
I_{OHDD}	Output high current,	-100		-80		μA	$V_{OH}=2.4V$
	direct drive pins	-1.5	-8.5	-1.3	-11	mA mA	$V_{OH}=1.5V$ $V_{OH}=0.7V$
I_{OL}	Output low current, I/O ports	1.8		1.65		mA	$V_{OL}=0.4V$
I_{OHS}	$\overline{STROBE}$ Output High current	-300		-270		μA	$V_{OH}=2.4V$
I_{OLS}	$\overline{STROBE}$ output low current	5.0		4.5		mA	$V_{OL}=0.4V$

VIII

DC CHARACTERISTICS FOR MK38P73

(Signals brought out at socket)

T_A, V_{CC} within specifiec operating range, I/O Power Dissipation ≤ 100mW. (Note 2)

SYM	PARAMETER	-00, -05		-10, -15		UNIT	CONDITION
		MIN	MAX	MIN	MAX		
	Power Supply Current for EPROM		-185		-185	mA	
V_{IL}	Input Low Level Data bus in	-0.3	0.8	-0.3	0.7	V	
V_{IH}	Input High Level Data bus in	2.0	5.8	2.0	5.8	V	
I_{OH}	Output High Current	-100 -30		-90 -25		μA μA	V_{OH}=2.4V V_{OH}=3.9V
I_{OL}	Output Low Current	1.8		1.65		mA	V_{OL}=0.4V
I_{IL}	Input Leakage Current		10		10	μA	Data Bus in Float

DC CHARACTERISTICS FOR SERIAL PORT I/O PINS

T_A, V_{CC} within specified operating range

I/O Power Dissipation ≤ 100mW (Note 2)

SYM	PARAMETER	-00, -05		-10, -15		UNIT	TEST CONDITIONS
		MIN	MAX	MIN	MAX		
V_{IHS}	Input High for SI, SRCLK	2.0	5.8	2.0	5.8	V	
V_{ILS}	Input Low level for SI, SRCLK	-.3	.8	-.3	0.7	V	
I_{ILS}	Input low current for SI, SRCLK		-1.6		-1.9	mA	V_{IL} = 0.4V
I_{OHSO}	Output High Current SO	-100 -30		-90 -25		μA μA	V_{OH} = 2.4V V_{OL} = 3.9V
I_{OLSO}	Output Low Current SO	1.8		1.65		mA	V_{OL} = 0.4V
I_{OHSRC}	Output High Current SRCLK	-300		-270		μA	V_{OH} = 2.4V
I_{OLSRC}	Output Low Current SRCLK	5.0		4.5		mA	V_{OL} = 0.4V

1. $\overline{\text{RESET}}$ and EXT INT have internal Schmit triggers giving minimum .2V hysteresis.
2. Power dissipation for I/O pins is calculated by $\Sigma (V_{CC} - V_{IL})(I_{IL}) + \Sigma (V_{CC} - V_{OH})(I_{OH}) + \Sigma (V_{OL})(I_{OL})$

TIMER AC CHARACTERISTICS

Definitions:

Error = Indicated time value - actual time value

tpsc = t Φ x Prescale Value

Interval Timer Mode:

Single interval error, free running (Note 3) ..... ±6tΦ
Cumulative interval error, free running (Note 3) 0
Error between two Timer reads (Note 2) ..... ± (tpsc + tΦ
Start Timer to stop Timer error (Notes 1,4) ..... +tΦ to —(tpsc +tΦ)
Start Timer to read Timer error (Notes 1,2) ..... —5tΦ to —(tpsc + 7tΦ)
Start Timer to interrupt request error (Notes 1,3) ..... —2tΦ to —8tΦ)
Load Timer to stop Timer error (Note 1) ..... +tΦ to —(tpsc + 2tΦ)
Load Timer to read Timer error (Notes 1,2) ..... —5tΦ to —(tpsc + 8tΦ)
Load Timer to interrupt request error (Notes 1,3) ..... —2tΦ to —9tΦ)

Pulse Width Measurement Mode:

Measurement accuracy (Note 4)	+t Φ to —(tpsc +2t Φ)
Minimum pulse width of EXT INT pin	2tΦ

Event Counter Mode:

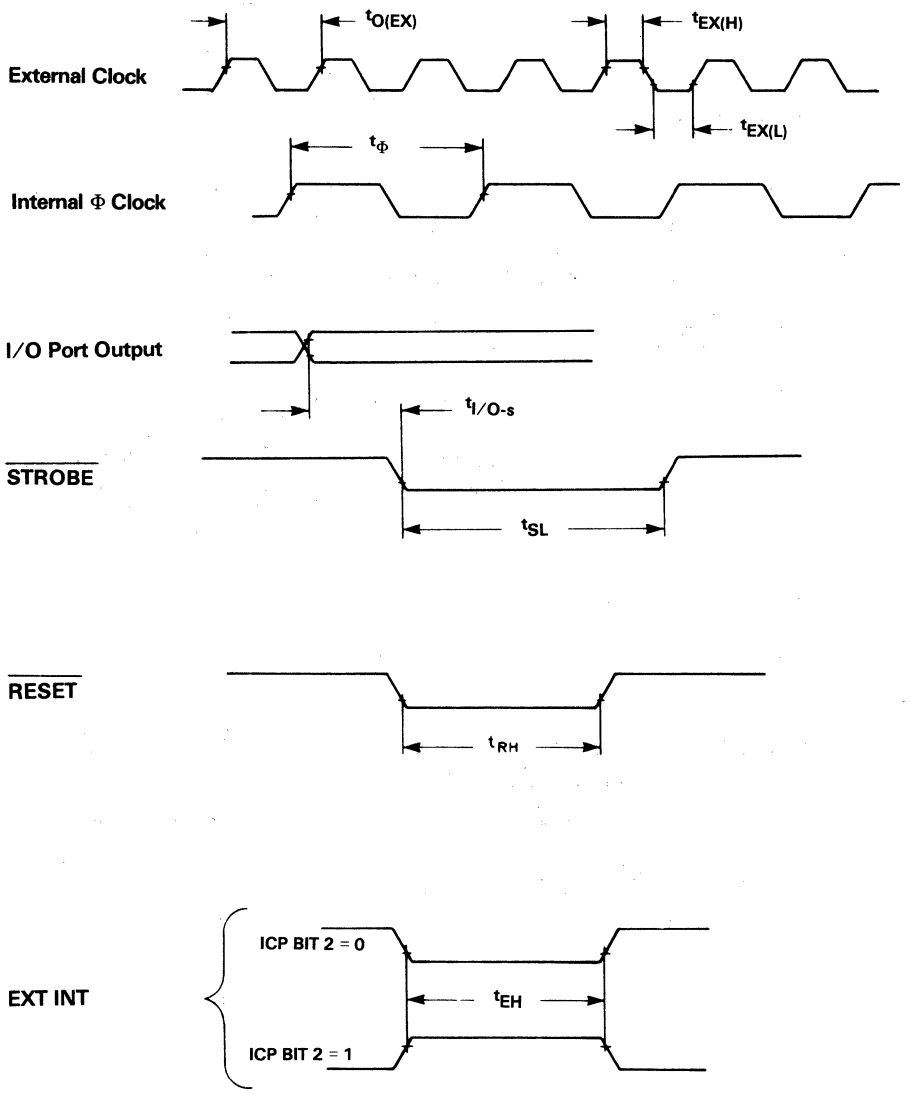
Minimum active time of EXT INT pin	2tΦ
Minimum inactive time of EXT INT pin	2tΦ

Notes:

1. All times which entail loading, starting, or stopping the Timer are referenced from the end of the last machine cycle of the OUT or OUTS instruction.
2. All times which entail reading the Timer are referenced from the end of the last machine cycle of the IN or INS instruction.
3. All times which entail the generation of an interrupt request are referenced from the start of the machine cycle in which the appropriate interrupt request latch is set. Additional time may elapse if the interrupt request occurs during a privileged or multicycle instruction.
4. Error may be cumulative if operation is repetitively performed.

AC TIMING DIAGRAM

Figure 20

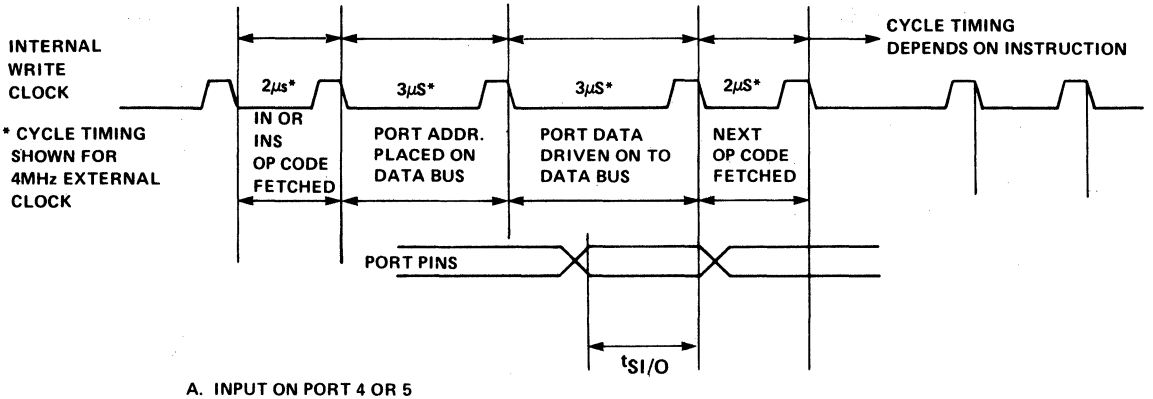


Note: All AC measurements are referenced to V_{IL} max., V_{IH} min., V_{OL} (.8v), or V_{OH} (2.0v).

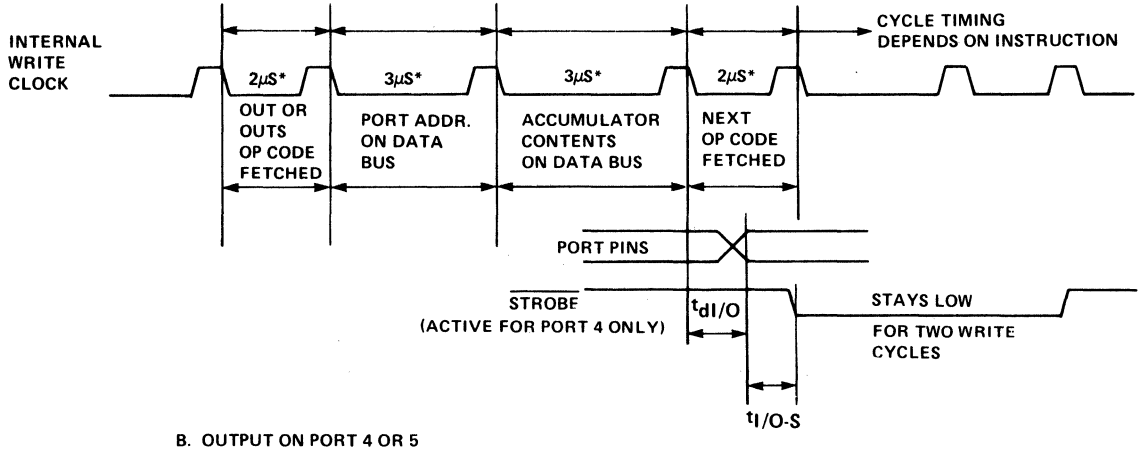
VIII

INPUT/OUTPUT AC TIMING

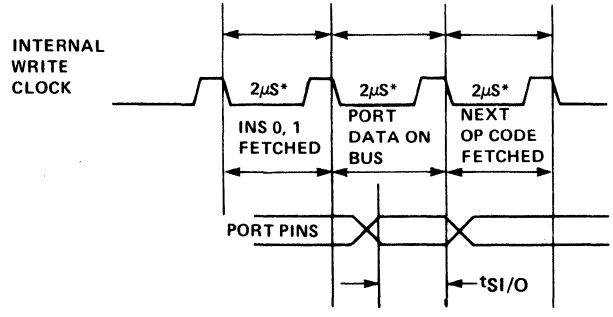
Figure 21



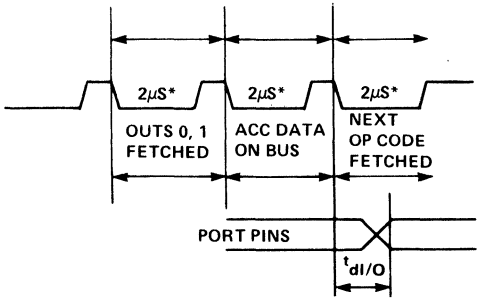
A. INPUT ON PORT 4 OR 5



B. OUTPUT ON PORT 4 OR 5



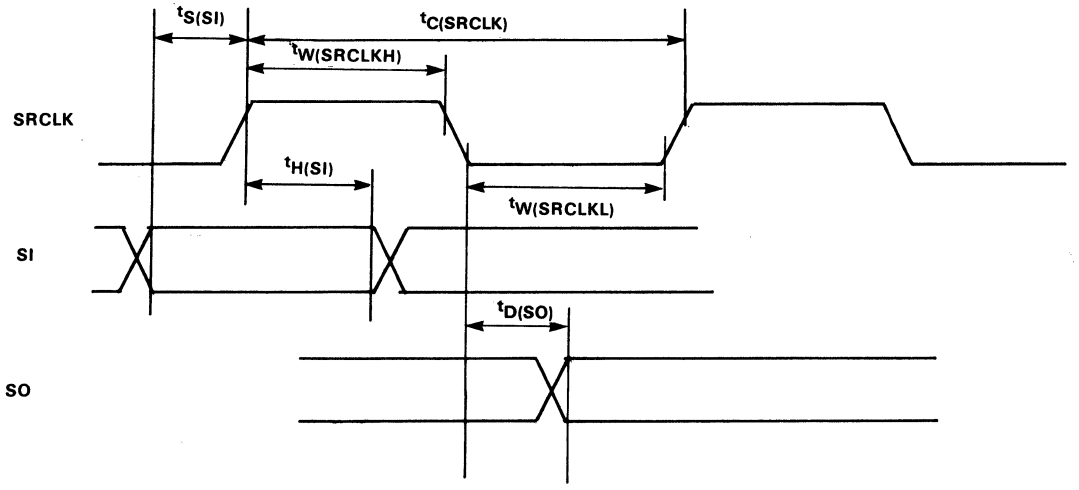
C. INPUT ON PORT 0 OR 1



D. OUTPUT ON PORT 0, 1

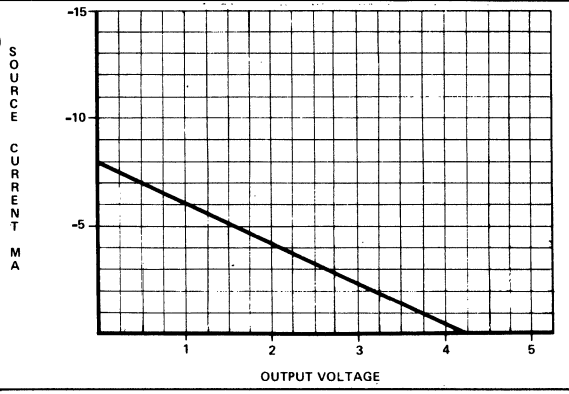
AC TIMING DIAGRAM FOR SERIAL I/O PINS.

Figure 22



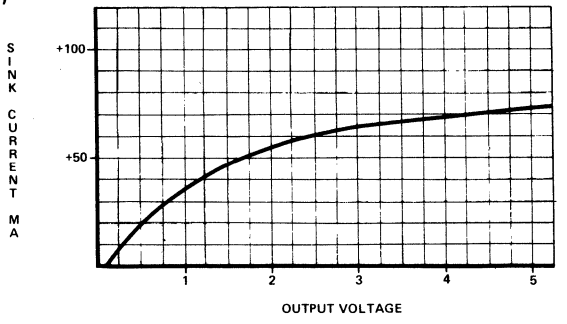
STROBE SOURCE CAPABILITY (TYPICAL AT V_{CC} = 5V, T_A = 25°C)

Figure 23



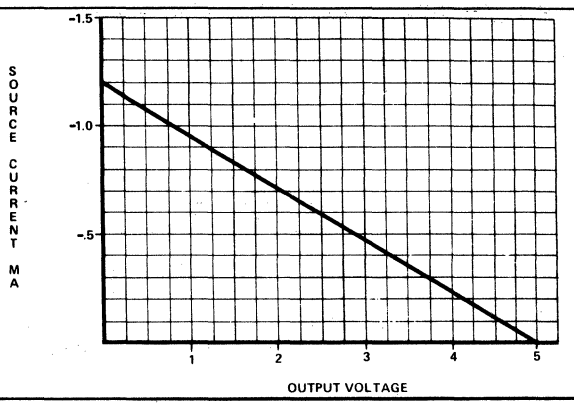
STROBE SINK CAPABILITY (TYPICAL AT V_{CC} = 5V, T_A = 25°C)

Figure 24

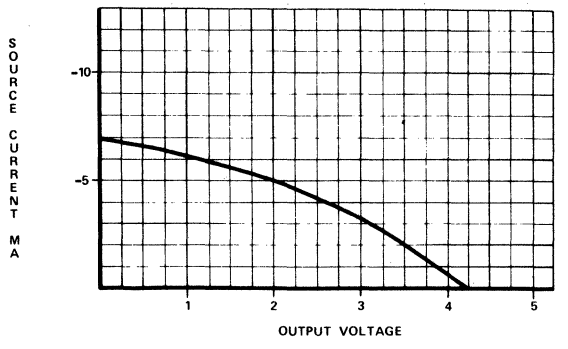


VIII

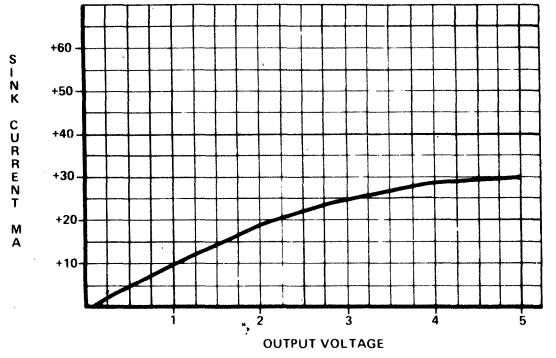
STANDARD I/O PORT SOURCE CAPABILITY
(TYPICAL AT V_{CC} = 5V, T_A = 25°C)
Figure 25



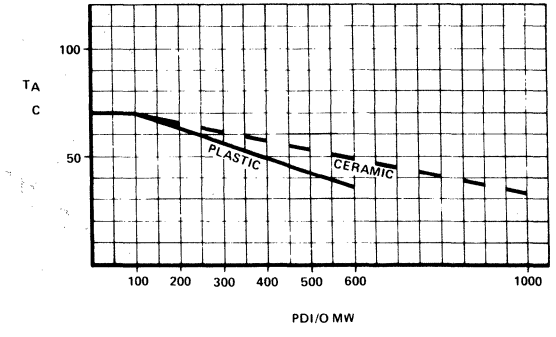
DIRECT DRIVE I/O PORT SOURCE CAPABILITY
(TYPICAL AT V_{CC} = 5V, T_A = 25°C)
Figure 26



I/O PORT SINK CAPABILITY
(TYPICAL AT V_{CC} = 5V, T_A = 25°C)
Figure 27



MAXIMUM OPERATING TEMPERATURE VS. I/O POWER DISSIPATION
Figure 28

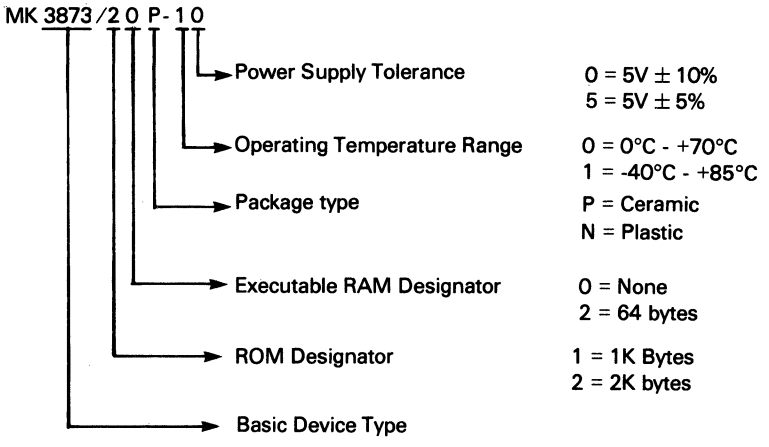


ORDERING INFORMATION

There are two types of part numbers for the 3870 family of devices. The generic part number describes the basic device type, the amount of ROM and Executable RAM, the desired package type, temperature range, and power supply tolerance. For each customer specific code, additional information defining I/O options and oscillator options will be combined with the information described in the generic part number to define a customer/code specific device order number.

GENERIC PART NUMBER

An example of the generic part number is shown below.

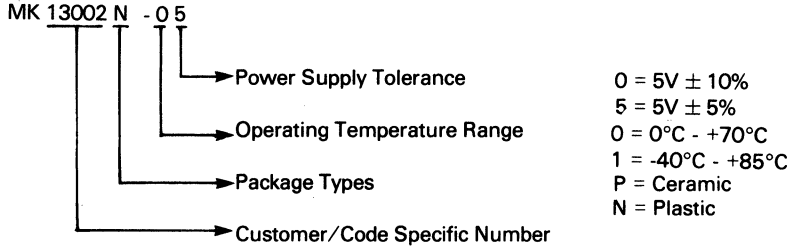


An example of the generic part number for the PPROM device is shown below.

MK38P73/02 R-05

DEVICE ORDER NUMBER

An example of the device order number is shown below.



The Customer/Code specific number defines the ROM bit pattern, I/O configuration, oscillator type, and generic part type to be used to satisfy the requirements of a particular customer purchase order. For further information on the ordering of mask ROM devices, the customer should refer to the 3870 Family Technical Manual.

MK3875 and MK38P75

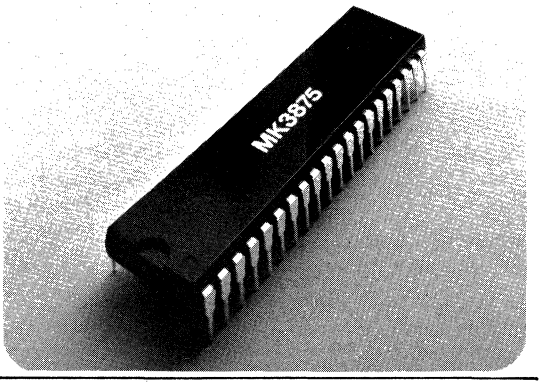
MK3875 FEATURES

- ☐ Available with 2K or 4K bytes of mask programmable ROM memory.
- ☐ 64 bytes scratchpad RAM
- ☐ 64 bytes of Executable RAM
- ☐ Standby feature for low power data retention of executable RAM including:
  Low standby power
  Low standby supply voltage
  No external components required to trickle charge battery.
- ☐ Software compatible with 3870 family
- ☐ 30 bits (4 ports) TTL compatible I/O
- ☐ Programmable binary Timer
  Interval Timer Mode
  Pulse Width Measurement Mode
  Event Counter Mode
- ☐ External Interrupt Input
- ☐ Crystal, LC, RC, or external time base options available
- ☐ Low power under normal operation (285 mW typ.)
- ☐ +5 volt main power supply
- ☐ Pinout compatible with 3870 family

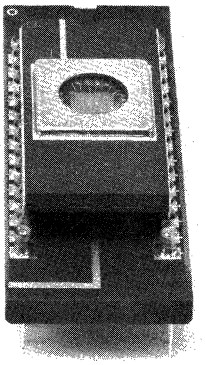
MK38P75 FEATURES

- ☐ EPROM version of MK3875
- ☐ Piggyback RPOM (P-PROM)™ package
- ☐ Accepts 24 pin or 28 pin EPROM memories
- ☐ Identical pinout as MK3875
- ☐ In-socket emulation of MK3875

MK3875

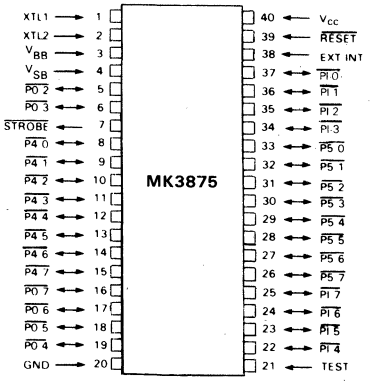


MK38P75

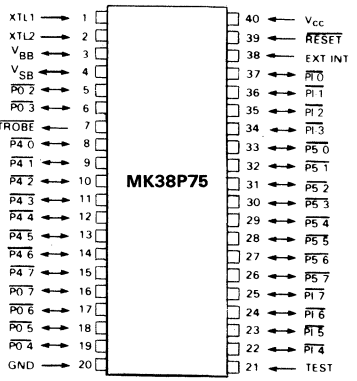


VIII

PIN CONNECTIONS
MK3875



PIN CONNECTIONS
MK38P75



PIN NAME	DESCRIPTION	TYPE
$\overline{P0\text{-}2}$ - $\overline{P0\text{-}7}$	I/O Port 0	Bidirectional
$\overline{P1\text{-}0}$ - $\overline{P1\text{-}7}$	I/O Port 1	Bidirectional
$\overline{P4\text{-}0}$ - $\overline{P4\text{-}7}$	I/O Port 4	Bidirectional
$\overline{P5\text{-}0}$ - $\overline{P5\text{-}7}$	I/O Port 5	Bidirectional
$\overline{STROBE}$	Ready Strobe	Output
EXT INT	External Interrupt	Input
$\overline{RESET}$	External Reset	Input
TEST	Test Line	Input
XTL 1, XTL 2	Time Base	Input
V_{CC}, GND	Power Supply Lines	Input
V_{SB}	Standby Power	Input
V_{BB}	Substrate Decoupling	Input

GENERAL DESCRIPTION

The MK3875 Single Chip Microcomputer offers a Low Power Standby mode of operation as an addition to the 3870 Family. The Low Power Standby feature provides a means of retaining data in the executable RAM on the MK3875 while the main power supply line (V_{CC}) is at 0 volts and the rest of the MK3875 microcomputer is shut down. The executable RAM is powered from an auxiliary power supply input (V_{SB}) while operating in the Lower Power Standby mode. When V_{SB} is maintained at or above its minimum level, data is retained in the executable RAM memory with a very low power dissipation.

The MK3875 retains commonality with the rest of the industry standard 3870 family of single chip microcomputers. It has the same central processing unit, oscillator and clock circuits, and 64 byte scratchpad memory array. Also, the 3870's sophisticated programmable binary timer is included which provides three different operating modes. Two pins on the MK3875 are dedicated to the Low Power Standby mode and are designated as V_{SB} and V_{BB}. The $\overline{RESET}$ line serves to reset the MK3875 and place it in a protected state so that the contents of the Executable RAM will remain unchanged when V_{CC} is being powered down to 0 volts. All other pins on the MK3875 are identical in function to corresponding pins on the MK3870, so that pin compatibility is maintained. The MK3875 executes the entire 3870 instruction set.

The MK38P75 microcomputer is the PROM based version of the MK3875. It is called the piggyback PROM (P-PROM)™ because of its packaging concept. This concept allows a standard 24-pin or 28-pin EPROM to be mounted directly on top of the microcomputer itself. The EPROM can be removed and reprogrammed as required with a standard PROM programmer. The MK38P75 retains the pinout and architectural features as other members of the 3870 family. The MK38P75 is discussed in more detail in a later section.

FUNCTIONAL PIN DESCRIPTION

$\overline{P0\text{-}2}$ - $\overline{P0\text{-}7}$, $\overline{P1\text{-}0}$ - $\overline{P1\text{-}7}$, $\overline{P4\text{-}0}$ - $\overline{P4\text{-}7}$, and $\overline{P5\text{-}0}$ - $\overline{P5\text{-}7}$ are 30 lines which can be individually used as either TTL compatible inputs or as latched outputs.

$\overline{STROBE}$ is a ready strobe associated with I/O Port 4. This pin, which is normally high, provides a single low pulse after valid data are present on the $\overline{P4\text{-}0}$ - $\overline{P4\text{-}7}$ pins during an output instruction.

$\overline{RESET}$ - may be used to externally reset the MK3875. When pulled low, the Mk3875 will reset. When allowed to go high the MK3875 will begin program execution at program location H '000'. Additionally, when $\overline{RESET}$ is brought low all accesses of the executable RAM are prevented and the RAM is placed in a protected state for powering down V_{CC} without loss of data.

EXT INT is the external interrupt input. Its active state is software programmable. This input is also used in conjunction with the timer for pulse width measurement and event counting.

XTL 1 and XTL 2 are the time base inputs to which a crystal (2 to 4 MHz), LC network, RC network, or an external single-phase clock may be connected. The time base network must be specified when ordering an MK3875.

TEST is an input used only in testing the MK3875. For normal circuit function this pin may be left unconnected but it is recommended that TEST be grounded.

V_{CC} is the power supply input +5 V.

V_{SB} is the RAM standby power supply input.

V_{BB} is the substrate decoupling pin. A .01 micro-Farad capacitor is required which is tied between V_{BB} and GND.

MK3875 ARCHITECTURE

The basic functional elements of the mask ROM MK3875 single chip microcomputer are shown in the block diagram in Figure 1. A programming model is shown in Figure 2. Much of the Mk3875 architecture is identical with the rest of the devices in the 3870 family. The significant features of the MK3875 are discussed in the following sections. The user is referred to the 3870 Family Technical Manual for a thorough discussion of the architecture, instruction set, and other features which are common to the 3870 family.

MAIN MEMORY

The main memory section on the MK3875 consists of a combination of ROM and executable RAM.

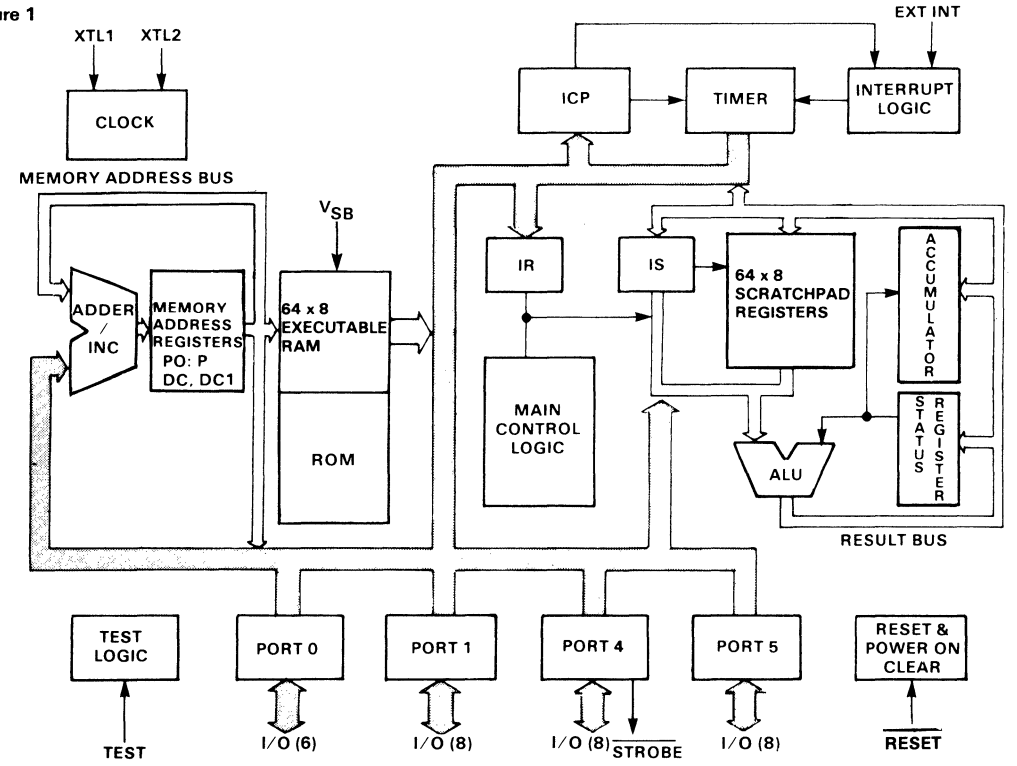
There are four registers associated with the main memory section. These are the Program Counter (PO), the Stack Register (P), the Data Counter (DC) and the Auxiliary Data Counter (DC1). The Program Counter is used to address instructions during program execution. P is used to save the contents of PO during an interrupt or subroutine call. Thus, P contains the return address at which processing is to resume upon completion of the subroutine or the interrupt routine.

The Data Counter (DC) is used to address data tables. This register is auto-incrementing. Of the two data counters only DC can access the memory. However, the XDC instruction allows DC and DC1 to be exchanged.

The length of the PO, P, DC, and DC1 registers for all MK3875 devices is 12 bits. Figure 3 shows the amounts of

MK3875 BLOCK DIAGRAM

Figure 1



ROM and Executable RAM for each device in the MK3875 family.

EXECUTABLE RAM

The upper bytes of the total address space in all MK3875 devices are RAM memory. As with the ROM memory, the RAM may be addressed by the PO and DC address registers. The executable RAM may be accessed by all 3870 instructions which address main memory indirectly through the Data Counter (DC) register. Additionally, the MK3875 may execute an instruction sequence which resides in the executable RAM. Note that this sequence cannot be done with the scratchpad RAM memory, which is the reason the term "executable RAM" is given to this additional memory. The contents of the executable RAM memory are preserved when the Low Power Standby mode is in operation.

I/O PORTS

The MK3875 provides 30 bits of bidirectional parallel I/O. These lines are addressed as Ports 0, 1, 4 and 5. In addition, the Interrupt Control Port is addressed as Port 6 and the binary timer is addressed as Port 7. The programming of Ports 6 and 7 and the bidirectional I/O pins are covered in the 3870 Family Technical Manual.

Since two pins are dedicated to serve the Standby Power mode (V_{SB}), port 0 has only the upper 6 bits, $\overline{P0\text{-}2}$ - $\overline{P0\text{-}7}$, available for use as general purpose I/O pins. Ports 1, 4, and 5 are all a full 8 bits wide.

The schematic of an I/O pin and available output drive options are shown in Figure 4.

An output ready strobe is associated with Port 4. This flag may be used to signal a peripheral device that the MK3875 has just completed an output of new data to Port 4. The strobe provides a single low pulse shortly after the output operation is completely finished, so either edge may be used to signal the peripheral. $\overline{\text{STROBE}}$ may be used as an input strobe simply by doing a dummy output of H '00' to Port 4 after completing the input operation.

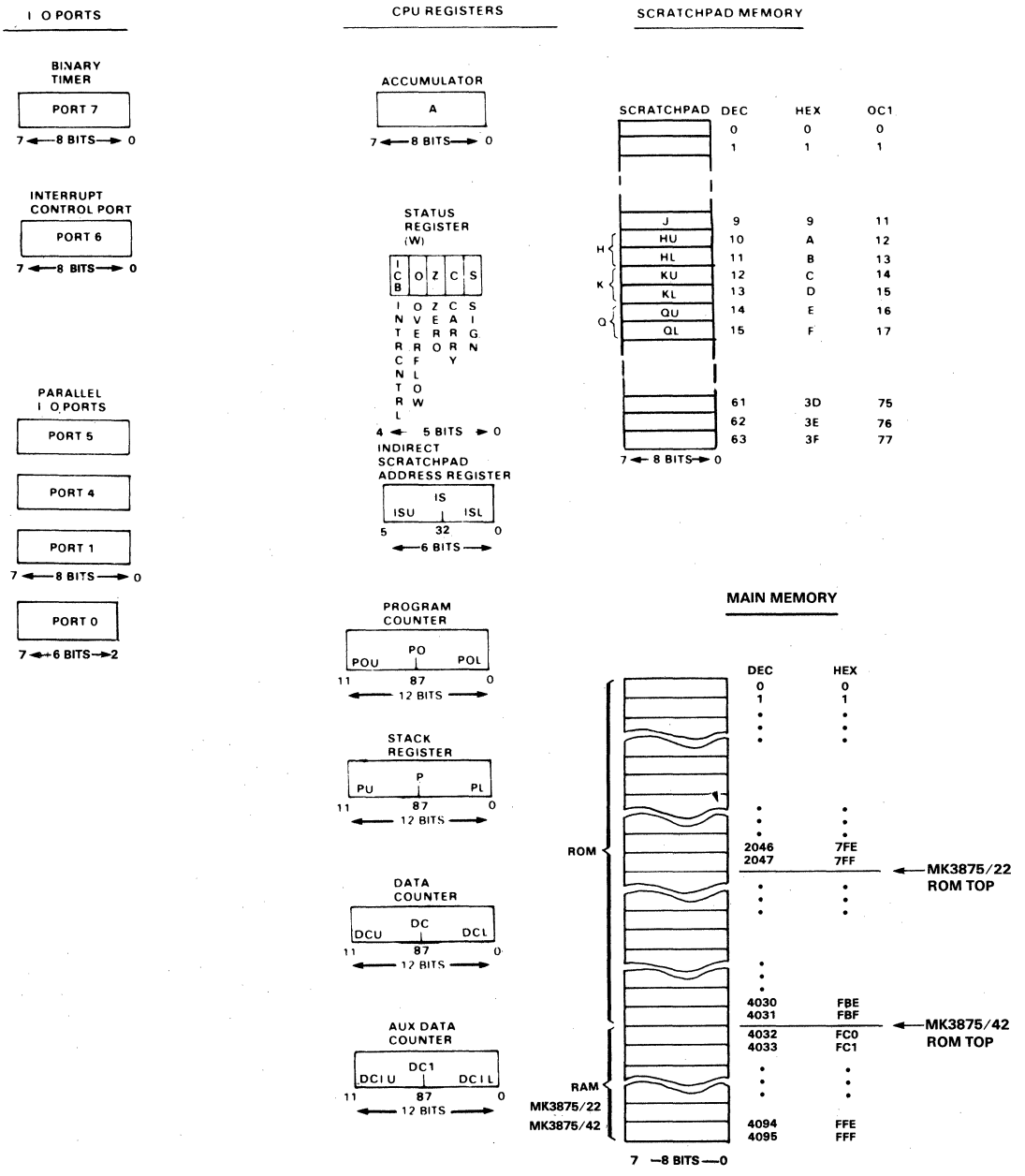
STANDBY POWER MODE

On the MK3875, the contents of the on-chip executable RAM can be saved when the Standby Power mode is operative. The Standby Power mode allows the MK3875's main power supply to drop all way down to 0 volts while the on-chip executable RAM is powered from the auxiliary low power supply input, V_{SB}. Thus, key variables may be maintained within the MK3875 executable RAM during the time that the rest of the microcomputer is powered down.

On the MK3875, two of the pins which are used as bidirectional port pins on the MK3870 are used for the Standby Power feature. Port 0, Bit 0 (PO-0), remains readable and writeable although it is not connected to a package pin. The logic level being applied to the auxiliary

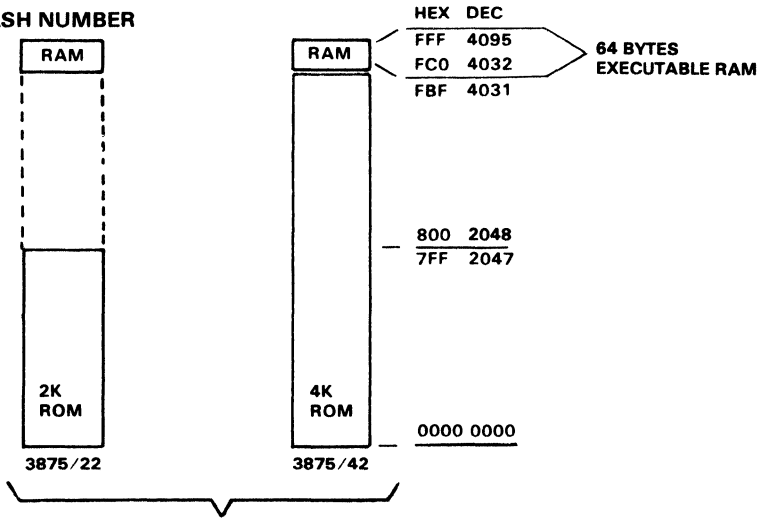
3875 PROGRAMMABLE REGISTERS, PORTS AND MEMORY MAP

Figure 2



MK3875 MAIN MEMORY SIZES AND TYPES BY SLASH NUMBER

Figure 3



All devices contain 64 bytes of scratchpad RAM

Data derived from addressing any locations other than within the specified ROM or RAM space is not tested nor is it guaranteed. Users should refrain from entering this area of the memory map.

Device	Scratchpad RAM Size (Decimal)	Address Register Size (P0,P,DC,DC1)	ROM Size (Decimal)	Executable RAM Size
MK3875/22	64 bytes	12 bits	2048 bytes	64 bytes
MK3875/42	64 bytes	12 bits	4032 bytes	64 bytes

VIII

power supply input (V_{SB}) can be read at Port 0, Bit 1 ($\overline{PO\text{-}1}$). Writing to $\overline{PO\text{-}1}$ has no effect.

A capacitor (.01 microfarads) must be connected between pin 3 (V_{BB}) and ground. V_{BB} is bonded directly to the substrate of the MK3875. The purpose of the capacitor is to decouple noise on the substrate of the circuit when V_{CC} is switched on and off.

It is recommended that Nickel Cadmium batteries (typical voltage of 3 series cells = 3.6V) be used for standby power, since the MK3875 can automatically trickle charge the three NiCads. If more than three cells in series are used, the charging circuit must be provided outside the MK3875.

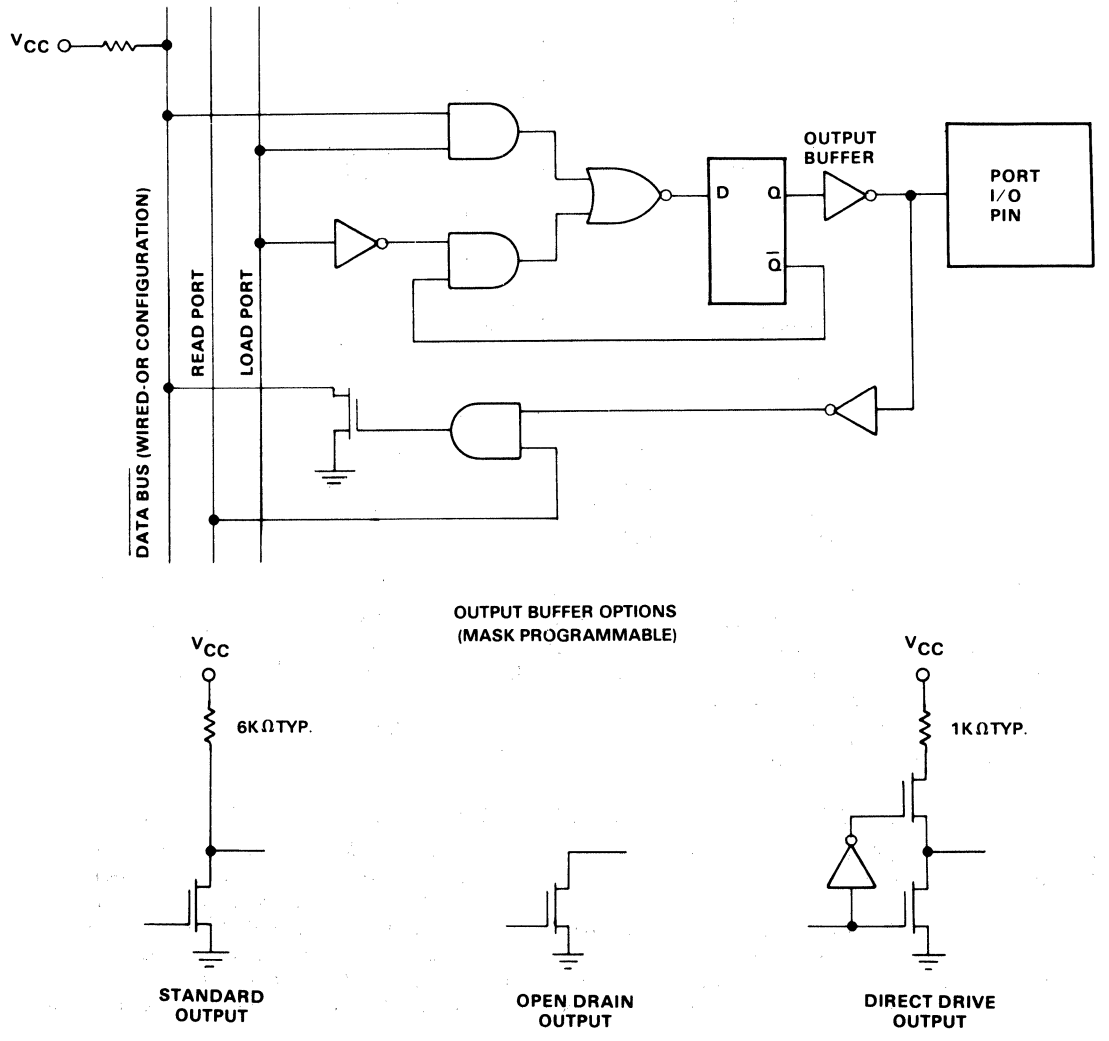
Whenever $\overline{RESET}$ is brought low, the executable RAM is placed in a protected state. Also the RAM is switched from V_{CC} power to the V_{SB} power. When powering down, it may be desirable to interrupt the MK3875 when an impending power down condition is detected, so that the necessary data can be saved before V_{CC} falls below the minimum level. After the save is completed, $\overline{RESET}$ can fall, which prevents any further access of the RAM. The timing for this power down sequence is illustrated in Figure 5A.

A second power down sequence is illustrated in Figure 5B, and may be used if a special save data routine is not needed. The EXT INT line need not be used. Note that for both cases shown in Figures 5A and 5B, $\overline{RESET}$ must be low before V_{CC} drops below the minimum specified operating voltage for the MK3875. This is to ensure that the contents of the executable RAM are not altered during the power down sequence.

There may be a set of variables stored in the RAM memory which is continually updated during the tme when the MK3875 is in its normal operating mode. If a particular variable occupies more than one byte of RAM, there can be a problem if a reset occurs in response to an impending power down condition during the time that the multi-byte variable was being modified. If such a reset occurs, then only part of the variable may contain the updated value, while the rest contains the old value. An example of this case would be when a double precision (2 byte) binary number is being saved in the executable RAM. Suppose that a new value of the number has been calculated in the program, and that this new value is to replace the old value contained in the executable RAM; note that a reset could occur just after the program wrote one byte of the new value

I/O PIN CONCEPTUAL DIAGRAM WITH OUTPUT BUFFER OPTIONS

Figure 4



Ports 0 and 1 are Standard Output type only.

Ports 4 and 5 may both be any of the three output options (mask programmable bit by bit)

The $\overline{\text{STROBE}}$ output is always configured similar to a Direct Drive Output except that it is capable of driving 3 TTL loads.

$\overline{\text{RESET}}$ and EXT INT may have standard 6KΩ (typical) pull-up or may have no pull-up (mask programmable). These two inputs have Schmitt trigger inputs with a minimum of 0.2 volts of hysteresis.

$\overline{\text{RESET}}$ and EXT INT do not have internal pull up on the MK38P75.

into the RAM. When power is restored following the Standby Power mode, the double precision variable would contain an erroneous value.

This problem can be avoided if the external interrupt is used to signal the MK3875 of an impending power down condition. The user's system should be designed so that the MK3875 can properly save all variables between the time that the external interrupt occurs and $\overline{\text{RESET}}$ falls. If multi-byte variables must be saved during the Standby Power mode and it is not desirable to use the external interrupt in the manner described above, then each byte of a multi-byte variable may be kept with an associated flag. The method of updating a two byte variable would be as follows:

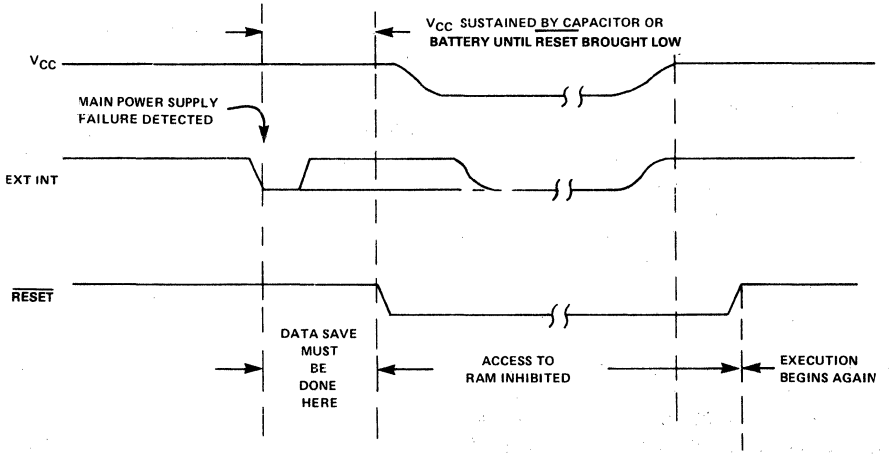
- Clear Flag Word 1
- Update Byte 1
- Set Flag Word 1
- Clear Flag Word 2
- Update Byte 2
- Set Flag Word 2

Now if $\overline{\text{RESET}}$ goes low during the update of a byte of a variable, the flag word associated with that byte of data will be reset. Any byte of the variable where the flag word is "set" is a good byte of data. While this method significantly encumbers the data storage process, it eliminates the need for a power fail interrupt which both reduces external circuitry and leaves the external interrupt pin completely free for other use.

Often it is necessary to distinguish between an initial power-on condition wherein there is no valid data stored in the RAM (or where V_{SB} has dropped below the minimum required stand-by level) and a re-application of power wherein valid RAM data has been maintained during the power outage. One method of distinguishing between these two conditions is to reserve several memory locations for key words and checksums. When V_{CC} is applied and processor operation begins, these locations can be checked for proper contents. However, this method may not be perfectly accurate as those locations holding key codes may be maintained even though V_{SB} drops below its minimum required level while other RAM locations may lose data, or they could power up with the exact data required to match the key codes. Also a checksum may be matched on occasion even though RAM data has been corrupted. The accuracy of this method is improved by increasing the number of memory locations used and the variety of key codes and or checksums used.

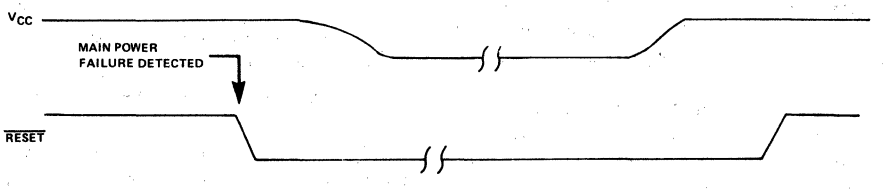
SAVE ROUTINE REQUIRED, $V_{SB} > 3.2$ VOLTS

Figure 5a



NO SAVE ROUTINE REQUIRED, $V_{SB} > 3.2$ VOLTS

Figure 5b



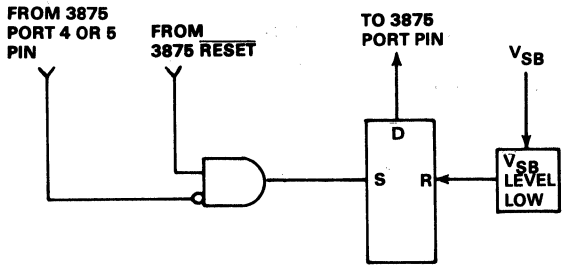
VIII

A more reliable method is the external V_{SB} flip-flop. The flip-flop is designed to power up in a known first state and hold that first state until forced into a second state. As long as V_{SB} is above the minimum operating level, the flip-flop can hold the second state, but, if V_{SB} drops below the minimum level, the flip-flop will flip back to the first state. Thus when power is initially applied or if V_{SB} drops below the minimum level during a V_{CC} outage, the flip-flop will be in the first state. The flip-flop output can be read through a port pin by the processor when processor operation begins to determine whether the RAM data is valid (second state) or invalid (first state). If the flip-flop is found to be in the first state it can be forced to the second state by the processor. If it holds the second state, V_{SB} is above the minimum level (batteries are charged).

A conceptual diagram is shown in Figure 6.

CONCEPTUAL DIAGRAM

Figure 6



MK38P75 GENERAL DESCRIPTION

The MK38P75 is the EPROM version of the MK3875. It retains an identical pinout with the MK3875, which is documented in the section of this data sheet entitled "FUNCTIONAL PIN DESCRIPTION". The MK38P75 is housed in the "R" package which incorporates a 28-pin socket located directly on top of the package. A number of standard EPROMs may be plugged into this socket.

The MK38P75 can act as an emulator for the purpose of verification of user code prior to the ordering of mask ROM MK3875 devices. Thus, the MK38P75 eliminates the need for emulator board products. In addition, several MK38P75s can be used in prototype systems in order to test design concepts in field service before commiting to high-volume production with mask ROM MK3875s. The compact size of the MK38P75/EPROM combination allows the packaging of such prototype systems to be the same as that used in production. Finally, in low-volume applications, the MK38P75 can be used as the actual production device.

Most of the material which has been presented for the MK3875 in this document applies to the MK38P75. This includes the description of the pin configuration, architecture, and programming mode. Additional information is presented in the following sections.

MK38P75 I/O PORTS

The MK38P75 is offered with two types of output buffer options on Ports 4 and 5. These are the open drain output buffer and the standard output buffer which are pictured in Figure 4. The open drain version of the MK38P75 is provided so that user-selected open drain port pins on the MK3875 can be emulated prior to ordering those mask ROM devices. Figure 9 lists which version(s) of the MK38P75 has open drain output buffers and which has standard output buffers in parentheses following the specified MK38P75 part ordering number (MK9XXXX).

MK38P75 MAIN MEMORY

As can be seen from the block diagram in Figure 7, the MK38P75 contains executable RAM in the main memory map. The MK38P75 contains no on-chip ROM. Instead, the memory address lines are brought out to the 28-pin socket located directly on top of the 40-pin package, so the external ERPOM memory is addressed as main memory.

There is one memory version of the MK38P75 and it is designated as the MK38P75/02. The MK38P75/02 contains 64 bytes of on-chip executable RAM. The MK38P75/02 can emulate the following devices.

MK3875/22
MK3875/42

The MK38P75/02 cannot exactly emulate the MK3875/40 because of the 64 bytes of executable RAM in the upper ROM space of the MK3875/40.

Addressing of main memory on the MK38P75 is accomplished in the same way as it is for the MK3875. See Figure 8 for main memory addresses and for address register size in the MK38P75.

MK38P75 EPROM SOCKET

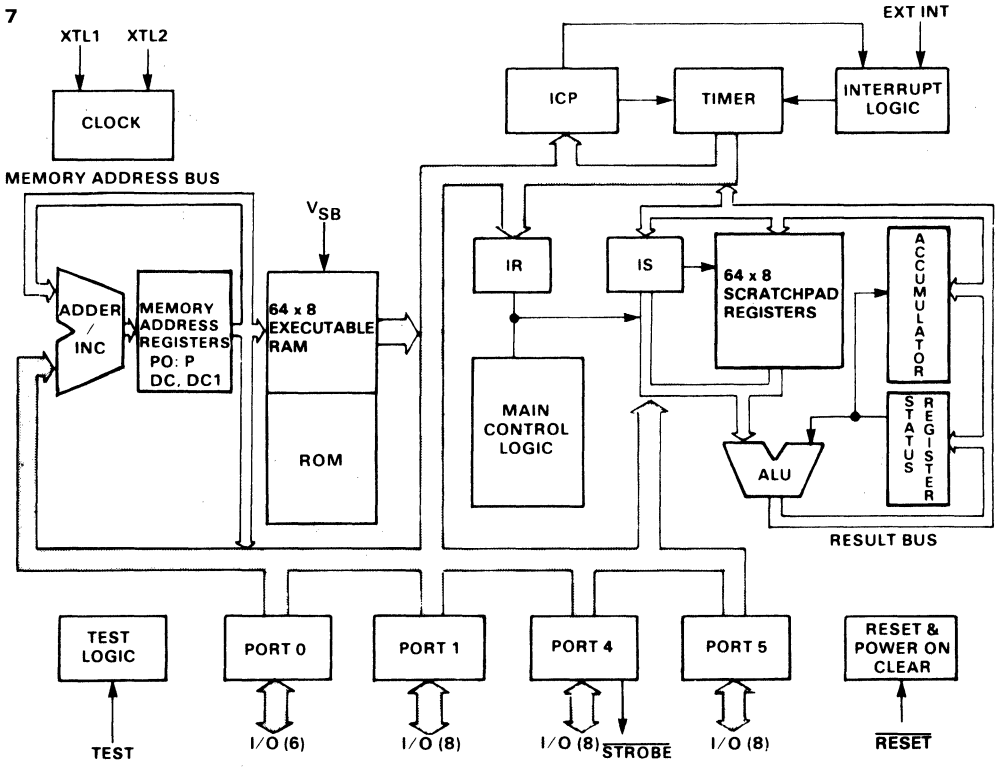
A 28-pin ERPOM socket is located on top of the MK38P75 "R" package. The socket and compatible ERPOM memories are shown in Figure 9. When 24-pin memories are used in the 28-pin socket, they should be inserted so that pin 1 of the memory device is plugged into pin 3 of the socket (the 24-pin memory should be lower justified in the 28-pin socket).

The 28-pin socket has been provided to allow use of both 24-pin and 28-pin memory devices. Minor pin-out differences in the memory devices must be accommodated by providing different versions of the MK38P75.

Initially, the MK38P75 that is compatible with the MK2716 is available. The MK38P75 designed to accommodate the 28-pin memory devices will be available at a later date.

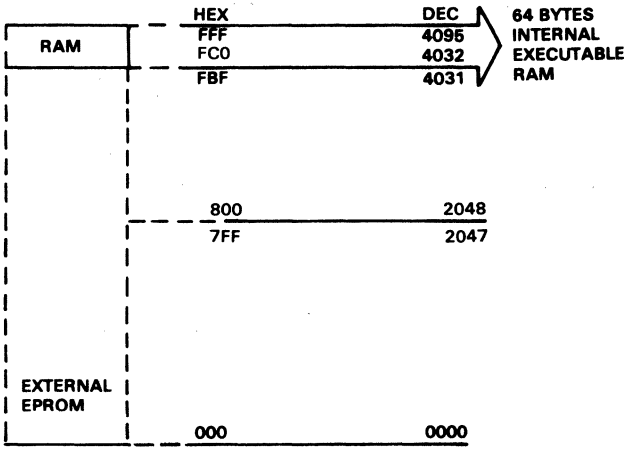
MK38P75 BLOCK DIAGRAM

Figure 7



MK38P75 MAIN MEMORY MAP

Figure 8



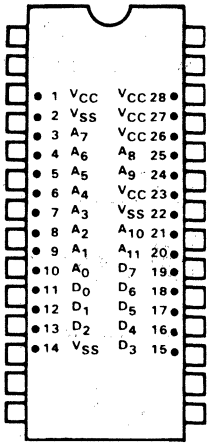
MK38P75/02

Device	Scratchpad RAM Size (Decimal)	Address Register Size P0, P, DC, DC1)	ROM Size (Decimal)	Executable RAM Size
MK38P73/02 97310	64 bytes	12 bits	0 bytes	64 bytes

VIII

MK38P75 "R" PACKAGE SOCKET PINOUT

Figure 9



MK97413 (Open Drain Outputs) Compatible Memories
2758
MK2716
2516
2532

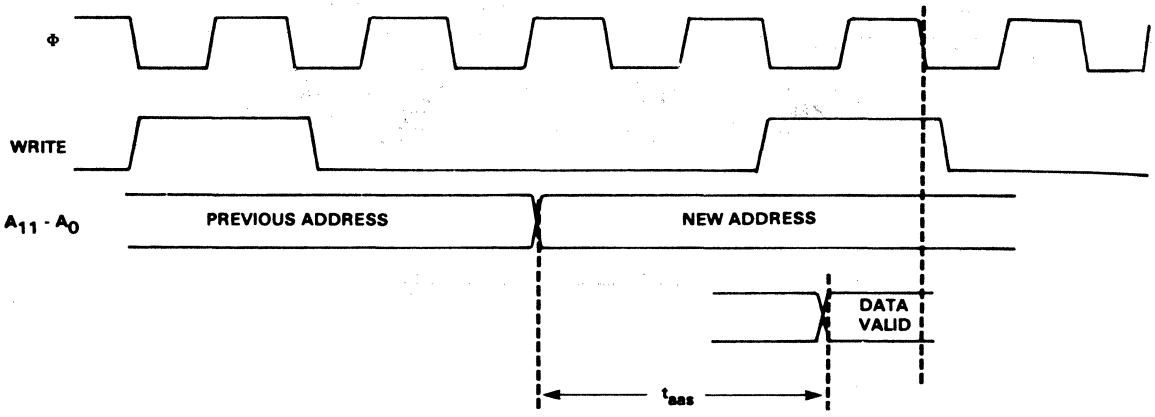
MK97403 (Standard Outputs) Compatible Memories
2758
MK2716
2516
2532

MEMORY ACCESS TIMING

A timing diagram depicting the memory access timing of the MK38P75 is shown in the next table. The Φ clock signal is derived internally in the MK38P75 by dividing the time base frequency by two and is used to establish all timing frequencies. The WRITE signal is another internal signal to the MK38P75 which corresponds to a machine cycle, during which time a memory access may be performed. Each machine cycle is either 4 Φ clock periods or 6 Φ clock periods long. These machine cycles are termed short cycles and long cycles, respectively. The worst case memory cycle is the short cycle, during which time an op code fetch is performed. This is the cycle which is pictured in the timing diagram. After a delay from the falling edge of the WRITE clock, the address lines become stable. Data must be valid at the data out lines of the PROM for a setup time prior to the next falling edge of the WRITE pulse. The total access time available for the MK38P75 version is shown as t_{aas} or the time when address is stable until data must be valid on the data bus lines. The equation for calculating available memory access time along with some calculated access times based on the listed time base frequencies is shown in the following table.

MEMORY ACCESS SHORT CYCLE OP CODE FETCH MK38P75

Figure 10



Φ Signal is internal to the MK38P75

$$t_{aas} = \frac{6}{\text{time base freq.}} - 850 \text{ ns}$$

(FROM ADDRESS STABLE)

	4 MHz	3.5 MHz	3 MHz	2.5 MHz	2 MHz
ACCESS TIME	650 ns	825 ns	1.15 μs	1.55 μs	2.15 μs

3875 TIME BASE OPTIONS

The 3875 contains an on-chip oscillator circuit which provides an internal clock. The frequency of the oscillator circuit is set from the external time base network. The time base for the 3875 may originate from one of four sources:

1) Crystal
2) LC Network
3) RC Network
4) External Clock

The type of network which is to be used with the mask ROM MK3875 must be specified at the time when mask ROM devices are ordered. However, the MK38P75 may operate with any of the four configurations so that it may emulate any configuration used with a mask ROM device.

The specifications for the four configurations are given in the following text. There is an internal 26 pF capacitor between XTL 1 and GND and an internal 26 pF capacitor between XTL 2 and GND. Thus, external capacitors are not necessarily required. In all external clock modes the external time base frequently is divided by two to form the internal PHI clock.

CRYSTAL SELECTION

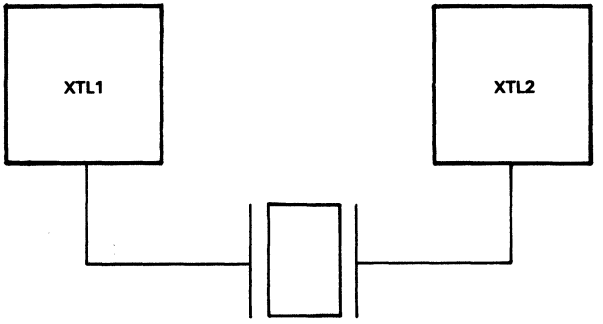
The use of a crystal as the time base is highly recommended as the frequency stability and reproducability from system to system is unsurpassed. The 3875 has an internal divide by two to allow the use of inexpensive and widely available TV Color Burst Crystals (3.58 MHz). Figure 12 lists the required crystal parameters for use with the 3875. The Crystal Mode time base configuration is shown in Figure 11.

Through careful buffering of the XTL1 pin it may be possible to amplify this waveform and distribute it to other devices. However, Mostek recommends that a separate active device (such as a 7400 series TTL gate) be used to oscillate the crystal and that the waveform from that oscillator be buffered and supplied to all devices, including the 3875, in the event that a single crystal is to provide the time base for more than just a single 3875.

While a ceramic resonator may work with the 3875 crystal oscillator, it was not designed specifically to support the use of this component. Thus, Mostek does not support the use of a ceramic resonator either through proper testing, parametric specification, or applications support.

CRYSTAL MODE CONNECTION

Figure 11



CRYSTAL PARAMETERS

Figure 12

a) Parallel resonance, fundamental mode AT-Cut
b) Shunt capacitance (C_0) = 7 pf max.
c) Series resistance (R_S) = See table
d) Holder = See table below.

Frequency	Series Resistance	Holder
f = 2-2.7 MHz	Rs = 300 ohms max	HC-6 HC-33
f = 2.8-4 MHz	Rs = 150 ohms max	HC-6 HC-18* HC-25* HC-33

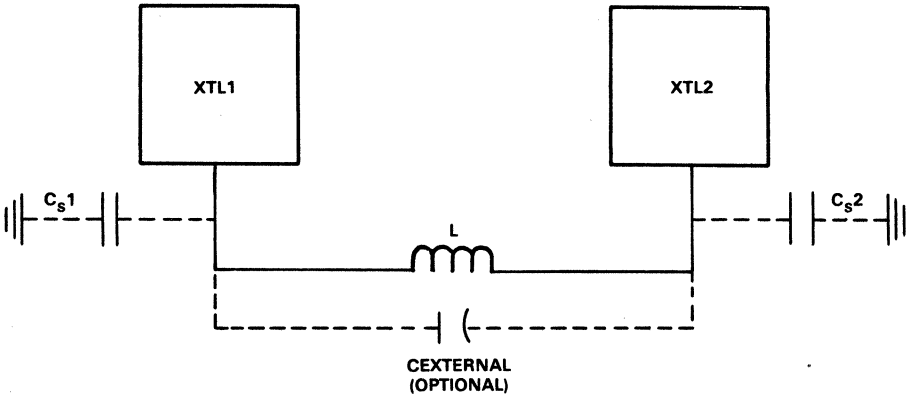
*This holder may not be available at frequencies near the lower end of this range.

LC NETWORK

The LC time base configuration can be used to provide a less expensive time base for the 3875 than can be provided with a crystal. However, the LC configuration is much less accurate than is the crystal configuration. The LC time base configuration is shown in Figure 13. Also shown in the figure are the specified parameters for the LC components, along with the formula for calculating the resulting time base frequency. The minimum value of the inductor which is required for proper operation of the LC time base network is 0.1 millihenries. The inductor must have a Q factor which is no less than 40. The value of C is derived from C external, the internal capacitance of the 3875, C_{XTL}, and the stray capacitances, C_{S1} and C_{S2}. C_{XTL} is the at XTL1 and capacitance looking into the internal two port network XTL2. C_{XTL} is listed under the "Capacitance" section of the Electrical Specifications. C_{S1} and C_{S2} are stray capacitances from XTL1 to ground and from XTL2 to ground, respectively. C external should also include the stray shunt capacitance across the inductor. This is typically in the 3 to 5 pf range and significant error can result if it is not included in the frequency calculation.

LC MODE CONNECTION

Figure 13

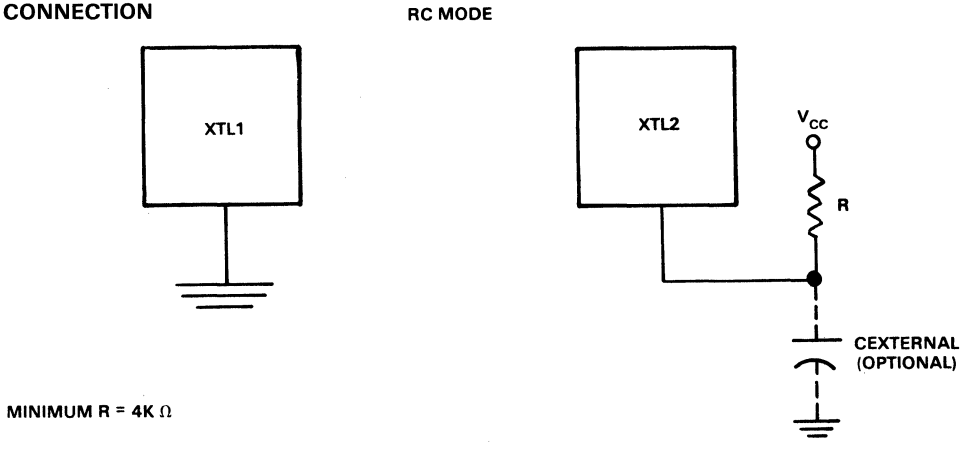


Variation in time base frequency with the LC network can arise from one of four sources: 1) Variation in the value of the inductor. 2) Variation in the value of the external capacitor. 3) Variation in the value of the internal capacitance of the 3875 at XTL1 and XTL2, and 4) Variation in the amount of stray capacitance which exists in the circuit. Therefore, the actual frequency which is generated by the LC circuit is within a range of possible frequencies, where the range of frequencies is determined by the worst case variation in circuit parameters. The designer must select component values such that the range of possible frequencies with the LC mode does not go outside of the specified operating frequency range for the 3875.

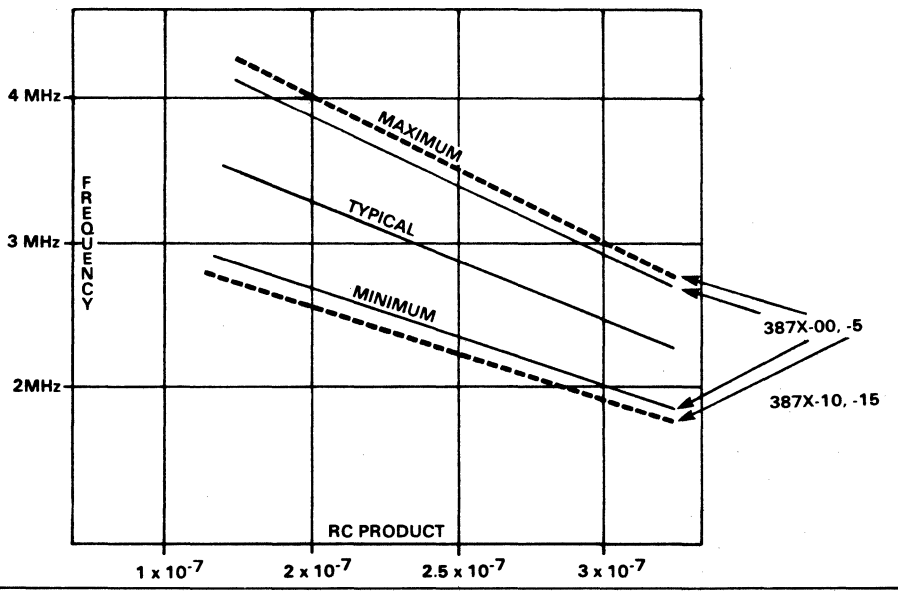
RC CLOCK CONFIGURATION

The time base for the 3875 may be provided from an RC network tied to the XTL2 pin, when XTL1 is grounded. A schematic picturing the RC clock configuration is shown in Figure 14. The RC time base configuration is intended to provide an inexpensive time base source for applications in which timing is not critical. Some users have elected to tune each unit using a variable resistor or external capacitor thus reducing the variation in frequency. However, for increased time base accuracy Mostek recommends the use of the Crystal or LC time base configuration. Figure 15 illustrates a curve which gives the resulting operating frequency for a particular RC value. The x-axis represents the product of the value of the resistor times the value of the capacitor. Note that three curves are actually shown. The curve in the middle represents the nominal frequency obtained for a given value of RC. A maximum curve and a minimum curve for different types of 3875 devices are also shown in the diagram.

RC MODE CONNECTION
Figure 14



FREQUENCY VS. RC
Figure 15



VIII

The designer must select the RC product such that a frequency of less than 2 MHz is not possible taking into account the maximum possible RC product and using the minimum curve shown in Figure 15. Also, the RC product must not allow a frequency of more than 4 MHz taking into account the minimum possible R and C and using the Maximum curve shown. Temperature induced variations in the external components should be considered in calculating the RC product.

Frequency variation from unit to unit due to switching speed and level at constant temperature and V_{CC} = + or – 5 percent.

Frequency variation due to V_{CC} with all other parameters constant with respect to +5V = +7 percent to –4 percent on all devices.

Frequency variation due to temperature with respect to 25 C (all other parameters constant) is as follows:

PART #	VARIATION
387X-00, –05	+6 percent to – 9 percent
387X-10, –15	+9 percent to –12 percent

Variations in frequency due to variations in RC components may be calculated as follows:

Maximum RC = (R max) (C external max + C_{XTL} max)

Minimum RC = (R min) (C external min + C_{XTL} min)

$$\text{Typical RC} = (\text{R typ})\left(\text{C external typ} + \frac{\{C_{XTL}\ \text{max} + C_{XTL}\ \text{min}\}}{2}\right)$$

Positive Freq. Variation = $\frac{\text{RC typical - RC minimum}}{\text{RC typical}}$

Negative Freq. Variation due to RC Components = $\frac{\text{RC maximum - RC typical}}{\text{RC typical}}$

Total frequency variation due to all factors:

387X-00, –05	387X-10, –15
= +18 percent plus positive frequency variation due to RC components	= +21 percent plus positive frequency variation due to RC components
= –18 percent minus negative frequency variation due to RC components	= –21 percent minus negative frequency variation due to RC components

Total frequency variation due to V_{CC} and temperature of a unit tuned to frequency at +5V V_{CC}, 25 C

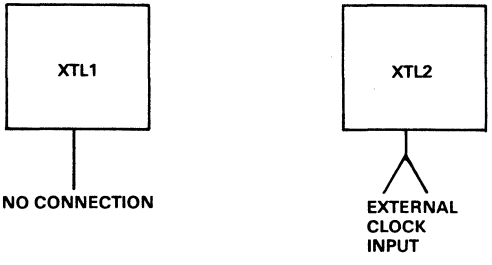
387X-00, –05	387X-10, –15
= + 13 percent	= + 16 percent

EXTERNAL CLOCK CONFIGURATION

The connection for the external clock time base configuration is shown in Figure 16. Refer to the DC Characteristics section for proper input levels and current requirements.

Refer to the Capacitance section of the appropriate 3875 Family device data sheet for input capacitance.

EXTERNAL MODE CONNECTION
Figure 16



OPERATING VOLTAGES AND TEMPERATURES

Dash Number Suffix	Operating Voltage V_{CC}	Operating Temperature T_A
- 00	+5V ± 10%	0°C - 70°C
- 05	+5V ± 5%	0°C - 70°C
- 10	+5V ± 10%	-40°C - +85°C
- 15	+5V ± 5%	-40°C - +85°C

See order information for explanation of part numbers.

ABSOLUTE MAXIMUM RATINGS*

	-00, -05	-10, -15
Temperature Under Bias	-20°C +85°C	-50°C to 100°C
Storage Temperature	-65°C +150°C	-65°C to +150°C
Voltage on any Pin With Respect to Ground (Except open drain pins and TEST)	-1.0V to +7V	-1.0V to +7V
Voltage on TEST with Respect to Ground	-1.0V to +9V	-1.0V to +9V
Voltage on Open Drain Pins with Respect to Ground	-1.0V to +13.5V	-1.0V to 13.5V
Power Dissipation	1.5W	1.5W
Power Dissipation by any one I/O pin	60mW	60mW
Power Dissipation by all I/O pins	600mW	600mW

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating and conditions for extended periods may affect device reliability.

AC CHARACTERISTICS

T_A, V_{CC} within specified operating range
I/O Power Dissipation < 100mW (Note 4)

SIGNAL	SYM	PARAMETER	-00,-05 MIN	-00,-05 MAX	-10,-15 MIN	-10,-15 MAX	UNIT	NOTES
XTL1 XTL2	t_o	Time Base Period, all clock modes	250	500	250	500	ns	4MHz-2MHz
	$t_{ex(H)}$	External clock pulse width high	90	400	100	390	ns	
	$t_{ex(L)}$	External clock pulse width low	100	400	110	390	ns	
Φ	t_Φ	Internal Φ clock	$2t_0$		$2t_0$			
WRITE	t_W	Internal WRITE Clock period	4 t Φ 6 t Φ		4tΦ 6tΦ			Short Cycle Long Cycle
I/O	$t_{dI/O}$	Output delay from internal WRITE clock	0	1000	0	1200	ns	50pF plus one TTL load
	$t_{sI/O}$	Input setup time to internal WRITE clock	1000		1200		ns	
$\overline{STROBE}$	$t_{I/O-s}$	Output valid to $\overline{STROBE}$ delay	3tΦ -1000	3tΦ +250	3tΦ -1200	3tΦ +300	ns	I/O load = 50fF + 1 TTL load
	t_{sL}	$\overline{STROBE}$ low time	8tΦ -250	12tΦ +250	8tΦ -300	125Φ +300	ns	$\overline{STROBE}$ load = 50pF + 3TTL loads
$\overline{RESET}$	t_{RH}	$\overline{RESET}$ hold time, low	6tΦ +750		6tΦ +1000		ns	
	t_{RPOC}	$\overline{RESET}$ hold time, low for power clear	power supply rise time +5.0		power supply rise time +5.5		ms	
EXT INT	t_{EH}	EXT INT hold time in active and inactive state	6tΦ +750		6tΦ +1000		ns	To trigger interrupt
			2tΦ		2tΦ		ns	To trigger timer

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AC CHARACTERISTICS FOR MK38P75

(Signals brought out at socket)
T_A, V_{CC} within specified operating range.
I/O Power Dissipation ≤ 100 mW. (Note 2)

SYMBOL	PARAMETER	-00, -05		-10, -15		UNIT	CONDITION
		MIN	MAX	MIN	MAX		
t_{aas}*	Access time from Address A_{11}-A_0 stable until data must be valid at D_7-D_0	650		650		ns	Φ = 2.0 MHz

*See Table in Figure 10

CAPACITANCE

T_A = 25°C All Part Numbers

SYM	PARAMETER	MIN	MAX	UNIT	NOTES
C_{IN}	Input capacitance; I/O $\overline{\text{RESET}}$, EXT INT, TEST		10	pF	unmeasured pins grounded
C_{XTL}	Input capacitance; XTL1, XTL2	23.5	29.5	pF	

DC CHARACTERISTICS

T_A, V_{CC} within specified operating range
I/O Power Dissipation ≤ 100mW (Note 4)

SYM	PARAMETER	-00,-05		-10,-15		UNIT	NOTES
		MIN	MAX	MIN	MAX		
I_{CC}	Average Power Supply Current		94		125	mA	Outputs Open (5)
P_D	Average Power Dissipation		440		575	mW	Outputs Open (6)
V_{IHEX}	External Clock input high level	2.4	5.8	2.4	5.8	V	
V_{ILEX}	External Clock input low level	-.3	.6	-.3	.6	V	
I_{IHEX}	External Clock input high current		100		130	μA	V_{IHEX}=V_{CC}
I_{ILEX}	External Clock input low current		-100		-130	μA	V_{ILEX}=V_{SS}
$V_{IHI/O}$	Input high level, I/O pins	2.0	5.8	2.0	5.8	V	Standard Pull-Up (1,2)
		2.0	13.2	2.0	13.2	V	Open Drain (1,3)
V_{IHR}	Input high level, $\overline{\text{RESET}}$	2.0	5.8	2.2	5.8	V	Standard Pull-Up(1, 2)
		2.0	13.2	2.2	13.2	V	No Pull-Up (1,3)
V_{IHEI}	Input high level, EXT INT	2.0	5.8	2.2	3.8	V	Standard Pull-Up(1, 2)
		2.0	13.2	2.2	13.2	V	No Pull-Up (1,3)
V_{IL}	I/O ports, $\overline{\text{RESET}}$, EXT INT input low level	-.3	.8	-.3	.7	V	
V_{ILRPT}	$\overline{\text{RESET}}$ input low level to protect RAM during loss at V_{CC}	-.3	.4	-.3	.4	V	
I_{IL}	Input low current, standard pull-up pins		-1.6		-1.9	mA	V_{IN}=0.4V (2)

DC CHARACTERISTICS (Continued)

T_A, V_{CC} within specified operating range
I/O Power Dissipation ≤ 100 mW (Note 4)

SYM	PARAMETER	-00, -05 MIN	-00, -05 MAX	-10, -15 MIN	-10, -15 MAX	UNIT	NOTES
I_L	Input leakage current, open drain pins Reset and EXT INT inputs With no pull-up resistor		+10 -5		+18 -8	μA μA	V_{IN}=13.2V V_{IN}=0.0V (3)
I_{OH}	Output high current, standard	-100		-89		μA	V_{OH}=2.4V
	Pull-Up pins	-30		-25		μA	V_{OH}=3.9V
I_{OHDD}	Output high current	-100		-80		μA	V_{OH}=2.4V
	Direct Drive pins	-1.5		-1.3		mA	V_{OH}=1.5V
			-8.5		-11	mA	V_{OH}=0.7V
I_{OL}	Output low current, I/O ports	1.8		1.65		mA	V_{OL}=0.4V
I_{OHS}	STROBE Output High current	-300		-270		μA	V_{OL}=2.4V
I_{OLS}	STROBE output low current	5.0		4.5		mA	V_{OL}=0.4V

DC CHARACTERISTICS FOR STANDBY POWER PINS

V_{CC}, T_A within operating range I/O Power Dissipation ≤ 100 mW (Note 4)

SYMBOL	PARAMETER	-00, -05 MIN	-00, -05 MAX	-10,-15 MIN	-10,-15 MAX	UNIT	NOTES
V_{SB}	Standby V_{CC} for RAM	3.2	V_{CC} MAX	3.2	V_{CC} MAX	V	
I_{SB}	Standby Current		6		7.5	mA	V_{SB} = V_{SB} MAX
			3.7		5.0	mA	V_{SB} = V_{SB} MIN
I_{CHARGE}	Trickle charge available on V_{SB} with V_{CC} in operating range.	-.8		-.7		mA	V_{SB} = 3.8V
			-15		-19	mA	V_{SB} = 3.2V

DC CHARACTERISTICS FOR MK38P75

(Signals brought out at socket)
T_A, V_{CC} within specified operating range, I/O power dissipation ≤ 100 mW (Note 2)

SYM	PARAMETER	-00, -05 MIN	-00, -05 MAX	-10, -15 MIN	-10, -15 MAX	UNIT	CONDITION
I_{CCE}	Power Supply Current for EPROM		-185		-185	mA	
V_{IL}	Input Low Level Data bus in	-0.3	0.8	-0.3	0.8	V	
V_{IH}	Input High Level Data bus in	2.0	5.8	2.0	5.8	V	
I_{OH}	Output High Current	-100		-90		μA	V_{OH}=2.4 V
		-30		-25		μA	V_{OH}=3.9 V
I_{OL}	Output Low Current	1.8		1.65		mA	V_{OL}=0.4 V
I_{IL}	Input Leakage Current		10		10	μA	Data Bus in Float

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1. $\overline{\text{RESET}}$ and ET INT have internal Schmit triggers giving minimum .2V hysteresis.
2. $\overline{\text{RESET}}$ and EXT INT prgrammed with standard pull-up
3. $\overline{\text{RESET}}$ or EXT INT programmed without standard pull-up
4. Power dissipation for I/O pins is calculated by $\Sigma (V_{CC} - V_{IL})(|I_{IL}|) + \Sigma (V_{CC} - V_{OH})(|I_{OH}|) + \Sigma (V_{OL})(I_{OL})$
5. I_{CC} exclusive of I_{charge}
6. P_D exclusive of battery charging power. Battery charging power dissipated inside the MK3875 $(V_{CC} - V_{SB})(I_{charge})$

TIMER AC CHARACTERISTICS

Definitions:

Error = Indicated time value - actual time value

tpsc = tΦ x Prescale Value

Interval Timer Mode

Single interval error, free running (Note 3)	±6tΦ
Cumulative interval error, free running (Note 3)	0
Error between two Timer reads (Note 2)	±(tpsc + tΦ)
Start timer to stop Timer error (Notes 1, 4)	+tΦ to - (tpsc + tΦ)
Start Timer to read Timer error (Notes 1, 2)	-5tΦ to -(tpsc + 7tΦ)
Start Timer to interrupt request error (Notes 1, 3)	-2tΦ to -8tΦ
Load Timer to stop Timer error (Note 1)	+tΦ to –(tpsc + 2tΦ)
Load Timer to read Timer error (Notes 1, 2)	-5tΦ to -(tpsc + 8tΦ)
Load Timer to interrupt request error (Notes 1, 3)	-2tΦ to -9tΦ

Pulse Width Measurement Mode

Measurement accuracy (Note 4)	+t Φ to -(tpsc +2t Φ
Minimum pulse width of EXT INT pin	2t Φ

Event Counter Mode

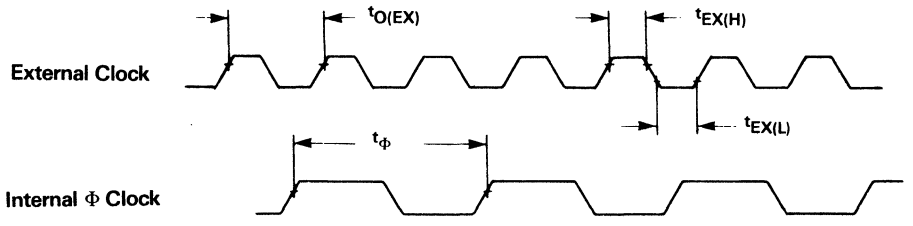
Minimum active time of EXT INT pin	2t Φ
Minimum inactive time of EXT INT pin	2t Φ

Notes:

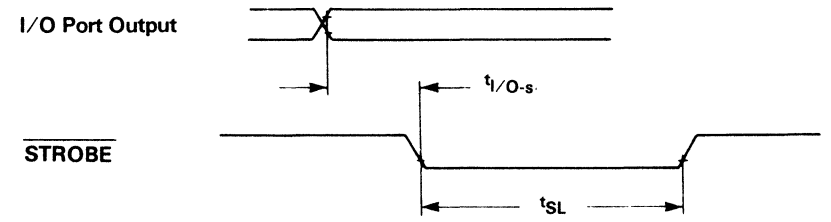
1. All times which entail loading, starting, or stopping the Timer are referenced from the end of the last machine cycle of the OUT or OUTS instruction.
2. All times which entail reading the Timer are referenced from the end of the last machine cycle of the IN or INS instruction.
3. All times which entail the generation of an interrupt request are referenced from the start of the machine cycle in which the appropriate interrupt request latch is set. Additional time may elapse if the interrupt request occurs during a privileged or multicycle instruction.
4. Error may be cumulative if operation is repetitively performed.

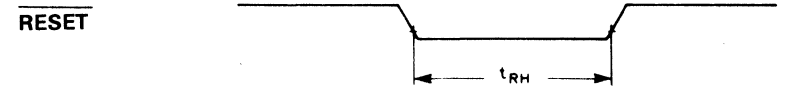
AC TIMING DIAGRAM

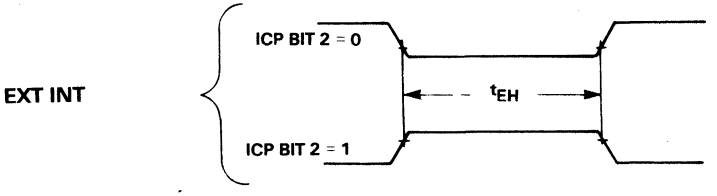
Figure 17



Input capacitance; I/O, $\overline{\text{RESET}}$, EXT INT,







Note: All AC measurements are referenced to V_{IL} max., V_{IH} min., V_{OL} (.8v), or V_{OH} (2.0v).

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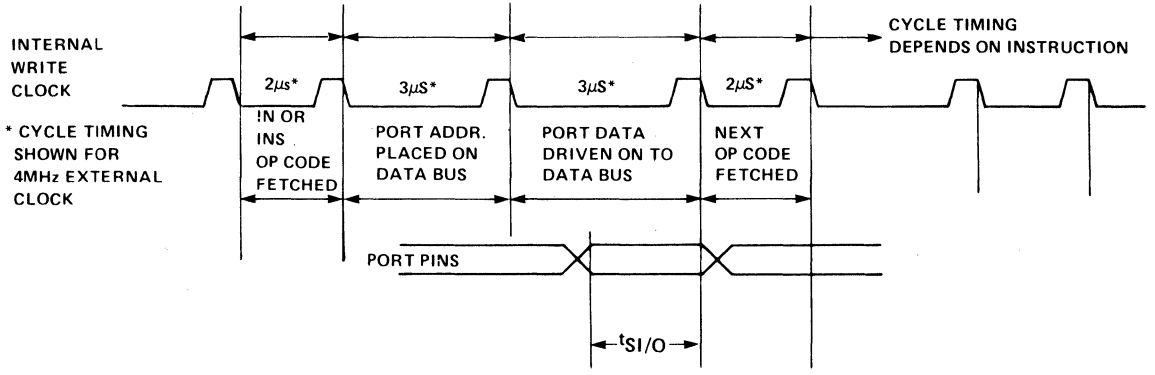
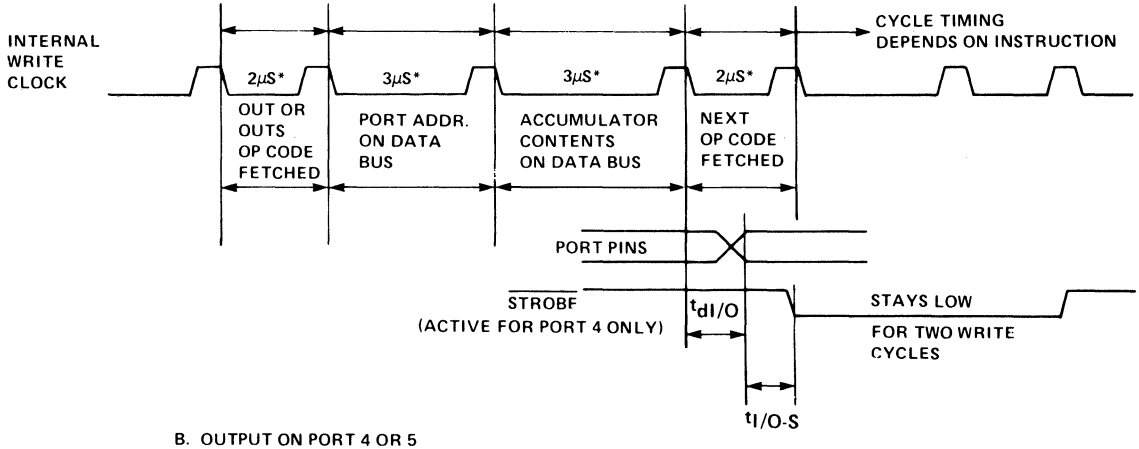
INPUT/OUTPUT AC TIMING

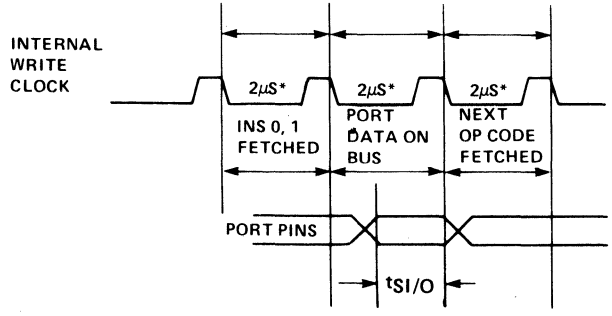
Figure 18



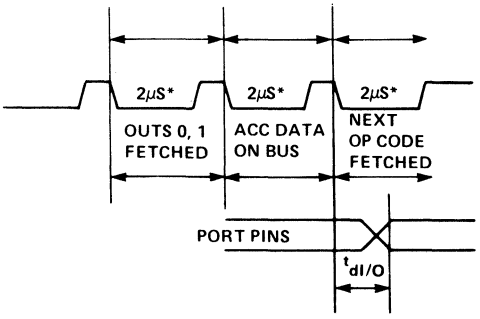
A. INPUT ON PORT 4 OR 5



B. OUTPUT ON PORT 4 OR 5



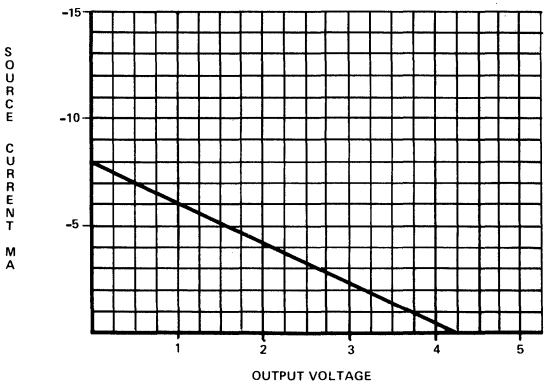
C. INPUT ON PORT 0 OR 1



D. OUTPUT ON PORT 0, 1

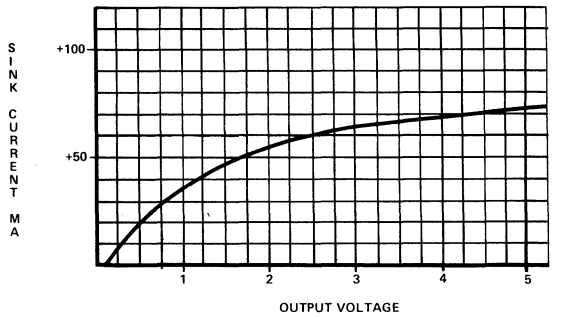
STROBE SOURCE CAPABILITY (TYPICAL AT V_{CC} = 5V, T_A = 25°C)

Figure 19



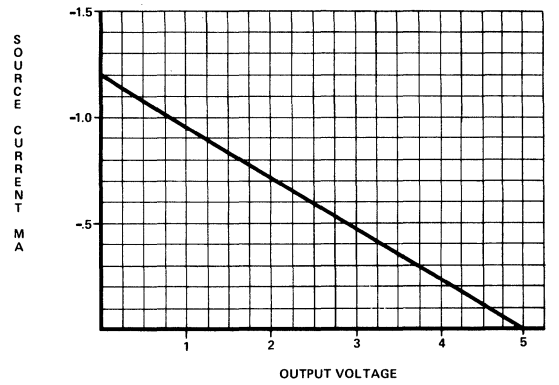
STROBE SINK CAPABILITY (TYPICAL AT V_{CC} = 5V, T_A = 25°C)

Figure 20



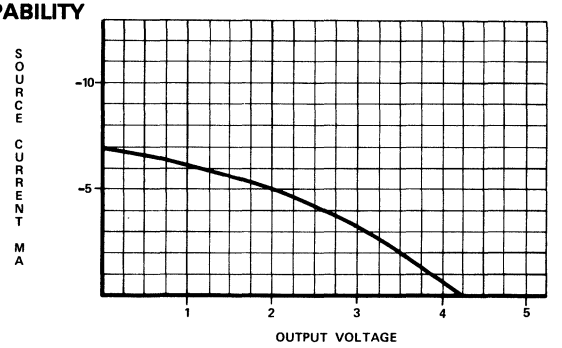
STANDARD I/O PORT SOURCE CAPABILITY (TYPICAL AT V_{CC} = 5V, T_A = 25°C)

Figure 21



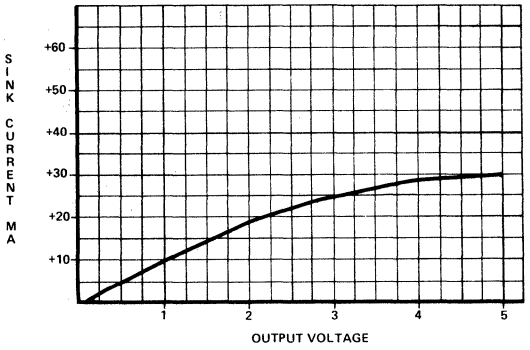
DIRECT DRIVE I/O PORT SOURCE CAPABILITY (TYPICAL AT V_{CC} = 5V, T_A = 25°C)

Figure 22



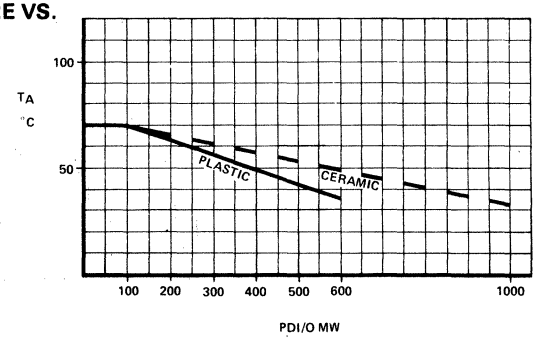
I/O PORT SINK CAPABILITY (TYPICAL AT V_{CC} = 5V, T_A = 25°C)

Figure 23



MAXIMUM OPERATING TEMPERATURE VS. I/O POWER DISSIPATION

Figure 24

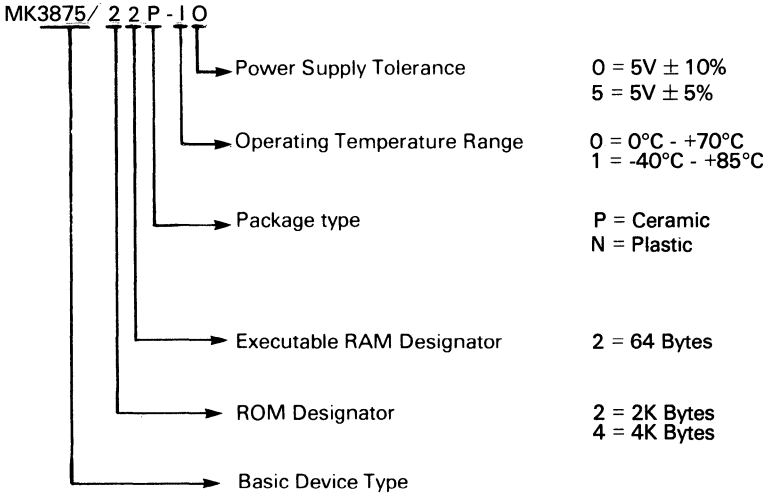


ORDERING INFORMATION

There are two types of part numbers for the 3870 family of devices. The generic part number describes the basic device type, the amount of ROM and executable RAM, the desired package type, temperature range and power supply tolerance. For each customer specific code, additional information defining I/O options and oscillator options will be combined with the information described in the generic part number to define a customer/code specific device order number.

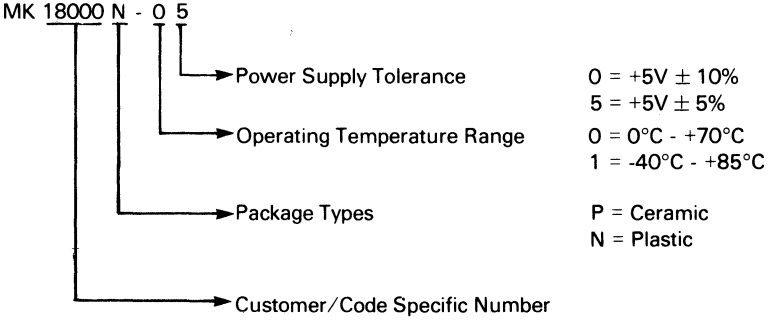
GENERIC PART NUMBER

An example of the generic part number is shown below.



DEVICE ORDER NUMBER

An example of the device order number is shown below.



The customer/code specific number defines the ROM bit pattern, I/O configuration, oscillator type, and generic part type to be used to satisfy the requirement of a particular customer purchase order. For further information on the ordering of mask ROM devices, the customer should refer to the 3870 Family Technical Manual.

VIII

1982/1983 MICROELECTRONIC DATA BOOK

PRELIMINARY

MOSTEK®

MICROCOMPUTER COMPONENTS

CMOS MICROCOMPUTER CLOCK/RAM

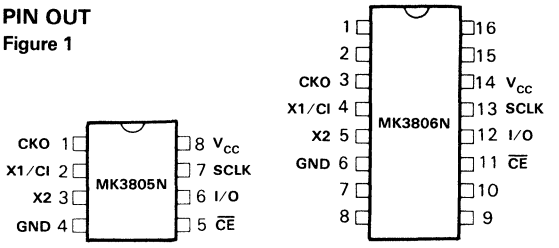
MK3805N/MK3806N

FEATURES

- Real-time clock counts seconds, minutes, hours, date of the month, day of the week, month, and year. Every 4th year, February has 29 days.
- Serial I/O for minimum pin count (8 pins)
- 24 x 8 RAM for scratchpad data storage
- Simple Microcomputer interface
- High speed shift clock independent of crystal oscillator frequency
- Single byte or multiple byte (Burst Mode) data transfer capability for read or write of clock or RAM data.
- TTL Compatible (V_{CC} = 5V)
- Low-power CMOS
- $I_{CC} \leq 2mA$ (V_{CC} = 5 V)
- $+3V \leq V_{CC} \leq 9.5V$

PIN OUT

Figure 1



PIN DESCRIPTION

Table 1

PIN 3805N	PIN 3806N	NAME	DESCRIPTION
1	3	CKO	Buffered Sytem Clock Output
2	4	X1/C1	Crystal or External Clock Input
3	5	X2	Crystal Input
4	6	GND	Power Supply Pin
5	11	$\overline{CE}$	Chip Enable for Serial I/O Transfer
6	12	I/O	Data Input/Output Pin
7	13	SCLK	Shift Clock for Serial I/O Transfer
8	14	V_{CC}	Power Supply Pin

GENERAL DESCRIPTION

Many microprocessor applications require a real-time clock and/or memory that can be battery powered with very low power drain. The MK3805N/MK3806N are specifically designed for these applications. The device contains a real-time clock/calendar, 24 bytes of static RAM, an on-chip oscillator, and it communicates with the microprocessor via a simple serial interface. The MK3805N/MK3806N are fabricated using CMOS technology, thus insuring very low power consumption.

The real-time clock/calendar provides seconds, minutes, hours, day, date, month, and year information to the microprocessor. The end of the month date is automatically adjusted for months with less than 31 days, including correction for leap year every 4 years. The clock operates in either the 24 hour or 12 hour format with an AM/PM indicator.

The on-chip oscillator provides a real-time clock source for the clock/calendar. It incorporates a programmable divider so that a wide variety of crystal frequencies can be accommodated. The oscillator also has an output available that can be connected to the microprocessor clock input. A separately programmable divider provides several different output frequencies for any given crystal frequency. This feature can eliminate having to use a separate crystal or external oscillator for the microprocessor, thereby reducing system cost.

Interfacing the CLOCK/RAM with a microprocessor is greatly simplified using synchronous serial communication. Only 3 lines are required to communicate with the CLOCK/RAM: (1) $\overline{CE}$ (chip enable), (2) I/O (data line) and (3) SCLK (shift register clock). Data can be transferred to and from the CLOCK/RAM one byte at a time or in a burst of up to 24 bytes.

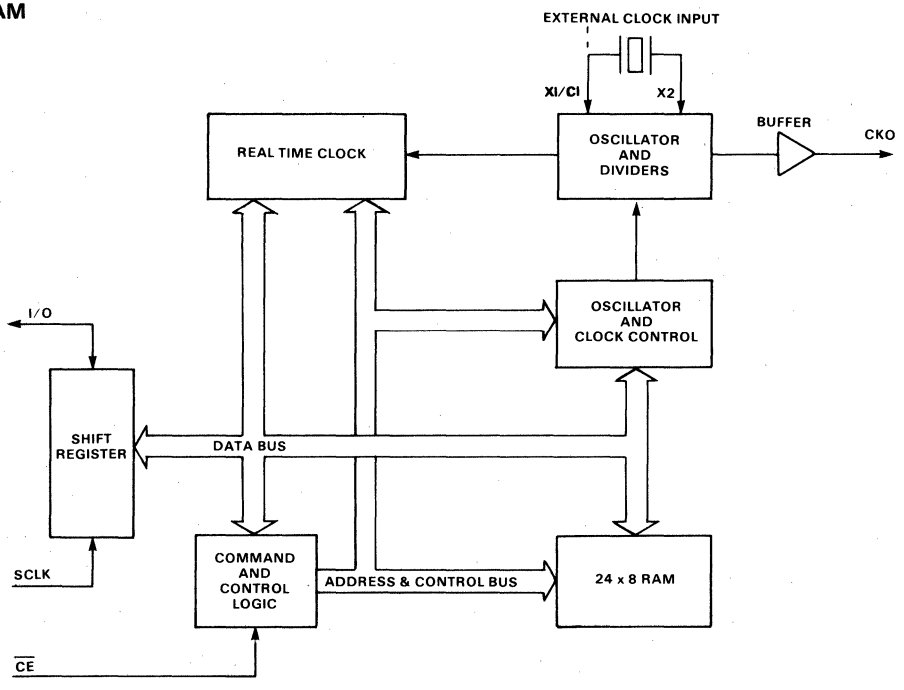
TECHNICAL DESCRIPTION

Figure 2 is a block diagram of the CLOCK/RAM chip. Its main elements are the oscillator and divider circuit, oscillator and clock control, the real-time clock/calendar, static RAM, the serial shift register, and the command and control logic.

IX

BLOCK DIAGRAM

Figure 2



The shift register is used to communicate with the outside world. Data on the I/O line is either input or output on each shift register clock pulse when the chip is enabled. If the chip is in the input mode, the data on the I/O line is input to the shift register on the rising edge of SCLK. If in the output mode, data is shifted out onto the I/O line on the falling edge of SCLK.

The command and control logic receives the first byte input by the shift register after $\overline{CE}$ goes active. This byte must be the command byte and will direct further operations within the CLOCK/RAM. The command specifies whether subsequent transfers will be data input or data output, and which register or RAM location will be involved.

A control register provides programmable control of the divider for the internal clock signal, the external clock signal, the crystal type and mode, and the write protect function.

The real-time clock/calendar is accessed via seven registers. These registers control seconds, minutes, hours, day, date, month, and year. Certain bits within these registers also control a run/stop function, 12/24 hour format, and indicate AM or PM (12 hour mode only). These registers can be accessed sequentially in Burst Mode, or randomly in a single byte transfer.

The static RAM is organized as 24 bytes of 8-bits each. They can be accessed either sequentially in burst mode, or randomly in a single byte transfer.

POWER UP

A clock signal is necessary for correct power up, and it should be noted that a delay exists between power up and the correct power up state of the clock and control registers.

DATA TRANSFER

Data Transfer is accomplished under control of the $\overline{CE}$ and SCLK inputs by an external microcomputer. Each transfer consists of a single byte ADDRESS/COMMAND input followed by a single byte or multiple byte (if Burst Mode is specified) data input or output, as specified by the ADDRESS/COMMAND byte. The serial data transfer occurs with LSB first, MSB last format.

ADDRESS/COMMAND BYTE

The ADDRESS/COMMAND Byte is shown below:

7	6	5	4	3	2	1	0
1	RAM / $\overline{CK}$	A4	A3	A2	A1	A0	Rd / $\overline{W}$

As defined, the MSB (bit 7) must be a logical 1; bit 6 specifies a Clock/Calendar/Control register if logical 0 or a RAM register if logical 1; bits 1-5 specify the designated

register(s) to be input or output; and the LSB (bit 0) specifies a WRITE operation (input) if logical 0 or READ operation (output) if logical 1.

BURST MODE

Burst Mode may be specified for either the Clock/Calendar/Control registers or for the RAM registers by addressing location 31 Decimal (ADDRESS/COMMAND bits 1-5 = logical 1). As before, bit 6 specifies Clock or RAM and bit 0 specifies read or write.

There is no data storage capability at location 31 in either the Clock/Calendar/Control registers or the RAM registers.

SCLK and $\overline{CE}$ CONTROL

All data transfers are initiated by $\overline{CE}$ going low. After $\overline{CE}$ goes low, the next 8 SCLK cycles input an ADDRESS/COMMAND byte of the proper format. A SCLK cycle is the sequence of a positive edge followed by a negative edge. For data inputs, the data must be valid during the SCLK cycle. If bit 7 is not a logical 1, indicating a valid CLOCK/RAM ADDRESS/COMMAND, the ADDRESS/COMMAND byte is ignored as are all SCLK cycles until $\overline{CE}$ goes high and returns low to initiate a new ADDRESS/COMMAND transfer. See Figure 3.

ADDRESS/COMMAND bits and DATA bits are input on the rising edge of SCLK, and DATA bits are output on the falling edge of SCLK.

A data transfer terminates if $\overline{CE}$ goes high, and the transfer must be reinitiated by the proper ADDRESS/ COMMAND when $\overline{CE}$ again goes low. The data I/O pin is high impedance when $\overline{CE}$ is high.

DATA INPUT

Following the 8 SCLK cycles that input the WRITE Mode ADDRESS/COMMAND byte (bit 0 = logical 0), a DATA byte is input on the rising edge of the next 8 SCLK cycles (per byte, if Burst Mode is specified). Additional SCLK cycles are ignored should they inadvertently occur.

DATA OUTPUT

Following the 8 SCLK cycles that input the READ Mode ADDRESS/COMMAND byte (bit 0 = logical 1), a DATA byte is output on the falling edge of the next 8 SCLK cycles (per byte, if Burst Mode is specified). Additional SCLK cycles retransmit the data byte(s) should they inadvertently occur, so long as $\overline{CE}$ remains low. This operation permits continuous Burst Read Mode capability.

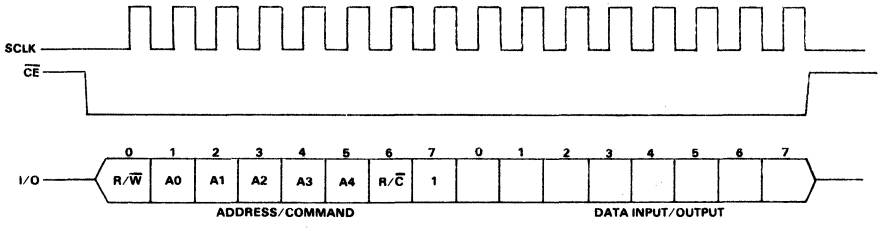
DATA TRANSFER SUMMARY

A data transfer summary is shown in Figure 3.

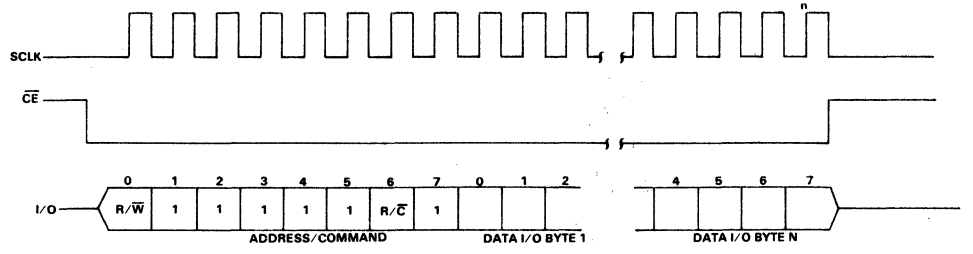
DATA TRANSFER SUMMARY

Figure 3

I. SINGLE BYTE TRANSFER



II. BURST MODE TRANSFER



FUNCTION	BYTE N	SCLK n
CLOCK	8	72
RAM	24	200

NOTES

1) Data input sampled on rising edge of clock
2) Data output changes on falling edge of clock
3) Rising edge of $\overline{CE}$ terminates operation and resets address/command

REGISTER DEFINITION

CLOCK/CALENDAR

The Clock/Calendar is contained in 7 addressable/writeable/readable registers, as defined below.

Address	Function	Range (BCD)
0	Seconds+Clock Halt Flag	00-59
1	Minutes	00-59
2	Hours/AM-PM/12-24 Mode	00-23 or 01-12
3	Date	01-28,29, 30,31
4	Month	01-12
5	Day	01-07
6	Year	00-99

Data contained in the Clock/Calendar registers is in binary coded decimal format (BCD).

CLOCK HALT FLAG

Bit 7 of the Seconds Register is defined as the Clock Halt Flag. Bit 7 = logical 1 inhibits the 1 Hz input to the Clock/Calendar. Bit 7 is set to logical 1 on power-up to prevent counting, and it may be set high or low by writing to the seconds register under normal operation of the device.

AM-PM/12-24 MODE

Bit 7 of the Hours Register is defined as the 12 or 24 hour mode select bit. When high, the 12 hour mode is selected. In the 12-hour mode, bit 5 is the AM/PM bit with logic high being PM. In the 24-hour mode, bit 5 is the second 10-hour bit (20-23 hours).

TEST MODE BITS

Bit 7 of the Date Register and Bit 7 of the Day Register are Test Mode Bits utilized in testing the MK3805N/MK3806N. These bits should be logic 0 for normal operation.

CONTROL REGISTER

The Control Register specifies the crystal mode/frequency to be used, the system clock output frequency, and the WRITE PROTECT Mode for data protection. The Control Register is located at address 7 in the Clock/Calendar/Control address space.

7	6	5	4	3	2	1	0
WP	C1	C0	X4	X3	X2	X1	X0

CRYSTAL DIVIDER MODE

X4 and X3 specify the Crystal frequency divider mode selected.

X4	X3	Xtal Mode	Primary Frequencies
0	0	Binary	2^{22}, 2^{21}, 2^{20} Hz
0	1	Microprocessor	8, 5, 4, 2.5, 2, 1.25, 1 MHz
1	0	Baud Rate	7.3728, 3.6864, 1.8432 MHz
1	1	Color Burst	3.5795 MHz

CRYSTAL DIVIDER PRESCALER

X2, X1, and X0 specify a particular prescaler divider selection necessary to generate a 1 Hz frequency for the Clock/Calendar. Refer to Table 2 for complete definition.

SYSTEM CLOCK OUTPUT

C1 and C0 designate the system clock output frequency selected. The options are X, X/2, X/4, and ~2 kHz. When in the Binary Mode and C1, C0 = '1', the output frequency is 2048 Hz. In any other mode, the output frequency is ~2048 Hz. Refer to Table 3 for complete definition.

WRITE PROTECT

Bit 7 of the Control Register is the WRITE PROTECT Flag. Bit 7 is set to logical 1 on power-up, and it may be set high or low by writing to the Control Register. When high, the WRITE PROTECT Flag prevents a write operation to any internal register, including the other bits of the Control Register. Further, logic is included such that the WRITE PROTECT bit may be reset to a logic 0 by a Write operation without altering the other bits of the Control Register.

CLOCK/CALENDAR/CONTROL BURST MODE

Address 31 Decimal of the Clock/Calendar/Control Address space specifies Burst Mode operation. In this mode, the 7 Clock/Calendar Registers and the Control Register may be consecutively read or written. Addresses above address 7 (Control Register) are non-existent; only addresses 0-7 are accessible.

RAM

The static RAM is contained in 24 addressable/writeable/readable registers, addressed consecutively in the RAM address space beginning at location 0.

RAM BURST MODE

Address 31 Decimal of the RAM address space specifies Burst Mode operation. In this mode, the 24 RAM registers may be consecutively read or written. Addresses above the maximum RAM address location are non-existent and are not accessible.

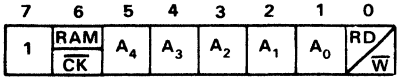
REGISTER SUMMARY

A Register, Data Format summary is shown in Figure 4.

MICROCOMPUTER CLOCK/RAM ADDRESS/COMMAND, REGISTER, DATA FORMAT SUMMARY

Figure 4

I. ADDRESS/COMMAND FORMAT



II. REGISTER ADDRESS

A. CLOCK

	7	6	5	4	3	2	1	0	REGISTER DEFINITION									POWER ON RESET
										7				4	3		0	
SEC	1	0	0	0	0	0	0	RD/W	00-59	CH		10 SEC				SEC		80
MIN	1	0	0	0	0	0	1	RD/W	00-59	0		10 MIN				MIN		00
HR	1	0	0	0	0	1	0	RD/W	01-12 00-23	12/24	0	10 A/P		HR		HR		00
DATE	1	0	0	0	0	1	1	RD/W	01-28/29 01-30 01-31	T_1	0	10 DATE				DATE		01
MONTH	1	0	0	0	1	0	0	RD/W	01-12	0	0	0	10 M			MONTH		01
DAY	1	0	0	0	1	0	1	RD/W	01-07	T_2	0	0	0	0		DAY		01
YEAR	1	0	0	0	1	1	0	RD/W	0-99	10 YEAR						YEAR		00
CONTROL	1	0	0	0	1	1	1	RD/W		WP	C_1	C_0	X_4	X_3	X_2	X_1	X_0	A0
CLOCK BURST	1	0	1	1	1	1	1	RD/W										

B. RAM

RAM 0	1	1	0	0	0	0	0	RD/W	RAM DATA 0	XX
RAM 23	1	1	1	0	1	1	1	RD/W	RAM DATA 23	XX
RAM BURST	1	1	1	1	1	1	1	RD/W		

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CRYSTAL FREQUENCY SELECTION

Table 2

X4	X3	X2	X1	X0	f_{XTAL} (MHz) Crystal Frequency	Comments
0	0	0	0	0	8.388608	Power on condition
0	0	0	0	1	8.388608	
0	0	0	1	0	4.194304	
0	0	0	1	1	4.194304	
0	0	1	0	0	2.097152	
0	0	1	0	1	2.097152	
0	0	1	1	0	1.048576	
0	0	1	1	1	0.032768	
0	1	0	0	0	8.000000	
0	1	0	0	1	5.000000	
0	1	0	1	0	4.000000	
0	1	0	1	1	2.500000	
0	1	1	0	0	2.000000	
0	1	1	0	1	1.250000	
0	1	1	1	0	1.000000	
0	1	1	1	1	0.031250	
1	0	0	0	0	7.372800	
1	0	0	0	1	7.372800	
1	0	0	1	0	3.686400	
1	0	0	1	1	3.686400	
1	0	1	0	0	1.843200	
1	0	1	0	1	1.843200	
1	0	1	1	0	0.921600	
1	0	1	1	1	0.028800	
1	1	0	0	0	7.159040	
1	1	0	0	1	7.159040	
1	1	0	1	0	3.579520	
1	1	0	1	1	3.579520	
1	1	1	0	0	1.789760	
1	1	1	0	1	1.789760	
1	1	1	1	0	0.894880	
1	1	1	1	1	0.027965	

CLOCK OUTPUT SELECTION

Table 3

C1	C0	CKO Output Frequency	Comments
0	0	f_{XTAL}	
0	1	$f_{XTAL} \div 2$	Power on condition
1	0	$f_{XTAL} \div 4$	
1	1	2048 Hz	Binary mode

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} relative to GND ..... -0.5 V to + 12.0 V
Voltage on any pin ..... -0.5 V to + V_{CC} + .5
Temperature under bias ..... -50°C + 95°C
Storage Temperature ..... -55°C to +125°C

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

DC OPERATING CONDITIONS
$-40°C \leq T_A \leq +85°C$

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	NOTES
V_{CC}	Supply Voltage	3.0	5.0	9.5	V	1

DC ELECTRICAL CHARACTERISTICS
$-40°C \leq T_A \leq +85°C$, $V_{CC} = 5V \pm 10\%$

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	NOTES
I_{CC1}	Power Supply Current			2.0	mA	2
I_{CC2}	Power Supply Current			0.1	mA	3
I_{LI}	Input Leakage Current, SCLK and CE	-1.0		1.0	μA	4
I_{LO}	Output Leakage Current, I/O Pin	-10.0		10.0	μA	4
V_{IH}	Logic "1" Voltage, All Inputs except X1	2.0			V	1, 5
V_{IL}	Logic "0" Voltage, All Inputs			0.8	V	1
V_{IHX2}	Logic "1" Voltage, X_2 Input		3.5			
$V_{I/OH}$	Output Logic "1" Voltage, I/O pin	2.4			V	1(I_{OH}=-100μA)
$V_{I/OL}$	Output Logic "0" Voltage, I/O pin			0.4	V	1(I_{OL}= 1.8 mA)
V_{CKH}	Output Logic "1" Voltage, CKO pin	2.4			V	1(I_{OH} = -400μA)
V_{CKL}	Output Logic "0" Voltage, CKO pin			0.4	V	1(I_{OL} = 4.0 mA)

NOTES:
1. All voltages referenced to GND.
2. Crystal/Clock Input frequency = 8.4 MHz, outputs open.
3. Crystal/Clock Input frequency = 32,768 Hz, outputs open.
4. Measured with $V_{CC} = 5.0$ V, $0 \leq V_I \leq 5.0$ V, outputs in high impedance state.
5. When X_1 is driven by an external signal, a pull-up resistor is required.

AC ELECTRICAL CHARACTERISTICS

$-40°C \leq T_A \leq +85°C$, V_{CC} 5 V ± 10%

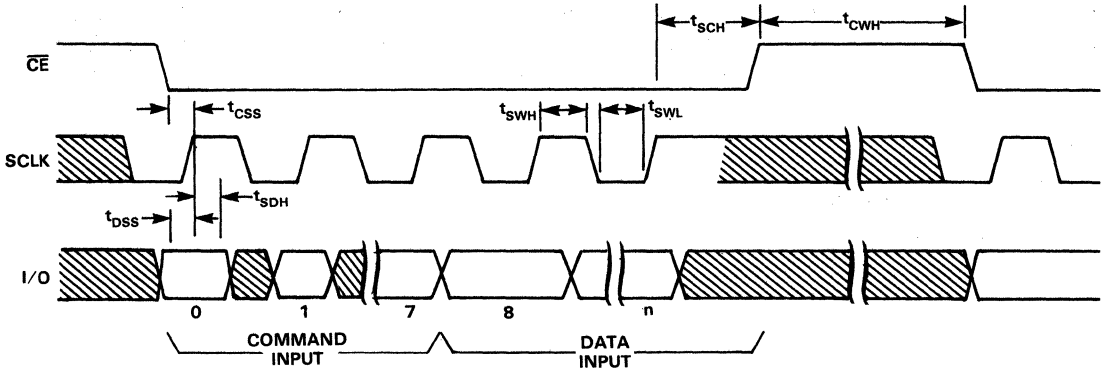
SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	NOTES
C_I	Capacitance on Input pin		6	10	pF	6
$C_{I/O}$	Capacitance on I/O pin		7	12	pF	6
C_X	Capacitance on XI/CI and X2		7	12	pF	6
f_X	Crystal frequency	27		8400	kHz	
t_{CSS}	$\overline{CE}$ to SCLK↑ set up time	1.0			μs	1,7
t_{SCH}	SCLK↑ to $\overline{CE}$↑ hold time	1.0			μs	1,7,12
t_{DSS}	Input Data to SCLK↑ set up time	1.0			μs	1,7
t_{SDH}	Input Data from SCLK↑ hold time	100			ns	1,7
t_{SDD}	Output Data from SCLK↓ delay time	300		1000	ns	1,7,8,9
t_{CDZ}	$\overline{CE}$↑ to I/O high impedance			500	ns	1,7,8,9
t_{SWL}	SCLK low time	1.95		∞	μs	
t_{SWH}	SCLK high time	1.95		∞	μs	
f_{SCLK}	SCLK frequency	DC		250	kHz	
t_{SR}, t_{SF}	SCLK Rise and Fall Time			1	μs	10
t_{CR}, t_{CF}	CKO Rise and Fall Time			50	ns	9,10
t_{CWH}	$\overline{CE}$ high time	2.0			μs	
t_{INIT}	Delay from power up till power up states valid — XTAL=27 kHz			500	ms	11
	XTAL=1 MHz			150	ms	11

NOTES:

6. Measured as $C = \frac{I \Delta t}{\Delta V}$, with $\Delta V = 3V$, and unmeasured pins grounded.
7. Measured at $V_{IH} = 2.0V$ or $V_{IL} = 0.8V$ and 50 ns rise and fall times on inputs.
8. Measured at $V_{OH} = 2.4V$ and $V_{OL} = 0.4V$.
9. Load Capacitance = 100 pF
10. t_r and t_f measured from 0.8V to 2.0V
11. t_{INIT} is measured from the time $V_{CC} = 4.5$ V and XTAL input is valid until the power up states of the CLOCK/RAM registers are valid.
12. t_{SCH} must follow the last rising edge of S_{CLK} during a write cycle in order to allow time to complete a write to the internal register.

I/O TIMING DIAGRAM

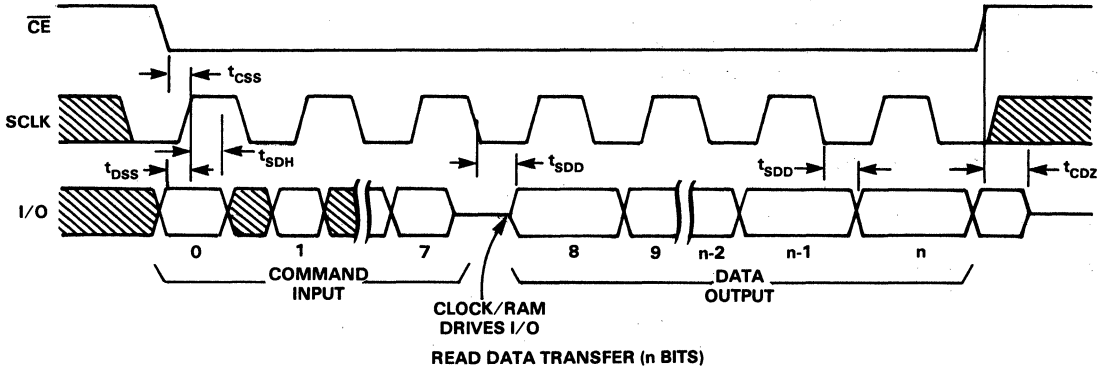
Figure 5



WRITE DATA TRANSFER (n BITS)

I/O TIMING DIAGRAM (Cont.)

Figure 5



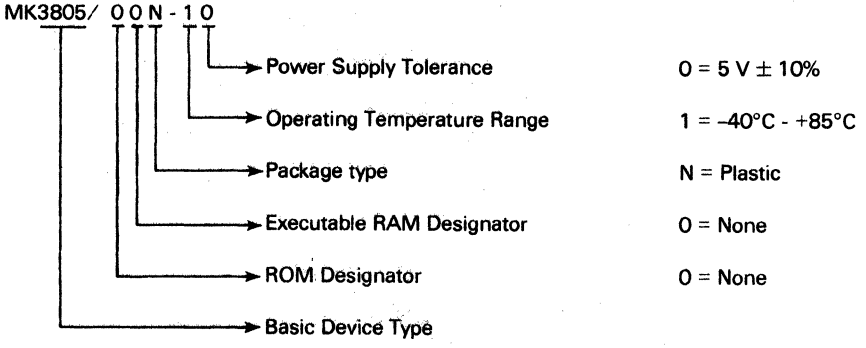
IX

ORDERING INFORMATION

There are two types of part numbers for the 3870 family of devices. The generic part number describes the basic device type, the amount of ROM and executable RAM, the desired package type, temperature range and power supply tolerence. For each customer specific code, additional information defining I/O options and oscillator options will be combined with the information describes in the generic part number to define a customer/code specific device order number.

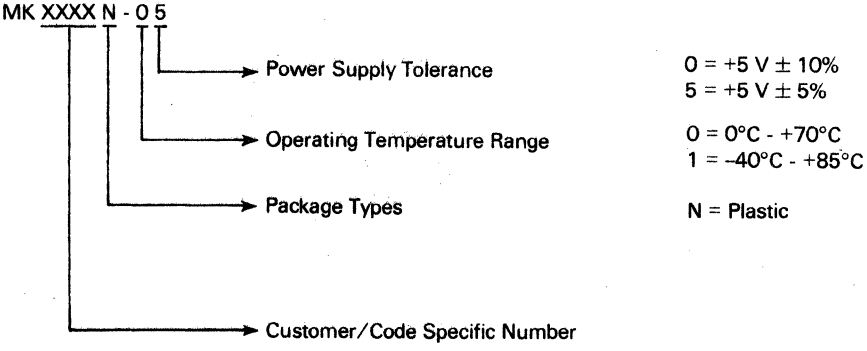
GENERIC PART NUMBER

An example of the generic part number is shown below.



DEVICE ORDER NUMBER

An example of the device order number is shown below.



The customer/code specific number defines the ROM bit pattern, I/O configuration, oscillator type, and generic part type to be used to satisfy the requirement of a particular customer purchase order. For further information on the ordering of mask ROM devices, the customer should refer to the 3870 Family Technical Manual.

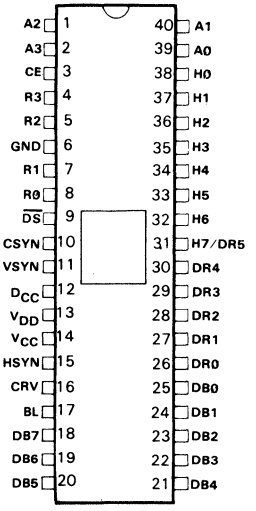
MK3807

Programmable CRT Video Control Unit (VCU)

FEATURES

- ☐ Fully Programmable Display Format
  - Characters per data row (1-200)
  - Data rows per frame (6-64)
  - Raster scans per data row (1-16)
- ☐ Programmable Monitor Sync Format
  - Raster Scans/Frame (256-1023)
  - "Front Porch"
  - Sync Width
  - "Back Porch"
  - Interlace/Non-Interlace
  - Vertical Blanking
- ☐ Direct Outputs to CRT Monitor
  - Horizontal Sync
  - Vertical Sync
  - Composite Sync
  - Blanking
  - Cursor coincidence
- ☐ Programmed via:
  - Processor data bus
  - External PROM
- ☐ Standard or Non-Standard CRT Monitor Compatible
- ☐ Refresh Rate: 60 Hz
- ☐ Scrolling
  - Single Line
  - Multi-Line
- ☐ Cursor Position Registers
- ☐ Programmable Character Format
- ☐ Programmable Vertical Data Positioning
- ☐ Balanced Beam Current Interlace
- ☐ Graphics Compatible
- ☐ Split-Screen Applications
  - Horizontal
  - Vertical
- ☐ Interlace or Non-Interlace operation

PIN CONFIGURATION



- ☐ TTL Compatibility
- ☐ BUS Oriented: Compatible with most microprocessors
- ☐ Second source to SMC CRT 5037
- ☐ N-Channel Silicon Gate Technology

IX

GENERAL DESCRIPTION

The Programmable CRT Video Control Unit (VCU) Chip is a user programmable 40-pin n channel MOS/LSI device containing the logic functions required to generate all the timing signals for the presentation and formatting of interlaced and non-interlaced video data on a standard or non-standard CRT monitor. The MK3807 VCU is a second source to SMC CRT 5037.

With the exception of the dot counter, which may be clocked at a video frequency above 25 MHz and is therefore not recommended for MOS implementation, all frame formatting, such as horizontal, vertical, and composite sync, characters per data row, data rows per frame, and raster scans per data row and per frame, are totally user programmable. The data row counter has been designed to facilitate scrolling. Refer to Table 1 for description of pin functions.

Programming is accomplished by loading seven 8-bit control registers directly off an 8-bit bidirectional data bus. Four register address lines and a chip enable line provide complete microprocessor compatibility for program controlled set up. The device can be "self loaded" via an external PROM tied on the data bus as described in the OPERATION section.

Figure 1 shows a block diagram of the internal functional components of the VCU.

The MK3807 (VCU) may be programmed for an odd or even number of scan lines per data row in both interlaced and non-interlaced modes.

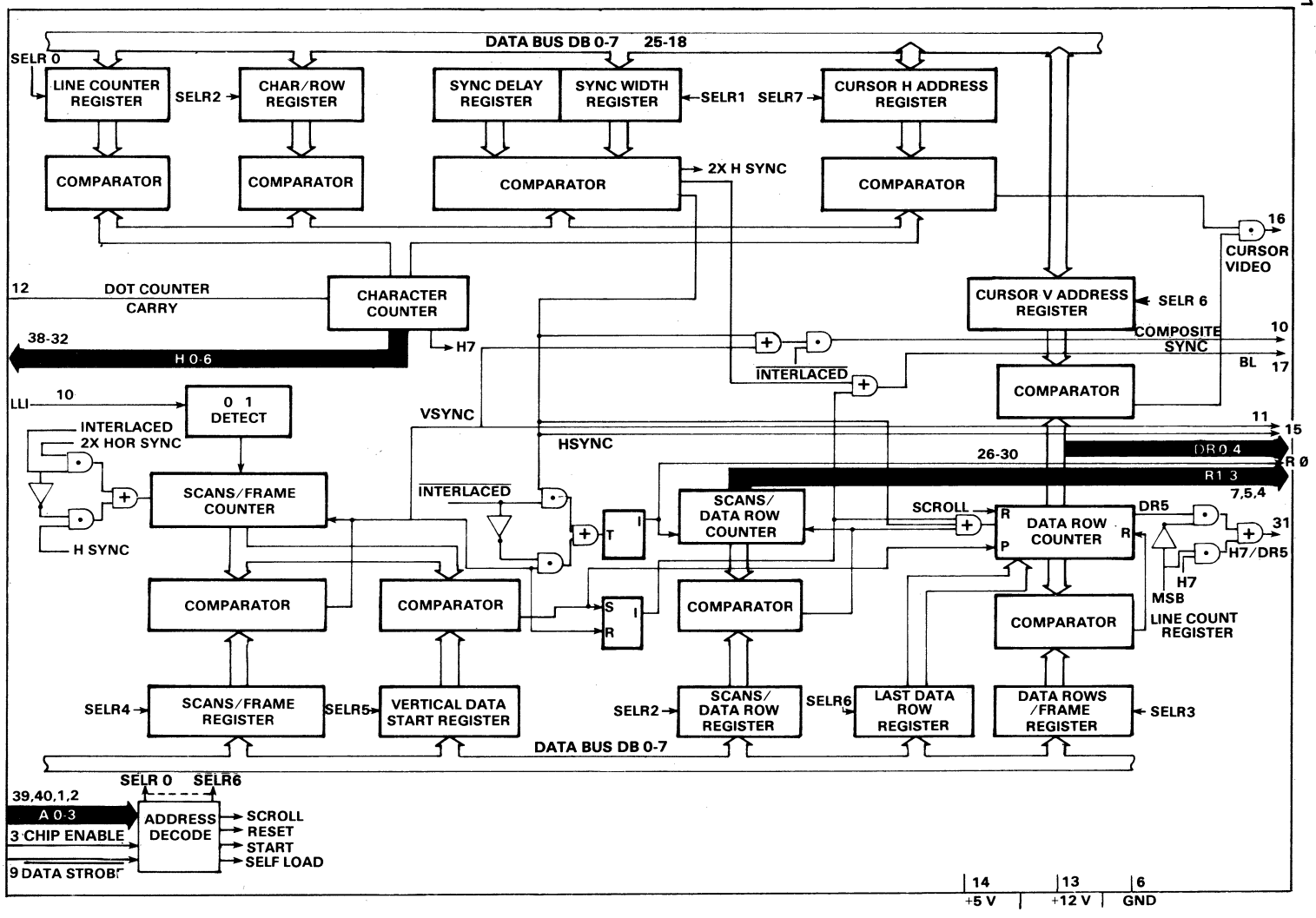
In addition to the seven control registers, two additional registers are provided to store the cursor character and data row addresses for generation of the cursor video signal. The contents of these two registers can also be read out onto the bus for update by the program.

DESCRIPTION OF PIN FUNCTIONS

Table 1

Pin No.	Symbol	Name	Input/ Output	Function
25-18	DB0-7	Data Bus	I/O	Data bus. Input bus for control words from microprocessor or PROM. Bi-directional bus for cursor address.
3	CE	Chip Enable	I	Signals chip that it is being addressed.
39,40,1,2	A0-3	Register Address	I	Register address bits for selecting one of seven control registers or either of the cursor address registers.
9	$\overline{DS}$	Data Strobe	I	Strobes DB0-7 into the appropriate register or outputs the cursor character address or cursor line address onto the data bus.
12	DCC	Dot Counter Carry	I	Carry from off-chip dot counter establishing basic character clock rate. Character clock.
38-32	H0-6	Character Counter Outputs	O	Character counter outputs.
7,5,4	R1-3	Scan Counter Outputs	O	Three most significant bits of the Scan Counter; row select inputs to character generator.
31	H7/DR5	H7/DR5	O	Pin definition is user programmable. Output is MSB of Character Counter if horizontal line counter (REG.0) is $\geq$ 128; otherwise output is MSB Of Data Row Counter.
8	R0	Scan Counter LSB	O	Least significant bit of the scan counter. In the interlaced mode with an even number of scans per data row, R0 will toggle at the field rate; for an odd number of scans per data row in the interlaced mode, R0 will toggle at the data row rate.
26-30	DR0-4	Data Row Counter Outputs	O	Data Row counter outputs.
17	BL	Blank	O	Defines non-active portion of horizontal and vertical scans.
15	HSYN	Horizontal Sync	O	Initiates horizontal retrace.
11	VSYN	Vertical Sync	O	Initiates vertical retrace.
10	CSYN	Composite Sync Output	O	Composite sync is provided on the MK3807. This output is active in non-interlaced mode only. Provides a true RS-170 composite sync wave form.
16	CRV	Cursor Video	O	Defines cursor location in data field.
14	V_{CC}	Power Supply	PS	+5 volt Power Supply
13	V_{DD}	Power Supply	PS	+12 volt Power Supply

BLOCK DIAGRAM
Figure 1



OPERATION

The design philosophy employed was to allow the MK3807 Programmable CRT Video Control Unit (VCU) to interface effectively with either a microprocessor based or hardwire logic system. The device is programmed by the user in one of two ways: via the processor data bus as part of the system initialization routine, or during power up via a PROM tied on the data bus and addressed directly by the Row Select outputs of the chip (See Figure 2). Seven 8-bit words are required to program the chip fully. Bit assignments for these words are shown in Tables 2, 3 and 4. The information contained in these seven words consists of the following:

Horizontal Formatting:

Characters/Data Row	A 3 bit code providing 8 mask programmable character lengths from 20 to 132. The standard device will be masked for the following character lengths; 20, 32, 40, 64, 72, 80, 96, and 132.
Horizontal Sync Delay	3 bits assigned providing up to 8 character times for generation of "front porch".
Horizontal Sync Width	4 bits assigned providing up to 16 character times for generation of horizontal sync width.
Horizontal Line Count	8 bits assigned providing up to 256 character times for total horizontal formatting.
Skew Bits	A 2 bit code providing from a 0 to 2 character skew (delay) between the horizontal address counter and the blank and sync (horizontal, vertical, composite) signals to allow for retiming of video data prior to generation of composite video signal. The Cursor Video signal is also skewed as a function of this code.

Vertical Formatting:

Interlaced/Non-interlaced	This bit provides for data presentation with odd/even field formatting for interlaced systems. It modifies the vertical timing counters as described below. A logic 1 establishes the interlace mode.
Scans/Frame	8 bits assigned, defined according to the following equations: Let X = value of 8 assigned bits. 1) in interlaced mode—scans/frame = 2X + 513. Therefore for 525 scans, program X = 6 (00000110). Vertical sync will occur precisely every 262.5 scans, thereby producing two interlaced fields. Range = 513 to 1023 scans/frame, odd counts only. 2) in non-interlaced mode—scans/frame = 2X + 256. Therefore for 262 scans, program X = 3 (00000011). Range = 256 to 766 scans/frame, even counts only. In either mode, vertical sync width is fixed at three horizontal scans (≡3H).
Vertical Data Start	8 bits defining the number of raster scans from the leading edge of vertical sync until the start of display data. At this raster scan the data row counter is set to the data row address at the top of the page.
Data Rows/Frame	6 bits assigned providing up to 64 data rows per frame.
Last Data Row	6 bits to allow up or down scrolling via a preload defining the count of the last displayed data row.
Scans/Data Row	4 bits assigned providing up to 16 scan lines per data row.

ADDITIONAL FEATURES

MK3807 VCU Initialization:

Under microprocessor control—The device can be reset under system or program control by presenting a 1010 address on A3-0. The device will remain reset at the top of the even field page until a start command is executed by presenting a 1110 address on A3-0.

Via "Self Loading"—In a non-processor environment, the self loading sequence is effected by presenting and holding the 1111 address on A3-0, and is initiated by the receipt of the strobe pulse ($\overline{DS}$). The 1111 address should be maintained long enough to ensure that all seven registers have been loaded (in most applications under one millisecond). The timing sequence will begin one line scan after the 1111 address is removed. In processor based systems, self loading is initiated by presenting the 0111 address to the device. Self loading is terminated by presenting the start command to the device which also initiates the timing chain.

Scrolling—In addition to the Register 6 storage of the last displayed data row a "scroll" command (address 1011) presented to the device will increment the first displayed data row count to facilitate up scrolling in certain applications.

CONTROL REGISTERS PROGRAMMING CHART
Table 2

Horizontal Line Count: Total Characters/Line = N + 1, N = 0 to 255 (DB0 = LSB)

Characters/Data Row:

DB2	DB1	DB0		
0	0	0	= 20	Active Characters/Data Row
0	0	1	= 32	
0	1	0	= 40	
0	1	1	= 64	
1	0	0	= 72	
1	0	1	= 80	
1	1	0	= 96	
1	1	1	= 132	

Horizontal Sync Delay: = N, from 1 to 7 character times (DB0 = LSB, N = 0 Disallowed)

Horizontal Sync Width: = N, from 1 to 15 character times (DB3 = LSB, N = 0 Disallowed)

Skew Bits DB7	DB8	Sync/Blank Delay (Character Times)	Cursor Delay (Character Times)
0	0	0	0
1	0	1	0
0	1	2	1
1	1	2	2

Scans/Frame: 8 bits assigned, defined according to the following equations:
Let X = value of 8 assigned bits. DB0 = LSB)
1) in interlaced mode— scans/frame = 2X + 513. Therefore for 525 scans, program X = 6 (0000110). Vertical sync will occur precisely every 262.5 scans, thereby producing two interlaced fields.
Range = 513 to 1023 scans/frame, odd counts only.
2) in non-interlaced mode—scans/frame = 2X + 256. Therefore for 262 scans, program X = 3 (00000011).
Range = 256 to 766 scans/frame, even counts only.
In either mode, vertical sync width is fixed at three horizontal scans (= 3H)

Vertical Data Start: N = number of raster lines delay after leading edge of vertical sync of vertical start position. (DB0 = LSB)

Data Rows/Frame: Number of data rows = N + 1, N = 0 to 63 (DB0 = LSB)

Last Data Row: N = Address of last displayed data row, N = 0 to 63, ie; for 24 data rows, program N = 23. (DB0 = LSB)

Mode: Register 1, DB7 = 1 established Interlace

Scans/Data Row:

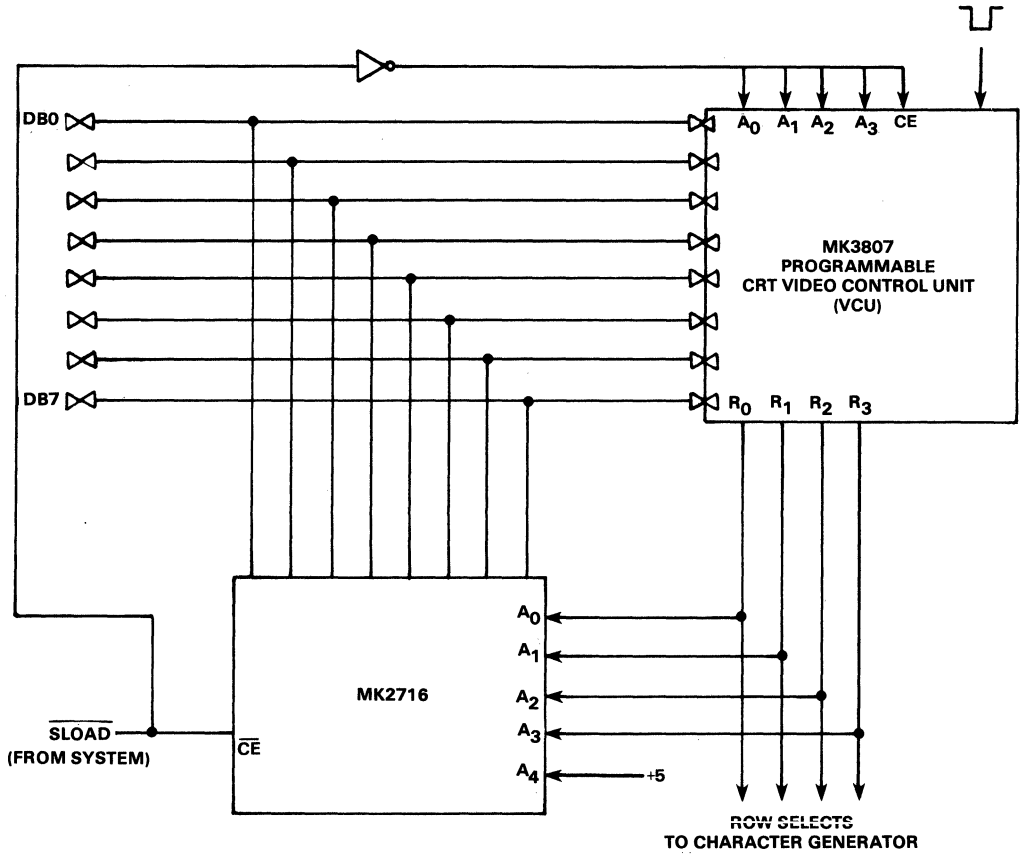
Interlace Mode

Scans per data Row = N + 2. N = 0 to 14, odd or even counts.

Non-Interlace Mode

Scans per Data Row = N + 1, odd or even count, N = 0 to 15.

SELF LOADING SCHEME
Figure 2



OPTIONAL START-UP SEQUENCE

When employing microprocessor controlled loading of the MK3807 VCU's registers, the following sequence of instruction may be used optionally:

ADDRESS	COMMAND
1 1 1 0	Start Timing Chain
1 0 1 0	Reset
0 0 0 0	Load Register 0
.	.
.	.
.	.
0 1 1 0	Load Register 6
1 1 1 0	Start Timing Chain

The sequence of START RESET LOAD START is necessary to ensure proper initialization of the registers.

This sequence is not required if register loading is via either of the Self Load modes.

REGISTER SELECTS/COMMAND CODES

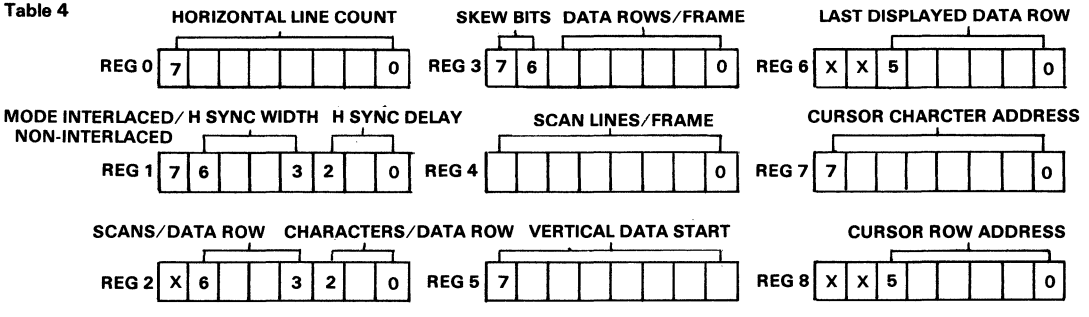
Table 3

A3	A2	A1	A0	Select/Command	Description
0	0	0	0	Load Control Register 0	See Table 4
0	0	0	1	Load Control Register 1	
0	0	1	0	Load Control Register 2	
0	0	1	1	Load Control Register 3	
0	1	0	0	Load Control Register 4	
0	1	0	1	Load Control Register 5	
0	1	1	0	Load Control Register 6	
0	1	1	1	Processor Initiated Self Load	Command from processor instructing MK3807 VCU to enter Self Load Mode (via external PROM)
1	0	0	0	Read Cursor Line Address	
1	0	0	1	Read Cursor Character Address	
1	0	1	0	Reset	Resets timing chain to top left of page. Reset is latched on chip by $\overline{DS}$ and counters are held until released by start command.
1	0	1	1	Up Scroll	Increments address of first displayed data row on page, i.e.; prior to receipt of scroll command—top line = 0, bottom line = 23. After receipt of Scroll Command—top line = 1, bottom line = 0.
1	1	0	0	Load Cursor Character Address[1]	
1	1	0	1	Load Cursor Line Address[1]	
1	1	1	0	Start Timing Chain	Receipt of this command after a Reset or Processor Self Load command will release the timing chain approximately one scan line later. In applications requiring synchronous operation of more than one VCU the dot counter carry should be held low during the $\overline{DS}$ for this command.
1	1	1	1	Non-Processor Self Load	Device will begin self load via PROM when $\overline{DS}$ goes low. The 1111 command should be maintained on A3-0 long enough to guarantee self load. (Scan counter should cycle through at least once). Self load is automatically terminated and timing chain initiated when the all "1's" condition is removed, independent of $\overline{DS}$. For synchronous operation of more than one VCU, the Dot Counter Carry should be held low when the command is removed.

NOTE 1: During Self-Load, the Cursor Character Address Register (REG 7) and the Cursor Row Address Register (REG 8) are enabled during states 0111 and 1000 of the R3-R0 Scan Counter outputs respectively. Therefore, Cursor data in the PROM should be stored at these addresses.

BIT ASSIGNMENT CHART

Table 4



IX

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range ..... 0°C to + 70°C
Storage Temperature Range ..... -55°C to + 150°C
Lead Temperature (soldering, 10 sec.) ..... + 325°C
Positive Voltage on any Pin, with respect to ground ..... + 18.0 V
Negative Voltage on any Pin, with respect to ground ..... -0.3 V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. For example, the bench power supply programmed to deliver +12 volts may have large voltage transients when the AC power is switched on and off. If this possibility exists it is suggested that a clamp circuit be used.

DC CHARACTERISTICS

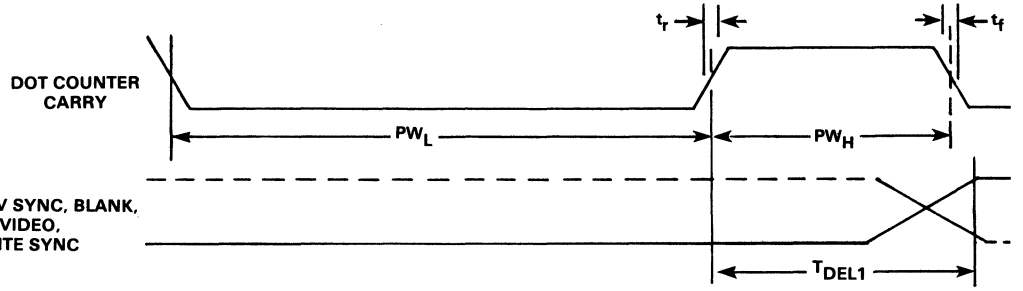
(T_A = 0°C to 70°C, V_{CC} = +5V ± 5%, V_{DD} = +12V ± 5%, unless otherwise noted)

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
INPUT VOLTAGE LEVELS					
Low Level, V_{IL}			0.8	V	
High Level, V_{IH}	V_{CC}-1.5		V_{CC}	V	
OUTPUT VOLTAGE LEVELS					
Low Level - V_{OL} for R0-3			0.4	V	I_{OL}=3.2 ma
Low Level - V_{OL}, all others			0.4	V	I_{OL}=1.6 ma
High Level - V_{OH} for R0-3, DB0-7	2.4				I_{OH}=80μa
High Level - V_{OH} all others	2.4				I_{OH}=40μa
INPUT CURRENT					
Low Level, I_{IL} (Address, CE only)			250	μA	V_{IN}=0.4 V
Leakage, I_{IL} (All inputs except Address, CE)			10	μA	$0 \leq V_{IN} \leq V_{CC}$
INPUT CAPACITANCE					
Data Bus, C_{IN}		10	15	pF	
$\overline{DS}$, Clock, C_{IN}		25	40	pF	
All other, C_{IN}		10	15	pF	
DATA BUS LEAKAGE in INPUT MODE					
I_{DB}			10	μA	$0.4 \leq V_{IN} \leq 5.25$ V
POWER SUPPLY CURRENT					
I_{CC}		80	100	mA	
I_{DD}		40	70	mA	

AC CHARACTERISTICS
(T_A = 70°C)

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
DOT COUNTER CARRY					
frequency	0.5		4.0	MHz	Figure 3
PW_H	35			ns	Figure 3
PW_L	215			ns	Figure 3
t_r, t_f		10	50	ns	Figure 3
DATA STROBE					
PW_{DS}	150ns		10μs		Figure 4
ADDRESS, CHIP ENABLE					
Set-up time	125			ns	Figure 4
Hold time	50			ns	Figure 4
DATA BUS - LOADING					
Set-up time	125			ns	Figure 4
Hold time	75			ns	Figure 4
DATA BUS - READING					
T_{DEL2}			125	ns	Figure 4, CL =50pF
T_{DEL4}	5		60	ns	Figure 4, CL =50pF
OUTPUTS, H0-7, HS, $\overline{VS}$, BL, CRV					
CE-T_{DEL1}			125	ns	Figure 3, CL =20pF
OUTPUTS: R0-3, DR0-5					
T_{DEL3}	*		750	ns	Figure 5, CL =20pF

AC TIMING DIAGRAMS
VIDEO TIMING
Figure 3



IX

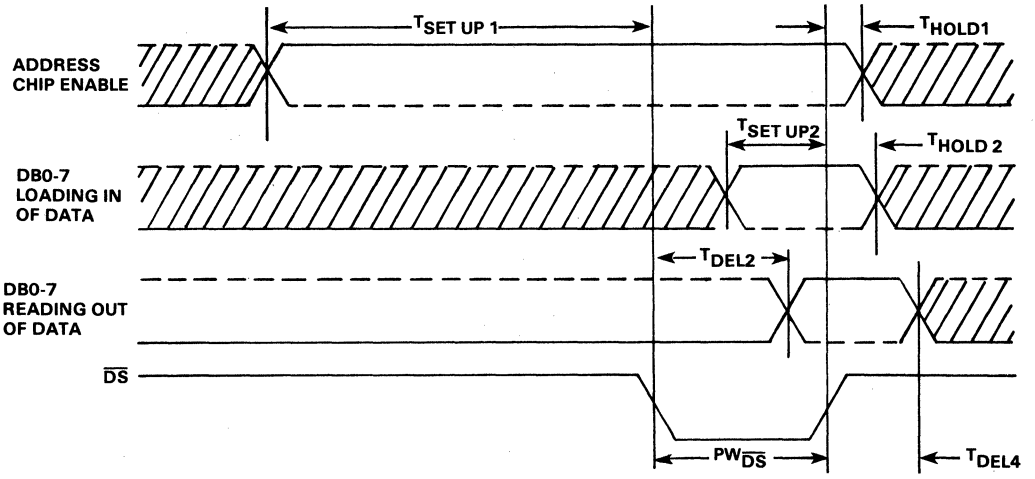
RESTRICTIONS

1. Only one pin is available for strobing data into the device via the data bus. The cursor X and Y coordinates are loaded into the chip by presenting one set of addresses and are output by presenting a different set of addresses. Therefore, the standard WRITE and READ control signals from most microprocessors must be "NORed" externally present a single strobe ($\overline{DS}$) signal to the device.

2. In interlaced mode, the total number of character slots assigned to the horizontal scan must be even to ensure that vertical sync occurs precisely between horizontal sync pulses.

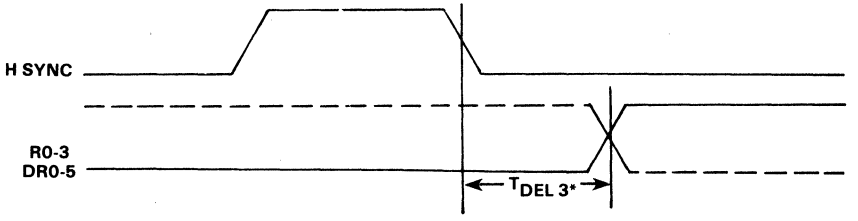
LOAD/READ TIMING

Figure 4



SCAN AND DATA ROW COUNTER TIMING

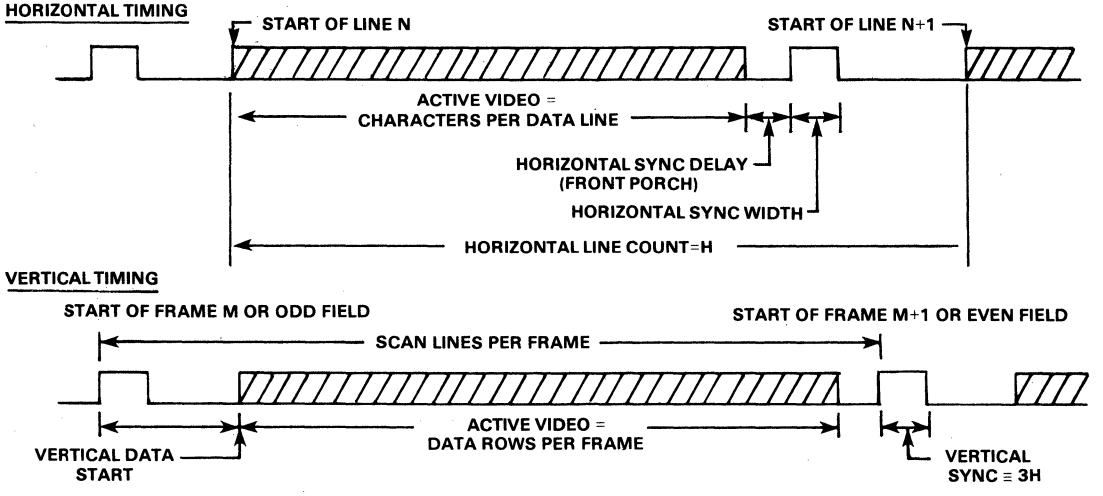
Figure 5



*R0-3 and DR0-5 may change prior to the falling edge of H sync

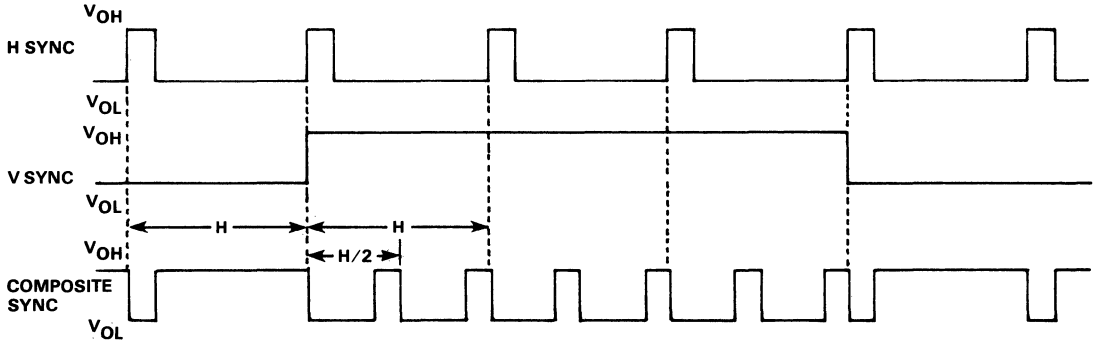
GENERAL TIMING

Figure 6



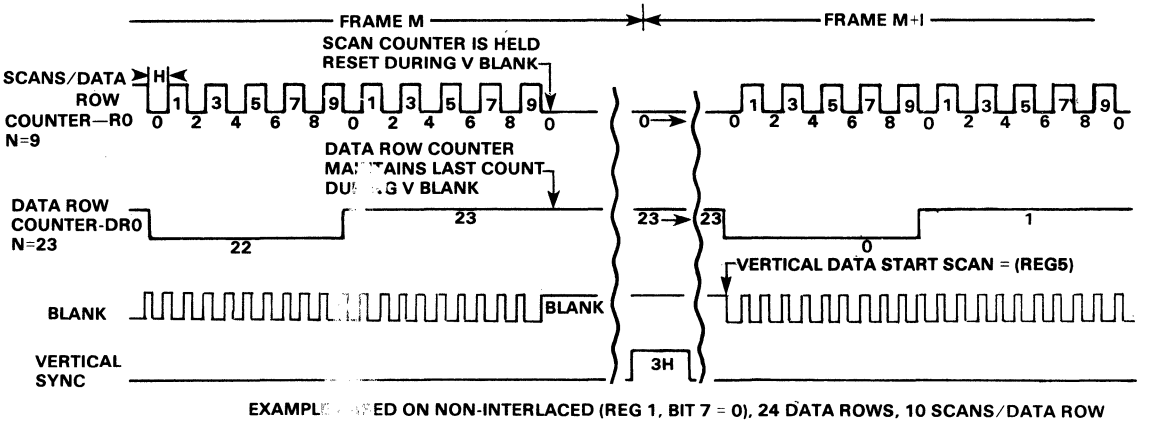
COMPOSITE SYNC TIMING

Figure 7



VERTICAL SYNC TIMING

Figure 8



EXAMPLE BASED ON NON-INTERLACED (REG 1, BIT 7 = 0), 24 DATA ROWS, 10 SCANS/DATA ROW

IX

1982/1983 MICROELECTRONIC DATA BOOK

MOSTEK

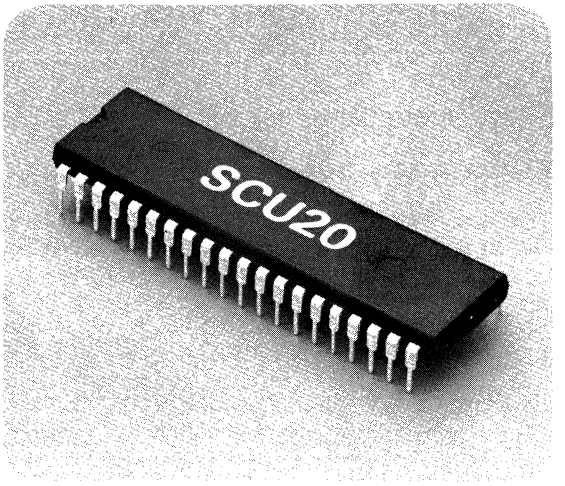
3870 MICROCOMPUTER COMPONENTS

Serial Control Unit SCU20

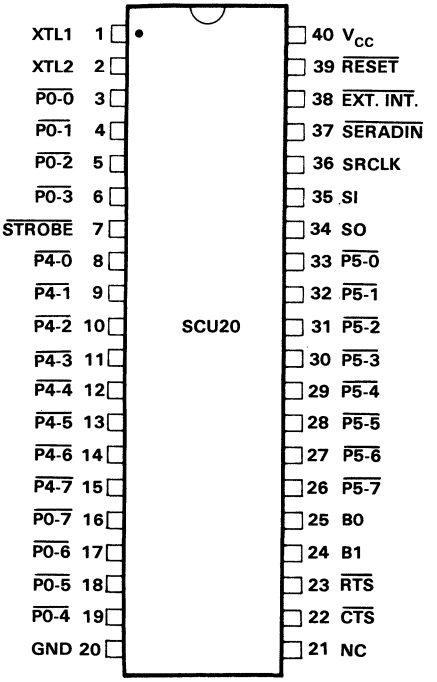
FEATURES

- ☐ Provides programmable remote I/O functions, real time operational capabilities, and standardized network communications on a 40 pin chip.
- ☐ Performs preprogrammed functions on command, including:
  - Byte input and output
  - Bit input and output
  - Set, clear, and toggle selected pins
  - Data access from real time functions
- ☐ Performs real time preprogrammed functions, including:
  - Data log on external interrupt, timer, or host control, up to 63 bytes of data
  - Five Event Counters driven from external interrupt, timer or host control
- ☐ Up to 24 programmable I/O pins
- ☐ Allows user to network up to 255 SCUs on a single communications channel
- ☐ Asynchronous serial data transmission
- ☐ Selectable Baud rate (300, 1200, 2400, or 9600 Baud)
- ☐ Secure, Error resistant data link protocol
- ☐ Requires single +5 volt supply
- ☐ Low power (275mW typ)

SCU20
Figure 1



SCU20 PINOUT
Figure 2



INTRODUCTION

The SCU20 serial control unit is a preprogrammed MK3873 single chip microcomputer. It is a general purpose remote control/data acquisition unit, with 38 preprogrammed functions available to the user.

Communications with the SCU20 take place over an asynchronous half duplex communications channel at 300, 1200, 2400, or 9600 Baud. The communications protocol is efficient and error resistant, and yet easy to implement on the host system.

X

The SCU20 can be used for both monitoring and control systems where remote intelligence is required. It can be configured to provide many different input/output and data acquisition functions through its 24 I/O pins. Such intelligent functions as Data Log and Event Counters allow many different applications that will not burden the host system with constant update requirements.

FUNCTIONAL PIN DESCRIPTION

The SCU20 is housed in a plastic 40 pin dual in-line package.

Figure 2 shows the location of each pin on the SCU20. The following describes the function of each pin.

SCU20 PINOUT DEFINITION

XTL1, XTL2 - Time base inputs for 3.6864 MHz crystal.

$\overline{P0\text{-}0}$ - $\overline{P0\text{-}7}$ - SCU20 port 0 (Bidirectional, active low). SCU20 address input or general purpose data port (see SCU20 Address section).

$\overline{STROBE}$ - Data available strobe for port 4 (output active low).

$\overline{P4\text{-}0}$ - $\overline{P4\text{-}7}$ - SCU20 port 4 (Bidirectional, active low). General purpose data port.

$\overline{P5\text{-}0}$ - $\overline{P5\text{-}7}$ - SCU20 port 5 (Bidirectional, active low). General purpose data port.

SRCLK - Clock signal generated by internal Baud rate generator.

SI - Serial input. Receives serial asynchronous data from the host.

SO - Serial output. Transmits serial asynchronous data to the host.

$\overline{RTS}$ - Request to send (output, active low).

$\overline{CTS}$ - Clear to send (input, active low).

$\overline{RESET}$ - External reset (input, active low).

$\overline{EXT.\ INT.}$ - External interrupt (input, active low).

$\overline{SERADIN}$ - Serial address input/address mode (input, active low. See SCU20 Address section).

B0, B1 - Baud rate select.

V_{CC} - Power supply, 5 volts.

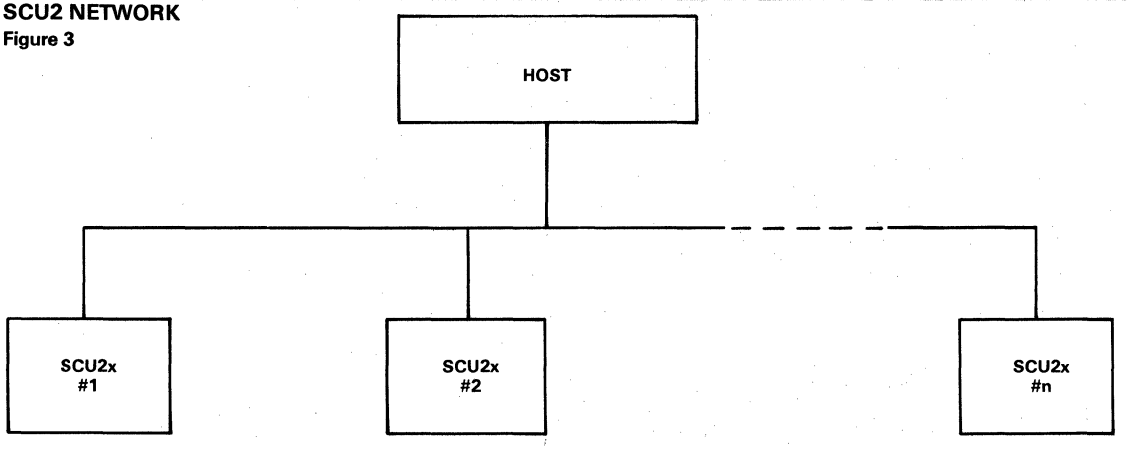
GND - Power supply ground.

SCU2 NETWORK

The SCU2 Network is a serial linked network of devices in the SCU2 family. All communications are via a common serial link using the SCU2 family communications protocol. In this way, a distributed control facility may be easily implemented from standard parts, and controlled by the host computer via the serial link.

Figure 3 illustrates the SCU2 Network.

SCU2 NETWORK
Figure 3



Each SCU2x in the network has an individual address to which it will respond. All SCU2x devices in the network are slave processors to the host, and are unable to initiate communications except in response to the host.

When the system is initialized, all SCU2x devices are in the listen mode, and are performing no functions. The host will issue an inquiry command to each device. Once all devices have been queried, the host will issue commands to each device to set up the particular operational parameters required of it. When this has been done, the host may then use the devices to control equipment, measure values, etc., by issuing commands and receiving responses.

Unless issuing a response, the SCU2x is always in the listen mode. If a command has been sent to an SCU2x, a response is expected within a specific time period. If none is forthcoming, it means that the command transmitted was not successfully received by the device. In this case, the host must take steps either to notify the operator or to retransmit the command.

If a system error occurs in the host, it may suspend operation of the entire network by transmitting the network reset command which causes all devices to be reset. This is the only command that does not require a specific SCU2x address as part of the command. It uses the system reset address which is recognized by each device.

SCU20 ADDRESS

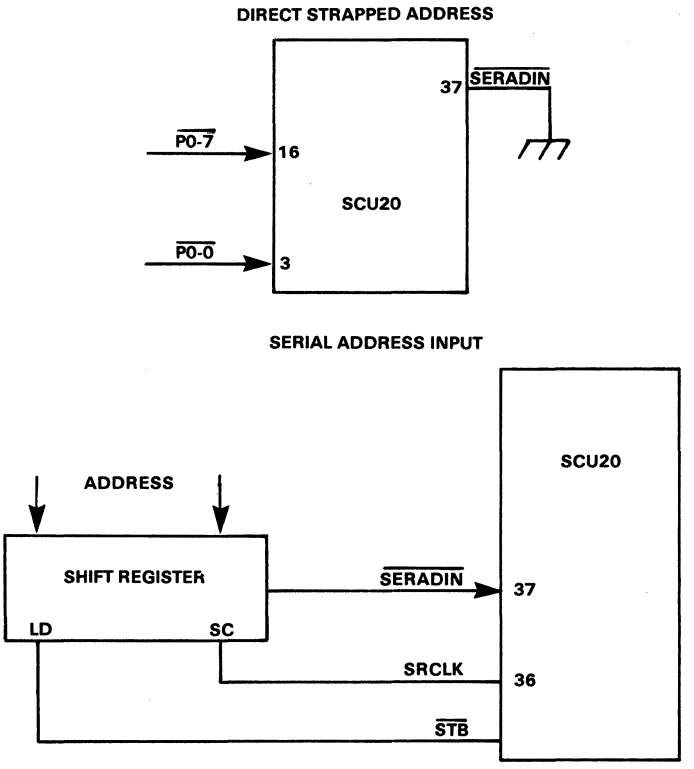
The address to which the SCU20 responds may be established in one of two ways.

The first mode is the Direct Strapped Address mode, and is enabled by tying the $\overline{\text{SERADIN}}$ pin directly to ground. In this mode, the SCU20 address is strapped at port 0. Because of this, port 0 is not available as a general purpose I/O port.

The second mode is the Serial Address Input mode. The $\overline{\text{SERADIN}}$ pin is used to input the address as a serial 8-bit stream from a shift register. SRCLK is used as a shift clock for this operation. The $\overline{\text{STROBE}}$ signal is used at initialization time to cause the address to be loaded into the shift register before shifting begins. In the Serial Address mode, port 0 becomes available for use as a general purpose data I/O port.

Figure 4 illustrates both methods of establishing the SCU20 address.

SCU20 ADDRESS ESTABLISHMENT
Figure 4



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SCU20 COMMUNICATIONS

The SCU20 communicates with the host computer over a half duplex asynchronous serial link. The communications protocol is simple, yet error resistant.

The general form of the communication message is as follows:

HDR	ADDR	CMD	DATA	DATA	• • • •	LRC

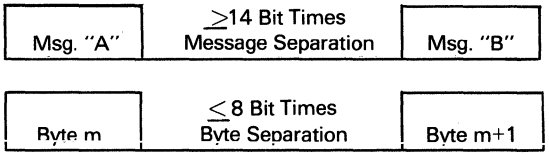
HDR - Message header. Hex '01' indicates a command message from the host; Hex '02' indicates a response from the SCU20.

ADDR - SCU20 Address. Indicates which SCU20 the message is for, or originates from.

CMD - Command. Indicates the function to be performed.

DATA - Any data that may be required by the particular command.

LRC - Linear Redundancy Check.



Messages are to be transmitted in block mode, with a message separation of at least 14 bit times. Interbyte separations should be no more than 8 bit times within a message.

A message from the host to the SCU20 will generate a response if there is no transmission error. If any transmission error is detected, no response will be made.

Possible transmission errors are LRC errors, parity errors, interbyte separation errors, or intermessage separation errors.

BAUD RATE SELECTION

The serial Baud rate is selected by a strapped option on the SCU20. Those options are listed below:

BAUD RATE	B0 (Pin 25)	B1 (Pin 24)
300	Low	Low
1200	Low	High
2400	High	Low
9600	High	High

MODEM SIGNALS

$\overline{RTS}$ and $\overline{CTS}$ are provided to facilitate handshaking with modems. Just prior to responding to a valid command, $\overline{RTS}$ will go to logic 1, indicating that the SCU20 is ready to send data back to the host. $\overline{CTS}$ is an input to the SCU20 that is tested after $\overline{RTS}$ goes active to determine if the SCU20 may begin transmitting data.

PARALLEL I/O PORTS

The SCU20 has a minimum of 2 parallel I/O ports and a maximum of 3 available for general use, depending on the address selection mode chosen. For each of these ports, there exist 2 registers that control and modify the I/O to and from the ports. These are the Data Direction Register (DDR) and the Mask Register(MR).

The Data Direction Register defines the usage of each pin in the port. If a bit is set to 0, then the corresponding pin is used as input. If a bit is set to 1, then the corresponding pin is used as an output. When a port is read, all bits are sampled for input whether or not they are marked for input. When a port is written to, however, only those pins declared as output will be modified.

The Mask Register provides a data mask that may be applied to the input data before transmission to the master. The mask is established once and may be used repeatedly before being changed by establishing a new mask value. If a pin is to be available upon read, the corresponding bit in the mask register is set to 1, while a pin that is to be masked out will have its mask bit set to 0.

SCU20 PREPROGRAMMED FUNCTIONS

The SCU20 has a variety of preprogrammed functions available to the user. Each of these functions addresses a different general area of application such that the SCU20 is truly a general purpose device.

PORT COMMANDS

There are several commands which allow the host to manipulate the 8-bit general purpose I/O ports. The host may load data into any one or all of the ports, may read any or all of the ports with or without a mask, may read with a new mask, or may read using the last defined mask. When data is loaded, the resulting port state is returned in the response message.

LOGIC COMMANDS

In addition to performing data I/O with the ports, the host may perform logical operations with the ports and data from the host. These commands allow the host to AND, OR, or Exclusive OR (XOR) data with any or all of the ports, and output the result to the ports. The resultant output is returned in the command response message.

BIT COMMANDS

These commands allow the host to SET, CLEAR, TEST, or TOGGLE bits in the ports by specifying bit number (0 - 24). Any pin that is declared as an input will not be changed.

EVENT COUNTERS

There are 5 Event Counters defined in SCU20. They are 16 bit up counters, and are driven by the timer, the external interrupt, or by host command. They may be used as simple event counters, or may be used in conjunction with the Data Log, and Pulse functions.

DATA LOG

The Data Log function allows the user to command the SCU20 to log data from the ports specified in the command, and store the data in the on-board RAM. Up to 63 bytes of data may be accumulated in the log, and may be captured on external interrupt, timer, or host command through use of an Event Counter.

Data from the Log is transmitted back to the host in a single read command burst.

CONTROL COMMANDS

There are several commands to control the SCU20 as well as the entire SCU2 network. These commands provide the host with the ability to query each individual SCU2x on the network for its type, the last message it sent, and for detailed error codes. In addition, there are commands that allow the host to reset an individual device, or to cause the entire SCU2 network to reset with a single command.

ERROR PROCESSING

The SCU20 does not provide a "negative acknowledge" response to command stream errors. Those errors are parity errors, LRC errors, unidentifiable commands, overrun, or violation of the separation specifications as described earlier.

In some cases, the SCU20 will provide error response to functional errors in commands that have been recognized. This response will be either a "NAK0" or a "NAK3" as specified for the command. "NAK0" is the hex value H'FB', and "NAK3" is the hex value H'FE'.

H'2'	ADDR	H'FB' or H'FE'	LRC

SCU20 COMMANDS

Figure 5 gives a complete list of the commands and functions available to the SCU20. For a full description of these commands and their use, refer to the SCU20 Operations Manual.

SCU20 COMMANDS
Figure 5

FUNCTION	COMMAND CODES	# DATA BYTES (CMD)	# DATA BYTES (RESP)	ERR COD RET
** PORT COMMANDS **				
Load Data Direction Registers	1E	3	0	-
Load Port (0, 4, 5)	00,01,02	1	1	-
Load All Ports	03	3	3	-
Read Port (0, 4, 5)	04,05,06	0	1	-
Read All Ports	07	0	3	-
Read Port Masked, Mask Provided	08,09,0A	1	1	-
Read All Ports, Masks Provided	0B	3	3	-
Read Port using Previous Mask	0C,0D,0E	0	1	-
Read All Ports using Previous Masks	0F	0	3	-

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... -20°C to +85°C
Storage Temperature ..... -65°C to +150°C
Voltage on any Pin With Respect to Ground
(Except open drain pins and TEST) ..... -1.0 V to +7 V
Voltage on TEST with Respect to Ground ..... -1.0 V to + 9 V
Voltage on Open Drain Pins With Respect to Ground ..... -1.0 V to +13.5 V
Power Dissipation ..... 1.5 W
Power Dissipation by any one I/O pin[2] ..... 60 mW
Power Dissipation by all I/O pins[2] ..... 600 mW

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING VOLTAGES AND TEMPERATURES

Operating Voltage V_{CC} ..... +5 V ± 10%
Operating Temperature T_A ..... 0° - 70°C

AC CHARACTERISTICS

T_A, V_{CC} within specified operating range.
I/O Power Dissipation ≤ 100 mW (Note 2)

SIGNAL	SYM	PARAMETER	MIN	MAX	UNIT	NOTES
XTL1 XTL2	t_o	Time Base Period, all clock modes	250	500	ns	4 MHz - 2 MHz 3.6864 required for
	$t_{ex(H)}$	External clock pulse width high	90	400	ns	standard baud
	$t_{ex(L)}$	External clock pulse width low	100	400	ns	frequencies
Φ	t_Φ	Internal Φ clock	$2t_O$			
$\overline{\text{STROBE}}$	$t_{I/O-s}$	output valid to $\overline{\text{STROBE}}$ delay	3tΦ -1000	3tΦ +250	ns	I/O load = 50 pF + 1 TTL load
	t_{sL}	$\overline{\text{STROBE}}$ low time	8tΦ -250	12tΦ +250	ns	$\overline{\text{STROBE}}$ load = 50 pF + 3TTL loads
$\overline{\text{RESET}}$	t_{RH}	$\overline{\text{RESET}}$ hold time, low	6tΦ +750		ns	
	t_{RPOC}	$\overline{\text{RESET}}$ hold time, low for power clear	power supply rise time +0.1		ms	
$\overline{\text{EXT INT}}$	t_{EH}	$\overline{\text{EXT INT}}$ hold time in active and inactive state	6tΦ +750		ns	To trigger interrupt

CAPACITANCE

T_A = 25°C
All Part Numbers

SYM	PARAMETER	MIN	MAX	UNIT	NOTES
C_{IN}	Input capacitance; I/O, $\overline{\text{RESET}}$, $\overline{\text{EXT INT}}$		10	pF	unmeasured pins grounded
C_{XTL}	Input capacitance; XTL1, XTL2	23.5	29.5	pF	

AC CHARACTERISTICS FOR SERIAL I/O PINS

T_A, V_{CC} within specified operating range.
I/O Power Dissipation ≤ 100 mW (Note 2)

SIGNAL	SYM	PARAMETER	MIN	MAX	UNIT	CONDITIONS
SRCLK	$t_{r(SRCLK)}$	Serial Clock Rise Time	60		ns	0.8 V - 2.0 V C_L = 100 pf
	$t_{f(SRCLK)}$	Serial Clock Fall Time	30		ns	2.4 V - 0.4 V C_L = 100 pf

DC CHARACTERISTICS

T_A, V_{CC} within specified operating range.
I/O Power Dissipation ≤ 100 mW (Note 2)

SYM	PARAMETER	MIN	MAX	UNIT	DEVICE
I_{CC}	Average Power Supply Current		103	mA	SCU20 Outputs Open
P_D	Power Dissipation		485	mW	SCU20 Outputs Open

X

DC CHARACTERISTICS

T_A, V_{CC} within specified operating range
I/O Power Dissipation ≤ 100 mW (Note 2)

SYM	PARAMETER	MIN	MAX	UNIT	CONDITIONS
V_{IHEX}	External Clock input high level	2.4	5.8	V	
V_{ILEX}	External Clock input low level	-.3	.6	V	
I_{IHEX}	External Clock input high current		100	μA	$V_{IHEX} = V_{CC}$
I_{ILEX}	External Clock input low current		-100	μA	$V_{ILEX} = V_{SS}$
$V_{IHI/O}$	I/O input high level	2.0	5.8	V	standard pull-up (1)
		2.0	13.2	V	open drain (1)
V_{IHR}	Input high level, $\overline{\text{RESET}}$	2.0	5.8	V	standard pull-up (1)
		2.0	13.2	V	No pull-up
V_{IHEI}	Input high level, $\overline{\text{EXT INT}}$	2.0	5.8	V	standard pull-up (1)
		2.0	13.2	V	No pull-up
V_{IL}	I/O ports, $\overline{\text{RESET}}$[1], $\overline{\text{EXT INT}}$[1] input low level	-.3	.8	V	(1)
I_{IL}	Input low current, I/O ports and $\overline{\text{EXT IN}}$		-1.6	mA	$V_{IN} = 0.4$ V
I_L	Input leakage current, $\overline{\text{RESET}}$ input		+10 -5	μA μA	$V_{IN} = 13.2$ V $V_{IN} = 0.0$V
I_{OH}	Output high current, I/O ports	-100		μA	$V_{OH} = 2.4$ V
		-30		μA	$V_{OH} = 3.9$ V
I_{OL}	Output low current, I/O ports	1.8		mA	$V_{OL} = 0.4$ V
I_{OHS}	$\overline{\text{STROBE}}$ Output High current	-300		μA	$V_{OL} = 2.4$ V
I_{OLS}	$\overline{\text{STROBE}}$ output low current	5.0		mA	$V_{OL} = 0.4$ V

DC CHARACTERISTICS FOR SERIAL PORT I/O PINS

T_A, V_{CC} within specified operating range
I/O Power Dissipation ≤ 100 mW (Note 2)

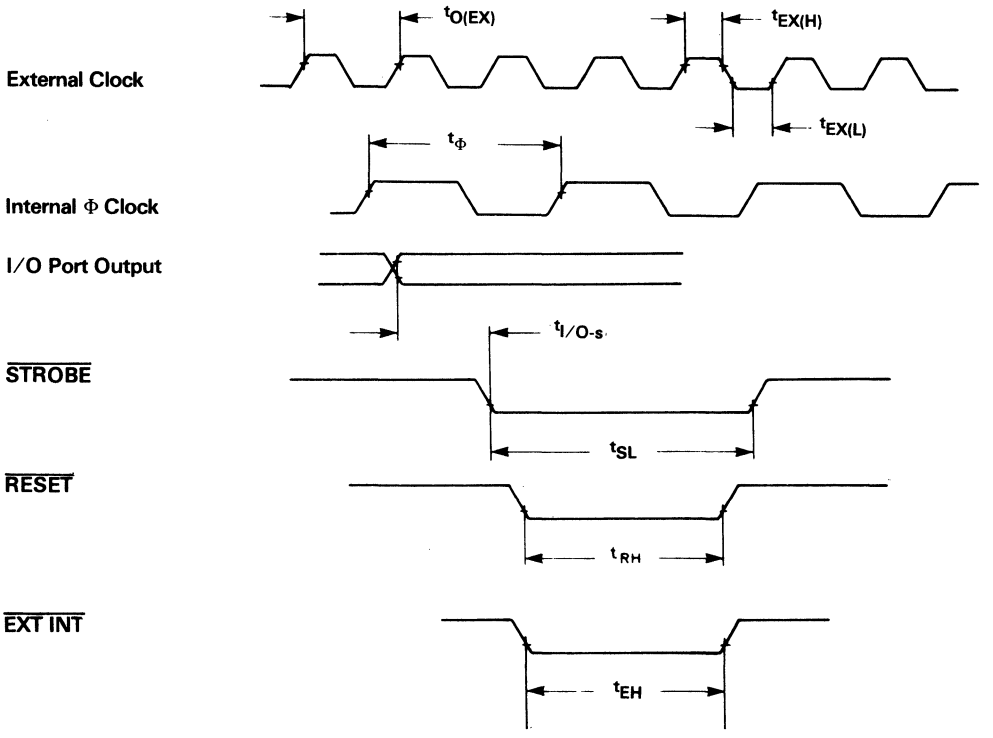
SYM	PARAMETER	MIN	MAX	UNIT	TEST CONDITIONS
V_{IHS}	Input High for SI	2.0	5.8	V	
V_{ILS}	Input Low level for SI	-.3	.8	V	
I_{ILS}	Input low current for SI		-1.6	mA	V_{IL} = 0.4 V
I_{OHSO}	Output High Current SO	-100 -30		μA μA	V_{OH} = 2.4 V V_{OL} = 3.9 V
I_{OLSO}	Output Low Current SO	1.8		mA	V_{OL} = 0.4 V
I_{OHSRC}	Output High Current, SRCLK	-300		μA	V_{OH} = 2.4 V
I_{OLSRC}	Output Low Current, SRCLK	5.0		mA	V_{OL} = 0.4 V

NOTES

1. RESET and EXT INT have internal Schmitt triggers giving minimum .2 V hysteresis.
2. Power dissipation for I/O pins is calculated by $\Sigma(V_{CC} - V_{IL})(I_{IL}) + \Sigma(V_{CC} - V_{OH})(I_{OH}) + \Sigma(V_{OL})(I_{OL})$

AC TIMING DIAGRAM

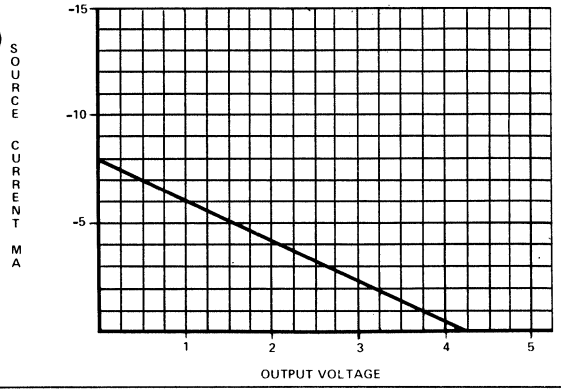
Figure 6



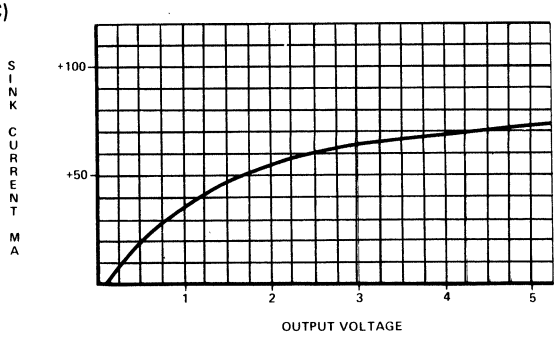
Note: All AC measurements are referenced to V_{IL} max., V_{IH} min., V_{OL} (.8v), or V_{OH} (2.0v).

X

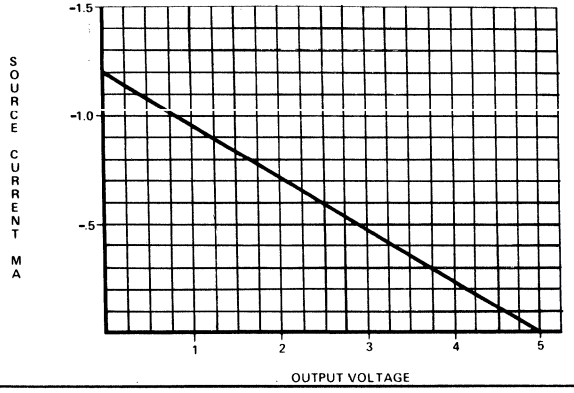
STROBE SOURCE CAPABILITY
(TYPICAL AT V_{CC} = 5V, T_A = 25°C)
Figure 7



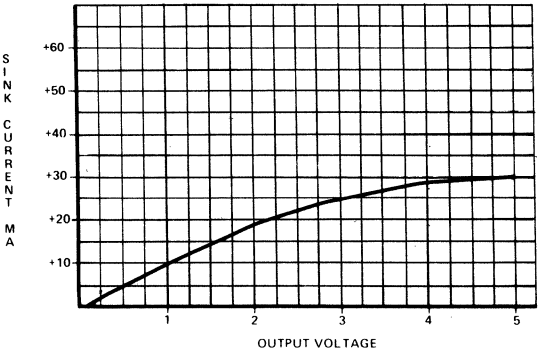
STROBE SINK CAPABILITY
(TYPICAL AT V_{CC} = 5V, T_A = 25°C)
Figure 8



STANDARD I/O PORT SOURCE CAPABILITY
(TYPICAL AT V_{CC} = 5V, T_A = 25°C)
Figure 9

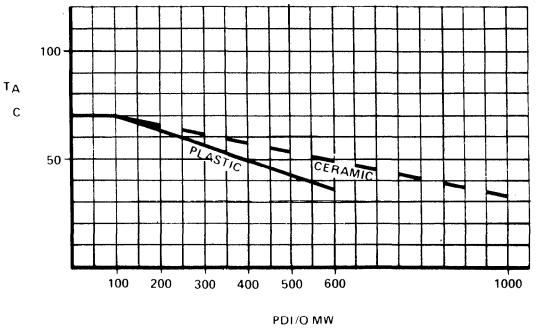


I/O PORT SINK CAPABILITY
(TYPICAL AT V_{CC} = 5V, T_A = 25°C)
Figure 10



MAXIMUM OPERATING TEMPERATURE VS. I/O POWER DISSIPATION

Figure 11



ORDERING INFORMATION

An example of the device order number is shown below.

MK 95010 N - 1 0

Power Supply Tolerance	0 = 5 V ±10% 5 = 5 V ± 5%
Operating Temperature Range	0 = 0°C - +70°C 1 = -40°C - +85°C
Package Types	P = Ceramic N = Plastic
Customer/Code Specific Number	

X

1982/1983 MICROELECTRONIC DATA BOOK

MOSTEK®

DEVELOPMENT SYSTEM PRODUCTS

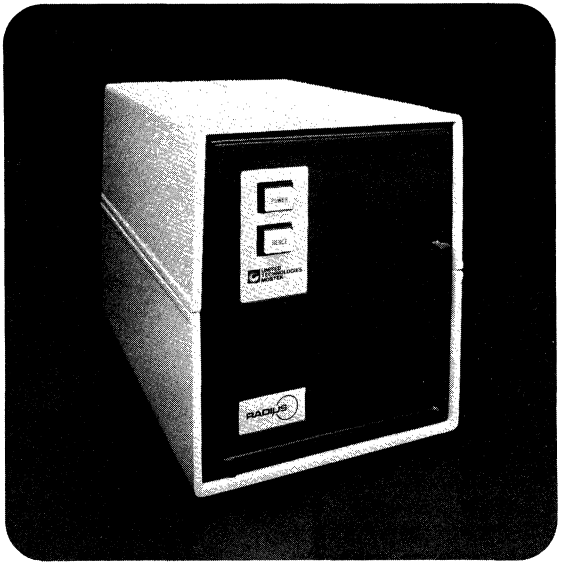
RADIUS™

Remote Development Station

FEATURES

- ☐ Microcomputer development with host computer
  - Software development on the host
  - Download to RADIUS
  - Hardware debug and software integration on RADIUS
- ☐ Utilizes standard Mostek SDE series AIM modules
- ☐ Host software supplied
  - Preconfigured for selected hosts
  - Reconfigurable for other hosts
- ☐ Upload/download performed with error tolerant protocol
- ☐ Emulation possible while disconnected from the host
- ☐ Serial I/O Baud rate up to 9600
- ☐ Supports optional line printer and PROM programmer
- ☐ Self-diagnostic test

RADIUS
Figure 1



INTRODUCTION

Mostek RADIUS - Remote Access Development and Integration μcomputer System - is a state-of-the-art microcomputer development system, designed specifically to be used in a host computer environment. RADIUS provides software development capability via the host computer and hardware development and software integration using the advanced in-circuit-emulation capability of Mostek AIM modules.

RADIUS is installed between the user's CRT terminal and the host computer via an ASCII RS-232 serial interface. See Figure 2. It can be operated in any of three modes: Transparent, Local or Utility.

In Transparent Mode, the user can:

- Perform any function that can be performed on the host computer. RADIUS becomes completely transparent to the user.

In Local Mode, the user can:

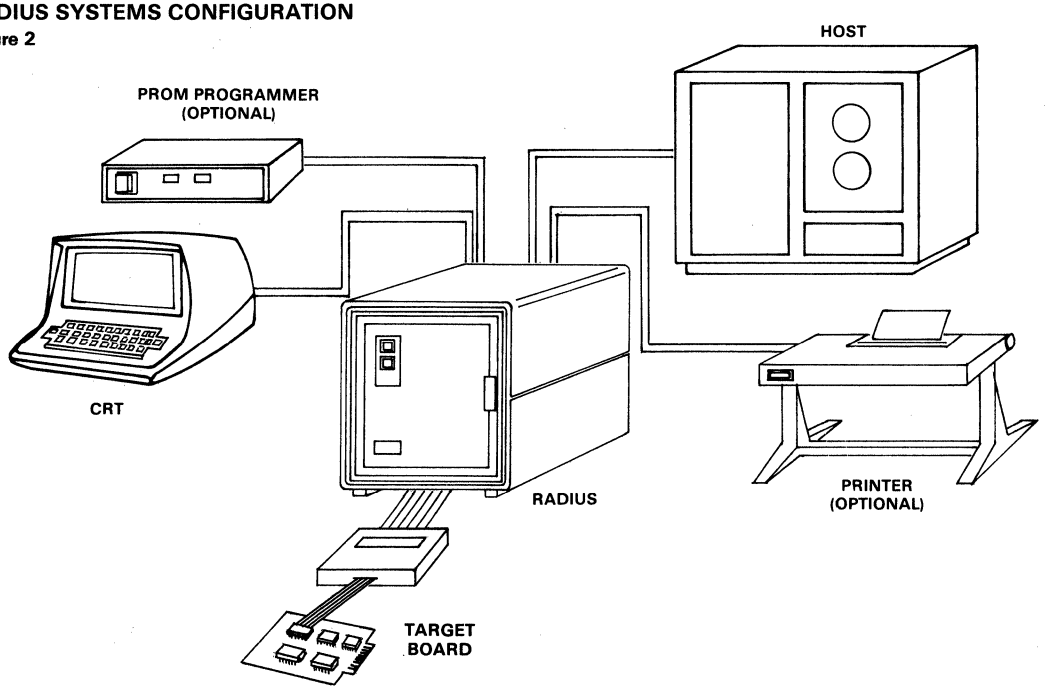
- Set optional Baud rates and special RADIUS control characters
- Perform self diagnostics on RADIUS

In Utility Mode, the user can:

- Run the host components of the RADIUS Utility Packages (i.e. AIM-Z80BE, AIM-7XE, Line Printer Utility, PROM Programmer Utility, etc.).
- Perform hardware debug and software integration.

RADIUS has no mass storage. Instead it uses the mass storage capabilities of the host. Once the user's target program is downloaded, the user has the option of disconnecting the RADIUS from the host. This allows the user to save connect time and long distance charges.

RADIUS SYSTEMS CONFIGURATION
Figure 2



RADIUS can be configured in a single-user environment or in a multi-user environment, in which several RADIUS units are connected to an appropriate host and operated simultaneously, performing entirely separate jobs. This configuration supports the development of multiple microprocessor/microcomputer systems. See Figure 3.

DEVELOPMENT SYSTEM

RADIUS is a cost effective microcomputer development tool. It consists of an integrated cabinet, power supply, I/O panel, and a Z80 based processor module with four serial I/O ports.

RADIUS is supplied with a host communications software package configured for several popular mini/microcomputer systems. (See ordering information.) A user rehostable version is available for other host computers. Additional preconfigured versions of the RADIUS host software will be provided in the future.

RADIUS HARDWARE FEATURES

RADIUS consists of a structural foam cabinet, Z80 CPU/Memory/IO board, and a power supply board. The user can add AIM-Z80BE or AIM-7XE modules to RADIUS to perform the full range of real time in-circuit emulation needed for hardware development and software integration. Future AIM products will be completely supported on RADIUS.

The cabinet is divided into two compartments: the power supply compartment on the left and the processing compartment on the right. The processing compartment can house up to five boards: a Z80 CPU/Memory board, two AIM modules boards, and two slots for future expansion.

The CPU/Memory board contains:

- Z80 CPU
- 64 Kbyte internal systems memory
- Four SIO ports;
  - one dedicated to user terminal, one to the host computer, and two for optional printer and PROM programmer
  - RADIUS supports 11 standard Baud rates from 50 to 9600 Baud

RADIUS SOFTWARE FEATURES

- Local mode to set options on RADIUS and to perform local diagnostics
- Most link parameters set at host configuration time
- Full AIM command set available
- AIM packages can run command files from the host
- AIM packages can log all terminal output to the host
- Progress of download/upload indicated on CRT
- Protocol re-transmits messages upon line error
- Self-explanatory error messages
- Translators to convert TEKHEX, F8HEX, and INTELHEX object formats to Mostek HEX
- Local PROM programming (optional)
- Local printing (optional)
- Self diagnostic test

RADIUS local mode provides the following commands:

- HELP
- PORT
- MEMORY
- OPTIONS
- DIAGNOSE
- QUIT

SPECIFICATIONS

The power supply board has single phase AC input at 47 Hz to 63 Hz for the following voltage ranges:

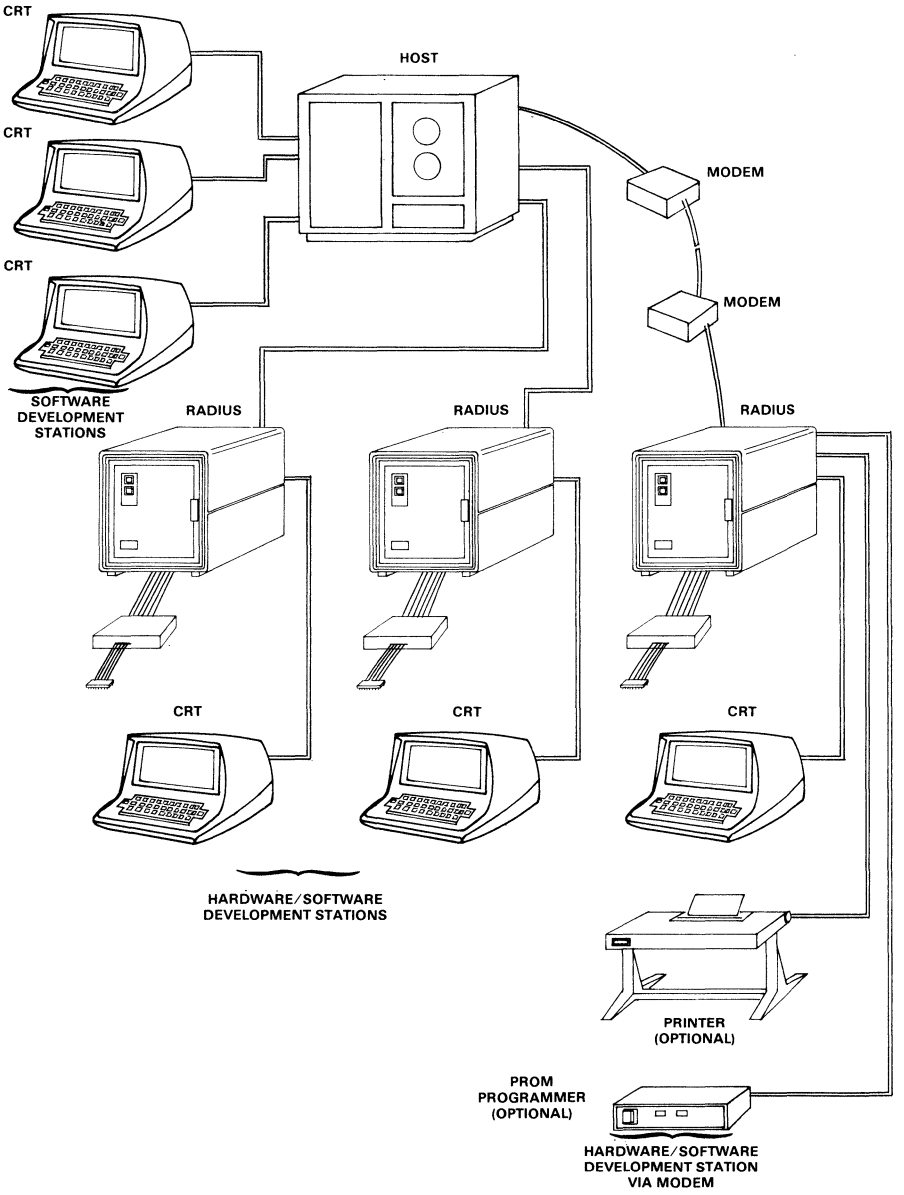
- 95 V to 132 V
- 190 V to 264 V

The approximate dimensions are:

- Width: 9.2"
- Height: 10.8"
- Depth: 12.6"

RADIUS INSTALLATION IN A MULTI-USER ENVIRONMENT

Figure 3



ORDERING INFORMATION

For detailed ordering information refer to the Development System Products Ordering Guide.

MOSTEK®

DEVELOPMENT SYSTEM PRODUCTS

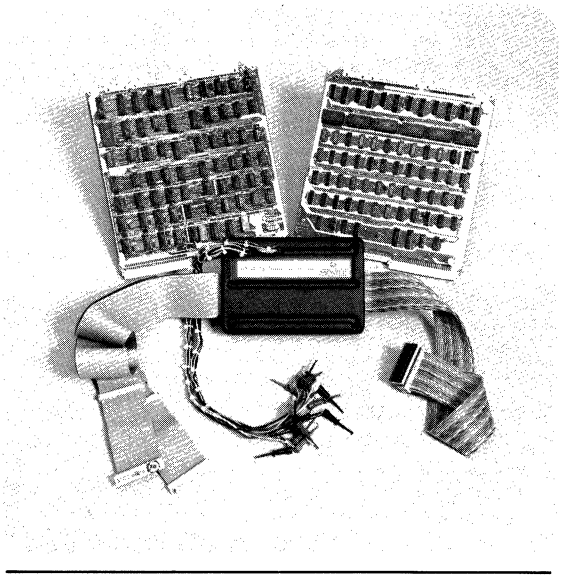
AIM-Z80BE

Application Interface Module

FEATURES

- ☐ Direct interface to Mostek's MATRIX-80SDS, SYS-80F, and RADIUS development systems
- ☐ In-circuit emulation of the Z80 microprocessor
- ☐ Real-time execution (1-6 MHz with no wait states)
- ☐ Flexible breakpoints (one hardware, eight software, and one timer)
- ☐ Single-step execution
- ☐ 16 K bytes of emulation RAM
- ☐ Memory mappable into target or AIM system memory in 256 byte blocks
- ☐ Illegal write-to-memory detection
- ☐ Non-existent memory mapping and access detection
- ☐ Forty-eight-channel-by-1024-words history memory for tracing bus events
- ☐ T-state timer to measure execution time
- ☐ English-oriented command structure
- ☐ Disassembly of instructions
- ☐ System configuration parameters can be saved for future use

AIM-Z80BE PRODUCTS
Figure 1



GENERAL DESCRIPTION

AIM-Z80BE is an advanced development tool which provides debug assistance for both software and hardware via in-circuit-emulation of the Z80 microprocessor. Use of the AIM-Z80BE is transparent to the user's final system configuration (referred to as the "target"). No memory space or user ports are used, and all signals, including $\overline{\text{RESET}}$ $\overline{\text{INT}}$, and NMI are functional during emulation. No memory wait states are required.

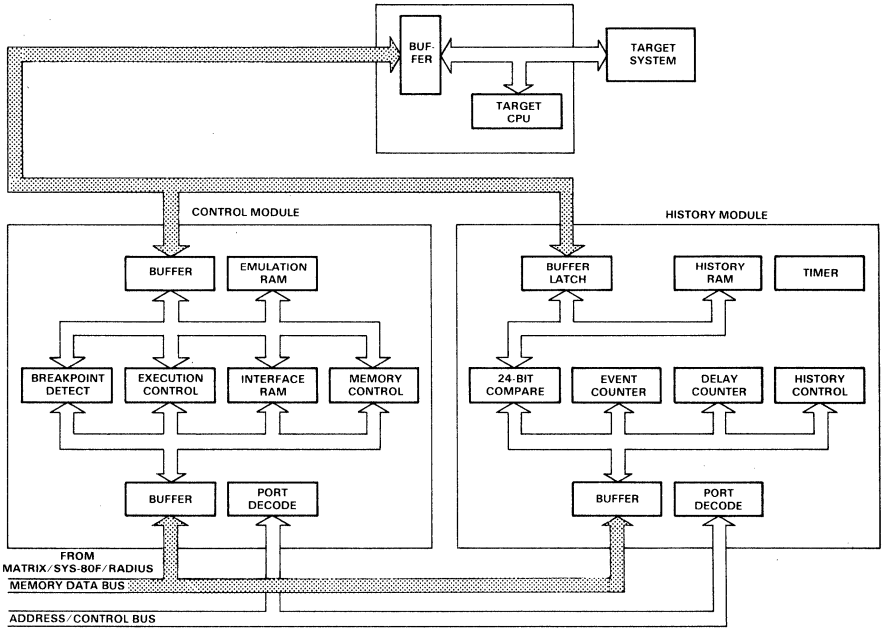
Single-step circuitry allows the user to execute target instructions one at a time to see the exact effect of each instruction. Single step is functional in both ROM and RAM. Up to 16 K bytes of emulation RAM can be used to emulate the target microprocessor RAM or ROM. Thus, debugging can begin before the user system is completely configured with memory.

Breakpoint-detect circuitry allows real-time execution to proceed to any desired point in the user's program and then terminate execution. All CPU status information and register contents can be displayed for the user and saved for later continuation of execution or single-stepping. Real-time execution may be terminated by the user at any time. EVENT and DELAY counters associated with the hardware breakpoint give added flexibility for viewing the exact point of interest in the user's program.

A forty-eight channel history memory records up to 1024 bus transactions. The address bus, data bus, control signals, and 18 external probes may be logged into the history memory and later displayed by the user.

AIM-Z80BE BLOCK DIAGRAM

Figure 2



BLOCK DIAGRAM DESCRIPTION

The Z80 emulation system is composed of two boards, the Control Board and the History Board, as shown in Figure 2. These boards are attached to a Buffer module which contains the target CPU and plugs directly into the target system CPU socket. Address, data, and control signals are buffered by the Buffer module and cabled to the Control and History Boards installed in the development system.

The Control Board has the circuitry for detecting the breakpoint condition(s) and forces program execution to begin in a separate System Interface RAM. The System Interface RAM is loaded with an interface program and is shadowed into the target memory space. This control program makes the target CPU a slave to the development system. When the user desires to resume execution of his program, the control program activates the execution control circuit and execution resumes at the desired address. The Control board contains 16 K bytes of emulation RAM, which may be mapped into any address space required by the target system. Alternatively, if the user's system has memory available, he may use that as his target memory instead of the memory on the Control board.

The History board has a 24-bit comparator circuit, an EVENT counter, and a DELAY counter to detect a hardware breakpoint condition. The 48-channel-by-1024-word history RAM is controlled by the History control circuit.

The Timer circuit is used to count target processor clocks for logging elapsed time and generating the timer breakpoint.

USING THE AIM-Z80BE

The Control and History boards of AIM-Z80BE are installed directly into the development system. To complete the emulation system the Buffer module is used as a buffer interface between the first two boards and the target system's Z80 CPU socket.

The program which controls the AIM-Z80BE emulator system is AIMZ80. After execution of AIMZ80 is started, the program takes control of the AIM-Z80BE emulation system. The user can then initialize the target system and use the AIMZ80 commands to load, test, and debug the target program.

AIMZ80 SOFTWARE

AIMZ80 is the software which operates the AIM-Z80BE emulation system in the Mostek MATRIX-80SDS or SYS-80F disk system or the RADIUS development tool. Target system programs may be developed on a Mostek disk system by use of the appropriate assembler. Programs may be developed for RADIUS cross products supplied by Mostek or other vendors. The AIM software is supplied on a variety of media for use with Mostek disk-based development systems and with different host systems for RADIUS. The commands available in AIMZ80 are summarized below. Each command also has a "short form" which allows abbreviated input with fewer keystrokes.

BATCH	Read AIM commands from a file
BREAK	Display and set breakpoints (8 software, 1 hardware, and 1 timer breakpoint)
CLEAR	Clear one breakpoint or all breakpoints
COPY	Copy one block of memory to another block
DISABLE	Disable target CPU interrupts
DISASSEMBLE	Display and/or update instructions
DUMP	Dump a block of memory to a file
	Dump the memory map to a file
ENABLE	Enable target CPU interrupts
EXECUTE	Start or continue execution of the target program
FILL	Fill memory with a data byte
GET	Load a target program into memory
	Load the target memory map from a file
HEXADECIMAL	Perform hexadecimal arithmetic
HELP	Display a menu of commands for the user
HISTORY	Set history logging options
INIT	Reinitialize target handshake
LOCATE	Locate a pattern in a memory block
LOG	Log all console output to a file
MAP	Map the block of memory as target supplied, AIM system supplied, or non-existent, and write protected or not write protected
MEMORY	Display and/or update memory
OFFSET	Set an offset value for relative module debugging
PORT	Display and update a port on the target CPU
	Output a value to a port without reading it
QUIT	Return to the resident operating system
RAMTEST	Perform a test on the target RAM
REGISTER	Display and/or update the target CPU registers
STATUS	Display the current status of the AIM system
STEP	Perform a single or multi-step execution
TRACE	Display the contents of the history RAM
TRANSPARENT	Allows the RADIUS user to temporarily access the host
VERIFY	Verify the contents of a block of memory with another block or with a file.

SPECIFICATIONS

Target operating frequency: 1 to 6 MHz (MK78204)

Target interface: all signals meet the specifications for the Z80 with the following exceptions:

1. The output low voltage is 0.5 V max at 1.8 mA for the ADDRESS, DATA, IORQ, RFSH, HALT, and BUSAK signals.
2. The input low current is 400 microamps max for the PHI clock, RESET, INT, NMI, and DATA signals.
3. The input high current if 20 microamps for the PHI clock, RESET, INT, NMI, and DATA signals.
4. The signals M1, MREQ, RD, and WR have a maximum of 25 nanoseconds added propagation delay.
5. The input signals RESET, INT, and NMI have a maximum of 45 nanoseconds propagation delay.

Target system power requirements (maximum): +5 V ±5% @ 600 milliamps

System compatibility: MATRIX-80/SDS, SYS-80F, or RADIUS

Operating temperature range; 0 to +50 degrees C

ORDERING INFORMATION

For detailed ordering information refer to the Development System Products Ordering Guide.

MOSTEK®

DEVELOPMENT SYSTEM PRODUCTS

AIM-7XE

Application Interface Module

FEATURES

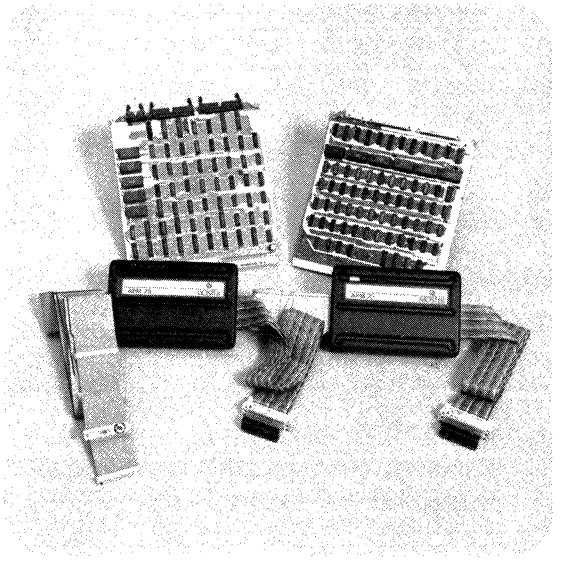
- Direct interface to Mostek's MATRIX-80/SDS, SYS-80F, and RADIUS™ development systems
- In-circuit emulation of all MK3870 and MK3873 family microprocessors (does not include piggy-back parts)
- Real-time execution (1-4 MHz with no wait states)
- Flexible breakpoints (one hardware, eight software, and one timer breakpoint) and any number of manually-inserted breakpoints
- Single-step execution
- 4 K bytes of emulation RAM
- Option of on-board oscillator or user clock
- Illegal write-to-memory detection
- Forty-eight-channel-by-1024-words history memory for tracing bus events
- Event counter and delay counter for monitoring bus events
- T-state timer to measure execution time
- English-oriented command structure
- Disassembly of instructions

GENERAL DESCRIPTION

AIM-7XE is an advanced development tool which provides debug assistance for both software and hardware via in-circuit-emulation of the MK3870 and MK3873 family of microprocessors. Use of the AIM-7XE is completely transparent to the user's final system configuration (referred to as the "target"). No memory space or user ports are used, and all signals, including /RESET and /EXT INT, are functional during emulation. No memory wait states are required.

Single-step circuitry allows the user to execute target instructions one at a time to see the exact effect of each instruction. 4 K bytes of emulation RAM are used to emulate the target microprocessor ROM.

AIM-7XE
Figure 1



Breakpoint-detect circuitry allows real-time execution to proceed to any desired point in the user's program and then terminate execution.

All CPU status information and registers can be displayed for the user and saved for later continuation of execution or single-stepping. Real-time execution may be terminated by the user at any time. EVENT and DELAY counters associated with the hardware breakpoint give added flexibility for viewing the exact point of interest in the user's program.

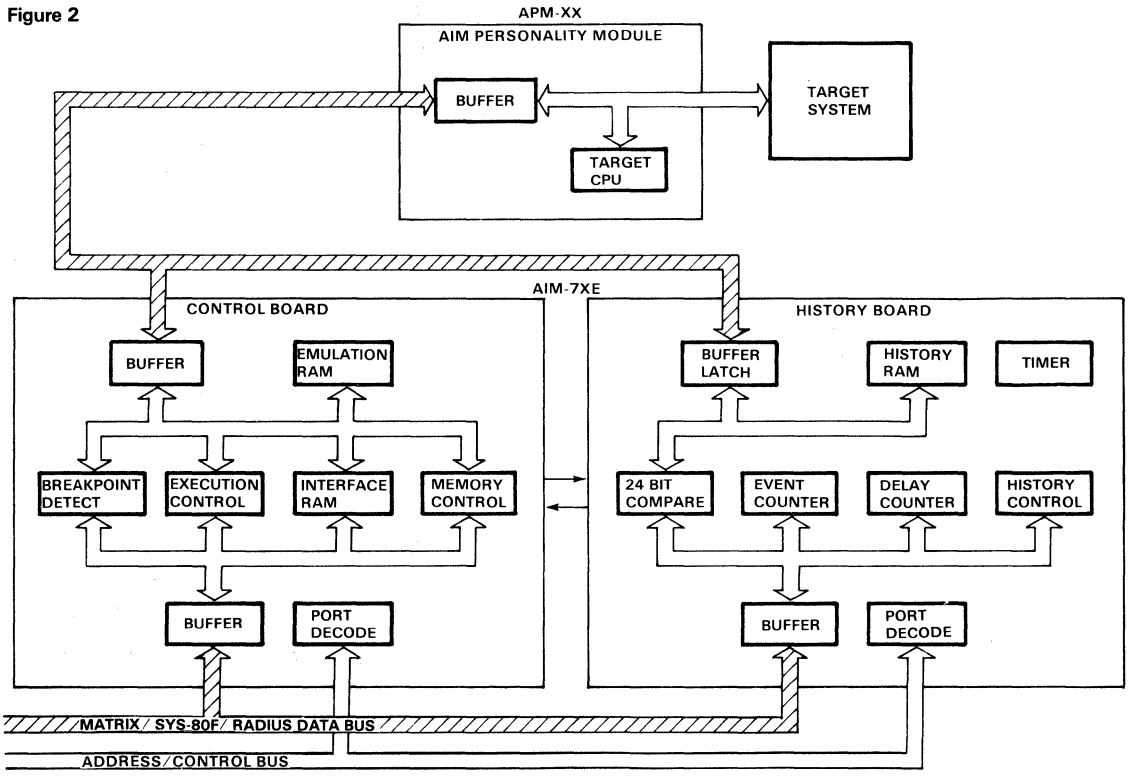
A forty-eight channel history memory records up to 1024 bus transactions. The address bus, data bus, ports 0, 1, and either port 4, 5, or 8 external probes may be logged into the history memory and later displayed by the user.

BLOCK DIAGRAM DESCRIPTION

The MK3870 Family emulation system is composed of both the AIM-7XE system and personality modules. AIM-7XE consists of two boards, the Control board and the History board, as shown in Figure 2. These boards are attached by cables to the personality module which contains the target

AIM-7XE BLOCK DIAGRAM

Figure 2



CPU and plugs directly into the target system CPU socket. Address, data, and control signals are buffered by the personality module.

The Control Board has the circuitry for detecting the breakpoint condition(s) and forces program execution to begin in the System Interface RAM. The System Interface RAM is loaded with an interface program and is shadowed into the target memory space. This control program makes the target CPU a slave to the development system. When the user desires to resume execution of his program, the control program activates the execution control circuit and execution resumes at the desired address.

The History Board has a 24-bit comparator circuit, an EVENT counter, and a DELAY counter to detect a hardware breakpoint condition. The 48-channel-by-1024-word history RAM is controlled by the History control circuit. The Timer circuit is used to count target processor clocks for logging elapsed time and generating the timer breakpoint.

USING THE AIM-7XE

The Control and History boards of the AIM-7XE are installed directly into the Mostek development system. To complete the emulation system a personality module is required. This module is a buffer interface between the first two boards and the target system's CPU socket. Note that a complete user target system is not required to do software debugging. Only the AIM-7XE boards and a personality module are needed.

The program which controls the AIM-7XE emulator system is named AIM7X. After execution of AIM7X is started, the program takes control of the AIM-7XE emulation system. The user can then initialize the target system and use the AIM7X commands to load, test, and debug the target program.

AIM7X SOFTWARE

AIM7X is the software which operates the AIM-7XE emulation system in the Mostek MATRIX-80/SDS or SYS-80F disk system or the RADIUS™ development tool. Target system programs may be developed on a Mostek disk system by use of the Mostek 3870/F8 Macro Cross Assembler (MACRO-70) and the resident linker. Programs may be developed for RADIUS™ using cross products supplied by Mostek or other vendors. The AIM7X software is supplied on standard FLP-80DOS diskette for Mostek disk-based systems and on a variety of media for different host systems for use with RADIUS™. The commands available in AIM7X are summarized below. Each command also has a "short form" which allows abbreviated input with fewer keystrokes.

BATCH	Read AIM commands from a file
BREAK	Display and set breakpoints (8 software, 1 hardware, and 1 timer breakpoint)
CLEAR	Clear one breakpoint or all breakpoints
COPY	Copy one block of memory to another block
DISABLE	Disable target CPU interrupts
DISASSEMBLE	Display and/or update instructions
DUMP	Dump a block of memory to a file
ENABLE	Enable target CPU interrupts
EXECUTE	Start or continue execution of the target program
FILL	Fill memory with a data byte
GET	Load a target program file into memory
HEXADECIMAL	Perform hexadecimal arithmetic
HELP	Display a menu of commands for the user
HISTORY	Set history logging options
INIT	Reinitialize target handshake
LOCATE	Locate a pattern in a memory block
LOG	Log all console output to a file
MEMORY	Display and/or update memory
OFFSET	Set an offset value for relative module debugging
PORT	Display and update a port on the target CPU
QUIT	Return to the resident operating system
RAMTEST	Perform a test on the target RAM
REGISTER	Display and/or update the target CPU registers
STATUS	Display the current status of the AIM system
STEP	Perform a single or multi-step execution
TRACE	Display the contents of the history RAM
TRANSPARENT	Allows the RADIUS user to temporarily access the host
VERIFY	Verify the contents of a block of memory with another block or a file

SPECIFICATIONS

Target operating frequency: 1 to 4 MHz

Target interface: All signals meet the specifications of the MK3870 family except that the XLT2 input will not accept a user crystal. It requires a TTL clock input.

System compatibility: MATRIX-80/SDS, SYS-80F, or RADIUS

Operating temperature range: 0 to +50°C

ORDERING INFORMATION

For detailed ordering information refer to the Development System Products Ordering Guide.

MOSTEK®

DEVELOPMENT SYSTEM PRODUCTS

MATRIX™

Microcomputer Development System

INTRODUCTION

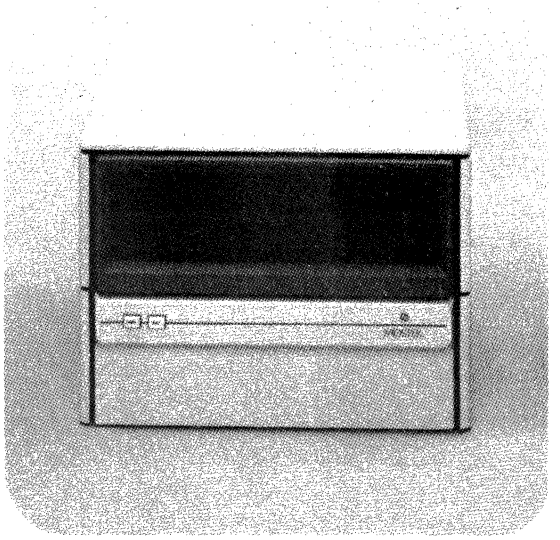
The Mostek MATRIX™ is a complete state-of-the-art, floppy disk-based computer. Not only does it provide all the necessary tools for software development, but it provides complete hardware/software debug through Mostek's AIM™ series of in-circuit emulation cards for the Z80 and the 3870 family of single-chip microcomputers. The MATRIX has at its heart the powerful OEM-80E (Single Board Computer), the RAM-80BE (RAM I/O add-on board), and the FLP-80E (floppy disk controller board). Because these boards and software are available separately to OEM users, the MATRIX serves as an excellent test bed for developing systems applications.

The disk-based system eliminates the need for other mass storage media and provides ease of interface to any peripheral normally used with computers. The file-based structure for storage and retrieval consolidates the data base and provides a reliable portable media to speed and facilitate software development.

The FLP-80DOS Disk Operating System is designed for maximum flexibility both in use and expansion to meet a multitude of end-user or OEM needs. FLP-80DOS is compatible with Mostek's SD and MD Series of OEM boards, allowing software designed on the MATRIX to be directly used in OEM board applications.

Development System Features

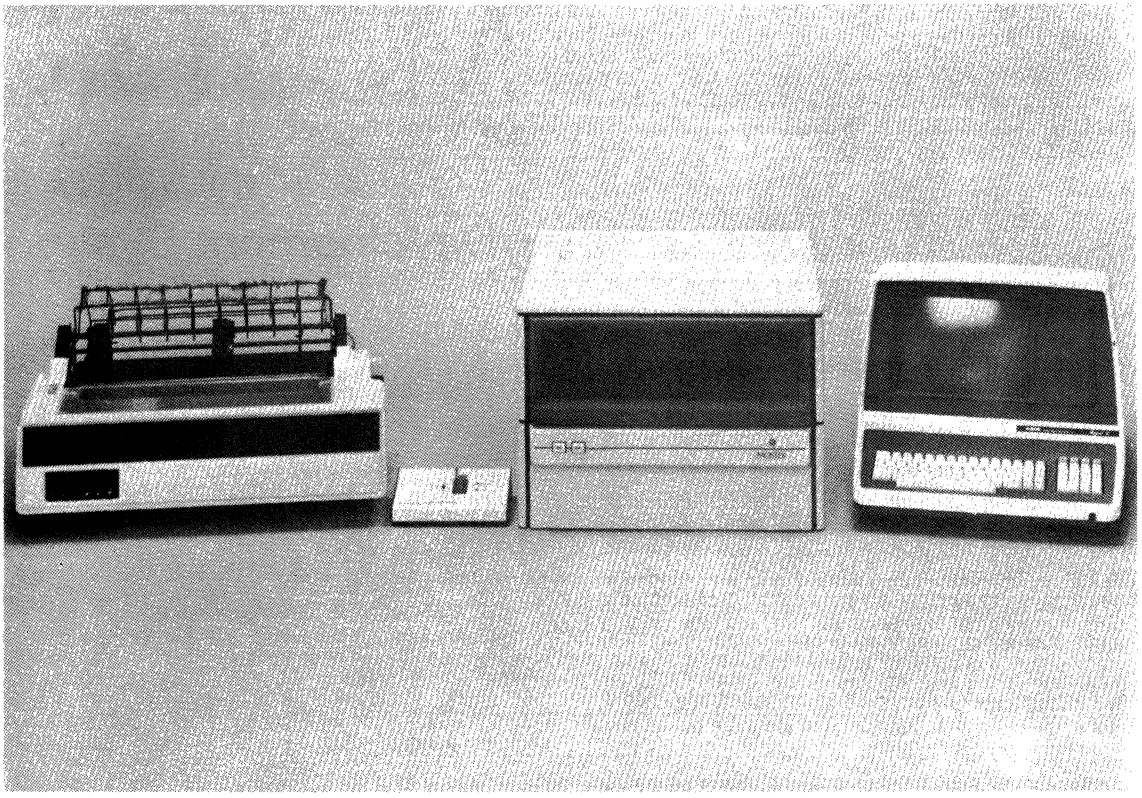
The MATRIX is an excellent integration of both hardware and software development tools for use throughout the complete system design and development phase. The software development is begun by using the combination of Mostek's Text Editor with "roll in-roll out" virtual memory operation and the Mostek relocating assembler. Debug can then proceed inside the MATRIX domain using its resources as if they were in the final system. Using combinations of the Monitor, Designer's Debugging Tool, execution time breakpoints, and single step/ multistep operation along with a formatted memory dump, provides control for attacking those tough problems. The use of the Mostek AIM™ options provides extended debug with versatile hardware breakpoints on memory or port locations, a buffered in-circuit emulation cable for extending the software debug into its own natural hardware environment, and a history memory to capture bus transactions in real time for later examination.



The relocatable and linking feature of the assembler enables the use of contemporary modular design techniques whereby major system alterations can be made in small tractable modules. Using the Linker, the small modules can be combined to form a run-time module without major reassembly of the entire program.

Package System Features

From a system standpoint, the MATRIX has been designed to be the basis of an end-product, such as a small business/industrial computer. The flexibility provided in the FLP-80DOS operating system permits application programs to be as diverse as a high-level language compiler or a supervisory control system in the industrial environment. Other hardware options are available, with even more to be added. Expansion of the disk drive units to a total of four single-sided or double-sided units provides up to two megabytes of storage. This computer uses the third-generation Z80 processor supported with the power of a complete family of peripheral chips. Through the use of its 158 instructions, including 16-bit arithmetic, bit manipulation, advanced block moves and interrupt handling, almost any application from communication concentrators to general purpose accounting systems is made easy.



OEM Features

The hardware and software basis for the MATRIX is also available separately to the OEM purchaser. Through a software licensing agreement, all Mostek software can be utilized on these OEM series of cards.

MATRIX RESIDENT SOFTWARE (FLP-80DOS)

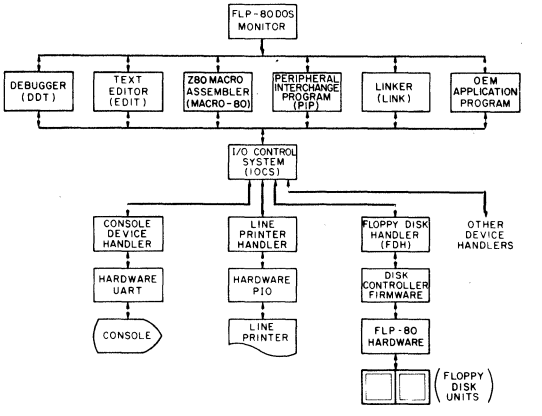
A totally integrated package of resident software is offered in conjunction with the MATRIX and consists of:

- Monitor
- Text Editor
- MACRO 80 Assembler
- Linker
- DDT-80 with extended debug through AIM™ modules
- Peripheral Interchange Program
- Floppy Disk Handler
- I/O Control System
- Device Driver Library
- Batch Mode Operation

Monitor

The FLP-80DOS Monitor is the environment from which all activity in the system initiates. From the Monitor, any system routine such as PIP or a user-generated program is begun by simply entering the program name. FLP-80DOS I/O is done in terms of logical unit numbers, as is commonly done in FORTRAN. A set of logical units is pre-assigned to default I/O drivers upon power up or reset. From the console, the user can reassign any logical unit to any new I/O device and can also display logical unit assignments. Executable file creation can be done by the Save command; printable absolute object files can be produced using the Dump command.

MATRIX BLOCK DIAGRAM



Text Editor

The Text Editor permits editing/creating of any source file independent of the language being written. The Editor is both line and string oriented to give maximum utility and user flexibility. The Editor, through its virtual memory "roll in-roll out" technique, can edit a file whose length is limited only by maximum diskette storage. Included in the repertoire of 15 commands are macro commands to save time when encountering a redundant editing task. The Editor is also capable of performing in one operation all the commands which will fit into an 80-column command buffer.

Summary of Editor Commands

Advance N	- Advance line pointer N line
Backup N	- backs up N lines
Change N/S1/S2	- change N occurrences of String 1 to String 2
Delete N	- Delete current line plus next N-1 lines of text
Exchange N	- Exchanges current line plus next N-1 lines with lines to be inserted while in insert mode
Get file	- Reads another file and inserts it into the file being edited after the current line
Insert	- Place Editor in insert mode. Text will be inserted after present line
Line N	- Place line pointer on Line N.
Macro 1 or Macro 2	- Defines Macro 1 or Macro 2 by the following string of Text Editor commands.
Put N file	- Outputs N lines of the file being edited to another disk file.
Quit	- Stores off file under editing process and returns to Monitor environment
Search N/S1	- Searches from existing pointer location until NTH occurrence of string SI is located and prints it.
Top	- Inerts records at top of file before first line.
Verify N	- Print current record to console plus next N-1 records while advancing pointer N records ahead.
Write N	- Prints current records plus next N-1 records to source output device while advancing pointer N records.
eXecute N	- Executes Macro 1 or Macro 2 as defined by Macro command.
Breakpoint	- sets software trap in user code for interrupting execution in order to examine CPU registers
Register	- displays contents of user's registers
Offset	- enters address adder for debug of relocatable modules
Fill	- fills specified portion of memory with 8 bit byte
Verify	- compares two blocks of memory
Walk	- software single step/multistep
Quit	- returns to Monitor

Debuggers for other processors have similar or enhanced capability and are included with the appropriate AIM.™

Z80 ASSEMBLER

The Z80 Resident Assembler generates relocatable or absolute object code from source files. The assembler recognizes all 158 Z80 instructions as well as 20 powerful pseudo operators. The object code generated is absolute or relocatable format. With the relocating feature, large programs can be easily developed in smaller sections and linked using the Linker. Because the assembler utilizes the I/O Control System, object modules or list modules can be directed to disk files, paper tape, console, or line printer. Portability of output media eliminates the requirement for a complete set of peripherals at every software/hardware development system. The assembler run-time options include sorted symbol table generation, no list, no object, pass 2 only, quit, cross reference table, and reset symbol table. The assembler is capable of handling 14 expression operators including logical, shift, multiplication, division, addition and subtraction operations. These permit complex expressions to be resolved at assembly time by the assembler rather than manually by the programmer. Comments can be placed anywhere but must be integrated with the listing file but can be directed to the console device. In addition, assembler pseudo operators are:

GLOBAL	- for global symbol definition.
PSECT operator	- to generate relocatable or absolute modules
IF expression	- conditional assembly IF expression is true
INCLUDE dataset	- to include other datasets (files) as in-line source code anywhere in source file.

Linker

The Linker program provides the capability of linking assembler-generated, absolute or relocatable object modules together to create a binary or run-time file. This process permits generation of programs which may require the total memory resources of the system. The linking process includes the library search option, which, if elected, will link in standard library object files from disk to resolve undefined global symbols. Another option selects a complete global symbol cross-reference listing.

DDT

The Designer's Debugging Tool consists of commands for facilitating an otherwise difficult debugging process. The MATRIX allows rapid source changes through the editor and assembler. This is followed by DDT operations which close the loop on the debug cycle. The DDT commands include:

Memory	- display, update, or tabulate memory
Port	- display, update or tabulate I/O ports
Execute	- execute user's program
Hexadecimal	- performs 16 bit add/sub
Copy	- copy one block to another

Peripheral Interchange Program

PIP provides complete file maintenance activity for operations such as copy file from disk to disk, disk to peripheral, or any peripheral to any other peripheral supporting both file-structured and character-oriented devices. Key operations such as renaming, appending, and erasing files also exist along with status commands for diskette ID and vital statistics. PIP can search the diskette directories for any file or a file of a specific name, extension, and user number. The PIP operations are:

Append	- appends file 1 to file 2 without changing file 1.
Copy	- copies input files or data from an input device to an output file or device. The Copy command can be used for a variety of purposes such as listing files, concatenating individual files, or copying all the files on a single file from one disk unit (e.g. DK0) to a second disk unit (e.g. DK1)
Date	- allows the specifying of the date in day, month, and year format. The date specified will be used to date tag any file which is created or edited.
Directory	- lists the directory of a specified disk unit (DK0, DK1, etc.). The file name, extension, and user number and creation or edited date are listed for each file in the directory. The user can also request listing-only files of a specified name, only files of a specified extension, or only files of a specified user number. The list device can be any device supported by the system as well as a file.
Erase	- erases a single file or files from a diskette in a specified disk unit. The user has the option to erase all files, only files of a specified file name, or only files of a specified user number.
Format	- takes completely unformatted soft-sectored diskettes, formats to IBM 3740, and prepares to be a system diskette. Operation is performed on diskette unit 1 and a unique 11-character name is assigned to that diskette.
Init	- initializes maps in the disk handler when a new diskette has been changed while in the PIP environment.
Rename	- renames a file, its extension, and user number to a file of name X, extension Y, and user Z.
Status	- lists all vital statistics of a disk unit to any device. These include the number of allocated records, the number of used records, and the number of bad records
Quit	- returns to Monitor Environment.

DOS/Disk Handler

The heart of the FLP-80DOS software package is the Disk Operating System. Capable of supporting up to 4 single-density, single or double-sided units, the system provides a file-structure orientation timed and optimized for rapid storage and retrieval. Program debug is enhanced by complete error reporting supplied with the DOS. Additionally, extensive error recovery and bad sector allocation ensure data and file integrity. The DOS not only provides file reading and writing capability, but special pointer manipulation, record deletions, record insertions, skip records both forward and backward, as well as directory manipulation such as file creation, renaming, and erasure. The DOS is initiated by a calling vector which is a subset of the I/O control system vector or by the standard IOCS calling sequence to elect buffer allocation, blocking, and deblocking of data to a user-selectable, logical record type.

A unique dynamic allocation algorithm makes optimal use of disk storage space. Run time (Binary) files are given first priority to large blocks of free space to eliminate overhead in operating system and overlay programs. The algorithm marks storage fragments as low priority and uses them only when the diskette is nearing maximum capacity. The DOS permits 7 files to be opened for operations at any one time, thus permitting execution of complex application programs.

I/O Control System

The I/O Control System provides a central facility from which all calls to I/O can be structured. This permits a system applications program to dissolve any device dependence by utilizing the logical unit approach of large, main-frame computers. For example, a programmer may want to structure the utility to use logical unit No. 5 as the list device which normally in the system defaults to the line printer. He may, however,

assign at run time a different device for logical unit No. 5. The application program remains unchanged.

Interface by a user to IOCS is done by entering a device mnemonic in a table and by observing the calling sequence format. IOCS supplies a physical buffer of desired length, handles buffer allocation, blocking, and deblocking, and provides a logical record structure as specified by the user.

Batch - Mode Operation

In Batch-Mode Operation, a command file is built on disk or assigned to a peripheral input device such as a card reader. The console input normally taken from the keyboard is taken from this batch device or batch file. While operating under direction of a batch file, the console output prompts the user as normal, or the prompting can be directed to any other output device. The Batch operation is especially useful for the execution of redundant procedures not requiring the constant attention of the operator.

MATRIX SYSTEM SPECIFICATIONS

- Z80 CPU.
- 4K byte PROM bootstrap and Z80 debugger
- 60K bytes user RAM. (56K contiguous)
- 8 x 8 bit I/O ports (4 x PIO) with user-definable drivers/receivers
- Serial port, RS 232 and 20 mA current loop.
- 4 channel counter/timer (CTC).
- 2 single-density, single-sided disk drives; 250K bytes per floppy disk.
- 3 positions for AIM modules, A/D cards, Serial Interface, etc.
- Device drivers for paper tape readers, punches, card readers, line printers, Silent 700's, Teletypes and CRT's are included. Others can be added.
- PROM programmer I/O port. Programmer itself is optional.
- Bus compatible with Mostek SD/E series of OEM boards.

HARDWARE DESCRIPTION OEM-80E

CPU Module

The OEM-80E provides the essential CPU power of the system. While using the Z80 as the central processing unit, the OEM-80E is provided with other Z80 family peripheral chip support. Two Z80 PIO's give 4 completely programmable 8 bit parallel I/O ports with handshake from which the standard system peripherals are interfaced. Also on the card is the Z80-CTC counter time circuit which has 3 free flexible channels to perform critical counting and timing functions. Along with 16K of RAM, the OEM-80 provides 5 ROM/PROM sockets which can be utilized for 10/20K of ROM or 5/10K PROM. Four sockets contain the firmware portion of FLP-80DOS. The remaining socket can be strapped for other ROM/PROM elements.

RAM-80BE

The RAM-80BE adds additional memory with Mostek's MK4116 16K dynamic memory along with more I/O. These two fully programmable 8-bit I/O ports with handshake provide additional I/O expansion as system RAM memory needs to grow. Standard system configuration is 48K bytes for a system total of 60K bytes user RAM (56K contiguous).

FLP-80E

Integral to the MATRIX system is the floppy controller. The FLP-80E is a complete IBM 3740 single-density/double-sided controller for up to 4 drives. The controller has 128 bytes of FIFO buffer resulting in a completely interruptable disk system.

OPTIONAL MODULES COMPATIBLE WITH MATRIX

AIM-Z80BE (6.0 MHz max. clock rate)

The AIM-Z80BE is an improved Z80 In-Circuit-Emulation module usable at Z80-CPU clock rates of up to 6MHz. The AIM-Z80BE is a two processor solution to In-Circuit Emulation which utilizes a Z80-CPU in the buffer box for accurate emulation at high clock rates with minimum restrictions on the target system. The AIM-Z80BE provides real time emulation (no WAIT states) while providing full access to RESET, NMI and INT control lines. Eight single byte software breakpoints (in RAM) are provided as well as one hardware trap (RAM or ROM). The emulation RAM on the AIM-Z80BE is mappable into the target system in 256 byte increments. A 1024 word x 48 bit history memory is triggerable by the hardware intercept and can be read back to the terminal to provide a formated display of the Z80-CPU address, data, and control busses during the execution of the program under test. Several trigger options are available to condition the loading of the history memory.

AIM-7XE

The AIM-7XE module provides debug and in-circuit emulation capabilities for the 3870 series microcomputers on the MATRIX. Multiple-breakpoint capability and single-step operation allow the designer complete control over the execution of the 3870 Series microcomputer.

Register, Port display, and modification capability provide information needed to find system "bugs." All I/O is in the user's system and is connected to AIM-7X by a 40-pin interface cable.

The debugging operation is controlled by a mnemonic debugger which controls the interaction between the Z80 host computer and the 3870 slave. It includes a history module for the last 1024 CPU cycles and also supports all 3870 family circuits.

Assembly and linking are done using the MACRO-70 Assembler and the standard FLP-80DOS linker.

MECHANICAL SPECIFICATIONS

Overall Dimensions:
CPU subsystem - 8" High x 21" wide x 22" deep
(20.3cm x 53.3 cm x 55.8cm)
Disk subsystem - 8" High x 21" wide x 22" deep
(20.3cm x 53.3 cm x 55.8cm)

Humidity: up to 90% relative, noncondensing.

Material: Structural Foam (Noryl)

Weight: CPU Subsystem 25 lbs (11.3 Kg)
Disk Subsystem 50 lbs (22.7 Kg)

Fan Capacity: 115 CFM

Card Cage: Six slots DIN 41612 type connectors

Operating Temperature: +10°C to +35°C

ELECTRICAL SPECIFICATIONS

INPUT 100/115/230 volts AC ± 10%
50 Hz (MK78189) or 60Hz (MK78188)

OUTPUT

CPU subsystem	+5 VDC at 12A max.
	+12 VDC at 1.7A max.
	-12 VDC at 1.7A max.
Disk subsystem	+5VDC at 3.0A max.
	-5 VDC at 0.5A max.
	+24 VDC at 3.4A max.

ORDERING INFORMATION

BASIC SYSTEM NO.

NAME	DESCRIPTION	PART NO.
MATRIX™	Z80 floppy disk based microcomputer with 60K bytes of RAM (56K bytes contiguous RAM), 4K bytes PROM bootstrap, two 250K byte single density floppy disk drives with Operations Manual. Includes the software package of FLP-80DOS distributed on diskette. Requires signed license agreement with purchase order.	MK78188 (60Hz) MK78189 (50Hz)
MATRIX™	Operations Manual Only	MK79730
FLP-80DOS	Operations Manual Only	MK78557

IN-CIRCUIT EMULATION MODULES

NAME	DESCRIPTION	PART NO.
AIM-Z80AE	4.0 MHz RAM based Z80 in-circuit emulator with expanded history trace, buffer box, cables and Operations Manual 16K Bytes emulation RAM 32K Bytes emulation RAM	 MK78181-1 MK78181-2
AIM-Z80AE	Operations Manual only	MK79650
AIM-7XE	RAM based in-circuit emulator for the 3870 series of single-chip microcomputers (3870, 3872, 3874 and 3876) with cables and Operations Manual.	MK79077
AIM-7XE	Operations Manual only	MK79579

SOFTWARE-FULLY SUPPORTED

NAME	DESCRIPTION	PART NO.
MACRO-70	Relocatable 3870/F8 MACRO assembler which speeds up development of 3870/F8 programs through use of MACRO to run on MATRIX with Operations Manual. Requires signed license agreement with purchase order.	MK79085
MACRO-70	Operations Manual Only	MK79658
MACRO-80	Operations Manual Only	MK79635

NAME	DESCRIPTION	PART NO.
ANSI BASIC	ANSI BASIC interpreter with random disk access for the MATRIX microcomputer including operations manual. Requires signed license agreement with purchase order.	MK78157
ANSI BASIC	Operations Manual only	MK79623

SOFTWARE-LEVEL 2 UNSUPPORTED

NAME	DESCRIPTION	PART NO.
MOSTEK FORTRAN IV	FORTRAN IV compiler (Z80 object code) for the MATRIX microcomputer with Operations Manual. Requires signed license agreement with purchase order.	MK78158
MOSTEK FORTRAN IV	Operations Manual only MK79644	MK79643
LIBRARY	Vol. 1 of Z80 Software Library including FLP-80DOS utilities, sort, 8080 to Z80 source translator, word processor program, LLL BASIC (6K). 23 Programs total including source, object, and binary.	MK78164

PERIPHERALS AND CABLES

NAME	DESCRIPTION	PART NO.
MOSTEK VT	110-9600 Baud CRT with upper and lowercase character set. Includes cable (78152) to MATRIX. 110/115 volt 50/60 Hz 230 volt 50/60 Hz	MK78190-1(60Hz) MK78190-2(50Hz)
MOSTEK LP	7 x 7 dot MATRIX printer with 120 character LP per second operation. Includes interface cable to MATRIX. 100/115 volt model 50/60 Hz 230 volt model 50/60Hz	MK78191-1(60Hz) MK78191-2(50Hz)
PPG-8/16	Programmer for 2708, 2758 and 2716 PROM Includes interfacing cables to MATRIX.	MK79081-1
SD-WW	Wire wrap card compatible with MATRIX.	MK79063
SD-EXT	Extender card compatible with MATRIX.	MK79062
LP-CABLE	Interface cable from MATRIX Microcomputer to Centronics 306 or 702 printer	MK79089
PPG-CABLE	Interface cables from MATRIX to PPG-8/16 PROM programmer (MK79081).	MK79090

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City State Zip Code

Country Telephone ( )

Mostek Disk System Serial # or Mostek Disk Controller Serial #

or ☐ Non Mostek Hardware

Date of Purchase

Place of Purchase

XI

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Purchase Order # to Mostek ☐ Customer PO # or ☐ Distributor PO # PO # _____

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Software Librarian, MS #510
Micro System Department
Mostek Corporation
1215 W. Crosby Road
P.O. Box 169
Carrollton, Texas 75006

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MOSTEK®

DEVELOPMENT SYSTEM PRODUCTS

EVAL-70

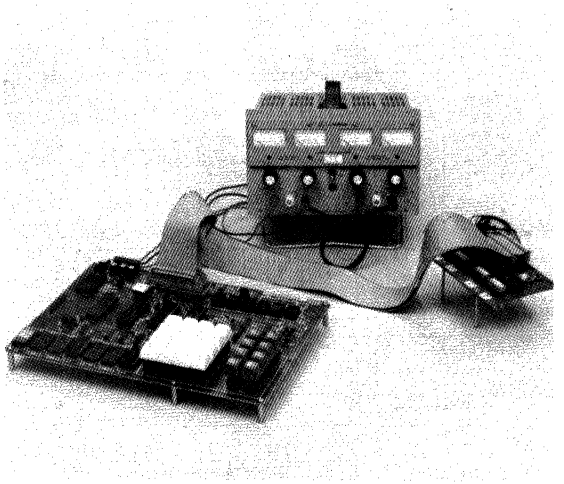
3870 Evaluation System

FEATURES

- An ideal hardware and/or software design aid for the MK38P70 and MK3870 family of Single-Chip Microcomputers
- Includes a 2K byte firmware monitor
- Keypad for command and data entry
- 7-segment address and data display
- Programming socket for MK2716/2758's
- Crystal controlled system clock
- 2K bytes of MK4118 static RAM (up to 4K optional)
- Sockets for up to 4K bytes of MK2716 PROM's
- Flexible memory map strapping options
- Current loop or RS-232 serial loader optional (110-300-1200 baud)
- 3 general purpose timer/counters
- 3 general purpose external interrupts
- Easy to use - requires only two supplies for normal operation (+5, +12)
- Ideal for evaluation of MK3870 family single-chip microcomputers
- Full in-circuit emulation of MK3870 single-chip microcomputer family.

DESCRIPTION

EVAL-70 is a single board computer with on-board keypad, address and data displays, and 2716 PROM programmer. EVAL-70 is designed to be an easy-to-use introduction to the industry standard MK3870 family of single-chip computers. Programs can be written and debugged in RAM using the powerful DDT-70 operating system. The 40 pin AIM cable can be used to perform real-time emulation of the MK3870 family of devices. After debugging, programs can be loaded into MK2716's for final circuit checkout (and emulation).



USING EVAL-70

The photograph above shows how EVAL-70 is used as a program development tool. Only an external power supply is required for operation of EVAL-70; the built-in keyboard and display offer all the functions needed to design, develop, and debug programs for the MK3870 family of single-chip microcomputers at the machine code level.

COMMAND SUMMARY

DM:	Display memory: allows memory to be displayed and (RAM) updated.
DR:	Display registers: allows the user's register values to be displayed and updated.
DP:	Display ports: allows the contents of ports 0 thru F to be displayed and updated
HX:	Hex calculator: allows hexadecimal arithmetic calculations to be performed (add and subtract)
GO:	causes execution of a user program at a specified address

BK: Breakpoint: allows a breakpoint to be set or reset

ST: Step: causes single-step execution of a user program at a specified address

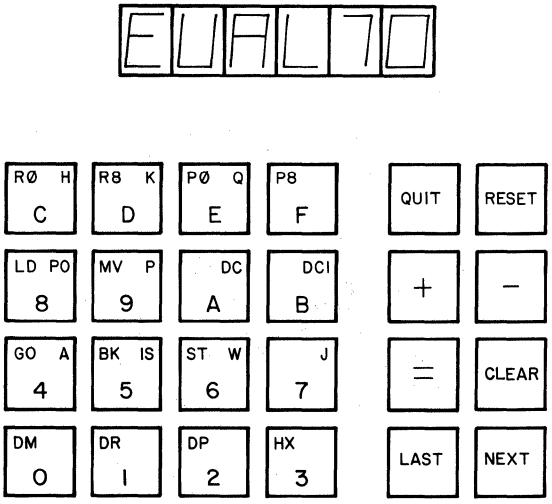
LD: Load: initiates the serial loader (optional)

MV: Move: allows a block of memory to be moved or copied from one space to another

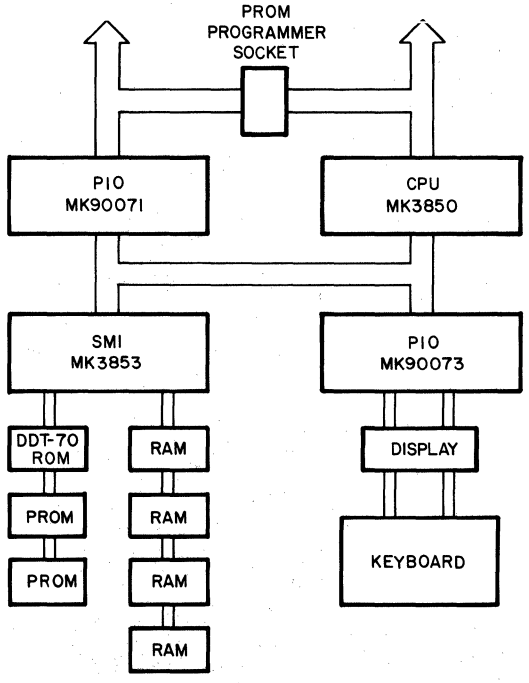
RO, R8: Read PROM: causes the PROM programmer socket to be read into address space 00-7FF or 800-F7F

PO, P8: Program PROM: causes the contents of address space 000-7FF or 800-F7F to be programmed into the PROM programmer socket

EVAL-70 KEYBOARD DRAWING



BLOCK DIAGRAM



BLOCK DIAGRAM

EVAL-70 uses several members of the F8 multichip family. A MK3850 Central Processing Unit (CPU) provides the ALU, registers, system control and two 8-bit ports. A MK90071 Peripheral Input Output chip (PIO) provides two more 8-bit ports plus a flexible timer/interrupt control block. These four ports are connected to the AIM cable connector for in-circuit emulation of the MK3870 family devices, and also to the PROM programmer socket. An additional PIO (MK90073) interfaces the LED display and keyboard. A MK3853 Static Memory Interface chip (SMI) interfaces the operating system ROM, up to two 2K PROMs and up to four 1K RAMs. A switch option allows either the 4K of PROM or the 4K of RAM to appear at address 0000H, with the other 4K appearing at 1000H. The operating system ROM may be up to 8K (currently 2K) starting at 8000H. A switch option allows reset to either 0000H or to the 8000H ROM.

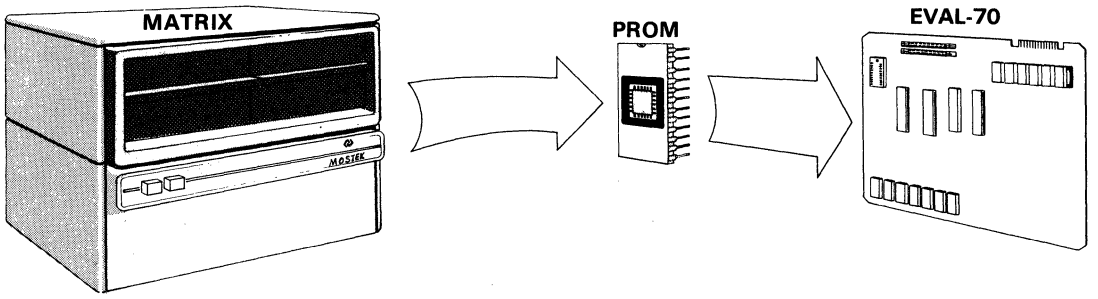
USING EVAL-70 WITH LARGER SYSTEMS

Although the EVAL-70 operating system (DDT-70) was designed to make program machine code entry simple and quick, many users will find it more efficient to assemble their programs on a larger computer and then download to EVAL-70.

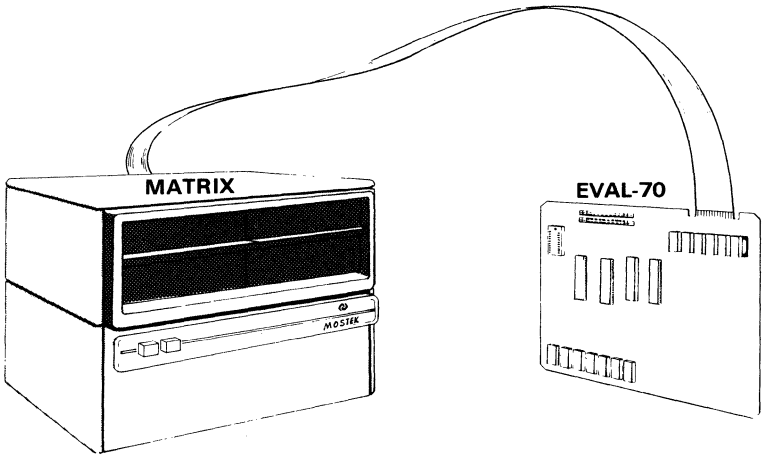
The download to EVAL-70 may be accomplished in either of two ways:

1) A PROM may be programmed on the Development System, and then read into RAM by the EVAL-70 for debugging.
2) A direct connection may be made between a serial port on the Development System and the serial loader port on EVAL-70. An optional serial loader program is provided in the EVAL-70 Operations Manual.

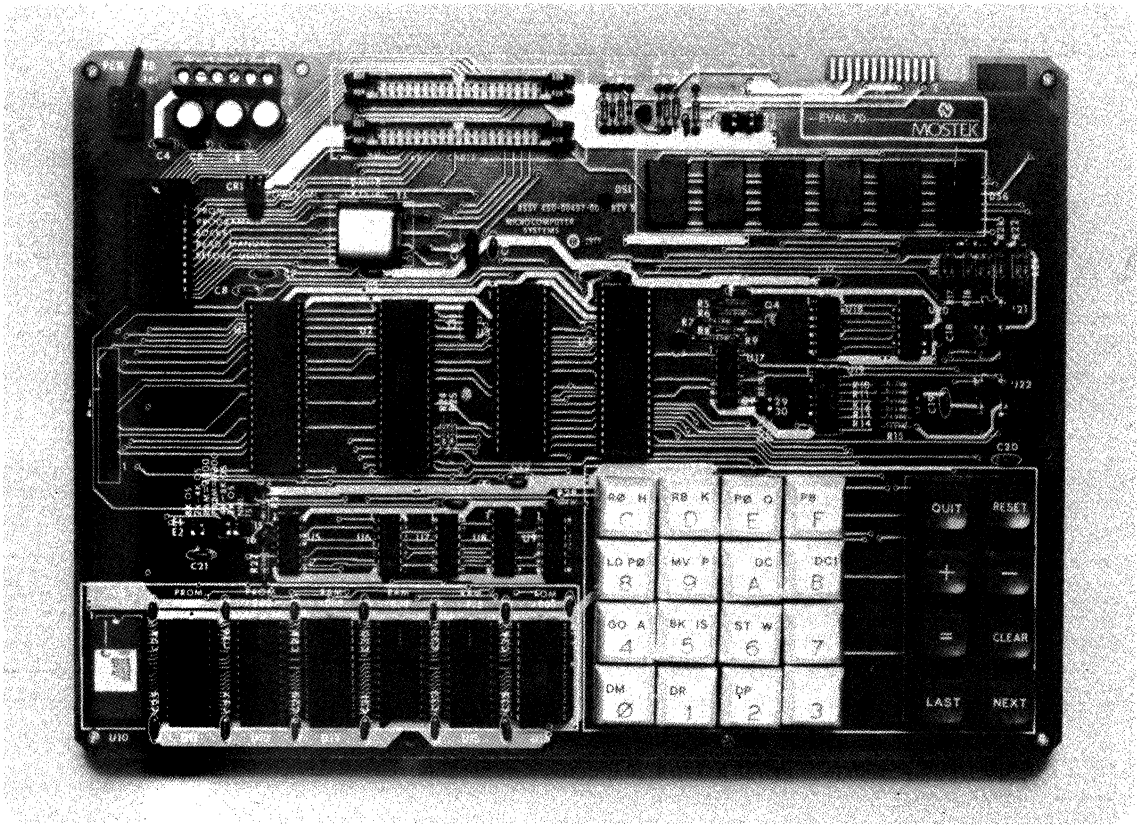
Owners of minicomputers may purchase XFOR-70, a 3870 cross-assembler written in ANSI standard Fortran IV. It may be compiled and executed on any computer system which has at least a 16-bit word length for integer storage and 13K (typical) of memory for program storage.



DEVELOPMENT SYSTEM



EVAL-70 BOARD



Owners of a Matrix Disk Development System may purchase MACRO-70, an advanced 3870 cross assembler. MACRO-70 will generate relocatable, linkable object modules and provides MACRO assembly capability.

SPECIFICATIONS

Operating Temperature: 0°C - 50°C

Power Supplies Required: +5VDC ±5% 1.0A max
+12VDC ±5% 0.1A max
+25VDC ±5% 0.1A max

Board Size: 8.5 in. (21.6 cm) x 12 in. (30.5cm) x 2 in. (5cm)

Connectors and Cables: 40 pin in-circuit-emulation cable is provided.

ORDERING INFORMATION

NAME	DESCRIPTION	PART NO.
EVAL-70	3870 Evaluation System, Assembled and tested with Operations Manual and In-circuit Emulation cable.	MK79086
EVAL-70 Manual	EVAL-70 Operations Manual only	MK79717
XFOR-50/70	FORTRAN Cross assembler for 3870 series	MK79012
MATRIX	Disk Based Development System	MK78189 (50Hz) MK78188 (60Hz)
AIM-72E	In-circuit emulation module for the MATRIX for the 3870, 3872, 3874 and 3876 Microcomputer	MK79077
MACRO-70	3870 Cross Assembler with MACRO capability for the Matrix Disk Development System	MK79085

MOSTEK.

DEVELOPMENT SYSTEM PRODUCTS

PPG 8/16C

PROM Programmer

FEATURES

- ☐ Programs, reads, and verifies 2708-, 2758-, and 2716-type PROMs (2758 and 2716 PROMS must be 5-Volt only type)
- ☐ Interfaces to MATRIX and MDX-PIO
- ☐ Driver software included on system diskette for FLP-80DOS
- ☐ Zero-insertion-force socket
- ☐ Power and programming indicators

DESCRIPTION

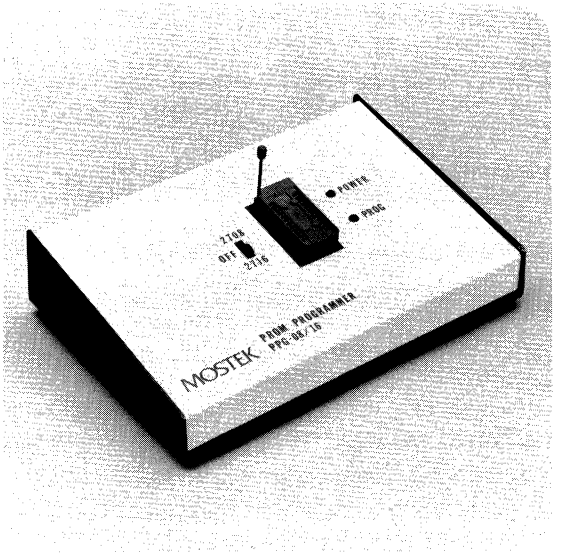
The PPG-8/16C PROM Programmer is a peripheral which provides a low-cost means of programming 2708, 2758, or 2716 PROMs. It is compatible with Mostek's MATRIX Microcomputer Development System and the MDX-PIO. The PPG-8/16C has a generalized computer interface (two 8-bit I/O ports) allowing it to be controlled by other types of host computers with user-generated driver software. A complete set of documentation is provided with the PPG-8/16C which describes the internal operation and details user's operating procedures

The PPG-8/16C is available in a metal enclosure for use with the MATRIX™ and the MDX-PIO. Interface cables for either the MATRIX or MDX-PIO must be purchased separately.

SOFTWARE DESCRIPTION

The driver software accomplishes four basic operations.

PPG 8/16C

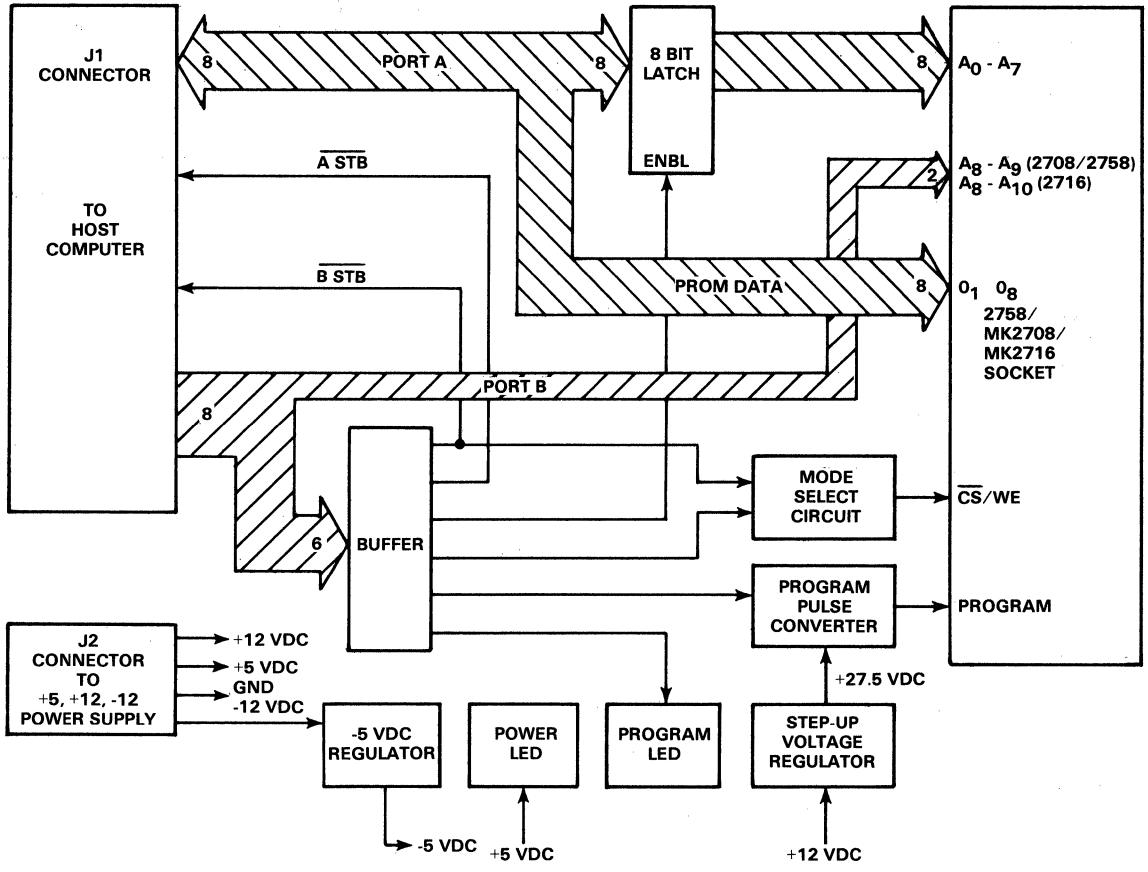


These are (1) loading data into host computer memory, (2) reading the contents of a PROM into host computer memory, (3) programming a PROM from the contents of the host computer memory, and (4) verifying the contents of a PROM with the contents of the host computer memory.

The driver software is provided on the FLP-80DOS system diskette. The user documentation provided with the PPG-8/16C fully explains programming procedures to enable a user to develop a software driver on a different host computer.

XI

PPG 8/16C BLOCK DIAGRAM



INTERFACE

25-pin control connector (D type)
40-pin control connector (0.1-in. centers card edge)
for AID-80F, SDB-80, SDB-50/70, or MATRIX™
12-pin power connector (0.156-in. centers card edge)
All control signals are TTL-compatible

POWER REQUIREMENTS

+12 VDC at 250mA typical
+5 VDC at 100mA typical
–12 VDC at 50mA typical

OPERATING TEMPERATURE

0°C –60°C

PROGRAMMING TIME

2708 - 2.5 minutes
2758 - 0.9 minutes
2716 - 1.8 minutes

ORDERING INFORMATION

DESIGNATOR	DESCRIPTION	PART NO.
PPG-8/16C	PROM Programmer for 2708/2758/2716 PROMs with Operations Manual for interface with MATRIX.	MK79081-1
MATRIX to PPG-8/16C	PPG-8/16C Interface Cable for MATRIX	MK79090
MD-PPG-C	PPG-8/16C Interface Cable for MDX-PIO	MK77957
	PPG-8/16C Operations Manual	MK79603

*NOTE: The PPG-8/16C will only program the 2708, 2758, and 2716 PROMs. The 2758 and 2716 are 5 Volt only type PROMs. THE PPG-8/16C WILL NOT PROGRAM THE TI2716 MULTIPLE-VOLTAGE 2K x 8 PROM.

SD To SDE Adapter

INTRODUCTION

The 'SD To SDE Adapter' is an inexpensive conversion aid for the AID-80F customers to expand their system to accept the AIM-Z80BE or AIM-7XE modules. The 'SD to SDE Adapter' is a bus converter PCB allowing the installation of the SDE series AIM modules into an AID-80F Development System.

HARDWARE

The 'SD To SDE Adapter' is a single SD form factor printed circuit board with connectors and card guides for the SDE form factor modules. The SDE series AIM modules are installed onto the Adapter and then become an insertable/removable unit configured to the AID-80F systems.

The 'SD To SDE Adapter' has three connectors: J1 is the AID-80F bus interface edge connector; SK1 and SK2 are the SDE series AIM module interface connectors.

SPECIFICATIONS

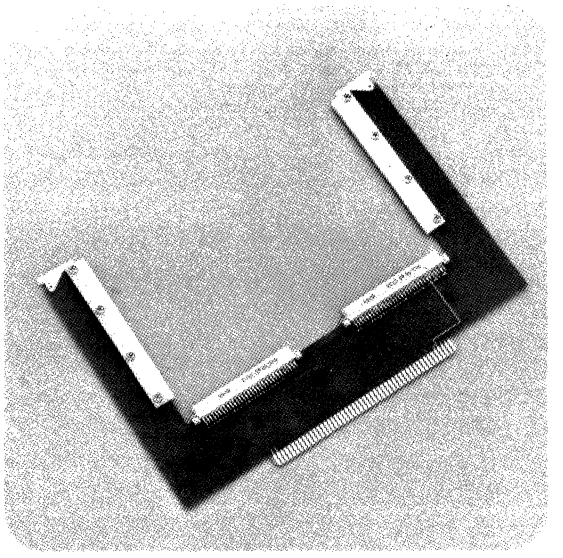
Width: 12.0 inches
Height: 8.5 inches
Power consumption: None

STRAPPING

The customer will need two of these Adapters to be able to use the AIM modules on his AID-80F system. He will need to strap J2 pins 1 and 2 on one Adapter for his AIM Logic board, and strap J3 pins 1 and 2 on the other Adapter for the AIM History board. Refer to the following table for the J2 and J3 strapping instructions.

AIM Board	J2	J3
AIM-Z80BE	Strap J2 pins 1 and 2	Leave J3 un-strapped
AIM-7XE	Strap J2 pins 1 and 2	Leave J3 un-strapped
AIM History	Leave J2 un-strapped	Strap J3 pins 1 and 2

SD TO SDE ADAPTER
Figure 1



INSTALLATION

A. Slide the AIM board into the properly strapped Adapter board so that the connectors gently mate. Do not force complete mating.
B. Slide the Adapter into the AID-80F card cage with the components facing the same direction as the other boards in the system.
C. Completely mate the Adapter with the 100 pin edge connector in the AID-80F system.
D. Completely mate the SDE board with the Adapter.

WARNING: Make sure that the components on the AIM boards are facing the same direction as the other boards in the AID-80F system. If not, the AIM boards will be damaged upon power up.

ORDERING INFORMATION

DESIGNATOR	DESCRIPTION	PART NO.
SD to SDE Adapter	The conversion aid for the AID-80F system to accept the new AIM modules.	MK79095

MOSTEK®

SOFTWARE PRODUCTS

MACRO-80

MK78165

FEATURES

- ☐ Assembles standard Z80 instruction set to produce relocatable, linkable, object modules.
- ☐ Provides nested conditional assembly, an extensive expression evaluation capability, and an extended set of assembler pseudo-ops:

ORG	- origin
EQU	- equate
DEFL	- set/define macro label
DEFM	- define message
DEFB	- define byte
DEFW	- define word
DEFS	- define storage
END	- end of program
GLOBAL	- global symbol definition
NAME	- module name definition
PSECT	- program section definition
IF/ENDIF	- conditional assembly
INCLUDE	- include another file in source module
LIST/NLIST	- list on/off
CLIST	- code listing only of macro expansions
ELIST	- list/no list of macro expansions
EJECT	- eject a page of listing
TITLE	- place title on listing

- ☐ Provides options for obtaining a printed cross-reference listing, terminating after pass one if errors are encountered, redefining standard Z80 opcodes via macros, and obtaining an unused-symbol reference table.
- ☐ Provides the most advanced macro handling capability in the microcomputer market which includes:
  - optional arguments
  - default arguments
  - looping capability
  - global/local macro labels
  - nested/recursive expansions
  - integer/boolean variables
  - string manipulation
  - conditional expansion based on symbol definition
  - call-by-value facility
  - expansion of code-producing statements only
  - expansion of macro-call statement only
- ☐ Listing and object modules can be output on disk files or any device.
- ☐ Compatible with other Mostek Z80 assemblers and FLP-80DOS Version 2.0 or higher. Requires 32K or more of system RAM.

DESCRIPTION

MACRO-80 is an advanced upgrade from the FLP-80DOS Assembler (ASM). In addition to its macro capabilities, it provides for nested conditional assembly and allows symbol lengths of any number of characters. It supports global symbols, relocatable programs, a symbol cross-reference listing, and an unused-symbol reference table. MACRO-80 is upward compatible with all other Mostek Z80 assemblers.

The Mostek Z80 Macro Assembler (MACRO-80) is designed to run on the Mostek Dual-Disk Development System with 32K or more of RAM. It requires FLP-80DOS, Version 2.0 or higher. Macro pseudo-ops include the following:

MACRO/MEND	- define a macro
MNEXT	- step to next argument
MIF	- evaluate expression and branch to local macro label if true
MGOTO	- branch to local macro label
MEXIT	- terminate macro expansion
MERROR	- print error message in listing
MLOCAL	- define local macro label

Predefined macro-related parameters include the following:

%NEXP	- current number of this expansion
%NARC	- number of arguments passed to expansion
#PRM	- expand last-used argument
%NPRM	- number of last-used argument
%NCHAR	- number of characters in argument

The operations manual describes in detail all facilites available in MACRO-80 and provides a host of examples and sample print-outs.

ORDERING INFORMATION

DESIGNATOR	DESCRIPTION	PART NO.
MACRO-80	Z80 Macro Assembler, binary program supplied on a standard FLP-80DOS diskette, with Operations Manual.	MK78165
	MACRO-80 Operations Manual	MK79635

MACRO-70
MK79085

FEATURES

- Assembles standard 3870/F8 instruction set to produce relocatable, linkable object modules.
- Provides nested conditional assembly, an extensive expression evaluation capability, and an extended set of assembler pseudo-ops:

ORG	- origin
EQU	- equate
DC	- define constant
DEFL	- set/define macro label
DEFM	- define message
DEFB	- define byte
DEFW	- define word
DEFS	- define storage
END	- end of program
GLOBAL	- global symbol definition
NAME	- module name definition
PSECT	- program section definition
IF/ENDIF	- conditional assembly
INCLUDE	- include another file in source module
LIST/NLIST	- list on/off
CLIST	- code listing only of macro expansions
ELIST	- list/no list of macro expansions
EJECT	- eject a page of listing
TITLE	- place title on listing

- Provides options for obtaining a printed cross-reference listing, terminating after pass one if errors are encountered, redefining standard MK3870 opcodes via macros, and obtaining an unused-symbol reference table.
- Provides the most advanced macro handling capability on the microcomputer market, which includes:
  - optional arguments
  - default arguments
  - looping capability
  - global/local macro labels
  - nested/recursive expansions
  - integer/boolean variables
  - string manipulation
  - conditional expansion based on symbol definition
  - call-by-value facility
  - expansion of code-producing statements only
  - expansion of macro-call statements only
- An extended instruction set for the MK3870 is defined via a macro definition file and is shipped with the MACRO-70 diskette.
- Listing and object modules can be output on disk files or any device.
- Compatible with other Mostek 3870/F8 assemblers and FLP-80DOS Version 2.0 or higher. Requires 32K or more of system RAM.

DESCRIPTION

MACRO-70 is an advanced upgrade from the 3870/F8 Cross Assembler (FZCASM). In addition to its macro capabilities, it provides for nested conditional assembly and allows symbol lengths of any number of characters. It supports global symbols, relocatable programs, a symbol cross-reference listing, and an unused-symbol reference table. MACRO-70 is upward compatible with all other Mostek 3870/F8 Assemblers.

The Mostek 3870/F8 Macro Assembler (MACRO-70) is designed to run on the Mostek Dual-Disk Development System with 32K or more of RAM. It requires FLP-80DOS, Version 2.0 or higher. Macro pseudo-ops include the following:

MACRO/MEND	- define a macro
MNEXT	- step to next argument
MIF	- evaluate expression and branch to local macro label if true
MGOTO	- branch to local macro label
MEXIT	- terminate macro expansion
MERROR	- print error message in listing
MLOCAL	- define local macro label

Predefined macro-related parameters include the following:

%NEXP	- current number of this expansion
%NARC	- number of arguments passed to expansion
#PRM	- expand last-used argument
%NPRM	- number of last-used argument
%NCHAR	- number of characters in argument

The operations manual describes in detail all facilities available in MACRO-70 and provides a host of examples

and sample print-outs. An extended instruction set which is designed to ease programming for the MK3870 is defined in the manual. The new instructions are provided on the MACRO-70 diskette in the form of a macro definition file which can be included in a source program.

Downloading to other Mostek systems is facilitated by a utility program called F8DUMP, which is supplied on the MACRO-70 diskette.

ORDERING INFORMATION

DESGINATOR	DESCRIPTION	PART NO.
MACRO-70	3870/F8 Macro Cross Assembler, binary program supplied on a standard FLP-80DOS diskette. Includes F8DUMP utility, an extended instruction set, macro definition file, and the Operations Manual.	MK79085
	MACRO-70 Operations Manual	MK79635

MOSTEK®

SOFTWARE PRODUCTS

FLP-80DOS

MK78142, MK77962

INTRODUCTION

The Mostek FLP-80DOS software package is designed for the Mostek dual floppy disk Z80 Development System or an MD board system. Further information on this system can be found in the MATRIX™ Data Sheet. FLP-80DOS includes:

- ☐ Monitor
- ☐ Debugger
- ☐ Text Editor
- ☐ Z80 Macro Assembler
- ☐ Relocating Linking Loader
- ☐ Peripheral Interchange Program
- ☐ Linker
- ☐ A Generalized I/O System For Peripherals

These programs provide state-of-the-art software for developing Z80 programs as well as establishing a firm basis for OEM products.

MONITOR

The Monitor provides user interface from the console to the rest of the software. The user can load and run system programs, such as the Assembler, using one simple command. Programs in object and binary format can be loaded into and dumped from RAM. All I/O is done via channels which are identified by Logical Unit Numbers. The Monitor allows any software device handler to be assigned to any Logical Unit Number. Thus, the software provides complete flexibility in configuring the system with different peripherals. The Monitor also allows two-character mnemonics to represent 16-bit address values. Using mnemonics simplifies the command language. Certain mnemonics are reserved for I/O device handlers such as 'DK' for the flexible disk handler. The user can create and assign his own mnemonics at any time from the console, thus simplifying the command language for his own use. The Monitor also allows "batch mode operation" from any input device or file.

The Monitor commands are:

$ASSIGN - assign a Logic Unit Number to a device.
$CLEAR - remove the assignment of a Logical Unit Number to a device.
$RTABLE - print a list of current Logic Unit Number-to-Device assignments.

FLP-80DOS

$DTABLE - print default Logical Unit Number-to-Device assignments.
$LOAD - load object modules into RAM.
$GTABLE - print a listing of global symbol table.
$GINIT - initialize global symbol table.
$DUMP - dump RAM to a device in object format.
$GET - load a binary file into RAM from disk.
$SAVE - save a binary file on disk.
$BEGIN - start execution of a loaded program.
$INIT - initialize disk handler.
$DDT - enter DDT debug environment.
IMPLIED RUN COMMAND - get and start execution of a binary file.

DESIGNER'S DEVELOPMENT TOOL - DDT

The DDT debugger program is supplied in ROM for debugging relocatable and absolute Z80 programs. Standard commands allow displaying and modifying memory and CPU registers, setting breakpoints, and executing programs. Mnemonics are used to represent Z80 registers, thus simplifying the command language.

The allowed commands are:

B - Insert a breakpoint in user's program.
C - Copy contents of a block of memory to another location in memory.
E - Execute a program.
F - Fill an area of RAM with a constant.
H - 16-bit hexadecimal arithmetic.
L - Locate and print every occurrence of an 8-bit pattern.
M - Display, update, or tabulate the contents of memory.
P - Display or update the contents of a port.
R - Display the contents of the user's register.
S - Hardware single step - requires Mostek's AIM-80 board or AIM-Z80A board.
W - Software single step.
V - Verify memory (compare two blocks and print differences).

TEXT EDITOR -EDIT

The FLP-80DOS Editor permits random-access editing of ASCII character strings. The Editor works on blocks of characters which are rolled in from disk. It can be used as a line-or character-oriented editor. Individual characters may be located by position or context. Each edited block is automatically rolled out to disk after editing. Although the Editor is used primarily for creating and modifying Z80 assembly language source statements, it may be applied to any ASCII text delimited by "carriage returns".

The Editor has a pseudo-macro command processing option. Up to two sets of commands may be stored and processed at any time during the editing process. The Editor allows the following commands:

An - Advance record pointer n records.
Bn - Backup record pointer n records.
Cn dS1dS2d - Change string S1 to string S2 for n occurrences.
Dn - Delete the next n records.
En - Exchange current records with records to be inserted.
Fn - If n = 0, reduce printout to console device (for TTY and slow consoles).
I - Insert records.
Ln - Go to line number n.
Mn - Enter commands into one of two alternate command buffers (pseudo-macro).
Q - Quit - Return to Monitor.
Sn dS1d - Search for nth occurrence of string S1.
T - Insert records at top of file before first record.
Vn - Output n records to console device.
Wn - Output n records to Logical Unit Number five (LUN 5) with line numbers.
Xn - Execute alternate command buffer n.

Z80 ASSEMBLER - ASM

The FLP-80DOS Assembler reads standard Z80 source mnemonics and pseudo-ops and outputs an assembly listing and object code. The assembly listing shows address, machine code, statement number, and source statement. The code is in industry-standard hexadecimal format modified for relocatable, linkable assemblies.

The Assembler supports conditional assemblies, global symbols, relocatable programs, and a printed symbol table. It can assemble any length program, limited only by a symbol table size of over 400 symbols. Expressions involving arithmetic and logical operations are allowed. Although normally used as a two-pass assembler, the Assembler can also be run as a single-pass assembler or as a learning tool. The following pseudo-ops are supported:

COND - same as IF.
DEFB - define byte.
DEFL - define label.
DEFM - define message (ASCII).
DEFS - define storage.
DEFW - define word.
END - end statement.
ENDC - same as ENDIF.
ENDIF - end of conditional assembly.
EQU - equate label.
GLOBAL - global symbol definition.
IF - conditional assembly.
INCLUDE - include another file within an assembly.
NAME - program name definition.
ORG - program origin.
PSECT - program section definition.
EJECT - eject a page of listing.
TITLE - place heading at top of each page of listing.
LIST - turn listing on.
NLIST - turn listing off.

RELOCATING LINKING LOADER - RLL

The Mostek FLP-80DOS Relocating Linking Loader provides state-of-the-art capability for loading programs into memory. Loading and linking of any number of relocatable or nonrelocatable object modules is done in one pass. A non-relocatable module is always loaded at its starting address as defined by the ORG pseudo-op during assembly. A relocatable object module can be positioned anywhere in memory at an offset address.

The Loader automatically links and relocates global symbols which are used to provide communication or linkage between program modules. As object modules are loaded, a table containing global symbol references and definitions is built up. The symbol table can be printed to list all global symbols and their load address. The number of object modules which can be loaded by the Loader is limited only by the amount of RAM available for the modules and the symbol table.

The Loader also loads industry-standard non-relocatable, non-linkable object modules.

LINKER - LINK

The Linker provides capability for linking object modules together and for creating a binary (RAM image) file on disk. A binary file can be loaded using the Monitor GET or IMPLIED RUN command. Modules are linked together using global symbols for communication between modules. The linker produces a global symbol table and a global cross reference table which may be listed on any output device.

The Linker also provides a library search option for all global symbols undefined after the specified object modules are processed. If a symbol is undefined, the Linker searches the disk for an object file having the file-name of the symbol. If the file is found, it is linked with the main module in an attempt to resolve the undefined symbol.

PERIPHERAL INTERCHANGE PROGRAM - PIP

The Peripheral Interchange Program provides complete file maintenance facilities for the system. In addition, it can be used to copy information from any device or file to any other device or file. The command language is easy to use and resembles that used on DEC minicomputers. The following commands are supported:

COMMAND	FUNCTION
APPEND	Append files.
COPY	Copy files from any device to another device or file.
DIRECT	List Directory of specified Disk Unit.
ERASE	Delete a file.
FORMAT	Format a disk.
INIT	Initialize the disk handler.
RENAME	Rename a file.
STATUS	List number of used and available sectors on specified disk unit.
QUIT	Return to Monitor.

The first letter only of each command may be used.

DISK OPERATING SOFTWARE

The disk software, as well as being the heart of the MATRIX development system, can be used directly in OEM applications. The software consists of two programs which provide a complete disk handling facility.

INPUT/OUTPUT CONTROL SYSTEM - IOCS

The first package is called the I/O Control System (IOCS). This is a generalized blocker/deblocker which can interface to any device handler. Input and output can be done via the IOCS in any of four modes:

1. Single-byte transfer.
2. Line at a time, where the end of a line is defined by carriage return.
3. Multibyte transfers, where the number of bytes to be transferred is defined as the logical record length.
4. Continuous transfer to end-of-file, which is used for binary (RAM-image) files.

The IOCS provides easy application of I/O oriented packages to any device. There is one entry point, and all parameters are passed via a vector defined by the calling program. Any given handler defines the physical attributes of its device which are, in turn, used by the IOCS to perform blocking and deblocking.

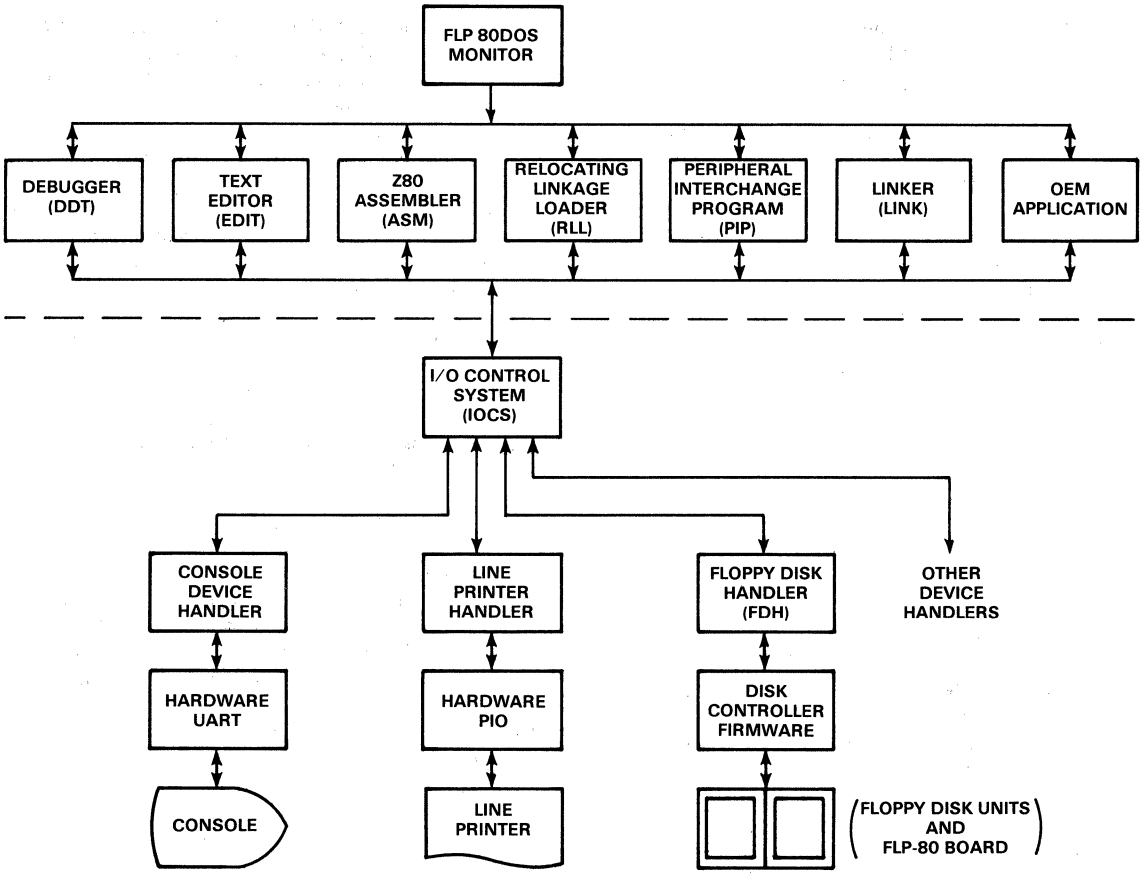
FLOPPY DISK HANDLER - FDH

The Floppy Disk Handler (FDH) interfaces from the IOCS to a firmware controller for up to four floppy disk units. The FDH provides a sophisticated command structure to handle advanced OEM products. The firmware controller interfaces to Mostek's FLP-80E Controller Board. The disk format is IBM 3740 soft sectored. The software can be easily adapted to double-sided and double-density disks. The Floppy Disk Handler commands include:

- erase file
- create file
- open file
- close file
- rename file
- rewind file
- read next n sectors
- reread current sector
- read previous sector
- skip forward n sectors
- skip backward n sectors
- replace (rewrite) current sector
- delete n sectors

The FDH has advanced error recovery capability. It supports a bad sector map and an extensive directory which allows multiple users. The file structure is doubly-linked to increase data integrity on the disk, and a bad file can be recovered from either its start or end.

FLP-80 DOS BLOCK DIAGRAM



ORDERING INFORMATION

DESIGNATOR	DESCRIPTION	PART NO.
FLP-80DOS	SDE based development system software (SD PROMs)	MK78142
FLP-80DOS	MD based development system software (MD PROMs)	MK77962
	FLP-80DOS Operations Manual Only	MK78557

FLEXIBLE DISK OPERATING SYSTEM - **M/OS-80**

USER FEATURES

- ☐ CP/M™ compatibility gives the user many available programs to choose from.
- ☐ Additional utilities and systems commands provide increased capability and functionality to the user.
- ☐ Provided on standard media for use with Mostek standard systems and MD Series boards for short system integration time.

INTRODUCTION

MO/S-80 is a CP/M™ compatible, floppy disk operating system for the MD or SD series of microcomputer board systems. It offers a comprehensive solution to a wide variety of system design problems. The software is provided on an 8-inch single-sided, single-density floppy diskette which can be booted on Mostek disk-development systems or user-configured systems (see "Hardware Required" paragraph). M/OS-80 can be altered for different input/output hardware configurations by using the MOSGEN Utility (sold separately).

Several powerful utilities are provided with M/OS-80. These programs give the user a broad base of support and will improve design efficiency. These include:

Editior (Edit)
Designer's Development Tool (Debugger)
Transfer Utility (XFER)
File/Disk Dumps (DSKDUMP)
Print Utility (PRINT)
Print Spooler (SPOOL)
Several System Utilities

Because of M/OS-80's C/PM compatibility, a large number of pre-written programs are available. M/OS-80 is designed to run programs written for other CP/M-compatible operating systems, such as CDOS™, I/OS™, and SDOS™, provided these programs conform to the standards described by Digital Research in versions 1.4 through 2.2. Virtually all compilers and interpreters now sold for use on CP/M (versions 1.4 -2.2) will work. For those Mostek customers who are currently running FLP-80DOS, M/OS-80 provides a direct migration path to CP/M compatibility without any changes to the system hardware.

SYSTEM FEATURES

M/OS-80 is a more sophisticated and powerful floppy disk operating system than any other micro-operating system available. It provides the user with a unique, but invisible, library structure. By assigning one system disk as a Master Library disk, the system can free the user to place all application-related files on another disk while still having the utility of the various system programs on-line.

Unlike other operating systems, M/OS-80 provides the user with comprehensive error messages. In most cases, methods of recovery are displayed and the operator is given several options from which to choose.

HARDWARE REQUIRED

M/OS-80 is currently supplied in three versions. V3 is designed to run on Mostek's MATRIX systems and on systems built with MD Series boards. An MD Series system must contain the following boards:

Item	Hardware Required
Processor	MDX-CPU1 or MDX-CPU2
Console Interface	MDX-EPROM/UART or MDX-SIO
Printer Interface	MDX-PIO or MDX-SIO
Floppy Interface	MDX-FLP1 or MDX FLP2
Memory	(2) MDX-DRAM with 64K of RAM

The V5 system is for use with a Mostek Phantom PROM system configuration. The following boards are required:

Item	Hardware Required
Processor	MDX-CPU3 or MDX-CPU4
Floppy Interface	MDX-FLP2
Memory	(2) MDX-DRAM with 64K of RAM (required only for MDX-CPU4)

The V6 system is for use with a Mostek Phantom hard-disk system. The following boards are required:

XI

CP/M is a Trademark of Digital Research, Inc.
CDOS is a Trademark of Cromemco, Inc.
SDOS is a Trademark of SD Systems, Inc.
I/OS is a Trademark of Infosoft Systems, Inc.

Item	Hardware Required
Processor	MDX-CPU3 or MDX-CPU4
Floppy Interface	MDX-FLP2
Memory	(2) MDX-DRAM with 64K of RAM (required only for MDX-CPU4)
Hard Disk Interface	MDX-SASI1

With either the V3, V5 or V6, M/OS-80 requires 64K bytes of RAM for operation. Four bootstrap PROMs are supplied with V3, and one bootstrap PROM is supplied with V5 or V6. The system initially must have at least one 8-inch, single-sided, single-density floppy disk drive in order to boot-up M/OS-80. Up-to-four disk drives are supported. The V6 configuration can also boot-up from hard disk.

Table 1 details the peripheral and CPU configurations required for the M/OS-80 versions.

M/OS-80 CONFIGURATION SUMMARY
Table 1

PERIPHERALS	CPU1	CPU2	CPU3	CPU4*
UART Console	V3	V3	N/A	N/A
SIO Console	V3	V3	N/A	N/A
STI Console	N/A	N/A	V5	V5
SIO Line Printer	V3**	V3**	V5**	V5**
PIO Line Printer	V3	V3	N/A	N/A
STI Line Printer	N/A	N/A	V5	V5
FLP1	V3	V3	N/A	N/A
FLP2	V3***	V3***	V5	V5
SASI	*	*	V6	V6

N/A Not Applicable.
* Future Design.
** SIO line printer configuration is supplied as alternate on systems disk.
*** Single-density only.

NOTE:
1. MOSGEN Utility may be purchased to configure systems for different peripherals and smaller sizes of RAM. See the MOSGEN Data Sheet for more information.

EDIT - Text Editor

The ASCII EDITor file provided with M/OS-80 provides a text editor for users who do not have access to a screen-editor. The editor allows creation and modification of the text files by several easy-to-use commands. EDIT features include:

- Find a text string
- Change a text string
- Find a line
- Insert new text
- Delete a line(s) or character(s)
- Put a block of text into another file
- Get a block of text from another file
- View text on the console screen
- Print text on the line printer
- Create a set of commands which can be executed as a macro

XFER — Transfer Utility

The XFER program is a general-file transfer utility. It allows for the moving of files from disks or devices to other (or the same) disks or devices. The XFER features include:

- Transfer an ASCII file
- Compare two files without moving
- Filter out illegal ASCII characters
- Conditionally transfer a file (user prompted)
- Transfer a Read-Only file
- Expand tabs
- Verify files after moving
- Print HEX address of comparison failure
- Transfer only old files
- Transfer only new files

DSKDUMP - Disk Dump

The DSKDUMP program allows reading or modifying of a file, the disk data area, or the disk directory. Each block requested is read into a 128-byte buffer, then displayed. The blocks are numbered sequentially. Any block can be selected, displayed, modified, and written back to the disk.

PRINT - Print Utility

The PRINT utility formats ASCII files to the CRT or printer with automatic headings, tabbing and pagination. User-specified options include page width and length, page headings, date printed of the top of each page, and page formatting.

SPOOL - Print Spooler

The SPOOL file system feature is used to output a file from the printer to a system list device while the system continues with other functions. Any ASCII file may be spool-printed, and direct printer activity is prevented while a spool-print is active.

Other System Utilities

M/OS-80 provides several other system utilities to permit a user the highest degree of flexibility in the manipulation of the files and programs created and used with the system. Some of these utilities include: programs to format disks, change disk labels, examine directories, and to diagnose disk problems. A PROM programming utility is also included that interfaces with Mostek's PPG 8/16.

ORDERING INFORMATION

DESIGNATOR	DESCRIPTION	PART NO.
M/OS-80 V3	One diskette containing all M/OS-80 programs in binary, four bootstrap PROMs, and one Operations Manual. (See Table 1 for hardware configuration requirements.) Requires the signed Software License Agreeement (enclosed) with purchase order.	MK71010C-81
M/OS-80 V5	One diskette containing all M/OS-80 programs in binary, one bootstrap PROM, and one Operations Manual. (See Table 1 for hardware configuration requirements.) Requires the signed Software License Agreement (enclosed) with purchase order.	MK71011C-81
M/OS-80 V6	One diskette containing all M/OS-80 programs in binary, one PROM for booting from floppy or hard disk, and an Operations Manual. (See Table 1 for hardware configuration requirements.) Requires the signed Software License Agreement (enclosed) with purchase order.	MK71012C-81
M/OS-80 Operations Manual	Detailed description of the operation and use of the M/OS-80 software package.	4420064

MOSGEN UTILITY
MK71001

USER FEATURES

- ☐ Adapts M/OS-80 to customized MDX and SD systems.
- ☐ Allows tailoring M/OS-80 for different I/O devices and RAM sizes.
- ☐ Works on systems configured around the DDT/DCF PROMs or Phantom PROM.
- ☐ Menu driven format to speed the configuration process.

DESCRIPTION

Mostek's MOSGEN Utility is a system generation package used to generate unique configurations of the M/OS-80 Operating System. MOSGEN allows the user to modify the M/OS-80 by rewriting existing I/O drivers or creating new drivers for specialized I/O operation, and configuring different system RAM sizes.

MOSGEN allows creation of a command file which will link a newly customized system. The MOSGEN package also includes a set of object and source files to provide the user with a valid set of device drivers. These drivers are provided to help the user create new drivers based on known-working examples. Users are permitted to modify or select drivers for the following logical-unit devices:

- System Console (output)
- Keyboard (input)
- List
- Punch
- Reader
- Disk
- Clock

MOSGEN is supplied on two single-sided, single-density 8-inch diskettes. They are the System Generation diskette and the Device Drivers/Library diskette.

MOSGEN OPERATION

The MOSGEN package creates a batch submit (.CMD) file which, when executed, walks the system through the complex re-assembly, trial linkage, and final linkage process automatically and without operator intervention. The last steps of the MOSGEN-created batch file test the newly-created system for errors in linkage, size, and conformity to system restrictions. The user-supplied drivers are linked into the main core of the system during this linkage process. A special linkage editor is provided for the sole purpose of this system generation link. MOSGEN proves itself useful, if not essential, when system restrictions limit the amount of available RAM in the target system, or require the use of non-standard peripherals or special-intelligent I/O drivers.

MOSGEN may be used to configure M/OS-80 for different sizes of RAM in the user system down to a minimum of 24K bytes.

MOSGEN SYSTEM REQUIREMENTS

MOSGEN and all related software require the user to have a running 64K M/OS-80 system in place. Depending on the requirements of the users development languages, the system memory requirements may be in excess of the 32K bytes of RAM required for a minimum M/OS-80 system.

ORDERING INFORMATION

DESIGNATOR	DESCRIPTION	PART NO.
MOSGEN Utility	Two diskettes containing MOSGEN system generation utilities and device drivers, both source and object files, and one Operations Manual. A signed Software License Agreement is required with purchase order.	MK71001C-80
MOSGEN Operations Manual	Detailed description of the operation and use of the MOSGEN Utility.	4420270

1982/1983 MICROELECTRONIC DATA BOOK

INTRODUCTION

Overview

Mostek's Military/Hi-Rel Products Department serves the special needs of the Defense, Aerospace and Commercial Hi-Rel markets. The organization's principal objective is to provide Mostek's state-of-the-art products screened to MIL-STD 883 Class B, Methods 5004 and 5005.

Traditional Military IC manufacturers have met stringent Military reliability requirements at a cost of being several years behind the state-of-the-art in commercial products. Mostek Military brings the leading edge in high reliability RAM, ROM, EPROM, Gate Array and microprocessor devices to the Military systems designer today. As MIL-M-38510 slash sheets are announced, the Military Products Department will qualify Mostek's products in the JAN 38510 program. Mostek has already received QPL listing of its 4116 dynamic RAM. Designated JM-38510/240, this device is one of the most advanced MOS circuits to receive QPL listing to date.

The Military Products Department is also heavily engaged in the development of high density leadless chip carrier packaging technology. Most circuits are currently offered in carriers or planned for the near future.

Product offerings are broken into two categories. Devices prefixed "MKB" are screened to the full requirements of MIL-STD-883 Class B. "MKI" (Industrial grade) prefixed devices are screened to a subset of 883B requirements and offer high reliability at significantly reduced cost (see the following sections for more detail concerning MKI products).

Quality Conformance/Reliability

Mostek has been providing MKB versions of selected memory products since 1978. Quality conformance inspections in accordance with Method 5005 of MIL-STD-883 are a central part of MKB screening procedures. Group A inspections are performed on a 100% basis to the requirements contained in the detail specification (Mostek data sheet). Group B, C and D inspections are performed periodically per the requirements of MIL-STD-883.

A data report documenting the results of Group B, C and D testing is available.

For more information contact:

Mostek Corporation
Military Products Department
Mail Station 1100
P.O. Box 169
Carrollton, Texas 75006

Telephone - (214) 323-7926/7718
TWX - 910-860-5856
Telex - 730423

APPLICATION	Military/Aerospace				Industrial				Commerical		Medical
TYPE OF SYSTEM	Ground	Airborne	Tactical Missile	Space	Process Control	Instrumen-tation	Telecom	Automotive Instrumen-tation	FAA	Airborne	Instrumen-tation
MOSTEK HI-REL TYPE	MKB/ MKI	MKB/JAN		Class S Equiv.	MKI				MKB/MKI		MKI

XII

SCD PROGRAM SIMPLIFIES DESIGN ACCEPTANCE AND DOCUMENTATION

To speed up the documentation cycle for government acceptance of a "non-standard part", Mostek has developed an innovative customer-oriented program. It's called Support-Customer-Documentation (SCD). This ready-made source control document is a complete procurement specification, per MIL-STD 883 Class B (Mostek MKB), for those devices without an existing DESC drawing or slash sheet. Patterned after DESC mini specifications, SCD provides a reliable, detailed spec. So detailed, in fact, that the only additional items required are your company's name and part number.

The Mostek SCD documents are available for all new military devices and will be written around DDL103 Guidelines for DESC Selected Item Drawings.

MOSTEK MILITARY/HI-REL SCREENING ATTRIBUTES

JAN—(MIL-M-38510 Slash Sheet)

- QPL listed, qualified per MIL-M-38510, Class B
- Tested to MIL-STD 883B, MIL-M-38510, and appropriate military specifications
- Produced in DESC-certified domestic wafer fabrication, assembly and test facilities

MKB—(MIL-STD-883)

- Compliance with MIL-STD 883, Method 5004, Level B
- 1/2 to 1/3 the cost of JAN circuits
- Quality conformance testing per method 5005, Groups B, C, D
- No charge for Group B, C and D generic data
- Group A data summary and certificate of compliance included with all shipments
- Off-the-shelf delivery from factory and distributor stock
- 10% burn-in PDA
- Available for broad spectrum of VLSI, RAM, ROM, EPROM and microprocessor devices

MKI—(Industrial Grade)

- Cost-effective: Nominal cost-adder over commerical hermetic devices, generally half of MKB (883B) cost
- Greater reliability than commercial device
- Eliminates logistics problems caused by sending units to outside burn-in labs
- Built-in reliability –40°C to +85°C operating range
- 44 hours minimum, 125°C MIL burn-in
- Hermetic packaging
- 0.4% parametric and functional outgoing AQL
- Available for most Mostek RAM, EPROM and microprocessor components

SCREENING AND LOT CONFORMANCE COMPARISON

ACTIVITY/ SCREEN	MKI (INDUSTRIAL)	MKB (883B METHOD 5004)	JAN
Die Inspection	75X Mostek Spec.	2010 Cond. B	2010 Cond. B
Pre-Seal Inspection	30X-60X Mostek Spec.	2010 Cond. B	2010 Cond. B
Stabilization Bake		1008 Cond. C	1008 Cond. C
Temperature Cycle	5 Cycles, 1010 Cond. C	1010 Cond. C	1010 Cond. C
Centrifuge	2001 Cond. D, 20 Kg, Y_1	2001 Cond. E	2001 Cond. E
Fine Leak	1014 Cond. B, 1 x 10^{-7} atm cc/sec	1014 Cond. C	1014 Cond. C
Gross Leak	Mostek Spec.	1014 Cond. C	1014 Cond. C
Voltage Stress (DRAMs Only)	1015 Cond. D 10 Hrs. Min., 125°C	1015 Cond. D 10 Hrs. Min., 125°C	Per Slash Sheet
Burn-In	1015 Cond. D 44 Hrs. Min. 125°C dynamic	1015 Cond. D 160 Hrs. Min. 125°C dynamic	1015 Cond. D 160 Hrs. Min. 125°C dynamic
Electrical Tests	Method 5005 Group A electrical subgroups, testing conditions and limits which guarantee AC, DC and functional performance over full temp. range.	Group A tests for AC, DC and functional performance at detail spec. min. and max. temp.	Tests for AC, DC and func. performance in conformance with slash sheet.
External Visual	Visual tests to guarantee marking, construction and mechanical integrity	2009	2009
QA Lot Acceptance	Method 5005 Group A sample testing to guarantee performance to data sheet over full temp. range.	5005 Group A and C. of C.	5005 Group A and C. of C.
Quality Conformance		5005 Groups B, C, D	5005 Groups B, C, D

PART NUMBER ORDERING INFORMATION

EXAMPLE: MKB 3880 P – 83

SCREENING	PART TYPE	PACKAGE	TEMPERATURE	SPEED
MKB=MIL-STD-883 Level B testing MKI=Industrial/Commercial hi-rel screening	Mostek device name	D=dual density RAM-PAC™ E=leadless chip carrier: JEDEC E/F F=flat package J=cerdip P=side-brazed DIP	7=Industrial Range (–40° to +85°C) 8=Military Range* (device dependent)	One or two number designator denoting access time. Device dependent)

MKI INDUSTRIAL PRODUCTS LISTING

Product	Device	Organization	Packages	Temp. Range	Access Time or Frequency
Dynamic RAMs	MKI4116-72	16K x 1	J	–40°C/+85°C	150 ns
	MKI4116-73	16K x 1	J	–40°C/+85°C	200 ns
	MKI4116-74	16K x 1	J	–40°C/+85°C	250 ns
	MKI4564-72	64K x 1	J	–40°C/+85°C	150 ns
Static RAMs	MKI4118A-71	1K x 8	J	–40°C/+85°C	120 ns
	MKI4118A-72	1K x 8	J	–40°C/+85°C	150 ns
	MKI4118A-73	1K x 8	J	–40°C/+85°C	200 ns
	MKI4802-790	2K x 8	J	–40°C/+85°C	90 ns
	MKI4802-71	2K x 8	J	–40°C/+85°C	120 ns
ROMs	MKI37000-74†	8K x 8	J	–40°C/+85°C	300 ns
EPROMs	MKI2716-77	2K x 8	J	–40°C/+85°C	390ns
	MKI2716-78	2K x 8	J	–40°C/+85°C	450 ns
Microprocessors	MKI3880-70	Z80 CPU	P	–40°C/+85°C	2.5 MHz
	MKI3880-74	Z80A CPU	P	–40°C/+85°C	4.0 MHz
	MKI3881-70	Z80 PIO	P	–40°C/+85°C	2.5 MHz
	MKI3881-74	Z80 PIO	P	–40°C/+85°C	4.0 MHz
	MKI3882-70	Z80 CTC	J	–40°C/+85°C	2.5 MHz
	MKI3882-74	Z80 CTC	J	–40°C/+85°C	4.0 MHz

†1982 Introduction

JAN PRODUCTS LISTING

Product	Device	Organization	Pkgs.	Temp. Range	Access Times/Freq.	Active Power	Standby Power
JAN Dynamic RAMs (4116)	JM-38510/24001 BEC	16K x 1	P	–55°C/+110°C	200 ns	462 mW	30 mW
	JM-38510/24002 BEC	16K x 1	P	–55°C/+110°C	250 ns	462 mW	30 mW

MKB MILITARY PRODUCTS LISTING

Product	Device	Organization	Pkgs.	Temp. Range	Access Times/Freq.	Active Power	Standby Power
Dynamic RAMs	MKB4116-82	16K x 1	E,F,J	-55°C/+110°C	150 ns	462 mW	30 mW
	MKB4116-83	16K x 1	E,F,J	-55°C/+110°C	200 ns	462 mW	30 mW
	MKB4116-84	16K x 1	E,F,J	-55°C/+110°C	250 ns	462 mW	30 mW
	MKB4516-81	16K x 1	E,P	-55°C/+110°C*	120 ns		
	MKB4564-82	64K x 1	E,P	-55°C/+110°C*	150 ns		
	MKB4564-83	64K x 1	E,P	-55°C/+110°C*	200 ns		
	MKB4564-84	64K x 1	E,P	-55°C/+110°C*	250 ns		
	MKM4332-83	32K x 1	D	-55°C/+110°C	200 ns	495 mW	60 mW
	MKM4332-84	32K x 1	D	-55°C/+110°C	250 ns	495 mW	60 mW
Static RAMs RAMs	MKB4104-84	4K x 1	E,J	-55°C/+125°C	250 ns	150 mW	53 mW
	MKB4104-85	4K x 1	E,J	-55°C/+125°C	300 ns	150 mW	53 mW
	MKB4104-86	4K x 1	E,J	-55°C/+125°C	350 ns	150 mW	53 mW
	MKB4167-885	16K x 1	E,P	-55°C/+125°C*	85 ns		
	MKB4167-870	16K x 1	E,P	-55°C/+125°C*	70 ns		
	MKB4118A-82	1K x 8	E,P	-55°C/+125°C	150 ns	500 mW	
	MKB4118A-83	1K x 8	E,P	-55°C/+125°C	200 ns	500 mW	
	MKB4801A-890	1K x 8	E,P	-55°C/+125°C	90 ns		
	MKB4801A-81	1K x 8	E,P	-55°C/+125°C	120 ns		
	MKB4802-890*	2K x 8	E,P	-55°C/+125°C*	90 ns	630 mW	
	MKB4802-81	2K x 8	E,P	-55°C/+125°C	120 ns	630 mW	
	MKB4802-83	2K x 8	E,P	-55°C/+125°C	200 ns	630 mW	
ROMs	MKB36000-83	8K x 8	P	-55°C/+125°C	250 ns	220 mW	55 mW
	MKB36000-84	8K x 8	P	-55°C/+125°C	300 ns	220 mW	55 mW
	MKB37000-84*	8K x 8	E,P	-55°C/+125°C*	300 ns	165 mW	45 mW
EPROMs	MKB2716-86	2K x 8	E,J	-55°C/+125°C	350 ns	633 mW	165 mW
	MKB2716-87	2K x 8	E,J	-55°C/+125°C	390 ns	633 mW	165 mW
	MKB2716-88	2K x 8	E,J	-55°C/+125°C	450 ns	633 mW	165 mW
Micro-processors	MKB3880-80	Z80 CPU	P	-55°C/+125°C	2.5 MHz	1.0 W	
	MKB3880-84	Z80A CPU	P	-55°C/+125°C	4.0 MHz	1.0 W	
	MKB3881-80*	Z80 PIO	P	-55°C/+125°C	2.5 MHz		
	MKB3881-84*	Z80 PIO	P	-55°C/+125°C	4.0 MHz		
	MKB3882-80*	Z80 CTC	P	-55°C/+125°C	2.5 MHz		
	MKB3882-84	Z80 CTC	P	-55°C/+125‡C	4.0 MHz		
	MKB3884/5/7†	Z80 SIO	P	-55°C/+125°C			

*1982 Introduction
†Planned

QUALITY CONFORMANCE
TEST REPORT
GROUPS B, C AND D
1978 - 1981

NOTE: This report covers testing performed through June 1981. For a more recent report, contact your local Mostek representative.

GROUP B INSPECTION - METHOD 5005.7
Chart 1

TEST	METHOD	CONDITIONS	CLASS B
Subgroup 1 Physical dimension	2016		2 devices (No failures)
Subgroup 2 Resistance to solvents	2015		4 devices (No failures)
Subgroup 3 Solderability	2003	Soldering temperature of 260 ± 10°C	15 leads (3 units min (No failures)
Subgroup 4 Internal visual and mechanical	2014	Failure criteria from design and construction requirements of applicable procurement document	1 device (No failures)
Subgroup 5 Bond strength	2011	Test condition C or D	15 Bonds (10 units min (No failures)
Subgroup 6 Internal water vapor content	1018	1,000 PPM max @ 100°C	3 devices (No failures)
Subgroup 7 Seal	1014	As Applicable	5
Subgroup 8 Electrical parameters ESD sensitivity Electrical parameters	Group A, Subgroup 1 3015 Test Condition A or B Group A, Subgroup 1		15

GROUP C INSPECTION - METHOD 5005.7

Chart 2

TEST	METHOD	CONDITIONS	CLASS B LTPD
Subgroup 1			
Operating Life Test	1005	Test conditions to be specified 1000 hours @ 125°C	5
End point electricals		As specified in the applicable detail specification	
Subgroup 2			
Temperature cycling	1010	Test condition C	15
Constant acceleration	2001	Test condition E, Y1 axis	
Seal	1014	As applicable	
Fine			
Gross			
Visual examination	1010		
End point electrical parameters		As specified in applicable device specification	

GROUP D INSPECTION - METHOD 5005.7
Chart 3

TEST	METHOD	CONDITIONS LTPD	CLASS B LTPD
Subgroup 1			
Physical dimensions	2016		15
Subgroup 2			
Lead integrity	2004	Test conditions B2 (lead fatigue)	15
Seal	1014	As applicable	
Fine			
Gross			
Lid torque	2024	As applicable	
Subgroup 3			
Thermal shock	1011	Test condition B, 15 cycles	15
Temperature cycling	1010	Test condition C, 100 cycles	
Moisture resistance	1004		
Seal	1014	As applicable	
Fine			
Gross			
Visual examination	1004/2009		
End point electrical parameters		As specified in the applicable device specification	
Subgroup 4			
Mechanical shock	2002	Test condition B	15
Vibration, variable freq.	2007	Test condition A	
Constant acceleration	2001	Test condition E, Y1 Axis	
Seal	1014	As applicable	
Fine			
Gross			
Visual examination	1010 or 1011		
End point electrical parameters		As specified in the applicable device specification	
Subgroup 5			
Salt atmosphere	1009	Test condition A	15
Seal	1014	As applicable	
Visual examination	1009	Paragraph 3.3.1 of Method 1009	
Subgroup 6			
Internal water vapor content	1018	5,000 ppm max @ 100°C	3 devices (No failures)
Subgroup 7			
Adhesion of lead finish	2025		15

GROUP B TEST RESULTS

Chart 4

		Subgroup									
		B-1		B-2		B-3		B-4		B-5	
Package	Year	Samples	Rejects	Samples	Rejects	Samples	Rejects	Samples	Rejects	Samples	Rejects
16 Pin*	1979	30	0	51	3	42	0	17	0	80	0
P package	1980	28	0	67	0	39	0	16	0	70	0
(side brazed)	1981	20	0	48	0	30	0	13	0	302	2
16 Pin	1979	74	0	119	1	114	0	42	0	281	0
J package	1980	50	0	46	0	39	0	21	0	89	0
(CERDIP)	1981	18	0	37	0	29	1	9	0	225	1
16 Pin	1979	154	0	324	0	195	0	84	0	700	1
F package	1980	52	0	105	0	75	0	23	0	76	0
(flatpack)	1981	85	0	248	0	154	0	45	1	1075	2
18 Pad	1979										
E package	1980	14	0	18	0	18	0	7	0	36	0
(chip carrier)	1981	10	0	4	0	16	0	5	0	125	0
18 Pin	1979										
P package	1980	8	0	16	0	12	0	4	0	16	0
(side brazed)											
18 Pin	1979	8	0	12	0	12	0	4	0	40	0
J package	1980	28	0	47	0	24	0	12	0	48	0
(CERDIP)	1981	6	0	12	0	9	0	8	2	75	4
24 Pin	1979	34	0	60	0	66	0	19	0	128	0
P package	1980	30	0	43	0	33	0	15	0	60	0
(side brazed)	1981	10	0	24	0	15	0	5	0	325	2
24 Pin	1979										
T package	1980	15	0	24	0	18	0	9	0	162	0
(side brazed	1981	16	0	43	1	30	0	9	0	176	0
w/window)											
24 Pin											
J package	1980	45	0	15	0	15	0	15	0	15	0
(w/window)	1981	28	0	61	0	64	0	14	0	375	9
40 Pin											
P package											
(side brazed)	1981	4	0	4	0	7	0	2	0	50	0

*Includes data from M38510/24001BEC (JAN MKB4116P) subgroups 6 (water vapor and 7 (VZAP) passed with no failures.

GROUP C TEST RESULTS
Chart 5

Microcircuit Group[2]	Device Type	Year	Subgroup C-1 Samples	C-1 Rejects	C-2[1] Samples	C-2[1] Rejects	C-3 Samples	C-3 Rejects
46-NMOS RAM	STATIC	1979	440	0	108	0	152	0
		1980	430	0	100	2	152	0
		1981	213	3	50	1	76	0
	DYNAMIC	1979	1306	5	294	1	380	0
		1980	755	3	230	1	338	0
		1981	214	3	50	0	76	0
	JAN/240	1980	105	2	25	0	110	0
47-NMOS ROM/PROM	MASK ROM	1979	330	3	108	3	152	0
		1980	215	1	54	1	76	0
		1981	315	3	75	0	114	0
	UVEPROM	1980	210	2	50	0	76	0
		1981	107	2	25	1	38	0

NOTES: 1) Subgroup C-2 testing is performed following the completion of Subgroup C-1 testing.
2) See Chart 7 for Microcircuit Group Assignment.

FAILURE RATE CALCULATIONS
Chart 6

Based upon Group C testing per MIL-M-38510, failure rates for the following devices have been determined.

Device	Hours	Failure Rate at 125°C	Average Activation Energy	Failure Rate at 70°C	Failure Rate at 55°C
2716	317,000	0.63 %/Khr	0.8 eV	.015%/Khr	.0044%/Khr
36000	860,000	0.814	0.68	.034	.012
4027	537,000	0.372	0.61	.022	.0085
4104	977,000	0.102	0.57	.0071	.0030
4116	1,738,000	0.288	0.76	.0083	.0026
4118	106,000	1.89	0.67	.083	.029

NOTES: 1) Derating performed using the Arrhenius equation. Refer to the Reliability Report for more information.
2) Activation energies based upon analysis of Group C failures.

GROUP D TEST RESULTS
Chart 7

		Subgroup													
		D-1		D-2		D-3		D-4		D-5		D-6		D-7	
Package	Year	Sam.	Rej.	Sam.	Rej.	Sam.	Rej.	Sam.	Rej.	Sam.	Rej.	Sam.	Rej.	Sam.	Rej.
16 Pin P[1]	1979	75	0	29	0	75	0	80	1	50	0				
	1980	50	0	50	0	75	0	50	0	50	0				
16 Pin J	1979	125	0	75	0	55	6	180	9	151	2				
	1980	50	0	50	0	80	1	50	0	50	0				
	1981	50	0	50	0	50	0	50	0	50	0	6	0	30	0
16 Pin F	1980	25	0	25	0	25	6	25	0	25	3				
18 Pad E	1980	25	0	25	0	47	0	47	4	25	2				
18 Pin P	1979	26	0	25	0	30	0	30	0	25	1				
18 Pin J	1980	25	0	50	0	25	1	50	0	50	0				
	1981	75	0	75	0	75	0	75	0	75	0	15	0	45	0
24 Pin P	1979	76	0	185	0	77	0	47	3	27	0				
	1980	76	0	50	0	50	0	75	2	50	0				
	1981	25	0	25	0	25	0	25	0	25	0	3	0	15	0
24 Pin J	1980	32	0	32	0	32	0	32	0	106	0				
	1981	25	0	25	0	25	1	25	0	25	0	5	0	15	0
24 Pin T	1980	24	0	58	0	53	0	97	1	25	0				

NOTES: 1) Includes M38510/24001BEC (JAN 4116)
2) Subgroups 6 and 7 added in Method 5005.7 dated 4 Nov. 1980

MICROCIRCUIT GROUP ASSIGNMENTS PER MIL-M-38510E

Chart 8

Microcircuit Group 46
NMOS RAM

MKB4027	4K X 1	Dynamic RAM	16 pin
MKB4116	16K X 1	Dynamic RAM	16 pin
MKB4104	4K X 1	Static RAM	18 pin
MKB4118	1K X 8	Static RAM	24 pin

Microcircuit Group 47
NMOS ROM/PROM

MKB2716	2K X 8	UV Eraseable PROM	24 pin
MKB36000	8K X 8	ROM	24 pin

MOSTEK

MILITARY/HIGH-REL PRODUCTS

Processed to MIL-STD-883, Method 5004, Class B

2048 x 8-Bit UV Erasable PROM

MKB2716(J/E)-86/87/88/90

FEATURES

- Military temperature range ($-55°C \leq T_A \leq +125°C$)
- Qualified per Method 5005, MIL-STD 883. Group B, C, D data report available
- Available processed to DESC selected item drawing number 78022 (part no. 7802201JX)
- Pin compatible with Mostek's BYTEWYDE™ memory family
- Single +5 volt power supply during read operation
- Low power dissipation: 663 mW max active, 165 mW max standby
- Three state output OR-tie capability
- Five modes of operation for greater system flexibility (see Table)

P/N	Access Time
MKB2716-86	350 ns
MKB2716-87	390 ns
MKB2716-88	450 ns
MKB2716-90	550 ns

- Single programming requirement: single location programming with one 50 msec pulse
- Industrial MKI version available (-40°C to 85°C)
- TTL compatible in all operating modes
- Standard 24 pin JEDEC DIP pinout

DESCRIPTION

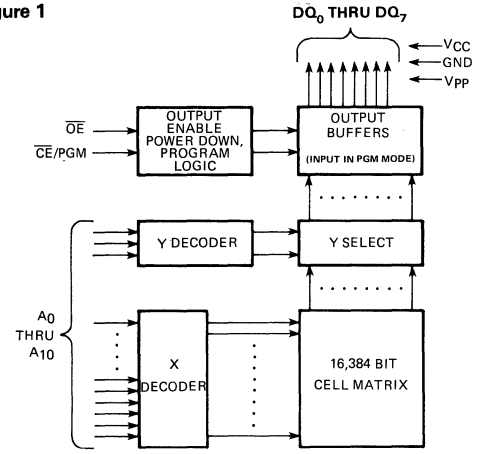
The MKB2716 is a 2048 x 8 bit electrically programmable/ ultraviolet erasable read only memory. The circuit is fabricated with Mostek's advanced N-channel silicon gate technology for the highest performance and reliability. The MKB2716 offers significant advances over hardwired logic cost, system flexibility, turnaround time and performance.

The device has many useful system oriented features including a standby mode of operation which lowers power from 633 mW maximum active power to 165 mW maximum for an overall savings of 75%.

Programming is done with a single TTL level pulse, and may

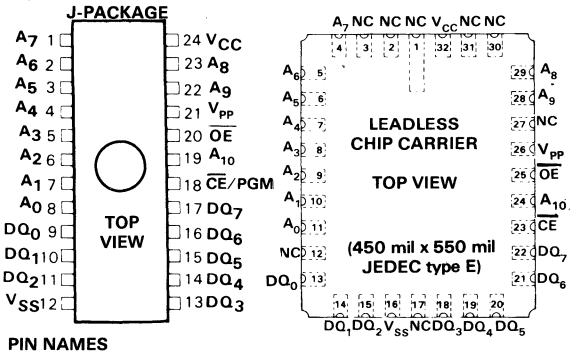
BLOCK DIAGRAM

Figure 1



PIN CONNECTIONS

Figure 2



PIN NAMES

A_0 - A_{10}	Addresses	DQ_0 - DQ_7	Data Outputs*
$\overline{CE}$/PGM	Chip Enable/ Program	$\overline{OE}$	Output Enable
		V_{SS}	Ground

*Inputs in Program Mode

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ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to V_{SS} (Except V_{PP}) ..... -0.3 V to +6 V
Voltage on V_{PP} supply pin relative to V_{SS} ..... -0.3 V to +28 V
Operating Temperature T_A (Ambient) ..... $-55°C \leq T_A \leq +125°C$
Storage Temperature (Ambient) ..... $-65°C \leq T_A \leq +125°C$
Power Dissipation ..... 1 Watt
Short Circuit Output Current ..... 50 mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

READ OPERATION

RECOMMENDED DC OPERATING CONDITIONS

($-55°C \leq T_A \leq 125°C$)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{IH}	Input High Voltage	2.0		$V_{CC}+1$	V	
V_{IL}	Input Low voltage	-0.1		0.8	V	

DC ELETRICAL CHARACTERISTICS[1,2,4,8]

($-55°C \leq T_A \leq 125°C$) ($V_{CC}$ = +5 V ± 10%, $V_{PP} = V_{CC}$)[2]

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
I_{CC1}	V_{CC} Standby Power Supply Current (OE = V_{IL}; CE = V_{IH})		10	30	mA	2
I_{CC2}	V_{CC} Active Power Supply Current (OE = CE = V_{IL}) T_A = -55°C		57	115	mA	2,10
	T_A = +125°C		43	90		
I_{PP1}	V_{PP} Current (V_{PP} = 5.5 V)		2.0	10	mA	2
V_{OH}	Output High Voltage (I_{OH} = -400 µA)	2.4			V	
V_{OL}	Output Low Voltage (I_{OL} = 2.1 mA)			.45	V	
I_{IL}	Input Leakage Current V_{IN} = 5.5 V)			10	µA	
I_{OL}	Output Leakage Current (V_{OUT} = 5.5 V)			10	µA	

AC ELECTRICAL CHARACTERISTICS[1,2,5]

($-55°C \leq T_A \leq 125°C$) ($V_{CC}$ = +5 V ± 10%, $V_{PP} = V_{CC}$)[2]

		-86		-87		-88		-90			
SYM	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
t_{ACC}	Address to Output Delay ($\overline{CE}$ = $\overline{OE}$ = V_{IL})		350		390		450		550	ns	
t_{CE}	CE to Output Delay ($\overline{OE}$ = V_{IL})		350		390		450		550	ns	5
t_{OE}	Output Enable to Output Delay ($\overline{CE}$ = V_{IL})		150		150		150		180	ns	9
t_{DF}	Chip Deselect to Output Float ($\overline{CE}$ = V_{IL})	0	130	0	130	0	130	0	130	ns	8
t_{OH}	Address to Output Hold ($\overline{CE}$ = $\overline{OE}$ = V_{IL})	0		0		0		0		ns	

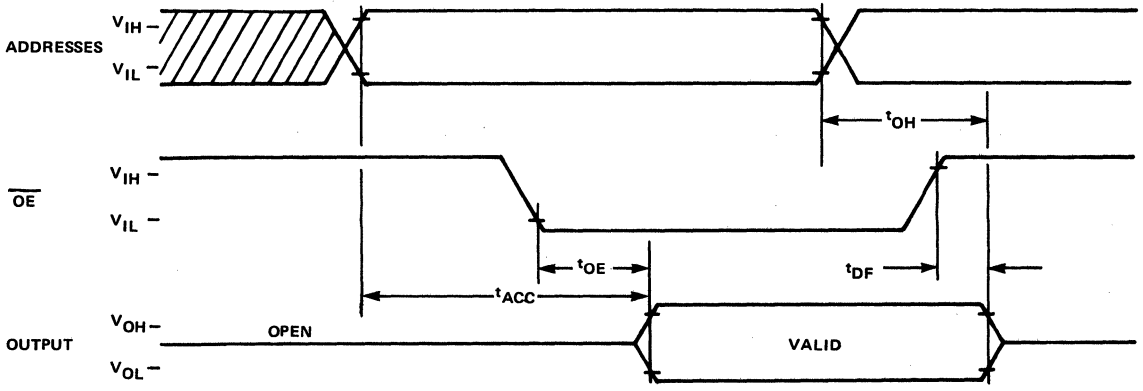
CAPACITANCE
(T_A = 25°C)

SYM	PARAMETER	TYP	MAX	UNITS	NOTES
C_{IN}	Input Capacitance	4	6	pF	6
C_{OUT}	Output Capacitance	8	12	pF	6

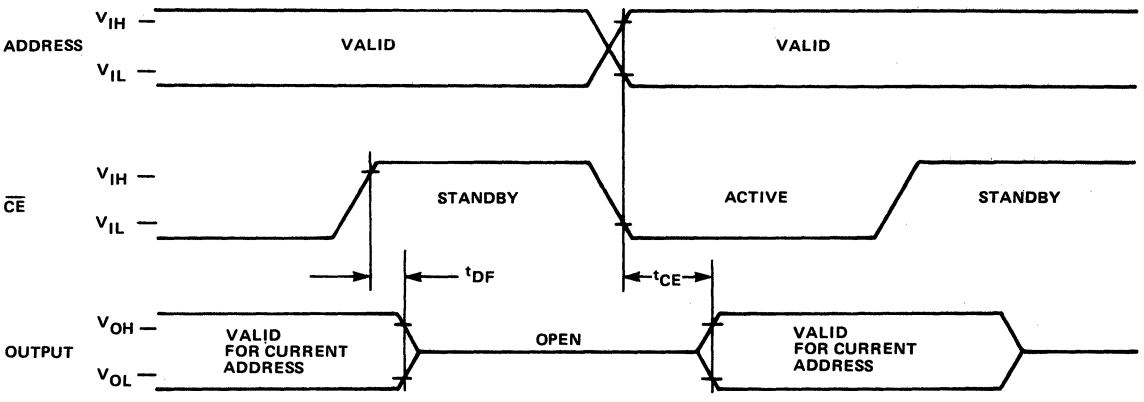
READ OPERATION NOTES:

1. V_{CC} must be applied at the same time or before V_{PP} and removed after or at the same time as V_{PP}.
2. V_{PP} and V_{CC} may be connected together except during programming. With $V_{PP} = V_{CC}$, the supply current is the sum of I_{CC} and I_{PP1}.
3. All voltages with respect to V_{SS}.
4. Load conditions = 1 TTL load and 100 pf, $t_r = t_f$ = 20 ns, reference levels are 1 V and 2 V for inputs and .8 V and 2 V for outputs.
5. t_{OE} is referenced to $\overline{CE}$ or the addresses, whichever occurs last.
6. Effective Capacitance calculated from the equation $C = \frac{\Delta Q}{\Delta V}$ where $\Delta V = 3V$.
7. Typical numbers are for T_A = 25°C and V_{CC} = 5.0 V.
8. t_{DF} is applicable to both $\overline{CE}$ and $\overline{OE}$, which occurs first.
9. $\overline{OE}$ may follow up to t_{ACC}-t_{OE} after the falling edge of $\overline{CE}$ without affecting t_{ACC}.
10. Power consumption decreases with temperature from a maximum at low temperature to a minimum at high temperature.

TIMING DIAGRAMS
READ CYCLE ($\overline{CE}$ = V_{IL})
Figure 3



STANDBY POWER DOWN MODE ($\overline{OE}$ = V_{IL})
Figure 4



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PROGRAM OPERATION

RECOMMENDED DC OPERATING CONDITIONS[8]

(T_A = 25°C ± 5°C) (V_{CC} = +5 V ± 10%, V_{PP} = 25 V ± 1 V)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
V_{IL}	Input Low Level	-0.1	0.8	V	
V_{IH}	Input High Level	2.0	V_{CC} + 1	V	

DC ELECTRICAL CHARACTERISTICS

(T_A = 25°C ± 5°C) (V_{CC} = +5 V ± 10%, V_{PP} = 25 V ± 1 V)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
I_{IL}	Input Leakage Current		10	μA	3
I_{CC}	V_{CC} Power Supply Current		100	mA	
I_{PP1}	V_{PP} Supply Current		10	mA	4
I_{PP2}	V_{PP} Supply Current during Programming Pulse		30	mA	5

RECOMMENDED AC OPERATING CONDITIONS AND ELECTRICAL CHARACTERISTICS[1,2,6,7]

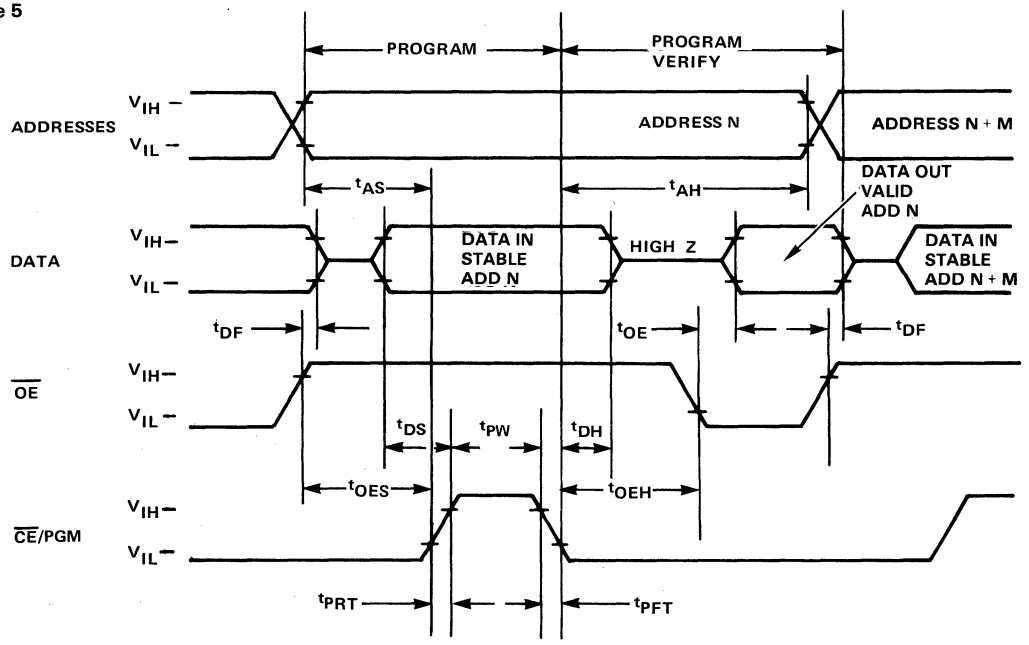
(T_A = 25°C ± 5°C) (V_{CC} = +5 V ± 10%, V_{PP} = 25 V ± 1 V)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
t_{AS}	Address Setup Time	2			μs	
t_{OES}	$\overline{OE}$ Setup Time	2			μs	
t_{DS}	Data Setup Time	2			μs	
t_{AH}	Address Hold Time	2			μs	
t_{OEH}	$\overline{OE}$ Hold Time	2			μs	
t_{DH}	Data Hold Time	2			μs	
t_{DF}	Output Enable to Output Float	0		130	ns	4
t_{OE}	Output Enable to Output Delay			120	ns	4
t_{PW}	Program Pulse Width	45	50	55	ms	
t_{PRT}	Program Pulse Rise Time	5			ns	
t_{PFT}	Program Pulse Fall Time	5			ns	

PROGRAM OPERATION NOTES:

1. V_{CC} must be applied at the same time or before V_{PP} and removed after or at the same time as V_{PP}. To prevent damage to the device it must not be inserted into a board with V_{PP} at 25 V.
2. Care must be taken to prevent overshoot of the V_{PP} supply when switching to +25 V.
3. 0.45 V ≤ V_{IN} ≤ 5.50 V
4. $\overline{CE}$/PGM = V_{IL}.
5. $\overline{CE}$/PGM = V_{IH}.
6. t_T = 20 nsec.
7. 1 V and 2 V for inputs and .8 V and 2 V for outputs are used as timing reference levels.
8. Although speed selections are made for read operation all programming specifications are the same for all dash numbers.

TIMING DIAGRAM
(Program Mode)
Figure 5



MODE SELECTION

	Pin:			
Mode	$\overline{CE}$/PGM (18)	$\overline{OE}$ (20)	V_{PP} (21)	Output
Read	V_{IL}	V_{IL}	+5	Valid Out
Standby	V_{IH}	Don't Care	+5	Open
Program	Pulsed V_{IL} to V_{IH}	V_{IH}	+25	Data Inputs
Program Verify	V_{IL}	V_{IL}	+25	Valid Out
Program Inhibit	V_{IL}	V_{IH}	+25	Open
V_{CC} (24) = 5 V all modes				

DESCRIPTION (Continued)

be done at any individual word address, sequencially or at random. The three-state output controlled by the $\overline{OE}$ input allows OR-tie capability for construction of large arrays. A single power supply requirement of +5 volts makes the MKB2716 ideally suited for use with Mostek's 5-volt only microprocessors such as the MKB3880 (Z80). The MKB2716 is packaged in the industry standard 24-pin dual-in-line package with a transparent, hermetically sealed lid. This allows the user to expose the chip to ultraviolet light to erase the data pattern. A new pattern may then be written into the device by following the program procedures outlined in this data sheet.

The MKB2716 is specifically designed to fit those applications where fast turnaround time and pattern experimentation are required. Since data may be altered in the device (erase and reprogram) it allows for early debugging of the system program. Since single location programming is available the MKB2716 can have its data content increased (assuming all 2048 bytes were not programmed) at any time for easy updating of system capabilities in the field. Once the contents become fixed and the system enters production, mask programmable ROMs can offer speed, cost per bit and power per bit benefits. Mostek offers the MKB36000 and MKB37000 8 K x 8 ROMs which allow the user to quadruple memory density in the application. A "ROM Programming Guide" is available to aid the user in preparing the code for submission once prototyping with MKB2716s has verified its accuracy.

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READ OPERATION

The MKB2716 has five basic modes of operation. Under normal operating conditions (non-programming) there are two modes; READ and STANDBY. A READ operation is accomplished by maintaining pin 18 ($\overline{CE}$) at V_{IL} and pin 21 (V_{PP}) at +5 volts. If $\overline{OE}$ (pin 20) is held active low after addressing (A_0 - A_{10} have stabilized) then valid output data will appear on the output pins at access time t_{ACC} (address

access). In this mode, access time may be referenced to $\overline{OE}$ (t_{OE}) depending on when $\overline{OE}$ occurs (see timing diagrams).

POWER DOWN operation is accomplished in STANDBY mode by taking pin 18 ($\overline{CE}$) to a TTL high level (V_{IH}). The power is reduced by 75% from 633 mW maximum to 165 mW. During power down V_{PP} must be at +5 volts, and the outputs will be open-circuit regardless of the condition of $\overline{OE}$. Access time from a high to low transition of $\overline{CE}$ (t_{CE}) is the same as from addresses (t_{ACC}). (See STANDBY Timing Diagram).

PROGRAMMING INSTRUCTIONS

The MKB2716 is shipped from Mostek completely erased. In this initial state, and after any subsequent erasure, all bits will be at a '1' level (output high). Information is introduced by selectively programming '0's into the proper bit locations. Once a '0' has been programmed into the chip it may be changed only by erasing the entire chip with UV light.

The MKB2716 is put into the PROGRAM mode by maintaining V_{PP} at +25 V, and $\overline{OE}$ at V_{IH}. In this mode the output pins serve as inputs (8 bits in parallel) for the required program data. Word address selection is done the same as in the READ mode, and logic levels for other inputs and the V_{CC} supply voltage are the same as in the READ mode.

To program a "byte" (8 bits) of data, a TTL active high level pulse is applied to the $\overline{CE}$/PGM pin after address inputs and data have stabilized. Each location to be programmed must have a pulse applied, and only one pulse per location is required. Any individual location, a sequence of locations or locations at random may be programmed in this manner. (The program pulse has a maximum width of 55 msec, and programming must not be attempted with a high level D.C. signal applied to the $\overline{CE}$/PGM pin.)

PROGRAM INHIBIT is another useful mode of operation when programming multiple, parallel addressed MKB2716's with different data. It is necessary only to maintain $\overline{OE}$ at V_{IH}, V_{PP} at +25, allow addresses and data to stabilize, and pulse the $\overline{CE}$/PGM pin of the device to be programmed. The devices with $\overline{CE}$/PGM at V_{IL} will not be programmed. Data may then be changed and the next device pulsed.

PROGRAM VERIFY allows the MKB2716 program data to be verified without having to reduce V_{PP} from +25 V to +5 V. V_{PP} = 25 V should only be used in the PROGRAM, PROGRAM INHIBIT and PROGRAM VERIFY modes and must be at +5 V in all other modes.

MKB2716 ERASING PROCEDURE

The MKB2716 may be erased by exposure to high intensity ultraviolet light, illuminating the chip through the transparent window. This exposure to ultraviolet light induces the flow of a photo current from the floating gate, thereby discharging the gate to its initial state. An ultraviolet source of 2537Å yielding a total integrated dosage of 15 Watt-seconds/cm^2 is required. Note that all bits of the MKB2716 will be erased. The erasure time is approximately 15 to 20 minutes utilizing a ultra-violet lamp with a 12000 μW/CM^2 power rating. The lamp should be used without short wave filters, and the MKB2716 to be erased should be placed about one inch away from the lamp tubes. It should be noted that as the distance between the lamp and the chip is doubled, the exposure time required goes up by a factor of 4. The UV content of sunlight is not sufficient to provide a practical means of erasing the MKB2716. However, it is recommended that the MKB2716 not be operated or stored in direct sunlight, as the UV content of sunlight may cause erasure of some bits in a short period of time.

MOSTEK®

64K-BIT READ-ONLY MEMORY

Processed to MIL-STD-883, Method 5004, Class B

MKB36000(P/J)-80/83/84

FEATURES

- MKB36000 8K x 8 Organization - "Edge Activated" operation (CE)
- Maximum access time: 300ns (—84)
  250ns (—83)
  250ns (—80)
- Low Power Dissipation — 220mW max active
- Extended operating ambient temperature range
  ($-55°C \leq T_A \leq +125°C$): —84
  ($-55°C \leq T_A \leq +125°C$):—83
  ($-40°C \leq T_A \leq +80°C$):—80
- Standard 24 pin DIP (EPROM Pin Out Compatible)
- Low Standby Power Dissipation — 55mW typical (CE High)
- On chip latches for addresses
- Inputs and three-state outputs-TTL compatible
- Outputs drive 2 TTL loads and 100 pF
- Ruggedized for use in severe military environments
- Single +5V ± 10% power supply

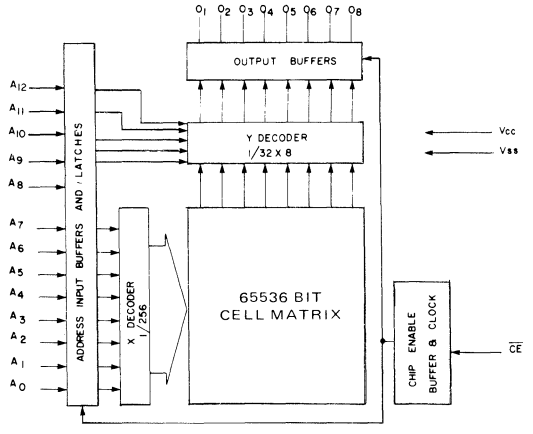
DESCRIPTION

The MKB36000 is a new generation N-channel silicon gate MOS Read Only Memory, organized as 8192 words by 8 bits. As a state-of-the-art device, the MKB36000 incorporates advanced circuit techniques designed to provide maximum circuit density and reliability with the highest possible performance, while maintaining lower power dissipation and wide operating margins.

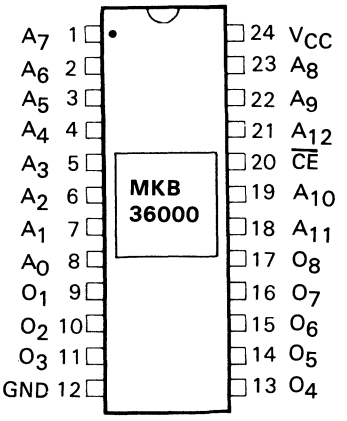
The MKB36000 utilizes what is fast becoming an industry standard method of device operation. Use of a static storage cell with clocked control periphery allows the circuit to be put into an automatic low power standby mode. This is accomplished by maintaining the chip enable ($\overline{CE}$) input at a TTL high level. In this mode, power dissipation is reduced to typically 35mW, as compared to unclocked deviced which draw full power continuously. In system operation, a device is selected by the $\overline{CE}$ input, while all other are in a low power mode, reducing the overall system power. Lower power means reduced power supply cost, less heat to dissipate and an increase in device and system reliability.

The edge activated chip enable also means greater system flexibility and an increase in system speed. The MKB36000 features onboard address latches controlled by the $\overline{CE}$ input. Once the address hold time specification has been met, new address data can be applied in anticipation of the next cycle. Outputs can be

FUNCTIONAL DIAGRAM



PIN CONNECTIONS



XII

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Terminal Relative to V_{SS} ..... -0.5V to +7V
Operating Temperature T_A (Ambient) -83/84..... -55°C to +125°C
Operating Temperature T_A (Ambient) -80..... -40°C to +85°C
Storage Temperature — Ceramic (Ambient) ..... -65°C to +150°C
Power Dissipation ..... 1 Watt

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS[6]

($-55°C \leq T_A \leq +125°C$) for -84; ($-40° \leq T_A \leq +85°C$) for -80

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Power Supply Voltage	4.5	5.0	5.5	Volts	6
V_{IL}	Input Logic 0 Voltage	-1.0		0.8	Volts	
V_{IH}	Input Logic 1 Voltage	2.4		V_{CC}	Volts	

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%) (ELECTRICAL CHARACTERISTICS VALID OVER TEMPERATURE RANGE FOR EACH DEVICE)[6]

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
I_{CC1}	V_{CC} Power Supply Current Active			40	mA	1
I_{CC2}	V_{CC} Power Supply Current Standby			10	mA	7
$I_{I(L)}$	Input Leakage Current	-10		10	μA	2
$I_{O(L)}$	Output Leakage Current	-10		10	μA	3
V_{OL}	Output Logic "0" Voltage @ I_{OU1} = 3.3mA			0.4	Volts	
V_{OH}	Output Logic "1" Voltage @ I_{OU1} = 220 μA	2.4			Volts	

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%)[6] (ELECTRICAL CHARACTERISTICS VALID OVER TEMPERATURE RANGE FOR EACH DEVICE)[6]

		36000-80/83		36000-84			
SYM	PARAMETER	MIN	MAX	MIN	MAX	UNITS	NOTES
t_C	Cycle Time	375		450		ns	4
t_{CE}	CE Pulse Width	250	7500	300	7500	ns	4
t_{AC}	CE Access Time		250		300	ns	4
t_{OFF}	Output Turn Off Delay		60		75	ns	4
t_{AH}	Address Hold Time Referenced to CE	60		75		ns	4
t_{AS}	Address Setup Time Referenced to CE	0		0		ns	
t_P	CE Precharge Time	125		150		ns	

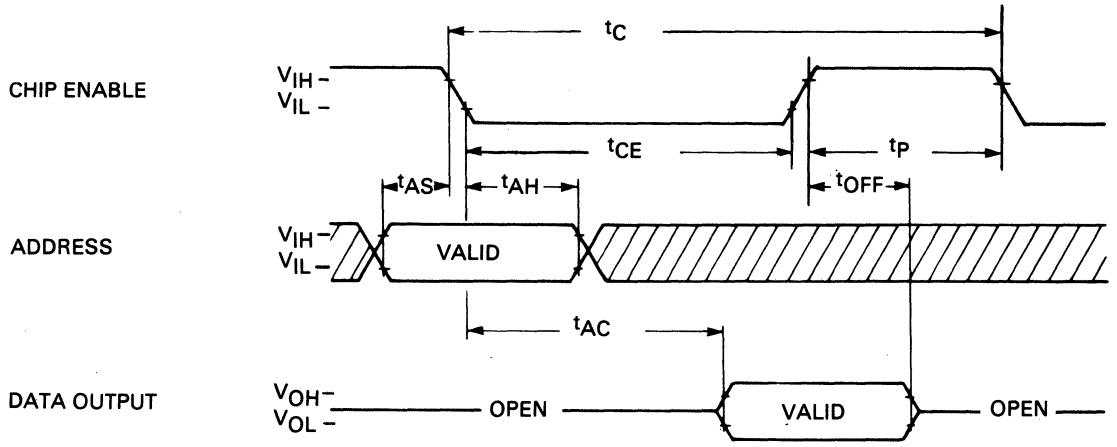
CAPACITANCE

($-55°C \leq T_A \leq +125°C$)

SYM	PARAMETER	TYP	MAX	UNITS	NOTES
C_1	Input Capacitance	5	8	pF	5
C_O	Output Capacitance	7	15	pF	5

NOTES:
1. Current is proportional to cycle rate. I_{CC} is measured at the specified minimum cycle time.
2. V_{IN} = 0V to 5.5V
3. Device unselected; V_{OUT} = 0V to 5.5V
4. Measured with 2 TTL loads and 100pF, transition times = 20ns.
5. Capacitance measured with Boonton Meter or effective capacitance calculated from the equation: $C = \frac{\Delta}{\Delta V}$ with ΔV = 3volts
6. A minimum 2ms time delay is required after the application of V_{CC} (+5) before proper device operation is achieved. $\overline{CE}$ must be high during this period.
7. $\overline{CE}$ high.

TIMING DIAGRAM



MKB 36000 ROM PUNCHED CARD CODING FORMAT (1 & 6)

	COLS	INFORMATION FIELD	DATA FORMAT	
FIRST CARD	1-30 31-50 60-72	Customer Customer Part Number Mostek Part Number (2)	512 data cards (16 data words/card) with the following format:	
			COLS	INFORMATION FIELD
SECOND CARD	1-30 31-50	Engineer at Customer Site Direct Phone Number for Engineer	1-4	Four digit octal address of first output word on card
			5-7	Three digit octal output word specified by address in column 1-4
THIRD CARD	1-5	Mostek Part Number (2)		
FOURTH CARD	1-9 15-28 35-57	Data Format (3) Logic — ("Positive Logic" or "Negative Logic") Verification Code (4)	8-52	Next fifteen output words, each word consists of three octal digits.

NOTES:
1. Positive or negative logic formats are accepted as noted in the fourth card.
2. Assigned by Mostek; may be left blank.
3. Mostek punched card coding format should be used Punch "Mostek" starting in column one.
4. Punches as (a) VERIFICATION HOLD — i.e., customer verification of the data as reproduced by Mostek is required prior to production of the ROM. To accomplish this Mostek supplies a copy of its Customer Verification Data Sheet (CVDS) to the customer. (b) VERIFICATION PROCESS — i.e., the customer will receive a CVDS but production will begin prior to receipt of customer verification; (c) VERIFICATION NOT NEEDED — i.e., the customer will not receive a CVDS and production will begin immediately.
5. 512 cards for MKB36000.
6. Please consult Mostek ROM Programming Guide for further details on other formats.

DESCRIPTION (Continued)

wire- 'OR'ed together, and a specific device can be selected by utilizing the $\overline{CE}$ input with no bus conflict on the outputs. The $\overline{CE}$ input allows the fastest access times yet available in 5 volt only ROM's and imposes no loss in system operating flexibility over an unclocked device.

Other system oriented features include fully TTL compatible inputs and outputs. The three state outputs, controlled by the $\overline{CE}$ input, will drive a minimum of 2 standard TTL loads. The MKB36000 operates from a single +5 volt power supply with a wide ± 10% tolerance, providing the widest operating margins available. The MKB36000 is packaged in the industry standard 24 pin DIP.

Any application requiring a high performance, high bit density ROM can be satisfied by the MKB36000 ROM. This device is ideally suited for 8 bit microprocessor systems such as those which utilize the Z80. It can offer significant cost advantages over PROM.

OPERATION

The MKB36000 is controlled by the chip enable ($\overline{CE}$) input. A negative going edge at the $\overline{CE}$ input will activate the device as well as strobe and latch the inputs into the onchip address registers. At access time the outputs will become active and contain the data read from the selected location. The outputs will remain latched and active until $\overline{CE}$ is returned to the inactive state.

PROGRAMMING DATA

Mostek is now able to utilize a wide spectrum of data input formats and media. Those presently available are listed in the following table:

Table 1

Acceptable Media	Acceptable Format
CARDS PAPER PROMS DATA LINK	MOSTEK INTEL CARD INTEL TAPE EA MOSTEK F-8 MOTOROLA 6800

MOSTEK®

64K-BIT READ-ONLY MEMORY

Processed to MIL-STD-883, Method 5004, Class B

MKB37000 (P/J/E) -84/85

FEATURES

- ☐ Organization: 8K x 8 Bit ROM - JEDEC Pinout
- ☐ Bytewyde version of MKB36000
- ☐ Pin compatible with Mostek's BYTEWYDE™ Memory Family

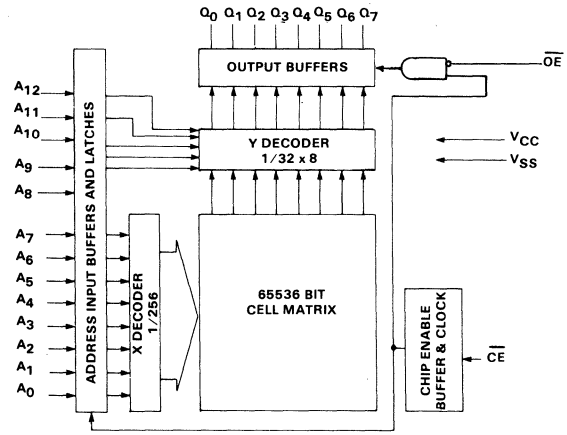
P/N	ACCESS	CYCLE
MKB37000-85	300 ns	450 ns
MKB37000-84	250 ns	375 ns

- ☐ Access Time/Cycle Time
- ☐ Mask ROM replacement for BYTEWYDE EPROMs
- ☐ No Connections allow easy upgrade to MK38000 32K x 8 ROM
- ☐ Low power dissipation: 165mW max active. 45mW max standby
- ☐ $\overline{CE}$ and $\overline{OE}$ functions facilitate Bus control
- ☐ Extended Operating Temperature Range −55°C to +125°C

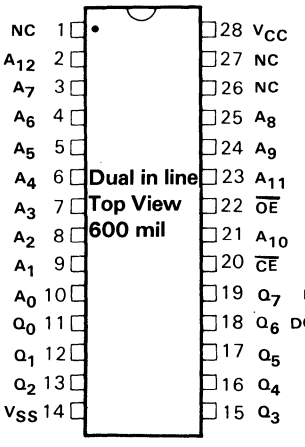
DESCRIPTION

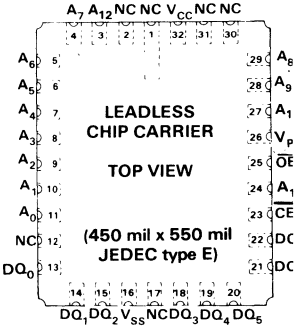
The MKB37000 is a N-channel silicon gate MOS Read Only Memory, organized as 8192 words by 8 bits. As a state-of-the-art device, the MKB37000 incorporates advanced circuit techniques designed to provide maximum circuit density and reliability with the highest possible performance, while maintaining low power dissipation and wide operating margins. The MK37000 is to be used as a pin/function compatible mask programmable alternative to BYTEWYDE 8K x 8 bit EPROMs. As a member of the Mostek BYTEWYDE Memory Family, the MKB37000 brings to the memory

FUNCTIONAL DIAGRAM (MK37000)



PIN CONNECTIONS





TRUTH TABLE

$\overline{CE}$	$\overline{OE}$	MODE	OUTPUTS	POWER
V_{IH}	X	Deselect	High-Z	Standby
V_{IL}	V_{IH}	Inhibit	High-Z	Active
V_{IL}	V_{IL}	Read	D_{OUT}	Active

X = Don't Care

A0 - A12-Address
$\overline{CE}$ - Chip Enable
Q_0 - Q_7 - Outputs

NC - No Connection
$\overline{OE}$ - Output Enable
V_{CC} - +5V supply
V_{SS} - Ground

XII

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Terminal Relative to V_{SS} ..... -1.0 V to +7 V
Operating Temperature T_C(case) ..... -55°C to 125°C
Storage Temperature-Ceramic (Ambient) ..... -65°C to +150°C
Power Dissapation ..... 1 Watt

*Stresses of greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS [6]

($-55°C \leq T_c \leq 125°C$)

SYM	PARAMETER	MIN	TYPE	MAX	UNITS	NOTES
V_{CC}	Power Supply	4.5	5.0	5.5	V	
V_{IL}	Input Logic 0 Voltage	-1.0		0.8	V	
V_{IH}	Input Logic 1 Voltage	2.0		V_{CC}	V	

DC ELECTRICAL CHARACTERISTICS [6]

(V_{CC} = 5 V ± 10%) ($-55°C \leq T_c \leq 125°C$)

SYM	PARAMETER	MIN	TYPE	MAX	UNITS	NOTES
I_{CC1}	V_{CC} Power Supply Current (Active)			30	mA	**1,8**
I_{CC2}	V_{CC} Power Supply Current (Standby)			8	mA	**7**
$I_{I(L)}$	Input Leakage Current	-10		10	μA	**2**
$I_{O(L)}$	Output Leakage Current	-10		10	μA	**3**
V_{OL}	Output Logic "0" Voltage @ I_{OUT} = 3.3mA			0.4	V	
V_{OH}	Output Logic "1" Voltage @ I_{OUT} = -220 μA	2.4			V	

AC ELECTRICAL CHARACTERISTICS [6]

(V_{CC} = 5 V ± 10%) (-55°C ≤ T_c ≤ 125°C)

SYM	PARAMETER	84		85		UNITS	NOTES
		MIN	MAX	MIN	MAX		
t_{RC}	Read Cycle Time	375		450		ns	4
t_{CE}	$\overline{CE}$ Pulse Width	250	7500-	300	7500-	ns	4
t_{CEA}	$\overline{CE}$ Access Time		250		300	ns	4
t_{CEZ}	Chip Enable Data Off Time		60		75	ns	
t_{AH}	Addressed Hold Time Referenced to $\overline{CE}$	60		75		ns	
t_{AS}	Address Setup Time Referenced to $\overline{CE}$	0		0		ns	
t_p	$\overline{CE}$ Precharge Time	125		150		ns	
t_{OEA}	Output Enable Access Time		80		100	ns	
t_{OEZ}	Output Enable Data Time Off		60		75	ns	

CAPACITANCE

(0°C ≤ T_A ≤ 70°C)

SYM	PARAMETER	TYPE	MAX	UNITS	NOTES
C_I	Input Capacitance	5	8	pF	5
C_O	Output Capacitance	7	15	pF	5

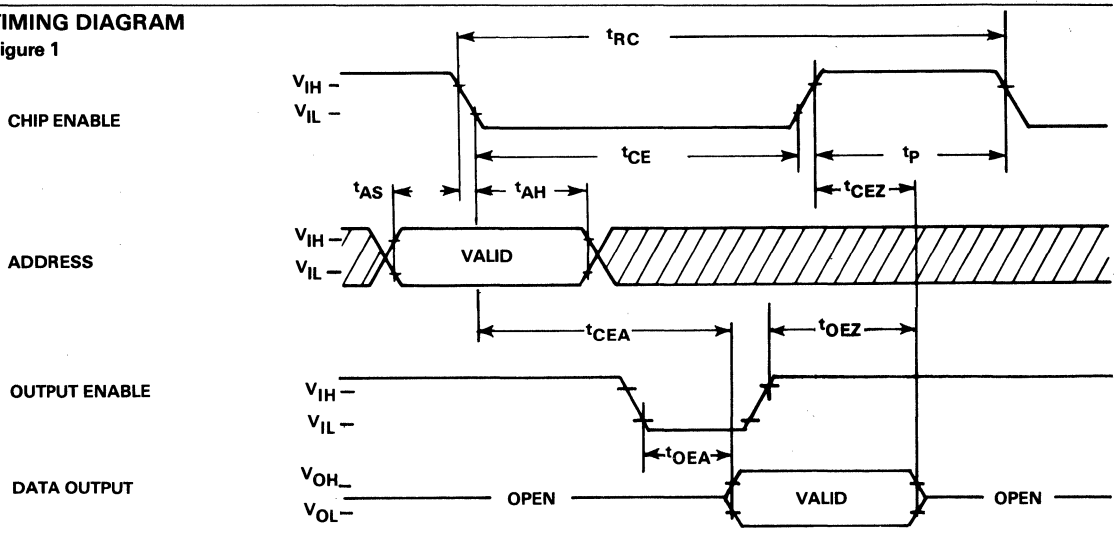
NOTES:

1. Current is proportional to cycle rate. I_{CC1} is measured at the specified minimum cycle time. Data Outputs open.
2. V_{IN} = 0 V to 5.5 V
3. Device unselected; V_{OUT} = 0 V to 5.5 V
4. Measured with 2 TTL loads and 100pF, tranisition times = 20 ns
5. Capacitance measured with Boonton Meter or effective capacitance calculated formt he equation:
   $C = \frac{\Delta Q}{\Delta V}$ with ΔV = 3 volts
6. A minimum 2ms time delay is required after the application of V_{CC} (+5) before proper device operation is achieved $\overline{CE}$ must be at V_{IH} for this time period.
7. $\overline{CE}$ high
8. Power supply current decreases with increasing temperature.

XII

TIMING DIAGRAM

Figure 1



DESCRIPTION (Continued)

market a new era of ROM, PROM and EPROM compatibility previously unavailable.

Use of clocked control periphery and a standard static ROM cell makes the MKB37000 the lowest power 64K ROM available. Power consumption is a low 165mW maximum. To provide greater system flexibility an output enable ($\overline{OE}$) function has been added using one of the extra pins available on the 28 pin DIP. This function matches that found on all of the new BYTEWYDE family of memories available from Mostek.

The use of clocked $\overline{CE}$ mode of operation provides an automatic power down mode of operation. The MKB37000 features on chip address latches controlled by the $\overline{CE}$ input. Once address hold time is met, new address data can be provided to the device in anticipation of a subsequent cycle. It is not necessary to maintain the address up to access time to access valid data. The output enable function controls only the outputs and is not latched by the $\overline{CE}$. The $\overline{CE}$ input can be used for device selection and the $\overline{OE}$ input used to avoid bus conflicts so that outputs can be 'OR'ed together when using multiple devices.

Other system oriented features include fully TTL compatible inputs and outputs. The three state outputs, controlled by the $\overline{OE}$ input, will drive a minimum of 2 standard TTL loads. The MKB37000 operates from a single +5 volt power supply with a wide +10% tolerance, providing the widest operating margins available. The MKB37000 is packaged in the industry standard 28 pin DIP. Pin 1 and 26 are not connected to allow easy upward compatibility with next generation higher density ROM which will use these pins for addresses. Pin 27 is not connected in order to maintain compatibility with RAMs which use this pin as a write enable ($\overline{WE}$) control function.

Any application requiring a high performance, high bit density ROM can be satisfied by the MKB37000. This device is ideally suited for 8 bit microprocessor systems such as those which utilize the MKB3880. It can offer significant cost advantages over EPROM.

OPERATION

The MK37000 is controlled by the chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) inputs. A negative going edge at the $\overline{CE}$ input will activate the device and latch the addresses into the on chip address registers. The output buffers, under the control of $\overline{OE}$, will become active in $\overline{CE}$ access time (t_{CEA}) if the output enable access time (t_{OEA}) requirement is met. The on-chip address register allows addresses to be changed after the specified hold time (t_{AH}) in preparation for the next cycle. The outputs will remain valid and active until either $\overline{CE}$ or $\overline{OE}$ is returned to the inactive state. After chip deselect time (t_{CEZ}) the output buffers will go to a high impedance state. The $\overline{CE}$ input must remain inactive (high) between subsequent cycles for time t_p to allow for precharging the nodes of the internal circuitry.

MK37000 ROM CODE DATA INPUT PROCEDURE

The preferred method of supplying code data to Mostek is in the form of programmed EPROMs (see table). In addition to the programmed set of blank EPROMs for supplying customer code verification . When multiple EPROMs are required to describe the ROM they shall be designated in ascending address space with the numbers 1, 2, 3, etc. As an example, EPROM #1 would start with address space 0000 and go to 07FF for a 2K x 8 device. EPROM #2 would then start at address space 0800 and so on. A total of (4) 2K x 8 devices would be required to toally describe the address space of the 8K x 8 MK37000.

A paper printout and verification approval letter will accompany each verification EPROM set returned to the customer. Approval is considered to be excepted when the signed verification letter is returned to Mostek. The original set of EPROMs will be retained by Mostek for the duration of the prototyping process. Please consult with your local Mostek representative for more information.

Acceptable EPROMs for Code Data
Table 1

EPROM	# REQUIRED
2716/2516	4
2732	2
2764	1

PRELIMINARY

PROCESSED TO MIL-STD-883, METHOD 5004 256K-BIT MOS READ-ONLY MEMORY MKB38000(P/J/E)-84/85

FEATURES

- Organized 32K x 8
- Pin compatible with Mostek's BYTEWYDE™ Memory Family
- Upward compatible with the MKB3700
- Access Time = Cycle Time
- Static Operation
- Automatic Power Down
- Temperature range: $-55°C \leq T_C \leq 125°C$
- Fully screened to MIL-STD-883 Method 5004, Class B
- $\overline{CE}$ and $\overline{OE}$ functions facilitate bus control
- Pin 27 no connection permits interchange with static RAM ($\overline{WE}$)
- High performance

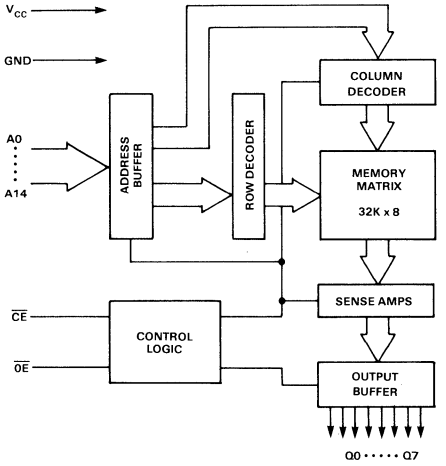
Part No.	Access Time	Cycle Time
MKB38000-84	250 ns	250 ns
MKB38000-85	300 ns	300 ns

DESCRIPTION

The MKB38000 is a N-channel silicon gate MOS Read Only Memory, organized as 32,768 words by 8 bits. As a state-of-the-art device, the MKB38000 incorporates advanced circuit techniques designed to provide maximum circuit density and reliability with the highest possible performance, while maintaining low power dissipation and wide operating margins.

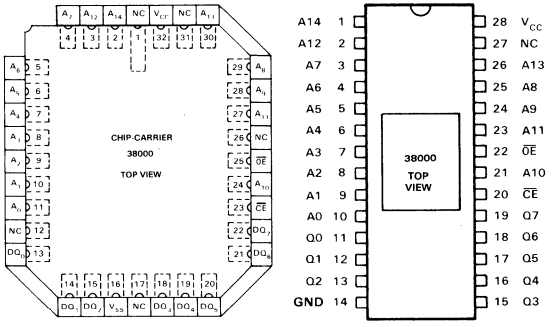
FUNCTIONAL DIAGRAM (MKB38000)

Figure 1



PIN CONNECTIONS

Figure 2



TRUTH TABLE

$\overline{CE}$	$\overline{OE}$	MODE	OUTPUTS	POWER
H	X	Deselect	High-Z	Standby
L	H	Inhibit	High-Z	Active
L	L	Read	D_{OUT}	Active

PIN NAMES

A0-A14	Address	$\overline{OE}$	Output Enable
$\overline{CE}$	Chip Enable	V_{CC}	+5 V
NC	No Connection	GND	Ground
		Q0-Q7	Data Outputs

XII

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Terminal Relative to GND ..... -0.5 V to +7 V
Operating Temperature T_C (Case) ..... 55°C to +125°C
Storage Temperature—Ceramic (Ambient) ..... -65°C to +150°C
Power Dissipation ..... 1 Watt

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS[1,6]

($-55°C \leq T_C \leq +125°C$)

SYM	PARAMETER	MIN	TYP	MAX*	UNITS	NOTES
V_{CC}	Power Supply Voltage	4.75	5.0	5.25	V	
V_{IL}	Input Logic 0 Voltage	-0.3		0.8	V	8
V_{IH}	Input Logic 1 Voltage	2.0		V_{CC}	V	

DC ELECTRICAL CHARACTERISTICS[1,6]

($V_{CC} = 5\ V \pm 5\%$) ($-55°C \leq T_C \leq +125°C$)

SYM	PARAMETER	MIN	TYP	MAX*	UNITS	NOTES
I_{CC1}	V_{CC} Power Supply Current (Active)		75	100	mA	5
I_{CC2}	V_{CC} Power Supply Current (Standby)		35	50	mA	7
$I_{I(L)}$	Input Leakage Current	-10	0.1	10	μA	3
$I_{O(L)}$	Output Leakage Current	-10	0.1	10	μA	2
V_{OL}	Output Logic "0" Voltage @ $I_{OUT} = 4$ mA			0.4	V	
V_{OH}	Output Logic "1" Voltage @ $I_{OUT} = -1$ mA	2.4			V	

NOTE:
1. *Preliminary values. Contact factory for current status

AC ELECTRICAL CHARACTERISTICS[1,4,6,9,10]

($V_{CC} = 5\ V \pm 5\%$) ($-55°C \leq T_C \leq +125°C$)

SYM	PARAMETER	-84		-85		UNITS	NOTES
		MIN	MAX	MIN	MAX		
t_{RC}	Read Cycle Time	250		300		ns	
t_{AA}	Address Access Time		250		300	ns	
t_{CEA}	CE Access Time		250		300	ns	
t_{CEZ}	Chip Enable Data Off Time		40		50	ns	
t_{CEL}	Chip Enable to Data Bus Active	5		5		ns	
t_{OEA}	Output Enable Access Time	50		60		ns	
t_{OEZ}	Output Enable Data Off Time	40		50		ns	
t_{OH}	Output Hold from Address Change	5		5		ns	

CAPACITANCE

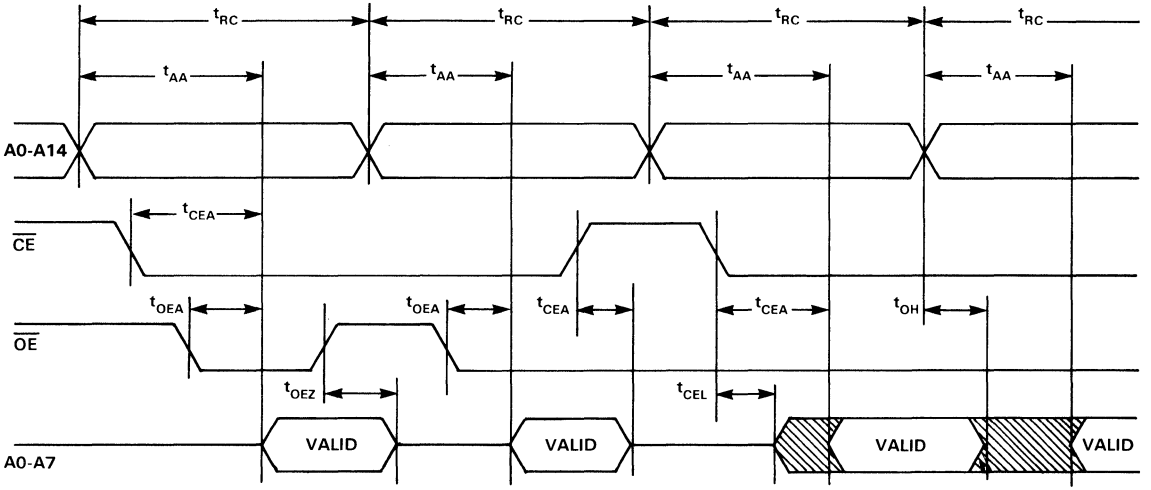
($-55°C \leq T_C \leq 125°C$)

SYM	PARAMETER	TYP	MAX	UNITS	NOTES
C_I	Input Capacitance	5*		pF	
C_O	Output Capacitance	7*		pF	5

*Sample tested only and guaranteed by design

TIMING DIAGRAM

Figure 3

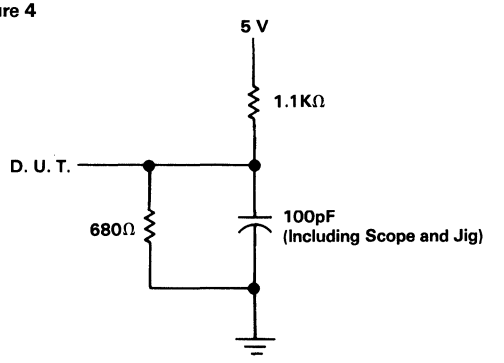


NOTES:

1. All voltages referenced to GND.
2. Measured with $0.4\ V \leq V_O \leq 5.0\ V$ outputs deselected and $V_{CC} = 5\ V$.
3. $V_{IN} = 0\ V$ to $5.25\ V$.
4. Input and output timing reference levels are at 1.5 V for inputs and .8 and 2.0 for outputs.
5. Measured with outputs open.
6. A minimum of 2 ms time delay is required after the application of V_{CC} (+5) before proper device operation is achieved. $\overline{CE}$ must be at V_{IH} for this time period.
7. $\overline{CE}$ high.
8. Negative undershoots to a minimum of −1.5 V are allowed with a maximum of 10 ns pulse width once per cycle.
9. Measured with a load as shown in Figure 1.
10. A.C. measurements assume transition time = 5 ns levels GND to 3 V.

OUTPUT LOAD

Figure 4



XII

DESCRIPTION (continued)

As a member of the Mostek BYTEWYDE Memory Family, the MKB38000 allows compatibility between RAM, ROM, and EPROM. The MKB38000 can be used as a pin/function density upgrade to the MKB37000 8K x 8 bit ROM.

The output enable function controls only the outputs. The $\overline{CE}$ input can be used for device selection and the $\overline{OE}$ input used to avoid bus conflicts so that outputs can be 'OR'ed together when using multiplexed or bi-directional busses.

Other system oriented features include fully TTL compatible inputs and outputs. The three state outputs, controlled by the $\overline{OE}$ input, will drive a minimum of 2 standard TTL loads. The MKB38000 operates from a single +5 volt power supply. It is packaged in the industry standard 28 pin DIP. Pin 27 is not connected in order to maintain compatiblity with RAMs which use this pin as a write enable ($\overline{WE}$) control function.

Any application requiring a high performance high bit density ROM can be satisfied by the MKB38000. This device is ideally suited for 8 bit microprocessor systems such as those which can utilize the MKB3880. It can offer significant cost advantages over PROM.

OPERATION

The MKB38000 is controlled by the chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) inputs. A low level at the $\overline{CE}$ input powers up the memory for an active cycle. The output buffers, under the control of $\overline{OE}$, will become active in $\overline{CE}$ access time (t_{CEA}) if the output enable access time (t_{OEA}) requirement is met.

By maintaining valid address, the outputs will remain valid and active until either $\overline{CE}$ or $\overline{OE}$ is returned to the high state or until an address is changed. After chip deselect time (t_{CEZ}) or output enable deselect time (t_{OEZ}), the output buffers will go to a high impedance state.

MKB38000 ROM CODE DATA INPUT PROCEDURE

The preferred method of supplying code data to Mostek is in the form of programmed EPROMs (see table). In addition to the programmed set, Mostek requires an additional set of blank EPROMs for supplying customer code verification. When multiple EPROMs are required to describe the ROM, they shall be designated in ascending address space with the numbers 1, 2, 3, etc. As an example, EPROM #1 would start with address space 0000 and go to 1FFF for an 8K x 8 device. EPROM #2 would then start at address space 2000 and so on. A total of four 8K x 8 devices would be required to totally describe the address space of the 32K x 8 MKB38000.

A paper printout and verification approval letter will accompany each verification EPROM set returned to the customer. Approval is considered to be accepted when the signed verification letter is returned to Mostek. The original set of EPROMs will be retained by Mostek for the duration of the prototyping process.

ACCEPTABLE EPROMs FOR CODE DATA

Table 1

EPROM	# REQUIRED
2732	8
2764	4

SUPPLEMENT

MOSTEK®

4096 x 1-BIT DYNAMIC RAM

Processed to MIL-STD-883, Method 5004, Class B

MKB4027(J)-83/84

FEATURES

- Extended operating temperature range ($-55°C \leq T_A \leq +85°C$)
- Industry standard 16-pin DIP (MK4096) configuration
- 200ns access time, 375ns cycle (-83)
  250ns access time, 375ns cycle (-84)
- ± 10% tolerance on all supplies (+12V, ± 5V)
- Low Power: 467mW active (max)
  40mW standby (max)
- Improved performance with "gated $\overline{CAS}$," "$\overline{RAS}$ only" refresh and page mode capability
- All inputs are low capacitance and TTL compatible
- Input latches for addresses, chip select and data in
- Three-state TTL compatible output
- Output data latched and valid into next cycle
- Ruggedized for use in severe military environments

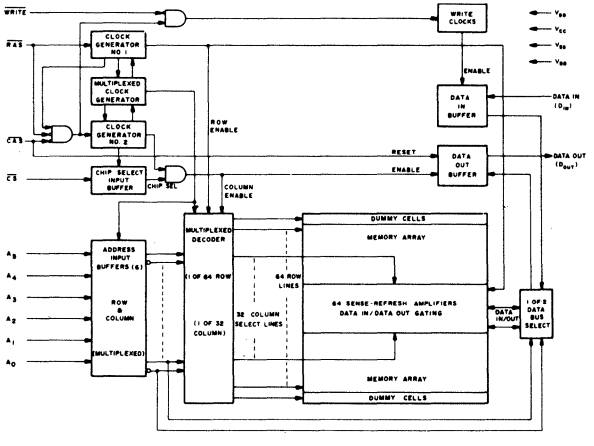
DESCRIPTION

The MKB4027 is a 4096 word by 1 bit MOS random access memory circuit fabricated with Mostek's N-channel silicon gate process. This process allows the MKB4027 to be a high performance state-of-the-art memory circuit that is manufacturable in high volume. The MKB4027 employs a single transistor storage cell utilizing a dynamic storage technique and dynamic control circuitry to achieve optimum performance with low power dissipation.

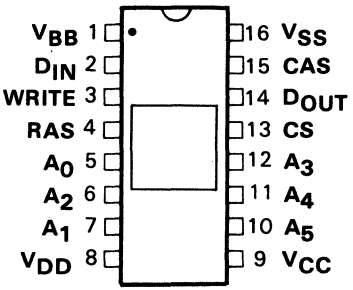
A unique multiplexing and latching technique for the address inputs permits the MKB4027 to be packaged in a standard 16-pin DIP on 0.3 in. centers. This package size provides high system-bit densities and is compatible with widely available automated testing and insertion equipment.

System oriented features include direct interfacing capability with TTL, only 6 very low capacitance address lines to drive, on-chip address and data registers which eliminates the need for interface registers, input logic levels selected to optimize noise immunity, and two chip select methods to allow the user to determine the appropriate speed/power characteristics of his memory system. The MKB4027 also incorporates several flexible operating modes. In addition to the usual read and write cycles, read-modify write, page-mode, and $\overline{RAS}$ only refresh cycles are available with the MKB4027. Page-mode timing is very useful in systems requiring Direct Memory Access (DMA) operation.

FUNCTIONAL DIAGRAM



PIN CONNECTIONS



PIN NAMES

A_0 - A_6	Address Inputs	WRITE	Read/Write Input
CS	Col Address Strobe	V_{BB}	Power (-5V)
D_{IN}	Data In	V_{CC}	Power (+5V)
D_{OUT}	Data Out	V_{DD}	Power (+12V)
RAS	Row Address Strobe	V_{SS}	Ground

XII

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to V_{BB} ..... -0.5V to +20V
Voltage on V_{DD}, V_{CC} relative to V_{SS} ..... -1.0V to +15V
V_{BB} - V_{SS} (V_{DD} - V_{SS} > 0) 0V
Operating Temperature (Ambient)(Ceramic) ..... -55°C to +85°C
Storage Temperature (Ambient)(Ceramic) ..... -65°C to +150°C
Short Circuit Output Current 50mA
Power Dissipation ..... 1 Watt

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS[4]

(-55°C ≤ T_A ≤ 85°C)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{DD}	Supply Voltage	10.8	12.0	13.2	V	2
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2,3
V_{SS}	Ground	0	0	0	V	2
V_{BB}	Supply Voltage	-4.5	-5.0	-5.5	V	2
V_{IHC}	Logic 1 Voltage, $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	2.7		7.0	V	2
V_{IH}	Logic 1 Voltage, all inputs except $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	2.4		7.0	V	2
V_{IL}	Logic 0 Voltage, all inputs	-1.0		.8	V	2

DC ELECTRICAL CHARACTERISTICS[4]

(-55°C ≤ T_A ≤ 85°C)[1] (V_{DD} = 12.0V ± 10%; V_{CC} = 5.0V ± 10%; V_{SS} = 0V; V_{BB} = -5.0V ± 10%)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
I_{DD1}	Avg. V_{DD} Power Supply Current			35	mA	5
I_{DD2}	Standby V_{DD} Power Supply Current			3.0	mA	8
I_{DD3}	Avg. V_{DD} Power Supply Current during "$\overline{RAS}$ only" cycles			27	mA	
I_{CC}	V_{CC} Power Supply Current				mA	6
I_{BB}	Avg. V_{BB} Power Supply Current			200	μA	
$I_{I(L)}$	Input Leakage Current (any input)			10	μA	7
$I_{O(L)}$	Output Leakage Current			10	μA	8,9
V_{OH}	Output Logic 1 Voltage @ I_{OUT} = -5mA	2.4			V	
V_{OL}	Output Logic 0 Voltage @ I_{OUT} = 3.2mA			0.4	V	

NOTES:

1. T_A is specified for operation at frequencies to $t_{RC} \geq t_{RC}$ (min). Operation at higher cycle rates with reduced ambient temperatures and higher power dissipation is permissible provided that all AC parameters are met.
2. All voltages referenced to V_{SS}.
3. Output voltage will swing from V_{SS} to V_{CC} when enabled, with no output load. For purposes of maintaining data in standby mode, V_{CC} may be reduced to V_{SS} without affecting refresh operations or data retention. However, the V_{OH} (min) specification is not guaranteed in this mode.
4. Several cycles are required after power-up before proper device operation is achieved. Any 8 cycles which perform refresh are adequate for this purpose.
5. Current is proportional to cycle rate. I_{DD1} (max) is measured at the cycle rate specified by t_{RC} (min). See Figure 1 for I_{DD1} limits at other cycle rates.
6. I_{CC} depends on output loading. During readout of high level data V_{CC} is connected through a low impedance (135Ω typ) to Data Out. At all other times I_{CC} consists of leakage currents only.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (4,11,7)
$(-55°C \leq T_A \leq 85°C)^1$ (V_{DD} = 12.0V ± 10%, V_{CC} = 0V, V_{BB} = -5.0V ± 10%)

		MKB4027-83		MKB4027-84			
SYM	PARAMETER	MIN	MAX	MIN	MAX	UNITS	NOTES
t_{RC}	Random read or write cycle time	375		380		ns	12
t_{RWC}	Read-write cycle time	375		395		ns	12
t_{RMW}	Read Modify Write Cycle	405		470		ns	12
t_{PC}	Page mode cycle time	225		285		ns	12
t_{RAC}	Access time from row address strobe		200		250	ns	13,15
t_{CAC}	Access time from column address strobe		135		165	ns	14,15
t_{OFF}	Output buffer turn-off delay		50		60	ns	
t_{RP}	Row address strobe precharge time	120		120		ns	
t_{RAS}	Row address and strobe pulse width	200	5000	250	5000	ns	
t_{RSH}	Row address strobe hold time	135		165		ns	
t_{CAS}	Column address strobe pulse width	135		165		ns	
t_{CSH}	$\overline{CAS}$ hold time	200		250		ns	
t_{RCD}	Row to column strobe delay	25	65	35	85	ns	16
t_{ASR}	Row address set-up time	0		0		ns	
t_{RAH}	Row address hold time	25		35		ns	
t_{ASC}	Column address set-up time	0		0		ns	
t_{CAH}	Column address hold-time	55		75		ns	
t_{AR}	Column address hold time referenced to $\overline{RAS}$	120		160		ns	
t_{CSC}	Chip select set-up time	0		0		ns	
t_{CH}	Chip select hold time	55		75		ns	
t_{CHR}	Chip select hold time referenced to $\overline{RAS}$	120		160		ns	
t_T	Transition time (rise and fall)	3	50	3	50	ns	17
t_{RCS}	Read command set-up time	0		0		ns	
t_{RCH}	Read command hold time	0		0		ns	
t_{WCH}	Write command hold time	55		75		ns	
t_{WCR}	Write command hold time referenced to $\overline{RAS}$	120		160		ns	
t_{WP}	Write command pulse width	55		75		ns	
t_{RWL}	Write command to row strobe lead time	70		85		ns	
t_{CWL}	Write command to column strobe lead time	70		85		ns	
t_{DS}	Data in set-up time	0		0		ns	18

SYM	PARAMETER	MKB4027-83		MKB4027-84		UNITS	NOTES
		MIN	MAX	MIN	MAX		
t_{DH}	Data in hold time	55		75		ns	18
t_{DHR}	Data in hold time referenced to $\overline{RAS}$	120		160		ns	
t_{CRP}	Column to row strobe precharge time	0		0		ns	
t_{CP}	Column precharge time	80		110		ns	
t_{RFSH}	Refresh Period		2		2	ms	
t_{WCS}	Write command set-up time	0		0			19
t_{CWD}	$\overline{CAS}$ to WRITE delay	80		80		ns	19
t_{RWD}	$\overline{RAS}$ to WRITE delay	145		175		ns	19
t_{DOH}	Data out hold time	5		5		μs	

NOTES (Continued)

7. All device pins at 0 volts except V_{BB} which is at -5 volts and the pin under test which is at -10 volts.
8. Output logic is disabled (high-impedance) and $\overline{RAS}$ and $\overline{CAS}$ are both at a logic 1. Transient stabilization is required prior to measurement of this parameter.
9. $0V \leq V_{OUT} \leq -10V$
10. Effective capacitance is calculated from the equation: $C = \frac{\Delta Q}{V}$ with $\Delta V = 3$ Volts
11. AC measurements assume $t_T = 5ns$.
12. The specification for t_{RC} (min) and t_{RWC} (min) are used only to indicate cycle time at which proper operation over the full temperature range ($-55°C \leq T_A \leq 85°C$) is assured. See Figure 2 for derating curve.
13. Assumes that $t_{RCD} \leq t_{RCD}$ (max)
14. Assumes that $t_{RCD} \geq t_{RCD}$ (max)
15. Measured with a load circuit equivalent to 2 TTL loads and 100pF.
16. Operation within the t_{RAC} (max) limit insures that t_{RCD} (max) is specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
17. V_{IHC} (min) or V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IHC} or V_{IH} and V_{IL}.
18. These parameters are referenced to CAS leading edge in random write cycles to WRITE leading edge in delayed write or read-modify-write cycles.
19. t_{WCS}, t_{CWD}, and t_{RWD} are restrictive operating parameters in a read/write or read/modify/write cycle only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the Data Out will contain the data written into the selected cell. If $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min), the cycle is a read-write cycle and Data Out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of Data Out (at access time) is indetermined.

AC ELECTRICAL CHARACTERISTICS

($-55°C \leq T_A \leq 85°C$)[1] ($V_{DD} = 12.0V \pm 10\%$, $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$, $V_{BB} = -5.0V \pm 10\%$)

SYM	PARAMETER	TYP	MAX	UNITS	NOTES
C_{I1}	Input Capacitance (A_0 - A_5), D_{IN}, $\overline{CS}$	4	5	pF	10
C_{I2}	Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	8	10	pF	10
C_O	Output Capacitance (D_{OUT})	5	7	pF	8,10

SUPPLEMENTAL DATA SHEET TO BE USED IN CONJUNCTION WITH MOSTEK MK4027(J)-1/2/3 and MK4027(J)-4 DATA SHEETS

MOSTEK®

4096 x 1-BIT STATIC RAM

Processed to MIL-STD-883, Method 5004, Class B

MKB4104 (P/J/E)-84/85

FEATURES

- ☐ Extended operating temperature range ($-55°C \leq T_A \leq 125°C$)
- ☐ Combination static storage cells and dynamic control circuitry for truly high performance

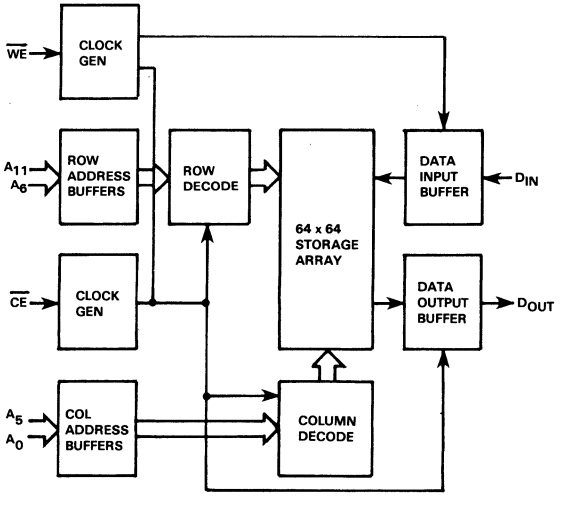
Part Number	Access Time	Cycle Time
4104(J)-84	250ns	385ns
4104(J)-85	300ns	510ns

- ☐ Average power dissipation less than 150mW
- ☐ Standby power dissipation less than 53mW
- ☐ Single +5V power supply (5% tolerance)
- ☐ Fully TTL compatible
  Fanout: 2 - Standard TTL
  2 - Schottky TTL
  12 - Low Power Schottky TTL
- ☐ Standard 18 pin DIP
- ☐ Leadless chip carrier (E package) available for high density applications
- ☐ Ruggedized for use in severe military environments

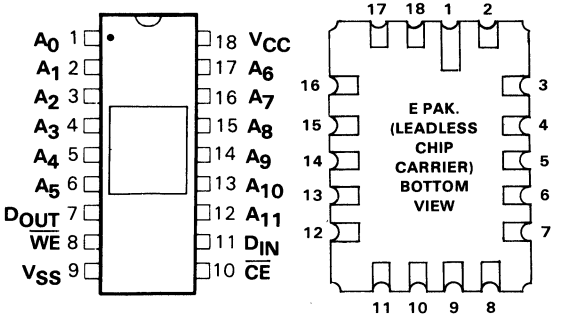
DESCRIPTION

The Mostek MKB4104 is a high performance static random access memory organized as 4096 one bit words. The MKB4104 combines the best characteristics of static and dynamic memory techniques to achieve a TTL compatible, 5 volt only, high performance, low power memory device. It utilizes advanced circuit design concepts and an innovative state-of-the-art N-channel silicon gate process specially tailored to provide static data storage with the performance (speed and power) of dynamic RAMs. Since the storage cell is static the device may be stopped indefinitely with the $\overline{CE}$ clock in the off (Logic 1) state.

FUNCTIONAL DESCRIPTION



PIN CONNECTIONS



PIN NAMES

A0-A11	Address Inputs	V_{SS}	Ground
$\overline{CE}$	Chip Enable	V_{CC}	Power (+5V)
D_{IN}	Data Input	$\overline{WE}$	Write Enable
D_{OUT}	Data Output		

XII

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to V_{SS} ..... -1.0V to +7.0V
Operating Temperature T_A (Ambient) ..... -55°C to +125°C
Storage Temperature (Ambient)(Ceramic) ..... -65°C to +150°C
Power Dissipation ..... 1 Watt
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS[6]

($-55°C \leq T_A \leq +125°C$)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.75	5.0	5.25	V	1
V_{SS}	Supply Voltage	0	0	0	V	1
V_{IH}	Logic "1" Voltage All Inputs	2.4		7.0	V	1
V_{IL}	Logic "0" Voltage All Inputs	-1.0		.65	V	1

DC ELECTRICAL CHARACTERISTICS

($-55°C \leq T_A \leq +125°C$) ($V_{CC}$ = 5.0 volts ± 5%)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC1}	Average V_{CC} Power Supply Current		27	mA	2
I_{CC2}	Standby V_{CC} Power Supply Current		10	mA	3
I_{IL}	Input Leakage Current (Any Input)	-10	10	μA	4
I_{OL}	Output Leakage Current	-10	10	μA	3,5
V_{OH}	Output Logic "1" Voltage I_{OUT} = -500μA	2.4		V	11
V_{OL}	Output Logic "-" Voltage I_{OUT} = 5mA		0.4	V	11

AC ELECTRICAL CHARACTERISTICS

($-55°C \leq T_A \leq +125°C$) ($V_{CC}$ = +5.0 volts ± 5%)

SYM	PARAMETER	MIN	TYP	MAX	NOTES
C_I	Input Capacitance		4pF	6pF	14
C_O	Output Capacitance		7pF	7pF	14

NOTES:

1. All voltages referenced to V_{SS}.
2. I_{CC1} is related to precharge and cycle times. Guaranteed maximum values for I_{CC1} are at minimum cycle time.
3. Output is disabled (open circuit), $\overline{CE}$ is at logic 1.
4. All device pins at 0 volts except pin under test at $0 \leq V_{IN} \leq 5.5V$ (V_{CC} 5V)
5. $0V \leq V_{OUT} \leq +5.5V$ (V_{CC} 5V)
6. During power up, $\overline{CE}$ and $\overline{WE}$ must be at V_{IH} for minimum of 2ms after V_{CC} reaches 4.75V, before a valid memory cycle can be accomplished.
7. Measured with load circuit equivalent to 2 TTL loads and CL 100pF.
8. If $\overline{WE}$ follows after $\overline{CE}$ by more than t_{WS}, then data out may not remain open circuited.
9. Determined by user. Total cycle time cannot exceed t_{CF} max.
10. Data-in set-up time is referenced to the later of the two failing clock edges $\overline{CE}$ or $\overline{WE}$.
11. AC measurements assume t_t 5ns. Timing points are taken at .8V and 2.0V on inputs and .8V and 2.0V on the output. Transition times are also taken between these levels.
12. t_C t_{CL} + t_P + $2t_t$.
13. The true level of the output in the open circuit condition will be determined totally by output load conditions. The output is guaranteed to be open circuit within t_{OFF}.
14. Effective capacitance calculated from the equation $C \frac{\Delta t}{\Delta V}$ with ΔV equal to 3V and V_{CC} nominal.
15. For RMW, t_{CE} t_{AC} + t_{WPL} + $5t_{MOD}$
16. t_C t_{AC} + t_{WPL} + t_P + $3t_t$ + t_{MOD}.

AC ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS[6,11]

($-55°C \leq T_A \leq +125°C$) ($V_{CC}$ = +5.0 Volts ± 5%)

SYM	PARAMETER	MKB4104-84		MKB4104-85		UNITS	NOTES
		MIN	MAX	MIN	MAX		
t_C	Read or Write Cycle Time		410	510		ns	12
t_{AC}	Random Access		250		300	ns	7
t_{CE}	Chip Enable Pulse Width	250	5000	300	5000	ns	15
t_P	Chip Enable Precharge Time	150		200		ns	
t_{AH}	Address Hold Time	135		165		ns	
t_{AS}	Address Set-Up Time	0		0		ns	
t_{OFF}	Output Buffer Turn-Off Delay	0	65	0	75	ns	13
t_{WS}	Write Enable Set-Up Time	0		0		ns	8
t_{DHC}	Data Input Hold Time Referenced to CE	210		250		ns	
t_{DHW}	Data Input Hold Time Referenced to WE	90		105			
t_{WW}	Write Enabled Pulse Width	60		90		ns	
t_{MOD}	Modify Time	0	5000	0	5000	ns	9
t_{WPL}	WE to CE Precharge Lead Time	85		105		ns	10
t_{DS}	Data Input Set-Up Time	0		0		ns	
t_{WH}	Write Enable Hold Time	185		225		ns	
t_T	Transition Time	5	50	5	50	ns	
t_{RMW}	Read-Modify-Write Cycle Time	500		620		ns	16
t_{RS}	Read Set-Up Time	0		0		ns	

DESCRIPTION (Continued)

All input levels, including write enable ($\overline{WE}$) and chip enable ($\overline{CE}$) are TTL with a one level of 2.4 volts and a zero level of .65 volts. The push-pull output (no pull-up resistor required) delivers a one level of 2.4V minimum and a zero level of .4 volts maximum. The output has a fanout of 2 standard TTL loads or 12 low power Schottky loads.

The RAM employs an innovative static cell which occupies a mere 2.75 square mils (½ the area of previous cells) and dissipates power levels comparable to CMOS. The static cell eliminates the need for refresh cycles and associated hardware thus allowing easy system implementation.

Power supply requirement of +5V combined with TTL compatibility on all I/O pins permits easy integration into large memory configurations. The single supply reduces capacitor count and permits denser packaging on printed circuit boards. The 5V only supply requirement and TTL compatible I/O makes this part an ideal choice for next generation +5V only microprocessors such as Mostek's Z80. The early write mode ($\overline{WE}$ active prior to $\overline{CE}$) permits common I/O operation, needed for Z80 interfacing, without external circuitry.

Reliability is greatly enhanced by the low power dissipation which causes a maximum junction rise of only 6.6° at 1.6 Megahertz operation. The MKB4104 was designed for the system designer and user who require the highest performance available along with Mostek's proven reliability.

SUPPLEMENTAL DATA SHEET TO BE USED IN CONJUNCTION WITH MOSTEK MK4104(P/N) DATA SHEET

MOSTEK®

16,384 x 1-BIT DYNAMIC RAM

Processed to MIL-STD-883, Method 5004, Class B

MKB4116(P/J)-82/83/84

MKB4116(E/F)-83/84

FEATURES

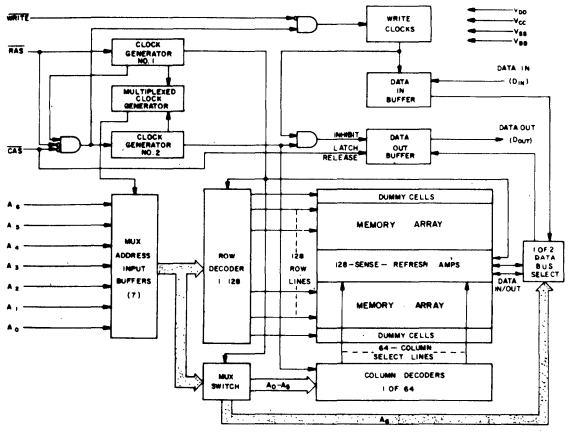
- ☐ Extended operating temperature range (−55°C ≤ T_C ≤ +110°C)
- ☐ Recognized industry standard 16-pin configuration from Mostek
- ☐ 150ns access time, 320ns cycle (MKB4116-82)
  200ns access time, 375ns cycle (MKB4116-83)
  250ns access time, 410ns cycle (MKB4116-84)
- ☐ ± 10% tolerance on all power supplies (+12V, ± 5V)
- ☐ Low power: 462mW active, 30mW standby (max)
- ☐ Output data controlled by CAS and unlatched at end of cycle to allow two dimensional chip selection and extended page boundary
- ☐ Common I/O capability using "early write" operation
- ☐ Read-Modify-Write, RAS-only refresh, and Page-mode capability
- ☐ All inputs TTL compatible, low capacitance, and protected against static charge
- ☐ 128 refresh cycles (2msec refresh interval)
- ☐ Leadless chip carrier (E) and flat pack (F) available for high density applications, -83/84
- ☐ Ruggedized for use in severe military environments

DESCRIPTION

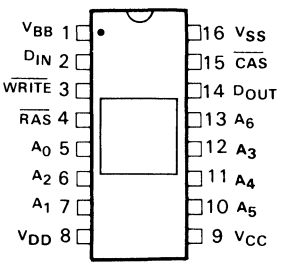
The MKB4116 is a new generation MOS dynamic random access memory circuit organized as 16,384 words by 1 bit. As a state-of-the-art MOS memory device, the MKB4116 (16K RAM) incorporates advanced circuit techniques designed to provide wide operating margins, both internally and to the system user, while achieving performance levels in speed and power previously seen only in Mostek's high performance MK4027 (4K RAM).

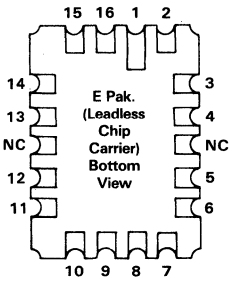
The technology used to fabricate the MKB4116 is Mostek's double-poly, N-channel silicon gate, POLY I™ process. This process, coupled with the use of a single transistor dynamic storage cell, provides the maximal circuit density and reliability, while maintaining high performance capability. The use of dynamic circuitry throughout, including sense amplifiers, assures that power dissipation is minimized without any sacrifice in speed or operating margin. These factors combine to make the MKB4116 a truly superior RAM product.

BLOCK DIAGRAM



PIN CONNECTIONS





PIN NAMES

A0 - A6	Address Inputs	WRITE	Read/Write Input
CAS	Col. Address Strobe	V_{BB}	Power (-5V)
D_{IN}	Data In	V_{CC}	Power (+5V)
D_{OUT}	Data Out	V_{DD}	Power (+12V)
RAS	Row Address Strobe	V_{SS}	Ground

XII

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to V_{BB} ..... -0.5V to +20V
Voltage on V_{DD}, V_{CC} supplies relative to V_{SS} ..... -1.0V to +15.0V
V_{BB} - V_{SS} (V_{DD} - V_{SS} > 0V) 0V
Operating Temperature, T_C (Case) ..... -55°C to +110°C
Storage Temperature (Ambient) ..... -65°C to +150°C
Short Circuit Output Current 50mA
Power Dissipation ..... 1 Watt

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS[6]

(-55°C ≤ T_C ≤ +110°C)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{DD}	Supply Voltage	10.8	12.0	13.2	Volts	2
V_{CC}	Supply Voltage	4.5	5.0	5.5	Volts	2,3
V_{SS}	Supply Voltage	0	0	0	Volts	2
V_{BB}	Supply Voltage	-4.5	-5.0	-5.5	Volts	2
V_{IHC}	Input High (Logic 1) Voltage, $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	2.7	—	7.0	Volts	2
V_{IH}	Input High (Logic 1) Voltage, all inputs except $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	2.4	—	7.0	Volts	2
V_{IL}	Input Low (Logic 0) Voltage, all inputs	-1.0	—	.8	Volts	2

DC ELECTRICAL CHARACTERISITCS

(-55°C ≤ T_C ≤ +110°C) (V_{DD} = 5.0V ± 10%; -5.5V ≤ V_{BB} ≤ -4.5V; V_{SS} = 0V)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
I_{DD1} I_{CC1} I_{BB1}	OPERATING CURRENT Average power supply operating current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = t_{RC} (min)		35 400	mA µA	4 5
I_{DD2} I_{CC2} I_{BB2}	STANDBY CURRENT Power supply standby current ($\overline{RAS}$ = V_{IHC}, D_{OUT} = High Impedance)	-10	2.25 10 200	mA µA µA	
I_{DD3} I_{CC3} I_{BB3}	REFRESH CURRENT Average power supply current, refesh mode ($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IHC}; t_{RC} = t_{RC} min)	-10	27 10 400	mA µA µA	4
I_{DD4} I_{CC4} I_{BB4}	PAGE MODE CURRENT Average power supply current, page-mode operation ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling; t_{PC} = t_{PC} min)		27 400	mA µA	4 5
$I_{I(L)}$	INPUT LEAKAGE Input leakage, any input (V_{BB} = -5V, 0V ≤ V_{IN} ≤ +7.0V, all other pins not under test = 0 volts)	-10	10	µA	
$I_{O(L)}$	OUTPUT LEAKAGE Output leakage current (D_{OUT} is disabled, 0V ≤ V_{OUT} ≤ +5.5V)	-10	10	µA	
V_{OH} V_{OL}	OUTPUT LEVELS Output high (Logic 1) voltage (I_{OUT} = -5mA) Output low (Logic 0) voltage (I_{OUT} = 4.2mA)	2.4	 0.4	Volts Volts	3

NOTES

1. T_C is specified here for operation at frequencies to $t_{RC} \geq t_{RC}$ (min). Operation at higher cycle rates with reduced ambient temperatures and higher power dissipation is permissible, however, provided AC operating parameters are met.
2. All voltages referenced to V_{SS}.
3. Output voltage will swing from V_{SS} to V_{CC} when activated with no current loading. For purposes of maintaing data in standby mode, V_{CC} may be reduced to V_{SS} without affecting refresh operations or data retention. However, the V_{OH} (min) specifications is not guaranteed in this mode.
4. I_{DD1}, I_{DD3}, and I_{DD4} depend on cycle rate. See Figures 2, 3 and 4 for I_{DD} limits at other cycle rates.
5. I_{CC1} and I_{CC4} depend upon output loading. During readout of high level data V_{CC} is connected through a low impedance (135 Ω typ) to data out. At all other times I_{CC} consists of leakage currents only.
6. Several cycles are required after power-up before proper device operation is achieved. Any 8 cycles which perform refresh are adequate for this purpose.
7. AC measurements assume t1 5ns.
8. V_{IHC}(min) or V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IHC} or V_{IH} or V_{IL}.
9. The specifications for t_{RC} (min) t_{RMW} (min) are used only to indicate cycle which proper operation over the full temperature range (-55°C ≤ T_C ≤ 110°C) is assured.
10. Assumes that $t_{RCD} \leq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RCD} will increase by the amount that t_{RCD} exceeds the value shown.
11. Assumes that $t_{RCD} \geq t_{RCD}$ (max)
12. Measured with a load equivalent to 2 TTL loads and 100pF.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (6,7,8)

(-55°C ≤ T_C ≤ 110°C)[1] (V_{DD} = 12.0V ± 10%; V_{CC} = 5.0V ± 10%, V_{SS} = 0V, -5.5V ≤ V_{BB} ≤ -4.5V)

		MKB4116-82		MKB4116-83		MKB4116-84			
SYM	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
t_{RC}	Random read or write cycle time	320		375		410		ns	9
t_{RWC}	Read-write cycle time	320		375		425		ns	9
t_{RMW}	Read-modify-write cycle time	320		405		500		ns	9
t_{PC}	Page mode cycle time	170		225		275		ns	9
t_{RAC}	Access time from $\overline{RAS}$		150		200		250	ns	10,12
t_{CAC}	Access time from $\overline{CAS}$		100		135		165	ns	11,12
t_{OFF}	Output buffer turn-off delay	0	40	0	50	0	60	ns	13
t_T	Transition time (rise and fall)	3	35	3	50	3	50	ns	8
t_{RP}	RAS precharge time	100		120		150		ns	
t_{RAS}	$\overline{RAS}$ pulse width	150	5000	200	5000	250	5000	ns	
t_{RSH}	$\overline{RAS}$ hold time	100		135		165		ns	
t_{CSH}	$\overline{CAS}$ hold time	150		200		250		ns	
t_{CAS}	$\overline{CAS}$ pulse width	100	5000	135	5000	165	5000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ delay time	20	50	25	65	35	85	ns	15
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ precharge time	0		0		0		ns	
t_{ASR}	Row Address set-up time	0		0		0		ns	
t_{RAH}	Row Address hold time	20		25		35		ns	
t_{ASC}	Column Address set-up time	0		0		0		ns	
t_{CAH}	Column Address hold time	45		55		75		ns	
t_{AR}	Column Address hold time referenced to $\overline{RAS}$	95		120		160		ns	
t_{RCS}	Read command set-up time	0		0		0		ns	
t_{RCH}	Read command hold time	0		0		0		ns	
t_{WCH}	Write command hold time	45		55		75		ns	
t_{WCR}	Write command hold time referenced to $\overline{RAS}$	95		120		160		ns	
t_{WP}	Write command pulse width	45		55		75		ns	

XII

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS [6,7,8]

($-55°C \leq T_C \leq +110°C$)[1] ($V_{DD}$ = 12.0V ± 10%; V_{CC} = 5.0V ± 10%, V_{SS} = 0V, $-5.5V \leq V_{BB} \leq -4.5V$)

		MKB4116-82		MKB4116-83		MKB4116-84			
SYM	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
t_{RWL}	Write command to $\overline{RAS}$ lead time	50		70		85		ns	
t_{CWL}	Write command to $\overline{CAS}$ lead time	50		70		85		ns	
t_{DS}	Data-in set-up time	0		0		0		ns	15
t_{DH}	Date-in hold time	45		55		75		ns	15
t_{DHR}	Data-in hold time referenced to $\overline{RAS}$	95		120		160		ns	
t_{CP}	$\overline{CAS}$ precharge time (for page-mode cycle only)	60		80		100		ns	
t_{REF}	Refresh period		2		2		2	ms	19
t_{WCS}	$\overline{WRITE}$ command set-up time	0		0		0		ns	16
t_{CWD}	$\overline{CAS}$ to $\overline{WRITE}$ delay	60		80		90		ns	16
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ delay	110		145		175		ns	16

AC ELECTRICAL CHARACTERISTICS

($-55°C \leq T_C \leq +110°C$) ($V_{DD}$ = 12.0V ± 10%; V_{SS} = 0V; $-5.5V \leq V_{BB} \leq -4.5V$)

SYM	PARAMETER	TYP	MAX	UNITS	NOTES
C_{I1}	Input Capacitance (A_0 - A_6), D_{IN}	4	5	pF	17
C_{I2}	Input Capacitance, $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	8	10	pF	17
C_O	Output Capacitance (D_{OUT})	5	7	pF	17,18

NOTES: Continued

13. t_{OPI} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
14. Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met t_{RCD} (max) is specified as a reference point only, if t_{RCP} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
15. These parameters are referenced to CAS leading edge in early write cycles and to WRITE leading edge in delayed write or read-modify-write cycles.
16. t_{WCS}, t_{CWD}, and t_{RWD} are restrictive operating parameters in read-write and read-modify-write cycles only. If $t_{WCS} \leq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle. If $t_{CWD} \leq t_{CWD}$ (min) and $t_{RWD} \leq t_{RWD}$ (min), the cycle is a read-write cycle and the data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.
17. Effective capacitance calculated from the equation $C = \frac{I\Delta t}{\Delta V}$ with ΔV = 3 volts and power supplies at nominal levels.
18. CAS = V_{IHC} to disable D_{OUT}.

DESCRIPTION (Continued)

Multiplexed address inputs (a feature pioneered by Mostek for its 4K RAMs) permits the MKB4116 to be packaged in a standard 16-pin DIP. This recognized industry standard package configuration, while compatible with widely available automated testing and insertion equipment, provides highest possible system bit densities and simplifies system upgrade from 4K to 16K RAMs for new generation applications. Non-critical clock timing requirements allow use of the multiplexing technique while maintaining high perfomance.

SUPPLEMENTAL DATA SHEET TO BE USED IN CONJUNCTION WITH MOSTEK MK4116-2/3 AND MK4116-4 DATA SHEETS

MOSTEK®

MILITARY HIGH-REL PRODUCTS

Processed to MIL-STD-883, Method 5004, Class B

1K x 8-Bit Static RAM

MKB4118A(P/J/E)-82/83/84

FEATURES

- ☐ Tested per MIL-STD-883B method 5004 and qualified per method 5005.
- ☐ Static operation, single +5 V power supply
- ☐ Military temperature range ($-55°C \leq T_A \leq +125°C$)
- ☐ Organization: 1K x 8 bit RAM JEDEC pinout
- ☐ Pin compatible with Mostek's BYTEWYDE™ memory family
- ☐ 24/28 pin ROM/PROM compatible pin configuration

Part No.	Access Time	R/W cycle Time
MKB4118A-82	150 nsec	150 nsec
MKB4118A-83	200 nsec	200 nsec
MKB4118A-84	250 nsec	250 nsec

- ☐ $\overline{CE}$ and $\overline{OE}$ functions facilitate bus control
- ☐ Industrial MK[illegible]sion available (–40°C/85°C)

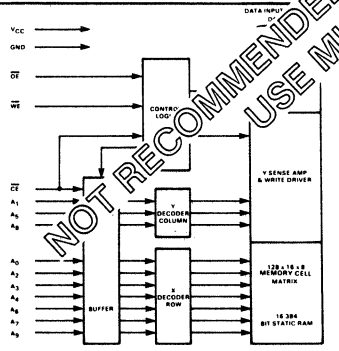
DESCRIPTION

The MKB4118A uses Mostek's advanced circuit design techniques to package 8,192 bits of static RAM on a single chip. Static operation is achieved with high performance and lower power dissipation by utilizing Address[illegible]Activated™ circuit design techniques.

The MK[illegible]18A excels in high speed memory applications wh[illegible]e organization requires relatively shallow depth [illegible] wide word format. The MKB4118A presents to the [illegible]s high density cost effective N-MOS memory with the [illegible]iance characteristics necessary for today's micro-[illegible]essor applications.

BLOCK DIAGRAM

Figure 1



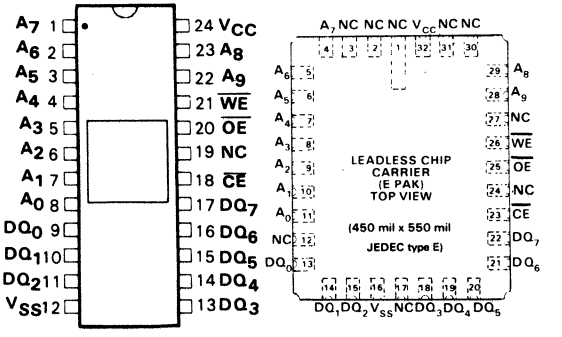
TRUTH TABLE

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	DQ
V_{IH}	X	X	Deselect	High Z
V_{IL}	X	V_{IL}	Write	D_{IN}
V_{IL}	V_{IL}	V_{IH}	Read	D_{OUT}
V_{IL}	V_{IH}	V_{IH}	Read	High Z

X = Don't Care

PIN CONNECTIONS

Figure 2



PIN NAMES

A_0 - A_9	Address Inputs	$\overline{WE}$	Write Enable
$\overline{CE}$	Chip Enable	$\overline{OE}$	Output Enable
V_{SS}	Ground	NC	No Connection
V_{CC}	Power (+5 V)	DQ_0 - DQ_7	Data In/Data Out

XII

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to V_{SS} ..... -.5 V to +7.0 V
Operating Temperature T_A (Ambient) ..... -55°C to +125°C
Storage Temperature (Ambient) ..... -65°C to +150°C
Power Dissipation ..... 1 Watt
Output Current ..... 20 mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated int he operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS[7]

(-55°C ≤ T_A ≤ +125°C)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.75	5.0	5.25	V	1
V_{SS}	Supply Voltage	0	0	0	V	1
V_{IH}	Logic "1" Voltage All Inputs	2.4		7.0	V	1
V_{IL}	Logic "0" Voltage All Inputs	-0.3		.8	V	1, 9

DC ELECTRICAL CHARACTERISTICS[1,7]

(-55°C ≤ T_A ≤ +125°C) (V_{CC} = +5.0 V ± 5%)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC1}	Average V_{CC} Power Supply Current		90	mA	8
I_{CC1}	Average V_{CC} Power Supply Current T_A = 125°C		65	mA	10
I_{IL}	Input Leakage Current (Any Input)	-10	10	μA	2
I_{OL}	Output Leakage Current	-10	10	μA	2
V_{OH}	Output Logic "1" Voltage I_{OUT} = 1 mA	2.4		V	
V_{OL}	Output Logic "0" Voltage I_{OUT} = 4 mA		0.4	V	

AC ELECTRICAL CHARACTERISTICS[3]

(-55°C ≤ T_A ≤ 125°C) (V_{CC} = 5.0 V ± 5%)

		MKB4118A-82		MKB4118A-83		MKB4118A-84			
SYM	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
t_{RC}	Read Cycle Time	150		200		250		ns	
t_{AA}	Address Access Time		150		200		250	ns	4
t_{CEA}	Chip Enable Access Time		75		100		125	ns	4
t_{CEZ}	Chip Enable Data Off Time	5	35	5	40	5	45	ns	
t_{OEA}	Output Enable Access Time		75		100		125	ns	4
t_{OEZ}	Output Enable Data Off Time	5	35	5	40	5	45	ns	
t_{AZ}	Address Data Off Time	10		10		10		ns	
t_{WC}	Write Cycle Time	150		200		250		ns	

AC ELECTRICAL CHARACTERISTICS[3]

($-55°C \leq T_A \leq +125°C$) ($V_{CC} = 5.0\ V \pm 5\%$)

SYM	PARAMETER	MKB4118A-82		MKB4118A-83		MKB4118A-84		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX		
t_{AS}	Address Setup Time	0		0		0		ns	see text
t_{AH}	Address Hold Time	50		65		80		ns	see text
t_{DSW}	Data To Write Setup Time	10		15		20		ns	
t_{DHW}	Data From Write Hold Time	20		25		30		ns	
t_{WD}	Write Pulse Duration	50		60		70		ns	see text
t_{WEZ}	Write Enable Data Off Time	5	35	5	40	5	45	ns	
t_{WPL}	Write Pulse Lead Time	90		130		170		ns	

CAPACITANCE[1,7]

($-55°C \leq T_A \leq +125°C$) ($V_{CC} = +5.0\ V \pm 5\%$)

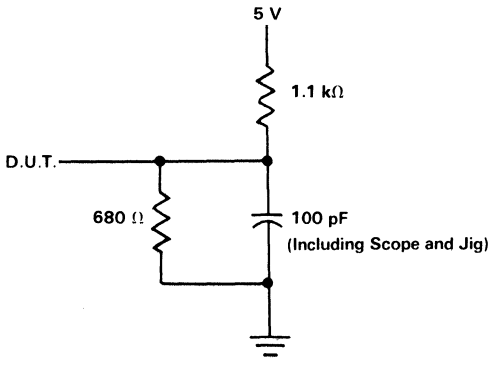
SYM	PARAMETER	TYP	MAX	NOTES
C_I	Capacitance on all pins (except D/Q)	4 pF		5
$C_{D/Q}$	Capacitance on D/Q pins	10 pF		5,6

NOTES:

1. All voltages referenced to V_{SS}.
2. Measured with $.4 \leq V_I$ 5.0 V, outputs deselected and $V_{CC} = 5$ V.
3. AC test conditions: input rise and fall times ≤ 5 ns; input levels 0 V to 3 V; timing measurement reference level 1.5 V.
4. Measured with a load as shown in Figure 3.
5. Effective capacitance calculated from the equation $C = \frac{\Delta Q}{\Delta V}$ with $\Delta V = 3$ volts and power supplies at nominal levels.
6. Output buffer is deselected.
7. A minimum of 2 ms time delay is required after application of V_{CC} (+5 V) before proper device operation can be achieved.
8. I_{CC1} measured with outputs open.
9. Negative undershoots to a minimum of -1.5 V are allowed with maximum of 50 ns pulse width. DC value of low level must not exceed -0.3 V.
10. Power consumption decreases with temperature from a maximum at low temperature to a minimum at high temperature.

OUTPUT LOAD

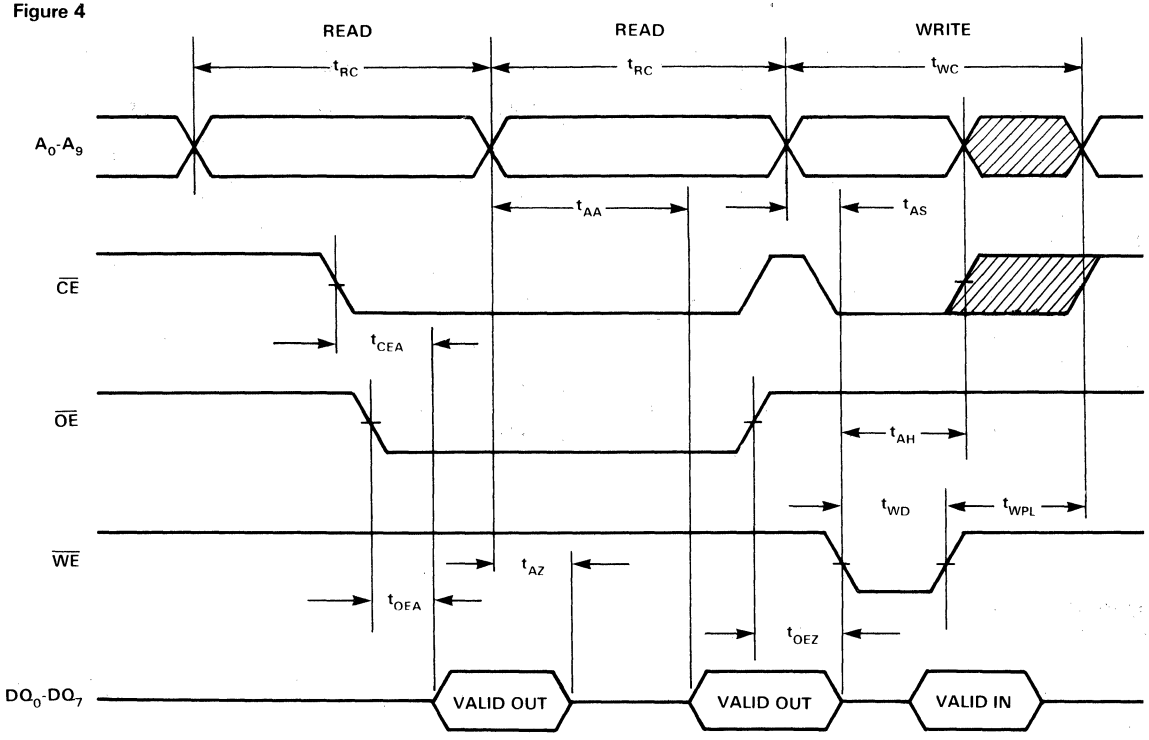
Figure 3



XII

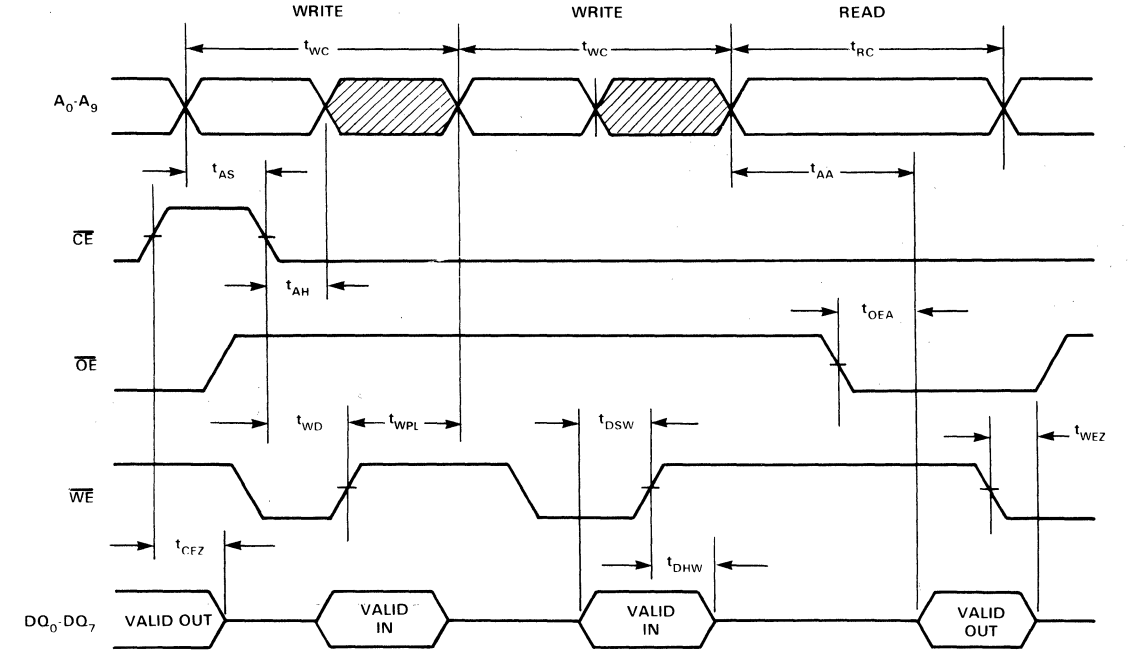
TIMING DIAGRAM

Figure 4



TIMING DIAGRAM

Figure 5



DESCRIPTION (Cont.)

The MKB4118A features a fast $\overline{CE}$ (50% of Address Access) function to permit memory expansion without impacting system access time. A fast $\overline{OE}$ (50% of access time) is included to permit data interleaving for enhanced system performance.

The MKB4118A is pin compatible with Mostek's BYTEWYDE™ memory family of RAMs, ROMs and EPROMs.

OPERATION

Read Mode

The MKB4118A is in the read mode whenever the Write Enable Control input ($\overline{WE}$) is in the high state.

In the read mode of operation, the MKB4118A provides a fast address ripple-through access of data from 8 of 8192 locations in the static storage array. Thus, the unique address specified by the 10 Address Inputs (An) define which 1 of 1024 bytes of data is to be accessed.

A transition on any of the 10 address inputs will disable the 8 data output drivers after t_{AZ}. Valid Data will be available to the 8 data output drivers within t_{AA} after the last address input signal is stable, providing that the $\overline{CE}$ and $\overline{OE}$ access times are satisfied. If $\overline{CE}$ or $\overline{OE}$ access times are not met, data access will be measured from the limiting parameter (t_{CEA} or t_{OEA}) rather than the address. The state of the 8 data I/O signals is controlled by the Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) control signals.

Write Mode

The MKB4118A is in the write mode whenever the Write Enable ($\overline{WE}$) and Chip Enable ($\overline{CE}$) control inputs are in the low state.

The write cycle is initiated by the $\overline{WE}$ pulse going low provided that $\overline{CE}$ is also low. The leading edge of the $\overline{WE}$ pulse is used to latch the status of the address bus.

NOTE: In a write cycle the latter occurring edge of either $\overline{WE}$ or $\overline{CE}$ will determine the start of the write cycle. Therefore, t_{AS}, t_{WD} and t_{AH} are referenced to the latter occurring edge of $\overline{CE}$ or $\overline{WE}$. Addresses are latched at this time. All write cycles whether initiated by $\overline{CE}$ or $\overline{WE}$ must be terminated by the rising edge of $\overline{WE}$. If the output bus has been enabled ($\overline{CE}$ and $\overline{OE}$ low) then $\overline{WE}$ will cause the output to go to the high Z state in t_{WEZ}.

Data In must be valid t_{DSW} prior to the low to high transition of $\overline{WE}$. The Data In lines must remain stable for t_{DHW} after $\overline{WE}$ goes inactive. The write control of the MKB4118A disables the data out buffers during the write cycle; however, $\overline{OE}$ should be used to disable the data out buffers to prevent bus contention between the input data and data that would be output upon completion of the write cycle.

PRELIMINARY

PROCESSED TO MIL-STD-883, METHOD 5004, CLASS B, 16,384 x 1-BIT STATIC RAM MKB4167(P)-870/885/80

FEATURES

- ☐ -55 to +125°C operating temperature range
- ☐ Industry standard 20 pin 300 mil DIP
- ☐ Scaled POLY 5™ technology
- ☐ Fully TTL compatible
- ☐ Density upgrade over the 2147
- ☐ Chip select power down feature
- ☐ Access time equal to cycle time

Part Number	Access Time	Cycle Time	Active Max	Standby Max
MKB4167-870	70 ns	70 ns	660 mW	220 mW
MKB4167-885	85 ns	85 ns	660 mW	220 mW
MKB4167-80	100 ns	100 ns	660 mW	220 mW

DESCRIPTION

The MKB4167 is a high performance 16K x 1 fully static RAM suited for either high speed cache memories or for slower main memory applications. The low standby power allows maximum packing density with the JEDEC Type F chip carrier or the 300 mil wide DIP.

This static RAM offers a cycle time equal to its access time and has fully TTL compatible inputs and outputs resulting in a part that fits easily into a wide range of applications.

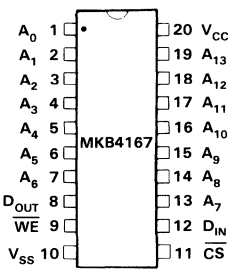
DEVICE OPERATION

The MKB4167 is a fully static Random Access Memory which accesses one of its 16,384 address locations based upon the value presented at its 14 address input pins. This power gated part will function in either a ripple through fashion when the Chip Select ($\overline{CS}$) line is held active (low) or as a clocked part with the $\overline{CS}$ selecting the device. When the $\overline{CS}$ returns high the output is placed in a high impedance or disabled mode and the power drops to a fraction of its active level.

A charge pump is employed on the MKB4167 giving the user two notable advantages. The function of the charge pump is to negatively bias the substrate giving sufficient operating margin internally which allows a single 5 V power supply to be used. Since the charge pump applies a negative

PIN CONNECTIONS

Figure 1



TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	Mode	Output	Power
H	X	Not Selected	High Z	Standby
L	L	Write	High Z	Active
L	H	Read	D_{OUT}	Active

PIN NAMES

A_0 - A_{13}	Address Inputs
$\overline{CS}$	Chip Select
D_{IN}	Data Input
D_{OUT}	Data Output
V_{SS}	Ground
V_{CC}	Power (+5 V)
$\overline{WE}$	Write Enable

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ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to V_{SS} ..... -2.0 V to +7 V
Operating temperature (T_C) ..... -55°C to +125°C
Storage temperature (Ambient) ..... -65°C to +150°C
DC output current ..... 20 mA
Power dissipation ..... 1 Watt

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS[1,10]

($-55°C \leq T_C \leq +125°C$)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	1
V_{SS}	Supply Voltage	0	0	0	V	1
V_{IH}	Logic "1" Voltage All Inputs	2.0	—	$V_{CC}+1$	V	1
V_{IL}	Logic "0" Voltage All Inputs	-2.5	—	0.8	V	1

DC ELECTRICAL CHARACTERISTICS[1,10]

($-55°C \leq T_C \leq +125°C$) ($V_{CC}$ = 5.0 V ± 10%)

SYM	PARAMETER	MKB4167-870		MKB4167-885		MKB4167-80		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX		
I_{CC}	Operating Current AC (t_{RC} = t_{RC} min)		120		120		120	mA	9
I_{CC}	Operating Current (t_C = 125°C)		90		90		90	mA	9,11
I_{SB}	Standby Current (CS ≥ V_{IH})		40		40		40	mA	
I_L	Input Leakage Current (Any Input)		10		10		10	µA	3,12
I_{OL}	Output Leakage Current		50		50		50	µA	2
V_{OH}	Output Logic "1" Voltage I_{OUT} = -4 mA	2.4		2.4		2.4		V	
V_{OL}	Output Logic "0" Voltage I_{OUT} = 8 mA		0.4		0.4		0.4	V	

RECOMMENDED AC OPERATING CONDITIONS AND ELECTRICAL CHARACTERISTICS[10]

($-55°C \leq T_C \leq +125°C$) ($V_{CC} = 5.0\ V \pm 10\%$)

READ CYCLE TIMING

SYM	PARAMETER	MKB4167-870		MKB4167-885		MKB4167-80		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX		
t_{RC}	Read Cycle Time	70		85		100		ns	
t_{AA}	Address Access Time		70		85		100	ns	6
t_{CSA}	Chip Select Access Time		70		85		100	ns	6
t_{OH}	Output Hold From Address Change	5		5		5		ns	
t_{LZ}	Chip Selection to Output Low Z	10		10		10		ns	
t_{HZ}	Chip Deselection to Output High Z	0	30	0	35	0	40	ns	7
t_{PU}	Chip Selection to Power Up Time	0		0		0		ns	
t_{PD}	Chip Deselection to Power Down		50		60		70	ns	

WRITE CYCLE TIMING

SYM	PARAMETER	MKB4167-870		MKB4167-885		MKB4167-80		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX		
t_{WC}	Write Cycle Time	70		85		100		ns	
t_{CW}	Chip Select to End of Write	60		75		85		ns	
t_{AW}	Address Valid to End of Write	60		75		85		ns	
t_{AS1}	Address Setup Time $\overline{WE}$ Controlled Cycle	10		10		10		ns	
t_{AS2}	Address Setup Time $\overline{CS}$ Controlled Cycle	0		0		0		ns	
t_{WP}	Write Pulse Width	40		55		65		ns	
t_{WR}	Write Recovery Time	0		0		0		ns	
t_{DW}	Data Valid to End of Write	30		35		40		ns	
t_{DH}	Data Hold Time	10		10		10		ns	
t_{WZ}	Write Enable to Output in High Z	0	35	0	45	0	50	ns	7
t_{OW}	Output Active From End of Write	0		0		0		ns	

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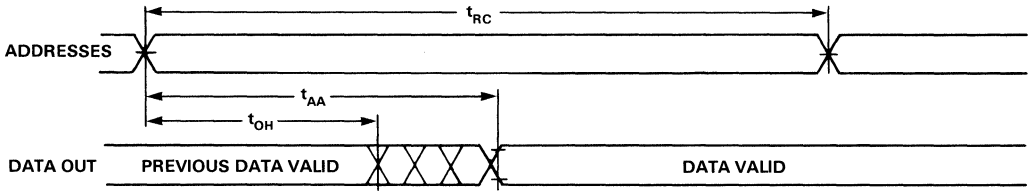
CAPACITANCE[1]

($-55°C \leq T_C \leq +125°C$) ($V_{CC} = +5.0\ V \pm 10\%$)

SYM	PARAMETER	MAX	UNITS	NOTES
C_{IN}	Input Capacitance	5	pF	8
C_{OUT}	Output Capacitance	6	pF	8,9

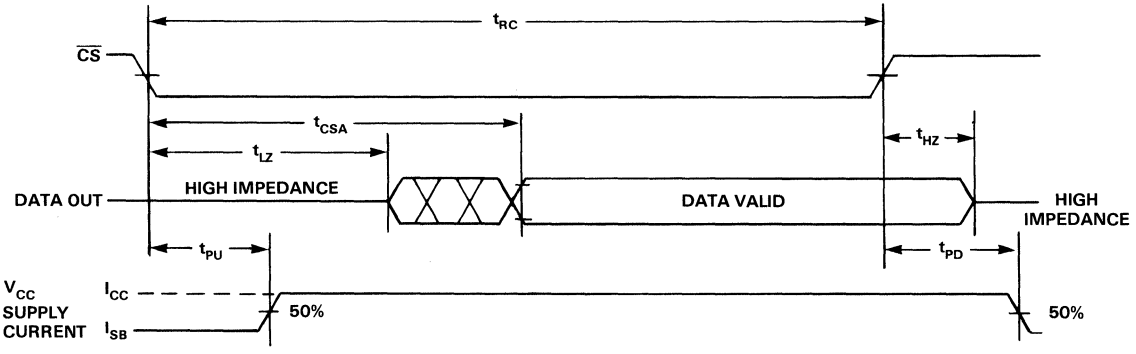
READ CYCLE NUMBER 1 (5,6)

Figure 2



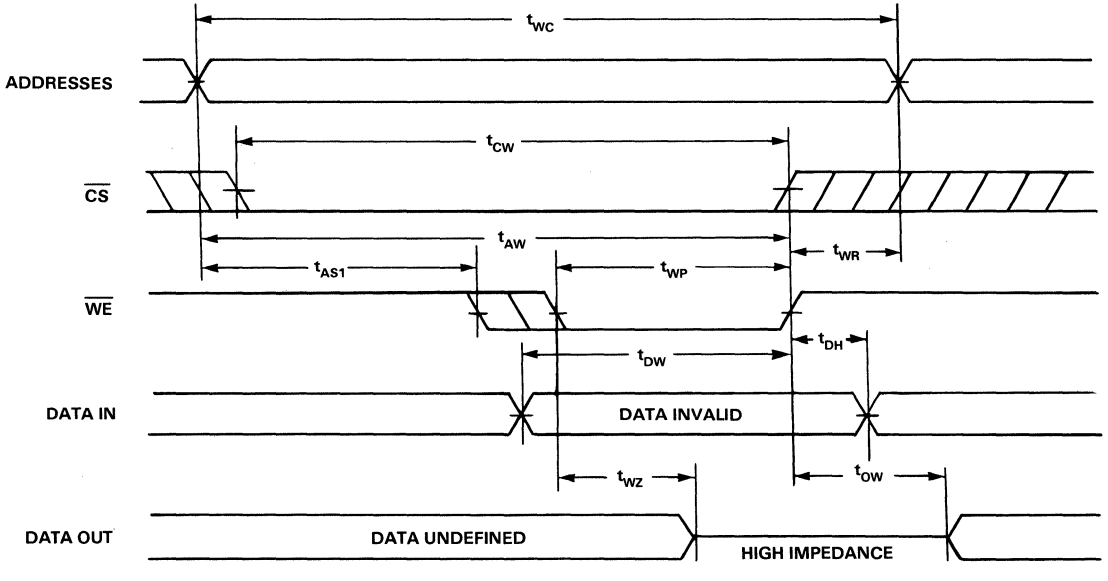
READ CYCLE NUMBER 2 (5,7)

Figure 3



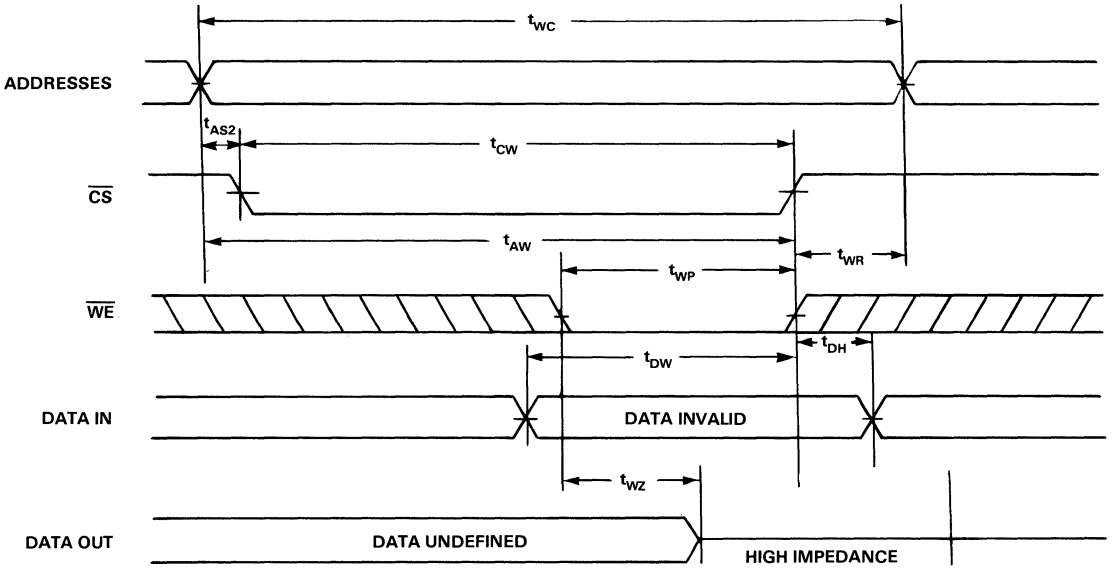
WRITE CYCLE NUMBER 1 ($\overline{WE}$ CONTROLLED)

Figure 4



WRITE CYCLE NUMBER 2
(CS CONTROLLED)

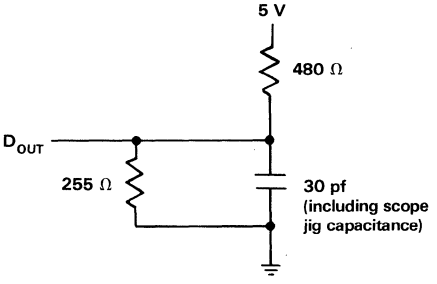
Figure 5



A.C. TEST CONDITIONS

Input Levels .....0 V to 3.0 V
Transition Times .....5 ns
Input timing reference level .....1.5 V
Output timing reference levels....0.8 V - 2.0 V
Output load .....See figure

OUTPUT LOAD



NOTES:

1. All voltages referenced to V_{SS}.
2. $\overline{CS}$ = V_{IH}, V_{CC} = MAX, V_{OUT} = V_{SS} to 4.5 V.
3. V_{CC} = MAX. Also $0 \leq V_{IN} \leq V_{CC}$.
4. t_{HZ} and t_{WZ} defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
5. $\overline{WE}$ is high for Read Cycles.
6. Device is continuously selected $\overline{CS} \leq V_{IL}$.
7. Addresses valid prior to or coincident with $\overline{CS}$ transition low.
8. Effective capacitance calculated from the equation $C = I\frac{\Delta t}{\Delta V}$ with ΔV = 3 volts and power supplies at nominal levels. This parameter is sample tested only.
9. Output buffer is deselected.
10. A minimum of 2 ms is required following the application of V_{CC} (+5 V) before proper device operation is achieved.
11. Power consumption decreases with increasing temperature.

XII

bias to the substrate, it also allows large negative values to exist on the inputs without the fear of damaging the device. Large negative spikes have other drawbacks though, as discussed in the application section. To allow the charge pump sufficient start up time, 2 ms is required following the application of V_{CC} prior to device operation.

Read Cycle

A read cycle occurs whenever $\overline{WE}$ is high and the part is selected. Access time is measured from either the falling edge of CS or from the stable address.

The read cycle number 1 waveform shown in Figure 2 demonstrates the fully static operation of this part when $\overline{CS}$ is held active. The output retains the previous valid data for t_{OH}, after which it is indeterminate until t_{AA}. The output will remain valid until there is a transition on the address inputs and another read cycle occurs.

Operation as shown in read cycle 2 (Figure 3) will take advantage of the power gating feature. If the addresses become stable prior to or as $\overline{CS}$ falls operation is as shown for read cycle 2. The output changes from a high impedance mode after t_{LZ} and becomes indeterminate until t_{CEA} when it is valid.

Once the cycle is ended by the rising edge of $\overline{CS}$, the output becomes undefined. T_{PD} later the part is in the standby mode.

Write Cycle

A write cycle is initiated by the later of $\overline{CS}$ or $\overline{WE}$ going low and is terminated by the rising edge of $\overline{CS}$ or $\overline{WE}$. The output remains in a high impedance mode during a write cycle.

A write enable ($\overline{WE}$) controlled write cycle is shown in Figure 4. The addresses must be valid for t_{ASI} prior to the falling edge of $\overline{WE}$ and remain valid for t_{WR} after $\overline{WE}$ has gone high. If these times are not met, the contents of other cells may be altered. The data in valid is referenced to the rising edge of $\overline{WE}$. Once $\overline{WE}$ goes high, the output again goes active and a read cycle may begin.

A $\overline{CS}$ controlled write cycle is shown in Figure 5. In this cycle, timing is referred to the rising edge of $\overline{CS}$, and both the addresses and $\overline{WE}$ may change following that time. Note that the data must remain valid for t_{DH}.

POWER SUPPLY GRIDDING

All high speed NMOS devices share the trait that their current consumption is composed of high frequency transients. Proper device operation depends on both the use of decoupling capacitors and low impedance printed circuit board paths for both V_{CC} and V_{SS}.

When a designer has the ability to take advantage of multilayer board construction for separate V_{SS} and V_{CC} power planes on optimal low inductance path for power distribution can be had. If a two layer approach is chosen, some care in the design to fully grid V_{CC} and V_{SS} on both sides of the board will give quite satisfactory results. Regardless of the approach taken, a high frequency decoupling capacitor (0.1 μf) should be placed next to each device with larger tantalum capacitors for each row of devices. These efforts will help reduce the ringing on V_{CC} and V_{SS} due to the long inductive path between the power supply and the device.

LINE TERMINATION

To take advantage of high speed memories, high speed TTL drivers are often used. Unfortunately, a printed circuit board trace terminating into a MOS input behaves line an unterminated transmission line. Ringing is the natural result with the potentially destructive voltage levels and noise induced into neighboring PC traces. While the MKB4167 with its charge pump can withstand -2.0 V on any input, such large negative spikes result in a noisy board.

Series termination is a method to dampen these reflections in an easy to implement fashion. By placing a 30 Ω to 5 Ω resistor at the TTL driver's output, the effective impedance of the driver has been raised to more closely match the impedance of the PC trace. These printed circuit board design ideas are explained in more detail in the Memory Data Book And Designers Guide.

MOSTEK®

32,768 x 1-BIT DYNAMIC RAM

Processed to MIL-STD-883, Class B

MKM4332(D)-83/84

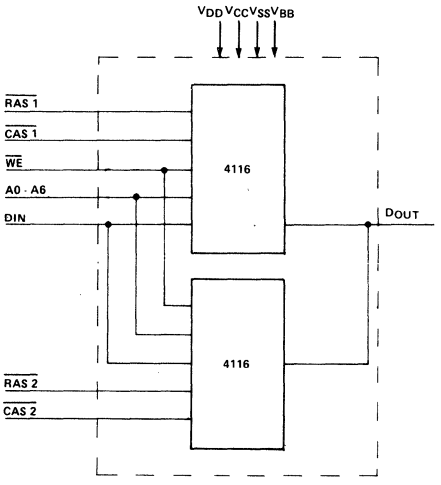
FEATURES

- Extended operating temperature range $-55°C \leq T_C \leq 110°C$
- Utilizes two industry standard MKB4116 devices in chip carriers mounted on an 18-pin ceramic motherboard DIP
- 200ns access time, 375ns cycle (MKM4332-83)
  250ns access time, 410ns cycle (MKM4332-84)
- Separate $\overline{RAS}$, $\overline{CAS}$ Clocks
- ± 10% tolerance on all power supplies (+12V, ± 5V)
- Low power: 482mW active, 40mW standby (max)
- Output data controlled by $\overline{CAS}$ and unlatched at end of cycle to allow two dimensional chip selection and extended page boundary
- Common I/O capability using "early write" operation
- Read-Modify-Write, $\overline{RAS}$-only refresh capability
- All inputs TTL compatible, low capacitance, and protected against static charge
- 128 refresh cycles (2 msec refresh interval)
- Pin compatible to MKB4116, MKB4516 and MKB4164
- Detailed test flows for the individual MKB4116 chip carriers and the completed D-package motherboard assembly are presented in the last pages of this data sheet.

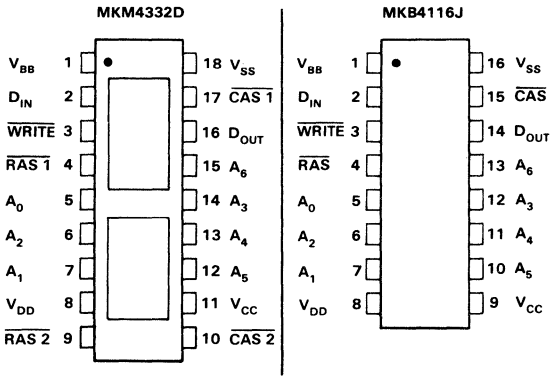
DESCRIPTION

The MKM4332 is a new generation MOS dynamic random access memory circuit organized as 32,768 words by 1 bit. As a state-of-the-art MOS memory device, the MKM4332 (32K RAM) incorporates advanced circuit techniques

FUNCTIONAL DIAGRAM



PIN CONNECTIONS AND MKB4116 COMPATIBILITY



PIN NAMES

A_0-A_6	Address Inputs	$\overline{WRITE}$	Read/Write Input
$\overline{CAS}$	Column Address Strobe	V_{BB}	Power (-5)
D_{IN}	Data In	V_{CC}	Power (+5V)
D_{OUT}	Data Out	V_{DD}	Power (+12V)
$\overline{RAS}$	Row Address Strobe	V_{SS}	Ground

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ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to V_{BB} ..... -0.5V to +20V
Voltage on V_{DD}, V_{CC} supplies relative to V_{SS} ..... -1.0V to +15.0V
V_{BB} - V_{SS} (V_{DD} - V_{SS} > 0V) 0V
Operating Temperature, T_C (case operating) ..... -55°C to +110°C
Storage Temperature (Ambient) ..... -65°C to +130°C
Short Circuit Output Current 50mA
Power Dissipation ..... 1 Watt

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS[6]

(0°C ≤ T_C ≤ 110°C)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{DD}	Supply Voltage	10.8	12.0	13.2	V	2
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2,3
V_{SS}	Supply Voltage	0	0	0	V	2
V_{BB}	Supply Voltage	-4.5	-5.0	-5.5	V	2
V_{IHC}	Input High (Logic 1) Voltage $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	2.4	—	7.0	V	2
V_{IH}	Input High (Logic 1) Voltage all inputs except $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	2.2	—	7.0	V	2
V_{IL}	Input Low (Logic 0) Voltage, all inputs	-1.0	—	.8	V	2

DC ELECTRICAL CHARACTERISTICS

(0°C ≤ T_C ≤ 110°C) (V_{DD} = 12.0V ± 10%; V_{CC} = 5.0V ± 10%; -5.5V ≤ V_{BB} ≤ -4.5V; V_{SS} = 0V)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
I_{DD1} I_{CC1} I_{BB1}	OPERATING CURRENT Average power supply operating current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = t_{RC} Min)		37.5 400	mA μA	4 5
I_{DD2} I_{CC2} I_{BB2}	STANDBY CURRENT Power supply standby current ($\overline{RAS}$ = V_{IHC} D_{OUT} = High Impedance)	 -20 	4.5 20 200	mA μA μA	
I_{DD3} I_{CC3} I_{BB3}	REFRESH CURRENT Average power supply current, refresh mode	 -20 	27 20 400	mA μA μA	4
I_{DD4} I_{CC4} I_{BB4}	PAGE MODE CURRENT Average power supply current, page-mode operation ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling; t_{PC} = t_{PC} Min)		29.5 400	mA μA	4 5
$I_{I(L)}$	INPUT LEAKAGE Input leakage current, any input (V_{BB} = -5V, 0V ≤ V_{IN} ≤ +7.0V, all other pins not under test = 0 volts)	-20	20	μA	

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
$I_{O(L)}$	OUTPUT LEAKAGE Output leakage current (D_{OUT} is disabled, 0V ≤ V_{OUT} ≤ +5.5V)	-20	20	μA	
	OUTPUT LEVELS				
V_{OH}	Output high (Logic 1) voltage (I_{OUT} = -5mA)	2.4		V	3
V_{OL}	Output low (Logic 0) voltage (I_{OUT} = 4.2mA)		0.4	V	

NOTES

1. T_C is specified here for operation at frequencies to $t_{RC} \leq t_{RC}$ (min). Operation at higher cycle rates with reduced ambient temperatures and higher power dissipation is permissible, however, provided AC operating parameters are met. See supplemental MK4332 data sheet for AC derating curves.
2. All voltages referenced to V_{SS}.
3. Output voltage will swing from V_{SS} to V_{CC} when activated with no current loading. For purposes of maintaining data in standby mode, V_{CC} may be reduced to V_{SS} without affecting refresh operations or data retention. However, the V_{OH} (min) specification is not guaranteed in this mode.
4. I_{DD1}, I_{DD3}, and I_{DD4} depend on cycle rate.
5. I_{CC1} and I_{CC4} depend upon output loading. During readout of high level data V_{CC} is connected through a low impedance (135 Ω typ) to data out. At all other times I_{CC} consists of leakage currents only.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS[6,7,8]

(0°C ≤ T_C ≤ 110°C)[1] (V_{DD} = 12.0V ± 10%; V_{CC} = 5.0V ± 10%, V_{SS} = 0V, -5.5V ≤ V_{BB} ≤ -4.5V)

		MKM4332-83		MKM4332-84			
SYM	PARAMETER	MIN	MAX	MIN	MAX	UNITS	NOTES
t_{RC}	Random read or write cycle time	375		410		ns	9
t_{RWC}	Read-write cycle time	375		425		ns	9
t_{RMW}	Read modify write cycle time	405		500		ns	9
t_{PC}	Page mode cycle time	225		275		ns	9
t_{RAC}	Access time from $\overline{RAS}$		200		250	ns	10,12
t_{CAC}	Access time from $\overline{CAS}$		135		165	ns	11,12
t_{OFF}	Output buffer turn-off delay	0	50	0	60	ns	13
t_T	Transition time (rise and fall)	3	50	3	50	ns	8
t_{RP}	$\overline{RAS}$ precharge time	120		150		ns	
t_{RAS}	$\overline{RAS}$ pulse width	200	5000	250	5000	ns	
t_{RSH}	$\overline{RAS}$ hold time	135		165		ns	
t_{CSH}	$\overline{CAS}$ hold time	200		250		ns	
t_{CAS}	$\overline{CAS}$ pulse width	135	5000	165	5000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ delay time	25	65	35	85	ns	14
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ precharge time	0		0		ns	
t_{ASR}	Row Address set-up time	0		0		ns	
t_{RAH}	Row Address hold time	25		35		ns	
t_{ASC}	Column Address set-up time	0		0		ns	
t_{CAH}	Column Address hold time	55		75		ns	

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SYM	PARAMETER	MKM4332-85		MKM4332-84		UNITS	NOTES
		MIN	MAX	MIN	MAX		
t_{AR}	Column Address hold time referenced to $\overline{RAS}$	120		160		ns	
t_{RCS}	Read command set-up time	0		0		ns	
t_{RCH}	Read command hold time	0		0		ns	
t_{WCH}	Write command hold time	55		75		ns	
t_{WCR}	Write command hold time referenced to $\overline{RAS}$	120		160		ns	
t_{WP}	Write command pulse width	55		75		ns	
t_{RWL}	Write command to $\overline{RAS}$ lead time	70		85		ns	
t_{CWL}	Write command to $\overline{CAS}$ lead time	70		85		ns	
t_{DS}	Data-in set-up time	0		0		ns	15
t_{DH}	Data-in hold time	55		75		ns	15
t_{DHR}	Data-in hold time referenced to $\overline{RAS}$	120		160		ns	
t_{CP}	$\overline{CAS}$ precharge time (for page-mode cycle only)	80		100		ns	
t_{REF}	Refresh period		2		2	ms	
t_{WCS}	$\overline{WRITE}$ command set-up time	0		0		ns	16
t_{CWD}	$\overline{CAS}$ to $\overline{WRITE}$ delay	80		90		ns	16
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ delay	145		175		ns	16

NOTES

6. Several cycles are required after power-up before proper device operation is achieved. Any 8 cycles which perform refresh are adequate for this purpose.
7. AC measurements assume t_T = 5ns.
8. V_{IHC} (min) or V_{IH} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IHC} or V_{IH} and V_{IL}.
9. The specifications for t_{RC} (min) t_{RMW} (min) and t_{RWC} (min) are used only to indicate cycle time at which proper operation over the full temperature range (-55°C ≤ T_C ≤ 110°C) is assured.
10. Assumes that $t_{RCD} \leq t_{RCD}$ (max). If t_{RCD} is grater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
11. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
12. Measured with a load equivalent to 2 TTL loads and 100pF.
13. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
14. Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively ty t_{CAC}.
15. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in delayed write or read-modify-write cycles.
16. t_{WCS}, t_{CWD} and t_{RWD} are restrictive operating parameters in read-write and read-modify-write cycles only. If $t_{WCS} \leq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle. If $t_{CWD} \leq t_{CWD}$ (min) and $t_{RWD} \leq t_{RWD}$ (min), the cycle is a read-write cycle and the data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.
17. Effective capacitance calculated from the equation C - 1Δt/ΔV with ΔV - 3 volts and power supplies at nominal levels.
18. $\overline{CAS}$ = V_{HK} to disable D_{OUT}.

AC ELECTRICAL CHARACTERISTICS

(-55°C ≤ T_C ≤ 110°C) (V_{DD} = 12.0V ± 10%; V_{SS} = 0V; -5.5V ≤ V_{BB} ≤ -4.5)

SYM	PARAMETER	TYP	MAX	UNITS	NOTES
C_{I1}	Input Capacitance (A_0 - A_6), D_{IN}	8	10	pF	17
C_{I2}	Input Capacitance $\overline{RAS}$, $\overline{CAS}$	8	10	pF	17
C_O	Output Capacitance (D_{OUT})	10	14	pF	17,18
C_{I3}	Input Capacitance $\overline{WRITE}$	16	20	pF	17

MKB4116 CHIP CARRIER PROCESSING
(MIL-STD-883, Class B)

PROCESS STEP	CONDITION	LIMITS
[Q][1] Die Inspect	Method 2010 Condition B	100%
[Q] Preseal Inspect	Method 2010 Condition B	100%
Stabilization Bake	24 hrs., 150°C	100%
Temp Cycle	-65/+150°C, 10 cycles	100%
Centrifuge	30 Kg, Y_1	100%
Fine Leak	5×10^{-8}cc/sec	100%
Gross Leak	Method 1014, Condition C	100%
Pre-Stress Electrical Test 1	Max Rated Temperature	100%
Voltage/Temp Stress	12 hr., +125°C, Dynamic	100%
Post Stress Electrical Test 2	Max Rated Temperature	100%
Burn-in	160 hr., +125°C, Dynamic	100%
Final Electrical Tests 3, 4	Max. Rated Temperature	100%
	Min. Rated Temperature	100%
[Q] Q.A. Lot Acceptance	Method 5005.5, Group A, Class B	
[Q] Fine Leak Sample	5×10^{-8} cc/sec	AQL = .4%
[Q] Gross Leak Sample	Method 1014, Condition C	AQL = .4%
External Visual		100%
[Q] Q.C. Final Inspect		AQL = 2.5%
[Q] Q.C. Pre-Shipment Inspect		AQL = 1.0%

[1] [Q] = Quality Control Check

MKM4332D D PACKAGE (MOTHERBOARD) PROCESSING

PROCESS STEP	CONDITION	LIMITS
Motherboard Assembly		
[Q][1] Visual Inspection		100%
Electrical Test	Max. Rated Temp.	100%
Visual Inspection		100%
[Q] Fine Leak Sample	5×10^{-8} cc/sec	
[Q] Gross Leak Sample	Method 1014, Condition C	AQL = .4%
[Q] Group A Electrical Lot Acceptance	Method 5005.5, Group A, Subgroups 2, 5, 8 Max, 10	
[Q] QC Final Inspection		AQL = 2.5%

[1] [Q] = Quality Control Check

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DESCRIPTION (Continued)

designed to provide wide operating margins, both internally and to the system user.

The technology used to fabricate the MKM4332 is Mostek's double-poly, N-channel silicon gate, POLY II™ process. This process, coupled with the use of a single transistor dynamic storage cell, provides the maximum possible circuit density and reliability, while maintaining high performance capability. The use of dynamic circuitry throughout, including sense amplifiers, assures that power dissipation is minimized without any sacrifice in speed or operating margin. These factors combine to make the MKM4332 a truly superior RAM product.

Multiplexed address inputs (a feature pioneered by Mostek for its 4K RAMs) permits the MKM4332 to be packaged in a standard 18-pin DIP. This standard package configuration, is compatible with widely available automated testing and insertion equipment, and it provides the highest possible system bit densities and simplifies system upgrade from 16K to 64K RAMs for new generation applications. Non-critical clock timing requirements allow use of the multiplexing technique while maintaining high performance.

PRELIMINARY

PROCESSED TO MIL-STD-883, METHOD 5004, CLASS B, 16,384 x 1 BIT-DYNAMIC RAM MKB4516(P/J/E) - 80/81/82

FEATURES

- Military temperature range: $-55°C \leq T_C \leq +110°C$
- Recognized industry standard 16-pin configuration from Mostek
- Single +5 V (± 10%) supply operation
- On chip substrate bias generator for optimum performance
- 100 ns access time, 235 ns cycle time (MKB4516-80)
  120 ns access time, 270 ns cycle time (MKB4516-81)
  150 ns access time, 320 ns cycle time (MKB4516-82)
- Common I/O capability using "early write"
- Interchangeable with M2118
- Read, Write, Read-Write, Read-Modify-Write and Page-Mode capability
- All inputs TTL compatible, low capacitance, and are protected against static charge
- Scaled POLY 5 technology
- Pin compatible with the MKB4564 (64K RAM)
- 128 refresh cycles (2 msec)
- Available to the DESC part number 8101501EX
- Indefinite D_{OUT} hold using $\overline{CAS}$ control

DESCRIPTION

The MKB4516 is a single +5 V power supply version of the industry standard MKB4116, 16,384 x 1 bit dynamic RAM.

The high performance features of the MKB4516 are achieved by state-of-the-art circuit device techniques as well as utilization of Mostek's "Scaled POLY 5" process technology. Features include access times starting where the current generation 16K RAMs leave off, TTL compatibility, and +5 V operation.

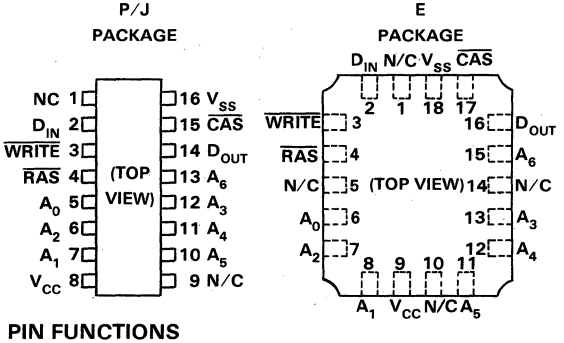
The MKB4516 is capable of a variety of operations including READ, WRITE, READ-WRITE, READ-MODIFY-WRITE, PAGE MODE, and REFRESH. The output of the MKB4516 can be held valid indefinitely by holding $\overline{CAS}$ active low. This is quite useful since a refresh cycle can be performed while holding data valid from a previous cycle.

The MKB4516 is designed to be compatible with JEDEC standards for the 64K x 1 dynamic RAM. It is intended to extend the life cycle of the 16K RAM, as well as create new applications due to its superior performance. Compatibility with the MKB4564 will also permit a common board design to service both the MKB4516 and the MKB4564 (64K RAM) designs. The MKB4516 will therefore permit a smoother transition to the 64K RAM as the industry standard MKB4027 did for the MKB4116.

The small memory user need no longer pay a three power supply penalty for achieving the economics of using dynamic RAM over static RAM with this new generation device.

PIN OUT

Figure 1



PIN FUNCTIONS

A_0 - A_6	Address Inputs	$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Col. Address Strobe	$\overline{WRITE}$	Read/Write Input
D_{IN}	Data In	$\overline{RFSH}$	Refresh
D_{OUT}	Data Out	V_{CC}	Power (+5 V)
NC	Not Connected	V_{SS}	GND

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ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -2.0 V to +7.0 V
Operating Temperature, T_C (Case) ..... -55°C to +110°C
Storage Temperature ..... -65°C to +150°C
Power Dissipation ..... 1 Watt
Short Circuit Output Current ..... 50 mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

($-55°C \leq T_C \leq 110°C$)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High (Logic 1) Voltage, All Inputs	2.4	—	$V_{CC}+1$	V	2
V_{IL}	Input Low (Logic 0) Voltage, All Inputs	-2.0	—	.8	V	2,17

DC ELECTRICAL CHARACTERISTICS

($-55°C \leq T_C \leq 110°C$)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC1}	OPERATING CURRENT Average power supply operating current ($\overline{RAS}$, $\overline{CAS}$ cycling, $t_{RC} = t_{RC}$ min.)		38	mA	3
I_{CC1}	Operating Current (T_C = 110°C)		30	mA	3,18
I_{CC2}	STANDBY CURRENT Power supply standby current ($\overline{RAS} = \overline{CAS} = V_{IH}$ D_{OUT} = High Impedance)		4	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply current, refresh mode ($\overline{RAS}$ cycling, $\overline{CAS} = V_{IH}$; t_{RC} = min.)		32	mA	3
I_{CC4}	PAGE MODE CURRENT Average power supply current, page mode operation ($\overline{RAS} = V_{IL}$, $t_{RAS} = t_{RAS}$ max., $\overline{CAS}$ cycling; $t_{PC} = t_{PC}$ min.)		35	mA	3
$I_{I(L)}$	INPUT LEAKAGE Input leakage current, any input ($0 V \leq V_{IN} \leq +5.5$ V, all other pins not under test = 0 volts	-10	10	μA	
$I_{O(L)}$	OUTPUT LEAKAGE Output leakage current (D_{OUT} is disabled, $0 V \leq V_{OUT} \leq +5.5$ V)	-10	10	μA	
V_{OH} V_{OL}	OUTPUT LEVELS Output High (Logic 1) voltage (I_{OUT} = -5 mA) Output Low (Logic 0) voltage (I_{OUT} = 4.2 mA	2.4	 0.4	V V	

AC ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATION CONDITIONS (4, 5, 9)

($-55°C \leq T_C \leq 110°C$), $V_{CC} = 5.0\ V \pm 10\%$

SYMBOL		PARAMETER	MK4516-80		MK4516-81		MK4516-82		UNITS	NOTES
STD	ALT		MIN	MAX	MIN	MAX	MIN	MAX		
t_{RELREL}	t_{RC}	Random read or write cycle time	235		270		320		ns	6
t_{RELREL} (RMW)	t_{RMW}	Read-modify-write cycle time	285		320		410		ns	6
t_{RELREL} (PC)	t_{PC}	Page mode cycle time	125		145		190		ns	6
t_{RELQV}	t_{RAC}	Access time from $\overline{RAS}$		100		120		150	ns	7
t_{CELQV}	t_{CAC}	Access time from $\overline{CAS}$		55		65		80	ns	8
t_{CEHQZ}	t_{OFF}	Output buffer turn-off delay	0	45	0	50	0	60	ns	9
t_T	t_T	Transition time (rise and fall)	3	50	3	50	3	50	ns	5
t_{REHREL}	t_{RP}	$\overline{RAS}$ precharge time	110		120		135		ns	
t_{RELREH}	t_{RAS}	$\overline{RAS}$ pulse width	115	10^4	140	10^4	175	10^4	ns	
t_{CELREH}	t_{RSH}	$\overline{RAS}$ hold time	70		85		105		ns	
t_{RELCEH}	t_{CSH}	$\overline{CAS}$ hold time	100		120		165		ns	
t_{CELCEH}	t_{CAS}	$\overline{CAS}$ pulse width	55	10^4	65	10^4	95	10^4	ns	
t_{RELCEL}	t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ delay time	25	45	25	55	25	70	ns	10
t_{REHWX}	t_{RRH}	Read command hold time referenced to $\overline{RAS}$	0		0		0		ns	11
t_{AVREL}	t_{ASR}	Row Address set-up time	0		0		0		ns	
t_{RELAX}	t_{RAH}	Row Address hold time	15		15		15		ns	
t_{AVCEL}	t_{ASC}	Column Address set-up time	0		0		0		ns	
t_{CELAX}	t_{CAH}	Column Address hold time	15		15		20		ns	
$t_{RELA(C)X}$	t_{AR}	Column Address hold time referenced to $\overline{RAS}$	60		70		90		ns	
t_{WHCEL}	t_{RCS}	Read command set-up time	0		0		0		ns	
t_{CEHWX}	t_{RCH}	Read command hold time referenced to $\overline{CAS}$	0		0		0		ns	11
t_{CELWX}	t_{WCH}	Write command hold time	25		30		45		ns	
t_{RELWX}	t_{WCR}	Write command hold time referenced to $\overline{RAS}$	70		85		115		ns	
t_H	t_{WP}	Write command pulse width	25		30		50		ns	
t_{WLREH}	t_{RWL}	Write command to $\overline{RAS}$ lead time	60		65		110		ns	
t_{WLCEH}	t_{CWL}	Write command to $\overline{CAS}$ lead time	45		50		100		ns	

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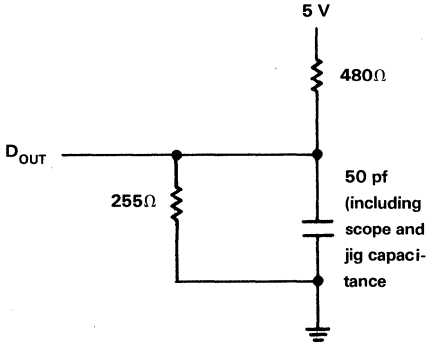
AC ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS (Continued)

SYMBOL		PARAMETER	MK4516-10		MK4516-12		MK4516-15		UNITS	NOTES
STD	ALT		MIN	MAX	MIN	MAX	MIN	MAX		
t_{DVCEL}	t_{DS}	Data-in set-up time	0		0		0		ns	12
t_{CELDX}	t_{DH}	Data-in hold time	25		30		45		ns	12
t_{RELDX}	t_{DHR}	Data-in hold time referenced to $\overline{RAS}$	70		85		115		ns	
t_{CEHCEL} (PC)	t_{CP}	$\overline{CAS}$ precharge time (for page mode cycle only)	60		70		85		ns	
t_{RVRV}	t_{REF}	Refresh period		2		2		2	ms	
t_{WLCEL}	t_{WCS}	WRITE command set-up time	0		0		0		ns	13
t_{CELWL}	t_{CWD}	$\overline{CAS}$ to WRITE delay	55		65		80		ns	13
t_{RELWL}	t_{RWD}	$\overline{RAS}$ to WRITE delay	100		120		150		ns	13
t_{CEHREL}	t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ precharge time	0		0		0		ns	

AC TEST CONDITIONS

Input Levels.....0 V to 3.0 V
Transition times ..... 5 ns
Input timing reference level .....1.5 V
Output timing reference levels.....0.8 V - 2.0 V
Output load .....See figure

OUTPUT LOAD



CAPACITANCE

($-55°C \leq T_C \leq 110°C$) ($V_{CC}$ = 5.0 V ± 10%)

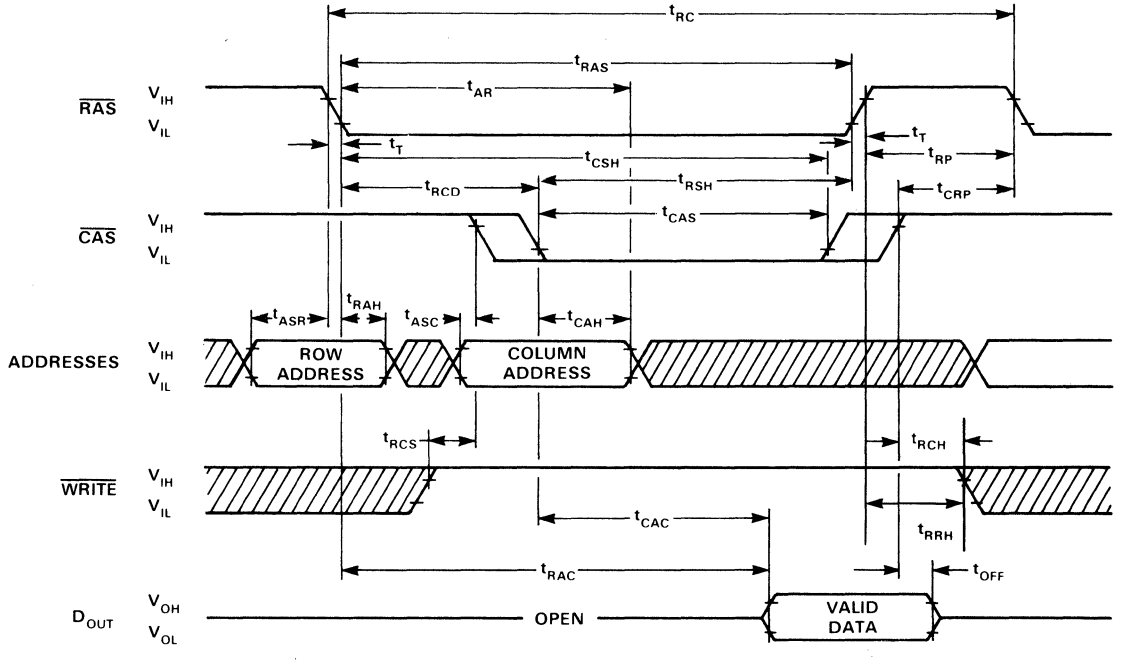
SYMBOL	PARAMETER	TYP	MAX	UNITS	NOTES
C_{11}	Input (A_0 - A_5), D_{IN}	4	5	pF	15
C_{12}	Input $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	8	10	pF	15
C_O	Output (D_{OUT})	5	7	pF	15,16

NOTES:

1. No user connection to Pin 1 (Leadless Chip Carrier only). This pin must be left floating.
2. All voltages referenced to V_{SS}.
3. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open.
4. An initial pause of 500 μs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved. $\overline{RAS}$ may be cycled during the initial pause.
5. V_{IH} min. and V_{IL} max are reference levels for measuring timing of Input signals. Transition times are measured between V_{IH} and V_{IL}.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($-55°C \leq T_C \leq +110°C$) is assigned.
7. Assumes that $t_{RCD} \leq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
8. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
9. t_{OFF} max defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
10. Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
11. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
12. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in delayed write or read-modify-write.
13. t_{WCS}, t_{CWD}, and t_{RWD} are restrictive operating parameters in READ/WRITE and READ/MODIFY/WRITE cycles only. If $t_{WCS} \geq t_{WCS}$ (min) the cycle is an EARLY WRITE cycle and the data output will remain open circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min) the cycle is a READ/WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met the condition of the data out (at access time and until $\overline{CAS}$ goes back to V_{IH}) is indeterminate.
14. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transmit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
15. Effective capacitance calculated from the equation $c = I \frac{\Delta T}{\Delta V}$ with $\Delta V = 3$ volts and power supply at nominal level. This parameter is sample tested only.
16. $\overline{CAS}$ = V_{IH} D_{OUT}.
17. Includes the dc level and all instantaneous signal excursions.
18. Power consumption decreases with increasing temperature.

READ CYCLE

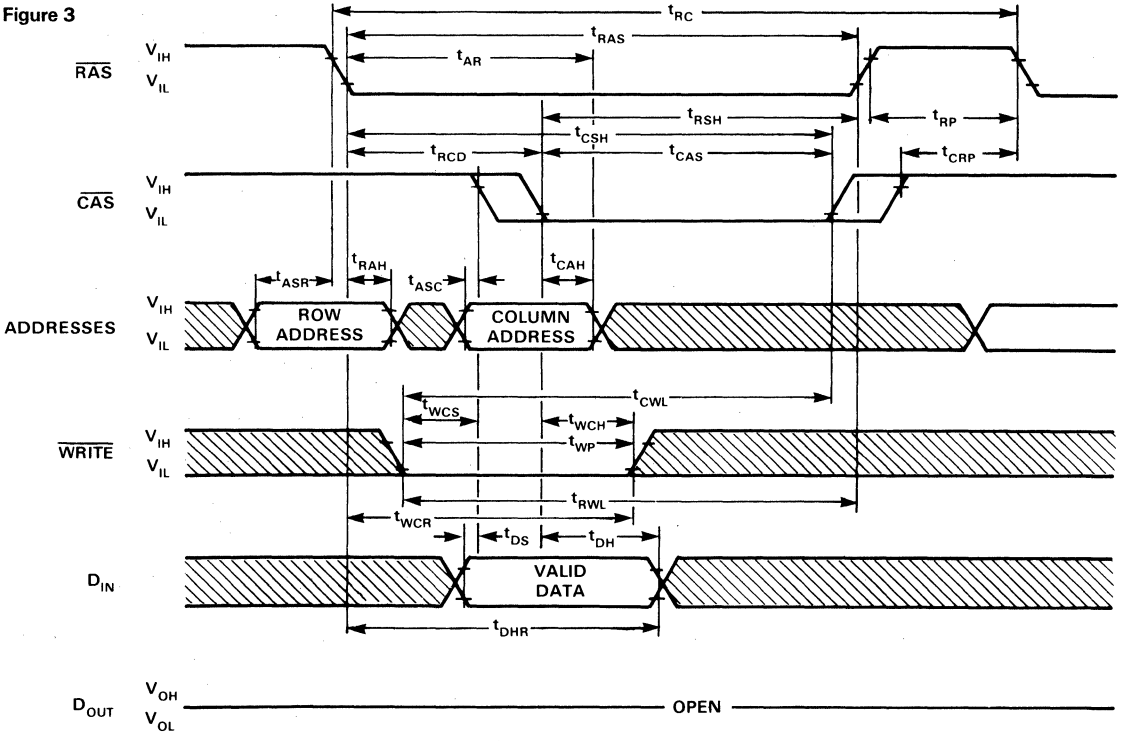
Figure 2



XII

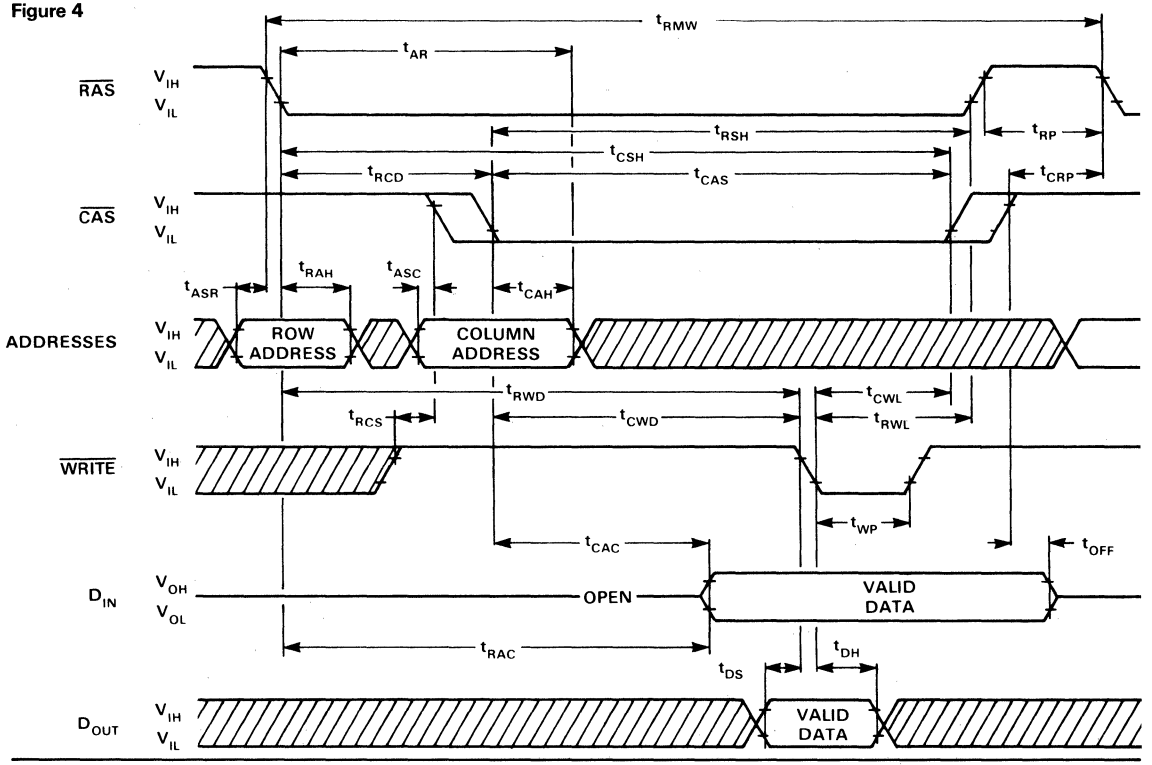
WRITE CYCLE

Figure 3



READ-WRITE/READ-MODIFY-WRITE CYCLE

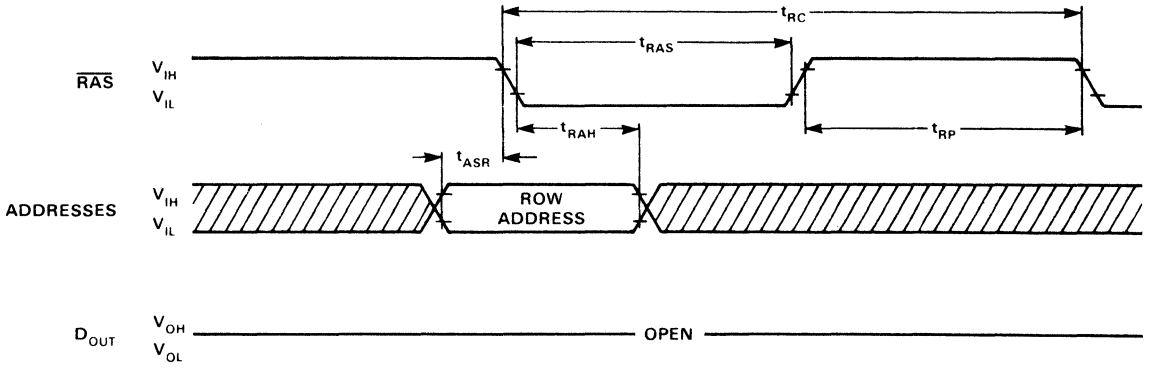
Figure 4



"$\overline{RAS}$-ONLY" REFRESH CYCLE

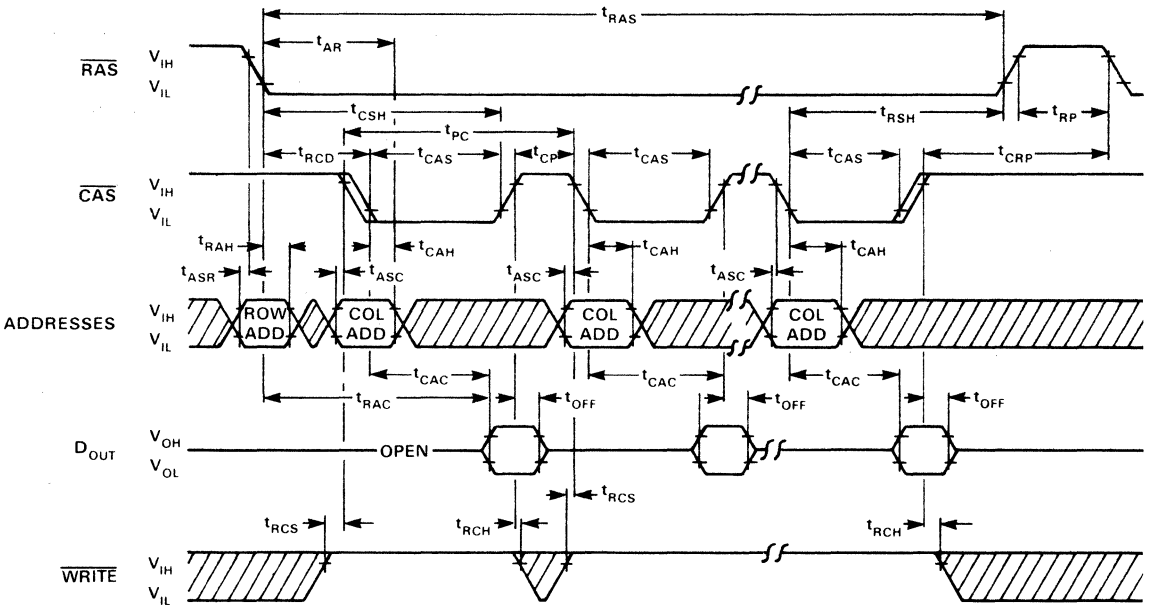
NOTE: $\overline{CAS}$ = V_{IH} $\overline{WRITE}$ = DON'T CARE

Figure 5



PAGE MODE READ CYCLE

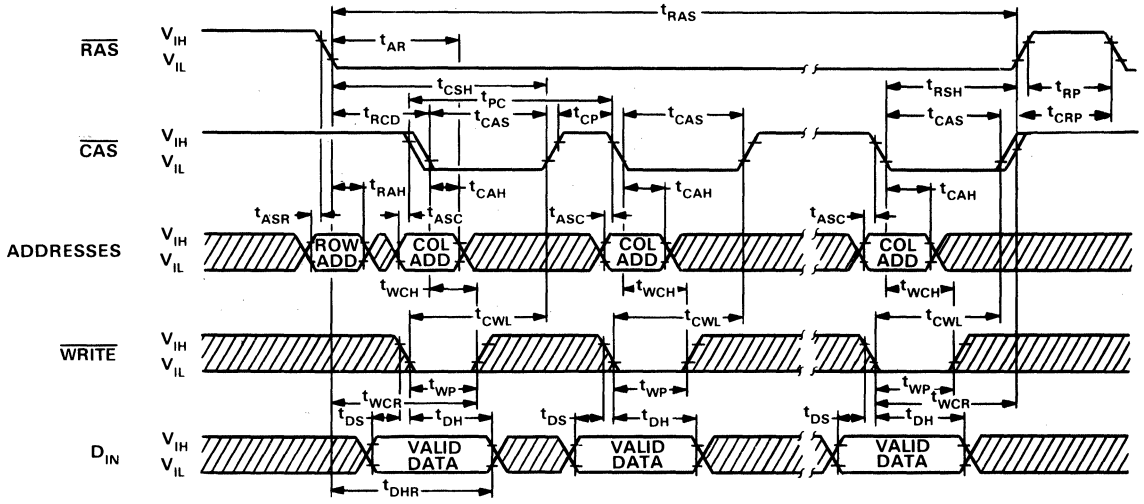
Figure 6



XII

PAGE MODE WRITE CYCLE

Figure 7



OPERATION

The 14 address bits required to decode 1 of the 16,384 cell locations within the MKB4516 are multiplexed onto the 7 address inputs and latched into the on-chip address latches by externally applying two negative going TTL-level clocks. The first clock, Row Address Strobe ($\overline{RAS}$), latches the 7 row addresses into the chip. The high-to-low transition of the second clock, Column Address Strobe ($\overline{CAS}$), subsequently latches the 7 column addresses into the chip. Each of these signals, $\overline{RAS}$ and $\overline{CAS}$, triggers a sequence of events which are controlled by different delayed internal clocks. The two clock chains are linked together logically in such a way that the address multiplexing operation is done outside of the critical timing path for read data access. The later events in the $\overline{CAS}$ clock sequence are inhibited until the occurence of a delayed signal derived from the $\overline{RAS}$ clock chain. This "gated $\overline{CAS}$" feature allows the $\overline{CAS}$ clock to be externally activated as soon as the Row Address Hold specification (t_{RAH}) has been satisfied and the address inputs have been changed from Row address to Column address information.

The "gated $\overline{CAS}$" feature permits $\overline{CAS}$ to be acitvated at any time after t_{RAH} and it will have no effect on the worst case data access time (t_{RAC}) up to the point in time when the delayed row clock no longer inhibits the remaining sequence of column clocks. Two timing endpoints result from the internal gating of $\overline{CAS}$ which are called t_{RCD} (min) and t_{RCD} (max). No data storage or reading errors will result if $\overline{CAS}$ is applied to the MKB4516 at a point in time beyond the t_{RCD} (max) limit. However, access time will then be determined exclusively by the accesss time from $\overline{CAS}$ (t_{CAC}) rather than from $\overline{RAS}$ (t_{RAC}), and $\overline{RAS}$ access time will be lengthed by the amount that t_{RCD} exceeds the t_{RCD} (max) limit.

Data Input/Output

Data to be written into a selected cell is latched into an on-chip register by a combination of $\overline{WRITE}$ and $\overline{CAS}$ while $\overline{RAS}$ is active. The latter of $\overline{WRITE}$ or $\overline{CAS}$ to make its negative transition is the strobe for the Data In (D_{IN}) register. This permits several options in the write cycle timing. In a write cycle, if the $\overline{WRITE}$ input is brought low (active) prior to $\overline{CAS}$ being brought low (active), the D_{IN} is strobed by $\overline{CAS}$, and the Input Data set-up and hold times are referenced to $\overline{CAS}$. If the input data is not available at $\overline{CAS}$ time (late write), or if it is desired that the cycle be a read-write or read-modify-write cycle the $\overline{WRITE}$ signal should be delayed until after $\overline{CAS}$ has made its negative transition. In this "delayed write cycle" the data input is set-up and hold times are referenced to the negative edge of $\overline{WRITE}$ rather than $\overline{CAS}$.

Data is retrieved from the memory in a read cycle by maintaining $\overline{WRITE}$ in the inactive or high state throughout the portion of the memory cycle in which both the $\overline{RAS}$ and $\overline{CAS}$ are low (active). Data read from the selected cell is available at the output port within the specified access time. The output data is the same polarity (not inverted) as the input data.

Data Output Control

The normal condition of the Data Output (D_{OUT}) of the MK4516 is the high impedance (open circuit) state; anytime $\overline{CAS}$ is high (inactive) the D_{OUT} pin will be floating.

Once the output data port has gone active, it wil remain valid until $\overline{CAS}$ is taken to the precharge (inactive high) state.

Page Mode Operation

The Page Mode feature of the MKB4516 allows for successive memory operations at multiple column locations within the same row address. This is done by strobing the row address into the chip and maintaining the $\overline{RAS}$ signal low (active) throughout all successive memory cycles in which the row address is common. The first success within a page mode operation will be available at t_{RAC} or t_{CAC} time, whichever is the limiting parameter. However, all successive accesses within the page mode operation will be available at t_{CAC} time (referenced to $\overline{CAS}$). With the MKB4516, this results in as much as a 45% improvement in access times! Effective memory cycle times are also reduced when using page mode.

The page mode boundary of a single MKB4516 is limited to the 128 column locations determined by all combinations of the seven column address bits. Operations within the page mode boundary need not be sequentially addressed and any combination of read-write and read-modify-write cycle are permitted within the page mode operation.

Refresh

Refresh of the dynamic cell matrix is accomplished by performing a memory cycle at all 128 combinations of the seven row address bits within each 2 ms interval. Although any normal memory cycle will perform the required refreshing, this function is most easily accomplished with "$\overline{RAS}$-only" cycles.

SUPPLEMENT

131,072 x 1-BIT DYNAMIC RAM MKM4528(D) - 83/84

FEATURES

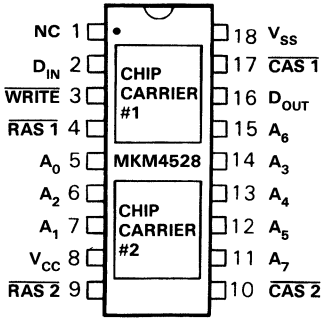
- Utilizes two standard MKB4564E devices in an 18-pin dual in-line package configuration
- -55°C to +110°C case operating temperature range
- Single +5 V (± 10%) supply operation
- Each MKB4564E Leadless Chip Carrier fully processed and burned in to MIL-STD-883 Method 5004 Class B
- Active power 325mW (Single MKB4564E active) Standby power 55mW
- 200ns access time, 345ns cycle time MKM4528D-83 250ns access time, 425ns cycle time MKM4528D-84
- Common I/O capability using "early write"
- Separate $\overline{RAS}$, $\overline{CAS}$ Clocks
- Read, Write, Read-Write, Read-Modify-Write and Page-Mode capability
- MKM Module electrically tested at maximum temperature following assembly
- Scaled POLY 5 technology
- 128 refresh cycles (2 msec) for each MKB4564 device in the dual density configuration (address A_7 is not used for refresh)
- Indefinite D_{OUT} hold using $\overline{CAS}$ control and unlatched at end of cycle to allow two dimensional chip selection and extended page boundary

DESCRIPTION

The MKM4528 sets a new milestone in the state of the art in package technology to give you dual density now before the next generation of MOS RAMs are available. This device is made up of two 64K (MKB4564E) 5 volt only RAMs and it is organized as 131,072 by 1 bit.

The high performance features of the MKM4528 are achieved by state-of-the-art circuit design techniques as well as utilization of Mostek's "Scaled POLY 5" process technology. Features include access times starting where the current generation 16K RAMs leave off, plus compatibility with the 128 refresh cycles of the previous generation.

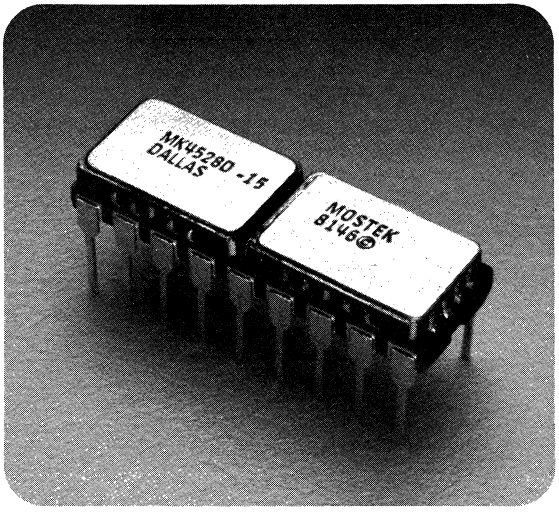
PIN CONNECTIONS



PIN FUNCITONS

A_0 - A_7	Address Inputs	$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe	$\overline{WRITE}$	Read/Write Input
D_{IN}	Data In	V_{CC}	Power (+5 V)
D_{OUT}	Data Out	NC	No Connect
V_{SS}	GND		

DEVICE PROFILE



XII

The completed MKM module is composed of individually processed and burned in devices which are then reflow soldered onto a cofired ceramic substrate. This inherently reliable assembly is then visually and electrically tested to confirm its quality.

The MKM4528 is capable of a variety of operations including READ, WRITE, READ-WRITE, READ-MODIFY-WRITE, PAGE MODE, and REFRESH. The output of the MKM4528 can be held valid indefinitely by holding $\overline{CAS}$ active low. This is quite useful since a refresh cycle can be performed while holding data valid from a previous cycle.

Multiplexed address inputs (a feature pioneered by Mostek for its 4K RAMs) permits the MKM4528 to be packaged in a standard 18-pin DIP. This standard package configuration, is compatible with widely available automated testing and insertion equipment, and it provides the highest possible system bit densities. Non-critical clock timing requirements allow use of the multiplexing technique while maintaining high performance. Device selection occurs through RAS decoding in the same manner as if the devices were independently placed in a memory matrix.

PRELIMINARY

PROCESSED TO MIL-STD-883, METHOD 5004, CLASS B, 65,536 x 1-BIT DYNAMIC RAM MKB4564 (P/E) - 82/83/84

FEATURES

- Military temperature range: $-55°C \leq T_C \leq +110°C$
- Dynamic burn in at 125°C for 160 hours
- Recognized industry standard 16-pin configuration from Mostek
- Single +5 V (± 10%) supply operation
- On chip substrate bias generator for optimum performance
- Typical ordering information

  MKB4564P-82 150 ns t_{RAC}
  MKB4564P-83 200 ns t_{RAC}
  MKB4564P-84 250 ns t_{RAC}

- Low power: 300 mW active, max
  22 mW standby, max
- Extended D_{OUT} hold using $\overline{CAS}$ control (Hidden Refresh)
- Common I/O capability using "early write"
- Read, Write, Read-Write, Read-Modify-Write and Page Mode capability
- All inputs TTL compatible, low capacitance, and protected against static charge
- Scaled POLY 5™ technology
- 128 refresh cycles (2 msec)
  Pin 9 is not needed for refresh

DESCRIPTION

The MKB4564 is the new generation dynamic RAM. Organized 65,536 words by 1 bit, it is the successor to the industry standard MKB4116. The MKB4564 utilizes Mostek's scaled POLY 5 process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user. The use of dynamic circuitry throughout, including the 512 sense amplifiers, assures that power dissipation is minimized without any sacrifice in speed or internal and external operating margins. Refresh characteristics have been chosen to maximize yield (low cost to user) while maintaining compatibility between dynamic RAM generations.

Multiplexed address inputs (a feature dating back to the industry standard MK4096, 1973) permit the MKB4564 to be packaged in a standard 16-pin DIP with only 15 pins required for basic functionality. The MKB4564 is designed to be compatible with the JEDEC standards for the 64K x 1 dynamic RAM.

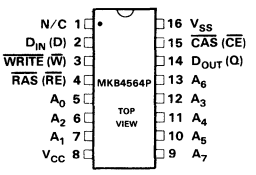
The output of the MKB4564 can be held valid up to 10 μsec by holding $\overline{CAS}$ active low. This is quite useful since refresh cycles can be performed while holding data valid from a previous cycle. This feature is referred to as Hidden Refresh.

The 64K RAM from Mostek is the culmination of several years of circuit and process development, proven in predecessor products.

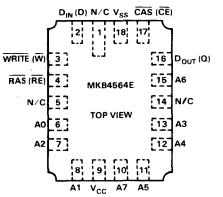
PIN OUT

Figure 1

DUAL-IN-LINE PACKAGE



LEADLESS CHIP CARRIER



PIN FUNCTIONS

Table 1

A_0-A_7	Address Inputs	$\overline{RAS}$ ($\overline{RE}$)	Row Address Strobe
$\overline{CAS}$ ($\overline{CE}$)	Column Address Strobe	$\overline{WRITE}$ ($\overline{W}$)	Read/Write Input
		V_{CC}	Power (5 V)
D_{IN} (D)	Data In	V_{SS}	GND
D_{OUT} (Q)	Data Out	N/C	Not Connected

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ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... 1.0 V to +7.0 V
Operating Temperature Tc (case) ..... -55°C to +110°C
Storage Temperature ..... -65°C to +150°C
Power Dissipation ..... 1 Watt
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

($-55°C \leq T_C \leq +110°C$)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	1
V_{IH}	Input High (Logic 1) Voltage, All Inputs	2.4	—	$V_{CC}+1$	V	1
V_{IL}	Input Low (Logic 0) Voltage, All inputs	-2.0	—	.8	V	1,16

DC ELECTRICAL CHARACTERISTICS

($-55°C \leq T_C \leq +110°C$) ($V_{CC}$ = 5.0 V ± 10%)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC1}	OPERATING CURRENT Average power supply operating current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = t_{RC} min.)		60.0	mA	2
I_{CC1}	OPERATING CURRENT (Tc = +110°C)		45	mA	2,18
I_{CC2}	STANDBY CURRENT Power supply standby current ($\overline{RAS}$ = V_{IH}, D_{OUT} = High Impedance)		5	mA	
I_{CC3}	RAS ONLY REFRESH CURRENT Average power supply current, refresh mode ($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH} ; t_{RC} = t_{RC} min.)		45	mA	2
I_{CC4}	PAGE MODE CURRENT Average power supply current, page mode operation ($\overline{RAS}$ = V_{IL} , t_{RAS} = t_{RAS} max., $\overline{CAS}$ cycling; t_{PC} = t_{PC} min.)		35	mA	2
$I_{I(L)}$	INPUT LEAKAGE Input leakage current, any input ($0 V \leq V_{IN} \leq V_{CC}$), all other pins not under test = 0 V	-10	10	µA	
$I_{O(L)}$	OUTPUT LEAKAGE Output leakage current (D_{OUT} is disabled, $0 V \leq V_{OUT} \leq V_{CC}$)	-10	10	µA	
V_{OH} V_{OL}	OUTPUT LEVELS Output High (Logic 1) voltage (I_{OUT} = -5 mA Output Low (Logic 0) voltage (I_{OUT} = 4.2 mA)	2.4	 0.4	V V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (3,4,5,15)
($-55°C \leq T_C \leq 110°C$), $V_{CC} = 5.0\ V \pm 10\%$

SYMBOL			MK4564-15		MK4564-20		MK4564-25			
STD	ALT	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
t_{RELREL}	t_{RC}	Random read or write cycle time	260		345		425		ns	6,7
t_{RELREL} (RMW)	t_{RMW}	Read-modify-write cycle time	310		405		490		ns	6,7
t_{RELREL} (PC)	t_{PC}	Page mode cycle time	155		200		240		ns	6,7
t_{RELQV}	t_{RAC}	Access time from $\overline{RAS}$		150		200		250	ns	7,8
t_{CELQV}	t_{CAC}	Access time from $\overline{CAS}$		85		115		145	ns	7,9
t_{CEHQZ}	t_{OFF}	Output buffer turn-off delay	0	40	0	50	0	60	ns	10
t_T	t_T	Transition time (rise and fall)	3	50	3	50	3	50	ns	5,15
t_{REHREL}	t_{RP}	$\overline{RAS}$ precharge time	100		135		165		ns	
t_{RELREH}	t_{RAS}	$\overline{RAS}$ pulse width	150	10,000	200	10,000	250	10,000	ns	
t_{CELREH}	t_{RSH}	$\overline{RAS}$ hold time	85		115		145		ns	
t_{RELCEH}	t_{CSH}	$\overline{CAS}$ hold time	150		200		250		ns	
t_{CELCEH}	t_{CAS}	$\overline{CAS}$ pulse width	85	10,000	115	10,000	145	10,000	ns	
t_{RELCEL}	t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ delay time	30	65	35	85	45	105	ns	11
t_{REHWX}	t_{RRH}	Read command hold time referenced to $\overline{RAS}$	20		25		30		ns	12
t_{AVREL}	t_{ASR}	Row address set-up time	0		0		0		ns	
t_{RELAX}	t_{RAH}	Row address hold time	20		25		30		ns	
t_{AVCEL}	t_{ASC}	Column address set-up time	0		0		0		ns	
t_{CELAX}	t_{CAH}	Column address hold time	30		40		50		ns	
$t_{RELA(C)X}$	t_{AR}	Column address hold time referenced to $\overline{RAS}$	100		130		160		ns	
t_{CELWX}	t_{RCH}	Read command hold time referenced to $\overline{CAS}$	0		0		0		ns	12
t_{CELWX}	t_{WCH}	Write command hold time	45		55		70		ns	
t_{RELWX}	t_{WCR}	Write command hold time referenced to $\overline{RAS}$	115		150		185		ns	
t_{WLWH}	t_{WP}	Write command pulse width	35		45		55		ns	
t_{WLREH}	t_{RWL}	Write command to $\overline{RAS}$ lead time	45		55		65		ns	
t_{WLCEH}	t_{CWL}	Write command to $\overline{CAS}$ lead time	45		55		65		ns	

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (3,4,5,15,)

($-55°C \leq T_C \leq 110°C$), $V_{CC} = 5.0\ V \pm 10\%$

SYMBOL		PARAMETER	MK4564-15		MK4564-20		MK4564-25		UNITS	NOTES
STD	ALT		MIN	MAX	MIN	MAX	MIN	MAX		
t_{DVCEL}	t_{DS}	Data-in set-up time	0		0		0		ns	13
t_{CELDX}	t_{DH}	Data-in hold time	45		55		70		ns	13
t_{RELDX}	t_{DHR}	Data-in hold time referenced to $\overline{RAS}$	115		150		190		ns	
t_{CEHCEL} (PC)	t_{CP}	$\overline{CAS}$ precharge time (for page-mode cycle only)	60		75		85		ns	
t_{RVRV}	t_{REF}	Refresh period		2		2		2	ms	
t_{WLCEL}	t_{WCS}	$\overline{WRITE}$ command set-up time	-10		-10		-10		ns	14
t_{CELWL}	t_{CWD}	$\overline{CAS}$ to $\overline{WRITE}$ delay	55		80		100		ns	14
t_{RELWL}	t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ delay	120		165		205		ns	14
t_{CEHCEL}	t_{CPN}	$\overline{CAS}$ precharge time	30		35		45		ns	

AC ELECTRICAL CHARACTERISTICS

($-55°C \leq T_C \leq 110°C$) = $5.0\ V \pm 10\%$

SYM	PARAMETER	MAX	UNITS	NOTES
C_{I1}	Input Capacitance (A_0 - A_7), D_{IN}	5	pF	14
C_{I2}	Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	10	pF	14
C_O	Output Capacitance (D_{OUT})	7	pF	14

NOTES:

1. All voltages referenced to V_{SS}.
2. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open.
3. An initial pause of 500 μs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved. Note that $\overline{RAS}$ may be cycled during the initial pause.
4. V_{IH} min. and V_{IL} max. are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
5. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($-55°C \leq T_C \leq 110°C$) is assured.
6. Assumes that $t_{RCD} \leq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
7. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
8. t_{OFF} max. defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
9. Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} limit, then access time is controlled exclusively by t_{CAC}.
10. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
11. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in delayed or read-modify-write cycles.
12. t_{WCS}, t_{CWD}, and t_{RWD} are restrictive operating parameters in READ/WRITE and READ/MODIFY/WRITE cycles only. If $t_{WCS} \geq t_{WCS}$ (min) the cycle is an EARLY WRITE cycle and the data output will remain open circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min) the cycle is a READ/WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met the condition of the data out (at access time and until $\overline{CAS}$ goes back to V_{IH}) is indeterminate.
13. In addition to meeting the transition rate specification, all input signals must transmit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
14. Effective capacitance calculated from the equation $C = I\frac{\Delta t}{\Delta V}$ with $\Delta V = 3$ volts and power supply is at nominal level. This parameter is sample tested only.
15. CAS = V_{IH} to disable D_{OUT}.
16. Includes the DC level and all instantaneous signals excursions.
17. $\overline{WRITE}$ = don't care. Data out depends on the state of $\overline{CAS}$. If $\overline{CAS} = V_{IH}$, data output is high impedance. If $\overline{CAS} = V_{IL}$, the data output will contain data from the last valid read cycle.
18. Power consumption decreases with increasing temperature.

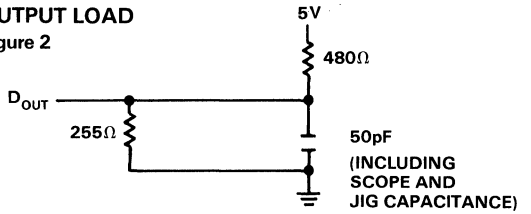
AC TEST CONDITIONS

Table 2

Input Levels	0 to 3.0 V
Transistion Times	5 ns
Input timing reference levels	1.5 V
Output timing reference levels	0.8 V - 2.0 V
Output Load	See figure

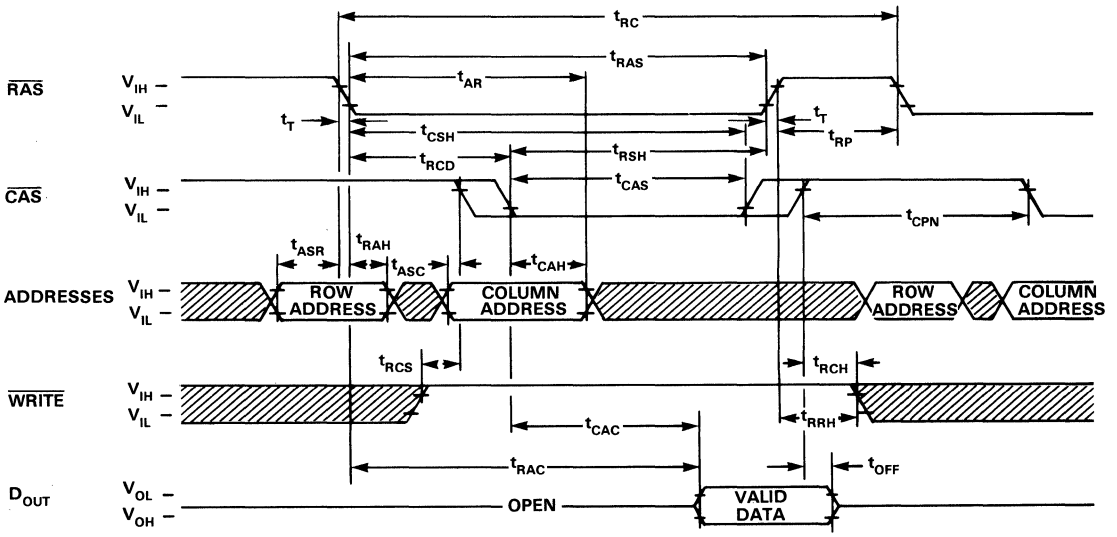
OUTPUT LOAD

Figure 2



READ CYCLE

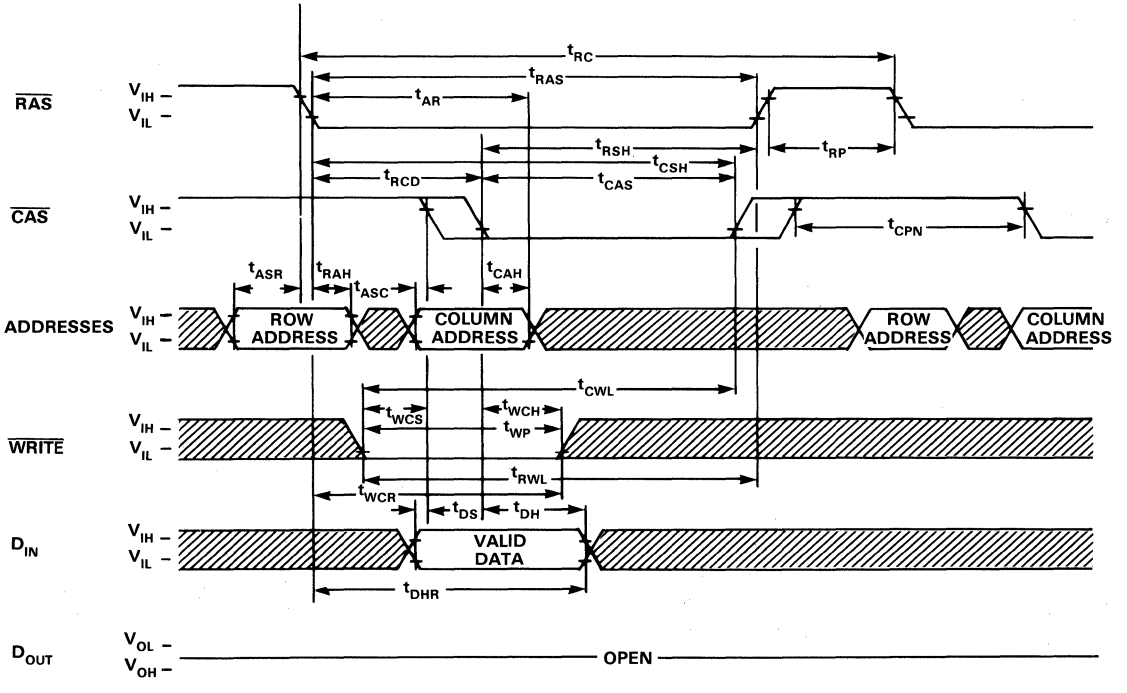
Figure 4



XII

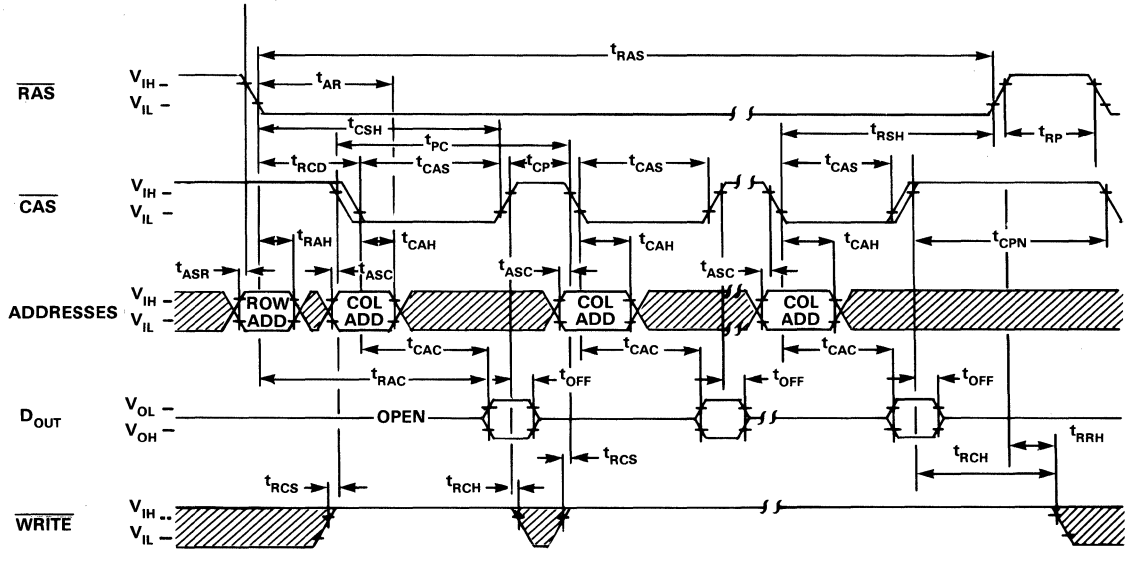
WRITE CYCLE (EARLY WRITE)

Figure 5



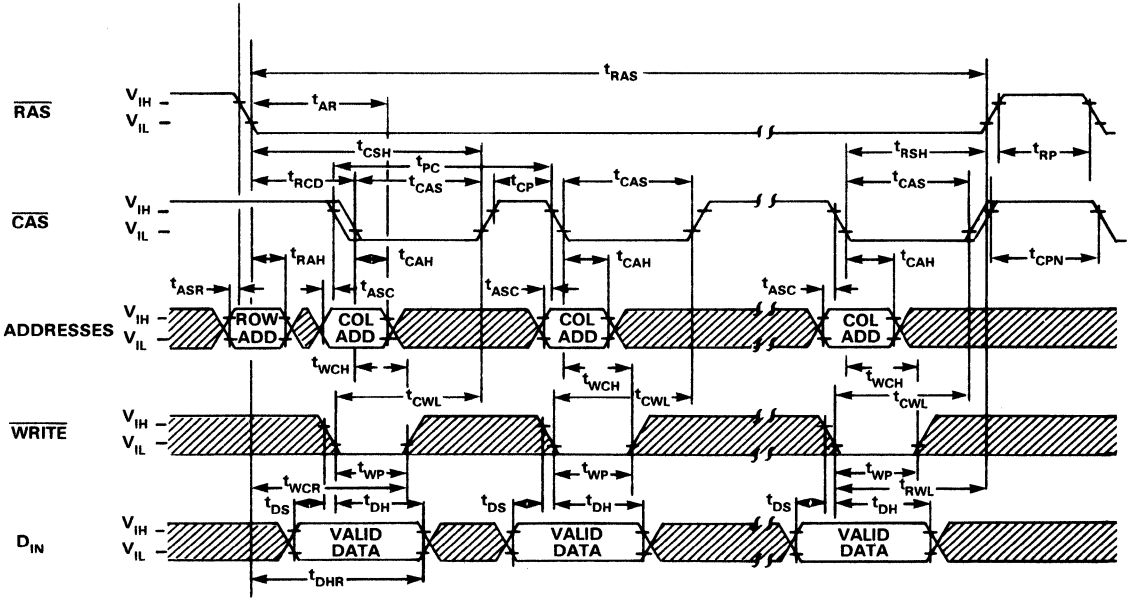
PAGE MODE READ CYCLE

Figure 6



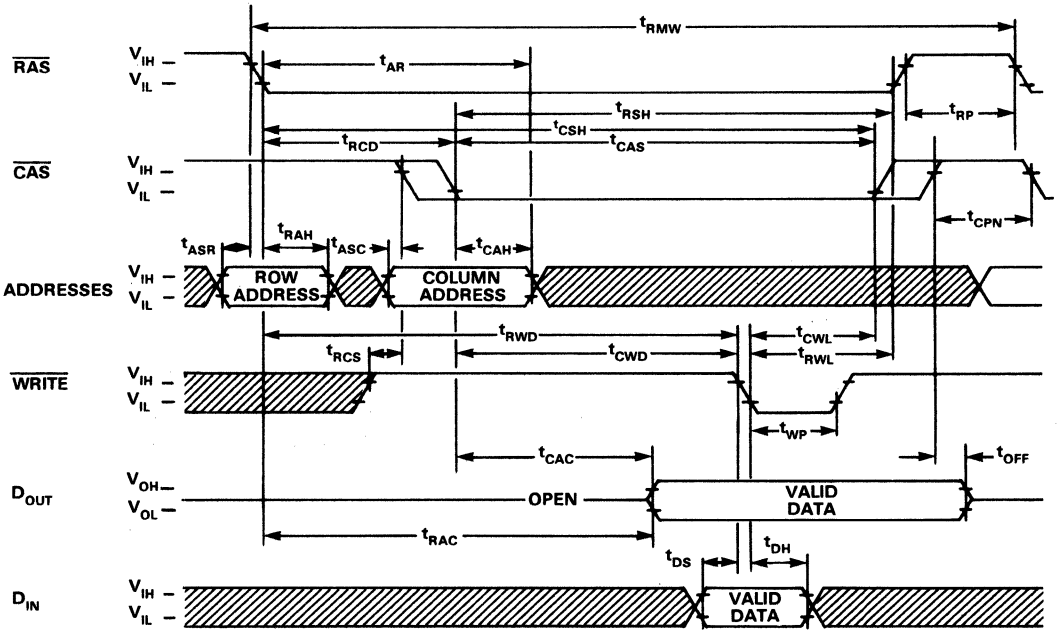
PAGE MODE WRITE CYCLE

Figure 7



READ-WRITE/READ-MODIFY-WRITE CYCLE

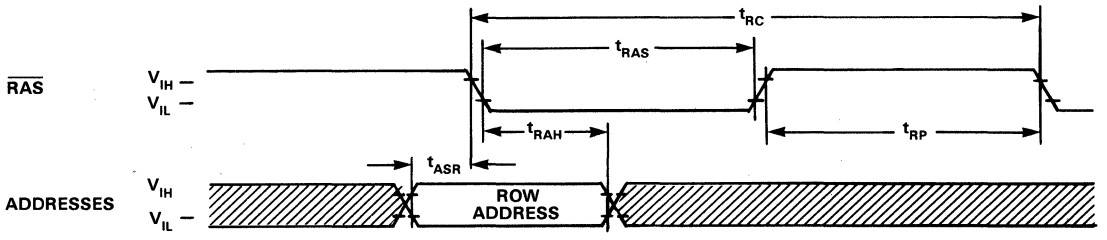
Figure 8



XII

"$\overline{RAS}$-ONLY" REFRESH CYCLE

Figure 9



OPERATION

The eight address bits required to decode 1 of the 65,536 cell locations within the MKB4564 are multiplexed onto the eight address inputs and latched into the on-chip address latches by externally applying two negative going TTL-level clocks. The first clock, Row Address Strobe ($\overline{RAS}$), latches the eight row addresses into the chip. The high-to-low transition of the second clock, Column Address Strobe ($\overline{CAS}$), subsequently latches the eight column addresses into the chip. Each of these signals, $\overline{RAS}$ and $\overline{CAS}$, triggers a sequence of events which are controlled by different delayed internal clocks. The two clock chains are linked together logically in such a way that the address multiplexing operation is done outside of the critical timing path for read data access. The later events in the $\overline{CAS}$ clock sequence are inhibited until the occurrence of a delayed signal derived from the $\overline{RAS}$ clock chain. This "gated $\overline{CAS}$" feature allows the $\overline{CAS}$ clock to be externally activated as soon as the Row Address Hold specification (t_{RAH}) has been satisfied and the address inputs have been changed from Row address to Column address information.

The "gated $\overline{CAS}$" feature permits $\overline{CAS}$ to be activated at any time after t_{RAH} and it will have no effect on the worst case data access time (t_{RAC}) up to the point in time when the dalayed row clock no longer inhibits the remaining sequence of column clocks. Two timing endpoints result from the internal gating of $\overline{CAS}$ which are called t_{RCD} (min) and t_{RCD} (max). No data storage or reading errors will result if $\overline{CAS}$ is applied to the MKB4564 at a point in time beyond the t_{RCD} (max) limit. However, access time will then be determined exclusively by the access time from $\overline{CAS}$ (t_{CAC}) rather than from $\overline{RAS}$ (t_{RAC}), and $\overline{RAS}$ access time will be lengthened by the amount that t_{RCD} exceeds the t_{RCD} (max) limit.

DATA INPUT/OUTPUT

Data to be written into a selected cell is latched into an on-chip register by a combination of $\overline{WRITE}$ and $\overline{CAS}$ while $\overline{RAS}$ is active. The latter of $\overline{WRITE}$ or $\overline{CAS}$ to make its negative transition is the strobe for the Data In (D_{IN}) register. This permits several options in the write cycle timing. In a write cycle, if the $\overline{WRITE}$ input is brought low (active) prior to $\overline{CAS}$ being brought low (active), the D_{IN} is strobed by $\overline{CAS}$, and the Input Data set-up and hold times are referenced to $\overline{CAS}$. If the input data is not available at $\overline{CAS}$ time (late write) or if it is desired that the cycle be a read-write or read-modify-write cycle the $\overline{WRITE}$ signal should be delayed until after $\overline{CAS}$ has made its negative transition. In this "delayed write cycle" the data input set-up and hold times are referenced to the negative edge of $\overline{WRITE}$ rather than $\overline{CAS}$.

Data is retrieved from the memory in a read cycle by maintaining $\overline{WRITE}$ in the inactive or high state throughout the portion of the memory cycle in which both the $\overline{RAS}$ and $\overline{CAS}$ are low (active). Data read from the selected cell is available at the output port within the specified access time. The output data is the same polarity (not inverted) as the input data.

DATA OUTPUT CONTROL

The normal condition of the Data Output (D_{OUT}) of the MKB4564 is the high impedance (open-circuit) state; anytime $\overline{CAS}$ is high (inactive) the D_{OUT} pin will be floating. Once the output data port has gone active, it will remain valid until $\overline{CAS}$ is taken to the precharge (inactive high) state.

PAGE MODE OPERATION

The Page Mode feature of the MKB4564 allows for the successive memory operations at multiple column locations within the same row address. This is done by strobing the row address into the chip and maintaining the $\overline{RAS}$ signal low (active) throughout all successive memory cycles in which the row address is common. The first access within a page mode operation will be available at t_{RAC} or t_{CAC} time, whichever is the limiting parameter. However, all successive accesses within the page mode operation will be available at t_{CAC} time (referenced to $\overline{CAS}$). With the MKB4564 this results in approximately a 45% improvement in access times. Effective memory cycle times are also reduced when using page mode.

The page mode boundary of a single MKB4564 is limited to the 256 column locations determined by all combinations of the eight column address bits. Operations within the page boundary need not be sequentially addressed and any combination of read, write, and read-modify-write cycles is permitted within the page mode operation.

REFRESH

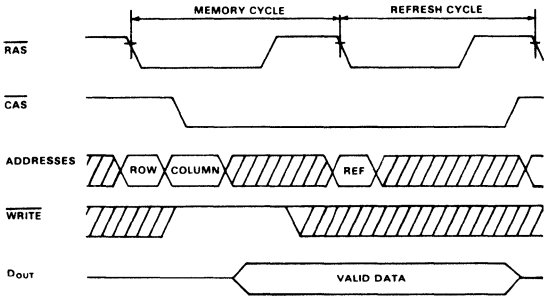
Refresh of the dynamic cell matrix is accomplished by performing a memory cycle at each of the 128 row addresses within each 2ms interval. Although any normal memory cycle will perform the required refreshing, this function is most easily accomplished with "$\overline{RAS}$-only" cycles.

The $\overline{RAS}$-only refresh cycle requires that a 7 bit refresh address (A0-A6) be valid at the device address inputs when $\overline{RAS}$ goes low (active). The state of the output data port during a $\overline{RAS}$-only refresh is controlled by $\overline{CAS}$. If $\overline{CAS}$ is high (inactive) during the entire time that $\overline{RAS}$ is asserted, the output will remain in the high impedance state. If $\overline{CAS}$ is low (active) the entire time that $\overline{RAS}$ is asserted, the output port will remain in the same state that it was prior to the issuance of the $\overline{RAS}$ signal. If $\overline{CAS}$ makes a low-to-high transition during the $\overline{RAS}$-only refresh cycle, the output data buffer will assume the high impedance state. However, $\overline{CAS}$ may not make a high to low transition during the $\overline{RAS}$-only refresh cycle since the device interprets this as a normal $\overline{RAS}/\overline{CAS}$ (read or write) type cycle.

HIDDEN REFRESH

A $\overline{RAS}$-only refresh cycle may take place while maintaining valid output data by extending the $\overline{CAS}$ active time from a previous memory read cycle. This feature is referred to as a hidden refresh. (See figure below.)

HIDDEN REFRESH CYCLE (SEE NOTE 19)
Figure 10



XII

MOSTEK®

MILITARY/HIGH-REL PRODUCTS

PROCESSED TO MIL-STD 883, METHOD 5004, CLASS B

1024 x 8-Bit Static RAM

MKB4801A(P/J/E)-870/890/81

FEATURES

- ☐ Static operation
- ☐ Organization: 1K x 8 bit RAM JEDEC pinout
- ☐ Pin compatible with Mostek's BYTEWYDE™ memory family
- ☐ 24/28 pin ROM/PROM compatible pin configuration
- ☐ $\overline{CE}$ and $\overline{OE}$ functions facilitate bus control
- ☐ –55°C to 125°C operating temperature
- ☐ High performance

Part No.	Access Time	R/W Cycle Time
MKB4801A-870	70 nsec	70/80 nsec
MKB4801A-890	90 nsec	90/100 nsec
MKB4801A-81	120 nsec	120 nsec

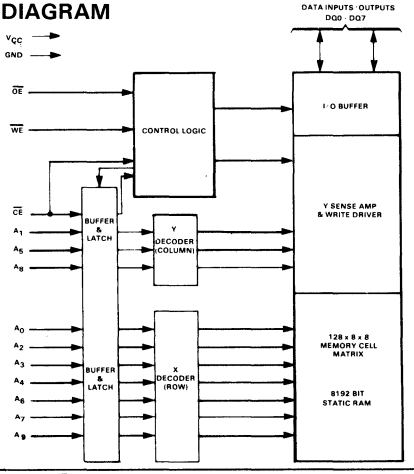
DESCRIPTION

The MKB4801A uses Mostek's Scaled POLY 5™ process and advanced circuit design techniques to package 8,192 bits of static RAM on a single chip. Static operation is achieved with high performance and low power dissipation by utilizing Address Activated™ circuit design techniques.

The MKB4801A excels in high speed memory applications where the organization requires relatively shallow depth with a wide word format. The MKB4801A presents the user a high density cost effective alternative to bipolar and previous generation N-MOS fast memory.

BLOCK DIAGRAM

Figure 1



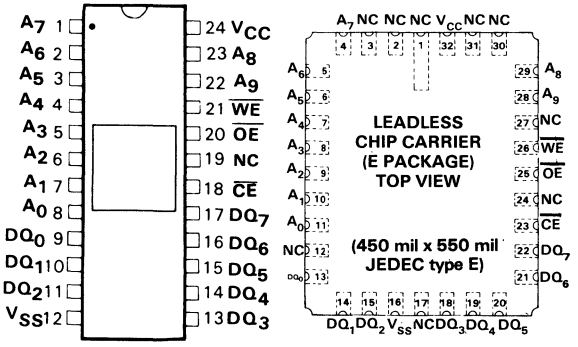
TRUTH TABLE

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	DQ
V_{IH}	X	X	Deselect	High Z
V_{IL}	X	V_{IL}	Write	D_{IN}
V_{IL}	V_{IL}	V_{IH}	Read	D_{OUT}
V_{IL}	V_{IH}	V_{IH}	Read	High Z

X = Don't Care

PIN CONNECTIONS

Figure 2



PIN NAMES

A_0-A_9	Address Inputs	$\overline{WE}$	Write Enable
$\overline{CE}$	Chip Enable	$\overline{OE}$	Output Enable
V_{SS}	Ground	NC	No Connection
V_{CC}	Power (+5 V)	DQ_0-DQ_7	Data In/Data Out

XII

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to V_{SS} ..... -0.3 V to +7.0 V
Operating Temperature T_A (Ambient) ..... -55°C to +125°C
Storage Temperature (Ambient) (Ceramic) ..... -65°C to +150°C
Power Dissipaion ..... 1 Watt
Output Current ..... 20 mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS[8]

(-55°C ≤ T_A ≤ +125°C)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.75	5.0	5.25	V	1
V_{SS}	Supply Voltage	0	0	0	V	1
V_{IH}	Logic "1" Voltage All Inputs	2.4		7.0	V	1
V_{IL}	Logic "0" Voltage All Inputs	-0.3		.65	V	1, 10

DC ELECTRICAL CHARACTERISTICS[1,8]

(-55°C ≤ T_A ≤ +125°C) (V_{CC} = 5.0 volts ±5%)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC1}	Average V_{CC} Power Supply Current		120	mA	9
I_{CC1}	Average V_{CC} Power Supply Current (T_A = 125°C)		90	mA	9, 11
I_{IL}	Input Leakage Current (Any Input)	-10	10	μA	2
I_{OL}	Output Leakage Current	-50	50	μA	2
V_{OH}	Output Logic "1" Voltage I_{OUT} = -1 mA	2.4		V	
V_{OL}	Output Logic "0" Voltage I_{OUT} = 4 mA		0.4	V	

AC ELECTRICAL CHARACTERISTICS[3,4]

(−55°C ≤ T_A ≤ 125°C) (V_{CC} = 5.0 volts ± 5%)

SYM	PARAMETER	MKB4801A-870		MKB4801A-890		MKB4801A-81		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX		
t_{RC}	Read Cycle Time	70		90		120		ns	
t_{AA}	Address Access Time		70		90		120	ns	5
t_{CEA}	Chip Enable Access Time		35		45		60	ns	5
t_{CEZ}	Chip Enable Data Off Time	5	20	5	30	5	30	ns	
t_{OEA}	Output Enable Access Time		35		45		60	ns	5
t_{OEZ}	Output Enable Data Off Time	5	20	5	30	5	30	ns	
t_{AZ}	Address Data Off Time	10		10		10		ns	
t_{WC}	Write Cycle Time	80		100		120		ns	
t_{AS}	Address Setup Time	0		0		0		ns	see text
t_{AH}	Address Hold Time	20		30		40		ns	see text
t_{DSW}	Data To Write Setup Time	5		5		10		ns	
t_{DHW}	Data From Write Hold Time	10		10		15		ns	
t_{WD}	Write Pulse Duration	30		40		45		ns	see text
t_{WEZ}	Write Enable Data Off Time	5	15	5	25	5	30	ns	
t_{WPL}	Write Pulse Lead Time	50		60		75		ns	

CAPACITANCE[1,8]

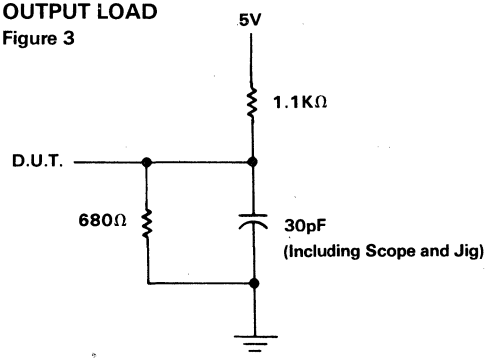
(−55°C ≤ T_A ≤ +125°C) (V_{CC} = +5.0 volts ± 5%)

SYM	PARAMETER	TYP	MAX	NOTES
C_I	All pins (except D/Q)	4 pF		6
$C_{D/Q}$	D/Q pins	10 pF		6,7

NOTES:

1. All voltages referenced to V_{SS}.
2. Measured with .4 ≤ V_I ≤ 5.0 V, outputs deselected and V_{CC} = 5 V.
3. AC measurements assume Transition Time = 5 ns; levels V_{SS} to 3.0 V.
4. Input and output timing reference levels are at 1.5 V.
5. Measured with a load as shown in Figure 3.
6. Effective capacitance calculated from the equation $C = \frac{\Delta Q}{\Delta V}$ with ΔV = 3 volts and power supplies at nominal levels.
7. Output buffer is deselected.
8. A minimum of 2 ms time delay is required after application of V_{CC} (+5 V) before proper device operation can be achieved.
9. I_{CC1} measured with outputs open.
10. Negative undershoots to a minimum of −1.5 V are allowed with a maximum of 50 ns pulse width. DC value of low level input must not exceed −0.3 V.
11. Power supply current decreases with increasing temperature.

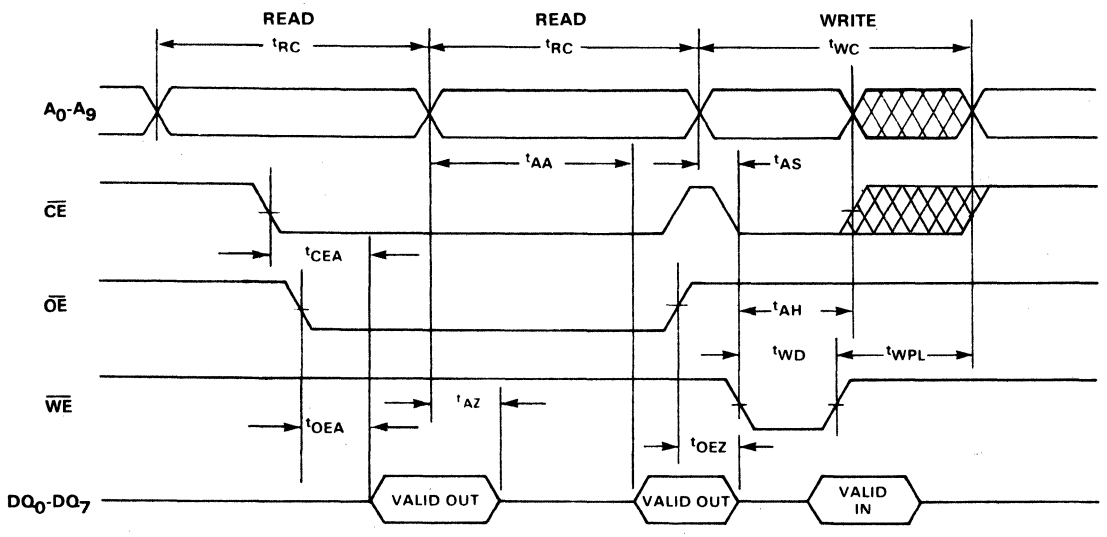
OUTPUT LOAD
Figure 3



XII

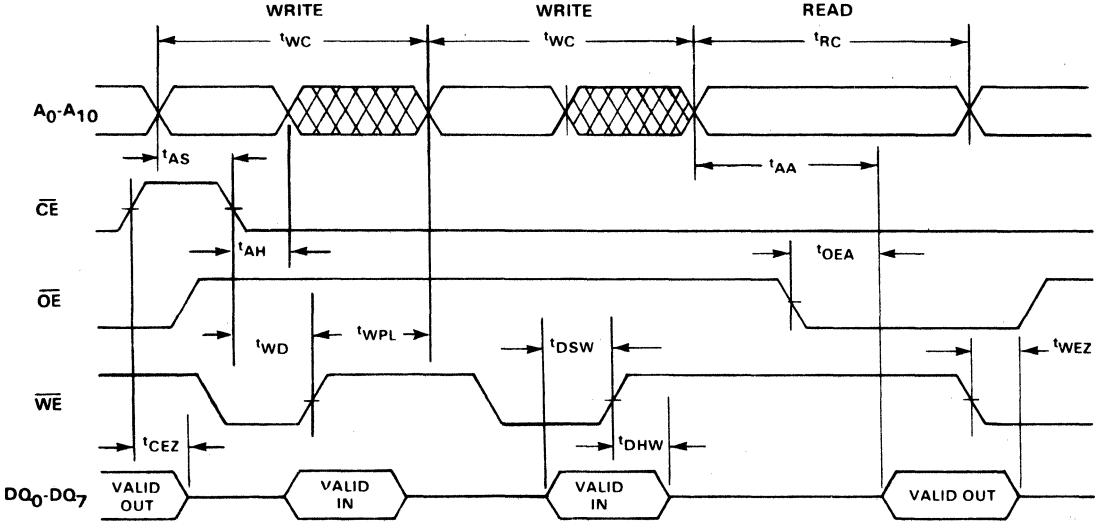
TIMING DIAGRAM

Figure 4



TIMING DIAGRAM

Figure 5



DESCRIPTION (Cont.)

The MKB4801A features a fast $\overline{CE}$ (50% of Address Access) function to permit memory expansion without impacting system access time. A fast $\overline{OE}$ (50% of access time) is included to permit data interleaving for enhanced system performance.

The MKB4801A is pin compatible with Mostek's BYTEWYDE™ memory family of RAMs, ROMs and EPROMs.

OPERATION

Read Mode

The MKB4801A is in the READ MODE whenever the Write Enable Control input ($\overline{WE}$) is in the high state.

In the READ mode of operation, the MKB4801A provides a fast address ripple-through access of data from 8 of 8192 locations in the static storage array. Thus, the unique address specified by the 10 Address Inputs (An) define which 1 of 1024 bytes of data is to be accessed.

A transition on any of the 10 address inputs will disable the 8 Data Output Drivers after t_{AZ}. Valid Data will be available to the 8 Data Output Drivers within t_{AA} after the last address input signal is stable, providing that the $\overline{CE}$ and $\overline{OE}$ access times are satisfied. If $\overline{CE}$ or $\overline{OE}$ access times are not met, data access will be measured from the limiting parameter (t_{CEA} or t_{OEA}) rather than the address. The state of the 8 data I/O signals is controlled by the Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) control signals.

Write Mode

The MKB4801A is in the Write Mode whenever the Write Enable ($\overline{WE}$) and Chip Enable ($\overline{CE}$) control inputs are in the low state.

The WRITE cycle is initiated by the $\overline{WE}$ pulse going low provided that $\overline{CE}$ is also low. The leading edge of the $\overline{WE}$ pulse is used to latch the status of the address bus.

NOTE: In a write cycle the latter occurring edge of either $\overline{WE}$ or $\overline{CE}$ will determine the start of the write cycle. Therefore, t_{AS}, t_{WD} and t_{AH} are referenced to the latter occurring edge of $\overline{CE}$ or $\overline{WE}$. Addresses are latched at this time. All write cycles whether initiated by $\overline{CE}$ or $\overline{WE}$ must be terminated by the rising edge of $\overline{WE}$. If the output bus has been enabled ($\overline{CE}$ and $\overline{OE}$ low) then $\overline{WE}$ will cause the output to go to the high Z state in t_{WEZ}.

Data In must be valid t_{DSW} prior to the low to high transition of $\overline{WE}$. The Data In lines must remain stable for t_{DHW} after $\overline{WE}$ goes inactive. The write control of the MKB4801A disables the data out buffers during the write cycle; however, $\overline{OE}$ should be used to disable the data out buffers to prevent bus contention between the input data and data that would be output upon completion of the write cycle.

MOSTEK®

MILITARY/HIGH-REL PRODUCTS

PROCESSED TO MIL-STD 883, METHOD 5004, CLASS B

2048 x 8 Bit Static RAM

MKB4802(P/J/E)-81/83

FEATURES

- ☐ Static operation
- ☐ Organization: 2K x 8 bit RAM JEDEC pinout
- ☐ Pin compatible with Mostek's BYTEWYDE™ memory family
- ☐ Double density version of the MKB4118 1K x 8 static RAM
- ☐ 24/28 pin ROM/PROM compatible pin configuration
- ☐ $\overline{CE}$ and $\overline{OE}$ functions facilitate bus control
- ☐ –55°C to 125°C operating temperature
- ☐ High performance

Part No.	Access Time	R/W Cycle Time
MKB4802-81	120 nsec	120 nsec
MKB4802-83	200 nsec	200 nsec

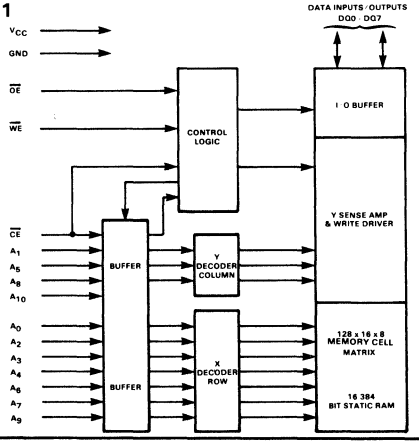
DESCRIPTION

The MKB4802 uses Mostek's Scaled POLY 5™ process and advanced circuit design techniques to package 16,384 bits of static RAM on a single chip. Static operation is achieved with high performance and low power dissipation by utilizing Address Activated™ circuit design techniques.

The MKB4802 series presents to the user a high density cost effective N-MOS memory with the performance charac-

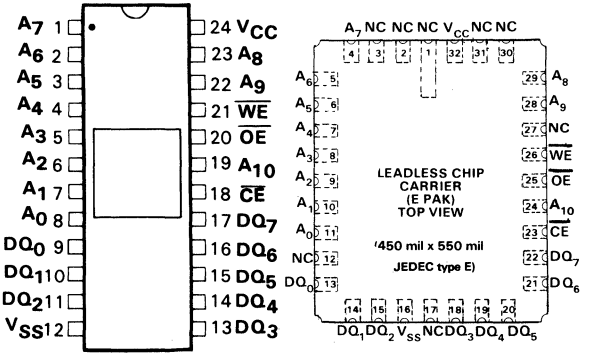
BLOCK DIAGRAM

Figure 1



PIN CONNECTIONS

Figure 2



TRUTH TABLE

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	DQ
V_{IH}	X	X	Deselect	High Z
V_{IL}	X	V_{IL}	Write	D_{IN}
V_{IL}	V_{IL}	V_{IH}	Read	D_{OUT}
V_{IL}	V_{IH}	V_{IH}	Read	High Z

X = Don't Care

PIN NAMES

A_0-A_{10}	Address Inputs	V_{CC}	Power (+5 V)
$\overline{CE}$	Chip Enable	$\overline{WE}$	Write Enable
V_{SS}	Ground	$\overline{OE}$	Output Enable
DQ_0-DQ_7	Data In/Data Out		

XII

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to V_{SS} ..... -0.5 V to +7.0 V
Operating Temperature T_A (Ambient) ..... -55°C to +125°C
Storage Temperature (Ambient) ..... -65°C to +150°C
Power Dissipation ..... 1 Watt
Output Current ..... 20 mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED D.C. OPERATING CONDITIONS[8]

(-55°C ≤ T_A ≤ +125°C)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.75	5.0	5.25	V	1
V_{SS}	Supply Voltage	0	0	0	V	1
V_{IH}	Logic "1" Voltage All Inputs	2.4		V_{CC} + .5 V	V	1
V_{IL}	Logic "0" Voltage All Inputs	-0.3		.65	V	1,10

DC ELECTRICAL CHARACTERISTICS[1,8]

(-55°C ≤ T_A ≤ +125°C) (V_{CC} = 5.0 volts ± 5%)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC1}	Average V_{CC} Power Supply Current		120	mA	9
I_{CC1}	Average V_{CC} Power Supply Current (T_A = 125°C)		90	mA	9, 11
I_{IL}	Input Leakage Current (Any Input)	-10	10	μA	2
I_{OL}	Output Leakage Current	-10	10	μA	2
V_{OH}	Output Logic "1" Voltage I_{OUT} = -1 mA	2.4		V	
V_{OL}	Output Logic "0" Voltage I_{OUT} = 4 mA		0.4	V	

AC ELECTRICAL CHARACTERISTICS[1,8]

(-55°C ≤ T_A ≤ +125°C) (V_{CC} = +5.0 volts ± 5%)

SYM	PARAMETER	TYP	MAX	NOTES
C_I	Capacitance on all pins (except D/Q)	4 pF		6
$C_{D/Q}$	Capacitance on D/Q pins	10 pF		6,7

ELECTRICAL CHARACTERISTICS[3,4]

($-55°C \leq T_A \leq +125°C$) ($V_{CC}$ = 5.0 volts ± 5%)

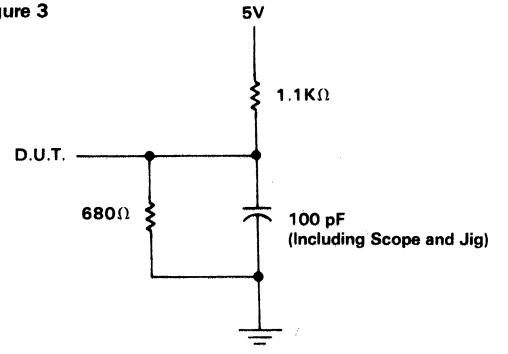
SYM	PARAMETER	MKB4802-81		MKB4802-83		UNITS	NOTES
		MIN	MAX	MIN	MAX		
t_{RC}	Read Cycle Time	120		200		ns	
t_{AA}	Address Access Time		120		200	ns	5
t_{CEA}	Chip Enable Access Time		60		100	ns	5
t_{CEZ}	Chip Enable Data Off Time	5	35	5	35	ns	
t_{OEA}	Output Enable Access Time		60		100	ns	5
t_{OEZ}	Output Enable Data Off Time	5	35	5	35	ns	
t_{AZ}	Address Data Off Time	10		10		ns	
t_{WC}	Write Cycle Time	120		200		ns	
t_{AS}	Address Setup Time	0		0		ns	see text
t_{AH}	Address Hold Time	40		65		ns	see text
t_{DSW}	Data To Write Setup Time	10		20		ns	
t_{DHW}	Data From Write Hold Time	10		10		ns	
t_{WD}	Write Pulse Duration	45		60		ns	see text
t_{WEZ}	Write Enable Data Off Time	5	35	5	35	ns	
t_{WPL}	Write Pulse Lead Time	65		130		ns	

NOTES:

1. All voltages referenced to V_{SS}.
2. Measured with $.4 \leq V_I \leq 5.0$ V, outputs deselected and V_{CC} = 5 V.
3. AC measurements assume Transition Time = 5 ns; levels V_{SS} to 3.0 V.
4. Input and output timing reference levels are at 1.5 V.
5. Measured with a load as shown in Figure 3.
6. Effective capacitance calculated from the equation $C = \frac{\Delta Q}{\Delta V}$ with ΔV = 3 volts and power supplies at nominal levels.
7. Output buffer is deselected.
8. A minimum of 2 ms time delay is required after application of V_{CC} (+5 V) before proper device operation can be achieved.
9. I_{CC1} measured with outputs open.
10. Negative undershoots to a minimum of -1.5 V are allowed with a maximum of 50 ns pulse width. DC value of low level input must not exceed -0.3 V.
11. Power supply current decreases with increasing temperature.

OUTPUT LOAD

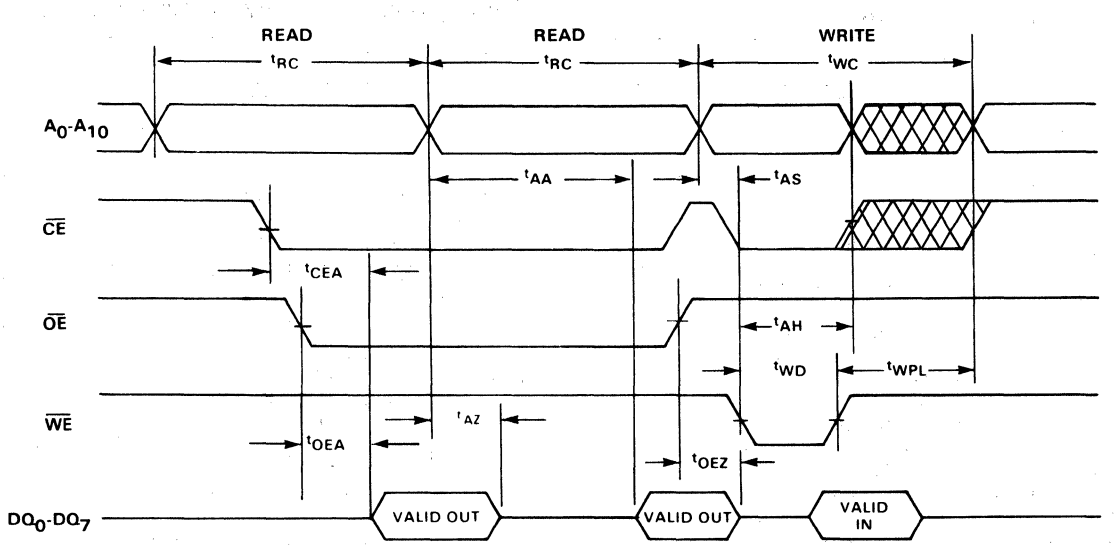
Figure 3



XII

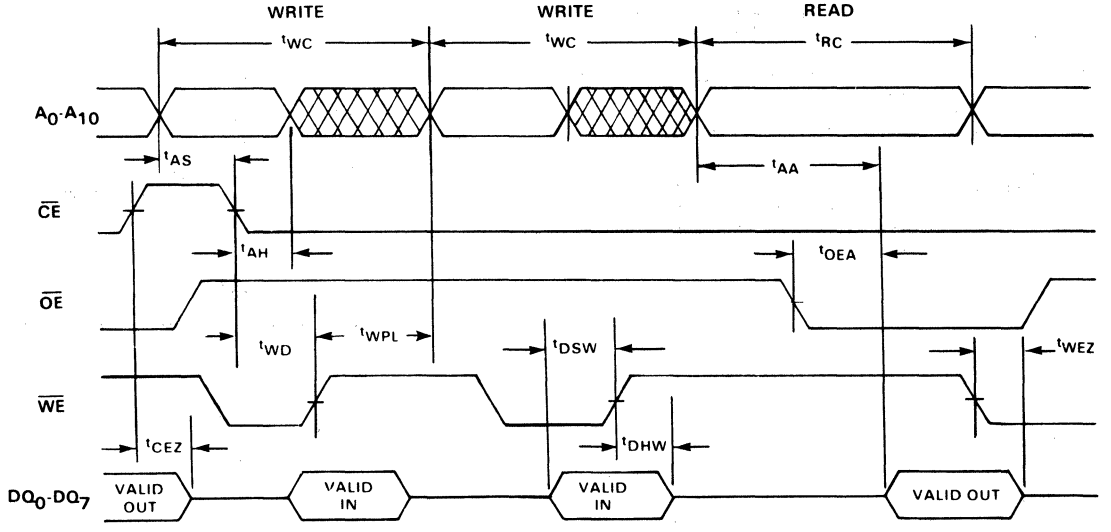
TIMING DIAGRAM

Figure 4



TIMING DIAGRAM

Figure 5



teristics necessary for today's high performance microprocessor applications. The MKB4802 is ideal for memory applications where the organization requires relatively shallow depth with a wide word format.

The MKB4802 features a fast $\overline{CE}$ (50% of Address Access) function to permit memory expansion without impacting system access time. A fast $\overline{OE}$ (50% of access time) is included to permit data interleaving for enhanced system performance.

The MKB4802 is pin compatible with Mostek's BYTEWYDE™ Memory Family of RAMs, ROMs and EPROMs.

OPERATION

READ MODE

The MKB4802 is in the READ MODE whenever the Write Enable Control Input ($\overline{WE}$) is in the high state. In the READ mode of operation, the MKB4802 provides a fast address ripple-through access of data from 8 of 16,384 locations in the static storage array. Thus, the unique address specified by the 11 Address Inputs (A_n) define which 1 of 2048 bytes of data is to be accessed.

A transition on any of the 11 address inputs will disable the 8 Data Output Drivers after t_{AZ}. Valid Data will be available to the 8 Data Output Drivers within t_{AA} after the last address input signal is stable, providing that the $\overline{CE}$ and $\overline{OE}$ access time are satisfied. If $\overline{CE}$ or $\overline{OE}$ access times are not met, data access will be measured from the limiting parameter (t_{CEA} or t_{OEA}) rather than the address. The state of the 8 data I/O signals is controlled by the Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) control signals.

WRITE MODE

The MKB4802 is in the Write Mode whenever the Write Enable ($\overline{WE}$) and Chip Enable ($\overline{CE}$) control inputs are in the low state.

The WRITE cycle is initiated by the $\overline{WE}$ pulse going low provided that $\overline{CE}$ is also low. The leading edge of the $\overline{WE}$ pulse is used to latch the status of the address bus.

NOTE: In a write cycle the latter occurring edge of either $\overline{WE}$ or $\overline{CE}$ will determine the start of the write cycle. Therefore, t_{AS}, t_{WD} and t_{AH} are referenced to the latter occurring edge of $\overline{CE}$ or $\overline{WE}$. Addresses are latched at this time. All write cycles whether initiated by $\overline{CE}$ or $\overline{WE}$ must be terminated by the rising edge of $\overline{WE}$. If the output bus has been enabled ($\overline{CE}$ and $\overline{OE}$ low) the $\overline{WE}$ will cause the output to go to the high Z state in t_{WEZ}.

Data In must be valid t_{DSW} prior to the low to high transition of $\overline{WE}$. The Data In lines must remain stable for t_{DHW} after $\overline{WE}$ goes inactive. The write control of the MKB4802 disables the data out buffers during the write cycle; however, $\overline{OE}$ should be used to disable the data out buffers to prevent bus contention between the input data and data that would be output upon completion of the write cycle.

1982/1983 MICROELECTRONIC DATA BOOK

MOSTEK

Z80 CENTRAL PROCESSING UNIT

Processed to MIL-STD 883, Method 5004, Class B

MKB3880(P)-80/84

FEATURES

- ☐ Screened per MIL-STD-883, Method 5004 Class B
- ☐ –55°C to 125°C temperature range
- ☐ Two speeds
  - 2.5 MHz MKB3880)P)-80
  - 4.0 MHz MKB3880(P)-84
- ☐ Single 5-Volt supply and single-phase clock required
- ☐ Z80 CPU and Z80 A CPU
- ☐ Software compatible with 8080A CPU
- ☐ Complete development and OEM system product support
- ☐ Industrial MKI version available (-40°C to 85°C)

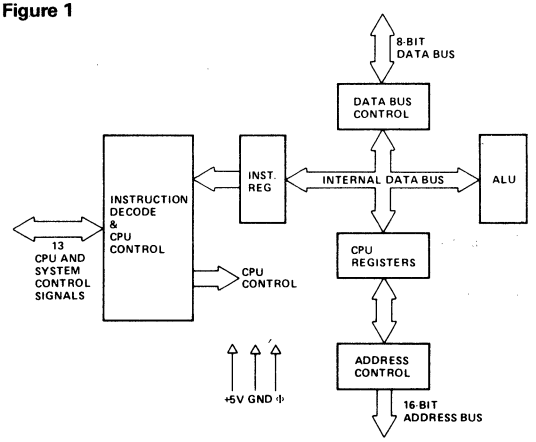
DESCRIPTION

The Mostek Z80 family of components is a significant advancement in the state-of-art of microcomputers. These components can be configured with any type of standard semiconductor memory to generate computer systems with an extremely wide range of capabilities. For example, as few as two LSI circuits and three standard TTL MSI packages can be combined to form a simple controller. With additional memory and I/O devices, a computer can be constructed with capabilities that only a minicomputer could deliver previously. This wide range of computational power allows standard modules to be constructed by a user that can satisfy the requirements of an extremely wide range of applications.

The CPU is the heart of the system. Its function is to obtain instructions from the memory and perform the desired operations. The memory is used to contain instructions and, in most cases, data that is to be processed. For example, a typical instruction sequence may be to read data from a specific peripheral device, store it in a location in memory, check the parity, and write it out to another peripheral device. Note that the Mostek component set includes the CPU and various general purpose I/O device controllers, as well as a wide range of memory devices. Thus, all required components can be connected together in a very simple manner with virtually no other external logic. The user's effort then becomes primarily one of the software development. That is, the user can concentrate on describing his problem and translating it into a series of instructions that can be loaded into the microcomputer memory. Mostek is dedicated to making this step of software generation as simple as possible. A good example of this is our assembly language in which a simple mnemonic is used to represent every instruction that the CPU can perform. This language is self-documenting in such a way that from the mnemonic the user can understand exactly what the instruction is doing without constantly checking back to a complex cross listing.

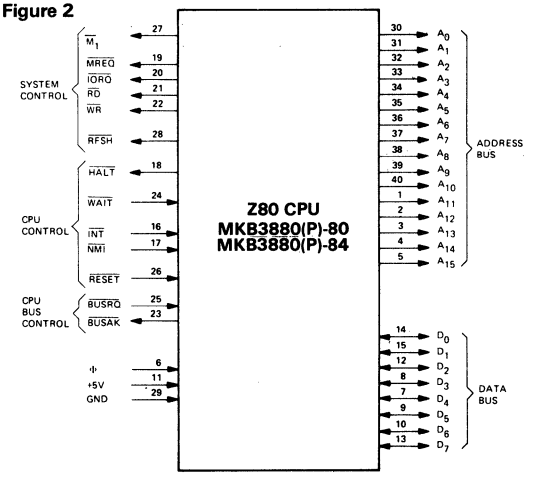
Z80-CPU BLOCK DIAGRAM

Figure 1



Z80 PIN CONFIGURATION

Figure 2



XIII

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... -55°C to +125°C
Storage Temperature ..... -65°C to +150°C
Voltage on Any Pin with Respect to Ground ..... -0.3V to +7V
Power Dissipation 1.5W

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

(T_A = -55°C to 125°C, V_{CC} = 5 V ± 5% unless otherwise specified)

SYM	PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITION
V_{ILC}	Clock Input Low Voltage	-0.3		0.8	V	
V_{IHC}	Clock Input High Voltage	V_{CC}-.6		V_{CC}+.3	V	
V_{IL}	Input Low Voltage	-0.3		0.8	V	
V_{IH}	Input High Voltage All inputs except NMI	2.4		V_{CC}	V	
$V_{IH(NMI)}$	Input High Voltage (NMI)	2.7		V_{CC}	V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 1.8mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = -250 μA
I_{CC}	Power Supply Current			200	mA	
I_{LI}	Input Leakage Current			10	μA	V_{IN} = 0 to V_{CC}
I_{LOH}	Tri-State Output Leakage Current in Float			10	μA	V_{OUT} = 2.4 to V_{CC}
I_{LOL}	Tri-State Output Leakage Current in Float			-10	μA	V_{OUT} = 0.4V
I_{LD}	Data Bus Leakage Current In Input Mode			±10	μA	$0 < V_{IN} < V_{CC}$

CAPACITANCE

T_A = 25°C, f = 1 MHz

SYM	PARAMETER	MAX	UNIT	TEST CONDITIONS
CΦ	Clock Capacitance	35	pF	Unmeasured Pins
C_{IN}	Input Capacitance	5	pF	Returned to Ground
C_{OUT}	Output Capacitance	10	pF	

AC CHARACTERISTICS

MKB3880(P)-80 Z80-CPU

(T_A = -55°C to 125°C, V_{CC} = +5V, ±5%, Unless Otherwise Noted)

SIGNAL	SYM	PARAMETER	MIN	MAX	UNIT	TEST CONDITION
	t_c	Clock Period	.4	[12]	μsec	
	$t_w(\Phi H)$	Clock Pulse Width, Clock High	180	(D)	nsec	
Φ	$t_w(\Phi L)$	Clock Pulse Width, Clock Low	180	2000	nsec	
	t_r,f	Clock Rise and Fall Time		30	nsec	
	$t_{D(AD)}$	Address Output Delay		145	nsec	
	$t_{F(AD)}$	Delay to Float		110	nsec	
	t_{acm}	Address Stable Prior to $\overline{MREQ}$ (Memory Cycle)	[1]		nsec	C_L = 50pF
A_{0-15}	t_{aci}	Address Stable Prior to $\overline{IORQ}$, $\overline{RD}$ or $\overline{WR}$ (I/O Cycle)	[2]		nsec	
	t_{ca}	Address Stable From $\overline{RD}$, $\overline{WR}$, $\overline{IORQ}$ or $\overline{MREQ}$	[3]		nsec	Except T3-M1
	t_{caf}	Address Stable From $\overline{RD}$ or $\overline{WR}$ During Float	[4]		nsec	
	$t_{D(D)}$	Data Output Delay		250	nsec	
	$t_{F(D)}$	Delay to Float During Write Cycle		90	nsec	
	$t_{S\Phi(D)}$	Data Setup Time to Rising Edge of Clock During M1 Cycle	50		nsec	
D_{0-7}	$t_{S\bar{\Phi}(D)}$	Data Setup Time to Falling Edge at Clock During M2 to M5	60		nsec	C_L = 50pF
	t_{dcm}	Data Stable Prior to $\overline{WR}$ (Memory Cycle)	[5]		nsec	
	t_{dci}	Data Stable Prior to $\overline{WR}$ (I/O Cycle)	[6]		nsec	
	t_{cdf}	Data Stable From $\overline{WR}$	[7]		nsec	
	t_H	Input Hold Time	0		nsec	
	$t_{DL\bar{\Phi}(MR)}$	$\overline{MREQ}$ Delay From Falling Edge of Clock, $\overline{MREQ}$ Low		100	nsec	
$\overline{MREQ}$	$t_{DH\Phi(MR)}$	$\overline{MREQ}$ Delay From Rising Edge of Clock, $\overline{MREQ}$ High		100	nsec	
	$t_{DH\bar{\Phi}(MR)}$	$\overline{MREQ}$ Delay From Falling Edge of Clock, $\overline{MREQ}$ High		100	nsec	C_L = 50pF
	$t_{w(\overline{MRL})}$	Pulse Width, $\overline{MREQ}$ Low	[8]		nsec	
	$t_{w(\overline{MRH})}$	Pulse Width, $\overline{MREQ}$ High	[9]		nsec	
	$t_{DL\Phi(IR)}$	$\overline{IORQ}$ Delay From Rising Edge of Clock, $\overline{IORQ}$ Low		90	nsec	
$\overline{IORQ}$	$t_{DL\bar{\Phi}(IR)}$	$\overline{IORQ}$ Delay From Falling Edge of Clock, $\overline{IORQ}$ Low		110	nsec	C_L = 50pF
	$t_{DH\Phi(IR)}$	$\overline{IORQ}$ Delay From Rising Edge of Clock, $\overline{IORQ}$ High		100	nsec	
	$t_{DH\bar{\Phi}(IR)}$	$\overline{IORQ}$ Delay From Falling Edge of Clock, $\overline{IORQ}$ High		110	nsec	
	$t_{DL\Phi(RD)}$	$\overline{RD}$ Delay From Rising Edge of Clock, $\overline{RD}$ Low		100	nsec	
$\overline{RD}$	$t_{DL\bar{\Phi}(RD)}$	$\overline{RD}$ Delay From Falling Edge of Clock, $\overline{RD}$ Low		130	nsec	C_L = 50pF
	$t_{DH\Phi(RD)}$	$\overline{RD}$ Delay From Rising Edge of Clock, $\overline{RD}$ High		100	nsec	
	$t_{DH\bar{\Phi}(RD)}$	$\overline{RD}$ Delay From Falling Edge of Clock, $\overline{RD}$ High		110	nsec	

AC CHARACTERISTICS (Cont.)

SIGNAL	SYM	PARAMETER	MIN	MAX	UNIT	TEST CONDITION
$\overline{WR}$	$t_{DL\Phi(WR)}$	$\overline{WR}$ Delay From Rising Edge of Clock, $\overline{WR}$ Low		80	nsec	C_L = 50pF
	$t_{DL\overline{\Phi}(WR)}$	$\overline{WR}$ Delay From Falling Edge of Clock, $\overline{WR}$ Low		90	nsec	
	$t_{DH\Phi(WR)}$	$\overline{WR}$ Delay From Falling Edge of Clock, $\overline{WR}$ High		100	nsec	
	$t_{w(\overline{WRL})}$	Pulse Width, $\overline{WR}$ Low	[10]		nsec	
$\overline{M1}$	$t_{DL(M1)}$	$\overline{M1}$ Delay From Rising Edge of Clock $\overline{M1}$ Low		130	nsec	C_L = 50pF
	$t_{DH(M1)}$	$\overline{M1}$ Delay From Rising Edge of Clock, $\overline{M1}$ High		130	nsec	
$\overline{RFSH}$	$t_{DL(RF)}$	$\overline{RFSH}$ Delay From Rising Edge of Clock, $\overline{RFSH}$ Low		180	nsec	C_L = 30pF
	$t_{DH(RF)}$	$\overline{RFSH}$ Delay From Rising Edge of Clock $\overline{RFSH}$ High		150	nsec	
$\overline{WAIT}$	$t_{S(WT)}$	$\overline{WAIT}$ Setup Time to Falling Edge of Clock	70		nsec	
$\overline{HALT}$	$t_{D(HT)}$	$\overline{HALT}$ Delay Time From Falling Edge of Clock		300	nsec	C_L = 50pF
$\overline{INT}$	$t_{s(IT)}$	$\overline{INT}$ Setup Time to Rising Edge of Clock	80		nsec	
$\overline{NMI}$	$t_{w(\overline{NML})}$	Pulse Width, $\overline{NMI}$ Low	80		nsec	
$\overline{BUSRQ}$	$t_{s(BQ)}$	$\overline{BUSRQ}$ Setup Time to Rising Edge of Clock	80		nsec	
$\overline{BUSAK}$	$t_{DL(BA)}$	$\overline{BUSAK}$ Delay From Rising Edge of Clock, $\overline{BUSAK}$ Low		120	nsec	C_L = 50pF
	$t_{DH(BA)}$	$\overline{BUSAK}$ Delay From Falling Edge of Clock, $\overline{BUSAK}$ High		110	nsec	
$\overline{RESET}$	$t_{s(RS)}$	$\overline{RESET}$ Setup Time to Rising Edge of Clock	90		nsec	
	$t_{F(C)}$	Delay to/from Float ($\overline{MREQ}$, $\overline{IORQ}$, $\overline{RD}$ and $\overline{WR}$)		100	nsec	
	t_{mr}	$\overline{M1}$ Stable Prior to IORQ (Interrupt Ack.)	[11]		nsec	

NOTES

1. Data should be enabled onto the CPU data bus when RD is active. During interrupt acknowledge data should be enabled when $\overline{M1}$ and $\overline{IORQ}$ are both active.
2. The $\overline{RESET}$ signal must be active for a minimum of 3 clock cycles.
3. Output Delay vs. Load Capacitance
   T_A = 125°C V_{CC} = 5 V ± 5%
   Add 10 nsec delay for each 50pF increase in load up to a maximum of 200pF for the data bus and 100pF for address and control lines.
4. Although static by design, testing guarantees t_w (ΦH) of 200 μsec maximum.

[1] $t_{acm} = t_w(\Phi H) + t_f - 75$

[2] $t_{aci} = t_c - 80$

[3] $t_{ca} = t_w(\Phi L) + t_r - 40$

[4] $t_{caf} = t_w(\Phi L) + t_r - 60$

[5] $t_{dcm} = t_c - 210$

[6] $t_{dci} = t_w(\Phi L) + t_r - 210$

[7] $t_{cdf} = t_w(\Phi L) + t_r - 80$

[8] $t_w(\overline{MRL}) = t_c - 40$

[9] $t_w(\overline{MRH}) = t_w(\Phi H) + t_f - 70$

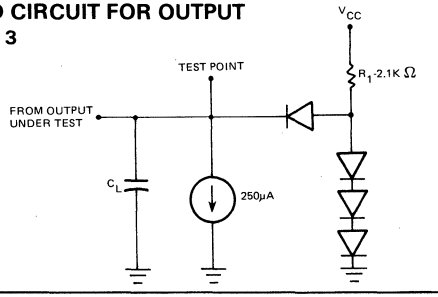
[10] $t_w(\overline{WR}) = t_c - 40$

[11] $t_{mr} = 2t_c + t_w(\Phi H) + t_f - 80$

[12] $t_c = t_w(\Phi H) + t_w(\Phi L) + t_r + t_f$

LOAD CIRCUIT FOR OUTPUT

Figure 3



AC CHARACTERISTICS
MKB3880(P)-84 Z80A-CPU
(T_A = -55°C to 125°C, V_{CC} = +5V, ±5%, Unless Otherwise Noted)

SIGNAL	SYM	PARAMETER	MIN	MAX	UNIT	TEST CONDITION
	t_c	Clock Period	.25	[12]	μsec	
	$t_w(\Phi H)$	Clock Pulse Width, Clock High	110	(D)	nsec	
Φ	$t_w(\Phi L)$	Clock Pulse Width, Clock Low	110	2000	nsec	
	t_r, f	Clock Rise and Fall Time		30	nsec	
	$t_{D(AD)}$	Address Output Delay		110	nsec	
	$t_{F(AD)}$	Delay to Float		90	nsec	
	t_{acm}	Address Stable Prior to $\overline{MREQ}$ (Memory Cycle)	[1]		nsec	C_L = 50pF
A_{0-15}	t_{aci}	Address Stable Prior to $\overline{IORQ}$, $\overline{RD}$ or $\overline{WR}$ (I/O Cycle)	[2]		nsec	
	t_{ca}	Address Stable From $\overline{RD}$, $\overline{WR}$, $\overline{IORQ}$ or $\overline{MREQ}$	[3]		nsec	Except T3-M1
	t_{caf}	Address Stable From $\overline{RD}$ or $\overline{WR}$ During Float	[4]		nsec	
	$t_{D(D)}$	Data Output Delay		170	nsec	
	$t_{F(D)}$	Delay to Float During Write Cycle		90	nsec	
	$t_{S\Phi(D)}$	Data Setup Time to Rising Edge of Clock During M1 Cycle	50		nsec	
D_{0-7}	$t_{S\overline{\Phi}(D)}$	Data Setup Time to Falling Edge at Clock During M2 to M5	60		nsec	C_L = 50pF
	t_{dcm}	Data Stable Prior to $\overline{WR}$ (Memory Cycle)	[5]		nsec	
	t_{dci}	Data Stable Prior to $\overline{WR}$ (I/O Cycle)	[6]		nsec	
	t_{cdf}	Data Stable From $\overline{WR}$	[7]		nsec	
	t_H	Input Hold Time	0		nsec	
	$t_{DL\Phi(MR)}$	$\overline{MREQ}$ Delay From Falling Edge of Clock, $\overline{MREQ}$ Low	20	85	nsec	
$\overline{MREQ}$	$t_{DH\Phi(MR)}$	$\overline{MREQ}$ Delay From Rising Edge of Clock, $\overline{MREQ}$ High		85	nsec	
	$t_{DH\overline{\Phi}(MR)}$	$\overline{MREQ}$ Delay From Falling Edge of Clock, $\overline{MREQ}$ High		85	nsec	C_L = 50pF
	$t_{w(\overline{MRL})}$	Pulse Width, $\overline{MREQ}$ Low	[8]		nsec	
	$t_{w(\overline{MRH})}$	Pulse Width, $\overline{MREQ}$ High	[9]		nsec	
	$t_{DL\Phi(IR)}$	$\overline{IORQ}$ Delay From Rising Edge of Clock, $\overline{IORQ}$ Low		75	nsec	
$\overline{IORQ}$	$t_{DL\overline{\Phi}(IR)}$	$\overline{IORQ}$ Delay From Falling Edge of Clock, $\overline{IORQ}$ Low		85	nsec	C_L = 50pF
	$t_{DH\overline{\Phi}(IR)}$	$\overline{IORQ}$ Delay From Rising Edge of Clock, $\overline{IORQ}$ High		85	nsec	
	$t_{DH\Phi(IR)}$	$\overline{IORQ}$ Delay From Falling Edge of Clock, $\overline{IORQ}$ High		85	nsec	
	$t_{DL\Phi(RD)}$	$\overline{RD}$ Delay From Rising Edge of Clock, $\overline{RD}$ Low		85	nsec	
$\overline{RD}$	$t_{DL\overline{\Phi}(RD)}$	$\overline{RD}$ Delay From Falling Edge of Clock, $\overline{RD}$ Low		95	nsec	C_L = 50pF
	$t_{DH\Phi(RD)}$	$\overline{RD}$ Delay From Rising Edge of Clock, $\overline{RD}$ High		85	nsec	
	$t_{DH\overline{\Phi}(RD)}$	$\overline{RD}$ Delay From Falling Edge of Clock, $\overline{RD}$ High		85	nsec	

XIII

AC CHARACTERISTICS (Cont.)

SIGNAL	SYM	PARAMETER	MIN	MAX	UNIT	TEST CONDITION
$\overline{WR}$	$t_{DL\Phi(WR)}$	$\overline{WR}$ Delay From Rising Edge of Clock, $\overline{WR}$ Low		65	nsec	C_L = 50pF
	$t_{DL\overline{\Phi}(WR)}$	$\overline{WR}$ Delay From Falling Edge of Clock, $\overline{WR}$ Low		80	nsec	
	$t_{DH\Phi(WR)}$	$\overline{WR}$ Delay From Falling Edge of Clock, $\overline{WR}$ High		80	nsec	
	$t_{w(\overline{WR}L)}$	Pulse Width, $\overline{WR}$ Low	[10]		nsec	
$\overline{M1}$	$t_{DL(M1)}$	$\overline{M1}$ Delay From Rising Edge of Clock $\overline{M1}$ Low		100	nsec	C_L = 50pF
	$t_{DH(M1)}$	$\overline{M1}$ Delay From Rising Edge of Clock, $\overline{M1}$ High		100	nsec	
$\overline{RFSH}$	$t_{DL(RF)}$	$\overline{RFSH}$ Delay From Rising Edge of Clock, $\overline{RFSH}$ Low		130	nsec	C_L = 50pF
	$t_{DH(RF)}$	$\overline{RFSH}$ Delay From Rising Edge of Clock $\overline{RFSH}$ High		120	nsec	
$\overline{WAIT}$	$t_{S(WT)}$	$\overline{WAIT}$ Setup Time to Falling Edge of Clock	70		nsec	
$\overline{HALT}$	$t_{D(HT)}$	$\overline{HALT}$ Delay Time From Falling Edge of Clock		300	nsec	C_L = 50pF
$\overline{INT}$	$t_{s(IT)}$	$\overline{INT}$ Setup Time to Rising Edge of Clock	80		nsec	
$\overline{NMI}$	$t_{w(\overline{NML})}$	Pulse Width, $\overline{NMI}$ Low	80		nsec	
$\overline{BUSRQ}$	$t_{s(BQ)}$	$\overline{BUSRQ}$ Setup Time to Rising Edge of Clock	50		nsec	
$\overline{BUSAK}$	$t_{DL(BA)}$	$\overline{BUSAK}$ Delay From Rising Edge of Clock, $\overline{BUSAK}$ Low		100	nsec	C_L = 50pF
	$t_{DH(BA)}$	$\overline{BUSAK}$ Delay From Falling Edge of Clock, $\overline{BUSAK}$ High		100	nsec	
$\overline{RESET}$	$t_{s(RS)}$	$\overline{RESET}$ Setup Time to Rising Edge of Clock	60		nsec	
	$t_{F(C)}$	Delay to/From Float ($\overline{MREQ}$, $\overline{IORQ}$, $\overline{RD}$ and $\overline{WR}$)		80	nsec	
	t_{mr}	$\overline{M1}$ Stable Prior to $\overline{IORQ}$ (Interrupt Ack.)	[11]		nsec	

NOTES

1. Data should be enabled onto the CPU data bus when $\overline{RD}$ is active. During interrupt acknowledge data should be enabled when $\overline{M1}$ and $\overline{IORQ}$ are both active.
2. The $\overline{RESET}$ signal must be active for a minimum of 3 clock cycles.
3. Output Delay vs. Load Capacitance
   T_A = 125°C V_{CC} = 5 V ± 5%
   Add 10 nsec delay for each 50pF increase in load up to a maximum of 200pF for the data bus and 100pF for address and control lines.
4. Although static by design, testing guarantees t_w (ΦH) of 200 μsec maximum.

[1] $t_{acm} = t_w(\Phi H) + t_f - 65$

[2] $t_{aci} = t_c - 70$

[3] $t_{ca} = t_w(\Phi L) + t_r - 50$

[4] $t_{caf} = t_w(\Phi L) + t_r - 45$

[5] $t_{dcm} = t_c - 170$

[6] $t_{dci} = t_w(\Phi L) + t_r - 170$

[7] $t_{cdf} = t_w(\Phi L) + t_r - 70$

[8] $t_w(\overline{MRL}) = t_c - 30$

[9] $t_w(\overline{MRH}) = t_w(\Phi H) + t_f - 40$

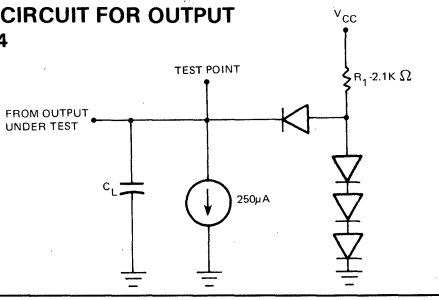
[10] $t_w(\overline{WR}) = t_c - 30$

[11] $t_{mr} = 2t_c + t_w(\Phi H) + t_f - 65$

[12] $t_c = 6_w(\Phi H) + t_w(\Phi L) + t_r + t_f$

LOAD CIRCUIT FOR OUTPUT

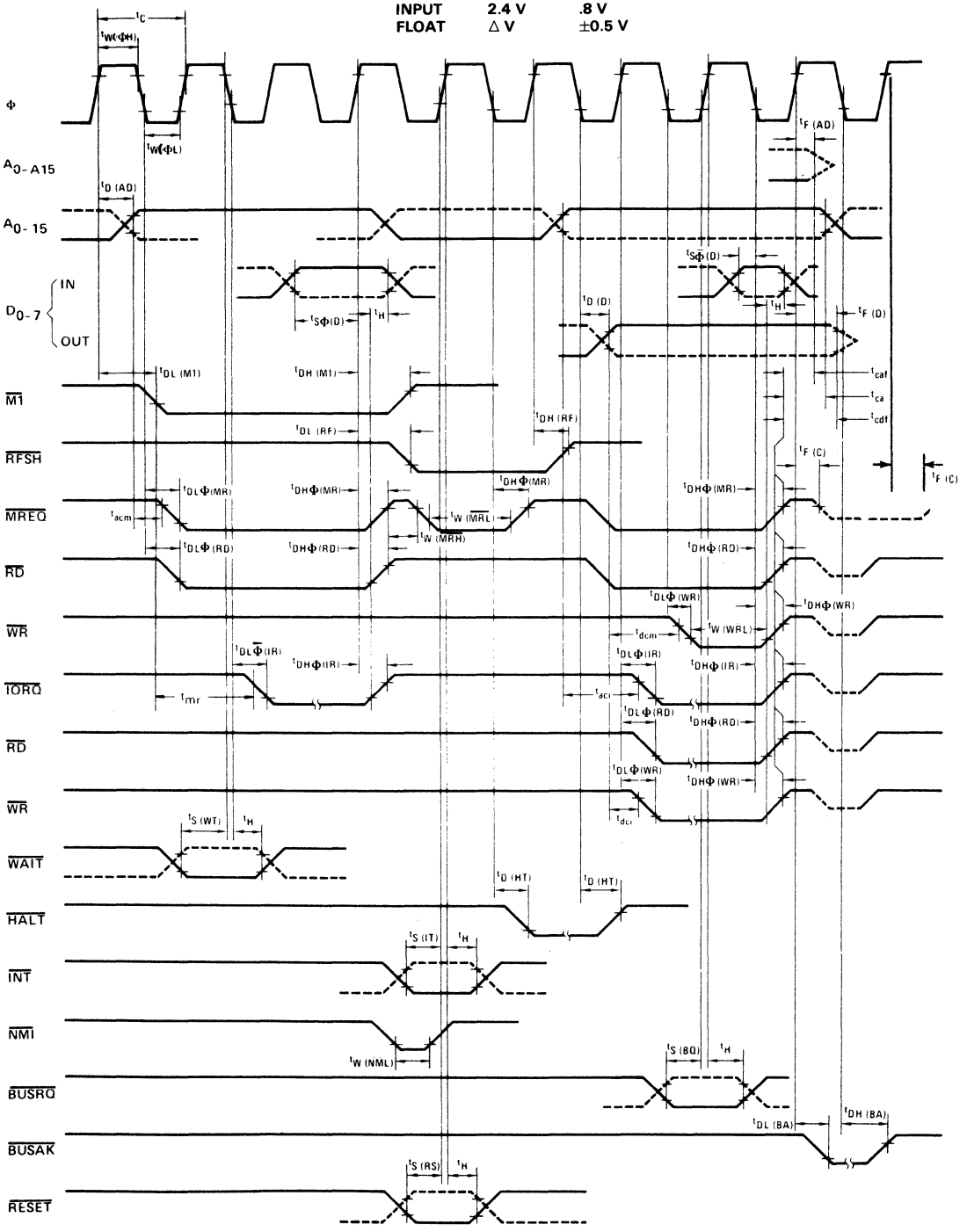
Figure 4



A.C. TIMING DIAGRAM

Timing measurements are made at the following voltages, unless otherwise specified.

	"1"	"0"
CLOCK	V_{CC}—.6	.8 V
OUTPUT	2.4 V	.8 V
INPUT	2.4 V	.8 V
FLOAT	Δ V	±0.5 V



PRODUCT PREVIEW

MOSTEK®

MILITARY/HIGH-REL PRODUCTS

Processed to MIL-STD 883, Method 5004, Class B

Parallel I/O Controller

MKB3881(P)-80/84

FEATURES

- ☐ Two independent 8 bit bidirectional peripheral interface ports with 'handshake' data transfer control
- ☐ Interrupt driven 'handshake' for fast response
- ☐ Any one of four distinct modes of operation may be selected for a port including:
  - Byte output
  - Byte input
  - Byte bidirectional bus (Available on Port A only)
  - Bit control mode

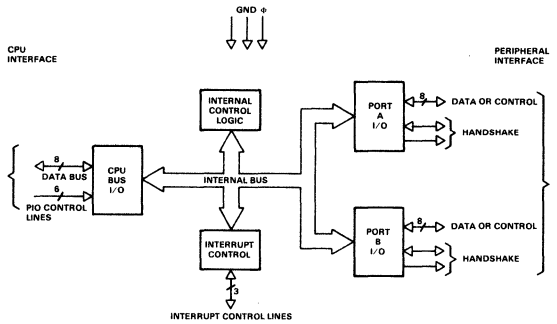
  All with interrupt controlled handshake
- ☐ Daisy chain priority interrupt logic included to provide for automatic interrupt vectoring without external logic
- ☐ Eight outputs are capable of driving Darlington transistors
- ☐ Typical ordering: MKB3881P-80 2.5 MHz Z80-PIO
  MKB3881P-84 4.0 MHz Z80-PIO
- ☐ Single 5 volt supply and single phase clock required
- ☐ Fully processed to MIL-STD-883 Method 5004, Class B. -55°C to 125°C temperature range
- ☐ MKI3881 available for Industrial/Hi-Rel users

DESCRIPTION

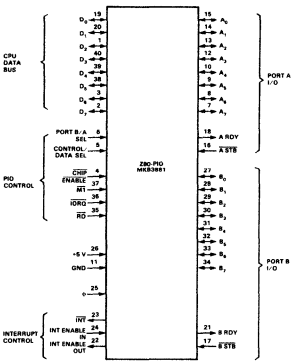
The Z80 Parallel I/O Circuit is a programmable, two port device which provides a TTL compatible interface between peripheral devices and the Z80-CPU. The CPU can configure the Z80-PIO to interface with a wide range of peripheral devices with no other external logic required. Typical peripheral devices that are fully compatible with the Z80-PIO include most keyboards, paper tape readers and punches, printers, PROM programmers, etc. The Z80-PIO utilizes N channel silicon gate depletion load technology and is packaged in a hermetic 40 pin DIP.

One of the unique features of the Z80-PIO that separates it from other interface controllers is that all data transfer between the peripheral device and the CPU is accomplished under total interrupt control. The interrupt logic of the PIO permits full usage of the efficient interrupt capabilities of the Z80-CPU during I/O transfers. All logic necessary to implement a fully nested interrupt structure is included in the PIO so that additional circuits are not required. Another unique feature of the PIO is that it can be programmed to interrupt the CPU on the occurrence of specified status conditions in the peripheral device. For example, the PIO can be programmed to interrupt if any specified peripheral alarm conditions should occur. This interrupt capability reduces the amount of time that the processor must spend in polling peripheral status.

PIO BLOCK DIAGRAM



PIO PIN CONFIGURATION



XIII

PRODUCT PREVIEW

MOSTEK®

MILITARY/HIGH-REL PRODUCTS

Processed to MIL-STD 883, Method 5004, Class B

Counter Timer Circuit

MKB3882 (P/J)-80/84

FEATURES

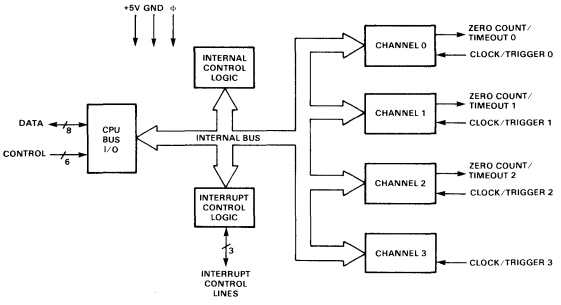
- Each channel may be selected to operate in either Counter Mode or Timer Mode
- Used in either mode, a CPU-readable Down Counter indicates number of counts-to-go until zero
- A Time Constant Register can automatically reload the Down Counter at Count Zero in Counter and Timer Mode
- Selectable positive or negative trigger initiates time operation in Timer Mode. The same input is monitored for event counts in Counter Mode
- Three channels have Zero Count/Timeout outputs capable of driving Darlington transistors
- Interrupts may be programmed to occur on the zero count condition in any channel
- Daisy chain priority interrupt logic included to provide for automatic interrupt vectoring without external logic
- Typical ordering: MKB3882P-80 2.5 MHz Z80-CTC
  MKB3882P-84 4.0 MHz Z80-CTC
- Fully processed to MIL-STD-883 Method 5004 Class B. −55°C to +125°C operating range
- MKI3882 available for Industrial Hi-Rel users

DESCRIPTION

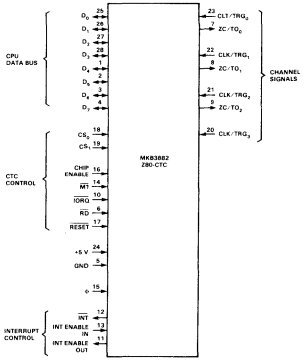
The Z80-Counter Timer Circuit (CTC) is a programmable component with four independent channels that provide counting and timing functions for microcomputer systems based on the Z80-CPU. The CPU can configure the CTC channels to operate under various modes and conditions as required to interface with a wide range of devices. In most applications, little or no external logic is required. The Z80-CTC utilizes N-channel silicon gate depletion load technology and is packaged in a 28-pin DIP. The Z80-CTC requires only a single 5 volt supply and a one-phase 5 volt clock.

A block diagram of the Z80-CTC is shown in the figure. The internal structure of the Z80-CTC consists of a Z80-CPU bus interface, Internal Control Logic, four sets of Counter/Timer Channel Logic, and Interrupt Control Logic. The four independent counter/timer channels are identified by sequential numbers from 0 to 3. The CTC has the capability of generating a unique interrupt vector for each separate channel (for automatic vectoring to an interrupt service routine). The 4 channels can be connected into four contiguous slots in the standard Z80 priority chain with channel number 0 having the highest priority. The CPU bus interface logic allows the CTC device to interface directly to the CPU with no other external logic. However, port address decoders and/or line buffers may be required for large systems.

Z80-CTC BLOCK DIAGRAM



Z80-CTC PIN CONFIGURATION



XIII

PRODUCT PREVIEW

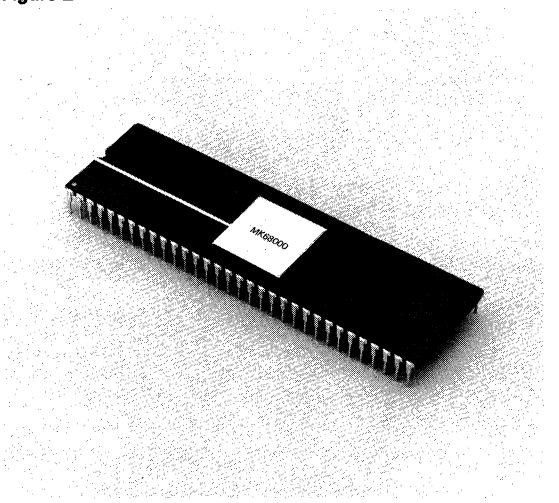
SCREENED TO MIL-STD-883 16-BIT MICROPROCESSOR MKB68000

Advances in semiconductor technology have provided the capability to place on a single silicon chip a microprocessor at least an order of magnitude higher in performance and circuit complexity than has been previously available. The MKB68000 is the first of a family of such VLSI microprocessors from Mostek. It combines state-of-the-art technology and advanced circuit design techniques with computer sciences to achieve an architecturally advanced 16-bit microprocessor.

The resources available to the MKB68000 user consist of the following:

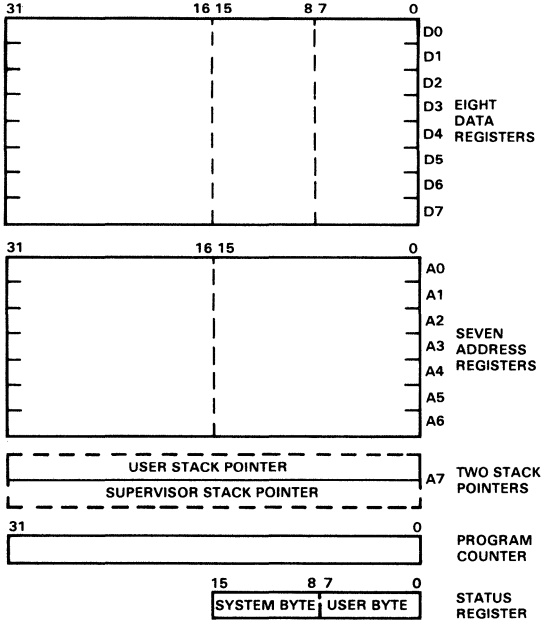
- 32-Bit Data and Address Registers
- 16 Megabyte Direct Addressing Range
- 56 Powerful Instruction Types
- Operations on Five Main Data Types
- Memory Mapped I/O
- 14 Addressing Modes

MKB68000
Figure 2



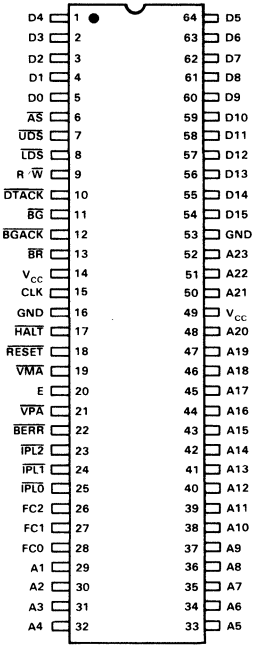
PROGRAMMING MODEL

Figure 1



PIN ASSIGNMENT

Figure 3



XIII

This is advance information and specifications are subject to change without notice.

1982/1983 MICROELECTRONIC DATA BOOK

MKI INDUSTRIAL HIGH RELIABILITY PRODUCTS

The MKI family of memories and microprocessors is manufactured by Mostek to be cost-effective for industrial hi-rel applications. These devices are produced by the Military Products Department using QPL facilities to insure high quality and built-in reliability. Compared with commercial devices, MKI offers these principle product enhancements:

1. **Extended temperature operation.** All devices receive complete electrical testing to verify funtionality to AC and DC parameters over the -40°C to +85°C temperature range.

2. **Greater system reliability.** Each device receives a 125°C dynamic burn-in of at least 44 hours to remove potential early life failures. Hermetic packaging exclusively is employed.

3. **Improved quality.** Stringent military 100% test criteria are applied and tightened AQL levels are guaranteed.

These reliability and capability enhancements make the MKI device family ideally suited for high-reliability extended temperature industrial applications. And, because improved quality and reliability mean lower cost of ownership, virtually any application should benefit economically. Table 1 illustrates the breadth of application of the MKI device family.

Partial MKI Applications Spectrum
Table 1

INDUSTRY	SYSTEM APPLICATION
TELECOMMUNICATIONS	MESSAGE SWITCHING DATA TRANSLATION
MILITARY/AEROSPACE	GROUND EQUIPMENT
AUTOMOTIVE	ENGINE CONTROL INSTRUMENTATION
MANUFACTURING	PROCESS CONTROL INSTRUMENTATION DATA GATHERING/ANALYSIS
MEDICAL	DIAGNOSTIC/LIFE SUPPORT EQUIPMENT INSTRUMENTATION
AVIATION	FAA RADAR AIRCRAFT GUIDANCE AND CONTROL

WHY DEMAND GREATER DEVICE QUALITY

From the user's standpoint, improved incoming integrated circuit quality means a lower cost of ownership.

As devices are mounted onto boards and then assembled into systems, it becomes increasingly difficult and expensive to remove failed devices from the manufacturing process. The full cost of locating and replacing one bad IC during system assembly can range between $7 and $50 at today's rates. Figure 1 depicts this.

Typical costs for detection and replacement of IC failures at various manufacturing stages.
Figure 1

At the component level, complex VLSI devices demand extremely expensive testers for incoming evaluation. A costly support staff must be maintained for test software generation, tester operation and maintenance and parts control.

At the board level, failed components reduce board test throughput causing production delays. And inefficient use of expensive automatic board test systems results if they are time-shared for troubleshooting. To keep the production flow smooth, failed boards are usually accumulated for later repair. This increases work-in-process and component inventories and their carrying costs.

At the system level, the cost of component failure is magnified further. Due to the increased level of integration, problem devices at this point are more difficult to find. And failures at this late a stage often mean late customer deliveries.

OPTIONS FOR ACHIEVING IMPROVED DEVICE QUALITY

The user has a choice of any of three alternatives for achieving greater IC quality. These are:

1. In-house incoming test

2. Use of burn-in test laboratories

3. Original purchase of vendor-screened hi-rel devices.

Alternative 1, as noted before, can be very expensive. Usually, this option is reserved for only the very large user (consumption approaching 100 million units/year). His volume presents the opportunity to realize economies of scale, and the large capital equipment outlay is easily absorbed.

Burn-in labs can generally be expected to effectively test SSI and most MSI functions. But complex, highly integrated devices require an intimate familiarity with their design and layout plus an extensive characterization and production test database to insure consistently effective screening. This level of ability resides with the IC manufacturer alone. For example, many VLSI devices can exhibit pattern and temperature sensitivities that may only become apparent years after their introduction. A particular sensitivity might even vary from manufacturer to manufacturer for the same generic part type. Screens for these potential failure modes are frequently considered proprietary by the device maker. They are therefore rarely part of the test procedure used by burn-in labs.

Beyond these fundamental concerns about test integrity itself, use of burn-in labs often results in various logistics problems (Table 2), such as:

1. Unpredictable losses due to burn-in and temperature test fallout. Possible ESD handling losses.

2. Additional receiving inspections plus shipping and handling costs.

3. Maintenance of larger in-transit and stockroom inventories.

The use of manufacturer screened hi-rel devices such as Mostek's MKI series, avoids all of the problems associated with other alternatives. Mostek is experienced in every phase of volume VLSI production and test. Simply, quality and reliability are assured by letting "the experts do it".

Considerations in the decision to upgrade commercial or purchase vendor produced hi-rel ICs.
Table 2

CONSIDERATION	VARIABLES OF UPGRADING COMMERCIAL ICs	THE CERTAINTIES OF BUYING MKI
Test Adequacy	Often Inadequate	Complete & Guaranteed
Delivery	Slow: missed shipments, processing time, ESD and yield losses	Fast: usually from stock
Cost	Excessive at low to moderate volumes	Cost-effective
Verifying Inspections	Many	One
Handling	Increased (ESD problems)	Minimized
Inventory Levels	Increased: in transit plus work-in-process	No Increase
Extended Temperature Operation	Test and yield unpredictable without characterization database	Standard with MKI
Warranty	None	New Product Warranty

MKI: ACHIEVING IMPROVED QUALITY

IC FAILURE MECHANISMS

In typical usage, IC failures are traceable to random defects or errors that occurred at some stage in their production. Table 3 below illustrates the types of failure mechanisms affecting device quality in each of three major production stages. Also noted are the MKI controls applied to eliminate these defects during production.

QUALITY STARTS IN WAFER FAB

Quality and reliability are built into Mostek MKI products starting in wafer fabrication. Facilities and equipment in this critical area are among the most advanced in the world today. Five-inch wafers are positioned and exposed with direct-step-on-wafer (DSW) projection systems. This assures highly accurate feature definition, enhancing yields and minimizing defect density. In ultra-clean darkroom areas, dust particles are controlled to within 10 ppm not exceeding ½ micron in size, further minimizing chances of contamination that could jeopardize reliability. Tightly controlled processes, coupled with Mostek's history of innovative circuit design and fabrication experience, result in MKI devices with built-in reliability.

MKI TESTING

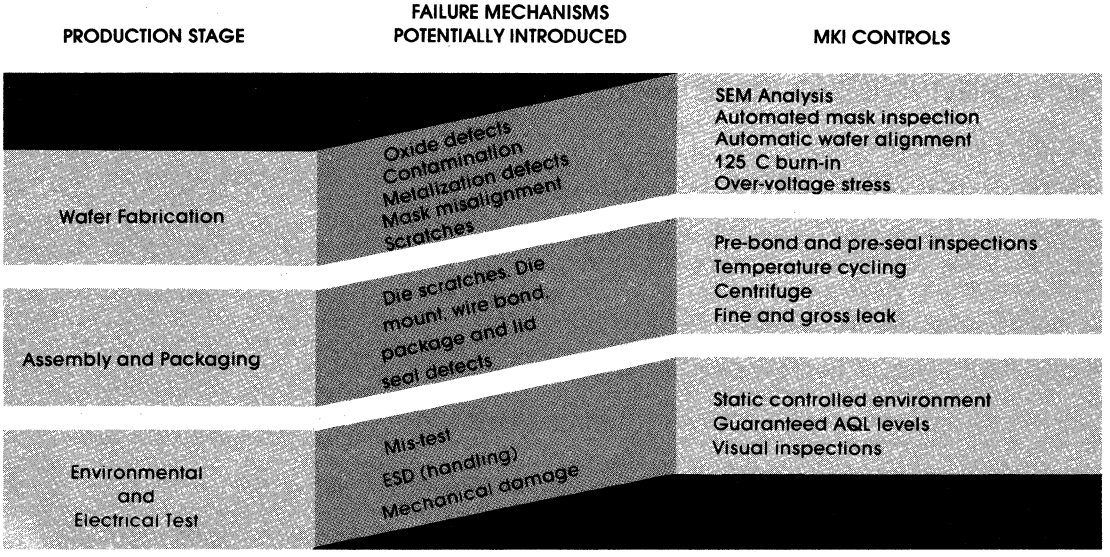
The MKI program subjects each device to a battery of 100% environmental and electrical tests to weed out defectives and assure conformance to specifications. Table 4 depicts the rigorous screening MKI devices undergo. Test criteria are based upon MIL-STD-883B methods.

MKI Test Flow
Table 4

SCREEN	100% TEST REQUIREMENTS
Die Inspection	75X magnification
Pre-Seal Inspection	30X-60X magnification
Temperature Cycle	883B, 1010 Cond. C, 5 Cycles, -65°C to +150°C
Centrifuge	883B, 2001 Cond. D, 20 Kg, Y_1
Fine Leak	883B, 1014 Cond. B, 1 X 10^{-7} atm cc/sec
Gross Leak	883B, Method 1014, Cond. C1
Voltage Stress (DRAMs Only)	883B, 1015 Cond. D, dynamic 10 Hrs. Min., 125°C
Electrical Tests	883B, Group A electrical subgroups, testing AC, DC, and functional performance over full temp. range
Burn-In	883B, 1015 Cond. D, dynamic 44 Hrs. Min.,* 125°C
Electrical Tests	AC and DC at max temp.
External Visual	Visual tests to guarantee marking, construction and mechanical integrity
QA Lot Acceptance	883B, Method 5005 Group A sample testing to guarantee performance to data sheet over full temp. range.

*Burn-in is generally longer. The MKI program requires the removal of infant failures to the point at which the failure rate becomes essentially flat. Analysis of device complexity, production maturity and Group C life test data help determine burn-in length required.

IC Failure Mechanisms and MKI Controls
Table 3



TIGHTENED AQL REQUIREMENTS VERIFY QUALITY

The MKI Quality Level program is designed to prevent the possibility of shipment of defective devices to the user. Table 5 details AQL levels all MKI devices must meet prior to shipment.

MKI AQL Guarantee
Table 5

Functionality	-40 C 25 C 85 C	.4% .4% .4%
DC Parameters	-40 C 25 C 85 C	.4% .4% .4%
AC Parameters	-40 C 25 C 85 C	.4% .4% .4%
Mechanical	— — —	.65%
Hermeticity	Fine Leak Gross Leak	.25% .25%
Solderability	— — —	LTPD 10

The MKI guarantee of .4% electrical AQL applies to all AC and DC parameters and functionality over the entire -40°C to +85°C range. For extended temperature designs requiring critical parametric performance at temperature, MKI provides an extra margin of design safety. Temperature upgrading of standard commercial devices at a burn-in lab is generally not practical. Without access to a device's temperature characterization database, extended temperature testing at a test lab may result in extremely low yields. It may also compromise reliability since the commercial device manufacturer's "maximum operating temperature" warning has been exceeded. With MKI from Mostek, extended temperature performance to spec is **guaranteed.**

MKI: ACHIEVING IMPROVED RELIABILITY

PRODUCT RELIABILITY

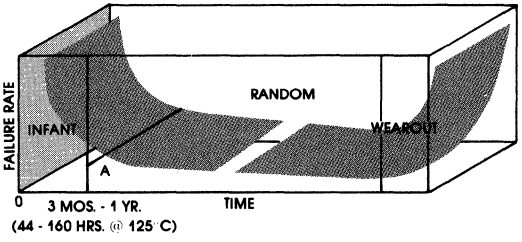
Reliability cannot be tested into a device. It must be built in through proper, worst-case circuit design and tightly-controlled wafer fab processes. The implementation of this philosophy keeps Mostek products among the most reliable available anywhere.

Reliability however, must be verified before a device reaches the user through stress testing. The MKI program incorporates a variety of 100% screens (Table 4) to compress time and weed out early life failures. Temperature cycling, centrifuge, hermeticity, voltage stress, and high temperature test all effectively screen a percentage of the infant mortality, thereby improving system reliability. The most important MKI reliability screen applied is the 125°C, 44 hour minimum, dynamic burn-in. This stress test, accomplished at higher than nominal voltage, eliminates the two major sources of early device failure: oxide defects and contamination. Together, these two failure mechanisms account for between 60% and 85% of MOS LSI failures in normal system usage.

MKI BURN-IN AND INFANT FAILURES

It has been shown that the failure rate of semiconductor devices over time is well described by the curve in Figure 2 below. The bathtub curve, as it's commonly called, is divided into three regions. Failures per unit time are greatest in the first 3 months to 1 year of normal usage, corresponding to the infant failure region of Figure 2. Beyond this, the failure rate is small and gradually declining throughout the useful life of the device (20 years or more). Defective devices in this phase are random and infrequent and remain so until wearout sets in.

Semiconductor failure rate vs. time
Figure 2



MKI devices recieve a variable length burn-in (44 hours minimum) sufficient to remove the vast majority of infant failures. Data from ongoing MIL-STD 883, Method 5005, Group C, 1000 hour life testing is periodically analyzed to describe the shape of a device's reliability curve. The required length of MKI burn-in is accurately determined from this and other considerations.

What is the importance of MKI burn-in to the user? Point A in Figure 2 represents the reduced failure rate of MKI devices at delivery. This rate is as much as 10 to 15 times lower than that exhibited by standard commercial devices. It would take between 3 and 12 months of normal operation of a system using commercial devices to weed out enough failures before the remainder were as reliable as MKI devices are at delivery. Further, the MKI variable length burn-in can be expected to eliminate between 40% and 60% of devices subject to fail anytime in their useful life. With MKI, a system manufacturer need not be subject to the expense of repairing early failures at the customer's site. And, the cost and difficulty of stressing his system in-house for long periods of time before delivery is eliminated. In short, the use of MKI ICs can help minimize system cost and maximize customer satisfaction.

MKI PRODUCTS AND ORDERING INFORMATION

MKI industrial hi-rel components are produced by the Military Products Department at Mostek using QPL facilities. Table 6 shows currently available and planned future MKI products. Generally, every MKI device is also available screened to Method 5004, Class B of MIL-STD-883 (prefixed "MKB").

MKI Device Listing
Table 6

PRODUCT	DEVICE	ORGANIZATION	TEMP. RANGE	ACCESS TIME OR FREQUENCY
DYNAMIC RAMs	MKI4116J-72	16 K x 1	-40/+85°C	150 ns
	MKI4116J-73	16 K x 1	-40/+85°C	200 ns
	MKI4116J-74	16 K x 1	-40/+85°C	250 ns
	MKI4564P/J-73†	64 K x 1	-40/+85°C	200 ns
	MKI4564P/J-74†	64 K x 1	-40/+85°C	250 ns
STATIC RAMs	MKI4118AJ-71	1 K x 8	-40/+85°C	120 ns
	MKI4118AJ-72	1 K x 8	-40/+85°C	150 ns
	MKI4118AJ-73	1 K x 8	-40/+85°C	200 ns
	MKI4802P/J-790	2 K x 8	-40/+85°C	90 ns
	MKI4802P/J-71	2 K x 8	-40/+85°C	120 ns
	MKI4802P/J-73	2 K x 8	-40/+85°C	200 ns
ROMs	MKI37000P/J-74	8 K x 8	-40/+85°C	300 ns
EPROMs	MKI2716J-77	2 K x 8	-40/+85°C	390 ns
	MKI2716J-78	2 K x 8	-40/+85°C	450 ns
MICROPROCESSORS	MKI3880P/J-70	Z80 CPU	-40/+85°C	2.5 MHz
	MKI3880P/J-74	Z80 CPU	-40/+85°C	4.0 MHz

†1982 Introduction

PART NUMBERING

Example: MKI4116J-73

MK	I	4116	J	–	7	3
Mostek Corp. standard prefix	Device screening level: I = Industrial Hi-Rel	Mostek generic part number	Package: J = cerdip P = ceramic side-brazed DIP		Temperature: -40/+85°C for MKI Products	Access time: device dependent

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MOSTEK®

MILITARY/HIGH-REL PRODUCTS

Extended Temperature, Extended Burn-in Industrial Processing

2048 x 8-Bit UV Erasable PROM

MKI2716(J)-77/78

FEATURES

- ☐ 44 hr. min., 125°C burn-in plus Industrial screening for greater reliability (see Figure 3 for processing description)
- ☐ Extended operating temperature ($-40°C \leq T_A \leq 85°C$)
- ☐ Pin compatible with Mostek's BYTEWYDE™ memory family
- ☐ Single +5 volt power supply during read operation
- ☐ Fast 450ns access time in read mode
- ☐ Low power dissipation: 633 mW max active
- ☐ Power down mode: 165 mW max standby
- ☐ Three state output OR-tie capability
- ☐ Five modes of operation for greater system flexibility (see Table)
- ☐ Single programming requirement: single location programming with one 50 msec pulse
- ☐ Military MKB version available (-55°C to 125°C)
- ☐ TTL compatible in all operating modes
- ☐ Standard 24 pin DIP with transparent lid

DESCRIPTION

The MKI2716 is a 2048 x 8 bit electrically programmable/ultraviolet erasable read only memory. The circuit is fabricated with Mostek's advanced N-channel silicon gate technology for the highest performance and reliability. The MKI2716 offers significant advances over hardwired logic cost, system flexibility, turnaround time and performance.

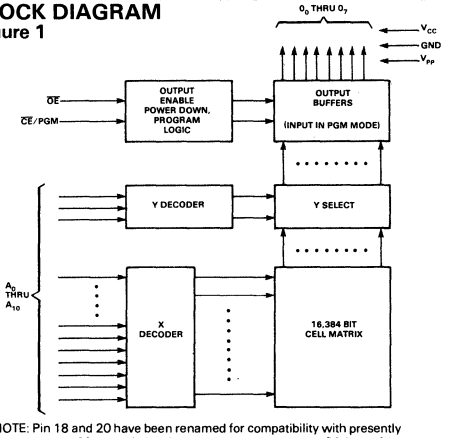
The MKI2716 has many useful system oriented features including a standby mode of operation which lowers the device power from 633mW maximum active power to 165mW maximum for an overall savings of 75%.

MODE SELECTION

Pin / Mode	$\overline{CE}$/PGM (18)	$\overline{OE}$ (20)	V_{PP} (21)	Output
Read	V_{IL}	V_{IL}	+5	Valid Out
Standby	V_{IH}	Don't Care	+5	Open
Program	Pulsed V_{IL} to V_{IH}	V_{IH}	+25	Input
Program Verify	V_{IL}	V_{IL}	+25	Valid Out
Program Inhibit	V_{IL}	V_{IH}	+25	Open

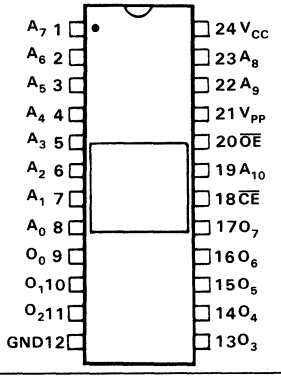
V_{CC}(24) = 5V all modes

BLOCK DIAGRAM
Figure 1



NOTE: Pin 18 and 20 have been renamed for compatibility with presently available 16K, 32K and 64K ROMs and future generation 32K and 64K EPROMs. All other specifications for this device remain unaffected by this change.

PIN CONNECTIONS
Figure 2



PIN NAMES

A0 - A10	Addresses	OE	Output Enable
$\overline{CE}$/PGM	Chip Enable/ Program	O_0 - O_7	Outputs

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ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to V_{SS} (Except V_{PP}) ..... -0.3 V to +6 V
Voltage on V_{PP} supply pin relative to V_{SS} ..... -0.3 V to +28 V
Operating Temperature T_A (Ambient) ..... $-40°C \leq T_A \leq 85°C$
Storage Temperature (Ambient) ..... $-65°C \leq T_A \leq +125°C$
Power Dissipation ..... 1 Watt
Short Circuit Output Current ..... 50 mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

READ OPERATION

RECOMMENDED DC OPERATING CONDITIONS

($-40°C \leq T_A \leq 85°C$)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{IH}	Input High Voltage	2.0		$V_{CC}+1$	V	
V_{IL}	Input Low Voltage	-0.1		0.8	V	

DC ELECTRICAL CHARACTERISTICS[1,2,4,8]

($-40°C \leq T_A \leq 85°C$) (V_{CC} = +5 V ± 5%, $V_{PP} = V_{CC}$)[2]

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
I_{CC1}	V_{CC} Standby Power Supply Current ($\overline{OE} = V_{IL}$; CE = V_{IH})		10	30	mA	2
I_{CC2}	V_{CC} Active Power Supply Current ($\overline{OE} = \overline{CE} = V_{IL}$)		57	115	mA	2
I_{PP1}	V_{PP} Current (V_{PP} = 5.25 V)			10	mA	2
V_{OH}	Output High Voltage (I_{OH} = -400 μA)	2.4			V	
V_{OL}	Output Low Voltage (I_{OL} = 2.1mA)			.45	V	
I_{IL}	Input Leakage Current (V_{IN} = 5.25 V)			10	μA	
I_{OL}	Output Leakage Current (V_{OUT} = 5.25 V)			10	μA	

AC ELECTRICAL CHARACTERISTICS[1,2,5]

($-40°C \leq T_A \leq 85°C$) (V_{CC} = +5 V ± 5%, $V_{PP} = V_{CC}$)[2]

SYM	PARAMETER	-77		-78		UNITS	NOTES
		MIN	MAX	MIN	MAX		
t_{ACC}	Address to Output Delay ($\overline{CE} = \overline{OE} = V_{IL}$)		390		450	ns	
t_{CE}	CE to Output Delay ($\overline{OE} = V_{IL}$)		390		450	ns	5
t_{OE}	Output Enable to Output Delay ($\overline{CE} = V_{IL}$)		150		150	ns	9
t_{DF}	Chip Deselect to Output Float ($\overline{CE} = V_{IL}$)	0	130	0	130	ns	8
t_{OH}	Address to Output Hold ($\overline{CE} = \overline{OE} = V_{IL}$)	0		0		ns	

RECOMMENDED AC OPERATING CONDITIONS AND ELECTRICAL CHARACTRISTICS[1,2,6,7]

(T_A = 25°C ± 5°C) (V_{CC} = +5V ± 5%, V_{PP} = 25V ± 1V)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
t_{AS}	Address Setup Time	2			µs	
t_{OES}	$\overline{OE}$ Setup Time	2			µs	
t_{DS}	Data Setup Time	2			µs	
t_{AH}	Address Hold Time	2			µs	
t_{OEH}	$\overline{OE}$ Hold Time	2			µs	
t_{DH}	Data Hold Time	2			µs	
t_{DF}	Output Enable to Output Float	0		130	ns	4
t_{OE}	Output Enable to Output Delay			120	ns	4
t_{PW}	Program Pulse Width	45	50	55	ms	
t_{PRT}	Program Pulse Rise Time	5			ns	
t_{PFT}	Program Pulse Fall Time	5			ns	

PROGRAM OPERATION NOTES:

1. V_{CC} must be applied at the same time or before V_{PP} and removed after or at the same time as V_{PP}. To prevent damage to the device it must not be inserted into a board with V_{PP} at 25V.
2. Care must be taken to prevent overshoot of the V_{PP} supply when switching to -25V.
3. $0.45V \leq V_{IN} \leq 5.25V$
4. $\overline{CE}$/PGM – V_{IL}
5. $\overline{CE}$/PGM – V_{IH}
6. t_T – 20nsec
7. 1V or 2V for inputs and 8V or 2V for outputs are used as timing reference levels.
8. Although speed selections are made for read operation all programming specifications are the same for all dash numbers.

MKI INDUSTRIAL HI-REL SCREENING

Figure 3

	Screen	MIL-STD 883 Method	Reqmt.
Package Assembly	Die Inspect Pre-Seal Inspect	75X Mostek Spec. 30X-60X Mostek Spec.	100% 100%
Environmental	Temperature Cycle Centrifuge Fine Leak Gross Leak	1010 Cond. C, 5 Cycles 2001 Cond. D, 20Kg Y_1 1014 Cond. B, 1 X 10^{-7} atm cc/sec Mostek Spec.	100% 100% 100% 100%
Electrical	Electrical Screens	5005 Grp. A electrical sub-groups, testing conditions and limits which guarantee ac, dc and functional performance over the full temperature range.	100%
Voltage Stress (DRAMs only)		1015 Cond. D, 10 hrs. min., 125°C	100%
Burn-in		1015 Cond. D, 44 hrs. min., 125°C	100%
QA Acceptance	Hermeticity Electrical Tests Visual/Mechanical Solderability Pre-shipment Inspect	Fine and gross leak samples 5005 Grp. A sample testing to guarantee performance to data sheet over full temp. range. Visual tests to guarantee marking, construction and mechanical integrity	.25% AQL .4% AQL .65% AQL LTPD 10 .65% AQL

CAPACITANCE

(T_A = 25°C) [8]

SYM	PARAMETER	TYP	MAX	UNITS	NOTES
C_{IN}	Input Capacitance	4	6	pF	6
C_{OUT}	Output Capacitance	8	12	pF	6

READ OPERATION NOTES:

1. V_{CC} must be applied on or before V_{PP} and removed after or at the same time as V_{PP}.
2. V_{PP} and V_{CC} may be connected together except during programming, in which case the supply current is the sum of I_{CC} and I_{PP1}.
3. All voltages with respect to V_{SS}.
4. Load conditions = I_{TTL} load and 100pF., tr = tF = 20ns, reference levels are 1V and 2V for inputs and .8V and 2V for outputs.
5. t_{OE} is referenced to $\overline{CE}$ or the addresses, whichever occurs last.
6. Effective Capacitance calculated from the equation $C = \frac{\Delta Q}{\Delta V}$ where $\Delta V = 3V$.
7. Typical numbers are for T_A = 25°C and V_{CC} = 5.0 V.
8. t_{DF} is applicable to both $\overline{CE}$ and $\overline{OE}$, whichever occurs first.
9. OE may follow up to t_{ACC}-t_{OE} after the falling edge of $\overline{CE}$ without effecting t_{ACC}.

PROGRAM OPERATION[8]

RECOMMENDED DC OPERATING CONDITIONS[8]

(T_A = 25°C ± 5°C) (V_{CC} = +5V ± 5%, V_{PP} = 25V ± 1V)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
V_{IL}	Input Low Level	-0.1	0.8	V	
V_{IH}	Input High Level	2.0	V_{CC} + 1	V	

DC ELECTRICAL CHARACTERISTICS

(T_A = 25°C ± 5°C) (V_{CC} = +5V ± 5%, V_{PP} = 25V ± 1V)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
I_{IL}	Input Leakage Current		10	μA	3
I_{CC}	V_{CC} Power Supply Current		100	mA	
I_{PP1}	V_{PP} Supply Current		10	mA	4
I_{PP2}	V_{PP} Supply Current during Programming Pulse		30	mA	5

MOSTEK

MILITARY/HIGH-REL PRODUCTS

Extended Temperature, Extended Burn-In Industrial Processing

Z80/Z80A Central Processing Unit

MKI3880-70/74

FEATURES

- ☐ 44 hr. min., 125°C burn-in plus industrial screening for greater reliability (see Figure 6 for processing description)
- ☐ –40°C to 85°C temperature range
- ☐ Two speeds
  - 2.5 MHz MKI3880(P)-70 (Z80 CPU)
  - 4.0 MHz MKI3880(P)-74 (Z80A CPU)
- ☐ Single 5-Volt supply and single-phase clock required
- ☐ Software compatible with 8080A CPU
- ☐ Complete development and OEM system product support
- ☐ Military MKB version available (-55°C/125°C)
- ☐ Typical power 625 mW

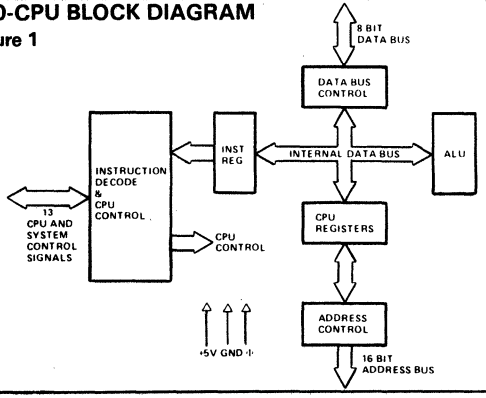
DESCRIPTION

The Mostek Z80 family of components is a significant advancement in the state-of-art of microcomputers. These components can be configured with any type of standard semiconductor memory to generate computer systems with an extremely wide range of capabilities. For example, as few as two LSI circuits and three standard TTL MSI packages can be combined to form a simple controller. With additional memory and I/O devices, a computer can be constructed with capabilities that only a minicomputer could deliver previously. This wide range of computational power allows standard modules to be constructed by a user that can satisfy the requirements of an extremely wide range of applications.

The CPU is the heart of the system. Its function is to obtain instructions from the memory and perform the desired operations. The memory is used to contain instructions and, in most cases, data that is to be processed. For example, a typical instruction sequence may be to read data from a specific peripheral device, store it in a location in memory, check the parity, and write it out to another peripheral device. Note that the Mostek component set includes the CPU and various general purpose I/O device controllers, as well as a wide range of memory devices. Thus, all required components can be connected together in a very simple manner with virtually no other external logic. The user's effort then becomes primarily one of the software development. That is, the user can concentrate on describing his problem and translating it into a series of instructions that can be loaded into the microcomputer memory. Mostek is dedicated to making this step of software generation as simple as possible. A good example of this is our assembly language in which a simple mnemonic is used to represent every instruction that the CPU can perform. This language is self-documenting in such a way that from the mnemonic the user can understand exactly what the instruction is doing without constantly checking back to a complex cross listing. Please refer to the Z80 Data Book for extensive Z80 operation documentation.

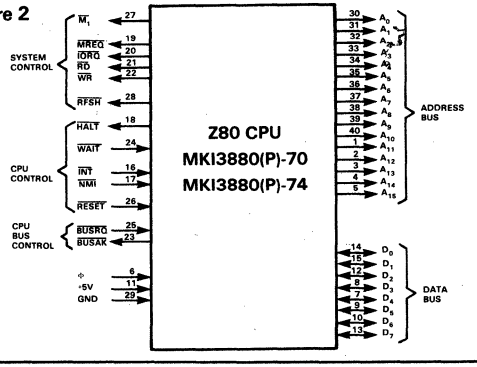
Z80-CPU BLOCK DIAGRAM

Figure 1



Z80 PIN CONNECTIONS

Figure 2



XIV

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... -40°C to +85°C
Storage Temperature ..... -65°C to +150°C
Voltage on Any Pin with Respect to Ground ..... -0.3 V to +7 V
Power Dissipation ..... 1.5 W

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(T_A = -40°C to 85°C, V_{CC} = 5 V ± 5% unless otherwise specified)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
V_{ILC}	Clock Input Low Voltage	-0.3		0.8	V	
V_{IHC}	Clock Input High Voltage	V_{CC}-.6		V_{CC}+.3	V	
V_{IL}	Input Low Voltage	-0.3		0.8	V	
V_{IH}	Input High Voltage All inputs except NMI	2.4		V_{CC}	V	
$V_{IH(NMI)}$	Input High Voltage (NMI)	2.7		V_{CC}	V	

DC ELECTRICAL CHARACTERISTICS

(T_A = -40°C to 85°C, V_{CC} = 5 V ± 5% unless otherwise specified)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 1.8mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = -250 μA
I_{CC}	Power Supply Current			200	mA	
I_{LI}	Input Leakage Current			±10	μA	V_{IN} = 0 to V_{CC}
I_{LOH}	Tri-State Output Leakage Current in Float			10	μA	V_{OUT} = 2.4 to V_{CC}
I_{LOL}	Tri-State Output Leakage Current in Float			-10	μA	V_{OUT} = 0.4V
I_{LD}	Data Bus Leakage Current In Input Mode			±10	μA	$0 < V_{IN} < V_{CC}$

AC ELECTRICAL CHARACTERISTICS

MKI3880(P)-70 Z80-CPU

(T_A = -40°C to 85°C, V_{CC} = +5 V, ±5%, Unless Otherwise Noted)

SIGNAL	SYM	PARAMETER	MIN	MAX	UNIT	TEST CONDITIONS
Φ	t_c	Clock Period	.4	[12]	μsec	
	$t_w(\Phi H)$	Clock Pulse Width, Clock High	180	(D)	nsec	
	$t_w(\Phi L)$	Clock Pulse Width, Clock Low	180	2000	nsec	
	t_r, f	Clock Rise and Fall Time		30	nsec	
A_{0-15}	$t_{D(AD)}$	Address Output Delay		145	nsec	
	$t_{F(AD)}$	Delay to Float		110	nsec	
	t_{acm}	Address Stable Prior to $\overline{MREQ}$ (Memory Cycle)	[1]		nsec	C_L = 50pF
	t_{aci}	Address Stable Prior to $\overline{IORQ}$, $\overline{RD}$ or $\overline{WR}$ (I/O Cycle)	[2]		nsec	
	t_{ca}	Address Stable From $\overline{RD}$, $\overline{WR}$, $\overline{IORQ}$ or $\overline{MREQ}$	[3]		nsec	Except T3-M1
	t_{caf}	Address Stable From $\overline{RD}$ or $\overline{WR}$ During Float	[4]		nsec	
D_{0-7}	$t_{D(D)}$	Data Output Delay		250	nsec	
	$t_{F(D)}$	Delay to Float During Write Cycle		90	nsec	
	$t_{S\Phi(D)}$	Data Setup Time to Rising Edge of Clock During M1 Cycle	50		nsec	
	$t_{S\overline{\Phi}(D)}$	Data Setup Time to Falling Edge at Clock During M2 to M5	60		nsec	C_L = 50pF
	t_{dcm}	Data Stable Prior to $\overline{WR}$ (Memory Cycle)	[5]		nsec	
	t_{dci}	Data Stable Prior to $\overline{WR}$ (I/O Cycle)	[6]		nsec	
	t_{cdf}	Data Stable From $\overline{WR}$	[7]		nsec	
	t_H	Input Hold Time	0		nsec	
$\overline{MREQ}$	$t_{DL\overline{\Phi}(MR)}$	$\overline{MREQ}$ Delay From Falling Edge of Clock, $\overline{MREQ}$ Low		100	nsec	
	$t_{DH\Phi(MR)}$	$\overline{MREQ}$ Delay From Rising Edge of Clock, $\overline{MREQ}$ High		100	nsec	
	$t_{DH\overline{\Phi}(MR)}$	$\overline{MREQ}$ Delay From Falling Edge of Clock, $\overline{MREQ}$ High		100	nsec	C_L = 50pF
	$t_{w(\overline{MRL})}$	Pulse Width, $\overline{MREQ}$ Low	[8]		nsec	
	$t_{w(\overline{MRH})}$	Pulse Width, $\overline{MREQ}$ High	[9]		nsec	
$\overline{IORQ}$	$t_{DL\Phi(IR)}$	$\overline{IORQ}$ Delay From Rising Edge of Clock, $\overline{IORQ}$ Low		90	nsec	
	$t_{DL\overline{\Phi}(IR)}$	$\overline{IORQ}$ Delay From Falling Edge of Clock, $\overline{IORQ}$ Low		110	nsec	C_L = 50pF
	$t_{DH\Phi(IR)}$	$\overline{IORQ}$ Delay From Rising Edge of Clock, $\overline{IORQ}$ High		100	nsec	
	$t_{DH\overline{\Phi}(IR)}$	$\overline{IORQ}$ Delay From Falling Edge of Clock, $\overline{IORQ}$ High		110	nsec	
$\overline{RD}$	$t_{DL\Phi(RD)}$	$\overline{RD}$ Delay From Rising Edge of Clock, $\overline{RD}$ Low		100	nsec	
	$t_{DL\overline{\Phi}(RD)}$	$\overline{RD}$ Delay From Falling Edge of Clock, $\overline{RD}$ Low		130	nsec	C_L = 50pF
	$t_{DH\Phi(RD)}$	$\overline{RD}$ Delay From Rising Edge of Clock, $\overline{RD}$ High		100	nsec	
	$t_{DH\overline{\Phi}(RD)}$	$\overline{RD}$ Delay From Falling Edge of Clock, $\overline{RD}$ High		110	nsec	

AC ELECTRICAL CHARACTERISTICS (Cont.)

(T_A = -40°C to 85°C, V_{CC} = +5 V, ± 5%, unless otherwise noted)

SIGNAL	SYM	PARAMETER	MIN	MAX	UNIT	TEST CONDITIONS
$\overline{WR}$	$t_{DL\Phi(WR)}$	$\overline{WR}$ Delay From Rising Edge of Clock, $\overline{WR}$ Low		80	nsec	C_L = 50pF
	$t_{DL\overline{\Phi}(WR)}$	$\overline{WR}$ Delay From Falling Edge of Clock, $\overline{WR}$ Low		90	nsec	
	$t_{DH\Phi(WR)}$	$\overline{WR}$ Delay From Falling Edge of Clock, $\overline{WR}$ High		100	nsec	
	$t_{W(\overline{WRL})}$	Pulse Width, $\overline{WR}$ Low	[10]		nsec	
$\overline{M1}$	$t_{DL(M1)}$	$\overline{M1}$ Delay From Rising Edge of Clock $\overline{M1}$ Low		130	nsec	C_L = 50pF
	$t_{DH(M1)}$	$\overline{M1}$ Delay From Rising Edge of Clock, $\overline{M1}$ High		130	nsec	
$\overline{RFSH}$	$t_{DL(RF)}$	$\overline{RFSH}$ Delay From Rising Edge of Clock, $\overline{RFSH}$ Low		180	nsec	C_L = 30pF
	$t_{DH(RF)}$	$\overline{RFSH}$ Delay From Rising Edge of Clock $\overline{RFSH}$ High		150	nsec	
$\overline{WAIT}$	$t_{S(WT)}$	$\overline{WAIT}$ Setup Time to Falling Edge of Clock	70		nsec	
$\overline{HALT}$	$t_{D(HT)}$	$\overline{HALT}$ Delay Time From Falling Edge of Clock		300	nsec	C_L = 50pF
$\overline{INT}$	$t_{s(IT)}$	$\overline{INT}$ Setup Time to Rising Edge of Clock	80		nsec	
$\overline{NMI}$	$t_{w(\overline{NML})}$	Pulse Width, $\overline{NMI}$ Low	80		nsec	
$\overline{BUSRQ}$	$t_{s(BQ)}$	$\overline{BUSRQ}$ Setup Time to Rising Edge of Clock	80		nsec	
$\overline{BUSAK}$	$t_{DL(BA)}$	$\overline{BUSAK}$ Delay From Rising Edge of Clock, $\overline{BUSAK}$ Low		120	nsec	C_L = 50pF
	$t_{DH(BA)}$	$\overline{BUSAK}$ Delay From Falling Edge of Clock, $\overline{BUSAK}$ High		110	nsec	
$\overline{RESET}$	$t_{s(RS)}$	$\overline{RESET}$ Setup Time to Rising Edge of Clock	90		nsec	
	$t_{F(C)}$	Delay to/from Float ($\overline{MREQ}$, $\overline{IORQ}$, $\overline{RD}$ and $\overline{WRI}$)		80	nsec	
	t_{mr}	$\overline{M1}$ Stable Prior to $\overline{IORQ}$ (Interrupt Ack.)	[11]		nsec	

NOTES:

A. Data should be enabled onto the CPU data bus when RD is active. During interrupt acknowledge data should be enabled when $\overline{M1}$ and $\overline{IORQ}$ are both active.

B. The $\overline{RESET}$ signal must be active for a minimum of 3 clock cycles.

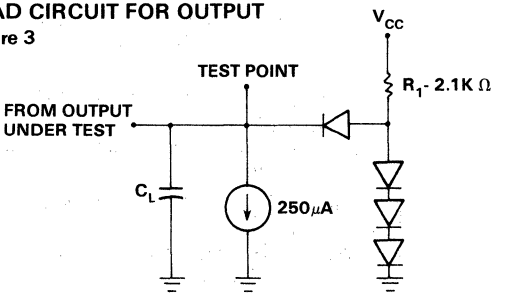
C. Output Delay vs. Load Capacitance
T_A = 85°C V_{CC} = 5V ± 5%
Add 10 nsec delay for each 50pF increase in load up to a maximum of 200pF for the data bus and 100pF for address and control lines.

D. Although static by design, testing guarantees t_W (ΦH) of 200 μsec maximum.

[1] $t_{acm} = t_W(\Phi H) + t_f - 75$
[2] $t_{aci} = t_c - 80$
[3] $t_{ca} = t_W(\Phi L) + t_r - 40$
[4] $t_{caf} = t_W(\Phi L) + t_r - 60$
[5] $t_{dcm} = t_c - 210$
[6] $t_{dci} = t_W(\Phi L) + t_r - 210$
[7] $t_{cdf} = t_W(\Phi L) + tr - 80$
[8] $t_W(\overline{MRL}) = t_c - 40$
[9] $t_W(\overline{MRH}) = t_W(\Phi H) + t_f - 70$
[10] $t_W(\overline{WR}) = t_c - 40$
[11] $t_{mr} = 2t_c + t_W(\Phi H) + t_f - 80$
[12] $t_c = t_W(\Phi H) + t_W(\Phi L) + t_r + t_f$

LOAD CIRCUIT FOR OUTPUT

Figure 3



AC ELECTRICAL CHARACTERISTICS

MKI3880(P)-74 Z80A-CPU

(T_A = -40°C to 85°C, V_{CC} = +5V, ±5%, Unless Otherwise Noted)

SIGNAL	SYM	PARAMETER	MIN	MAX	UNIT	TEST CONDITIONS
Φ	t_c	Clock Period	.25	[12]	μsec	
	$t_w(\Phi H)$	Clock Pulse Width, Clock High	110	(D)	nsec	
	$t_w(\Phi L)$	Clock Pulse Width, Clock Low	110	2000	nsec	
	t_r, f	Clock Rise and Fall Time		30	nsec	
A_{0-15}	$t_{D(AD)}$	Address Output Delay		110	nsec	
	$t_{F(AD)}$	Delay to Float		90	nsec	
	t_{acm}	Address Stable Prior to $\overline{MREQ}$ (Memory Cycle)	[1]		nsec	C_L = 50pF
	t_{aci}	Address Stable Prior to $\overline{IORQ}$, $\overline{RD}$ or $\overline{WR}$ (I/O Cycle)	[2]		nsec	
	t_{ca}	Address Stable From $\overline{RD}$, $\overline{WR}$, $\overline{IORQ}$ or $\overline{MREQ}$	[3]		nsec	Except T3-M1
	t_{caf}	Address Stable From $\overline{RD}$ or $\overline{WR}$ During Float	[4]		nsec	
D_{0-7}	$t_{D(D)}$	Data Output Delay		170	nsec	
	$t_{F(D)}$	Delay to Float During Write Cycle		90	nsec	
	$t_{S\Phi(D)}$	Data Setup Time to Rising Edge of Clock During M1 Cycle	35		nsec	
	$t_{S\overline{\Phi}(D)}$	Data Setup Time to Falling Edge at Clock During M2 to M5	50		nsec	C_L = 50pF
	t_{dcm}	Data Stable Prior to $\overline{WR}$ (Memory Cycle)	[5]		nsec	
	t_{dci}	Data Stable Prior to $\overline{WR}$ (I/O Cycle)	[6]		nsec	
	t_{cdf}	Data Stable From $\overline{WR}$	[7]		nsec	
	t_H	Input Hold Time	0		nsec	
$\overline{MREQ}$	$t_{DL\overline{\Phi}(MR)}$	$\overline{MREQ}$ Delay From Falling Edge of Clock, $\overline{MREQ}$ Low	20	85	nsec	
	$t_{DH\Phi(MR)}$	$\overline{MREQ}$ Delay From Rising Edge of Clock, $\overline{MREQ}$ High		85	nsec	
	$t_{DH\overline{\Phi}(MR)}$	$\overline{MREQ}$ Delay From Falling Edge of Clock, $\overline{MREQ}$ High		85	nsec	C_L = 50pF
	$t_{w(\overline{MRL})}$	Pulse Width, $\overline{MREQ}$ Low	[8]		nsec	
	$t_{w(\overline{MRH})}$	Pulse Width, $\overline{MREQ}$ High	[9]		nsec	
$\overline{IORQ}$	$t_{DL\Phi(IR)}$	$\overline{IORQ}$ Delay From Rising Edge of Clock, $\overline{IORQ}$ Low		75	nsec	
	$t_{DL\overline{\Phi}(IR)}$	$\overline{IORQ}$ Delay From Falling Edge of Clock, $\overline{IORQ}$ Low		85	nsec	C_L = 50pF
	$t_{DH\overline{\Phi}(IR)}$	$\overline{IORQ}$ Delay From Rising Edge of Clock, $\overline{IORQ}$ High		85	nsec	
	$t_{DH\Phi(IR)}$	$\overline{IORQ}$ Delay From Falling Edge of Clock, $\overline{IORQ}$ High		85	nsec	
$\overline{RD}$	$t_{DL\Phi(RD)}$	$\overline{RD}$ Delay From Rising Edge of Clock, $\overline{RD}$ Low		85	nsec	
	$t_{DL\overline{\Phi}(RD)}$	$\overline{RD}$ Delay From Falling Edge of Clock, $\overline{RD}$ Low		95	nsec	C_L = 50pF
	$t_{DH\Phi(RD)}$	$\overline{RD}$ Delay From Rising Edge of Clock, $\overline{RD}$ High		85	nsec	
	$t_{DH\overline{\Phi}(RD)}$	$\overline{RD}$ Delay From Falling Edge of Clock, $\overline{RD}$ High		85	nsec	

AC ELECTRICAL CHARACTERISTICS (Cont.)

(T_A = -40°C to 85°C, V_{CC} = +5 V, ± 5%, unless otherwise noted)

SIGNAL	SYM	PARAMETER	MIN	MAX	UNIT	TEST CONDITIONS
	$t_{DL\Phi(WR)}$	$\overline{WR}$ Delay From Rising Edge of Clock, $\overline{WR}$ Low		65	nsec	
$\overline{WR}$	$t_{DL\Phi(WR)}$	$\overline{WR}$ Delay From Falling Edge of Clock, $\overline{WR}$ Low		80	nsec	C_L = 50pF
	$t_{DH\Phi(WR)}$	$\overline{WR}$ Delay From Falling Edge of Clock, $\overline{WR}$ High		80	nsec	
	$t_{w(\overline{WRL})}$	Pulse Width, $\overline{WR}$ Low	[10]		nsec	
$\overline{M1}$	$t_{DL(M1)}$	$\overline{M1}$ Delay From Rising Edge of Clock $\overline{M1}$ Low		100	nsec	C_L = 50pF
	$t_{DH(M1)}$	$\overline{M1}$ Delay From Rising Edge of Clock, $\overline{M1}$ High		100	nsec	
$\overline{RFSH}$	$t_{DL(RF)}$	$\overline{RFSH}$ Delay From Rising Edge of Clock, $\overline{RFSH}$ Low		130	nsec	C_L = 50pF
	$t_{DH(RF)}$	$\overline{RFSH}$ Delay From Rising Edge of Clock $\overline{RFSH}$ High		120	nsec	
$\overline{WAIT}$	$t_{S(WT)}$	$\overline{WAIT}$ Setup Time to Falling Edge of Clock	70		nsec	
$\overline{HALT}$	$t_{D(HT)}$	$\overline{HALT}$ Delay Time From Falling Edge of Clock		300	nsec	C_L = 50pF
$\overline{INT}$	$t_{s(IT)}$	$\overline{INT}$ Setup Time to Rising Edge of Clock	80		nsec	
$\overline{NMI}$	$t_{w(\overline{NML})}$	Pulse Width, $\overline{NMI}$ Low	80		nsec	
$\overline{BUSRQ}$	$t_{s(BQ)}$	$\overline{BUSRQ}$ Setup Time to Rising Edge of Clock	50		nsec	
$\overline{BUSAK}$	$t_{DL(BA)}$	$\overline{BUSAK}$ Delay From Rising Edge of Clock, $\overline{BUSAK}$ Low		100	nsec	C_L = 50pF
	$t_{DH(BA)}$	$\overline{BUSAK}$ Delay From Falling Edge of Clock, $\overline{BUSAK}$ High		100	nsec	
$\overline{RESET}$	$t_{s(RS)}$	$\overline{RESET}$ Setup Time to Rising Edge of Clock	60		nsec	
	$t_{F(C)}$	Delay to/From Float ($\overline{MREQ}$, $\overline{IORQ}$, $\overline{RD}$ and $\overline{WR}$)		80	nsec	
	t_{mr}	$\overline{M1}$ Stable Prior to $\overline{IORQ}$ (Interrupt Ack.)	[11]		nsec	

NOTES:

A. Data should be enabled onto the CPU data bus when $\overline{RD}$ is active. During interrupt acknowledge data should be enabled when $\overline{M1}$ and $\overline{IORQ}$ are both active.

B. The $\overline{RESET}$ signal must be active for a minimum of 3 clock cycles.

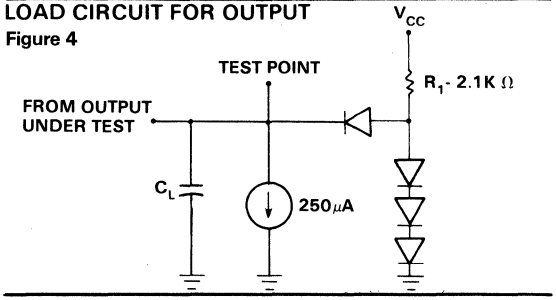
C. Output Delay vs. Load Capacitance
T_A = 85°C V_{CC} = 5V ± 5%
Add 10 nsec delay for each 50pF increase in load up to a maximum of 200pF for the data bus and 100pF for address and control lines.

D. Although static by design, testing guarantees t_w (ΦH) of 200 μsec maximum.

[1] $t_{acm} = t_w(\Phi H) + t_f - 65$
[2] $t_{aci} = t_c - 70$
[3] $t_{ca} = t_w(\Phi L) + t_r - 50$
[4] $t_{caf} = t_w(\Phi L) + t_r - 45$
[5] $t_{dcm} = t_c - 170$
[6] $t_{dci} = t_w(\Phi L) + t_r - 170$
[7] $t_{cdf} = t_w(\Phi L) + t_r - 70$
[8] $t_w(\overline{MRL}) = t_c - 30$
[9] $t_w(\overline{MRH}) = t_w(\Phi H) + t_f - 40$
[10] $t_w(\overline{WR}) = t_c - 30$
[11] $t_{mr} = 2t_c + t_w(\Phi H) + t_f - 65$
[12] $t_c = t_w(\Phi H) + t_w(\Phi L) + t_r + t_f$

LOAD CIRCUIT FOR OUTPUT

Figure 4



CAPACITANCE

T_A = 25°C, f = 1 MHz

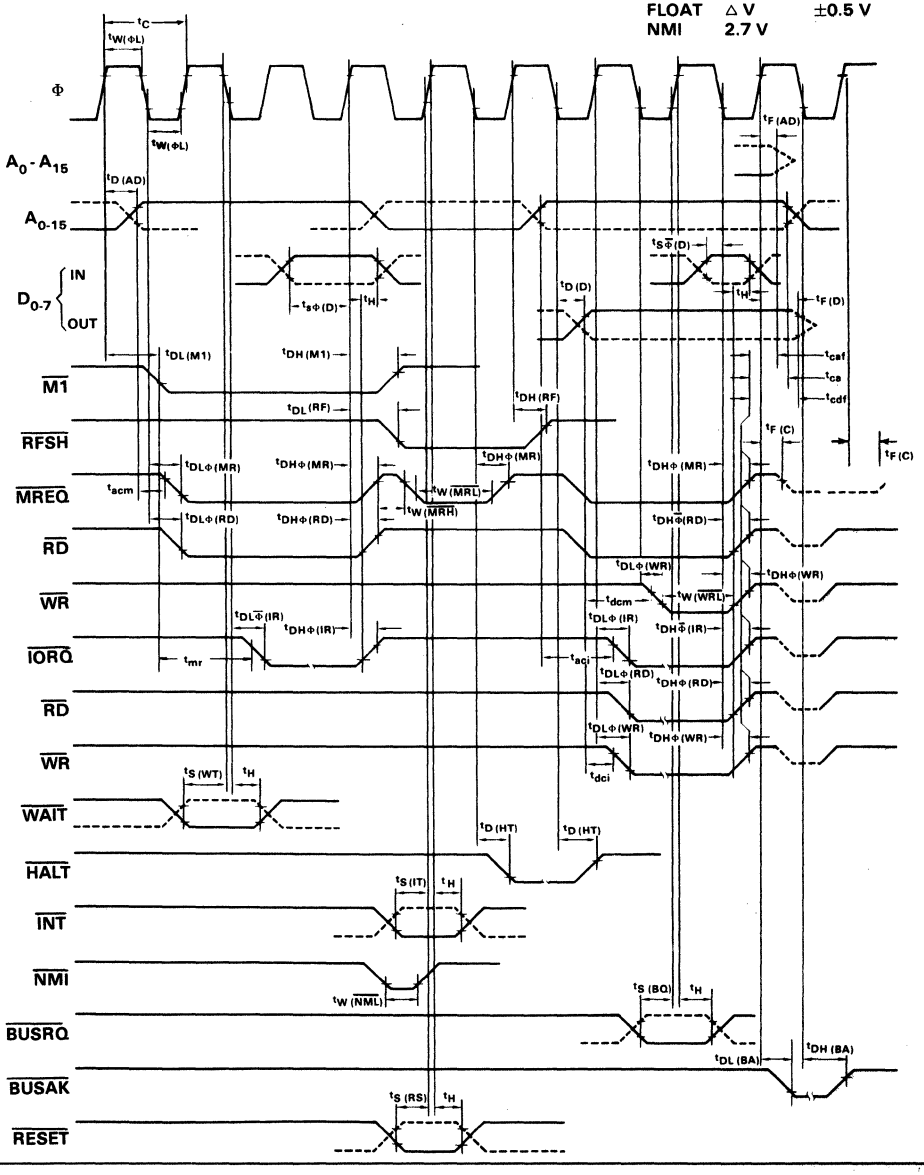
SYM	PARAMETER	MAX	UNIT	TEST CONDITIONS
$C\Phi$	Clock Capacitance	35	pF	Unmeasured Pins
C_{IN}	Input Capacitance	5	pF	Returned to Ground
C_{OUT}	Output Capacitance	10	pF	

AC TIMING DIAGRAM

Figure 5

Timing measurements are made at the following voltages, unless otherwise specified.

	"1"	"0"
CLOCK	V_{CC}—.6	.8 V
OUTPUT	2.0 V	.8 V
INPUT	2.4 V	.8 V
FLOAT	Δ V	±0.5 V
NMI	2.7 V	



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MKI INDUSTRIAL HI-REL SCREENING

Figure 6

	Screen	MIL-STD 883 Method	Reqmt.
Package Assembly	Die Inspect Pre-Seal Inspect	75X Mostek Spec. 30X-60X Mostek Spec.	100% 100%
Environmental	Temperature Cycle Centrifuge Fine Leak Gross Leak	1010 Cond. C, 5 Cycles 2001 Cond. D, 20Kg Y_1 1014 Cond. B, 1 X 10^{-7} atm cc/sec Mostek Spec.	100% 100% 100% 100%
Electrical	Electrical Screens	5005 Grp. A electrical sub-groups, testing conditions and limits which guarantee ac, dc and functional performance over the full temperature range.	100%
Voltage Stress (DRAMs only)		1015 Cond. D, 10 hrs. min., 125°C	100%
Burn-in		1015 Cond. D, 44 hrs. min., 125°C	100%
QA Acceptance	Hermeticity Electrical Tests Visual/Mechanical Solderability Pre-shipment Inspect.	Fine and gross leak samples 5005 Grp. A sample testing to guarantee performance to data sheet over full temp. range. Visual tests to guarantee marking, construction and mechanical integrity	.25% AQL .4% AQL .65% AQL LTPD 10 .65% AQL

PRODUCT PREVIEW

MOSTEK®

MILITARY/HIGH-REL PRODUCTS

Extended Temperature, Extended Burn-in Industrial Processing

Parallel I/O Controller

MKI3881-70/74

FEATURES

- Two independent 8 bit bidirectional peripheral interface ports with 'handshake' data transfer control
- Interrupt driven 'handshake' for fast response
- Any one of four distinct modes of operation may be selected for a port including:
  - Byte output
  - Byte input
  - Byte bidirectional bus (Available on Port A only)
  - Bit control mode

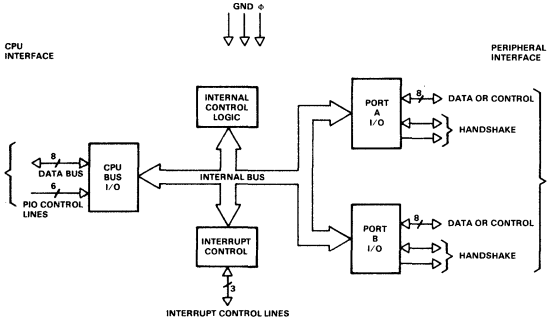
  All with interrupt controlled handshake
- Daisy chain priority interrupt logic included to provide for automatic interrupt vectoring without external logic
- Eight outputs are capable of driving Darlington transistors
- –40°C to +85°C operating range
- 44 hour Mil Spec burn in
- MKB3881 available for military requirements per MIL-STD-883B
- Typical ordering: MKI3881P-70 2.5 MHz Z80-PIO
  MKI3881P-74 4.0 MHz Z80-PIO

DESCRIPTION

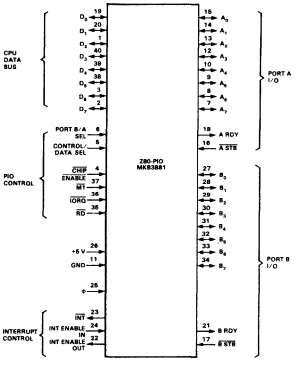
The Z80 Parallel I/O Circuit is a programmable, two port device which provides a TTL compatible interface between peripheral devices and the Z80-CPU. The CPU can configure the Z80-PIO to interface with a wide range of peripheral devices with no other external logic required. Typical peripheral devices that are fully compatible with the Z80-PIO include most keyboards, paper tape readers and punches, printers, PROM programmers, etc. The Z80-PIO utilizes N channel silicon gate depletion load technology and is packaged in a hermetic 40 pin DIP.

One of the unique features of the Z80-PIO that separates it from other interface controllers is that all data transfer between the peripheral device and the CPU is accomplished under total interrupt control. The interrupt logic of the PIO permits full usage of the efficient interrupt capabilities of the Z80-CPU during I/O transfers. All logic necessary to implement a fully nested interrupt structure is included in the PIO so that additional circuits are not required. Another unique feature of the PIO is that it can be programmed to interrupt the CPU on the occurrence of specified status conditions in the peripheral device. For example, the PIO can be programmed to interrupt if any specified peripheral alarm conditions should occur. This interrupt capability reduces the amount of time that the processor must spend in polling peripheral status.

PIO BLOCK DIAGRAM



PIO PIN CONFIGURATION



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PRODUCT PREVIEW

MOSTEK®

MILITARY/HIGH-REL PRODUCTS

Extended Temperature, Extended Burn-in Industrial Processing

Counter Timer Circuit

MKI3882 (P/J)-70/74

FEATURES

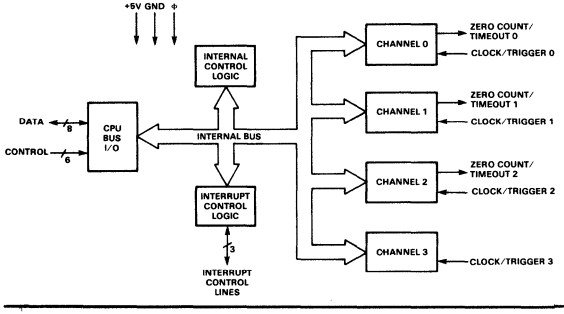
- Each channel may be selected to operate in either Counter Mode or Timer Mode
- Used in either mode, a CPU-readable Down Counter indicates number of counts-to-go until zero
- A Time Constant Register can automatically reload the Down Counter at Count Zero in Counter and Timer Mode
- Selectable positive or negative trigger initiates time operation in Timer Mode. The same input is monitored for event counts in Counter Mode
- Three channels have Zero Count/Timeout outputs capable of driving Darlington transistors
- Interrupts may be programmed to occur on the zero count condition in any channel
- Daisy chain priority interrupt logic included to provide for automatic interrupt vectoring without external logic
- –40°C to +85°C operating range
- 44 hour Mil Spec burn in
- MKB3882 available for military requirements per MIL-STD-883B
- Typical ordering: MKI3882P-70 2.5 MHz Z80-CTC
  MKI3882P-74 4.0 MHz Z80-CTC

DESCRIPTION

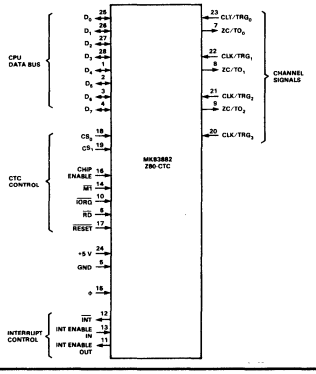
The Z80-Counter Timer Circuit (CTC) is a programmable component with four independent channels that provide counting and timing functions for microcomputer systems based on the Z80-CPU. The CPU can configure the CTC channels to operate under various modes and conditions as required to interface with a wide range of devices. In most applications, little or no external logic is required. The Z80-CTC utilizes N-channel silicon gate depletion load technology and is packaged in a 28-pin DIP. The Z80-CTC requires only a single 5 volt supply and a one-phase 5 volt clock.

A block diagram of the Z80-CTC is shown in the figure. The internal structure of the Z80-CTC consists of a Z80-CPU bus interface, Internal Control Logic, four sets of Counter/Timer Channel Logic, and Interrupt Control Logic. The four independent counter/timer channels are identified by sequential numbers from 0 to 3. The CTC has the capability of generating a unique interrupt vector for each separate channel (for automatic vectoring to an interrupt service routine). The 4 channels can be connected into four contiguous slots in the standard Z80 priority chain with channel number 0 having the highest priority. The CPU bus interface logic allows the CTC device to interface directly to the CPU with no other external logic. However, port address decoders and/or line buffers may be required for large systems.

Z80-CTC BLOCK DIAGRAM



Z80-CTC PIN CONFIGURATION



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SUPPLEMENT

MOSTEK®

MILITARY/HIGH-REL PRODUCTS

Extended Temperature, Extended Burn-In Industrial Processing

16,384 x 1-Bit Dynamic RAM

MKI4116(J)-72/73/74

FEATURES

- ☐ Extended operating temperature range (-40°C ≤ T_A ≤ +85°C)
- ☐ 44 hr. min., 125°C burn-in plus industrial screening for greater reliability (see Figure 3 for processing description)
- ☐ Recognized industry standard 16-pin configuration from Mostek
- ☐ 150 ns access time, 320 ns cycle (MKI4116-72)
  200 ns access time, 375 ns cycle (MKI4116-73)
  250 ns access time, 410 ns cycle (MKI4116-74)
- ☐ ± 10% tolerance on all power supplies (+12 V, ± 5 V)
- ☐ Low power: 462 mW active, 30 mW standby (max)
- ☐ Output data controlled by CAS and unlatched at end of cycle to allow two dimensional chip selection and extended page boundary
- ☐ Common I/O capability using "early write" operation
- ☐ Read-modify-write, RAS-only refresh, and page-mode capability
- ☐ All inputs TTL compatible, low capacitance, and protected against static charge
- ☐ 128 refresh cycles (2 msec refresh interval)
- ☐ MKB military version available (-55 to 110°C)

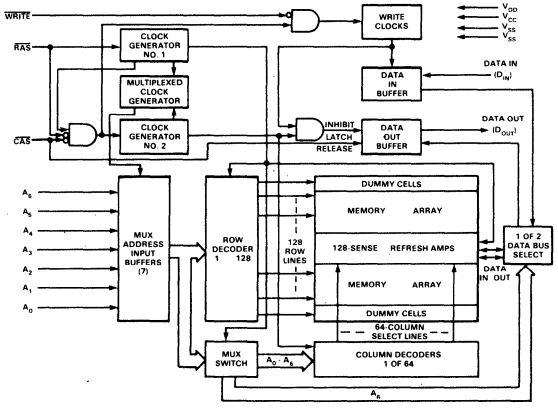
DESCRIPTION

The MKI4116 is a new generation MOS dynamic random access memory circuit organized as 16,384 words by 1 bit. As a state-of-the-art MOS memory device, the MKI4116 (16K RAM) incorporates advanced circuit techniques designed to provide wide operating margins, both internally and to the system user, while achieving performance levels in speed and power previously seen only in Mostek's high performance MK4027 (4K RAM).

The technology used to fabricate the MKI4116 is Mostek's double-poly, N-channel silicon gate, POLY I™ process. This process, coupled with the use of a single transistor dynamic storage cell, provides the maximal circuit density and reliability, while maintaining high performance capability. The use of dynamic circuitry throughout, including sense amplifiers, assures that power dissipation is minimized without any sacrifice in speed or operating margin. These factors combine to make the MKI4116 a truly superior RAM product.

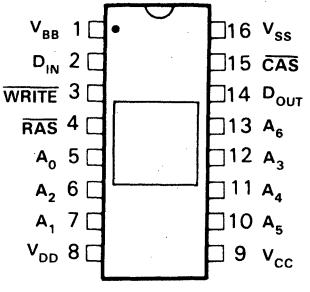
BLOCK DIAGRAM

Figure 1



PIN CONNECTIONS

Figure 2



PIN NAMES

A0 - A6	Address Inputs	WRITE	Read/Write Input
CAS	Col. Address Strobe	V_{BB}	Power (-5V)
D_{IN}	Data In	V_{CC}	Power (+5V)
D_{OUT}	Data Out	V_{DD}	Power (+12V)
RAS	Row Address Strobe	V_{SS}	Ground

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ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to V_{BB} ..... -0.5 V to +20 V
Voltage on V_{DD}, V_{CC} supplies relative to V_{SS} ..... -1.0 V to +15.0 V
V_{BB} - V_{SS} (V_{DD} - V_{SS} > 0 V) 0V
Operating Temperature, T_A (Ambient) ..... -40°C to +85°C
Storage Temperature (Ambient) ..... -65°C to +150°C
Short Circuit Output Current ..... 50 mA
Power Dissipation ..... 1 Watt

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS[6]

(-40°C ≤ T_A ≤ +85°C)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{DD}	Supply Voltage	10.8	12.0	13.2	V	2
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2,3
V_{SS}	Supply Voltage	0	0	0	V	2
V_{BB}	Supply Voltage	-4.5	-5.0	-5.5	V	2
V_{IHC}	Input High (Logic 1) Voltage, $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	2.7	—	7.0	V	2
V_{IH}	Input High (Logic 1) Voltage, all inputs except $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	2.4	—	7.0	V	2
V_{IL}	Input Low (Logic 0) Voltage, all inputs	-1.0	—	.8	V	2

DC ELECTRICAL CHARACTERISTICS

(-40°C ≤ T_A ≤ +85°C) (V_{DD} = 5.0 V ± 10%; -5.5 V ≤ V_{BB} ≤ -4.5 V; V_{SS} = 0 V)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
I_{DD1} I_{CC1} I_{BB1}	OPERATING CURRENT Average power supply operating current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = t_{RC} (min)		35 400	mA µA	4 5
I_{DD2} I_{CC2} I_{BB2}	STANDBY CURRENT Power supply standby current ($\overline{RAS}$ = V_{IHC}, D_{OUT} = High Impedance)	-10	2.25 10 200	mA µA µA	
I_{DD3} I_{CC3} I_{BB3}	REFRESH CURRENT Average power supply current, refesh mode ($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IHC}; t_{RC} = t_{RC} min)	-10	27 10 400	mA µA µA	4
I_{DD4} I_{CC4} I_{BB4}	PAGE MODE CURRENT Average power supply current, page-mode operation ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling; t_{PC} = t_{PC} min)		27 400	mA µA	4 5
$I_{I(L)}$	INPUT LEAKAGE Input leakage, any input (V_{BB} = -5 V, 0 V ≤ V_{IN} ≤ +7.0 V, all other pins not under test = 0 volts)	-10	10	µA	
$I_{O(L)}$	OUTPUT LEAKAGE Output leakage current (D_{OUT} is disabled, 0 V ≤ V_{OUT} ≤ +5.5 V)	-10	10	µA	
 V_{OH} V_{OL}	OUTPUT LEVELS Output high (Logic 1) voltage (I_{OUT} = -5 mA) Output low (Logic 0) voltage (I_{OUT} = 4.2 mA)	 2.4	 0.4	 V V	 3

RECOMMENDED AC OPERATING CONDITIONS AND ELECTRICAL CHARACTERISTICS[6,7,8]
($-40°C \leq T_A \leq 85°C$)[1] (V_{DD} = 12.0 V ± 10%; V_{CC} = 5.0 V ± 10%, V_{SS} = 0 V, $-5.5\ V \leq V_{BB} \leq -4.5\ V$)

		MKI4116-72		MKI4116-73		MKI4116-74			
SYM	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
t_{RC}	Random read or write cycle time	320		375		410		ns	9
t_{RWC}	Read-write cycle time	320		375		425		ns	9
t_{RMW}	Read-modify-write cycle time	320		405		500		ns	9
t_{PC}	Page mode cycle time	170		225		275		ns	9
t_{RAC}	Access time from $\overline{RAS}$		150		200		250	ns	10,12
t_{CAC}	Access time from $\overline{CAS}$		100		135		165	ns	11,12
t_{OFF}	Output buffer turn-off delay	0	40	0	50	0	60	ns	13
t_T	Transition time (rise and fall)	3	35	3	50	3	50	ns	8
t_{RP}	RAS precharge time	100		120		150		ns	
t_{RAS}	$\overline{RAS}$ pulse width	150	5000	200	5000	250	5000	ns	
t_{RSH}	$\overline{RAS}$ hold time	100		135		165		ns	
t_{CSH}	$\overline{CAS}$ hold time	150		200		250		ns	
t_{CAS}	$\overline{CAS}$ pulse width	100	5000	135	5000	165	5000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ delay time	20	50	25	65	35	85	ns	15
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ precharge time	0		0		0		ns	
t_{ASR}	Row Address set-up time	0		0		0		ns	
t_{RAH}	Row Address hold time	20		25		35		ns	
t_{ASC}	Column Address set-up time	0		0		0		ns	
t_{CAH}	Column Address hold time	45		55		75		ns	
t_{AR}	Column Address hold time referenced to $\overline{RAS}$	95		120		160		ns	
t_{RCS}	Read command set-up time	0		0		0		ns	
t_{RCH}	Read command hold time	0		0		0		ns	
t_{WCH}	Write command hold time	45		55		75		ns	
t_{WCR}	Write command hold time referenced to $\overline{RAS}$	95		120		160		ns	
t_{WP}	Write command pulse width	45		55		75		ns	
t_{RWL}	Write command to $\overline{RAS}$ lead time	50		70		85		ns	
t_{CWL}	Write command to $\overline{CAS}$ lead time	50		70		85		ns	
t_{DS}	Data-in set-up time	0		0		0		ns	15
t_{DH}	Date-in hold time	45		55		75		ns	15
t_{DHR}	Data-in hold time referenced to $\overline{RAS}$	95		120		160		ns	
t_{CP}	$\overline{CAS}$ precharge time (for page-mode cycle only)	60		80		100		ns	

RECOMMENDED AC OPERATING CONDITIONS AND ELECTRICAL CHARACTERISTICS (Cont.)[6,7,8]

($-40°C \leq T_A \leq +85°C$)[1] ($V_{DD}$ = 12.0 V ± 10%; V_{CC} = 5.0 V ± 10%, V_{SS} = 0 V, $-5.5\ V \leq V_{BB} \leq -4.5\ V$)

SYM	PARAMETER	MKI4116-72		MKI4116-73		MKI4116-74		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX		
t_{REF}	Refresh period		2		2		2	ms	19
t_{WCS}	$\overline{WRITE}$ command set-up time	0		0		0		ns	16
t_{CWD}	$\overline{CAS}$ to $\overline{WRITE}$ delay	60		80		90		ns	16
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ delay	110		145		175		ns	16

CAPACITANCE

($-40°C \leq T_A \leq +85°C$) ($V_{DD}$ = 12.0 V ± 10%; V_{SS} = 0 V; $-5.5\ V \leq V_{BB} \leq -4.5\ V$)

SYM	PARAMETER	TYP	MAX	UNITS	NOTES
C_{I1}	Input Capacitance (A_0 - A_6), D_{IN}	4	5	pF	17
C_{I2}	Input Capacitance, RAS, CAS, WRITE	8	10	pF	17
C_O	Output Capacitance (D_{OUT})	5	7	pF	17,18

NOTES:

1. T_A is specified here for operation at frequencies to $t_{RC} \geq t_{RC}$ (min). Operation at higher cycle rates with reduced ambient temperatures and higher power dissipation is permissible, however, provided AC operating parameters are met.
2. All voltages referenced to V_{SS}.
3. Output voltage will swing from V_{SS} to V_{CC} when activated with no current loading. For purposes of maintaining data in standby mode, V_{CC} may be reduced to V_{SS} without affecting refresh operations or data retention. However, the V_{OH} (min) specifications is not guaranteed in this mode.
4. I_{DD1}, I_{DD3}, and I_{DD4} depend on cycle rate. See Figures 2, 3 and 4 for I_{DD} limits at other cycle rates.
5. I_{CC1} and I_{CC4} depend upon output loading. During readout of high level data V_{CC} is connected through a low impedance (135 Ω typ) to data out. At all other times I_{CC} consists of leakage currents only.
6. Several cycles are required after power-up before proper device operation is achieved. Any 8 cycles which perform refresh are adequate for this purpose.
7. AC measurements assume t_T = 5 ns.
8. V_{IHC}(min) or V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IHC} or V_{IH} or V_{IL}.
9. The specifications for t_{RC} (min) t_{RMW} (min) are used only to indicate cycle which proper operation over the full temperature range ($-40°C \leq T_A \leq 85°C$) is assured.
10. Assumes that $t_{RCD} \leq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RCD} will increase by the amount that t_{RCD} exceeds the value shown.
11. Assumes that $t_{RCD} \geq t_{RCD}$ (max)
12. Measured with a load equivalent to 2 TTL loads and 100pF.
13. t_{OPI} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
14. Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met t_{RCD} (max) is specified as a reference point only, if t_{RCP} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
15. These parameters are referenced to CAS leading edge in early write cycles and to WRITE leading edge in delayed write or read-modify-write cycles.
16. t_{WCS}, t_{CWD}, and t_{RWD} are restrictive operating parameters in read-write and read-modify-write cycles only. If $t_{WCS} \leq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle. If $t_{CWD} \leq t_{CWD}$ (min) and $t_{RWD} \leq t_{RWD}$ (min), the cycle is a read-write cycle and the data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.
17. Effective capacitance calculated from the equation $C = \frac{I\Delta t}{\Delta V}$ with ΔV = 3 volts and power supplies at nominal levels.
18. CAS = V_{IHC} to disable D_{OUT}.

DESCRIPTION (Continued)

Multiplexed address inputs (a feature pioneered by Mostek for its 4K RAMs) permits the MKI4116 to be packaged in a standard 16-pin DIP. This recognized industry standard package configuration, while compatible with widely available automated testing and insertion equipment, provides highest possible system bit densities and simplifies system upgrade from 4K to 16K RAMs for new generation applications. Non-critical clock timing requirements allow use of the multiplexing technique while maintaining high performance.

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