MEMORY DATA BOOK & DESIGNERS GUIDE

MOSTEK®1978

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SHIFT REGISTERS

MOSTEK®

DUAL 128-BIT STATIC SHIFT REGISTER

MK1002(P/N)

FEATURES

☐ Ion-implanted for full TTL/DTL compatibility no interface circuitry required

☐ Single-phase, TTL/DTL compatible clocks

☐ Dual 128-bit static shift registers—256 bits total

☐ Dual sections have independent clocks

☐ Recirculate logic built in

☐ DC to 1 MHz clock rates

☐ Low power dissipation—130 mW

☐ 16-pin dual-in-line package

DESCRIPTION

The MK 1002 is a P-channel MOS static shift register utilizing low threshold-voltage processing and ion-implantation to achieve full TTL/DTL compatibility. Each of the two independent 128 bit sections has a built-in clock generator to generate three internal clock phases from a single-phase TTL-level external input. In addition, each section has input logic for loading or recirculating data within the register. (See Functional Diagram.) The positive-logic Boolean expression for this action is:

$$OUT \text{ (delayed 128 bits)} = (R_C)(D_{IN}) + (\overline{R_C})(R_{IN})$$

The Data, Recirculate Control, and Clock inputs are provided with internal pull-up resistors to V_{SS} (+5V) for use when driving from TTL. These resistors can be disabled when driving from circuitry with larger output-voltage swings, such as DTL. Enabling of pull-up resistors is accomplished by connecting the appropriate terminal to V_{GG}; disabling by connecting to V_{SS}. The Recirculate inputs are not provided with pull-up resistors since they are generally driven from MOS.

Shifting data into the register is accomplished while the Clock input is low. Output data appears following the positive-going Clock edge. Data in each register can be held indefinitely by maintaining the Clock input high.

FUNCTIONAL DIAGRAM

PIN CONNECTIONS

VR$_B$	1	16	VR$_A$
D$_{inB}$	2	15	D$_{inA}$
R$_{inB}$	3	14	R$_{inA}$
RC$_B$	4	13	RC$_A$
Out$_B$	5	12	Out$_A$
V$_{DD}$	6	11	V$_{GG}$
V$_{SS}$	7	10	VR$_\emptyset$
Clock$_B$	8	9	Clock$_A$

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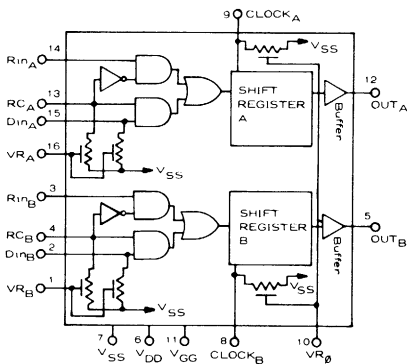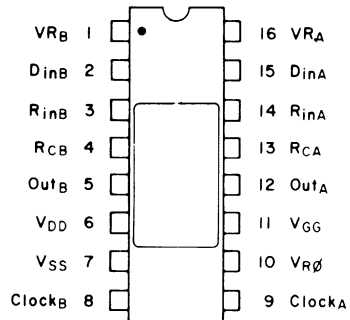
ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD} . . . . $V_{SS} - 10.0$ V
Supply Voltage, V_{GG} . . . . $V_{SS} - 20.0$ V
Voltage at any Input or Output. . . . . $V_{SS} + 0.3$ V to $V_{SS} - 10.0$ V
Operating Free-Air Temperature Range. . . . . 0°C to +75°C
Storage Temperature Range (Ceramic) . . . . −65°C to +150°C
Storage Temperature Range (Plastic). . . . . −55°C to +125°C

RECOMMENDED OPERATING CONDITIONS $(0°C \leq T_A \leq 75°C)$

		PARAMETER	MIN	TYP	MAX	UNITS	COMMENTS
POWER	V_{SS}	Supply Voltage	4.75	5.0	5.25	V	$V_{DD} = 0$ V
	V_{GG}	Supply Voltage[1]	−12.6	−12.0	−11.4	V	
INPUTS	V_{IL}	Input Voltage, Logic 0[2]		0	$V_{SS} - 4$	V	
	V_{IH}	Input Voltage, Logic 1	$V_{SS} - 1$	5.0	V_{SS}	V	
INPUT TIMING	f	Clock Repetition Rate	DC		1	MHz	
	$t_{\phi p}$	Clock Pulse Width	0.35		10	μs	
	$t_{\phi d}$	Clock Pulse Delay	0.4			μs	See
	$t_{\phi r}$	Clock Pulse Risetime	.010		0.2	μs	Timing
	$t_{\phi f}$	Clock Pulse Falltime	.010		0.2	μs	Diagram
	t_{dld}	Data Leadtime	50			ns	
	t_{dlg}	Data Lagtime	200			ns	
	t_{rld}	Recirculate Control Leadtime	100			ns	
	t_{rlg}	Recirculate Control Lagtime	300			ns	

ELECTRICAL CHARACTERISTICS

$(V_{SS} = +5 \pm 0.25V, V_{GG} = -12 \pm 0.6V, V_{DD} = 0V, T_A = 0°C$ to $+75°C$, using test circuit shown, unless otherwise noted.)

		PARAMETER	MIN	TYP[3]	MAX	UNITS	CONDITIONS
POWER	I_{SS}	Power Supply Current, V_{SS}		14	25	mA	$f_\phi = 1$ MHz Inputs & Outputs open
	I_{GG}	Power Supply Current, V_{GG}		5	10	mA	
INPUTS	C_i	Input Capacitance, any Input		3	10	pF	$V_I = V_{SS}$, f $= 1$ MHz $T_A = 25°C$
	I_{IL}	Input Current, Logic 0: Resistors Disabled[2]			−40	μA	$V_I = V_{SS} - 5V$
		Resistors Enabled[2]	−0.3		−1.6	mA	$V_I = +0.4V$
	I_{IH}	Input Current, Logic 1, Any Input			40	μA	$VR_A, VR_B, VR_\phi = V_{SS}$ $V_I = V_{SS}$
	$I_{IR(on)}$	Input Current at Recirculate Inputs[2]			−40	μA	$VR_A, VR_B, VR_\phi = V_{GG}$ $V_I = V_{SS} - 5V$
OUTPUTS	V_{OL}	Output Voltage, Logic 0 (3)			0.4	V	$I_L = -1.6$ mA
	V_{OH}	Output Voltage, Logic 1 (3)	$V_{SS} - 1$			V	$I_L = +100$ μA
DYNAMIC CHAR.	t_{DLH}	Output Delay, Low to High (3)			450	ns	See Timing
	t_{DHL}	Output Delay, High to Low (3)			450	ns	Diagram and
	t_{VOR}	Output Voltage Rise Time (3)		100	150	ns	Test
	t_{VOF}	Output Voltage Fall Time (3)		100	150	ns	Circuit

NOTES:
1. Other supply voltages are permissible providing that supply and input voltages are adjusted to maintain the same potential relative to V_{SS}, e.g., $V_{SS} = 0V$, $V_{DD} = -5 \pm 0.25V$, $V_{GG} = -17 \pm 0.85V$.
2. MOS pull-up resistors to $+5V$ are provided internally. These MOS resistors are enabled by connecting VR_A, VR_B and VR_ϕ to V_{GG}, and disabled by connecting VR_A, VR_B and VR_ϕ to V_{SS}. Pull-up resistors not provided at recirculate inputs.
3. At $T_A = 25°C$.

TIMING

$t_{\phi f}$ $t_{\phi r}$
$t_{\phi p}$ $t_{\phi d}$

CLOCK

Vss 90%
10%
1 2 128 1 2 128 1 2

t_{did} t_{dig}

Din

Vss 90%
10%

t_{rld} t_{rlg}

Rc

Vss 90%
10%

t_{DLH} t_{DHL} t_{DLH} t_{DHL}

LOGIC "1"
OUTPUT 50%
and Rin LOGIC "0"

"1" stored from Din
"0" stored from Din
"1" out from Din(dly-128)
Rin enabled
"1" stored from Rin
"0" out from Din(dly-128)
"0" stored from Rin
"1" out from Rin(dly-128)
"0" out from Rin(dly-128)
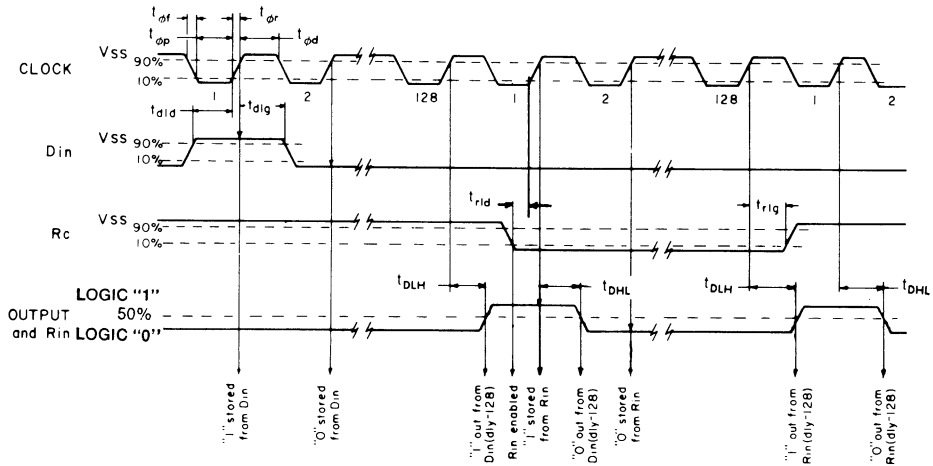
The timing diagram applies to either section of the dual shift register. The test conditions for these wave-forms are illustrated below. A logic "1" is defined as +5 V and a logic "0" is defined as 0V

As long as R_C is at a "1", R_{in} is disabled and D_{in} is enabled. The data that is present at D_{in} while the clock is at "0" is shifted in and will be stored as the clock goes to a "1" This data must have been present t_{did} time prior to the clock "1" edge. The data must also remain in that same state for t_{dig} time after that edge. These times are necessary to insure proper data storage in the first register-cell.

On the clock "1" edge, data is shifted through the register causing bit 127 to be shifted to position 128. This cell's output is buffered and appears at the output in the same logic polarity that appeared at the input 128 clocks prior. This data appears within t_{pd} time of the clock "1" edge.

R_{in} may be hardwired to the data output. When R_C is at a "0", R_{in} is enabled and D_{in} is disabled. Therefore, the output data will appear at the input of the first cell. When R_{in} is tied to the data output, the output delay will insure t_{dig} and t_{did} times. R_C "0" time must lead the clock "1" edge by t_{rld} time and must lag that edge by t_{rlg} time to insure proper data storage when recirculate storage is desired.

TEST CIRCUIT

GRD Vss

RIN VSS VDD VGG

OUT

2.9K 1%

T.P.

word pattern

DIN

VR RC CLK

MK1002P
circuit
under test

20 pF

-12 V
VDD

VSS

VDD

clock
pulse Inverters are 74 series TTL

* Includes scope and
test jig capacitance

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APPLICATIONS

This shows the MK 1002 P connected to operate as a single, 256-bit, static shift register Pull-up resistors are enabled at TTL driven inputs and disabled at MOS or DTL driven inputs Any similar TTL/DTL device may be used in place of the inverters shown

Inverters are 74-series TTL

TYPICAL PERFORMANCE

$f_\emptyset = 1 \text{MH}_Z$
$V_{SS} = 5.0 V$
$V_{DD} = 0.0 V$
$V_{GG} = -12.0 V$

$V_{SS} = 5.0V$
$V_{DD} = 0V$
$V_{GG} = -12.0V$

OPERATING NOTES

R_C	R_{in}	D_{in}	DATA ENTERED
1	X	1	1
1	X	0	0
0	1	X	1
0	0	X	0

"1" = V_{SS} = +5V
"0" = V_{DD} = Grd
 X = No Effect
Output Logic: See Description.

MOSTEK®

320-BIT DYNAMIC SHIFT REGISTER
MK1007(P/N)

FEATURES

□ Ion-Implanted for full TTL/DTL compatibility

□ Single-phase, TTL/DTL compatible clock

□ Internal pull-up resistors

□ Clock Frequency 10 kHz to 2.5 MHz

□ Built-in recirculate logic for each register

□ Power Supplies: +5V and −12V

DESCRIPTION

The MK 1007 P contains four separate 80-bit MOS dynamic shift registers on a single chip, using ion-implantation in conjunction with P-channel processing to achieve low threshold voltage and direct TTL/DTL compatibility. All logic inputs, including the single-phase Clock, can be driven directly from DTL or TTL logic. Pull-up resistors to +5V are provided for worst-case TTL inputs.

Each 80-bit register has independent inputs and outputs and a control input (RE) which allows external data to be shifted into the register (at logical 0) or data at the output to be recirculated into the register (at logical 1).

All four registers use a common (external) Clock input. With the Clock high (1), data is shifted into the registers. Following the negative-going edge of the Clock, data shifting is inhibited and output data appears. Output data is True, delayed 80 bits.

Since the MK 1007 P has zero lag-time requirements for data inputs, devices may be cascaded, i.e., the output of one device may be fed directly to the input of another device. All inputs are protected to prevent damage due to static charge accumulation.

FUNCTIONAL DIAGRAM
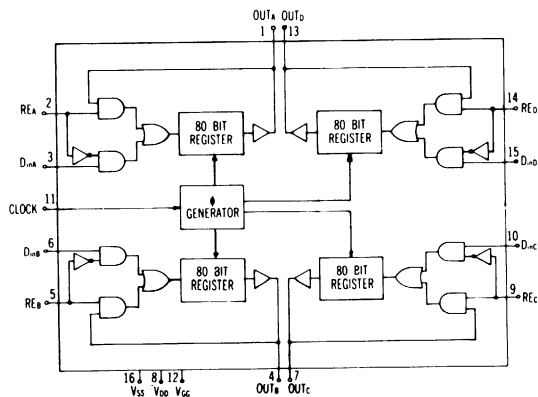
PIN CONNECTIONS
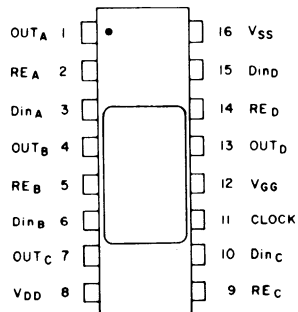
ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD} . . . . $V_{SS} + 0.3$ V to $V_{SS} - 20$ V
Supply Voltage, V_{GG} . . . . $V_{SS} + 0.3$ V to $V_{SS} - 20$ V
Voltage at any Input or Output. . . . . $V_{SS} + 0.3$ V to $V_{SS} - 20$ V
Operating Free-Air Temperature Range. . . . . 0°C to +75°C
Storage Temperature Range (Ceramic) . . . . −65°C to +150°C
Storage Temperature Range (Plastic). . . . . −55°C to +125°C

RECOMMENDED OPERATING CONDITIONS

($0°C \leq T_A \leq 75°C$)

	PARAMETER		MIN	TYP	MAX	UNITS	COMMENTS
POWER	V_{SS}	Supply Voltage	4.75	5.0	5.25	V	$V_{DD} = 0$ V
	V_{GG}	Supply Voltage[1]	−12.6	−12.0	−11.4	V	
INPUTS	V_{IL}	Logic "0" Voltage, any input		0.0	0.8	V	
	V_{IH}	Logic "1" Voltage, any input [2]	$V_{SS} - 1.5$	+5.0	V_{SS}	V	
INPUT TIMING	$f\phi$	Clock Repetition Rate	.01		2.5	MHz	NOTE: Total permitted clock times will be determined by clock frequency, $f\phi$.
	$t\phi_P$	Clock Pulse Width	.150		100	μs	
	$t\phi_d$	Clock Pulse Delay	.150		100	μs	
	$t\phi_r$	Clock Pulse Risetime	.010		5	μs	
	$t\phi_f$	Clock Pulse Falltime	.010		5	μs	
	t_{dld}	Data Leadtime	150			ns	
	t_{dlg}	Data Lagtime	0			ns	
	t_{rld}	Recirculate Control Leadtime	200			ns	
	t_{rlg}	Recirculate Control Lagtime	50			ns	

ELECTRICAL CHARACTERISTICS

($V_{SS} = +5 \pm 0.25$ V, $V_{GG} = -12 \pm 0.6$V, $V_{DD} = 0$V, $T_A = 0°C$ to $+75°C$, unless otherwise specified.)

	PARAMETER		MIN	TYP[3]	MAX	UNITS	CONDITIONS
POWER	I_{SS}	V_{SS} Power Supply Current[4][5]		22.0	40.0	mA	$f\phi = 2.5$ MHz;
	I_{GG}	V_{GG} Power Supply Current[5]		9.0	16.0	mA	outputs open
INPUTS	C_{IN}	Capacitance at Data, RE, and Clock Inputs[5]		3	6	pF	$V_I = V_{SS}, f\phi = 1$ MHz
	I_{IL}	Logic "0" Current, any input[5]	0.6	1.1	1.6	mA	$V_I = 0.4$ V
	$I_{I(lk)}$	Leakage Current, any input			1	μA	$V_I = V_{SS} - 5.5$V; $V_{SS} = V_{DD} = V_{GG}$
	R_{IN}	Input Pullup Resistance[5]	3.0		8.4	kΩ	$V_I = 0.4$ V
OUT-PUTS	V_{OL}	Logic "0" Output Voltage[5]			0.4	V	$I_L = -1.6$ mA
	V_{OH}	Logic "1" Output Voltage[5]	$V_{SS} - 1$			V	$I_L = +100$ μA
DYN. CHAR.	t_{DLH}	Output Delay, Low to High		75	200	ns	
	t_{DHL}	Output Delay, High to Low		75	200	ns	See Timing Diagrams
POWER DIS.	$P_{D(1)}$	Power Dissipation[4]		220		mW	$f\phi = 2.5$ MHz
	$P_{D(2)}$	Power Dissipation[4]		195		mW	$f\phi = 1$ MHz
	$P_{D(3)}$	Power Dissipation[4]		170		mW	$f\phi = 10$ kHz

NOTES:
(1) Other supply voltages are permissible providing that supply and input voltages are adjusted to maintain the same potential relative to V_{SS}, e.g., $V_{SS} = 0$ V, $V_{DD} = -5$V, $V_{GG} = -17$ V.
(2) Pull-up resistances to +5V are provided internally.
(3) Typical values at $T_A = 25°C$, $V_{SS} = +5.0$ V, $V_{DD} = -12.0$ V.
(4) I_{SS} will increase a maximum of 1.6 mA for each input at logic "0."
(5) At $T_A = 25°C$.
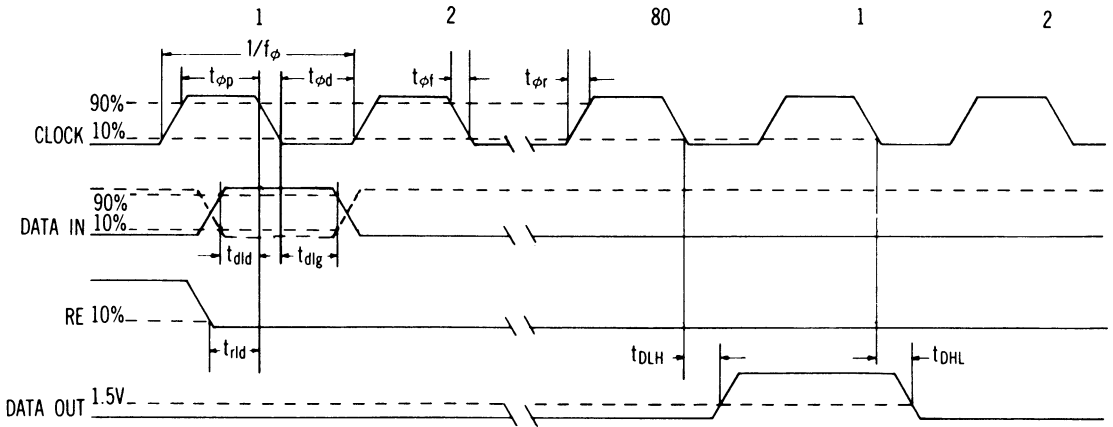
SHIFT: Fig. 1 illustrates shifting a logic 1 bit from the Data Input (D_{IN}) through one of the 80-bit registers RE (Recirculate Enable) at logic 0 enables D_{IN}. RE must go to logic 0 for t_{rid} time (Recirculate Control Leadtime) prior to the Clock's negative edge, and must maintain that state at least until the Clock's negative edge (t_{dlg}) to insure proper data shifting. This data bit entered will appear 80 clock pulses later within Output Delay Time (t_D) of that Clock's negative edge.
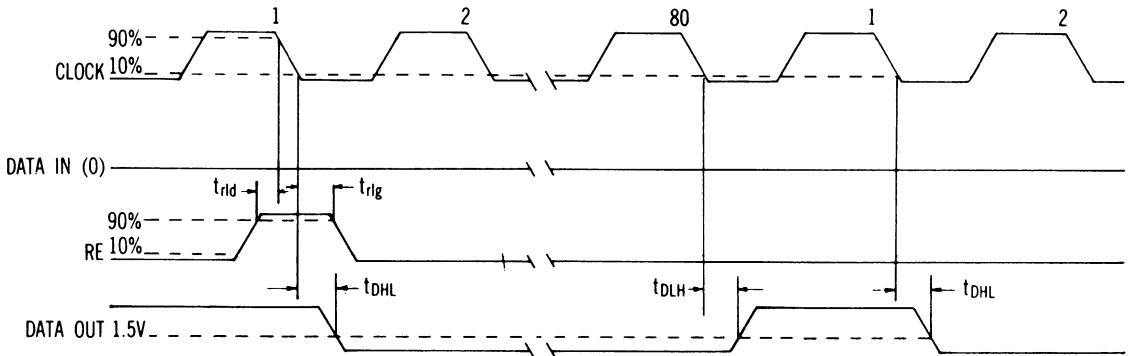
RECIRCULATE: Fig. 2 illustrates recirculating a bit present at the output back through the register. RE must attain a logic 1 for t_{RID} time (Recirculate Control Leadtime) prior to the Clock's negative edge, and must maintain that state at least until the Clock's negative edge (t_{rig}) to insure proper data recirculation. The bit entered will appear 80 clocks later as shown.

CONDITIONS:

1. All timing relationships apply to any of the four registers.   2. Logic 0 is defined as V_{DD} or ground; logic 1 as V_{SS} or +5V.

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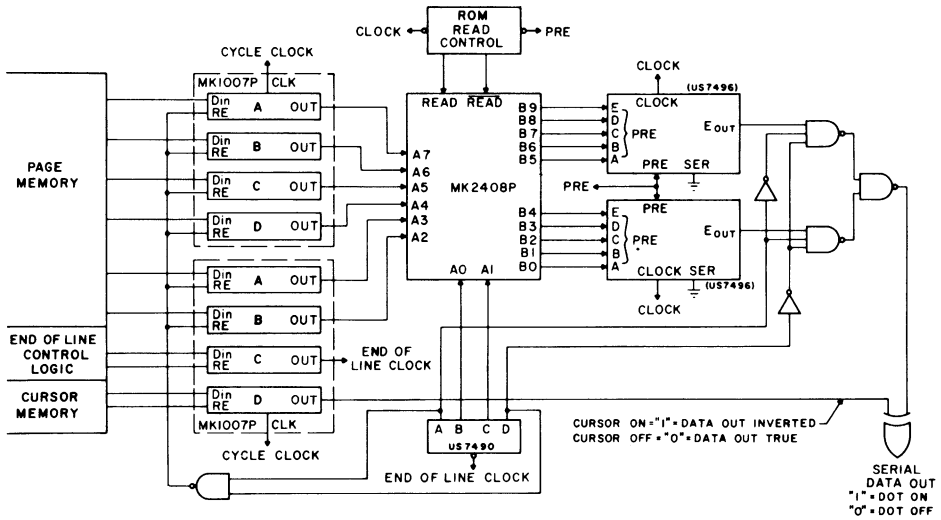
LINE REFRESH MEMORY FOR CRT DISPLAY

This application shows the MK 1007 P used as the Line Refresh Memory, driving MOSTEK's MK 2408 P TTL-compatible character generator. The MK 1007 P receives new data from the Page Memory (which may also consist of MK 1007 P's) on the tenth row of any character line, this being the third vertical space between rows of characters. The MK 1007 P recirculates the character-address data as these characters are scanned and displayed on a CRT screen.

The decade counter selects the appropriate rows from the character generator which outputs two rows of the addressed character at one time (see MK 2408 P data sheet), and also controls the multiplexed output of the character generator so that only one row of the addressed characters is displayed on any CRT horizontal sweep.

One stage of the MK 1007 P may be used to shift a single data bit, which may be used to determine the end of the horizontal sweep. Another stage may be used as a cursor control and, as shown above, may blank the cursored character dots while surrounding dots are on, to give a reverse image of that particular character.

OPERATING NOTES

1. Recirculate Enable (RE) = Logic 1 = output data recirculated.

2. Output data (delayed 80 bits) maintains same logic state when RE = 1.

3. Recirculate Enable (RE) = Logic 0 = Data In (D_{in}) enabled.

4. Output data (delayed 80 bits) attains same logic state as D_{in} when RE = 0.

5. Output data follows the clock negative edge.

TEST CIRCUIT

MEMORY DATA BOOK
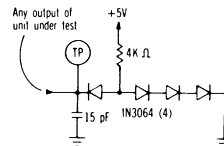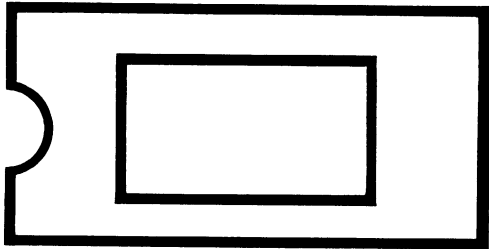
READ-ONLY MEMORY
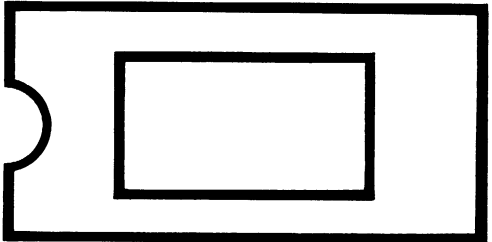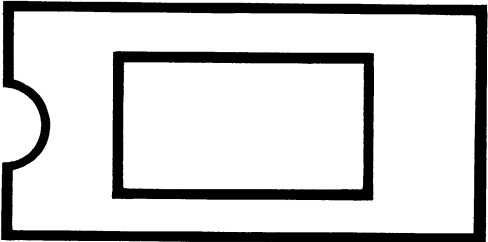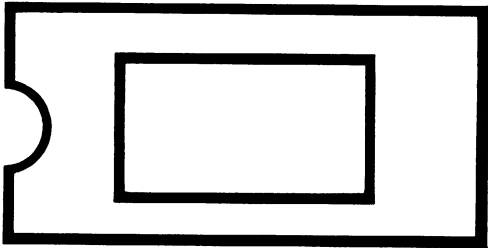
MOSTEK®

2240-BIT ROM CHARACTER GENERATORS
MK2300/2302(P/N)

FEATURES

☐ Ion-implantation processing for full TTL/DTL compatibility

☐ 2240 bits of storage organized as 64 5x7 dot matrix characters with column-by-column output

☐ MK 2302 P is pre-programmed with ASCII encoding

☐ Internal counter provides clocked column selection

☐ Counter output for updating external character address registers

☐ Internal provision for one- or two-column inter-character spacing

☐ Output enable and blanking capability

☐ Operates from +5V and −12V supplies

DESCRIPTION

The MK 2300 P Series MOS, TTL/DTL-compatible read-only memories (ROMs) are designed specifically for dot-matrix character generation. Each ROM provides 2240 bits of programmable storage, organized as 64 characters each having 5 columns of 7 bits. A row output capability of 64 7x10 characters is possible, as illustrated on the back page.

Low threshold-voltage processing, utilizing ion-implantation, is used with P-channel, enhancement-mode MOS technology to provide direct input/output interface with TTL and DTL logic families. All inputs are protected to prevent damage from static charge accumulation.

The MK 2302 P is preprogrammed with ASCII-encoded characters (font shown on back page). Other ROMs in the series are programmed during manufacture to customer specifications by modification of a single mask.

Characters are selected by a six-bit binary word at the Character Address inputs. Each character consists of five columns, the columns selected by an internal counter which is clocked by the Counter Clock input. Column information appears sequentially beginning with the left-most column. Two additional intercharacter spacing columns are available, selectable for one or two spaces by the Count Control Input. During the spacing, the Data Outputs are high (+5V), or the "dot-off" condition. After the last space, the modulo counter automatically increments to the leftmost column.

Synchronizing other system components with the ROM is possible using the Counter Reset Input to reset the counter to the last intercharacter spacing column, or using the Counter Output which occurs only on the last spacing column.

The Blanking Input allows all Data Outputs to be driven high (+5V) without affecting any other ROM functions. The Output Enable input allows the outputs to be open-circuited for wire-ORing.

Memory operation is static; refresh clocks are not required to maintain output information. The Clock input is used only to select columns and need not be pulsed continuously.

FUNCTIONAL DIAGRAM

PIN CONNECTIONS

A1	1	24	VSS
A2	2	23	VGG
A3	3	22	BLANKING INPUT
A4	4	21	OUTPUT ENABLE
A5	5	20	NC
A6	6	19	OUT1
COUNTER CLOCK	7	18	OUT2
COUNTER REST	8	17	OUT3
NC	9	16	OUT4
COUNTER CONTROL	10	15	OUT5
COUNTER OUTPUT	11	14	OUT6
VDD	12	13	OUT7

NC = NO CONNECTION

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ABSOLUTE MAXIMUM RATINGS

Voltage on any terminal relative to V_{SS}................................ +0.3V to −20V
Operating temperature range.. 0°C to +75°C
Storage temperature (Ambient) Ceramic............................ −65°C to +150°C
Storage temperature (Ambient) Plastic............................. −55°C to +125°C

RECOMMENDED OPERATING CONDITIONS (0°C ≤ T_A ≤ 75°C)

	PARAMETER		MIN	TYP	MAX	UNITS	COMMENTS
POWER	V_{SS}	Supply voltage	+4.75	+5.0	+5.25	V	
	V_{DD}	Supply voltage	—	0.0	—	V	See note 1
	V_{GG}	Supply voltage	−12.6	−12.0	−11.4	V	
INPUTS	$V_{in(0)}$	Input voltage, logic "0"			+0.6	V	See note 2
	$V_{in(1)}$	Input voltage, logic "1"	$V_{SS} - 1.5$			V	Count control input should be
	$V_{in(cc)}$	Count Control input voltage, ÷ 6		−12.0	−11.4	V	returned to V_{GG} for ÷ 6 oper-
		÷ 7	+4.75	+5.0		V	ation, or V_{SS} for ÷ 7 operation
COUNTER TIMING	f_{clk}	Counter Clock input frequency	0		200	kHz	
	$t_{clk(0)}$	Clock time at logic "0"	2			μs	
	$t_{clk(1)}$	Clock time at logic "1"	2			μs	See timing
	$t_{r(clk)}$	Clock rise time			0.1	μs	diagrams
	$t_{f(clk)}$	Clock fall time			0.1	μs	
	t_{rp}	Reset pulse width	1.0			μs	
	t_{crd}	Clock-to-reset pulse delay	0.4			μs	See note 4

ELECTRICAL CHARACTERISTICS

($V_{SS} = +5.0V \pm 0.25V$, $V_{GG} = -12.0V \pm 0.6V$, 0°C ≤ T_A ≤ +75°C, unless noted otherwise)

	PARAMETER		MIN	TYP*	MAX	UNITS	CONDITIONS
POW	I_{SS}	Supply current (V_{SS})		20	40	mA	Outputs unconnected
	I_{GG}	Supply current (V_{GG})		20	40	mA	$f_{clk} = 200$ kHz
INPUTS	C_{in}	input capacitance			10	pF	$V_{in} = V_{SS}$, $f_{meas} = 1$MHz See
	I_{in}	Input leakage current			10	μA	$V_{in} = V_{SS} - 6V$, $T_A = 25°C$ note 2
OUTPUTS	$V_{out(0)}$	Output voltage, logical "0"		0.2	0.4	V	$I_{out} = 2.0$ mA (into output) See
	$V_{out(1)}$	Output voltage, logical "1"	2.4			V	$I_{out} = 0.6$ mA note (out of output) 3
	I_{out}	Data Output leakage current	−10		+10	μA	$V_{SS} - 6V \leq V_{out} \leq V_{SS}$ $T_A = 25°C$ (outputs disabled)
DYNAMIC CHARACTERISTICS	t_{AO}	Address-to-output delay time			1	μs	
	t_{CO}	Clock-to-output delay time			1	μs	
	t_{CCO}	Clock-to-counter output delay time			1	μs	Rise and fall See timing
	t_{BO}	Blanking/unblanking delay time			1	μs	times included diagrams
	t_{OEO}	Output enable/disable delay time			1	μs	in delay times
	t_{CRO}	Counter reset delay time			1	μs	$R_L = 4$ kΩ to V_{SS}
	t_{CRCO}	Reset-to-counter output delay time			1	μs	$C_L = 15$ pF to V_{DD}
	t_F	Output fall time			0.3	μs	$T_A = 25°C$
	t_R	Output rise time			0.3	μs	

*Typical values apply at $V_{SS} = +5.0V$, $V_{GG} = -12.0V$, $T_A = 25°C$

NOTES: 1 Supply voltages shown are for operation in a TTL/DTL system. Other supply voltages may be used if V_{DD} and V_{GG} maintain the same relationship to V_{SS}. e.g., $V_{SS} = 0V$, $V_{DD} = -5V$, $V_{GG} - 17V$. Input voltages would also need to be adjusted accordingly

2 These parameters apply to the character address, counter clock, counter reset, blanking, and output enable inputs.

3 These parameters apply to both the data outputs and counter output.

4. The counter clock must not make a negative transition within the period tcrd, before or after a positive counter reset transition. The counter reset negative edge may occur any time.

TIMING

Timing diagram (1)* shows the time relationships between character address, data output, counter clock, and counter output during typical operation of an MK 2300 P Series character generator. An output sequence from the MK 2302 P is shown to help clarify operation. This sequence can be seen from the top rows (OUT₁) of the characters "I" and "N".

(waveforms not to scale)

(1)

```
           "I"              "N"
OUT₁  1 0 0 0 1 1 1   0 1 1 1
      1 1 0 1 1 1 1   0 1 1 1
      1 1 0 1 1 1 1   0 0 1 1
      1 1 0 1 1 1 1   0 1 0 1
      1 1 0 1 1 1 1   0 1 1 0
      1 1 0 1 1 1 1   0 1 1 0
OUT₇  1 0 0 0 1 1 1   0 1 1 1
      └─── COUNT OF 7 ───┘
```
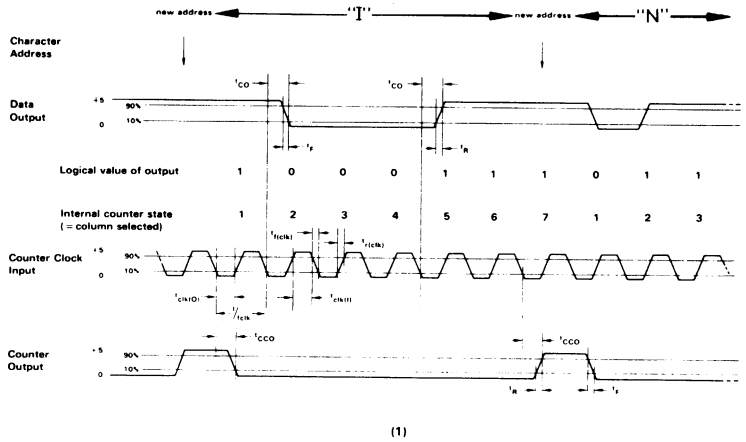
All timing relationships shown in diagram (1) apply to any other output or combination of characters as well.

Relevant input conditions assumed but not shown in timing diagram (1) are as follows:

Count Control,	+5V
Counter Reset,	+5V
Blanking Input,	+5V
Output Enable,	+5V

Had the Count Control input been at −12V, the count sequence would have been six positions instead of seven and the Counter Output would have been high during the sixth position.

New character addresses are shown coinciding with the rising edge of the Counter Output waveform in diagram (1). This condition was selected to demonstrate use of the Counter Output to advance an external input register to a new character address. Character addresses can be changed at any other time as well. Timing diagram (2) depicts output response to a character address change when, for example, the counter is stationary in one of the five character column positions.

Timing diagrams (3) through (6) show timing relationships for the Counter Reset, Blanking Input, and Output Enable. The "open" condition in (6) implies that both the pull-up and pull-down devices in each data output push-pull buffer are turned off

(2)

(3)

(4)

(5)

(6)
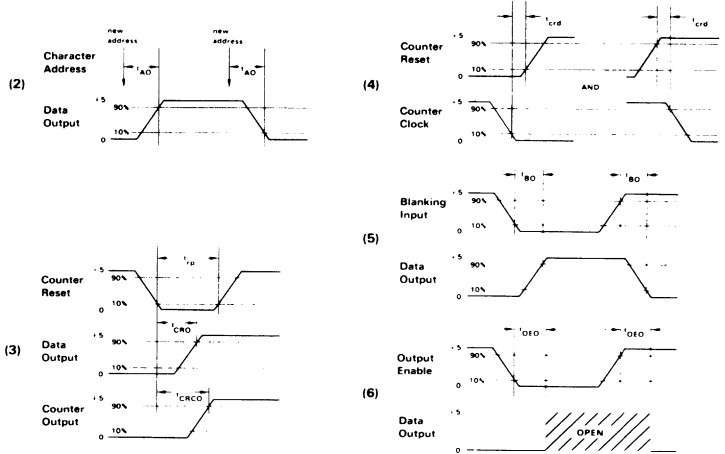
OPERATING NOTES

The following table summarizes the MK 2300 P Series input control states and corresponding drive levels:

Count Control	
÷6	−12V
÷7	+5V
Counter Reset	
operate	+5V
reset	0V
Blanking Input	
unblank	+5V
blank*	0V
Output Enable	
enable	+5V
disable**	0V

*All data outputs high (+5V)
**All data outputs open-circuited

2240-BIT ROM CHAR GEN

15

MK 2302 P

Logic 1 = input @ +5V
Logic 0 = input @ 0V

Output dot "on" = 0V
Output dot "off" = +5V

OUT$_1$ →
OUT$_2$ →
OUT$_3$ →
OUT$_4$ →
OUT$_5$ →
OUT$_6$ →
OUT$_7$ →

ROM CODING

7x10 Non-Interlace Configuration: (As illustrated) For row-out (7-bit) horizontal raster-scan application, code ROM #1 for Rows 1 through 5; and ROM #2 for Rows 6 through 10.

7x10 Interlace (525-line): Code ROM #1 for Rows 1, 3, 5, 7, 9; Code ROM #2 for Rows 2, 4, 6, 8, 10. The Enable Flip-flop should be changed to clock only at vertical retrace time, thus allowing ROM #1 to be enabled for the 1st page sweep (262 ½ lines) and then allowing ROM #2 to be enabled for the interlaced 2nd page sweep of 262 ½ lines.

ADDRESS INPUT

SN 7473
ENABLE   ENABLE
(HORIZONTAL RETRACE)
END OF LINE CLOCK
6 BITS
ROM #1 (MK 2300 P)
A1 A6 CLK
ENABLE   OUTPUT ENABLE   RST ← RESET
CLR
K CP J
RESET
POWER ON AND/OR VERTICAL RETRACE
+5V
CTR OUT
07 ← → 01
END OF LINE CLOCK
A1 A6 CLK
ENABLE ← OUTPUT ENABLE
RST ← RESET
ROM #2 (MK 2300 P)
07 ← → 01
SN74165 SN74166
PARALLEL LOAD 8 BIT SHIFT REGISTER
A B C D E F G H
CLK ← CLOCK
SER
STROBE ← LOAD
H OUT
TO VERTICAL AMPLIFIER

Combining two 5x7 column-output ROMs provides a 7x10 row output.

7 BIT COL
5 BIT ROW
5 BIT ROW
10 Bit Col.
7 Bit Row

A$_4$	A$_3$	A$_2$	A$_1$	A$_6$ 1 / A$_5$ 0	1 / 1	0 / 0	0 / 1
0	0	0	0				
0	0	0	1				
0	0	1	0				
0	0	1	1				
0	1	0	0				
0	1	0	1				
0	1	1	0				
0	1	1	1				
1	0	0	0				
1	0	0	1				
1	0	1	0				
1	0	1	1				
1	1	0	0				
1	1	0	1				
1	1	1	0				
1	1	1	1				

MOSTEK ROM PUNCHED-CARD CODING FORMAT[1]

MK 2300 P

Cols.   Information Field

First Card

1-30	Customer
31-50	Customer Part Number
60-72	Mostek Part Number[2]

Second Card

1-30	Engineer at Customer Site
31-50	Direct Phone Number for Engineer

Third Card

1-5	Mostek Part Number[1]
10-15	Organization[2]

Fourth Card

1-6	Data Format[3] — "MOSTEK"
15-28	Logic[4] — "Positive Logic" or
35-57	Verification Code[5]

Data Cards 4

1-6	Binary Address
8-12	First row of character
14-18	Second row of character
20-24	Third row of character
26-30	Fourth row of character
32-36	Fifth row of character
38-42	Sixth row of character
44-48	Seventh row of character

Notes: 1. Assigned by Mostek Marketing Department; may be left blank.

2. Punched as 64x5x7.

3. "MOSTEK" format only is accepted on this part.

4. A dot "ON" should be coded as a "1".

5. Punched as: (a) VERIFICATION HOLD — i.e. the customer verification of the data as reproduced by MOSTEK is required prior to production of the ROM. To accomplish this MOSTEK supplies a copy of its Customer Verification Data Sheet (CVDS) to the customer.

(b) VERIFICATION PROCESS — i.e. the customer will receive a CVDS but production will begin prior to receipt of customer verification.

(c) VERIFICATION NOT NEEDED — i.e. the customer will not receive a CVDS and production will begin immediately.

2240-BIT ROM CHAR GEN

MOSTEK.®

FEATURES

☐ Ion-implanted for full TTL/DTL compatibility

☐ Chip enable permits wire-ORing

☐ Custom-programmed memory requires single mask modification

☐ 550 ns cycle time (0° ≤ T_A ≤ 75°C)

☐ Static output storage latches

☐ Optional 3-bit, chip-select decoder available

☐ 2560 bits of storage, organized as 256 10-bit words

☐ Operates from +5V and −12V supplies

DESCRIPTION

The MK 2400 P Series TTL/DTL-compatible MOS Read-Only Memories (ROM's) are designed for a wide range of general-purpose memory applications where large quantity bit storage is required. Each ROM provides 2560 bits of programmable storage, organized as 256 words of 10 bits each. Low threshold-voltage processing, utilizing ion implantation with P-channel enhancement-mode MOS technology, provides direct input/output interface with TTL and DTL logic.

Programming is accomplished during manufacture by modification of a single mask, according to customer specifications. The MK 2400 P Series is available in either 24-lead or 28-lead ceramic dual-in-line packages. On the 28-pin ROM, an optional Chip Select Decoder may also be programmed according to customer specifications to provide a 3-bit Chip Select Code.

Operation involves transferring addressed information from the memory matrix into the storage latches using the READ and READ inputs (see Timing). Information stored in the latches will remain despite address changes or chip disabling until the READ and READ inputs are again cycled. READ and READ input signals may be generated from separate timing circuits if desired, or either may be the inverse of the other.

The Chip Enable input forces the normally push-pull output buffer stages to an open-circuit condition when disabling the chip. If desired, new data can be stored in the storage latches while the chip is disabled. When the chip is reenabled, this data would be present at the outputs.

All inputs are protected against static charge accumulation. Pull-up resistors on all inputs are available as a programmable option.

FUNCTIONAL DIAGRAM
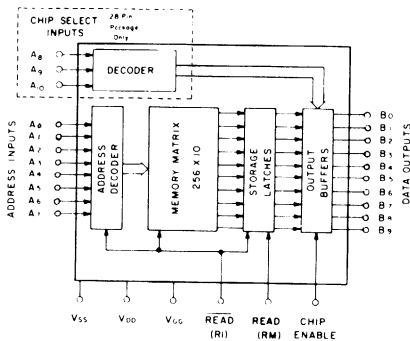
OPERATING NOTES

CHIP ENABLE	READ	READ	OUTPUT
0	X	X	A
1	0	1	B
1	1	0	C

"1" = V_{SS} (+5V); "0" = V_{DD} (0V)

X = No effect on output

A = Output open-circuited

B = Output retains data last stored in latches

C = Output assumes state of addressed cells

ABSOLUTE MAXIMUM RATINGS

Voltage on any terminal relative to V_{SS} . . . . +0.3V to −10V

Operating temperature range . . . . 0°C to +75°C

Storage temperature range . . . . −65°C to +150°C

RECOMMENDED OPERATING CONDITIONS (0°C ≤ T_A ≤ 75°C)

		PARAMETER	MIN	TYP	MAX	UNITS	COMMENTS
POWER	V_{SS}	Supply voltage	+4.75	+5.0	+5.25	V	
	V_{DD}	Supply voltage	—	0.0	—	V	See note 1
	V_{GG}	Supply voltage	−12.6	−12.0	−11.4	V	
INPUTS	$V_{in(0)}$	Input voltage, logic "0"		0	+0.8	V	Pull-up resistors (≈5K~) to
	$V_{in(1)}$	Input voltage, logic "1"	V_{SS}−1.5	V_{SS}		V	V_{SS} available as programmable option.
INPUT TIMING	t_{cyc}	Address change cycle time	550			ns	
	t_d	Address to $\overline{Read}$ lead time	250			ns	
	t_{lg1}	Read lag time 1	−.05		.05	μs	See
	t_{lg2}	Read lag time 2	−.05		.05	μs	Timing
	$t_{\overline{rd}}$	$\overline{Read}$ pulse width	300			ns	Section
	t_{rd}	Read pulse width	0.3		100	μs	
	t_r	Rise time, any input			100	ns	
	t_f	Fall time, any input			100	ns	

ELECTRICAL CHARACTERISTICS (V_{SS} = +5.0V ±0.25V, V_{GG} = −12.0V ±0.6V, 0°C ≤ T_A ≤ +75°C, unless noted otherwise. Pull-up resistors not programmed.)

		PARAMETER	MIN	TYP*	MAX	UNITS	CONDITIONS
POWER	I_{SS}	Supply current (V_{SS})		12	25	mA	Outputs unconnected
	I_{GG}	Supply current (V_{GG})		−12	−25	mA	See Note 2 and Note 3
INPUTS	C_{in}	Input capacitance		5	10	pF	$V_{in}=V_{SS}$, f_{meas} = 1MHz
	I_{in}	Input leakage current			10	μA	$V_{in}=V_{SS}$ −6V T_A=25°C
OUTPUTS	$V_{out(0)}$	Output voltage, logical "0"			0.4	V	I_{out} = 1.6 mA (into output) See note
	$V_{out(1)}$	Output voltage, logical "1"	2.4			V	I_{out} = 0.4 mA 3
							(out of output) and
							V_{SS} −6V ≤ V_{out} ≤ V_{SS} Figure #1
	I_{out}	Output leakage current	−10		+10	μA	T_A=25°C (outputs disabled)
DYNAMIC CHARACTERISTICS	t_{ACC}	Address-to-output access time			600	ns	t_{rd} = 250ns
	t_{OD}	Output delay time			350	ns	t_{lg1} = 0
	t_{OEO}	Output enable/disable time		125	300	ns	t_{lg2} = 0 See timing
	t_{CS}	Chip Select to Output Delay			600	ns	See note 4 Section and Figure #1
	t_{CD}	Chip Deselect to Output Delay			600	ns	

*Typical values apply at V_{SS} = +5.0V, V_{GG} = −12.0V, T_A=25°C

NOTES: 1. Supply voltages shown are for operation in a TTL/DTL system. Other supply voltages may be used if V   and V_{GG} maintain the same relationship to V_{SS}, e.g., V_{SS}=0V, V_{DD} = −5V, V_{GG}=−17V. Input voltages would also need to be adjusted accordingly.

2. Max measurements at 0°C. (MOS supply currents increase as temperature decreases.) I_{SS} will increase 1.6mA (max) for each input at logic 0 when pull-up resistors are programmed.

3. Unit operated at minimum specified cycle time.

4. The outputs become open circuited when disabled or deselected. As shown in Fig. 1, an output with a "1" expected out does not transition through the 1.5V point when enabled (selected) or disabled (deselected); this is true because the TTL equivalent load pulls the open-circuited output to approximately 2 volts.

TIMING

Notes:

1. All times are referenced to the 1.5V point relative to V_{DD} (ground) except rise and fall time measurements
2. Chip enable = V_{SS} for all measurements except when measuring T_{OEO}
3. Logic 0 is defined as V_{DD} or ground, logic 1 as V_{SS} or +5V

INTERNAL FUNCTION OF READ/READ SIGNALS
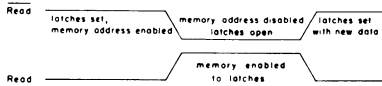
Set up time, t_{LS}, allows the input address to propagate through the address decoder and memory matrix prior to READ logic 0 time. As indicated above, READ at a logic 0 internally disables the input address so that an external address change may occur without affecting the location previously selected. The latches are also readied to receive new data which is enabled from the matrix when READ is at a logic 1. Data is set in the latches when READ is allowed to rise back to its logic 1 state. In actual use, the READ rising and falling edges can precede the falling and rising edges of READ, respectively, as implied by the specification of negative read lag times. This allows a very flexible timing relation between the two pulses, in that either input can be the inversion of the other or both may be generated from separate timing circuits.

Output data appears following the rise of the READ pulse but correct output data will not appear until READ has gone low. For this reason, READ is shown preceding READ even though other relationships are allowed. If READ is made to precede READ, delay time, t_{OD}, should be referenced to the fall of READ rather than as shown.

The chip is disabled by applying a logical 0 to the chip enable input, forcing the outputs to an open-circuit condition. The output data present at the time of disable will again be present upon re-enabling unless a new read cycle was initiated for a different address while the chip was disabled, in which case the new data would be present at the outputs.

The programmable 3-bit chip select timing would be the same as the address inputs.
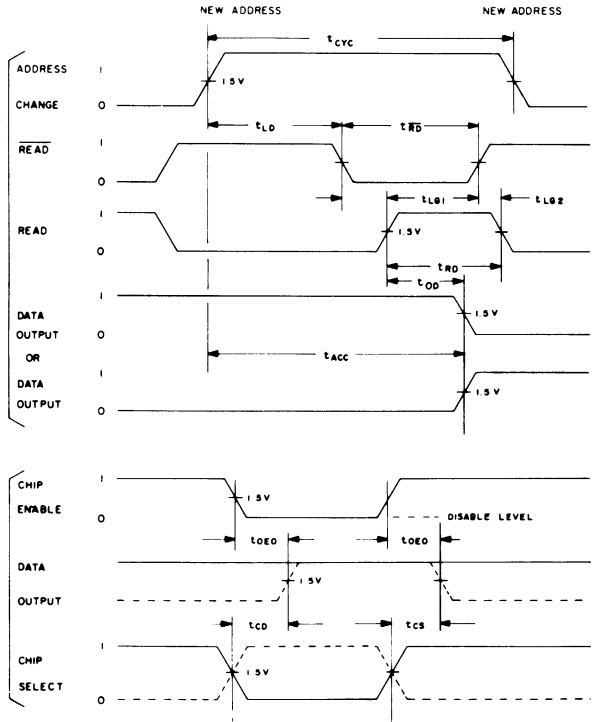
NOTE: Wave forms are not to scale.

FIGURE #1 t_{ACC} and t_{OD} test circuit

APPLICATIONS

Application shows wire-Or'ing for expansion to a 512 X 10 memory. Further expansion is possible by 1 of N decoding to the Chip Enable input (or with the optional 3-bit decoder) while maintaining the time relationships shown. t... should include the desired data-valid time. Interface devices may be TTL or DTL.

PIN CONNECTIONS

top view, 24 pin CDIP

Vss	1		24	B9
VGG	2		23	B8
A1	3		22	B7
A0	4		21	B6
A2	5		20	B5
A7	6		19	B4
A6	7		18	B3
A5	8		17	B2
A4	9		16	B1
RM/READ	10		15	B0
A3	11		14	VDD
RI/READ	12		13	C.E.

PIN CONNECTIONS

top view, 28 pin CDIP

Vss	1		28	B9
VGG	2		27	B8
(NC)A1	3		26	B7
(NC)A0	4		25	B6
(A1)A2	5		24	B5
(A0)A7	6		23	NC
(A2)A6	7		22	B4
(A7)A5	8		21	B3
(A6)A4	9		20	B2
(A5)RM/READ	10		19	B1
(A4)A3	11		18	B0
(NC)RI/READ	12		17	VDD
(READ)A8	13		16	CE
(A3)A9	14		15	A10(READ)

N.C. = no connection

( ) OPTIONAL PIN ARRANGEMENT

MOSTEK ROM PUNCHED-CARD CODING FORMAT[1]

MK 2400 P

Cols.   Information Field

First Card

1-30	Customer
31-50	Customer Part Number
60-72	Mostek Part Number[2]

Second Card

1-30	Engineer at Customer Site
31-50	Direct Phone Number for Engineer

Third Card

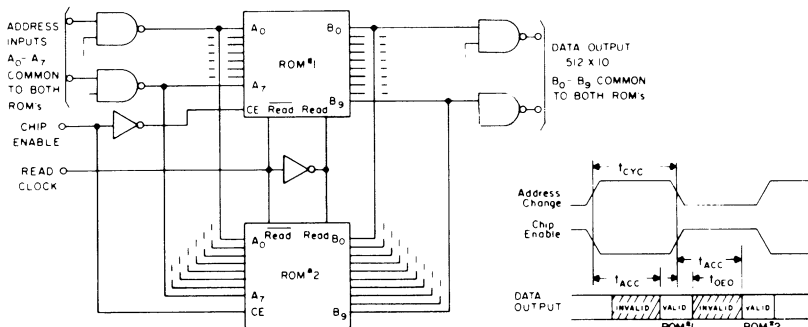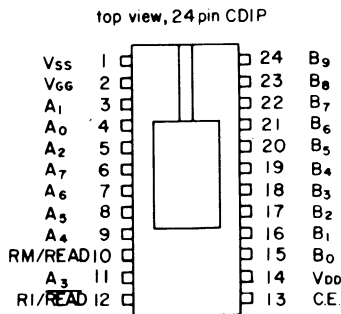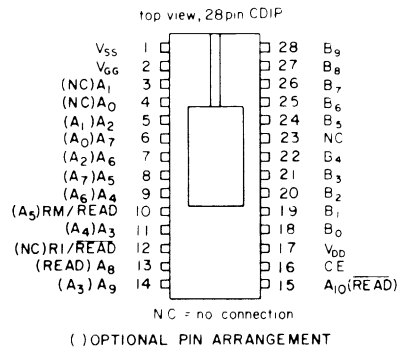|	
1-5	Mostek Part Number[2]
10-16	Organization[3]
29	A8[4]
30	A9[4]
31	A10[4]
32	Pull-up Resistor[5]

Fourth Card

0-6	Data Format[6] — "MOSTEK"
15-28	Logic — "Positive Logic" or

	"Negative Logic"
35-57	Verification Code[7]
60-74	Package Choice[8]

Data Cards

1-3	Decimal Address
5	Output B9
6	Output B8
7	Output B7
8	Output B6
9	Output B5
10	Output B4
11	Output B3
12	Output B2
13	Output B1
14	Output B0
16	Octal Equivalent of: B9[9]
17	Octal Equivalent of: B8, B7, B6[9]
18	Octal Equivalent of: B5, B4, B3[9]
19	Octal Equivalent of: B2, B1, B0[9]

Notes: 1. Positive or negative logic formats are accepted as noted in the fourth card.

2. Assigned by Mostek Marketing Department; may be left blank.

3. Punched as 0256x10.

4. A "0" indicates the chip is enabled by a logic 0, a "1" indicates it is enabled by a logic 1, and a "2" indicates a "Don't Care" condition.

5. A "1" indicates pull-ups; a "0" indicates no pull-ups.

6. "MOSTEK" format only is accepted on this part.

7. Punched as: (a) VERIFICATION HOLD — i.e. customer verification of the data as reproduced by MOSTEK is required prior to production of the ROM. To accomplish this MOSTEK supplies a copy of its Customer Verification Data Sheet (CVDS) to the customer.

(b) VERIFICATION PROCESS — i.e. the customer will receive a CVDS but production will begin prior to receipt of customer verification.

(c) VERIFICATION NOT NEEDED — i.e. the customer will not receive a CVDS and production will begin immediately.

8. "24 PIN", "28 PIN STANDARD", or "28 PIN OPTIONAL" (left justified to column 60).

9. The octal parity check is created by breaking up the output word into groups of three from right to left and creating a base 8 (octal) number in place of these groups. For example the output word 1010011110 would be separated into groups 1/010/011/110 and the resulting octal equivalent number is 1236.

MK 2400 P

Cols.   Information Field

First Card

1-30   Customer
31-50   Customer Part Number
60-72   Mostek Part Number[2]

Second Card

1-30   Engineer at Customer Site
31-50   Direct Phone Number for Engineer

Third Card

1-5   Mostek Part Number[2]
10-16   Organization[3]
29   A8[4]
30   A9[4]
31   A10[4]
32   Pull-up Resistor[5]

Fourth Card

0-6   Data Format[4] — "MOSTEK"
15-28   Logic — "Positive Logic" or

"Negative Logic"
35-57   Verification Code[7]
60-74   Package Choice[8]

Data Cards

1-3   Decimal Address
5   Output B9
6   Output B8
7   Output B7
8   Output B6
9   Output B5
10   Output B4
11   Output B3
12   Output B2
13   Output B1
14   Output B0
16   Octal Equivalent of: B9[9]
17   Octal Equivalent of: B8, B7, B6[9]
18   Octal Equivalent of: B5, B4, B3[9]
19   Octal Equivalent of: B2, B1, B0[9]

Notes: 1. Positive or negative logic formats are accepted as noted in the fourth card.

2. Assigned by Mostek Marketing Department; may be left blank.

3. Punched as 0256x10.

4. A "0" indicates the chip is enabled by a logic 0, a "1" indicates it is enabled by a logic 1, and a "2" indicates a "Don't Care" condition.

5. A "1" indicates pull-ups; a "0" indicates no pull-ups.

6. "MOSTEK" format only is accepted on this part.

7. Punched as: (a) VERIFICATION HOLD — i.e. customer verification of the data as reproduced by MOSTEK is required prior to production of the ROM. To accomplish this MOSTEK supplies a copy of its Customer Verification Data Sheet (CVDS) to the customer.

   (b) VERIFICATION PROCESS — i.e. the customer will receive a CVDS but production will begin prior to receipt of customer verification.

   (c) VERIFICATION NOT NEEDED — i.e. the customer will not receive a CVDS and production will begin immediately.

8. "24 PIN", "28 PIN STANDARD", or "28 PIN OPTIONAL" (left justified to column 60).

9. The octal parity check is created by breaking up the output word into groups of three from right to left and creating a base 8 (octal) number in place of these groups. For example the output word 1010011110 would be separated into groups 1/010/011/110 and the resulting octal equivalent number is 1236.

2560-BIT STATIC ROM
MK2400(P)

MOSTEK®

256 x 10-BIT ROM CHARACTER GENERATOR
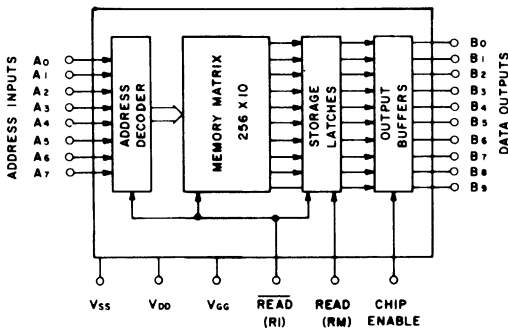
MK2408(P)

DESCRIPTION

The MK 2408 P is a pre-programmed member of the MK 2400 P Series. It is programmed as a dot-matrix character generator (64 characters) with ASCII encoded inputs and row (5-bit) outputs. The MK 2408 P outputs two rows at the same time. Row 1 is available at outputs B9 (left), B8, B7, B6, and B5 (right) while row 2 is available at outputs B4 (left), B3, B2, B1, and B0 (right). Row 3 is available at B9 through B5 while row 4 is available at B4 through B0. Row 5 and row 6 are available at B9 through B5 and B4 through B0. Row 5 and row 6 are available at B9 through B5 and B4 through B0. Row selection is determined by the address combination of bits A0 and A1.

The MK 2408 P meets and operates by the specifications outlined in the MK 2400 P Series data sheet (DS-24001270-2)

The example in Figure 1 demonstrates the correspondence of the device outputs and row select sequence to the 7 x 5 dot-matrix font. The complete character font patterns (truth table) are illustrated on the back. A logic 1 or a DOT represents an input or output voltage equal to Vss (+5V) and a logic 0 or a blank represents a voltage equal to VDD (OV). The eighth row outputs (B4 through B0 when inputs A1 and A0 equal logic 1) are not illustrated since in each case they are equal to all 0's.
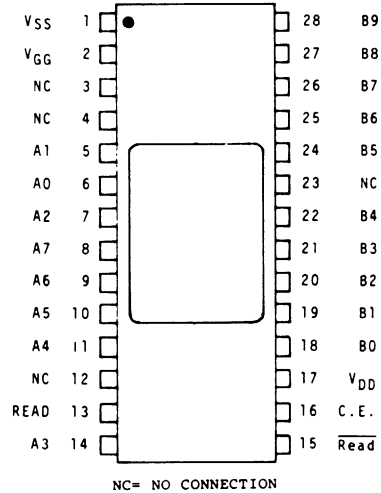
FUNCTIONAL DIAGRAM

PIN CONNECTIONS

NC= NO CONNECTION

FIGURE 1

A1	A0		B9 B4	B8 B3	B7 B2	B6 B1	B5 B0			
0	0		1	0	0	0	1	--	B9-B5	A7 = 0
			1	1	0	1	1	--	B4-B0	A6 = 0
0	1		1	0	1	0	1	--	B9-B5	A5 = 1
			1	0	1	0	1	--	B4-B0	
1	0		1	0	0	0	1	--	B9-B5	A4 = 1
			1	0	0	0	1	--	B4-B0	A3 = 0
1	1		1	0	0	0	1	--	B9-B5	A2 = 1
			0	0	0	0	0	--	B4-B0	

25

CODING & CHARACTER FONTS

APPLICATION

Valid 2 presets address #1 data in shift registers. Valid 3 presets address #2, etc.

MOSTEK®

FEATURES

- High-speed, static operation—400nsec. typical access time
- Active input pull-ups provide worst-case TTL compatibility
- Push-pull outputs provide three output states: one, zero, and open

- Ion-implantation for constant current loads and lower power
- Standard power supplies: +5V, −12V
- MK2500P is pin-for-pin replacement for National 5232
- MK2600P is pin-for-pin replacement for Fairchild 3514

DESCRIPTION

The MK2500(P) and MK2600(P) series of TTL/DTL compatible MOS read-only memories (ROMs) are designed to store 4096 bits of information by programming one mask pattern. The word and bit organization of these ROM series is either 512W x 8B or 1024W x 4B.

The MK2500/2600(P) series has push-pull outputs that can be in one of three states: logic one, logic zero, or open or unselected state. This, plus the programmable Chip Selects, enables the use of sev-

eral ROMs in parallel with no external components. Since the ROM is a static device, no clocks are required, making the MK2500/2600(P) series of ROMs very versatile and easy to use.

Low threshold-voltage processing, utilizing ion-implantation, is used with P-channel, enhancement-mode MOS technology to provide direct input/output interfacing with TTL and DTL logic families. All inputs are protected to prevent damage from static charge accumulation.

PIN CONNECTIONS

MK 2500 P

MODE CONTROL	1	24	V_{LL}
CHIP SELECT 1	2	23	V_{CC}
CHIP SELECT 2	3	22	B8
CHIP SELECT 3/A10	4	21	B7
A1	5	20	B6
A2	6	19	B5
A3	7	18	B4
A4	8	17	B3
A5	9	16	B2
A6	10	15	B1
A7	11	14	A9
V_{SS}	12	13	A8

MK 2600 P

V_{CC}	1	24	V_{SS}
CHIP SELECT 2	2	23	CHIP SELECT 1
CHIP SELECT 3	3	22	CHIP SELECT 0/A10
B1	4	21	A1
B2	5	20	A2
B3	6	19	A3
B4	7	18	A4
B5	8	17	A5
B6	9	16	A6
B7	10	15	A7
B8	11	14	A8
V_{DD}	12	13	A9
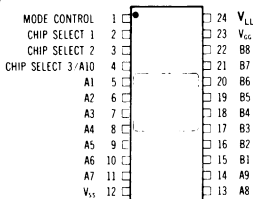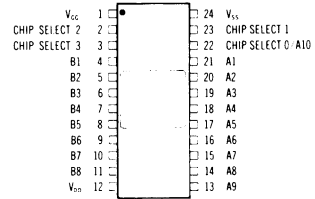
FUNCTIONAL DIAGRAMS

MK 2500 P

MK 2600 P

ABSOLUTE MAXIMUM RATINGS

Voltage on Any Terminal Relative to V_{SS} (except V_{GG}) .... +0.3V to –10V
Voltage on V_{GG} Terminal Relative to V_{SS} .... +0.3V to –20V
Operating Temperature Range (Ambient) .... 0°C to +70°C
Storage Temperature Range (Ambient) .... –65°C to +150°C

RECOMMENDED OPERATING CONDITIONS

($0°C \leq T_A \leq 70°C$)

	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{SS}	Supply Voltage	+4.75	+5.0	+5.25	V	
V_{DD}	Supply Voltage	——	0.0	——	V	Note 1
V_{GG}	Supply Voltage	–11.4	–12.0	–12.6	V	
V_{IL}	Input Voltage, Logic "0"			+0.8	V	
V_{IH}	Input Voltage, Logic "1"	$V_{SS}-1.5$			V	Note 2
V_{IH}	Input Voltage, Logic "1"	2.4			V	Note 3

ELECTRICAL CHARACTERISTICS

($V_{SS} = +5.0V \pm 5\%$; $V_{DD} = 0$ V; $V_{GG} = -12V \pm 5\%$; $0°C \leq T_A \leq 70°C$ unless noted otherwise)

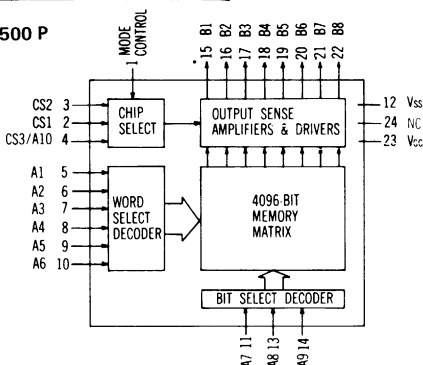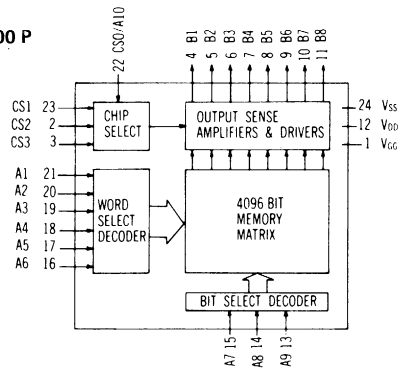|	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
I_{SS}	Supply Current, V_{SS}		19.0	28.0	mA	Note 4
I_{GG}	Supply Current, V_{GG}		19.0	28.0	mA	Note 4
$I_{I(L)}$	Input Leakage Current, Any Input			10.0	μA	$V_I = V_{SS}-6.0V$. Note 2
I_{IL}	Input Current, Logic 0, Any Input			–100.0	μA	$V_I = .4V$. Note 3
I_{IH}	Input Current, Logic 1, Any Input			–600.0	μA	$V_I = 2.4V$. Note 3
V_{OL}	Output Voltage, Logic "0"			0.4	V	$I_{OL} = 1.6mA$
V_{OH}	Output Voltage, Logic "1"	2.4			V	$I_{OH} = -40\mu A$
$I_{O(L)}$	Output Leakage Current			+10	μA	Outputs disabled ($V_O = V_{SS}-6V$)
C_{IN}	Input Capacitance			10	pF	Note 5
C_O	Output Capacitance			10	pF	Note 5
t_{ACCESS}	Address to Output Access Time	100	400	700	nsec	Refer to
t_{CS}	Chip Select to Output Delay	100	250	500	nsec	Test
t_{CD}	Chip Deselect to Output Delay	100	250	800	nsec	Note 6 Circuit

Notes:
1. This is V_{LL} on MK 2500 P.
2. This parameter is for inputs without active pull-ups (programmable).
3. This parameter is for inputs with active pull-ups (programmable) for TTL interfaces. As the TTL driver goes to a logic 1 it must only provide 2.4V (this voltage must not be clamped) and the circuit pulls the input to V_{SS}. Refer to the Input pull-up figure for a graphical description of the active pull-up's operation.
4. Inputs at V_{SS}, outputs unloaded.
5. $V_{Bias} - V_{SS} = OV$; f = 1 MHz.
6. t_{CD} is primarily dependent on the RC time constant of the load (i.e. the outputs become open circuited upon being disabled). As noted in the Timing Diagram, disabling or enabling an output with a "1" expected out does not yield a transition through the 1.5V point; this is true because the TTL equivalent load pulls the open-circuited output to approximately 2 volts.

PROGRAMMING OPTIONS

MK 2500 P

OPTIONS

Function	512 X 8	1024 X 4
Mode Control	1	0
Chip Select 1	1 or 0	1 or 0
Chip Select 2	1 or 0	1 or 0
Chip Select 3/A10	1 or 0	address A10

1 = Most Positive = High Level Voltage

Pin 1 in the MK 2500 P is used as a Mode Control, setting the circuit in the 1024x4 or 512x8 mode. In the 1024x4 mode a tenth address bit is required, which is provided at Pin 4. If the circuit is in the 512x8 mode, then Pin 4 may be used for a third chip select.

Additional Options: The MK 2500 P can have the address and control inputs set by the user so that:

    512x8:   Mode Control — High
             A10 — Low

    1024x4: Mode Control — Low
             A10 aid as an address
             See Note 9, following page

MK 2600 P

OPTIONS

Function	512 X 8	1024 X 4
Chip Select 0/A10	1 or 0	A10
Chip Select 1	1 or 0	1 or 0
Chip Select 2	1 or 0	1 or 0
Chip Select 3	1 or 0	1 or 0

1 = Most Positive = High Level Voltage

The MK 2600 P is programmed either as a 512x8 array or a 1024x4 array. In the 1024x4 arrays, Pin 22 provides the tenth address bit. When A10 is low the four bits are present at the even outputs (B2, B4, B6, and B8); when A10 is high, the bits are at the odd outputs (B1, B3, B5, and B7).

In 512x8 arrays, Pin 22 may be used to provide a fourth chip select. Thus, with four programmable chip selects, sixteen MK 2600 P ROMS in the 512x8 configuration can be arranged in an 8192x8 array requiring no external decoding.

4096-BIT STATIC ROM MK2500/2600(P)

TIMING
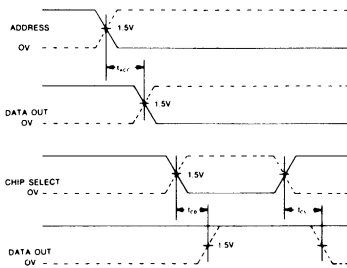
T_{ACCESS} TEST CIRCUIT
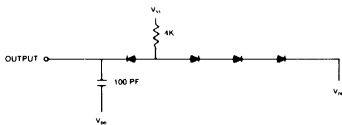
DIODES ARE IN447

INPUT
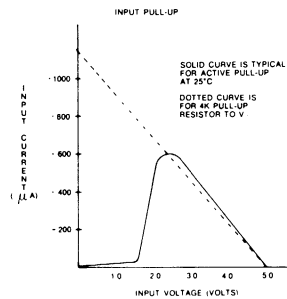
MOSTEK ROM PUNCHED-CARD CODING FORMAT[1]

MK 2500 P
First Card

Cols.	Information Field
1-30	Customer
31-50	Customer Part Number
60-72	Mostek Part Number[2]

Second Card

1-30	Engineer at Customer Site
31-50	Direct Phone Number for Engineer

Third Card

1-5	Mostek Part Number[2]
10-16	Organization[3]
29	CS3[10]
30	CS2[4]
31	CS1[4]
32	Active Pull-ups[5]

Fourth Card

1-9	Data Format[6]
15-28	Logic — "Positive Logic" or "Negative Logic"
35-57	Verification Code[7]
60-67	"A10 EVEN" or "A10 ODD" (left justified)[9]

Data Cards/512x08 Organization

1-4	Decimal Address
6-13	Output B8- B1 (MSB thru LSB)
15-17	Octal Equivalent of output data[8]

Data Cards/1024x04 Organization

1-4	Decimal Address (0-1022), even addresses
6-9	Output (MSB-LSB)
11-12	Octal Equivalent of output data[8]
50-53	Decimal Address (1-1023), odd addresses
55-58	Output (MSB-LSB)
60-61	Octal Equivalent of output data[8]

MK 2600 P
First Card

Cols.	Information Field
1-30	Customer
31-50	Customer Part Number
60-72	Mostek Part Number[2]

Second Card

1-30	Engineer at Customer Site
31-50	Direct Phone Number for Engineer

Third Card

1-5	Mostek Part Number[2]
10-16	Organization[3]
29	CS3[4]
30	CS2[4]
31	CS1[4]
32	CS0[10]
33	Active Pull-ups[5]

Fourth Card

1-9	Data Format[6]
15-28	Logic — "Positive Logic" or "Negative Logic"
35-57	Verification Code[7]

Data Cards/512x08 Organization

1-4	Decimal Address
6-13	Output B8- B1 (MSB thru LSB)
15-17	Octal Equivalent of output data[8]

Data Cards/1024x04 Organization

1-4	Decimal Address (0-1022), even addresses
6-9	Output (MSB-LSB)
11-12	Octal Equivalent of output data[8]
50-53	Decimal Address (1-1023), odd addresses
55-58	Output (MSB-LSB)
60-61	Octal Equivalent of output data[8]

Notes:

1. Positive or negative logic formats are accepted as noted in the fourth card.

2. Assigned by Mostek Marketing Department; may be left blank.

3. Punched as "0512x08" or "1024x04".

4. A "0" indicates the chip is enabled by a logic 0, a "1" indicates it is enabled by a logic 1, and a "2" indicates a "Don't Care" condition.

5. A "1" indicates active pull-ups; a "0" indicates no pull-ups.

6. MOSTEK, Fairchild, or National Punched-Card Coding Format may be used. Specify which punched card format used by punching either "MOSTEK", "Fairchild", or "National". Start name at column one.

7. Punched as: (a) VERIFICATION HOLD — i.e. customer verification of the data as reproduced by MOSTEK is required prior to production of the ROM. To accomplish this MOSTEK supplies a copy of its Customer Verification Data Sheet (CVDS) to the customer.
    (b) VERIFICATION PROCESS — i.e. the customer will receive a CVDS but production will begin prior to receipt of customer verification.
    (c) VERIFICATION NOT NEEDED — i.e. the customer will not receive a CVDS and production will begin immediately.

8. The octal parity check is created by breaking up the output word into groups of three from right to left and creating a base 8 (octal) number in place of these groups. For example the output word 10011110 would be separated into groups 10/011/110 and the resulting octal equivalent number is 236.

9. "A10 EVEN" and "A10 ODD" applies to the 1024 x 4 mode. "A10 EVEN" means the even outputs are enabled when A10 is high. "A10 ODD" means the odd outputs are enabled when A10 is high.

10. Punched as "2" for 1024 x 4 organization.

ASCII-TO-EBCDIC CODE CONVERTER
EBCDIC-TO-ASCII CODE CONVERTER

A₁ = LSB   B₁ = LSB
A₉ = MSB   B₈ = MSB

| MK 2503 P Function	512 X 8
Mode Control	1
Chip Select 1	0
Chip Select 2	0
Chip Select 3/A10	0

MK 2601 P Function	512 X 8
Chip Select 0/A10	0
Chip Select 1	0
Chip Select 2	0
Chip Select 3	0

ASCII (ADDRESS) TO EBCDIC (DATA)

Addr	Data	Addr	Data	Addr	Data	Addr	Data
0	00000000	1	00000001	2	00000010	3	00000011
4	00110111	5	00101101	6	00101110	7	00101111
8	00010110	9	00000101	10	00100101	11	00001011
12	00001100	13	00001101	14	00001110	15	00001111
16	00010000	17	00010001	18	00010010	19	00010011
20	00111101	21	00111101	22	00110010	23	00100110
24	00011000	25	00011001	26	00111111	27	00100111
28	00011100	29	00011101	30	00011110	31	00011111
32	01000000	33	01001111	34	01111111	35	01111011
36	01011011	37	01101100	38	01010000	39	01111101
40	01001101	41	01011101	42	01011100	43	01001110
44	01101011	45	01100000	46	01001011	47	01100001
48	11110000	49	11110001	50	11110010	51	11110011
52	11110100	53	11110101	54	11110110	55	11110111
56	11111000	57	11111001	58	01111010	59	01011110
60	01001100	61	01111110	62	01101110	63	01101111
64	01111100	65	11000001	66	11000010	67	11000011
68	11000100	69	11000101	70	11000110	71	11000111
72	11001000	73	11001001	74	11010001	75	11010010
76	11010011	77	11010100	78	11010101	79	11010110
80	11010111	81	11011000	82	11011001	83	11100010
84	11100011	85	11100100	86	11100101	87	11100110
88	11100111	89	11101000	90	11101001	91	01001010
92	11100000	93	01011010	94	01011111	95	01101101
96	01111001	97	10000001	98	10000010	99	10000011
100	10000100	101	10000101	102	10000110	103	10000111
104	10001000	105	10001001	106	10010001	107	10010010
108	10010011	109	10010100	110	10010101	111	10010110
112	10010111	113	10011000	114	10011001	115	10100010
116	10100011	117	10100100	118	10100101	119	10100110
120	10100111	121	10101000	122	10101001	123	11000000
124	01101010	125	11010000	126	10100001	127	00000111
128	00100000	129	00100001	130	00100010	131	00100011
132	00100100	133	00010101	134	00000110	135	00010111
136	00101000	137	00101001	138	00101010	139	00101011
140	00101100	141	00001001	142	00001010	143	00011011
144	00110100	145	00110101	146	00010110	147	00110011
148	00110100	149	00110101	150	00110110	151	00001000
152	00111001	153	00111010	154	00111011	155	00111011
156	00000100	157	00010100	158	00111110	159	11100001
160	01000000	161	01000010	162	01000010	163	01000100
164	01000101	165	01000110	166	01000111	167	01001000
168	01001001	169	01010001	170	01010010	171	01010011
172	01010100	173	01010101	174	01010110	175	01010111
176	01011000	177	01011001	178	01100010	179	01100011
180	01100100	181	01100101	182	01100110	183	01100111
184	01101000	185	01101001	186	01110000	187	01110001
188	01110010	189	01110011	190	01110100	191	01110101
192	01110110	193	01110111	194	01111000	195	10000000
196	10001010	197	10001011	198	10001100	199	10001101
200	10001110	201	10001111	202	10010010	203	10011010
204	10011011	205	10011100	206	10011101	207	10011110
208	10011011	209	10100000	210	10101010	211	10101011
212	10101100	213	10101101	214	10101110	215	10101111
216	10110100	217	10110101	218	10110110	219	10110111
220	10110100	221	10110101	222	10110110	223	10110111
224	10111010	225	10111011	226	10111100	227	10111101
228	10111100	229	10111101	230	10111110	231	10111111
232	11001010	233	11001011	234	11001100	235	11001101
236	11001010	237	11001011	238	11001100	239	11001101
240	11011100	241	11011101	242	11011110	243	11011111
244	11101010	245	11101011	246	11101100	247	11101101
248	11101110	249	11101111	250	11111010	251	11111011
252	11111100	253	11111101	254	11111110	255	11111111

EBCDIC (ADDRESS) TO ASCII (DATA)

Addr	Data	Addr	Data	Addr	Data	Addr	Data
256	00000000	257	00000001	258	00000010	259	00000011
260	10011100	261	00001001	262	10000110	263	01111111
264	10010111	265	10001101	266	10001110	267	00001011
268	00001101	269	00001101	270	00001110	271	00001111
272	00010000	273	00010001	274	00010010	275	00010011
276	10011101	277	00001010	278	00001000	279	10000111
280	00011000	281	00011001	282	10010010	283	10001111
284	00011100	285	00011101	286	00011110	287	00011111
288	10000000	289	10000001	290	10000010	291	10000011
292	10000100	293	00001010	294	00010111	295	00011011
296	10001001	297	10010001	298	10001001	299	10010001
300	00011100	301	00000101	302	00000110	303	00000111
304	10010000	305	10010001	306	00010110	307	10010011
308	10010100	309	10010101	310	00000100	311	00000100
312	10011000	313	10011001	314	10011010	315	10011011
316	00010100	317	00010101	318	00011001	319	00011010
320	00100000	321	10100000	322	10100001	323	10100010
324	10100011	325	10100100	326	10100101	327	10100110
328	10100111	329	10101000	330	01011011	331	00101110
332	00111100	333	00101000	334	00101011	335	00100001
336	00100110	337	10101001	338	10101010	339	10101011
340	10101100	341	10101101	342	10101110	343	10101111
344	10110000	345	10110001	346	01011101	347	00100100
348	00101010	349	00101001	350	00111011	351	01011110
352	00101101	353	00101111	354	10110010	355	10110011
356	10110100	357	10110101	358	10110110	359	10110111
360	10111000	361	10111001	362	01111100	363	00101100
364	00100101	365	01011111	366	00111110	367	00111111
368	10111010	369	10111011	370	10111100	371	10111101
372	10111110	373	10111111	374	11000000	375	11000001
376	11000010	377	01100000	378	00111010	379	00100011
380	01000000	381	00100111	382	00111101	383	00100010
384	11000011	385	01100001	386	01100010	387	01100011
388	01100100	389	01100101	390	01100110	391	01100111
392	01101000	393	01101001	394	11000100	395	11000101
396	11000110	397	11000111	398	11001000	399	11001001
400	11001010	401	01101010	402	01101011	403	01101100
404	01101101	405	01101110	406	01101111	407	01110000
408	01110001	409	01110010	410	11001011	411	11001100
412	11001101	413	11001110	414	11001111	415	11010000
416	11010001	417	01111110	418	01110011	419	01110100
420	01110101	421	01110110	422	01110111	423	01111000
424	01111001	425	01111010	426	11010010	427	11010011
428	11010100	429	11010101	430	11010110	431	11010111
432	11011000	433	11011001	434	11011010	435	11011011
436	11011100	437	11011101	438	11011110	439	11011111
440	11100000	441	11100001	442	11100010	443	11100011
444	11100100	445	11100101	446	11100110	447	11100111
448	01111011	449	01000001	450	01000010	451	01000011
452	01000100	453	01000101	454	01000110	455	01000111
456	01001000	457	11101000	458	11101001	459	11101010
460	11101011	461	11101100	462	11101101	463	11101110
464	01111101	465	01001010	466	01001011	467	01001100
468	01001101	469	01001110	470	01001111	471	01010000
472	01010001	473	01010010	474	11101110	475	11101111
476	11110000	477	11110001	478	11110010	479	11110011
480	01010100	481	10011111	482	01010011	483	01010100
484	01010101	485	01010110	486	01010111	487	01011000
488	01011001	489	01011010	490	11110100	491	11110101
492	11110110	493	11110111	494	11111000	495	11111001
496	00110000	497	00110001	498	00110010	499	00110011
500	00110100	501	00110101	502	00110110	503	00110111
504	00111000	505	00111001	506	11111010	507	11111011
508	11111100	509	11111101	510	11111110	511	11111111

MOSTEK®

8K-BIT MOS READ-ONLY MEMORY
MK30000(P/N)

FEATURES

☐ High performance replacement for Intel 2308/8308, and TI 4700

☐ 350ns max access time

☐ Single +5V ±10% power supply

☐ Contact programmed for fast turn-around

☐ Two programmable chip selects

☐ Inputs and three-state outputs TTL compatible

☐ Eight bit output for use with microprocessor systems

☐ Pin compatible with MK 2708 EPROM

DESCRIPTION

The MK 30000 is a 8,192 bit Read Only Memory designed as a high performance replacement for the Intel 2308/8308 and the TI 4700. The MK 30000 is organized as a 1K x 8 array which makes the device very attractive for use with 8-bit microprocessors such as the F8, 8080, 6800, Z-80 or any memory application requiring a high performance, high bit density ROM.

The device uses a single +5V (±10% tolerance) power supply. The two chip select inputs can be programmed for any desired combination of active high's or low's. These programmable chip select inputs coupled with the three-state TTL compatible outputs provide a high performance memory circuit with extremely simple interface requirements.

An outstanding feature of the MK 30000 is the use of contact programming instead of gate mask programming. Since the contact mask is applied at a later processing stage, wafers can be partially processed and stored. When an order is received, a contact mask, which represents the desired bit pattern, is generated and applied to the wafers. Only a few processing steps are left to complete the part. Therefore, the use of contact programming reduces the turnaround time for a custom ROM.

The MK 30000 is fabricated with N-channel silicon gate MOS technology for optimum size and circuit performance. Ion-implantation is utilized to allow full TTL compatibility at the inputs and outputs. All inputs are protected against static charge.

FUNCTIONAL DIAGRAM
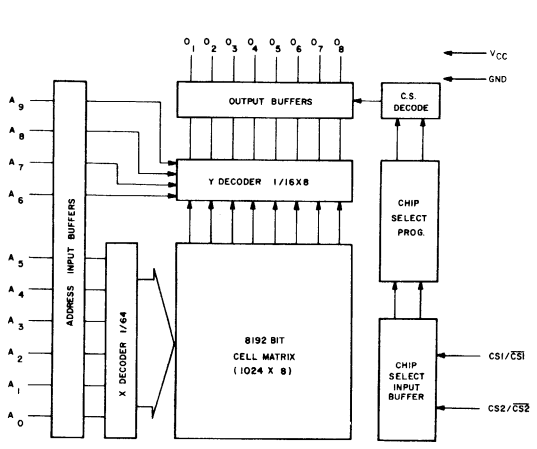
PIN CONNECTIONS
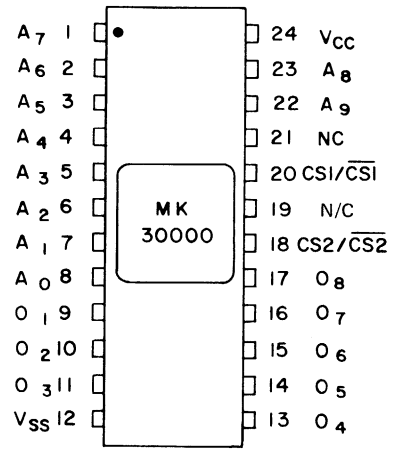
ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Terminal Relative to Ground . . . . —0.5V to + 7V

Operating Temperature T_A (Ambient) . . . . 0°C to + 70°C

Storage Temperature — Ceramic (Ambient) . . . . —65°C to + 150°C

Storage Temperature — Plastic (Ambient) . . . . —55°C to +125°C

Power Dissipation . . . . 1 Watt

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS
(V_{CC} = 5V ± 10%; 0°C ⩽ T_A ⩽ + 70°C)

	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Power Supply Voltage	4.5	5.0	5.5	Volts	6
V_{IL}	Input Logic 0 Voltage	—0.5		0.8	Volts	
V_{IH}	Input Logic 1 Voltage	2.0		V_{CC}	Volts	

DC ELECTRICAL CHARACTERISTICS
(V_{CC} = 5V ± 10%; 0°C ⩽ T_A ⩽ + 70°C)[6]

	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC}	V_{CC} Power Supply Current		60	mA	1
$I_{I(L)}$	Input Leakage Current		10	μA	2
$I_{O(L)}$	Output Leakage Current		10	μA	3
V_{OL}	Output Logic 0 Voltage @ I_{OUT} = 3.3mA		0.4	volts	
V_{OH}	Output Logic 1 Voltage @ I_{OUT} = —220 μA	2.4	V_{CC}	volts	

AC ELECTRICAL CHARACTERISTICS
(V_{CC} = 5V ± 10%; 0°C ⩽ T_A ⩽ + 70°C)[6]

	PARAMETER	MIN	MAX	UNITS	NOTES
t_{ACC}	Address to output delay time		350	ns	4
t_{CS}	Chip select to output delay time		175	ns	4
t_{CD}	Chip deselect to output delay time		150	ns	4

CAPACITANCE

	PARAMETER	TYP	MAX	UNITS	NOTES
C_{IN}	Input Capacitance	6	8	pF	5
C_{OUT}	Output Capacitance	10	15	pF	5

NOTES:

1. All inputs 5.5V; Data Outputs open.
2. V_{IN} = 0V to 5.5V
3. Device unselected; V_{OUT} = 0V to 5.5V.
4. Measured with 2 TTL loads and 100pF, transition times = 20ns

5. Capacitance measured with Boonton Meter or effective capacitance calculated from the equation :
$C = \dfrac{I \triangle t}{\triangle V}$ with current equal to a constant 20mA.

6. A minimum 100 μs time delay is required after the application of V_{CC} (+5) before proper device operation is achieved.

TIMING DIAGRAM

$$\text{ADDRESS} \quad \begin{array}{l} V_{IH} \\ V_{IL} \end{array} \quad \text{VALID}$$

$$t_{ACC}$$
$$t_{CS}$$
$$t_{CD}$$

$$\text{PROGRAMMABLE CHIP SELECTS} \quad \begin{array}{l} V_{IH} \\ V_{IL} \end{array} \quad \text{VALID}$$

$$\text{DATA OUTPUT} \quad \begin{array}{l} V_{OH} \\ V_{OL} \end{array} \quad \text{OPEN} \quad \text{VALID} \quad \text{OPEN}$$
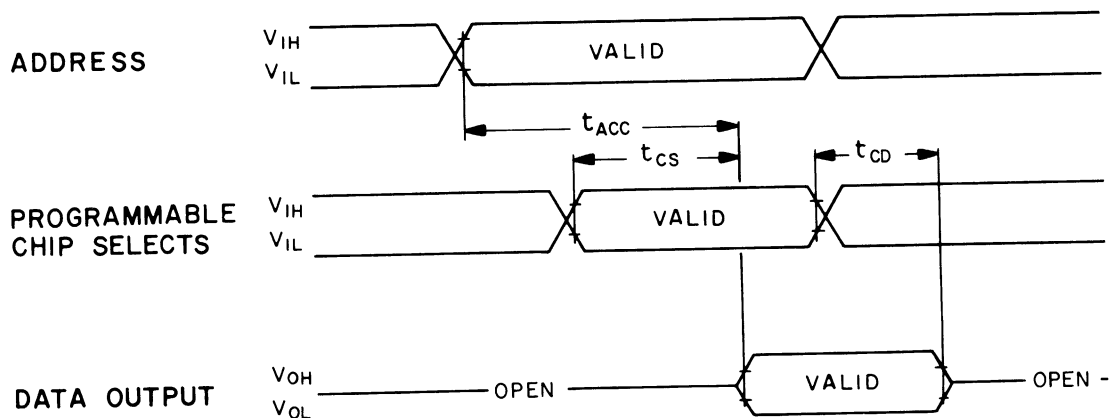
MOSTEK 30000 ROM PUNCHED CARD CODING FORMAT [1]

FIRST CARD

COLS	INFORMATION FIELD
1-30	Customer
31-50	Customer Part Number
60-72	MOSTEK Part Number [2]

SECOND CARD

1-30	Engineer at Customer Site
31-50	Direct Phone Number for Engineer

THIRD CARD

1-5	MOSTEK Part Number [2]
33	Chip Select One "1" = CS_1 or "0" = $\overline{CS}_1$
35	Chip Select Two "1" = CS_2 or "0" = $\overline{CS}_2$

FOURTH CARD

1-9	Data Format [3]
15-28	Logic - ("Positive Logic" or "Negative Logic")
35-57	Verification Code [4]

DATA FORMAT [3]

MOSTEK OR INTEL

MOSTEK FORMAT
64 data cards (16 data words/card)
with the following format:

COLS	INFORMATION FIELD
1-4	Four digit octal address of first output word on card
5-7	Three digit octal output word specified by address in column 1-4
8-52	Next fifteen output words, each word consists of three octal digits.

NOTES:

1. Positive or negative logic formats are accepted as noted in the fourth card.
2. Assigned by MOSTEK; may be left blank.
3. MOSTEK or Intel Punched card coding format may be used. Specify which card format used by punching either "MOSTEK" or "Intel". Start at column one.
4. Punches as: (a) VERIFICATION HOLD - i.e. customer verification of the data as reproduced by MOSTEK is required prior to production of the ROM. To accomplish this MOSTEK supplies a copy of its Customer Verification Data Sheet (CVDS) to the customer.
   (b) VERIFICATION PROCESS - i.e. the customer will receive a CVDS but production will begin prior to receipt of customer verification; (c) VERIFICATION NOT NEEDED - i.e. the customer will not receive a CVDS and production will begin immediately.

MOSTEK®

16K-BIT DYNAMIC ROM
MK28000(P/N)

FEATURES

☐ 600 ns Maximum Access Time

☐ Low Power Dissipation
 Active – 0.02 mW/bit Typ.
 Inactive – .007 mW/bit Typ.

☐ EA 4900 and EA 4800 Pin-for-pin Replacement

☐ 2K x 8 or 4K x 4 organization with Open Drain Outputs

☐ Standard Supplies +5 volts, – 12 volts

☐ Ion-Implanted for Full TTL/DTL Compatibility

DESCRIPTION

The MK 28000 is a mask programmable read only memory utilizing low-threshold Ion-Implant, P-Channel technology. The MK 28000 is a pin-for-pin replacement for the EA 4900. The MK 28000 may be organized as either a 2K x 8 or 4K x 4 memory.

The MK 28000 open drain outputs are divided into two groups with one Output Enable line controlling each group of outputs. This feature allows the MK 28000 to be either a 2K x 8 or a 4K x 4 memory without any internal mask changes. For a 2K x 8 organization, the Output Enables (OE_1, OE_2) are tied together. For a 4K x 4 organization, the four outputs associated with OE_1 are wire-ORed to the four outputs associat-

ed with OE_2. OE_1 and OE_2 are inverted with respect to each other and used as the twelfth address input in the 4K x 4 organization.

The internal circuitry of the MK 28000 is dynamic. This features means low standby power consumption when the ROM is not being addressed.

All inputs are protected against static charge accumulation. Pullup resistors on all inputs are available as a programmable option.

With no address lead time required, system design is simplified; address and $\overline{AR}$ may appear simultaneously.

FUNCTIONAL DIAGRAM

PIN CONNECTIONS

ABSOLUTE MAXIMUM RATINGS

Voltage on any terminal relative to V$_{SS}$ . . . . +0.3V to −20V
Operating temperature range (Ambient) . . . . .0°C to 70°C
Storage temperature range (Ambient) Ceramic . . . .−65°C to +150°C
Storage temperature range (Ambient) Plastic . . . .−55°C to +125°C

	PARAMETER	MIN	TYP	MAX	COMMENTS
V$_{SS}$	Supply Voltage	+4.75V	+5V	+5.25V	
	TTL Reference	−	0	−	
V$_{GG}$	Supply Voltage	−12.6V	−12V	−11.4V	
V$_{IL}$	Input Voltage, Logic "0"	V$_{GG}$		+.8V	
V$_{IH}$	Input Voltage, Logic "1"	V$_{SS}$ − 1.5V		V$_{SS}$	Pullup resistors to V$_{SS}$(≈5K) available as an option

ELECTRICAL CHARACTERISTICS
(V$_{SS}$= +5.0V ±5%; V$_{DD}$= 0V; V$_{GG}$= −12V ±5%; 0°C ≤ T$_A$ ≤ 70°C)

	PARAMETER	MIN	TYP	MAX	COMMENTS
I$_{SS}$	Supply Current		20 mA	35 mA	See Note 1
I$_{GG}$	Supply Current		−20 mA	−35 mA	Inputs at V$_{SS}$
I$_{GG}$	Supply Current (Standby)		7 mA	12 mA	See Note 1
C$_{IN}$	Input Capacitance (Address & OE's)		8 pF	10 pF	See Note 2
C$_{IN}$	Input Capacitance ($\overline{AR}$)		12 pF	15 pF	See Note 2
I$_{IN}$	Input Leakage			10 µA	See Note 3
R$_{IN}$	Input Pullup Resistors	3 KΩ		11 KΩ	Optional
V$_{OH}$	Output Voltage, Logic "1"	2.4V			See Note 4
I$_{OL}$	Output Leakage Current	−10 µA		+10 µA	V$_O$ = V$_{SS}$ −6V, T$_A$ = 25°C (outputs disabled)

	PARAMETER	MIN	TYP	MAX	COMMENTS
t_{PW}	$\overline{AR}$ Precharge Time	400 ns		∞	
t_C	Cycle Time	1 μs + t_R+ t_F			t_{ACC}+ t_{PW} + t_R + t_F
t_{ACC}	Access Time			600 ns	See note 4
t_{LD}	Address Lead Time	0			
t_{HD}	Address Hold Time	250 ns			
t_R	$\overline{AR}$ Rise Time			100 ns	
t_F	$\overline{AR}$ Fall Time			100 ns	
t_{HOLD}	Data Output Valid Time	2 μs			See note 5
t_{CD}	Output Disable Time			300 ns	See note 4
t_{OR}	Output Reset Time	75 ns	.	400 ns	See note 4

NOTES:

1. Outputs disconnected with no internal pullup resistors.
2. $V_{BIAS} - V_{SS} = 0V$; f = 1 MHz
3. This parameter is for inputs without pullups (optional)
4. With test circuit shown below
5. or, until the next precharge + T_{OR} [if $\overline{AR}$ makes a negative transition before t_{HOLD} (min) has elapsed].

TIMING
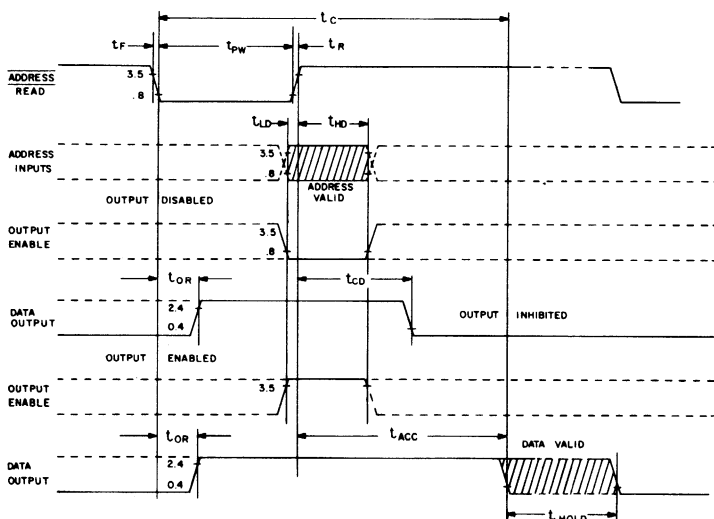
TEST CIRCUIT
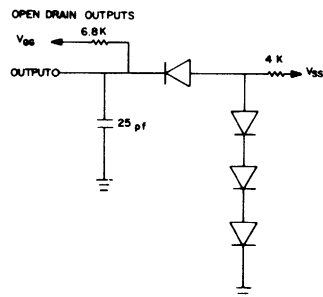
MOSTEK 28000 ROM Punched (Coding Format[1]

First Card

Cols	Information Field
1-30	Customer
31-50	Customer Part Number
60-72	MOSTEK Part Number[2]

Second Card

1-30	Engineer at Customer Site
31-50	Direct Phone Number for Engineer

Data Cards

MOSTEK Format   or   EA Format

1-4	Decimal Address
6-13	Output 08-01 (MSB Thru LSB)
15-17	Octal Equivalent of Output Data

Third Card

1-5	MOSTEK Part Number[2]
33	Input Pullups (0 = no, 1 = yes, 2 = Selectable Pull-up Option)[5]

Fourth Card

1-9	Data Format[3]
15-28	Logic — ("Positive Logic" or "Negative Logic")
35-57	Verification Code[4]

NOTES:

1. Positive or negative logic formats are accepted as noted in the fourth card.
2. Assigned by MOSTEK; may be left blank.
3. MOSTEK or Electronic Arrays Punched card coding format may be used. Specify which card format used by punching either "MOSTEK" or "EA". Start at column one.
4. Punches as:

   (a) VERIFICATION HOLD — i.e. customer verification of the data as reproduced by MOSTEK is required prior to production of the ROM. To accomplish this MOSTEK supplies a copy of its Customer Verification Data Sheet (CVDS) to the customer.

   (b) VERIFICATION PROCESS — i.e. the customer will receive a CVDS but production will begin prior to receipt of customer verification

   (c) VERIFICATION NOT NEEDED — i.e. the customer will not receive a CVDS and production will begin immediately.

5. Columns 34-47 represent A1—A11, $\overline{AR}$, OE1, OE2 respectively.   0= No pull-up, 1 = Pull-up

MOSTEK®

16 K-BIT MOS READ-ONLY MEMORY

MK31000(P/N)-3

FEATURES

☐ High performance replacement for Intel 2316A/8316A and General Instrument RO-3-8316A

☐ Maximum access time 550ns

☐ Single +5V ±10% power supply

☐ Contact programmed for fast turn-around

☐ Three programmable chip selects

☐ Inputs and three-state outputs TTL compatible

☐ Outputs drive 2 TTL loads and 100pF

☐ Low power

☐ Eight bit output for use with microprocessor systems

DESCRIPTION

The MK 31000 is a 16,384 bit Read Only Memory designed as a high performance replacement for the Intel 2316A/8316A and the General Instrument RO-3-8316A. The MK 31000 is organized as a 2K x 8 array which makes the device very attractive for use with 8 bit microprocessors such as the F8, 8080, 6800, Z-80 or any memory application requiring a high performance, high bit density ROM.

The device uses a single +5 volt (± 10% tolerance) power supply. The three chip select inputs can be programmed for any desired combination of active high's or low's. These programmable chip select inputs coupled with the three-state TTL compatible outputs provide a high performance memory circuit with extremely simple interface requirements.

An outstanding feature of the MK 31000 is the use of contact programming instead of gate mask programming. Since the contact mask is applied at a later processing stage, wafers can be partially processed and stored. When an order is received, a contact mask, which represents the desired bit pattern, is generated and applied to the wafers. Only a few processing steps are left to complete the part. Therefore, the use of contact programming reduces the turnaround time for a custom ROM.

The MK 31000 is fabricated with N-channel silicon gate MOS technology for optimum size and circuit performance. Ion-implantation is utilized to allow full TTL compatibility at the inputs and outputs. All inputs are protected against static charge.

FUNCTIONAL DIAGRAM
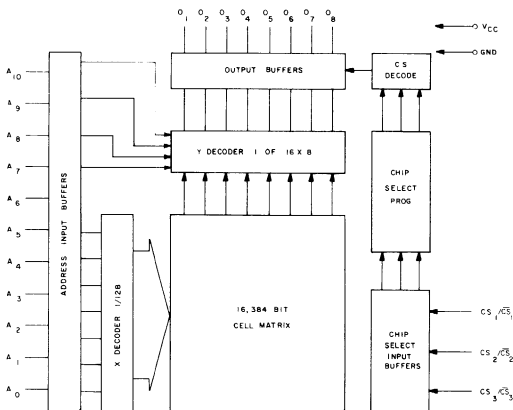
PIN CONNECTIONS
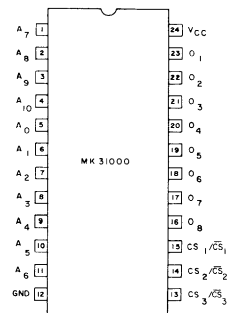
ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Terminal Relative to Ground . . . . —0.5V to +7V
Operating Temperature T_A (Ambient) . . . . .0°C to +70°C
Storage Temperature (Ambient) Ceramic . . . .—65°C to +150°C
Storage Temperature (Ambient) Plastic . . . .—55°C to +125°C
Power Dissipation 1W

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED D C OPERATING CONDITIONS
(V_{CC} = 5V ± 10%; 0°C $\leqslant T_A \leqslant$ + 70 C)

	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Power Supply Voltage	4.5	5.0	5.5	Volts	
V_{IL}	Input Logic 0 Voltage	—0.5		0.8	Volts	
V_{IH}	Input Logic 1 Voltage	2.0		V_{CC}	Volts	

D C ELECTRICAL CHARACTERISTICS
(V_{CC} = 5V ± 10%; 0°C $\leqslant T_A \leqslant$ + 70°C)

	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC}	V_{CC} Power Supply Current		60	mA	1
$I_{I(L)}$	Input Leakage Current		10	μ A	2
$I_{O(L)}$	Output Leakage Current		10	μ A	3
V_{OL}	Output Logic 0 Voltage @ I_{OUT} = 3.3mA		0.4	volts	
V_{OH}	Output Logic 1 Voltage @ I_{OUT} = —220 μA	2.2	V_{CC}	volts	

A C ELECTRICAL CHARACTERISTICS
(V_{CC} = 5V ± 10%; 0°C $\leqslant T_A \leqslant$ + 70°C)

	PARAMETER	MIN	MAX	UNITS	NOTES
t_{ACC}	Address to output delay time		550	ns	4
t_{CS}	Chip select to output delay time		250	ns	4
t_{CD}	Chip deselect to output delay time		150	ns	4

CAPACITANCE

	PARAMETER	TYP	MAX	UNITS	NOTES
C_{IN}	Input Capacitance	6	8	pf	5
C_{OUT}	Output Capacitance	10	15	pf	5

NOTES:

1. All inputs 5.5V ; Data Outputs open.
2. V_{in} = 0V to 5.5V.
3. Device unselected; V_{out} = 0V to 5.5V
4. Measured with 2 TTL loads and 100pf.
5. Capacitance measured with Boonton Meter or effective capacitance calculated from the equation $C = \dfrac{I \Delta t}{\Delta V}$ with current equal to a constant 20mA.

TIMING DIAGRAM
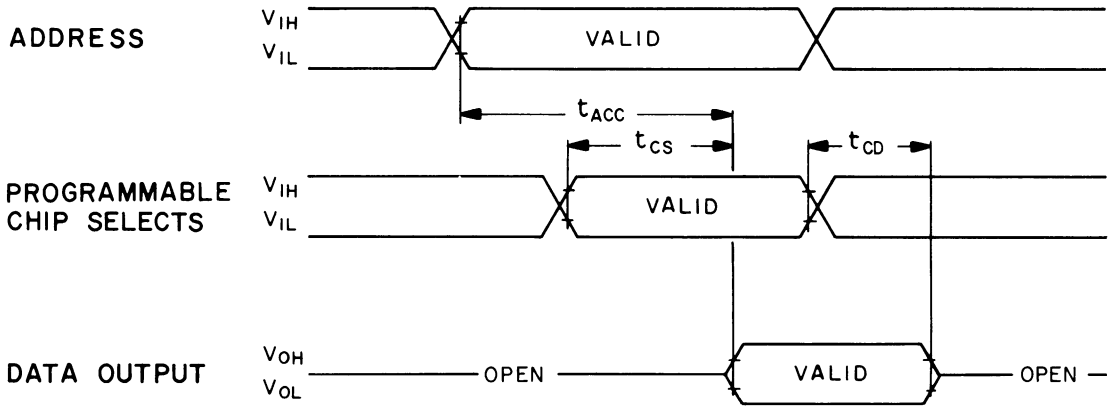
MOSTEK 31000 ROM PUNCHED CARD CODING FORMAT [1]

FIRST CARD

COLS	INFORMATION FIELD
1-30	Customer
31-50	Customer Part Number
60-72	MOSTEK Part Number (2)

SECOND CARD

1-30	Engineer at Customer Site
31-50	Direct Phone Number for Engineer

THIRD CARD

1-5	MOSTEK Part Number (2)
33	Chip Select One "1" = CS_1 or "0" = $\overline{CS}_1$
35	Chip Select Two "1" = CS_2 or "0" = $\overline{CS}_2$
37	Chip Select Three "1" = CS_3 or "0" = $\overline{CS}_3$

FOURTH CARD

1-9	Data Format (3)
15-28	Logic - ("Positive Logic" or "Negative Logic")
35-57	Verification Code (4)

DATA FORMAT

MOSTEK OR INTEL

MOSTEK FORMAT
128 data cards (16 data words/card) with the following format:

COLS	INFORMATION FIELD
1-4	Four digit octal address of first output word on card
5-7	Three digit octal output word specified by address in column 1-4
8-52	Next fifteen output words, each word consists of three octal digits.

NOTES:

1. Positive or negative logic formats are accepted as noted in the fourth card.
2. Assigned by MOSTEK; may be left blank.
3. MOSTEK or Intel Punched card coding format may be used. Specify which card format used by punching either "MOSTEK" or "Intel". Start at column one.
4. Punches as: (a) VERIFICATION HOLD - i.e. customer verification of the data as reproduced by MOSTEK is required prior to production of the ROM. To accomplish this MOSTEK supplies a copy of its Customer Verification Data Sheet (CVDS) to the customer.
   (b) VERIFICATION PROCESS - i.e. the customer will receive a CVDS but production will begin prior to receipt of customer verification; (c) VERIFICATION NOT NEEDED - i.e. the customer will not receive a CVDS and production will begin immediately.

MOSTEK®

16K-BIT MOS READ-ONLY MEMORY

MK34000(P/N)-3

FEATURES

☐ 2K x 8 organization with static interface

☐ 350ns max access time

☐ Single +5V ± 10% power supply

☐ 330mW max power dissipation

☐ Contact programmed for fast turn-around

☐ Three programmable chip selects

☐ Inputs and three-state outputs—TTL compatible

☐ Outputs drive 2 TTL loads and 100pF

DESCRIPTION

The MK 34000 is a new generation N-channel silicon gate MOS Read Only Memory circuit organized as 2048 words by 8 bits. As a state-of-the-art device, the MK 34000 incorporates advanced circuit techniques designed to provide maximum circuit density and reliability with highest possible performance, while maintaining low power dissipation and wide operating margins.

The MK 34000 requires a single +5 volt (± 10% tolerance) power supply and has complete TTL compatibility at all inputs and outputs (a feature made possible by MOSTEK's Ion-implantation technique). The three chip select inputs can be programmed for any desired combination of active high's or low's or even an optional "DON'T CARE" state. The convenient static operation of the MK 34000 coupled with the programmable chip select inputs and three-state TTL compatible outputs results in extremely simple interface requirements.

An outstanding feature of the MK 34000 is the use of contact programming over gate mask programming. Since the contact mask is applied at a later processing stage, wafers can be partially processed and stored. When an order is received, a contact mask, which represents the desired bit pattern, is generated and applied to the wafers. Only a few processing steps are left to complete the part. Therefore, the use of contact programming reduces the turnaround time for a custom ROM.

Any application requiring a high performance, high bit density ROM can be satisfied by this device. The MK 34000 is ideally suited for 8-bit microprocessor systems such as those which utilize the Z80 or F8. The MK 34000 also provides significant cost advantages over PROM.

FUNCTIONAL DIAGRAM

PIN CONNECTIONS

*Programmable Chip Selects

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Terminal Relative to Ground . . . . −0.5V to + 7V

Operating Temperature T_A (Ambient) . . . . 0℃ to + 70℃

Storage Temperature — Ceramic (Ambient) . . . . −65℃ to + 150℃

Storage Temperature — Plastic (Ambient) . . . . −55℃ to +125℃

Power Dissipation . . . . 1 Watt

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS
(V_{CC} = 5V ± 10%; 0℃ ⩽ T_A ⩽ + 70℃)

	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Power Supply Voltage	4.5	5.0	5.5	Volts	6
V_{IL}	Input Logic 0 Voltage	−0.5		0.8	Volts	
V_{IH}	Input Logic 1 Voltage	2.0		V_{CC}	Volts	

D C ELECTRICAL CHARACTERISTICS
(V_{CC} = 5V ± 10%; 0℃ ⩽ T_A ⩽ + 70℃)[6]

	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC}	V_{CC} Power Supply Current		60	mA	1
$I_{I(L)}$	Input Leakage Current		10	μA	2
$I_{O(L)}$	Output Leakage Current		10	μA	3
V_{OL}	Output Logic 0 Voltage @ I_{OUT} = 3.3mA		0.4	volts	
V_{OH}	Output Logic 1 Voltage @ I_{OUT} = −220 μA	2.4	V_{CC}	volts	

A C ELECTRICAL CHARACTERISTICS
(V_{CC} = 5V ± 10%; 0℃ ⩽ T_A ⩽ + 70℃)[6]

	PARAMETER	MIN	MAX	UNITS	NOTES
t_{ACC}	Address to output delay time		350	ns	4
t_{CS}	Chip select to output delay time		175	ns	4
t_{CD}	Chip deselect to output delay time		150	ns	4

CAPACITANCE

	PARAMETER	TYP	MAX	UNITS	NOTES
C_{IN}	Input Capacitance	6	8	pF	5
C_{OUT}	Output Capacitance	10	15	pF	5

NOTES:

1. All inputs 5.5V; Data Outputs open.
2. V_{IN} = 0V to 5.5V
3. Device unselected; V_{OUT} = 0V to 5.5V.
4. Measured with 2 TTL loads and 100pF, transition times = 20ns

5. Capacitance measured with Boonton Meter or effective capacitance calculated from the equation :
$C = \dfrac{I \Delta t}{\Delta V}$ with current equal to a constant 20mA.

6. A minimum 100 μs time delay is required after the application of V_{CC} (+5) before proper device operation is achieved.

ADDRESS

V_{IH}
V_{IL}

VALID

t_{ACC}

t_{CS}

t_{CD}

PROGRAMMABLE
CHIP SELECTS

V_{IH}
V_{IL}

VALID

DATA OUTPUT

V_{OH}
V_{OL}

OPEN

VALID

OPEN

*16K-BIT ROM
MK34000(P/N)-3*

* The chip select inputs can be user programmed so that either the input is enabled by a Logic 0 voltage (V_{IL}), a Logic 1 voltage (V_{IH}), or the input is always enabled (regardless of the state of the input). See chart below for programming instructions.

MOSTEK 34000 ROM PUNCHED CARD CODING FORMAT [1]

FIRST CARD

COLS	INFORMATION FIELD
1-30	Customer
31-50	Customer Part Number
60-72	MOSTEK Part Number (2)

SECOND CARD

1-30	Engineer at Customer Site
31-50	Direct Phone Number for Engineer

THIRD CARD

1-5	MOSTEK Part Number (2)
33	Chip Select One "1" = CS_1 or "0" = $\overline{CS_1}$ or "2" = Don't Care
35	Chip Select Two "1" = CS_2 or "0" = $\overline{CS_2}$ or "2" = Don't Care
37	Chip Select Three "1" = CS_3 or "0" = $\overline{CS_3}$ or "2" = Don't Care

FOURTH CARD

1-9	Data Format (3)
15-28	Logic - ("Positive Logic" or "Negative Logic")
35-57	Verification Code (4)

DATA FORMAT

128 data cards (16 data words/card) with the following format:

COLS	INFORMATION FIELD
1-4	Four digit octal address of first output word on card
5-7	Three digit octal output word specified by address in column 1-4
8-52	Next fifteen output words, each word consists of three octal digits.

NOTES:

1. Positive or negative logic formats are accepted as noted in the fourth card.
2. Assigned by MOSTEK; may be left blank.
3. MOSTEK punched card coding format should be used. Punch "MOSTEK" starting in column one.
4. Punches as: (a) VERIFICATION HOLD - i.e. customer verification of the data as reproduced by MOSTEK is required prior to production of the ROM. To accomplish this MOSTEK supplies a copy of its Customer Verification Data Sheet (CVDS) to the customer.
   (b) VERIFICATION PROCESS - i.e. the customer will receive a CVDS but production will begin prior to receipt of customer verification; (c) VERIFICATION NOT NEEDED - i.e. the customer will not receive a CVDS and production will begin immediately.

MOSTEK®

16K-BIT MOS READ-ONLY MEMORY

MK34073 (P/N)-3

FEATURES

□ 2K x 8 organization with static interface

□ 350ns max access time

□ Single +5V ± 10% power supply

□ 330mW max power dissipation

□ Full ASCII compatible character sets (128 characters)

□ Contains both Horizontal (5x8) and Vertical (5x7) character sets.

□ Inputs and three-state outputs—TTL compatible

□ Outputs drive 2 TTL loads and 100pF

DESCRIPTION

The MK34073 is a pre-programmed version of MOS-TEK's high performance MK34000 16K bit ROM. The MK34073 incorporates advanced circuit techniques to provide maximum circuit density and reliability along with high speed (350ns access) and low power operation. The MK34073 requires a single +5 volt (± 10% tolerance) power supply and has complete TTL compatibility on all inputs and outputs.

The MK34073 is pre-programmed for character generator applications. It contains two separate character fonts for use in raster scan or matrix printer applications. Each font is ASCII compatible

and contains augmented character sets with all upper and lower case characters. Font selection is accomplished by setting Pin 19 (HV) to a logic '1' ($V_{IN} \geqslant 2.0$ Volts) to select the 5 x 8 horizontal output character set or to a logic '0' ($V_{IN} \leqslant 0.8$ Volts) to select the 5 x 7 vertical output character set. Character selection is made by placing the ASCII code of the desired character on A3-A9 and row/column selection is made on A0-A2.

Electrical specifications for the MK34073 can be found on the MK34000 data sheet available from MOSTEK.

FUNCTIONAL DIAGRAM
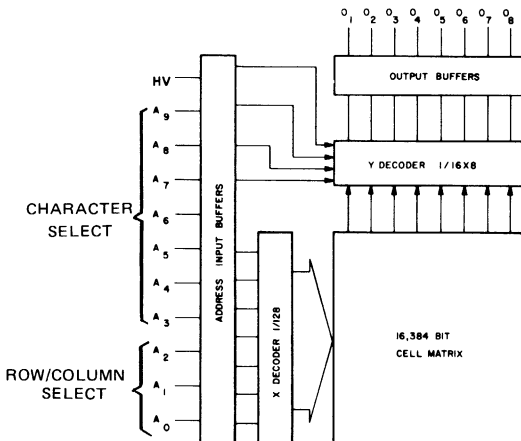
PIN CONNECTIONS
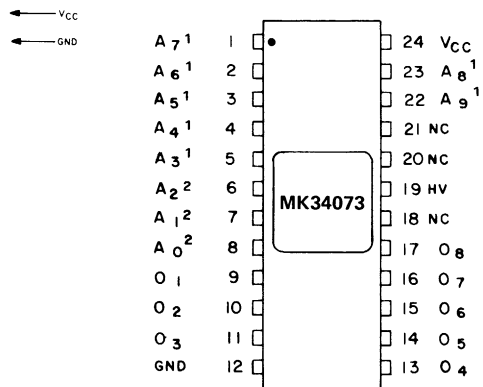
1 Character Select A9 = MSB
2 Row/Column Select A2 = MSB

COLUMN OUTPUT (HV = 0)

HORIZONTAL OUTPUT (HV = 1)

50

MOSTEK®

HIGH PERFORMANCE

64K-BIT MOS READ-ONLY MEMORY

MK36000(P/N)-4

FEATURES

☐ MK36000 8K x 8 Organization— "Edge Activated" * operation ($\overline{CE}$)

☐ Maximum access time: 250ns (-4)

☐ Single +5V ± 10% power supply

☐ Low Power Dissipation—220mW max active

☐ Low Standby Power Dissipation— 35mW typical ($\overline{CE}$ High)

☐ On chip latches for addresses

☐ Inputs and three-state outputs-TTL compatible

☐ Outputs drive 2 TTL loads and 100 pF

☐ Standard 24 pin DIP (EPROM Pin Out Compatible)

DESCRIPTION

The MK36000 is a new generation N-channel silicon gate MOS Read Only Memory, organized as 8192 words by 8 bits. As a state-of-the-art device, the MK 36000 incorporates advanced circuit techniques designed to provide maximum circuit density and reliability with the highest possible performance, while maintaining low power dissipation and wide operating margins.

The MK36000 utilizes what is fast becoming an industry standard method of device operation. Use of a static storage cell with clocked control periphery allows the circuit to be put into an automatic low power standby mode. This is accomplished by maintaining the chip enable ($\overline{CE}$) input at a TTL high level. In this mode, power dissipation is reduced to typically 35mW, as compared to unclocked devices which

draw full power continuously. In system operation, a device is selected by the $\overline{CE}$ input, while all others are in a low power mode, reducing the overall system power. Lower power means reduced power supply cost, less heat to dissipate and an increase in device and system reliability.

The edge activated chip enable also means greater system flexibility and an increase in system speed. The MK36000 features onboard address latches controlled by the $\overline{CE}$ input. Once the address hold time specification has been met, new address data can be applied in anticipation of the next cycle. Outputs can be wire- 'OR'ed together, and a specific device can be selected by utilizing the $\overline{CE}$ input with no bus conflict on the outputs. The $\overline{CE}$ input allows the fastest access times yet available in 5 volt only

FUNCTIONAL DIAGRAM (MK 36000)
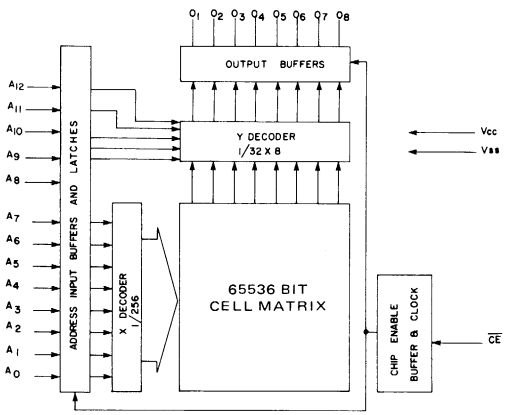
PIN CONNECTIONS
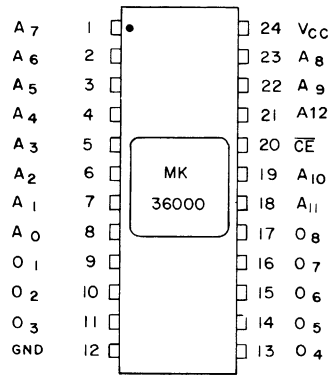
* Trademark of Mostek Corporation

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Terminal Relative to V_{SS} .... −0.5V to + 7V

Operating Temperature T_A (Ambient) .... 0°C to + 70° C

Storage Temperature — Ceramic (Ambient) .... −65°C to + 150°C

Power Dissipation .... 1 Watt

RECOMMENDED DC OPERATING CONDITIONS[6]
(0°C ⩽ T_A ⩽ + 70°C)

	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Power Supply Voltage	4.5	5.0	5.5	Volts	6
V_{IL}	Input Logic 0 Voltage	−0.5		0.8	Volts	
V_{IH}	Input Logic 1 Voltage	2.0		V_{CC}	Volts	

D C ELECTRICAL CHARACTERISTICS
(V_{CC} = 5V ± 10%) (0°C ⩽ T_A ⩽ + 70°C)[6]

	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
I_{CC1}	V_{CC} Power Supply Current (Active)			40	mA	1
I_{CC2}	V_{CC} Power Supply Current (Standby)		7		mA	7
$I_{I(L)}$	Input Leakage Current	−10		10	μA	2
$I_{O(L)}$	Output Leakage Current	−10		10	μA	3
V_{OL}	Output Logic "0" Voltage @ I_{OUT} = 3.3mA			0.4	volts	
V_{OH}	Output Logic "1" Voltage @ I_{OUT} = −220 μA	2.4			volts	

A C ELECTRICAL CHARACTERISTICS
(V_{CC} = 5V ± 10%) (0°C ⩽ T_A ⩽ + 70°C)[6]

	PARAMETER	MIN	MAX	UNITS	NOTES
t_C	Cycle Time	375		ns	4
t_{CE}	$\overline{CE}$ Pulse Width	250			4
t_{AC}	$\overline{CE}$ Access Time		250	ns	4
t_{OFF}	Output Turn Off Delay		60	ns	4
t_{AH}	Address Hold Time Referenced to $\overline{CE}$	60		ns	
t_{AS}	Address Setup Time Referenced to $\overline{CE}$	0		ns	
t_p	$\overline{CE}$ Precharge Time	125		ns	

NOTES:

1. Current is proportional to cycle rate. I_{CCI} is measured at the specified minimum cycle time.

2. V_{IN} = 0V to 5.5V

3. Device unselected; V_{OUT} = 0V to 5.5V

4. Measured with 2 TTL loads and 100pF, transistion times = 20ns

5. Capacitance measured with Boonton Meter or effective capacitance calculated from the equation:

   $C = \frac{\Delta Q}{\Delta V}$ with ΔV = 3 volts

6. A minimum 100 μs time delay is required after the application of V_{CC} (+5) before proper device operation is achieved.

7. $\overline{CE}$ high.

CAPACITANCE
(0°C ≤ TA ≤ 70°C)

	PARAMETER	TYP	MAX	UNITS	NOTES
CI	Input Capacitance	5		pF	5
CO	Output Capacitance	7		pF	5

TIMING DIAGRAM
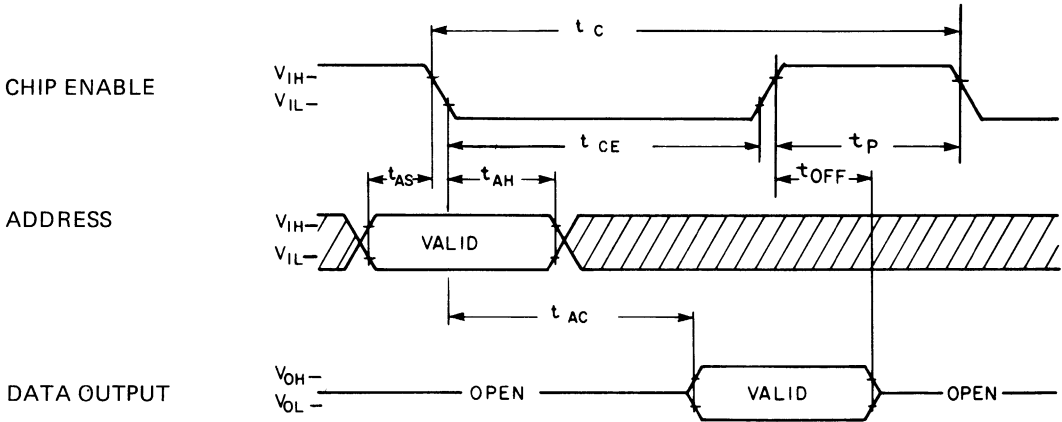
MK36000 ROM PUNCHED CARD CODING FORMAT (1 & 6)

FIRST CARD

COLS	INFORMATION FIELD
1-30	Customer
31-50	Customer Part Number
60-72	MOSTEK Part Number (2)

SECOND CARD

COLS	INFORMATION FIELD
1-30	Engineer at Customer Site
31-50	Direct Phone Number for Engineer

THIRD CARD

COLS	INFORMATION FIELD
1-5	MOSTEK Part Number (2)

FOURTH CARD

COLS	INFORMATION FIELD
1-9	Data Format (3)
15-28	Logic - ("Positive Logic" or "Negative Logic")
35-57	Verification Code (4)

DATA FORMAT

512 data cards (16 data words/card) with the following format:

COLS	INFORMATION FIELD
1-4	Four digit octal address of first output word on card
5-7	Three digit octal output word specified by address in column 1-4
8-52	Next fifteen output words, each word consists of three octal digits.

NOTES:

1. Positive or negative logic formats are accepted as noted in the fourth card.

2. Assigned by MOSTEK; may be left blank.

3. MOSTEK punched card coding format should be used. Punch "MOSTEK" starting in column one.

4. Punches as: (a) VERIFICATION HOLD - i.e. customer verification of the data as reproduced by MOSTEK is required prior to production of the ROM. To accomplish this MOSTEK supplies a copy of its Customer Verification Data Sheet (CVDS) to the customer.
(b) VERIFICATION PROCESS - i.e. the customer will receive a CVDS but production will begin prior to receipt of customer verification; (c) VERIFICATION NOT NEEDED - i.e. the customer will not receive a CVDS and production will begin immediately.

5. 512 cards for MK 36000

6. Please consult MOSTEK ROM Programming Guide for further details on other formats.

DESCRIPTION (Continued)

ROM's and imposes no loss in system operating flexibility over an unclocked device.

Other system oriented features include fully TTL compatible inputs and outputs. The three state outputs, controlled by the $\overline{CE}$ input, will drive a minimum of 2 standard TTL loads. The MK36000 operates from a single +5 volt power supply with a wide ± 10% tolerance, providing the widest operating margins available. The MK36000 is packaged in the industry standard 24 pin DIP.

Any application requiring a high performance, high bit density ROM can be satisfied by the MK36000 ROM. This device is ideally suited for 8 bit microprocessor systems such as those which utilize the Z-80. It can offer significant cost advantages over PROM.

OPERATION

The MK36000 is controlled by the chip enable ($\overline{CE}$) input. A negative going edge at the $\overline{CE}$ input will activate the device as well as strobe and latch the inputs into the onchip address registers. At access time the outputs will become active and contain the data read from the selected location. The outputs will remain latched and active until $\overline{CE}$ is returned to the inactive state.

Programming Data

MOSTEK is now able to utilize a wide spectrum of data input formats and media. Those presently available are listed in the following table:

Table 1

Acceptable Media	Acceptable Format
CARDS PAPER TAPE PROMS DATA LINK	MOSTEK INTEL CARD INTEL TAPE EA MOSTEK F-8 MOTOROLA 6800

MOSTEK®

HIGH PERFORMANCE

16K-BIT PROM
Electrically Programmable/Ultraviolet Erasable

MK2716(T)

16K-BIT EPROM

FEATURES

☐ Replacement for popular 2048x8 bit 2716 type EPROM

☐ Single +5 volt power supply during READ operation

☐ Fast Access Time: 450ns maximum

☐ Low Power Dissipation: 525 mW max active

☐ Power Down mode: 132 mW max standby

☐ Three State Output OR-tie capability

☐ Six modes of operation for greater system flexibility (see Table)

☐ Single programming requirement: single location programming with one 50 msec pulse

☐ Pin Compatible with MK34000 16K ROM

☐ TTL compatible in all operating modes

☐ Standard 24 pin DIP with transparent lid

DESCRIPTION

The MK2716 is a 2048x8 bit electrically programmable/ultraviolet erasable Read Only Memory. The circuit is fabricated with MOSTEK's advanced N-channel silicon gate technology for the highest performance and reliability. The MK2716 offers significant advantages over hardwired logic in cost, system flexibility, turnaround time and performance.

The MK2716 has many useful system oriented features including a POWER DOWN mode of oper-

MODE SELECTION

PIN \ MODE	PD/PGM (18)	$\overline{CS}$ (20)	V_{PP} (21)	OUTPUTS
READ	V_{IL}	V_{IL}	+5	Valid Out
DESELECT	Don't Care	V_{IH}	+5	Open
POWER DOWN	V_{IH}	Don't Care	+5	Open
PROGRAM	Pulsed V_{IL} to V_{IH}	V_{IH}	+25	Input
PROGRAM VERIFY	V_{IL}	V_{IL}	+25	Valid Out
PROGRAM INHIBIT	V_{IL}	V_{IH}	+25	Open
V_{CC} (24) = 5V all modes				

BLOCK DIAGRAM
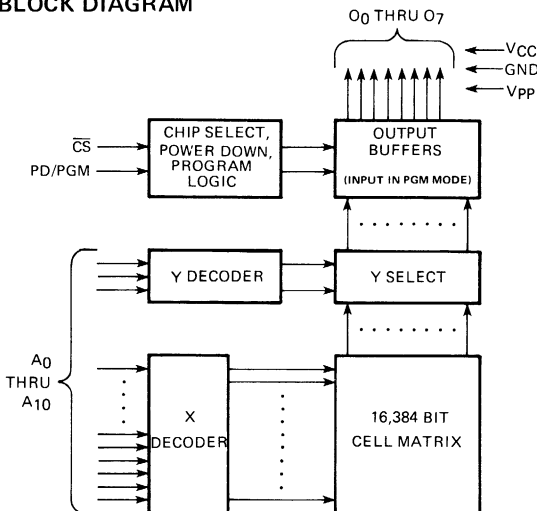
O_0 THRU O_7

PIN OUT

A_7	1	24	V_{CC}
A_6	2	23	A_8
A_5	3	22	A_9
A_4	4	21	V_{PP}
A_3	5	20	$\overline{CS}$
A_2	6	19	A_{10}
A_1	7	18	PD/PGM
A_0	8	17	O_7
O_0	9	16	O_6
O_1	10	15	O_5
O_2	11	14	O_4
GND	12	13	O_3

A_0 - A_{10} ADDRESSES
PD/PGM   POWER DOWN/PROGRAM
$\overline{CS}$ CHIP SELECT
O_0 - O_7 OUTPUTS
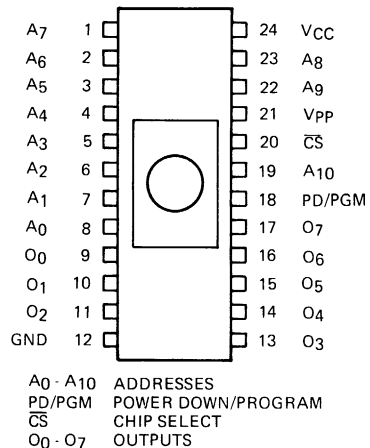
ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to V_{SS} . . . . −0.3V to +6V
(Except V_{PP})
Voltage on V_{PP} supply pin relative to V_{SS} . . . . −0.3V to +28V
Operating Temperature T_A (Ambient) . . . . $0°C \leqslant T_A \leqslant 70°C$
Storage Temperature (Ambient) . . . . $−65°C \leqslant T_A \leqslant +125°C$
Power Dissipation . . . . 1 Watt
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

READ OPERATION
RECOMMENDED D.C. OPERATING CONDITIONS AND CHARACTERISTICS[1,2,4,8]

$(0°C \leqslant T_A \leqslant 70°C)$ $(V_{CC} = +5V \pm 5\%, V_{PP} = V_{CC} \pm 0.6V)$[3]

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{IH}	Input High Voltage	2.2		$V_{CC}+1$	Volts	
V_{IL}	Input Low Voltage	0.1		0.8	Volts	
I_{CC1}	V_{CC} Standby Power Supply Current ($\overline{CS}=V_{IL}$; PD/PGM=V_{IH})		10	25	mA	2
I_{CC2}	V_{CC} Active Power Supply Current ($\overline{CS}=$PD/PGM=V_{IL})		57	100	mA	2
I_{PP1}	V_{PP} Current ($V_{PP} = 5.85V$)			5	mA	2,3
V_{OH}	Output High Voltage ($I_{OH} = -400\mu A$)	2.4			Volts	
V_{OL}	Output Low Voltage ($I_{OL} = 2.1mA$)			.45	Volts	
I_{IL}	Input Leakage Current ($V_{IN} = 5.25V$)			10	μA	
I_{OL}	Output Leakage Current ($V_{OUT} = 5.25V$)			10	μA	

A.C. CHARACTERISTICS[1,2,5]

$(0°C \leqslant T_A \leqslant 70°C)$ $(V_{CC} = +5V \pm 5\%, V_{PP} = 5V \pm 0.6V)$[3]

	PARAMETER	LIMITS		UNITS	NOTES
		MIN	MAX		
t_{ACC1}	Address to Output Delay (PD/PGM = $\overline{CS}$ = V_{IL})		450	ns	
t_{ACC2}	PD/PGM to Output Delay ($\overline{CS}$ = V_{IL})		450	ns	6
t_{CO}	Chip Select to Output Delay (PD/PGM = V_{IL})		120	ns	
t_{PF}	PD/PGM to Output Float ($\overline{CS}$ = V_{IL})	0	100	ns	
t_{DF}	Chip Deselect to Output Float (PD/PGM = V_{IL})	0	100	ns	
t_{OH}	Address to Output Hold (PD/PGM = $\overline{CS}$ = V_{IL})	0		ns	

CAPACITANCE
Capacitance (T_A = 25°C)[8]

	PARAMETER	TYP	MAX	UNITS	NOTES
C_{IN}	Input Capacitance	4	6	pF	7
C_{OUT}	Output Capacitance	8	12	pF	7

NOTES:
1. V_{CC} must be applied on or before V_{PP} and removed after or at the same time as V_{PP}.
2. V_{PP} and V_{CC} may be connected together except during programming, in which case the supply current is the sum of I_{CC} and I_{PP1}.
3. The tolerance on V_{PP} is to allow use of a driver circuit to switch V_{PP} from V_{CC} to +25V in the READ and PROGRAM mode respectively.
4. All voltages with respect to V_{SS}.
5. Load conditions = ITTL load and 100pF., t_r = t_f = 20ns, reference levels are 1V or 2V for inputs and .8V and 2V for outputs.
6. t_{ACC2} is referenced to PD/PGM or the addresses, whichever occurs last.
7. Effective Capacitance calculated from the equation $C = \frac{\Delta Q}{\Delta V}$ where ΔV = 3V
8. Typical numbers are for T_A = 25°C and V_{CC} = 5.0V

TIMING DIAGRAM
READ CYCLE (PD/PGM = V_{IL})
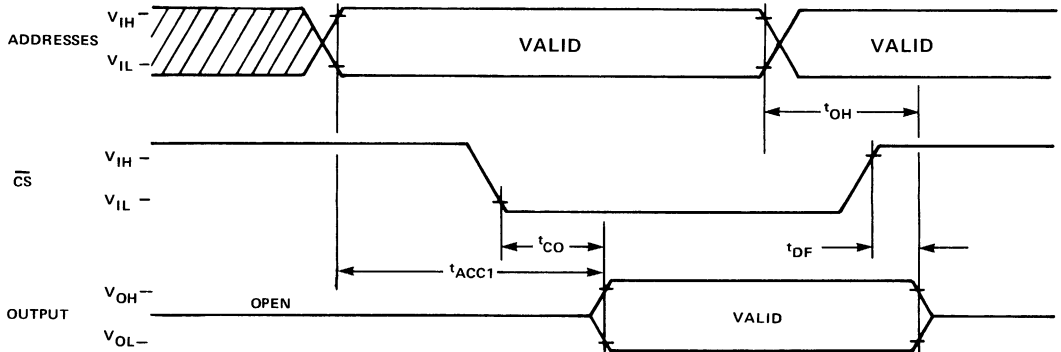
STANDBY POWER
DOWN MODE
($\overline{CS}$ = V_{IL})

57
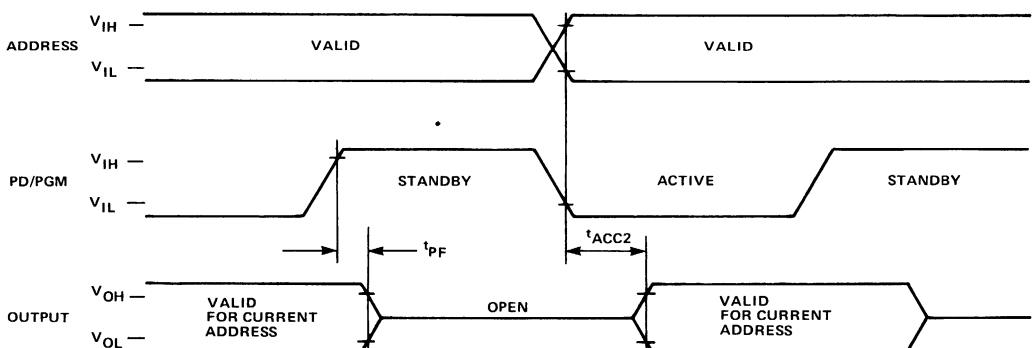
PROGRAM OPERATION
D.C. ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS[1,2]

$(T_A = 25°C \pm 5°C)$ $(V_{CC} = 5V \pm 5\%, V_{PP} = 25V \pm 1V)$

	PARAMETER	MIN	MAX	UNITS	NOTES
I_{IL}	Input Leakage Current		10	μA	3
V_{IL}	Input Low Level	-0.1	0.8	Volts	
V_{IH}	Input High Level	2.2	V_{CC} +1	Volts	
I_{CC}	V_{CC} Power Supply Current		100	mA	
I_{PP1}	V_{PP} Supply Current		5	mA	4
I_{PP2}	V_{PP} Supply Current During Programming Pulse		30	mA	5

A.C. CHARACTERISTICS AND OPERATING CONDITIONS[1, 2, 6, 7]

$(T_A = 25°C \pm 5°C)$ $(V_{CC} = 5V \pm 5\%, V_{PP} = 25V \pm 1V)$

	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
t_{AS}	Address Setup Time	2			μs	
t_{CSS}	$\overline{CS}$ Setup Time	2			μs	
t_{DS}	Data Setup Time	2			μs	
t_{AH}	Address Hold Time	2			μs	
t_{CSH}	$\overline{CS}$ Hold Time	2			μs	
t_{DH}	Data Hold Time	2			μs	
t_{DF}	Chip Deselect to Output Float Delay	0		120	ns	4
t_{CO}	Chip Select to Output Delay			120	ns	4
t_{PW}	Program Pulse Width	45	50	55	ms	
t_{PRT}	Program Pulse Rise Time	5			ns	
t_{PFT}	Program Pulse Fall Time	5			ns	

NOTES:
1. V_{CC} must be applied at the same time or before V_{PP} and removed after or at the same time as V_{PP}. To prevent damage to the device it must not be inserted into a board with V_{PP} at 25V.
2. Care must be taken to prevent overshoot of the V_{PP} supply when switching to +25V.
3. $0.45V \leqslant VIN \leqslant 5.25V$
4. PD/PGM = V_{IL}
5. PD/PGM = V_{IH}
6. t_T = 20nsec
7. 1V or 2V for inputs and .8V or 2V for outputs are used as timing reference levels.
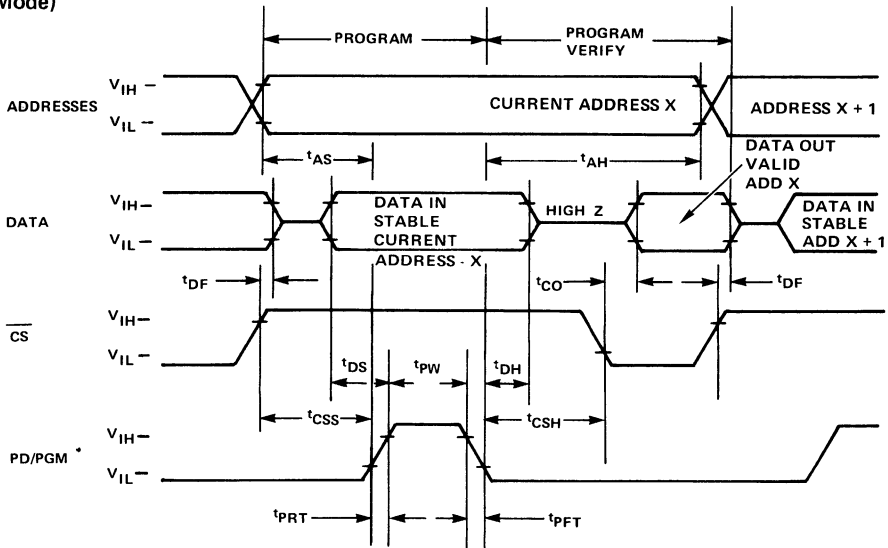
ation which lowers the device power from 525 mW maximum active power to 132 mW maximum for an overall savings of 75%. Programming can be done with a single TTL level pulse and may be done on any individual location either sequencially or at random. The three-state output controlled by the $\overline{CS}$ input allows OR-tie capability for construction of large arrays. A single power supply requirement of +5 volts makes the MK2716 ideally suited for use with MOSTEK's new 5 volt only microprocessors such as the MK3880 (Z-80). The MK2716 is packaged in the industry standard 24 pin dual-in line package with a transparent hermetically sealed lid. This allows the user to expose the chip to ultraviolet light to erase the data pattern. A new pattern may then be written into the device by following the program procedures outlined in this data sheet.

The MK2716 is specifically designed to fit those applications where fast turnaround time and pattern experimentation are required. Since data may be altered in the device (erase and reprogram) it allows for early debugging of the system program. Since single location programming is available, the MK2716 can have its data content increased (assuming all 2048 bytes were not programmed) at any time for easy updating of system capabilities in the field. Once the data/program is fixed and the intention is to produce large numbers of systems, MOSTEK also supplies a pin compatible mask programmable ROM, the MK34000. To transfer the program data to ROM, the user need only send the PROM along with device information to MOSTEK, from which the ROM with the desired pattern can be generated. This means a

reduction in the possibility of error when converting data to other forms (cards, tape, etc.) for this purpose. However, data may still be input by any of these traditional means such as paper tape, card deck, etc.

READ OPERATION

The MK2716 has six basic modes of operation. Under normal operating conditions (non-programming) there are three modes including READ, DESELECT and POWER DOWN. A READ operation is accomplished by maintaining pin 18 (PD/PGM) at V_{IL} and pin 21 (V_{PP}) at +5 volts. If $\overline{CS}$ (pin 20) is held active low after addresses (A_0 - A_{10}) have stabilized then valid output data will appear on the output pins at access time t_{ACC1} (address access). In this mode, access time may be referenced to $\overline{CS}$ (t_{CO}) depending on when $\overline{CS}$ occurs (see timing diagrams).

The DESELECT mode can be utilized when OR-tying the outputs of two or more 2716's. The output will go to a high impedance state when $\overline{CS}$ goes inactive (V_{IH}). In this case PD/PGM is a "don't care".

POWER DOWN operation is accomplished by taking pin 18 (PD/PGM) to a TTL high level (V_{IH}). The power is reduced by 75%, from 525mW maximum to 132mW. In power down V_{PP} must be at +5 volts and the outputs will be open-circuit regardless of the condition of $\overline{CS}$. Access time from a high to low transition of PD/PGM (t_{ACC2}) is the same as from addresses (t_{ACC1}). (See Power Down Timing Diagram).

PROGRAMMING INSTRUCTIONS

The MK2716 as shipped from MOSTEK will be completely erased. In this initial state and after any subsequent erasure, all bits will be at a '1' level (output high). Information is introduced by selectively programming 'O's into the proper bit locations. Once a '0' has been programmed into the chip it may be changed only by erasing the entire chip with UV light.

Word address selection is done by the same decode circuitry used in the READ mode. The MK2716 is put into the PROGRAM mode by maintaining V_{PP} at +25V, and $\overline{CS}$ at V_{IH}. In this mode the output pins serve as inputs (8 bits in parallel) for the required program data. Logic levels for other inputs and the V_{CC} supply voltage are the same as in the READ mode.

To program a "byte" (8 bits) of data, a TTL active high level pulse is applied to the PD/PGM pin once addresses and data have stabilized on the inputs. Each location must have a pulse applied with only one pulse per location required. Any individual location, a sequence of locations or locations at random may be programmed in this manor. The program pulse has a minimum width of 45msec and a maximum of 55msec, and must not be programmed with a high level D.C. signal applied to the PD/PGM pin.

PROGRAM INHIBIT is another useful mode of operation when programming multiple parallel addressed MK2716's with different data. It is necessary only to maintain $\overline{CS}$ at V_{IH}, V_{PP} at +25, allow addresses and data to stabilize and pulse the PD/PGM

pin of the device to be programmed. Data may then be changed and the next device pulsed. The devices with PD/PGM at V_{IL} will not be programmed.

PROGRAM VERIFY allows the MK2716 program data to be verified without having to reduce V_{PP} from +25V to +5V. V_{PP} should only be used in the PROGRAM/PROGRAM INHIBIT and PROGRAM VERIFY modes and must be at +5V in all other modes.

MK2716 ERASING PROCEDURE

The MK2716 may be erased by exposure to high intensity ultraviolet light, illuminating the chip thru the transparent window. This exposure to ultraviolet light induces the flow of a photo current from the floating gate thereby discharging the gate to its initial state. An ultraviolet source of 2537A° yielding a total integrated dosage of 15 Watt-seconds/cm^2 is required. Note that all bits of the MK2716 will be erased. The erasure time is approximately 15 to 20 minutes utilizing an ultra-violet lamp with a 12000μW/cm^2 power rating. The lamp should be used without short wave filters, and the MK2716 to be erased should be placed about one inch away from the lamp tubes. It should be noted that as the distance between the lamp and the chip is doubled, the exposure time required goes up by a factor of 4. The UV content of sunlight is insufficient to provide a practical means of erasing the MK2716. However, it is not recommended that the MK2716 be operated or stored in direct sunlight, as the UV content of sunlight may cause erasure of some bits in a short period of time.

PACKAGE DESCRIPTION
24-Pin Side-Braze Ceramic with Transparent Lid
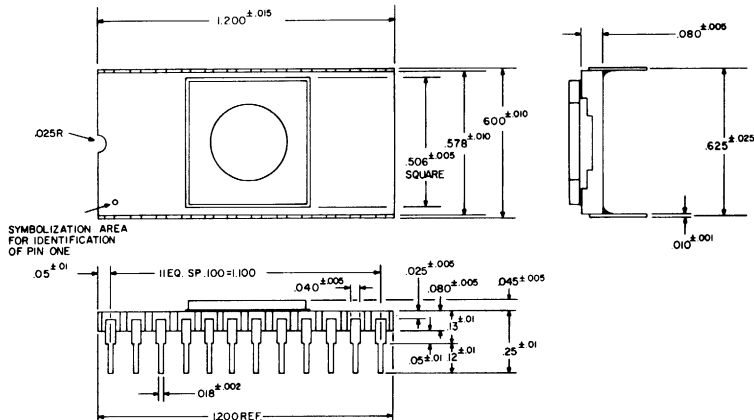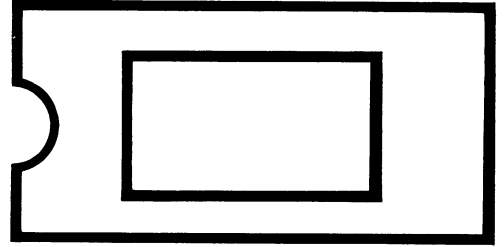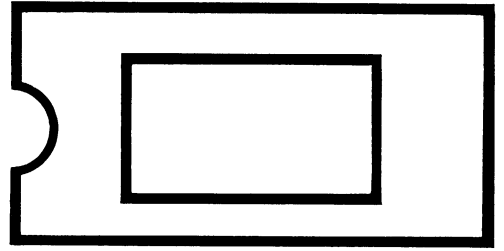
RANDOM ACCESS MEMORY
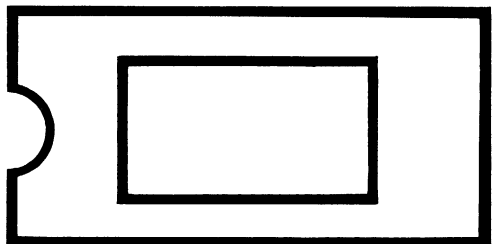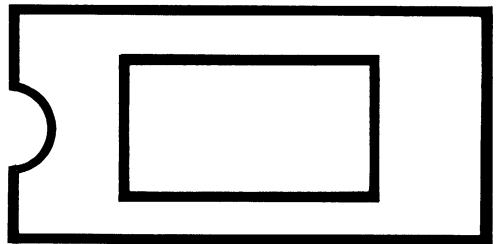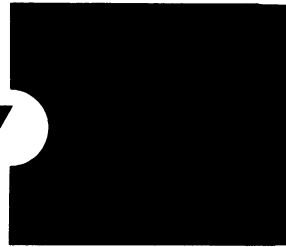
MOSTEK®

1024x1-BIT DYNAMIC RAM
MK4006(P)-6/MK4008(P)-6

FEATURES

☐ TTL/DTL Compatible inputs

☐ No Clocks Required

☐ Access time:
MK 4006 P-6 under 400 ns
MK 4008 P-6 under 500 ns

☐ Standby Power: under 50 mW

☐ 16-Pin Standard CDIP

☐ Supply Voltage: +5V and −12V

DESCRIPTION

This is a family of MOS dynamic 1024x1 random-access memories having identical functional characteristics, differing only in speed. Access time in the MK 4006 P-6 is less than 400 ns; in the MK 4008 P-6 less than 500.

Full address decoding is provided internally. Information is read out non-destructively (NDRO) and has the same polarity as the input data.

TTL/DTL compatibility at all inputs allows economical use in small systems by eliminating the need for special interface circuitry. Large main-memory applications also benefit from the low drive-voltage swings as well as the packing density afforded by the standard 16-pin dual-in-line packaging and low standby power.

The internal memory element of this RAM is a capacitance, and refreshing must be periodically initiated (see TIMING). However, all internal decoding and sensing is static, so that precharging or clocking normally associated with dynamic memories is not required. From the user's viewpoint, memory control and addressing are essentially those of a static device.

Noise suppression measures normally employed in DTL or TTL systems are sufficient. High voltage input swings and high peak-current line drivers are unnecessary for driving memory inputs and the memory itself does not exhibit large supply current transients.
Data output is single-ended to minimize propagation delay. Output current is sourced from V_{SS} (+5V), and easily sensed using readily available components. A logic 1 at the output terminal appears as a 5,000 Ohm resistor (MK 4006) to +5V; a logic 0 as an open circuit.

The performance of this RAM is made possible by Mostek's ion-implantation process. In addition to offering low threshold voltages for TTL/DTL compatibility and utilizing conventional P-channel processing, ion-implantation allows both enhancement (normally OFF) and depletion (normally ON) MOS transistors to be fabricated on the same chip. By replacing conventional MOS load resistors with constant-current depletion transistors, operational speeds and functional density are increased.

FUNCTIONAL DIAGRAM
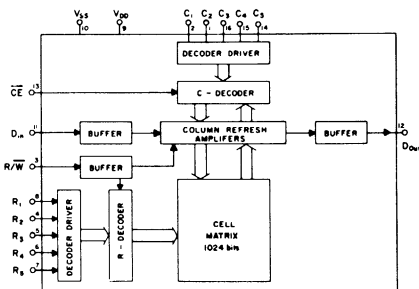
PIN CONNECTIONS
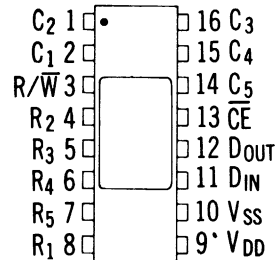
ABSOLUTE MAXIMUM RATINGS

Voltage on any pin relative to V_{SS} .... +0.3 to −20V

Operating Temperature .... 0°C to +70°C

Storage Temperature Range .... −65°C to +150°C

RECOMMENDED DC OPERATING CONDITIONS
($0°C \leq T_A \leq 70°C$)

	PARAMETER	MK 4006P-6 MIN | MAX	MK 4008P-6 MIN | MAX	UNITS	NOTES
V_{SS}	Supply Voltage	+4.75	+5.25	V	
V_{DD}	Supply Voltage	−11.4	−12.6	V	
V_{IL}	Input Voltage, Logic 0		+0.8	V	
V_{IH}	Input Voltage, Logic 1	$V_{SS}-1$	V_{SS}	V	
V_{SB}	Standby Supply Voltage (Fig. 4)	$V_{SS}-4$	$V_{SS}-6$	V	Note 1

RECOMMENDED AC OPERATING CONDITIONS[2]
($0°C \leq T_A \leq 70°C$)

	PARAMETER	MK 4006P-6 MIN | MAX	MK 4008P-6 MIN | MAX	UNITS	NOTES
t_{RC}	Read Cycle Time (Fig. 1)	400	500	ns	
t_{WC}	Write Cycle Time (Fig. 2)	650	900	ns ns	$t_{WP}=250$ ns $t_{WP}=400$ ns
t_{WP}	Write Pulse Width (Fig. 2)	250	400	ns ns	$t_{AW}=400$ ns $t_{AW}=500$ ns
t_{AW}	Address-to-Write Delay (Fig. 2)	400	500	ns ns	$t_{WP}=250$ ns $t_{WP}=400$ ns
t_{DLD}	Data-to-Write Lead Time (Fig. 2)	300	400	ns ns	$t_{WP}=250$ ns $t_{WP}=400$ ns
t_{RDLY}	Refresh Time (Fig. 3)	2	2	ms	See Note 3.
t_{CDPD}	Chip-Disable-to-Power-Down Delay (Fig. 4)	200	200	ns	See Note 1 See Note 4

DC ELECTRICAL CHARACTERISTICS
($V_{SS} = +5V \pm 5\%$; $V_{DD} = -12V \pm 5\%$; $0°C \leq T_A \leq 70°C$ unless otherwise noted)

	PARAMETER	MK 4006P-6 MIN | MAX	MK 4008P-6 MIN | MAX	UNITS	NOTES
I_{SS}, I_{DD}	Supply Current: At $T_A=0°C$	32	32	mA	Output
	At $T_A=70°C$	27	27	mA	Open
P_{SDBY}	Power Dissipation, Standby	50	50	mW	$V_{SS}-V_{DD} = 5V$; Note 1
I_{IH}	Input Current, Logic 1. Any Input	−5 +5	−5 +5	μA	$V_I = V_{SS}-1V$
I_{IL}	Input Current, Logic 0, Any Input	−5 +5	−5 +5	μA	$V_I = 0.8V$
I_{OH}	Output Current, Logic 1	1.0	0.8	mA	Note 5
I_{OL}	Output Current, Logic 0	5	5	μA	

AC ELECTRICAL CHARACTERISTICS

($V_{SS} = +5V \pm 5\%$; $V_{DD} = -12V \pm 5\%$; $0 C \leq T_A \leq 70 C$ unless otherwise noted)

	PARAMETER	MK 4006P-6 MIN	MAX	MK 4008P-6 MIN	MAX	UNITS	NOTES
t_{ACCESS}	Read Access Time (Fig. 1 & 1-A)		400		500	ns	Note 2
t_{CE}	Chip Enable Time (Fig. 1A & 5)		350		450	ns	Note 2
t_{CD}	Chip Disable Time (Fig. 1A & 5)		350		450	ns	
C_i	Input Capacitance, Any Input		5.0		5.0	pF	$T_A = 25°C$; $V_i = V_{SS}$; $f = 1MHz$
C_O	Output Capacitance		10		10	pF	$T_A = 25°C$; $V_O = V_{SS} - 5V$; $f = 1MHz$
C_{DD}	V_{DD} Capacitance		75		75	pF	$T_A = 25°C$; Note 6

NOTES:

(1) Applies to MK 4006-6 and MK 4008-6 only.

(2) Measurement Criteria: Input voltage swing, all inputs 0.8V to $V_{SS} - 1$
Input rise and fall times: 20 ns
Measurement point on input signals +1.5V above ground
Measurement point on output signal +60 mV above ground, using a load circuit of a 200 ohm resistor in parallel with a 100 pF capacitance connected to ground.

(3) t_{RDLY} is the time between refresh cycles for a given row address.

(4) The rise time of V_{HH} must not be faster than 20 ns

(5) Steady-state values. (Refer to Fig. 1A for clarification)

(6) Average capacitance of the V_{DD} terminal relative to the V_{SS} terminal. Measured by switching the V_{DD} terminal from 0V to −12V with an applied $V_{SS} = 5V$. Peak I_{DD} is observed and the circuit replaced by a capacitance which yields the same peak current as the circuit under test.

TIMING (Note 2)

FIG. 1 READ CYCLE
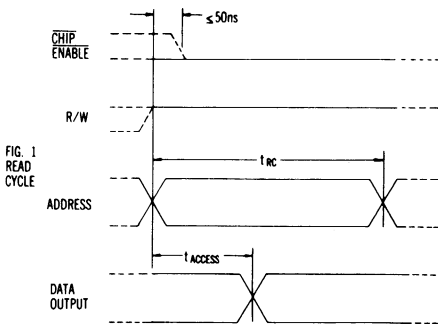
READING (Fig. 1)

Reading is accomplished with the Read/Write input held high. Data output directly follows the application of an address. As long as the address is unchanged and the chip enabled, data output will remain valid until the next refresh cycle. Input addresses can be changed as soon as output data is accessed. Any address can be applied repetitively without degrading stored data, providing that the refresh period of 2 ms is observed.

$t_1 = 20$ nanosec (Max)
$t_2 = 200$ nanosec (Max), 100 nanosec (Typ)
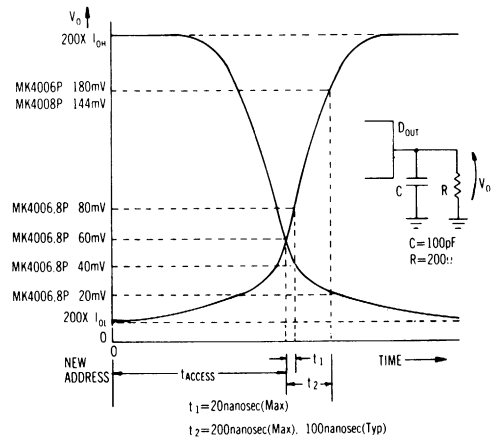
ACCESS TIME (Fig. 1-A)

Figure 1-A illustrates the measurement of access time after application of new address for the MK 4006 P and the MK 4008 P.

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TIMING
(Note 2)

WRITING (Fig. 2)

Writing is accomplished by bringing the Read/Write input low with valid data present at the data input and the Chip-Enable input low (chip enabled). Following the return of the Read/Write line to a high state, new address and input data can be applied. If a read-after-write operation is desired, valid data will appear at the output within one read access time following the rising edge of the Write Pulse. Read-modify-write operation is easily achieved by delaying the Write Pulse until data has been read and modification is complete.

REFRESHING (Figs. 2 & 3))

The dynamic memory cell employed in the MK 4006 P and MK 4008 P will not store data indefinitely. Stored data must be written back into the cell at least once every 2 ms. Rewriting is accomplished internally without the need to reapply external data. This rewriting operation is called *refreshing*.

Refreshing of the MK 4006 P and MK 4008 P is accomplished during both *write cycles* and *refresh cycles*. During a write cycle the state of the Row Address (R_1-R_5) determines which of the 32 memory matrix rows will be internally refreshed. An entire row (32 bits) is refreshed during one write cycle. Since it is difficult in practice to assure that each of the 32 possible R addresses is associated with a write cycle in every 2 ms period, a separate refresh cycle is normally employed.

The refresh cycle is identical to the write cycle except that the chip is disabled while the Read/Write line is pulsed. Disabling the chip removes the data output and prevents data at the data input from being written into the memory. An entire refresh cycle consists of 32 address changes and associated write pulses, involving a total time of approximately 20 microseconds.

STANDBY MODE (Fig. 4)

Power dissipation of the MK 4006-6 P and MK 4008-6 P can be reduced below 50 mW without loss of stored data by lowering the V_{DD} supply voltage to system ground (V_{SS}-5V). Figure 4 illustrates the proper input conditions that should be observed when reducing V_{DD}. If the standby mode is maintained as long as 2 milliseconds, the V_{DD} supply should be returned to −12V and a refresh cycle initiated. Read or write cycles can commence immediately following the return of V_{DD} to −12V.

Figure 2
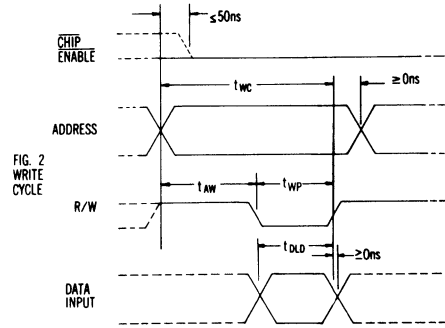
Figure 3
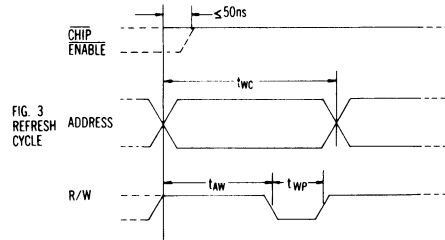
Figure 4
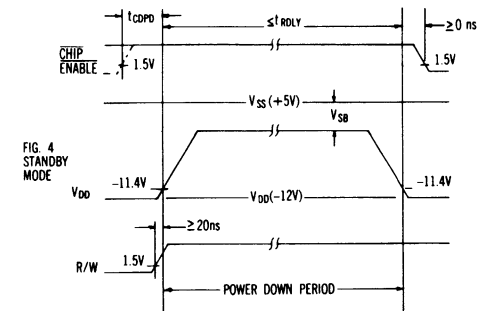
TIMING
(Note 2)

CHIP ENABLING (Fig. 5)

The negative-going $\overline{CE}$ enables the chip, and output data becomes valid within t_{CE} time. Return of the $\overline{CE}$ input to logic 1 disables the chip; data out remains for t_{CD} time.

Figure 5

FIG. 5 CHIP ENABLING
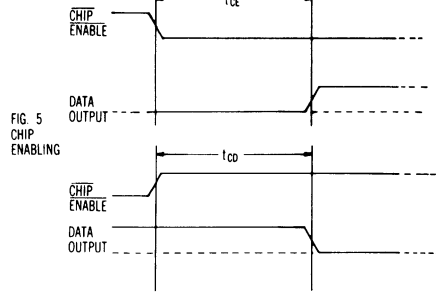
TESTING CONSIDERATIONS

The functional diagram (Fig. 6) indicates signal flow for selected row and column.

A simplified listing of functional tests is shown in Table 1. (high = Logic 1; low = Logic 0)

Tests are performed in an address sequence which requires the maximum number of changes in the row and column decoders between addresses. Addressing Rows 0 through 31 is accomplished by using the binary equivalent of the row address. The internal organization of the memory matrix requires the logic shown in Fig. 7 for column addresses; this logic provides the necessary conversion from binary equivalent to column address.
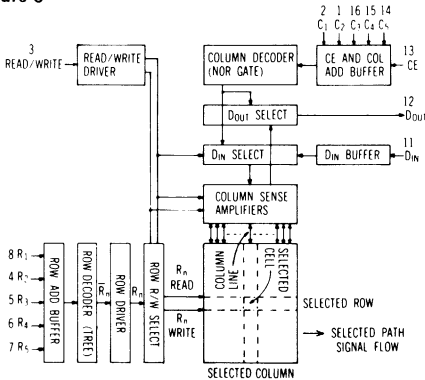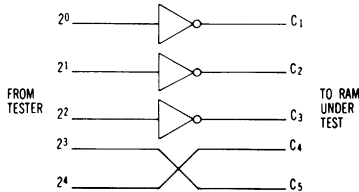
TABLE 1: FUNCTIONAL TESTS (SIMPLIFIED)

TEST DESC.	TEST SEQ.	OPER.	CHIP ENABLE	DATA INPUT	COMPARE DATA
Bit & Decoder Test¹	First	Write	E	Parity	
	Next	Read	E		Parity
Column Shorts & No Write During Disable	First	Write	E	V-Bar	
	Next	Write	D	$\overline{\text{V-Bar}}$	
	Next	Read	E		V-Bar
Row Shorts, No Read During Disable, & Max. Power	First	Write	E	H-Bar	
	Next	Read	D	1	0
	Next	Read	E	0	H-Bar
Access Time, Refresh, Write Cycle, & Standby¹	First	Write, Write	E	V-Bar, V-Bar	
	Next	Delay	D	0	
	Next	Read	E		$\overline{\text{V-Bar}}$
Disturb Test	First	Write Row of 1's	E	1	
	Next	Write Adj. Row with 0's	E	0	
	Next	Continue Writing Same Row for Max. Refresh Delay	E	0	
	Next	Read original Row of 1's	E		1

1. Test performed as shown and repeated with complementary data.

Figure 6

Figure 7

FROM TESTER — TO RAM UNDER TEST

ORDERING INFORMATION

MK 4006 P–6 1024x1 RAM/w/400 ns access time with power down
MK 4008 P–6 1024x1 RAM/w/500 ns access time with power down

APPLICATION

SENSE AMPLIFIERS FOR MK 4006/4008 RAM's

Since the interface circuitry used to convert memory signals to system logic levels strongly influences system access times, this circuitry should always be designed to meet the speed and cost requirements of the particular application.

Fig. 1-A (See "Timing") is shown to assist in the design of such amplifiers. This figure shows output voltage (across a specified load) vs. time from application of new address with several points indicated where specified voltage levels are referenced to specific times. Although all the various access times vs. output current levels cannot be shown, a few guidelines are given for interpolation between the specified points.

In Fig. 1-A, the two points at $t_{access} + 20$ nsec give the minimum "1" level and the maximum "0" level for this particular time (80 mV and 40 mV respectively). At $t_{access} + 200$ nsec, voltage levels are specified for the 90% and 10% points of the minimum "1" and maximum "0" levels.

INTERPOLATION

These interpolation guidelines are selected to give the designer a high level of confidence in his sense amplifier design.
From O to 1: This portion of the access curve can be estimated by two linear portions: (1) from the 60 mV to the 80 mV level; and (2) from the 80 mV level to 180/144 mV level.
From 1 to O: This portion of the access curve can be estimated by a semi-logarithmic plot decreasing 20 mV for each decade or 10 nsec of time added to t_{access}, with the end points being 60 mV at 2 nsec and 20 mV at 200 nsec.

EXAMPLE: Let us consider how this data can be used in a sense amplifier design utilizing the 75107/108 Dual-Line-Receiver-and-Driver.

The manufacturer's data sheet for this circuit shows us that at strobe time, three conditions of the line receiver can exist: (1) the input voltage differential can be more positive than 25 mV, resulting in a logic 1 at the output (Input differential voltage is referenced to the inverting terminal); (2) the input differential can be more negative than 25 mV, resulting in a logic O at the output; (3) the input differential is less than 25 mV (absolute value), which will result in an output of an undetermined state. In other words, the line receiver has a 50 mV "window" centered around zero, and a signal must fall outside this window to provide reliable information at the output.

The standard configuration for using the 75107/108 as a sense amp is shown in Fig. 8 with the voltage and current conventions used in this analysis.

FIG. 8: Illustrating use of 75107/108 Line Receivers as sense amplifiers for the MK 4006/4008 P.
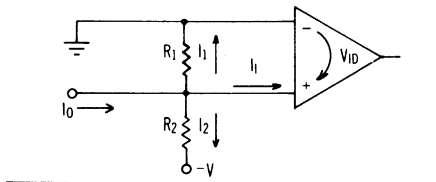
From the worst-case access at the *chip* level, one can use the interpolation technique described above to determine maximum "O" current level $[I_{OLC}(MAX)]$ and the minimum "1" current level $[I_{OH}(MIN)]$.

However, to use a worst-case approach to this design, in addition to the chip's characteristics, one must include in the "O" level current the effect of leakage from all outputs that are wired together. Also the input currents required by the 75107/108 (75 mA and 10 mA) must be included. Let us call this $I_{OLT}(MAX)$:

$$I_{OLT}(MAX) = I_{OLC}(MAX) + (N-1) (5\ \mu A) \quad [1]$$
where N = number of outputs wired together

Using the maximum zero level at the line receiver input ($V_{ID} \leq -25mV = V_{ID}^-$), the following equation is derived:

$$I_{OLT}(MAX) = I_1 - I_2 + I_{IL}(MIN)$$
and $I_{IL}(MIN) = O\ \mu A \quad [2]$

therefore:

$$I_{OLT}(MAX) = \frac{V_{ID}^-}{R1} + \frac{V + V_{ID}^-}{R2} \quad [3]$$

Using the minimum "1" level at the line receiver input ($V_{ID} \geq +25$ mV $= V_{ID}^+$), the equation becomes

$$I_{OH}(MIN) = I_1 - I_2 + I_{IH}(MAX) \quad [4]$$
and $I_{IH}(MAX) = 75\ \mu A$

$$I_{OH}(MIN) = \frac{V_{ID}^+}{R1} + \frac{V + V_{ID}^+}{R2} + 75\ \mu A \quad [5]$$

Solving these equations ([3] and [5]) simultaneously yields R1 and R2.
As an example, assume a memory system with 4 outputs wired-ORed to a sense amplifier, requiring a chip access time of 460 nsec. Then the associated current and resistor values are:

$$I_{OLT}(MAX) = 152.3\ \mu A + 3\ (5\ \mu A) = 167.3\ \mu A$$
$$I_{OH}(MIN) = 511.12\ \mu A$$

Therefore:

R1 = 190 Ω
R2 = 16.5 KΩ

Sense amplifiers vary from the very fast, low-threshold types to the slower, high-threshold kind. The ideal choice will depend on the application. Fig. 1-A and the guidelines in this note are intended to help the designer tailor his sense amplifier design to meet the speed and cost requirements of his particular application.

It should also be noted that a portion of the output current from the memory chip is used to charge the capacitance on the data output. If the output impedance differs greatly from the specified load, this current must also be calculated.

MOSTEK.

256x1-BIT DYNAMIC RAM

MK4007(P/N)

FEATURES

☐ Versatile RAM can replace any existing 1101-type 256x1 MOS RAM pin for pin.

☐ Ion-implanted for superior performance.

☐ **Lower power dissipation:** TOTAL 370 mW max over entire temperature range.

☐ **Faster access time:** Typically 525 ns with V_D and V_{DD} at −9V.

☐ **Less temperature-sensitive:** specified over entire AMBIENT temperature range 0° to 75°C.

☐ **Tight control of output sink current capabilities:** made possible by use of depletion-mode transistors.

☐ **No restrictions** on address input sequence, skew, or rise and fall times.

DESCRIPTION

Ion-implantation processes used in manufacturing the Mostek MK 4007 P Random Access MOS Memory result in a low-cost device with performance exceeding other industry types over the entire temperature and voltage supply ranges. It may be used to replace any existing 1101 type RAM pin for pin.

The depletion-load ion-implantation technique allows the fabrication of both depletion and enhancement mode transistors on the same chip. The result is not only superior operating characteristics within the region usually specified for devices of this type, but also wider operational areas without severe performance degradation. For example, while specifications for this device are given for V_D and V_{DD} from −7 to −13.2V, V_D and V_{DD} may actually range from −6.5 to −15V (see DC Operating Conditions and Figure 1). Access times are improved (See Figure 2); power dissipation is reduced (see

☐ Full DTL/TTL compatibility.

☐ Wide power supply range: +5V; −6.5 to −15V.

APPLICATIONS

Ideal for small buffer storage requiring low cost, superior performance, and bipolar compatibility, such as:

☐ Scratchpad memories

☐ Data link buffers

☐ Key-to-tape buffers

☐ Tape-to-printer buffers

☐ Editing memories

Figure 3) and output sink current capabilities are improved (see Figure 4). The device is less temperature-dependent (see Figures 5 and 6) and is specified over the entire ambient temperature range of 0° to 75°C.

The ion-implantation process also makes the MK 4007 P RAM fully TTL/DTL compatible at all inputs and outputs.

The 4007 P is a static memory, requiring no clocks or refreshing. Data is written into the address location by applying a logic "1" to the R/W input. Addressing the desired location, with the chip enabled and R/W at logic "0", provides a nondestructive read-out (NDRO) of true and complement data. A "Chip Select" allows output buffers to be open-circuited during disable time for wire ORing. All inputs are protected against static charge accumulation.

FUNCTIONAL DIAGRAM
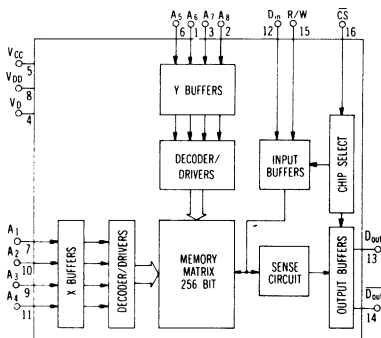
PIN CONNECTIONS
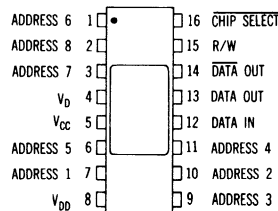
256 X 1-BIT DYN RAM
MK4007(P/N)

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ABSOLUTE MAXIMUM RATINGS

Voltage on Any Terminal Relative to V_{CC} .... + 0.3V to −25V
Operating Temperature Range (Ambient) .... 0°C to +75°C
Storage Temperature Range (Ambient) Ceramic .... −65°C to +150°C
Storage Temperature Range (Ambient) Plastic .... −55°C to 125°C

DC OPERATING CONDITIONS

(Ambient Temperature Range: 0°C to +75°C)

		PARAMETER	MIN	TYP	MAX	UNITS	COMMENTS
POWER	V_{CC}	Supply Voltage	4.75	5.0	5.25	V	
	V_{DD}	Supply Voltage	−6.5	−9.0	−15.0	V	See Fig. 1 for
	V_D	Supply Voltage	−6.5	−9.0	−15.0	V	V_D, V_{DD} differential
INPUTS	V_{IL}	Logic "0" Voltage, any input		0	+0.8	V	
	V_{IH}	Logic "1" Voltage, any input	V_{CC} −2.0	V_{CC}	V_{CC}+0.3	V	

ELECTRICAL CHARACTERISTICS

(Ambient Temperature Range: 0°C to +75°C. $V_{CC} = +5$ V ±5%;
$V_D = V_{DD} = -7$ V to −13.2 V, unless otherwise specified.)

		PARAMETER	MIN	TYP(1)	MAX	UNITS	CONDITIONS
POWER	I_D	Supply Current. V_D		8.0	16	mA	$V_D = V_{DD} = -9V \pm 5\%$
	I_{DD}	Supply Current, V_{DD}		4.0	9	mA	Outputs open-circuited.
	P_D	Power Dissipation, Total		170	370	mW	
	I_D	Supply Current. V_D			19	mA	$V_D = V_{DD} = -13.2$ V
	I_{DD}	Supply Current, V_{DD}			10	mA	$V_{CC} = +5.25$ V
	P_D	Power Dissipation, Total			535	mW	Outputs open-circuited.
	P_{SDBY}	Power Dissipation, Standby		30	75	mW	$V_D = V_{CC}$; $V_{DD} = -9V \pm 5\%$
INPUTS	$I_{I(L)}$	Input Leakage Current			1.0	μA	$V_{IN} = 0$ V, $T_A = 25°C$
	C_{IN}	Input Capacitance, Any Logic Input		7	10	pF	$T_A = 25°C$, F. meas. =
	$C_{V(D)}$	Capacitance, V_D Power Supply		35		pF	1 MHz; Tested input = V_{CC}
OUTPUTS	I_{OL}	Output Current, Logic "0"	3.2	5.6		mA	$V_O = +0.40$ V
	I_{OH}	Output Current, Logic "1"	−1.0	−4.2		mA	$V_O = +2.6$ V
	I_{OLC}	Output Clamp Current, Logic "0"			8.0	mA	$V_O = -1.0$ V
	$I_{O(L)}$	Output Leakage Current			1.0	μA	$V_O = V_{CC} -5V$; $\overline{CS} = $ Logic 1; $T_A = 25°C$.
	C_{OUT}	Output Capacitance		7	10	pF	$T_A = 25°C$; F meas. = 1 MHz; $V_O = V_{CC}$

NOTES:

(1) Typical values at $V_{CC} = +5$ V, $V_D = V_{DD} = -9.0$ V*, $T_A = 25°C$.

   (*Except Standby Power)

TIMING

(Ambient Temperature Range: 0°C to 75°C; $V_{CC} = +5$ V $\pm 5\%$; $V_D = V_{DD} = -7V$ to -13.2 V, unless otherwise specified. See Notes 1 and 2.)

		PARAMETER	MIN	TYP	MAX	UNITS	
OPERATING CONDITIONS	t_{wc}	Write Cycle Time	700			ns	
	t_{wd}	Write Set-up Delay	300			ns	
	t_{wp}	Write Pulse Width	400			ns	
	t_{dld}	Data Lead Time	300			ns	
	t_{dlg}	Data Lag Time	0			ns	
	t_{cw}	Chip Select Pulse Width	400			ns	
DYNAMIC CHAR.	t_{ACC}	Access Time		525	900	ns	$V_D = V_{DD} = -9V \pm 5\%$.
	t_{RC}	Read Cycle Time			800	ns	(See Note 3.)
	t_{ACC}	Access Time			1.0	μs	$V_D = V_{DD} = -7V$ to $-13.2V$.
	t_{RC}	Read Cycle Time			900	ns	(See Note 3.)
	t_{OH}	Data Output Hold Time	100			ns	
	t_{CSE}	Chip-Select-to-Output Enable			300	ns	
	t_{CSD}	Chip-Select-to-Output Disable			300	ns	

NOTES:

(1) All measurements to the 1.5 V level; inputs for test are 0 to 5 V and ≤ 10 ns rise and fall times; output is loaded with 1 TTL and approx. 20 pF.

(2) R/W should be brought to logical "0" whenever address bits are changed; however, there are no restrictions on rise and fall times of address bits, nor on the sequence (or skew) of address bit changes.

(3) Read Cycle may be "pipe-lined," i.e., the minimum hold time (t_{OH}) may be subtracted from the maximum access time (t_{ACC}).

TIMING
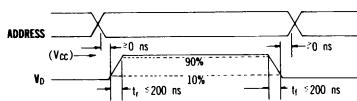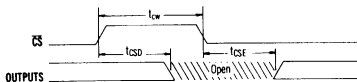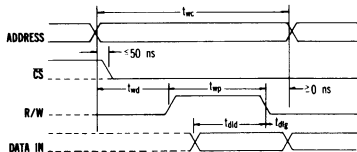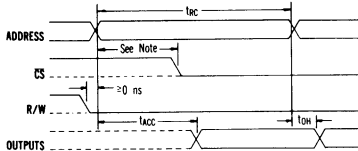
READ CYCLE

Reading is accomplished with R/W (Read/Write) and $\overline{CS}$ (Chip Select) at logical "0."

NOTE: $\overline{CS}$ logical "1" overlap time shown must be 300 ns (max t_{CSE}) less than the desired access time; e.g., if desired access time $t_{ACC} = 1.2$ μs, then $\overline{CS}$ should go to logical "0" no later than 900 ns following address change.

WRITE CYCLE

Writing is accomplished with R/W at logical "1" and $\overline{CS}$ at logical "0." $\overline{CS}$ at logical "1" may overlap the address change as much as 50 ns. R/W may be taken to logical "0" coincidentally with an address change, but should not overlap an address change while in the logical "1" state.

CHIP SELECT

Chip Select at logical "1" causes the normal push-pull output buffers to be open-circuited for purposes of wire-ORing. The Chip Select may be used to access the memory at a faster rate by maintaining a constant address and selecting individual chips with the $\overline{CS}$ Select input.

POWER SWITCHING

During standby operation the MK 4007 P will dissipate only 30 mW of power (typically) if the peripheral power supply, V_D, is reduced to V_{CC}. The R/W input may be maintained at logical "0" or "1"; however, if R/W is at logical "1," Chip Select should also be logical "1" (to disable chip during standby operation). With the return of power, either read or write cycles may commence as described above.

**TYPICAL
PERFORMANCE
CURVES**

FIG. 1: POWER SUPPLY OPERATING REGION & DIFFERENTIAL

FIG. 2: ACCESS TIME VS SUPPLY VOLTAGE, (V$_D$)

FIG. 3: TOTAL POWER DISSIPATION, (P$_D$), VS SUPPLY VOLTAGE, (V$_D$ and V$_{DD}$)

FIG. 4: OUTPUT CURRENT VS OUTPUT VOLTAGE

FIG. 5: OUTPUT CURRENT VS AMBIENT TEMPERATURE

FIG. 6: WORST-CASE ACCESS TIME VS SUPPLY VOLTAGE
(At Various Capacitances and Ambient Temperatures)

FIG. 7: SUPPLY CURRENT, (I$_D$ and I$_{DD}$), VS SUPPLY VOLTAGE (V$_D$ and V$_{DD}$)

FIG. 8: MK 4007 P MEMORY CELL

D = Depletion-mode Load

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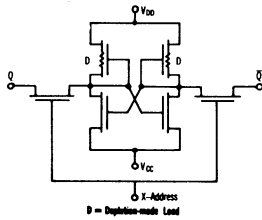
MOSTEK®

256x1-BIT DYNAMIC RAM

MK4007(P/N)-4

FEATURES

☐ Low-cost 256x1 RAM in 16-pin package.

☐ Identical with Mostek's MK 4007 P in all specifications except output current

DESCRIPTION

This economical version of Mostek's 256x1 bit RAM is identical with the MK 4007 P in all electrical characteristics except output current. Performance, operating conditions, timing characteristics, package, and all other specifications are identical with the MK 4007 P. See the MK 4007 P Data Sheet for additional information.

FUNCTIONAL DIAGRAM

ELECTRICAL CHARACTERISTICS

(Ambient Temperature Range: 0°C to +75°C. $V_{CC} = +5$ V $\pm 5\%$; $V_D = V_{DD} = -7$ V to -13.2 V, unless otherwise specified.)

<table>
<tr><th colspan="2"></th><th>PARAMETER</th><th>MIN</th><th>TYP</th><th>MAX</th><th>UNITS</th><th>CONDITIONS</th></tr>
<tr><td rowspan="8">POWER</td><td>I_D</td><td>Supply Current, V_D</td><td></td><td></td><td>8.0</td><td>16</td><td>mA</td><td>$V_D = V_{DD} = -9$ V $\pm 5\%$</td></tr>
<tr><td>I_{DD}</td><td>Supply Current, V_{DD}</td><td></td><td></td><td>4.0</td><td>9</td><td>mA</td><td>Outputs open-circuited.</td></tr>
<tr><td>P_D</td><td>Power Dissipation, Total</td><td></td><td></td><td>170</td><td>370</td><td>mW</td><td></td></tr>
<tr><td>I_D</td><td>Supply Current, V_D</td><td></td><td></td><td></td><td>19</td><td>mA</td><td>$V_D = V_{DD} = -13.2$ V</td></tr>
<tr><td>I_{DD}</td><td>Supply Current, V_{DD}</td><td></td><td></td><td></td><td>10</td><td>mA</td><td>$V_{CC} = +5.25$ V</td></tr>
<tr><td>P_D</td><td>Power Dissipation, Total</td><td></td><td></td><td></td><td>535</td><td>mW</td><td>Outputs open-circuited.</td></tr>
<tr><td>P_{SDBY}</td><td>Power Dissipation, Standby</td><td></td><td></td><td>30</td><td>75</td><td>mW</td><td>$V_D = V_{CC}$; $V_{DD} = -9$V $\pm 5\%$</td></tr>
<tr><td colspan="8"></td></tr>
<tr><td rowspan="2">INPUTS</td><td>$I_{I(L)}$</td><td>Input Leakage Current</td><td></td><td></td><td></td><td>1.0</td><td>μA</td><td>$V_{IN} = 0$ V, $T_A = 25°$C</td></tr>
<tr><td>C_{IN}
$C_{V(D)}$</td><td>Input Capacitance, Any Logic Input
Capacitance, V_D Power Supply</td><td></td><td></td><td>7
35</td><td>10</td><td>pF
pF</td><td>$T_A = 25°$C, F. Meas. =
1 MHz; Tested input = V_{CC}</td></tr>
<tr><td rowspan="4">OUTPUTS</td><td>I_{OL}

I_{OH}
I_{OLC}</td><td>Output Current, Logic "0": @ $T_A = 25°$C
Output Current, Logic "0": @ $T_A = 70°$C
Output Current, Logic "1"
Output Clamp Current, Logic "0"</td><td>3.0
2.0
-1.0</td><td>5.6

-4.2</td><td>

8.0</td><td>mA
mA
mA
mA</td><td>$V_O = +0.40$ V $\quad$ { $V_{CC} = 5.0$ V $\pm 5\%$
$V_O = +0.40$ V $\quad$ } $V_D = V_{DD} = -9.0$ V
$V_O = +2.6$ V $\quad$) $\pm 10\%$
$V_O = -1.0$ V $\quad$ (</td></tr>
<tr><td>$I_{O(L)}$</td><td>Output Leakage Current</td><td></td><td></td><td></td><td>1.0</td><td>μA</td><td>$V_O = V_{CC} -5$V; $\overline{CS} =$ Logic 1;
$T_A = 25°$C.</td></tr>
<tr><td>C_{OUT}</td><td>Output Capacitance</td><td></td><td></td><td>7</td><td>10</td><td>pF</td><td>$T_A = 25°$C; F meas. =
1 MHz; $V_O = V_{CC}$</td></tr>
</table>

NOTES:

(1) Typical values at $V_{CC} = +5$ V, $V_D = V_{DD} = -9.0$ V*, $T_A = 25°$C.
    (*Except Standby Power)

MOSTEK®

FEATURES

☐ Industry standard 16-pin DIP (MK 4096) configuration

☐ 120ns access time, 320ns cycle (MK4027-1)
150ns access time, 320ns cycle (MK4027-2)
200ns access time, 375ns cycle (MK4027-3)

☐ ±10% tolerance on all supplies (+12V, ±5V)

☐ ECL compatible on V_{BB} power supply (−5.7V)

☐ Low Power: 462mW active (max)
27mW standby (max)

☐ Improved performance with "gated $\overline{CAS}$", "$\overline{RAS}$ only" refresh and page mode capability

☐ All inputs are low capacitance and TTL compatible

☐ Input latches for addresses, chip select and data in

☐ Three-state TTL compatible output

☐ Output data latched and valid into next cycle

DESCRIPTION

The MK 4027 is a 4096 word by 1 bit MOS random access memory circuit fabricated with MOSTEK's N-channel silicon gate process. This process allows the MK 4027 to be a high performance state-of-the-art memory circuit that is manufacturable in high volume. The MK 4027 employs a single transistor storage cell utilizing a dynamic storage technique and dynamic control circuitry to achieve optimum performance with low power dissipation.

A unique multiplexing and latching technique for the address inputs permits the MK 4027 to be packaged in a standard 16-pin DIP on 0.3 in. centers. This package size provides high system-bit densities and is compatible with widely available automated testing and insertion equipment.

System oriented features include direct interfacing capability with TTL, only 6 very low capacitance address lines to drive, on-chip address and data registers which eliminates the need for interface registers, input logic levels selected to optimize noise immunity, and two chip select methods to allow the user to determine the appropriate speed/power characteristics of his memory system. The MK 4027 also incorporates several flexible operating modes. In addition to the usual read and write cycles, read-modify write, page-mode, and $\overline{RAS}$-only refresh cycles are available with the MK 4027. Page-mode timing is very useful in systems requiring Direct Memory Access (DMA) operation.

4096 X 1-BIT DYN RAM
MK4027(P/J/N)-1/2/3

FUNCTIONAL DIAGRAM

PIN CONNECTIONS

PIN NAMES

A_0-A_5	ADDRESS INPUTS
$\overline{CAS}$	COLUMN ADDRESS STROBE
$\overline{CS}$	CHIP SELECT
D_{IN}	DATA IN
D_{OUT}	DATA OUT
$\overline{RAS}$	ROW ADDRESS STROBE
$\overline{WRITE}$	READ/WRITE INPUT
V_{BB}	POWER (−5V)
V_{CC}	POWER (+5V)
V_{DD}	POWER (+ 12V)
V_{SS}	GROUND

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to V_{BB} . . . . −0.5V to +20V
Voltage on V_{DD}, V_{CC} relative to V_{SS} . . . . −1.0V to +15V
$V_{BB}−V_{SS}$ ($V_{DD}−V_{SS} > 0$) 0V
Operating temperature, T_A (Ambient) . . . . 0°C to + 70°C
Storage temperature (Ambient)(Ceramic) . . . . −65°C to + 150°C
Storage temperature (Ambient)(Plastic) . . . . −55°C to + 125°C
Short circuit output current 50mA
Power dissipation . . . . 1 Watt

RECOMMENDED DC OPERATING CONDITIONS [4]
(0°C ≤ T_A ≤ 70°C) [1]

	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{DD}	Supply Voltage	10.8	12.0	13.2	volts	2
V_{CC}	Supply Voltage	4.5V	5.0	5.5	volts	2,3
V_{SS}	Supply Voltage	0	0	0	volts	2
V_{BB}	Supply Voltage	−4.5	−5.0	−5.7	volts	2
V_{IHC}	Logic 1 Voltage, $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	2.4		7.0	volts	2
V_{IH}	Logic 1 Voltage, all inputs except $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	2.2		7.0	volts	2
V_{IL}	Logic 0 Voltage, all inputs	−1.0		.8	volts	2

DC ELECTRICAL CHARACTERISTICS [4]
(0°C ≤ T_A ≤ 70°C)[1] (V_{DD} = 12.0V ± 10%; V_{CC} = 5.0V ± 10%; V_{SS} = 0V; −5.7V ≤ V_{BB} ≤ −4.5V)

	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
I_{DD1}	Average V_{DD} Power Supply Current			35	mA	5
I_{DD2}	Standby V_{DD} Power Supply Current			2	mA	8
I_{DD3}	Average V_{DD} Power Supply Current during "$\overline{RAS}$ only" cycles			25	mA	
I_{CC}	V_{CC} Power Supply Current				mA	6
I_{BB}	Average V_{BB} Power Supply Current			150	μA	
$I_{I(L)}$	Input Leakage Current (any input)			10	μA	7
$I_{O(L)}$	Output Leakage Current			10	μA	8,9
V_{OH}	Output Logic 1 Voltage @ I_{OUT} = −5mA	2.4			volts	
V_{OL}	Output Logic 0 Voltage @ I_{OUT} = 3.2mA			0.4	volts	

NOTES

1. T_A is specified for operation at frequencies to $t_{RC} \geqslant t_{RC}$ (min). Operation at higher cycle rates with reduced ambient temperatures and higher power dissipation is permissible provided that all AC parameters are met. See figure 2 for derating curve.

2. All voltages referenced to V_{SS}.

3. Output voltage will swing from V_{SS} to V_{CC} when enabled,with no output load. For purposes of maintaining data in standby mode, V_{CC} may be reduced to V_{SS} without affecting refresh operations or data retention. However, the V_{OH} (min) specification is not guaranteed in this mode.

4. Several cycles are required after power-up before proper device operation is achieved. Any 8 cycles which perform refresh are adequate for this purpose.

5. Current is proportional to cycle rate. I_{DD1} (max) is measured at the cycle rate specified by t_{RC} (min). See figure 1 for I_{DD1} limits at other cycle rates.

6. I_{CC} depends on output loading. During readout of high level data V_{CC} is connected through a low impedance (135Ω typ) to Data Out. At all other times I_{CC} consists of leakage currents only.

7. All device pins at 0 volts except V_{BB} which is at −5 volts and the pin under test which is at +10 volts.

8. Output is disabled (high-impedance) and $\overline{RAS}$ and $\overline{CAS}$ are both at a logic 1. Transient stabilization is required prior to measurement of this parameter.

9. 0V ≤ V_{OUT} ≤ + 10V.

10. Effective capacitance is calculated from the equation:

$$C = \frac{\Delta Q}{\Delta V} \text{ with } \Delta V = 3 \text{ volts.}$$

11. A.C. measurements assume t_T = 5ns.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS[4, 11, 17]

$(0^\circ C \leqslant T_A \leqslant 70^\circ C)^1$ ($V_{DD} = 12.0V \pm 10\%$, $V_{CC} = 5.0V \pm 10\%$, $V_{SS} = 0V$, $-5.7V \leqslant V_{BB} \leqslant -4.5V$)

	PARAMETER	MK4027-1 MIN	MK4027-1 MAX	MK4027-2 MIN	MK4027-2 MAX	MK4027-3 MIN	MK4027-3 MAX	UNITS	NOTES
t_{RC}	Random read or write cycle time	320		320		375		ns	12
t_{RWC}	Read write cycle time	320		320		375		ns	12
t_{RMW}	Read modify write cycle time	320		320		405		ns	12
t_{PC}	Page mode cycle time	160		170		225		ns	12
t_{RAC}	Access time from row address strobe		120		150		200	ns	13, 15
t_{CAC}	Access time from column address strobe		80		100		135	ns	14, 15
t_{OFF}	Output buffer turn-off delay		35		40		50	ns	
t_{RP}	Row address strobe precharge time	100		100		120		ns	
t_{RAS}	Row address strobe pulse width	120	10,000	150	10,000	200	10,000	ns	
t_{RSH}	Row address strobe hold time	80		100		135		ns	
t_{CAS}	Column address strobe pulse width	80		100		135		ns	
t_{CSH}	Column address strobe hold time	120		150		200		ns	
t_{RCD}	Row to column strobe delay	15	40	20	50	25	65	ns	16
t_{ASR}	Row address set-up time	0		0		0		ns	
t_{RAH}	Row address hold time	15		20		25		ns	
t_{ASC}	Column address set-up time	−5		−10		−10		ns	
t_{CAH}	Column address hold time	40		45		55		ns	
t_{AR}	Column address hold time referenced to $\overline{RAS}$	80		95		120		ns	
t_{CSC}	Chip select set-up time	0		−10		−10		ns	
t_{CH}	Chip select hold time	40		45		55		ns	
t_{CHR}	Chip select hold time referenced to $\overline{RAS}$	80		95		120		ns	
t_T	Transition time (rise and fall)	3	35	3	35	3	50	ns	17
t_{RCS}	Read command set-up time	0		0		0		ns	
t_{RCH}	Read command hold time	0		0		0		ns	
t_{WCH}	Write command hold time	40		45		55		ns	
t_{WCR}	Write command hold time referenced to $\overline{RAS}$	80		95		120		ns	
t_{WP}	Write command pulse width	40		45		55		ns	
t_{RWL}	Write command to row strobe lead time	50		50		70		ns	
t_{CWL}	Write command to column strobe lead time	50		50		70		ns	
t_{DS}	Data in set-up time	0		0		0		ns	18
t_{DH}	Data in hold time	40		45		55		ns	18
t_{DHR}	Data in hold time referenced to $\overline{RAS}$	80		95		120		ns	
t_{CRP}	Column to row strobe precharge time	0		0		0		ns	
t_{CP}	Column precharge time	60		60		80		ns	
t_{RFSH}	Refresh period		2		2		2	ms	
t_{WCS}	Write command set-up time	0		0		0		ns	19
t_{CWD}	$\overline{CAS}$ to $\overline{WRITE}$ delay	60		60		80		ns	19
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ delay	100		110		145		ns	19
t_{DOH}	Data out hold time	10		10		10		μs	

Notes Continued

12. The specifications for t_{RC} (min) and t_{RWC} (min) are used only to indicate cycle time at which proper operation over the full temperature range $(0^\circ C \leqslant T_A \leqslant 70^\circ C)$ is assured. See figure 2 for derating curve.

13. Assumes that $t_{RCD} \leqslant t_{RCD}$ (max).

14. Assumes that $t_{RCD} \geqslant t_{RCD}$ (max).

15. Measured with a load circuit equivalent to 2 TTL loads and 100pF.

16. Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.

17. V_{IHC} (min) or V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IHC} or V_{IH} and V_{IL}.

18. These parameters are referenced to $\overline{CAS}$ leading edge in random write cycles and $\overline{WRITE}$ leading edge in delayed write or read-modify-write cycles.

19. t_{WCS}, t_{CWD}, and t_{RWD} are restrictive operating parameters in a read/write or read/modify/write cycle only. If $t_{WCS} \geqslant t_{WCS}$ (min), the cycle is an early write cycle and Data Out will contain the data written into the selected cell. If $t_{CWD} \geqslant t_{CWD}$ (min) and $t_{RWD} \geqslant t_{RWD}$ (min), the cycle is a read-write cycle and Data Out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of Data Out (at access time) is indeterminate.

AC ELECTRICAL CHARACTERISTICS

$(0°C \leqslant T_A \leqslant 70°C)$ $(V_{DD} = 12.0V \pm 10\%; V_{SS} = 0V; -5.7V \leqslant V_{BB} \leqslant -4.5V)$

	PARAMETER	TYP	MAX	UNITS	NOTES
C_{I1}	Input Capacitance $(A_0\text{-}A_5)$, D_{IN}, $\overline{CS}$	4	5	pF	10
C_{I2}	Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	8	10	pF	10
C_0	Output Capacitance (D_{OUT})	5	7	pF	8,10

Figure 1. Maximum I_{DD1} versus cycle rate for device operation at extended frequencies.
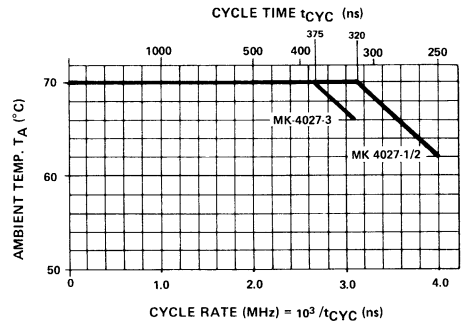
Figure 2. Maximum ambient temperature versus cycle rate for extended frequency operation.

READ CYCLE

t_{RC}
t_{RAS}
t_{AR}

$\overline{RAS}$ V_{IHC} V_{IL}

t_{CSH}
t_{RCD}
t_{RSH}
t_{RP}
t_{CAS}
t_{CRP}

$\overline{CAS}$ V_{IHC} V_{IL}

t_{ASR} t_{RAH} t_{ASC} t_{CAH}

ADDRESSES V_{IH} V_{IL} ROW ADDRESS COLUMN ADDRESS

t_{RCS} t_{RCH}

$\overline{WRITE}$ V_{IHC} V_{IL}

t_{CHR}
t_{CSC} t_{CH}

$\overline{CS}$ V_{IH} V_{IL}

t_{RAC}
t_{CAC}
t_{OFF} t_{DOH}

D_{OUT} V_{OH} V_{OL} OPEN VALID DATA

WRITE CYCLE

t_{RC}
t_{RAS}
t_{AR}

$\overline{RAS}$ V_{IHC} V_{IL}

t_{CSH}
t_{RCD}
t_{RSH}
t_{RP}
t_{CAS}
t_{CRP}

$\overline{CAS}$ V_{IHC} V_{IL}

t_{ASR} t_{RAH} t_{ASC} t_{CAH}

ADDRESSES V_{IH} V_{IL} ROW ADDRESS COLUMN ADDRESS

t_{WCS} t_{CWL}
t_{WCH}
t_{WP}

$\overline{WRITE}$ V_{IHC} V_{IL}

t_{WCR} t_{RWL}
t_{DS} t_{DH}

D_{IN} V_{IH} V_{IL} VALID DATA

t_{DHR}
t_{CSC} t_{CH}

$\overline{CS}$ V_{IH} V_{IL}

t_{CHR}
t_{RAC}
t_{CAC}
t_{OFF} t_{DOH}

D_{OUT} V_{OH} V_{OL} OPEN VALID DATA

4096 X 1-BIT DYN RAM

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READ-WRITE / READ-MODIFY-WRITE CYCLE

t_{RWC}/t_{RMW}

$\overline{RAS}$ — V_{IHC}, V_{IL} — t_{AR} — t_{RSH} — t_{RP}

$\overline{CAS}$ — V_{IHC}, V_{IL} — t_{RCD} — t_{CAS} — t_{CRP} — t_{CSH}

ADDRESSES — V_{IH}, V_{IL} — t_{ASR} — t_{RAH} — t_{ASC} — t_{CAH} — ROW ADDRESS — COLUMN ADDRESS

t_{RWD} — t_{CWD} — t_{CWL} — t_{RWL}

$\overline{WRITE}$ — V_{IHC}, V_{IL} — t_{RCS} — t_{WP}

t_{CHR} — t_{CSC} — t_{CH}

$\overline{CS}$ — V_{IH}, V_{IL}

t_{CAC} — t_{DOH}

t_{OFF}

D_{OUT} — V_{OH}, V_{OL} — OPEN — VALID DATA

t_{RAC}

t_{DS} — t_{DH}

D_{IN} — V_{IH}, V_{IL} — VALID DATA

"$\overline{RAS}$ ONLY" REFRESH CYCLE

t_{RC} — t_{RAS}

$\overline{RAS}$ — V_{IHC}, V_{IL} — t_{RAH} — t_{RP}

t_{ASR}

ADDRESSES — V_{IH}, V_{IL} — ROW ADDRESS

D_{OUT} — V_{OH}, V_{OL}

NOTE: D_{OUT} remains unchanged from previous cycle.

PAGE MODE READ CYCLE

$\overline{RAS}$ V_{IHC} — V_{IL} —

t_{RAS}, t_{AR}, t_{RSH}, t_{RP}

$\overline{CAS}$ V_{IHC} — V_{IL} —

t_{CSH}, t_{PC}, t_{RCD}, t_{CAS}, t_{CP}, t_{CAS}, t_{CAS}, t_{CRP}

t_{RAH}, t_{CAH}, t_{CAH}

ADDRESS V_{IH} — V_{IL} —

t_{ASR}, t_{ASC}, t_{ASC}, t_{ASC}

ROW ADD, COL ADD, COL ADD, COL ADD

t_{CHR}, t_{CH}, t_{CH}, t_{CH}

$\overline{CS}$ V_{IH} — V_{IL} —

t_{CSC}, t_{CSC}, t_{CSC}

t_{RAC}, t_{CAC}, t_{CAC}, t_{CAC}, t_{OFF}, t_{OFF}, t_{OFF}, t_{DOH}

D_{OUT} V_{OH} — V_{OL} —

VALID DATA, VALID DATA, VALID DATA

t_{RCS}, t_{RCH}, t_{RCS}, t_{RCH}

$\overline{WRITE}$ V_{IHC} — V_{IL} —

PAGE MODE WRITE CYCLE

$\overline{RAS}$ V_{IHC} — V_{IL} —

t_{RAS}, t_{AR}, t_{RSH}, t_{RP}

$\overline{CAS}$ V_{IHC} — V_{IL} —

t_{CSH}, t_{PC}, t_{RCD}, t_{CAS}, t_{CP}, t_{CAS}, t_{CAS}, t_{CRP}

t_{RAH}, t_{CAH}, t_{CAH}, t_{CAH}

ADDRESSES V_{IH} — V_{IL} —

t_{ASR}, t_{ASC}, t_{ASC}, t_{ASC}

ROW ADD, COL ADD, COL ADD, COL ADD

t_{CH}, t_{CH}, t_{CH}

$\overline{CS}$ V_{IH} — V_{IL} —

t_{CSC}, t_{CSC}, t_{CSC}

t_{CHR}

t_{OFF}, t_{OFF}, t_{OFF}, t_{DOH}

D_{OUT} V_{OH} — V_{OL} —

VALID DATA, VALID DATA, VALID DATA

t_{WCH}, t_{CWL}, t_{WCH}, t_{CWL}, t_{WCH}, t_{CWL}

$\overline{WRITE}$ V_{IHC} — V_{IL} —

t_{WCR}, t_{RWL}

t_{DS}, t_{WP}, t_{DH}, t_{DS}, t_{WP}, t_{DH}, t_{DS}, t_{WP}, t_{DH}

D_{IN} V_{IH} — V_{IL} —

VALID DATA, VALID DATA, VALID DATA

t_{DHR}

ADDRESSING

The 12 address bits required to decode 1 of the 4096 cell locations within the MK 4027 are multiplexed onto the 6 address inputs and latched into the on-chip address latches by externally applying two negative going TTL level clocks. The first clock, the Row Address Strobe ($\overline{RAS}$), latches the 6 row address bits into the chip. The second clock, the Column Address Strobe ($\overline{CAS}$), subsequently latches the 6 column address bits plus Chip Select ($\overline{CS}$) into the chip. The internal circuitry of the MK 4027 is designed to allow the column information to be externally applied to the chip before it is actually required. Because of this, the hold time requirements for the input signals associated with the Column Address Strobe are also referenced to $\overline{RAS}$. However, this gated $\overline{CAS}$ feature allows the system designer to compensate for timing skews that may be encountered in the multiplexing operation. Since the Chip Select signal is not required until $\overline{CAS}$ time, which is well into the memory cycle, its decoding time does not add to system access or cycle time.

DATA INPUT/OUTPUT

Data to be written into a selected cell is latched into an on-chip register by a combination of $\overline{WRITE}$ and $\overline{CAS}$ while $\overline{RAS}$ is active. The later of the signals ($\overline{WRITE}$ or $\overline{CAS}$) to make its negative transition is the strobe for the Data In register. This permits several options in the write cycle timing. In a write cycle, if the $\overline{WRITE}$ input is brought low prior to $\overline{CAS}$, the Data In is strobed by $\overline{CAS}$, and the set-up and hold times are referenced to $\overline{CAS}$. If the data input is not available at $\overline{CAS}$ time or if it is desired that the cycle be a read-write cycle, the $\overline{WRITE}$ signal must be delayed until after $\overline{CAS}$. In this "delayed write cycle" the data input set-up and hold times are referenced to the negative edge of $\overline{WRITE}$ rather than to $\overline{CAS}$. (To illustrate this feature, Data In is referenced to $\overline{WRITE}$ in the timing diagram depicting the read-write and page mode write cycles while the "early write" cycle diagram shows Data In referenced to $\overline{CAS}$.) Note that if the chip is unselected ($\overline{CS}$ high at $\overline{CAS}$ time) $\overline{WRITE}$ commands are not executed and, consequently, data stored in the memory is unaffected.

Data is retrieved from the memory in a read cycle by maintaining $\overline{WRITE}$ in the inactive or high state throughout the portion of the memory cycle in which $\overline{CAS}$ is active. Data read from the selected cell will be available at the output within the specified access time.

DATA OUTPUT LATCH

Any change in the condition of the Data Out Latch is initiated by the $\overline{CAS}$ signal. The output buffer is not affected by memory (refresh) cycles in which only the $\overline{RAS}$ signal is applied to the MK 4027.

Whenever $\overline{CAS}$ makes a negative transition, the output will go unconditionally open-circuited, independent of the state of any other input to the chip. If the cycle in progress is a read, read-modify-write, or a delayed write cycle and the chip is selected, then the output latch and buffer will again go active and at access time will contain the data read from the selected cell. This output data is the same polarity (not inverted) as the input data. If the cycle in progress is a write cycle ($\overline{WRITE}$ active low before $\overline{CAS}$ goes low) and the chip is selected, then at access time the output latch and buffer will contain the input data. Once having gone active, the output will remain valid until the MK 4027 receives the next $\overline{CAS}$ negative edge. Intervening refresh cycles in which a $\overline{RAS}$ is received (but no $\overline{CAS}$) will not cause valid data to be affected. Conversely, the output will assume the open-circuit state during any cycle in which the MK 4027 receives a $\overline{CAS}$ but no $\overline{RAS}$ signal (regardless of the state of any other inputs). The output will also assume the open circuit state in normal cycles (in which both $\overline{RAS}$ and $\overline{CAS}$ signals occur) if the chip is unselected.

The three-state data output buffer presents the data output pin with a low impedance to V_{CC} for a logic 1 and a low impedance to V_{SS} for a logic 0. The output resistance to V_{CC} (logic 1 state) is $420\,\Omega$ maximum and $135\,\Omega$ typically. The output resistance to V_{SS} (logic 0 state) is $125\,\Omega$ maximum and $35\,\Omega$ typically. The separate V_{CC} pin allows the output buffer to be powered from the supply voltage of the logic to which the chip is interfaced. During battery standby operation, the V_{CC} pin may have power removed without affecting the MK 4027 refresh operation. This allows all system logic except the $\overline{RAS}$ timing circuitry and the refresh address logic to be turned off during battery standby to conserve power.

REFRESH

Refresh of the dynamic cell matrix is accomplished by performing a memory cycle at each of the 64 row addresses within each 2 millisecond time interval. Any cycle in which a $\overline{RAS}$ signal occurs, accomplishes a refresh operation. A read cycle will refresh the selected row, regardless of the state of the Chip Select ($\overline{CS}$) input. A write or read-modify-write cycle also refreshes the selected row, but the chip should be unselected to prevent writing data into the selected cell. If, during a refresh cycle, the MK 4027 receives a $\overline{RAS}$ signal but no $\overline{CAS}$ signal, the state of the output will not be affected. However, if "$\overline{RAS}$-only" refresh cycles (where $\overline{RAS}$ is the only signal applied to the chip) are continued for extended periods, the output buffer may eventually lose proper data and go open-circuit. The output buffer will regain activity with the first cycle in which a $\overline{CAS}$ signal is applied to the chip.

POWER DISSIPATION/STANDBY MODE

Most of the circuitry used in the MK 4027 is dynamic and most of the power drawn is the result of an address strobe edge. Because the power is not drawn during the whole time the strobe is active, the dynamic power is a function of operating frequency rather than active duty cycle. Typically, the power is 170mW at 1 μsec cycle rate for the MK 4027 with a worse case power of less than 470mW at 320nsec cycle time. To minimize the overall system power, the Row Address Strobe ($\overline{RAS}$) should be decoded and supplied to only the selected chips. The $\overline{CAS}$ must be supplied to all chips (to turn off the unselected output). Those chips that did not receive a $\overline{RAS}$, however, will not dissipate any power on the $\overline{CAS}$ edges, except for that required to turn off the outputs. If the $\overline{RAS}$ signal is decoded and supplied only to the selected chips, then the Chip Select ($\overline{CS}$) input of all chips can be at a logic 0. The chips that receive a $\overline{CAS}$ but no $\overline{RAS}$ will be unselected (output open-circuited) regardless of the Chip Select input. For refresh cycles, however, either the $\overline{CS}$ input of all chips must be high or the $\overline{CAS}$ input must be held high to prevent several "wire-OR'd" outputs from turning on with opposing force. Note that the MK 4027 will dissipate considerably less power when the refresh operation is accomplished with a "$\overline{RAS}$-only" cycle as opposed to a normal $\overline{RAS}/\overline{CAS}$ memory cycle.

PAGE MODE OPERATION

The "Page Mode" feature of the MK 4027 allows for successive memory operations at multiple column locations of the same row address with increased speed without an increase in power. This is done by strobing the row address into the chip and keeping the $\overline{RAS}$ signal at a logic 0 throughout all successive memory cycles in which the row address is common.

This "page mode" of operation will not dissipate the power associated with the negative going edge of $\overline{RAS}$. Also, the time required for strobing in a new row address is eliminated, thereby decreasing the access and cycle times. The chip select input ($\overline{CS}$) is operative in page mode cycles just as in normal cycles. It is not necessary that the chip be selected during the first operation in a sequence of page cycles. Likewise, the $\overline{CS}$ input can be used to select or disable any cycle(s) in a series of page cycles. This feature allows the page boundary to be extended beyond the 64 column locations in a single chip. The page boundary can be extended by applying $\overline{RAS}$ to multiple 4K memory blocks and decoding $\overline{CS}$ to select the proper block.

POWER UP

The MK 4027 requires no particular power supply sequencing so long as the Absolute Maximum Rating Conditions are observed. However, in order to insure compliance with the Absolute Maximum Ratings, MOSTEK recommends sequencing of power supplies such that V_{BB} is applied first and removed last. V_{BB} should never be more positive than V_{SS} when power is applied to V_{DD}.

Under system failure conditions in which one or more supplies exceed the specified limits significant additional margin against catastrophic device failure may be achieved by forcing $\overline{RAS}$ and Data Out to the inactive state.

After power is applied to the device, the MK 4027 requires several cycles before proper device operation is achieved. Any 8 cycles which perform refresh are adequate for this purpose.

4096 X 1-BIT DYN RAM
MK4027/P/J/N-1/2/3

TYPICAL DEVICE CHARACTERISTICS

TYPICAL ADDRESS AND DATA INPUT LEVELS vs. V_{DD}

$T_J = 50°C$
$V_{BB} = -5.0V$

INPUT LEVEL (VOLTS)

V_{IH} (MIN)

V_{IL} (MAX)

V_{DD} SUPPLY VOLTAGE (VOLTS)

TYPICAL CLOCK INPUT LEVELS vs. V_{DD}

$T_J = 50°C$
$V_{BB} = -5.0V$

INPUT LEVEL (VOLTS)

V_{IHC} (MIN)

V_{ILC} (MAX)

V_{DD} SUPPLY VOLTAGE (VOLTS)

TYPICAL ADDRESS AND DATA INPUT LEVELS vs. V_{BB}

$T_J = 50°C$
$V_{DD} = 12.0V$

INPUT LEVEL (VOLTS)

V_{IH} (MIN)

V_{IL} (MAX)

V_{BB} SUPPLY VOLTAGE (VOLTS)

TYPICAL CLOCK INPUT LEVELS vs. V_{BB}

$T_J = 50°C$
$V_{DD} = 12.0V$

INPUT LEVEL (VOLTS)

V_{IHC} (MIN)

V_{ILC} (MAX)

V_{BB} SUPPLY VOLTAGE (VOLTS)

TYPICAL ADDRESS AND DATA INPUT LEVELS vs. T_J

$V_{DD} = 12.0V$
$V_{BB} = -5.0V$

INPUT LEVEL (VOLTS)

V_{IH} (MIN)

V_{IL} (MAX)

T_J, JUNCTION TEMPERATURE (°C)

TYPICAL CLOCK INPUT LEVELS vs. T_J

$V_{DD} = 12.0V$
$V_{BB} = -5.0V$

INPUT LEVEL (VOLTS)

V_{IHC} (MAX)

V_{IL} (MAX)

T_J, JUNCTION TEMPERATURE (°C)

TYPICAL ACCESS TIME (NORMALIZED) vs. V$_{DD}$

$T_J = 50°C$

T$_{RAC}$ (V$_{DD}$)/T$_{RAC}$ (V$_{DD}$ = 12.0V)

1.2
1.1
1.0
0.9
0.8
0.7
10   11   12   13   14

V$_{DD}$ SUPPLY VOLTAGE (VOLTS)

TYPICAL ACCESS TIME (NORMALIZED) vs. V$_{BB}$

$T_J = 50°C$

T$_{RAC}$ (V$_{BB}$)/T$_{RAC}$ (V$_{BB}$ = −5.0V)

1.2
1.1
1.0
0.9
0.8
0.7
−4.0   −4.5   −5.0   −5.5   −6.0

V$_{BB}$ SUPPLY VOLTAGE (VOLTS)

TYPICAL ACCESS TIME (NORMALIZED) vs. V$_{CC}$

$T_J = 50°C$

T$_{RAC}$ (V$_{CC}$)/T$_{RAC}$ (V$_{CC}$ = 5.0V)

1.2
1.1
1.0
0.9
0.8
0.7
4.0   4.5   5.0   5.5   6.0

V$_{CC}$ SUPPLY VOLTAGE (VOLTS)

TYPICAL ACCESS TIME (NORMALIZED)
vs. JUNCTION TEMPERATURE

T$_{RAC}$ (T$_J$)/T$_{RAC}$ (T$_J$ = 50°C)

1.2
1.1
1.0
0.9
0.8
0.7
−10   20   50   80   110

T$_J$, JUNCTION TEMPERATURE (°C)

TYPICAL I$_{DD1}$ vs. V$_{DD}$

$T_J = 50°C$

I$_{DD1}$ SUPPLY CURRENT (mA)

35
30
25
20
15
10
10   11   12   13   14

t$_{RC}$ = 320ns
t$_{RC}$ = 375ns
t$_{RC}$ = 500ns
t$_{RC}$ = 600ns

V$_{DD}$ SUPPLY VOLTAGE VOLTS

TYPICAL I$_{DD1}$ vs. JUNCTION TEMPERATURE

I$_{DD1}$ SUPPLY CURRENT (mA)

35
30
25
20
15
10
−10   20   50   80   110

t$_{RC}$ = 320ns
t$_{RC}$ = 375ns
t$_{RC}$ = 500ns
t$_{RC}$ = 600ns

T$_J$, JUNCTION TEMPERATURE (°C)

4096 X 1-BIT DYN RAM

MOSTEK®

4096 x 1-BIT DYNAMIC RAM

MK4027(P/J/N)-4

FEATURES

□ Industry standard 16-pin DIP (MK 4096) configuration

□ 250ns access time, 380ns cycle

□ ±10% tolerance on all supplies (+12V, ±5V)

□ ECL compatible on V_{BB} power supply (−5.7V)

□ Low Power: 462mW active (max)
27mW standby (max)

□ Improved performance with "gated $\overline{CAS}$", "$\overline{RAS}$ only" refresh and page mode capability

□ All inputs are low capacitance and TTL compatible

□ Input latches for addresses, chip select and data in

□ Three-state TTL compatible output

□ Output data latched and valid into next cycle

DESCRIPTION

The MK 4027 is a 4096 word by 1 bit MOS random access memory circuit fabricated with MOSTEK's N-channel silicon gate process. This process allows the MK 4027 to be a high performance state-of-the-art memory circuit that is manufacturable in high volume. The MK 4027 employs a single transistor storage cell utilizing a dynamic storage technique and dynamic control circuitry to achieve optimum performance with low power dissipation.
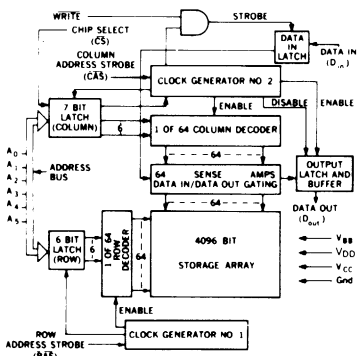
A unique multiplexing and latching technique for the address inputs permits the MK 4027 to be packaged in a standard 16-pin DIP on 0.3 in. centers. This package size provides high system-bit densities and is compatible with widely available automated testing and insertion equipment.

System oriented features include direct interfacing capability with TTL, only 6 very low capacitance address lines to drive, on-chip address and data registers which eliminates the need for interface registers, input logic levels selected to optimize noise immunity, and two chip select methods to allow the user to determine the appropriate sp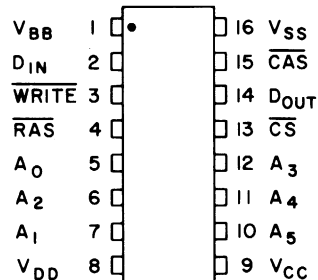eed/power characteristics of his memory system. The MK 4027 also incorporates several flexible operating modes. In addition to the usual read and write cycles, read-modify write, page-mode, and $\overline{RAS}$-only refresh cycles are available with the MK 4027. Page-mode timing is very useful in systems requiring Direct Memory Access (DMA) operation.

FUNCTIONAL DIAGRAM

PIN CONNECTIONS

PIN NAMES

A_0-A_5	ADDRESS INPUTS
$\overline{CAS}$	COLUMN ADDRESS STROBE
$\overline{CS}$	CHIP SELECT
D_{IN}	DATA IN
D_{OUT}	DATA OUT
$\overline{RAS}$	ROW ADDRESS STROBE
$\overline{WRITE}$	READ/WRITE INPUT
V_{BB}	POWER (−5V)
V_{CC}	POWER (+5V)
V_{DD}	POWER (+ 12V)
V_{SS}	GROUND

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to V_{BB} . . . . −0.5V to +20V
Voltage on V_{DD}, V_{CC} relative to V_{SS} . . . . −1.0V to +15V
$V_{BB}−V_{SS}$ ($V_{DD}−V_{SS} > 0$) 0V
Operating temperature, T_A (Ambient) . . . . 0°C to + 70°C
Storage temperature (Ambient)(Ceramic) . . . . −65°C to + 150°C
Storage temperature (Ambient)(Plastic) . . . . −55°C to + 125°C
Short Circuit Output Current 50mA
Power dissipation . . . . 1 Watt

RECOMMENDED DC OPERATING CONDITIONS [4]
(0°C ≤ T_A ≤ 70°C) [1]

	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{DD}	Supply Voltage	10.8	12.0	13.2	volts	2
V_{CC}	Supply Voltage	4.5V	5.0	5.5	volts	2,3
V_{SS}	Supply Voltage	0	0	0	volts	2
V_{BB}	Supply Voltage	−4.5	−5.0	−5.7	volts	2
V_{IHC}	Logic 1 Voltage, $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	2.4		7.0	volts	2
V_{IH}	Logic 1 Voltage, all inputs except $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	2.2		7.0	volts	2
V_{IL}	Logic 0 Voltage, all inputs	−1.0		.8	volts	2

DC ELECTRICAL CHARACTERISTICS [4]
(0°C ≤ T_A ≤ 70°C)[1] (V_{DD} = 12.0V ± 10%; V_{CC} = 5.0V ± 10%; V_{SS} = 0V; −5.7V ≤ V_{BB} ≤ −4.5V)

	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
I_{DD1}	Average V_{DD} Power Supply Current			35	mA	5
I_{DD2}	Standby V_{DD} Power Supply Current			2	mA	8
I_{DD3}	Average V_{DD} Power Supply Current during "$\overline{RAS}$ only" cycles			25	mA	
I_{CC}	V_{CC} Power Supply Current				mA	6
I_{BB}	Average V_{BB} Power Supply Current			150	μA	
$I_{I(L)}$	Input Leakage Current (any input)			10	μA	7
$I_{O(L)}$	Output Leakage Current			10	μA	8,9
V_{OH}	Output Logic 1 Voltage @ I_{OUT} = −5mA	2.4			volts	
V_{OL}	Output Logic 0 Voltage @ I_{OUT} = 3.2mA			0.4	volts	

NOTES

1. T_A is specified for operation at frequencies to t_{RC} ≥ t_{RC} (min).

2. All voltages referenced to V_{SS}.

3. Output voltage will swing from V_{SS} to V_{CC} when enabled, with no output load. For purposes of maintaining data in standby mode, V_{CC} may be reduced to V_{SS} without affecting refresh operations or data retention. However, the V_{OH} (min) specification is not guaranteed in this mode.

4. Several cycles are required after power-up before proper device operation is achieved. Any 8 cycles which perform refresh are adequate for this purpose.

5. Current is proportional to cycle rate. I_{DD1} (max) is measured at the cycle rate specified by t_{RC} (min). See figure 1 for I_{DD1} limits at other cycle rates.

6. I_{CC} depends on output loading. During readout of high level data V_{CC} is connected through a low impedance (135Ω typ) to Data Out. At all other times I_{CC} consists of leakage currents only.

7. All device pins at 0 volts except V_{BB} which is at −5 volts and the pin under test which is at +10 volts.

8. Output is disabled (high-impedance) and $\overline{RAS}$ and $\overline{CAS}$ are both at a logic 1. Transient stabilization is required prior to measurement of this parameter.

9. 0V ≤ V_{OUT} ≤ + 10V.

10. Effective capacitance is calculated from the equation:

$$C = \frac{\Delta Q}{\Delta V} \text{ with } \Delta V = 3 \text{ volts.}$$

11. A.C. measurements assume t_T = 5ns.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS[4, 11, 17]

$(0°C \leqslant T_A \leqslant 70°C)^1$ $(V_{DD} = 12.0V \pm 10\%, V_{CC} = 5.0V \pm 10\%, V_{SS} = 0V, -5.7V \leqslant V_{BB} \leqslant -4.5V)$

	PARAMETER	MK4027-4 MIN	MK4027-4 MAX	UNITS	NOTES
t_{RC}	Random read or write cycle time	380		ns	
t_{RWC}	Read write cycle time	395		ns	
t_{RMW}	Read modify write cycle time	470		ns	
t_{PC}	Page mode cycle time	285		ns	
t_{RAC}	Access time from row address strobe		250	ns	13, 15
t_{CAC}	Access time from column address strobe		165	ns	14, 15
t_{OFF}	Output buffer turn-off delay		60	ns	
t_{RP}	Row address strobe precharge time	120		ns	
t_{RAS}	Row address strobe pulse width	250	10,000	ns	
t_{RSH}	Row address strobe hold time	165		ns	
t_{CAS}	Column address strobe pulse width	165		ns	
t_{CSH}	Column address strobe hold time	250		ns	
t_{RCD}	Row to column strobe delay	35	85	ns	16
t_{ASR}	Row address set-up time	0		ns	
t_{RAH}	Row address hold time	35		ns	
t_{ASC}	Column address set-up time	-10		ns	
t_{CAH}	Column address hold time	75		ns	
t_{AR}	Column address hold time referenced to $\overline{RAS}$	160		ns	
t_{CSC}	Chip select set-up time	-10		ns	
t_{CH}	Chip select hold time	75		ns	
t_{CHR}	Chip select hold time referenced to $\overline{RAS}$	160		ns	
t_T	Transition time (rise and fall)	3	50	ns	17
t_{RCS}	Read command set-up time	0		ns	
t_{RCH}	Read command hold time	0		ns	
t_{WCH}	Write command hold time	75		ns	
t_{WCR}	Write command hold time referenced to $\overline{RAS}$	160		ns	
t_{WP}	Write command pulse width	75		ns	
t_{RWL}	Write command to row strobe lead time	85		ns	
t_{CWL}	Write command to column strobe lead time	85		ns	
t_{DS}	Data in set-up time	0		ns	18
t_{DH}	Data in hold time	75		ns	18
t_{DHR}	Data in hold time referenced to $\overline{RAS}$	160		ns	
t_{CRP}	Column to row strobe precharge time	0		ns	
t_{CP}	Column precharge time	110		ns	
t_{RFSH}	Refresh period		2	ms	
t_{WCS}	Write command set-up time	0		ns	19
t_{CWD}	$\overline{CAS}$ to $\overline{WRITE}$ delay	90		ns	19
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ delay	175		ns	19
t_{DOH}	Data out hold time	10		μs	

Notes Continued

13. Assumes that $t_{RCD} \leqslant t_{RCD}$ (max).

14. Assumes that $t_{RCD} \geqslant t_{RCD}$ (max).

15. Measured with a load circuit equivalent to 2 TTL loads and 100pF

16. Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.

17. V_{IHC} (min) or V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IHC} or V_{IH} and V_{IL}.

18. These parameters are referenced to $\overline{CAS}$ leading edge in random write cycles and to $\overline{WRITE}$ leading edge in delayed write or read-modify-write cycles.

19. t_{WCS}, t_{CWD}, and t_{RWD} are restrictive operating parameters in a read/write or read/modify/write cycle only. If $t_{WCS} \geqslant t_{WCS}$ (min), the cycle is an early write cycle and Data Out will contain the data written into the selected cell. If $t_{CWD} \geqslant t_{CWD}$ (min) and $t_{RWD} \geqslant t_{RWD}$ (min), the cycle is a read-write cycle and Data Out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of Data Out (at access time) is indeterminate.

AC ELECTRICAL CHARACTERISTICS

$(0°C \leqslant T_A \leqslant 70°C)$ $(V_{DD} = 12.0V \pm 10\%; V_{SS} = 0V; -5.7V \leqslant V_{BB} \leqslant -4.5V)$

	PARAMETER	TYP	MAX	UNITS	NOTES
C_{I1}	Input Capacitance (A_0-A_5), D_{IN}, $\overline{CS}$	4	5	pF	10
C_{I2}	Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	8	10	pF	10
C_0	Output Capacitance (D_{OUT})	5	7	pF	8,10

MAXIMUM I_{DD1} vs. CYCLE RATE FOR DEVICE OPERATION AT EXTENDED FREQUENCIES

Figure 1
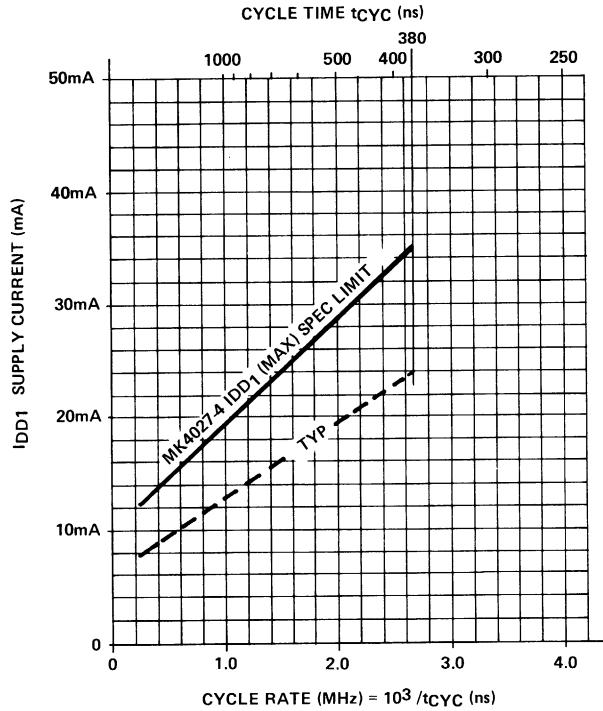
SUPPLEMENT - To be used in conjunction with MK4027(P/J/N)-1/2/3 data sheet.

MOSTEK®

4096 x 1-BIT DYNAMIC RAM

MK4096(K/N)-6/16/11

FEATURES

□ Industry standard 16-pin DIP configuration (available in plastic (N) and ceramic (K) packages)

□ All inputs are low capacitance and TTL compatible

□ Input latches for address, chip select and data in

□ Inputs protected against static charge

□ Three-state TTL compatible output, latched and valid into next cycle

□ Proven reliability with high performance

DESCRIPTION

The MK 4096 is the recognized industry standard 4096 word by 1 bit MOS Random Access Memory circuit packaged in a standard 16-pin DIP on 0.3 inch centers. This package configuration is made possible by a unique multiplexing and latching technique for the address inputs. The use of the 16-pin DIP for the MK 4096 provides high system bit densities and is compatible with widely available automated testing and insertion equipment.

The MK 4096 is fabricated with MOSTEK's standard Self-Aligned, Poly-Interconnect, N-Channel (SPIN) process. The SPIN process allows the MK 4096 to be a highly manufacturable, state-of-the-art memory circuit that exhibits the reliability and performance standards necessary for today's (and tomorrow's) data processing applications. The MK 4096 employs a single transistor storage cell, utilizing a dynamic storage technique and dynamic control circuitry to

achieve optimum performance with low power dissipation.

System oriented features incorporated within the MK 4096 include direct interfacing capability with TTL, 6 instead of 12 address lines to drive, on-chip registers which can eliminate the need for interface registers, input logic levels selected to optimize the noise immunity, and two chip select methods to allow the user to determine the speed/power characteristics of his memory system.

Part Number	Access Time	Cycle Time	Max Power*
MK 4096—6	250 ns	375 ns	450mW
MK 4096—16	300 ns	425 ns	385mW
MK 4096—11	350 ns	500 ns	320mW

*Standby power for all parts < 19mW

FUNCTIONAL DIAGRAM

PIN CONNECTIONS

PIN NAMES

$A_0 - A_5$	ADDRESS INPUTS	D_{IN}	DATA IN
$\overline{CAS}$	COLUMN ADDRESS STROBE	D_{OUT}	DATA OUT
$\overline{CS}$	CHIP SELECT	V_{BB}	POWER (−5V)
$\overline{RAS}$	ROW ADDRESS STROBE	V_{CC}	POWER (+5V)
$\overline{WRITE}$	READ/WRITE INPUT	V_{DD}	POWER (+12V)
		V_{SS}	GROUND

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to V_{BB} .... −0.5V to + 25V
$(V_{SS}-V_{BB} \geqslant 4.5V$
Operating temperature T_A (Ambient) .... 0°C to + 70°C
Storage temperature (Ceramic) ...... −65°C to + 150°C
Storage temperature (Plastic) .... −55°C to + 125°C
Power dissipation .... 1 Watt
Data out current 50mA

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS (17)
(0°C $\leqslant T_A \leqslant$ +70°C)

	PARAMETER	MK 4096−6 MIN	MK 4096−6 MAX	MK 4096−16 MIN	MK 4096−16 MAX	MK 4096−11 MIN	MK 4096−11 MAX	UNITS	NOTE
V_{DD}	Supply Voltage	11.4	12.6	11.4	12.6	11.4	12.6	Volts	1
V_{CC}	Supply Voltage	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V_{SS}	V_{DD}	Volts	1,2
V_{SS}	Supply Voltage	0	0	0	0	0	0	Volts	1
V_{BB}	Supply Voltage	−4.5	−5.5	−4.5	−5.5	−4.5	−5.5	Volts	1
V_{IHC}	Logic 1 Voltage − $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	2.7	7.0	2.7	7.0	3.0	7.0	Volts	1,3
V_{IH}	Logic 1 Voltage, all inputs except $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	2.4	7.0	2.4	7.0	2.4	7.0	Volts	1,3
V_{IL}	Logic 0 Voltage, all inputs	−1.0	0.8	−1.0	0.8	−1.0	0.8	Volts	1,3

DC ELECTRICAL CHARACTERISTICS (17)
(0°C $\leqslant T_A \leqslant$ 70°C)(V_{DD} = 12.0V ± 5%; V_{CC} = 5.0V ± 10%; V_{SS} = 0V; V_{BB} = −5.0V ± 10%)

	PARAMETER	MK4096-6 MIN	MK4096-6 MAX	MK4096-16 MIN	MK4096-16 MAX	MK4096-11 MIN	MK4096-11 MAX	UNITS	NOTES
I_{DD1}	Average V_{DD} Power Supply Current		35		30		25	mA	4
I_{CC}	V_{CC} Power Supply Current							mA	5
I_{BB}	Average V_{BB} Power Supply Current		75		75		75	μA	
I_{DD2}	Standby V_{DD} Power Supply Current		1.5		1.5		1.5	mA	7
I_{DD3}	Average V_{DD} Supply Current during "$\overline{RAS}$-only" cycles		25		22		18	mA	4
$I_{I(L)}$	Input Leakage Current (any input)		5		5		5	μA	6
$I_{O(L)}$	Output Leakage Current		10		10		10	μA	7,8
V_{OH}	Output Logic 1 Voltage @ I_{OUT} = −5mA	2.4		2.4		2.4		Volts	2
V_{OL}	Output Logic 0 Voltage @ I_{OUT} = 2mA		0.4		0.4		0.4	Volts	

NOTES

1. All voltages referenced to V_{SS}. V_{BB} must be applied to and removed from the device within 5 seconds of V_{DD}.

2. Output voltage will swing from V_{SS} to V_{CC} if $V_{CC} \leqslant V_{DD}$ −4 volts. If $V_{CC} \geqslant V_{DD}$ −4 volts, the output will swing from V_{SS} to a voltage somewhat less than V_{DD}.

3. Device speed is not guaranteed at input voltages greater than TTL levels (0 to 5V).

4. Current is proportional to cycle rate; maximum current is measured at the fastest cycle rate.

5. I_{CC} depends upon output loading. The V_{CC} supply is connected to the output buffer only.

6. All device pins at 0 volts except V_{BB} which is at −5 volts and the pin under test which is at +10 volts.

7. Output is disabled (open-circuit) and $\overline{RAS}$ and $\overline{CAS}$ are both at a logic 1.

8. 0V $\leqslant V_{OUT} \leqslant$ +10V.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (10, 15, 17)

$(0°C \leqslant T_A \leqslant 70°C)$ $(V_{DD} = 12.0V \pm 5\%, V_{CC} = 5.0V \pm 10\%, V_{SS} = 0V, V_{BB} = -5.0V \pm 10\%)$

	PARAMETER	MK 4096-6 MIN	MK 4096-6 MAX	MK 4096-16 MIN	MK 4096-16 MAX	MK 4096-11 MIN	MK 4096-11 MAX	UNITS	NOTES
t_{RC}	Random Read or Write Cycle Time	375		425		500		nsec	11
t_{RAC}	Access time from Row Address Strobe		250		300		350	nsec	11,13
t_{CAC}	Access Time from Column Address Strobe		140		165		200	nsec	12,13
t_{OFF}	Output Buffer Turn-Off Delay	0	65	0	80	0	100	nsec	
t_{RP}	Row Address Strobe Precharge Time	115		125		150		nsec	
t_{RAS}	Row Address Strobe Pulse Width	250	10,000	300	10,000	350	10,000	nsec	
t_{RCL}	Row To Column Strobe Lead Time	60	110	80	135	100	150	nsec	14
t_{CAS}	Column Address Strobe Pulse Width	140		165		200		nsec	12
t_{AS}	Address Set-Up Time	0		0		0		nsec	
t_{AH}	Address Hold Time	60		80		100		nsec	
t_{CH}	Chip Select Hold Time	100		100		100		nsec	
t_T	Rise and Fall Times	3	50	3	50	3	50	nsec	15
t_{RCS}	Read Command Set-Up Time	0		0		0		nsec	
t_{RCH}	Read Command Hold Time	0		0		0		nsec	
t_{WCH}	Write Command Hold Time	110		130		150		nsec	
t_{WP}	Write Command Pulse Width	110		130		150		nsec	
t_{CRL}	Column to Row Strobe Lead Time	−40	+40	−50	+50	−50	+50	nsec	
t_{CWL}	Write Command to Column Strobe Lead Time	110		130		150		nsec	
t_{DS}	Data In Set-Up Time	0		0		0		nsec	16
t_{DH}	Data In Hold Time	110		130		150		nsec	16
t_{RFSH}	Refresh Period		2		2		2	msec	
t_{MOD}	Modify Time		10		10		10	μsec	
t_{DOH}	Data Out Hold Time	10		10		10		μsec	

4096 X 1-BIT DYN RAM MK4096(K)(N)-6/16/11

NOTES Continued

9. Capacitance measured with Boonton Meter or effective capacitance calculated from the equation: $C = \frac{I \triangle t}{\triangle V}$ with current equal to a constant 20mA and $\triangle V = 3V$.

10. A C measurements assume $t_T = 5$ns.

11. Assumes that $t_{RCL} + t_T \leqslant t_{RCL}$ (max).

12. Assumes that $t_{RCL} + t_T \geqslant t_{RCL}$ (max).

13. Measured with a load circuit equivalent to 1 TTL load and $C_L = 100$pF

14. Operation within the t_{RCL} (max) limit insures that t_{RAC} (max) can be met. t_{RCL} (max) is specified as a reference point only; if t_{RCL} is greater than the specified t_{RCL} (max) limit, then access time is controlled exclusively by t_{CAC} and t_{RAS}, t_{RAC} and t_{RCL} will be longer by the amount $t_{RCL} + t_T$ exceeds t_{RCL} (max).

15. V_{IHC} (min) or V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IHC} or V_{IH} and V_{IL}.

16. These parameters are referenced to $\overline{CAS}$ leading edge in random write cycles and to $\overline{WRITE}$ leading edge in delayed write or read-modify-write cycles.

17. After the application of supply voltages or after extended periods of operation without clocks, the device must perform a minimum of one initialization cycle (any valid memory cycle containing both $\overline{RAS}$ and $\overline{CAS}$) prior to normal operation.

AC ELECTRICAL CHARACTERISTICS

($0°C \leqslant T_A \leqslant +70°C$) ($V_{DD}$ = 12.0V ± 5%, V_{CC} = 5.0V ±10%, V_{SS} = 0V, V_{BB} = −5.0V ± 10%)

	PARAMETER	TYP	MAX	UNITS	NOTES
C_{I1}	Input Capacitance ($A_0 - A_5$)	7	10	pF	9
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, D_{IN}, $\overline{WRITE}$, $\overline{CS}$)	5	7	pF	9
C_0	Output Capacitance (D_{OUT})	5	8	pF	7,9

TIMING WAVEFORMS

READ CYCLE

WRITE CYCLE

TIMING WAVEFORMS

READ-WRITE/READ-MODIFY-WRITE CYCLE

"RAS ONLY" REFRESH CYCLE

NOTE:

Prior to the first memory cycle following a period (beyond 2mS) of "RAS-only refresh, a memory-cycle employing both RAS and CAS must be performed to insure proper device operation.

ADDRESSING

The 12 address bits required to decode one of the 4096 cell locations within the MK 4096 are multiplexed onto the 6 address inputs and latched into the on-chip address latches by externally applying two negative going TTL level clocks. The first clock, the Row Address Strobe ($\overline{RAS}$), latches the 6 row address bits into the chip. The second clock, the Column Address Strobe ($\overline{CAS}$), subsequently latches the 6 column address bits plus Chip Select ($\overline{CS}$) into the chip. (Note that since the Chip Select signal is not required until $\overline{CAS}$ time, which is well into the memory cycle, its decoding time does not add to system access or cycle time). Each of these signals, $\overline{RAS}$ and $\overline{CAS}$, triggers a sequence of events which are controlled by different delayed internal clocks. The two clock chains are linked together logically in such a way that the address multiplexing operation is done outside of the critical path timing sequence for read data access. The later events in the $\overline{CAS}$ clock sequence are inhibited until the occurrence of a delayed signal derived from the $\overline{RAS}$ clock chain. This "gated $\overline{CAS}$" feature allows the $\overline{CAS}$ clock to be externally activated as soon as the Row Address Hold Time specification (t_{AH}) has been satisfied and the 6 address inputs have been changed from Row address to Column address information.

Note that $\overline{CAS}$ can be activated at any time after t_{AH} and it will have no effect on the worst case data access time (t_{RAC}) up to the point in time when the delayed row clock no longer inhibits the remaining sequence of column clocks. Two timing end points result from the internal gating of $\overline{CAS}$ which are called t_{RCL} (min) and t_{RCL} (max). No data storage or reading errors will result if $\overline{CAS}$ is applied to the MK 4096 at a point in time beyond the t_{RCL} (max) limit. However, access time will then be determined exclusively by the access time from $\overline{CAS}$ (t_{CAC}) rather than from $\overline{RAS}$ (t_{RAC}), and access time from $\overline{RAS}$ will be lengthened by the amount that t_{RCL} exceeds the t_{RCL} (max) limit.

DATA INPUT/OUTPUT

Data to be written into a selected cell is latched into an on-chip register by a combination of $\overline{WRITE}$ and $\overline{CAS}$ while $\overline{RAS}$ is active. The later of the signals ($\overline{WRITE}$ or $\overline{CAS}$) to make its negative transition is the strobe for the Data In register. This permits several options in the write cycle timing. In a write cycle, if the $\overline{WRITE}$ input is brought low prior to $\overline{CAS}$, the Data In is strobed by $\overline{CAS}$, and the set-up and hold times are referenced to $\overline{CAS}$. If the data input is not available at $\overline{CAS}$ time or if it is desired that the cycle be a read-write or read-modify-write cycle, the $\overline{WRITE}$ signal must be delayed until after $\overline{CAS}$. In this "delayed write cycle" the data input set-up and hold times are referenced to the negative edge of $\overline{WRITE}$ rather than to $\overline{CAS}$.

(To illustrate this feature, Data In is referenced to $\overline{WRITE}$ in the timing diagram depicting the read-modify-write cycle while the "early write" cycle diagram shows Data In referenced to $\overline{CAS}$). Note that if the chip is unselected ($\overline{CS}$ high at $\overline{CAS}$ time) $\overline{WRITE}$ commands are not executed and, consequently, data stored in the memory is unaffected.

Data is retrieved from the memory in a read cycle by maintaining $\overline{WRITE}$ in the inactive or high state throughout the portion of the memory cyle in which $\overline{CAS}$ is active. Data read from the selected cell will be available at the output within the specified access time.

DATA OUTPUT LATCH

Any change in the condition of the Data Out Latch is initiated by the $\overline{CAS}$ signal. The output buffer is not affected by memory (refresh) cycles in which only the $\overline{RAS}$ signal is applied to the MK 4096. Whenever $\overline{CAS}$ makes a negative transition, the output will go unconditionally open-circuited, independent of the state of any other input to the chip. If the cycle in progress is a read, read-modify-write, or a delayed write cycle and the chip is selected, then the output latch and buffer will again go active and at access time will contain the data read from the selected cell. This output data is the same polarity (not inverted) as the input data. If the cycle in progress is a write cycle ($\overline{WRITE}$ active low before $\overline{CAS}$ goes low) and the chip is selected, then at access time the output latch and buffer will contain a logic 1. Once having gone active, the output will remain valid until the MK 4096 receives the next $\overline{CAS}$ negative edge. Intervening refresh cycles in which a $\overline{RAS}$ is received (but no $\overline{CAS}$) will not cause valid data to be affected. Conversely, the output will assume the open-circuit state during any cycle in which the MK 4096 receives a $\overline{CAS}$ but no $\overline{RAS}$ signal (regardless of the state of any other inputs). The output will also assume the open-circuit state in normal cycles (in which both $\overline{RAS}$ and $\overline{CAS}$ signals occur) if the chip is unselected.

The three-state data output buffer presents the data output pin with a low impedance to V_{CC} for a logic 1 and a low impedance to V_{SS} for a logic 0. The effective resistance to V_{CC} (logic 1 state) is 500Ω maximum and 150Ω typically. The resistance to V_{SS} (logic 0 state) is 200Ω maximum and 100Ω typically. The separate V_{CC} pin allows the output buffer to be powered from the supply voltage of the logic to which the chip is interfaced. During battery standby operation, the V_{CC} pin may have power removed without affecting the MK 4096 refresh operation. This allows all system logic except the $\overline{RAS}/\overline{CAS}$ timing circuitry and the refresh address logic to be turned off during battery standby to conserve power.

REFRESH

Refresh of the dynamic cell matrix is accomplished by performing a memory cycle at each of the 64 row addresses within each 2 millisecond time interval. Any cycle in which a $\overline{RAS}$ signal occurs accomplishes a refresh operation. A read cycle will refresh the selected row, regardless of the Chip Select ($\overline{CS}$) input. A write or read-modify-write cycle also refreshes the selected row, but the chip should be unselected to prevent writing data into the selected cell.

For standby operation, a "$\overline{RAS}$-only" cycle can be employed to refresh the MK 4096. However, if "$\overline{RAS}$-only" refresh cycles (where $\overline{RAS}$ is the only signal applied to the chip) are continued for extended periods, the output buffer may eventually lose proper

data and go open-circuit. Prior to the first memory cycle following a period (beyond 2ms) of "RAS only" refresh, a memory cycle employing both RAS and CAS must be performed to precharge the internal circuitry. This "dummy cycle" allows the output buffer to regain activity and enables the device to perform a read or write cycle upon command.

POWER DISSIPATION/STANDBY MODE

Most of the circuitry used in the MK 4096 is dynamic and most of the power drawn is the result of an address strobe edge. Because the power is not drawn during the whole time the strobe is active, the dynamic power is a function of operating frequency rather than active duty cycle. Typically, the power is 120 mW at a 1 μsec cycle rate for the MK 4096 with a maximum power of less than 450 mW at 375 nsec cycle time. To minimize the overall system power, the Row Address Strobe (RAS) should be decoded and supplied to only the selected chips. The CAS must be supplied to all chips (to turn off the unselected output). Those chips that did not receive a RAS, however, will not dissipate any power on the CAS edges, except for that required to turn off the outputs. If the RAS signal is decoded and supplied only to the selected chips, then the Chip Select (CS) input of all chips can be at a logic 0. The chips that receive a CAS but no RAS will be unselected (output open-circuited) regardless of the Chip Select input. For refresh cycles, however, either the CS input of all chips must be high or the CAS input must be held high to prevent several "wire-ORed" outputs from turning on with opposing force.

The current waveforms for the current drawn from the V_{DD} and V_{BB} supplies are shown in Figure A. Since the current is pulsed, proper power distribution and bypassing techniques are required to maintain system power supply noise levels at an acceptable level. Low inductance supply lines for V_{DD} and V_{SS} are desirable. One 0.01 microfarad, low inductance, bypass capacitor per two MK 4096 devices and one 6.8 microfarad electrolytic capacitor per eight MK 4096 devices on each of the V_{DD} and V_{BB} supply lines is desirable.

POWER—UP

Under normal operating conditions the MK 4096 requires no particular power-up sequence. However, in order to achieve the most reliable performance from the MK 4096, proper consideration should be given to the V_{BB}/V_{DD} power supply relationship. The V_{BB} supply is an extremely important "protective voltage" since it performs two essential functions within the device. It establishes proper junction isolation and sets field-effect thresholds, both thin field and thick field. Misapplication of V_{BB} or device operation without the V_{BB} supply can affect long term device reliability. For optimum reliability performance from the MK 4096, it is suggested that measures be taken to not have V_{DD} (+12V) applied to the device for over five (5) seconds without the application of V_{BB} (−5V).

After power is applied to the device, the MK 4096 requires at least one memory cycle (RAS/CAS) before proper device operation is achieved. A normal 64 cycle refresh with both RAS and CAS is adequate for this purpose.

POWER SUPPLY CURRENT WAVEFORMS

ROW ADD STROBE (RAS)

COL ADD STROBE (CAS)

CURRENT
DRAWN
FROM
SUPPLIES
} I_{DD} $\left(\begin{array}{c}\text{+12 VOLT}\\\text{SUPPLY}\end{array}\right)$

I_{BB} $\left(\begin{array}{c}\text{−5 VOLT}\\\text{SUPPLY}\end{array}\right)$

(50 MA/DIV)

100 ns/DIV
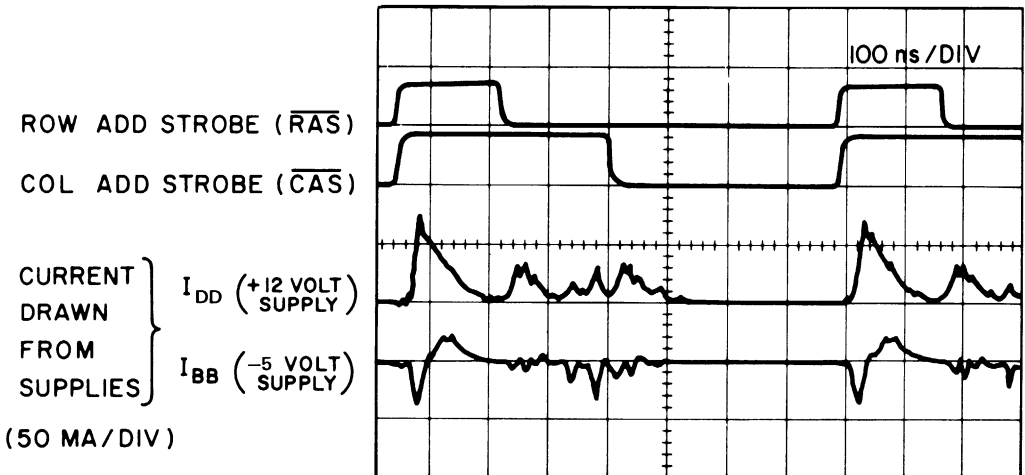
MOSTEK®

FEATURES

☐ Industry standard 16-pin DIP configuration (available in plastic (N) and ceramic (K) packages)

☐ All inputs are low capacitance and TTL compatible, except RAS (MOS level)

☐ Input latches for address, chip select and data in

☐ Inputs protected against static charge

☐ Three-state TTL compatible output, latched and valid into next cycle

☐ Proven reliability with high performance

Part Number	Access Time	Cycle Time	Max Power*
MK 4200-16	300 ns	425 ns	380 mW
MK 4200-11	350 ns	500 ns	300 mW

*Standby power for all parts < .6 mW

DESCRIPTION

The MK 4200 is a 4096 word by 1 bit MOS Random Access Memory circuit packaged in a standard 16-pin DIP on 0.3 inch centers. This package configuration is made possible by a unique multiplexing and latching technique for the address inputs. The use of the 16-pin DIP for the MK 4200 provides high system bit densities and is compatible with widely available automated testing and insertion equipment.

The MK 4200 is fabricated with MOSTEK's standard Self-Aligned, Poly-Interconnect, N-Channel (SPIN) process. The SPIN process allows the MK 4200 to be a highly manufacturable, state-of-the-art memory circuit that exhibits the reliability and performance standards necessary for today's (and tomorrow's) data processing applications. The MK 4200 employs a single transistor storage cell, utilizing a dynamic storage technique and dynamic control circuitry to achieve optimum performance with low power dissipation.

System oriented features incorporated within the MK 4200 include direct interfacing capability with TTL, 6 instead of 12 address lines to drive, on-chip registers which can eliminate the need for interface registers, input logic levels selected to optimize the noise immunity, and two chip select methods to allow the user to determine the speed/power characteristics of his memory system.

FUNCTIONAL DIAGRAM

PIN CONNECTIONS

PIN NAMES

A₀ - A₅	ADDRESS INPUTS	D_{IN}	DATA IN
$\overline{CAS}$	COLUMN ADDRESS STROBE	D_{OUT}	DATA OUT
$\overline{CS}$	CHIP SELECT	V_{BB}	POWER (−5V)
RAS	ROW ADDRESS STROBE	V_{CC}	POWER (+5V)
$\overline{WRITE}$	READ/WRITE INPUT	V_{DD}	POWER (+12V)
		V_{SS}	GROUND

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to V_{BB} .... −0.5V to + 25V
(V_{SS}−$V_{BB} \geqslant 4.5V$)
Operating temperature T_A (Ambient) .... 0°C to + 70°C
Storage temperature (Ceramic) ...... −65°C to + 150°C
Storage temperature (Plastic) .... −55°C to + 125°C
Power dissipation 1Watt
Data out current 50mA

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS [17]
($0°C \leqslant T_A \leqslant 70°C$)

	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{DD}	Supply Voltage	11.4	12.0	12.6	Volts	1
V_{CC}	Supply Voltage	V_{SS}	5.0	V_{DD}	Volts	1,2
V_{SS}	Supply Voltage	0	0	0	Volts	1
V_{BB}	Supply Voltage	−4.5	−5.0	−5.5	Volts	1
V_{IHC}	Logic 1 Voltage, $\overline{CAS}$, $\overline{WRITE}$	2.7	5.0	7.0	Volts	1,3
V_{IH}	Logic 1 Voltage, all inputs except RAS, $\overline{CAS}$, $\overline{WRITE}$	2.4	5.0	7.0	Volts	1,3
V_{IHR}	Logic 1 Voltage, RAS input	V_{DD}−1	12.0	V_{DD}+1	Volts	1
V_{IL}	Logic 0 Voltage, all inputs	−1.0	0	0.8	Volts	1,3

DC ELECTRICAL CHARACTERISTICS [17]
($0°C \leqslant T_A \leqslant 70°C$) ($V_{DD}$ = 12.0V ± 5%; V_{CC} = 5.0V ± 10%; V_{SS} = 0V; V_{BB} = −5.0V ± 10%)

	PARAMETER	MK 4200-16 MIN	MK 4200-16 MAX	MK 4200-11 MIN	MK 4200-11 MAX	UNITS	NOTES
I_{DD1}	Average V_{DD} Power Supply Current		30		25	mA	4
I_{CC}	V_{CC} Power Supply Current					mA	5
I_{BB}	Average V_{BB} Power Supply Current		75		75	μA	
I_{DD2}	Standby V_{DD} Power Supply Current		50		50	μA	7
I_{DD3}	Average V_{DD} Supply Current during "RAS - only" cycles		22		18	mA	4
$I_{I(L)}$	Input Leakage Current (any input)		5		5	μA	6
$I_{O(L)}$	Output Leakage Current		10		10	μA	7,8
V_{OH}	Output Logic 1 Voltage @ I_{OUT} = −5mA	2.4		2.4		Volts	2
V_{OL}	Output Logic 0 Voltage @ I_{OUT} = 2mA		0.4		0.4	Volts	

NOTES

1. All voltages referenced to V_{SS}. V_{BB} must be applied to and removed from the device within 5 seconds of V_{DD}.

2. Output voltage will swing from V_{SS} to V_{CC} if $V_{CC} \leqslant V_{DD}$ −4 volts. If $V_{CC} \geqslant V_{DD}$ −4 volts, the output will swing from V_{SS} to a voltage somewhat less than V_{DD}.

3. Device speed is not guaranteed at input voltages greater than TTL levels (0 to 5V).

4. Current is proportional to cycle rate; maximum current is measured at the fastest cycle rate.

5. I_{CC} depends upon output loading. The V_{CC} supply is connected to the output buffer only.

6. All device pins at 0 volts except V_{BB} which is at −5 volts and the pin under test which is at +10 volts.

7. Output is disabled (open-circuit); RAS = V_{IL} and $\overline{CAS}$ = V_{IHC}.

8. $0V \leqslant V_{OUT} \leqslant +10V$.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (10, 15, 17)
($0°C \leqslant T_A \leqslant 70°C$) ($V_{DD} = 12.0V \pm 5\%$, $V_{CC} = 5.0V \pm 10\%$, $V_{SS} = 0V$, $V_{BB} = -5.0V \pm 10\%$)

	PARAMETER	MK 4200-16 MIN	MK 4200-16 MAX	MK 4200-11 MIN	MK 4200-11 MAX	UNITS	NOTES
t_{RC}	Random Read or Write Cycle Time	425		500		nsec	11
t_{RAC}	Access time from Row Address Strobe		300		350	nsec	11,13
t_{CAC}	Access Time from Column Address Strobe		165		200	nsec	12,13
t_{OFF}	Output Buffer Turn-Off Delay	0	80	0	100	nsec	
t_{RP}	Row Address Strobe Precharge Time	125		150		nsec	
t_{RAS}	Row Address Strobe Pulse Width	300	10,000	350	10,000	nsec	
t_{RCL}	Row To Column Strobe Lead Time	80	135	100	150	nsec	14
t_{CAS}	Column Address Strobe Pulse Width	165		200		nsec	12
t_{AS}	Address Set-Up Time	0		0		nsec	
t_{AH}	Address Hold Time	80		100		nsec	
t_{CH}	Chip Select Hold Time	100		100		nsec	
t_T	Rise and Fall Times	3	50	3	50	nsec	15
t_{RCS}	Read Command Set-Up Time	0		0		nsec	
t_{RCH}	Read Command Hold Time	0		0		nsec	
t_{WCH}	Write Command Hold Time	130		150		nsec	
t_{WP}	Write Command Pulse Width	130		150		nsec	
t_{CRL}	Column to Row Strobe Lead Time	−50	+50	−50	+50	nsec	
t_{CWL}	Write Command to Column Strobe Lead Time	130		150		nsec	
t_{DS}	Data In Set-Up Time	0		0		nsec	16
t_{DH}	Data In Hold Time	130		150		nsec	16
t_{RFSH}	Refresh Period		2		2	msec	
t_{MOD}	Modify Time		10		10	μsec	
t_{DOH}	Data Out Hold Time	10		10		μsec	

<div style="writing-mode: vertical">4096 X 1-BIT DYN RAM</div>

NOTES Continued

9. Capacitance measured with Boonton Meter or effective capacitance calculated from the equation: $C = I \frac{\triangle t}{\triangle V}$ with current equal to a constant 20mA.

10. A C measurements assume t_T = 5ns.

11. Assumes that $t_{RCL} + t_T \leqslant t_{RCL}$ (max).

12. Assumes that $t_{RCL} + t_T \geqslant t_{RCL}$ (max).

13. Measured with a load circuit equivalent to 1 TTL load and C_L = 100pF.

14. Operation within the t_{RCL} (max) limit insures that t_{RAC} (max) can be met. t_{RCL} (max) is specified as a reference point only; if t_{RCL} is greater than the specified t_{RCL} (max) limit, then access time is controlled exclusively by t_{CAC} and t_{RAS}, t_{RAC} and t_{RCL} will be longer by the amount $t_{RCL} + t_T$ exceeds t_{RCL} (max).

15. V_{IHC} or V_{IHR} or V_{IH} and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IHC} or V_{IHR} or V_{IH} and V_{IL}.

16. These parameters are referenced to $\overline{CAS}$ leading edge in random write cycles and to $\overline{WRITE}$ leading edge in delayed write or read-modify-write cycles.

17. After the application of supply voltages or after extended periods of operation without clocks, the device must perform a minimum of one initialization cycles (any valid memory cycle containing both RAS and $\overline{CAS}$) prior to normal operation.

AC ELECTRICAL CHARACTERISTICS

$(0°C \leq T_A \leq +70°C)$ $(V_{DD} = 12.0V \pm 5\%, V_{CC} = 5.0V \pm 10\%, V_{SS} = 0V, V_{BB} = -5.0V \pm 10\%)$

	PARAMETER	TYP	MAX	UNITS	NOTES
C_{I1}	Input Capacitance ($A_0 - A_5$)	7	10	pF	9
C_{I2}	Input Capacitance (RAS, $\overline{CAS}$, D_{IN}, $\overline{WRITE}$, $\overline{CS}$)	5	7	pF	9
C_0	Output Capacitance (D_{OUT})	5	8	pF	7,9

TIMING WAVEFORMS

TIMING WAVEFORMS
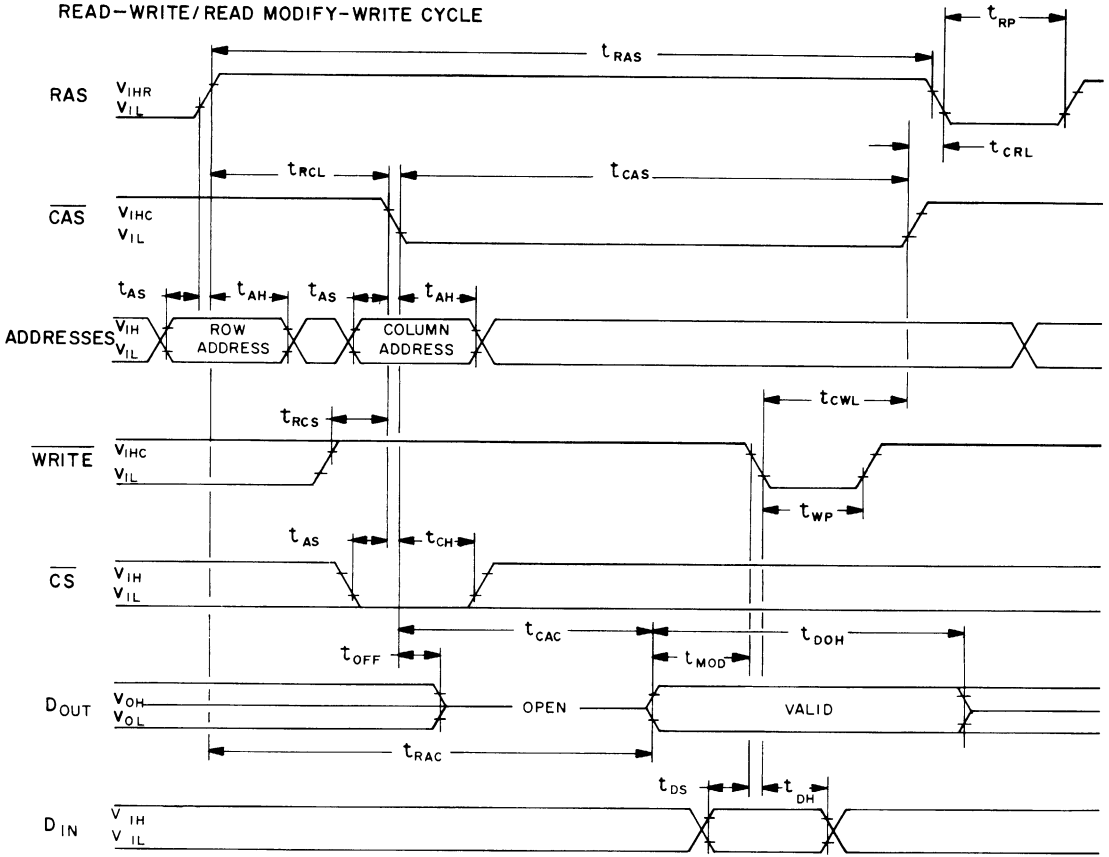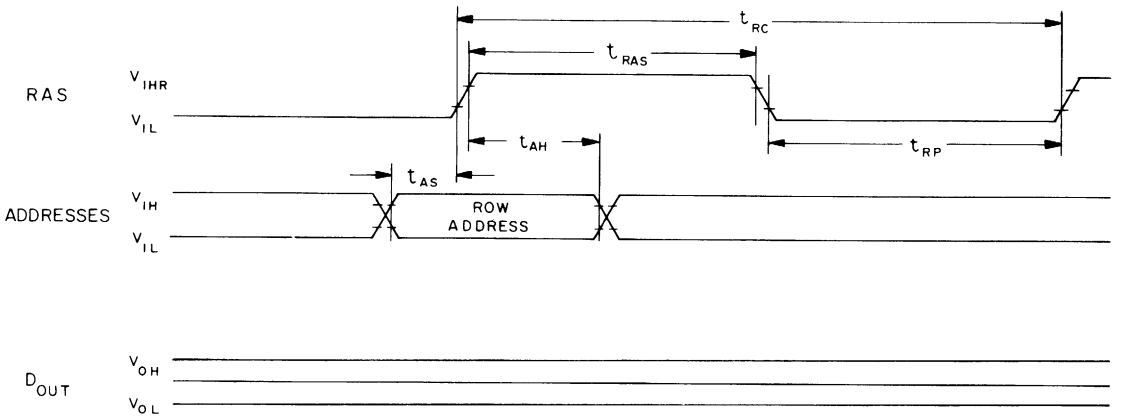
READ−WRITE/READ MODIFY−WRITE CYCLE

"RAS ONLY" REFRESH CYCLE

NOTE:

Prior to the first memory cycle following a period (beyond 2mS) of "RAS-only refresh, a memory cycle employing both RAS and $\overline{CAS}$ must be performed to insure proper device operation.

ADDRESSING

The 12 address bits required to decode one of the 4096 cell locations within the MK 4200 are multiplexed onto the 6 address inputs and latched into the on-chip address latches by externally applying a positive going MOS level clock and a negative going TTL level clock. The first clock, the Row Address Strobe (RAS), latches the 6 row address bits into the chip. The second clock, the Column Address Strobe (CAS), subsequently latches the 6 column address bits plus Chip Select (CS) into the chip. (Note that since the Chip Select signal is not required until CAS time, which is well into the memory cycle its decoding time does not add to system access or cycle time). Each of these signals, RAS and CAS, triggers a sequence of events which are controlled by different delayed internal clocks. The two clock chains are linked together logically in such a way that the address multiplexing operation is done outside of the critical path timing sequence for read data access. The later events in the CAS clock sequence are inhibited until the occurrence of a delayed signal derived from the RAS clock chain. This "gated CAS" feature allows the CAS clock to be externally activated as soon as the Row Address Hold Time specification (t$_{AH}$) has been satisfied and the 6 address inputs have been changed from Row address to Column address information.

Note that CAS can be activated at any time after t$_{AH}$ and it will have no effect on the worst case data access time (t$_{RAC}$) up to the point in time when the delayed row clock no longer inhibits the remaining sequence of column clocks. Two timing end points result from the internal gating of CAS which are called t$_{RCL}$ (min) and t$_{RCL}$ (max). No data storage or reading errors will result if CAS is applied to the MK 4200 at a point in time beyond the t$_{RCL}$ (max) limit. However, access time will then be determined exclusively by the access time from CAS (t$_{CAC}$) rather than from RAS (t$_{RAC}$), and access time from RAS will be lengthened by the amount that t$_{RCL}$ exceeds the t$_{RCL}$ (max) limit.

INPUT LEVELS

All inputs to the MK 4200 except address strobe (RAS) are TTL compatible. The RAS input has been specially designed so that very little steady state (DC) power is dissipated by the MK 4200 while in standby operation. In doing this, the RAS input requires a high level signal to activate the chip. The RAS input driver must be able to change the capacitance load of the RAS input from within 8 volt at V$_{SS}$ (0V) to within 1 volt of V$_{DD}$ (+12).

DATA INPUT/OUTPUT

Data to be written into a selected cell is latched into an on-chip register by a combination of WRITE and CAS while RAS is active. The later of the signals (WRITE or CAS) to make its negative transition is the strobe for the Data In register. This permits several options in the write cycle timing. In a write cycle, if the WRITE input is brought low prior to CAS, the Data In is strobed by CAS, and the set-up and hold times are referenced to CAS. If the data input is not available at CAS time or if it is desired that the cycle be a read-write or read-modify-write cycle, the WRITE signal must be delayed until after CAS. In this "delayed write cycle" the data input set-up and hold times are referenced to the

negative edge of WRITE rather than to CAS.

(To illustrate this feature, Data In is referenced to WRITE in the timing diagram depicting the read-modify-write cycle while the "early write" cycle diagram shows Data In referenced to CAS). Note that if the chip is unselected (CS high at CAS time) WRITE commands are not executed and, consequently, data stored in the memory is unaffected.

Data is retrieved from the memory in a read cycle by maintaining WRITE in the inactive or high state throughout the portion of the memory cyle in which CAS is active. Data read from the selected cell will be available at the output within the specified access time.

DATA OUTPUT LATCH

Any change in the condition of the Data Out Latch is initiated by the CAS signal. The output buffer is not affected by memory (refresh) cycles in which only the RAS signal is applied to the MK 4200. Whenever CAS makes a negative transition, the output will go unconditionally open-circuited, independent of the state of any other input to the chip. If the cycle in progress is a read, read-modify-write, or a delayed write cycle and the chip is selected, then the output latch and buffer will again go active and at access time will contain the data read from the selected cell. This output data is the same polarity (not inverted) as the input data. If the cycle in progress is a write cycle (WRITE active low before CAS goes low) and the chip is selected, then at access time the output latch and buffer will contain a logic 1. Once having gone active, the output will remain valid until the MK 4200 receives the next CAS negative edge. Intervening refresh cycles in which a RAS is received (but no CAS) will not cause valid data to be affected. Conversely, the output will assume the open-circuit state during any cycle in which the MK 4200 receives a CAS but no RAS signal (regardless of the state of any other inputs). The output will also assume the open-circuit state in normal cycles (in which both RAS and CAS signals occur) if the chip is unselected.

The three-state data output buffer presents the data output pin with a low impedance to V$_{CC}$ for a logic 1 and a low impedance to V$_{SS}$ for a logic 0. The effective resistance to V$_{CC}$ (logic 1 state) is 500Ω maximum and 150Ω typically. The resistance to V$_{SS}$ (logic 0 state) is 200Ω maximum and 100Ω typically. The separate V$_{CC}$ pin allows the output buffer to be powered from the supply voltage of the logic to which the chip is interfaced. During battery standby operation, the V$_{CC}$ pin may have power removed without affecting the MK 4200 refresh operation. This allows all system logic except the RAS/CAS timing circuitry and the refresh address logic to be turned off during battery standby to conserve power.

REFRESH

Refresh of the dynamic cell matrix is accomplished by performing a memory cycle at each of the 64 row addresses within each 2 millisecond time interval. Any cycle in which a RAS signal occurs accomplishes a refresh operation. A read cycle will refresh the selected row, regardless of the Chip Select (CS) input. A write or read-modify-write cycle also refreshes the selected row, but the chip should be unselected to

prevent writing data into the selected cell.

For standby operation, a "RAS-only" cycle can be employed to refresh the MK 4200. However, if "RAS-only" refresh cycles (where RAS is the only signal applied to the chip) are continued for extended periods, the output buffer may eventually lose proper data and go open-circuit. Prior to the first memory cycle following a period (beyond 2ms) of "RAS-only" refresh, a memory cycle employing both RAS and CAS must be performed to precharge the internal circuitry. This "dummy cycle" allows the output buffer to regain activity and enables the device to perform a read or write cycle upon command.

POWER DISSIPATION/STANDBY MODE

Most of the circuitry used in the MK 4200 is dynamic and most of the power drawn is the result of an address strobe edge. Because the power is not drawn during the whole time the strobe is active, the dynamic power is a function of operating frequency rather than active duty cycle. Typically, the power is 120 mW at a 1 μsec cycle rate for the MK 4200 with a maximum power of less than 450 mW at 375 nsec cycle time. To minimize the overall system power, the Row Address Strobe (RAS) should be decoded and supplied to only the selected chips. The CAS must be supplied to all chips (to turn off the unselected output). Those chips that did not receive a RAS, however, will not dissipate any power on the CAS edges, except for that required to turn off the outputs. If the RAS signal is decoded and supplied only to the selected chips, then the Chip Select (CS) input of all chips can be at a logic 0. The chips that receive a CAS but no RAS will be unselected (output open-circuited) regardless of the Chip Select input. For refresh cycles, however, either the CS input of all chips must be high or the CAS input must be held high to prevent several "wire-ORed" outputs from turning on with opposing force.

The current waveforms for the current drawn from the V_{DD} and V_{BB} supplies are shown in Figure A. Since the current is pulsed, proper power distribution and bypassing techniques are required to maintain system power supply noise levels at an acceptable level. Low inductance supply lines for V_{DD} and V_{SS} are desirable. One 0.01 microfarad, low inductance, bypass capacitor per two MK 4200 devices and one 6.8 microfarad electrolytic capacitor per eight MK 4200 devices on each of the V_{DD} and V_{BB} supply lines is desirable.

POWER—UP

Under normal operating conditions the MK 4200 requires no particular power-up sequence. However, in order to achieve the most reliable performance from the MK 4200, proper consideration should be given to the V_{BB}/V_{DD} power supply relationship. The V_{BB} supply is an extremely important "protective voltage" since it performs two essential functions within the device. It establishes proper junction isolation and sets field-effect thresholds, both thin field and thick field. Misapplication of V_{BB} or device operation without the V_{BB} supply can affect long term device reliability. For optimum reliability performance from the MK 4200, it is suggested that measures be taken to not have V_{DD} (+12V) applied to the device for over five (5) seconds without the application of V_{BB} (−5V).

After power is applied to the device, the MK 4200 requires at least one memory cycle (RAS/CAS) before proper device operation is achieved. A normal 64 cycle refresh with both RAS and CAS is adequate for this purpose.

POWER SUPPLY CURRENT WAVEFORMS
Figure A

ROW ADD STROBE (RAS)

COL ADD STROBE (CAS)

CURRENT DRAWN FROM SUPPLIES $\Big\}$ I_{DD} (+12 VOLT SUPPLY) I_{BB} (-5 VOLT SUPPLY)

(50 MA/DIV)

100 ns/DIV
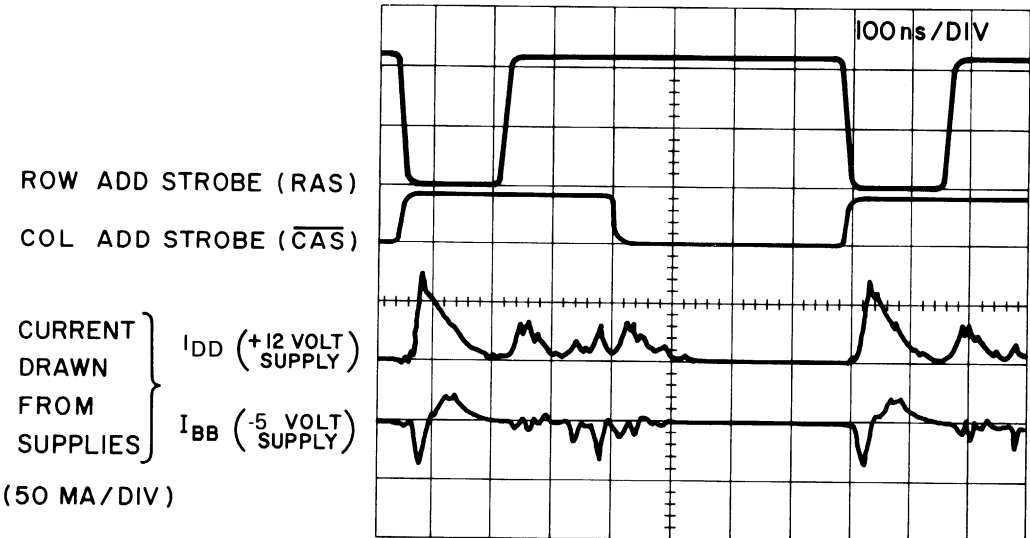
MOSTEK®

16,384 x 1-BIT DYNAMIC RAM

MK4116(P)-2/3

FEATURES

- □ Recognized industry standard 16-pin configuration from MOSTEK

- □ 150ns access time, 320ns cycle (MK 4116-2)
  200ns access time, 375ns cycle (MK 4116-3)

- □ ± 10% tolerance on all power supplies (+12V,±5V)

- □ Low power: 462mW active, 20mW standby (max)

- □ Output data controlled by $\overline{CAS}$ and unlatched at end of cycle to allow two dimensional chip selection and extended page boundary

- □ Common I/O capability using "early write" operation

- □ Read-Modify-Write, $\overline{RAS}$-only refresh, and Page-mode capability

- □ All inputs TTL compatible, low capacitance, and protected against static charge

- □ 128 refresh cycles (2msec refresh interval)

- □ ECL compatible on V_{BB} power supply (-5.7V)

DESCRIPTION

The MK 4116 is a new generation MOS dynamic random access memory circuit organized as 16,384 words by 1 bit. As a state-of-the-art MOS memory device, the MK 4116 (16K RAM) incorporates advanced circuit techniques designed to provide wide operating margins, both internally and to the system user, while achieving performance levels in speed and power previously seen only in MOSTEK's high performance MK 4027 (4K RAM).

The technology used to fabricate the MK 4116 is MOSTEK's double-poly, N-channel silicon gate, POLY II ® process. This process, coupled with the use of a single transistor dynamic storage cell, provides the maximum possible circuit density and reliability, while maintaining high performance capability. The use of dynamic circuitry through-

out, including sense amplifiers, assures that power dissipation is minimized without any sacrifice in speed or operating margin. These factors combine to make the MK 4116 a truly superior RAM product.

Multiplexed address inputs (a feature pioneered by MOSTEK for its 4K RAMS) permits the MK 4116 to be packaged in a standard 16-pin DIP. This recognized industry standard package configuration, while compatible with widely available automated testing and insertion equipment, provides highest possible system bit densities and simplifies system upgrade from 4K to 16K RAMs for new generation applications. Non-critical clock timing requirements allow use of the multiplexing technique while maintaining high performance.

FUNCTIONAL DIAGRAM

PIN CONNECTIONS

PIN NAMES

A_0-A_6	ADDRESS INPUTS
$\overline{CAS}$	COLUMN ADDRESS STROBE
D_{IN}	DATA IN
D_{OUT}	DATA OUT
$\overline{RAS}$	ROW ADDRESS STROBE
$\overline{WRITE}$	READ/WRITE INPUT
V_{BB}	POWER (—5V)
V_{CC}	POWER (+5V)
V_{DD}	POWER (+12V)
V_{SS}	GROUND

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to V_{BB} . . . . −0.5V to +20V
Voltage on V_{DD}, V_{CC} supplies relative to V_{SS} . . . . −1.0V to +15.0V
V_{BB}−V_{SS} (V_{DD}−V_{SS} >0V) 0V
Operating temperature, T_A (Ambient) . . . . 0°C to + 70°C
Storage temperature (Ambient). . . . . −65°C to + 150°C
Short circuit output current 50mA
Power dissipation . . . . 1 Watt

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS[6]
(0°C ≤ T_A ≤ 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{DD}	10.8	12.0	13.2	Volts	2
	V_{CC}	4.5	5.0	5.5	Volts	2,3
	V_{SS}	0	0	0	Volts	2
	V_{BB}	−4.5	−5.0	−5.7	Volts	2
Input High (Logic 1) Voltage, $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	V_{IHC}	2.7	–	7.0	Volts	2
Input High (Logic 1) Voltage, all inputs except $\overline{RAS}$, $\overline{CAS}$ $\overline{WRITE}$	V_{IH}	2.4	–	7.0	Volts	2
Input Low (Logic 0) Voltage, all inputs	V_{IL}	−1.0	–	.8	Volts	2

DC ELECTRICAL CHARACTERISTICS
(0°C ≤ T_A ≤ 70°C) (V_{DD} = 12.0V ± 10%; V_{CC} = 5.0V ± 10%; −5.7V ≤ V_{BB} ≤ −4.5V; V_{SS} = 0V)

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
OPERATING CURRENT Average power supply operating current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = t_{RC} Min)	I_{DD1}		35	mA	4
	I_{CC1}				5
	I_{BB1}		200	μA	
STANDBY CURRENT Power supply standby current ($\overline{RAS}$ = V_{IHC}, D_{OUT} = High Impedance)	I_{DD2}		1.5	mA	
	I_{CC2}	−10	10	μA	
	I_{BB2}		100	μA	
REFRESH CURRENT Average power supply current, refresh mode ($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IHC}; t_{RC} = t_{RC} Min)	I_{DD3}		27	mA	4
	I_{CC3}	−10	10	μA	
	I_{BB3}		200	μA	
PAGE MODE CURRENT Average power supply current, page-mode operation ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling; t_{PC} = t_{PC} Min)	I_{DD4}		27	mA	4
	I_{CC4}				5
	I_{BB4}		200	μA	
INPUT LEAKAGE Input leakage current, any input (V_{BB} = −5V, 0V ≤ V_{IN} ≤ +7.0V, all other pins not under test = 0 volts)	$I_{I(L)}$	−10	10	μA	
OUTPUT LEAKAGE Output leakage current (D_{OUT} is disabled, 0V ≤ V_{OUT} ≤ +5.5V)	$I_{0(L)}$	−10	10	μA	
OUTPUT LEVELS Output high (Logic 1) voltage (I_{OUT} = −5mA)	V_{OH}	2.4		Volts	3
Output low (Logic 0) voltage (I_{OUT} = 4.2 mA)	V_{OL}		0.4	Volts	

NOTES:

1. T_A is specified here for operation at frequencies to t_{RC} ≥ t_{RC} (min). Operation at higher cycle rates with reduced ambient temperatures and higher power dissipation is permissible, however, provided AC operating parameters are met. See figure 1 for derating curve.

2. All voltages referenced to V_{SS}.

3. Output voltage will swing from V_{SS} to V_{CC} when activated with no current loading. For purposes of maintaining data in standby mode, V_{CC} may be reduced to V_{SS} without affecting refresh operations or data retention. However, the V_{OH} (min) specification is not guaranteed in this mode.

4. I_{DD1}, I_{DD3}, and I_{DD4} depend on cycle rate. See figures 2,3, and 4 for I_{DD} limits at other cycle rates.

5. I_{CC1} and I_{CC4} depend upon output loading. During readout of high level data V_{CC} is connected through a low impedance (135 Ω typ) to data out. At all other times I_{CC} consists of leakage currents only.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (6,7,8)
$(0 \,^\circ\text{C} \leqslant T_A \leqslant 70\,^\circ\text{C})^1 (V_{DD} = 12.0V \pm 10\%; V_{CC} = 5.0V \pm 10\%, V_{SS} = 0V, -5.7V \leqslant V_{BB} \leqslant -4.5V)$

PARAMETER	SYMBOL	MK 4116-2 MIN	MK 4116-2 MAX	MK 4116-3 MIN	MK 4116-3 MAX	UNITS	NOTES
Random read or write cycle time	tRC	320		375		ns	9
Read-write cycle time	tRWC	320		375		ns	9
Read modify write cycle time	tRMW	320		405		ns	9
Page mode cycle time	tPC	170		225		ns	9
Access time from RAS	tRAC		150		200	ns	10,12
Access time from CAS	tCAC		100		135	ns	11,12
Output buffer turn-off delay	tOFF	0	40	0	50	ns	13
Transition time (rise and fall)	tT	3	35	3	50	ns	8
RAS precharge time	tRP	100		120		ns	
RAS pulse width	tRAS	150	10,000	200	10,000	ns	
RAS hold time	tRSH	100		135		ns	
CAS hold time	tCSH	150		200		ns	
CAS pulse width	tCAS	100		135		ns	
RAS to CAS delay time	tRCD	20	50	25	65	ns	14
CAS to RAS precharge time	tCRP	−20		−20		ns	
Row Address set-up time	tASR	0		0		ns	
Row Address hold time	tRAH	20		25		ns	
Column Address set-up time	tASC	−10		−10		ns	
Column Address hold time	tCAH	45		55		ns	
Column Address hold time referenced to RAS	tAR	95		120		ns	
Read command set-up time	tRCS	0		0		ns	
Read command hold time	tRCH	0		0		ns	
Write command hold time	tWCH	45		55		ns	
Write command hold time referenced to RAS	tWCR	95		120		ns	
Write command pulse width	tWP	45		55		ns	
Write command to RAS lead time	tRWL	50		70		ns	
Write command to CAS lead time	tCWL	50		70		ns	
Data-in set-up time	tDS	0		0		ns	15
Data-in hold time	tDH	45		55		ns	15
Data-in hold time referenced to RAS	tDHR	95		120		ns	
CAS precharge time (for page-mode cycle only)	tCP	60		80		ns	
Refresh period	tREF		2		2	ms	
WRITE command set-up time	tWCS	−20		−20		ns	16
CAS to WRITE delay	tCWD	60		80		ns	16
RAS to WRITE delay	tRWD	110		145		ns	16

NOTES (Continued)

6. Several cycles are required after power-up before proper device operation is achieved. Any 8 cycles which perform refresh are adequate for this purpose.
7. AC measurements assume tT = 5ns.
8. VIHC (min) or VIH (min) and VIL (max) are reference levels for measuring timing of input signals. Also, transition times are measured between VIHC or VIH and VIL.
9. The specifications for tRC (min) tRMW (min) and tRWC (min) are used only to indicate cycle time at which proper operation over the full temperature range (0 C ≤ TA ≤ 70 C) is assured.
10. Assumes that tRCD ≤ tRCD (max). If tRCD is greater than the maximum recommended value shown in this table, tRAC will increase by the amount that tRCD exceeds the value shown.
11. Assumes that tRCD ≥ tRCD (max).
12. Measured with a load equivalent to 2 TTL loads and 100pF.
13. tOFF (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
14. Operation within the tRCD (max) limit insures that tRAC (max) can be met. tRCD (max) is specified as a reference point only; if tRCD is greater than the specified tRCD (max) limit, then access time is controlled exclusively by tCAC.
15. These parameters are referenced to CAS leading edge in early write cycles and to WRITE leading edge in delayed write or read-modify-write cycles.
16. tWCS, tCWD and tRWD are restrictive operating parameters in read write and read modify write cycles only. If tWCS ≥ tWCS (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; If tCWD ≥ tCWD (min) and tRWD ≥ tRWD (min), the cycle is a read-write cycle and the data out will contain data read from the selected cell; If neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.
17. Effective capacitance calculated from the equation $C = I \frac{\Delta t}{\Delta V}$ with ΔV - 3 volts and power supplies at nominal levels.
18. CAS = VIHC to disable DOUT.

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AC ELECTRICAL CHARACTERISTICS

$(0°C \leqslant T_A \leqslant 70°C)$ $(V_{DD} = 12.0V \pm 10\%; V_{SS} = 0V; -5.7V \leqslant V_{BB} \leqslant -4.5V)$

PARAMETER	SYMBOL	TYP	MAX	UNITS	NOTES
Input Capacitance (A_0-A_6), D_{IN}	C_{I1}	4	5	pF	17
Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	C_{I2}	8	10	pF	17
Output Capacitance (D_{OUT})	C_0	5	7	pF	17, 18

Fig. 1 Maximum ambient temperature versus cycle rate for extended frequency operation. T_A (max) for operation at cycling rates greater than 2.66 MHz $(t_{CYC} < 375ns)$ is determined by T_A (max) $°C = 70 - 9.0 \times$ (cycle rate MHz -2.66) for -3. T_A (max) $°C = 70 - 9.0 \times$ cycle rate MHz $-3.125MHz$) for -2 only.
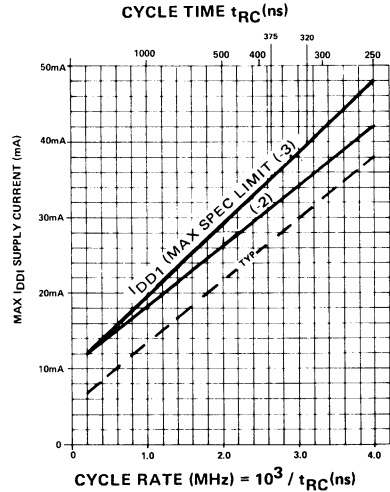
Fig. 2 Maximum I_{DD1} versus cycle rate for device operation at extended frequencies. I_{DD1} (max) curve is defined by the equation:

I_{DD1} (max) mA = 10 + 9.4 × cycle rate [MHz] for -3
I_{DD1} (max) mA = 10 + 8.0 × cycle rate [MHz] for -2
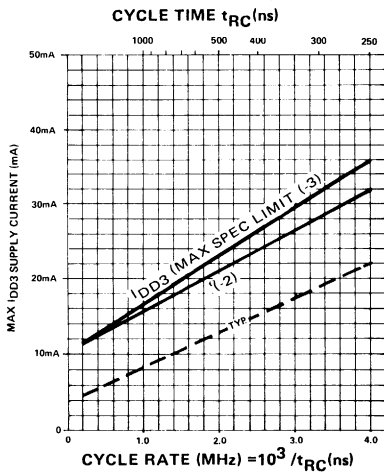
Fig. 3 Maximum I_{DD3} versus cycle rate for device operation at extended frequencies. I_{DD3} (max) curve is defined by the equation:

I_{DD3}(max) mA = 10 + 6.5 × cycle rate [MHz] for -3
I_{DD3}(max) mA = 10 + 5.5 × cycle rate [MHz] for -2
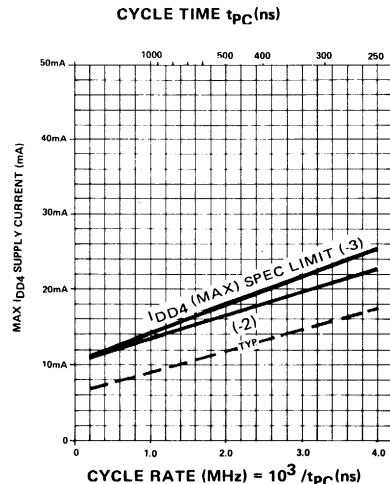
Fig. 4 Maximum I_{DD4} versus cycle rate for device operation in page mode. I_{DD4} (max) curve is defined by the equation:

I_{DD4} (max) mA = 10 + 3.75 × cycle rate [MHz] for -3
I_{DD4} (max) mA = 10 + 3.2 × cycle rate [MHz] for -2

READ CYCLE
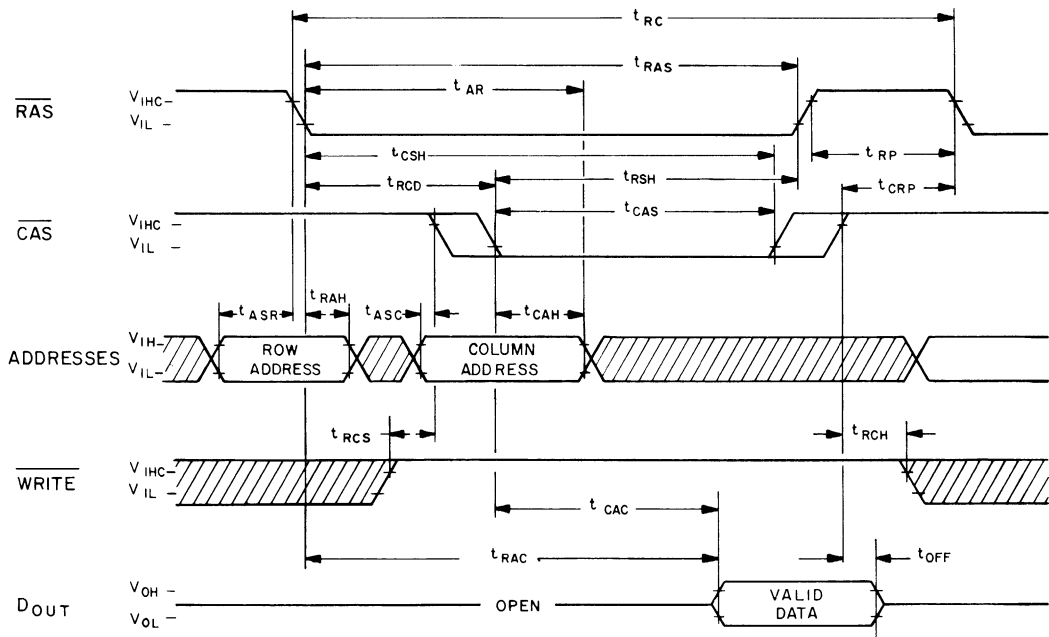
WRITE CYCLE (EARLY WRITE)
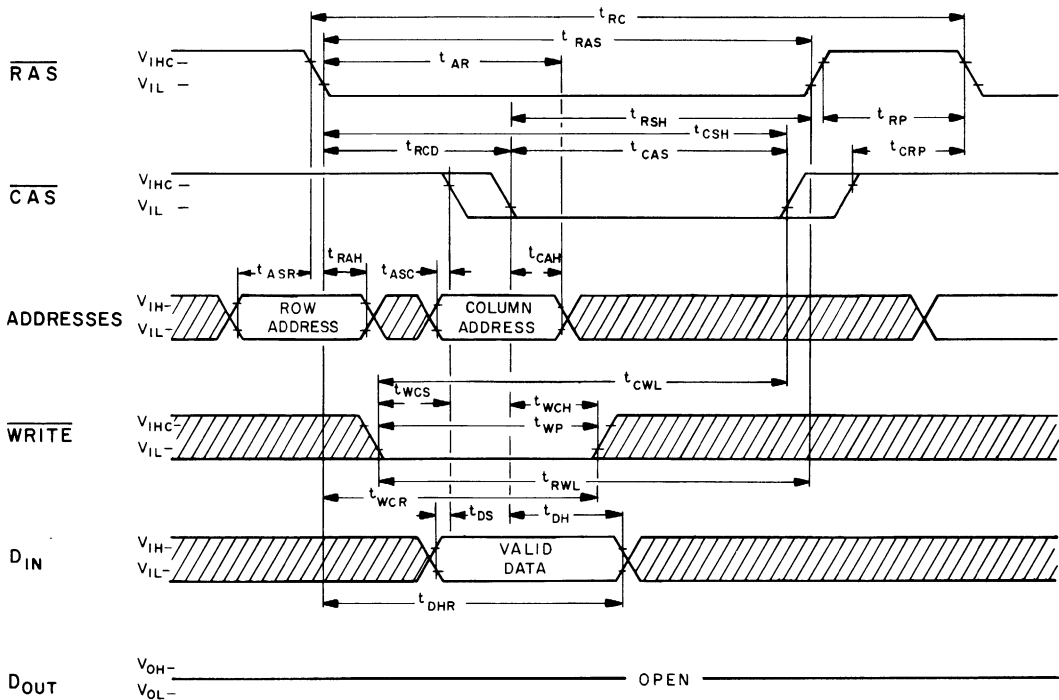
READ–WRITE/READ–MODIFY–WRITE CYCLE
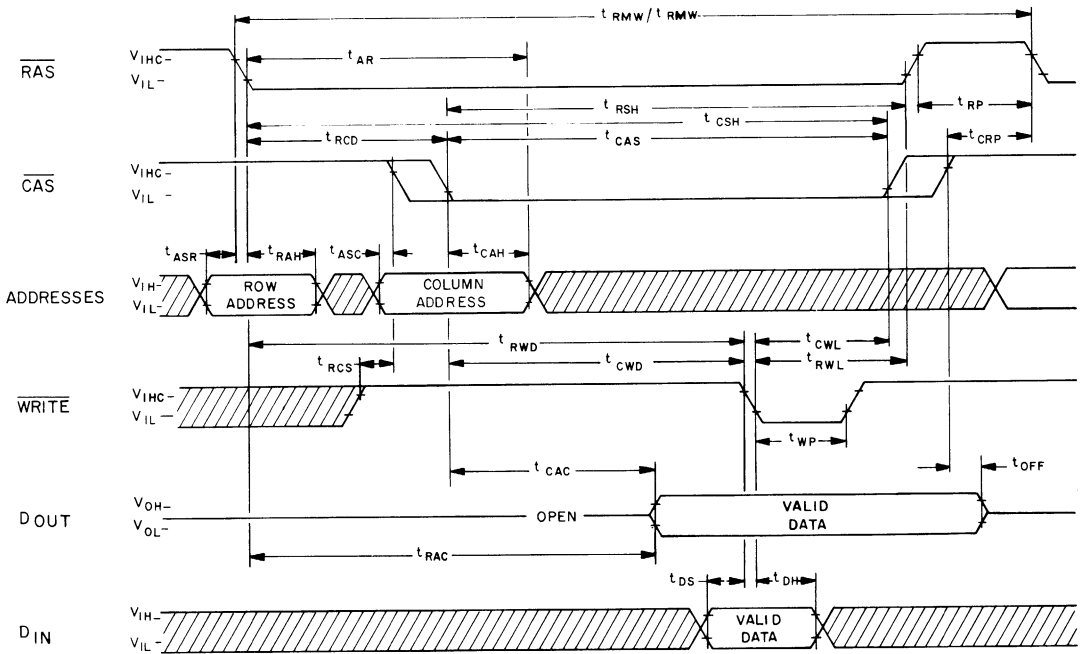
"RAS–ONLY" REFRESH CYCLE

NOTE: $\overline{CAS}$ = V$_{IHC}$, $\overline{WRITE}$ = Don't Care
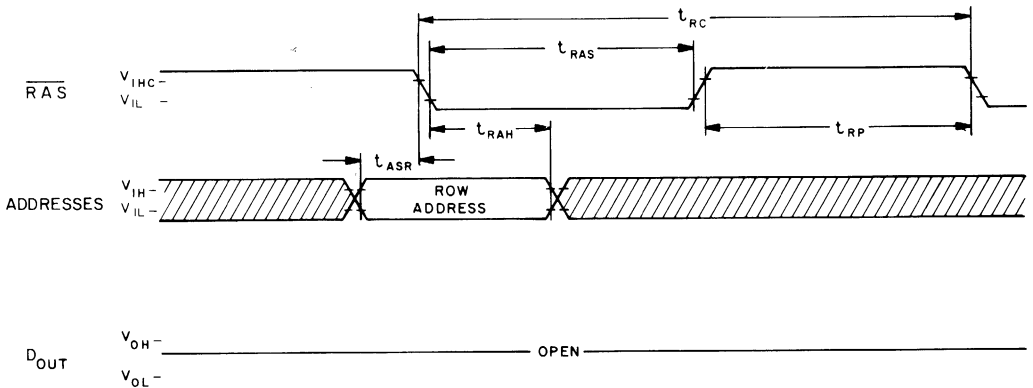
PAGE MODE READ CYCLE

PAGE MODE WRITE CYCLE

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DESCRIPTION (continued)

System oriented features include ± 10% tolerance on all power supplies, direct interfacing capability with high performance logic families such as Schottky TTL, maximum input noise immunity to minimize "false triggering" of the inputs (a common cause of soft errors), on-chip address and data registers which eliminate the need for interface registers, and two chip select methods to allow the user to determine the appropriate speed/power characteristics of his memory system. The MK 4116 also incorporates several flexible timing/operating modes. In addition to the usual read, write, and read-modify-write cycles, the MK 4116 is capable of delayed write cycles, page-mode operation and $\overline{RAS}$-only refresh. Proper control of the clock inputs($\overline{RAS}$, $\overline{CAS}$ and $\overline{WRITE}$) allows common I/O capability, two dimensional chip selection, and extended page boundaries (when operating in page mode).

ADDRESSING

The 14 address bits required to decode 1 of the 16,384 cell locations within the MK 4116 are multiplexed onto the 7 address inputs and latched into the on-chip address latches by externally applying two negative going TTL-level clocks. The first clock, the Row Address Strobe ($\overline{RAS}$), latches the 7 row address bits into the chip. The second clock, the Column Address Strobe ($\overline{CAS}$), subsequently latches the 7 column address bits into the chip. Each of these signals, $\overline{RAS}$ and $\overline{CAS}$, triggers a sequence of events which are controlled by different delayed internal clocks. The two clock chains are linked together logically in such a way that the address multiplexing operation is done outside of the critical path timing sequence for read data access. The later events in the $\overline{CAS}$ clock sequence are inhibited until the occurence of a delayed signal derived from the $\overline{RAS}$ clock chain. This "gated $\overline{CAS}$" feature allows the $\overline{CAS}$ clock to be externally activated as soon as the Row Address Hold Time specification (t_{RAH}) has been satisfied and the address inputs have been changed from Row address to Column address information.

Note that $\overline{CAS}$ can be activated at any time after t_{RAH} and it will have no effect on the worst case data access time (t_{RAC}) up to the point in time when the delayed row clock no longer inhibits the remaining sequence of column clocks. Two timing endpoints result from the internal gating of $\overline{CAS}$ which are called t_{RCD} (min) and t_{RCD} (max). No data storage or reading errors will result if $\overline{CAS}$ is applied to the MK 4116 at a point in time beyond the t_{RCD} (max) limit. However, access time will then be determined exclusively by the access time from $\overline{CAS}$ (t_{CAC}) rather than from $\overline{RAS}$ (t_{RAC}), and access time from $\overline{RAS}$ will be lengthened by the amount that t_{RCD} exceeds the t_{RCD} (max) limit.

DATA INPUT/OUTPUT

Data to be written into a selected cell is latched into an on-chip register by a combination of $\overline{WRITE}$ and $\overline{CAS}$ while $\overline{RAS}$ is active. The later of the signals ($\overline{WRITE}$ or $\overline{CAS}$) to make its negative transition is the strobe for the Data In (D_{IN}) register. This permits several options in the write cycle timing. In a write cycle, if the $\overline{WRITE}$ input is brought low (active)

prior to $\overline{CAS}$, the D_{IN} is strobed by $\overline{CAS}$, and the set-up and hold times are referenced to $\overline{CAS}$. If the input data is not available at $\overline{CAS}$ time or if it is desired that the cycle be a read-write cycle, the $\overline{WRITE}$ signal will be delayed until after $\overline{CAS}$ has made its negative transition. In this "delayed write cycle" the data input set-up and hold times are referenced to the negative edge of $\overline{WRITE}$ rather than $\overline{CAS}$. (To illustrate this feature, D_{IN} is referenced to $\overline{WRITE}$ in the timing diagrams depicting the read-write and page-mode write cycles while the "early write" cycle diagram shows D_{IN} referenced to $\overline{CAS}$).

Data is retrieved from the memory in a read cycle by maintaining $\overline{WRITE}$ in the inactive or high state throughout the portion of the memory cycle in which $\overline{CAS}$ is active (low). Data read from the selected cell will be available at the output within the specified access time.

DATA OUTPUT CONTROL

The normal condition of the Data Output (D_{OUT}) of the MK 4116 is the high impedance (open-circuit) state. That is to say, anytime $\overline{CAS}$ is at a high level, the D_{OUT} pin will be floating. The only time the output will turn on and contain either a logic 0 or logic 1 is at access time during a read cycle. D_{OUT} will remain valid from access time until $\overline{CAS}$ is taken back to the inactive (high level) condition.

If the memory cycle in progress is a read, read-modify write, or a delayed write cycle, then the data output will go from the high impedance state to the active condition, and at access time will contain the data read from the selected cell. This output data is the same polarity (not inverted) as the input data. Once having gone active, the output will remain valid until $\overline{CAS}$ is taken to the precharge (logic 1) state, whether or not $\overline{RAS}$ goes into precharge.

If the cycle in progress is an "early-write" cycle ($\overline{WRITE}$ active before $\overline{CAS}$ goes active), then the output pin will maintain the high impedance state throughout the entire cycle. Note that with this type of output configuration, the user is given full control of the D_{OUT} pin simply by controlling the placement of $\overline{WRITE}$ command during a write cycle, and the pulse width of the Column Address Strobe during read operations. Note also that even though data is not latched at the output, data can remain valid from access time until the beginning of a subsequent cycle without paying any penalty in overall memory cycle time (stretching the cycle).

This type of output operation results in some very significant system implications.

Common I/O Operation – If all write operations are handled in the "early write" mode, then D_{IN} can be connected directly to D_{OUT} for a common I/O data bus.

Data Output Control – D_{OUT} will remain valid during a read cycle from t_{CAC} until $\overline{CAS}$ goes back to a high level (precharge), allowing data to be valid from one cycle up until a new memory cycle begins with no penalty in cycle time. This also makes the $\overline{RAS}/\overline{CAS}$ clock timing relationship very flexible.

Two Methods of Chip Selection – Since D_{OUT}

is not latched, $\overline{CAS}$ is not required to turn off the outputs of unselected memory devices in a matrix. This means that both $\overline{CAS}$ and/or $\overline{RAS}$ can be decoded for chip selection. If both $\overline{RAS}$ and $\overline{CAS}$ are decoded, then a two dimensional (X,Y) chip select array can be realized.

Extended Page Boundary — Page-mode operation allows for successive memory cycles at multiple column locations of the same row address. By decoding $\overline{CAS}$ as a page cycle select signal, the page boundary can be extended beyond the 128 column locations in a single chip. (See page-mode operation).

OUTPUT INTERFACE CHARACTERISTICS

The three state data output buffer presents the data output pin with a low impedance to V_{CC} for a logic 1 and a low impedance to V_{SS} for a logic 0. The effective resistance to V_{CC} (logic 1 state) is 420 Ω maximum and 135Ω typically. The resistance to V_{SS} (logic 0 state) is 95 Ω maximum and 35 Ω typically. The separate V_{CC} pin allows the output buffer to be powered from the supply voltage of the logic to which the chip is interfaced. During battery standby operation, the V_{CC} pin may have power removed without affecting the MK 4116 refresh operation. This allows all system logic except the $\overline{RAS}$ timing circuitry and the refresh address logic to be turned off during battery standby to conserve power.

PAGE MODE OPERATION

The "Page Mode" feature of the MK 4116 allows for successive memory operations at multiple column locations of the same row address with increased speed without an increase in power. This is done by strobing the row address into the chip and maintaining the $\overline{RAS}$ signal at a logic 0 throughout all successive memory cycles in which the row address is common. This "page-mode" of operation will not dissipate the power associated with the negative going edge of $\overline{RAS}$. Also, the time required for strobing in a new row address is eliminated, thereby decreasing the access and cycle times.

The page boundary of a single MK 4116 is limited to the 128 column locations determined by all combinations of the 7 column address bits. However, in system applications which utilize more than 16,384 data words, (more than one 16K memory block), the page boundary can be extended by using $\overline{CAS}$ rather than $\overline{RAS}$ as the chip select signal. $\overline{RAS}$ is applied to all devices to latch the row address into each device and then $\overline{CAS}$ is decoded and serves as a page cycle select signal. Only those devices which receive both $\overline{RAS}$ and $\overline{CAS}$ signals will execute a read or write cycle.

REFRESH

Refresh of the dynamic cell matrix is accomplished by performing a memory cycle at each of the 128 row addresses within each 2 millisecond time interval. Although any normal memory cycle will perform the refresh operation, this function is most easily accomplished with "$\overline{RAS}$-only" cycles. $\overline{RAS}$-only refresh results in a substantial reduction in operating power. This reduction in power is reflected in the I_{DD3} specification.

POWER CONSIDERATIONS

Most of the circuitry used in the MK 4116 is dynamic and most of the power drawn is the result of an address strobe edge. Consequently, the dynamic power is primarily a function of operating frequency rather than active duty cycle (refer to the MK 4116 current waveforms in figure 5). This current characteristic of the MK 4116 precludes inadvertent burn out of the device in the event that the clock inputs become shorted to ground due to system malfunction.

Although no particular power supply noise restriction exists other than the supply voltages remain within the specified tolerance limits, adequate decoupling should be provided to suppress high frequency noise resulting from the transient current of the device. This insures optimum system performance and reliability. Bulk capacitance requirements are minimal since the MK 4116 draws very little steady state (DC) current.

In system applications requiring lower power dissipation, the operating frequency (cycle rate) of the MK 4116 can be reduced and the (guaranteed maximum) average power dissipation of the device will be lowered in accordance with the I_{DD1} (max) spec limit curve illustrated in figure 2. NOTE: The MK 4116 family is guaranteed to have a maximum I_{DD1} requirement of 35mA @ 375ns cycle (320ns cycle for the -2) with an ambient temperature range from 0° to 70°C. A lower operating frequency, for example 1 microsecond cycle, results in a reduced maximum I_{DD1} requirement of under 20mA with an ambient temperature range from 0° to 70°C.

It is possible the MK4116 family (-2 and 3 speed selections for example) at frequencies higher than specified, provided all AC operating parameters are met. Operation at shorter cycle times ($< t_{RC}$ min) results in higher power dissipation and, therefore, a reduction in ambient temperature is required. Refer to figure 1 for derating curve.

NOTE: Additional power supply tolerance has been included on the V_{BB} supply to allow direct interface capability with both $-5V$ systems $-5.2V$ ECL systems.

TYPICAL CURRENT WAVEFORMS

Figure 5
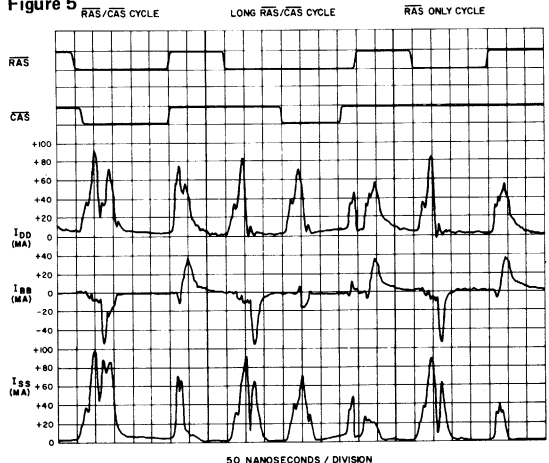
50 NANOSECONDS / DIVISION

Although $\overline{RAS}$ and/or $\overline{CAS}$ can be decoded and used as a chip select signal for the MK 4116, overall system power is minimized if the Row Address Strobe ($\overline{RAS}$) is used for this purpose. All unselected devices (those which do not receive a $\overline{RAS}$) will remain in a low power (standby) mode regardless of the state of $\overline{CAS}$.

POWER UP

The MK 4116 requires no particular power supply sequencing so long as the Absolute Maximum Rating Conditions are observed. However, in order to insure compliance with the Absolute Maximum Ratings, MOSTEK recommends sequencing of power supplies such that V_{BB} is applied first and removed last. V_{BB} should never be more positive than V_{SS} when power is applied to V_{DD}.

Under system failure conditions in which one or more supplies exceed the specified limits significant additional margin against catastrophic device failure may be achieved by forcing $\overline{RAS}$ and $\overline{CAS}$ to the inactive state (high level).

After power is applied to the device, the MK 4116 requires several cycles before proper device operation is achieved. Any 8 cycles which perform refresh are adequate for this purpose.

TYPICAL CHARACTERISTICS

TYPICAL ACCESS TIME (NORMALIZED) vs. V$_{DD}$

TYPICAL I$_{DD1}$ vs. V$_{DD}$

TYPICAL I$_{DD1}$ vs. JUNCTION TEMPERATURE

TYPICAL ACCESS TIME (NORMALIZED) vs. V$_{BB}$

TYPICAL I$_{DD2}$ vs. V$_{DD}$

TYPICAL I$_{DD2}$ vs JUNCTION TEMPERATURE

TYPICAL ACCESS TIME (NORMALIZED) vs. V$_{CC}$

TYPICAL I$_{DD3}$ vs. V$_{DD}$

TYPICAL I$_{DD3}$ vs JUNCTION TEMPERATURE

TYPICAL ACCESS TIME (NORMALIZED) vs. JUNCTION TEMPERATURE

TYPICAL I$_{DD4}$ vs V$_{DD}$

TYPICAL I$_{DD4}$ vs. JUNCTION TEMPERATURE

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TYPICAL CLOCK INPUT LEVELS vs. V$_{DD}$

$T_J = 50°C$
$V_{BB} = -5.0V$

INPUT LEVEL (VOLTS)

V$_{IHC}$ (MIN)

V$_{ILC}$ (MAX)

V$_{DD}$ SUPPLY VOLTAGE (VOLTS)

TYPICAL CLOCK INPUT LEVELS vs. V$_{BB}$

$T_J = 50°C$
$V_{DD} = 12.0V$

INPUT LEVEL (VOLTS)

V$_{IHC}$ (MIN)

V$_{ILC}$ (MAX)

V$_{BB}$ SUPPLY VOLTAGE (VOLTS)

TYPICAL CLOCK INPUT LEVELS vs. T$_J$

$V_{DD} = 12.0V$
$V_{BB} = -5.0V$

INPUT LEVEL (VOLTS)

V$_{IHC}$ (MIN)

V$_{ILC}$ (MAX)

T$_J$, JUNCTION TEMPERATURE (°C)

TYPICAL ADDRESS AND DATA INPUT LEVELS vs. V$_{DD}$

$T_J = 50°C$
$V_{BB} = -5.0V$

INPUT LEVEL (VOLTS)

V$_{IH}$ (MIN)

V$_{IL}$ (MAX)

V$_{DD}$ SUPPLY VOLTAGE (VOLTS)

TYPICAL ADDRESS AND DATA INPUT LEVELS vs. V$_{BB}$

$T_J = 50°C$
$V_{DD} = 12.0V$

INPUT LEVEL (VOLTS)

V$_{IH}$ (MIN)

V$_{IL}$ (MAX)

V$_{BB}$ SUPPLY VOLTAGE (VOLTS)

TYPICAL ADDRESS AND DATA INPUT LEVELS vs. T$_J$

$V_{DD} = 12.0V$
$V_{BB} = -5.0V$

INPUT LEVEL (VOLTS)

V$_{IH}$ (MIN)

V$_{IL}$ (MAX)

T$_J$, JUNCTION TEMPERATURE (°C)

MOSTEK®

16,384 x1-BIT DYNAMIC RAM

MK4116(P)-4

FEATURES

☐ Recognized industry standard 16-pin config-
uration from MOSTEK

☐ 250ns access time, 410ns cycle

☐ ± 10% tolerance on all power supplies (+12V, ±5V)

☐ Low power: 462mW active, 20mW standby (max)

☐ Output data controlled by $\overline{CAS}$ and unlatched at
end of cycle to allow two dimensional chip selec-
tion and extended page boundary

☐ Common I/O capability using "early write"
operation

☐ Read-Modify-Write, $\overline{RAS}$-only refresh, and Page-
mode capability

☐ All inputs TTL compatible,low capacitance, and
protected against static charge

☐ 128 refresh cycles

☐ ECL compatible on V_{BB} power supply (-5.7V)

DESCRIPTION

The MK 4116 is a new generation MOS dynamic
random access memory circuit organized as 16,384
words by 1 bit. As a state-of-the-art MOS memory
device, the MK 4116 (16K RAM) incorporates
advanced circuit techniques designed to provide
wide operating margins, both internally and to the
system user, while achieving performance levels
in speed and power previously seen only in MOSTEK's
high performance MK 4027 (4K RAM).

The technology used to fabricate the MK 4116 is
MOSTEK's double-poly, N-channel silicon gate,
POLY II℗ process. This process, coupled with the
use of a single transistor dynamic storage cell, pro-
vides the maximum possible circuit density and
reliability, while maintaining high performance

capability. The use of dynamic circuitry through-
out, including sense amplifiers, assures that power
dissipation is minimized without any sacrifice in
speed or operating margin. These factors combine
to make the MK 4116 a truly superior RAM product.

Multiplexed address inputs (a feature pioneered by
MOSTEK for its 4K RAMS) permits the MK 4116
to be packaged in a standard 16-pin DIP. This
recognized industry standard package configuration,
while compatible with widely available automated
testing and insertion equipment, provides highest
possible system bit densities and simplifies system
upgrade from 4K to 16K RAMs for new generation
applications. Non-critical clock timing requirements
allow use of the multiplexing technique while main-
taining high performance.

FUNCTIONAL DIAGRAM

PIN CONNECTIONS

PIN NAMES

A_0-A_6	ADDRESS INPUTS
$\overline{CAS}$	COLUMN ADDRESS STROBE
D_{IN}	DATA IN
D_{OUT}	DATA OUT
$\overline{RAS}$	ROW ADDRESS STROBE
$\overline{WRITE}$	READ/WRITE INPUT
V_{BB}	POWER (−5V)
V_{CC}	POWER (+5V)
V_{DD}	POWER (+12V)
V_{SS}	GROUND

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to V_{BB} . . . . −0.5V to +20V
Voltage on V_{DD}, V_{CC} supplies relative to V_{SS} . . . . −1.0V to +15.0V
$V_{BB}-V_{SS}$ ($V_{DD}-V_{SS} > 0V$) 0V
Operating temperature, T_A (Ambient) . . . . 0°C to + 70°C
Storage temperature (Ambient) . . . . −65°C to + 150°C
Short circuit output current 50mA
Power dissipation . . . . 1 Watt

RECOMMENDED DC OPERATING CONDITIONS
($0°C \leqslant T_A \leqslant 70°C$)[1]

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{DD}	10.8	12.0	13.2	Volts	1
	V_{CC}	4.5	5.0	5.5	Volts	1,2
	V_{SS}	0	0	0	Volts	1
	V_{BB}	−4.5	−5.0	−5.7	Volts	1
Input High (Logic 1) Voltage, $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	V_{IHC}	2.7	—	7.0	Volts	1
Input High (Logic 1) Voltage, all inputs except $\overline{RAS}$, $\overline{CAS}$ $\overline{WRITE}$	V_{IH}	2.4	—	7.0	Volts	1
Input Low (Logic 0) Voltage, all inputs	V_{IL}	−1.0	—	.8	Volts	1

DC ELECTRICAL CHARACTERISTICS
($0°C \leqslant T_A \leqslant 70°C$)[1] ($V_{DD} = 12.0V \pm 10\%$; $V_{CC} = 5.0V \pm 10\%$; $-5.7V \leqslant V_{BB} \leqslant -4.5V$; $V_{SS} = 0V$)

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
OPERATING CURRENT Average power supply operating current ($\overline{RAS}$, $\overline{CAS}$ cycling; $t_{RC} = 410ns$)	I_{DD1} I_{CC1} I_{BB1}		35 200	mA μA	3 4
STANDBY CURRENT Power supply standby current ($\overline{RAS} = V_{IHC}$, D_{OUT} = High Impedance)	I_{DD2} I_{CC2} I_{BB2}	−10	1.5 10	mA μA μA	
REFRESH CURRENT Average power supply current, refresh mode ($\overline{RAS}$ cycling, $\overline{CAS} = V_{IHC}$; $t_{RC} = 410ns$)	I_{DD3} I_{CC3} I_{BB3}	−10	27 10	mA μA μA	3
PAGE MODE CURRENT Average power supply current, page-mode operation ($\overline{RAS} = V_{IL}$, $\overline{CAS}$ cycling; $t_{PC} = 275ns$)	I_{DD4} I_{CC4} I_{BB4}		27	mA μA	3 4
INPUT LEAKAGE Input leakage current, any input ($V_{BB} = -5V$, $0V \leqslant V_{IN} \leqslant +7.0V$, all other pins not under test = 0 volts)	$I_{I(L)}$	−10	10	μA	
OUTPUT LEAKAGE Output leakage current (D_{OUT} is disabled, $0V \leqslant V_{OUT} \leqslant +5.5V$)	$I_{0(L)}$	−10	10	μA	
OUTPUT LEVELS Output high (Logic 1) voltage ($I_{OUT} = -5mA$)	V_{OH}	2.4		Volts	3
Output low (Logic 0) voltage ($I_{OUT} = 4.2$ mA)	V_{OL}		0.4	Volts	

NOTES:

1. All voltages referenced to V_{SS}.

2. Output voltage will swing from V_{SS} to V_{CC} when activated with no current loading. For purposes of maintaining data in standby mode, V_{CC} may be reduced to V_{SS} without affecting refresh operations or data retention. However, the V_{OH} (min) specification is not guaranteed in this mode.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (5,6,7)
(0°C ≤ T_A ≤ 70°C) (V_{DD} = 12.0V ± 10%; V_{CC} = 5.0V ± 10%, V_{SS} = 0V, -5.7V ≤ V_{BB} ≤ -4.5V)

PARAMETER	SYMBOL	MK 4116 MIN	MAX	UNITS	NOTES
Random read or write cycle time	t_{RC}	410		ns	
Read-write cycle time	t_{RWC}	425		ns	
Read Modify Write	t_{RMW}	500		ns	
Page mode cycle time	t_{PC}	275		ns	
Access time from $\overline{RAS}$	t_{RAC}		250	ns	8,10
Access time from $\overline{CAS}$	t_{CAC}		165	ns	9,10
Output buffer turn-off delay	t_{OFF}	0	60	ns	11
Transition time (rise and fall)	t_T	3	50	ns	7
$\overline{RAS}$ precharge time	t_{RP}	150		ns	
$\overline{RAS}$ pulse width	t_{RAS}	250	10000	ns	
$\overline{RAS}$ hold time	t_{RSH}	165		ns	
$\overline{CAS}$ pulse width	t_{CAS}	165		ns	
$\overline{CAS}$ hold time	t_{CSH}	250		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	35	85	ns	12
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	−20		ns	
Row Address set-up time	t_{ASR}	0		ns	
Row Address hold time	t_{RAH}	35		ns	
Column Address set-up time	t_{ASC}	−10		ns	
Column Address hold time	t_{CAH}	75		ns	
Column Address hold time referenced to $\overline{RAS}$	t_{AR}	160		ns	
Read command set-up time	t_{RCS}	0		ns	
Read command hold time	t_{RCH}	0		ns	
Write command hold time	t_{WCH}	75		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	160		ns	
Write command pulse width	t_{WP}	75		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	85		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	85		ns	
Data-in set-up time	t_{DS}	0		ns	13
Data-in hold time	t_{DH}	75		ns	13
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	160		ns	
$\overline{CAS}$ precharge time (for page-mode cycle only)	t_{CP}	100		ns	
Refresh period	t_{REF}		2	ms	
$\overline{WRITE}$ command set-up time	t_{WCS}	−20		ns	14
$\overline{CAS}$ to $\overline{WRITE}$ delay	t_{CWD}	90		ns	14
$\overline{RAS}$ to $\overline{WRITE}$ delay	t_{RWD}	175		ns	14

3. I_{DD1}, I_{DD3}, and I_{DD4} depend on cycle rate. The maximum specified current values are for t_{RC}=410ns and t_{PC}=275ns. I_{DD} limit at other cycle rates are determined by the following equations:

I_{DD1} (max) [MA] =10+10.25 x cycle rate [MHz]
I_{DD3} (max) [MA] =10+7 x cycle rate [MHz]
I_{DD4} (max) [MA] =10 + 4.7 x cycle rate [MHz]

4. I_{CC1} and I_{CC4} depend upon output loading. During readout of high level data V_{CC} is connected through a low impedance (135 typ) to data out. At all other times I_{CC} consists of leakage currents only.

5. Several cycles are required after power-up before proper device operation is achieved. Any 8 cycles which perform refresh are adequate for this purpose.

6. AC measurements assume t_T=5ns.

7. V_{IHC} (min) or V_{IH}((min) and V_{IL}(max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IHC} or V_{IH} and V_{IL}.

8. Assumes that t_{RCD}≤t_{RCD} (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.

9. Assumes that t_{RCD}≥t_{RCD} (max).

10. Measured with a load equivalent to 2 TTL loads and 100pF.

11. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

12. Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.

13. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in delayed write or read-modify-write cycles.

14. t_{WCS}, t_{CWD} and t_{RWD} are restrictive operating parameters in read write and read modify write cycles only. If t_{WCS} ≥ t_{WCS} (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) ≥ (min), the cycle is a read-write cycle and the data out will contain data read from the selected cell; If neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.

15. Effective capacitance calculated from the equation $C = \dfrac{I \triangle t}{\triangle v}$ with $\triangle v$ = 3 volts and power supplies at nominal levels.

16. $\overline{CAS}$ = V_{IHC} to disable D_{OUT}.

16,384 X 1-BIT DYN RAM
MK4116(P)-4

AC ELECTRICAL CHARACTERISTICS

$(0°C \leqslant T_A \leqslant 70°C)$ $(V_{DD} = 12.0V \pm 10\%; V_{SS} = 0V; -5.7V \leqslant V_{BB} \leqslant -4.5V)$

PARAMETER	SYMBOL	TYP	MAX	UNITS	NOTES
Input Capacitance (A_0-A_6), D_{IN}	C_{I1}	4	5	pF	17
Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	C_{I2}	8	10	pF	17
Output Capacitance (D_{OUT})	C_0	5	7	pF	17,18

DESCRIPTION (continued)

System oriented features include ± 10% tolerance on all power supplies, direct interfacing capability with high performance logic families such as Schottky TTL, maximum input noise immunity to minimize "false triggering" of the inputs (a common cause of soft errors), on-chip address and data registers which eliminate the need for interface registers, and two chip select methods to allow the user to determine the appropriate speed/power characteristics of his memory system. The MK 4116 also incorporates several flexible timing/operating modes. In addition to the usual read, write, and read-modify-write cycles, the MK 4116 is capable of delayed write cycles, page-mode operation and $\overline{RAS}$-only refresh. Proper control of the clock inputs($\overline{RAS}$, $\overline{CAS}$ and $\overline{WRITE}$) allows common I/O capability, two dimensional chip selection, and extended page boundaries (when operating in page mode).

Supplemental Data Sheet to be used in conjunction with the Mostek MK4116(P)-2/3 Data Sheet.

MOSTEK®

4096 x 1-BIT STATIC RAM
MK4104 (P/N) Series

FEATURES

☐ Combination static storage cells and dynamic control circuitry for truly high performance

PART NUMBER	ACCESS TIME	CYCLE TIME
MK4104-3/-33	200ns	310ns
MK4104-4/-34	250ns	385ns
MK4104-5/-35	300ns	460ns
MK4104-6	350ns	535ns

☐ Low Active Power Dissipation 120mW (Max)

☐ Battery backup mode (3V/10mW on -33, 34 and -35)

☐ Standby Power Dissipation less than 28 mW (at V_{CC} = 5.5V)

☐ Single +5V Power Supply (± 10% tolerance) (±5% on -6 only)

☐ Fully TTL Compatible

Fanout: 2 – Standard TTL
2 – Schottky TTL
12 – Low Power Schottky TTL

☐ Standard 18-pin DIP

DESCRIPTION

The MOSTEK MK 4104 is a high performance static random access memory organized as 4096 one bit words. The MK 4104 combines the best character-istics of static and dynamic memory techniques to achieve a TTL compatible, 5 volt only, high perfor-mance, low power memory device. It utilizes ad-vanced circuit design concepts and an innovative state-of-the-art N-channel silicon gate process special-ly tailored to provide static data storage with the per-formance (speed and power) of dynamic RAMs. Since the storage cell is static the device may be stopped indefinitely with the $\overline{CE}$ clock in the off (Logic 1) state.

All input levels, including write enable ($\overline{WE}$) and chip enable ($\overline{CE}$) are TTL compatible with a one level of 2.2 volts and a zero level of 0.8 volts. This gives the system designer for a logic "1" state, at least 200mV of noise margin when driven by standard TTL and a minimum of 500mV when used with high perfor-mance Schottky TTL. These margins are wider than on most TTL compatible MOS memories available. The push-pull output (no pull-up resistor required) delivers a one level of 2.4V minimum and a zero level of .4 volts maximum. The output has a fanout of 2 standard TTL loads or 12 low power Schottky loads.

The RAM employs an innovative static cell which occupies a mere 2.75 square mils (½ the area of pre-vious cells) and dissipates power levels comparable

FUNCTIONAL DIAGRAM
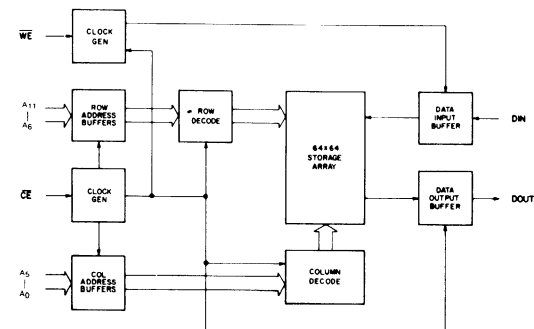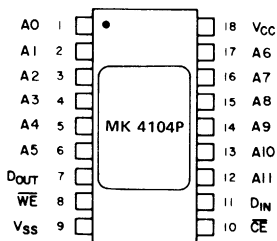
PIN CONNECTIONS

PIN NAMES

$A_0 - A_{11}$	ADDRESS INPUTS	V_{SS}	GROUND
$\overline{CE}$	CHIP ENABLE	V_{CC}	POWER (+5V)
D_{IN}	DATA INPUT	$\overline{WE}$	WRITE ENABLE
D_{OUT}	DATA OUTPUT		

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to V$_{SS}$ . . . . −1.0V to +7.0V
Operating Temperature T$_A$ (Ambient) . . . . 0°C to + 70°C
Storage Temperature (Ambient) (Ceramic) . . . . −65°C to +150°C
Storage Temperature (Ambient) (Plastic) . . . . −55°C to +125°C
Power Dissipation . . . . 1 Watt
Short Circuit Output Current 50mA

RECOMMENDED DC OPERATING CONDITIONS[6]
(0°C ≤ T$_A$ ≤ + 70°C)

	PARAMETER	MK4104 -3/-33/-4/ -34/-5/-35			MK4104 -6 ONLY			UNITS	NOTES
V$_{CC}$	Supply Voltage	4.5	5.0	5.5	4.75	5.0	5.25	Volts	1
V$_{SS}$	Supply Voltage	0	0	0	0	0	0	Volts	1
V$_{IH}$	Logic "1" Voltage All Inputs	2.2		7.0	2.2		7.0	Volts	1
V$_{IL}$	Logic "0" Voltage All Inputs	-1.0		.8	-1.0		.8	Volts	1

DC ELECTRICAL CHARACTERISTICS[1]
(0°C ≤ T$_A$ ≤ + 70°C) (V$_{CC}$ = 5.0 volts ± 10%)

	PARAMETER	MIN	MAX	UNITS	NOTES
I$_{CC1}$	Average V$_{CC}$ Power Supply Current		21	mA	2
I$_{CC2}$	Standby V$_{CC}$ Power Supply Current		5	mA	3
I$_{IL}$	Input Leakage Current (Any Input)	−10	10	μA	4
I$_{OL}$	Output Leakage Current	−10	10	μA	3, 5
V$_{OH}$	Output Logic "1" Voltage I$_{OUT}$=−500μA	2.4		Volts	
V$_{OL}$	Output Logic "0" Voltage I$_{OUT}$= 5mA		0.4	Volts	

AC ELECTRICAL CHARACTERISTICS[1]
(0°C ≤ T$_A$ ≤ + 70°C) (V$_{CC}$ = + 5.0 volts ± 10%)

	PARAMETER	TYP	MAX	NOTES
C$_I$	Input Capacitance	4pF	6pF	14
C$_0$	Output Capacitance	6pF	7pF	14

NOTES:

1. All voltages referenced to V$_{SS}$. ±5% tolerance on V$_{CC}$ for -6 only.

2. I$_{CC1}$ is related to precharge and cycle times. Guaranteed maximum values for I$_{CC1}$ may be calculated by:
   I$_{CC1}$ [ma] = (5t$_p$ + 13(t$_C$ − t$_p$) + 3420) ÷ t$_C$
   where t$_p$ and t$_C$ are expressed in nanoseconds. Equation is referenced to the -3 device, other devices derate to the same curve.

3. Output is disabled (open circuit), $\overline{CE}$ is at logic 1.

4. All device pins at 0 volts except pin under test at 0 ≤ V$_{IN}$ ≤ 5.5 volts.

5. 0V ≤ V$_{OUT}$ ≤ + 5.5V.

6. During power up, $\overline{CE}$ and $\overline{WE}$ must be at V$_{IH}$ for minimum of 2ms after V$_{CC}$ reaches 4.5V, before a valid memory cycle can be accomplished.

7. Measured with load circuit equivalent to 2 TTL loads and CL = 100 pF.

8. If $\overline{WE}$ follows $\overline{CE}$ by more than t$_{WS}$ then data out may not remain open circuited.

9. Determined by user. Total cycle time cannot exceed t$_{CE}$ max.

10. Data-in set-up time is referenced to the later of the two falling clock edges $\overline{CE}$ or $\overline{WE}$.

11. AC measurements assume t$_T$ = 5ns. Timing points are taken as V$_{IL}$ = 0.8V and V$_{IH}$ = 2.2V on the inputs and V$_{OL}$ = 0.4V and V$_{OH}$ = 2.4V on the output waveform.

12. t$_C$ = t$_{CE}$ + t$_P$ + 2t$_T$.

13. The true level of the output in the open circuit condition will be determined totally by output load conditions. The output is guaranteed to be open circuit within t$_{OFF}$.

14. Effective capacitance calculated from the equation C = I$\frac{\Delta t}{\Delta V}$ with Δ V equal to 3V and V$_{CC}$ nominal.

15. t$_{RMW}$ = t$_{AC}$ + t$_{WPL}$ + t$_P$ + 3t$_T$ + t$_{MOD}$

AC ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS[6,11]
($0°C \leqslant T_A \leqslant +70°C$) ($V_{CC} = +5.0$ volts $\pm$ 10%)[1]

SYMBOL	PARAMETER	MK4104-3/33		MK4104-4/34		MK4104-5/35		MK4104-6		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
t_C	Read or Write Cycle Time	310		385		460		535		ns	12
t_{AC}	Random Access		200		250		300		350		7
t_{CE}	Chip Enable Pulse Width	200	10,000	250	10,000	300	10,000	350	10,000		
t_P	Chip Enable Precharge Time	100		125		150		175			
t_{AH}	Address Hold Time	110		135		165		190			
t_{AS}	Address Set-Up Time	0		0		0		0			
t_{OFF}	Output Buffer Turn-Off Delay	0	50	0	65	0	75	0	100		13
t_{RS}	Read Command Set-Up Time	0		0		0		0			8
t_{WS}	Write Enable Set-Up Time	-20		-20		-20		-20			8
t_{DHC}	Data Input Hold Time Referenced to $\overline{CE}$	170		210		250		285			
t_{DHW}	Data Input Hold Time Referenced to $\overline{WE}$	70		90		105		125			
t_{WW}	Write Enabled Pulse Width	60		75		90		105			
t_{MOD}	Modify Time	0	10,000	0	10,000	0	10,000	0	10,000		9
t_{WPL}	$\overline{WE}$ to $\overline{CE}$ Precharge Lead Time	70		85		105		120			10
t_{DS}	Data Input Set-Up Time	0		0		0		0			
t_{WH}	Write Enable Hold Time	150		185		225		260			
t_T	Transition Time	5	50	5	50	5	50	5	50		
t_{RMW}	Read-Modify-Write Cycle Time	385		475		570		660			16

STANDBY CHARACTERISTICS
($T_A = 0°C$ to $70°C$)

SYMBOL	PARAMETER	MK4104-33		MK4104-34		MK4104-35				UNITS
		MIN	MAX	MIN	MAX	MIN	MAX			
V_{PD}	V_{CC} In Standby	3.0		3.0		3.0				Volts
I_{PD}	Standby Current		3.3		3.3		3.3			mA
T_F	Power Supply Fall Time	100		100		100				μsec
T_R	Power Supply Rise Time	100		100		100				μsec
T_{CE}	Chip Enable Pulse $\overline{CE}$ Width	200		250		300				μsec
T_{PPD}	Chip Enable Precharge To Power Down Time	100		125		150				nsec
V_{IH}	"I" Level $\overline{CE}$ Min Level	2.2		2.2		2.2				Volts
T_{RC}	Standby Recovery Time	500		500		500				μsec

POWER DOWN WAVEFORM
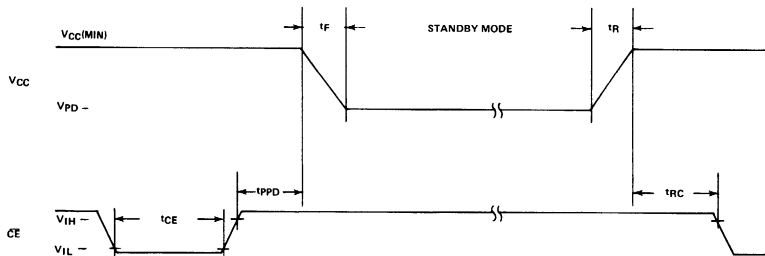
DESCRIPTION (Cont'd)

to CMOS. The static cell eliminates the need for refresh cycles and associated hardware thus allowing easy system implementation.

Power supply requirements of +5V ± 5% tolerance combined with TTL compatability on all I/O pins permits easy integration into large memory configurations. The single supply reduces capacitor count and permits denser packaging on printed circuit boards. The 5V only supply requirement and TTL compatible I/O makes this part an ideal choice for next generation +5V only microprocessors such as MOSTEK's MK3880 (Z80) and MK3870. The early write mode ($\overline{WE}$ active prior to $\overline{CE}$) permits common I/O operation, needed for Z80 interfacing, without external circuitry.

The MK4104-3 series has the added capability of retaining data in a reduced power mode. V_{CC} maybe lowered to 3V with a guaranteed power dissipation of only 10mW maximum. This makes the MK4104 ideal for those applications requiring data retention at the lowest possible power as in battery operation.

Reliability is greatly enhanced by the low power dissipation which causes a maximum junction rise of only at 8°C at 1.86 Megahertz operation. The MK 4104 was designed for the system designer and user who require the highest performance available along with MOSTEK's proven reliability.

READ CYCLE

WRITE CYCLE

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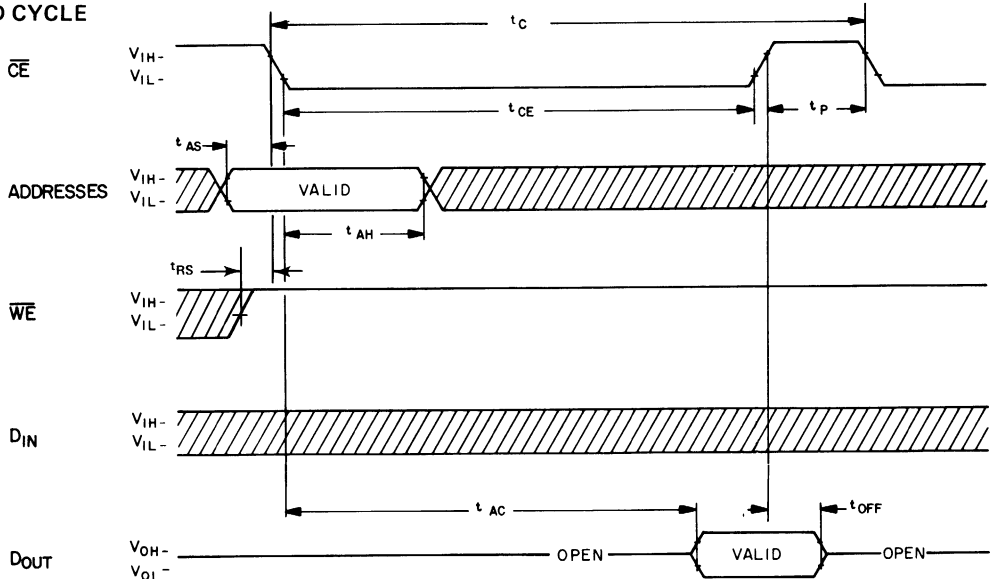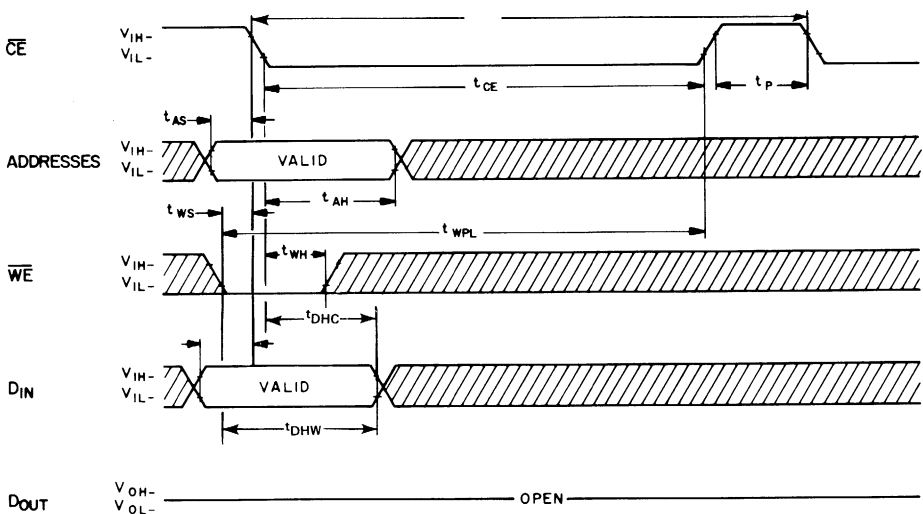
READ-MODIFY-WRITE CYCLE
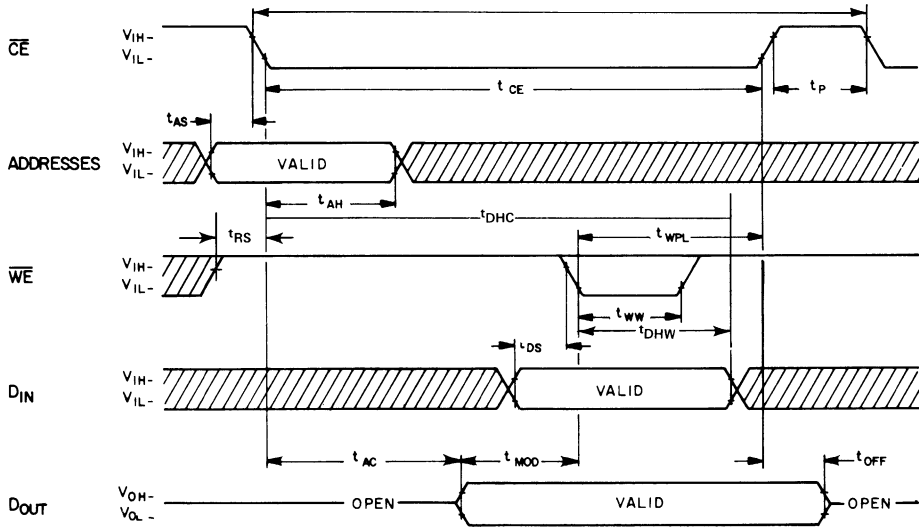
OPERATION

READ CYCLE

The circuit offers one bit of the possible 4096 by decoding the 12 address bits presented at the inputs. The address bits are strobed into the chip by the negative-going edge of the Chip Enable ($\overline{CE}$) clock. A read cycle is accomplished by holding the 'write enable' ($\overline{WE}$) input at a high level (V_{IH}) while clocking the $\overline{CE}$ input to a low level (V_{IL}). At access time (t_{AC}) valid data will appear at the output. The output is unlatched by a positive transition of $\overline{CE}$ and therefore will be open circuited (high impedance state) from the previous cycle to access time and will go open again at the end of the present cycle when $\overline{CE}$ goes high.

Once the address hold time has been satisfied, the addresses may be changed for the next cycle.

WRITE CYCLE

Data that is to be written into a selected cell is strobed into the chip on the later occurring negative edge of $\overline{CE}$ or $\overline{WE}$. If the negative transition of $\overline{WE}$ occurs prior to the leading edge of $\overline{CE}$ as in an "early" write cycle then the $\overline{CE}$ input serves as the strobe for data-in. If $\overline{CE}$ leading edge occurs prior to the leading edge of $\overline{WE}$ as in a read-modify-write cycle then data-in is strobed by the $\overline{WE}$ input. Due to the internal timing generator, two independent timing parameters must be satisfied for DI hold time, these are, t_{DHW} and t_{DHC}. For a R/W or RMW cycle t_{DHC} is automatically satisfied making t_{DHW} the more restrictive parameter. For a write only cycle either parameter can be more restrictive depending on the position of $\overline{WE}$ relative to $\overline{CE}$. In any event both parameters must be satisfied.

In an 'early' write cycle the output will remain in an open or high impedance state. In a read-modify write operation the output will go active through the modify and write period until $\overline{CE}$ goes to precharge. If the cycle is such that $\overline{WE}$ goes active after $\overline{CE}$ but before valid data appears on the output (prior to t_{AC}) then the output may not remain open. However, if data-in is valid on the leading edge of $\overline{WE}$, and $\overline{WE}$ occurs prior to the positive transition of $\overline{CE}$ by the minimum lead time t_{WPL}, then valid data will be written into the selected cell. The Data in hold time parameters t_{DHW} and t_{DHC} must be satisfied.

READ-MODIFY-WRITE CYCLE

The read-modify-write (RMW) cycle is no more than an extension of the read and write cycles. Data is read at access time, modified during a period determined by the user and the same or new data written between $\overline{WE}$ active (low) and the rising edge of $\overline{CE}$ (t_{WPL}). Data out will remain valid until the rising edge of $\overline{CE}$. A minimum RMW cycle time can be approximated by the following equation (t_{RMW} = RMW cycle time and t_P = $\overline{CE}$ precharge time).

$$t_{RMW} = t_{AC} + t_{MOD} + t_{WPL} + t_P + 3t_T$$

POWER DOWN MODE

In power down data may be retained indefinitely by maintaining V_{CC} at +3V. However, prior to V_{CC} going below V_{CC} minimum ($\leqslant 4.5V$) $\overline{CE}$ must be taken high (V_{IH} = 2.2V) and held for a minimum time period t_{PPD} and maintained at V_{IH} for the entire standby period. After power is returned to V_{CC} min or above, $\overline{CE}$ must be held high for a minimum of t_{RC} in order that the device may operate properly. See power down waveforms herein. Any active cycle in progress prior to power down must be completed so that t_{CE} min is not violated.

OPERATING POWER VS CYCLE TIME
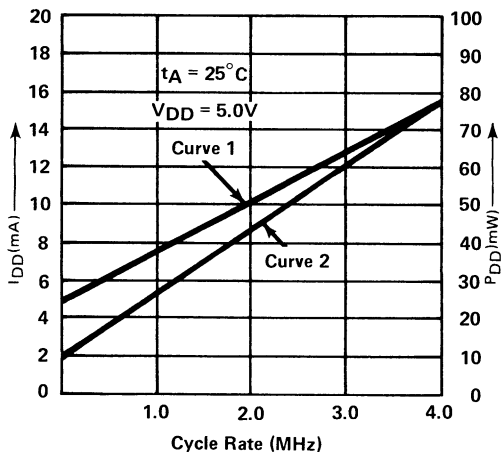
Characterization data plot of frequency vs power dissipation for a typical MK4104 device.

Curve 1 - Clock on time (low level) is bottom scale minus 100 NSEC

Curve 2 - Clock off time (high level) is bottom scale minus 200 NSEC

PACKAGE DESCRIPTION

18-Pin Dual In-Line Ceramic

PACKAGE DESCRIPTION

18-Pin Dual In-Line Plastic

MEMORY DATA BOOK
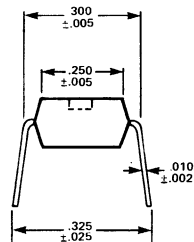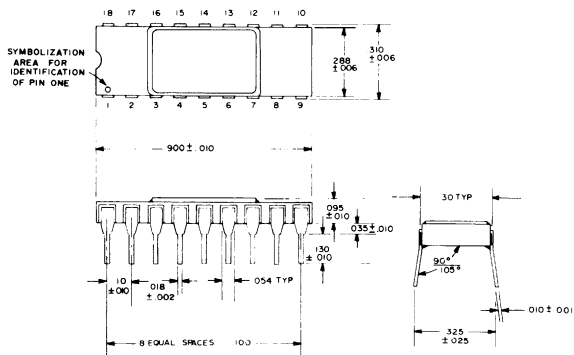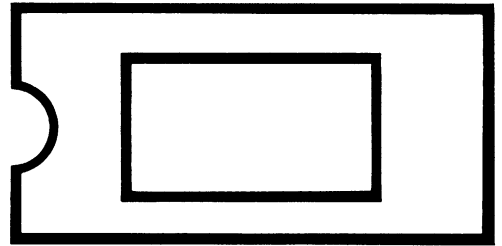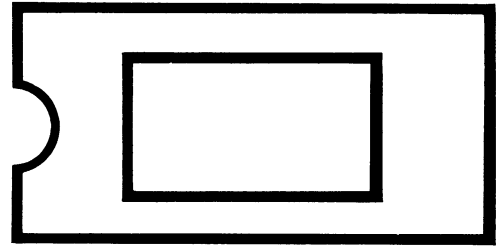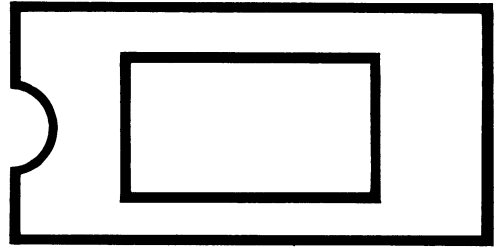
HI-REL MEMORY
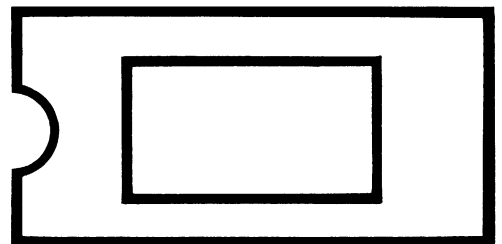
1.0 PURPOSE — To provide a general quality specification for Military/Hi-Rel to be used with the applicable detail specification to ensure a higher than commercial level of device screening, product assurance and quality control.

2.0 SCOPE —

2.1 Statement of Scope. This specification establishes the GENERAL requirements for Military/Hi-Rel monolithic MOS/LSI microcircuits supplied by MOSTEK. This document is applicable only to devices with MKB, MKM, or MKX product designator prefixes.

2.2 Product Assurance Levels. This specification provides for three (3) levels of product assurance and screening as outlined below and in 3.4 and 3.4.1.

2.2.1. MKB MOSTEK product designator for a device processed to MIL-STD-883, Method 5004, Class B.

2.2.2. MKM MOSTEK product designator for a device processed to MIL-STD-883, Method 5004, Class B, except as modified in 3.4 and 3.4.1 (basic difference from MKB is single pass correlated hi-temp testing with guard band to guarantee 25°C and low temp).

2.2.3. MKX MOSTEK product designator for a custom military device purpose built to a customer P.O. that has some degree of military processing. See 3.4 and 3.4.1.

2.3. Applicable Documents. The following documents of issue in effect on the date of release of the MOSTEK Sales Order form a part of this specification to the extent specified herein.
A. MIL-M-38510 Microcircuits General Specification For
B. MIL-STD-883 Test Methods and Procedures for Microelectronics.
C. MIL-STD-1313 Microelectronics Terms and Definitions
D. MIL-C-45662 Calibration System Requirements
E. MOSTEK Sales Order
F. CUSTOMER Purchase Order
G. Detail Specification of Applicable Device Type (Military Data Sheet)

2.3.1. Document Hierarchy. In the event of any conflict between this document and the referred documents, the following order of precedence shall apply:
A. MOSTEK Sales Order
B. Customer Purchase Order
C. This document
D. Detail Specification (Military Data Sheet)
E. Referenced documents

3.0 GENERAL

3.1. General. MOSTEK, in compliance with this specification, shall have and use production and test facilities and a quality and reliability assurance program adequate to assure successful compliance with the provisions of this specification and the detail specification. The individual item requirements shall be as specified herein, and in the detail specification or drawing.

HI-REL MEMORY

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3.1.1. Reference to Detail Specification. For purposes of this specification, when the term "as specified" is used without additional reference to a specific location or document, the intended reference shall be to the detail specification or drawing number which constitutes the applicable individual device specification.

3.1.2. Terms, Definitions, and Symbols. For the purpose of this specification, the terms, definitions, and symbols of MIL-STD-883, MIL-STD-1313, and MIL-STD-1331 and those contained herein shall apply and shall be used in the applicable detail specification wherever they are pertinent.

A. **Production Lot.** A production lot shall consist of devices manufactured on the same production line(s) by means of the same production technique, materials, controls and design. Where a production lot identification is terminated upon completion of wafer or substrate processing, or at any later point prior to device dealing, it shall be permissible to process more than a single device type in a single production lot provided traceability is maintained by assembling devices into inspection lots as defined herein, at the point where production lot identification is terminated.

B. **Inspection Lot.** A quantity of microcircuits submitted at one time for inspection to determine compliance with the requirements and acceptance criteria of the applicable device specification. Each inspection lot shall consist of microcircuits of a single type, in a single package type, outline and lead finish, or may consist of inspection sublots of several different types, in a single package type, outline and lead finish defined by a single detail specification. Each inspection lot shall be manufactured on the same production line(s) through final seal by the same production techniques, and to the same device design rules and case with the same material requirements, and sealed within the same period not exceeding six weeks.

C. **Inspection Sublot** - An inspection sublot shall consist of microcircuits of a single type in a single package type, outline and lead finish, contained on a single detail specification, manufactured on the same production line(s) through final seal by the same production techniques, and to the same device design rules and package with the same material requirements, and sealed within the same period not exceeding six weeks.

D. **Microcircuit Group** - Microcircuits which are designed to perform the same type of basic circuit function, which are designed for the same supply, bias and signal voltages and for input/output compatibility and which are fabricated by use of the same basic die construction and metallization; the same die-attach method; and by use of bonding interconnects of the same size, material and attachment method.

E. **Percent Defective Allowable (PDA).** Percent defective allowable is the maximum observed percent defective which will permit the lot to be accepted after the specified 100 percent test.

F. **Delta ($\triangle$) Limit.** The maximum change in a specified parameter reading which will permit a device to be accepted on a specified test, based on a comparison of the present measurement with a specified previous measurement. NOTE: When expressed as a percentage value, it shall be calculated as a proportion of the previous measured value.

G. **Rework.** Any processing or reprocessing operation, other than testing, applied to an individual device, or part thereof, and performed subsequent to the prescribed nonrepairing manufacturing operations which are applicable to all devices of that type at that stage.

H. **Final Seal.** That manufacturing operation which completes the enclosure of a device so that further internal processing cannot be completed without disassembling the device.

I. **Device Type.** The term device type refers to a single specific microcircuit configuration. Samples of the same device type will be electrically and functionally interchangeable with each other at the die level and environmental limits will be the same for a given device type even though the device class, the case outline, and the lead finish and the lot identification code may be different. A given type shall appear on only one device specification but that detail specification may also specify other similar devices.

3.2. Item Requirements. The individual item requirements for microcircuits delivered under this specification shall be documented in the detail specification or drawing. Unless otherwise specified, all microcircuits shall have an operating ambient temperature range from -55°C to +125°C and any reference to minimum or maximum operating temperatures shall refer to the respective lower and upper limits of this range.

3.3 Classification of Requirements. The requirements of the microcircuits are classified herein as follows:

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REQUIREMENTS	PARAGRAPH
Product Assurance	3.4
Screening	3.4.3
Quality conformance inspection	3.4.4
Traceability	3.4.5
Design and construction	3.5
Marking	3.6
Workmanship	3.7

3.4. Product Assurance Requirements. Three levels of microcircuit quality and reliability assurance are provided for in this specification. MKB, MKM and MKX devices shall be those which have been subjected to, and passed all applicable requirements, tests, and inspections detailed herein, for the specified class. Where shown, method references are per MIL-STD-883. For general guidance, the following table summarizes these requirements for the respective device classes:

3.4 Cont.	SCREENING PER METHOD 5004 of MIL-STD-883			
TEST	MIL-STD-883A	CONDITION	MKB	MKM
Internal Visual	2010	Cond. 'B	100%	100%
Stabilization Bake	1008	24 Hrs @ +150°C	100%	100%
Temperature Cycling	1010	10 cycles min. −65°C to +150°C	100%	100%
Constant Acceleration	2001	30 KG Y_1 Plane Only	100%	100%
Seal Fine	1014	5×10^{-8} ATM-CM^3/SEC	100%	100%
Gross	1014	Condition C2	100%	100%
Pre-Burn-in Electrical 1/	Static & Dynamic		100%	100%
Burn-In	1015	MOSTEK Dynamic +160 hours minimum T_A = +125°C	100%	100%
Final Electrical Test		Static and Dynamic per Detail Spec	100% Max, 25°C and min rated Temp	100% Max Rated Temp
External Visual	2009		100%	100%
Quality Conformance	5005	Group A See Quality Conformance	Max., 25°C and Min. Rated Temp	7%LTPD 3/Max Rated Temp

1/ Manufacturer's Option
2/ Delete Subgroups 9, 10 and 11
3/ Subgroups 2, 5, and 8 combined at maximum rated temp.

NOTE: MKX is a custom flow, built per the customer drawing and may contain all, some or none of the above flow.

MIL-STD-883A QUALITY CONFORMANCE TEST

Group A (Each Lot)	TEST METHOD OF MIL-STD-883	LTPD IN %	TEST CONDITIONS		
			MKB Series	MKM Series	NOTES
Static Test	——		Per Detail Spec at min., 25°C and max temperature 1/	Max Rated Temp 2/	
Dynamic Test	5005				
Functional Test	——				
GROUP B (Each Lot) Physical Dimensions	2016	2 Dev	Per Detail Spec	Per Detail Spec	3, 4
Resistance to Solvents	2015	3 Dev	Marking Durability	Marking Durability	3, 5
Internal Visual	2014	2 Dev	Internal Construction Verification	Internal Construction Verification	3, 6
Bond Strength	2011	15	Condition D	Condition D	3, 7
Solderability	2003	15	260 ± 10°C	260 ± 10°C	3, 8
GROUP C (9/) Operating Life End Point Electrical	1005	5	+125°C 1000 Hrs. Max Rated Temp	+125°C 1000 Hrs Max Rated Temp	9
Temp Cycle	1010		−65°C to +150°C Cond. E	−65°C to +150°C Cond. E	
Constant Acceleration	2001	15			
Fine and Gross Leak	1014		5×10^{-8} ATM-CM^3/SEC Max Rated Temp	5×10^{-8} ATM-CM^3/SEC Max Rated Temp	
End Point Electrical					
GROUP D (9/) Physical Dimensions	2016	15	Per Detail Spec	Per Detail Spec	9
Lead Integrity	2004	15	Condition B2	Condition B2	
Fine and Gross Leak	1014	15	5×10^{-8} ATM-CM^3/SEC	5×10^{-8} ATM-CM^3/SEC	
Thermal Shock	1011	15	Condition B	Condition B	
Temperature Cycling	1010	15	Condition C -100 Cycles	Condition C -100 Cycles	
Moisture Resistance	1004	15	10 Cycles	10 Cycles	
Fine and Gross Leak	1014	15	5×10^{-8} ATM-CM^3/SEC Max Rated Temp	5×10^{-8} ATM-CM^3/SEC Max Rated Temp	
End Point Electrical					
Mechanical Shock	2002	15	Condition B	Condition B	
Vibration	2007	15	Condition A	Condition A	
Constant Acceleration	2001	15	Condition D	Condition D	
Fine and Gross Leak	1014	15	5×10^{-8} ATM-CM^3/SEC Max Rated Temp	5×10^{-8} ATM-CM^3/SEC Max Rated Temp	
End Point Electrical					
Salt Atmosphere	1009	15	Condition A	Condition A	

3.4.1. Cont:

(1/) Delete Subgroups 9, 10, 11 (2/) Subgroups 2, 5, and 8 at Maximum Rated Temp to a combined LTPD of 7% (3/) Electrical Rej. may be used (4/) 2 Devices from each lot will be tested. Accept on 0/, reject on 1. (5/) 3 Devices from each lot will be tested. Accept on 0/, reject on 1. (6/) 1 Device from lot will be tested. Accept on 0/, reject on 1. (7/) Test Sample may be pulled prior

to sealing. (8/) Solderability sample must have seen time/temp exposure or burn-in. (9/) Group C and D tests will be performed "only" when specified on the Customer Purchase Order.

3.4.2 Change of Qualified Product. MOSTEK shall notify the customer prior to the implementation of any major change of the product or product assurance program which may affect performance, quality-reliability and interchangeability.

3.4.3. Screening. All microcircuits to be delivered in accordance with this specification shall have been subjected to, and passed, all the screening tests detailed in Paragraph 3.4 for the type of microcircuit and product assurance level (device class) specified. Sampling inspections shall not be an acceptable substitute for any specified screening test.

3.4.4. Quality Conformance Inspection. Microcircuits shall not be accepted or approved for delivery until the inspection lot has passed quality conformance inspection. (See 4.3.)

3.4.5. Tracability. See 3.1.2. (A)

3.5. Design and Construction. Microcircuit design and construction shall be in accordance with all the requirements specified herein and in the detail specification or drawing.

3.5.1. Package. All devices supplied under this specification shall be hermetically sealed in glass, metal or ceramic (or combinations of these) packages. No organic or polymetic materials (lacquers, varnishes, coatings, adhesives, greases, etc.) shall be used inside the microcircuit package, and no desiccants shall be contained in the microcircuit package unless otherwise specified. Polymer impregnations (backfill, docking, etc.) of the microcircuit packages shall not be permitted.

3.5.2. Metals. External metal surfaces shall be corrosion-resistant or shall be plated or treated to resist corrosion. External leads shall meet the requirements specified in 3.5.5.

3.5.3. Other Materials. External parts, elements or coatings including markings shall be inherently non-nutrient to fungus and shall not blister, crack, outgas, soften, flow or exhibit defects that adversely affect storage, operation or environmental capabilities of microcircuits delivered to this specification under the specified test conditions.

3.5.4 Internal Conductors. Internal thick film conductors on silicon die or substrate (metallization stripes, contact areas, bonding interfaces, etc.) shall be designed so that no properly fabricated conductor shall experience in normal operation (at worst case specified operating conditions), a current density in excess of the maximum allowable value shown below for the applicable conductor material:

CONDUCTOR MATERIAL	MAXIMUM ALLOWABLE CURRENT DENSITY
Aluminum (99.99% pure or doped) without glassivation	2×10^5 A/cm^2
Aluminum (99.99% pure or doped) glassivated	5×10^5 A/cm^2
Gold	6×10^5 A/cm^2
All other (unless otherwise specified)	2×10^5 A/cm^2

The current density shall be calculated at the point(s) of maximum current density (i.e. greatest current (see 3.5.5 (a)) per unit cross section) for the specific device type and schematic or configuration.

(a) Use a current value equal to the maximum continuous current (at a full fanout for digitals or at maximum load for linears) or equal to the simple time-averaged current

obtained at maximum rated frequency and duty cycle with maximum load, whichever results in the greater current value at the point(s) of maximum current density. This current value shall be determined at the maximum recommended supply voltage(s) and with the current assumed to be uniform over the entire conductor cross sectional areas.

3.5.5. Lead Material and Finish.

3.5.5.1. Lead Material. Lead material shall conform to one of the following chemical compositions:

A.   Type A

Iron . . . . 53 percent, nominal
Nickel . . . . 29 ± 1 percent
Cobalt . . . . 17 ± 1 percent
Manganese . . . . 0.65 percent, maximum
Carbon . . . . 0.06 percent, maximum
Silicon . . . . 0.20 percent, maximum
Aluminum . . . . 0.10 percent, maximum
Magnesium . . . . 0.10 percent, maximum
Zirconium . . . . 0.10 percent, maximum
Titanium . . . . 0.10 percent, maximum

(Combined total of aluminum, magnesium, zirconium and titanium to be a maximum of 0.20 percent).

B.   Type B

Nickel . . . . 40-43 percent
Manganese . . . . 0.08 percent, maximum
Silicon . . . . 0.30 percent, maximum
Carbon . . . . 0.10 percent, maximum
Chronium . . . . 0.25 percent, maximum
Cobalt . . . . 0.50 percent, maximum
Phosphorous . . . . 0.025 percent, maximum
Sulfur . . . . 0.025 percent, maximum
Aluminum . . . . 0.10 percent, maximum
Iron . . . . Remainder

3.5.5.2. Lead Finish. Lead finish shall conform to one of the following as applicable.

A.   Hot solder dip - The hot solder dip shall be homogeneous with a minimum thickness at the crest of the major flats of 200 microinches (50.8 nm) of solder (SN60 to SN63) over the preliminary finishes in accordance with (b) or (c) below or over nickel plate with a plating thickness of 100 microinches (25.4 nm) minimum and 200 microinches (50.8 nm) maximum.

B.   Bright acid tin plate - Thickness of 100 microinches (25.4 nm) minimum and 400 microinches (101.6 nm) maximum. Optional electroless or electrolytic nickel or copper underplating, if used, shall be a minimum of 10 microinches (25.4 nm) in thickness. NOTE: It is recognized that "bright acid tin plate", a term which refers to the process as well as the appearance, can yield a range of texture or reflectivity. It is intended that this finish be dense and continuous and that it will meet the solderability and environmental requirements of this specification.

C.   Gold plate - Gold plating shall be a minimum of 99.7 percent gold (0.3 percent maximum for all impurities and other metals combined). Gold plating shall be a minimum of 50 microinches (12.7 nm) and a maximum of 225 microinches (57.4 nm) thick. Optional electroless or electrolytic nickel or copper underplating, if used, shall be a minimum of 10 microinches (2.54 nm) and a maximum of 100 microinches (25.4 nm) in thickness.

3.5.6. Die Thickness. Unless otherwise specified, the minimum die thickness for all microcircuits shall be 0.006 inch (.15 mm).

3.6. Marking of Microcircuits. Marking shall be in accordance with the requirements of this specification, and the identification and marking provisions of the detail specification or drawing. The marking shall be legible, and complete and shall meet the resistance to solvents requirements of MIL-STD-883, Method 2015. If any special marking is used, it shall in no way interfere with the marking required herein, and shall be visibly separated therefrom. The following marking shall be placed on each microcircuit unless otherwise specified:

A. Index point (3.6.1)
B. Part number
C. Inspection lot identification code (3.6.2)
D. Manufacturer's identification
E. Country of origin (3.6.3)
F. Serialization, when applicable (3.6.4)

3.6.1. Index Point. The index point, tab or other marking indicating the starting point for numbering of leads or for mechanical orientation shall be as specified.

3.6.2. Inspection Lot Identification Code. Microcircuits shall be marked by a unique code to identify the inspection lot (see 3.1.3 (b) and 3.1.3 (c)) and identify the first or the last week of the period (six weeks maximum) during which devices in that inspection lot were sealed. The first two numbers in the code shall be the last two digits of the number of the year, and the third and fourth numbers shall be two digits indicating the calendar week of the year. When the number of the week is a single digit, it shall be preceded by a zero. Reading from left to right or from top to bottom, the code number shall designate the year and week, in that order. When more than one lot of a type is to be identified within the same week, an inspection lot identification suffix letter, representing each lot identified during that week and lettered uniquely shall appear on each microcircuit immediately following the inspection lot data code so that each inspection lot is identified by the inspection lot date code and by the lot identification suffix letter, if one is required.

3.6.3. Country of Origin. The phrase "Made in U.S.A." shall be marked in small characters below or adjacent to the other marking specified, except that for microcircuits made in a foreign country the phrase shall be changed accordingly. If there is limited space, the marking may be shortened to "U.S.A." or to the appropriate accepted abbreviation for the country of origin.

3.6.4. Serialization. Prior to the first recorded electrical measurement in screening, when specified, each microcircuit shall be marked with a unique serial number assigned consecutively within the inspection lot. This serial number allows traceability of test results down to the level of the individual microcircuit within that inspection lot.

3.6.5. Marking Location and Sequence. Unless otherwise specified, the part number, inspection lot identification code, and serialization (where applicable), shall be located on top surface of flat packages or dual-in-line configurations and on either the top or side of cylindrical packages (TO-96 and similar configurations). The index point shall be marked as specified. The balance of the markings may be placed in any suitable location so as to perform their required functions and not interfere with the other markings.

3.6.6. Marking on Initial Container. All of the markings specified in 3.6, except the index point and serialization shall appear on the initial protection or wrapping for delivery (container, carton, box, plastic envelope, etc.) and this marking shall be in accordance with MIL-STD-129.

3.6.7. Marking Option for Controlled Storage. Where microcircuits are subjected to testing and screening in accordance with some portion of the product assurance requirements and stored in controlled storage areas pending receipt of orders requiring conformance to the same or a different level, the inspection lot identification code shall be placed on the microcircuit package along with the other markings specified in 3.6 sufficient to assure identification of the material. As an alternative, if the microcircuits are stored together with sufficient data to assure traceability to processing and inspection records, all markings may be applied after completion of all inspections to the specified level.

3.6.8. Marking Procedure Option. MOSTEK has the option of marking the entire lot or only the sample devices to be submitted to qualification or Groups B, C, and D quality conformance inspection as applicable. If the manufacturer exercises the option to mark only the sample devices, the procedures shall be as follows:

A. The sample devices shall be marked prior to performance of Groups B, C and D quality conformance inspections, as applicable.

B. At the completion of inspection, the marking of the sample devices shall be inspected for conformance with the requirements of 3.6.

C. The inspection lot represented by a conforming inspection sample shall then be marked and any specified visual and mechanical inspection performed.

D. The marking materials and processing applied to the inspection lot shall be to the same specifications as those used for the inspection sample.

3.7. Workmanship. Microcircuits shall be manufactured, processed, and tested in a careful and workman-like manner in accordance with good engineering practice and with the requirements of this specification.

3.7.1. Rework Provisions. All rework permitted on microcircuits procurred under this specification shall be accomplished in accordance with procedures and safeguards documented and available for review. No delidding or package opening for rework shall be permitted for microcircuits of any class. Allowable rework of sealed packages includes recleaning of any microcircuit or portion thereof, rebranding to correct defective marking and lead straightening (provided the reworked devices meet the requirements of 4.6.2 for conditions of leads).

3.7.1.1. Rebonding of Monolithic Devices. Unless otherwise specified, rebonding of monolithic microcircuits shall be permitted with the following limitations:

A. No scratched, open or discontinuous metallization paths or conductor patterns shall be repaired by bridging with or addition of bonding wire or ribbon.

B. All rebonds shall be placed on at least 50% undisturbed metal and no more than one rebond attempt at any design bond location shall be permitted at any pad or post and no rebonds shall be made directly over an area where metallization of intended bond areas has been lifted.

C. The total number of rebond attempts shall be limited to a maximum of 10 percent of the total number of bonds in the microcircuit. The 10 percent limit on rebonds may be interpreted as the nearest whole number of bonds in the microcircuit. A bond shall be defined as a wire to post or wire to pad bond (i.e. for a 14 lead wire bonded package there are 28 bonds). Bond-offs required to clear the bonder after an unsuccessful first bond attempt need not be considered as rebonds provided they can be identified as bond-offs by being made physically off the plated post or if they contain a non-typical number of wedge marks. The initial bond attempt need not be visible. A rebond attempt at one end of the wire counts as one rebond; a replacement of a wire bonded at both ends, or an unsuccessful bond attempt of a wire already bonded at the other end, counts as two rebonds. A bond on top of another bond is not permissible.

4.0 PRODUCT ASSURANCE PROVISIONS

4.1. Safety Requirements - Not Applicable

4.1.1. Responsibility for Tests and Inspections. Unless otherwise specified in the contract or purchase order, MOSTEK is responsible for the performance of all tests and inspection requirements as specified herein and in the detail specification. Except as otherwise specified in the contract or order, the manufacturer may use his own or other suitable facilities.

4.1.2. Inspection During Manufacture. MOSTEK shall establish and maintain inspection at appropriately located points in the manufacturing process in accordance with the procedures described in 20.1.1 of Appendix A of MIL-M-38510 to assure continuous control of quality of materials, subunits and parts during fabrication and testing. This inspection shall be adequate to assure

compliance with the applicable procurement documentation and quality standards for microcircuits manufactured to this specification and the applicable detail specification.

4.1.3. Control and Inspection of Procurement Sources. MOSTEK shall be responsible for assuring that all supplies and services used in the manufacture and test of microcircuits conform to all the requirements of this specification, the detail specification, and other provisions of the applicable procurement documentation.

4.1.4. Inspection Records.

4.1.4. Inspection Records. MOSTEK shall maintain adequate records of all examinations, inspections, and tests accomplished in accordance with 4.0. Records shall be retained as specified in 20.1.2 of Appendix A of MIL-M-38510.

4.2. General Inspection Conditions. The general requirements of MIL-STD-883 shall apply.

4.2.1. Classification of Examinations and Tests. The examinations and tests required to assure conformance to the specified product assurance levels of microcircuits or lots thereof are classified as follows:

Requirement	Paragraph
Quality Conformance Inspection	4.3
Screening	4.4
Data reporting	4.6

4.2.2. Sampling. Statistical sampling for quality conformance inspections shall be in accordance with the sampling procedures of appendix B of MIL-M-38510, and as specified in the detail specification or drawing, as applicable. Reserve sample devices may be tested with the subgroups to provide replacements in the case of test equipment failure or operator error. These devices shall be used in predesignated order.

4.2.2.1. Disposal Of Samples. Devices subjected to destructive tests or which fail any test shall not be shipped on the contract or purchase order as acceptable product. They may, however, be delivered at the request of the procuring activity if they are isolated from, and clearly identified so as to prevent their being mistaken for acceptable product. Sample microcircuits, form lots which have passed product assurance inspections or tests and which have been subjected to mechanical or environmental tests specified in Groups B, C and D inspection and not classified as destructive, may be shipped on the contract or purchase order provided the test has been proved to be nondestructive (see 4.2.2.3) and each of the microcircuits subsequently passes final electrical tests per the applicable device specification.

4.2.2.2. Destructive Tests. Unless otherwise specified, the following MIL-STD-883 tests shall be classified as destructive:

Internal visual and mechanical (Method 2014)
Bond strength.
Solderability.
Moisture resistance.
Lead integrity.
Salt atmosphere.
SEM inspection for metallization.
Steady state life test (accelerated).
Die shear strength test.

All other mechanical or environmental tests (other than those listed in 4.2.2.3), shall be considered destructive initially, but may subsequently be considered nondestructive. The accumulation of data from five repetitions of the specified test on the same sample of product, without evidence of cumulative degradation or failure to pass the specified test

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requirements in any microcircuit in the sample, is considered sufficient evidence that the test is nondestructive. Any test specified as a 100 percent screen shall be considered non-destructive for the stress level and duration or number of cycles applied as a screen.

4.2.2.3. Nondestructive Tests. Unless otherwise specified, the following tests are classified as nondestructive:

Barometric pressure
*Steady state life
*Intermittent life
Seal
External visual
Internal visual (pre-cap)
*Burn-in screen
Radiography

*When the test temperature exceeds the maximum specified junction temperature for the device (including maximum specified for operation or test), these tests shall be considered destructive.

4.2.3. Formation of Lots. Microcircuits shall be segregated into identifiable production lots as defined in 3.1.3(a) as required to meet the production control and inspection requirements of Appendix A of MIL-M-38510. Microcircuits shall be assembled into inspection lots as defined in 3.1.3(b) and 3.1.3(c) as required to meet the product assurance inspection and test requirements of this specification.

4.2.3.1. Resubmission of Failed Lots. Resubmitted lots shall be kept separate from new lots and shall be clearly identified as resubmitted lots. When any lot submitted for quality conformance inspection fails any subgroup requirement of group A, B, C or D tests, it may be resubmitted once for that particular subgroup using tightened inspection criteria (as defined in 30.2.6 of Appendix B of MIL-M-38510). A second resubmission using tightened inspection criteria is permitted only if failure analysis is performed to determine the mechanism of failure for each failed microcircuit from the prior submissions and it is determined that failure(s) is due to:

A.   A defect that can be effectively removed by rescreening the entire lot, or
B.   Random type defects which do not reflect poor basic device design or poor basic processing procedures.
C.   Testing errors resulting in electrical damage to the device.

In all instances where analysis of the failed devices indicates that the failure mechanism is due to poor basic processing procedures, a basic design fault or non-screenable defects, the lot shall not be resubmitted.

4.2.4. Test Method Deviation. Deviations from test methods or tests circuits specified are allowed provided that such deviations in no way relax the requirements of this specification.

4.2.5. Procedure in Case of Test Equipment Failure or Operator Error. Whenever a microcircuit is believed to have failed as a result of faulty test equipment or operator error, the failure shall be entered in the test record which shall be retained for review along with a complete explanation verifying why the failure is believed to be invalid.

4.2.5.1. Procedure for Sample Tests. When it has been established that a failure is due to test equipment failure or operator error and it has been established that the product has not been damaged or degraded, a replacement microcircuit from the same inspection lot may be added to the sample. The replacement microcircuit shall be subject to all those test to which the discarded microcircuit was subjected prior to its failure and to any remaining specified tests to which the discarded microcircuit was not subjected prior to its failure. The manufacturer, at his own risk, has the option of replacing the failed microcircuit and

continuing with the tests before the validity of the test equipment failure or operator error has been established.

4.2.5.2. Procedure for Screening Tests. When it has been established that a lot failure(s) during the screening test(s) is due to operator or equipment error and it has been established that the remaining product has not been damaged or degraded, the lot or surviving portion of the lot, as the case may be, may be resubmitted to the corrected screening test(s) in which the error occurred. Failures verified as having been caused by test equipment failure or operator error shall not be counted in the PDA calculation (when applicable).

4.3. Quality Conformance Inspection.

4.3.1. General. Quality conformance inspection shall be conducted in accordance with the applicable requirements of Groups A, B, C and D of Method 5005, MIL-STD-883, for the specified device class. (See 3.4.1.)

4.3.2. Group A Inspection. Group A inspection shall be performed on each inspection lot in accordance with Method 5005 of MIL-STD-883 and shall consist of electrical parameter tests specified for the specified device class. Group A inspection may be performed in any order. If an inspection lot is made up of a collection of sublots, each sublot shall pass Group A inspection as specified.

4.3.3. Group B Inspection. Group B inspection shall be performed on each inspection lot, for each different package type (i.e. case outline, materials and lead finish), on each different device specification. Group B shall consist of mechanical and environmental tests in accordance with Method 5005 of MIL-STD-883 for the specified device class. Testing of one device type sublot in any subgroup shall be considered as complying with the requirements for that subgroup for all types in the inspection lot. Different device types may be used for each subgroup. A different device type sublot shall be tested for subgroup 2 at each successive Group B inspection until all qualified device types on that detail specification, being submitted for acceptance, have been tested. Except as otherwise specified, this inspection shall be applied only to completed and fully marked devices from lots which have been subjected to and passed the Group A tests.

4.3.3.1. Group B Sample Selection. Samples for Group B subgroups shall be chosen at random from any sublot which has completed the screening requirements of paragraph 4.4 and been submitted to quality conformance inspection (see 30.1.1 of Appendix B of MIL-M-38510).

4.3.4. Group C Inspection. Group C inspection (die related tests) shall be in accordance with Method 5005 of MIL-STD-883 and shall include those tests specified which are performed periodically. Group C tests shall be performed only when specified on the Purchase Order.

4.3.4.1. Group C Sample Selection. Samples for subgroups in Group C shall be chosen at random from any inspection lot of a particular microcircuit group which is submitted to and passes Group A tests for quality conformance inspection during the week in which the first lot of that microcircuit group is submitted in each specified Group C inspection period. Samples from the lot may be subjected to Group C inspection whether or not the specified inspection lot has passed Group B quality conformance inspection. Testing of one device type for each subgroup shall be considered as complying with the requirements for that subgroup for all types on the detail specification(s) within that same microcircuit group. A different device type shall be tested at each successive inspection interval until all device types qualified on the detail specification(s) with the microcircuit group have been tested.

When none of the lots passing Group A during the week in which the first lot is submitted contains the devices type which is due to be tested, the samples for inspection shall be chosen from those types in the lot being tested which have not been used for the longest time for Group C die-related inspection. The next lot submitted which contains the skipped type shall be subjected to Group C inspection as part of its quality conformance inspection. Successful completion of Group C inspection shall initiate a new Group C die-related inspection period. For nonconformance see 4.3.7.

4.3.5. Group D Inspection. Group D inspection (package-related tests) shall be in accordance with Method 5005 of MIL-STD-883 and shall include those package or case-related tests which are performed periodically. The group D tests shall be performed periodically as specified on the Purchase Order for each different package, case or construction.

4.3.5.1. Group D Sample Selection. Samples for subgroups in Group D shall be chosen at random from any inspection lot containing the intended package, case or construction which is submitted to and passes Group A tests for quality conformance inspection during the week in which the first lot containing the intended package is submitted in each Group D inspection period. Testing of a subgroup using a single device type enclosed in the intended package shall be considered as complying with the requirements for that subgroup for all detail specifications utilizing that package. Different types from the inspection lot may be used for each subgroup. Testing of different types on a rotation basis is not required. Successful completion of Group D inspection shall initiate a new group D package-related inspected period. For non conformance see 4.3.7.

4.3.6. End Point Tests for Groups C and D Inspection. Specified post-test parameters shall be measured for each microcircuit for the sample after completion of all other specified tests in the subgroup. Additional measurements may be made at the discretion of the manufacturer.

At the end of each Group C and D subgroup, end point measurements shall include visual examination without magnification to assure marking on each microcircuit tested is legible and complete (see 3.6). Damage to marking caused by mechanical fixturing or handling during tests shall not be cause for lot rejection, but devices so damaged shall be individually remarked or shall be rejected for shipment.

4.3.7. Nonconformance. Samples which fail subgroup requirements of Groups A, B, C, or D may be resubmitted in accordance with the provisions of 4.2.3.1. However, if the lot is not resubmitted or fails the resubmission of 4.2.3.1 the lot shall not be shipped. Samples from subsequent lots of the same microcircuit group for Group C failures or the same package type for Group D failures shall then be subjected to all the tests in the subgroup in which the failure occurred, on a lot-by-lot basis until three successive lots pass the failed subgroup. The testing may then return to periodic testing. A device type which fails a Group C inspection shall not be accepted until the device type which failed successfully completes the failed Group C subgroup(s). No other device types in the group represented by the failed device type may be accepted until the Group C inspection requirements have been satisfied with a device type in the group. A package type which fails a Group D inspection shall not be accepted until the package type which failed successfully completes the failed Group D inspection subgroup(s).

4.4 Screening. Each microcircuit shall have been subjected to and passed all the screening tests detailed in Paragraph 3.4. for the specified product assurance level and type of microcircuit in order to be acceptable for delivery. When a PDA (see 3.1.2(c) or delta limits (see 3.1.2(f)) have been specified or other conditions for lot acceptance have been imposed, the required data shall be recorded and maintained as a basis for lot acceptance. Devices which fail any test criteria in the screening sequence shall be removed from the lot at the time of observation or immediately at the conclusion of the test in which the failure was observed. Once rejected and verified as a device failure, no device may be retested for acceptance.

4.4.1. Burn-in. Burn-in shall be performed on all microcircuits where specified and the specified pre- and post-burn-in electrical parameters shall be measured.

4.4.1.1. Lots Resubmitted for Burn-In. Unless otherwise specified, lots may be resubmitted for burn-in one time only and may be resubmitted only when the observed percentage of parts which were in the original lots. Resubmitted lots shall be kept separate from new lots and shall be inspected for all specified characteristics using a tightened inspection PDA equal to the next lower number in the LTPD series.

4.5. External Visual Screen. The final external visual screen shall be conducted in accordance with Method 2009 of MIL-STD-883 after all other 100 percent screens have been performed to determine that no damage to, or contamination of the package exterior has occurred.

4.6   Data Recording. The results of all quality conformance tests and inspections and the results of all required failure analyses shall be recorded and maintained in the manufacturer's facility.   The disposition of all lots or samples submitted for screening (where PDA is specified), or quality conformance inspection shall be fully documented and lots which fail any specified requirement shall be recorded at failed lots whether resubmitted or withdrawn. Disposition of resubmitted lots shall likewise be recorded so that a complete history is available for every lot tested from initial submission to final disposition including all failures, resubmissions and withdrawals.

4.7.   Inspection of Preparation for Delivery. Sample packages and packs shall be selected and inspected in accordance with MIL-M-55565, or as specified in the contract or order.

5.0 PREPARATION FOR DELIVERY.

5.1 Preservation-packaging and Packing. Microcircuits shall be prepared for delivery in accordance with preservation-packaging and packing conforming to Level A, B or C requirements of MIL-M-55565 unless otherwise specified in the procurement document (see 6.1(e)).

5.1.1.   Packaging and Packing. No packaging or packing material that is used shall crumble, flake, powder or shred. The cushioning material near or in contact with the microcircuits shall not be fibrous in form which might cause the microcircuit leads to be caught and damaged upon removal. Individual microcircuits shall be separated from all others, physically restrained from vibration and mechánically isolated from shock that might cause damage or degradation to the part. Leads must be supported to prevent vibration and retain their shape and position.

5.1.2.   Unit Container. When specified on the detail drawing or purchase order (see 6.1(e)) individual microcircuits shall be supplied mounted in the specified carrier or unit container. Leads must be secured to protect against vibration and retain their shape. Marking on the unit pack, carrier container, or initial contained shall be as specified in 3.6.10.

6.0 NOTES.

6.1 Ordering Data. Procurement documents should specify the following:
A. Part number.
B. Title, number and date of this specification.
C. Title, number and date of applicable detail specification or drawing and identification or the originating design activity.
D. Test data to be furnished.
E. Selection of applicable level of packaging and packing required (see 5.0). Specification of unit container, when applicable (see 5.1), and special marking when applicable.
F. Product assurance level and product assurance options, when applicable (see 3.4)
G. Design documentation to be furnished (see 3.5.4)
H. Lead finish letter when required (see 3.5.5)
I. Requirements for failure analysis, when applicable.
J. Requirements for notification of change (see 3.4.2) to the procuring activity, when applicable.

6.2.   Re-evaluation of Lot Quality. The specified LTPD method is designed for source inspection and provides a high degree of assurance that a lot has a proportion defective no greater than the specified LTPD value. Re-evaluation of any given lot to the same LTPD and acceptance number has the net effect of increasing the probability of rejection or the manufacturer's risk. This is especially true when the initial sampling plan is based on a low acceptance number or when lot re-evaluation is done using a lower acceptance number than was used in the initial sampling plan. Table B-I of Appendix A of MIL-M-38510 provides examples of the approximate quality levels required to satisfy any selected sampling plan. To minimize the effect of re-evaluation on the manufacturer's risk, whenever the quality of a lot is re-evaluated by sampling inspection subsequent to the manufacturer's demonstration of compliance with the quality requirements, the sampling plan shall be based on the next higher acceptance number (for the same LTPD) above that used in the initial lot evaluation. If the initial acceptance number is not known, or if the original inspection was conducted as a screening or 100 percent inspection, then the lot being re-evaluated shall not be rejected using an acceptance number of less than 3. Lots may, however, be accepted on re-evaluation using an acceptance number as low as 0. When deemed necessary, the purchase order may specify detailed criteria for lot re-evaluation and disposition other than the above. Government sources inspection procedures or resubmission of failed lots shall not be considered as re-evaluation of lot quality but rather as a part of the initial quality conformance procedure.

MOSTEK®

4096 x 1-BIT DYNAMIC RAM
Extended Operating Temperature Range (−55°C to +85°C)

MK4027(P)-83/84

FEATURES

☐ Extended operating temperature range
(−55° ≤ T$_A$ ≤ +85°C)

☐ Industry standard 16-pin DIP (MK 4096) configuration

☐ 200ns access time, 375ns cycle
250ns access time, 375ns cycle

☐ ±10% tolerance on all supplies (+12V, ±5V)

☐ Low Power: 467 mW active (max)
40 mW standby (max)

☐ Improved performance with "gated $\overline{CAS}$", "$\overline{RAS}$ only" refresh and page mode capability

☐ All inputs are low capacitance and TTL compatible

☐ Input latches for addresses, chip select and data in

☐ Three-state TTL compatible output

☐ Output data latched and valid into next cycle

DESCRIPTION

The MK 4027 is a 4096 word by 1 bit MOS random access memory circuit fabricated with MOSTEK's N-channel silicon gate process. This process allows the MK 4027 to be a high performance state-of-the-art memory circuit that is manufacturable in high volume. The MK 4027 employs a single transistor storage cell utilizing a dynamic storage technique and dynamic control circuitry to achieve optimum performance with low power dissipation.

A unique multiplexing and latching technique for the address inputs permits the MK 4027 to be packaged in a standard 16-pin DIP on 0.3 in. centers. This package size provides high system-bit densities and is compatible with widely available automated testing and insertion equipment.

System oriented features include direct interfacing capability with TTL, only 6 very low capacitance address lines to drive, on-chip address and data registers which eliminates the need for interface registers, input logic levels selected to optimize noise immunity, and two chip select methods to allow the user to determine the appropriate speed/power characteristics of his memory system. The MK 4027 also incorporates several flexible operating modes. In addition to the usual read and write cycles, read-modify write, page-mode, and $\overline{RAS}$-only refresh cycles are available with the MK 4027. Page-mode timing is very useful in systems requiring Direct Memory Access (DMA) operation.

FUNCTIONAL DIAGRAM

PIN CONNECTIONS

V$_{BB}$	1	16	V$_{SS}$
D$_{IN}$	2	15	$\overline{CAS}$
$\overline{WRITE}$	3	14	D$_{OUT}$
$\overline{RAS}$	4	13	$\overline{CS}$
A$_0$	5	12	A$_3$
A$_2$	6	11	A$_4$
A$_1$	7	10	A$_5$
V$_{DD}$	8	9	V$_{CC}$

PIN NAMES

A$_0$-A$_5$	ADDRESS INPUTS
$\overline{CAS}$	COLUMN ADDRESS STROBE
$\overline{CS}$	CHIP SELECT
D$_{IN}$	DATA IN
D$_{OUT}$	DATA OUT
$\overline{RAS}$	ROW ADDRESS STROBE
$\overline{WRITE}$	READ/WRITE INPUT
V$_{BB}$	POWER (−5V)
V$_{CC}$	POWER (+5V)
V$_{DD}$	POWER (+ 12V)
V$_{SS}$	GROUND

HI-REL 4K DYN RAM
MK4027(P) 83/84

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to V_{BB} . . . . −0.5V to +20V
Voltage on V_{DD}, V_{CC} relative to V_{SS} . . . . −1.0V to +15V
V_{BB}−V_{SS} (V_{DD}−V_{SS} > 0) 0V
Operating temperature, T_A (Ambient) . . . . −55°C to + 85°C
Storage temperature (Ambient)(Ceramic) . . . . −65°C to + 150°C
Short Circuit Output Current 50mA
Power dissipation . . . . 1 Watt

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS [4]
(−55°C ≤ T_A ≤ 85°C)

	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{DD}	Supply Voltage	10.8	12.0	13.2	volts	2
V_{CC}	Supply Voltage	4.5V	5.0	5.5	volts	2,3
V_{SS}	Supply Voltage	0	0	0	volts	2
V_{BB}	Supply Voltage	−4.5	−5.0	−5.5	volts	2
V_{IHC}	Logic 1 Voltage, $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	2.7		7.0	volts	2
V_{IH}	Logic 1 Voltage, all inputs except $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	2.7		7.0	volts	2
V_{IL}	Logic 0 Voltage, all inputs	−1.0		.8	volts	2

DC ELECTRICAL CHARACTERISTICS [4]
(−55°C ≤ T_A ≤ 85°C)[1] (V_{DD} = 12.0V ± 10%; V_{CC} = 5.0V ± 10%; V_{SS} = 0V; V_{BB} = −5.0V ± 10%)

	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
I_{DD1}	Average V_{DD} Power Supply Current			35	mA	5
I_{DD2}	Standby V_{DD} Power Supply Current			3.0	mA	8
I_{DD3}	Average V_{DD} Power Supply Current during "$\overline{RAS}$ only" cycles			27	mA	
I_{CC}	V_{CC} Power Supply Current				mA	6
I_{BB}	Average V_{BB} Power Supply Current			200	μA	
$I_{I(L)}$	Input Leakage Current (any input)			10	μA	7
$I_{O(L)}$	Output Leakage Current			10	μA	8,9
V_{OH}	Output Logic 1 Voltage @ I_{OUT} = −5mA	2.4			volts	
V_{OL}	Output Logic 0 Voltage @ I_{OUT} = 3.2mA			0.4	volts	

NOTES

1. T_A is specified for operation at frequencies to t_{RC} ≥ t_{RC} (min). Operation at higher cycle rates with reduced ambient temperatures and higher power dissipation is permissible provided that all AC parameters are met.

2. All voltages referenced to V_{SS}.

3. Output voltage will swing from V_{SS} to V_{CC} when enabled, with no output load. For purposes of maintaining data in standby mode, V_{CC} may be reduced to V_{SS} without affecting refresh operations or data retention. However, the V_{OH} (min) specification is not guaranteed in this mode.

4. Several cycles are required after power-up before proper device operation is achieved. Any 8 cycles which perform refresh are adequate for this purpose.

5. Current is proportional to cycle rate. I_{DD1} (max) is measured at the cycle rate specified by t_{RC} (min). See figure 1 for I_{DD1} limits at other cycle rates.

6. I_{CC} depends on output loading. During readout of high level data V_{CC} is connected through a low impedance (135Ω typ) to Data Out. At all other times I_{CC} consists of leakage currents only.

7. All device pins at 0 volts except V_{BB} which is at −5 volts and the pin under test which is at +10 volts.

8. Output is disabled (high-impedance) and $\overline{RAS}$ and $\overline{CAS}$ are both at a logic 1. Transient stabilization is required prior to measurement of this parameter.

9. 0V ≤ V_{OUT} ≤ + 10V.

10. Effective capacitance is calculated from the equation:

$$C = \frac{\Delta Q}{\Delta V} \text{ with } \Delta V = 3 \text{ volts.}$$

11. A.C. measurements assume t_T = 5ns.

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (4,11,17)

($-55°C \leqslant T_A \leqslant 85°C$) [1] ($V_{DD}$ = 12.0V ± 10%, V_{CC} = 5.0V ± 10%, V_{SS} = 0V, V_{BB} = −5.0V ± 10%)

	PARAMETER	MK4027-83 MIN	MK4027-83 MAX	MK4027-84 MIN	MK4027-84 MAX	UNITS	NOTES
t_{RC}	Random read or write cycle time	375		380		ns	12
t_{RWC}	Read write cycle time	375		395		ns	12
t_{RMW}	Read Modify Write Cycle	405		470		ns	12
t_{PC}	Page mode cycle time	225		285		ns	12
t_{RAC}	Access time from row address strobe		200		250	ns	13,15
t_{CAC}	Access time from column address strobe		135		165	ns	14,15
t_{OFF}	Output buffer turn-off delay		50		60	ns	
t_{RP}	Row address strobe precharge time	120		120		ns	
t_{RAS}	Row address strobe pulse width	200	5,000	250	5,000	ns	
t_{RSH}	Row address strobe hold time	135		165		ns	
t_{CAS}	Column address strobe pulse width	135		165		ns	
t_{CSH}	$\overline{CAS}$ hold time	200		250		ns	
t_{RCD}	Row to column strobe delay	25	65	35	85	ns	16
t_{ASR}	Row address set-up time	0		0		ns	
t_{RAH}	Row address hold time	25		35		ns	
t_{ASC}	Column address set-up time	0		0		ns	
t_{CAH}	Column address hold time	55		75		ns	
t_{AR}	Column address hold time referenced to $\overline{RAS}$	120		160		ns	
t_{CSC}	Chip select set-up time	0		0		ns	
t_{CH}	Chip select hold time	55		75		ns	
t_{CHR}	Chip select hold time referenced to $\overline{RAS}$	120		160		ns	
t_T	Transition time (rise and fall)	3	50	3	50	ns	17
t_{RCS}	Read command set-up time	0		0		ns	
t_{RCH}	Read command hold time	0		0		ns	
t_{WCH}	Write command hold time	55		75		ns	
t_{WCR}	Write command hold time referenced to $\overline{RAS}$	120		160		ns	
t_{WP}	Write command pulse width	55		75		ns	
t_{RWL}	Write command to row strobe lead time	70		85		ns	
t_{CWL}	Write command to column strobe lead time	70		85		ns	
t_{DS}	Data in set-up time	0		0		ns	18
t_{DH}	Data in hold time	55		75		ns	18
t_{DHR}	Data in hold time referenced to $\overline{RAS}$	120		160		ns	
t_{CRP}	Column to row strobe precharge time	0		0		ns	
t_{CP}	Column precharge time	80		110		ns	
t_{RFSH}	Refresh period		2		2	ms	
t_{WCS}	Write command set-up time	0		0			19
t_{CWD}	$\overline{CAS}$ to $\overline{WRITE}$ delay	80		90		ns	19
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ delay	145		175		ns	19
t_{DOH}	Data out hold time	5		5		μs	

Notes Continued

12. The specifications for t_{RC} (min) and t_{RWC} (min) are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \leqslant T_A \leqslant 70°C$) is assured. See figure 2 for derating curve.

13. Assumes that $t_{RCD} \leqslant t_{RCD}$ (max).

14. Assumes that $t_{RCD} \geqslant t_{RCD}$ (max).

15. Measured with a load circuit equivalent to 2 TTL loads and 100pF

16. Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.

17. V_{IHC} (min) or V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IHC} or V_{IH} and V_{IL}.

18. These parameters are referenced to $\overline{CAS}$ leading edge in random write cycles and to $\overline{WRITE}$ leading edge in delayed write or read-modify-write cycles.

19. t_{WCS}, t_{CWD}, and t_{RWD} are restrictive operating parameters in a read/write or read/modify/write cycle only. If $t_{WCS} \geqslant t_{WCS}$ (min), the cycle is an early write cycle and Data Out will contain the data written into the selected cell. If $t_{CWD} \geqslant t_{CWD}$ (min) and $t_{RWD} \geqslant t_{RWD}$ (min), the cycle is a read-write cycle and Data Out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of Data Out (at access time) is indeterminate.

AC ELECTRICAL CHARACTERISTICS
$(-55\,°C \leqslant T_A \leqslant 85\,°C)$ $(V_{DD} = 12.0V \pm 10\%; V_{SS} = 0V; V_{BB} = -5.0V \pm 10\%)$

	PARAMETER	TYP	MAX	UNITS	NOTES
C_{I1}	Input Capacitance $(A_0\text{-}A_5)$, D_{IN}, $\overline{CS}$	4	5	pF	10
C_{I2}	Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	8	10	pF	10
C_0	Output Capacitance (D_{OUT})	5	7	pF	8,10

Supplemental data to be used in conjunction with the Mostek MK4027(P/J/N)-1/2/3/4.

MOSTEK®

4096 x 1-BIT STATIC RAM
Extended Operating Temperature (−55°C to +125°C)
MK4104(P)-85/86

FEATURES

☐ Combination static storage cells and dynamic control circuitry for truly high performance

Part Number	Access Time	Cycle Time
4104(P)-85	300ns	510ns
4104(P)-86	350ns	610ns

☐ Average Power Dissipation less than 110 mW

☐ Standby Power Dissipation less than 53 mW/

☐ Single +5V Power Supply (5% tolerance)

☐ Fully TTL Compatible
Fanout: 2 − Standard TTL
2 − Schottky TTL
12 − Low Power Schottky TTL

☐ Standard 18-pin DIP

DESCRIPTION

The MOSTEK MK 4104 is a high performance static random access memory organized as 4096 one bit words. The MK 4104 combines the best characteristics of static and dynamic memory techniques to achieve a TTL compatible, 5 volt only, high performance, low power memory device. It utilizes advanced circuit design concepts and an innovative state-of-the-art N-channel silicon gate process specially tailored to provide static data storage with the performance (speed and power) of dynamic RAMs. Since the storage cell is static the device may be stopped indefinitely with the $\overline{CE}$ clock in the off (Logic 1) state.

All input levels, including write enable ($\overline{WE}$) and chip enable ($\overline{CE}$) are TTL with a one level of 2.4 volts and a zero level of .65 volts. The push-pull output (no pull-up resistor required) delivers a one level of 2.4V minimum and a zero level of .4 volts maximum. The output has a fanout of 2 standard TTL loads or 12 low power Schottky loads.

The RAM employs an innovative static cell which occupies a mere 2.75 square mils (½ the area of previous cells) and dissipates power levels comparable to CMOS. The static cell eliminates the need for refresh cycles and associated hardware thus allowing easy system implementation.

Power supply requirement of +5V combined with TTL compatability on all I/O pins permits easy integration into large memory configurations. The single supply reduces capacitor count and permits denser packaging on printed circuit boards. The 5V only supply requirement and TTL compatible I/O makes this part an ideal choice for next generation +5V only microprocessors such as MOSTEK's Z80 and MK3870. The early write mode ($\overline{WE}$ active prior to $\overline{CE}$) permits common I/O operation, needed for Z80 interfacing, without external circuitry.

Reliability is greatly enhanced by the low power dissipation which causes a maximum junction rise of only 6.6°C at 1.6 Megahertz operation. The MK4104 was designed for the system designer and user who require the highest performance available along with MOSTEK's proven reliability.

FUNCTIONAL DIAGRAM
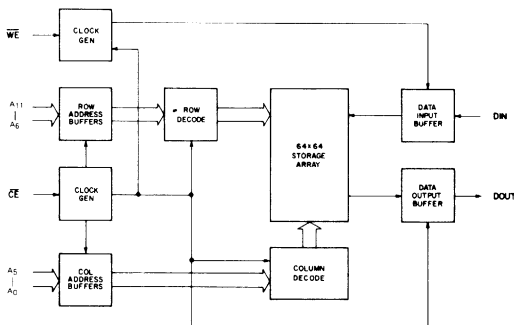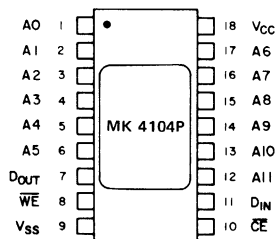
PIN CONNECTIONS

PIN NAMES

$A_0 \cdot A_{11}$	ADDRESS INPUTS	V_{SS}	GROUND
$\overline{CE}$	CHIP ENABLE	V_{CC}	POWER (+5V)
D_{IN}	DATA INPUT	$\overline{WE}$	WRITE ENABLE
D_{OUT}	DATA OUTPUT		

4096x1-BIT STATIC RAM
MK4104(P)-85/86

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ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to V_{SS} . . . . −0.5V to + 7.0V

Operating Temperature T_A (Ambient) . . . . −55°C to 125°C

Storage Temperature (Ambient) (Ceramic) . . . . −65°C to +150°C

Power Dissipation . . . . 1 Watt

Short Circuit Output Current 50mA

RECOMMENDED DC OPERATING CONDITIONS[6]
($-55°C \leqslant T_A \leqslant +125°C$)

	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.75	5.0	5.25	Volts	1
V_{SS}	Supply Voltage	0	0	0	Volts	1
V_{IH}	Logic "1" Voltage All Inputs	2.4		7.0	Volts	1
V_{IL}	Logic "0" Voltage All Inputs	−0.5		.65	Volts	1

DC ELECTRICAL CHARACTERISTICS
($-55°C \leqslant T_A \leqslant +125°C$) ($V_{CC}$ = 5.0 volts ± 5%)

	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC1}	Average V_{CC} Power Supply Current		21	mA	2
I_{CC2}	Standby V_{CC} Power Supply Current		10	mA	3
I_{IL}	Input Leakage Current (Any Input)	−10	10	μA	4
I_{OL}	Output Leakage Current	−10	10	μA	3, 5
V_{OH}	Output Logic "1" Voltage I_{OUT}=−500μA	2.4		Volts	11
V_{OL}	Output Logic "0" Voltage I_{OUT}= 5mA		0.4	Volts	11

AC ELECTRICAL CHARACTERISTICS
($-55°C \leqslant T_A \leqslant +125°C$) ($V_{CC}$ = + 5.0 volts ± 5%)

	PARAMETER	MIN	TYP	MAX	NOTES
C_I	Input Capacitance		4pF		14
C_0	Output Capacitance		7pF		14

NOTES:

1. All voltages referenced to V_{SS}.

2. I_{CC1} is related to precharge and cycle times. Guaranteed maximum values for I_{CC1} are at minimum cycle time.

3. Output is disabled (open circuit), $\overline{CE}$ is at logic 1.

4. All device pins at 0 volts except pin under test at $0 \leqslant V_{IN} \leqslant 5.5V$

5. $0V \leqslant V_{OUT} \leqslant + 5.5V$.

6. During power up, $\overline{CE}$ and $\overline{WE}$ must be at V_{IH} for minimum of 2ms after V_{CC} reaches 4.5V, before a valid memory cycle can be accomplished.

7. Measured with load circuit equivalent to 2 TTL loads and CL = 100 pF.

8. If WE follows after $\overline{CE}$ by more than $\overline{t_{WS}}$, then data out may not remain open circuited.

9. Determined by user. Total cycle time cannot exceed t_{CE} max.

10. Data-in set-up time is referenced to the later of the two falling clock edges $\overline{CE}$ or $\overline{WE}$.

11. AC measurements assume t_T = 5ns. Timing points are taken as V_{IL} = .65V and V_{IH} = 2.4V on the inputs and V_{OL} = 0.4V and V_{OH} = 2.4V on the output waveform.

12. $t_C = t_{CE} + t_P + 2t_T$.

13. The true level of the output in the open circuit condition will be determined totally by output load conditions. The output is guaranteed to be open circuit within t_{OFF}.

14. Effective capacitance calculated from the equation $C = I \frac{\Delta t}{\Delta V}$ with ΔV equal to 3V and V_{CC} nominal.

15. For RMW, $t_{CE} = t_{AC} + t_{WPL} + t_{MOD}$.

16. $t_C = t_{AC} + t_{WPL} + t_P + 3t_T + t_{MOD}$.

AC ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS[6, 11]
$(-55°C \leqslant T_A \leqslant +125°C)$ $(V_{CC} = +5.0 \text{ Volts} \pm 5\%)$

	PARAMETER	MK4104-85 MIN	MK4104-85 MAX	MK4104-86 MIN	MK4104-86 MAX	UNIT	NOTES
t_C	Read or Write Cycle Time	510		610		ns	12
t_{AC}	Random Access		300		350	ns	7
t_{CE}	Chip Enable Pulse Width	300	5000	350	5000	ns	15
t_P	Chip Enable Precharge Time	200		250		ns	
t_{AH}	Address Hold Time	165		190		ns	
t_{AS}	Address Set-Up Time	0		0		ns	
t_{OFF}	Output Buffer Turn-Off Delay	0	75	0	100	ns	13
t_{WS}	Write Enable Set-Up Time	0		0		ns	8
t_{DHC}	Data Input Hold Time Referenced to $\overline{CE}$	250		285		ns	
t_{DHW}	Data Input Hold Time Referenced to $\overline{WE}$	105		125			
t_{WW}	Write Enabled Pulse Width	90		105		ns	
t_{MOD}	Modify Time	0	5000	0	5000	ns	9
t_{WPL}	$\overline{WE}$ to $\overline{CE}$ Precharge Lead Time	105		120		ns	10
t_{DS}	Data Input Set-Up Time	0		0		ns	
t_{WH}	Write Enable Hold Time	225		260		ns	
t_T	Transition Time	5	50	5	50	ns	
t_{RMW}	Read-Modify-Write Cycle Time	620		735		ns	16
t_{RS}	Read Set-Up Time	0		0		ns	

Supplemental data to be used in conjunction with the Mostek MK4104(P/N)Series data sheet.

MOSTEK®

4096 x1-BIT DYNAMIC RAM
Extended Operating Temperature Range (−55°C to +85°C)

MK4096(K)-77/86/85

FEATURES

☐ Industry standard 16-pin DIP configuration (available in hermetic ceramic (K) package only)

☐ Extended operating temperature range (−55°C to + 85°C)

☐ All inputs are low capacitance and TTL compatible

☐ Input latches for address, chip select and data in

☐ Inputs protected against static charge

☐ Three-state TTL compatible output, latched and valid into next cycle

☐ Proven reliability with high performance

Part Number	Access Time	Cycle Time	Max Power*
MK 4096−77	250 ns	375 ns	570mW
MK 4096−86	300 ns	425 ns	500mW
MK 4096−85	350 ns	500 ns	450mW

*Standby power for all parts < 27mW

DESCRIPTION

The MK 4096 is the recognized industry standard 4096 word by 1 bit MOS Random Access Memory circuit packaged in a standard 16-pin DIP on 0.3 inch centers. This package configuration is made possible by a unique multiplexing and latching technique for the address inputs. The use of the 16-pin DIP for the MK 4096 provides high system bit densities and is compatible with widely available automated testing and insertion equipment.

The MK 4096 is fabricated with MOSTEK's standard Self-Aligned, Poly-Interconnect, N-Channel (SPIN) process. The SPIN process allows the MK 4096 to be a highly manufacturable, state-of-the-art memory circuit that exhibits the reliability and performance

standards necessary for today's (and tomorrow's) data processing applications. The MK 4096 employs a single transistor storage cell, utilizing a dynamic storage technique and dynamic control circuitry to achieve optimum performance with low power dissipation.

System oriented features incorporated within the MK 4096 include direct interfacing capability with TTL, 6 instead of 12 address lines to drive, on-chip registers which can eliminate the need for interface registers, input logic levels selected to optimize the noise immunity, and two chip select methods to allow the user to determine the speed/power characteristics of his memory system.

FUNCTIONAL DIAGRAM

PIN CONNECTIONS

PIN NAMES

A_0 - A_5	ADDRESS INPUTS	D_{IN}	DATA IN
$\overline{CAS}$	COLUMN ADDRESS STROBE	D_{OUT}	DATA OUT
$\overline{CS}$	CHIP SELECT	V_{BB}	POWER (−5V)
$\overline{RAS}$	ROW ADDRESS STROBE	V_{CC}	POWER (+5V)
$\overline{WRITE}$	READ/WRITE INPUT	V_{DD}	POWER (+12V)
		V_{SS}	GROUND

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to V_{BB} .... −0.5V to + 25V
(V_{SS}−V_{BB} ⩾ 4.5V)
Operating temperature T_A (Ambient). . −55°C to + 85°C
Storage temperature (Ceramic) . . . . . . −65°C to + 150°C
Power dissipation 1Watt
Data out current 50mA

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS (17)
(-55°C ⩽ T_A ⩽ + 85°C)

	PARAMETER	MK 4096K−77 MIN	MAX	MK 4096K−86 MIN	MAX	MK 4096K−85 MIN	MAX	UNITS	NOTES
V_{DD}	Supply Voltage	11.4	12.6	11.4	12.6	11.4	12.6	Volts	1
V_{CC}	Supply Voltage	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V_{SS}	V_{DD}	Volts	1,2
V_{SS}	Supply Voltage	0	0	0	0	0	0	Volts	1
V_{BB}	Supply Voltage	−4.5	−5.5	−4.5	−5.5	−4.5	−5.5	Volts	1
V_{IHC}	Logic 1 Voltage − $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	2.7	7.0	2.7	7.0	3.0	7.0	Volts	1,3
V_{IH}	Logic 1 Voltage, all inputs except $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	2.4	7.0	2.4	7.0	2.4	7.0	Volts	1,3
V_{IL}	Logic 0 Voltage, all inputs	−1.0	0.8	−1.0	0.8	−1.0	0.8	Volts	1,3

DC ELECTRICAL CHARACTERISTICS (17)
(-55°C ⩽ T_A ⩽ + 85°C)(V_{DD} = 12.0V ± 5%; V_{CC} = 5.0V ± 10%; V_{SS} = 0V; V_{BB} = −5.0V ±10%)

	PARAMETER	MK4096K-77 MIN	MAX	MK4096K-86 MIN	MAX	MK4096K-85 MIN	MAX	UNITS	NOTES
I_{DD1}	Average V_{DD} Power Supply Current		45		40		35	mA	4
I_{CC}	V_{CC} Power Supply Current							mA	5
I_{BB}	Average V_{BB} Power Supply Current		75		75		75	μA	
I_{DD2}	Standby V_{DD} Power Supply Current		2		2		2	mA	7
I_{DD3}	Average V_{DD} Supply Current during "$\overline{RAS}$-only" cycles		35		30		25	mA	4
$I_{I(L)}$	Input Leakage Current (any input)		5		5		5	μA	6
$I_{O(L)}$	Output Leakage Current		10		10		10	μA	7,8
V_{OH}	Output Logic 1 Voltage @ I_{OUT} = −5mA	2.4		2.4		2.4		Volts	2
V_{OL}	Output Logic 0 Voltage @ I_{OUT} = 2mA		0.4		0.4		0.4	Volts	

NOTES

1. All voltages referenced to V_{SS}. V_{BB} must be applied to and removed from the device within 5 seconds of V_{DD}.

2. Output voltage will swing from V_{SS} to V_{CC} if V_{CC} ⩽ V_{DD} −4 volts. If V_{CC} ⩾ V_{DD} −4 volts, the output will swing from V_{SS} to a voltage somewhat less than V_{DD}.

3. Device speed is not guaranteed at input voltages greater than TTL levels (0 to 5V).

4. Current is proportional to cycle rate; maximum current is measured at the fastest cycle rate.

5. I_{CC} depends upon output loading. The V_{CC} supply is connected to the output buffer only.

6. All device pins at 0 volts except V_{BB} which is at −5 volts and the pin under test which is at +10 volts.

7. Output is disabled (open-circuit) and $\overline{RAS}$ and $\overline{CAS}$ are both at a logic 1.

8. 0V ⩽ V_{OUT} ⩽ +10V.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (10, 15, 17)
($-55°C \leqslant T_A \leqslant +85°C$) ($V_{DD} = 12.0V \pm 5\%$, $V_{CC} = 5.0V \pm 10\%$, $V_{SS} = 0V$, $V_{BB} = -5.0V \pm 10\%$)

	PARAMETER	MK4096K-77		MK4096K-86		MK4096K-85		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX		
t_{RC}	Random Read or Write Cycle Time	375		425		500		nsec	11
t_{RAC}	Access time from Row Address Strobe		250		300		350	ns	11,13
t_{CAC}	Access Time from Column Address Strobe		140		165		200	ns	12,13
t_{OFF}	Output Buffer Turn-Off Delay	0	65	0	80	0	100	ns	
t_{RP}	Row Address Strobe Precharge Time	115		125		150		ns	
t_{RAS}	Row Address Strobe Pulse Width	250	10,000	300	10,000	350	10,000	ns	
t_{RCL}	Row To Column Strobe Lead Time	60	110	80	135	100	150	ns	14
t_{CAS}	Column Address Strobe Pulse Width	140		165		200		ns	12
t_{AS}	Address Set-Up Time	0		0		0		ns	
t_{AH}	Address Hold Time	60		80		100		ns	
t_{CH}	Chip Select Hold Time	100		100		100		ns	
t_{T}	Rise and Fall Times	3	50	3	50	3	50	ns	15
t_{RCS}	Read Command Set-Up Time	0		0		0		ns	
t_{RCH}	Read Command Hold Time	0		0		0		ns	
t_{WCH}	Write Command Hold Time	110		130		150		ns	
t_{WP}	Write Command Pulse Width	110		130		150		ns	
t_{CRL}	Column to Row Strobe Lead Time	-40	$+40$	-50	$+50$	-50	$+50$	ns	
t_{CWL}	Write Command to Column Strobe Lead Time	110		130		150		ns	
t_{DS}	Data In Set-Up Time	0		0		0		ns	16
t_{DH}	Data In Hold Time	110		130		150		ns	16
t_{RFSH}	Refresh Period		2		2		2	msec	
t_{MOD}	Modify Time		10		10		10	μsec	
t_{DOH}	Data Out Hold Time	10		10		10		μsec	

<div style="text-align: right">**HI-REL 4K DYN RAM**</div>

NOTES Continued

9. Capacitance measured with Boonton Meter or effective capacitance calculated from the equation: $C = \frac{I \triangle t}{\triangle V}$ with current equal to a constant 20mA.

10. A C measurements assume $t_T = 5$ns.

11. Assumes that $t_{RCL} + t_T \leqslant t_{RCL}$ (max).

12. Assumes that $t_{RCL} + t_T \geqslant t_{RCL}$ (max).

13. Measured with a load circuit equivalent to 1 TTL load and $C_L = 100$pF

14. Operation within the t_{RCL} (max) limit insures that t_{RAC} (max) can be met. t_{RCL} (max) is specified as a reference point only; if t_{RCL} is greater than the specified t_{RCL} (max) limit, then access time is controlled exclusively by t_{CAC} and t_{RAS}, t_{RAC} and t_{RCL} will be longer by the amount $t_{RCL} + t_T$ exceeds t_{RCL} (max).

15. V_{IHC} (min) or V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IHC} or V_{IH} and V_{IL}.

16. These parameters are referenced to $\overline{CAS}$ leading edge in random write cycles and to $\overline{WRITE}$ leading edge in delayed write or read-modify-write cycles.

17. After the application of supply voltages or after extended periods of operation without clocks, the device must perform a minimum of one initialization cycle (any valid memory cycle containing both $\overline{RAS}$ and $\overline{CAS}$) prior to normal operation.

AC ELECTRICAL CHARACTERISTICS

$(-55°C \leqslant T_A \leqslant +85°C)$ $(V_{DD} = 12.0V \pm 5\%; V_{CC} = 5.0V \pm 10\%, V_{SS} = 0V, V$ — $-5.0V \pm 10\%)$

	PARAMETER	TYP	MAX	UNITS	NOTES
C_{I1}	Input Capacitance ($A_0 - A_5$)	7	10	pF	9
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, D_{IN}, $\overline{WRITE}$, $\overline{CS}$)	5	7	pF	9
C_0	Output Capacitance (D_{OUT})	5	8	pF	7,9

Supplemental data to be used in conjunction with the Mostek MK4096(K)-6/16/11.

MOSTEK®

16K-BIT MOS READ ONLY MEMORY
Extended Operating Temperature Range
MK34000(P)-84

FEATURES

☐ 2K x 8 organization with static interface

☐ 450 ns max access time

☐ Single +5V ± 10% power supply

☐ 550mW max power dissipation

☐ Extended operating temperature range
$-55°C \leqslant T_A \leqslant 125°C$

☐ Contact programmed for fast turn-around

☐ Three programmable chip selects

☐ Inputs and three-state outputs — TTL compatible

☐ Outputs drive 1 TTL load and 100pF

DESCRIPTION

The MK 34000 is a new generation N-channel silicon gate MOS Read Only Memory circuit organized as 2048 words by 8 bits. As a state-of-the-art device, the MK 34000 incorporates advanced circuit techniques designed to provide maximum circuit density and reliability with highest possible performance, while maintaining low power dissipation and wide operating margins.

The MK 34000 requires a single +5 volt (± 10% tolerance) power supply and has complete TTL compatibility at all inputs and outputs (a feature made possible by MOSTEK's Ion-implantation technique). The three chip select inputs can be programmed for any desired combination of active high's or low's or even an optional "DON'T CARE" state. The convenient static operation of the MK 34000 coupled with the programmable chip select inputs and three-state TTL compatible outputs results in extremely simple interface requirements.

An outstanding feature of the MK 34000 is the use of contact programming over gate mask programming. Since the contact mask is applied at a later processing stage, wafers can be partially processed and stored. When an order is received, a contact mask, which represents the desired bit pattern, is generated and applied to the wafers. Only a few processing steps are left to complete the part. Therefore, the use of contact programming reduces the turnaround time for a custom ROM.

Any application requiring a high performance, high bit density ROM can be satisfied by this device. The MK 34000 is ideally suited for 8-bit microprocessor systems such as those which utilize the Z80 or F8. The MK 34000 also provides significant cost advantages over PROM.

FUNCTIONAL DIAGRAM

PIN CONNECTIONS

*Programmable Chip Selects

HI-REL 16K ROM

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Terminal Relative to Ground . . . . −0.5V to + 7V

Operating Temperature T$_A$ (Ambient) . . . . −55 °C to +125 °C

Storage Temperature − Ceramic (Ambient) . . . . −65°C to + 150°C

Power Dissipation . . . . 1 Watt

RECOMMENDED DC OPERATING CONDITIONS [6]
(V$_{CC}$ = 5V ± 10%; −55°C ⩽ TA ⩽ +125°C)

	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V$_{CC}$	Power Supply Voltage	4.5	5.0	5.5	Volts	6
V$_{IL}$	Input Logic 0 Voltage	−0.5		0.8	Volts	
V$_{IH}$	Input Logic 1 Voltage	2.2		V$_{CC}$	Volts	

D C ELECTRICAL CHARACTERISTICS
(V$_{CC}$ = 5V ± 10%; −55°C⩽TA⩽+125°C)[6]

	PARAMETER	MIN	MAX	UNITS	NOTES
I$_{CC}$	V$_{CC}$ Power Supply Current		100	mA	1
I$_{I(L)}$	Input Leakage Current		10	μA	2
I$_{O(L)}$	Output Leakage Current		10	μA	3
V$_{OL}$	Output Logic 0 Voltage @ I$_{OUT}$ = 2.0mA		0.4	volts	
V$_{OH}$	Output Logic 1 Voltage @ I$_{OUT}$ = − 220 μA	2.4	V$_{CC}$	volts	

A C ELECTRICAL CHARACTERISTICS
(V$_{CC}$ = 5V ± 10%; −55°C⩽TA⩽+125°C)[6]

	PARAMETER	MIN	MAX	UNITS	NOTES
t$_{ACC}$	Address to output delay time		450	ns	4
t$_{CS}$	Chip select to output delay time		250	ns	4
t$_{CD}$	Chip deselect to output delay time		200	ns	4

CAPACITANCE

	PARAMETER	TYP	MAX	UNITS	NOTES
C$_{IN}$	Input Capacitance	6	8	pF	5
C$_{OUT}$	Output Capacitance	10	15	pF	5

NOTES:

1. All inputs 5.5V; Data Outputs open.
2. V$_{IN}$ = 0V to 5.5V
3. Device unselected; V$_{OUT}$ = 0V to 5.5V.
4. Measured with 1 TTL load and 100pF, transition times = 20ns

5. Capacitance measured with Boonton Meter or effective capacitance calculated from the equation :
$$C = \frac{I \triangle t}{\triangle V} \text{ with current equal to a constant 20mA.}$$
6. A minimum 250 μs time delay is required after the application of V$_{CC}$ (+5) before proper device operation is achieved.

ADDRESS

PROGRAMMABLE CHIP SELECTS

DATA OUTPUT

* The chip select inputs can be user programmed so that either the input is enabled by a Logic 0 voltage (V_{IL}), a Logic 1 voltage (V_{IH}), or the input is always enabled (regardless of the state of the input). See chart below for programming instructions.

MOSTEK 34000 ROM PUNCHED CARD CODING FORMAT [1]

FIRST CARD

COLS	INFORMATION FIELD
1-30	Customer
31-50	Customer Part Number
60-72	MOSTEK Part Number (2)

SECOND CARD

1-30	Engineer at Customer Site
31-50	Direct Phone Number for Engineer

THIRD CARD

1-5	MOSTEK Part Number (2)
33	Chip Select One "1" = CS$_1$ or "0" = $\overline{CS_1}$ or "2" = Don't Care
35	Chip Select Two "1" = CS$_2$ or "0" = $\overline{CS_2}$ or "2" = Don't Care
37	Chip Select Three "1" = CS$_3$ or "0" = $\overline{CS_3}$ or "2" = Don't Care

FOURTH CARD

1-9	Data Format (3)
15-28	Logic - ("Positive Logic" or "Negative Logic")
35-57	Verification Code (4)

DATA FORMAT

128 data cards (16 data words/card) with the following format:

COLS	INFORMATION FIELD
1-4	Four digit octal address of first output word on card
5-7	Three digit octal output word specified by address in column 1-4
8-52	Next fifteen output words, each word consists of three octal digits.

NOTES:

1. Positive or negative logic formats are accepted as noted in the fourth card.

2. Assigned by MOSTEK; may be left blank.

3. MOSTEK punched card coding format should be used. Punch "MOSTEK" starting in column one.

4. Punches as: (a) VERIFICATION HOLD - i.e. customer verification of the data as reproduced by MOSTEK is required prior to production of the ROM. To accomplish this MOSTEK supplies a copy of its Customer Verification Data Sheet (CVDS) to the customer.

   (b) VERIFICATION PROCESS - i.e. the customer will receive a CVDS but production will begin prior to receipt of customer verification; (c) VERIFICATION NOT NEEDED - i.e. the customer will not receive a CVDS and production will begin immediately.

HI-REL 16K ROM

MIL STD 105D

TABLE I — Sample size code letters

Lot or batch size	General inspection levels I	General inspection levels NORMAL LEVEL II	General inspection levels III
2 to 8	A	A	B
9 to 15	A	B	C
16 to 25	B	C	D
26 to 50	C	D	E
51 to 90	C	E	F
91 to 150	D	F	G
151 to 280	E	G	H
281 to 500	F	H	J
501 to 1200	G	J	K
1201 to 3200	H	K	L
3201 to 10000	J	L	M
10001 to 35000	K	M	N
35001 to 150000	L	N	P
150001 to 500000	M	P	Q
500001 and over	N	Q	R

TABLE II-A — Single sampling plans for normal inspection (Master table)

Acceptable Quality Levels (normal inspection). Each AQL column gives Ac (Acceptance number) and Re (Rejection number).

Code letter	Sample size	.010	.015	.025	.040	.065	0.10	0.15	0.25	0.40	0.65	1.0	1.5	2.5	4.0	6.5	10	15	25
A	2															0 1			1 2
B	3														0 1			1 2	2 3
C	5													0 1			1 2	2 3	3 4
D	8												0 1			1 2	2 3	3 4	5 6
E	13											0 1			1 2	2 3	3 4	5 6	7 8
F	20										0 1			1 2	2 3	3 4	5 6	7 8	10 11
G	32									0 1			1 2	2 3	3 4	5 6	7 8	10 11	14 15
H	50								0 1			1 2	2 3	3 4	5 6	7 8	10 11	14 15	21 22
J	80							0 1			1 2	2 3	3 4	5 6	7 8	10 11	14 15	21 22	
K	125						0 1			1 2	2 3	3 4	5 6	7 8	10 11	14 15	21 22		
L	200					0 1			1 2	2 3	3 4	5 6	7 8	10 11	14 15	21 22			
M	315				0 1			1 2	2 3	3 4	5 6	7 8	10 11	14 15	21 22				
N	500			0 1			1 2	2 3	3 4	5 6	7 8	10 11	14 15	21 22					
P	800		0 1			1 2	2 3	3 4	5 6	7 8	10 11	14 15	21 22						
Q	1250	0 1			1 2	2 3	3 4	5 6	7 8	10 11	14 15	21 22							
R	2000			1 2	2 3	3 4	5 6	7 8	10 11	14 15	21 22								

▼ = Use first sampling plan below arrow. If sample size equals, or exceeds, lot or batch size, do 100 percent inspection
▲ = Use first sampling plan above arrow.

Re = Rejection number.   Ac = Acceptance number.

TABLE C—1. LTPD sampling plans 1/2/

Minimum size of sample to be tested to assure, with a 90 percent confidence, that a lot having percent-defective equal to the specified LTPD will not be accepted (single sample).

Max. Percent Defective (LTPD) or λ	20	15	10	7	5	3	2	1.5	1	0.7	0.5	0.3
Acceptance Number (C) (r = c + 1)	Minimum Sample Sizes (For device-hours required for life test, multiply by 1000)											
0	11 (0.46)	15 (0.34)	22 (0.23)	32 (0.16)	45 (0.11)	76 (0.07)	116 (0.04)	153 (0.03)	231 (0.02)	328 (0.02)	461 (0.01)	767 (0.007)
1	18 (2.0)	25 (1.4)	38 (0.94)	55 (0.65)	77 (0.46)	129 (0.28)	195 (0.18)	258 (0.14)	390 (0.09)	555 (0.06)	778 (0.045)	1296 (0.027)
2	25 (3.4)	34 (2.24)	52 (1.6)	75 (1.1)	105 (0.78)	176 (0.47)	266 (0.31)	354 (0.23)	533 (0.15)	759 (0.11)	1065 (0.080)	1773 (0.045)
3	32 (4.4)	43 (3.2)	65 (2.1)	94 (1.5)	132 (1.0)	221 (0.62)	333 (0.41)	444 (0.31)	668 (0.20)	953 (0.14)	1337 (0.10)	2226 (0.062)
4	38 (5.3)	52 (3.9)	78 (2.6)	113 (1.8)	158 (1.3)	265 (0.75)	398 (0.50)	531 (0.37)	798 (0.25)	1140 (0.17)	1599 (0.12)	2663 (0.074)
5	45 (6.0)	60 (4.4)	91 (2.9)	131 (2.0)	184 (1.4)	308 (0.85)	462 (0.57)	617 (0.42)	927 (0.28)	1323 (0.20)	1855 (0.14)	3090 (0.085)
6	51 (6.6)	68 (4.9)	104 (3.2)	149 (2.2)	209 (1.6)	349 (0.94)	528 (0.62)	700 (0.47)	1054 (0.31)	1503 (0.22)	2107 (0.155)	3509 (0.093)
7	57 (7.2)	77 (5.3)	116 (3.5)	166 (2.4)	234 (1.7)	390 (1.0)	589 (0.67)	783 (0.51)	1178 (0.34)	1680 (0.24)	2355 (0.17)	3922 (0.101)
8	63 (7.7)	85 (5.6)	128 (3.7)	184 (2.6)	258 (1.8)	431 (1.1)	648 (0.72)	864 (0.54)	1300 (0.36)	1854 (0.25)	2599 (0.18)	4329 (0.108)
9	69 (8.1)	93 (6.0)	140 (3.9)	201 (2.7)	282 (1.9)	471 (1.2)	709 (0.77)	945 (0.58)	1421 (0.38)	2027 (0.27)	2842 (0.19)	4733 (0.114)
10	75 (8.4)	100 (6.3)	152 (4.1)	218 (2.9)	306 (2.0)	511 (1.2)	770 (0.80)	1025 (0.60)	1541 (0.40)	2199 (0.28)	3082 (0.20)	5133 (0.120)

1/ Sample sizes are based upon the Poisson exponential binomial limit.

2/ The minimum quality (approximate AQL) required to accept (on the average) 19 of 20 lots is shown in parenthesis for information only.

MIL—S—19500E

MEMORY DATA BOOK
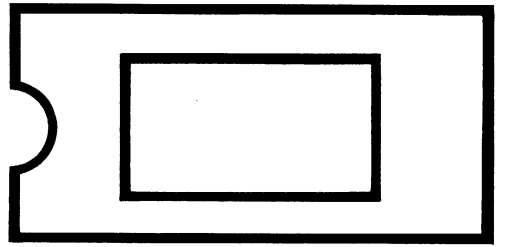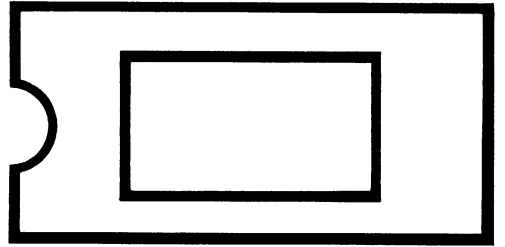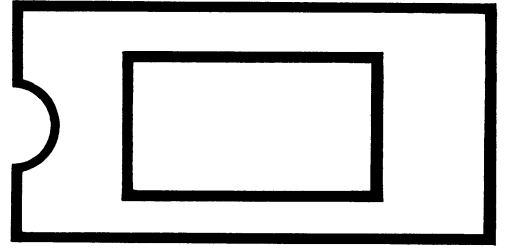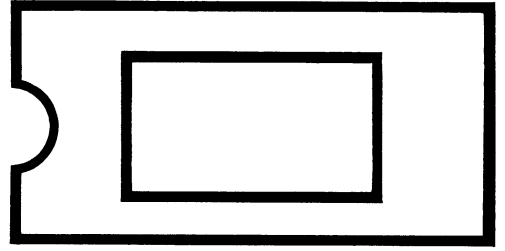
Dynamic Random Access Memory
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MEMORY DESIGNERS GUIDE

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DYNAMIC MOS RAMS
Technology
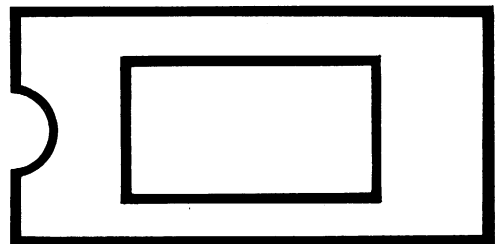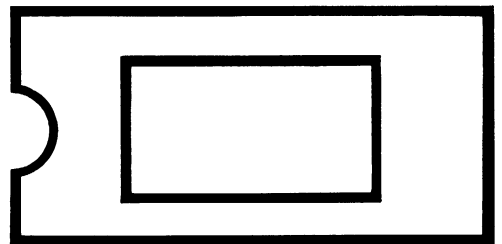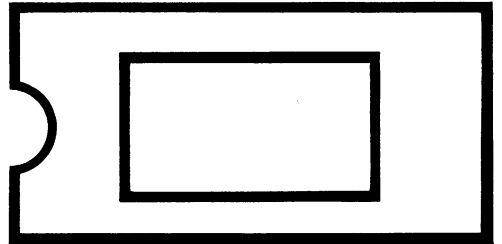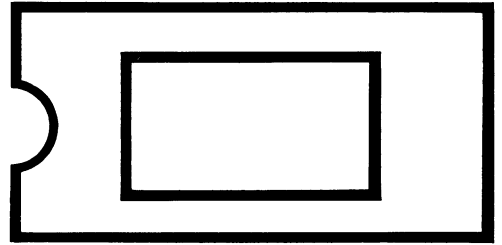
By DR. ROBERT PROEBSTING

ABSTRACT

This paper discusses the evolution of dynamic MOS RAMs. Included is a discussion of address multiplexing and timing considerations of multiplexed address MOS RAMs. Static and dynamic sense amplifiers are compared in terms of power consumption and layout problems and the benefits resulting from the use of dynamic sense amplifiers are discussed. Data sheet specifications of three presently available 16K dynamic MOS RAMs are presented.

INTRODUCTION

Semiconductor random access memories have been developed at a very rapid pace throughout this decade. RAMs with very impressive performance have been produced using bipolar technology, while RAMs with moderate performance but very low cost have been produced using MOS technology. This paper will discuss dynamic MOS random access memories which are rapidly replacing core memories in most memory applications. This recent dominance by dynamic MOS RAMs in the random access memory market comes about as a result of the cost, performance, and reliability associated with the integration of up to 16,384 bits of RAM on a single integrated circuit. This level of integration in turn is made possible by the use of dynamic circuit techniques, and more specifically by the use of dynamic data storage. These techniques have undergone very rapid development, causing the performance characteristics of available memory circuits to vary greatly from design to design as different techniques are incorporated. Dynamic and static sense amplifiers will be discussed, and the performance specifications of a commercially available 16K RAM using dynamic sense amplifiers will be compared to the specifications of two 16K RAMs using static sense amplifiers. The state-of-the-art in commercially available MOS memory is a 16K x 1 dynamic circuit with a chip access time of 150 nanoseconds, and a read-modify-write cycle time of 320 nanoseconds. Cost of dynamic MOS memory is rapidly decreasing and is now about 0.1 cent per bit at the chip level and about 0.15 cent per bit at the system level.

DEVELOPMENT OF DYNAMIC MEMORY

The first MOS RAMs used cross-coupled flip-flops as storage cells, each cell containing six or eight MOS transistors. The combination of a complex cell structure and a new technology gave rise to a high per-bit memory cost that found very few applications. But applications were expanded by major breakthroughs that significantly reduced the cost of MOS RAM. The first breakthrough was the development of the concept of dynamic memory storage — storing a digital "0" or "1" by a low or high voltage stored on a capacitor in a 3-transistor cell. However, this can cause a problem since the charge will eventually leak off any capacitor. If data is to be retained for longer than the self discharge time of a cell storage capacitor, typically two milliseconds, the data must be sensed before it is lost and then restored to its original voltage level. The operation of restoring the cell voltages to good levels is called a refresh operation. This simultaneously occurs in all cells of the externally addressed row of the memory matrix. To refresh the entire memory array, it is necessary to perform a refresh cycle to each of the 16 to 128 rows of the memory array at least once every two milliseconds.

The second major breakthrough in the development of MOS RAMs was the development of the single transistor cell. This cell is poorly named because it really consists of a single transistor plus a single capacitor, and the capacitor occupies the majority of the cell area. But this cell still occupied less than half the area of the earlier 3-transistor cell and permitted integration of 4096 bits per chip compared to only 1024 bits per chip using the earlier 3-transistor cell. The three year delay between the introduction of the 1-transistor cell was due to the difficulty in sensing the small signal from the 1-transistor cell. For the first time, there was no amplifier built into every cell, and signal levels out of the memory matrix became millivolts instead of volts. Sense amplifiers have been developed to sense the small signals from the 1-transistor cell and will be discussed later.

The 1-transistor cell permitted integration of 4K bits per chip. In addition, improvements in the inter-

nal peripheral or support circuits made this new generation of circuits much easier to use than were the earlier 1K circuits. The 1K circuits required multiple, critically-timed, high-capacitance, high-voltage clock signals. In the 4K chips, these were replaced by a single high-voltage, high-capacitance clock (22 pin version) or two TTL-level, low-capacitance clocks (16 pin version). The 1K chips required high voltages for address and data inputs, which were replaced by TTL-level inputs in the 4K chips. The high impedance output of the 1K chips, requiring an external sense amplifier, was replaced by a low impedance output capable of driving one or more TTL loads in the 4K circuits. The relatively slow P-channel technology used for the 1K chips was replaced by faster N-channel technology for the 4K chips. Integration of 4096 bits per chip reduced the per-bit chip cost, while the simplification of external support circuitry reduced other system costs. These savings made MOS memory cost competitive with magnetic core for the first time in most general applications. Integration of 16,384 bits per chip promises to reduce the per-bit cost even further. Although 16K chips require the same external support circuitry as that required by 4K chips, a given printed circuit board size, power supply, cooling system, set of address buffers, etc., supports four times as many bits when using 16K chips as when using 4K chips. Memory systems using 16K chips should become less expensive than those using 4K chips some time in the first half of 1978.

ADDRESS MULTIPLEXING

While use of the single transistor cell increased the bit density on a chip, it degraded the access time by about 25 percent. This is due to the delay through the sense amplifiers in detecting and amplifying the very small signals from the memory cells. This delay, however, made the multiplexing of addresses a very attractive means for reducing package pin count for increased memory density on a printed circuit board.

An MOS memory chip is physically arranged as a two dimentional array of cells. Certain address inputs are used for row selection and the remaining address inputs are used for column selection. Row selection is required before the sense amplifiers can begin their slow detection process. Column selection is not required until the outputs of the sense amplifiers are valid, since its function is to gate data from the selected sense amplifier to the data output circuitry. Since the column selection information is not used internally until well after the row selection information is required, only the row addresses need to be available to the chip at the start of a cycle. The column address can come later with no penalty of access time. The multiplexed address memory takes advantage of this delayed need for column address. Instead of using 12 address pins to select one of 4096 memory cells, six address pins are used to first select one of 64 rows, and subsequently the same pins are used to select one of 64 columns. The result is a 4096 bit RAM in a 16 pin package, rather than in the more straightforward 22 pin package.

When compared to the 22 pin 4K RAM, the 16 pin 4K RAM has both advantages and disadvantages. The primary advantage of the 16 pin approach is the substantial increase in board density that it allows. A second advantage is the reduction in the required number of address buffers from 12 to 6. A third advantage is that multiplexing permits a faster mode of operation, called page mode, which shall be discussed later. Finally, two more specific advantages were available to users of the 16 pin design. These were the use of TTL-level timing signals rather than a high voltage clock, and the use of dynamic sense amplifiers rather than static sense amplifiers to reduce power comsumption. These last two differences were not a result of the multiplexing but were nevertheless, advantageous for users of the 16 pin design.

The 16 pin implementation also had disadvantages. The multiplexed part required two timing signals and hence more complex timing. The first signal, $\overline{RAS}$, initiates a cycle and strobes in the row address, and the second signal, $\overline{CAS}$, strobes in the column address. Any skew in the timing of the second signal with respect to the first added directly to access time. Systems using the 22 pin design, which required only a single clock, had less complex timing and suffered no such degradation of access time. Finally, the 22 pin design, not having the TTL to MOS level clock driver on the chip, dissipated less than 1 mW in the standby mode compared to about 10 mW per chip for the 16 pin part.

In the first year after various designs were introduced, the 22 pin approach gained greater acceptance than the 16 pin approach, not because of the technical advantages or disadvantages of the two approaches, but because there were two major MOS memory suppliers manufacturing the 22 pin part and only one manufacturing the 16 pin part. Many users would not choose a single-sourced product. Other users had a strong enough preference for the multiplexed concept to commit to that design, correctly assuming that the market they created for the 16 pin design would cause additional manufacturers to offer their own 16 pin designs. Meanwhile, the 16 pin design was improved to eliminate the access time penalty due to multiplexing. This was accomplished by performing the critical timing of the second clock with circuitry on the chip rather than with external circuitry—a feature referred to as "gated $\overline{CAS}$." With many users committed to a multiplexed design, other manufacturers began supplying this part. And with multiple sourcing available, more and more users designed systems using the 16 pin part. This trend has escalated to the point where virtually all new memory system designs now incorporate the 16 pin device.

The acceptance of address multiplexing generated by 4K RAMs virtually assured its use in the next generation of dynamic MOS RAMs. And indeed all 16K RAMs on the market today use address multiplexing and are pin compatible with each other. Many new memory system designs take advantage of the pinout similarity between the 4K and 16K parts. Printed circuit boards are designed to accommodate either part, with only a single jumper wire required to switch from 4K to 16K chips, caused by the need for a seventh address pin on the 16K part, which replaces the chip select pin of the 4K part. Chip selection is accomplished on the 16K part by decoding $\overline{RAS}$ or $\overline{CAS}$ or both.

MULTIPLEX TIMING CONSIDERATIONS

Although address multiplexing provides some very substantial system benefits, it complicated system timing. It requires that both row and column addresses get into the chip in a short time using the same address pins. This establishes a rather tight timing window during which the individual events must occur. The sequence of events required to address the chip is as follows: (1) establish row addresses, (2) bring $\overline{RAS}$ low, (3) maintain row addresses valid for some minimum hold time, (4) establish column addresses, (5) bring $\overline{CAS}$ low, and (6) hold column addresses valid for some minimum time. To achieve specified access time from $\overline{RAS}$, it is necessary to bring $\overline{CAS}$ low within some specified maximum delay after $\overline{RAS}$.

Every attempt is made during the design of multiplexed chips to simplify the system timing problem. This is done by first reducing the row address hold time to an absolute minimum, since the system must not begin to establish column addresses until the minimum row address hold time is met. Then, if possible, the design is made to tolerate a negative set-up time for the column addresses, which means that column addresses need not be valid until some time after $\overline{CAS}$ starts low. This also increases the time available for multiplexing. Finally, the critical $\overline{RAS}$ to $\overline{CAS}$ timing is done on the chip, which means that if $\overline{CAS}$ occurs earlier than needed by the chip, it is internally delayed until it is needed ("gated $\overline{CAS}$"). For high performance memory systems, the use of a delay line to minimize timing skews is essential. With a delay line, the timing sequence can be net such that $\overline{CAS}$ occurs early enough after $\overline{RAS}$ to guarantee the specified access time from $\overline{RAS}$.

OPERATION OF MULTIPLEXED DYNAMIC RAMS

In a multiplexed design, the 12 addresses of a 4K memory or the 14 addresses of a 16K memory are strobed into the memory chip in two groups of 6 or 7 respectively. When an address becomes available for a memory operation, the row address must first be presented to the chip address pins. As soon as the row address inputs are valid, the first of two timing signals to the chip initiates a cycle. This signal strobes or latches the row address into the chip and is appropriately called Row Address Strobe or $\overline{RAS}$. With no further commands to the chip, the latched addresses are converted to MOS voltage levels, decoded, and the selected row is enabled. Data is thereby destructively read from each cell in the selected row by dumping its charge onto its respective column sense line. A sense amplifier for each column detects the change in voltage level on the column line resulting from this deposited charge, and amplifies this signal. The amplified signals from the sense amplifiers are then impressed back onto the column sense lines, returning the cells to their original voltages. A cell whose voltage had decayed is restored to its original voltage in the process. At this time the sense amplifiers contain the same data or information contained in the selected row, and the destructively-read cells in the row are restored (refreshed) to their proper voltage.

When an active cycle is initiated by $\overline{RAS}$ going low, it must not be aborted. It is necessary to keep $\overline{RAS}$ low for some minimum length of time to allow the sense amplifiers time to restore data back into the destructively-read cells. To summarize, the function of the Row Address Strobe is to initiate a cycle, strobe or latch the row address, enable the selected row of memory cells, sense and restore the data in that row of memory cells, and maintain the sensed data from the entire row of addressed memory cells in their respective sense amplifiers. The sense amplifiers maintain this data as long as $\overline{RAS}$ remains active. At the end of a cycle, when $\overline{RAS}$ is taken high, the selected row is immediately turned off, isolating the correct data in the cells. After the row is off, the half-digit lines are prepared for a new cycle.

The Column Address Strobe ($\overline{CAS}$), on the other hand, controls column selection circuitry and the transfer of data from the selected sense amplifier to the output circuitry. After $\overline{RAS}$ strobes the row address information from the multiplexed address input pins, $\overline{CAS}$ strobes the column address from the same pins. When $\overline{CAS}$ goes active (low), the column address is strobed or latched into the circuit. This address is then decoded to select the proper column. Data from the selected sense amplifier is then transferred to the output buffer, completing read access.

During a write operation, the same sequence of events occurs as in a read cycle, with identically the same timing as in a read cycle except that the write enable signal, $\overline{WRITE}$, is brought active (low). This causes the data at the data input to be strobed into the chip, buffered, and written into the selected sense amplifier and, thereby, into the selected cell. A -read-modify-write cycle starts out as a read cycle until read access

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time. Then when input data becomes available to the memory, $\overline{\text{WRITE}}$ must be activated. As in a write-only cycle, this causes the data to be written into both the selected sense amplifier and into the selected cell. The active cycle must not be terminated until the internal write circuitry has had sufficient time to complete the write operation.

PAGE MODE OPERATION

The Row Address Strobe transfers the data from an entire row of memory cells into their respective sense amplifiers. The Column Address Strobe transfers the single bit of data from the selected sense amplifier into the output buffer. This organization permits data to be transferred into or out of multiple column locations of the same row by having multiple column cycles during a single active row cycle. This mode of operation is called page mode. A page of memory is defined as those memory locations sharing a common row address, but not necessarily confined to a single chip.

After a row has been selected by the Row Address Strobe, the contents of all cells in that row are available in their respective sense amplifiers. Repetitive column address cycles, while maintaining a single active row cycle, permit faster operation than is possible in the normal operating mode. This is because the delay through the sense amplifier only adds to the access time of the first column in the page. Data to be accessed from each subsequent column is already available in its respective sense amplifier. Therefore, page mode access is the access time from $\overline{\text{CAS}}$, which is typically two-thirds the access time from $\overline{\text{RAS}}$. Page mode reduces power consumption while typically doubling maximum operating frequency. Read, write, and read-modify-write cycles can be performed in either normal cycles or in page cycles. Page mode operation has a number of applications, with high-speed block transfer of data being the most important.

SENSE AMPLIFIER CONSIDERATIONS

The one-transistor memory cell has been simplified to a rather minimal structure: a capacitor stores digital data as a high or low voltage, and a transistor selectively connects the capacitor to a digit/sense line. (See Fig. 1.) Conduction through the transistor is controlled by its gate which is electrically connected to the other gates in a row. When a row is enabled by the row decoder, all transistors in that row become conductive, transferring charge from their respective capacitors to their respective digit/sense lines, destructively reading data. Each column has its own sense amplifier, whose function is to detect this charge and to amplify the signal caused

by this charge. The amplified signal is a full logic level, either at ground or close to V_{DD}.

The cell transistors remain conductive throughout this period so that the amplified signals from the sense amplifiers feed back into their respective cells, refreshing the voltage levels in the cells.

To maximize the signal into the sense amplifier, a large cell capacitance and a small digit/sense line capacitance are desired. This is because the cell and its digit line form a capacitive divider that attenuates the signal from the cell. But integration of large numbers of bits on one circuit requires a physically small cell size which implies an electrically small cell capacitance. Integration of large numbers of bits also requires that many cells share a common digit/sense line, causing this line to be physically long and to therefore have high stray capacitance. To keep the signal attenuation to an acceptable level, steps are taken to both maximize cell capacitance and to minimize digit line capacitance. Cell capacitance can be increased by using a double layer polysilicon fabrication process, which increases the percentage of cell area used for the capacitor. Digit line capacitance can be reduced by simply cutting the line in half. The sense amplifier is then placed in the center of a digit line, and senses a differential voltage between the two halves of the line. In 16K designs, the cell capacitance is typically 0.04 picofarad and the stray capacitance of one half-digit is typically 1 picofarad. Thus the signal from the memory cell is attenuated by a factor of 25 before being sensed by the sense amplifier.

Between cycles, the two halves of each digit line are equilibrated to precisely the same voltage. When an active cycle is initiated by $\overline{\text{RAS}}$ going low, these lines are momentarily allowed to float. Then a row is enabled, transferring charge from the enabled cell in each column to its half of its digit line. On each digit line, only a single memory cell is selected. This cell may be located on either the top or bottom half of the digit line. If the cell was originally at a high voltage, it causes its half-digit line voltage to be at some "high" value. If the cell was originally at a low voltage, its resulting half-digit line voltage is some "low" value. It should be noted that the attenuation of the digit line causes the "high" and "low" voltages to differ by less than one-half volt. The half-digit line not containing the addressed cell is simultaneously adjusted to a voltage somewhere between the "high" and "low" voltages of the addressed half by a special cell called a "dummy cell." Thus if a cell originally contained a high voltage, the voltage of its half-digit line will be approximately one-quarter volt above the adjusted intermediate voltage of the other half-digit line. If the cell originally contained a low voltage, the voltage of its half-digit line will be approximately one-quarter volt below the intermediate

voltage of the other half-digit line. It is now up to the sense amplifier to detect this differential signal of one-quarter volt or less.

A detailed analysis of the sense amplifier will not be attempted. It will simply be noted that the sense amplifier consists of a balanced flip-flop. Since the addressed cell, in conjunction with the dummy cell, guarantees an initial voltage imbalance to this flip-flop, the positive feedback of the flip-flop causes it to latch up. The half-digit line having the lower initial voltage goes to ground while the other half-digit line goes to or in the case of a dynamic sense amplifier, remains near V_{DD}.

Two types of sense amplifiers have been used in commercially available products. These are variations of the static amplifier in Fig. 1, and of the dynamic amplifier in Fig. 2. Both are about equal in their ability to detect and amplify small signals. The load resistors, R1 and R2, in the static amplifiers consume a substantial amount of power, typically half or more of the total chip power. Since these resistors are not present in dynamic amplifiers, the total power consumption of memory chips employing dynamic sense amplifiers is much less than that of circuits employing static sense amplifiers. There are, however, formidable design or layout problems associated with the use of dynamic sense amplifiers which will be discussed presently. These problems are severe enough that many chip designers chose to incorporate power-consuming static sense amplifiers into their designs.

To understand the differing circuit requirements for static and dynamic sense amplifiers, one must look at a write cycle or more accurately, a read-modify-write cycle. Suppose, in Fig. 1, cell 64 had originally stored a low voltage and was read. The sense amplifier, detecting a lower voltage on node B than on node A, will drive node B to ground and node A near V_{DD}. Transistor T3 then turns on, and the data from the cell becomes available to the output buffer at one end of the data bus. Now, assume that it is desired to write opposite data back into the cell. This requires forcing a high voltage onto node B and onto the storage capacitor, C64. To do this, the data input buffer will drive the input/output data bus to ground. Transistor T3 then forces node A to ground, over-powering R1. When node A goes to ground, transistor T2 turns off. This allows R2 to pull node B to V_{DD} as required to write the high level into the storage cell. Without R2, node B would simply remain at ground, and a high voltage could not have been written into the cell. With these resistors, data can be written into a cell in either half of the matrix with a single input/output data bus. A trade-off exists in the resistance value chosen for R1 and R2. Since either R1 or R2 will dissipate power in all of the sense amplifiers, a low value resistor results in a very high

power consumption. But the digit line capacitance of node B is quite large, and a high value resistor means an excessively long write time. There is no good compromise, and circuits using static sense amplifiers consume high power and have long write times.
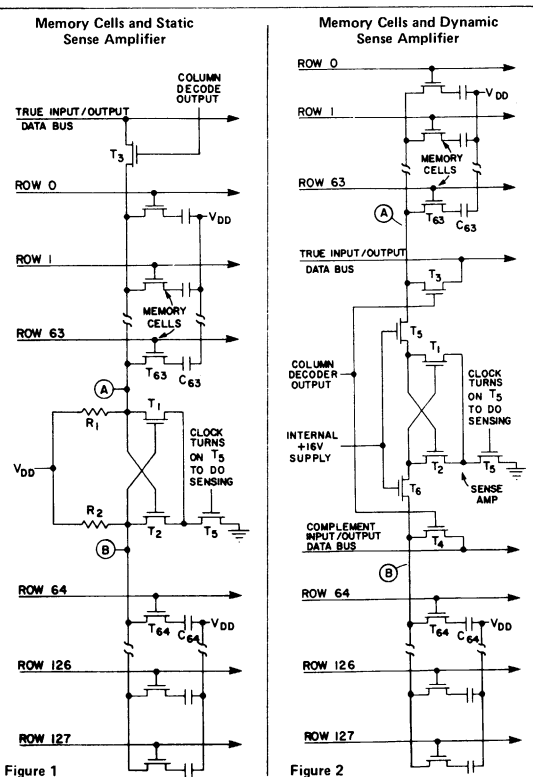
Figure 1 Memory Cells and Static Sense Amplifier. Memory chips using static sense amplifiers consume twice the power of chips using dynamic sense amplifiers, due to the conduction through either R1 or R2.

Figure 2 Memory Cells and Dynamic Sense Amplifier. The use of dynamic sense amplifiers requires both true and complement input/output data busses. This, in turn, requires either two full column decoders or placement of a single column decoder with the sense amplifiers in the center of the memory.

On paper, the dynamic sense amplifier solves the problem very well. Referring now to Fig. 2 and having again read a low voltage from cell 64, assume it is again desired to write a high voltage back into the cell. Now, as before, the input buffer drives the true data bus to ground, with transistor T3 causing node A to follow. But, in addition the input buffer also forces the complement data bus to V_{DD}, with transistor T4 causing node B to follow. In forcing node B to V_{DD}, the complement data bus performed the job previously done by the resistor. With row 64 still selected, the high voltage on node B is transferred into the cell, and the write operation is complete. It should be noted that transistors T3 and T4 function only as switches and can have very low resistances to

speed-up write time. No speed—power trade-off is involved. Therefore, memory designs using dynamic sense amplifiers consume far less power and write much faster than do designs using static sense amplifiers.

The layout problem associated with the dynamic sense amplifier is that it requires both a true and a complement data bus. These, in turn, require that the column decode outputs be available in both the top and bottom halves of the memory array. Placing single column decoder above (or below) the memory array is ruled out since it is not practical to run its outputs through the memory array to the other side. One solution to the layout problem is to use two entire column decoders, one above the top half of the array to service the true data bus, and the other below the bottom half of the array to service the complement data bus. This gains all the advantages of using dynamic sense amplifiers, but the duplication of the column decoder consumes a substantial amount of silicon area, thereby raising the cost of the chip.

A second solution is to use a single column decoder located in the center of the memory array along with the sense amplifiers. This approach requires great care in design. If the column decoder is located in the center of the chip, it is topologically necessary for the digit lines to cross the buffered column address signals. Just one address signal, moving from ground to V_{DD}, capacitively couples more signal onto a digit line than that provided by the memory cell. At first thought, this is frightening indeed. But on second thought, there are 127 unselected row lines that cross the digit lines and they do not cause a problem. They are quiet. Indeed if all lines crossing the digit line are kept quiet until the sense amplifier detects and amplifies its signal, there is no problem. With a multiplexed design, it is particularly easy to insure that the buffered column address lines remain quiet during this time, since multiplexing automatically causes the column address to be processed after the row addresses have been processed.

The advantages of dynamic sense amplifiers over static sense amplifiers are rather dramatically illustrated in Table 1. The power differences between the MK4116 and the other parts is due almost entirely to the choice of sense amplifiers. So is the write time. Other performance differences between the various designs are due to alternate circuit techniques used throughout the designs, not necessarily related to the choice of sense amplifier.

OTHER MOS RAMS

The very small area occupied by a single-transistor cell makes dynamic MOS RAM substantially less

Table 1

PART NUMBER	MK4116-2 MOSTEK	2116-2 (INTEL)	TMS 4070-2 (TI)
SENSE AMP	DYNAMIC	STATIC	STATIC
MAX I_{DD}(MA)	35	69	76
V_{DD} TOLERANCE	±10%	±10%	±5%
ACCESS TIME (FROM $\overline{RAS}$) (ns)	150	200	250
ACCESS TIME (FROM $\overline{CAS}$) (ns)	100	125	165
MAX $\overline{RAS}$ to $\overline{CAS}$ delay for specified $\overline{RAS}$ access (ns)	50	75	80
Row Address Hold Time (ns)	20	45	50
Col Address Setup Time (ns)	−10	−10	0
WRITE TIME After READ	60	125	165
MIN READ or WRITE CYCLE (ns)	375	350	400
MIN READ-MODIFY-WRITE CYCLE	375	400	590
REFRESH Cycles REFRESH Interval	128 2ms	64 2ms	128 2ms
PAGE MODE	Yes	Yes	Yes
Package Pins	16	16	16

DATA SHEET SPECIFICATIONS FOR COMMERCIALLY AVAILABLE 16K MOS RAMs. All numbers pertain to fastest speed selection.

expensive than other forms of MOS RAM. For many applications, however, other forms of MOS RAM deserve consideration. All of the RAMs described below operate from a single +5 volt supply, compared to the +12, +5, and −5 volt supplies required by dynamic RAMs. All use static cells, eliminating the refresh cycles required by dynamic RAMs. These circuits are not multiplexed, simplifying system timing. These considerations make this group particularly attractive in small memory systems.

By using dynamic circuit techniques with a static (flip-flop) cell, low active power and even lower standby power can be achieved. Such 4K RAMs are now available with under 100 mW active power and under 10 mW standby power. Access times are similar to those of dynamic RAMs.

When access time is of paramount importance, static cells are used with static peripheral circuits. This permits access times of 50 nanoseconds or below at

active power levels of about 500 mW, and standby power of about 35 mW. Lower power versions are also available with longer access times.

For applications requiring extremely low power dissipation, complementary MOS RAMs are very attractive. These circuits are the most expensive of the group, but consume nanowatts to microwatts during standby and microwatts to milliwatts when active. They also tolerate extremely wide variations in power supply voltage, often from 3 to 15 volts.

CONCLUSION

Some of the dynamic MOS RAMs on the market today consume considerably less power than others. Some are considerably faster than others. But compared to other technologies, all of these parts represent very attractive building blocks for random access memory systems. The highest power 16K circuits only consume about 35 watts in a 256K work

x 32 bit per word system. The slowest circuits permit system access times faster than 500 nanoseconds.

The high storage density resulting from the use of small 16 pin packages, each containing 16K bits, is very important in the design of large memory systems. The combination of TTL compatibility of all inputs and outputs, and relatively straightforward timing requirements make these circuits equally attractive for small memory systems.

In systems requiring extremely fast access times, bipolar technology provides the best answer. In systems tolerant of relatively slow serial access rather than requiring fast random access, other technologies, including disc, CCD, or bubble memories are potentially less expensive than dynamic MOS. But for those applications requiring random access memory of low to moderate performance, the combination speed, power, density, reliability and cost of dynamic MOS memory just can't be matched by any other technology today.

CHIP PHOTOGRAPH OF MK4116
Figure 3
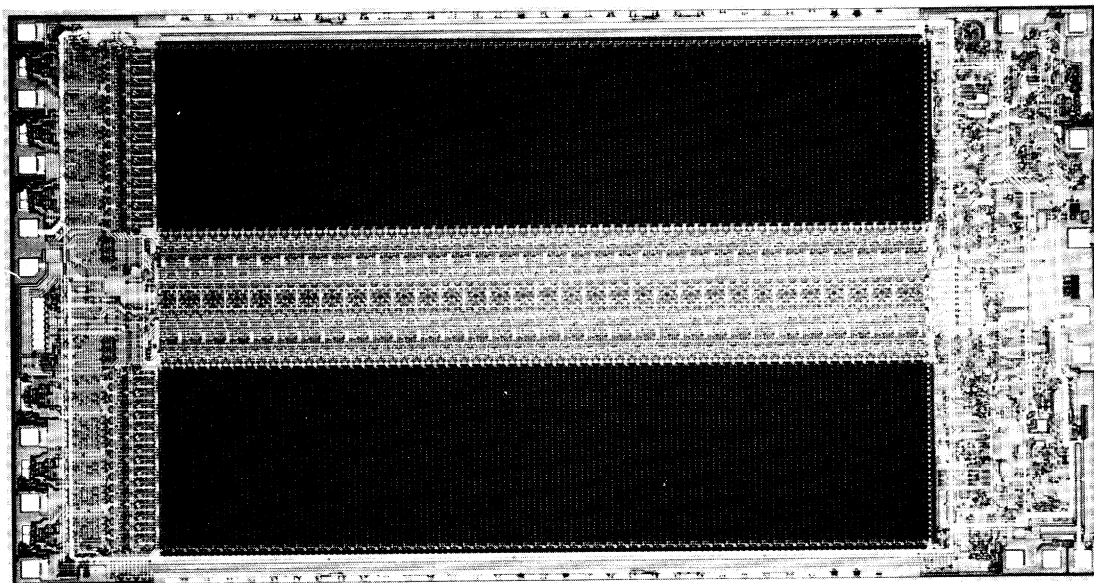
The column decoders are located with the sense amplifiers between the top and bottom halves of the memory array. The chip size of this 16K RAM is 122 mils x 227 mils.

MOSTEK®

AN IN-DEPTH LOOK AT MOSTEK'S HIGH PERFORMANCE MK4027

By DERRELL COKER

Application Note

The MK 4027, like its predecessor the MK 4096, is a 4096 word by 1 bit N-Channel MOS Random Access Memory circuit that is packaged in a standard 16-pin DIP. This small package size is the result of a unique multiplexing and latching technique for the address inputs which MOSTEK pioneered for its 4K RAM family. This innovative approach to dynamic RAM design has proven to be one of the most important semiconductor memory milestones in the past few years. With more than a dozen manufacturers having announced their intentions to produce equivalent circuits with identical pin configurations, the MOSTEK 16-pin 4K RAM family has become an industry standard.

The purpose of this application note is to acquaint the user with the MK 4027, and to provide a more complete and in-depth understanding of the circuit (and its use) than can be obtained from the data sheet alone. MOSTEK realizes that most experienced memory system designers go through a process of evaluating many potential memory devices and making a judgement as to which device is best for a particular application. MOSTEK also realizes that this evaluation process can be a very tedious and time consuming endeavor, especially if several potential candidates are to be evaluated. Therefore, the information presented in this application note is divided into major sections and presented in the order that MOSTEK has found to be most desirable in the typical evaluation process used by most designers.

Figure 1
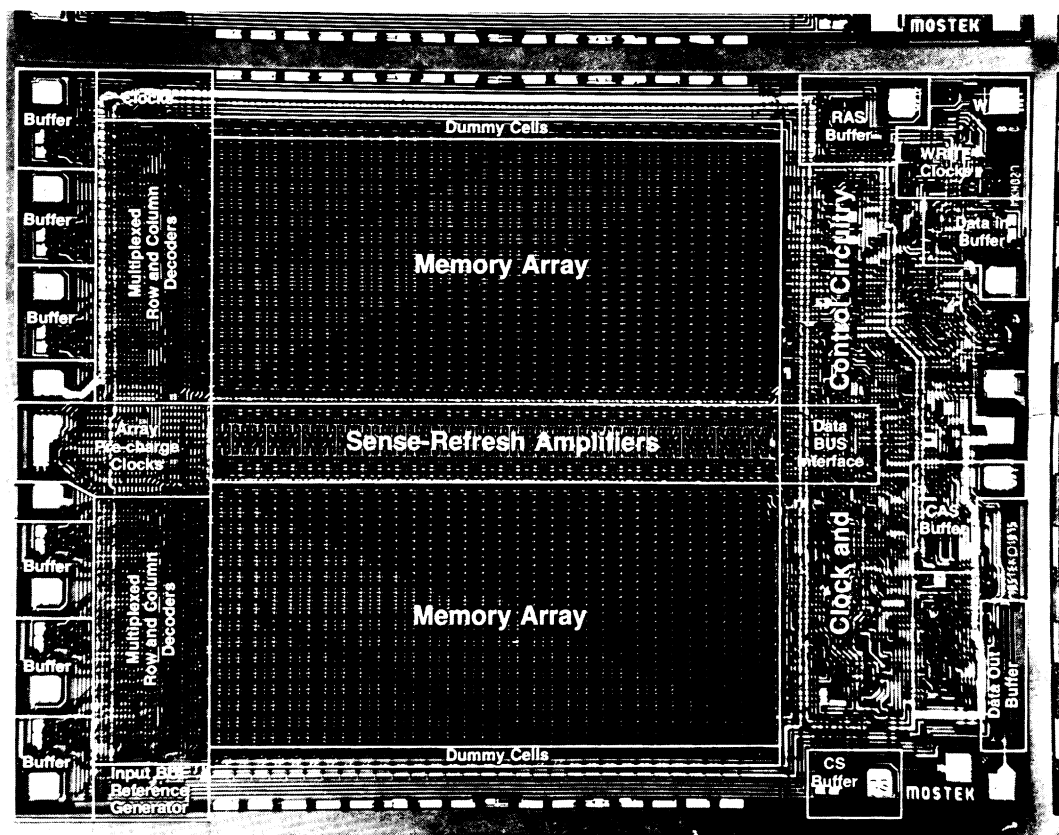
BACKGROUND

The pin configuration for the 16-pin 4K RAM was originated by MOSTEK Corporation when the MK 4096 was announced in 1973. Basically, the 16 pin device is made possible by eliminating six of the twelve address inputs required to select one out of 4096 bit locations in the RAM. Addressing is accomplished by the external generation of negative going Row and Column Address Strobe signals ($\overline{RAS}$ and $\overline{CAS}$) which latch incoming multiplexed addresses into the chip. This same addressing technique is carried over from the MK 4096 to the higher performance MK 4027.

PIN CONNECTIONS
Figure 2

(-5 V POWER SUPPLY)	V_{BB}	1	16 V_{SS}	(GROUND REF, 0 VOLTS)
(DATA INPUT)	D_{IN}	2	15 $\overline{CAS}$	(COLUMN ADDRESS STROBE)
(WRITE ENABLE STROBE)	$\overline{WRITE}$	3	14 D_{OUT}	(DATA OUTPUT)
(ROW ADDRESS STROBE)	$\overline{RAS}$	4	13 $\overline{CS}$	(CHIP SELECT)
(ADDRESS INPUT)	A_0	5	12 A_3	(ADDRESS INPUT)
(ADDRESS INPUT)	A_2	6	11 A_4	(ADDRESS INPUT)
(ADDRESS INPUT)	A_1	7	10 A_5	(ADDRESS INPUT)
(+12 V POWER SUPPLY)	V_{DD}	8	9 V_{CC}	(+5 V POWER SUPPLY)
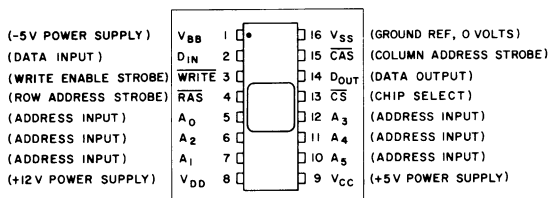
In addition to improved performance characteristics, the MK 4027 also incorporates several different and flexible operating modes and system-oriented features. These features include direct interfacing capability with TTL, low capacitance inputs and output, on-chip address and data registers, two methods of chip selection, simplified ($\overline{RAS}$-only) refresh operation, and flexible column address timing to compensate for system timing skews. Also, the MK4027 offers a unique cycling operation called page-mode. Page-mode timing is very useful in systems requiring Direct Memory Access (DMA) operation.

Before delving into the more detailed aspects of the MK 4027, it is helpful to obtain a basic understanding of the internal circuit operation. Once a designer understands the fundamental operation of the MK 4027, it is much easier to see how and why the device operates with such improved performance over existing 4K dynamic RAM designs.

Much of the internal structure of the MK 4027 is made possible by state-of-the-art processing. The MK 4027 is fabricated with MOSTEK's ion-implanted N-Channel silicon gate (Poly I) process, whose basic steps are illustrated in figure 3. This process allows independent adjustment of gate and field oxide thresholds by ion-implantation (a technique introduced by MOSTEK in 1971), which maximizes performance, density, and reliability.

INTERNAL CIRCUIT OPERATION

The internal circuit operation of the MK 4027 is unlike any other 4K RAM in the industry. The MK 4027 utilizes a revolutionary new architecture for semiconductor memories. The circuit layout and design techniques incorporated within the MK 4027 are the main reasons for the increased performance capabilities and the additional system-oriented features. As an aid in understanding the operation of the MK 4027 refer to the block diagram in figure 4.

A major difference between the MK 4027 and most conventional RAMs is that the MK 4027 has

4027 PROCESS STEPS
Figure 3

DEPOSIT SILICON NITRIDE ($Si_3 N_4$) ON WAFER AND COAT WITH PHOTORESIST.

DEFINE ACTIVE AREA WITH MASK 1 AND IMPLANT FIELDS USING PHOTORESIST AND NITRIDE AS MASK.

REMOVE PHOTORESIST AND GROW FIELD OXIDE USING NITRIDE AS MASK.

REMOVE NITRIDE, GROW THIN GATE OXIDE, IMPLANT GATE REGION FOR THRESHOLD CONTROL AND DEPOSIT POLY-SILICON.

DEFINE POLY TRANSISTOR GATES AND INTERCONNECT USING MASK 2.

DIFFUSE PHOSPHORUS N+ DOPANT FOR SOURCE, DRAIN AND INTERCONNECT DIFFUSIONS.

DEPOSIT OXIDE TO INSULATE POLY FROM ALUMINUM AND DEFINE ALUMINUM CONTACTS WITH MASKS 3 & 4.

DEPOSIT ALUMINUM AND DEFINE BONDING PADS AND METAL INTERCONNECT WITH MASK 5.

DEPOSIT PASSIVATION OXIDE AND DEFINE BONDING PAD OPENINGS WITH NON-CRITICAL MASK 6.

only one internal decoder and only one set of input buffers for both the Row and Column addresses. This feature greatly reduces the active silicon area and input capacitance. Note also that the internal single transistor storage cell matrix is divided into two sections with the sense amplifiers and input/output circuitry located between the two. This type of sense amp configuration causes data stored in half of the memory to be inverted from the data stored in the opposite half. However, this inversion is completely invisible at the device terminals. The sense amplifiers incorporated within the MK 4027 are dynamic, balanced, differential sense amps which dissipate no D C or steady-state power. Furthermore, virtually all of the circuitry used in the MK 4027 is dynamic and consequently, most of the power dissipated by the MK 4027 is a function of operating frequency rather than active duty cycle.

MEMORY CYCLES

The MK 4027 will begin a memory cycle as soon as the Row Address Strobe ($\overline{RAS}$) input is activated. This is done by changing the voltage potential at the $\overline{RAS}$ input from a high level to a low level. The first internal action that takes place is the conversion of the TTL-compatible $\overline{RAS}$ signal to the MOS (12 volt) level that is required within the chip. The internal amplifier that performs this conversion is, of necessity, powered up at all times. Therefore, the $\overline{RAS}$ input buffer always dissipates some D C power. The steady-state power dissipated by the $\overline{RAS}$ input buffer is the main component of the overall standby power.

After the Row strobe reaches the proper level internally, a series of internal clock edges are generated to perform special control functions. The first of these clocks serves as a signal to "trap" the first set of six addresses into the address input buffers. These input buffers then generate the address into both true and complement form in high level, as required by the decoder. The addresses are then decoded for selection of the proper row in the memory cell matrix. Also, as the selected row is enabled, a set of dummy cells are enabled on the opposite side of the sense amplifier from the selected Row. These dummy cells serve to establish the proper trip point or reference voltage as required by the sense amps to differentiate between a one level and a zero level when the selected cell is read. As the selected Row and dummy cells are enabled, the address input buffers are already being reset and precharged so that the column addresses can be multiplexed into the chip.

The last action initiated by the row clocks causes the data in all 64 cell locations in the selected Row to be latched into the sense amplifiers which, in turn, restore proper data back into the cells. (This action is known as refreshing.) The selected Row output from the decoder remains enabled as long as the Row Address Strobe ($\overline{RAS}$) is at a logic 0 level.

The second chain of events within the MK 4027 memory cycle, assuming that $\overline{RAS}$ is active, occurs when the Column Address Strobe ($\overline{CAS}$) is activated. As soon as the $\overline{CAS}$ is brought to logic 0 level, the output buffer is turned off and the output assumes the high impedance (open-circuit) state. If, at this time, the input circuitry is ready to process the column data, the low level $\overline{CAS}$ signal is converted to

MK 4027 FUNCTIONAL BLOCK DIAGRAM
Figure 4
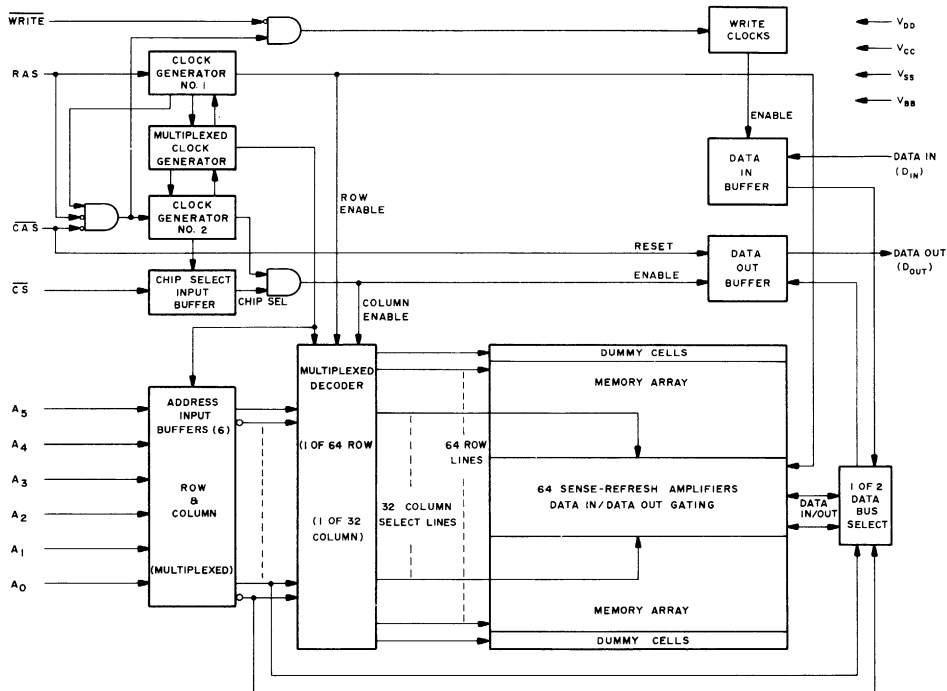
high level (12V) CAS. However, if the circuit is not yet ready to process column data, generation of the high level CAS signal is delayed. The internal mechanism for determining whether the MK 4027 is ready to process the column information is controlled by a signal from the row clock generator. This signal inhibits all column clocks until the sequence of row clocks has progressed to the appropriate time in the memory cycle. The internal "gating" of the RAS and CAS clocks has a very significant impact on external operation of the part. This is discussed in detail in a later section of this application note.

After CAS reaches the proper internal level, a series of clock edges are generated which operate in a similiar manner to the RAS clocks. In the case of CAS, however, the second rather than the first clock serves to "trap" the second set of six addresses into the address input buffers. These buffers again generate true and complement high level addresses as required by the decoder. Also, at this time the WRITE circuitry is enabled and the input/output data buses, which are routed through the center of the cell matrix, and the output buffer are all precharged to proper levels.

If the WRITE input is activated, a parallel series of clocks are enabled in addition to those enabled by the CAS circuitry alone. While the column addresses are trapped into the address input buffers and converted into true and complement high-level addresses, the WRITE input is converted to a high-level clock and data is latched into the data input buffer where it is also converted to true and complement, high-level information. It should be pointed out that the CAS circuitry also enables the Chip Select (CS) input. The Chip Select input buffer is essentially the same type of circuit as an address input buffer, but, if the Chip Select input is not activated, the remaining series of CAS clocks are inhibited.

If, at this point in time, the chip has received a Row Address Strobe and a Column Address Strobe (with the Chip Select active), the chip will initiate either the Read or Write operation as indicated by the state of the WRITE input. The decoder selects the proper column by enabling the coupling transistors which connect the selected columns to the data input/data output differential bus pairs. During a read cycle, data is transferred from the selected sense lines to the I/O bus pairs. A write cycle will cause data to be transferred from the selected data I/O bus to the sense lines so that proper data is forced into the selected storage cell. After the correct data is present on the I/O bus, the data output buffer is latched and the correct information is presented at the output of the chip. Once the output buffer is latched, the output is decoupled from the internal I/O bus.

FUNCTIONAL FLOW CHART
Figure 5

178
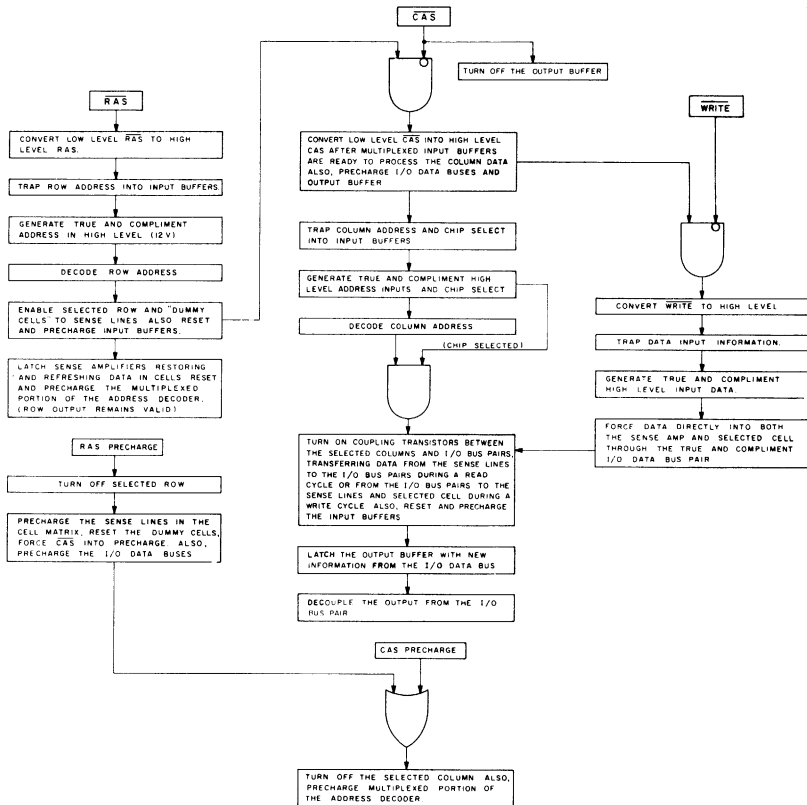
After the chip has performed all the functions required for a read, write or refresh operation, it remains in a quiescent state until the input control clocks ($\overline{RAS}$ and $\overline{CAS}$) are taken to the inactive (high) state. If $\overline{RAS}$ remains active and $\overline{CAS}$ is taken to the precharge (high) condition, the previously selected column will be turned off and the multiplexed portion of the address decoder will be reset and precharged, ready for a new $\overline{CAS}$ cycle. However, the previously selected row will remain enabled and the sense amps will retain the information read from that row. (This feature of the MK 4027 makes possible "page-mode" operation.) When $\overline{RAS}$ is terminated, the selected Row is turned off, the sense lines and the data I/0 buses are precharged and the dummy cells are reset. Also, the input buffers and decoders are reset and precharged, ready for a new $\overline{RAS}$ cycle. Deactivating $\overline{RAS}$ also forces $\overline{CAS}$ into the precharge condition internally, even though $\overline{CAS}$ may remain active at the input.

The internal workings of the MK 4027 can be best summarized by referring to the Functional Flow Chart in figure 5. From this brief outline of the internal operation of the device it is easy to see how the MK 4027 is capable of so many different and flexible timing modes. Besides the usual read, write, and read-modify-write cycles, the MK 4027 is also capable of "page-mode" cycles (very useful in Direct Memory Access operation) and "delayed-write" cycles (very useful in shift register applications.) While keeping in mind the internal structure of the MK 4027 it is now appropriate to delve into a more detailed discussion of the external characteristics and system implications of the MK 4027 memory device.

EXTERNAL DEVICE CHARACTERISTICS

ADDRESSING

As stated earlier, the 12 address bits required to decode one of the 4096 cell locations within the MK 4027 are multiplexed onto the 6 address inputs and latched into the on-chip address latches by externally applying two negative-going, TTL-level clocks. The first clock, the Row Address Strobe ($\overline{RAS}$), latches the 6 row address bits into the chip. The second clock, the Column Address Strobe ($\overline{CAS}$), subsequently latches the 6 column address bits plus Chip Select ($\overline{CS}$) into the chip. Each of these clock signals, $\overline{RAS}$ and $\overline{CAS}$, triggers off a sequence of events which are controlled by different delayed internal clocks. The two clock chains are linked together logically in such a way that the address multiplexing operation is done outside of the critical path timing sequence for read data access. The later events in the $\overline{CAS}$ clock sequence are inhibited until the occurence of a delayed signal derived from the $\overline{RAS}$ clock chain. This "gated $\overline{CAS}$" features allows the $\overline{CAS}$ clock to be externally activated as soon as the Row Address Hold Time specification (t_{RAH}) has been satisfied and the 6 address inputs have been changed from Row address to Column address information. This results in a system limit of $t_{RCD} = t_{RAH} + t_T + t_{ASC}$ ($t_T =$ one transition time).

Note that $\overline{CAS}$ can be activated at any time after t_{RAH} and it will have no affect on the worst case data access time (t_{RAC}) up to the point in time when the delayed row clock no longer inhibits the remaining sequence of column clocks. Two timing end points result from the internal gating of $\overline{CAS}$ which are called t_{RCD} (min) and t_{RCD} (max). No

data storage or reading errors will result if $\overline{CAS}$ is applied to MK 4027 at a point in time beyond the t_{RCD} (max) limit. However, access time will then be determined exclusively by the access time for $\overline{CAS}$ (t_{CAC}) rather than from $\overline{RAS}$ (t_{RAC}), and access time from $\overline{RAS}$ will be lengthened by the amount that t_{RCD} exceeds the t_{RCD} (max) limit.

The significance of this "gated $\overline{CAS}$" feature is that it allows a multiplexed circuit, such as the MK 4027, to be comparable in performance (access time) with non-multiplexed devices such as the 18- and 22-pin 4K RAMs. In essence, it allows the designer to compensate for system timing skews that may be encountered in the multiplexing operation when addressing the device. In the MK 4027, the "window" available for multiplexing from row address to column address information while still achieving minimum access time (t_{RAC}) is a full 25% of access time.

MEMORY CYCLES

Once the MK 4027 is properly addressed, the device is capable of performing various types of memory cycles. Selection of the various cycles, whether read, write or some combination thereof, is controlled by a combination of $\overline{CAS}$ and $\overline{WRITE}$ while $\overline{RAS}$ is active. Also, since Chip Select ($\overline{CS}$) does not have to be valid until $\overline{CAS}$, which is well into the memory cycle, it is possible to start a cycle before it is known which is the selected device.

Data is retrieved from the memory in a read-only cycle by maintaining $\overline{WRITE}$ in the inactive or high state throughout the portion of the memory cycle in which $\overline{CAS}$ is active. Data read from the selected cell will be available at the output within the specified access time.

Data to be written into a selected cell is latched into an on-chip register by a combination of $\overline{WRITE}$ and $\overline{CAS}$ while $\overline{RAS}$ is active. The later of these signals ($\overline{WRITE}$ or $\overline{CAS}$) to make its negative transition is the strobe for the Data-In register. This permits several options in the write cycle timing. In a write cycle, if the $\overline{WRITE}$ input is brought low prior to $\overline{CAS}$, the Data In is strobed in by $\overline{CAS}$, and the set-up and hold times are referenced to $\overline{CAS}$. If the data input is not available at $\overline{CAS}$ time or if it is desired that the cycle be a read-write cycle, the $\overline{WRITE}$ signal will be delayed until after $\overline{CAS}$ goes low. In this "delayed write cycle" the data input set-up and hold times are referenced to the negative edge of $\overline{WRITE}$ rather than to $\overline{CAS}$. Note that delaying $\overline{WRITE}$ until after the negative edge of $\overline{CAS}$ is termed a "read-write cycle" rather than read-modify-write. In a read-write cycle, it is not necessary to wait until data is valid at the output before the write operation is started. This feature is very useful when the MK 4027 is used in sequential memory applications or in systems that employ "interleaving techniques." However, if a true read-modify-write cycle is required (where the write operation occurs after read access), then $\overline{WRITE}$ can occur while $\overline{RAS}$ and $\overline{CAS}$ are still active and after t_{CAC}.

To take full advantage of this $\overline{CAS}/\overline{WRITE}$ signal relationship it is necessary for one to understand how the Data Out Latch is controlled. The most important fact to remember is that any change in the condition of the Data Out Latch is initiated by the $\overline{CAS}$ negative edge. The output buffer is not affected by memory cycles in which only the $\overline{RAS}$ signal is applied to the MK 4027. Whenever $\overline{CAS}$ makes a negative transition, the output will go unconditionally open-

circuited, independent of the state of any other input to the chip. If the cycle in progress is a read, read-modify-write, or a delayed write cycle and the chip is selected, then the output latch and buffer will again go active, and at access time will contain the data read from the selected cell. This output data is the same polarity (not inverted) as the input data. If the cycle in progress is a write cycle ($\overline{WRITE}$ active low before $\overline{CAS}$ goes low) and the chip is selected, then at access time the output latch and buffer will contain the input data. Once having gone active, the output will remain valid until the MK 4027 receives the next $\overline{CAS}$ negative edge. Intervening refresh cycles in which $\overline{RAS}$ is received, but no $\overline{CAS}$, will not cause valid data to be affected. Conversely, the output will assume the open-circuited state during any cycle in which the MK 4027 receives a $\overline{CAS}$ but no $\overline{RAS}$ signal (regardless of the state of any other inputs). The output will also assume the open-circuit state in normal cycles if the chip is unselected. Note that if the chip is unselected ($\overline{CS}$ high at $\overline{CAS}$ time) $\overline{WRITE}$ commands are not executed and, consequently, data stored in the memory is unaffected.

The three-state data output buffer presents the data output pin with a low impedance to V_{CC} for a logic 1 and a low impedance to V_{SS} (Ground) for a logic 0. The effective resistance to V_{CC} (logic "1" state) is 420Ω maximum and < 100 Ω typically. The resistance to V_{SS} (logic "0" state) is 125Ω maximum and < 50Ω typically. The separate V_{CC} pin allows the output buffer to be powered from the positive supply voltage of the logic to which the chip is interfaced. During battery standby operation, the V_{CC} pin may have power removed without affecting the MK 4027 refresh operation. This allows all system logic except the $\overline{RAS}$ timing circuitry and the refresh address logic to be turned off during battery standby to conserve power.

Specified on the MK 4027 data sheet are two electrical characteristics of the device which guarantee the appropriate state of the data output during a write cycle. These two specifications, $\overline{RAS}$ to $\overline{WRITE}$ delay (t_{RWD}) and $\overline{CAS}$ to $\overline{WRITE}$ delay (t_{CWD}) are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. The values listed in the "minimum" and "maximum"

THESE PARAMETERS APPLY TO ALL MK 4027 MEMORY CYCLES:

SYMBOL	DEFINITION
t_{RFSH}	Maximum time that the device will retain stored data without being refreshed.
t_{RP}	$\overline{RAS}$ precharge, or $\overline{RAS}$ inactive time of a cycle.
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ lead time. Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
t_{ASR}	Row address set-up time.
t_{RAH}	Row address hold time.
t_{ASC}	Column address set-up time.
t_{CAH}	Column address hold time.
t_{CSH}	Column address strobe hold time
t_{AR}	Column address hold time referenced to $\overline{RAS}$.
t_{CSC}	Chip select set-up time.
t_{CH}	Chip select hold time.
t_{CHR}	Chip select hold time referenced to $\overline{RAS}$.
t_{CRP}	$\overline{CAS}$ inactive to $\overline{RAS}$ active precharge time.
t_{OFF}	Output buffer turn-off delay.
t_{RAS}	$\overline{RAS}$ pulse width or active time.
t_{CAS}	$\overline{CAS}$ pulse width or active time.
t_{RAC}	Access time from $\overline{RAS}$ falling edge.
t_{CAC}	Access time from $\overline{CAS}$ falling edge.
t_T	Transition time (rise and fall). Transition times are measured between V_{IHC} or V_{IH} and V_{IL}. V_{IHC} (min) or V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.

columns should be inserted as terms in the following equations:

1. If $t_{CWD} + t_T \leqslant t_{CWD}$ (min), the data out latch will contain the data written into the selected cell.

2. If $t_{CWD} \geqslant t_{CWD}$ (max) + t_T and $t_{RWD} \geqslant t_{RWD}$ (max) + t_T, the data out latch will contain the data read from the selected cell.

3. If t_{CWD} does not meet the above constraints then the data out latch will contain indeterminate data at access time.

The following diagrams are representations of the MK 4027 timing waveforms for read, write and delayed-write or read-modify-write cycles. A list of the timing parameters associated with each cycle is also included.

READ CYCLE
Figure 6

READ CYCLE ONLY

t_{RC}	Random read or write cycle time. t_{RC} (min) $\geqslant$ $t_T + t_{RAS} + t_T + t_{RP}$.
t_{RCS}	Read command set-up time.
t_{RCH}	Read command hold time.
t_{ACC}*	Device access time, t_{ACC}, is the longer of two calculated intervals: 1. $t_{ACC} = t_{RAC}$, or 2. $t_{ACC} = t_{RCD} + t_T + t_{CAC}$ * This parameter is not shown in the timing waveforms.
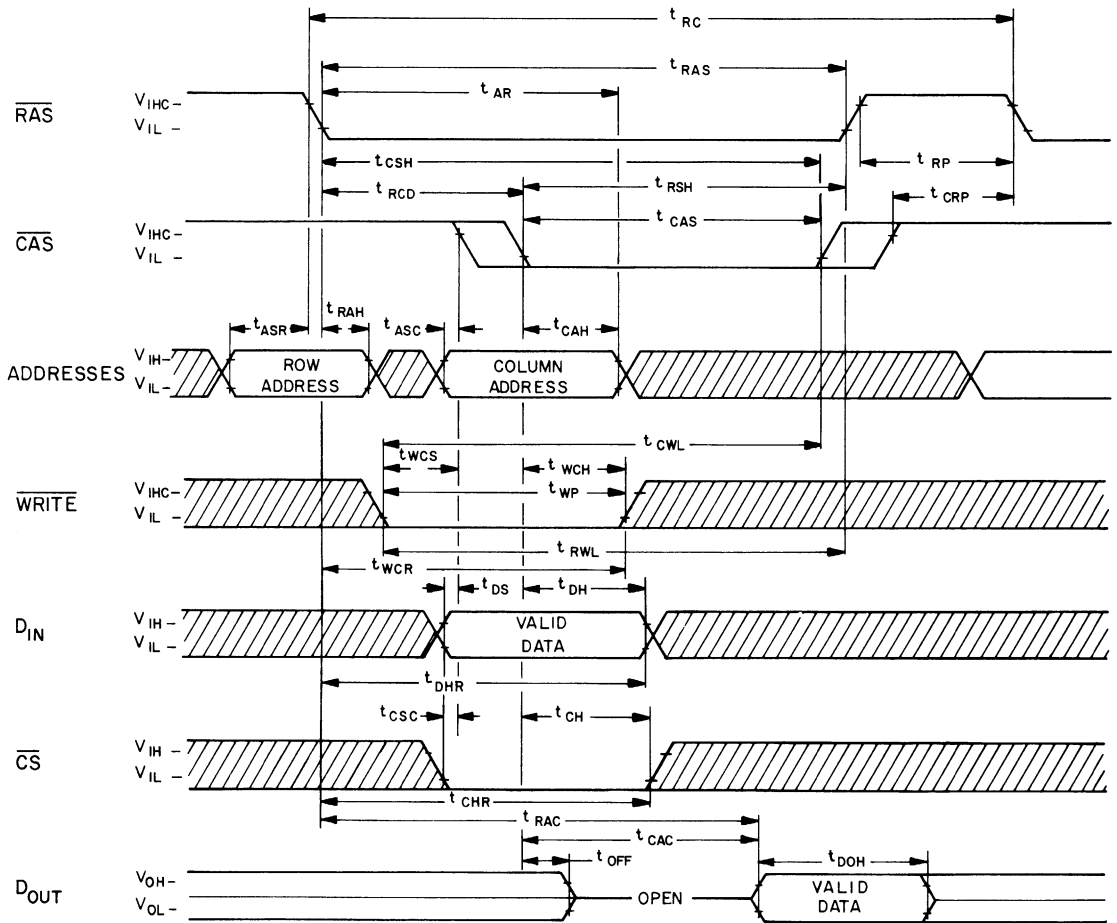
WRITE CYCLE ONLY

tRC	Random read or write cycle time. t_{RC} (min) $\geqslant t_T + t_{RAS} + t_T + t_{RP}$.
tWCH	Write command hold time referenced to $\overline{CAS}$.
tWCR	Write command hold time referenced to $\overline{RAS}$.
tWP	Write command pulse width.
tRWL	Write command to $\overline{RAS}$ lead time.
tCWL	Write command to $\overline{CAS}$ lead time.
tDS	Data In set-up time (referenced to $\overline{CAS}$).
tDH	Data In hold time (referenced to $\overline{CAS}$)
tDHR	Data In hold time (referenced to $\overline{RAS}$)

READ - WRITE / READ - MODIFY - WRITE CYCLE
Figure 8
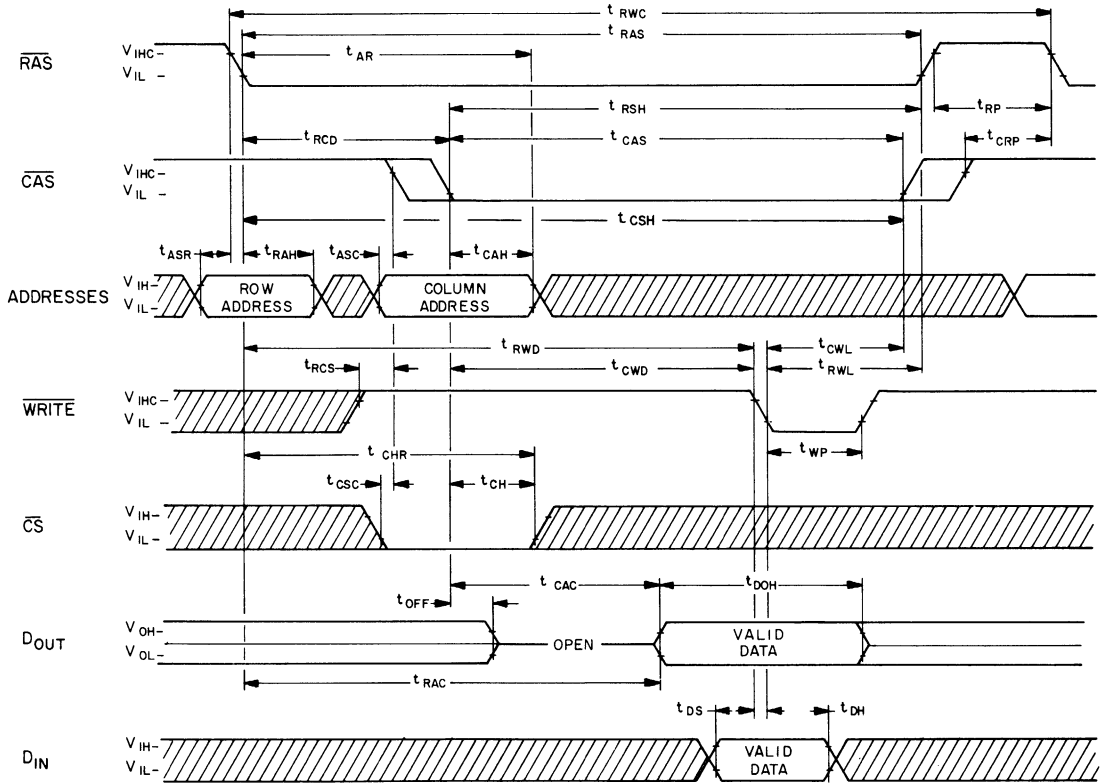
READ/WRITE CYCLE

tRWC	Read-write or "delayed write" cycle time. t_{RWC} (min) $\geq$ $t_T + t_{RCD} + t_T + T_{CWD} + t_{RWL} + t_T + t_{RP}$. This is the minimum time to insure that both a read and write operation will occur at the same address in a single memory cycle.
tRCS	Read command set-up time.
tWP	Write command pulse width.
tRWD	$\overline{RAS}$ to $\overline{WRITE}$ delay.
tCWD	$\overline{CAS}$ to $\overline{WRITE}$ delay.
tRWL	Write command to $\overline{RAS}$ lead time.
tCWL	Write command to $\overline{CAS}$ lead time.
tDS	Data In set-up time (referenced to $\overline{WRITE}$).
tDH	Data In hold time (referenced to $\overline{WRITE}$).

PAGE MODE READ CYCLE
Figure 9
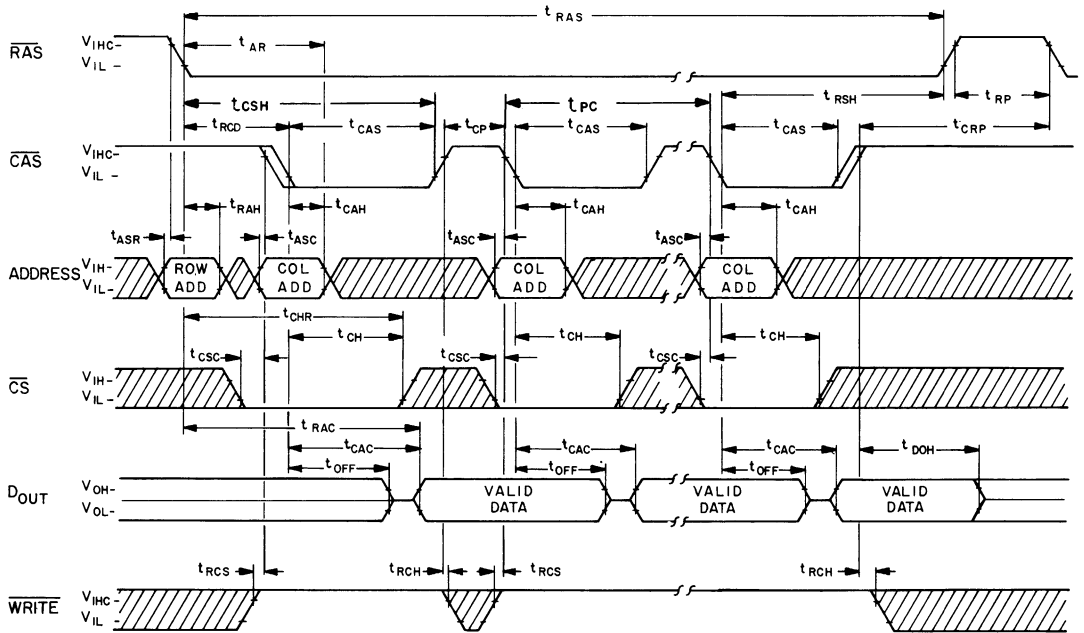
PAGE MODE WRITE CYCLE
Figure 10
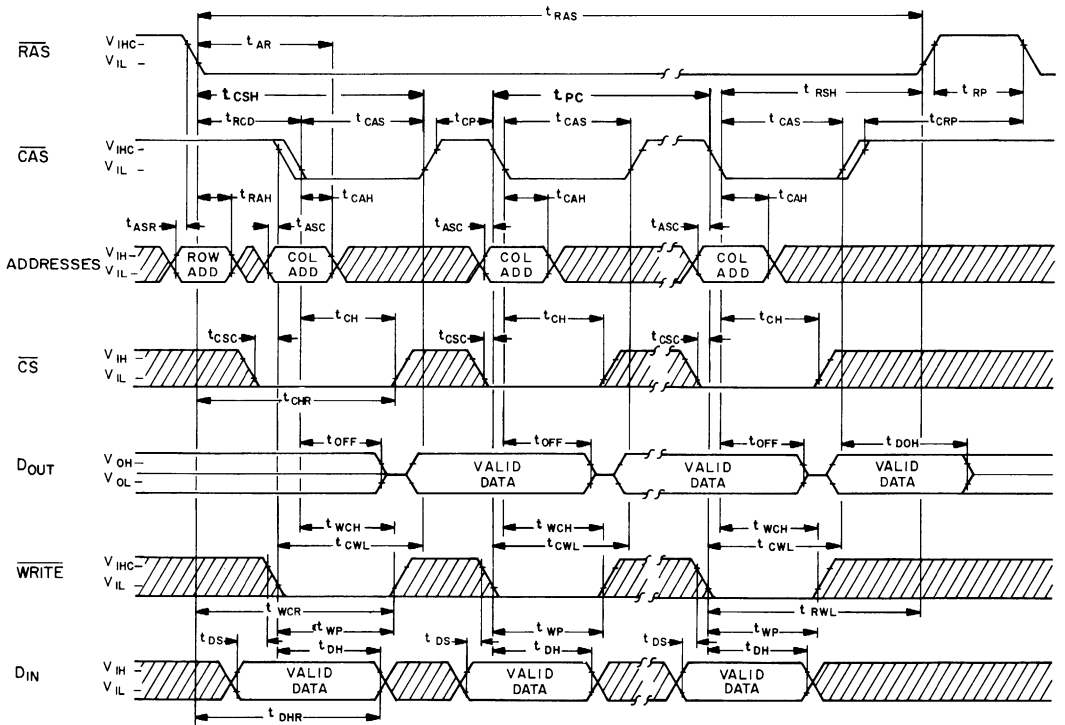
PAGE MODE

Keeping in mind the above mentioned cycle operations, it is now appropriate to introduce another category of memory cycles. The "page-mode" operation allows for successive memory operations at multiple column locations at the same row address with increased speed and with decreased power. This is done by strobing the row address into the chip and keeping the $\overline{RAS}$ signal active (at a logic 0) throughout all successive memory cycles in which the row address is common. This "page-mode" operation will not dissipate the power associated with the negative going edge of $\overline{RAS}$. Also, the time required for strobing in a new row address is eliminated, thereby decreasing the access and cycle times. Every type of cycle–read, write, read-modify-write and delayed-write cycles–can all be performed in the page mode. Also, the chip select ($\overline{CS}$) is operative in page mode just as in normal cycles. It is not necessary that the chip be selected during the first cycle for subsequent cycles to be selected properly in a page operation. Likewise, the $\overline{CS}$ input can be used to select or disable any cycle (s) in a series of "page" cycles. This feature allows the page boundary to be extended beyond the 64 column locations in a single chip. The page boundary can be extended by applying $\overline{RAS}$ to multiple 4K memory blocks and decoding $\overline{CS}$ to select the proper block.

The addition of page mode to the MK 4027's repertoire of features adds only two additional constraints to the timing parameters mentioned earlier. The first constraint is that the length of time that a single chip can remain in the page mode is limited to the maximum $\overline{RAS}$ pulse width (t_{RAS}) as specified on the data sheet. Second, the $\overline{CAS}$ precharge time (t_{CP}), or the time from the positive edge of $\overline{CAS}$ in one page cycle to the negative edge of $\overline{CAS}$ in subsequent page cycles must be obeyed.

The following timing waveforms illustrate the page mode operation. Note that the page-mode write cycle depicts the Data In set-up and hold times referenced to $\overline{WRITE}$ rather than $\overline{CAS}$. Once again, this is to illustrate the flexibility of the write cycle operation. Page-mode operation is particularly useful in transferring large blocks of data into or out of memory.

REFRESH

Refresh of the dynamic cell matrix is accomplished by performing a memory cycle at each of the 64 row addresses within each 2 millisecond time interval.

Any cycle in which a $\overline{RAS}$ signal occurs, accomplishes a refresh operation. A read cycle will refresh the selected row, regardless of the state of the Chip Select ($\overline{CS}$) input. A write or read-modify-write cycle also refreshes the selected row, but the chip should be unselected to prevent writing data into the selected cell. If during a refresh cycle, the MK 4027 receives a $\overline{RAS}$ signal but no $\overline{CAS}$ signal, the state of the output will not be affected. Therefore, data from the previous cycle will remain valid throughout the refresh cycle. However, if "$\overline{RAS}$-only" refresh cycles (where $\overline{RAS}$ is the only signal applied to the chip) are continued for extended periods, the output buffer may eventually lose proper data and go open-circuit. The output buffer will regain activity with the first cycle in which $\overline{CAS}$ is applied to the chip.

The following diagram illustrates the "$\overline{RAS}$-only" refresh cycle:

POWER DISSIPATION

The worst case power dissipation of the MK 4027, continuously operating at the fastest cycle rate, is the sum of [V_{DD} (max) X I_{DD} (max) plus V_{BB} (max) X I_{BB} (max)], where maximum currents are the maximum currents averaged over one memory cycle. The worst case power for the MK 4027 with a cycle rate of 375 nanoseconds is less than 470mW, while the typical power is 170 mW at a 1 μs cycle time.

Typical power supply current waveforms for various types of memory cycles are shown in figure 12. From this picture it is easy to see that most of the power drawn by the MK 4027 is the result of an address strobe charging the capacitances of various internal circuit nodes.

Note also that there is very small DC component in the current waveforms, independent of how long the address strobes remain active. This is because most of the circuitry in the MK 4027 is dynamic, with the exception of the $\overline{RAS}$ input buffer.

The first portion of the current waveforms illustrates a normal $\overline{RAS}/\overline{CAS}$ memory cycle. As expected, the I_{DD} waveform has three major current peaks above ground level. These occur when $\overline{RAS}$ goes active, then when $\overline{CAS}$ internally goes active, and finally when both $\overline{RAS}$ and $\overline{CAS}$ go back into precharge. On the other hand, both positive and negative current transients are associated with I_{BB}. This results in peak currents that can be two to four orders of magnitude higher than the average D C value.

The second cycle is representative of a page-mode cycle in which $\overline{CAS}$ is completely enveloped by $\overline{RAS}$.

"RAS ONLY" REFRESH CYCLE
Figure 11
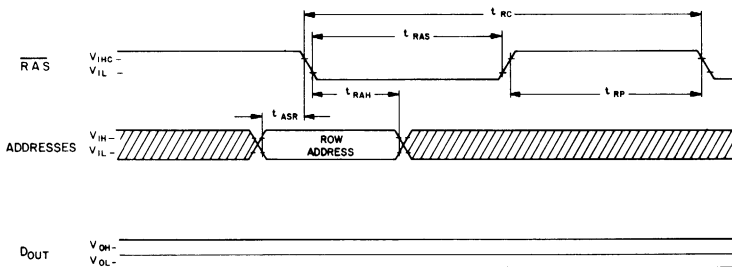
Note that delaying $\overline{CAS}$ until well after $\overline{RAS}$ goes negative demonstrates the relative contributions of $\overline{RAS}$ and $\overline{CAS}$ to total power. This type of cycle operation has the effect of reducing the peak current associated with $\overline{RAS}$ and $\overline{CAS}$ going into precharge simultaneously. Instead, two smaller current spikes are generated, each coinciding with the separate termination of $\overline{CAS}$ and $\overline{RAS}$. From the current waveform it is clear that approximately 60% of all active power is due to $\overline{RAS}$ and only about 40% of all active power is due to $\overline{CAS}$. Thus, even with increased frequency, the maximum power dissipated in a page-mode operation is less than that in a normal cycle.

The third cycle is a "$\overline{RAS}$-only" cycle which can be used for the refresh operation. Note that the MK 4027 will dissipate considerably less power when the refresh operation is accomplished with a "$\overline{RAS}$-only" cycle as opposed to a normal $\overline{RAS}/\overline{CAS}$ cycle.

TESTING THE MK 4027 MEMORY DEVICE

Production testing of each MK 4027 memory device begins early in the process of every MK 4027 wafer. Once a wafer is processed, each individual die on that wafer is subjected to probe testing. This is where each die is probed and tested for functionality, leakage and continuity. All die that pass this test are then packaged and subjected to further Quality Assurance Processing.

The next barrage of tests include the following:

100% Pre-burn testing at high temperature (for function, leakage, and continuity)

100% Temperature Cycling-screened to 10 cycles, $-65°C$ to $+150°C$

100% Centrifuge - screened to insure positive die and bond attachment

100% Dynamic Burn-In - each device is operated at conditions well beyond data sheet limits for many hours to insure that only quality devices reach the end user.

All MK 4027 devices that pass the previous tests are then final tested for customer use. At final test, all devices are tested at high temperature, to all data sheet AC and DC specifications with wide guardbands. This type of Quality Assurance Processing and Testing insures that not only does every MK 4027 perform well within the established data sheet limits, but also exhibits the quality and reliability standards necessary for today's (and tomorrow's) data processing applications.

Thorough testing of every MK 4027 is performed on what MOSTEK calls "MASTER TESTERS." These machines incorporate a very versatile pattern generator made by Computest and a very sophisticated parametric measurement unit (PMU) and clock section that was conceived and constructed by MOSTEK Test Equipment design engineers. This combination of purchased and custom designed hardware is controlled by a PDP-11 minicomputer. These MASTER TESTERS are used not only in production testing but also in the engineering characterization of the MK 4027. This permits excellent correlation between characterization and production testing on the device. The test equipment is also used as an analysis tool in

RAS / CAS CYCLE - LONG RAS / CAS CYCLE - RAS ONLY CYCLE
Figure 12
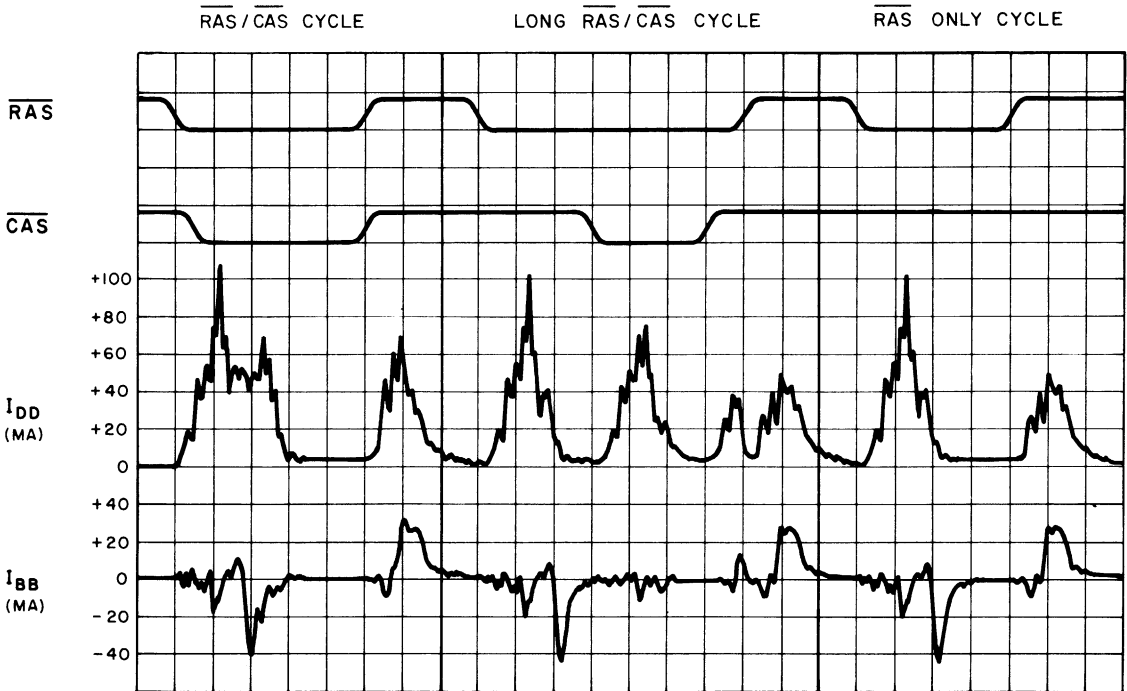
MOSTEK's 4K testing area.

circuitry shown below. Note that this is for testing purposes only and is certainly not required or recommended for system use.

MK 4027 ADDRESS INTERPOLATION
Figure 13
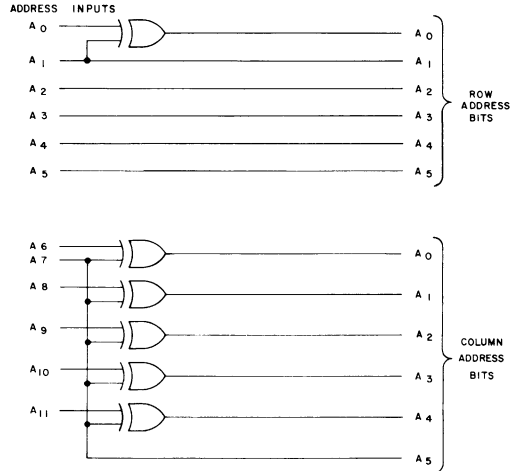
the "continuing engineering" phase of MK 4027 production.

Establishing one's own incoming inspection and testing procedures for a device as complicated as a 4K dynamic RAM is one of the most important and critical procedures in any production program. Usually the effectiveness of the screening procedure may not be known until several assembled systems have been field tested for several months. Therefore, it is important that proper screening procedures are employed early in any production program.

Many times, in establishing electrical end-point tests, it is necessary to know the proper external addressing sequence to insure sequential addressing within a memory device. The internal address bit map of the MK 4027 is arranged in a somewhat unusual fashion to keep the chip size to a minimum. Therefore, sequentially addressing the MK 4027 cannot be done with a straight binary count without the

Also, since the sense amplifiers within the MK 4027 are located in the center of the memory matrix, data stored in half of the memory will be inverted from the data presented at the input pin. Once again, this inversion is completely transparent to the user (i.e., data stored in the memory as a "1" or "0" at the input will, when subsequently accessed, appear as a "1" or "0" respectively at the output). However, if one wishes to determine the polarity of data stored in the memory, refer to the following chart.

ROW ADDRESS A_5	DATA STORED
0	inverted data
1	true data

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MOSTEK®

16K-THE NEW GENERATION DYNAMIC RAM

By DERRELL COKER

Technical Brief

Extensive design effort has been expended in the development of 16K RAMs to insure that many of the problems and peculiarities of the previous generation RAMs (1K's and 4K's) have been eliminated. This paper will show how such undesirable device characteristics as excessive power dissipation, inadequate noise margins (at the input and output terminals), restrictive timing, and unexplained "soft errors", have all been designed out of the new generation 16K dynamic RAMs.

Looking back at some of the popular MOS RAMs of the early 1970's, one cannot help but remember the many different device configurations, each with its own peculiar operating modes and timing restrictions. Memory devices have emerged which require multiphase, high level clocks and others with multiplexed address inputs and/or multiplexed I/O. With a strong move towards standardization, the semiconductor memory industry is in a much more fortunate situation with 16K RAMs than with any previous memory product. Never before could the user experience such numerous benefits from a single memory device.

16K Technology Overview

Before delving into the user benefits and features of 16K RAMs, it is first necessary to take a look at two of the most important, yet most often ignored aspects of a device – chip architecture and process. These two elements combine to serve as a reference point for comparing any LSI device to a similar one, and for establishing a device as a "state-of-the-art" product.

MK 4116 FUNCTIONAL DIAGRAM
Figure 1.
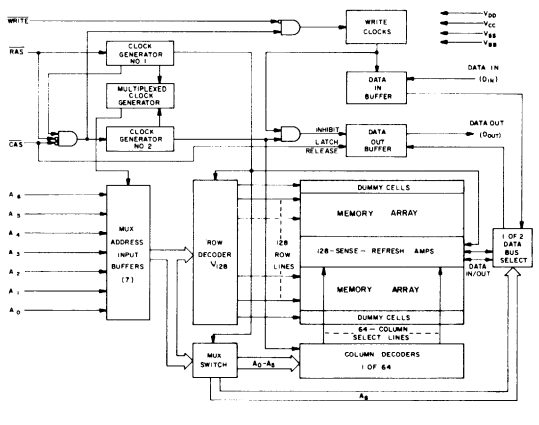
The block diagram (functional layout) of the MOSTEK MK 4116 appears in Figure 1. The chip is organized internally as two 8K sub-arrays which form a single 128x128 balanced array. The column decoder and sense-refresh amplifiers are in the middle of the matrix and "dummy cells" are located at each side. The "dummy cells" establish a voltage reference for the balanced sense amplifiers. One of the array halves inverts data and will store an input "one" as a low level in the storage cell (a second inversion is performed by the output circuitry so that this internal inversion is not seen at the device terminals). The control circuitry surrounding the array is controlled by networks of clock generators which are activated by the externally applied Row and Column Address Strobe ($\overline{RAS}$ and $\overline{CAS}$) signals. Access time is determined exclusively by clock delays internal to the circuit and is influenced only by influencing these internal delays. This design feature can greatly inpact testing since there is no reason to search for a test sequence or data pattern which is worst-case for access time. As a final comment, note that the address input buffers are multiplexed between row and column addresses while the row and column decoders are independent circuits. This greatly reduces the input capacitance at these terminals over previous multiplexed RAMs where each address pin was connected to two input buffer circuits.

As with most 16K RAM devices, the MOSTEK MK 4116 is fabricated with a two level N-channel polysilicon gate process and a single transistor dynamic storage cell. The two level polysilicon process greatly enhances circuit density without a substantial increase in process complexity over the standard single level N-channel polysilicon process. Both processes, however, allow independent adjustment of gate and field oxide thresholds by ion-implantation which maximizes performance, density, and reliability.

The layout of the storage cell in the MK 4116 is shown in Figure 2. This is a conventional one-transistor dynamic storage cell implemented with MOSTEK's double-level polysilicon (Poly II) process. The row (word) select lines are metal eliminating concern over propagation delays down the long (80 mil) word lines. Data transfer to and from the cell is through the diffused column (digit) lines. The top plate of the storage capacitor is V_{DD} (first level of polysilicon) which allows charge to be stored in the depleted region beneath this level. Metal word lines contact the second poly level which forms the gate of the transfer device isolating the storage cell from the digit line. The cell is relatively insensitive to variations in the doping level of both first and second poly. In fact, performance of the cell is primarily influenced by junction depth, oxide thickness, and mask geometry, all parameters which tend to remain constant.

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MK 4116 CELL LAYOUT
Figure 2.

WORD LINE

WORD LINE

WORD LINE

DIGIT LINE

ACTIVE —
POLY I —·—·—
POLY II ········
METAL — — —
CONTACT X

A cross section of a single storage cell is shown in Figure 3. Using the standard silicon gate process this cell would be made of two elements – the pass transistor and a storage capacitor. However, because of the use of two levels of poly-silicon, no layout space is required to separate these components and, therefore, should be regarded as one component only. Actual dimensions of the double-poly cell are approximately 14.5 μm x 30 μm. It is estimated that by the end of 1977, further refinements of the basic five mask Poly II* process technology will produce 16K RAM devices with an overall chip area less than 18,000 mil^2.

MK 4116 CELL AND CROSS-SECTION
Figure 3.

METAL

POLY I   POLY II

N$^+$

| POLY I CAPACITOR | POLY II TRANSISTOR | DIFFUSED BIT LINE |

METAL
WORD LINE

POLY II

POLY I

BIT LINE
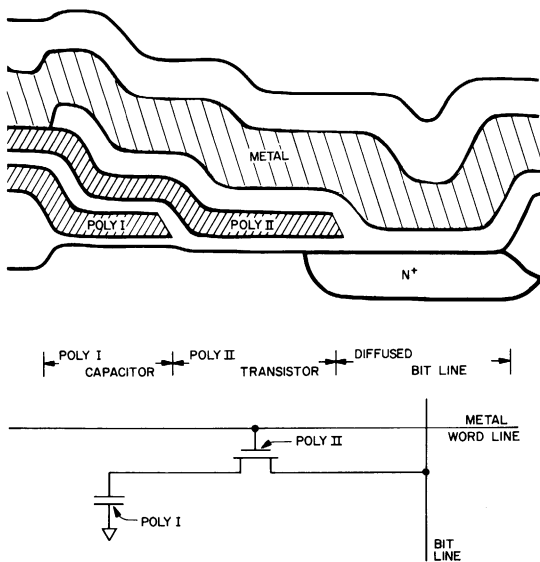
* Actually, the Poly II process uses a total of seven mask steps. However, only five mask steps are required to define the product; the other two are very non-critical mask operations which enhance device reliability and improve yield.

<u>Timing Considerations</u>

Although the multiplexed address 16K RAM requires two strobe signals ($\overline{RAS}$ and $\overline{CAS}$) for control purposes, the timing of these clocks is very flexible when compared to the original multiplexed RAM introduced in 1973. The original design made no allowances for the additional time required to perform the address multiplexing. Also, since the internal $\overline{RAS}$ and $\overline{CAS}$ clock generators functioned totally independent of one another, several unnecessary restrictions were put on the "precharge" and "refresh" operations. Several 16K RAM designs (including MOSTEK's MK 4116) have overcome these timing inconveniences by enhancing the operation of the internal clock generators and implementing a feature called "gated $\overline{CAS}$".

The inclusion of the "gated $\overline{CAS}$" feature allows for more flexible timing on the $\overline{RAS}$ to $\overline{CAS}$ delay time specification so that the system designer can compensate for timing skews and "uncertainties" that may be encountered in the multiplexing operation (refer to Figure 4).

READ CYCLE
Figure 4.

READ CYCLE

$\overline{RAS}$

$t_{RCD(max)}$
$t_{RCD(min)}$

$\overline{CAS}$

t_{RAH}

ADDRESSES   ROW   COLUMN

$\overline{WRITE}$

D_{IN}

t_{CAC}
t_{RAC} t_{OFF}

D_{OUT} VALID DATA
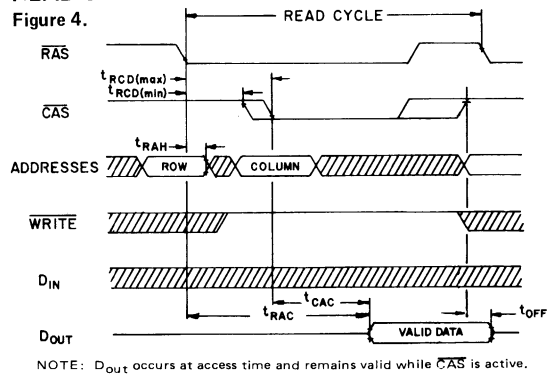
NOTE: D_{out} occurs at access time and remains valid while $\overline{CAS}$ is active.

Each of the control signals, $\overline{RAS}$ and $\overline{CAS}$, triggers a sequence of events which are controlled by different delayed internal clocks. The two clock chains, as illustrated in Figure 5, are linked together logically such that the address multiplexing operation is done outside of the critical path timing sequence for read data access.

GATED INTERNAL CLOCK CIRCUITRY
Figure 5.
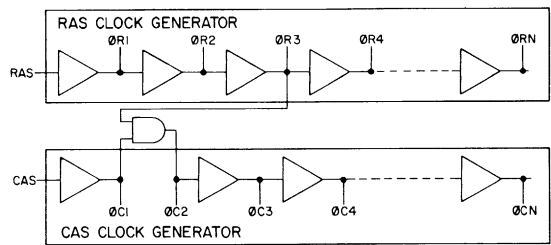
RAS CLOCK GENERATOR
ØRI   ØR2   ØR3   ØR4   ØRN
RAS

CAS
ØCI   ØC2   ØC3   ØC4   ØCN
CAS CLOCK GENERATOR

The later events in the $\overline{CAS}$ clock sequence are inhibited until the occurance of a delayed signal derived from the $\overline{RAS}$ clock chain. This "gated $\overline{CAS}$" feature allows the $\overline{CAS}$ clock to be externally activated as soon as the Row Address Hold Time (tRAH) specification has been satisfied and the address inputs have been changed from Row Address to Column Address information.

Note that $\overline{CAS}$ can be activated at any time after tRAH and it will have no effect on the worst-case data access time (tRAC) up to the point in time when the delayed row clock no longer inhibits the remaining sequence of column clocks. Two timing end-points result from the internal gating of $\overline{CAS}$ which are called tRCD (min) and tRCD (max). No data storage or reading errors will result if $\overline{CAS}$ is applied to the device at a point in time beyond the tRCD (max) limit. However, access time will then be determined exclusively by the access time from $\overline{CAS}$ (tCAC) rather than from $\overline{RAS}$ (tRAC), and access time from $\overline{RAS}$ will be lengthened by the amount that tRCD exceeds the tRCD (max) limit. This relationship is depicted in Figure 6.

GATED CAS TIMING RELATIONSHIP
Figure 6.
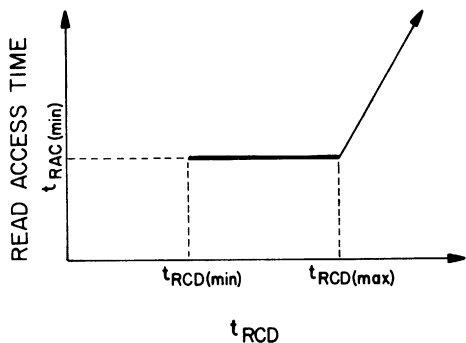
Also, as a result of the entertwined clock generators, precharge of all internal circuitry is initiated by $\overline{RAS}$ going to the inactive state. This removes several timing restrictions from the trailing edge of $\overline{CAS}$, allowing the simplified "$\overline{RAS}$ only" refresh operation as well as improved operation of the Data Output.

WRITE CYCLE
Figure 7
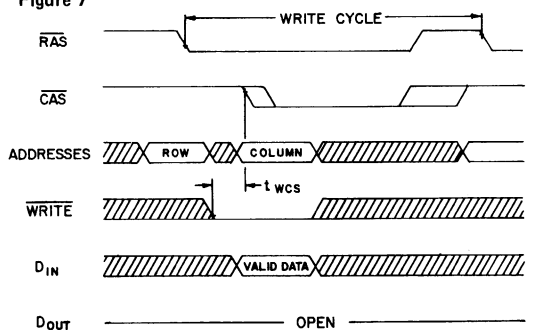
NOTE: If, WRITE command occurs before $\overline{CAS}$, then D_{out} remains high impedance.

Basically, Data Out of the "unlatched" type of 16K RAM is valid within the specified access time and will remain valid until the Column Address Strobe ($\overline{CAS}$) is taken to the inactive state. However, in early write cycles ($\overline{WRITE}$ active low before $\overline{CAS}$ goes low, see Figure 7) the data output will remain in the high impedance (open-circuit) state throughout the entire cycle. This type of output operation results in some very significant system implications.

Common I/O Operation — If all write operations are handled in the "early write" mode, then D_{IN} can be connected directly to D_{OUT} for a common I/O data bus.

Data Output Control — D_{OUT} will remain valid during a read cycle from tCAC until $\overline{CAS}$ goes back to a high level (precharge), allowing data to remain valid from one cycle up until a new memory cycle begins with no penalty in cycle time. This makes the $\overline{RAS}/\overline{CAS}$ clock timing relationship very flexible.

Two Methods of Chip Selection — Since D_{OUT} is not latched, $\overline{CAS}$ and/or $\overline{RAS}$ can be decoded for chip selection. If both $\overline{RAS}$ and $\overline{CAS}$ are decoded, then a two dimensional (X,Y) chip select array can be realized.

Noise Margins

The ability of an MOS memory device to interface with logic families outside its own has always been a marginal situation. With the new generation 16K RAM, the problems of high capacitance, high level address inputs have been eliminated along with the old familiar design glitch which caused the address inputs of several popular RAM types to source current out of their input terminals. As veteran designers might recall, this condition injected a significant current spike on the address lines which decreased noise margin and prevented the use of Schottky address drivers in the system. To overcome these problems in 16K RAM design means, that for the first time, MOS memory elements can be surrounded by high performance logic families (Schottky TTL) in the system to achieve maximum performance with adequate noise margins.

To provide wide operating margins and noise immunity desired by users, a special input stage has been incorporated into the MK 4116 to detect true TTL input levels. A circuit schematic of this stage is shown in Figure 8. The principle behind this circuit is a simple differential amplifier which compares the incoming TTL level to an on-chip 1.5 volt reverence level. This type of circuit can be designed to detect "one" levels greater than or equal to 2.2 volts and "zero" levels less than or equal to 0.8 volts.

In the circuit in Figure 8, a positive common mode voltage boost is capacitively coupled to the gates of transistors T3 and T4 to assure that at least one of them is turned on when the "latch" command is initiated from the control clock generator. Note that the input buffer will latch properly even though both the input and reference voltages may be less than the device threshold voltage. The addition of T1 and C1 in the V_{IN} path helps to increase the amount of negative undershoot on V_{IN} which can be tolerated between the time TA goes low and the time the latching action takes place. This type of input circuit

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MK 4116 ADDRESS INPUT BUFFER
Figure 8.
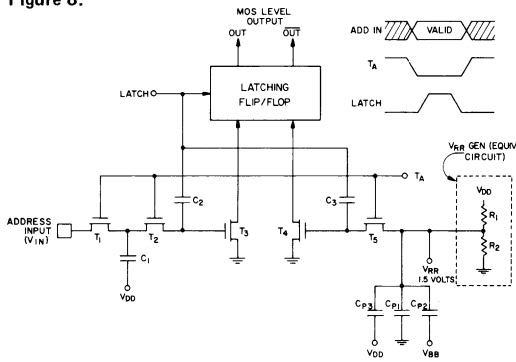
requires the shortest possible address hold times and allows the input circuitry to function independent of device thresholds and other process parameters.

The output drive capability of a RAM is also a very important area of concern. Many times the load circuit which a vendor uses to measure the access time of a device is not representative of typical system loading conditions. If actual system loading is much greater than the load used by the manufacturer to measure access time, then the device will be marginal in the system. With typical system capacitance loading far in excess of 60pF, it is necessary for the new generation 16K RAMS to accommodate two TTL loads in addition to driving 100pF capacitance.

Power Dissipation

A major breakthrough in the reduction of active power dissipation in dynamic RAMs results from the use of dynamic circuitry throughout the entire device, specifically in the sense amplifiers. Without going into a detailed discussion of dynamic RAM design, it will suffice to say that dynamic flipflop type level detector is made possible by providing an access path to both the true and complement sense lines associated with each amplifier. This sense amplifier configuration does not require digit pull-up transistors which are the major source of active power dissipation in a dynamic RAM. Figure 9 is a comparison of the current waveforms (characteristics) of two similar RAMs, one incorporating the dynamic sensing approach and the other using static loads in the sense amp circuits.

The user benefits derived from RAMs designed with dynamic sense amplifiers extends far beyond a simple reduction of the power dissipation. Although low power is of significant importance, even more important is the increased inherent reliability (which will be discussed later) and the impact that the dynamic current characteristics have on system design.

Since most of the power drawn by the MK 4116 is the result of an address strobe transition, the dynamic power is primarily a function of operating frequency rather than active duty cycle (as is the case with "static" sense amp designs). This dynamic current characteristic precludes inadvertent burn-out of the device in the event that the clock inputs become shorted to ground due to system malfunction. With the old conventional design, maximum current is drawn by the device any time the strobe inputs are activated. This is the reason that many of the previous generation RAMs had restrictions on the maximum time the chip enable strobe could remain active.

STATIC VS. DYNAMIC SENSE AMP CHARACTERISTICS
Figure 9.
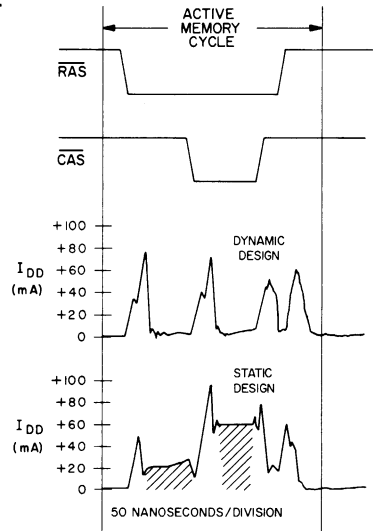
SUPPLY CURRENT VS. CYCLE RATE
Figure 10.
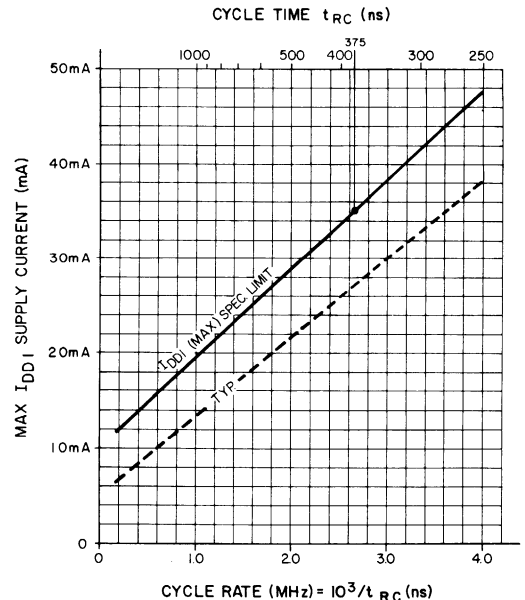
Fig. 10 Maximum I_{DD1} versus cycle rate for device operation at various frequencies. I_{DD1} (max) curve is defined by the equation:
I_{DD1} (max) [mA] $= 10 + 9.4 \times$ cycle rate [MHz].

Not only does the dynamic current characteristic of this device prevent inadvertent burnout, it also allows the manufacturer of such devices to specify the operating power as a function of frequency rather than by a "fixed" condition. As illustrated in Figure 10, this allows the system designer to have a worst-case power specification, guaranteed by the manufacturer, which applies to real "use" conditions.

System Relaibility

Reliability is certainly not a new buzz word in the MOS memory market. Reliability (or in some cases, the lack of it) has been an important topic for many years. As most of the "old-timers" will recall, many of the 1K and early 4K dynamic RAMs exhibited a phenomenon known as "soft failures" that drove even the experts into a state of panic. As 4K RAMs matured it became apparent that something had to be done to improve the reliability of dynamic RAMs and restore the credibility of the manufacturers before the advent of 16K devices.

In evaluating the problems of system reliability, it has been determined that there exists a strong correlation between memory devices which exhibit "soft failures" in systems and memory devices which are intolerent of power supply noise and/or marginal input levels. Discrete device testing may prove that the RAM is functional and meets all specifications; however, what is important to the user is the "real" system environment.

The new 16K RAM devices have overcome the problems associated with power supply noise by insuring proper operation over a wider power supply range — ± 10% rather than ± 5% — and by enhanced testing which closely matches possible user conditions.

POWER SUPPLY TOLERANCE

Figure 11
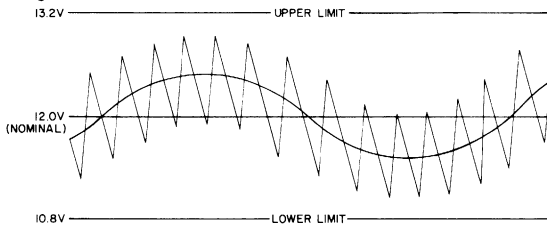
Fig. 11 Power Supply Tolerance: means that any combination of (1.) nominal DC level, and (2.) low frequency ripple, and (3.) high frequency noise is acceptable so long as the sum of all noise does not go outside the specified plus and minus (±) envelope.

For any dynamic RAM whose storage capacitor is returned to V_{DD} (+12V), a change in V_{DD} between data accesses will capacitively couple onto the storage node. For example, suppose that a low level is written with V_{DD} at its lower limit (10.8V) and that the storage node is discharged to zero volts. If before the next access to this cell the V_{DD} level increases, some percentage (typically about 80%) of this increase will couple onto the storage node. In older RAM designs, the sense amplifier circuits had a tendency to recognize this level as a high rather than the low level which was originally stored.

This condition is further aggravated in dynamic RAMs with the static type of sense amplifiers as described earlier. These high power devices, with their hefty DC current requirement, have a tendency to cause the DC power busses, which are routed through the memory matrix, to droop. The basic nature of a dynamic RAM is such that the current drawn by the device during an active cycle can be several orders of magnitude greater than the current drawn while the device is in standby. This sudden change in current requirement can create seemingly incurable noise problems within a system if proper decoupling is not implemented.

Although no particular power supply noise restriction exists other than the supply voltages remain within the specified limits, adequate decoupling should be provided to suppress high frequency noise resulting from the transient current of the new 16K RAM devices. This insures optimum system performance and reliability. Bulk capacitance requirements are minimal since the MK 4116 draws very little steady state (DC) current. This characteristic of the 16K RAM can greatly reduce the expense and complexity of power supply design. This is especially important when costs of $1 to $1.50/watt are common for a good, quality power subsystem.

In addition to operating margin, memory component power consumption is also a major factor affecting reliability. As described earlier, the technology used to manufacture 16K RAMS produces low power devices which generate little heat and are less prone to failures induced by high temperature. Remember, system reliability is inversely proportional to operating temperature.

CONCLUSION

The new generation 16K RAM devices come closer to answering the needs and addressing the complaints of semiconductor memory users than any previous Random Access Memory Product. These emerging 16K RAM devices are designed and manufactured with the latest state-of-the-art processing techniques; one which requires few devices per memory cell; has simple, easily controlled, mature processing techniques, requires minimal, simple peripheral circuitry; dissipates little power; is free of intrinsic reliability problems; and is manufactured by responsible, careful, and experienced vendors.

REFERENCES

1. Schroeder, P.R.; and Proebsting, R.J.; "A 16K x 1 Bit Dynamic RAM", ISSCC Digest of Technical Papers, Feb., 1977.

2. Owen, R.W.; "Optimized Testing of 16K RAMS", CompCon '77. Digest of Technical Papers, Feb., 1977.

3. Coker, D.C.; "An In-Depth Look at MOSTEK's High Performance MK 4027", Application Note, Jan., 1976.

4. Brown, J.R.; Timing Peculiarities of the 16 Pin Multiplexed Address RAM", Burroughs Technical Memorandum, Nov., 1976.

5. Coker, D.C.; and Davis, K.; "16K RAM - From Micros to Mainframes", CompCon '76 Digest of Technical Papers, Sept., 1976.

6. Proebsting, R.J.; and Green, R.; "A TTL Compatible 4096-Bit N-Channel RAM", ISSCC Digest of Technical Papers, Feb., 1973.

7. Frankenberg, R.J.; "Designers Guide to: Semiconductor Memories", <u>EDN Magazine</u>, 1975.

8. Carey, B.J.; Grossman, H.J.; Jodoin, R.C., Coker, D.C. Squelch Memory System Noise with P-C Board Bus Bars", <u>Electronic Products Magazine</u>, Oct., 1976.

MOSTEK®

COMPATIBLE MK4027 AND MK4116 MEMORY SYSTEM DESIGNS

By DAVID WOOTEN

Application Note

INTRODUCTION

Memory Systems design is very much like any other interface design. It requires knowledge of the system being interfaced to and also an in-depth knowledge of the resource being interfaced. This in-depth knowledge must include the functional and electrical characteristics of the device as well as power requirement, noise sensitivities and driver requirements. This application note will attempt to cover all of the areas that are relevant to designing a memory system using the MK4027 or the MK4116. The discussion centers around a memory board that was designed for the LSI-11* microcomputer. Many of the techniques and methods used in this design can be applied to almost any other memory system design.

THE LSI-11* BUS

The LSI-11* microcomputer bus is used for all data transfers within the system. It has four types of cycles that are of significance to the memory system: read, write, read-modify-write and refresh. The timing for each of these cycles as seen from the interface side of the bus receivers is given in Figs. 1, 2, and 3. Since the memory can never institute a bus cycle it is always a slave device. As can be seen from the timing diagrams, all cycles are interlocked asynchronous. The bus cycles have three phases; device selection, transfer initiation and transfer termination. Device selection (either memory or peripheral) is accomplished by the bus master placing the device address on the multiplexed address-data lines. After allowing time for bus delays, driver-receiver skews and address decode the bus master sends SYNC to signal that a transfer will take place between the bus master and the addressed device. The type of cycle is identified by the state of the WTBT and the REF lines. Transfer initiation occurs when the bus master asserts DIN or DOUT. DIN and DOUT are used to control the direction of data flow. DIN causes the flow to be from slave to master (read cycle) and DOUT from master to slave(write cycle). Transfer termination is caused by the addressed device (slave) asserting RPLY. This indicates to the master that the read data is available on the address/data lines or that the write data has been received by the slave. In response to RPLY the bus master drops DIN or DOUT and the slave in turn drops RPLY. For a read-modify-write cycle the DIN-RPLY sequence is followed by

a DOUT-RPLY sequence. This allows read-modify-write to be done with only one address assertion. The LSI-11* also has a protocol to allow for refresh of dynamic RAMs. Refresh is normally done under control of the LSI-11* microcode. A refresh cycle consists of a DIN-RPLY sequence with RFSH active. During a refresh cycle no data is transferred and only A1-A6 have any significance. These addresses are used to indicate which row of a dynamic RAM is to be refreshed. Sixty-four refresh cycles are generated in a burst every 1.6ms.

READ (REFRESH) CYCLE TIMING
Figure 1
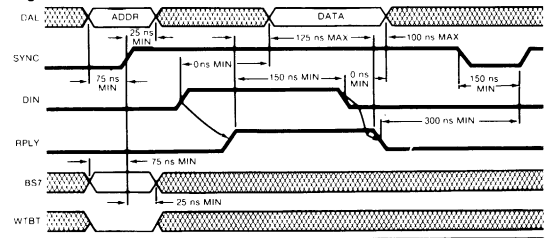
WRITE CYCLE TIMING
Figure 2
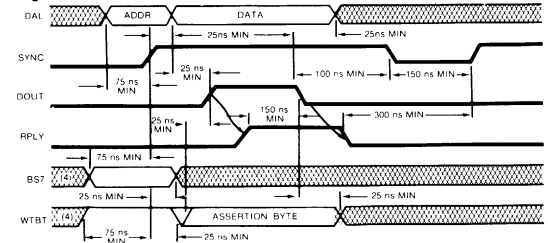
READ MODIFY WRITE CYCLE TIMING
Figure 3
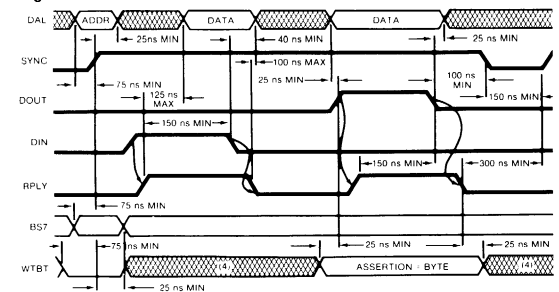
*LSI 11 is a trademark of Digital Equipment Corporation

There are several points about the bus timing that should be mentioned in passing as they will influence some of the decisions made later. Since the transfers on the bus are asynchronous the memory does not have to respond in a fixed period of time. This is unlike many other microprocessors that favor synchronous transfers. Another point that should be made is that the cycle time requirements for the memory are not very stringent. In fact, the absolute minimum cycle time with a Øns access memory is over 800 ns. This leaves quite a bit of 'dead' time in the cycle as far as the memory is concerned.

The final point is that logically there is no difference between transfers between the CPU and memory, or CPU and peripheral. Usually, the upper 4K words of the 32K word address space is reserved for peripheral addresses. When an address within the range is placed on the bus, BS7 is asserted to flag the address as being within the 4K I/O page. There is, however, no reason why the memory cannot be made to respond to some of the addresses in the I/O page as long as it does not conflict with peripheral addresses.

MK4027 FUNCTIONAL DESCRIPTION

Addressing

The 12 address bits required to decode 1 of the 4096 cell locations within the MK 4027 are multiplexed onto the 6 address inputs and latched into the on-chip address latches by externally applying two negative going TTL level clocks. The first clock, the Row Address Strobe ($\overline{RAS}$), latches the 6 row address bits into the chip. The second clock, the Column Address Strobe ($\overline{CAS}$), subsequently latches the 6 column address bits plus Chip Select ($\overline{CS}$) into the chip. The internal circuitry of the MK 4027 is designed to allow the column information to be externally applied to the chip before it is actually required. Because of this, the hold time requirements for the input signals associated with the Column Address Strobe are also referenced to $\overline{RAS}$. However, this gated $\overline{CAS}$ feature allows the system designer to compensate for timing skews that may be encountered in the multiplexing operation. Since the Chip Select signal is not required until $\overline{CAS}$ time, which is well into the memory cycle, its decoding time does not add to system access or cycle time.

Data Input/Output

Data to be written into a selected cell is latched into an on-chip register by a combination of $\overline{WRITE}$ and $\overline{CAS}$ while $\overline{RAS}$ is active. The later of the signals ($\overline{WRITE}$ or $\overline{CAS}$) to make its negative transition is the strobe for the Data In register. This permits several options in the write cycle timing. In a write cycle, if the $\overline{WRITE}$ input is brought low prior to $\overline{CAS}$, the Data In is strobed by $\overline{CAS}$, and the set-up

and hold times are referenced to $\overline{CAS}$. If the data input is not available at $\overline{CAS}$ time or if it is desired that the cycle be a read-write cycle, the $\overline{WRITE}$ signal must be delayed until after $\overline{CAS}$. In this "delayed write cycle" the data input set-up and hold times are referenced to the negative edge of $\overline{WRITE}$ rather than to $\overline{CAS}$. Note that if the chip is unselected ($\overline{CS}$ high at $\overline{CAS}$ time) $\overline{WRITE}$ commands are not executed and, consequently, data stored in the memory is unaffected.

Data is retrieved from the memory in a read cycle by maintaining $\overline{WRITE}$ in the inactive or high state throughout the portion of the memory cycle in which $\overline{CAS}$ is active. Data read from the selected cell will be available at the output within the specified access time.

Data Output Latch

Any change in the condition of the Data Out Latch is initiated by the $\overline{CAS}$ signal. The output buffer is not affected by memory (refresh) cycles in which only the $\overline{RAS}$ signal is applied to the MK 4027. Whenever $\overline{CAS}$ makes a negative transition, the output will go unconditionally open-circuited, independent of the state of any other input to the chip. If the cycle in progress is a read, read-modify-write, or a delayed write cycle and the chip is selected, then the output latch and buffer will again go active and at access time will contain the data read from the selected cell. This output data is the same polarity (not inverted) as the input data. If the cycle in progress is a write cycle ($\overline{WRITE}$ active low before $\overline{CAS}$ goes low) and the chip is selected, then at access time the output latch and buffer will contain the input data. Once having gone active, the output will remain valid until the MK 4027 receives the next $\overline{CAS}$ negative edge. Intervening refresh cycles in which a $\overline{RAS}$ is received (but no $\overline{CAS}$) will not cause valid data to be affected. Conversely, the output will assume the open-circuit state during any cycle in which the MK 4027 receives a $\overline{CAS}$ but no $\overline{RAS}$ signal (regardless of the state of any other inputs). The output will also assume the open circuit state in normal cycles (in which both $\overline{RAS}$ and $\overline{CAS}$ signals occur) if the chip is unselected.

The three-state data output buffer presents the data output pin with a low impedance to V_{CC} for a logic 1 and a low impedance to V_{SS} for a logic 0. The output resistance to V_{CC} (logic 1 state) is 420 Ω maximum and 135 Ω typically. The output resistance to V_{SS} (logic 0 state) is 125 Ω maximum and 35 Ω typically. The separate V_{CC} pin allows the output buffer to be powered from the supply voltage of the logic to which the chip is interfaced. During battery standby operation, the V_{CC} pin may have power removed without affecting the MK 4027 refresh operation. This allows all system logic except the $\overline{RAS}$ timing circuitry and the refresh address logic to be turned off during battery standby to conserve power.

Refresh

Refresh of the dynamic cell matrix is accomplished by performing a memory cycle at each of the 64 row addresses within each 2 millisecond time interval. Any cycle in which a $\overline{RAS}$ signal occurs, accomplishes a refresh operation. A read cycle will refresh the selected row, regardless of the state of the Chip Select ($\overline{CS}$) input. A write or read-modify-write cycle also refreshes the selected row, but the chip should be unselected to prevent writing data into the selected cell. If, during a refresh cycle, the MK 4027 receives a $\overline{RAS}$ signal but no $\overline{CAS}$ signal, the state of the output will not be affected. However, if "$\overline{RAS}$-only" refresh cycles (where $\overline{RAS}$ is the only signal applied to the chip) are continued for extended periods, the output buffer may eventually lose proper data and go open circuit. The output buffer will regain activity with the first cycle in which a $\overline{CAS}$ signal is applied to the chip.

Power Dissipation/Standby Mode

Most of the circuitry in the MK 4027 is dynamic and most of the power drawn is the result of an address strobe edge. Because the power is not drawn during the whole time the strobe is active, the dynamic power is a function of operating frequency rather than active duty cycle. Typically, the power is 170mW at 1 μ sec cycle rate for the MK 4027 with a worse case power of less than 470mW at 320 nsec cycle time. To minimize the overall system power, the Row Address Strobe ($\overline{RAS}$) should be decoded and supplied to only the selected chips. The $\overline{CAS}$ must be supplied to all chips (to turn off the unselected output). Those chips that did not receive a $\overline{RAS}$, however, will not dissipate any power on the $\overline{CAS}$ edges, except for that required to turn off the outputs. If the $\overline{RAS}$ signal is decoded and supplied only to the selected chips, then the Chip Select ($\overline{CS}$) input of all chips can be at a logic 0.

The chips that receive a $\overline{CAS}$ but no $\overline{RAS}$ will be unselected (output open-circuited) regardless of the Chip Select input. For refresh cycles, however, either the $\overline{CS}$ input of all chips must be high or the $\overline{CAS}$ input must be held high to prevent several "wire-OR'd" outputs from turning on with opposing force. Note that the MK 4027 will dissipate considerably less power when the refresh operation is accomplished with a "$\overline{RAS}$-only" cycle as opposed to a normal $\overline{RAS}/\overline{CAS}$ memory cycle.

Page Mode Operation

The "Page Mode" feature of the MK 4027 allows for successive memory operations at multiple column locations of the same row address with increased speed without an increase in power. This is done by strobing the row address into the chip and keeping the $\overline{RAS}$ signal at a logic 0 throughout all successive memory cycles in which the row address is common.

This "page mode" of operation will not dissipate the power associated with the negative going edge of $\overline{RAS}$ Also, the time required for strobing in a new row address is eliminated, thereby decreasing the access and cycle times. The chip select input ($\overline{CS}$) is operative in page mode cycles just as in normal cycles. It is not necessary that the chip be selected during the first operation in a sequence of page cycles.

Likewise, the $\overline{CS}$ input can be used to select or disable any cycle(s) in a series of page cycles. This feature allows the page boundary to be extended beyond the 64 column locations in a single chip. The page boundary can be extended by applying $\overline{RAS}$ to multiple 4K memory blocks and decoding $\overline{CS}$ to select the proper block.

MK4116 FUNCTIONAL DESCRIPTION

Addressing

The 14 address bits required to decode 1 of the 16,384 cell locations within the MK 4116 are multiplexed onto the 7 address inputs and latched into the on-chip address latches by externally applying two negative going TTL-level clocks. The first clock, the Row Address Strobe ($\overline{RAS}$), latches the 7 row address bits into the chip. The second clock, the Column Address Strobe ($\overline{CAS}$), subsequently latches the 7 column address bits into the chip. Each of these signals, $\overline{RAS}$ and $\overline{CAS}$, triggers a sequence of events which are controlled by different delayed internal clocks. The two clock chains are linked together logically in such a way that the address multiplexing operation is done outside of the critical path timing sequence for read data access. The later events in the $\overline{CAS}$ clock sequence are inhibited until the occurence of a delayed signal derived from the $\overline{RAS}$ clock chain. This "gated $\overline{CAS}$" feature allows the $\overline{CAS}$ clock to be externally activated as soon as the Row Address Hold Time specification (tRAH) has been satisfied and the address inputs have been changed from Row address to Column address information.

Note that $\overline{CAS}$ can be activated at any time after tRAH and it will have no effect on the worst case data access time (tRAC) up to the point in time when the delayed row clock no longer inhibits the remaining sequence of column clocks. Two timing endpoints result from the internal gating of $\overline{CAS}$ which are called tRCD (min) and tRCD (max). No data storage or reading errors will result if $\overline{CAS}$ is applied to the MK 4116 at a point in time beyond the tRCD (max) limit. However, access time will then be determined exclusively by the access time from $\overline{CAS}$ (tCAC) rather than from $\overline{RAS}$ (tRAC), and access time from $\overline{RAS}$ will be lengthened by the amount that tRCD exceeds the tRCD (max) limit.

Data Input/Output

Data to be written into a selected cell is latched into an on-chip register by a combination of $\overline{\text{WRITE}}$ and $\overline{\text{CAS}}$ while $\overline{\text{RAS}}$ is active. The later of the signals ($\overline{\text{WRITE}}$ or $\overline{\text{CAS}}$) to make its negative transition is the strobe for the Data In (Din) register. This permits several options in the write cycle timing. In a write cycle, if the $\overline{\text{WRITE}}$ input is brought low (active) prior to $\overline{\text{CAS}}$, the Din is strobed by $\overline{\text{CAS}}$, and the set-up and hold times are referenced to $\overline{\text{CAS}}$. If the input data is not available at $\overline{\text{CAS}}$ time or if it is desired that the cycle be a read-write cycle, the $\overline{\text{WRITE}}$ signal will be delayed until after $\overline{\text{CAS}}$ has made its negative transition. In this "delayed write cycle" the data input set-up and hold times are referenced to the negative edge of $\overline{\text{WRITE}}$ rather than $\overline{\text{CAS}}$. (To illustrate this feature, Din is referenced to $\overline{\text{WRITE}}$ in the timing diagrams depicting the read-write and page-mode write cycles while the "early write" cycle diagram shows Din referenced to $\overline{\text{CAS}}$).

Data is retrieved from the memory in a read cycle by maintaining $\overline{\text{WRITE}}$ in the inactive or high state throughout the portion of the memory cycle in which $\overline{\text{CAS}}$ is active (low). Data read from the selected cell will be available at the output within the specified access time.

Data Output Control

The normal condition of the Data Output (Dout) of the MK 4116 is the high impedance (open-circuit) state. That is to say, anytime $\overline{\text{CAS}}$ is at a high level, the Dout pin will be floating. The only time the output will turn on and contain either a logic 0 or logic 1 is at access time during a read cycle. Dout will remain valid from access time until $\overline{\text{CAS}}$ is taken back to the inactive (high level) condition.

If the memory cycle in progress is a read, read-modify write, or a delayed write cycle, then the data output will go from the high impedance state to the active condition, and at access time will contain the data read from the selected cell. This output data is the same polarity (not inverted) as the input data. Once having gone active, the output will remain valid until $\overline{\text{CAS}}$ is taken to the precharge (logic 1) state, whether or not $\overline{\text{RAS}}$ goes into precharge.

If the cycle in progress is an "early-write" cycle ($\overline{\text{WRITE}}$ active before $\overline{\text{CAS}}$ goes active), then the output pin will maintain the high impedance state throughout the entire cycle. Note that with this type of output configuration, the user is given full control of the Dout pin simply by controlling the placement of $\overline{\text{WRITE}}$ command during a write cycle, and the pulse width of the Column Address Strobe during read operations. Note also that even though data is not latched at the output, data can remain valid from access time until the beginning of a subsequent cycle without paying any penalty in overall memory cycle time (stretching the cycle).

This type of output operation results in some very significant system implications.

Common I/O Operation — If all write operations are handled in the "early write" mode, then Din can be connected directly to Dout for a common I/O data bus.

Data Output Control— Dout will remain valid during a read cycle from tCAC until $\overline{\text{CAS}}$ goes back to a high level (precharge), allowing data to be valid from one cycle up until a new memory cycle begins with no penalty in cycle time. This also makes the $\overline{\text{RAS}}/\overline{\text{CAS}}$ clock timing relationship very flexible.

Two Methods of Chip Selection— Since Dout is not latched, $\overline{\text{CAS}}$ is not required to turn off the outputs of unselected memory devices in a matrix. This means that both $\overline{\text{CAS}}$ and/or $\overline{\text{RAS}}$ can be decoded for chip selection. If both $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ are decoded, then a two dimensional (X, Y) chip select array can be realized.

Extended Page Boundary— Page-mode operation allows for successive memory cycles at multiple column locations of the same row address. By decoding $\overline{\text{CAS}}$ as a page cycle select signal, the page boundary can be extended beyond the 128 column locations in a single chip. (See page-mode operation).

Output Interface Characteristics

The three state data output buffer presents the data output pin with a low impedance to V_{CC} for a logic 1 and a low impedance to V_{SS} for a logic 0. The effective resistance to V_{CC} (logic 1 state) is 420 Ω maximum and 135 Ω typically. The resistance to V_{SS} (logic 0 state) is 95 Ω maximum and 35 Ω typically. The separate V_{CC} pin allows the output buffer to be powered from the supply voltage of the logic to which the chip is interfaced. During battery standby operation, the V_{CC} pin may have power removed without affecting the MK 4116 refresh operation. This allows all system logic except the $\overline{\text{RAS}}$ timing circuitry and the refresh address logic to be turned off during battery standby to conserve power.

Page Mode Operation

The "Page Mode" feature of the MK 4116 allows for successive memory operations at multiple column locations of the same row address with increased speed without an increase in power. This is done by strobing the row address into the chip and maintaining the $\overline{\text{RAS}}$ signal at a logic 0 throughout all successive memory cycles in which the row address

is common. This "page-mode" of operation will not dissipate the power associated with the negative going edge of $\overline{RAS}$. Also, the time required for strobing in a new row address is eliminated, thereby decreasing the access and cycle times.

The page boundary of a single MK 4116 is limited to the 128 column locations determined by all combinations of the 7 column address bits. However, in system applications which utilize more than 16,384 data words, (more than one 16K memory block), the page boundary can be extended by using $\overline{CAS}$ rather than $\overline{RAS}$ as the chip select signal. $\overline{RAS}$ is applied to all devices to latch the row address into each device and then $\overline{CAS}$ is decoded and serves as a page cycle select signal. Only those devices which receive both $\overline{RAS}$ and $\overline{CAS}$ signals will execute a read or write cycle.

Refresh

Refresh of the dynamic cell matrix is accomplished by performing a memory cycle at each of the 128 row addresses within each 2 millisecond time interval. Although any normal memory cycle will perform the refresh operation, this function is most easily accomplished with "$\overline{RAS}$-only" cycles. $\overline{RAS}$-only refresh results in a substantial reduction in operating power. This reduction in power is reflected in the I_{DD3} specification called out in the MK4116 data sheet.

Power Considerations

Most of the circuitry used in the MK 4116 is dynamic and most of the power drawn is the result of an address strobe edge. Consequently, the dynamic power is primarily a function of operating frequency rather than active duty cycle. This current characteristic of the MK 4116 precludes inadvertent burn out of the device in the event that the clock inputs become shorted to ground due to system malfunction.

Although no particular power supply noise restriction exists other than the supply voltages remain within the specified tolerance limits, adequate decoupling should be provided to suppress high frequency noise resulting from the transient current of the device. This insures optimum system performance and reliability. Bulk capacitance requirements are minimal since the MK 4116 draws very little steady state (DC) current.

In system applications requiring lower power dissipation, the operating frequency (cycle rate) of the MK 4116 can be reduced and the (guaranteed maximum) average power dissipation of the device will be lowered in accordance with the I_{DD1} (max) spec limit curve illustrated in Figure 4. NOTE: The MK 4116 family is guaranteed to have a maximum I_{DD1} requirement of 35mA @ 375ns

cycle with an ambient temperature range from 0° to 70°C. A lower operating frequency, for example 1 microsecond cycle, results in a reduced maximum I_{DD1} requirement of under 20mA with an ambient temperature range from 0° to 70°C.
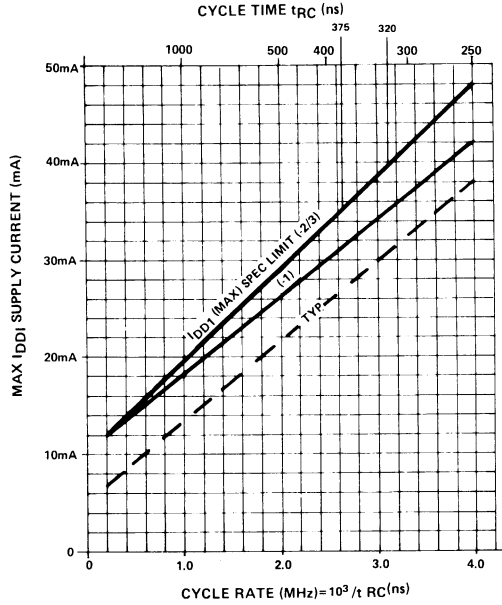
Fig. 4 Maximum I_{DD1} versus cycle rate for device operation at extended frequencies. I_{DD1} (max) curve is defined by the equation-

I_{DD1} (max) mA = 10 + 9.4 x cycle rate [MHz] for -2/3 only

I_{DD1} (max) mA = 10 + 8.0 x cycle rate [MHz] for -1 only

It is possible to operate certain versions of the MK 4116 family (the -2 and -3 speed selections for example) at frequencies higher than 2.66 MHz (375ns cycle), provided all AC operating parameters are met. Operation at shorter cycle times (< 375ns) results in higher power dissipation and, therefore, a reduction in ambient temperature is required.

Although $\overline{RAS}$ and/or $\overline{CAS}$ can be decoded and used as a chip select signal for the MK 4116, overall system power is minimized if the Row Address Strobe ($\overline{RAS}$) is used for this purpose. All unselected devices (those which do not receive a $\overline{RAS}$) will remain in a low power (standby) mode regardless of the state of $\overline{CAS}$.

TERMINAL CHARACTERISTICS OF THE MK4027 AND MK4116

Inputs

Addresses, Chip Select and Din — The address, Din and $\overline{CS}$ input circuitry for the MK4027 and MK4116 is shown in Fig. 5. This particular input circuit has some characteristics that make it particularly useful for the address and data inputs. First of all, it has a low input capacitance which is very important in

large arrays of memory chips where it is desirable to tie many address inputs together and to drive them with a single buffer. This circuit also allows the address hold time for row addresses to be very short. This makes the available 'window' for address multiplexing as wide as possible.

Clocks — The $\overline{RAS}$, $\overline{CAS}$, and $\overline{WRITE}$ inputs are basically MOS inverter stages. (Fig 6) The $\overline{RAS}$ input buffer is always active (the depletion load on the inverter is always supplying current to the inverter) because the device must always be able to respond to $\overline{RAS}$ transitions. The $\overline{RAS}$ input buffer accounts for the vast majority of the 1.5 ma of standby current on V_{DD}. The $\overline{CAS}$ and $\overline{WRITE}$ buffers differ from the $\overline{RAS}$ buffer in that the load device is clocked. When the memory is in standby ($\overline{RAS}$ high), the $\overline{CAS}$ and $\overline{WRITE}$ buffers load device is turned off. The input capacitance of the $\overline{RAS}$, $\overline{CAS}$, and $\overline{WRITE}$ buffers is fairly high (10pf) in comparison to the address inputs. This is because the input transistors are comparatively large since they have to have good current handling capability and also because of "Miller" effects during input transitions. In most cases this higher input capacitance is not a problem because the number of devices on each $\overline{RAS}$ or $\overline{CAS}$ buffer is small when compared to the number of devices on each address buffer.

$V_{RR} \approx 1.5V$
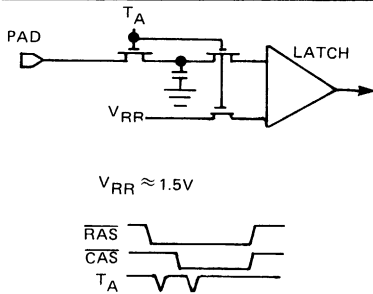
Figure 5 : ADDRESS AND DATA INPUTS
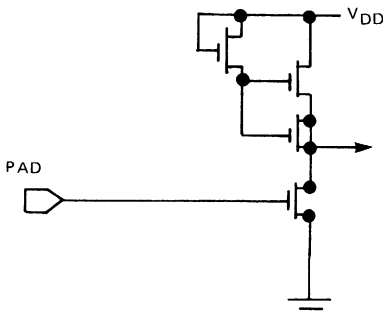
Figure 6: CLOCK INPUT CIRCUIT

MK4116 AND MK4027 COMPATIBLE DESIGNS

Because of their similarities it is very easy to design a memory system that will accommodate either the MK4027 or the MK4116. This is often a very desirable goal because it allows the memory system to be tailored to meet a wide range of overall system requirements. There are some differences however, between the MK4027 and MK4116 that require special consideration.

Refresh And Dout Interaction

In many systems that use transparent refresh, such as this *LSI-11 memory system, it is required that refresh take place immediately after a memory read or write cycle. If refresh takes place after a read cycle it may be required that the read data be held while refresh takes place. The only way to accomplish this in a compatible design is by adding data latches. The MK4027 will, in fact, work without latches if "$\overline{RAS}$ only" refresh is used. The MK4116, however, requires that $\overline{CAS}$ be held low to maintain the output data which means that no cycle may start while the data is being held.

Address Multiplexing

The differing address requirements for the MK4027 and MK4116 can be accommodated without jumpers. Fig. 7 shows a multiplexing scheme that uses the 'extra' multiplexer in a 74S158 to supply an inverted address to half the memory. When row addresses are selected two of the multiplexor outputs contain the same address data. The MK4027 will ignore this address data because it is applied to the $\overline{CS}$ input which is a 'don't care' at $\overline{RAS}$ time. The MK4116, however sees this input as another address and will strobe it in at $\overline{RAS}$ time. When column addresses are selected the extra multiplexor contains a complement address. The MK4027 uses this input as a $\overline{CS}$ input and the MK4116 uses it as another column address. Two high order addresses are used such that they are part of the $\overline{RAS}$ decode for the MK4027 but are not terms in the $\overline{RAS}$ decode for the MK4116. The net effect is that for the MK4027 half the chips will receive $\overline{CS}$ and only one selected row will receive $\overline{RAS}$. For the MK4116 the column data on half the rows will be reversed around A6.

Generating The Memory Timing

The timing generator for the *LSI-11 memory system has many responsibilities. It must provide the row address hold time (t_{RAH}), it must generate the multiplexing control signal, it must provide column address setup time, it must generate a column address strobe delay, it must generate a valid data or end of write signal, and must provide the necessary precharge interval (T_{RP}).

Any number of methods may be used to generate this timing such as an oscillator driving a counter or a shift register; or a series of one-shots. However, each of these methods has a number of problems. The oscillator is necessarily asynchronous to cycle initiation and the cycle startup problems are acute. The one-shot approach simply cannot be made accurate when short delays are required. The simplest and most reliable solution to generating the necessary timing edges is to use a delay line.

The timing and control logic is shown in Fig. 8 All cycle timing is derived from the delay line. The input to the delay line is a low going signal that propagates to the end of the line and resets the input such that the new memory cycle can be initiated whenever the output of the line returns high.

The delay line shown has a 200 ns total delay with 5 taps at 40 ns intervals. This line was chosen because it was a standard 'off the shelf' item and was adequate for prototyping. The delay line timing and resulting system timing for read and write cycles is shown in figs. 9 and 10.

The synchronous refresh timing is similar to the read cycle timing but the asynchronous refresh (fig. 11) cycle has some interesting features. When the refresh interval timer indicates that a refresh should occur all further external cycles are inhibited from starting. After a 50ns delay if no cycle is in progress the address multiplexor can be switched to select the refresh addresses from the refresh address counter. After an additional 50ns delay to allow refresh addresses to stabilize, the cycle is started and proceeds much like any other cycle except no RPLY is generated and CAS is inhibited.

FIG. 7 MEMORY ADDRESS DECODING LOGIC
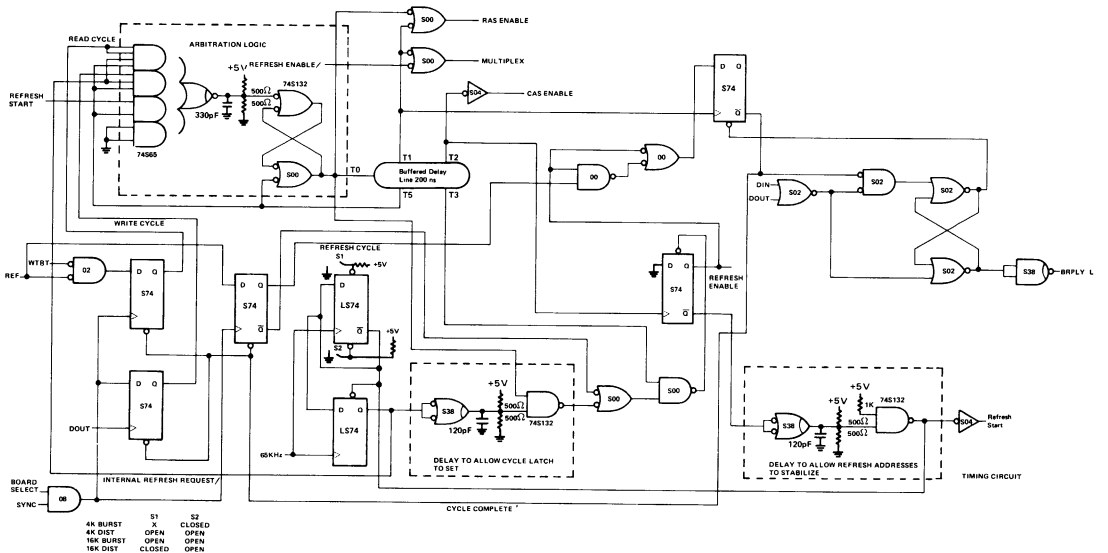
FIG. 8 MEMORY TIMING AND CONTROL LOGIC
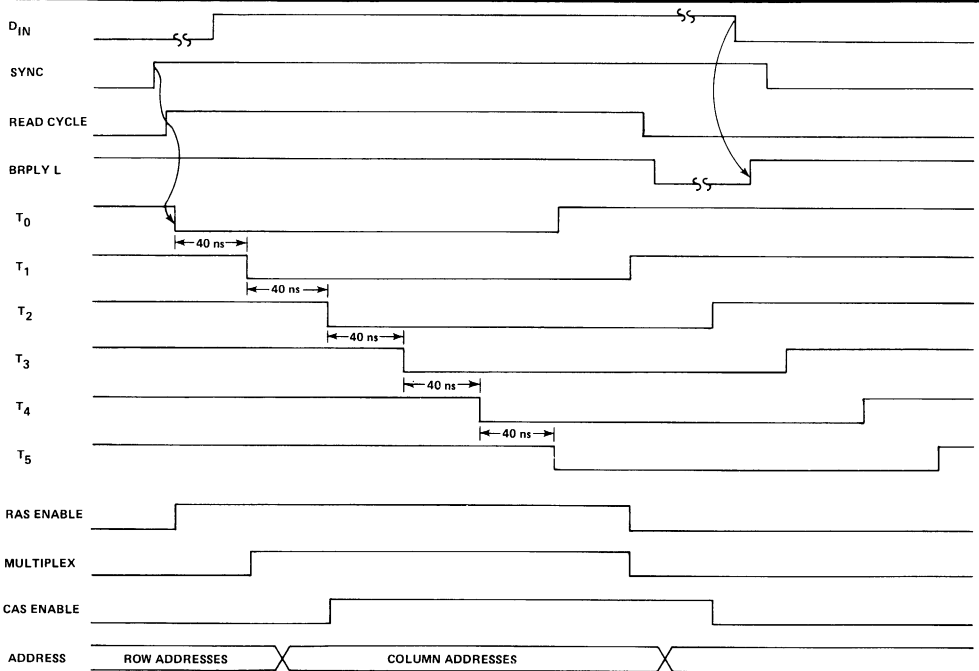
FIG. 9 READ CYCLE TIMING
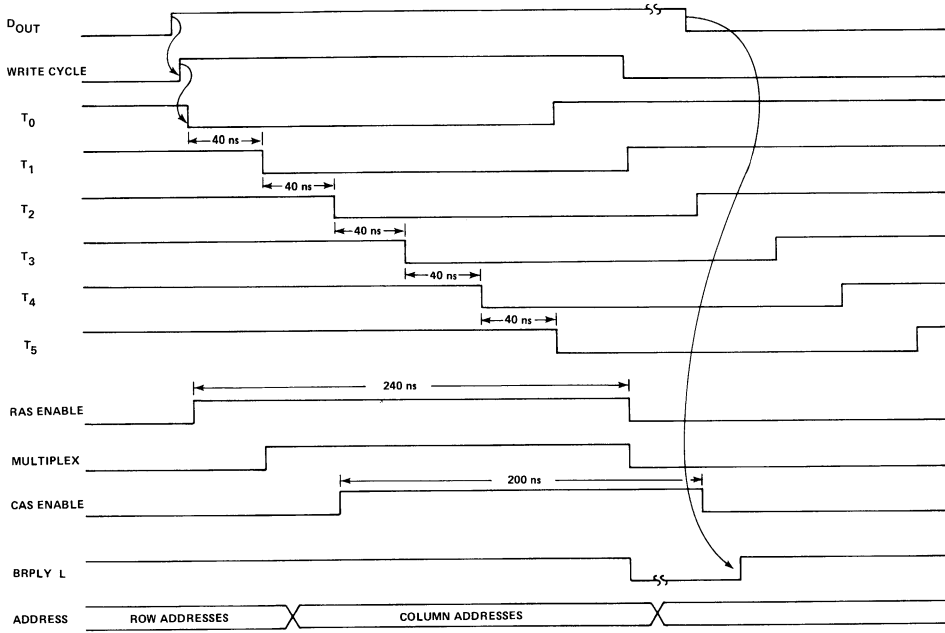
FIG. 10 WRITE CYCLE TIMING
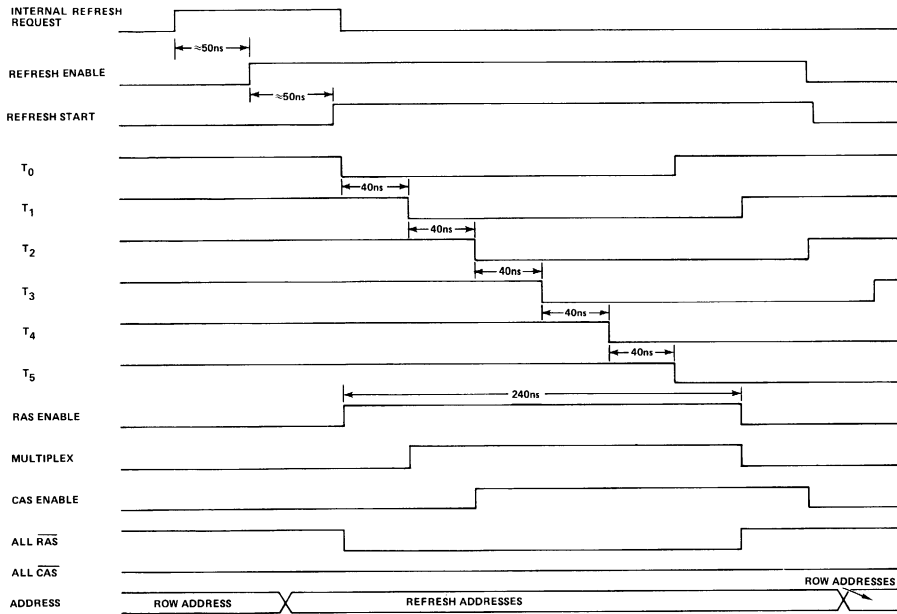
FIG. 11 INTERNAL REFRESH CYCLE TIMING

Refresh Techniques

In most memory systems it is difficult to guarantee that the normal order of events will cause all the rows within a memory to be accessed within the specified refresh interval. For this reason, most dynamic memory systems have special circuitry that will cause extra memory cycles in an ordered manner such that all rows of memory devices are accessed within the 2 ms interval.

There are three commonly used techniques for introducing these extra memory refresh cycles. The first is in a "burst" where all normal memory accesses are inhibited for a fixed period of time while all rows are accessed. The second is "cycle stealing" where single memory cycles are periodically stolen from the CPU in order to refresh a single row. The third and most common is "transparent" where refresh cycles are periodically generated for refresh but they are introduced at a time when the memory is not being accessed and thus they are transparent to the CPU (i.e. the CPU is not affected by refresh).

The *LSI-11 microcode has provisions for performing "burst" refresh and the memory system described here will respond to the "burst" refresh from the LSI-11.* In addition, this memory system also has provisions for "transparent" refresh so that the "burst" refresh on the LSI-11* can be disabled for enhanced real-time system response.

The LSI-11* generates 64 cycles for refresh of 4K dynamic RAMs. The MK4116 requires 128 cycles for refresh. Instead of trying to do two refresh cycles for each synchronous refresh request, the distributed refresh is allowed to run even in the burst mode when the board is populated with MK4116's. Thus, 64 refresh cycles are provided by the LSI-11* and 64 cycles are generated by the on-board refresh running at half speed. In order to eliminate addressing problems the on-board refresh counter is used for all refresh cycles.

Synchronous and Asynchronous Refresh

One of the most important factors in a dynamic memory design is deciding whether the memory refresh will be synchronous or asynchronous. For synchronous refresh, the designer can use some system event (clock) to trigger refresh. In the asynchronous system the designer must provide for a local event to trigger the refresh. With an asynchronous refresh there will usually be cases when a system memory request and local refresh request occur simultaneously. To provide for such circumstances, some arbitration scheme must be present on the asynchronously refreshed memory. Extreme care must be taken in the design of the arbitration logic because if it does not contain adequate safeguards the memory system can (and will) malfunction causing some rather interesting and impossible to duplicate errors. Because of the inherent difficulties of asynchronous refresh it should be used only as a last resort. This is probably why DEC included the refresh microcode in the LSI-11* to allow refresh to be system synchronous.

The arbitration logic for this memory system is shown in Fig. 8. For normal read or write cycles, without refresh interference, the and-or-invert (AOI) sets the cycle start latch which feeds the delay line generating the memory timing signals. When an asynchronous refresh must take place the INTERNAL REFRESH REQUEST signal inhibits any bus requested cycles (read, or write) from setting the cycle start latch. After a short delay the output of the cycle start latched is sampled and if no cycle is in progress the address multiplexer is switched to select the refresh addresses and the refresh cycle is allowed to start. In the event of the refresh request overriding the read/write requests, the output of the AOI might not allow the cycle start latch to set properly and a timing glitch could propagate through the delay line. To prevent such a catastrophic event, the output of the open collector AOI gate has an RC delay that serves to stretch any low going pulse making it wide enough to insure proper setting of the latch.

The refresh enable has an alternate path that bypasses the arbitration delay. This is used for synchronous refresh cycles that are generated by the LSI-11.* The arbitration can be bypassed because it is possible to merge the synchronous refresh requests and not cause a conflict with a normal cycle.

DRIVING MOS WITH TTL

Driver Characteristics

For the Schottky devices the important parameters are the output impedance in the high and low level output state and the rise and fall time of the signal. The worst case high level output impedance can be calculated by using the I_{OS} values for the device and observing that the voltage across the current limiting resistor in the Schottky output stage is given by:

$$V = V_{CC} - 2V_{BE} + V_D$$

The larger the voltage across the resistor the higher its resistance, so by assuming a small value for V_{BE} (0.65V) and a large value for the drop across the Schottky diode in the driver (0.6V), a safe worst case number can be calculated.

For the low level output impedance the low level output current (I_{OL}) and low level output voltage (V_{OL}) can be used. Assuming a small value for the low level open circuit output voltage (V_{OLO}) of about 0.2 volts the output impedance can be estimated by:

$$R_{OL} = \frac{V_{OL} - V_{OLO}}{I_{OL}}$$

Calculations for the 74S04 give a worst case output impedance of about 114Ω in the high level state and about 15Ω in the low level state. The 74S04 has a worst case high level output impedance of about 89Ω and a worst case low level impedance of about 5Ω. The values for the 74S04 can be used for most Schottky TTL functions because the output structures are similar.

Line Termination

It is not obvious that line termination is necessary, but it is. If no termination is used, a low going signal will be injected into the line having an amplitude that can be calculated by dividing the signal swing between the source impedance and the characteristic impedance of the line. For a 3 volt negative signal swing from a 75S37 into a 50Ω line the transmitted signal will have an amplitude of 2.7 volts. This signal will propagate to the end of the line, be 100% reflected at the end of the line and return to the driver. At the driver the signal will reflect about 80% and 180° out of phase. In the case where the fall time of the signal is shorter than the two way propagation delay of the line the resulting reflection from the driver will cause the signal to swing positive at the end of the line to about 2.0 volts. This amount of ringing obviously cannot be tolerated so some types of termination must be used.

Termination of the line at the 'receiving' end is one method that is often used in TTL transmission line systems.. This type of termination has several drawbacks. If a simple pullup resistor to +5 volts is used, the low level DC current through a resistor with a resistance equal to the impedance of the line will in most cases consume almost all of the drive capability of the bus driver. Even if the line impedance is as high as 200Ω the logic '0' level current through a 200 Ω resistor would be 25 mA.

When considering termination of lines in a memory array it becomes very impractical to use receiving end termination. If terminating pairs were used the driver would have to be capable of sinking about 30 mA for each terminated line because of the low impedance of signal lines in a memory array.

The best choice for line termination is to use a series resistor at the driver. This approach is not practical when driving TTL loads because the I_{IL} current causes a loss of logic '0' level. MOS loads however, have such small current requirements that this is not a problem. A series resistor of 100Ω with 100 MOS loads would produce only 0.1 volt of signal level loss. Series damping has an additional advantage over parallel termination in that it draws no DC supply current. For proper termination of the line it is necessary to match the low level source impedance of the driver to the impedance of the line being driven. This reduces ringing in the low level where the margins are most critical. In cases where multiple lines are being driven by the driver, the parallel combination of the lines should be used for the line impedance and the series resistor chosen accordingly. In practice, the resistor value is best chosen empirically. The board should be designed to accommodate the resistors and then different values tried on a prototype. The waveform with the ideal resistor will be slightly underdamped.

DELAY TIME CALCULATIONS

The switching delays for TTL devices driving capacitive loads such as memory signal lines can best be estimated by using the equation for the charge time of an RC circuit. R will be the maximum output impedance of the gate plus the series damping resistance, and C is the sum of the capacitances of the inputs being driven plus the capacitance of the board. When calculating the capacitance of the line the data sheet typical values for capacitance should be used rather than the maximums. This is because high input capacitance is not a function of the wafer lot, and the probability of having mostly worst case capacitance on the same signal line is very very small.

The equation for the maximum rise time is:

$$t_r = -RC \, ln \, \frac{3.85V - V_{IH}}{3.85V - 0.2V} = -RC \, ln \, \frac{3.85V - V_{IH}}{3.65V}$$

V_{IH} = 2.2 volts for addresses on 4027

V_{IH} = 2.4 volts for addresses on 4116 and clocks on 4027

V_{IH} = 2.7 volts for clocks on 4116

The fall time is:

$$t_f = -RC \, ln \frac{.8}{3.95} = 1.6RC$$

SIGNAL	V_{IH}	DRIVER	SERIES RESISTOR	LOADS/ LINE	LOAD CAPACITANCE	t_{pLH}	t_{pHL}
4027 CLOCKS	2.4	74S37	22 Ω	16	148pF	15ns	6.5ns
4116 CLOCKS	2.7	74S37	22 Ω	16	148pF	19ns	6.5ns
4027 ADDRESSES	2.2	74S37	22 Ω	32	169pF	18ns	10ns
4116 ADDRESSES	2.4	74S04	22 Ω	32	168pF	21ns	10ns

Table 1 Calculated Propagation Delays for Memory Signal Buffers

Power Distribution and Decoupling

The layout for dynamic memories is of special importance. Layout techniques that have been used successfully in the past for older generation MOS memories are simply inadequate for current state-of-the-art memories such as the MK4027 and MK4116. The newer devices have shallow diffusions that make possible fast memory devices but the shallow diffusions and fast switching speeds create larger current transients with higher frequency components than did the older designs.(Fig. 12) In order to tame these current transients and prevent them from generating voltage spikes that can cause loss of data and 'soft' errors every effort must be made to minimize the impedance in the decoupling path for the device.

The decoupling path is the trace distance from a power pin through a decoupling capacitor and to package ground. The impedance of this path is determined by the line inductance and the series impedance of the decoupling capacitor. Because the current transients on the MK4027 and MK4116 have significant harmonic content up to 100MHz the line inductance is one of the most critical factors. The line inductance can be minimized either by providing a power plane or by griding the power. In order to increase the effectiveness of the grided power, decoupling capacitors should be placed judiciously. A capacitor placement that has shown to be very effective is shown in Fig. 13. V_{DD} and V_{BB} are decoupled at every other chip with $0.1\mu F$ capacitors such that the decoupling creates a 'checkerboard' pattern. This particular pattern was used on the LSI-11* memory board and measurements of the V_{DD} noise with a differential probe showed that the noise was below 400 mV peak-to-peak.

FIG. 12 CURRENT WAVEFORMS FOR MK4116

X = 0.1 μ F from V_{DD} to V_{SS}
O = 0.1μ F from V_{BB} to V_{SS}
□ = 0.1 μ F from V_{CC} to V_{SS}
X = 2→5 μ F from V_{DD} to V_{SS}
● = 1 μ F from V_{BB} to V_{SS}

Placement of Decoupling Capacitors in 4 x 8 Memory Matrix
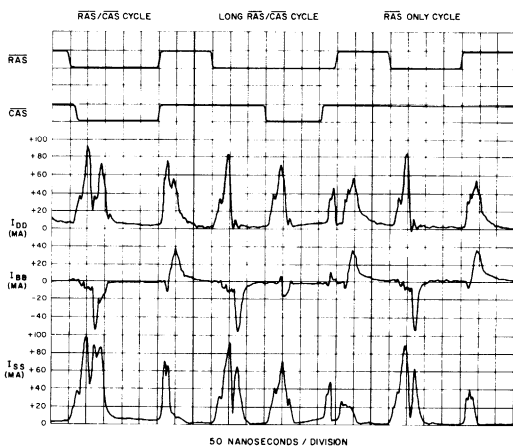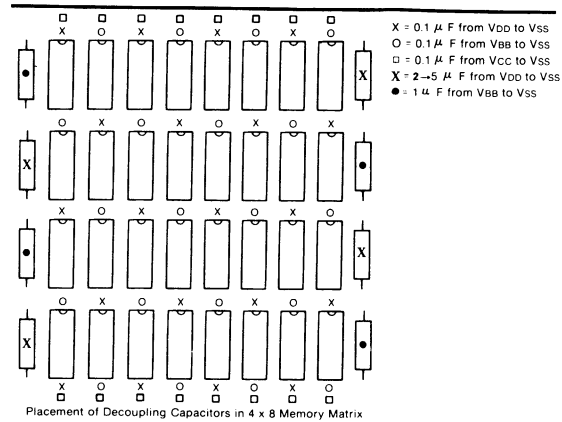
FIG. 13

While the 0.1 μ F decoupling capacitors are more than adequate for suppression of transients some larger bulk capacitors should be used to provide enough energy storage to prevent supply droop. The long term (cycle time) current requirements of the MK4027 and MK4116 are fairly low at 35 mA max. Assuming 64 memory devices all cycling at the maximum rate of 375 ns with 120 ns of precharge only 8.4 μ F of capacitance is required to keep the voltage drop below .1 volts. As with the high frequency decoupling it is good practice to distribute the bulk capacitance around the storage matrix to minimize the effects of the inductive and resistive voltage drops.

Decoupling of the V_{CC} (+5) supply is fairly non-critical. In most cases only one row of memory devices is accessed at a time. The V_{CC} supply, therefore only needs to provide enough current to charge one Dout line for each column of memories. The V_{CC} decoupling capacitors (0.1μ F) were placed at the top and bottom of each column of memories. The V_{CC} voltage at each device was measured when a data '1' was being read. The drop in V_{CC} was less than 300 mV. Calculations of the resultant rise time indicate that a 300 mV decrease in V_{CC} would cause less than a 10% increase in output rise time at V_{CC}=4.75 volts.

Bulk decoupling of the V_{CC} supply is usually not required in the memory. The DC current loading of the V_{CC} supply is dependent on the TTL loading and is usually quite small (less than 1mA for each 8 bits in the output word). The bulk decoupling, therefore, can be provided by the bulk capacitance used for the TTL.

The other performance advantages of griding the power are the crosstalk between signal lines is decreased because of the close proximity of ground; and ground voltage differentials between the TTL drivers and the memory devices is reduced enhancing the noise immunity to switching transients from the TTL devices.

Most of the layout techniques used in the memory array should be extended to the TTL circuitry on all boards. Ground should be grided wherever possible. The decoupling paths should be kept as short as possible. Board ground should connect to backplane ground at as many points as possible.
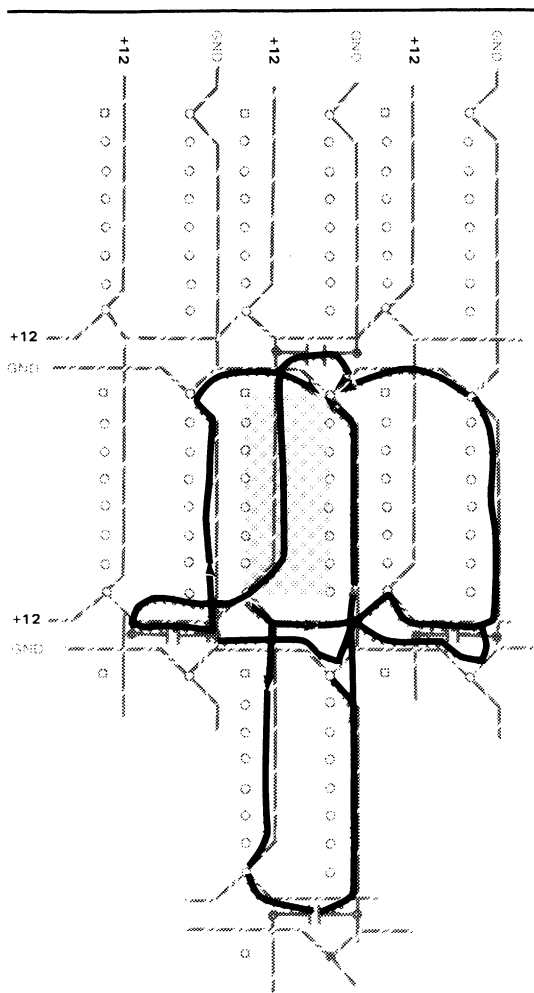
FIG. 14

Decoupling Currents With Grided Power And

Checkerboard Decoupling

Signal Lines

Routing of the signal lines within the memory matrix is fairly straight forward. Address and clock lines can be daisy chained along each row and cause no cross-

talk problems when a good ground mesh is employed. In cases where multiple rows of chips are driven by the same TTL buffer the lines should be vertically bused outside the memory and tapped for each horizontal row of chips. The lines should in no case be snaked through the memory. Snaked lines are more susceptible to externally induced noise and crosstalk because of the longer path to the signal source.

Naturally, all lines should be kept as short as possible. This implies that the signal drivers and receivers should be physically close to the memory array. In cases where there are a large number of memory chips in each row the address drivers should be placed in the center of the array. (Fig. 16) If the $\overline{RAS}$ and $\overline{CAS}$ buffers drive one row of memory chips each can be placed either in the center of the array or on the side of the array. If the drivers will not fit in the middle of the matrix, they may be placed below the matrix. The signal lines would then be routed vertically and 'T'd' for each horizontal connection. In such cases, it is recommended that each stub be the same length in order to minimize the distortion of the signal edges caused by mismatched stubs.

MISCELLANEOUS POWER CONSIDERATIONS

Power Sequencing

The data sheets for the MK4027 and MK4116 state that no special power sequencing is required for proper device operation. This does not mean that the power sequencing should be ignored. In many systems the power supply lines exhibit overshoot on power up. This can cause V_{DD} at the memory to exceed data sheet limits for a short period of time. If V_{BB} is not applied when V_{DD} overshoots, breakdown can occur and destroy the memory. If a system does have this overshoot, sequencing the supplies so that V_{BB} is applied first will provide extra margin and help prevent device destruction.

The data sheet specified that V_{BB} should not be allowed to go positive with respect to ANY other input. If it does, injection currents can occur and cause loss of functionality. Special precautions should be taken in the V_{BB} power distribution to prevent this occurance. A high current Schottky diode from V_{BB} to ground can protect against many of the hazards such as an open V_{BB} supply or a momentary short to a signal or power line. Note that the layout in Fig. 15 has the V_{BB} run next to ground in the memory array. This will help reduce the chance of memory damage should a screwdriver or scope probe get loose in the system.

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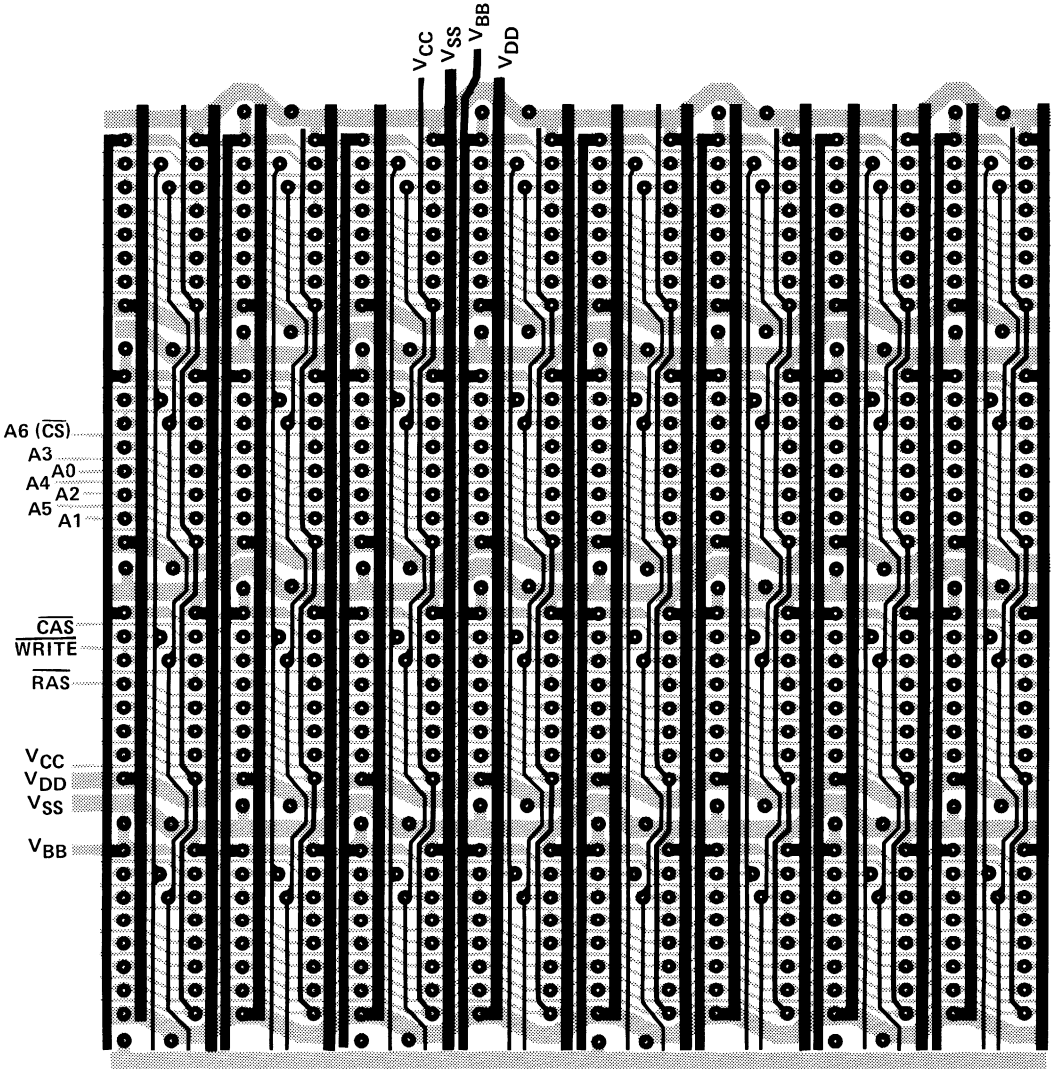
FIG. 15   SUGGESTED P.C. LAYOUT FOR MK4027 OR MK4116
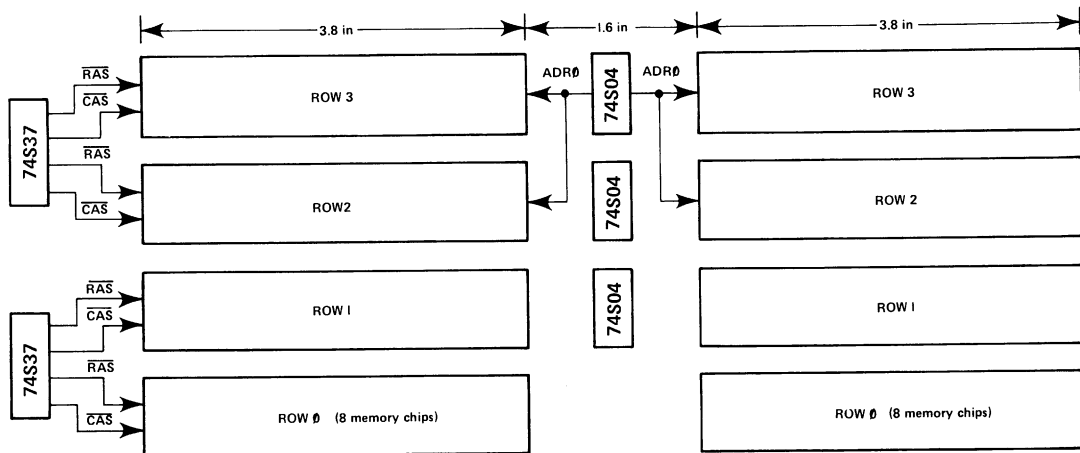
FIG. 16 TYPICAL PLACEMENT FOR DRIVERS WITHIN MEMORY MATRIX

Power Calculations

Calculation of the V_{DD} supply current involves a fairly simple averaging procedure. The active refresh and standby currents are averaged over any given time period and multiplied times the maximum supply voltage to give the maximum power dissipation. The equation for the maximum average I_{DD} is given by:

$$I_{DD_{AVE}} = [n_{ACC} \times c_{ACC} [10mA (t_{RAS} + 120ns) +$$

$$9.4mA \times 10^{-6} s] + n_{REF} \times c_{REF} [10mA (t_{RRAS} +$$

$$120ns) + 6.5mA \times 10^{-6}s] + I_{DD2} [n_{TOTAL} \times 1s - n_{ACC} \times$$

$$c_{ACC}(t_{RAS} + 120ns) - n_{REF} \times c_{REF} (t_{RRAS} + 120ns)] / 1s$$

n_{ACC} = Number of devices accessed per normal cycle

n_{REF} = Number of devices refreshed per $\overline{RAS}$ only refresh cycle

n_{TOTAL} = Total number of devices in system

c_{ACC} = Frequency of normal accesses

c_{REF} = Frequency of refresh cycles

t_{RAS} = $\overline{RAS}$ active time for normal cycles

t_{RRAS} = $\overline{RAS}$ active time for refresh cycles

This equation takes into account the variations in current vs operating frequency and current vs duty cycle and provides for differences in number of devices in standby and number of devices active. As an example, assume a board with 8 rows of 8 chips per row. Refresh will occur every 7μs but only half the devices will be refreshed every refresh cycle. The other parameters are:

n_{ACC} = 8

n_{REF} = 32

n_{TOTAL} = 64

c_{ACC} = 2MHz

c_{REF} = 1/7μs ~ 143KHz

t_{RAS} = 240ns

t_{RRAS} = 200ns

I_{DD2} = 1.5ma (MK4116)

$$I_{DD_{AVE}} = 8 \times 2 \times 10^6 [1 \times 10^{-2}A (240 \times 10^{-9}s)$$

$$+ 9.4 \times 10^{-3}A \times 1 \times 10^{-6}s] + 32 \times 143 \times 10^3$$

$$[1 \times 10^{-2}A (200 \times 10^{-9}s + 120 \times 10^{-9}s) + 6.5$$

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$x \ 10^{-3} \ x \ 1 \ x \ 10^{-6}s] + 1.5 \ x \ 10^{-3} \ [64 \ x \ ls \ -8$

$x \ 2 \ x \ 10^6 \ (240 \ x \ 10^{-9}s + 120 \ x \ 10^{-9}s) \cdot 32 \ x \ 143$

$x \ 10^3 \ (200 \ x \ 10^{-9}s + 120 \ x \ 10(-9s)]$

$I_{DD_{AVE}} = 337.6ma$

Power calculations for the LSI-11 board using distributed refresh and with MK4027 gives:

$n_{ACC} = 16$

$n_{REF} = 16, 32, 48, 64$

$n_{TOTAL} = 16, 32, 48, 64$

$c_{ACC} = 1 \ MHz$ (bus limit)

$c_{REF} = 32.5 \ Khz$

$t_{RAS} = 240ns$

$t_{RRAS} = 240ns$

$I_{DD2} = 2.0ma$

Yielding a maximum I_{DD} current of 233 mA for 4K words, 270 mA for 8K, 307 mA for 12K and 344mA for 16K.

Using the MK4116 we have:

$n_{ACC} = 16$

$n_{REF} = 16, 32$

$n_{TOTAL} = 16, 32$

$c_{ACC} = 1MHz$

$c_{REF} = 65KHz$

$t_{RAS} = 240ns$

$t_{RRAS} = 240 \ ns$

$I_{DD2} = 1.5ma$

This gives a maximum average I_{DD} current of 233 mA for 16K and 267 mA for 32K.

It is interesting to note that on a per chip basis the MK4116 actually consumes less power than the MK4027 even though the MK4116 is refreshed at twice the rate.

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Z80 INTERFACING TECHNIQUES FOR DYNAMIC RAM
Application Note

By JERRY WINFIELD

INTRODUCTION

Since the introduction of second generation micro-processors, there has been a steady increase in the need for larger RAM memory for microcomputer systems. This need for larger RAM memory is due in part to the availability of higher level languages such as PL/M, PL/Z, FORTRAN, BASIC and COBOL. Until now, when faced with the need to add memory to a microcomputer system, most designers have chosen static memories such as the 2102 1Kx1 or possibly one of the new 4Kx1 static memories. However, as most mini or mainframe memory designers have learned, 16-pin dynamic memories are often the best overall choice for reliability, low power, performance, and board density. This same philosophy is true for a microcomputer system. Why then have microcomputer designers been reluctant to use dynamic memory in their system? The most important reason is that second generation micro-processors such as the 8080 and 6800 do not provide the necessary signals to easily interface dynamic memories into a microcomputer system.

Today, with the introduction of the Z80, a true third generation microprocessor, not only can a micro-computer designer increase system throughput by the use of more powerful instructions, but he can also easily interface either static or dynamic memories into the microcomputer system. This application note provides specific examples of how to inter-face 16-pin dynamic memories to the Z80.

OPERATION OF 16-PIN DYNAMIC MEMORIES

The 16-pin dynamic memory concept, pioneered by MOSTEK, uses a unique address multiplexing technique which allows memories as large as 16,384 bits x 1 to be packaged in a 16-pin package. For example the MK4027 (4,096x1 dynamic MOS RAM) and the MK4116 (16,384x1 dynamic MOS RAM) both use address multiplexing to load the address bits into memory. The MK4027 needs 12 address bits to select 1 out of 4,096 locations, while the MK4116 requires 14 bits to select 1 out of 16,384. The internal memories of the MK4027 and MK4116 can be thought of as a matrix. The MK4027 matrix can be thought of as 64x64, and the MK4116 as 128x128. To select a particular location, a row and column address is supplied to the memory. For the MK4027, address bits A_0-A_5 are the row address, and bits A_6-A_{11}

are the column addresses. For the MK4116, address bits A_0-A_6 are the row address, and A_7-A_{13} are the column address. The row and column addresses are strobed into the memory by two negative going clocks called Row Address Strobe ($\overline{RAS}$) and Column Address Strobe ($\overline{CAS}$). By the use of $\overline{RAS}$ and $\overline{CAS}$, the address bits are latched into the memory for access to the desired memory location.

Dynamic memories store their data in the form of a charge on a small capacitor. In order for the dynamic memory to retain valid data, this charge must be periodically restored. The process by which data is restored in a dynamic memory is known as refreshing. A refresh cycle is performed on a row of data each time a read or write cycle is performed on any bit within the given row. A row consists of 64 locations for the MK4027 and 128 locations for the MK4116. The refresh period for the MK4027 and the MK4116 is 2ms which means that the memory will retain a row of data for 2ms without a refresh. Therefore, to refresh all rows within 2ms, a refresh cycle must be executed every $32\mu s$ (2ms÷64) for the MK4027 and $16\mu s$ (2ms÷128) for the MK4116.

To ensure that every row within a given memory is refreshed within the specified time, a refresh row address counter must be implemented either in external hardware or as an internal CPU function as in the Z80. (Discussed in more detail under Z80 Refresh Control and Timing.) The refresh row address counter should be incremented each time that a refresh cycle is executed. When a refresh is performed, all RAMs in the system should be loaded with the refresh row address. For the MK4027 and the MK4116, a refresh cycle consists of loading the refresh row address on the address lines and then generating a $\overline{RAS}$ for all RAMs in the system. This is known as a $\overline{RAS}$ only refresh. The row that was addressed will be refreshed in each memory. The $\overline{RAS}$ only refresh prevents a conflict between the outputs of all the RAMs by disabling the output on the MK4116, and maintaining the output state from the previous memory cycle on the MK4027.

Z80 TIMING AND MEMORY CONTROL SIGNALS

The Z80 was designed to make the job of interfacing

to dynamic memories easier. One of the reasons the Z80 makes dynamic memory interfacing easier is because of the number of memory control signals that are available to the designer. The Z80 control signals associated with memory operations are:

MEMORY REQUEST ($\overline{MREQ}$) - Memory request signal indicating that the address bus holds a valid memory address for a memory read, memory write, or memory refresh cycle.

READ ($\overline{RD}$) - Read signal indicating that the CPU wants to read data from memory or an I/O device. The addressed I/O device or memory should use this signal to gate data onto the CPU data bus.

WRITE ($\overline{WR}$) - Write signal indicating that the CPU data bus hold valid data to be stored in the addressed memory or I/O device.

REFRESH ($\overline{RFSH}$) - Refresh signal indicates that the lower 7 bits of the address bus contain a refresh address for dynamic memories and the current MREQ signal should be used to generate a refresh cycle for all dynamic memories in the system.

Figures 1a, 1b, and 1c show the timing relationships of the control signals, address bus, data bus and system clock Φ. By using these timing diagrams, a set of equations can be derived to show the worst case access times needed for dynamic memories with the Z80 operating at 2.5MHz.

The access time needed for the op code fetch cycle and the memory read cycle can be computed by equations 1 and 2.

(1) $t_{ACCESS\ OP\ CODE} = 3(t_c/2) - t_{DL\overline{\Phi}(MR)} - t_{S\Phi(D)}$

where: t_c = Clock period

$t_{DL\overline{\Phi}(MR)}$ = $\overline{MREQ}$ delay from falling edge of clock.

$t_{s\Phi(D)}$ = Data setup time to rising edge of clock during op code fetch cycle.

let: t_C = 400ns; $t_{DL\overline{\Phi}(MR)}$ = 100ns; $t_{s\Phi}$ = 50ns

then: $t_{ACCESS\ OP\ CODE}$ = 450ns

(2) $t_{ACCESS\ MEMORY\ READ} = 4(t_c/2) - t_{DL\overline{\Phi}(MR)} - t_{S\overline{\Phi}(D)}$

where: t_C = Clock period

$t_{DL\overline{\Phi}(MR)}$ = MREQ delay from falling edge of clock

$t_{S\overline{\Phi}(D)}$ = Data Setup time to falling edge of clock

let: t_C = 400ns; $t_{DL\ (MR)}$ = 100ns; $t_{S\ (D)\ \overline{\Phi}}$ = 60ns

then: $t_{ACCESS\ MEMORY\ READ}$ = 640ns

The access times computed in equations 1 and 2 are overall worst case access times required by the CPU. The overall access times must include all TTL buffer delays and the access time for the memory device. For example, a typical dynamic memory design would have the following characteristics, (see Figure 2).

The example in Figure 2 shows an overall access time of 336ns. This would more than satisfy the 450ns required for the op code fetch and the 640ns required for a memory read.

CPU $\overline{MREQ}$ buffer delay 12ns (8T97)
Memory gating and timing delays 40ns
Memory device access time 250ns (MK4027/4116-4)
Memory data bus buffer delay 17ns (8T28)
CPU data bus buffer delay. 17ns (8T28)

336ns

OP CODE FETCH TIMING
Figure 1a.

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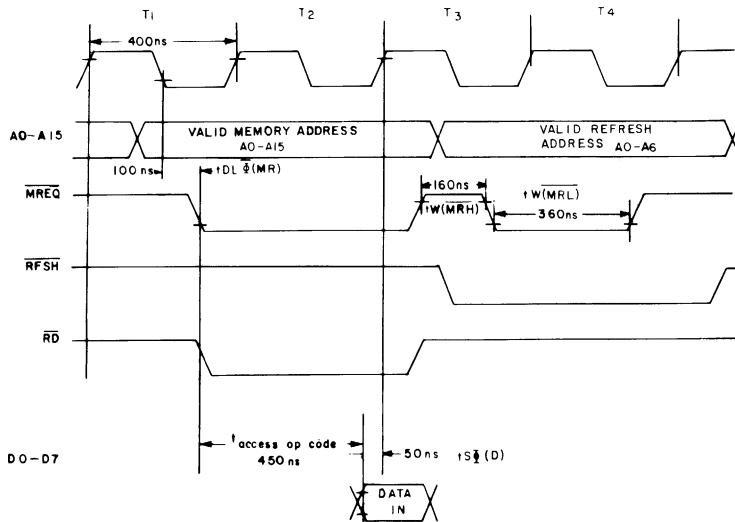
MEMORY READ TIMING
Figure 1b.
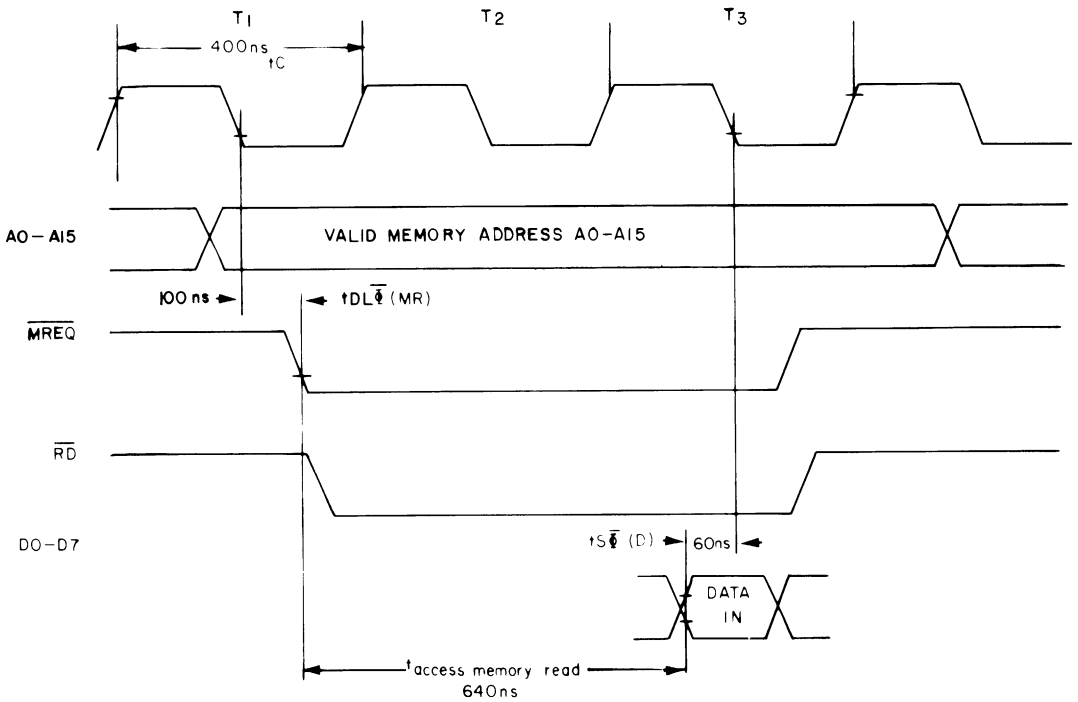
MEMORY WRITE TIMING
Figure 1c.
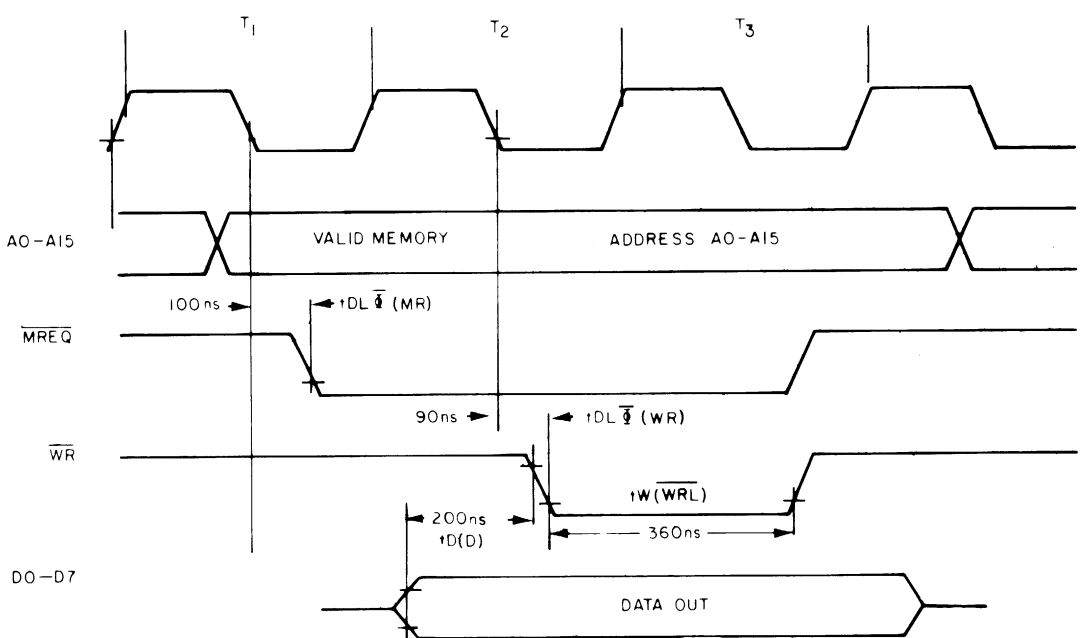
Z80 REFRESH CONTROL AND TIMING

One of the most important features provided by the Z80 for interfacing to dynamic memories is the execution of a refresh cycle every time an op code fetch cycle is performed. By placing the refresh cycle in the op code fetch, the Z80 does not have to allocate time in the form of "wait states" or by "stretching" the clock to perform the refresh cycle. In other words, the refresh cycle is "totally transparent" to the CPU and does not decrease the system throughput (see Figure 1a). The refresh cycle is "transparent" to the CPU because, once the op code has been fetched from memory during states T_1 and T_2, the memory would normally be idle during states T_3 and T_4.

Therefore, by placing the refresh in the T_3 and T_4 states of the op code fetch, no time is lost for refreshing dynamic memory. The critical timing parameters involving the Z80 and dynamic memories during the refresh cycle are: $t_{W(MRH)}$ and $t_{W(MRL)}$. The parameter known as $t_{W(MRH)}$ refers to the time that $\overline{MREQ}$ is high during the op code fetch between the fetch of the op code and the refresh cycle. This time is known as "precharge" for dynamic memories and is necessary to allow certain internal nodes of the RAM to be charged-up for another memory cycle. The equation for the minimum $t_{W(MRH)}$ time period is:

(3) $t_{W(MRH)} = t_{W(\Phi H)} + t_f - 30$
where: $t_{W(\Phi H)}$ is clock pulse width high
           t_f is clock fall time
let: $t_{W(\Phi H)} = 180ns$; $t_f = 10ns$
then: $t_{W(MRH)} = 160ns$ (min)

A $t_{W(MRH)}$ of 160ns is more than adequate to meet the worst case precharge times for most dynamic RAMs. For example, the MK4027-4 and the MK4116-4 require a 120ns precharge. The other refresh cycle parameter of importance to dynamic RAMs is $t_{W(MRL)}$, (the time that $\overline{MREQ}$ is low during the refresh cycle). This time is important because $\overline{MREQ}$ is used to directly generate $\overline{RAS}$. The equation for the minimum time period is:

(4) $t_{W(MRL)} = t_c - 40$
where: t_c is the clock period
let: $t_c = 400ns$
then: $t_{W(MRL)} = 360ns$

A 360ns $t_{W(MRL)}$ exceeds the 250ns min $\overline{RAS}$ time required for the MK4027-4 and the MK4116-4.

By controlling the refresh internally with the Z80, the designer must be aware of one limitation. The limitation is that to refresh memory properly, the Z80 CPU must be able to execute op codes since the refresh cycle occurs during the op code fetch. The following conditions cause the execution of op codes to be inhibited, and will destroy the contents of dynamic memory.

(1) Prolonged reset > 1ms
(2) Prolonged wait state operation > 1ms
(3) Prolonged bus acknowledge (DMA) > 1ms
(4) Φ clock of < 1.216 MHz for 16K RAMs
               < .608 MHz for 4K RAMs

The clocks rate in number 4 are based on the Z80 continually executing the worst case instruction which is an EX (SP), HL that executes in 19 T states. Therefore, by operating the Z80 at or above these clocks frequencies, the user is ensured that the dynamic memories in the system will be refreshed properly.

Remember to refresh memory properly, the Z80 must be able to execute op codes!

DELAY FOR A TYPICAL MEMORY SYSTEM
Figure 2.
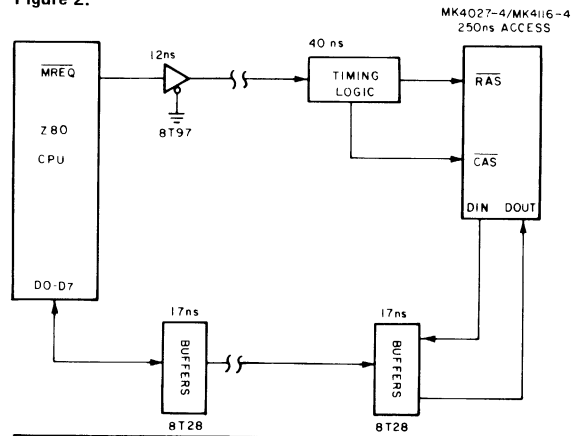
SUPPORT CIRCUITS FOR DYNAMIC MEMORY INTERFACE

Two support circuits are necessary to ensure reliable operation of dynamic memory with the Z80.

The first of these circuits is an address latch shown in Figure 3. The latch is used to hold addresses A_{12}-A_{15} while $\overline{MREQ}$ is active. This action is necessary because the Z80 does not ensure the validity of the address bus at the end of the op code fetch (see Figure 4). This action does not directly affect dynamic memories because they latch addresses internally. The problem comes from the address decoder which generates $\overline{RAS}$. If the address lines which drive the decoder are allowed to change while $\overline{MREQ}$ is low, then a "glitch" can occur on the $\overline{RAS}$ line or lines (if more than one row of RAMs are used) which may have the effect of destroying one row of data.

The second support circuit is used to generate a power on and short manual reset pulse. Recall from the discussion under Z80 Timing and Memory Con-

ADDRESS LATCH
Figure 3.
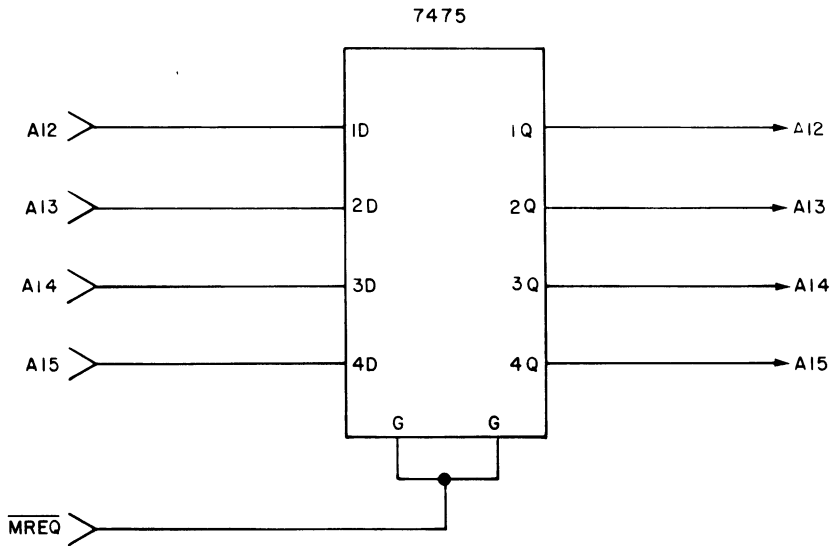
RAS TIMING WITH AND WITHOUT ADDRESS LATCH
Figure 4.
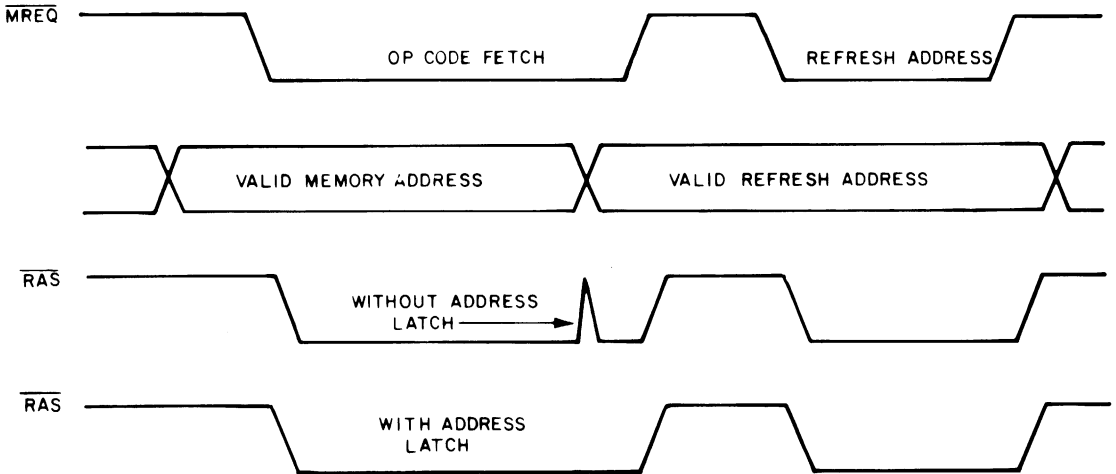
trol Signals that one of the conditions that will cause dynamic memory to be destroyed is a reset pulse of duration greater than 1ms. The circuit shown in Figure 5a can be used to generate a short reset pulse from either a push button or an external source. Additionally the manual reset is synchronized to the start of an M1 cycle so that the reset will not fall during the middle of a memory cycle. Along with the manual reset, the circuit will also generate a power on reset.

If it is not necessary that the contents of the dynamic memory be preserved, then the reset circuit shown in Figure 5b may be used to generate a manual or power on reset.

MANUAL AND POWER-ON RESET CIRCUIT
Figure 5a.
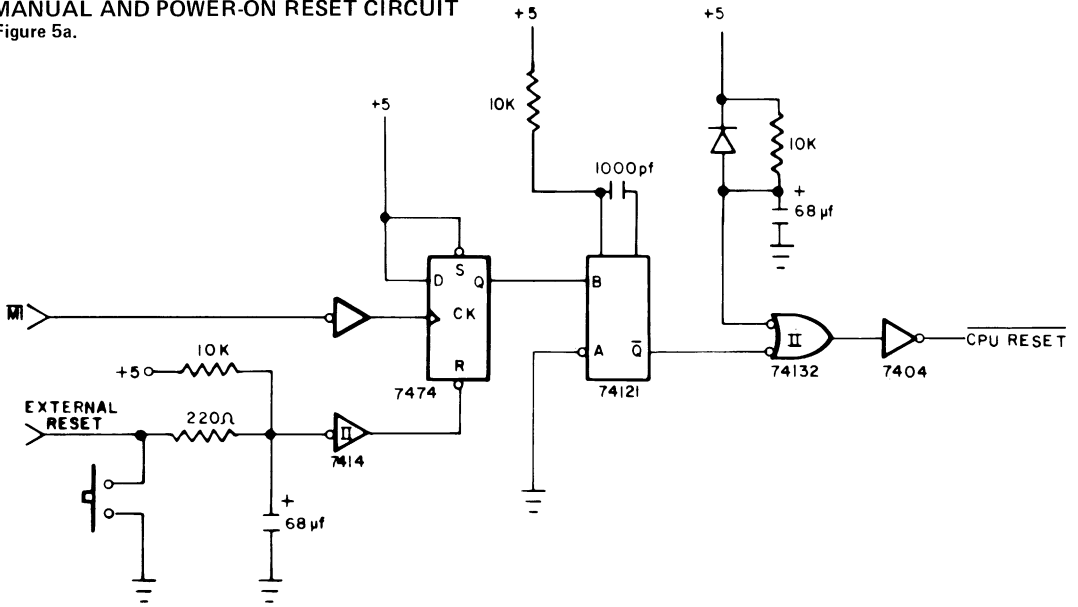
MANUAL AND POWER-ON RESET CIRCUIT
Figure 5b.
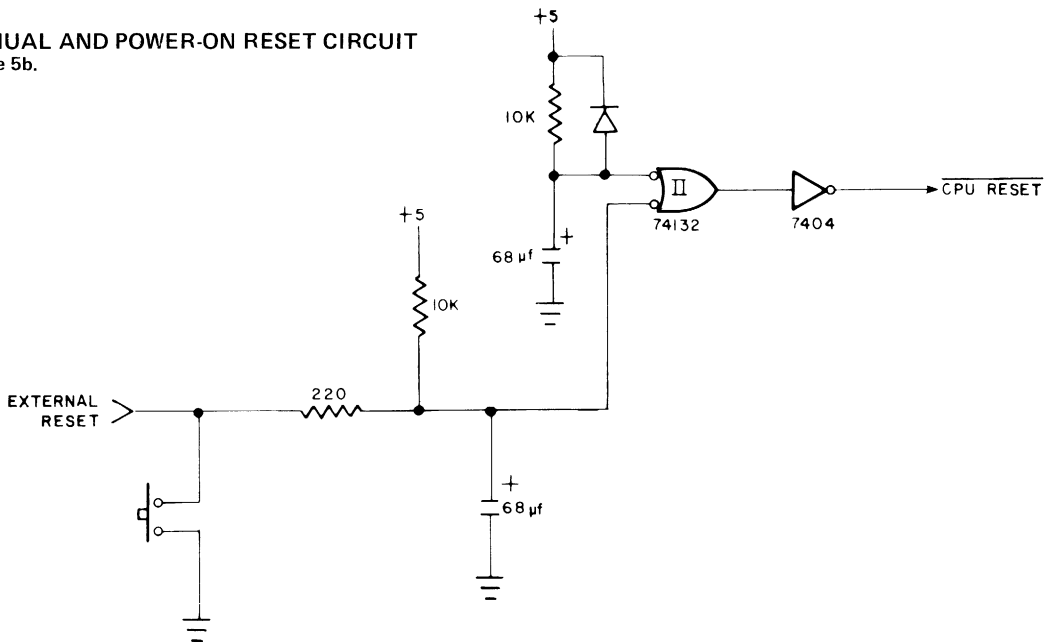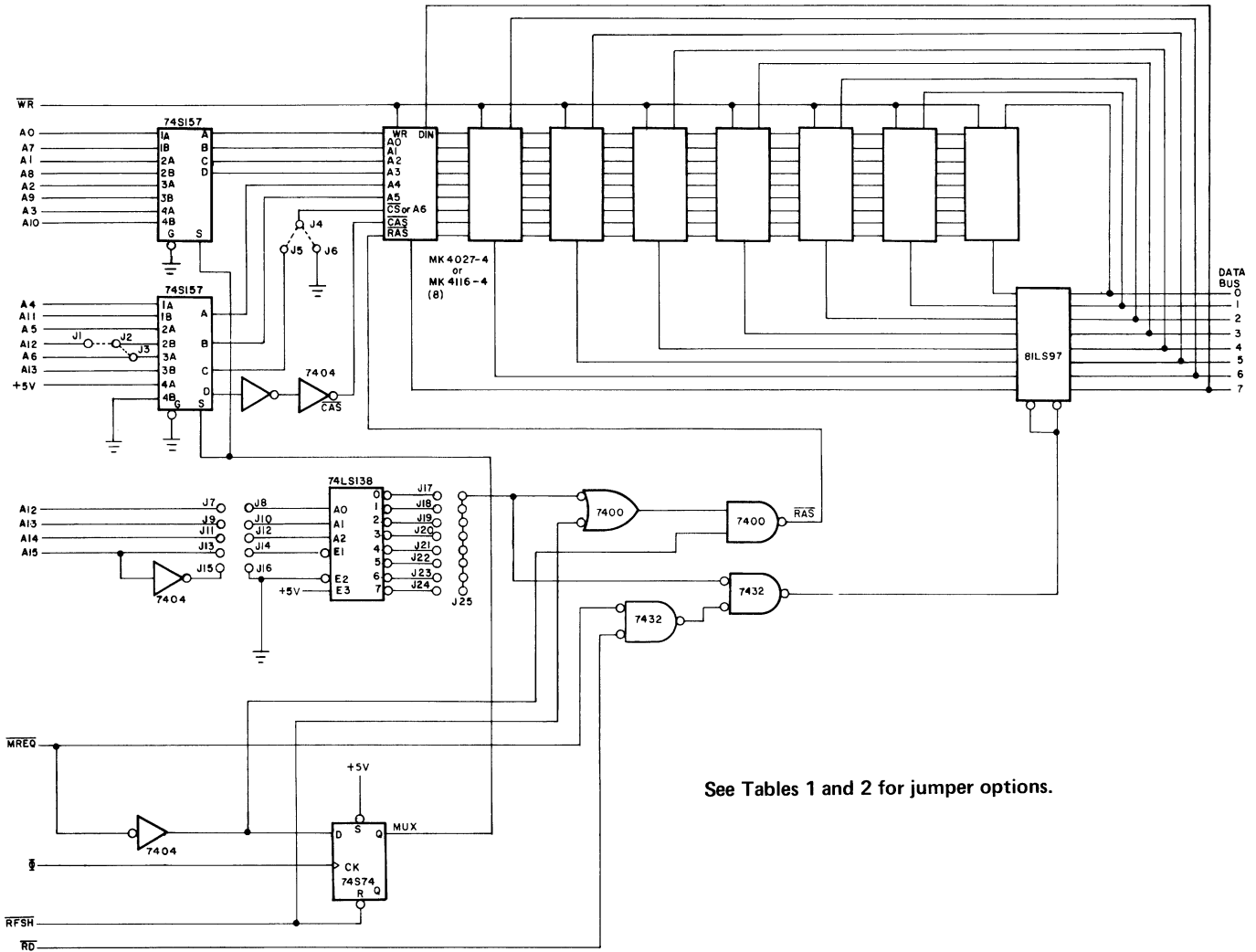
See Tables 1 and 2 for jumper options.

DESIGN EXAMPLES FOR INTERFACING THE Z80 TO DYNAMIC MEMORY

To illustrate the interface between the Z80 and dynamic memory, two design examples are presented. Example number 1 is for a 4K/16Kx8 memory and the example number 2 is a 16K/64Kx8 memory.

Design Example Number 1: 4K/16Kx8 Memory

This design example describes a 4K/16Kx8 memory that is best suited for a small single board Z80 based microcomputer system. The memory devices used in the example are the MK4027 (4,096x1 MOS Dynamic RAM) and the MK4116 (16,384x1 MOS Dynamic RAM). A very important feature of this design is the ease in which the memory can be expanded from a 4Kx8 to a 16Kx8 memory. This is made possible by the use of jumper options which configure the memory for either the MK4027 or the MK4116. See Table 1 and 2 for jumper options.

Figure 6 shows the schematic diagram for the 4K/16Kx8 memory. A timing diagram for the Z80 control signals and memory control signals is shown in Figure 7. The operation of the circuit may be described as follows: $\overline{RAS}$ is generated by NANDing MREQ with RFSH + ADDRESS DECODE. $\overline{RFSH}$ is generated directly from the Z80 while address decode comes from the 74LSl38 decoder. Address decode indicates that the address on the bus falls within the memory boundaries of the memory. If an op code fetch or memory read is being executed the 81LS97 output buffer will be enabled at approximately the same time as $\overline{RAS}$ is generated for the memory array. The output buffer is enabled only during an op code fetch or memory read when $\overline{ADDRESS}$ $\overline{DECODE}$, $\overline{MREQ}$, and $\overline{RD}$ are all low. The switch multiplexer signal (MUX) is generated on the rising edge of Φ after $\overline{MREQ}$ has gone low during an op code fetch, memory read or memory write. After MUX is generated and the address multiplexers switch from the row address to column address, $\overline{CAS}$ will be generated. $\overline{CAS}$ comes from one of the outputs of the multiplexer and is delayed by two gate delays to ensure that the proper column address set-up time will be achieved. Once $\overline{RAS}$ and $\overline{CAS}$ have been generated for the memory array, the memory will then access the desired location for a read or write operation.

7404	22ns	Generate $\overline{RAS}$ from $\overline{MREQ}$
7400	15ns	
	63ns	$\overline{RAS}$ to rising edge of Φ
74S74	10ns	Φ to MUX
74S157	15ns	
7404	22ns	Generate $\overline{CAS}$ from MUX
7404	15ns	
t_{CAC}	165ns	$\overline{CAS}$ access time
81LS97	22ns	Output buffer delay
	349ns	Worst case access

DESIGN EXAMPLE NO. 1 MEMORY TIMING
Figure 7.
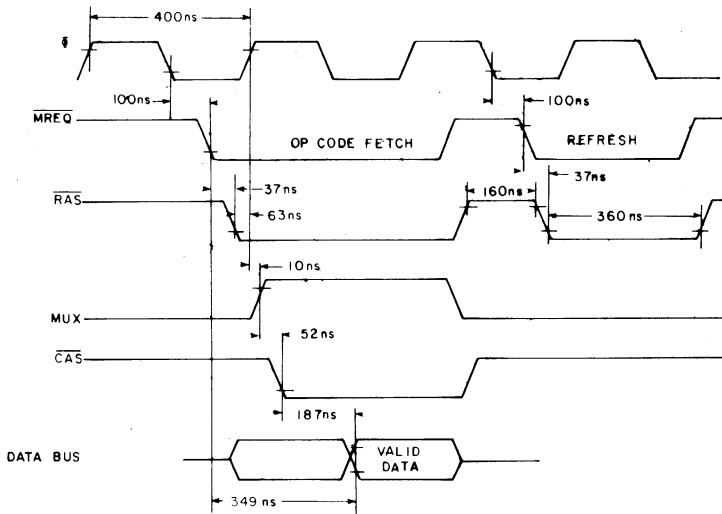
The worst case access time required by the CPU for the op code fetch is 450ns (from equation 1); therefore, the circuit exceeds the required access time by 101ns (worst case).

The circuit shown in Figure 6 provides excellent performance when used as a small on board memory. The memory size should be held at eight devices because there is not sufficient timing margin to allow the interface circuit to drive a larger memory array.

Design Example Number 2: 16Kx8 Memory

This design example describes a 16K/64Kx8 memory which is best suited for a Z80 based microcomputer system where a large amount of RAM is desired. The memory devices used in this example are the same as for the first example, the MK4027 and the MK4116. Again as with the first example, the memory may be expanded from a 16Kx8 to a 64Kx8 by reconfiguring jumpers. See Table 3 and 4 for jumper options.

Figure 8 shows the schematic diagram for the 16K/64K memory. A timing diagram is shown in Figure 9. The operation of the circuit can be described as follows: $\overline{RAS}$ is generated by NANDing MREQ with ADDRESS DECODE (from the two 74LSI38s) + RFSH. Only one row of RAMs will receive a $\overline{RAS}$ during an op code fetch, memory read or memory write. However, a $\overline{RAS}$ will be generated for all rows within the array during a refresh cycle. $\overline{MREQ}$ is inverted and fed into a TTL compatible delay line to generate MUX and $\overline{CAS}$. (This particular approach differs from the method used in example number 1 in that all memory timing is referenced to MREQ, whereas the circuit in example number 1 bases its

memory timing from both $\overline{MREQ}$ and the clock. Both methods offer good results, however, the TTL delay line approach offers the best control over the memory timing.) MUX is generated 65ns later and is used to switch the 74157 multiplexers from the row to the column address. The 65ns delay was chosen to allow adequate margin for the row address hold time t_{RAH}. At 110ns, $\overline{CAS}$ is generated from the delay line and NANDed with RFSH, which inhibits a $\overline{CAS}$ during refresh cycle. After $\overline{CAS}$ is applied to the memory, the desired location is then accessed. A worst case access timing analysis for the circuit shown in Figure 8 can be computed as follows:

74LS14	22ns	} Generate $\overline{RAS}$ from $\overline{MREQ}$
74LS00	15ns	
delay line	50ns	MUX from $\overline{RAS}$
delay line	45ns	} $\overline{CAS}$ delay from MUX
7400	20ns	
t_{CAC}	165ns	Access time from $\overline{CAS}$
8833	30ns	Output buffer delay
	347ns	

The required access time from the CPU is 450ns (from equation 1). This leaves 103ns of margin for additional CPU buffers on the control and address lines. This particular circuit offers excellent results for an application which requires a large amount of RAM memory. As mentioned earlier, the memory timing used in this example offers the best control over the memory timing and would be ideally suited for an application which required direct memory access (DMA).

4K x 8 CONFIGURATION (MK4027) JUMPER
Table 1

CONNECT: J13 to J14		Connect:	J2 to J3	CONNECT: J14 to J15	
ADDRESS	CONNECT		J4 to J6	ADDRESS	CONNECT
0000-0FFF	J17 to J25		J7 to J8	8000-8FFF	J17 to J25
1000-1FFF	J18 to J25		J9 to J10	9000-9FFF	J18 to J25
2000-2FFF	J19 to J25		J11 to J12	A000-AFFF	J19 to J25
3000-3FFF	J20 to J25			B000-BFFF	J20 to J25
4000-4FFF	J21 to J25			C000-CFFF	J21 to J25
5000-5FFF	J22 to J25			D000-DFFF	J22 to J25
6000-6FFF	J23 to J25			E000-EFFF	J23 to J25
7000-7FFF	J24 to J25			F000-FFFF	J24 to J25

16K x 8 CONFIGURATION (MK4116) JUMPER CONNECTIONS
Table 2

CONNECT:		ADDRESS	CONNECT
	J1 to J2		
	J4 to J5		
	J8 to J11	0-3FFF	J17 to J25
	J10 to J13	4000-7FFF	J18 to J25
	J12 to J16	8000-BFFF	J19 to J25
	J14 to J16	C000-FFFF	J20 to J25

16K x 8 CONFIGURATION (MK4027)
Table 3

CONNECT: J1 to J3
            J5 to J6
            J7 to J8
            J9 to J10
            J11 to J12
            J13 to J14

ADDRESS:	0-3FFF	ADDRESS:	4000-7FFF	ADDRESS:	8000-BFFF	ADDRESS:	C000-FFFF
CONNECT:	J24 to J25	CONNECT:	J16 to J17	CONNECT:	J40 to J41	CONNECT:	J32 to J33
	J26 to J27		J18 to J19		J42 to J43		J34 to J35
	J28 to J29		J20 to J21		J44 to J43		J36 to J37
	J30 to J31		J22 to J23		J46 to J47		J38 to J39

64K x 8 CONFIGURATION (MK4116)
Table 4

CONNECT: J1 to J2   ADDRESS: 0-FFFF
          J4 to J5   CONNECT: J32 to J33
          J8 to J11   J34 to J35
          J10 to J13   J36 to J37
          J12 to J15   J38 to J39
          J14 to J15

SYSTEM PERFORMANCE CHARACTERISTICS
Table 5

The system characteristics for the preceeding design
examples are shown in Table 5.

EXAMPLE #	MEMORY CAPACITY	MEMORY ACCESS	POWER REQUIREMENTS
1	4K/16Kx8	349ns max.	+12V @ 0.0250 A max. +5V @ 0.422 A max.* -5V @ 0.030 A max.
2	16K/64Kx8	347ns max.	+12V @ 0.600 A max. +5V @ 0.550 A max. * -5V @ 0.030 A max.

*All power requirements are max.; operating temperature 0°C
to 70°C ambient, max +12V current computed with Z80
executing continuous op code fetch cycles from RAM at
1.6 μ s intervals.
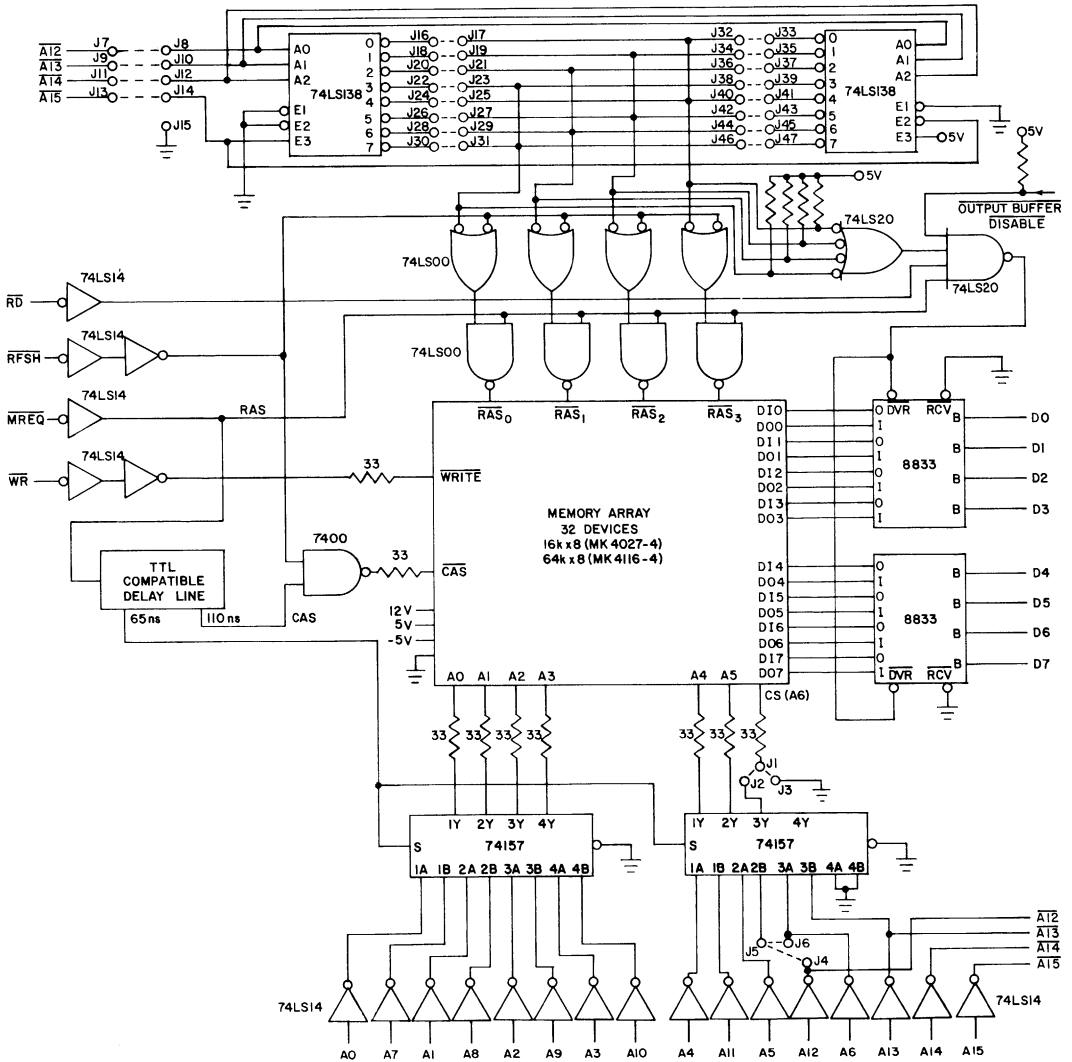
FOR JUMPER OPTIONS SEE TABLES 3 AND 4

DESIGN EXAMPLE NO. 2 MEMORY TIMING
Figure 9.
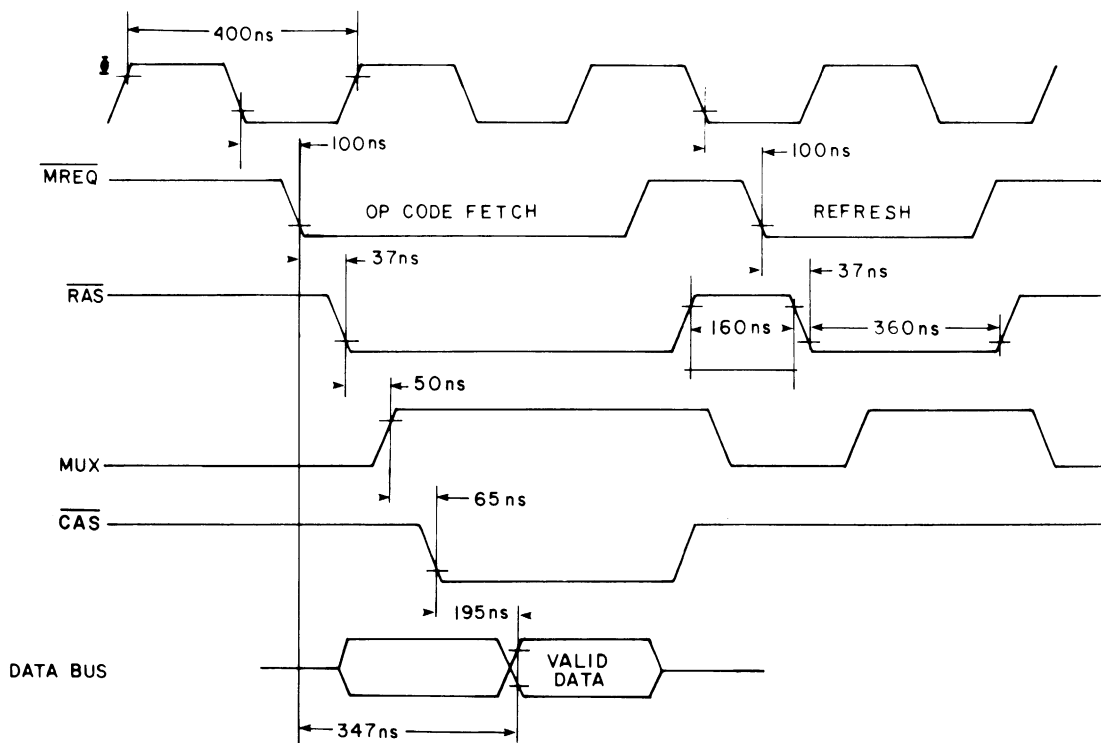
PRINTED CIRCUIT LAYOUT

One of the most important parts of a dynamic memory design is the printed circuit layout. Figure 10 illustrates a recommended layout for 32 devices. A very important factor in the P.C. layout is the power distribution. Proper power distribution on the V_{DD} and V_{BB} supply lines is necessary because of the transient current characteristics which dynamic memories exhibit. To achieve proper power distribution, V_{DD}, V_{BB}, V_{CC} and ground should be laid out in a grid to help minimize the power distribution impedance. Along with good power distribution, adequate capacitive bypassing for each device in the memory array is necessary. In addition to the individual by-passing capacitors, it is recommended that each supply (V_{BB}, V_{CC} and V_{DD}) be bypassed with an electrolytic capacitor $20\mu F$.

By using good power distribution techniques and using the recommended number of bypassing capacitors, the designer can minimize the amount of noise in the memory array. Other layout considerations are the placement of signal lines. Lines such as address, chip select, column address strobe, and write should be bussed together as rows; then, bus all rows together at one end of the array. Interconnection between rows should be avoided. Row address strobe lines should be bussed together as a row, then connected to the appropriate $\overline{RAS}$ driver. TTL drivers for the memory array signals should be located as close as possible to the array to help minimize signal noise.

For a large memory array such as the one shown in design example number 2, series terminating resistors should be used to minimize the amount of negative undershoot. These resistors should be used on the address lines, $\overline{CAS}$ and $\overline{WRITE}$, and have values between 20 Ω to a 33 Ω .

The layout for a 32 device array can be put in a 5" x 5" area on a two sided printed circuit board.
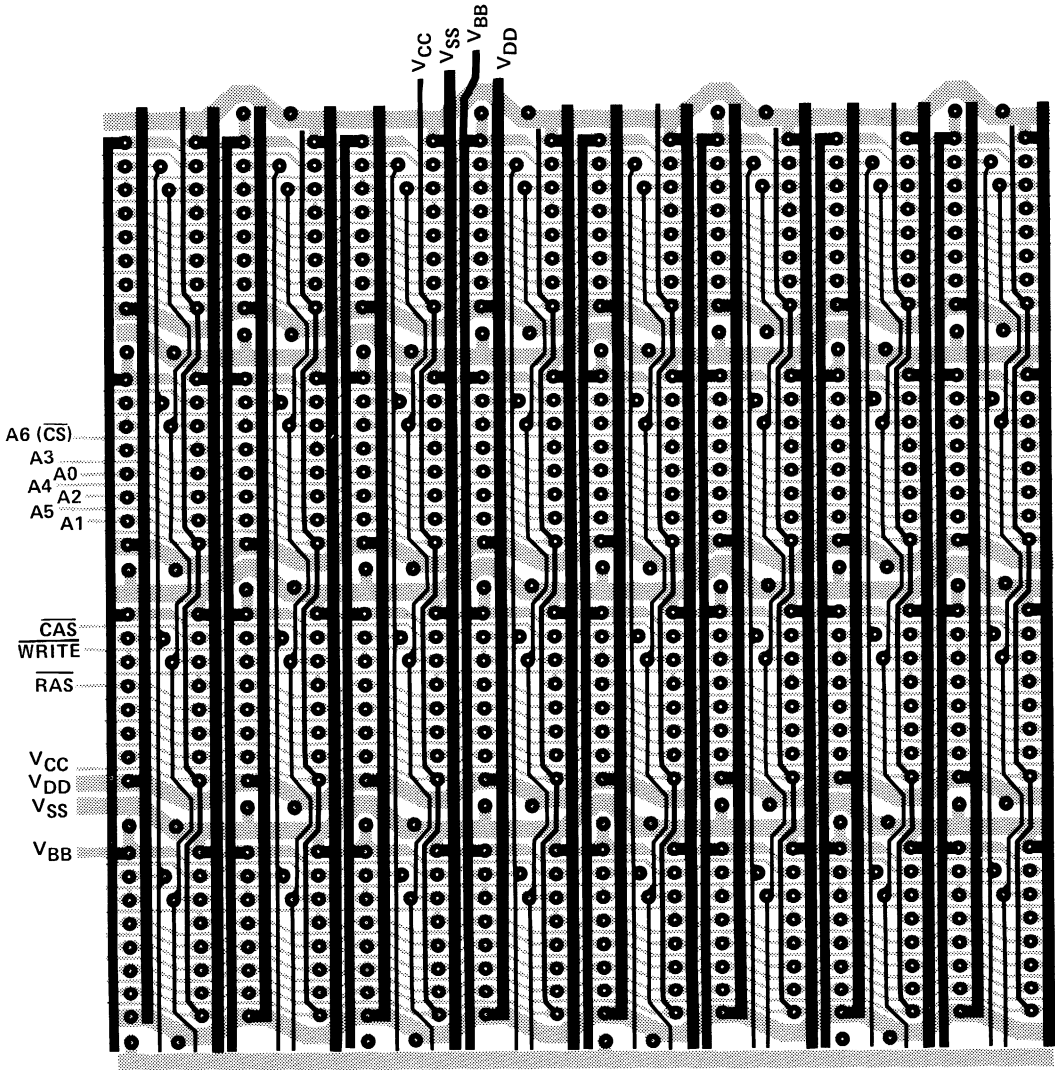
4MHz Z80 DYNAMIC MEMORY INTERFACE CONSIDERATIONS

A 4MHz Z80 is available for the microcomputer designer who needs higher system throughput. Considerations which must be faced by the designer when interfacing the 4MHz Z80 to dynamic memory are the need for memories with faster access times and for providing minimum RAM precharge time. The access times required for dynamic memory interfaced to a 4MHz Z80 can be computed from equations 1 and 2 under Z80 Timing and Memory Control Signals.

Access time for op code fetch for 4MHz Z80,
let: t_C = 250ns; $t_{DL\overline{\Phi}(MR)}$ = 75ns; $t_{s\Phi(D)}$ = 35ns
then: $t_{ACCESS\ OP\ CODE}$ = 265ns
    Access time for memory read for 4MHz Z80,
let: t_C = 250ns; $t_{DL\overline{\Phi}(MR)}$ = 75ns; $t_{S\Phi(D)}$ = 50ns
then: $t_{ACCESS\ MEMORY\ READ}$ = 375ns

The problem of faster access times can be solved by using 200ns memories such as the MK4027-3 or MK4116-3. Depending on the number of buffer delays in the system, the designer may have to use 150ns memories such as the MK4027-2 or MK4116-2. The most critical problem that exists when interfacing dynamic memory to the 4MHz Z80 is the RAM precharge time (trp). This parameter is called $t_{W(MRH)}$ on the Z80 and can be computed by the following equation.

(4) $t_{W(RH)} = t_{W(\Phi H)} + t_f - 20ns$
let: $t_{W(\Phi H)}$ = 110ns; t_f = 5ns
then: $t_{W(MRH)}$ = 95ns

A $t_{W(MRH)}$ of 95ns will not meet the minimum precharge time of the MK4027-2 or MK4116-2 which is 100ns. The MK4027-3 and MK4116-3 require a 120ns precharge. Figure 11 shows a circuit that will lengthen the $t_{W(MRH)}$ pulse from 95ns to a minimum of 126ns while only inserting one gate delay into the access timing chain. Figure 12 shows the timing for the circuit of Figure 11. The operation of the circuit in Figure 11 can be explained as follows: The D flip flops are held in a reset condition until MREQ goes to its active state. After MREQ goes active, on the next positive clock edge, the D input of U1 and U2 will be transferred to the outputs of the flip flops. Output QA will go high if M1 was high when Φ clocked U1. Output QB will go low on the next positive going clock edge, which will cause the output of U3 to go low and force the output of U4, which is $\overline{RAS}$, high. The flip flops will be reset when MREQ goes inactive.

The circuit shown in Figure 11 will give a minimum of 126ns precharge for dynamic memories, with the Z80 operating at 4MHz. The 126ns $t_{W(MRH)}$ is computed as follows.

110ns	$t_{W(\Phi H)}$ - clock pulse width high (min)
5ns	t_F - clock full time (min)
20ns	$t_{DL\overline{\Phi}(MR)}$ - MREQ delay (min)
-9ns	74S74 delay (min)
126ns	$t_{W(MRH)}$ modified (min)

4MHz Z80 PRECHARGE EXTENDER FOR DYNAMIC MEMORIES
Figure 11.
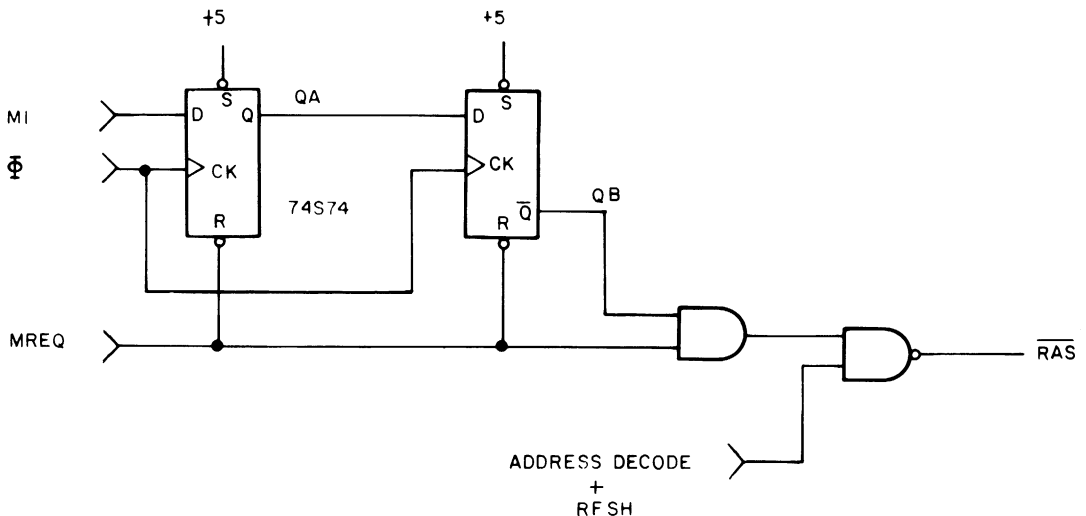
TIMING DIAGRAM FOR 4MHz Z80 PRECHARGE EXTENDER

Figure 12

OP CODE FETCH | PRECHARGE | REFRESH
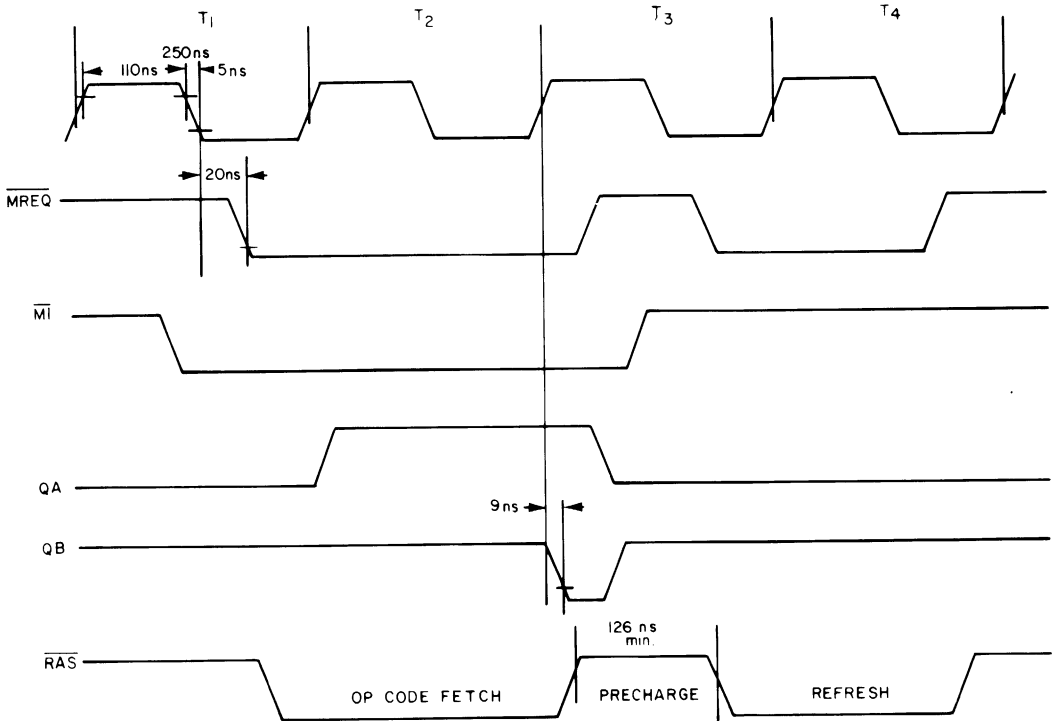
APPENDIX

MEMORY TEST ROUTINE

This section is intended to give the microcomputer designer a memory diagnostic suitable for testing memory systems such as the ones shown in Section VI.

The routine is a modified address storage test with an incrementing pattern. A complete test requires 256_{10} passes, which will execute in less than 4 minutes for a 16Kx8 memory. If an error occurs, the program will store the pattern in location '2C'H and the address of the error at locations '2D'H and '2E'H.

The program is set up to test memory starting at location '2F'H up to the end of the block of memory defined by the bytes located at '0C'H and '0D'H. The test may be set up to start at any location by modifying locations '03'H - '04'H and '11'H - '12'H with the starting address that is desired.

```
                         MXRTS   LISTING                    PAGE    0001
        LOC    OBJ CODE   STMT SOURCE STATEMENT
                          0001 ;TRANSLATED FROM DEC 1976 INTERFACE MAGAZINE
                          0002 ;
                          0003 ;THIS IS A MODIFIED ADDRESS STORAGE TEST WITH AN
                          0004 ;INCREMENTING PATTERN
                          0005 ;
                          0006 ;256 PASSES MUST BE EXECUTED BEFORE THE MEMORY IS
                          0007 ;COMPLETELY TESTED.
                          0008 ;
                          0009 ;IF AN ERROR OCCURS, THE PATTERN WILL BE STORED
                          0010 ;AT LOCATION '002C'H AND THE ADDRESS OF THE
                          0011 ;ERROR LOCATION WILL BE STORED AT '002D'H AND
                          0012 ;'002E'H.
                          0013 ;
```

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```
                        0014 ;THE CONTENTS OF LOCATIONS '000C'H AND '001D'H
                        0015 ;SHOULD BE SELECTED ACCORDING TO THE FOLLOWING
                        0016 ;MEMORY SIZE TO BE TESTED
                        0017 ;
                        0018 ;TOP OF MEMORY TO
                        0019 ;BE TESTED                              VALUE OF EPAGE
                        0020 ;
                        0021 ;     4K                                      '10'H
                        0022 ;     8K                                      '20'H
                        0023 ;    16K                                      '40'H
                        0024 ;    32K                                      '80'H
                        0025 ;    48K                                      'C0'H
                        0026 ;    64K                                      'FF'H
                        0027 ;
                        0028 ;THE PROGRAM IS SET UP TO START TESTING AT
                        0029 ;LOCATION '002F'H. THE STARTING ADDRESS FOR THE
                        0030 ;TEST CAN BE MODIFIED BY CHANGING LOCATIONS
                        0031 ;'0003-0004'H AND '0011-0012'H.
                        0032 ;
                        0033 ;TEST TIME FOR A 16K X 8 MEMORY IS APPROX. 4 MIN
                        0034 ;
0000                    0035           ORG   0000H
0000      0600          0036           LD    B,0          ;CLEAR B PATRN MODIFIER
                        0037 ;LOAD UP MEMORY
0002      212F00        0038 LOOP:     LD    HL,START     ;GET STARTING ADDR
0005      7D            0039 FILL:     LD    A,L          ;LOW BYTE TO ACCM
0006      AC            0040           XOR   H            ;XOR WITH HIGH BYTE
0007      A8            0041           XOR   B            ;XOR WITH PATTERN
0008      77            0042           LD    (HL),A       ;STORE IN ADDR
0009      23            0043           INC   HL           ;INCREMENT ADDR
000A      7C            0044           LD    A,H          ;LOAD HIGH BYTE OF ADDR
000B      FE10          0045           CP    EPAGE        ;COMPARE WITH STOP ADDR
000D      C20500        0046           JP    NZ,FILL      ;NOT DONE,GO BACK
                        0047 ;READ AND CHECK TEST DATE
0010      212F00        0048           LD    HL,START     ;GET STARTING ADDR
0013      7D            0049 TEST:     LD    A,L          ;LOAD LOW BYTE
0014      AC            0050           XOR   H            ;XOR WITH HIGH BYTE
0015      A8            0051           XOR   B            ;XOR WITH MODIFIER
0016      BE            0052           CP    (HL)         ;COMPARE WITH MEMORY LOC
0017      C22500        0053           JP    NZ,FXIT      ;ERROR EXIT
001A      23            0054           INC   HL           ;UPDATE MEMORY ADDRESS
001B      7C            0055           LD    A,H          ;LOAD HIGH BYTE
001C      FE10          0056           CP    EPAGE        ;COMPARE WITH STOP ADDR
001E      C21300        0057           JP    NZ,TEST      ;LOOP BACK
0021      04            0058           INC   B            ;UPDATE MODIFIER
```

```
                           MXRTS  LISTING                       PAGE   0002
     LOC   OBJ CODE   STMT SOURCE STATEMENT

     0022  C30200     0059           JP    LOOP       ;RST WITH NEW MODIFIER
                      0060 ;ERROR EXIT
     0025  222D00     0061 FXIT:     LD    (BYTE),HL ;SAVE ERROR ADDRESS
     0028  322C00     0062           LD    (PATRN),A ;SAVE BAD PATTERN
     002B  76         0063           HALT            ;FLAG OPERATOR
     002C             0064 PATRN:    DEFS  1
     002D             0065 BYTE:     DEFS  2
     002F  2F00       0066 START:    DEFW  S
                      0068 EPAGE:    EQU   10H        ;SET UP FOR 4K TEST
                      0069           END
```

MOSTEK®

A TESTING PHILOSOPHY FOR 16K DYNAMIC MEMORIES
Testing

By ROBERT W. OWEN

Today several semiconductor manufacturers are moving 16384 bit dynamic MOS memories into volume production. The circuit will be the most cost-effective method of providing medium performance, large capacity randomly accessible data storage over the next several years and will in all likelihood be shipped in larger volume to more users than has any previous memory chip. This burgeoning market will confront many engineers with the problems of performing comparative evaluations, writing incoming device tests, system and diagnostic tests, and field troubleshooting and repair of memory systems containing many 16K chips. A thorough understanding of the device permits the engineer to evaluate the adequacy of manufacturers' outgoing screens and, if necessary, to institute efficient incoming tests which comprehend the differences or shortcomings in the individual designs or outgoing test procedures.

Since the 16K has established the state-of-the-art in MOS design and processing at this point in time, the test sequences utilized must be carefully considered to keep test times to a reasonable minimum while at the same time adequately screening out marginal devices. The testing considerations themselves are applicable to earlier 1K and 4K circuits as well; the penalties for inadequacy are greater.

A brief description of manufacturing test procedures which relate ultimately to the quality and reliability of the memory chip would include characterization tests, in which the processing constraints and operating limits of a specific design are determined; reliability tests, which subject production lots to abnormal stresses in order to convert latent defects into failures prior to the final test; and the final test itself in which the manufacturer must always tread a thin line between test·throughput (minimum test cost per device) and thoroughness. The quality of these tests varies from manufacturer to manufacturer and is manifested in the quality of their shipped product. Good design and quality processing are not enough, alone, to guarantee reliability; they must always be augmented by adequate testing.

BASIC CONSIDERATIONS

The storage element in all 16K RAMs is an MOS capacitor with data transfer and isolation controlled by a single transistor. This is the well known single transistor (IT) cell, used for the first time in the 4K memory devices which have been available for several years. The small size of the cell (about 0.7 mil^2 when fabricated in the double level polysilicon process) is sufficient inducement that the disadvantages are tolerated by the designer. Read-out is destructive, requiring an internal restore operation after each read. Available signal levels are dictated by the ratio of cell to digit line capacitance and are on the order of one to two hundred millivolts. Charge storage is of course dynamic in nature, since the charge stored on the capacitor will eventually leak off.

Storage time is an intrinsic device parameter; refresh time (more properly refresh interval) is a timing parameter which specifies the maximum allowable interval separating two operations on the same storage location which will re-establish the full charge on a partially-decayed high level.

The storage time of any dynamic MOS RAM may be expressed by the empirical equation

$$t_{STORAGE} = A \exp(-BT)$$

where

T is junction temperature in °C

B is a variable relating the magnitude of the generation-recombination current to the junction temperature (units of 1/°C)

and

A is a scaling constant reflecting such variables as junction area, bulk defect density, and sense amplifier design.

Note that the term "B" in the equation is not a constant. Conventionally it is assumed that the storage time doubles for every 10 °C decrease in junction temperature, which is equivalent to assuming that B = 0.069. Data shows that a typical value for B is 0.055, but that it does in fact vary at least 30% from this typical value. This equation is graphed in Figure 1 for several different values of B, arbitrarily assuming a minimum storage time of 2 milliseconds at $T_J = 100$°C. The storage time at $T_J = 25$°C for this hypothetical device will lie somewhere between 50 milliseconds and 381 milliseconds. If room temperature testing is to be attempted, the refresh interval would have to be set at 381 milliseconds, since any lesser value would not guarantee 2 milliseconds at 100° C. The devices which failed such a test would

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not necessarily be failures at 2 ms, 100°C, and would therefore have to be rescreened at the 100°C temperature. The efficiency of this procedure depends upon the number of good devices found by the first screen, but in general the number of units requiring a second test is so great that the first screen may as well be eliminated in favor of a 100% screen at the maximum junction temperature.

Storage time is of course not the only parameter of interest. Other parameters which need to be verified over the temperature range include access time, power dissipation, and input/output levels. Access time and power dissipation are functions of transistor gain. Gain is temperature dependent through carrier mobility and is about 25% lower at 100°C than at 0°C. Access time is therefore worst-case at elevated temperatures. The memory will dissipate more power at low temperature, although much of the power required is capacitive and therefore frequency rather than temperature related. Signal levels are functions of transistor threshold voltage, which decreases about two millivolts for every 1°C increase in temperature. Input high levels and output high and low levels are normally worst-case at low temperature and must be guardbanded if tested only at high temperature. (One 16K RAM, the MOSTEK MK 4116, utilizes an integrated reference voltage for address and data inputs which removes the threshold voltage dependence and therefore the temperature dependence of these inputs.) As will be discussed later, a few timing parameters become worst-case as the memory becomes faster, and need to be guardbanded if testing only at high temperature. On balance, however, due primarily to the extreme variation of storage time with temperature, it is most practical to conduct tests at the maximum junction temperature only and guardband non-worst-case parameters.

The two junction temperatures singled out in Figure 1 were not chosen at random. The equation describing temperature rise over an ambient is

$$T_J - T_A = \triangle T = \theta_{JA} P_D$$

where

θ_{JA} is the junction to ambient thermal resistance (for 16 pin ceramic DIP mounted in a socket on a double-sided PC board, the most widely accepted value is 70°C/watt)

and

P_D is the power dissipation of the device under the conditons of interest.

To calculate $\triangle T$, assume the following specified values:

$$I_{DD} \text{ (ACTIVE)} = 35 \text{ MA}$$
$$I_{DD} \text{ (STANDBY)} = 1.5 \text{ MA}$$
$$V_{DD} \text{ (MAXIMUM)} = 13.2 \text{V}$$
$$t_{cycle} = 375 \text{ ns}$$

and assume that the refresh test is conducted by writing 16384 bits at the 375 ns cycle rate, pausing in the standby condition for the refresh interval, then reading all bits again at 375 ns. The rise in junction temperature can now be calculated:

$$t_{REFRESH} = 2\text{ms; duty factor (DF)} =$$
$$\frac{2(16384)375\text{ns}}{2(16384)375\text{ns} + 2\text{ms}} = 0.86$$

$$\triangle T = \theta_{JA} (P_D \text{ ACTIVE (DF)} + P_D \text{ STANDBY}$$
$$(1 - DF))$$

$$= 70 °C/W (0.035 (13.2) 0.86 + 0.0015$$
$$(1 - 0.86))$$

$$= 28°C$$

$$t_{REFRESH} = 381\text{ms; duty factor (DF)} =$$
$$\frac{2(16384)375\text{ns}}{2(16384)375\text{ns} + 381\text{ms}} = 0.03$$

$$\triangle T = 70° C/W (0.035 (13.2) 0.03 + 0.0015$$
$$(13.2) (1 - 0.03))$$

$$= 2.3°C$$

The junction temperature of a device executing a 381 ms refresh test at $T_A = 25°$ C would rise only 2.3 degrees to 27.3 °C, while the same device executing a 2ms refresh test at $T_A = 70°$ C would have a junction temperature of 98°C.

Strictly speaking, the foregoing calculations are true only if the refresh test in question is run in a continuous mode allowing the junction temperature to stabilize. The thermal mass of the device is not negligible; in fact θ_{JA} is a function of time and has a time constant of approximately 60 seconds in most test situations. Much of the effectiveness of the N^2 test patterns can be attributed to higher junction temperatures due simply to the test length. An N^2 pattern, with N equal to 16384 and a cycle time of 375ns, requires 100 seconds. The value of θ_{JA} after 100 seconds of testing is about 80% of its final

STORAGE TIME VS JUNCTION TEMPERATURE

Figure 1

$t_{STORAGE} = A \exp(-BT)$

381 ms

124 ms

DOUBLES EVERY 9.9°C

DOUBLES EVERY 12.6°C

DOUBLES EVERY 16.1°C

50 ms

STORAGE TIME $t_{STORAGE}$ (Milliseconds)

($t_{STORAGE}$ = 2 ms at T_J = 100°C arbitrary)   JUNCTION TEMPERATURE T_J
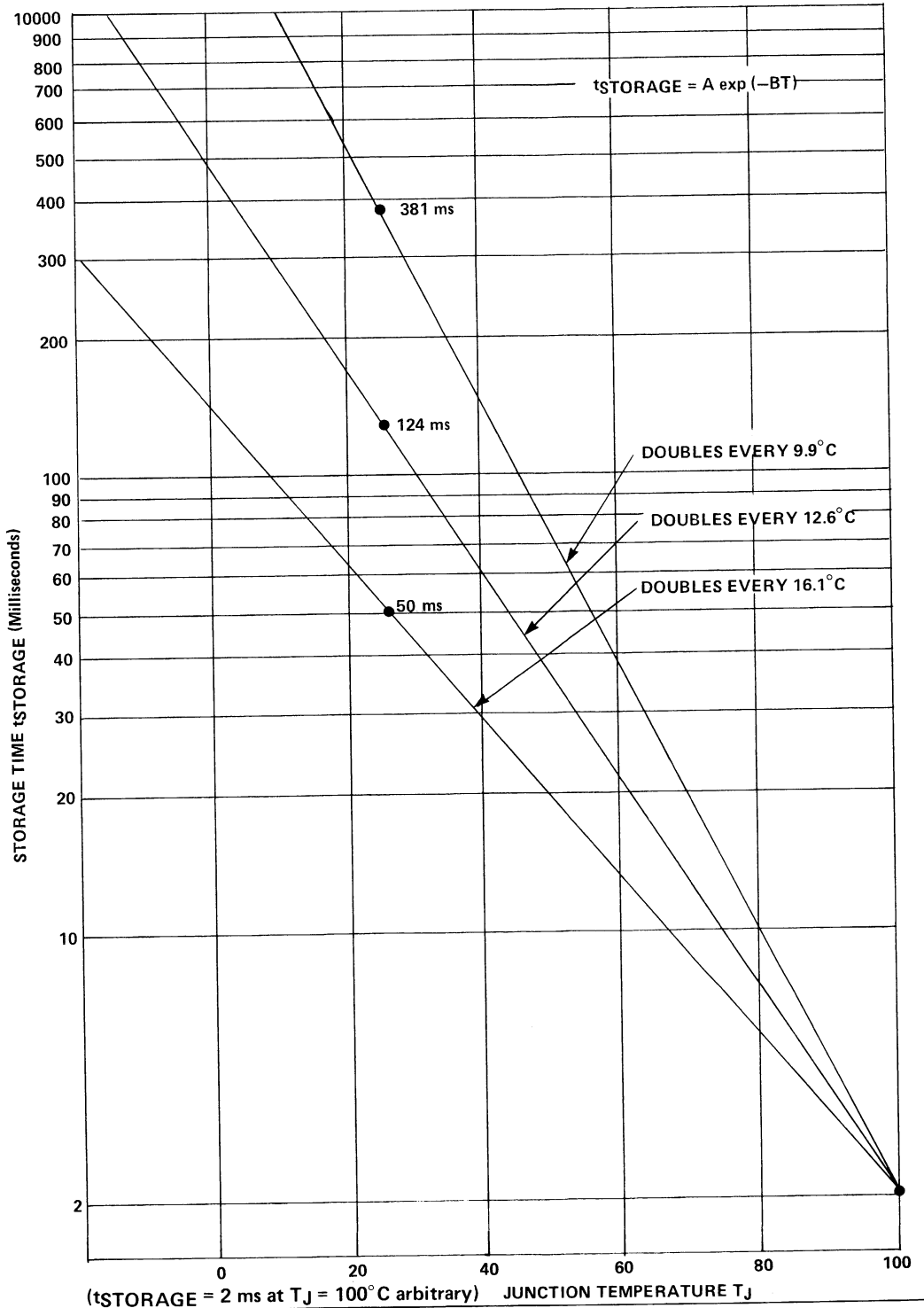
value. The junction rise for P_D = 462 milliwatts is

$$\triangle T = \theta_{JA} \, P_D = (0.8) \, (70^\circ C/W) \, (.462) = 26^\circ C$$

and this rise has occurred during the test. The storage time of the device may be reduced by as much as a factor of 6 and the device speed is approximately 10% less. These benefits can of course be attained without resorting to the use of N^2 patterns by pre-calculating the final junction temperature and setting the temperature chamber accordingly. This approach is common but not without its pitfalls. If the construction of the test chamber is such that heat is maintained throughout the test, the self-heating must be considered; if the device is held in an elevated ambient prior to the test, then removed and inserted into the test socket, the combined effects of heat loss in the socket and self-heating during the test must be characterized.

An accurate method for measuring junction temperature uses the device itself as a temperature reference. All signal inputs connect to pn^+ diodes which may be calibrated by utilizing the fact that if diode current is held constant, diode voltage is linearly proportional to temperature. Calibrate an input on a reference device by stabilizing the device at an accurately measured reference temperature, injecting a constant current, and measuring the diode drop (from the input to the V_{BB} pin). When this has been performed at several temperatures a calibration curve of diode voltage versus temperature may be constructed and the device used to measure unknown temperatures by injecting current, measuring the diode voltage, and referring to the calibration chart. The procedure requires care, but once calibrated the device is capable of profiling heat loss at the test site or junction temperature rise during operation with great accuracy. Several hints: a good value for the current is $100\,\mu A$; the voltage measurement requires millivolt accuracy; the measurement cannot be made while the device is operating because of noise in the substrate (operate the device, then switch out the functional inputs and switch in the measurement circuitry). Each device must be calibrated separately since the magnitude and slope of the relationship varies.

RELIABILITY TESTING

Although the user may not resort to reliability screening himself, relying solely on the manufacturer to choose appropriate tests and apply them wisely, he should be familiar with the basic failure mechanisms and methods employed to screen them out prior to shipment.

Published data on 4K and 16K silicon gate MOS memories [1][2] indicate that two failure mechanisms account for between 50% and 85% of all reported RAM failures. These two mechanisms, oxide defects and defects caused by foreign contamination, vary in the type of screen required for elimination.

Oxide defects are imperfections in the SiO_2 gate oxide introduced during the manufacturing process which can rupture when subjected to an electrical field for some period of time. This failure mode may be screened by subjecting all devices to an overvoltage stress; the effectiveness of the screen is directly dependent upon the field intensity, hence the voltage applied, and to a lesser degree on time. One screen employed by several manufacturers subjects the RAM to an operational test in which the magnitude of the supply voltages is increased by approximately 50% over nominal. This may occur in the testing prior to burn-in, at the burn-in itself, or in the final test prior to shipment. If the overstress occurs at the burn-in itself it may last for 12 to 24 hours, while an overstress during a functional test sequence normally would last less than one second. A commonly-accepted rule of thumb is that the effectiveness of the oxide defect screen varies with $E\sqrt{t}$. A 24 hour burn-in would, according to this rule, be about 17 times as effective as a one-second test assuming both were run at the same voltage, however, increasing the voltage (field strength E) by 50% increases the efficiency of the screen by the same 50%. Clearly the overvoltage screen is necessary; it is incumbent upon the manufacturer to perfrom such a screen himself as it is doubtful he would authorize the user to stress the RAM beyond the data-sheet limits.

The second large category of failures are those caused by contamination of the device by some mobile impurity ion such as sodium. These impurities can move under applied voltage and temperature conditions to some point in the circuit where they can alter the threshold voltage of the MOS transistor. For an N channel 16K memory, the threshold voltages will be lowered if the contaminant is a positive ion and failures can occur either on normal transistors or on spurious field oxide transistors. This failure mode is widely known and reported, and is accelerated by thermal stress. The rate of acceleration is predicated by the equation [3],

$$R = R_O \exp\left(-\frac{E_A}{KT_k}\right)$$

where

R is reaction rate

R_O is a constant

E_A is activation energy in electron volts (eV)

K is Boltzmann's constant (8.63×10^{-5} eV/°K)

T_k is temperature in degrees Kelvin (°K).

The activation energy for contamination-related failures is approximately 1.0 eV, and therefore such failures are subject to removal by high-temperature burn-in, and most manufacturers perform an operating burn-in at 125°C for some number of hours (normally 12 - 24 hours) to reduce the incidence of field failures. On the other hand, the acceleration rate for for gate oxide failures is reported to be between $0.1 - .05$ eV and the high-temperature screen would be marginally effective for gate oxide defects.

At least one manufacturer has combined the overvoltage and high temperature screens and is currently subjecting all 16K RAM's to a 24 hour burn-in at 125°C with the device power supplies at 50% overvoltage (+18 v, −7 v). Here again, such testing is properly done by the manufacturer, but the user should satisfy himself as to the adequacy of the reliability screens performed by the various manufacturers.

Reliability can be greatly impacted by proper design techniques. As an example, consider the equation given for thermal acceleration of failures. Rewriting the equation to allow a comparison of reaction rates at two different temperatures T_{k1} and T_{k2}, we have:

$$\frac{R_1}{R_2} = \exp\left(-\frac{E_A}{K}\left(\frac{T_{k2} - T_{k1}}{T_{k1} T_{k2}}\right)\right).$$

Now the effect of power dissipation upon reliability can be evaluated. For two 16K RAMS, one dissipating 900 milliwatts and one dissipating 450 milliwatts while operating at $T_A = 70°C$,

$$T_{J1} = 70°C + (70°C/W)(0.900 \text{ W}) = 133°C$$

$$T_{J2} = 70°C + (70°C/W)(0.450 \text{ W}) = 101.5°C$$

and assuming that $E_A = 1$ eV,

$$\frac{R_1}{R_2} = \exp\left(-\frac{1}{8.63 \times 10^{-5}}\left(\frac{133 - 101.5}{(133+273)(101.5+273)}\right)\right)$$

$$\frac{R_1}{R_2} = 0.097$$

which predicts a failure rate for the 900 milliwatt device of about 11 times that of the 450 milliwatt device, due to the 31.5°C difference in junction temperature.

MULTIPLEXED DEVICES

All 16K devices announced to date have followed the pinout and address multiplexed architecture pioneered by MOSTEK for their 4K RAM in 1973. The reduction in number of address lines from 14 to 7 (for the 16K) is bought at the expense of a more complex cycle with more timing parameters[4].

Some of these parameters must be examined in detail, as a proper understanding of their interrelationship is necessary. The timing diagram of Figure 2 shows the timing parameters necessary for standard write and read operations. The data output signal is shown for both the MOSTEK and Intel designs.

Three clocks, $\overline{RAS}$ (Row Address Strobe), $\overline{CAS}$ (Column Address Strobe) and $\overline{WRITE}$, must be provided along with seven multiplexed address lines and the D_{IN} (data in) if the memory is to execute a write cycle. Most of the testing difficulties arise from the relationship of $\overline{RAS}$ to $\overline{CAS}$, from the relationships of the addresses to $\overline{RAS}$ and $\overline{CAS}$, and from the relationships of the addresses to $\overline{RAS}$ and $\overline{CAS}$, and from $\overline{CAS}$ to the D_{OUT} (data output).

$\overline{RAS}$ initiates the cycle by going from the high state to the low state. It must have remained high long enough for internal nodes to be precharged to a known initial state prior to initiation of a new cycle; if the parameter t_{RP} is violated (made too short) internal clocks, address buffers, decoders, and sense amplifiers are not adequately initialized. Once $\overline{RAS}$ goes low it must remain low long enough (t_{RAS}) for the selection of the accessed cells, sense operation, and restoration of the destroyed data (the 1T cell reads out destructively). When $\overline{RAS}$ goes low it clocks in the seven row addresses if the row address setup and hold specifications (t_{ASR} and t_{RAH}) have been met. For the Intel design, if $\overline{CAS}$ is low when $\overline{RAS}$ goes low, a refresh-only operation is initiated; for the MOSTEK design, $\overline{CAS}$ may be low at the $\overline{RAS}$ transition (may in fact stay low for some time after the $\overline{RAS}$ transition since the parameter t_{CRP} is

negative) without prejudicing the new cycle, which may be either a read or write cycle. The Intel ability to perform a 64 cycle refresh hinges on this timing parameter. If $\overline{RAS}$ finds $\overline{CAS}$ low, the most significant row address bit along with all column address bits are ignored. This causes the selection of one row in each 8K half of the array and activation of all 256 sense amplifiers. Refresh may then be performed as though the array were organized as 64 rows by 256 columns. For the MOSTEK part, and for the Intel part if $\overline{RAS}$ finds $\overline{CAS}$ high, refresh must be performed on all 128 rows.

$\overline{CAS}$ is used to clock the column addresses, select one of the 128 active sense amplifiers and transfer its data to the output in a read or read/-write cycle. The high to low transition of $\overline{CAS}$ latches the column addresses if the column address setup and hold specifications (t_{ASC} and t_{CAH}) have been met. To prevent the $\overline{RAS}$ to $\overline{CAS}$ timing from intruding into the access time specification, 16K designs allow $\overline{CAS}$ to go active as soon as the row address hold time has been met and the column address is established on the address inputs. In fact, a negative specification on the column address setup allows switching $\overline{CAS}$ low even during the multiplex time. This negative specification becomes harder to meet as the part becomes faster (higher V_{DD}, lower

temperature) and in any event is one of the more trying parameters to test, since the slowest of the seven address signals (with respect to $\overline{CAS}$) determines the actual value of t_{ASC}. Even though $\overline{CAS}$ can go negative at t_{RAH}, it is not required to do so until somewhat later in the cycle. The latest time for the $\overline{CAS}$ transition with respect to $\overline{RAS}$ is given by the parameter t_{RCD} (max) — note that t_{RCD} (min) equals the row address hold time t_{RAH}. The parameter t_{RCD} (max) is actually a pseudo-limitation, since the only effect of exceeding t_{RCD}(max) is to extend the access time specification (actually the row access) t_{RAC} by the actual value of t_{RCD} minus t_{RCD} (max).

Manufacturers are willing to live with the limitations posed by the negative value for column address setup time in order to provide a more usable part. The amount of time available to the user to switch his multiplexer without artificially delaying $\overline{CAS}$ and thereby degrading access time is simply the value of the maximum allowable $\overline{RAS}$ to $\overline{CAS}$ delay minus the required row address hold time, minus the required column address setup time (Multiplex time = t_{RCD} (max) − t_{RAH} − t_{ASC}). If t_{ASC} is a negative number it adds to rather than decreases the multiplex time. In order to guarantee this specification, the

TIMING DIAGRAM
Figure 2
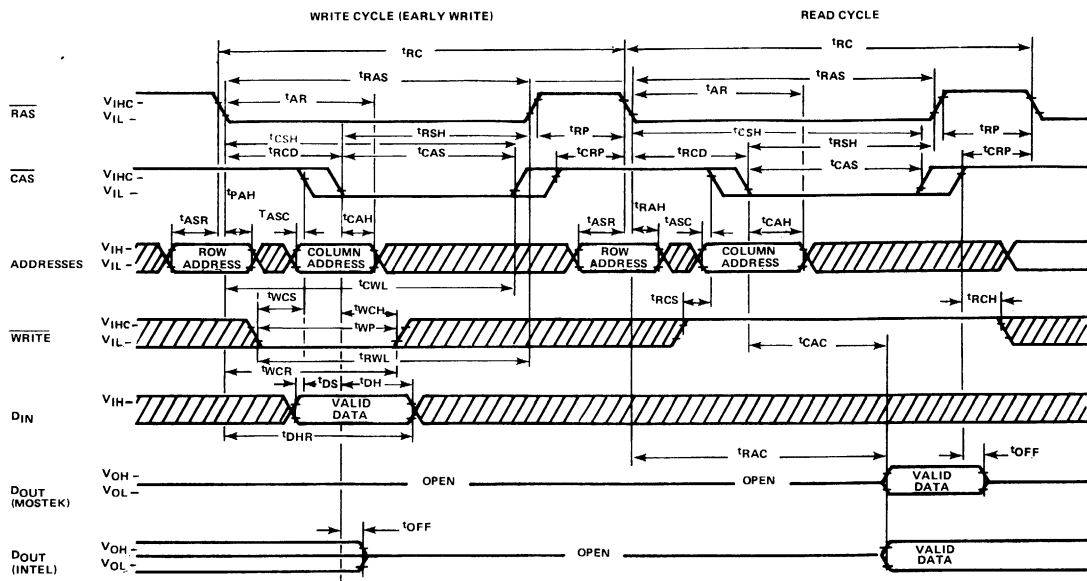
MANUFACTURER	INTEL	MOSTEK
PART NUMBER	2116-2	4116-2
$\overline{RAS}$ ACCESS	200 ns	150 ns
$\overline{CAS}$ ACCESS	125 ns	100 ns
MULTIPLEX TIME	40 ns	40 ns
PRECHARGE TIME	75 ns	100 ns
NUMBER OF REFRESH CYCLES	64 or 128	128
NUMBER OF SENSE AMPS	256	128
DIE AREA	33930 mils^2	22330 mils^2
V_{DD} TOLERANCE	± 10%	± 10%
I_{DD} CURRENT (MAXIMUM)	69 mA	35 mA
POWER DISSIPATION (MAXIMUM)	911 mW	462 mW

manufacturer must place a minimum access time requirement on his testing — that is, parts which are too fast must be rejected, as they will not meet the negative t_{ASC} specification. It is to be expected that as faster 16K designs become available, this negative parameter will become smaller, or possibly will go to zero.

In addition to clocking the column addresses, $\overline{CAS}$ controls the state of the data output. The MOSTEK version open-circuits the output with the low to high transition of $\overline{CAS}$. Intel uses the high to low edge of $\overline{CAS}$ for the same purpose. This allows compatibility with the earlier 4K designs which also used the high to low edge of $\overline{CAS}$. The 4K's have, however, an extra chip select input which can be used in conjunction with $\overline{RAS}$ and $\overline{CAS}$ to deselect the output. With the Intel 16K the only way to guarantee a deselected output is to insert an extra cycle which leaves $\overline{RAS}$ high while clocking $\overline{CAS}$. MOSTEK overcomes this difficulty by unlatching the output with the rising edge of $\overline{CAS}$. This makes the output state independent of the previous cycle and eliminates the need for the "$\overline{CAS}$-only" deselect cycle. If the MOSTEK part is operated in a minimum cycle with $\overline{RAS}$ and $\overline{CAS}$ going high at the same time, the output is only valid for the deselect time (t_{OFF}) plus the amount that the speed of the actual device exceeds the specified speed (if any). To overcome this difficulty, MOSTEK allows the user to leave $\overline{CAS}$ low while $\overline{RAS}$ goes into precharge, thereby

prolonging the output and, incidentally, adding the second major timing difference, that of the state of $\overline{CAS}$ when $\overline{RAS}$ goes low, which was discussed earlier.

CHIP ARCHITECTURE AND CELL LAYOUT

The architecture of the chip can have a direct bearing on the types of tests which should be conducted, as can the layout of the storage cell. Precise details are difficult to acquire as most manufacturers consider them proprietary. Interest in the 16K has prompted the generation of several articles and papers which give some details useful in testing considerations[5][6][7]. Figure 4 gives a gross overview of two chip architectures which nevertheless provide some useful information.

The most obvious difference is in the division of the 16K array into two 8K halves serviced from the middle by 128 sense amplifiers (MOSTEK MK 4116), or into four 4K quadrants, each pair serviced by 128 sense amplifiers (for a total of 256) from their respective centers (Intel 2116). All other factors being equal, in particular assuming approximately equal cell capacitances (reported by MOSTEK and Intel as 0.04 pF and 0.03 pF, respectively), the extra subdivision on the Intel chip means that the digit lines are only half as long as in the MOSTEK chip

TWO 16K RAM CHIP ARCHITECTURES
Figure 4
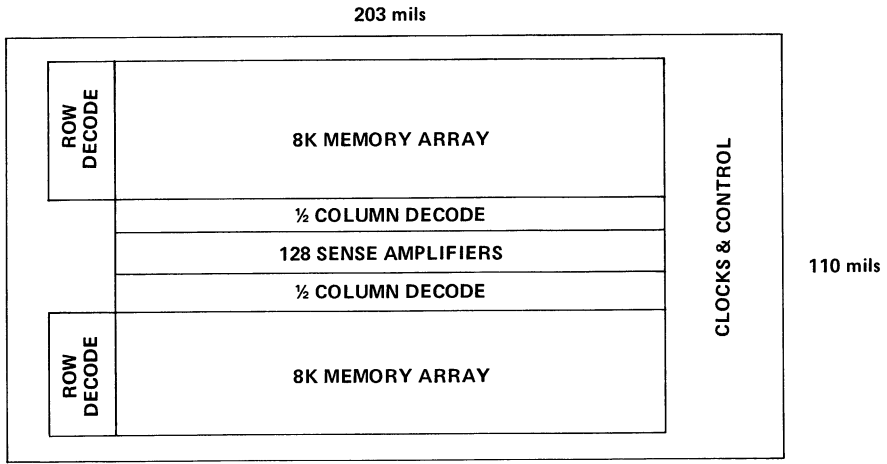
203 mils

ROW DECODE	8K MEMORY ARRAY	CLOCKS & CONTROL
	½ COLUMN DECODE	
	128 SENSE AMPLIFIERS	
	½ COLUMN DECODE	
ROW DECODE	8K MEMORY ARRAY	

110 mils

MOSTEK MK 4116

234 mils

CLOCKS

CLOCKS & CONTROL	ROW DECODE	4K MEMORY ARRAY
		128 SENSE AMPLIFIERS
		4K MEMORY ARRAY
		COLUMN DECODER
		4K MEMORY ARRAY
		128 SENSE AMPLIFIERS
		4K MEMORY ARRAY

145 mils

CLOCKS
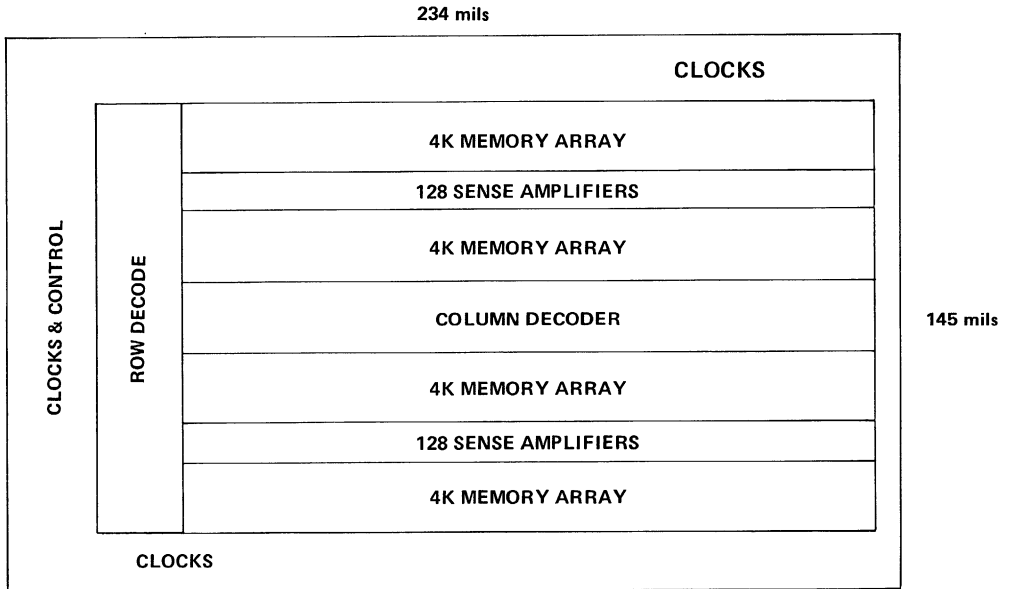
INTEL 2116

SINGLE LEVEL POLYSILICON GATE PROCESS FLOW	DOUBLE-LEVEL POLYSILICON GATE PROCESS FLOW
INITIAL OXIDE/NITRIDE	INITIAL OXIDE/NITRIDE
MASK 1 DEFINES ACTIVE AREA	MASK 1 DEFINES ACTIVE AREA
FIELD OXIDATION	FIELD OXIDATION
GATE OXIDATION	GATE OXIDATION
DEPOSIT POLYSILICON	DEPOSIT POLYSILICON
	MASK 2 DEFINES POLY I
	INSULATING OXIDE
	DEPOSIT POLYSILICON
MASK 2 DEFINES POLY	MASK 3 DEFINES POLY II
PHOSPHOROUS DIFFUSION	PHOSPHOROUS DIFFUSION
INSULATING OXIDE	INSULATING OXIDE
MASKS 3 & 4 DEFINE CONTACTS	MASKS 4 & 5 DEFINE CONTACTS
ALUMINUM	ALUMINUM
MASK 5 DEFINES METALLIZATION	MASK 6 DEFINES METALLIZATION
TOP GLASS	TOP GLASS
MASK 6 OPENS PAD AREAS	MASK 7 OPENS PAD AREAS

and, since signal varies with the ratio of digit line to cell capacitance, that the Intel sense amplifier should have twice the available signal as does the MOSTEK version. Since the digit line halves (or quarters) are precharged during the $\overline{RAS}$ inactive time (t_{RP}) to (hopefully) equal voltage, and since any difference in the starting values of the digit line voltages subtract directly from the available signal, MOSTEK may be rather more concerned about the precharge time than Intel, and, in fact, the value of t_{RP} for the MOSTEK 150 nanosecond part is specified to be 100 nanoseconds, while the t_{RP} value for the Intel 200 nanosecond part is actually smaller (75 nanoseconds).

On the other hand, the substrate (back of the chip) may be considered a noise collector which couples all areas of the circuit together. Since the clocks and decoders, prime noise generators, are strung along the short dimension of both chips, a reasonable estimate of the substrate noise would be that it peaks in the center of the short axis, falling to zero toward the edges. The sense amplifiers in the MOSTEK design are located in the center and would presumably see a balanced noise coupling onto the digit lines, while the Intel sense amplifiers, located at the one quarter and three quarter points, might see more noise coupled onto the digit line quarters near the chip center than on the outer digit line quarters.

Since the sense amplifier naturally inverts one of the digit lines, it would be convenient if the test equipment made provision for exclusive - OR'ing either the most significant row address bit (for the MOSTEK design) or the second most significant row address bit (for the Intel design) with data into and out of the device under test such that a programmed input of all "ones" would be stored by the chip as all "highs". This facility would greatly simplify refresh and disturb tests. Of course, the sense amplifier inversion is logically removed by the chip itself so that it is transparent to the user, but the capability would be extremely useful in a test environment.

Both MOSTEK and Intel have resorted to the double-level polysilicon gate process to reduce the area of the memory cell. The process is basically an extension of the single-level polysilicon gate process common in the semi-conductor industry for years. Figure 5 is a basic comparison of the POLY II™ process as implemented by MOSTEK, and the standard single level poly process. There is only one additional mask required, plus one extra deposition and one extra oxidation step. Figure 6 depicts a cross-section through the cell and the cell schematic. The transfer gate (POLY II transistor) is used only in the cell; the threshold voltage for this transitor may be adjusted independently of the threshold voltage of the peripheral transistors. The ratio of digit line to cell capacitance is about 20:1 for the MOSTEK design and approximately 13:1 for the Intel.

MK4116 CELL AND CROSS–SECTION
Figure 6

POLY I CAPACITOR — POLY II TRANSISTOR — DIFFUSED BIT LINE

METAL WORD LINE — POLY II
POLY I
BIT LINE
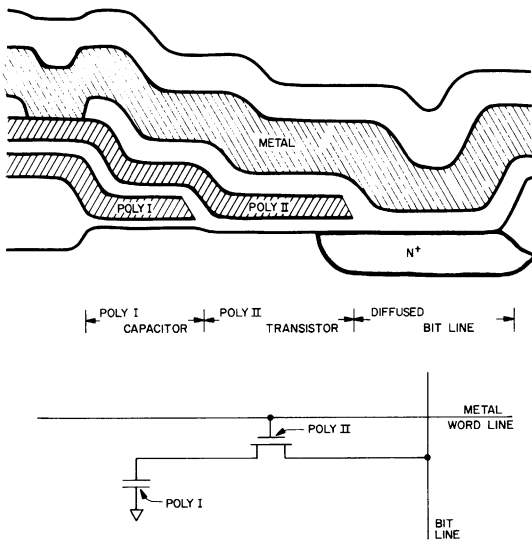
Figure 7 shows the cell layout which with minor variations, is used by both MOSTEK and Intel. The adjacent cells are located either on the same row or on rows separated by one word line and are always on adjacent columns. The first level polysilicon sheet which forms the common capacitor plate for all cells also forms the gate of an MOS field transistor which links neighboring cells. It may therefore be necessary to check for cell to cell interactions due to less than ideal field threshold voltage of this device. Also, the channel length of the transfer gate is determined by the relative alignment of first poly to second. If the misalignment is too great, the threshold voltage of the transfer gate may be reduced due to short channel effects, making it advisable to check carefully for data loss due to the inability to keep deselected cells from leaking through the transfer gate to the digit line.

TEST PATTERNS

The problem of developing test patterns to test memories for various pattern sensitivities has been extensively reported in the literature [8][9][10]. More recently, the emphasis has shifted towards analysis of the design and adoption of test sequences which exploit possible weaknesses [11]. This approach is necessary if test times for 16K RAM's are to be kept within practical bounds. The following information, although believed to be general, applies specifically to the MOSTEK design.

The 16K RAM is basically a synchronous machine built around a rectangular memory array, the coordinates of which are "rows" and "columns". The synchronous machine provides the timing control for the input latches, row decoder, sense amplifier, column decoder, write circuitry, and output latch. In contrast to earlier, asynchronous RAM's, the 16K nearly always fails digitally. That is, if a problem exists with the input latches, the wrong output will be generated (but not a "late" output which is correct but delayed by, for example, poor input levels). There is no "worst-case" pattern for access time since access time is controlled by the internal clock generators. This greatly simplifies the testing of gross functionality, which must only assure cell uniqueness and output validity over the specified timing and power supply ranges.

On the other hand, the memory array and sense amplifiers must still be checked for pattern sensitivities. Considering the signal detection capabilities of the sense amplifier, and its precharge requirements, a probable "worst-case" pattern for a sense amplifier is a single bit of DATA in a field of $\overline{\text{DATA}}$. If such a pattern is run in a "row fast" mode, each sense amplifier will be required to perform some number of reads of $\overline{\text{DATA}}$, a single detection of DATA, and complete the scan reading $\overline{\text{DATA}}$. If the DATA bit occupies, at some time, each of the locations along the digit line, the ability of the sense amplifier to pick signal out of noise and to remove completely any influence of the preceding cycles on the present cycle will have been checked. Note that this pattern would require only as many scans as there are bits per

sense amplifier, and that all columns can be checked simultaneously.

MK4116 CELL LAYOUT
Figure 7
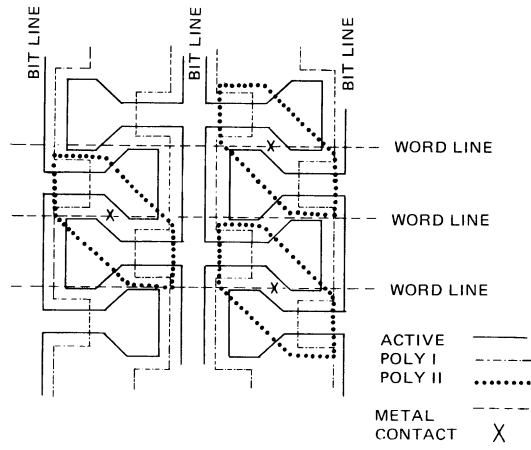
Considering the row select function, noise coupling considerations indicate that here too a worst case pattern might be either a single DATA bit in a field of $\overline{\text{DATA}}$, or, perhaps, a solid field. Here also the word "field" has a restricted meaning, applying only to all cells connected to a single row select line.

Several patterns check for the above failure modes efficiently; one of particular interest is the $2N^{3/2}$ "Moving Diagonal" pattern, which requires 128 write-read scans through the entire array. On the first scan, all bits are written to $\overline{\text{DATA}}$ with the exception of the 128 bits along the major diagonal which are written to $\overline{\text{DATA}}$. The read scan verifies the correct operation of the array under these conditions. On each succeeding scan, the position of the diagonal of DATA is shifted until, on the 128 scan, it has occupied every possible position in the array. Each cell has once been the only DATA cell in a row and column of $\overline{\text{DATA}}$. This pattern has proven to be quite effective in screening the 16K RAM.

Refresh tests can be separated into two categories: still and dynamic. Still refresh tests are per-formed by writing all locations, pausing for the refresh interval with $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ inactive (high), and reading all cells. The inactive pause allows the cells to leak low but also allows internal nodes which are bootstrapped above V_{DD} by the trailing edge of $\overline{\text{RAS}}$ or $\overline{\text{CAS}}$ to decay so that both the cells and the dynamic periphery are tested. Unfortunately, such a test normally is not worst case for the cell, as noise generated during active cycles can contribute to the loss of data in the cell. The dynamic refresh tests write data into some subset of cell (normally half of the cells) and, during the refresh interval, perform either read or write cycles on the cells not being tested, the intent being to couple charge-degrading noise onto the unaccessed test cells. Both tests are necessary to completely guarantee functionality of the 16K.

During the active portion of a cycle, 127 of the 128 rows are not selected, and must remain at OFF to prevent partial selection of a transfer gate. A test with maximum active time provides greatest opportunity for such partial selection to occur. This test might perform a write scan with minimum precharge times (t_{RP}) and maximum active time (t_{RAS}), followed by a read-modify-write scan under the same basic timing conditions, followed by a read scan to verify the "modify-write" operation. This important test is often overlooked but is in fact worst-case for many of the internal circuits.

For users desiring a basic but adequate test sequence, the above patterns provide a good starting point. Figure 8 summarizes such a sequence which should provide a reasonable degree of confidence in any RAM which passed. Special timing modes and certain timing parameters would be left unchecked, but could be easily added if desired. This test sequence requires ($28N + 4N^{3/2}$) cycles, of which all but 8N may be at the fastest allowable cycle rate. The 8N are at the slowest allowable cycle rate (maximum cycle length). If the cycle times are 375 nanoseconds and 10 microseconds, respectively, this sequence would execute in just over 4.5 seconds, exclusive of tester overhead and power supply settling times.

POSSIBLE MINIMUM TEST SEQUENCE FOR 16K RAM
Figure 8

TEST DESCRIPTION	DATA PATTERN	FUNCTION	POWER SUPPLIES V_{DD}	V_{BB}	CYCLE COUNT
MAXIMUM CYCLE	DIAGONAL	FUNCTIONALITY	13.2	−4.5	2N (t cyc = 10 μS)
	$\overline{DIAGONAL}$		13.2	−5.5	2N (t cyc = 10 μS)
	DIAGONAL		10.8	−5.5	2N (t cyc = 10 μS)
	$\overline{DIAGONAL}$		10.8	−4.5	2N (t cyc = 10 μS)
LOAD READ	PARITY and $\overline{PARITY}$		10.8	−5.5	2N
			10.8	−4.5	2N
			13.2	−5.5	2N
			13.2	−4.5	2N
LOAD READ	CHECKERBOARD and $\overline{CHECKERBOARD}$	BIT INTERACTIONS	10.8	−5.5	2N
			10.8	−4.5	2N
			13.2	−5.5	2N
			13.2	−4.5	2N
MOVING DIAGONAL	DIAGONAL	FUNCTIONALITY	10.8	−5.5	$2N^{3/2}$
			13.2	−4.5	$2N^{3/2}$
DYNAMIC REFRESH	ALTERNATE ROWS	DATA RETENTION	10.8	−5.5	1N + 2 mS
DYNAMIC REFRESH	$\overline{ALTERNATE ROWS}$	DATA RETENTION	10.8	−5.5	1N + 2 mS
STILL REFRESH	ALL HIGHS	DATA RETENTION	10.8	−5.5	2N + 2 mS

REFERENCES

MOSTEK 1977 MEMORY PRODUCTS CATALOG, pages VII-1 through VII-15.

Battett, C.R., and Smith, R.C. "Failure Modes and Reliability of Dynamic RAMS", COMPCON Spring 1977 Technical Digest, March 1977, pp. 179-182.

Peck, D.S. and Zierdt, C.R., "The Reliability of Semiconductor Devices in the Bell System", Proceedings of the IEEE, Vol. 62, No. 2, February 1974, pp. 185-211.

Brown, J.R. Jr. "Timing Pecularities of the 16 Pin Multiplexed Address RAM", Burroughs Technical Memorandum, November 1976.

Ahlquist, C.N., et al, "A 16384 — Bit Dynamic RAM", IEEE Journal of Solid-State Circuits, Vol. SC-11, No. 5, October 1976, pp. 570-573.

Schroeder, P.R., and Proebsting, R.J., "A 16K x 1 Bit Dynamic RAM, ISSCC Digest of Technical Papers, February 1977, pp. 12-13.

Kuo, C.K., et al, "16-K RAM Built with Proven Process May Offer High Start-Up Reliability", Electronics, May 13, 1976, pp. 83-86.

Huston, R.E., "Testing Semiconductor Memories", 1973 Symposium on Semiconductor Memory Testing Digest of Papers, October 1973, pp. 27-62;

Feldmann, D., and Healy, J.E., "Probleme bei der Freigabe - und Wareneingangspruefung von Halbleiterspeichern", Elektro-Anzeiger, No. 18, September 24, 1976.

Cocking, J., "RAM Test Patterns and Test Strategy", 1975 Semiconductor Test Symposium, Digest of Papers, October 1975, pp. 1-8.

Foss, R.C., and Harlan, R., "MOS Dynamic RAM—Design for Testability", 1976 Semiconductor Test Symposium, Digest of Papers, October 1976, pp. 9-12

MOSTEK®

OPTIMIZED TESTING OF 16K RAMS
Testing

By ROBERT W. OWEN

The new generation of 16K dynamic MOS memories places a much greater burden on the test engineer than did the earlier 1K and 4K designs. The size of the memory means that generalized test sequences which test these devices as black boxes will be far too expensive in terms of test time per device. Even though the semiconductor industry appears to have standardized on one compatible pin-out with the major controversies being decided in favor of 128 — cycle refresh and output latch controlled by the column address strobe as in the MOSTEK MK 4116, there are pitfalls for the user who does not appreciate the fact that vendor design and testing differences will result in devices with different characteristics. Test sequences which do not comprehend these differences will not be successful in eliminating marginal devices. Therefore, the test engineer must acquire an in-depth knowledge of each vendor's device and the test sequences utilized must reflect this knowledge.

The following table illustrates graphically the test time penalties paid in moving from 4K to 16K:

	Test times for various test patterns (375 ns cycle)	
	N=4096	N=16384
2N (Load-Read)	3 mS	12 mS
$2N^{3/2}$ (Moving pattern, row or column ping-pong)	197 mS	1. 6 Sec
$2N^2$ (Ping-pong) GALPAT)	12. 6 Sec	201 Sec

When testing the 4K RAM, the test engineer could treat the device as a black box, generate all address transitions by using N^2 patterns, and hope for the best. Using such an approach on the 16K would result in a tester throughput of fewer than 400 parts per day.

TEST TEMPERATURE

The single most important decision to be made concerning dynamic RAM testing is test temperature. MOS devices have three basic parameters which are functions of temperature: threshold voltage, carrier mobility, and leakage currents. For N-channel silicon gate processes, threshold voltage is typically 200 millivolts lower at 100°C than at 0°C. Carrier mobility, which relates to transistor gain and therefore to circuit speed, is about 25% lower at 100°C than at 0°C. The effects of these two variables, once charac-

terized for a particular device, may be easily included by adjusting parameters such as input and output levels for the temperature range variations expected. A third variable, leakage current, is more dramatic in its effect on the device.

The refresh time of any dynamic MOS Memory may be expressed by

$$t_{REF}=Ae^{-BT}$$

where   T is junction temperature in °C
         B is a variable relating the magnitude of the generation — recombination current to the junction temperature (units of 1/°C)

and   A is a scaling constant reflecting such variables as junction area, sense amplifier design, bulk defect density.

Typical values for the variable B range from 0.053/°C to 0.060/°C implying a temperature behavior in which refresh time is halved for every 11.6°C to 13.1°C increase in junction temperature.

Testing should be conducted at elevated temperatures in order that this large variation may be tested without having to extrapolate from some non-worst-case temperature. (Since mobility is also worst-case at elevated temperature, most timing parameters are also worst-case at elevated temperatures and need not be guardbanded.)

Most 16K RAMS are specified over the temperature range 0°C to 70°C ambient. The junction temperature T_J depends, however, on the power dissipation (P_D) of the device by the equation

$$T_J=T_A + P_D\theta_{JAX}$$

Where θ_{JAX} is the thermal impedance between the device junction and system ambient. Figure 1 graphs this equation for θ_{JAX}=70°C per watt (standard 16 pin ceramic dual in line package).

If the device junction temperature is stabilized by using a long warm-up cycle prior to the first test, the proper test temperature is the system ambient temperature. If the test is short enough that the junction temperature does not rise appreciably under test, the proper test temperature is the junction temperature given in Figure 1. For example, a device which dissipates 430 mW must be tested at T_J=100°C in order to guarantee functionality at T_A=70°C.

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JUNCTION TEMPERATURE VS. POWER DISSIPATION

Figure 1

JUNCTION TEMPERATURE VS POWER DISSIPATION

$T_A = 70\,C$
$\theta\,JAX = 70\,C/WATT$

(Y-axis) T_J, JUNCTION TEMPERATURE (°C): 70, 80, 90, 100, 110, 120

(X-axis) P_D POWER DISSIPATION (MILLIWATTS): 100, 200, 300, 400, 500, 600, 700
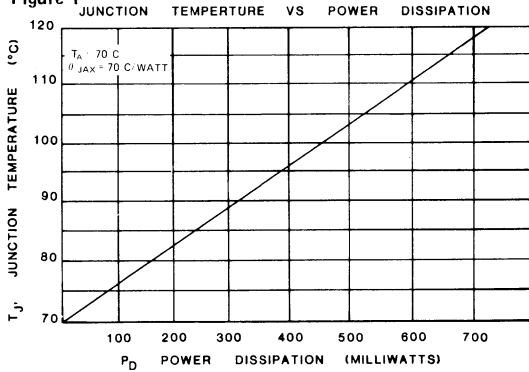
THE MOSTEK MK 4116

The block diagram of the MOSTEK MK 4116 (Figure 2) may be examined for testing implications. Note that the address input buffers are shared while the row and column decoders are independent. An addressing scheme which provides the maximum possible number of bit reversals per cycle will check for possible interactions due to the previous address. This can be accomplished efficiently in a basic load-read (2N) test by using one of the addressing schemes variously referred to as "address complement", "address select", or "MASEST".

Note further that the data out buffer is timed exclusively by an internal clock generator driven by $\overline{CAS}$. There is no reason, then, to search for some test sequence or data pattern which is "worst-case" for the access time. Access time is absolutely determined by clock delays internal to the circuit and is only influenced by influencing these delays. Access time, along with most other timing parameters is worst-case at low V_{DD} (+10.8 volts). V_{BB} has almost no influence on access time.

Still referring to Figure 2, note that there are two 8K sub-arrays split by the sense-refresh amplifiers in the middle and having "dummy cells" at each side. These establish a voltage reference for the balanced sense amplifiers. One of the array halves, therefore, inverts data and will store an input "one" as a <u>low</u> level in the storage cell (a second inversion is performed by the output circuitry so that this internal inversion is not seen at the device terminals). This inversion must be taken into account when performing a refresh test.

BLOCK DIAGRAM MK4116

Figure 2

The layout of the storage cell in the MK 4116 is shown in Figure 3. This is a conventional one-transistor dynamic storage cell, although implemented by using MOSTEK's double-level polysilicon (Poly II^{TM}) process. The row (word) select lines are metal, eliminating concern over propagation delays down the long 80 mil word lines. Data transfer to and from the cell is through the diffused column (digit) lines. The top plate of the storage capacitor is V_{DD} (first level of polysilicon) which allows charge to be stored in the depleted region beneath this level. Metal word lines contact the second poly level which forms the gate of the transfer device isolating the storage cell from the digit line. The cell is relatively insensitive to variations in the doping level of both first and second poly. In fact, performance of the cell is primarily influenced by junction depth, oxide thickness, and mask geometry, all parameters which tend to remain constant.

MK4116 CELL LAYOUT
Figure 3


```
                              WORD LINE

                              WORD LINE

                              WORD LINE

DIGIT LINE   DIGIT LINE   DIGIT LINE

                         ACTIVE _____
                         POLY I _ . _ . _
                         POLY II . . . . . . .
                         METAL _ _ _ _ _
                         CONTACT  X
```
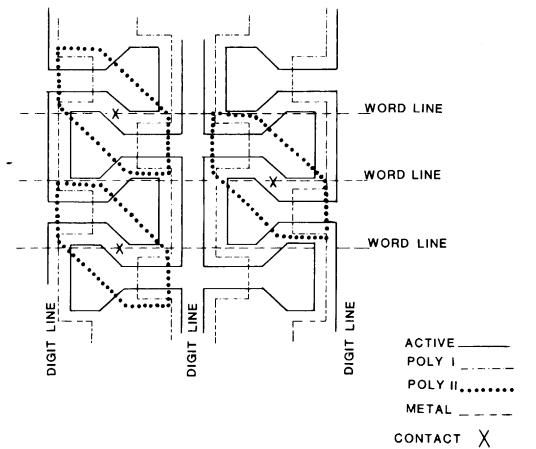
Figure 4 relates the cell, sense amplifier, and dummy cells. This figure provides a measure of topological information in addition to the electrical schematic. Capacitor-to-capacitor adjacencies in Figure 4 were carefully drawn to reflect the physical relationship of the actual layout.

MK4116 CELL, DUMMY CELL, SENSE AMPLIFIER
Figure 4


```
            DIGIT N + 1      DIGIT N + 1

            DIGIT N          DIGIT N

WORD M + 1   WORD M                    DUMMY
                                       WORD

            LATCH   VDD
```
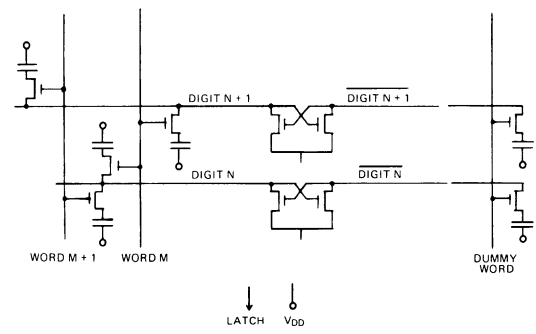
Because of the cell layout, tests to eliminate bit-to-bit sensitivities need to be considered carefully. The conventional "checkboard" pattern will result in an alternating bit-by-bit data pattern, as usual, but a "vertical bar" pattern consisting of alternate columns of highs and lows will accomplish the same result.

Two neighboring bits which might influence one another may be located on the same row or be separated by one row, but will not be on adjacent rows. Such bits must be on adjacent columns. There is also a topological mapping in the decoder layout which must be considered if rows and columns are to be accessed in a sequential manner.

SENSE AMPLIFIER MARGIN

Sense amp operation is straightforward:

1. Digit and $\overline{Digit}$ lines are precharged high, word lines and the dummy cell are precharged low, and LATCH is precharged high.

2. The selected word line turns on to V_{DD} along with the dummy word line accessing the dummy cells in the array half which does not contain the accessed cells. The accessed cells are thus connected via the transfer gates to the digit and $\overline{digit}$ lines. Charge redistribution between the cells and digit lines causes a voltage drop on the digit line of zero to 0.3 volts if the cell contained a high level (depending on the amount of decay in the cell since the last access), or of about 0.5 volts if the cell was initially low. The dummy cell pulls the $\overline{digit}$ line down by 0.4 volts.

3. Latch is driven to ground allowing the balanced sense amplifier to discharge the digit or $\overline{digit}$ line, whichever started at the lower voltage.

Accessing a stored low level requires that the digit line be discharged by the cell, whereas accessing a stored high level is accomplished whenever the digit line is relatively undisturbed.

Design and layout of the storage array and sense amplifier is complicated by the presence on critical nodes of noise which adds to or subtracts from signal voltages, causing a data-dependent reduction in overall margin. The data pattern which creates worst-case coupling and smallest margins in the MK 4116 is a solid field of discharged cells.

Insufficient precharge of the sense amplifier, which can arise from several distinct types of processing defects, causes the result of the current cycle to depend upon the preceding cycle. One data pattern which efficiently checks for such failure modes is the "major diagonal" or its extension, the $2N^{3/2}$ "moving diagonal". Beginning with a major diagonal of ones in a field of zeroes, each successive pass through the memory moves the diagonal up one

position such that in 128 passes it has occupied every possible position. Each bit has then been the only high in a row and column of low bits.

REFRESH TESTING

Refresh tests may be roughly divided into two subgroups — active and static. Active refresh indicates that the device is continuously operated for the period during which the unaddressed row or rows is allowed to decay.

Such a test provides an opportunity for increased cell leakage, either by sub-threshold conduction through transfer gates whose word line has been driven slightly positive due to noise coupling, by cell to cell leakage if the disturbing cycles are conducted on adjacent cells, or by charge carriers injected into the substrate by some nearby node. On the other hand, a static refresh test in which both $\overline{RAS}$ and $\overline{CAS}$ remain inactive for the entire refresh interval allows internally precharged nodes to decay. Such a test insures that, in addition to data being retained for the refresh interval, the peripheral circuits are also functioning after the pause.

If the refresh tests are being conducted at elevated temperatures with a stable junction temperature, the worst voltage corner for refresh is low V_{DD} (10.8 volts) and high V_{BB} (−5.5 volts). If the devices are allowed to self-heat prior to testing, then the high V_{DD} (13.2 volt) corner provides maximum power dissipation, maximum junction temperature, and minimum refresh time. In any event, high V_{BB} results in higher leakage current and shorter refresh times.

VOLTAGE BUMP

For any dynamic RAM whose storage capacitor plate is returned to V_{DD}, a change in V_{DD} between accesses will couple onto the storage node. For example suppose that a low level is written with V_{DD} low and that the storage node is in fact discharged to zero volts. If before the next access to this cell the V_{DD} level increases, some percentage (typically about 80%) of this increase will couple onto the storage node. The sense amplifier design must allow proper recognition of this level as low and not falsely read this out as a high.

DECODER AND I/O

In addition to functional tests to check for the failure modes just described it is, of course, necessary to verify proper operation of the decoders and the input and output of data. Here no special techniques are required beyond those widely utilized in industry 1K and 4K RAM testing since this functionality may be proven with simple 2N tests. In fact, testing of the MK 4116 with its data output latch controlled exclusively by $\overline{CAS}$ is much simpler since there is no influence on the current cycle by a previous cycle as is the case for latched output designs. Parametric tests verifying input and output leakage specifications are also identical to that required by 4K devices, although here again the control of data out by $\overline{CAS}$ simplifies the output leakage measurement.

SUMMARY

Some of the basic failure mechanisms of the MK 4116 have been explained, along with suggested tests which efficiently isolate each mechanism. The only other required tests check the remaining data sheet timing parameters at the specified voltage limits to verify mimimum and maximum values, and are simple load-read patterns. It should be possible to implement a highly effective device screen which takes no longer than 20 seconds per device and still provides high confidence that defective devices will be eliminated.

INPUT PROTECTION CIRCUIT

All signal inputs to the MK 4116 have the input protection circuit shown in Figure 1 integrated onto the chip. The purpose of the circuit is to protect the device from damage caused by static voltages that may be encountered during shipping and handling.

INPUT PROTECTIVE CIRCUITRY
Figure 1
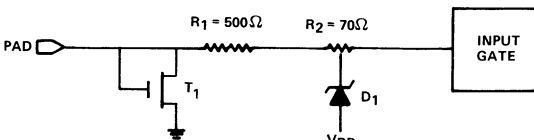
T_1 is a metal gate field transistor having a threshold voltage of approximately 12 volts, and D_1 is a $N^+ - P$ diode whose breakdown is lowered by the presence of a gate electrode at substrate (V_{BB}) potential on the periphery of the diode.

Conventional testing of the electrostatic protection devices using a 50–100 picofarad capacitor charged to some variable potential in the range of 500 to 1000 volts and discharged into the input through a 1K-2K ohm resistor have been performed by MOSTEK and demonstrate that the protection is adequate. Customer tests of the protective devices should be limited to 50 picofarads, 500 volts discharged through a 1K ohm resistor. Exposure to conditions exceeding these may affect reliability of the device.

All power supply inputs (V_{DD}, V_{CC}, V_{SS}) are essentially large area N^+ diffusions to the P-type substrate (V_{BB}).

The functional circuitry for the clock inputs ($\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$) looks like:

CLOCK INPUT CIRCUIT
Figure 2
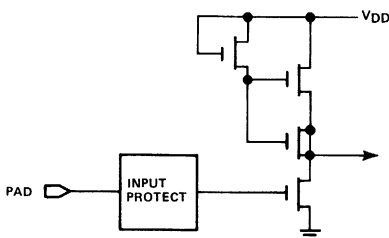
which is a fairly conventional MOS inverter. When determining the input capacitance of any such circuit, the power supplies should be at normal operational levels and, if an AC signal is supplied at the input, the amplitude of this signal should be normal (0–3 volts) to reduce the voltage gain and therefore the Miller capacitance of the input stage.

The input stage for address and data input signals is:

ADDRESS AND DATA INPUTS
Figure 3
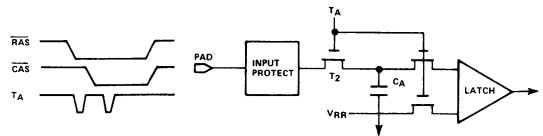
where T_A is an internally generated clock and V_{RR} an internally generated reference voltage (approximately one-eighth of V_{DD}). T_A isolates the storage capacitor C_A from the external signal as soon as possible after $\overline{RAS}$ or $\overline{CAS}$, allowing the applied signal to change during the operation of the internal latch. Note that, if the external signal switches to a level more than one threshold voltage below ground (or has negative undershoot going more than one threshold below ground) the transistor T_2 may turn back on at the improper moment, allowing the discharge of capacitor C_A and resulting in improper operation of the input latch. This is the reason that the V_{IL} of all signals is limited to −1.0 volts in the negative direction.

The data output circuitry is given in Figure 4.

DATA OUTPUT CIRCUITRY
Figure 4

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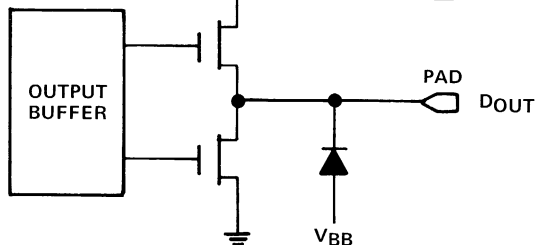
In general, extreme care must be exercised when making measurements on the D_{OUT} that both the transistors of the output stage are turned "OFF". It is sufficient on the MK 4116 (although not on the earlier MK 4027 which has a latched output) to have V_{DD} and V_{BB} within the normal operating range and the $\overline{CAS}$ level above 2.7 volts (V_{IHC}). Under these conditions, both transistors will be held "OFF" and leakage measurements may be made on the output pin.

ADDRESSING CONSIDERATIONS WHEN TESTING THE MK4116

By ROBERT W. OWEN

Testing

Customer engineers responsible for evaluation and incoming testing of Random Access Memories normally require a description of the internal topology of a device in order to check for "worst case" patterns or to optimize test sequences. This paper will provide such information for the MK 4116 16-kilobit dynamic RAM.

Due to the complexity of the part, this information is not quite so straightforward as in earlier RAMs produced by MOSTEK. It is necessary that the test engineer keep in mind four separate topological alterations:

1. Address Topology

   The labels for address pins as given on the MK 4116 data sheet were selected for marketing convenience and do not reflect the internal least significant bit (LSB) to most significant bit (MSB) layout. It is necessary to relabel the seven address lines according to Figure 6.

   All references in this paper to a particular address are understood to refer to the actual MK 4116 address, not the data sheet address.

2. Decode Topology

   Efficient layout of the row and column decoders results in a scramble of the address inputs which must be observed if, for example, it is required that rows and columns be accessed in a "nearest neighbor" manner. The logic necessary to descramble this decode topology is given in Figure 7. Note carefully that Figure 7 gives addresses in terms of their row (R_n) and column (C_n) components. The multiplexing of R_n and C_n such that R_n is valid at $\overline{RAS}$ time and C_n is valid at $\overline{CAS}$ time produces the address input A_n.

3. Data Polarity

   Utilization of a balanced sense amp located between rows 63_{10} and 64_{10} of the matrix requires that one of the two halves of the matrix invert data (this inversion is comprehended by internal circuitry so that it is

transparent to the user). If it is necessary, for example, to write all 16 kilobits to a charged state, the data polarity of Figure 8 must be observed.

4. Bit Topology

   Maximum utilization of silicon real estate required that the matrix layout be done as indicated by Figure 9.

   Note that instead of "conventional" layouts which have all cells on the same side of the bit line, the cells of the MK 4116 are laid out in pairs, one on each side of the bit line. Also, in contrast to "conventional" layouts having the transfer gates in one row, the transfer gates associated with one word line in the MK 4116 occur in pairs, one above and one below the (metal) word line. This layout has implications for the test engineer. For example, a data pattern which writes alternate columns to the same data state (called by MOSTEK "VBAR") will perform a check for bit-to-bit shorts as well as the conventional "checkerboard" pattern. The addressing sequences required to perform a "nearest neighbor disturb" are therefore a function of both the decode and the bit topology.

   For the sake of completeness, although not strictly necessary, Figure 10 relates the location of inputs and the individual bits to the actual chip.

TRANSFORMATION FROM DATA SHEET PIN NAMES TO MK4116 INTERNAL PIN NAMES
Figure 6

PIN NUMBER	MK 4116 DATA SHEET	MK 4116 ACTUAL
13	A_6	A_0
10	A_5	A_1
11	A_4	A_2
12	A_3	A_3
7	A_1	A_4
6	A_2	A_5
5	A_0	A_6

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EXTERNAL ADDRESS TRANSFORMATION REQUIRED TO DESCRAMBLE MK4116 INTERNAL DE—CODER (MULTIPLEXER NOT SHOWN)

Figure 7
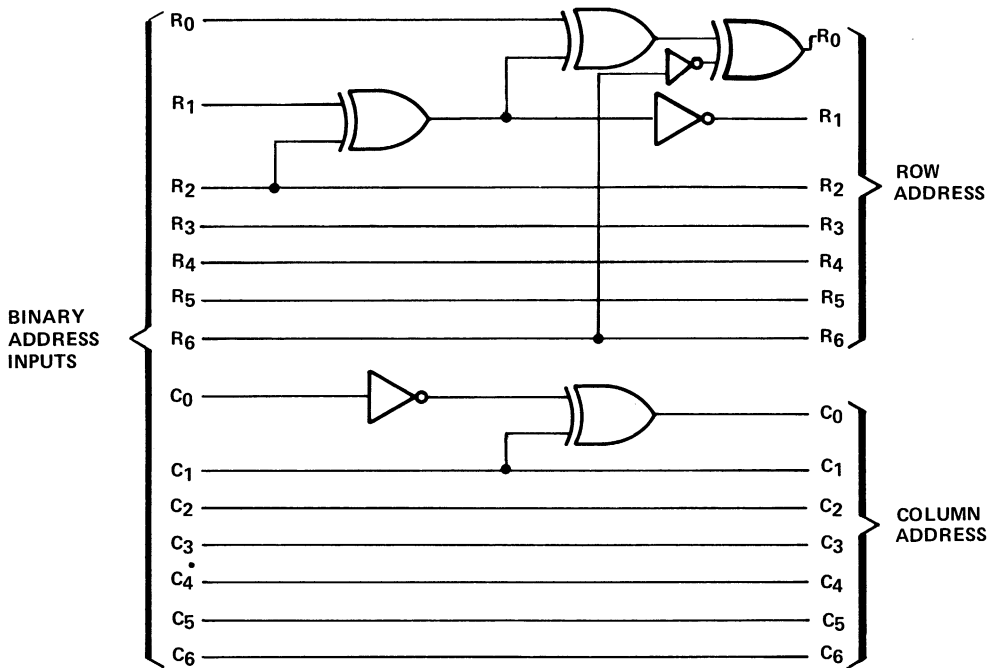
NOTE: The logic symbols
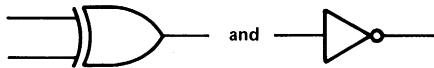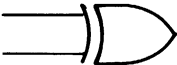
are used solely to indicate the logic function "Exclusive — OR" and "NOT", respectively;
The above figure is not a suggested implementation of logic.

EXTERNAL TRANSFORMATION NECESSARY TO COUNTERACT THE INTERNAL INVERSION OF DATA WITHIN THE MK4116

Figure 8

(ROW ADDRESS MSB)

NOTE: The same transformation will be required on the D_{OUT} of the MK 4116. This data inversion is transparent to the user and need be considered only in testing of the MK 4116.

NOTE: The logic symbol   is used solely to indicate the logic function "Exclusive — OR". The above figure is not a suggested implementation of logic.

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SENSE
AMPS

C4   C3   C2   C1   C0

R12 C4	R13 C2	R12 C2	R13 C0	R12 C0
R12 C3	R11 C3	R12 C1	R11 C1	
R10 C4	R11 C2	R10 C2	R11 C0	R10 C0
R10 C3	R9 C3	R10 C1	R9 C1	
R8 C4	R9 C2	R8 C2	R9 C0	R8 C0
R8 C3	R7 C3	R8 C1	R7 C1	
R6 C4	R7 C2	R6 C2	R7 C0	R6 C0
R6 C3	R5 C3	R6 C1	R5 C1	
R4 C4	R5 C2	R4 C2	R5 C0	R4 C0
R4 C3	R3 C3	R4 C1	R3 C1	
R2 C4	R3 C2	R2 C2	R3 C0	R2 C0
R2 C3	R1 C3	R2 C1	R1 C1	
R0 C4	R1 C2	R0 C2	R1 C0	R0 C0
R0 C3		R0 C1		
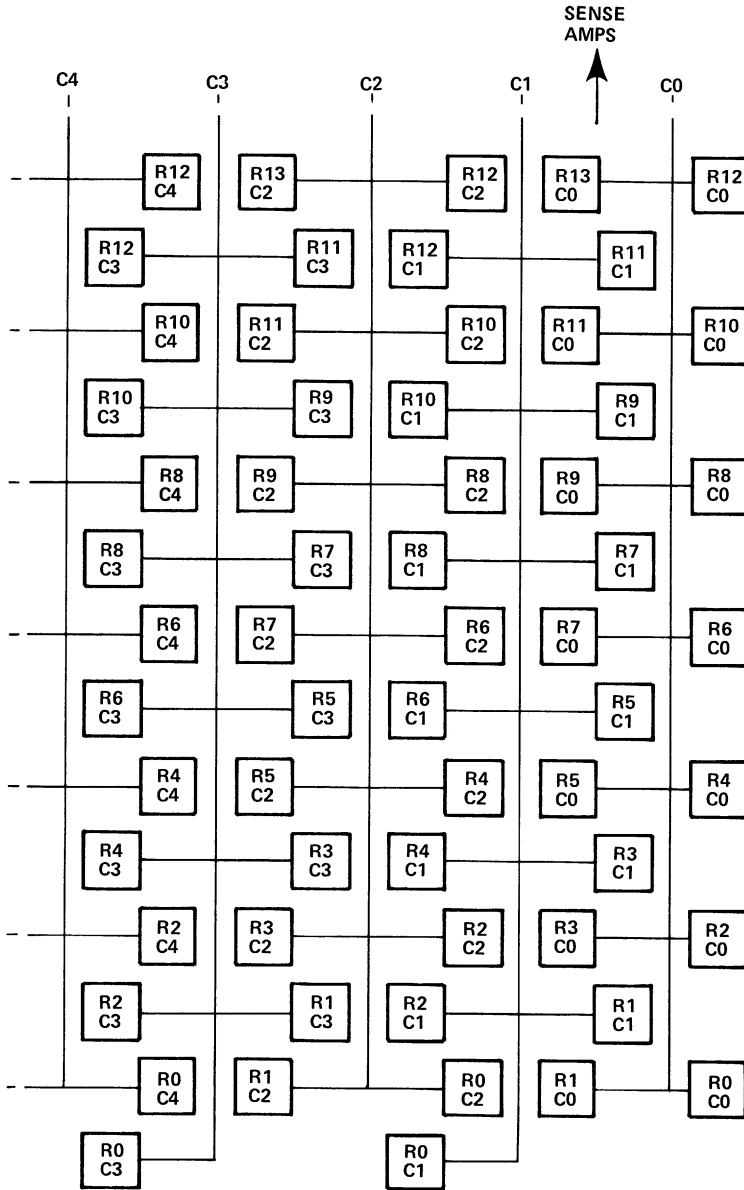
The area represented here is physically located in the lower right hand corner of the bottom half array. (See Figure 10)
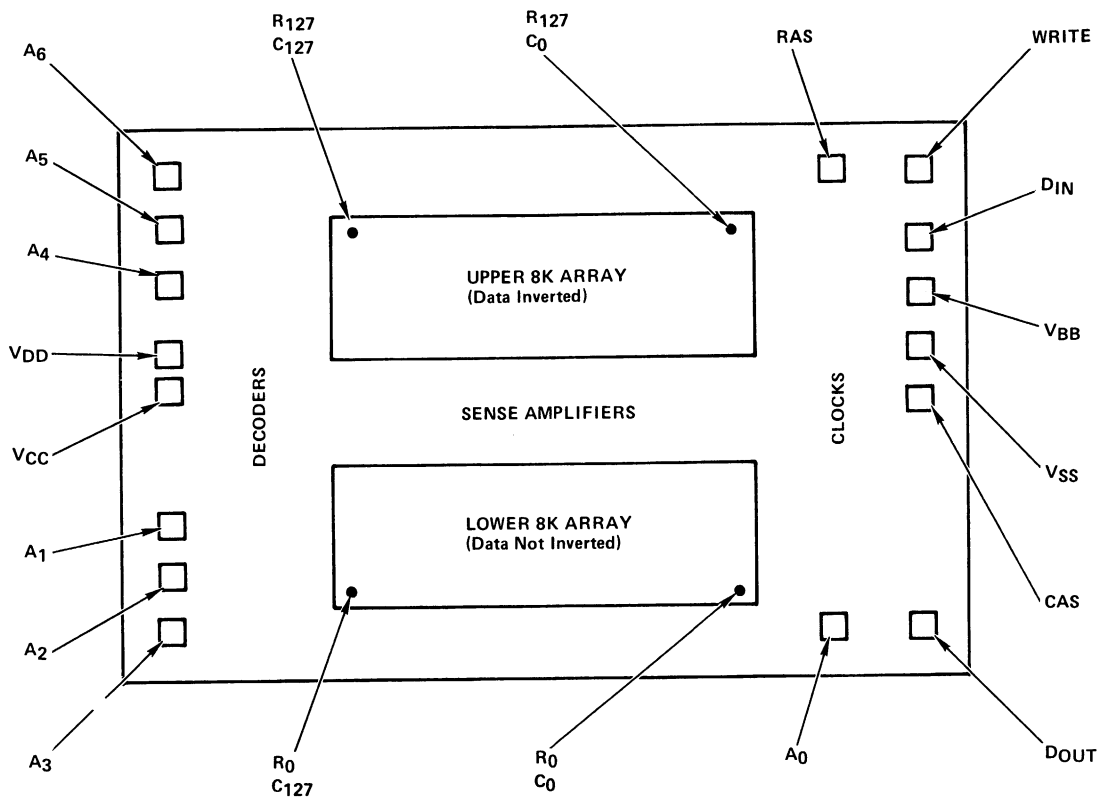
This defines the functional test sequence used by MOSTEK for post burn-in final testing of its 16384 bit dynamic randon-access memory, the MK 4116. The same sequence, with Test No. 4 deleted, is used for the QC audit performed immediately prior to shipment, and for periodic readings during all life test studies performed by MOSTEK. The testers used for all such testing at MOSTEK are Siemens 203 (or an earlier version of the same basic tester, the Computest V200).

The test temperature is an equivalent junction temperature for operation at 70°C continuous still air ambient as calcualted from the equation

$$T_J = T_A + P_D \, \theta_{JX}.$$

Any parameter which is not worst-case at the elevated temperature is compensated to account for variation over the 0°C—70°C specified operating temperature range.

All timing edges are set to data sheet limits plus or minus guardband deltas where appropriate; the power supplies are set to the minimum and maximum data sheet limits plus or minus appropriate guardband deltas (with the exception of V_{CC} which set to the minimum data sheet level only). Input levels are

V_{IH} = minimum data sheet limit minus guard-band delta.

V_{IHC} = minimum data sheet limit minus guard-band delta.

V_{IL} = maximum data sheet limit plus guard-band delta.

unless otherwise noted. The output load is as shown in the attached figure.

MOSTEK reserves the right to make changes in this test sequence at any time and without notice.

OUTPUT LOAD
Figure 5

V_{BIAS} (8.38 volts at MOSTEK Final Test)

402 Ω

D_{OUT} PIN 14 → TO COMPARATOR

C_L 100pF

125 Ω

TEST NO.	TITLE	DESCRIPTION	REASON
1	Continuity (low bias)	Force -0.7 volts relative to V_{BB} on each pin in turn, and check for a current of 100 μA or greater on each pin. If a pin fails continuity, High Bias Continuity (Test 2) is attempted.	
2	Continuity (high bias-attempted only if Test 1 fails)	Force -5.0 volts relative to V_{BB} on each pin in turn, and check for a current of 100 μA or greater on each pin. If all pins pass this test, the part is rejected as a "high substrate resistance" part.	
3	Pre-stress	An address parity data pattern is written into the matrix using a binary addressing sequence (rows fast). The data pattern is immediately read back using the same addressing sequence. The write and read sequences are repeated for data complement.	This test checks for minimum functionality.
4	Stress	Multiple runs are made using a procedure the same as Test 3 except that errors are ignored and the voltage between the power supplies is increased.	Places maximum field intensity across gate oxides.
5	Post-stress	Same as Test 3	This test checks to see if the stress either destroyed or latched up the part.
6	I_{DD} operating (average) (I_{DD1})	With V_{BB} at the data sheed minimum and V_{DD} at the data sheet maximum, measure I_{DD} (average) while repetitively writing "zero" at location (0,0) at minimum t_{RC}. Reject the part of the measured value exceeds I_{DD2} (max).	
7	Substrate Leakage (I_{BB2})	All pins other than V_{BB} are grounded. V_{BB} is biased at -20 volts through the meter and checked for less than 10 μA leakage current.	

TEST NO.	TITLE	DESCRIPTION	REASON
8	Input Leakage ($I_{I(L)}$)	V_{BB} is biased at -5 volts with respect to all other supplies, ground, and the output pin. All inputs are forced to 0 volts and the current measured on each individual input is considered a failure if it exceeds $7\ \mu A$ magnitude. 10 volts is then forced sequentially on each input, and the current is again measured to the same fail condition.	
9	I_{DD} Standby	The device is powered up with minimum V_{BB}, maximum V_{DD}, and maximum V_{CC}. The output is left floating and unused inputs are forced to 0 volts. Multiple toggles between 5 volts and 0 volts are applied to $\overline{RAS}$ and $\overline{CAS}$; after toggling $\overline{RAS}$ and $\overline{CAS}$ are at 5 volts. The maximum I_{DD} in the standby state is then measured.	
10	Output Leakage ($I_{O(L)}$)	The device is powered up with maximum V_{DD}, maximum V_{CC}, and minimum V_{BB}. Unused inputs are forced to 0 volts. Multiple toggles between 5 volts and 0 volts are applied to $\overline{RAS}$ and $\overline{CAS}$; after toggling, $\overline{RAS}$ and $\overline{CAS}$ are at 5 volts. 5.5 volts is connected to the output pin through the meter, and the current is measured against a failure condition of leakage greater than $7\ \mu A$. The output pin is then forced to 0 volts and the current is again measured against the same failure conditions.	
11	VBUMP	At minimum V_{DD} and maximum V_{BB} the entire matrix is written to discharge cells. The V_{DD} and V_{BB} supplies are then slewed in the positive direction, and the entire matrix is read for discharge cells.	This test verifies proper sense amp margins for detection of low storage states.
12	Start-up — Address Parity	After powering up all supplies from 0 volts, eight $\overline{RAS}$-only cycles at maximum cycle time are executed before the entire matrix is written with complement data using a binary addressing sequence (rows fast). It is then read for complement data, written with true data, and finally read for true data using the same addressing sequence.	This test checks that the internal circuitry is adequately initialized with 8 preliminary cycles.

TEST NO.	TITLE	DESCRIPTION	REASON
13	TMOD-Diagonal	The entire matrix is written to a background of complement data. Using a binary addressing sequence (rows fast) the matrix is written using cycles with $\overline{RAS}$ and $\overline{CAS}$ active pulse widths of 10 μSEC. There is a standby stall executed after each column has been written to finish the refresh limit interval. The matrix is then read using the same length cycles and addressing scheme with no standby stalls. The procedure is repeated for complement data.	This test checks both the ability to write and the validity of the output data at the end of a long active cycle. It checks the ability of the row decoders to hold the 127 non-selected row lines "OFF" during a long active cycle, and the ability of the sense amplifiers to read a single bit in a field of complement data.
14	YFAST-Rows 0, 63, 64, 127	Using a binary addressing sequence in a column fast mode, the matrix is written with data until the refresh limit interval is reached. At that time each row is refreshed using a single $\overline{RAS}$-only cycle. The entire matrix is written, read, written with complement data, and read for complement data is this matter.	This test checks for column decoder noise effects on the sense amps and for the other noise related failure modes.
15	Page Mode-Address Parity	Using a binary addressing sequence (rows fast), the entire matrix is written to a background of zeroes. For the number of page cycles that can be executed during the $\overline{RAS}$ active time of 10μ seconds, each row is written with true data. A portion of all 128 rows is written, read, written with complement data, and read for complement data using page mode. This procedure is repeated for a new set of addresses until the entire matrix has been finished. Finally using a normal cycle binary addressing sequence (rows fast) the entire matrix is read for complement data.	This test checks reading, writing, and duration of page mode operation. It also checks the refresh limit interval.
16	Early $\overline{CAS}$, Late $\overline{Write}$-Displaced double checkerboard	Using a binary addressing sequence (rows fast) throughout this test, the entire matrix is written with complement data, written with true data,	This test checks for the refresh limit during an inactive stall as well as "Early

TEST NO.	TITLE	DESCRIPTION	REASON
		read for true data, and written with complement data using normal cycles. Using a late write cycle, the matrix is read for complement data and written with true data in the same cycle. After the entire matrix is written, a standby stall is executed for the refresh limit interval. Using a late write cycle, the matrix is read for true data and written with complement data in the same cycle. Another standby stall for the refresh limit interval follows. The matrix is read for complement data using normal cycles. Finally, the entire matrix is written with true data, read, written with complement data, and read for complement data using cycles with minimum t_{RCD}.	$\overline{CAS}$" and "Late $\overline{Write}$" modes of operation.
17	Address Complement-Horizontal Bars	Using a rows fast, complement addressing sequence (address, address complement, address + 1, . . .), the entire matrix is written, read, written with complement data, and read for complement data.	This test checks the integrity of the address latches and decoders using an addressing sequence which generates many transitions on all address inputs.
18	March-Ones	Using a binary addressing sequence (rows fast), the entire matrix is written with true data. The matrix is then scanned by first reading a cell, then writing it with complement data, and finally reading it for complement data before proceding to the next cell location. The memory is scanned again by reading a cell for complement data, then writing it with true data, and finally reading it for true data before proceding to the next cell location. The procedure is then repeated with the addresses complemented during an identical data and data complement sequence.	Checks for address uniqueness.
19	March-Checkerboard	Same as Test 17.	

TEST NO.	TITLE	DESCRIPTION	REASON
20	High Impedance Output State	Using a binary addressing sequence (rows fast), the entire matrix is written with ones and the output is checked to be in an open-circuit state. Next, while the entire matrix is read, the output is checked to be in an open-circuit state during the time $\overline{CAS}$ is in precharge. The procedure is repeated with zeroes as the data.	This test checks the open-circuit state of D_{OUT}.
21	Vertical Bar	Using a binary addressing sequence (rows fast), the entire matrix is written to a background of complement data. Then the matrix is written with complement data, and finally read for complement data.	Checks for column decoder or adjacent bit interactions.
22	Vertical Bar; Wide inputs	This test is the same as Test 20 except input signal levels are at the data sheet extremes.	
23	Double Checkerboard	Same as Test 20	
24	Ones	Same as Test 20	
25	Walking Diagonal	This is the same as Test 20 except the test is run with the diagonal in all 128 possible positions.	
26	Matrix High	Using a binary addressing sequence (rows fast), all the cells in the matrix are written to a charged state. For the refresh limit interval an attempt is made to disturb half the matrix by generating write cycles which use column fast complement addressing. The test half of the matrix is then read for charged cells. The other half of the matrix is tested for the refresh with the same procedure (the disturbs generated use column fast addressing).	This test checks refresh in a dynamic disturb environment.

TEST NO.	TITLE	DESCRIPTION	REASON
27	Matrix Low	This is the same as Test 25 except the cells in the matrix are written to the discharged state and the disturb time is 100 milliseconds.	This test checks for faulty gate oxides which allow discharged cells to leak toward V_{DD}.
28	t_{CRP}-Address Parity	This is the same as Test 20 except that $\overline{CAS}$ goes into precharge (logic 1) after $\overline{RAS}$ goes active (logic 0), and the output is checked for a continued valid condition for the duration of the $\overline{CAS}$ active time.	This test checks that the output remaining is dependent only on $\overline{CAS}$ remaining active (logic 0) and is independent of $\overline{RAS}$ returning to the inactive (precharge: logic 1) state.

MK4116 POST BURN-IN
Testing

TEST NUMBER	PARAMETERS CHECKED
All functional Tests (additional parameters are listed below)	$t_{RAC}, t_{CAC}, t_{RP}, t_{RAS}$ (min), t_{RSH} t_{CSH}, t_{CAS} (min), t_{RCD} (max), t_{RSH} $t_{RAH}, t_{ASC}, t_{CAH}, t_{WP}, t_{DS}, t_{DH}$
Test 11	t_{RWL}, t_{CWL}
Test 12	t_{RAS} (max), t_{CAS} (max), $t_{RWL}, t_{CWL}, t_{REF}$
Test 13	$t_{RWL}, t_{CWL}, t_{REF}$
Test 14	$t_{RCS}, t_{RCH}, t_{WCH}, t_{CP}, t_{REF}, t_{RAS}$ (max)
Test 15	t_{RCD} (min), $t_{RCS}, t_{RCH}, t_{WCH}, t_{WCR}, t_{DHR}, t_{REF}, t_{CWD}, t_{RWD}$
Test 16, 17, 18 20, 21, 22 23, 24, 26	$t_{RCS}, t_{RCH}, t_{WCH}, t_{WCR}, t_{DHR}$
Test 19	t_{OFF} (max), t_{WCS}
Test 25	$t_{RCS}, t_{RCH}, t_{WCH}, t_{WCR}, t_{DHR}, t_{REF}$
Test 27	t_{CRP}

MOSTEK®

TEST IMPLICATIONS OF HIGHER SPEED 16K RAMS

Testing

By JERRY G. TAYLOR

As the delivery of a new generation of 16K dynamic MOS random access memories reaches higher volume stages, new and more complex problems are confronting both the device test engineer and the test equipment manufacturer. Economically feasible solutions to many of the problems will require the adoption of new and sometimes controversial philosophies regarding memory testing. Certainly a more thorough characterization and knowledge of each device type is required in order to insure adequate testing within reasonable test time limits.

TESTING PROBLEMS

Probably the most obvious problem associated with testing 16K RAMs is that of test times. Since many commonly used pattern sensitivity tests vary in length as a function of the number of bits in the memory (N) by a factor of $N^{3/2}$ or N^2, test time considerations for production testing of 16K RAMs can be quite significant. The following table illustrates the test time penalties paid in moving from 4K RAM testing to 16K RAMs:

TEST TIMES FOR VARIOUS TEST PATTERNS (CYCLE RATE = 375ns)		
	N=4096	N=16384
2N (load-read)	3ms	12ms
$2N^{3/2}$ (moving pattern, row or column Ping-Pong)	197ms	1.6sec.
$2N^2$ (Ping-Pong GALPAT)	12.6sec.	201sec.

The test times listed assume only one pass testing. Testing at multiple voltage corners, timing sets, temperatures, etc. will increase the test times listed for each pattern accordingly.

A second problem which is aggravated by higher speed specifications for 16K RAMs is that timing accuracies on presently available memory test equipment are often not adequate to test particular timing specifications. For example, higher speed 16K RAM specifications call for a row address setup time specification of 0ns and a row address hold time specification of 15ns relative to the row address strobe input. For a tester specified at ±1ns accuracy on any

timing edge from the programmed value including internal clock skews, cables, driver, and transition times, the actual value of a row address hold time programmed to be 15ns could be as little as 13ns or as much as 17ns and still be within the tester specification. Since the actual device speed distribution for this parameter may be less than 10ns wide, a ±2ns tester accuracy could result in significant correlation problems between testers if an attempt were made to specify and test this parameter to the actual device capabilities.

A potentially more severe problem affecting 16K RAM test correlation is power supply, input, and output noise during functional testing. Power dissipation on 16K dynamic RAMs is dynamic in nature with power supply current transients sometimes in excess of 100ma occurring synchronously with internal device clock edges charging and discharging the capacitive loads of internal circuit nodes. As seen in Figure 1, the rise and fall times of these current transients can sometimes be as short as 10ns. Because of these transients, it is extremely important that proper power supply decoupling techniques be used

TYPICAL CURRENT WAVEFORMS FOR MK4116
Figure 1

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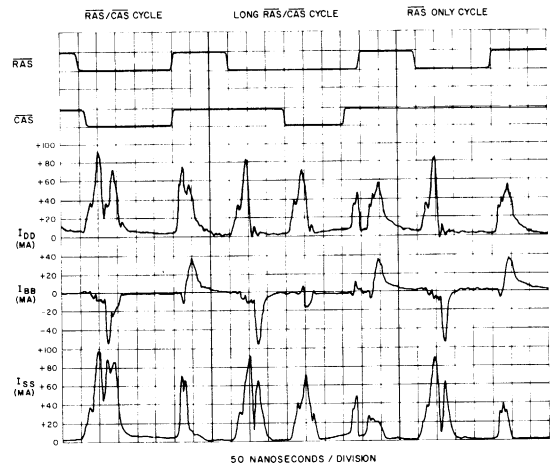
and that the amount of resistance and inductance in the power supply leads from the tester be minimized to insure relatively "clean" signals at the device during functional testing. However, even with extensive engineering precautions it is sometimes impractical to achieve less than two or three hundred millivolts of peak-to-peak noise on power supply and signal inputs at the device during functional testing especially when a temperature controlled handler is also involved. Temperature controlled handlers usually complicate the problem of minimizing inductance and decoupling power supplies as near to the device as possible and therefore can add significantly to the magnitude of noise at the device.

Figures 2 and 3 are examples of the relative integrity of the input signals measured at the device during functional testing of a 16K RAM with the device under the test being physically located first at the test head and then at the end of the handler interface connections. For the example shown, the total lead length for each handler interface signal connection including contactor is approximately 2 inches.

The effects of noise during functional testing vary depending on device type and test conditions. However, in general, noise problems become more severe on higher speed devices. Since the internal clocks of these devices operate at a higher speed, the current transients on the power supplies increase in magnitude and thus induce more noise than slower devices. Also the "windows" during which data is sampled become shorter on faster devices enabling noise of short durations to have a more severe effect. For example, consider a previous generation 4K RAM with a minimum specified access time of 250ns and a minimum address valid time of 60ns versus a new generation 16K RAM with a minimum specified access time of 120ns and a minimum address valid time of 15ns. The 250ns 4K RAM typically requires that the addresses be valid for a minimum of 30ns in order to interpret the address data correctly. However, on the faster 16K RAM design, in order to allow more time for system address multiplexing, a circuit was developed capable of interpreting valid addresses in less than 5ns. For the 4K RAM the effects of a noise transient of a 5ns duration on an address input during the valid address sampling time would probably be insignificant since it's magnitude would be integrated over a 30ns period but for the 16K RAM the effects of the same noise transient during it's address sampling time would obviously be much more significant. Noise transients should not cause failures in 16K RAM operation unless the peak voltages of the transients violate the specified dc opera-

16K RAM INPUT TEST SIGNALS AT TEST HEAD
Figure 2
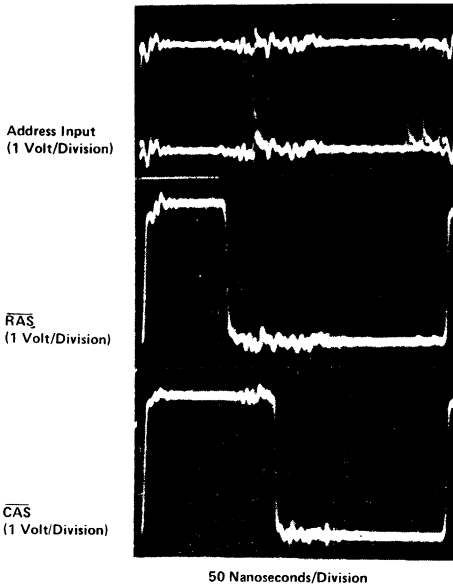
16K RAM INPUT TEST SIGNALS AT TEST SITE OF TEMPERATURE HANDLER
Figure 3

Address Input
(1 Volt/Division)

$\overline{RAS}$
(1 Volt/Division)

$\overline{CAS}$
(1 Volt/Division)

50 Nanoseconds/Division

Address Input
(1 Volt/Division)

$\overline{RAS}$
(1 Volt/Division)

$\overline{CAS}$
(1 Volt/Division)

50 Nanoseconds/Division
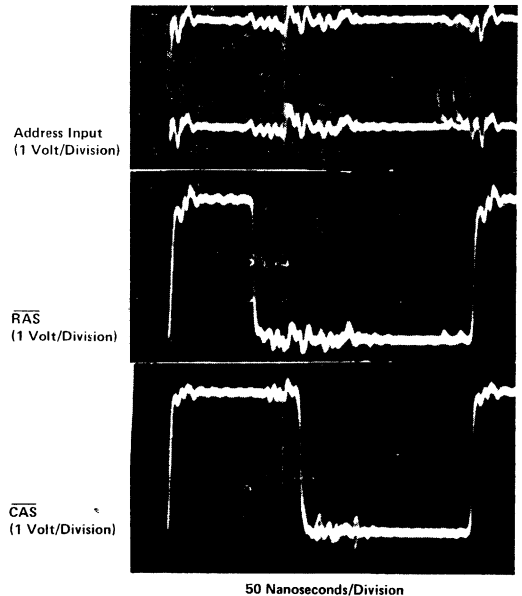
tion conditions for the device. Therefore for a system having a dc logic "0" level of 0.4 volts, a positive 400 millivolt noise transient should have no effect on the operation of 16K RAMs in the system specified to operate with an input logic "0" level of 0.8 volts maximum. However, under "worst case" test conditions with the dc logic "0" input level set at 0.8 volts, transients of even smaller magnitudes can cause device failures resulting in tester correlation problems.

As 16K RAM designs continue to achieve higher performance goals, the problems of distinguishing device failures versus failures induced by noise transients or timing inaccuracies of the test equipment are reaching a new order of significance. Attempts to do "worst case" testing of all specified device parameters simultaneously will usually result in the failure of some quantity of devices that actually, will meet specifications. In many cases a thorough characterization of the device design and process to be utilized can eliminate the need for 100% testing for all specified limits and conditions.

CHARACTERIZATION

The success of any characterization and resulting economically feasible production test program for a particular 16K RAM device type is highly dependent upon the RAM design. If the device is marginal and subject to complex pattern, data, temperature, or voltage sensitivities the development of a comprehensive and economically practical production test procedure could prove to be impossible. Unlike previous 1K and 4K RAM designs, deficiencies such as N^2 pattern sensitivities cannot be tolerated in 16K RAMs. When proper techniques are utilized, it is possible for 16K dynamic RAMs to be designed so that sensitivities due to process variations and weaknesses can be detected using relatively simple and economical address and data pattern test sequences.

The goal of a 16K RAM device characterization should be to identify any sensitivities of the particular 16K RAM design over the full production range of process parameters and the resulting production tests required that are comprehensive in screening for device sensitivities, optimized in terms of test time and economics, and operate within the constraints of the available test equipment. One of the first and most important steps in such a characterization is the selection of the sample to be analyzed. The sample should be large enough to contain a variety of process weaknesses and cover several different fabrication weeks to allow for a maximum of process parameter variation. For some tests such as timing and input voltage parameter characterization, a few hundred devices are probably sufficient, but for other tests such as pattern characterization where

more random types of sensitivities can occur, several thousand devices may be required. In order to insure that particular device characteristics do not change over a period of time, it is advisable to periodically repeat portions of the characterization sequence.

Since virtually all characterization tests will be repeated at the specified temperature extremes for the device, the junction temperature at which each device should be tested in order to guarantee the specified maximum ambient temperature for that device type should be first determined. Most 16K RAMs are specified over the temperature range 0°C to 70°C ambient. The junction temperature (T_J) of each device depends on the power dissipation (P_D) of that device by the equation:

$$T_J = T_A + P_D \, \theta_{JAX}$$

θ_{JAX} is the thermal impedance between the device junction and system ambient. Figure 4 is a graph of this equation for $\theta_{JAX} = 70°C$ per watt which is standard for a 16 pin ceramic dual-in-line package. In order to calculate the proper junction test temperature for a 70°C ambient, the power dissipation on a sample of 16K RAMs must be measured operating continuously at an ambient temperature of 70°C and at the maximum specified frequency.

JUNCTION TEMPERATURE VS. POWER DISSIPATION FOR T_A =70°C
Figure 4
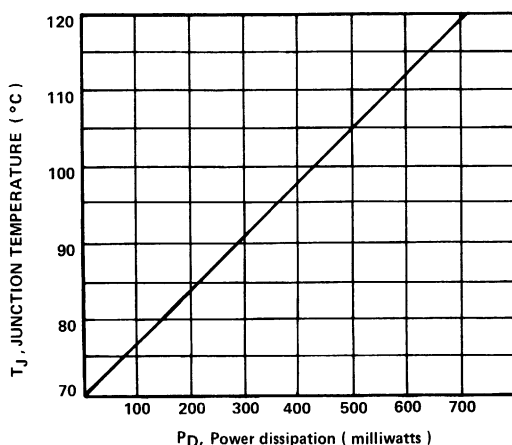
If the device junction temperature is stabilized by using a long warm-up period at the maximum specified operating frequency prior to the first test, the proper test temperature is the specified maximum ambient temperature. If the test is only a few seconds long, then the junction temperature will rise during test only by a few degrees and the proper test temperature should be nearer to the calculated value for junction temperature.

The first stages of the characterization tests should include an extensive analysis of the voltage, power dissipation, and timing characteristics and margins of the device. The test patterns used for these tests will generally be very simple such as a load-read checkerboard or diagonal pattern. For input voltage and timing testing, each device should first be tested at the specified limits for all parameters at the four voltage corner extremes of V_{DD} and V_{BB}. V_{CC} margin testing is usually not necessary since this power supply is connected only to the device output. Each input timing and voltage parameter should then be varied separately until a failure occurs, recording the last passing value of the parameter being tested. If during these tests any parameter evaluated appears to fail or be marginal to a specified limit, then the reason for this condition should be further evaluated with the cause being isolated to a design process or tester fault. A typical example of this type of condition for a 16K RAM might be an indication from the initial characterization data that the maximum input zero level specification of 0.9 volts on the address inputs is marginal when in fact further investigation isolates the problem to noise on the address inputs at the device during the times at which the row and column addresses were being strobed into the device. In this case it would be necessary to correct the problem on the test equipment or compensate the input zero voltage level so that the data from further characterization tests would not be erroneously influenced.

A widely used and highly effective method of characterizing power supply margins is to run a V_{DD} vs. V_{BB} schmoo plot. This method involves holding V_{DD} or V_{BB} at a fixed value while searching for the failure limits of the other power supply followed by changing the fixed value of the supply to a new value and repeating the procedure. All parameters except V_{DD} and V_{BB} should be held at the specified limits during the tests. Figure 5 is an example of a typical schmoo plot for a 16K RAM. Again any indication of a failing or marginal condition to a specified limit should be investigated further and the cause isolated.

Probably the most lengthy portion of a 16K RAM device characterization is the pattern sensitivity evaluation. In the case of many 1K and 4K RAM evaluations this portion of the characterization was not completed. Instead lengthy pattern sensitivity tests were inserted into production test programs with the hope that these tests would be effective in screening for any pattern sensitivities that might exist. This philosophy can obviously not be economically applied to 16K RAM testing.

A thorough 16K RAM pattern sensitivity characterization should include a variety of pattern tests designed to screen for different types of failure

V_{DD} VS. V_{BB} SCHMOO PLOT FOR 16K DYNAMIC RAM
Figure 5

modes and sensitivities of RAMs. These tests are usually referred to by names such as load-read, address complement, march, active refresh, still refresh, walking columns, walking diagonal, galloping rows, galloping columns, write disturb, surround disturb, column disturb, and galpat. It is usually sufficient to run most of the pattern tests at maximum specified frequency but a sample of patterns such as march, address complement, and walking diagonal should also be run at the slowest specified cycle rates. Each device in the characterization sample should be screened for pattern sensitivities at the four (4) corners of the V_{DD} and V_{BB} power supplies and at the specified temperature extremes. The test procedure should be such that all test patterns are tried on each device regardless of previous test pattern failures for the device under test with the test conditions recorded on all failures. Because of test time constraints it should be sufficient to run the longer N^2 pattern tests such as galpat on a sample of a few hundred devices covering a wide range of process parameters, while screening a larger sample of devices to the remaining pattern tests. By analyzing the data gathered from the test described, it should be possible to define a set of test patterns and conditions that is optimal in terms of test time without sacrificing test integrity. The result of an optimized test flow is that pattern tests

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are run only at the power supply voltage corners that have been identified as "worst case" for that pattern, and lengthy pattern sensitivity tests are utilized only when the device sensitivities that these patterns detect cannot be identified using shorter test patterns.

When sensitivities of a device to lengthy test pattern sequences are discovered, it is often possible to develop alternate test methods and patterns that result in dramatically reduced test times and are designed specifically to screen for device related failure modes. The development of such a procedure usually requires that the failure mechanism be well understood in relation to the particular device design.

A successful example of a test procedure developed to screen for a particular device sensitivity is presently being used in the production testing of one 4K RAM device. During the characterization of this device a sensitivity to a disturb type of pattern was discovered. The pattern used consisted of writing the full memory with "1's" followed by writing a "0" two thousand times at the base location. The entire memory, excluding the base cell, was then read checking for an all "1's" pattern. The base location was then written to a "1" and the entire procedure repeated with the base cell incrementing through all possible memory locations. Assuming a 500ns cycle rate, the test time for this sequence was greater than 20 seconds. Initial investigation of the problem revealed that after each base cell had been written 2000 times it was necessary to read only the column of the base location instead of the entire array in order to generate the failure mechanism, which reduced the test time to 4 seconds. Upon further investigation it was found that the failures were caused by voltages slightly in excess of the device threshold voltage being coupled onto the row select line connected to the gates of the one transistor storage cells for that row. Since the base cell on the failing column was repeatedly being written to a "0" causing the column digit bus to be low each cycle, the voltage coupled onto the failing row was sufficient to cause the stored "1" level on the failing cell to be discharged through the cell transistor somewhat each cycle. When enough disturb cycles had occurred to discharge the cell sufficiently, the failure resulted. Since the failure mechanism is highly dependent on the threshold voltage of the cell transistor which varies as a function of the V_{BB} supply voltage, it was possible to reduce the number of disturb write cycles of the base location required from 2000 to 100 cycles by implementing the test at a V_{BB} supply voltage 0.5 volts more positive than the specification normally allows, further reducing the test time requirement to approximately 200 milliseconds. In order to prevent an unnecessary yield loss due to the abnormal supply voltage conditions, a relaxation of the input "0" voltage level was required for the test.

PRODUCTION-TESTING

Once the initial 16K RAM device characterization is completed enough data concerning the characteristics and sensitivities of the particular design should be available to establish a logical and comprehensive production test sequence. Since single temperature production testing is economically desirable, the characterization data must be analyzed for the feasibility of insuring that all devices' specifications are met over the entire operating tempering range for the device while testing at a single temperature. The high temperature extreme virtually always proves to be the only practical choice for a single test temperature because of refresh and parameter margin characteristics of 16K dynamic RAMs. The "worst case" condition for pattern sensitivities power supply margins and timing parameters is typically at high temperatures, but the lower temperature limits can be "worst case" for some device parameters such as input levels and power dissipation. For the device parameters that prove to be the "worst case" at the lower temperature extreme, it should be possible to determine the proper guardbands to be used for high temperature testing from the characterization data.

An important factor which is too often not thoroughly comprehended in establishing the production test conditions for high performance 16K dynamic RAMs is the characteristics and limitations of the production test equipment to be utilized. As discussed previously, tester timing skews of as little as ±1ns can be significant and cause severe correlation problems considering the large number of critical input timing specifications relative to the clock inputs for 16K RAMs. Because of variables such as internal tester clocks, skews, cables to remote temperature handlers, and individual driver characteristics, controlling input timing skews to a tighter specification often proves to be impractical. Fortunately, however, for most 16K dynamic RAM designs, virtually all critical input timing parameters track the column access time of the device as a relatively constant percentage, and by analyzing the device characterization data a correlation factor for each input timing parameter relative to column access time can usually be established. Since the specified column access times, even for higher performance 16K dynamic RAMs, is a relatively large value (typically 90ns or greater), a ±2ns maximum total measurement error is of much less significance. Therefore for most 16K RAM designs, testing for the proper column access times on each device and relaxing the programmed test conditions on input timing signals by a few nanoseconds so that even "worst case" tester timing skews will not violate the specified device limits is sufficient to guarantee that all device timing specifications are met without causing severe tester correlation problems.

The problems associated with variations in signal integrity and noise are usually among the most difficult test equipment related problems to be addressed in 16K dynamic RAM testing. The maximum effort practical should be extended to insure that the integrity of the signals applied to the device under test are the best possible, but often even this does not prevent noise related tester correlation problems. For most 16K dynamic RAMs, test equipment noise related failures occur when noise transients on the input signals at the device during functional testing exceed the "worst case" specified input logic level voltages for that device. Unless the noise levels are excessive, relaxing the programmed dc input voltage levels usually eliminates most failures of this type, but may not be desirable if input voltage level specifications for the device are to be guaranteed. Even though it is not always possible to eliminate noise related device failures when testing for "worst case" input voltage levels, it is possible to separate potential noise related failures by running a portion of the test patterns for each V_{BB} and V_{DD} power supply voltage corner tested at relaxed dc input levels and then change the input voltage levels to the specified "worst case" limits for the remaining test patterns at that supply voltage. Devices which pass relaxed input levels tests and then fail when the specification dc limits are applied can be placed through the test program software into a separate physical bin. Devices in this bin would then require further analysis in order to determine if the failures were device or noise related.

CONCLUSION

In order to establish test conditions for higher speed 16K dynamic RAMs that are effective and economical, the particular characteristics and sensitivities of both the device and production test equipment to be utilized must be understood. Test flows that are optimized for the particular characteristics of a 16K RAM design can result in dramatic savings in production testing costs without sacrifices in test integrity. However, economic success of an optimized 16K dynamic RAM test flow depends upon performing a thorough and lengthy device characterization and the choice of a design that is not sensitive to a wide variety of complex test conditions.
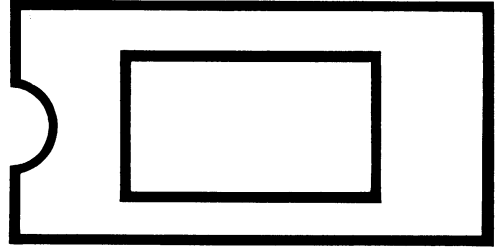
Static Random Access Memory
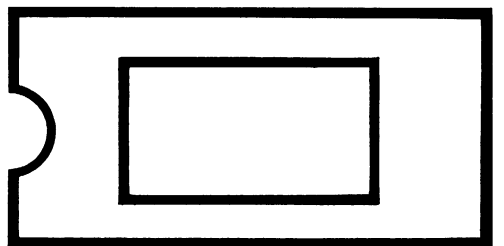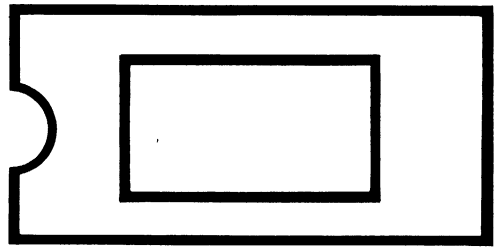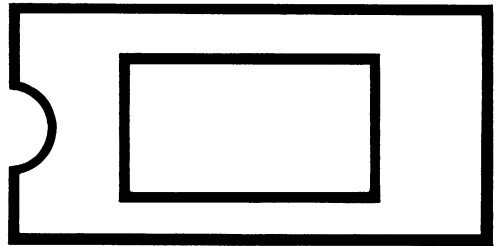
MOSTEK®

UNCOMPROMISING 4K STATIC RAM
RUNS FAST ON LITTLE POWER

By SAM YOUNG

Application Note

Easy to use the new crop of n-channel MOS 4096 static random-access memories may be, but the tug of war between speed and power still looms. However, one RAM stands out because it avoids a compromise between these vital parameters.

Some of its competitors offer fast access times of less than 100 nanoseconds, but require multiple power supplies or dissipate high power. Others, such as complementary-metal-oxide-semiconductor RAMs, use little power, say less than 200 milliwatts, but have access times well above 500ns. The MK4104 is special in being both fast and power-thrifty.

Combining static- and dynamic-memory techniques, the chip achieves a maximum access time of 200 ns (150 ns typical) and maximum cycle time of 260 ns. Yet it dissipates a maximum of only 120 milliwatts of active power at 4 megahertz and a very low 27 mW in standby. An additional low-power mode of 10 mW is available for battery backup operation, achieved simply by lowering the power supply voltage from 5 volts to 3 V.

Moreover, the 4104 is extremely easy to use. It needs only a single power supply, which is in the conventional transistor-transistor-logic position. The device is supplied in the 18-pin package now standard for static memories. It is designed to operate at ordinary transistor-transistor-logic levels with loose power-supply tolerances of ±10%, greatly reducing the cost of close regulation common with ±5% parts.

In addition, the 4104 can accept any TTL input signal meeting worst-case specifications, thus eliminating all level-converting interface circuits that may be needed with other 4K static designs. Moreover, since the 4104 was designed to be tolerant of inputs with very slow rise times, it can directly accept signals from low-power Schottky TTL for low-power applications. Finally, the 4104 will sink 4 milliamperes at

0.4 V and source 500 microamperes at 2.2 V, making it agreeable with all types of TTL-compatible data-bus interface circuits commonly used in memory system design.

A NEW CELL DESIGN

Unlike typical static memories with their six-transistor cells, the 4104 has cells of only four transistors and two ion-implanted polysilicon resistors that act as loads (Fig. 1). This cell design saves space, as well as reducing power dissipation.

Space is saved because polysilicon load resistors can be fabricated practically in the same region as the

NEW STATIC CELL
Figure 1
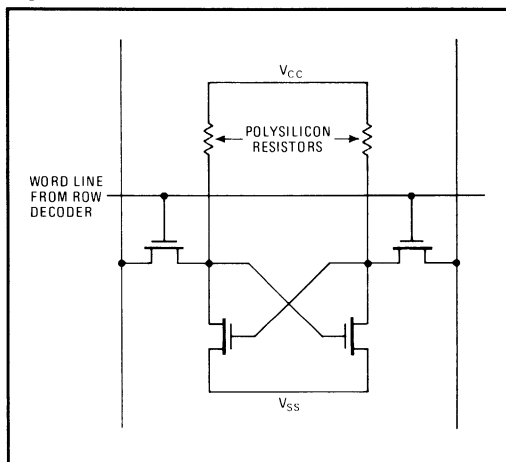
A new static RAM cell design that uses resistors as loads saves space and reduces power consumption. Each 5000 megohm resistor is an ion-implanted polysilicon device that draws less than 1 nanoampere of
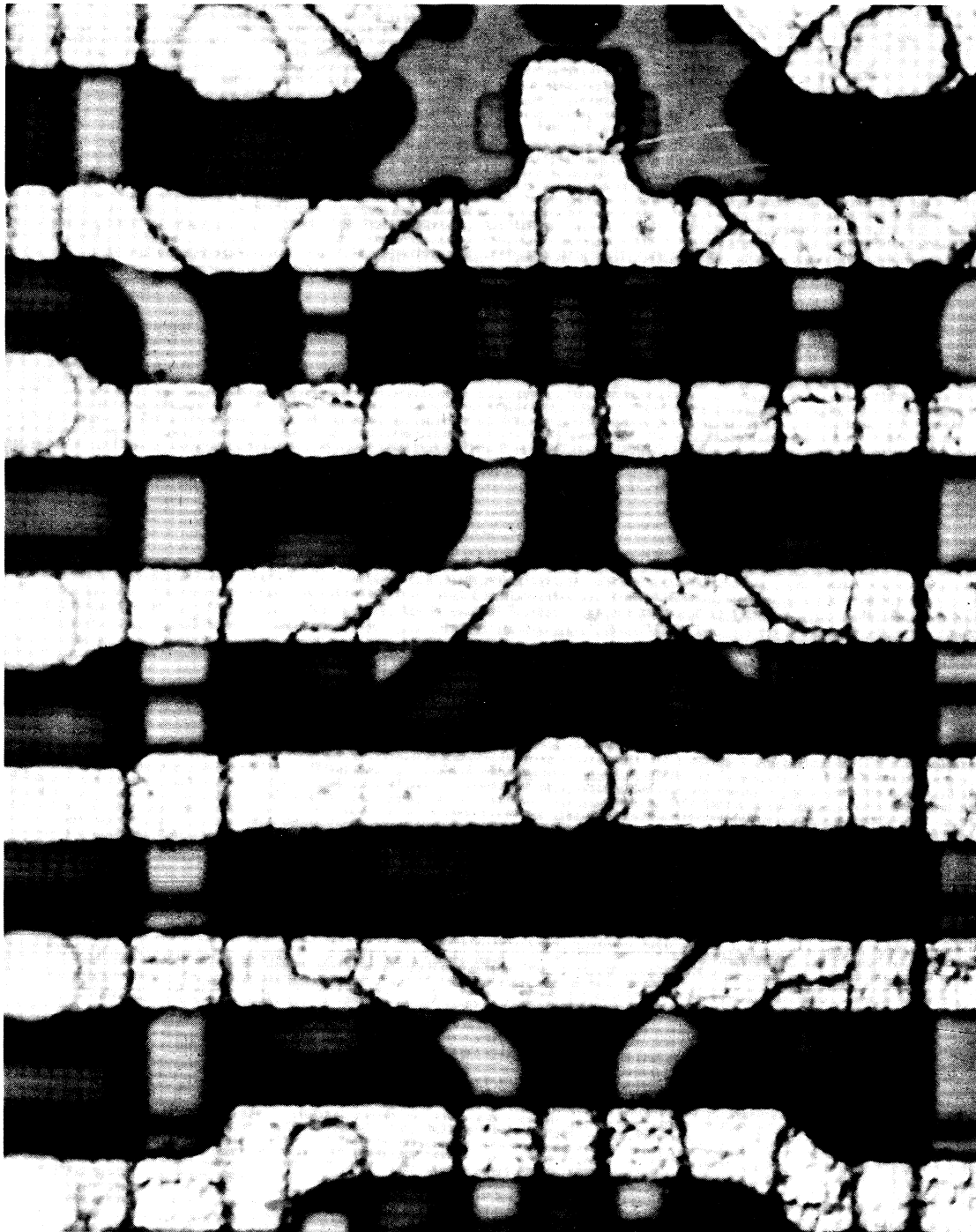
The 4104's cell, which contains four transistors and two ion-implanted resistors, is considerably smaller than conventional six transistor static cells. Cell area is only 2.75 mil^2 or less than half the size of standard static designs. Power is reduced in half.

transistors themselves (Fig. 2). The cell area is only 2.75 square mils—less than half the size of standard six-transistor cells.

Power is reduced because the high-impedance (5,000-megohm) resistors conduct less than 1 nanoampere of current. Also, using ion-implantation to fabricate these loads allows the load-current levels to be adjusted. The resulting power dissipation is only 20 microwatts per memory cell.

The resistors display a negative temperature coefficient and therefore are self-compensating for the increased current leakages that traditionally occur at elevated temperatures. The low currents in the resistors also allow the cell to retain data even when the power supply voltage is as low as a few hundred millivolts above the transistor threshold voltage (typically 1 V). It is this feature that permits the RAM to retain data reliably at very low levels of supply voltage.

Besides polysilicon resistive loads, the MK4104 is one of the few 4K static RAMs to use dynamic (clocked) interface circuits to control the memory array. This dynamic interface makes it possible to use performance-boosting circuit techniques similar to those employed in high-performance dynamic RAMs, such as the MK4027.

DYNAMIC INTERFACES AND SENSE AMP

As in the 4027, signals generated internally from the chip-enable clock cause the internal circuits to power down once their functions have been accomplished. This results in significantly lower power dissipation. Moreover, dynamic circuits are faster since low-capacitance precharge nodes can be employed to shorten the memory cell's RC discharge-time constant.

Once clocks are provided to power the interface, they may also be used to service dynamic sense amplifiers, further improving speed. The 4104 has a differential sense amp conceptually similar to those of the 4027. It can detect differential signals as low as 100 mV, as compared to other static RAM devices, which may require several volts for reliable operation.

As in the 4027, the dynamic balanced sense amplifier uses several clock phases to achieve low-power, high-performance sensing. High speed is achieved by sensing a small differential voltage, thereby minimizing the time required to charge the data bus. The sense amplifier is clocked on after enough time has been allowed for a 100 mV differential to appear on the data bus. Since the sense circuit has a 1-mV sensitivity, a 100-mV sense level allows enough margin for circuit and process variations.

Because the interfaces and sense amp utilize clocked operation and dissipate power only for short intervals when activated, the power dissipation is dependent on the clock frequency and therefore is subject to reduction at lower frequencies. For example, the typical power dissipation at 1 MHz is 23 mW, compared to 70 mW at 4 MHz (Fig. 3). By contrast, the power dissipation for a fully static RAM would remain constant at its high (active) level. Because there is no significant dc path during clock-on periods, damage from high currents cannot occur to the

POWER DOWN
Figure 3
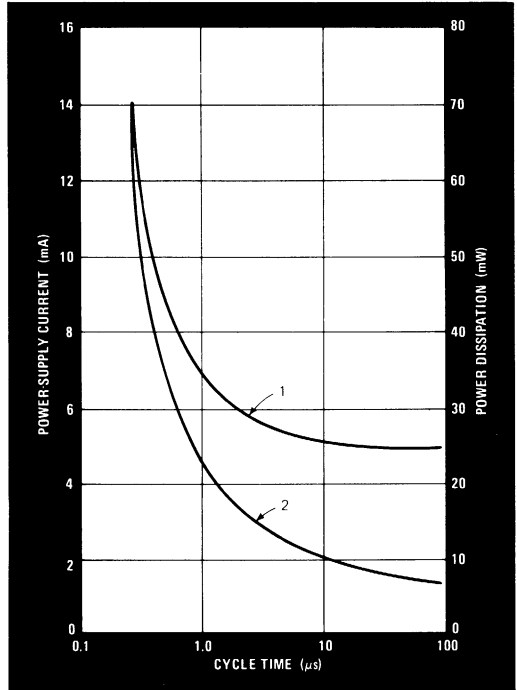
The 4104 is the only static RAM with frequency-dependent power dissipation, resulting from the use of dynamic interface circuits. Clock-on time (low-level) for curve 1 is 100 ns; clock-off time (high-level) for curve 2 is 200 ns. For both curves, ambient temperature is 25 C and power-supply voltage is 5 V.

memory should the clock input become shorted to ground when system malfunctioning may occur.

The MK4104 is organized internally as two 32-by-64 bit memory subarrays, with the row decoders in the middle (Fig. 4), although to the user it is simply a 4K-by-1-bit RAM. The device contains all buffers, decoders, and internal clock generators needed for complete static operation. The decoders are conventional dynamic NOR-gate circuits. The address buffers are a combination of static and dynamic circuitry, permitting a very fast sample-and-hold technique for address capture.
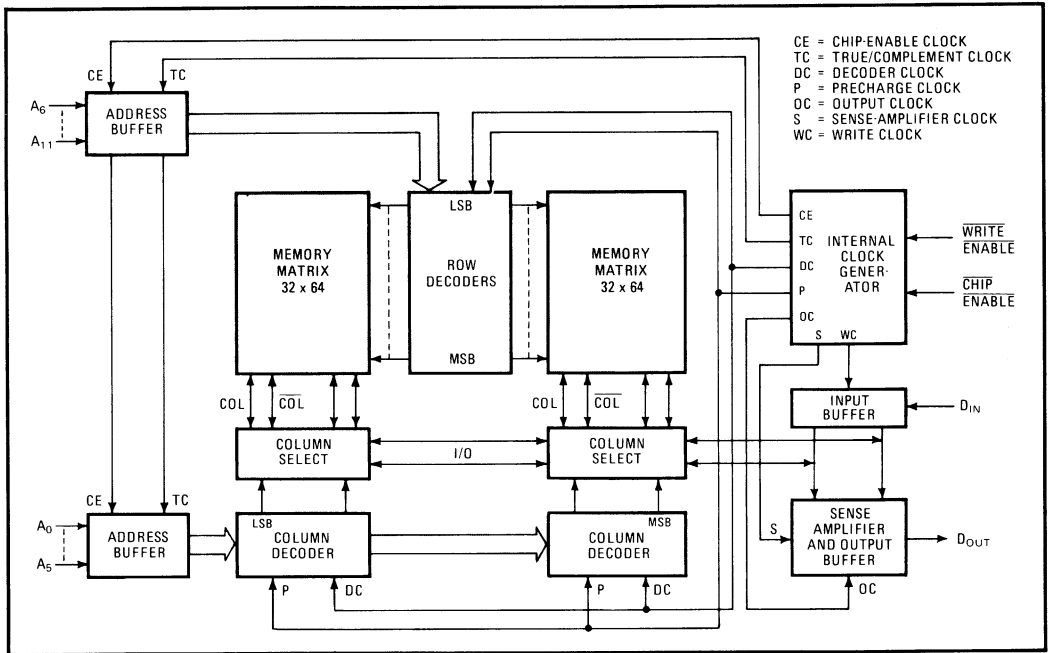
The chip is organized as two 32-by-64-bit arrays, resulting in a 4-k-by-1-bit static device containing all buffers, clock generators, decoders, and sense amplifiers. To minimize power consumption, the interface circuits are dynamic.

USING THE 4104

With a sense amp and interfaces of the dynamic type, this RAM operates differently from its static competitors. The negative-going edge of the chip-enable pulse triggers a sequence of internal clock edges. They activate the address buffers, discharge the precharge clock, transfer true and complement address data to the inputs of the row and column decoders, and finally transfer the decoded row and column addresses to the proper word line and select line.

Then the static input-address buffers are turned off so that they no longer consume power. After a delay to allow time for the cell to transfer data to the differential output sense circuitry, additional clocks activate the output sense circuitry and finally the output buffer. The data is now available at the output terminals of the device.

Once the data is present, the positive-going edge of the chip-enable pulse causes the precharge clock to go high, discharging all other clocks and opening the output circuit. As long as the chip-enable clock is high, the chip remains in the precharge mode, which is also the low-power standby mode. Data will be

maintained indefinitely in this mode. It is now ready for the next cycle: read, write, read/write, or read/modify/write. Each of these operating cycles is initiated by activation of the chip-enable clock.

Address inputs must be stable before this activation. Since these inputs are sampled and latched internally early in the cycle, only a short address-hold time (typically 75 ns) is required. This feature eliminates the need for system address latches to support the memory. Enhanced performance may be obtained by generating the new address in the previous cycle, thus circumventing the slow-address propagation path.

Data outputs become valid after activation of the chip-enable clock. The data-out pin will be in an open circuit mode before appearance of valid data for a simple read. By loading the output with a resistor to either the V_{CC} power supply or ground, the user may choose the data-valid direction on the output bus to which the RAM is connected. Now, during a write cycle, the data-out pin will remain an open circuit if the write-enable pin is activated (typically no later than 80 ns after chip-enable). This property permits the designer to employ common-I/O operation, which is useful for most microcomputer systems.

The data-out pin will then contain valid data during the write portion of the read/write or read/modify/write cycle, assuming the write-enable pulse's negative going edge occurs after the specified access-time interval. Data will remain valid for all cycle types until the chip-enable pin is deactivated.

To write into the MK4104, data inputs must be valid when the write-enable signal goes negative. Data inputs are sampled internally and must remain valid until all internal nodes are charged. This occurs before the write-enable trailing edge. The write cycle is then completed by either the write-enable signal or the return of the chip-enable signal to the inactive state.

BUILDING A SYSTEM

The MK4104 may be easily integrated into large memory configurations in highly compact board layouts. The single-supply device in an 18-pin dual in-line package yields a higher packing density than can be achieved with any dynamic or 22-pin static RAMs.

The pinout was chosen to eliminate crosstalk on critical signals within the array on the storage board. The power pins were positioned to allow maximum connection area between the chip and the power-ground bus of the printed-circuit card. Data-out and data-in pins were positioned to allow optimum placement of decoupling capacitors within the memory array, as well as to separate the clock signals from address signals.

Since refresh is not required, designers can eliminate components that cause time delays, as well as undesirable power-supply transients. And the 5-V ±10% supply, combined with the elimination of refresh

transients, greatly eases memory decoupling requirements. In fact, memory system of MK4104s will require less than a third of the decoupling capacitors recommended for dynamic-RAM systems.

In building memory sizes greater than 4096 bits, the typical power dissipation of 8 mW results in major power savings to the user. For example, a 16K-by-9-bit storage board designed with clocked-interface MK4104s would require 940 mW for the memory array, while the same configuration designed with static-interface RAMs would require approximately 18,000 mW. The larger the memory size or the lower the operating frequency, the greater this differential becomes. The power saving reduces cooling and power costs to the user, as well as improving overall reliability. At typical system design costs of $1.00 to $1.50 per watt, this savings can be significant.

The 16K-by-9-bit system's basic circuitry (Fig. 5) consists of readily available NAND gates and inverters. These support chips can be standard-TTL, high-speed-TTL, Schottky-TTL, or low-power-Schottky-TTL parts. Since the total signal capacitance is directly related to the number of RAMs connected to each signal, the performance of the overall system may be improved by dividing the capacitance load among several drivers when large numbers of memory chips must be driven.

For systems using microprocessors with common input/output data buses, the MK4104's data-in pin may be connected to the data-out pin. To avoid conflict on the data bus, the write operation must be implemented in the early write mode. This merely requires that the write-enable signal be activated prior to the chip-enable pulse, thereby guaranteeing the data-out pin will be open during write operations.

EASY DRIVING
Figure 5
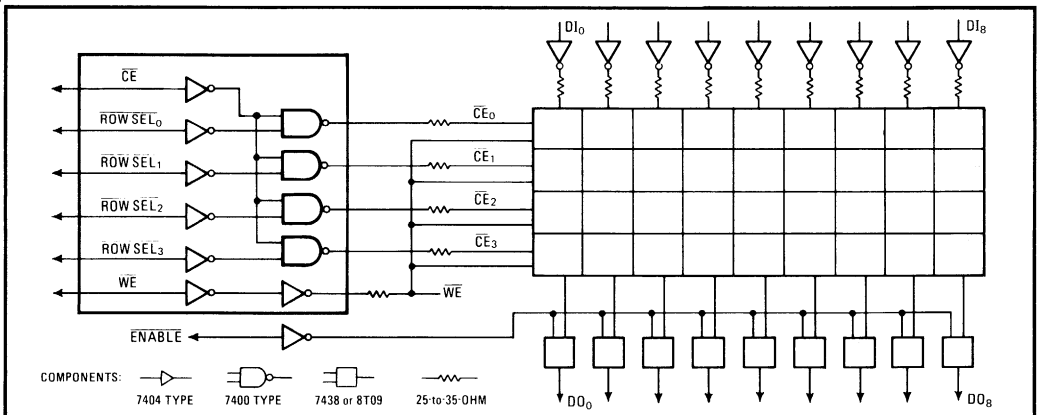
The support circuitry required with the 4104 can be designed with standard TTL or Schottky TTL parts. Low capacitance imputs permit high fan-out capability, which is useful in large control systems.

TESTING AND RELIABILITY

The MK4104 presents no significant testing problems beyond those intrinsic to static RAMs generally. Since the device uses an internal timing generator to strobe the data-out circuitry, the access time is insensitive to address and data patterns, which simplifies worst-case testing for the user.

In order to reduce the time for testing, a user can combine a static cell test with a low V_{cc} mode (3-V) test. Writing and reading data at normal voltage is combined with a wait period at Vcc = 3V to verify that all cells are static and that the part can retain data at reduced power-supply voltage.

A principal factor affecting reliability is junction temperature, which is related to power dissipation and ambient temperature. At 80mW dissipation, the MK4104 operates at a junction temperature of about 75°C (70°C ambient). Typical nonclocked parts under similar operating conditions have junction temperatures approximately 30°C higher because of their higher power dissipation. The lower junction temperature of the MK4104 should result in significantly better reliability.

The single 5-V supply reduces stress on oxides and other key areas within the die. Many failure modes requiring high voltage as a catalyst cannot occur within this RAM.

"Soft" errors, another problem plaguing static RAMs, are generally thought to be caused by poor margin-to-input signal levels, poor tolerances to supply noise, or both. Those error signal occurrences are minimized in the MK4104. The chip is designated for a loose ±10% power supply to increase its tolerance to system noise. Its peripheral circuitry is truly compatible with TTL input levels: a 2.2V input-high voltage level compared to a 2.4-V level for most other static random-access memories, and an 0.8-V input-low voltage that yields an easy-to-live-with 200-mW worst-case noise immunity.

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WHY "EDGE-ACTIVATED" STATIC MEMORIES?

By DAVID WOOTEN

Technical Brief

MOSTEK has recently introduced a new family of "edge-activated" static RAMs and ROMs. These devices have completely static data storage which requires no refresh; however, their peripheral circuitry takes advantage of many MOS circuit design techniques that were developed for dynamic memory devices. These techniques allow MOSTEK's ROMs and static RAMs to attain the best speed/power product that has yet been achieved in other static RAM or ROM of comparable size. The decision to combine a static storage cell with dynamic periphery was based on the fact that while the fully static approach lends itself to bipolar circuit design, it is actually an 'unnatural' mode for MOS circuits. Static circuits simply do not take full advantage of the character of MOS devices. With a properly executed dynamic MOS circuit it is possible to implement a very complex timing and logic function that can operate at speeds comparable to or exceeding the speed of a static circuit performing the same function. The dynamic circuit will also, in virtually every instance, have a much lower power dissipation than the static circuit.

The advantage of low power dissipation cannot be overstated. The feature makes feasible new applications for static memories; it means lower system costs by reducing power supply and cooling requirements; and it yields a more reliable product. Reliability is enhanced because there is so little heat generated by these devices to harm the memories or other components in the system. In short, the "edge-activated" static memory is an innovation that promises so many advantages over fully static memories that it should become the industry standard for NMOS static devices.

The speed/power advantages that dynamic circuits have over static circuits can easily be demonstrated with a 'NOR' decoder of the type that is commonly used in memory devices as row or column decoder. In a typical 4K RAM there are 64 of these decoders that are used as row decoders and 64 as column decoders. It should be obvious that the power consumption in each of these 128 decoders must be kept as small as practical or the chip's power consumption would be so large as to make it useless. In the static row decoder (Fig. 1A) a row is selected when all address inputs to the decoder are low making the output high. The need to keep the power consumption of this decoder at a minimum is in direct conflict with the desire to make it as fast as possible. The only way to make the decoder fast is to make the pull-up resistance small so that the capacitance of the

STATIC 'NOR' ROW DECODER
Figure 1A
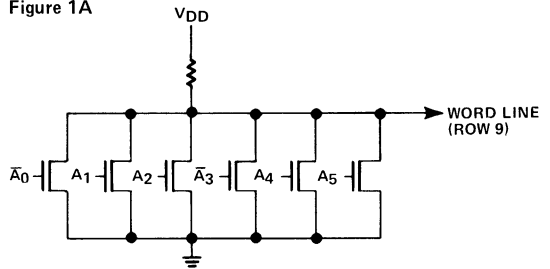
DYNAMIC 'NOR' ROW DECODER
Figure 1B
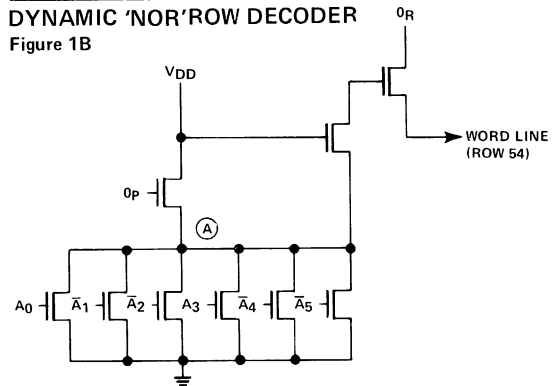
word line can be charged quickly. However, only one row decoder's output is high; while the output of each of the other 63 decoders is low, causing the resistor current to be shunted to ground. This means that the pull-up resistance must be large in order to reduce power consumption. As an illustration, assume that the row decoders in a 5 volt 4K RAM can be allowed to dissipate 300mW typical (this does not leave much for the rest of the chip but who's counting). 63 of the decoders are going to dissipate all of the power giving an allowable value of pull-up of about 5.3K. Since the 5.3K of the selected row must charge about 5pf of word line capacitance (typical word line capacitance in a 4K memory matrix) this gives a τ of about 16ns. Now, lets try the same problem with a dynamic decoder. In the dynamic decoder (Fig. 1B) the decode is accomplished by presetting (precharging) node A all of the decoders to a high state during the chip inactive time. The precharge clock is turned off at chip enable time and the addresses are strobed into the decoders causing node A on all but the one selected decoders to go low. The 'on' resistance of a decoder transistor is less than

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500 Ω and the total capacitance at node A is about .4pf giving a τ of only .2ns. If we allow 5 τ for the decoders to settle before turning on the low impedance row clock (Φ_R), that charges the selected row line, and assume a maximum row drive impedance of 1K, we see that we can get the output of the dynamic decoder to the 63% voltage point in only 6ns as opposed to the 26ns for the static decoder. The really interesting thing is that the only power consumed by the dynamic decoder is the transient power drawn during capacitor charge time. Therefore, by using a dynamic decoder, it is possible to accomplish the decode in less time at a much lower power dissipation than is possible with the static decoder.

Dynamic circuit techniques can offer similar savings in speed and power for virtually every function of the memory circuit. Also, in cases where it is desired to use static circuits, it is possible to use the clocks available from dynamic circuits to selectively disable power consuming portions of the static circuits when they are not being used. This, and the fact that the quiescent dynamic circuits consume only leakage currents, make it possible for the device to have an 'automatic standby'. The impact of this feature can be seen in typical memory systems that have a low average memory duty cycle. Table 1 is a comparison of two 64K byte memory systems one using the MK 4114 edge-activated 1K x 4 static RAM and the other using the fully static 2114. Note that even if the worst case numbers are used for the MK 4114 and typical numbers are used for the 2114, the 2114 system consumes 1250% more power than the MK 4114 system. Using worst case numbers we find that the 2114 system would consume over 90 watts which is over 20 times as much power as the MK 4114.

This difference in device power consumption has many system implications such as the size of the power supply and the cooling capacity of the enclosure. But if these factors are of no concern, the lower power consumption of the MK 4114 has an even more important system implication. Since each chip in our 4114 memory system dissipates at least 400 mW per chip, their junction temperature is about 28°C above ambient (θ_{JAX} for 18–pin ceramic package 70°C/watt). However, the average temperature rise in the MK 4114 memory system is only 1.47°C which is more than 26°C lower than the 2114. It should be noted that this does not include the effects of heat transfer between devices in a system. Actually, the difference in junction temperature will be much greater. As every component engineer knows, junction temperature has a profound effect on MOS device reliability. According to the temperature acceleration curves given in MIL-STD-883A, a 26°C decrease in junction temperature represents an order of magnitude increase in chip reliability.

The low power and high reliability advantages of using dynamic circuits in static RAMs and ROMs are not gained without some penalty. One penalty is that in order for the chip to generate clocks internally the user must supply an activation edge. Obviously, if this causes the chip to be impossible or even very difficult to design into a system, the advantages of the dynamic design would probably not be worth the penalty. However, this is hardly ever the case. In almost every application of static RAMs the system already provides a signal that can be used to generate the activation edge for the memory. In fact, most fully static designs are implemented using some kind of selection for the memory that can be used as the clock for the edge-activated devices. A good example is a Z80 to static RAM interface (Fig. 2). When the decoder is connected as shown (as it usually is) it makes absolutely no difference which flavor of static RAM is used. The static and edge-activated devices will both function properly.

Another penalty of the edge-activated approach is that dynamic circuits are more difficult to design. For manufacturers who do not have much background in dynamic circuit design, this means that edge-activated static memory design would be higher risk for them than fully static design. MOSTEK, of course, is the current industry leader in dynamic circuit design as evidenced by its MK 4027 4K dynamic

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COMPARISON OF FULLY STATIC VS. EDGE-ACTIVATED STATIC MEMORY SYSTEM POWER
Table 1

	2114 (TYPICAL VALUES)	MK4114 (WORST CASE VALUES)
Memory System Size	64K Bytes	64K Bytes
Required System Transfer Rate	3M Byte	3M Byte
Average Cycle Rate Per Chip	47 KHZ	47 KHZ
Average Power Per Chip	400 MW	32 MW
Total Memory Power Consumption	51.2 Watts	4.1 Watts
Total Memory Current at +5 Volts	10.24 Amps	0.82 Amps

8K BYTE STATIC RAM SYSTEM FOR Z80
Figure 2
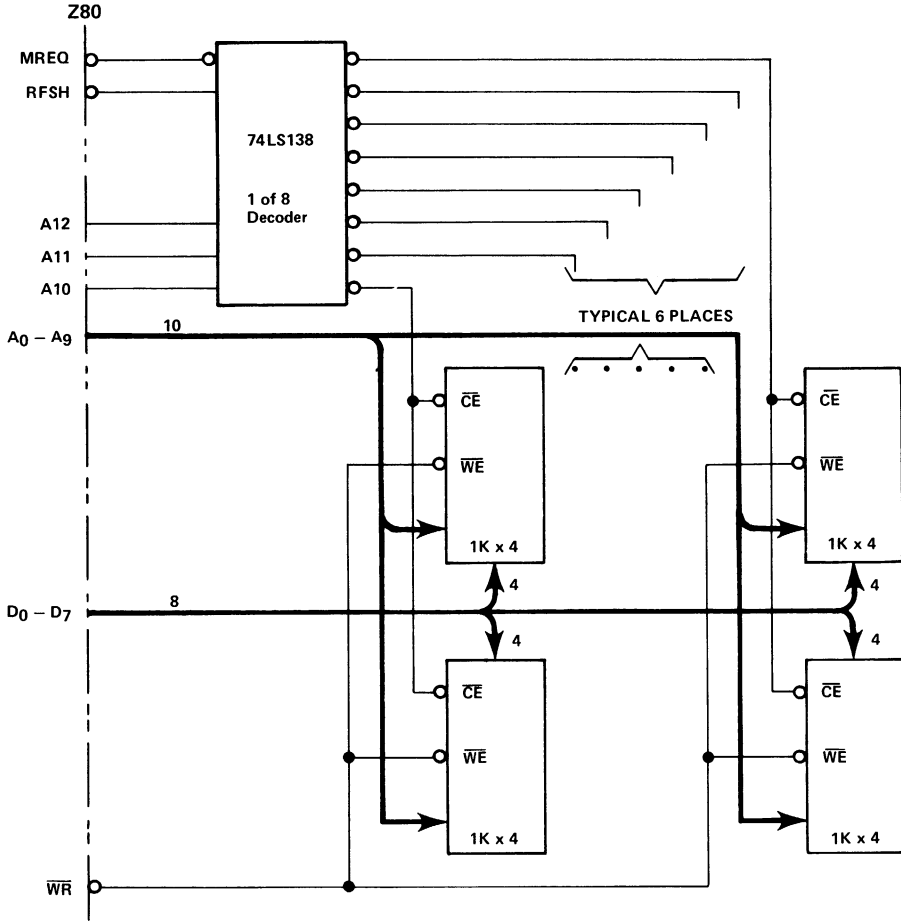
and MK 4116 16K dynamic RAMs. Therefore, MOSTEK has the expertise necessary to bring the benefits of dynamic circuit techniques to the static RAM and ROM market.

In conclusion, by using the dynamic circuitry wherever possible, MOSTEK is capable of producing static memory devices that offer great speed power benefits.

Systems that use these devices can have smaller power supplies, less cooling equipment and operate more reliably. Naturally, MOSTEK expects other semiconductor manufacturers to eventually follow it's lead in this area. The impetus for them will be provided for customers who recognize and demand the advantages that edge-activated devices provide.

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DESIGNING WITH MOSTEK'S
EDGE-ACTIVATED MEMORY CONCEPT

By SAM YOUNG

Application Note

ABSTRACT

Historically, 5V static MOS RAMs have been slow, or have had high operating power and standby power, or have been some compromise thereof. The user, therefore, had to give up the high speed, low standby power attributes of dynamic RAMs in order to avoid the complications of refresh, non-static storage and multiple power supplies. This compromise was not acceptable to MOSTEK designers. An alternative was sought and the Edge Activated* RAM concept was born.

INTRODUCTION

The Edge Activated concept permits the use of circuit techniques not previously possible with static storage. The Edge Activated concept employs an internal clock generator to permit operation with very low power consumption. The clock generator permits use of a unique cell which enhances performance and reduces chip area. The Edge Activated part, of course, does not require refresh or any other periodic activation. The Edge Activated component remains in low power mode, 75% of active power, when the clock is not active. For the static RAM member of the family, an additional power down option is available for battery back-up. The standby power may be reduced from 28 to 10mW reducing V_{CC} to 3V. The Edge Activated concept was designed for ease of use and reliable performance.

THE CONCEPT

The Edge Activated concept can best be explained by referencing Figure 1. The Edge Activated ™ RAM requires all address inputs to be valid prior to initiation of a negative going edge-on the chip enable input. The chip enable signal must remain valid for a specified duration, equivalent to the minimum access time of the component. A recovery time between cycles, 50% of specified access is required for proper operation. DO becomes available, t_{ACC} after $\overline{CE}$ and remains valid until chip enable is deactivated.

The requirements of the Edge Activated interface is one which is readily available from most microprocessor chips or can be readily obtained from processor/memory controller timing.

*Trademark of MOSTEK Corporation

LOW VOLTAGE, EDGE-ACTIVATED RAM/ROM FAMILY
Figure 1
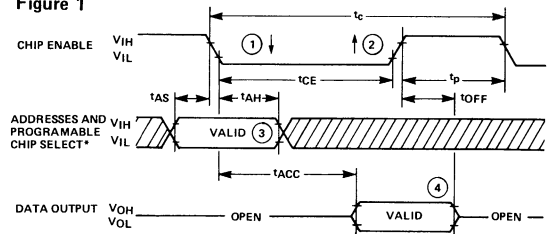
1. A SIMPLE HIGH TO LOW TRANSIS TION AT THE CHIP ENABLE (CE) INPUT ACTIVATES THIS ENTIRE FAMILY OF MEMORY DEVICES

2. RETURNING TO CE INPUT TO A HIGH LEVEL IS ALL THAT IS REQUIRED TO ACHIEVE A 75% REDUCTION IN DEVICE OPERATING POWER· WE CALL THIS FEATURE "AUTOMATIC STANDBY"

3. ADDRESS INFORMATION IS STROBED AND LATCHED INTO A SET OF ON–CHIP REGISTERS.

4. YOU HAVE FULL CONTROL OF THE DATA OUTPUT; THIS IS DETERMINED BY THE CE PULSE WIDTH.

BENEFITS TO THE USER

The Edge Activated concept brings multiple advantages to the user. These benefits are:

· 5 volt 10% tolerance power supply
· TTL logic compatibility
· Low active power - 1/5 that achieved with other design techniques.
· Low standby power- 1/5 to 1/30 that achieved with other design techniques.
· Increased system density
· Reduced voltage/power data retention mode
· Denser components
· Improved reliability
· Reduced system cost

The power savings achievable by utilizing MOSTEK's Edge Activated concept is graphed in Figure 2. This figure shows the power dissipation of MK4104 devices in various system configurations. For comparison, a 64Kx9 memory with Edge Activated static RAMs dissipates 4.9W while non-Edge Activated static RAMs would dissipate 102W in a similar application. As everyone knows, power costs money, reduces reliability and density in a system.

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MEMORY SIZE VERSUS POWER DISSIPATION
Figure 2
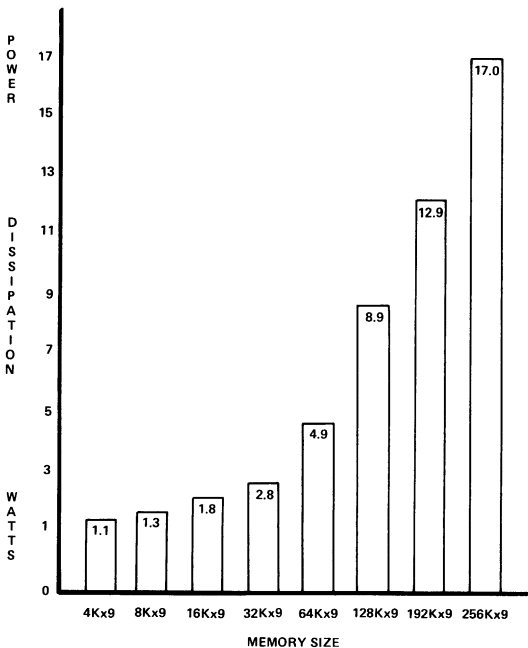
THE FAMILY

The Edge Activated family consists of the following products:

Dynamic RAM	Static RAM	ROM
MK4027	MK4104-4Kx1	MK36000-
MK4116	MK4114-1Kx4	64K ROM

4027/4116

The Edge Activated 4027/4116 have been widely copied and are presently the industry standard Dynamic 4K and 16K RAMs. The knowledge developed to permit these complex RAMs to meet the memory users objectives of speed, density, and reliability has been applied to the newer members of the Edge Activated family.

4104/4114

The MK4104 4Kx1 and its 1Kx4 equivalent the MK4114 are both static RAMs applying the Edge Activated concept previously defined. The static RAM features 200ns access time while expending a mere 120mW of power.

4104 OPERATION

The requirements for correct operation of this Edge Activated RAM for its various cycles types as follows:

READ CYCLE

The read cycle operates as follows, reference Figure 3. Address information present at input pins A_0-A_{11} must be valid ($\geqslant$ 2.2 for a logic "1"; $\leqslant$ 0.8 for a logic "0") before the $\overline{CE}$ clock becomes less negative than 2.2 volts. The address lines must be valid until T_{AH} (address hold timer) nsec after $\overline{CE}$ has been activated ($\leqslant$0.8V). Data out will become valid T_{ACC} nsec after $\overline{CE}$ is activated and will remain valid until $\overline{CE}$ becomes more positive than 0.8 volts. The data hold time t off is influenced by the capacitive loading external to the 4104 device. After a short recovery time, (TP) approximately 50% of access time, the 4104 is ready to accept a new cycle.

EARLY WRITE CYCLE

The early write cycle has the same address requirements as a read cycle. The early write cycle requires that $\overline{WE}$ be valid no later than 20nsec after $\overline{CE}$. In this mode the data out buffer will stay open circuit permitting common I/O operation (DO pin connected to the DI pin).

The cycle is initiated by $\overline{CE}$ going active (referenced Figure 4). Data in will be latched into the chips registers by the later occurring event of $\overline{CE}$ and $\overline{WE}$. The Data in line may change after the TDH (Data in hold) parameter has been met. The write enable pulse must remain valid for TWH (write enable hold) nanoseconds. Since TWH is much greater than the minimum write enable pulse width, it is the parameter which determines the $\overline{WE}$ pulse width. The write cycle is completed by the $\overline{CE}$ pulse returning to the inactive state. The trailing edge of $\overline{WE}$ may return to the inactive state as soon as TWH is met or as late as 0 nsec before $\overline{CE}$ goes active for the next cycle. If the next cycle is another early write the $\overline{WE}$ write enable signal may remain active low.

WRITE CYCLE

The write cycle is a less restrictive early write cycle. In this mode the user should not care what state the data out pin is in. The $\overline{WE}$ leading edge is then non-critical relative to $\overline{CE}$ being activated. In this mode (reference Figure 4) the TWPL (write enable to chip enable precharge lead time) and the TWW ($\overline{WE}$ pulse width) are the limiting parameters. This simply requires a minimum $\overline{WE}$ pulse width and a minimum $\overline{WE}$ pulse overlap with chip enable active. DI is latched in by $\overline{WE}$ being activated. The hold time is determined by T_{DHC} or T_{DHW} which ever is longer. The cycle is terminated in a manner similar to the early write.

READ CYCLE
Figure 3
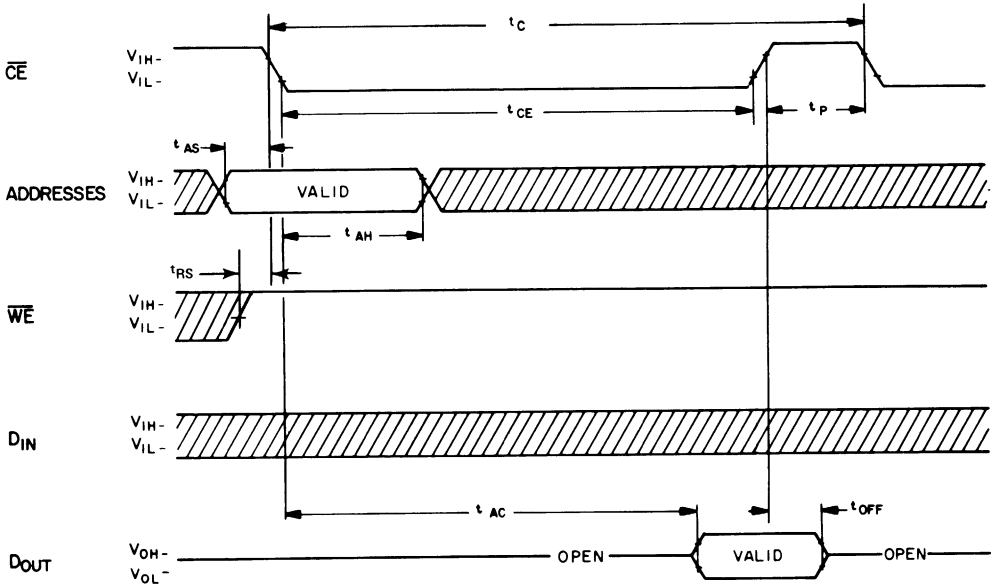
WRITE CYCLE
Figure 4
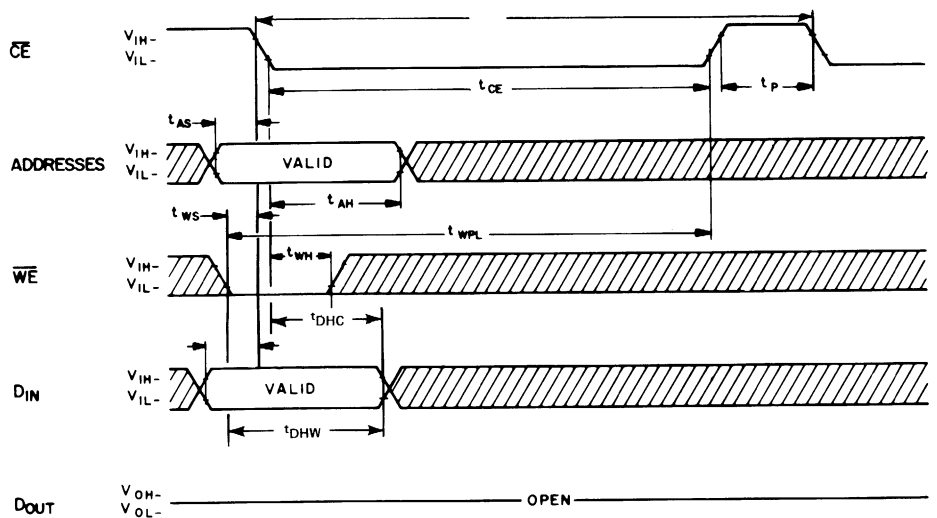
READ-WRITE

The read-write cycle is a combination of the read only and write only cycles. In this mode after address is stable $\overline{CE}$ is activated and T_{ACC} (access time) later data out is valid. At T_{ACC} time the $\overline{WE}$ pulse may be activated without disturbing the data out from the RAM. Data in must be valid prior to $\overline{WE}$ active for proper operation. The hold time in this mode is determined by T_{DHW}. The read-write cycle is terminated in a manner similar to the write cycle.

READ-MODIFY-WRITE CYCLE

The read-modify-write cycle is an extension of the read-write cycle. After data is read $\overline{WE}$ is delayed until data in information is available to the RAM. This cycle requires a longer $\overline{CE}$ active pulse, hence a longer cycle time, due to the time needed to modify the read data. This cycle terminates in a manner similar to the read-write cycle. Reference Figure 5.

MK36000

The MK36000 is an Edge Activated concept ROM. This unique ROM has a density of 65,536 bits with access time of less than 250ns while dissipating a stingy 200mW when selected and 50mW when de-selected. It is conceivable in 1978, this ROM concept can achieve performance characteristics approaching 100ns access times. The ROM uses MOSTEK's standard N-channel silicon gate process and obtains its performance features through the Edge Activated circuit design concept. For comparison, previous ROMs have achieved speeds of 350ns while expending about 600mW of power dissipation. The operation of the ROM is identical to the basic Edge Activated concept operation of Figure 1.

APPLICATION TO A Z-80 MICROPROCESSOR

The Edge Activated component may be interfaced to a Z-80 microprocessor with minimal additional components. Figures 6 and 7 show typical implementations of the 4104 (4Kx1 static) and 4114 (1Kx4 static) RAMs. A non-Edge Activated RAM would have a similar interface. A ROM could be implemented in a similar manner. For a ROM the R/W, DIN signals and associated logic could be eliminated.

IMPLEMENTING THE EDGE ACTIVATED

Implementing the Edge Activated component is similar to utilizing any other dense memory component. The requirements are typical of all dense memory products available today. The MK4104 is chosen for this section since much has already been written about dynamic RAMs. Several design fundamentals must be realized and adhered to in order to allow a successful design effort.

TIMING WAVEFORMS (CONT'D)
READ-MODIFY-WRITE CYCLE
Figure 5
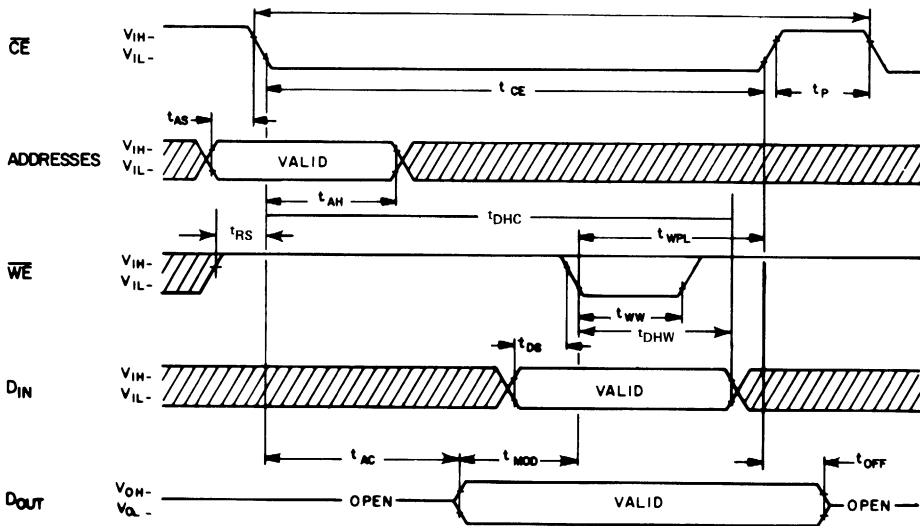
Z80 Nx1 STATIC RAM INTERFACE
Figure 6

MK4104—4K x 1
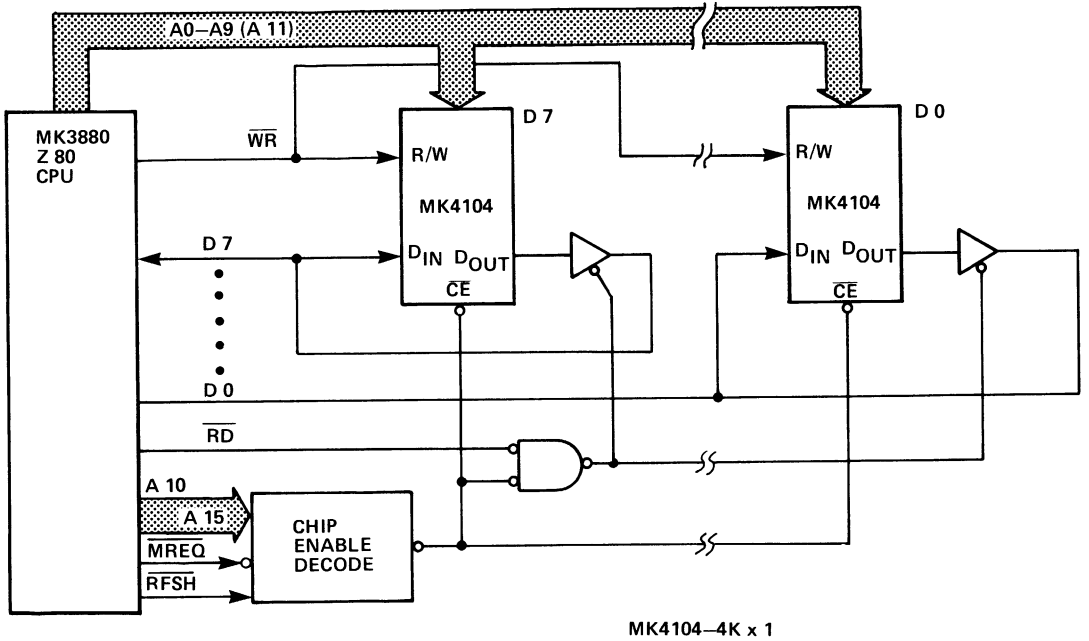
Z80 1Kx4 STATIC RAM INTERFACE
Figure 7
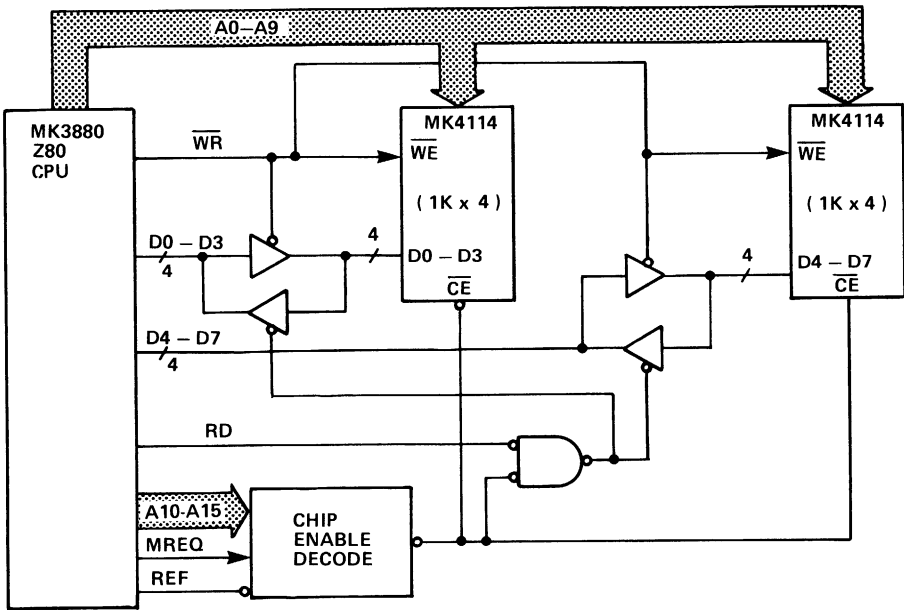
DECOUPLING

Edge Activated RAM's require a high current for a very short intervals of time. This requires use of high frequency decoupling capacitors within the memory matrix. Since the frequencies of interest can be as high as 100MHz very high frequency response capacitors are required. Ceramic $0.1\mu F$ capacitors have been empirically found to best serve this function. The MK4104 pinout was chosen to permit implementation of the required capacitors with minimum area loss. One capacitor every other RAM is suggested. The configuration of Figures 8 and 9 are suggested to achieve optimum performance with axial or radial lead capacitors.

MATRIX INTERCONNECT TECHNIQUE AND PLACEMENT OF HIGH FREQUENCY CAPACITOR WITHIN MK4104 MATRIX
Figure 8
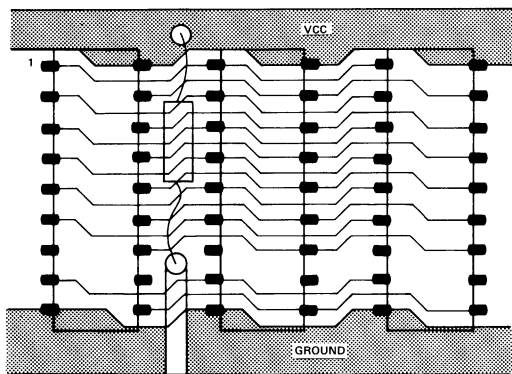
PLACEMENT OF RADIAL LEAD DECOUPLING CAP. WITHIN MK4104 MATRIX
Figure 9
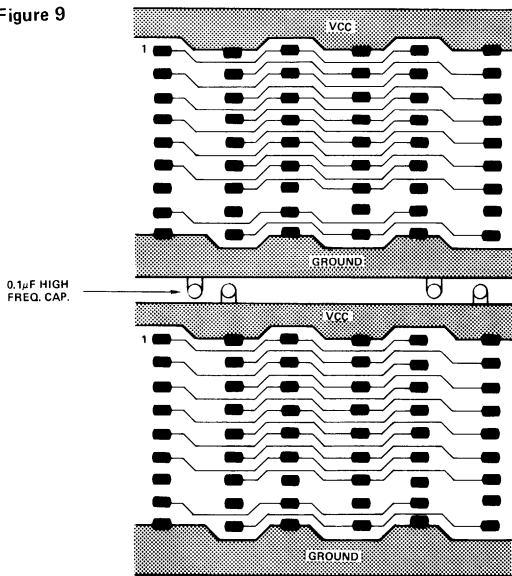
POWER DISTRIBUTION

The MK4104 pinout was designed to permit use of two-sided printed circuit boards. Multilayer boards can, of course, be utilized with good results. The power and ground distribution scheme of Figure 10 offers the following advantages:

A. Low inductive path between the RAM and its decoupling capacitors.
B. Low ground impedance to reduce induced noise.
C. Minimized ground offset between TTL memory drivers and memory chips.
D. Supplies constant impedance reference for signals traversing the board-reduces reflections
E. Reduces intersignal cross talk due to reduced signal to ground spacing.

MK4104 POWER—BUS DISTRIBUTION SCHEME, FOR COMPACT LAYOUTS
Figure 10
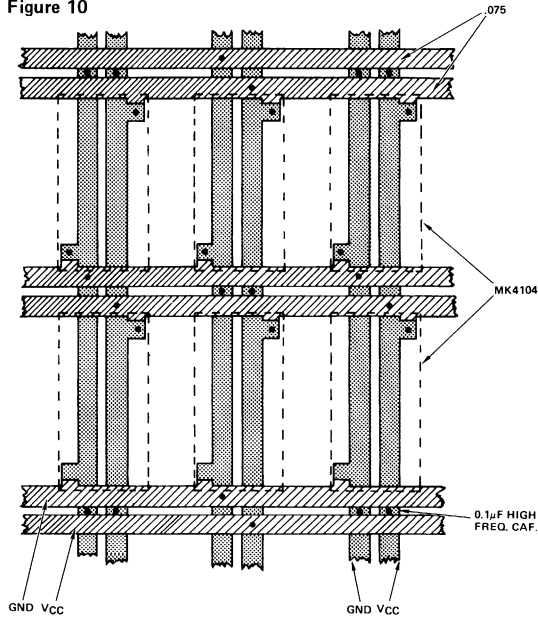
LOGIC DESIGN

The MK4104 was designed to permit use of standard TTL logic without requiring any level enhancing devices. A typical design of a 16Kx9 memory board is shown in Figure 11. Chip enable is decoded in order that it occurs on only one memory word simultaneously. Address lines and $\overline{WE}$ may go to all chips simultaneously. See Figure 12 for architecture.

The resistors in series with the line are required to eliminate signal ringing caused by the impedance mismatch between the driver and the line. In general, omitting these resistors will result in signal character-

Figure 11

Figure 11 diagram labels:
- $\overline{CE}$
- $\overline{ROW\,SEL_0}$
- $\overline{ROW\,SEL_1}$
- $ROW\,SEL_2$
- $ROW\,SEL_3$
- WE
- ENABLE
- DI_0 ... DI_8
- CE_0, CE_1, CE_2, CE_3
- WE
- DO_0 ... DO_8
- COMPONENTS: 7404 TYPE, 7400 TYPE, 7438 or 8T09, 25 to 35 OHM
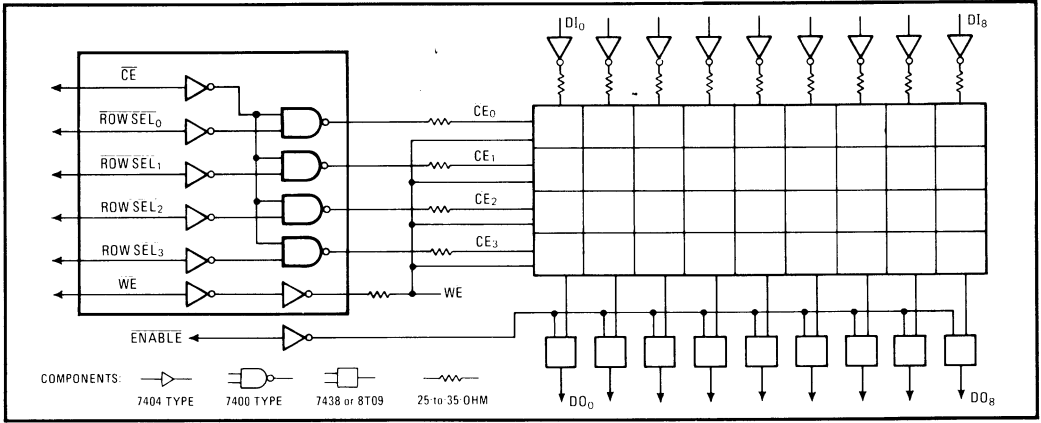
TYPICAL INTERCONNECT FOR 16K x 9 ARCHITECTURE

Figure 12

Figure 12 diagram labels:
- $A_0 - A_{11}$ 12
- $\overline{CE\,0}$
- $\overline{WE}$
- $\overline{CE\,1}$
- $\overline{CE\,2}$
- $\overline{CE\,3}$
- MK4104
- DO 0, DI 0, DO8, DI8
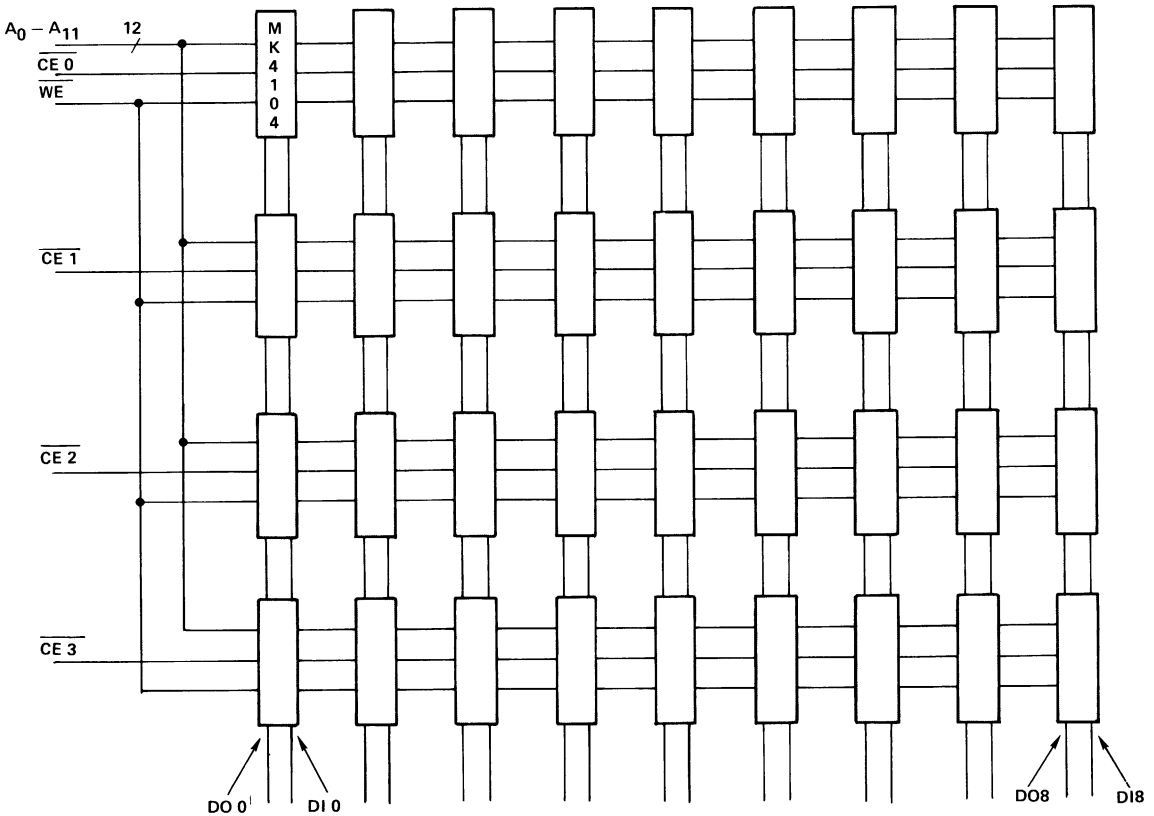
istics which violate the RAM specification. The exception to this is where a slow driver, such as low power Schottky, is utilized and the line lengths are kept reasonably short.

Terminating the signal line at the receiving end is an alternative method which may be employed, this techniques has several drawbacks which are as follows:

A. Termination to ground requires a driver which can source a large current.
B. Termination to +5 requires a driver which can sink a large current. Implementing a standard TTL gate will not permit the line to be correctly matched. This also reduces the V_{IL} margin.
C. Termination to ground and +5 can be implemented. This adds components and also reduces the V_{IL} margin due to current the driver must sink in the low state.
D. Quite often there are several ends to terminate making end termination impractical.

A third technique using Schottky diode clamps was found to be not as effective as the series damping resistor approach.

MATRIX ROUTING

The interconnect scheme shown in Figure 8 is suggested to minimize cross talk within the memory array. The MK4104 pinout was constructed to permit optimum signal routing without impacting board area. Chip enable is routed near ground to minimize cross talk problems.

SIGNAL ROUTING CONSIDERATIONS

Care should be taken in the memory layout to avoid routing signals in a manner that could cause cross talk problems. Signal cross talk is directly impacted by spacing between signals, length of parallelism and proximity to ground. The number of signals switching simultaneously will also influence the amount of signal induced into an adjacent line. To avoid cross talk problems, the designer should avoid placing signals sensitive to noise spikes in close proximity to groups of signals simultaneously switching at inopportune times. Many memory designers can attest to redesigning boards for this reason alone. A situation of this type to avoid with the MK4104, would be positioning the chip enable etch, in the boards logic area, in the center of the twelve address lines, or in a group of data lines. This problem exists for all memory devices be they Edge Activated or not.

CONCLUSION

The Edge Activated component is unique in today's memory market. The high density, fast performance and very low power make it a very flexible part to utilize. The battery mode feature of the MK4104/4114 opens up multiple portability and battery standby applications. Potential uses cover the gamut from mainframe memories to small specialty applications in biomedical electronics or process control. The simple interface of the RAM makes it a natural choice for manufacturers requiring an easy to use part. Above all, the Edge Activated family is manufactured by MOSTEK CORPORATION whose products are among the most reliable in the industry.

Read-Only Memory

MOSTEK®

AN UPDATE ON MOS ROMS

By DAVID HUFFMAN

Technical Brief
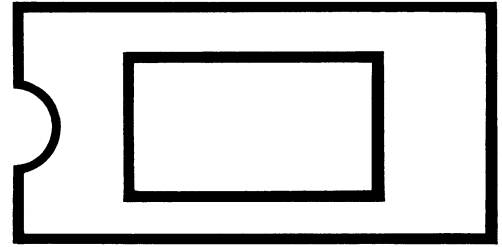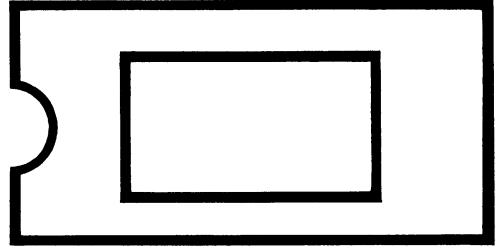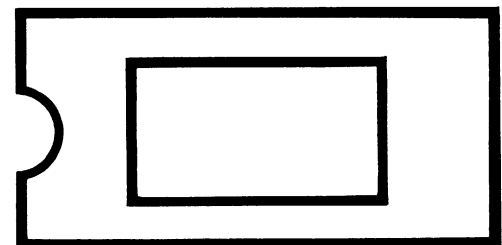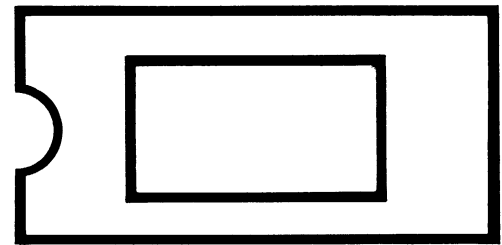
With today's faster, more powerful microcomputer chips emerging in abundance, and larger, more memory-intensive programs being written, semi-conductor memory requirements for larger storage capacities, faster access times, and lower subsequent costs have become dominant system design factors. Basic semiconductor memory-chip technology involves variations of random-access memory (RAM) and read-only memory (ROM). RAM allows binary data to be written in, and to be read out. New and different programs and data can be loaded and stored in RAM as needed by the processor. Because information is stored electrically in RAM its contents are lost whenever power goes down or off. When fixed, or unchanging, programs and data are needed by the processor, they are loaded into some form of ROM. In ROM, information is physically (permanently) embedded; therefore, its contents are preserved whenever power is off or interrupted momentarily.

Semiconductor memory chips are normally manu-factured using either bipolar or metal-oxide semicon-ductor (MOS) technologies. Bipolar and MOS memories implement bipolar transistor and MOS field-effect transistor (MOSFET) arrangements, res-pectively, to store addressable sequences of binary 1s and 0s. MOS memories are either static or dy-namic. Static memory depends on a dc level for operation; it is easier to implement in many cases, but requires more power. Dynamic memory requires clock signals or level changes for operation; thus more external circuitry may be needed. However, chip size and thus cost is reduced as is power dissipation.

Typically, ROM has been the limiting component in computer system design, operation, and manufac-turability. Problems like slow access time, high power dissipation, long prototype and production cycles, and lack of second sources have concerned computer system and equipment designers. This article sum-marizes the present MOS ROM state-of-the-art and describes the progress made by the semiconductor industry in manufacturing improved ROMs.

ROM TYPES AND PRINCIPLES

Major types of read-only memory (ROM) are: basic mask programmed ROM; electrically programmable, ultraviolet erasable (EPROM); electrically alterable (EAROM); electrically erasable (EEROM); and field

programmable (p/ROM). EPROM is electrically pro-grammable, then erasable by ultraviolet (UV) light, and programmable again. Erasability is based on the floating silicon gate structure of an n- or p-channel MOSFET. This gate, situated within the silicon dio-xide layer, effectively controls the flow of current between the source and drain of the storage device. During programming, a high positive voltage (nega-tive if p-channel) is applied to the source and gate of a selected MOSFET, causing the injection of electrons into the floating silicon gate. After voltage removal, the silicon gate retains its negative charge because it is electrically isolated (within the silicon dioxide layer) with no ground or discharge path. This gate then creates either the presence or absence of a conductive layer in the channel between the source and the drain directly under the gate region. In the case of an n-channel circuit, programming with a high positive voltage depletes the channel region of the cell; thus a higher turn-on voltage is required than on an unprogrammed device. The presence or absence of this conductive layer determines whether the binary 1-bit or the 0-bit is stored. The stored bit is erased by illuminating the chip's surface with UV light. The UV light sets up a photocurrent in the sili-con dioxide layer which causes the charge on the floating gate to discharge into the substrate. A transparent window over the chip allows the user to perform erasing, after the chip has been packaged and programmed, in the field. EAROMS use electrical pulses to clear all bits simultaneously.

The p/ROM has a memory matrix in which each storage cell contains a transistor or diode with a fusible link in series with one of the electrodes. After the programmer specifies which storage cell positions should have a 1-bit or a 0-bit, the p/ROM is placed in a programming tool which addresses the locations designated for a 1-bit. A high current is passed through the associated transistor or diode to destroy (open) the fusible link. A closed fusible link may represent a 0-bit, while an open link may rep-resent a 1-bit (depending on the number of data inversions done in the circuit). A disadvantage of the fusible-link p/ROM is that its programming is per-manent; that is, once the links are opened, the produced bit pattern cannot be changed.

Two other types of p/ROM that are not as prevalent in the industry, but deserve mention are EEROM and

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EAROM. The first, EEROM or electrically erasable ROM, works similarly to the "floating gate" EPROM but can be erased (all bits) by electrically pulsing the device. The EAROM or electrically alterable ROM utilizes special processing techniques that allow bit locations to be reprogrammed at any time. However, unlike a RAM, the write cycle is very long preventing its use as a non-volatile RAM where both read and write cycles are to be used. Both EEROM and EAROM are used mostly in specialized applications where nonvolatility and electrical erasability are requirements.

In mask-programmed ROM, the memory bit pattern is produced during fabrication of the chip by the manufacturer using a masking operation. The memory matrix is defined by row (X) and column (Y) bit-selection lines that locate individual memory cell positions.

For example, in Fig 1 refer to column C_2 and row 127 as the storage cell location of interest. When the proper binary inputs on the address lines are decoded, the cell at R_{127}, C_2 will be selected. If the drain contact of this cell is connected to bit line L^2, then L^2 will be pulled below threshold, turning off device C_2; note that devices C_0, C_1, and C_3 through C_{15} will also be off since they are not addressed. Therefore, device A pulls the OUT line to V_{cc} for a logic 1 output when cell R_{127}, C_2 is selected.

Alternatively, consider when cell R_{127}, C_2 is masked it does not have a drain contact to bit line L_2. Then when this cell is addressed, device C_2 is now connected to V_{cc} and will be turned on. Thus, the OUT line will be pulled to ground through device C_2 and will appear as a logic 0 output. To program a 1 or a 0 into a ROM storage cell, the drain contact will or will not be connected, respectively, to the particular bit line. Note that this type of programming is permanent. An alternative method of performing the same operation would be to eliminate the gate of the storage cell.

Typical ROM applications include code converters, look-up tables, character generators, and nonvolatile storage memories. In addition, ROMs are now playing an increasing role in microprocessor-based systems where a minimum parts configuration is the main design objective. The average amount of ROM in present microprocessor systems is in the 10K- to 20K-byte range, while some applications utilize as much as 30K or 40K bytes. Fig 2 shows a block diagram of a typical microprocessor system in which ROM is the predominant program storage element. In this particular application, the 16K ROM is used to store the control program that directs CPU operation. It may also store data that will eventually be output to some peripheral circuitry through the CPU and the peripheral input/output (P I/O) device.

PORTION OF ROM MATRIX AND OUTPUT CIRCUITRY OF MK 34000
Figure 1
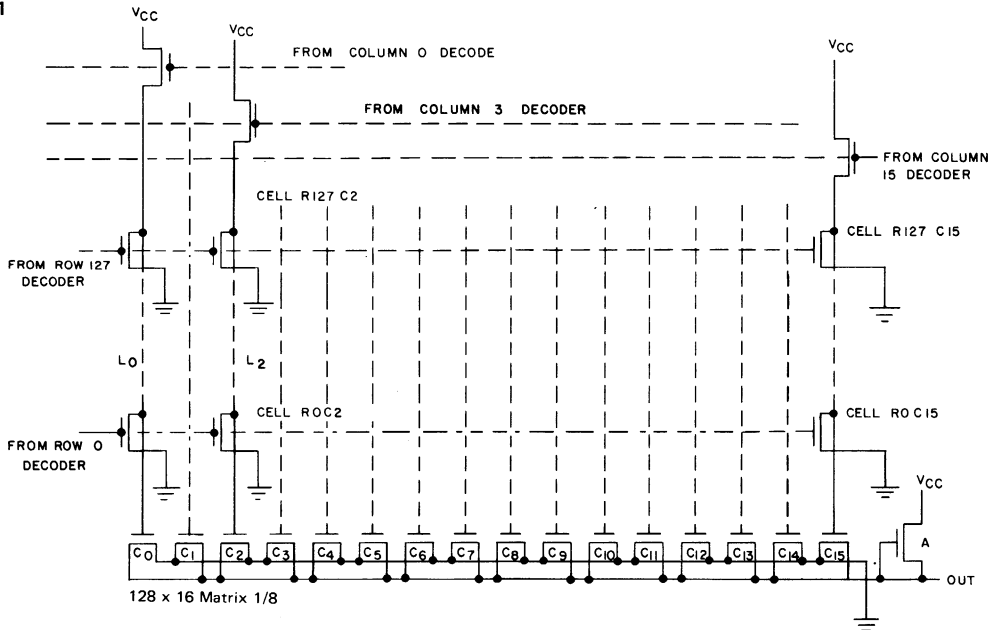
If drain contact is made (1 state) when particular cell is accessed, storage transistor will cause OUT line on device A to pull high (to Vcc). If contact is not made to drain, device will pull OUT line low (0 state).

SYSTEM DEVELOPMENT CYCLE

In a microprocessor system development cycle, several types of memory (RAM, ROM, and EPROM or p/ROM) are normally used to aid in the system design. After system definition, the designer will begin developing the software control program. At this point, RAM is usually used to store the program, because it allows for fast and easy editing of the data. As portions of the program are debugged, the designer may choose to transfer them to p/ROM or EPROM while continuing to edit in RAM. Thus, he avoids having to reload fixed portions of the program into RAM each time power is applied to the development system.

Decision making on the part of designer and manufacturer is required during the next step in the development cycle. Depending on the type and quantity of microprocessor systems to be produced, a decision has to be made as to whether ROM, p/ROM, or EPROM will be used for permanent program storage. If only a few systems are to be manufactured, it may be more cost-effective to use either p/ROM or EPROM. EPROM-based storage also allows the main program to be changed at any time, even in the field by the end-user. The p/ROM-based system requires replacement; however, it is field programmable. If the main requirement is a minimum parts configuration and many microprocessor systems must be produced the decision should be to use ROM-based storage.

For many designs, fast manufacturing turnaround time on ROM patterns is essential for fast entry into system production. This is especially true for the consumer "games" market. Several vendors now advertise turnaround times that vary from two to six weeks for prototype quantities (typically 25 pieces) after data verification. Data verification is the time when the user confirms that data have been transferred correctly into ROM in accordance with the input specifications.

Contact programming is one method that allows ROM programming to be accomplished in a shorter period of time than with gate mask programming. The step-by-step ROM manufacturing process is listed in Table 1. N-MOS ROMs go through basically the same processing steps. In mask programming, most ROMs are programmed with the required data bit pattern by vendors at the first (gate) mask level, which occurs very early in the manufacturing process. In contact programming, actual programming is not done until the fourth (contact) mask step, much later in the manufacturing process. That technique allows wafers to be processed through a significant portion of the manufacturing process, up to "contact mask". and then stored until required for a user pattern. Some vendors go one step further and program at fifth (metal) mask. This results in a significantly shorter lead time over the old gate-mask-programmable time of 8 to 10 weeks; the net effect is time and cost savings for the end user.

MICROPROCESSOR BLOCK DIAGRAM

Figure 2
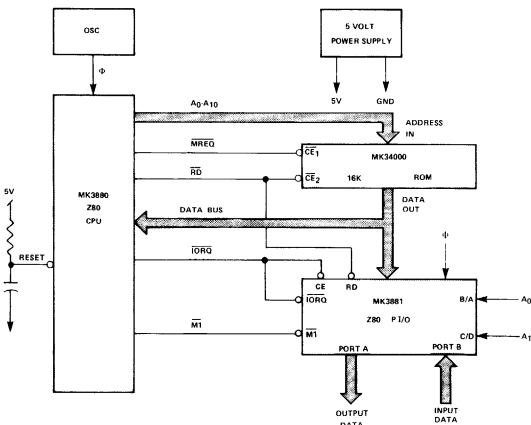
Typical microprocessor system utilizes CPU, P I/O, and 16K ROM.

MOS ROM MANUFACTURING PROCESS FLOW

Table 1

Wafer
Oxidation
Nitride
First Mast
(Gate Mask)
Etch
Second Mask
Implant
Polysilicon
Third Mask
Oxidation
Fourth Mask
(Contact)
Etch
Metallization
Fifth Mask
Glassification
Sixth Mask
Test
Assemble
Ship

Time Saved In
ROM Turnaround
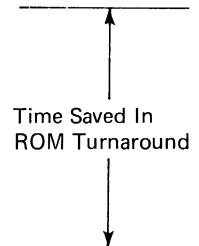
ROM VS DISCRETE LOGIC COSTS
Table 2

ROM Capacity (Total Bits)	ROM Cost	Functional IC Gates	ICs	Estimated IC Dollars
8K	$7 to 8	500 to 999	50 to 99	$20 to 39
16K	$8 to 9	1000 to 1999	100 to 199	$40 to 79
32K	$16*	2000 to 3999	200 to 399	$80 to 159
64K	$20*	4000 to 7999	400 to 799	$160 to 319

*Projected cost

COST CONSIDERATIONS

Consider a typical microprocessor system and what ROM can provide in terms of cost savings over discrete logic and EPROM. Assume that a single gate function can be replaced with eight to ten bits of ROM and that most of today's transistor-transistor logic (TTL) integrated circuits (ICs) contain on the order of ten functional gates having an average selling price of $0.40. The typical microprocessor system contains 20K bytes of ROM. Table 2 compares the costs of ROM versus discrete logic.

From the table, one 16K (2048 x 8-bit) ROM can replace 100 to 200 TTL packages. Depending on the total quantity of ROMs required, it can be seen that they are a cost-effective alternative to discrete logic.

Additional savings are possible when ROM is used. Board area is reduced, which lowers material cost; fewer packages reduce insertion costs; and, with smaller boards and fewer interconnections, the cost of incoming inspection is also decreased. When board troubleshooting costs go down, overall system reliability increases.

At this time, the largest cost-effective EPROM size available is 1024 x 8 bits or 8192 total bits. However, there are many 2048 x 8 bit, or 16K ROMs available. At an average selling price of $16/EPROM and $8/ROM, it is evident that ROM remains the most cost effective solution. For every two 8K EPROMs, only one 16K ROM is needed. The disadvantage of ROM in small quantities is the mask charge (usually $500 to $1000). In larger production quantities, the mask charge is waived when a minimum number of parts have been purchased (typically 500 to 1000 pieces/pattern).

KEY PERFORMANCE

With faster and more powerful microprocessors entering the market, ROM performance is more important than ever, especially since ROM has typically been the limiting factor in system processing speed and operation. When 16K ROMs were introduced several years ago they were fairly slow, with access times ranging from 550ns to well over 1.0 μs. These ROMs made it difficult to take advantage of the full speed capability of newer microprocessors. If processing speed was paramount, the designer usually selected bipolar ROMs, which possess fast speed but have high power dissipation. Density costs are also higher.

Newer MOS ROMs (such as the MK34000, and and 36000) provide the system designer with both speed and density. Access time is 300ns worst case, specified over the full power supply and temperature ranges. In addition, since many microprocessors now have only a single power supply requirement (5V), the trend in 16K,/32K/64K ROM designs is also slanted to this single voltage. Most vendors offer a ±5% supply voltage tolerance and at least one specifies ±10%.

OTHER PARAMETERS

Many ROM-based memory applications are subject to various detrimental environmental conditions. For instance, an intelligent data entry terminal used on a busy outdoor loading dock could be exposed to vibration-generated electrical noise, extreme temperature variations from −20 to 125°F (−28 to 51°C), machine-generated noise, and power line fluctuations. Critical ROM parameters, such as temperature range, input levels, output drive, power supply tolerance, and power dissipation, are being accommodated by innovative memory design and processing techniques to optimize performance and reliability.

Extensive use of ion implantation as a means of controlling circuit zero bias threshold voltages is now prevalent. One ROM vendor uses a substrate bias generator, often called a charge pump which results in much wider operating tolerances. Input levels of 2.0V, ±10% power supply tolerances, wider operating temperature ranges, faster access times, and lower power dissipation are now available.

Important data sheet parameters that a designer should examine when specifying ROMs are listed in Table 3. Of course, which parameters are important to the individual designer depends entirely on the application. In the loading dock example cited previously, temperature range may be the most critical. In a military airborne application, temperature range and power dissipation would be most important.

IMPORTANT DATA SHEET PARAMETERS
Table 3

General

Absolute maximum voltage ratings — voltages beyond which parts are likely to be destroyed

Absolute maximum temperature — operating and storage temperatures beyond which parts may be permanently damaged

"Recommended" operating conditions— operating conditions that the manufacturer requires for proper operation

DC parametrics— current and voltage parameters at specified conditions

Timing diagrams — part timing specifications essential for system design

Capacitance specifications — particular input and output specifications required to avert drive problems

Package specifications— pin-outs and package mechanical data for layout and environmental requirements

Specific

Voltage and current levels — input and output low and high voltage and current levels on all inputs and outputs

Power supply regulation — detailed power supply regulation specifications

Output capacitance test value — this value determines maximum number of parts which can be strung together and still meet specifications

Standby and output leakages

Input and output leakages

Timing parameters — all timing parameters required to totally specify system operation

Input methodologies — ROM's truth table should indicate accepted input methodologies including card, tape, or transmit formats

Operating temperature specifications — should allow for proper system margins after enclosure temperature rises are taken into account

CHARGE PUMP TECHNIQUE

Although the ROM charge pump technique has been utilized for several years, a new design approach has evolved (Fig 3). The charge pump is an on-chip bias generator that is used to shift the thick-field thresholds (V_T) to their proper operating levels, as well as to reduce junction capacitance of the circuit. In dynamic RAMs, an external V_{BB} power supply is used for this purpose. This fixed value bias is useful, as such, but it does not compensate thresholds over temperature. In the MK34000 and 36000 ROMs (16K, and 64K respectively), the charge pump approach does temperature compensate for thresholds by utilizing a method of V_T feedback. A threshold detector compares V_T values of the circuit with an on-chip voltage reference (V_R). Significantly, V_R is always a fixed percentage of the V_{CC} supply rather than being V_T dependent. Normally, the V_{CC} supply can be held constant over a specified temperature range; thus, the reference will also remain constant, keeping V_T constant. Even if the supply voltage changes, the reference voltage will cause the effective V_T to be within its operating range for a particular supply potential.

The bias generator is actually an on-chip gated oscillator (A) that, when operating, "charges up" the substrate capacitance of the chip with a negative potential. The threshold detector will turn the oscillator on or off if it detects either an inequality or an equality, respectively, of V_R and V_T. This is especially important for V_T versus temperature. Typically, as temperature goes up. V_T goes down; with normal process tolerance included in the total V_T, this could severely limit the allowable specified levels and temperature range. The threshold detector is sufficiently accurate so that it can compensate for small changes in V_T during normal operation of the part. Fig 4 shows the behavior of V_T, V_{BB}, and compensated V_{TC} over an extremely wide temperature range. The outstanding feature of the compensated V_T curve, is that it is flat over a significant range in temperature. It can be shown that the overall effect is an improvement in system margins, improved yields, and reliability. This is all possible with no increase in chip size and an insignificant increase in power supply current (typically 1 mA).

SYSTEM RELIABILITY

Replacing many random logic circuits with a single MOS ROM not only makes good economic sense, but also significantly increases reliability. Printed circuit (PC) board area is reduced along with a multitude or system interconnections. It is possible for a single ROM to eliminate 2000 interconnections when bonding wires and PC board etches are taken into account. This means fewer chances for opens, shorts and layout problems. When using ROMs, troubleshooting is
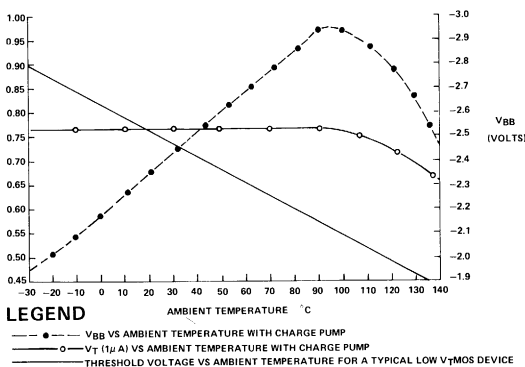
ON-CHIP SUBSTRATE BIAS GENERATOR
Figure 3

THRESHOLD DETECTOR — ON/OFF → OSCIL-LATOR

V_{CC}

SUBSTRATE DIODE

SUBSTRATE

V_{BB}

C_1

(B)

A

1

2

3

4

CORRECTION VOLTAGE

C_S

LEAKAGE

ON-CHIP (A) OSCILLATOR

SUPPLY VOLTAGE (V_{CC})

BIAS VOLTAGE (V_{BB})

REFERENCE VOLTAGE (V_R)

THRESHOLD VOLTAGE (V_T)

TURN-ON REGION

DRIFT REGION
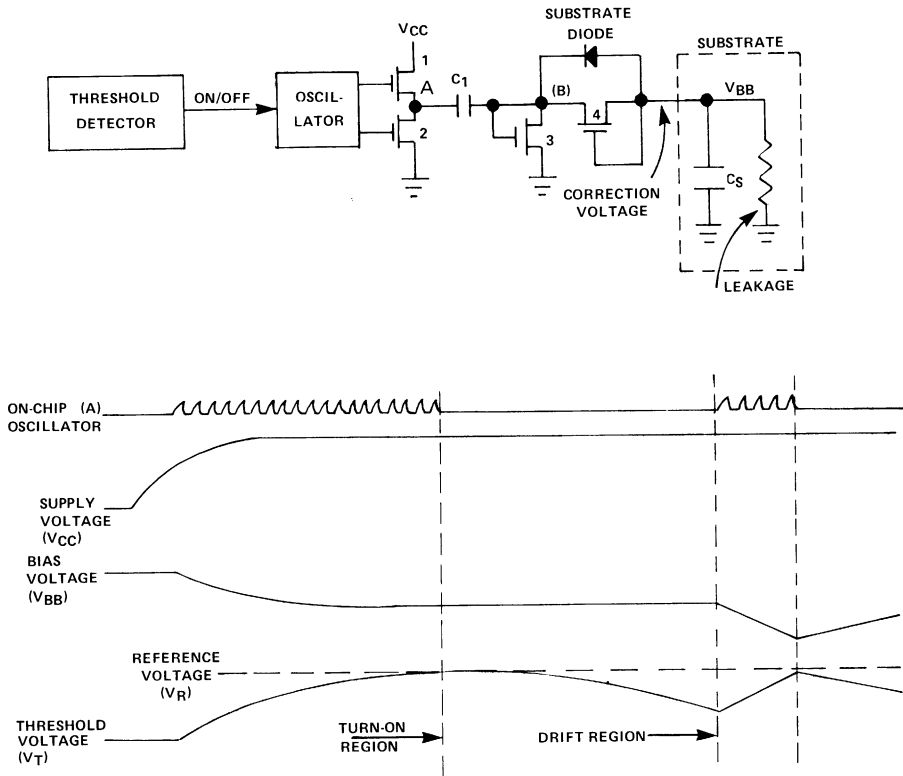
Simplified circuit diagram of an on-chip substrate bias generator which utilizes a method of V_T feedback. Circuit will only generate a negative bias when V_T does not equal reference voltage. When operating, circuit draws a minimum amount of power while requiring no additional layout space on chip.

OPERATING MARGINS
Figure 4

1.00
0.95
0.90
0.85
0.80
0.75
0.70
0.65
0.60
0.55
0.50
0.45

−3.0
−2.9
−2.8
−2.7
−2.6
−2.5
−2.4
−2.3
−2.2
−2.1
−2.0
−1.9

V_{BB} (VOLTS)

−30 −20 −10 0 10 20 30 40 50 60 70 80 90 100 110 120 130 140

AMBIENT TEMPERATURE °C

LEGEND

— ● — V_{BB} VS AMBIENT TEMPERATURE WITH CHARGE PUMP
—o— V_T (1μA) VS AMBIENT TEMPERATURE WITH CHARGE PUMP
——— THRESHOLD VOLTAGE VS AMBIENT TEMPERATURE FOR A TYPICAL LOW V_T MOS DEVICE

By comparing curves showing V_T versus ambient temperature for circuit with and without substrate bias generator, it can be seen that operating margins of a noncompensated device may be quite limited. By utilizing V_T feedback method of device operation, V_T can be held constant over significantly wide temperature range. Plot also shows V_{BB} versus temperature with generator operational.

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simplified because there are fewer components, interconnects, and contacts.

In addition, vendors have learned techniques for lowering the power supply current requirements of ROMs. One method utilized is a static matrix with dynamic or "edge activated"* control circuitry. The MK36000 ROM, for instance, draws a typical average current of only 40mA, compared with 80mA typical of a comparable density totally static device. When supply current is low, chip temperature is low and reliability is enhanced.

Many vendors now offer enhanced reliability screening as an option. This screening may include temperature cycling for detecting die- and bond-related problems, and also fine and gross hermeticity testing. In addition, many offer an option on burn-in to weed out infant mortalities. Extended temperature range 16K ROMs are available, as well as devices processed to MIL-STD-883A, Level B. Table 4 lists the 100% screening requirements called out by this specification. While this screening has historically been reserved for military applications, more users are requiring it as a matter of course. Screening of this type means that the user receives the highest reliability possible in his parts.

SCREENING REQUIREMENTS SPECIFIED FOR MIL-STD-883, CLASS B   Table 4

Test	Method	Condition	Test Level
Visual	2010.2	Condition B	100%
Stabilization Bake	1008.1	Condition C 24h at 150°C	100%
Temperature Cycle	1010.1	Condition C −65 to 150°C 10 cycles	100%
Centrifuge	2001.1	Condition E 30k Gs Yl Plane	100%
Hermiticity Fine	1014.1	5×10^{-8} Atm-cm^3/s	100%
Gross	1014.1	Condition C	
Pre-Burn-In Electrical Test	Static and Dynamic Tests		Mfg's Option
Burn-In	1015 (Dynamic Operating)	Condition D 160 h min at TA=125°C	100%
Final Electricals	Static and Dynamic per Data Sheet		100%
Quality Conformance	See Mfg's Quality Specification		Sample
External Visual	2009		100%

COMPARISON OF SEVERAL AVAILABLE 16K ROMs   Table 5

Parameter	Mostek MK34000	American Micro Systems S6831B	General Instruments R03-9316A/B	Intel 12316E/8316E	Motorola 68316E	Synertek 2316B
Input Voltage High (V_{IH}) Low (V_{IL})	2.0 V min 0.8 V max	2.0 V min 0.8 V max	2.2 V min 0.65 V max	2.4 V min 0.8 V max	2.0 V min 0.8 V max	2.0 V min 0.8 V max
Output Voltage High (V_{OH}) Low (V_{OL})	2.4 V at 220μA 0.4 V at 3.3 mA	2.4 V at 100μA 0.4 V at 2.1 mA	2.2 V at 100 μA 0.45 V at 1.6 mA	2.4 V at 400μA 0.4 V at 1 mA	2.4 V at 220μA 0.4 V at 1.6 mA	2.4 V at 200μA 0.4V at 2.1 mA
Power Supply Current (I_{CC}) OUtput Leakage Current	60 mA max 30 mA typ 10 μA	TBD max 30 mA typ 10 μA	110 mA max 90 mA typ 10 μA	120 mA 10 μA	130 mA 10 μA	98 mA max Typ 10 μA
Input Leakage Current	10 μA	2.5 μA	10 μA	10 μA	2.5 μA	10 μA
Power Supply Voltage	5 V ±10%	5 V ±5%	5 V ±5%	5 V ±5%	5 V ±5%	5V ±5%
Access Time Referred to Addresses	350 ns	450 ns	450 ns	450 ns	500 ns	450 ns
Chip Select To Output Delay Time	175 ns	200 ns	200 ns	120 ns	300 ns	250 ns
Chip Deselect To Output Delay Time	150 ns	150 ns	200 ns	100 ns	175 ns	250 ns
Operating Temp Range	0 to 70°C	0 to 70°C	0 to 70°C	0 to 70°C	0 to 70°C	0 to 70°C
Extended Temp	Yes	Yes	Yes	NA	Yes	NA

STANDARDIZATION

Standardization has resulted in several important advantages. Previously, different pin-out images, various data input formats and media, and different circuit operating modes made system design difficult. ROM vendors have now realized that future product upgrading has significant market value. Also, products that have a second source are more likely to succeed in the highly competitive memory market.

At the present time there are 1024 x 8 and 2048 x 8 bit EPROMs, 1024 x 8 ROMs, 2048 x 8 ROMs, and the newer 4096 x 8 and 8192 x 8 bit ROMs. All vendors sourcing these devices have chosen a standard pin-out configuration (Fig 5) to ease the designer's task in system upgrading.

PIN-OUT SEQUENCES
Figure 5
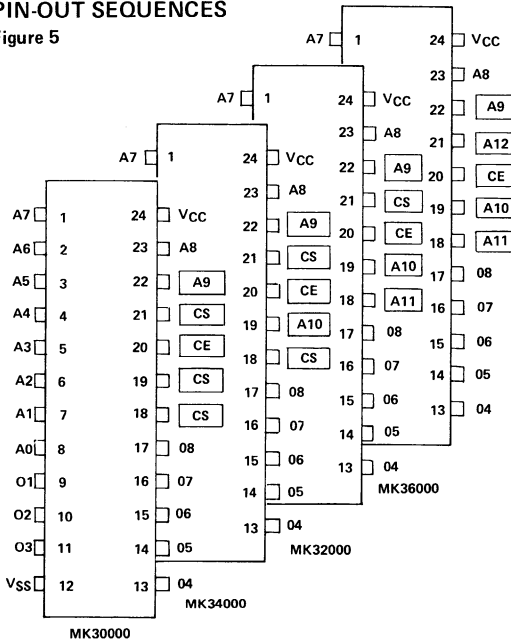
Manufacturers of 8K and larger density MOS ROMs have standardized their pin-out sequences. Significance of these pin images is that they are upgrade pin-compatible with presently available 1024 x 8 and 2048 x 8 EPROMs.

A designer that implements a standard 8K or 16K EPROM can easily change to an 8K, 16K, 32K or 64K ROM by simply using strap options on his standard board. A change from an 8K EPROM to an 8K ROM involves only opening the V_{BB} supply line to pin 21, opening the V_{DD} supply line to pin 19, and altering the function of pin 18 from PROGRAM to CS/$\overline{CS}$ (see Fig 6). This can be done on either the ROM or the card edge connector. The N/C (no-connect) option available on some 8K ROMs makes even this unnecessary. Upgrading to larger ROMs involves interchanging chip selects and address lines.

Second sources are now plentiful. While performance compatible ROMs are not always available, vendors are making progress along these lines. Some of the presently available 8K and 16K EPROM pin-compatible ROMs are analyzed in Table 5. The point of the analysis is that the devices listed are basically similar with the same pin-out, method of operation, and general characteristics. Not only do the manufacturers benefit but so do the users.

Standard input formats and media for ROM data have been problem areas. Not long ago, a vendor would accept data only in his format (ie, hexadecimal or octal) and only on card decks. Now virtually any form of transferring data is acceptable. For example, data have been transferred to ROM from media as diverse as telephone data links, EPROMs, and paper tapes. Table 6 lists some examples of the currently available methods of media data transfer. As can be seen from this table, the designer may put his ROM data into essentially any form. The possibility of error is reduced because no conversions of the data need be made to other media to accommodate different vendors.

ACCEPTABLE FORMAT AND MEDIA FOR INPUT OF ROM DATA
Table 6

Format	Media
Mostek	Card Deck
National	Paper Tape
Fairchild	ROM
Intel Card	p/ROM
Intel Tape	Data Link
Electronic Arrays	
Mostek F8	
Motorola 6800	

CONCLUSIONS

Turnaround time has been reduced to a tolerable level, pin-outs are being standardized, ROMs are providing larger memory capacity with higher performance, and data are more easily transferred. In the future, the greatest number of applications will most likely be in microprocessor systems. Microprocessor memory requirements continue to increase as control programs get larger and applications become more sophisticated. Concurrently the microprocessor is becoming higher performance with more control capability, as witnessed by recent 16-bit high speed devices. Today's new generation MOS ROMs are being designed to interface directly and easily while occupying a minimun of space. The importance and necessity of ROMs to system design have resulted in a continual effort by the semiconductor industry to improve performance, reliability, and cost.

EPROM AND ROM PIN CONNECTION COMPATIBILITY
Figure 6

64K ROM
32K ROM
16K ROM
8K ROM

Left side (8K ROM / 16K ROM / 32K ROM / 64K ROM = SAME for all):

Left column	EPROM Pin	Pin #
SAME	A_7	1
SAME	A_6	2
SAME	A_5	3
SAME	A_4	4
SAME	A_3	5
SAME	A_2	6
SAME	A_1	7
SAME	A_0	8
SAME	O_1	9
SAME	O_2	10
SAME	O_3	11
SAME	V_{SS}	12

8K EPROM (center)

Pin #	EPROM	8K ROM	16K ROM	32K ROM	64K ROM
24	$-V_{CC}$	SAME	SAME	SAME	SAME
23	$-A_8$	SAME	SAME	SAME	SAME
22	$-A_9$	SAME	SAME	SAME	SAME
21	$-V_{BB}$	CS/NC	CS/NC	CS/NC	A_{12}
20	$-CS/WE$	CS/NC	CS/NC	CE	CE
19	$-V_{DD}$	SAME/NC	A_{10}	A10	A_{10}
18	$-PROGRAM$	CS/NC	CS/NC	A_{11}	A_{11}
17	O_8	SAME	SAME	SAME	SAME
16	O_7	SAME	SAME	SAME	SAME
15	O_6	SAME	SAME	SAME	SAME
14	O_5	SAME	SAME	SAME	SAME
13	O_4	SAME	SAME	SAME	SAME

Virtually all pin connections are same for an 8K EPROM through a 64K ROM. Significant difference occurs on the EPROM V_{BB}, V_{DD}, and program pins. These pins in ROM are either CS/$\overline{CS}$ functions or address inputs with some manufacturers allowing no-connect options. With N/C option, EPROM can be directly replaced by ROM with no circuit change, except when using 16K or larger.

MOSTEK®

MINIMIZING THRESHOLD VOLTAGE TEMPERATURE
DEGRADATION WITH A SUBSTRATE BIAS GENERATOR

By DAVID HUFFMAN/DENNIS SEGERS/BOB GREEN

Application Note

As with any MOS circuit, tight controls must be maintained on process parameters to insure that performance and reliability are maximized. This is important not only to a semiconductor manufacturer but to the user as well. The dependence of proper operation on processing is more critical in today's advanced N-channel circuits than in older generation P-channel circuits. This partially accounts for the limited manufacture of N-channel in the early history of MOS technology. Through research and experience, it has become possible to manufacture highly reliable and good performance N-channel circuits with a fair degree of consistency.

There are still, however, problems that are intrinsic to MOS circuitry that are difficult to compensate for by just controlling process parameters, in particular temperature variations. In Mostek's MK30000/MK-34000 and MK36000 (8K/16K and 64K ROMs respectively), a circuit has been incorporated with the standard design that has minimized process and temperature dependence. This circuit called a substrate bias generator, compensates for variations in the threshold voltage due to temperature excursions, aging and other conditions. While the substrate bias generator is and has been utilized on various circuits, the approach used by Mostek presents an innovative departure from the old idea.

Threshold Voltage

One of the most critical parameters in an N-channel MOS circuit is threshold voltage (V_T), or the minimum voltage potential required to be applied to the gate of an MOS device to turn the device on. Threshold voltage can be defined by the following set of equations:

Eq. 1
$$V_T = V_{FB} + 2\phi_B + \sqrt{\frac{2E_s\, q\, N_A\, (2\phi_B)}{Co}}$$

Where $V_{FB} = \phi_{ms} + \dfrac{Q_{fs}}{Co}$

$$\phi_B = \frac{kT}{q} \ln\left(\frac{N_A}{ni}\right)$$

ϕ_{ms} = metal/silicon work function
Q_{fs} = surface charge density/unit area
Co = gate capacitance/unit area

The term Q_{fs} can also be divided into several components that will help to show how it is process dependent. It would include a term for the fixed surface charge on the Si/Si O_2 interface -Q_{ss}, a term for oxide ion contamination -Q_s and also some secondary terms which have only minor effect. Table I summarizes how each term is affected by the process.

Table 1

PARAMETER	PROCESS
N_A	Impurity concentration in gate region.
ϕ_{ms}	Gate metal (poly silicon/aluminum)
Q_{fs}	Crystal orientation, oxide growth technology, mobile gate oxide contamination, oxide charge due to ionization.
Co	Gate oxide thickness, density of dielectric.

Many different process techniques have been developed over the past few years to better control each of the above terms, so that any chosen optimum V_T can be as reproducible as possible. Mostek for example, pioneered the use of ion-implantation as a means of controlling the N_A term. Utilizing a 1-0-0 crystal orientation which has the lowest number of surface states on the Si/Si O_2 interface will minimize the Q_{fs} term. However, it is still very difficult to maintain a high percentage of the threshold distribution at the desired value. In a production environment a V_T distribution of ± 250mV is generally considered to be good.

This situation presents the MOS designer with a number of problems. He must take into account the fact that the V_T's as well as other important parameters will vary considerably from their ideal values. The design must be done on a basis of worst case conditions. Therefore, the designer is forced into a trade-off position between an ideal speed-power product and circuit stability. Obviously a superior circuit design would be achievable if the designer was assured that the V_T's would always be at their optimum values over the specified operating conditions in a system.

To the system designer, threshold voltage manifests itself in many ways in the actual operating characteristics of the circuit. Input high and low levels are directly dependent upon V_T. This in turn will determine noise margins of the circuit. Power supply tolerances and output drive capability also depend on thresholds. Due to the intrinsic dependence of V_T with temperature, the operating temperature range of a circuit and in turn the system is limited.

It is evident that if thresholds could be maintained at their optimum values regardless of process variations and temperature excursions, a superior I.C. is

possible. As a consequence the system designer is given the greatest latitude in his design tolerances.

Controlling Thresholds with V_{BB}

Controlling Thresholds with V_{BB}

The effective threshold voltage of a MOS device can be shifted from the process controlled value defined in Eq. 1 in the following manner:

Eq. 2 $\qquad V_{T\,eff} = V_T + \Delta\, V_T$

The ΔV_T term is caused by the addition or substraction of an electric field at the gate region, which is generally due to some negative potential applied to the substrate of the circuit. This potential is commonly known as back bias or V_{BB}. In dynamic RAMs for instance, a typical V_{BB} of -5 volts is used in order to shift thickfield thresholds to higher values and to reduce junction capacitances. However, until recently, the idea of making V_{BB} variable in order to precisely control thresholds has been overlooked. Mostek has utilized this idea in all of its new ROM designs by means of an on chip substrate bias generator. This bias generator, or "charge pump" as it is often called, is capable of supplying between -.5V to -3.5V to the substrate in order to maintain thresholds at their most desirable levels. Since V_{BB} is generated internal to the device, many of the problems associated with an external V_{BB} supply are avoided. Generally an external supply has to be well regulated and may require a special sequencing with the other supplies used. If this external V_{BB} supply is lost, the circuit may become catastrophically damaged or the longterm reliability can be adversely affected.

CHARGE PUMP
Figure 1
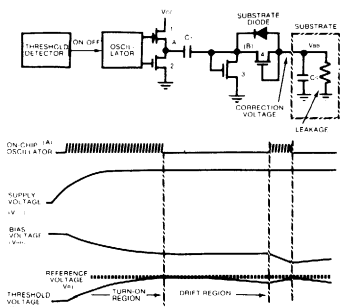
The charge pump is actually a gated oscillator which is controlled by a threshold detector. (See Figure 1) The threshold detector compares the thresholds of the circuit with an on chip voltage reference (V_R). This reference is not threshold dependent; rather, it is a voltage which remains at a fixed percentage of the V_{CC} power supply.

The operation of the charge pump can be understood by a careful examination of the power-up sequence illustrated in the left portion of Figure 1. When the V_{CC} supply is first turned on the threshold detector compares the unbiased V_T's (threshold voltage at V_{BB}=OV) with the reference voltage V_R. The unbiased

V_T's are set by the process at about .5 volts below the optimum value. The threshold detector sees this difference and turns on the oscillator. The substrate voltage will go more negative each time the charge from C_1 is dumped into C_s (the substrate capacitance).

During the first part of the cycle, device 1 turns on pulling node (A) to V_{CC} while node (B) is held approximately at V_T. The second part of the cycle, node (A) is pulled to ground by device 2. This forces node (B) below the V_{BB} node. Device 4 conducts and puts more charge on the substrate capacitor C_s. As V_{BB} goes more negative, the effective thresholds begin to rise correspondingly. When V_{BB} reaches a magnitude sufficient to raise $V_{T\,eff}$ to its desired value, the threshold detector turns off the oscillator.

During normal operation, substrate leakage will tend to decrease V_{BB} and thus $V_{T\,eff}$. The threshold detector however is sufficiently accurate that it can see these small changes and again activate the oscillator in order to bring $V_{T\,eff}$ back to its nominal level. This is shown in the right half of Figure 1.

Advantages of the Charge Pump

The advantages of a charge pump should be obvious. Because thresholds are no longer entirely dependent upon process parameters, much tighter V_T distributions are possible. Instead of V_T spreads of 400mV-500mV the circuit designer can expect to see distributions as tight as $\pm$ 25mV. To the user this means much wider operating tolerances while maintaining optimum performance in the circuit.

THRESHOLD VOLTAGE VS. AMBIENT TEMPERATURE FOR A TYPICAL LOW V_T MOS DEVICE

THRESHOLD VOLTAGE VS. AMBIENT TEMPERATURE FOR A TYPICAL LOW V_T MOS DEVICE

Figure 2
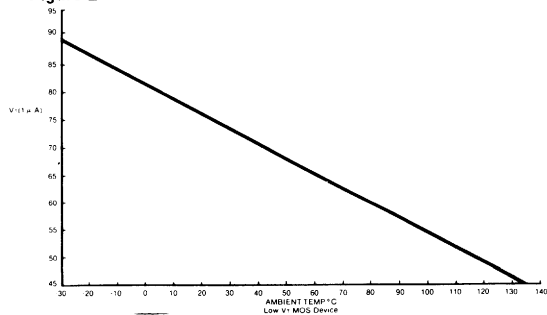
The most important aspect of the charge pump is how it compensates $V_{T\,eff}$ over temperature. All MOS circuits exhibit degrading characteristics as the ambient temperature varies. This is primarily due to the intrinsic dependence of V_T upon temperature. Virtually every term in Eq. 1 has some linear or logarithmic temperature dependence. The overall effect of this is illustrated in Figure 2. It appears as a linear decrease of V_T with increasing temperature at an approximate 2.7mV/°C rate. The limit to the operating range of a circuit can occur when the device thresholds shift to such an extent that either a DC level problem occurs within some critical inverter stage or the device no longer meets the required input or output levels.

VT (1μA) VS. AMBIENT TEMPERATURE WITH CHARGE PUMP
Figure 3
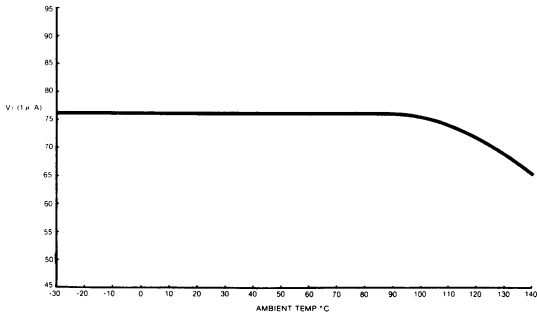
Figure 3 illustrates how the charge pump helps to overcome the problem. The data shown represents values typical of measurements taken from several manufacturing lots of the MK34000. Thresholds were found to be virtually constant from -35°C (the lower temperature limit of the experiment) up to about 95°C. Beyond 95°C, substrate leakage began exceeding the current capability of the charge pump. As a result V_T's begin falling at a rate close to the 2.7mV/°C typical of any low threshold MOS device. Figure 4 illustrates how V_{BB} varied with temperature in order to maintain the V_T's shown in Figure 3.

VBB VS. AMBIENT TEMPERATURE WITH CHARGE PUMP OPERATIONAL
Figure 4
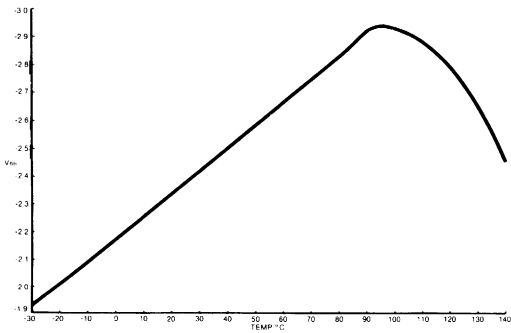
The real significance of the above is best seen when comparing Figures 2 and 3 on the same plot along with the limits of the distributions. This is graphically shown in Figure 5. A typical low V_T MOS device might be capable of operating over a range of thresholds from .40V to 1.05 volts. If an MOS circuit could be designed and processed repeatedly with ideal thresholds, the operating temperature range would be very wide. Since it cannot be done that accurately and consistently the operating temperature is more limited as shown by the typical MOS curve in Figure 5. For example, if it is assumed the device will not properly operate outside the .40V to 1.05V V_T range, then the device will only operate from -6°C to +87°C. Outside of this range, the processing tolerances of the non-charge pump part do not allow proper operation.

As can be seen in Figure 5, with the charge pump working, V_T is much tighter around the nominal value.

COMPARISON OF THRESHOLD DISTRIBUTIONS FOR A TYPICAL MOS DEVICE WITH AND WITHOUT A CHARGE PUMP
Figure 5
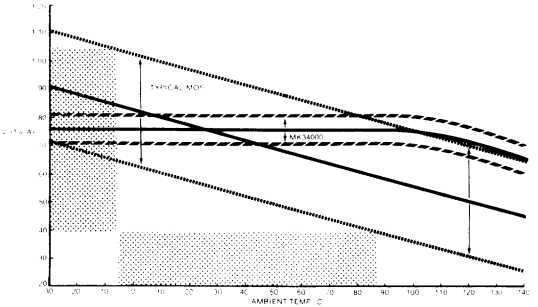
Even with large variations in the no bias V_T, the pump sufficiently compensates to keep $V_{T\,eff}$ well within its operating tolerances over a wide range in temperature. This means the circuit can be expected to operate over a much wider temperature limit with no significant change in V_T.

The result is the charge pump has its greatest effect on the input levels of a circuit. It allows the designer to process the circuit to a V_T level that gives the best speed/power product commensurate with the TTL level inputs. In a normal production situation on an uncompensated device, the thresholds would have to be set artificially high to allow for process and temperature tolerances on V_T. The following shows how the charge pump effects this situation.

In an MOS device, the lower limit that can be tolerated on V_T is determined by the input low level. On a 5 volt only ROM such as the MK 34000, the lower limit on V_T is set at .5 volts. This number is the lowest V_T tolerable for proper operation of the part. The upper limit to V_T can be determined by the following equations.

EQ 3 $V_{TNOM} = V_{T\,lower\,limit} + \Delta V_{TT} + V_P$

EQ 4 $V_{Tupper} = V_{TNOM} + \Delta V_{TBE} + \Delta V_{TT}$
where V_{TNOM}=Nominal V_T excluding tolerances

V_P=Process tolerance of V_T

ΔV_{TBE}=Change in V_T due to body effect

ΔV_{TT}=Change in V_T due to temperature

In Eq 3 the nominal V_T will be set by the lower limit of V_T plus whatever process and temperature tolerances have to be allowed for. Using the numbers mentioned before, where V_P= ± 250mV and ΔV_{TT}= -300mV (over

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range of -55°C to + 125°C centered at R.T.), it can be seen that V_T nominal is 1.05V. The upper limit to V_T would be 1.05V plus V_P (250mV) and ΔV_{TT} (200mV) or a total of 1.5V. The designer in this case would have to set the process V_T to 1.05 volts and design the circuit to operate over a range of .5 volts up to 1.5 volts.

This in itself may not be an unsolvable problem, however, the ΔV_{TBE} term has been neglected. At the upper level of V_T a problem occurs with the output high level. Equation 5 shows why.

EQ 5 V_{OH} max= V_{CC} - V_{Tupper} - ΔV_{TBE}

where V_{CC}= 5 volts ± 10%

V_{Tupper}= 1.5V

If V_{CC} is taken to be at the lower tolerance (4.5V) and V_{Tupper}=1.5 volts then ignoring the ΔV_{TBE} term puts the maximum output high level at 4.5 volts -1.5V or 3.0 volts. By the time the body effect term is subtracted, the level may be below 2.0 volts which is unacceptable in a TTL compatible product.

By going thru the same analysis with the charge pump operational, and using the following numbers for V_P and ΔV_{TT}, it can be shown that the process V_T can be set at a much lower level than before.

V_P= ± 50mV

ΔV_{TT}= ± 100mV

This fact helps to optimize the speed power/product of the circuit while allowing true TTL compatibility on the inputs and high drive capability on the outputs.

Figures 6 and 7 show the distribution of input levels of uncompensated and compensated 16K ROMs. Although these are room temperature distributions, extending the temperature would tend to further widen the uncompensated distribution.

INPUT HIGH LEVELS
Figure 6
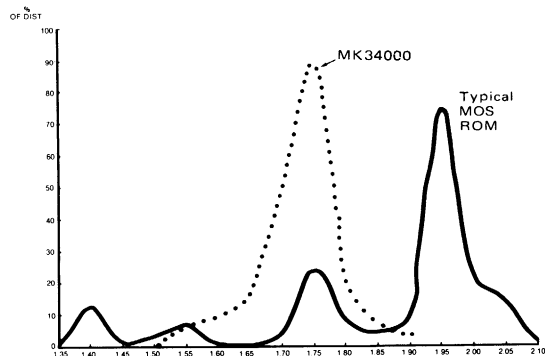
INPUT LOW LEVELS
Figure 7
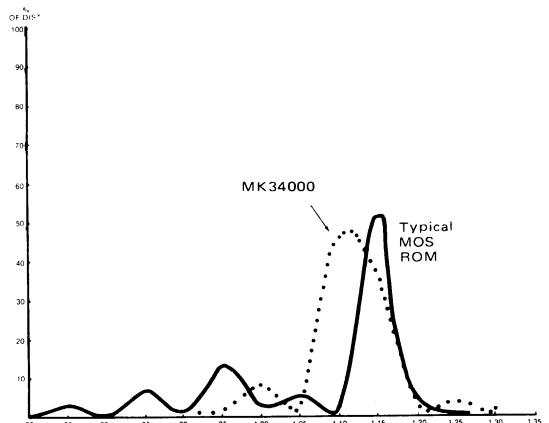
As was eluded to above, output drive is at least partially enhanced by the operation of the charge pump in two ways. Since V_{TNOM} is lower, the overall output drive is made larger (see Eq 5). Over temperature (particularly from –55°C to +125°C) the charge pump holds V_T constant, which in turn keeps output drive at a higher level.

Also with a compensated device, a power supply tolerance of ±10% is more easily accomplished. Again referring to Equation 5, if the upper limit of V_T is abnormally high, then the amount of tolerance on the power supply is reduced. On an uncompensated device, the V_T makes it extremely difficult to design an input stage with true TTL levels. Since the reference voltage V_R is kept at a fixed percentage of the V_{CC} supply, the output level will not decrease by the total change in V_{CC}, if V_{CC} should decrease. Rather output drive would only decrease by an amount determined by the fixed percentage that V_R is of V_{CC}.

User Benefits
The user benefits created by the charge pump are quite obvious. It is no longer necessary to utilize an external power supply (requiring regulation) to accomplish the tasks of shifting the operating thresholds and reducing junctions capacitance. The substrate bias generator performs these functions with only a slight increase in circuit power dissipation (typically 5mW) and not a significant increase in overall chip size. This saves the cost of an extra supply with a non-significant increase in the I.C. price.

The charge pump allows the circuit designer and thus the system designer greater design tolerances, as witnessed by the MK30000 and 34000 performance specifications. It gives the system designer ± 10% power supply tolerances while allowing greater output drive. This can be a significant advantage in a 5 volt only ROM. Input levels can be specified at true TTL levels providing the widest noise margins possible when used with high performance control circuitry such as standard TTL or Schottky TTL.

Power dissipation is kept to a minimum while access time is the fastest of any 5 volt only ROMs available. Due to the charge pump compensating for V_T changes with temperature the specified operating temperature range can be increased to -55°C to +125°C with only minimal loss in system performance (namely access time and power dissipation).

Another important factor is cost. The charge pump narrows the V_T distribution of the MK30000/34000 and MK36000 making them highly repeatable and manufacturable products. This not only reduces the device costs but increases yields, reducing the lead time for production quantities because of an increased number of available chips.

ROM PROGRAMMING GUIDE

It has always been MOSTEK's policy to service its customers ROM needs in the most efficient way possible. In continuing with this effort, MOSTEK has revised its ROM Procedure to better facilitate the market we serve. This new ROM programming guide and information form will insure that all pertinent information is received with the purchase order. This will reduce the unnecessary delays which develop when sufficient information is not available.

DESCRIPTION OF ROM FORM

The first part of the ROM programming form is concerned with providing all necessary customer information to MOSTEK. This will simplify any correspondence which may be necessary to complete the order in question.

The ROM generic type simply indicates the ROM series the customer wishes to purchase. This includes the following MOSTEK series:

> MK2300 Series
> MK2400 Series
> MK2500/2600 Series
> MK28000 Series
> MK30000 Series
> MK31000 Series
> MK34000 Series
> MK36000 Series

PACKAGE TYPE

The package type must be included on both the ROM form and the purchase order to prevent parts being produced in the wrong package. Currently, all prototypes and any follow-on quantities built in Dallas will be ceramic. Remember: P = Ceramic, N = Plastic.

CUSTOMER NUMBERS

In the event the customer assigns a part number to the MOSTEK ROM selected, this number should be entered on the ROM form. This number will simplify any communication which may be necessary between the customer and MOSTEK.

SPECIAL BRANDING

Special branding of MOSTEK ROMs is possible if the instructions are indicated on the ROM programming form. But due to space and printing limitations, any special branding desired must be limited to 10 characters on one line.

CUSTOMER SPECIFICATIONS

If the customer desires different specifications for the ROM selected than appears on the appropriate MOSTEK data sheet; it is imperative that these specification changes be well documented and sent to MOSTEK as early as possible. This is important because any specification change must be reviewed and accepted by MOSTEK before the ROM order can be processed.

ROM DATA

MOSTEK will accept a number of media and formats for the inputting of programming data. This flexibility will make it easy for a customer to have his ROM order processed as quickly as possible. In all cases the actual ROM contents is preceded by four header cards or records which contain important programming information such as chip select codes, logic, and verification codes. Refer to the appropriate MOSTEK data sheet for the description of the header cards and the MOSTEK format for the actual ROM data. The following table shows the formats and media that can be most easily processed by MOSTEK. When filling out the ROM programming form, check the appropriate block under pattern media.

PATTERN MEDIA

Punched Cards: Use standard 80 column cards punched as per the applicable format. MOSTEK's four header cards must be included.

Paper Tape: Use 1", 7 or 8 bit ASCII coded paper or mylar tape. Tape records should be card images ending with a carriage return and line feed if a card format is being used.

ROMS/PROMS: On MOSTEK's ROMs of 4096 bit and larger density, PROMs of the 2708 and 2716

type or pin compatible ROMs may be submitted for the ROM contents. They must, however, be accompanied by the header cards required for the MOSTEK ROM type or that information in written form. Each PROM or ROM submitted must also be clearly marked so that no question arises as to its starting memory location.

VERIFICATION MEDIA

For pattern verification, MOSTEK can supply either a printout, paper tape, card deck, or reprogrammed PROMs. Formats of cards and tapes are as shown in the table of acceptable formats.

To insure rapid turnaround of data verification information, acceptable media and formats should be used as outlined in the tables. If another method is desired, contact MOSTEK so that all arrangements can be made and an accurate schedule can be generated. Quick turnaround of verification information cannot be guaranteed in cases where new software has to be developed. Remember, when filling out the ROM programming form, check the appropriate block under verification media.

HOW THE PROGRAM WORKS

MOSTEK's ROM program is designed for maximum safety with two verification steps that limit the liability of both the customer and MOSTEK. However, if circumstances dictate, MOSTEK is flexible enough to vary its procedures to better serve its customers.

PATTERN VERIFICATION

Upon receipt of the ROM programming information form and the ROM input data, MOSTEK engineering will re-generate the pattern data for customer verification. At this point, no liability is incurred for either party. Following customer verification, MOSTEK begins prototype production. This verification step can be waived so that prototype production begins immediately upon receipt of the input data. The time savings is the time for MOSTEK engineering to generate verification plus the time necessary for the customer to receive and verify the data. This savings is usually less than two weeks. If data verification is waived, the customer is liable for the mask charge plus the prototype parts.

PROTOTYPE VERIFICATION

The second verification step in MOSTEK's ROM Program is that of prototype verification. The prototype quantity is usually 25 parts which are considered part of the order quantity for billing purposes. After the customer has verified the prototype, in writing, as being correct, MOSTEK will proceed with the production of the total remaining order.

The prototype verification step can also be waived and MOSTEK will immediately begin production instead of prototype. The time savings gained from waiving prototype verification is usually 5-6 weeks. If prototype verification is waived, the customer is liable for the mask charge plus all work-in-process material if a customer mistake occurs.

WAIVERS OF VERIFICATION

Arrangements must be worked out with MOSTEK prior to committing deliveries based on verification waivers. If an order is accepted by MOSTEK waiving pattern verification, the quoted cycle time begins upon receipt of the input data and only a small quantity of parts will be produced as prototypes. If MOSTEK accepts an order waiving prototype verification, the quoted cycle time will begin upon notification of pattern verification.

GENERAL INFORMATION

Production capacity cannot be reserved without a purchase order. Therefore any quotes for delivery will be subject to change until a purchase order is obtained.

Moderate quantities of parts are usually available from the MOSTEK Dallas Assembly facility shortly after prototype shipments. These units will always be ceramic packages and, if delivered in less than 8 weeks after prototypes, will require a $2.00 per unit adder in addition to the ceramic package price.

The appropriate MOSTEK price sheet contains information on order minimums and price adders.

ACCEPTABLE MEDIA				
MK TYPE	CARDS	PAPER TAPE	ROM	PROM
MK2300P Series	X	X		
MK2400P Series	X	X		
MK2500/2600P Series	X	X	X	
MK28000P/N Series	X	X	X	X
MK30000P/N Series	X	X	X	X
MK31000P/N Series	X	X	X	X
MK34000P/N Series	X	X	X	X
MK36000P/N	X	X	X	X

READ ONLY MEMORIES

DEVICE	ORGANIZATION	LOGIC	NUMBER BITS	ACCESS (ns)	V_{DD}	V_{GG}	V_{BB}	V_{CC}	V_{SS}	POWER DIS (MW) MAX	PACKAGE TYPE	PINS
MK2300	64x7x5	Static	2240	1000	0	-12			+5	750	Ceramic	24
MK2400	256x10	Static	2560	500	0	-12			+5	850	Ceramic	24
MK2500	512x8 or 1024x4	Static	4096	700	0	-12			+5	950	Cer/Plas	24
MK2600	512x8 or 1024 x 4	Static	4096	700	0	-12			+5	950	Cer/Plas	24
MK28000	2048x8 or 4096x4	Dynamic	16384	600		-12			+5	1000	Cer/Plas	24
MK30000	1024x8	Static	8192	450				+5	0	TBD	Cer/Plas	24
MK31000	2048x8	Static	16384	550				+5	0	300	Cer/Plas	24
MK34000	2048x8	Static	16384	350				+5	0	330	Cer/Plas	24
MK36000	8192x8	Dynamic	65536	250				+5	0	220	Cer/Plas	24

ROM CROSS REFERENCE

MOSTEK	AMD	INTEL	MOTOROLA	AMI	FCLD	SYNERTEK	NATIONAL	EA	G.I.
MK2500P				S5232			MM4232/5232		
MK2600P	AM9214			S3514	3514				
MK28000P/N								EA4800/4900	
MK30000P/N*	AM9208	2308/8308						EA2308A	
MK31000P/N		2316A/8316A		S6831A		SY2316A			RO-3-8316A/B
MK34000P/N		2316E/8316E	MCM68316E	S6831B		SY2316B			RO-3-9316A/B
MK36000P/N									

* MOSTEK's MK30000 operates from +5 volts only
** User must consult the applicable MOSTEK Data Sheet for timing conformance.

ACCEPTABLE FORMAT

MK TYPE	MOSTEK	NAT	FCLD	INTEL CARD	INTEL TAPE	EA	MOSTEK F–8	MOT 6800
MK 2300P Series	X							
MK 2400P Series	X							
MK 2500/2600P Series	X	X	X					
MK 28000P/N Series	X					X	X	X
MK 30000P/N Series	X			X	X	X	X	X
MK 31000P/N Series	X			X	X	X	X	X
MK 34000P/N Series	X			X	X	X	X	X
MK 36000P/N Series	X			X	X	X	X	X

ROMS
Programming Guide

ROM PROGRAMMING FORM

CUSTOMER NAME _____

ADDRESS _____

CITY _____ STATE _____ ZIP _____

PHONE (___) _____ EXTENSION _____

CUSTOMER CONTACT_____ TITLE _____

MOSTEK REP. OR DIST. _____

ROM Generic Type _____

Package Type _____

Customer Part Number _____

Branding Requirement _____

Customer Specification: | Yes
 | No | Parts to be tested to standard
 | | Data Sheet

Date customer spec sent to MOSTEK _____

PATTERN MEDIA	VERIFICATION MEDIA
☐ PROM (2708/2716)	☐ PROM (2708/2716)
☐ PIN COMPATIBLE ROMS	☐ PIN COMPATIBLE ROMS
☐ PAPER TAPES	☐ PAPER TAPES
☐ CARD DECK	☐ CARD DECK
☐ TAPE OF CARD DECK	☐ TAPE OF CARD DECK
☐ OTHER - NOTE 1	☐ OTHER - NOTE 1

NOTES: (1) Other Media Require Factory Approval

Date Pattern Data Sent to MOSTEK _____

Does Customer Require Prorotypes   Yes ___ No _____

Pattern Verification Required by Customer | Yes | | Waived | |

Prototype Verification Required by Customer | Yes | | Waived | |

COMMENTS: (waiver explanation)

Customer Order Number   _____

Date of Customer Order   _____

Distributor Order Number to MOSTEK   _____

Order Quantity and Price   _____

Delivery Requested/Committed   Prototypes _____

          Production _____

Date Form Completed   _____

Technology

MOSTEK®

NEW GENERATION SEMICONDUCTOR MEMORY DEVICES

By DR. PAUL SCHROEDER
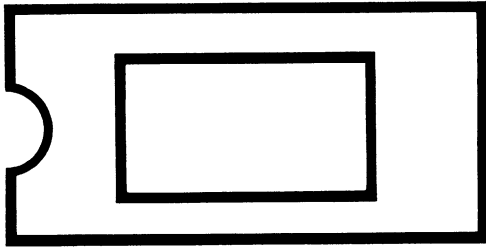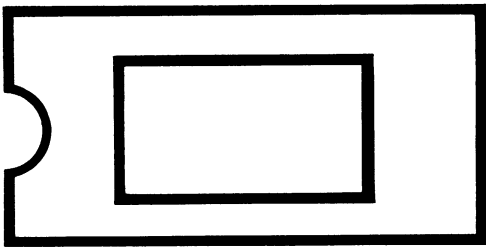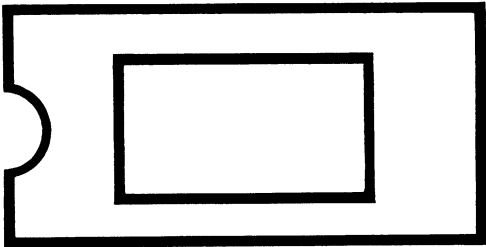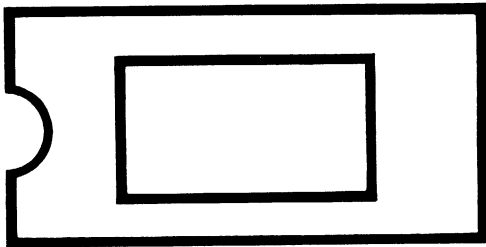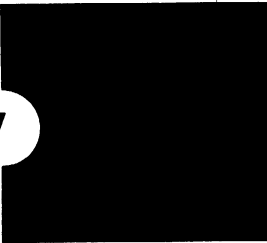
Technology

Semiconductor memory is an area which has been characterized by dramatic and revolutionary technology development. This process has led to the current generation of highly sophisticated memory devices which today offers the user greater density, performance and reliability than ever before at lower cost. While some signs of maturity in this field are now becoming discernable — particularly in the quality of design and product reliability — the pace of innovation seems little diminished. A host of recently or soon to be introduced new products provide the user a new generation of devices with superior characteristics for a wide spectrum of applications.

In this paper an overview of the status of process technology will be given first. Then individual areas of memory development will be examined with the intent of assessing the current state-of-the-art and providing some insight into where next generation efforts might lead.

Technology Status

Because of its market size and the importance of scale of integration, memory is unique in its capacity to support new process and device technologies. As a result, hardly a new technology is invented which is not immediately applied to some memory device. Nor is it likely that a major new device is designed which does not require a special process technology to build it. Today, supporters can be found for a variety of technologies which, in addition to standard NMOS and bipolar, include I^2L, CMOS, DMOS, VMOS, SOS, as well as a number of CCD structures. However, the overwhelming bulk of mainframe and general purpose devices utilize NMOS silicon gate or some variant thereon (such as two level poly). High performance versions, which employ shallow (preferably implanted) source drain regions and scaled device dimensions are beginning to appear which may significantly challenge bipolar in the very high speed ($< 50ns$ access) range, although the fastest speeds are still the exclusive preserve of bipolar devices.

At the opposite end of the spectrum, extremely low power static memories have been introduced which employ NMOS silicon gate

augmented with high impedance poly resistors. Memory cells implemented in this technology have standby currents comparable to CMOS while retaining the cost and speed advantages of the simpler NMOS process. Because of these it is likely that this form of NMOS will largely displace CMOS in the low power/battery back-up RAM market.

While NMOS silicon gate retains its preeminence as the mainstream memory technology, a number of challengers cannot be ignored. Newer forms of bipolar structures, particularly I^2L, are being used to achieve cell areas comparable to those in MOS. Dynamic concepts, previously an MOS exclusive, are now being introduced to bipolar. If these efforts are successful, the cost and density edge of MOS could be reduced. However, the gap is sufficiently great that it is unlikely that a major technology shift to bipolar will occur for main memory applications in the near future.

Another technology receiving current interest is VMOS. By using a vertical structure and anisotropic etch techniques, very short channel, high density MOS structures can be fabricated. Speeds comparable to those of bipolar devices have been achieved. Unfortunately, the level of process complexity required is high, and it is questionable whether acceptable reliability and yield can be achieved for LSI devices.

Other technologies such as DMOS and SOS, have found only limited interest or application to memory.

For the future, it appears that NMOS silicon gate will continue to dominate as an area of development activity. Efforts are underway to push to higher performance levels by reducing gate oxide thickness and other dimensions, along with the use of all-implanted shallow diffusions. These developments are expected to increase MOS speeds by as much as a factor of two beyond those presently achieved, even keeping conventional optical lithography. Further out, much more dramatic advances, both in performance and density, are expected when electron beam processing becomes a reality. A first solid step in this direction has now been taken with the commercial availability of E-beam mask exposure systems. Direct wafer processing, however, remains a number of years off, despite a number of laboratory systems which have existed for some time.

Let us next look at some of the product areas where these technologies are or will be applied.

Static RAMs

Several product areas show particularly strong activity as indicated by new product introductions. This is especially true of 4K static RAMs. Two main lines of development have emerged, one aimed at speed and the other power. In the high speed area, sub-50 nsec access time is the universal goal and both MOS and bipolar devices are or will soon be available. Parts in this speed range are generally asynchronous (no chip-enable clock) and high powered (~500mW dissipation).

However, by using the chip select input to gate power to selected internal circuits, a reduction of standby power to one tenth that of active has been achieved. Characteristically, the circuits used in these high speed parts are relatively simple, the burden of performance being placed on the process technology.

In the area of low power, 200 ns access devices have been recently introduced which provide dramatic power reductions over previous NMOS statics. This advance has been made possible by two new developments: (1) the successful implementation of a static cell which employs near-intrinsic polysilicon load resistors and (2) the application of dynamic circuit techniques to the peripheral circuitry. The high impedance loads permit static cell operation at current levels comparable to PN junction leakage. Consequently, virtually all power is dissipated in peripheral circuitry. This dissipation is, in turn, reduced to very low levels (without sacrificing speed) by using the same dynamic circuit techniques that have been used in dynamic RAMs. This clocked CE approach thus provides low active power (~50mW typically) with even lower standby power. For those applications which require data retention under battery-backup conditions for prolonged periods, additional power reduction is possible at reduced supply voltages. It is expected that further improvements of these devices will take place, particularly with regard to speed. Sub-100 ns access performance is possible with advanced but existing technology and efforts to achieve these speeds are underway.

ROMs and PROMs

The next big step in ROMs soon to hit the market will be devices at the 32K and 64K levels.

Cell area in these ROMs is 0.25 mil^2 or less, which represents about a factor of two reduction from previous designs. As in the case of static RAMs, application of dynamic circuit techniques provides a means of achieving much higher performance, both in terms of higher speed and lower power, than is possible with more conventional approaches. Typical operating power in one recently announced 64K ROM designed with a clocked CE should be well under 100mW in the active mode and approximately one fourth that in standby. Access speeds in the 200ns to 300ns range are achievable with such NMOS devices.

While the density in ROMs has quadrupled, that of new generation EPROMs has also increased, although only by a factor of two. New 16K devices are now available, either as three supply (+12V, +5V) versions, or as 5 volt single-supply parts (for read mode). While 5 volt operation is highly desirable, particularly in microprocessor systems, the multisupply versions offer easy upgrade of systems already designed for the older 8K devices.

Dynamic RAMs

For the moment, most of the controversy that has historically accompanied dynamic RAM progress has settled down with industry consensus on a single 16K (as well as 4K) multiplexed specification. Higher speed versions of these parts have been introduced recently with access times of 120ns. Even faster versions are in development and may be expected soon.

Most of the interest in this area now focuses on what is coming next and how soon. Generally, industry expectations are that the next major product will be at the 64K level, that its characteristics will be similar to the present 16K, and that parts will become available in the 1979-1980 time frame. The probable die size is anticipated to be in the range of 40,000 to 50,000 square mils.

However, the most desirable product or that which will emerge may not correspond to these projections. Some key questions that need to be answered are: How should the next part be organized — 64K x 1, 16K x 4, or other? How should the part be packaged? What values of supply voltage (and how many) are optimum? Should the inputs be TTL compatible, or ECL? What speed-power tradeoffs are there? Is a universal part possible or are different designs and organizations essential for different applications? The answers to these questions and others, if not assessed properly, may cause as much confusion in the next major dynamic RAM product as occurred in the early 4K days.

Serial CCD memories have now emerged at the 64K density level. However, the big question that still remains is whether a major market for CCD serial devices will actually develop. Die size for these new 64K parts are generally very large by current standards and involve rather complex processing. Consequently, the costs of these devices might not become low enough to be attractive for widespread applications. It seems possible that any big market for these CCD memories will wait until smaller cells, substantially faster operation, less expensive fabrication, or higher density, perhaps at the 256K level, allow the economics to become more attractive.

Conclusion

NMOS continues to be the dominant technology in semiconductor memory, with more advanced forms moving into both higher speed applications previously served only by bipolar and into some very low power areas which, up until now, were exclusively CMOS. While the fastest memory components are presently bipolar, it is significant that NMOS performance has relatively more to gain from anticipated future progress in reducing device dimensions.

The move to single 5 volt, clocked operation is becoming evident among most types of memory devices. Asynchronous operation will remain desirable only in the highest speed products where considerations of system skew become extremely important.

NEW GENERATION
Technology

DESIGNERS GUIDE
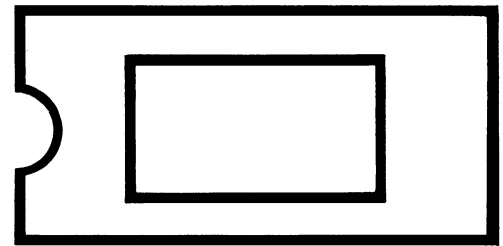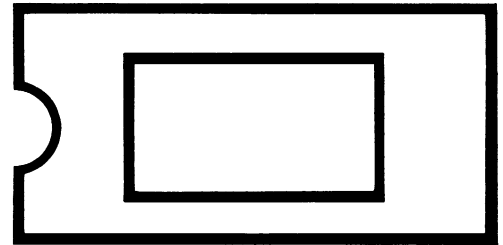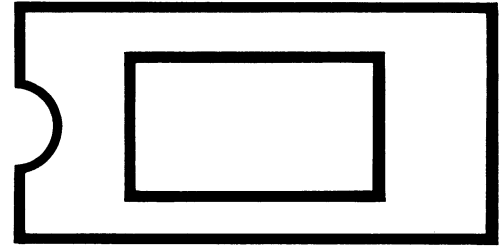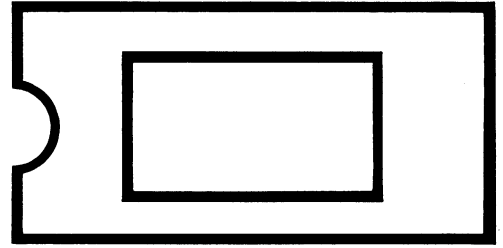
Packaging

CERAMIC DUAL-IN-LINE HERMETIC PACKAGING (P)

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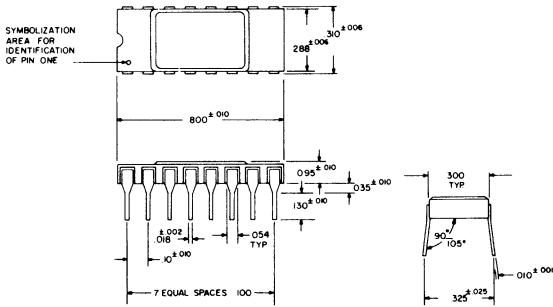
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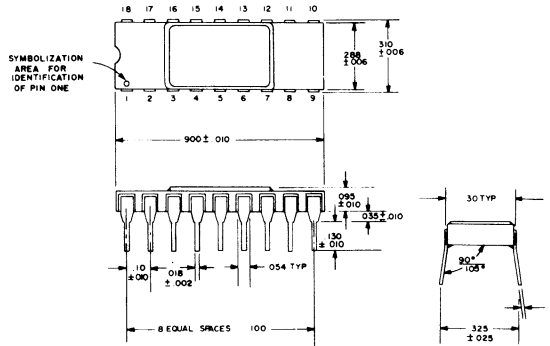
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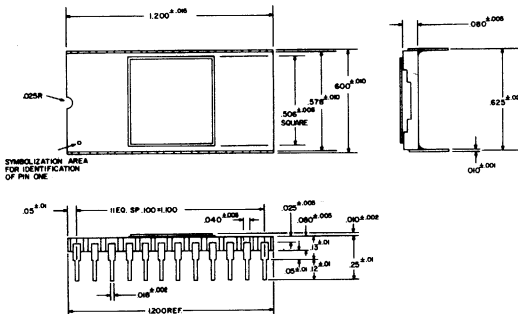
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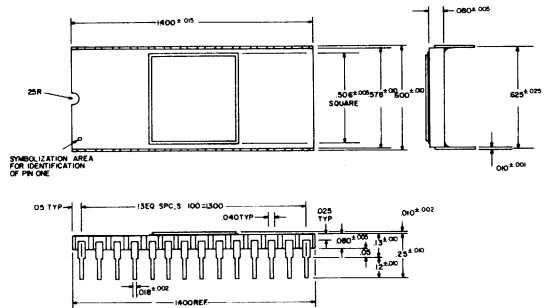
PLASTIC DUAL-IN-LINE PACKAGING (N)

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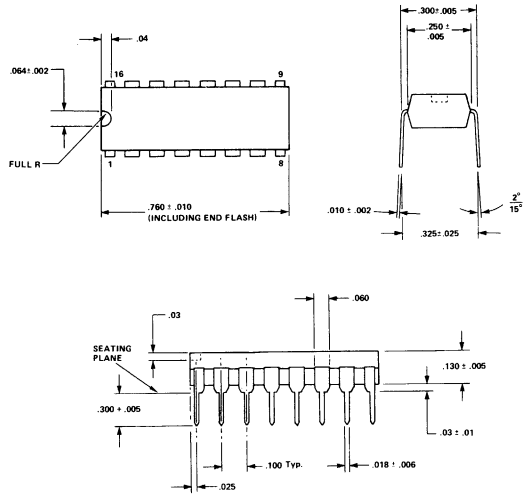
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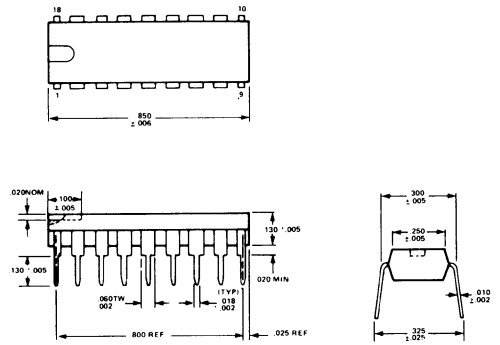
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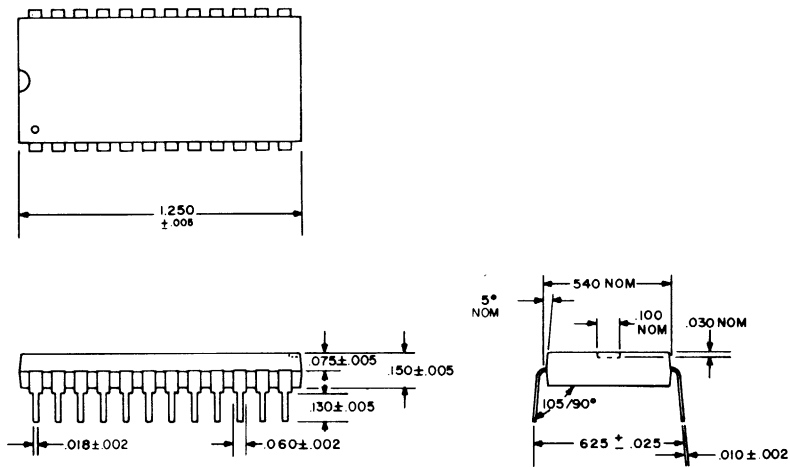
24-Lead Side-Braze Ceramic Package With Transparent Lid

Tin-Plated, Frit-Sealed Ceramic Lid, Side-Braze Package (K)

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