MITSUBISHI SEMICONDUCTORS 1992

SINGLE-CHIP 8-BIT MICROCOMPUTERS Vol. 2

DATA BOOK

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GUIDANCE

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■Series MELPS 740 single-chip microcomputers

Type	Circuit function and organization	Structure	Supply voltage (V)	Electrical characteristics			Package	Page
				Typ pwr dissipation (mW)	Min. cycle time (μs)	Max fre-quency (MHz)		
M50708-XXXSP/FP※	6K-Byte Mask-Prog. ROM, 128-Byte RAM, Serial I/O	C, Si	5±10%	15	2	4	64P4B/72P6	Note1
M50740A-XXXSP/FP ※	3K-Byte Mask-Prog. ROM, 96-Byte RAM	C, Si	5±10%	15	2	4	52P4B/50P6	Note1
M50740ASP ※	External ROM Type, 96-Byte RAM	C, Si	5±10%	15	2	4	52P4B	Note1
M50741-XXXSP/FP ※	4K-Byte Mask-Prog. ROM, 96-Byte RAM	C, Si	5±10%	15	2	4	52P4B/50P6	Note1
M50742-XXXSP/FP ※	4K-Byte Mask-Prog. ROM, 128-Byte RAM, Serial I/O	C, Si	5±10%	15	2	4	64P4B/72P6	Note1
M50743-XXXSP/FP ※	4K-Byte Mask-Prog. ROM, 128-Byte RAM	C, Si	5±10%	30	1	8	64P4B/72P6	Note1
M50744-XXXSP/FP ※	4K-Byte Mask-Prog. ROM, 144-Byte RAM	C, Si	5±10%	15	2	4	64P4B/72P6	Note1
M50745-XXXSP/FP ※	6K-Byte Mask-Prog. ROM, 192-Byte RAM	C, Si	5±10%	15	2	4	64P4B/60P6	Note1
M50746-XXXSP/FP ※	6K-Byte Mask-Prog. ROM, 144-Byte RAM	C, Si	5±10%	15	2	4	64P4B/72P6	Note1
M50747-XXXSP/FP ※	8K-Byte Mask-Prog. ROM, 256-Byte RAM	C, Si	5±10%	30	1	8	64P4B/72P6	Note1
M50747H-XXXSP/FP	8K-Byte Mask-Prog. ROM, 256-Byte RAM	C, Si	5±5%	45	0.67	12	64P4B/72P6	Note1
M50752-XXXSP ※	4K-Byte Mask-Prog. ROM, 128-Byte RAM, High Voltage Port, CR Oscillation Type	C, Si	5±10%	15	2	4	52P4B	Note1
M50753-XXXSP/FP	6K-Byte Mask-Prog. ROM, 96-Byte RAM, 8-Bit A-D Converter	C, Si	5±10%	15	2	4	64P4B/60P6	Note1
M50754-XXXSP/FP/GP	6K-Byte Mask-Prog. ROM, 160-Byte RAM, PWM, High Voltage Port, Serial I/O	C, Si	4~5.5	20	1.90	4.2	64P4B/72P6/ 64P6W	Note1
M50757-XXXSP ※	3K-Byte Mask-Prog. ROM, 96-Byte RAM, High Voltage Port, CR Oscillation Type	C, Si	5±10%	15	2	4	52P4B	Note1
M50758-XXXSP ※	3K-Byte Mask-Prog ROM, 96-Byte RAM, High Voltage Port, Ceramic Oscillation Type	C, Si	5±10%	15	2	4	52P4B	Note1
M50930-XXXFP	4K-Byte Mask-Prog. ROM, 128-Byte RAM, LCD Controller/Driver, Serial I/O	C, Si	5±10%	15	1.86	4.3	80P6	Note2
M50931-XXXFP	4K-Byte Mask-Prog. ROM, 512-Byte RAM, LCD Controller/Driver, Serial I/O	C, Si	5±10%	15	1.86	4.3	80P6	
M50932-XXXFP	8K-Byte Mask-Prog. ROM, 512-Byte RAM, LCD Controller/Driver, Serial I/O	C, Si	5±10%	15	1.86	4.3	80P6	
M50933-XXXFP	6K-Byte Mask-Prog. ROM, 192-Byte RAM, LCD Controller/Driver, Serial I/O	C, Si	3.8~5.5	15	1.86	4.3	80P6	Note2
M50934-XXXFP	8K-Byte Mask-Prog. ROM, 256-Byte RAM, LCD Controller/Driver, Serial I/O	C, Si	3.8~5.5	15	1.86	4.3	80P6	
M50940-XXXSP/FP	4K-Byte Mask-Prog ROM, 128-Byte RAM, 8-Bit A-D Converter, High Voltage Port, Serial I/O	C, Si	5±10%	15	2	4	64P4B/72P6	Note2
M50941-XXXSP/FP	8K-Byte Mask-Prog ROM, 192-Byte RAM, 8-Bit A-D Converter, High Voltage Port, Serial I/O	C, Si	5±10%	15	2	4	64P4B/72P6	
M50943-XXXSP/FP	8K-Byte Mask-Prog. ROM, 192-Byte RAM, 8-Bit A-D Converter, Serial I/O	C, Si	5±10%	30	1	8	64P4B/60P6	Note1
M50944-XXXSP/FP	12K-Byte Mask-Prog. ROM, 192-Byte RAM, 8-Bit A-D Converter, Two Serial I/Os	C, Si	3~5.5	15	1.91	4.19	64P4B/64P6S	Note2
M50945-XXXSP/FP	16K-Byte Mask-Prog. ROM, 256-Byte RAM, 8-Bit A-D Converter, High Voltage Port, Serial I/O	C, Si	5±10%	15	2	4	64P4B/72P6	Note2
M50950-XXXSP	6K-Byte Mask-Prog. ROM, 144-Byte RAM, High Voltage Port, Two Serial I/Os	C, Si	5±10%	20	1.6	5	52P4B	Note1
M50951-XXXSP	4K-Byte Mask-Prog ROM, 144-Byte RAM, High Voltage Port, Two Serial I/Os	C, Si	5±10%	20	1.6	5	52P4B	Note1
M50954-XXXSP/FP/GP	8K-Byte Mask-Prog. ROM, 192-Byte RAM, PWM, High Voltage Port, Serial I/O	C, Si	4~5.5	20	1.90	4.2	64P4B/72P6/ 64P6W	Note1
M50955-XXXSP/FP/GP	10K-Byte Mask-Prog. ROM, 192-Byte RAM, PWM, High Voltage Port, Serial I/O	C, Si	4~5.5	20	1.90	4.2	64P4B/72P6/ 64P6W	Note1

★ : New product ★★ : Under development

Note1 : Refer to the "1989 MITSUBISHI SEMICONDUCTORS DATA BOOK 〈SINGLE-CHIP 8-BIT MICROCOMPUTERS〉"

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※ : The production of this product is no longer planned due to announcement of new series or upgrades.

■Series MELPS 740 single-chip microcomputers (continued)

Type	Circuit function and organization	Structure	Supply voltage (V)	Electrical characteristics			Package	Page
				Typ pwr dissipation (mW)	Min. cycle time (μs)	Max. frequency (MHz)		
M50957-XXXSP/FP	10K-Byte Mask-Prog. ROM, 256-Byte RAM, PWM, High Voltage Port, 4-Bit Comparator, Serial I/O	C, Si	4~5.5	20	1.90	4.2	64P4B/72P6	Note2
M50958-XXXSP/FP ※	12K-Byte Mask-Prog. ROM, 256-Byte RAM, PWM, High Voltage Port, 4-Bit Comparator, Serial I/O	C, Si	4~5.5	20	1.90	4.2	64P4B/72P6	
M50959-XXXSP/FP ※	16K-Byte Mask-Prog. ROM, 256-Byte RAM, PWM, High Voltage Port, 4-Bit Comparator Serial I/O	C, Si	4~5.5	20	1.90	4.2	64P4B/72P6	
M50963-XXXSP/FP ※	10K-Byte Mask-Prog. ROM, 160-Byte RAM, 8-Bit A-D Converter, 5-Bit D-A Converter, PWM, Serial I/O	C, Si	5±10%	15	2	4	64P4B/72P6	Note1
M50964-XXXSP/FP ※	6K-Byte Mask-Prog. ROM, 160-Byte RAM, 8-Bit A-D Converter, 5-Bit D-A Converter, PWM, Serial I/O	C, Si	5±10%	15	2	4	64P4B/72P6	Note1
M50734SP/FP	External ROM, RAM Type, 5-Timer, 8-Bit A-D Converter, Serial I/O	C, Si	5±10%	30	1	8	64P4B/72P6	Note2
M50734SP/FP-10	External ROM, RAM Type, 5-Timer, 8-Bit A-D Converter, Serial I/O	C, Si	5±10%	35	0.8	10	64P4B/72P6	
M37100M8-XXXSP/FP	16K-Byte Mask-Prog. ROM, 320-Byte RAM, Two Serial I/Os, A-D Converter, OSD Function	C, Si	5±10%	27.5	2	4	64P4B/80P6	Note3
M37102M8-XXXSP/FP ★	16K-Byte Mask-Prog. ROM, 320-Byte RAM, Two Serial I/Os, A-D Converter, PWM, OSD Function	C, Si	5±10%	110	1	4	64P4B/80P6N	Note3
M37103M4-XXXSP ★	8K-Byte Mask-Prog. ROM, 320-Byte RAM, Serial I/O, A-D Converter, PWM, OSD Function	C, Si	5±10%	35	2	4	64P4B	Note3
M37120M6-XXXFP ★	12K-Byte Mask-Prog. ROM, 256-Byte RAM, Serial I/O, A-D Converter, D-A Converter, OSD Function	C, Si	5±10%	75	1	4	80P6N	Note3
M37201M6-XXXSP ★	24K-Byte Mask-Prog. ROM, 384-Byte RAM, Two Serial I/Os, A-D Converter, PWM, OSD Function	C, Si	5±10%	110	1	4	64P4B	Note3
M37202M3-XXXSP ★★	12K-Byte Mask-Prog. ROM, 256-Byte RAM, Serial I/O, A-D Converter, PWM, OSD Function, Four Timers	C, Si	5±10%	110	1	4	64P4B	Note3
M37204M8-XXXSP ★★	32K-Byte Mask-Prog ROM, 512-Byte RAM, Serial I/O, A-D Converter, D-A Converter, PWM, OSD Function, Four Timers	C, Si	5±10%	110	1	4	64P4B	Note3
M37250M6-XXXSP ★	24K-Byte Mask-Prog. ROM, 384-Byte RAM, Serial I/O, A-D Converter, PWM, OSD Function, PLL Function, Four Timers	C, Si	5±10%	137.5	1	4	64P4B	Note3
M37260M6-XXXSP ★★	24K-Byte Mask-Prog. ROM, 320-Byte RAM, 8-Byte Serial I/O, OSD Function, Four Timers	C, Si	5±10%	110	1	4	52P4B	Note3
M37408M2-XXXSP/FP ★★	4K-Byte Mask-Prog. ROM, 128-Byte RAM, Dual-Port RAM, UART, Bus Interface, Timer	C, Si	5±10%	50	0.8	10	42P4B/44P6N	Note3
M37409M2-XXXSP/FP	4K-Byte Mask-Prog. ROM, 128-Byte RAM, Dual-Port RAM, Three UARTs, Bus Interface, Timer	C, Si	5±10%	50	0.8	10	52P4B/56P6N	Note3
M37410M3HXXXFP	6K-Byte Mask-Prog. ROM, 192-Byte RAM, Serial I/O, A-D Converter, LCD Controller/Driver	C, Si	2.5~5.5	30	1	8	80P6S	Note3
M37410M4HXXXFP	8K-Byte Mask-Prog. ROM, 256-Byte RAM	C, Si	2.5~5.5	30	1	8	80P6S	
M37410M6HXXXFP	12K-Byte Mask-Prog. ROM, 256-Byte RAM	C, Si	2.5~5.5	30	1	8	80P6S	
M37412M4-XXXFP	8K-Byte Mask-Prog. ROM, 160-Byte RAM,Serial I/O, PWM, 8-Bit A-D Converter, 5-Bit D-A Converter	C, Si	5±10%	15	2	4	72P6	Note3
M37413M4HXXXFP	8K-Byte Mask-Prog. ROM, 256-Byte RAM, Serial I/O, A-D Converter	C, Si	2.5~5.5	30	1	8	80P6S	Note3
M37413M6HXXXFP ★★	12K-Byte Mask-Prog. ROM, 256-Byte RAM	C, Si	2.5~5.5	30	1	8	80P6S	Note3
M37414M5-XXXFP ★	10K-Byte Mask-Prog. ROM, 160-Byte RAM, Serial I/O, PWM, 8-Bit A-D Converter, 5-Bit D-A Converter	C, Si	5±10%	15	2	4	72P6	Note3
M37415M4-XXXFP	8K-Byte Mask-Prog. ROM, 512-Byte RAM, Serial I/O, LCD Controller/Driver, DTMF Generator	C, Si	2.5~5.5	20	2.5	3.2	80P6	Note3

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■Series MELPS 740 single-chip microcomputers (continued)

Type	Circuit function and organization	Structure	Supply voltage (V)	Electrical characteristics			Package	Page
				Typ pwr dissipation (mW)	Min. cycle time (µs)	Max. frequency (MHz)		
M37416M2-XXXSP/FP ★	4K-Byte Mask-Prog. ROM, 128-Byte RAM, UART, Comparator, Bus interface, Key on wake up	C, Si	5±10%	50	1	8	52P4B/56P6N	Note3
M37420M4-XXXSP	8K-Byte Mask-Prog. ROM, 256-Byte RAM, PWM, Serial I/O, A-D Converter, D-A Converter, Timer	C, Si	5±10%	30	1	8	52P4B	Note3
M37420M6-XXXSP	12K-Byte Mask-Prog. ROM, 256-Byte RAM	C, Si	5±10%	30	1	8	52P4B	
M37421M6-XXXSP/FP	12K-Byte Mask-Prog. ROM, 320-Byte RAM, PWM, Serial I/O, High Voltage Port, 4-Bit Comparator	C, Si	5±10%	25	0.95	4.2	64P4B/72P6	Note3
M37424M8-XXXSP★★	16K-Byte Mask-Prog. ROM, 256-Byte RAM, PWM, Serial I/O, 8-Bit A-D Converter, 5-Bit D-A Converter, Timer	C, Si	5±10%	30	1	4	64P4B	Note3
M37524M4-XXXSP★★	16K-Byte Mask-Prog. ROM, 256-Byte RAM, PWM, Serial I/O, 8-Bit A-D Converter, 5-Bit D-A Converter, Timer	C, Si	5±10%	30	1	4	64P4B	Note3
M37428M4-XXXFP★★	8K-Byte Mask-Prog. ROM, 384-Byte RAM, UART, LCD Controller/Driver, Timer	C, Si	5±10%	15	1	8	80P6N	Note3
M37450M2-XXXSP/FP	4K-Byte Mask-Prog. ROM, 128-Byte RAM, 8-Bit A-D Converter, 8-Bit D-A Converter, UART, DBB, Three Timers, PWM	C, Si	5±10%	30	0.8	10	64P4B/80P6	3—3
M37450M4-XXXSP/FP	8K-Byte Mask-Prog. ROM, 256-Byte RAM	C, Si	5±10%	30	0.8	10	64P4B/80P6	
M37450M8-XXXSP/FP	16K-Byte Mask-Prog ROM, 384-Byte RAM	C, Si	5±10%	30	0.8	10	64P4B/80P6	
M37450S1SP/FP	External ROM, 128-Byte RAM	C, Si	5±10%	30	0.8	10	64P4B/80P6	3—43
M37450S2SP/FP	External ROM, 256-Byte RAM	C, Si	5±10%	30	0.8	10	64P4B/80P6	
M37450S4SP/FP	External ROM, 384-Byte RAM	C, Si	5±10%	30	0.8	10	64P4B/80P6	
M37451M4-XXXSP/FP/GP ★	8K-Byte Mask-Prog. ROM, 256-Byte RAM, 8-Bit A-D Converter, 8-Bit D-A Converter, UART, DBB, Three Timers, PWM	C, Si	5±10%	40	0.64	12.5	64P4B/ 80P6N/80P6S	3—59
M37451M8-XXXSP/FP/GP ★	16K-Byte Mask-Prog. ROM, 384-Byte RAM	C, Si	5±10%	40	0.64	12.5	64P4B/ 80P6N/80P6S	
M37451MC-XXXSP/FP/GP ★★	24K-Byte Mask-Prog. ROM, 512-Byte RAM	C, Si	5±10%	40	0.64	12.5	64P4B/ 80P6N/80P6S	
M37451SSP/FP/GP ★★	External ROM, 1024-Byte RAM	C, Si	5±10%	40	0.64	12.5	64P4B/ 80P6N/80P6S	3—106
M37470M2-XXXSP ★	4K-Byte Mask-Prog ROM, 128-Byte RAM, Serial I/O, A-D Converter	C, Si	2.7~5.5	17.5	1	4	32P4B	4—3
M37470M4-XXXSP ★	8K-Byte Mask-Prog. ROM, 192-Byte RAM	C, Si	2.7~5.5	17.5	1	4	32P4B	
M37470M8-XXXSP ★	16K-Byte Mask-Prog. ROM, 384-Byte RAM	C, Si	2.7~5.5	17.5	1	4	32P4B	
M37471M2-XXXSP/FP ★	4K-Byte Mask-Prog. ROM, 128-Byte RAM, Serial I/O, A-D Converter	C, Si	2.7~5.5	17.5	1	4	42P4B/56P6N	4—30
M37471M4-XXXSP/FP ★	8K-Byte Mask-Prog ROM, 192-Byte RAM	C, Si	2.7~5.5	17.5	1	4	42P4B/56P6N	
M37471M8-XXXSP/FP ★	16K-Byte Mask-Prog. ROM, 384-Byte RAM	C, Si	2.7~5.5	17.5	1	4	42P4B/56P6N	

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■Extended operating temperature version of microcomputers

Type	Circuit function and organization	Structure	Supply voltage (V)	Electrical characteristics			Package	Page
				Typ pwr dissipation (mW)	Min cycle time (μs)	Max fre-quency (MHz)		
M50744T-XXXSP ×	4K-Byte Mask-Prog. ROM,144-Byte RAM, Extended Operating Temperature Version of M50744-XXXSP	C, Si	5±10%	15	2	4	64P4B	Note1
M50747T-XXXSP	8K-Byte Mask-Prog. ROM,256-Byte RAM, Extended Operating Temperature Version of M50747-XXXSP	C, Si	5±10%	30	1	8	64P4B	Note1
M50753T-XXXSP	6K-Byte Mask-Prog ROM,96-Byte RAM, Extended Operating Temperature Version of M50753-XXXSP	C, Si	5±10%	15	2	4	64P4B	Note1
M50930T-XXXFP	4K-Byte Mask-Prog. ROM,128-Byte RAM, Extended Operating Temperature Version of M50930-XXXFP	C, Si	5±10%	20	1.86	4.3	80P6	Note1
M37450M4TXXXSP/J	8K-Byte Mask-Prog ROM, 256-Byte RAM, Extended Operating Temperature Version of M37450M4-XXXSP	C, Si	5±10%	30	0.8	10	64P4B/84P0	3—125
M37451M4DXXXSP/FP ★★	8K-Byte Mask-Prog ROM, 256-Byte RAM, Extended Operating Temperature Version of M37451M4-XXXSP/FP	C, Si	5±10%	40	0.64	12.5	64P4B/80P6N	3—139
M37451M8DXXXSP/FP ★★	16K-Byte Mask-Prog ROM, 384-Byte RAM, Extended Operating Temperature Version of M37451M8-XXXSP/FP	C, Si	5±10%	40	0.64	12.5	64P4B/80P6N	

■Piggyback type microcomputers (EPROM mounted type)

Type	Circuit function and organization	Structure	Supply voltage (V)	Electrical characteristics			Package	Page
				Typ pwr dissipation (mW)	Min cycle time (μs)	Max fre-quency (MHz)		
M50740-PGYS	Piggyback for M50740/M50741	C, Si	5±5%	—	2	4	52S1M	Note1
M50742-PGYS	Piggyback for M50742/M50708	C, Si	5±5%	—	2	4	64S1M	Note1
M50743-PGYS	Piggyback for M50743	C, Si	5±5%	—	1	8	64S1M	Note1
M50745-PGYS	Piggyback for M50745	C, Si	5±5%	—	2	4	64S1M	Note1
M50752-PGYS	Piggyback for M50757/M50752	C, Si	5±5%	—	2	4	52S1M	Note1
M50753-PGYS	Piggyback for M50753	C, Si	5±5%	—	2	4	64S1M	Note1
M50931-PGYS	Piggyback for M50930/M50931/M50932	C, Si	5±5%	—	2	4	80S6M	Note1
M50945-PGYS	Piggyback for M50940/M50941/M50945	C, Si	5±5%	—	2	4	64S1M	Note2
M50950-PGYS	Piggyback for M50950/M50951	C, Si	5±5%	—	1.6	5	52S1M	Note1
M50955-PGYS	Piggyback for M50754/M50954/M50955	C, Si	5±5%	—	1.9	4.2	64S1M	Note1
M50957-PGYS	Piggyback for M50957/M50958/M50959	C, Si	5±5%	—	1.9	4.2	64S1M	Note2
M50964-PGYS	Piggyback for M50964/M50963	C, Si	5±5%	—	2	4	64S1M	Note1
M37409PSS ★	Piggyback for M37409M2-XXXSP	C, Si	5±5%	—	0.8	10	52S1M	Note3
M37415PFS	Piggyback for M37415M4-XXXFP	C, Si	3.0~5.5	—	2.5	3.2	80S6M	Note3
M37421P-000SS M37421P-001SS	Piggyback for M37421M6-XXXSP	C, Si	5±5%	—	0.95	4.2	64S1M	Note3
M37450PSS	Piggyback for M37450M2/M4/M8-XXXSP	C, Si	5±5%	—	0.8	10	64S1M	3—141
M37450PFS	Piggyback for M37450M2/M4/M8-XXXFP	C, Si	5±5%	—	0.8	10	80S6M	3—148

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■Built-in PROM type microcomputers

Type	Circuit function and organization	Structure	Supply voltage (V)	Electrical characteristics			Package	Page
				Typ. pwr dissipation (mW)	Min. cycle time (μs)	Max fre-quency (MHz)		
M50746E-XXXSP/FP	One Time Programmable Version of M50746-XXXSP/FP	C, Si	5±5%	15	2	4	64P4B/72P6	Note1
M50746ES/EFS	PROM Version of M50746-XXXSP/FP	C, Si	5±5%	15	2	4	64S1B/72S6	Note1
M50747E-XXXSP/FP	One Time Programmable Version of M50747-XXXSP/FP	C, Si	5±5%	30	1	8	64P4B/72P6	Note1
M50747ES/EFS	PROM Version of M50747-XXXSP/FP	C, Si	5±5%	30	1	8	64S1B/72S6	Note1
M50944E-XXXSP/FP	One Time Programmable Version of M50944-XXXSP/FP	C, Si	3~5.5	15	1.9	4.2	64P4B/64P6S	Note1
M50944ES	PROM Version of M50944-XXXSP	C, Si	3~5.5	15	1.9	4.2	64S1B	
M50957E-XXXSP	One Time Programmable Version of M50957-XXXSP	C, Si	5±5%	20	1.9	4.2	64P4B	Note1
M50957ES	PROM Version of M50957-XXXSP	C, Si	5±5%	20	1.9	4.2	64S1B	
M50963E-XXXSP/FP	One Time Programmable Version of M50963-XXXSP	C, Si	5±5%	15	2	4	64P4B/72P6	Note1
M50963ES/EFS	PROM Version of M50963-XXXSP/FP	C, Si	5±5%	15	2	4	64S1B/72S6	Note1
M37102E8-XXXSP/FP ★	One Time Programmable Version of M37102M8-XXXSP/FP	C, Si	5±10%	110	1	4	64P4B/80P6N	Note3
M37120E6-XXXFP ★	PROM Version of M37120M6-XXXFP	C, Si	5±5%	75	1	4	80P6N	Note3
M37201E6-XXXSP ★	One Time Programmable Version of M37201M6-XXXSP		5±10%	110	1	4	64P4B	Note3
M37410E6HXXXFP	One Time Programmable Version of M37410M6HXXXFP	C, Si	2.5~5.5	30	1	8	80P6S	Note3
M37410E6HFS	PROM Version of M37410M6HXXXFP	C, Si	2.5~5.5	30	1	8	80S6	
M37412E5-XXXFP	One Time Programmable Version of M37412M4-XXXFP	C, Si	5±5%	15	2	4	72P6	Note3
M37413E6HXXXFP★★	One Time Programmable Version of M37413M6HXXXFP	C, Si	2.5~5.5	30	1	8	80P6S	Note3
M37413E6HFS ★★	PROM Version of M37413M6HXXXFP	C, Si	5±5%	30	1	8	80S6	
M37414E5-XXXFP ★	One Time Programmable Version of M37414M5-XXXFP	C, Si	5±5%	15	2	4	72P6	Note3
M37420E6-XXXSP ★	One Time Programmable Version of M37420M6-XXXSP	C, Si	5±5%	30	1	8	52P4B	Note3
M37420E6SS ★	PROM Version of M37420M6-XXXSP	C, Si	5±5%	30	1	8	52S1	
M37424E8-XXXSP ★★	One Time Programmable Version of M37424M8-XXXSP	C, Si	5±10%	30	1	4	64P4B	Note3
M37524E4-XXXSP ★★	One Time Programmable Version of M37524M4-XXXSP	C, Si	5±10%	30	1	4	64P4B	Note3
M37450E4-XXXSP/FP	One Time Programmable Version of M37450M4-XXXSP/FP	C, Si	5±5%	30	0.8	10	64P4B/80P6	3—156
M37450E4SS/FS	PROM Version of M37450M4-XXXSP/FP	C, Si	5±5%	30	0.8	10	64S1B/80S6	
M37450E8-XXXSP/FP ★	One Time Programmable Version of M37450M8-XXXSP/FP	C, Si	5±5%	30	0.8	10	64P4B/80P6	3—174
M37450E8SS/FS ★	PROM Version of M37450M8-XXXSP/FP	C, Si	5±5%	30	0.8	10	64S1B/80D0	
M37450E4TXXXSP/J ★	One Time Programmable Version of M37450M4TXXXSP/J	C, Si	5±5%	30	0.8	10	64P4B/84P0	3—192
M37451E4-XXXSP/FP/GP ★	One Time Programmable Version of M37451M4-XXXSP/FP/GP	C, Si	5±10%	40	0.64	12.5	64P4B/80P6N/ 80P6S	3—210
M37451E4SS/FS ★	PROM Version of M37451M4-XXXSP/FP	C, Si	5±10%	40	0.64	12.5	64S1B/80D0	
M37451E8-XXXSP/FP/GP ★	One Time Programmable Version of M37451M8-XXXSP/FP/GP	C, Si	5±10%	40	0.64	12.5	64P4B/80P6N/ 80P6S	
M37451E8SS/FS ★	PROM Version of M37451M8-XXXSP/FP	C, Si	5±10%	40	0.64	12.5	64S1B/80D0	
M37451EC-XXXSP/FP/GP★★	One Time Programmable Version of M37451MC-XXXSP/FP/GP	C, Si	5±10%	40	0.64	12.5	64P4B/80P6N/ 80P6S	
M37451ECSS/FS ★★	PROM Version of M37451MC-XXXSP/FP	C, Si	5±10%	40	0.64	12.5	64S1B/80D0	
M37451E4DXXXSP/FP ★★	One Time Programmable Version of M37451M4DXXXSP/FP	C, Si	5±10%	40	0.64	12.5	64P4B/80P6N	3—222
M37451E8DXXXSP/FP ★★	One Time Programmable Version of M37451M8DXXXSP/FP	C, Si	5±10%	40	0.64	12.5	64P4B/80P6N	
M37470E4-XXXSP ★	One Time Programmable Version of M37470M4-XXXSP	C, Si	2.7~5.5	17.5	1	4	32P4B	4—64
M37470E8-XXXSP ★	One Time Programmable Version of M37470M8-XXXSP	C, Si	2.7~5.5	17.5	1	4	32P4B	
M37471E4-XXXSP/FP★	One Time Programmable Version of M37471M4-XXXSP/FP	C, Si	2.7~5.5	17.5	1	4	42P4B/56P6N	4—72
M37471E8-XXXSP/FP★	One Time Programmable Version of M37471M8-XXXSP/FP	C, Si	2.7~5.5	17.5	1	4	42P4B/56P6N	
M37471E8SS ★	PROM Version of M37471M8-XXXSP	C, Si	2.7~5.5	17.5	1	4	42S1B	

★ : New product ★★ : Under development

Note1 : Refer to the "1989 MITSUBISHI SEMICONDUCTORS DATA BOOK ⟨SINGLE-CHIP 8-BIT MICROCOMPUTERS⟩"
2 : Refer to the "1990 MITSUBISHI SEMICONDUCTORS DATA BOOK ⟨SINGLE-CHIP 8-BIT MICROCOMPUTERS Enlarged edition⟩"
3 : Refer to the "1992 MITSUBISHI SEMICONDUCTORS DATA BOOK ⟨SINGLE-CHIP 8-BIT MICROCOMPUTERS⟩ Vol. 1."
※ : The production of this product is no longer planned due to announcement of new series or upgrades.

■Series 38000 single-chip microcomputers

Refer to the "1991 MITSUBISHI SEMICONDUCTORS DATA BOOK ⟨SINGLE-CHIP 8-BIT MICROCOMPUTERS⟩ Vol. 3."

Development support systems (1)

MELPS 740		Assembler	Debug system			For evaluation
Type name	Processor mode		Debugger	Option board	Control software	
M50740A-XXXSP/FP M50741-XXXSP/FP M50740ASP	Single-chip mode	SRA74	PC4000E	PCA4040	RTT74	M50740-PGYS
M50742-XXXSP/FP M50708-XXXSP/FP	Single-chip mode			PCA4042		M50742-PGYS
M50743-XXXSP/FP	Single-chip mode			PCA4043 or PCA4043R		M50743-PGYS
M50744-XXXSP/FP M50744T-XXXSP M50746-XXXSP/FP M50746E-XXXSP/FP M50746ES/EFS	Single-chip mode			PCA4044G02 or PCA4044R		M50746ES/EFS (Note 2)
	Microprocessor mode			PCA4044XG02		
M50745-XXXSP/FP	Single-chip mode			PCA4045 or PCA4045R		M50745-PGYS
M50747-XXXSP/FP M50747H-XXXSP/FP M50747T-XXXSP M50747E-XXXSP/FP M50747ES/EFS	Single-chip mode			PCA4047G02 or PCA4047RG02		M50747ES/EFS (Note 2)
	Microprocessor mode			PCA4047XG02 or PCA4047XRG02		
M50752-XXXSP M50757-XXXSP M50758-XXXSP	Single-chip mode			PCA4057		M50752-PGYS
M50753-XXXSP/FP M50753T-XXXSP	Single-chip mode			PCA4053		M50753-PGYS (Note 2)
M50754-XXXSP/FP/GP M50954-XXXSP/FP/GP M50955-XXXSP/FP/GP	Single-chip mode			PCA4054G02 or PCA4054RG02		M50955-PGYS
M50930-XXXFP M50930T-XXXFP M50931-XXXFP M50932-XXXFP M50933-XXXFP M50934-XXXFP	Single-chip mode			PCA4093 or PCA4093R		M50931-PGYS (Note 2,3)
M50940-XXXSP/FP M50941-XXXSP/FP M50945-XXXSP/FP	Single-chip mode			PCA4094 or PCA4094RG02		M50945-PGYS
M50943-XXXSP/FP	Single-chip mode			PCA4033		PCA4333G02 (Note 1)
M50944-XXXSP/FP M50944E-XXXSP/FP M50944ES	Single-chip mode			PCA7044		M50944ES
M50950-XXXSP M50951-XXXSP	Single-chip mode			PCA4095		M50950-PGYS
M50957-XXXSP/FP M50957E-XXXSP M50957ES M50958-XXXSP/FP M50959-XXXSP/FP	Single-chip mode			PCA4054G02 or PCA4054RG02		M50957-PGYS M50957ES
M50963-XXXSP/FP M50963E-XXXSP/FP M50963ES/EFS M50964-XXXSP/FP	Single-chip mode			PCA4064 or PCA4064R		M50963ES/EFS

★ : New products ★★ : Under development

Note 1 : Evaluation board

2 : Notes for operating temperature range about the extended operating temperature version microcomputer.

3 : Notes for supply voltage range about the M50932-XXXFP, M50933-XXXFP.

Development support systems (2)

MELPS 740		Assembler	Debug system			For evaluation
Type name	Processor mode		Debugger	Option board	Control software	
M37100M8-XXXSP/FP	Single-chip mode	SRA74	PC4000E	M37100T-OPT or M37100T2-RTT	RTT74	M37100P-000SS
M37102M8-XXXSP/FP M37102E8-XXXSP/FP M37102E8SS/FS	Single-chip mode			M37102T-RTT		M37102E8SS/FS★★
M37103M4-XXXSP	Single-chip mode			M37100T2-RTT		—
M37120M6-XXXFP M37120E6-XXXFP	Single-chip mode			M37120T-RTT		M37120E6-XXXFP★
M37201M6-XXXSP M37201E6-XXXSP M37201E6SS	Single-chip mode		PC4000E + PC4600★	M37201T5-POD★		M37201E6SS★★
M37202M3-XXXSP M37202E3-XXXSP M37202E3SS						M37202E3SS★★
M37204M8-XXXSP M37204E8-XXXSP M37204E8SS						M37204E8SS★★
M37250M6-XXXSP M37250E6-XXXSP M37250E6SS	Single-chip mode		PC4000E	M37250T-RTT★		M37250E6SS★★
M37260M6-XXXSP M37260E6-XXXSP M37260E6SS	Single-chip mode		PC4000E + PC4600★	M37260T5-POD★		M37260E6SS★★
	Microprocessor mode		PC4000E	M37260TX-OPT★ (Be necessary to order producing this board)		
M37408M2-XXXSP/FP	Single-chip mode			—		—
M37409M2-XXXSP/FP	Single-chip mode			M37409T-OPT		M37409PSS★
M37410M3HXXXFP M37410M4HXXXFP M37410M6HXXXFP M37410E6HXXXFP M37410E6HFS	Single-chip mode			M37410T-OPT		M37410E6HFS
M37412M4-XXXFP M37412E5-XXXFP	Single-chip mode			M37412T-OPT		M37412E5-XXXFP
M37413M4HXXXFP M37413M6HXXXFP M37413E6HXXXFP M37413E6HFS	Single-chip mode			M37413T-RTT		M37413E6HFS★★
M37414M5-XXXFP M37414E5-XXXFP	Single-chip mode			M37414T-RTT		M37414E5-XXXFP★
M37415M4-XXXFP	Single-chip mode			M37415T-OPT		M37415PFS
M37416M2-XXXSP/FP	Single-chip mode			M37416T-RTT★		—
M37420M4-XXXSP M37420M6-XXXSP M37420E6-XXXSP M37420E6SS	Single-chip mode			M37420T-OPT		M37420E6SS★
M37421M6-XXXSP/FP	Single-chip mode			M37421T-OPT		M37421P-000SS M37421P-001SS
M37424M8-XXXSP M37424E8-XXXSP M37424E8SS	Single-chip mode			M37424T-RTT★		M37424E8SS★★
M37524M4-XXXSP M37524E4-XXXSP M37524E4SS	Single-chip mode			M37524T-RTT★		M37524E4SS★★
M37428M4-XXXFP	Single-chip mode		PC4000E + PC4600★(Note2)	M37428RFS		—

★ : New products ★★ : Under development
Note 1 : Evaluation board Note 2 : Be necessary to order exchanging the monitor ROM.

Development support systems (3)

MELPS 740		Assembler	Debug system			For evaluation
Type name	Processor mode		Debugger	Option board	Control software	
M50734SP/FP M50734SP-10	—		PC4000E	PCA4034G02 or PCA4034RG02		—

Development support systems (4) series 7450

Series 7450		Assembler	Debug system					For evaluation
			Control software	Base PC4000E		Base PC4600		
Type name	Processor mode			Debugger	Option board	Debugger	Emulator MCU	
M37450M2-XXXSP/FP	Single-chip mode	SRA74	RTT74 (Note 1)	PC4000E	M37450T-OPT or M37450T-RTT	PC4000E + PC4600★	M37450RSS or M37450RFS (Note 2)	M37450PSS/PFS, M37450E4SS/FS or M37450E8SS/FS★ (Note 3)
M37450M4-XXXSP/FP								
M37450M4TXXXSP/J								
M37450M8-XXXSP/FP								
M37450E4-XXXSP/FP	Microprocessor mode				M37450TX-OPT or M37450TX-RTT			
M37450E4TXXXSP/J								
M37450E4SS/FS								
M37450E8-XXXSP/FP								
M37450E8SS/FS								
M37450S1SP/FP	Microprocessor mode							
M37450S2SP/FP								
M37450S4SP/FP								
M37451M4-XXXSP/FP/GP				—			M37451RSS or M37451RFS (Note 2)	M37451E4SS/FS★, M37451E8SS/FS★ or M37451ECSS/FS★★ (Note 3)
M37451M8-XXXSP/FP/GP								
M37451MC-XXXSP/FP/GP								
M37451E4-XXXSP/FP/GP	Single-chip mode							
M37451E4SS/FS								
M37451E8-XXXSP/FP/GP								
M37451E8SS/FS								
M37451EC-XXXSP/FP/GP								
M37451ECSS/FS	Microprocessor mode							
M37451M4DXXXSP/FP								
M37451M8DXXXSP/FP								
M37451E4DXXXSP/FP								
M37451E8DXXXSP/FP								
M37451SSP/FP/GP	Microprocessor mode							

★ : New products

Note 1 : PC4600 is supported by software version up.

2 : Pitch converter PCA4932 is necessary to RFS type.

3 : Notes for operating temperature range about the extended operating temperature version microcomputer

Development support systems (5) series 7470

Series 7470		Assembler	Debug system			For evaluation
Type name	Processor mode		Control software	Debugger	Emulator MCU	
M37470M2-XXXSP	Single-chip mode	SRA74	RTT74 (Note 1)	PC4000E + PC4600★	M37471RSS (Note 2,3)	M37470E4-XXXSP★ M37470E8-XXXSP★
M37470M4-XXXSP						
M37470M8-XXXSP						
M37470E4-XXXSP						
M37470E8-XXXSP						
M37471M2-XXXSP/FP						M37471E8SS★
M37471M4-XXXSP/FP						
M37471M8-XXXSP/FP						
M37471E4-XXXSP/FP						
M37471E8-XXXSP/FP						
M37471E8SS						

★ : New products

Note 1 : PC4600 is supported by software version up.

2 : Pitch converter PCA4906 is necessary to M37470

3 : Pitch converter PCA4907 is necessary to QFP package type.

Development support systems (6) series 38000

Type name	Assembler	Debug system			For evaluation
		Control software	Debugger	Emulation MCU	
M38002M2-XXXSP/FP M38002E2-XXXSP/FP M38002E2SS/FS M38002M4-XXXSP/FP M38002E4-XXXSP/FP M38002E4SS/FS M38003M6-XXXSP/FP M38003E6-XXXSP/FP M38003E6SS/FS M38004M8-XXXSP/FP M38004E8-XXXSP/FP M38004E8SS/FS M38007M4-XXXSP/FP M38007E4-XXXSP/FP M38007E4SS/FS	SRA74	RTT74 (Note 1)	PC4000E + PC4600★	M38007RSS (Note 2)	M38002E2SS/FS M38002E4SS/FS M38003E6SS/FS M38004E8SS/FS M38007E4SS/FS
M38042M3-XXXFP M38042E3-XXXFP M38042E3FS				Under development	M38042E3FS
M38062M3-XXXFP/GP M38062E3-XXXFP/GP M38062E3FS M38062M4-XXXFP/GP M38062E4-XXXFP/GP M38062E4FS M38063M6-XXXFP/GP M38063E6-XXXFP/GP M38063E6FS M38064M8-XXXFP/GP M38064E8-XXXFP/GP M38064E8FS				M38067RFS (Note 3)	M38062E3FS M38062E4FS M38063E6FS M38064E8FS
M38102M5-XXXSP/FP M38102E5-XXXSP/FP M38102E5SS M38103M6-XXXSP/FP M38103E6-XXXSP/FP M38103E6SS				M38107RSS (Note 2)	M38102E5SS M38103E6SS
M38112M4-XXXSP/FP M38112E4-XXXSP/FP M38112E4SS				M38117RSS (Note 2)	M38112E4SS
M38172M4-XXXFP M38172E4-XXXFP M38172E4FS M38173M6-XXXFP M38173E6-XXXFP M38173E6FS M38174M8-XXXFP M38174E8-XXXFP M38174E8FS				M38177RFS (Note 3)	M38172E4FS M38173E6FS M38174E8FS
M38184M8-XXXFP M38184E8-XXXFP M38184E8FS				M38187RFS★★ (Note 3)	M38184E8FS

★ : New products ★★ : Under development

Note 1 : PC 4600 is supported by software version up

2 : Pitch converter M38007T-PRB is necessary to QFP package type.

3 : Pitch converter PCA4932 is necessary.

Program writing adapter for built-in PROM type microcomputers

Built-in PROM type microcomputers type name	Program writing adapter
M50746E-XXXSP	PCA4700G02
M50746ES	
M50746EFS	PCA4701G02
M50746E-XXXFP	
M50747E-XXXSP	PCA4700G02
M50747ES	
M50747E-XXXFP	PCA4701G02
M50747EFS	
M50944E-XXXSP	PCA4715
M50944ES	
M50944E-XXXFP	PCA4714
M50957E-XXXSP	PCA4703
M50957ES	
M50963E-XXXSP	PCA4700G02
M50963ES	
M50963E-XXXFP	PCA4701G02
M50963EFS	
M37102E8-XXXSP	PCA4724
M37102E8SS	
M37102E8-XXXFP	PCA4725
M37102E8FS	
M37120E6-XXXFP	PCA4716(Note 1)
M37201E6-XXXSP	PCA4723
M37201E6SS	
M37202E3-XXXSP	PCA4726★
M37202E3SS	
M37204E8-XXXSP	
M37204E8SS	
M37250E6-XXXSP	
M37250E6SS	
M37260E6-XXXSP	PCA4736★
M37260E6SS	
M37260E6-XXXFP	PCA4737★
M37260E6FS	
M37410E6HXXXFP	PCA4705
M37410E6HFS	PCA4706
M37412E5-XXXFP	PCA4720
M37413E6HXXXFP	PCA4728
M37413E6HFS	PCA4729
M37414E5-XXXFP	PCA4720
M37420E6-XXXSP	PCA4727
M37420E6SS	
M37424E8-XXXSP	PCA4721
M37424E8SS	
M37524E8-XXXSP	
M37524E8SS	
M37450E4-XXXSP	PCA4710
M37450E4SS	
M37450E8-XXXSP	
M37450E8SS	
M37451E4-XXXSP	
M37451E4SS	
M37451E8-XXXSP	
M37451E8SS	
M37451EC-XXXSP	

Program writing adapter for built-in PROM type microcomputers (continued)

Built-in PROM type microcomputers type name	Program writing adapter
M37451ECSS	PCA4710
M37450E4TXXXSP	
M37450E4TXXXJ	PCA4712(Note 1)
M37450E4-XXXFP	PCA4711
M37450E4FS	
M37450E8-XXXFP	
M37450E8FS	PCA4719
M37451E4FS	
M37451E8FS	
M37451ECFS	
M37451E4-XXXFP	PCA4751★
M37451E8-XXXFP	
M37451EC-XXXFP	
M37451E4-XXXGP	PCA4752★
M37451E8-XXXGP	
M37451EC-XXXGP	
M37451E4DXXXSP	PCA4710
M37451E8DXXXSP	
M37451E4DXXXFP	PCA4751★
M37451E8DXXXFP	
M37460E8-XXXFP	PCA4713(Note 1)
M37470E4-XXXSP	PCA4730
M37470E8-XXXSP	
M37471E4-XXXSP	
M37471E8-XXXSP	
M37471E8SS	
M37471E4-XXXFP	PCA4731
M37471E8-XXXFP	
M38002E2-XXXSP	Under development
M38002E2-XXXFP	
M38002E2SS	
M38002E2FS	
M38002E4-XXXSP	PCA4738S-64
M38002E4-XXXFP	PCA4738F-64
M38002E4SS	PCA4738S-64
M38002E4FS	PCA4738L-64★★
M38003E6-XXXSP	Under development
M38003E6-XXXFP	
M38003E6SS	
M38003E6FS	
M38004E8-XXXSP	
M38004E8-XXXFP	
M38004E8SS	
M38004E8FS	
M38007E4-XXXSP	
M38007E4-XXXFP	
M38007E4SS	
M38007E4FS	
M38042E3-XXXFP	
M38042E3FS	
M38062E3-XXXFP	
M38062E3-XXXGP	
M38062E3FS	

★ : New product ★★ : Under development
Note 1 : Be necessary to order producing this board.

Program writing adapter for built-in PROM type microcomputers (continued)

Built-in PROM type microcomputers type name	Program writing adapter
M38062E4-XXXFP	Under development
M38062E4-XXXGP	
M38062E4FS	
M38063E6-XXXFP	PCA4738F-80
M38063E6-XXXGP	PCA4738G-80
M38063E6FS	PCA4738L-80
M38064E8-XXXFP	Under development
M38064E8-XXXGP	
M38064E8FS	
M38102E5-XXXSP	PCA4738S-64
M38102E5-XXXFP	PCA4738F-64
M38102E5SS	PCA4738S-64
M38103E6-XXXSP	Under development
M38103E6-XXXFP	
M38103E6SS	
M38112E4-XXXSP	PCA4738S-64
M38112E4-XXXFP	PCA4738F-64
M38112E4SS	PCA4738S-64
M38172E4-XXXFP	Under development
M38172E4FS	
M38173E6-XXXFP	
M38173E6FS	
M38174E8-XXXFP	
M38174E8FS	
M38184E8-XXXFP	PCA4738F-100★
M38184E8FS	Under development

★ : New product ★★ : Under development

FUNCTION CODE

Mitsubishi integrated circuits may be ordered using the following simplified alphanumeric type-codes which define the function of the IC/LSIs and the package style.

1. Mitsubishi Original Products

Example 1. **M 5 07 40 - 001 SP -2**

M : Mitsubishi integrated prefix

Temperature range
5 : Standard industrial/commercial
(0 to 70/75℃ or −20 to 85℃)
9 : High reliability

Series designation using 1 or 2 alphanumeric chracters.
01~09 : CMOS
1 : Linear circuit
3 : TTL
10~19 : Linear circuit
32~33 : TTL
41~47 : TTL (the others)
81 : P-channel aluminum-gate MOS
84 : CMOS
85 : P-channel silicon-gate MOS
86 : P-channel aluminum-gate MOS
87 : N-channel silicon-gate MOS
88 : P-channel aluminum-gate ED-MOS
89 : CMOS
9 : DTL
S0~S2 : Schottky TTL

Circuit function identification code using 2 digits.
A character next to 2-digit alphanumeric characters, "T", is represented using for automobile/industrial

Mask ROM number.

Package style
K : Glass-sealed ceramic flat package
P : Molded plastic
FP : Molded plastic flat package
GP : Molded plastic flat package
SP : Molded plastic shrink package
S : Metal-sealed ceramic

Electrical characteristic identification code using 1 or 2 digits.

ORDERING INFORMATION

Example 2. **M 3 74 50 E 4 - 001 SP**

M : Mitsubishi integrated prefix

3 : Represent an original single-chip microcomputer

Series designation using 2 alphanumeric chracters

Circuit function identification code using 2 digits

Memory identification code using a digit
E : EPROM
M : Mask ROM
N : Mask ROM+EEPROM
P : Piggyback
S : External ROM

Memory size identification code using a digit

Normally, using hyphen.
When electrical characteristic, or division of quality identification code using alphanumeric character.
T : For automobile/industrial

Mask ROM number

Package style
J : PLCC, or SOJ package
K : Glass-sealed ceramic flat package
P : Molded plastic DIP
FP : Molded plastic flat package
FS : Ceramic flat package
GP : Molded plastic flat package
SP : Molded plastic shrink package
S : Ceramic (layered type) package
SS : Ceramic shrink package

2. PACKAGE CODE

Package style may be specified by using the following simplified alphanumeric code.

Example : 42 P 4 B

Number of pins

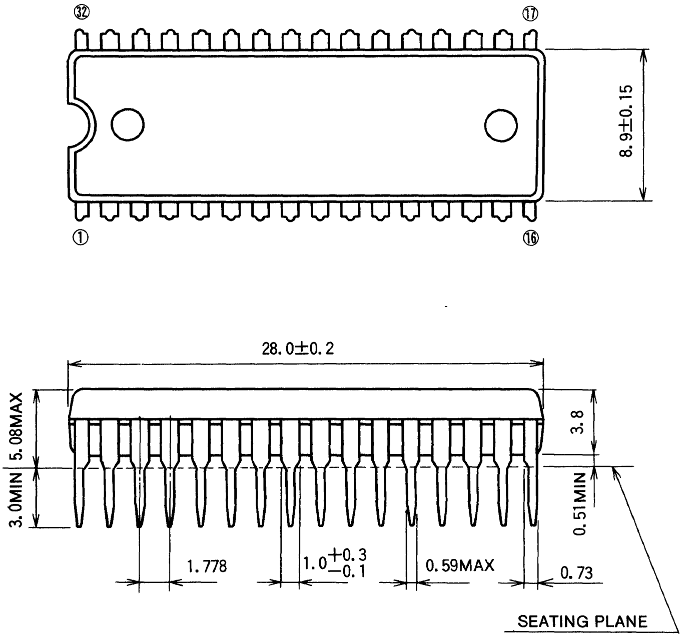
Package structure
K : Glass-sealed ceramic
P : Molded plastic
S : Metal-sealed ceramic

Package outline
1 : DIP
2 : SOP
4 : DIP
6 : QFP

Secondary outline code
Special-purpose secondary codes describing outline are included as necessary. For details, contact your sales representative.

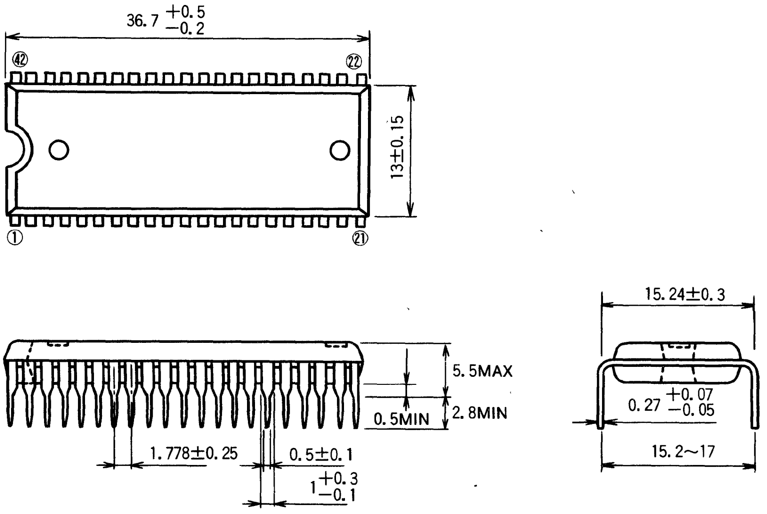
32P4B 32pin molded plastic DIP

Dimension in mm



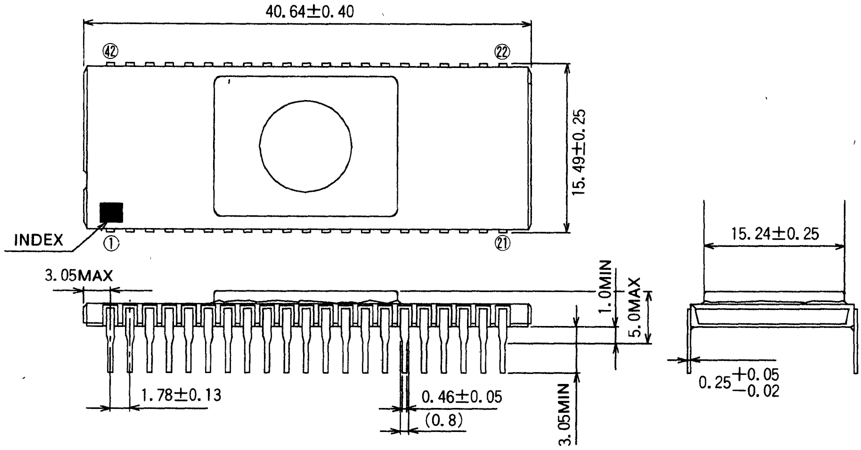
42P4B 42pin molded plastic DIP

Dimension in mm



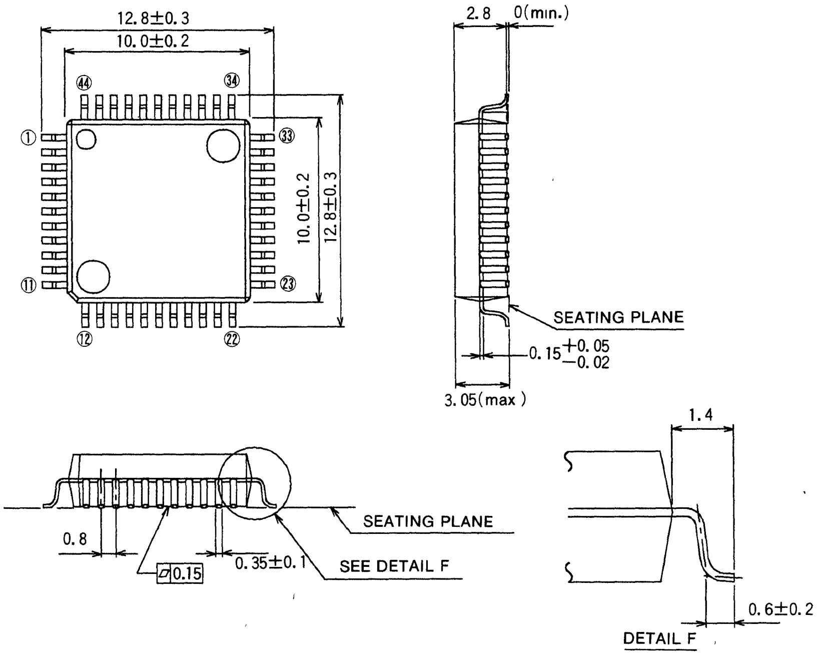
42S1B 42pin ceramic DIP

Dimension in mm



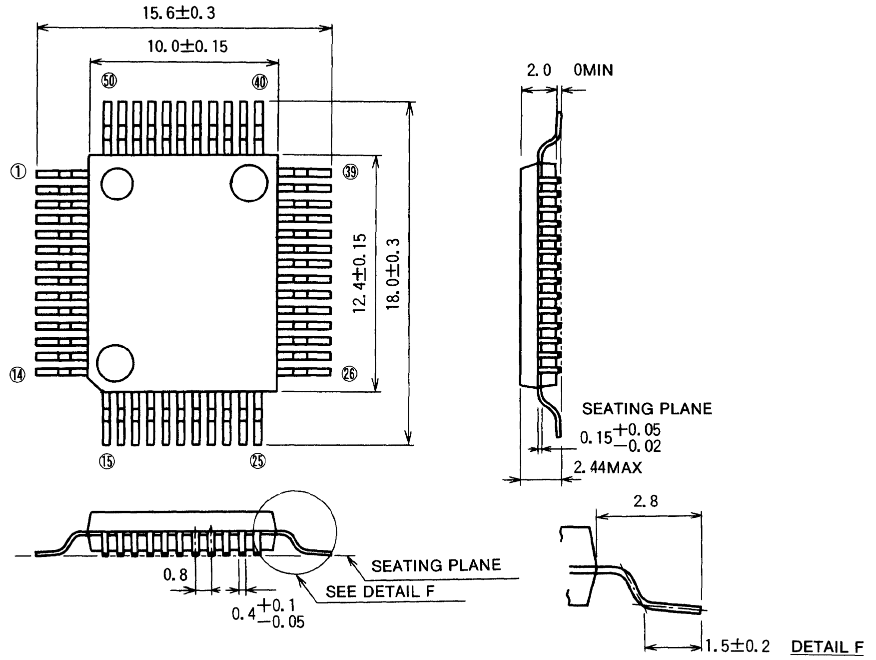
44P6N Plastic 44pin QFP

Dimension in mm



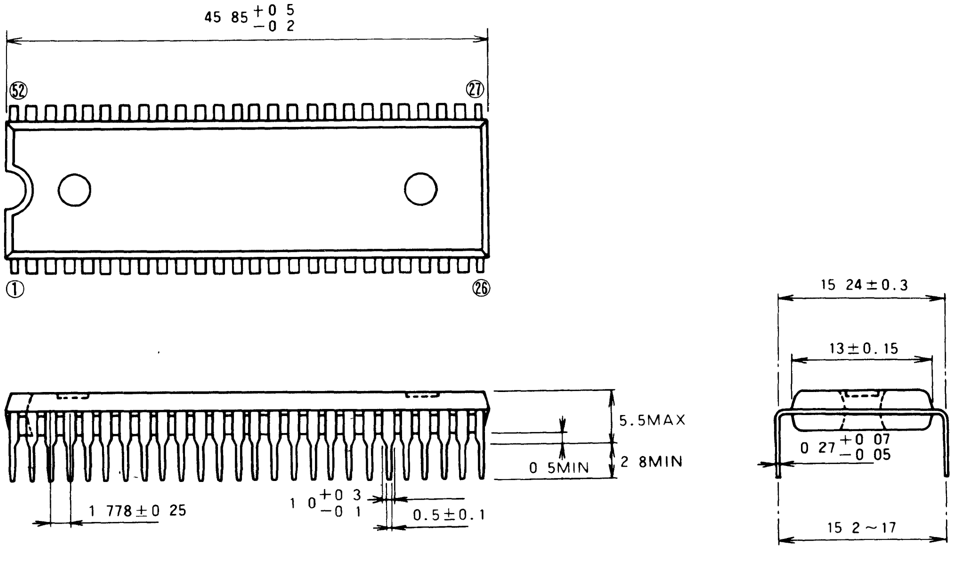
50P6 50pin molded plastic QFP

Dimension in mm



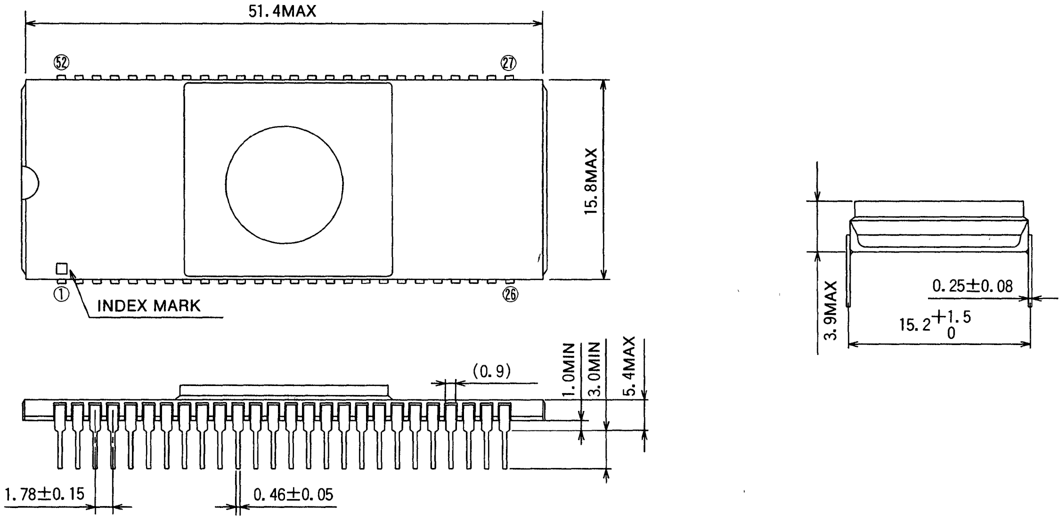
52P4B 52pin molded plastic DIP

Dimension in mm



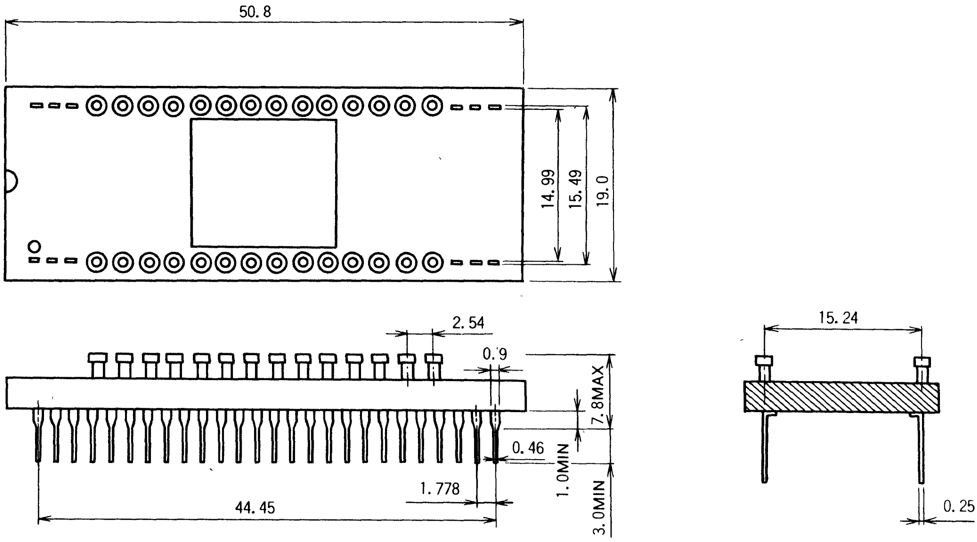
52S1 52pin ceramic DIP

Dimension in mm



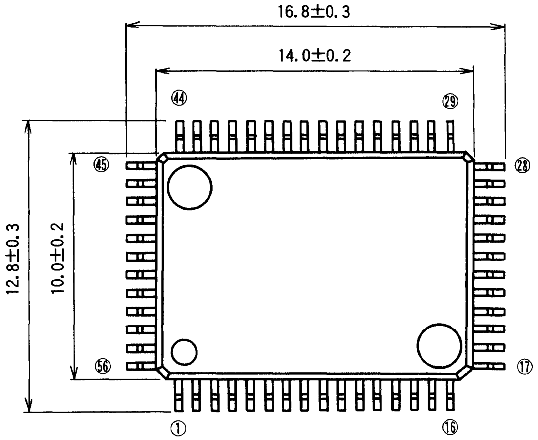
52S1M 52pin piggyback DIP

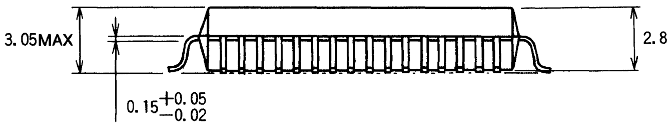
Dimension in mm

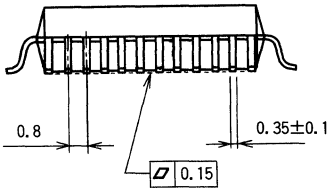


56P6N | **56pin molded plastic QFP**

Dimension in mm

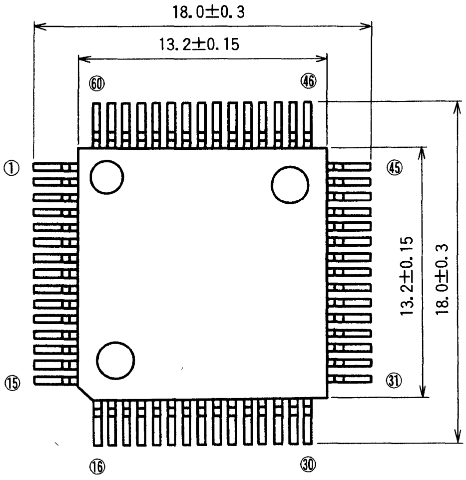


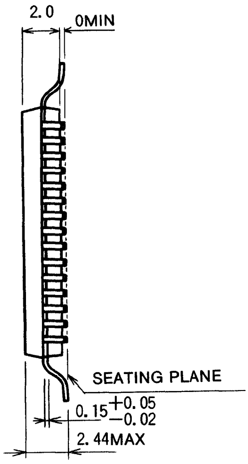


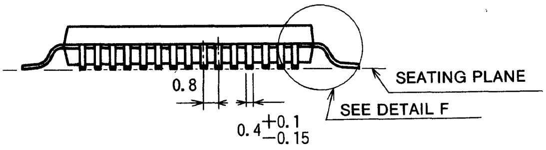


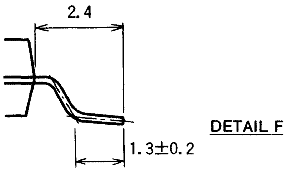
6 0P6 | **60pin molded plastic QFP**

Dimension in mm



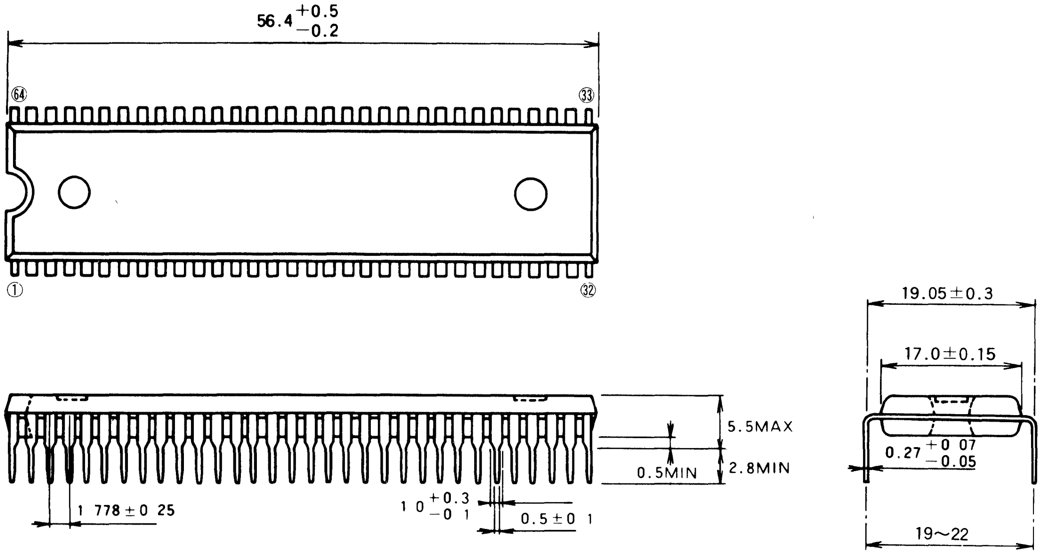






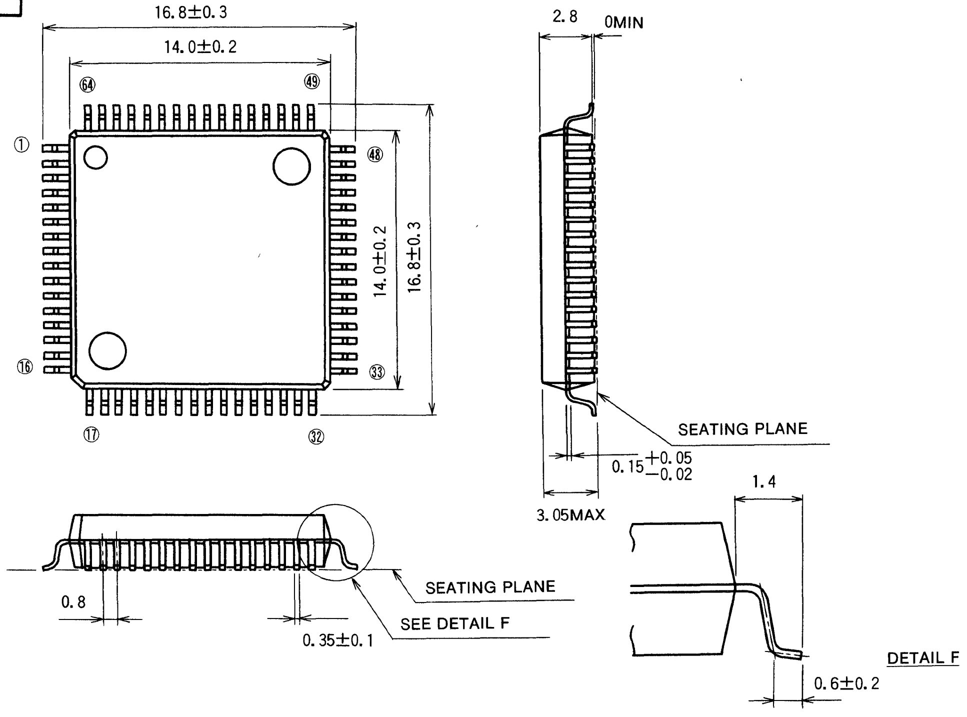
64P4B 64pin molded plastic DIP(Lead pitch 1.778mm)

Dimension in mm

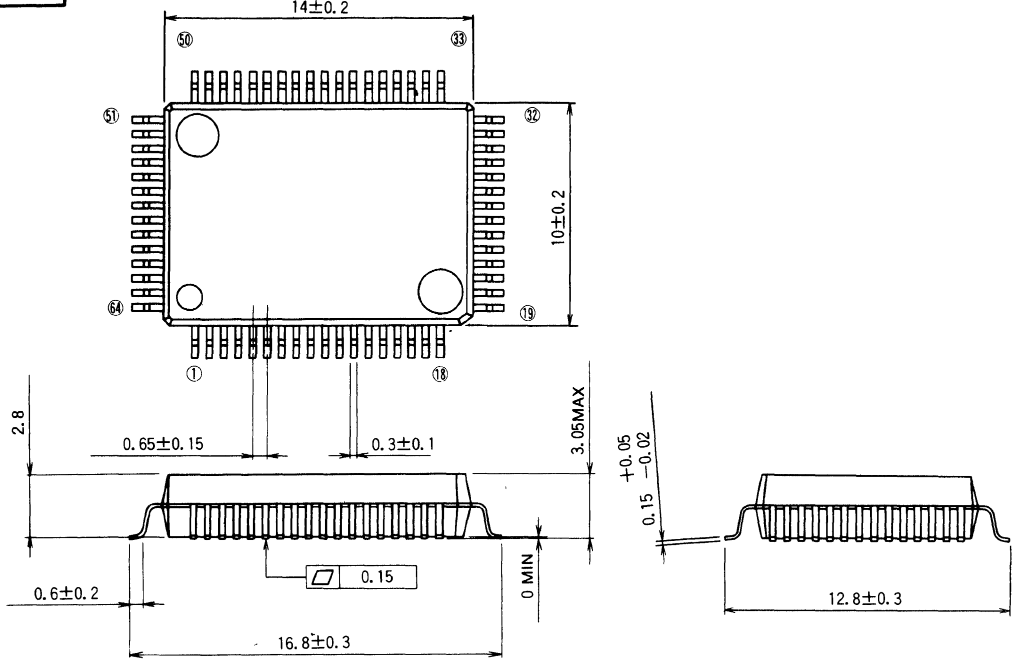


64P6N 64pin molded plastic QFP

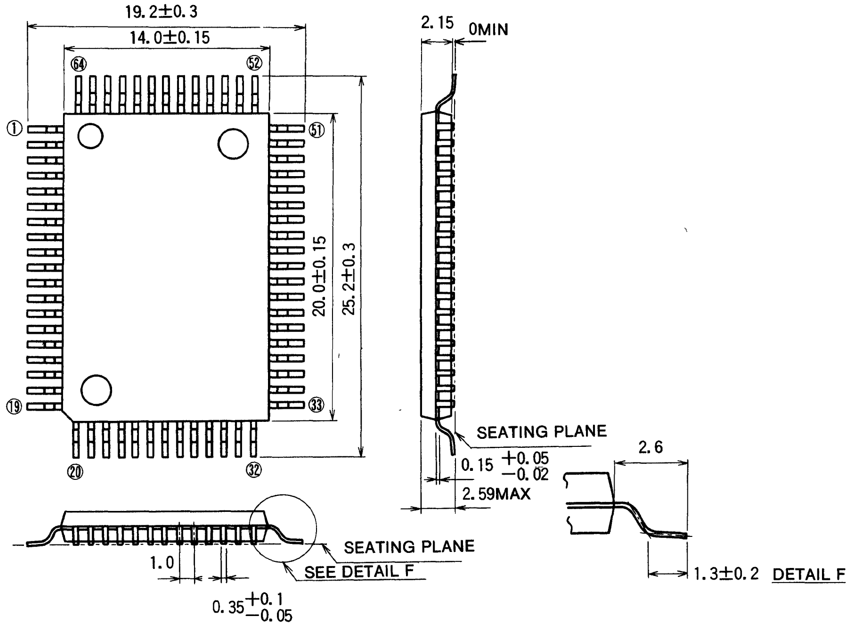
Dimension in mm



64P6S **64pin molded plastic QFP** Dimension in mm

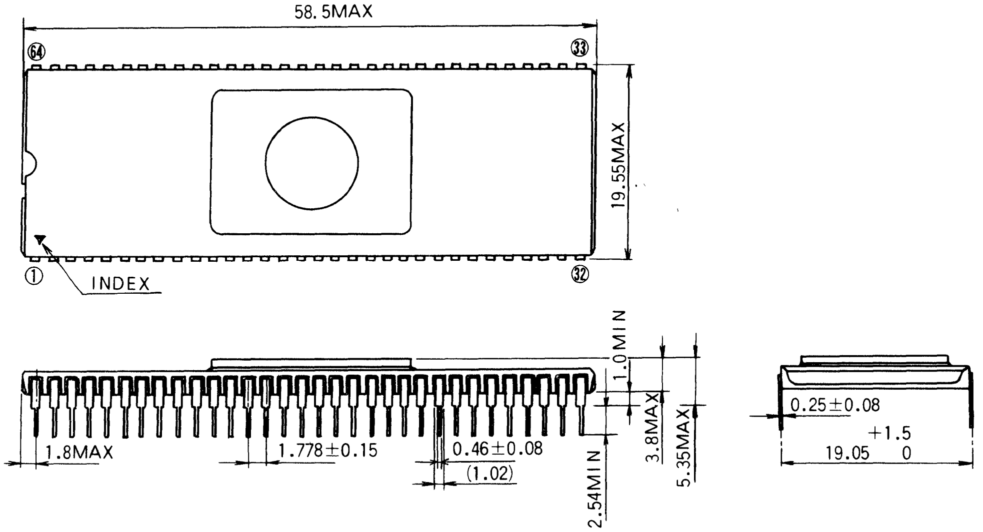


64P6W **64pin molded plastic QFP** Dimension in mm



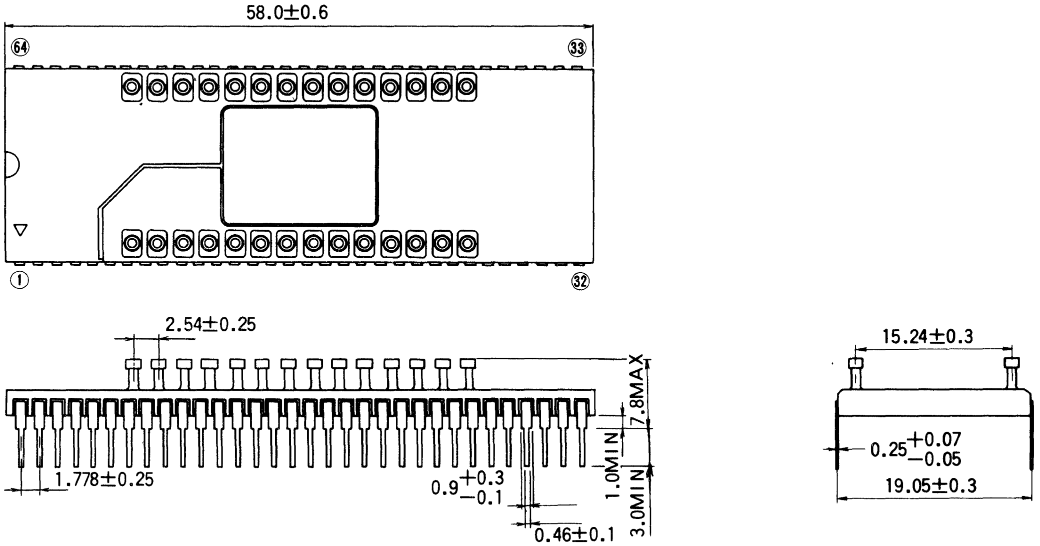
64S1B 64pin ceramic DIP

Dimension in mm



64S1M 64pin piggyback DIP

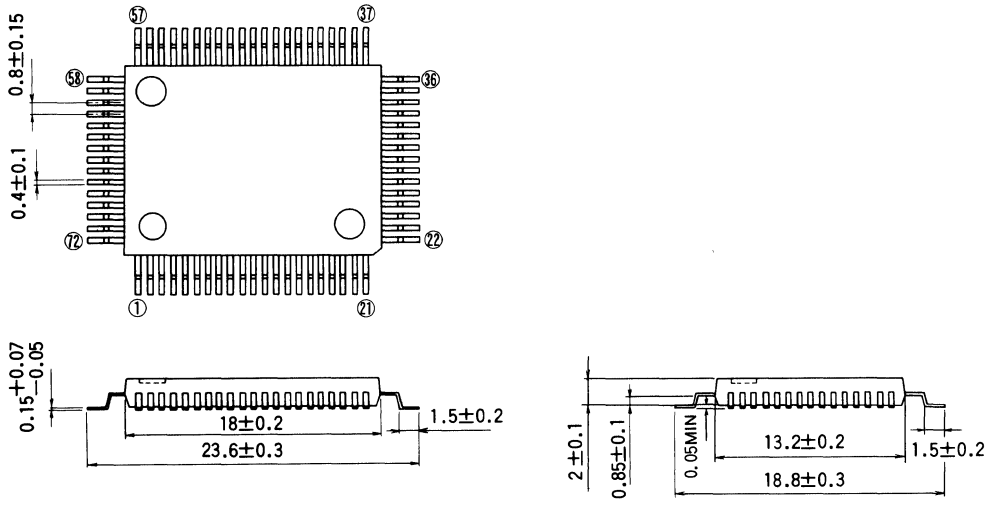
Dimension in mm



PACKAGE OUTLINES

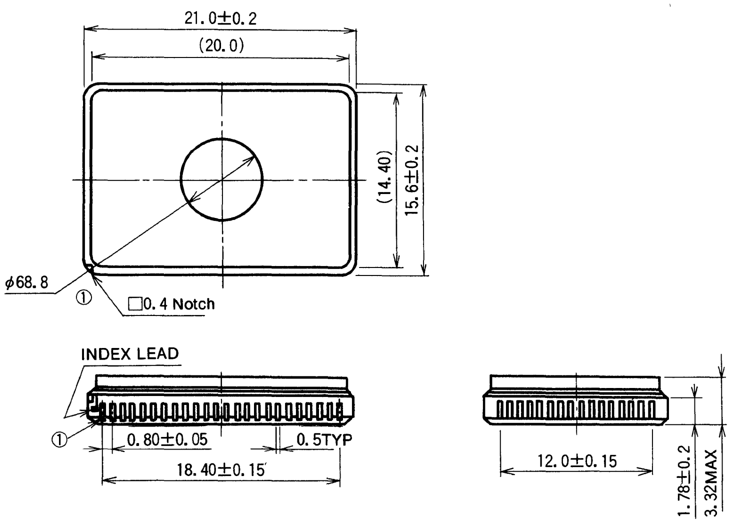
72P6 72pin molded plastic QFP

Dimension in mm



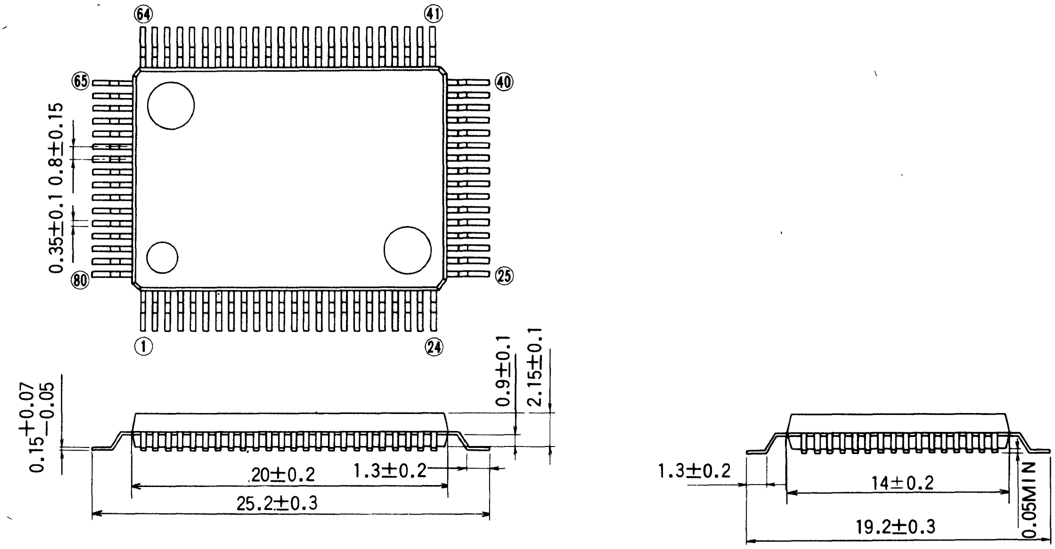
80D0 80pin molded ceramic LCC

Dimension in mm



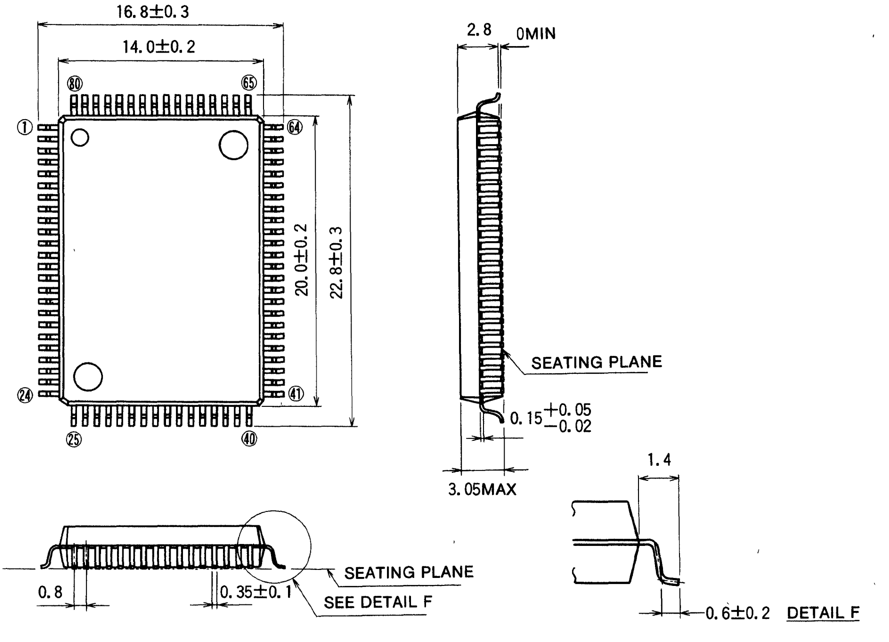
80P6 80pin molded plastic QFP

Dimension in mm



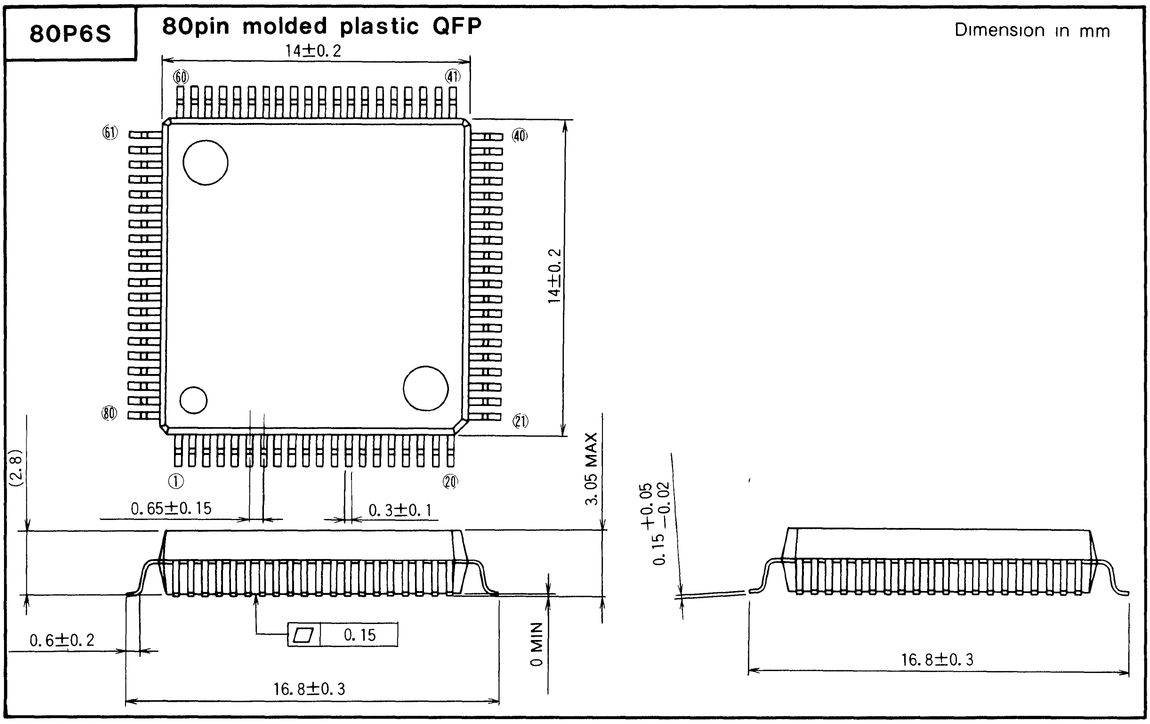
80P6N 80pin molded plastic QFP

Dimension in mm



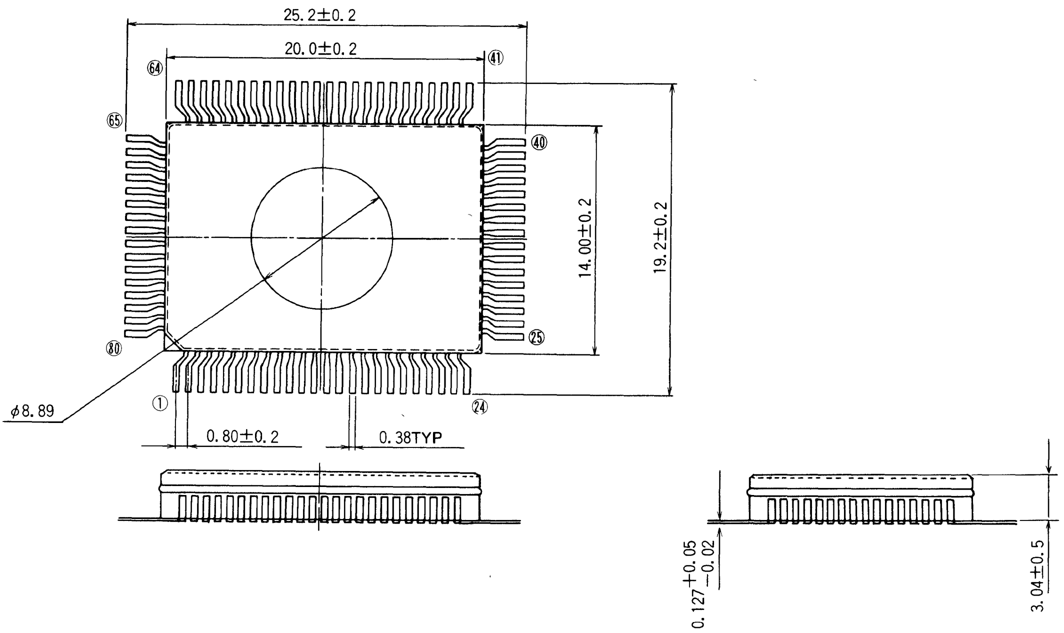
80P6S 80pin molded plastic QFP

Dimension in mm



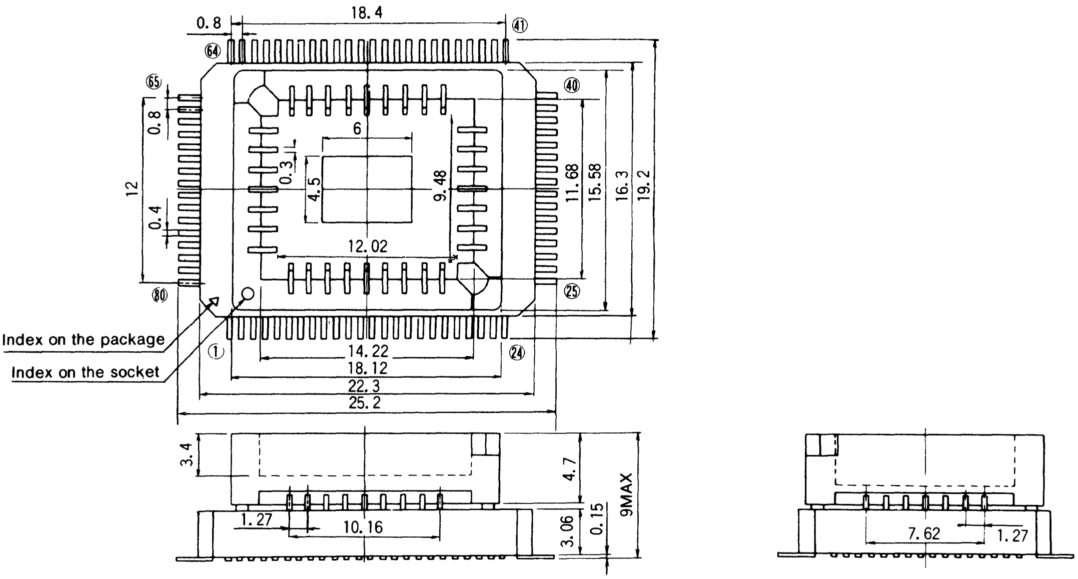
80S6 80pin molded ceramic QFP

Dimension in mm



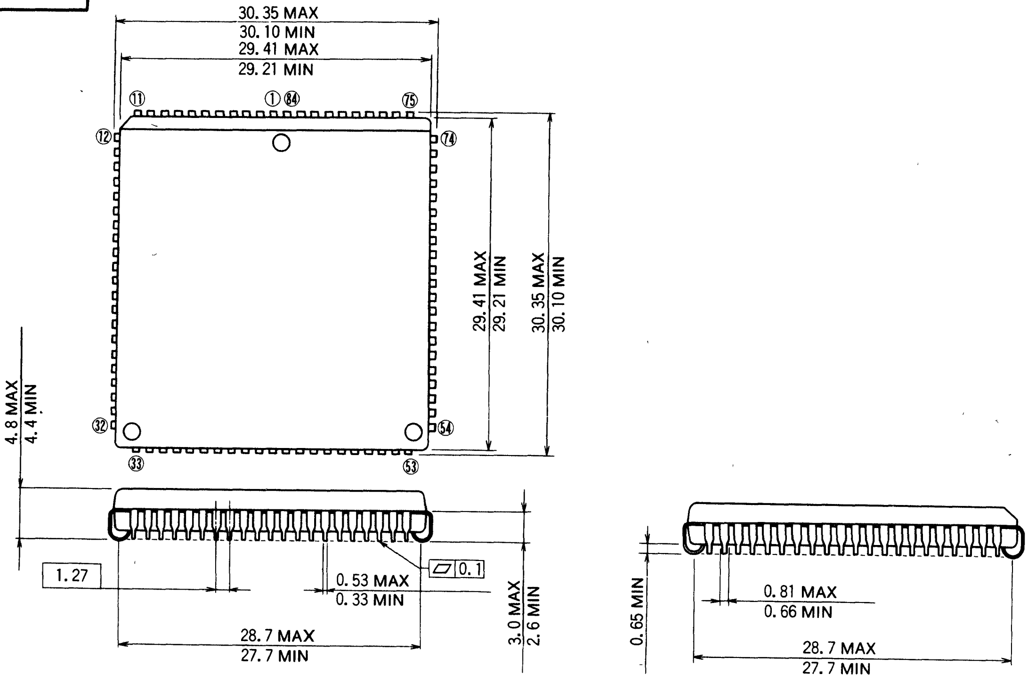
80S6M **80pin piggyback QFP**

Dimension in mm

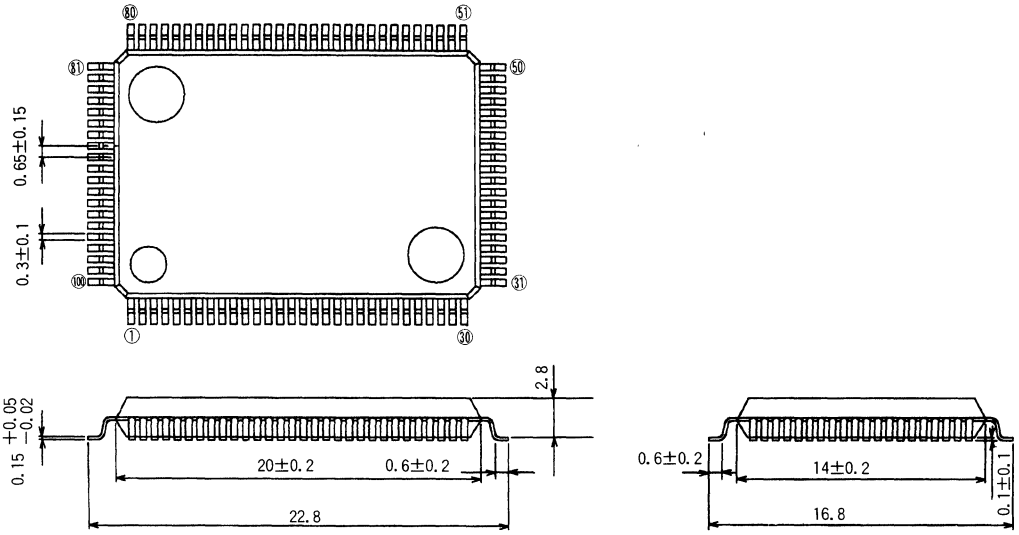


84P0 **84pin molded plastic leaded chip carrier**

Dimension in mm



100P6S	Plastic 100pin QFP	Dimension in mm



LETTER SYMBOLS FOR THE DYNAMIC PARAMETERS

1. INTRODUCTION

A system of letter symbols to be used to represent the dynamic parameters of intergrated circuit memories and other sequential circuits especially for single-chip microcomputers, microprocessors and LSIs for peripheral circuits has been discussed internationally in the TC47 of the International Electrotechnical Committee (IEC). Finally the IEC has decided on the meeting of TC47 in February 1980 that this system of letter symbols will be a Central Office document and circulated to all countries to vote which means this system of letter symbols will be a international standard.

The system is applied in this LSI data book for the new products only. Future editions of this data book will be applied this system. The IEC document which describes "Letter symbols for dynamic parameters of sequential integrated circuits, including memories" is introduced below. In this data book, the dynamic parameters in the IEC document are applied to timing requirements and switching characteristics.

2. LETTER SYMBOLS

The system of letter symbols outlined in this document enables symbols to be generated for the dynamic parameters of complex sequential circuits, including memories, and also allows these symbols to be abbreviated to simple mnemonic symbols when no ambiguity is likely to arise.

2.1. General Form

The dynamic parameters are represented by the general symbol of the form:-

$t_{A(BC-DC)F}$ .... (1)

where :

Subscript A indicates the type of dynamic parameter being represented, for example; cycle time, setup time, enable time, etc.

Subscript B indicates the name of the signal or terminal for which a change of state or level (or establishment of a state or level) constitutes a signal event assumed to occur first, that is, at the beginning of the time interval. If this event actually occurs last, that is, at the end of the time interval, the value of the time interval is negative.

Subscript C indicates the direction of the transition and/or the final state or level of the signal represented by B. When two letters are used, the initial state or level is also indicated.

Subscript D indicates the name of the signal or terminal for which a change of state or level (or establishment of a state or level) constitutes a signal event assumed to occur last, that is, at the end of the time interval. If this event actually occurs first, that is, at the beginning of the time interval, the value of the time interval is negative.

Subscript E indicates the direction of the transition and/or the final state or level of the signal represented by D. When two letters are used, the initial state or level is also indicated.

Subscript F indicates additional information such as mode of operation, test conditions, etc.

Note 1 Subscripts A to F may each consists of one or more letters

2 Subscripts D and E are not used for transition times

3 The "–" in the symbol (1) above is used to indicate "to", hence the symbol represents the time interval from signal event B occuring to signal event D occuring, and it is important to note that this convention is used for all dynamic parameters including hold times Where no misunderstanding can occur the hyphen may be omitted

2.2. Abbreviated Form

The general symbol given above may be abbreviated when no misunderstanding is likely to arise. For example to :

$t_{A(B-D)}$

or $t_{A(B)}$

or $t_{A(D)}$ – often used for hold times

or t_{AF} – no brackets are used in this case

or t_{A}

or t_{BC-DE} – often used for unclassified time intervals

2.3. Allocation of Subscripts

In allocating letter symbols for the subscripts, the most commonly used subscripts are given single letters where practicable and those less commonly used are designated by up to three letters. As far as possible, some form of mnemonic representation is used. Longer letter symbols may be used for specialised signals or terminals if this aids understanding.

3. SUBSCRIPT A (For Type of Dynamic Parameter

The subscript A represents the type of dynamic parameter to be designated by the symbol and, for memories, the parameters may be divided into two classes :

a) those that are timing requirements for the memory and

b) those that are characteristics of the memory. The letter symbols so far proposed for memory circuits are listed in sub-clauses 3.1 and 3.2 below.
All subscripts A should be in lower-case.

3.1. Timing Requirements

The letter symbols for the timing requirements of semiconductor memories are as follows :

Term	Subscript
Cycle time	c
Time interval between two signal events	d
Fall time	f
Hold time	h
Precharging time	pc
Rise time	r
Recovery time	rec
Refresh time interval	rf
Setup time	su
Transition time	t
Pulse duration (width)	w

3.2. Characteristics

The letter symbols for the dynamic characteristics of semiconductor memories are as follows :

Characteristic	Subscript
Access time	a
Disable time	dis
Enable time	en
Propagation time	P
Recovery time	rec
Transition time	T
Valid time	v

Note Recovery time for use as a characteristic is limited to sense recovery time

4. SUBSCRIPTS B AND D
(For Signal Name or Terminal Name)

The letter symbols for the signal name or the name of the terminal are as given below.
All subscripts B and D should be in upper-case.

Signal or terminal	Subscript
Address	A
Clock	C
Column address	CA
Column address strobe	CAS
Data input	D
Data input/output	DQ
Chip enable	E
Erasure	ER
Output enable	G
Program	PR
Data output	Q
Read	R
Row address	RA
Row address strobe	RAS
Refresh	RF
Read/Write	RW
Chip select	S
Write (write enable)	W

Note 1 In the letter symbols for time intervals, bars over the subscripts, for example CAS, should not be used
2 It should be noted, when further letter symbols are chosen, that the subscript should not end with H, K, V, X, or Z (See clause 5)
3 If the same terminal, or signal, can be used for two functions (for example Data input/output, Read/Write) the waveform should be labelled with the dual function, if appropriate, but the symbols for the dynamic parameters should include only that part of the subscript relevant to the parameter

5. SUBSCRIPTS C AND E
(For Transition of Signal)

The following symbols are used to represent the level or state of a signal :

Transition of signal	Subscript
High logic level	H
Low logic level	L
Valid steady-state level (either low or high)	V
Unknown, changing, or 'don't care' level	X
High-impedance state of three-state output	Z

The direction of transition is expressed by two letters, the direction being from the state represented by the first letter to that represented by the second letter, with the letters being as given above.
When no misunderstanding can occur, the first letter may be omitted to give an abbreviated symbol for subscripts C and E as indicated below.
All subscripts C and E should be in upper-case.

Examples	Subscript	
	Full	Abbreviated
Transition from high level to low level	HL	L
Transition from low level to high level	LH	H
Transition from unknown or changing state to valid state	XV	V
Transition from valid state to unknown or changing state	VX	X
Transition from high-impedance state to valid state	ZV	V

Note Since subscripts C and E may be abbreviated, and since subscripts B and D may contain an indeterminate number of letters, it is necessary to put the restriction on the subscripts B and D that they should not end with H, L, V, X, or Z, so as to avoid possible confusion

6. SUBSCRIPT F (For Additional Information)

If necessary, subscript F is used to represent any additional qualification of the parameter such as mode of operation, test conditions, etc. The letter symbols for subscript F are given below.
Subscript F should be in upper-case.

Modes of operation	Subscript
Power-down	PD
Page-mode read	PGR
Page-mode write	PGW
Read	R
Refresh	RF
Read-modify-write	RMW
Read-write	RW
Write	W

FOR DIGITAL INTEGRATED CIRCUITS

New symbol	Former symbol	Parameter—definition
C_I		Input capacitance
C_O		Output capacitance
$C_{I/O}$		Input/output terminal capacitance
$C_{I(\phi)}$		Input capacitance of clock input
f		Frequency
$f_{(\phi)}$		Clock frequency
I		Current—the current into an integrated circuit terminal is defined as a positive value and the current out of a terminal is defined as a negative value
I_{BB}		Supply current from V_{BB}
$I_{BB(AV)}$		Average supply current from V_{BB}
I_{CC}		Supply current from Vcc
$I_{CC(AV)}$		Avarage supply current from Vcc
$I_{CC(PD)}$		Power down supply current from Vcc
I_{DD}		Supply current from V_{DD}
$I_{DD(AV)}$		Average supply current from V_{DD}
I_{GG}		Supply current from V_{GG}
$I_{GG(AV)}$		Average supply current from V_{GG}
I_I		Input current
I_{IH}		High-level input current—the value of the input current when V_{OH} is applied to the input considered
I_{IL}		Low level input current—the value of the input current when V_{OL} is applied to the input considered
I_{LOAD}		Built-in resistor current
I_{PEAK}		Peak current
I_{OH}		High-level output current—the value of the output current when V_{OH} is applied to the output considered
I_{OL}		Low-level output current—the value of the output current when V_{OL} is applied to the output considered
I_{OZ}		Off-state (high-impedance state) output current—the current into an output having a three-state capability with input condition so applied that it will establish according to the product specification, the off (high-impedance) state at the output
I_{OZH}		Off-state (high-impedance state) output current, with high-level voltage applied to the output
I_{OZL}		Off-state (high-impedance state) output current, with low-level voltage applied to the output
I_{OS}		Short-circuit output current
I_{SS}		Supply current from V_{SS}
Pd		Power dissipation
N_{EW}		Number of erase/write cycles
N_{RA}		Number of read access unrefreshed
R_I		Input resistance
R_L		External load resistance
R_{OFF}		Off-state output resistance
R_{ON}		On-state output resistance
t_a		Access time—the time interval between the application of a specified input pulse during a read cycle and the availability of valid data signal at an output
$t_{a(A)}$	$t_{a(AD)}$	Address access time—the time interval between the application of an address input pulse and the availability of valid data signals at an output
$t_{a(CAS)}$		Column address strobe access time
$t_{a(E)}$	$t_{a(CE)}$	Chip enable access time
$t_{a(G)}$	$t_{a(OE)}$	Output enable access time
$t_{a(PR)}$		Data access time after program
$t_{a(RAS)}$		Row address strobe access time
$t_{a(S)}$	$t_{a(CS)}$	Chip select access time
t_C		Cycle time
t_{CR}	$t_{C(RD)}$	Read cycle time—the time interval between the start of a read cylce and the start of the next cycle
t_{CRF}	$t_{C(REF)}$	Refresh cycle time—the time interval between successive signals that are intended to restore the level in a dynamic memory cell to its original level
t_{CPG}	$t_{C(PG)}$	Page-mode cycle time

New symbol	Former symbol	Parameter—definition
t_{CRMW}	$t_{C(RMR)}$	Read-modify-write cycle time—the time interval between the start of a cycle in which the memory is read and new data is entered, and the start of the next cycle
t_{CW}	$t_{C(WR)}$	Write cycle time—the time interval between the start of a write cycle and the start of the next cycle
t_{d}		Delay time—the time between the specified reference points on two pulses
$t_{d(\phi)}$		Delay time between clock pulses—e g , symbology, delay time, clock 1 to clock 2 or clock 2 to clock 1
$t_{d(CAS\text{-}RAS)}$		Delay time, column address strobe to row address strobe
$t_{d(CAS\text{-}W)}$	$t_{d(CAS\ WR)}$	Delay time, column address strobe to write
$t_{d(RAS\text{-}CAS)}$		Delay time, row address strobe to column address strobe
$t_{d(RAS\text{-}W)}$	$t_{d(RAS\text{-}WR)}$	Delay time, row address strobe to write
$t_{dis(R\text{-}Q)}$	$t_{dis(R\text{-}DA)}$	Output disable time after read
$t_{dis(S)}$	$t_{PXZ(CS)}$	Output disable time after chip select
$t_{dis(W)}$	$t_{PXZ(WR)}$	Output disable time after write
t_{DHL}		High-level to low-level delay time } the time interval between specified reference points on the input and on the output pulses, when the output is going to the low (high) level and when the device is driven with a specified loading networks
t_{DLH}		Low-level to high-level delay time
$t_{en(A\text{-}Q)}$	$t_{PZV(A\text{-}DQ)}$	Output enable time after address
$t_{en(R\text{-}Q)}$	$t_{PZV(R\text{-}DQ)}$	Output enable time after read
$t_{en(S\text{-}Q)}$	$t_{PZX(CS\text{-}DQ)}$	Output enable time after chip select
t_{f}		Fall time
t_{h}		Hold time—the interval of time during which a signal at a specified input terminal appears after an active transition occurs at another specified input terminal
$t_{h(A)}$	$t_{h(AD)}$	Address hold time
$t_{h(A\text{-}E)}$	$t_{h(AD\text{-}CE)}$	Chip enable hold time after address
$t_{h(A\text{-}PR)}$	$t_{h(AD\text{-}PRO)}$	Program hold time after address
$t_{h(CAS\text{-}CA)}$		Column address hold time after column address strobe
$t_{h(CAS\text{-}D)}$	$t_{h(CAS\text{-}DA)}$	Data-in hold time after column address strobe
$t_{h(CAS\text{-}Q)}$	$t_{h(CAS\text{-}OUT)}$	Data-out hold time after column address strobe
$t_{h(CAS\text{-}RAS)}$		Row address strobe hold time after column address strobe
$t_{h(CAS\text{-}W)}$	$t_{h(CAS\text{-}WR)}$	Write hold time after column address strobe
$t_{h(D)}$	$t_{h(DA)}$	Data-in hold time
$t_{h(D\text{-}PR)}$	$t_{h(DA\text{-}PRO)}$	Program hold time after data-in
$t_{h(E)}$	$t_{h(CE)}$	Chip enable hold time
$t_{h(E\text{-}D)}$	$t_{h(CE\text{-}DA)}$	Data-in hold time after chip enable
$t_{h(E\text{-}G)}$	$t_{h(CE\text{-}OE)}$	Output enable hold time after chip enable
$t_{h(R)}$	$t_{h(RD)}$	Read hold time
$t_{h(RAS\text{-}CA)}$		Column address hold time after row address strobe
$t_{h(RAS\text{-}CAS)}$		Column address strobe hold time after row address strobe
$t_{h(RAS\text{-}D)}$	$t_{h(RAS\text{-}DA)}$	Data-in hold time after row address strobe
$t_{h(RAS\text{-}W)}$	$t_{h(RAS\text{-}WR)}$	Write hold time after row address strobe
$t_{h(S)}$	$t_{h(CS)}$	Chip select hold time
$t_{h(W)}$	$t_{h(WR)}$	Write hold time
$t_{h(W\text{-}CAS)}$	$t_{h(WR\text{-}CAS)}$	Column address strobe hold time after write
$t_{h(W\text{-}D)}$	$t_{h(WR\text{-}DA)}$	Data-in hold time after write
$t_{h(W\text{-}RAS)}$	$t_{h(WR\text{-}RAS)}$	Row address hold time after write
t_{PHL}		High-level to low-level propagation time } the time interval between specified reference points on the input and on the output pulses when the output is going to the low (high) level and when the device is driven and loaded by typical devices of stated type
t_{PLH}		Low-level to high-level propagation time
t_{r}		Rise time
$t_{rec(W)}$	t_{wr}	Write recovery time—the time interval between the termination of a write pulse and the initiation of a new cycle
$t_{rec(PD)}$	$t_{R(PD)}$	Power-down recovery time
t_{su}		Setup time—the time interval between the application of a signal which is maintained at a specifed input terminal and a consecutive active tarnsition at another specified input terminal
$t_{su(A)}$	$t_{su(AD)}$	Address setup time

New symbol	Former symbol	Parameter—definition
$t_{su(A-E)}$	$t_{su(AD-CE)}$	Chip enable setup time before address
$t_{su(A-W)}$	$t_{su(AD-WR)}$	Write setup time before address
$t_{su(CA-RAS)}$		Row address strobe setup time before column address
$t_{su(D)}$	$t_{su(DA)}$	Data-in setup time
$t_{su(D-E)}$	$t_{su(DA-CE)}$	Chip enable setup time before data-in
$t_{su(D-W)}$	$t_{su(DA-WR)}$	Write setup time before data in
$t_{su(E)}$	$t_{su(CE)}$	Chip enable setup time
$t_{su(E-P)}$	$t_{su(CE-P)}$	Precharge setup time before chip enable
$t_{su(G-E)}$	$t_{su(OE-CE)}$	Chip enable setup time before output enable
$t_{su(P-E)}$	$t_{su(P-CE)}$	Chip enable setup time before precharge
$t_{su(PD)}$		Power-down setup time
$t_{su(R)}$	$t_{su(RD)}$	Read setup time
$t_{su(R-CAS)}$	$t_{su(RA-CAS)}$	Column address strobe setup time before read
$t_{su(RA-CAS)}$		Column address strobe setup time before row address
$t_{su(S)}$	$t_{su(CS)}$	Chip select setup time
$t_{su(S-W)}$	$t_{su(CS-WR)}$	Write setup time before chip select
$t_{su(W)}$	$t_{su(WR)}$	Write setup time
t_{THL}		High-level to low-level transition time } the time interval between specified reference points on the edge of the output pulse when the output is going to the low (high) level and when a specified input signal is applied through a specified network and the output is loaded by another specified network
t_{TLH}		Low-level- to high-level transition time
$t_{v(A)}$	$t_{dv(AD)}$	Data valid time after address
$t_{v(E)}$	$t_{dv(CE)}$	Data valid time after chip enable
$t_{v(E)PR}$	$t_{v(CE)PR}$	Data valid time after chip enable in program mode
$t_{v(G)}$	$t_{v(OE)}$	Data valid time after output enable
$t_{v(PR)}$		Data valid time after program
$t_{v(S)}$	$t_{v(CS)}$	Data valid time after chip select
t_w		Pulse width (pulse duration) the time interval between specified reference points on the leading and training edges of the waveforms
$t_{w(E)}$	$t_{w(CE)}$	Chip enable pulse width
$t_{w(EH)}$	$t_{w(CEH)}$	Chip enable high pulse width
$t_{w(EL)}$	$t_{w(EL)}$	Chip enable low pulse width
$t_{w(PR)}$		Program pulse width
$t_{w(R)}$	$t_{w(RD)}$	Read pulse width
$t_{w(S)}$	$t_{w(CS)}$	Chip select pulse width
$t_{w(W)}$	$t_{w(WR)}$	Wrtie pulse width
$t_{w(\phi)}$		Clock pulse width
Ta		Ambient temperature
Topr		Operating temperature
Tstg		Storage temperature
V_{BB}		V_{BB} supply voltage
V_{CC}		V_{CC} supply voltage
V_{DD}		V_{DD} supply voltage
V_{GG}		V_{GG} supply voltage
V_I		Input voltage
V_{IH}		High-level input voltage—the value of the permitted high-state voltage at the input
V_{IL}		Low-level input voltage—the value of the permitted low-state voltage at the input
V_O		Output voltage
V_{OH}		High-level output voltage—the value of the guaranteed high-state voltage range at the output
V_{OL}		Low-level output voltage—the value of the guaranteed low-state voltage range at the output
V_{SS}		V_{SS} supply voltage

Note 1. These letter symbols are based on the IEC publication 148 except a part of them

QUALITY ASSURANCE AND RELIABILITY TESTING

1 INTRODUCTION

IC & LSI have made rapid technical progress in electrical performances of high integration, high speed, and sophisticated functionality. And now they have got boundless wider applications in electronic systems and electrical appliances.

To meet the above trend of expanding utilization of IC & LSI, Mitsubishi considers that it is extremely important to supply stable quality and high reliable products to customers.

Mitsubishi Electric places great emphasis on quality as a basic policy "Quality First", and has striven always to improve quality and reliability.

Mitsubishi has already developed the Quality Assurance System covering design, manufacturing, inventory and delivery for IC & LSI, and has supplied highly reliable products to customers for many years. The following articles describe the Quality Assurance System and examples of reliability control for Mitsubishi Single-chip 8-bit Microcomputer.

2. QUALITY ASSURANCE SYSTEM

The Quality Assurance System places emphasis on built-in reliability in designing and built-in quality in manufacturing. The System from development to delivery is summarized in Fig. 1.

2.1 Quality Assurance in Designing

The following steps are applied in the designing stage for a new product.

(1) Setting of perfomance, quality and reliability target for new product.
(2) Discussion of performance and quality for circuit design, device structure, process, material and package.
(3) Verification of design by CAD system to meet standardized design rule.
(4) Functional evaluation for bread-board device to confirm electrical performance.
(5) Reliability evaluation for TEG (Test Element Group) chip to detect basic failure mode and investigate failure mechanism.
(6) Reliability test (In-house qualification) for new product to confirm quality and reliability target.
(7) Decision of pre-production from the standpoint of performance, reliability, production flow/conditions, production capability, delivery and etc.

2.2 Quality Assurance in Manufacturing

Quality assurance in manufacturing is performed as follows.

(1) Environment control such as temperature, humidity and dust as well as deionized water and utility gases.
(2) Maintenance and calibration control for automatized manufacturing equipments, automatic testing equipments, and measuring instruments.
(3) Material control such as silicon wafer, lead frame, packaging material, mask and chemicals.
(4) In-process inspections in wafer-fabrication, assembly and testing.
(5) 100% final inspection of electrical characteristics, visual inspection and burn-in, if necessary.
(6) Quality assurance test
 -Electrical characteristics and visual inspection, lot by lot sampling
 -Environment and endurance test, periodical sampling.
(7) Inventory and shipping control, such as storage environment, date code identification, handling and ESD (Electro Static Discharge) preventive procedure.

2.3 Reliability Test

To verify the reliability of a product as described in the Mitsubishi Quality Assurance System, reliability tests are performed at three different stages in new product development, pre-production and mass-production.

At the development of a new product the reliability test plan is fixed corresponding to the quality and reliability target of each product, respectively. The test plan includes in-house qualification test and TEG evaluation, if necessary. TEG chips are designed and prepared for new device structure, new process and new material.

After the proto-type product has passed the in-house qualification test, the product advances to the pre-production. In the pre-production stage, the specific reliability tests are programmed and performed again to verify the quality of pre-production product.

In the mass production, the reliability tests are performed periodically to confirm the quality of the mass production product according to the quality assurance test program.

Table 1 shows an example of reliability test program for plastic encapsulated IC & LSI.

Table 1. TYPICAL RELIABILITY TEST PROGRAM FOR PLASTIC ENCAPSULATED IC & LSI

Group	Test	Test condition
1	Solderability	230℃, 5sec. Rosin flux
2	Soldering heat	260℃, 10sec
	Thermal shock	−55℃, 125℃, 15cycles
	Temperature cycling	−65℃, 150℃, 100cycles
3	Lead fatigue	250gr, 90°, 2arcs
4	Shock	1500G, 0. 5msec.
	Vibration	20G, 100∼2000Hz X, Y, Z direction 4min./cycle, 4cycles/direction
	Constant acceleration	20000G, Y direction, 1min.
5	Operation life	T_a=125℃, Vccmax 1000hours
6	High temperature storage life	T_a=150℃, 1000hours
7	High temperature and high humidity	85℃, 85%, 1000hours
	Pressure cooker	121℃, 100%, 100hours

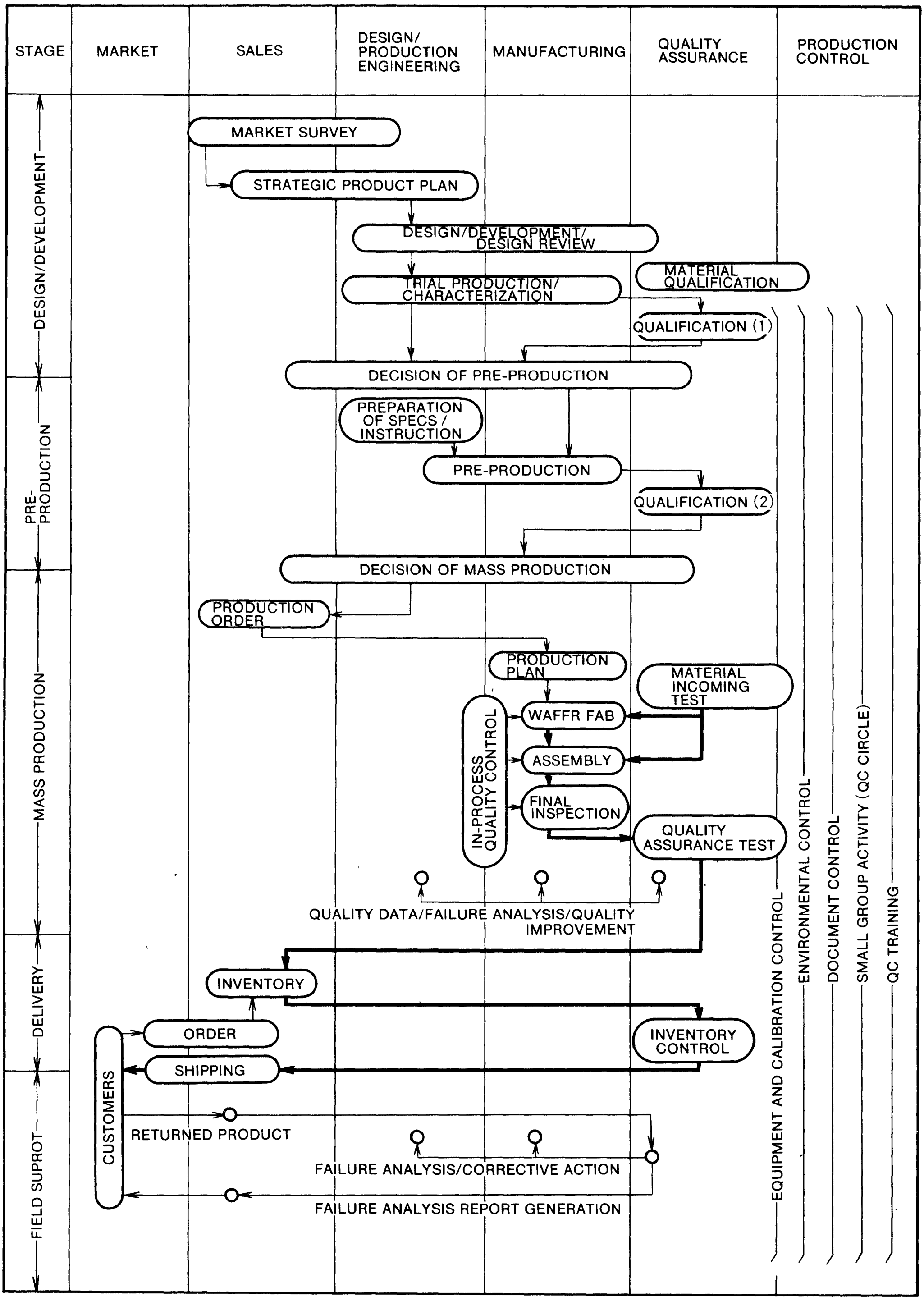


Fig.1 FLOW CHART OF QUALITY ASSURANCE SYSTEM

2.4 Returned Product Control

When failure analysis is requested by a customer, the failed devices are returned to Mitsubishi Electric via the sales office of Mitsubishi using the form of "Analysis Request of Returned Product"

Mitsubishi provides various failure analysis equipments to analyze the returned product. A failure analysis report is generated to the customer upon completion of the analysis. The failure analysis result enforces taking corrective action for the design, fabrication, assembly or testing of the product to improve reliability and realize lower failure rate.

Fig. 2 shows the procedure of returned product control from customer.

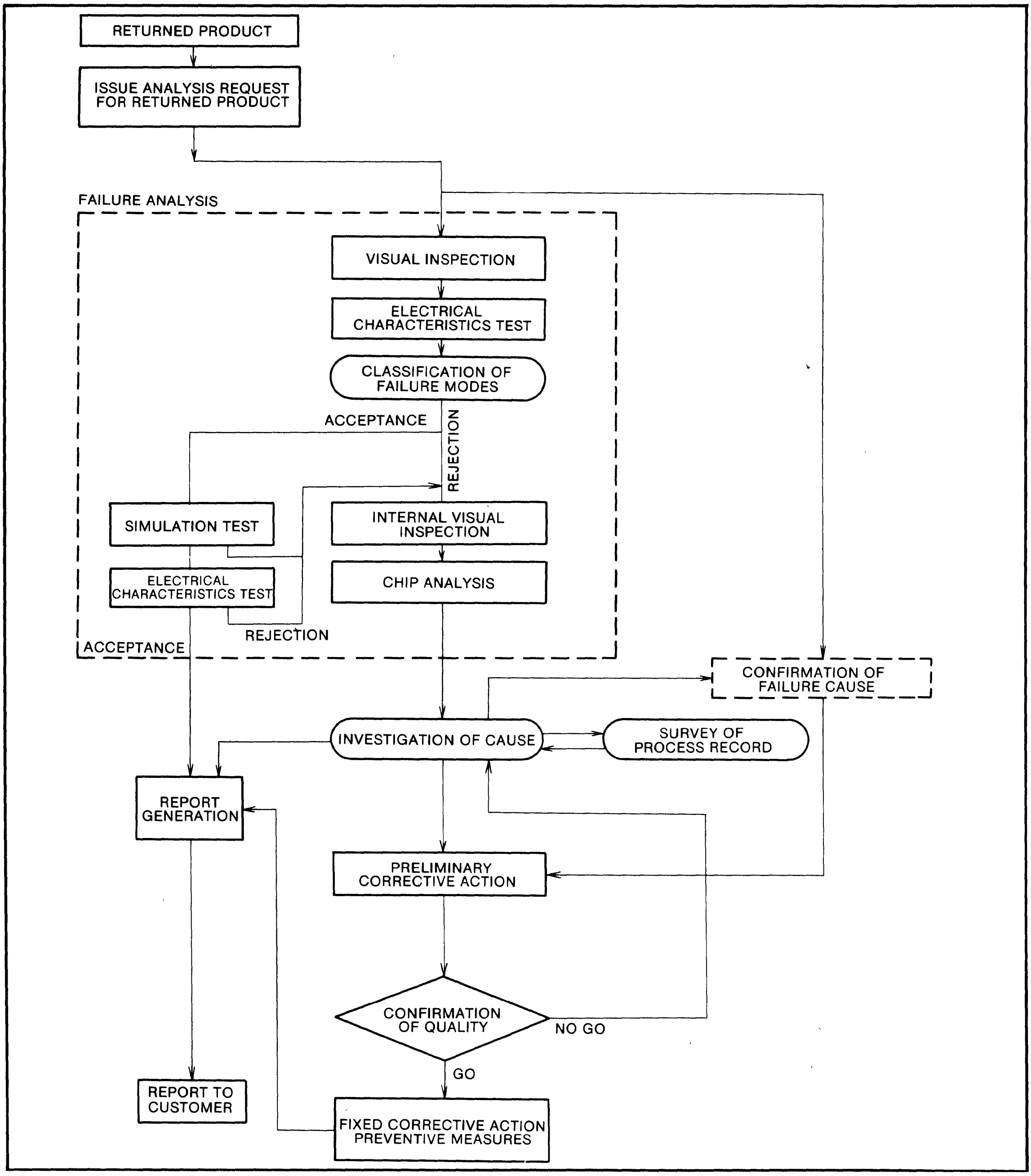


Fig.2 PROCEDURE OF RETURNED PRODUCT CONTROL

3 RELIABILITY TEST RESULTS

The reliability test results for Mitsubishi Single-chip 8-bit Microcomputers are shown in Table 2, Table 3 and Table 4. Table 2 shows the result of endurance tests of high temparature operation life and high temperature storage life test for representative types of Single-chip 8-bit Microcomputers.

Table 2. ENDURANCE TEST RESULTS

Test	Series	Type Number	Test Condition	Number of Samples	Device Hours (Hours)	Number of Failures
High Temperature Operation Life	38000 Series	M38002M2-XXXFP	125℃ 7 V	22	22000	0
		M38063M6-XXXFP		22	22000	0
		M38102M5-XXXSP		22	22000	0
		M38112M4-XXXSP		22	22000	0
		M38173M6-XXXFP		22	22000	0
		M38002E4-XXXFP		22	22000	0
		M38063E6-XXXFP		22	22000	0
		M38173E6-XXXFP		22	22000	0
	37450 Series	M37450M8-XXXFP		22	22000	0
		M37451M4-XXXSP		22	22000	0
		M37450M4TXXXSP		22	22000	0
		M37451M4DXXXSP		22	22000	0
		M37450E4-XXXSP		22	22000	0
		M37451E8-XXXSP		22	22000	0
		M37451E8DXXXSP		22	22000	0
	37470 Series	M37470M2-XXXSP		22	22000	0
		M37470M8-XXXSP		22	22000	0
		M37471M8-XXXSP		22	22000	0
		M37470E8-XXXSP		22	22000	0
		M37471E4-XXXSP		22	22000	0
		M37471E8-XXXSP		22	22000	0
High Temperature Storage Life	38000 Series	M38002M2-XXXFP	175℃	22	22000	0
		M38063M6-XXXFP		22	22000	0
		M38102M5-XXXSP		22	22000	0
		M38112M4-XXXSP		22	22000	0
		M38173M6-XXXFP		22	22000	0
		M38002E4-XXXFP		22	22000	0
		M38063E6-XXXFP		22	22000	0
		M38173E6-XXXFP		22	22000	0
	37450 Series	M37450M8-XXXFP		22	22000	0
		M37451M4-XXXSP		22	22000	0
		M37450E4-XXXSP		22	22000	0
		M37451E8-XXXSP		22	22000	0
	37470 Series	M37470M8-XXXSP		22	22000	0
		M37471M8-XXXFP		22	22000	0
		M37470E4-XXXSP		22	22000	0
		M37471E8-XXXSP		22	22000	0
Low Temperature Storage Life	38000 Series	M38063M6DXXXFP	−55℃ 5.5V	22	22000	0
		M38063E6DXXXFP		22	22000	0
	37450 Series	M37450M4TXXXSP		22	22000	0
		M37451E8DXXXSP		22	22000	0

Table 3 shows the results of the environment tests of thermal stress high temperature/high humidity and pressure cooker test for the same type of products in regards to endurance tests.

Table 4 shows the results of mechanical tests for representative products of various package types.

Table 3. ENVIRONMENTAL TEST RESULTS

Test	Series	Type Number	Test Condition	Number of Samples	Device Hours (Hours)	Number of Failures
High Temperature High Humidity Life	38000 Series	M38002M2-XXXFP	85℃ 85%RH 5.5V	22	22000	0
		M38063M6-XXXFP		22	22000	0
		M38102M5-XXXSP		22	22000	0
		M38112M4-XXXSP		22	22000	0
		M38173M6-XXXFP		22	22000	0
		M38002E4-XXXFP		22	22000	0
		M38063E6-XXXFP		22	22000	0
		M38102E5-XXXFP		22	22000	0
		M38173E6-XXXFP		22	22000	0
	37450 Series	M37450M8-XXXFP		22	22000	0
		M37451M4-XXXSP		22	22000	0
		M37450E4-XXXSP		22	22000	0
		M37451E8-XXXSP		22	22000	0
	37470 Series	M37470M8-XXXSP		22	22000	0
		M37471M8-XXXFP		22	22000	0
		M37470E4-XXXFP		22	22000	0
		M37471E8-XXXSP		22	22000	0

Test	Series	Type Number	Test Condition	96Hours	240Hours	500Hours
Pressure Cooker	38000 Series	M38002M2-XXXFP	121℃ 100%RH	0/22	0/22	—
		M38063M6-XXXFP		0/22	0/22	—
		M38102M5-XXXSP		0/22	0/22	—
		M38112M4-XXXSP		0/22	0/22	—
		M38173M6-XXXFP		0/22	0/22	—
		M38002E4-XXXFP		0/22	0/22	—
		M38063E6-XXXFP		0/22	0/22	—
		M38173E6-XXXFP		0/22	0/22	—
	37450 Series	M37450M8-XXXFP		0/22	0/22	—
		M37451M4-XXXSP		0/22	0/22	—
		M37450E4-XXXSP		0/22	0/22	—
		M37451E8-XXXSP		0/22	0/22	—
	37470 Series	M37470M8-XXXSP		0/22	0/22	—
		M37471M8-XXXSP		0/22	0/22	—
		M37470E4-XXXSP		0/22	0/22	—
		M37471E8-XXXSP		0/22	0/22	—

Test	Series	Type Number	Test Condition	10Cycles	100Cycles	300Cycles
Temperature Cycling	38000 Series	M38002M2-XXXFP	−65℃～150℃	0/22	0/22	0/22
		M38063M6-XXXFP		0/22	0/22	0/22
		M38102M5-XXXSP		0/22	0/22	0/22
		M38112M4-XXXSP		0/22	0/22	0/22
		M38173M6-XXXFP		0/22	0/22	0/22
		M38002E4-XXXFP		0/22	0/22	0/22
		M38063E6-XXXFP		0/22	0/22	0/22
		M38173E6-XXXFP		0/22	0/22	0/22
	37450 Series	M37450M8-XXXFP		0/22	0/22	0/22
		M37451M4-XXXSP		0/22	0/22	0/22
		M37450E4-XXXSP		0/22	0/22	0/22
		M37451E8-XXXSP		0/22	0/22	0/22
	37470 Series	M37470M8-XXXSP		0/22	0/22	0/22
		M37471M8-XXXFP		0/22	0/22	0/22
		M37470E4-XXXSP		0/22	0/22	0/22
		M37471E8-XXXSP		0/22	0/22	0/22

Table 4. MECHANICAL TEST RESULTS

Test	Test Condition	Package						
		32P4B	42P4B	64P4B	64P6N	80P6N	80P6	80P6S
Soldering Heat	260℃ 10sec	0/110	0/110	0/110	0/110	0/110	0/110	0/110
Thermal Shock	−40℃～125℃ 15cycle	0/110	0/110	0/110	0/110	0/110	0/110	0/110
Solderebility	230℃ 5sec Using a rosin-type Flux	0/110	0/110	0/110	0/110	0/110	0/110	0/110
Shock	1500G 0.5msec X, Y, and Z directions 3times	0/110	0/110	0/110	0/110	0/110	0/110	0/110
Vibration	20G X, Y, and Z directions 4times 100～2000Hz 4minutes/Cycle	0/110	0/110	0/110	0/110	0/110	0/110	0/110
Constant Acceleration	20000G Y_1 direction 1minute	0/110	0/110	0/110	0/110	0/110	0/110	0/110
Free Fall	75cm onto a maple wood board 3times	0/110	0/110	0/110	0/110	0/110	0/110	0/110
Lead Integrity	250g 90° Berding 2times (QFP, 125g)	0/110	0/110	0/110	0/110	0/110	0/110	0/110
	500g Tension 30sec (QFP, 250g)	0/110	0/110	0/110	0/110	0/110	0/110	0/110

4 FAILURE ANALYSIS

Accelerated reliability tests are applied to observe failures casued by temperature, voltage, humidity, current, mechanical stress and those combined stresses on chips and packages.

Examples of typical failure modes are shown below.

(1) Wire Bonding Failure by Thermal Stress

Fig. 3, Fig. 4 and Fig. 5 are example of a failure occurred by temperature storage test of 225℃, 1000hours.

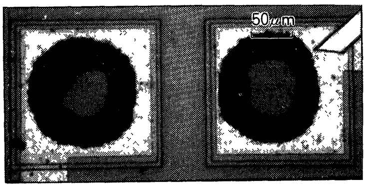


Fig.3
Micrograph of lifted Au ball trace on Al bonding pad

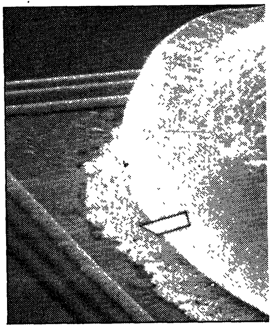


Fig.4
Au-Al plague formation on bonding pad

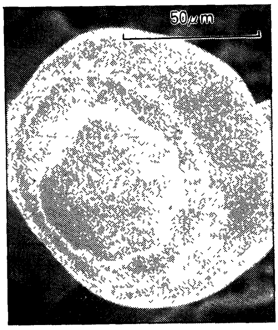


Fig.5
Lifted Au wire ball base

Au-Al intermetallic formation so-called "Purple plague" by thermal overstress makes Au wire lift off from aluminum metallization. The activation energy of this failure mode is estimated approximately 1.0eV and no failure has been observed so far in practical uses.

(2) Aluminum Corrosion Failure by Temperature/Humidity Stress.

Fig. 6, Fig 7 and Fig. 8 are an example of corroded failure of aluminum metallization in plastic encapsulated IC after accelerated temperature/humidity storage test (pressure cooker test) of 121℃, 100%RH, 1000hours duration.

Aluminum bonding pad is dissolved by penetrated water from plastic package, and chlorine concentration is observed on corroded aluminum bonding pad as shown in Fig. 8.

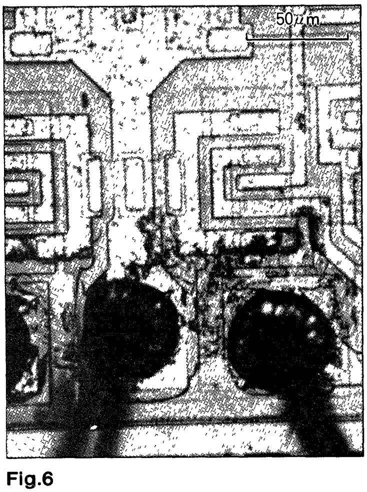


Fig.6
Micrograph of corroded Aluminum metallization

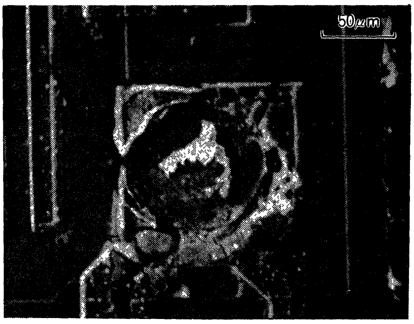


Fig.7 Enlarged micrograph of corroded Aluminum bonding pad

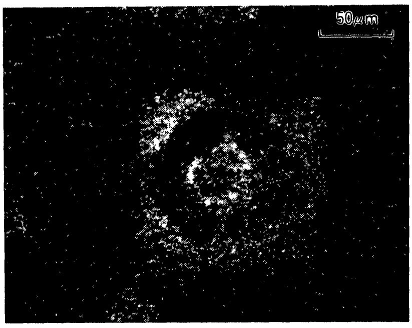


Fig.8 Cl distribution on corroded Aluminum bonding pad

(3) Destructive Failure by Electrical Overstress

ESD have been performed to reproduce the electrical overstress failure in field uses.

Fig. 9 and Fig. 10 are an example of failure observed by surge voltage test. The trace of destruction is verified as the aluminum bridge by X-ray micro analysis.

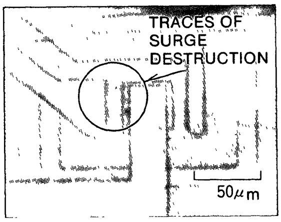


Fig.9 Micrograph of surge voltage destruction

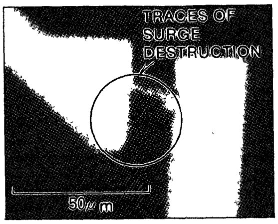


Fig.10 Aluminum trace of destructive spot

(4) Aluminum Electromigration

Fig. 11 shows an open circuit of aluminum metallization in high current density region caused by accelerated operating life test. This failure is caused by the aluminum electromigration. Voids and hillock have been formed in aluminum metallization by high current density.

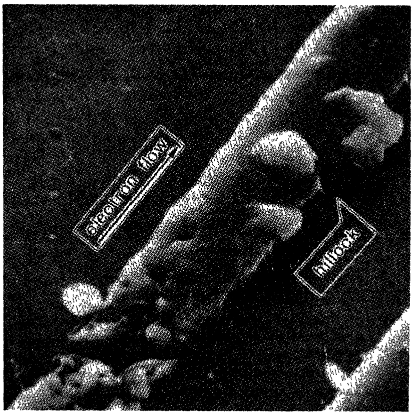


Fig.11 Voids and hillocks formation by Aluminum electromigration

5 SUMMARY

The Mitsubishi quality assurance system and examples of reliability control have been discussed. Customer's interest and requirement for high reliable IC & LSI are increasing significantly. To satisfy customer's expectancy. Mitsubishi as an IC vendor, would like to make perpetual efforts in the following areas.

(1) Emphasis on built-in reliability at design stage and reliability evaluation to investigate latent failure modes and acceleration factors.

(2) Execution of periodical endurance, environment and mechanical test to verify reliability target and realize higher reliability.

(3) Focus on development of advanced failure analysis techniques. Detail failure analysis, intensive corrective action and quick response to customer's analysis request.

(4) Collection of customer's quality data in qualification, incoming inspection, production and field use to improve PPM, fraction defective and FIT, failure rate.

Mitsubishi would highly appreciate if the customer would provide quality and reliability data of incoming inspection or field failure rate essential to verify and improve the quality/reliability of IC & LSI.

PRECAUTIONS IN HANDLING MOS IC/LSIs

A MOS transistor has a very thin oxide insulator under the gate electrode on the silicon substrate. It is operated by altering the conductance (g_m) between source and drain to control mobile charges in the channel formed by the applied gate voltage.

If a high voltage were applied to a gate terminal, the insulator-film under the gate electrode could be destroyed, and all Mitsubishi MOS IC/LSIs contain internal protection circuits at each input terminal to prevent this. It is inherently necessary to apply reverse bias to the P-N junctions of a MOS IC/LSI.

Under certain conditions, however, it may be impossible to completely avoid destruction of the thin insulator-film due to the application of unexpectedly high voltage or thermal destruction due to excessive current from a forward biased P-N junction. Therefore the following recommendations should be followed in handling MOS devices.

1. KEEPING VOLTAGE AND CURRENT TO EACH TERMINAL BELOW MAXIMUM RATINGS

1. The recommended ranges of operating conditions provide adequate safety margins. Operating within these limits'will assure maximum equipment performance and quality.
2. Forward bias should not be applied to any terminal since excessive current may cause thermal destruction.
3. Output terminals should not be connected directly to the power supply. Short-circuiting of a terminal to a power supply having low impedance may cause burn-out of the internal leads or thermal destruction due to excessive current.

2. KEEPING ALL TERMINALS AT THE SAME POTENTIAL DURING TRANSPORT AND STORAGE

When MOS IC/LSIs are not in use, both input and output terminals can be in a very high impedance state so that they are easily subjected to electrostatic induction from AC fields of the surrounding space or from charged objects in their vicinity. For this reason, MOS IC/LSIs should be protected from electrostatic charges while being transported and stored by conductive rubber foam, aluminum foil, shielded boxes or other protective precautions.

3. KEEPING ELECTRICAL EQUIPMENT, WORK TABLES AND OPERATING PERSONNEL AT THE SAME POTENTIAL

1. All electric equipment, work table surfaces and operating personnel should be grounded. Work tables should be covered with copper or aluminum plates of good conductivity, and grounded. One method of grounding personnel, after making sure that there is no potential difference with electrical equipment, is by the use of a wristwatch metallic ring, etc. attached around the wrist and grounded in series with a 1mΩ resistor. Be sure that the grounding meets national regulations on personnel safety.
2. Current leakage from electric equipment must be prevented not only for personnel safety, but also to avert the destruction of MOS IC/LSIs, as described above. Items such as testers, curve-tracers and synchroscopes must be checked for current leakage before being grounded.

4. PRECAUTIONS FOR MOUNTING OF MOS IC/LSIs

1. The printed wiring lines between input and output terminals of MOS IC/LSIs should not be close to or parallel to high-voltage or high-power signal lines. Turning power on while the device is short-circuited, either by a solder bridge made during assembly or by a probe during adjusting and testing, may cause maximum ratings to be exceeded, which can result in the destruction of the device.
2. When input/output, or input and/or output, terminals of MOS IC/LSIs (now open-circuits) are connected, we must consider the possibility of current leakage and take precautions similar to §2 above. To reduce such undesirable trouble, it is recommended that an interface circuit be inserted at the input or output terminal, or a resistor with a resistance that does not exceed the output driving capability of the MOS IC/LSI be inserted between the power supply and the ground.
3. A filter circuit should be inserted in the AC power supply line to absorb surges which can frequently be strong enough to destroy a MOS IC/LSI.
4. Terminal connections should be made as described in the catalog while being careful to meet specifications.
5. Ungrounded metal plates should not be placed near input or output terminals of any MOS IC/LSIs, since destruction of the insulation may result if they become electrostatically charged.
6. Equipment cases should provide shielding from electrostatic charges for more reliable operation. When a plastic case is used, it is desirable to coat the inside of the case with conductive paint and to ground it. This is considered necessary even for battery-operated equipment.

SERIES 38000

Series 38000 Index by Function

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

■Typical type

Group name	Clock oscillation frequency (MHz)	Shortest instruction execution time (μs)	I/O port (number)	Timer (bit×number)	Function					Interrupt cause		Package
					Serial I/O		A-D converter (bit×channel)	D-A converter (bit×channel)	8-bit PWM			
			I/O		UART/Clock-synchronized	Clock-synchronized (bit×number)				External	Internal	
M3800x	8	0.5	58	8×4	1	—	—	—	—	8	6	64P4B/64P6N
M3806x	8	0.5	72	8×4	1	8×1	8×8	8×2	—	7	8	80P6N/80P6S

■Internal high-breakdown-voltage port type

Group name	Clock oscillation frequency (MHz)	Shortest instruction execution time (μs)	I/O port (number)			Timer (bit×number)	Function											Interrupt cause		Package
							Serial I/O		A-D converter (bit×channel)	Comparator (bit×channel)	PWM		Sub clock	High-breakdown-voltage port (number)		FLP controller				
			Input	Output	I/O		Clock-synchronized (bit×number)	With an automatic data transfer function (bit×number)			8-bit	14-bit		Output	I/O	Segment	Digit	External	Internal	
M3810x	4.2	0.95	1	28	28	8×4	8×2	—	—	4×1	—	1	○	28	—	—	—	4	6	64P4B/ 64P6N
M3811x	4.2	0.95	1	28	28	8×4	8×1	8×1	—	4×1	—	1	○	28	—	8~16	8~16	4	9	64P4B/ 64P6N
M3817x	6.3	0.63	1	24	45	8×6	8×1	8×1	8×8	—	1	1	○	24	8	8~24	4~16	5	12	80P6N
M3818x	6.3	0.63	3	20	67	8×6	8×1	8×1	8×8	—	1	1	○	20	12	8~24	4~16	5	12	100P6S

MITSUBISHI MICROCOMPUTERS

M3800x Group

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

DESCRIPTION

The M3800x group is made up of 8-bit microcomputers based on the MELPS 740 core.

The M3800x group is designed for office automation equipment, household appliances and include four timers, serial I/O function.

The various microcomputers in the M3800x group include variations of internal memory size and packaging. For details, see the section on part numbering.

For details on availability of microcomputers in the M3800x group, see the section on group expansion.

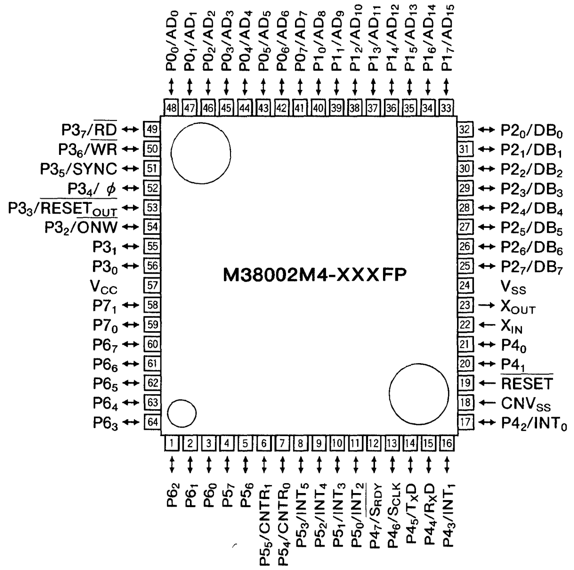
FEATURES

- Basic machine-language instructions ······················ 71
- Instruction execution time ································ 0.5μs
  (shortest instruction at 8MHz oscillation frequency)
- Memory size
  ROM ·· 4K to 32K bytes
  RAM ·· 192 to 1024 bytes
- Programmable input/output ports ·························· 58
- Interrupts ································ 15 sources, 15 vectors
- Timers ·· 8 bit×4
- Serial I/O ········· 8-bit×1(UART or Clock-synchronized)
- Clock generation circuit ······ Internal feedback amplifier
  (connect to external ceramic resonator or quartz crystal)
- Supply voltage ·· 3.0 to 5.5V
- Low power dissipation ································ 32mW
- Memory expansion possible
- Operating temperature range ················· −20 to 85℃

APPLICATIONS

Office automation, factory automation, household appliances, and other consumer applications, etc.

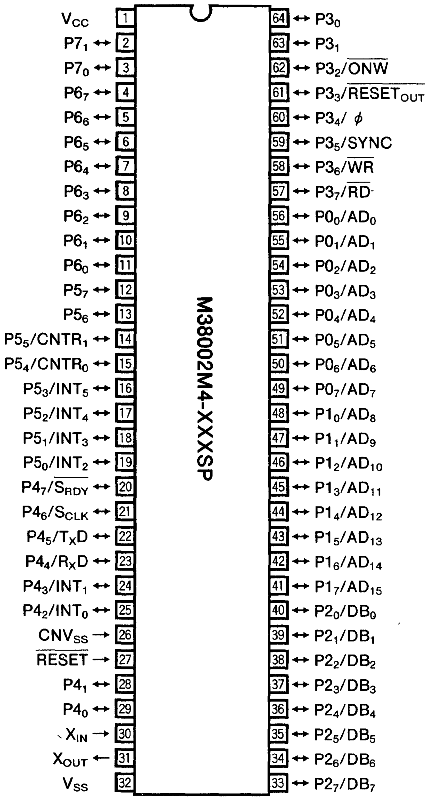
PIN CONFIGURATION (TOP VIEW)



Package type : 64P6N

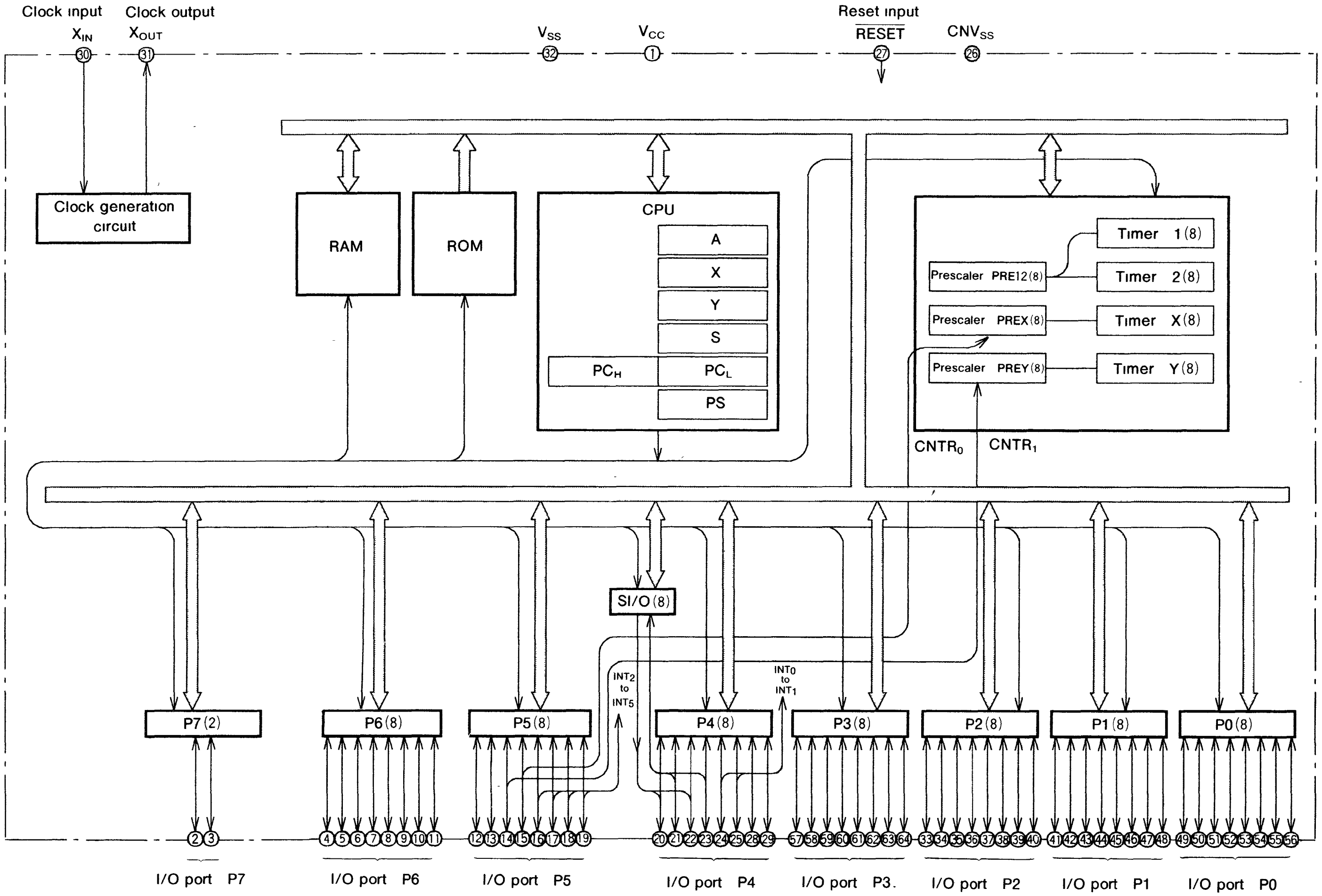
64-pin plastic-molded QFP

PIN CONFIGURATION (TOP VIEW)



Package type : 64P4B
64-pin shrink plastic-molded DIP

FUNCTIONAL BLOCK DIAGRAM (Package : 64P4B)



PIN DESCRIPTION

Pin	Name	Function	Alternate Function
V_{CC}	Power supply	Power supply inputs 3 0 to 5 5V to V_{CC}, and 0V to V_{SS}	
V_{SS}			
CNV_{SS}	CNV_{SS}	This pin controls the operation mode of the chip. Normally connected to V_{SS} If this pin is connected to V_{CC}, the internal ROM is inhibited and external memory is accessed.	
$\overline{\text{RESET}}$	Reset input	To reset the microcomputer, this pin should be kept at an "L" level for more than 2μs under normal operating conditions	
X_{IN}	Clock input	Input and output signals for the internal clock generation circuit. Connect a ceramic resonator or quartz crystal between the X_{IN} and X_{OUT} pins to set the oscillation frequency If an external clock is used, connect the clock source to the X_{IN} pin and leave the X_{OUT} pin open	
X_{OUT}	Clock output		
$P0_0$—$P0_7$	I/O port P0	An 8 bit CMOS I/O port An I/O direction register allows each pin to be individually programmed as either input or output At reset this port is set to input mode In modes other than single-chip, these pins are used as address, data, and control bus I/O pins	
$P1_0$—$P1_7$	I/O port P1		
$P2_0$—$P2_7$	I/O port P2		
$P3_0$—$P3_7$	I/O port P3		
$P4_0$, $P4_1$	I/O port P4	An 8-bit CMOS I/O port with the same function as port P0	
$P4_2/INT_0$, $P4_3/INT_1$			External interrupt input pins
$P4_4/R_XD$, $P4_5/T_XD$, $P4_6/S_{CLK}$, $P4_7/S_{RDY}$			Serial I/O I/O pins
$P5_0/INT_2$— $P5_3/INT_5$	I/O port P5	An 8-bit CMOS I/O port with the same function as port P0	External interrupt input pins
$P5_4/CNTR_0$, $P5_5/CNTR_1$			Timer X and Timer Y I/O pins
$P5_6$, $P5_7$			
$P6_0$—$P6_7$	I/O port P6	An 8-bit CMOS I/O port with the same function as port P0	
$P7_0$, $P7_1$	I/O port P7	An 2-bit CMOS I/O port with the same function as port P0	

PART NUMBERING

Product name M3800 2 M 4 - XXX SP

Package type
- SP: 64P4B package
- FP: 64P6N package
- SS· 64S1B package
- FS· 64D0 package

ROM number
- Omitted in some types.

ROM/PROM size
- 1 · 4096 bytes
- 2 8192 bytes
- 3 12288 bytes
- 4 · 16384 bytes
- 5 20480 bytes
- 6 24576 bytes
- 7 28672 bytes
- 8 · 32768 bytes

The first 128 bytes and the last two bytes of ROM are reserved areas, they can not be used

Memory type
- M. Mask ROM version
- E EPROM or one-time programmable version

RAM size
- 0 . 192 bytes
- 1 256 bytes
- 2 384 bytes
- 3 512 bytes
- 4 640 bytes
- 5 768 bytes
- 6 896 bytes
- 7 1024 bytes

GROUP EXPANSION

Mitsubishi plans to expand the M3800x group as follows:

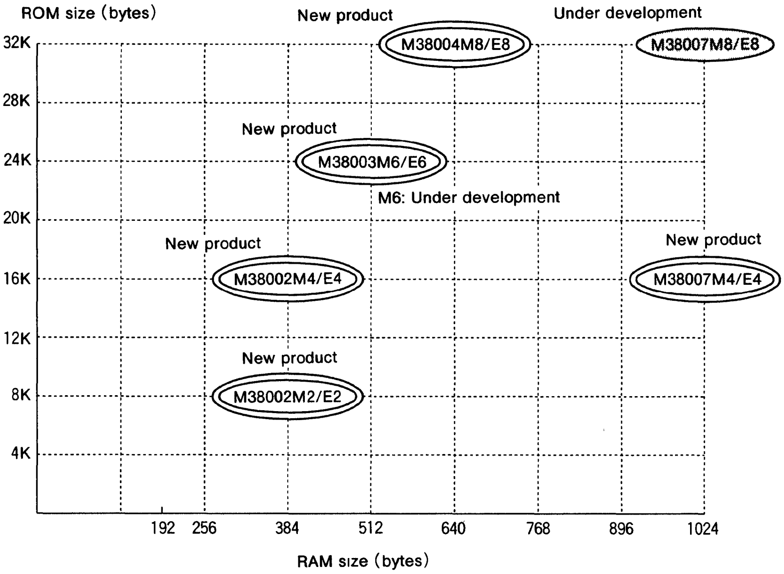
(1) Support for mask ROM, one-time programmable, and EPROM versions

ROM/PROM capacity	8K to 32K bytes
RAM capacity	384 to 1024 bytes

(2) Packages

64P4B	Shrink plastic molded DIP
64P6N	Plastic molded QFP
64S1B	Shrink ceramic DIP
64D0	Ceramic LCC

Memory expansion plan



The development schedule and other details of products under development may be revised without notice

Currently supported products are listed below

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

As of March 1992

Product name	(P) ROM size (bytes)	RAM size (bytes)	Package	Remarks
M38002M4-XXXSP	16K	384	64P4B	Mask ROM version
M38002E4-XXXSP				One-time programmable version
M38002E4SP				One-time programmable version (blank)
M38002M4-XXXFP			64P6N	Mask ROM version
M38002E4-XXXFP				One-time programmable version
M38002E4FP				One-time programmable version (blank)
M38002E4SS			64S1B	EPROM version
M38002E4FS			64D0	EPROM version
M38002M2-XXXSP	8K	384	64P4B	Mask ROM version
M38002E2-XXXSP				One-time programmable version
M38002E2SP				One-time programmable version (blank)
M38002M2-XXXFP			64P6N	Mask ROM version
M38002E2-XXXFP				One-time programmable version
M38002E2FP				One-time programmable version (blank)
M38002E2SS			64S1B	EPROM version
M38002E2FS			64D0	EPROM version
M38004M8-XXXSP	32K	640	64P4B	Mask ROM version
M38004E8-XXXSP				One-time programmable version
M38004E8SP				One-time programmable version (blank)
M38004M8-XXXFP			64P6N	Mask ROM version
M38004E8-XXXFP				One-time programmable version
M38004E8FP				One-time programmable version (blank)
M38004E8SS			64S1B	EPROM version
M38004E8FS			64D0	EPROM version
M38007M4-XXXSP	8K	1024	64P4B	Mask ROM version
M38007E4-XXXSP				One-time programmable version
M38007E4SP				One-time programmable version (blank)
M38007M4-XXXFP			64P6N	Mask ROM version
M38007E4-XXXFP				One-time programmable version
M38007E4FP				One-time programmable version (blank)
M38007E4SS			64S1B	EPROM version
M38007E4FS			64D0	EPROM version
M38003E6-XXXSP	24K	512	64P4B	One-time programmable version
M38003E6SP				One-time programmable version (blank)
M38003E6-XXXFP			64P6N	One-time programmable version
M38003E6FP				One-time programmable version (blank)
M38003E6SS			64S1B	EPROM version
M38003E6FS			64D0	EPROM version

FUNCTIONAL DESCRIPTION

Central Processing Unit (CPU)

Microcomputers of the M3800x group use the standard MELPS 740 instruction set. Refer to the table of MELPS 740 addressing modes and machine instructions or the MELPS 740 Software Manual for details on the instruction set.

Machine-resident MELPS 740 instructions are as follows·

The FST and SLW instructions are not available for use.
The STP, WIT, MUL, and DIV instructions can be used.

CPU Mode Register

The CPU mode register (address $003B_{16}$) contains processor mode bits that specify the operating mode of the chip. The CPU mode register also contains the stack page select bit.

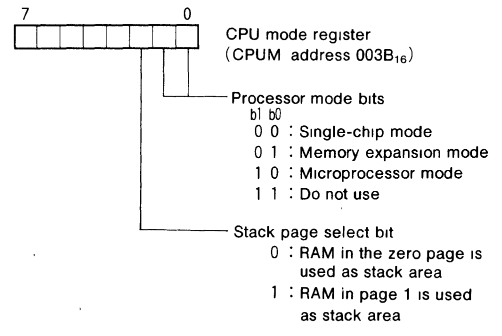


Fig. 1 Structure of CPU mode register

MEMORY

- **Special Function Register (SFR) Area**
  The Special Function Register area contains registers which control functions such as I/O ports and timers, and is located in the zero page area.
- **RAM**
  RAM is used for data storage as well for stack area.
- **ROM**
  The first 128 bytes and the last two bytes of ROM are reserved for device testing and the rest is user area for storing programs.
- **Interrupt Vector Area**
  The interrupt vector area contains reset and interrupt vectors.
- **Zero Page**
  The 256 bytes from addresses 0000_{16} to $00FF_{16}$ are called the zero page area. The internal RAM and the special function registers (SFR) are allocated to this area.
  The zero page addressing mode can be used to specify memory and register addresses in the zero page area. This dedicated zero page addressing mode enables access to this area with only 2 bytes.
- **Special Page**
  The 256 bytes from addresses $FF00_{16}$ to $FFFF_{16}$ are called the special page area. The special page addressing mode can be used to specify memory addresses in the special page area. This dedicated special page addressing mode enables access to this area with only 2 bytes.

RAM area

RAM capacity (bytes)	Address $XXXX_{16}$
192	$00FF_{16}$
256	$013F_{16}$
384	$01BF_{16}$
512	$023F_{16}$
640	$02BF_{16}$
768	$033F_{16}$
896	$03BF_{16}$
1024	$043F_{16}$

ROM area

ROM capacity (bytes)	Address $YYYY_{16}$	Address $ZZZZ_{16}$
4096	$F000_{16}$	$F080_{16}$
8192	$E000_{16}$	$E080_{16}$
12288	$D000_{16}$	$D080_{16}$
16384	$C000_{16}$	$C080_{16}$
20480	$B000_{16}$	$B080_{16}$
24576	$A000_{16}$	$A080_{16}$
28672	9000_{16}	9080_{16}
32768	8000_{16}	8080_{16}

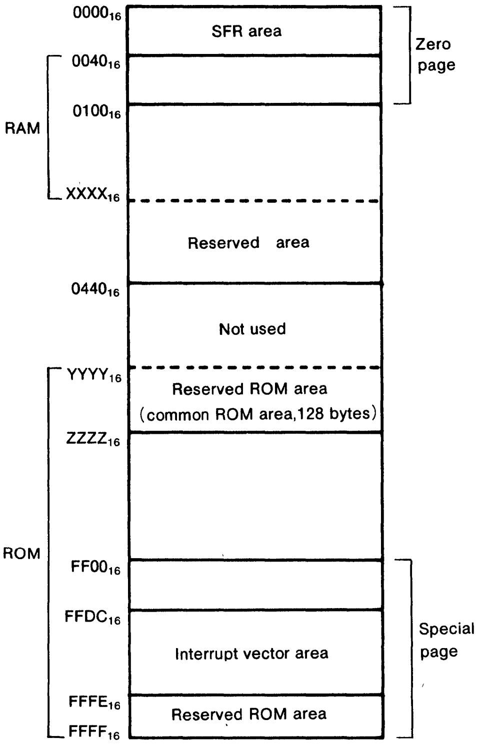


Fig. 2 Memory map diagram

0000_{16}	Port P0 (P0)	0020_{16}	Prescaler 12 (PRE12)
0001_{16}	Port P0 direction register (P0D)	0021_{16}	Timer 1 (T1)
0002_{16}	Port P1 (P1)	0022_{16}	Timer 2 (T2)
0003_{16}	Port P1 direction register (P1D)	0023_{16}	Timer XY mode register (TM)
0004_{16}	Port P2 (P2)	0024_{16}	Prescaler X (PREX)
0005_{16}	Port P2 direction register (P2D)	0025_{16}	Timer X (TX)
0006_{16}	Port P3 (P3)	0026_{16}	Prescaler Y (PREY)
0007_{16}	Port P3 direction register (P3D)	0027_{16}	Timer Y (TY)
0008_{16}	Port P4 (P4)	0028_{16}	
0009_{16}	Port P4 direction register (P4D)	0029_{16}	
$000A_{16}$	Port P5 (P5)	$002A_{16}$	
$000B_{16}$	Port P5 direction register (P5D)	$002B_{16}$	
$000C_{16}$	Port P6 (P6)	$002C_{16}$	
$000D_{16}$	Port P6 direction register (P6D)	$002D_{16}$	
$000E_{16}$	Port P7 (P7)	$002E_{16}$	
$000F_{16}$	Port P7 direction register (P7D)	$002F_{16}$	
0010_{16}		0030_{16}	
0011_{16}		0031_{16}	
0012_{16}		0032_{16}	
0013_{16}		0033_{16}	
0014_{16}		0034_{16}	
0015_{16}		0035_{16}	
0016_{16}		0036_{16}	
0017_{16}		0037_{16}	
0018_{16}	Transmit/receive buffer (TB/RB)	0038_{16}	
0019_{16}	Serial I/O status register (SIOSTS)	0039_{16}	
$001A_{16}$	Serial I/O control register (SIOCON)	$003A_{16}$	Interrupt edge selection register (INTEDGE)
$001B_{16}$	UART control register (UARTCON)	$003B_{16}$	CPU mode register (CPUM)
$001C_{16}$	Baud rate generator (BRG)	$003C_{16}$	Interrupt request register 1 (IREQ1)
$001D_{16}$		$003D_{16}$	Interrupt request register 2 (IREQ2)
$001E_{16}$		$003E_{16}$	Interrupt control register 1 (ICON1)
$001F_{16}$		$003F_{16}$	Interrupt control register 2 (ICON2)

Fig. 3 Memory map of special function register (SFR)

I/O PORTS

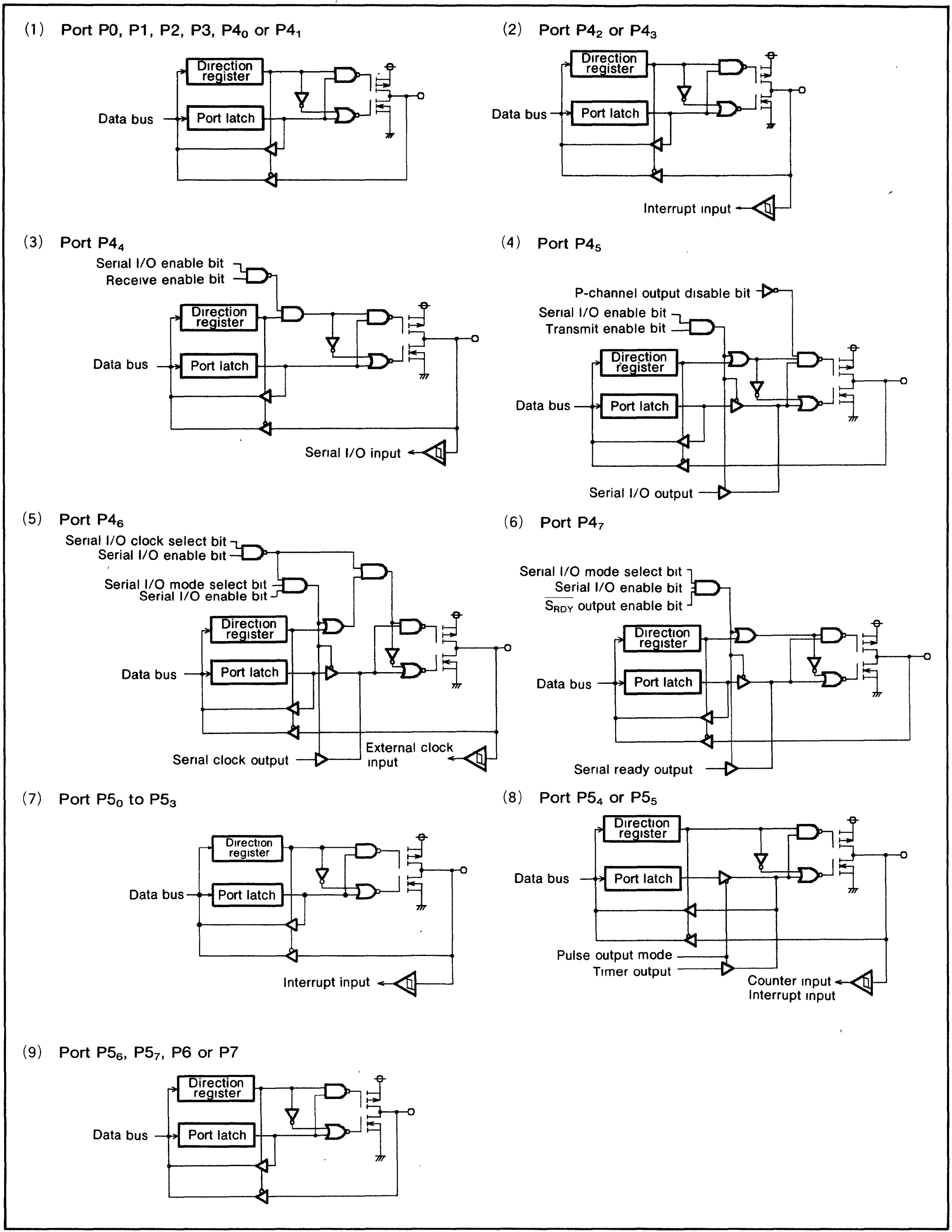
Direction Registers

The M3800x group microprocessors have 72 programmable I/O pins arranged in nine I/O ports (ports P0 to P7). The I/O ports have direction registers which determine the input/output direction of each individual pin. Each bit in a direction register corresponds to one pin, each pin can be set to be input or output. When "0" is written to the bit corresponding to a pin, that pin becomes an input pin. When "1" is written to that bit, that pin becomes an output pin.

If data is read from a pin which is set for output, the value of the port output latch is read, not the value of the pin itself. Pins set to input are floating. If a pin set to input is written to, only the port output latch is written to and the pin remains floating.

Pin	Name	Input/Output	I/O Format	Non-Port Function	Related SFRs	Ref No.
$P0_0$—$P0_7$	Port P0	Input/output, individual bits	CMOS 3-state output CMOS level input	Address lower-byte output	CPU mode register	(1)
$P1_0$—$P1_7$	Port P1	Input/output, individual bits	CMOS 3-state output CMOS level input	Address upper-byte output	CPU mode register	
$P2_0$—$P2_7$	Port P2	Input/output, individual bits	CMOS 3-state output CMOS level input	Data bus I/O	CPU mode register	
$P3_0$—$P3_7$	Port P3	Input/output, individual bits	CMOS 3-state output CMOS level input	Control signal I/O	CPU mode register	
$P4_0$, $P4_1$	Port P4	Input/output, individual bits	CMOS 3-state output CMOS level input			
$P4_2/INT_0$, $P4_3/INT_1$				External interrupt input	Interrupt edge selection register	(2)
$P4_4/R_XD$,				Serial I/O function I/O	Serial I/O control register UART control register	(3)
$P4_5/T_XD$,						(4)
$P4_6/S_{CLK}$,						(5)
$P4_7/\overline{S_{RDY}}$						(6)
$P5_0/INT_2$, $P5_1/INT_3$, $P5_2/INT_4$, $P5_3/INT_5$	Port P5	Input/output, individual bits	CMOS 3-state output CMOS level input	External interrupt input	Interrupt edge selection register	(7)
$P5_4/CNTR_0$, $P5_5/CNTR_1$				Timer XY function I/O		(8)
$P5_6$, $P5_7$						(9)
$P6_0$—$P6_7$	Port P6	Input/output, individual bits	CMOS 3-state output CMOS level input			
$P7_0$, $P7_1$	Port P7	Input/output, individual bits	CMOS 3-state output CMOS level input			

Note : For details of the functions of ports P0 to P3 in modes other than single-chip mode, and how to use double-function ports as function I/O ports, see the applicable sections



(1) Port P0, P1, P2, P3, $P4_0$ or $P4_1$

(2) Port $P4_2$ or $P4_3$

(3) Port $P4_4$

(4) Port $P4_5$

(5) Port $P4_6$

(6) Port $P4_7$

(7) Port $P5_0$ to $P5_3$

(8) Port $P5_4$ or $P5_5$

(9) Port $P5_6$, $P5_7$, P6 or P7

Fig. 4 Port block diagram (single-chip mode)

INTERRUPTS

A total of 15 sources can generate interrupts: 8 external, 6 internal, and 1 software.

- **Interrupt Control**

  Each interrupt is controlled by an interrupt request bit, an interrupt enable bit, and the interrupt disable flag-except for the software interrupt set by the BRK instruction. An interrupt is generated if the corresponding interrupt request and enable bits are "1" and the interrupt disable flag is "0".

  Interrupt enable bits can be set or cleared by software

  Interrupt request bits can be cleared by software, but cannot be set by software.

  The I flag disables all interrupts except for the BRK instruction interrupt.

- **Interrupt Operation**

  When an interrupt is received, the program counter and processor status register are automatically pushed onto the stack. The interrupt disable flag is set to inhibit other interrupts from interfering. The corresponding interrupt request bit is cleared and the interrupt jump destination address is read from the vector table into the program counter.

- **Notes on Use**

  When the active edge of an external interrupt (INT_0 to INT_5, $CNTR_0$, or $CNTR_1$) is changed, the corresponding interrupt request bit may also be set. To insure proper operation when selecting the active edge, disable interrupts before setting the interrupt edge selection.

Table 1 Interrupt vector addresses and priorities

Interrupt cause	Priority	Vector address (Note 1)		Interrupt request generation conditions	Remarks
		High	Low		
Reset (Note 2)	1	$FFFD_{16}$	$FFFC_{16}$	At reset	Non-maskable
INT_0	2	$FFFB_{16}$	$FFFA_{16}$	At detection of either rising or falling edge of INT_0 input	External interrupt (active edge selectable)
INT_1	3	$FFF9_{16}$	$FFF8_{16}$	At detection of either rising or falling edge of INT_1 input	External interrupt (active edge selectable)
Serial I/O reception	4	$FFF7_{16}$	$FFF6_{16}$	At end of serial I/O1 data reception	Valid when serial I/O1 is selected
Serial I/O transmission	5	$FFF5_{16}$	$FFF4_{16}$	At end of serial I/O1 transfer shift or when transmission buffer is empty	Valid when serial I/O1 is selected
Timer X	6	$FFF3_{16}$	$FFF2_{16}$	At timer X overflow	
Timer Y	7	$FFF1_{16}$	$FFF0_{16}$	At timer Y overflow	
Timer 1	8	$FFEF_{16}$	$FFEE_{16}$	At timer 1 overflow	STP release timer overflow
Timer 2	9	$FFED_{16}$	$FFEC_{16}$	At timer 2 overflow	
$CNTR_0$	10	$FFEB_{16}$	$FFEA_{16}$	At detection of either rising or falling edge of $CNTR_0$ input	External interrupt (active edge selectable)
$CNTR_1$	11	$FFE9_{16}$	$FFE8_{16}$	At detection of either rising or falling edge of $CNTR_1$ input	External interrupt (active edge selectable)
INT_2	12	$FFE7_{16}$	$FFE6_{16}$	At detection of either rising or falling edge of INT_2 input	External interrupt (active edge selectable)
INT_3	13	$FFE5_{16}$	$FFE4_{16}$	At detection of either rising or falling edge of INT_3 input	External interrupt (active edge selectable)
INT_4	14	$FFE3_{16}$	$FFE2_{16}$	At detection of either rising or falling edge of INT_4 input	External interrupt (active edge selectable)
INT_5	15	$FFE1_{16}$	$FFE0_{16}$	At detection of either rising or falling edge of INT_5 input	External interrupt (active edge selectable)
BRK instruction	16	$FFDD_{16}$	$FFDC_{16}$	At BRK instruction execution	Non-maskable software interrupt

Note 1 : Vector addresses contain interrupt jump destination addresses
2 : Reset function in the same way as an interrupt with the highest priority

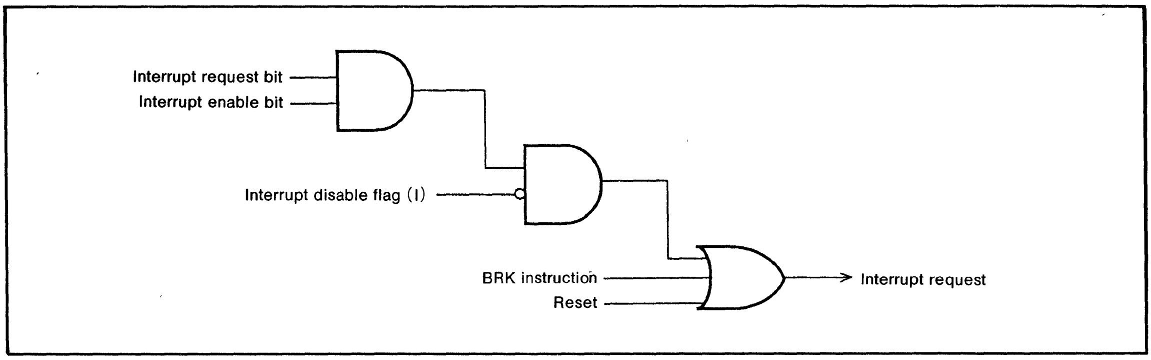


Fig. 5 Interrupt control

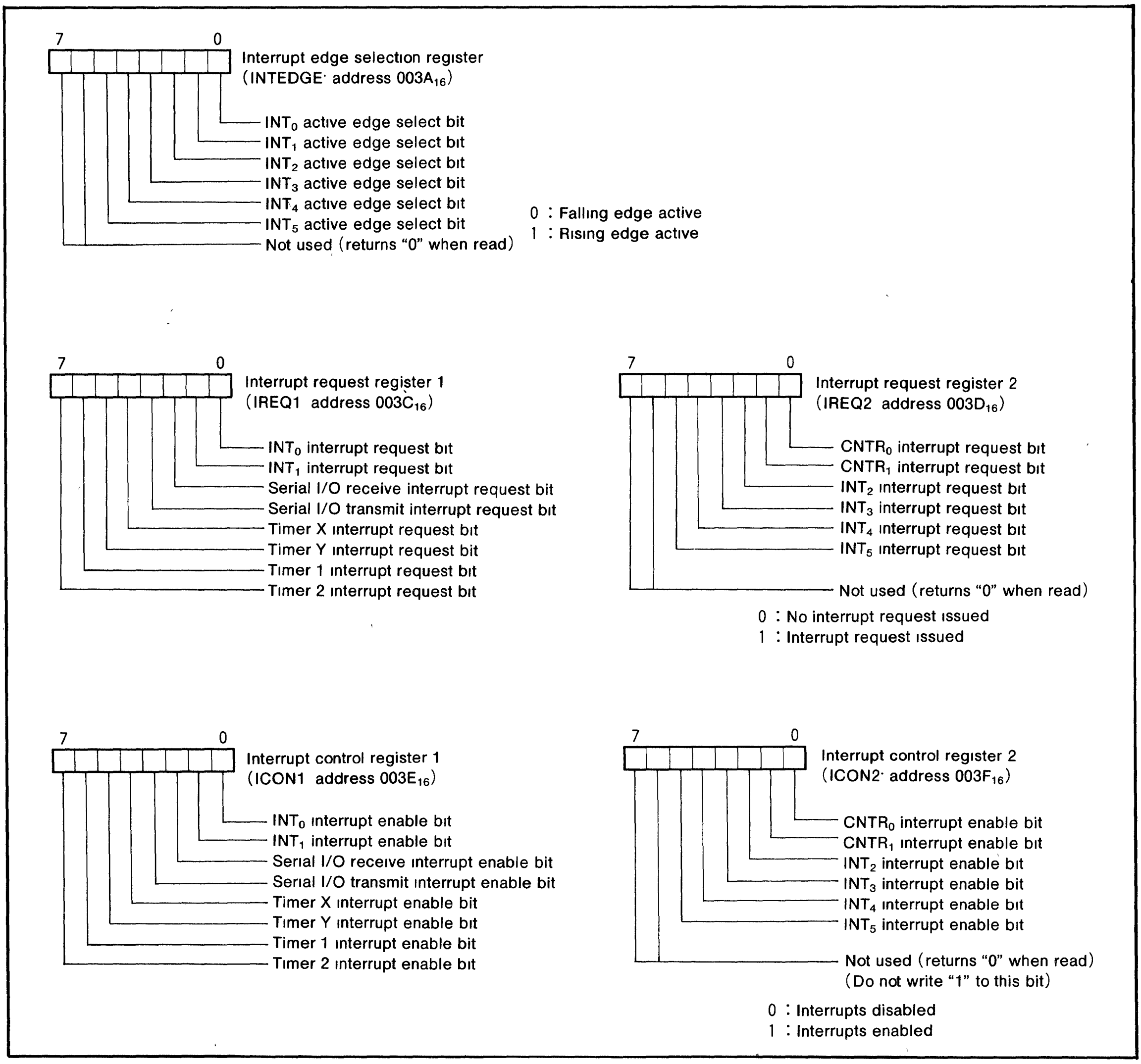


Fig. 6 Structure of interrupt-related registers

TIMERS

Microcomputers of the M3800x group have 4 timers: timer X, timer Y, timer 1, and timer 2.

The timers count down. Once a timer reaches 00_{16}, the next count pulse reloads the contents of the corresponding timer latch into the timer, and sets the corresponding interrupt request bit to 1.

The divide ratio of each timer or prescaler is given by $1/(n+1)$, where n is the value in the corresponding timer or prescaler latch.

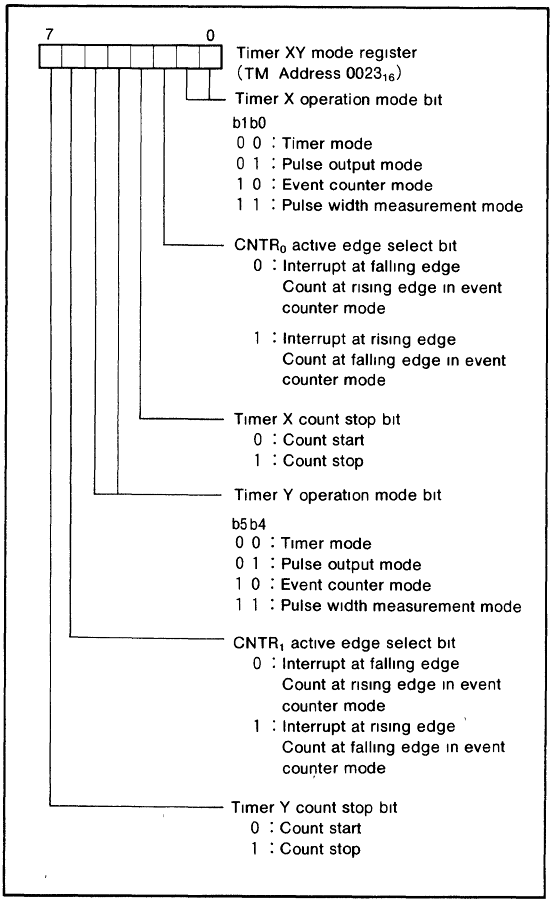


Fig. 7 Structure of timer XY register

Timer 1 and Timer 2

The count source of prescaler 12 is the oscillation frequency divided by 16. The output of prescaler 12 is counted by timer 1 and timer 2, and a timer overflow sets the interrupt request bit.

Timer X and Timer Y

Timer X and Timer Y can each be set to operate in one of four operating modes by setting the timer XY mode register.

1. Timer Mode
   In timer mode, the timer counts a signal that is the oscillation frequency divided by 16.
2. Pulse Output Mode
   Timer X (or timer Y) counts a signal which is the oscillation frequency divided by 16. Whenever the contents of the timer reach "0", the signal output from the $CNTR_0$ (or $CNTR_1$) pin is inverted. If the $CNTR_0$ (or $CNTR_1$) active edge select bit is "0", output begins at "H". If it is "1", output starts at "L". When using a timer in this mode, set the corresponding port $P5_4$ (or port $P5_5$) direction register to output mode.
3. Event Counter Mode
   Operation in event counter mode is the same as in timer mode, except the timer counts signals input through the $CNTR_0$ or $CNTR_1$ pin.
4. Pulse Width Measurement Mode
   If the $CNTR_0$ (or $CNTR_1$) active edge select bit is "0", the timer counts at the oscillation frequency divided by 16 while the $CNTR_0$ (or $CNTR_1$) pin is at "H". If the $CNTR_0$ (or $CNTR_1$) active edge select bit is "1", the count continues during the time that the $CNTR_0$ (or $CNTR_1$) pin is at "L"

In all of these modes, the count can be stopped by setting the timer X (timer Y) count stop bit to "1". Every time a timer overflows, the corresponding interrupt request bit is set.

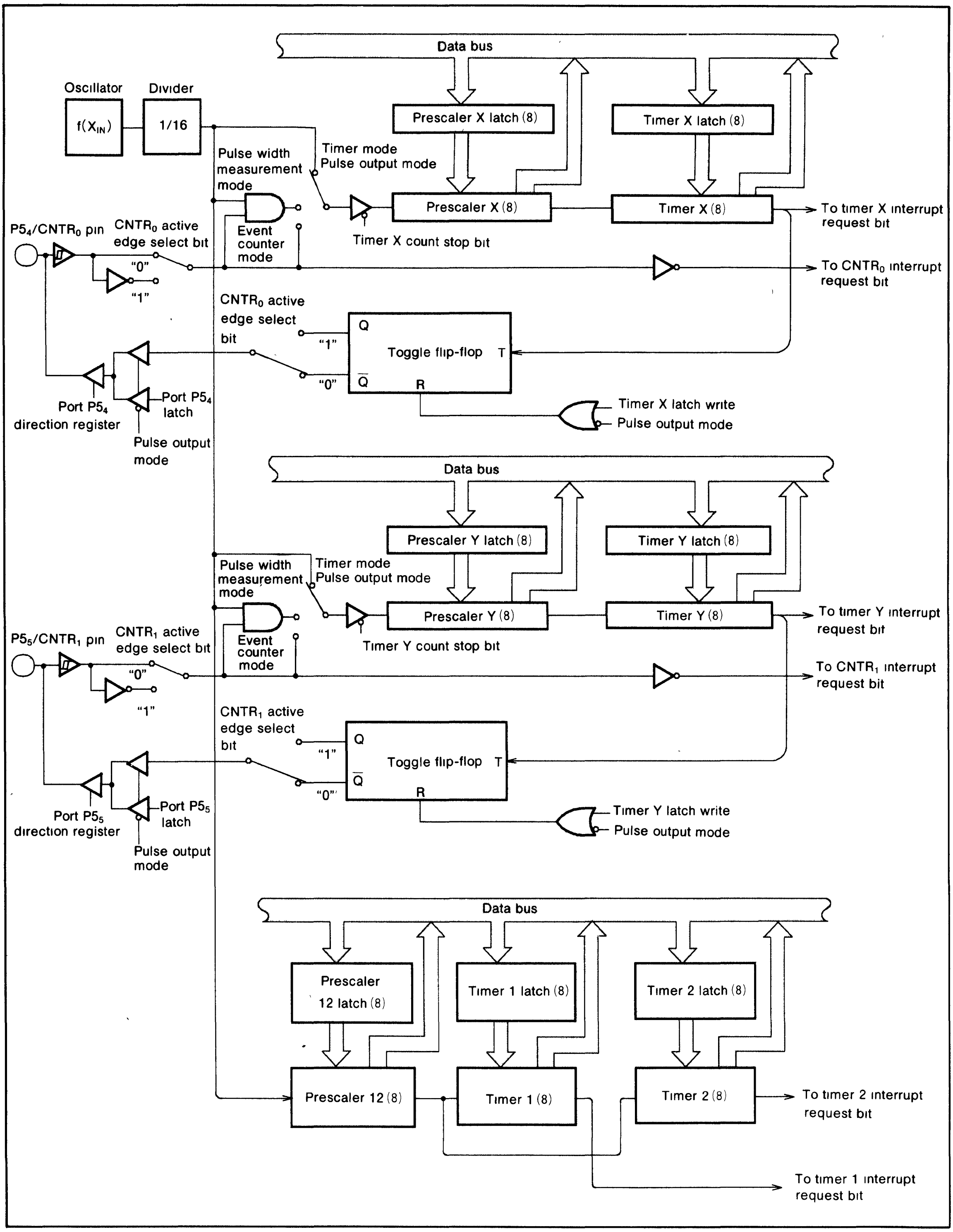


Fig. 8 Block diagram of timer X, timer Y, timer 1, and timer 2

SERIAL I/O

Serial I/O can be used as either clock synchronous or asynchronous (UART) serial I/O. A dedicated timer is also provided for baud rate generation.

(1) Clock Synchronous Serial I/O

Clock synchronous serial I/O mode can be selected by setting the mode select bit of the serial I/O control register to "1"

For clock-synchronized serial I/O, the transmitter and the receiver must use the same clock. If an internal clock is used, transfer is started by a write signal to the transmit or receive buffer.

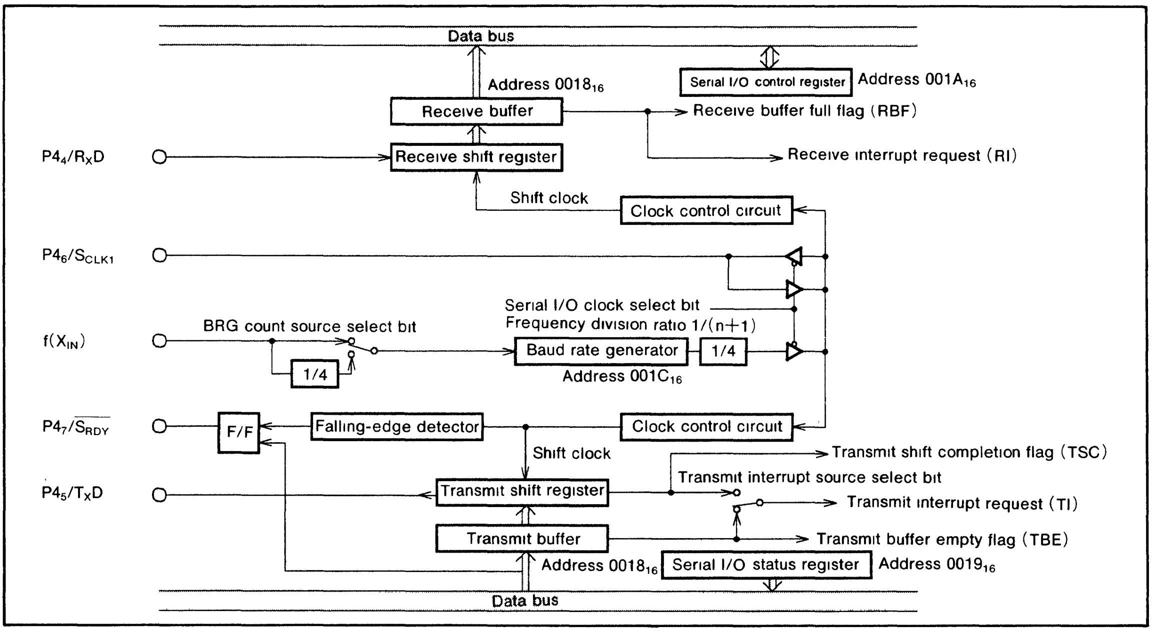
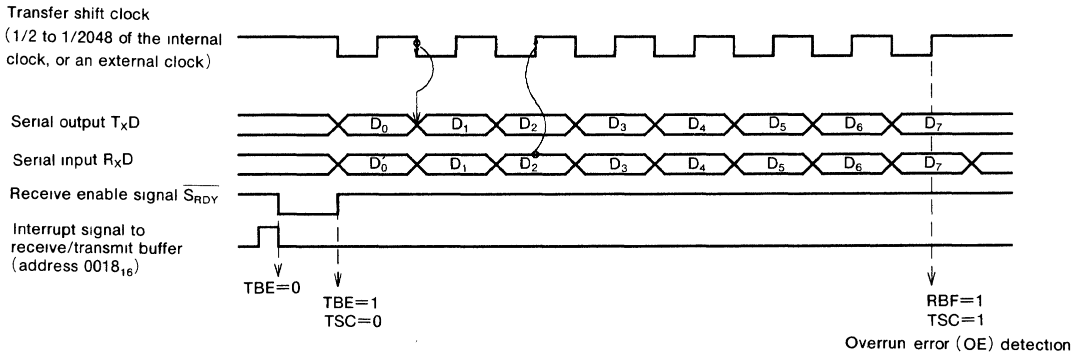


Fig. 9 Block diagram of clock-synchronized serial I/O



Note 1 : The transmit interrupt (TI) can be selected to occur either when the transmit buffer has emptied (TBE=1) or after the transmit shift operation has ended (TSC=1), by setting the transmit interrupt source select bit (TIC) of the serial I/O control register

2 : If data is written to the transfer buffer when TSC=0, the transmit clock is generated continuously and serial data is output continuously from the T_xD pin

3 : The receive interrupt (RI) is set when the receive buffer full (RBF) flag becomes "1"

Fig. 10 Operation of clock-synchronized serial I/O function

(2) Asynchronous serial I/O (UART) mode

Clock asynchronous serial I/O mode (UART) can be selected by clearing the serial I/O mode select bit of the serial I/O control register to "0".

Eight serial data transfer formats can be selected, and the transfer formats used by a transmitter and receiver must be identical.

The transmit and receive shift registers each have a buffer, but the two buffers have the same address in memory. Since the shift register cannot be written to or read from directly, transmit data is written to the transmit buffer, and receive data is read from the receive buffer. The transmit buffer can also hold the next data to be transmitted, and the receive buffer can hold a character while the next character is being received.

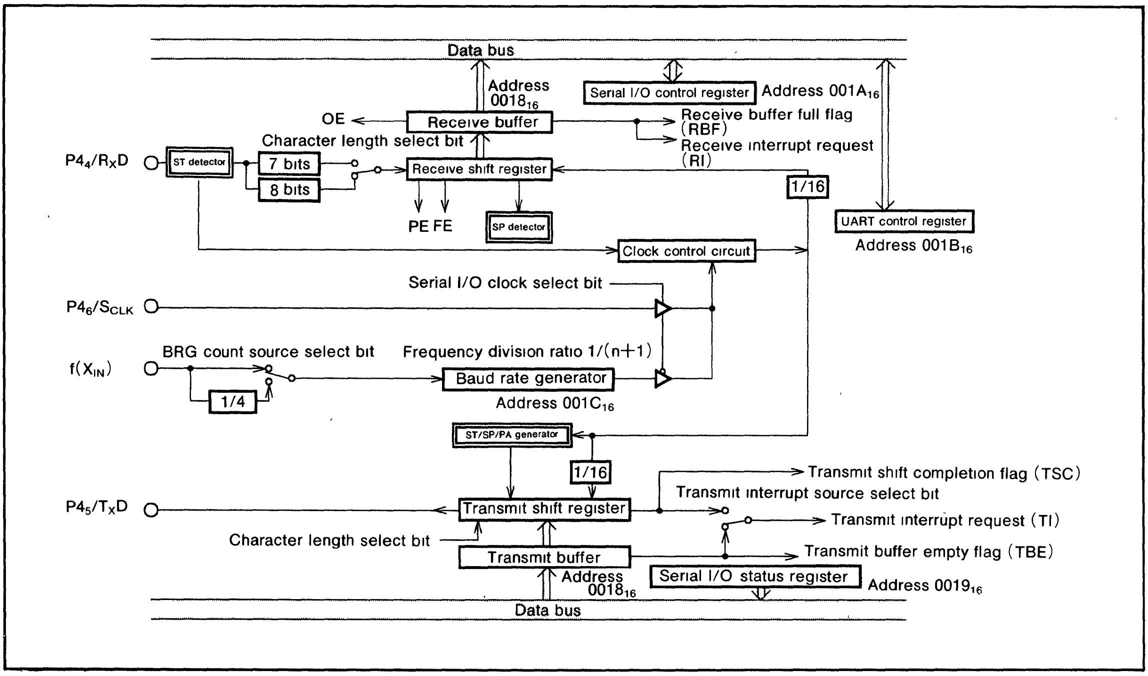
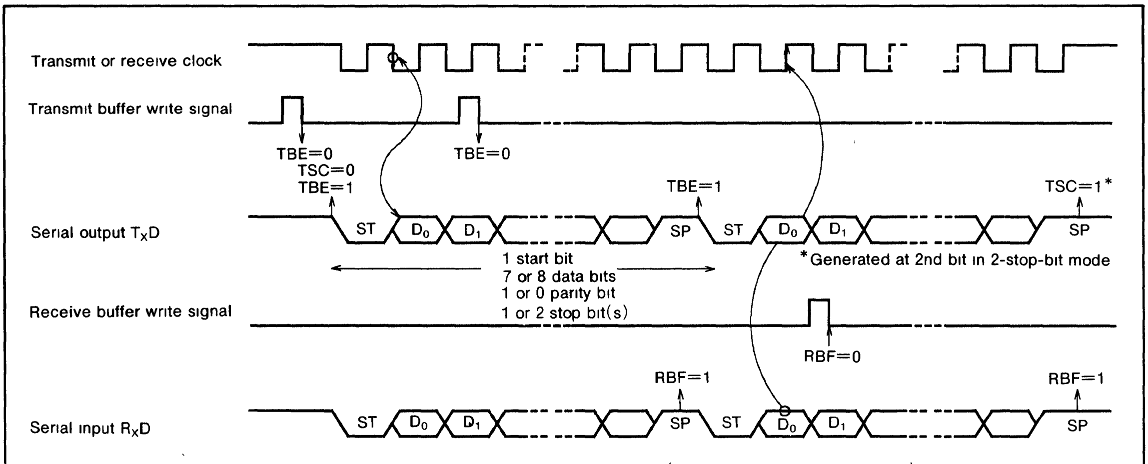


Fig. 11 Block diagram of UART serial I/O



Note 1 : Error flag detection occurs at the same time that the RBF flag becomes "1" (at 1st stop bit, during reception)
2 : The transmit interrupt (TI) can be selected to occur when either the TBE or TSC flag becomes "1", depending on the setting of the transmit interrupt source select bit (TIC) of the serial I/O control register
3 : The receive interrupt (RI) is set when the RBF flag becomes "1"

Fig. 12 Operation of UART serial I/O function

[Serial I/O Control Register (SIOCON) 001A$_{16}$]

The serial I/O control register contains eight control bits for the serial I/O function.

[UART Control Register (UARTCON) 001B$_{16}$]

The UART control register consists of four control bits (bits 0 to 3) which are valid when asynchronous serial I/O is selected and set the data format of an data transfer. One bit in this register (bit 4) is always valid and sets the output structure of the P4$_5$/T$_X$D pin.

[Serial I/O Status Register (SIO1STS) 0019$_{16}$]

The read-only serial I/O status register consists of seven flags (bits 0 to 6) which indicate the operating status of the serial I/O function and various errors.

Three of the flags (bits 4 to 6) are valid only in UART mode.

The receive buffer full flag (bit 1) is cleared to "0" when the receive buffer is read.

If there is an error, it is detected at the same time that data is transferred from the receive shift register to the receive buffer, and the receive buffer full flag is set. A write to the serial I/O status register clears all the error flags OE, PE, FE, and SE (bit 3 to bit six, respectively). Writing "0" to the serial I/O enable bit SIOE (bit 7 of the Serial I/O Control Register) also clears all the status flags, including the error flags.

All bits of the serial I/O status register are initialized to "0" at reset, but if the transmit enable bit (bit 4) of the serial I/O control register has been set to "1", the transmitter shift completion flag (bit 2) and the transmitter buffer empty flag (bit 0) become "1".

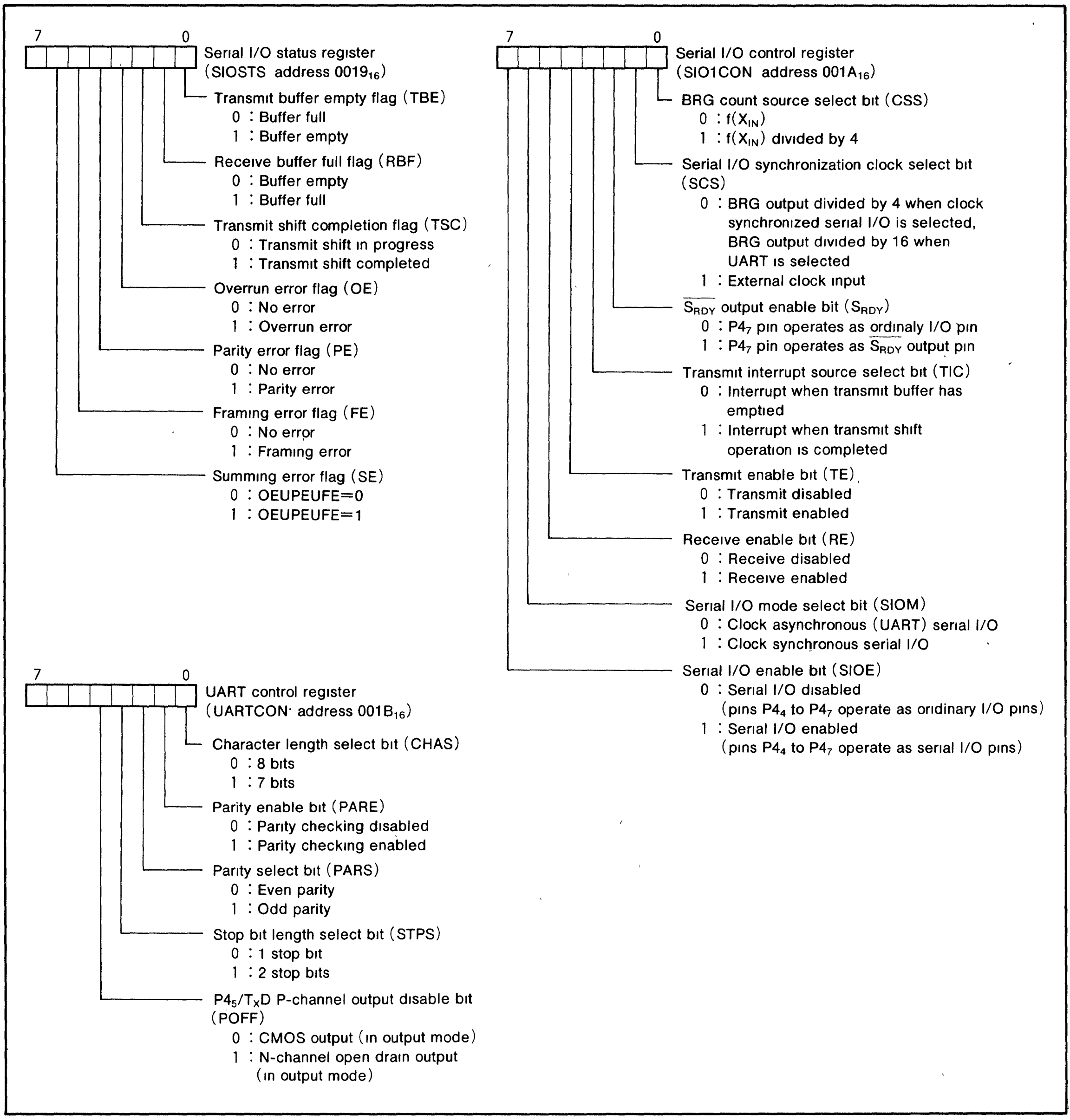
[Transmit Buffer/Receive Buffer (TB/RB) 0018$_{16}$]

The transmit buffer and the receive buffer are located at the same address. The transmit buffer is write-only and the receive buffer is read-only. If a character bit length is 7 bits, the MSB of data stored in the receive buffer is "0"

[Baud Rate Generator (BRG) 001C$_{16}$]

The baud rate generator determines the baud rate for serial transfer.

The baud rate generator divides the frequency of the count source by $1/(n+1)$, where n is the value written to the Baud Rate Generator.



Serial I/O status register
(SIOSTS address 0019_{16})

- Transmit buffer empty flag (TBE)
  - 0 : Buffer full
  - 1 : Buffer empty
- Receive buffer full flag (RBF)
  - 0 : Buffer empty
  - 1 : Buffer full
- Transmit shift completion flag (TSC)
  - 0 : Transmit shift in progress
  - 1 : Transmit shift completed
- Overrun error flag (OE)
  - 0 : No error
  - 1 : Overrun error
- Parity error flag (PE)
  - 0 : No error
  - 1 : Parity error
- Framing error flag (FE)
  - 0 : No error
  - 1 : Framing error
- Summing error flag (SE)
  - 0 : OEUPEUFE=0
  - 1 : OEUPEUFE=1

UART control register
(UARTCON· address $001B_{16}$)

- Character length select bit (CHAS)
  - 0 : 8 bits
  - 1 : 7 bits
- Parity enable bit (PARE)
  - 0 : Parity checking disabled
  - 1 : Parity checking enabled
- Parity select bit (PARS)
  - 0 : Even parity
  - 1 : Odd parity
- Stop bit length select bit (STPS)
  - 0 : 1 stop bit
  - 1 : 2 stop bits
- $P4_5/T_XD$ P-channel output disable bit (POFF)
  - 0 : CMOS output (in output mode)
  - 1 : N-channel open drain output (in output mode)

Serial I/O control register
(SIO1CON address $001A_{16}$)

- BRG count source select bit (CSS)
  - 0 : $f(X_{IN})$
  - 1 : $f(X_{IN})$ divided by 4
- Serial I/O synchronization clock select bit (SCS)
  - 0 : BRG output divided by 4 when clock synchronized serial I/O is selected, BRG output divided by 16 when UART is selected
  - 1 : External clock input
- $\overline{S_{RDY}}$ output enable bit (S_{RDY})
  - 0 : $P4_7$ pin operates as ordinaly I/O pin
  - 1 : $P4_7$ pin operates as $\overline{S_{RDY}}$ output pin
- Transmit interrupt source select bit (TIC)
  - 0 : Interrupt when transmit buffer has emptied
  - 1 : Interrupt when transmit shift operation is completed
- Transmit enable bit (TE)
  - 0 : Transmit disabled
  - 1 : Transmit enabled
- Receive enable bit (RE)
  - 0 : Receive disabled
  - 1 : Receive enabled
- Serial I/O mode select bit (SIOM)
  - 0 : Clock asynchronous (UART) serial I/O
  - 1 : Clock synchronous serial I/O
- Serial I/O enable bit (SIOE)
  - 0 : Serial I/O disabled (pins $P4_4$ to $P4_7$ operate as ordinary I/O pins)
  - 1 : Serial I/O enabled (pins $P4_4$ to $P4_7$ operate as serial I/O pins)

Fig. 13 Structure of serial I/O control registers

RESET CIRCUIT

A microcomputer in the M3800x group is reset if the $\overline{\text{RESET}}$ pin is held at a "L" level for at least $2\mu s$ then is returned to a "H" level (the power supply voltage should be between 4.0V and 5.5V). In order to give the X_{IN} clock time to stabilize, internal operation does not begin until after 8 to 12 X_{IN} clock cycles are complete. After the reset is completed, the program starts from the address contained in address $FFFD_{16}$ (upper byte) and address $FFFC_{16}$ (lower byte).
Make sure that the reset input voltage is no more than 0.8V for a power supply voltage of 4.0V.

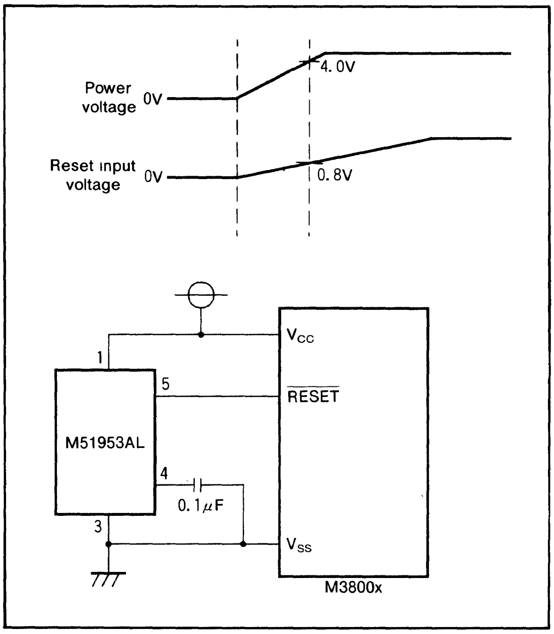
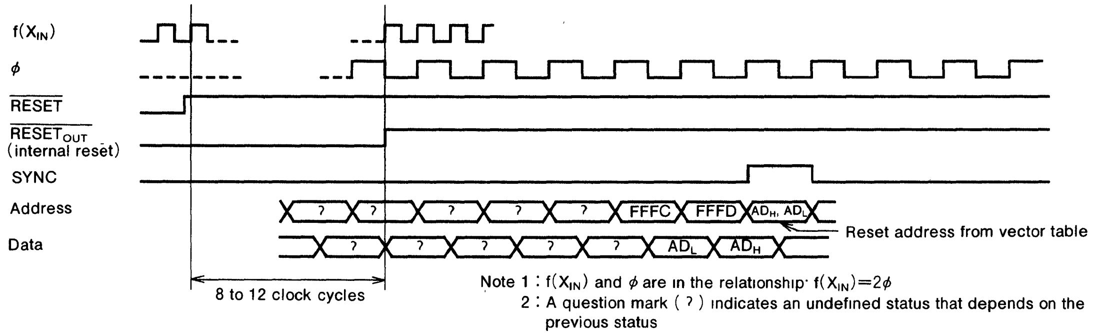


Fig. 14 Example of reset circuit

	Address	Register contents
(1) Port P0 direction register	(0001_{16})···	00_{16}
(2) Port P1 direction register	(0003_{16})···	00_{16}
(3) Port P2 direction register	(0005_{16})···	00_{16}
(4) Port P3 direction register	(0007_{16})···	00_{16}
(5) Port P4 direction register	(0009_{16})···	00_{16}
(6) Port P5 direction register	$(000B_{16})$···	00_{16}
(7) Port P6 direction register	$(000D_{16})$···	00_{16}
(8) Port P7 direction register	$(000F_{16})$···	00_{16}
(9) Serial I/O status register	(0019_{16})···	1 0 0 0 0 0 0 0
(10) Serial I/O control register	$(001A_{16})$···	00_{16}
(11) UART control register	$(001B_{16})$···	1 1 1 0 0 0 0 0
(12) Prescaler 12	(0020_{16})···	FF_{16}
(13) Timer 1	(0021_{16})···	01_{16}
(14) Timer 2	(0022_{16})···	FF_{16}
(15) Timer XY mode register	(0023_{16})···	00_{16}
(16) Prescaler X	(0024_{16})···	FF_{16}
(17) Timer X	(0025_{16})···	FF_{16}
(18) Prescaler Y	(0026_{16})···	FF_{16}
(19) Timer Y	(0027_{16})···	FF_{16}
(20) Interrupt edge selection register	$(003A_{16})$···	00_{16}
(21) CPU mode register	$(003B_{16})$···	0 0 0 0 0 0 ※ 0
(22) Interrupt control register 1	$(003E_{16})$···	00_{16}
(23) Interrupt control register 2	$(003F_{16})$···	00_{16}
(24) Processor status register	(PS)···	X X X X X 1 X X
(25) Program counter	(PC_H)···	Contents of address $FFFD_{16}$
	(PC_L)···	Contents of address $FFFC_{16}$

Note : X : Undefined
※ : The initial values of CM_1 are determined by the level at the CNV_{SS} pin
The contents of all other registers and RAM are undefined after a reset, so they must be initialized by software

Fig. 15 Internal status of microcomputer after reset



Note 1 : $f(X_{IN})$ and ϕ are in the relationship· $f(X_{IN})=2\phi$
2 : A question mark (?) indicates an undefined status that depends on the previous status

Fig. 16 Timing of reset

CLOCK GENERATION CIRCUIT

An oscillation circuit can be created by connecting a resonator between X_{IN} and X_{OUT}. When using an external clock signal, input the clock signal to the X_{IN} pin and leave the X_{OUT} pin open.

Oscillation Control

(1) Stop Mode

If the STP instruction is executed, oscillation stops with the internal clock ϕ at "H". Timer 1 is set to "FF_{16}" and prescaler 12 is set to "01_{16}".

Oscillation restarts when an external interrupt is received, but the internal clock ϕ remains at "H" until timer 1 overflows.

This allows time for the clock circuit oscillation to stabilize. If oscillation is restarted by a reset, no wait time is generated, so keep the $\overline{\text{RESET}}$ pin at "L" level until oscillation has stabilized.

(2) Wait Mode

If the WIT instruction is executed, the internal clock ϕ stops at a "H" level, but the oscillator itself does not stop. The internal clock restarts if a reset occurs or when an interrupt is received.

Since the oscillator does not stop, normal operation can be started immediately after the clock is restarted.

To ensure that interrupts will be received to release the STP or WIT state, interrupt enable bits must be set to "1" before the STP or WIT instruction is executed.

When the STP status is released, prescaler 12 and timer 1 will start counting and reset will not be released until timer 1 overflows, so set the timer 1 interrupt enable bit to "0" before the STP instruction is executed.

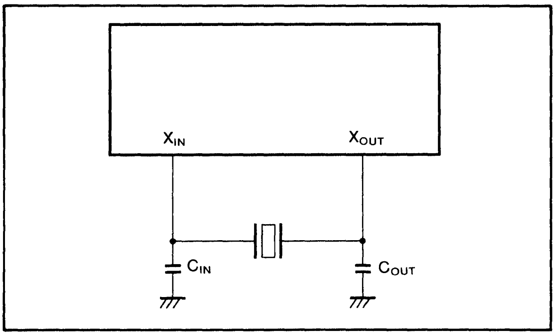


Fig. 17 Ceramic resonator circuit

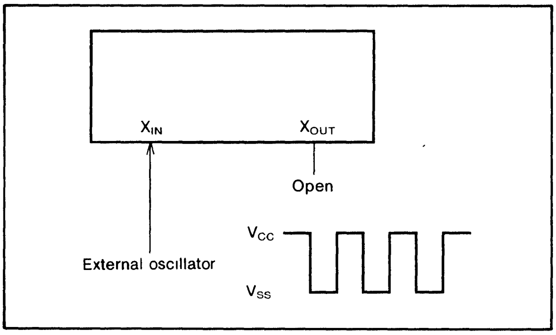


Fig. 18 External clock input circuit

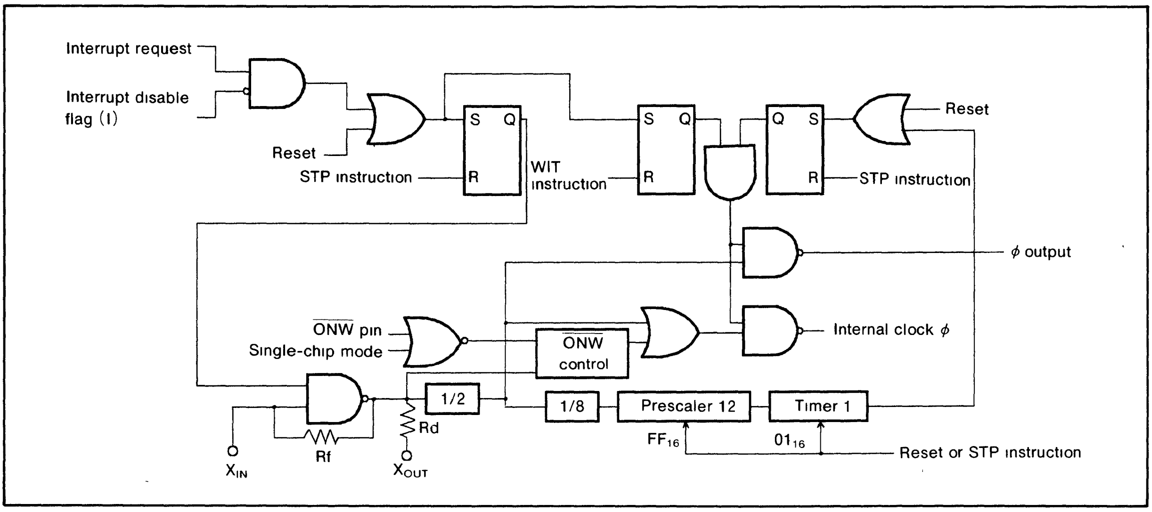


Fig. 19 Block diagram of clock generation circuit

PROCESSOR MODES

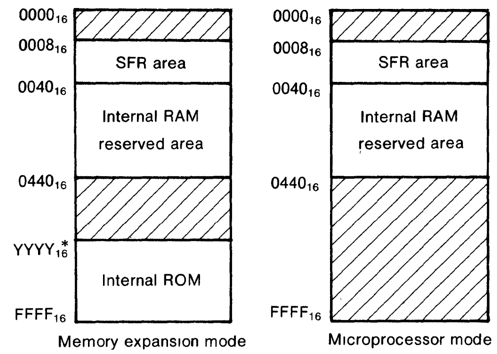
Single-chip mode, memory expansion mode, and microprocessor mode can be selected by changing the contents of the processor mode bits CM_0 and CM_1 (bits 0 and 1 of address $003B_{16}$). In memory expansion mode and microprocessor mode, memory can be expanded externally through ports P0 to P3. In these modes, ports P0 to P3 lose their I/O port functions and become bus pins.

Table 2 Functions of ports in memory expansion mode and microprocessor mode

Port Name	Function
Port P0	Outputs lower byte of address
Port P1	Outputs upper byte of address.
Port P2	Operates as I/O pins for data D_7 to D_0 (including instruction codes)
Port P3	$P3_0$ and $P3_1$ function only as output pins (except that the port latch cannot be read) $P3_2$ is the $\overline{\text{ONW}}$ input pin $P3_3$ is the $\overline{\text{RESET}_{\text{OUT}}}$ output pin. (Note) $P3_4$ is the ϕ output pin $P3_5$ is the SYNC output pin $P3_6$ is the $\overline{\text{WR}}$ output pin, and $P3_7$ is the $\overline{\text{RD}}$ output pin.

Note : If CNV_{SS} is connected to V_{SS}, the microcomputer goes to single-chip mode after a reset, so this pin cannot be used as the $\text{RESET}_{\text{OUT}}$ output pin

- **Single-Chip Mode**
  Select this mode by resetting the microcomputer with CNV_{SS} connected to V_{SS}.
- **Memory Expansion Mode**
  Select this mode by setting the processor mode bits to "01" in software with CNV_{SS} connected to V_{SS}. This mode enables external memory expansion while maintaining the validity of the internal ROM. Internal ROM will take precedence over external memory if addresses conflict.
- **Microprocessor Mode**
  Select this mode by resetting the microcomputer with CNV_{SS} connected to V_{CC}, or by setting the processor mode bits to "10" in software with CNV_{SS} connected to V_{SS}. In microprocessor mode, the internal ROM is no longer valid and external memory must be used.



The shaded areas are external memory areas
* : $YYYY_{16}$ is the start address of internal ROM

Fig. 20 Memory maps in various processor modes

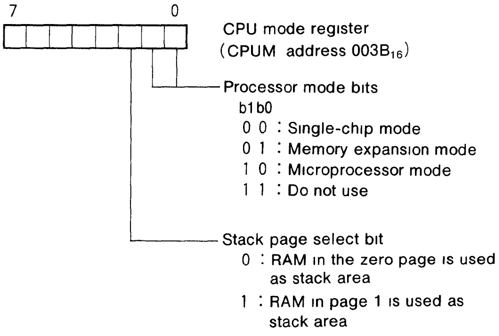
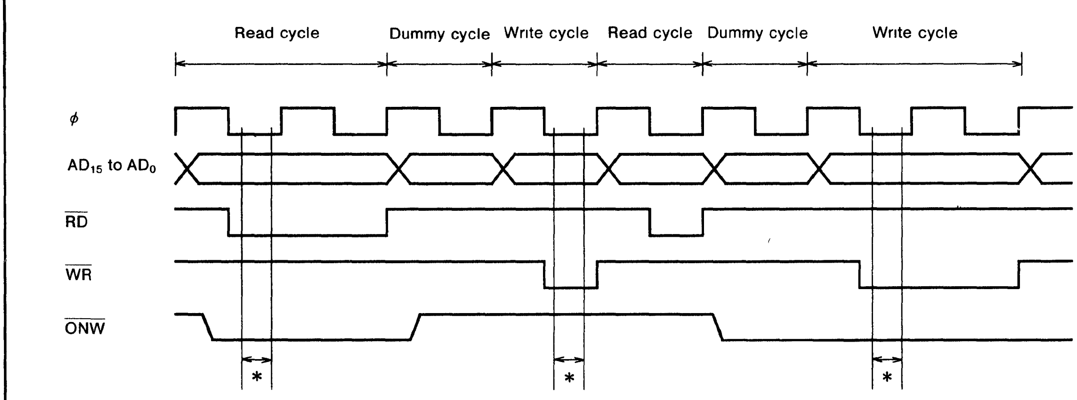


Fig. 21 Structure of CPU mode register

Bus Control with Memory Expansion

Microcomputers of the M3800x group have a built-in $\overline{\text{ONW}}$ function to facilitate access to extra memory and I/O functions in memory expansion mode or microprocessor mode. If an "L" level signal is input to the $\overline{\text{ONW}}$ pin when the CPU is in a read or write state, the corresponding read or write cycle is extended by one cycle of ϕ. During this extended period, the $\overline{\text{RD}}$ or $\overline{\text{WR}}$ signal remains at "L". This extension period is valid only for writing to and reading from addresses 0000_{16} to 0007_{16} and 0440_{16} to $FFFF_{16}$, and only read and write cycles are extended.



* : Period during which $\overline{\text{ONW}}$ input signal is received
During this period, the $\overline{\text{ONW}}$ signal must be fixed at either "H" or "L" At all other times, the input level of the $\overline{\text{ONW}}$ signal has no affect on operations
The bus cycles is not extended for an address in the area 0008_{16} to $043F_{16}$, regardless of whether the $\overline{\text{ONW}}$ signal is received

Fig. 22 $\overline{\text{ONW}}$ function timing

NOTES ON PROGRAMMING

Processor Status Register

The contents of the processor status register (PS) after a reset are undefined, except for the interrupt disable flag (I) which is "1". Therefore, flags that affect program execution must be initialized after a reset

In particular, it is essential to initialize the T and D flags because of their effect on calculations.

Interrupts

The contents of the interrupt request bits do not change immediately after they have been written. After writing to an interrupt request register, execute at least one instruction before performing a BBC or BBS instruction.

Decimal Calculations

To calculate in decimal notation, set the decimal mode flag (D) to "1", then execute a ADC or SBC instruction. Only the ADC and SBC instructions yield proper decimal results. After executing an ADC or SBC instruction, execute at least one instruction before executing a SEC, CLC, or CLD instruction.

In decimal mode, the values of the negative (N), overflow (V), and zero (Z) flags are invalid.

The carry flag can be used to indicate whether a carry or borrow has occurred, but must be initialized before each calculation. Clear the carry flag before an ADC and set the flag before an SBC.

Timers

If a value n (between 0 and 255) is written to a timer latch, the frequency division ratio is $1/(n+1)$

Multiplication and Division Instructions

The MUL and DIV instructions do not affect the T and D flags.

The execution of these instructions does not change the contents of the processor status register.

Ports

The contents of the port direction registers cannot be read. Programs can not use the value of a direction register as an index, or bit-test a direction register (BBC or BBS), or perform a read-modify-write instruction such as ROR, CLB, or SEB. Use instructions such as LDM and STA to set the port direction registers.

Serial I/O

In clock synchronous serial I/O, if the receive side is using an external clock and it is to output the $\overline{S_{RDY}}$ signal, set the transmit enable bit, the receive enable bit, and the $\overline{S_{RDY}}$ output enable bit to "1".

Serial I/O continues to output the final bit from the T_XD pin after transmission is completed.

Instruction Execution Time

The instruction execution time is obtained by multiplying the frequency of the internal clock ϕ by the number of cycles needed to execute an instruction.

The number of cycles required to execute an instruction is shown in the list of machine instructions.

The frequency of the internal clock ϕ is half of the X_{IN} frequency.

When the $\overline{ONW}$ function is used in modes other than single-chip mode, the frequency of the internal clock ϕ may be one fourth the X_{IN} frequency.

DATA REQUIRED FOR MASK ORDERS

The following are necessary when ordering a mask ROM production:

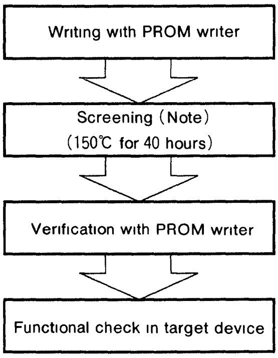
1. Mask ROM Order Confirmation Form
2. Mask Specification Form
3. Data to be written to ROM, in EPROM form (three identical copies)

ROM Writing Method

The built-in PROM of the blank one-time programmable version and built-in EPROM version can be read from and written to with an normal EPROM writer using a special write adapter.

Package	Name of Write Adapter
64P4B, 64S1B	PCA4738S-64
64P6N	PCA4738F-64
64D0	PCA4738L-64

The PROM of the blank one-time programmable version is not tested or screened after assembly. To ensure proper operation after writing, the procedure shown in Figure 23 is recommended to verify programming.



Note : The screening temperature is far higher than the storage temperature Do not leave the microcomputer at 150℃ for longer than 100 hours

Fig. 23 Writing and testing of one-time programmable version

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	All voltages measured with reference to the V_{SS} pin, output transistors isolated	−0. 3 to 7. 0	V
V_I	Input voltage $P0_0$—$P0_7$, $P1_0$—$P1_7$, $P2_0$—$P2_7$, $P3_0$—$P3_7$, $P4_0$—$P4_7$, $P5_0$—$P5_7$, $P6_0$—$P6_7$, $P7_0$, $P7_1$		−0. 3 to V_{CC}+0. 3	V
V_I	Input voltage $\overline{RESET}$, X_{IN}		−0. 3 to V_{CC}+0. 3	V
V_I	Input voltage CNV_{SS}		−0. 3 to 13	V
V_O	Output voltage $P0_0$—$P0_7$, $P1_0$—$P1_7$, $P2_0$—$P2_7$, $P3_0$—$P3_7$, $P4_0$—$P4_7$, $P5_0$—$P5_7$, $P6_0$—$P6_7$, $P7_0$, $P7_1$, X_{OUT}		−0. 3 to V_{CC}+0. 3	V
Pd	Power dissipation	T_a = 25℃	1000(Note)	mW
Topr	Operating temperature		−20 to 85	℃
Tstg	Storage temperature		−40 to 125	℃

Note : 300mW in case of the flat package

RECOMMENDED OPERATING CONDITIONS (V_{CC} = 3. 0 to 5. 5V, T_a = −20 to 85℃, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage (f (X_{IN})≦2MHz)	3. 0	5. 0	5. 5	V
	Supply voltage (f (X_{IN})>2MHz)	4. 0	5. 0	5. 5	
V_{SS}	Supply voltage		0		V
V_{IH}	"H" input voltage $P0_0$—$P0_7$, $P1_0$—$P1_7$, $P2_0$—$P2_7$, $P3_0$—$P3_7$, $P4_0$—$P4_7$, $P5_0$—$P5_7$, $P6_0$—$P6_7$, $P7_0$, $P7_1$	0. 8V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage $\overline{RESET}$, X_{IN}, CNV_{SS}	0. 8V_{CC}		V_{CC}	V
V_{IL}	"L" input voltage $P0_0$—$P0_7$, $P1_0$—$P1_7$, $P2_0$—$P2_7$, $P3_0$—$P3_7$, $P4_0$—$P4_7$, $P5_0$—$P5_7$, $P6_0$—$P6_7$, $P7_0$, $P7_1$	0		0. 2V_{CC}	V
V_{IL}	"L" input voltage $\overline{RESET}$	0		0. 2V_{CC}	V
V_{IL}	"L" input voltage X_{IN}	0		0. 16V_{CC}	V
V_{IL}	"L" input voltage CNV_{SS}	0		0. 2V_{CC}	V
$\Sigma I_{OH(peak)}$	"H" total peak output current $P0_0$—$P0_7$, $P1_0$—$P1_7$, $P2_0$—$P2_7$, $P3_0$—$P3_7$ (Note 1)			−80	mA
$\Sigma I_{OH(peak)}$	"H" total peak output current $P4_0$—$P4_7$, $P5_0$—$P5_7$, $P6_0$—$P6_7$, $P7_0$, $P7_1$ (Note 1)			−80	mA
$\Sigma I_{OL(peak)}$	"L" total peak output current $P0_0$—$P0_7$, $P1_0$—$P1_7$, $P2_0$—$P2_7$, $P3_0$—$P3_7$ (Note 1)			80	mA
$\Sigma I_{OL(peak)}$	"L" total peak output current $P4_0$—$P4_7$, $P5_0$—$P5_7$, $P6_0$—$P6_7$, $P7_0$, $P7_1$ (Note 1)			80	mA
$\Sigma I_{OH(avg)}$	"H" total average output current $P0_0$—$P0_7$, $P1_0$—$P1_7$, $P2_0$—$P2_7$, $P3_0$—$P3_7$ (Note 1)			−40	mA
$\Sigma I_{OH(avg)}$	"H" total average output current $P4_0$—$P4_7$, $P5_0$—$P5_7$, $P6_0$—$P6_7$, $P7_0$, $P7_1$ (Note 1)			−40	mA
$\Sigma I_{OL(avg)}$	"L" total average output current $P0_0$—$P0_7$, $P1_0$—$P1_7$, $P2_0$—$P2_7$, $P3_0$—$P3_7$ (Note 1)			40	mA
$\Sigma I_{OL(avg)}$	"L" total average output current $P4_0$—$P4_7$, $P5_0$—$P5_7$, $P6_0$—$P6_7$, $P7_0$, $P7_1$ (Note 1)			40	mA
$I_{OH}(peak)$	"H" peak output current $P0_0$—$P0_7$, $P1_0$—$P1_7$, $P2_0$—$P2_7$, $P3_0$—$P3_7$, $P4_0$—$P4_7$, $P5_0$—$P5_7$, $P6_0$—$P6_7$, $P7_0$, $P7_1$ (Note 2)			−10	mA
$I_{OL}(peak)$	"L" peak output current $P0_0$—$P0_7$, $P1_0$—$P1_7$, $P2_0$—$P2_7$, $P3_0$—$P3_7$, $P4_0$—$P4_7$, $P5_0$—$P5_7$, $P6_0$—$P6_7$, $P7_0$, $P7_1$ (Note 2)			10	mA
$I_{OH}(avg)$	"H" average output current $P0_0$—$P0_7$, $P1_0$—$P1_7$, $P2_0$—$P2_7$, $P3_0$—$P3_7$, $P4_0$—$P4_7$, $P5_0$—$P5_7$, $P6_0$—$P6_7$, $P7_0$, $P7_1$ (Note 3)			−5	mA
$I_{OL}(avg)$	"L" average output current $P0_0$—$P0_7$, $P1_0$—$P1_7$, $P2_0$—$P2_7$, $P3_0$—$P3_7$, $P4_0$—$P4_7$, $P5_0$—$P5_7$, $P6_0$—$P6_7$, $P7_0$, $P7_1$ (Note 3)			5	mA
$f(X_{IN})$	Internal clock oscillation frequency (V_{CC}=4. 0~5. 5V)			8	MHz
	Internal clock oscillation frequency (V_{CC}=3. 0~5. 5V)			2	

Note 1 The total output current is the sum of all the currents flowing through all the applicable ports The total average current is an average value measured over 100ms The total peak current is the peak value of all the currents

2 The peak output current is the peak current flowing in each port

3 The average output current I_{OL} (avg), I_{OH} (avg) in an average value measured over 100ms

ELECTRICAL CHARACTERISTICS (V_{CC} = 4.0 to 5.5V, V_{SS} = 0V, T_a = −20 to 85℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{OH}	"H" output voltage $P0_0$—$P0_7$, $P1_0$—$P1_7$, $P2_0$—$P2_7$, $P3_0$—$P3_7$, $P4_0$—$P4_7$, $P5_0$—$P5_7$, $P6_0$—$P6_7$, $P7_0$, $P7_1$ (Note)	I_{OH}=−10mA V_{CC}=4.0~5.5V	V_{CC}−2.0			V
		I_{OH}=−10mA V_{CC}=3.0~5.5V	V_{CC}−1.0			
V_{OL}	"L" output voltage $P0_0$—$P0_7$, $P1_0$—$P1_7$, $P2_0$—$P2_7$, $P3_0$—$P3_7$, $P4_0$—$P4_7$, $P5_0$—$P5_7$, $P6_0$—$P6_7$, $P7_0$, $P7_1$	I_{OL}=10mA V_{CC}=4.0~5.5V			2.0	V
		I_{OL}=1.0mA V_{CC}=3.0~5.5V			1.0	
$V_{T+}-V_{T-}$	Hysteresis $CNTR_0$, $CNTR_1$, INT_0—INT_5			0.4		V
$V_{T+}-V_{T-}$	Hysteresis R_XD, S_{CLK}			0.5		V
$V_{T+}-V_{T-}$	Hysteresis $\overline{RESET}$			0.5		V
I_{IH}	"H" input current $P0_0$—$P0_7$, $P1_0$—$P1_7$, $P2_0$—$P2_7$, $P3_0$—$P3_7$, $P4_0$—$P4_7$, $P5_0$—$P5_7$, $P6_0$—$P6_7$, $P7_0$, $P7_1$	V_I=V_{CC}			5.0	μA
I_{IH}	"H" input current $\overline{RESET}$, CNV_{SS}	V_I=V_{CC}			5.0	μA
I_{IH}	"H" input current X_{IN}	V_I=V_{CC}		4		μA
I_{IL}	"L" input current $P0_0$—$P0_7$, $P1_0$—$P1_7$, $P2_0$—$P2_7$, $P3_0$—$P3_7$, $P4_0$—$P4_7$, $P5_0$—$P5_7$, $P6_0$—$P6_7$, $P7_0$, $P7_1$ $\overline{RESET}$, CNV_{SS}	V_I=V_{SS}			−5.0	μA
I_{IL}	"L" input current X_{IN}	V_I=V_{SS}		−4		μA
V_{RAM}	RAM hold voltage	With clock stopped	2.0		5.5	V
I_{CC}	Supply current	f(X_{IN})=8MHz, V_{CC}=5V		6.4	13	mA
		f(X_{IN})=5MHz, V_{CC}=5V		4	8	
		f(X_{IN})=2MHz, V_{CC}=3V		0.8	2.0	
		When WIT instruction is executed with f(X_{IN})=8MHz, V_{CC}=5V		1.5		
		When WIT instruction is executed with f(X_{IN})=5MHz, V_{CC}=5V		1		
		When WIT instruction is executed with f(X_{IN})=2MHz, V_{CC}=3V		0.2		
		When STP instruction is executed with clock stopped, output transistors isolated T_a=25℃		0.1	1	μA
		T_a=85℃			10	

Note : $P4_5$ is measured when the $P4_5/T_XD$ P-channel output disable bit of the UART control register (bit 4 of address $001B_{16}$) is "0"

TIMING REQUIREMENTS 1 (V_{CC}=4.0 to 5.5V, V_{SS}=0V, T_a= −20 to 85℃, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ.	Max	
$t_{W(\overline{RESET})}$	Reset input "L" pulse width	2			μs
$t_{C(X_{IN})}$	External clock input cycle time	125			ns
$t_{WH(X_{IN})}$	External clock input "H" pulse width	50			ns
$t_{WL(X_{IN})}$	External clock input "L" pulse width	50			ns
$t_{C(CNTR)}$	$CNTR_0$, $CNTR_1$ input cycle time	200			ns
$t_{WH(CNTR)}$	$CNTR_0$, $CNTR_1$ input "H" pulse width	80			ns
$t_{WH(INT)}$	INT_0 to INT_5 input "H" pulse width	80			ns
$t_{WL(CNTR)}$	$CNTR_0$, $CNTR_1$ input "L" pulse width	80			ns
$t_{WL(INT)}$	INT_0 to INT_5 input "L" pulse width	80			ns
$t_{C(S_{CLK})}$	Serial I/O clock input cycle time (Note)	800			ns
$t_{WH(S_{CLK})}$	Serial I/O clock input "H" pulse width (Note)	370			ns
$t_{WL(S_{CLK})}$	Serial I/O clock input "L" pulse width (Note)	370			ns
$t_{SU(R_XD-S_{CLK})}$	Serial I/O input set up time	220			ns
$t_{h(S_{CLK}-R_XD)}$	Serial I/O input hold time	100			ns

Note : When $f(X_{IN})$=5MHz and bit 6 of address $001A_{16}$ is "1" Divide this value by four when $f(X_{IN})$=5MHz and bit 6 of address $001A_{16}$ is "0"

TIMING REQUIREMENTS 2 (V_{CC}=3.0 to 5.5V, V_{SS}=0V, T_a= −20 to 85℃, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
$t_{W(\overline{RESET})}$	Reset input "L" pulse width	2			μs
$t_{C(X_{IN})}$	External clock input cycle time	500			ns
$t_{WH(X_{IN})}$	External clock input "H" pulse width	200			ns
$t_{WL(X_{IN})}$	External clock input "L" pulse width	200			ns
$t_{C(CNTR)}$	$CNTR_0$, $CNTR_1$ input cycle time	500			ns
$t_{WH(CNTR)}$	$CNTR_0$, $CNTR_1$ input "H" pulse width	230			ns
$t_{WH(INT)}$	INT_0 to INT_5 input "H" pulse width	230			ns
$t_{WL(CNTR)}$	$CNTR_0$, $CNTR_1$ input "L" pulse width	230			ns
$t_{WL(INT)}$	INT_0 to INT_5 input "L" pulse width	230			ns
$t_{C(S_{CLK})}$	Serial I/O clock input cycle time (Note)	2000			ns
$t_{WH(S_{CLK})}$	Serial I/O clock input "H" pulse width (Note)	950			ns
$t_{WL(S_{CLK})}$	Serial I/O clock input "L" pulse width (Note)	950			ns
$t_{SU(R_XD-S_{CLK})}$	Serial I/O input set up time	400			ns
$t_{h(S_{CLK}-R_XD)}$	Serial I/O input hold time	200			ns

Note : When $f(X_{IN})$=5MHz and bit 6 of address $001A_{16}$ is "1" Divide this value by four when $f(X_{IN})$=5MHz and bit 6 of address $001A_{16}$ is "0"

SWITCHING CHARACTERISTICS 1 (V_{CC} = 4.0 to 5.5V, V_{SS} = 0V, T_a = −20 to 85℃, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
$t_{WH(S_{CLK})}$	Serial I/O clock output "H" pulse width	$t_{C(S_{CLK})}/2-30$			ns
$t_{WL(S_{CLK})}$	Serial I/O clock output "L" pulse width	$t_{C(S_{CLK})}/2-30$			ns
$t_{d(S_{CLK}-T_XD)}$	Serial I/O output delay time (Note 1)			140	ns
$t_{v(S_{CLK}-T_XD)}$	Serial I/O output valid time (Note 1)	−30			ns
$t_{r(S_{CLK})}$	Serial I/O clock output rise time			30	ns
$t_{f(S_{CLK})}$	Serial I/O clock output fall time			30	ns
$t_{r(CMOS)}$	CMOS output rise time (Note 2)		10	30	ns
$t_{f(CMOS)}$	CMOS output fall time (Note 2)		10	30	ns

Note 1 : When the $P4_5/T_XD$ P-channel output disable bit of the UART control register (bit 4 of address $001B_{16}$) is "0"
2 : X_{OUT} pin excluded

SWITCHING CHARACTERISTICS 2 (V_{CC} = 3.0 to 5.5V, V_{SS} = 0V, T_a = −20 to 85℃, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
$t_{WH(S_{CLK})}$	Serial I/O clock output "H" pulse width	$t_{C(S_{CLK})}/2-50$			ns
$t_{WL(S_{CLK})}$	Serial I/O clock output "L" pulse width	$t_{C(S_{CLK})}/2-50$			ns
$t_{d(S_{CLK}-T_XD)}$	Serial I/O output delay time (Note 1)			350	ns
$t_{v(S_{CLK}-T_XD)}$	Serial I/O output valid time (Note 1)	−30			ns
$t_{r(S_{CLK})}$	Serial I/O clock output rise time			50	ns
$t_{f(S_{CLK})}$	Serial I/O clock output fall time			50	ns
$t_{r(CMOS)}$	CMOS output rise time (Note 2)		20	50	ns
$t_{f(CMOS)}$	CMOS output fall time (Note 2)		20	50	ns

Note 1 : When the $P4_5/T_XD$ P-channel output disable bit of the UART control register (bit 4 of address $001B_{16}$) is "0"
2 : X_{OUT} pin excluded

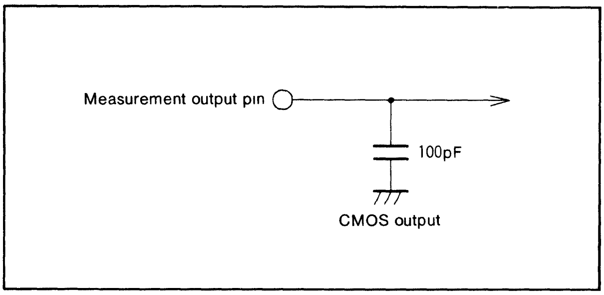


Fig. 24 Circuit for measuring output switching characteristics (1)

TIMING REQUIREMENTS IN MEMORY EXPANSION MODE AND MICROPROCESSOR MODE

(V_{CC} = 4.0 to 5.5V, V_{SS} = 0V, T_a = −20 to 85℃, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
$t_{su(\overline{ONW}-\phi)}$	$\overline{\text{ONW}}$ input set up time	−20			ns
$t_{h(\phi-\overline{ONW})}$	$\overline{\text{ONW}}$ input hold time	−20			ns
$t_{su(DB-\phi)}$	Data bus set up time	60			ns
$t_{h(\phi-DB)}$	Data bus hold time	0			ns

SWITCHING CHARACTERISTICS IN MEMORY EXPANSION MODE AND MICROPROCESSOR MODE

(V_{CC} = 4.0 to 5.5V, V_{SS} = 0V, T_a = −20 to 85℃, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
$t_{c(\phi)}$	ϕ clock cycle time		$2\text{X}t_{c(X_{IN})}$		ns
$t_{WH(\phi)}$	ϕ clock "H" pulse width	$t_{c(X_{IN})}-10$			ns
$t_{WL(\phi)}$	ϕ clock "L" pulse width	$t_{c(X_{IN})}-10$			ns
$t_{d(\phi-AH)}$	AD_{15} to AD_8 delay time		20	40	ns
$t_{v(\phi-AH)}$	AD_{15} to AD_8 valid time	6	10		ns
$t_{d(\phi-AL)}$	AD_7 to AD_0 delay time		25	45	ns
$t_{v(\phi-AL)}$	AD_7 to AD_0 valid time	6	10		ns
$t_{d(\phi-SYNC)}$	SYNC delay time		20		ns
$t_{v(\phi-SYNC)}$	SYNC valid time		10		ns
$t_{d(\phi-\overline{WR})}$	$\overline{\text{RD}}$ and $\overline{\text{WR}}$ delay time		10	20	ns
$t_{v(\phi-\overline{WR})}$	$\overline{\text{RD}}$ and $\overline{\text{WR}}$ valid time	3	5	10	ns
$t_{d(\phi-DB)}$	Data bus delay time		20	70	ns
$t_{v(\phi-DB)}$	Data bus valid time	15			ns
$t_{d(\overline{RESET}-\overline{RESET_{OUT}})}$	$\overline{\text{RESET}_{OUT}}$ output delay time (Note)			200	ns
$t_{v(\phi-\overline{RESET})}$	$\overline{\text{RESET}_{OUT}}$ output valid time (Note)	0		200	ns

Note : The $\overline{\text{RESET}_{OUT}}$ output goes "H" in sync with the rise of the ϕ clock that is anywhere between about 1 cycle and 19 cycles after the RESET input goes "H"

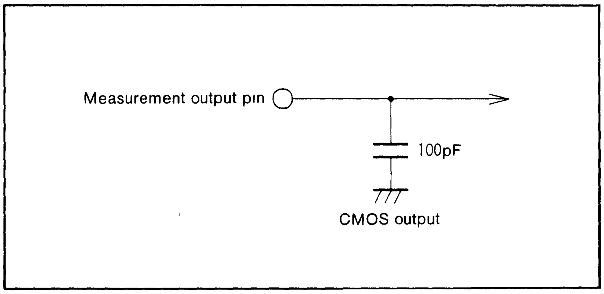
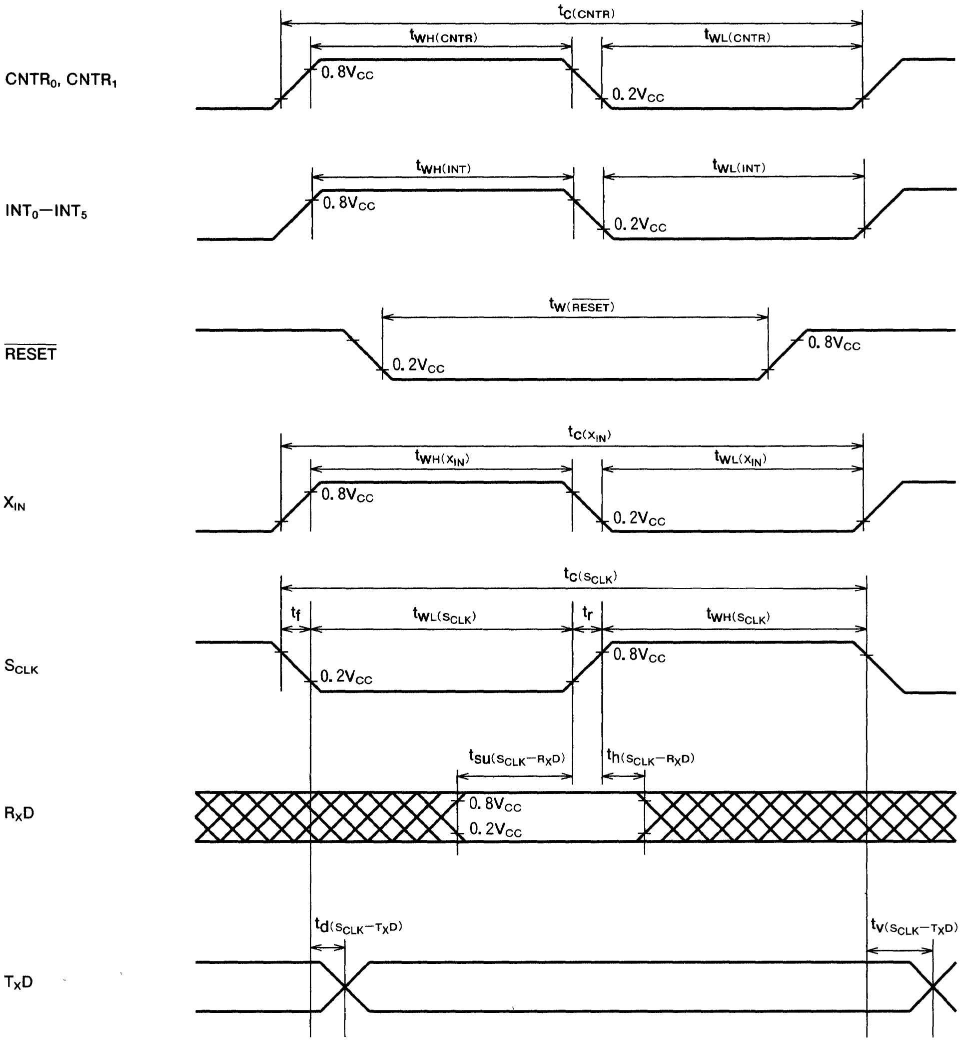


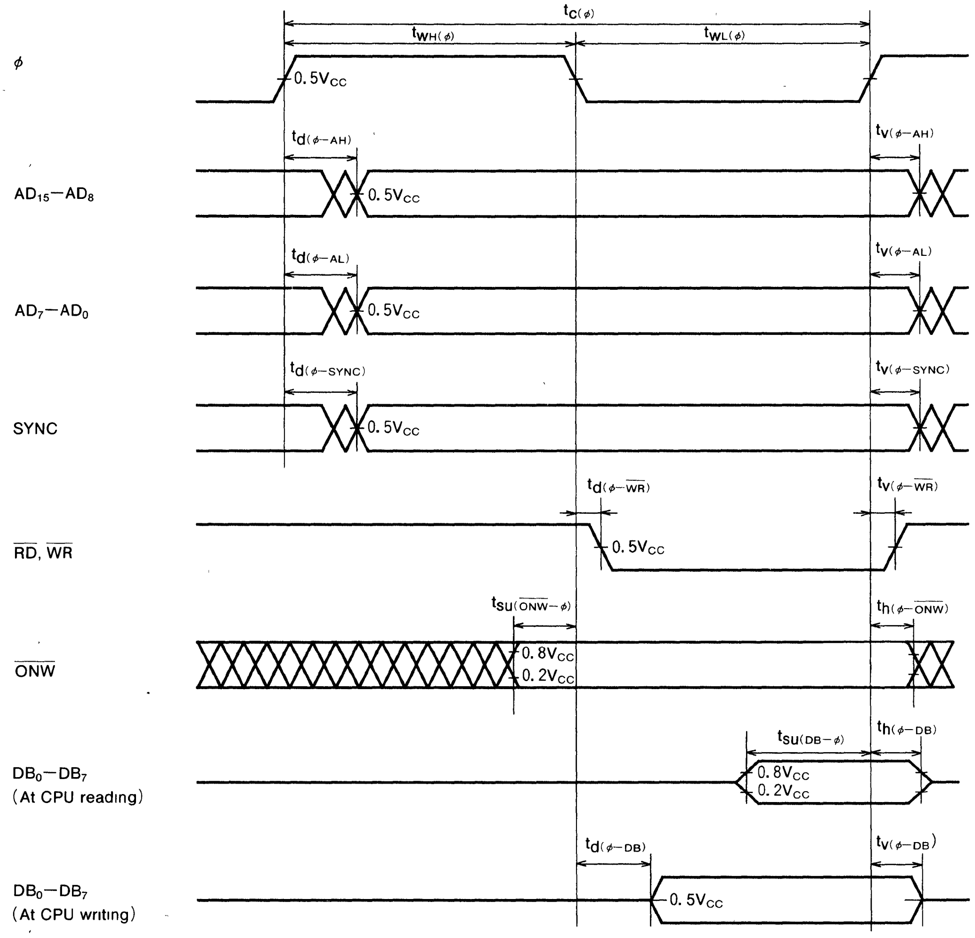
Fig. 25 Circuit for measuring output switching characteristics (2)

TIMING DIAGRAM

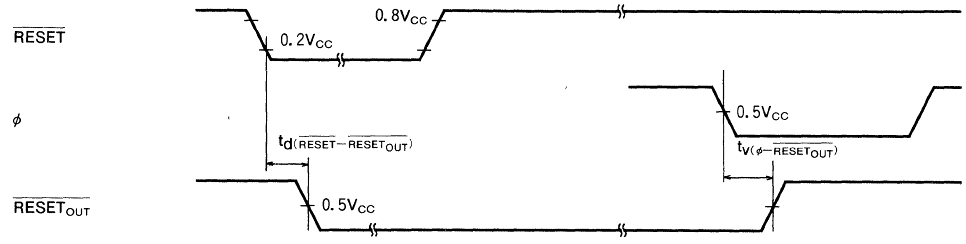
(1) Timing diagram



(2) Timing diagram in memory expansion mode and microprocessor mode



(3) Timing diagram in microprocessor mode



MITSUBISHI MICROCOMPUTERS

M3806x Group

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

DESCRIPTION

The M3806x group is made up of 8-bit microcomputers based on the MELPS 740 core.

The M3806x group is designed for controlling systems that require analog signal processing and include two serial I/O functions, A-D converters, and D-A converters.

The various microcomputers in the M3806x group include variations of internal memory size and packaging. For details, see the section on part numbering.

For details on availability of microcomputers in the M3806x group, see the section on group expansion.

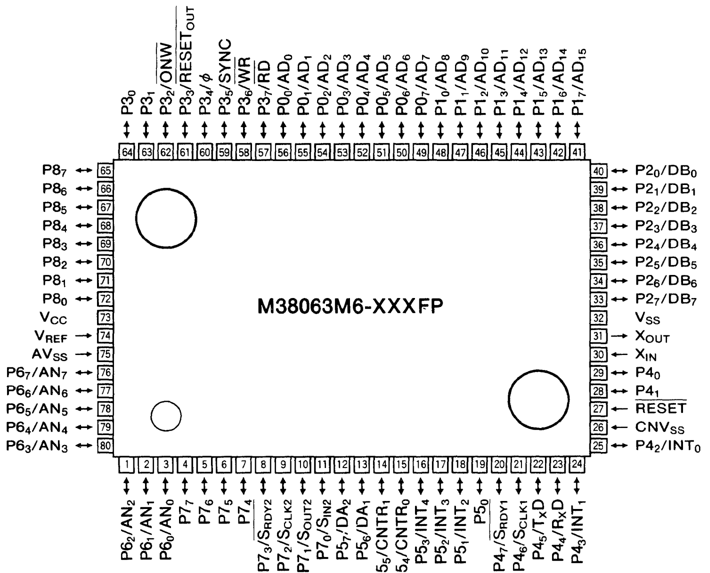
FEATURES

- Basic machine-language instructions ········ 71
- Instruction execution time ········ 0.5μs
  (shortest instruction at 8MHz oscillation frequency)
- Memory size
  ROM ········ 4K to 32K bytes
  RAM ········ 192 to 1024 bytes
- Programmable input/output ports ········ 72
- Interrupts ········ 16 sources, 16 vectors
- Timers ········ 8 bit×4
- Serial I/O1 ········ 8-bit×1(UART or Clock-synchronized)
- Serial I/O2 ········ 8-bit×1(Clock-synchronized)
- A-D converter ········ 8-bit×8 channels
- D-A converter ········ 8-bit×2 channels
- Clock generation circuit ········ Internal feedback amplifier
  (connect to external ceramic resonator or quartz crystal)
- Supply voltage ········ 3.0 to 5.5V
- Low power dissipation ········ 32mW
- Memory expansion possible
- Operating temperature range ········ −20 to 85°C

APPLICATIONS

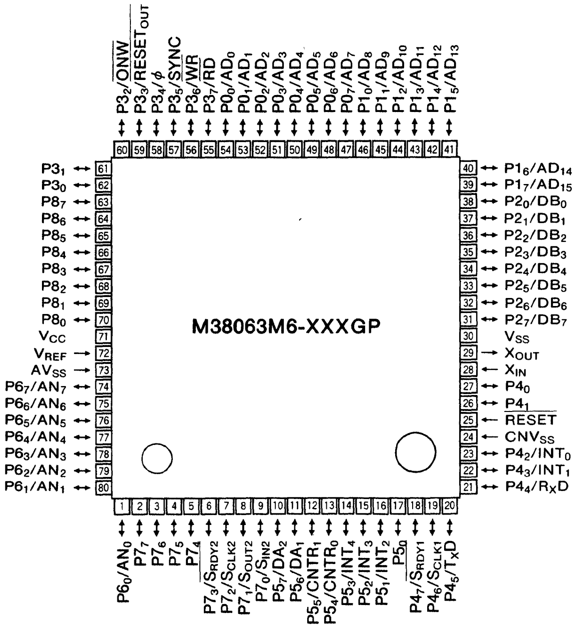
Office automation, VCRs, tuners, musical instruments, cameras, air conditioners, etc.

PIN CONFIGURATION (TOP VIEW)



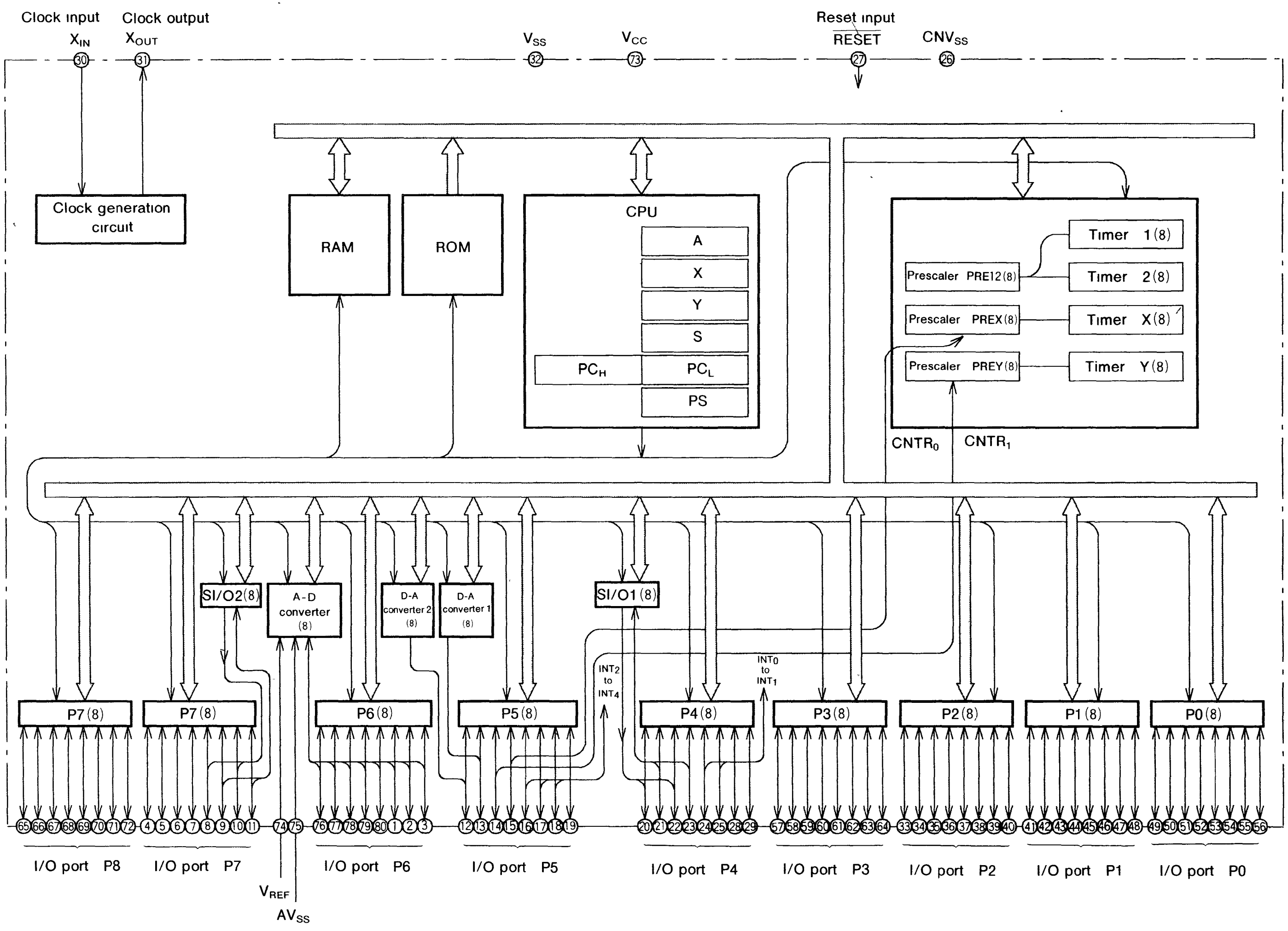
Package type : 80P6N
80-pin plastic-molded QFP

PIN CONFIGURATION (TOP VIEW)



Package type : 80P6S
80-pin plastic-molded QFP

FUNCTIONAL BLOCK DIAGRAM (Package : 80P6N)



PIN DESCRIPTION

Pin	Name	Function	Alternate Function
V_{CC}	Power supply	Power supply inputs 4 0 to 5 5V to V_{CC}, and 0V to V_{SS}.	
V_{SS}			
CNV_{SS}	CNV_{SS}	This pin controls the operation mode of the chip Normally connected to V_{SS} If this pin is connected to V_{CC}, the internal ROM is inhibited and external memory is accessed	
V_{REF}	Analog reference voltage	Reference voltage input pin for A-D and D-A converters	
AV_{SS}	Analog power supply	GND input pin for A-D and D-A converter Keep at the same potential as V_{SS}	
$\overline{RESET}$	Reset input	To reset the microcomputer, this pin should be kept at an "L" level for more than 2μs under normal operating conditions	
X_{IN}	Clock input	Input and output signals for the internal clock generation circuit Connect a ceramic resonator or quartz crystal between the X_{IN} and X_{OUT} pins to set the oscillation frequency If an external clock is used, connect the clock source to the X_{IN} pin and leave the X_{OUT} pin open	
X_{OUT}	Clock output		
$P0_0$—$P0_7$	I/O port P0	An 8 bit CMOS I/O port An I/O direction register allows each pin to be individually programmed as either input or output At reset this port is set to input mode In modes other than single-chip, these pins are used as address, data, and control bus I/O pins	
$P1_0$—$P1_7$	I/O port P1		
$P2_0$—$P2_7$	I/O port P2		
$P3_0$—$P3_7$	I/O port P3		
$P4_0$, $P4_1$	I/O port P4	An 8-bit CMOS I/O port with the same function as port P0	
$P4_2/INT_0$, $P4_3/INT_1$			External interrupt input pin
$P4_4/R_XD$, $P4_5/T_XD$, $P4_6/S_{CLK1}$, $P4_7/\overline{S_{RDY1}}$			Serial I/O1 I/O pins
$P5_0$	I/O port P5	An 8-bit CMOS I/O port with the same function as port P0	
$P5_1/INT_2$— $P5_3/INT_4$			External interrupt input pin
$P5_4/CNTR_0$, $P5_5/CNTR_1$			Timer X and Timer Y I/O pins
$P5_6/DA_1$, $P5_7/DA_2$			D-A converter output pins
$P6_0/AN_0$— $P6_7/AN_7$	I/O port P6	An 8-bit CMOS I/O port with the same function as port P0	A-D converter input pins
$P7_0/S_{IN2}$, $P7_1/S_{OUT2}$, $P7_2/S_{CLK2}$, $P7_3/\overline{S_{RDY2}}$	I/O port P7	An 8-bit I/O port with the same function as port P0 The output structure of this port is N-channel open drain, and the input levels are CMOS compatible	Serial I/O2 I/O pins
$P7_4$—$P7_7$			
$P8_0$—$P8_7$	I/O port P8	An 8-bit CMOS I/O port with the same function as port P0	

PART NUMBERING

Product name M3806 3 M 6 - XXX FP

Package type
- FP 80P6N package
- GP 80P6S package
- FS 80D0 package

ROM number
- Omitted in some types

ROM/PROM size
- 1 4096 bytes
- 2 8192 bytes
- 3 12288 bytes
- 4 16384 bytes
- 5 20480 bytes
- 6 24576 bytes
- 7 28672 bytes
- 8 32768 bytes

The first 128 bytes and the last two bytes of ROM are reserved areas, they can not be used

Memory type
- M Mask ROM version
- E EPROM or one-time programmable version

RAM size
- 0 192 bytes
- 1 256 bytes
- 2 384 bytes
- 3 512 bytes
- 4 640 bytes
- 5 768 bytes
- 6 896 bytes
- 7 1024 bytes

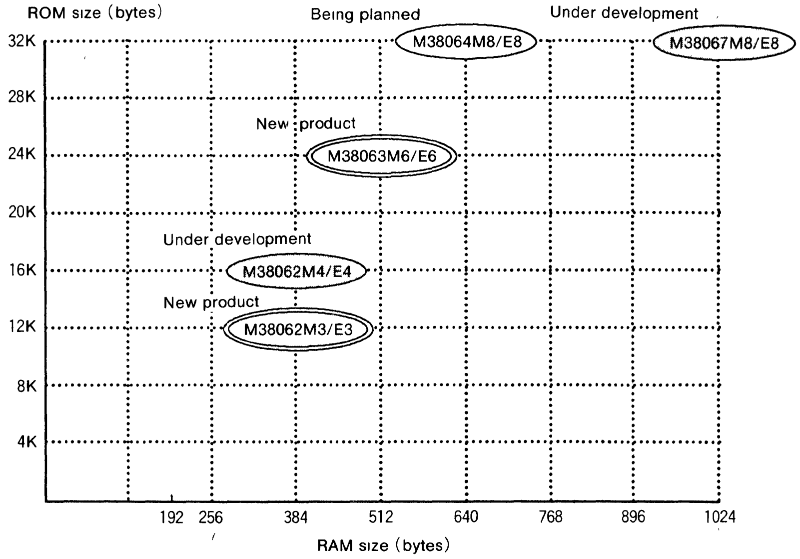
GROUP EXPANSION

Mitsubishi plans to expand the M3806x group as follows:

(1) Support for mask ROM, one-time programmable, and EPROM versions
ROM/PROM capacity ·····················12K to 32K bytes
RAM capacity ·································384 to 1024 bytes

(2) Packages
80P6N ···················· 0.8mm-pitch plastic molded QFP
80P6S ···················· 0.65mm-pitch plastic molded QFP
80D0 ······························ 0.8mm-pitch ceramic LCC

Memory expansion plan



The development schedule and other details of products under development may be revised without notice
Currently supported products are listed below

As of March 1992

Product name	(P) ROM size (bytes)	RAM size (bytes)	Package	Remarks
M38062M3-XXXFP	12K	384	80P6N	Mask ROM version
M38062E3-XXXFP				One-time programmable version
M38062E3FP				One-time programmable version (blank)
M38062M3-XXXGP			80P6S	Mask ROM version
M38062E3-XXXGP				One-time programmable version
M38062E3GP				One-time programmable version (blank)
M38062E3FS			80D0	EPROM version
M38062M6-XXXFP	24K	512	80P6N	Mask ROM version
M38062E6-XXXFP				One-time programmable version
M38063E6FP				One-time programmable version (blank)
M38063M6-XXXGP			80P6S	Mask ROM version
M38063E6-XXXGP				One-time programmable version
M38063E6GP				One-time programmable version (blank)
M38063E6FS			80D0	EPROM version

FUNCTIONAL DESCRIPTION

Central Processing Unit (CPU)

Microcomputers of the M3806x group use the standard MELPS 740 instruction set. Refer to the table of MELPS 740 addressing modes and machine instructions or the MELPS 740 Software Manual for details on the instruction set.

Machine-resident MELPS 740 instructions are as follows:
The FST and SLW instructions are not available for use.
The STP, WIT, MUL, and DIV instructions can be used.

CPU Mode Register

The CPU mode register (address $003B_{16}$) contains processor mode bits that specify the operating mode of the chip. The CPU mode register also contains the stack page select bit.

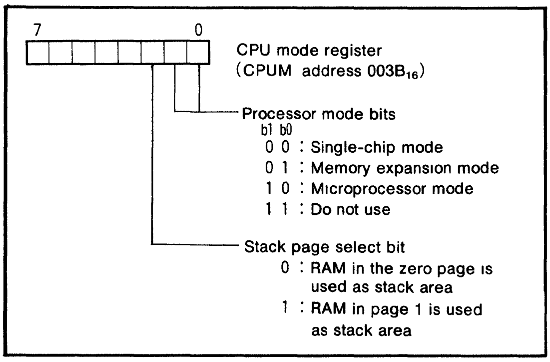


Fig. 1 Structure of CPU mode register

MEMORY

- **Special Function Register (SFR) Area**
  The Special Function Register area contains registers which control functions such as I/O ports and timers, and is located in the zero page area.
- **RAM**
  RAM is used for data storage as well for stack area.
- **ROM**
  The first 128 bytes and the last two bytes of ROM are reserved for device testing and the rest is user area for storing programs.
- **Interrupt Vector Area**
  The interrupt vector area contains reset and interrupt vectors.
- **Zero Page**
  The 256 bytes from addresses 0000_{16} to $00FF_{16}$ are called the zero page area. The internal RAM and the special function registers (SFR) are allocated to this area.
  The zero page addressing mode can be used to specify memory and register addresses in the zero page area. This dedicated zero page addressing mode enables access to this area with only 2 bytes.
- **Special Page**
  The 256 bytes from addresses $FF00_{16}$ to $FFFF_{16}$ are called the special page area. The special page addressing mode can be used to specify memory addresses in the special page area. This dedicated special page addressing mode enables access to this area with only 2 bytes.

RAM area

RAM capacity (bytes)	Address $XXXX_{16}$
192	$00FF_{16}$
256	$013F_{16}$
384	$01BF_{16}$
512	$023F_{16}$
640	$02BF_{16}$
768	$033F_{16}$
896	$03BF_{16}$
1024	$043F_{16}$

ROM area

ROM capacity (bytes)	Address $YYYY_{16}$	Address $ZZZZ_{16}$
4096	$F000_{16}$	$F080_{16}$
8192	$E000_{16}$	$E080_{16}$
12288	$D000_{16}$	$D080_{16}$
16384	$C000_{16}$	$C080_{16}$
20480	$B000_{16}$	$B080_{16}$
24576	$A000_{16}$	$A080_{16}$
28672	9000_{16}	9080_{16}
32768	8000_{16}	8080_{16}

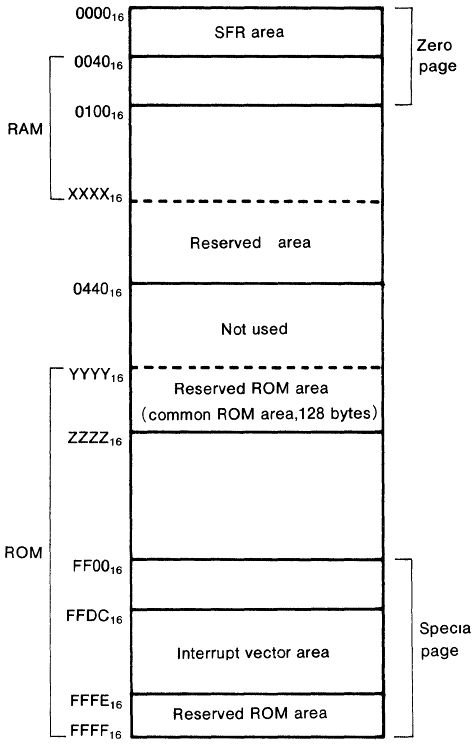


Fig. 2 Memory map diagram

0000_{16}	Port P0 (P0)	0020_{16}	Prescaler 12 (PRE12)
0001_{16}	Port P0 direction register (P0D)	0021_{16}	Timer 1 (T1)
0002_{16}	Port P1 (P1)	0022_{16}	Timer 2 (T2)
0003_{16}	Port P1 direction register (P1D)	0023_{16}	Timer XY mode register (TM)
0004_{16}	Port P2 (P2)	0024_{16}	Prescaler X (PREX)
0005_{16}	Port P2 direction register (P2D)	0025_{16}	Timer X (TX)
0006_{16}	Port P3 (P3)	0026_{16}	Prescaler Y (PREY)
0007_{16}	Port P3 direction register (P3D)	0027_{16}	Timer Y (TY)
0008_{16}	Port P4 (P4)	0028_{16}	
0009_{16}	Port P4 direction register (P4D)	0029_{16}	
$000A_{16}$	Port P5 (P5)	$002A_{16}$	
$000B_{16}$	Port P5 direction register (P5D)	$002B_{16}$	
$000C_{16}$	Port P6 (P6)	$002C_{16}$	
$000D_{16}$	Port P6 direction register (P6D)	$002D_{16}$	
$000E_{16}$	Port P7 (P7)	$002E_{16}$	
$000F_{16}$	Port P7 direction register (P7D)	$002F_{16}$	
0010_{16}	Port P8 (P8)	0030_{16}	
0011_{16}	Port P8 direction register (P8D)	0031_{16}	
0012_{16}		0032_{16}	
0013_{16}		0033_{16}	
0014_{16}		0034_{16}	AD/DA control register (ADCON)
0015_{16}		0035_{16}	A-D conversion register (AD)
0016_{16}		0036_{16}	D-A1 conversion register (DA1)
0017_{16}		0037_{16}	D-A2 conversion register (DA2)
0018_{16}	Transmit/receive buffer 1 (TB1/RB1)	0038_{16}	
0019_{16}	Serial I/O1 status register (SIO1STS)	0039_{16}	
$001A_{16}$	Serial I/O1 control register (SIO1CON)	$003A_{16}$	Interrupt edge selection register (INTEDGE)
$001B_{16}$	UART control register (UARTCON)	$003B_{16}$	CPU mode register (CPUM)
$001C_{16}$	Baud rate generator (BRG)	$003C_{16}$	Interrupt request register 1 (IREQ1)
$001D_{16}$	Serial I/O2 control register (SIO2CON)	$003D_{16}$	Interrupt request register 2 (IREQ2)
$001E_{16}$		$003E_{16}$	Interrupt control register 1 (ICON1)
$001F_{16}$	Serial I/O2 register (SIO2)	$003F_{16}$	Interrupt control register 2 (ICON2)

Fig. 3 Memory map of special function register (SFR)

I/O PORTS

Direction Registers

The M3806x group microprocessors have 72 programmable I/O pins arranged in nine I/O ports (ports P0 to P8). The I/O ports have direction registers which determine the input/output direction of each individual pin. Each bit in a direction register corresponds to one pin, each pin can be set to be input or output. When "0" is written to the bit corresponding to a pin, that pin becomes an input pin. When "1" is written to that bit, that pin becomes an output pin.

If data is read from a pin which is set for output, the value of the port output latch is read, not the value of the pin itself. Pins set to input are floating. If a pin set to input is written to, only the port output latch is written to and the pin remains floating.

Pin	Name	Input/Output	I/O Format	Non-Port Function	Related SFRs	Ref No
$P0_0$—$P0_7$	Port P0	Input/output, individual bits	CMOS 3-state output CMOS level input	Address lower-byte output	CPU mode register	(1)
$P1_0$—$P1_7$	Port P1	Input/output, individual bits	CMOS 3-state output CMOS level input	Address upper-byte output	CPU mode register	
$P2_0$—$P2_7$	Port P2	Input/output, individual bits	CMOS 3-state output CMOS level input	Data bus I/O	CPU mode register	
$P3_0$—$P3_7$	Port P3	Input/output, individual bits	CMOS 3-state output CMOS level input	Control signal I/O	CPU mode register	
$P4_0$, $P4_1$	Port P4	Input/output, individual bits	CMOS 3-state output CMOS level input			
$P4_2/INT_0$, $P4_3/INT_1$				External interrupt input	Interrupt edge selection register	(2)
$P4_4/R_XD$,				Serial I/O1 function I/O	Serial I/O control register UART control register	(3)
$P4_5/T_XD$,						(4)
$P4_6/S_{CLK1}$,						(5)
$P4_7/\overline{S_{RDY1}}$						(6)
$P5_0$	Port P5	Input/output, individual bits	CMOS 3-state output CMOS level input			(1)
$P5_1/INT_2$, $P5_2/INT_3$, $P5_3/INT_4$				External interrupt input	Interrupt edge selection register	(2)
$P5_4/CNTR_0$, $P5_5/CNTR_1$				Timer XY function I/O		(7)
$P5_6/DA_1$, $P5_7/DA_2$				D-A converter output	AD/DA control register	(8)
$P6_0/AN_0$— $P6_7/AN_7$	Port P6	Input/output, individual bits	CMOS 3-state output CMOS level input	A-D converter input		(9)
$P7_0/S_{IN2}$,	Port P7	Input/output, individual bits	N-channel open-drain output CMOS level input	Serial I/O2 function I/O	Serial I/O2 control register	(10)
$P7_1/S_{OUT2}$,						(11)
$P7_2/S_{CLK2}$,						(12)
$P7_3/\overline{S_{RDY2}}$						(13)
$P7_4$—$P7_7$						(14)
$P8_0$—$P8_7$	Port P8	Input/output, individual bits	CMOS 3-state output CMOS level input			(1)

Note : For details of the functions of ports P0 to P3 in modes other than single-chip mode, and how to use double-function ports as function I/O ports, see the applicable sections.

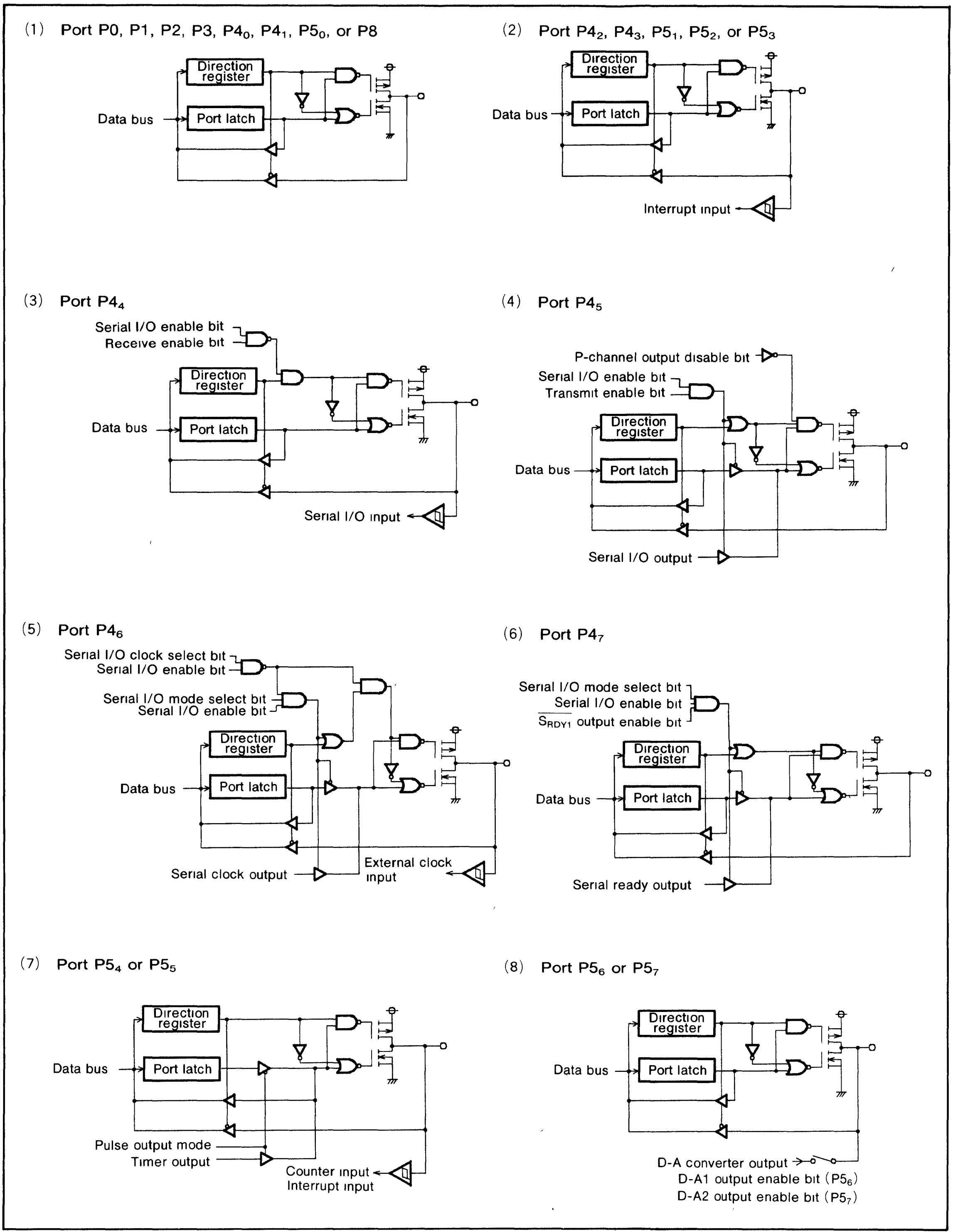
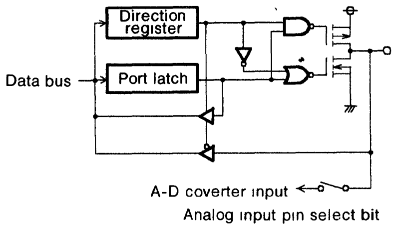
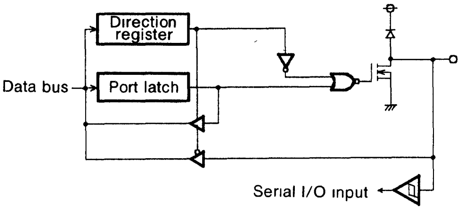


Fig. 4 Port block diagram (single-chip mode) (1)

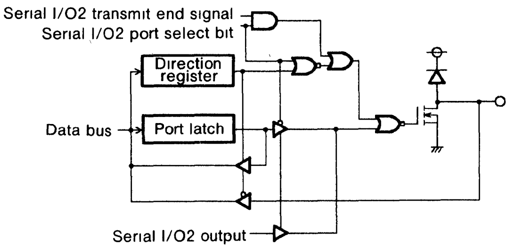
(9) Port P6



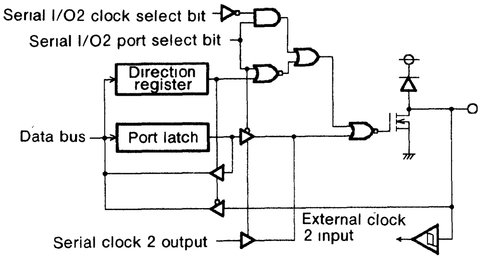
(10) Port $P7_0$



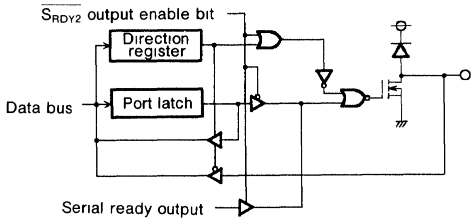
(11) Port $P7_1$



(12) Port $P7_2$



(13) Port $P7_3$



(14) Port $P7_4$ to Port $P7_7$

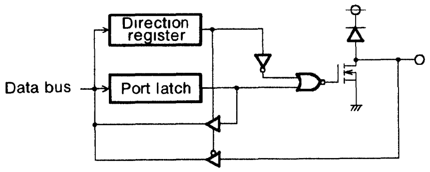


Fig. 5 Port block diagram (single-chip mode) (2)

INTERRUPTS

A total of 16 sources can generate interrupts: 7 external, 8 internal, and 1 software.

- **Interrupt Control**

Each interrupt is controlled by an interrupt request bit, an interrupt enable bit, and the interrupt disable flag-except for the software interrupt set by the BRK instruction. An interrupt is generated if the corresponding interrupt request and enable bits are "1" and the interrupt disable flag is "0".

Interrupt enable bits can be set or cleared by software.

Interrupt request bits can be cleared by software, but cannot be set by software.

The I flag disables all interrupts except for the BRK instruction interrupt.

- **Interrupt Operation**

When an interrupt is received, the program counter and processor status register are automatically pushed onto the stack. The interrupt disable flag is set to inhibit other interrupts from interfering. The corresponding interrupt request bit is cleared and the interrupt jump destination address is read from the vector table into the program counter.

- **Notes on Use**

When the active edge of an external interrupt (INT_0 to INT_4, $CNTR_0$, or $CNTR_1$) is changed, the corresponding interrupt request bit may also be set. To insure proper operation when selecting the active edge, disable interrupts before setting the interrupt edge selection.

Table 1 Interrupt vector addresses and priorities

Interrupt cause	Priority	Vector address (Note 1)		Interrupt request generation conditions	Remarks
		High	Low		
Reset (Note 2)	1	$FFFD_{16}$	$FFFC_{16}$	At reset	Non-maskable
INT_0	2	$FFFB_{16}$	$FFFA_{16}$	At detection of either rising or falling edge of INT_0 input	External interrupt (active edge selectable)
INT_1	3	$FFF9_{16}$	$FFF8_{16}$	At detection of either rising or falling edge of INT_1 input	External interrupt (active edge selectable)
Serial I/O1 reception	4	$FFF7_{16}$	$FFF6_{16}$	At end of serial I/O1 data reception	Valid when serial I/O1 is selected
Serial I/O1 transmission	5	$FFF5_{16}$	$FFF4_{16}$	At end of serial I/O1 transfer shift or when transmission buffer is empty	Valid when serial I/O1 is selected
Timer X	6	$FFF3_{16}$	$FFF2_{16}$	At timer X overflow	
Timer Y	7	$FFF1_{16}$	$FFF0_{16}$	At timer Y overflow	
Timer 1	8	$FFEF_{16}$	$FFEE_{16}$	At timer 1 overflow	STP release timer overflow
Timer 2	9	$FFED_{16}$	$FFEC_{16}$	At timer 2 overflow	
$CNTR_0$	10	$FFEB_{16}$	$FFEA_{16}$	At detection of either rising or falling edge of $CNTR_0$ input	External interrupt (active edge selectable)
$CNTR_1$	11	$FFE9_{16}$	$FFE8_{16}$	At detection of either rising or falling edge of $CNTR_1$ input	External interrupt (active edge selectable)
Serial I/O2	12	$FFE7_{16}$	$FFE6_{16}$	At end of serial I/O2 data transfer	Valid when serial I/O2 is selected
INT_2	13	$FFE5_{16}$	$FFE4_{16}$	At detection of either rising or falling edge of INT_2 input	External interrupt (active edge selectable)
INT_3	14	$FFE3_{16}$	$FFE2_{16}$	At detection of either rising or falling edge of INT_3 input	External interrupt (active edge selectable)
INT_4	15	$FFE1_{16}$	$FFE0_{16}$	At detection of either rising or falling edge of INT_4 input	External interrupt (active edge selectable)
A-D converter	16	$FFDF_{16}$	$FFDE_{16}$	At end of A-D conversion	
BRK instruction	17	$FFDD_{16}$	$FFDC_{16}$	At BRK instruction execution	Non-maskable software interrupt

Note 1 : Vector addresses contain interrupt jump destination addresses
2 : Reset function in the same way as an interrupt with the highest priority

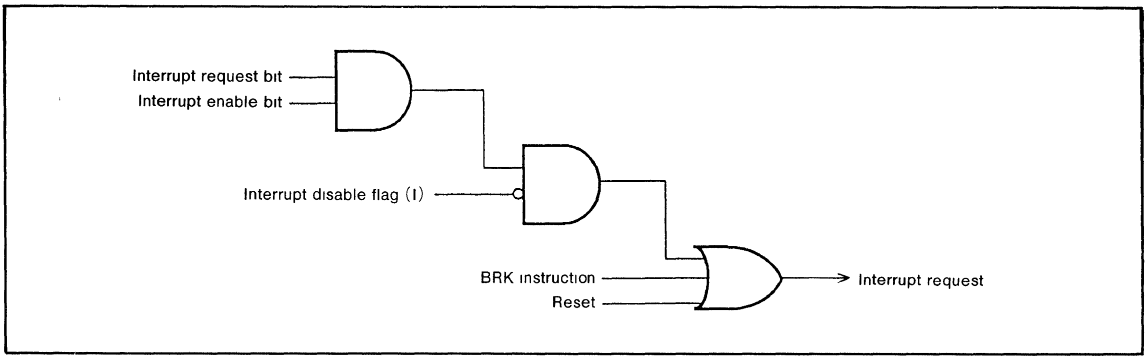


Fig. 6 Interrupt control

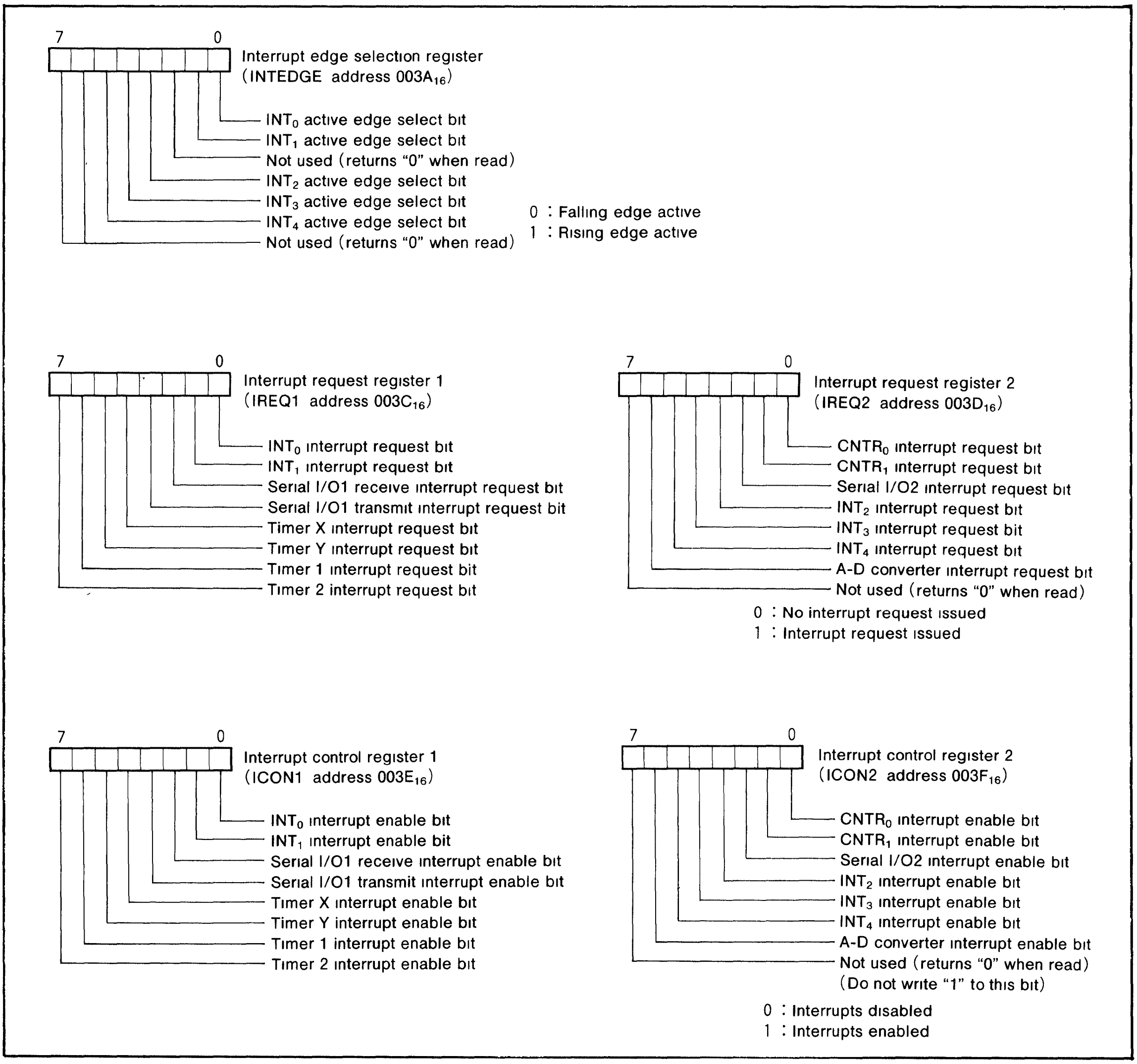


Fig. 7 Structure of interrupt-related registers

TIMERS

Microcomputers of the M3806x group have 4 timers: timer X, timer Y, timer 1, and timer 2.

The timers count down. Once a timer reaches 00_{16}, the next count pulse reloads the contents of the corresponding timer latch into the timer, and sets the corresponding interrupt request bit to 1.

The divide ratio of each timer or prescaler is given by $1/(n+1)$, where n is the value in the corresponding timer or prescaler latch.

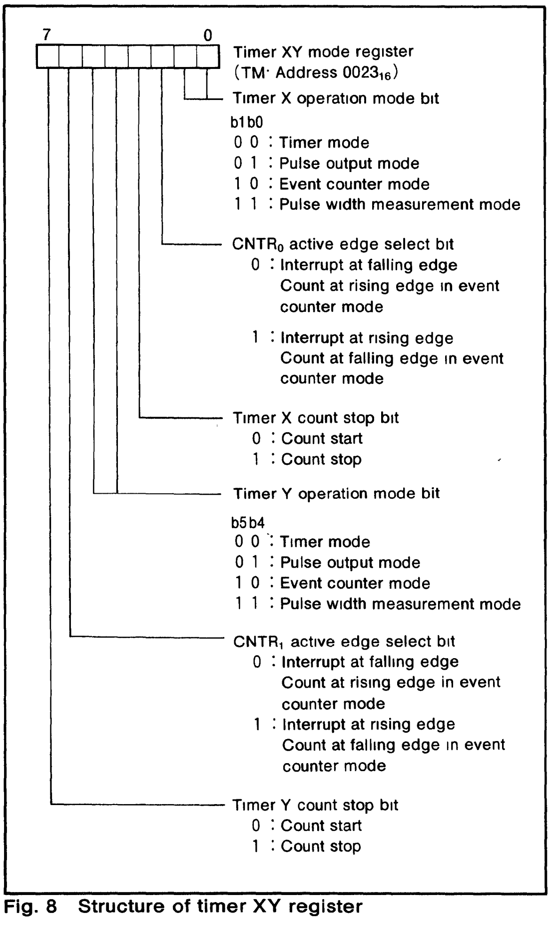


Fig. 8 Structure of timer XY register

Timer 1 and Timer 2

The count source of prescaler 12 is the oscillation frequency divided by 16. The output of prescaler 12 is counted by timer 1 and timer 2, and a timer overflow sets the interrupt request bit.

Timer X and Timer Y

Timer X and Timer Y can each be set to operate in one of four operating modes by setting the timer XY mode register.

1. Timer Mode
   In timer mode, the timer counts a signal that is the oscillation frequency divided by 16.
2. Pulse Output Mode
   Timer X (or timer Y) counts a signal which is the oscillation frequency divided by 16. Whenever the contents of the timer reach "0", the signal output from the $CNTR_0$ (or $CNTR_1$) pin is inverted. If the $CNTR_0$ (or $CNTR_1$) active edge select bit is "0", output begins at "H". If it is "1", output starts at "L" When using a timer in this mode, set the corresponding port $P5_4$ (or port $P5_5$) direction register to output mode.
3. Event Counter Mode
   Operation in event counter mode is the same as in timer mode, except the timer counts signals input through the $CNTR_0$ or $CNTR_1$ pin.
4. Pulse Width Measurement Mode
   If the $CNTR_0$ (or $CNTR_1$) active edge select bit is "0", the timer counts at the oscillation frequency divided by 16 while the $CNTR_0$ (or $CNTR_1$) pin is at "H". If the $CNTR_0$ (or $CNTR_1$) active edge select bit is "1", the count continues during the time that the $CNTR_0$ (or $CNTR_1$) pin is at "L".

In all of these modes, the count can be stopped by setting the timer X (timer Y) count stop bit to "1". Every time a timer overflows, the corresponding interrupt request bit is set.

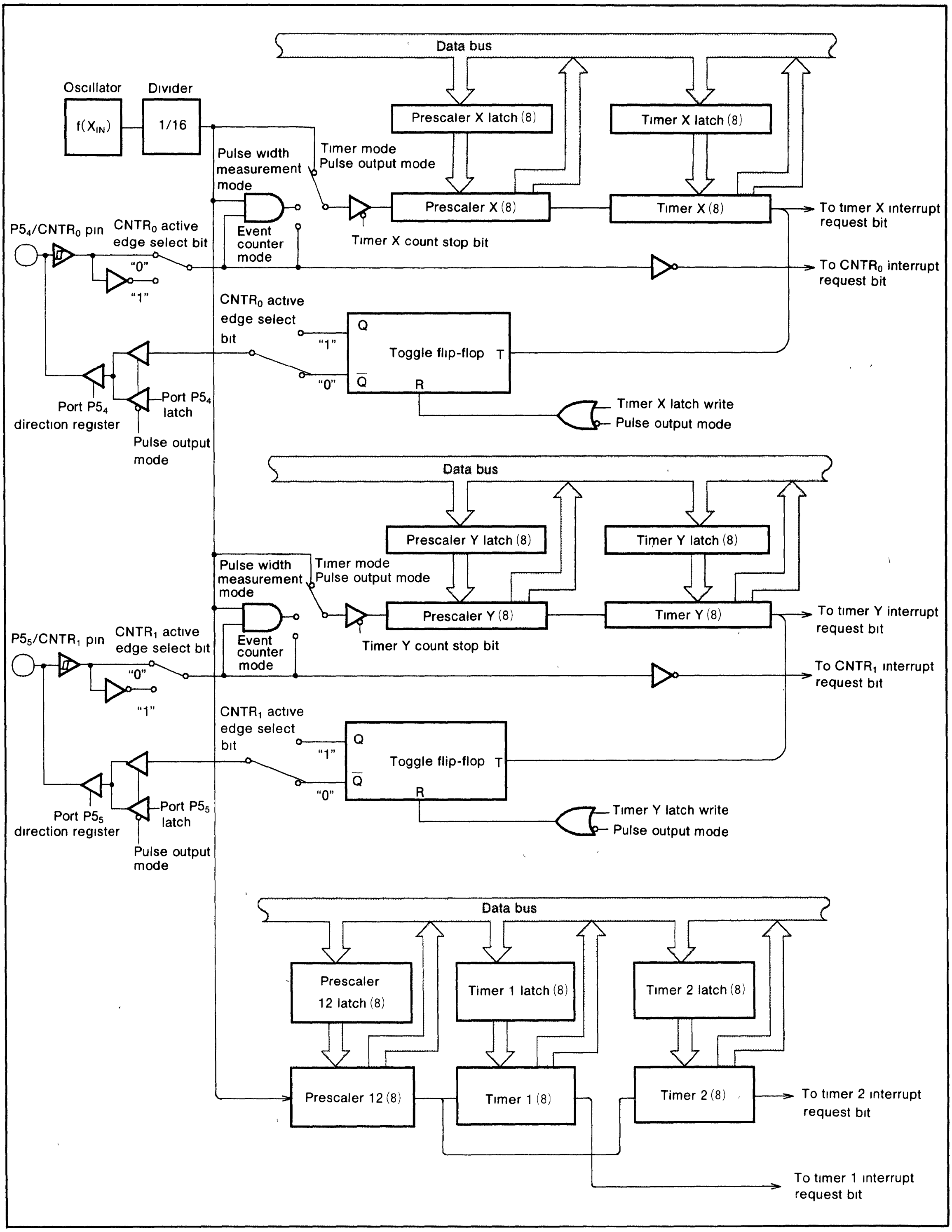


Fig. 9 Block diagram of timer X, timer Y, timer 1, and timer 2

SERIAL I/O1

Serial I/O1 can be used as either clock synchronous or asynchronous (UART) serial I/O. A dedicated timer is also provided for baud rate generation.

(1) Clock Synchronous Serial I/O

Clock synchronous serial I/O1 mode can be selected by setting the mode select bit of the serial I/O1 control register to "1"

For clock-synchronized serial I/O1, the transmitter and the receiver must use the same clock. If an internal clock is used, transfer is started by a write signal to the transmit or receive buffer.

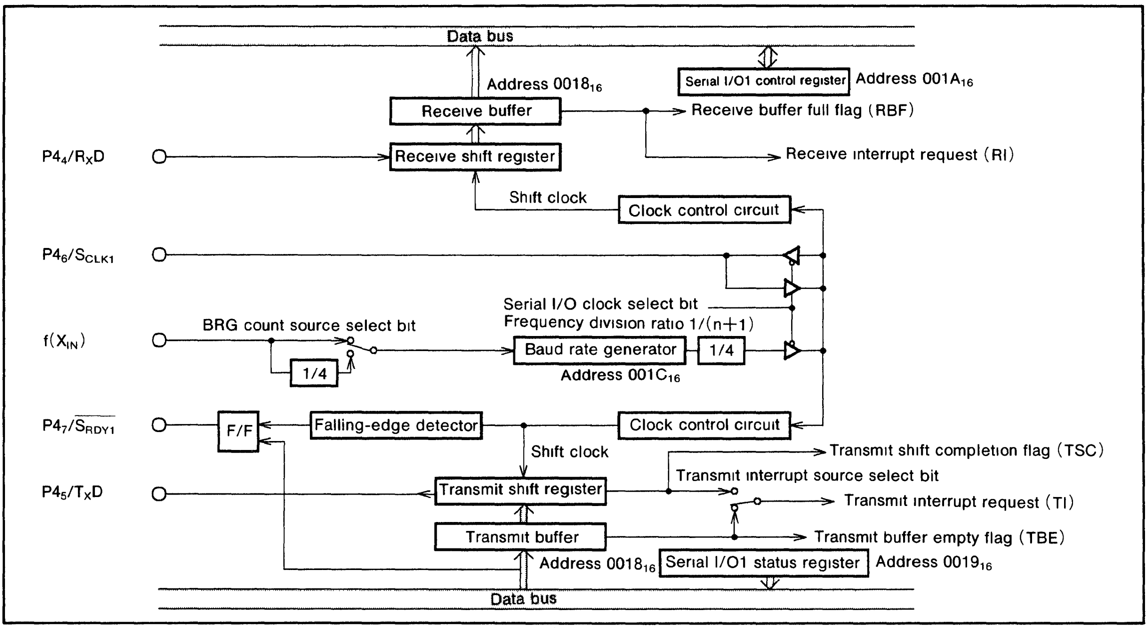
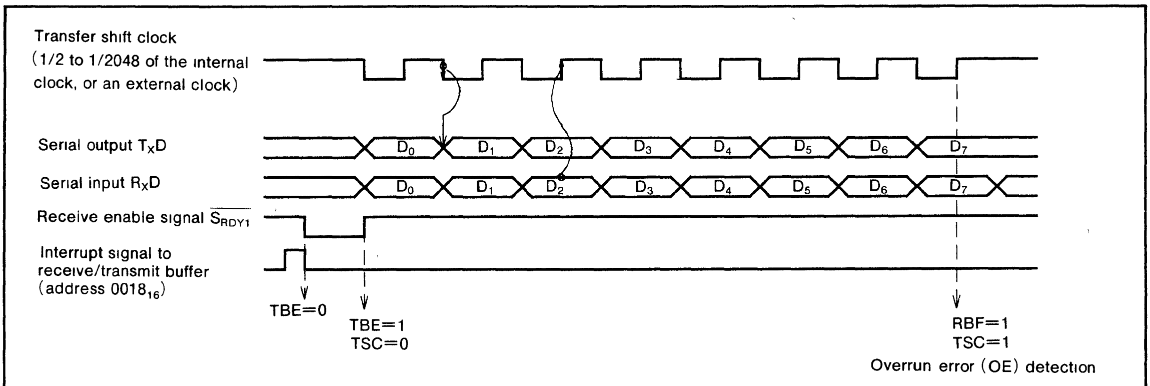


Fig. 10 Block diagram of clock-synchronized serial I/O1



Note 1 : The transmit interrupt (TI) can be selected to occur either when the transmit buffer has emptied (TBE=1) or after the transmit shift operation has ended (TSC=1), by setting the transmit interrupt source select bit (TIC) of the serial I/O1 control register

2 : If data is written to the transfer buffer when TSC=0, the transmit clock is generated continuously and serial data is output continuously from the TxD pin

3 : The receive interrupt (RI) is set when the receive buffer full (RBF) flag becomes "1"

Fig. 11 Operation of clock-synchronized serial I/O1 function

(2) Asynchronous serial I/O (UART) mode

Clock asynchronous serial I/O mode (UART) can be selected by clearing the serial I/O mode select bit of the serial I/O control register to "0".

Eight serial data transfer formats can be selected, and the transfer formats used by a transmitter and receiver must be identical.

The transmit and receive shift registers each have a buffer, but the two buffers have the same address in memory. Since the shift register cannot be written to or read from directly, transmit data is written to the transmit buffer, and receive data is read from the receive buffer. The transmit buffer can also hold the next data to be transmitted, and the receive buffer can hold a character while the next character is being received.

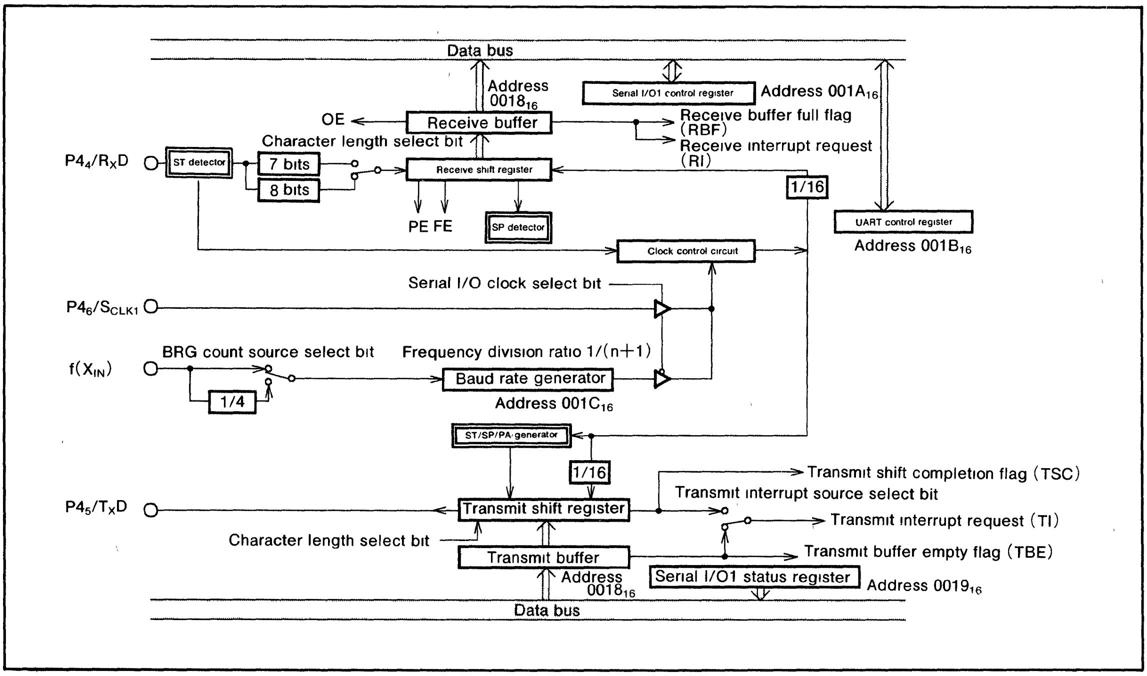
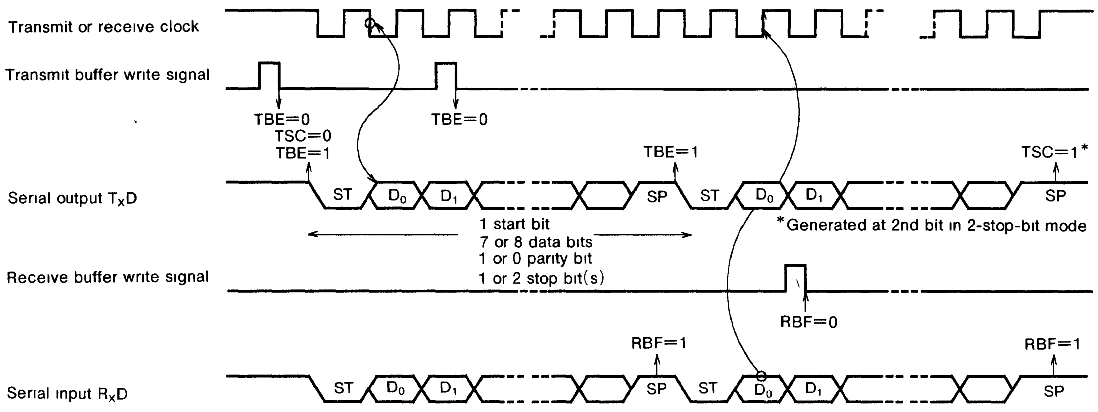


Fig. 12 Block diagram of UART serial I/O



Note 1 : Error flag detection occurs at the same time that the RBF flag becomes "1" (at 1st stop bit, during reception)
2 : The transmit interrupt (TI) can be selected to occur when either the TBE or TSC flag becomes "1", depending on the setting of the transmit interrupt source select bit (TIC) of the serial I/O control register
3 : The receive interrupt (RI) is set when the RBF flag becomes "1"

Fig. 13 Operation of UART serial I/O function

[Serial I/O Control Register (SIO1CON) $001A_{16}$]

The serial I/O control register contains eight control bits for the serial I/O function.

[UART Control Register (UARTCON) $001B_{16}$]

The UART control register consists of four control bits (bits 0 to 3) which are valid when asynchronous serial I/O is selected and set the data format of an data transfer. One bit in this register (bit 4) is always valid and sets the output structure of the $P4_5/T_XD$ pin.

[Serial I/O1 Status Register (SIO1STS) 0019_{16}]

The read-only serial I/O1 status register consists of seven flags (bits 0 to 6) which indicate the operating status of the serial I/O function and various errors.

Three of the flags (bits 4 to 6) are valid only in UART mode.

The receive buffer full flag (bit 1) is cleared to "0" when the receive buffer is read.

If there is an error, it is detected at the same time that data is transferred from the receive shift register to the receive buffer, and the receive buffer full flag is set. A write to the serial I/O status register clears all the error flags OE, PE, FE, and SE (bit 3 to bit six, respectively). Writing "0" to the serial I/O enable bit SIOE (bit 7 of the Serial I/O Control Register) also clears all the status flags, including the error flags.

All bits of the serial I/O1 status register are initialized to "0" at reset, but if the transmit enable bit (bit 4) of the serial I/O control register has been set to "1", the transmitter shift completion flag (bit 2) and the transmitter buffer empty flag (bit 0) become "1".

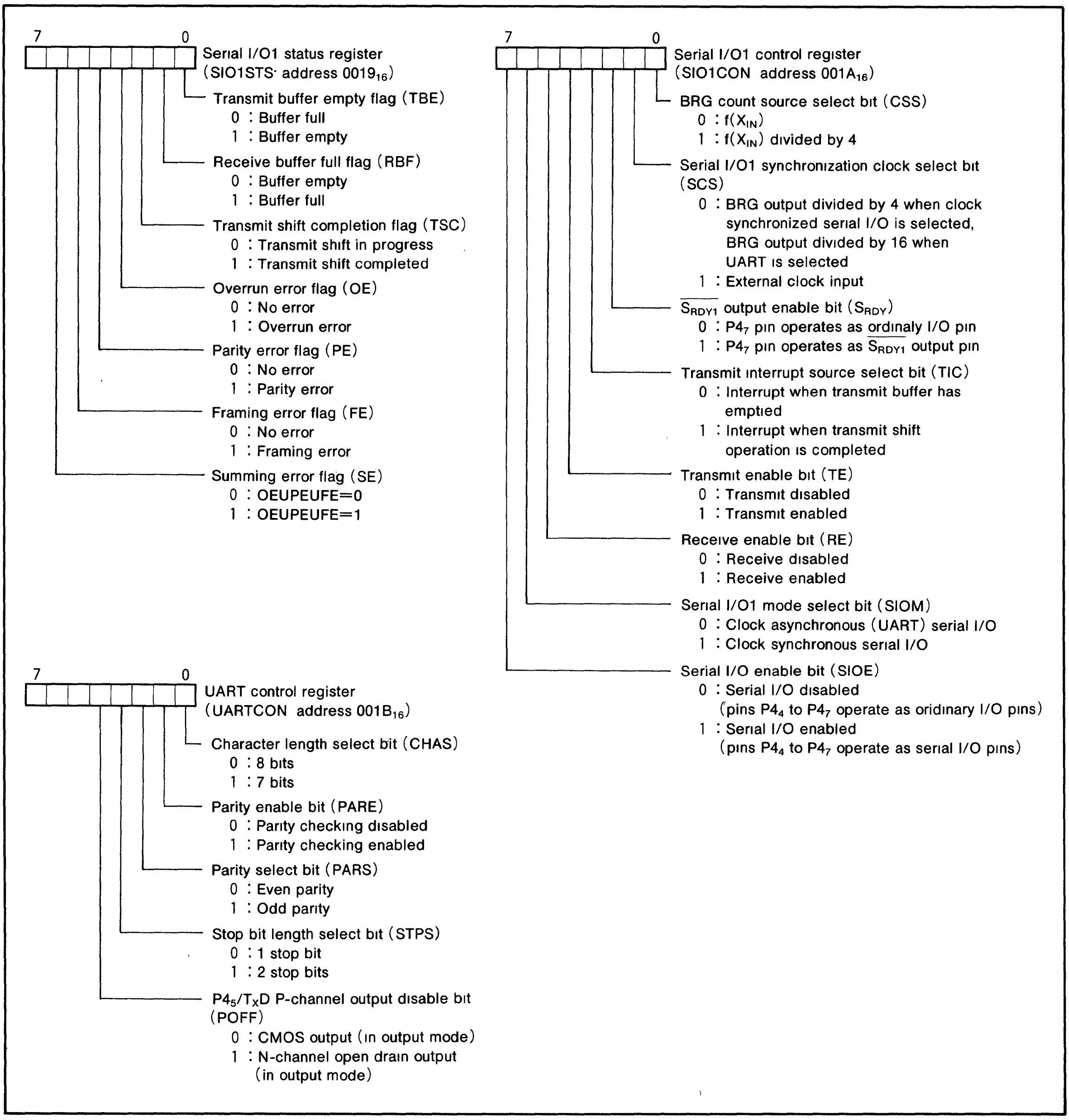
[Transmit Buffer/Receive Buffer (TB/RB) 0018_{16}]

The transmit buffer and the receive buffer are located at the same address. The transmit buffer is write-only and the receive buffer is read-only. If a character bit length is 7 bits, the MSB of data stored in the receive buffer is "0".

[Baud Rate Generator (BRG) $001C_{16}$]

The baud rate generator determines the baud rate for serial transfer.

The baud rate generator divides the frequency of the count source by $1/(n+1)$, where n is the value written to the Baud Rate Generator



Serial I/O1 status register
($SIO1STS$· address 0019_{16})

- Transmit buffer empty flag (TBE)
  - 0 : Buffer full
  - 1 : Buffer empty
- Receive buffer full flag (RBF)
  - 0 : Buffer empty
  - 1 : Buffer full
- Transmit shift completion flag (TSC)
  - 0 : Transmit shift in progress
  - 1 : Transmit shift completed
- Overrun error flag (OE)
  - 0 : No error
  - 1 : Overrun error
- Parity error flag (PE)
  - 0 : No error
  - 1 : Parity error
- Framing error flag (FE)
  - 0 : No error
  - 1 : Framing error
- Summing error flag (SE)
  - 0 : OEUPEUFE=0
  - 1 : OEUPEUFE=1

UART control register
(UARTCON address $001B_{16}$)

- Character length select bit (CHAS)
  - 0 : 8 bits
  - 1 : 7 bits
- Parity enable bit (PARE)
  - 0 : Parity checking disabled
  - 1 : Parity checking enabled
- Parity select bit (PARS)
  - 0 : Even parity
  - 1 : Odd parity
- Stop bit length select bit (STPS)
  - 0 : 1 stop bit
  - 1 : 2 stop bits
- $P4_5/T_XD$ P-channel output disable bit (POFF)
  - 0 : CMOS output (in output mode)
  - 1 : N-channel open drain output (in output mode)

Serial I/O1 control register
(SIO1CON address $001A_{16}$)

- BRG count source select bit (CSS)
  - 0 : $f(X_{IN})$
  - 1 : $f(X_{IN})$ divided by 4
- Serial I/O1 synchronization clock select bit (SCS)
  - 0 : BRG output divided by 4 when clock synchronized serial I/O is selected, BRG output divided by 16 when UART is selected
  - 1 : External clock input
- $\overline{S_{RDY1}}$ output enable bit (S_{RDY})
  - 0 : $P4_7$ pin operates as ordinaly I/O pin
  - 1 : $P4_7$ pin operates as $\overline{S_{RDY1}}$ output pin
- Transmit interrupt source select bit (TIC)
  - 0 : Interrupt when transmit buffer has emptied
  - 1 : Interrupt when transmit shift operation is completed
- Transmit enable bit (TE)
  - 0 : Transmit disabled
  - 1 : Transmit enabled
- Receive enable bit (RE)
  - 0 : Receive disabled
  - 1 : Receive enabled
- Serial I/O1 mode select bit (SIOM)
  - 0 : Clock asynchronous (UART) serial I/O
  - 1 : Clock synchronous serial I/O
- Serial I/O enable bit (SIOE)
  - 0 : Serial I/O disabled (pins $P4_4$ to $P4_7$ operate as oridinary I/O pins)
  - 1 : Serial I/O enabled (pins $P4_4$ to $P4_7$ operate as serial I/O pins)

Fig. 14 Structure of serial I/O control registers

SERIAL I/O2

The serial I/O2 function can be used only for clock synchronous serial I/O.

For clock synchronous serial I/O the transmitter and the receiver must use the same clock. If the internal clock is used, transfer is started by a write signal to the serial I/O2 register.

Serial I/O2 Control Register (SIO2CON) $001D_{16}$

The serial I/O2 control register contains seven bits which control various serial I/O functions.

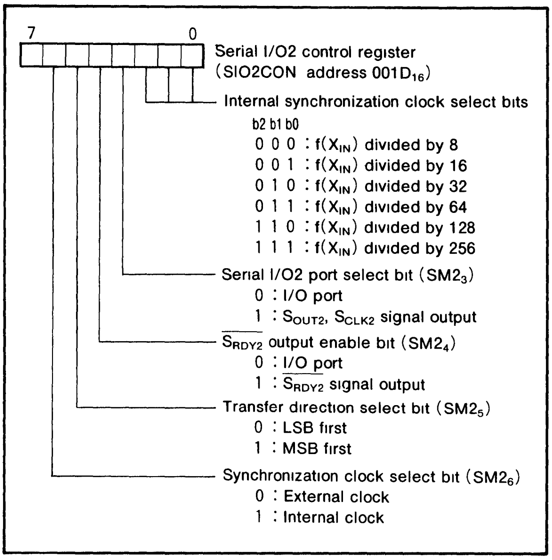


Fig. 15 Structure of serial I/O2 control register

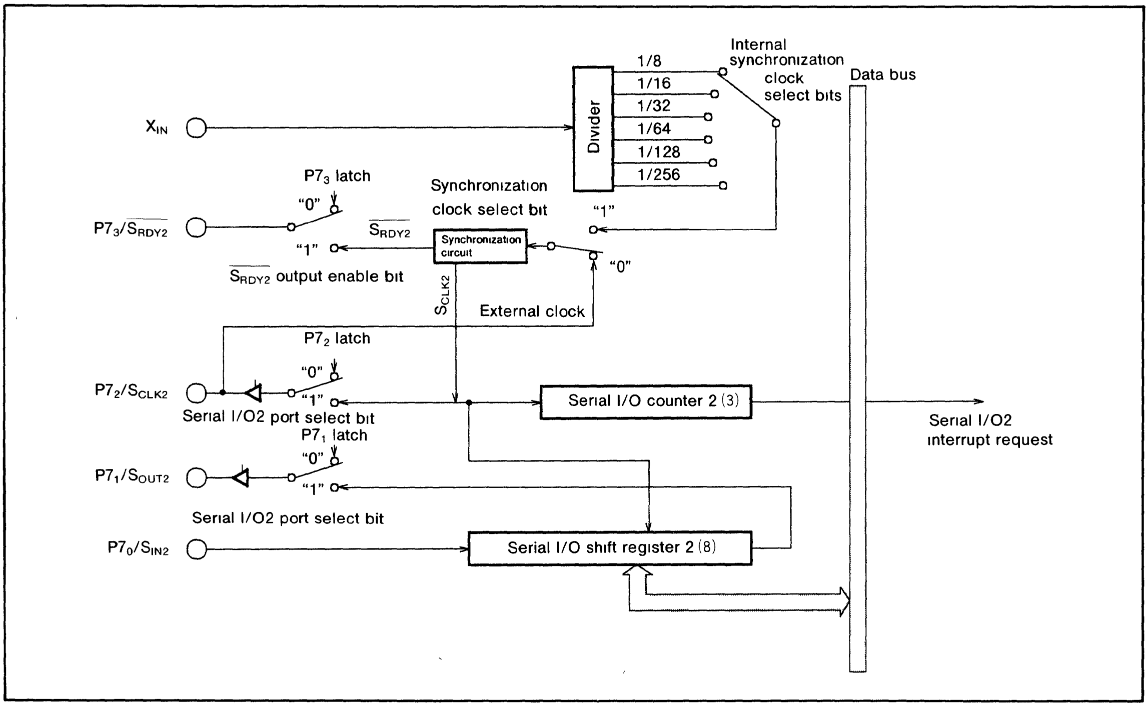
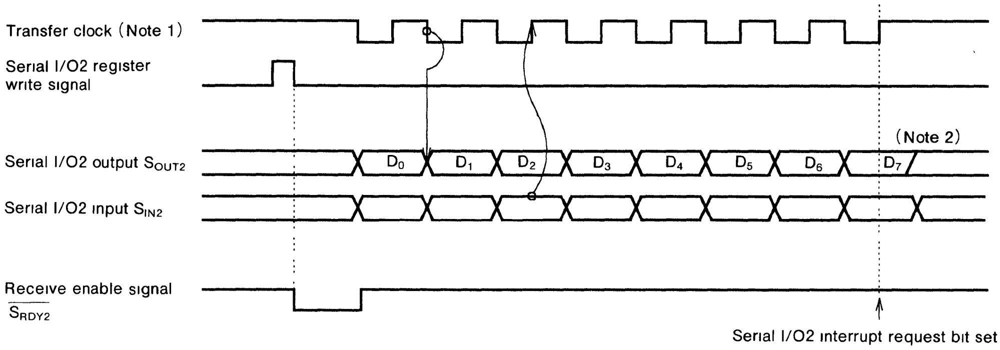


Fig. 16 Block diagram of serial I/O2 function



Note 1. When the internal clock is selected as the transfer clock, the divide ratio can be selected by setting bits 0 to 2 of the serial I/O2 control register

2. When the internal clock is selected as the transfer clock, the S_{OUT2} pin goes to high impedance after transfer completion

Fig. 17 Timing of serial I/O2 function

A-D CONVERTER

The functional blocks of the A-D converter are described below.

[A-D Conversion Register]

The A-D conversion register is a read-only register which contains the result of an A-D conversion. This register should not be read during an A-D conversion.

[AD/DA Control Register]

The AD/DA control register controls the A-D conversion process. Bits 0 to 2 select a specific analog input pin. Bit 3 signals the completion of an A-D conversion. The value of this bit remains at "0" during an A-D conversion, and changes to "1" when an A-D conversion ends. Writing "0" to this bit starts the A-D conversion. Bits 6 and 7 are used to control the output of the D-A converter.

[Comparison Voltage Generator]

The comparison voltage generator divides the voltage between AV_{SS} and V_{REF} into 256 steps for comparison to the analog input.

[Channel Selector]

The channel selector selects one of the ports $P6_0/AN_0$ to $P6_7/AN_7$, and inputs the voltage to the comparator.

[Comparator and Control Circuit]

The comparator and control circuit compares an analog input voltage with the comparison voltage, then stores the result in the A-D conversion register. When an A-D conversion is complete, the control circuit sets the A-D conversion completion bit and the A-D interrupt request bit to "1".

The comparator contains a capacitor, so $f(X_{IN})$ should be at least 500kHz during an A-D conversion.

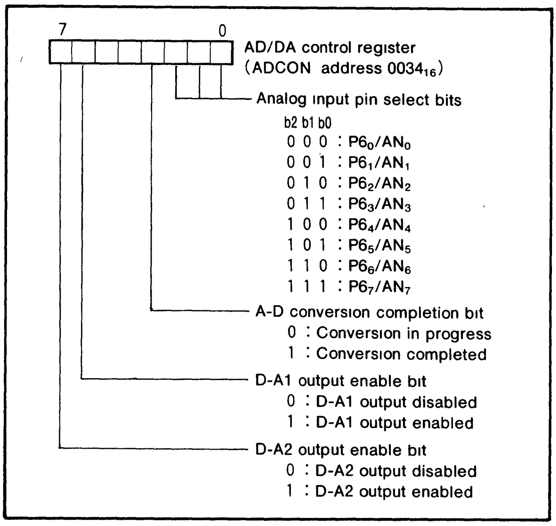


Fig. 18 Structure of AD/DA control register

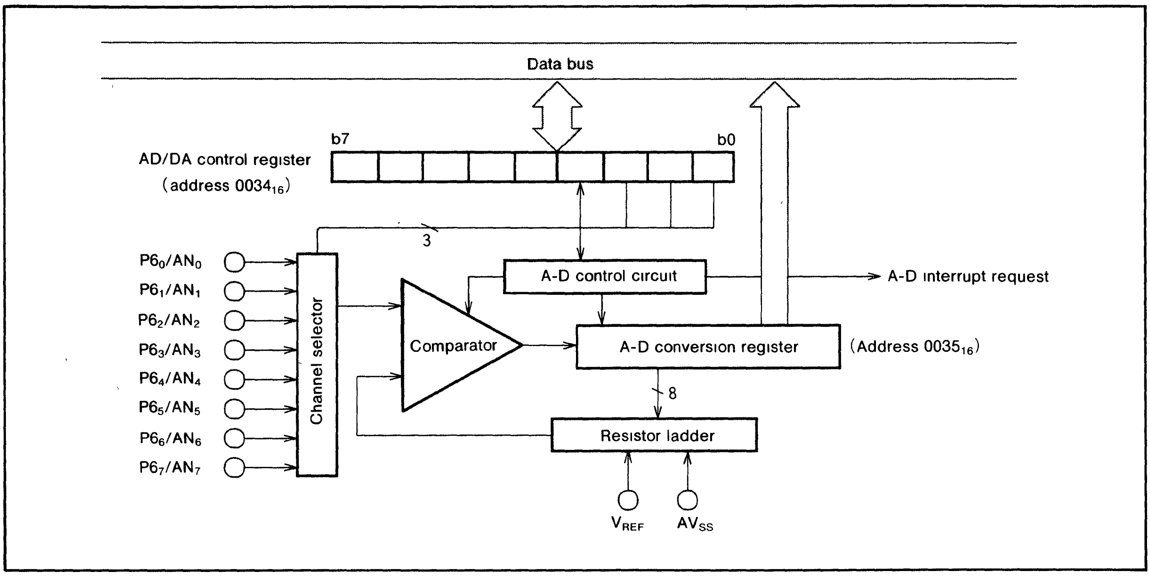


Fig. 19 Block diagram of A-D converter

D-A CONVERTER

Microcomputers of the M3806x group have two internal D-A converters (D-A1 and D-A2) with 8-bit resolutions.

The D-A converter outputs a voltage corresponding to the value in the D-A conversion register. The voltage is output from the DA$_1$ or DA$_2$ pin by setting the D-A output enable bit to "1".

When using the D-A converter,. the corresponding port direction register bit (DA$_1$/P5$_6$ or DA$_2$/P5$_7$) should be set to "0" (input status).

The output analog voltage V is determined by the value n (base 10) in the D-A conversion register as follows:

$V=V_{REF} \times n/256$ (n=0 to 255)

Where V_{REF} is the reference voltage.

At reset, the D-A conversion registers are cleared to "00", the D-A output enable bits are cleared to "0", and the P5$_6$/DA$_1$ and P5$_7$/DA$_2$ pins are set to input (high impedance). The D-A output is not buffered, so the user must supply an external buffer when driving a low-impedance load.

Set V_{CC} to at least 4.0V, when using the D-A converter.

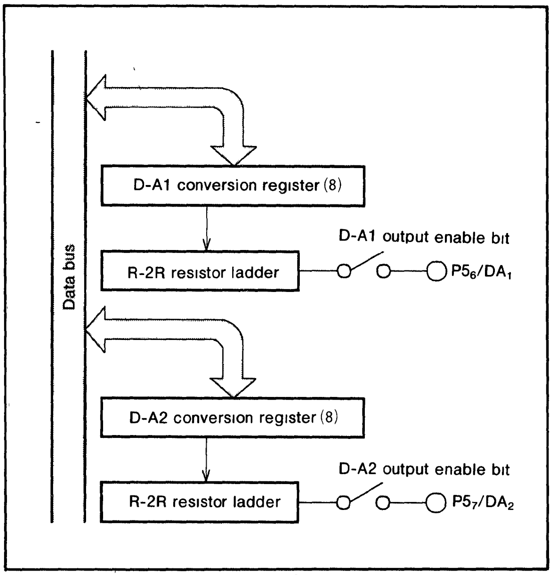


Fig. 20 Block diagram of D-A converter

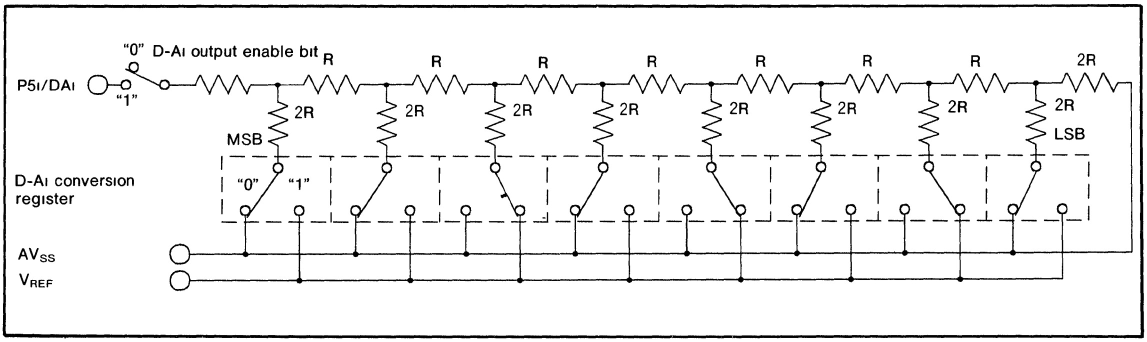


Fig. 21 Equivalent connection circuit of D-A converter

RESET CIRCUIT

A microcomputer in the M3806x group is reset if the $\overline{\text{RESET}}$ pin is held at a "L" level for at least 2μs then is returned to a "H" level (the power supply voltage should be between 4.0V and 5.5V). In order to give the X_{IN} clock time to stabilize, internal operation does not begin until after 8 to 12 X_{IN} clock cycles are complete. After the reset is completed, the program starts from the address contained in address FFFD$_{16}$ (upper byte) and address FFFC$_{16}$ (lower byte). Make sure that the reset input voltage is no more than 0.8V for a power supply voltage of 4.0V.

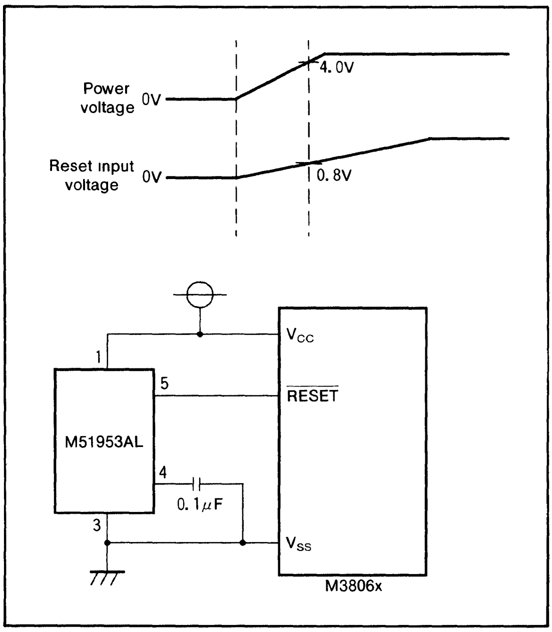
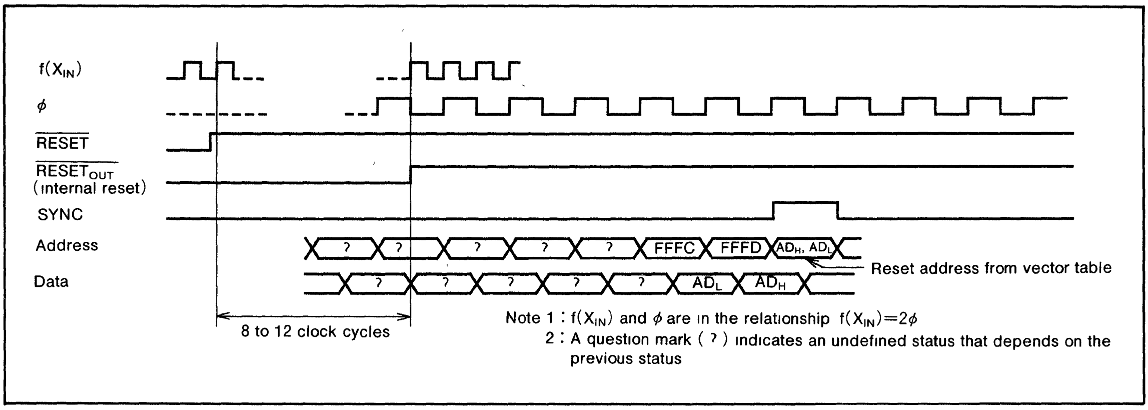


Fig. 22 Example of reset circuit

	Address	Register contents
(1) Port P0 direction register	(0 0 0 1$_{16}$)···	00$_{16}$
(2) Port P1 direction register	(0 0 0 3$_{16}$)···	00$_{16}$
(3) Port P2 direction register	(0 0 0 5$_{16}$)···	00$_{16}$
(4) Port P3 direction register	(0 0 0 7$_{16}$)···	00$_{16}$
(5) Port P4 direction register	(0 0 0 9$_{16}$)···	00$_{16}$
(6) Port P5 direction register	(0 0 0 B$_{16}$)···	00$_{16}$
(7) Port P6 direction register	(0 0 0 D$_{16}$)···	00$_{16}$
(8) Port P7 direction register	(0 0 0 F$_{16}$)···	00$_{16}$
(9) Port P8 direction register	(0 0 1 1$_{16}$)···	00$_{16}$
(10) Serial I/O1 status register	(0 0 1 9$_{16}$)···	1 0 0 0 0 0 0 0
(11) Serial I/O1 control register	(0 0 1 A$_{16}$)···	00$_{16}$
(12) UART control register	(0 0 1 B$_{16}$)···	1 1 1 0 0 0 0 0
(13) Serial I/O2 control register	(0 0 1 D$_{16}$)···	00$_{16}$
(14) Prescaler 12	(0 0 2 0$_{16}$)···	FF$_{16}$
(15) Timer 1	(0 0 2 1$_{16}$)···	01$_{16}$
(16) Timer 2	(0 0 2 2$_{16}$)···	FF$_{16}$
(17) Timer XY mode register	(0 0 2 3$_{16}$)···	00$_{16}$
(18) Prescaler X	(0 0 2 4$_{16}$)···	FF$_{16}$
(19) Timer X	(0 0 2 5$_{16}$)···	FF$_{16}$
(20) Prescaler Y	(0 0 2 6$_{16}$)···	FF$_{16}$
(21) Timer Y	(0 0 2 7$_{16}$)···	FF$_{16}$
(22) AD/DA control register	(0 0 3 4$_{16}$)···	0 0 0 0 1 0 0 0
(23) D-A1 conversion register	(0 0 3 6$_{16}$)···	00$_{16}$
(24) D-A2 conversion register	(0 0 3 7$_{16}$)···	00$_{16}$
(25) Interrupt edge selection register	(0 0 3 A$_{16}$)···	00$_{16}$
(26) CPU mode register	(0 0 3 B$_{16}$)···	0 0 0 0 0 0 ※ 0
(27) Interrupt control register 1	(0 0 3 E$_{16}$)···	00$_{16}$
(28) Interrupt control register 2	(0 0 3 F$_{16}$)···	00$_{16}$
(29) Processor status register	(P S)	X X X X X 1 X X
(30) Program counter	(P C$_H$)	Contents of address FFFD$_{16}$
	(P C$_L$)	Contents of address FFFC$_{16}$

Note : X : Undefined
※ : The initial values of CM_1 are determined by the level at the CNV_{SS} pin
The contents of all other registers and RAM are undefined after a reset, so they must be initialized by software

Fig. 23 Internal status of microcomputer after reset



Note 1 : $f(X_{IN})$ and ϕ are in the relationship $f(X_{IN})=2\phi$

2 : A question mark (?) indicates an undefined status that depends on the previous status

Fig. 24 Timing of reset

CLOCK GENERATION CIRCUIT

An oscillation circuit can be created by connecting a resonator between X_{IN} and X_{OUT}. When using an external clock signal, input the clock signal to the X_{IN} pin and leave the X_{OUT} pin open.

Oscillation Control

(1) Stop Mode

If the STP instruction is executed, oscillation stops with the internal clock ϕ at "H". Timer 1 is set to "FF_{16}" and prescaler 12 is set to "01_{16}".

Oscillation restarts when an external interrupt is received, but the internal clock ϕ remains at "H" until timer 1 overflows.

This allows time for the clock circuit oscillation to stabilize. If oscillation is restarted by a reset, no wait time is generated, so keep the $\overline{\text{RESET}}$ pin at "L" level until oscillation has stabilized.

(2) Wait Mode

If the WIT instruction is executed, the internal clock ϕ stops at a "H" level, but the oscillator itself does not stop. The internal clock restarts if a reset occurs or when an interrupt is received.

Since the oscillator does not stop, normal operation can be started immediately after the clock is restarted.

To ensure that interrupts will be received to release the STP or WIT state, interrupt enable bits must be set to "1" before the STP or WIT instruction is executed.

When the STP status is released, prescaler 12 and timer 1 will start counting and reset will not be released until timer 1 overflows, so set the timer 1 interrupt enable bit to "0" before the STP instruction is executed.

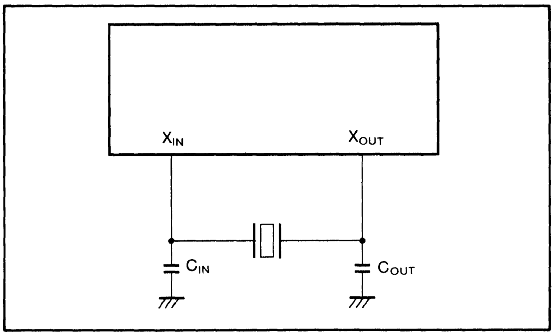


Fig. 25 Ceramic resonator circuit

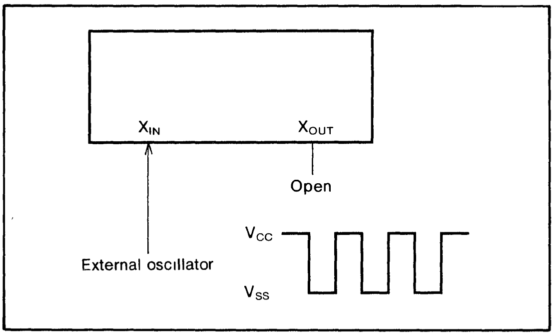


Fig. 26 External clock input circuit

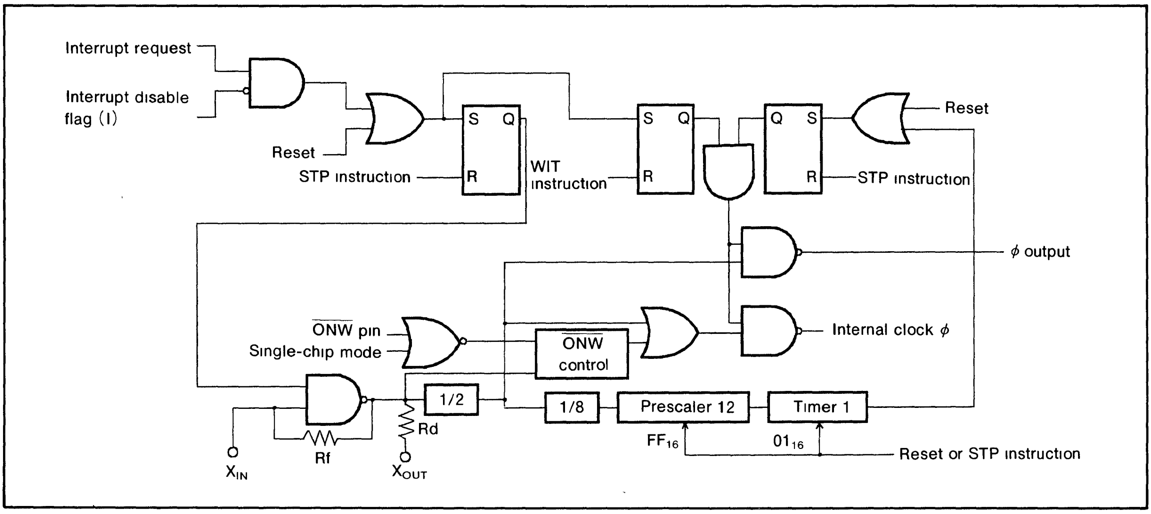


Fig. 27 Block diagram of clock generation circuit

PROCESSOR MODES

Single-chip mode, memory expansion mode, and microprocessor mode can be selected by changing the contents of the processor mode bits CM_0 and CM_1 (bits 0 and 1 of address $003B_{16}$). In memory expansion mode and microprocessor mode, memory can be expanded externally through ports P0 to P3. In these modes, ports P0 to P3 lose their I/O port functions and become bus pins.

Table 2 Functions of ports in memory expansion mode and microprocessor mode

Port Name	Function
Port P0	Outputs lower byte of address.
Port P1	Outputs upper byte of address
Port P2	Operates as I/O pins for data D_7 to D_0 (including instruction codes)
Port P3	$P3_0$ and $P3_1$ function only as output pins (except that the port latch cannot be read) $P3_2$ is the $\overline{ONW}$ input pin. $P3_3$ is the $\overline{RESET_{OUT}}$ output pin (Note) $P3_4$ is the ϕ output pin. $P3_5$ is the SYNC output pin. $P3_6$ is the $\overline{WR}$ output pin, and $P3_7$ is the $\overline{RD}$ output pin

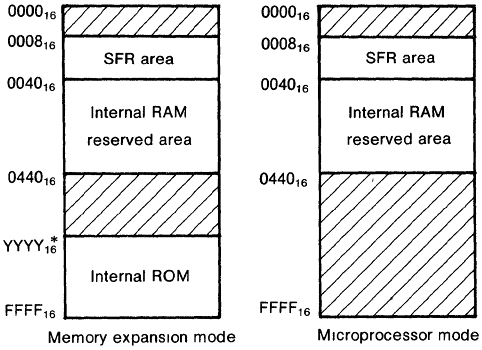
Note : If CNV_{SS} is connected to V_{SS}, the microcomputer goes to single-chip mode after a reset, so this pin cannot be used as the $RESET_{OUT}$ output pin

- **Single-Chip Mode**

  Select this mode by resetting the microcomputer with CNV_{SS} connected to V_{SS}.
- **Memory Expansion Mode**

  Select this mode by setting the processor mode bits to "01" in software with CNV_{SS} connected to V_{SS}. This mode enables external memory expansion while maintaining the validity of the internal ROM. Internal ROM will take precedence over external memory if addresses conflict.
- **Microprocessor Mode**

  Select this mode by resetting the microcomputer with CNV_{SS} connected to V_{CC}, or by setting the processor mode bits to "10" in software with CNV_{SS} connected to V_{SS}. In microprocessor mode, the internal ROM is no longer valid and external memory must be used.



The shaded areas are external memory areas

* : $YYYY_{16}$ is the start address of internal ROM

Fig. 28 Memory maps in various processor modes

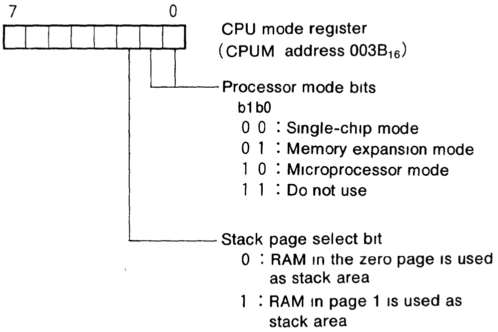
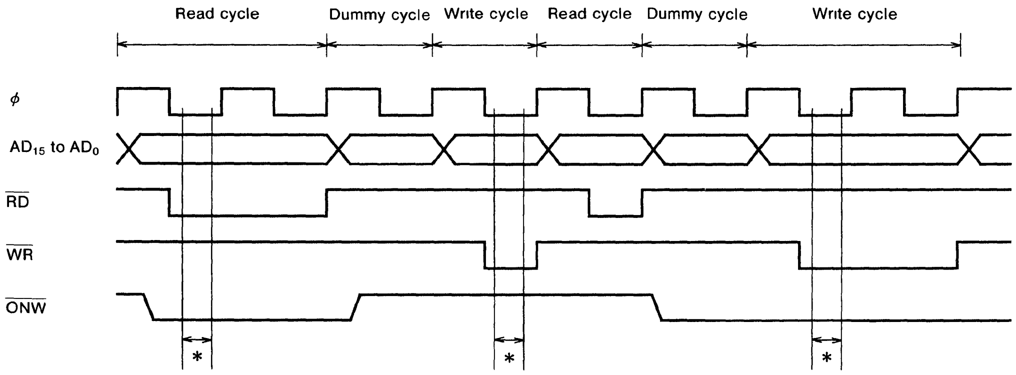


Fig. 29 Structure of CPU mode register

Bus Control with Memory Expansion

Microcomputers of the M3806x group have a built-in $\overline{\mathrm{ONW}}$ function to facilitate access to extra memory and I/O functions in memory expansion mode or microprocessor mode. If an "L" level signal is input to the $\overline{\mathrm{ONW}}$ pin when the CPU is in a read or write state, the corresponding read or write cycle is extended by one cycle of ϕ. During this extended period, the $\overline{\mathrm{RD}}$ or $\overline{\mathrm{WR}}$ signal remains at "L". This extension period is valid only for writing to and reading from addresses 0000_{16} to 0007_{16} and 0440_{16} to FFFF_{16}, and only read and write cycles are extended.



* : Period during which $\overline{\mathrm{ONW}}$ input signal is received
During this period, the $\overline{\mathrm{ONW}}$ signal must be fixed at either "H" or "L" At all other times, the input level of the $\overline{\mathrm{ONW}}$ signal has no affect on operations.
The bus cycles is not extended for an address in the area 0008_{16} to $043F_{16}$, regardless of whether the $\overline{\mathrm{ONW}}$ signal is received

Fig. 30 $\overline{\mathrm{ONW}}$ function timing

NOTES ON PROGRAMMING

Processor Status Register

The contents of the processor status register (PS) after a reset are undefined, except for the interrupt disable flag (I) which is "1". Therefore, flags that affect program execution must be initialized after a reset.

In particular, it is essential to initialize the T and D flags because of their effect on calculations.

Interrupts

The contents of the interrupt request bits do not change immediately after they have been written. After writing to an interrupt request register, execute at least one instruction before performing a BBC or BBS instruction.

Decimal Calculations

To calculate in decimal notation, set the decimal mode flag (D) to "1", then execute a ADC or SBC instruction. Only the ADC and SBC instructions yield proper decimal results. After executing an ADC or SBC instruction, execute at least one instruction before executing a SEC, CLC, or CLD instruction.

In decimal mode, the values of the negative (N), overflow (V), and zero (Z) flags are invalid.

The carry flag can be used to indicate whether a carry or borrow has occurred, but must be initialized before each calculation. Clear the carry flag before an ADC and set the flag before an SBC.

Timers

If a value n (between 0 and 255) is written to a timer latch, the frequency division ratio is 1/(n+1).

Multiplication and Division Instructions

The MUL and DIV instructions do not affect the T and D flags.

The execution of these instructions does not change the contents of the processor status register.

Ports

The contents of the port direction registers cannot be read. Programs can not use the value of a direction register as an index, or bit-test a direction register (BBC or BBS), or perform a read-modify-write instruction such as ROR, CLB, or SEB. Use instructions such as LDM and STA to set the port direction registers.

Serial I/O

In clock synchronous serial I/O, if the receive side is using an external clock and it is to output the $\overline{S_{RDY1}}$ signal, set the transmit enable bit, the receive enable bit, and the $\overline{S_{RDY1}}$ output enable bit to "1".

Serial I/O1 continues to output the final bit from the T_XD pin after transmission is completed. The S_{OUT2} pin from serial I/O2 goes to high impedance after transmission is completed

A-D Converter

The comparator uses internal capacitors whose charge will be lost if the clock frequency is too low.

Make sure that $f(X_{IN})$ is at least 500kHz during an A-D conversion. (If the $\overline{ONW}$ pin has been set to "L", the A-D conversion will take twice as long to match the longer bus cycle, and so $f(X_{IN})$ must be at least 1MHz.)

Do not execute the STP or WIT instruction during an A-D conversion.

D-A Converter

The accuracy of the D-A converter becomes poor rapidly under the V_{CC} =4.0V or less condition. So set V_{CC} to at least 4.0V, when using the D-A converter.

Instruction Execution Time

The instruction execution time is obtained by multiplying the frequency of the internal clock ϕ by the number of cycles needed to execute an instruction.

The number of cycles required to execute an instruction is shown in the list of machine instructions.

The frequency of the internal clock ϕ is half of the X_{IN} frequency.

When the $\overline{ONW}$ function is used in modes other than single-chip mode, the frequency of the internal clock ϕ may be one fourth the X_{IN} frequency.

DATA REQUIRED FOR MASK ORDERS

The following are necessary when ordering a mask ROM production:

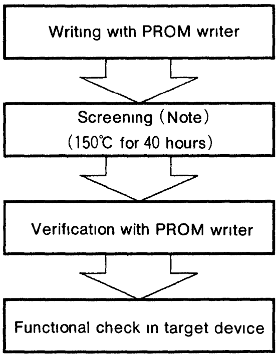
1. Mask ROM Order Confirmation Form
2. Mask Specification Form
3. Data to be written to ROM, in EPROM form (three identical copies)

ROM Writing Method

The built-in PROM of the blank one-time programmable version and built-in EPROM version can be read from and written to with an normal EPROM writer using a special write adapter.

Package	Name of Write Adapter
80P6N	PCA4738F-80
80P6S	PCA4738G-80
80D0	PCA4738L-80

The PROM of the blank one-time programmable version is not tested or screened after assembly. To ensure proper operation after writing, the procedure shown in Figure 31 is recommended to verify programming.



Note : The screening temperature is far higher than the storage temperature Do not leave the microcomputer at 150℃ for longer than 100 hours

Fig. 31 Writing and testing of one-time programmable version

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	All voltages measured with reference to the V_{SS} pin, output transistors isolated	−0.3 to 7.0	V
V_I	Input voltage $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_0$-$P7_7$, $P8_0$-$P8_7$, V_{REF}		−0.3 to V_{CC}+0.3	V
V_I	Input voltage $\overline{RESET}$, X_{IN}		−0.3 to V_{CC}+0.3	V
V_I	Input voltage CNV_{SS}		−0.3 to 13	V
V_O	Output voltage $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_0$-$P7_7$, $P8_0$-$P8_7$, X_{OUT}		−0.3 to V_{CC}+0.3	V
P_d	Power dissipation	T_a = 25℃	500	mW
T_{opr}	Operating temperature		−20 to 85	℃
Tstg	Storage temperature		−40 to 125	℃

RECOMMENDED OPERATING CONDITIONS (V_{CC} = 3.0 to 5.5V, T_a = −20 to 85℃, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage ($f(X_{IN}) \leqq 2MHz$)	3.0	5.0	5.5	V
	Supply voltage ($f(X_{IN}) > 2MHz$)	4.0	5.0	5.5	
	Supply voltage (when D-A converter is used)	4.0	5.0	5.5	
V_{SS}	Supply voltage		0		V
V_{REF}	Analog reference voltage (when A-D converter is used)	2.0		V_{CC}	V
	Analog reference voltage (when D-A converter is used)	4.0		V_{CC}	
AV_{SS}	Analog power voltage		0		V
V_{IA}	Analog input voltage AN_0-AN_7	AV_{SS}		V_{CC}	V
V_{IH}	"H" input voltage $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_0$-$P7_7$, $P8_0$-$P8_7$	0.8V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage $\overline{RESET}$, X_{IN}, CNV_{SS}	0.8V_{CC}		V_{CC}	V
V_{IL}	"L" input voltage $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_0$-$P7_7$, $P8_0$-$P8_7$	0		0.2V_{CC}	V
V_{IL}	"L" input voltage $\overline{RESET}$	0		0.2V_{CC}	V
V_{IL}	"L" input voltage X_{IN}	0		0.16V_{CC}	V
V_{IL}	"L" input voltage CNV_{SS}	0		0.2V_{CC}	V
$\Sigma I_{OH(peak)}$	"H" total peak output current $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P8_0$-$P8_7$ (Note 1)			−80	mA
$\Sigma I_{OH(peak)}$	"H" total peak output current $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$ (Note 1)			−80	mA
$\Sigma I_{OL(peak)}$	"L" total peak output current $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P8_0$-$P8_7$ (Note 1)			80	mA
$\Sigma I_{OL(peak)}$	"L" total peak output current $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_0$-$P7_7$ (Note 1)			80	mA
$\Sigma I_{OH(avg)}$	"H" total average output current $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P8_0$-$P8_7$ (Note 1)			−40	mA
$\Sigma I_{OH(avg)}$	"H" total average output current $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$ (Note 1)			−40	mA
$\Sigma I_{OL(avg)}$	"L" total average output current $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P8_0$-$P8_7$ (Note 1)			40	mA
$\Sigma I_{OL(avg)}$	"L" total average output current $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_0$-$P7_7$ (Note 1)			40	mA
$I_{OH(peak)}$	"H" peak output current $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P8_0$-$P8_7$ (Note 2)			−10	mA
$I_{OL(peak)}$	"L" peak output current $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_0$-$P7_7$, $P8_0$-$P8_7$ (Note 2)			10	mA
$I_{OH(avg)}$	"H" average output current $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P8_0$-$P8_7$ (Note 3)			−5	mA
$I_{OL(avg)}$	"L" average output current $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_0$-$P7_7$, $P8_0$-$P8_7$ (Note 3)			5	mA
$f(X_{IN})$	Internal clock oscillation frequency (V_{CC}=4.0~5.5V)			8	MHz
	Internal clock oscillation frequency (V_{CC}=3.0~5.5V)			2	

Note 1 The total output current is the sum of all the currents flowing through all the applicable ports The total average current is an average value measured over 100ms The total peak current is the peak value of all the currents

2 The peak output current is the peak current flowing in each port

3 The average output current I_{OL} (avg), I_{OH} (avg) in an average value measured over 100ms

ELECTRICAL CHARACTERISTICS (V_{CC} = 3.0 to 5.5V, V_{SS} = 0V, T_a = −20 to 85℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max	
V_{OH}	"H" output voltage $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P8_0$-$P8_7$ (Note 1)	$I_{OH}=-10mA$ $V_{CC}=4.0\sim5.5V$	$V_{CC}-2.0$			V
		$I_{OH}=-1.0mA$ $V_{CC}=3.0\sim5.5V$	$V_{CC}-1.0$			
V_{OL}	"L" output voltage $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_0$-$P7_7$, $P8_0$-$P8_7$	$I_{OL}=10mA$ $V_{CC}=4.0\sim5.5V$			2.0	V
		$I_{OL}=1.0mA$ $V_{CC}=3.0\sim5.5V$			1.0	
$V_{T+}-V_{T-}$	Hysteresis $CNTR_0$, $CNTR_1$, INT_0-INT_4			0.4		V
$V_{T+}-V_{T-}$	Hysteresis R_xD, S_{CLK1}, S_{IN2}, S_{CLK2}			0.5		V
$V_{T+}-V_{T-}$	Hysteresis $\overline{RESET}$			0.5		V
I_{IH}	"H" input current $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_0$-$P7_7$, $P8_0$-$P8_7$	$V_I=V_{CC}$			5.0	μA
I_{IH}	"H" input current $\overline{RESET}$, CNV_{SS}	$V_I=V_{CC}$			5.0	μA
I_{IH}	"H" input current X_{IN}	$V_I=V_{CC}$		4		μA
I_{IL}	"L" input current $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_0$-$P7_7$, $P8_0$-$P8_7$, $\overline{RESET}$, CNV_{SS}	$V_I=V_{SS}$			−5.0	μA
I_{IL}	"L" input current X_{IN}	$V_I=V_{SS}$		−4		μA
V_{RAM}	RAM hold voltage	With clock stopped	2.0		5.5	V
I_{CC}	Supply current	$f(X_{IN})=8MHz$, $V_{CC}=5V$		6.4	13	mA
		$f(X_{IN})=5MHz$, $V_{CC}=5V$		4	8	
		$f(X_{IN})=2MHz$, $V_{CC}=3V$		0.8	2.0	
		When WIT instruction is executed with $f(X_{IN})=8MHz$, $V_{CC}=5V$		1.5		
		When WIT instruction is executed with $f(X_{IN})=5MHz$, $V_{CC}=5V$		1		
		When WIT instruction is executed with $f(X_{IN})=2MHz$, $V_{CC}=3V$		0.2		
		When STP instruction is executed with clock stopped, output transistors isolated T_a=25℃ (Note 2)		0.1	1	μA
		T_a=85℃ (Note 2)			10	

Note 1 : $P4_5$ is measured when the $P4_5/T_xD$ P-channel output disable bit of the UART control register (bit 4 of address $001B_{16}$) is "0"
2 : With output transistors isolated and A-D converter having completed conversion, and not including current flowing through V_{REF} pin

A-D CONVERTER CHARACTERISTICS

(V_{CC}=3.0 to 5.5V, V_{SS}=AV_{SS}=0V, V_{REF}=2.0V to V_{CC}, T_a=−20 to 85℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
—	Resolution				8	Bits
—	Absolute accuracy (excluding quantization error)			±1	±2.5	LSB
t_{CONV}	Conversion time				50	t_C (ϕ)
R_{LADDER}	Ladder resistor			35		kΩ
I_{VREF}	Reference power source input current (Note)	V_{REF}=5.0V	50	150	200	μA
$I_{I(AD)}$	A-D port input current			0.5		μA

Note : When D-A conversion registers (addresses 0036_{16} and 0037_{16}) contain "00_{16}"

D-A CONVERTER CHARACTERISTICS

(V_{CC}=4.0 to 5.5V, V_{SS}=AV_{SS}=0V, V_{REF}=4.0V to V_{CC}, T_a=−20 to 85℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
—	Resolution				8	Bits
—	Absolute accuracy				1.0	%
t_{SU}	Setting time				3	μs
R_O	Output resistor		1	2.5	4	kΩ
I_{VREF}	Reference power source input current (Note)				3.2	mA

Note : Using one D-A converter, with the value in the D-A conversion register of the other D-A converter being "00_{16}", and excluding currents flowing through the A-D resistance ladder

TIMING REQUIREMENTS 1 (V_{CC} =4.0 to 5.5V, V_{SS} = 0V, T_a = −20 to 85℃, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max.	
$t_{W(\overline{RESET})}$	Reset input "L" pulse width	2			μs
$t_{C(X_{IN})}$	External clock input cycle time	125			ns
$t_{WH(X_{IN})}$	External clock input "H" pulse width	50			ns
$t_{WL(X_{IN})}$	External clock input "L" pulse width	50			ns
$t_{C(CNTR)}$	$CNTR_0$, $CNTR_1$ input cycle time	200			ns
$t_{WH(CNTR)}$	$CNTR_0$, $CNTR_1$ input "H" pulse width	80			ns
$t_{WH(INT)}$	INT_0 to INT_4 input "H" pulse width	80			ns
$t_{WL(CNTR)}$	$CNTR_0$, $CNTR_1$ input "L" pulse width	80			ns
$t_{WL(INT)}$	INT_0 to INT_4 input "L" pulse width	80			ns
$t_{C(S_{CLK1})}$	Serial I/O1 clock input cycle time (Note)	800			ns
$t_{C(S_{CLK2})}$	Serial I/O2 clock input cycle time	1000			ns
$t_{WH(S_{CLK1})}$	Serial I/O1 clock input "H" pulse width (Note)	370			ns
$t_{WH(S_{CLK2})}$	Serial I/O2 clock input "H" pulse width	400			ns
$t_{WL(S_{CLK1})}$	Serial I/O1 clock input "L" pulse width (Note)	370			ns
$t_{WL(S_{CLK2})}$	Serial I/O2 clock input "L" pulse width	400			ns
$t_{SU(R_XD-S_{CLK1})}$	Serial I/O1 input set up time	220			ns
$t_{SU(S_{IN2}-S_{CLK2})}$	Serial I/O2 input set up time	200			ns
$t_{h(S_{CLK1}-R_XD)}$	Serial I/O1 input hold time	100			ns
$t_{h(S_{CLK2}-S_{IN2})}$	Serial I/O2 input hold time	200			ns

Note : When $f(X_{IN})$=8MHz and bit 6 of address $001A_{16}$ is "1" Divide this value by four when $f(X_{IN})$=8MHz and bit 6 of address $001A_{16}$ is "0"

TIMING REQUIREMENTS 2 (V_{CC} =3.0 to 5.5V, V_{SS} = 0V, T_a = −20 to 85℃, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
$t_{W(\overline{RESET})}$	Reset input "L" pulse width	2			μs
$t_{C(X_{IN})}$	External clock input cycle time	500			ns
$t_{WH(X_{IN})}$	External clock input "H" pulse width	200			ns
$t_{WL(X_{IN})}$	External clock input "L" pulse width	200			ns
$t_{C(CNTR)}$	$CNTR_0$, $CNTR_1$ input cycle time	500			ns
$t_{WH(CNTR)}$	$CNTR_0$, $CNTR_1$ input "H" pulse width	230			ns
$t_{WH(INT)}$	INT_0 to INT_4 input "H" pulse width	230			ns
$t_{WL(CNTR)}$	$CNTR_0$, $CNTR_1$ input "L" pulse width	230			ns
$t_{WL(INT)}$	INT_0 to INT_4 input "L" pulse width	230			ns
$t_{C(S_{CLK1})}$	Serial I/O1 clock input cycle time (Note)	2000			ns
$t_{C(S_{CLK2})}$	Serial I/O2 clock input cycle time	2000			ns
$t_{WH(S_{CLK1})}$	Serial I/O1 clock input "H" pulse width (Note)	950			ns
$t_{WH(S_{CLK2})}$	Serial I/O2 clock input "H" pulse width	950			ns
$t_{WL(S_{CLK1})}$	Serial I/O1 clock input "L" pulse width (Note)	950			ns
$t_{WL(S_{CLK2})}$	Serial I/O2 clock input "L" pulse width	950			ns
$t_{SU(R_XD-S_{CLK1})}$	Serial I/O1 input set up time	400			ns
$t_{SU(S_{IN2}-S_{CLK2})}$	Serial I/O2 input set up time	400			ns
$t_{h(S_{CLK1}-R_XD)}$	Serial I/O1 input hold time	200			ns
$t_{h(S_{CLK2}-S_{IN2})}$	Serial I/O2 input hold time	300			ns

Note : When $f(X_{IN})$=2MHz and bit 6 of address $001A_{16}$ is "1" Divide this value by four when $f(X_{IN})$=2MHz and bit 6 of address $001A_{16}$ is "0"

SWITCHING CHARACTERISTICS 1 (V_{CC} = 4.0 to 5.5V, V_{SS} = 0V, T_a = −20 to 85℃, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
$t_{WH(S_{CLK1})}$	Serial I/O1 clock output "H" pulse width	$t_{c(S_{CLK1})}/2-30$			ns
$t_{WH(S_{CLK2})}$	Serial I/O2 clock output "H" pulse width	$t_{c(S_{CLK2})}/2-160$			ns
$t_{WL(S_{CLK1})}$	Serial I/O1 clock output "L" pulse width	$t_{c(S_{CLK1})}/2-30$			ns
$t_{WL(S_{CLK2})}$	Serial I/O2 clock output "L" pulse width	$t_{c(S_{CLK2})}/2-160$			ns
$t_{d(S_{CLK1}-T_XD)}$	Serial I/O1 output delay time (Note 1)			140	ns
$t_{d(S_{CLK2}-S_{OUT2})}$	Serial I/O2 output delay time			$0.2 \times t_{c(S_{CLK2})}$	ns
$t_{v(S_{CLK1}-T_XD)}$	Serial I/O1 output valid time (Note 1)	−30			ns
$t_{v(S_{CLK2}-S_{OUT2})}$	Serial I/O2 output valid time	0			ns
$t_{r(S_{CLK1})}$	Serial I/O1 clock output rise time			30	ns
$t_{f(S_{CLK1})}$	Serial I/O1 clock output fall time			30	ns
$t_{f(S_{CLK2})}$	Serial I/O2 clock output fall time			40	ns
$t_{r(CMOS)}$	CMOS output rise time (Note 2)		10	30	ns
$t_{f(CMOS)}$	CMOS output fall time (Note 2)		10	30	ns

Note 1 : When the $P4_5/T_XD$ P-channel output disable bit of the UART control register (bit 4 of address $001B_{16}$) is "0"
2 : X_{OUT} pin excluded.

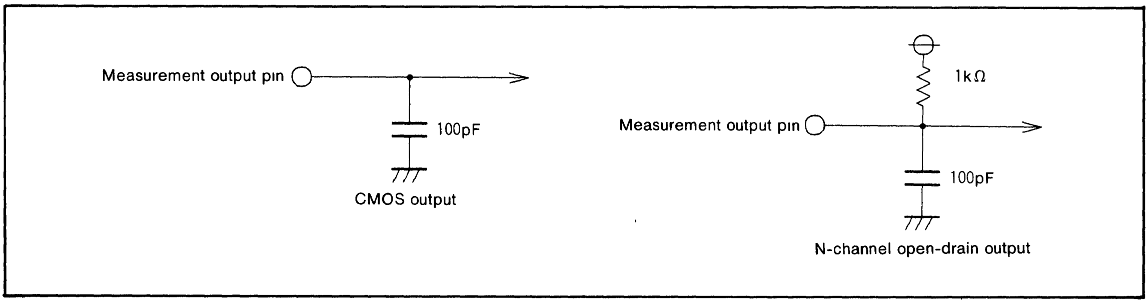


Fig. 32 Circuit for measuring output switching characteristics (1)

SWITCHING CHARACTERISTICS 2 (V_{CC} = 3.0 to 5.5V, V_{SS} = 0V, T_a = −20 to 85℃, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
$t_{WH(S_{CLK1})}$	Serial I/O1 clock output "H" pulse width	$t_{c(S_{CLK1})}/2-50$			ns
$t_{WH(S_{CLK2})}$	Serial I/O2 clock output "H" pulse width	$t_{c(S_{CLK2})}/2-240$			ns
$t_{WL(S_{CLK1})}$	Serial I/O1 clock output "L" pulse width	$t_{c(S_{CLK1})}/2-50$			ns
$t_{WL(S_{CLK2})}$	Serial I/O2 clock output "L" pulse width	$t_{c(S_{CLK2})}/2-240$			ns
$t_{d(S_{CLK1}-T_XD)}$	Serial I/O1 output delay time (Note 1)			350	ns
$t_{d(S_{CLK2}-S_{OUT2})}$	Serial I/O2 output delay time			$0.2 \times t_{c(S_{CLK2})}$	ns
$t_{v(S_{CLK1}-T_XD)}$	Serial I/O1 output valid time (Note 1)	−30			ns
$t_{v(S_{CLK2}-S_{OUT2})}$	Serial I/O2 output valid time	0			ns
$t_{r(S_{CLK1})}$	Serial I/O1 clock output rise time			50	ns
$t_{f(S_{CLK1})}$	Serial I/O1 clock output fall time			50	ns
$t_{f(S_{CLK2})}$	Serial I/O2 clock output fall time			50	ns
$t_{r(CMOS)}$	CMOS output rise time (Note 2)		20	50	ns
$t_{f(CMOS)}$	CMOS output fall time (Note 2)		20	50	ns

Note 1 : When the $P4_5/T_XD$ P-channel output disable bit of the UART control register (bit 4 of address $001B_{16}$) is "0"
2 : X_{OUT} pin excluded.

TIMING REQUIREMENTS IN MEMORY EXPANSION MODE AND MICROPROCESSOR MODE

(V_{CC} = 4.0 to 5.5V, V_{SS} = 0V, T_a = −20 to 85℃, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ	Max	
$t_{su(\overline{ONW}-\phi)}$	$\overline{\text{ONW}}$ input set up time	−20			ns
$t_{h(\phi-\overline{ONW})}$	$\overline{\text{ONW}}$ input hold time	−20			ns
$t_{su(DB-\phi)}$	Data bus set up time	60			ns
$t_{h(\phi-DB)}$	Data bus hold time	0			ns

SWITCHING CHARACTERISTICS IN MEMORY EXPANSION MODE AND MICROPROCESSOR MODE

(V_{CC} = 4.0 to 5.5V, V_{SS} = 0V, T_a = −20 to 85℃, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
$t_{c(\phi)}$	ϕ clock cycle time		$2 \times t_{c(X_{IN})}$		ns
$t_{WH(\phi)}$	ϕ clock "H" pulse width	$t_{c(X_{IN})}-10$			ns
$t_{WL(\phi)}$	ϕ clock "L" pulse width	$t_{c(X_{IN})}-10$			ns
$t_{d(\phi-AH)}$	AD_{15} to AD_8 delay time		20	40	ns
$t_{v(\phi-AH)}$	AD_{15} to AD_8 valid time	6	10		ns
$t_{d(\phi-AL)}$	AD_7 to AD_0 delay time		25	45	ns
$t_{v(\phi-AL)}$	AD_7 to AD_0 valid time	6	10		ns
$t_{d(\phi-SYNC)}$	SYNC delay time		20		ns
$t_{v(\phi-SYNC)}$	SYNC valid time		10		ns
$t_{d(\phi-\overline{WR})}$	$\overline{\text{RD}}$ and $\overline{\text{WR}}$ delay time		10	20	ns
$t_{v(\phi-\overline{WR})}$	$\overline{\text{RD}}$ and $\overline{\text{WR}}$ valid time	3	5	10	ns
$t_{d(\phi-DB)}$	Data bus delay time		20	70	ns
$t_{v(\phi-DB)}$	Data bus valid time	15			ns
$t_{d(\overline{RESET}-\overline{RESET_{OUT}})}$	$\overline{\text{RESET}_{\text{OUT}}}$ output delay time (Note 1)			200	ns
$t_{v(\phi-\overline{RESET})}$	$\overline{\text{RESET}_{\text{OUT}}}$ output valid time (Note 1)	0		200	ns

Note 1 : The $\overline{\text{RESET}_{\text{OUT}}}$ output goes "H" in sync with the rise of the ϕ clock that is anywhere between about 1 cycle and 19 cycles after the RESET input goes "H"

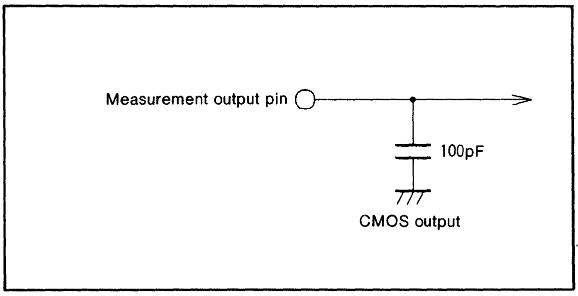
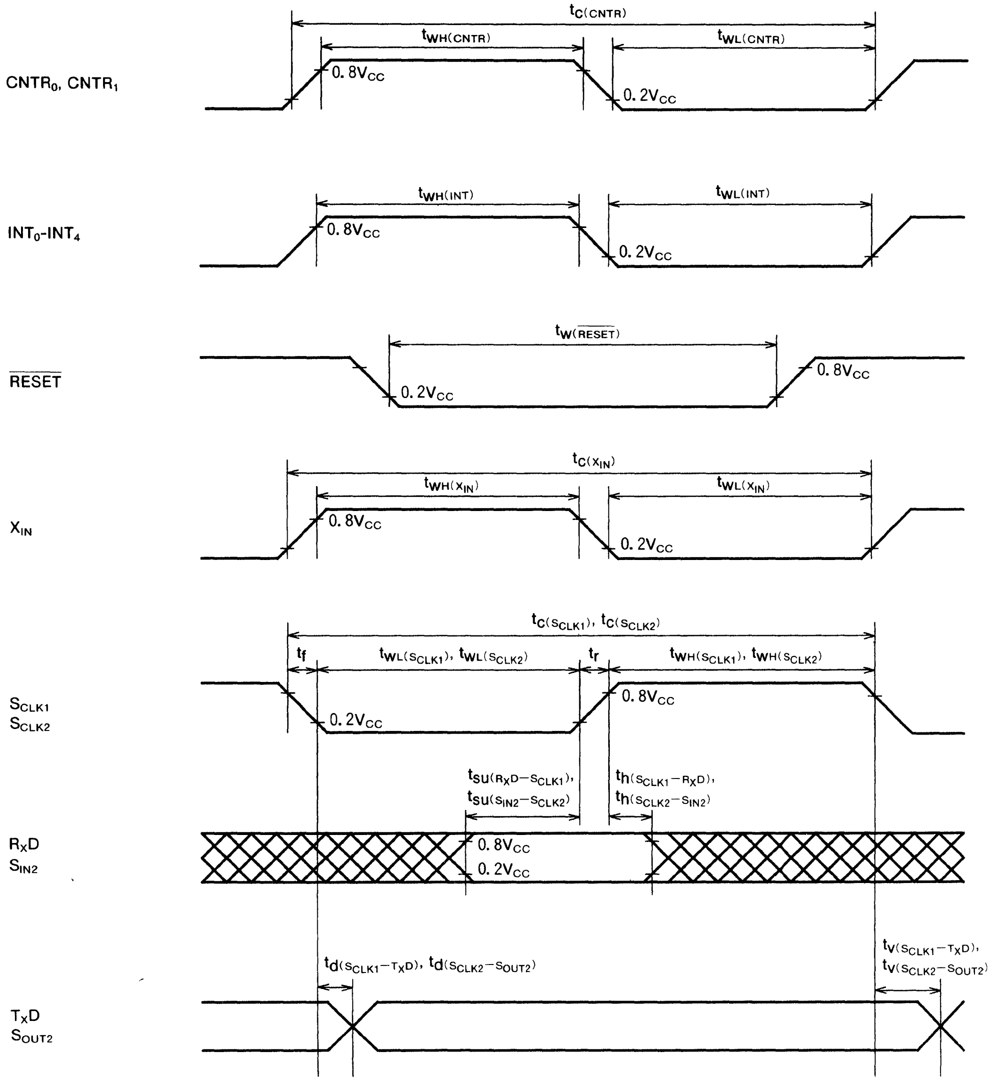


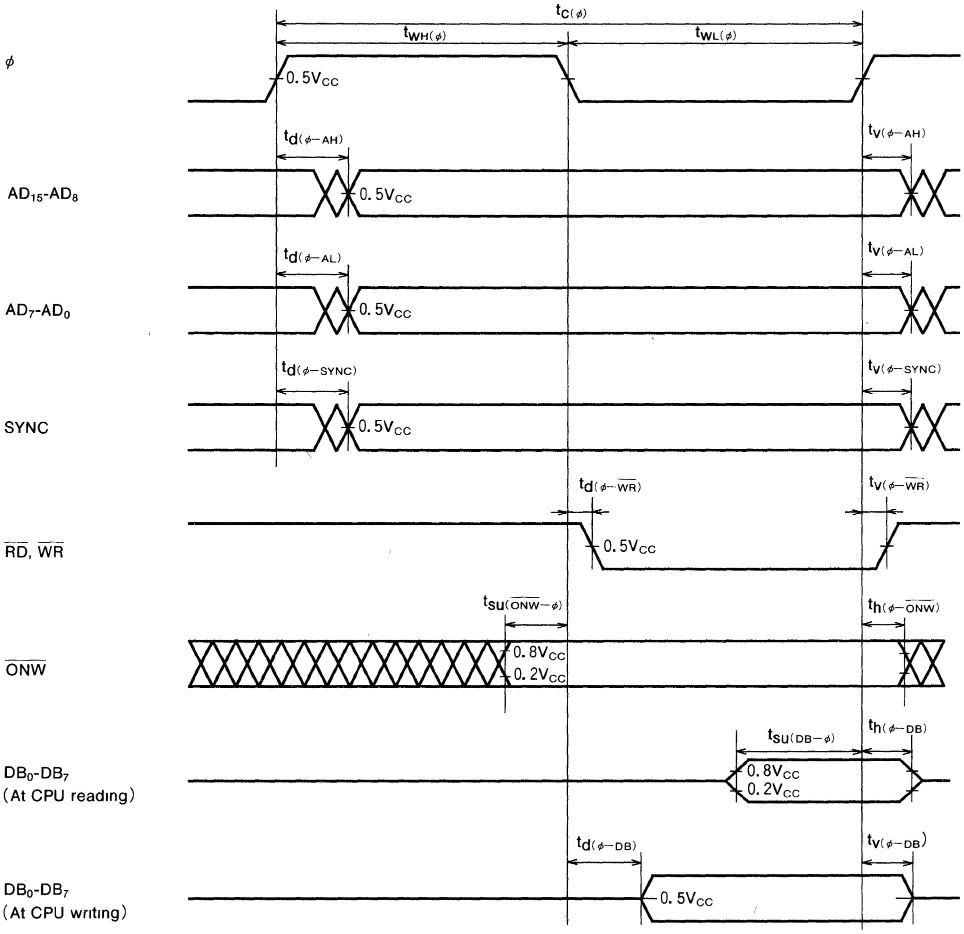
Fig. 33 Circuit for measuring output switching characteristics (2)

TIMING DIAGRAM

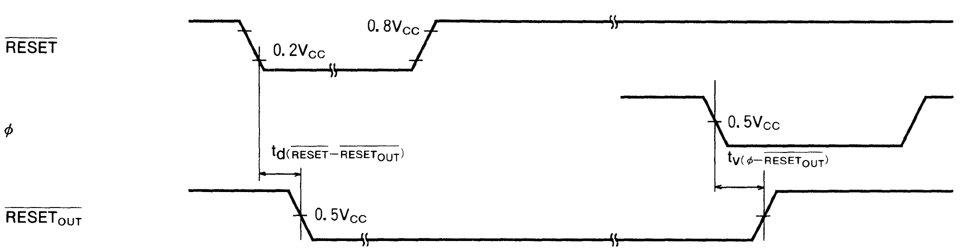
(1) Timing diagram



(2) Timing diagram in memory expansion mode and microprocessor mode



(3) Timing diagram in microprocessor mode



MITSUBISHI MICROCOMPUTERS

M3810x Group

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

DESCRIPTION

The M3810x group is made up of 8-bit microcomputers based on the MELPS 740 core.

The M3810x group is designed mainly for VCR control, and include four 8-bit timers, a PWM function, and a 4-bit comparator circuit.

The various microcomputers in the M3810x group include variations of internal memory size and packaging. For details, see the section on part numbering.

For details on availability of microcomputers in the M3810x group, see the section on group expansion.

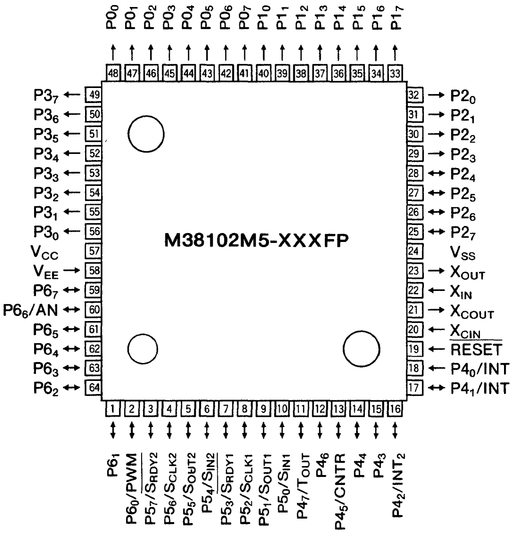
FEATURES

- Basic machine-language instructions ························ 71
- Instruction execution time ································ 0.95μs
  (shortest instruction at 4.19MHz oscillation frequency)
- Memory size
  ROM ··· 4K to 32K bytes
  RAM ·· 192 to 1024 bytes
- Programmable input/output ports ··························· 27
- High-breakdown-voltage output ports ······················ 28
- Interrupts ································ 11 sources, 11 vectors
- Timers ··· 8-bit×4
- Serial I/O ··················· 8-bit×2 (Clock-synchronized)
- PWM output circuit ······································ 14-bit×1
- Comparator circuit ······································· 4-bit×1
- 2 Clock generation circuit
  Clock (X_{IN}-X_{OUT}) ················ Internal feedback amplifier
  Sub clock (X_{CIN}-X_{COUT}) ······ Internal amplifier without feedback
- Supply voltage ·· 4.0 to 5.5V
- Low power dissipation
  In high-speed operation ···································· 25mW
  (at 4.19MHz oscillation frequency)
  In low-speed operation ···································· 300μW
  (at 32kHz oscillation frequency)
- Operating temperature range ················· −10 to +85℃

APPLICATIONS

VCRs, tuners, musical instruments, office automation, etc.

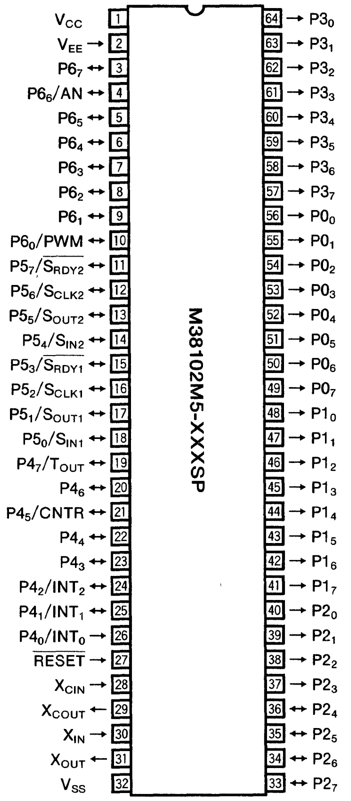
PIN CONFIGURATION (TOP VIEW)



Package type : 64P6N

64-pin plastic-molded QFP

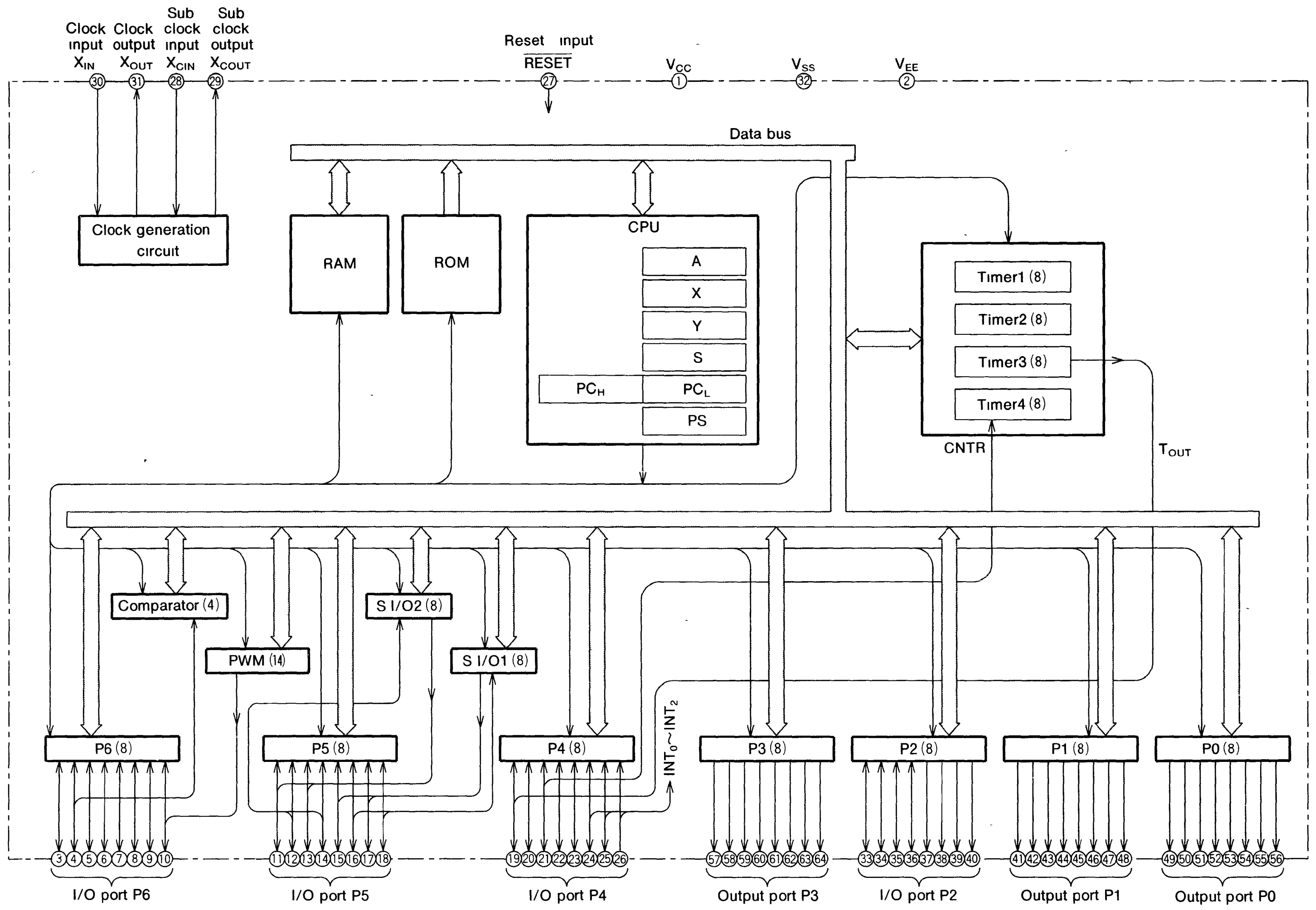
PIN CONFIGURATION (TOP VIEW)



Package type : 64P4B

64-pin shrink plastic-molded DIP

FUNCTIONAL BLOCK DIAGRAM (Package : 64P4B)



PIN DESCRIPTION

Pin	Name	Function	Alternate Function
V_{CC}, V_{SS}	Power supply	Power supply inputs 4 0 to 5 5V to V_{CC}, and 0V to V_{SS}.	
V_{EE}	Pull-down power input	Applies voltage supplied to pull-down resistors of ports P0, P1, $P2_0$-$P2_3$, and P3	
$\overline{RESET}$	Reset input	To reset the microcomputer, this pin should be kept at an "L" level for more than $2\mu s$ under high-speed operating conditions In low-speed operation start mode, internal reset is not released until the X_{CIN}-X_{COUT} clock has had time to stabilize	
X_{IN}	Clock input	Input and output signals for the internal clock generation circuit It consist of internal feedback amplifier Connect a ceramic resonator or quartz crystal between the X_{IN} and X_{OUT} pins to set the oscillation frequency If an external clock is used, connect the clock source to the X_{IN} pin and leave the X_{OUT} pin open This clock is used as system clok	
X_{OUT}	Clock output		
X_{CIN}	Sub clock input	Input and output signals for the internal sub clock generation circuit It consist of internal amplifier without feedback Connect a ceramic resonator or quartz crystal and external feedback resistor between the X_{CIN} and X_{COUT} pins If an external clock is used, connect the clock source to the X_{CIN} pin and leave the X_{COUT} pin open This clock can also be used as the system clock	
X_{COUT}	Sub clock output		
$P0_0$-$P0_7$	Output port P0	8-bit output port The output structure is high-breakdown-voltage P-channel open drain with internal pull-down resistors connected between the output and the V_{EE} pin	
$P1_0$-$P1_7$	Output port P1		
$P2_0$-$P2_3$	Output port P2	A 4-bit output port with the same function as port P0.	
$P2_4$-$P2_7$	I/O port P2	A 4-bit I/O port An I/O direction register allows each pin to be individually programmed as either input or output At reset this port is set to input mode The output structure of this port is CMOS 3-state, and the input levels are TTL compatible.	
$P3_0$-$P3_7$	Output port P3	An 8-bit output port with the same function as port P0	
$P4_0/INT_0$	Input port $P4_0$	1-bit CMOS input pin	External interrupt input pins
$P4_1/INT_1$, $P4_2/INT_2$	I/O port P4	A 7-bit CMOS I/O port with the same function as port $P2_4$-$P2_7$, with CMOS compatible input levels.	
$P4_3$, $P4_4$			
$P4_5$/CNTR			Event counter input pin
$P4_6$			
$P4_7/T_{OUT}$			Timer output pin
$P5_0/S_{IN1}$, $P5_1/S_{OUT1}$, $P5_2/S_{CLK1}$, $P5_3/\overline{S_{RDY1}}$	I/O port P5	An 8-bit CMOS I/O port with the same function as port $P2_4$-$P2_7$ The output structure of this port is N-channel open drain, and the input levels are CMOS compatible Keep the input voltage of this port between 0V and V_{CC}	Serial I/O1 I/O pins
$P5_4/S_{IN2}$, $P5_5/S_{OUT2}$, $P5_6/S_{CLK2}$, $P5_7/\overline{S_{RDY2}}$			Serial I/O2 I/O pins
$P6_0$/PWM	I/O port P6	An 8-bit CMOS I/O port with the same function as port $P2_4$-$P2_7$, with CMOS compatible input levels	14-bit PWM output pin
$P6_1$-$P6_5$			
$P6_6$/AN			Comparator input pin
$P6_7$			

PART NUMBERING

Product name M3810 2 M 5 - XXX SP

Package type
- SP : 64P4B package
- FP : 64P6N package
- SS : 64S1B package
- FS : 64D0 package

ROM number
- Omitted in some types

ROM/PROM size
- 1 4096 bytes
- 2 : 8192 bytes
- 3 : 12288 bytes
- 4 : 16384 bytes
- 5 . 20480 bytes
- 6 24576 bytes
- 7 · 28672 bytes
- 8 · 32768 bytes

The first 128 bytes and the last two bytes of ROM are reserved areas, they can not be used

Memory type
- M : Mask ROM version
- E : EPROM or one-time programmable version

RAM size
- 0 192 bytes
- 1 256 bytes
- 2 384 bytes
- 3 512 bytes
- 4 640 bytes
- 5 768 bytes
- 6 896 bytes
- 7 1024 bytes

GROUP EXPANSION

Mitsubishi plans to expand the M3810x group as follows:

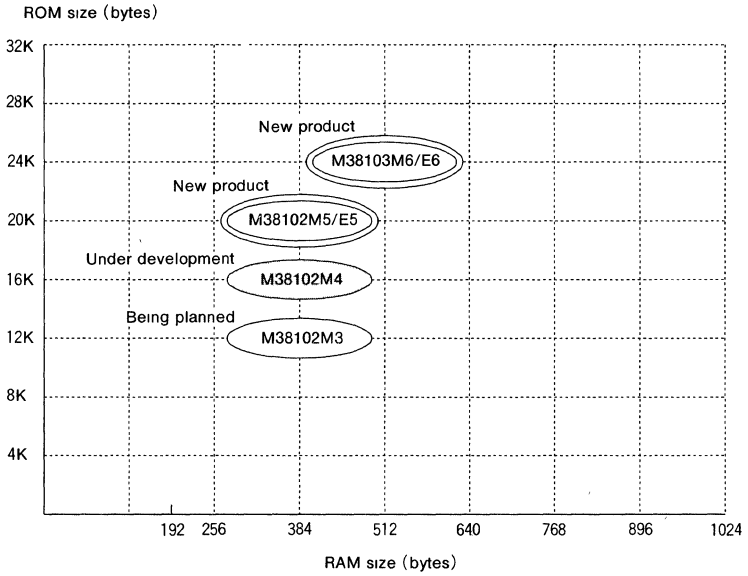
(1) Support for mask ROM, one-time programmable, and EPROM versions

ROM/PROM capacity ························ 12K-24K bytes
RAM capacity ···································· 384-512 bytes

(2) Packages

64P4B	Shrink plastic molded DIP
64P6N	Plastic molded QFP
64S1B	Shrink ceramic DIP
64D0	Ceramic LCC

Memory expansion plan



The development schedule and other details of products under development may be revised without notice
Currently supported products are listed below

As of March 1992

Product name	(P) ROM size (bytes)	RAM size (bytes)	Package	Remarks
M38102M5-XXXSP	20K	384	64P4B	Mask ROM version
M38102E5-XXXSP				One-time programmable version
M38102E5SP				One-time programmable version (blank)
M38102M5-XXXFP			64P6N	Mask ROM version
M38102E5-XXXFP				One-time programmable version
M38102E5FP				One-time programmable version (blank)
M38102E5SS			64S1B	EPROM version
M38102E5FS			64D0	EPROM version
M38103M6-XXXSP	24K	512	64P4B	Mask ROM version
M38103E6-XXXSP				One-time programmable version
M38103E6SP				One-time programmable version (blank)
M38103M6-XXXFP			64P6N	Mask ROM version
M38103E6-XXXFP				One-time programmable version
M38103E6FP				One-time programmable version (blank)
M38103E6SS			64S1B	EPROM version
M38103E6FS			64D0	EPROM version

FUNCTIONAL DESCRIPTION

CENTRAL PROCESSING UNIT (CPU)

Microcomputers of the M3810x group use the standard MELPS 740 instruction set. Refer to the table of MELPS 740 addressing modes and machine instructions or the MELPS 740 Software Manual for details on the instruction set.

Machine-resident MELPS 740 instructions are as follows:
The FST and SLW instructions are not available for use.
The STP, WIT, MUL, and DIV instructions can be used.

CPU MODE REGISTER

The CPU mode register is allocated to address $003B_{16}$.

Bits 0 and 1 of this register are processor mode bits and should always be set to "0".

The CPU mode register contains the stack page selection bit.

For details of the X_{COUT} drivability selection bit, main clock stop bit, and internal system clock selection bit, see the section on the clock generation circuit.

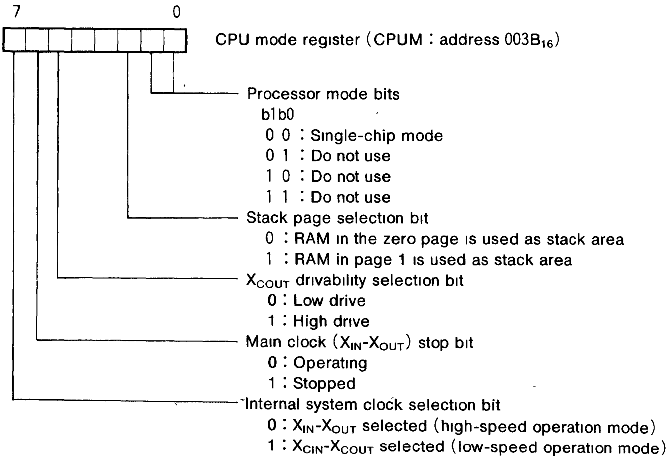


Fig. 1 Structure of CPU mode register

MEMORY

Special Function Register (SFR) Area

The Special Function Register area contains registers which control functions such as I/O ports and timers, and is located in the zero page area.

RAM

RAM is used for data storage as well for stack area.

ROM

The first 128 bytes and the last two bytes of ROM are reserved for device testing and the rest is user area for storing programs.

Interrupt Vector Area

The interrupt vector area contains reset and interrupt vectors.

Zero Page

The 256 bytes from addresses 0000_{16} to $00FF_{16}$ are called the zero page area. The internal RAM and the special function registers (SFR) are allocated to this area.

The zero page addressing mode can be used to specify memory and register addresses in the zero page area. This dedicated zero page addressing mode enables access to this area with only 2 bytes.

Special Page

The 256 bytes from addresses $FF00_{16}$ to $FFFF_{16}$ are called the special page area. The special page addressing mode can be used to specify memory addresses in the special page area. This dedicated special page addressing mode enables access to this area with only 2 bytes.

RAM area

RAM capacity (bytes)	Address $XXXX_{16}$
192	$00FF_{16}$
256	$013F_{16}$
384	$01BF_{16}$
512	$023F_{16}$
640	$02BF_{16}$
768	$033F_{16}$
896	$03BF_{16}$
1024	$043F_{16}$

ROM area

ROM capacity (bytes)	Address $YYYY_{16}$	Address $ZZZZ_{16}$
4096	$F000_{16}$	$F080_{16}$
8192	$E000_{16}$	$E080_{16}$
12288	$D000_{16}$	$D080_{16}$
16384	$C000_{16}$	$C080_{16}$
20480	$B000_{16}$	$B080_{16}$
24576	$A000_{16}$	$A080_{16}$
28672	9000_{16}	9080_{16}
32768	8000_{16}	8080_{16}

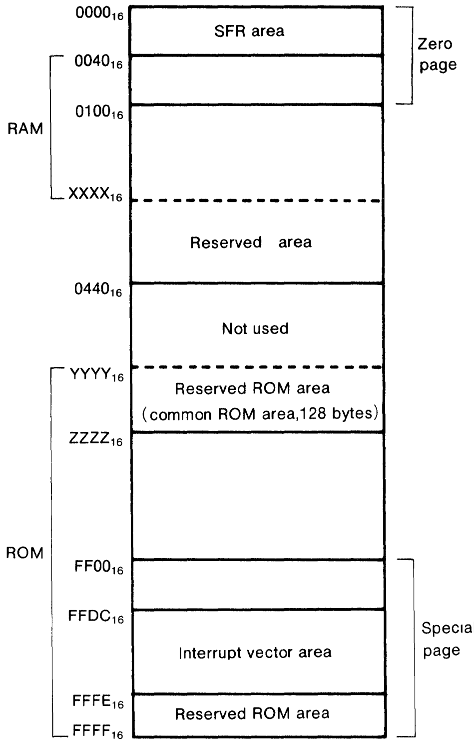


Fig. 2 Memory map diagram

0000_{16}	Port P0 (P0)	0020_{16}	
0001_{16}		0021_{16}	
0002_{16}	Port P1 (P1)	0022_{16}	
0003_{16}		0023_{16}	
0004_{16}	Port P2 (P2)	0024_{16}	Timer 1 (T1)
0005_{16}	Port P2 direction register (P2D)	0025_{16}	Timer 2 (T2)
0006_{16}	Port P3 (P3)	0026_{16}	Timer 3 (T3)
0007_{16}		0027_{16}	Timer 4 (T4)
0008_{16}	Port P4 (P4)	0028_{16}	Timer 12 mode register (T12M)
0009_{16}	Port P4 direction register (P4D)	0029_{16}	Timer 34 mode register (T34M)
$000A_{16}$	Port P5 (P5)	$002A_{16}$	
$000B_{16}$	Port P5 direction register (P5D)	$002B_{16}$	PWM control register (PWMCON)
$000C_{16}$	Port P6 (P6)	$002C_{16}$	PWM register (upper)(PWMH)
$000D_{16}$	Port P6 direction register (P6D)	$002D_{16}$	PWM register (lower)(PWML)
$000E_{16}$		$002E_{16}$	
$000F_{16}$		$002F_{16}$	
0010_{16}		0030_{16}	Comparator register (CMP)
0011_{16}		0031_{16}	
0012_{16}		0032_{16}	
0013_{16}		0033_{16}	
0014_{16}		0034_{16}	
0015_{16}		0035_{16}	
0016_{16}		0036_{16}	
0017_{16}		0037_{16}	
0018_{16}		0038_{16}	High-breakdown-voltage port control register (HVPC)
0019_{16}	Serial I/O1 control register (SIO1CON)	0039_{16}	
$001A_{16}$		$003A_{16}$	Interrupt edge selection register (INTEDGE)
$001B_{16}$	Serial I/O1 register (SIO1)	$003B_{16}$	CPU mode register (CPUM)
$001C_{16}$		$003C_{16}$	Interrupt request register 1 (IREQ1)
$001D_{16}$	Serial I/O2 control register (SIO2CON)	$003D_{16}$	Interrupt request register 2 (IREQ2)
$001E_{16}$		$003E_{16}$	Interrupt control register 1 (ICON1)
$001F_{16}$	Serial I/O2 register (SIO2)	$003F_{16}$	Interrupt control register 2 (ICON2)

Fig. 3 Memory map of special function register (SFR)

I/O PORTS

Direction Registers

The M3810x group microprocessors have 27 programmable I/O pins arranged in four I/O ports (ports $P2_4$~$P2_7$, $P4_1$~$P4_7$, P5, and P6). The I/O ports have direction registers which determine the input/output direction of each individual pin. Each bit in a direction register corresponds to one pin, each pin can be set to be input or output.

When "0" is written to the bit corresponding to a pin, that pin becomes an input pin. When "1" is written to that bit, that pin becomes an output pin.

If data is read from a pin which is set for output, the value of the port output latch is read, not the value of the pin itself. Pins set to input are floating. If a pin set to input is written to, only the port output latch is written to and the pin remains floating.

High-Breakdown-Voltage Output Ports

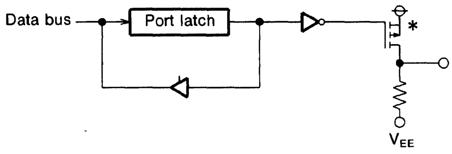
The M3810x group microprocessors have four ports with high-breakdown-voltge pins (ports P0, P1, $P2_0$~$P2_3$, and P3). The high-breakdown-voltage ports have P-channel open drain output with a breakdown voltage of $V_{CC}-40V$. Each pin has an internal pull-down resistor connected to V_{EE}. At reset, the P-channel output transistor of each port latch is turned off, so it is forced to the level of V_{EE} by the pull-down resistor.

Writing "1" to bit 0 of the high-breakdown-voltage port control register (address 0038_{16}) slows the transition of the output transistors to reduce transient noise. At reset, bit 0 of the high-breakdown-voltage port control register is set to "0" (strong drive).

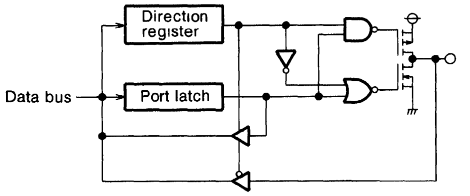
Pin	Name	Input/Output	I/O Format	Non-Port Function	Related SFRs	Diagram No
$P0_0$-$P0_7$	Port P0	Output	High-breakdown-voltage P-channel open-drain output with pull-down resistor		High-breakdown-voltage port control register	(1)
$P1_0$-$P1_7$	Port P1	Output	High-breakdown-voltage P-channel open-drain output with pull-down resistor		High-breakdown-voltage port control register	
$P2_0$-$P2_3$	Port P2	Output	High-breakdown-voltage P-channel open-drain output with pull-down resistor		High-breakdown-voltage port control register	
$P2_4$-$P2_7$		Input/output, individual bits	TTL level input CMOS 3-state output			(2)
$P3_0$-$P3_7$	Port P3	Output	High-breakdown-voltage P-channel open-drain output with pull-down resistor		High-breakdown-voltage port control register	(1)
$P4_0/INT_0$	Port P4	Input	CMOS level input	External interrupt input	Interrupt edge selection register	(3)
$P4_1/INT_1$, $P4_2/INT_2$		Input/output, individual bits	CMOS level input CMOS 3-state output			(4)
$P4_3$, $P4_4$						(2)
$P4_5$/CNTR				Event counter input	Timer 34 mode register	(4)
$P4_6$						(2)
$P4_7/T_{OUT}$				Timer 3 output	Timer 34 mode register	(5)
$P5_0/S_{IN1}$,	Port P5	Input/output, individual bits	CMOS level input N-channel open-drain output	Serial I/O1 function I/O	Serial I/O1 control register	(6)
$P5_1/S_{OUT1}$, $P5_2/S_{CLK1}$,						(7)
$P5_3/\overline{S_{RDY1}}$						(8)
$P5_4/S_{IN2}$,				Serial I/O2 function I/O	Serial I/O2 control register	(6)
$P5_5/S_{OUT2}$, $P5_6/S_{CLK2}$,						(7)
$P5_7/\overline{S_{RDY2}}$						(8)
$P6_0$/PWM	Port P6	Input/output, individual bits	CMOS level input CMOS 3-state output	14-bit PWM output	PWM control register PWML register PWMH register	(9)
$P6_1$-$P6_5$						(2)
$P6_6$/AN				Comparator input	Comparator register	(10)
$P6_7$						(2)

Note Make sure that the input level at each pin is either 0V or V_{CC} during execution of the STP instruction.
If an input level is at an intermediate potential, a current will flow in the input-stage gate

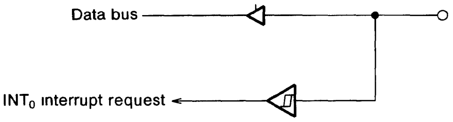
(1) Port P0, P1, $P2_0$~ $P2_3$, P3



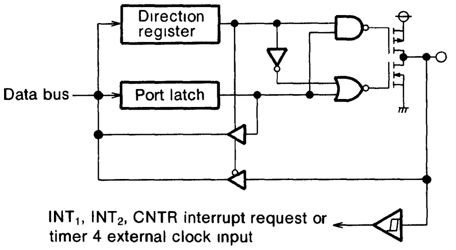
(2) Port $P2_4$~ $P2_7$, $P4_3$, $P4_4$, $P4_6$, $P6_1$~ $P6_5$, $P6_7$



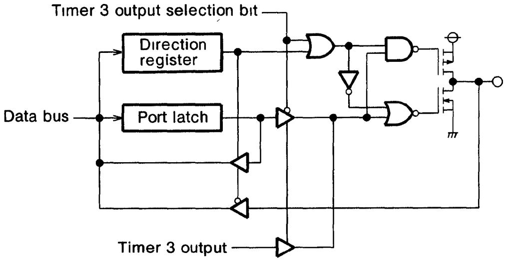
(3) Port $P4_0$



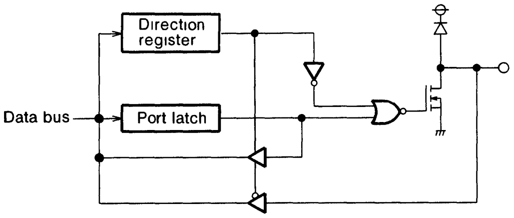
(4) Port $P4_1$, $P4_2$, $P4_5$



(5) Port $P4_7$



(6) Port $P5_0$, $P5_4$



* High-breakdown-voltage P-channel transistor

Fig. 4 Port block diagram (1)

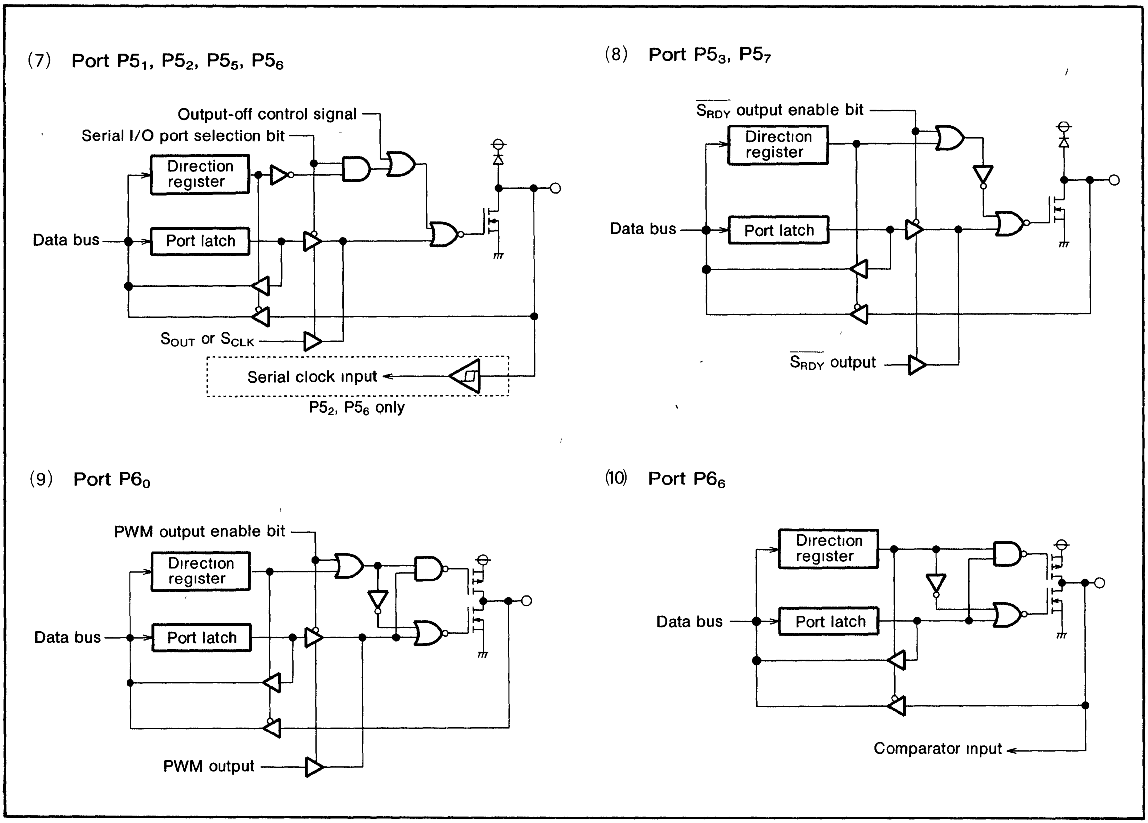


Fig. 5 Port block diagram (2)

INTERRUPTS

A total of 11 sources can generate interrupts: 4 external, 6 internal, and 1 software.

Interrupt Control

Each interrupt is controlled by an interrupt request bit, an interrupt enable bit, and the interrupt disable flag-except for the software interrupt set by the BRK instruction. An interrupt is generated if the corresponding interrupt request and enable bits are "1" and the interrupt disable flag is "0".
Interrupt enable bits can be set or cleared by software.
Interrupt request bits can be cleared by software, but cannot be set by software.
The I flag disables all interrupts except for the BRK instruction interrupt.

Interrupt Operation

When an interrupt is received, the program counter and processor status register are automatically pushed onto the stack. The interrupt disable flag is set to inhibit other interrupts from interfering. The corresponding interrupt request bit is cleared and the interrupt jump destination address is read from the vector table into the program counter.

Notes on Use

If you will change interrupt edge selection from rising edge to falling edge, interrupt request bit will be set to "1" automatically. Therefore, please make following process;

(1) Disable INT which is selected.
(2) Change INT edge selection.
(3) Clear interrupt request which is selected.
(4) Enable INT which is selected.

Table 1. Interrupt vector addresses and priorities

Interrupt cause	Priority	Vector address (Note 1)		Interrupt request generation conditions	Remarks
		High	Low		
Reset (Note 2)	1	$FFFD_{16}$	$FFFC_{16}$	At reset	Non-maskable
INT_0	2	$FFFB_{16}$	$FFFA_{16}$	At detection of either rising or falling edge of INT_0 input	External interrupt (active edge selectable)
INT_1	3	$FFF9_{16}$	$FFF8_{16}$	At detection of either rising or falling edge of INT_1 input	External interrupt (active edge selectable)
INT_2	4	$FFF7_{16}$	$FFF6_{16}$	At detection of either rising or falling edge of INT_2 input	External interrupt (active edge selectable)
Serial I/O1	5	$FFF5_{16}$	$FFF4_{16}$	At end of serial I/O1 data transfer	Valid when serial I/O1 is selected
Serial I/O2	6	$FFF3_{16}$	$FFF2_{16}$	At end of serial I/O2 data transfer	Valid when serial I/O2 is selected
Timer 1	7	$FFF1_{16}$	$FFF0_{16}$	At timer 1 overflow	
Timer 2	8	$FFEF_{16}$	$FFEE_{16}$	At timer 2 overflow	STP release timer overflow
Timer 3	9	$FFED_{16}$	$FFEC_{16}$	At timer 3 overflow	
Timer 4	10	$FFEB_{16}$	$FFEA_{16}$	At timer 4 overflow	
CNTR	11	$FFE9_{16}$	$FFE8_{16}$	At detection of either rising or falling edge of CNTR input	External interrupt (active edge selectable)
BRK instruction	12	$FFDD_{16}$	$FFDC_{16}$	At BRK instruction execution	Non-maskable software interrupt

Note 1 Vector addresses contain interrupt jump destination addresses
2 Reset function in the same way as an interrupt with the highest priority

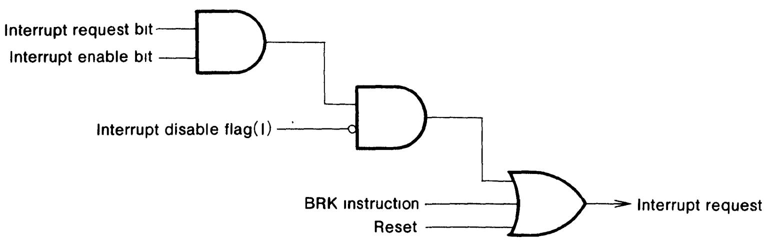


Fig. 6 Interrupt control

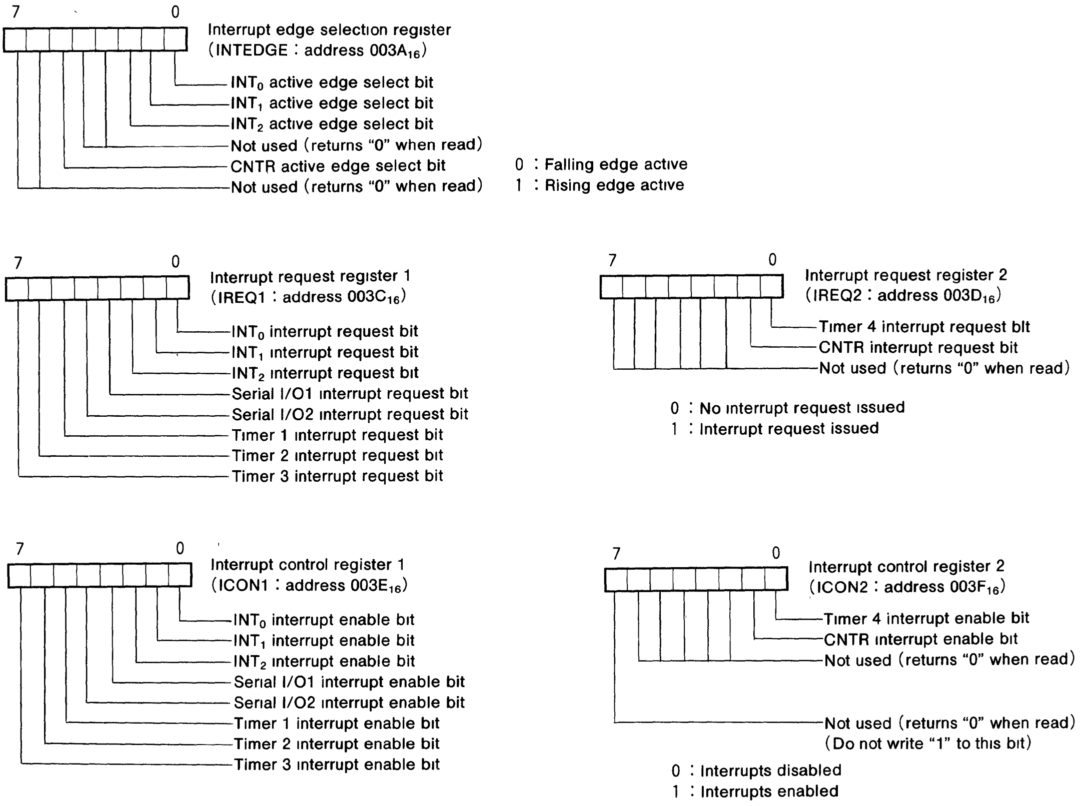


Fig. 7 Structure of interrupt-related registers

TIMERS

Microcomputers of the M3810x group have four built-in timers. The timers count down. Once a timer reaches 00_{16}, the next count pulse loads the contents of the corresponding timer latch into the timer, and sets the corresponding interrupt request bit to 1. Each timer also has a stop bit that stops the count of that timer when it is set to “1” .

Note that the system clock ϕ can be set to either high-speed mode or low-speed mode by the CPU mode register.

Timer 1 and Timer 2

The count sources of timer 1 and timer 2 can be selected by setting the timer 12 mode register.

When the chip is reset or the STP instruction is executed, all bits of the timer 12 mode register are cleared, timer 1 is set to FF_{16}, and timer 2 is set to 01_{16}.

Timer 3 and Timer 4

The count sources of timer 3 and timer 4 can be selected by setting the timer 34 mode register.

Timer 3 can also output a rectangular waveform from the $P4_7$/T_{OUT} pin. The waveform changes polarity each time timer 3 overflows.

When timer 4 is assigned to external event count mode, rising edge is active.

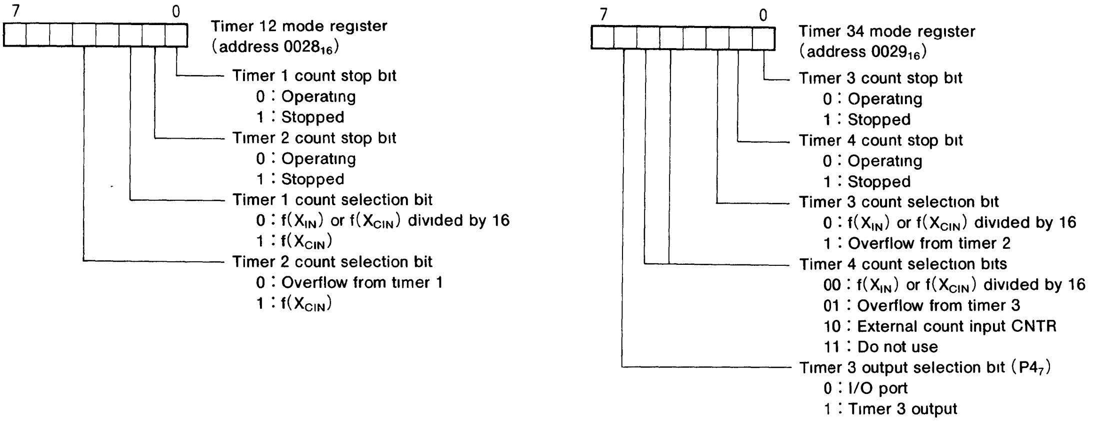


Fig. 8 Structure of timer-related registers

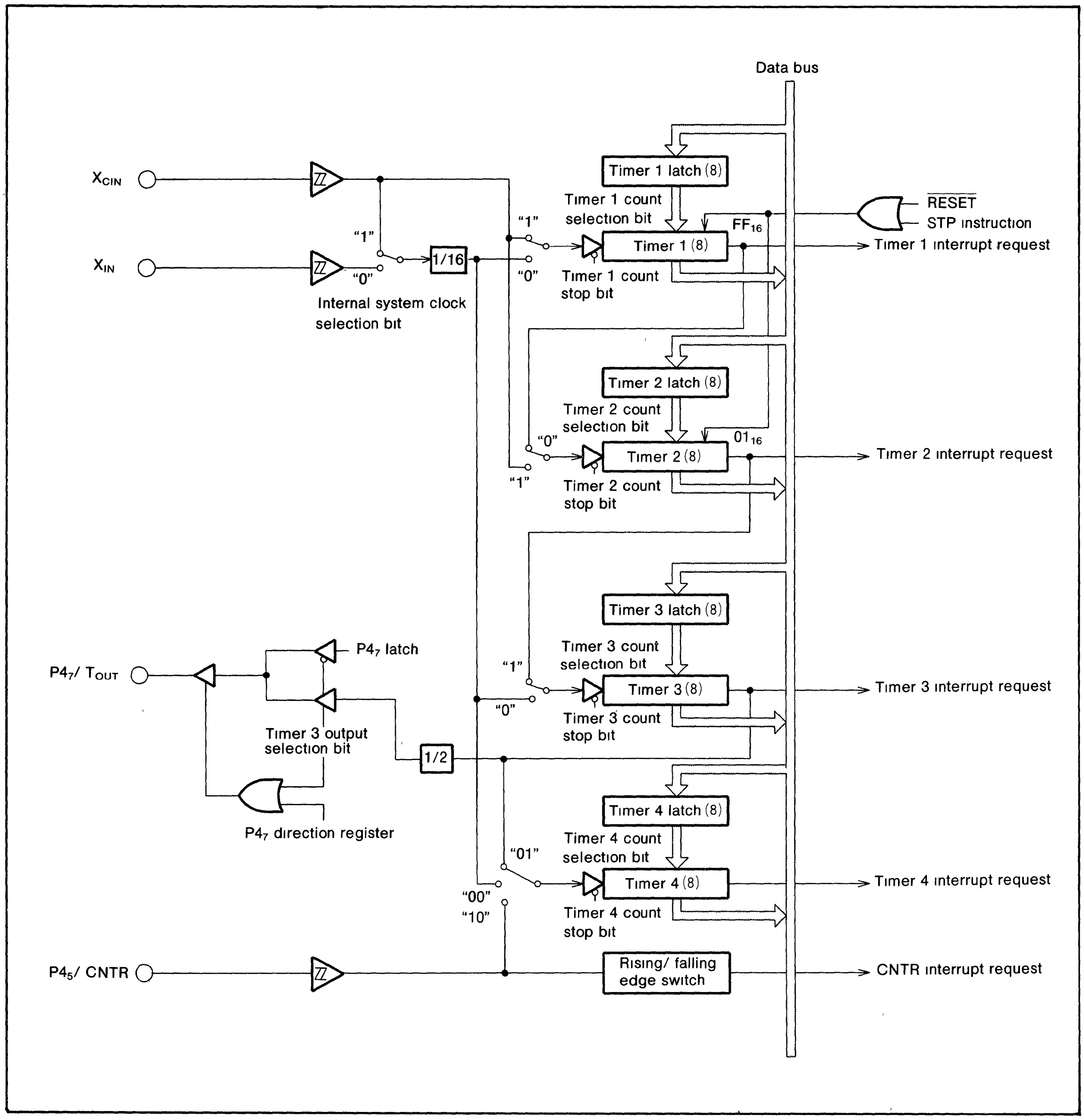


Fig. 9 Timer block diagram

SERIAL I/O

Microcomputers of the M3810x group have two built-in 8-bit clock synchronized serial I/O channels (serial I/O1 and serial I/O2).

Serial I/O1 has the same function as serial I/O2.

The I/O pins of the serial I/O function also operate as I/O port P5, and their operation is selected by the serial I/O control registers (adresses 0019_{16} and $001D_{16}$).

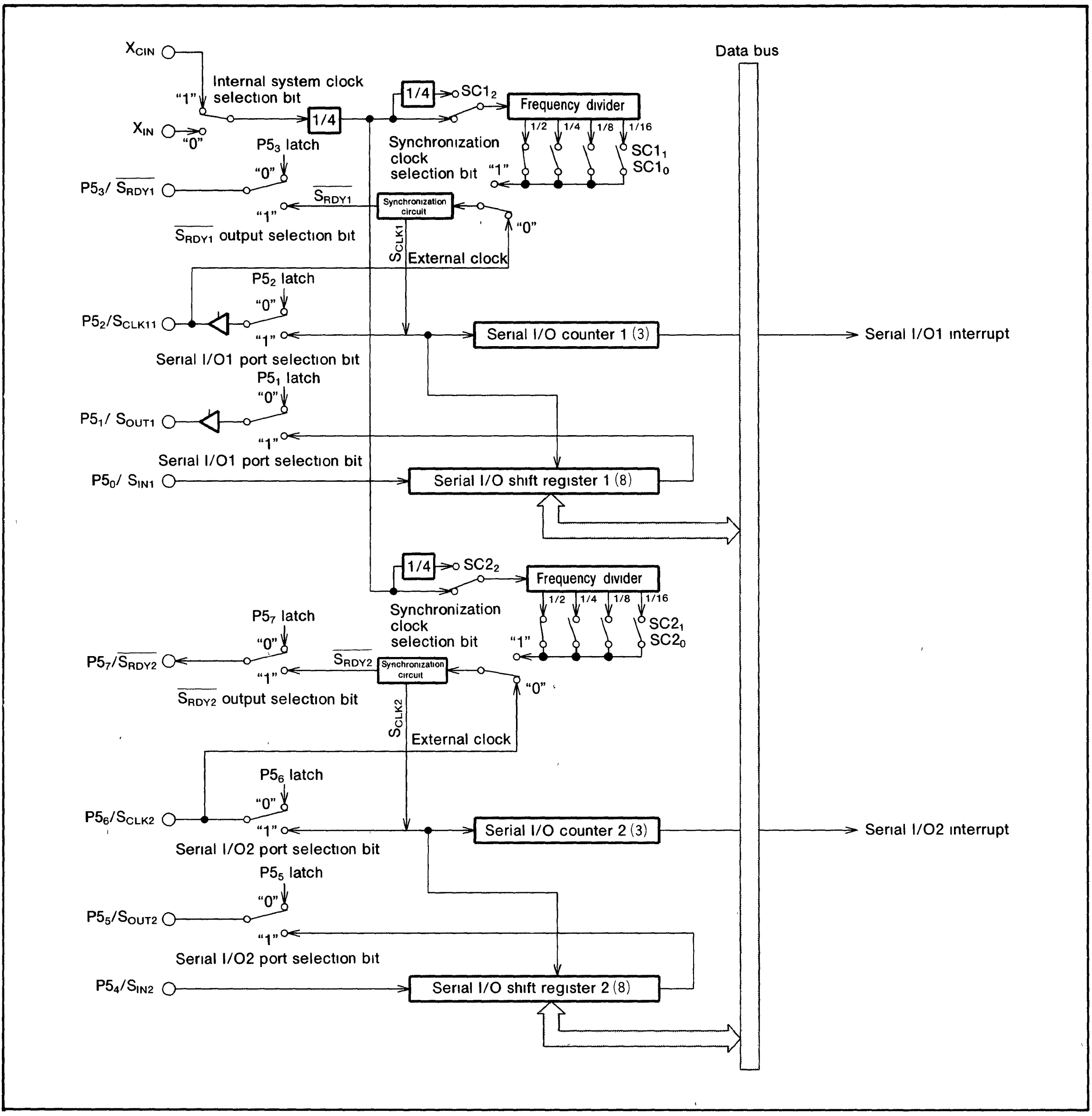
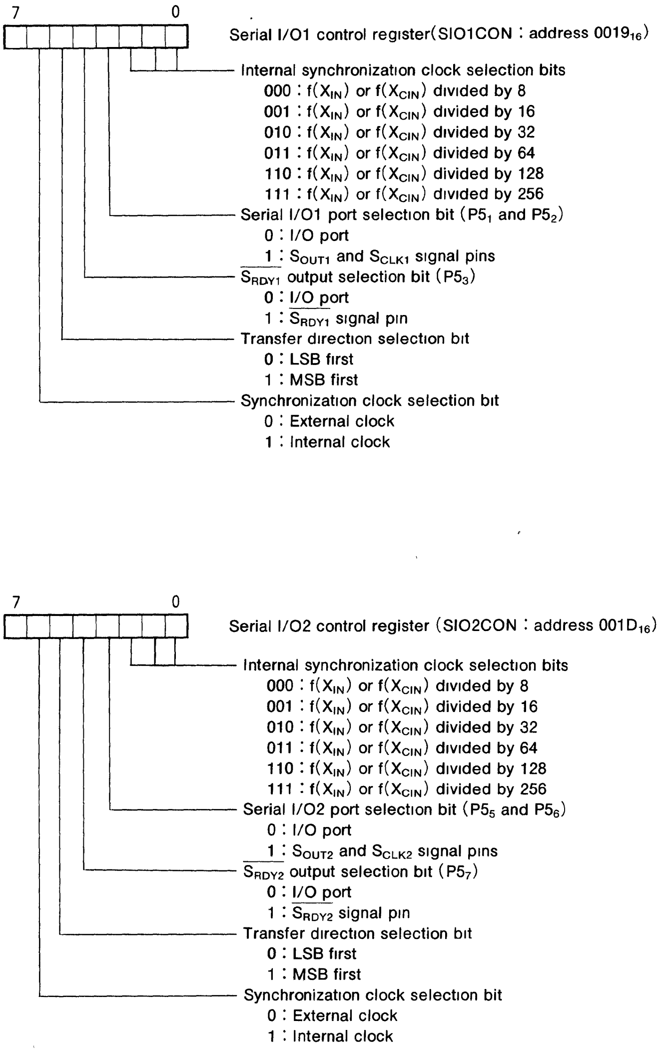


Fig. 10 Serial I/O block diagram

[Serial I/O Control Registers] SIO1CON, SIO2CON
Each of the serial I/O control registers (addresses 0019_{16} and $001D_{16}$) contains seven bits that select various control parameters of the serial I/O function.



Serial I/O1 control register(SIO1CON : address 0019_{16})

Internal synchronization clock selection bits
000 : $f(X_{IN})$ or $f(X_{CIN})$ divided by 8
001 : $f(X_{IN})$ or $f(X_{CIN})$ divided by 16
010 : $f(X_{IN})$ or $f(X_{CIN})$ divided by 32
011 : $f(X_{IN})$ or $f(X_{CIN})$ divided by 64
110 : $f(X_{IN})$ or $f(X_{CIN})$ divided by 128
111 : $f(X_{IN})$ or $f(X_{CIN})$ divided by 256

Serial I/O1 port selection bit ($P5_1$ and $P5_2$)
0 : I/O port
1 : S_{OUT1} and S_{CLK1} signal pins

$\overline{S_{RDY1}}$ output selection bit ($P5_3$)
0 : I/O port
1 : $\overline{S_{RDY1}}$ signal pin

Transfer direction selection bit
0 : LSB first
1 : MSB first

Synchronization clock selection bit
0 : External clock
1 : Internal clock

Serial I/O2 control register (SIO2CON : address $001D_{16}$)

Internal synchronization clock selection bits
000 : $f(X_{IN})$ or $f(X_{CIN})$ divided by 8
001 : $f(X_{IN})$ or $f(X_{CIN})$ divided by 16
010 : $f(X_{IN})$ or $f(X_{CIN})$ divided by 32
011 : $f(X_{IN})$ or $f(X_{CIN})$ divided by 64
110 : $f(X_{IN})$ or $f(X_{CIN})$ divided by 128
111 : $f(X_{IN})$ or $f(X_{CIN})$ divided by 256

Serial I/O2 port selection bit ($P5_5$ and $P5_6$)
0 : I/O port
1 : S_{OUT2} and S_{CLK2} signal pins

$\overline{S_{RDY2}}$ output selection bit ($P5_7$)
0 : I/O port
1 : $\overline{S_{RDY2}}$ signal pin

Transfer direction selection bit
0 : LSB first
1 : MSB first

Synchronization clock selection bit
0 : External clock
1 : Internal clock

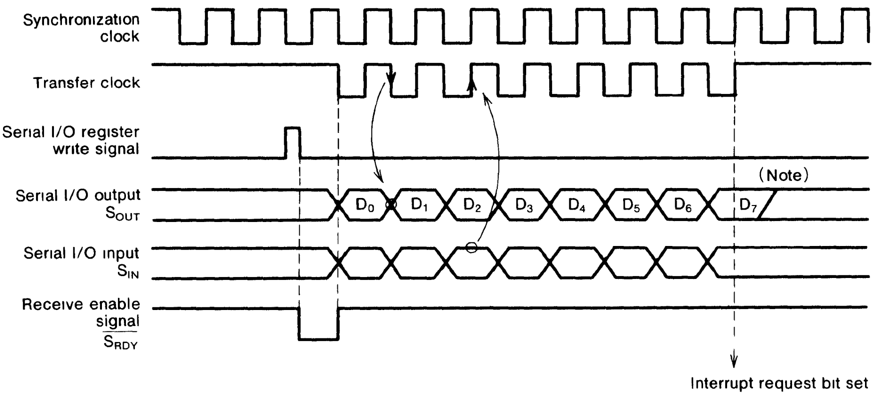
Fig. 11 Structure of serial I/O control registers

Operation In Serial I/O Mode

Either an internal clock or an external clock can be selected as the synchronization clock for serial I/O transfer. A dedicated divider is built-in as the internal clock, giving a choice of six clocks.

If internal clock is selected, transfer start is activated by a write signal to a serial I/O register (address $001B_{16}$ or $001F_{16}$). After eight bits have been transferred, the S_{OUT} pin goes to high impedance.

If external clock is selected, the clock must be controlled externally because the contents of the serial I/O register continue to shift while the transfer clock is input. In this case, note that the S_{OUT} pin does not go to high impedance at the completion of data transfer. The interrupt request bit is set at the end of the transfer of eight bits, regardless of whether the internal or external clock is selected.



Note. If internal clock is selected, the S_{OUT} pin is at high impedance after transfer ends

Fig. 12 Serial I/O timing (for LSB first)

PULSE WIDTH MODULATION (PWM) OUTPUT CIRCUIT

Microcomputers in the M3810x group have a PWM function with a 14-bit resolution. When the oscillation frequency X_{IN} is 4MHz, the minimum resolution bit width is 500ns and the cycle period is 8192μs. The PWM timing generator supplies a PWM control signal based on a signal that is half the frequency of the X_{IN} clock.

The explanation in the rest of this data sheet assumes X_{IN} = 4MHz.

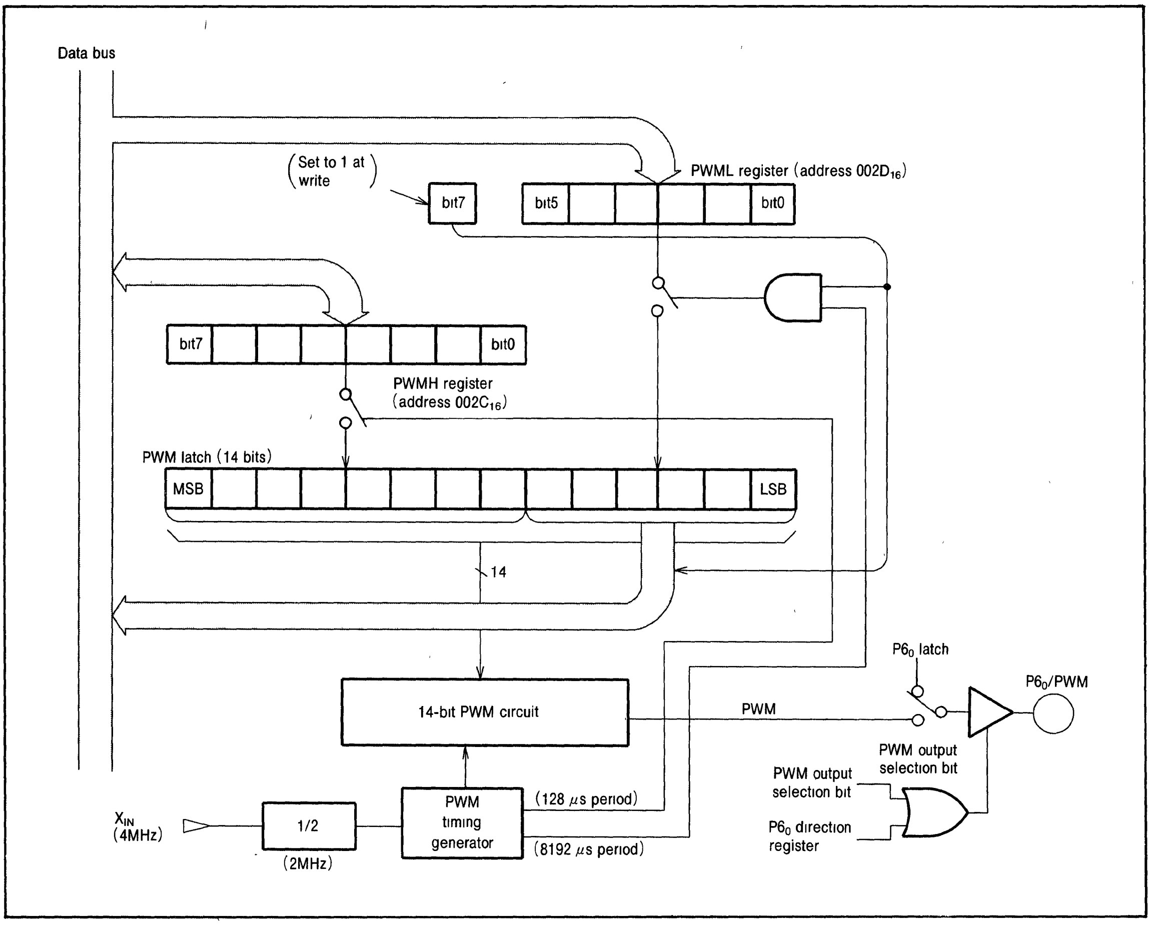


Fig. 13 PWM block diagram

(1) Date Set-up

The PWM output pin also functions as port $P6_0$. Set port $P6_0$ to be the PWM output pin by setting bit 0 of the PWM mode register (address $002B_{16}$). The upper eight bits of output data are set in the upper PWM register PWMH (address $002C_{16}$) and the lower six bits are set in the lower PWM register PWML (address $002D_{16}$).

(2) Transfer From Register to Latch

Date written to the PWML register is transferred to the PWM latch once in each PWM period (every 8192μs), and data written to the PWMH register is transferred to the PWM latch once in each sub-period (every 128μs). When the PWML register is read, the contents of the latch are read. However, bit 7 of the PWML register indicates whether the transfer to the PWM latch is completed; the transfer is completed when bit 7 is "0".

Table 2. Relationship between lower 6 bits of data and period set by the ADD bit

Lower 6 Bits of Data(PWML)	Sub-periods tm Lengthened (m =0 to 63)
0 0 0 0 0 0 (LSB)	None
0 0 0 0 0 1	m=32
0 0 0 0 1 0	m=16, 48
0 0 0 1 0 0	m= 8, 24, 40, 56
0 0 1 0 0 0	m= 4, 12, 20, 28, 36, 44, 52, 60
0 1 0 0 0 0	m= 2, 6, 10, 14, 18, 22, 26, 30, 34, 38, 42, 46, 50, 54, 58, 62
1 0 0 0 0 0	m= 1, 3, 5, 7, ………………, 57, 59, 61, 63

(3) PWM Operation

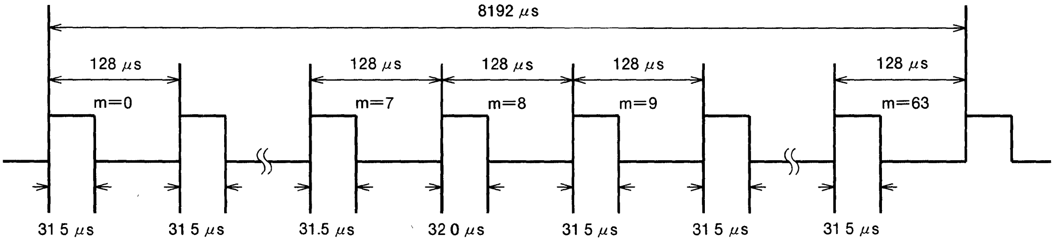
The timing of the 14-bit PWM function is shown in Fig. 16. The 14-bit PWM data is divided into the lower six bits and the upper eight bits in the PWM latch.

The upper eight bits of data determine how long an "H"-level signal is output during each sub-period. There are 64 sub-periods in each period, and each sub-period is 256× τ (128μs) long. The signal is "H" for a length equal to N times τ, where τ is the minimum resolution (500ns).

The contents of the lower six bits of data enable the lengthening of the high signal by τ (500ns). As shown in Fig. 13, the six bits of PWML determine which sub-cycles are lengthened.

As shown in Fig. 16, the leading edge of the pulse is lengthened. By changing the length of specific sub-periods instead of simply changing the "H" duration, an accurate waveform can be duplicated without the use of complex external filters.

For example, if the upper eight bits of the 14-bit data are 03_{16} and the lower six bits are 05_{16}, the length of the "H"-level output in sub-periods t_8, t_{24}, t_{32}, t_{40}, and t_{56} is 4 τ, and its length 3 τ in all other sub-periods.



Pulse width modulation register H : 00111111
Pulse width modulation register L : 000101
Sub-periods where "H" pulse width is 32 μs : m = 8, 24, 32, 40, 56
Sub-periods where "H" pulse width is 31 5 μs : m = all other values

Fig. 14 PWM timing

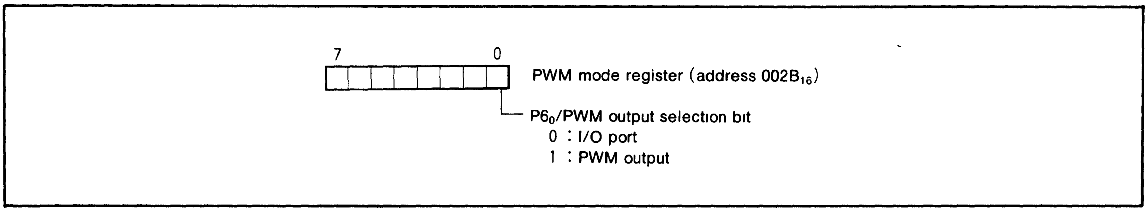


Fig. 15 Structure of PWM mode register

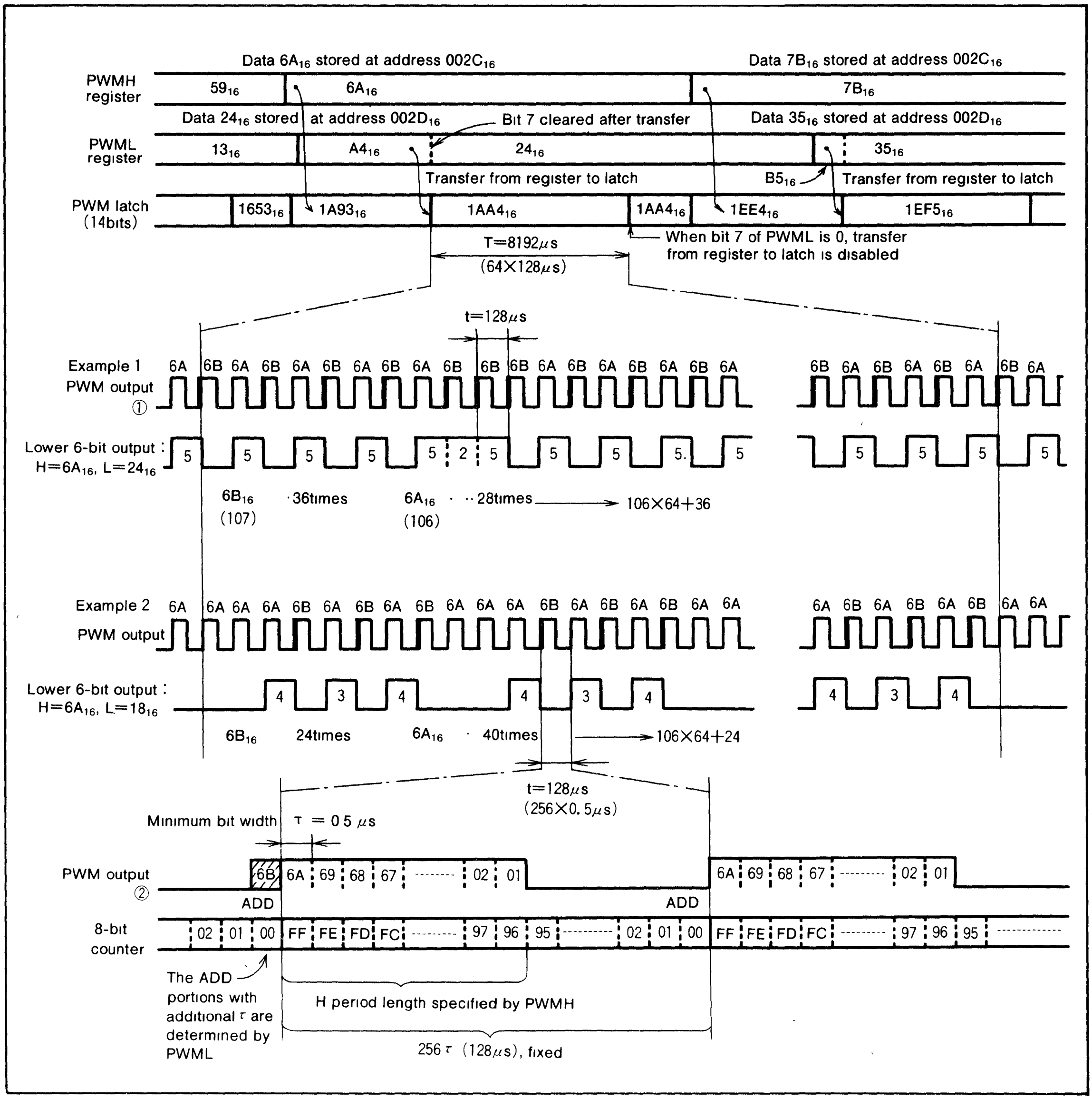


Fig. 16 14-bit PWM timing

COMPARATOR CIRCUIT

Comparator Configuration

The comparator circuit consists of a switch tree, ladder resistors, a comparator, a comparator control circuit, a comparator register (address 0030_{16}), and an analog signal input pin ($P6_6$/AN). The analog signal input pin ($P6_6$/AN) also functions as an ordinary digital port.

Comparator Register (CMP)

The comparator register is a 5-bit register of which bits 0 to 3 can be used to generate internal reference voltages in steps of 1/16 V_{CC}. The result of the comparison between the analog input voltage and an internal reference voltage is stored in bit 4 of the comparator register.

Comparator Operation

To activate the comparator, first set port $P6_6$ to input mode by setting the corresponding direction register (address $000D_{16}$) to "0"—this ensures that port $P6_6$/AN is used as an analog voltage input pin. Then write a digital value corresponding to the internal comparison voltage into bits 0 to 3 of the comparator register (address 0030_{16}). This write operation immediately activates the comparison. After 14 cycles of the system clock ϕ (the time required for the comparison), the comparison result is stored in bit 4 of the comparator.

If the analog input voltage is greater than the internal reference voltage, bit 4 is "1"; if it is less than the internal reference voltage, bit 4 is "0". To perform another comparison, the comparator must be written to again, even if the same internal reference voltage is to be used.

Table 3. Correspondence between bits 0 to 3 of the comparator register and internal reference voltage

Comparator register				Internal reference voltage
Bit 3	Bit 2	Bit 1	Bit 0	
0	0	0	0	$1/32V_{CC}$
0	0	0	1	$1/16V_{CC}+1/32V_{CC}$
0	0	1	0	$2/16V_{CC}+1/32V_{CC}$
0	0	1	1	$3/16V_{CC}+1/32V_{CC}$
0	1	0	0	$4/16V_{CC}+1/32V_{CC}$
0	1	0	1	$5/16V_{CC}+1/32V_{CC}$
0	1	1	0	$6/16V_{CC}+1/32V_{CC}$
0	1	1	1	$7/16V_{CC}+1/32V_{CC}$
1	0	0	0	$8/16V_{CC}+1/32V_{CC}$
1	0	0	1	$9/16V_{CC}+1/32V_{CC}$
1	0	1	0	$10/16V_{CC}+1/32V_{CC}$
1	0	1	1	$11/16V_{CC}+1/32V_{CC}$
1	1	0	0	$12/16V_{CC}+1/32V_{CC}$
1	1	0	1	$13/16V_{CC}+1/32V_{CC}$
1	1	1	0	$14/16V_{CC}+1/32V_{CC}$
1	1	1	1	$15/16V_{CC}+1/32V_{CC}$

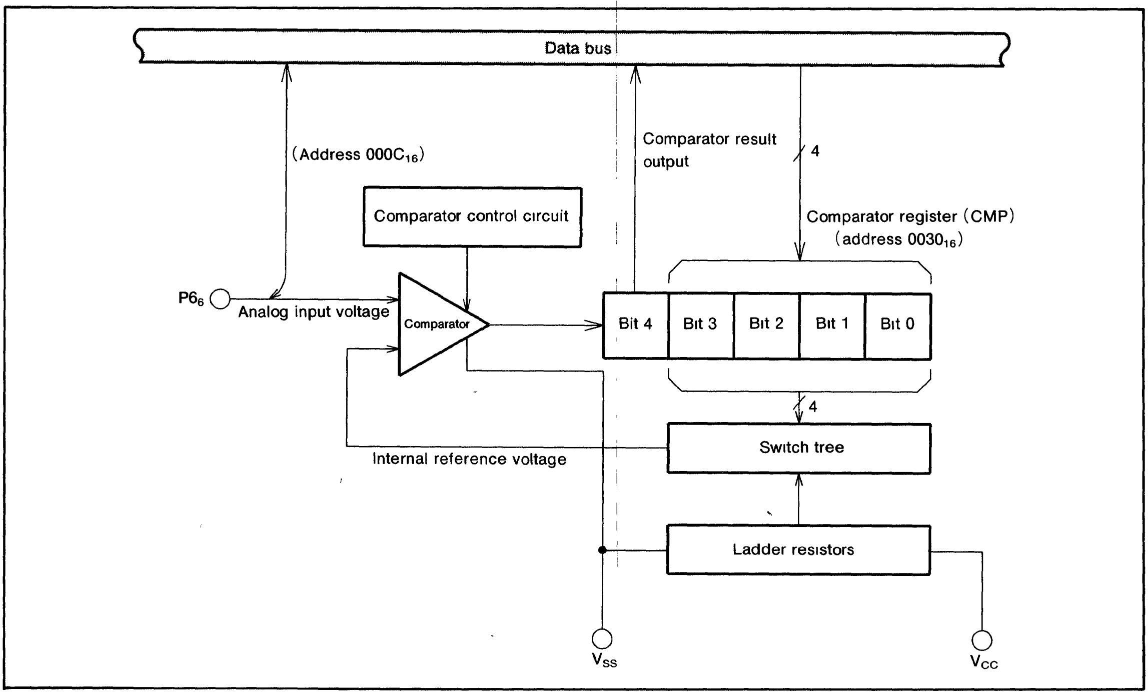


Fig. 17 Comparator circuit

RESET CIRCUIT

After a reset, the microcomputer will start in high-speed mode or low-speed mode depending on a mask-programmable option.

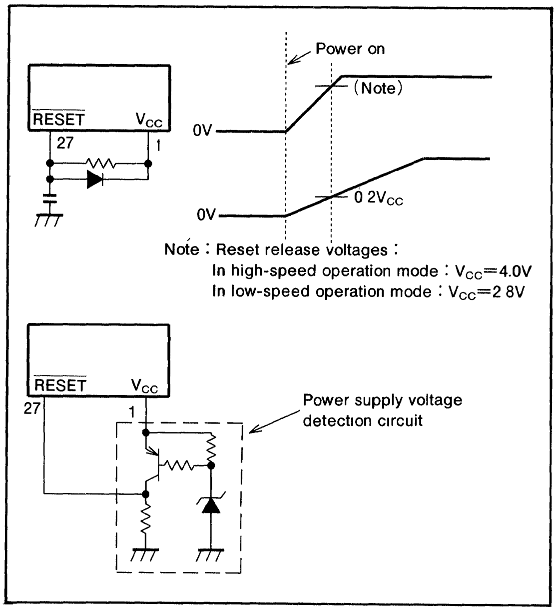
High-Speed Start Mode

In high-speed start mode, reset occurs if the $\overline{\text{RESET}}$ pin is held at a "L" level for at least 2μs then is returned to a "H" level (the power supply voltage should be between 4.0V and 5.5V). Both the X_{IN} and the X_{CIN} clocks begin oscillating. In order to give the X_{IN} clock time to stabilize, internal operation does not begin until after 13 X_{IN} clock cycles are complete. After the reset is completed, the program starts from the address contained in address $FFFD_{16}$ (upper byte) and address $FFFC_{16}$ (lower byte).

Low-Speed Start Mode

In low-speed start mode, reset occurs if the $\overline{\text{RESET}}$ pin is held at a "L" level for at least 2μs then is returned to a "H" level (the power supply voltage should be between 2.8V and 5.5V). The X_{IN} clock does not begin oscillating. In order to give the X_{CIN} time to stabilize, timer 1 and timer 2 are connected together and 512 cycles of the $X_{CIN}/16$ are counted before internal operation begins. After the reset is completed, the program starts from the address contained in address $FFFD_{16}$ (upper byte) and address $FFFC_{16}$ (lower byte).

If the X_{CIN} clock is stable, reset will complete after approximately 250ms (assuming $f(X_{CIN})=32.768$kHz). Immediately after a power-on, the stability of the clock circuit will determine the reset timing and will vary according to the characteristics of the oscillation circuit used.



Note : Reset release voltages :
In high-speed operation mode : V_{CC}=4.0V
In low-speed operation mode : V_{CC}=2 8V

Fig. 18 Power-on reset circuit example

Note on Use

Make sure that the reset input voltage is no more than 0.8V in high-speed start mode, or no more than 0.5V in low-speed start mode.

		Address	Register contents
(1)	Port P0 register	$(0000_{16})\cdots$	00_{16}
(2)	Port P1 register	$(0002_{16})\cdots$	00_{16}
(3)	Port P2 register	$(0004_{16})\cdots$	00_{16}
(4)	Port P2 direction register	$(0005_{16})\cdots$	00_{16}
(5)	Port P3 register	$(0006_{16})\cdots$	00_{16}
(6)	Port P4 register	$(0008_{16})\cdots$	00_{16}
(7)	Port P4 direction register	$(0009_{16})\cdots$	00_{16}
(8)	Port P5 register	$(000A_{16})\cdots$	00_{16}
(9)	Port P5 direction register	$(000B_{16})\cdots$	00_{16}
(10)	Port P6 register	$(000C_{16})\cdots$	00_{16}
(11)	Port P6 direction register	$(000D_{16})\cdots$	00_{16}
(12)	Serial I/O1 control register	$(0019_{16})\cdots$	00_{16}
(13)	Serial I/O2 control register	$(001D_{16})\cdots$	00_{16}
(14)	Timer 1 register	$(0024_{16})\cdots$	FF_{16}
(15)	Timer 2 register	$(0025_{16})\cdots$	01_{16}
(16)	Timer 3 register	$(0026_{16})\cdots$	FF_{16}
(17)	Timer 4 register	$(0027_{16})\cdots$	FF_{16}
(18)	Timer 12 mode register	$(0028_{16})\cdots$	00_{16}
(19)	Timer 34 mode register	$(0029_{16})\cdots$	00_{16}
(20)	PWM control register	$(002B_{16})\cdots$	00_{16}
(21)	Comparator	$(0030_{16})\cdots$	00_{16}
(22)	High-breakdown-voltage port control register	$(0038_{16})\cdots$	00_{16}
(23)	Interrupt edge selection register	$(003A_{16})\cdots$	00_{16}
(24)	CPU mode register	$(003B_{16})\cdots$	* * 1 0 0 0 0 0
(25)	Interrupt control register 1	$(003E_{16})\cdots$	00_{16}
(26)	Interrupt control register 2	$(003F_{16})\cdots$	00_{16}
(27)	Processor status register	$(PS)\cdots$	X X X X X 1 X X
(28)	Program counter	$(PC_H)\cdots$	Contents of address $FFFD_{16}$
		$(PC_L)\cdots$	Contents of address $FFFC_{16}$

Note : * : The initial values of bits 7 and 6 of the CPU mode register are determined by a mask option
X : Undefined
The contents of all other registers and RAM are undefined after a reset, so programs must set their initial values

Fig. 19 Internal status at reset

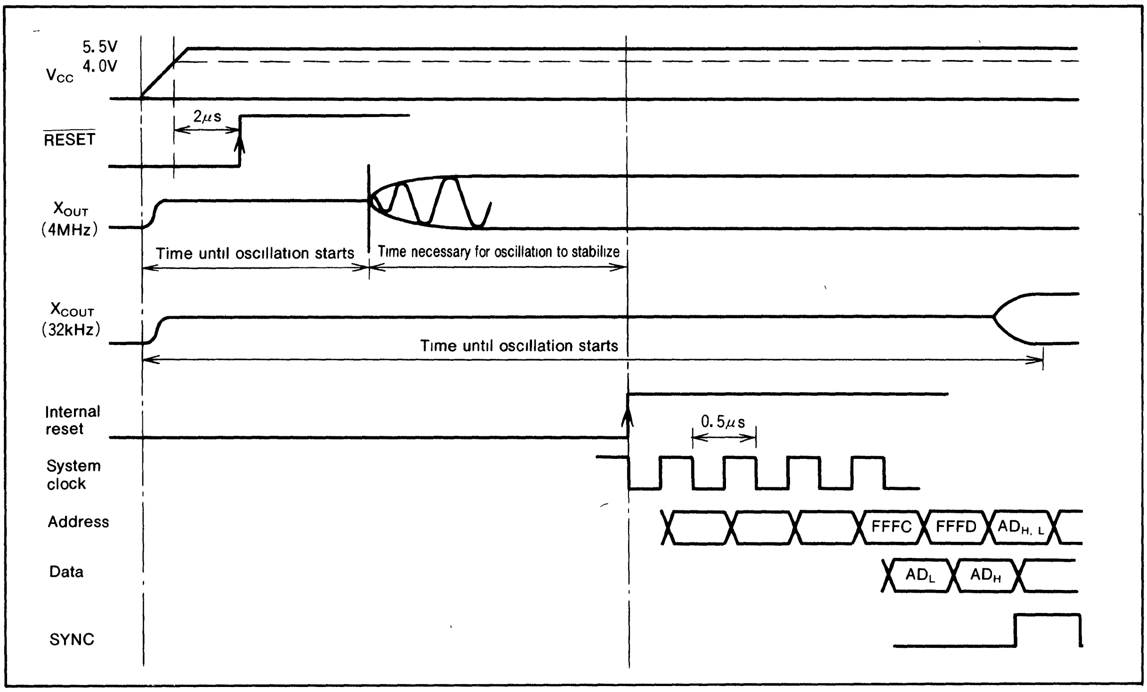


Fig. 20 Reset sequence in high-speed operation mode

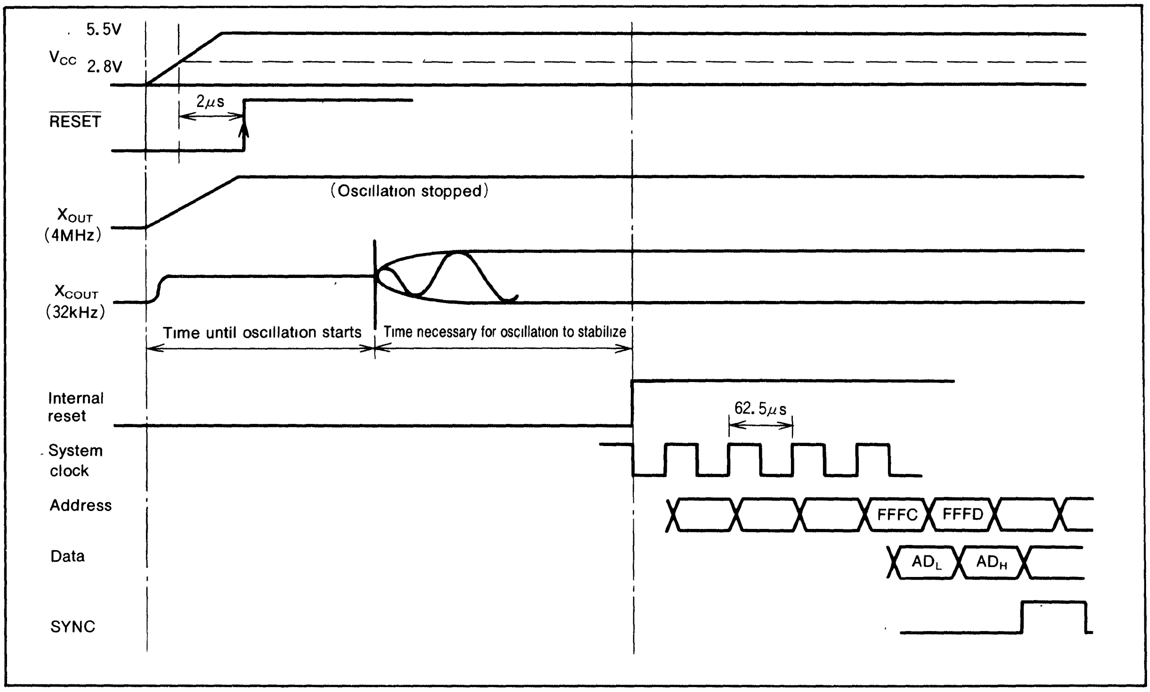


Fig. 21 Reset sequence in low-speed operation mode

CLOCK GENERATION CIRCUIT

When using an external clock signal, input the clock signal to the X_{IN} (X_{CIN}) pin and leave the X_{OUT} (X_{COUT}) pin open.If the X_{CIN} clock is not used, connect the X_{CIN} pin to V_{SS}, and leave the X_{COUT} pin open.

Either high-speed operation start mode or low-speed operation start mode can be selected by using a mask option.

(1) High-Speed Operation Start Mode

After reset has completed, the internal clock ϕ is half the frequency of X_{IN}. Immediately after power-on, both the X_{IN} and X_{CIN} clock start oscillating. To set the internal clock ϕ to low-speed mode, set bit 7 of the CPU mode register (address $003B_{16}$) to "1".

(2) Low-Speed Operation Start Mode

After reset has completed, the internal clock ϕ is half the frequency of X_{CIN}. Immediately after power-on, only the X_{CIN} clock starts oscillating. To set the internal clock ϕ to normal operation mode, first set bit 6 (CM_6) of the CPU mode register (address $003B_{16}$) to "0", the set bit 7 (CM_7) to "0" .Note that the program must allow time for oscillation to stabilize.

(3) Oscillation Control

Stop mode

If the STP instruction is executed, oscillation stops with the internal clock ϕ at an "H" level. Timer 1 is set to "FF_{16}" and timer 2 is set to "01_{16}".

Either X_{IN} or X_{CIN} divided by 16 is input to timer 1, and the output of timer 1 is connected to timer 2. The timer 1 and timer 2 interrupt enable bits must be set to disabled ("0"), so a program must set these bits before executing a STP instruction. Oscillation restarts at reset or when an external interrupt is received, but the internal clock ϕ is not supplied to the CPU until timer 2 overflows. This allows time for the clock circuit oscillation to stabilize.

Wait mode

If the WIT instruction is executed, the internal clock ϕ stops at a "H" level but the oscillator itself does not stop. The internal clock restarts if a reset occurs or when an interrupt is received. Since the oscillator does not stop, normal operation can be started immediately after the clock is restarted.

Low-speed mode

If the internal clock is generated from the sub clock (X_{CIN}), a low power consumption operation can be entered by stopping only the main clock X_{IN}. To stop the main clock, set bit 6 (CM_6) of the CPU mode register ($003B_{16}$) to "1". When the main clock X_{IN} is restarted, the program must allow enough time to for oscillation to stabilize.

Note that in low-power-consumption mode the X_{CIN}-X_{COUT} drive performance can be reduced, allowing even lower power consumption (20μA with X_{CIN} =32kHz). To reduce the X_{CIN}-X_{COUT} drive performance, clear bit 5 (CM_5) of the CPU mode register ($003B_{16}$) to "0". At reset or when a STP instruction is executed, this bit is set to "1" and strong drive is selected to help the oscillation to start.

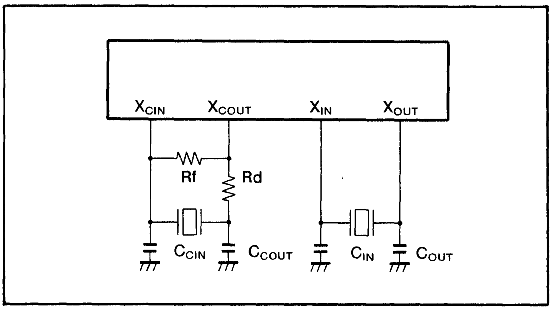


Fig. 22 Ceramic resonator circuit

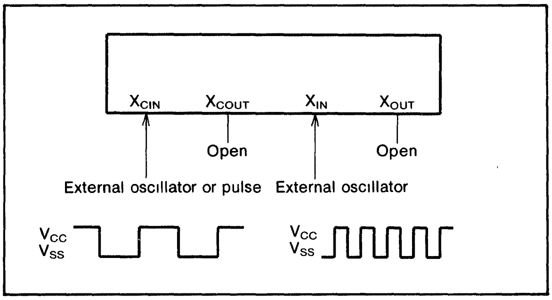
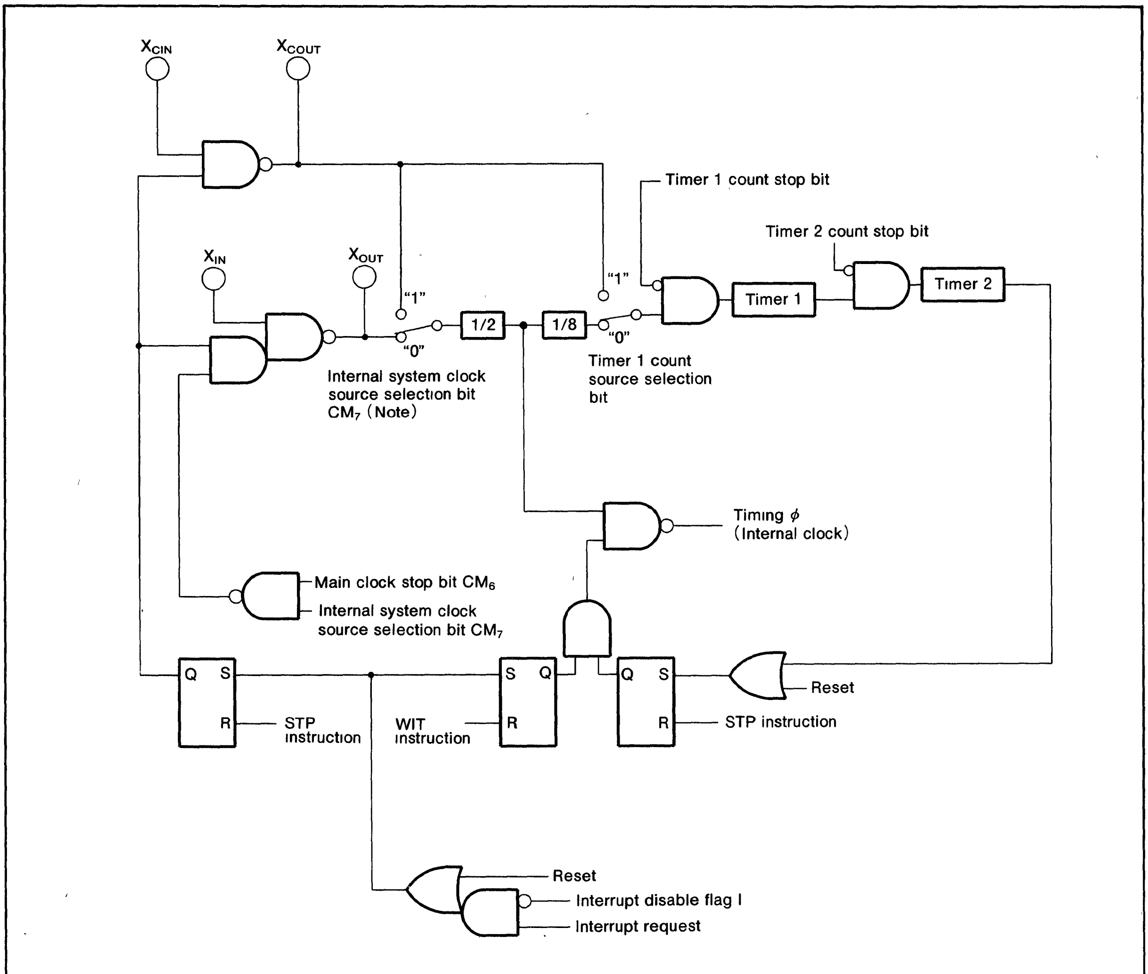
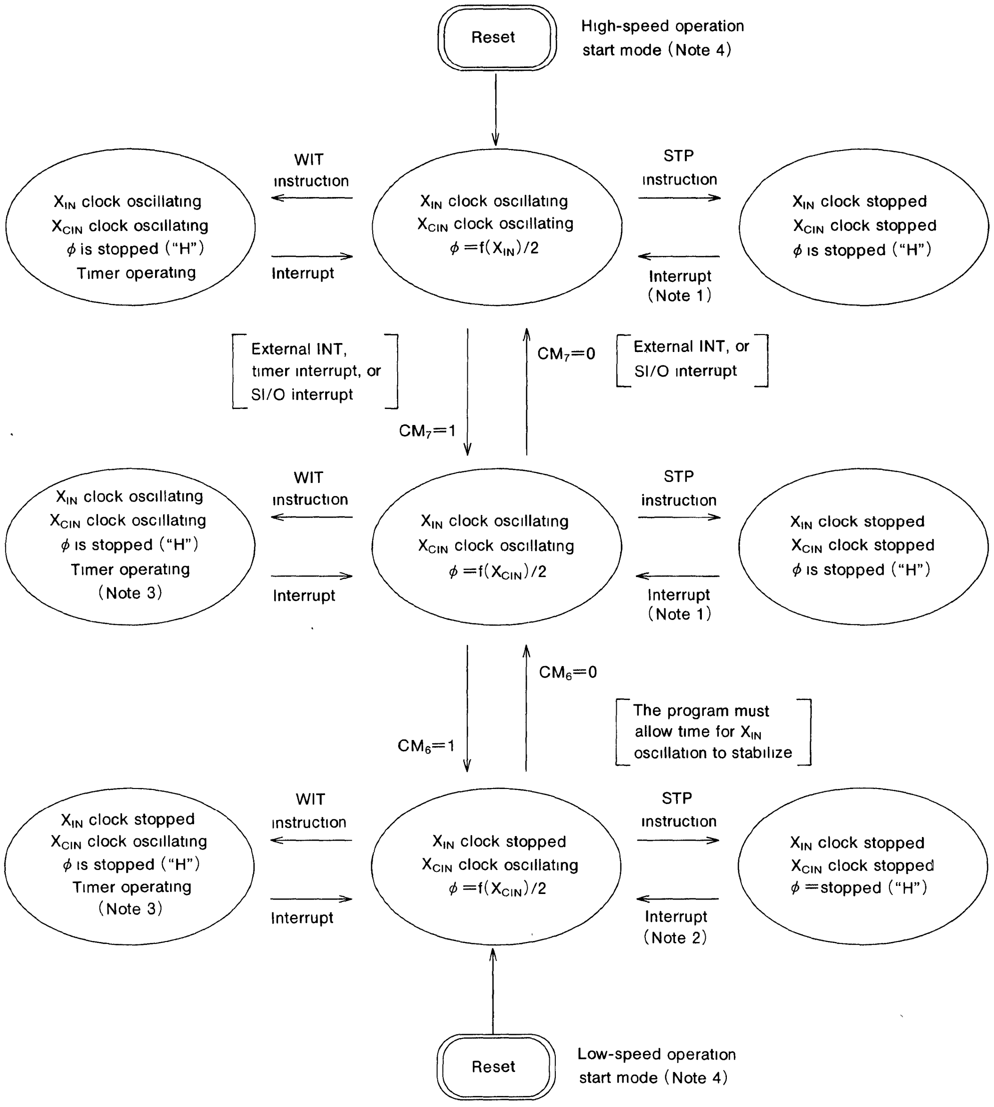


Fig. 23 External clock input circuit



Note : The values of CM_7 and CM_6 at reset are determined by a mask option

Fig. 24 System clock generation circuit block diagram



The example assumes that 4 MHz is being applied to the X_{IN} pin and 32 kHz to the X_{CIN} pin

Note 1 When the STP state is ended, a delay of approximately 2ms is automatically generated by timer 1 and timer 2
2 The delay after the STP state ends is approximately 0 25s
3 If the internal clock ϕ divided by 8 is used as the timer count source, the frequency of the count source is f(X_{CIN})/16
4 Specify this option when ordering a mask ROM version

Fig. 25 State transitions of system clock

NOTES ON PROGRAMMING

Processor Status Register

The contents of the processor status register (PS) after a reset are undefined, except for the interrupt disable flag (I) which is "1". Therefore, flags that affect program execution must be initialized after a reset.In particular, it is essential to initialize the T and D flags because of their effect on calculations.

Interrupts

The contents of the interrupt request bits do not change immediately after they have been written.

After writing to an interrupt request register, execute at least one instruction before performing a BBC or BBS instruction.

Decimal Calculations

To calculate in decimal notation, set the decimal mode flag (D) to "1", then execute a ADC or SBC instruction. Only the ADC and SBC instruction yield proper decimal results. After executing an ADC or SBC instruction, execute at least one instruction before executing a SEC, CLC, or CLD instruction.

In decimal mode, the values of the negative (N), overflow (V), and zero (Z) flags are invalid. The carry flag can be used to indicate whether a carry or borrow has occurred, but must be initialized before each calculation. Clear the carry flag before an ADC and set the flag before an SBC.

Timers

If a value n (between 0 and 255) is written to a timer latch, the frequency division ratio is 1/(n+1).

Multiplication and Division Instructions

The MUL and DIV instructions do not affect the T and D flags.

The execution of these instructions does not change the contents of the processor status register.

Ports

The contents of the port direction registers cannot be read. Programs can not use the value of a direction register as an index, or bit-test a direction register (BBC or BBS), or perform a read-modify-write instruction such as ROR, CLB, or SEB. Use instructions such as LDM and STA to set the port direction registers.

Serial I/O

When using an external clock, input "H" to the external clock input pin and clear the serial I/O interrupt request bit before executing a serial I/O transfer.

When using the internal clock, set the synchronization clock to internal clock, then clear the serial I/O interrupt request bit before executing a serial I/O transfer.

Instruction Execution Timing

The instruction execution time is obtained by multiplying the frequency of the internal clock ϕ by the number of cycles needed to execute an instruction. The number of cycles required to execute an instruction is shown in the list of machine instructions. The frequency of the internal clock ϕ is half of the X_{IN} or X_{CIN} frequency.

DATA REQUIRED FOR MASK ORDERS

The following are necessary when ordering a mask ROM production:

(1) Mask ROM Order Confirmation Form
(2) Mask Specification Form
(3) Data to be written to ROM, in EPROM form (three identical copies)

If required, specify the following option on the Mask Confirmation Form:

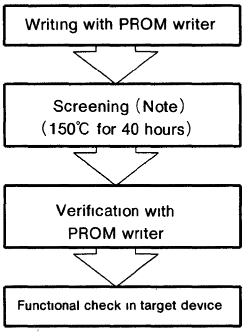
- Operation start mode switching option

ROM Writing Method

The built-in PROM of the blank one-time programmable version and built-in EPROM version can be read from and written to with an normal EPROM writer using a special write adapter.

Package	Name of Write Adapter
64P4B, 64S1B	PCA4738S-64
64P6N	PCA4738F-64
64D0	PCA4738L-64

The PROM of the blank one-time programmable version is not tested or screened after assembly. To ensure proper operation after writing, the procedure shown in Figure 26 is recommended to verify programming.



Note : The screening temperature is far higher than the storage temperature Do not leave the microcomputer at 150℃ for longer than 100 hours

Fig. 26 Writing and testing of one-time programmable version

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	All voltages measured based on the V_{SS} pin Output transistors are isolated.	−0. 3 to 7. 0	V
V_{EE}	Pull-down power supply voltage		V_{CC}−40 to V_{CC}+0. 3	V
V_I	Input voltage $P2_4$-$P2_7$, $P4_1$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$		−0. 3 to V_{CC}+0. 3	V
V_I	Input voltage $P4_0$		−0. 3 to V_{CC}+0. 3	V
V_I	Input voltage $\overline{RESET}$, X_{IN}		−0. 3 to V_{CC}+0. 3	V
V_I	Input voltage X_{CIN}		−0. 3 to V_{CC}+0. 3	V
V_O	Output voltage $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_3$, $P3_0$-$P3_7$		V_{CC}−40 to V_{CC}+0. 3	V
V_O	Output voltage $P2_4$-$P2_7$, $P4_1$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_5$, $P7_0$-$P7_7$, X_{OUT}, X_{COUT}		−0. 3 to V_{CC}+0. 3	V
P_d	Power dissipation	T_a = 25℃	1000(Note 1)	mW
Topr	Operating temperature		−10 to 85	℃
Tstg	Storage temperature		−40 to 125	℃

Note 1 600mW in case of the flat package

RECOMMENDED OPERATING CONDITIONS (V_{CC} = 4. 0 to 5. 5V, T_a = −10 to 85℃, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage	High-speed operation mode	4. 0	5. 0	5. 5	V
		Low-speed operation mode	2. 8	5. 0	5. 5	
V_{SS}	Supply voltage			0		V
V_{EE}	Pull-down power supply voltage		V_{CC}−38		V_{CC}	V
V_{IA}	Analog input voltage		0		V_{CC}	V
V_{IH}	"H" input voltage $P2_4$-$P2_7$		0. 4V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage $P4_0$		0. 75V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage $P4_1$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$		0. 75V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage $\overline{RESET}$		0. 8V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage X_{IN}, X_{CIN}		0. 8V_{CC}		V_{CC}	V
V_{IL}	"L" input voltage $P2_4$-$P2_7$		0		0. 16V_{CC}	V
V_{IL}	"L" input voltage $P4_0$		0		0. 25V_{CC}	V
V_{IL}	"L" input voltage $P4_1$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$		0		0. 25V_{CC}	V
V_{IL}	"L" input voltage $\overline{RESET}$		0		0. 2V_{CC}	V
V_{IL}	"L" input voltage X_{IN}, X_{CIN}		0		0. 2V_{CC}	V

RECOMMENDED OPERATING CONDITIONS (V_{CC}=4.0 to 5.5V, T_a=−10 to 85℃, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
$\Sigma I_{OH(peak)}$	"H" total peak output current $P0_0$-$P0_7$, $P1_0$-$P1_7$, (Note 1) $P2_0$-$P2_7$, $P3_0$-$P3_7$			−240	mA
$\Sigma I_{OH(peak)}$	"H" total peak output current $P4_1$-$P4_7$, $P6_0$-$P6_7$			−60	mA
$\Sigma I_{OL(peak)}$	"L" total peak output current $P2_4$-$P2_7$, $P4_1$-$P4_7$, $P5_0$-$P5_7$, $P6_1$-$P6_7$			100	mA
$\Sigma I_{OL(peak)}$	"L" total peak output current $P6_0$			3.0	mA
$\Sigma I_{OH(avg)}$	"H" total average output current $P0_0$-$P0_7$, $P1_0$-$P1_7$, (Note 1) $P2_0$-$P2_7$, $P3_0$-$P3_7$			−120	mA
$\Sigma I_{OH(avg)}$	"H" total average output current $P4_1$-$P4_7$, $P6_0$-$P6_7$			−30	mA
$\Sigma I_{OL(avg)}$	"L" total average output current $P2_4$-$P2_7$, $P4_1$-$P4_7$, $P5_0$-$P5_7$, $P6_1$-$P6_7$			50	mA
$\Sigma I_{OL(avg)}$	"L" total average output current $P6_0$			1.5	mA
$I_{OH(peak)}$	"H" peak output current $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_3$, $P3_0$-$P3_7$ (Note 2)			−40	mA
$I_{OH(peak)}$	"H" peak output current $P2_4$-$P2_7$, $P4_1$-$P4_7$, $P6_0$-$P6_7$			−10	mA
$I_{OL(peak)}$	"L" peak output current $P2_4$-$P2_7$, $P6_1$-$P6_7$			10	mA
$I_{OL(peak)}$	"L" peak output current $P4_1$-$P4_7$, $P5_0$-$P5_7$			10	mA
$I_{OL(peak)}$	"L" peak output current $P6_0$			3.0	mA
$I_{OH(avg)}$	"H" average output current $P0_0$-$P0_7$, $P1_0$-$P1_7$, (Note 3) $P2_0$-$P2_3$, $P3_0$-$P3_7$			−18	mA
$I_{OH(avg)}$	"H" average output current $P2_4$-$P2_7$, $P4_1$-$P4_7$, $P6_0$-$P6_7$			−5.0	mA
$I_{OL(avg)}$	"L" average output current $P2_4$-$P2_7$, $P6_1$-$P6_7$			5.0	mA
$I_{OL(avg)}$	"L" average output current $P4_1$-$P4_7$, $P5_0$-$P5_7$			10	mA
$I_{OL(avg)}$	"L" average output current $P6_0$			1.5	mA
f(CNTR)	Clock input frequency for timers 4 (duty cycle 50%)			250	kHz
$f(X_{IN})$	Main clock input oscillation frequency (Note 4)			4.2	MHz
$f(X_{CIN})$	Sub clock input oscillation frequency (Note 4, 5)		32.768	50	kHz

Note 1. The total output current is the sum of all the currents flowing through all the applicable ports The total average current is an average value measured over 100ns The total peak current is the peak value of all the currents.
2. The peak output current is the peak current flowing in each port
3. The average output current in an average value measured over 100ms
4. When the oscillation frequency has a duty cycle of 50%.
5. When using the microcomputer in low-speed mode, make sure that the sub clock's input frequency $f(X_{CIN})$ is less than $f(X_{IN})/3$

ELECTRICAL CHARACTERISTICS (V_{CC} = 4.0 to 5.5V, T_a = −10 to 85°C, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits		Unit
			Min.	Typ.	Max	
V_{OH}	"H" output voltage $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_3$, $P3_0$-$P3_7$	I_{OH}=−18mA, V_{CC}=4.5 to 5.5V	V_{CC}−2.0			V
V_{OH}	"H" output voltage $P2_4$-$P2_7$, $P4_1$-$P4_7$, $P6_0$-$P6_7$	I_{OH}=−10mA, V_{CC}=4.5 to 5.5V	V_{CC}−2.0			V
V_{OL}	"L" output voltage $P2_4$-$P2_7$, $P4_1$-$P4_7$, $P5_0$-$P5_7$, $P6_1$-$P6_7$	I_{OL}=10mA, V_{CC}=4.5 to 5.5V			2.0	V
V_{OL}	"L" output voltage $P6_0$	I_{OL}=1.5mA, V_{CC}=4.5 to 5.5V			0.5	V
$V_{T+}-V_{T-}$	Hysteresis $\overline{INT_0}$-$\overline{INT_2}$, S_{IN1}, S_{IN2}, CLK1, CLK2, CNTR	When using a non-port function		0.4		V
$V_{T+}-V_{T-}$	Hysteresis $\overline{RESET}$, X_{IN}	$\overline{RESET}$: V_{CC}=2.8V to 5.5V		0.5		V
$V_{T+}-V_{T-}$	Hysteresis X_{CIN}			0.5		V
I_{IH}	"H" input current $P2_4$-$P2_7$, $P4_1$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$	V_I=V_{CC}			5.0	μA
I_{IH}	"H" input current $P4_0$	V_I=V_{CC}			5.0	μA
I_{IH}	"H" input current $\overline{RESET}$, X_{CIN}	V_I=V_{CC}			5.0	μA
I_{IH}	"H" input current X_{IN}	V_I=V_{CC}		4		μA
I_{IL}	"L" input current $P2_4$-$P2_7$, $P4_1$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$	V_I=V_{SS}			−5.0	μA
I_{IL}	"L" input current $P4_0$	V_I=V_{SS}			−5.0	μA
I_{IL}	"L" input current $\overline{RESET}$, X_{CIN}	V_I=V_{SS}			−5.0	μA
I_{IL}	"L" input current X_{IN}	V_I=V_{SS}		−4		μA
I_{LOAD}	Output load current $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_3$, $P3_0$-$P3_7$	V_{EE}=V_{CC}−36V, V_O=V_{CC}, With output transistors off	150	500	900	μA
I_{LEAK}	Output leakage current $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_3$, $P3_0$-$P3_7$	V_{EE}=V_{CC}−38V, V_O=V_{CC}−38V, With output transistors off (Except for reset)			−10	μA
V_{RAM}	RAM hold voltage	When clock is stopped	2.0		5.5	V
I_{CC}	Power supply current	In high-speed operation mode $f(X_{IN})$=4MHz $f(X_{CIN})$=32kHz Output transistors off Comparator operating		5	10	mA
		In high-speed operation mode $f(X_{IN})$=4MHz (in WIT state) $f(X_{CIN})$=32kHz Output transistors off Comparator stopped		1		mA
		In low-speed operation mode $f(X_{IN})$= stopped $f(X_{CIN})$=32kHz Low-power dissipation mode set (CM_5=0) Output transistors off		60	200	μA
		In low-speed operation mode $f(X_{IN})$= stopped $f(X_{CIN})$=32kHz (in WIT state) Low-power dissipation mode set (CM_5=0) Output transistors off		20	40	μA
		All oscillation stopped (in STP state) Output transistors off — T_a=25°C		0.1	1.0	μA
		All oscillation stopped (in STP state) Output transistors off — T_a=85°C			10	μA

COMPARATOR CHARACTERISTICS

(V_{CC}=4.0 to 5.5V, V_{SS}=0V, T_a=−10 to 85℃, high-speed operation mode, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ	Max	
—	Resolution				4	Bits
—	Absolute accuracy				1/2	LSB
T_{CONV}	Conversion time				7	μs
I_{IA}	Analog port input current				5.0	μA
R_{LADDER}	Ladder resistor			30		kΩ

TIMING REQUIREMENTS

(V_{CC}=4.0 to 5.5V, V_{SS}=0V, T_a=−10 to 85℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{W(\overline{RESET})}$	Reset input "L" pulse width		2			μs
$t_{C(X_{IN})}$	Main clock input cycle time (X_{IN} input)		238			ns
$t_{WH(X_{IN})}$	Main clock input "H" pulse width		60			ns
$t_{WL(X_{IN})}$	Main clock input "L" pulse width		60			ns
$t_{C(X_{CIN})}$	Sub clock input cycle time (X_{CIN})		2.0			ms
$t_{W(X_{CIN})}$	Sub clock input pulse width (X_{CIN})		1.0			ms
$t_{C(CNTR)}$	CNTR input cycle time		4			μs
$t_{WH(CNTR)}$	CNTR input "H" pulse width		1.6			μs
$t_{WL(CNTR)}$	CNTR input "L" pulse width		1.6			μs
$t_{WH(INT)}$	INT_0~INT_2 input "H" pulse width		80			ns
$t_{WL(INT)}$	INT_0~INT_2 input "L" pulse width		80			ns
$t_{C(S_{CLK})}$	Serial clock input cycle time		1		1000	μs
$t_{WH(S_{CLK})}$	Serial clock input "H" pulse width		40	1		%
$t_{WL(S_{CLK})}$	Serial clock input "L" pulse width		40			%
$t_{r(S_{CLK})}$	Serial clock input clock rise time		5		50	ns
$t_{r(S_{CLK})}$	Serial clock input clock fall time		5		40	ns
$t_{h(S_{CLK}\text{-}S_{IN})}$	Serial input hold time		0.2tc			ns
$t_{su(S_{CLK}\text{-}S_{IN})}$	Serial input setup time		0.2tc			ns

SWITCHING CHARACTERISTICS

(V_{CC}=4.0 to 5.5V, V_{SS}=0V, T_a=−10 to 85℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{WH(S_{CLK})}$	Serial clock output "H" pulse width	C_L=100pF, R_L=1kΩ	t_C/2−160			ns
$t_{WL(S_{CLK})}$	Serial clock output "L" pulse width	C_L=100pF, R_L=1kΩ	t_C/2−160			ns
$t_{d(S_{CLK}\text{-}S_{OUT})}$	Serial clock delay time				0.2t_C	ns
$t_{v(S_{CLK}\text{-}S_{OUT})}$	Serial clock hold time		0			ns
$t_{f(S_{CLK})}$	Serial clock output fall time	C_L=100pF, R_L=1kΩ			40	ns
$t_{r(P_{ch}\text{-}strg)}$	P-channel high-breakdown voltage output rise time (Note 1)	C_L=100pF, V_{EE}=V_{CC}−36V		55		ns
$t_{r(P_{ch}\text{-}weak)}$	P-channel high-breakdown voltage output fall time (Note 2)	C_L=100pF, V_{EE}=V_{CC}−36V		1.8		ns

Note 1. When bit 0 of the high-breakdown voltage port control register (address 0038_{16}) is at "0"

2. When bit 0 of the high-breakdown voltage port control register (address 0038_{16}) is at "1"

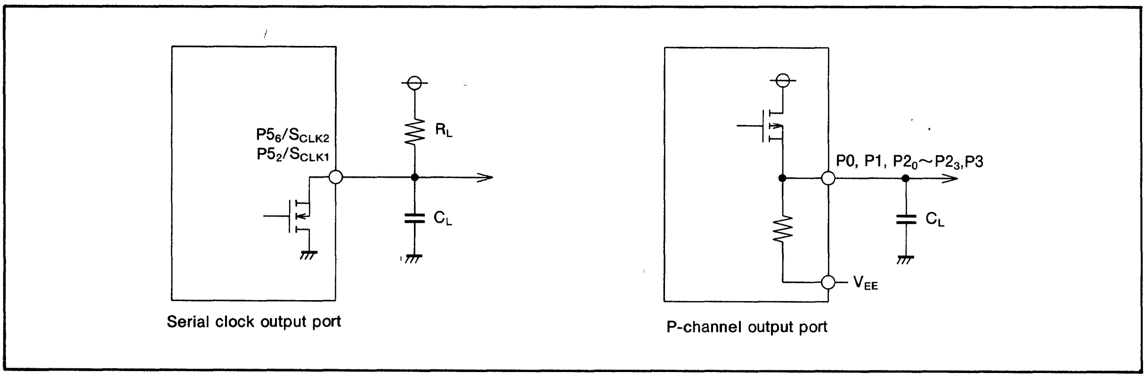
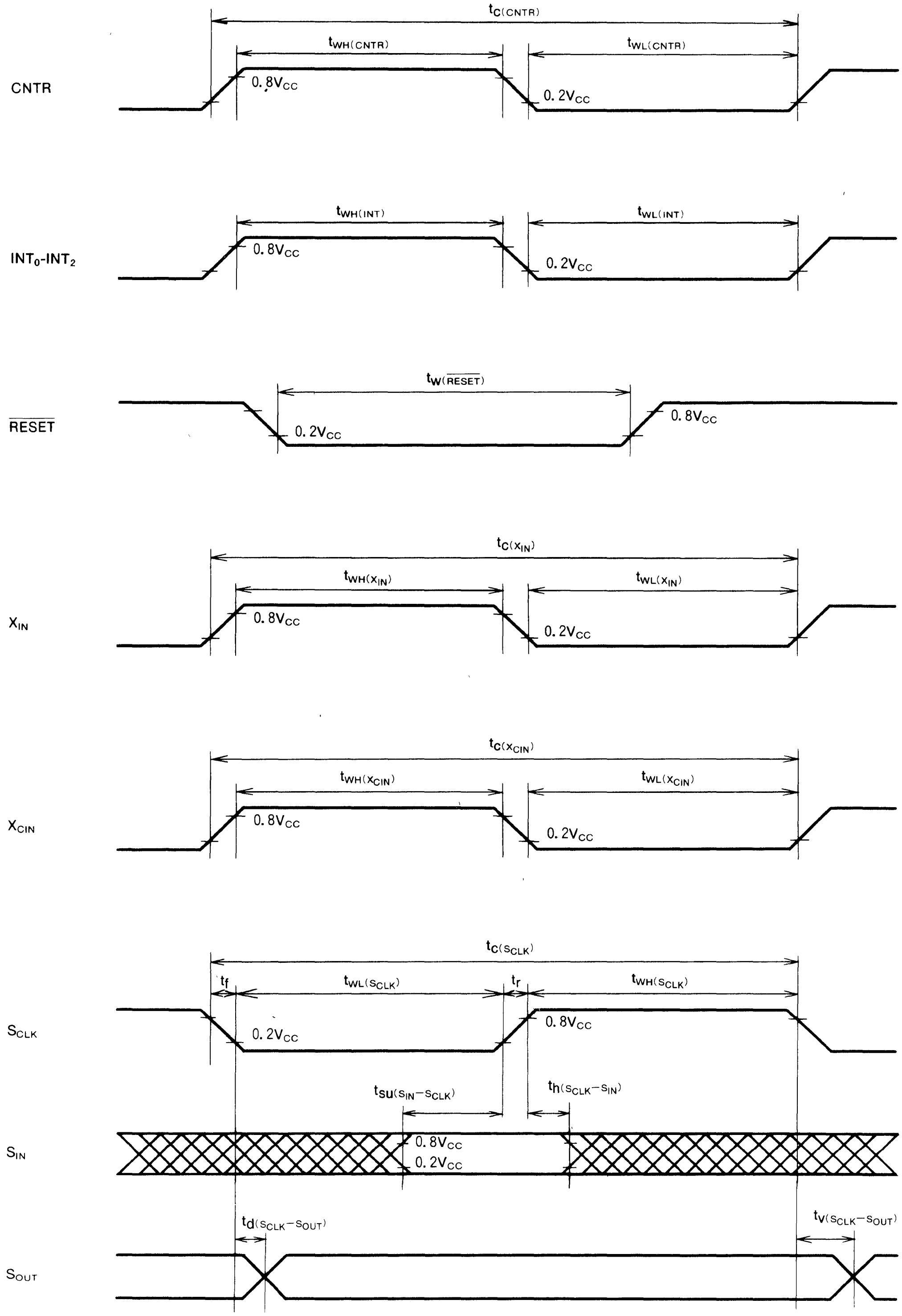


Fig. 27 Output switching characteristics measurement circuit

TIMING CHART



MITSUBISHI MICROCOMPUTERS

M3811x Group

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

DESCRIPTION

The M3811x group is made up of 8-bit microcomputers based on the MELPS 740 core.

The M3811x group is designed mainly for VCR timer/function control, and include four 8-bit timers, a fluorescent display automatic display circuit, a PWM function, and a comparator.

The various microcomputers in the M3811x group include variations of internal memory size and packaging. For details, see the section on part numbering.

For details on availability of microcomputers in the M3811x group, see the section on group expansion.

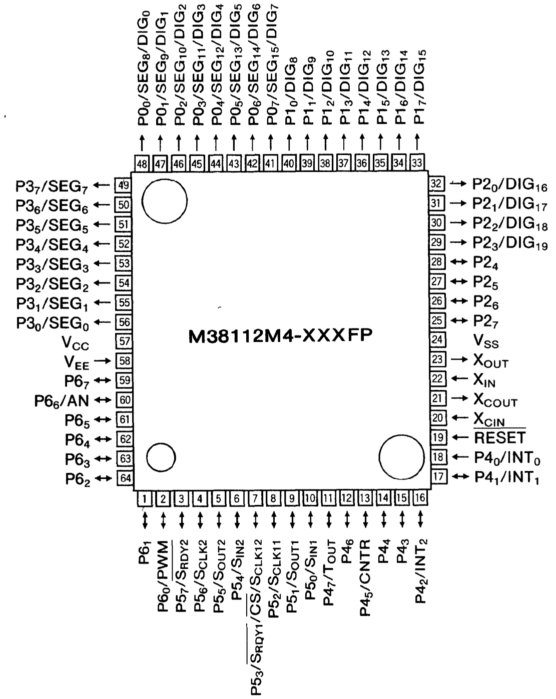
FEATURES

- Basic machine-language instructions ························ 71
- Instruction execution time ································ 0.95μs
  (shortest instruction at 4.19MHz oscillation frequency)
- Memory size
  ROM ·· 4K to 32K bytes
  RAM ·· 192 to 1024 bytes
- Programmable input/output ports ···························· 27
- High-breakdown-voltage output ports ························ 28
- Interrupts ································ 14 sources, 12 vectors
- Timers ·· 8-bit×4
- Serial I/O ························ Clock-synchronized 8-bit×2
  (Serial I/O1 has an automatic data transfer function)
- PWM output circuit ······································ 14-bit×1
- Comparator ··· 4-bit×1
- Fluorescent display function
  Segments ·· 8 to 16
  Digits ··· 8 to 16
- 2 Clock generation circuit
  Clock (X_{IN}-X_{OUT}) ················ Internal feedback amplifier
  Sub clock (X_{CIN}-X_{COUT}) ······ Internal amplifier without feedback
- Supply voltage ······································· 4.0 to 5.5V
- Low power dissipation
  In high-speed operation ································· 25mW
  (at 4.19MHz oscillation frequency)
  In low-speed operation ·································· 300μW
  (at 32kHz oscillation frequency)
- Operating temperature range ···················· −10 to 85℃

APPLICATIONS

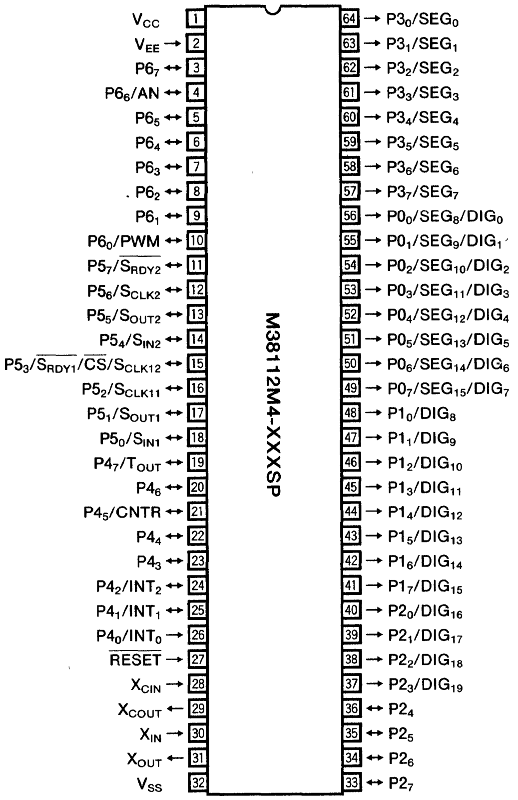
VCRs, tuners, musical instruments, office automation, etc.

PIN CONFIGURATION (TOP VIEW)



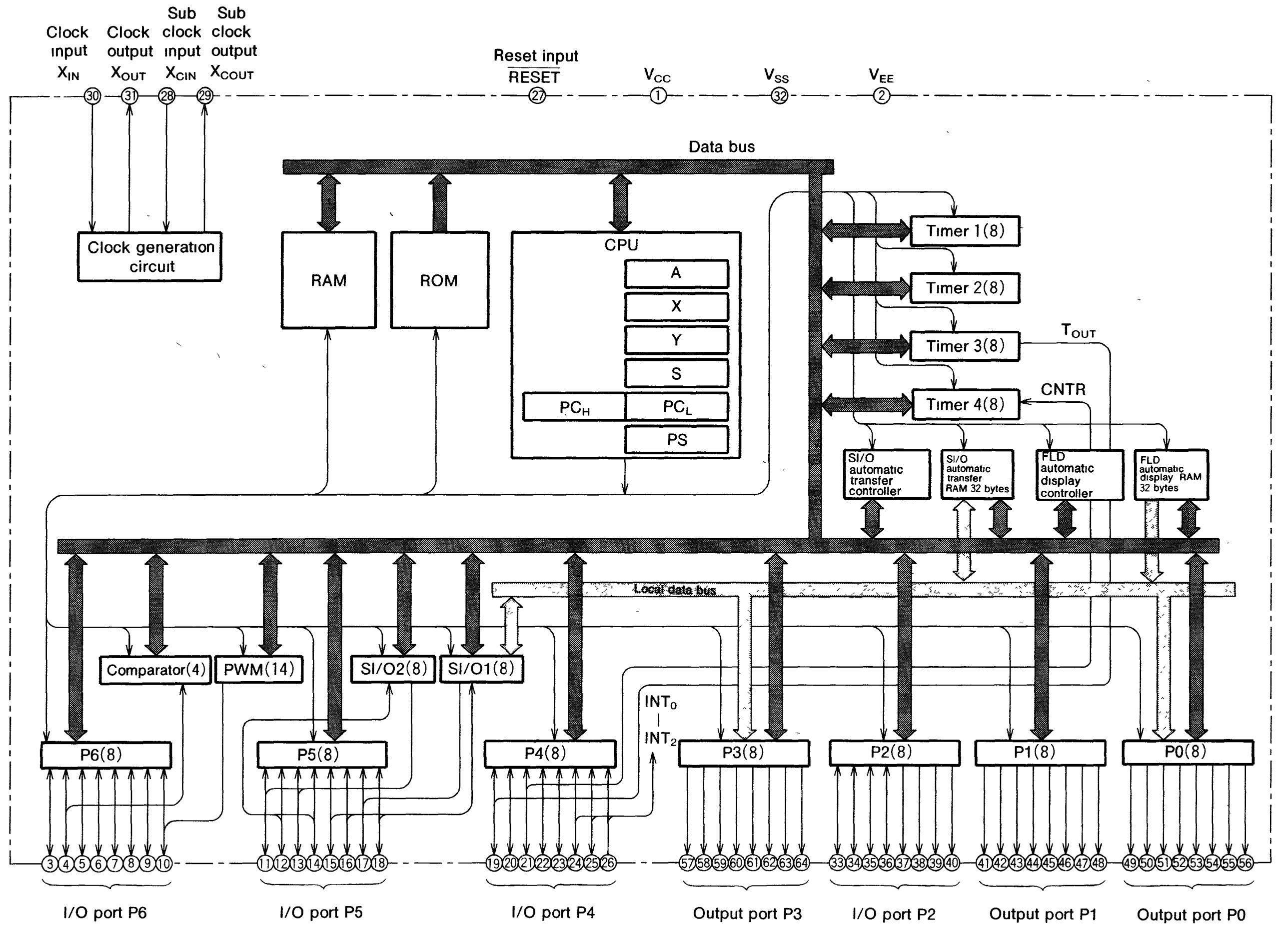
Package type : 64P6N
64-pin plastic molded QFP

PIN CONFIGURATION (TOP VIEW)



Outline 64P4B
64-pin shrink plastic molded DIP

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTION

Pin	Name	Function	Alternate Function
V$_{CC}$, V$_{SS}$	Power supply	Power supply inputs 4 0 to 5.5V to V$_{CC}$, and 0V to V$_{SS}$.	
V$_{EE}$	Pull-down power input	Applies voltage supplied to pull-down resistors of ports P0, P1, P2$_0$-P2$_3$ and P3.	
$\overline{\text{RESET}}$	Reset input	To reset the microcomputer, this pin should be kept at an "L" level for more than 2μs under high-speed operating conditions. In low-speed operation start mode, internal reset is not released until the X$_{CIN}$-X$_{COUT}$ clock has had time to stabilize	
X$_{IN}$	Clock input	Input and output signals for the internal clock generation circuit. It consist of internal feedback amplifier Connect a ceramic resonator or quartz crystal between the X$_{IN}$ and X$_{OUT}$ pins to set the oscillation frequency If an external clock is used, connect the clock source to the X$_{IN}$ pin and leave the X$_{OUT}$ pin open This clock is used as system clock	
X$_{OUT}$	Clock output		
X$_{CIN}$	Sub clock input	Input and output signals for the internal sub clock generation circuit It consist of internal amplifier without feedback Connect a ceramic resonator or quartz crystal and external feedback resistor between the X$_{CIN}$ and X$_{COUT}$ pins If an external clock is used, connect the clock source to the X$_{CIN}$ pin and leave the X$_{COUT}$ pin open This clock can also be used as the system clock.	
X$_{COUT}$	Sub clock output		
P0$_0$/SEG$_8$/DIG$_0$-P0$_7$/SEG$_{15}$/DIG$_7$	Output port P0	An 8-bit output port The output structure is high-breakdown-voltage P-channel open drain with internal pull-down resistors connected between the output and the V$_{EE}$ pin Are "L" at reset.	FLD automatic display pins
P1$_0$/DIG$_8$-P1$_7$/DIG$_{15}$	Output port P1	An 8-bit output port with the same function as port P0.	FLD automatic display pins
P2$_0$/DIG$_{16}$-P2$_3$/DIG$_{19}$	Output port	A 4-bit output port with the same function as port P0	FLD automatic display pins
P2$_4$-P2$_7$	I/O port P2	A 4-bit CMOS I/O port An I/O direction register allows each pin to be individually programmed as either input or output. At reset this port is set to input mode The input levels are TTL compatible	
P3$_0$/SEG$_0$-P3$_7$/SEG$_7$	Output port P3	An 8-bit output port with the same function as port P0	FLD automatic display pins
P4$_0$/INT$_0$	Input port P4$_0$	A 1-bit CMOS input pin	External interrupt input pin
P4$_1$/INT$_1$, P4$_2$/INT$_2$	I/O port P4	A 7-bit CMOS I/O port with the same function as port P2$_4$-P2$_7$, with CMOS compatible input levels	External interrupt input pins
P4$_3$, P4$_4$, P4$_6$			
P4$_5$/CNTR			Event count input pin
P4$_7$/T$_{OUT}$			Timer output pin
P5$_0$/S$_{IN1}$, P5$_1$/S$_{OUT1}$, P5$_2$/S$_{CLK11}$, P5$_3$/$\overline{\text{S}_{RDY1}}$/$\overline{\text{CS}}$/S$_{CLK12}$	I/O port P5	An 8-bit I/O port with the same function as port P2$_4$-P2$_7$ The output structure of this port is N-channel open drain, and the input levels are CMOS compatible Keep the input voltage of this port between 0V and V$_{CC}$.	Serial I/O1 I/O pins
P5$_4$/S$_{IN2}$, P5$_5$/S$_{OUT2}$, P5$_6$/S$_{CLK2}$, P5$_7$/$\overline{\text{S}_{RDY2}}$			Serial I/O2 I/O pins

PIN DESCRIPTION

Pin	Name	Function	
			Alternate Function
$P6_0$/PWM	I/O port P6	An 8-bit CMOS I/O port with the same function as port $P2_4$-$P2_7$, with CMOS compatible input levels.	14-bit PWM output pins
$P6_1$-$P6_5$, $P6_7$			
$P6_6$/AN			Comparator input pin

PART NUMBERING

Product name M3811 0 M X - XXX SP

Package type
- SP : 64P4B package
- FP : 64P6N package
- SS : 64S1B package
- FS : 64D0 package

ROM number
- Omitted in some types

ROM/PROM size
- 1 : 4096 bytes
- 2 : 8192 bytes
- 3 : 12288 bytes
- 4 : 16384 bytes
- 5 : 20480 bytes
- 6 : 24576 bytes
- 7 : 28672 bytes
- 8 : 32768 bytes

The first 128 bytes and the last two bytes of ROM are reserved areas; they cannot be used

Memory type
- M : Mask ROM version
- E : EPROM or one-time programmable version

RAM size
- 0 . 192 bytes
- 1 : 256 bytes
- 2 · 384 bytes
- 3 512 bytes
- 4 : 640 bytes
- 5 768 bytes
- 6 . 896 bytes
- 7 · 1024 bytes

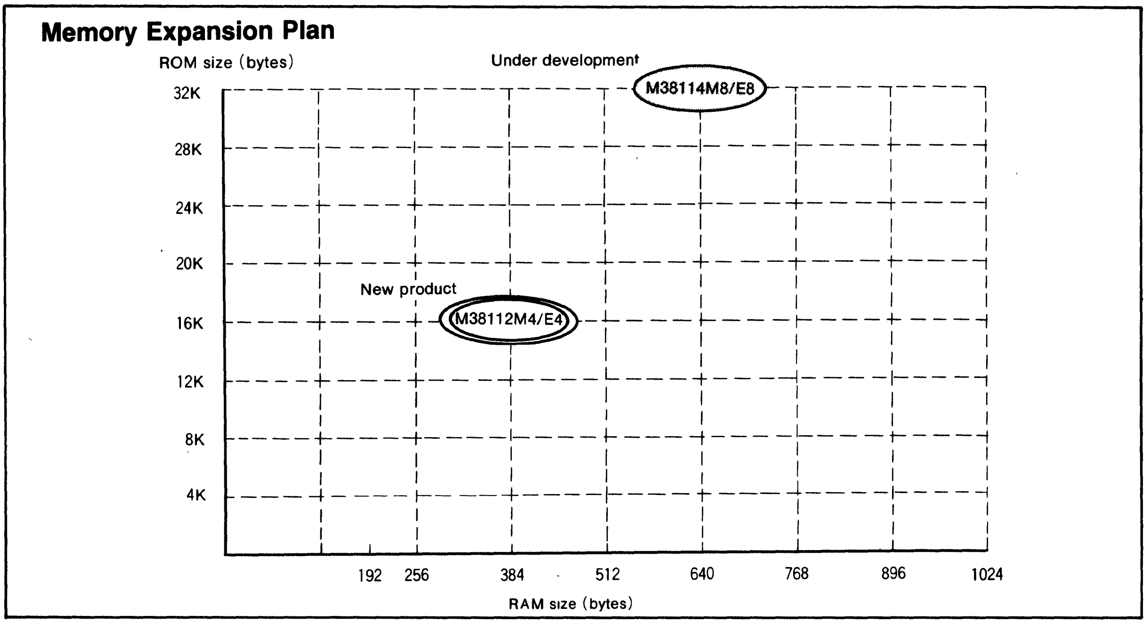
GROUP EXPANSION

Mitsubishi plans to expand the M3817x group as follows:

(1) Support for mask ROM, one-time programmable, and EPROM versions

(2) ROM/PROM size ····························16K to 32K bytes
RAM size ······································ 384 to 640 bytes

(3) Packages
64P4B ······························ Shrink plastic molded DIP
64P6N ······································Plastic molded QFP
64S1B ·····················Window type shrink ceramic DIP
80D0 ·······························Window type ceramic LCC



The development schedule and other details of products under development may be revised without notice.

Currently supported products are listed below. **As of March 1992**

Product name	(P) ROM size (bytes)	RAM size (bytes)	Package	Remarks
M38112M4-XXXSP	16K	382	64P4B	Mask ROM version
M38112E4-XXXSP				One-time programmable version
M38112E4SP				One-time programmable version (blank)
M38112E4SS			64S1B	EPROM version
M38112M4-XXXFP			64P6N	Mask ROM version
M38112E4-XXXFP				One-time programmable version
M38112E4FP				One-time programmable version (blank)
M38112E4FS			64D0	EPROM version

FUNCTIONAL DESCRIPTION
CENTRAL PROCESSING UNIT (CPU)

Microcomputers of the M3811x group use the standard MELPS 740 instruction set. Refer to the table of MELPS 740 addressing modes and machine instructions or the MELPS 740 Software Manual for details on the instruction set.

Machine-resident MELPS 740 instructions are as follows:

The FST and SLW instructions are not available for use.

The STP, WIT, MUL, and DIV instructions can be used.

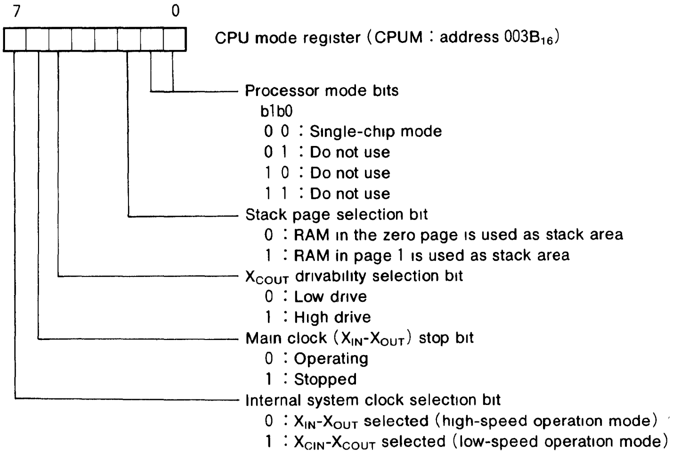
CPU MODE REGISTER

The CPU mode register is allocated to address 003B$_{16}$.

Bits 0 and 1 of this register are processor mode bits and should always be set to "0".

The CPU mode register contains the stack page selection bit.

For details of the X_{COUT} drivability selection bit, main clock stop bit, and internal system clock selection bit, see the section on the clock qeneration circuit.



CPU mode register (CPUM : address 003B$_{16}$)

Processor mode bits
b1b0
0 0 : Single-chip mode
0 1 : Do not use
1 0 : Do not use
1 1 : Do not use

Stack page selection bit
0 : RAM in the zero page is used as stack area
1 : RAM in page 1 is used as stack area

X_{COUT} drivability selection bit
0 : Low drive
1 : High drive

Main clock (X_{IN}-X_{OUT}) stop bit
0 : Operating
1 : Stopped

Internal system clock selection bit
0 : X_{IN}-X_{OUT} selected (high-speed operation mode)
1 : X_{CIN}-X_{COUT} selected (low-speed operation mode)

Fig. 1 Structure of CPU mode register

MEMORY

- **Special Function Register (SFR) Area**
  The Special Function Register area contains registers which control functions such as I/O ports and timers, and is located in the zero page area.
- **RAM**
  RAM is used for data storage as well for stack area.
- **ROM**
  The first 128 bytes and the last two bytes of ROM are reserved for device testing and the rest is user area for storing programs.
- **Interrupt Vector Area**
  The interrupt vector area contains reset and interrupt vectors.
- **Zero Page**
  The 256 bytes from addresses 0000_{16} to $00FF_{16}$ are called the zero page area. The internal RAM and the special function registers (SFR) are allocated to this area.
  The zero page addressing mode can be used to specify memory and register addresses in the zero page area. This dedicated zero page addressing mode enables access to this area with only 2 bytes.
- **Special Page**
  The 256 bytes from addresses $FF00_{16}$ to $FFFF_{16}$ are called the special page area. The special page addressing mode can be used to specify memory addresses in the special page area. This dedicated special page addressing mode enables access to this area with only 2 bytes.

RAM area

RAM capacity (bytes)	Address $XXXX_{16}$
192	$00FF_{16}$
256	$013F_{16}$
384	$01BF_{16}$
512	$023F_{16}$
640	$02BF_{16}$
768	$033F_{16}$
896	$03BF_{16}$
1024	$043F_{16}$

ROM area

ROM capacity (bytes)	Address $YYYY_{16}$	Address $ZZZZ_{16}$
4096	$F000_{16}$	$F080_{16}$
8192	$E000_{16}$	$E080_{16}$
12288	$D000_{16}$	$D080_{16}$
16384	$C000_{16}$	$C080_{16}$
20480	$B000_{16}$	$B080_{16}$
24576	$A000_{16}$	$A080_{16}$
28672	9000_{16}	9080_{16}
32768	8000_{16}	8080_{16}

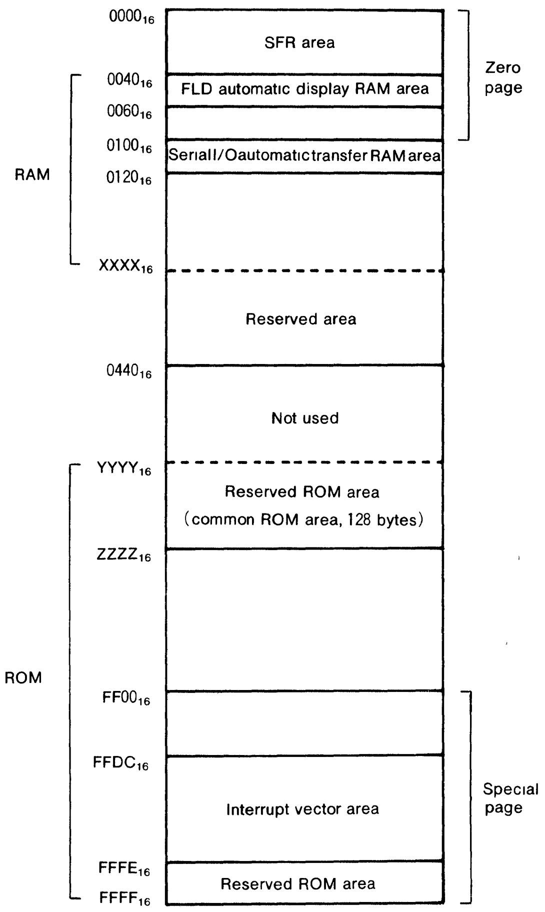


Fig. 2 Memory map diagram

0000_{16}	Port P0 (P0)	0020_{16}	
0001_{16}		0021_{16}	
0002_{16}	Port P1 (P1)	0022_{16}	
0003_{16}		0023_{16}	
0004_{16}	Port P2 (P2)	0024_{16}	Timer 1 (T1)
0005_{16}	Port P2 direction register (P2D)	0025_{16}	Timer 2 (T2)
0006_{16}	Port P3 (P3)	0026_{16}	Timer 3 (T3)
0007_{16}		0027_{16}	Timer 4 (T4)
0008_{16}	Port P4 (P4)	0028_{16}	Timer 12 mode register (T12M)
0009_{16}	Port P4 direction register (P4D)	0029_{16}	Timer 34 mode register (T34M)
$000A_{16}$	Port P5 (P5)	$002A_{16}$	
$000B_{16}$	Port P5 direction register (P5D)	$002B_{16}$	PWM control register (PWMCON)
$000C_{16}$	Port P6 (P6)	$002C_{16}$	PWM register (upper)(PWMH)
$000D_{16}$	Port P6 direction register (P6D)	$002D_{16}$	PWM register (lower)(PWML)
$000E_{16}$		$002E_{16}$	
$000F_{16}$		$002F_{16}$	
0010_{16}		0030_{16}	Comparator register (CMP)
0011_{16}		0031_{16}	
0012_{16}	Port P0 segment/digit switching register (P0SDR)	0032_{16}	
0013_{16}		0033_{16}	
0014_{16}	Port P2 digit/port switching register (P2DPR)	0034_{16}	
0015_{16}	Key-scan blanking register (KSCN)	0035_{16}	
0016_{16}	FLDC mode register (FLDM)	0036_{16}	
0017_{16}	FLD data pointer (FLDDP)	0037_{16}	
0018_{16}	Serial I/O automatic transfer data pointer (SIODP)	0038_{16}	High-breakdown-voltage port control register (HVPC)
0019_{16}	Serial I/O1 control register (SIO1CON)	0039_{16}	
$001A_{16}$	Serial I/O automatic transfer control register (SIOAC)	$003A_{16}$	Interrupt edge selection register (INTEDGE)
$001B_{16}$	Serial I/O1 register (SIO1)	$003B_{16}$	CPU mode register (CUPM)
$001C_{16}$	Serial I/O automatic transfer interval register (SIOAI)	$003C_{16}$	Interrupt request register 1 (IREQ1)
$001D_{16}$	Serial I/O2 control register (SIO2CON)	$003D_{16}$	Interrupt request register 2 (IREQ2)
$001E_{16}$		$003E_{16}$	Interrupt control register 1 (ICON1)
$001F_{16}$	Serial I/O2 register (SIO2)	$003F_{16}$	Interrupt control register 2 (ICON2)

Fig. 3 Memory map of special function register (SFR)

I/O PORTS

- **Direction Registers**

The M3811x group microprocessors have 27 programmable I/O pins arranged in four I/O ports (ports $P2_4$-$P2_7$, $P4_1$-$P4_7$, P5 and P6). The I/O ports have direction registers which determine the input/output direction of each individual pin. Each bit in a direction register corresponds to one pin, each pin can be set to be input or output.

When "0" is written to the bit corresponding to a pin, that pin becomes an input pin. When "1" is written to that bit, that pin becomes an output pin.

If data is read from a pin which is set for output, the value of the port output latch is read, not the value of the pin itself. Pins set to input are floating. If a pin set to input is written to, only the port output latch is written to and the pin remains floating.

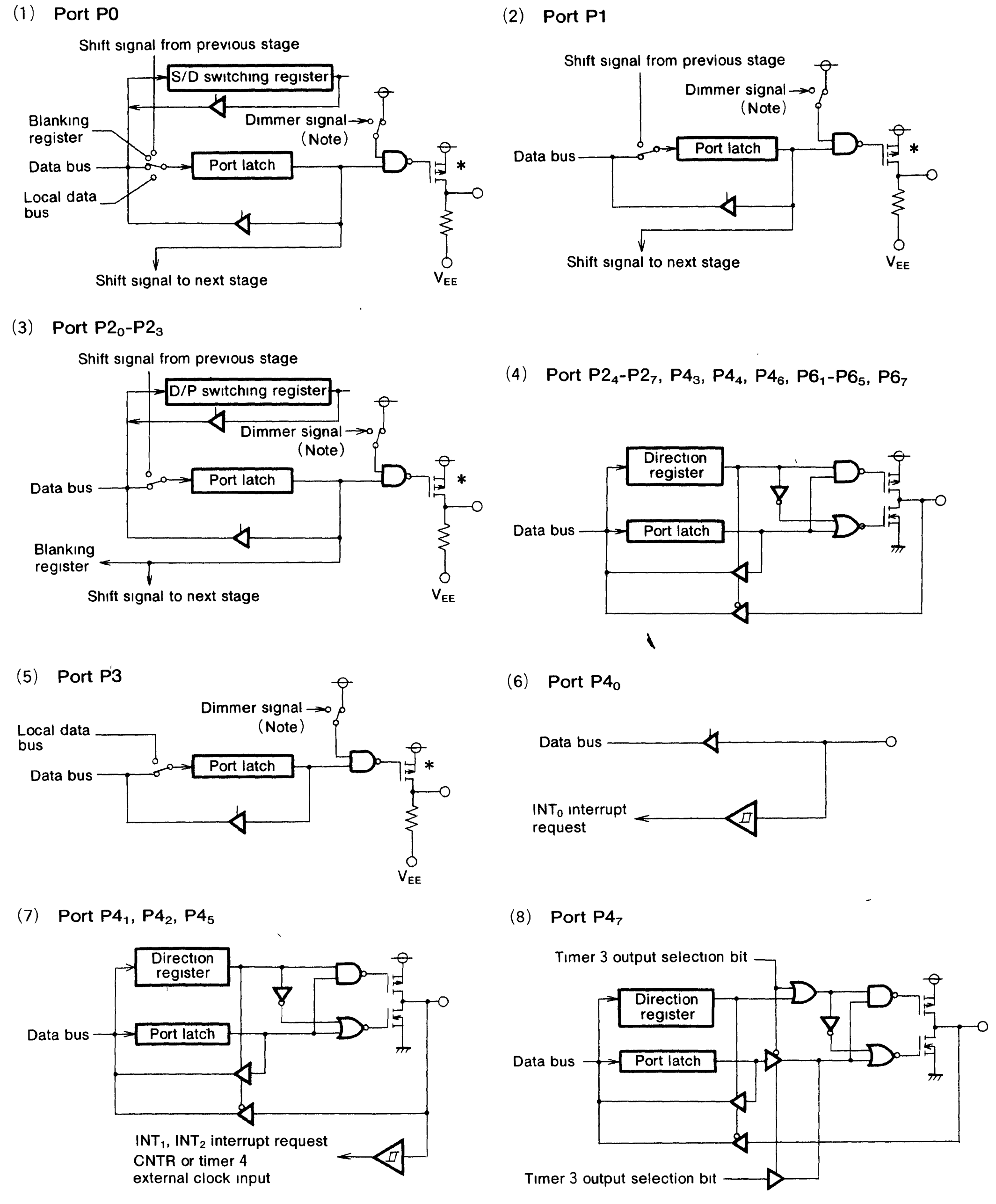
- **High-Breakdown-Voltage Output Ports**

The M3811x group microprocessors have four ports with high-breakdown-voltage pins(ports P0, P1, $P2_0$-$P2_3$, P3). The high-breakdown-voltage ports have P-channel open drain output with a breakdown voltage of $V_{CC}-40V$. Each pin in Ports P0, P1, $P2_0$-$P2_3$ and P3 has an internal pull-down resistor connected to V_{EE}. At reset, the P-channel output transistor of each port latch is turned off, so it is forced to the level of V_{EE} by the pull-down resistor.

Writing "1" to bit 0 of the high-breakdown-voltage port control register(address 0038_{16})slows the transition of the output transistors to reduce transient noise. At reset, bit 0 of the high-breakdown-voltage port control register is set to "0" (strong drive).

Pin	Name	Input/Output	I/O Format	Non-Port Function	Related SFRs	Diagram No.
$P0_0/SEG_8/DIG_0$–$P0_7/SEG_{15}/DIG_7$	Port P0	Output	High-breakdown-voltage P-channel open-drain output with pull-down resistor	FLD automatic display function	FLDC mode register Segment/digit switching register High-breakdown-voltage port control register	(1)
$P1_0/DIG_8$–$P1_7/DIG_{15}$	Port P1	Output	High-breakdown-voltage P-channel open-drain output with pull-down resistor	FLD automatic display function	FLDC mode register High-breakdown-voltage port control register	(2)
$P2_0/DIG_{16}$–$P2_3/DIG_{19}$	Port P2	Output	High-breakdown-voltage P-channel open-drain output with pull-down resistor	FLD automatic display function	FLDC mode register Digit/port switching register High-breakdown-voltage port control register	(3)
$P2_4$-$P2_7$		Input/output, individual bits	TTL level input CMOS 3-state output			(4)
$P3_0/SEG_0$–$P3_7/SEG_7$	Port P3	Output	High-breakdown-voltage P-channel open-drain output with pull-down resistor	FLD automatic display function	FLDC mode register High-breakdown-voltage port control register	(5)
$P4_0/INT_0$	Port P4	Input	CMOS level input	External interrupt input	Interrupt edge selection register	(6)
$P4_1/INT_1$, $P4_2/INT_2$		Input/output, individual bits	CMOS level input CMOS 3-state output	External interrupt input	Interrupt edge selection register	(7)
$P4_3$, $P4_4$, $P4_6$						(4)
$P4_5/CNTR$				Event count input	Timer 34 mode register	(7)
$P4_7/T_{OUT}$				Timer 3 output	Timer 34 mode register	(8)
$P5_0/S_{IN1}$,	Port P5	Input/output, individual bits	CMOS level input N-channel open-drain output	Serial I/O1 function I/O	Serial I/O1 control register Serial I/O automatic transfer control register	(9)
$P5_1/S_{OUT1}$, $P5_2/S_{CLK1}$,						(10)
$P5_3/\overline{S_{RDY1}}/\overline{CS}/S_{CLK12}$						(11)
$P5_4/S_{IN2}$,				Serial I/O2 function I/O	Serial I/O2 control register	(9)
$P5_5/S_{OUT2}$, $P5_6/S_{CLK2}$,						(10)
$P5_7/\overline{S_{RDY2}}$						(11)
$P6_0/PWM$	Port P6	Input/output, individual bits	CMOS level input CMOS 3-state output	14-bit PWM output	PWM mode register PWML register PWMH register	(12)
$P6_1$-$P6_5$, $P6_7$						(4)
$P6_6/AN$				Comparator input	Comparator register	(13)

Note. Make sure that the input level at each pin is either 0V or V_{CC} during execution of the STP instruction
If an input level is at an intermediate potential, a current will flow in the input-stage gate



* : High-breakdown-voltage P-channel transistor

Note. The dimmer signal sets the Toff timing

Fig. 4 Port block diagram (1)

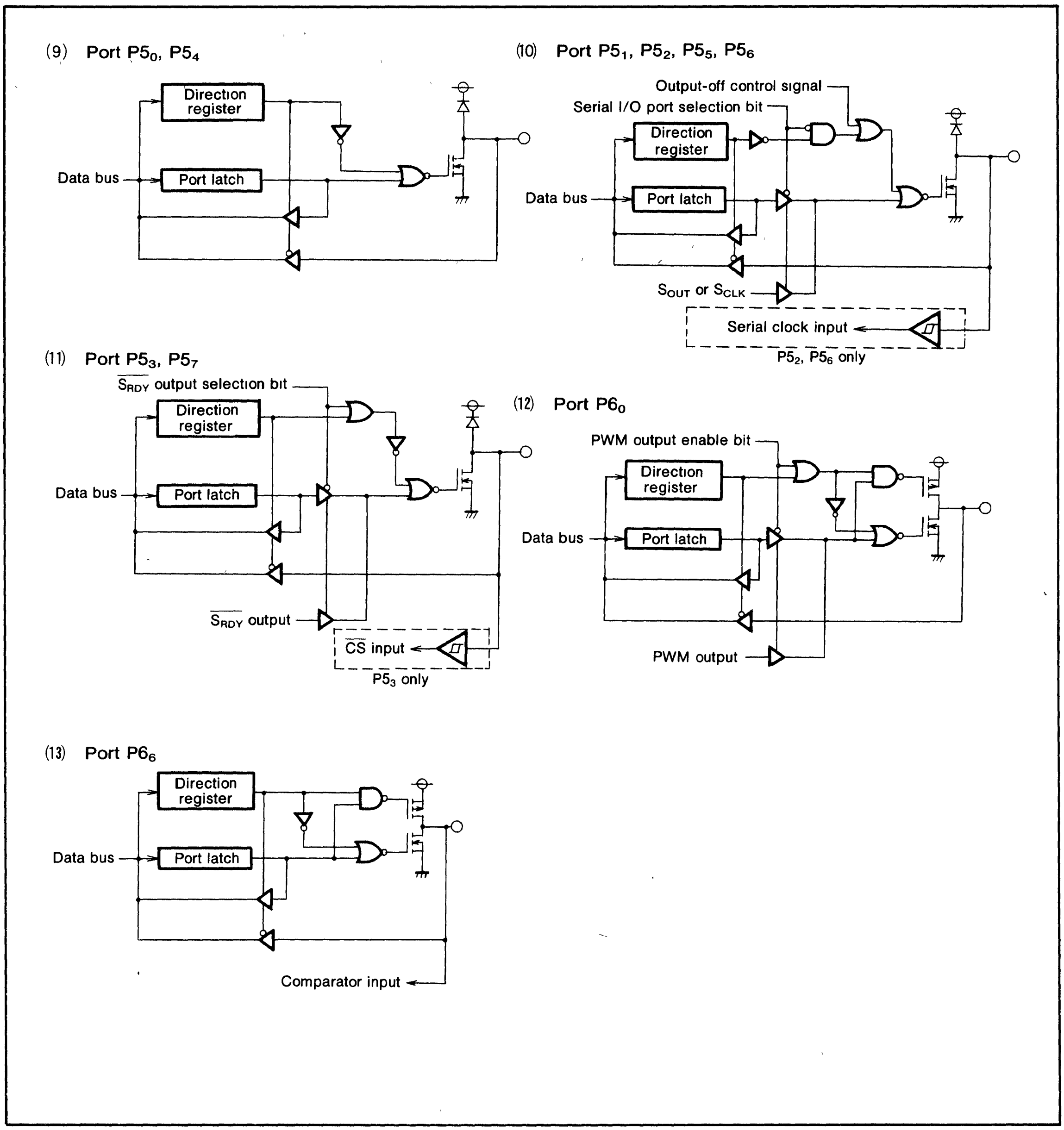


Fig. 5 Port block diagram (2)

INTERRUPTS

A total of 14 source can generate interrupts: 4 external, 9 internal, and 1 software.

- **Interrupt Control**

  Each interrupt is controlled by its interrupt request bit, its interrupt enable bit, and the interrupt disable flag except for the software interrupt set by the BRK instruction. An interrupt is generated if the corresponding interrupt request and enable bits are "1" and the interrupt disable flag is "0".

  Interrupt enable bits can be set or cleared by software.

  Interrupt request bits can be cleared by software, but cannot be set by software.

  The I flag disables all interrupts except for the BRK instruction interrupt.

- **Interrupt Operation**

  When an interrupt is received, the program counter and processor status register are automatically pushed onto the stack. The interrupt disable flag is set to inhibit other interrupts from interfering. The corresponding interrupt request bit is cleared and the interrupt jump destination address is read from the vector table into the program counter.

- **Notes on Use**

  If you will change interrupt edge selection from rising edge to falling edge, interrupt request bit will be set to "1" automatically. Therefore, please make following process;

(1) Disable INT which is selected.
(2) Change INT edge selection.
(3) Clear interrupt request which is selected.
(4) Enable INT which is selected.

Table 1. Interrupt vector addresses and priorities

Interrupt Cause	Priority	Vector Address (Note 1)		Interrupt Request Generation Conditions	Remarks
		High	Low		
Reset (Note 2)	1	FFFD$_{16}$	FFFC$_{16}$	At reset	Non-maskable
INT$_0$	2	FFFB$_{16}$	FFFA$_{16}$	At detection of either rising or falling edge of INT$_0$ input	External interrupt (active edge selectable)
INT$_1$	3	FFF9$_{16}$	FFF8$_{16}$	At detection of either rising or falling edge of INT$_1$ input	External interrupt (active edge selectable)
INT$_2$	4	FFF7$_{16}$	FFF6$_{16}$	At detection of either rising or falling edge of INT$_2$ input	External interrupt (active edge selectable)
Serial I/O1	5	FFF5$_{16}$	FFF4$_{16}$	At end of data transfer	Valid when serial I/O normal mode is selected
Serial I/O automatic transfer				At end of final data transfer	Valid when serial I/O automatic transfer mode is selected
Serial I/O2	6	FFF3$_{16}$	FFF2$_{16}$	At end of data transfer	
Timer 1	7	FFF1$_{16}$	FFF0$_{16}$	At timer 1 overflow	
Timer 2	8	FFEF$_{16}$	FFEE$_{16}$	At timer 2 overflow	STP release timer overflow
Timer 3	9	FFED$_{16}$	FFEC$_{16}$	At timer 3 overflow	
Timer 4	10	FFEB$_{16}$	FFEA$_{16}$	At timer 4 overflow	
CNTR	11	FFE9$_{16}$	FFE8$_{16}$	At detection of either rising or falling edge of CNTR input	External interrupt (active edge selectable)
FLD blanking	12	FFE5$_{16}$	FFE4$_{16}$	At fall of final digit	Valid when FLD blanking interrupt is selected
FLD digit				At rise of each digit	Valid when FLD digit interrupt is selected
BRK instruction	13	FFDD$_{16}$	FFDC$_{16}$	At BRK instruction execution	Non-maskable software interrupt

Note 1. Vector addresses contain interrupt jump destination addresses.
2. Reset function in the same way as an interrupt with the highest priority.

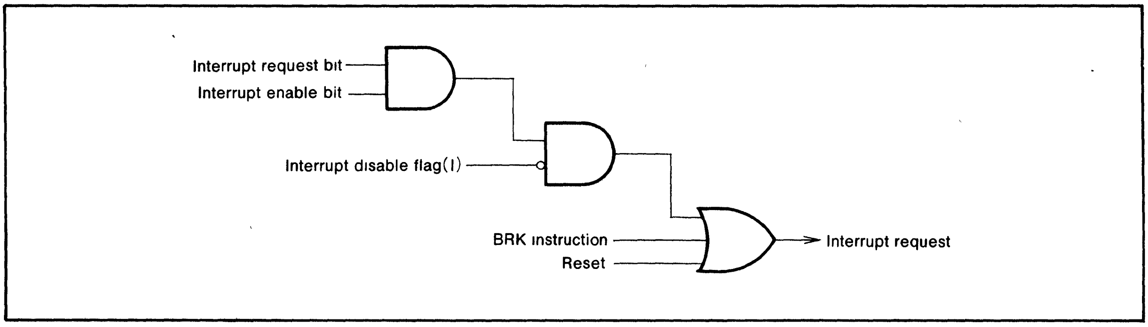


Fig. 6 Interrupt control

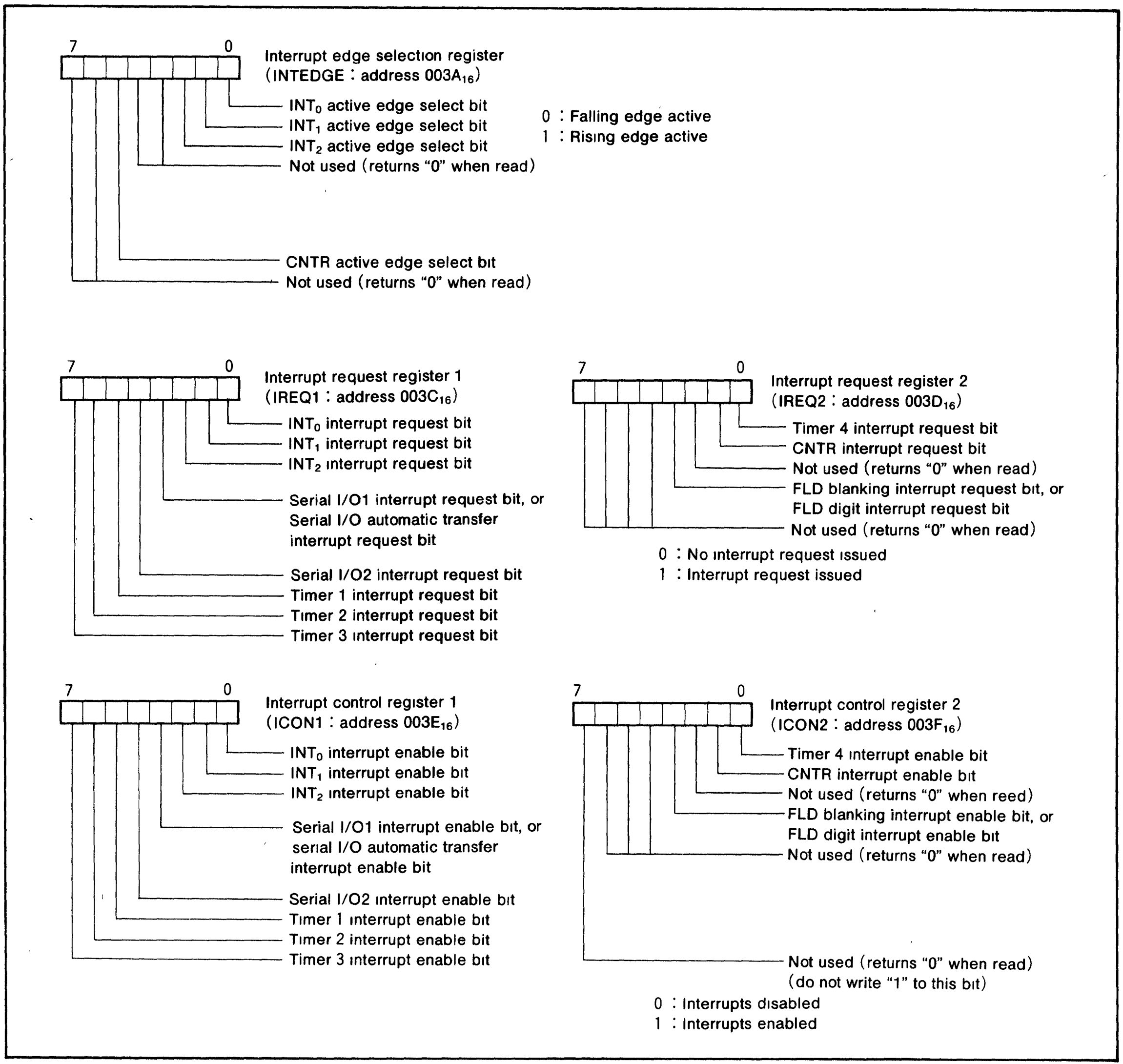


Fig. 7 Structure of interrupt-related registers

TIMERS

Microcomputers of the M3811x group have four built-in timers. The timers count down. Once a timer reaches 00_{16}, the next count pulse loads the contents of the corresponding timer latch into the timer, and sets the corresponding interrupt request bit to 1. Each timer also has a stop bit that stops the count of that timer when it is set to "1".

Note that the system clock ϕ can be set to either high-speed mode or low-speed mode by the CPU mode register.

- **Timer 1 and Timer 2**

  The count sources of timer 1 and timer 2 can be selected by setting the timer 12 mode register.

  When the chip is reset or the STP instruction is executed, all bits of the timer 12 mode register are cleared, timer 1 is set to FF_{16}, and timer 2 is set to 01_{16}.

- **Timer 3 and Timer 4**

  The count sources of timer 3 and timer 4 can be selected by setting the timer 34 mode register.

  Timer 3 can also output a rectangular waveform from the $P4_7/T_{OUT}$ pin. The waveform changes polarity each time timer 3 overflows.

  When Timer 4 is assigned to external event count mode, rising edge is active.

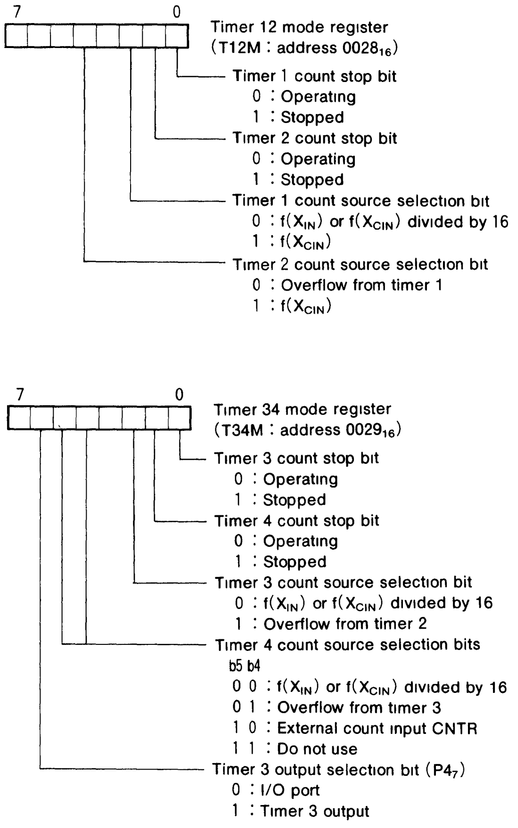


Fig. 8 Structure of timer-related registers

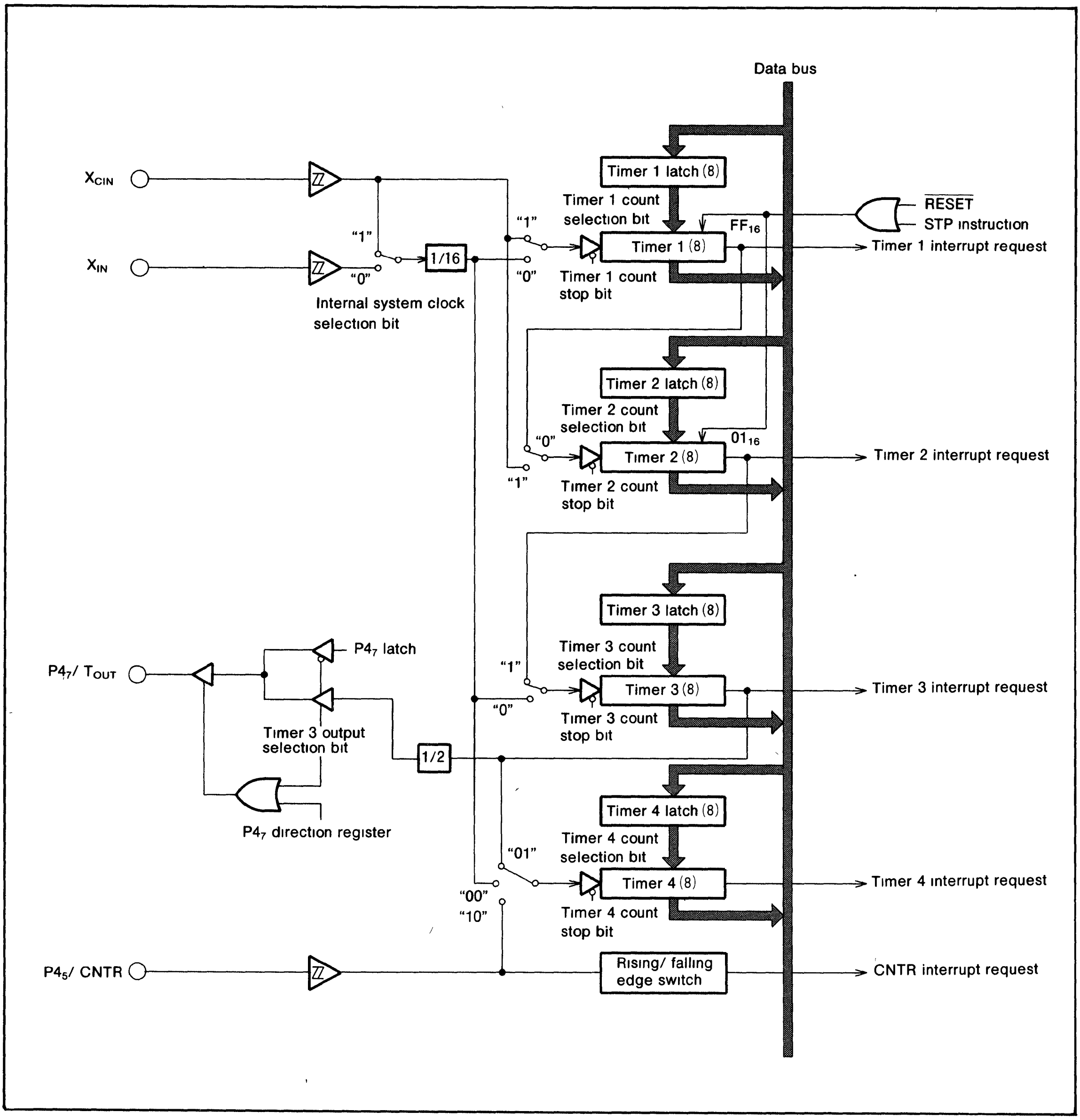


Fig. 9 Timer block diagram

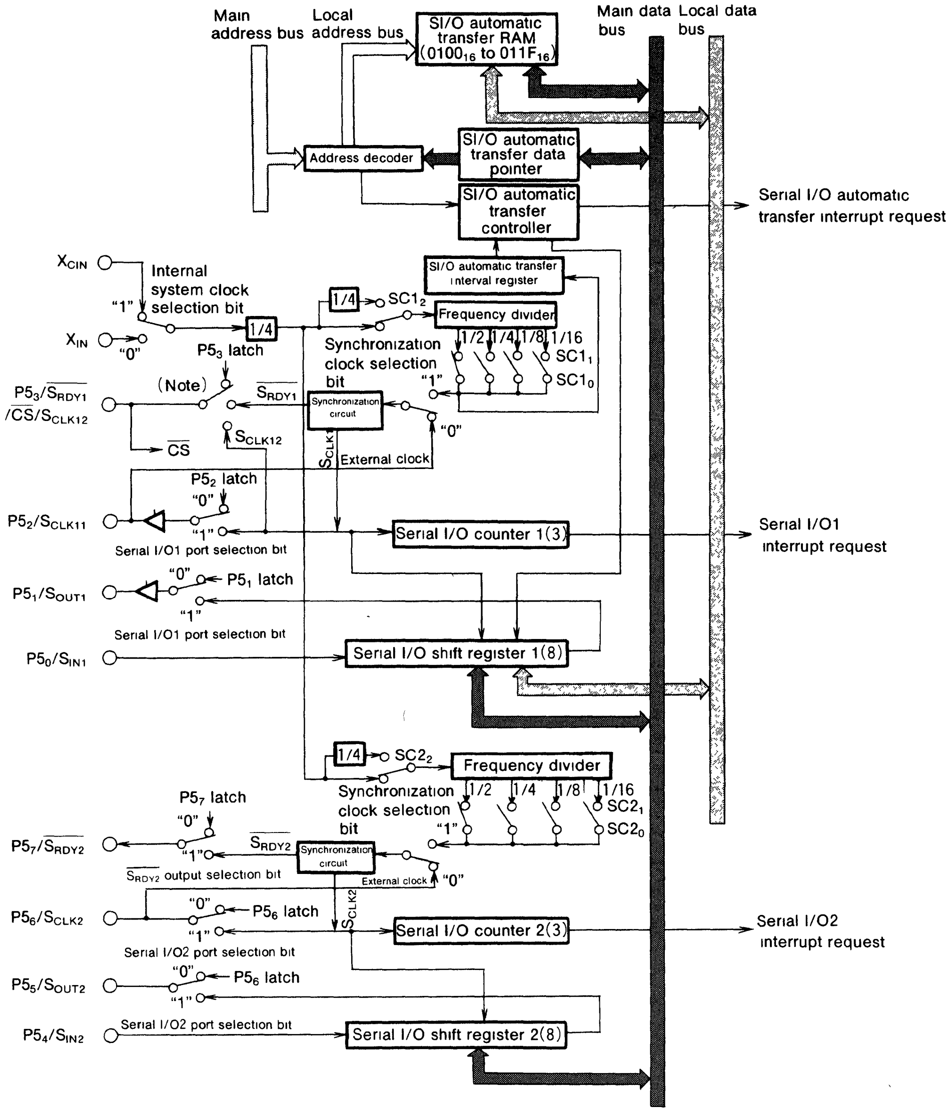
SERIAL I/O

Microcomputers of the M3811x group have two built-in 8-bit clock synchronized serial I/O channels (serial I/O1 and serial I/O2).

Serial I/O1 has a built-in automatic transfer function.Normal serial operation can be set via the serial I/O automatic transfer control register (address $001A_{16}$).

Serial I/O2 can only be used in normal operation mode.

The I/O pins of the serial I/O function also operate as I/O port P5, and their operation is selected by the serial I/O control registers (addresses 0019_{16} and $001D_{16}$).



Note. Selection is by the synchronization clock selection bit, the $\overline{S_{RDY1}}$ output selection bit, and the serial I/O1 port selection bit of the serial I/O1 control register, and the automatic transfer control bit and synchronization clock output pin selection bit of the serial I/O automatic transfer control register

Fig. 10 Serial I/O block diagram

(Serial I/O Control Registers) SIO1CON, SIO2CON

Each of the serial I/O control registers (addresses 0019_{16} and $001D_{16}$) contains seven bits that select various control parameters of the serial I/O function.

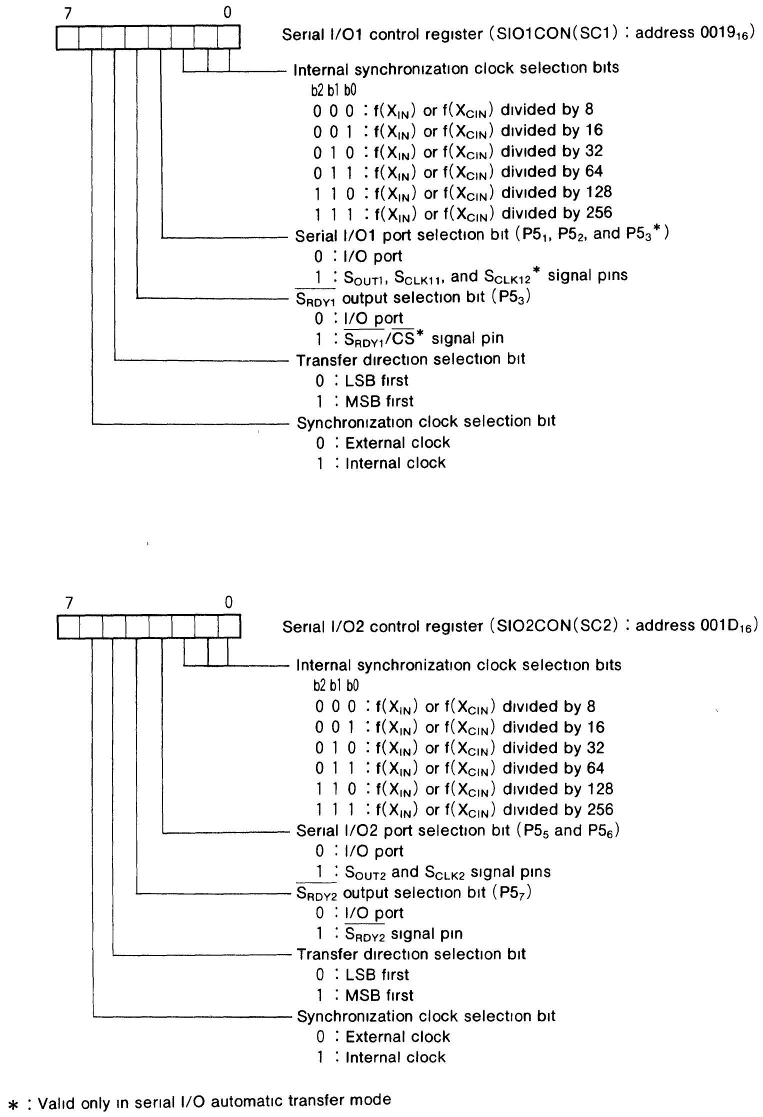
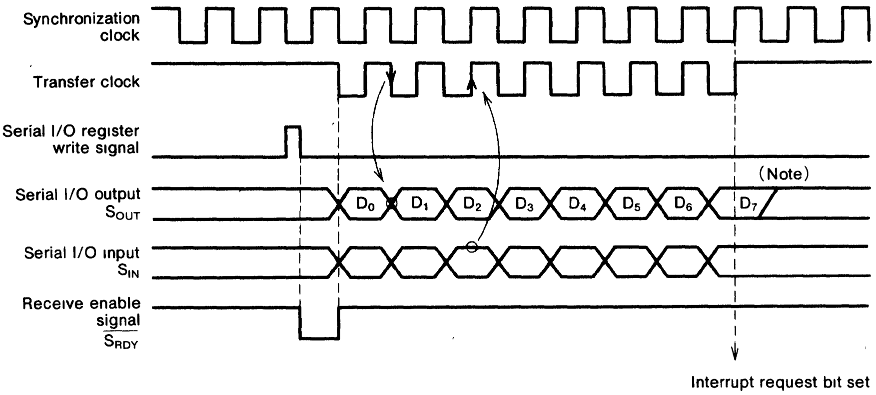


Fig. 11 Structure of serial I/O control registers

(1) Operation in Normal Serial I/O Mode
Either an internal clock or an external clock can be selected as the synchronization clock for serial I/O transfer. A dedicated divider is built-in as the internal clock, giving a choice of six clocks.
If internal clock is selected, transfer start is activated by a write signal to a serial I/O register (address $001B_{16}$ or $001F_{16}$). After eight bits have been transferred, the S_{OUT} pin goes to high impedance.
If external clock is selected, the clock must be controlled externally because the contents of the serial I/O register continue to shift while the transfer clock is input. In this case, note that the S_{OUT} pin does not go to high impedance at the completion of data transfer. The interrupt request bit is set at the end of the transfer of eight bits, regardless of whether the internal or external clock is selected.



Note. If internal clock is selected, the S_{OUT} pin is at high impedance after transfer ends.

Fig. 12 Serial I/O timing in normal mode (for LSB first)

(2) Serial I/O Automatic Transfer Mode
The serial I/O1 function has an automatic transfer function. For automatic transfer, switch to the automatic transfer mode by setting the serial I/O automatic transfer control register (address $001A_{16}$).
The following memory spaces are added to the circuits used for the serial I/O1 function in ordinary mode, to enable automatic transfer mode:

- 32 bytes of serial I/O automatic transfer RAM
- A serial I/O automatic transfer control register
- A serial I/O automatic transfer interval register
- A serial I/O automatic transfer data pointer

When using serial I/O automatic transfer, set the serial I/O control register (address 0019_{16}) in the same way as for ordinary mode. However, note that if external clock is selected and bit 4 (the $\overline{S_{RDY1}}$ output selection bit) of the serial I/O1 control register is set to "1", port $P5_3$ becomes the $\overline{CS}$ input pin.

(Serial I/O Automatic Transfer Control Register)
SIOAC

The serial I/O automatic transfer control register (address $001A_{16}$) contains four bits that select various control parameters for automatic transfer.

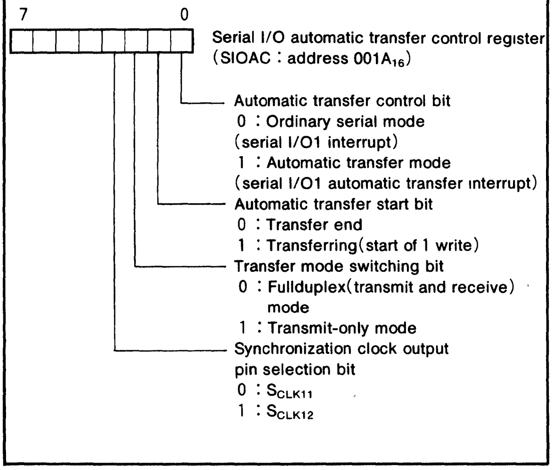


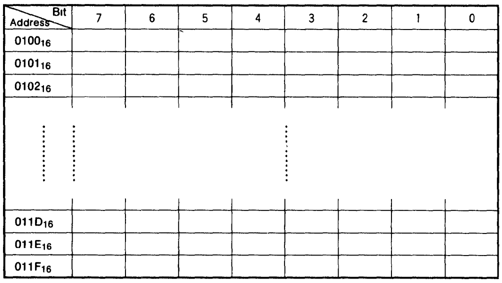
Fig. 13 Structure of serial I/O automatic transfer control register

(Serial I/O Automatic Transfer Data Pointer) SIODP

The serial I/O automatic transfer data pointer (address 0018_{16}) contains five bits that indicate addresses in serial I/O automatic transfer RAM (each address in memory is actually the value in the serial I/O automatic transfer data pointer plus 0100_{16}).

Set the serial I/O automatic transfer data pointer to (the number of transfer data−1), to specify the storage position of the start of data.

- **Serial I/O Automatic Transfer RAM**
  The serial I/O automatic transfer RAM is the 32 bytes from address 0100_{16} to address $011F_{16}$.



Address \ Bit	7	6	5	4	3	2	1	0
0100_{16}								
0101_{16}								
0102_{16}								
⋮	⋮				⋮			
$011D_{16}$								
$011E_{16}$								
$011F_{16}$								

Fig. 14 Bit allocation of serial I/O automatic transfer RAM

- **Setting of Serial I/O Automatic Transfer Data**
  When data is stored in the serial I/O automatic transfer RAM, it is stored with the start of the data at the address set by the serial I/O automatic transfer data pointer and the end of the data at address 0100_{16}.

(Serial I/O Automatic Transfer Interval Register) SIOAI

The serial I/O automatic transfer interval register (address $001C_{16}$) consists of a 5-bit counter that determines the transfer interval Ti during automatic transfer.

If a value n is written to the serial I/O automatic transfer interval register, a value of $Ti=(n+2)\times Tc$ is generated, where Tc is the length of one bit of the transfer clock. However, note that this transfer interval setting is only valid when internal clock has been selected as the clock source.

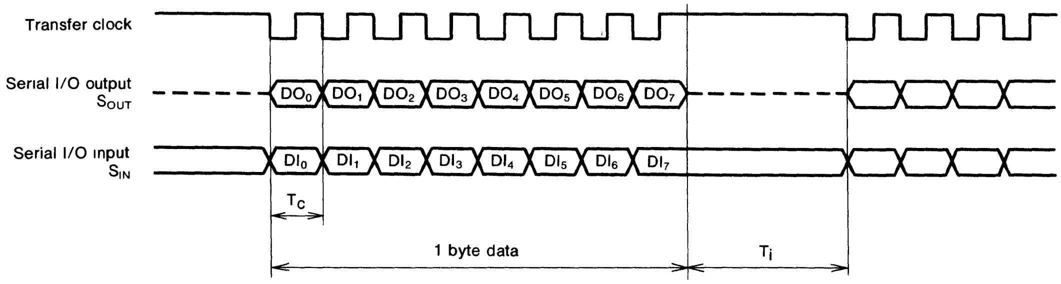


Fig. 15 Serial I/O automatic transfer interval timing

- **Setting of Serial I/O Automatic Transfer Timing**
  Use the serial I/O1 control register (address 0019_{16}) and the serial I/O automatic transfer interval register (address $001C_{16}$) to set the timing of serial I/O automatic transfer.
  The serial I/O1 control register sets the transfer clock speed, and the serial I/O automatic transfer interval register sets the serial I/O automatic transfer interval.
  This setting of transfer interval is valid only when internal clock is selected as the clock source.
- **Start of Serial I/O Automatic Transfer**
  Automatic transfer mode is set by writing "1" to bit 0 of the serial I/O automatic transfer control register (address $001A_{16}$), then automatic transfer starts when "1" is written to that bit. Bit 1 of the serial I/O automatic transfer control register is always "1" during automatic transfer; writing "0" to it is one way to end automatic transfer.
- **Operation in Serial I/O Automatic Transfer Modes**
  There are two modes for serial I/O automatic transfer: full duplex mode and transmit-only mode. Either internal or external clock can be selected for each of these modes.

(2.1) Operation in Full Duplex Mode

In full duplex mode, data can be transmitted and received at the same time. Data in the automatic transfer RAM is sent in sequence and simultaneously receive data is written to the automatic transfer RAM, in accordance with the serial I/O automatic transfer data pointer.

The transfer timing of each bit is the same as in ordinary operation mode, and the transfer clock stops at "H" after eight transfer clocks are counted. If internal clock is selected, the transfer clock remains at "H" for the time set by the serial I/O automatic transfer interval register, then the data at the next address indicated by the serial I/O automatic transfer data pointer is transferred. If external clock is selected, the setting of the automatic transfer interval register is invalid, so the user must ensure that the transfer clock is controlled externally.

Data transfer ends when the contents of the serial I/O automatic transfer pointer reach "00_{16}". At that point, the serial I/O automatic transfer interrupt request bit is set to "1" and bit 1 of the serial I/O automatic transfer control register is cleared to "0" to complete the serial I/O automatic transfer.

(2.2) Operation in Transmit-Only Mode

The operation in transmit-only mode is the same as that in full duplex mode, except that data is not transferred from the serial I/O1 register to the serial I/O automatic transfer RAM.

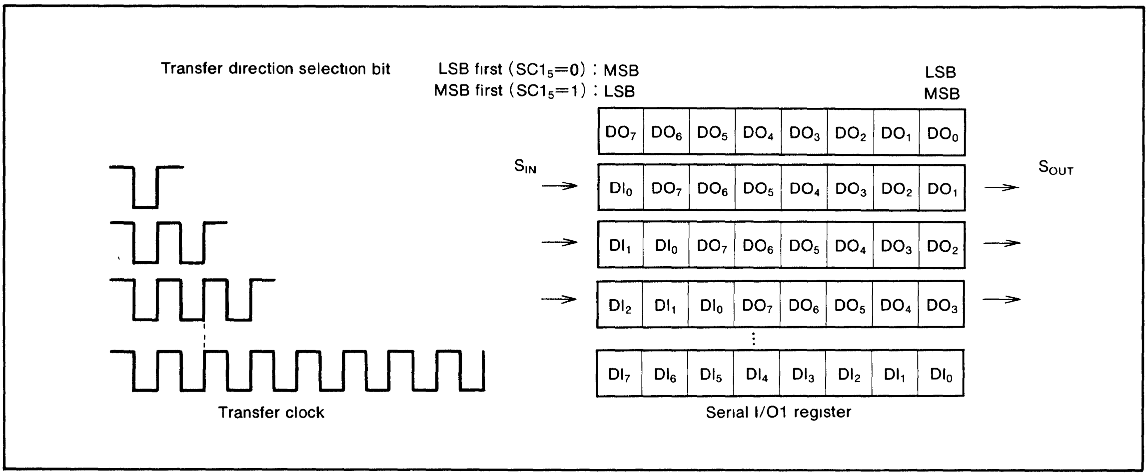


Fig. 16 Serial I/O1 register in full duplex mode

(2.3) If Internal Clock is Selected

If internal clock is selected, the $P5_3/\overline{S_{RDY1}}/\overline{CS}/S_{CLK12}$ pin can be used as the $\overline{S_{RDY1}}$ pin by setting the $SC1_4$ bit to "1".

If internal clock is selected, the $P5_3$ pin can be used as the synchronization clock output pin S_{CLK12} by setting the $SIOAC_3$ bit to "1". In this case, the S_{CLK11} pin is at high impedance.

Select the function of the $P5_3/\overline{S_{RDY1}}/\overline{CS}/S_{CLK12}$ and $P5_2/S_{CLK11}$ pins by setting bit 3 ($SC1_3$), bit 4 ($SC1_4$), and bit 6 ($SC1_6$) of the serial I/O1 control register (address 0019_{16}) and bit 3 ($SIOAC_3$) of the serial I/O automatic transfer control register (address $001A_{16}$). (See Table 2.)

If using the S_{CLK11} and S_{CLK12} pins for switching, set the $P5_3/\overline{S_{RDY1}}/\overline{CS}/S_{CLK12}$ pin to $P5_3$ by setting the $SC1_4$ bit to "0", and set the $P5_3$ direction register to input mode.

Make sure that the $SIOAC_3$ bit is switched after automatic transfer is completed, while the transfer clock is still "H".

Table 2. S_{CLK11} and S_{CLK12} selection

$SC1_6$	$SC1_4$	$SC3_3$	$SIOAC_3$	$P5_2/S_{CLK11}$	$P5_3/S_{CLK12}$
1	0	1	0	S_{CLK11}	$P5_3$
			1	High impedanse	S_{CLK12}

Note. $SC1_3$: Serial I/O1 port selection bit
$SC1_4$: $\overline{S_{RDY1}}$ output selection bit
$SC1_6$: Synchronization clock selection bit
$SIOAC_3$: Synchronization clock output pin selection bit

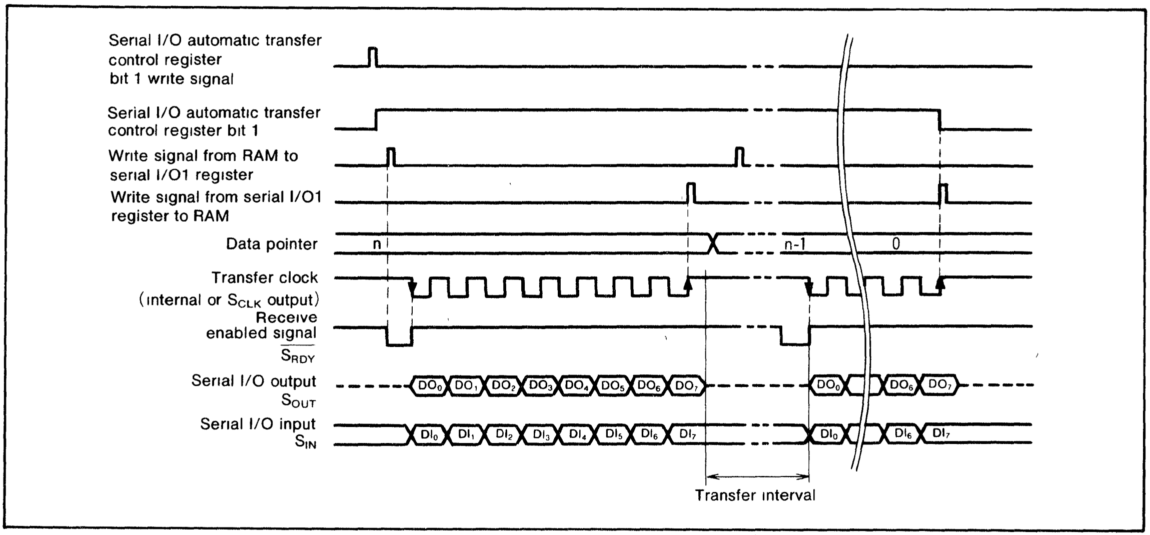


Fig. 17 Timing during serial I/O automatic transfer (internal clock selected, $\overline{S_{RDY}}$ used)

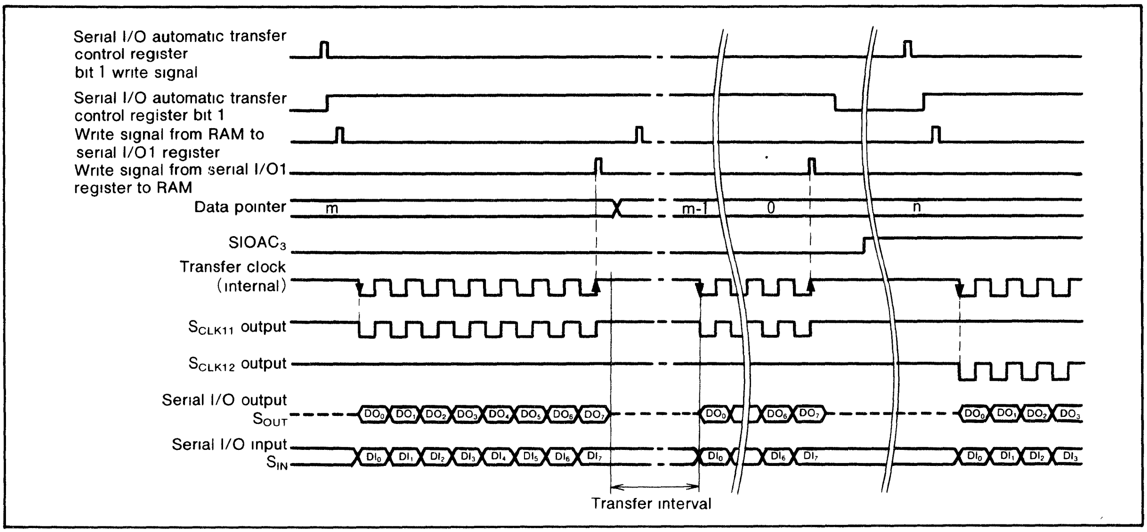


Fig. 18 Timing during serial I/O automatic transfer (internal clock selected, S_{CLK11} and S_{CLK12} used)

(2.4) If External Clock is Selected

If an external clock is selected, the internal clock and the transfer interval set by the serial I/O automatic transfer interval register are invalid, but the serial I/O output pin S_{OUT} and the internal transfer clock can be controlled from the outside by setting the $\overline{S_{RDY1}}$ and $\overline{CS}$ (input) pins.

When the $\overline{CS}$ input is "L", the S_{OUT} pin and the internal transfer clock are enabled. When the $\overline{CS}$ input is "H", the S_{OUT} pin is at high impedance and the internal transfer clock is at "H".

Select the function of the $P5_3/\overline{S_{RDY1}}/\overline{CS}/S_{CLK12}$ pin by setting bit 4 ($SC1_4$) and bit 6 ($SC1_6$) of the serial I/O1 control register (address 0019_{16}) and bit 0 ($SIOAC_0$) of the serial I/O automatic transfer control register (address $001A_{16}$).

Make sure that the $\overline{CS}$ pin switches from "L" to "H" or from "H" to "L" while the transfer clock (S_{CLK} input) is "H" after one byte of data has been transferred.

If external clock is selected, make sure that the external clock goes "L" after at least nine cycles of the internal system clock ϕ after the start bit is set. Leave at least 11 cycles of the system clock ϕ free for the transfer interval after one byte of data has been transferred.

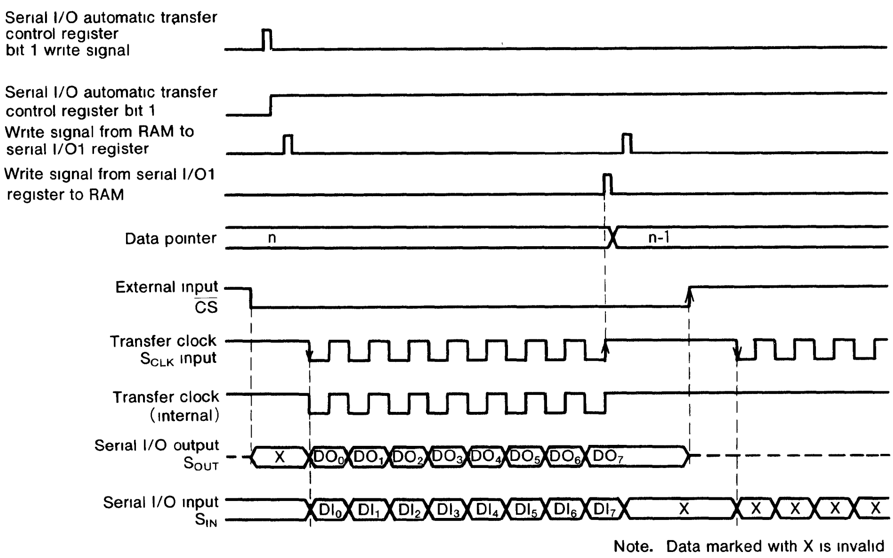
If $\overline{CS}$ input is not being used, note that the S_{OUT} pin will not go high impedance, even after transfer is completed.

If $\overline{CS}$ input is not being used, or if $\overline{CS}$ is "L", control the external clock because the data in the serial I/O register will continue to shift while the external clock is input, even after the completion of automatic transfer. (Note that the automatic transfer interrupt request bit is set and bit 1 of the automatic transfer register is cleared at the point at which the specified number of bytes of data have been transferred.)

Table 3. $P5_3/\overline{S_{RDY1}}/\overline{CS}$ selection

$SC1_6$	$SC1_4$	$SIOAC_0$	$P5_3/\overline{S_{RDY1}}/\overline{CS}$
0	0	X	$P5_3$
	1	0	$\overline{S_{RDY1}}$
		1	$\overline{CS}$

Note. $SC1_4$: $\overline{S_{RDY1}}$ output selection bit
$SC1_6$: Synchronization clock selection bit
$SIOAC_0$: Automatic transfer control bit



Note. Data marked with X is invalid

Fig. 19 Timing during serial I/O automatic transfer (external clock selected)

PULSE WIDTH MODULATION (PWM) OUTPUT CIRCUIT

Microcomputers of the M3811x group have a PWM function with a 14-bit resolution. When the oscillation frequency X_{IN} is 4MHz, the minimum resolution bit width is 500ns and the cycle period is 8192μs. The PWM timing generator supplies a PWM control signal based on a signal that is half the frequency of the X_{IN} clock.

The explanation in the rest of this data sheet assumes X_{IN}= 4MHz.

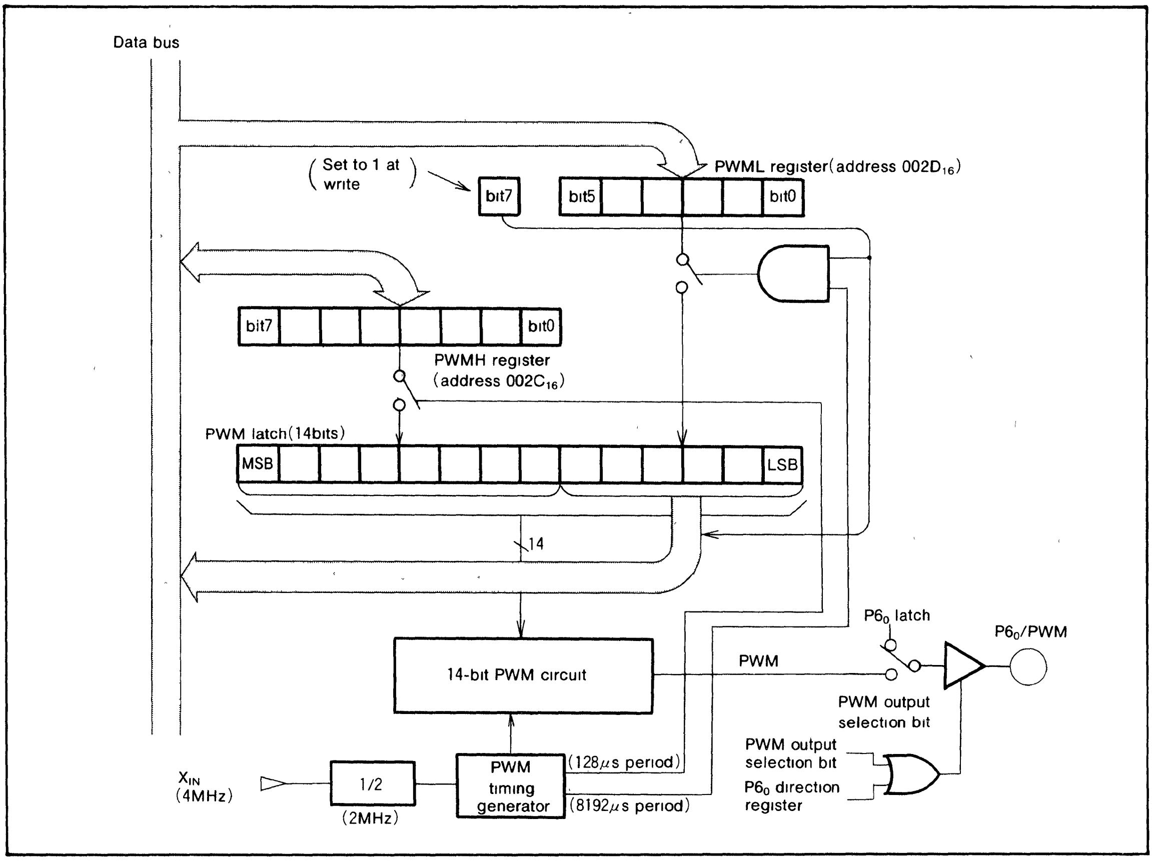


Fig. 20 PWM block diagram

(1) Data Set-up

The PWM output pin also functions as port $P6_0$. Set port $P6_0$ to be the PWM output pin by setting bit 0 of the PWM mode register (address $002B_{16}$). The upper eight bits of output data are set in the upper PWM register PWMH (address $002C_{16}$) and the lower six bits are set in the lower PWM register PWML (address $002D_{16}$).

(2) Transfer From Register to Latch

Data written to the PWML register is transferred to the PWM latch once in each PWM period (every 8192μs), and data written to the PWMH register is transferred to the PWM latch once in each sub-period (every 128μs). When the PWML register is read, the contents of the latch are read. However, bit 7 of the PWML register indicates whether the transfer to the PWM latch is completed; the transfer is completed when bit 7 is "0".

Table 4. Relationship between lower 6 bits of data and period set by the ADD bit

Lower 6 Bits of Data(PWML)	Sub-periods tm Lengthened (m =0 to 63)
0 0 0 0 0 $\overset{LSB}{0}$	None
0 0 0 0 0 1	m=32
0 0 0 0 1 0	m=16, 48
0 0 0 1 0 0	m= 8, 24, 40, 56
0 0 1 0 0 0	m= 4, 12, 20, 28, 36, 44, 52, 60
0 1 0 0 0 0	m= 2, 6, 10, 14, 18, 22, 26, 30, 34, 38, 42, 46, 50, 54, 58, 62
1 0 0 0 0 0	m= 1, 3, 5, 7, ························, 57, 59, 61, 63

(3) PWM Operation

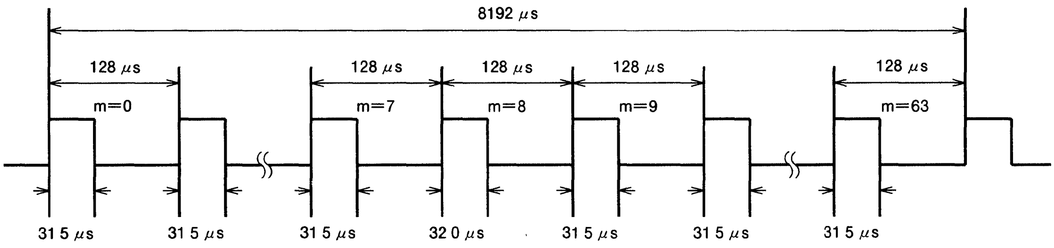
The timing of the 14-bit PWM function is shown in Fig. 23. The 14-bit PWM data is divided into the lower six bits and the upper eight bits in the PWM latch.

The upper eight bits of data determine how long an "H"-level signal is output during each sub-period. There are 64 sub-periods in each period, and each sub-period is 256X τ (128μs) long. The signal is "H" for a length equal to N times τ, where τ is the minimum resolution (500ns).

The contents of the lower six bits of data enable the lengthening of the high signal by τ (500ns). As shown in Fig. 20, the six bits of PWML determine which sub-cycles are lengthened.

As shown in Fig. 23, the leading edge of the pulse is lengthened. By changing the length of specific sub-periods instead of simply changing the "H" duration, an accurate waveform can be duplicated without the use of complex external filters.

For example, if the upper eight bits of the 14-bit data are 03_{16} and the lower six bits are 05_{16}, the length of the "H"-level output in sub-periods t_8, t_{24}, t_{32}, t_{40}, and t_{56} is 4 τ, and its length 3 τ in all other sub-periods.



Pulse width modulation register H : 00111111
Pulse width modulation register L : 000101
Sub-periods where "H" pulse width is 32 μs : m = 8, 24, 32, 40, 56
Sub-periods where "H" pulse width is 31.5 μs : m = all other values

Fig. 21 PWM timing

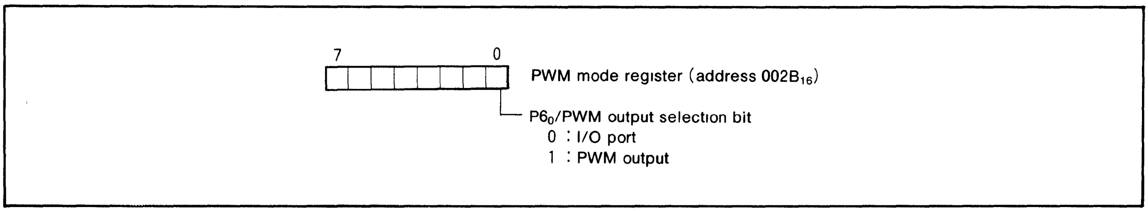


Fig. 22 Structure of PWM mode register

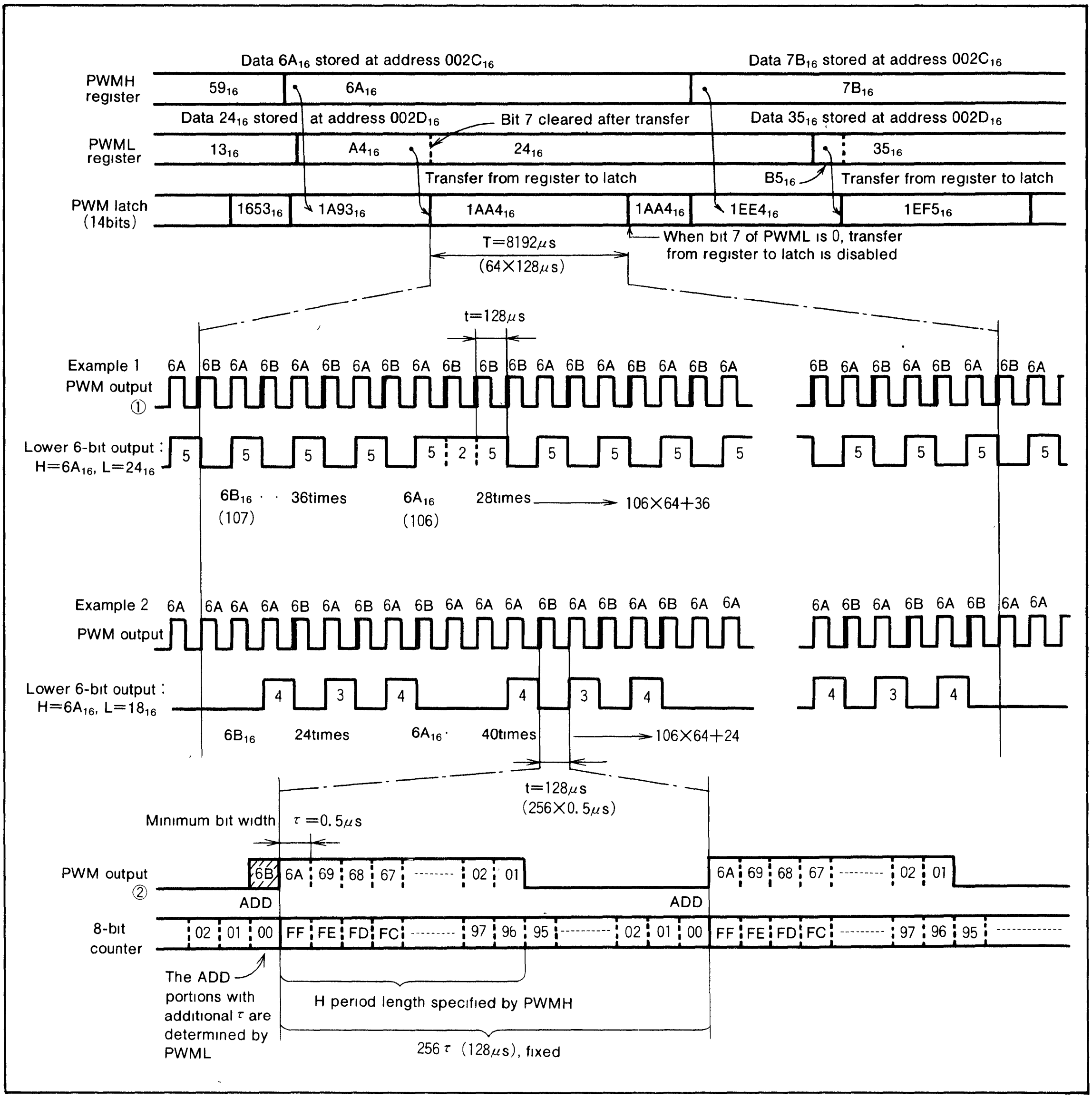


Fig. 23 14-bit PWM timing

COMPARATOR CIRCUIT

Comparator Configuration

The comparator circuit consists of a switch tree, ladder resistors, a comparator, a comparator control cricuit, a comparator register (address 0030_{16}), and an analog signal input pin ($P6_6$/AN). The analog signal input pin ($P6_6$/AN) also functions as an ordinary digital I/O port.

Comparator Register (CMP)

The comparator register is a 5-bit register of which bits 0 to 3 can be used to generate internal refernce voltage in steps of 1/16 V_{CC}, The result of the comparision between the analog input voltage and an internal reference voltage is stored in bit 4 of comparator register.

Comparator Operation

To activate the comparator, first set port $P6_6$ to input mode by setting the corresponding direction register (address $000D_{16}$) to "0"—this ensures that port $P6_6$/AN is used as an analog voltage input pin. Then write a digital value corresponding to the internal comparison voltage into bits 0 to 3 of the comparator register (address 0030_{16}). This write operation immediately activates the comparison. After 14 cycles of the system clock ϕ (the time required for the comparison), the comparison result is stored in bit 4 of the comparator.

If the analog input voltage is greater than the internal reference voltage, bit 4 is "1"; if it is less than the internal reference voltage, bit 4 is "0". To perform another omparison, the comparator must be written to again, even if the same internal reference voltage is to be used.

Table 5. Correspondence between bits 0 to 3 of the comparator register and internal reference voltage

Comparator register				Internal reference voltage
Bit 3	Bit 2	Bit 1	Bit 0	
0	0	0	0	$1/32V_{CC}$
0	0	0	1	$1/16V_{CC}+1/32V_{CC}$
0	0	1	0	$2/16V_{CC}+1/32V_{CC}$
0	0	1	1	$3/16V_{CC}+1/32V_{CC}$
0	1	0	0	$4/16V_{CC}+1/32V_{CC}$
0	1	0	1	$5/16V_{CC}+1/32V_{CC}$
0	1	1	0	$6/16V_{CC}+1/32V_{CC}$
0	1	1	1	$7/16V_{CC}+1/32V_{CC}$
1	0	0	0	$8/16V_{CC}+1/32V_{CC}$
1	0	0	1	$9/16V_{CC}+1/32V_{CC}$
1	0	1	0	$10/16V_{CC}+1/32V_{CC}$
1	0	1	1	$11/16V_{CC}+1/32V_{CC}$
1	1	0	0	$12/16V_{CC}+1/32V_{CC}$
1	1	0	1	$13/16V_{CC}+1/32V_{CC}$
1	1	1	0	$14/16V_{CC}+1/32V_{CC}$
1	1	1	1	$15/16V_{CC}+1/32V_{CC}$

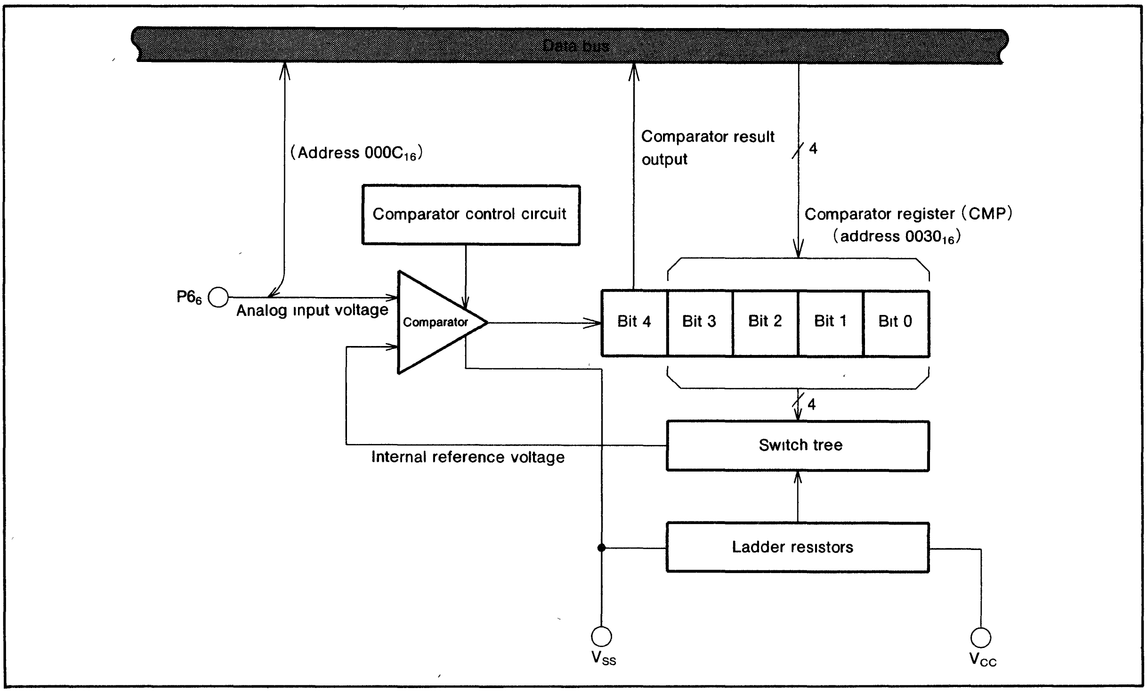


Fig. 24 Comparator circuit

FLD CONTROLLER

Microcomputers of the M3811x group have fluorescent display (FLD) drive and control circuits.

The FLD controller consists of the following components:

- 16 pins for segments
- 20 pins for digits
- FLDC mode register
- FLD data pointer
- FLD data pointer reload register
- Port P0 segment/digit switching register
- Port P2 digit/port switching register
- Key-scan blanking register
- 32-byte FLD automatic display RAM

Eight to sixteen pins can be used as segment pins and eight to sixteen pins can be used as digit pins.

Note that only 28 pins (maximum) can be used as segment and digit pins.

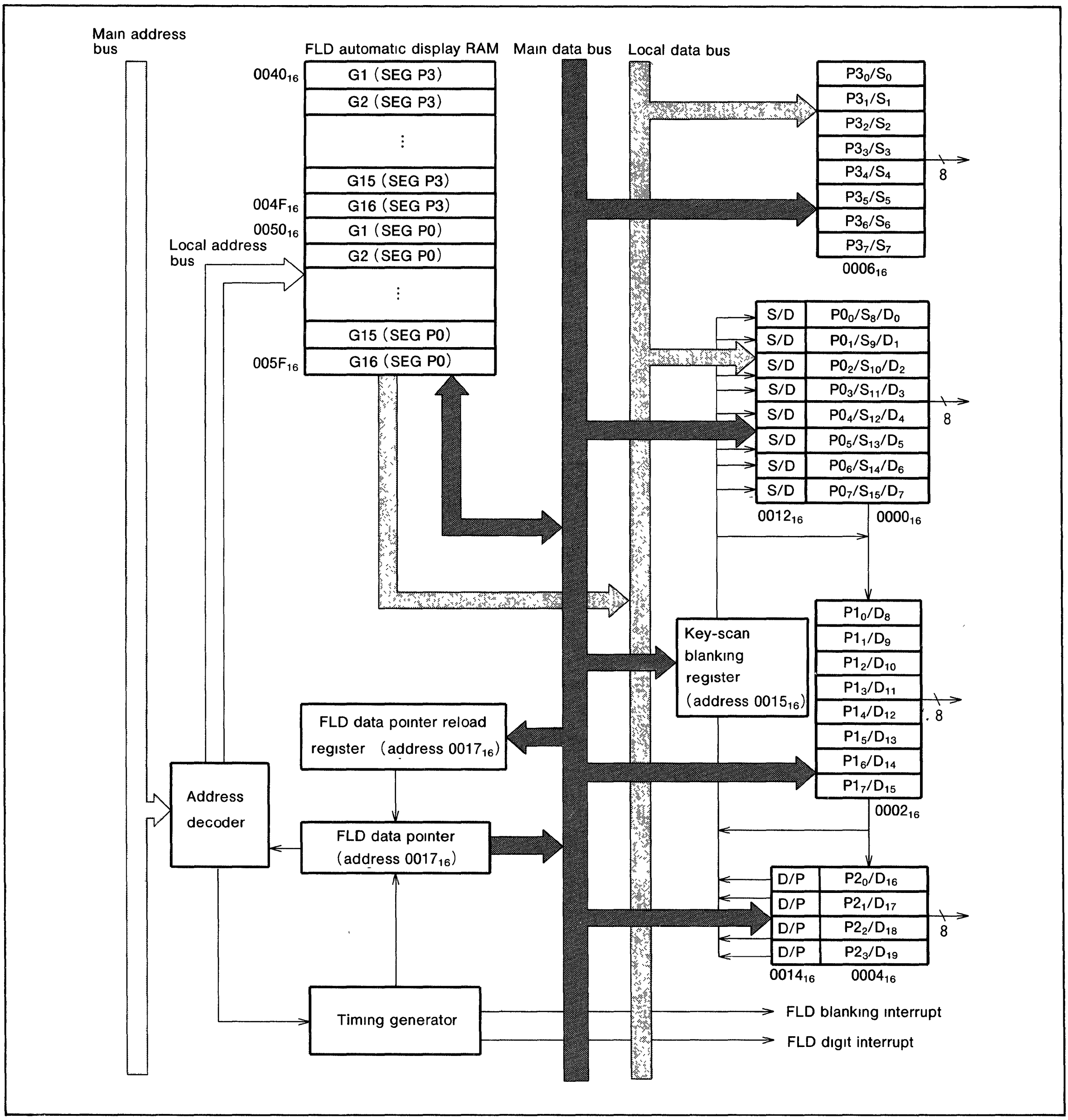


Fig. 25 FLD control circuit block diagram

FLDC Mode Register (FLDM)

The FLDC mode register (address 0016_{16}) is a seven bit control register which is used to control the FLD automatic display.

Key-scan Blanking Register (KSCN)

The key-scan blanking register (address 0015_{16}) is a two bit register which sets the blanking period T_{scan} between the last digit and the first digit of the next cycle.

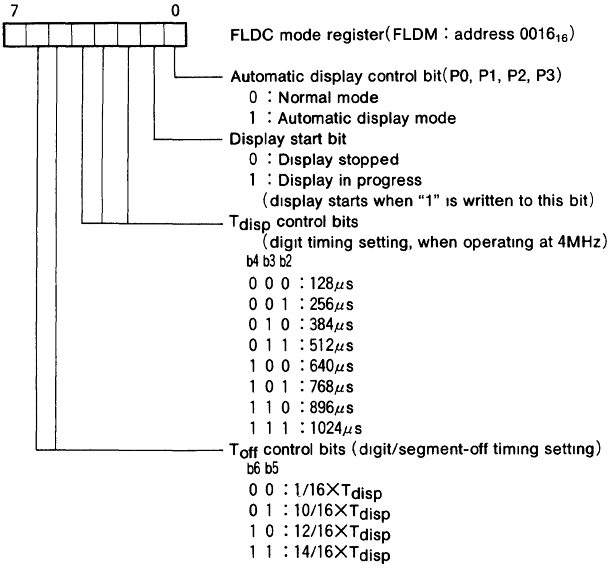


Fig. 26 Structure of FLDC mode register (FLDM)

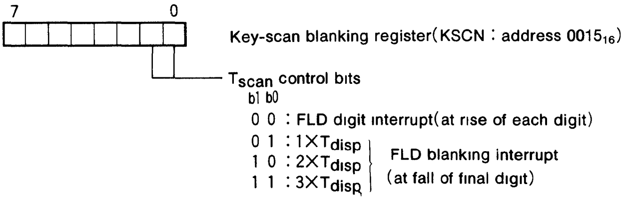


Fig. 27 Structure of key-scan blanking register (KSCN)

FLD Automatic Display Pins

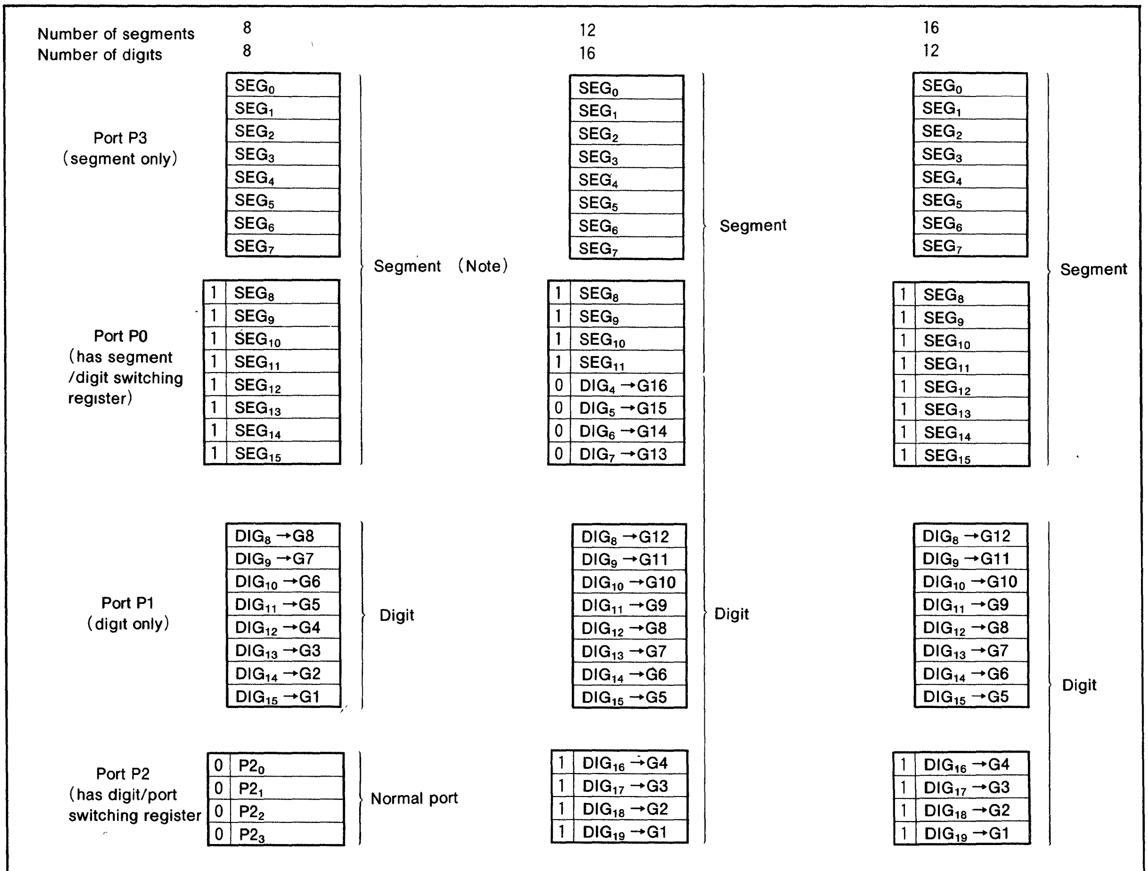
The FLD automatic display function of Ports P0, P1, $P2_0$-$P2_3$, and P3 is selected by setting the automatic display control bit of the FLDC mode register (address 0016_{16}) to "1".

When using the FLD automatic display mode, set the number of segments and digits for each port.

Table 6. Pins in FLD automatic display mode

Port Name	Automatic Display Pins	Setting Method
$P3_0$-$P3_7$	SEG_0-SEG_7	None (segment only)
$P0_0$-$P0_7$	SEG_8-SEG_{15} or DIG_0-DIG_7	The individual bits of the segment/digit switching register (address 0012_{16}) can be used to set each pin to segment ("1") or digit ("0") (Note)
$P1_0$-$P1_7$	DIG_8-DIG_{15}	None (digit only)
$P2_0$-$P2_3$	DIG_{16}-DIG_{19} or $P2_0$-$P2_3$	The individual bits of the digit/port switching register (address 0014_{16}) can be used to set each pin to digit ("1") or normal port output ("0") (Note)

Note. Always set digits in sequence



Note : Eight pins are used among the sixteen segment pins (SEG_0 to SEG_{15})

Fig. 28 Segment/digit setting example

FLD Automatic Display RAM

The FLD automatic display RAM area is the 32 bytes from address 0040_{16} to $005F_{16}$. The FLD automatic display RAM area can be used to store 2-byte data items for a maximum of 16 digits. Addresses 0040_{16} to $004F_{16}$ are used for P3 segment data, addresses 0050_{16} to $005F_{16}$ are used for P0 segment data.

- **FLD Data Pointer and FLD Data Pointer Reload Register**
  The FLD data pointer indicates the data address in the FLD automatic display RAM to be transferred to a segment, and the FLD data pointer reload register indicates the address of the first digit of segment P0.

Both the FLD data pointer and the FLD data pointer reload register are allocated to address 0017_{16} and are 5-bits wide. Data written to this address is written to the FLD data pointer reload register, data read from this address is read from the FLD data pointer.

The actual memory address is the value of the data pointer plus 40_{16}, 50_{16}.

The contents of the FLD data pointer indicate the start address of segment P0 at the start of automatic display. If segment P0 data is transferred to the segment, the FLD data pointer returns −16; if segment P3 data is transferred, it returns +15. After it reaches "00", the value in the FLD data pointer reload register is transferred to the FLD data pointer. In this way, two bytes of data for the P0 and P3 segments of one digit are transferred.

Bit / Address	7	6	5	4	3	2	1	0
0040_{16}	SEG_7	SEG_6	SEG_5	SEG_4	SEG_3	SEG_2	SEG_1	SEG_0
0041_{16}	SEG_7	SEG_6	SEG_5	SEG_4	SEG_3	SEG_2	SEG_1	SEG_0
0042_{16}	SEG_7	SEG_6	SEG_5	SEG_4	SEG_3	SEG_2	SEG_1	SEG_0
⋮	⋮			⋮				
$004D_{16}$	SEG_7	SEG_6	SEG_5	SEG_4	SEG_3	SEG_2	SEG_1	SEG_0
$004E_{16}$	SEG_7	SEG_6	SEG_5	SEG_4	SEG_3	SEG_2	SEG_1	SEG_0
$004F_{16}$	SEG_7	SEG_6	SEG_5	SEG_4	SEG_3	SEG_2	SEG_1	SEG_0
0050_{16}	SEG_{15}	SEG_{14}	SEG_{13}	SEG_{12}	SEG_{11}	SEG_{10}	SEG_9	SEG_8
0051_{16}	SEG_{15}	SEG_{14}	SEG_{13}	SEG_{12}	SEG_{11}	SEG_{10}	SEG_9	SEG_8
0052_{16}	SEG_{15}	SEG_{14}	SEG_{13}	SEG_{12}	SEG_{11}	SEG_{10}	SEG_9	SEG_8
⋮	⋮			⋮				
$005D_{16}$	SEG_{15}	SEG_{14}	SEG_{13}	SEG_{12}	SEG_{11}	SEG_{10}	SEG_9	SEG_8
$005E_{16}$	SEG_{15}	SEG_{14}	SEG_{13}	SEG_{12}	SEG_{11}	SEG_{10}	SEG_9	SEG_8
$005F_{16}$	SEG_{15}	SEG_{14}	SEG_{13}	SEG_{12}	SEG_{11}	SEG_{10}	SEG_9	SEG_8

Final digit (final data of segment P3)

Segment P3 data area

Final digit (final data of segment P0)

Segment P0 data area

Fig. 29 FLD automatic display RAM and bit allocation

- Data Setup

When data is stored in the FLD automatic display RAM, the end of segment P3 data is stored at address 0040$_{16}$, and the end of segment P0 data is stored at address 0050$_{16}$. The head of each of the segment P3 and P0 data is stored at an address that is the number of digits − 1 away from the corresponding address 0040$_{16}$, 0050$_{16}$.

Set the FLD data pointer reload register to the value given by the number of digits − 1. "1" is always written to bit 4. Note that "0" is always read from bit 4 during a read.

For 12 segments and 16 digits
(FLD data pointer reload register=15)

Bit Address	7	6	5	4	3	2	1	0
0040$_{16}$	▨	▨	▨	▨	▨	▨	▨	▨
0041$_{16}$	▨	▨	▨	▨	▨	▨	▨	▨
0042$_{16}$	▨	▨	▨	▨	▨	▨	▨	▨
0043$_{16}$	▨	▨	▨	▨	▨	▨	▨	▨
0044$_{16}$	▨	▨	▨	▨	▨	▨	▨	▨
0045$_{16}$	▨	▨	▨	▨	▨	▨	▨	▨
0046$_{16}$	▨	▨	▨	▨	▨	▨	▨	▨
0047$_{16}$	▨	▨	▨	▨	▨	▨	▨	▨
0048$_{16}$	▨	▨	▨	▨	▨	▨	▨	▨
0049$_{16}$	▨	▨	▨	▨	▨	▨	▨	▨
004A$_{16}$	▨	▨	▨	▨	▨	▨	▨	▨
004B$_{16}$	▨	▨	▨	▨	▨	▨	▨	▨
004C$_{16}$	▨	▨	▨	▨	▨	▨	▨	▨
004D$_{16}$	▨	▨	▨	▨	▨	▨	▨	▨
004E$_{16}$	▨	▨	▨	▨	▨	▨	▨	▨
004F$_{16}$	▨	▨	▨	▨	▨	▨	▨	▨
0050$_{16}$					▨	▨	▨	▨
0051$_{16}$					▨	▨	▨	▨
0052$_{16}$					▨	▨	▨	▨
0053$_{16}$					▨	▨	▨	▨
0054$_{16}$					▨	▨	▨	▨
0055$_{16}$					▨	▨	▨	▨
0056$_{16}$					▨	▨	▨	▨
0057$_{16}$					▨	▨	▨	▨
0058$_{16}$					▨	▨	▨	▨
0059$_{16}$					▨	▨	▨	▨
005A$_{16}$					▨	▨	▨	▨
005B$_{16}$					▨	▨	▨	▨
005C$_{16}$					▨	▨	▨	▨
005D$_{16}$					▨	▨	▨	▨
005E$_{16}$					▨	▨	▨	▨
005F$_{16}$					▨	▨	▨	▨

For 16 segments and 12 digits
(FLD data pointer reload register=11)

Bit Address	7	6	5	4	3	2	1	0
0040$_{16}$	▨	▨	▨	▨	▨	▨	▨	▨
0041$_{16}$	▨	▨	▨	▨	▨	▨	▨	▨
0042$_{16}$	▨	▨	▨	▨	▨	▨	▨	▨
0043$_{16}$	▨	▨	▨	▨	▨	▨	▨	▨
0044$_{16}$	▨	▨	▨	▨	▨	▨	▨	▨
0045$_{16}$	▨	▨	▨	▨	▨	▨	▨	▨
0046$_{16}$	▨	▨	▨	▨	▨	▨	▨	▨
0047$_{16}$	▨	▨	▨	▨	▨	▨	▨	▨
0048$_{16}$	▨	▨	▨	▨	▨	▨	▨	▨
0049$_{16}$	▨	▨	▨	▨	▨	▨	▨	▨
004A$_{16}$	▨	▨	▨	▨	▨	▨	▨	▨
004B$_{16}$	▨	▨	▨	▨	▨	▨	▨	▨
004C$_{16}$								
004D$_{16}$								
004E$_{16}$								
004F$_{16}$								
0050$_{16}$	▨	▨	▨	▨	▨	▨	▨	▨
0051$_{16}$	▨	▨	▨	▨	▨	▨	▨	▨
0052$_{16}$	▨	▨	▨	▨	▨	▨	▨	▨
0053$_{16}$	▨	▨	▨	▨	▨	▨	▨	▨
0054$_{16}$	▨	▨	▨	▨	▨	▨	▨	▨
0055$_{16}$	▨	▨	▨	▨	▨	▨	▨	▨
0056$_{16}$	▨	▨	▨	▨	▨	▨	▨	▨
0057$_{16}$	▨	▨	▨	▨	▨	▨	▨	▨
0058$_{16}$	▨	▨	▨	▨	▨	▨	▨	▨
0059$_{16}$	▨	▨	▨	▨	▨	▨	▨	▨
005A$_{16}$	▨	▨	▨	▨	▨	▨	▨	▨
005B$_{16}$	▨	▨	▨	▨	▨	▨	▨	▨
005C$_{16}$								
005D$_{16}$								
005E$_{16}$								
005F$_{16}$								

Note. ▨ Shaded areas are not used

Fig. 30 Example of using the FLD automatic display RAM.

- **Timing Setting**

The digit timing (T_{disp}) and digit/segment turn-off timing (T_{off}) can be set by the FLDC mode register (address 0016_{16}). The scan timing (T_{scan}) can be set by the key-scan blanking register (address 0015_{16}).

Note that flickering will occur if the repetition frequency ($1/(T_{disp}\times$number of digits$+T_{scan}))$ is an integral multiple of the digit timing T_{disp}.

- **FLD Start**

To perform FLD automatic display, you have to use the following registers.

- Port P0 segment/digit switching register
- Port P2 digit/port switching register
- Key-scan blanking register
- FLDC mode register
- FLD data pointer

Automatic display mode is activated by writing "1" to bit 0 of the FLDC mode register (address 0016_{16}), and the automatic display is started by writing "1" to bit 1.

During automatic display bit 1 always keeps "1", automatic display can be interrupted by writing "0" to bit 1.

If key-scan is to be performed by segment during the key-scan blanking period T_{scan},

1. Write "0" to bit 0 (automatic display control bit) of FLDC mode register (address 0016_{16}).
2. Set the port corresponding to the segment to the normal port.
3. After the key-scan is performed, write "1" (automatic display mode) to bit 0 of FLDC mode register (address 0016_{16}).

Note on performance of key-scan in the above 1 to 3 order.

1. Do not write "0" to bit 1 of FLDC mode register (address 0016_{16}).
2. Do not write "1" to the port corresponding to the digit.

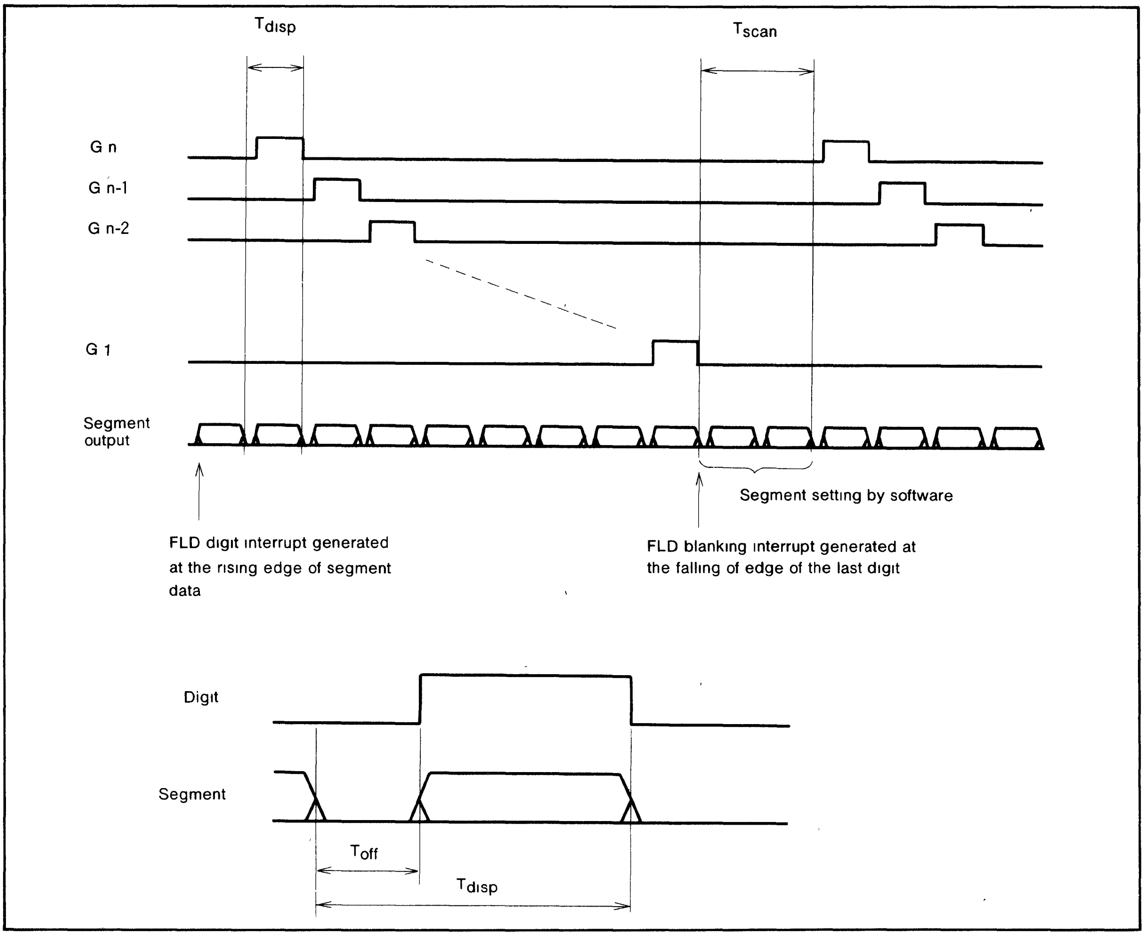
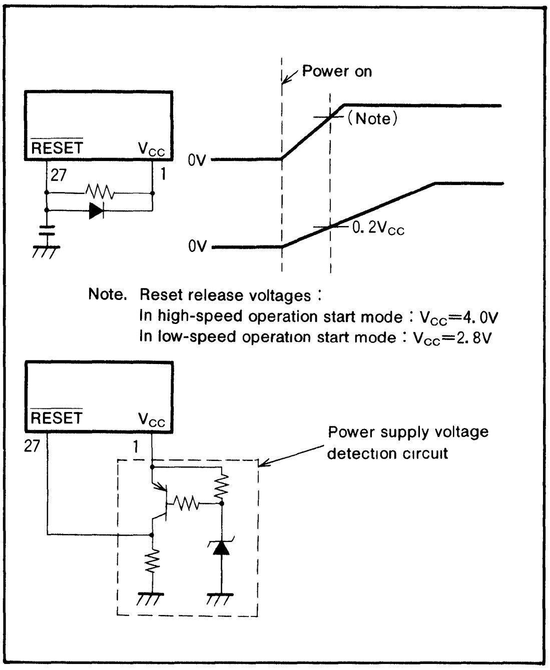


Fig. 31 FLDC timing

RESET CIRCUIT

After a reset, the microcomputer will start in high-speed operation start mode or low-speed operation start mode depending on a mask-programmable option.

- **High-Speed Operation Start Mode**
  In high-speed operation start mode, reset occurs if the $\overline{\text{RESET}}$ pin is held at an "L" level for at least 2μs then is returned to an "H" level (the power supply voltage should be between 4.0V and 5.5V). Both the X_{IN} and the X_{CIN} clocks begin oscillating. In order to give the X_{IN} clock time to stabilize, internal operation does not begin until after 13 X_{IN} clock cycles are complete. After the reset is completed, the program starts from the address contained in address $FFFD_{16}$ (upper byte) and address $FFFC_{16}$ (lower byte).



Note. Reset release voltages :
In high-speed operation start mode : V_{CC}=4. 0V
In low-speed operation start mode : V_{CC}=2. 8V

Fig. 32 Power-on reset circuit example

- **Low-Speed Operation Start Mode**
  In low-speed operation start mode, reset occurs if the $\overline{\text{RESET}}$ pin is held at an "L" level for at least 2μs then is returned to an "H" level (the power supply voltage should be between 2.8V and 5.5V). The X_{IN} clock does not begin oscillating. In order to give the X_{CIN} time to stabilize, timer 1 and timer 2 are connected together and 512 cycles of the $X_{CIN}/16$ are counted before internal operation begins. After the reset is completed, the program starts from the address contained in address $FFFD_{16}$ (upper byte) and address $FFFC_{16}$ (lower byte).
  If the X_{CIN} clock is stable, reset will complete after approximately 250ms (assuming $f(X_{CIN})$=32.768kHz).
  Immediately after a power-on, the stability of the clock circuit will determine the reset timing and will vary according to the characteristics of the oscillation circuit used.
- **Note on Use**
  Make sure that the reset input voltage is no more than 0.8V in high-speed operation start mode, or no more than 0.5V in low-speed operation start mode.

		Address	Register contents
(1)	Port P0 register	(0000$_{16}$)···	00$_{16}$
(2)	Port P1 register	(0002$_{16}$)···	00$_{16}$
(3)	Port P2 register	(0004$_{16}$)···	00$_{16}$
(4)	Port P2 direction register	(0005$_{16}$)···	00$_{16}$
(5)	Port P3 register	(0006$_{16}$)···	00$_{16}$
(6)	Port P4 register	(0008$_{16}$)···	00$_{16}$
(7)	Port P4 direction register	(0009$_{16}$)···	00$_{16}$
(8)	Port P5 register	(000A$_{16}$)···	00$_{16}$
(9)	Port P5 direction register	(000B$_{16}$)···	00$_{16}$
(10)	Port P6 register	(000C$_{16}$)···	00$_{16}$
(11)	Port P6 direction register	(000D$_{16}$)···	00$_{16}$
(12)	Port P0 segment/digit switching register	(0012$_{16}$)···	00$_{16}$
(13)	Port P2 digit/port switching register	(0014$_{16}$)···	00$_{16}$
(14)	Key-scan blanking register	(0015$_{16}$)···	00$_{16}$
(15)	FLDC mode register	(0016$_{16}$)···	00$_{16}$
(16)	Serial I/O1 control register	(0019$_{16}$)···	00$_{16}$
(17)	Serial I/O automatic transfer control register	(001A$_{16}$)···	00$_{16}$
(18)	Serial I/O automatic transfer interval register	(001C$_{16}$)···	00$_{16}$
(19)	Serial I/O2 control register	(001D$_{16}$)···	00$_{16}$
(20)	Timer 1 register	(0024$_{16}$)···	FF$_{16}$
(21)	Timer 2 register	(0025$_{16}$)···	01$_{16}$
(22)	Timer 3 register	(0026$_{16}$)···	FF$_{16}$
(23)	Timer 4 register	(0027$_{16}$)···	FF$_{16}$
(24)	Timer 12 mode register	(0028$_{16}$)···	00$_{16}$
(25)	Timer 34 mode register	(0029$_{16}$)···	00$_{16}$
(26)	PWM control register	(002B$_{16}$)···	00$_{16}$
(27)	Comparator register	(0030$_{16}$)···	00$_{16}$
(28)	High-breakdown-voltage port control register	(0038$_{16}$)···	00$_{16}$
(29)	Interrupt edge selection register	(003A$_{16}$)···	00$_{16}$
(30)	CPU mode register	(003B$_{16}$)···	∗ ∗ 1 0 0 0 0 0
(31)	Interrupt request register 1	(003C$_{16}$)···	00$_{16}$
(32)	Interrupt request register 2	(003D$_{16}$)···	00$_{16}$
(33)	Interrupt control register 1	(003E$_{16}$)···	00$_{16}$
(34)	Interrupt control register 2	(003F$_{16}$)···	00$_{16}$
(35)	Processor status register	(PS)···	X X X X X 1 X X
(36)	Program counter	(PC$_H$)···	Contents of address FFFD$_{16}$
		(PC$_L$)···	Contents of address FFFC$_{16}$

Note. ∗ : The initial values of bits 7 and 6 of the CPU mode register are determined by a mask option.
X : Underfined
The contents of all other registers and RAM are undefined after a reset, so programs must set their initial values

Fig. 33 Internal status at reset

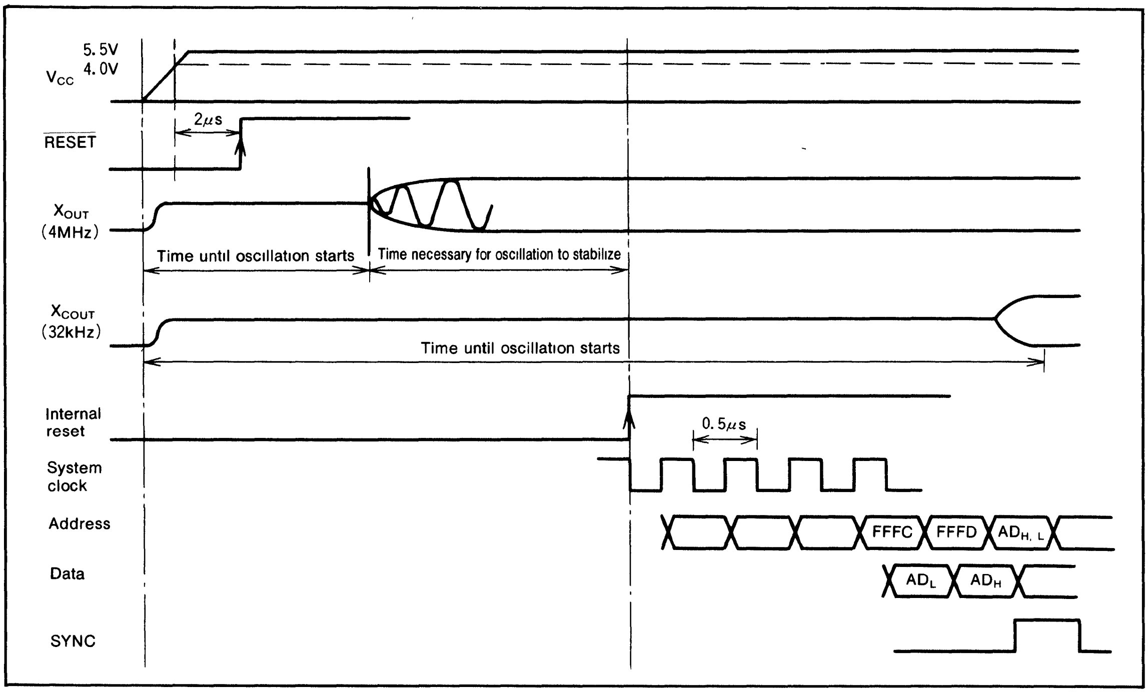


Fig. 34 Reset sequence in high-speed operation mode

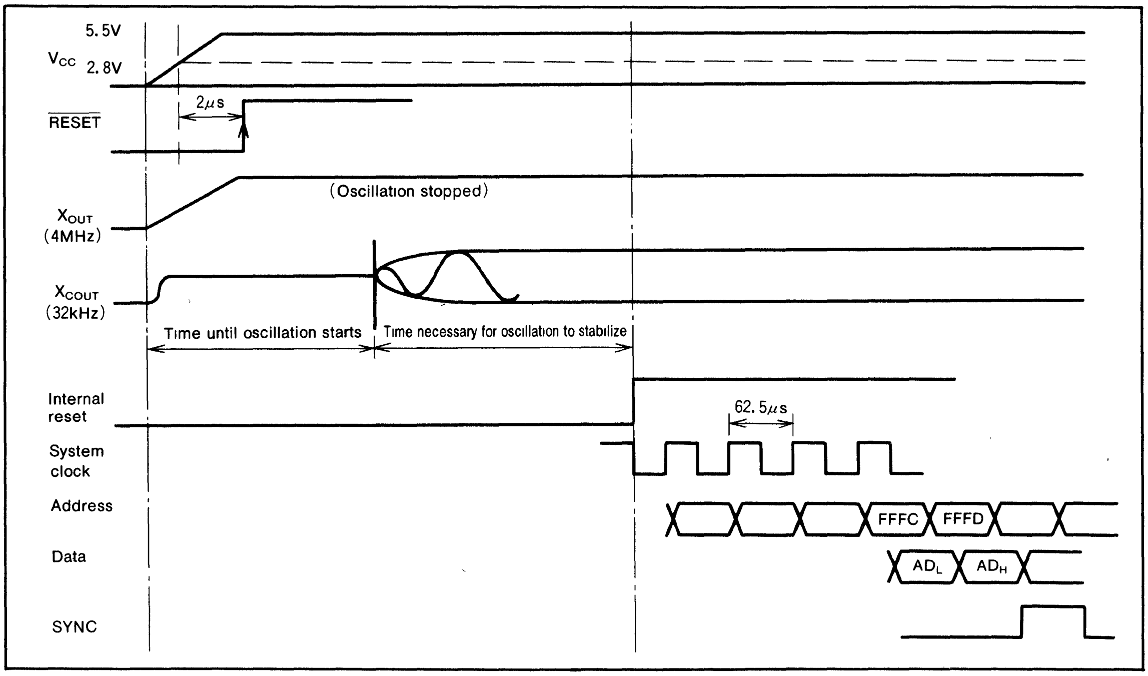


Fig. 35 Reset sequence in low-speed operation mode

CLOCK GENERATION CIRCUIT

When using an external clock signal, input the clock signal to the X_{IN} (X_{CIN}) pin and leave the X_{OUT} (X_{COUT}) pin open. If the X_{CIN} clock is not used, connect the X_{CIN} pin to V_{SS}, and leave the X_{COUT} pin open.

Either high-speed operation start mode or low-speed start mode can be selected by using a mask option.

- **High-Speed Operation Start Mode**
  After reset has completed, the internal clock ϕ is half the frequency of X_{IN}. Immediately after power-on, both the X_{IN} and X_{CIN} clock start oscillating. To set the internal clock ϕ to low-speed operation mode, set bit 7 of the CPU mode register (address $003B_{16}$) to "1".
- **Low-Speed Operation Start Mode**
  After reset has completed, the internal clock ϕ is half the frequency of X_{CIN}. Immediately after power-on, only the X_{CIN} clock starts oscillating. To set the internal clock ϕ to high-speed operation mode, first set bit 6 (CM_6) of the CPU mode register (address $003B_{16}$) to "0", the set bit 7 (CM_7) to "0". Note that the program must allow time for oscillation to stabilize.
- **Oscillation Control**

Stop Mode

If the STP instruction is executed, oscillation stops with the internal clock ϕ at an "H" level. Timer 1 is set to "FF_{16}" and timer 2 is set to "01_{16}".

Either X_{IN} or X_{CIN} divided by 16 is input to timer 1, and the output of timer 1 is connected to timer 2. The timer 1 and timer 2 interrupt enable bits must be set to disabled ("0"), so a program must set these bits before executing an STP instruction. Oscillation restarts at reset or when an external interrupt is received, but the internal clock ϕ is not supplied to the CPU until timer 2 overflows. This allows time for the clock circuit oscillation to stabilize.

Wait Mode

If the WIT instruction is executed, the internal clock ϕ stops at an "H" level but the oscillator itself does not stop. The internal clock restarts if a reset occurs or when an interrupt is received. Since the oscillator does not stop, normal operation can be started immediately after the clock is restarted.

Low-Speed Mode

If the internal clock is generated from the sub clock (X_{CIN}), a low power consumption operation can be entered by stopping only the main clock X_{IN}. To stop the main clock, set bit 6 (CM_6) of the CPU mode register ($003B_{16}$) to "1". When the main clock X_{IN} is restarted, the program must allow enough time to for oscillation to stabilize.

Note that in low-power-consumption mode the X_{CIN}-X_{COUT} drive performance can be reduced, allowing even lower power consumption (20μA with X_{CIN}= 32kHz). To reduce the X_{CIN}-X_{COUT} drive performance, clear bit 5 (CM_5) of the CPU mode register ($003B_{16}$) to "0". At reset or when an STP instruction is executed, this bit is set to "1" and strong drive is selected to help the oscillation to start.

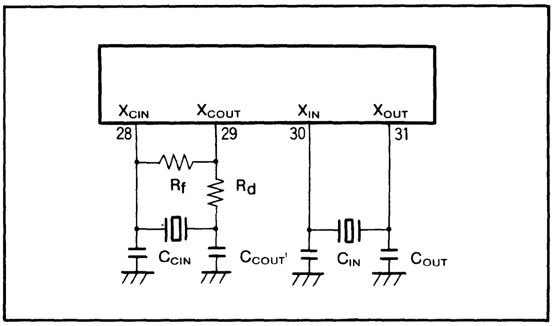


Fig. 36 Ceramic resonator circuit

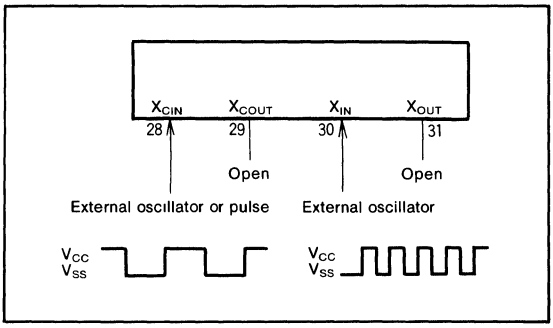
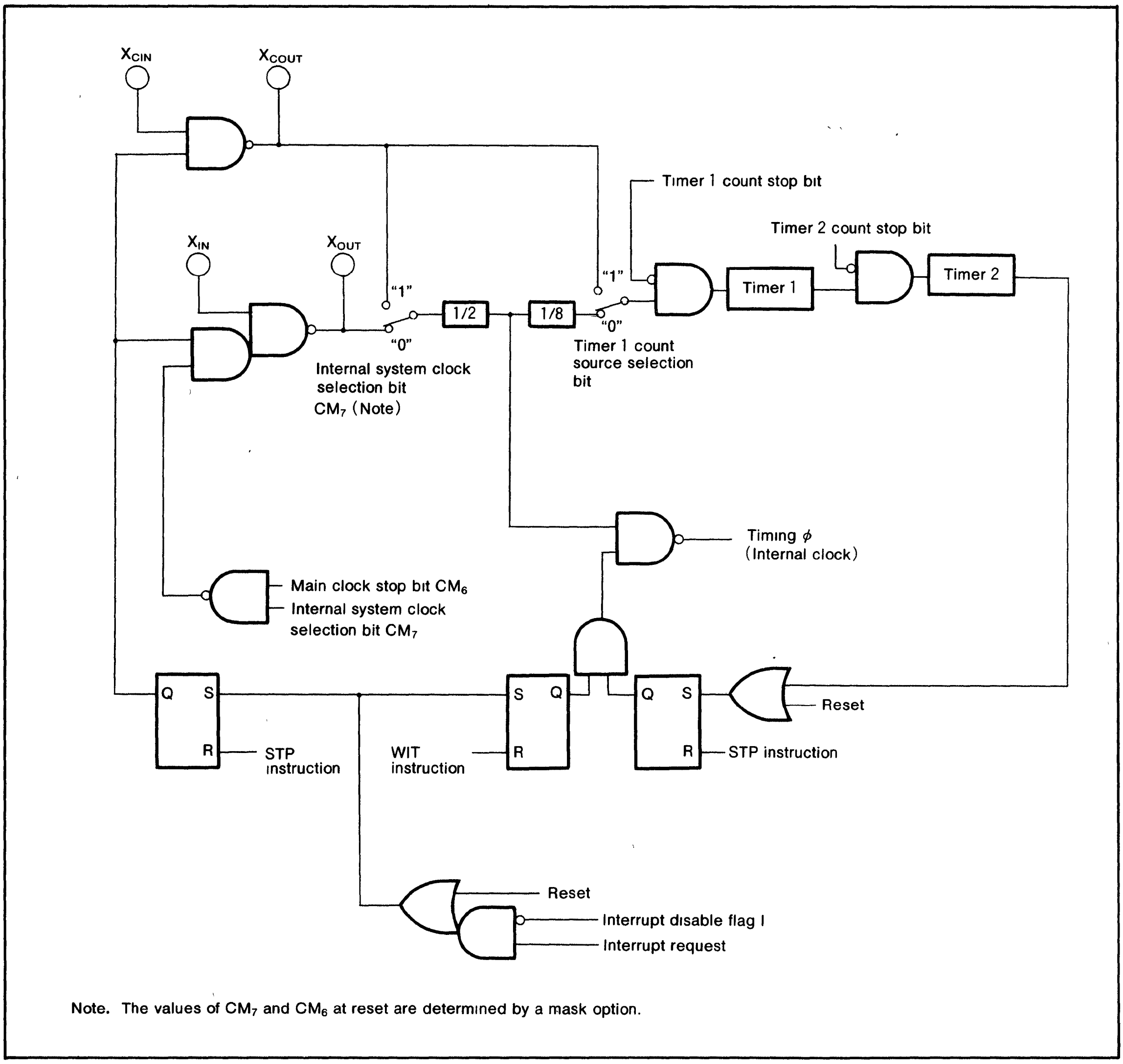
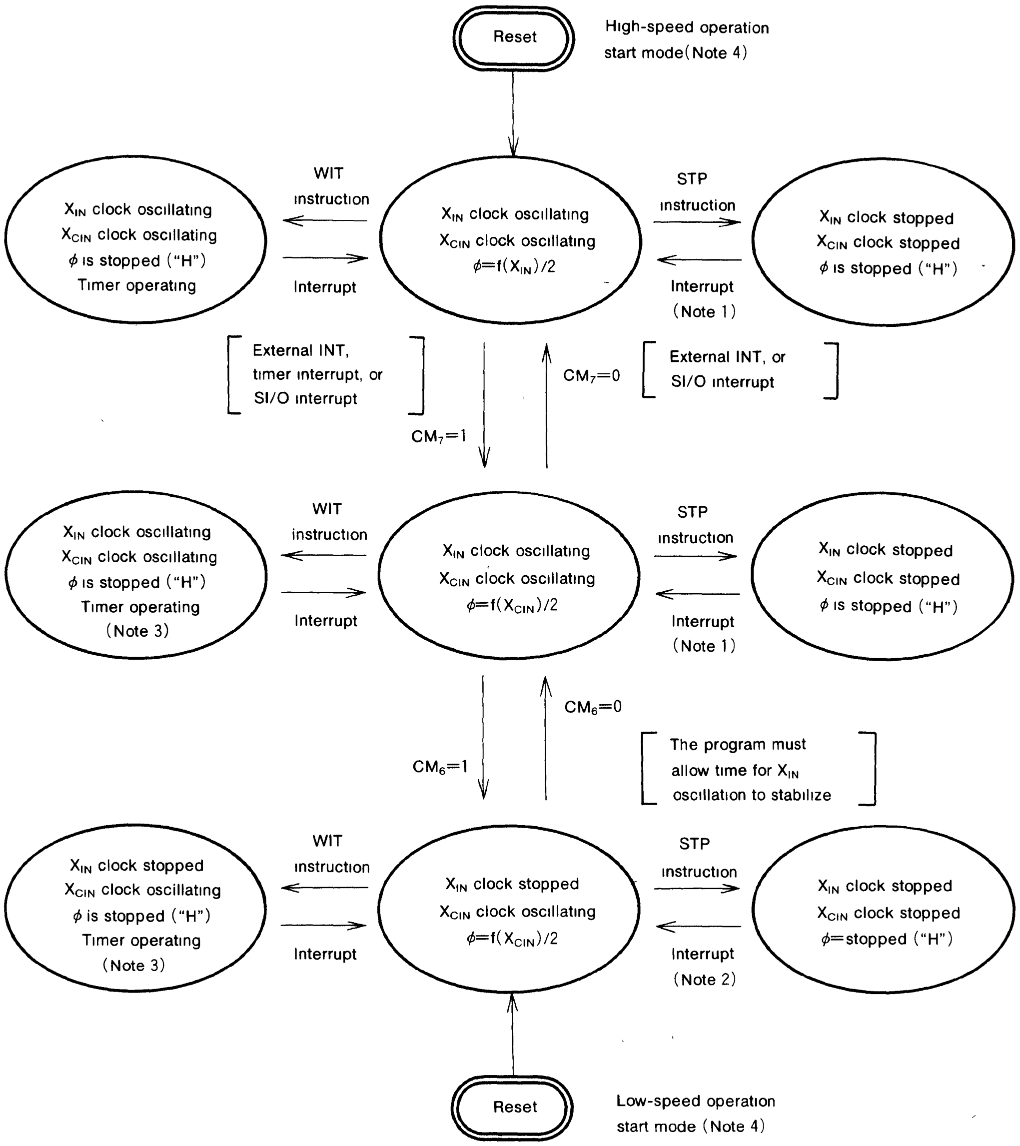


Fig. 37 External clock input circuit



Note. The values of CM_7 and CM_6 at reset are determined by a mask option.

Fig. 38 System clock generation circuit block diagram



The example assumes that 4MHz is being applied to the X_{IN} pin and 32kHz to the X_{CIN} pin

Note 1. When the STP state is ended, a delay of approximately 2ms is automatically generated by timer 1 and timer 2
2. The delay after the STP state ends is approximately 0. 25s
3. If the internal clock ϕ divided by 8 is used as the timer count source, the frequency of the count source is $f(X_{CIN})/16$
4. Specify this option when ordering a mask ROM version

Fig. 39 State transitions of system clock

NOTES ON PROGRAMMING

- **Processor Status Register**

  The contents of the processor status register (PS) after a reset are undefined, except for the interrupt disable flag (I) which is "1". Therefore, flags that affect program execution must be initialized after a reset. In particular, it is essential to initialize the T and D flags because of their effect on calculations.
- **Interrupts**

  The contents of the interrupt request bits do not change immediately after they have been written.

  After writing to an interrupt request register, execute at least one instruction before performing a BBC or BBS instruction.
- **Decimal Calculations**

  To calculate in decimal notation, set the decimal mode flag (D) to "1", then execute a ADC or SBC instruction. Only the ADC and SBC instruction yield proper decimal results. After executing an ADC or SBC instruction, execute at least one instruction before executing a SEC, CLC, or CLD instruction.

  In decimal mode, the values of the negative (N), overflow (V), and zero (Z) flags are invalid.

  The carry flag can be used to indicate whether a carry or borrow has occurred, but must be initialized before each calculation. Clear the carry flag before an ADC and set the flag before an SBC.
- **Timers**

  If a value n (between 0 and 255) is written to a timer latch, the frequency division ratio is 1/(n+1).
- **Multiplication and Division Instructions**

  The MUL and DIV instructions do not affect the T and D flags.

  The execution of these instructions does not change the contents of the processor status register.
- **Ports**

  The contents of the port direction registers cannot be read. Programs can not use the value of a direction register as an index, or bit-test a direction register (BBC or BBS), or perform a read-modify-write instruction such as ROR, CLB, or SEB. Use instructions such as LDM and STA to set the port direction registers.
- **Serial I/O**

  When using an external clock, input "H" to the external clock input pin and clear the serial I/O interrupt request bit before executing a serial I/O transfer.

  When using the internal clock, set the synchronization clock to internal clock, then clear the serial I/O interrupt request bit before executing a serial I/O transfer.
- **Instruction Execution Timing**

  The instruction execution time is obtained by multiplying the frequency of the internal clock ϕ by the number of cycles needed to execute an instruction.

  The number of cycles required to execute an instruction is shown in the list of machine instructions.

  The frequency of the internal clock ϕ is half of the X_{IN} or X_{CIN} frequency.

DATA REQUIRED FOR MASK ORDERS

The following are necessary when ordering a mask ROM production:

(1) Mask ROM Order Confirmation Form
(2) Mark Specification Form
(3) Data to be written to ROM, in EPROM form
(three identical copies)

If required, specify the following option on the Mask Confirmation Form:

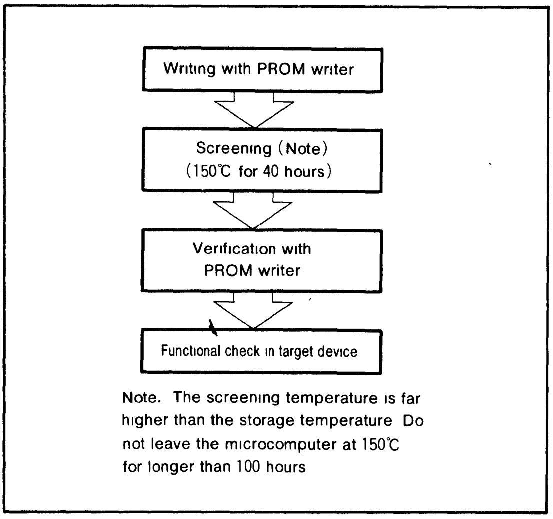
- Operation start mode switching option

ROM Writing Method

The built-in PROM of the blank one-time programmable version and built-in EPROM version can be read from and written to with an normal EPROM writer using a special write adapter.

Package	Name of Write Adapter
64P4B, 64S1B	PCA4738S-64
64P6N	PCA4738F-64
64D0	PCA4738L-64

The PROM of the blank one-time programmable version is not tested or screened after assembly. To ensure proper operation after writing, the procedure shown in Figure 40 is recommended to verify programming



Note. The screening temperature is far higher than the storage temperature Do not leave the microcomputer at 150℃ for longer than 100 hours

Fig. 40 Writing and testing of one-time programmable version

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	All voltages measured based on the V_{SS} pin Output transistors are isolated	−0.3 to 7.0	V
V_{EE}	Pull-down power supply voltage		V_{CC}−40 to V_{CC}+0.3	V
V_I	Input voltage $P2_4$-$P2_7$, $P4_1$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$		−0.3 to V_{CC}+0.3	V
V_I	Input voltage $P4_0$		−0.3 to V_{CC}+0.3	V
V_I	Input voltage $\overline{\text{RESET}}$, X_{IN}		−0.3 to V_{CC}+0.3	V
V_I	Input voltage X_{CIN}		−0.3 to V_{CC}+0.3	V
V_O	Output voltage $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_3$, $P3_0$-$P3_7$		V_{CC}−40 to V_{CC}+0.3	V
V_O	Output voltage $P2_4$-$P2_7$, $P4_1$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, X_{OUT}, X_{COUT}		−0.3 to V_{CC}+0.3	V
P_d	Power dissipation	T_a = 25℃	1000(Note 1)	mW
T_{opr}	Operating temperature		−10 to 85	℃
T_{stg}	Storage temperature		−40 to 125	℃

Note 1 : 600mW in case of the flat package

RECOMMENDED OPERATING CONDITIONS (V_{CC} = 4.0 to 5.5V, T_a = −10 to 85℃, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage	High-speed operation mode	4.0	5.0	5.5	V
		Low-speed operation mode	2.8	5.0	5.5	
V_{SS}	Supply voltage			0		V
V_{EE}	Pull-down power supply voltage		V_{CC}−38		V_{CC}	V
V_{IA}	Analog input voltage		0		V_{CC}	V
V_{IH}	"H" input voltage $P2_4$-$P2_7$		0.4V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage $P4_0$		0.75V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage $P4_1$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$		0.75V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage $\overline{\text{RESET}}$		0.8V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage X_{IN}, X_{CIN}		0.8V_{CC}		V_{CC}	V
V_{IL}	"L" input voltage $P2_4$-$P2_7$		0		0.16V_{CC}	V
V_{IL}	"L" input voltage $P4_0$		0		0.25V_{CC}	V
V_{IL}	"L" input voltage $P4_1$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$		0		0.25V_{CC}	V
V_{IL}	"L" input voltage $\overline{\text{RESET}}$		0		0.2V_{CC}	V
V_{IL}	"L" input voltage X_{IN}, X_{CIN}		0		0.2V_{CC}	V

RECOMMENDED OPERATING CONDITIONS (V_{CC}=4.0 to 5.5V, T_a=−10 to 85℃, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
$\Sigma I_{OH(peak)}$	"H" total peak output current $P0_0$-$P0_7$, $P1_0$-$P1_7$, (Note 1) $P2_0$-$P2_7$, $P3_0$-$P3_7$			−240	mA
$\Sigma I_{OH(peak)}$	"H" total peak output current $P4_1$-$P4_7$, $P6_0$-$P6_5$			−60	mA
$\Sigma I_{OL(peak)}$	"L" total peak output current $P2_4$-$P2_7$, $P4_1$-$P4_7$, $P5_0$-$P5_7$, $P6_1$-$P6_7$			100	mA
$\Sigma I_{OL(peak)}$	"L" total peak output current $P6_0$			3.0	mA
$\Sigma I_{OH(avg)}$	"H" total average output current $P0_0$-$P0_7$, $P1_0$-$P1_7$, (Note 1) $P2_4$-$P2_7$, $P3_0$-$P3_7$			−120	mA
$\Sigma I_{OH(avg)}$	"H" total average output current $P4_1$-$P4_7$, $P6_0$-$P6_7$			−30	mA
$\Sigma I_{OL(avg)}$	"L" total average output current $P2_4$-$P2_7$, $P4_1$-$P4_7$, $P5_0$-$P5_7$, $P6_1$-$P6_7$			50	mA
$\Sigma I_{OL(avg)}$	"L" total average output current $P6_0$			1.5	mA
$I_{OH(peak)}$	"H" peak output current $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_3$, $P3_0$-$P3_7$ (Note 2)			−40	mA
$I_{OH(peak)}$	"H" peak output current $P2_4$-$P2_7$, $P4_1$-$P4_7$, $P6_0$-$P6_7$			−10	mA
$I_{OL(peak)}$	"L" peak output current $P2_4$-$P2_7$, $P6_1$-$P6_7$			10	mA
$I_{OL(peak)}$	"L" peak output current $P4_1$-$P4_7$, $P5_0$-$P5_7$			10	mA
$I_{OL(peak)}$	"L" peak output current $P6_0$			3.0	mA
$I_{OH(avg)}$	"H" average output current $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_3$, (Note 3) $P3_0$-$P3_7$			−18	mA
$I_{OH(avg)}$	"H" average output current $P2_4$-$P2_7$, $P4_1$-$P4_7$, $P6_0$-$P6_7$			−5.0	mA
$I_{OL(avg)}$	"L" average output current $P2_4$-$P2_7$, $P6_1$-$P6_7$			5.0	mA
$I_{OL(avg)}$	"L" average output current $P4_1$-$P4_7$, $P5_0$-$P5_7$			5.0	mA
$I_{OL(avg)}$	"L" average output current $P6_0$			1.5	mA
f(CNTR)	Clock input frequency for timer 4 (duty cycle 50%)			250	kHz
$f(X_{IN})$	Main clock input oscillation frequency (Note 4)			4.2	MHz
$f(X_{CIN})$	Sub clock input oscillation frequency (Note 4, 5)		32.768	50	kHz

Note 1. The total output current is the sum of all the currents flowing through all the applicable ports The total average current is an average value measured over 100ms. The total peak current is the peak value of all the currents

2. The peak output current is the peak current flowing in each port.
3. The average output current in an average value measured over 100ms
4. When the oscillation frequency has a duty cycle of 50%
5. When using the microcomputer in low-speed operation mode, make sure that the sub clock's input frequency $f(X_{CIN})$ is less than $f(X_{IN})/3$

ELECTRICAL CHARACTERISTICS (V_{CC} = 4.0 to 5.5V, T_a = −10 to 85℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{OH}	"H" output voltage $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_3$, $P3_0$-$P3_7$	I_{OH}=−18mA	V_{CC}−2.0			V
V_{OH}	"H" output voltage $P2_4$-$P2_7$, $P4_1$-$P4_7$, $P6_0$-$P6_7$	I_{OH}=−10mA	V_{CC}−2.0			V
V_{OL}	"L" output voltage $P2_4$-$P2_7$, $P4_1$-$P4_7$, $P5_0$-$P5_7$, $P6_1$-$P6_7$	I_{OL}=10mA			2.0	V
V_{OL}	"L" output voltage $P6_0$	I_{OL}=1.5mA			0.5	V
$V_{T+}-V_{T-}$	Hysteresis $\overline{INT_0}$-$\overline{INT_2}$, S_{IN1}, S_{IN2}, S_{CLK1}, S_{CLK2}, CNTR	When using a non-port function		0.4		V
$V_{T+}-V_{T-}$	Hysteresis $\overline{RESET}$, X_{IN}	$\overline{RESET}$: V_{CC}=2.8V to 5.5V		0.5		V
$V_{T+}-V_{T-}$	Hysteresis X_{CIN}			0.5		V
I_{IH}	"H" input current $P2_4$-$P2_7$, $P4_1$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$	V_I=V_{CC}			5.0	μA
I_{IH}	"H" input current $P4_0$	V_I=V_{CC}			5.0	μA
I_{IH}	"H" input current $\overline{RESET}$, X_{CIN}	V_I=V_{CC}			5.0	μA
I_{IH}	"H" input current X_{IN}	V_I=V_{CC}		4.0		μA
I_{IL}	"L" input current $P2_4$-$P2_7$, $P4_1$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$	V_I=V_{SS}			−5.0	μA
I_{IL}	"L" input current $P4_0$	V_I=V_{SS}			−5.0	μA
I_{IL}	"L" input current $\overline{RESET}$, X_{CIN}	V_I=V_{SS}			−5.0	μA
I_{IL}	"L" input current X_{IN}	V_I=V_{SS}		−4.0		μA
I_{LOAD}	Output load current $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_3$, $P3_0$-$P3_7$	V_{EE}=V_{CC}−36V, V_{OL}=V_{CC}, With output transistors off	150	500	900	μA
I_{LEAK}	Output leakage current $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_3$, $P3_0$-$P3_7$	V_{EE}=V_{CC}−38V, V_{OL}=V_{CC}−38V, With output transistors off (Except for reset)			−10	μA
V_{RAM}	RAM hold voltage	When clock is stopped	2.0		5.5	V
I_{CC}	Power supply current	In high-speed operation mode f(X_{IN})=4MHz f(X_{CIN})=32kHz Output transistors off Comparator operating		5	10	mA
		In high-speed operation mode f(X_{IN})=4MHz (in WIT state) f(X_{CIN})=32kHz Output transistors off Comparator stopped		1		mA
		In low-speed operation mode f(X_{IN})= stopped, f(X_{CIN})=32kHz Low-power dissipation mode set (CM_5=0) Output transistors off		60	200	μA
		In low-speed operation mode f(X_{IN})= stopped f(X_{CIN})=32kHz (in WIT state) Low-power dissipation mode set (CM_5=0) Output transistors off		20	40	μA
		All oscillation stopped (in STP state) Output transistors off T_a=25℃		0.1	1.0	μA
		T_a=85℃			10	

COMPARATOR CHARACTERISTICS

(V_{CC}=4.0 to 5.5V, V_{SS}=0V, T_a=−10 to 85℃, high-speed operation mode, $f(X_{IN})$=500kHz to 4MHz unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
—	Resolution				4	Bits
—	Absolute accuracy				1/2	LSB
T_{CONV}	Conversion time				7	μs
I_{IA}	Analog port input current				5.0	μA
R_{LADDER}	Ladder resistor			30		kΩ

TIMING REQUIREMENTS

(V_{CC}=4.0 to 5.5V, V_{SS}=0V, T_a=−10 to 85℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{W(\overline{RESET})}$	Reset input "L" pulse width		2			μs
$t_{C(X_{IN})}$	Main clock input cycle time (X_{IN} input)		238			ns
$t_{WH(X_{IN})}$	Main clock input "H" pulse width		60			ns
$t_{WL(X_{IN})}$	Main clock input "L" pulse width		60			ns
$t_{C(X_{CIN})}$	Sub clock input cycle time (X_{CIN} input)		2.0			ms
$t_{WH(X_{CIN})}$	Sub clock input "H" pulse width		0.5			ms
$t_{WL(X_{CIN})}$	Sub clock input "L" pulse width		0.5			ms
$t_{C(CNTR)}$	CNTR input cycle time		4			μs
$t_{WH(CNTR)}$	CNTR input "H" pulse width		1.6			μs
$t_{WL(CNTR)}$	CNTR input "L" pulse width		1.6			μs
$t_{WH(INT)}$	INT_0-INT_2 input "H" pulse width		80			ns
$t_{WL(INT)}$	INT_0-INT_2 input "L" pulse width		80			ns
$t_{C(S_{CLK})}$	Serial clock input cycle time		1			μs
$t_{WH(S_{CLK})}$	Serial clock input clock "H" pulse width		400			ns
$t_{WL(S_{CLK})}$	Serial clock input clock "L" pulse width		400			ns
$t_{SU(S_{CLK}-S_{IN})}$	Serial input setup time		200			ns
$t_{h(S_{CLK}-S_{IN})}$	Serial input hold time		200			ns

SWITCHING CHARACTERISTICS

(V_{CC}=4.0 to 5.5V, V_{SS}=0V, T_a=−10 to 85℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{WH(S_{CLK})}$	Serial clock output "H" pulse width	C_L=100pF, R_L=1kΩ	$t_C/2-160$			ns
$t_{WL(S_{CLK})}$	Serial clock output "L" pulse width	C_L=100pF, R_L=1kΩ	$t_C/2-160$			ns
$t_{d(S_{CLK}-S_{OUT})}$	Serial output delay time				$0.2t_C$	ns
$t_{V(S_{CLK}-S_{OUT})}$	Serial output hold time		0			ns
$t_{f(S_{CLK})}$	Serial clock output fall time	C_L=100pF, R_L=1kΩ			40	ns
$t_{r(Pch-strg)}$	P-channel high-breakdown voltage output rise time (Note 1)	C_L=100pF, V_{EE}=V_{CC}−36V		55		ns
$t_{r(Pch-weak)}$	P-channel high-breakdown voltage output rise time (Note 2)	C_L=100pF, V_{EE}=V_{CC}−36V		1.8		μs

Note 1. When bit 0 of the high-breakdown voltage port control register (address 0038_{16}) is at "0"
2. When bit 0 of the high-breakdown voltage port control register (address 0038_{16}) is at "1"

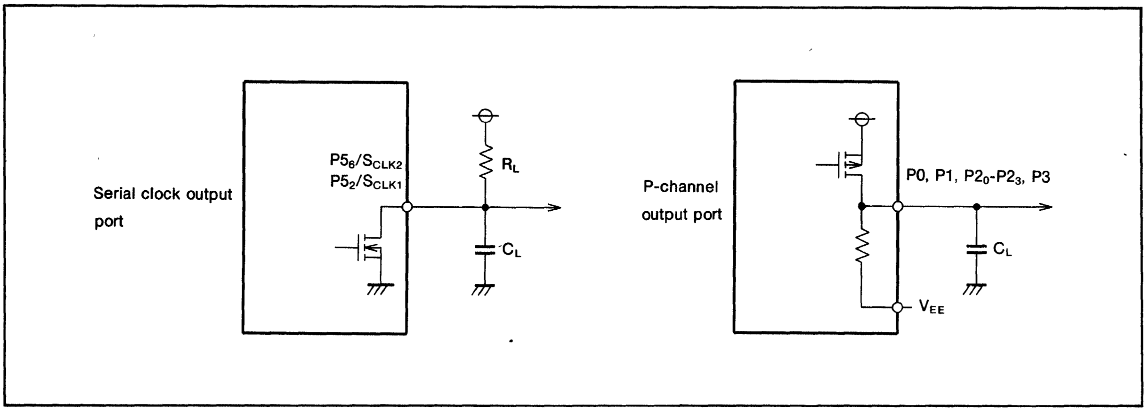
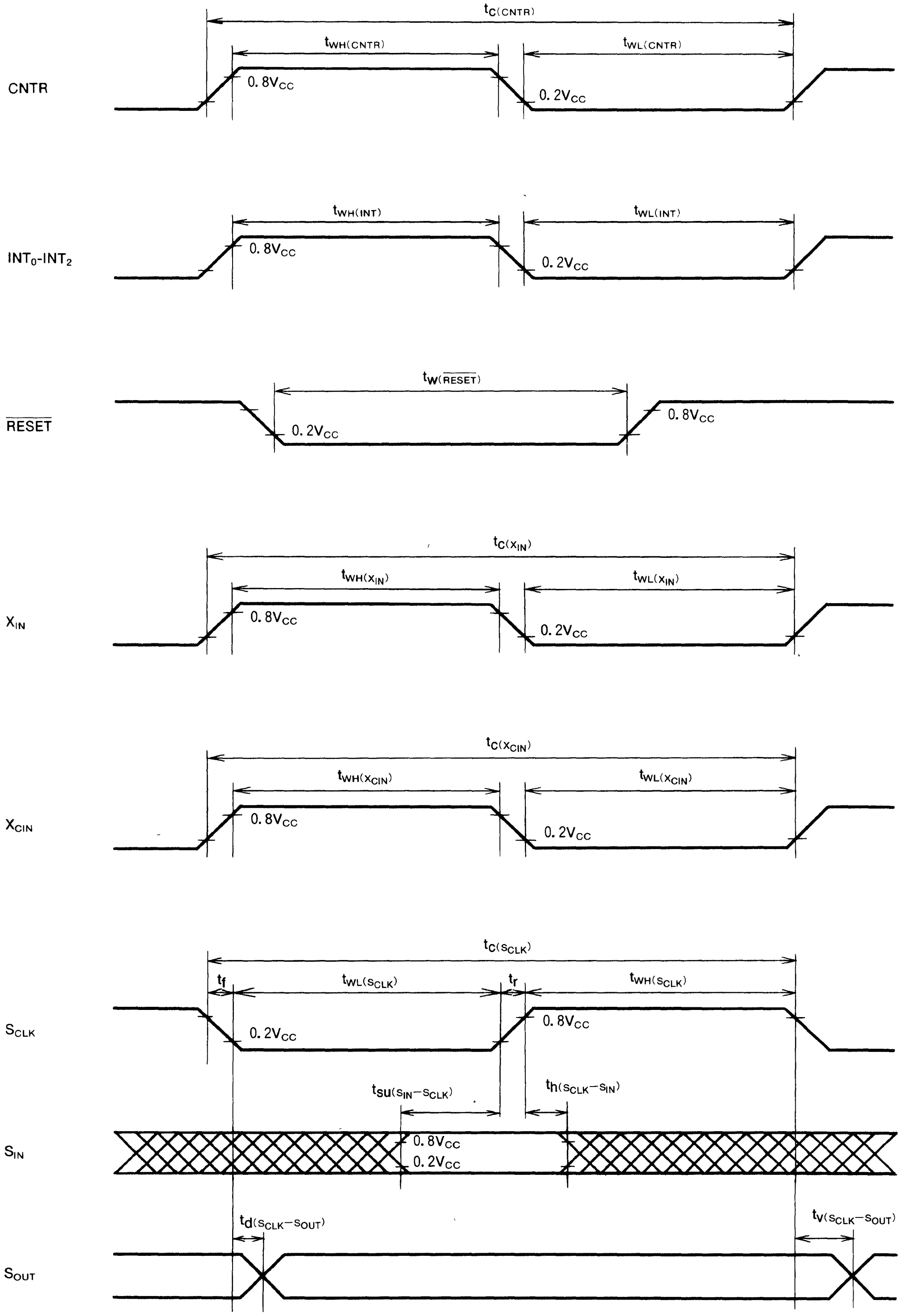


Fig. 41 Output switching characteristics measurement circuit

Timing Chart



MITSUBISHI MICROCOMPUTERS

M3817x Group

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

DESCRIPTION

The M3817x group is made up of 8-bit microcomputers based on the MELPS 740 core.

The M3817x group is designed mainly for VCR timer/function control, and include six 8-bit timers, a fluorescent display automatic display circuit, a PWM function, and an 8-channel A-D converter.

The various microcomputers in the M3817x group include variations of internal memory size and packaging. For details, see the section on part numbering.

For details on availability of microcomputers in the M3817x group, see the section on group expansion.

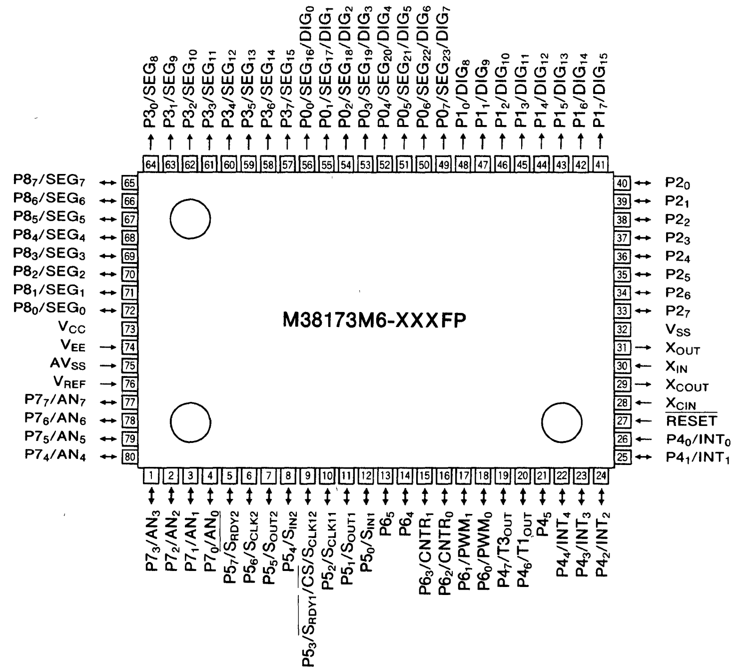
FEATURES

- Basic machine-language instructions ······ 71
- Instruction execution time ······ 0.63μs
  (shortest instruction at 6.3MHz oscillation frequency)
- Memory size
  ROM ······ 4K to 32K bytes
  RAM ······ 192 to 1024 bytes
- Programmable input/output ports ······ 45
- High-breakdown-voltage output ports ······ 32
- Interrupts ······ 18 sources, 15 vectors
- Timers ······ 8-bit×6
- Serial I/O ······ Clock-synchronized 8-bit×2
  (Serial I/O1 has an automatic data transfer function)
- PWM output circuit ······ 14-bit×1
  8-bit×1 (also functions as timer 6)
- A-D converter ······ 8-bit×8 channels
- Fluorescent display function
  Segments ······ 8 to 24
  Digits ······ 4 to 16
- 2 Clock generation circuit
  Clock (X_{IN}-X_{OUT}) ······ Internal feedback amplifier
  Sub clock (X_{CIN}-X_{COUT}) ······ Internal amplifier without feedback
- Supply voltage ······ 4.0 to 5.5V
- Low power dissipation
  In high-speed operation ······ 38mW
  (at 6.3MHz oscillation frequency)
  In low-speed operation ······ 300μW
  (at 32kHz oscillation frequency)
- Operating temperature range ······ −10 to 85℃

APPLICATIONS

VCRs, tuners, musical instruments, office automation, etc.

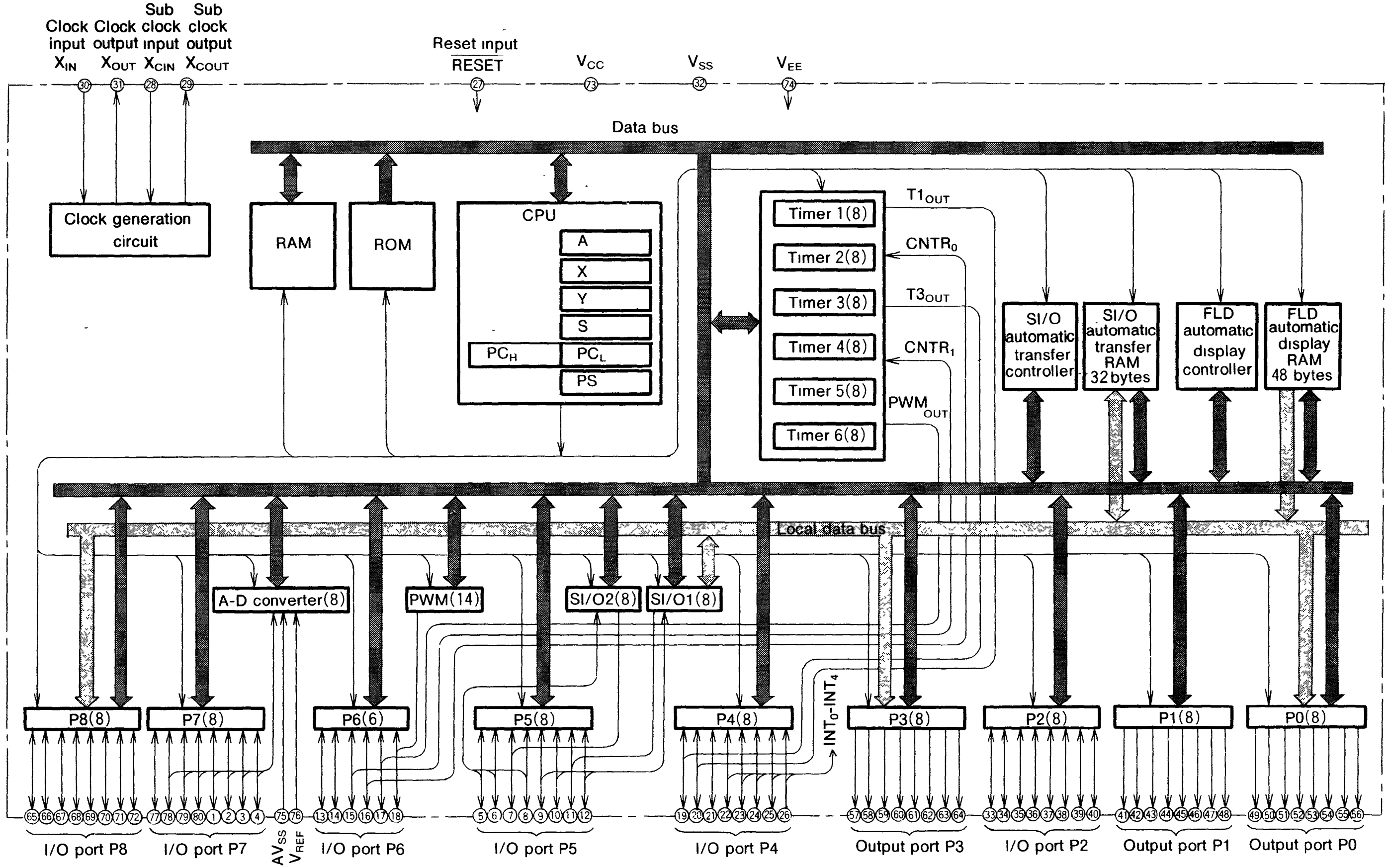
PIN CONFIGURATION (TOP VIEW)



Package type : 80P6N

80-pin plastic molded QFP

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTION

Pin	Name	Function	
			Alternate Function
V_{CC}, V_{SS}	Power supply	Power supply inputs 4 0 to 5 5V to V_{CC}, and 0V to V_{SS}	
V_{EE}	Pull-down power input	Applies voltage supplied to pull-down resistors of ports P0, P1, P2 and P3	
V_{REF}	Analog reference voltage	Reference voltage input pin for A-D converter	
AV_{SS}	Analog power supply	GND input pin for A-D converter Keep at the same potential as V_{SS}	
$\overline{RESET}$	Reset input	To reset the microcomputer, this pin should be kept at an "L" level for more than 2μs under high-speed operating conditions In low-speed operation start mode, internal reset is not released until the X_{CIN}-X_{COUT} clock has had time to stabilize	
X_{IN}	Clock input	Input and output signals for the internal clock generation circuit It consist of internal feedback amplifier Connect a ceramic resonator or quartz crystal between the X_{IN} and X_{OUT} pins to set the oscillation frequency If an external clock is used, connect the clock source to the X_{IN} pin and leave the X_{OUT} pin open This clock is used as system clock	
X_{OUT}	Clock output		
X_{CIN}	Sub clock input	Input and output signals for the internal sub clock generation circuit It consist of internal amplifier without feedback Connect a ceramic resonator or quartz crystal and external feedback resistor between the X_{CIN} and X_{COUT} pins If an external clock is used, connect the clock source to the X_{CIN} pin and leave the X_{COUT} pin open This clock can also be used as the system clock	
X_{COUT}	Sub clock output		
$P0_0/SEG_{16}/DIG_0$-$P0_7/SEG_{23}/DIG_7$	Output port P0	An 8-bit output port The output structure is high-breakdown-voltage P-channel open drain with internal pull-down resistors connected between the output and the V_{EE} pin Are "L" at reset	FLD automatic display pins
$P1_0/DIG_8$-$P1_7/DIG_{15}$	Output port P1	An 8-bit output port with the same function as port P0	FLD automatic display pins
$P2_0$-$P2_7$	I/O port P2	An 8-bit CMOS I/O port An I/O direction register allows each pin to be individually programmed as either input or output At reset this port is set to input mode The input levels are TTL compatible	
$P3_0/SEG_8$-$P3_7/SEG_{15}$	Output port P3	An 8-bit output port with the same function as port P0	FLD automatic display pins
$P4_0/INT_0$	Input port $P4_0$	A 1-bit CMOS input pin	External interrupt input pin
$P4_1/INT_1$-$P4_4/INT_4$	I/O port P4	A 7-bit CMOS I/O port with the same function as port P2, with CMOS compatible input levels	External interrupt input pins
$P4_5$			
$P4_6/T1_{OUT}$, $P4_7/T3_{OUT}$			Timer output pin
$P5_0/S_{IN1}$, $P5_1/S_{OUT1}$, $P5_2/S_{CLK11}$, $P5_3/\overline{S_{RDY1}}/\overline{CS}/S_{CLK12}$	I/O port P5	An 8-bit I/O port with the same function as port P2 The output structure of this port is N-channel open drain, and the input levels are CMOS compatible Keep the input voltage of this port between 0V and V_{CC}	Serial I/O1 I/O pins
$P5_4/S_{IN2}$, $P5_5/S_{OUT2}$, $P5_6/S_{CLK2}$, $P5_7/\overline{S_{RDY2}}$			Serial I/O2 I/O pins

MITSUBISHI
ELECTRIC

PIN DESCRIPTION

Pin	Name	Function	
			Alternate Function
$P6_0/PWM_0$	I/O port P6	A 6-bit CMOS I/O port with the same function as port P2, with CMOS compatible input levels.	14-bit PWM output pin
$P6_1/PWM_1$			8-bit PWM output pin
$P6_2/CNTR_0$, $P6_3/CNTR_1$			Event counter input pins
$P6_4$, $P6_5$			
$P7_0/AN_0$- $P7_7/AN_7$	I/O port P7	An 8-bit CMOS I/O port with the same function as port P2, with CMOS compatible input levels.	A-D converter input pins
$P8_0/SEG_0$- $P8_7/SEG_7$	I/O port P8	An 8-bit I/O port with the same function as port P2. The output structure of this port is P-channel open drain, and the input levels are CMOS compatible. Please note that this port does not have internal pull-down resistors.	FLD automatic display pins

PART NUMBERING

Product name M3817 0 M X - XXX FP

Package type
FP : 80P6N package
FS : 80D0 package

ROM number
Omitted in some types

ROM/PROM size
1 : 4096 bytes
2 : 8192 bytes
3 : 12288 bytes
4 : 16384 bytes
5 : 20480 bytes
6 : 24576 bytes
7 : 28672 bytes
8 : 32768 bytes

The first 128 bytes and the last two bytes of ROM are reserved areas; they cannot be used

Memory type
M : Mask ROM version
E : EPROM or one-time programmable version

RAM size
0 192 bytes
1 : 256 bytes
2 384 bytes
3 : 512 bytes
4 640 bytes
5 768 bytes
6 : 896 bytes
7 1024 bytes

GROUP EXPANSION

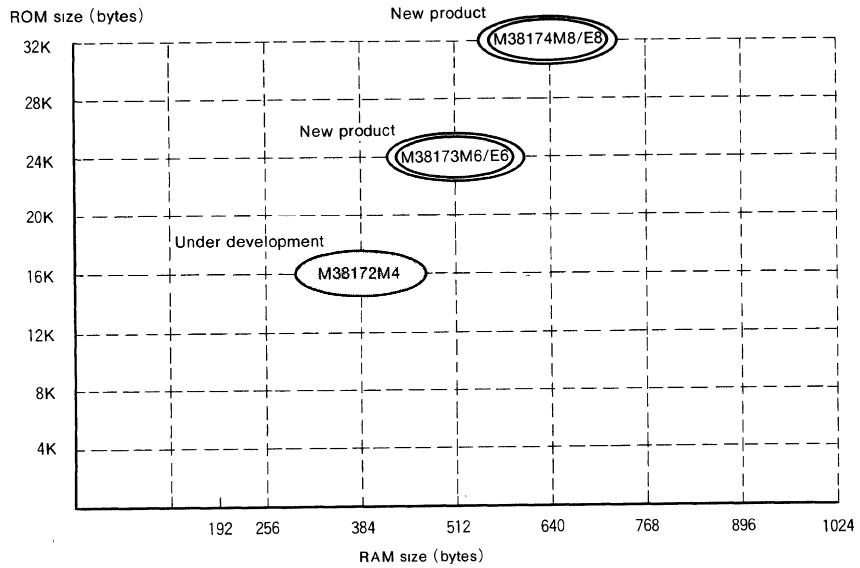
Mitsubishi plans to expand the M3817x group as follows:

(1) Support for mask ROM, one-time programmable, and EPROM versions

(2) ROM/PROM size ···························· 16K to 32K bytes
RAM size ···································· 384 to 640 bytes

(3) Packages
80P6N ··································· Plastic molded QFP
80D0 ······························ Window type ceramic LCC

Memory Expansion Plan



The development schedule and other details of products under development may be revised without notice

Currently supported products are listed below. **As of March 1992**

Product name	(P) ROM size (bytes)	RAM size (bytes)	Package	Remarks
M38173M6-XXXFP	24K	512	80P6N	Mask ROM version
M38173E6-XXXFP				One-time programmable version
M38173E6FP				One-time programmable version (blank)
M38173E6FS			80D0	EPROM version
M38174M8-XXXFP	32K	640	80P6N	Mask ROM version
M38174E8-XXXFP				One-time programmable version
M38174E8FP				One-time programmable version (blank)
M38174E8HXXXFP				One-time programmable version (High-speed operation start version)
M38174E8HFP				One-time programmable version (blank) (High-speed operation start version)
M38174E8FS			80D0	EPROM version

FUNCTIONAL DESCRIPTION
CENTRAL PROCESSING UNIT (CPU)

Microcomputers of the M3817x group use the standard MELPS 740 instruction set. Refer to the table of MELPS 740 addressing modes and machine instructions or the MELPS 740 Software Manual for details on the instruction set.

Machine-resident MELPS 740 instructions are as follows:

The FST and SLW instructions are not available for use.
The STP, WIT, MUL and DIV instructions can be used.

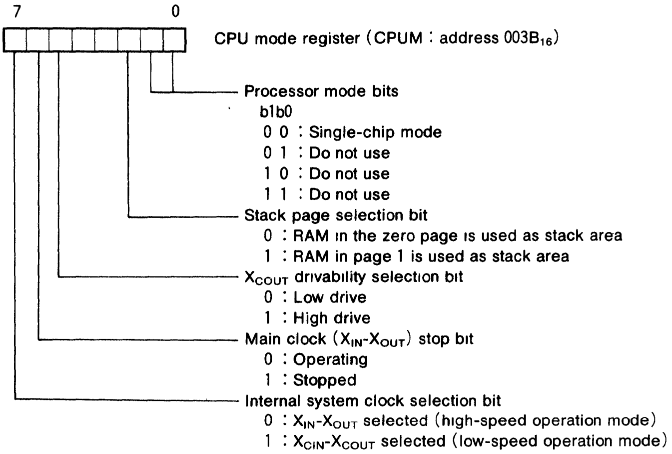
CPU MODE REGISTER

The CPU mode register is allocated to address $003B_{16}$.

Bits 0 and 1 of this register are processor mode bits and should always be set to "0".

The CPU mode register contains the stack page selection bit.

For details of the X_{COUT} drivability selection bit, main clock stop bit, and internal system clock selection bit, see the section on the clock generation circuit.



CPU mode register (CPUM : address $003B_{16}$)

Processor mode bits
b1b0
0 0 : Single-chip mode
0 1 : Do not use
1 0 : Do not use
1 1 : Do not use

Stack page selection bit
0 : RAM in the zero page is used as stack area
1 : RAM in page 1 is used as stack area

X_{COUT} drivability selection bit
0 : Low drive
1 : High drive

Main clock (X_{IN}-X_{OUT}) stop bit
0 : Operating
1 : Stopped

Internal system clock selection bit
0 : X_{IN}-X_{OUT} selected (high-speed operation mode)
1 : X_{CIN}-X_{COUT} selected (low-speed operation mode)

Fig. 1 Structure of CPU mode register

MEMORY

- **Special Function Register (SFR) Area**
  The Special Function Register area contains registers which control functions such as I/O ports and timers, and is located in the zero page area.
- **RAM**
  RAM is used for data storage as well for stack area.
- **ROM**
  The first 128 bytes and the last two bytes of ROM are reserved for device testing and the rest is user area for storing programs.
- **Interrupt Vector Area**
  The interrupt vector area contains reset and interrupt vectors.
- **Zero Page**
  The 256 bytes from addresses 0000_{16} to $00FF_{16}$ are called the zero page area. The internal RAM and the special function registers (SFR) are allocated to this area.
  The zero page addressing mode can be used to specify memory and register addresses in the zero page area. This dedicated zero page addressing mode enables access to this area with only 2 bytes.
- **Special Page**
  The 256 bytes from addresses $FF00_{16}$ to $FFFF_{16}$ are called the special page area. The special page addressing mode can be used to specify memory addresses in the special page area. This dedicated special page addressing mode enables access to this area with only 2 bytes.

RAM area

RAM capacity (bytes)	Address $XXXX_{16}$
192	$00FF_{16}$
256	$013F_{16}$
384	$01BF_{16}$
512	$023F_{16}$
640	$02BF_{16}$
768	$033F_{16}$
896	$03BF_{16}$
1024	$043F_{16}$

ROM area

ROM capacity (bytes)	Address $YYYY_{16}$	Address $ZZZZ_{16}$
4096	$F000_{16}$	$F080_{16}$
8192	$E000_{16}$	$E080_{16}$
12288	$D000_{16}$	$D080_{16}$
16384	$C000_{16}$	$C080_{16}$
20480	$B000_{16}$	$B080_{16}$
24576	$A000_{16}$	$A080_{16}$
28672	9000_{16}	9080_{16}
32768	8000_{16}	8080_{16}

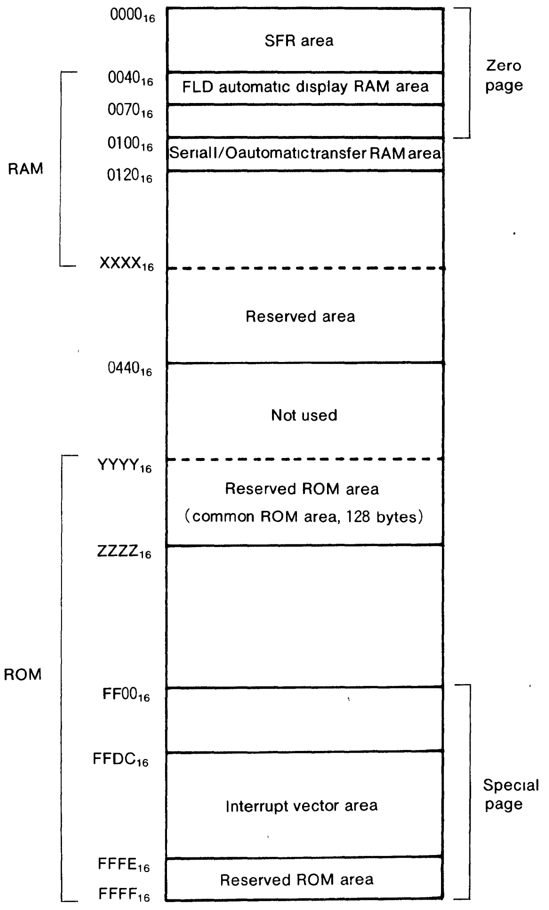


Fig. 2 Memory map diagram

0000_{16}	Port P0 (P0)	0020_{16}	Timer 1 (T1)
0001_{16}		0021_{16}	Timer 2 (T2)
0002_{16}	Port P1 (P1)	0022_{16}	Timer 3 (T3)
0003_{16}		0023_{16}	Timer 4 (T4)
0004_{16}	Port P2 (P2)	0024_{16}	Timer 5 (T5)
0005_{16}	Port P2 direction register (P2D)	0025_{16}	Timer 6 (T6)
0006_{16}	Port P3 (P3)	0026_{16}	
0007_{16}		0027_{16}	Timer 6 PWM register (T6PWM)
0008_{16}	Port P4 (P4)	0028_{16}	Timer 12 mode register (T12M)
0009_{16}	Port P4 direction register (P4D)	0029_{16}	Timer 34 mode register (T34M)
$000A_{16}$	Port P5 (P5)	$002A_{16}$	Timer 56 mode register (T56M)
$000B_{16}$	Port P5 direction register (P5D)	$002B_{16}$	PWM control register (PWMCON)
$000C_{16}$	Port P6 (P6)	$002C_{16}$	PWM register (upper)(PWMH)
$000D_{16}$	Port P6 direction register (P6D)	$002D_{16}$	PWM register (lower)(PWML)
$000E_{16}$	Port P7 (P7)	$002E_{16}$	
$000F_{16}$	Port P7 direction register (P7D)	$002F_{16}$	
0010_{16}	Port P8 (P8)	0030_{16}	A-D control register (ADCON)
0011_{16}	Port P8 direction register (P8D)	0031_{16}	A-D conversion register (AD)
0012_{16}		0032_{16}	Port P0 segment/digit switching register (P0SDR)
0013_{16}		0033_{16}	Port P1 digit/port switching register (P1DPR)
0014_{16}		0034_{16}	Port P8 segment/port switching register (P8SPR)
0015_{16}		0035_{16}	Key-scan blanking register (KSCN)
0016_{16}		0036_{16}	FLDC mode register (FLDM)
0017_{16}		0037_{16}	FLD data pointer (FLDDP)
0018_{16}	Serial I/O automatic transfer data pointer (SIODP)	0038_{16}	High-breakdown-voltage port control register (HVPC)
0019_{16}	Serial I/O1 control register (SIO1CON)	0039_{16}	
$001A_{16}$	Serial I/O automatic transfer control register (SIOAC)	$003A_{16}$	Interrupt edge selection register (INTEDGE)
$001B_{16}$	Serial I/O1 register (SIO1)	$003B_{16}$	CPU mode register (CUPM)
$001C_{16}$	Serial I/O automatic transfer interval register (SIOAI)	$003C_{16}$	Interrupt request register 1 (IREQ1)
$001D_{16}$	Serial I/O2 control register (SIO2CON)	$003D_{16}$	Interrupt request register 2 (IREQ2)
$001E_{16}$		$003E_{16}$	Interrupt control register 1 (ICON1)
$001F_{16}$	Serial I/O2 register (SIO2)	$003F_{16}$	Interrupt control register 2 (ICON2)

Fig. 3 Memory map of special function register (SFR)

I/O PORTS

- **Direction Registers**

The M3817x group microprocessors have 45 programmable I/O pins arranged in six I/O ports (ports P2 and P4 to P8). The I/O ports have direction registers which determine the input/output direction of each individual pin. Each bit in a direction register corresponds to one pin, each pin can be set to be input or output.

When "0" is written to the bit corresponding to a pin, that pin becomes an input pin. When "1" is written to that bit, that pin becomes an output pin.

If data is read from a pin which is set for output, the value of the port output latch is read, not the value of the pin itself. Pins set to input are floating. If a pin set to input is written to, only the port output latch is written to and the pin remains floating.

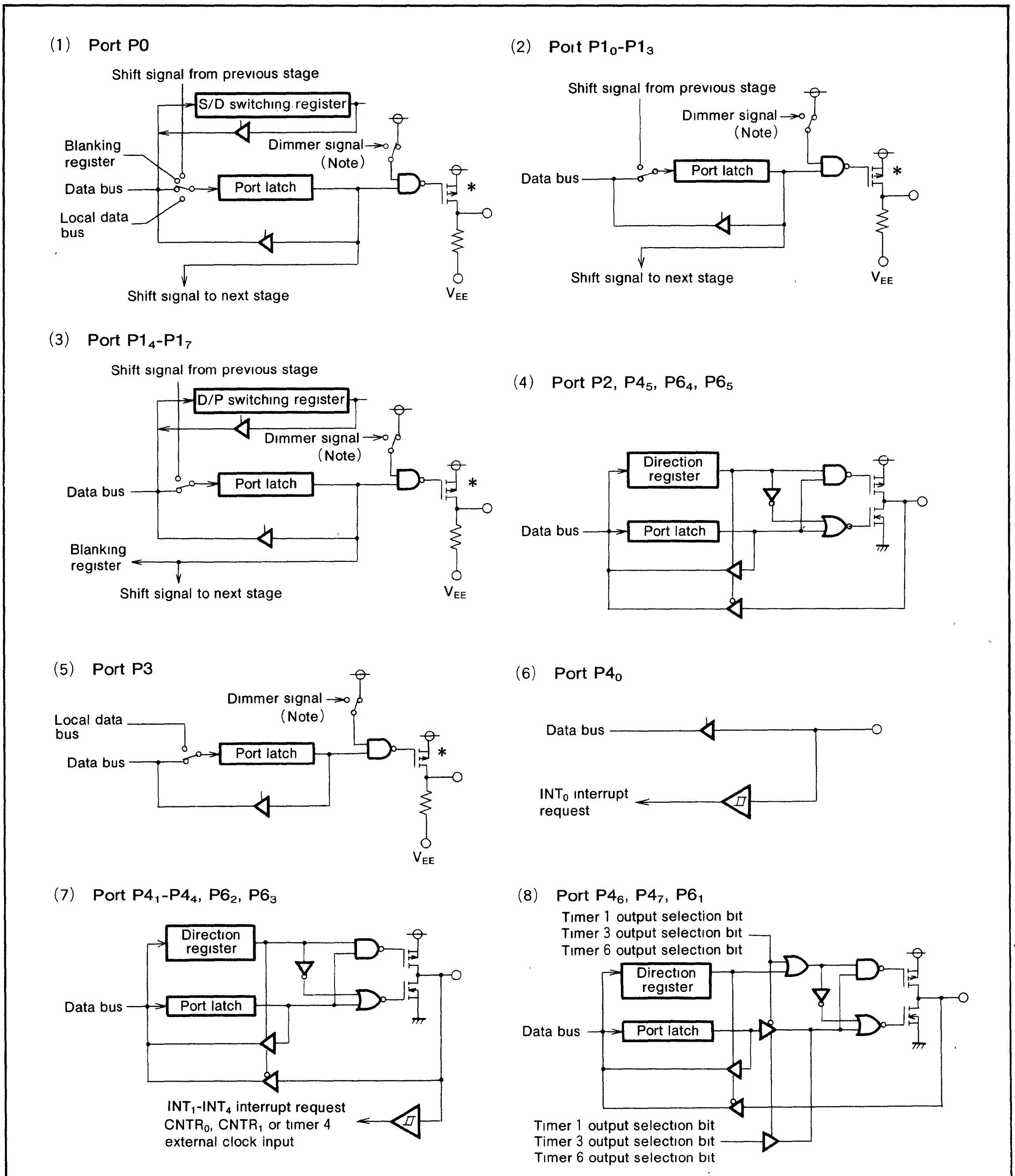
- **High-Breakdown-Voltage Output Ports**

The M3817x group microprocessors have four ports with high-breakdown-voltage pins(ports P0, P1, P3, P8). The high-breakdown-voltage ports have P-channel open drain output with a breakdown voltage of $V_{CC}-40V$. Each pin in Ports P0, P1, and P3 has an internal pull-down resistor connected to V_{EE}. Port P8 has no internal pull-down resistors and external resistors should be used if necessary. At reset, the P-channel output transistor of each port latch is turned off, so it is forced to the level of V_{EE} by the pull-down resistor.

Writing "1" to bit 0 of the high-breakdown-voltage port control register(address 0038_{16})slows the transition of the output transistors to reduce transient noise. At reset, bit 0 of the high-breakdown-voltage port control register is set to "0" (strong drive).

Pin	Name	Input/Output	I/O Format	Non-Port Function	Related SFRs	Diagram No
$P0_0/SEG_{16}/DIG_0$-$P0_7/SEG_{23}/DIG_7$	Port P0	Output	High-breakdown-voltage P-channel open-drain output with pull-down resistor	FLD automatic display function	FLDC mode register Segment/digit switching register High-breakdown-voltage port control register	(1)
$P1_0/DIG_8$-$P1_3/DIG_{11}$	Port P1	Output	High-breakdown-voltage P-channel open-drain output with pull-down resistor	FLD automatic display function	FLDC mode register High-breakdown-voltage port control register	(2)
$P1_4/DIG_{12}$-$P1_7/DIG_{15}$					FLDC mode register Digit/port switching register High-breakdown-voltage port control register	(3)
$P2_0$-$P2_7$	Port P2	Input/output, individual bits	TTL level input CMOS 3-state output			(4)
$P3_0/SEG_8$-$P3_7/SEG_{15}$	Port P3	Output	High-breakdown-voltage P-channel open-drain output with pull-down resistor	FLD automatic display function	FLDC mode register High-breakdown-voltage port control register	(5)
$P4_0/INT_0$	Port P4	Input	CMOS level input	External interrupt input	Interrupt edge selection register	(6)
$P4_1/INT_1$-$P4_4/INT_4$		Input/output, individual bits	CMOS level input CMOS 3-state output	External interrupt input	Interrupt edge selection register	(7)
$P4_5$						(4)
$P4_6/T1_{OUT}$, $P4_7/T3_{OUT}$				Timer output	Timer 12 mode register Timer 34 mode register	(8)
$P5_0/S_{IN1}$,	Port P5	Input/output, individual bits	CMOS level input N-channel open-drain output	Serial I/O1 function I/O	Serial I/O1 control register Serial I/O automatic transfer control register	(9)
$P5_1/S_{OUT1}$, $P5_2/S_{CLK1}$,						(10)
$P5_3/\overline{S_{RDY1}}/\overline{CS}/S_{CLK12}$						(11)
$P5_4/S_{IN2}$,				Serial I/O2 function I/O	Serial I/O2 control register	(9)
$P5_5/S_{OUT2}$, $P5_6/S_{CLK2}$,						(10)
$P5_7/\overline{S_{RDY2}}$						(11)
$P6_0/PWM_0$	Port P6	Input/output, individual bits	CMOS level input CMOS 3-state output	14-bit PWM output	PWM control register PWML register PWMH register	(12)
$P6_1/PWM_1$				8-bit PWM output	Timer 56 mode register Timer6 PWM register	(8)
$P6_2/CNTR_0$, $P6_3/CNTR_1$				External count input	Interrupt edge selection register	(7)
$P6_4$, $P6_5$						(4)
$P7_0/AN_0$-$P7_7/AN_7$	Port P7	Input/output, individual bits	CMOS level input CMOS 3-state output	A-D converter input	A-D control register	(13)
$P8_0/SEG_0$-$P8_7/SEG_7$	Port P8	Input/output, individual bits	CMOS level input High-breakdown-voltage P-channel open-drain output without pull-down resistor	FLD automatic display function	FLDC mode register Segment/port switching register High-breakdown-voltage port control registor	(14)

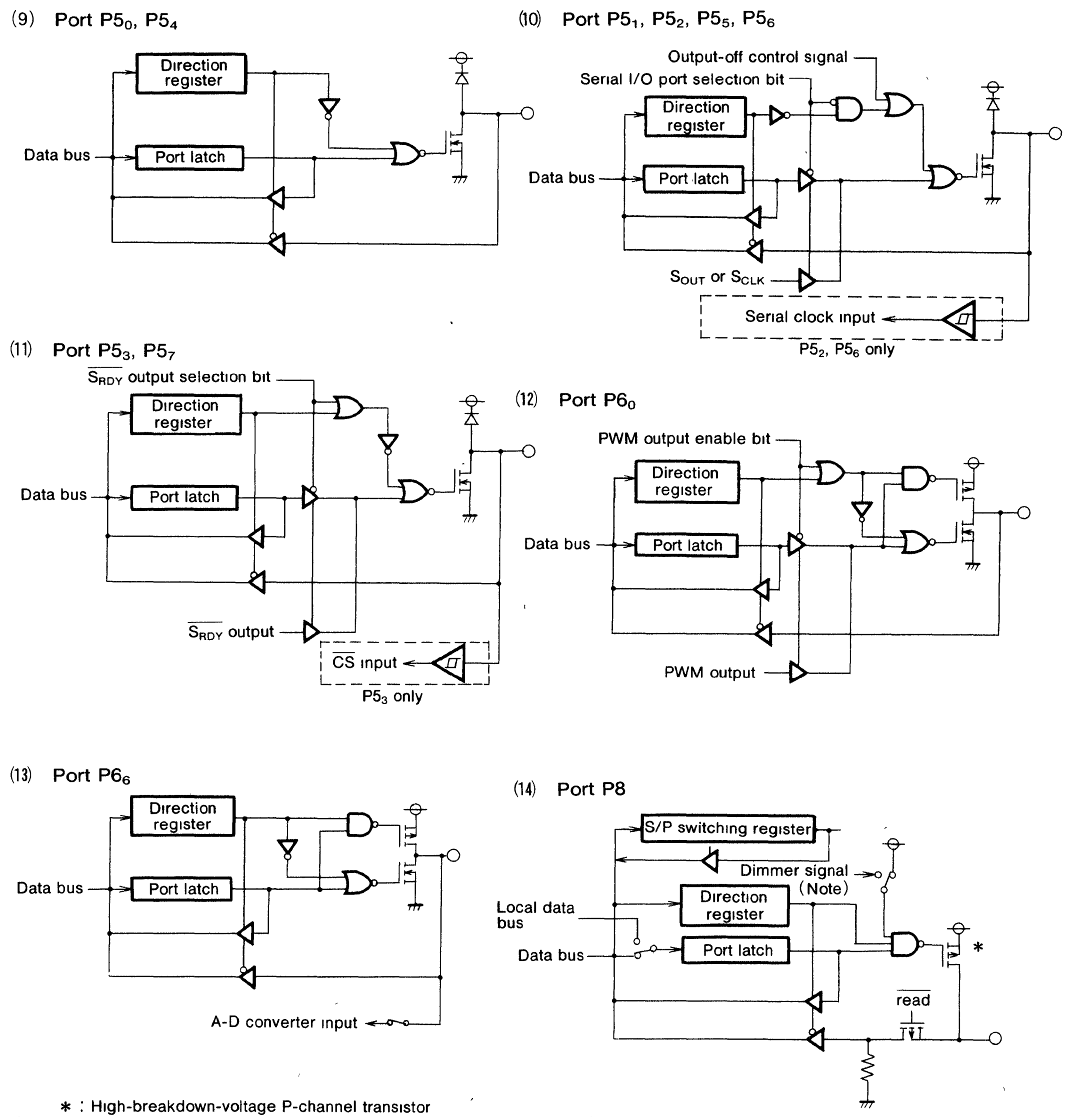
Note. Make sure that the input level at each pin is either 0V or V_{CC} during execution of the STP instruction
If an input level is at an intermediate potential, a current will flow in the input-stage gate



* : High-breakdown-voltage P-channel transistor

Note. The dimmer signal sets the Toff timing

Fig. 4 Port block diagram (1)


(9) Port $P5_0$, $P5_4$

(10) Port $P5_1$, $P5_2$, $P5_5$, $P5_6$

(11) Port $P5_3$, $P5_7$

(12) Port $P6_0$

(13) Port $P6_6$

(14) Port P8

* : High-breakdown-voltage P-channel transistor

Note: Note The dimmer signal sets the Toff timing

Fig. 5 Port block diagram (2)

INTERRUPTS

A total of 18 source can generate interrupts: 5 external, 12 internal, and 1 software.

- **Interrupt Control**

  Each interrupt is controlled by its interrupt request bit, its interrupt enable bit, and the interrupt disable flag except for the software interrupt set by the BRK instruction. An interrupt is generated if the corresponding interrupt request and enable bits are "1" and the interrupt disable flag is "0".

  Interrupt enable bits can be set or cleared by software.

  Interrupt request bits can be cleared by software, but cannot be set by software.

  The I flag disables all interrupts except for the BRK instruction interrupt.

- **Interrupt Operation**

  When an interrupt is received, the program counter and processor status register are automatically pushed onto the stack. The interrupt disable flag is set to inhibit other interrupts from interfering. The corresponding interrupt request bit is cleared and the interrupt jump destination address is read from the vector table into the program counter.

- **Notes on Use**

  If you will change interrupt edge selection from rising edge to falling edge, interrupt request bit will be set to "1" automatically. Therefore, please make following process;

  (1) Disable INT which is selected.
  (2) Change INT edge selection.
  (3) Clear interrupt request which is selected.
  (4) Enable INT which is selected.

Table 1. Interrupt vector addresses and priorities

Interrupt Cause	Priority	Vector Address (Note 1)		Interrupt Request Generation Conditions	Remarks
		High	Low		
Reset (Note 2)	1	FFFD$_{16}$	FFFC$_{16}$	At reset	Non-maskable
INT$_0$	2	FFFB$_{16}$	FFFA$_{16}$	At detection of either rising or falling edge of INT$_0$ input	External interrupt (active edge selectable)
INT$_1$	3	FFF9$_{16}$	FFF8$_{16}$	At detection of either rising or falling edge of INT$_1$ input	External interrupt (active edge selectable)
INT$_2$	4	FFF7$_{16}$	FFF6$_{16}$	At detection of either rising or falling edge of INT$_2$ input	External interrupt (active edge selectable)
Serial I/O1	5	FFF5$_{16}$	FFF4$_{16}$	At end of data transfer	Valid when serial I/O normal mode is selected
Serial I/O automatic transfer				At end of final data transfer	Valid when serial I/O automatic transfer mode is selected
Serial I/O2	6	FFF3$_{16}$	FFF2$_{16}$	At end of data transfer	
Timer 1	7	FFF1$_{16}$	FFF0$_{16}$	At timer 1 overflow	
Timer 2	8	FFEF$_{16}$	FFEE$_{16}$	At timer 2 overflow	STP release timer overflow
Timer 3	9	FFED$_{16}$	FFEC$_{16}$	At timer 3 overflow	
Timer 4	10	FFEB$_{16}$	FFEA$_{16}$	At timer 4 overflow	
Timer 5	11	FFE9$_{16}$	FFE8$_{16}$	At timer 5 overflow	
Timer 6	12	FFE7$_{16}$	FFE6$_{16}$	At timer 6 overflow	
INT$_3$	13	FFE5$_{16}$	FFE4$_{16}$	At detection of either rising or falling edge of INT$_3$ input	External interrupt (active edge selectable)
INT$_4$	14	FFE3$_{16}$	FFE2$_{16}$	At detection of either rising or falling edge of INT$_4$ input	External interrupt valid when INT$_4$ interrupt is selected (active edge selectable)
A-D converter				At end of A-D conversion	Valid when A-D interrupt is selected
FLD blanking	15	FFE1$_{16}$	FFE0$_{16}$	At fall of final digit	Valid when FLD blanking interrupt is selected
FLD digit				At rise of each digit	Valid when FLD digit interrupt is selected
BRK instruction	16	FFDD$_{16}$	FFDC$_{16}$	At BRK instruction execution	Non-maskable software interrupt

Note 1. Vector addresses contain interrupt jump destination addresses
2. Reset function in the same way as an interrupt with the highest priority

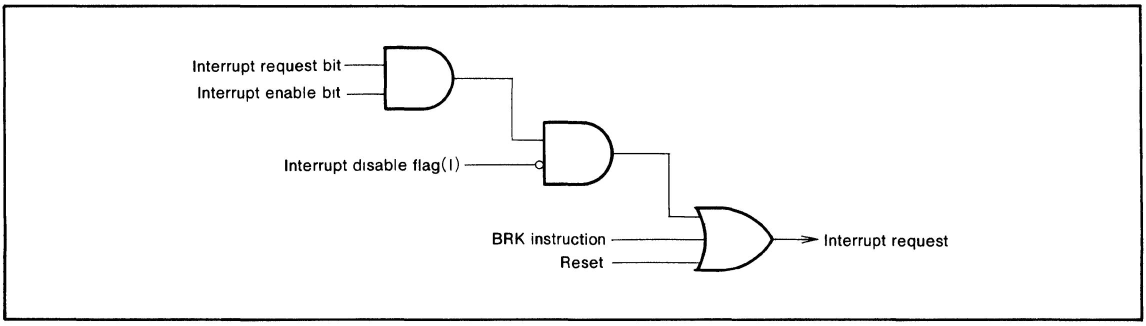


Fig. 6 Interrupt control

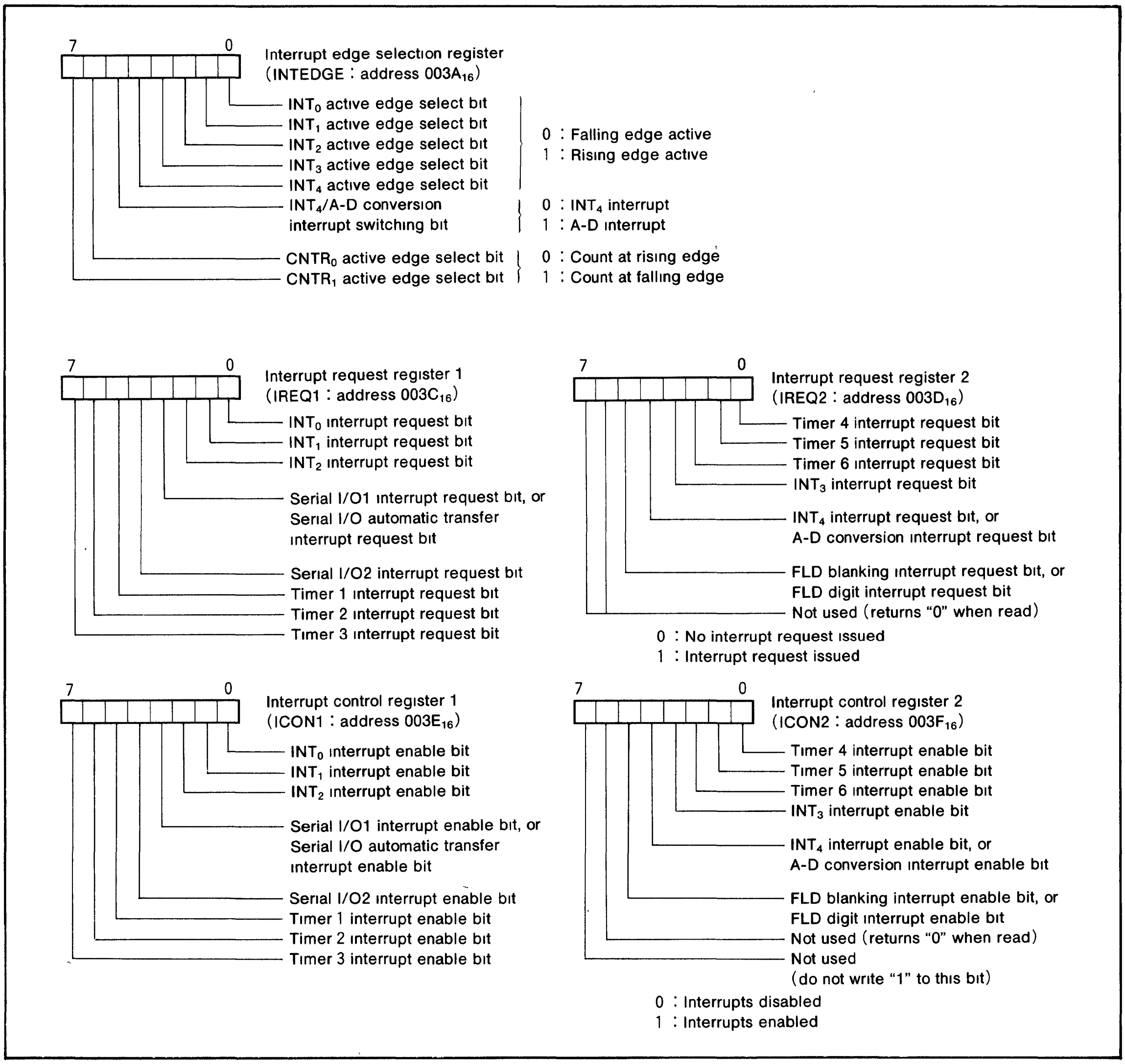


Fig. 7 Structure of interrupt-related registers

TIMERS

Microcomputers of the M3817x group have six built-in timers. The timers count down. Once a timer reaches 00_{16}, the next count pulse loads the contents of the corresponding timer latch into the timer, and sets the corresponding interrupt request bit to 1. Each timer also has a stop bit that stops the count of that timer when it is set to "1".

Note that the system clock ϕ can be set to either high-speed mode or low-speed mode by the CPU mode register.

- **Timer 1 and Timer 2**

  The count sources of timer 1 and timer 2 can be selected by setting the timer 12 mode register.

  Timer 1 can also output a rectangular waveform from the $P4_6/T1_{OUT}$ pin. The waveform changes polarity each time timer 1 overflows.

  The active edge of the external signal $CNTR_0$ can be set by the interrupt edge selection register.

  When the chip is reset or the STP instruction is executed, all bits of the timer 12 mode register are cleared, timer 1 is set to FF_{16}, and timer 2 is set to 01_{16}.

- **Timer 3 and Timer 4**

  The count sources of timer 3 and timer 4 can be selected by setting the timer 34 mode register.

  Timer 3 can also output a rectangular waveform from the $P4_7/T3_{OUT}$ pin. The waveform changes polarity each time timer 3 overflows.

  The active edge of the external signal $CNTR_1$ can be set by the interrupt edge selection register.

- **Timer 5 and Timer 6**

  The count sources of timer 5 and timer 6 can be selected by setting the timer 56 mode register.

  Timer 6 can also output a rectangular waveform from the $P6_1/PWM_1$ pin. The waveform changes polarity each time timer 6 overflows.

- **Timer 6 PWM_1 Mode**

  Timer 6 can also output a rectangular waveform of n cycles high and m cycles low. The n is the value set in timer latch 6 (address 0025_{16}) and m is the value in the timer 6 PWM register (address 0027_{16}). If n is "0", the PWM_1 output is "L", if m is "0" and n is not "0", then the PWM_1 output is "H". In PWM mode, interrupts are generated at the rising edge of the PWM_1 output.

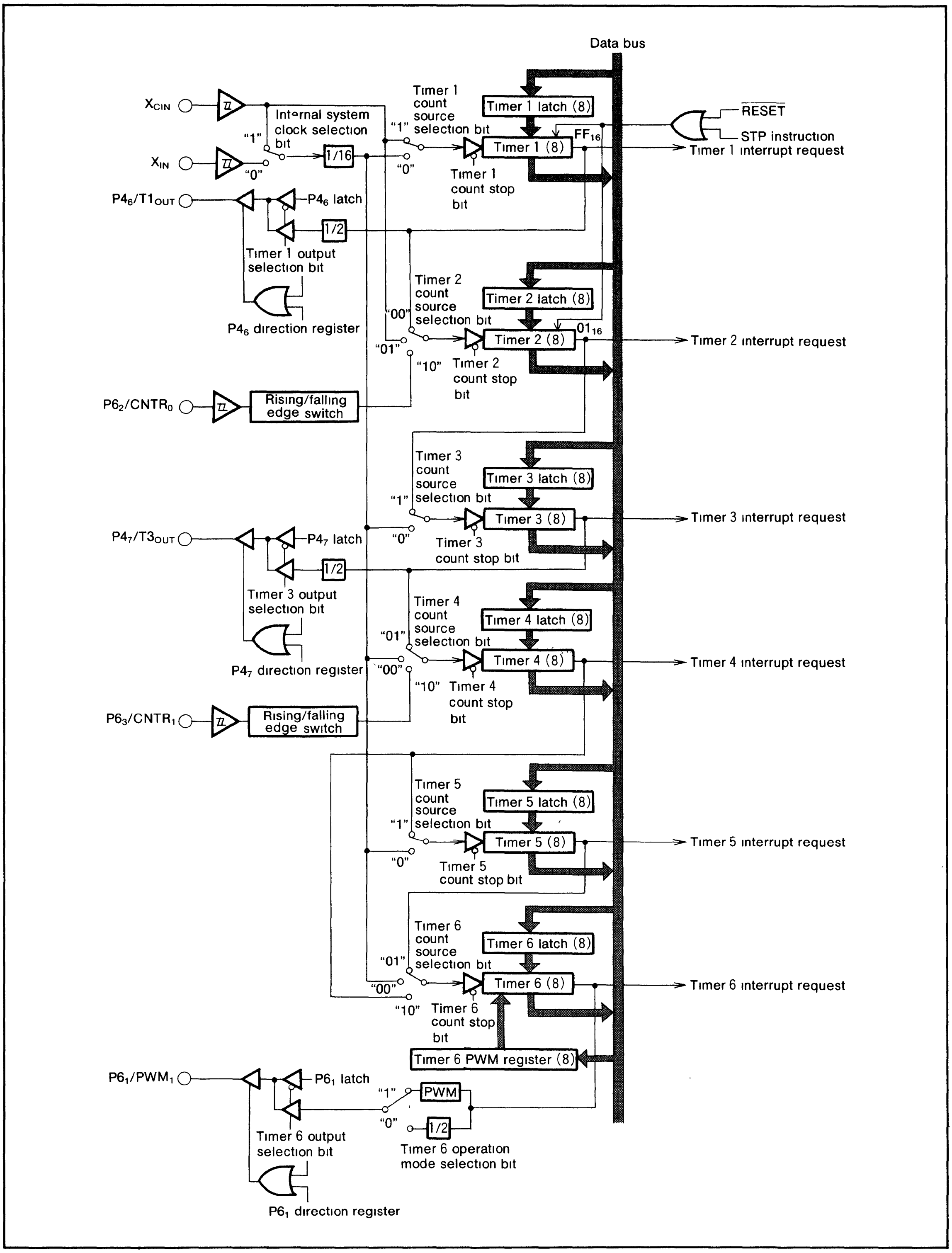
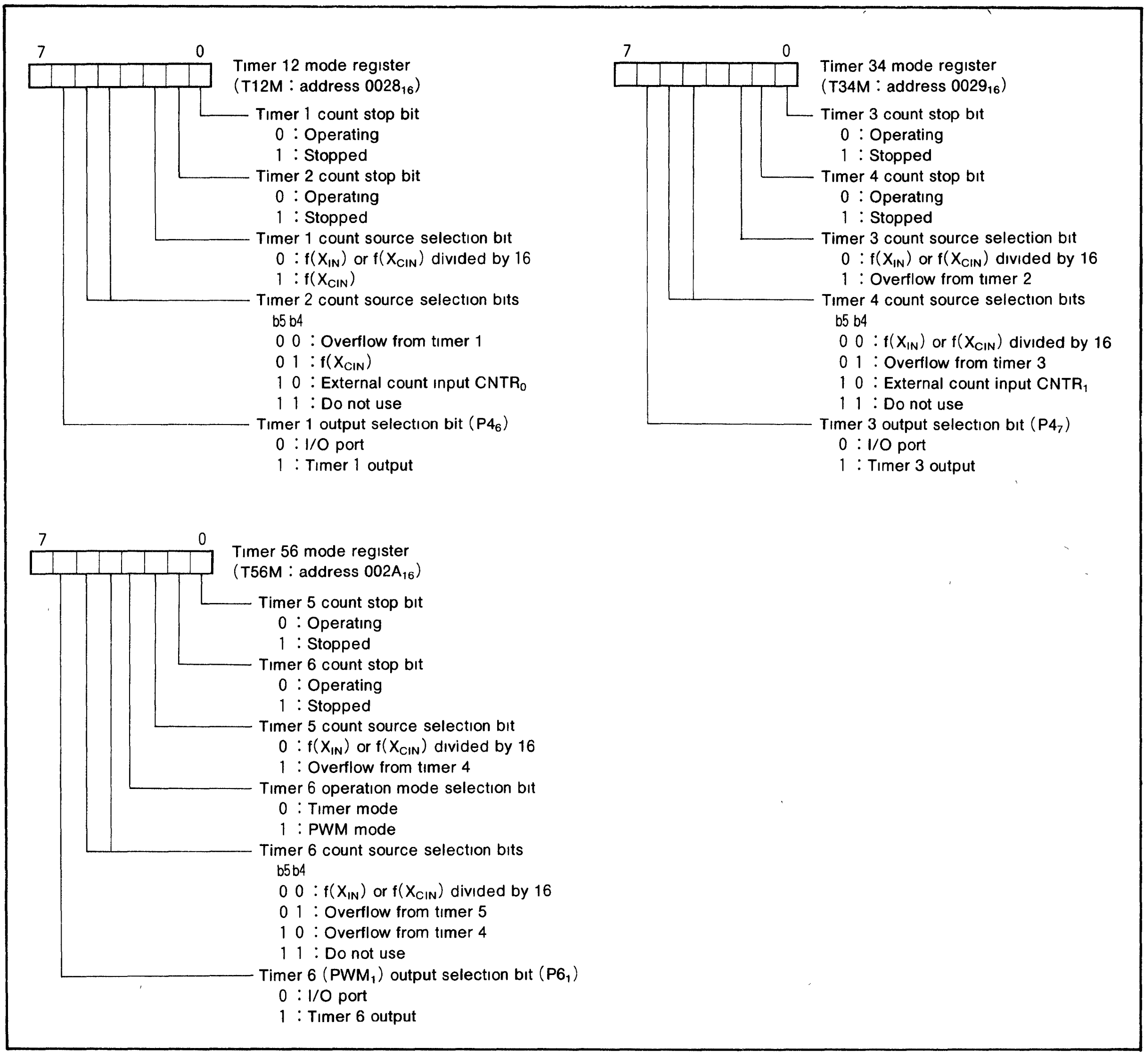


Fig. 8 Timer block diagram



Timer 12 mode register
(T12M : address 0028_{16})

- Timer 1 count stop bit
  - 0 : Operating
  - 1 : Stopped
- Timer 2 count stop bit
  - 0 : Operating
  - 1 : Stopped
- Timer 1 count source selection bit
  - 0 : $f(X_{IN})$ or $f(X_{CIN})$ divided by 16
  - 1 : $f(X_{CIN})$
- Timer 2 count source selection bits
  - b5 b4
  - 0 0 : Overflow from timer 1
  - 0 1 : $f(X_{CIN})$
  - 1 0 : External count input $CNTR_0$
  - 1 1 : Do not use
- Timer 1 output selection bit ($P4_6$)
  - 0 : I/O port
  - 1 : Timer 1 output

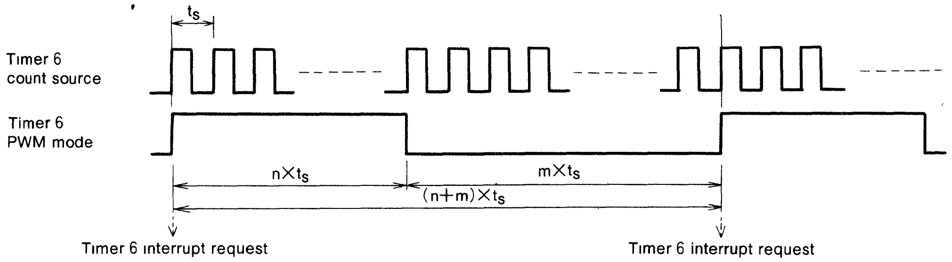
Timer 34 mode register
(T34M : address 0029_{16})

- Timer 3 count stop bit
  - 0 : Operating
  - 1 : Stopped
- Timer 4 count stop bit
  - 0 : Operating
  - 1 : Stopped
- Timer 3 count source selection bit
  - 0 : $f(X_{IN})$ or $f(X_{CIN})$ divided by 16
  - 1 : Overflow from timer 2
- Timer 4 count source selection bits
  - b5 b4
  - 0 0 : $f(X_{IN})$ or $f(X_{CIN})$ divided by 16
  - 0 1 : Overflow from timer 3
  - 1 0 : External count input $CNTR_1$
  - 1 1 : Do not use
- Timer 3 output selection bit ($P4_7$)
  - 0 : I/O port
  - 1 : Timer 3 output

Timer 56 mode register
(T56M : address $002A_{16}$)

- Timer 5 count stop bit
  - 0 : Operating
  - 1 : Stopped
- Timer 6 count stop bit
  - 0 : Operating
  - 1 : Stopped
- Timer 5 count source selection bit
  - 0 : $f(X_{IN})$ or $f(X_{CIN})$ divided by 16
  - 1 : Overflow from timer 4
- Timer 6 operation mode selection bit
  - 0 : Timer mode
  - 1 : PWM mode
- Timer 6 count source selection bits
  - b5 b4
  - 0 0 : $f(X_{IN})$ or $f(X_{CIN})$ divided by 16
  - 0 1 : Overflow from timer 5
  - 1 0 : Overflow from timer 4
  - 1 1 : Do not use
- Timer 6 (PWM_1) output selection bit ($P6_1$)
  - 0 : I/O port
  - 1 : Timer 6 output

Fig. 9 Structure of timer-related registers



Note. If the value set in timer 6 is n and the value set in the timer 6 PWM register is m, a PWM waveform with duty cycle n/(n+m) and period $(n+m) \times t_S$ is output (where is t_S the frequency of the timer 6 count source)

Fig. 10 Timing in timer 6 PWM_1 mode

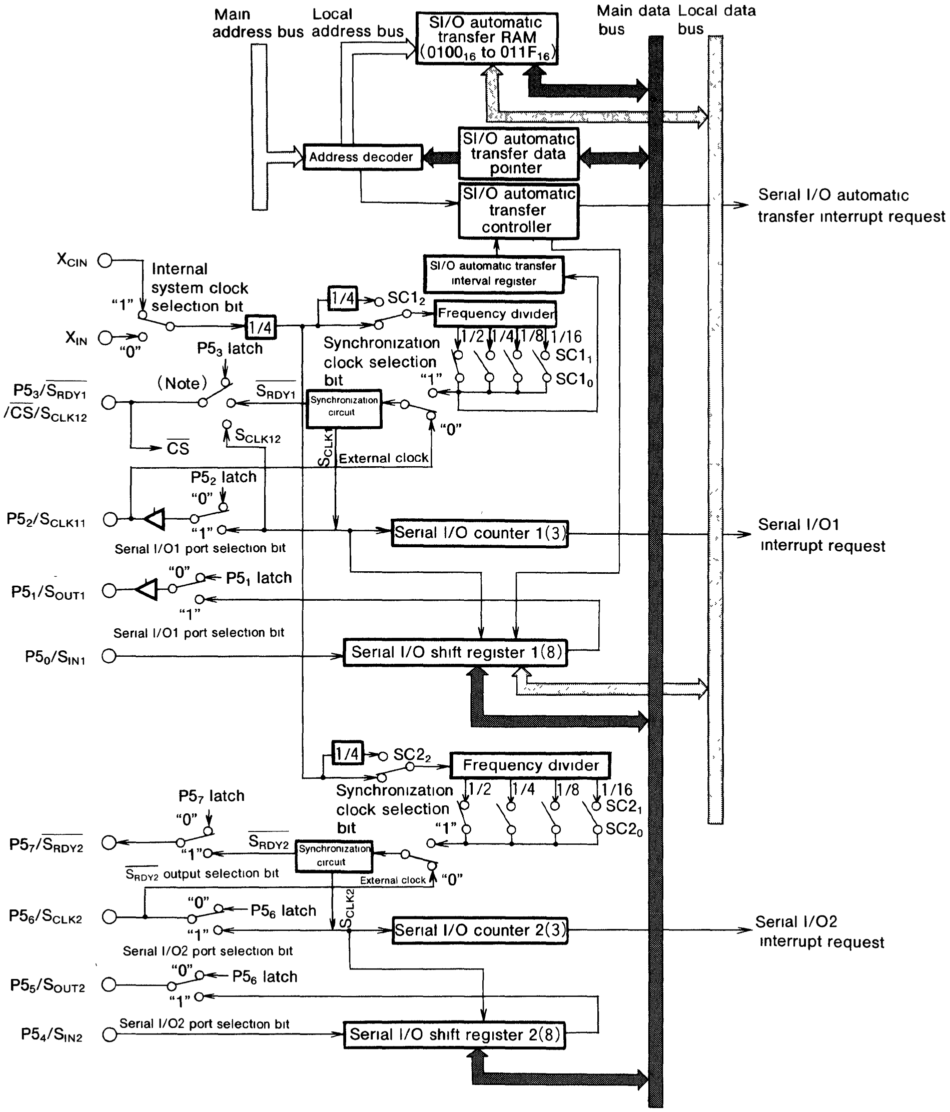
SERIAL I/O

Microcomputers of the M3817x group have two built-in 8-bit clock synchronized serial I/O channels (serial I/O1 and serial I/O2).

Serial I/O1 has a built-in automatic transfer function.Normal serial operation can be set via the serial I/O automatic transfer control register (address $001A_{16}$).

Serial I/O2 can only be used in normal operation mode.

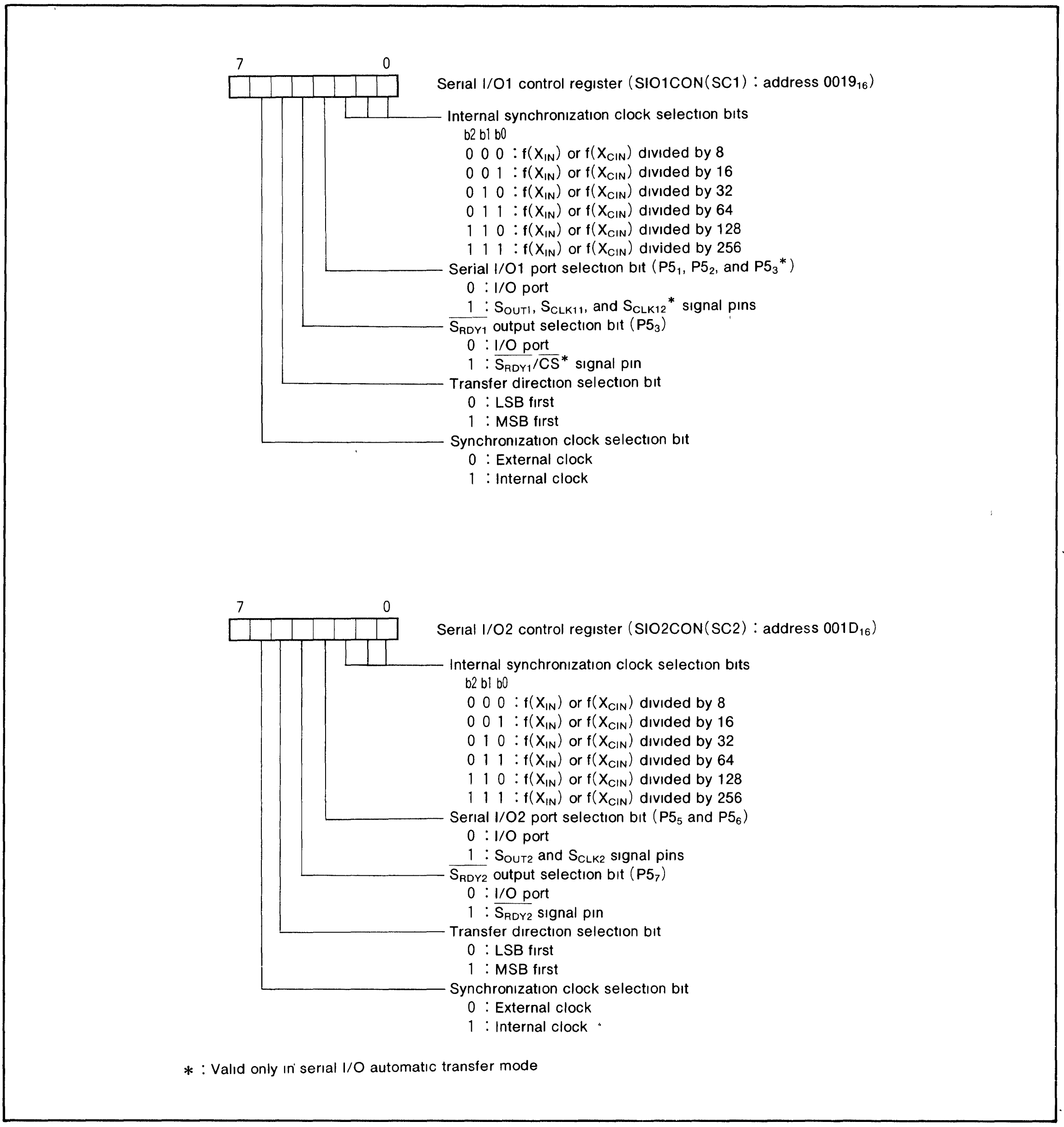
The I/O pins of the serial I/O function also operate as I/O port P5, and their operation is selected by the serial I/O control registers (addresses 0019_{16} and $001D_{16}$).



Note. Selection is by the synchronization clock selection bit, the $\overline{S_{RDY1}}$ output selection bit, and the serial I/O1 port selection bit of the serial I/O1 control register, and the automatic transfer control bit and synchronization clock output pin selection bit of the serial I/O automatic transfer control register

Fig. 11 Serial I/O block diagram

(Serial I/O Control Registers) SIO1CON, SIO2CON
Each of the serial I/O control registers (addresses 0019_{16} and $001D_{16}$) contains seven bits that select various control parameters of the serial I/O function.



Serial I/O1 control register (SIO1CON(SC1) : address 0019_{16})

Internal synchronization clock selection bits
b2 b1 b0
0 0 0 : f(X_{IN}) or f(X_{CIN}) divided by 8
0 0 1 : f(X_{IN}) or f(X_{CIN}) divided by 16
0 1 0 : f(X_{IN}) or f(X_{CIN}) divided by 32
0 1 1 : f(X_{IN}) or f(X_{CIN}) divided by 64
1 1 0 : f(X_{IN}) or f(X_{CIN}) divided by 128
1 1 1 : f(X_{IN}) or f(X_{CIN}) divided by 256

Serial I/O1 port selection bit ($P5_1$, $P5_2$, and $P5_3$*)
0 : I/O port
1 : S_{OUT1}, S_{CLK11}, and S_{CLK12}* signal pins

$\overline{S_{RDY1}}$ output selection bit ($P5_3$)
0 : I/O port
1 : $\overline{S_{RDY1}}/\overline{CS}$* signal pin

Transfer direction selection bit
0 : LSB first
1 : MSB first

Synchronization clock selection bit
0 : External clock
1 : Internal clock

Serial I/O2 control register (SIO2CON(SC2) : address $001D_{16}$)

Internal synchronization clock selection bits
b2 b1 b0
0 0 0 : f(X_{IN}) or f(X_{CIN}) divided by 8
0 0 1 : f(X_{IN}) or f(X_{CIN}) divided by 16
0 1 0 : f(X_{IN}) or f(X_{CIN}) divided by 32
0 1 1 : f(X_{IN}) or f(X_{CIN}) divided by 64
1 1 0 : f(X_{IN}) or f(X_{CIN}) divided by 128
1 1 1 : f(X_{IN}) or f(X_{CIN}) divided by 256

Serial I/O2 port selection bit ($P5_5$ and $P5_6$)
0 : I/O port
1 : S_{OUT2} and S_{CLK2} signal pins

$\overline{S_{RDY2}}$ output selection bit ($P5_7$)
0 : I/O port
1 : $\overline{S_{RDY2}}$ signal pin

Transfer direction selection bit
0 : LSB first
1 : MSB first

Synchronization clock selection bit
0 : External clock
1 : Internal clock

* : Valid only in serial I/O automatic transfer mode

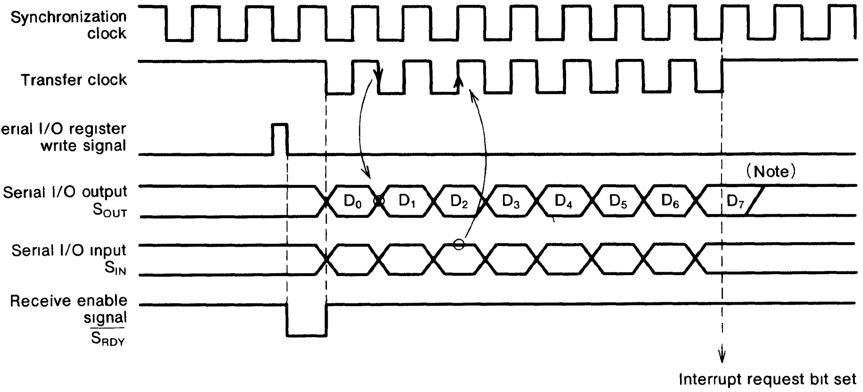
Fig. 12 Structure of serial I/O control registers

(1) Operation in Normal Serial I/O Mode

Either an internal clock or an external clock can be selected ,as the synchronization clock for serial I/O transfer. A dedicated divider is built-in as the internal clock, giving a choice of six clocks.

If internal clock is selected, transfer start is activated by a write signal to a serial I/O register (address $001B_{16}$ or $001F_{16}$). After eight bits have been transferred, the S_{OUT} pin goes to high impedance.

If external clock is selected, the clock must be controlled externally because the contents of the serial I/O register continue to shift while the transfer clock is input. In this case, note that the S_{OUT} pin does not go to high impedance at the completion of data transfer. The interrupt request bit is set at the end of the transfer of eight bits, regardless of whether the internal or external clock is selected.



Note. If internal clock is selected, the S_{OUT} pin is at high impedance after transfer ends

Fig. 13 Serial I/O timing in normal mode (for LSB first)

(2) Serial I/O Automatic Transfer Mode

The serial I/O1 function has an automatic transfer function. For automatic transfer, switch to the automatic transfer mode by setting the serial I/O automatic transfer control register (address $001A_{16}$).

The following memory spaces are added to the circuits used for the serial I/O1 function in ordinary mode, to enable automatic transfer mode:

- 32 bytes of serial I/O automatic transfer RAM
- A serial I/O automatic transfer control register
- A serial I/O automatic transfer interval register
- A serial I/O automatic transfer data pointer

When using serial I/O automatic transfer, set the serial I/O control register (address 0019_{16}) in the same way as for ordinary mode. However, note that if external clock is selected and bit 4 (the $\overline{S_{RDY1}}$ output selection bit) of the serial I/O1 control register is set to "1", port $P5_3$ becomes the $\overline{CS}$ input pin.

(Serial I/O Automatic Transfer Control Register) SIOAC

The serial I/O automatic transfer control register (address $001A_{16}$) contains four bits that select various control parameters for automatic transfer.

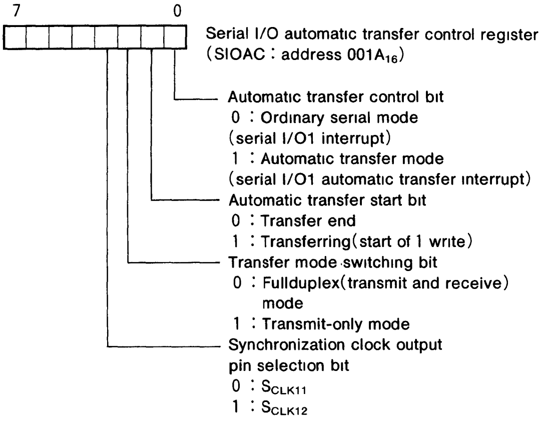


Fig. 14 Structure of serial I/O automatic transfer control register

(Serial I/O Automatic Transfer Data Pointer) SIODP

The serial I/O automatic transfer data pointer (address 0018_{16}) contains five bits that indicate addresses in serial I/O automatic transfer RAM (each address in memory is actually the value in the serial I/O automatic transfer data pointer plus 0100_{16}).

Set the serial I/O automatic transfer data pointer to (the number of transfer data−1), to specify the storage position of the start of data.

- Serial I/O Automatic Transfer RAM
  The serial I/O automatic transfer RAM is the 32 bytes from address 0100_{16} to address $011F_{16}$.
- Setting of Serial I/O Automatic Transfer Data
  When data is stored in the serial I/O automatic transfer RAM, it is stored with the start of the data at the address set by the serial I/O automatic transfer data pointer and the end of the data at address 0100_{16}.

(Serial I/O Automatic Transfer Interval Register) SIOAI

The serial I/O automatic transfer interval register (address $001C_{16}$) consists of a 5-bit counter that determines the transfer interval Ti during automatic transfer.

If a value n is written to the serial I/O automatic transfer interval register, a value of $Ti=(n+2)\times Tc$ is generated, where Tc is the length of one bit of the transfer clock. However, note that this transfer interval setting is only valid when internal clock has been selected as the clock source.

Bit / Address	7	6	5	4	3	2	1	0
0100_{16}								
0101_{16}								
0102_{16}								
⋮	⋮				⋮			
$011D_{16}$								
$011E_{16}$								
$011F_{16}$								

Fig. 15 Bit allocation of serial I/O automatic transfer RAM

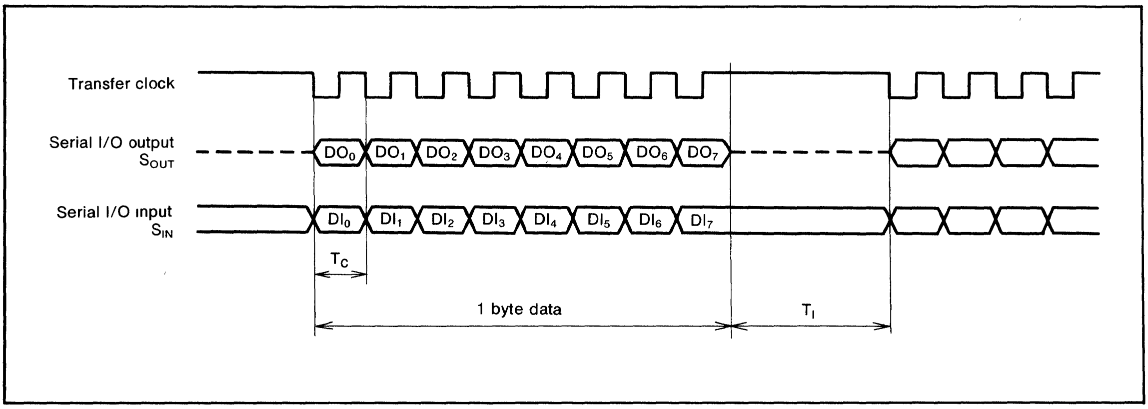


Fig. 16 Serial I/O automatic transfer interval timing

- **Setting of Serial I/O Automatic Transfer Timing**
  Use the serial I/O1 control register (address 0019_{16}) and the serial I/O automatic transfer interval register (address $001C_{16}$) to set the timing of serial I/O automatic transfer.
  The serial I/O1 control register sets the transfer clock speed, and the serial I/O automatic transfer interval register sets the serial I/O automatic transfer interval.
  This setting of transfer interval is valid only when internal clock is selected as the clock source.
- **Start of Serial I/O Automatic Transfer**
  Automatic transfer mode is set by writing "1" to bit 0 of the serial I/O automatic transfer control register (address $001A_{16}$), then automatic transfer starts when "1" is written to that bit. Bit 1 of the serial I/O automatic transfer control register is always "1" during automatic transfer; writing "0" to it is one way to end automatic transfer.
- **Operation in Serial I/O Automatic Transfer Modes**
  There are two modes for serial I/O automatic transfer: full duplex mode and transmit-only mode. Either internal or external clock can be selected for each of these modes.

(2.1) Operation in Full Duplex Mode

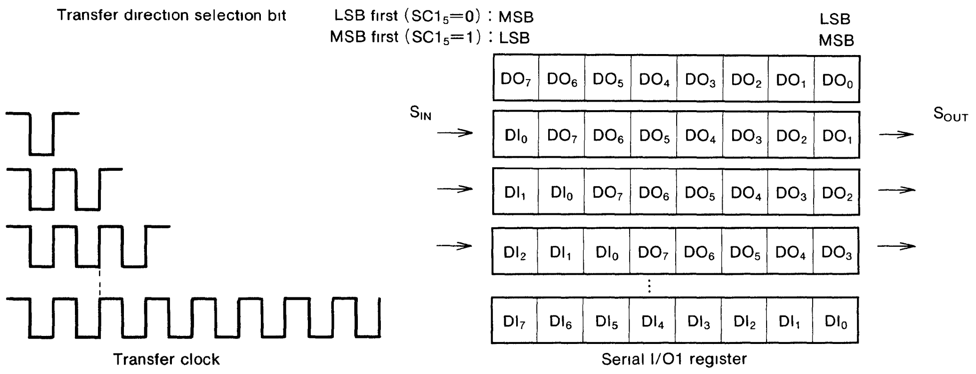
In full duplex mode, data can be transmitted and received at the same time. Data in the automatic transfer RAM is sent in sequence and simultaneously receive data is written to the automatic transfer RAM, in accordance with the serial I/O automatic transfer data pointer.

The transfer timing of each bit is the same as in ordinary operation mode, and the transfer clock stops at "H" after eight transfer clocks are counted If internal clock is selected, the transfer clock remains at "H" for the time set by the serial I/O automatic transfer interval register, then the data at the next address indicated by the serial I/O automatic transfer data pointer is transferred. If external clock is selected, the setting of the automatic transfer interval register is invalid, so the user must ensure that the transfer clock is controlled externally.

Data transfer ends when the contents of the serial I/O automatic transfer pointer reach "00_{16}". At that point, the serial I/O automatic transfer interrupt request bit is set to "1" and bit 1 of the serial I/O automatic transfer control register is cleared to "0" to complete the serial I/O automatic transfer.

(2.2) Operation in Transmit-Only Mode

The operation in transmit-only mode is the same as that in full duplex mode, except that data is not transferred from the serial I/O1 register to the serial I/O automatic transfer RAM.



DO_7	DO_6	DO_5	DO_4	DO_3	DO_2	DO_1	DO_0
DI_0	DO_7	DO_6	DO_5	DO_4	DO_3	DO_2	DO_1
DI_1	DI_0	DO_7	DO_6	DO_5	DO_4	DO_3	DO_2
DI_2	DI_1	DI_0	DO_7	DO_6	DO_5	DO_4	DO_3
			⋮				
DI_7	DI_6	DI_5	DI_4	DI_3	DI_2	DI_1	DI_0

Fig. 17 Serial I/O1 register in full duplex mode

(2.3) If Internal Clock is Selected

If internal clock is selected, the P5$_3$/$\overline{S_{RDY1}}$/$\overline{CS}$/S$_{CLK12}$ pin can be used as the $\overline{S_{RDY1}}$ pin by setting the SC1$_4$ bit to "1".

If internal clock is selected, the P5$_3$ pin can be used as the synchronization clock output pin S$_{CLK12}$ by setting the SIOAC$_3$ bit to "1". In this case, the S$_{CLK11}$ pin is at high impedance.

Select the function of the P5$_3$/$\overline{S_{RDY1}}$/$\overline{CS}$/S$_{CLK12}$ and P5$_2$/S$_{CLK11}$ pins by setting bit 3 (SC1$_3$), bit 4 (SC1$_4$), and bit 6 (SC1$_6$) of the serial I/O1 control register (address 0019$_{16}$) and bit 3 (SIOAC$_3$) of the serial I/O automatic transfer control register (address 001A$_{16}$). (See Table 2.)

If using the S$_{CLK11}$ and S$_{CLK12}$ pins for switching, set the P5$_3$/$\overline{S_{RDY1}}$/$\overline{CS}$/S$_{CLK12}$ pin to P5$_3$ by setting the SC1$_4$ bit to "0", and set the P5$_3$ direction register to input mode.

Make sure that the SIOAC$_3$ bit is switched after automatic transfer is completed, while the transfer clock is still "H".

Table 2. S$_{CLK11}$ and S$_{CLK12}$ selection

SC1$_6$	SC1$_4$	SC3$_3$	SIOAC$_3$	P5$_2$/S$_{CLK11}$	P5$_3$/S$_{CLK12}$
1	0	1	0	S$_{CLK11}$	P5$_3$
			1	High impedanse	S$_{CLK12}$

Note. SC1$_3$: Serial I/O1 port selection bit
SC1$_4$: $\overline{S_{RDY1}}$ output selection bit
SC1$_6$: Synchronization clock selection bit
SIOAC$_3$: Synchronization clock output pin selection bit

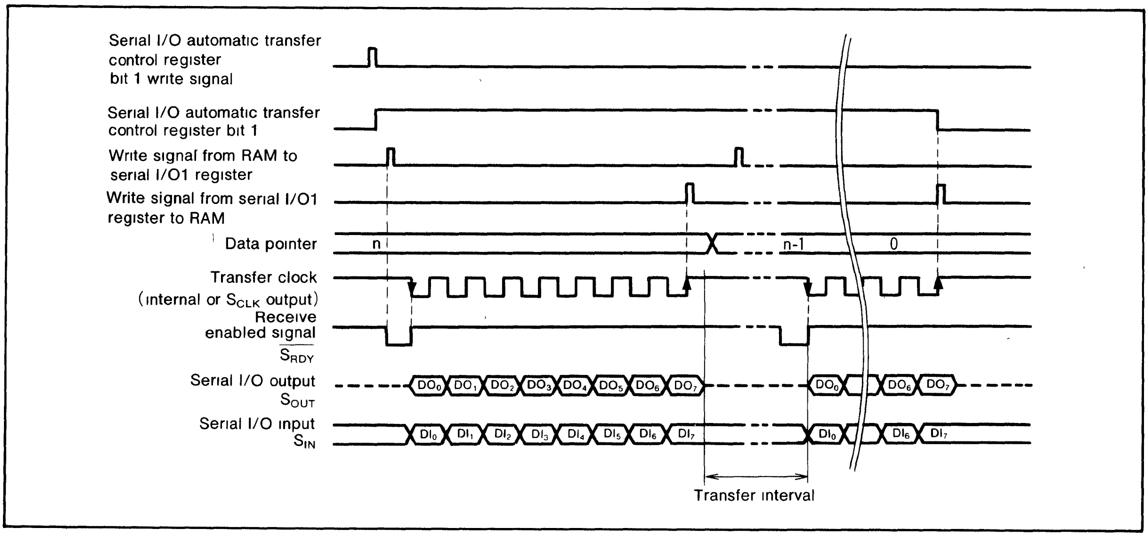


Fig. 18 Timing during serial I/O automatic transfer (internal clock selected, $\overline{S_{RDY}}$ used)

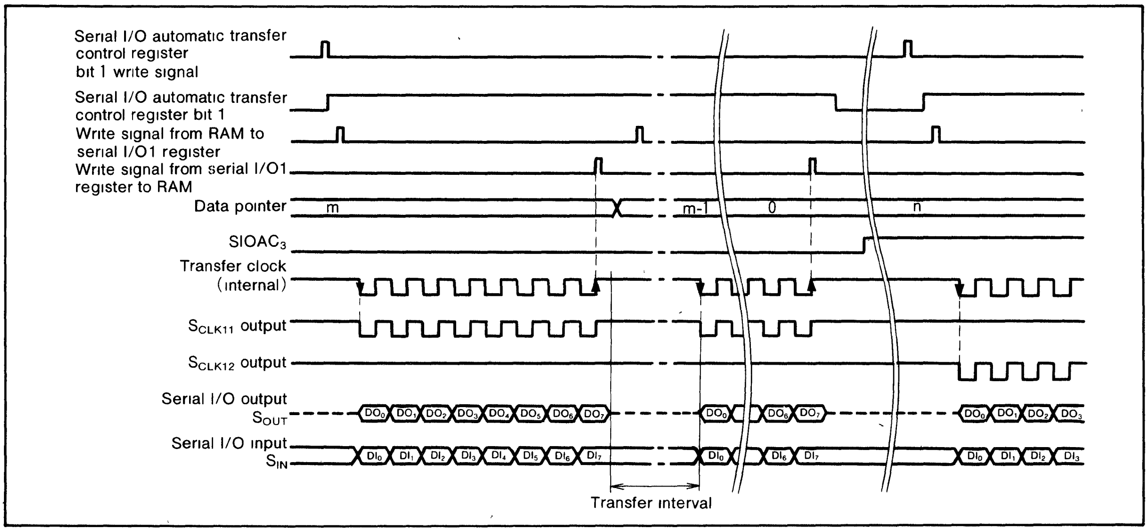


Fig. 19 Timing during serial I/O automatic transfer (internal clock selected, S$_{CLK11}$ and S$_{CLK12}$ used)

(2.4) If External Clock is Selected

If an external clock is selected, the internal clock and the transfer interval set by the serial I/O automatic transfer interval register are invalid, but the serial I/O output pin S_{OUT} and the internal transfer clock can be controlled from the outside by setting the $\overline{S_{RDY1}}$ and $\overline{CS}$ (input) pins.

When the $\overline{CS}$ input is "L", the S_{OUT} pin and the internal transfer clock are enabled. When the $\overline{CS}$ input is "H", the S_{OUT} pin is at high impedance and the internal transfer clock is at "H".

Select the function of the $P5_3/\overline{S_{RDY1}}/\overline{CS}/S_{CLK12}$ pin by setting bit 4 ($SC1_4$) and bit 6 ($SC1_6$) of the serial I/O1 control register (address 0019_{16}) and bit 0 ($SIOAC_0$) of the serial I/O automatic transfer control register (address $001A_{16}$).

Make sure that the $\overline{CS}$ pin switches from "L" to "H" or from "H" to "L" while the transfer clock (S_{CLK} input) is "H" after one byte of data has been transferred.

If external clock is selected, make sure that the external clock goes "L" after at least nine cycles of the internal system clock ϕ after the start bit is set. Leave at least 11 cycles of the system clock ϕ free for the transfer interval after one byte of data has been transferred.

If $\overline{CS}$ input is not being used, note that the S_{OUT} pin will not go high impedance, even after transfer is completed.

If $\overline{CS}$ input is not being used, or if $\overline{CS}$ is "L", control the external clock because the data in the serial I/O register will continue to shift while the external clock is input, even after the completion of automatic transfer. (Note that the automatic transfer interrupt request bit is set and bit 1 of the automatic transfer register is cleared at the point at which the specified number of bytes of data have been transferred.)

Table 3. $P5_3/\overline{S_{RDY1}}/\overline{CS}$ selection

$SC1_6$	$SC1_4$	$SIOAC_0$	$P5_3/\overline{S_{RDY1}}/\overline{CS}$
0	0	X	$P5_3$
	1	0	$\overline{S_{RDY1}}$
		1	$\overline{CS}$

Note. $SC1_4$: $\overline{S_{RDY1}}$ output selection bit
$SC1_6$: Synchronization clock selection bit
$SIOAC_0$: Automatic transfer control bit

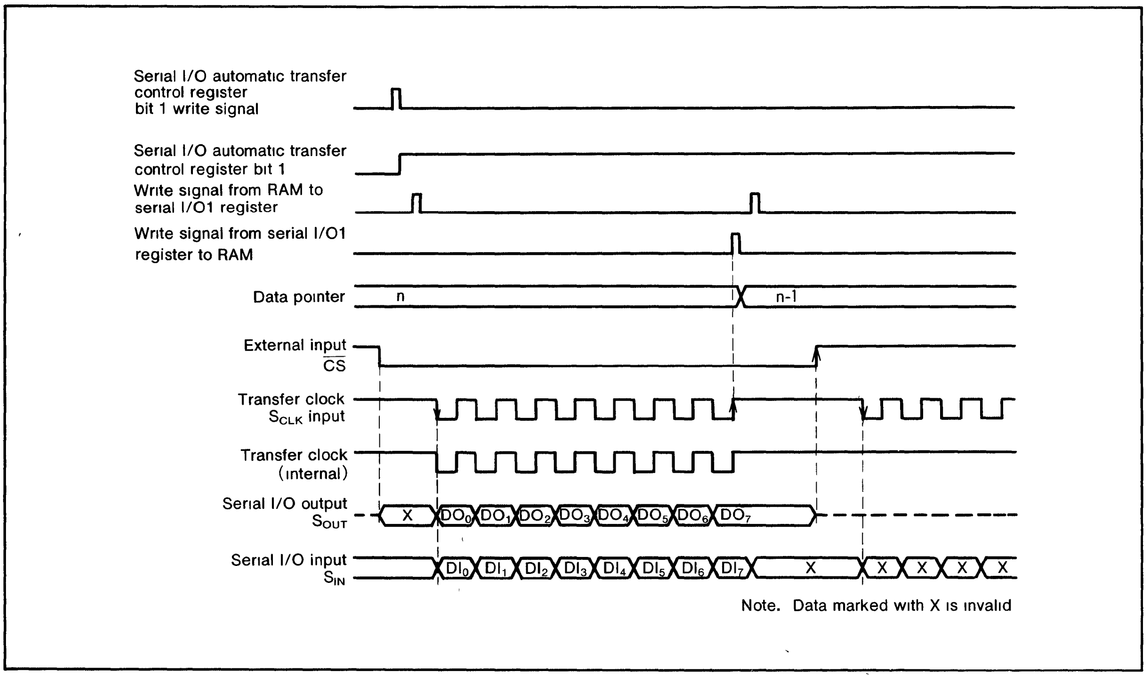


Fig. 20 Timing during serial I/O automatic transfer (external clock selected)

PULSE WIDTH MODULATION (PWM) OUTPUT CIRCUIT

Microcomputers of the M3817x group have a PWM function with a 14-bit resolution. When the oscillation frequency X_{IN} is 4MHz, the minimum resolution bit width is 500ns and the cycle period is 8192μs. The PWM timing generator supplies a PWM control signal based on a signal that is half the frequency of the X_{IN} clock.

The explanation in the rest of this data sheet assumes X_{IN}= 4MHz.

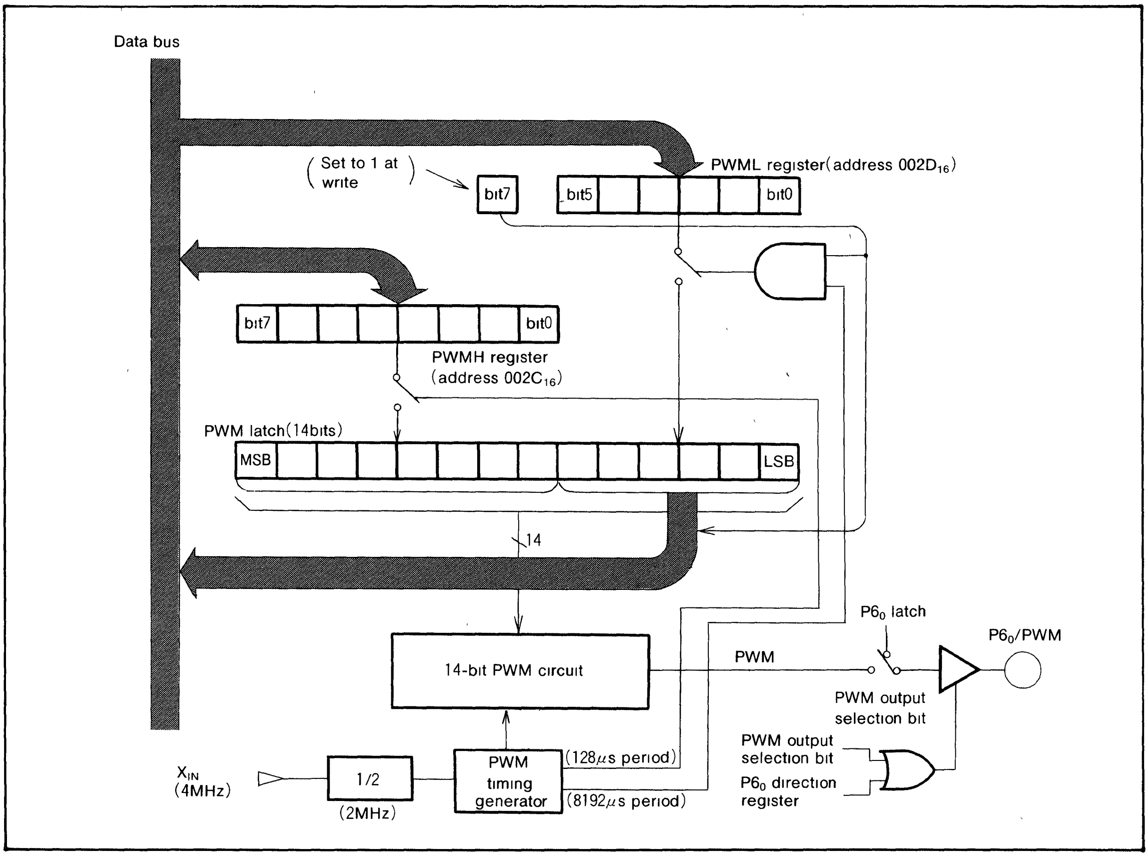


Fig. 21 PWM block diagram

(1) Data Set-up
The PWM output pin also functions as port $P6_0$. Set port $P6_0$ to be the PWM output pin by setting bit 0 of the PWM mode register (address $002B_{16}$). The upper eight bits of output data are set in the upper PWM register PWMH (address $002C_{16}$) and the lower six bits are set in the lower PWM register PWML (address $002D_{16}$).

(2) Transfer From Register to Latch
Data written to the PWML register is transferred to the PWM latch once in each PWM period (every 8192µs), and data written to the PWMH register is transferred to the PWM latch once in each sub-period (every 128µs). When the PWML register is read, the contents of the latch are read. However, bit 7 of the PWML register indicates whether the transfer to the PWM latch is completed; the transfer is completed when bit 7 is "0".

Table 4. Relationship between lower 6 bits of data and period set by the ADD bit

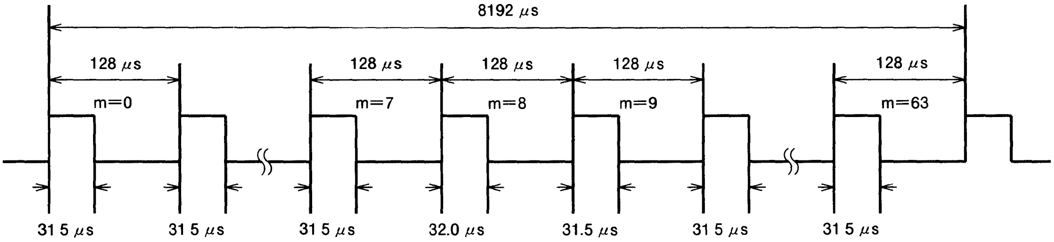
Lower 6 Bits of Data(PWML)	Sub-periods tm Lengthened (m =0 to 63)
0 0 0 0 0 0 (LSB)	None
0 0 0 0 0 1	m=32
0 0 0 0 1 0	m=16, 48
0 0 0 1 0 0	m= 8, 24, 40, 56
0 0 1 0 0 0	m= 4, 12, 20, 28, 36, 44, 52, 60
0 1 0 0 0 0	m= 2, 6, 10, 14, 18, 22, 26, 30, 34, 38, 42, 46, 50, 54, 58, 62
1 0 0 0 0 0	m= 1, 3, 5, 7, ························ ··, 57, 59, 61, 63

(3) PWM Operation
The timing of the 14-bit PWM function is shown in Fig. 24. The 14-bit PWM data is divided into the lower six bits and the upper eight bits in the PWM latch.

The upper eight bits of data determine how long an "H"-level signal is output during each sub-period. There are 64 sub-periods in each period, and each sub-period is 256× τ (128µs) long. The signal is "H" for a length equal to N times τ, where τ is the minimum resolution (500ns).

The contents of the lower six bits of data enable the lengthening of the high signal by τ (500ns). As shown in Fig. 21, the six bits of PWML determine which sub-cycles are lengthened.
As shown in Fig. 24, the leading edge of the pulse is lengthened. By changing the length of specific sub-periods instead of simply changing the "H" duration, an accurate waveform can be duplicated without the use of complex external filters.

For example, if the upper eight bits of the 14-bit data are 03_{16} and the lower six bits are 05_{16}, the length of the "H"-level output in sub-periods t_8, t_{24}, t_{32}, t_{40}, and t_{56} is 4 τ, and its length 3 τ in all other sub-periods.



Pulse width modulation register H : 00111111
Pulse width modulation register L : 000101
Sub-periods where "H" pulse width is 32 µs : m = 8, 24, 32, 40, 56
Sub-periods where "H" pulse width is 31 5 µs : m = all other values

Fig. 22 PWM timing

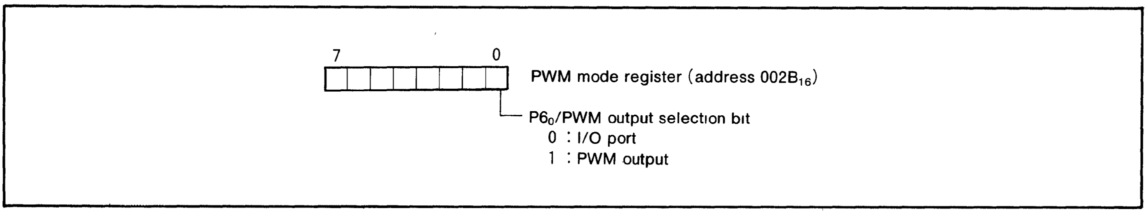


Fig. 23 Structure of PWM mode register

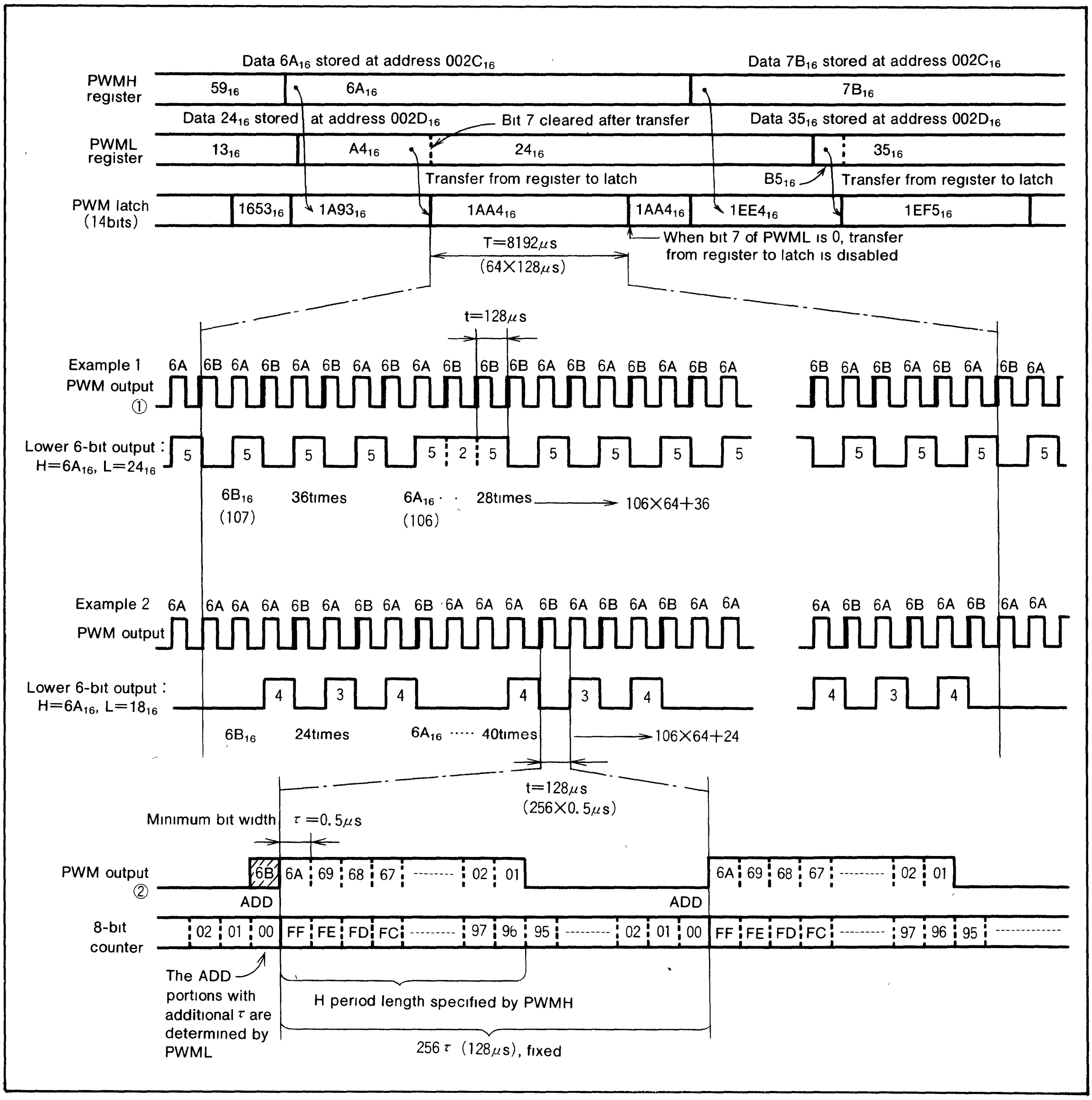


Fig. 24 14-bit PWM timing

A-D CONVERTER

The functional blocks of the A-D converter are described below.

〔A-D Conversion Register〕 AD

The A-D conversion register is a read-only register that contains the result of an A-D conversion. This register should not be read during an A-D conversion.

〔A-D Control Register〕 ADCON

The A-D control register controls the A-D conversion process. Bits 0 to 2 of this register select specific analog input pins. Bit 3 signals the completion of an A-D conversion. The value of this bit remains at "0" during an A-D conversion, then changes to "1" when the A-D conversion is completed. Writing "0" to this bit starts the A-D conversion.

〔Comparison Voltage Generator〕

The comparison voltage generator divides the voltage between AV_{SS} and V_{REF} by 256, and outputs the divided voltages.

〔Channel Selector〕

The channel selector selects one of the input ports $P7_7/AN_7$ to $P7_0/AN_0$

〔Comparator and Control Circuit〕

The comparator and control circuit compares an analog input voltage with the comparison voltage and stores the result in the A-D conversion register. When an A-D conversion is complete, the control circuit sets the A-D conversion completion bit and the A-D interrupt request bit to "1".

Note that the comparator is constructed linked to a capacitor, so set f (X_{IN}) to at least 500kHz during A-D conversion.

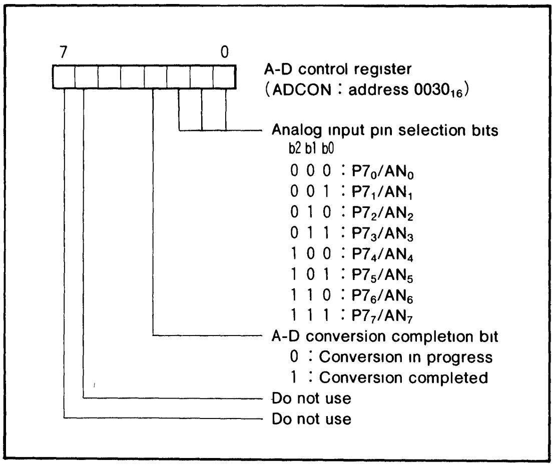


Fig. 25 Structure of A-D control register

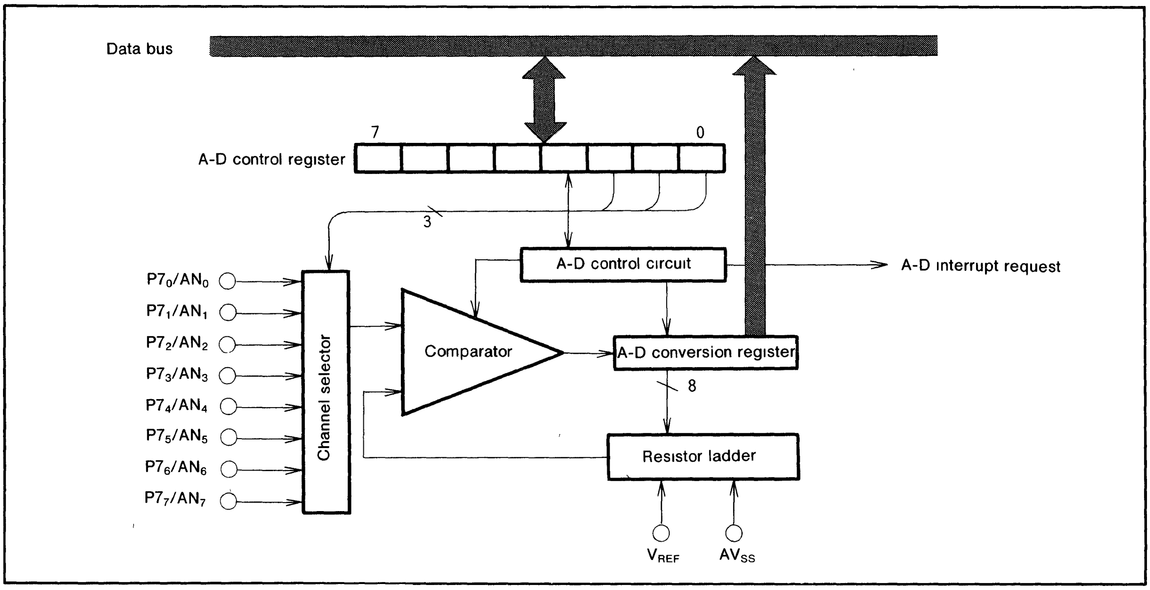


Fig. 26 A-D converter block diagram

FLD CONTROLLER

Microcomputers of the M3817x group have fluorescent display (FLD) drive and control circuits.

The FLD controller consists of the following components:

- 24 pins for segments
- 16 pins for digits
- FLDC mode register
- FLD data pointer
- FLD data pointer reload register
- Port P0 segment/digit switching register
- Port P1 digit/port switching register
- Port P8 segment/port switching register
- Key-scan blanking register
- 48-byte FLD automatic display RAM

Eight to twenty-four pins can be used as segment pins and four to sixteen pins can be used as digit pins.

Note that only 32 pins (maximum) can be used as segment and digit pins.

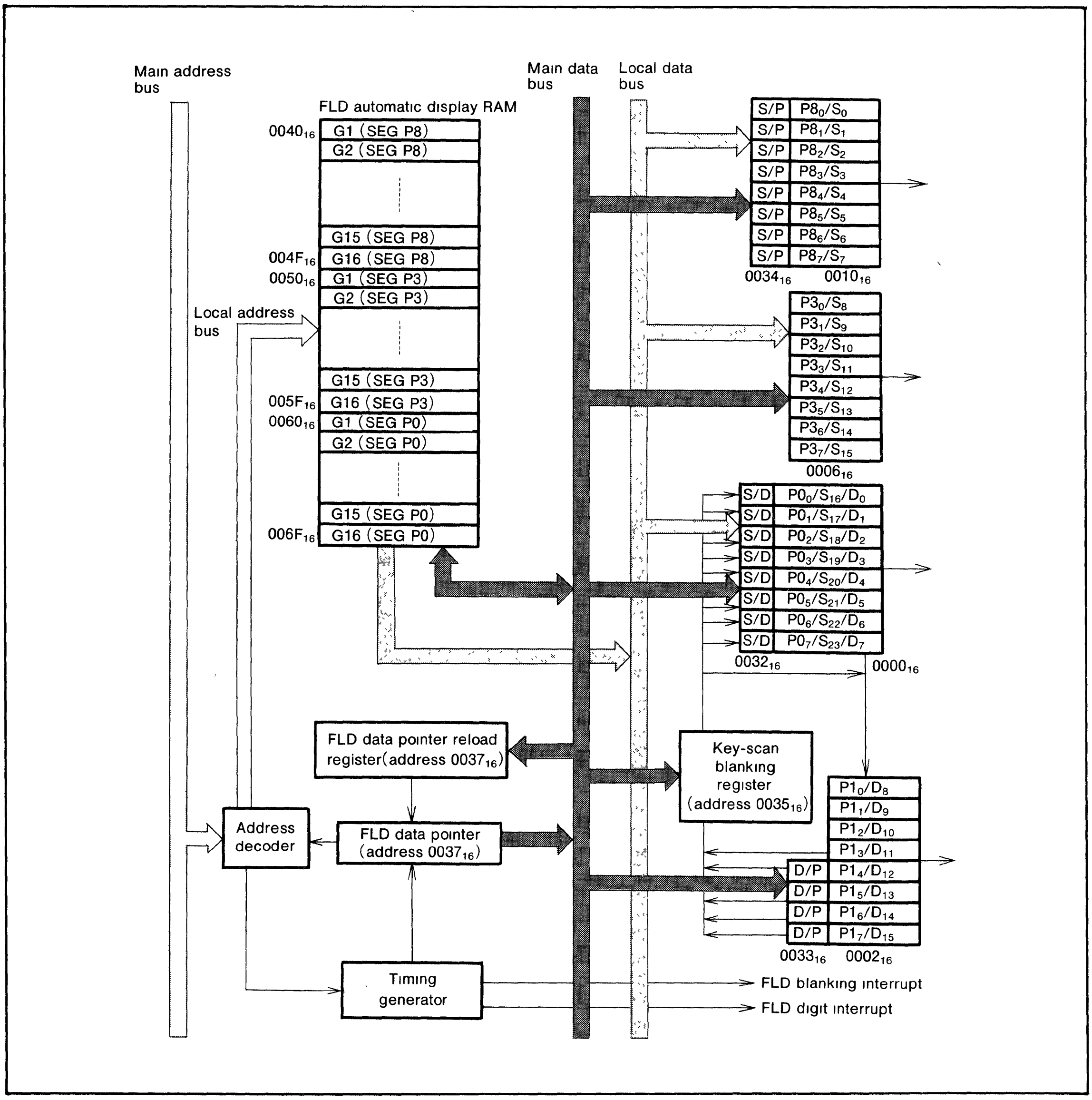


Fig. 27 FLD control circuit block diagram

FLDC Mode Register (FLDM)

The FLDC mode register (address 0036_{16}) is a seven bit control register which is used to control the FLD automatic display.

Key-scan Blanking Register (KSCN)

The key-scan blanking register (address 0035_{16}) is a two bit register which sets the blanking period T_{scan} between the last digit and the first digit of the next cycle.

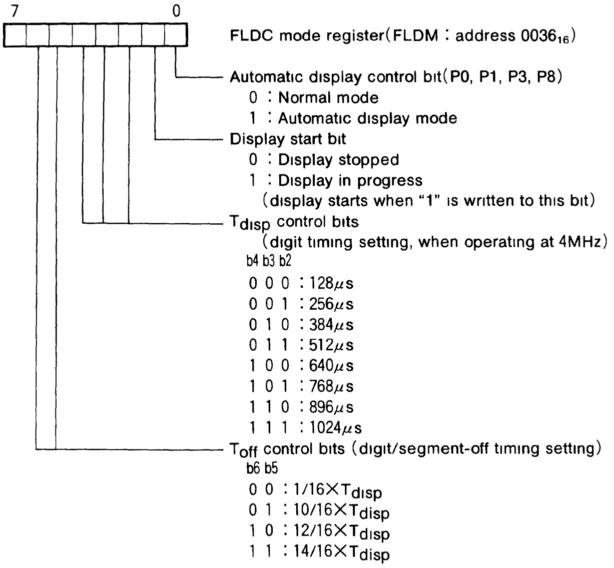


Fig. 28 Structure of FLDC mode register (FLDM)

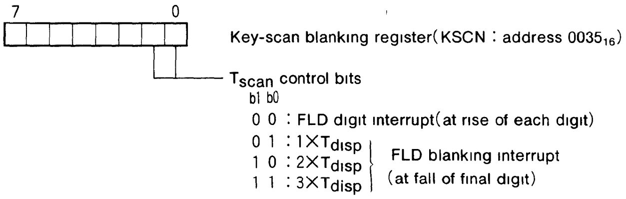


Fig. 29 Structure of key-scan blanking register (KSCN)

FLD Automatic Display Pins

The FLD automatic display function of Ports P0, P1, P3, and P8 is selected by setting the automatic display control bit of the FLDC mode register (address 0036_{16}) to "1".

When using the FLD automatic display mode, set the number of segments and digits for each port.

Table 5. Pins in FLD automatic display mode

Port Name	Automatic Display Pins	Setting Method
P8$_0$-P8$_7$	SEG$_0$-SEG$_7$ or P8$_0$-P8$_7$	The individual bits of the segment/port switching register (address 0034_{16}) can be used to set each pin to either segment ("1") or normal port input ("0") (Note)
P3$_0$-P3$_7$	SEG$_8$-SEG$_{15}$	None (segment only)
P0$_0$-P0$_7$	SEG$_{16}$-SEG$_{23}$ or DIG$_0$-DIG$_7$	The individual bits of the segment/digit switching register (address 0032_{16}) can be used to set each pin to segment ("1") or digit ("0") (Note)
P1$_0$-P1$_3$	DIG$_8$-DIG$_{11}$	None (digit only)
P1$_4$-P1$_7$	DIG$_{12}$-DIG$_{15}$ or P1$_4$-P1$_7$	The individual bits of the digit/port switching register (address 0033_{16}) can be used to set each pin to digit ("1") or normal port output ("0") (Note)

Note. Always set digits in sequence.

Number of segments		16		8		16		24		16
Number of digits		4		12		10		8		16
Port P8 (has segment/port switching register)	0	P8$_0$	0	P8$_0$	0	P8$_0$	1	SEG$_0$	1	SEG$_0$
	0	P8$_1$	0	P8$_1$	0	P8$_1$	1	SEG$_1$	1	SEG$_1$
	0	P8$_2$	0	P8$_2$	0	P8$_2$	1	SEG$_2$	1	SEG$_2$
	0	P8$_3$	0	P8$_3$	0	P8$_3$	1	SEG$_3$	1	SEG$_3$
	0	P8$_4$	0	P8$_4$	1	SEG$_4$	1	SEG$_4$	1	SEG$_4$
	0	P8$_5$	0	P8$_5$	1	SEG$_5$	1	SEG$_5$	1	SEG$_5$
	0	P8$_6$	0	P8$_6$	1	SEG$_6$	1	SEG$_6$	1	SEG$_6$
	0	P8$_7$	0	P8$_7$	1	SEG$_7$	1	SEG$_7$	1	SEG$_7$
Port P3 (segment only)		SEG$_8$		SEG$_8$		SEG$_8$		SEG$_8$		SEG$_8$
		SEG$_9$		SEG$_9$		SEG$_9$		SEG$_9$		SEG$_9$
		SEG$_{10}$		SEG$_{10}$		SEG$_{10}$		SEG$_{10}$		SEG$_{10}$
		SEG$_{11}$		SEG$_{11}$		SEG$_{11}$		SEG$_{11}$		SEG$_{11}$
		SEG$_{12}$		SEG$_{12}$		SEG$_{12}$		SEG$_{12}$		SEG$_{12}$
		SEG$_{13}$		SEG$_{13}$		SEG$_{13}$		SEG$_{13}$		SEG$_{13}$
		SEG$_{14}$		SEG$_{14}$		SEG$_{14}$		SEG$_{14}$		SEG$_{14}$
		SEG$_{15}$		SEG$_{15}$		SEG$_{15}$		SEG$_{15}$		SEG$_{15}$
Port P0 (has segment/digit switching register)	1	SEG$_{16}$	0	DIG$_0$ →G12	1	SEG$_{16}$	1	SEG$_{16}$	0	DIG$_0$ →G16
	1	SEG$_{17}$	0	DIG$_1$ →G11	1	SEG$_{17}$	1	SEG$_{17}$	0	DIG$_1$ →G15
	1	SEG$_{18}$	0	DIG$_2$ →G10	1	SEG$_{18}$	1	SEG$_{18}$	0	DIG$_2$ →G14
	1	SSG$_{19}$	0	DIG$_3$ →G9	1	SEG$_{19}$	1	SEG$_{19}$	0	DIG$_3$ →G13
	1	SEG$_{20}$	0	DIG$_4$ →G8	0	DIG$_4$ →G10	1	SEG$_{20}$	0	DIG$_4$ →G12
	1	SEG$_{21}$	0	DIG$_5$ →G7	0	DIG$_5$ →G9	1	SEG$_{21}$	0	DIG$_5$ →G11
	1	SEG$_{22}$	0	DIG$_6$ →G6	0	DIG$_6$ →G8	1	SEG$_{22}$	0	DIG$_6$ →G10
	1	SEG$_{23}$	0	DIG$_7$ →G5	0	DIG$_7$ →G7	1	SEG$_{23}$	0	DIG$_7$ →G9
Port P1 (has digit/port switching register)		DIG$_8$ →G4		DIG$_8$ →G4		DIG$_8$ →G6		DIG$_8$ →G8		DIG$_8$ →G8
		DIG$_9$ →G3		DIG$_9$ →G3		DIG$_9$ →G5		DIG$_9$ →G7		DIG$_9$ →G7
		DIG$_{10}$ →G2		DIG$_{10}$ →G2		DIG$_{10}$ →G4		DIG$_{10}$ →G6		DIG$_{10}$ →G6
		DIG$_{11}$ →G1		DIG$_{11}$ →G1		DIG$_{11}$ →G3		DIG$_{11}$ →G5		DIG$_{11}$ →G5
	0	P1$_4$	0	P1$_4$	1	DIG$_{12}$ →G2	1	DIG$_{12}$ →G4	1	DIG$_{12}$ →G4
	0	P1$_5$	0	P1$_5$	1	DIG$_{13}$ →G1	1	DIG$_{13}$ →G3	1	DIG$_{13}$ →G3
	0	P1$_6$	0	P1$_6$	0	P1$_6$	1	DIG$_{14}$ →G2	1	DIG$_{14}$ →G2
	0	P1$_7$	0	P1$_7$	0	P1$_7$	1	DIG$_{15}$ →G1	1	DIG$_{15}$ →G1

Fig. 30 Segment/digit setting example

FLD Automatic Display RAM

The FLD automatic display RAM area is the 48 bytes from address 0040$_{16}$ to 006F$_{16}$. The FLD automatic display RAM area can be used to store 3-byte data items for a maximum of 16 digits. Addresses 0040$_{16}$ to 004F$_{16}$ are used for P8 segment data, addresses 0050$_{16}$ to 005F$_{16}$ are used for P3 segment data, and addresses 0060$_{16}$ to 006F$_{16}$ are used for P0 segment data.

- **FLD Data Pointer and FLD Data Pointer Reload Register**
  The FLD data pointer indicates the data address in the FLD automatic display RAM to be transferred to a segment, and the FLD data pointer reload register indicates the address of the first digit of segment P3.

Both the FLD data pointer and the FLD data pointer reload register are allocated to address 0037$_{16}$ and are 6-bits wide. Data written to this address is written to the FLD data pointer reload register, data read from this address is read from the FLD data pointer

The actual memory address is the value of the data pointer plus 40$_{16}$, 50$_{16}$, or 60$_{16}$.

The contents of the FLD data pointer indicate the start address of segment P0 at the start of automatic display. If segment P0 or P3 data is transferred to the segment, the FLD data pointer returns − 16; if segment P8 data is transferred, it returns + 31. After it reaches "00", the value in the FLD data pointer reload register is transferred to the FLD data pointer. In this way, three bytes of data for the P0, P3, and P8 segments of one digit are transferred

Bit Address	7	6	5	4	3	2	1	0	
0040$_{16}$	SEG$_7$	SEG$_6$	SEG$_5$	SEG$_4$	SEG$_3$	SEG$_2$	SEG$_1$	SEG$_0$	← Final digit (final data of segment P8)
0041$_{16}$	SEG$_7$	SEG$_6$	SEG$_5$	SEG$_4$	SEG$_3$	SEG$_2$	SEG$_1$	SEG$_0$	
⋮	⋮			⋮					Segment P8 data area
004E$_{16}$	SEG$_7$	SEG$_6$	SEG$_5$	SEG$_4$	SEG$_3$	SEG$_2$	SEG$_1$	SEG$_0$	
004F$_{16}$	SEG$_7$	SEG$_6$	SEG$_5$	SEG$_4$	SEG$_3$	SEG$_2$	SEG$_1$	SEG$_0$	
0050$_{16}$	SEG$_{15}$	SEG$_{14}$	SEG$_{13}$	SEG$_{12}$	SEG$_{11}$	SEG$_{10}$	SEG$_9$	SEG$_8$	← Final digit (final data of segment P3)
0051$_{16}$	SEG$_{15}$	SEG$_{14}$	SEG$_{13}$	SEG$_{12}$	SEG$_{11}$	SEG$_{10}$	SEG$_9$	SEG$_8$	
⋮	⋮			⋮					Segment P3 data area
005E$_{16}$	SEG$_{15}$	SEG$_{14}$	SEG$_{13}$	SEG$_{12}$	SEG$_{11}$	SEG$_{10}$	SEG$_9$	SEG$_8$	
005F$_{16}$	SEG$_{15}$	SEG$_{14}$	SEG$_{13}$	SEG$_{12}$	SEG$_{11}$	SEG$_{10}$	SEG$_9$	SEG$_8$	
0060$_{16}$	SEG$_{23}$	SEG$_{22}$	SEG$_{21}$	SEG$_{20}$	SEG$_{19}$	SEG$_{18}$	SEG$_{17}$	SEG$_{16}$	← Final digit (final data of segment P0)
0061$_{16}$	SEG$_{23}$	SEG$_{22}$	SEG$_{21}$	SEG$_{20}$	SEG$_{19}$	SEG$_{18}$	SEG$_{17}$	SEG$_{16}$	
⋮	⋮			⋮					Segment P0 data area
006E$_{16}$	SEG$_{23}$	SEG$_{22}$	SEG$_{21}$	SEG$_{20}$	SEG$_{19}$	SEG$_{18}$	SEG$_{17}$	SEG$_{16}$	
006F$_{16}$	SEG$_{23}$	SEG$_{22}$	SEG$_{21}$	SEG$_{20}$	SEG$_{19}$	SEG$_{18}$	SEG$_{17}$	SEG$_{16}$	

Fig. 31 FLD automatic display RAM and bit allocation

- **Data Setup**

When data is stored in the FLD automatic display RAM, the end of segment P8 data is stored at address 0040_{16}, the end of segment P3 data is stored at address 0050_{16}, and the end of segment P0 data is stored at address 0060_{16}. The head of each of the segment P8, P3, and P0 data is stored at an address that is the number of digits−1 away from the corresponding address 0040_{16}, 0050_{16}, 0060_{16}.

Set the FLD data pointer reload register to the value given by the number of digits−1. "1" is always written to bit 5, and "0" is always written to bit 4. Note that "0" is always read from bit 5 or 4 during a read.

For 17 segments and 15 digits
(FLD data pointer reload register=14)

Bit Address	7	6	5	4	3	2	1	0
0040_{16}	▨	▨	▨	▨	▨	▨	▨	▨
0041_{16}	▨	▨	▨	▨	▨	▨	▨	▨
0042_{16}	▨	▨	▨	▨	▨	▨	▨	▨
0043_{16}	▨	▨	▨	▨	▨	▨	▨	▨
0044_{16}	▨	▨	▨	▨	▨	▨	▨	▨
0045_{16}	▨	▨	▨	▨	▨	▨	▨	▨
0046_{16}	▨	▨	▨	▨	▨	▨	▨	▨
0047_{16}	▨	▨	▨	▨	▨	▨	▨	▨
0048_{16}	▨	▨	▨	▨	▨	▨	▨	▨
0049_{16}	▨	▨	▨	▨	▨	▨	▨	▨
$004A_{16}$	▨	▨	▨	▨	▨	▨	▨	▨
$004B_{16}$	▨	▨	▨	▨	▨	▨	▨	▨
$004C_{16}$	▨	▨	▨	▨	▨	▨	▨	▨
$004D_{16}$	▨	▨	▨	▨	▨	▨	▨	▨
$004E_{16}$	▨	▨	▨	▨	▨	▨	▨	▨
$004F_{16}$								
0050_{16}	▨	▨	▨	▨	▨	▨	▨	▨
0051_{16}	▨	▨	▨	▨	▨	▨	▨	▨
0052_{16}	▨	▨	▨	▨	▨	▨	▨	▨
0053_{16}	▨	▨	▨	▨	▨	▨	▨	▨
0054_{16}	▨	▨	▨	▨	▨	▨	▨	▨
0055_{16}	▨	▨	▨	▨	▨	▨	▨	▨
0056_{16}	▨	▨	▨	▨	▨	▨	▨	▨
0057_{16}	▨	▨	▨	▨	▨	▨	▨	▨
0058_{16}	▨	▨	▨	▨	▨	▨	▨	▨
0059_{16}	▨	▨	▨	▨	▨	▨	▨	▨
$005A_{16}$	▨	▨	▨	▨	▨	▨	▨	▨
$005B_{16}$	▨	▨	▨	▨	▨	▨	▨	▨
$005C_{16}$	▨	▨	▨	▨	▨	▨	▨	▨
$005D_{16}$	▨	▨	▨	▨	▨	▨	▨	▨
$005E_{16}$	▨	▨	▨	▨	▨	▨	▨	▨
$005F_{16}$								
0060_{16}								▨
0061_{16}								▨
0062_{16}								▨
0063_{16}								▨
0064_{16}								▨
0065_{16}								▨
0066_{16}								▨
0067_{16}								▨
0068_{16}								▨
0069_{16}								▨
$006A_{16}$								▨
$006B_{16}$								▨
$006C_{16}$								▨
$006D_{16}$								▨
$006E_{16}$								▨
$006F_{16}$								

For 24 segments and 8 digits
(FLD data pointer reload register=7)

Bit Address	7	6	5	4	3	2	1	0
0040_{16}	▨	▨	▨	▨	▨	▨	▨	▨
0041_{16}	▨	▨	▨	▨	▨	▨	▨	▨
0042_{16}	▨	▨	▨	▨	▨	▨	▨	▨
0043_{16}	▨	▨	▨	▨	▨	▨	▨	▨
0044_{16}	▨	▨	▨	▨	▨	▨	▨	▨
0045_{16}	▨	▨	▨	▨	▨	▨	▨	▨
0046_{16}	▨	▨	▨	▨	▨	▨	▨	▨
0047_{16}	▨	▨	▨	▨	▨	▨	▨	▨
0048_{16}								
0049_{16}								
$004A_{16}$								
$004B_{16}$								
$004C_{16}$								
$004D_{16}$								
$004E_{16}$								
$004F_{16}$								
0050_{16}	▨	▨	▨	▨	▨	▨	▨	▨
0051_{16}	▨	▨	▨	▨	▨	▨	▨	▨
0052_{16}	▨	▨	▨	▨	▨	▨	▨	▨
0053_{16}	▨	▨	▨	▨	▨	▨	▨	▨
0054_{16}	▨	▨	▨	▨	▨	▨	▨	▨
0055_{16}	▨	▨	▨	▨	▨	▨	▨	▨
0056_{16}	▨	▨	▨	▨	▨	▨	▨	▨
0057_{16}	▨	▨	▨	▨	▨	▨	▨	▨
0058_{16}								
0059_{16}								
$005A_{16}$								
$005B_{16}$								
$005C_{16}$								
$005D_{16}$								
$005E_{16}$								
$005F_{16}$								
0060_{16}	▨	▨	▨	▨	▨	▨	▨	▨
0061_{16}	▨	▨	▨	▨	▨	▨	▨	▨
0062_{16}	▨	▨	▨	▨	▨	▨	▨	▨
0063_{16}	▨	▨	▨	▨	▨	▨	▨	▨
0064_{16}	▨	▨	▨	▨	▨	▨	▨	▨
0065_{16}	▨	▨	▨	▨	▨	▨	▨	▨
0066_{16}	▨	▨	▨	▨	▨	▨	▨	▨
0067_{16}	▨	▨	▨	▨	▨	▨	▨	▨
0068_{16}								
0069_{16}								
$006A_{16}$								
$006B_{16}$								
$006C_{16}$								
$006D_{16}$								
$006E_{16}$								
$006F_{16}$								

Note. ▨ Shaded areas are not used

Fig. 32 Example of using the FLD automatic display RAM.

- **Timing Setting**

The digit timing (T_{disp}) and digit/segment turn-off timing (T_{off}) can be set by the FLDC mode register (address 0036_{16}). The scan timing (T_{scan}) can be set by the key-scan blanking register (address 0035_{16}).

Note that flickering will occur if the repetition frequency ($1/(T_{disp}\times$number of digits$+T_{scan}))$ is an integral multiple of the digit timing T_{disp}.

- **FLD Start**

To perform FLD automatic display, you have to use the following registers.

- Port P0 segment/digit switching register
- Port P1 digit/port switching register
- Port P8 segment/port switching register
- Key-scan blanking register
- FLDC mode register
- FLD data pointer

Automatic display mode is activated by writing “1” to bit 0 of the FLDC mode register (address 0036_{16}), and the automatic display is started by writing “1” to bit 1.

During automatic display bit 1 always keeps “1”, automatic display can be interrupted by writing “0” to bit 1.

If key-scan is to be performed by segment during the key-scan blanking period T_{scan},

1. Write “0” to bit 0 (automatic display control bit) of FLDC mode register (address 0036_{16}).
2. Set the port corresponding to the segment to the normal port.
3. After the key-scan is performed, write “1” (automatic display mode) to bit 0 of FLDC mode register (address 0036_{16}).

Note on performance of key-scan in the above 1 to 3 order.

1. Do not write “0” to bit 1 of FLDC mode register (address 0036_{16}).
2. Do not write “1” to the port corresponding to the digit.

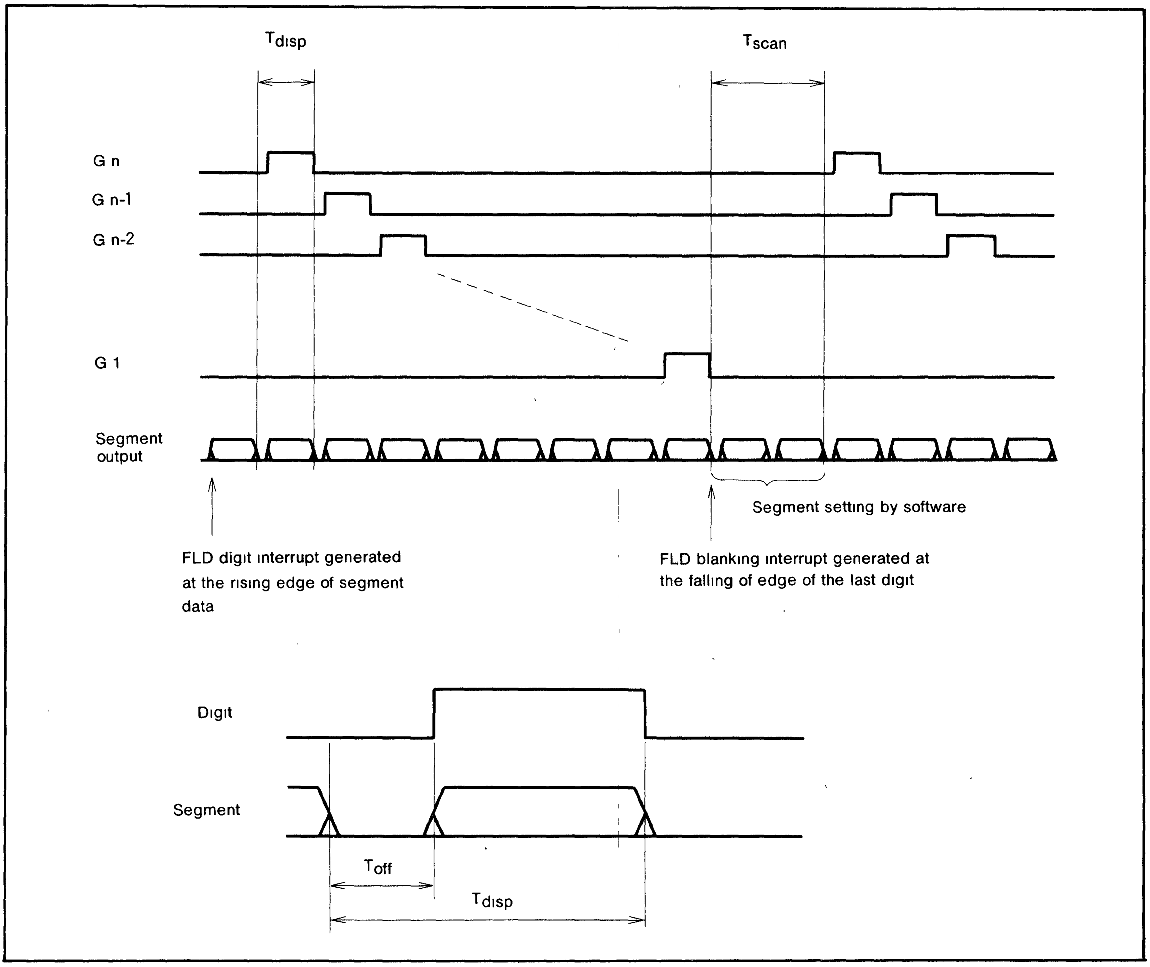
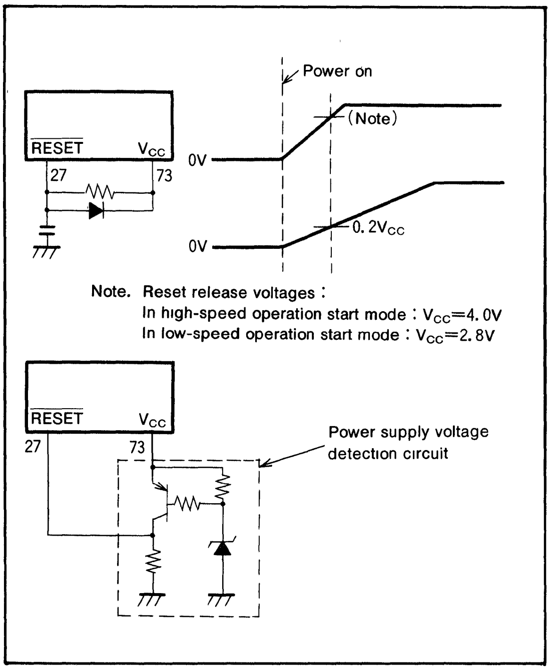


Fig. 33 FLDC timing

RESET CIRCUIT

After a reset, the microcomputer will start in high-speed operation start mode or low-speed operation start mode depending on a mask-programmable option.

- **High-Speed Operation Start Mode**
  In high-speed operation start mode, reset occurs if the $\overline{\text{RESET}}$ pin is held at an "L" level for at least 2μs then is returned to an "H" level (the power supply voltage should be between 4.0V and 5.5V). Both the X_{IN} and the X_{CIN} clocks begin oscillating. In order to give the X_{IN} clock time to stabilize, internal operation does not begin until after 13 X_{IN} clock cycles are complete. After the reset is completed, the program starts from the address contained in address $FFFD_{16}$ (upper byte) and address $FFFC_{16}$ (lower byte).
- **Low-Speed Operation Start Mode**
  In low-speed operation start mode, reset occurs if the $\overline{\text{RESET}}$ pin is held at a "L" level for at least 2μs then is returned to an "H" level (the power supply voltage should be between 2.8V and 5.5V). The X_{IN} clock does not begin oscillating. In order to give the X_{CIN} time to stabilize, timer 1 and timer 2 are connected together and 512 cycles of the $X_{CIN}/16$ are counted before internal operation begins. After the reset is completed, the program starts from the address contained in address $FFFD_{16}$ (upper byte) and address $FFFC_{16}$ (lower byte).
  If the X_{CIN} clock is stable, reset will complete after approximately 250ms (assuming $f(X_{CIN})=32.768kHz$).
  Immediately after a power-on, the stability of the clock circuit will determine the reset timing and will vary according to the characteristics of the oscillation circuit used.
- **Note on Use**
  Make sure that the reset input voltage is no more than 0.8V in high-speed operation start mode, or no more than 0.5V in low-speed operation start mode.



Note. Reset release voltages :
In high-speed operation start mode : V_{CC}=4. 0V
In low-speed operation start mode : V_{CC}=2. 8V

Fig. 34 Power-on reset circuit example

		Address	Register contents
(1)	Port P0 register	(0000_{16})…	00_{16}
(2)	Port P1 register	(0002_{16})…	00_{16}
(3)	Port P2 register	(0004_{16})…	00_{16}
(4)	Port P2 direction register	(0005_{16})…	00_{16}
(5)	Port P3 register	(0006_{16})…	00_{16}
(6)	Port P4 register	(0008_{16})…	00_{16}
(7)	Port P4 direction register	(0009_{16})…	00_{16}
(8)	Port P5 register	($000A_{16}$)…	00_{16}
(9)	Port P5 direction register	($000B_{16}$)…	00_{16}
(10)	Port P6 register	($000C_{16}$)…	00_{16}
(11)	Port P6 direction register	($000D_{16}$)…	00_{16}
(12)	Port P7 register	($000E_{16}$)…	00_{16}
(13)	Port P7 direction register	($000F_{16}$)…	00_{16}
(14)	Port P8 register	(0010_{16})…	00_{16}
(15)	Port P8 direction register	(0011_{16})…	00_{16}
(16)	Serial I/O1 control register	(0019_{16})…	00_{16}
(17)	Serial I/O automatic transfer control register	($001A_{16}$)…	00_{16}
(18)	Serial I/O automatic transfer interval register	($001C_{16}$)…	00_{16}
(19)	Serial I/O2 control register	($001D_{16}$)…	00_{16}
(20)	Timer 1 register	(0020_{16})…	FF_{16}
(21)	Timer 2 register	(0021_{16})…	01_{16}
(22)	Timer 3 register	(0022_{16})…	FF_{16}
(23)	Timer 4 register	(0023_{16})…	FF_{16}
(24)	Timer 5 register	(0024_{16})…	FF_{16}
(25)	Timer 6 register	(0025_{16})…	FF_{16}
(26)	Timer 12 mode register	(0028_{16})…	00_{16}
(27)	Timer 34 mode register	(0029_{16})…	00_{16}
(28)	Timer 56 mode register	($002A_{16}$)…	00_{16}
(29)	PWM control register	($002B_{16}$)…	00_{16}
(30)	A-D control register	(0030_{16})…	08_{16}
(31)	Port P0 segment/digit switching register	(0032_{16})…	00_{16}
(32)	Port P1 digit/port switching register	(0033_{16})…	00_{16}
(33)	Port P8 segment/port switching register	(0034_{16})…	00_{16}
(34)	Key-scan blanking register	(0035_{16})…	00_{16}
(35)	FLDC mode register	(0036_{16})…	00_{16}
(36)	High-breakdown-voltage port control register	(0038_{16})…	00_{16}
(37)	Interrupt edge selection register	($003A_{16}$)…	00_{16}
(38)	CPU mode register	($003B_{16}$)…	* * 1 0 0 0 0 0
(39)	Interrupt request register 1	($003C_{16}$)…	00_{16}
(40)	Interrupt request register 2	($003D_{16}$)…	00_{16}
(41)	Interrupt control register 1	($003E_{16}$)…	00_{16}
(42)	Interrupt control register 2	($003F_{16}$)…	00_{16}
(43)	Processor status register	(PS)…	X X X X X 1 X X
(44)	Program counter	(PC_H)…	Contents of address $FFFD_{16}$
		(PC_L)…	Contents of address $FFFC_{16}$

Note. * : The initial values of bits 7 and 6 of the CPU mode register are determined by a mask option
X : Underfined
The contents of all other registers and RAM are undefined after a reset, so programs must set their initial values

Fig. 35 Internal status at reset

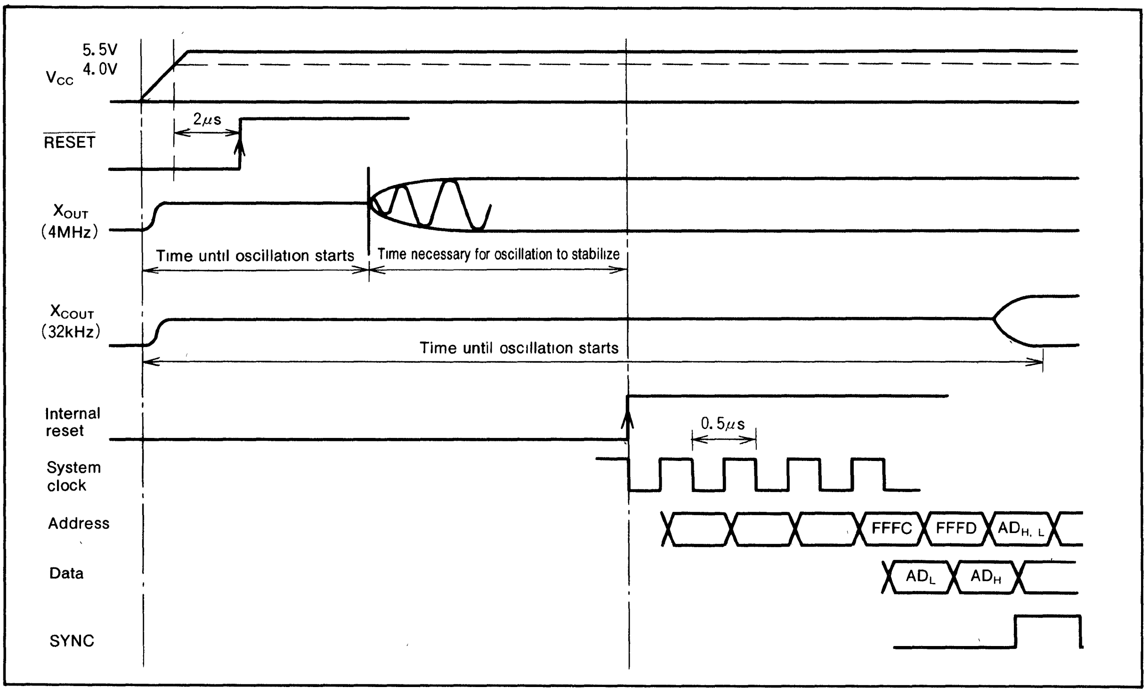


Fig. 36 Reset sequence in high-speed operation mode

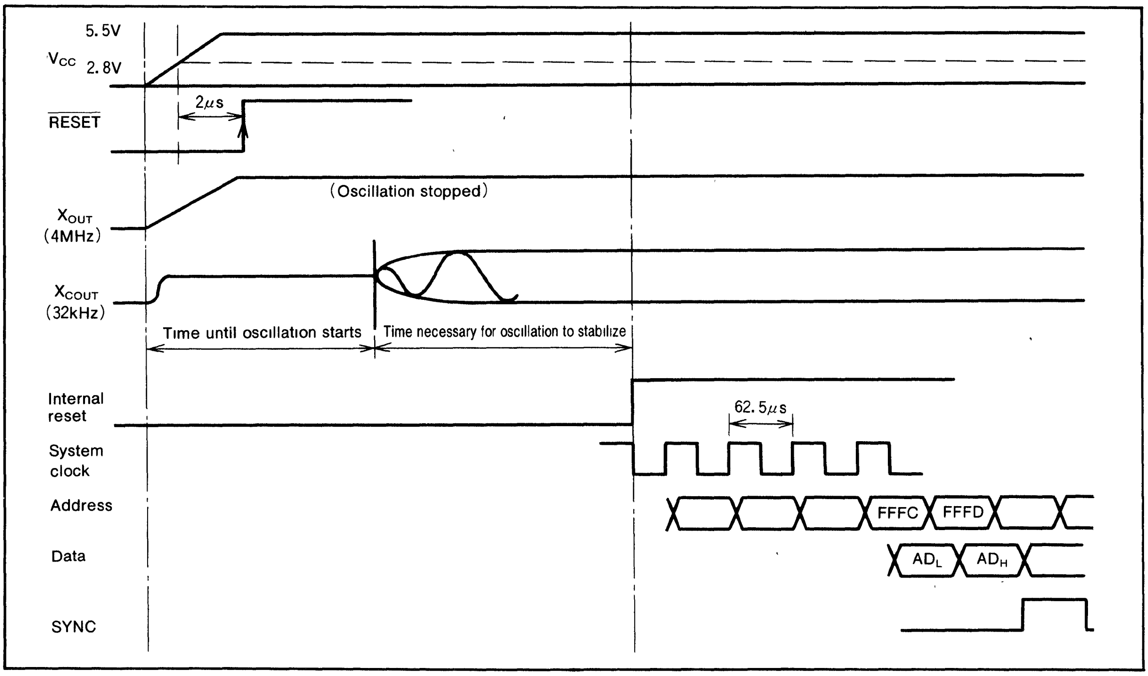


Fig. 37 Reset sequence in low-speed operation mode

CLOCK GENERATION CIRCUIT

When using an external clock signal, input the clock signal to the X_{IN} (X_{CIN}) pin and leave the X_{OUT} (X_{COUT}) pin open. If the X_{CIN} clock is not used, connect the X_{CIN} pin to V_{SS}, and leave the X_{COUT} pin open.

Either high-speed operation start mode or low-speed operation start mode can be selected by using a mask option.

- **High-Speed Operation Start Mode**
  After reset has completed, the internal clock ϕ is half the frequency of X_{IN}. Immediately after power-on, both the X_{IN} and X_{CIN} clock start oscillating. To set the internal clock ϕ to low-speed operation mode, set bit 7 of the CPU mode register (address $003B_{16}$) to "1".
- **Low-Speed Operation Start Mode**
  After reset has completed, the internal clock ϕ is half the frequency of X_{CIN}. Immediately after power-on, only the X_{CIN} clock starts oscillating. To set the internal clock ϕ to high-speed operation mode, first set bit 6 (CM_6) of the CPU mode register (address $003B_{16}$) to "0", the set bit 7 (CM_7) to "0". Note that the program must allow time for oscillation to stabilize.
- **Oscillation Control**

Stop Mode

If the STP instruction is executed, oscillation stops with the internal clock ϕ at an "H" level. Timer 1 is set to "FF_{16}" and timer 2 is set to "01_{16}".

Either X_{IN} or X_{CIN} divided by 16 is input to timer 1, and the output of timer 1 is connected to timer 2. The timer 1 and timer 2 interrupt enable bits must be set to disabled ("0"), so a program must set these bits before executing a STP instruction. Oscillation restarts at reset or when an external interrupt is received, but the internal clock ϕ is not supplied to the CPU until timer 2 overflows. This allows time for the clock circuit oscillation to stabilize.

Wait Mode

If the WIT instruction is executed, the internal clock ϕ stops at a "H" level but the oscillator itself does not stop. The internal clock restarts if a reset occurs or when an interrupt is received. Since the oscillator does not stop, normal operation can be started immediately after the clock is restarted.

Low-Speed Mode

If the internal clock is generated from the sub clock (X_{CIN}), a low power consumption operation can be entered by stopping only the main clock X_{IN}. To stop the main clock, set bit 6 (CM_6) of the CPU mode register ($003B_{16}$) to "1". When the main clock X_{IN} is restarted, the program must allow enough time to for oscillation to stabilize.

Note that in low-power-consumption mode the X_{CIN}-X_{COUT} drive performance can be reduced, allowing even lower power consumption (20μA with X_{CIN}= 32kHz). To reduce the X_{CIN}-X_{COUT} drive performance, clear bit 5 (CM_5) of the CPU mode register ($003B_{16}$) to "0". At reset or when a STP instruction is executed, this bit is set to "1" and strong drive is selected to help the oscillation to start.

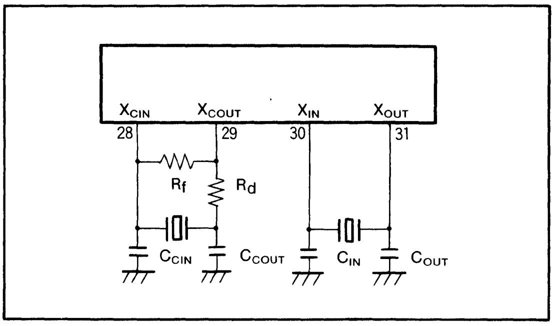


Fig. 38 Ceramic resonator circuit

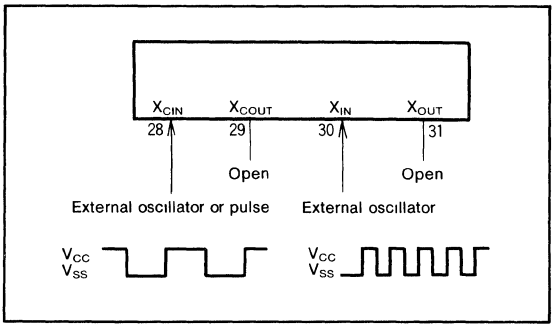
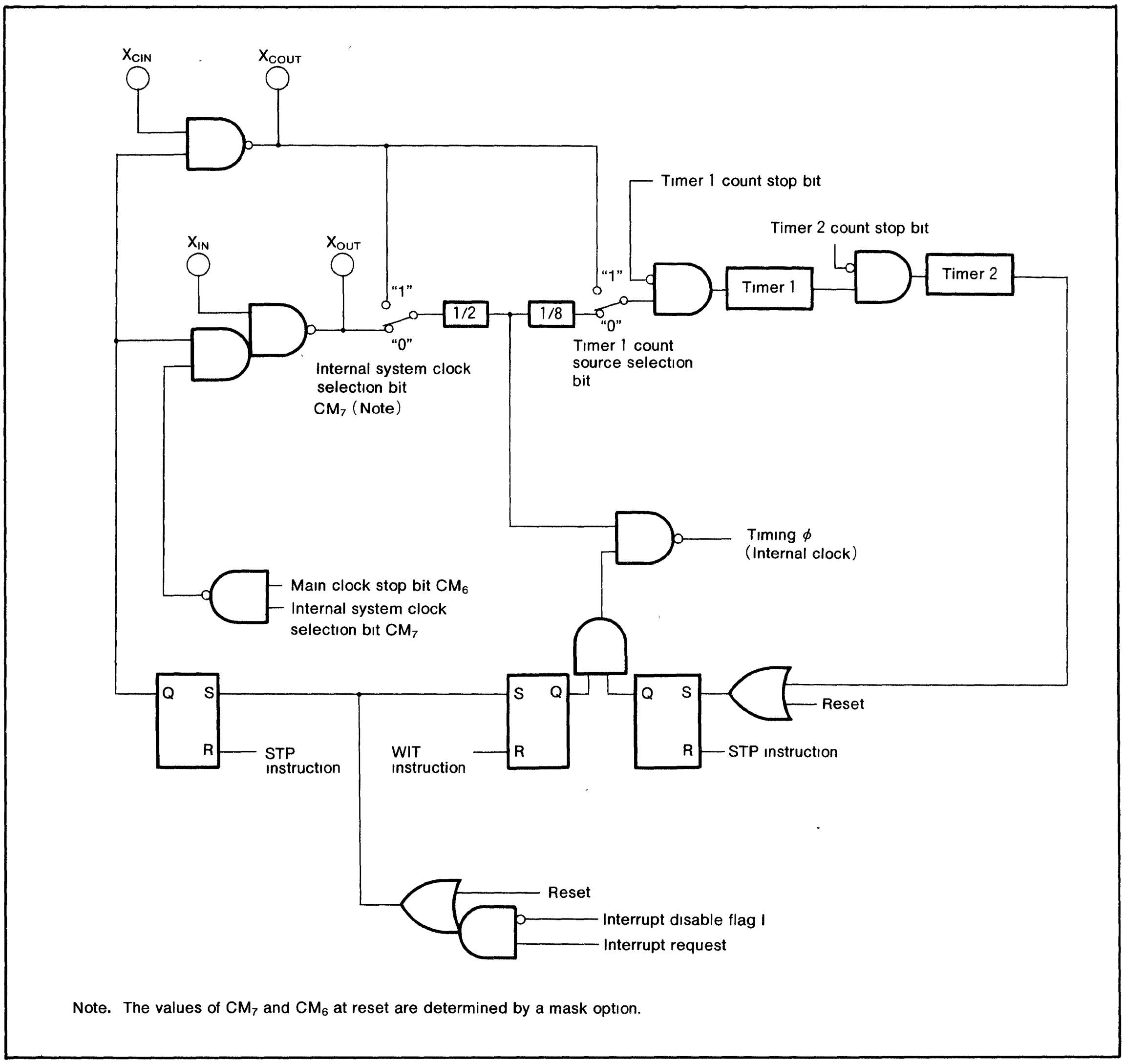
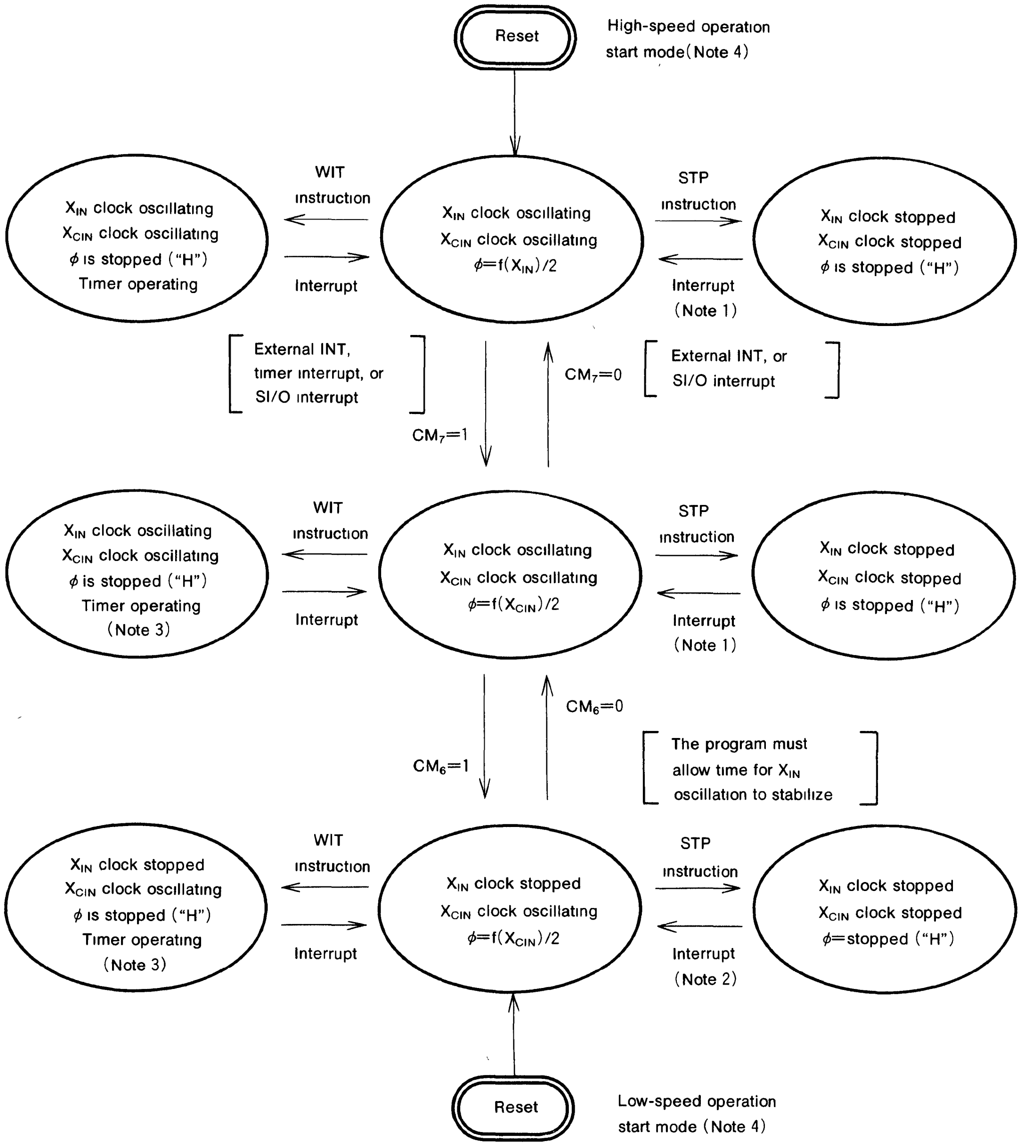


Fig. 39 External clock input circuit



Note. The values of CM_7 and CM_6 at reset are determined by a mask option.

Fig. 40 System clock generation circuit block diagram



The example assumes that 6.3MHz is being applied to the X_{IN} pin and 32kHz to the X_{CIN} pin

Note 1. When the STP state is ended, a delay of approximately 1.3ms is automatically generated by timer 1 and timer 2
2. The delay after the STP state ends is approximately 0.25s
3. If the internal clock ϕ divided by 8 is used as the timer count source, the frequency of the count source is f(X_{CIN})/16
4. Specify this option when ordering a mask ROM version

Fig. 41 State transitions of system clock

NOTES ON PROGRAMMING

- **Processor Status Register**

  The contents of the processor status register (PS) after a reset are undefined, except for the interrupt disable flag (I) which is "1". Therefore, flags that affect program execution must be initialized after a reset. In particular, it is essential to initialize the T and D flags because of their effect on calculations.

- **Interrupts**

  The contents of the interrupt request bits do not change immediately after they have been written.

  After writing to an interrupt request register, execute at least one instruction before performing a BBC or BBS instruction.

- **Decimal Calculations**

  To calculate in decimal notation, set the decimal mode flag (D) to "1", then execute a ADC or SBC instruction. Only the ADC and SBC instruction yield proper decimal results. After executing an ADC or SBC instruction, execute at least one instruction before executing a SEC, CLC, or CLD instruction.

  In decimal mode, the values of the negative (N), overflow (V), and zero (Z) flags are invalid.

  The carry flag can be used to indicate whether a carry or borrow has occurred, but must be initialized before each calculation. Clear the carry flag before an ADC and set the flag before an SBC.

- **Timers**

  If a value n (between 0 and 255) is written to a timer latch, the frequency division ratio is 1/(n+1).

- **Multiplication and Division Instructions**

  The MUL and DIV instructions do not affect the T and D flags.

  The execution of these instructions does not change the contents of the processor status register.

- **Ports**

  The contents of the port direction registers cannot be read. Programs can not use the value of a direction register as an index, or bit-test a direction register (BBC or BBS), or perform a read-modify-write instruction such as ROR, CLB, or SEB. Use instructions such as LDM and STA to set the port direction registers.

- **Serial I/O**

  When using an external clock, input "H" to the external clock input pin and clear the serial I/O interrupt request bit before executing a serial I/O transfer.

  When using the internal clock, set the synchronization clock to internal clock, then clear the serial I/O interrupt request bit before executing a serial I/O transfer.

- **Instruction Execution Timing**

  The instruction execution time is obtained by multiplying the frequency of the internal clock ϕ by the number of cycles needed to execute an instruction.

  The number of cycles required to execute an instruction is shown in the list of machine instructions.

  The frequency of the internal clock ϕ is half of the X_{IN} or X_{CIN} frequency.

DATA REQUIRED FOR MASK ORDERS

The following are necessary when ordering a mask ROM production:

(1) Mask ROM Order Confirmation Form
(2) Mark Specification Form
(3) Data to be written to ROM, in EPROM form (three identical copies)

If required, specify the following option on the Mask Confirmation Form:

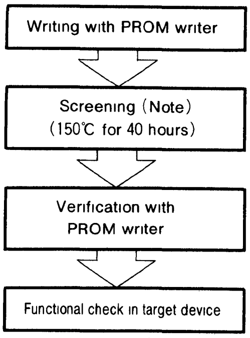
- Operation start mode switching option

ROM Writing Method

The built-in PROM of the blank one-time programmable version and built-in EPROM version can be read from and written to with an normal EPROM writer using a special write adapter.

Package	Name of Write Adapter
80P6N	PCA4738F-80
80D0	PCA4738L-80

The PROM of the blank one-time programmable version is not tested or screened after assembly. To ensure proper operation after writing, the procedure shown in Figure 42 is recommended to verify programming.



Note. The screening temperature is far higher than the storage temperature Do not leave the microcomputer at 150℃ for longer than 100 hours

Fig. 42 Writing and testing of one-time programmable version

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	All voltages measured based on the V_{SS} pin Output transistors are isolated	−0.3 to 7.0	V
V_{EE}	Pull-down power supply voltage		V_{CC}−40 to V_{CC}+0.3	V
V_I	Input voltage $P2_0$-$P2_7$, $P4_1$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_5$, $P7_0$-$P7_2$		−0.3 to V_{CC}+0.3	V
V_I	Input voltage $P4_0$		−0.3 to V_{CC}+0.3	V
V_I	Input voltage $P8_0$-$P8_7$		V_{CC}−40 to V_{CC}+0.3	V
V_I	Input voltage $\overline{\text{RESET}}$, X_{IN}		−0.3 to V_{CC}+0.3	V
V_I	Input voltage X_{CIN}		−0.3 to V_{CC}+0.3	V
V_O	Output voltage $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P3_0$-$P3_7$, $P8_0$-$P8_7$		V_{CC}−40 to V_{CC}+0.3	V
V_O	Output voltage $P2_4$-$P2_7$, $P4_1$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_5$, $P7_0$-$P7_7$, X_{OUT}, X_{COUT}		−0.3 to V_{CC}+0.3	V
P_d	Power dissipation	T_a = 25℃	600	mW
T_{opr}	Operating temperature		−10 to 85	℃
T_{stg}	Storage temperature		−40 to 125	℃

RECOMMENDED OPERATING CONDITIONS (V_{CC} = 4.0 to 5.5V, T_a = −10 to 85℃, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max.	
V_{CC}	Supply voltage	High-speed operation mode	4.0	5.0	5.5	V
		Low-speed operation mode	2.8	5.0	5.5	
V_{SS}	Supply voltage			0		V
V_{EE}	Pull-down power supply voltage		V_{CC}−38		V_{CC}	V
V_{REF}	Reference input voltage		2		V_{CC}	V
AV_{SS}	Analog power voltage			0		V
V_{IA}	Analog input voltage		0		V_{CC}	V
V_{IH}	"H" input voltage $P2_0$-$P2_7$		0.4V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage $P4_0$		0.75V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage $P4_1$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_5$, $P7_0$-$P7_7$		0.75V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage $P8_0$-$P8_7$		0.8V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage $\overline{\text{RESET}}$		0.8V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage X_{IN}, X_{CIN}		0.8V_{CC}		V_{CC}	V
V_{IL}	"L" input voltage $P2_4$-$P2_7$		0		0.16V_{CC}	V
V_{IL}	"L" input voltage $P4_0$		0		0.25V_{CC}	V
V_{IL}	"L" input voltage $P4_1$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_5$, $P7_0$-$P7_7$		0		0.25V_{CC}	V
V_{IL}	"L" input voltage $P8_0$-$P8_7$		0		0.2V_{CC}	V
V_{IL}	"L" input voltage $\overline{\text{RESET}}$		0		0.2V_{CC}	V
V_{IL}	"L" input voltage X_{IN}, X_{CIN}		0		0.2V_{CC}	V

RECOMMENDED OPERATING CONDITIONS (V_{CC}=4.0 to 5.5V, T_a=−10 to 85℃, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
$\Sigma I_{OH(peak)}$	"H" total peak output current $P0_0$-$P0_7$, $P1_0$-$P1_7$, (Note 1) $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P8_0$-$P8_7$			−240	mA
$\Sigma I_{OH(peak)}$	"H" total peak output current $P4_1$-$P4_7$, $P6_0$-$P6_5$, $P7_0$-$P7_7$			−60	mA
$\Sigma I_{OL(peak)}$	"L" total peak output current $P2_4$-$P2_7$, $P4_1$-$P4_7$, $P5_0$-$P5_7$, $P6_1$-$P6_5$, $P7_0$-$P7_7$			100	mA
$\Sigma I_{OL(peak)}$	"L" total peak output current $P6_0$			3.0	mA
$\Sigma I_{OH(avg)}$	"H" total average output current $P0_0$-$P0_7$, $P1_0$-$P1_7$, (Note 1) $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P8_0$-$P8_7$			−120	mA
$\Sigma I_{OH(avg)}$	"H" total average output current $P4_1$-$P4_7$, $P6_0$-$P6_5$			−30	mA
$\Sigma I_{OL(avg)}$	"L" total average output current $P2_0$-$P2_7$, $P4_1$-$P4_7$, $P5_0$-$P5_7$, $P6_1$-$P6_5$, $P7_0$-$P7_7$			50	mA
$\Sigma I_{OL(avg)}$	"L" total average output current $P6_0$			1.5	mA
$I_{OH(peak)}$	"H" peak output current $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P3_0$-$P3_7$, (Note 2) $P8_0$-$P8_7$			−40	mA
$I_{OH(peak)}$	"H" peak output current $P2_0$-$P2_7$, $P4_1$-$P4_7$, $P6_0$-$P6_7$, $P7_0$-$P7_7$			−10	mA
$I_{OL(peak)}$	"L" peak output current $P2_0$-$P2_7$, $P6_1$-$P6_5$, $P7_0$-$P7_7$			10	mA
$I_{OL(peak)}$	"L" peak output current $P4_1$-$P4_7$, $P5_0$-$P5_7$			10	mA
$I_{OL(peak)}$	"L" peak output current $P6_0$			3.0	mA
$I_{OH(avg)}$	"H" average output current $P0_0$-$P0_7$, $P1_0$-$P1_7$, (Note 3) $P3_0$-$P3_7$, $P8_0$-$P8_7$			−18	mA
$I_{OH(avg)}$	"H" average output current $P2_0$-$P2_7$, $P4_1$-$P4_7$, $P6_0$-$P6_7$, $P7_0$-$P7_7$			−5.0	mA
$I_{OL(avg)}$	"L" average output current $P2_0$-$P2_7$, $P6_1$-$P6_5$, $P7_0$-$P7_7$			5.0	mA
$I_{OL(avg)}$	"L" average output current $P4_1$-$P4_7$, $P5_0$-$P5_7$			5.0	mA
$I_{OL(avg)}$	"L" average output current $P6_0$			1.5	mA
$f(CNTR_0)$ $f(CNTR_1)$	Clock input frequency for timers 2 and 4 (duty cycle 50%)			250	kHz
$f(X_{IN})$	Main clock input oscillation frequency (Note 4)			6.3	MHz
$f(X_{CIN})$	Sub clock input oscillation frequency (Note 4, 5)		32.768	50	kHz

Note 1. The total output current is the sum of all the currents flowing through all the applicable ports The total average current is an average value measured over 100ms The total peak current is the peak value of all the currents.

2. The peak output current is the peak current flowing in each port
3. The average output current in an average value measured over 100ms
4. When the oscillation frequency has a duty cycle of 50%
5. When using the microcomputer in low-speed operation mode, make sure that the sub clock's input frequency $f(X_{CIN})$ is less than $f(X_{IN})/3$

ELECTRICAL CHARACTERISTICS (V_{CC} = 4.0 to 5.5V, T_a = −10 to 85℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{OH}	"H" output voltage P0$_0$-P0$_7$, P1$_0$-P1$_7$, P3$_0$-P3$_7$, P8$_0$-P8$_7$	I_{OH}=−18mA	V_{CC}−2.0			V
V_{OH}	"H" output voltage P2$_0$-P2$_7$, P4$_1$-P4$_7$, P6$_0$-P6$_5$, P7$_0$-P7$_7$	I_{OH}=−10mA	V_{CC}−2.0			V
V_{OL}	"L" output voltage P2$_4$-P2$_7$, P4$_1$-P4$_7$, P5$_0$-P5$_7$, P6$_1$-P6$_5$	I_{OL}=10mA			2.0	V
V_{OL}	"L" output voltage P6$_0$	I_{OL}=1.5mA			0.5	V
$V_{T+}-V_{T-}$	Hysteresis $\overline{INT_0}$-$\overline{INT_4}$, S_{IN1}, S_{IN2}, S_{CLK1}, S_{CLK2}, $CNTR_0$, $CNTR_1$	When using a non-port function		0.4		V
$V_{T+}-V_{T-}$	Hysteresis $\overline{RESET}$, X_{IN}	$\overline{RESET}$: V_{CC}=2.8V to 5.5V		0.5		V
$V_{T+}-V_{T-}$	Hysteresis X_{CIN}			0.5		V
I_{IH}	"H" input current P2$_0$-P2$_7$, P4$_1$-P4$_7$, P5$_0$-P5$_7$, P6$_0$-P6$_5$, P7$_0$-P7$_7$	V_I=V_{CC}			5.0	μA
I_{IH}	"H" input current P4$_0$	V_I=V_{CC}			5.0	μA
I_{IH}	"H" input current P8$_0$-P8$_7$ (Note 1)	V_I=V_{CC}			5.0	μA
I_{IH}	"H" input current $\overline{RESET}$, X_{CIN}	V_I=V_{CC}			5.0	μA
I_{IH}	"H" input current X_{IN}	V_I=V_{CC}		4		μA
I_{IL}	"L" input current P2$_0$-P2$_7$, P4$_1$-P4$_7$, P5$_0$-P5$_7$, P6$_0$-P6$_5$, P7$_0$-P7$_7$	V_I=V_{SS}			−5.0	μA
I_{IL}	"L" input current P4$_0$	V_I=V_{SS}			−5.0	μA
I_{IL}	"L" input current P8$_0$-P8$_7$ (Note 1)	V_I=V_{SS}			−5.0	μA
I_{IL}	"L" input current $\overline{RESET}$, X_{CIN}	V_I=V_{SS}			−5.0	μA
I_{IL}	"L" input current X_{IN}	V_I=V_{SS}		−4		μA
I_{LOAD}	Output load current P0$_0$-P0$_7$, P1$_0$-P1$_7$, P3$_0$-P3$_7$	V_{EE}=V_{CC}−36V, V_{OL}=V_{CC}, With output transistors off	150	500	900	μA
I_{LEAK}	Output leakage current P0$_0$-P0$_7$, P1$_0$-P1$_7$, P3$_0$-P3$_7$, P8$_0$-P8$_7$	V_{EE}=V_{CC}−38V, V_{OL}=V_{CC}−38V, With output transistors off (Except for reset)			−10	μA
V_{RAM}	RAM hold voltage	When clock is stopped	2.0		5.5	V

Note 1. Except when reading ports P8.

ELECTRICAL CHARACTERISTICS (V_{CC} = 4.0 to 5.5V, T_a = −10 to 85℃, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ	Max	
I_{CC}	Power supply current	In high-speed operation mode $f(X_{IN})$=6.3MHz $f(X_{CIN})$=32kHz Output transistors off A-D converter operating			7.5	15	mA
		In high-speed operation mode $f(X_{IN})$=6.3MHz (in WIT state) $f(X_{CIN})$=32kHz Output transistors off A-D converter stopped			1.5		mA
		In low-speed operation mode $f(X_{IN})$= stopped, $f(X_{CIN})$=32kHz Low-power dissipation mode set (CM_5=0) Output transistors off			60	200	μA
		In low-speed operation mode $f(X_{IN})$= stopped $f(X_{CIN})$=32kHz (in WIT state) Low-power dissipation mode set (CM_5=0) Output transistors off			20	40	μA
		All oscillation stopped (in STP state) Output transistors off	T_a=25℃		0.1	1.0	μA
			T_a=85℃			10	

A-D CONVERTER CHARACTERISTICS

(V_{CC}=4.0 to 5.5V, V_{SS}=0V, T_a=−10 to 85℃, high-speed operation mode, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ.	Max	
—	Resolution				8	Bits
—	Absolute accuracy	$V_{CC}=V_{REF}$=5.12V		±1	±2.5	LSB
T_{CONV}	Conversion time		49		50	t_C (φ)
V_{REF}	Reference input voltage		2		V_{CC}	V
I_{VREF}	Reference input current	V_{REF}=5V	50	150	200	μA
I_{IA}	Analog port input current			0.5	5.0	μA
R_{LADDER}	Ladder resistor			35		kΩ

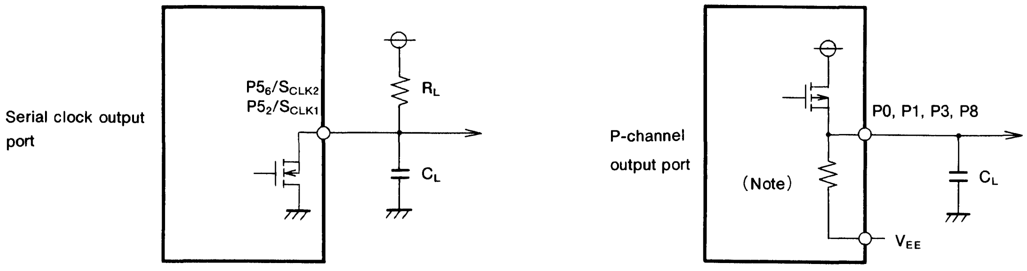
TIMING REQUIREMENTS (V_{CC} =4.0 to 5.5V, V_{SS} = 0V, T_a = −10 to 85℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{W(\overline{RESET})}$	Reset input "L" pulse width		2			μs
$t_{C(X_{IN})}$	Main clock input cycle time (X_{IN} input)		158			ns
$t_{WH(X_{IN})}$	Main clock input "H" pulse width		40			ns
$t_{WL(X_{IN})}$	Main clock input "L" pulse width		40			ns
$t_{C(X_{CIN})}$	Sub clock input cycle time (X_{CIN} input)		2.0			ms
$t_{WH(X_{CIN})}$	Sub clock input "H" pulse width		0.5			ms
$t_{WL(X_{CIN})}$	Sub clock input "L" pulse width		0.5			ms
$t_{C(CNTR)}$	$CNTR_0$, $CNTR_1$ input cycle time		4			μs
$t_{WH(CNTR)}$	$CNTR_0$, $CNTR_1$, input "H" pulse width		1.6			μs
$t_{WL(CNTR)}$	$CNTR_0$, $CNTR_1$, input "L" pulse width		1.6			μs
$t_{WH(INT)}$	INT_0-INT_4 input "H" pulse width		80			ns
$t_{WL(INT)}$	INT_0-INT_4 input "L" pulse width		80			ns
$t_{C(S_{CLK})}$	Serial clock input cycle time		1			μs
$t_{WH(S_{CLK})}$	Serial clock input clock "H" pulse width		400			ns
$t_{WL(S_{CLK})}$	Serial clock input clock "L" pulse width		400			ns
$t_{su(S_{CLK}-S_{IN})}$	Serial input setup time		200			ns
$t_{h(S_{CLK}-S_{IN})}$	Serial input hold time		200			ns

SWITCHING CHARACTERISTICS (V_{CC} = 4.0 to 5.5V, V_{SS} = 0V, T_a = −10 to 85℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{WH(S_{CLK})}$	Serial clock output "H" pulse width	C_L=100pF, R_L=1kΩ	t_C/2−160			ns
$t_{WL(S_{CLK})}$	Serial clock output "L" pulse width	C_L=100pF, R_L=1kΩ	t_C/2−160			ns
$t_{d(S_{CLK}-S_{OUT})}$	Serial output delay time				0.2t_C	ns
$t_{v(S_{CLK}-S_{OUT})}$	Serial output hold time		0			ns
$t_{f(S_{CLK})}$	Serial clock output fall time	C_L=100pF, R_L=1kΩ			40	ns
$t_{r(Pch-strg)}$	P-channel high-breakdown voltage output rise time (Note 1)	C_L=100pF, V_{EE}=V_{CC}−36V		55		ns
$t_{r(Pch-weak)}$	P-channel high-breakdown voltage output rise time (Note 2)	C_L=100pF, V_{EE}=V_{CC}−36V		1.8		μs

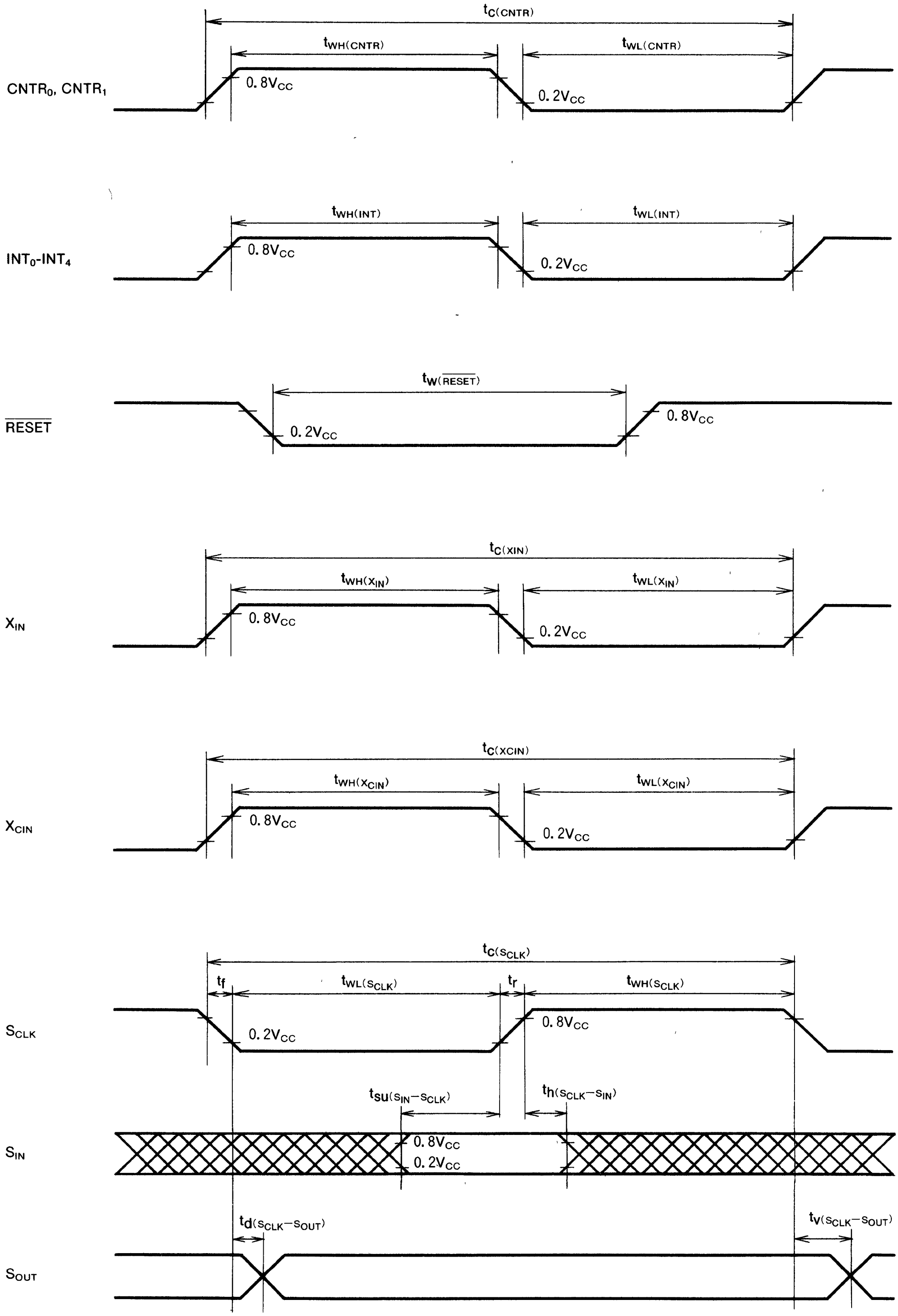
Note 1. When bit 0 of the high-breakdown voltage port control register (address 0038_{16}) is at "0"
2. When bit 0 of the high-breakdown voltage port control register (address 0038_{16}) is at "1"



Note : Port P8 has no internal pull-down resistors and external resistors should be used if necessary.

Fig. 43 Output switching characteristics measurement circuit

Timing Chart



MITSUBISHI MICROCOMPUTERS

M3818x Group

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

DESCRIPTION

The M3818x group is made up of 8-bit microcomputers based on the MELPS 740 core.

The M3818x group is designed mainly for VCR timer/function control, and include six 8-bit timers, a fluorescent display automatic display circuit, a PWM function, and an 8-channel A-D converter.

The various microcomputers in the M3818x group include variations of internal memory size and packaging. For details, see the section on part numbering.

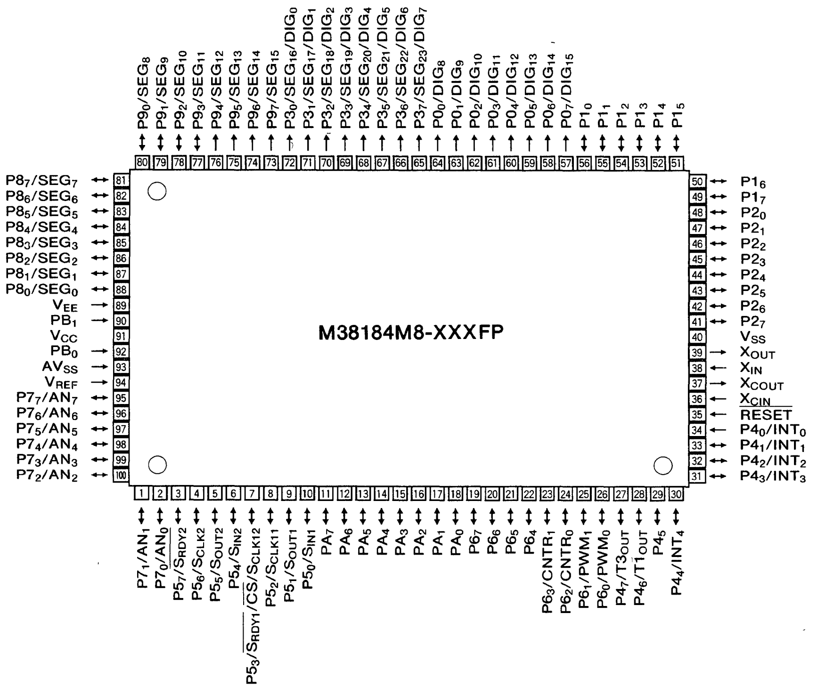
FEATURES

- Basic machine-language instructions 71
- Instruction execution time 0.63μs
  (shortest instruction at 6.3MHz oscillation frequency)
- Memory size
  ROM .... 4K to 40K bytes
  RAM .... 192 to 1024 bytes
- Programmable input/output ports 67
- High-breakdown-voltage output ports 32
- Interrupts .... 18 sources, 15 vectors
- Timers .... 8-bit×6
- Serial I/O .... Clock-synchronized 8-bit×2
  (Serial I/O1 has an automatic data transfer function)
- PWM output circuit .... 14-bit×1
  8-bit×1 (also functions as timer 6)
- A-D converter .... 8-bit×8 channels
- Fluorescent display function
  Segments .... 8 to 24
  Digits .... 4 to 16
- 2 Clock generation circuit
  Clock (X_{IN}-X_{OUT}) .... Internal feedback amplifier
  Sub clock (X_{CIN}-X_{COUT}) ··· Internal amplifier without feedback
- Supply voltage .... 4.0 to 5.5V
- Low power dissipation
  In high-speed operation 38mW
  (at 6.3MHz oscillation frequency)
  In low-speed operation 300μW
  (at 32kHz oscillation frequency)
- Operating temperature range .... −10 to 85℃

APPLICATIONS

VCRs, microwave ovens, domestic appliances, ECRs, etc.

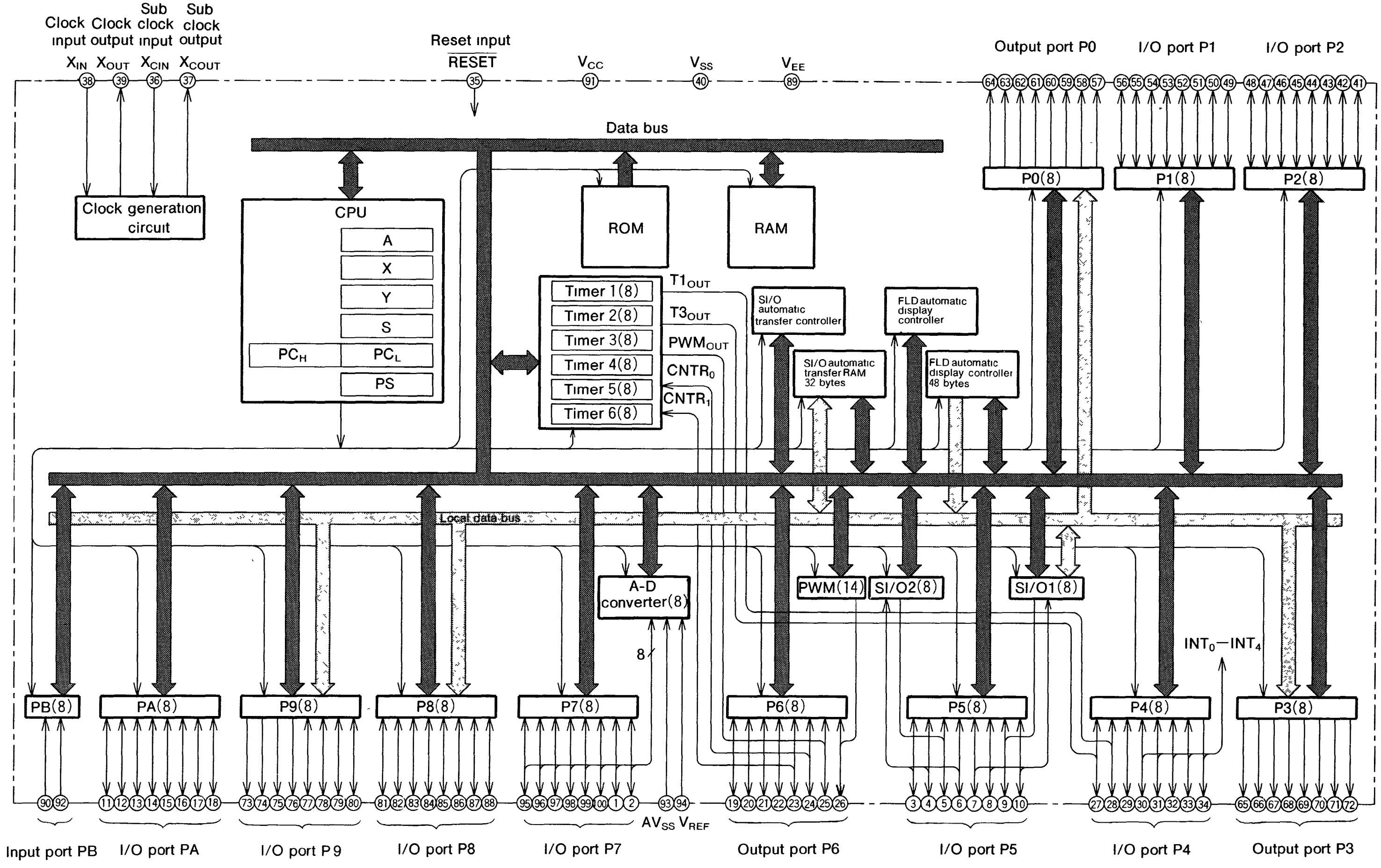
PIN CONFIGURATION (TOP VIEW)



Package type : 100P6S

100-pin plastic molded QFP

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTION

Pin	Name	Function	Alternate Function
V_{CC}, V_{SS}	Power supply	Power supply inputs 4 0 to 5 5V to V_{CC}, and 0V to V_{SS}.	
V_{EE}	Pull-down power input	Applies voltage supplied to pull-down resistors of ports P0, P3 and 8	
V_{REF}	Analog reference voltage input	Reference voltage input pin for A-D converter	
AV_{SS}	Analog power supply	GND input pin for A-D converter Keep at the same potential as V_{SS}	
$\overline{\text{RESET}}$	Reset input	To reset the microcomputer, this pin should be kept at an “L” level for more than 2μs under high-speed operating conditions In low-speed operation start mode, internal reset is not released until the X_{CIN}-X_{COUT} clock has had time to stabilize.	
X_{IN}	Clock input	Input and output signals for the internal clock generation circuit. It consist of internal feedback amplifier Connect a ceramic resonator or quartz crystal between the X_{IN} and X_{OUT} pins to set the oscillation frequency If an external clock is used, connect the clock source to the X_{IN} pin and leave the X_{OUT} pin open This clock is used as system clock	
X_{OUT}	Clock output		
X_{CIN}	Sub clock input	Input and output signals for the internal sub clock generation circuit It consist of internal amplifier without feedback Connect a ceramic resonator or quartz crystal and external feedback resistor between the X_{CIN} and X_{COUT} pins If an external clock is used, connect the clock source to the X_{CIN} pin and leave the X_{COUT} pin open This clock can also be used as the system clock	
X_{COUT}	Sub clock output		
$P0_0/DIG_8$—$P0_7/DIG_{15}$	Output port P0	An 8-bit output port The output structure is high-breakdown-voltage P-channel open drain with internal pull-down resistors connected between the output and the V_{EE} pin Are “L” at reset	FLD automatic display pins
$P1_0$—$P1_7$	I/O port P1	An 8-bit CMOS I/O port An I/O direction register allows each pin to be individually programmed as either input or output At reset this port is set to input mode The input levels are CMOS compatible	
$P2_0$—$P2_7$	I/O port P2	An 8-bit CMOS I/O port with the same function as port P1 The input levels are TTL compatible	
$P3_0/SEG_{16}/DIG_0$—$P3_7/SEG_{23}/DIG_7$	Output port P3	An 8-bit output port with the same function as port P0	FLD automatic display pins
$P4_0/INT_0$	Input port $P4_0$	A 1-bit CMOS input port	External interrupt input pin
$P4_1/INT_1$—$P4_4/INT_4$	I/O port P4	A 7-bit CMOS I/O port with the same function as port P1, with CMOS compatible input levels	External interrupt input pins
$P4_5$			
$P4_6/T1_{OUT}$, $P4_7/T3_{OUT}$			Timer output pin
$P5_0/S_{IN1}$, $P5_1/S_{OUT1}$, $P5_2/S_{CLK11}$, $P5_3/\overline{S_{RDY1}}/\overline{CS}/S_{CLK12}$	I/O port P5	An 8-bit I/O port with the same function as port P1 The output structure of this port is N-channel open drain, and the input levels are CMOS compatible Keep the input voltage of this port between 0V and V_{CC}	Serial I/O1 I/O pins
$P5_4/S_{IN2}$, $P5_5/S_{OUT2}$, $P5_6/S_{CLK2}$, $P5_7/\overline{S_{RDY2}}$			Serial I/O2 I/O pins

PIN DESCRIPTION

Pin	Name	Function	Alternate Function
P6$_0$/PWM$_0$	I/O port P6	An 8-bit CMOS I/O port with the same function as port P1, with CMOS compatible input levels	14-bit PWM output pin
P6$_1$/PWM$_1$			8-bit PWM output pin
P6$_2$/CNTR$_0$, P6$_3$/CNTR$_1$			Event counter input pins
P6$_4$— P6$_7$			
P7$_0$/AN$_0$— P7$_7$/AN$_7$	I/O port P7	An 8-bit CMOS I/O port with the same function as port P1, with CMOS compatible input levels	A-D converter input pins
P8$_0$/SEG$_0$— P8$_7$/SEG$_7$	I/O port P8	An 8-bit I/O port with the same function as port P1 The output structure of this port is P-channel open drain, and the input levels are CMOS compatible Please note that this port does not have internal pull-down resistors	FLD automatic display pins
P9$_0$/SEG$_8$— P9$_3$/SEG$_{11}$	I/O port P9	A 4-bit I/O port with the same function as port P1 The output structure of this port is P-channel open drain, and the input levels are CMOS compatible This port has internal pull-down resistors	FLD automatic display pins
P9$_4$/SEG$_{12}$— P9$_7$/SEG$_{15}$	Output port P9	A 4-bit output port with the same function as port P0	FLD automatic display pins
PA$_0$—PA$_7$	I/O port PA	An 8-bit CMOS I/O port with the same function as port P1, with CMOS compatible input levels	
PB$_0$, PB$_1$	Input port PB	A 2-bit CMOS input port	

PART NUMBERING

Product name M3818 0 M X - XXX FP

Package type
FP : 100P6S package
FS : 100D0 package

ROM number
Omitted in some types

ROM/PROM size

1 : 4096 bytes	9 : 36864 bytes
2 : 8192 bytes	A : 40960 bytes
3 : 12288 bytes	B : 45056 bytes
4 : 16384 bytes	C : 49152 bytes
5 : 20480 bytes	D : 53248 bytes
6 : 24576 bytes	E : 57344 bytes
7 : 28672 bytes	
8 : 32768 bytes	

The first 128 bytes and the last two bytes of ROM are reserved areas; they cannot be used

Memory type
M : Mask ROM version
E : EPROM or one-time programmable version

RAM size
0 : 192 bytes
1 : 256 bytes
2 : 384 bytes
3 : 512 bytes
4 : 640 bytes
5 : 768 bytes
6 : 896 bytes
7 : 1024 bytes

GROUP EXPANSION

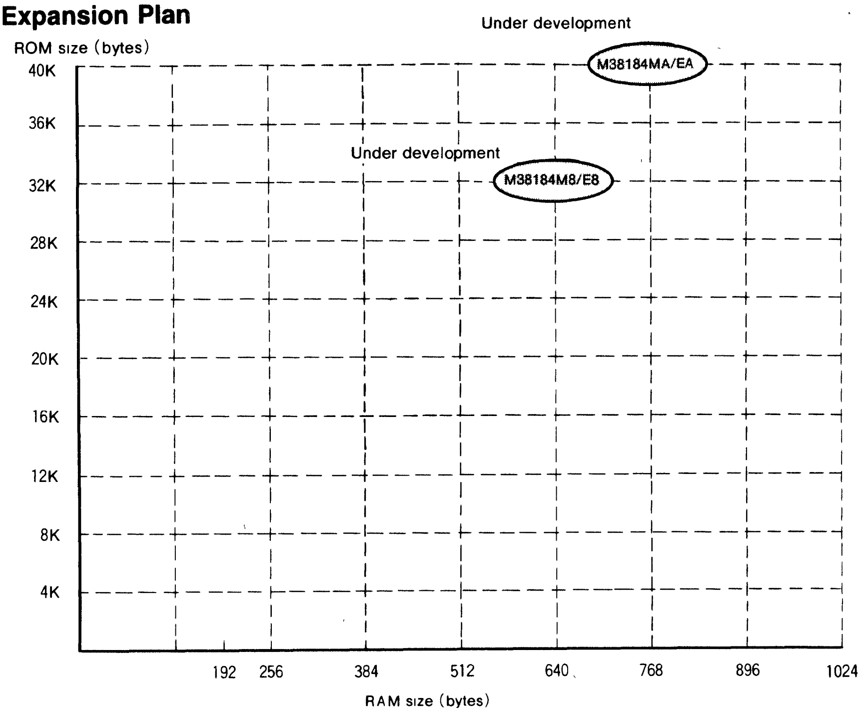
Mitsubishi plans to expand the M3818x group as follows:

(1) Support for mask ROM, one-time programmable, and EPROM versions

(2) ROM/PROM size ··························· 32K to 40K bytes
RAM size ··· 640 bytes

(3) Packages
100P6S ································· Plastic molded QFP
100D0 ····························· Window type ceramic LCC

Memory Expansion Plan



The development schedule and other details of products under development may be revised without notice

FUNCTIONAL DESCRIPTION
CENTRAL PROCESSING UNIT (CPU)

Microcomputers of the M3818x group use the standard MELPS 740 instruction set. Refer to the table of MELPS 740 addressing modes and machine instructions, or the MELPS 740 Software Manual for details on the instruction set.

Machine-resident MELPS 740 instructions are as follows:
The FST and SLW instructions are not available for use.
The STP, WIT, MUL and DIV instructions can be used.

CPU MODE REGISTER

The CPU mode register is allocated to address $003B_{16}$.

Bits 0 and 1 of this register are processor mode bits and should always be set to "0".

The CPU mode register contains the stack page selection bit.

For details of the X_{COUT} drivability selection bit, main clock stop bit, and internal system clock selection bit, see the section on the clock qeneration circuit.

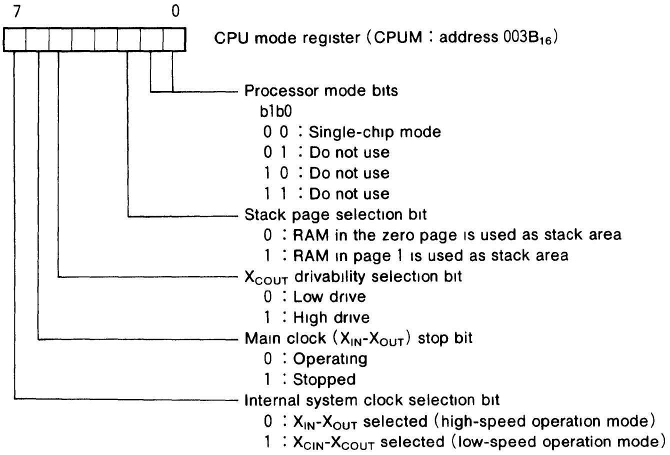


Fig. 1 Structure of CPU mode register

MEMORY

- **Special Function Register (SFR) Area**
  The Special Function Register area contains registers which control functions such as I/O ports and timers, and is located in the zero page area.
- **RAM**
  RAM is used for data storage as well for stack area.
- **ROM**
  The first 128 bytes and the last two bytes of ROM are reserved for device testing and the rest is user area for storing programs.
- **Interrupt Vector Area**
  The interrupt vector area contains reset and interrupt vectors.
- **Zero Page**
  The 256 bytes from addresses 0000_{16} to $00FF_{16}$ are called the zero page area. The internal RAM and the special function registers (SFR) are allocated to this area.
  The zero page addressing mode can be used to specify memory and register addresses in the zero page area. This dedicated zero page addressing mode enables access to this area with only 2 bytes.
- **Special Page**
  The 256 bytes from addresses $FF00_{16}$ to $FFFF_{16}$ are called the special page area. The special page addressing mode can be used to specify memory addresses in the special page area. This dedicated special page addressing mode enables access to this area with only 2 bytes.

RAM area

RAM capacity (bytes)	Address $XXXX_{16}$
192	$00FF_{16}$
256	$013F_{16}$
384	$01BF_{16}$
512	$023F_{16}$
640	$02BF_{16}$
768	$033F_{16}$
896	$03BF_{16}$
1024	$043F_{16}$

ROM area

ROM capacity (bytes)	Address $YYYY_{16}$	Address $ZZZZ_{16}$
4096	$F000_{16}$	$F080_{16}$
8192	$E000_{16}$	$E080_{16}$
12288	$D000_{16}$	$D080_{16}$
16384	$C000_{16}$	$C080_{16}$
20480	$B000_{16}$	$B080_{16}$
24576	$A000_{16}$	$A080_{16}$
28672	9000_{16}	9080_{16}
32768	8000_{16}	8080_{16}
36864	7000_{16}	7080_{16}
40960	6000_{16}	6080_{16}

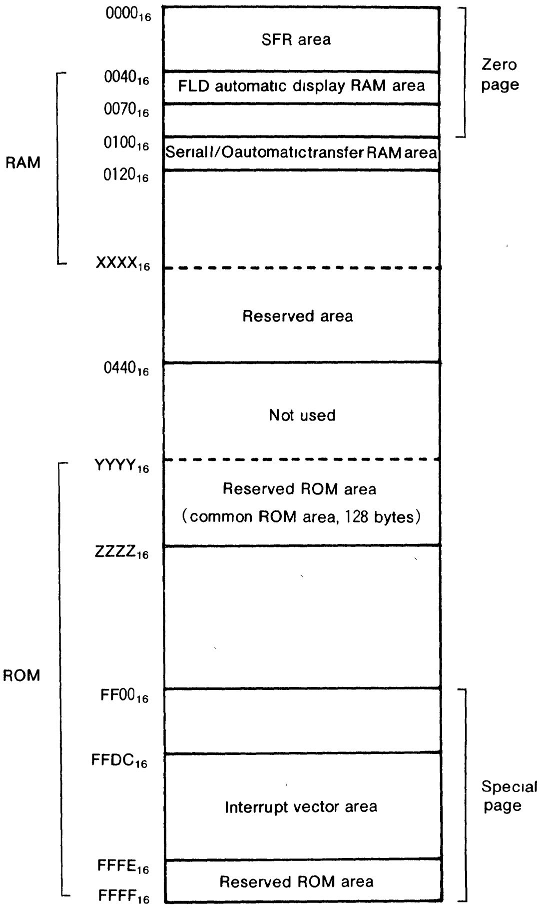


Fig. 2 Memory map diagram

0000_{16}	Port P0 (P0)	0020_{16}	Timer 1 (T1)
0001_{16}		0021_{16}	Timer 2 (T2)
0002_{16}	Port P1 (P1)	0022_{16}	Timer 3 (T3)
0003_{16}	Port P1 direction register (P1D)	0023_{16}	Timer 4 (T4)
0004_{16}	Port P2 (P2)	0024_{16}	Timer 5 (T5)
0005_{16}	Port P2 direction register (P2D)	0025_{16}	Timer 6 (T6)
0006_{16}	Port P3 (P3)	0026_{16}	
0007_{16}		0027_{16}	Timer 6 PWM register (T6PWM)
0008_{16}	Port P4 (P4)	0028_{16}	Timer 12 mode register (T12M)
0009_{16}	Port P4 direction register (P4D)	0029_{16}	Timer 34 mode register (T34M)
$000A_{16}$	Port P5 (P5)	$002A_{16}$	Timer 56 mode register (T56M)
$000B_{16}$	Port P5 direction register (P5D)	$002B_{16}$	PWM control register (PWMCON)
$000C_{16}$	Port P6 (P6)	$002C_{16}$	PWM register (upper)(PWMH)
$000D_{16}$	Port P6 direction register (P6D)	$002D_{16}$	PWM register (lower)(PWML)
$000E_{16}$	Port P7 (P7)	$002E_{16}$	
$000F_{16}$	Port P7 direction register (P7D)	$002F_{16}$	
0010_{16}	Port P8 (P8)	0030_{16}	A-D control register (ADCON)
0011_{16}	Port P8 direction register (P8D)	0031_{16}	A-D conversion register (AD)
0012_{16}	Port P9 (P9)	0032_{16}	Port P3 segment/digit switching register (P3SDR)
0013_{16}	Port P9 direction register (P9D)	0033_{16}	Port P0 digit/port switching register (P0DPR)
0014_{16}	Port PA (PA)	0034_{16}	Port P8 segment/port switching register (P8SPR)
0015_{16}	Port PA direction register (PAD)	0035_{16}	Key-scan blanking register (KSCN)
0016_{16}	Port PB (PB)	0036_{16}	FLDC mode register (FLDM)
0017_{16}		0037_{16}	FLD data pointer (FLDDP)
0018_{16}	Serial I/O automatic transfer data pointer (SIODP)	0038_{16}	High-breakdown-voltage port control register (HVPC)
0019_{16}	Serial I/O1 control register (SIO1CON)	0039_{16}	
$001A_{16}$	Serial I/O automatic transfer control register (SIOAC)	$003A_{16}$	Interrupt edge selection register (INTEDGE)
$001B_{16}$	Serial I/O1 register (SIO1)	$003B_{16}$	CPU mode register (CUPM)
$001C_{16}$	Serial I/O automatic transfer interval register (SIOAI)	$003C_{16}$	Interrupt request register 1 (IREQ1)
$001D_{16}$	Serial I/O2 control register (SIO2CON)	$003D_{16}$	Interrupt request register 2 (IREQ2)
$001E_{16}$		$003E_{16}$	Interrupt control register 1 (ICON1)
$001F_{16}$	Serial I/O2 register (SIO2)	$003F_{16}$	Interrupt control register 2 (ICON2)

Fig. 3 Memory map of special function register (SFR)

I/O PORTS

- **Direction Registers**

The M3818x group microprocessors have 67 programmable I/O pins arranged in nine I/O ports (ports P1, P2, $P4_1$-$P4_7$, P5-P8, $P9_0$-$P9_3$ and PA). The I/O ports have direction registers which determine the input/output direction of each individual pin. Each bit in a direction register corresponds to one pin, each pin can be set to be input or output.

When "0" is written to the bit corresponding to a pin, that pin becomes an input pin. When "1" is written to that bit, that pin becomes an output pin.

If data is read from a pin which is set for output, the value of the port output latch is read, not the value of the pin itself. Pins set to input are floating. If a pin set to input is written to, only the port output latch is written to and the pin remains floating.

- **High-Breakdown-Voltage Output Ports**

The M3818x group microprocessors have four ports with high-breakdown-voltage pins(ports P0, P3, P8, P9). The high-breakdown-voltage ports have P-channel open drain output with a breakdown voltage of $V_{CC}-40V$. Each pin in Ports P0, P3, and P9 has an internal pull-down resistor connected to V_{EE}. Port P8 has no internal pull-down resistors and external resistors should be used if necessary. At reset, the P-channel output transistor of each port latch is turned off, so it is forced to the level of V_{EE} by the pull-down resistor.

Writing "1" to bit 0 of the high-breakdown-voltage port control register(address 0038_{16})slows the transition of the output transistors to reduce transient noise. At reset, bit 0 of the high-breakdown-voltage port control register is set to "0" (strong drive).

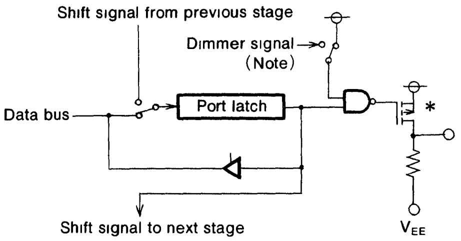
SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

Pin	Name	Input/Output	I/O Format	Non-Port Function	Related SFRs	Diagram No.
$P0_0/SEG_8$— $P0_3/DIG_{11}$	Port P0	Output	High-breakdown-voltage P-channel open-drain output with pull-down resistor	FLD automatic display function	FLDC mode register High-breakdown-voltage port control register	(1)
$P0_4/SEG_{12}$— $P0_7/SEG_{15}$					FLDC mode register Digit/port switching register High-breakdown-voltage port control register	(2)
$P1_0$—$P1_7$	Port P1	Input/output, individual bits	CMOS level input CMOS 3-state output			(3)
$P2_0$—$P2_7$	Port P2	Input/output, individual bits	TTL level input CMOS 3-state output			(3)
$P3_0/SEG_{16}/DIG_{16}$—$P3_7/SEG_{23}/DIG_7$	Port P3	Output	High-breakdown-voltage P-channel open-drain output with pull-down resistor	FLD automatic display function	FLDC mode register Segment/digit switching register High-breakdown-voltage port control register	(4)
$P4_0/INT_0$	Port P4	Input	CMOS level input	External interrupt input	Interrupt edge selection register	(5)
$P4_1/INT_1$— $P4_4/INT_4$		Input/output, individual bits	CMOS level input CMOS 3-state output	External interrupt input	Interrupt edge selection register	(6)
$P4_5$						(3)
$P4_6/T1_{OUT}$, $P4_7/T3_{OUT}$				Timer output	Timer 12 mode register Timer 34 mode register	(7)
$P5_0/S_{IN1}$,	Port P5	Input/output, individual bits	CMOS level input N-channel open-drain output	Serial I/O1 function I/O	Serial I/O1 control register Serial I/O automatic transfer control register	(8)
$P5_1/S_{OUT1}$, $P5_2/S_{CLK1}$,						(9)
$P5_3/\overline{S_{RDY1}}/\overline{CS}/S_{CLK12}$						(10)
$P5_4/S_{IN2}$,				Serial I/O2 function I/O	Serial I/O2 control register	(8)
$P5_5/S_{OUT2}$, $P5_6/S_{CLK2}$,						(9)
$P5_7/\overline{S_{RDY2}}$						(10)
$P6_0/PWM_0$	Port P6	Input/output, individual bits	CMOS level input CMOS 3-state output	14-bit PWM output	PWM control register PWML register PWMH register	(11)
$P6_1/PWM_1$				8-bit PWM output	Timer 56 mode register Timer 6 PWM register	(7)
$P6_2/CNTR_0$, $P6_3/CNTR_1$				External count input	Interrupt edge selection register	(6)
$P6_4$— $P6_7$						(3)
$P7_0/AN_0$— $P7_7/AN_7$	Port P7	Input/output, individual bits	CMOS level input CMOS 3-state output	A-D converter input	A-D control register	(12)
$P8_0/SEG_0$— $P8_7/SEG_7$	Port P8	Input/output, individual bits	CMOS level input High-breakdown-voltage P-channel open-drain output without pull-down resistor	FLD automatic display function	FLDC mode register Segment/port switching register High-breakdown-voltage port control registor	(13)

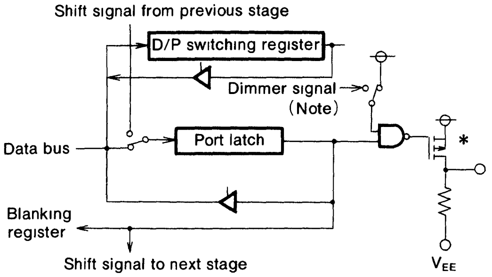
Note. Make sure that the input level at each pin is either 0V or V_{CC} during execution of the STP instruction
If an input level is at an intermediate potential, a current will flow in the input-stage gate

Pin	Name	Input/Output	I/O Format	Non-Port Function	Related SFRs	Diagram No.
$P9_0/SEG_8$—$P9_3/SEG_{11}$	Port P9	Input/output, individual bits	CMOS level input High-breakdown-voltage P-channel open-drain output with pull-down resistor	FLD automatic display function	FLDC mode register High-breakdown-voltage port control registor	(14)
$P9_4/SEG_{12}$—$P9_7/SEG_{15}$		Output	High-breakdown-voltage P-channel open-drain output with pull-down resistor			(15)
PA_0—PA_7	Port PA	Input/output, individual bits	CMOS level input CMOS 3-state output			(3)
PB_0, PB_1	Port PB	Input	CMOS level input			(16)

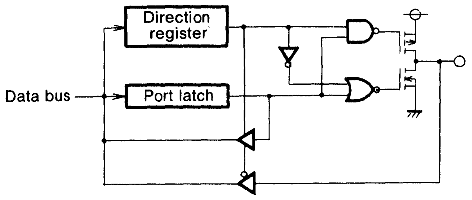
(1) Port $P0_0$-$P0_3$



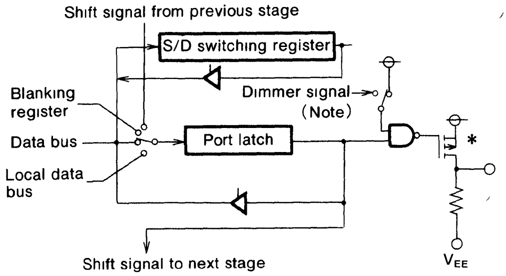
(2) Port $P0_4$-$P0_7$



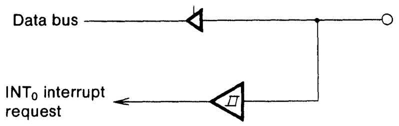
(3) Port P1, P2, $P4_5$, $P6_4$- $P6_7$, PA



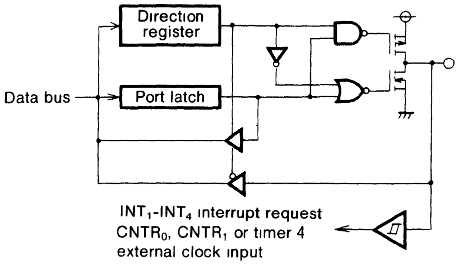
(4) Port P3



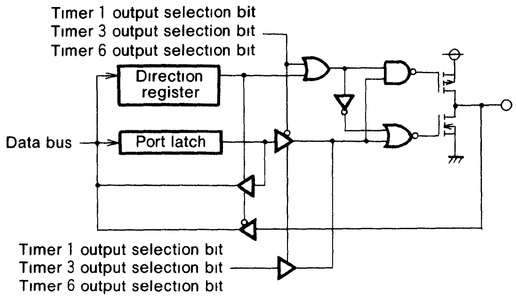
(5) Port $P4_0$



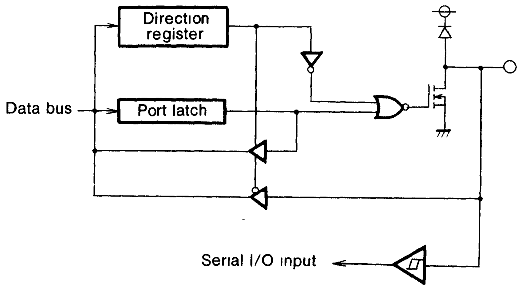
(6) Port $P4_1$-$P4_4$, $P6_2$, $P6_3$



(7) Port $P4_6$, $P4_7$, $P6_1$



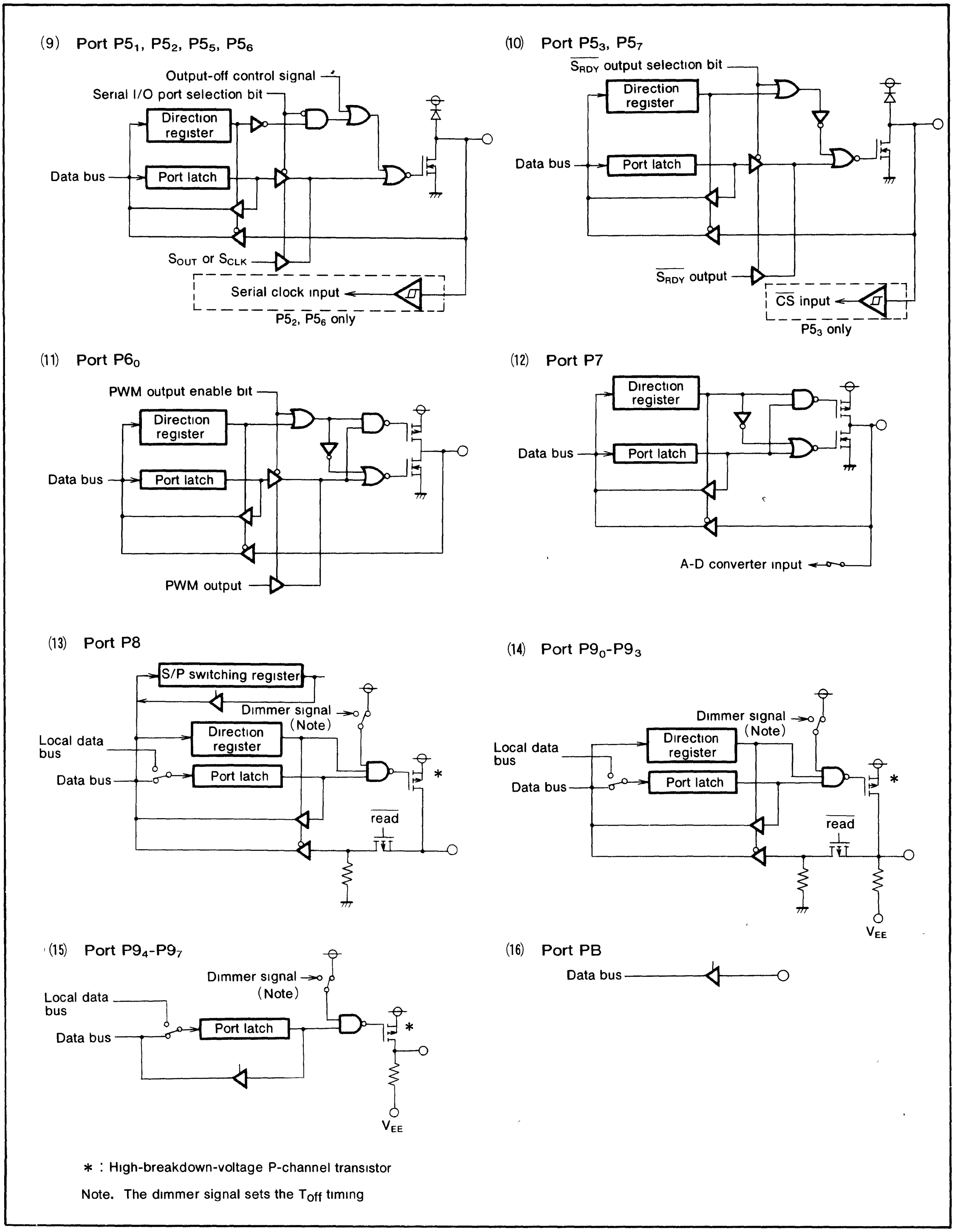
(8) Port $P5_0$, $P5_4$



* : High-breakdown-voltage P-channel transistor

Note. The dimmer signal sets the T_{off} timing

Fig. 4 Port block diagram (1)



* : High-breakdown-voltage P-channel transistor

Note. The dimmer signal sets the T_{off} timing

Fig. 5 Port block diagram (2)

INTERRUPTS

A total of 18 source can generate interrupts: 5 external, 12 internal, and 1 software.

- **Interrupt Control**

  Each interrupt is controlled by its interrupt request bit, its interrupt enable bit, and the interrupt disable flag except for the software interrupt set by the BRK instruction. An interrupt is generated if the corresponding interrupt request and enable bits are "1" and the interrupt disable flag is "0".

  Interrupt enable bits can be set or cleared by software.

  Interrupt request bits can be cleared by software, but cannot be set by software.

  The I flag disables all interrupts except for the BRK instruction interrupt.

- **Interrupt Operation**

  When an interrupt is received, the program counter and processor status register are automatically pushed onto the stack. The interrupt disable flag is set to inhibit other interrupts from interfering. The corresponding interrupt request bit is cleared and the interrupt jump destination address is read from the vector table into the program counter.

- **Notes on Use**

  If you will change interrupt edge selection from rising edge to falling edge, interrupt request bit will be set to "1" automatically. Therefore, please make following process;

  (1) Disable INT which is selected.
  (2) Change INT edge selection.
  (3) Clear interrupt request which is selected.
  (4) Enable INT which is selected.

Table 1. Interrupt vector addresses and priorities

Interrupt Cause	Priority	Vector Address (Note 1)		Interrupt Request Generation Conditions	Remarks
		High	Low		
Reset (Note 2)	1	FFFD$_{16}$	FFFC$_{16}$	At reset	Non-maskable
INT$_0$	2	FFFB$_{16}$	FFFA$_{16}$	At detection of either rising or falling edge of INT$_0$ input	External interrupt (active edge selectable)
INT$_1$	3	FFF9$_{16}$	FFF8$_{16}$	At detection of either rising or falling edge of INT$_1$ input	External interrupt (active edge selectable)
INT$_2$	4	FFF7$_{16}$	FFF6$_{16}$	At detection of either rising or falling edge of INT$_2$ input	External interrupt (active edge selectable)
Serial I/O1	5	FFF5$_{16}$	FFF4$_{16}$	At end of data transfer	Valid when serial I/O normal mode is selected
Serial I/O automatic transfer				At end of final data transfer	Valid when serial I/O automatic transfer mode is selected
Serial I/O2	6	FFF3$_{16}$	FFF2$_{16}$	At end of data transfer	
Timer 1	7	FFF1$_{16}$	FFF0$_{16}$	At timer 1 overflow	
Timer 2	8	FFEF$_{16}$	FFEE$_{16}$	At timer 2 overflow	STP release timer overflow
Timer 3	9	FFED$_{16}$	FFEC$_{16}$	At timer 3 overflow	
Timer 4	10	FFEB$_{16}$	FFEA$_{16}$	At timer 4 overflow	
Timer 5	11	FFE9$_{16}$	FFE8$_{16}$	At timer 5 overflow	
Timer 6	12	FFE7$_{16}$	FFE6$_{16}$	At timer 6 overflow	
INT$_3$	13	FFE5$_{16}$	FFE4$_{16}$	At detection of either rising or falling edge of INT$_3$ input	External interrupt (active edge selectable)
INT$_4$	14	FFE3$_{16}$	FFE2$_{16}$	At detection of either rising or falling edge of INT$_4$ input	External interrupt valid when INT$_4$ interrupt is selected (active edge selectable)
A-D converter				At end of A-D conversion	Valid when A-D interrupt is selected
FLD blanking	15	FFE1$_{16}$	FFE0$_{16}$	At fall of final digit	Valid when FLD blanking interrupt is selected
FLD digit				At rise of each digit	Valid when FLD digit interrupt is selected
BRK instruction	16	FFDD$_{16}$	FFDC$_{16}$	At BRK instruction execution	Non-maskable software interrupt

Note 1. Vector addresses contain interrupt jump destination addresses
2. Reset function in the same way as an interrupt with the highest priority

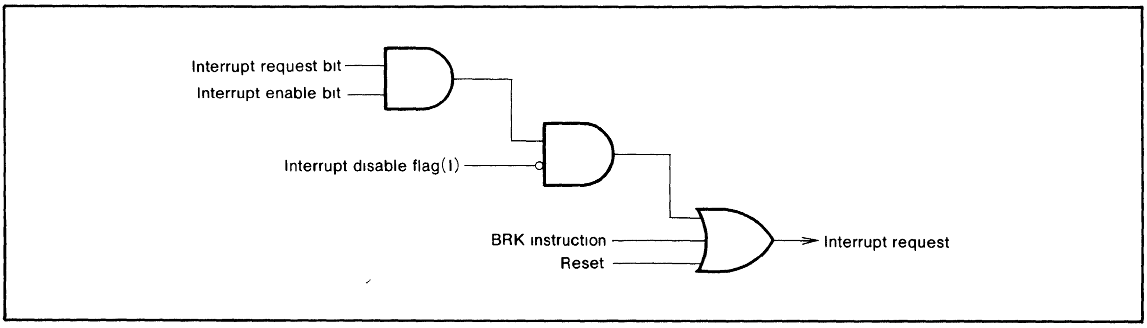


Fig. 6 Interrupt control

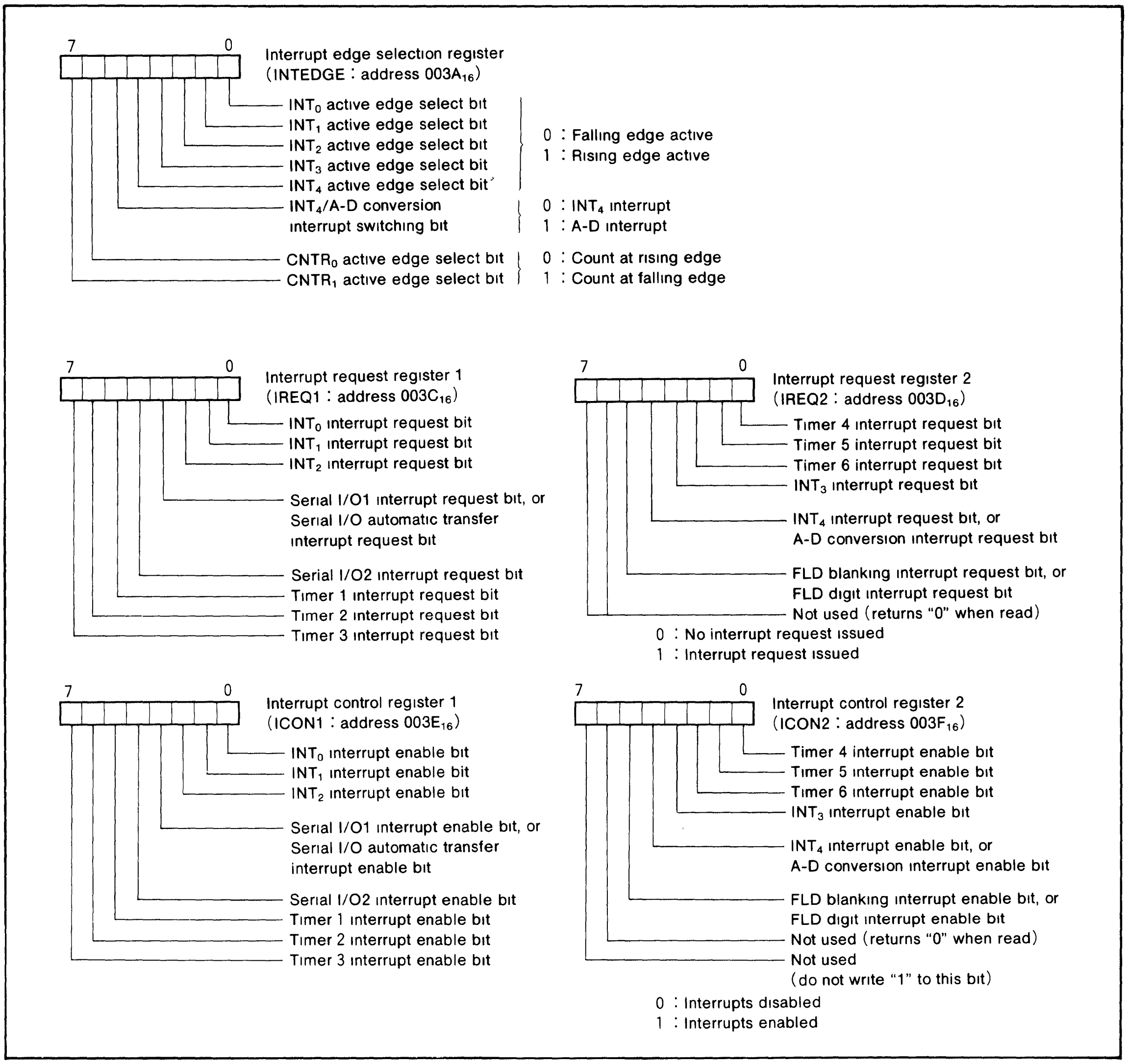


Fig. 7 Structure of interrupt-related registers

TIMERS

Microcomputers of the M3818x group have six built-in timers. The timers count down. Once a timer reaches 00_{16}, the next count pulse loads the contents of the corresponding timer latch into the timer, and sets the corresponding interrupt request bit to 1. Each timer also has a stop bit that stops the count of that timer when it is set to "1".

Note that the system clock ϕ can be set to either high-speed mode or low-speed mode by the CPU mode register.

- **Timer 1 and Timer 2**

  The count sources of timer 1 and timer 2 can be selected by setting the timer 12 mode register.

  Timer 1 can also output a rectangular waveform from the $P4_6/T1_{OUT}$ pin. The waveform changes polarity each time timer 1 overflows.

  The active edge of the external signal $CNTR_0$ can be set by the interrupt edge selection register.

  When the chip is reset or the STP instruction is executed, all bits of the timer 12 mode register are cleared, timer 1 is set to FF_{16}, and timer 2 is set to 01_{16}.

- **Timer 3 and Timer 4**

  The count sources of timer 3 and timer 4 can be selected by setting the timer 34 mode register.

  Timer 3 can also output a rectangular waveform from the $P4_7/T3_{OUT}$ pin. The waveform changes polarity each time timer 3 overflows.

  The active edge of the external signal $CNTR_1$ can be set by the interrupt edge selection register.

- **Timer 5 and Timer 6**

  The count sources of timer 5 and timer 6 can be selected by setting the timer 56 mode register.

  Timer 6 can also output a rectangular waveform from the $P6_1/PWM_1$ pin. The waveform changes polarity each time timer 6 overflows.

- **Timer 6 PWM_1 Mode**

  Timer 6 can also output a rectangular waveform of n cycles high and m cycles low. The n is the value set in timer latch 6 (address 0025_{16}) and m is the value in the timer 6 PWM register (address 0027_{16}). If n is "0", the PWM_1 output is "L", if m is "0" and n is not "0", then the PWM_1 output is "H". In PWM mode, interrupts are generated at the rising edge of the PWM_1 output.

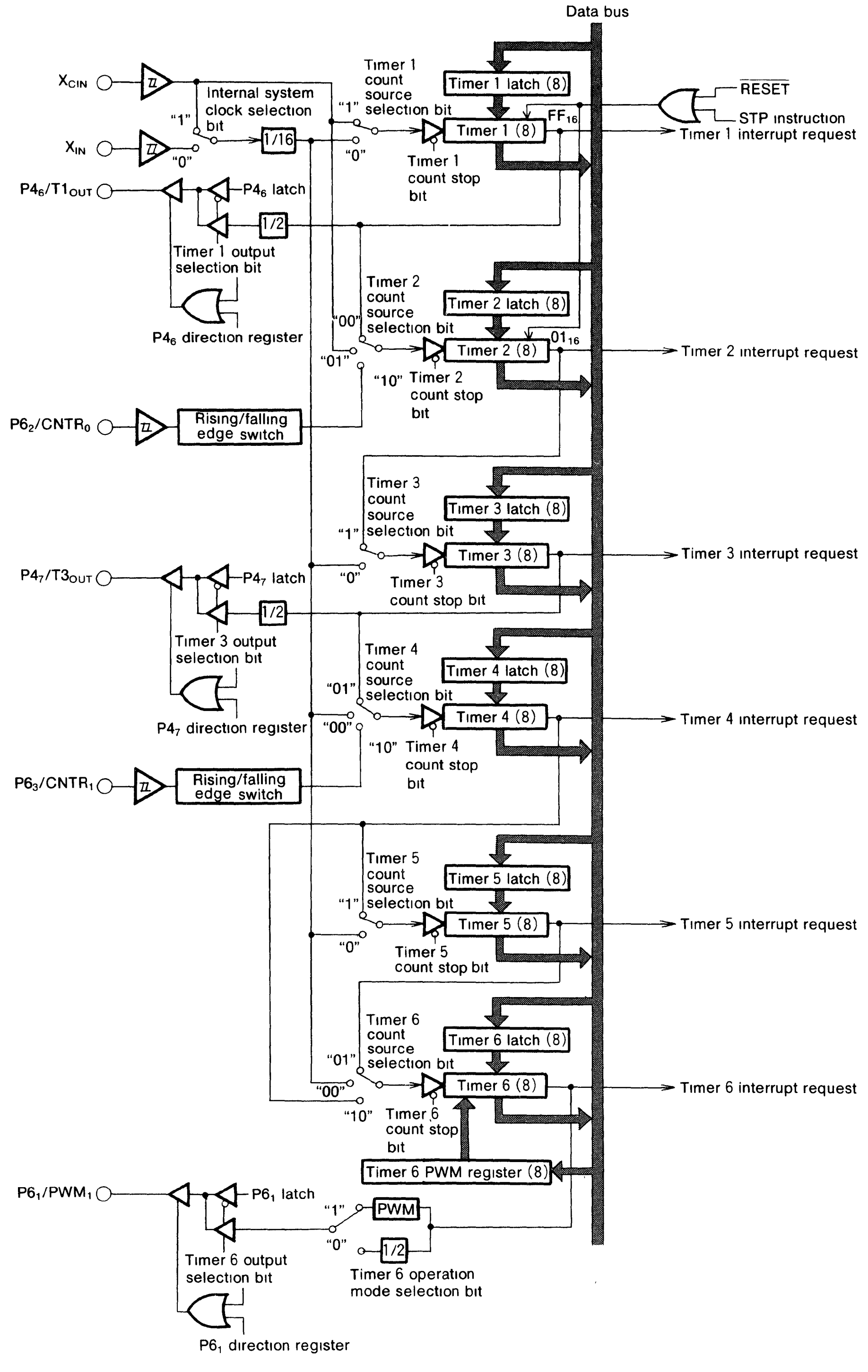


Fig. 8 Timer block diagram

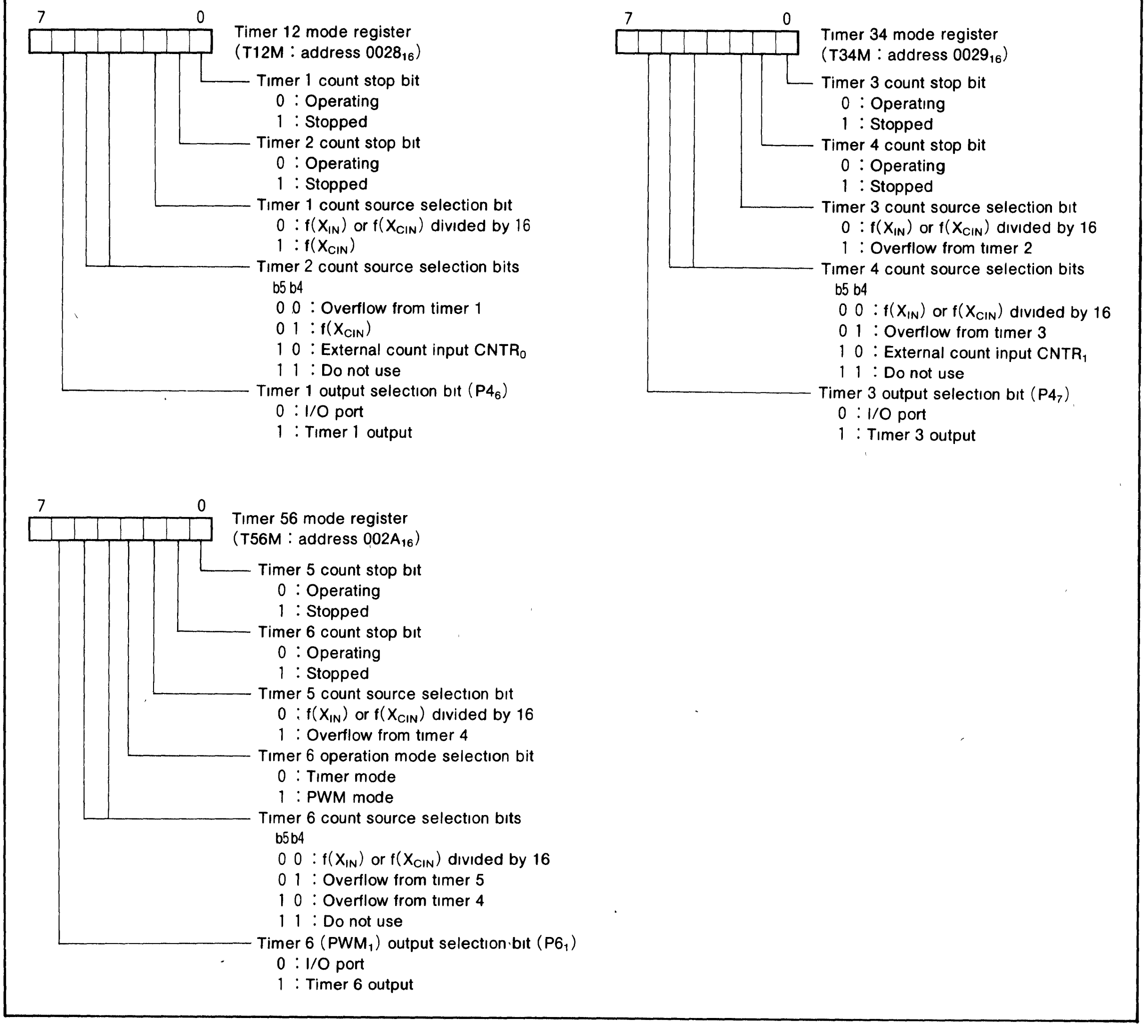
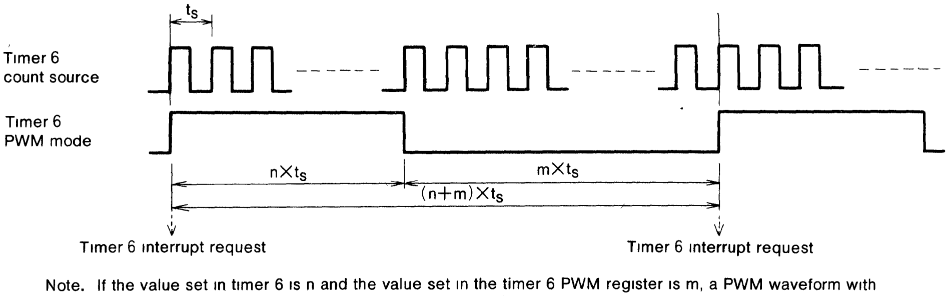


Fig. 9 Structure of timer-related registers



Note. If the value set in timer 6 is n and the value set in the timer 6 PWM register is m, a PWM waveform with duty cycle n/(n+m) and period $(n+m) \times t_S$ is output (where is t_S the frequency of the timer 6 count source)

Fig. 10 Timing in timer 6 PWM_1 mode

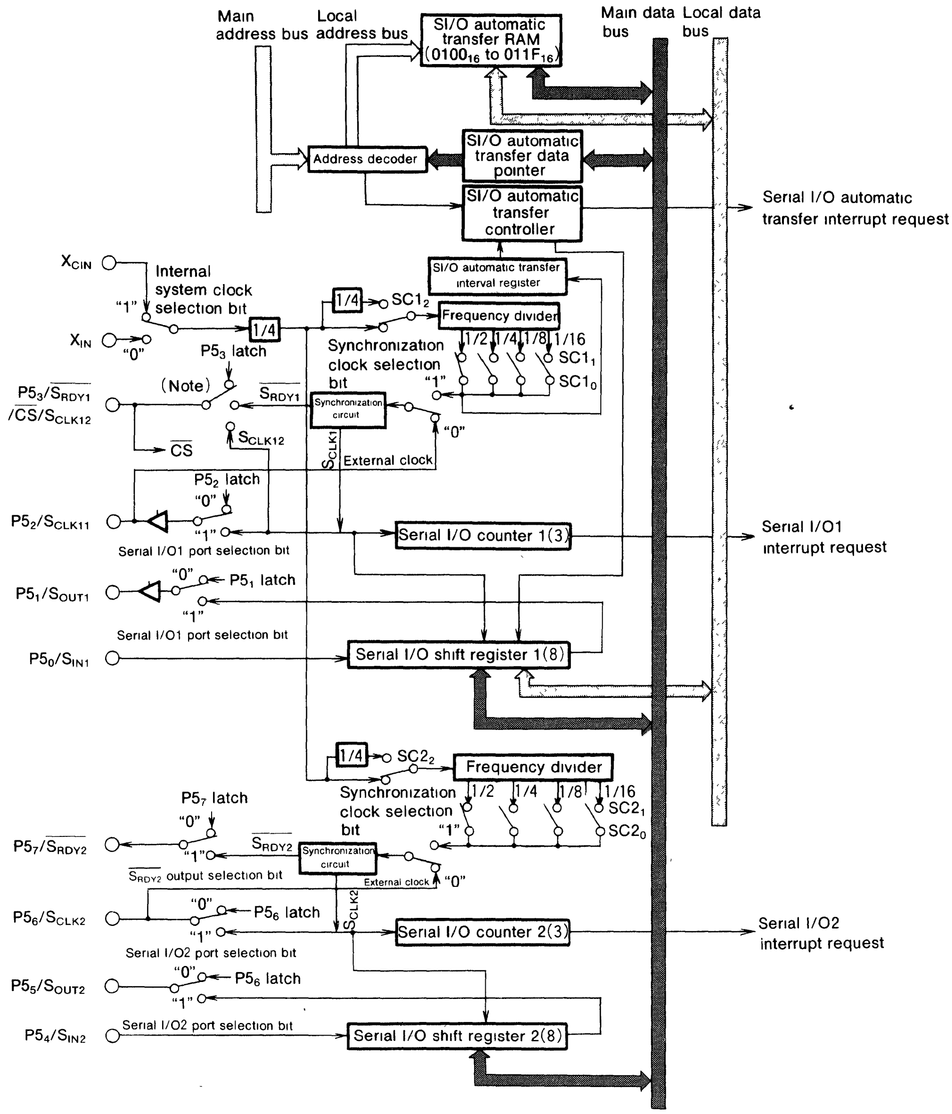
SERIAL I/O

Microcomputers of the M3818x group have two built-in 8-bit clock synchronized serial I/O channels (serial I/O1 and serial I/O2).

Serial I/O1 has a built-in automatic transfer function.Normal serial operation can be set via the serial I/O automatic transfer control register (address $001A_{16}$).

Serial I/O2 can only be used in normal operation mode.

The I/O pins of the serial I/O function also operate as I/O port P5, and their operation is selected by the serial I/O control registers (addresses 0019_{16} and $001D_{16}$).

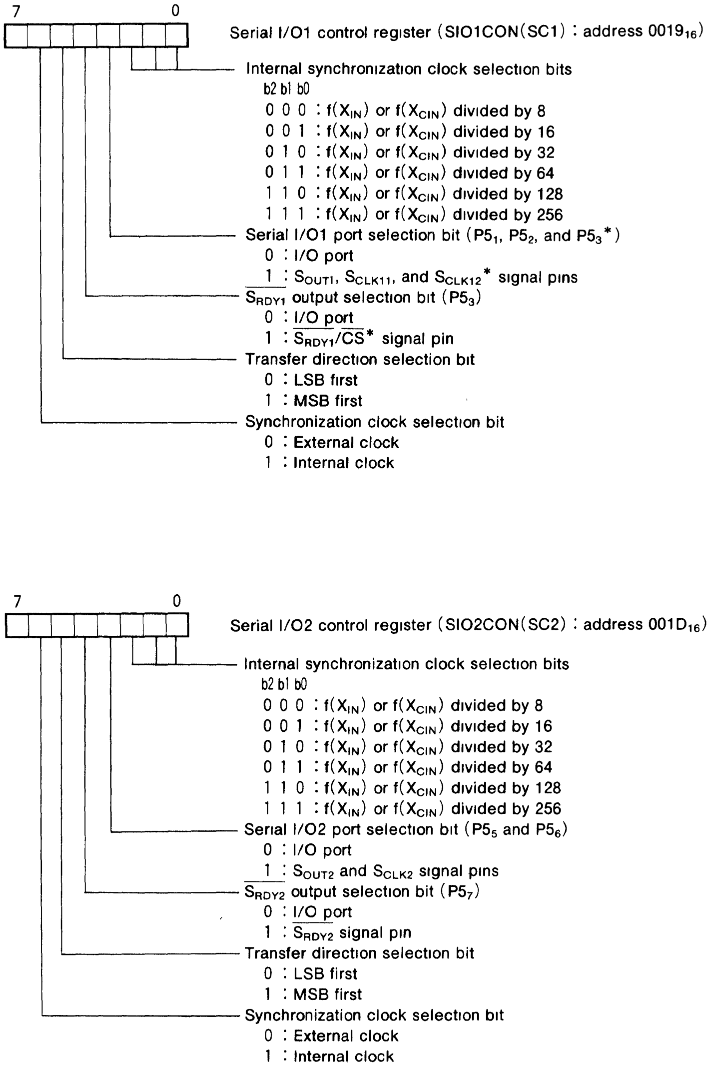


Note. Selection is by the synchronization clock selection bit, the $\overline{S_{RDY1}}$ output selection bit, and the serial I/O1 port selection bit of the serial I/O1 control register, and the automatic transfer control bit and synchronization clock output pin selection bit of the serial I/O automatic transfer control register

Fig. 11 Serial I/O block diagram

(Serial I/O Control Registers) SIO1CON, SIO2CON

Each of the serial I/O control registers (addresses 0019_{16} and $001D_{16}$) contains seven bits that select various control parameters of the serial I/O function.



Serial I/O1 control register (SIO1CON(SC1) : address 0019_{16})

Internal synchronization clock selection bits
b2 b1 b0
0 0 0 : f(X_{IN}) or f(X_{CIN}) divided by 8
0 0 1 : f(X_{IN}) or f(X_{CIN}) divided by 16
0 1 0 : f(X_{IN}) or f(X_{CIN}) divided by 32
0 1 1 : f(X_{IN}) or f(X_{CIN}) divided by 64
1 1 0 : f(X_{IN}) or f(X_{CIN}) divided by 128
1 1 1 : f(X_{IN}) or f(X_{CIN}) divided by 256

Serial I/O1 port selection bit ($P5_1$, $P5_2$, and $P5_3$*)
0 : I/O port
1 : S_{OUT1}, S_{CLK11}, and S_{CLK12}* signal pins

$\overline{S_{RDY1}}$ output selection bit ($P5_3$)
0 : I/O port
1 : $\overline{S_{RDY1}}/\overline{CS}$* signal pin

Transfer direction selection bit
0 : LSB first
1 : MSB first

Synchronization clock selection bit
0 : External clock
1 : Internal clock

Serial I/O2 control register (SIO2CON(SC2) : address $001D_{16}$)

Internal synchronization clock selection bits
b2 b1 b0
0 0 0 : f(X_{IN}) or f(X_{CIN}) divided by 8
0 0 1 : f(X_{IN}) or f(X_{CIN}) divided by 16
0 1 0 : f(X_{IN}) or f(X_{CIN}) divided by 32
0 1 1 : f(X_{IN}) or f(X_{CIN}) divided by 64
1 1 0 : f(X_{IN}) or f(X_{CIN}) divided by 128
1 1 1 : f(X_{IN}) or f(X_{CIN}) divided by 256

Serial I/O2 port selection bit ($P5_5$ and $P5_6$)
0 : I/O port
1 : S_{OUT2} and S_{CLK2} signal pins

$\overline{S_{RDY2}}$ output selection bit ($P5_7$)
0 : I/O port
1 : $\overline{S_{RDY2}}$ signal pin

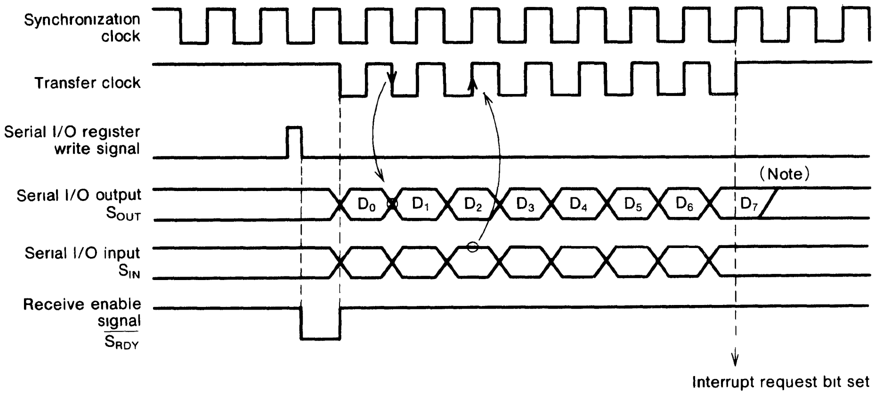
Transfer direction selection bit
0 : LSB first
1 : MSB first

Synchronization clock selection bit
0 : External clock
1 : Internal clock

* : Valid only in serial I/O automatic transfer mode

Fig. 12 Structure of serial I/O control registers

(1) Operation in Normal Serial I/O Mode
Either an internal clock or an external clock can be selected as the synchronization clock for serial I/O transfer. A dedicated divider is built-in as the internal clock, giving a choice of six clocks.
If internal clock is selected, transfer start is activated by a write signal to a serial I/O register (address $001B_{16}$ or $001F_{16}$). After eight bits have been transferred, the S_{OUT} pin goes to high impedance.
If external clock is selected, the clock must be controlled externally because the contents of the serial I/O register continue to shift while the transfer clock is input. In this case, note that the S_{OUT} pin does not go to high impedance at the completion of data transfer. The interrupt request bit is set at the end of the transfer of eight bits, regardless of whether the internal or external clock is selected.



Note. If internal clock is selected, the S_{OUT} pin is at high impedance after transfer ends

Fig. 13 Serial I/O timing in normal mode (for LSB first)

(2) Serial I/O Automatic Transfer Mode
The serial I/O1 function has an automatic transfer function. For automatic transfer, switch to the automatic transfer mode by setting the serial I/O automatic transfer control register (address $001A_{16}$).
The following memory spaces are added to the circuits used for the serial I/O1 function in ordinary mode, to enable automatic transfer mode:

- 32 bytes of serial I/O automatic transfer RAM
- A serial I/O automatic transfer control register
- A serial I/O automatic transfer interval register
- A serial I/O automatic transfer data pointer

When using serial I/O automatic transfer, set the serial I/O control register (address 0019_{16}) in the same way as for ordinary mode. However, note that if external clock is selected and bit 4 (the $\overline{S_{RDY1}}$ output selection bit) of the serial I/O1 control register is set to "1", port $P5_3$ becomes the $\overline{CS}$ input pin.

(Serial I/O Automatic Transfer Control Register)
SIOAC

The serial I/O automatic transfer control register (address $001A_{16}$) contains four bits that select various control parameters for automatic transfer.

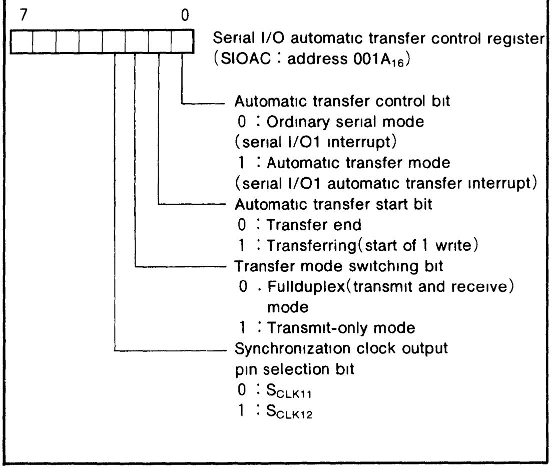


Fig. 14 Structure of serial I/O automatic transfer control register

(Serial I/O Automatic Transfer Data Pointer) SIODP

The serial I/O automatic transfer data pointer (address 0018_{16}) contains five bits that indicate addresses in serial I/O automatic transfer RAM (each address in memory is actually the value in the serial I/O automatic transfer data pointer plus 0100_{16}).

Set the serial I/O automatic transfer data pointer to (the number of transfer data−1), to specify the storage position of the start of data.

- Serial I/O Automatic Transfer RAM

  The serial I/O automatic transfer RAM is the 32 bytes from address 0100_{16} to address $011F_{16}$.

Address \ Bit	7	6	5	4	3	2	1	0
0100_{16}								
0101_{16}								
0102_{16}								
⋮				⋮				
$011D_{16}$								
$011E_{16}$								
$011F_{16}$								

Fig. 15 Bit allocation of serial I/O automatic transfer RAM

- Setting of Serial I/O Automatic Transfer Data

  When data is stored in the serial I/O automatic transfer RAM, it is stored with the start of the data at the address set by the serial I/O automatic transfer data pointer and the end of the data at address 0100_{16}.

(Serial I/O Automatic Transfer Interval Register) SIOAI

The serial I/O automatic transfer interval register (address $001C_{16}$) consists of a 5-bit counter that determines the transfer interval Ti during automatic transfer.

If a value n is written to the serial I/O automatic transfer interval register, a value of $Ti = (n+2) \times Tc$ is generated, where Tc is the length of one bit of the transfer clock. However, note that this transfer interval setting is only valid when internal clock has been selected as the clock source.

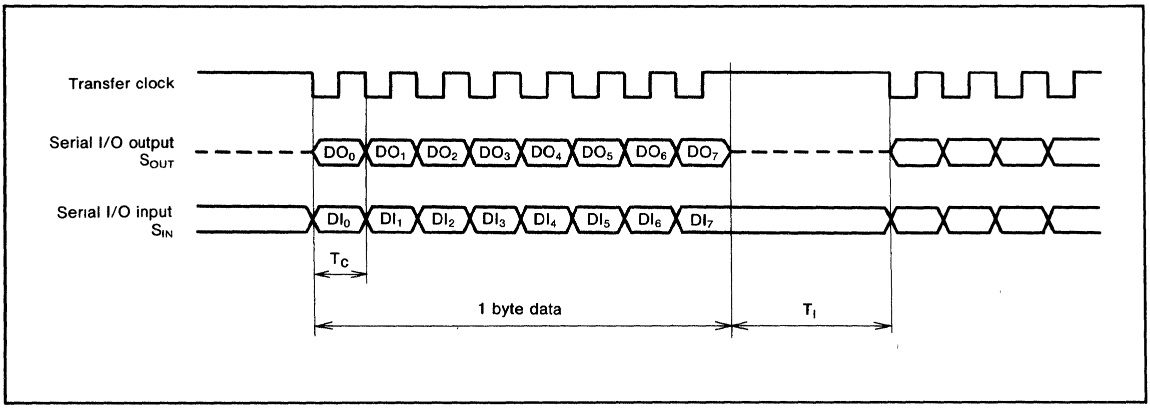


Fig. 16 Serial I/O automatic transfer interval timing

- **Setting of Serial I/O Automatic Transfer Timing**

  Use the serial I/O1 control register (address 0019_{16}) and the serial I/O automatic transfer interval register (address $001C_{16}$) to set the timing of serial I/O automatic transfer.

  The serial I/O1 control register sets the transfer clock speed, and the serial I/O automatic transfer interval register sets the serial I/O automatic transfer interval.

  This setting of transfer interval is valid only when internal clock is selected as the clock source.
- **Start of Serial I/O Automatic Transfer**

  Automatic transfer mode is set by writing "1" to bit 0 of the serial I/O automatic transfer control register (address $001A_{16}$), then automatic transfer starts when "1" is written to that bit. Bit 1 of the serial I/O automatic transfer control register is always "1" during automatic transfer; writing "0" to it is one way to end automatic transfer.
- **Operation in Serial I/O Automatic Transfer Modes**

  There are two modes for serial I/O automatic transfer: full duplex mode and transmit-only mode. Either internal or external clock can be selected for each of these modes

(2.1) Operation in Full Duplex Mode

In full duplex mode, data can be transmitted and received at the same time. Data in the automatic transfer RAM is sent in sequence and simultaneously receive data is written to the automatic transfer RAM, in accordance with the serial I/O automatic transfer data pointer.

The transfer timing of each bit is the same as in ordinary operation mode, and the transfer clock stops at "H" after eight transfer clocks are counted. If internal clock is selected, the transfer clock remains at "H" for the time set by the serial I/O automatic transfer interval register, then the data at the next address indicated by the serial I/O automatic transfer data pointer is transferred. If external clock is selected, the setting of the automatic transfer interval register is invalid, so the user must ensure that the transfer clock is controlled externally.

Data transfer ends when the contents of the serial I/O automatic transfer pointer reach "00_{16}". At that point, the serial I/O automatic transfer interrupt request bit is set to "1" and bit 1 of the serial I/O automatic transfer control register is cleared to "0" to complete the serial I/O automatic transfer.

(2.2) Operation in Transmit-Only Mode

The operation in transmit-only mode is the same as that in full duplex mode, except that data is not transferred from the serial I/O1 register to the serial I/O automatic transfer RAM.

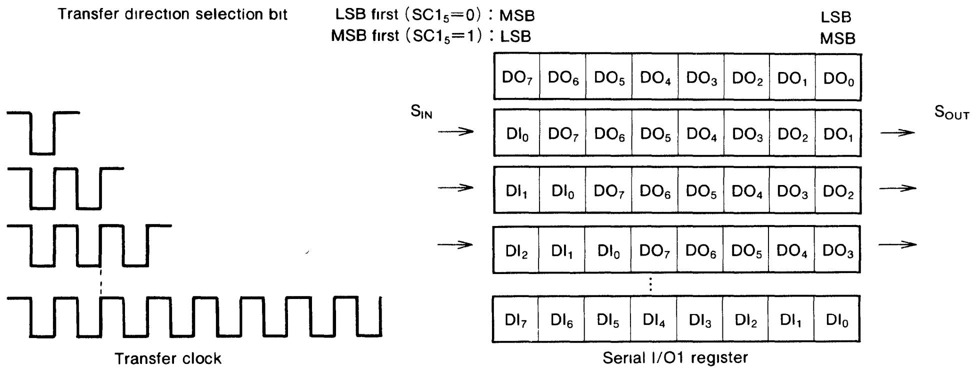


Fig. 17 Serial I/O1 register in full duplex mode

(2.3) If Internal Clock is Selected

If internal clock is selected, the $P5_3/\overline{S_{RDY1}}/\overline{CS}/S_{CLK12}$ pin can be used as the $\overline{S_{RDY1}}$ pin by setting the $SC1_4$ bit to "1".

If internal clock is selected, the $P5_3$ pin can be used as the synchronization clock output pin S_{CLK12} by setting the $SIOAC_3$ bit to "1". In this case, the S_{CLK11} pin is at high impedance.

Select the function of the $P5_3/\overline{S_{RDY1}}/\overline{CS}/S_{CLK12}$ and $P5_2/S_{CLK11}$ pins by setting bit 3 ($SC1_3$), bit 4 ($SC1_4$), and bit 6 ($SC1_6$) of the serial I/O1 control register (address 0019_{16}) and bit 3 ($SIOAC_3$) of the serial I/O automatic transfer control register (address $001A_{16}$). (See Table 2.)

If using the S_{CLK11} and S_{CLK12} pins for switching, set the $P5_3/\overline{S_{RDY1}}/\overline{CS}/S_{CLK12}$ pin to $P5_3$ by setting the $SC1_4$ bit to "0", and set the $P5_3$ direction register to input mode.

Make sure that the $SIOAC_3$ bit is switched after automatic transfer is completed, while the transfer clock is still "H".

Table 2. S_{CLK11} and S_{CLK12} selection

$SC1_6$	$SC1_4$	$SC3_3$	$SIOAC_3$	$P5_2/S_{CLK11}$	$P5_3/S_{CLK12}$
1	0	1	0	S_{CLK11}	$P5_3$
			1	High impedanse	S_{CLK12}

Note. $SC1_3$: Serial I/O1 port selection bit
$SC1_4$: $\overline{S_{RDY1}}$ output selection bit
$SC1_6$: Synchronization clock selection bit
$SIOAC_3$: Synchronization clock output pin selection bit

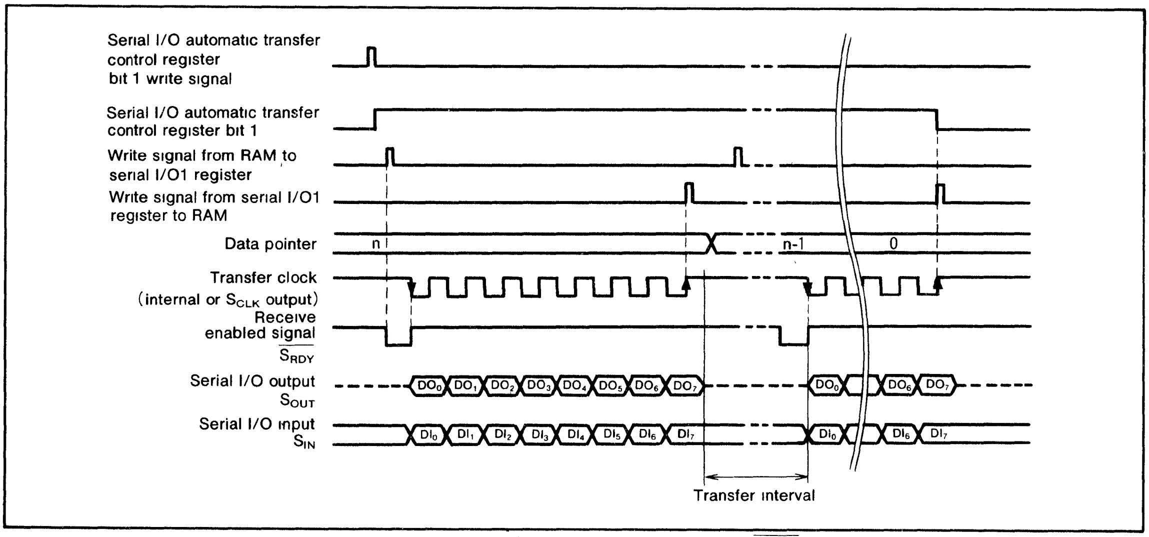


Fig. 18 Timing during serial I/O automatic transfer (internal clock selected, $\overline{S_{RDY}}$ used)

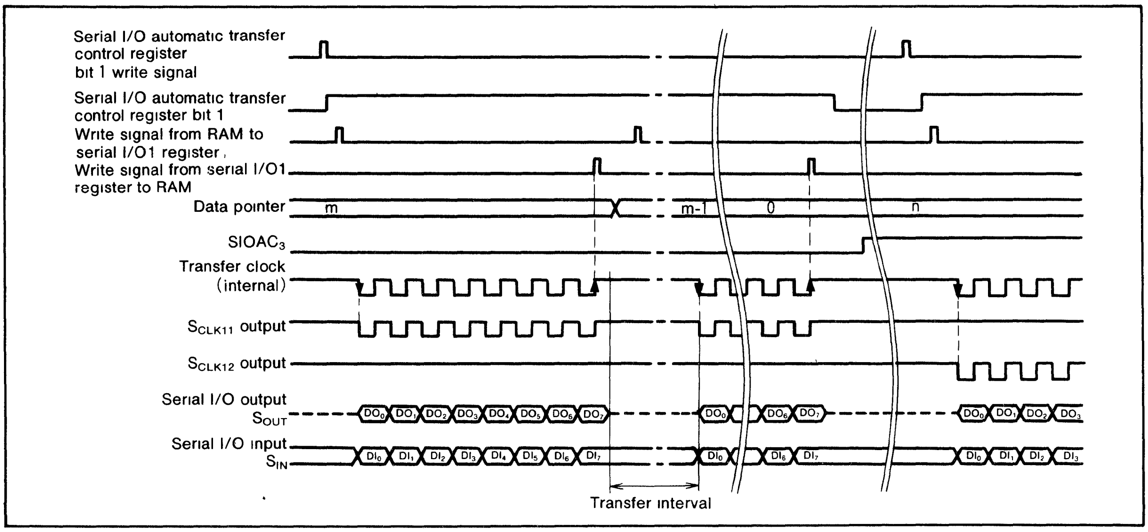


Fig. 19 Timing during serial I/O automatic transfer (internal clock selected, S_{CLK11} and S_{CLK12} used)

(2.4) If External Clock is Selected

If an external clock is selected, the internal clock and the transfer interval set by the serial I/O automatic transfer interval register are invalid, but the serial I/O output pin S_{OUT} and the internal transfer clock can be controlled from the outside by setting the $\overline{S_{RDY1}}$ and $\overline{CS}$ (input) pins.

When the $\overline{CS}$ input is "L", the S_{OUT} pin and the internal transfer clock are enabled. When the $\overline{CS}$ input is "H", the S_{OUT} pin is at high impedance and the internal transfer clock is at "H".

Select the function of the $P5_3/\overline{S_{RDY1}}/\overline{CS}/S_{CLK12}$ pin by setting bit 4 ($SC1_4$) and bit 6 ($SC1_6$) of the serial I/O1 control register (address 0019_{16}) and bit 0 ($SIOAC_0$) of the serial I/O automatic transfer control register (address $001A_{16}$).

Make sure that the $\overline{CS}$ pin switches from "L" to "H" or from "H" to "L" while the transfer clock (S_{CLK} input) is "H" after one byte of data has been transferred

If external clock is selected, make sure that the external clock goes "L" after at least nine cycles of the internal system clock ϕ after the start bit is set. Leave at least 11 cycles of the system clock ϕ free for the transfer interval after one byte of data has been transferred.

If $\overline{CS}$ input is not being used, note that the S_{OUT} pin will not go high impedance, even after transfer is completed.

If $\overline{CS}$ input is not being used, or if $\overline{CS}$ is "L", control the external clock because the data in the serial I/O register will continue to shift while the external clock is input, even after the completion of automatic transfer. (Note that the automatic transfer interrupt request bit is set and bit 1 of the automatic transfer register is cleared at the point at which the specified number of bytes of data have been transferred.)

Table 3. $P5_3/\overline{S_{RDY1}}/\overline{CS}$ selection

$SC1_6$	$SC1_4$	$SIOAC_0$	$P5_3/\overline{S_{RDY1}}/\overline{CS}$
0	0	X	$P5_3$
	1	0	$\overline{S_{RDY1}}$
		1	$\overline{CS}$

Note. $SC1_4$: $\overline{S_{RDY1}}$ output selection bit
$SC1_6$: Synchronization clock selection bit
$SIOAC_0$: Automatic transfer control bit

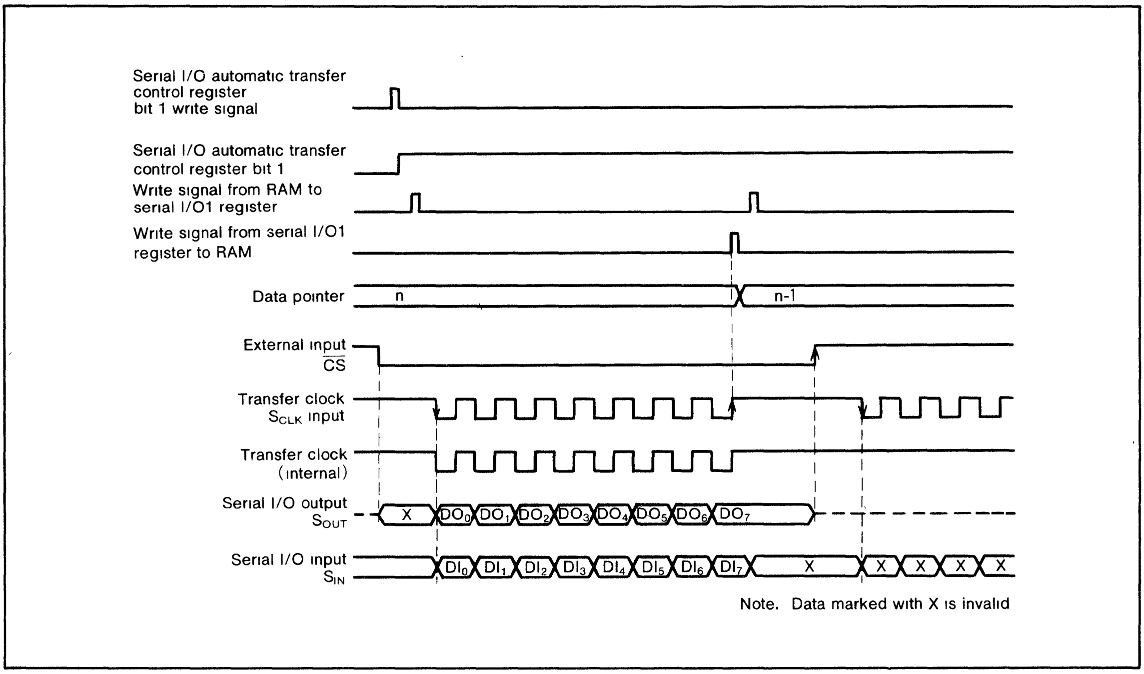


Fig. 20 Timing during serial I/O automatic transfer (external clock selected)

PULSE WIDTH MODULATION (PWM) OUTPUT CIRCUIT

Microcomputers of the M3818x group have a PWM function with a 14-bit resolution. When the oscillation frequency X_{IN} is 4MHz, the minimum resolution bit width is 500ns and the cycle period is 8192μs. The PWM timing generator supplies a PWM control signal based on a signal that is half the frequency of the X_{IN} clock.

The explanation in the rest of this data sheet assumes X_{IN}= 4MHz.

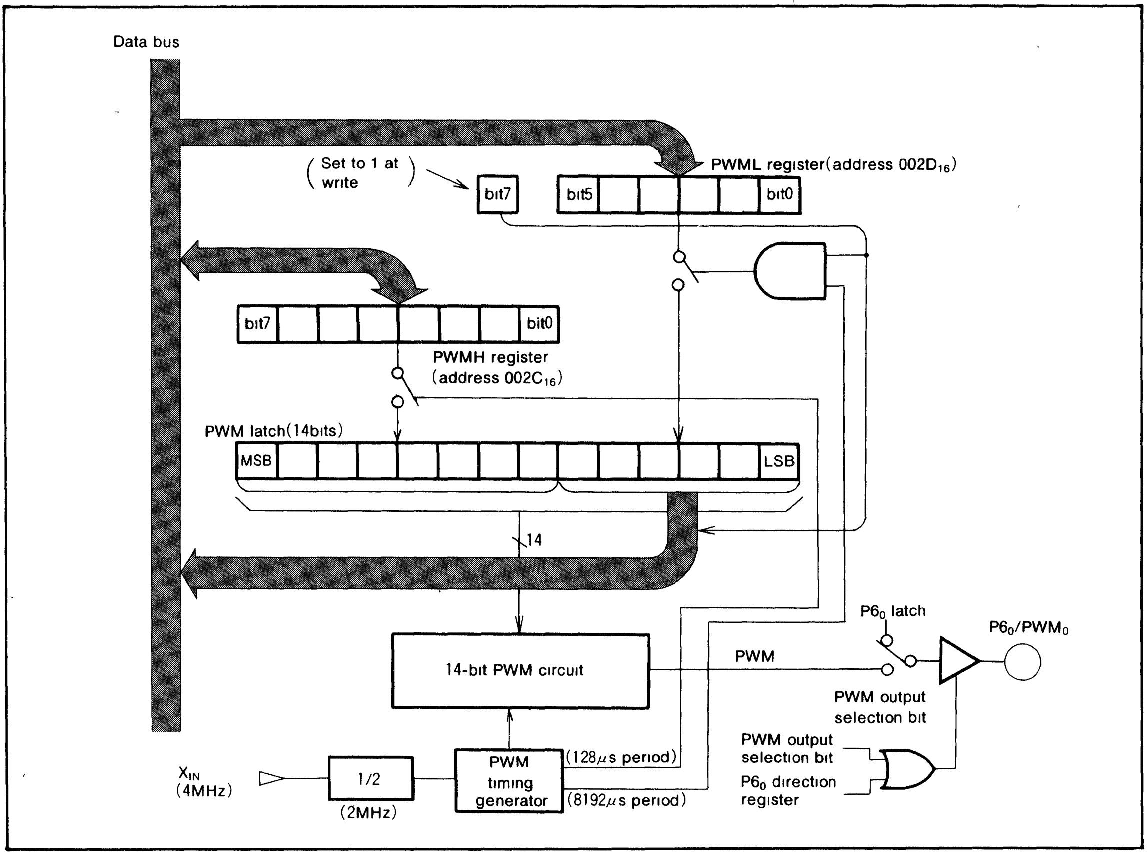


Fig. 21 PWM block diagram

(1) Data Set-up

The PWM output pin also functions as port $P6_0$. Set port $P6_0$ to be the PWM output pin by setting bit 0 of the PWM mode register (address $002B_{16}$). The upper eight bits of output data are set in the upper PWM register PWMH (address $002C_{16}$) and the lower six bits are set in the lower PWM register PWML (address $002D_{16}$).

(2) Transfer From Register to Latch

Data written to the PWML register is transferred to the PWM latch once in each PWM period (every 8192μs), and data written to the PWMH register is transferred to the PWM latch once in each sub-period (every 128μs). When the PWML register is read, the contents of the latch are read. However, bit 7 of the PWML register indicates whether the transfer to the PWM latch is completed; the transfer is completed when bit 7 is "0".

Table 4. Relationship between lower 6 bits of data and period set by the ADD bit

Lower 6 Bits of Data(PWML)	Sub-periods tm Lengthened (m =0 to 63)
0 0 0 0 0 $\overset{LSB}{0}$	None
0 0 0 0 0 1	m=32
0 0 0 0 1 0	m=16, 48
0 0 0 1 0 0	m= 8, 24, 40, 56
0 0 1 0 0 0	m= 4, 12, 20, 28, 36, 44, 52, 60
0 1 0 0 0 0	m= 2, 6, 10, 14, 18, 22, 26, 30, 34, 38, 42, 46, 50, 54, 58, 62
1 0 0 0 0 0	m= 1, 3, 5, 7, ························ ,57, 59, 61, 63

(3) PWM Operation

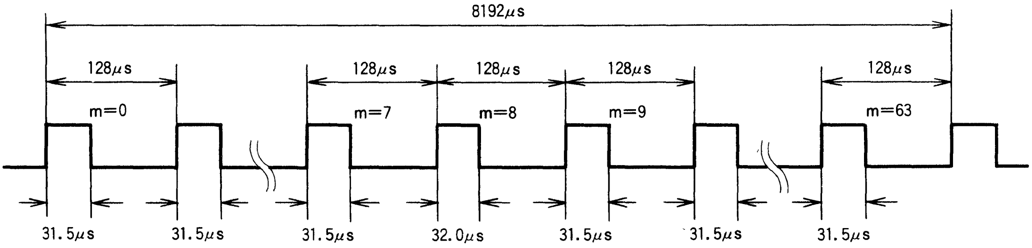
The timing of the 14-bit PWM function is shown in Fig. 24. The 14-bit PWM data is divided into the lower six bits and the upper eight bits in the PWM latch.

The upper eight bits of data determine how long an "H"-level signal is output during each sub-period. There are 64 sub-periods in each period, and each sub-period is 256× τ (128μs) long. The signal is "H" for a length equal to N times τ, where τ is the minimum resolution (500ns).

The contents of the lower six bits of data enable the lengthening of the high signal by τ (500ns). As shown in Fig. 21, the six bits of PWML determine which sub-cycles are lengthened.

As shown in Fig. 24, the leading edge of the pulse is lengthened. By changing the length of specific sub-periods instead of simply changing the "H" duration, an accurate waveform can be duplicated without the use of complex external filters.

For example, if the upper eight bits of the 14-bit data are 03_{16} and the lower six bits are 05_{16}, the length of the "H"-level output in sub-periods t_8, t_{24}, t_{32}, t_{40}, and t_{56} is 4 τ, and its length 3 τ in all other sub-periods.



Pulse width modulation register H : 00111111
Pulse width modulation register L : 000101
Sub-periods where "H" pulse width is 32μs : m=8, 24, 32, 40, 56
Sub-periods where "H" pulse width is 31.5μs : m=all other values

Fig. 22 PWM timing

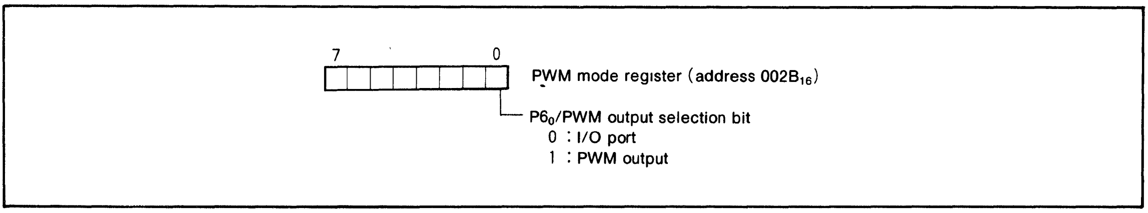


Fig. 23 Structure of PWM mode register

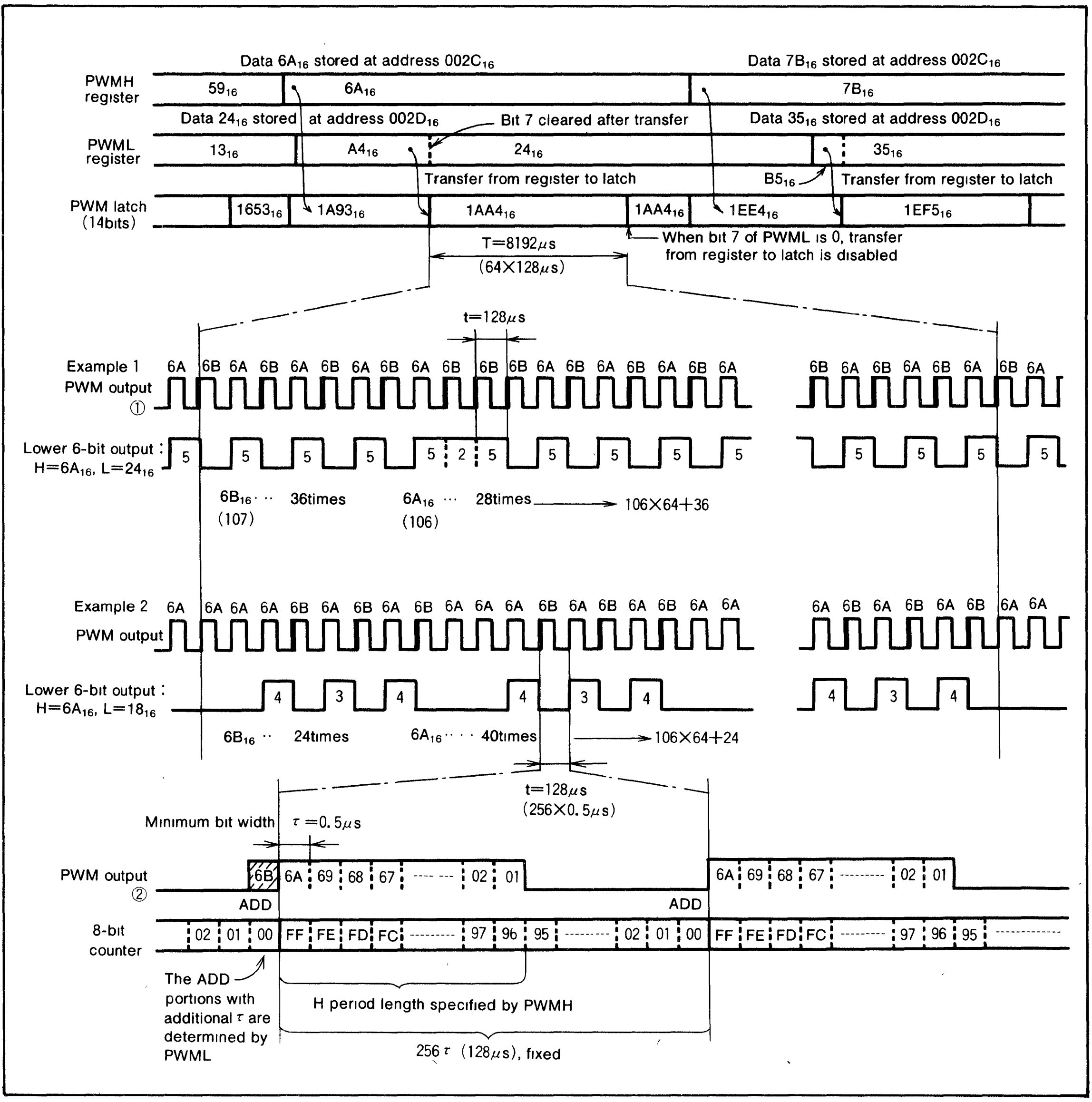


Fig. 24 14-bit PWM timing

A-D CONVERTER

The functional blocks of the A-D converter are described below.

〔A-D Conversion Register〕 AD

The A-D conversion register is a read-only register that contains the result of an A-D conversion. This register should not be read during an A-D conversion.

〔A-D Control Register〕 ADCON

The A-D control register controls the A-D conversion process. Bits 0 to 2 of this register select specific analog input pins. Bit 3 signals the completion of an A-D conversion. The value of this bit remains at "0" during an A-D conversion, then changes to "1" when the A-D conversion is completed. Writing "0" to this bit starts the A-D conversion.

〔Comparison Voltage Generator〕

The comparison voltage generator divides the voltage between AV_{SS} and V_{REF} by 256, and outputs the divided voltages.

〔Channel Selector〕

The channel selector selects one of the input ports $P7_7/AN_7$ to $P7_0/AN_0$.

〔Comparator and Control Circuit〕

The comparator and control circuit compares an analog input voltage with the comparison voltage and stores the result in the A-D conversion register. When an A-D conversion is complete, the control circuit sets the A-D conversion completion bit and the A-D interrupt request bit to "1".
Note that the comparator is constructed linked to a capacitor, so set f (X_{IN}) to at least 500kHz during A-D conversion.

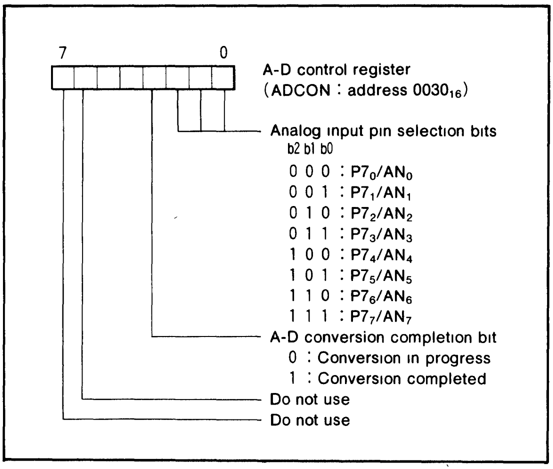


Fig. 25 Structure of A-D control register

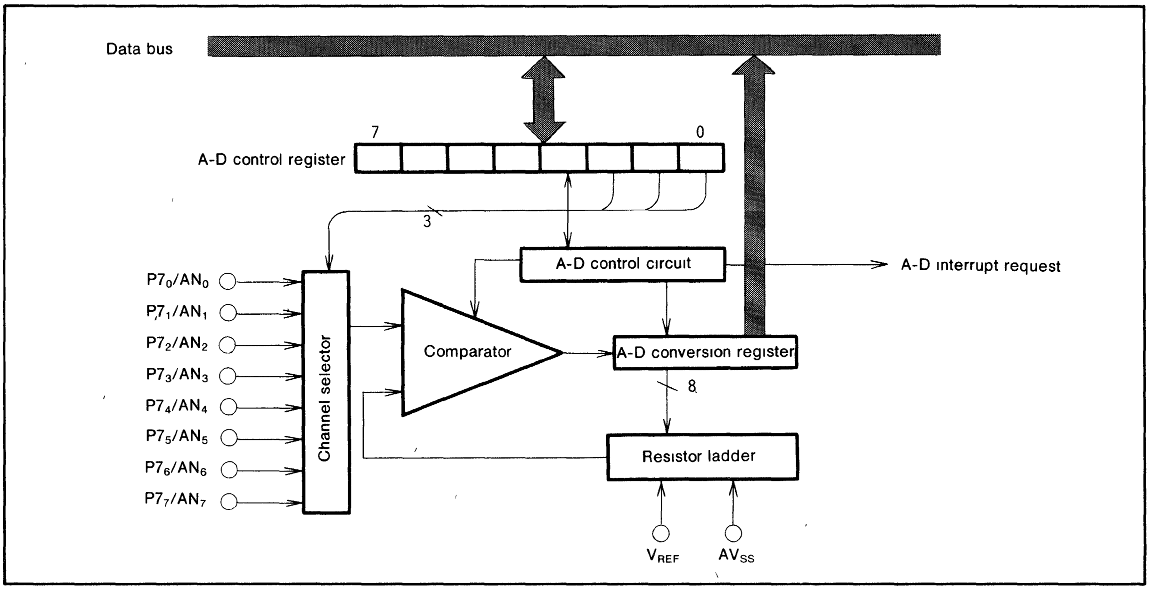


Fig. 26 A-D converter block diagram

FLD CONTROLLER

Microcomputers of the M3818x group have fluorescent display (FLD) drive and control circuits.

The FLD controller consists of the following components:

- 24 pins for segments
- 16 pins for digits
- FLDC mode register
- FLD data pointer
- FLD data pointer reload register
- Port P3 segment/digit switching register
- Port P0 digit/port switching register
- Port P8 segment/port switching register
- Key-scan blanking register
- 48-byte FLD automatic display RAM

Eight to twenty-four pins can be used as segment pins and four to sixteen pins can be used as digit pins.

Note that only 32 pins (maximum) can be used as segment and digit pins.

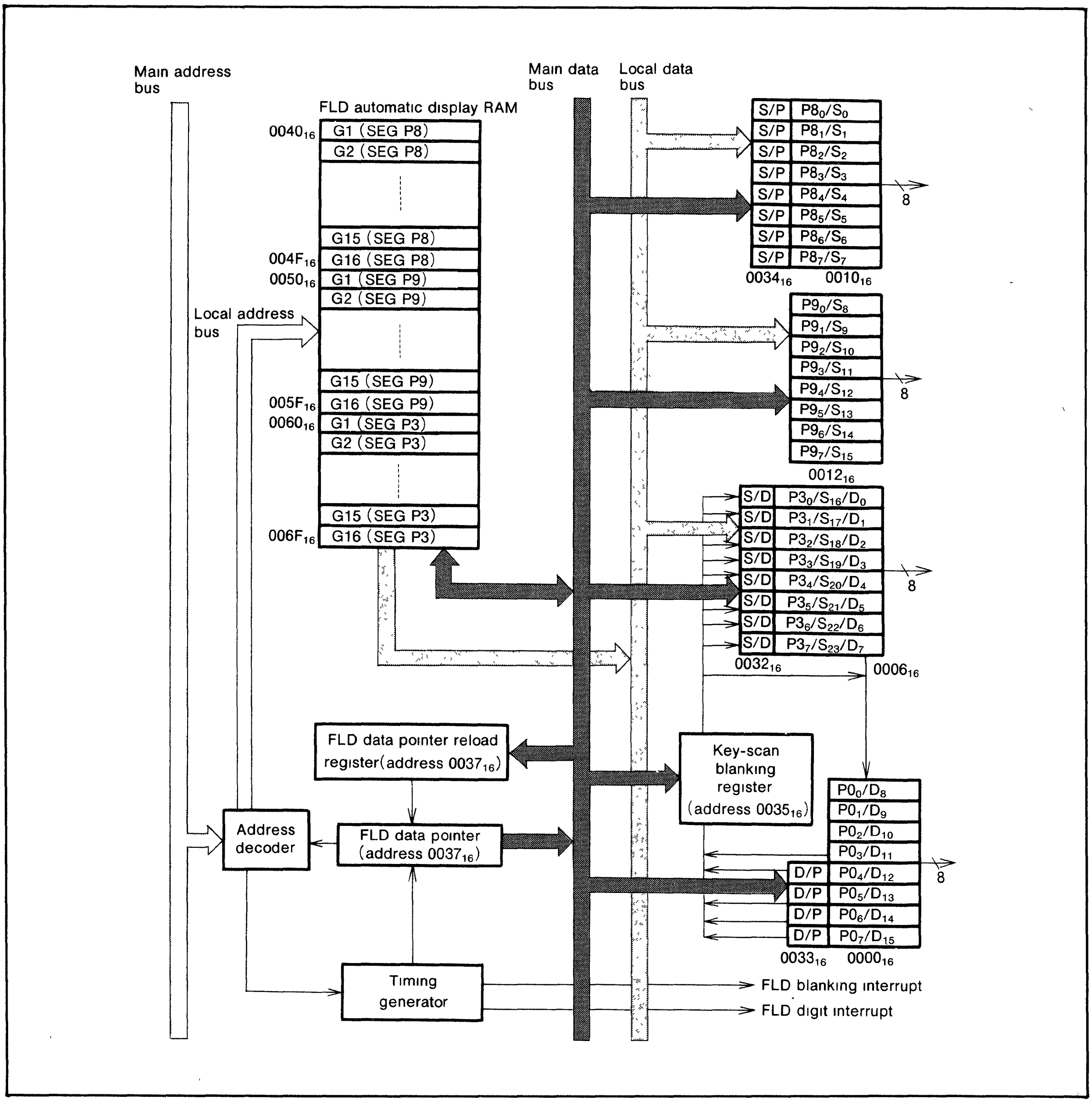


Fig. 27 FLD control circuit block diagram

FLDC Mode Register (FLDM)

The FLDC mode register (address 0036_{16}) is a seven bit control register which is used to control the FLD automatic display.

Key-scan Blanking Register .(KSCN)

The key-scan blanking register (address 0035_{16}) is a two bit register which sets the blanking period T_{scan} between the last digit and the first digit of the next cycle.

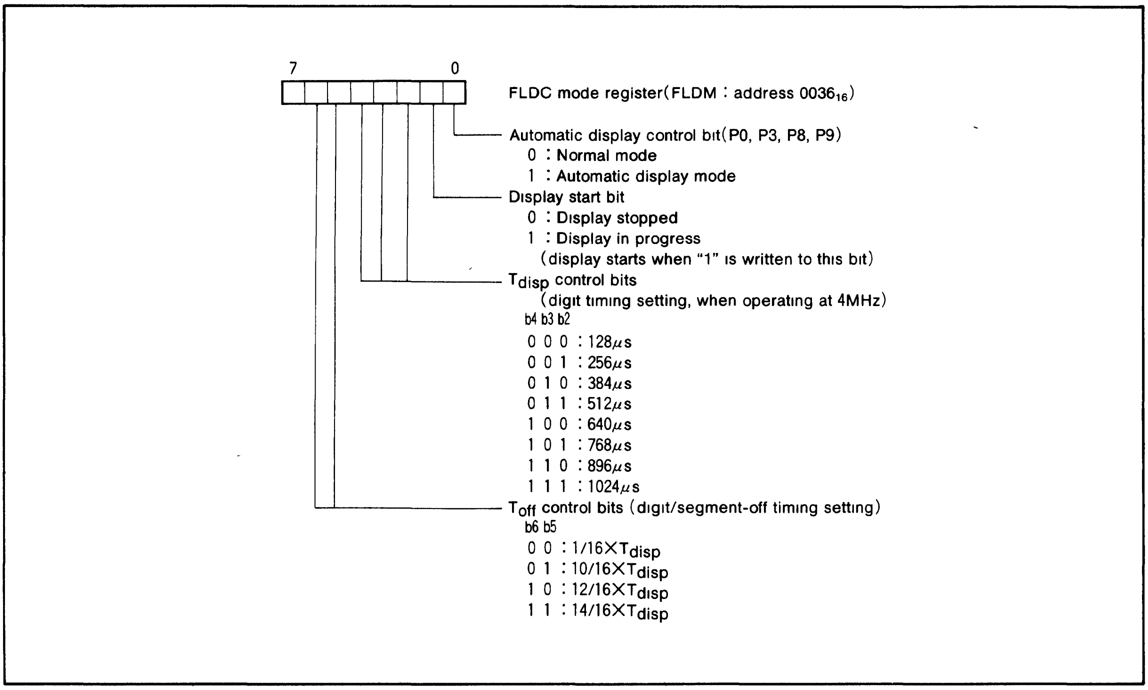


Fig. 28 Structure of FLDC mode register (FLDM)

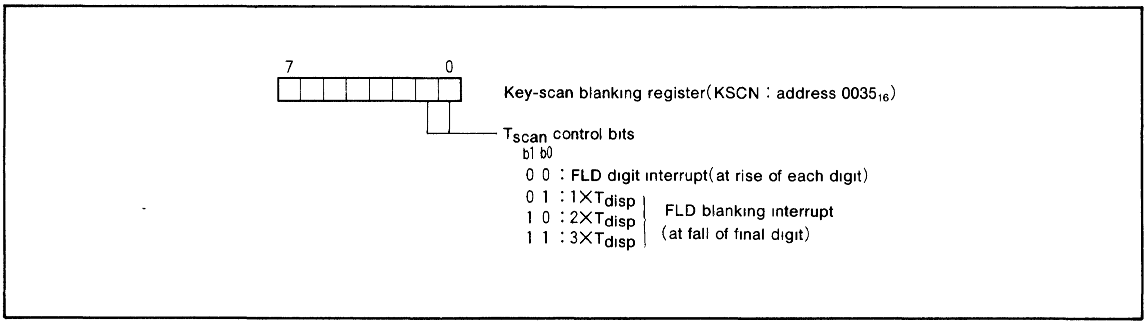


Fig. 29 Structure of key-scan blanking register (KSCN)

FLD Automatic Display Pins

The FLD automatic display function of Ports P3, P0, P9, and P8 is selected by setting the automatic display control bit of the FLDC mode register (address 0036_{16}) to "1".

When using the FLD automatic display mode, set the number of segments and digits for each port.

Table 5. Pins in FLD automatic display mode

Port Name	Automatic Display Pins	Setting Method
$P8_0$-$P8_7$	SEG_0-SEG_7 or $P8_0$-$P8_7$	The individual bits of the segment/port switching register (address 0034_{16}) can be used to set each pin to either segment ("1") or normal port input ("0")
$P9_0$-$P9_7$	SEG_8-SEG_{15}	None (segment only)
$P3_0$-$P3_7$	SEG_{16}-SEG_{23} or DIG_0-DIG_7	The individual bits of the segment/digit switching register (address 0032_{16}) can be used to set each pin to segment ("1") or digit ("0") (Note)
$P0_0$-$P0_3$	DIG_8-DIG_{11}	None (digit only)
$P0_4$-$P0_7$	DIG_{12}-DIG_{15} or $P0_4$-$P0_7$	The individual bits of the digit/port switching register (address 0033_{16}) can be used to set each pin to digit ("1") or normal port output ("0") (Note)

Note. Always set digits in sequence

Number of segments		16		8		16		24		16
Number of digits		4		12		10		8		16
Port P8 (has segment/port switching register)	0	$P8_0$	0	$P8_0$	0	$P8_0$	1	SEG_0	1	SEG_0
	0	$P8_1$	0	$P8_1$	0	$P8_1$	1	SEG_1	1	SEG_1
	0	$P8_2$	0	$P8_2$	0	$P8_2$	1	SEG_2	1	SEG_2
	0	$P8_3$	0	$P8_3$	0	$P8_3$	1	SEG_3	1	SEG_3
	0	$P8_4$	0	$P8_4$	1	SEG_4	1	SEG_4	1	SEG_4
	0	$P8_5$	0	$P8_5$	1	SEG_5	1	SEG_5	1	SEG_5
	0	$P8_6$	0	$P8_6$	1	SEG_6	1	SEG_6	1	SEG_6
	0	$P8_7$	0	$P8_7$	1	SEG_7	1	SEG_7	1	SEG_7
Port P9 (segment only)		SEG_8		SEG_8		SEG_8		SEG_8		SEG_8
		SEG_9		SEG_9		SEG_9		SEG_9		SEG_9
		SEG_{10}		SEG_{10}		SEG_{10}		SEG_{10}		SEG_{10}
		SEG_{11}		SEG_{11}		SEG_{11}		SEG_{11}		SEG_{11}
		SEG_{12}		SEG_{12}		SEG_{12}		SEG_{12}		SEG_{12}
		SEG_{13}		SEG_{13}		SEG_{13}		SEG_{13}		SEG_{13}
		SEG_{14}		SEG_{14}		SEG_{14}		SEG_{14}		SEG_{14}
		SEG_{15}		SEG_{15}		SEG_{15}		SEG_{15}		SEG_{15}
Port P3 (has segment/digit switching register)	1	SEG_{16}	0	DIG_0 →G12	1	SEG_{16}	1	SEG_{16}	0	DIG_0 →G16
	1	SEG_{17}	0	DIG_1 →G11	1	SEG_{17}	1	SEG_{17}	0	DIG_1 →G15
	1	SEG_{18}	0	DIG_2 →G10	1	SEG_{18}	1	SEG_{18}	0	DIG_2 →G14
	1	SSG_{19}	0	DIG_3 →G9	1	SEG_{19}	1	SEG_{19}	0	DIG_3 →G13
	1	SEG_{20}	0	DIG_4 →G8	0	DIG_4 →G10	1	SEG_{20}	0	DIG_4 →G12
	1	SEG_{21}	0	DIG_5 →G7	0	DIG_5 →G9	1	SEG_{21}	0	DIG_5 →G11
	1	SEG_{22}	0	DIG_6 →G6	0	DIG_6 →G8	1	SEG_{22}	0	DIG_6 →G10
	1	SEG_{23}	0	DIG_7 →G5	0	DIG_7 →G7	1	SEG_{23}	0	DIG_7 →G9
Port P0 (has digit/port switching register)		DIG_8 →G4		DIG_8 →G4		DIG_8 →G6		DIG_8 →G8		DIG_8 →G8
		DIG_9 →G3		DIG_9 →G3		DIG_9 →G5		DIG_9 →G7		DIG_9 →G7
		DIG_{10} →G2		DIG_{10} →G2		DIG_{10} →G4		DIG_{10} →G6		DIG_{10} →G6
		DIG_{11} →G1		DIG_{11} →G1		DIG_{11} →G3		DIG_{11} →G5		DIG_{11} →G5
	0	$P0_4$	0	$P0_4$	1	DIG_{12} →G2	1	DIG_{12} →G4	1	DIG_{12} →G4
	0	$P0_5$	0	$P0_5$	1	DIG_{13} →G1	1	DIG_{13} →G3	1	DIG_{13} →G3
	0	$P0_6$	0	$P0_6$	0	$P0_6$	1	DIG_{14} →G2	1	DIG_{14} →G2
	0	$P0_7$	0	$P0_7$	0	$P0_7$	1	DIG_{15} →G1	1	DIG_{15} →G1

Fig. 30 Segment/digit setting example

FLD Automatic Display RAM

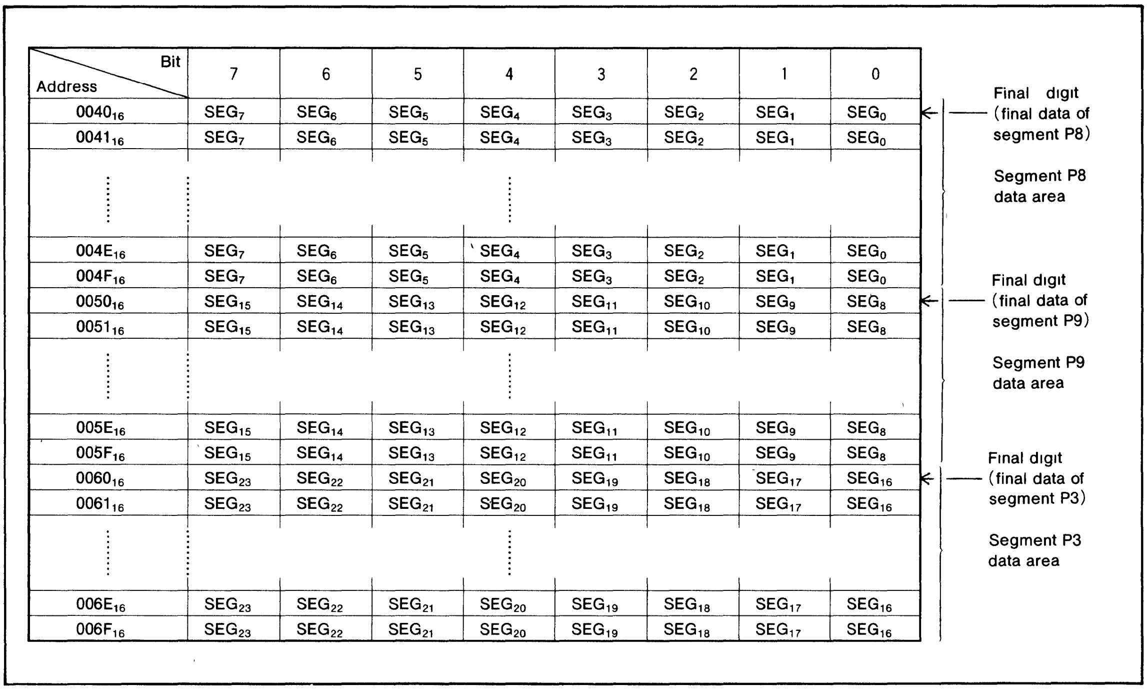
The FLD automatic display RAM area is the 48 bytes from addresses 0040_{16} to $006F_{16}$. The FLD automatic display RAM area can be used to store 3-byte data items for a maximum of 16 digits. Addresses 0040_{16} to $004F_{16}$ are used for P8 segment data, addresses 0050_{16} to $005F_{16}$ are used for P9 segment data, and addresses 0060_{16} to $006F_{16}$ are used for P3 segment data.

- **FLD Data Pointer and FLD Data Pointer Reload Register**
  The FLD data pointer indicates the data address in the FLD automatic display RAM to be transferred to a segment, and the FLD data pointer reload register indicates the address of the first digit of segment P9.

Both the FLD data pointer and the FLD data pointer reload register are allocated to address 0037_{16} and are 6-bits wide. Data written to this address is written to the FLD data pointer reload register, data read from this address is read from the FLD data pointer.

The actual memory address is the value of the data pointer plus 40_{16}, 50_{16}, or 60_{16}.

The contents of the FLD data pointer indicate the start address of segment P9 at the start of automatic display. If segment P3 or P9 data is transferred to the segment, the FLD data pointer returns − 16; if segment P8 data is transferred, it returns + 31. After it reaches "00", the value in the FLD data pointer reload register is transferred to the FLD data pointer. In this way, three bytes of data for the P3, P9, and P8 segments of one digit are transferred.



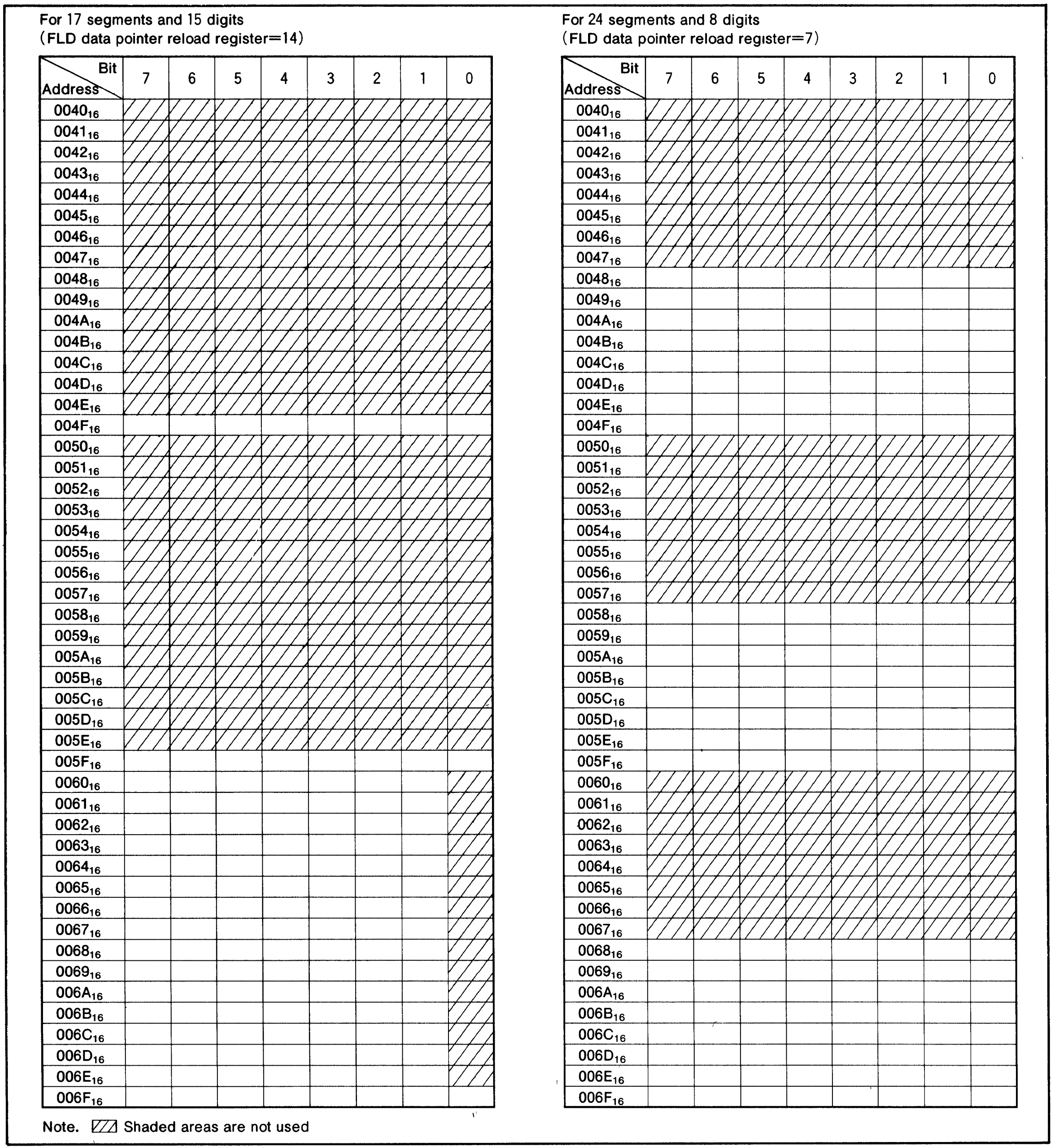
Address \ Bit	7	6	5	4	3	2	1	0
0040_{16}	SEG_7	SEG_6	SEG_5	SEG_4	SEG_3	SEG_2	SEG_1	SEG_0
0041_{16}	SEG_7	SEG_6	SEG_5	SEG_4	SEG_3	SEG_2	SEG_1	SEG_0
⋮	⋮			⋮				
$004E_{16}$	SEG_7	SEG_6	SEG_5	SEG_4	SEG_3	SEG_2	SEG_1	SEG_0
$004F_{16}$	SEG_7	SEG_6	SEG_5	SEG_4	SEG_3	SEG_2	SEG_1	SEG_0
0050_{16}	SEG_{15}	SEG_{14}	SEG_{13}	SEG_{12}	SEG_{11}	SEG_{10}	SEG_9	SEG_8
0051_{16}	SEG_{15}	SEG_{14}	SEG_{13}	SEG_{12}	SEG_{11}	SEG_{10}	SEG_9	SEG_8
⋮	⋮			⋮				
$005E_{16}$	SEG_{15}	SEG_{14}	SEG_{13}	SEG_{12}	SEG_{11}	SEG_{10}	SEG_9	SEG_8
$005F_{16}$	SEG_{15}	SEG_{14}	SEG_{13}	SEG_{12}	SEG_{11}	SEG_{10}	SEG_9	SEG_8
0060_{16}	SEG_{23}	SEG_{22}	SEG_{21}	SEG_{20}	SEG_{19}	SEG_{18}	SEG_{17}	SEG_{16}
0061_{16}	SEG_{23}	SEG_{22}	SEG_{21}	SEG_{20}	SEG_{19}	SEG_{18}	SEG_{17}	SEG_{16}
⋮	⋮			⋮				
$006E_{16}$	SEG_{23}	SEG_{22}	SEG_{21}	SEG_{20}	SEG_{19}	SEG_{18}	SEG_{17}	SEG_{16}
$006F_{16}$	SEG_{23}	SEG_{22}	SEG_{21}	SEG_{20}	SEG_{19}	SEG_{18}	SEG_{17}	SEG_{16}

Fig. 31 FLD automatic display RAM and bit allocation

- **Data Setup**

When data is stored in the FLD automatic display RAM, the end of segment P8 data is stored at address 0040_{16}, the end of segment P9 data is stored at address 0050_{16}, and the end of segment P3 data is stored at address 0060_{16}. The head of each of the segment P8, P9, and P3 data is stored at an address that is the number of digits−1 away from the corresponding address 0040_{16}, 0050_{16}, 0060_{16}.

Set the FLD data pointer reload register to the value given by the number of digits−1. "1" is always written to bit 5, and "0" is always written to bit 4. Note that "0" is always read from bit 5 or 4 during a read.



For 17 segments and 15 digits
(FLD data pointer reload register=14)

Address \ Bit	7	6	5	4	3	2	1	0
0040_{16}	▨	▨	▨	▨	▨	▨	▨	▨
0041_{16}	▨	▨	▨	▨	▨	▨	▨	▨
0042_{16}	▨	▨	▨	▨	▨	▨	▨	▨
0043_{16}	▨	▨	▨	▨	▨	▨	▨	▨
0044_{16}	▨	▨	▨	▨	▨	▨	▨	▨
0045_{16}	▨	▨	▨	▨	▨	▨	▨	▨
0046_{16}	▨	▨	▨	▨	▨	▨	▨	▨
0047_{16}	▨	▨	▨	▨	▨	▨	▨	▨
0048_{16}	▨	▨	▨	▨	▨	▨	▨	▨
0049_{16}	▨	▨	▨	▨	▨	▨	▨	▨
$004A_{16}$	▨	▨	▨	▨	▨	▨	▨	▨
$004B_{16}$	▨	▨	▨	▨	▨	▨	▨	▨
$004C_{16}$	▨	▨	▨	▨	▨	▨	▨	▨
$004D_{16}$	▨	▨	▨	▨	▨	▨	▨	▨
$004E_{16}$	▨	▨	▨	▨	▨	▨	▨	▨
$004F_{16}$								
0050_{16}	▨	▨	▨	▨	▨	▨	▨	▨
0051_{16}	▨	▨	▨	▨	▨	▨	▨	▨
0052_{16}	▨	▨	▨	▨	▨	▨	▨	▨
0053_{16}	▨	▨	▨	▨	▨	▨	▨	▨
0054_{16}	▨	▨	▨	▨	▨	▨	▨	▨
0055_{16}	▨	▨	▨	▨	▨	▨	▨	▨
0056_{16}	▨	▨	▨	▨	▨	▨	▨	▨
0057_{16}	▨	▨	▨	▨	▨	▨	▨	▨
0058_{16}	▨	▨	▨	▨	▨	▨	▨	▨
0059_{16}	▨	▨	▨	▨	▨	▨	▨	▨
$005A_{16}$	▨	▨	▨	▨	▨	▨	▨	▨
$005B_{16}$	▨	▨	▨	▨	▨	▨	▨	▨
$005C_{16}$	▨	▨	▨	▨	▨	▨	▨	▨
$005D_{16}$	▨	▨	▨	▨	▨	▨	▨	▨
$005E_{16}$	▨	▨	▨	▨	▨	▨	▨	▨
$005F_{16}$								
0060_{16}								▨
0061_{16}								▨
0062_{16}								▨
0063_{16}								▨
0064_{16}								▨
0065_{16}								▨
0066_{16}								▨
0067_{16}								▨
0068_{16}								▨
0069_{16}								▨
$006A_{16}$								▨
$006B_{16}$								▨
$006C_{16}$								▨
$006D_{16}$								▨
$006E_{16}$								▨
$006F_{16}$								

For 24 segments and 8 digits
(FLD data pointer reload register=7)

Address \ Bit	7	6	5	4	3	2	1	0
0040_{16}	▨	▨	▨	▨	▨	▨	▨	▨
0041_{16}	▨	▨	▨	▨	▨	▨	▨	▨
0042_{16}	▨	▨	▨	▨	▨	▨	▨	▨
0043_{16}	▨	▨	▨	▨	▨	▨	▨	▨
0044_{16}	▨	▨	▨	▨	▨	▨	▨	▨
0045_{16}	▨	▨	▨	▨	▨	▨	▨	▨
0046_{16}	▨	▨	▨	▨	▨	▨	▨	▨
0047_{16}	▨	▨	▨	▨	▨	▨	▨	▨
0048_{16}								
0049_{16}								
$004A_{16}$								
$004B_{16}$								
$004C_{16}$								
$004D_{16}$								
$004E_{16}$								
$004F_{16}$								
0050_{16}	▨	▨	▨	▨	▨	▨	▨	▨
0051_{16}	▨	▨	▨	▨	▨	▨	▨	▨
0052_{16}	▨	▨	▨	▨	▨	▨	▨	▨
0053_{16}	▨	▨	▨	▨	▨	▨	▨	▨
0054_{16}	▨	▨	▨	▨	▨	▨	▨	▨
0055_{16}	▨	▨	▨	▨	▨	▨	▨	▨
0056_{16}	▨	▨	▨	▨	▨	▨	▨	▨
0057_{16}	▨	▨	▨	▨	▨	▨	▨	▨
0058_{16}								
0059_{16}								
$005A_{16}$								
$005B_{16}$								
$005C_{16}$								
$005D_{16}$								
$005E_{16}$								
$005F_{16}$								
0060_{16}	▨	▨	▨	▨	▨	▨	▨	▨
0061_{16}	▨	▨	▨	▨	▨	▨	▨	▨
0062_{16}	▨	▨	▨	▨	▨	▨	▨	▨
0063_{16}	▨	▨	▨	▨	▨	▨	▨	▨
0064_{16}	▨	▨	▨	▨	▨	▨	▨	▨
0065_{16}	▨	▨	▨	▨	▨	▨	▨	▨
0066_{16}	▨	▨	▨	▨	▨	▨	▨	▨
0067_{16}	▨	▨	▨	▨	▨	▨	▨	▨
0068_{16}								
0069_{16}								
$006A_{16}$								
$006B_{16}$								
$006C_{16}$								
$006D_{16}$								
$006E_{16}$								
$006F_{16}$								

Note. ▨ Shaded areas are not used

Fig. 32 Example of using the FLD automatic display RAM.

- **Timing Setting**

The digit timing (T_{disp}) and digit/segment turn-off timing (T_{off}) can be set by the FLDC mode register (address 0036_{16}). The scan timing (T_{scan}) can be set by the key-scan blanking register (address 0035_{16}).
Note that flickering will occur if the repetition frequency ($1/(T_{disp} \times$ number of digits$+T_{scan})$) is an integral multiple of the digit timing T_{disp}.

- **FLD Start**

To perform FLD automatic display, you have to use the following registers.
  - Port P3 segment/digit switching register
  - Port P0 digit/port switching register
  - Port P8 segment/port switching register
  - Key-scan blanking register
  - FLDC mode register
  - FLD data pointer

Automatic display mode is activated by writing "1" to bit 0 of the FLDC mode register (address 0036_{16}), and the automatic display is started by writing "1" to bit 1.
During automatic display bit 1 always keeps "1", automatic display can be interrupted by writing "0" to bit 1.

If key-scan is to be performed by segment during the key-scan blanking period T_{scan},
1. Write "0" to bit 0 (automatic display control bit) of FLDC mode register (address 0036_{16}).
2. Set the port corresponding to the segment to the normal port.
3. After the key-scan is performed, write "1" (automatic display mode) to bit 0 of FLDC mode register (address 0036_{16}).

Note on performance of key-scan in the above 1 to 3 order.
1. Do not write "0" to bit 1 of FLDC mode register (address 0036_{16}).
2. Do not write "1" to the port corresponding to the digit.

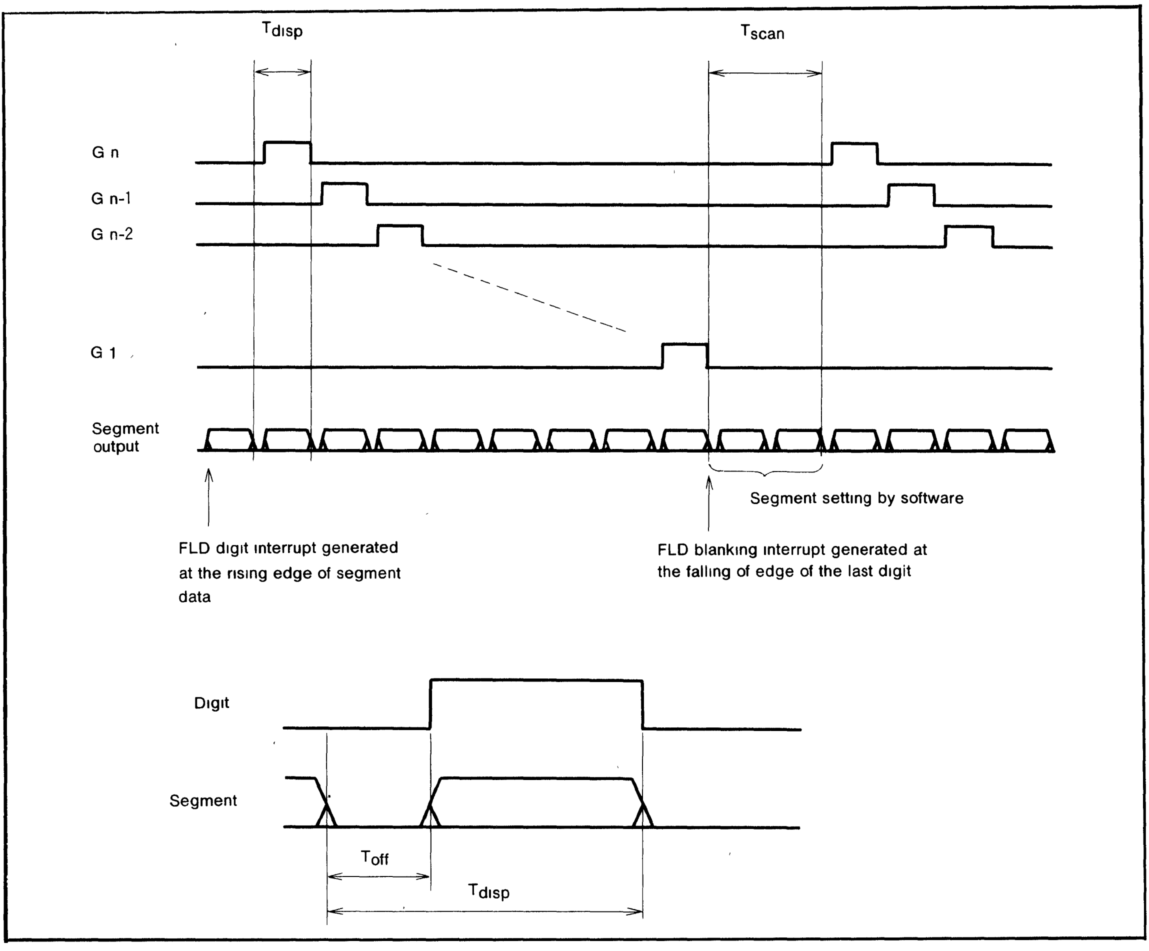
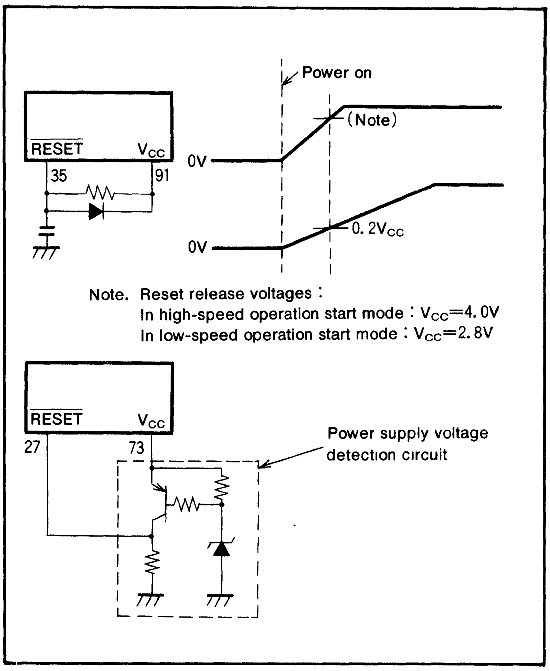


Fig. 33 FLDC timing

RESET CIRCUIT

After a reset, the microcomputer will start in high-speed operation start mode or low-speed operation start mode depending on a mask-programmable option.

- **High-Speed Operation Start Mode**
  In high-speed operation start mode, reset occurs if the $\overline{\text{RESET}}$ pin is held at an "L" level for at least 2µs then is returned to an "H" level (the power supply voltage should be between 4.0V and 5.5V). Both the X_{IN} and the X_{CIN} clocks begin oscillating. In order to give the X_{IN} clock time to stabilize, internal operation does not begin until after 13 X_{IN} clock cycles are complete. After the reset is completed, the program starts from the address contained in address $FFFD_{16}$ (upper byte) and address $FFFC_{16}$ (lower byte).
- **Low-Speed Operation Start Mode**
  In low-speed operation start mode, reset occurs if the $\overline{\text{RESET}}$ pin is held at an "L" level for at least 2µs then is returned to an "H" level (the power supply voltage should be between 2.8V and 5.5V). The X_{IN} clock does not begin oscillating. In order to give the X_{CIN} time to stabilize, timer 1 and timer 2 are connected together and 512 cycles of the $X_{CIN}/16$ are counted before internal operation begins. After the reset is completed, the program starts from the address contained in address $FFFD_{16}$ (upper byte) and address $FFFC_{16}$ (lower byte).
  If the X_{CIN} clock is stable, reset will complete after approximately 250ms (assuming $f(X_{CIN})=32.768kHz$).
  Immediately after a power-on, the stability of the clock circuit will determine the reset timing and will vary according to the characteristics of the oscillation circuit used.
- **Note on Use**
  Make sure that the reset input voltage is no more than 0.8V in high-speed operation start mode, or no more than 0.5V in low-speed operation start mode.



Note. Reset release voltages :
In high-speed operation start mode : $V_{CC}=4.0V$
In low-speed operation start mode : $V_{CC}=2.8V$

Fig. 34 Power-on reset circuit example

		Address	Register contents
(1)	Port P0 register	(0 0 0 0$_{16}$)···	00$_{16}$
(2)	Port P1 register	(0 0 0 2$_{16}$)···	00$_{16}$
(3)	Port P1 direction register	(0 0 0 3$_{16}$)···	00$_{16}$
(4)	Port P2 register	(0 0 0 4$_{16}$)···	00$_{16}$
(5)	Port P2 direction register	(0 0 0 5$_{16}$)···	00$_{16}$
(6)	Port P3 register	(0 0 0 6$_{16}$)···	00$_{16}$
(7)	Port P4 register	(0 0 0 8$_{16}$)···	00$_{16}$
(8)	Port P4 direction register	(0 0 0 9$_{16}$)···	00$_{16}$
(9)	Port P5 register	(0 0 0 A$_{16}$)···	00$_{16}$
(10)	Port P5 direction register	(0 0 0 B$_{16}$)···	00$_{16}$
(11)	Port P6 register	(0 0 0 C$_{16}$)···	00$_{16}$
(12)	Port P6 direction register	(0 0 0 D$_{16}$)···	00$_{16}$
(13)	Port P7 register	(0 0 0 E$_{16}$)···	00$_{16}$
(14)	Port P7 direction register	(0 0 0 F$_{16}$)···	00$_{16}$
(15)	Port P8 register	(0 0 1 0$_{16}$)···	00$_{16}$
(16)	Port P8 direction register	(0 0 1 1$_{16}$)···	00$_{16}$
(17)	Port P9 register	(0 0 1 2$_{16}$)···	00$_{16}$
(18)	Port P9 direction register	(0 0 1 3$_{16}$)···	00$_{16}$
(19)	Port PA register	(0 0 1 4$_{16}$)···	00$_{16}$
(20)	Port PA direction register	(0 0 1 5$_{16}$)···	00$_{16}$
(21)	Serial I/O1 control register	(0 0 1 9$_{16}$)···	00$_{16}$
(22)	Serial I/O automatic transfer control register	(0 0 1 A$_{16}$)···	00$_{16}$
(23)	Serial I/O automatic transfer interval register	(0 0 1 C$_{16}$)···	00$_{16}$
(24)	Serial I/O2 control register	(0 0 1 D$_{16}$)···	00$_{16}$
(25)	Timer 1 register	(0 0 2 0$_{16}$)···	FF$_{16}$
(26)	Timer 2 register	(0 0 2 1$_{16}$)···	01$_{16}$
(27)	Timer 3 register	(0 0 2 2$_{16}$)···	FF$_{16}$
(28)	Timer 4 register	(0 0 2 3$_{16}$)···	FF$_{16}$
(29)	Timer 5 register	(0 0 2 4$_{16}$)···	FF$_{16}$
(30)	Timer 6 register	(0 0 2 5$_{16}$)···	FF$_{16}$
(31)	Timer 12 mode register	(0 0 2 8$_{16}$)···	00$_{16}$
(32)	Timer 34 mode register	(0 0 2 9$_{16}$)···	00$_{16}$
(33)	Timer 56 mode register	(0 0 2 A$_{16}$)···	00$_{16}$
(34)	PWM control register	(0 0 2 B$_{16}$)···	00$_{16}$
(35)	A-D control register	(0 0 3 0$_{16}$)···	08$_{16}$
(36)	Port P3 segment/digit switching register	(0 0 3 2$_{16}$)···	00$_{16}$
(37)	Port P0 digit/port switching register	(0 0 3 3$_{16}$)···	00$_{16}$
(38)	Port P8 segment/port switching register	(0 0 3 4$_{16}$)···	00$_{16}$
(39)	Key-scan blanking register	(0 0 3 5$_{16}$)···	00$_{16}$
(40)	FLDC mode register	(0 0 3 6$_{16}$)···	00$_{16}$
(41)	High-breakdown-voltage port control register	(0 0 3 8$_{16}$)···	00$_{16}$
(42)	Interrupt edge selection register	(0 0 3 A$_{16}$)···	00$_{16}$
(43)	CPU mode register	(0 0 3 B$_{16}$)···	* * 1 0 0 0 0 0
(44)	Interrupt request register 1	(0 0 3 C$_{16}$)···	00$_{16}$
(45)	Interrupt request register 2	(0 0 3 D$_{16}$)···	00$_{16}$
(46)	Interrupt control register 1	(0 0 3 E$_{16}$)···	00$_{16}$
(47)	Interrupt control register 2	(0 0 3 F$_{16}$)···	00$_{16}$
(48)	Processor status register	(P S)···	X X X X X 1 X X
(49)	Program counter	(P C$_H$)···	Contents of address FFFD$_{16}$
		(P C$_L$)···	Contents of address FFFC$_{16}$

Note. * : The initial values of bits 7 and 6 of the CPU mode register are determined by a mask option
X : Underfined
The contents of all other registers and RAM are undefined after a reset, so programs must set their initial values

Fig. 35 Internal status at reset

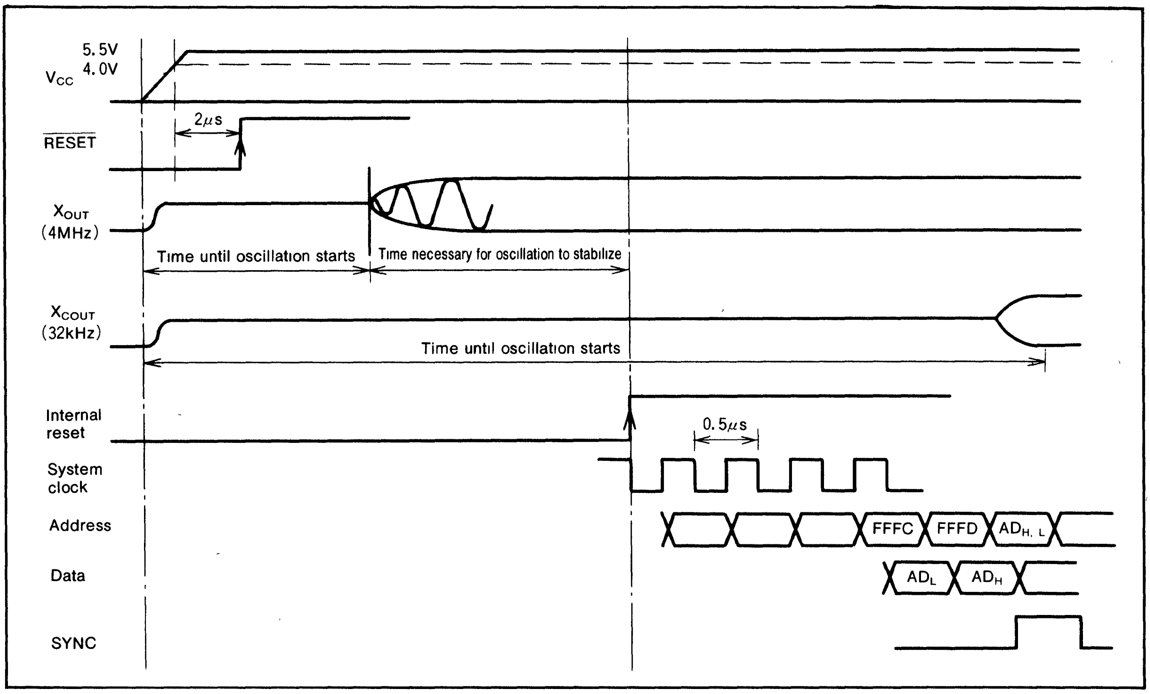


Fig. 36 Reset sequence in high-speed operation mode

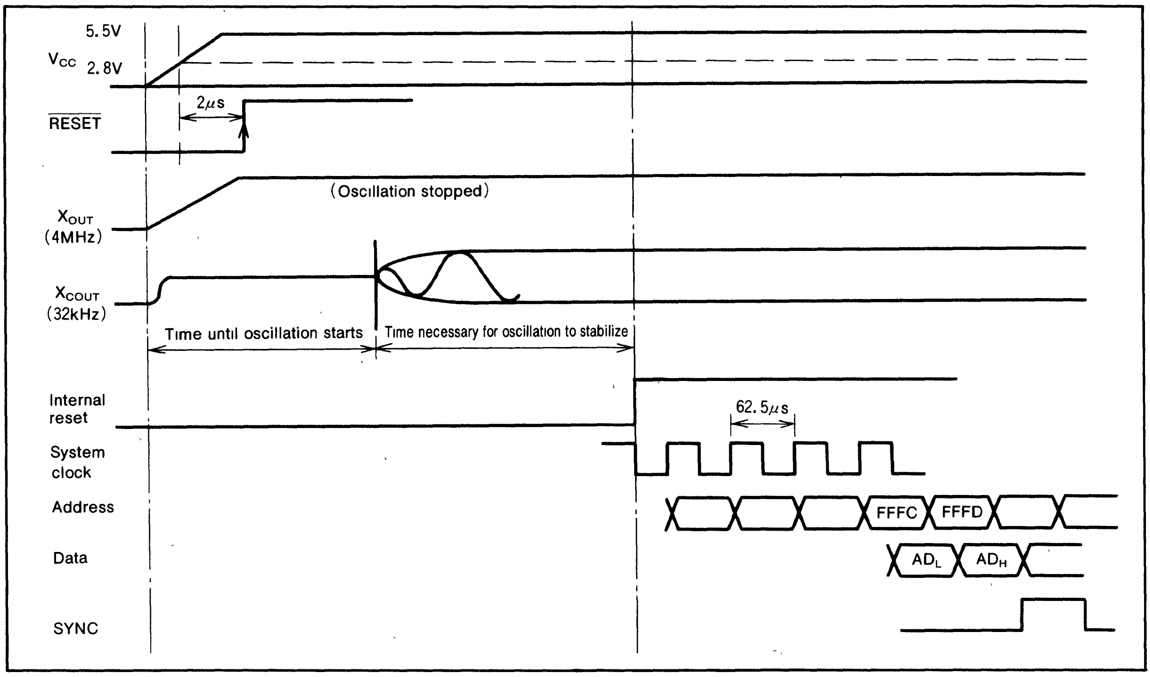


Fig. 37 Reset sequence in low-speed operation mode

CLOCK GENERATION CIRCUIT

When using an external clock signal, input the clock signal to the X_{IN} (X_{CIN}) pin and leave the X_{OUT} (X_{COUT}) pin open. If the X_{CIN} clock is not used, connect the X_{CIN} pin to V_{SS}, and leave the X_{COUT} pin open.

Either high-speed operation start mode or low-speed operation start mode can be selected by using a mask option.

- **High-Speed Operation Start Mode**
  After reset has completed, the internal clock ϕ is half the frequency of X_{IN}. Immediately after power-on, both the X_{IN} and X_{CIN} clock start oscillating. To set the internal clock ϕ to low-speed operation mode, set bit 7 of the CPU mode register (address $003B_{16}$) to "1".
- **Low-Speed Operation Start Mode**
  After reset has completed, the internal clock ϕ is half the frequency of X_{CIN}. Immediately after power-on, only the X_{CIN} clock starts oscillating To set the internal clock ϕ to high-speed operation mode, first set bit 6 (CM_6) of the CPU mode register (address $003B_{16}$) to "0", the set bit 7 (CM_7) to "0". Note that the program must allow time for oscillation to stabilize.
- **Oscillation Control**

Stop Mode

If the STP instruction is executed, oscillation stops with the internal clock ϕ at an "H" level. Timer 1 is set to "FF_{16}" and timer 2 is set to "01_{16}".

Either X_{IN} or X_{CIN} divided by 16 is input to timer 1, and the output of timer 1 is connected to timer 2. The timer 1 and timer 2 interrupt enable bits must be set to disabled ("0"), so a program must set these bits before executing an STP instruction. Oscillation restarts at reset or when an external interrupt is received, but the internal clock ϕ is not supplied to the CPU until timer 2 overflows. This allows time for the clock circuit oscillation to stabilize

Wait Mode

If the WIT instruction is executed, the internal clock ϕ stops at an "H" level but the oscillator itself does not stop. The internal clock restarts if a reset occurs or when an interrupt is received. Since the oscillator does not stop, normal operation can be started immediately after the clock is restarted.

Low-Speed Mode

If the internal clock is generated from the sub clock (X_{CIN}), a low power consumption operation can be entered by stopping only the main clock X_{IN}. To stop the main clock, set bit 6 (CM_6) of the CPU mode register ($003B_{16}$) to "1". When the main clock X_{IN} is restarted, the program must allow enough time to for oscillation to stabilize.

Note that in low-power-consumption mode the X_{CIN}-X_{COUT} drive performance can be reduced, allowing even lower power consumption ($20\mu A$ with X_{CIN}= 32kHz). To reduce the X_{CIN}-X_{COUT} drive performance, clear bit 5 (CM_5) of the CPU mode register ($003B_{16}$) to "0". At reset or when an STP instruction is executed, this bit is set to "1" and strong drive is selected to help the oscillation to start.

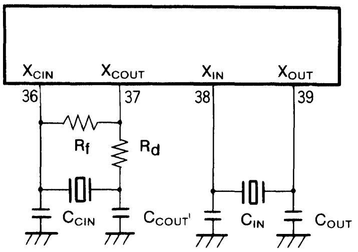


Fig. 38 Ceramic resonator circuit

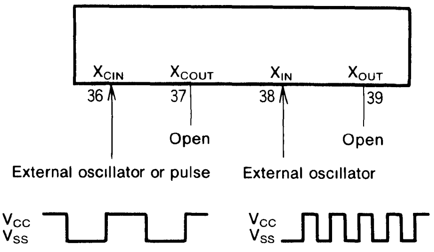
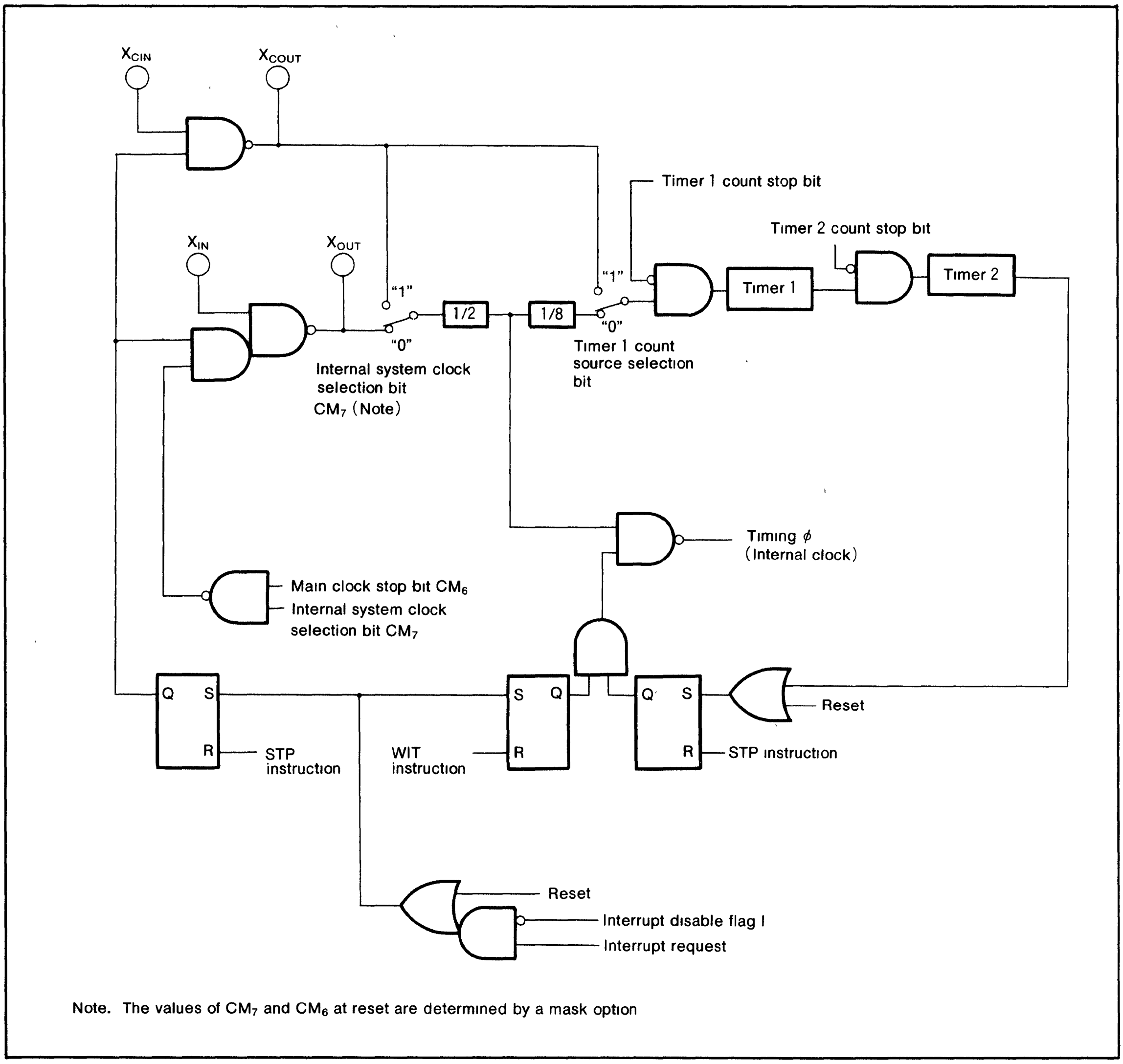
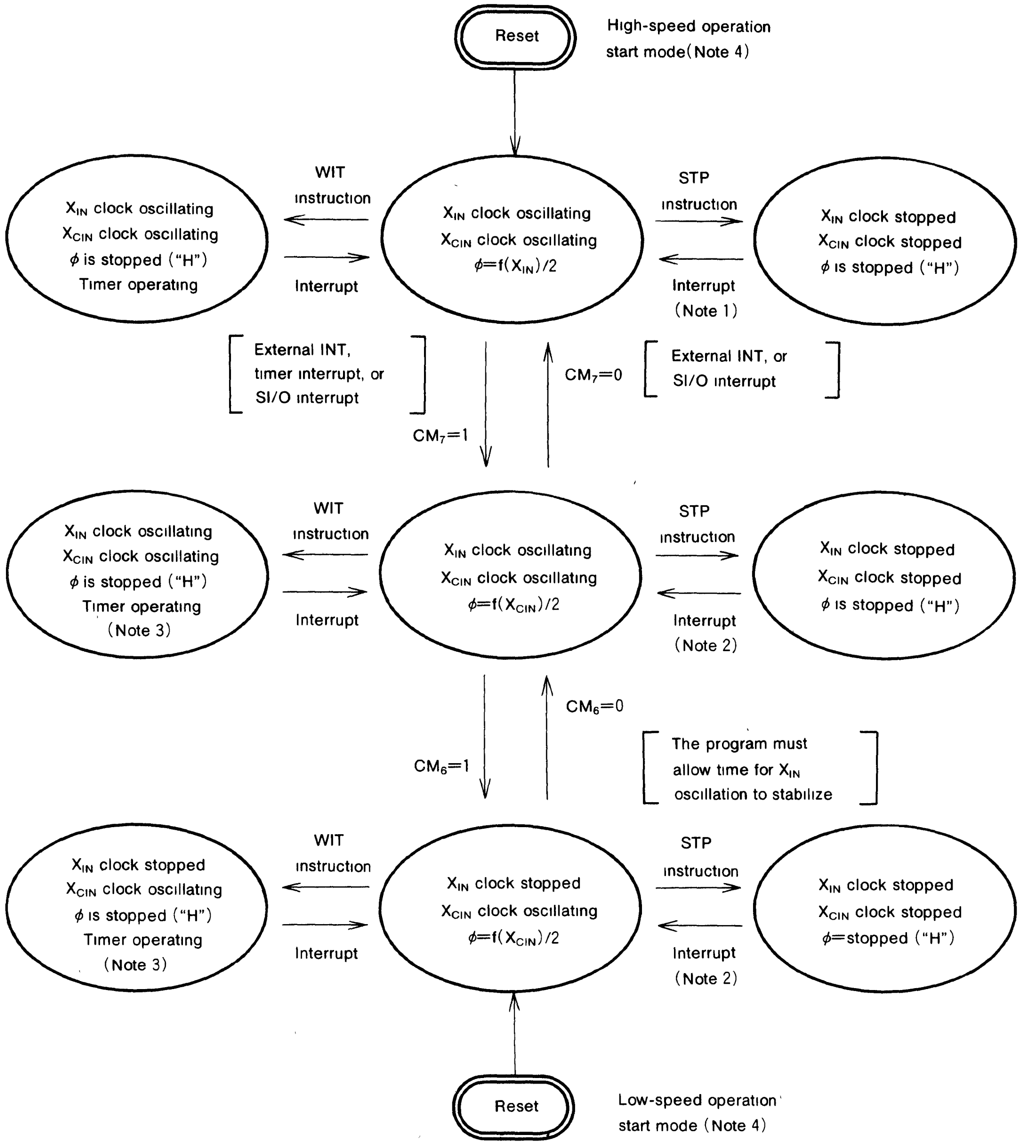


Fig. 39 External clock input circuit



Note. The values of CM_7 and CM_6 at reset are determined by a mask option

Fig. 40 System clock generation circuit block diagram



The example assumes that 6.3MHz is being applied to the X_{IN} pin and 32kHz to the X_{CIN} pin

Note 1. When the STP state is ended, a delay of approximately 1.3ms is automatically generated by timer 1 and timer 2
2. The delay after the STP state ends is approximately 0.25s
3. If the internal clock ϕ divided by 8 is used as the timer count source, the frequency of the count source is f(X_{CIN})/16
4. Specify this option when ordering a mask ROM version

Fig. 41 State transitions of system clock

NOTES ON PROGRAMMING

- **Processor Status Register**

  The contents of the processor status register (PS) after a reset are undefined, except for the interrupt disable flag (I) which is "1". Therefore, flags that affect program execution must be initialized after a reset. In particular, it is essential to initialize the T and D flags because of their effect on calculations.
- **Interrupts**

  The contents of the interrupt request bits do not change immediately after they have been written.

  After writing to an interrupt request register, execute at least one instruction before performing a BBC or BBS instruction.
- **Decimal Calculations**

  To calculate in decimal notation, set the decimal mode flag (D) to "1", then execute a ADC or SBC instruction. Only the ADC and SBC instruction yield proper decimal results. After executing an ADC or SBC instruction, execute at least one instruction before executing a SEC, CLC, or CLD instruction.

  In decimal mode, the values of the negative (N), overflow (V), and zero (Z) flags are invalid.

  The carry flag can be used to indicate whether a carry or borrow has occurred, but must be initialized before each calculation. Clear the carry flag before an ADC and set the flag before an SBC.
- **Timers**

  If a value n (between 0 and 255) is written to a timer latch, the frequency division ratio is 1/(n+1).
- **Multiplication and Division Instructions**

  The MUL and DIV instructions do not affect the T and D flags.

  The execution of these instructions does not change the contents of the processor status register.
- **Ports**

  The contents of the port direction registers cannot be read. Programs can not use the value of a direction register as an index, or bit-test a direction register (BBC or BBS), or perform a read-modify-write instruction such as ROR, CLB, or SEB. Use instructions such as LDM and STA to set the port direction registers.
- **Serial I/O**

  When using an external clock, input "H" to the external clock input pin and clear the serial I/O interrupt request bit before executing a serial I/O transfer.

  When using the internal clock, set the synchronization clock to internal clock, then clear the serial I/O interrupt request bit before executing a serial I/O transfer.
- **Instruction Execution Timing**

  The instruction execution time is obtained by multiplying the frequency of the internal clock ϕ by the number of cycles needed to execute an instruction.

  The number of cycles required to execute an instruction is shown in the list of machine instructions.

  The frequency of the internal clock ϕ is half of the X_{IN} or X_{CIN} frequency.

DATA REQUIRED FOR MASK ORDERS

The following are necessary when ordering a mask ROM production:

(1) Mask ROM Order Confirmation Form
(2) Mark Specification Form
(3) Data to be written to ROM, in EPROM form (three identical copies)

If required, specify the following option on the Mask Confirmation Form:

- Operation start mode switching option

ROM Writing Method

The built-in PROM of the blank one-time programmable version and built-in EPROM version can be read from and written to with an normal EPROM writer using a special write adapter.

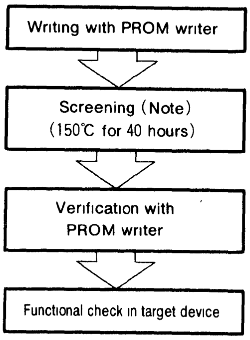
In case PROM is 32K bytes or under;

Package	Name of Write Adapter
100P6S	PCA4738F-100
100D0	PCA4738L-100

In case PROM is 36K bytes or over;

Package	Name of Write Adapter
100P6S	Under development
100D0	Under development

The PROM of the blank one-time programmable version is not tested or screened after assembly. To ensure proper operation after writing, the procedure shown in Figure 42 is recommended to verify programming.



Note. The screening temperature is far higher than the storage temperature Do not leave the microcomputer at 150℃ for longer than 100 hours

Fig. 42 Writing and testing of one-time programmable version

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	All voltages measured based on the V_{SS} pin Output transistors are isolated	−0.3 to 7.0	V
V_{EE}	Pull-down power supply voltage		V_{CC}−40 to V_{CC}+0.3	V
V_I	Input voltage $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P4_1$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_0$-$P7_2$, $P9_0$-$P9_3$, PA_0-PA_7 PB_0, PB_1		−0.3 to V_{CC}+0.3	V
V_I	Input voltage $P4_0$		−0.3 to V_{CC}+0.3	V
V_I	Input voltage $P8_0$-$P8_7$		V_{CC}−40 to V_{CC}+0.3	V
V_I	Input voltage $\overline{RESET}$, X_{IN}		−0.3 to V_{CC}+0.3	V
V_I	Input voltage X_{CIN}		−0.3 to V_{CC}+0.3	V
V_O	Output voltage $P0_0$-$P0_7$, $P3_0$-$P3_7$, $P8_0$-$P8_7$, $P9_0$-$P9_7$		V_{CC}−40 to V_{CC}+0.3	V
V_O	Output voltage $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P4_1$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_0$-$P7_7$, PA_0-PA_7, X_{OUT}, X_{COUT}		−0.3 to V_{CC}+0.3	V
P_d	Power dissipation	T_a = 25℃	600	mW
T_{opr}	Operating temperature		−10 to 85	℃
T_{stg}	Storage temperature		−40 to 125	℃

RECOMMENDED OPERATING CONDITIONS (V_{CC} = 4.0 to 5.5V, T_a = −10 to 85℃, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage	High-speed operation mode	4.0	5.0	5.5	V
		Low-speed operation mode	2.8	5.0	5.5	
V_{SS}	Supply voltage			0		V
V_{EE}	Pull-down power supply voltage		V_{CC}−38		V_{CC}	V
V_{REF}	Reference input voltage		2		V_{CC}	V
AV_{SS}	Analog power voltage			0		V
V_{IA}	Analog input voltage		0		V_{CC}	V
V_{IH}	"H" input voltage $P1_0$-$P1_7$, $P4_1$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_0$-$P7_7$, PA_0-PA_7, PB_0, PB_1		0.75V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage $P2_0$-$P2_7$		0.4V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage $P4_0$		0.75V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage $P8_0$-$P8_7$, $P9_0$-$P9_3$		0.8V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage $\overline{RESET}$		0.8V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage X_{IN}, X_{CIN}		0.8V_{CC}		V_{CC}	V
V_{IL}	"L" input voltage $P1_0$-$P1_7$, $P4_1$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_0$-$P7_7$, PA_0-PA_7, PB_0, PB_1		0		0.25V_{CC}	V
V_{IL}	"L" input voltage $P2_0$-$P2_7$		0		0.16V_{CC}	V
V_{IL}	"L" input voltage $P4_0$		0		0.25V_{CC}	V
V_{IL}	"L" input voltage $P8_0$-$P8_7$, $P9_0$-$P9_3$		0		0.2V_{CC}	V
V_{IL}	"L" input voltage $\overline{RESET}$		0		0.2V_{CC}	V
V_{IL}	"L" input voltage X_{IN}, X_{CIN}		0		0.2V_{CC}	V

RECOMMENDED OPERATING CONDITIONS (V_{CC}=4.0 to 5.5V, T_a=−10 to 85℃, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
$\Sigma I_{OH(peak)}$	"H" total peak output current $P0_0$-$P0_7$, $P1_0$-$P1_7$, (Note 1) $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P8_0$-$P8_7$, $P9_0$-$P9_7$			−240	mA
$\Sigma I_{OH(peak)}$	"H" total peak output current $P4_1$-$P4_7$, $P6_0$-$P6_5$, $P7_0$-$P7_7$, PA_0-PA_7			−60	mA
$\Sigma I_{OL(peak)}$	"L" total peak output current $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P4_1$-$P4_7$, $P5_0$-$P5_7$, $P6_1$-$P6_7$, $P7_0$-$P7_7$, PA_0-PA_7			100	mA
$\Sigma I_{OL(peak)}$	"L" total peak output current $P6_0$			3.0	mA
$\Sigma I_{OH(avg)}$	"H" total average output current $P0_0$-$P0_7$, $P1_0$-$P1_7$, (Note 1) $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P8_0$-$P8_7$, $P9_0$-$P9_7$			−120	mA
$\Sigma I_{OH(avg)}$	"H" total average output current $P4_1$-$P4_7$, $P6_0$-$P6_7$, $P7_0$-$P7_7$, PA_0-PA_7			−30	mA
$\Sigma I_{OL(avg)}$	"L" total average output current $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P4_1$-$P4_7$, $P5_0$-$P5_7$, $P6_1$-$P6_7$, $P7_0$-$P7_7$, PA_0-PA_7			50	mA
$\Sigma I_{OL(avg)}$	"L" total average output current $P6_0$			1.5	mA
$I_{OH(peak)}$	"H" peak output current $P0_0$-$P0_7$, $P3_0$-$P3_7$, $P8_0$-$P8_7$, $P9_0$-$P9_7$ (Note 2)			−40	mA
$I_{OH(peak)}$	"H" peak output current $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P4_1$-$P4_7$, $P6_0$-$P6_7$, $P7_0$-$P7_7$, PA_0-PA_7			−10	mA
$I_{OL(peak)}$	"L" peak output current $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P4_1$-$P4_7$, $P6_1$-$P6_7$, $P7_0$-$P7_7$, PA_0-PA_7			10	mA
$I_{OL(peak)}$	"L" peak output current $P5_0$-$P5_7$			10	mA
$I_{OL(peak)}$	"L" peak output current $P6_0$			3.0	mA
$I_{OH(avg)}$	"H" average output current $P0_0$-$P0_7$, $P3_0$-$P3_7$, $P8_0$-$P8_7$, $P9_0$-$P9_7$			−18	mA
$I_{OH(avg)}$	"H" average output current $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P4_1$-$P4_7$, $P6_1$-$P6_7$, $P7_0$-$P7_7$, PA_0-PA_7			−5.0	mA
$I_{OL(avg)}$	"L" average output current $P1_0$-$P1_7$, $P2_0$-$P2_7$, (Note 3) $P4_1$-$P4_7$, $P6_0$-$P6_7$, $P7_0$-$P7_7$, PA_0-PA_7			5.0	mA
$I_{OL(avg)}$	"L" average output current $P5_0$-$P5_7$			5.0	mA
$I_{OL(avg)}$	"L" average output current $P6_0$			1.5	mA
$f(CNTR_0)$ $f(CNTR_1)$	Clock input frequency for timers 2 and 4 (duty cycle 50%)			250	kHz
$f(X_{IN})$	Main clock input oscillation frequency (Note 4)			6.3	MHz
$f(X_{CIN})$	Sub clock input oscillation frequency (Note 4, Note 5)		32.768	50	kHz

Note 1. The total output current is the sum of all the currents flowing through all the applicable ports The total average current is an average value measured over 100ms The total peak current is the peak value of all the currents
2. The peak output current is the peak current flowing in each port
3. The average output current in an average value measured over 100ms
4. When the oscillation frequency has a duty cycle of 50%
5. When using the microcomputer in low-speed operation mode, make sure that the sub clock's input frequency $f(X_{CIN})$ is less than $f(X_{IN})/3$

ELECTRICAL CHARACTERISTICS (V_{CC} = 4.0 to 5.5V, T_a = −10 to 85℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ	Max	
V_{OH}	"H" output voltage $P0_0$-$P0_7$, $P3_0$-$P3_7$, $P8_0$-$P8_7$, $P9_0$-$P9_7$	$I_{OH}=-18$mA	$V_{CC}-2.0$			V
V_{OH}	"H" output voltage $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P4_1$-$P4_7$, $P6_0$-$P6_7$, $P7_0$-$P7_7$, PA_0-PA_7	$I_{OH}=-10$mA	$V_{CC}-2.0$			V
V_{OL}	"L" output voltage $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P4_1$-$P4_7$, $P5_0$-$P5_7$, $P6_1$-$P6_7$, $P7_0$-$P7_7$, PA_0-PA_7	$I_{OL}=10$mA			2.0	V
V_{OL}	"L" output voltage $P6_0$	$I_{OL}=1.5$mA			0.5	V
$V_{T+}-V_{T-}$	Hysteresis $\overline{INT_0}$—$\overline{INT_4}$, S_{IN1}, S_{IN2}, S_{CLK1}, S_{CLK2}, $CNTR_0$, $CNTR_1$	When using a non-port function		0.4		V
$V_{T+}-V_{T-}$	Hysteresis $\overline{RESET}$, X_{IN}	$\overline{RESET}$: $V_{CC}=2.8$V to 5.5V		0.5		V
$V_{T+}-V_{T-}$	Hysteresis X_{CIN}			0.5		V
I_{IH}	"H" input current $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P4_1$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_0$-$P7_7$, PA_0-PA_7, PB_0, PB_1	$V_I=V_{CC}$			5.0	µA
I_{IH}	"H" input current $P4_0$	$V_I=V_{CC}$			5.0	µA
I_{IH}	"H" input current $P8_0$-$P8_7$, $P9_0$-$P9_3$ (Note 1)	$V_I=V_{CC}$			5.0	µA
I_{IH}	"H" input current $\overline{RESET}$, X_{CIN}	$V_I=V_{CC}$			5.0	µA
I_{IH}	"H" input current X_{IN}	$V_I=V_{CC}$		4.0		µA
I_{IL}	"L" input current $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P4_1$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_0$-$P7_7$, PA_0-PA_7, PB_0, PB_1	$V_I=V_{SS}$			−5.0	µA
I_{IL}	"L" input current $P4_0$	$V_I=V_{SS}$			−5.0	µA
I_{IL}	"L" input current $P8_0$-$P8_7$, $P9_0$-$P9_3$ (Note 1)	$V_I=V_{SS}$			−5.0	µA
I_{IL}	"L" input current $\overline{RESET}$, X_{CIN}	$V_I=V_{SS}$			−5.0	µA
I_{IL}	"L" input current X_{IN}	$V_I=V_{SS}$		−4.0		µA
I_{LOAD}	Output load current $P0_0$-$P0_7$, $P3_0$-$P3_7$, $P9_0$-$P9_7$	$V_{EE}=V_{CC}-36$V, $V_{OL}=V_{CC}$, With output transistors off	150	500	900	µA
I_{LEAK}	Output leakage current $P0_0$-$P0_7$, $P3_0$-$P3_7$, $P8_0$-$P8_7$, $P9_0$-$P9_7$	$V_{EE}=V_{CC}-38$V, $V_{OL}=V_{CC}-38$V, With output transistors off (Except for reset)			−10	µA
V_{RAM}	RAM hold voltage	When clock is stopped	2.0		5.5	V
I_{CC}	Power supply current	In high-speed operation mode $f(X_{IN})=6.3$MHz $f(X_{CIN})=32$kHz Output transistors off A-D converter operating		7.5	15	mA
		In high-speed operation mode $f(X_{IN})=6.3$MHz (in WIT state) $f(X_{CIN})=32$kHz Output transistors off A-D converter stopped		1.0		mA
		In low-speed operation mode $f(X_{IN})$= stopped, $f(X_{CIN})=32$kHz Low-power dissipation mode set ($CM_5=0$) Output transistors off		60	200	µA
		In low-speed operation mode $f(X_{IN})$= stopped $f(X_{CIN})=32$kHz (in WIT state) Low-power dissipation mode set ($CM_5=0$) Output transistors off		20	40	µA
		All oscillation stopped (in STP state) Output transistors off $T_a=25$℃		0.1	1.0	µA
		$T_a=85$℃			10	

Note 1. Except when reading ports P8 or ports $P9_0$—$P9_3$

A-D CONVERTER CHARACTERISTICS

(V_{CC}=4. 0 to 5. 5V, V_{SS}=0V, T_a=−10 to 85℃, high-speed operation mode, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
—	Resolution				8	Bits
—	Absolute accuracy	$V_{CC}=V_{REF}=5.12V$		±1	±2. 5	LSB
T_{CONV}	Conversion time		49		50	t_C (ϕ)
V_{REF}	Reference input voltage		2		V_{CC}	V
I_{VREF}	Reference input current	$V_{REF}=5V$	50	150	200	μA
I_{IA}	Analog port input current			0. 5	5. 0	μA
R_{LADDER}	Ladder resistor			35		kΩ

TIMING REQUIREMENTS

(V_{CC}=4. 0 to 5. 5V, V_{SS} = 0V, T_a = −10 to 85℃, unless otherwise noted)

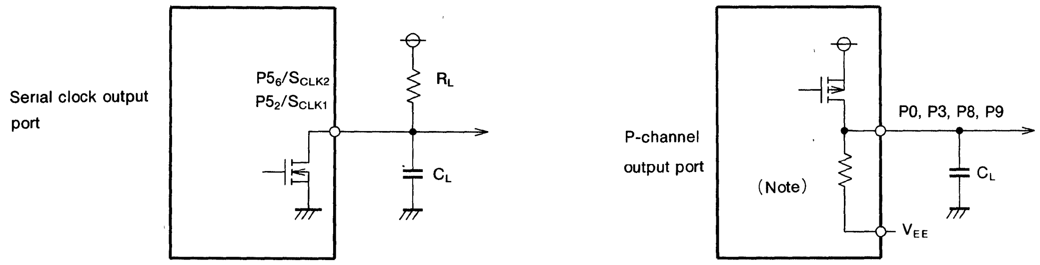
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{W(\overline{RESET})}$	Reset input "L" pulse width		2. 0			μs
$t_{C(X_{IN})}$	Main clock input cycle time (X_{IN} input)		158			ns
$t_{WH(X_{IN})}$	Main clock input "H" pulse width		40			ns
$t_{WL(X_{IN})}$	Main clock input "L" pulse width		40			ns
$t_{C(X_{CIN})}$	Sub clock input cycle time (X_{CIN} input)		2. 0			ms
$t_{WH(X_{CIN})}$	Sub clock input "H" pulse width		0. 5			ms
$t_{WL(X_{CIN})}$	Sub clock input "L" pulse width		0. 5			ms
$t_{C(CNTR)}$	$CNTR_0$, $CNTR_1$ input cycle time		4. 0			μs
$t_{WH(CNTR)}$	$CNTR_0$, $CNTR_1$, input "H" pulse width		1. 6			μs
$t_{WL(CNTR)}$	$CNTR_0$, $CNTR_1$, input "L" pulse width		1. 6			μs
$t_{WH(INT)}$	INT_0-INT_4 input "H" pulse width		80			ns
$t_{WL(INT)}$	INT_0-INT_4 input "L" pulse width		80			ns
$t_{C(S_{CLK})}$	Serial clock input cycle time		1. 0			μs
$t_{WH(S_{CLK})}$	Serial clock input clock "H" pulse width		400			ns
$t_{WL(S_{CLK})}$	Serial clock input clock "L" pulse width		400			ns
$t_{SU(S_{CLK}-S_{IN})}$	Serial input setup time		200			ns
$t_{h(S_{CLK}-S_{IN})}$	Serial input hold time		200			ns

SWITCHING CHARACTERISTICS

(V_{CC} = 4. 0 to 5. 5V, V_{SS} = 0V, T_a = −10 to 85℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{WH(S_{CLK})}$	Serial clock output "H" pulse width	C_L=100pF, R_L=1kΩ	$t_C/2-160$			ns
$t_{WL(S_{CLK})}$	Serial clock output "L" pulse width	C_L=100pF, R_L=1kΩ	$t_C/2-160$			ns
$t_{d(S_{CLK}-S_{OUT})}$	Serial output delay time				0. 2t_C	ns
$t_{v(S_{CLK}-S_{OUT})}$	Serial output hold time		0			ns
$t_{f(S_{CLK})}$	Serial clock output fall time	C_L=100pF, R_L=1kΩ			40	ns
$t_{r(Pch-strg)}$	P-channel high-breakdown voltage output rise time (Note 1)	C_L=100pF, $V_{EE}=V_{CC}-36V$		55		ns
$t_{r(Pch-weak)}$	P-channel high-breakdown voltage output rise time (Note 2)	C_L=100pF, $V_{EE}=V_{CC}-36V$		1. 8		μs

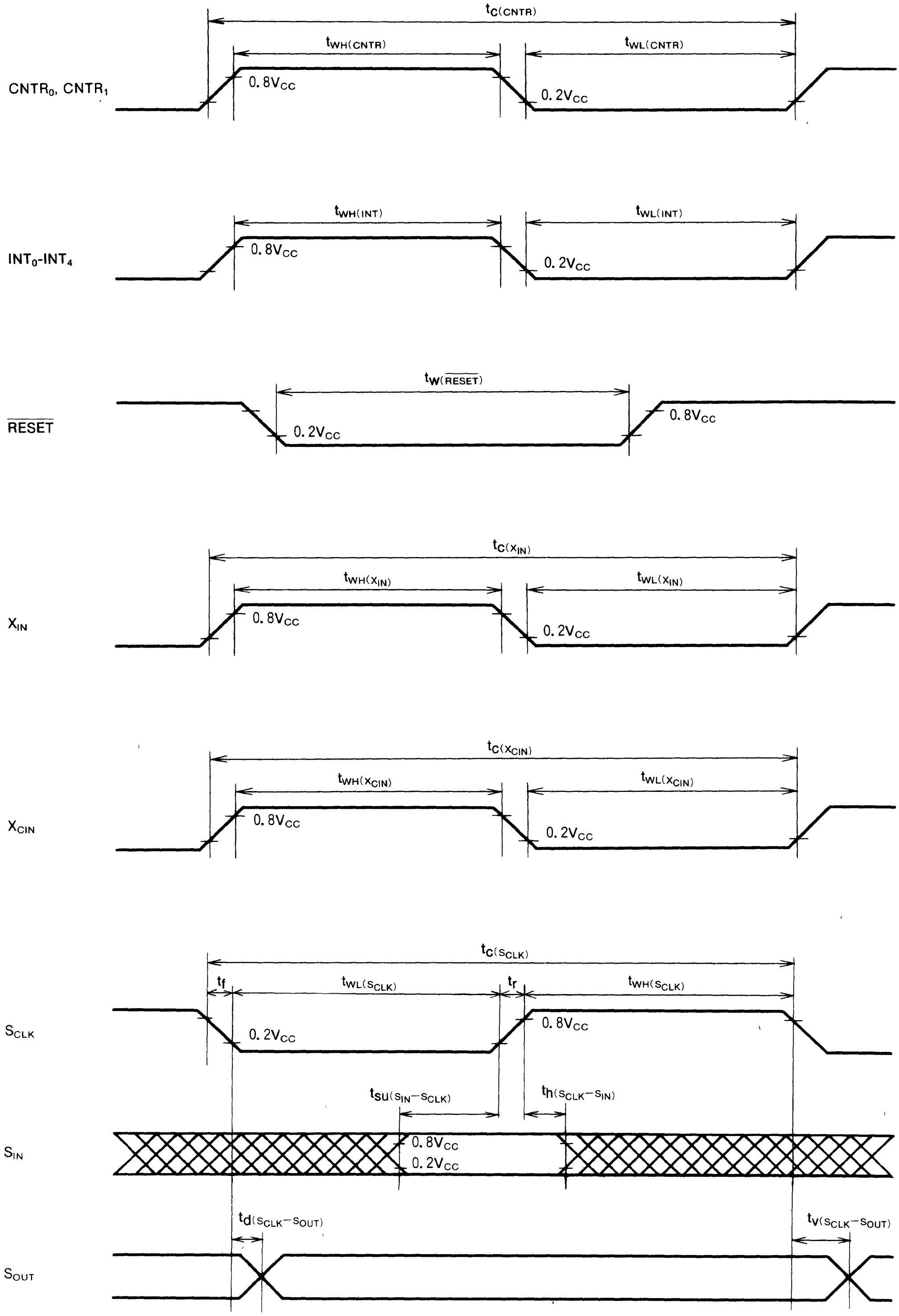
Note 1. When bit 0 of the high-breakdown voltage port control register (address 0038_{16}) is at "0"
2. When bit 0 of the high-breakdown voltage port control register (address 0038_{16}) is at "1"



Note : Port P8 has no internal pull-down resistors and external resistors should be used if necessary

Fig. 43 Output switching characteristics measurement circuit

Timing Chart



SERIES 7450

MITSUBISHI MICROCOMPUTERS

M37450M2-XXXSP/FP,M37450M4-XXXSP/FP
M37450M8-XXXSP/FP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

DESCRIPTION

The M37450M2-XXXSP/FP is a single-chip microcomputer designed with CMOS sillicon gate technology. It is housed in a 64-pin shrink plastic molded DIP or an 80-pin plastic molded QFP.

In addition to its simple instruction sets, the ROM, RAM, and I/O addresses are placed on the same memory map to enable easy programming.

It is suited for office automation equipment and control devices. The low power consumption made by the use of a CMOS process makes it especially suitable for battery powered devices requiring low power consumption. It also has a unique feature that enables it to be used as a slave microcomputer.

The differences among M37450M2-XXXSP/FP, M37450M4-XXXSP/FP and M37450M8-XXXSP/FP are as shown below. The descriptions that follow describe the M37450M2-XXXSP/FP (abbreviated as M37450) unless otherwise noted.

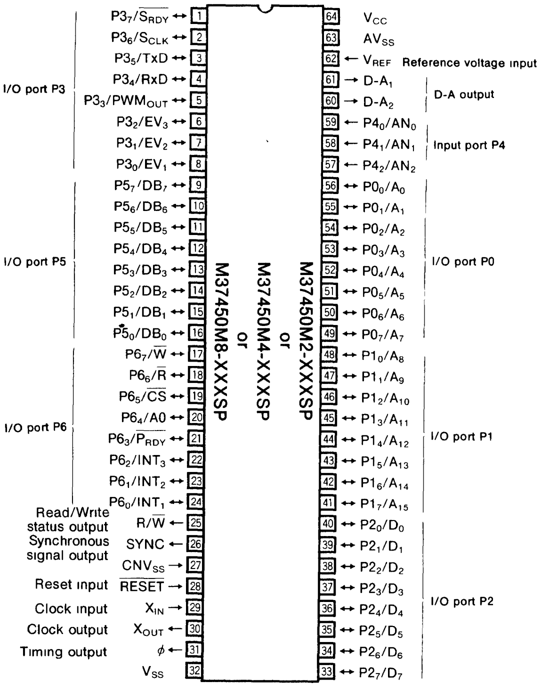
Type name	ROM size	RAM size
M37450M2-XXXSP/FP	4096 bytes	128 bytes
M37450M4-XXXSP/FP	8192 bytes	256 bytes
M37450M8-XXXSP/FP	16384 bytes	384 bytes

The number of analog input pins for the 80-pin model (FP version) is different from the 64-pin model (SP version). In addition, the 80-pin model has special pins for $\overline{RD}$, $\overline{WR}$, $RESET_{OUT}$, DAV_{REF}, ADV_{REF}, AV_{CC} and the 64-pin model has a special V_{REF} pin.

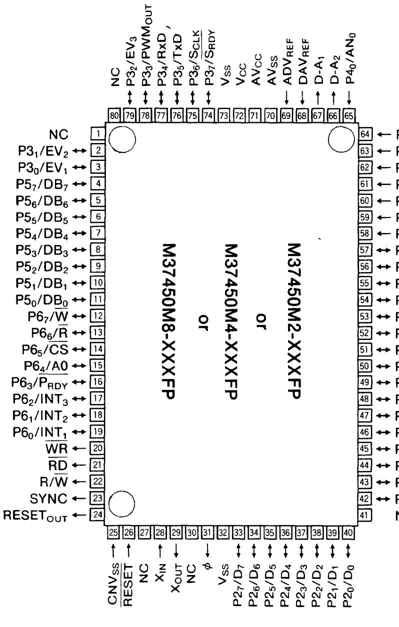
FEATURES

- Number of basic instructions ···················· 71
  69 MELPS 740 basic instructions+2 multiply/divide instructions
- Instruction execution time
  (minimum instructions at 10MHz frequency) ········ 0.8μs
- Single power supply ···················· 5V±10%
- Power dissipation normal operation mode
  (at 10MHz frequency) ···················· 30mW
- Subroutine nesting ············ 64 levels max.(M37450M2)
  96 levels max.(M37450M4, M37450M8)
- Interrupt ···················· 15 events
- Master CPU bus interface ···················· 1 byte
- 16-bit timer ···················· 3
- 8-bit timer (Serial I/O use) ···················· 1
- Serial I/O (UART or clock synchronous) ···················· 1
- A-D converter (8-bit resolution) ········ 3 channels (DIP)
  8 channels (QFP)
- D-A converter (8-bit resolution) ················ 2 channels
- PWM output (8 bit or 16 bit) ···················· 1
- Programmable I/O ports
  (Ports P0, P1, P2, P3, P5, P6) ···················· 48
- Input port (Port P4) ················ 3(DIP), 8(QFP)
- Output ports (Ports D-A1, D-A2) ···················· 2

PIN CONFIGURATION (TOP VIEW)



Outline 64P4B



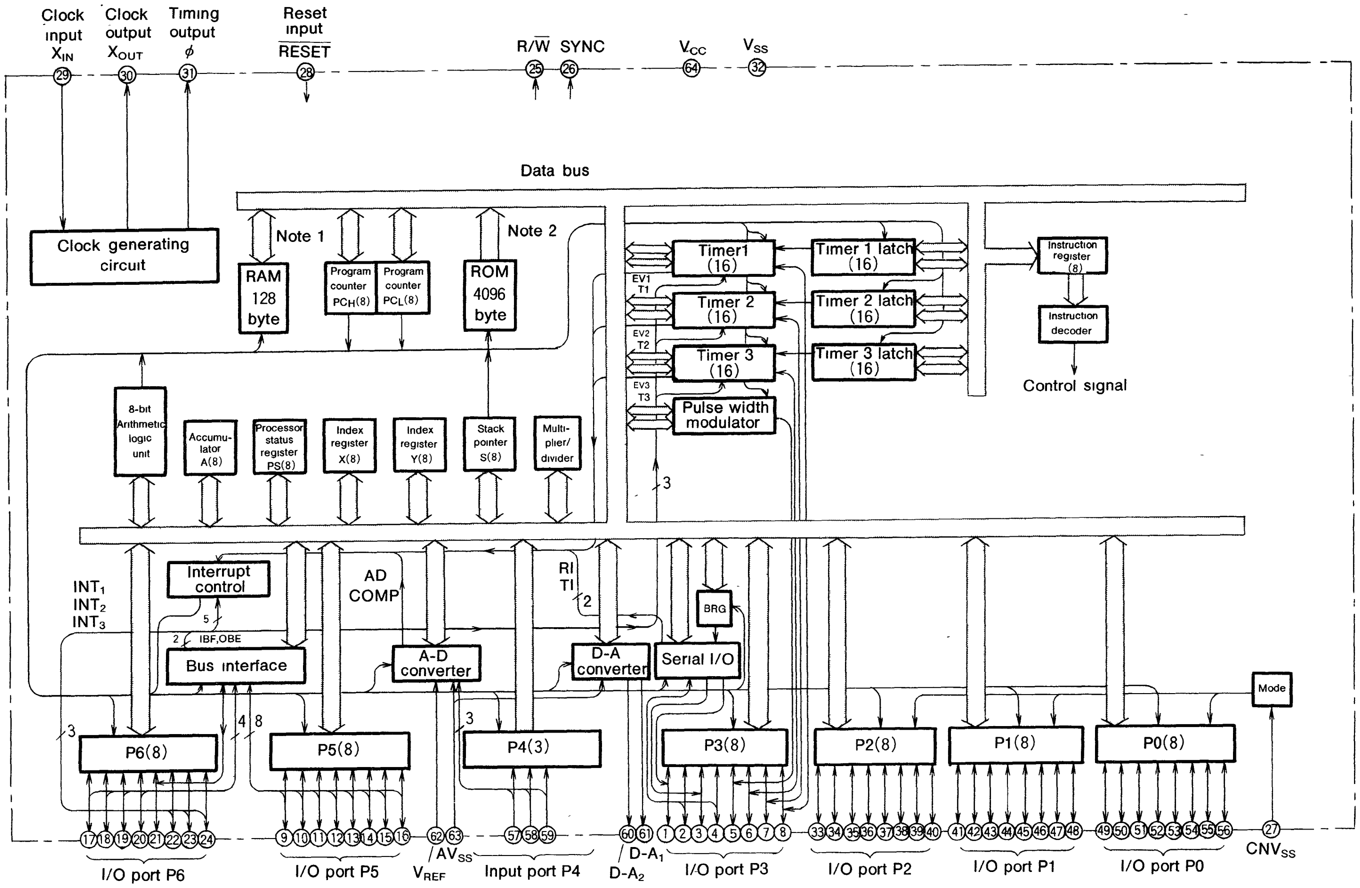
Outline 80P6

NC : No connection

APPLICATION

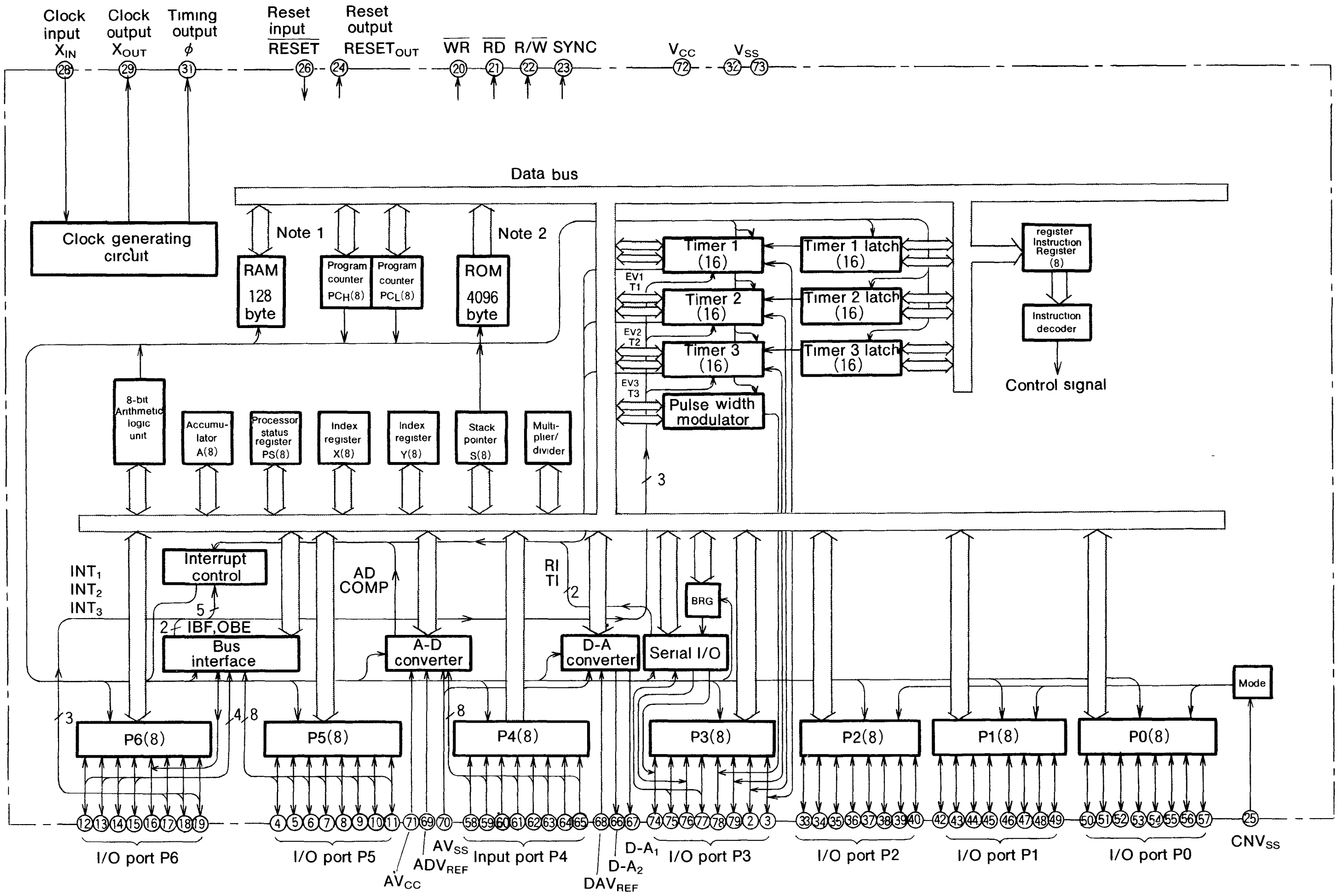
Slave controller for PPCs, facsimiles, and page printers. HDD, optical disk, inverter, and industrial motor controllers. Industrial robots and machines.

M37450M2-XXXSP BLOCK DIAGRAM



Note 1 : 256 bytes for M37450M4-XXXSP and 384 bytes for M37450M8-XXXSP
2 : 8192 bytes for M37450M4-XXXSP and 16384 bytes for M37450M8-XXXSP

M37450M2-XXXFP BLOCK DIAGRAM



Note 1 : 256 bytes for M37450M4-XXXFP and 384 bytes for M37450M8-XXXFP
2 : 8192 bytes for M37450M4-XXXFP and 16384 bytes for M37450M8-XXXFP

FUNCTIONS OF M37450M2-XXXSP/FP, M37450M4-XXXSP/FP, M37450M8-XXXSP/FP

Parameter			Functions
Number of basic instructions			71(69 MELPS 740 basic instructions+2)
Instruction execution time			0 8μs (minimum instructions, at 10MHz frequency)
Clock frequency			10MHz (max)
Memory size	M37450M2-XXXSP/FP	ROM	4096 bytes
		RAM	128 bytes
	M37450M4-XXXSP/FP	ROM	8192 bytes
		RAM	256 bytes
	M37450M8-XXXSP/FP	ROM	16384 bytes
		RAM	384 bytes
Input/Output ports	P0-P3, P5, P6	I/O	8-bit×6
	P4	Input	3-bit×1 (8-bit×1 for 80-pin model)
	D-A	Output	2-bit×1
Serial I/O			UART or clock synchronous
Timers			16-bit timer×3, 8-bit timer (serial I/O baud rate generator)×1
A-D converter			8-bit×3 channels (8 channels for 80-pin model)
D-A converter			8-bit×2 channels
Pulse width modulator			8-bit or 16-bit×1
Data bus buffer			1-byte input and output each
Subroutine nesting			64-levels (max for M37450M2)
			96-levels (max for M37450M4, M37450M8)
Interrupt			6 external interrupts, 8 internal interrupts 1 software interrupt
Clock generating circuit			Built-in (ceramic or quarts crystal oscillator)
Supply voltage			5V±10%
Power dissipation			30mW (at 10MHz frequency)
Input/Output characters	Input/Output voltage		5V
	Output current		±5mA (max.)
Memory expansion			Possible
Operating temperature range			−10 to 70℃
Device structure			CMOS silicon gate
Package	M37450M2-XXXSP		64-pin shrink plastic molded DIP
	M37450M4-XXXSP		
	M37450M8-XXXSP		
	M37450M2-XXXFP		80-pin plastic molded QFP
	M37450M4-XXXFP		
	M37450M8-XXXFP		

PIN DESCRIPTION

Pin	Name	Input/ Output	Functions
V_{CC}, V_{SS}	Supply voltage		Power supply inputs 5V±10% to V_{CC}, and 0V to V_{SS}
CNV_{SS}	CNV_{SS}		Controls the processor mode of the chip. Normally connected to V_{SS} or V_{CC}
$\overline{RESET}$	Reset input	Input	To enter the reset state, the reset input pin must be kept at a "L" for more than 8 clock cycles (under normal V_{CC} conditions). If more time is needed for the crystal oscillator to stabilize, this "L" condition should be maintained for the required time
X_{IN}	Clock input	Input	This chip has an internal clock generating circuit To control generating frequency, an external ceramic or a quartz crystal oscillator is connected between the X_{IN} and X_{OUT} pins If an external clock is used, the clock source should be connected to the X_{IN} pin and the X_{OUT} pin should be left open
X_{OUT}	Clock output	Output	
ϕ	Timing output	Output	Outputs signal consisting of oscillating frequency divided by four
SYNC	Synchronous signal output	Output	This signal is output "H" during operation code fetch and is used to control single stepping of programs
$R/\overline{W}$	Read/Write status output	Output	This signal determines the direction of the data bus It is "H" during read and "L" during write
$P0_0$-$P0_7$	I/O port P0	I/O	Port P0 is an 8-bit I/O port with directional registers allowing each I/O bit to be individually programmed as input or output The output structure is CMOS output The low-order bits of the address are output except in single-chip mode
$P1_0$-$P1_7$	I/O port P1	I/O	Port P1 is an 8-bit I/O port and has basically the same functions as port P0 The high-order bits of the address are output except in single-chip mode
$P2_0$-$P2_7$	I/O port P2	I/O	Port P2 is an 8-bit I/O port and has basically the same functions as port P0 Used as data bus except in single-chip mode
$P3_0$-$P3_7$	I/O port P3	I/O	Port P3 is an 8-bit I/O port and has basically the same functions as port P0 Serial I/O, PWM output, or event I/O function can be selected with a program
$P4_0$-$P4_2$ ($P4_0$-$P4_7$)	Input port P4	Input	Analog input pin for the A-D converter The 64-pin model has three pins and the 80-pin model has eight pins They may also be used as digital input pins
$P5_0$-$P5_7$	I/O port P5	I/O	Port P5 is an 8-bit I/O port and has basically the same functions as port P0 This port functions as an 8-bit data bus for the master CPU when slave mode is selected with a program
$P6_0$-$P6_7$	I/O port P6	I/O	Port P6 is an 8-bit I/O port and has basically the same function as port P0 Pins $P6_3$-$P6_7$ change to a control bus for the master CPU when slave mode is selected with a program Pins $P6_0$-$P6_2$ may be programmed as external interrupt input pins
D-A_1, D-A_2	D-A output	Output	Analog signal from D-A converter is output
V_{REF}	Reference voltage input	Input	Reference voltage input pin for A-D and D-A converter This pin is for 64-pin model only
ADV_{REF}	A-D reference voltage input	Input	Reference voltage input pin for A-D converter This pin is for 80-pin model only
DAV_{REF}	D-A reference voltage input	Input	Reference voltage input pin for D-A converter This pin is for 80-pin model only
AV_{SS}	Analog power supply		Ground level input pin for A-D and D-A converter Same voltage as V_{SS} is applied
AV_{CC}	Analog power supply		Power supply input pin for A-D converter This pin is for 80-pin model only Same voltage as V_{CC} is applied In the case of the 64-pin model, AV_{CC} is connected to V_{CC} internally
$\overline{RD}$	Read signal output	Output	Control signal output as active "L" when valid data is read from data bus This pin is for 80-pin model only
$\overline{WR}$	Write signal output	Output	Control signal output as active "L" when writing data from data bus to external component This pin is for 80-pin model only
$RESET_{OUT}$	Reset output	Output	Control signal output as active "H" during reset It is used as a reset output signal for peripheral components This pin is for 80-pin model only

FUNCTIONAL DESCRIPTION

Central Processing Unit (CPU)

The M37450 microcomputers use the standard MELPS 740 instruction set. For details of instructions, refer to the MELPS 740 CPU core basic functions, or the MELPS 740 Software Manual.

Machine-resident instructions are as follows:

The FST and SLW instructions are not provided.

The MUL and DIV instructions can be used.

The WIT instruction can be used.

The STP instruction can be used.

MISRG2 Register

The MISRG2 register is allocated to address $00DF_{16}$. Bits 0 and 1 of this register are processor mode bits. This register also has a stack page selection bit.

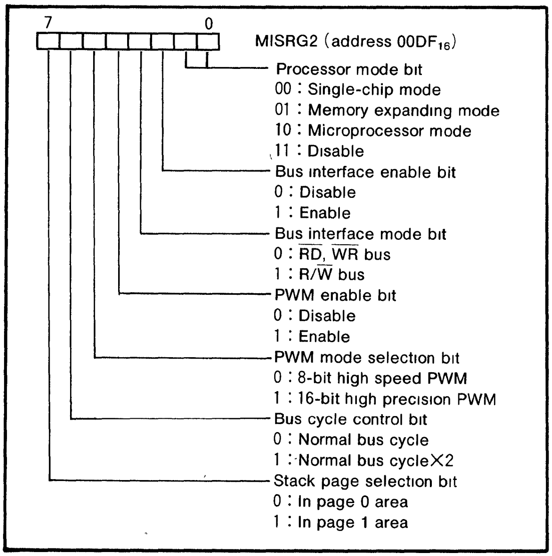


Fig. 1 Structure of MISRG2 register

MEMORY

- **Special Function Register (SFR) Area**

The special function register (SFR) area contains the registers relating to functions such as I/O ports and timers.

- **RAM**

RAM is used for data storage as well as a stack area.

- **ROM**

ROM is used for storing user programs as well as the interrupt vector area.

- **Interrupt Vector Area**

The interrupt vector area is for storing jump destination addresses used at reset or when an interrupt is generated.

- **Zero Page**

Zero page addressing mode is useful because it enables access to this area with fewer instruction cycles.

- **Special Page**

Special page addressing mode is useful because it enables access to this area with fewer instruction cycles.

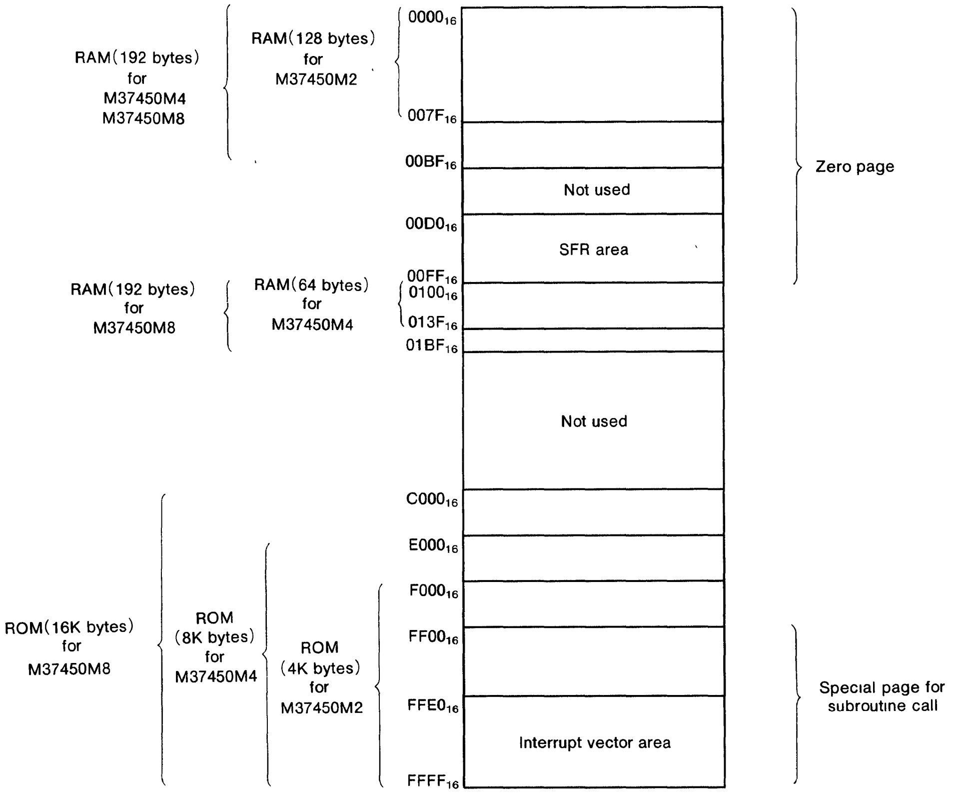


Fig. 2 Memory map

$00D0_{16}$	P0 register
$00D1_{16}$	P0 directional register
$00D2_{16}$	P1 register
$00D3_{16}$	P1 directional register
$00D4_{16}$	P2 register
$00D5_{16}$	P2 directional register
$00D6_{16}$	P3 register
$00D7_{16}$	P3 directional register
$00D8_{16}$	P4 register
$00D9_{16}$	Reserved
$00DA_{16}$	P5 register
$00DB_{16}$	P5 directional register
$00DC_{16}$	P6 register
$00DD_{16}$	P6 directional register
$00DE_{16}$	MISRG1
$00DF_{16}$	MISRG2
$00E0_{16}$	D-A1 register
$00E1_{16}$	D-A2 register
$00E2_{16}$	A-D register
$00E3_{16}$	A-D control register
$00E4_{16}$	Data bus buffer register
$00E5_{16}$	Data bus buffer status register
$00E6_{16}$	Receive/Transmit buffer register
$00E7_{16}$	Serial I/O status register
$00E8_{16}$	Serial I/O control register
$00E9_{16}$	UART control register
$00EA_{16}$	Baud rate generator
$00EB_{16}$	PWM register (low-order)
$00EC_{16}$	PWM register (high-order)
$00ED_{16}$	Timer 1 control register
$00EE_{16}$	Timer 2 control register
$00EF_{16}$	Timer 3 control register
$00F0_{16}$	Timer 1 register (low-order)
$00F1_{16}$	Timer 1 register (high-order)
$00F2_{16}$	Timer 1 latch (low-order)
$00F3_{16}$	Timer 1 latch (high-order)
$00F4_{16}$	Timer 2 register (low-order)
$00F5_{16}$	Timer 2 register (high-order)
$00F6_{16}$	Timer 2 latch (low-order)
$00F7_{16}$	Timer 2 latch (high-order)
$00F8_{16}$	Timer 3 register (low-order)
$00F9_{16}$	Timer 3 register (high-order)
$00FA_{16}$	Timer 3 latch (low-order)
$00FB_{16}$	Timer 3 latch (high-order)
$00FC_{16}$	Interrupt request register 1
$00FD_{16}$	Interrupt request register 2
$00FE_{16}$	Interrupt control register 1
$00FF_{16}$	Interrupt control register 2

Fig. 3 SFR (Special Function Register) memory map

INTERRUPTS

Interrupts can be caused by 15 different events consisting of six external, eight internal, and one software events.

Interrupts are vectored interrupts with priorities shown in Table 1. Reset is also included in the table because its operation is similar to an interrupt.

When an interrupt is accepted, the registers are pushed interrupt inhibit flag I is set, and the program jumps to the address specified in the vector table. The interrupt request flag is cleared automatically. The reset and BRK instruction interrupt can never be inhibited. Other interrupts are disabled when the interrupt inhibit flag is set.

All interrupts except the BRK instruction interrupt have an interrupt request bit and an interrupt enable bit. The interrupt request bits are in interrupt request registers 1 and 2 and the interrupt enable bits are in interrupt control registers 1 and 2. Figure 4 shows the structure of the interrupt request registers 1 and 2 and interrupt control registers 1 and 2.

Interrupts other than the BRK instruction interrupt and reset are accepted when the interrupt enable bit is "1", interrupt request bit is "1", and the interrupt inhibit bit is "0". The interrupt request bit can be reset with a program, but not set. The interrupt enable bit can be set and reset with a program.

Reset is treated as a non-maskable interrupt with the highest priority. Figure 5 shows interrupts control.

Table 1. Interrupt vector address and priority.

Event	Priority	Vector addresses	Remarks
$\overline{\text{RESET}}$	1	$FFFF_{16}$, $FFFE_{16}$	Non-maskable
Input buffer full interrupt	2	$FFFD_{16}$, $FFFC_{16}$	Valid only in slave mode
Output buffer empty interrupt	3	$FFFB_{16}$, $FFFA_{16}$	Valid only in slave mode
INT_1 interrupt	4	$FFF9_{16}$, $FFF8_{16}$	External interrupt (phase programmable)
INT_2 interrupt	5	$FFF7_{16}$, $FFF6_{16}$	External interrupt (phase programmable)
INT_3 interrupt	6	$FFF5_{16}$, $FFF4_{16}$	External interrupt (phase programmable)
Timer 1 interrupt	7	$FFF3_{16}$, $FFF2_{16}$	
Timer 2 interrupt	8	$FFF1_{16}$, $FFF0_{16}$	
Timer 3 interrupt	9	$FFEF_{16}$, $FFEE_{16}$	
EV_1 interrupt	10	$FFED_{16}$, $FFEC_{16}$	External event interrupt (phase programmable)
EV_2 interrupt	11	$FFEB_{16}$, $FFEA_{16}$	External event interrupt (phase programmable)
EV_3 interrupt	12	$FFE9_{16}$, $FFE8_{16}$	External event interrupt (phase programmable)
Serial I/O receive interrupt	13	$FFE7_{16}$, $FFE6_{16}$	Valid only when serial I/O is selected
Serial I/O transmit interrupt	14	$FFE5_{16}$, $FFE4_{16}$	Valid only when serial I/O is selected
A-D conversion completion flag	15	$FFE3_{16}$, $FFE2_{16}$	
BRK instruction interrupt	16	$FFE1_{16}$, $FFE0_{16}$	Non-maskable software interrupt

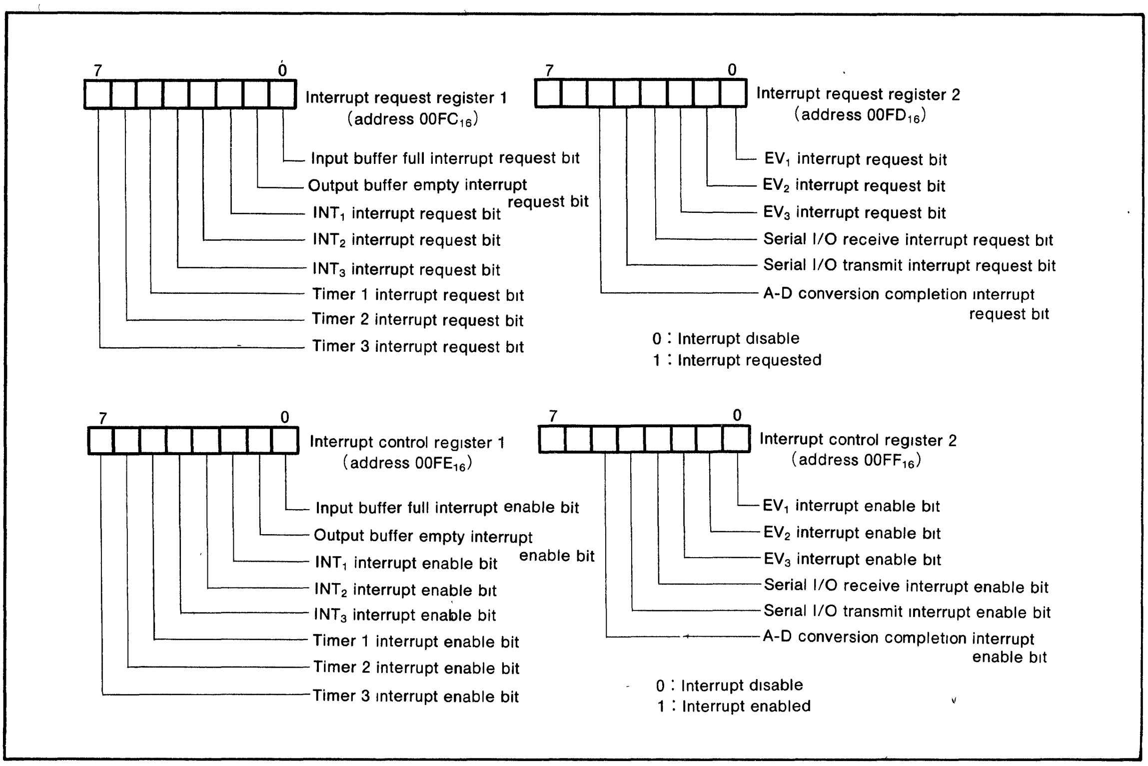


Fig. 4 Structure of registers related to interrupt

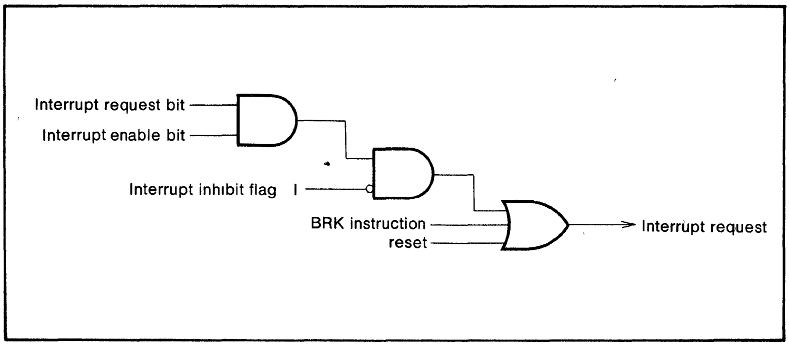


Fig. 5 Interrupt control

TIMER

The M37450 has three independent 16-bit internal timers as shown in Figure 6.

The timers are controlled by the timer i control register (i= 1, 2, 3) and MISRG1 shown in Figure 7 and 8.

The timer and the timer latch are independent of each other and a value must be written in both when setting a timer.

A write to a timer is performed in the order of T_L to T_H after setting the count enable bit to count inhibit "0".

A read from a timer is performed in the order of T_H to T_L. The value of T_L is latched in the read timer latch at the timing when T_H is read. All timers are decrement counters and are started by setting the timer i count enable bit to "1". When the value of the timer reaches 0000_{16}, and overflow occurs and the timer i interrupt request bit is set to "1" at the next count pulse.

During a reset or an STP instruction execution, the low-order byte of the timer 1 register is set to FF_{16} and the high-order byte is set to 03_{16} Also, when an STP instruction is executed, a frequency obtained by dividing the oscillating frequency by four becomes the timer 1 input regardless of the timer 1 count source selection bit. This condition is canceled and the original count source is resumed when the timer i interrupt request bit is set to "1" or when a reset occurs. Refer to the section on the clock generator for details concerning the operation of the STP instruction.

The M37450 provides seven timer modes selectable with the timer mode selection bit in the timer i control register.

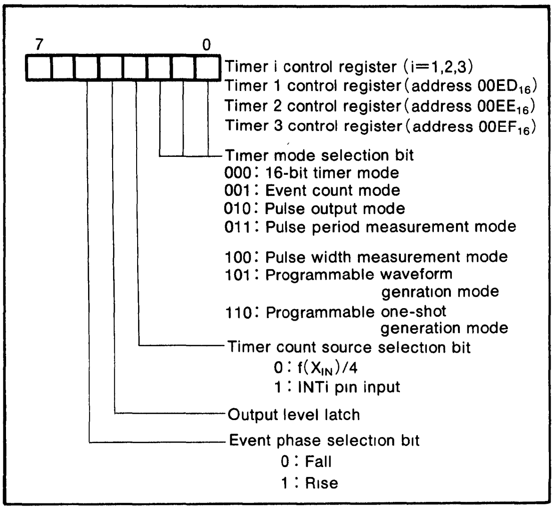


Fig. 7 Structure of timer i control register

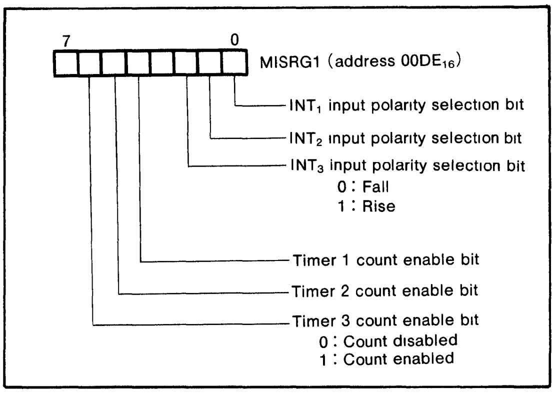


Fig. 8 Structure of MISRG1

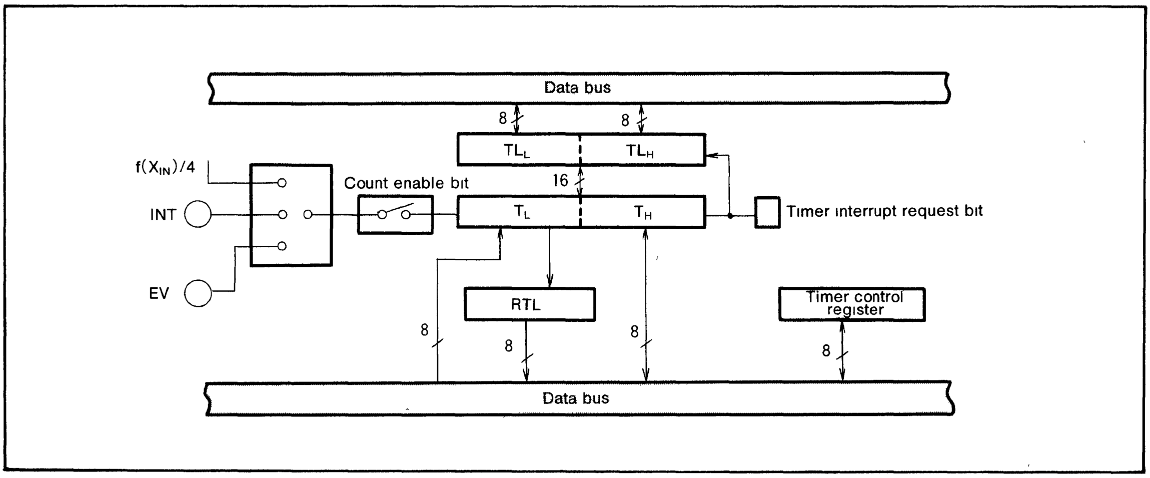


Fig. 6 Timer block diagram

(1) 16-bit Timer Mode [000]

In this mode, an interrupt request occurs and the value of the timer latch is loaded in the timer each time the timer overflows.

The timer count source is set to $f(X_{IN})$ divided by four regardless of the count sorce selection bit. Assuming that the timer latch is n, the frequency dividing ratio is $1/(n+1)$.

Figure 9 shows the timer operation duruing 16-bit timer mode.

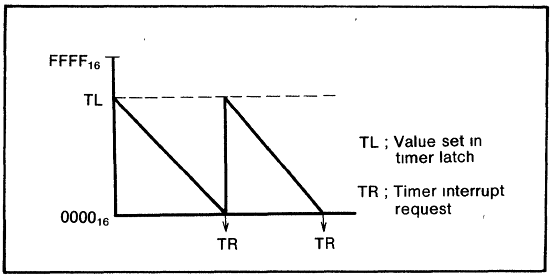


Fig. 9 16-bit timer mode operation

(2) Event Count Mode [001]

In this mode, the EVi pin input signal are counted in the direction selected by the event input polarity selection bit.

The input signal from the EVi pin is used as the count source regardless of the count source selection bit. The operation is the same as with the 16-bit timer mode except for the difference in the count source.

Both the "H" and "L" pulse width of the EVi pin input signal must be not less than $(4/f(X_{IN}))+100$ns.

Figure 10 shows the timer operation during event count mode.

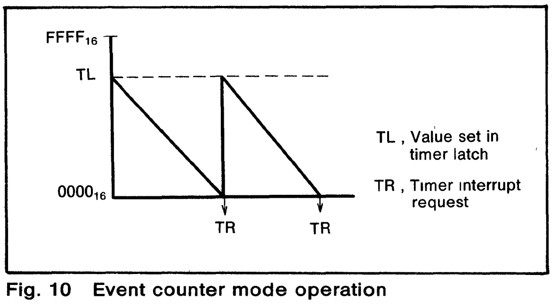


Fig. 10 Event counter mode operation

(3) Pulse Output Mode [010]

In this mode, a 50% duty pulse is output from the EVi pin.

The count source selected with the count source selection bit is counted. When it overflows, the phase of the EVi pin output level is reversed and the value of the timer latch is loaded in the timer.

When this mode is selected, the EVi pin output level is initialized to "L".

Figure 11 shows the timer operation during pulse output mode.

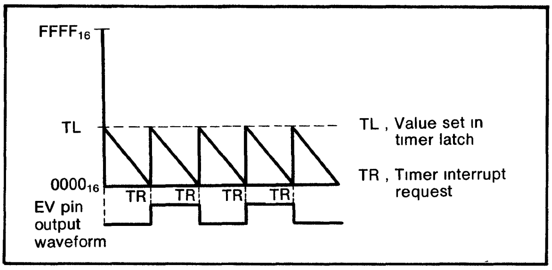


Fig. 11 Square wave output mode

(4) Pulse Period Measurement Mode [011]

This mode is used to measure the pulse period of the EVi pin input signal.

The timer counts the count source selected by the count source selection bit between the rise-to-rise or fall-to-fall interval (selected with the event input polarity selection bit in the timer i control register) of the EVi pin input signal.

At a valid edge on the EVi pin input, the 1's complement of the timer value is stored in the timer latch and the timer value is set to $FFFF_{16}$.

Figure 12 shows the timer operation during pulse frequency measurement mode.

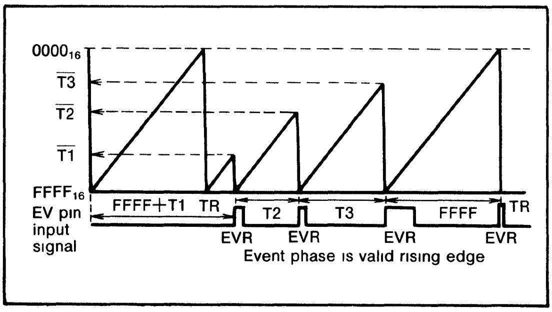
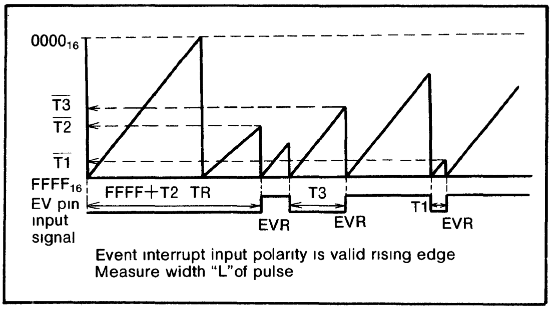


Fig. 12 Pulse period measurement mode

(5) Pulse Width Measurement Mode [100]

This mode measures the pulse width while the EVi pin input signal is "H" or "L".

Whether to measure the "H" or "L" interval is determined by the event input polarity selection bit. If this bit is "0", the count source selected with the count source selection bit is counted while the input pulse is "H". If it is "1", the count source is counted while the input pulse is "L". A 1's complement of the timer value is stored in the timer latch for a valid edge on the EVi pin input. In addition, the timer value is set to $FFFF_{16}$ for an edge (both rise and fall) on the EVi pin input. Figure 13 shows the timer operation during pulse width measurement mode.



Event interrupt input polarity is valid rising edge
Measure width "L"of pulse

Fig. 13 Pulse width measurement mode

In pulse period measurement mode [011] and pulse width measurement mode [100], an EVi interrupt request is issued at the valid edge selected by the event phase selection bit. That is, an interrupt occurs at the end of the pulse period measurement or pulse width measurement. Also, when a timer overflow occurs, the count continues from $FFFF_{16}$ without the value of the timer latch being loaded in the timer.

Write to timer latch is inhibited in these modes. Furthermore, EVi interrupt is disabled during STP instruction execution.

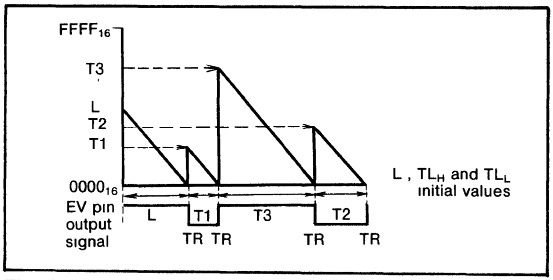
(6) Programmable Waveform Generation Mode [101]

In this mode, the level set in the output level latch of the timer i control register is output to the EVi pin every time the timer overflows.

The timer counts the source selected by the count source selection bit and when it overflows, the value in the timer latch is loaded in the timer.

After it overflows, the value of the output level latch and the timer latch can be modified to generate any waveform from the EVi pin.

Figure 14 shows the timer operation during programmable waveform generation mode.



L , TL_H and TL_L initial values

Fig. 14 Programmable waveform generation mode

(7) Programmable One-shot Generation Mode [110]

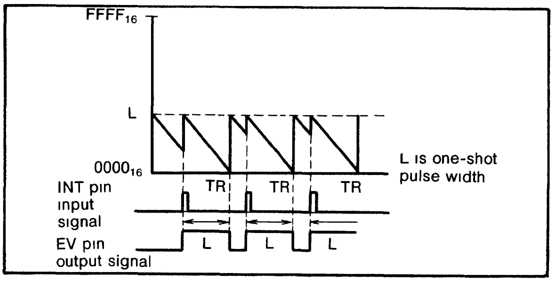
This mode uses the INTi pin input signal as a trigger and counts by writing the value of the timer latch in the timer.

The output level of the EVi pin goes "H" when the trigger is issued and goes "L" when the timer overflows.

The EVi pin level is initialized to "L" when this mode is selected.

The timer count souce is set to $f(X_{IN})$ divided by four regardless of the count source selection bit.

A valid edge of the INTi pin input trigger signal is determined by the INTi phase selection bit of MISRG1 ($00DE_{16}$). Figure 15 shows the timer operation during programmable one-shot generation mode.



L is one-shot pulse width

Fig. 15 Programmable one-shot generation mode

When the INTi pin input signal is selected as the count source for pulse output mode [010], pulse period measurement mode [011], pulse width measurement mode [100], and programmable waveform generation mode [101], the "H" and "L" pulse width of the input signal must not be less than $(6/f(X_{IN}))+100ns$.

SERIAL I/O

Serial I/O can operate in either clock synchronous or clock asynchronous (UART) mode. An exclusive baud rate generation timer (baud rate generator) is provided for serial I/O operation. Figure 16 shows the structure of the registers used for serial I/O.

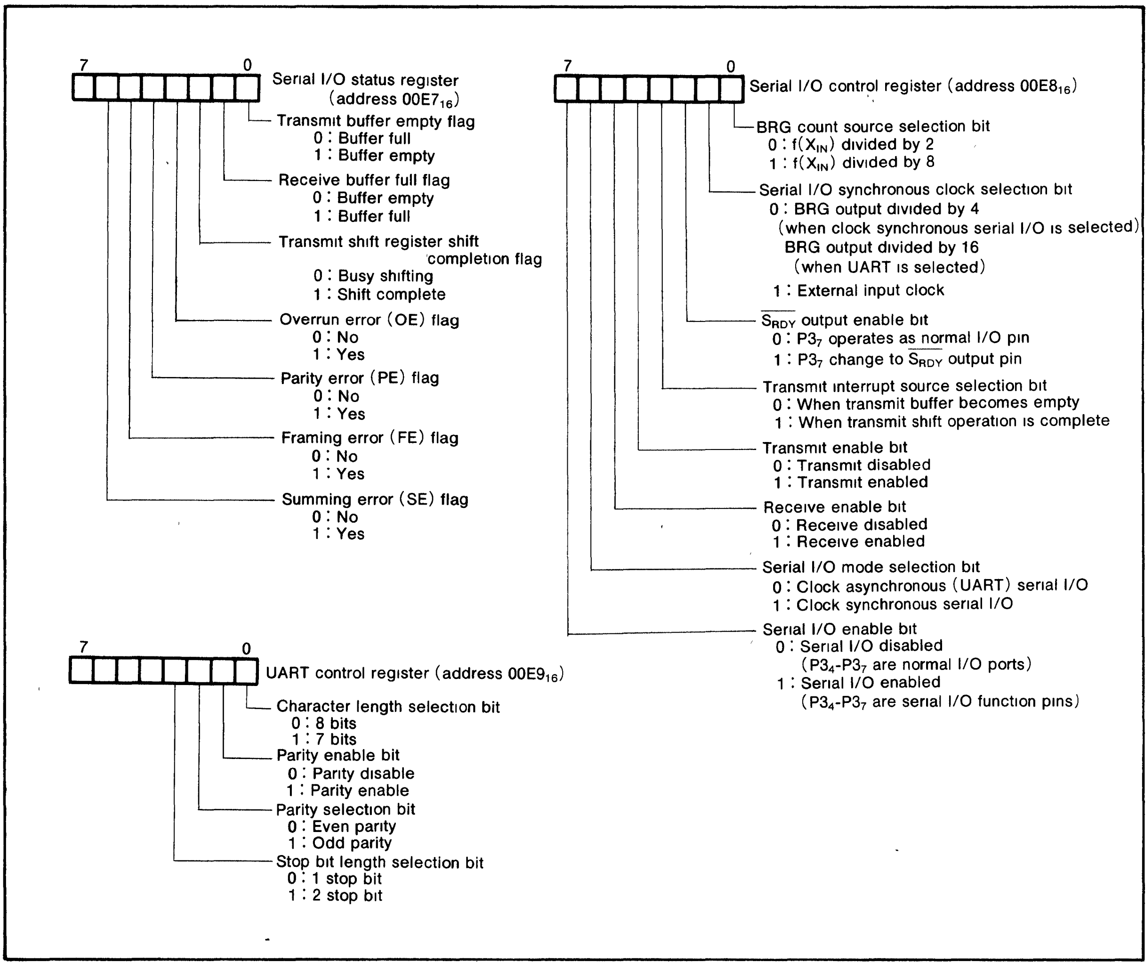


Fig. 16 Structure of registers related to serial I/O

(1) Clock Synchronous Serial I/O

Clock synchronous serial I/O is selected by setting the mode selection bit of the serial I/O control register to "1". Figure 17 shows a block diagram of clock synchronous serial I/O and Figure 18 shows its operation.

With clock synchronous serial I/O, the same clock is used as the operating clock between the transmitting and receiving microcomputers. If an internal clock is used for operating clock, transmit/receive is started by writing a signal in the transmit/receive buffer register.

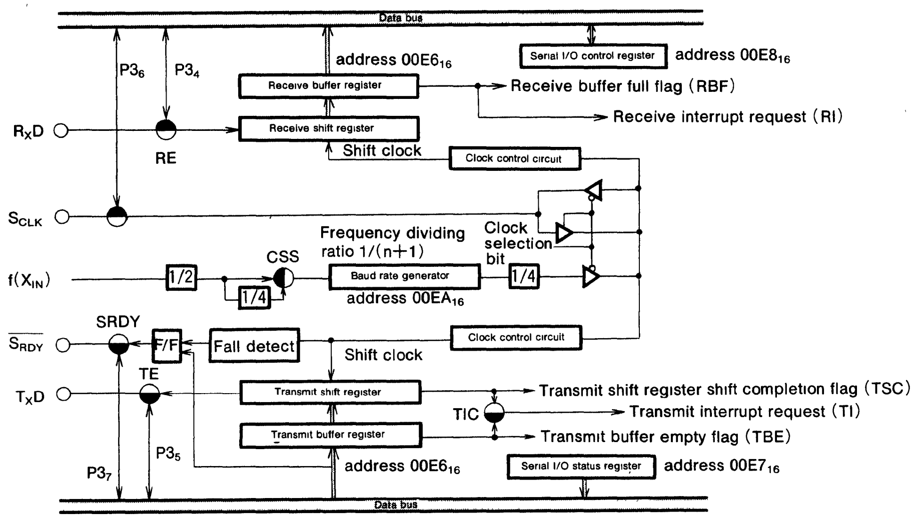
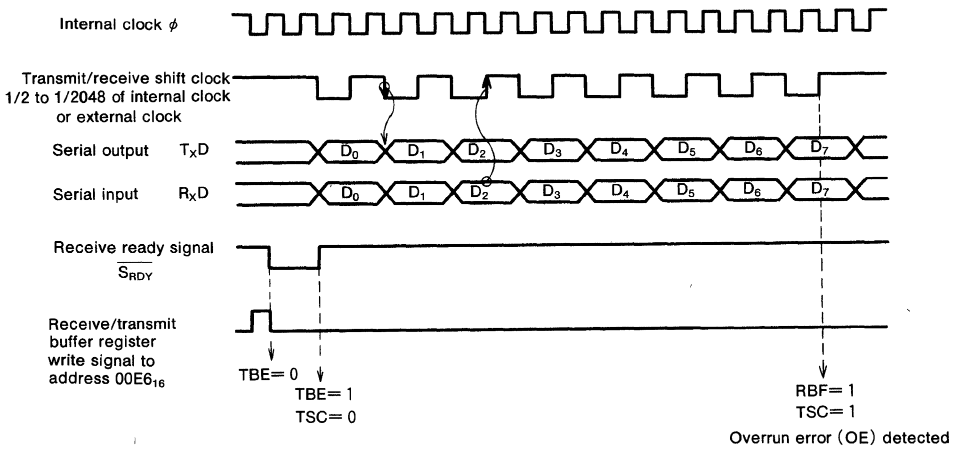


Fig. 17 Clock synchronous serial I/O block diagram



Note 1. Use the transmit interrupt source selection bit (TIC) in the serial I/O control register to specify whether to generate a transmit interrupt (TI) when the transmit buffer becomes empty (TBE=1) or when transmit shift operation completes (TSC=1)

2. If data is written in the transmit buffer register when TSC=0, transmit clock is generated continuously and serial data is output continuously from the T_XD pin.

3. The receive interrupt (RI) is set when the receive buffer full flag (RBF) is set

4. This example shows the case that the BRG count source is $f(X_{IN})/2$ and the contents of BRG reload latch is "00_{16}"

Fig. 18 Clock synchronous serial I/O operation

(2) Asynchronous Serial I/O (UART)

UART is selected by setting the mode selection bit of the serial I/O control register to "0". Figure 19 shows a block diagram of UART and Figure 20 shows its operation.

With the M37450, one of eight serial data transmission formats can be selected with the UART control register as shown in Figure 16. The transmission format must be agreed upon between the transmit side and the receive side.

The transmit shift register and the receive shift register has its buffer register respectively to perform serial data transfer (same memory addresses).

Data cannot be written or read directly to/from the shift registers. Therefore, the data to be transmitted is written to a buffer register and the received data is read from a buffer register. The buffer registers can also be used to store data to be transmitted next or to receive 2-byte data consecutively.

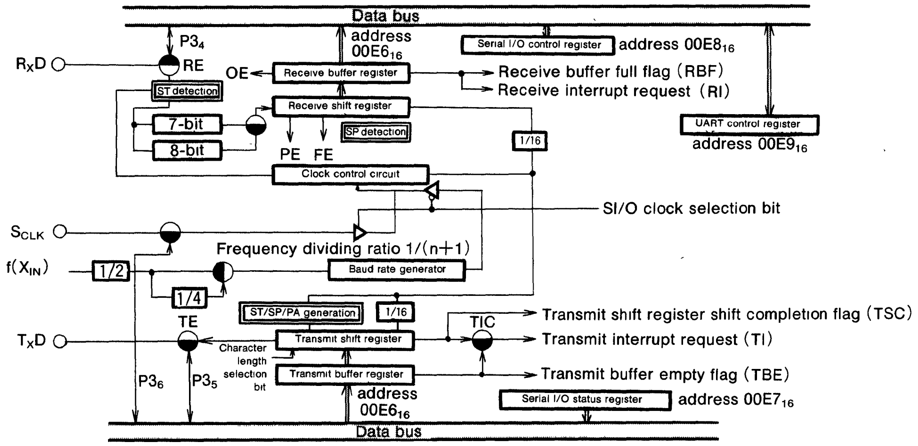
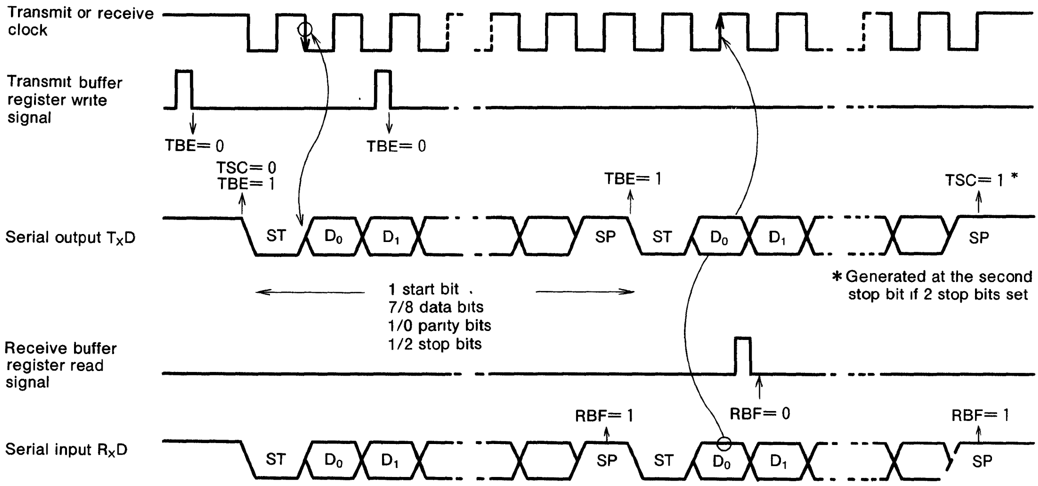


Fig. 19 UART serial I/O block diagram



Note 1. Error flag detection is performed as soon as RBF=1 (first stop bit for receive)
2. Transmit interrupt (TI) is set to either TBE=1 or TSC=1 according to the transmit interrupt source selection bit (TIC) in the serial I/O control register
3. Receive interrupt (RI) is set by RBF=1

Fig. 20 UART serial I/O operation

[Serial I/O control register] SIOCON

The serial I/O control register is an 8-bit register consisting of selection bits for controlling the serial I/O function.

- **Serial I/O enable bit SIOE**

When this bit is set to "1", serial I/O is enabled and pins $P3_4$~$P3_7$ can be used as serial I/O function pins.

- **Serial I/O mode selection bit SIOM**

This bit is used to select the serial I/O operation mode. When this bit is "0", asynchronous serial I/O (UART), which transfers data using start and stop bits, is selected. When it is "1", clock synchronous serial I/O which performs transmission and receive using the same clock is selected.

- **Receive enable bit RE**

Receive operation is enabled when this bit is set to "1" and pin $P3_4$ becomes a serial data input pin.

- **Transmission enable bit TE**

Transmission operation is enabled when this bit is set to "1". Pin $P3_5$ becomes a serial data output pin and shift data is output.

- **Transmission interrupt source selection bit TIC**

This bit is used to selelct events that can cause a transmission interrupt.

- **$\overline{S_{RDY}}$ output enable bit SRDY**

If this bit is set to "1" when clock synchronous serial I/O is selected, pin $P3_7$ becomes an $\overline{S_{RDY}}$ signal output pin and $\overline{S_{RDY}}$ signal is output.

When an external clock is used during clock synchronous serial I/O, the $\overline{S_{RDY}}$ signal is used to notify the clock sender that it can send the serial clock signal. It goes "L" when data is written in the transmit/receive buffer register and goes "H" at the first fall of the receive clock. When using the $\overline{S_{RDY}}$ signal, the transmission enable bit must be set to "1" even when performing receive only.

- **Serial I/O synchronous clock selection bit SCS**

When this bit is "1", pin $P3_6$ becomes an input pin and the external clock input from the S_{CLK} pin is selected as the serial I/O synchronous clock. When this bit is "0", the baud rate generator (BRG) overflow signal is selected as the serial I/O synchronous clock. Also, when this bit is "0" during clock synchronous serial I/O, pin $P3_6$ becomes an output pin and the shift clock is output from the S_{CLK} pin.

When clock synchronous serial I/O is selected, the baud rate generator (BRG) output signal divided by four or an external clock input is used. When UART is selected, the BRG output signal divided by sixteen or an external clock input signal divided by sixteen is used.

- **BRG count source selection bit CSS**

The baud rate generator is an 8-bit counter with a reload register. By setting a value n in the BRG register (address $00EA_{16}$), the count source selected by the BRG count source selection bit is divided by $(n+1)$.

[UART control register] UARTCON

The UART control regsiter is a 4-bit register consisting of control bits that are valid when UART is selected. The content of this register is used to set the data format for serial data transmission/receiving.

- **Character length selection bit CHAS**

This bit is used to select the transmission/receiving character length.

- **Parity enable bit PARE**

When this bit is set to "1", a parity bit is added next to the most significant bit (MSB) of the transmission data and parity is checked during receive.

- **Parity selection bit PARS**

This bit is used to specify the type of parity to be generated during transmission and checked when data is received. The number of 1's in the data is set to even or odd according to this bit.

- **Stop bit length selection STPS**

This bit is used to determine the number of stop bits to be used during transmission.

[Serial I/O status register] SIOSTS

The serial I/O status register is a 7-bit read only register consisting of serial I/O operation status flags and error flags. Bits 4 to 6 are valid only during UART mode.

All bits of this register are initialized to "0" at reset, and when the transmit enable bit in the serial I/O control register is set to "1", bits "0" and "2" change to "1".

- **Transmission buffer empty flag TBE**

This bit is cleared to "0" when transmission data is written in the transmission buffer register and set to "1" when that data is transferred to the transmit shift register. It is also cleared when TE=0.

- **Receive buffer full flag RBF**

When receiving serial data, data is transferred to the receive buffer register and this bit is set to "1" when the receive shift register completes receiving a data byte. This bit is cleared when the data is read. This bit is also cleared when RE=0.

- **Transmit shift register shift completion flag TSC**

This bit is cleared to "0" when the data in the transmission buffer register is transferred to the transmit shift register and set to "1" when data shift completes. It is also set to "1" when TE=0.

- **Overrun error flag OE**

When continuously receiving serial data, this bit is set when the next data fill the receive shift register before the data in the receive buffer register has been read.

- **Parity error flag PE**

When receiving serial data with parity, this bit is set to "1" if the parity of the received data differs from the specified parity.

- **Framing error flag FE**

This bit is set to "1" when there is no stop bit when transferring data from the receive shift register to the receive buffer.

- **Summing error flag SE**

This bit is set when either overrun, a parity, or a framing error occurs.

Tests for these errors are performed as soon as the data is transferred from the receive shift register to the receive buffer register and at the same time the receive buffer full flag is set. The error flags (OE, PE, FE, and SE) are cleared when any data is written in the serial I/O status register. Also, all status flags including error flags are cleared when SIOE=0.

BUS INTERFACE

The M37450 is equipped with a bus interface that is functionally similar to the MELPS 8-41 series. Its operation can be controlled with control signals from the host CPU (slave mode).

The M37450 bus interface can be connected directly to either a R/$\overline{W}$ type CPU or separate $\overline{RD}$, $\overline{WR}$ type CPU. Figure 21 shows a block diagram of the bus interface function.

Slave mode is selected with MISRG2 (address 00DF$_{16}$) bit 2 and 3 as shown in Figure 22.

An input buffer full interrpt occurs when data is received from the host CPU and an output buffer empty interrupt occurs when data is read by the host CPU.

In slave mode, ports P5$_0$-P5$_7$ become a tri-state data bus used to transfer data, commands, and status to and from the host CPU.

Furthermore, ports P6$_4$-P6$_7$ become host CPU control signal input pins and P6$_3$ becomes a slave status output pin.

[Data bus buffer status register] DBBSTS

This is an 8-bit register. Bits 0, 1, and 3 are read-only bits indicating the status of the data bus buffer. Bits 2, 4, 5, 6, and 7 are read/write enabled user-definable flags that can be set with a program. The host CPU can only read these flags by setting the A0 pin to "H".

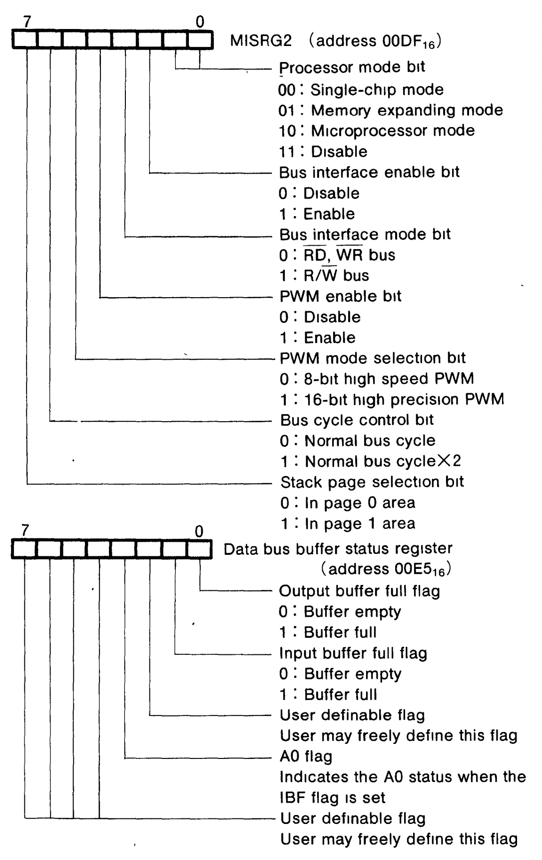


Fig. 22 Structure of bus interface relation registers

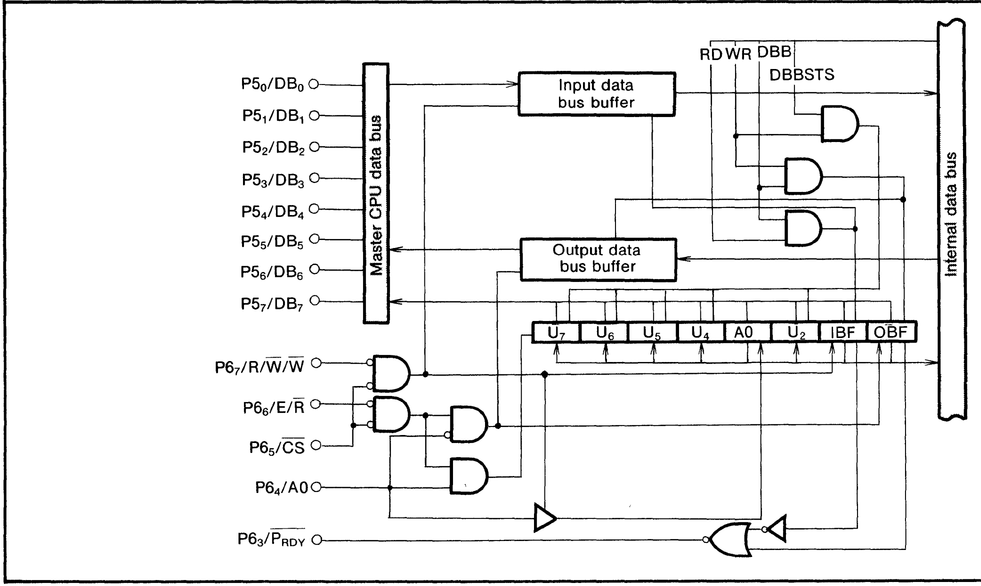


Fig. 21 Bus interface circuit diagram

- **Output buffer full flag OBF**

This flag is set when data is written in the output data bus buffer and cleared when the host CPU reads the data in the output data bus buffer. It is initialized to "1" at reset and cleared to "0" when the slave mode is selected with the bus interface enable bit set.

- **Input buffer full flag IBF**

This flag is set when the host CPU writes data in the input data bus buffer and cleared when the slave CPU reads the data in the input data bus buffer. This bit is initialized to "0" at reset.

A0 Flag

The level of the A0 pin is latched when the host CPU writes data in the input data bus buffer.

[Input data bus buffer] DBBIN

Data on the data bus is latched in DBBIN when there is a write request from the host CPU. The data in DBBIN can be read from the data bus buffer register (SFR address $00E4_{16}$).

[Output data bus buffer] DBBOUT

Data is written in DBBOUT by writing data in data bus buffer register (SFR address $00E4_{16}$). The data in DBBOUT is output to the data bus (P5) when the host CPU issues a read request with setting the A0 pin to "L".

Table 2. Control I/O pin functions when bus interface function is selected

Pin	Name	Bus interface mode bit	Input/ Output	Function
$P6_3$	$\overline{P_{RDY}}$	—	Output	Status output The NOR of OBF and IBF is output
$P6_4$	A0	—	Input	Address input Used to select between DBBSTS and DBBOUT during host CPU read Also used to identify commands and data during write
$P6_5$	$\overline{CS}$	—	Input	Chip select input Used to select the data bus buffer Select when "L"
$P6_6$	$\overline{R}$	0	Input	Timing signal used by the host CPU to read data from the data bus buffer
	E	1	Input	Inputs a timing signal E or inverse of ϕ
$P6_7$	$\overline{W}$	0	Input	Timing signal used by the host CPU to write data to the data bus buffer
	R/$\overline{W}$	1	Input	Input R/$\overline{W}$ signal used to control the data transfer direction When this signal is "L", data bus buffer write is synchronized with the E signal When it is "H", data bus buffer read is synchronized with the E signal

PWM

The PWM generator has two program-selectable modes; the high-speed mode (8-bit resolution) and the high-precision mode (16-bit resolution). Figure 23 shows a block diagram.

The register MISRG2 (address $00DF_{16}$) shown in Figure 22 is used to enable/disable the PWM and change its mode. When the PWM enable bit is set, the PWM timer starts from its initial state.

As shown in Figure 24, the output frequency is

$(2X255)/f(X_{IN})$ 51μs at $f(X_{IN})=10MHz$

in high-speed mode and

$(2X65535)/f(X_{IN})$ 13.107ms at $f(X_{IN})=10MHz$

in high-precision mode.

The "H" width of the output pulse is determined by setting a value only in the PWM_L register for high-speed mode and in both the PWM_H and PWM_L in this order for high-precision mode.

If the value set in the PWM register is m, the "H" width of the output pulse is

(PWM period$\times$m)/255 for high-speed mode and

(PWM period$\times$m)/65535 for high-precision mode.

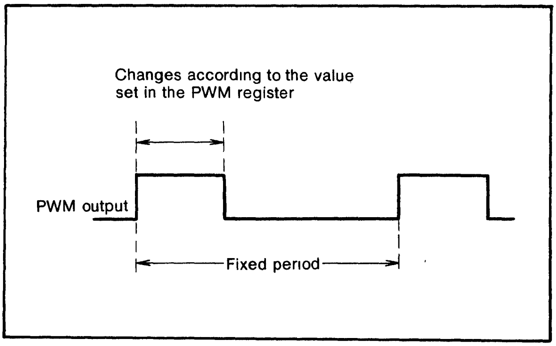


Fig. 24 PWM output

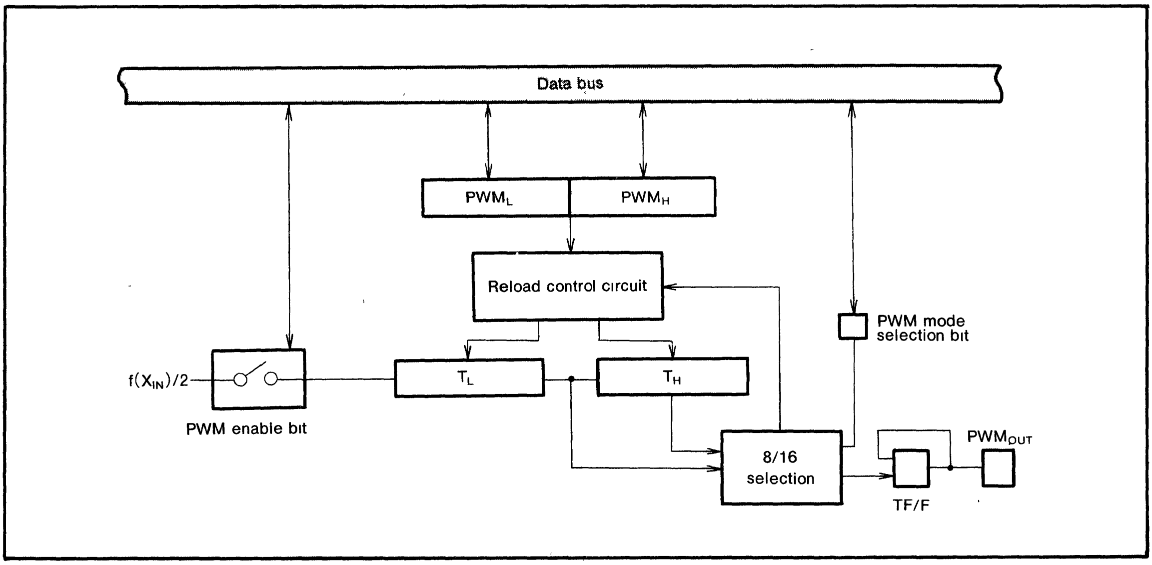


Fig. 23 PWM generator block diagram

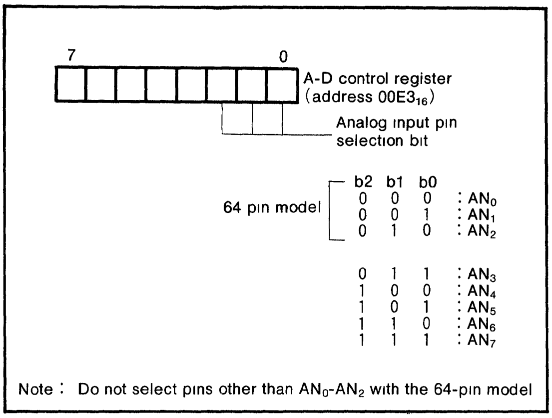
A-D CONVERTER

An A-D converter is an 8-bit successive approximation method. Figure 26 shows a block diagram of the A-D converter.

The 64-pin model has three analog voltage input pins, the 80-pin model has eight.

A-D conversion is started by a write operation to the analog input pin selection bit of the A-D control register shown in Figure 25 and by selecting the analog voltage input pin. The A-D interrupt request bit in the interrupt request register 2 is set when A-D conversion completes. The result of A-D conversion is stored in the A-D register.

The contents of the A-D register must not be read during A-D conversion and $f(X_{IN})$ must be no less than 1 MHz during A-D conversion.



Note : Do not select pins other than AN_0-AN_2 with the 64-pin model

Fig. 25 Structure of A-D control register

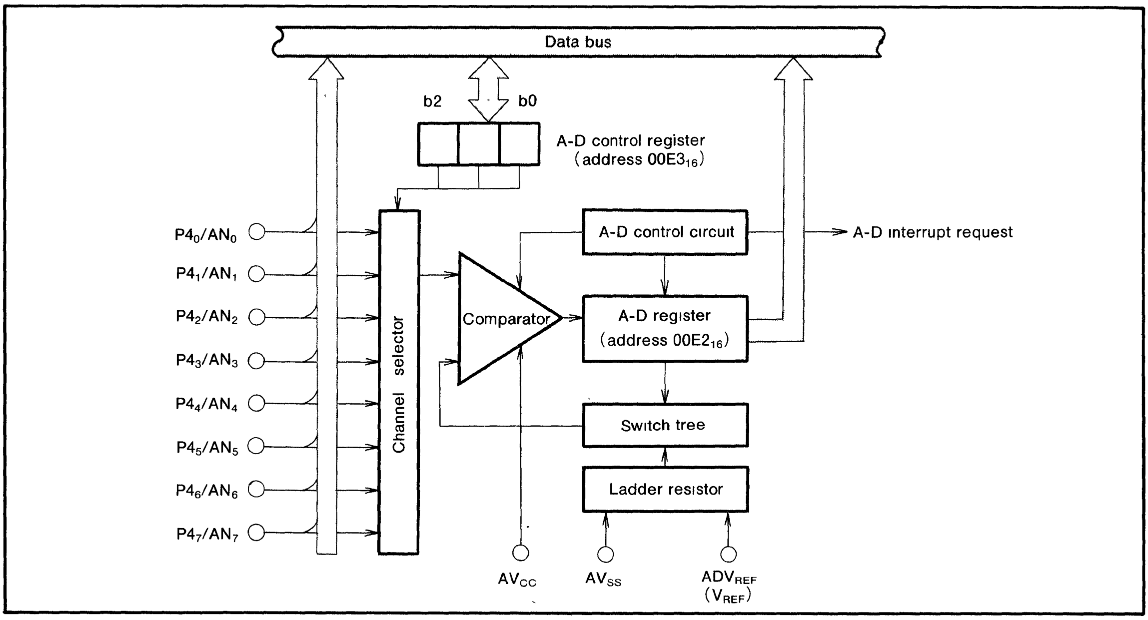


Fig. 26 A-D converter block diagram

D-A CONVERTER

Two 8-bit resolution D-A converter channels are provided. Figure 27 shows a block diagram of the D-A converter.

D-A conversion is performed by setting a value in the D-Ai register (addresses $00E0_{16}$ and $00E1_{16}$). The result of D-A conversion is output from the D-Ai output pin.

The output analog voltage V_{DA} is determined by the value n (decimal) set in the D-Ai register as follows:

$V_{DA}=DAV_{REF}{}^{*}\times n/256$

$*V_{REF}$ for 64-pin model.

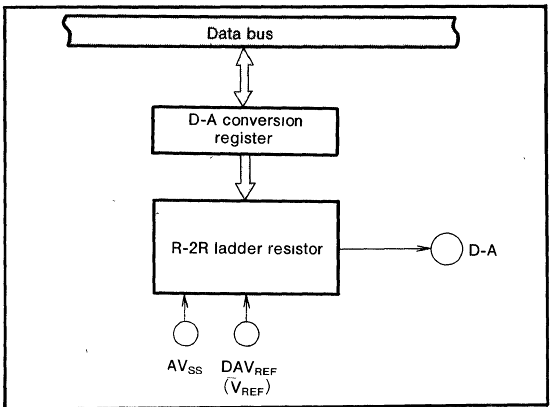


Fig. 27 D-A converter block diagram

RESET CIRCUIT

The M37450 is reset according to the sequence shown in Figure 30. It starts the program from the address formed by using the content of address FFFF$_{16}$ as the high order address and the content of the address FFFE$_{16}$ as the low order address, when the $\overline{\text{RESET}}$ pin is held at "L" level for no less than 8 clock cycles while the power voltage is 5V± 10% and the crystal oscillator oscillation is stable and then returned to "H" level. The internal initializations following reset are shown in Figure 28.

An example of the reset circuit is shown in Figure 29. The reset input voltage must be kept below 0.6V until the supply voltage surpasses 4.5V.

	address								
(1) Port P0 directional register	00D1$_{16}$	00$_{16}$							
(2) Port P1 directional register	00D3$_{16}$	00$_{16}$							
(3) Port P2 directional register	00D5$_{16}$	00$_{16}$							
(4) Port P3 directional register	00D7$_{16}$	00$_{16}$							
(5) Port P4 directional register	00DB$_{16}$	00$_{16}$							
(6) Port P5 directional register	00DD$_{16}$	00$_{16}$							
(7) MISRG1	00DE$_{16}$		0	0	0		0	0	0
(8) MISRG2	00DF$_{16}$	00$_{16}$							
(9) D-A1 register	00E0$_{16}$	00$_{16}$							
(10) D-A2 register	00E1$_{16}$	00$_{16}$							
(11) Data bus buffer status register	00E5$_{16}$							0	1
(12) Serial I/O status register	00E7$_{16}$		0	0	0	0	0	0	0
(13) Serial I/O control register	00E8$_{16}$	00$_{16}$							
(14) UART control register	00E9$_{16}$					0	0	0	0
(15) Timer 1 control register	00ED$_{16}$			0	0	0	0	0	0
(16) Timer 2 control register	00EE$_{16}$			0	0	0	0	0	0
(17) Timer 3 control register	00EF$_{16}$			0	0	0	0	0	0
(18) Timer 1 register (low order)	00F0$_{16}$	FF$_{16}$							
(19) Timer 2 register (high order)	00F1$_{16}$	03$_{16}$							
(20) Interrupt request register 1	00FC$_{16}$	00$_{16}$							
(21) Interrupt request register 2	00FD$_{16}$			0	0	0	0	0	0
(22) Interrupt control register 1	00FE$_{16}$	00$_{16}$							
(23) Interrupt control register 2	00FF$_{16}$			0	0	0	0	0	0
(24) Processor status register	(PS)						1		
(25) Program counter	(PC$_H$)	Contents of address FFFF$_{16}$							
	(PC$_L$)	Contents of address FFFE$_{16}$							

Note. Since the contents of both registers other than those listed above (including timer 1, timer 2, timer 3, and the serial I/O register) and the RAM are undefined at reset, it is necessary to set initial values

Fig. 28 Internal state of microcomputer at reset

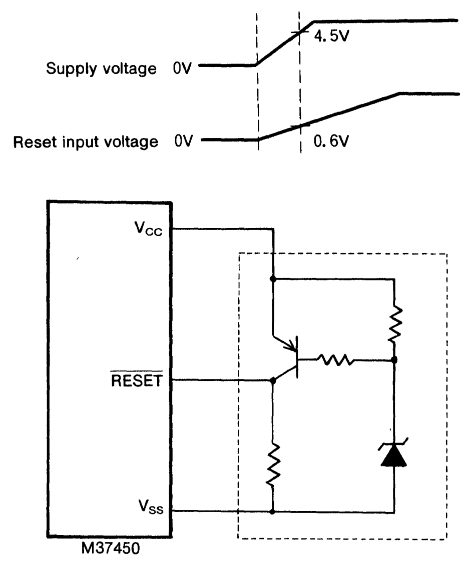
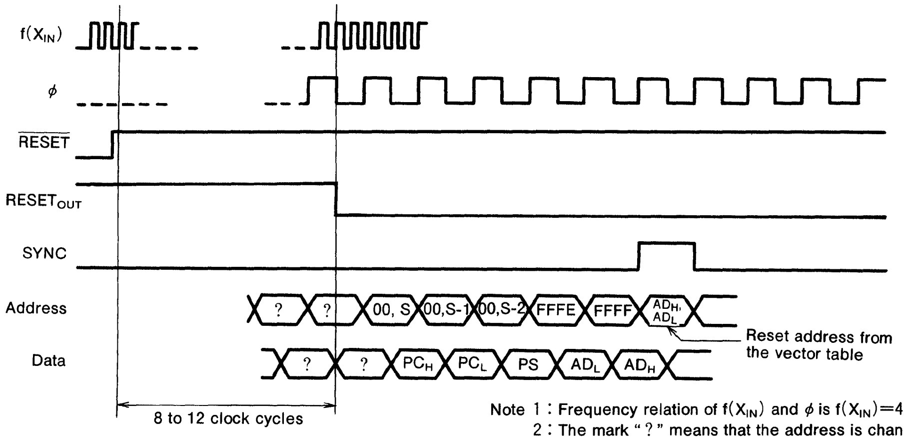


Fig. 29 Example of reset circuit



Note 1 : Frequency relation of $f(X_{IN})$ and ϕ is $f(X_{IN})=4 \cdot \phi$.
2 : The mark " ? " means that the address is changable depending upon the previous state.

Fig. 30 Timing diagram at reset

I/O PORTS

(1) Port P0

Port P0 is an 8-bit I/O port with CMOS output.
As shown in the memory map (Figure 2), port P0 can be accessed at zero page memory address $00D0_{16}$.
Port P0 has a directional register (address $00D1_{16}$) which can be used to program each individual bit as input ("0") or as output ("1"). If the pins are programmed as output, the output data is latched to the port register and then output. When data is read from the output port the output pin level is not read, only the latched data in the port register is read. This allows a previously ouptut value to be read correctly even though the output voltage level is shifted up or down. Pins set as input are in the floating state and the signal levels can thus be read. When data is written into the input port, the data is latched only to the port latch and the pin still remains in the floating state.
Depending on the contents of the processor status register (bit 0 and bit 1 at address $00DF_{16}$), three different modes can be selected; single-chip mode, memory expanding mode and microprocessor mode.
In these modes it functions as address (A_7-A_0) output port (excluding single-chip mode). For more details, see the processor mode information.

(2) Port P1

In single-chip mode, port P1 has the same function as port P0. In other modes, it functions as address (A_{15}-A_8) output port.
Refer to the section on processor modes for details.

(3) Port P2

In single-chip mode, port P2 has the same function as port P0. In other modes, it functions as data (D_0-D_7) input/output port. Refer to the section on processor modes for details.

(4) Port P3

Port P3 is an 8-bit I/O port with function similar to port P0. All pins have program selectable dual functions. When a serial I/O function is selected, the input and output from pins $P3_4$-$P3_7$ are determined by the contents of the serial I/O registers.
This port is unaffected by the processor mode.

(5) Port P4

This is an input-only port and may be used as an analog voltage input port. The number of ports is different for the 64-pin model and 80-pin model. The 64-pin model has three ports and the 80-pin model has eight ports.

(6) Port P5

This is an 8-bit I/O port with function similar to port P0. When slave mode is selected with a program, all ports change to the data bus for the master CPU. In this case, port input/output is unaffected by the directional register.
This port is unaffected by the processor mode register.

(7) Port P6

This is an 8-bit input/output port with function similar to port P0.
When slave mode is selected with a program, ports $P6_3$-$P6_7$ change to the control bus for the bus interface function. In this case, port input/output is unaffected by the directional register.
Ports $P6_0$-$P6_2$ are shared with the external interrupt input pins (INT_1-INT_3). The INT interrupt constantly monitors the status of this port and generates an interrupt at a valide edge. Therefore, if the INT interrupt is not used, it must be disabled and if it is used, this port must be set to input.

(8) Port D-A

Port D-A consists of two analog voltage output pins. Any analog voltage can be generated by setting a value in the D-A register.

(9) ϕ pin

The internal system clock (1/4 the frequency of the oscillator connected between the X_{IN} and X_{OUT} pins) is output from this pin. If an STP or WIT instruction is executed, output stops after going "H".

(10) SYNC pin

This pin outputs a signal that is "H" during one cycle of the ϕ during operation code fetch.

(11) $R/\overline{W}$ pin

This is a control signal output pin that indicates the local bus direction in memory expanding and microprocessor modes.

(12) $\overline{RD}$, $\overline{WR}$ pins

These are local bus write and read timing signal output pins for memory expanding and microprocessor modes. A signal equivalent to the signal otuput from the $R/\overline{W}$ separated by the ϕ signal is output.
These pins are used exclusively by the 80-pin model.

(13) $RESET_{OUT}$ pin

This pin goes "H" while the microprocessor is being reset. It can be used as a reset signal output pin for peripheral devices.
This pin is used exclusively by the 80-pin model.

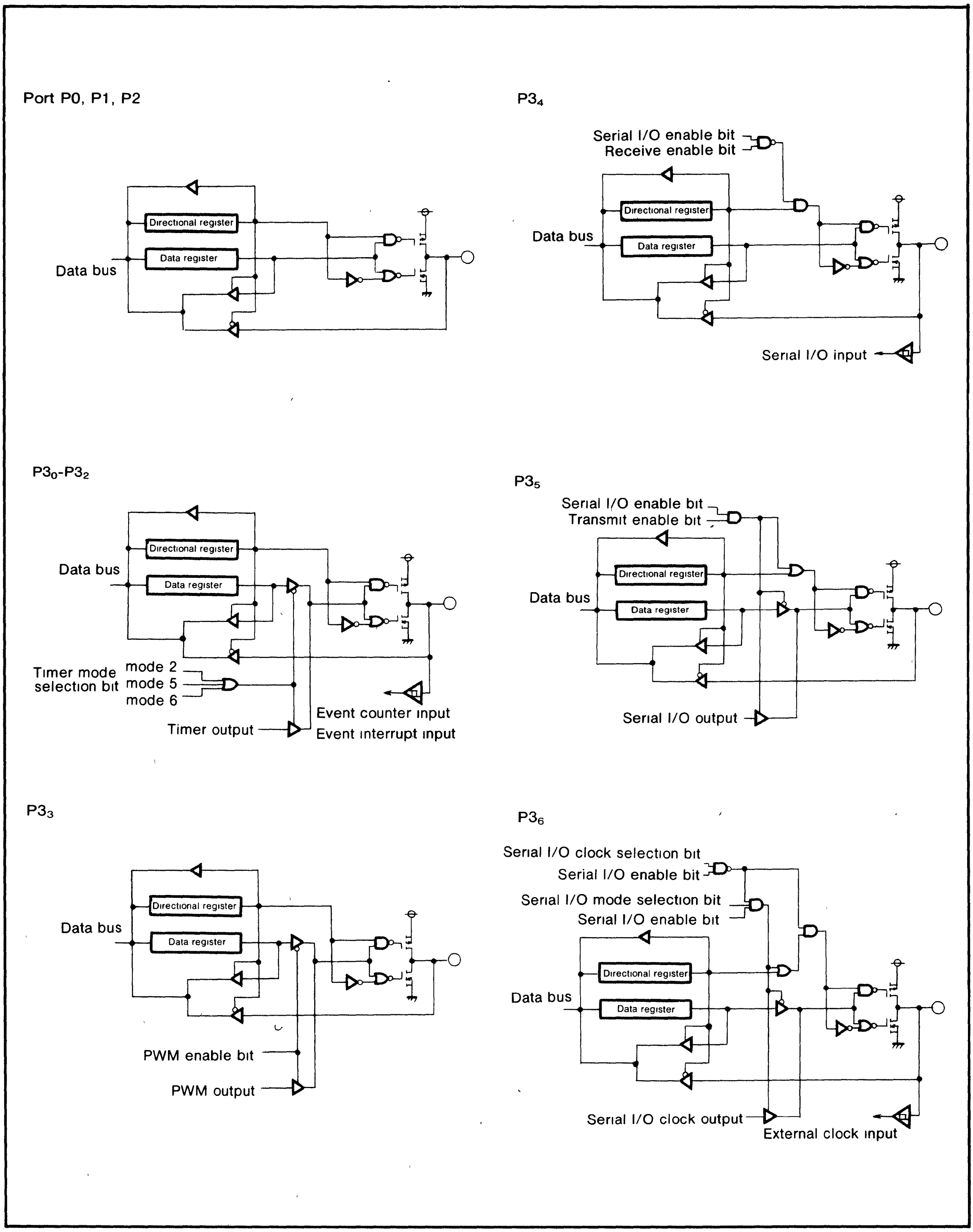
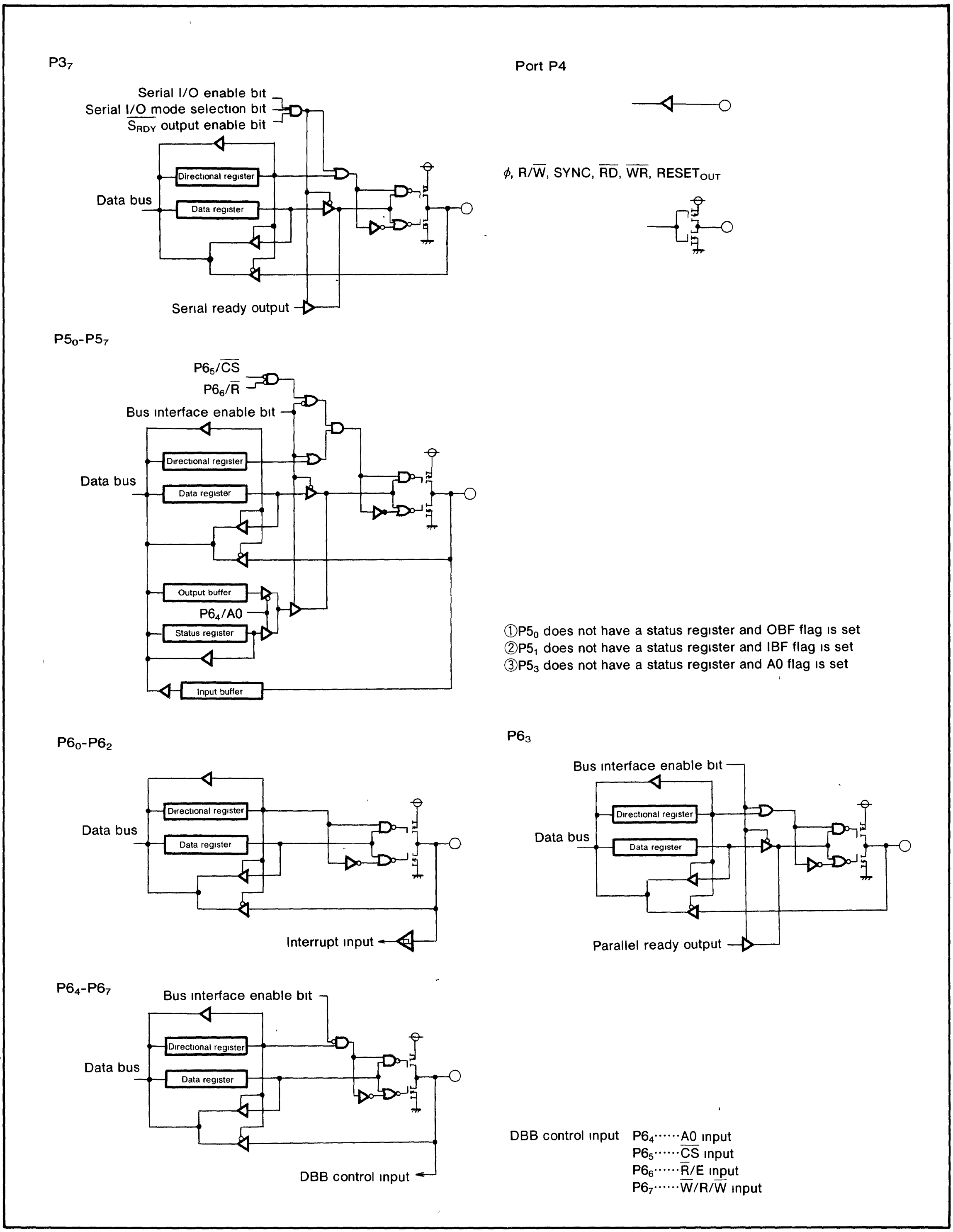


Fig. 31 Ports P0-P6 block diagram (single-chip mode) and output only pin output format (1)



①$P5_0$ does not have a status register and OBF flag is set
②$P5_1$ does not have a status register and IBF flag is set
③$P5_3$ does not have a status register and A0 flag is set

DBB control input $P6_4$······A0 input
$P6_5$······$\overline{CS}$ input
$P6_6$······$\overline{R}$/E input
$P6_7$······$\overline{W}$/R/$\overline{W}$ input

Fig. 32 Ports P0-P6 block diagram (single-chip mode) and output only pin output format (2)

PROCESSOR MODE

By changing the contents of the processor mode bit (bit 0 and 1 at address 00DF$_{16}$), three different operation modes can be selected; single-chip mode, memory expanding mode, and microprocessor mode

In the memory expanding mode and the microprocessor mode, ports P0-P2 can be used as address, and data input/output pins.

Figure 34 shows the functions of ports P0-P2.

The memory map for the single-chip mode is illustrated in Figure 1 and for other modes, in Figure 33.

By connecting CNV$_{SS}$ to V$_{SS}$, all three modes can be selected through software by changing the processor mode bits. Connecting CNV$_{SS}$ to V$_{CC}$ automatically forces the microcomputer into microprocessor mode.

The three different modes are explained as follows:

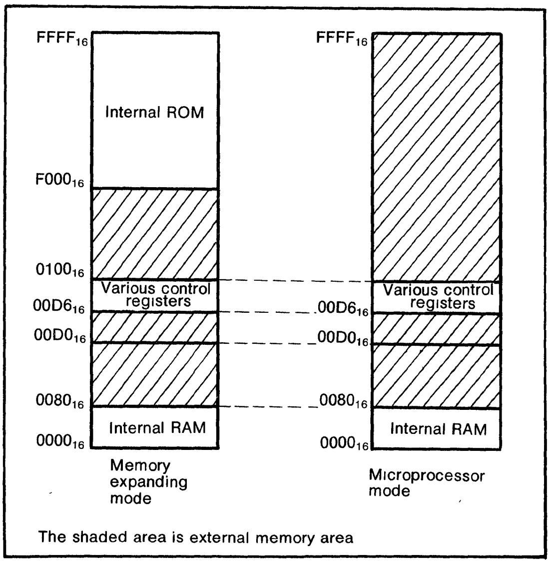


Fig. 33 External memory area in processor mode (M37450M2)

(1) Single-chip mode [00]
The microcomputer will automatically be in the single-chip mode when started from reset, if CNV$_{SS}$ is connected to V$_{SS}$. Ports P0-P2 will work as original I/O ports

(2) Memory expanding mode [01]
The microcomputer will be placed in the memory expanding mode when CNV$_{SS}$ is connected to V$_{SS}$ and the processor mode bits are set to "01". This mode is used to add external memory when the internal memory is not sufficient.
In this mode, port P0 and port P1 are as a system address bus and the original I/O pin function is lost.
Port P2 becomes the data bus of D$_7$-D$_0$ (including instruction code) and loses its normal I/O functions.

(3) Microprocessor mode [10]
After connecting CNV$_{SS}$ to V$_{CC}$ and initiating a reset or connecting CNV$_{SS}$ to V$_{SS}$ and the processor mode bits are set to "10", the microcomputer will automatically default to this mode. In this mode, the internal ROM is inhibited so the external memory is required Other functions are same as the memory expanding mode. The relationship between the input level of CNV$_{SS}$ and the processor mode is shown in Table 3.

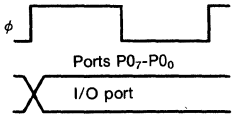
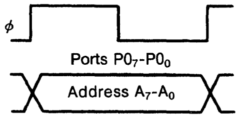
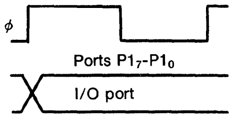
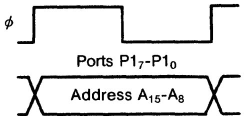
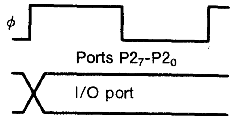
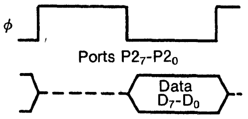
CM_1	0	0	1
CM_0	0	1	0
Mode Port	Single-chip mode	Memory expanding mode	Microprocessor mode
Port P0			Same as left
Port P1			Same as left
Port P2			Same as left

Fig. 34 Processor mode and function of port P0-P2

Table 3. Relationship between CNV_{SS} pin input level and processor mode

CNV_{SS}	Mode	Explanation
V_{SS}	• Single-chip mode • Memory expanding mode • Microprocessor mode	The single-chip mode is set by the reset All modes can be selected by changing the processor mode bit with the program
V_{CC}	• Microprocessor mode	The microprocessor mode is set by the reset

CLOCK GENERATING CIRCUIT

The built-in clock generating circuits are shown in Figure 37.

When an STP instruction is executed, the internal clock ϕ stops oscillating at "H" level At the same time, FF_{16} is set in the low-order byte of timer 1, 03_{16} is set in the high-order byte, and timer 1 count source is forced to f(X_{IN}) divided by four. This connection is cleared when timer 1 overflows or the reset is in, as discussed in the timer section.

The oscillator is restarted when an interrupt is accepted However, the clock ϕ keeps its "H" level until timer 1 overflows.

This is because the oscillator needs a set-up period if a ceramic or a quartz crystal oscillator is used.

When the WIT instruction is executed, the clock ϕ stops in the "H" level but the oscillator continues running. This wait state is cleared when an interrupt is accepted Since the oscillation does not stop, the next instructions are executed at once.

To return from the stop or the wait status, the interrupt enable bit must be set to "1" before executing STP or WIT instruction. Especially, to return from the stop status, the timer 1 count enable bit must be set to "1" and the timer 1 interrupt enable bit must be set to "0" before executing STP instruction.

With the M37450, the MISRG2 bit 6 shown in Figure 22 can be used to double the bus cycle. However, the timer, UART, and PWM operations are unafffected. This facilitates accessing of slow peripheral LSIs when external memory and I/O are extended in memory expanding mode or microprocessor mode Note that this bit also affects the bus cycle in single-chip mode.

The circuit example using a ceramic oscillator (or a quartz crystal oscillator) is shown in Figure 35.

The constant capacitance will differ depending on which oscillator is used, and should be set to the manufactures suggested value.

The example of external clock usage is shown in Figure 36. X_{IN} is the input, and X_{OUT} is open.

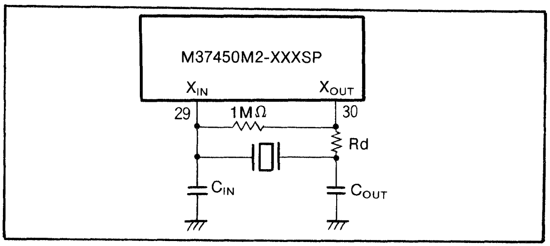


Fig. 35 External ceramic resonator circuit

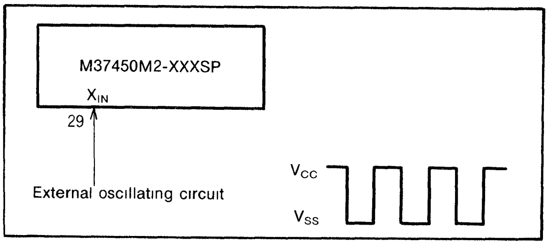


Fig. 36 External clock input circuit

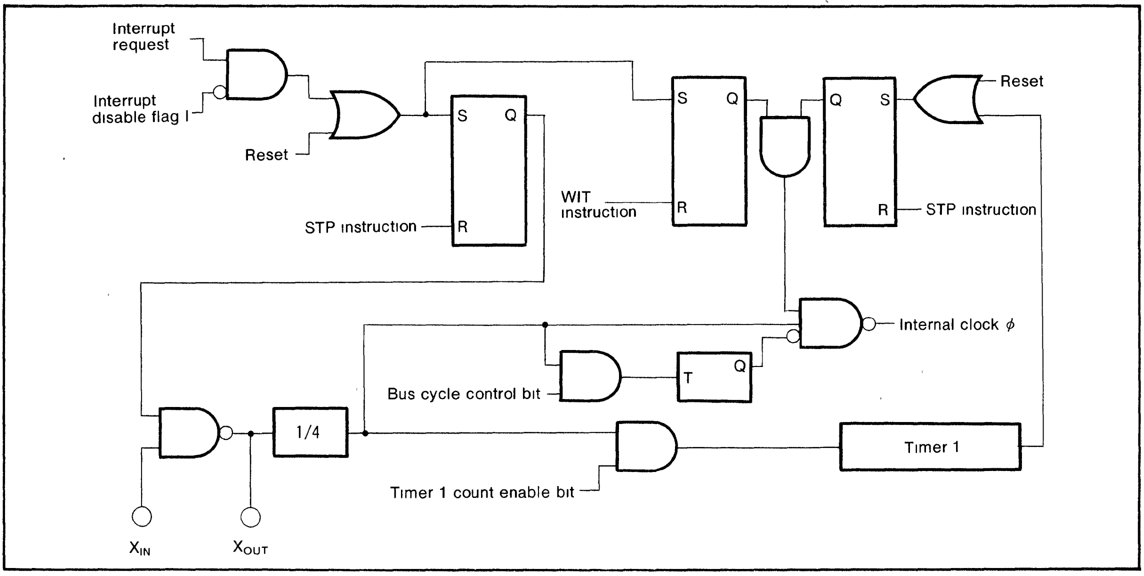


Fig. 37 Block diagram of clock generating circuit

PROGRAMMING NOTES

(1) Processor status register

1. Except for the interrupt inhibit flag (I) being set to "1", the content of the processor status register (PS) is unpredictable after a reset. Therefore, flags affecting program execution must be initialized.
   The T flag and D flag which affect arithmetic operations, must always be initialized.
2. A NOP instruction must be used after the execution of a PLP instruction.

(2) Interrupts

Even though the BBC and BBS instructions are executed just after the interrupt request bits are modified (by the program), those instructions are only valid for the contents before the modification. Also, at least one instruction cycle must be used (such as a NOP) between the modification of the interrupt request bits and the execution of the BBC and BBS instructions.

(3) Decimal operations

1. Decimal operations are performed by setting the decimal mode flag (D) and executing the ADC or SBC instruction. In this case, there must be at least one instruction following the ADC or SBC instruction before executing the SEC, CLC, or CLD instruction.
2. The N (Negative), V(Overflow), and Z(Zero) flags are ignored during decimal mode.

(4) Timers

1. The frequency dividing ratio when n (0 to 65535) is written in the timer latch is 1/(n+1).
2. When directly writing a value in the timer, set the count enable bit to count disable (0) and write in the low-order byte first and then in the high-order byte.
3. The timer value must be read from the high-order byte first.

(5) Serial I/O

In clock synchronous serial I/O mode, if the receiver is to output an $\overline{S_{RDY}}$ using an external clock, the receive enable bit, $\overline{S_{RDY}}$ output enable bit, and transmission enable bit must be set to "1".

(6) A-D conversion

The comparator consists of coupling capacitors that lose their charge when the clock frequency is low. Therefore,f(X_{IN})must be no less than 1MHz during A-D conversion. (If the bus cycle control bit is "1", the bus cycle is doubled and the A-D conversion time is also doubled, therefore, f (X_{IN}) must not be less than 2MHz.) Also, the STP and WIT instructions must not be executed during A-D conversion.

(7) STP instruciton

The STP instruction must be executed after setting the timer 1 count enable bit (bit 4 at address 00DE$_{16}$) to enable ("1").

(8) Multiply/Divide instructions

1. The MUL and DIV instructions are not affected by the T and D flags.
2. The contents of the processor status register are unaffected by multiply or divide instructions.

DATA REQUIRED FOR MASK ORDERING

Please send the following data for mask orders.

- mask ROM order confirmation form
- mark specification form
- ROM data······EPROM 3 sets

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS} Output transistors are at "off" state	−0.3 to 7	V
V_I	Input voltage X_{IN}, $\overline{RESET}$		−0.3 to 7	V
V_I	Input voltage $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, ADV_{REF}, DAV_{REF}, V_{REF}, AV_{CC}		−0.3 to V_{CC}+0.3	V
V_I	Input voltage CNV_{SS}		−0.3 to 13	V
V_O	Output voltage $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, X_{OUT}, ϕ $R/\overline{W}$, $\overline{RD}$, $\overline{WR}$, SYNC, $RESET_{OUT}$		−0.3 to V_{CC}+0.3	V
Pd	Power dissipation	T_a = 25℃	1000(Note 1)	mW
Topr	Operating temperature		−10 to 70	℃
Tstg	Storage temperature		−40 to 125	℃

Note 1 : 500mW in case of the flat package

RECOMMENDED OPERATING CONDITIONS

(V_{CC}=5V±10%, Ta=−10 to 70℃ unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage		0		V
V_{IH}	"H" input voltage $\overline{RESET}$, X_{IN}, CNV_{SS} (Note 1)	0.8V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$ (expect Note 1)	2.0		V_{CC}	V
V_{IL}	"L" input voltage CNV_{SS} (Note 1)	0		0.2V_{CC}	V
V_{IL}	"L" input voltage $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$ (expect Note 1)	0		0.8	V
V_{IL}	"L" input voltage $\overline{RESET}$	0		0.12V_{CC}	V
V_{IL}	"L" input voltage X_{IN}	0		0.16V_{CC}	V
I_{OL}(peak)	"L" peak output current $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$			10	mA
I_{OL}(avg)	"L" average output current $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$ (Note 2)			5	mA
I_{OH}(peak)	"H" peak output current $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$			−10	mA
I_{OH}(avg)	"H" average output current $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$ (Note 2)			−5	mA
f(X_{IN})	Internal clock oscillating frequency	1		10	MHz

Note 1 : Ports operating as special function pins INT_1-INT_3($P6_0$-$P6_2$), EV_1-EV_3($P3_0$-$P3_2$), R_XD($P3_4$), S_{CLK}($P3_6$)

2 : I_{OL}(avg) and I_{OH}(avg) are the average current in 100ms

3 : The total of I_{OL} of Port P0, P1 and P2 should be 40mA (max.)
The total of I_{OL} of Port P3, P5, P6, $R/\overline{W}$ SYNC, $RESET_{OUT}$, $\overline{RD}$, $\overline{WR}$ and ϕ should be 40mA (max)
The total of I_{OH} of Port P0, P1, and P2 should be 40mA (max)
The total of I_{OH} of Port P3, P5, P6, $R/\overline{W}$, SYNC, $RESET_{OUT}$, $\overline{RD}$, $\overline{WR}$, and ϕ should be 40mA (max).

ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10%, V_{SS}= 0 V, T_a=−10 to 70℃, f(X_{IN})=10MHz)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{OH}	"H" output voltage $\overline{RD}$, $\overline{WR}$, R/$\overline{W}$, SYNC, $RESET_{OUT}$, ϕ	I_{OH} =− 2 mA	V_{CC}−1			V
V_{OH}	"H" output voltage $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$	I_{OH} =− 5 mA	V_{CC}−1			V
V_{OL}	"L" output voltage $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $\overline{RD}$, $\overline{WR}$, R/$\overline{W}$, SYNC, $RESET_{OUT}$, ϕ	I_{OL} =2 mA			0. 45	V
V_{OL}	"L" output voltage $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$ ·	I_{OL} =5 mA			1	V
$V_{T+} - V_{T-}$	Hysteresis INT_1-INT_3($P6_0$-$P3_2$), EV_1-EV_3($P3_0$-$P3_2$), R_XD($P3_4$), S_{CLK}($P3_6$)	Function input level	0. 3		1	V
$V_{T+} - V_{T-}$	Hysteresis $\overline{RESET}$				0. 7	V
$V_{T+} - V_{T-}$	Hysteresis X_{IN}		0. 1		0. 5	V
I_{IL}	"L" input current $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $\overline{RESET}$, X_{IN}	V_I =V_{SS}	−5		5	μA
I_{IH}	"H" input current $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $\overline{RESET}$, X_{IN}	V_I =V_{CC}	−5		5	μA
V_{RAM}	RAM retention voltage	At stop mode	2			V
I_{CC}	Supply current	f(X_{IN})=10MHz At system operation		6	10	mA
		At stop mode (Note 1)		1	10	μA

Note 1 : The terminals $\overline{RD}$, $\overline{WR}$, SYNC, R/$\overline{W}$, $RESET_{OUT}$, ϕ, D-A_1 and D-A_2 are all open The other ports, which are in the input mode, are connected to V_{SS} A-D converter is in the A-D completion state The current through ADV_{REF} and DAV_{REF} is not included. (Fig 41)

A-D CONVERTER CHARACTERISTICS

(V_{CC}=AV_{CC}= 5 V, V_{SS}=AV_{SS}= 0 V, T_a =25℃, f(X_{IN})=10MHz unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
—	Resolution				8	Bits
—	Absolute accuracy	V_{CC}=AV_{CC}=ADV_{REF}=5. 12V		±1. 5	±3	LSB
t_{CONV}	Conversion time				49	$t_{c(\phi)}$
V_{IA}	Analog input voltage		AV_{SS}		AV_{CC}	V
V_{ADVREF}	Reference input voltage		2		V_{CC}	V
R_{LADDER}	Ladder resistance value	ADV_{REF}= 5 V	2	7. 5	10	kΩ
$I_{IADVREF}$	Reference input current	ADV_{REF}= 5 V	0. 5	0. 7	2. 5	mA
V_{AVCC}	Analog power supply input voltage			V_{CC}		V
V_{AVSS}	Analog power supply input voltage			0		V

D-A CONVERTER CHARACTERISTICS (V_{CC}= 5 V, V_{SS}=AV_{SS}= 0 V, T_a =25℃ unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
—	Resolution				8	Bits
—	Full scale deviation	V_{CC}=DAV_{REF}=5V			1. 0	%
t_{SU}	Set time				3	μs
R_O	Output resistance		1	2	4	kΩ
V_{AVSS}	Analog power supply input voltage			0		V
V_{DAVREF}	Reference input voltage		4		V_{CC}	V
I_{DAVREF}	Reference power input current (Each pin)		0	2. 5	5	mA

TIMING REQUIREMENTS

Port/single-chip mode (V_{CC}=5V±10%, V_{SS}=0V, T_a=−10 to 70℃, unless otherwise noted)

Symbol	Parameter	Test condition	Limits			Unit
			Min.	Typ	Max	
$t_{su(P0D-\phi)}$	Port P0 input setup time	Fig 38	200			ns
$t_{su(P1D-\phi)}$	Port P1 input setup time		200			ns
$t_{su(P2D-\phi)}$	Port P2 input setup time		200			ns
$t_{su(P3D-\phi)}$	Port P3 input setup time		200			ns
$t_{su(P4D-\phi)}$	Port P4 input setup time		200			ns
$t_{su(P5D-\phi)}$	Port P5 input setup time		200			ns
$t_{su(P6D-\phi)}$	Port P6 input setup time		200			ns
$t_{h(\phi-P0D)}$	Port P0 input hold time		40			ns
$t_{h(\phi-P1D)}$	Port P1 input hold time		40			ns
$t_{h(\phi-P2D)}$	Port P2 input hold time		40			ns
$t_{h(\phi-P3D)}$	Port P3 input hold time		40			ns
$t_{h(\phi-P4D)}$	Port P4 input hold time		40			ns
$t_{h(\phi-P5D)}$	Port P5 input hold time		40			ns
$t_{h(\phi-P6D)}$	Port P6 input hold time		40			ns
$t_c(X_{IN})$	External clock input cycle time		100		1000	ns
$t_w(X_{IN}L)$	External clock input "L" pulse width		30			ns
$t_w(X_{IN}H)$	External clock input "H" pulse width		30			ns
$t_r(X_{IN})$	External clock rising edge time				20	ns
$t_f(X_{IN})$	External clock falling edge time				20	ns

Master CPU bus interface timing ($\overline{R}$ and $\overline{W}$ separation type mode)

(V_{CC}=5V±10%, V_{SS}=0V, T_a=−10 to 70℃, unless otherwise noted)

Symbol	Parameter	Test condition	Limits			Unit
			Min	Typ	Max	
$t_{su(CS-R)}$	$\overline{CS}$ setup time	Fig 39	0			ns
$t_{su(CS-W)}$	$\overline{CS}$ setup time		0			ns
$t_{h(R-CS)}$	$\overline{CS}$ hold time		0			ns
$t_{h(W-CS)}$	$\overline{CS}$ hold time		0			ns
$t_{su(A-R)}$	A0 setup time		40			ns
$t_{su(A-W)}$	A0 setup time		40			ns
$t_{h(R-A)}$	A0 hold time		10			ns
$t_{h(W-A)}$	A0 hold time		10			ns
$t_{w(R)}$	Read pulse width		160			ns
$t_{w(W)}$	Write pulse width		160			ns
$t_{su(D-W)}$	Date input setup time before write		100			ns
$t_{h(W-D)}$	Date input hold time after write		10			ns

Master CPU bus interface timing (R/$\overline{W}$ type mode)

(V_{CC}=5V±10%, V_{SS}=0V, T_a=−10 to 70℃, unless otherwise noted)

Symbol	Parameter	Test condition	Limits			Unit
			Min	Typ.	Max.	
$t_{su(CS-E)}$	$\overline{CS}$ setup time	Fig 39	0			ns
$t_{h(E-CS)}$	$\overline{CS}$ hold time		0			ns
$t_{su(A-E)}$	A0 setup time		40			ns
$t_{h(E-A)}$	A0 hold time		10			ns
$t_{su(RW-E)}$	R/$\overline{W}$ setup time		40			ns
$t_{h(E-RW)}$	R/$\overline{W}$ hold time		10			ns
$t_{w(EL)}$	Enable clock "L" pulse width		160			ns
$t_{w(EH)}$	Enable clock "H" pulse width		160			ns
$t_{r(E)}$	Enable clock rising edge time				25	ns
$t_{f(E)}$	Enable clock falling edge time				25	ns
$t_{su(D-E)}$	Data input setup time before write		100			ns
$t_{h(E-D)}$	Data input hold time after write		10			ns

Local bus/memory expansion mode, microprocessor mode

(V_{CC}=5V±10%, V_{SS}=0V, T_a=−10 to 70℃, unless otherwise noted)

Symbol	Parameter	Test condition	Limits			Unit
			Min	Typ	Max	
$t_{su(D-\phi)}$	Data input setup time	Fig 40	130			ns
$t_{h(\phi-D)}$	Data input hold time		0			ns
$t_{su(D-RD)}$	Data input setup time		130			ns
$t_{h(RD-D)}$	Data input hold time		0			ns

SWITCHING CHARACTERISTICS

Port/single-chip mode (V_{CC}=5V±10%, V_{SS}=0V, T_a=−10 to 70℃, unless otherwise noted)

Symbol	Parameter	Test condition	Limits			Unit
			Min.	Typ	Max	
$t_{d(\phi-P0Q)}$	Port P0 data output delay time	Fig 38			200	ns
$t_{d(\phi-P1Q)}$	Port P1 data output delay time				200	ns
$t_{d(\phi-P2Q)}$	Port P2 data output delay time				200	ns
$t_{d(\phi-P3Q)}$	Port P3 data output delay time				200	ns
$t_{d(\phi-P5Q)}$	Port P5 data output delay time				200	ns
$t_{d(\phi-P6Q)}$	Port P6 data output delay time				200	ns
$t_{C(\phi)}$	Cycle time		400		4000	ns
$t_{W(\phi H)}$	ϕ clock pulse width ("H" level)		190			ns
$t_{W(\phi L)}$	ϕ clock pulse width ("L" level)		170			ns
$t_{r(\phi)}$	ϕ clock rising edge time				20	ns
$t_{f(\phi)}$	ϕ clock falling edge time				20	ns

Master CPU bus interface ($\overline{R}$ and $\overline{W}$ separation type mode)

(V_{CC}=5V±10%, V_{SS}=0V, T_a=−10 to 70℃, unless otherwise noted)

Symbol	Parameter	Test condition	Limits			Unit
			Min	Typ	Max	
$t_{a(R-D)}$	Data output enable time after read	Fig 39			120	ns
$t_{v(R-D)}$	Data output disable time after read		10		85	ns
$t_{PLH(R-PR)}$	$\overline{P_{RDY}}$ output transmission time after read				150	ns
$t_{PLH(W-PR)}$	$\overline{P_{RDY}}$ output transmission time after write				150	ns

Master CPU bus interface (R/$\overline{W}$ type mode) (V_{CC}=5V±10%, V_{SS}=0V, T_a=−10 to 70℃, unless otherwise noted)

Symbol	Parameter	Test condition	Limits			Unit
			Min	Typ	Max	
$t_{a(E-D)}$	Data output enable time after read	Fig 39			120	ns
$t_{v(E-D)}$	Data output disable time after read		10		85	ns
$t_{PLH(E-PR)}$	$\overline{P_{RDY}}$ output transmission time after E clock				150	ns

Local bus/memory expansion mode, microprocessor mode

(V_{CC}=5V±10%, V_{SS}=0V, T_a=−10 to 70℃, unless otherwise noted)

Symbol	Parameter	Test condition	Limits			Unit
			Min.	Typ.	Max	
$t_{d(\phi-A)}$	Address delay time after ϕ	Fig 40			150	ns
$t_{v(\phi-A)}$	Address effective time after ϕ		10			ns
$t_{v(RD-A)}$	Address effective time after $\overline{RD}$		10			ns
$t_{v(WR-A)}$	Address effective time after $\overline{WR}$		10			ns
$t_{d(\phi-D)}$	Data output delay time after ϕ				160	ns
$t_{d(WR-D)}$	Data output delay time after $\overline{WR}$				160	ns
$t_{v(\phi-D)}$	Data output effective time after ϕ		20			ns
$t_{v(WR-D)}$	Data output effective time after $\overline{WR}$		20			ns
$t_{d(\phi-RW)}$	R/$\overline{W}$ delay time after ϕ				150	ns
$t_{d(\phi-SYNC)}$	SYNC delay time after ϕ				150	ns
$t_{W(RD)}$	$\overline{RD}$ pulse width		170			ns
$t_{W(WR)}$	$\overline{WR}$ pulse width		170			ns

TEST CONDITION

Input voltage level : V_{IH} 2.4V
V_{IL} 0.45V
Output test level : V_{OH} 2.0V
V_{OL} 0.8V

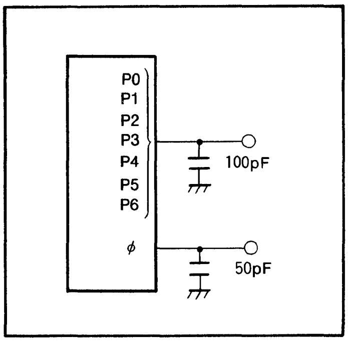


Fig. 38 Test circuit in single-chip mode

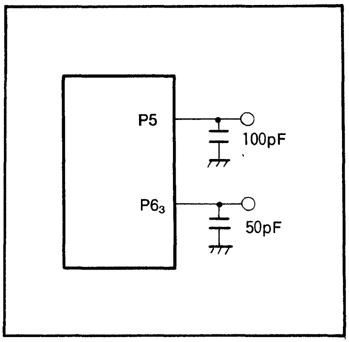


Fig. 39 Master CPU bus interface test circuit

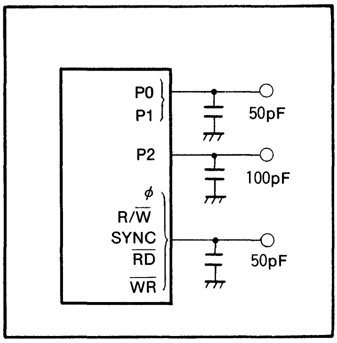


Fig. 40 Local bus test circuit

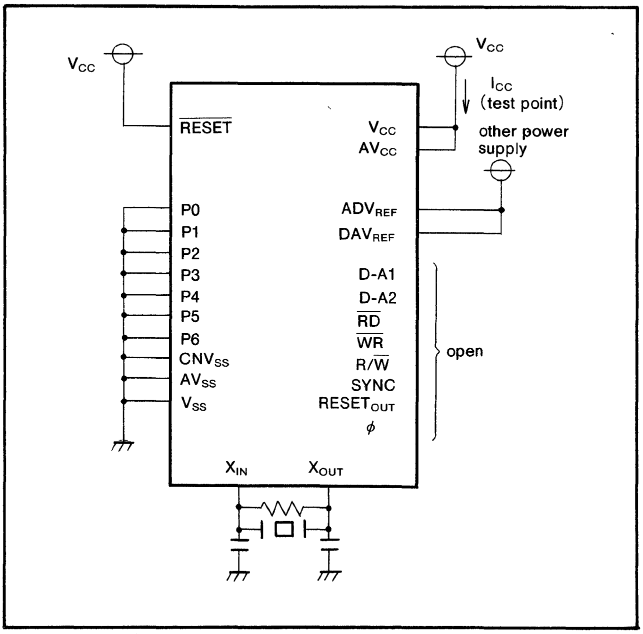
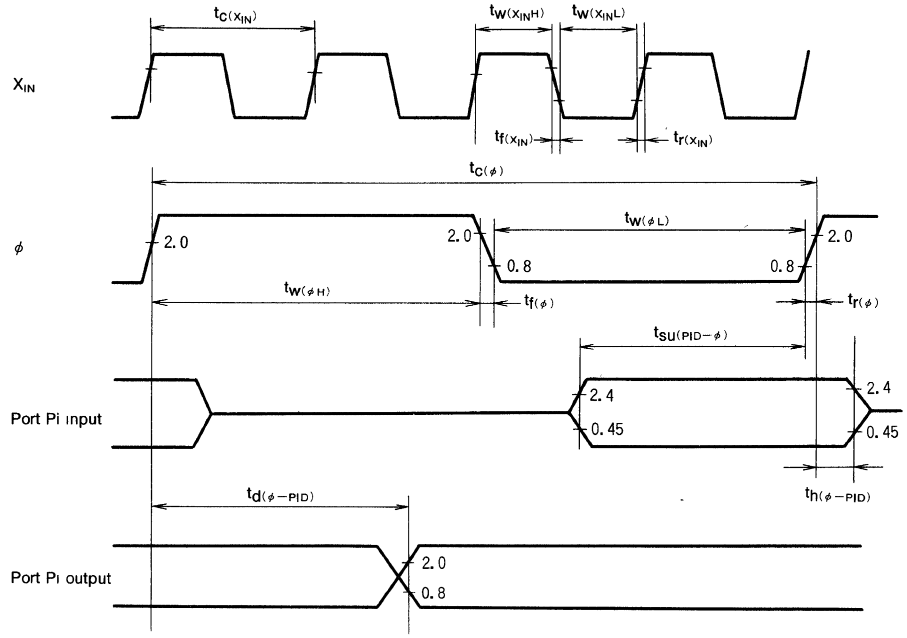


Fig. 41 I_{CC} (at stop mode) test condition

TIMING DIAGRAM

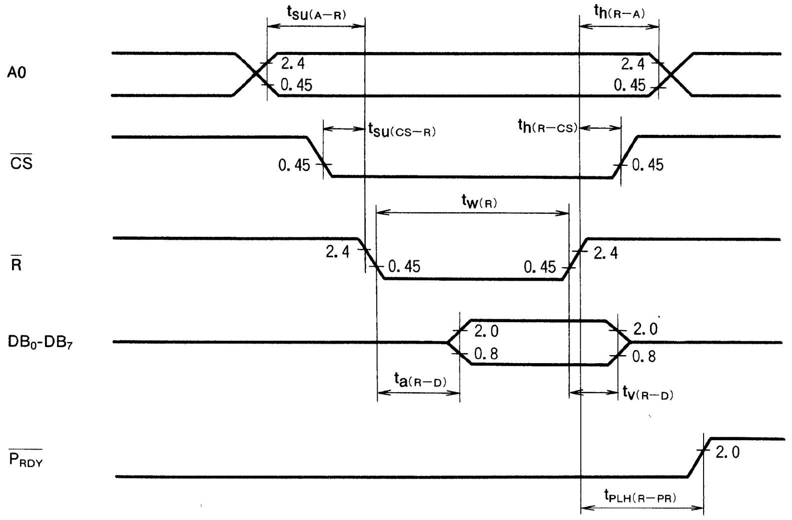
Port/single-chip mode timing diagram



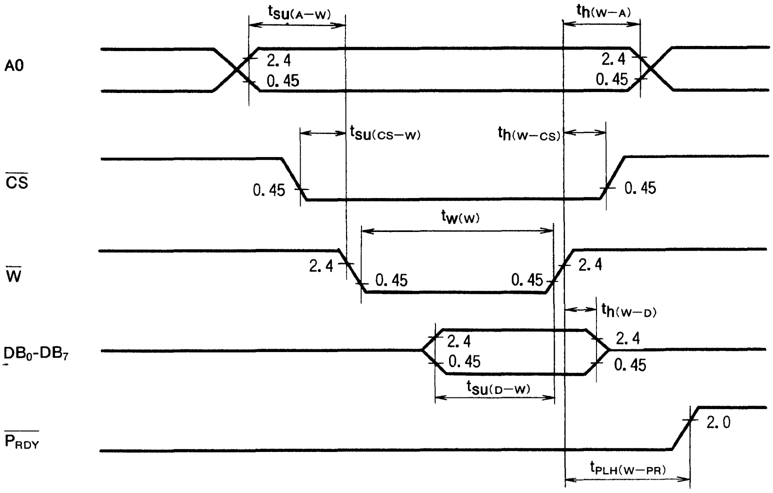
Note : V_{IH}=0.8V_{CC}, V_{IL}=0.16V_{CC} of X_{IN}

Master CPU bus interface/ $\overline{R}$ and $\overline{W}$ separation type timing diagram

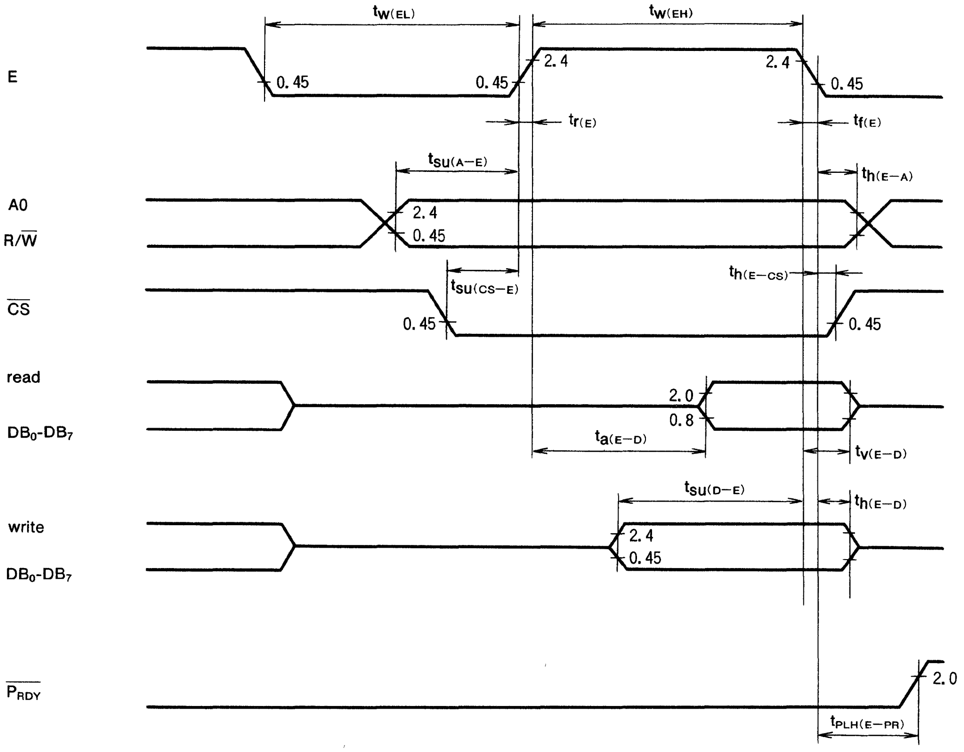
Read



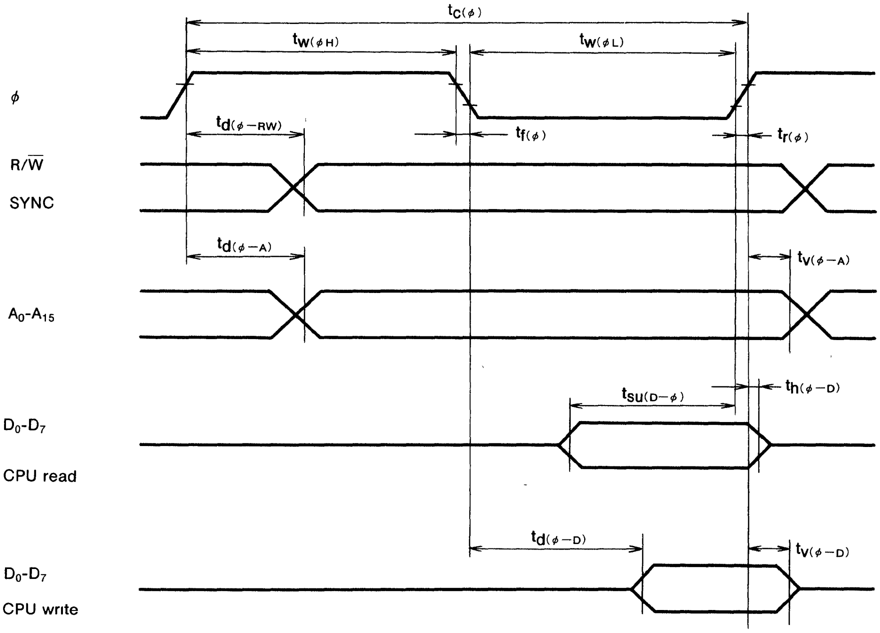
Write

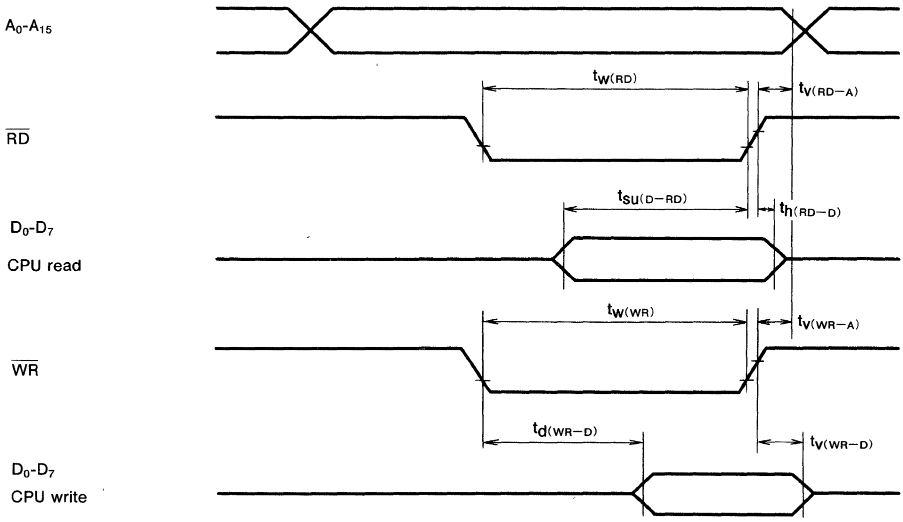


Master CPU interface/ R/W type timing diagram



Local bus timing diagram





M37450S1SP/FP,M37450S2SP/FP
M37450S4SP/FP

8-BIT CMOS MICROCOMPUTER

DESCRIPTION

The M37450S1SP/FP is a single-chip microcomputer designed with CMOS silicon gate technology. It is housed in a 64-pin shrink plastic molded DIP or an 80-pin plastic molded QFP. In addition to its simple instruction sets, the ROM, RAM and I/O addresses are placed on the same memory map to enable easy programming. It is suited for office automation equipment and control devices. The low power consumption made possible by the use of a CMOS process makes it especially suitable for battery powered devices requiring low power consumption. It also has a unique feature that enables it to be used as a slave microcomputer.

M37450S1SP/FP, M37450S2SP/FP and M37450S4SP/FP have basically the same functions as M37450M2-XXXSP/FP except the RAM size and the fact that these three need external ROM area. The differences among M37450S1SP/FP, M37450S2SP/FP and M37450S4SP/FP are as shown below.

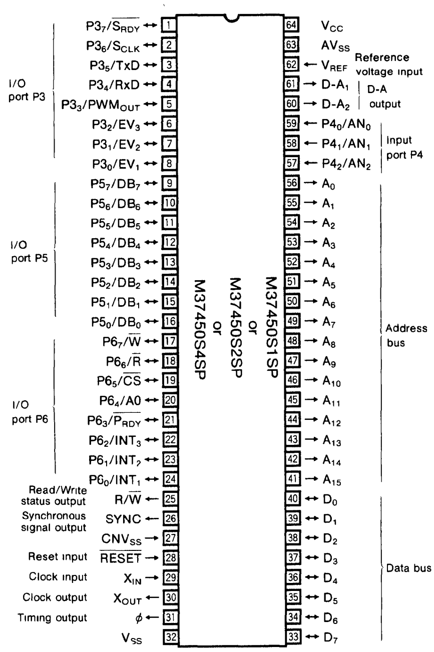
Type	RAM size
M37450S1SP/FP	128 bytes
M37450S2SP/FP	256 bytes
M37450S4SP/FP	448 bytes

Also M37450S1SP has the same function as M37450M2-XXXSP/FP in microprocessor mode and M37450S2SP/FP has the same function as M37450M4-XXXSP/FP in microprocessor mode.

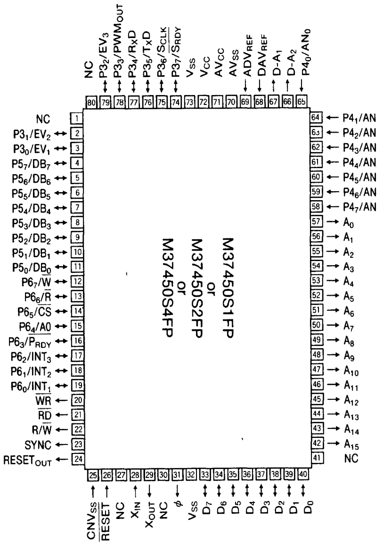
FEATURES

- Number of basic instructions ······························ 71
  69 MELPS 740 basic instructions+2 multiply/divide instructions
- Memory size ROM ······························ None
  RAM········· 128 bytes (M37450S1SP/FP)
  256 bytes (M37450S2SP/FP)
  448 bytes (M37450S4SP/FP)
- Instruction execution time
  (minimum instructions at 10 MHz frequency) ····· 0.8μs
- Single power supply ······························ 5V±10%
- Power dissipation normal operation mode
  (at 10MHz frequency) ······························ 30mW
- Subroutine nesting ···· 64 levels max. (M37450S1SP/FP)
- Interrupt ······························ 15 events
- Master CPU bus interface ······························ 1 byte
- 16-bit timer ······························ 3
- 8-bit timer (Serial I/O use) ······························ 1
- Serial I/O (UART or clock synchronous) ··················· 1
- A-D converter (8bit resolution) ········· 3 channels (DIP)
  8 channels (QFP)
- D-A converter (8-bit resolution) ················ 2 channels
- PWM output (8-bit or 16-bit) ······························ 1
- Programmable I/O
  (Ports P0, P1, P2, P3, P5, P6) ······························ 48
- Input (Port P4) ······························ 3 (DIP), 8 (QFP)
- Output (Port D-A_1, D-A_2) ······························ 2

PIN CONFIGURATION (TOP VIEW)



Outline 64P4B

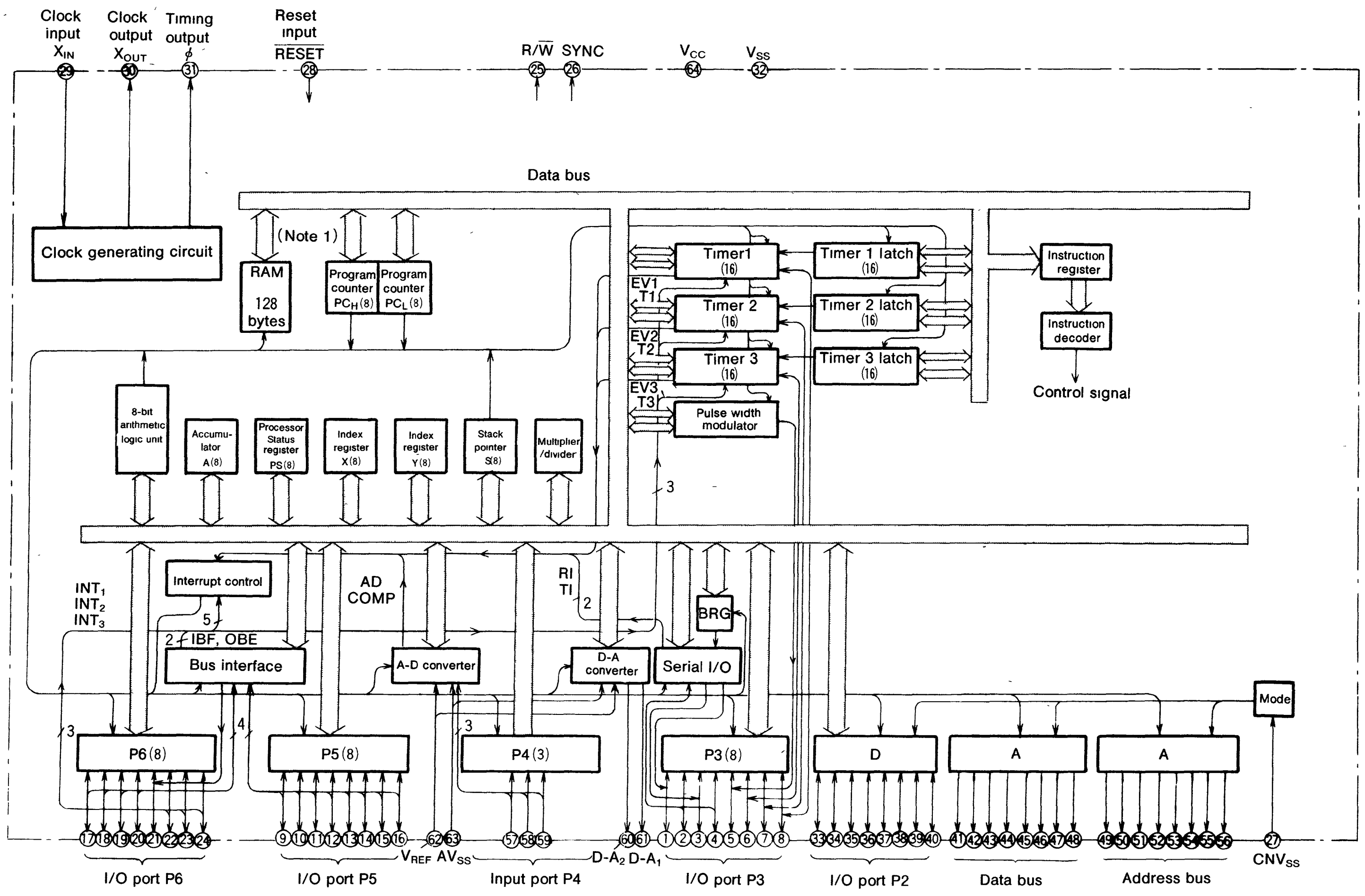


Outline 80P6 NC : No connection

APPICATION

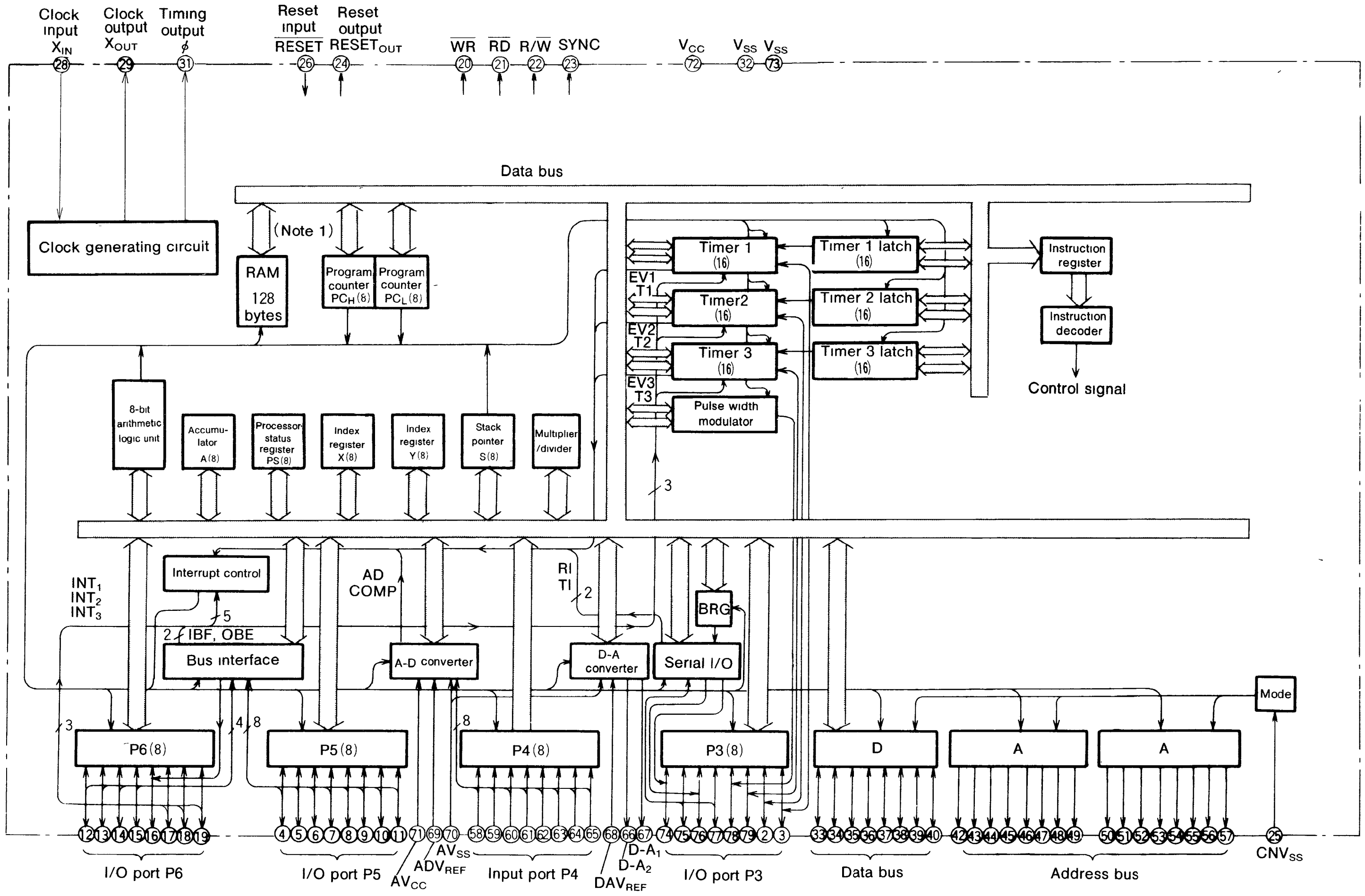
Slave controller for PPCs, facsimiles and page printers
HDD, optical disk, inverter and industrial motor controllers
Industrial robots and machines

M37450S1SP BLOCK DIAGRAM



Note 1 : 256 bytes for M37450S2SP and 448 bytes for M37450S4SP

M37450S1FP BLOCK DIAGRAM



Note 1 : 256 bytes for M37450S2FP and 448 bytes for M37450S4FP

FUNCTIONS OF M37450S1SP/FP, M37450S2SP/FP, M37450S4SP/FP

Parameter			Function
Number of basic instructions			71(69 MELPS 740 basic instructions+2)
Instruction execution time			0. 8μs(minimum instructions, at 10MHz of frequency)
Clock frequency			10MHz(max)
RAM size	M37450S1SP/FP		128 bytes
	M37450S2SP/FP		256 bytes
	M37450S4SP/FP		448 bytes
Input/Output port	P3, P5, P6	I/O	8-bit×3
	P4	Input	3-bit×1(8-bit×1 for 80-pin model)
	D-A	Output	2-bit×1
Serial I/O			UART or clock synchronous
Timers			16-bit timer×3, 8-bit timer(serial I/O baud rate generator)×1
A-D converter			8-bit×3 channels(8 channels for 80-pin model)
D-A converter			8-bit×2 channels
Pulse width modulator			8-bit or 16-bit×1
Data bus buffer			1-byte input and output each
Subroutine nesting			64-levels(max for M37450S1SP/FP)
			96-levels(max for M37450S2SP/FP, M37450S4SP/FP)
Interrupt			6 external interrupts, 8 internal interrupts one software interrupt
Clock generating circuit			Built-in(ceramic or quarts crystal oscillator)
Supply voltage			5V±10%
Power dissipation			30mW(at 10MHz frequency)
Input/Output characters	Input/Output voltage		5V
	Output current		±5mA(max)
Operating temperature range			−10~70℃
Device structure			CMOS silicon gate
Package	M37450S1SP, M37450S2SP, M37450S4SP		64-pin shrink plastic molded DIP
	M37450S1FP, M37450S2FP, M37450S4FP		80-pin plastic molded QFP

PIN DESCRIPTION

Pin	Name	Input/ Output	Functions
V_{CC}, V_{SS}	Supply voltage		Power supply inputs 5V±10% to V_{CC}, and 0V to V_{SS}
CNV_{SS}	CNV_{SS}	Input	This is connected to V_{CC}
$\overline{RESET}$	Reset input	Input	To enter the reset state, the reset input pin must be kept at a "L" for more than 8 clock cycles(under normal V_{CC} conditions) If more time is needed for the crystal oscillator to stabilize, this "L" condition should be maintained for the required time
X_{IN}	Clock input	Input	This chip has an internal clock generating circuit To control generating frequency, an external ceramic or a quartz crystal oscillator is connected between the X_{IN} and X_{OUT} pins If an external clock is used, the clock source should be connected to the X_{IN} pin and the X_{OUT} pin should be left open
X_{OUT}	Clock output	Output	
ϕ	Timing output	Output	Outputs signal consisting of oscillating frequency divided by four
SYNC	Synchronous signal output	Output	This signal is output "H" during operation code fetch and is used to control single stepping of programs
$R/\overline{W}$	Read/Write status output	Output	This signal determines the direction of the data bus It is "H" during read and "L" during write
A_0~A_{15}	Address bus	Output	This is 16-bit address bus
D_0~D_7	Data bus	I/O	This is 8-bit data bus
$P3_0$~$P3_7$	Input/Output port P3	I/O	Port P3 is an 8-bit I/O port with directional registers allowing each I/O bit to be individually programed as input or output The output structure is CMOS output Serial I/O, PWM output, or even I/O function can be selected with a program
$P4_0$~$P4_2$ ($P4_0$~$P4_7$)	Input port P4	Input	Analog input pin for the A-D converter The 64-pin model has three pins and the 80-pin model has eight pins They may also be used as digital input pins
$P5_0$~$P5_7$	Input/Output port P5	I/O	An 8-bit input/output port with the same function as P3 This port functions as an 8-bit data bus for the master CPU when slave mode is selected with a program.
$P6_0$~$P6_7$	Input/Output port P6	I/O	An 8-bit input/output port with the same function as P3 Pins $P6_3$~$P6_7$ change to a control bus for the master CPU when slave mode is selected with a program Pins $P6_0$~$P6_2$ may be programmed as external interrupt input pins
D-A_1, D-A_2	D-A output	Output	Analog signal from D-A converter is output
V_{REF}	Reference voltage input	Input	Reference voltage input pin for A-D and D-A converter This pin is for 64-pin model only
ADV_{REF}	A-D reference voltage input	Input	Reference voltage input pin for A-D converter This pin is for 80-pin model only
DAV_{REF}	D-A reference voltage input	Input	Reference voltage input pin for D-A converter This pin is for 80-pin model only
AV_{SS}	Analog power supply		Ground level input pin for A-D and D-A converter Same voltage as V_{SS} is applied
AV_{CC}	Analog power supply		Power supply input pin for A-D converter This pin is for 80-pin model only Same voltage as $V_{CC}$is applied In the case of the 64-pin model AV_{CC} is connected to V_{CC} internally
$\overline{RD}$	Read signal output	Output	Control signal output as active "L" when valid data is read from data bus This pin is for 80-pin model only
$\overline{WR}$	Write signal output	Output	Control signal output as active "L" when writing data from data bus to external component This pin is for 80-pin model only
$RESET_{OUT}$	Reset output	Output	Control signal output as active "H" during reset It is used as a reset output signal for peripheral components This pin is for 80-pin model only

BASIC FUNCTION BLOCKS

The differences between M37450M2-XXXSP/FP and M37450S1SP/FP are noted below. Other functions are the same as M37450M2-XXXSP/FP in microprocessor mode.

MEMORY

- **Special Function Register (SFR) Area**

The special function register (SFR) area contains the registers relating to functions such as I/O ports and timers.

- **RAM**

RAM is used for data storage as well as a stack area.

- **Interrupt Vector Area**

The interrupt vector area is for storing jump destination addresses used at reset or when an interrupt is generated. This area must be located in ROM area.

- **Zero Page**

Zero page addressing mode is useful because it enables access to this area with only 2 bytes.

- **Special Page**

Special page addressing mode is useful because it enables access to this area with only 2 bytes

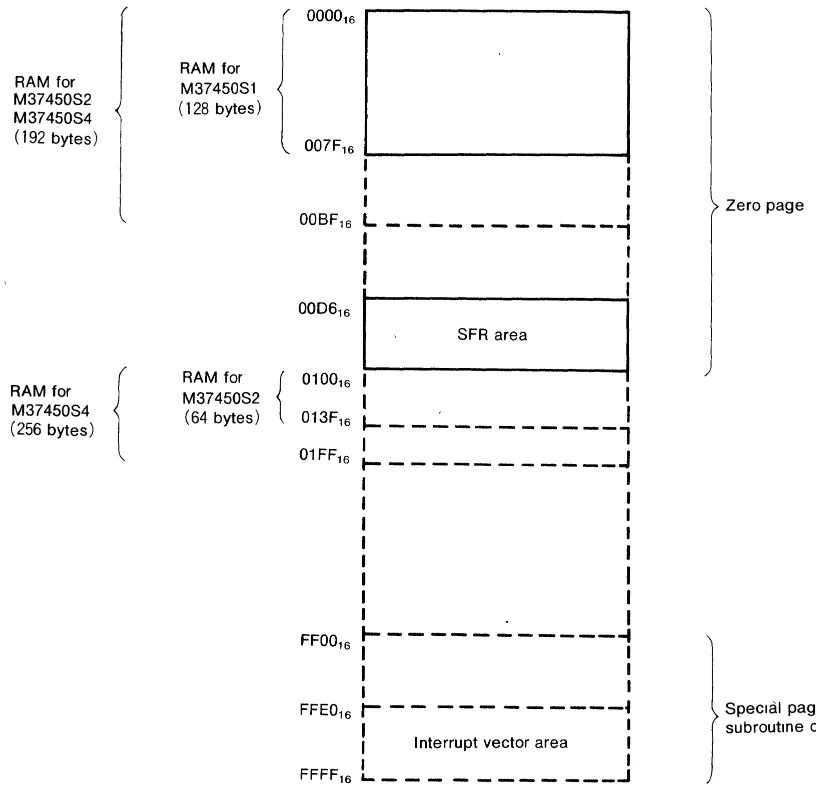


Fig. 1 Memory map

$00D6_{16}$	P3 register
$00D7_{16}$	P3 directional register
$00D8_{16}$	P4 register
$00D9_{16}$	Reserved
$00DA_{16}$	P5 register
$00DB_{16}$	P5 directional register
$00DC_{16}$	P6 register
$00DD_{16}$	P6 directional register
$00DE_{16}$	MISRG1
$00DF_{16}$	MISRG2
$00E0_{16}$	D-A1 register
$00E1_{16}$	D-A2 register
$00E2_{16}$	A-D register
$00E3_{16}$	A-D control register
$00E4_{16}$	Data bus buffer register
$00E5_{16}$	Data bus buffer status register
$00E6_{16}$	Receive/transmit buffer register
$00E7_{16}$	Serial I/O status register
$00E8_{16}$	Serial I/O control register
$00E9_{16}$	UART control register
$00EA_{16}$	Baud rate generator
$00EB_{16}$	PWM register (low-order)
$00EC_{16}$	PWM register (high-order)
$00ED_{16}$	Timer 1 control register
$00EE_{16}$	Timer 2 control register
$00EF_{16}$	Timer 3 control register
$00F0_{16}$	Timer 1 register (low-order)
$00F1_{16}$	Timer 1 register (high-order)
$00F2_{16}$	Timer 1 latch (low-order)
$00F3_{16}$	Timer 1 latch (high-order)
$00F4_{16}$	Timer 2 register (low-order)
$00F5_{16}$	Timer 2 register (high-order)
$00F6_{16}$	Timer 2 latch (low-order)
$00F7_{16}$	Timer 2 latch (high-order)
$00F8_{16}$	Timer 3 register (low-order)
$00F9_{16}$	Timer 3 register (high-order)
$00FA_{16}$	Timer 3 latch (low-order)
$00FB_{16}$	Timer 3 latch (high-order)
$00FC_{16}$	Interrupt request register 1
$00FD_{16}$	Interrupt request register 2
$00FE_{16}$	Interrupt control register 1
$00FF_{16}$	Interrupt control register 2

Fig. 2 SFR (Special Function Register) memory map

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS} Output transistors are at "OFF" state	−0.3∼7	V
V_I	Input voltage $\overline{RESET}$, X_{IN}		−0.3∼7	V
V_I	Input voltage D_0∼D_7, $P3_0$∼$P3_7$, $P4_0$∼$P4_7$, $P5_0$∼$P5_7$, $P6_0$∼$P6_7$, ADV_{REF}, DAV_{REF}, V_{REF}, AV_{CC}		−0.3∼V_{CC}+0.3	V
V_I	Input voltage CNV_{SS}		−0.3∼13	V
V_O	Output voltage A_0∼A_{15}, D_0∼D_7, $P3_0$∼$P3_7$, $P5_0$∼$P5_7$, $P6_0$∼$P6_7$, X_{OUT}, ϕ, $\overline{RD}$, $\overline{WR}$, R/$\overline{W}$, $RESET_{OUT}$, SYNC		−0.3∼V_{CC}+0.3	V
Pd	Power dissipation	T_a = 25℃	1000 (Note 1)	mW
Topr	Operating temperature		−10∼70	℃
Tstg	Storage temperature		−40∼125	℃

Note 1 : 500mW for QFP type

RECOMMENDED OPERATING CONDITIONS

(V_{CC}=5V±10%, Ta=−10∼70℃ unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage		0		V
V_{IH}	"H" Input voltage $\overline{RESET}$, X_{IN}, CNV_{SS} (Note 1)	0.8V_{CC}		V_{CC}	V
V_{IH}	"H" Input voltage D_0∼D_7, $P3_0$∼$P3_7$, $P4_0$∼$P4_7$, $P5_0$∼$P5_7$, $P6_0$∼$P6_7$ (except Note 1)	2.0		V_{CC}	V
V_{IL}	"L" Input voltage CNV_{SS} (Note 1)	0		0.2V_{CC}	V
V_{IL}	"L" Input voltage D_0∼D_7, $P3_0$∼$P3_7$, $P4_0$∼$P4_7$, $P5_0$∼$P5_7$, $P6_0$∼$P6_7$ (except Note 1)	0		0.8	V
V_{IL}	"L" Input voltage $\overline{RESET}$	0		0.12V_{CC}	V
V_{IL}	"L" Input voltage X_{IN}	0		0.16V_{CC}	V
$I_{OL(peak)}$	"L" peak output current A_0∼A_{15}, D_0∼D_7, $P3_0$∼$P3_7$, $P5_0$∼$P5_7$, $P6_0$∼$P6_7$			10	mA
$I_{OL(avg)}$	"L" average output current A_0∼A_{15}, D_0∼D_7, $P3_0$∼$P3_7$, $P5_0$∼$P5_7$, $P6_0$∼$P6_7$ (Note 2)			5	mA
$I_{OH(peak)}$	"H" peak output current A_0∼A_{15}, D_0∼D_7, $P3_0$∼$P3_7$, $P5_0$∼$P5_7$, $P6_0$∼$P6_7$			−10	mA
$I_{OH(avg)}$	"H" average output current A_0∼A_{15}, D_0∼D_7, $P3_0$∼$P3_7$, $P5_0$∼$P5_7$, $P6_0$∼$P6_7$ (Note 2)			−5	mA
$f(X_{IN})$	Clock oscillating frequency	1		10	MHz

Note 1 : Ports operate as INT_1∼INT_3($P6_0$∼$P6_2$), EV_1∼EV_3($P3_0$∼$P3_2$), R_xD($P3_4$) and S_{CLK}($P3_6$)

2 : The average output current $I_{OH(avg)}$ and $I_{OL(avg)}$ are the average value during a 100ms

3 : The total of "L" output current $I_{OL(peak)}$ of port P3, P5, P6, R/$\overline{W}$, SYNC, $RESET_{OUT}$, $\overline{RD}$, $\overline{WR}$ and ϕ is less than 40mA

The total of "H" output current $I_{OH(peak)}$ of port P3, P5, P6, R/$\overline{W}$, SYNC, $RESET_{OUT}$, $\overline{RD}$, $\overline{WR}$ and ϕ is less than 40mA

ELECTRICAL CHARACTERISTICS (V_{CC} = 5V±10%, V_{SS} = 0V, T_a = −10~70℃, f(X_{IN}) = 10MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{OH}	"H" output voltage $\overline{RD}$, $\overline{WR}$, R/$\overline{W}$, SYNC, $RESET_{OUT}$, ϕ	I_{OH}=−2mA	V_{CC}−1			V
V_{OH}	"H" output voltage A_0~A_{15}, D_0~D_7, $P3_0$~$P3_7$, $P5_0$~$P5_7$, $P6_0$~$P6_7$	I_{OH}=−5mA	V_{CC}−1			V
V_{OL}	"L" output voltage A_0~A_{15}, D_0~D_7, $P3_0$~$P3_7$, $P5_0$~$P5_7$, $P6_0$~$P6_7$, $\overline{RD}$, $\overline{WR}$, R/$\overline{W}$, SYNC, $RESET_{OUT}$, ϕ	I_{OL}=2mA			0. 45	V
V_{OL}	"L" output voltage A_0~A_{15}, D_0~D_7, $P3_0$~$P3_7$, $P5_0$~$P5_7$, $P6_0$~$P6_7$	I_{OL}=5mA			1	V
$V_{T+}-V_{T-}$	Hysterisis INT_1~INT_3($P6_0$~$P6_2$), EV_1~EV_3($P3_0$~$P3_2$), R_XD($P3_4$), S_{CLK}($P3_6$)	Function input level	0. 3		1	V
$V_{T+}-V_{T-}$	Hysterisis $\overline{RESET}$				0. 7	V
$V_{T+}-V_{T-}$	Hysterisis X_{IN}		0. 1		0. 5	V
I_{IL}	"L" input current D_0~D_7, $P3_0$~$P3_7$, $P4_0$~$P4_7$, $P5_0$~$P5_7$, $P6_0$~$P6_7$, $\overline{RESET}$, X_{IN}	V_I=V_{SS}	−5		5	μA
I_{IH}	"H" input current D_0~D_7, $P3_0$~$P3_7$, $P4_0$~$P4_7$, $P5_0$~$P5_7$, $P6_0$~$P6_7$, $\overline{RESET}$, X_{IN}	V_I=V_{CC}	−5		5	μA
V_{RAM}	RAM retention voltage	At stop mode	2			V
I_{CC}	Supply current	At system operation f(X_{IN})=10MHz		6	10	mA
		At stop mode (Note 1)		1	10	μA

Note 1 : The terminals $\overline{RD}$, $\overline{WR}$, R/$\overline{W}$, SYNC, $RESET_{OUT}$, ϕ, D-A_1 and D-A_2 are all open The other ports, which are in the input mode, are connected to V_{SS} A-D converter is in the A-D completion state. The current through ADV_{REF} and DAV_{REF} is not included(Fig 6)

A-D CONVERTER CHARACTERISTICS

(V_{CC} = AV_{CC} = 5V, V_{SS} = AV_{SS} = 0V, T_a = 25℃, f(X_{IN})=10MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
—	Resolution				8	Bits
—	Absolute accuracy	V_{CC}=AV_{CC}=ADV_{REF}=5. 12V		±1. 5	±3	LSB
t_{CONV}	Conversion time				49	t_C(ϕ)
V_{IA}	Analog input voltage		AV_{SS}		AV_{CC}	V
V_{ADVREF}	Reference input voltage		2		V_{CC}	V
R_{LADDER}	Ladder resistance value	ADV_{REF}=5V	2	7. 5	10	kΩ
$I_{IADVREF}$	Reference input current	ADV_{REF}=5V	0. 5	0. 7	2. 5	mA
V_{AVCC}	Analog power supply input voltage			V_{CC}		V
V_{AVSS}	Analog power supply input voltage			0		V

D-A CONVERTER CHARACTERISTICS (V_{CC} = 5V, V_{SS} = AV_{SS} = 0V, T_a = 25℃, unless otherwise noted)

Symbol	Parameter	Test condition	Limits			Unit
			Min	Typ	Max	
—	Resolution				8	Bits
—	Absolute accuracy	V_{CC}=DAV_{REF}=5. 12V			1. 0	%
t_{SU}	Setup time				3	μs
R_O	Output resistance		1	2	4	kΩ
V_{AVSS}	Analog power supply input voltage			0		V
V_{DAVREF}	Reference input voltage		4		V_{CC}	V
I_{DAVREF}	Reference power input current (Each pin)		0	2. 5	5	mA

TIMING REQUIREMENTS

Port/Single-chip mode (V_{CC}=5V±10%, V_{SS}=0V, T_a=−10~70℃, unless otherwise noted)

Symbol	Parameter	Test condition	Limits			Unit
			Min	Typ	Max	
$t_{su(P3D-\phi)}$	Port P3 input setup time	Fig 3	200			ns
$t_{su(P4D-\phi)}$	Port P4 input setup time		200			ns
$t_{su(P5D-\phi)}$	Port P5 input setup time		200			ns
$t_{su(P6D-\phi)}$	Port P6 input setup time		200			ns
$t_{h(\phi-P3D)}$	Port P3 input hold time		40			ns
$t_{h(\phi-P4D)}$	Port P4 input hold time		40			ns
$t_{h(\phi-P5D)}$	Port P5 input hold time		40			ns
$t_{h(\phi-P6D)}$	Port P6 input hold time		40			ns
$t_c(X_{IN})$	External clock input cycle time		100		1000	ns
$t_w(X_{IN}L)$	External clock input "L" pulse width		30			ns
$t_w(X_{IN}H)$	External clock input "H" pulse width		30			ns
$t_r(X_{IN})$	External clock rising edge time				20	ns
$t_f(X_{IN})$	External clock falling edge time				20	ns

Master CPU bus interface timing ($\overline{R}$ and $\overline{W}$ separation type mode)

(V_{CC}=5V±10%, V_{SS}=0V, T_a=−10~70℃, unless otherwise noted)

Symbol	Parameter	Test condition	Limits			Unit
			Min	Typ	Max	
$t_{su(CS-R)}$	$\overline{CS}$ setup time	Fig. 3	0			ns
$t_{su(CS-W)}$	$\overline{CS}$ setup time		0			ns
$t_{h(R-CS)}$	$\overline{CS}$ hold time		0			ns
$t_{h(W-CS)}$	$\overline{CS}$ hold time		0			ns
$t_{su(A-R)}$	A0 setup time		40			ns
$t_{su(A-W)}$	A0 setup time		40			ns
$t_{h(R-A)}$	A0 hold time		10			ns
$t_{h(W-A)}$	A0 hold time		10			ns
$t_{w(R)}$	Read pulse width		160			ns
$t_{w(W)}$	Write pulse width		160			ns
$t_{su(D-W)}$	Date input setup time before write		100			ns
$t_{h(W-D)}$	Date input hold time after write		10			ns

Master CPU bus interface timing ($R/\overline{W}$ type mode)

(V_{CC}=5V±10%, V_{SS}=0V, T_a=−10~70℃, unless otherwise noted)

Symbol	Parameter	Test condition	Limits			Unit
			Min	Typ	Max	
$t_{su(CS-E)}$	$\overline{CS}$ setup time	Fig 4	0			ns
$t_{h(E-CS)}$	$\overline{CS}$ hold time		0			ns
$t_{su(A-E)}$	A0 setup time		40			ns
$t_{h(E-A)}$	A0 hold time		10			ns
$t_{su(RW-E)}$	$R/\overline{W}$ setup time		40			ns
$t_{h(E-RW)}$	$R/\overline{W}$ hold time		10			ns
$t_{w(EL)}$	Enable clock "L" pulse width		160			ns
$t_{w(EH)}$	Enable clock "H" pulse width		160			ns
$t_{r(E)}$	Enable clock rising edge time				25	ns
$t_{f(E)}$	Enable clock falling edge time				25	ns
$t_{su(D-E)}$	Data input setup time before write		100			ns
$t_{h(E-D)}$	Data input hold time after write		10			ns

Local bus/Memory expansion mode, Microprocessor mode

(V_{CC}=5V±10%, V_{SS}=0V, T_a=−10~70℃, unless otherwise noted)

Symbol	Parameter	Test condition	Limits			Unit
			Min	Typ.	Max.	
$t_{su(D-\phi)}$	Data input setup time	Fig 5	100			ns
$t_{h(\phi-D)}$	Data input hold time		0			ns
$t_{su(D-RD)}$	Data input setup time		100			ns
$t_{h(RD-D)}$	Data input hold time		0			ns

SWITCHING CHARACTERISTICS

Port/Single-chip mode (V_{CC}=5V±10%, V_{SS}=0V, T_a=−10~70℃, unless otherwise noted)

Symbol	Parameter	Test condition	Limits			Unit
			Min	Typ	Max	
$t_{d(\phi-P3Q)}$	Port P3 data output delay time	Fig 3			200	ns
$t_{d(\phi-P5Q)}$	Port P5 data output delay time				200	ns
$t_{d(\phi-P6Q)}$	Port P6 data output delay time				200	ns
$t_{C(\phi)}$	Cycle time		400		4000	ns
$t_{W(\phi H)}$	ϕ clock pulse width ("H" level)		190			ns
$t_{W(\phi L)}$	ϕ clock pulse width ("L" level)		170			ns
$t_{r(\phi)}$	ϕ clock rising edge time				20	ns
$t_{f(\phi)}$	ϕ clock falling edge time				20	ns

Master CPU bus interface ($\overline{R}$ and $\overline{W}$ separation type mode)

(V_{CC}=5V±10%, V_{SS}=0V, T_a=−10~70℃, unless otherwise noted)

Symbol	Parameter	Test condition	Limits			Unit
			Min	Typ	Max	
$t_{a(R-D)}$	Data output enable time after read	Fig 4			120	ns
$t_{V(R-D)}$	Data output disable time after read		10		85	ns
$t_{PLH(R-PR)}$	$\overline{P_{RDY}}$ output transmission time after read				150	ns
$t_{PLH(W-PR)}$	$\overline{P_{RDY}}$ output transmission time after write				150	ns

Master CPU bus interface (R/$\overline{W}$ type mode) (V_{CC}=5V±10%, V_{SS}=0V, T_a=−10~70℃, unless otherwise noted)

Symbol	Parameter	Test condition	Limits			Unit
			Min	Typ	Max	
$t_{a(E-D)}$	Data output enable time after read	Fig 4			120	ns
$t_{V(E-D)}$	Data output disable time after read		10		85	ns
$t_{PLH(E-PR)}$	$\overline{P_{RDY}}$ output transmission time after E clock				150	ns

Local bus/Memory expansion mode, microprocessor mode

(V_{CC}=5V±10%, V_{SS}=0V, T_a=−10~70℃, unless otherwise noted)

Symbol	Parameter	Test condition	Limits			Unit
			Min	Typ	Max	
$t_{d(\phi-A)}$	address delay time after ϕ	Fig 5			120	ns
$t_{V(\phi-A)}$	address effective time after ϕ		10			ns
$t_{V(RD-A)}$	address effective time after $\overline{RD}$		10			ns
$t_{V(WR-A)}$	address effective time after $\overline{WR}$		10			ns
$t_{d(\phi-D)}$	data output delay time after ϕ				140	ns
$t_{d(WR-D)}$	data output delay time after $\overline{WR}$				140	ns
$t_{V(\phi-D)}$	data output effective time after ϕ		20			ns
$t_{V(WR-D)}$	data output effective time after $\overline{WR}$		20			ns
$t_{d(\phi-RW)}$	R/$\overline{W}$ delay time after ϕ				120	ns
$t_{d(\phi-SYNC)}$	SYNC delay time after ϕ				120	ns
$t_{W(RD)}$	$\overline{RD}$ pulse width		170			ns
$t_{W(WR)}$	$\overline{WR}$ pulse width		170			ns

TEST CONDITION

Input voltage level : V_{IH} 2.4V

V_{IL} 0.45V

Output test level : V_{OH} 2.0V

V_{OL} 0.8V

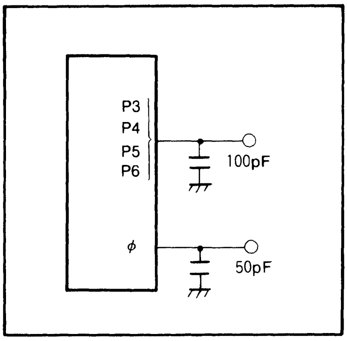


Fig. 3 Test circuit in single-chip mode

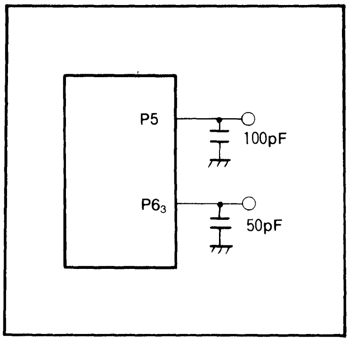


Fig. 4 Master CPU bus interface test circuit

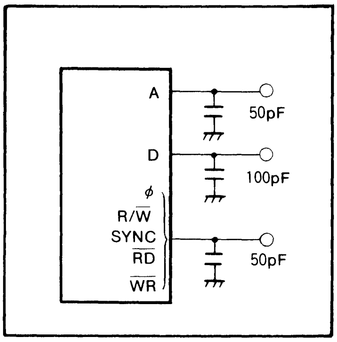


Fig. 5 Local bus test circuit

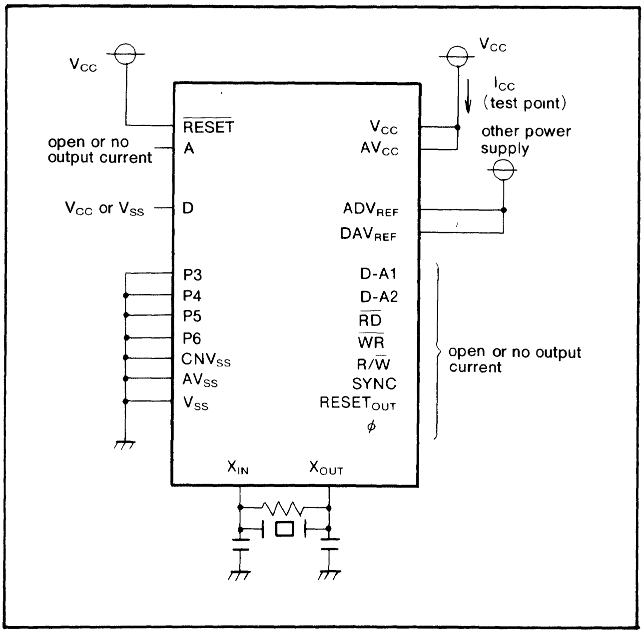
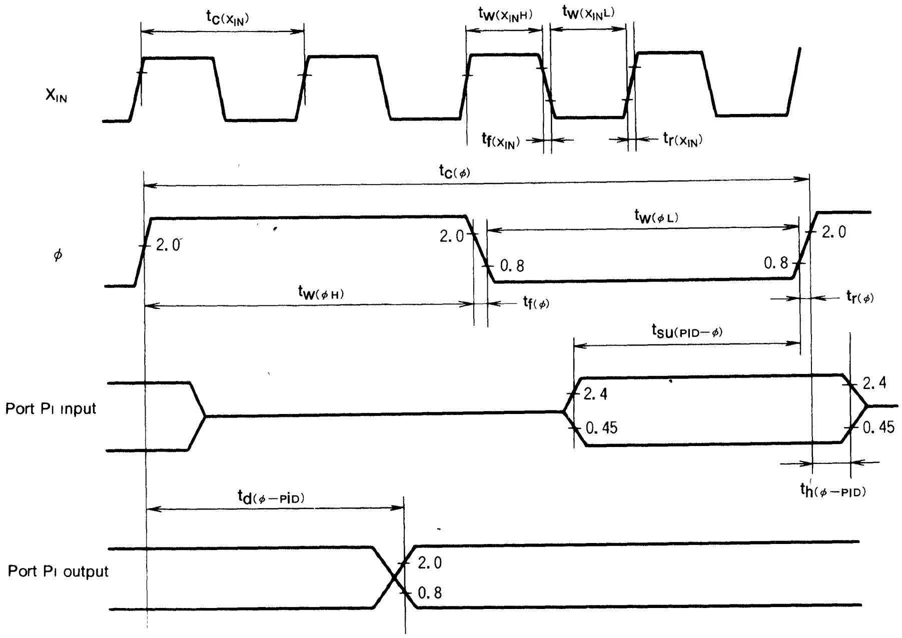


Fig. 6 I_{CC} (at stop mode) test condition

TIMING DIAGRAM

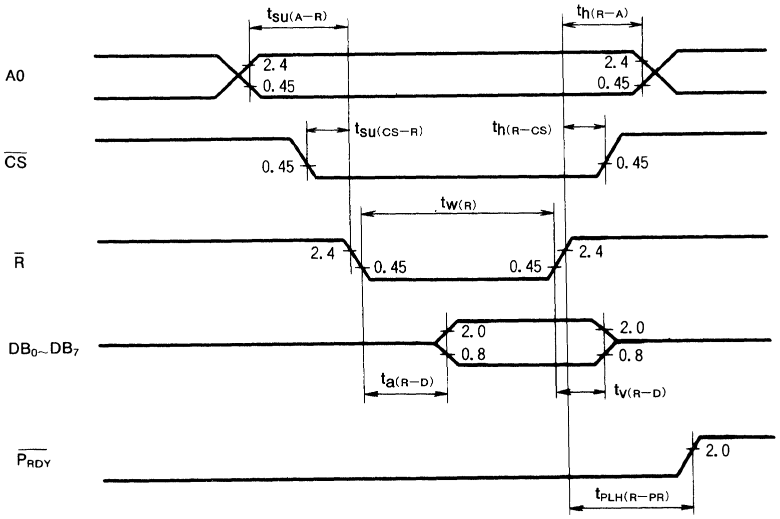
Port/single-chip mode timing diagram



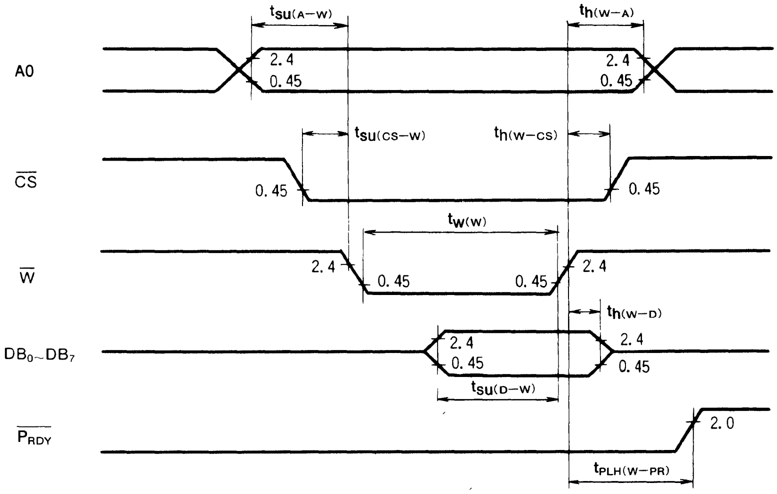
Note : $V_{IH}=0.8V_{CC}$, $V_{IL}=0.16V_{CC}$ of X_{IN}

Master CPU bus interface/ $\overline{R}$ and $\overline{W}$ separation type timing diagram

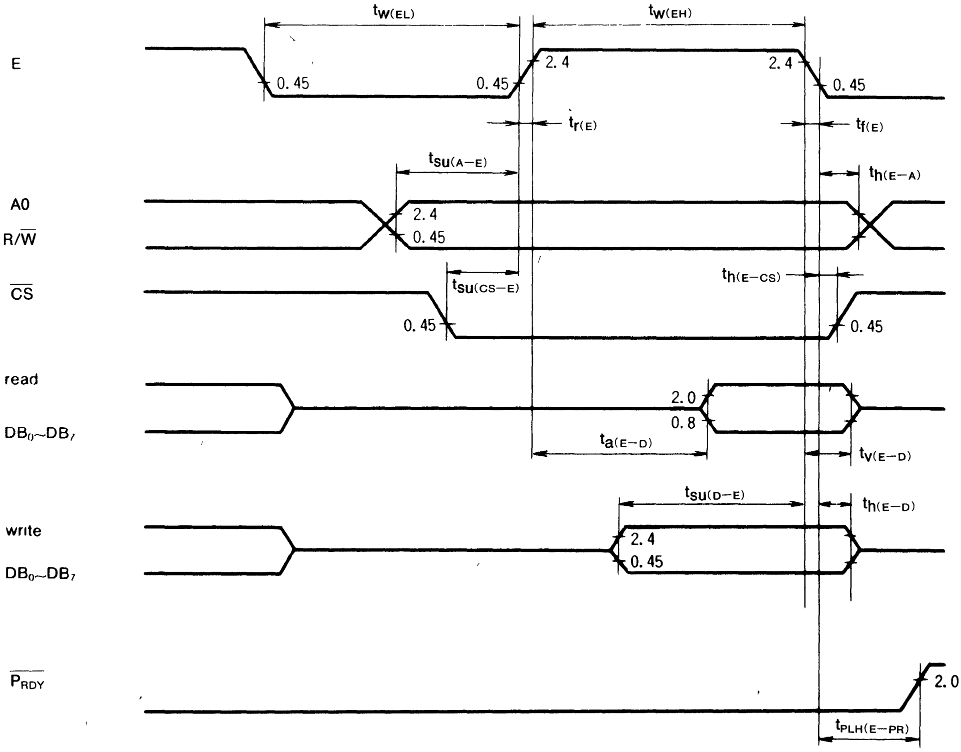
$\overline{\text{Read}}$



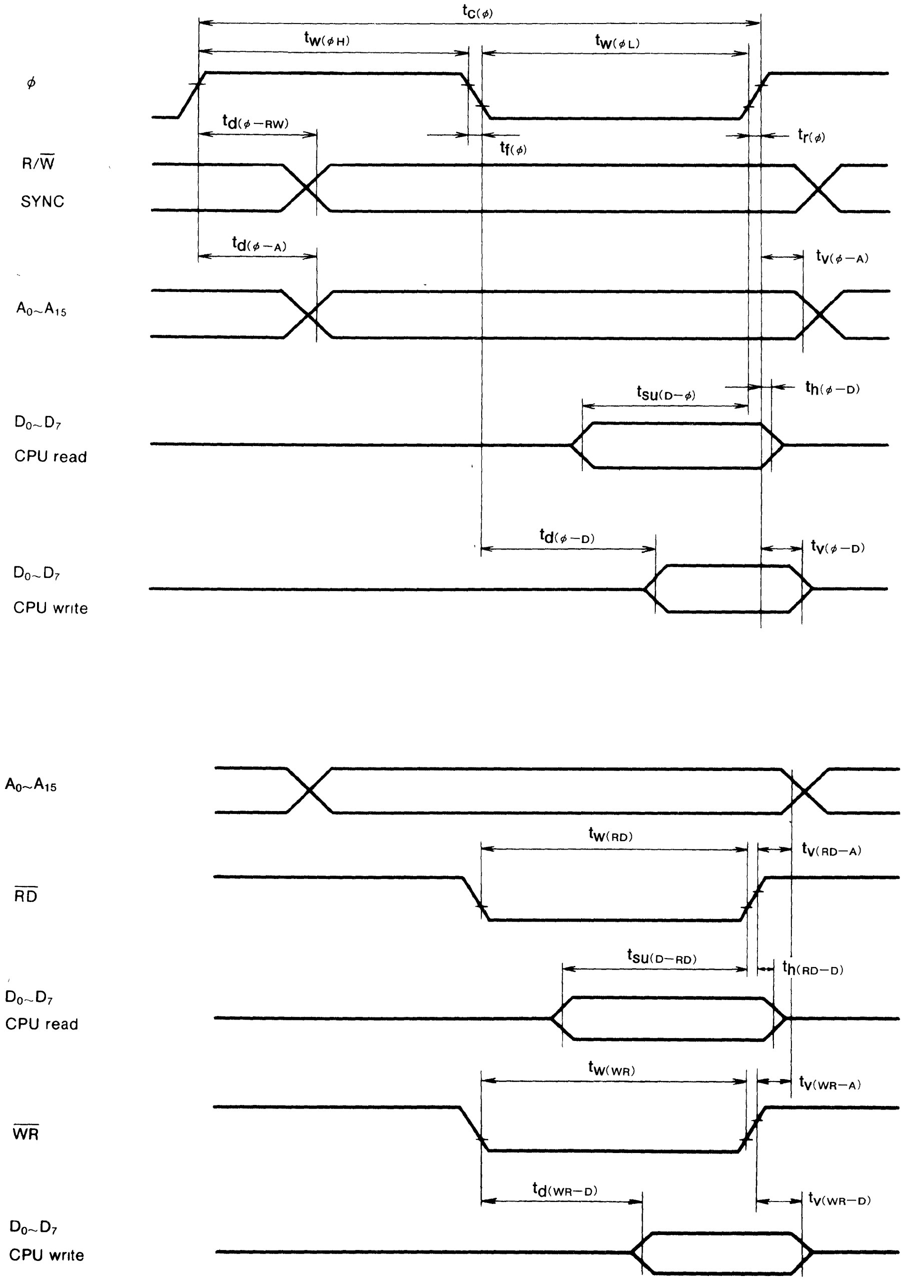
Write



Master CPU interface/ R/W type timing diagram



Local bus timing diagram



M37451M4-XXXSP/FP/GP
M37451M8-XXXSP/FP/GP
M37451MC-XXXSP/FP/GP
SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

DESCRIPTION

The M37451M4-XXXSP/FP/GP is a single-chip microcomputer designed with CMOS silicon gate technology. It is housed in a 64-pin shrink plastic molded DIP or a 0.8mm-pitch or 0.65mm-pitch 80-pin plastic molded QFP.

In addition to its simple instruction sets, the ROM, RAM, and I/O addresses are placed on the same memory map to enable easy programming.

It is suited for office automation equipment and control devices The low power consumption made by the use of a CMOS process makes it especially suitable for battery powered devices requiring low power consumption. It also has a unique feature that enables it to be used as a slave microcomputer.

The differences among M37451M4-XXXSP/FP/GP, M37451 M8-XXXSP/FP/GP and M37451MC-XXXSP/FP/GP are as shown below. The descriptions that follow describe the M37451M4-XXXSP/FP/GP (abbreviated as M37451) unless otherwise noted.

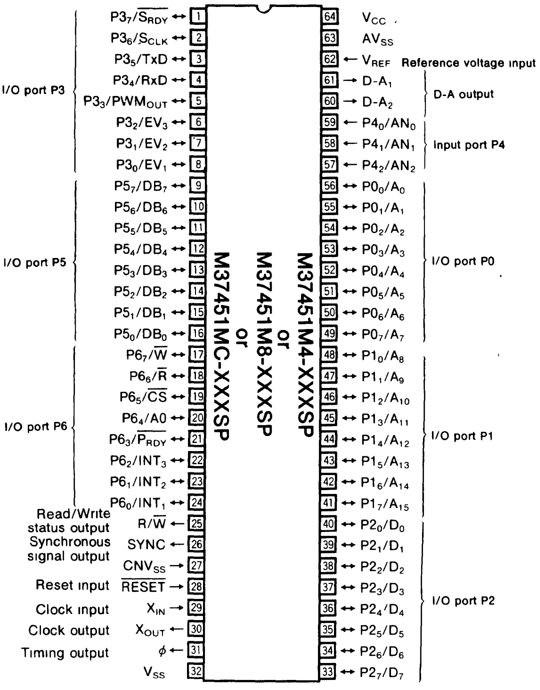
Type name	ROM size	RAM size
M37451M4-XXXSP/FP/GP	8192 bytes	256 bytes
M37451M8-XXXSP/FP/GP	16384 bytes	384 bytes
M37451MC-XXXSP/FP/GP	24576 bytes	512 bytes

The number of analog input pins for the 80-pin model (FP, GP version) is different from the 64-pin model (SP version). In addition, the 80-pin model has special pins for $\overline{RD}$, $\overline{WR}$, $RESET_{OUT}$, DAV_{REF}, ADV_{REF}, AV_{CC} and the 64-pin model has a special V_{REF} pin.

FEATURES

- Number of basic instructions ···································· 71
  69 MELPS 740 basic instructions+2 multiply/divide instructions
- Instruction execution time
  (minimum instructions at 12.5MHz frequency) ···· 0.64μs
- Single power supply ························· ···········5V±10%
- Power dissipation normal operation mode
  (at 12.5MHz frequency) ································40mW
- Subroutine nesting ············· 96 levels max.(M37451M4)
  96 levels max.(M37451M8)
  128 levels max.(M37451MC)
- Interrupt ··· 15 events
- Master CPU bus interface ······························1 byte
- 16-bit timer ··3
- 8-bit timer (Serial I/O use) ·································1
- Serial I/O (UART or clock synchronous) ···················1
- A-D converter (8-bit resolution) ········· 3 channels (DIP)
  8 channels (QFP)
- D-A converter (8-bit resolution) ················· 2 channels
- PWM output with 8-bit prescaler
  (Either resolution 8 bit or 16 bit is software selectable) ····1

PIN CONFIGURATION (TOP VIEW)



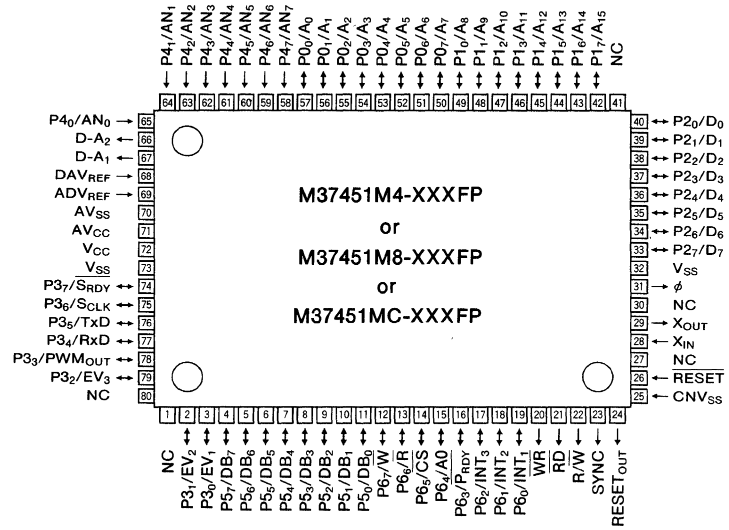
Outline 64P4B

- Programmable I/O ports
  (Ports P0, P1, P2, P3, P5, P6) ······························ 48
- Input port (Port P4) ··························· 3(DIP), 8(QFP)
- Output ports (Ports D-A_1, D-A_2) ·······························2

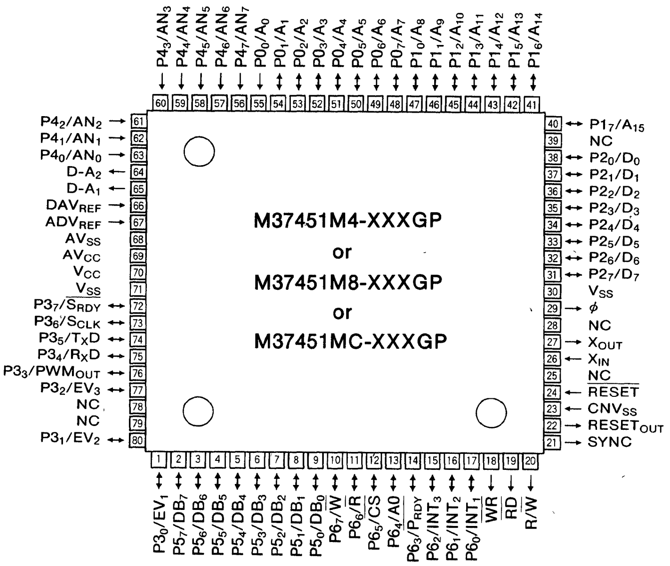
APPLICATION

Slave controller for PPCs, facsimiles, and page printers. HDD, optical disk, inverter, and industrial motor controllers. Industrial robots and machines.

PIN CONFIGURATION (TOP VIEW)



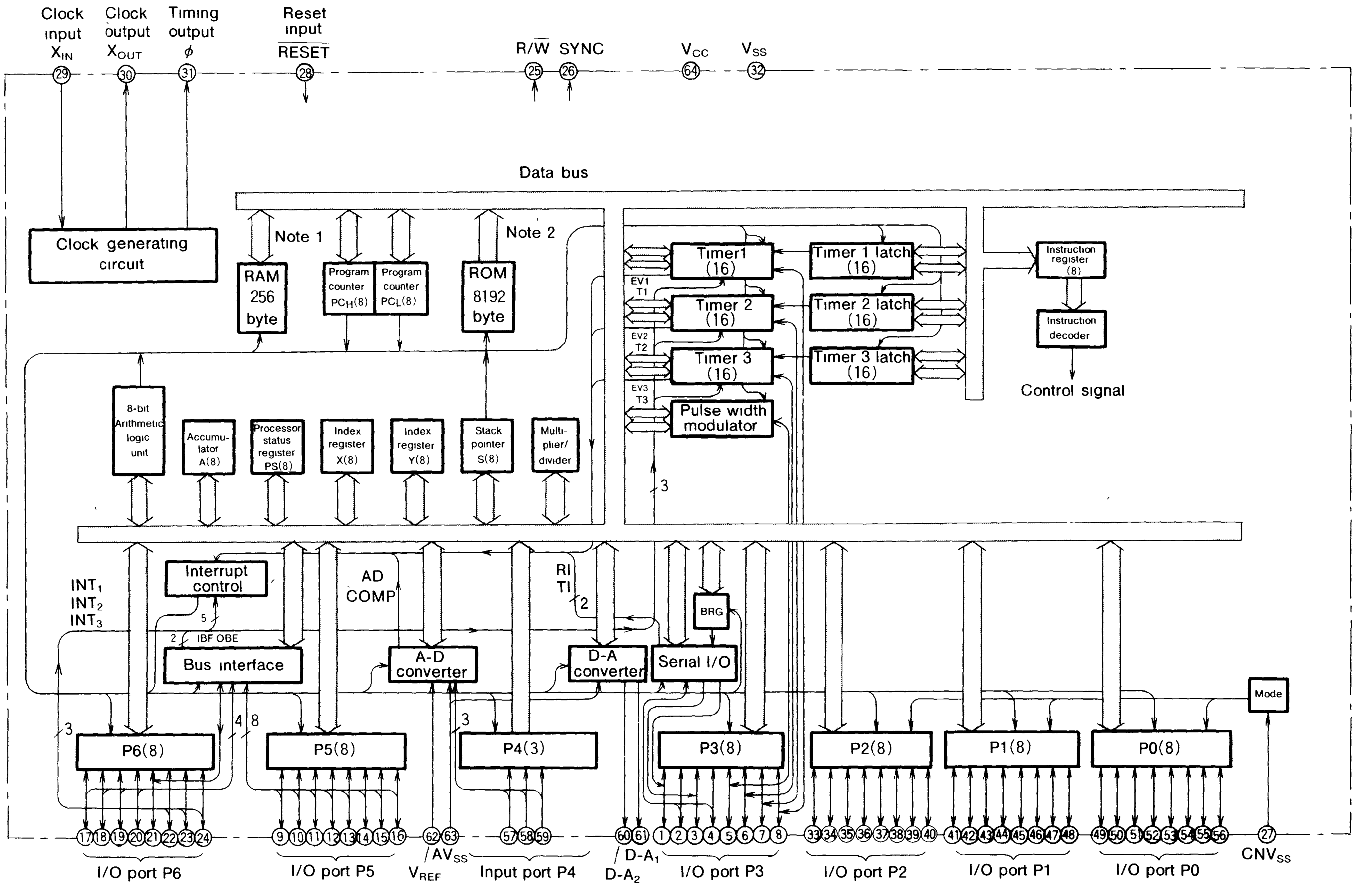
Outline 80P6N



Outline 80P6S

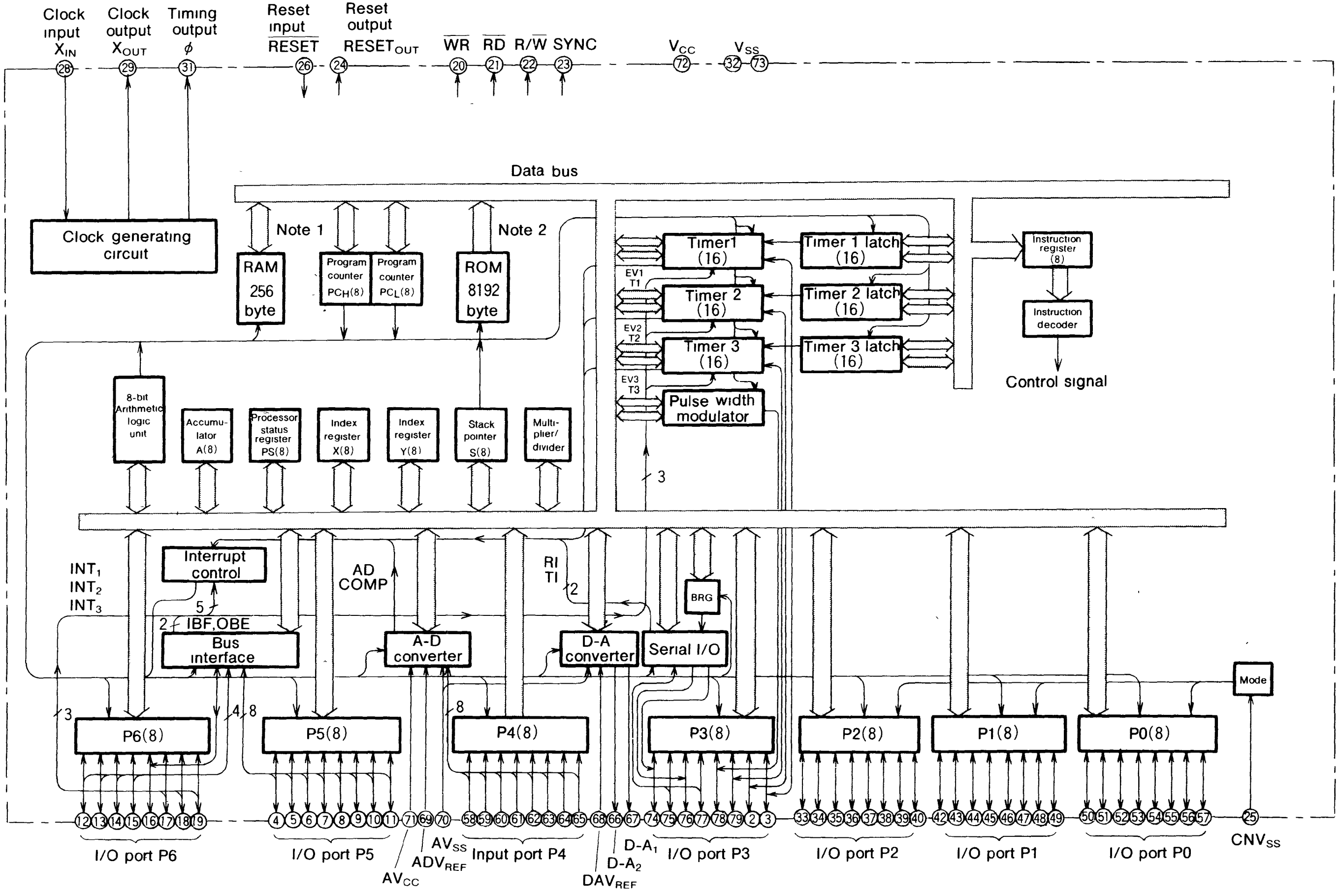
NC : No connection

M37451M4-XXXSP BLOCK DIAGRAM



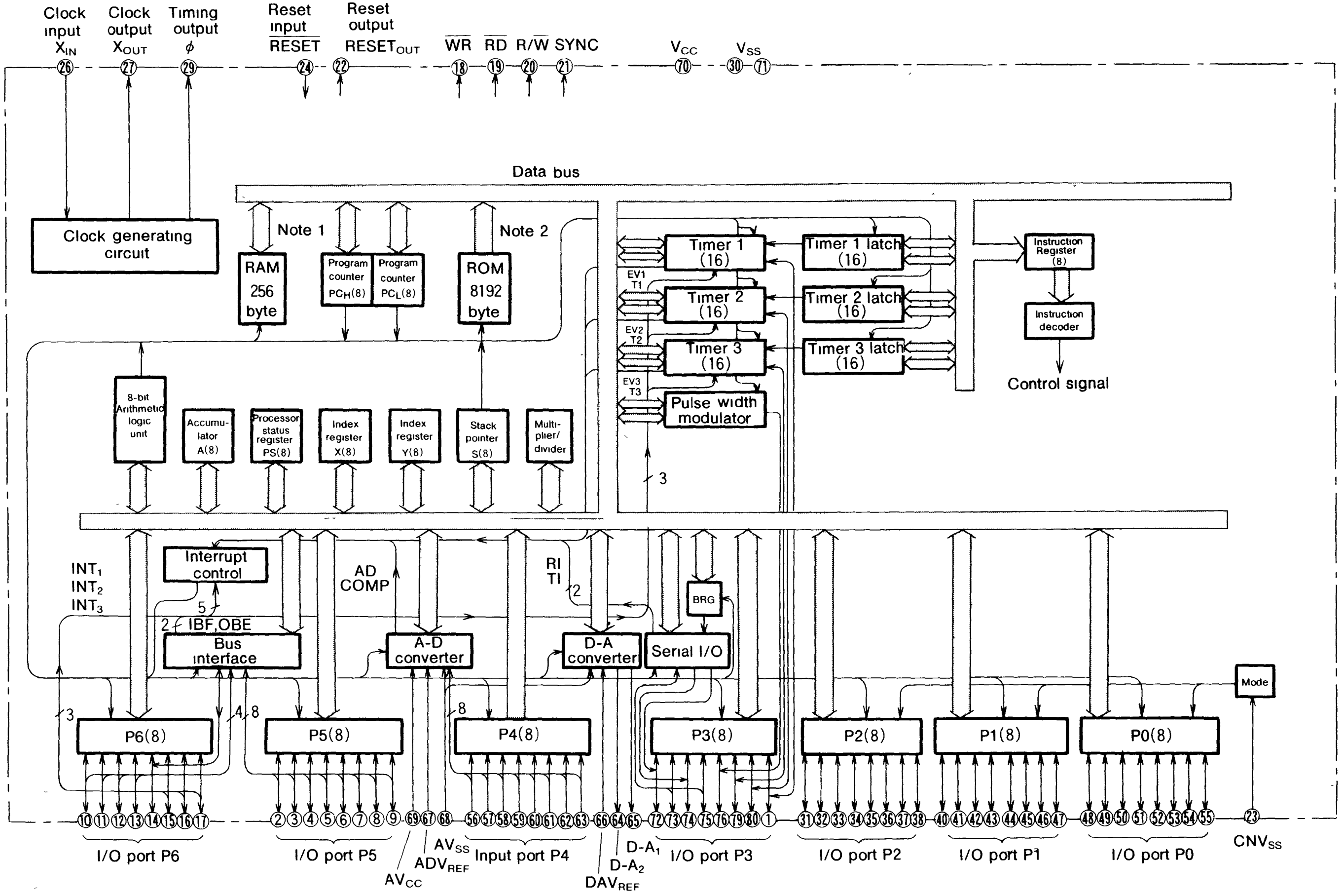
Note 1 : 384 bytes for M37451M8-XXXSP and 512 bytes for M37451MC-XXXSP
2 : 16384 bytes for M37451M8-XXXSP and 24576 bytes for M37451MC-XXXSP

M37451M4-XXXFP BLOCK DIAGRAM



Note 1 : 384 bytes for M37451M8-XXXFP and 512 bytes for M37451MC-XXXFP
2 : 16384 bytes for M37451M8-XXXFP and 24576 bytes for M37451MC-XXXFP

M37451M4-XXXGP BLOCK DIAGRAM



Note 1 : 384 bytes for M37451M8-XXXGP and 512 bytes for M37451MC-XXXGP
2 : 16384 bytes for M37451M8-XXXGP and 24576 bytes for M37451MC-XXXGP

FUNCTIONS OF M37451M4-XXXSP/FP/GP, M37451M8-XXXSP/FP/GP, M37451MC-XXXSP/FP/GP

Parameter			Functions
Number of basic instructions			71(69 MELPS 740 basic instructions+2)
Instruction execution time			0.64μs (minimum instructions, at 12.5MHz frequency)
Clock frequency			12.5MHz (max.)
Memory size	M37451M4-XXXSP/FP/GP	ROM	8192 bytes
		RAM	256 bytes
	M37451M8-XXXSP/FP/GP	ROM	16384 bytes
		RAM	384 bytes
	M37451MC-XXXSP/FP/GP	ROM	24576 bytes
		RAM	512 bytes
Input/Output ports	P0-P3, P5, P6	I/O	8-bit×6
	P4	Input	3-bit×1 (8-bit×1 for 80-pin model)
	D-A	Output	2-bit×1
Serial I/O			UART or clock synchronous
Timers			16-bit timer×3, 8-bit timer (serial I/O baud rate generator)×1
A-D converter			8-bit×3 channels (8 channels for 80-pin model)
D-A converter			8-bit×2 channels
Pulse width modulator with 8-bit prescaler			8-bit or 16-bit×1
Data bus buffer			1-byte input and output each
Subroutine nesting			96-levels (max. for M37451M4, M37451M8)
			128-levels (max. for M37451MC)
Interrupt			6 external interrupts, 8 internal interrupts 1 software interrupt
Clock generating circuit			Built-in (ceramic or quarts crystal oscillator)
Supply voltage			5V±10%
Power dissipation			40mW (at 12.5MHz frequency)
Input/Output characters	Input/Output voltage		5V
	Output current		±5mA (max.)
Memory expansion			Possible (64K bytes max.)
Operating temperature range			−20 to 85℃
Device structure			CMOS silicon gate
Package	M37451M4-XXXSP		64-pin shrink plastic molded DIP
	M37451M8-XXXSP		
	M37451MC-XXXSP		
	M37451M4-XXXFP		80-pin plastic molded QFP (0.8mm-pitch)
	M37451M8-XXXFP		
	M37451MC-XXXFP		
	M37451M4-XXXGP		80-pin plastic molded QFP (0.65mm-pitch)
	M37451M8-XXXGP		
	M37451MC-XXXGP		

PIN DESCRIPTION

Pin	Name	Input/ Output	Functions
V_{CC}, V_{SS}	Supply voltage		Power supply inputs 5V±10% to V_{CC}, and 0V to V_{SS}
CNV_{SS}	CNV_{SS}	Input	Controls the processor mode of the chip Normally connected to V_{SS} or V_{CC}
$\overline{RESET}$	Reset input	Input	To enter the reset state, the reset input pin must be kept at a "L" for more than 8 clock cycles (under normal V_{CC} conditions) If more time is needed for the crystal oscillator to stabilize, this "L" condition should be maintained for the required time
X_{IN}	Clock input	Input	This chip has an internal clock generating circuit To control generating frequency, an external ceramic or a quartz crystal oscillator is connected between the X_{IN} and X_{OUT} pins If an external clock is used, the clock source should be connected to the X_{IN} pin and the X_{OUT} pin should be left open
X_{OUT}	Clock output	Output	
ϕ	Timing output	Output	Normally outputs signal consisting of oscillating frequency divided by four
SYNC	Synchronous signal output	Output	This signal is output "H" during operation code fetch and is used to control single stepping of programs
$R/\overline{W}$	Read/Write status output	Output	This signal determines the direction of the data bus It is "H" during read and "L" during write
$P0_0$-$P0_7$	I/O port P0	I/O	Port P0 is an 8-bit I/O port with directional registers allowing each I/O bit to be individually programmed as input or output The output structure is CMOS output The low-order bits of the address are output except in single-chip mode
$P1_0$-$P1_7$	I/O port P1	I/O	Port P1 is an 8-bit I/O port and has basically the same functions as port P0 The high-order bits of the address are output except in single-chip mode
$P2_0$-$P2_7$	I/O port P2	I/O	Port P2 is an 8-bit I/O port and has basically the same functions as port P0 Used as data bus except in single-chip mode
$P3_0$-$P3_7$	I/O port P3	I/O	Port P3 is an 8-bit I/O port and has basically the same functions as port P0 Serial I/O, PWM output, or event I/O function can be selected with a program
$P4_0$-$P4_2$ ($P4_0$-$P4_7$)	Input port P4	Input	Analog input pin for the A-D converter The 64-pin model has three pins and the 80-pin model has eight pins They may also be used as digital input pins
$P5_0$-$P5_7$	I/O port P5	I/O	Port P5 is an 8-bit I/O port and has basically the same functions as port P0 This port functions as an 8-bit data bus for the master CPU when slave mode is selected with a program
$P6_0$-$P6_7$	I/O port P6	I/O	Port P6 is an 8-bit I/O port and has basically the same function as port P0 Pins $P6_3$-$P6_7$ change to a control bus for the master CPU when slave mode is selected with a program Pins $P6_0$-$P6_2$ may be programmed as external interrupt input pins
D-A_1, D-A_2	D-A output	Output	Analog signal from D-A converter is output
V_{REF}	Reference voltage input	Input	Reference voltage input pin for A-D and D-A converter This pin is for 64-pin model only
ADV_{REF}	A-D reference voltage input	Input	Reference voltage input pin for A-D converter This pin is for 80-pin model only
DAV_{REF}	D-A reference voltage input	Input	Reference voltage input pin for D-A converter This pin is for 80-pin model only
AV_{SS}	Analog power supply		Ground level input pin for A-D and D-A converter Same voltage as V_{SS} is applied
AV_{CC}	Analog power supply		Power supply input pin for A-D converter This pin is for 80-pin model only Same voltage as V_{CC} is applied. In the case of the 64-pin model, AV_{CC} is connected to V_{CC} internally
$\overline{RD}$	Read signal output	Output	Control signal output as active "L" when valid data is read from data bus This pin is for 80-pin model only.
$\overline{WR}$	Write signal output	Output	Control signal output as active "L" when writing data from data bus to external component This pin is for 80-pin model only
$RESET_{OUT}$	Reset output	Output	Control signal output as active "H" during reset It is used as a reset output signal for peripheral components This pin is for 80-pin model only

FUNCTIONAL DESCRIPTION

Central Processing Unit (CPU)

The M37451 microcomputers use the standard MELPS 740 instruction set. For details of instructions, refer to the MELPS 740 CPU core basic functions, or the MELPS 740 Software Manual.

Machine-resident instructions are as follows:

The FST and SLW instructions are not provided.

The MUL and DIV instructions can be used.

The WIT instruction can be used.

The STP instruction can be used.

MISRG2 Register

The MISRG2 register is allocated to address $00DF_{16}$. Bits 0 and 1 of this register are processor mode bits. This register also has a stack page selection bit.

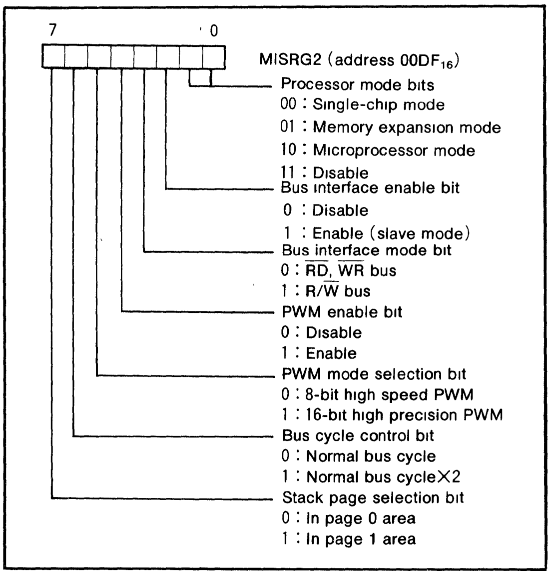


Fig. 1 Structure of MISRG 2

MEMORY

- **Special Function Register (SFR) Area**

The special function register (SFR) area contains the registers relating to functions such as I/O ports and timers.

- **RAM**

RAM is used for data storage as well as a stack area.

- **ROM**

ROM is used for storing user programs as well as the interrupt vector area.

- **Interrupt Vector Area**

The interrupt vector area is for storing jump destination addresses used at reset or when an interrupt is generated.

- **Zero Page**

Zero page addressing mode is useful because it enables access to this area with only 2 bytes.

- **Special Page**

Special page addressing mode is useful because it enables access to this area with only 2 bytes.

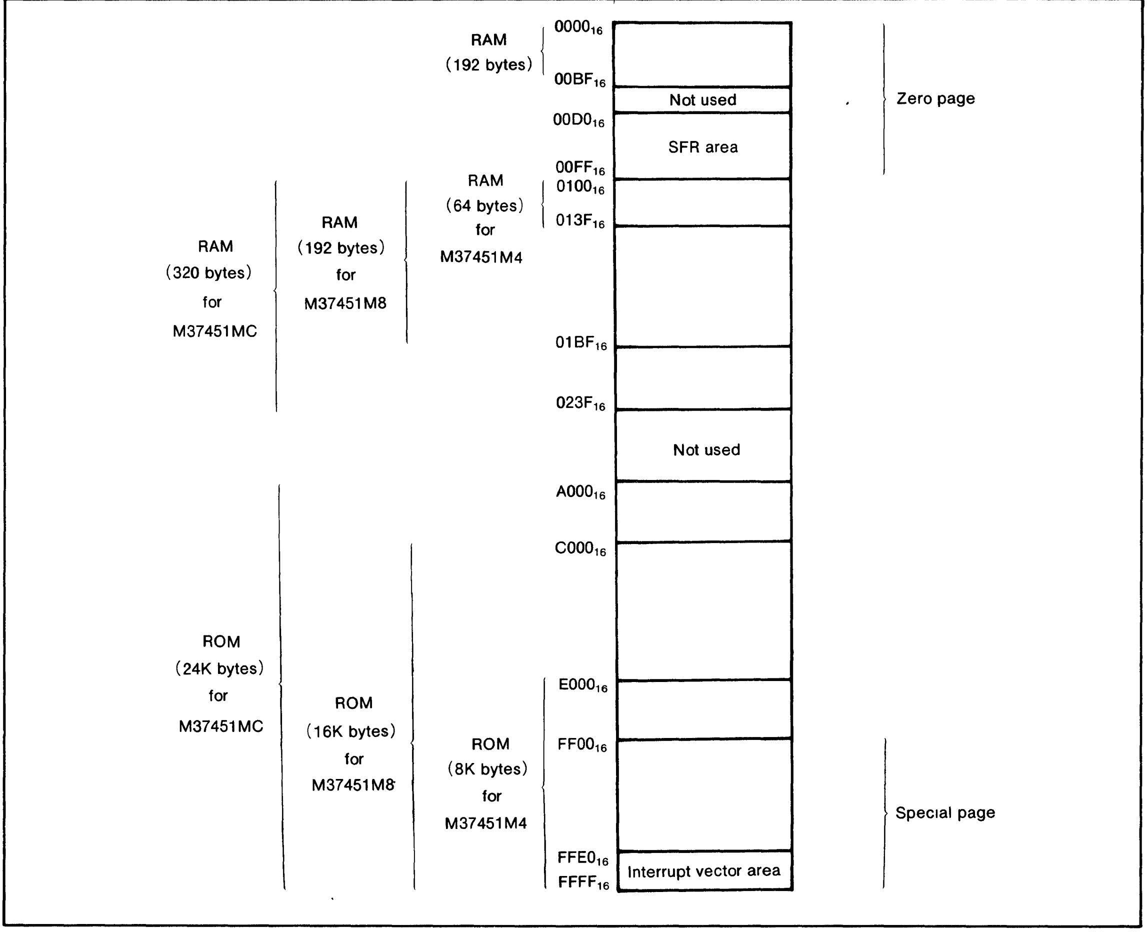


Fig. 2 Memory map

$00D0_{16}$	P0 register
$00D1_{16}$	P0 directional register
$00D2_{16}$	P1 register
$00D3_{16}$	P1 directional register
$00D4_{16}$	P2 register
$00D5_{16}$	P2 directional register
$00D6_{16}$	P3 register
$00D7_{16}$	P3 directional register
$00D8_{16}$	P4 register/PWM prescaler latch
$00D9_{16}$	Additional function register
$00DA_{16}$	P5 register
$00DB_{16}$	P5 directional register
$00DC_{16}$	P6 register
$00DD_{16}$	P6 directional register
$00DE_{16}$	MISRG1
$00DF_{16}$	MISRG2
$00E0_{16}$	D-A1 register
$00E1_{16}$	D-A2 register
$00E2_{16}$	A-D register
$00E3_{16}$	A-D control register
$00E4_{16}$	Data bus buffer register
$00E5_{16}$	Data bus buffer status register
$00E6_{16}$	Receive/Transmit buffer register
$00E7_{16}$	Serial I/O status register
$00E8_{16}$	Serial I/O control register
$00E9_{16}$	UART control register
$00EA_{16}$	Baud rate generator
$00EB_{16}$	PWM register (low-order)
$00EC_{16}$	PWM register (high-order)
$00ED_{16}$	Timer 1 control register
$00EE_{16}$	Timer 2 control register
$00EF_{16}$	Timer 3 control register
$00F0_{16}$	Timer 1 register (low-order)
$00F1_{16}$	Timer 1 register (high-order)
$00F2_{16}$	Timer 1 latch (low-order)
$00F3_{16}$	Timer 1 latch (high-order)
$00F4_{16}$	Timer 2 register (low-order)
$00F5_{16}$	Timer 2 register (high-order)
$00F6_{16}$	Timer 2 latch (low-order)
$00F7_{16}$	Timer 2 latch (high-order)
$00F8_{16}$	Timer 3 register (low-order)
$00F9_{16}$	Timer 3 register (high-order)
$00FA_{16}$	Timer 3 latch (low-order)
$00FB_{16}$	Timer 3 latch (high-order)
$00FC_{16}$	Interrupt request register 1
$00FD_{16}$	Interrupt request register 2
$00FE_{16}$	Interrupt control register 1
$00FF_{16}$	Interrupt control register 2

Fig. 3 SFR (Special Function Register) memory map

INTERRUPTS

Interrupts can be caused by 15 different events consisting of six external, eight internal, and one software events.

Interrupts are vectored interrupts with priorities shown in Table 1. Reset is also included in the table because its operation is similar to an interrupt.

When an interrupt is accepted, the registers are pushed, interrupt disable flag I is set, and the program jumps to the address specified in the vector table. The interrupt request bit is cleared automatically. The reset and BRK instruction interrupt can never be disabled. Other interrupts are disabled when the interrupt disable flag is set.

All interrupts except the BRK instruction interrupt have an interrupt request bit and an interrupt enable bit. The interrupt request bits are in interrupt request registers 1 and 2 and the interrupt enable bits are in interrupt control registers 1 and 2. Figure 4 shows the structure of the interrupt request registers 1 and 2 and interrupt control registers 1 and 2.

Interrupts other than the BRK instruction interrupt and reset are accepted when the interrupt enable bit is "1", interrupt request bit is "1", and the interrupt disable flag is "0". The interrupt request bit can be reset with a program, but not set. The interrupt enable bit can be set and reset with a program.

Reset is treated as a non-maskable interrupt with the highest priority. Figure 5 shows interrupts control.

Table 1. Interrupt vector address and priority.

Event	Priority	Vector addresses	Remarks
$\overline{\text{RESET}}$	1	$FFFF_{16}$, $FFFE_{16}$	Non-maskable
Input buffer full interrupt	2	$FFFD_{16}$, $FFFC_{16}$	Valid only in slave mode
Output buffer empty interrupt	3	$FFFB_{16}$, $FFFA_{16}$	Valid only in slave mode
INT_1 interrupt	4	$FFF9_{16}$, $FFF8_{16}$	External interrupt (phase programmable)
INT_2 interrupt	5	$FFF7_{16}$, $FFF6_{16}$	External interrupt (phase programmable)
INT_3 interrupt	6	$FFF5_{16}$, $FFF4_{16}$	External interrupt (phase programmable)
Timer 1 interrupt	7	$FFF3_{16}$, $FFF2_{16}$	
Timer 2 interrupt	8	$FFF1_{16}$, $FFF0_{16}$	
Timer 3 interrupt	9	$FFEF_{16}$, $FFEE_{16}$	
EV_1 interrupt	10	$FFED_{16}$, $FFEC_{16}$	External event interrupt (phase programmable)
EV_2 interrupt	11	$FFEB_{16}$, $FFEA_{16}$	External event interrupt (phase programmable)
EV_3 interrupt	12	$FFE9_{16}$, $FFE8_{16}$	External event interrupt (phase programmable)
Serial I/O receive interrupt	13	$FFE7_{16}$, $FFE6_{16}$	Valid only when serial I/O is selected
Serial I/O transmit interrupt	14	$FFE5_{16}$, $FFE4_{16}$	Valid only when serial I/O is selected
A-D conversion completion flag	15	$FFE3_{16}$, $FFE2_{16}$	
BRK instruction interrupt	16	$FFE1_{16}$, $FFE0_{16}$	Non-maskable software interrupt

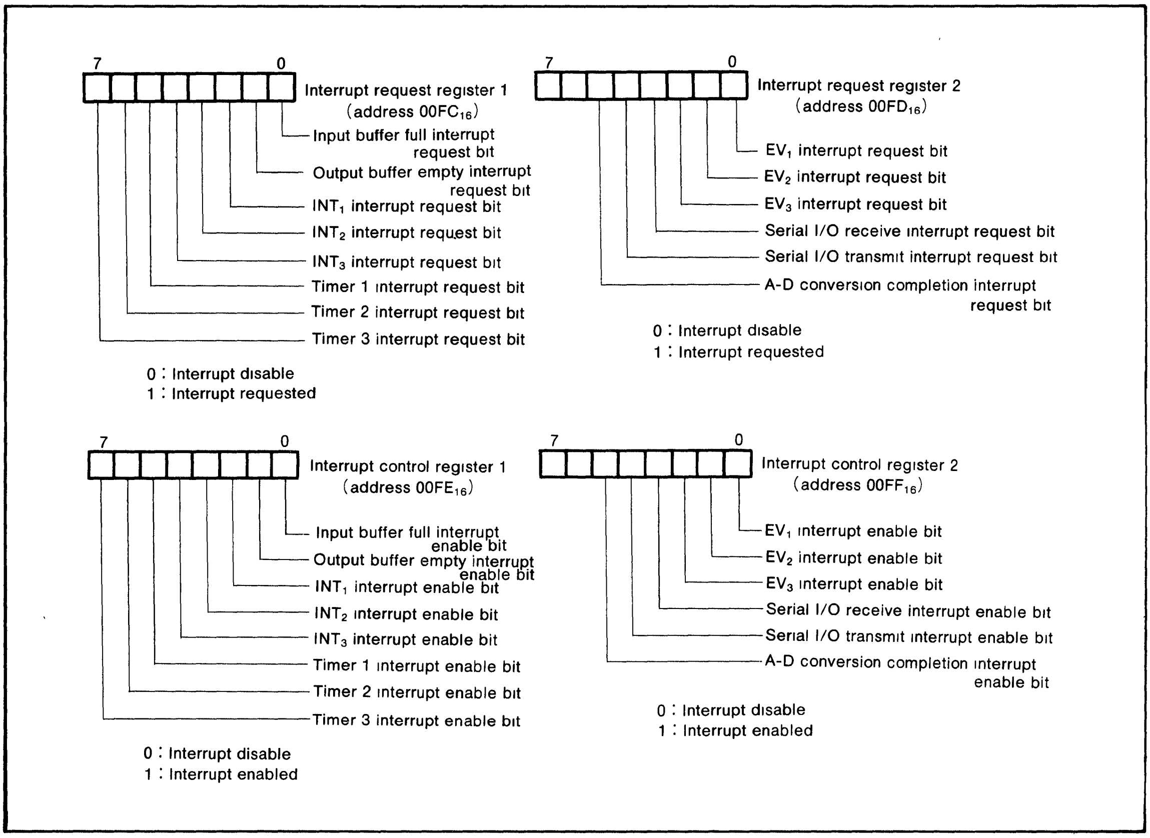


Fig. 4 Structure of registers related to interrupt

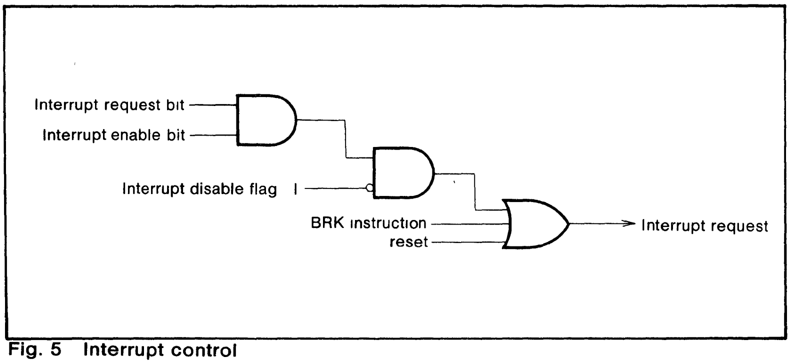


Fig. 5 Interrupt control

TIMER

The M37451 has three independent 16-bit internal timers as shown in Figure 6.

The timers are controlled by the timer i control register (i= 1, 2, 3) and MISRG1 shown in Figure 7 and 8.

The timer and the timer latch are independent of each other and a value must be written in both when setting a timer.

A write to a timer is performed in the order of T_L to T_H after setting the count enable bit to count inhibit "0".

A read from a timer is performed in the order of T_H to T_L. The value of T_L is latched in the read timer latch at the timing when T_H is read. All timers are decrement counters and are started by setting the timer i count enable bit to "1". When the value of the timer reaches 0000_{16}, and overflow occurs and the timer i interrupt request bit is set to "1" at the next count pulse.

During a reset or an STP instruction execution, the low-order byte of the timer 1 register is set to FF_{16} and the high-order byte is set to 03_{16}. Also, when an STP instruction is executed, a frequency obtained by dividing the oscillating frequency by four becomes the timer 1 input regardless of the timer 1 count source selection bit. This condition is canceled and the original count source is resumed when the timer i interrupt request bit is set to "1" or when a reset occurs. Refer to the section on the clock generator for details concerning the operation of the STP instruction.

The M37451 provides seven timer modes selectable with the timer mode selection bit in the timer i control register.

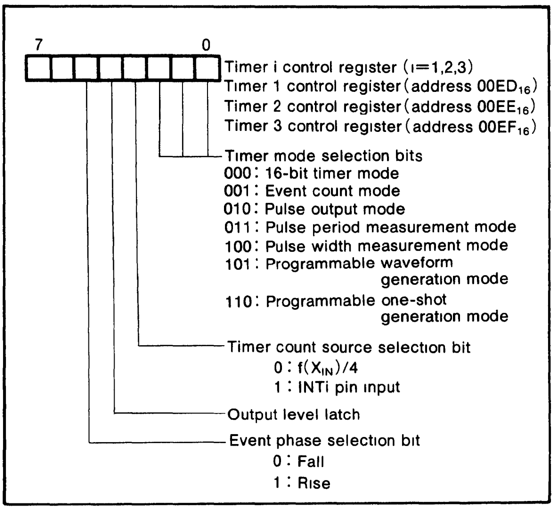


Fig. 7 Structure of timer i control register

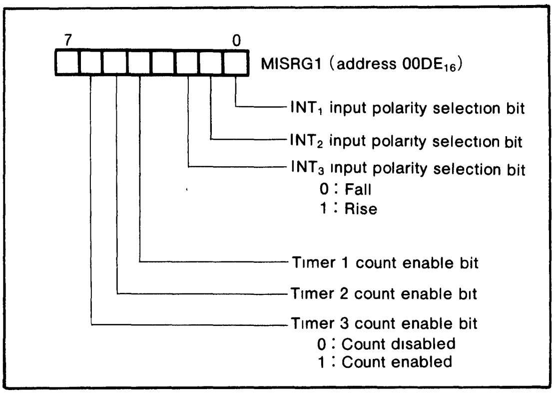


Fig. 8 Structure of MISRG1

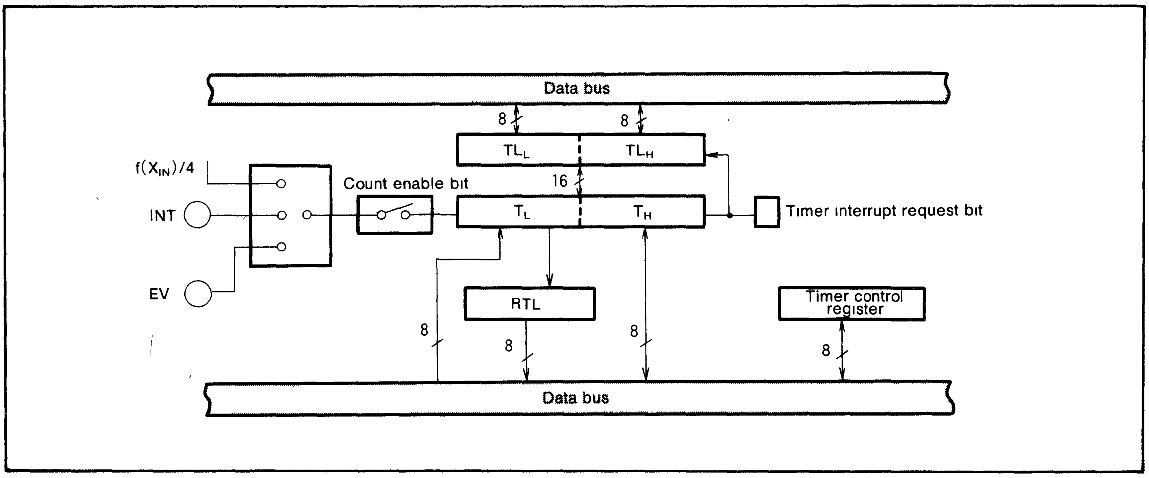


Fig. 6 Timer block diagram

(1) 16-bit Timer Mode [000]

In this mode, an interrupt request occurs and the value of the timer latch is loaded in the timer each time the timer overflows.

The timer count source is set to $f(X_{IN})$ divided by four regardless of the count sorce selection bit. Assuming that the timer latch is n, the frequency dividing ratio is $1/(n+1)$.

Figure 9 shows the timer operation during 16-bit timer mode.

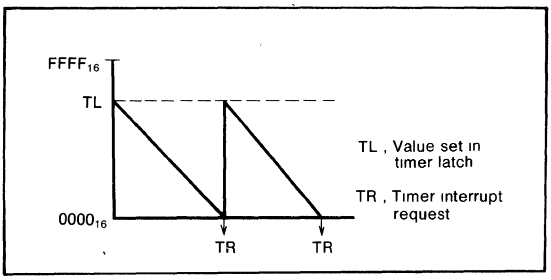


Fig. 9 16-bit timer mode operation

(2) Event Count Mode [001]

In this mode, the EVi pin input signal are counted in the direction selected by the event input polarity selection bit.

The input signal from the EVi pin is used as the count source regardless of the count source selection bit. The operation is the same as with the 16-bit timer mode except for the difference in the count source.

Both the "H" and "L" pulse width of the EVi pin input signal must be not less than $(4/f(X_{IN}))+100ns$.

Figure 10 shows the timer operation during event count mode.

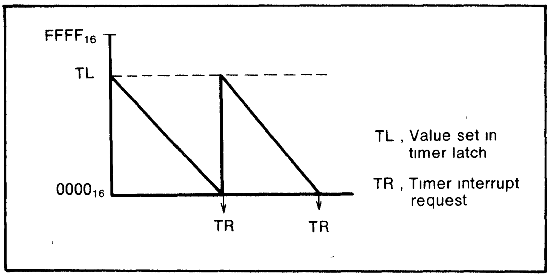


Fig. 10 Event counter mode operation

(3) Pulse Output Mode [010]

In this mode, a 50% duty pulse is output from the EVi pin.

The count source selected with the count source selection bit is counted. When it overflows, the phase of the EVi pin output level is reversed and the value of the timer latch is loaded in the timer.

When this mode is selected, the EVi pin output level is initialized to "L".

Figure 11 shows the timer operation during pulse output mode.

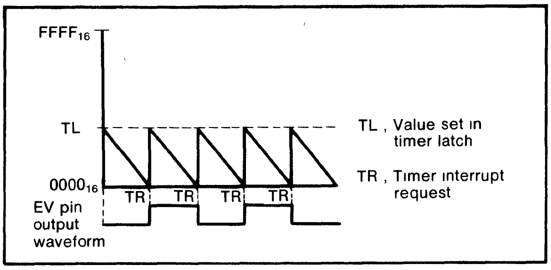


Fig. 11 Pulse output mode

(4) Pulse Period Measurement Mode [011]

This mode is used to measure the pulse period of the EVi pin input signal.

The timer counts the count source selected by the count source selection bit between the rise-to-rise or fall-to-fall interval (selected with the event input polarity selection bit in the timer i control register) of the EVi pin input signal.

At a valid edge on the EVi pin input, the 1's complement of the timer value is stored in the timer latch and the timer value is set to $FFFF_{16}$.

Figure 12 shows the timer operation during pulse frequency measurement mode.

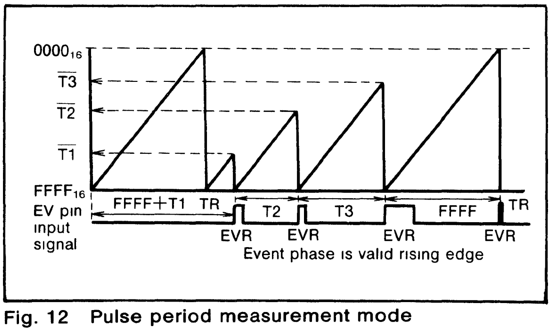
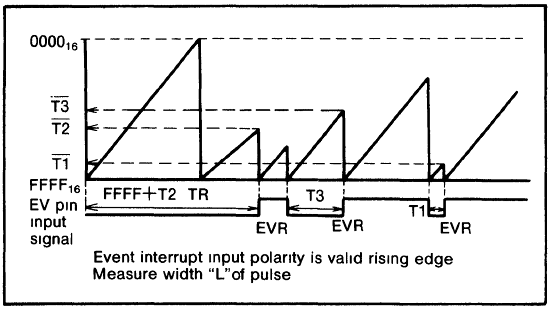


Fig. 12 Pulse period measurement mode

(5) Pulse Width Measurement Mode [100]

This mode measures the pulse width while the EVi pin input signal is "H" or "L".

Whether to measure the "H" or "L" interval is determined by the event input polarity selection bit. If this bit is "0", the count source selected with the count source selection bit is counted while the input pulse is "H". If it is "1", the count source is counted while the input pulse is "L". A 1's complement of the timer value is stored in the timer latch for a valid edge on the EVi pin input. In addition, the timer value is set to $FFFF_{16}$ for an edge (both rise and fall) on the EVi pin input. Figure 13 shows the timer operation during pulse width measurement mode.



Event interrupt input polarity is valid rising edge
Measure width "L"of pulse

Fig. 13 Pulse width measurement mode

In pulse period measurement mode [011] and pulse width measurement mode [100], an EVi interrupt request is issued at the valid edge selected by the event phase selection bit. That is, an interrupt occurs at the end of the pulse period measurement or pulse width measurement. Also, when a timer overflow occurs, the count continues from $FFFF_{16}$ without the value of the timer latch being loaded in the timer.

Write to timer latch is inhibited in these modes. Furthermore, EVi interrupt is disabled during STP instruction execution.

(6) Programmable Waveform Generation Mode [101]

In this mode, the level set in the output level latch of the timer i control register is output to the EVi pin every time the timer overflows.

The timer counts the source selected by the count source selection bit and when it overflows, the value in the timer latch is loaded in the timer.

After it overflows, the value of the output level latch and the timer latch can be modified to generate any waveform from the EVi pin.

Figure 14 shows the timer operation during programmable waveform generation mode.

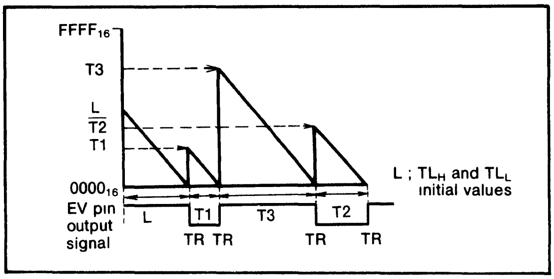


Fig. 14 Programmable waveform generation mode

(7) Programmable One-shot Generation Mode [110]

This mode uses the INTi pin input signal as a trigger and counts by writing the value of the timer latch in the timer.

The output level of the EVi pin goes "H" when the trigger is issued and goes "L" when the timer overflows.

The EVi pin level is initialized to "L" when this mode is selected.

The timer count souce is set to $f(X_{IN})$ divided by four regardless of the count source selection bit.

A valid edge of the INTi pin input trigger signal is determined by the INTi phase selection bit of MISRG1 ($00DE_{16}$). Figure 15 shows the timer operation during programmable one-shot generation mode.

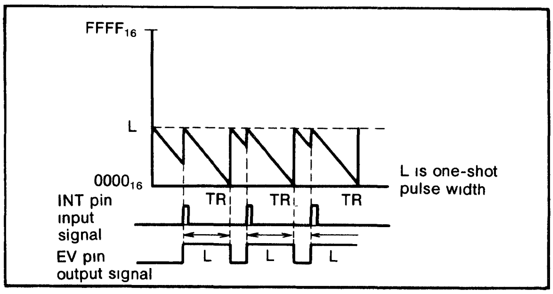


Fig. 15 Programmable one-shot generation mode

When the INTi pin input signal is selected as the count source for pulse output mode [010], pulse period measurement mode [011], pulse width measurement mode [100], and programmable waveform generation mode [101], the "H" and "L" pulse width of the input signal must not be less than $(6/f(X_{IN}))+100ns$.

SERIAL I/O

Serial I/O can operate in either clock synchronous or clock asynchronous (UART) mode. An exclusive baud rate generation timer (baud rate generator) is provided for serial I/O operation. Figure 16 shows the structure of the registers used for serial I/O.

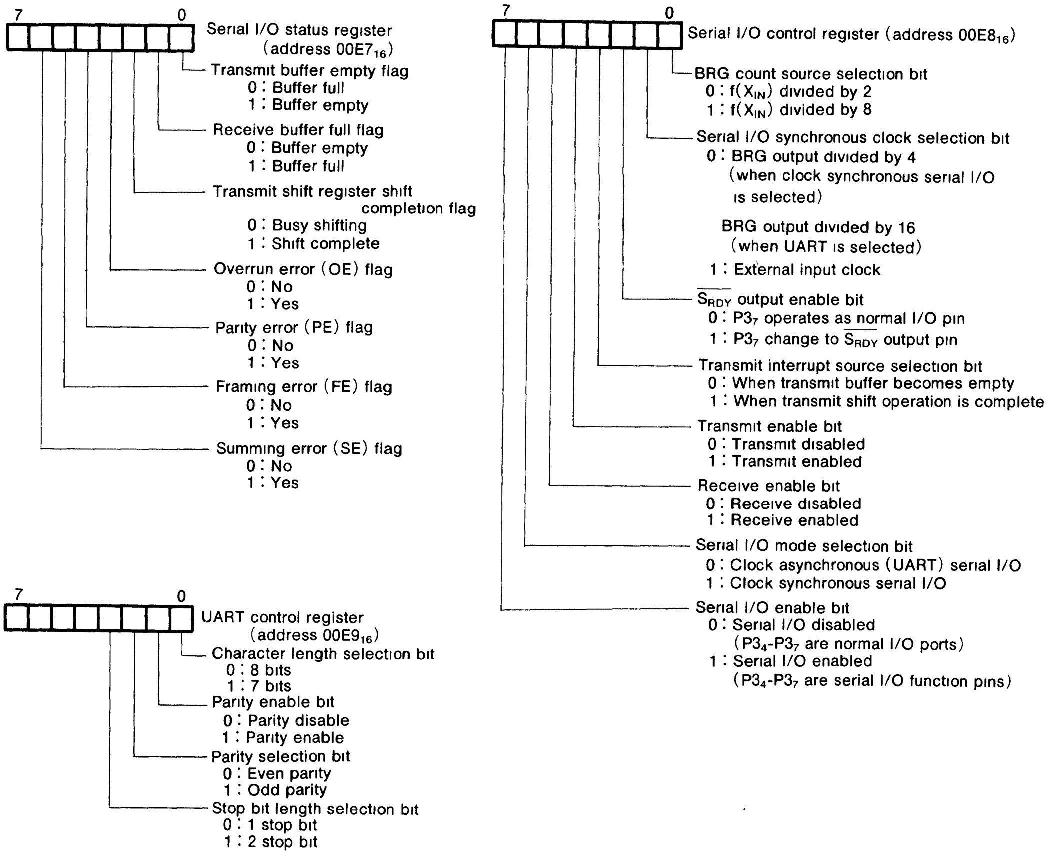


Fig. 16 Structure of registers related to serial I/O

(1) Clock Synchronous Serial I/O

Clock synchronous serial I/O is selected by setting the mode selection bit of the serial I/O control register to "1". Figure 17 shows a block diagram of clock synchronous serial I/O and Figure 18 shows its operation.

With clock synchronous serial I/O, the same clock is used as the operating clock between the transmitting and receiving microcomputers. If an internal clock is used for operating clock, transmit/receive is started by writing a signal in the transmit/receive buffer register.

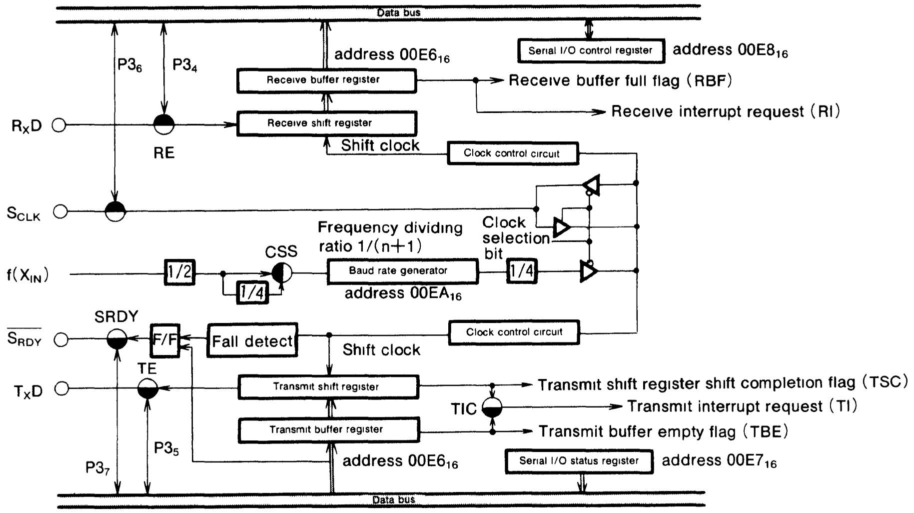
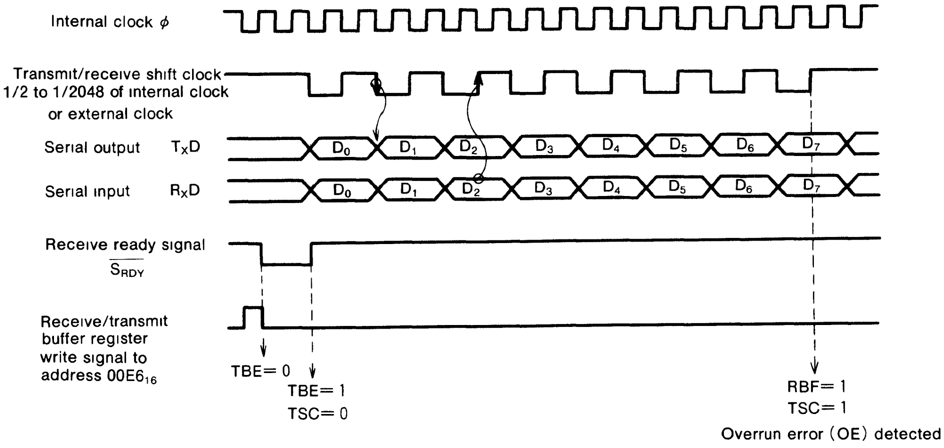


Fig. 17 Clock synchronous serial I/O block diagram



Note 1. Use the transmit interrupt source selection bit (TIC) in the serial I/O control register to specify whether to generate a transmit interrupt (TI) when the transmit buffer becomes empty (TBE=1) or when transmit shift operation completes (TSC=1)
2. If data is written in the transmit buffer register when TSC=0, transmit clock is generated continuously and serial data is output continuously from the T_XD pin
3. The receive interrupt (RI) is set when the receive buffer full flag (RBF) is set
4. This example shows the case that the BRG count source is $f(X_{IN})/2$ and the contents of BRG reload latch is "00_{16}"
5. If the transmit enable bit (TE) goes from "0" to "1" when the serial I/O enable bit is at "1", the TxD pin goes to "H" level After the TxD has transmitted serial data, it is held at the "D_7" level of the final bit of the last data to be transmitted until the next serial data is transmitted

Fig. 18 Clock synchronous serial I/O operation

(2) Clock Asynchronous Serial I/O (UART)

UART is selected by setting the mode selection bit of the serial I/O control register to "0". Figure 19 shows a block diagram of UART and Figure 20 shows its operation.

With the M37451, one of eight serial data transmission formats can be selected with the UART control register as shown in Figure 16. The transmission format must be agreed upon between the transmit side and the receive side.

The transmit shift register and the receive shift register has its buffer register respectively to perform serial data transfer (same memory addresses).

Data cannot be written or read directly to/from the shift registers. Therefore, the data to be transmitted is written to a buffer register and the received data is read from a buffer register. The buffer registers can also be used to store data to be transmitted next or to receive 2-byte data consecutively.

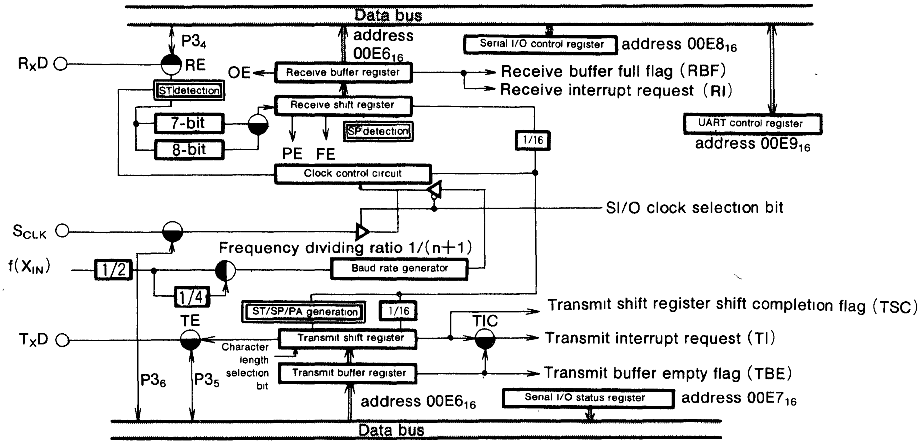
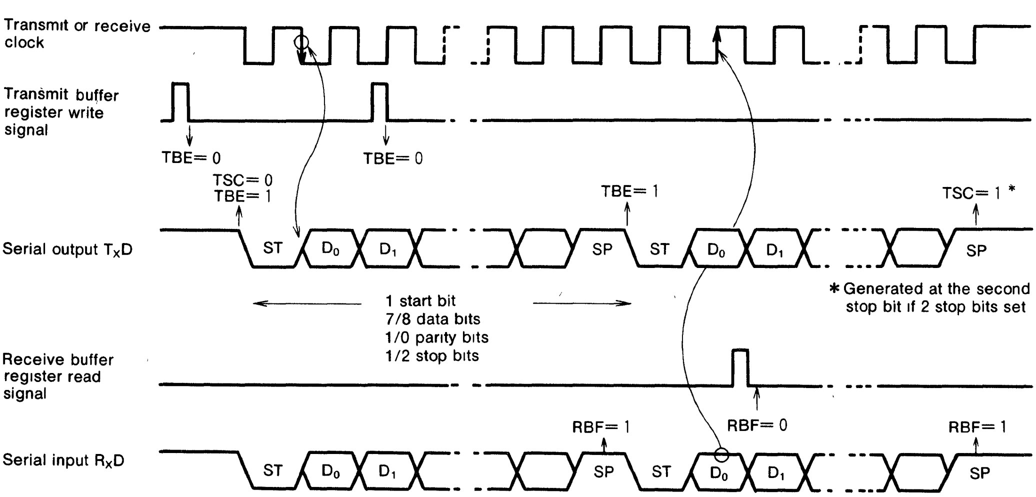


Fig. 19 UART serial I/O block diagram



Note 1. Error flag detection is performed as soon as RBF=1 (first stop bit for receive)
2. Transmit interrupt (TI) is set to either TBE=1 or TSC=1 according to the transmit interrupt source selection bit (TIC) in the serial I/O control register
3. Receive interrupt (RI) is set by RBF=1.

Fig. 20 UART serial I/O operation

[Serial I/O control register] SIOCON

The serial I/O control register is an 8-bit register consisting of selection bits for controlling the serial I/O function.

- **Serial I/O enable bit SIOE**

When this bit is set to "1", serial I/O is enabled and pins $P3_4$-$P3_7$ can be used as serial I/O function pins.

- **Serial I/O mode selection bit SIOM**

This bit is used to select the serial I/O operation mode. When this bit is "0", asynchronous serial I/O (UART), which transfers data using start and stop bits, is selected. When it is "1", clock synchronous serial I/O which performs transmission and receive using the same clock is selected.

- **Receive enable bit RE**

Receive operation is enabled when this bit is set to "1" and pin $P3_4$ becomes a serial data input pin.

- **Transmission enable bit TE**

Transmission operation is enabled when this bit is set to "1". Pin $P3_5$ becomes a serial data output pin and shift data is output.

- **Transmission interrupt source selection bit TIC**

This bit is used to selelct events that can cause a transmission interrupt.

- **S_{RDY} output enable bit SRDY**

If this bit is set to "1" when clock synchronous serial I/O is selected, pin $P3_7$ becomes an $\overline{S_{RDY}}$ signal output pin and $\overline{S_{RDY}}$ signal is output.

When an external clock is used during clock synchronous serial I/O, the $\overline{S_{RDY}}$ signal is used to notify the clock sender that it can send the serial clock signal. It goes "L" when data is written in the transmit/receive buffer register and goes "H" at the first fall of the receive clock. When using the $\overline{S_{RDY}}$ signal, the transmission enable bit must be set to "1" even when performing receive only.

- **Serial I/O synchronous clock selection bit SCS**

When this bit is "1", pin $P3_6$ becomes an input pin and the external clock input from the S_{CLK} pin is selected as the serial I/O synchronous clock. When this bit is "0", the baud rate generator (BRG) overflow signal is selected as the serial I/O synchronous clock. Also, when this bit is "0" during clock synchronous serial I/O, pin $P3_6$ becomes an output pin and the shift clock is output from the S_{CLK} pin.

When clock synchronous serial I/O is selected, the baud rate generator (BRG) output signal divided by four or an external clock input is used. When UART is selected, the BRG output signal divided by sixteen or an external clock input signal divided by sixteen is used.

- **BRG count source selection bit CSS**

The baud rate generator is an 8-bit counter with a reload register. By setting a value n in the BRG register (address $00EA_{16}$), the count source selected by the BRG count source selection bit is divided by $(n+1)$.

[UART control register] UARTCON

The UART control regsiter is a 4-bit register consisting of control bits that are valid when UART is selected. The content of this register is used to set the data format for serial data transmission/receiving.

- **Character length selection bit CHAS**

This bit is used to select the transmission/receiving character length.

- **Parity enable bit PARE**

When this bit is set to "1", a parity bit is added next to the most significant bit (MSB) of the transmission data and parity is checked during receive.

- **Parity selection bit PARS**

This bit is used to specify the type of parity to be generated during transmission and checked when data is received. The number of 1's in the data is set to even or odd according to this bit.

- **Stop bit length selection STPS**

This bit is used to determine the number of stop bits to be used during transmission.

[Serial I/O status register] SIOSTS

The serial I/O status register is a 7-bit read only register consisting of serial I/O operation status flags and error flags. Bits 4 to 6 are valid only during UART mode.

All bits of this register are initialized to "0" at reset, and when the transmit enable bit in the serial I/O control register is set to "1", bits "0" and "2" change to "1".

- **Transmission buffer empty flag TBE**

This bit is cleared to "0" when transmission data is written in the transmission buffer register and set to "1" when that data is transferred to the transmit shift register. It is also cleared when TE=0.

- **Receive buffer full flag RBF**

When receiving serial data, data is transferred to the receive buffer register and this bit is set to "1" when the receive shift register completes receiving a data byte. This bit is cleared when the data is read. This bit is also cleared when RE=0.

- **Transmit shift register shift completion flag TSC**

This bit is cleared to "0" when the data in the transmission buffer register is transferred to the transmit shift register and set to "1" when data shift completes. It is also set to "1" when TE=0.

- **Overrun error flag OE**

When continuously receiving serial data, this bit is set when the next data fill the receive shift register before the data in the receive buffer register has been read

- **Parity error flag PE**

When receiving serial data with parity, this bit is set to "1 " if the parity of the received data differs from the specified parity.

· Framing error flag FE
This bit is set to "1" when there is no stop bit when transferring data from the receive shift register to the receive buffer.

· Summing error flag SE
This bit is set when either overrun, a parity, or a framing error occurs.

Tests for these errors are performed as soon as the data is transferred from the receive shift register to the receive buffer register and at the same time the receive buffer full flag is set. The error flags (OE, PE, FE, and SE) are cleared when any data is written in the serial I/O status register. Also, all status flags including error flags are cleared when SIOE=0.

Usage cautions

(1) To reset the serial I/O control register
Reset the serial I/O control register after disabling the transmit and receive enable bits that were enabled at that point and resetting the transmit and receive circuits. If the serial I/O control register is reset without resetting the other items, the settings will not operate correctly.

(2) Transmit and receive interrupt requests when transmit and receive enable bits are set.
Setting the transmit and receive enable bits to "1" sets the receive buffer empty flag and the transmit shift register shift completion flag to "1". Therefore, an interrupt request is generated and the transmit interrupt request bit is set, regardless of which timing is selected for the generation of transmit interrupts.
If interrupts of this timing are not used, first clear the transmit interrupt enable bit to "0" (disabled status), set the transmit enable bit, then clear the transmit interrupt request bit again after executing one instruction (e. g., the NOP instruction). Finally, set the transmit interrupt enable bit to "1" (enabled status).

(3) To disable transmission after one byte of data has been transmitted.
The method used in the M37451 to post the completion of data transmission is to reference the transmit shift register shift completion flag (TSC flag). The TSC flag is cleared to "0" while data is being transmitted, and it is set to "1" when the data transmission is completed. Therefore, if transmission is disabled after it has been confirmed that the TSC flag has been set, transmission can be forced to end after one byte of data is transmitted.
However, the TSC flag can also be set by enabling serial I/O, but it is not cleared by shift clock generation and transmission start (after data has been transferred from the transmit buffer to the transmit shift register, after 0.5 to 1.5 cycles of the shift clock), so if the TSC flag is referenced and transmission is disabled at this point, data will not be transmitted. Make sure that the TSC flag is referenced after transmission has started.

BUS INTERFACE

The M37451 is equipped with a bus interface that is functionally similar to the MELPS 8-41 series. Its operation can be controlled with control signals from the host CPU (slave mode).

The M37451 bus interface can be connected directly to either a R/$\overline{W}$ type CPU or separate $\overline{RD}$, $\overline{WR}$ type CPU. Figure 21 shows a block diagram of the bus interface function.

Slave mode is selected with MISRG2 (address $00DF_{16}$) bit 2 and 3 as shown in Figure 22.

An input buffer full interrpt occurs when data is received from the host CPU and an output buffer empty interrupt occurs when data is read by the host CPU.

In slave mode, ports $P5_0$-$P5_7$ become a tri-state data bus used to transfer data, commands, and status to and from the host CPU.

Furthermore, ports $P6_4$-$P6_7$ become host CPU control signal input pins and $P6_3$ becomes a slave status output pin.

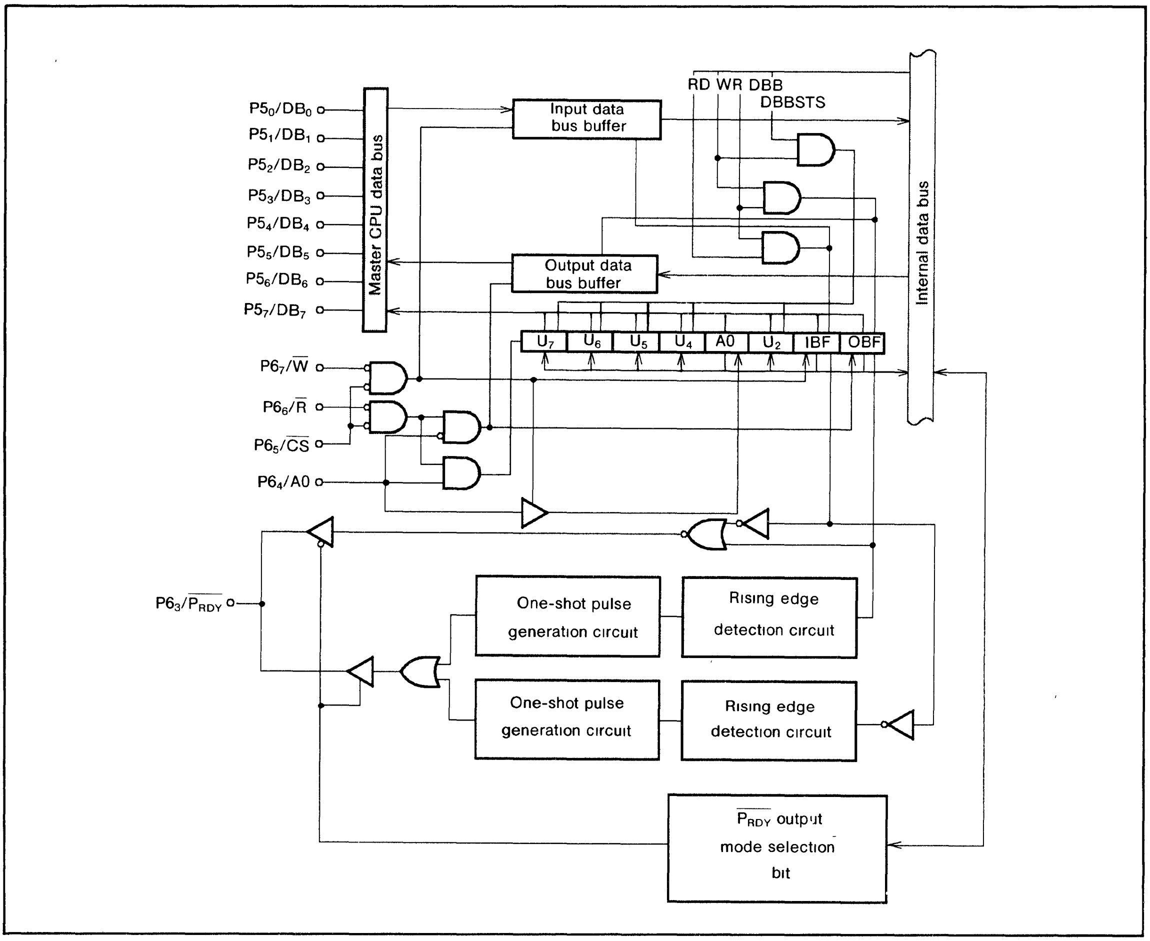


Fig. 21 Bus interface circuit diagram

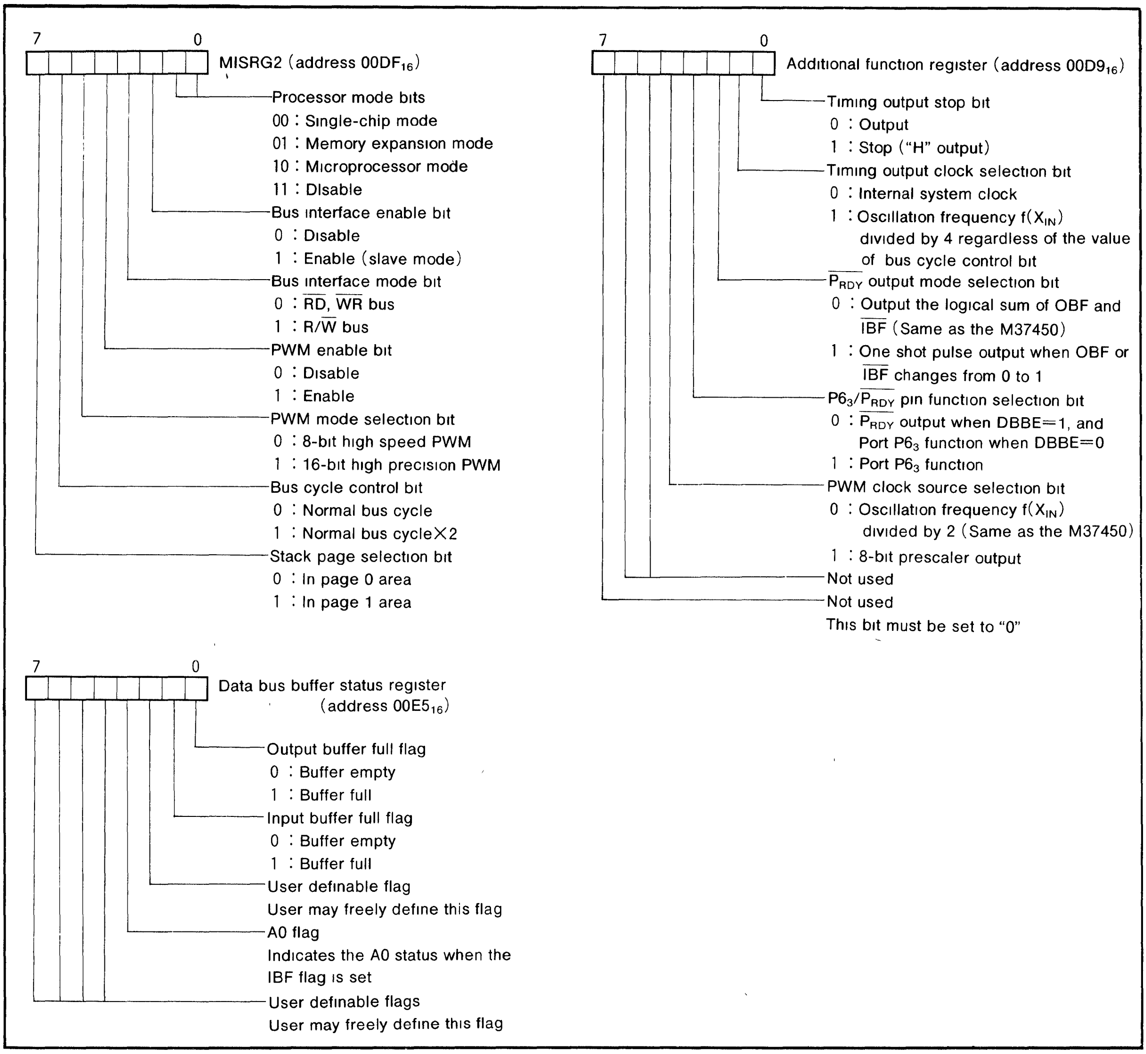


Fig. 22 Structure of bus interface relation registers

[Data bus buffer status register] DBBSTS

This is an 8-bit register. Bits 0, 1, and 3 are read-only bits indicating the status of the data bus buffer. Bits 2, 4, 5, 6, and 7 are read/write enabled user-definable flags that can be set with a program. The host CPU can only read these flags by setting the A0 pin to "H".

- **Output buffer full flag OBF**

This flag is set when data is written in the output data bus buffer and cleared when the host CPU reads the data in the output data bus buffer. When the $\overline{P_{RDY}}$ output mode selection bit is "0", OBF is initialized to "1" only at reset and is cleared to "0" by setting the bus interface enable bit to "1". In this case, OBF is set to "1" when the bus interface enable bit changes from "1"(enable) to "0"(disable). But when the bus interface enable bit is set to "1" again, it is set to the value directly before clearing the bus interface enable bit. When the $\overline{P_{RDY}}$ output mode selection bit is "1", OBF is initialized to "1" when the bus interface enable bit is cleared to "0" or reset.

In this case, OBF is set to "1" by clearing the bus interface enable bit and it is cleared to "0" by setting the bus interface enable bit.

- **Input buffer full flag IBF**

This flag is set when the host CPU writes data in the input data bus buffer and cleared when the slave CPU reads the data in the input data bus buffer. When the $\overline{P_{RDY}}$ output mode selection bit is "0", IBF is initialized to "0" only at reset.

When the $\overline{P_{RDY}}$ output mode selection bit is "1", IBF is initialized to "0" when the bus interface enable bit is cleared to "0" or reset.

A0 Flag

The level of the A0 pin is latched when the host CPU writes data in the input data bus buffer.

[Input data bus buffer] DBBIN

Data on the data bus is latched in DBBIN when there is a write request from the host CPU. The data in DBBIN can be read from the data bus buffer register (SFR address $00E4_{16}$).

[Output data bus buffer] DBBOUT

Data is written in DBBOUT by writing data in data bus buffer register (SFR address $00E4_{16}$). The data in DBBOUT is output to the data bus (P5) when the host CPU issues a read request with setting the A0 pin to "L".

Table 2. Control I/O pin functions when bus interface function is selected

Pin	Name	Bus interface mode bit	$\overline{P_{RDY}}$ output mode selection bit	$P6_3/\overline{P_{RDY}}$ pin function selection bit	Input/ Output	Function
$P6_3$	$\overline{P_{RDY}}$	—	0	0	Output	Status output The NOR of OBF and $\overline{IBF}$ is output
				1	I/O	Port $P6_3$ function
			1	0	Output	Status output Normally output "0" One shot pulse whose length is half of a period of internal system clock ϕ is output, when OBF or $\overline{IBF}$ changes from "0" to "1" (See Fig 23)
				1	I/O	Port $P6_3$ function
$P6_4$	A0	—	—	—	Input	Address input Used to select between DBBSTS and DBBOUT during host CPU read Also used to identify commands and data during write
$P6_5$	$\overline{CS}$	—	—	—	Input	Chip select input Used to select the data bus buffer Select when "L"
$P6_6$	$\overline{R}$	0	—	—	Input	Timing signal used by the host CPU to read data from the data bus buffer
	E	1	—	—	Input	Inputs a timing signal E or inverse of ϕ
$P6_7$	$\overline{W}$	0	—	—	Input	Timing signal used by the host CPU to write data to the data bus buffer
	$R/\overline{W}$	1	—	—	Input	Input $R/\overline{W}$ signal used to control the data transfer direction When this signal is "L", data bus buffer write is synchronized with the E signal When it is "H", data bus buffer read is synchronized with the E signal

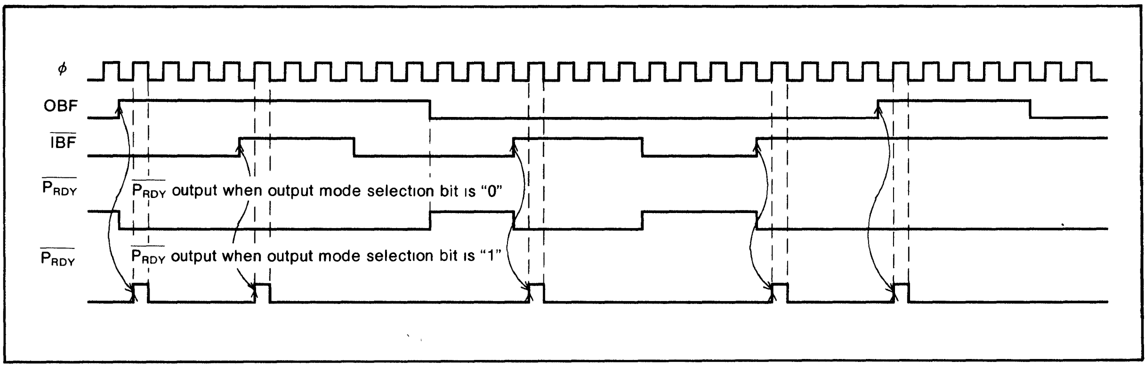


Fig. 23 Output status of $\overline{P_{RDY}}$ pin

PWM

The PWM generator has two program-selectable modes; the high-speed mode (8-bit resolution) and the high-precision mode (16-bit resolution).

Also two clocks listed below can be selected as the count clock of each PWM mode.

- Oscillation frequency $f(X_{IN})$ divided by 2
- 8-bit prescaler output (The count source of prescaler is oscillation frequency $f(X_{IN})$ divided by 2)

Figure 26 shows a block diagram of PWM.

The count clock of PWM can be selected by the PWM clock source selection bit of additional function register (address $00D9_{16}$). And the register MISRG2 (address $00DF_{16}$) is used to enable/disable the PWM and change its mode. When the PWM enable bit is set, the PWM generator starts from its initial state.

When PWM clock source selection bit is "0", as shown in Figure 24, the output period is fixed.

In high-speed mode

$(2 \times 255)/f(X_{IN})$ 40.8μs at $f(X_{IN})=12.5$MHz

In high-precision mode

$(2 \times 65535)/f(X_{IN})$ 10.4856ms at $f(X_{IN})=12.5$MHz

When PWM clock source selection bit is "1", as shown in Figure 25, the output period can be changed by setting the value to prescaler latch (address $00D8_{16}$).(Note)

In high-speed mode

$\{2(n+1) \times 255\}/f(X_{IN})$ 40.8$(n+1)\mu$s at $f(X_{IN}) = 12.5$MHz

In high-precision mode

$\{2(n+1) \times 65535\}/f(X_{IN})$ 10.4856$(n+1)$ms at $f(X_{IN}) = 12.5$MHz

n : Set value to prescaler latch

The "H" width of the output pulse is determined by setting a value only in the PWM_L register for high-speed mode and in both the PWM_H and PWM_L in this order for high-precision mode.

If the value set in the PWM register is m, the "H" width of the output pulse is

(PWM period$\times$m)/255 for high-speed mode and

(PWM period$\times$m)/65535 for high-precision mode.

Note : Address $00D8_{16}$ functions as port P4 register (read only) when read, and functions as PWM prescaler latch (write only) when write. So the value of PWM prescaler can not be read out.

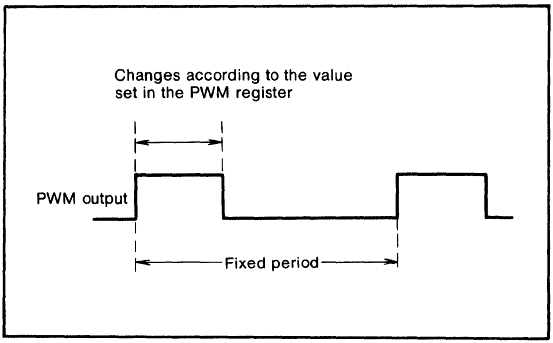


Fig. 24 PWM output (when PWM clock source selection bit is "0")

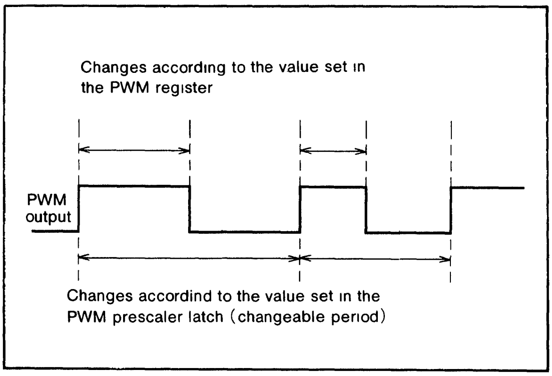


Fig. 25 PWM output (when PWM clock source selection bit is "1")

Notes on PWM start

(1) Notes on PWM start

PWM starts after the PWM enable bit is set to enable and "L" level is output from the PWM_{OUT} pin. The length of this "L"-level output is as follows:

If the PWM prescaler is not used (PWM clock source selection bit=0): 1/2 clock cycle

If the PWM prescaler is used (PWM clock source selection bit=1): (1+n)/2 clock cycle (where n is the value set in the prescaler)

(2) Notes on PWM restart (only when PWM clock source selection bit is "1")

If the PWM enable bit is set to enabled, then to disabled, then back to enabled, temporarily clear the PWM clock source selection bit to "0" then reset it to "1" to re-enable PWM.

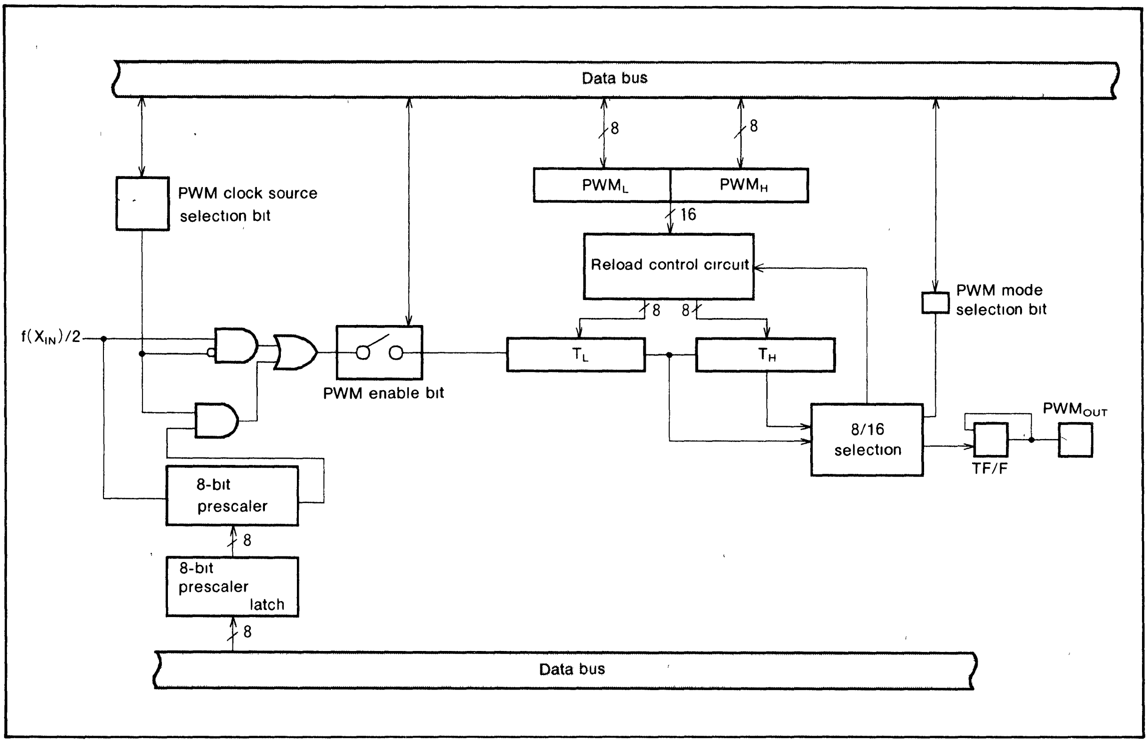


Fig. 26 PWM generator block diagram

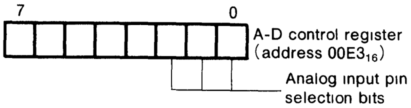
A-D CONVERTER

An A-D converter is an 8-bit successive approximation method. Figure 28 shows a block diagram of the A-D converter.

The 64-pin model has three analog voltage input pins; the 80-pin model has eight.

A-D conversion is started by a write operation to the analog input pin selection bit of the A-D control register shown in Figure 27 and by selecting the analog voltage input pin. The A-D interrupt request bit in the interrupt request register 2 is set when A-D conversion completes. The result of A-D conversion is stored in the A-D register.

The contents of the A-D register must not be read during A-D conversion and $f(X_{IN})$ must be no less than 1 MHz during A-D conversion.



	b2	b1	b0	
64 pin model	0	0	0	: AN$_0$
	0	0	1	: AN$_1$
	0	1	0	: AN$_2$
	0	1	1	: AN$_3$
	1	0	0	: AN$_4$
	1	0	1	: AN$_5$
	1	1	0	: AN$_6$
	1	1	1	: AN$_7$

Note : Do not select pins other than AN$_0$-AN$_2$ with the 64-pin model

Fig. 27 Structure of A-D control register

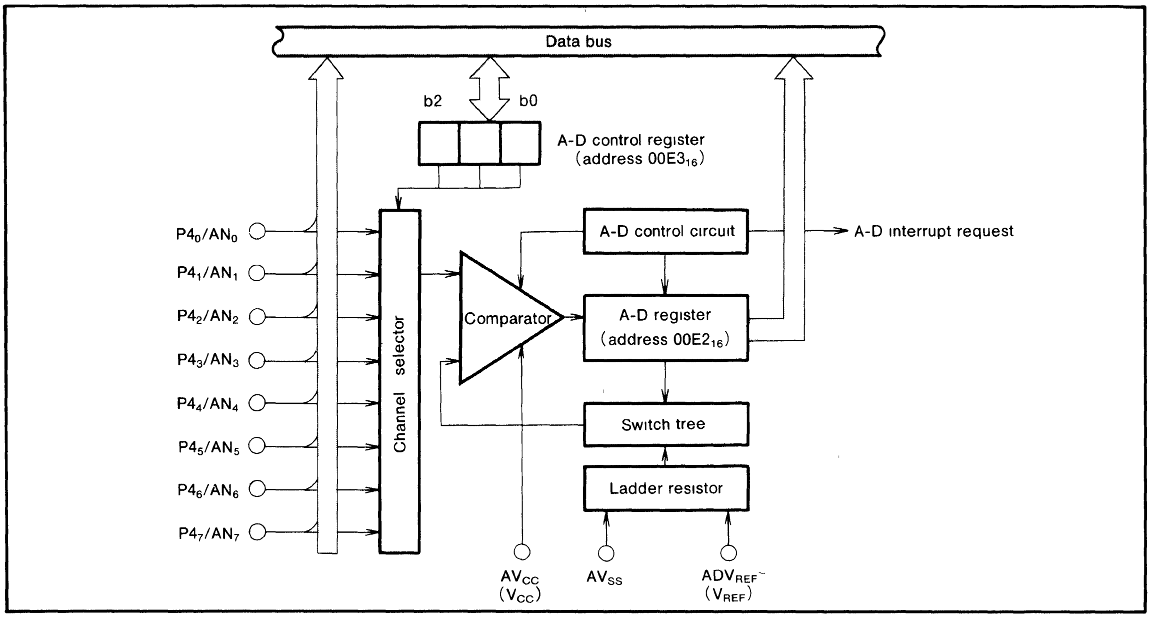


Fig. 28 A-D converter block diagram

D-A CONVERTER

Two 8-bit resolution D-A converter channels are provided. Figure 29 shows a block diagram of the D-A converter.

D-A conversion is performed by setting a value in the D-Ai register (addresses 00E0$_{16}$ and 00E1$_{16}$). The result of D-A conversion is output from the D-Ai output pin.

The output analog voltage V_{DA} is determined by the value n (decimal) set in the D-Ai register as follows:

$V_{DA}=DAV_{REF}{}^{*}\times n/256$

$*V_{REF}$ for 64-pin model.

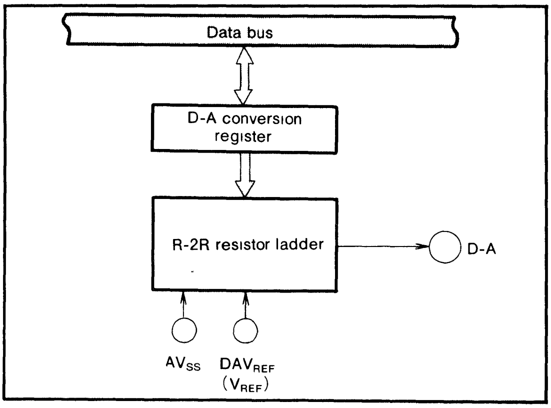


Fig. 29 D-A converter block diagram

RESET CIRCUIT

The M37451 is reset according to the sequence shown in Figure 30. It starts the program from the address formed by using the content of address FFFF$_{16}$ as the high order address and the content of the address FFFE$_{16}$ as the low order address, when the $\overline{\text{RESET}}$ pin is held at "L" level for no less than 8 clock cycles while the power voltage is 5V± 10% and the crystal oscillator oscillation is stable and then returned to "H" level. The internal initializations following reset are shown in Figure 30.

An example of the reset circuit is shown in Figure 31. The reset input voltage must be kept below 0.6V until the supply voltage surpasses 4.5V.

		address								
(1)	Port P0 directional register	00D1$_{16}$	00$_{16}$							
(2)	Port P1 directional register	00D3$_{16}$	00$_{16}$							
(3)	Port P2 directional register	00D5$_{16}$	00$_{16}$							
(4)	Port P3 directional register	00D7$_{16}$	00$_{16}$							
(5)	Additional function register	00D9$_{16}$	0			0	0	0	0	0
(6)	Port P5 directional register	00DB$_{16}$	00$_{16}$							
(7)	Port P6 directional register	00DD$_{16}$	00$_{16}$							
(8)	MISRG1	00DE$_{16}$		0	0	0		0	0	0
(9)	MISRG2	00DF$_{16}$	0	0	0	0	0	0	CM1	0
(10)	D-A1 register	00E0$_{16}$	00$_{16}$							
(11)	D-A2 register	00E1$_{16}$	00$_{16}$							
(12)	Data bus buffer status register	00E5$_{16}$							0	1
(13)	Serial I/O status register	00E7$_{16}$		0	0	0	0	0	0	0
(14)	Serial I/O control register	00E8$_{16}$	00$_{16}$							
(15)	UART control register	00E9$_{16}$					0	0	0	0
(16)	Timer 1 control register	00ED$_{16}$			0	0	0	0	0	0
(17)	Timer 2 control register	00EE$_{16}$			0	0	0	0	0	0
(18)	Timer 3 control register	00EF$_{16}$			0	0	0	0	0	0
(19)	Timer 1 register (low order)	00F0$_{16}$	FF$_{16}$							
(20)	Timer 2 register (high order)	00F1$_{16}$	03$_{16}$							
(21)	Interrupt request register 1	00FC$_{16}$	00$_{16}$							
(22)	Interrupt request register 2	00FD$_{16}$			0	0	0	0	0	0
(23)	Interrupt control register 1	00FE$_{16}$	00$_{16}$							
(24)	Interrupt control register 2	00FF$_{16}$			0	0	0	0	0	0
(25)	Processor status register	(PS)						1		
(26)	Program counter	(PC$_H$)	Contents of address FFFF$_{16}$							
		(PC$_L$)	Contents of address FFFE$_{16}$							

Note 1 Since the contents of both registers other than those listed above (including timer 1, timer 2, timer 3, and the serial I/O register) and the RAM are undefined at reset, it is necessary to set initial values

2 The initial value of CM1 depends on the level on the CNV$_{SS}$ pin

Fig. 30 Internal state of microcomputer at reset

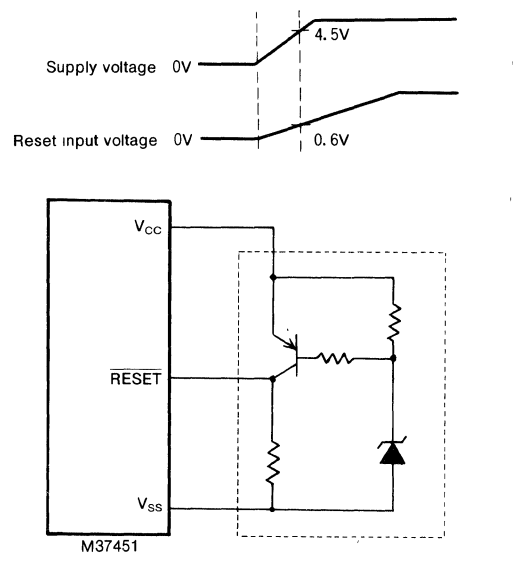
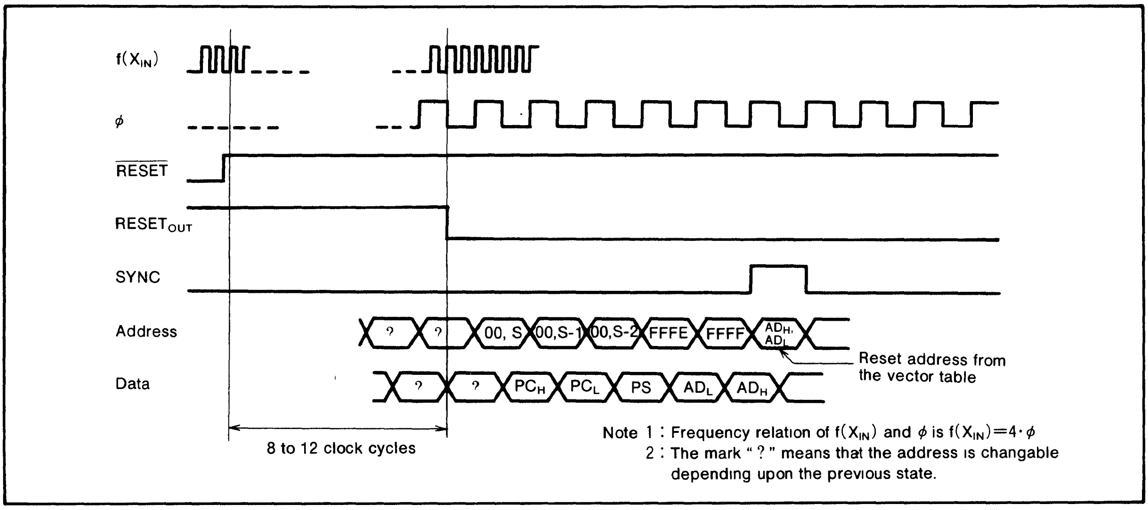


Fig. 31 Example of reset circuit



Note 1 : Frequency relation of $f(X_{IN})$ and ϕ is $f(X_{IN})=4\cdot\phi$
2 : The mark " ? " means that the address is changable depending upon the previous state.

Fig. 32 Timing diagram at reset

I/O PORTS

(1) Port P0

Port P0 is an 8-bit I/O port with CMOS output.

As shown in the memory map (Figure 3), port P0 can be accessed at zero page memory address $00D0_{16}$.

Port P0 has a directional register (address $00D1_{16}$) which can be used to program each individual bit as input ("0") or as output ("1"). If the pins are programmed as output, the output data is latched to the port register and then output. When data is read from the output port the output pin level is not read, only the latched data in the port register is read. This allows a previously ouptut value to be read correctly even though the output voltage level is shifted up or down. Pins set as input are in the floating state and the signal levels can thus be read When data is written into the input port, the data is latched only to the port latch and the pin still remains in the floating state.

Depending on the contents of the processor status register (bit 0 and bit 1 at address $00DF_{16}$), three different modes can be selected; single-chip mode, memory expansion mode and microprocessor mode.

In these modes it functions as address (A_7-A_0) output port (excluding single-chip mode). For more details, see the processor mode information

(2) Port P1

In single-chip mode, port P1 has the same function as port P0. In other modes, it functions as address (A_{15}-A_8) output port.

Refer to the section on processor modes for details.

(3) Port P2

In single-chip mode, port P2 has the same function as port P0. In other modes, it functions as data (D_0-D_7) input/output port. Refer to the section on processor modes for details.

(4) Port P3

Port P3 is an 8-bit I/O port with function similar to port P0. All pins have program selectable dual functions. When a serial I/O function is selected, the input and output from pins $P3_4$-$P3_7$ are determined by the contents of the serial I/O registers.

This port is unaffected by the processor mode.

(5) Port P4

This is an input-only port and may be used as an analog voltage input port. The number of ports is different for the 64-pin model and 80-pin model The 64-pin model has three ports and the 80-pin model has eight ports.

(6) Port P5

This is an 8-bit I/O port with function similar to port P0. When slave mode is selected with a program, all ports change to the data bus for the master CPU. In this case, port input/output is unaffected by the directional register

This port is unaffected by the processor mode register.

(7) Port P6

This is an 8-bit input/output port with function similar to port P0.

When slave mode is selected with a program, ports $P6_3$-$P6_7$ change to the control bus for the bus interface function. In this case, port input/output is unaffected by the directional register.

Ports $P6_0$-$P6_2$ are shared with the external interrupt input pins (INT_1-INT_3). The INT interrupt constantly monitors the status of this port and generates an interrupt at a valide edge. Therefore, if the INT interrupt is not used, it must be disabled and if it is used, this port must be set to input.

(8) Port D-A

Port D-A consists of two analog voltage output pins. Any analog voltage can be generated by setting a value in the D-A register.

(9) ϕ pin

The ϕ pin normally outputs the internal system clock (the oscillation frequency of the resonator connected between the X_{IN} and X_{OUT} pins, divided by four).

The timing clock output from the ϕ pin is in output mode if the timing output stop bit (bit 0 of address $00D9_{16}$) is set to "0", and in stop mode if that bit is set to "1" and the timing clock output is "H".

If the timing output clock selection bit (bit 1 of address $00D9_{16}$) is set to "0" when the timing output stop bit is "0" (timing output is being output), the internal system clock that is output from the ϕ pin is the oscillation frequency divided by four if the bus cycle control bit is "0", or the oscillation frequency divided by eight if that bit is "1". If the timing output clock selection bit is "1", the bus cycle control bit is ignored — the clock that is output is the oscillation frequency divided by four. (See Fig. 33)

(10) SYNC pin

This pin outputs a signal that is "H" during one cycle of the ϕ during operation code fetch.

(11) R/$\overline{W}$ pin

This is a control signal output pin that indicates the local bus direction in memory expansion and microprocessor modes.

(12) $\overline{RD}$, $\overline{WR}$ pins

These are local bus write and read timing signal output pins for memory expansion and microprocessor modes.

A signal equivalent to the signal otuput from the R/$\overline{W}$ separated by the ϕ signal is output.

These pins are used exclusively by the 80-pin model.

(13) $RESET_{OUT}$ pin

This pin goes "H" while the microprocessor is being reset. It can be used as a reset signal output pin for peripheral devices.

This pin is used exclusively by the 80-pin model.

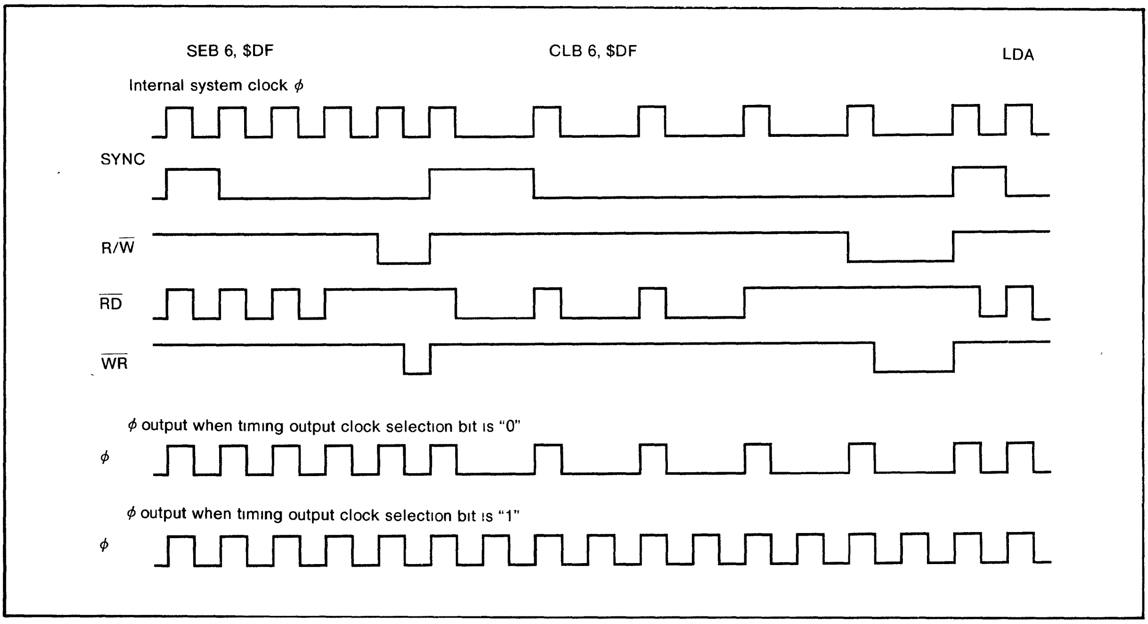


Fig. 33 Output from ϕ pin

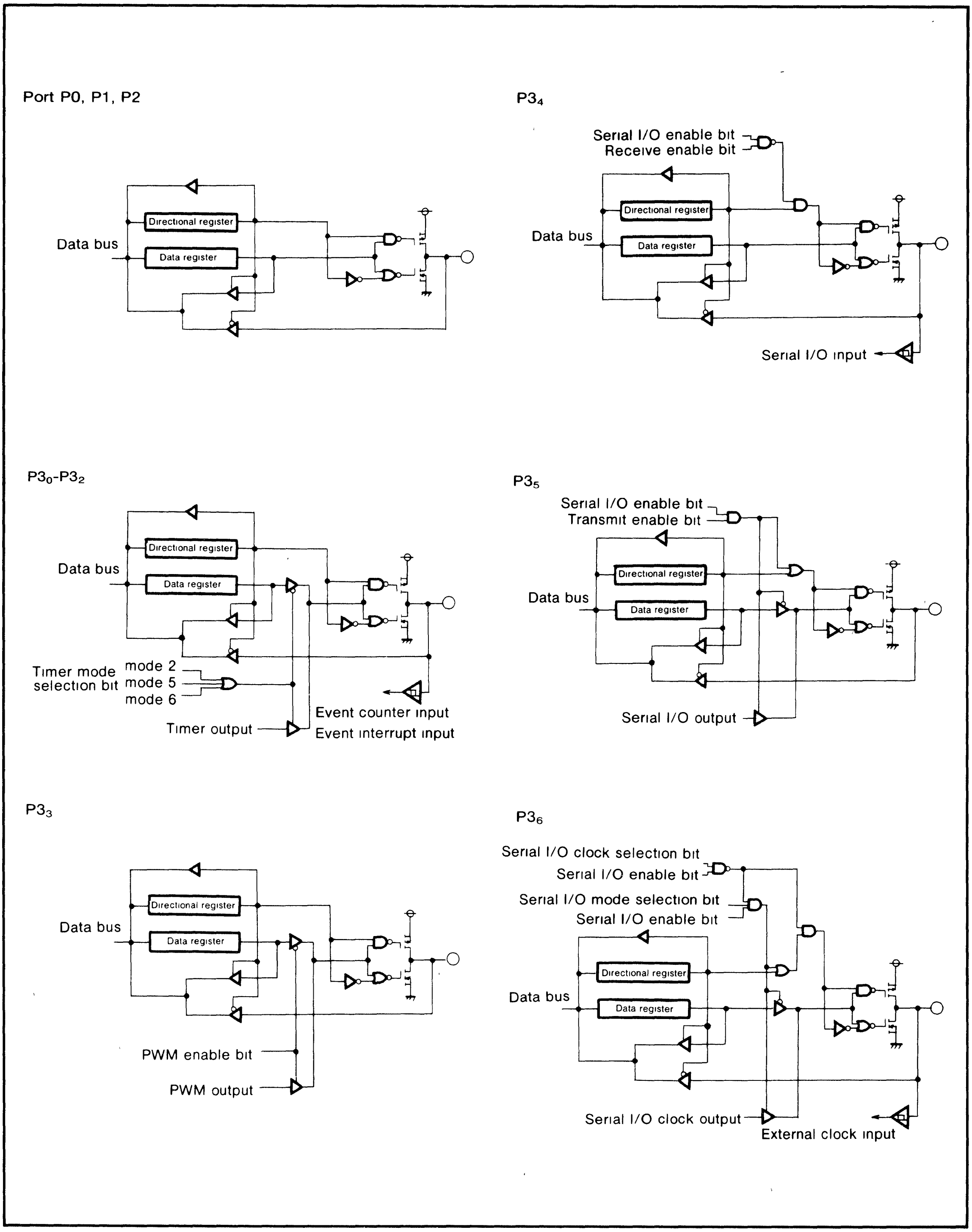
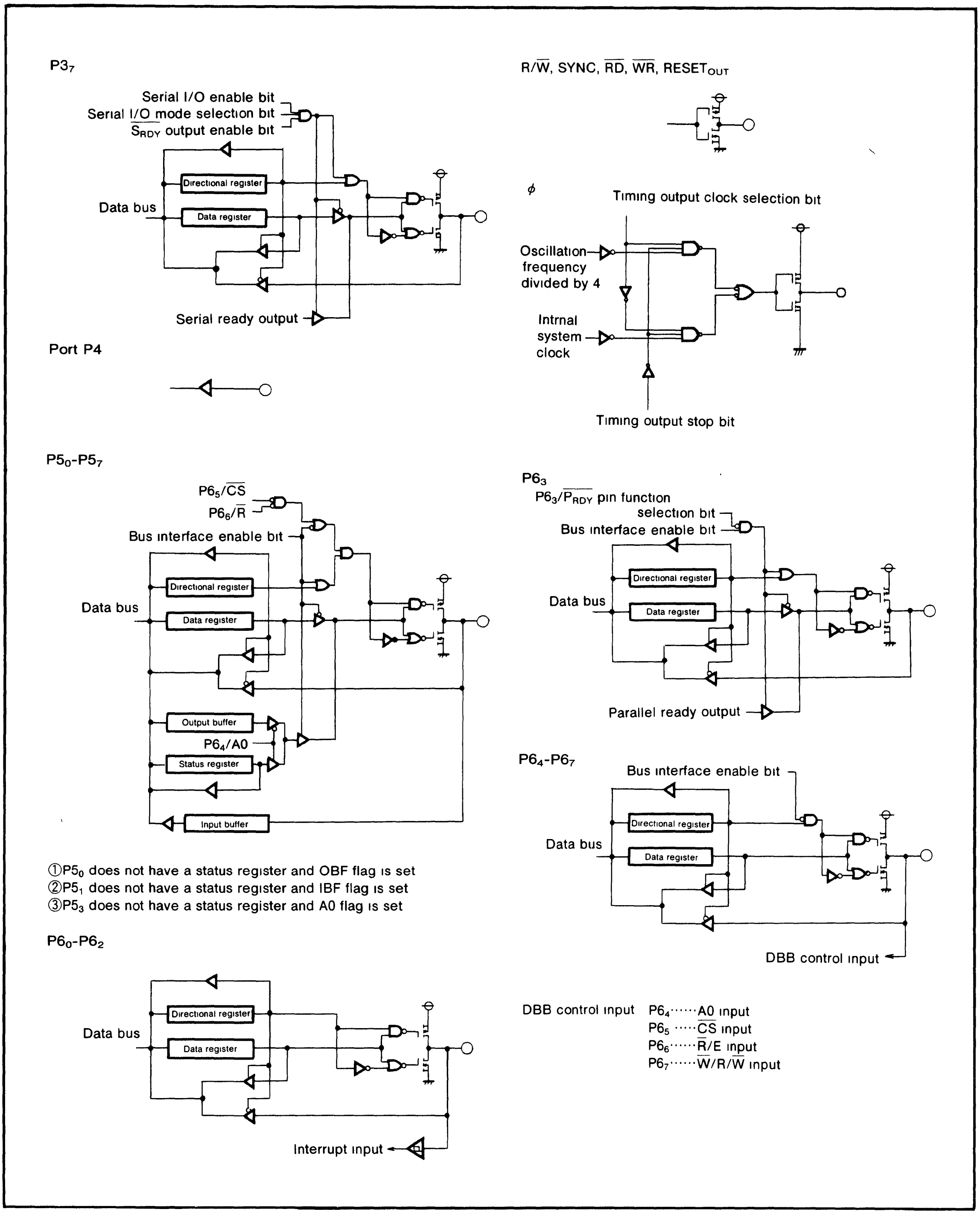


Fig. 34 Ports P0-P6 block diagram (single-chip mode) and output only pin output format (1)



①P5₀ does not have a status register and OBF flag is set
②P5₁ does not have a status register and IBF flag is set
③P5₃ does not have a status register and A0 flag is set

DBB control input P6₄······A0 input
P6₅ ·····C̄S̄ input
P6₆······R̄/E input
P6₇······W/R/W̄ input

Fig. 35 Ports P0-P6 block diagram (single-chip mode) and output only pin output format (2)

PROCESSOR MODE

By changing the contents of the processor mode bits (bits 0 and 1 at address $00DF_{16}$), three different operation modes can be selected; single-chip mode, memory expansion mode, and microprocessor mode.

In the memory expansion mode and the microprocessor mode, ports P0-P2 can be used as address, and data input/output pins.

Figure 37 shows the functions of ports P0-P2

The memory map for the single-chip mode is shown in Figure 2 and for other modes, in Figure 36.

By connecting CNV_{SS} to V_{SS}, all three modes can be selected through software by changing the processor mode bits. Connecting CNV_{SS} to V_{CC} automatically forces the microcomputer into microprocessor mode.

The three different modes are explained as follows

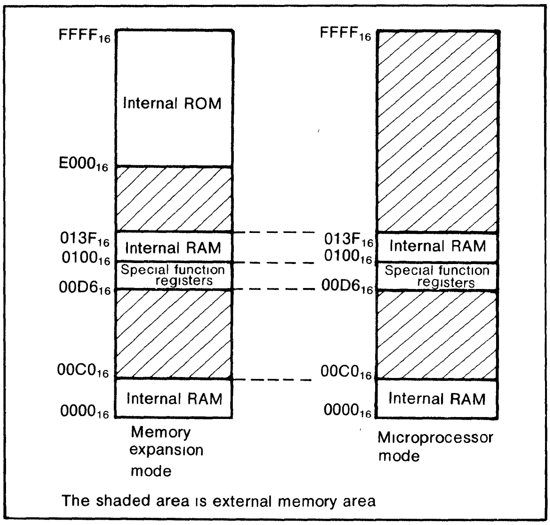


Fig. 36 External memory map in processor mode (M37451M4)

(1) Single-chip mode [00]
The microcomputer will automatically be in the single-chip mode when started from reset, if CNV_{SS} is connected to V_{SS}. Ports P0-P2 will work as original I/O ports.

(2) Memory expansion mode [01]
The microcomputer will be placed in the memory expansion mode when CNV_{SS} is connected to V_{SS} and the processor mode bits are set to "01" This mode is used to add external memory when the internal memory is not sufficient.
In this mode, port P0 and port P1 are as a system address bus and the original I/O pin function is lost.
Port P2 becomes the data bus of D_7-D_0 (including instruction code) and loses its normal I/O functions.

(3) Microprocessor mode [10]
After connecting CNV_{SS} to V_{CC} and initiating a reset or connecting CNV_{SS} to V_{SS} and the processor mode bits are set to "10", the microcomputer will automatically default to this mode. In this mode, the internal ROM is disabled so the external memory is required. Other functions are same as the memory expansion mode. The relationship between the input level of CNV_{SS} and the processor mode is shown in Table 3.

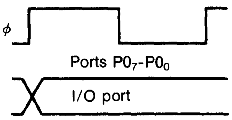
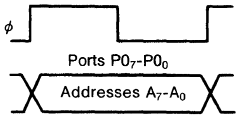
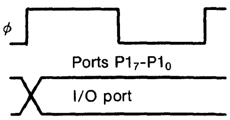
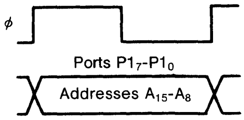
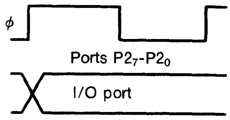
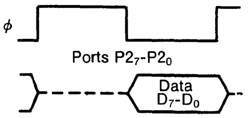
	CM_1	0	0	1
	CM_0	0	1	0
Port	Mode	Single-chip mode	Memory expansion mode	Microprocessor mode
Port P0				Same as left
Port P1				Same as left
Port P2				Same as left

Fig. 37 Processor mode and function of ports P0-P2

Table 3. Relationship between CNV_{SS} pin input level and processor mode

CNV_{SS}	Mode	Explanation
V_{SS}	• Single-chip mode • Memory expansion mode • Microprocessor mode	The single-chip mode is set by the reset All modes can be selected by changing the processor mode bit with the program
V_{CC}	• Microprocessor mode	The microprocessor mode is set by the reset

CLOCK GENERATING CIRCUIT

The built-in clock generating circuits are shown in Figure 40.

When an STP instruction is executed, the internal clock ϕ stops oscillating at "H" level. At the same time, FF_{16} is set in the low-order byte of timer 1, 03_{16} is set in the high-order byte, and timer 1 count source is forced to $f(X_{IN})$ divided by four. This connection is cleared when timer 1 overflows or the reset is in, as discussed in the timer section.

The oscillator is restarted when an interrupt is accepted. However, the clock ϕ keeps its "H" level until timer 1 overflows.

This is because the oscillator needs a set-up period if a ceramic or a quartz crystal oscillator is used

When the WIT instruction is executed, the clock ϕ stops in the "H" level but the oscillator continues running. This wait state is cleared when an interrupt is accepted. Since the oscillation does not stop, the next instructions are executed at once.

To return from the stop or the wait status, the interrupt enable bit must be set to "1" before executing STP or WIT instruction. Especially, to return from the stop status, the timer 1 count enable bit must be set to "1" and the timer 1 interrupt enable bit must be set to "0" before executing STP instruction.

With the M37451, the MISRG2 bit 6 shown in Figure 22 can be used to double the bus cycle. However, the timer, UART, and PWM operations are unafffected. This facilitates accessing of slow peripheral LSIs when external memory and I/O are extended in memory expansion mode or microprocessor mode. Note that this bit also affects the bus cycle in single-chip mode.

The circuit example using a ceramic oscillator (or a quartz crystal oscillator) is shown in Figure 38.

The constant capacitance will differ depending on which oscillator is used, and should be set to the manufactures suggested value.

The example of external clock usage is shown in Figure 39. X_{IN} is the input, and X_{OUT} is open.

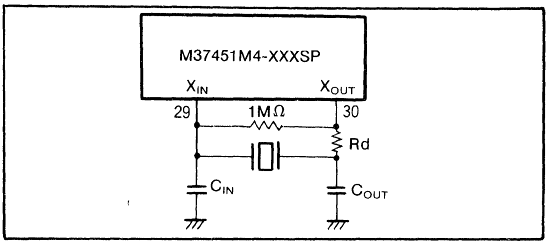


Fig. 38 External ceramic resonator circuit

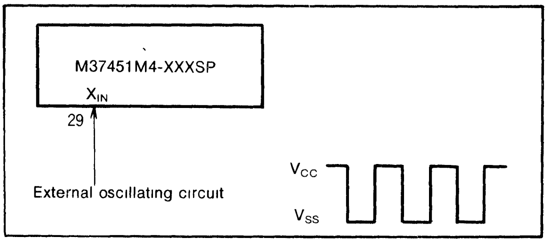


Fig. 39 External clock input circuit

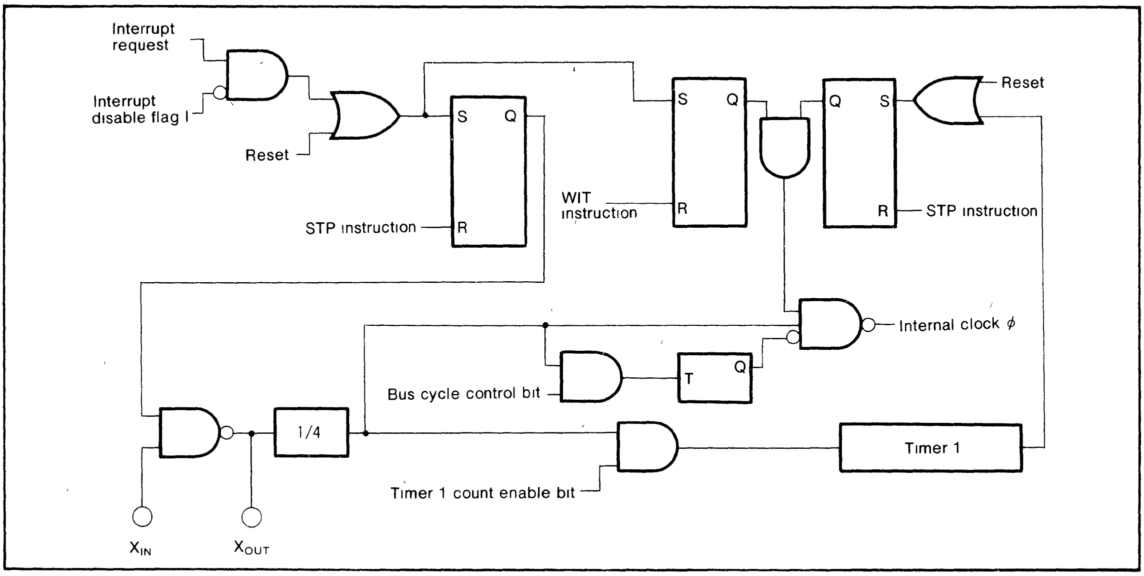


Fig. 40 Block diagram of clock generating circuit

PROGRAMMING NOTES

(1) Processor status register

1. Except for the interrupt disable flag (I) being set to "1", the content of the processor status register (PS) is unpredictable after a reset. Therefore, flags affecting program execution must be initialized.
   The T flag and D flag which affect arithmetic operations, must always be initialized.
2. An NOP instruction must be used after the execution of a PLP instruction.

(2) Interrupts

Even though the BBC and BBS instructions are executed just after the interrupt request bits are modified (by the program), those instructions are only valid for the contents before the modification. Also, at least one instruction cycle must be used (such as an NOP) between the modification of the interrupt request bits and the execution of the BBC and BBS instructions.

(3) Decimal operations

1. Decimal operations are performed by setting the decimal mode flag (D) and executing the ADC or SBC instruction In this case, there must be at least one instruction following the ADC or SBC instruction before executing the SEC, CLC, or CLD instruction.
2. The N (Negative), V(Overflow), and Z(Zero) flags are ignored during decimal mode.

(4) Timers

1. The frequency dividing ratio when n (0 to 65535) is written in the timer latch is 1/(n+1).
2. When directly writing a value in the timer, set the count enable bit to count disable (0) and write in the low-order byte first and then in the high-order byte.
3. The timer value must be read from the high-order byte first.

(5) Serial I/O

In clock synchronous serial I/O mode, if the receiver is to output an $\overline{S_{RDY}}$ using an external clock, the receive enable bit, $\overline{S_{RDY}}$ output enable bit, and transmission enable bit must be set to "1"

(6) A-D conversion

The comparator consists of coupling capacitors that lose their charge when the clock frequency is low. Therefore,f(X_{IN})must be no less than 1MHz during A-D conversion. (If the bus cycle control bit is "1", the bus cycle is doubled and the A-D conversion time is also doubled, therefore, f (X_{IN}) must not be less than 2MHz.) Also, the STP and WIT instructions must not be executed during A-D conversion

(7) STP instruciton

The STP instruction must be executed after setting the timer 1 count enable bit (bit 4 at address $00DE_{16}$) to enable ("1").

(8) Multiply/Divide instructions

1. The MUL and DIV instructions are not affected by the T and D flags.
2. The contents of the processor status register are unaffected by multiply or divide instructions.

DATA REQUIRED FOR MASK ORDERING

Please send the following data for mask orders.

- mask ROM order confirmation form
- mark specification form
- ROM data······EPROM 3 sets

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS} Output transistors are at "off" state	−0.3 to 7	V
V_I	Input voltage X_{IN}, $\overline{RESET}$		−0.3 to 7	V
V_I	Input voltage $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, ADV_{REF}, DAV_{REF}, V_{REF}, AV_{CC}		−0.3 to V_{CC}+0.3	V
V_I	Input voltage CNV_{SS}		−0.3 to 13	V
V_O	Output voltage $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, X_{OUT}, ϕ, $R/\overline{W}$, $\overline{RD}$, $\overline{WR}$, SYNC, $RESET_{OUT}$		−0.3 to V_{CC}+0.3	V
P_d	Power dissipation	T_a = 25℃	1000(Note 1)	mW
Topr	Operating temperature		−20 to 85	℃
Tstg	Storage temperature		−40 to 125	℃

Note 1 : 500mW in case of the flat package

RECOMMENDED OPERATING CONDITIONS

(V_{CC}=5V±10%, Ta=−20 to 85℃ unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage		0		V
V_{IH}	"H" input voltage $\overline{RESET}$, X_{IN}, CNV_{SS} (Note 1)	0.8V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$ (expect Note 1)	2.0		V_{CC}	V
V_{IL}	"L" input voltage CNV_{SS} (Note 1)	0		0.2V_{CC}	V
V_{IL}	"L" input voltage $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$ (expect Note 1)	0		0.8	V
V_{IL}	"L" input voltage $\overline{RESET}$	0		0.12V_{CC}	V
V_{IL}	"L" input voltage X_{IN}	0		0.16V_{CC}	V
$I_{OL(peak)}$	"L" peak output current $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$			10	mA
$I_{OL(avg)}$	"L" average output current $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$ (Note 2)			5	mA
$I_{OH(peak)}$	"H" peak output current $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$			−10	mA
$I_{OH(avg)}$	"H" average output current $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$ (Note 2)			−5	mA
$f(X_{IN})$	Internal clock oscillating frequency	1		12.5	MHz

Note 1 : Ports operating as special function pins INT_1-INT_3($P6_0$-$P6_2$), EV_1-EV_3($P3_0$-$P3_2$), R_XD($P3_4$), S_{CLK}($P3_6$)

2 : $I_{OL(avg)}$ and $I_{OH(avg)}$ are the average current in 100ms

3 : The total of I_{OL} of Port P0, P1, and P2 should be 40mA (max)
The total of I_{OL} of Port P3, P5, P6, $R/\overline{W}$, SYNC, $RESET_{OUT}$, $\overline{RD}$, $\overline{WR}$ and ϕ should be 40mA (max)
The total of I_{OH} of Port P0, P1, and P2 should be 40mA (max)
The total of I_{OH} of Port P3, P5, P6, $R/\overline{W}$, SYNC, $RESET_{OUT}$, $\overline{RD}$, $\overline{WR}$, and ϕ should be 40mA (max)

ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10%, V_{SS}= 0 V, T_a=−20 to 85℃, f(X_{IN})=12.5MHz)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{OH}	"H" output voltage $\overline{RD}$, $\overline{WR}$, R/$\overline{W}$, SYNC, $RESET_{OUT}$, ϕ	I_{OH} =− 2 mA	V_{CC}−1			V
V_{OH}	"H" output voltage $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$	I_{OH} =− 5 mA	V_{CC}−1			V
V_{OL}	"L" output voltage $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $\overline{RD}$, $\overline{WR}$, R/$\overline{W}$, SYNC, $RESET_{OUT}$, ϕ	I_{OL} =2 mA			0.45	V
V_{OL}	"L" output voltage $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$	I_{OL} =5 mA			1	V
$V_{T+} - V_{T-}$	Hysteresis INT1-INT3($P6_0$-$P6_2$), EV_1-EV_3($P3_0$-$P3_2$), R_xD($P3_4$), S_{CLK}($P3_6$)	Function input level	0.3		1	V
$V_{T+} - V_{T-}$	Hysteresis $\overline{RESET}$				0.7	V
$V_{T+} - V_{T-}$	Hysteresis X_{IN}		0.1		0.5	V
I_{IL}	"L" input current $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $\overline{RESET}$, X_{IN}	V_I =V_{SS}	−5		5	μA
I_{IH}	"H" input current $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $\overline{RESET}$, X_{IN}	V_I =V_{CC}	−5		5	μA
V_{RAM}	RAM retention voltage	At stop mode	2			V
I_{CC}	Supply current	f(X_{IN})=12 5MHz At system operation		8	15	mA
		At stop mode (Note 1)		1	10	μA

Note 1 : The terminals $\overline{RD}$, $\overline{WR}$, SYNC, R/$\overline{W}$, $RESET_{OUT}$, ϕ, D-A_1 and D-A_2 are all open The other ports, which are in the input mode, are connected to V_{SS} A-D converter is in the A-D completion state The current through ADV_{REF} and DAV_{REF} is not included. (Fig 45)

A-D CONVERTER CHARACTERISTICS

(V_{CC}=AV_{CC}=5V±10%, V_{SS}=AV_{SS}= 0 V, T_a =−20 to 85℃, f(X_{IN})=12.5MHz unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
—	Resolution				8	Bits
—	Absolute accuracy	V_{CC}=AV_{CC}=ADV_{REF}=5V±10%		±1.5	±3	LSB
t_{CONV}	Conversion time				49	$t_{c(\phi)}$
V_{IA}	Analog input voltage		AV_{SS}		AV_{CC}	V
V_{ADVREF}	Reference input voltage		2		V_{CC}	V
R_{LADDER}	Ladder resistance value	ADV_{REF}= 5 V	20	35	50	kΩ
$I_{IADVREF}$	Reference input current	ADV_{REF}= 5 V	0.1	0.14	0.25	mA
V_{AVCC}	Analog power supply input voltage			V_{CC}		V
V_{AVSS}	Analog power supply input voltage			0		V

D-A CONVERTER CHARACTERISTICS (V_{CC}=5V±10%, V_{SS}=AV_{SS}= 0 V, T_a =−20 to 85℃ unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
—	Resolution				8	Bits
—	Full scale deviation	V_{CC}=DAV_{REF}=5V±10%			1.0	%
t_{SU}	Set time				3	μs
R_O	Output resistance		1	2	4	kΩ
V_{AVSS}	Analog power supply input voltage			0		V
V_{DAVREF}	Reference input voltage		4		V_{CC}	V
I_{DAVREF}	Reference power input current		0	5	10	mA

TIMING REQUIREMENTS

Port/single-chip mode (V_{CC}=5V±10%, V_{SS}=0V, T_a=−20 to 85℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{su(P0D-\phi)}$	Port P0 input setup time	Fig 41	160			ns
$t_{su(P1D-\phi)}$	Port P1 input setup time		160			ns
$t_{su(P2D-\phi)}$	Port P2 input setup time		160			ns
$t_{su(P3D-\phi)}$	Port P3 input setup time		160			ns
$t_{su(P4D-\phi)}$	Port P4 input setup time		160			ns
$t_{su(P5D-\phi)}$	Port P5 input setup time		160			ns
$t_{su(P6D-\phi)}$	Port P6 input setup time		160			ns
$t_{h(\phi-P0D)}$	Port P0 input hold time		40			ns
$t_{h(\phi-P1D)}$	Port P1 input hold time		40			ns
$t_{h(\phi-P2D)}$	Port P2 input hold time		40			ns
$t_{h(\phi-P3D)}$	Port P3 input hold time		40			ns
$t_{h(\phi-P4D)}$	Port P4 input hold time		40			ns
$t_{h(\phi-P5D)}$	Port P5 input hold time		40			ns
$t_{h(\phi-P6D)}$	Port P6 input hold time		40			ns
$t_c(X_{IN})$	External clock input cycle time		80		1000	ns
$t_w(X_{IN}L)$	External clock input "L" pulse width		20			ns
$t_w(X_{IN}H)$	External clock input "H" pulse width		20			ns
$t_r(X_{IN})$	External clock rising edge time				20	ns
$t_f(X_{IN})$	External clock falling edge time				20	ns

Master CPU bus interface timing ($\overline{R}$ and $\overline{W}$ separation type mode)

(V_{CC}=5V±10%, V_{SS}=0V, T_a=−20 to 85℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{su(CS-R)}$	$\overline{CS}$ setup time	Fig 42	0			ns
$t_{su(CS-W)}$	$\overline{CS}$ setup time		0			ns
$t_{h(R-CS)}$	$\overline{CS}$ hold time		0			ns
$t_{h(W-CS)}$	$\overline{CS}$ hold time		0			ns
$t_{su(A-R)}$	A0 setup time		10			ns
$t_{su(A-W)}$	A0 setup time		10			ns
$t_{h(R-A)}$	A0 hold time		0			ns
$t_{h(W-A)}$	A0 hold time		0			ns
$t_{w(R)}$	Read pulse width		120			ns
$t_{w(W)}$	Write pulse width		120			ns
$t_{su(D-W)}$	Date input setup time before write		50			ns
$t_{h(W-D)}$	Date input hold time after write		0			ns

Master CPU bus interface timing (R/$\overline{W}$ type mode)

(V_{CC}=5V±10%, V_{SS}=0V, T_a=−20 to 85℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{su(CS-E)}$	$\overline{CS}$ setup time	Fig 42	0			ns
$t_{h(E-CS)}$	$\overline{CS}$ hold time		0			ns
$t_{su(A-E)}$	A0 setup time		10			ns
$t_{h(E-A)}$	A0 hold time		0			ns
$t_{su(RW-E)}$	R/$\overline{W}$ setup time		0			ns
$t_{h(E-RW)}$	R/$\overline{W}$ hold time		0			ns
$t_{w(EL)}$	Enable clock "L" pulse width		120			ns
$t_{w(EH)}$	Enable clock "H" pulse width		120			ns
$t_{r(E)}$	Enable clock rising edge time				25	ns
$t_{f(E)}$	Enable clock falling edge time				25	ns
$t_{su(D-E)}$	Data input setup time before write		50			ns
$t_{h(E-D)}$	Data input hold time after write		0			ns

Local bus/memory expansion mode, microprocessor mode

(V_{CC}=5V±10%, V_{SS}=0V, T_a=−20 to 85℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{su(D-\phi)}$	Data input setup time	Fig 43	60			ns
$t_{h(\phi-D)}$	Data input hold time		0			ns
$t_{su(D-\overline{RD})}$	Data input setup time		60			ns
$t_{h(\overline{RD}-D)}$	Data input hold time		0			ns

Clock synchronous serial I/O

(V_{CC}=5V±10%, V_{SS}=0V, T_a=−20 to 85℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{su(R_XD-S_{CLK})}$	Serial input setup time	Fig. 44	160			ns
$t_{h(S_{CLK}-R_XD)}$	Serial input hold time		80			ns
$t_{r(R_XD)}$	Serial input rising edge time				30	ns
$t_{f(R_XD)}$	Serial input falling edge time				30	ns
$t_{r(S_{CLK})}$	Serial input clock rising edge time				30	ns
$t_{f(S_{CLK})}$	Serial input clock falling edge time				30	ns
$t_{C(S_{CLK})}$	Serial input clock period		640			ns
$t_{W(S_{CLK}L)}$	Serial input clock "L" pulse width		290			ns
$t_{W(S_{CLK}H)}$	Serial input clock "H" pulse width		290			ns

SWITCHING CHARACTERISTICS

Port/single-chip mode (V_{CC}=5V±10%, V_{SS}=0V, T_a=−20 to 85℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{d(\phi-P0Q)}$	Port P0 data output delay time	Fig 41			200	ns
$t_{d(\phi-P1Q)}$	Port P1 data output delay time				200	ns
$t_{d(\phi-P2Q)}$	Port P2 data output delay time				200	ns
$t_{d(\phi-P3Q)}$	Port P3 data output delay time				200	ns
$t_{d(\phi-P5Q)}$	Port P5 data output delay time				200	ns
$t_{d(\phi-P6Q)}$	Port P6 data output delay time				200	ns
$t_{C(\phi)}$	Cycle time		320		4000	ns
$t_{W(\phi H)}$	ϕ clock pulse width ("H" level)		150			ns
$t_{W(\phi L)}$	ϕ clock pulse width ("L" level)		130			ns
$t_{r(\phi)}$	ϕ clock rising edge time				20	ns
$t_{f(\phi)}$	ϕ clock falling edge time				20	ns

Master CPU bus interface ($\overline{R}$ and $\overline{W}$ separation type mode)

(V_{CC}=5V±10%, V_{SS}=0V, T_a=−20 to 85℃, unless otherwise noted)

Symbol	Parameter	Test condition	Limits			Unit
			Min	Typ	Max	
$t_{a(R-D)}$	Data output enable time after read	Fig 42			80	ns
$t_{V(R-D)}$	Data output disable time after read		0		30	ns
$t_{PLH(R-PR)}$	$\overline{P}_{RDY}$ output transmission time after read				150	ns
$t_{PLH(W-PR)}$	$\overline{P}_{RDY}$ output transmission time after write				150	ns

Master CPU bus interface (R/$\overline{W}$ type mode) (V_{CC}=5V±10%, V_{SS}=0V, T_a=−20 to 85℃, unless otherwise noted)

Symbol	Parameter	Test condition	Limits			Unit
			Min	Typ	Max	
$t_{a(E-D)}$	Data output enable time after read	Fig.42			80	ns
$t_{V(E-D)}$	Data output disable time after read		0		30	ns
$t_{PLH(E-PR)}$	$\overline{P}_{RDY}$ output transmission time after E clock				150	ns

Local bus/memory expansion mode, microprocessor mode

(V_{CC}=5V±10%, V_{SS}=0V, T_a=−20 to 85℃, unless otherwise noted)

Symbol	Parameter	Test condition	Limits			Unit
			Min	Typ	Max	
$t_{d(\phi-A)}$	Address delay time after ϕ	Fig 43			80	ns
$t_{V(\phi-A)}$	Address effective time after ϕ		10			ns
$t_{V(RD-A)}$	Address effective time after $\overline{RD}$		10			ns
$t_{V(WR-A)}$	Address effective time after $\overline{WR}$		10			ns
$t_{d(\phi-D)}$	Data output delay time after ϕ				80	ns
$t_{d(WR-D)}$	Data output delay time after $\overline{WR}$				80	ns
$t_{V(\phi-D)}$	Data output effective time after ϕ		20			ns
$t_{V(WR-D)}$	Data output effective time after $\overline{WR}$		20			ns
$t_{d(\phi-RW)}$	R/$\overline{W}$ delay time after ϕ				80	ns
$t_{d(\phi-SYNC)}$	SYNC delay time after ϕ				80	ns
$t_{W(RD)}$	$\overline{RD}$ pulse width		130			ns
$t_{W(WR)}$	$\overline{WR}$ pulse width		130			ns

Clock synchronous serial I/O (V_{CC}=5V±10%, V_{SS}=0V, T_a=−20 to 85℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ.	Max.	
$t_{d(S_{CLK}-T_XD)}$	Serial output delay time	Fig 44			100	ns
$t_{r(S_{CLK})}$	Serial output clock rising edge time				30	ns
$t_{f(S_{CLK})}$	Serial output clock falling edge time				30	ns
$t_{C(S_{CLK})}$	Serial output clock period		640			ns
$t_{W(S_{CLK}L)}$	Serial output clock "L" pulse width		290			ns
$t_{W(S_{CLK}H)}$	Serial output clock "H" pulse width		290			ns

TEST CONDITION

Input voltage level : V_{IH} 2.4V
V_{IL} 0.45V
Output test level : V_{OH} 2.0V
V_{OL} 0.8V

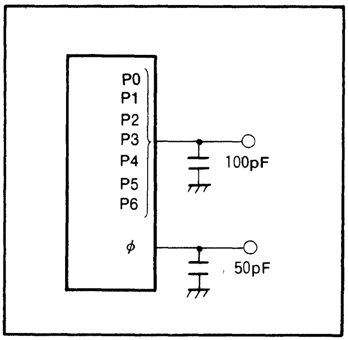


Fig. 41 Test circuit in single-chip mode

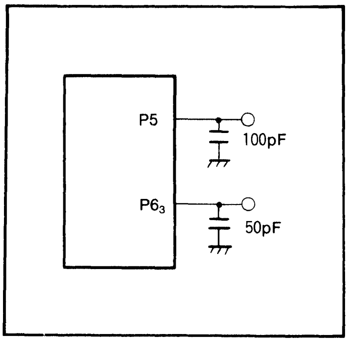


Fig. 42 Master CPU bus interface test circuit

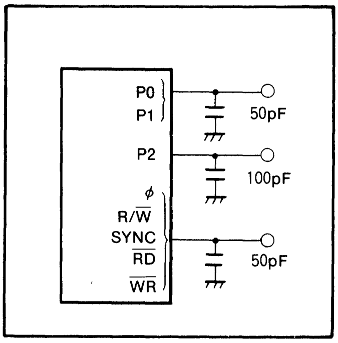


Fig. 43 Local bus test circuit

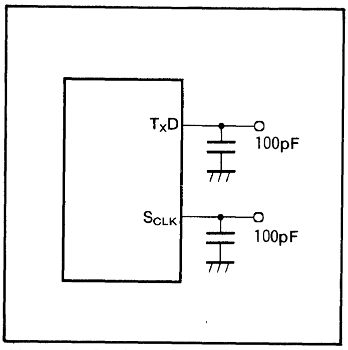


Fig. 44 Serial I/O test circuit

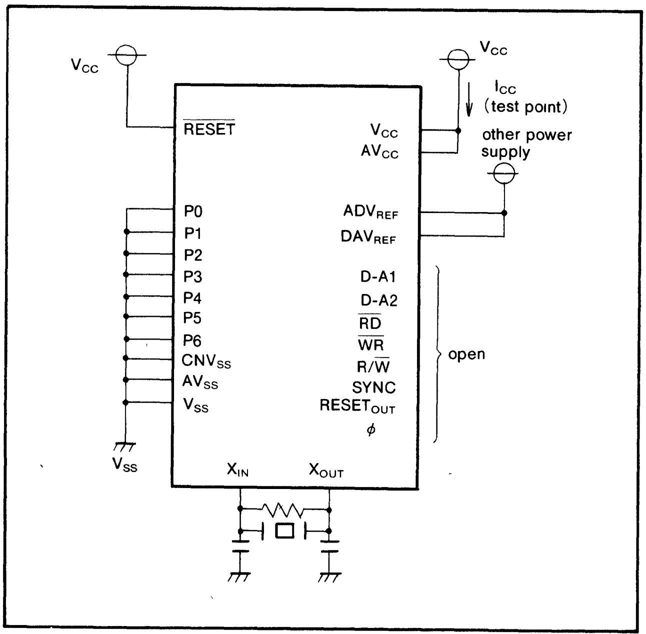
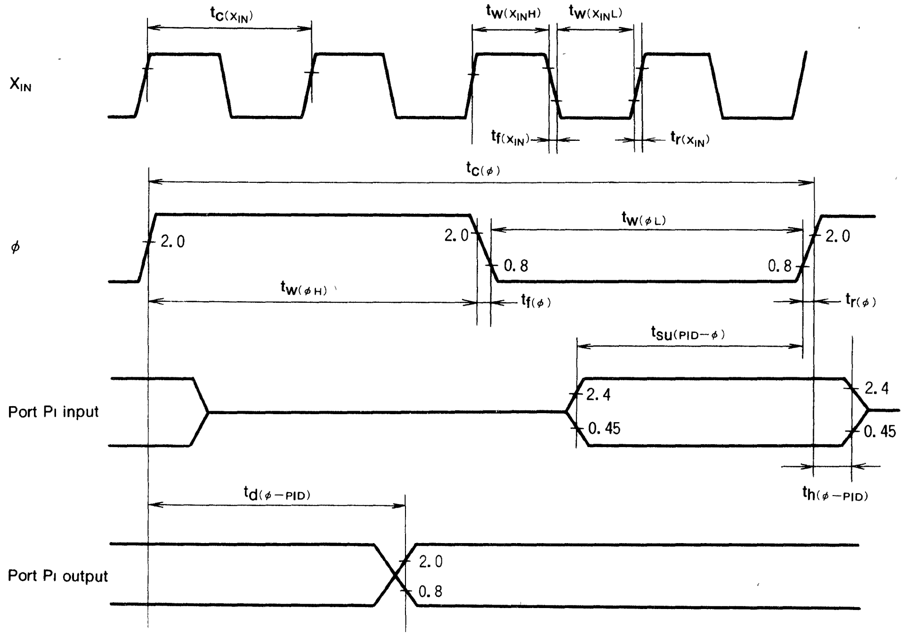


Fig. 45 I_{CC} (at stop mode) test condition

TIMING DIAGRAM

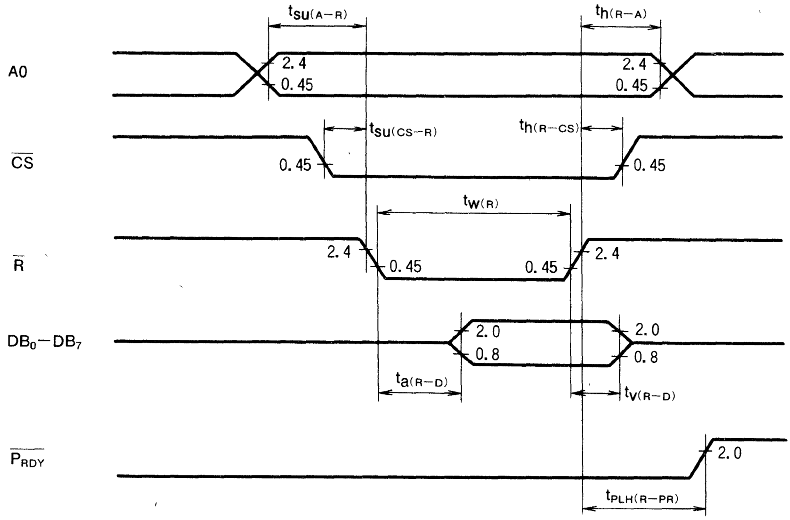
Port/single-chip mode timing diagram



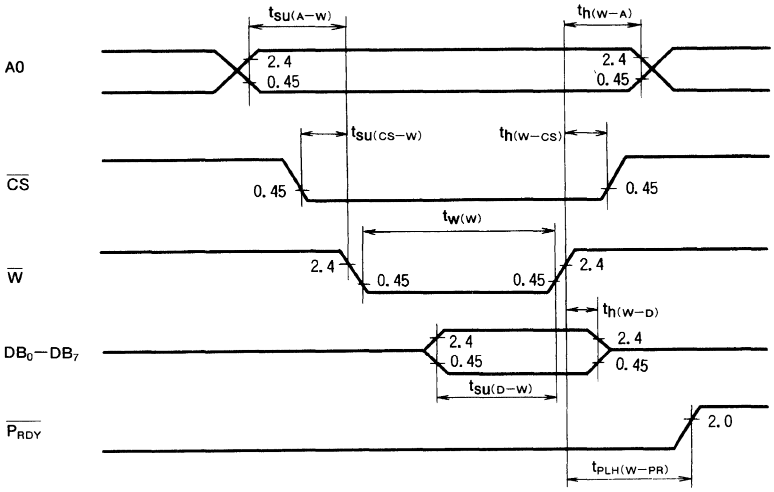
Note : $V_{IH}=0.8V_{CC}$, $V_{IL}=0.16V_{CC}$ of X_{IN}

Master CPU bus interface/ $\overline{R}$ and $\overline{W}$ separation type timing diagram

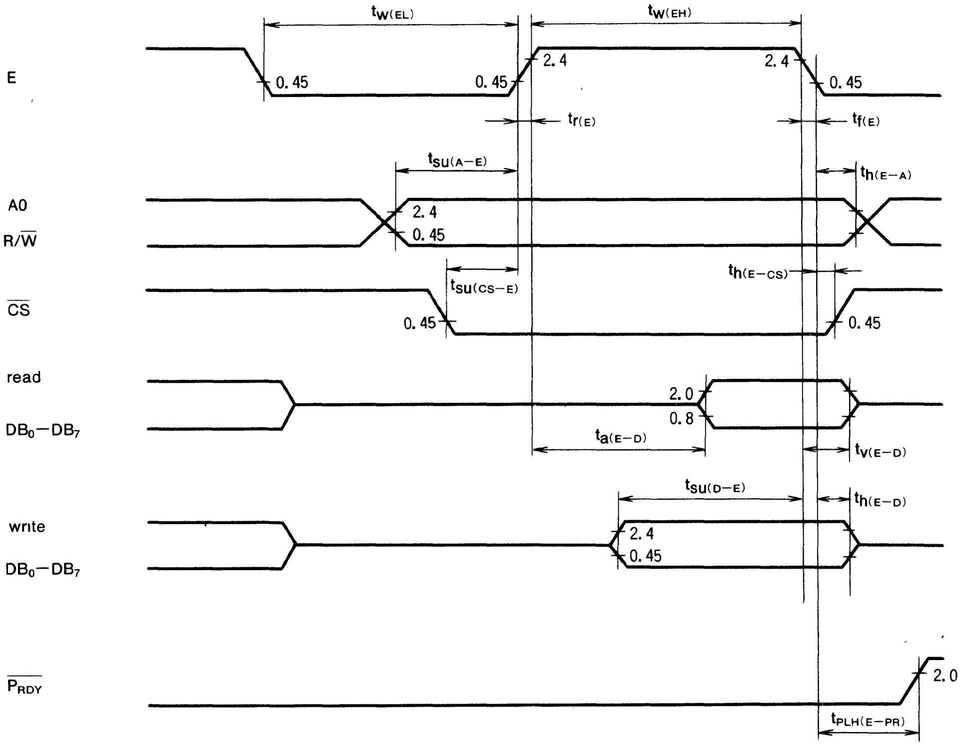
Read



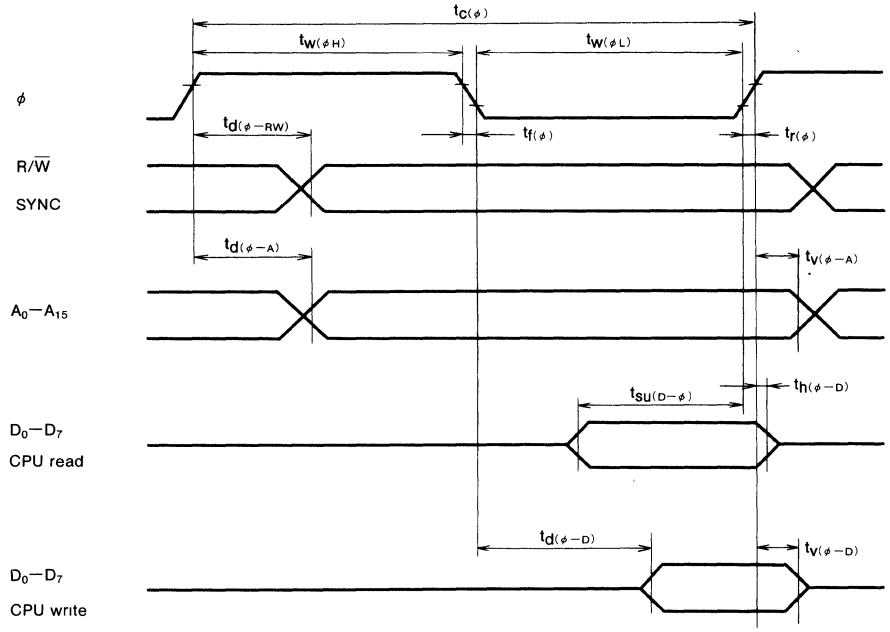
Write

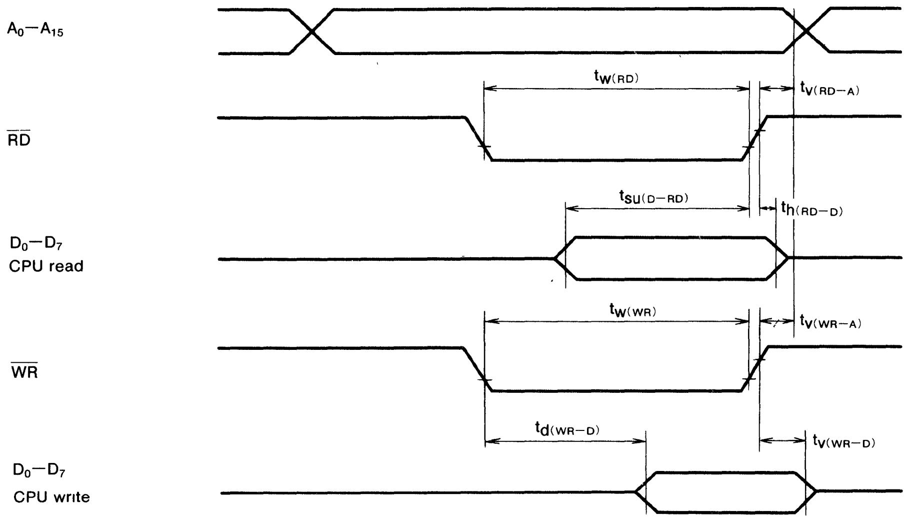


Master CPU interface/ R/$\overline{W}$ type timing diagram

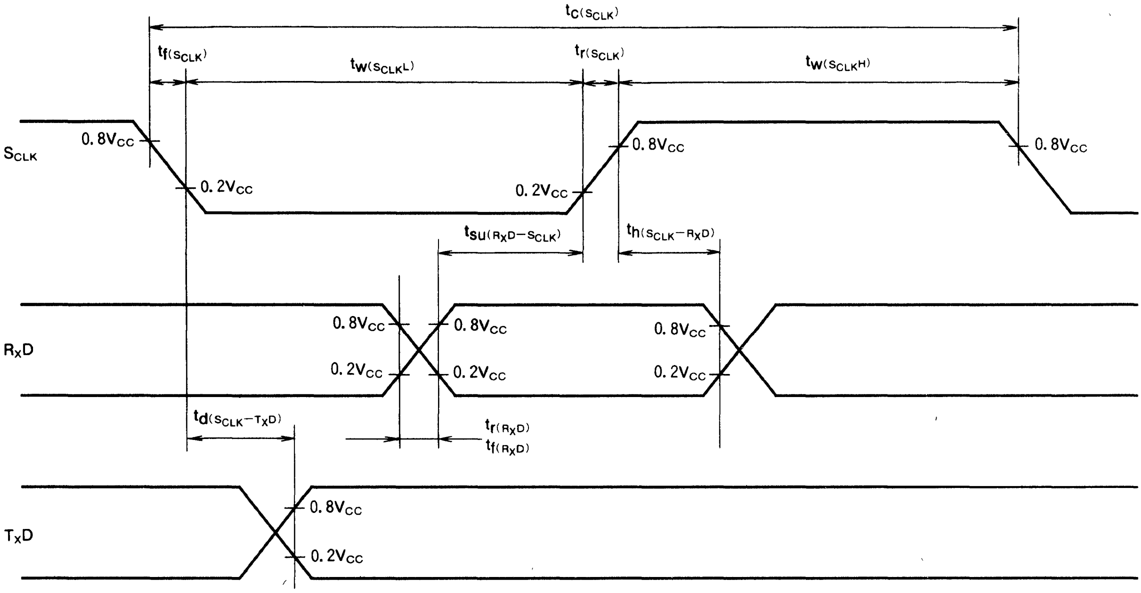


Local bus timing diagram





Serial I/O timing diagram



MITSUBISHI MICROCOMPUTERS

M37451SSP/FP/GP

8-BIT CMOS MICROCOMPUTER

DESCRIPTION

The M37451SSP/FP/GP is a single-chip microcomputer designed with CMOS silicon gate technology. It is housed in a 64-pin shrink plastic molded DIP or a 0.8mm pitch or 0.65mm pitch 80-pin plastic molded QFP. In addition to its simple instruction sets, the ROM, RAM and I/O addresses are placed on the same memory map to enable easy programming. It is suited for office automation equipment and control devices. The low power consumption made possible by the use of a CMOS process makes it especially suitable for battery powered devices requiring low power consumption. It also has a unique feature that enables it to be used as a slave microcomputer.

M37451SSP/FP/GP has basically the same functions as M37451M4-XXXSP/FP/GP except the RAM size and the fact that these three need external ROM area.

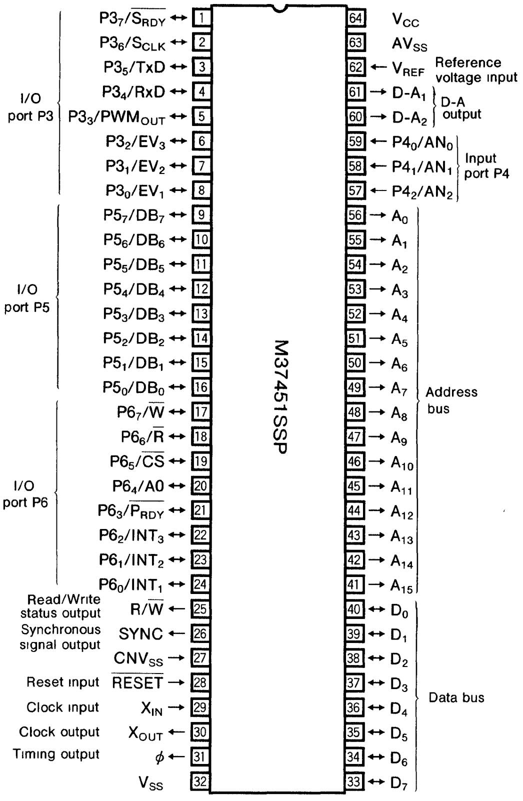
FEATURES

- Number of basic instructions ········· 71
  69 MELPS 740 basic instructions+2 multiply/divide instructions
- Memory size ROM ········· None
  RAM ········· 1024 bytes
- Instruction execution time
  (minimum instructions at 12.5 MHz frequency) 0.64μs
- Single power supply ········· 5V±10%
- Power dissipation normal operation mode
  (at 12.5MHz frequency) ········· 40mW
- Subroutine nesting ········· 128 levels max.
- Interrupt ········· 15 events
- Master CPU bus interface ········· 1 byte
- 16-bit timer ········· 3
- 8-bit timer (Serial I/O use) ········· 1
- Serial I/O (UART or clock synchronous) ········· 1
- A-D converter (8-bit resolution) ········· 3 channels (DIP)
  8 channels (QFP)
- D-A converter (8-bit resolution) ········· 2 channels
- PWM output with 8-bit prescaler
  (Either resolution 8-bit or 16-bit is software selectable) 1
- Programmable I/O
  (Ports P3, P5, P6) ········· 24
- Input (Port P4) ········· 3 (DIP), 8 (QFP)
- Output (Port D-A$_1$, D-A$_2$) ········· 2

APPLICATION

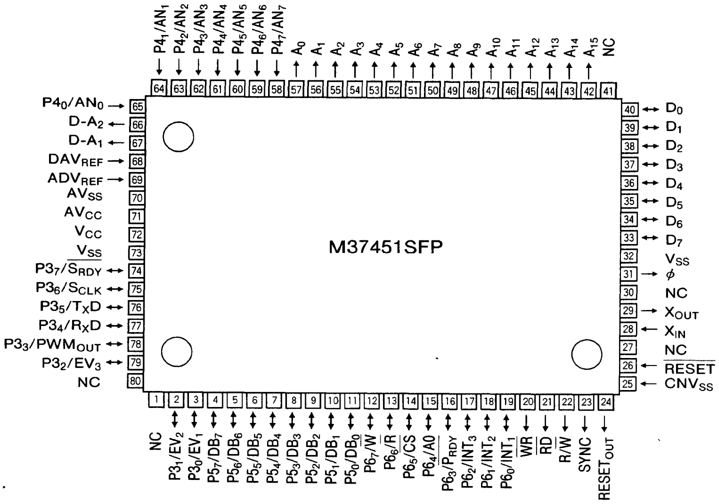
Slave controller for PPCs, facsimiles and page printers
HDD, optical disk, inverter and industrial motor controllers
Industrial robots and machines

PIN CONFIGURATION (TOP VIEW)

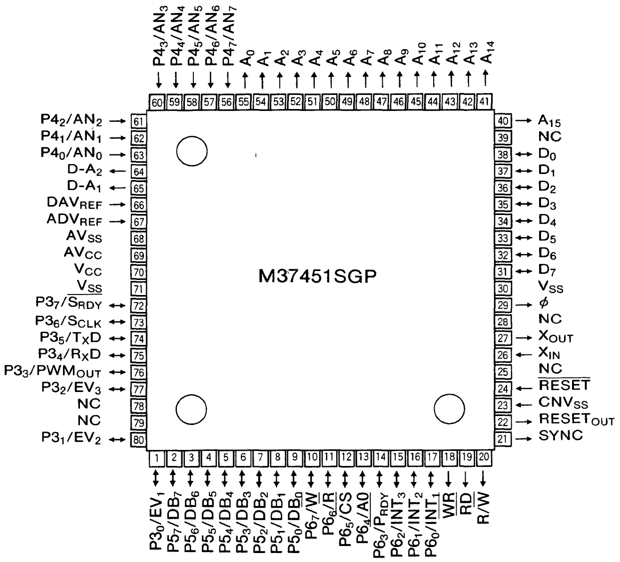


Outline 64P4B

PIN CONFIGURATION (TOP VIEW)



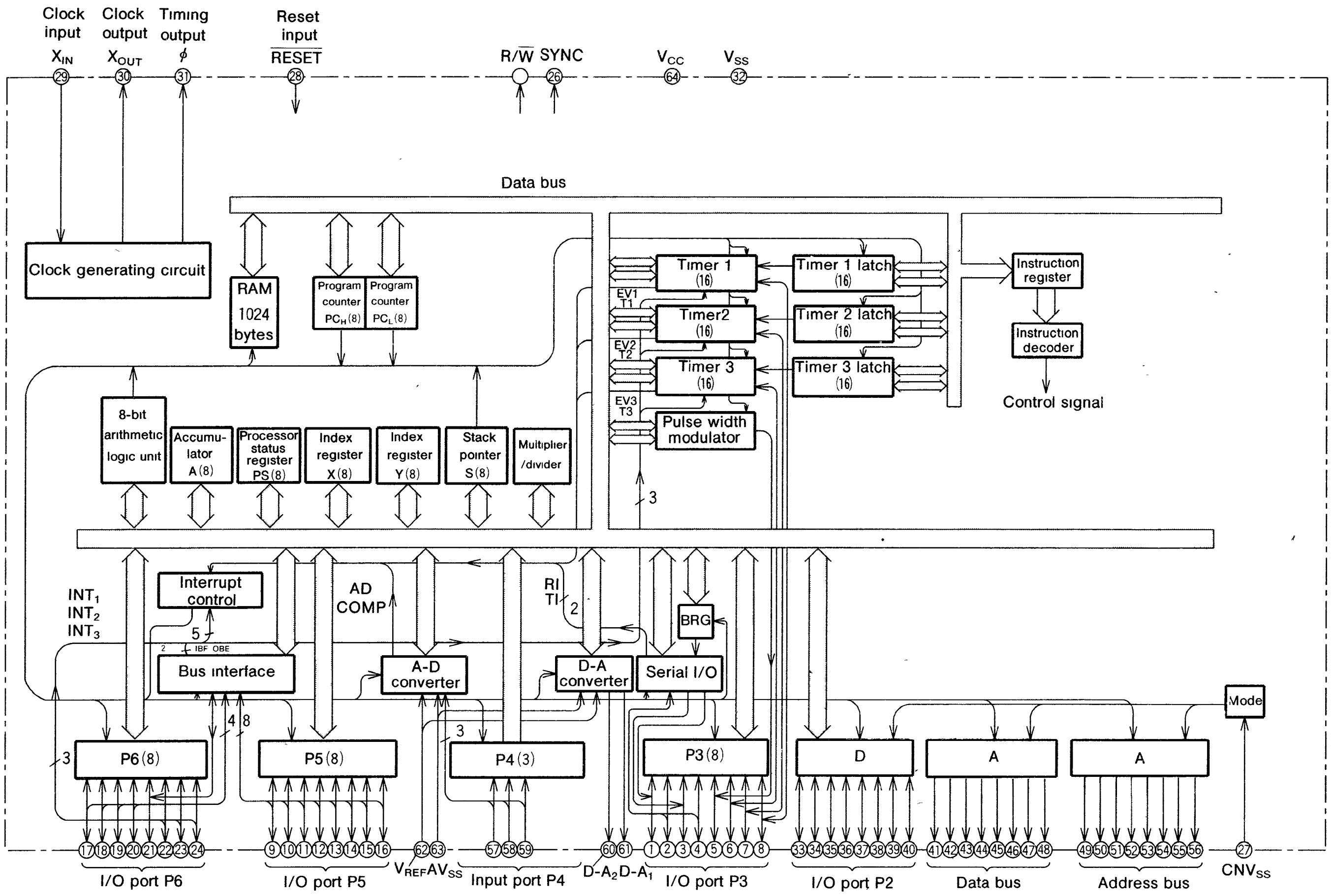
Outline 80P6N



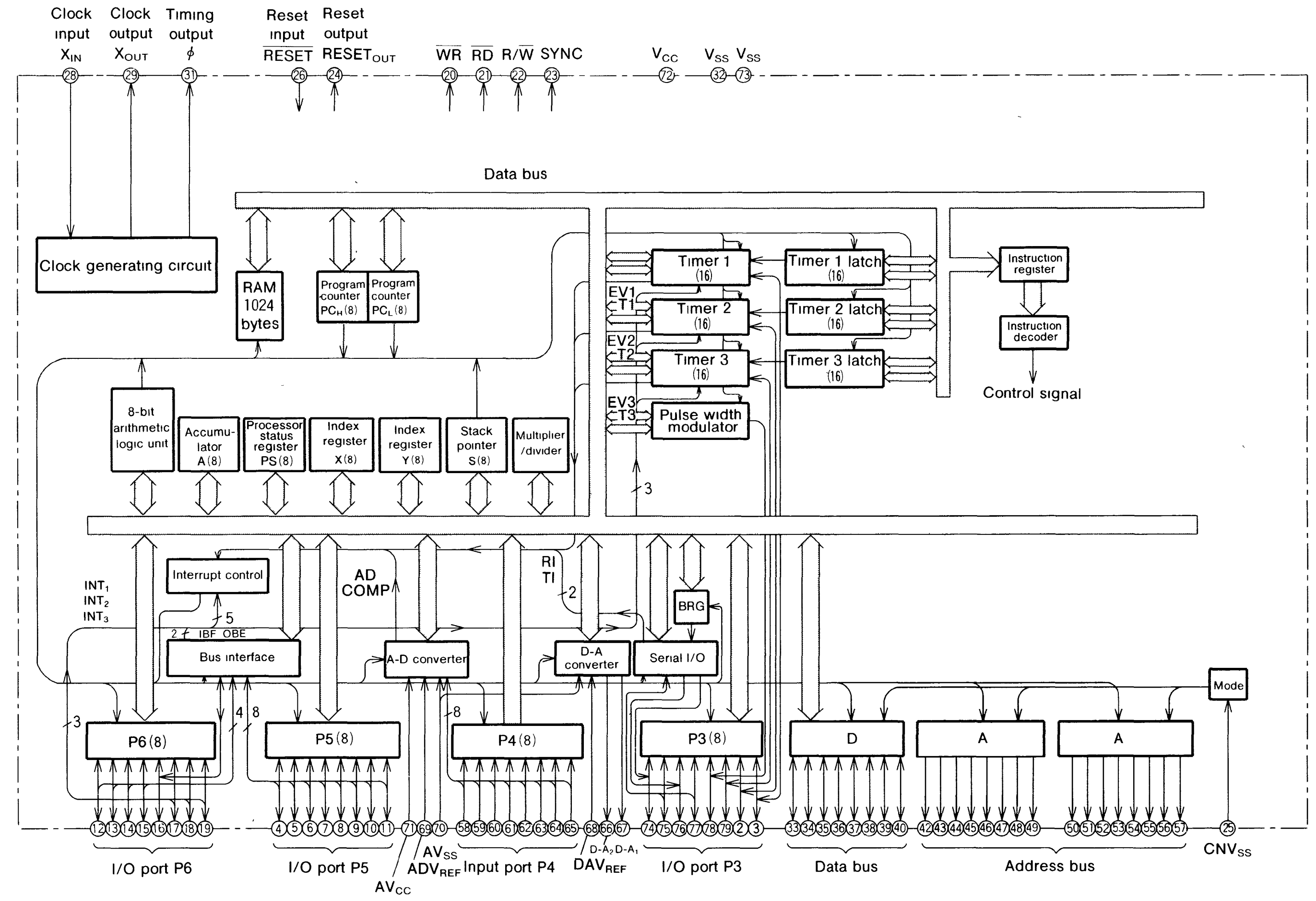
Outline 80P6S

NC : No connection

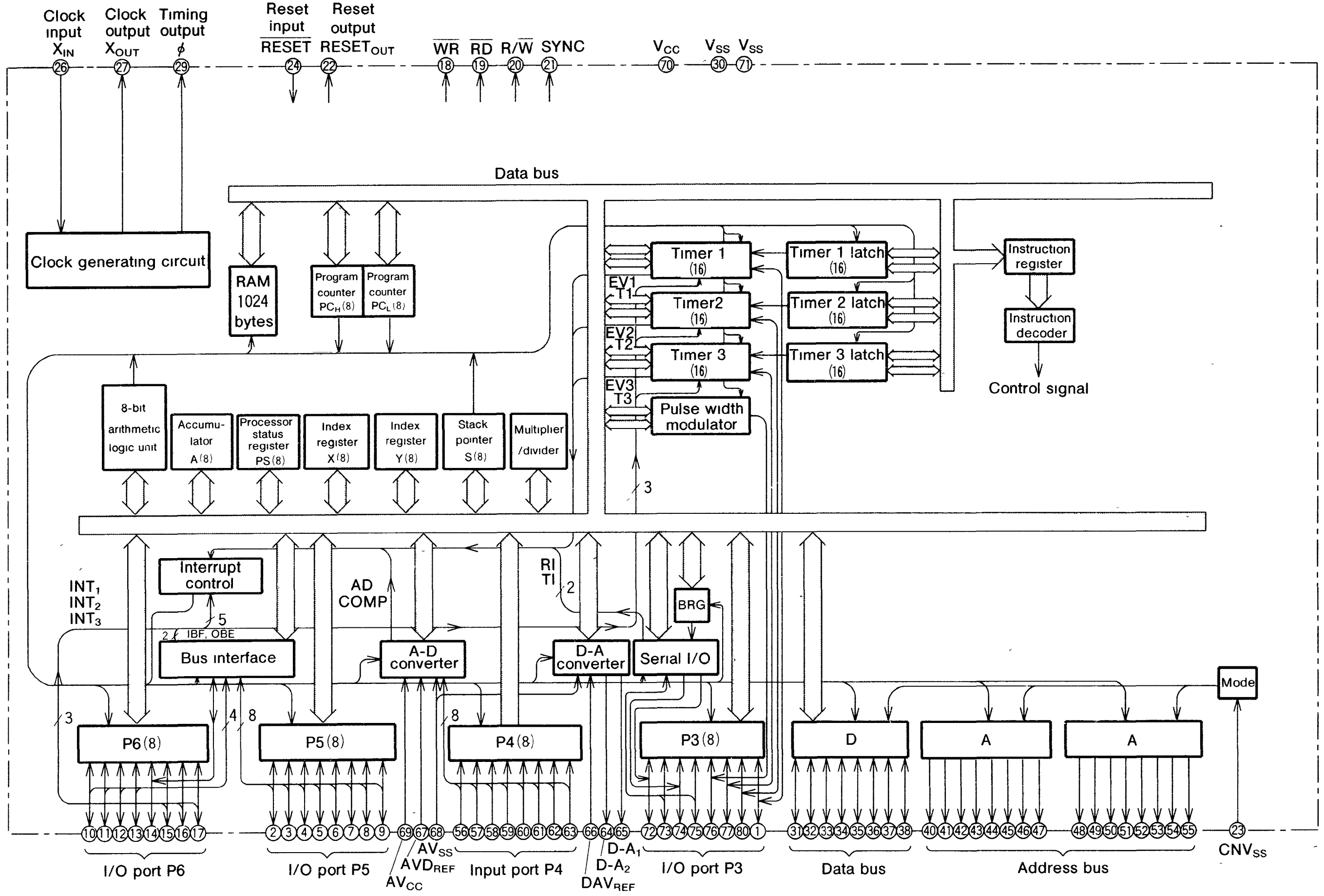
M37451SSP BLOCK DIAGRAM



M37451SFP BLOCK DIAGRAM



M37451SGP BLOCK DIAGRAM



FUNCTIONS OF M37451SSP/FP/GP

Parameter			Functions
Number of basic instructions			71(69 MELPS 740 basic instructions+2)
Instruction execution time			0 64μs(minimum instructions, at 12 5MHz frequency)
Clock frequency			12 5MHz(max)
RAM size	M37451SSP/FP/GP		1024 bytes
Input/Output port	P3, P5, P6	I/O	8-bit×3
	P4	Input	3-bit×1(8-bit×1 for 80-pin model)
	D-A	Output	2-bit×1
Serial I/O			UART or clock synchronous
Timers			16-bit timer×3, 8-bit timer(serial I/O baud rate generator)×1
A-D converter			8-bit×3 channels(8 channels for 80-pin model)
D-A converter			8-bit×2 channels
Pulse width modulator(with 8-bit prescaler)			8-bit or 16-bit×1
Data bus buffer			1-byte input and output each
Subroutine nesting			128-levels (max)
Interrupt			6 external interrupts, 8 internal interrupts, 1 software interrupt
Clock generating circuit			Built-in(ceramic or quarts crystal oscillator)
Supply voltage			5V±10%
Power dissipation			40mW(at 12 5MHz frequency)
Input/Output characters	Input/Output voltage		5V
	Output current		±5mA(max)
Operating temperature range			−20 to 85℃
Device structure			CMOS silicon gate
Package	M37451SSP		64-pin shrink plastic molded DIP
	M37451SFP		80-pin plastic molded QFP(0 8mm pitch)
	M37451SGP		80-pin plastic molded QFP(0 65mm pitch)

PIN DESCRIPTION

Pin	Name	Input/ Output	Functions
V_{CC}, V_{SS}	Supply voltage		Power supply inputs 5V±10% to V_{CC}, and 0V to V_{SS}
CNV_{SS}	CNV_{SS}	Input	This is connected to V_{CC}
$\overline{RESET}$	Reset input	Input	To enter the reset state, the reset input pin must be kept at a "L" for more than 8 clock cycles(under normal V_{CC} conditions) If more time is needed for the crystal oscillator to stabilize, this "L" condition should be maintained for the required time
X_{IN}	Clock input	Input	This chip has an internal clock generating circuit To control generating frequency, an external ceramic or a quartz crystal oscillator is connected between the X_{IN} and X_{OUT} pins If an external clock is used, the clock source should be connected to the X_{IN} pin and the X_{OUT} pin should be left open
X_{OUT}	Clock output	Output	
ϕ	Timing output	Output	Normally outputs signal consisting of oscillating frequency divided by four
SYNC	Synchronous signal output	Output	This signal is output "H" during operation code fetch and is used to control single stepping of programs
R/$\overline{W}$	Read/Write status output	Output	This signal determines the direction of the data bus It is "H" during read and "L" during write
A_0-A_{15}	Address bus	Output	This is 16-bit address bus
D_0-D_7	Data bus	I/O	This is 8-bit data bus
$P3_0$-$P3_7$	Input/Output port P3	I/O	Port P3 is an 8-bit I/O port with directional registers allowing each I/O bit to be individually programed as input or output The output structure is CMOS output Serial I/O, PWM output, or even I/O function can be selected with a program
$P4_0$-$P4_2$ ($P4_0$-$P4_7$)	Input port P4	Input	Analog input pin for the A-D converter The 64-pin model has three pins and the 80-pin model has eight pins They may also be used as digital input pins
$P5_0$-$P5_7$	Input/Output port P5	I/O	An 8-bit input/output port with the same function as P3 This port functions as an 8-bit data bus for the master CPU when slave mode is selected with a program
$P6_0$-$P6_7$	Input/Output port P6	I/O	An 8-bit input/output port with the same function as P3 Pins $P6_3$-$P6_7$ change to a control bus for the master CPU when slave mode is selected with a program Pins $P6_0$-$P6_2$ may be programmed as external interrupt input pins
D-A_1, D-A_2	D-A output	Output	Analog signal from D-A converter is output
V_{REF}	Reference voltage input	Input	Reference voltage input pin for A-D and D-A converter This pin is for 64-pin model only
ADV_{REF}	A-D reference voltage input	Input	Reference voltage input pin for A-D converter This pin is for 80-pin model only
DAV_{REF}	D-A reference voltage input	Input	Reference voltage input pin for D-A converter This pin is for 80-pin model only
AV_{SS}	Analog power supply		Ground level input pin for A-D and D-A converter Same voltage as V_{SS} is applied
AV_{CC}	Analog power supply		Power supply input pin for A-D converter This pin is for 80-pin model only Same voltage as $V_{CC}$is applied In the case of the 64-pin model AV_{CC} is connected to V_{CC} internally
$\overline{RD}$	Read signal output	Output	Control signal output as active "L" when valid data is read from data bus This pin is for 80-pin model only
$\overline{WR}$	Write signal output	Output	Control signal output as active "L" when writing data from data bus to external component This pin is for 80-pin model only
$RESET_{OUT}$	Reset output	Output	Control signal output as active "H" during reset It is used as a reset output signal for peripheral components This pin is for 80-pin model only

BASIC FUNCTION BLOCKS

The differences between M37451M4-XXXSP/FP/GP and M37451SSP/FP/GP are noted below. Other functions are the same as M37451M4-XXXSP/FP/GP in microprocessor mode.

MEMORY

- Special Function Register (SFR) Area

The special function register (SFR) area contains the registers relating to functions such as I/O ports and timers.

- RAM

RAM is used for data storage as well as a stack area.

- Interrupt Vector Area

The interrupt vector area is for storing jump destination addresses used at reset or when an interrupt is generated. (This area must be located in ROM area)

- Zero Page

Zero page addressing mode is useful because it enables access to this area with only 2 bytes,

- Special Page

Special page addressing mode is useful because it enables access to this area with only 2 bytes.

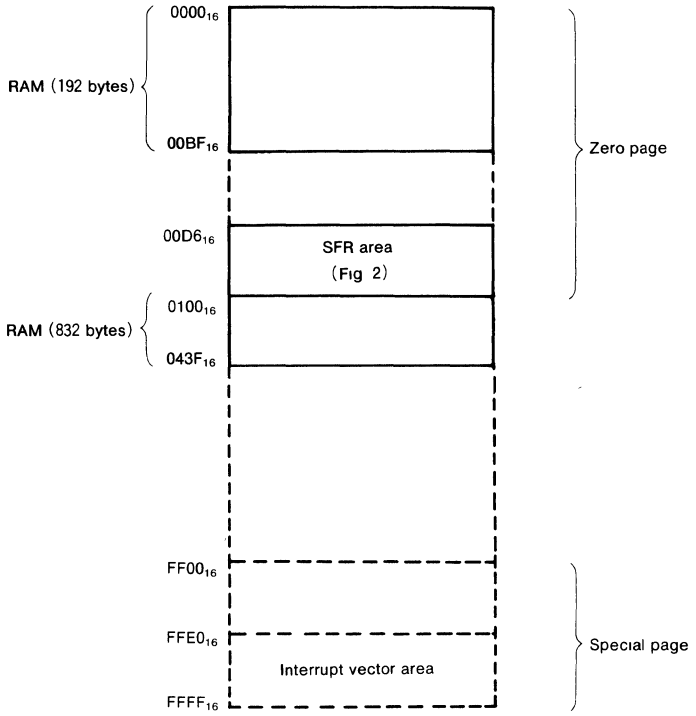


Fig. 1 Memory map

00D6$_{16}$	P3 register
00D7$_{16}$	P3 directional register
00D8$_{16}$	P4 register/PWM prescaler latch
00D9$_{16}$	Additional function register
00DA$_{16}$	P5 register
00DB$_{16}$	P5 directional register
00DC$_{16}$	P6 register
00DD$_{16}$	P6 directional register
00DE$_{16}$	MISRG1
00DF$_{16}$	MISRG2
00E0$_{16}$	D-A1 register
00E1$_{16}$	D-A2 register
00E2$_{16}$	A-D register
00E3$_{16}$	A-D control register
00E4$_{16}$	Data bus buffer register
00E5$_{16}$	Data bus buffer status register
00E6$_{16}$	Receive/transmit buffer register
00E7$_{16}$	Serial I/O status register
00E8$_{16}$	Serial I/O control register
00E9$_{16}$	UART control register
00EA$_{16}$	Baud rate generator
00EB$_{16}$	PWM register (low-order)
00EC$_{16}$	PWM register (high-order)
00ED$_{16}$	Timer 1 control register
00EE$_{16}$	Timer 2 control register
00EF$_{16}$	Timer 3 control register
00F0$_{16}$	Timer 1 register (low-order)
00F1$_{16}$	Timer 1 register (high-order)
00F2$_{16}$	Timer 1 latch (low-order)
00F3$_{16}$	Timer 1 latch (high-order)
00F4$_{16}$	Timer 2 register (low-order)
00F5$_{16}$	Timer 2 register (high-order)
00F6$_{16}$	Timer 2 latch (low-order)
00F7$_{16}$	Timer 2 latch (high-order)
00F8$_{16}$	Timer 3 register (low-order)
00F9$_{16}$	Timer 3 register (high-order)
00FA$_{16}$	Timer 3 latch (low-order)
00FB$_{16}$	Timer 3 latch (high-order)
00FC$_{16}$	Interrupt request register 1
00FD$_{16}$	Interrupt request register 2
00FE$_{16}$	Interrupt control register 1
00FF$_{16}$	Interrupt control register 2

Fig. 2 SFR (Special Function Register) memory map

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS} Output transistors are at "OFF" state	−0.3 to 7	V
V_I	Input voltage $\overline{RESET}$, X_{IN}		−0.3 to 7	V
V_I	Input voltage D_0-D_7, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, ADV_{REF}, DAV_{REF}, V_{REF}, AV_{CC}		−0.3 to V_{CC}+0.3	V
V_I	Input voltage CNV_{SS}		−0.3 to 13	V
V_O	Output voltage A_0-A_{15}, D_0-D_7, $P3_0$-$P3_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, X_{OUT}, ϕ, $\overline{RD}$, $\overline{WR}$, $R/\overline{W}$, $RESET_{OUT}$, SYNC		−0.3 to V_{CC}+0.3	V
Pd	Power dissipation	T_a = 25℃	1000 (Note 1)	mW
Topr	Operating temperature		−20 to 85	℃
Tstg	Storage temperature		−40 to 125	℃

Note 1 : 500mW for QFP type

RECOMMENDED OPERATING CONDITIONS

(V_{CC}=5V±10%, Ta=−20 to 85℃ unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage		0		V
V_{IH}	"H" input voltage $\overline{RESET}$, X_{IN}, CNV_{SS} (Note 1)	0.8V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage D_0-D_7, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$ (except Note 1)	2.0		V_{CC}	V
V_{IL}	"L" input voltage CNV_{SS} (Note 1)	0		0.2V_{CC}	V
V_{IL}	"L" input voltage D_0-D_7, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$ (except Note 1)	0		0.8	V
V_{IL}	"L" input voltage $\overline{RESET}$	0		0.12V_{CC}	V
V_{IL}	"L" input voltage X_{IN}	0		0.16V_{CC}	V
I_{OL}(peak)	"L" peak output current A_0-A_{15}, D_0-D_7, $P3_0$-$P3_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$			10	mA
I_{OL}(avg)	"L" average output current A_0-A_{15}, D_0-D_7, $P3_0$-$P3_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$ (Note 2)			5	mA
I_{OH}(peak)	"H" peak output current A_0-A_{15}, D_0-D_7, $P3_0$-$P3_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$			−10	mA
I_{OH}(avg)	"H" average output current A_0-A_{15}, D_0-D_7, $P3_0$-$P3_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$ (Note 2)			−5	mA
f(X_{IN})	Clock oscillating frequency	1		12.5	MHz

Note 1 : Ports operate as INT_1-INT_3($P6_0$-$P6_2$), EV_1-EV_3($P3_0$-$P3_2$), R_XD($P3_4$) and S_{CLK}($P3_6$)
2 : The average output current I_{OH}(avg) and I_{OL}(avg) are the average value during a 100ms
3 : The total of "L" output current I_{OL}(peak) of port P3, P5, P6, $R/\overline{W}$, SYNC, $RESET_{OUT}$, $\overline{RD}$, $\overline{WR}$ and ϕ is less than 40mA
The total of "H" output current I_{OH}(peak) of port P3, P5, P6, $R/\overline{W}$, SYNC, $RESET_{OUT}$, $\overline{RD}$, $\overline{WR}$ and ϕ is less than 40mA

ELECTRICAL CHARACTERISTICS ($V_{CC}=5V\pm10\%$, $V_{SS}=0V$, $T_a=-20$ to 85℃, $f(X_{IN})=12.5MHz$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ.	Max	
V_{OH}	"H" output voltage $\overline{RD}$, $\overline{WR}$, R/$\overline{W}$, SYNC, $RESET_{OUT}$, ϕ	$I_{OH}=-2mA$	$V_{CC}-1$			V
V_{OH}	"H" output voltage A_0-A_{15}, D_0-D_7, $P3_0$-$P3_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$	$I_{OH}=-5mA$	$V_{CC}-1$			V
V_{OL}	"L" output voltage A_0-A_{15}, D_0-D_7, $P3_0$-$P3_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $\overline{RD}$, $\overline{WR}$, R/$\overline{W}$, SYNC, $RESET_{OUT}$, ϕ	$I_{OL}=2mA$			0.45	V
V_{OL}	"L" output voltage A_0-A_{15}, D_0-D_7, $P3_0$-$P3_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$	$I_{OL}=5mA$			1	V
$V_{T+}-V_{T-}$	Hysterisis INT_1-INT_3($P6_0$-$P6_2$), EV_1-EV_3($P3_0$-$P3_2$), R_XD($P3_4$), S_{CLK}($P3_6$)	Function input level	0.3		1	V
$V_{T+}-V_{T-}$	Hysterisis $\overline{RESET}$				0.7	V
$V_{T+}-V_{T-}$	Hysterisis X_{IN}		0.1		0.5	V
I_{IL}	"L" input current D_0-D_7, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $\overline{RESET}$, X_{IN}	$V_I=V_{SS}$	−5		5	μA
I_{IH}	"H" input current D_0-D_7, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $\overline{RESET}$, X_{IN}	$V_I=V_{CC}$	−5		5	μA
V_{RAM}	RAM retention voltage	At stop mode	2			V
I_{CC}	Supply current	At system operation $f(X_{IN})=12.5MHz$		8	15	mA
		At stop mode (Note 1)		1	10	μA

Note 1 : The terminals $\overline{RD}$, $\overline{WR}$, R/$\overline{W}$, SYNC, $RESET_{OUT}$, ϕ, D-A_1 and D-A_2 are all open The other ports, which are in the input mode, are connected to V_{SS} A-D converter is in the A-D completion state The current through ADV_{REF} and DAV_{REF} is not included(Fig.7)

A-D CONVERTER CHARACTERISTICS

($V_{CC}=AV_{CC}=5V\pm10\%$, $V_{SS}=AV_{SS}=0V$, $T_a=-20$ to 85℃, $f(X_{IN})=12.5MHz$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
—	Resolution				8	Bits
—	Absolute accuracy	$V_{CC}=AV_{CC}=ADV_{REF}=5V\pm10\%$		±1.5	±3	LSB
t_{CONV}	Conversion time				49	$t_C(\phi)$
V_{IA}	Analog input voltage		AV_{SS}		AV_{CC}	V
V_{ADVREF}	Reference input voltage		2		V_{CC}	V
R_{LADDER}	Ladder resistance value	$ADV_{REF}=5V$	20	35	50	kΩ
$I_{IADVREF}$	Reference input current	$ADV_{REF}=5V$	0.1	0.14	0.25	mA
V_{AVCC}	Analog power supply input voltage			V_{CC}		V
V_{AVSS}	Analog power supply input voltage			0		V

D-A CONVERTER CHARACTERISTICS ($V_{CC}=5V\pm10\%$, $V_{SS}=AV_{SS}=0V$, $T_a=-20$ to 85℃, unless otherwise noted)

Symbol	Parameter	Test condition	Limits			Unit
			Min.	Typ	Max	
—	Resolution				8	Bits
—	Absolute accuracy	$V_{CC}=DAV_{REF}=5V\pm10\%$			1.0	%
t_{SU}	Setup time				3	μs
R_O	Output resistance		1	2	4	kΩ
V_{AVSS}	Analog power supply input voltage			0		V
V_{DAVREF}	Reference input voltage		4		V_{CC}	V
I_{DAVREF}	Reference power input current		0	5	10	mA

TIMING REQUIREMENTS

Port (V_{CC}=5V±10%, V_{SS}=0V, T_a=−20 to 85℃, unless otherwise noted)

Symbol	Parameter	Test condition	Limits			Unit
			Min	Typ	Max	
$t_{su(P3D-\phi)}$	Port P3 input setup time	Fig 3	160			ns
$t_{su(P4D-\phi)}$	Port P4 input setup time		160			ns
$t_{su(P5D-\phi)}$	Port P5 input setup time		160			ns
$t_{su(P6D-\phi)}$	Port P6 input setup time		160			ns
$t_{h(\phi-P3D)}$	Port P3 input hold time		40			ns
$t_{h(\phi-P4D)}$	Port P4 input hold time		40			ns
$t_{h(\phi-P5D)}$	Port P5 input hold time		40			ns
$t_{h(\phi-P6D)}$	Port P6 input hold time		40			ns
$t_c(X_{IN})$	External clock input cycle time		80		1000	ns
$t_w(X_{IN}L)$	External clock input "L" pulse width		20			ns
$t_w(X_{IN}H)$	External clock input "H" pulse width		20			ns
$t_r(X_{IN})$	External clock rising edge time				20	ns
$t_f(X_{IN})$	External clock falling edge time				20	ns

Master CPU bus interface timing ($\overline{R}$ and $\overline{W}$ separation type mode)

(V_{CC}=5V±10%, V_{SS}=0V, T_a=−20 to 85℃, unless otherwise noted)

Symbol	Parameter	Test condition	Limits			Unit
			Min	Typ	Max	
$t_{su(CS-R)}$	$\overline{CS}$ setup time	Fig 4	0			ns
$t_{su(CS-W)}$	$\overline{CS}$ setup time		0			ns
$t_{h(R-CS)}$	$\overline{CS}$ hold time		0			ns
$t_{h(W-CS)}$	$\overline{CS}$ hold time		0			ns
$t_{su(A-R)}$	A0 setup time		10			ns
$t_{su(A-W)}$	A0 setup time		10			ns
$t_{h(R-A)}$	A0 hold time		0			ns
$t_{h(W-A)}$	A0 hold time		0			ns
$t_{w(R)}$	Read pulse width		120			ns
$t_{w(W)}$	Write pulse width		120			ns
$t_{su(D-W)}$	Date input setup time before write		50			ns
$t_{h(W-D)}$	Date input hold time after write		0			ns

Master CPU bus interface timing ($R/\overline{W}$ type mode)

(V_{CC}=5V±10%, V_{SS}=0V, T_a=−20 to 85℃, unless otherwise noted)

Symbol	Parameter	Test condition	Limits			Unit
			Min	Typ	Max	
$t_{su(CS-E)}$	$\overline{CS}$ setup time	Fig 4	0			ns
$t_{h(E-CS)}$	$\overline{CS}$ hold time		0			ns
$t_{su(A-E)}$	A0 setup time		10			ns
$t_{h(E-A)}$	A0 hold time		0			ns
$t_{su(RW-E)}$	$R/\overline{W}$ setup time		0			ns
$t_{h(E-RW)}$	$R/\overline{W}$ hold time		0			ns
$t_{w(EL)}$	Enable clock "L" pulse width		120			ns
$t_{w(EH)}$	Enable clock "H" pulse width		120			ns
$t_{r(E)}$	Enable clock rising edge time				25	ns
$t_{f(E)}$	Enable clock falling edge time				25	ns
$t_{su(D-E)}$	Data input setup time before write		50			ns
$t_{h(E-D)}$	Data input nold time after write		0			ns

Local bus/Memory expansion mode, Microprocessor mode

(V_{CC}=5V±10%, V_{SS}=0V, T_a=−20 to 85℃, unless otherwise noted)

Symbol	Parameter	Test condition	Limits			Unit
			Min	Typ	Max	
$t_{su(D-\phi)}$	Data input setup time	Fig 5	60			ns
$t_{h(\phi-D)}$	Data input hold time		0			ns
$t_{su(D-RD)}$	Data input setup time		60			ns
$t_{h(RD-D)}$	Data input hold time		0			ns

Clock synchronous serial I/O (V_{CC}=5V±10%, V_{SS}=0V, T_a=−20 to 85℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{su(R_XD-S_{CLK})}$	Serial input setup time	Fig 6	160			ns
$t_{h(S_{CLK}-R_XD)}$	Serial input hold time		80			ns
$t_{r(R_XD)}$	Serial input rising edge time				30	ns
$t_{f(R_XD)}$	Serial input falling edge time				30	ns
$t_{r(S_{CLK})}$	Serial input clock rising edge time				30	ns
$t_{f(S_{CLK})}$	Serial input clock falling edge time				30	ns
$t_{c(S_{CLK})}$	Serial input clock period		640			ns
$t_{w(S_{CLK}L)}$	Serial input clock "L" pulse width		290			ns
$t_{w(S_{CLK}H)}$	Serial input clock "H" pulse width		290			ns

SWITCHING CHARACTERISTICS

Port (V_{CC}=5V±10%, V_{SS}=0V, T_a=−20 to 85℃, unless otherwise noted)

Symbol	Parameter	Test condition	Limits			Unit
			Min	Typ	Max	
$t_{d(\phi-P3Q)}$	Port P3 data output delay time	Fig 3			200	ns
$t_{d(\phi-P5Q)}$	Port P5 data output delay time				200	ns
$t_{d(\phi-P6Q)}$	Port P6 data output delay time				200	ns
$t_{c(\phi)}$	Cycle time		320		4000	ns
$t_{w(\phi H)}$	ϕ clock pulse width ("H" level)		150			ns
$t_{w(\phi L)}$	ϕ clock pulse width ("L" level)		130			ns
$t_{r(\phi)}$	ϕ clock rising edge time				20	ns
$t_{f(\phi)}$	ϕ clock falling edge time				20	ns

Master CPU bus interface ($\overline{R}$ and $\overline{W}$ separation type mode)

(V_{CC}=5V±10%, V_{SS}=0V, T_a=−20 to 85℃, unless otherwise noted)

Symbol	Parameter	Test condition	Limits			Unit
			Min	Typ	Max	
$t_{a(R-D)}$	Data output enable time after read	Fig 4			80	ns
$t_{v(R-D)}$	Data output disable time after read		0		30	ns
$t_{PLH(R-PR)}$	$\overline{P_{RDY}}$ output transmission time after read				150	ns
$t_{PLH(W-PR)}$	$\overline{P_{RDY}}$ output transmission time after write				150	ns

Master CPU bus interface (R/$\overline{W}$ type mode) (V_{CC}=5V±10%, V_{SS}=0V, T_a=−20 to 85℃, unless otherwise noted)

Symbol	Parameter	Test condition	Limits			Unit
			Min	Typ	Max	
$t_{a(E-D)}$	Data output enable time after read	Fig 4			80	ns
$t_{v(E-D)}$	Data output disable time after read		0		30	ns
$t_{PLH(E-PR)}$	$\overline{P_{RDY}}$ output transmission time after E clock				150	ns

Local bus/Memory expansion mode, microprocessor mode

(V_{CC}=5V±10%, V_{SS}=0V, T_a=−20 to 85℃, unless otherwise noted)

Symbol	Parameter	Test condition	Limits			Unit
			Min	Typ	Max	
$t_{d(\phi-A)}$	Address delay time after ϕ	Fig 5			80	ns
$t_{v(\phi-A)}$	Address effective time after ϕ		10			ns
$t_{v(RD-A)}$	Address effective time after $\overline{RD}$		10			ns
$t_{v(WR-A)}$	Address effective time after $\overline{WR}$		10			ns
$t_{d(\phi-D)}$	Data output delay time after ϕ				80	ns
$t_{d(WR-D)}$	Data output delay time after $\overline{WR}$				80	ns
$t_{v(\phi-D)}$	Data output effective time after ϕ		20			ns
$t_{v(WR-D)}$	Data output effective time after $\overline{WR}$		20			ns
$t_{d(\phi-RW)}$	R/$\overline{W}$ delay time after ϕ				80	ns
$t_{d(\phi-SYNC)}$	SYNC delay time after ϕ				80	ns
$t_{W(RD)}$	$\overline{RD}$ pulse width		130			ns
$t_{W(WR)}$	$\overline{WR}$ pulse width		130			ns

Clock synchronous serial I/O (V_{CC}=5V±10%, V_{SS}=0V, T_a=−20 to 85℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{d(S_{CLK}-T_XD)}$	Serial output delay time	Fig 6			100	ns
$t_{r(S_{CLK})}$	Serial output clock rising edge time				30	ns
$t_{f(S_{CLK})}$	Serial output clock falling edge time				30	ns
$t_{C(S_{CLK})}$	Serial output clock period		640			ns
$t_{W(S_{CLK}L)}$	Serial output clock "L" pulse width		290			ns
$t_{W(S_{CLK}H)}$	Serial output clock "H" pulse width		290			ns

TEST CONDITION

Input voltage level : V_{IH} 2.4V

V_{IL} 0.45V

Output test level : V_{OH} 2.0V

V_{OL} 0.8V

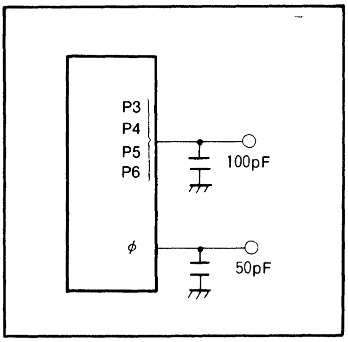


Fig. 3 Port test circuit

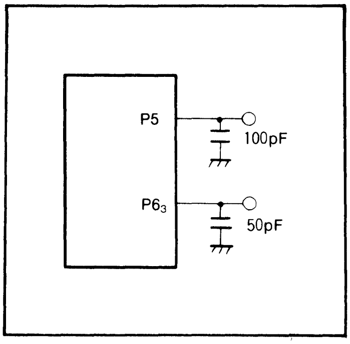


Fig. 4 Master CPU bus interface test circuit

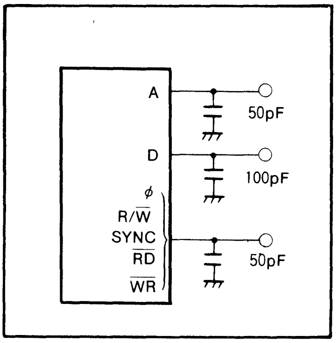


Fig. 5 Local bus test circuit

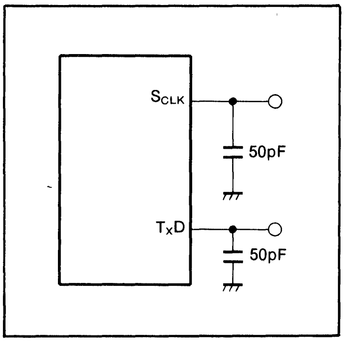


Fig. 6 Serial I/O test circuit

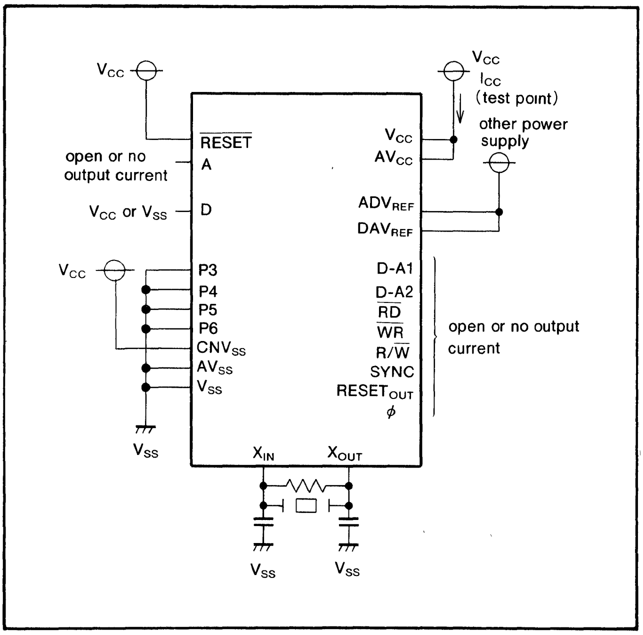
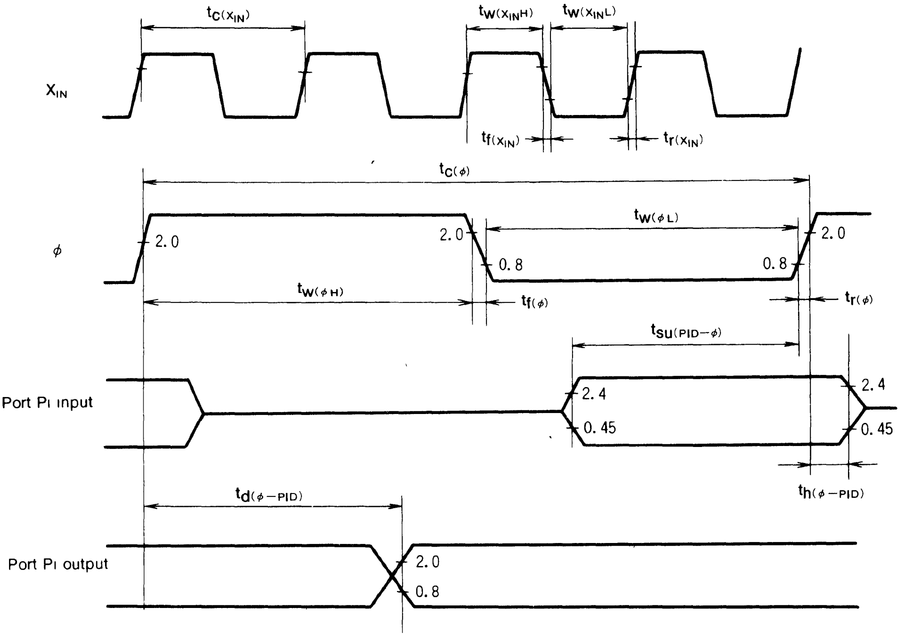


Fig. 7 I_{CC} (at stop mode) test condition

TIMING DIAGRAM

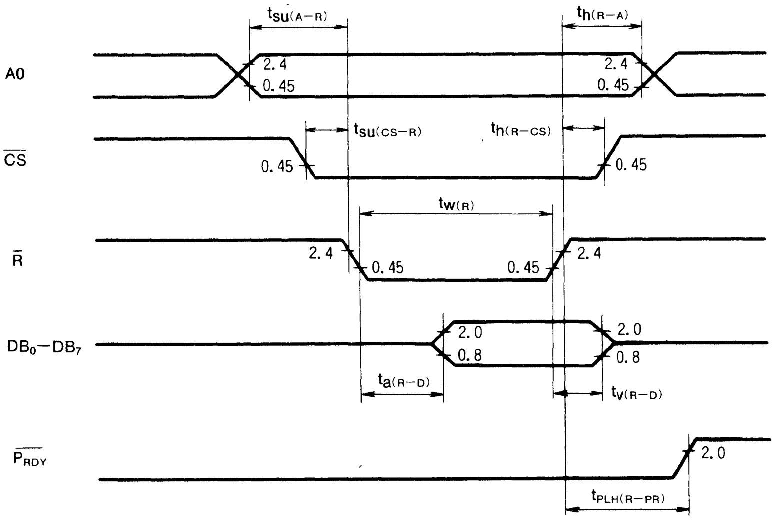
Port/single-chip mode timing diagram



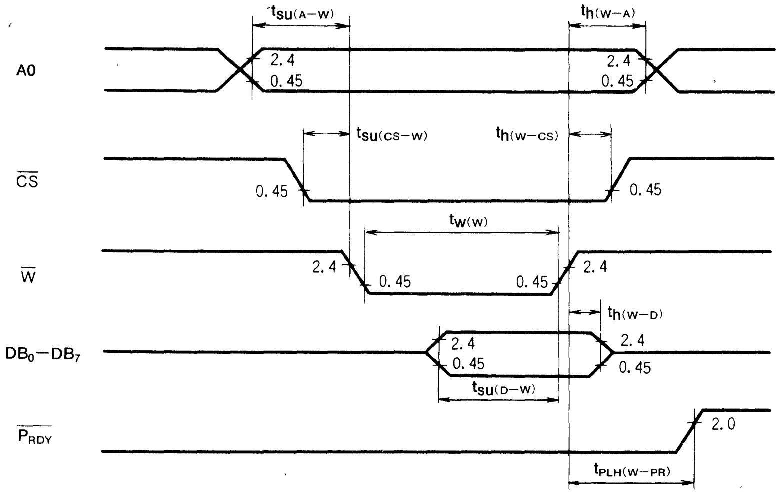
Note : V_{IH}=0. 8V_{CC}, V_{IL}=0. 16V_{CC} of X_{IN}

Master CPU bus interface/ $\overline{R}$ and $\overline{W}$ separation type timing diagram

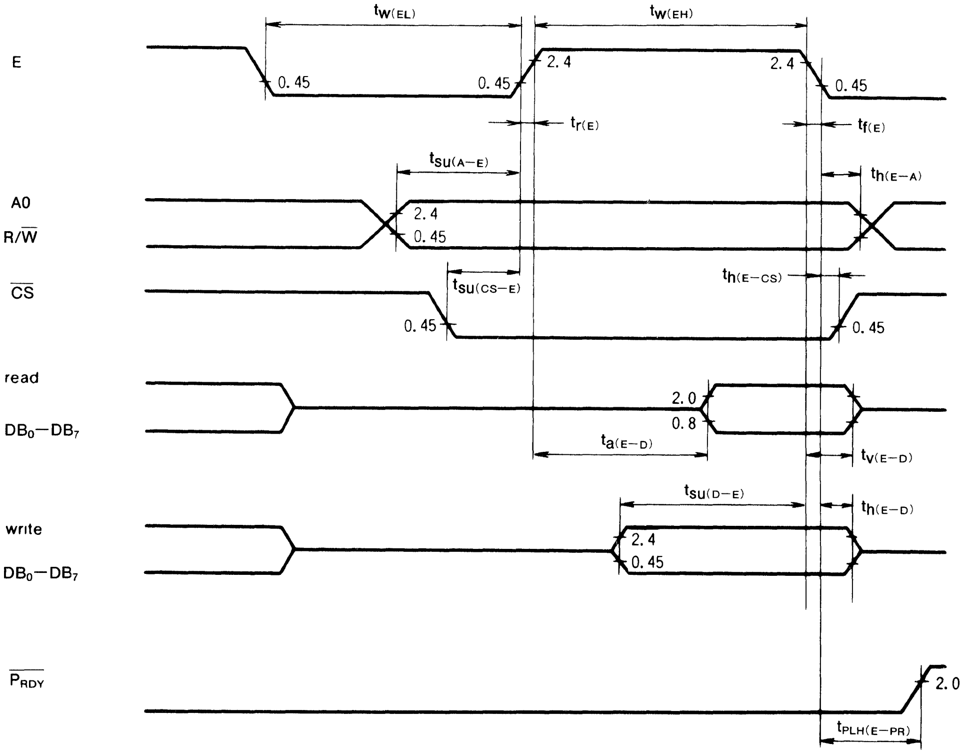
Read



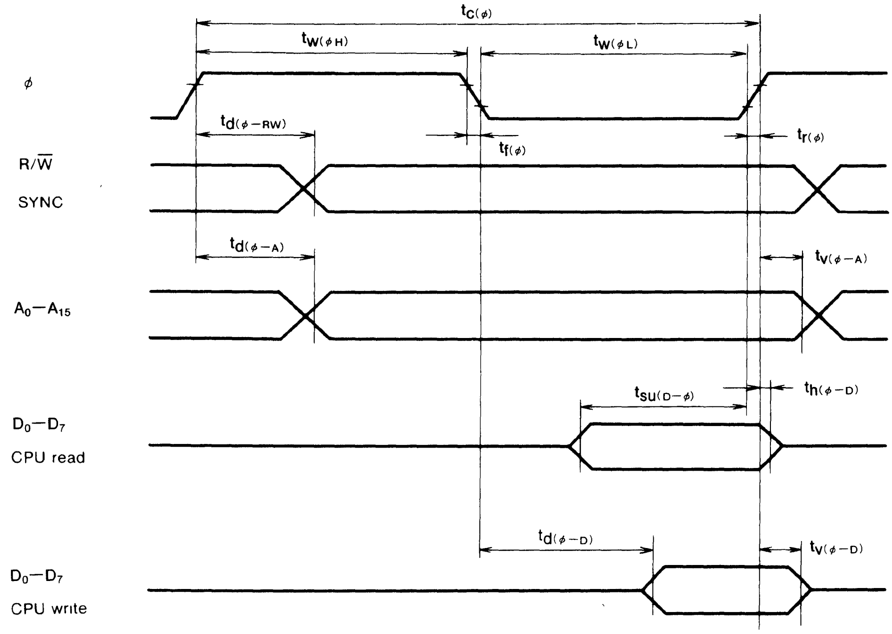
Write

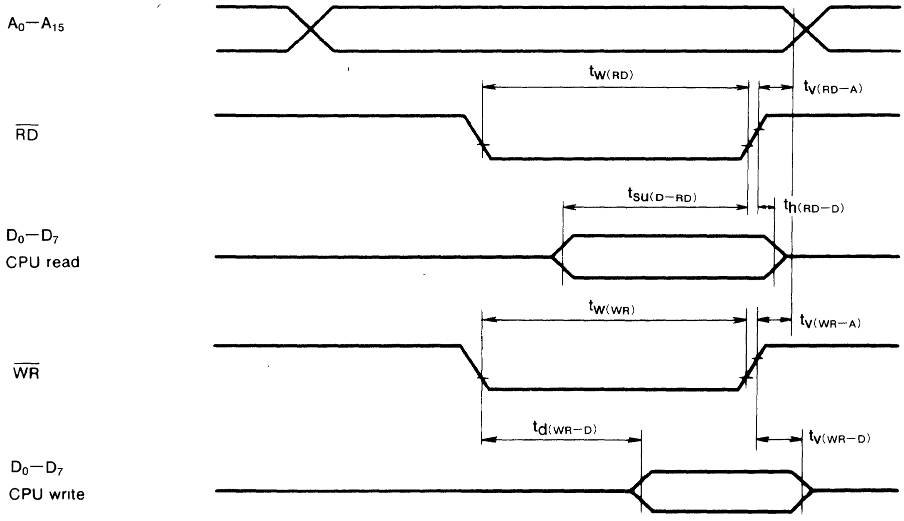


Master CPU interface/ R/W type timing diagram

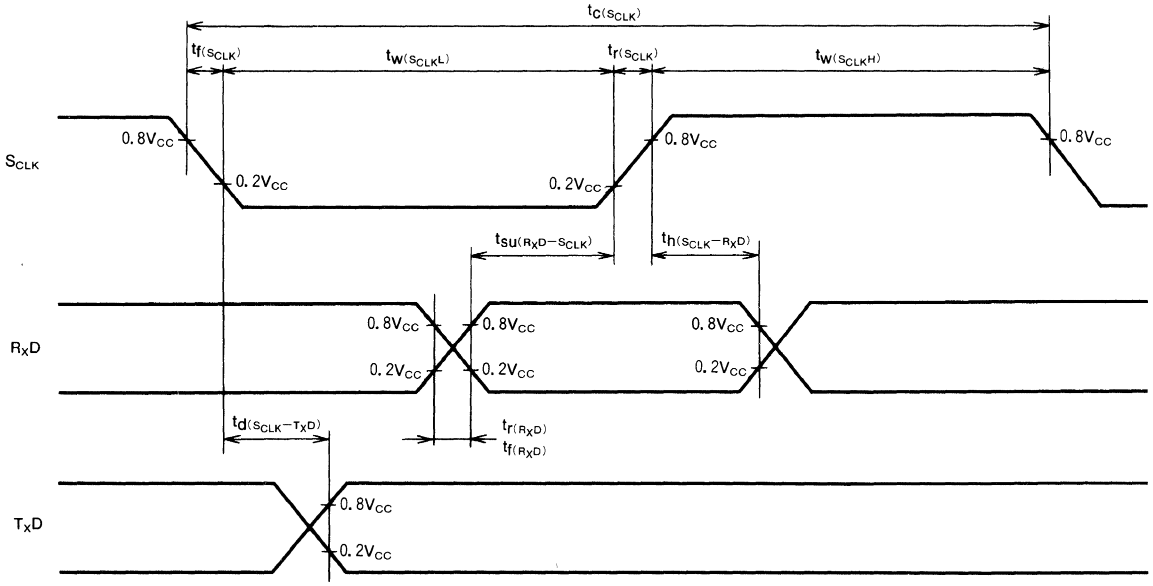


Local bus timing diagram





Clock synchronous serial I/O timing diagram



MITSUBISHI MICROCOMPUTERS

M37450M4TXXXSP/J

EXTENDED OPERATING TEMPERATURE VERSION of M37450M4-XXXSP

DESCRIPTION

The M37450M4TXXXSP/J is a single-chip microcomputer designed with CMOS sillicon gate technology. It is housed in a 64-pin shrink plastic molded DIP or an 84-pin plastic molded QFJ (PLCC).

In addition to its simple instruction sets, the ROM, RAM, and I/O addresses are placed on the same memory map to enable easy programming.

It is suited for office automation equipment and control devices The low power consumption made by the use of a CMOS process makes it especially suitable for battery powered devices requiring low power consumption. It also has a unique feature that enables it to be used as a slave microcomputer.

The differences between the M37450M4TXXXSP/J and the M37450M4-XXXSP/FP are some electrical characteristics, the expansion of operating temperature range, and the package.

The number of analog input pins for the 84-pin PLCC (J version) is different from the 64-pin model (SP version). In addition, the 84-pin model has special pins for $\overline{RD}$, $\overline{WR}$, $RESET_{OUT}$, DAV_{REF}, ADV_{REF}, AV_{CC} and the 64-pin model has a special V_{REF} pin.

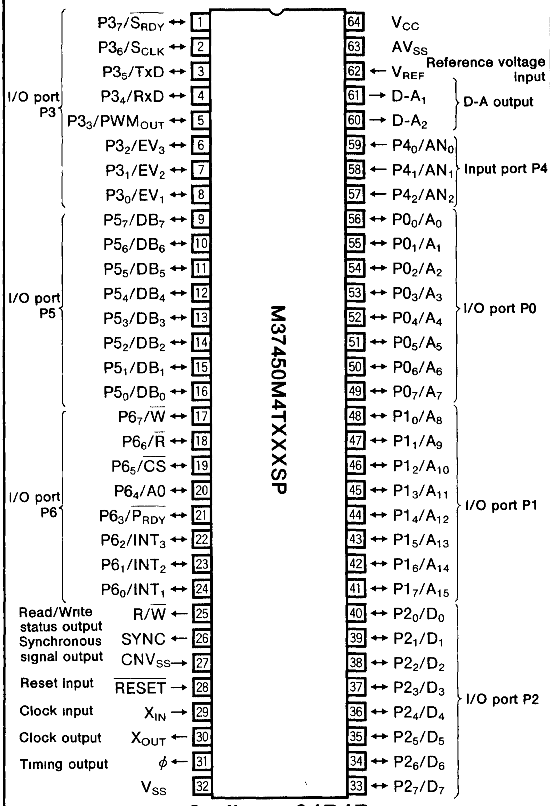
FEATURES

- Number of basic instructions ………………………… 71
  69 MELPS 740 basic instructions+2 multiply/divide instructions
- Memory size
  - ROM ………………………… 8192 bytes
  - RAM ………………………… 256 bytes
- Instruction execution time
  (minimum instructions at 10MHz frequency) ……… 0.8μs
- Single power supply ………………………… 5V±10%
- Power dissipation normal operation mode
  (at 10MHz frequency) ………………………… 30mW
- Subroutine nesting ………………………… 96 levels max
- Interrupt ………………………… 15 events
- Master CPU interface ………………………… 1 byte
- 16-bit timer ………………………… 3
- 8-bit timer (Serial I/O use) ………………………… 1
- Serial I/O (UART or clock synchronous) ………………… 1
- A-D converter (8-bit resolution) ……… 3 channels (DIP)
  8 channels (QFJ)
- D-A converter (8-bit resolution) ……………… 2 channels
- PWM output (8 bit or 16 bit) ………………………… 1
- Programmable I/O ports
  (Ports P0, P1, P2, P3, P5, P6) ………………………… 48
- Input port (Port P4) ………………………… 3(DIP), 8(QFJ)
- Output ports (Ports D-A$_1$, D-A$_2$) ………………………… 2

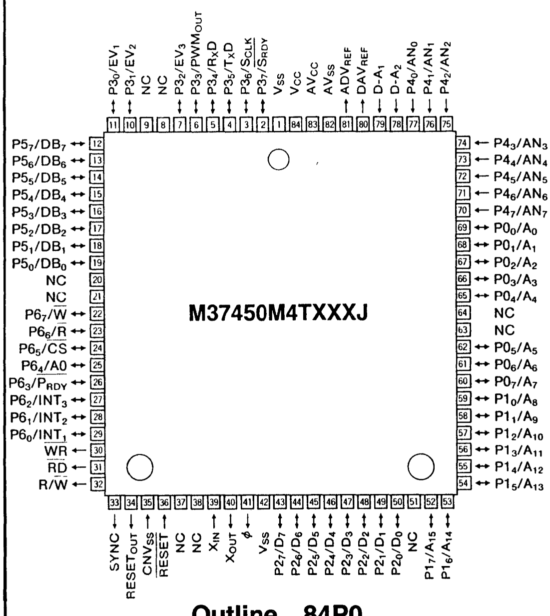
APPLICATION

Slave controller for PPCs, facsimiles, and page printers.
HDD, optical disk, inverter, and industrial motor controllers.
Industrial robots and machines.

PIN CONFIGURATION (TOP VIEW)



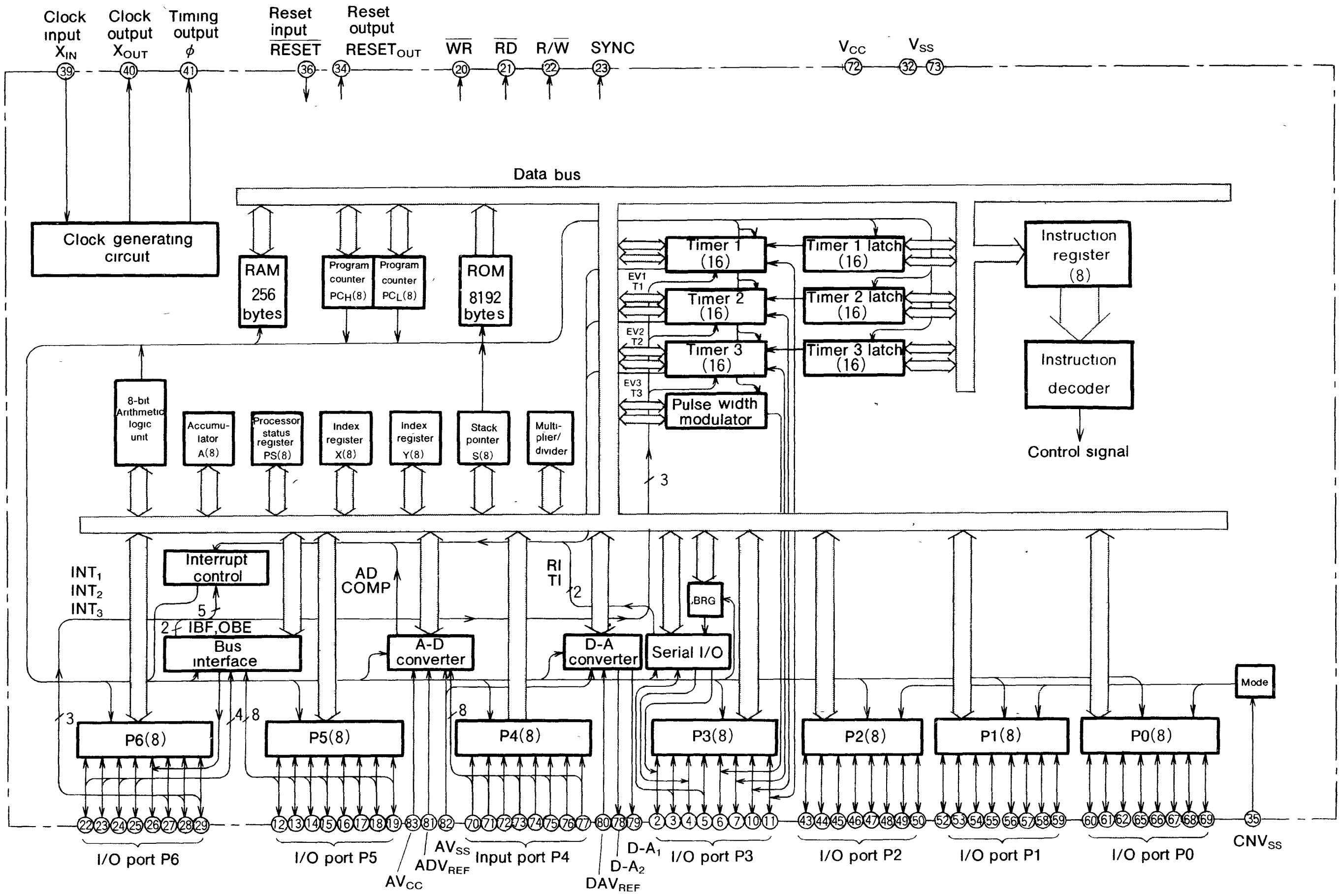
Outline 64P4B



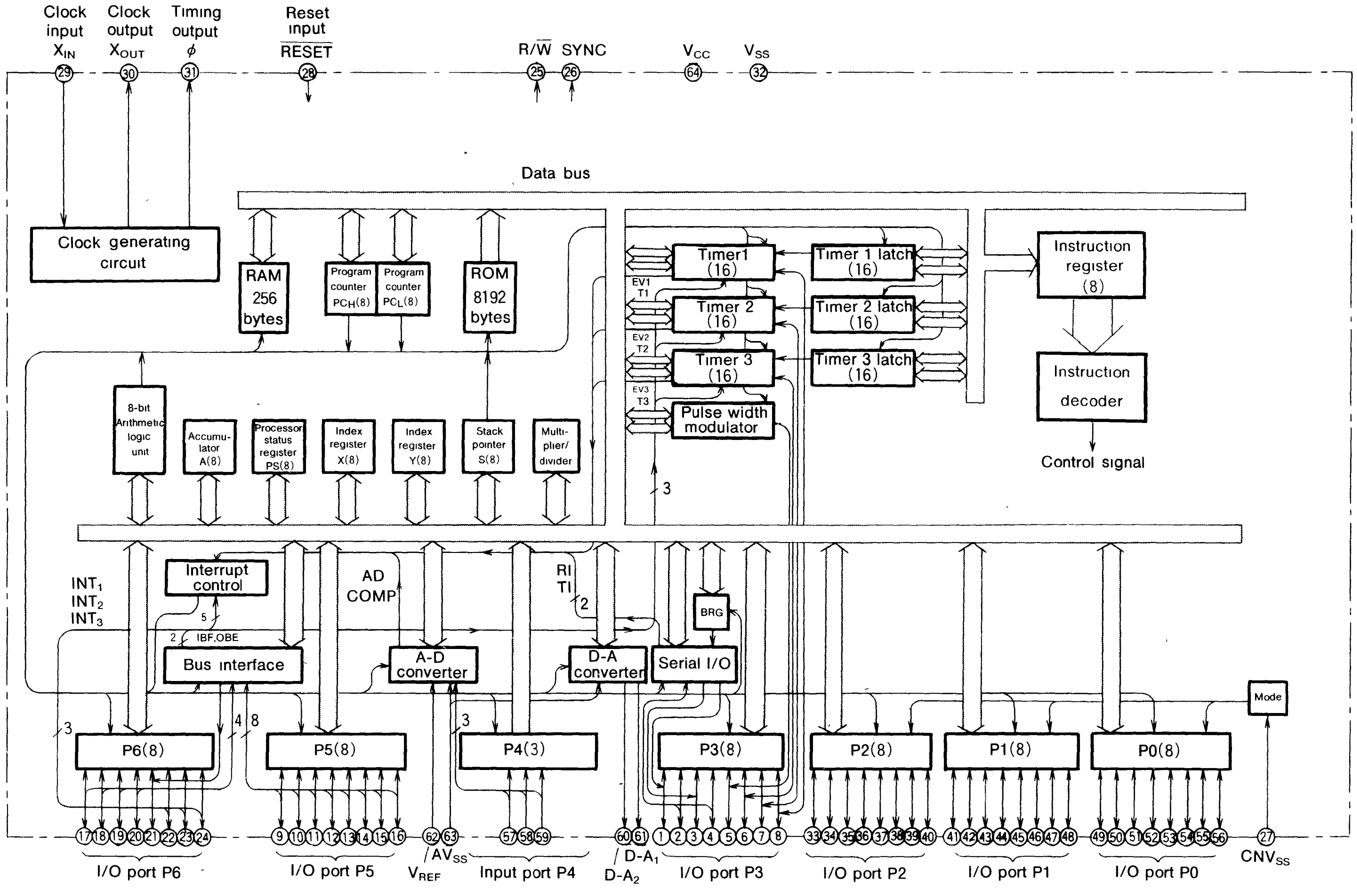
Outline 84P0

NC : No connection

M37450M4TXXXJ BLOCK DIAGRAM



M37450M4TXXXSP BLOCK DIAGRAM



FUNCTIONS OF M37450M4TXXXSP/J

Parameter			Functions
Number of basic instructions			71(69 MELPS 740 basic instructions+2)
Instruction execution time			0.8μs (minimum instructions, at 10MHz of frequency)
Clock frequency			10MHz (max.)
Memory size	ROM		8192 bytes
	RAM		256 bytes
Input/Output ports	P0-P3, P5, P6	I/O	8-bit×6
	P4	Input	3-bit×1 (8-bit×1 for 84-pin model)
	D-A	Output	2-bit×1
Serial I/O			UART or clock synchronous
Timers			16-bit timer×3, 8-bit timer (serial I/O baud rate generator)×1
A-D converter			8-bit×3 channels (8 channels for 84-pin model)
D-A converter			8-bit×2 channels
Pulse width modulator			8-bit or 16-bit×1
Data bus buffer			1-byte input and output each
Subroutine nesting			96-levels (max.)
Interrupt			6 external interrupts, 8 internal interrupts 1 software interrupt
Clock generating circuit			Built-in (ceramic or quarts crystal oscillator)
Supply voltage			5V±10%
Power dissipation			30mW (at 10MHz frequency)
Input/Output characters	Input/Output voltage		5V
	Output current		±5mA (max.)
Memory expansion			Possible
Operating temperature range			−40 to 85℃
Device structure			CMOS silicon gate
Package	M37450M4TXXXSP		64-pin shrink plastic molded DIP
	M37450M4TXXXJ		84-pin plastic molded QFJ (PLCC)

PIN DESCRIPTION

Pin	Name	Input/ Output	Functions
V_{CC}, V_{SS}	Supply voltage		Power supply inputs 5V±10% to V_{CC}, and 0V to V_{SS}
CNV_{SS}	CNV_{SS}		Controls the processor mode of the chip Normally connected to V_{SS} or V_{CC}
$\overline{RESET}$	Reset input	Input	To enter the reset state, the reset input pin must be kept at a "L" for more than 8 clock cycles (under normal V_{CC} conditions) If more time is needed for the crystal oscillator to stabilize, this "L" condition should be maintained for the required time
X_{IN}	Clock input	Input	This chip has an internal clock generating circuit To control generating frequency, an external ceramic or a quartz crystal oscillator is connected between the X_{IN} and X_{OUT} pins If an external clock is used, the clock source should be connected to the X_{IN} pin and the X_{OUT} pin should be left open.
X_{OUT}	Clock output	Output	
ϕ	Timing output	Output	Outputs signal consisting of oscillating frequency divided by four
SYNC	Synchronous signal output	Output	This signal is output "H" during operation code fetch and is used to control single stepping of programs
$R/\overline{W}$	Read/Write status output	Output	This signal determines the direction of the data bus It is "H" during read and "L" during write
$P0_0$-$P0_7$	I/O port P0	I/O	Port P0 is an 8-bit I/O port with directional registers allowing each I/O bit to be individually programmed as input or output The output structure is CMOS output The low-order bits of the address are output except in single-chip mode
$P1_0$-$P1_7$	I/O port P1	I/O	Port P1 is an 8-bit I/O port and has basically the same functions as port P0 The high-order bits of the address are output except in single-chip mode
$P2_0$-$P2_7$	I/O port P2	I/O	Port P2 is an 8-bit I/O port and has basically the same functions as port P0 Used as data bus except in single-chip mode
$P3_0$-$P3_7$	I/O port P3	I/O	Port P3 is an 8-bit I/O port and has basically the same functions as port P0 Serial I/O, PWM output, or event I/O function can be selected with a program
$P4_0$-$P4_2$ ($P4_0$-$P4_7$)	Input port P4	Input	Analog input pin for the A-D converter The 64-pin model has three pins and the 84-pin model has eight pins They may also be used as digital input pins
$P5_0$-$P5_7$	I/O port P5	I/O	Port P5 is an 8-bit I/O port and has basically the same functions as port P0 This port functions as an 8-bit data bus for the master CPU when slave mode is selected with a program
$P6_0$-$P6_7$	I/O port P6	I/O	Port P6 is an 8-bit I/O port and has basically the same function as port P0 Pins $P6_3$ to $P6_7$ change to a control bus for the master CPU when slave mode is selected with a program Pins $P6_0$ to $P6_2$ may be programmed as external interrupt input pins
D-A_1, D-A_2	D-A output	Output	Analog signal from D-A converter is output
V_{REF}	Reference voltage input	Input	Reference voltage input pin for A-D and D-A converter This pin is for 64-pin model only
ADV_{REF}	A-D reference voltage input	Input	Reference voltage input pin for A-D converter This pin is for 84-pin model only
DAV_{REF}	D-A reference voltage input	Input	Reference voltage input pin for D-A converter This pin is for 84-pin model only
AV_{SS}	Analog power supply		Ground level input pin for A-D and D-A converter Same voltage as V_{SS} is applied
AV_{CC}	Analog power supply		Power supply input pin for A-D converter This pin is for 84-pin model only Same voltage as V_{CC} is applied In the case of the 64-pin model, AV_{CC} is connected to V_{CC} internally
$\overline{RD}$	Read signal output	Output	Control signal output as active "L" when valid data is read from data bus This pin is for 84-pin model only
$\overline{WR}$	Write signal output	Output	Control signal output as active "L" when writing data from data bus to external component This pin is for 84-pin model only
$RESET_{OUT}$	Reset output	Output	Control signal output as active "H" during reset It is used as a reset output signal for peripheral components This pin is for 84-pin model only

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS} Output transistors are at "off" state	−0.3 to 7	V
V_I	Input voltage X_{IN}, $\overline{RESET}$		−0.3 to 7	V
V_I	Input voltage $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, ADV_{REF}, DAV_{REF}, V_{REF}, AV_{CC}		−0.3 to V_{CC}+0.3	V
V_I	Input voltage CNV_{SS}		−0.3 to 13	V
V_O	Output voltage $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, X_{OUT}, ϕ $R/\overline{W}$, $\overline{RD}$, $\overline{WR}$, SYNC, $RESET_{OUT}$		−0.3 to V_{CC}+0.3	V
P_d	Power dissipation	T_a = 25℃	1000	mW
Topr	Operating temperature		−40 to 85	℃
Tstg	Storage temperature		−65 to 150	℃

RECOMMENDED OPERATING CONDITIONS

(V_{CC}=5V±10%, Ta=−40 to 85℃ unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage		0		V
V_{IH}	"H" input voltage $\overline{RESET}$, X_{IN}, CNV_{SS} (Note 1)	0.8V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$ (expect Note 1)	2.0		V_{CC}	V
V_{IL}	"L" input voltage CNV_{SS} (Note 1)	0		0.2V_{CC}	V
V_{IL}	"L" input voltage $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$ (expect Note 1)	0		0.8	V
V_{IL}	"L" input voltage $\overline{RESET}$	0		0.12V_{CC}	V
V_{IL}	"L" input voltage X_{IN}	0		0.16V_{CC}	V
$I_{OL(peak)}$	"L" peak output current $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$			10	mA
$I_{OL(avg)}$	"L" average output current $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$ (Note 2)			5	mA
$I_{OH(peak)}$	"H" peak output current $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$			−10	mA
$I_{OH(avg)}$	"H" average output current $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$ (Note 2)			−5	mA
$f(X_{IN})$	Internal clock oscillating frequency	1		10	MHz

Note 1 : Ports operating as special function pins INT_1-INT_3($P6_0$-$P6_2$), EV_1-EV_3($P3_0$-$P3_2$), R_XD($P3_4$), S_{CLK}($P3_6$)

2 : $I_{OL(avg)}$ and $I_{OH(avg)}$ are the average current in 100ms.

3 : The total of I_{OL} of Port P0, P1 and P2 should be 40mA (max)
The total of I_{OL} of Port P3, P5, P6, $R/\overline{W}$, SYNC, $RESET_{OUT}$, $\overline{RD}$, $\overline{WR}$ and ϕ should be 40mA (max)
The total of I_{OH} of Port P0, P1, and P2 should be 40mA (max)
The total of I_{OH} of Port P3, P5, P6, $R/\overline{W}$, SYNC, $RESET_{OUT}$, $\overline{RD}$, $\overline{WR}$, and ϕ should be 40mA (max)

ELECTRIC CHARACTERISTICS (V_{CC}=5V±10%, V_{SS}= 0 V, T_a=−40 to 85℃, f(X_{IN})=10MHz)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ.	Max.	
V_{OH}	"H" output voltage $\overline{RD}$, $\overline{WR}$, R/$\overline{W}$, SYNC, $RESET_{OUT}$, ϕ	I_{OH} =− 2 mA	V_{CC}−1			V
V_{OH}	"H" output voltage $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$	I_{OH} =− 5 mA	V_{CC}−1			V
V_{OL}	"L" output voltage $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $\overline{RD}$, $\overline{WR}$, R/$\overline{W}$, SYNC, $RESET_{OUT}$, ϕ	I_{OL} =2 mA			0. 45	V
V_{OL}	"L" output voltage $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$	I_{OL} =5 mA			1	V
$V_{T+}-V_{T-}$	Hysteresis INT_1-INT_3($P6_0$-$P3_2$), EV_1-EV_3($P3_0$-$P3_2$), R_XD($P3_4$), S_{CLK}($P3_6$)	Function input level	0. 3		1	V
$V_{T+}-V_{T-}$	Hysteresis $\overline{RESET}$				0. 7	V
$V_{T+}-V_{T-}$	Hysteresis X_{IN}		0. 1		0. 5	V
I_{IL}	"L" input current $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $\overline{RESET}$, X_{IN}	V_I =V_{SS}	−5		5	μA
I_{IH}	"H" input current $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $\overline{RESET}$, X_{IN}	V_I =V_{CC}	−5		5	μA
V_{RAM}	RAM retention voltage	At stop mode	2			V
I_{CC}	Supply current	f(X_{IN})=10MHz At system operation		6	15	mA
		At stop mode (Note 1)		1	10	μA

Note 1 : The terminals $\overline{RD}$, $\overline{WR}$, SYNC, R/$\overline{W}$, $RESET_{OUT}$, ϕ, D-A_1 and D-A_2 are all open The other ports, which are in the input mode, are connected to V_{SS} A-D converter is in the A-D completion state The current through ADV_{REF} and DAV_{REF} is not included (Fig 4)

A-D CONVERTER CHARACTERISTICS

(V_{CC}=AV_{CC}= 5 V±10%, V_{SS}=AV_{SS}= 0 V, T_a=−40 to 85℃, f(X_{IN})=10MHz unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
—	Resolution				8	Bits
—	Absolute accuracy	V_{CC}=AV_{CC}=ADV_{REF}=5V±10%		±1. 5	±3	LSB
t_{CONV}	Conversion time				49	$t_{c(\phi)}$
V_{IA}	Analog input voltage		AV_{SS}		AV_{CC}	V
V_{ADVREF}	Reference input voltage		2		V_{CC}	V
R_{LADDER}	Ladder resistance value	ADV_{REF}= 5 V	2	7. 5	10	kΩ
$I_{IADVREF}$	Reference input current	ADV_{REF}= 5 V	0. 5	0. 7	2. 5	mA
V_{AVCC}	Analog power supply input voltage			V_{CC}		V
V_{AVSS}	Analog power supply input voltage			0		V

D-A CONVERTER CHARACTERISTICS (V_{CC}= 5 V±10%, V_{SS}=AV_{SS}= 0 V, T_a=−40 to 85℃ unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
—	Resolution				8	Bits
—	Full scale deviation	V_{CC}=DAV_{REF}=5V			1. 0	%
t_{SU}	Set time				3	μs
R_O	Output resistance		1	2	4	kΩ
V_{AVSS}	Analog power supply input voltage			0		V
V_{DAVREF}	Reference input voltage		4		V_{CC}	V
I_{DAVREF}	Reference power input current (Each pin)		0	2. 5	5	mA

TIMING REQUIREMENTS

Port/single-chip mode (V_{CC}=5V±10%, V_{SS}=0V, T_a=−40 to 85℃, unless otherwise noted)

Symbol	Parameter	Test condition	Limits			Unit
			Min.	Typ	Max.	
$t_{su(P0D-\phi)}$	Port P0 input setup time	Fig.1	200			ns
$t_{su(P1D-\phi)}$	Port P1 input setup time		200			ns
$t_{su(P2D-\phi)}$	Port P2 input setup time		200			ns
$t_{su(P3D-\phi)}$	Port P3 input setup time		200			ns
$t_{su(P4D-\phi)}$	Port P4 input setup time		200			ns
$t_{su(P5D-\phi)}$	Port P5 input setup time		200			ns
$t_{su(P6D-\phi)}$	Port P6 input setup time		200			ns
$t_{h(\phi-P0D)}$	Port P0 input hold time		40			ns
$t_{h(\phi-P1D)}$	Port P1 input hold time		40			ns
$t_{h(\phi-P2D)}$	Port P2 input hold time		40			ns
$t_{h(\phi-P3D)}$	Port P3 input hold time		40			ns
$t_{h(\phi-P4D)}$	Port P4 input hold time		40			ns
$t_{h(\phi-P5D)}$	Port P5 input hold time		40			ns
$t_{h(\phi-P6D)}$	Port P6 input hold time		40			ns
$t_c(X_{IN})$	External clock input cycle time		100		1000	ns
$t_w(X_{IN}L)$	External clock input "L" pulse width		30			ns
$t_w(X_{IN}H)$	External clock input "H" pulse width		30			ns
$t_r(X_{IN})$	External clock rising edge time				20	ns
$t_f(X_{IN})$	External clock falling edge time				20	ns

Master CPU bus interface timing ($\overline{R}$ and $\overline{W}$ separation type mode)

(V_{CC}=5V±10%, V_{SS}=0V, T_a=−40 to 85℃, unless otherwise noted)

Symbol	Parameter	Test condition	Limits			Unit
			Min.	Typ	Max	
$t_{su(CS-R)}$	$\overline{CS}$ setup time	Fig 2	0			ns
$t_{su(CS-W)}$	$\overline{CS}$ setup time		0			ns
$t_{h(R-CS)}$	$\overline{CS}$ hold time		0			ns
$t_{h(W-CS)}$	$\overline{CS}$ hold time		0			ns
$t_{su(A-R)}$	A0 setup time		40			ns
$t_{su(A-W)}$	A0 setup time		40			ns
$t_{h(R-A)}$	A0 hold time		10			ns
$t_{h(W-A)}$	A0 hold time		10			ns
$t_{w(R)}$	Read pulse width		160			ns
$t_{w(W)}$	Write pulse width		160			ns
$t_{su(D-W)}$	Date input setup time before write		100			ns
$t_{h(W-D)}$	Date input hold time after write		10			ns

Master CPU bus interface timing (R/$\overline{W}$ type mode)

(V_{CC}=5V±10%, V_{SS}=0V, T_a=−40 to 85℃, unless otherwise noted)

Symbol	Parameter	Test condition	Limits			Unit
			Min	Typ	Max	
$t_{su(CS-E)}$	$\overline{CS}$ setup time	Fig 2	0			ns
$t_{h(E-CS)}$	$\overline{CS}$ hold time		0			ns
$t_{su(A-E)}$	A0 setup time		40			ns
$t_{h(E-A)}$	A0 hold time		10			ns
$t_{su(RW-E)}$	R/$\overline{W}$ setup time		40			ns
$t_{h(E-RW)}$	R/$\overline{W}$ hold time		10			ns
$t_{w(EL)}$	Enable clock "L" pulse width		160			ns
$t_{w(EH)}$	Enable clock "H" pulse width		160			ns
$t_{r(E)}$	Enable clock rising edge time				25	ns
$t_{f(E)}$	Enable clock falling edge time				25	ns
$t_{su(D-E)}$	Data input setup time before write		100			ns
$t_{h(E-D)}$	Data input hold time after write		10			ns

Local bus/memory expansion mode, microprocessor mode

(V_{CC}=5V±10%, V_{SS}=0V, T_a=−40 to 85℃, unless otherwise noted)

Symbol	Parameter	Test condition	Limits			Unit
			Min	Typ.	Max	
$t_{su(D-\phi)}$	Data input setup time	Fig 3	130			ns
$t_{h(\phi-D)}$	Data input hold time		0			ns
$t_{su(D-RD)}$	Data input setup time		130			ns
$t_{h(RD-D)}$	Data input hold time		0			ns

SWITCHING CHARACTERISTICS

Port/single-chip mode (V_{CC}=5V±10%, V_{SS}=0V, T_a=−40 to 85℃, unless otherwise noted)

Symbol	Parameter	Test condition	Limits			Unit
			Min	Typ	Max	
$t_{d(\phi-P0Q)}$	Port P0 data output delay time	Fig.3			200	ns
$t_{d(\phi-P1Q)}$	Port P1 data output delay time				200	ns
$t_{d(\phi-P2Q)}$	Port P2 data output delay time				200	ns
$t_{d(\phi-P3Q)}$	Port P3 data output delay time				200	ns
$t_{d(\phi-P5Q)}$	Port P5 data output delay time				200	ns
$t_{d(\phi-P6Q)}$	Port P6 data output delay time				200	ns
$t_{c(\phi)}$	Cycle time		400		4000	ns
$t_{w(\phi H)}$	ϕ clock pulse width ("H" level)		190			ns
$t_{w(\phi L)}$	ϕ clock pulse width ("L" level)		170			ns
$t_{r(\phi)}$	ϕ clock rising edge time				20	ns
$t_{f(\phi)}$	ϕ clock falling edge time				20	ns

Master CPU bus interface ($\overline{R}$ and $\overline{W}$ separation type mode)

(V_{CC}=5V±10%, V_{SS}=0V, T_a=−40 to 85℃, unless otherwise noted)

Symbol	Parameter	Test condition	Limits			Unit
			Min	Typ	Max	
$t_{a(R-D)}$	Data output enable time after read	Fig.4			120	ns
$t_{v(R-D)}$	Data output disable time after read		10		85	ns
$t_{PLH(R-PR)}$	$\overline{P}_{RDY}$ output transmission time after read				150	ns
$t_{PLH(W-PR)}$	$\overline{P}_{RDY}$ output transmission time after write				150	ns

Master CPU bus interface (R/$\overline{W}$ type mode) (V_{CC}=5V±10%, V_{SS}=0V, T_a=−40 to 85℃, unless otherwise noted)

Symbol	Parameter	Test condition	Limits			Unit
			Min	Typ	Max	
$t_{a(E-D)}$	Data output enable time after read	Fig 4			120	ns
$t_{v(E-D)}$	Data output disable time after read		10		85	ns
$t_{PLH(E-PR)}$	$\overline{P}_{RDY}$ output transmission time after E clock				150	ns

Local bus/memory expansion mode, microprocessor mode

(V_{CC}=5V±10%, V_{SS}=0V, T_a=−40 to 85℃, unless otherwise noted)

Symbol	Parameter	Test condition	Limits			Unit
			Min	Typ.	Max	
$t_{d(\phi-A)}$	Address delay time after ϕ	Fig.40			150	ns
$t_{v(\phi-A)}$	Address effective time after ϕ		10			ns
$t_{v(RD-A)}$	Address effective time after $\overline{RD}$		10			ns
$t_{v(WR-A)}$	Address effective time after $\overline{WR}$		10			ns
$t_{d(\phi-D)}$	Data output delay time after ϕ				160	ns
$t_{d(WR-D)}$	Data output delay time after $\overline{WR}$				160	ns
$t_{v(\phi-D)}$	Data output effective time after ϕ		20			ns
$t_{v(WR-D)}$	Data output effective time after $\overline{WR}$		20			ns
$t_{d(\phi-RW)}$	R/$\overline{W}$ delay time after ϕ				150	ns
$t_{d(\phi-SYNC)}$	SYNC delay time after ϕ				150	ns
$t_{w(RD)}$	$\overline{RD}$ pulse width		170			ns
$t_{w(WR)}$	$\overline{WR}$ pulse width		170			ns

TEST CONDITION

Input voltage level : V_{IH} 2.4V

V_{IL} 0.45V

Output test level : V_{OH} 2.0V

V_{OL} 0.8V

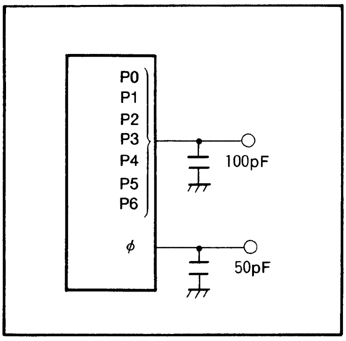


Fig. 1 Test circuit in single-chip mode

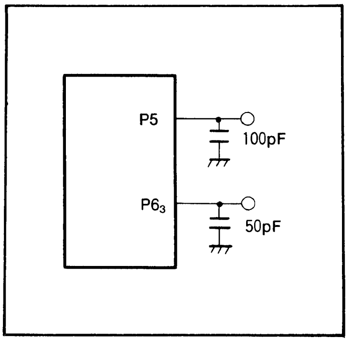


Fig. 2 Master CPU bus interface test circuit

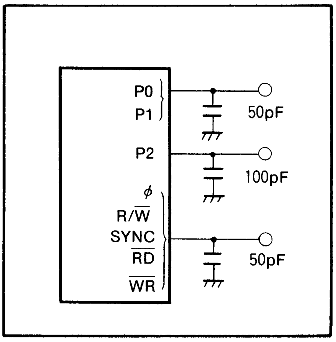


Fig. 3 Local bus test circuit

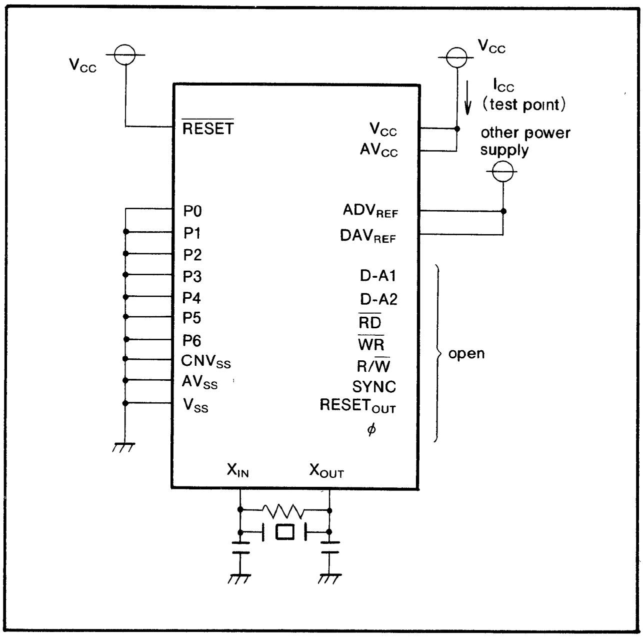
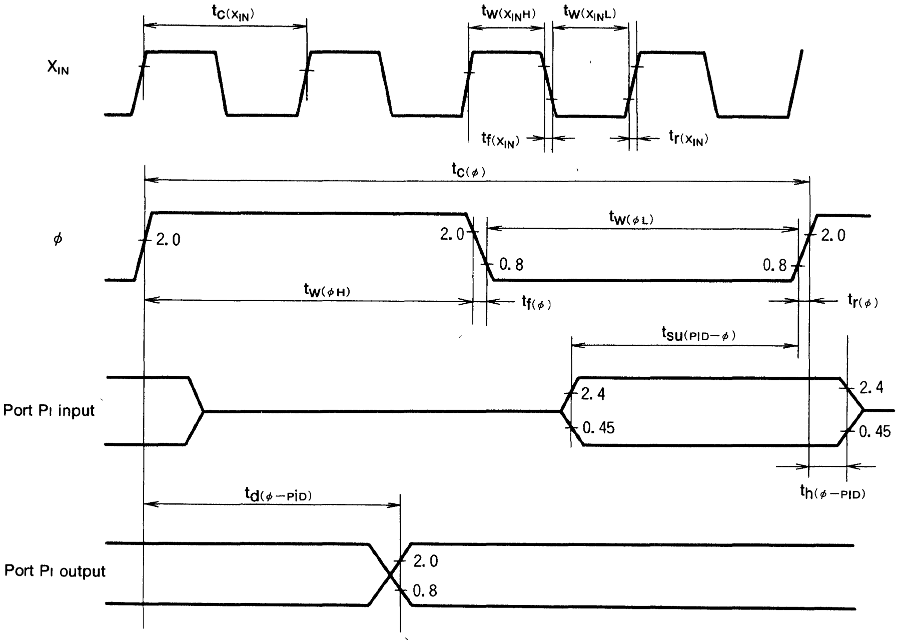


Fig. 4 I_{CC} (at stop mode) test condition

TIMING DIAGRAM

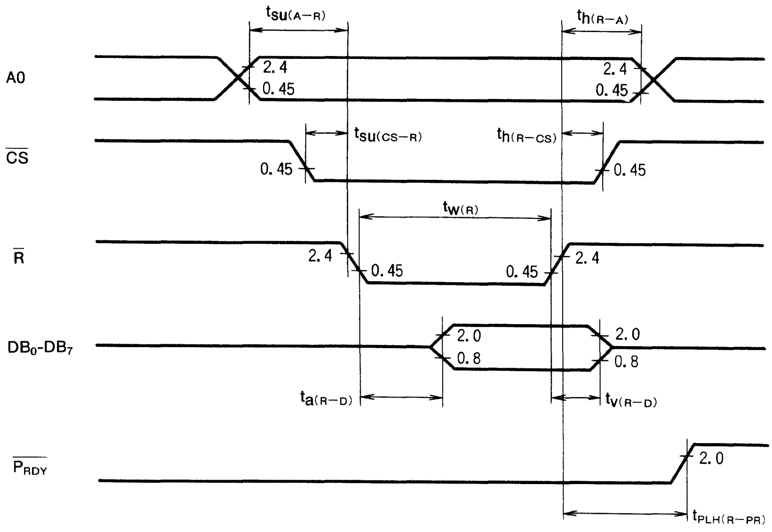
Port/single-chip mode timing diagram



Note : $V_{IH}=0.8V_{CC}$, $V_{IL}=0.16V_{CC}$ of X_{IN}

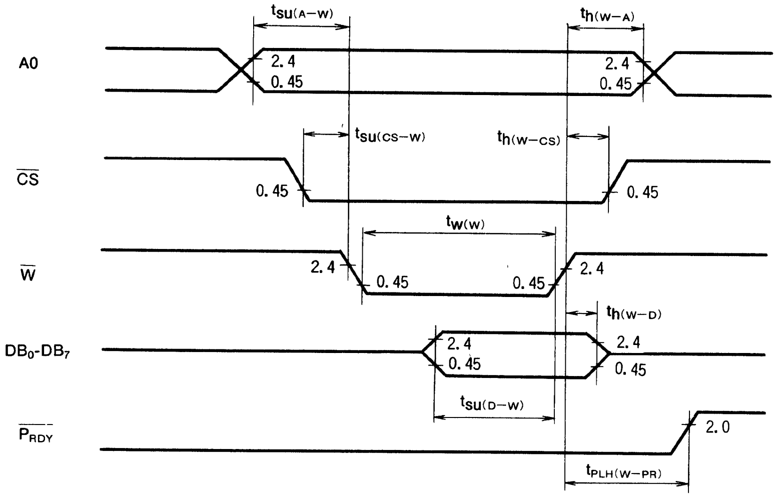
Master CPU bus interface/ $\overline{R}$ and $\overline{W}$ separation type timing diagram

Read

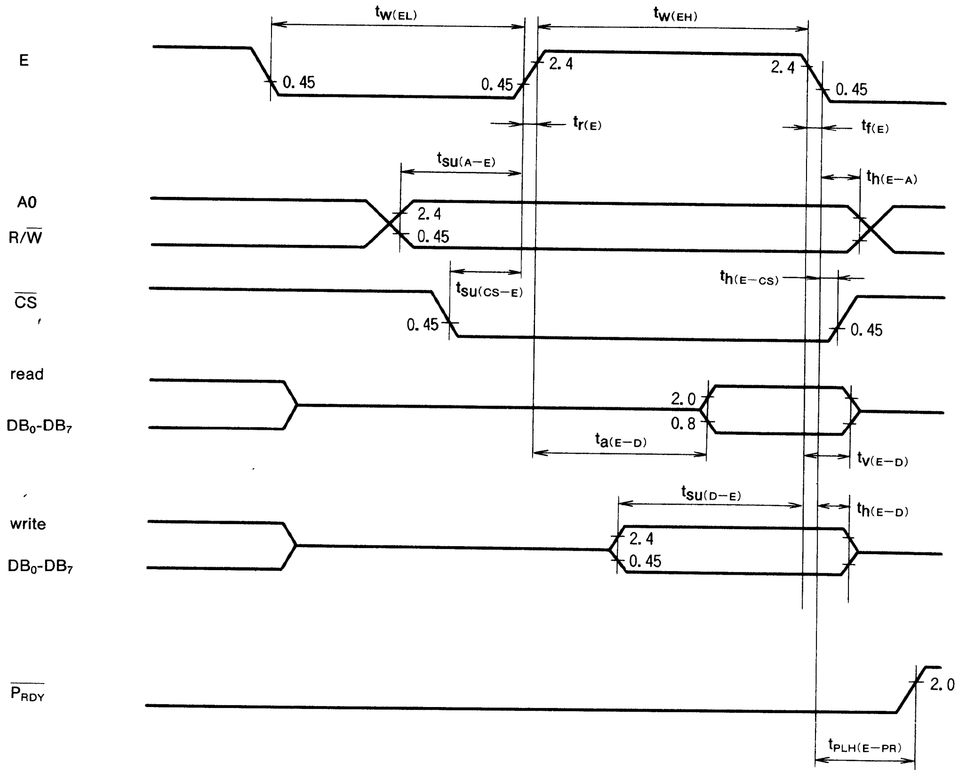


EXTENDED OPERATING TEMPERATURE VERSION of M37450M4-XXXSP

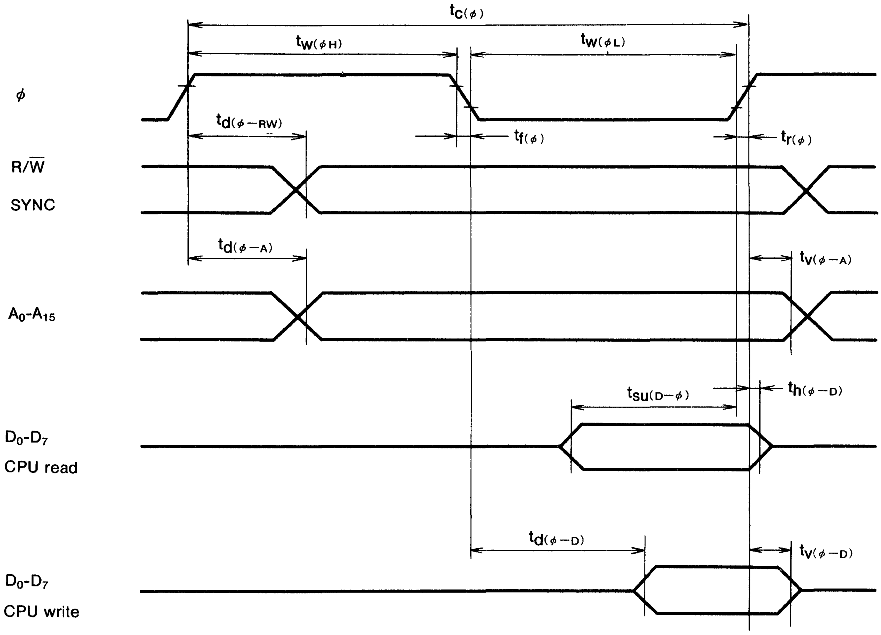
Write

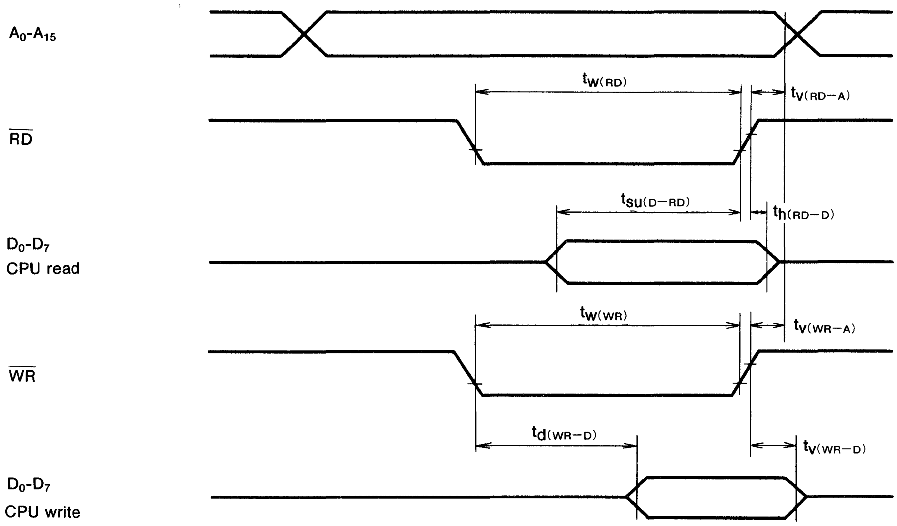


Master CPU interface/ R/$\overline{W}$ type timing diagram



Local bus timing diagram





MITSUBISHI MICROCOMPUTERS

M37451M4DXXXSP/FP
M37451M8DXXXSP/FP

EXTENDED OPERATING TEMPERATURE VERSION of M37451M4-XXXSP/FP,M37451M8-XXXSP/FP

DESCRIPTION

The M37451M4DXXXSP/FP is a single-chip microcomputer designed with CMOS sillicon gate technology. It is housed in a 64-pin shrink plastic molded DIP or an 80-pin plastic molded QFP (0.8mm-pitch).

In addition to its simple instruction sets, the ROM, RAM, and I/O addresses are placed on the same memory map to enable easy programming.

It is suited for office automation equipment and control devices. The low power consumption made by the use of a CMOS process makes it especially suitable for battery powered devices requiring low power consumption. It also has a unique feature that enables it to be used as a slave microcomputer.

Apart from the expansion in operating temperature range and consequent differences in electrical characteristics (Note), functions are the same as those of the M37451M4-XXXSP/FP.

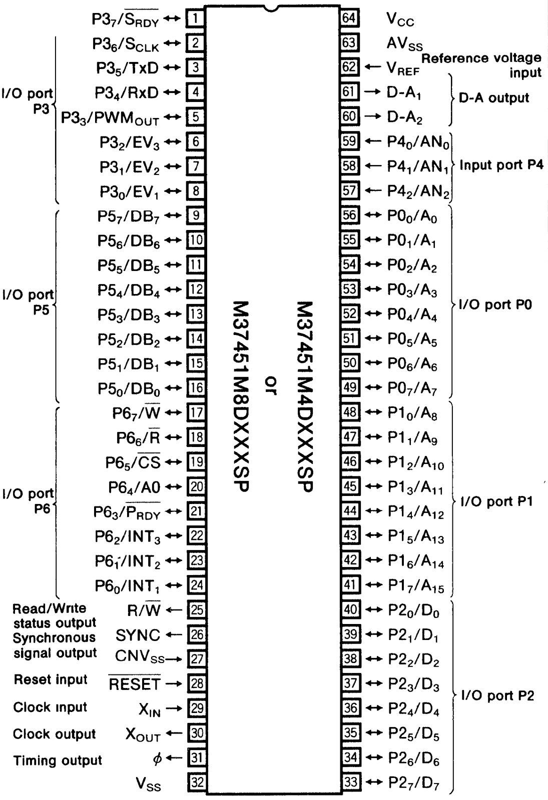
The differences between the M37451M4DXXXSP/FP and M37451M8DXXXSP/FP are as shown below.

Type name	ROM size	RAM size
M37451M4DXXXSP/FP	8192 bytes	256 bytes
M37451M8DXXXSP/FP	16384 bytes	384 bytes

The number of analog input pins for the 80-pin model (FP version) is different from the 64-pin model (SP version) In addition, the 80-pin model has special pins for $\overline{RD}$, $\overline{WR}$, $RESET_{OUT}$, DAV_{REF}, ADV_{REF}, AV_{CC} and the 64-pin model has a special V_{REF} pin.

Note : The maximum value of supply current is 20mA.
All other values are the same as that of M37451M4-XXXSP/FP.

PIN CONFIGURATION (TOP VIEW)



Outline 64P4B

FEATURES

- Number of basic instructions ······ 71
  69 MELPS 740 basic instructions+2 multiply/divide instructions
- Instruction execution time
  (minimum instructions at 12.5MHz frequency) ······ 0.64μs
- Single power supply ······ 5V±10%
- Power dissipation normal operation mode
  (at 12.5MHz frequency) ······ 40mW
- Subroutine nesting ······ 96 levels max.
- Interrupt ······ 15 events
- Master CPU interface ······ 1 byte
- 16-bit timer ······ 3
- 8-bit timer (Serial I/O use) ······ 1
- Serial I/O (UART or clock synchronous) ······ 1
- A-D converter (8-bit resolution) ······ 3 channels (DIP)
  8 channels (QFP)
- D-A converter (8-bit resolution) ······ 2 channels
- PWM output with 8-bit prescaler
  (Either resolution 8 bit or 16 bit is software selectable) ··· 1
- Programmable I/O ports
  (Ports P0, P1, P2, P3, P5, P6) ······ 48
- Input port (Port P4) ······ 3(DIP), 8(QFP)
- Output ports (Ports $D\text{-}A_1$, $D\text{-}A_2$) ······ 2
- Operating temperature ······ −40 to 85℃

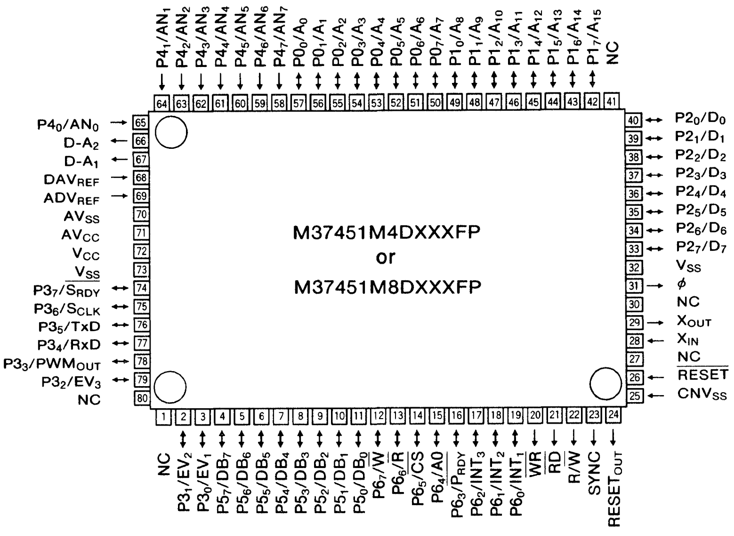
APPLICATION

Industrial machinery

M37451M4DXXXSP/FP
M37451M8DXXXSP/FP

EXTENDED OPERATING TEMPERATURE VERSION of M37451M4-XXXSP/FP,M37451M8-XXXSP/FP

PIN CONFIGURATION (TOP VIEW)



Outline 80P6N

NC : No connection

MITSUBISHI MICROCOMPUTERS

M37450PSS

PIGGYBACK for M37450M2-XXXSP,M37450M4-XXXSP,M37450M8-XXXSP

DESCRIPTION

The M37450PSS is an EPROM mounted-type microcomputer employing a silicon gate CMOS process and was designed for developing programs for single-chip, 8-bit microcomputers M37450M2-XXXSP, M37450M4-XXXSP and M37450M8-XXXSP. The M37450PSS, being housed in a piggyback-type 64-pin shrink DIP, is compatible with the M37450M2-XXXSP, M37450M4-XXXSP and M37450M8-XXXSP.

There is a 28-pin socket on the upper surface so that the M5M27C256K-12 or the M5M27C256K-15 EPROM may be used.

The M37450PSS simplifies the development of programs for the M37450M2-XXXSP, M37450M4-XXXSP and M37450 M8-XXXSP and is excellent for making prototypes.

FEATURES

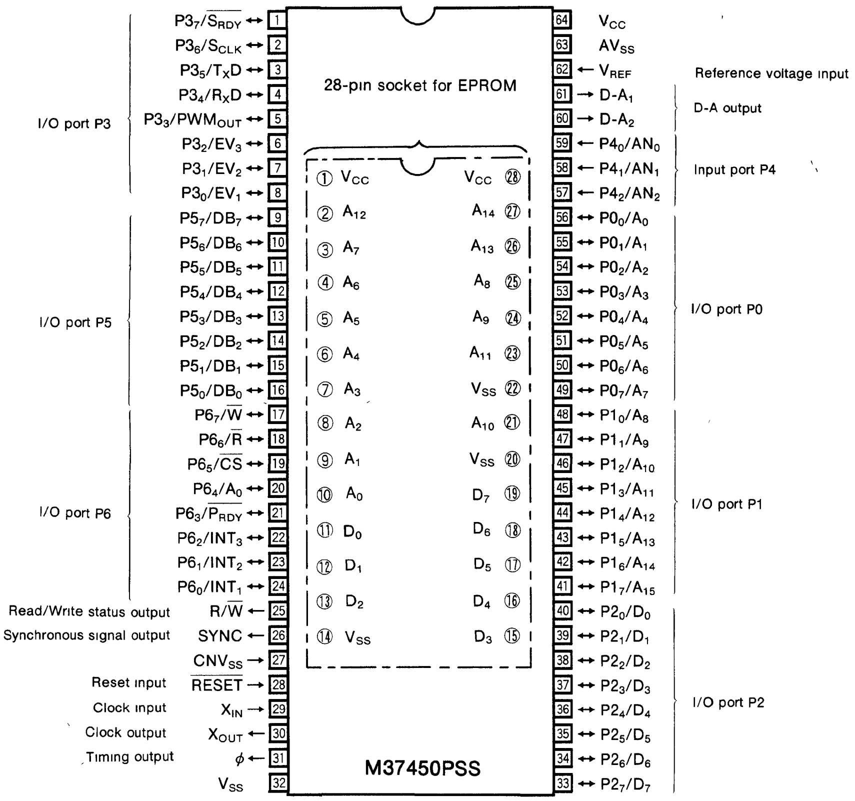
- Differences with the M37450M2-XXXSP, M37450M4-XXXSP and M37450M8-XXXSP are:
  (1) ROMless, EPROM is attached externally.
  (2) Suitable EPROM is M5M27C256K-12, M5M27C256K -15.

APPLICATION

Development of programs for the following systems;

- Slave controller for PPCs, facsimiles, and page printers
- HDD, optical disk, inverter, and industrial motor controllers
- Industrial robots and machines

PIN CONFIGURATION (TOP VIEW)



Outline 64S1M

The symbol "○" indicates sockets for EPROM

PIN DESCRIPTION

Pin	Name	Input/ Output	Functions
V_{CC}, V_{SS}	Supply voltage		Power supply inputs 5V±10% to V_{CC} and 0V to V_{SS}
CNV_{SS}	CNV_{SS}		Controls the processor mode of the chip Normally connected to V_{SS} or V_{CC}
$\overline{RESET}$	Reset input	Input	To enter the reset state, the reset input pin must be kept at a "L" for more than 8 clock cycles (under normal V_{CC} conditions) If more time is needed for the crystal oscillator to stabillize, this "L" condition should be maintained for the required time
X_{IN}	Clock input	Input	These are I/O pins of internal clock generating circuit for main clock To control generating frequency, an external ceramic or a quartz crystal oscillator is connected between the X_{IN} and X_{OUT} pins If an external clock is used, the clock source should be connected to the X_{IN} pin and the X_{OUT} pin should be left open
X_{OUT}	Clock output	Output	
ϕ	Timing output	Output	Outputs signal consisting of oscillating frequency divided by four
SYNC	Synchronous signal output	Output	This signal is output "H" during operation code fetch and is used to control single stepping of programs
$R/\overline{W}$	Read/Write status output	Output	This signal determines the direction of the data bus It is "H" during read and "L" during write
$P0_0$-$P0_7$	I/O port P0	I/O	Port P0 is an 8-bit I/O port with directional registers allowing each I/O bit to be individually programed as input or output The output structure is CMOS output The low-order bits of the address are output except in single-chip mode
$P1_0$-$P1_7$	I/O port P1	I/O	Port P1 is an 8-bit I/O port and has basically the same function as port P0 The high-order bits of the address are output except in single-chip mode
$P2_0$-$P2_7$	I/O port P2	I/O	Port P2 is an 8-bit I/O port and has basically the same function as P0 Used as data bus except in single-chip mode
$P3_0$-$P3_7$	I/O port P3	I/O	Port P3 is an 8-bit I/O port and has basically the same function as P0 Serial I/O, PWM output, or even I/O function can be selected with a program
$P4_0$-$P4_2$	Input port P4	Input	Analog input pin for the A-D converter They may also be used as digital input pins
$P5_0$-$P5_7$	I/O port P5	I/O	Port P5 is an 8-bit I/O port and has basically the same function as P0 This port functions as an 8-bit data bus for the master CPU when slave mode is selected with a program
$P6_0$-$P6_7$	I/O port P6	I/O	Port P6 is an 8-bit I/O port and has basically the same function as P0 Pins $P6_3$ to $P6_7$ change to control bus for the master CPU when slave mode is selected with a program Pins $P6_0$ to $P6_2$ may be programed as external interrupt input pins
D-A_1, D-A_2	D-A output	Output	Analog signal from D-A converter is output
V_{REF}	Refference voltage input	Input	Reference voltage input pin for A-D and D-A converter
AV_{SS}	Analog power supply		Ground level input pin for A-D and D-A converter
A_0-A_{14}	Output port A	Output	Port A outputs the adresses to the EPROM mounted on the top of the package
D_0-D_7	Input port D	Input	Port D takes the input data from the EPROM mounted on the top of the package

EXPLANATION OF FUNCTION BLOCK OPERATION

The differences between the M37450PSS and the M37450M2-XXXSP, M37450M4-XXXSP and M37450M8-XXXSP are explained below. As all other points are the same, only the differences are explained.

MEMORY

Instead of an internal ROM, an EPROM is mounted. The addresses of EPROM are 8000_{16} to $FFFF_{16}$, having 32K bytes. Internal RAMs are provided from 0000_{16} to $00BF_{16}$ (192 bytes) and from 0100_{16} to $01FF_{16}$ (256 bytes) for a total of 448 bytes. However, the 64-byte area from $01C0_{16}$ to $01FF_{16}$ cannot be used when creating masked ROM. The rest of the functions are equivalent to the M37450M2-XXXSP, M37450M4-XXXSP and M37450M8-XXXSP

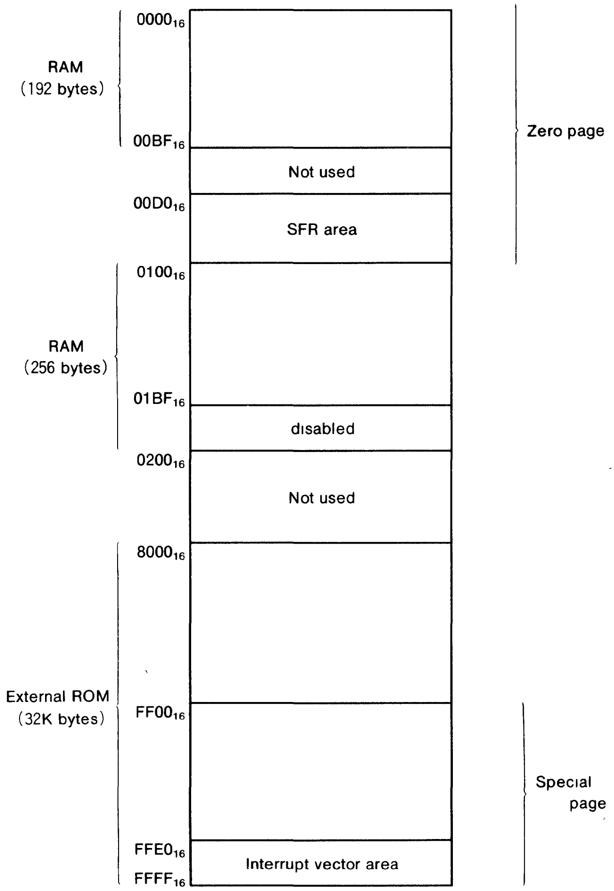


Fig. 1 Memory map

00D0$_{16}$	Port P0 register	00E8$_{16}$	Serial I/O control register
00D1$_{16}$	Port P0 directional register	00E9$_{16}$	UART control register
00D2$_{16}$	Port P1 register	00EA$_{16}$	Baud rate generator
00D3$_{16}$	Port P1 directional register	00EB$_{16}$	PWM register (lower-byte)
00D4$_{16}$	Port P2 register	00EC$_{16}$	PWM register (higher-byte)
00D5$_{16}$	Port P2 directional register	00ED$_{16}$	Timer 1 control register
00D6$_{16}$	Port P3 register	00EE$_{16}$	Timer 2 control register
00D7$_{16}$	Port P3 directional register	00EF$_{16}$	Timer 3 control register
00D8$_{16}$	Port P4	00F0$_{16}$	Timer 1 register (lower-byte)
00D9$_{16}$	Reserved	00F1$_{16}$	Timer 1 register (higher-byte)
00DA$_{16}$	Port P5 register	00F2$_{16}$	Timer 1 latch (lower-byte)
00DB$_{16}$	Port P5 directional register	00F3$_{16}$	Timer 1 latch (higher-byte)
00DC$_{16}$	Port P6 register	00F4$_{16}$	Timer 2 register (lower-byte)
00DD$_{16}$	Port P6 directional register	00F5$_{16}$	Timer 2 register (higher-byte)
00DE$_{16}$	MISRG1	00F6$_{16}$	Timer 2 latch (lower-byte)
00DF$_{16}$	MISRG2	00F7$_{16}$	Timer 2 latch (higher-byte)
00E0$_{16}$	D-A1 register	00F8$_{16}$	Timer 3 register (lower-byte)
00E1$_{16}$	D-A2 register	00F9$_{16}$	Timer 3 register (higher-byte)
00E2$_{16}$	A-D register	00FA$_{16}$	Timer 3 latch (lower-byte)
00E3$_{16}$	A-D control register	00FB$_{16}$	Timer 3 latch (higher-byte)
00E4$_{16}$	Data bus buffer register	00FC$_{16}$	Interrupt request register 1
00E5$_{16}$	Data bus buffer status register	00FD$_{16}$	Interrupt request register 2
00E6$_{16}$	Receive/transfer buffer register	00FE$_{16}$	Interrupt control register 1
00E7$_{16}$	Serial I/O status register	00FF$_{16}$	Interrupt control register 2

Fig. 2 SFR (Special Function Register) memory map

PROCESSOR MODE

External memory area differs from the M37450M2-XXXSP, M37450M4-XXXSP and M37450M8-XXXSP.

Figure 3 shows the external memory area when the M37450PSS is in the memory expanding mode and Fig. 4 shows the external memory area when the M37450PSS is in the microprocessor mode.

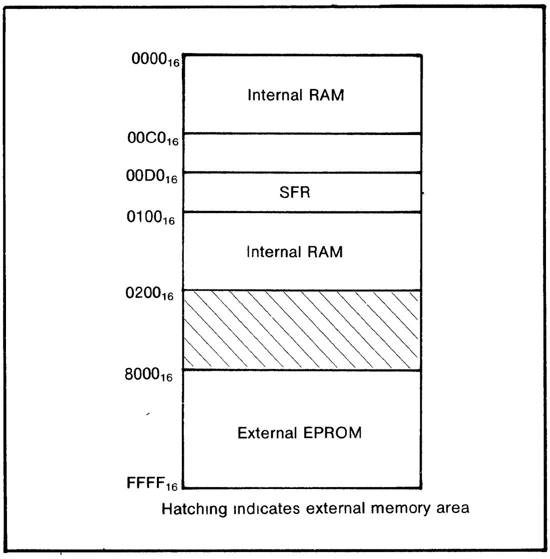


Fig. 3 Memory map in memory expanding mode

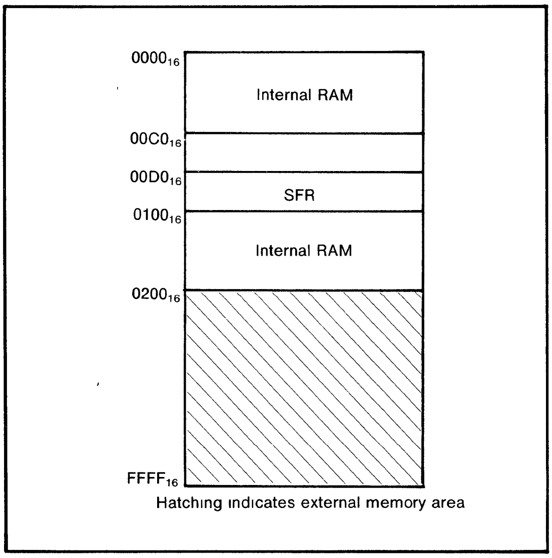


Fig. 4 Memory map in memory expanding mode

PRECAUTION FOR USE

(1) Program area

When developing programs on the M37450PSS, the ROM and RAM sizes of the M37450M2-XXXSP, M37450M4-XXXSP, and M37450M8-XXXSP must be considered.

For the M37450M2-XXXSP, use the M37450PSS ROM program area from $F000_{16}$ to $FFFF_{16}$. (Write the program from 7000_{16} to $7FFF_{16}$ on the EPROM.)

Also, when creating masked ROMs, note that the RAM area for the M37450M2-XXXSP is 128 bytes from 0000_{16} to $007F_{16}$.

For the M37450M4-XXXSP, use the M37450PSS ROM program area from $E000_{16}$ to $FFFF_{16}$. (Write the program from 6000_{16} to $7FFF_{16}$ on the EPROM.)

Also, when creating masked ROMs, note that the RAM area for the M37450M4-XXXSP is 192 bytes from 0000_{16} to $00BF_{16}$ and 64 bytes from 0100_{16} to $013F_{16}$ for a total of 256 bytes.

For the M37450M8-XXXSP, use the M37450PSS ROM program area from $C000_{16}$ to $FFFF_{16}$. (Write the program from 4000_{16} to $7FFF_{16}$ on the EPROM.)

Also, when creating masked ROMs, note that the RAM area for the M37450M8-XXXSP is 192 bytes from 0000_{16} to $00BF_{16}$ and 192 bytes from 0100_{16} to $01BF_{16}$ for a total of 384 bytes.

The 64 byte area from $01C0_{16}$ to $01FF_{16}$ can also be used as internal RAM. However, it cannot be used when creating masked ROMs because there is no corresponding device

(2) External memory

When developing programs, note that the external memory area of the M37450PSS is as described in the previous section.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS} Output transistors are at "OFF" state	−0. 3 to 7	V
V_I	Input voltage $\overline{RESET}$, X_{IN}		−0. 3 to 7	V
V_I	Input voltage, $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, V_{REF}		−0. 3 to V_{CC}+0. 3	V
V_I	Input voltage CNV_{SS}		−0. 3 to 13	V
V_O	Output voltage, $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, X_{OUT}, ϕ, R/$\overline{W}$, SYNC		−0. 3 to V_{CC}+0. 3	V
Pd	Power dissipation	T_a=25℃	1000	mW
T_{opr}	Operating temperature		−10 to 70	℃
T_{stg}	Storage temperature		−40 to 125	℃

RECOMMENDED OPERATING CONDITIONS (V_{CC} = 5V±10%, T_a = −10 to 70℃, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4. 5	5	5. 5	V
V_{SS}	Supply voltage		0		V
V_{IH}	"H" input voltage $\overline{RESET}$, X_{IN}, CNV_{SS} (Note1)	0. 8V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$ (except Note1)	2. 0		V_{CC}	V
V_{IL}	"L" input voltage CNV_{SS} (Note1)	0		0. 2V_{CC}	V
V_{IL}	"L" input voltage $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$ (except Note1)	0		0. 8	V
V_{IL}	"L" input voltage $\overline{RESET}$	0		0. 12V_{CC}	V
V_{IL}	"L" input voltage X_{IN}	0		0. 16V_{CC}	V
$I_{OL(peak)}$	"L" peak output current $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$			10	mA
$I_{OL(avg)}$	"L" average output current $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$ (Note2)			5	mA
$I_{OH(peak)}$	"H" peak output current $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$			−10	mA
$I_{OH(avg)}$	"H" average output current $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$ (Note2)			−5	mA
$f(X_{IN})$	Clock oscillating frequency	1		10	MHz

Note 1 : Ports operate as INT_1-INT_3($P6_0$-$P6_2$), EV_1-EV_3($P3_0$-$P3_2$), R_XD($P3_4$)and S_{CLK}($P3_6$)
2 : The average output current $I_{OH(avg)}$ and $I_{OL(avg)}$ are the average value during a 100ms
3 : The total of "L" output $I_{OL(peak)}$ of port P0, P1 and P2 is 40mA max
The total of "H" output $I_{OH(peak)}$ of port P0, P1 and P2 is 40mA max
The total of "L" output $I_{OL(peak)}$ of port P3, P5, P6, R/$\overline{W}$, SYNC and ϕ is 40mA max
The total of "H" output $I_{OH(peak)}$ of port P3, P5, P6, R/$\overline{W}$, SYNC and ϕ is 40mA max

ELECTRICAL CHARACTERISTICS (V_{CC} = 5V±10%, V_{SS} = 0V, T_a = −10 to 70℃, f(X_{IN}) = 10MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{OH}	"H" output R/$\overline{W}$, SYNC, ϕ	I_{OH}=−2mA	V_{CC}−1			V
V_{OH}	"H" output voltage $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$	I_{OH}=−5mA	V_{CC}−1			V
V_{OL}	"L" output voltage $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, R/$\overline{W}$, SYNC, ϕ	I_{OL}=2mA			0.45	V
V_{OL}	"L" output voltage $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$	I_{OL}=5mA			1	V
$V_{T+}-V_{T-}$	Hysterisis INT_1-INT_3($P6_0$-$P6_2$), EV_1-EV_3($P3_0$-$P3_2$), R_XD($P3_4$), S_{CLK}($P3_6$)	Function input level	0.3		1	V
$V_{T+}-V_{T-}$	Hysterisis $\overline{RESET}$				0.7	V
$V_{T+}-V_{T-}$	Hysterisis X_{IN}		0.1		0.5	V
I_{IL}	"L" input current $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $\overline{RESET}$, X_{IN}	V_I=V_{SS}	−5		5	μA
I_{IH}	"H" input current $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $\overline{RESET}$, X_{IN}	V_I=V_{CC}	−5		5	μA
V_{RAM}	RAM retention voltage	At stop mode	2			V
I_{CC}	Supply current	At system operation f(X_{IN})=10MHz(Note 1)		6	10	mA

Note 1 : Only for M37450PSS (not contact in EPROM dissipation current)

A-D CONVERTER CHARACTERISTICS (V_{CC} = 5V, V_{SS} = AV_{SS} = 0V, T_a = 25℃, f(X_{IN})= 10MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max.	
—	Resolution				8	Bits
—	Absolute accuracy	V_{CC}=V_{REF}=5.12V		±1.5	±3	LSB
t_{CONV}	Conversion time				49	t_C(ϕ)
V_{IA}	Analog input voltage		AV_{SS}		AV_{CC}	V
V_{VREF}	Reference analog input voltage		2		V_{CC}	V
R_{LADDER}	Ladder resistance value	V_{REF}=5V	2	7.5	10	kΩ
I_{IVREF}	Reference analog input current	V_{REF}=5V	0.5	0.7	2.5	mA
V_{AVSS}	Analog power input			0		V

D-A CONVERTER CHARACTERISTICS (V_{CC} = 5V, V_{SS} = AV_{SS} = 0V, T_a = 25℃, f(X_{IN})= 10MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
—	Resolution				8	Bits
—	Absolute accuracy	V_{CC}=V_{REF}=5.12V			1.0	%
t_{SU}	Setup time				3	μs
R_O	Output resistance		1	2	4	kΩ
V_{AVSS}	Analog power input			0		V
V_{VREF}	Analog power input		4		V_{CC}	V
I_{VREF}	Reference power input current (Each pin)		0	2.5	5	mA

M37450PFS

PIGGYBACK for M37450M2-XXXFP,M37450M4-XXXFP,M37450M8-XXXFP

DESCRIPTION

The M37450PFS is an EPROM mounted-type microcomputer employing a silicon gate CMOS process and was designed for developing programs for single-chip, 8-bit microcomputers M37450M2-XXXFP, M37450M4-XXXFP and M37450M8-XXXFP. The M37450PFS, being housed in a piggyback-type 80-pin plastic QFP is compatible with the M37450M2-XXXFP, M37450M4-XXXFP and M37450M8-XXXFP.

There is a 32-pin socket on the upper surface so that the outline is LCC-32C-A01 and 27C256 EPROM may be used.

The M37450PSS simplifies the development of programs for the M37450M2-XXXFP, M37450M4-XXXFP and M37450 M8-XXXFP and is excellent for making prototypes.

FEATURES

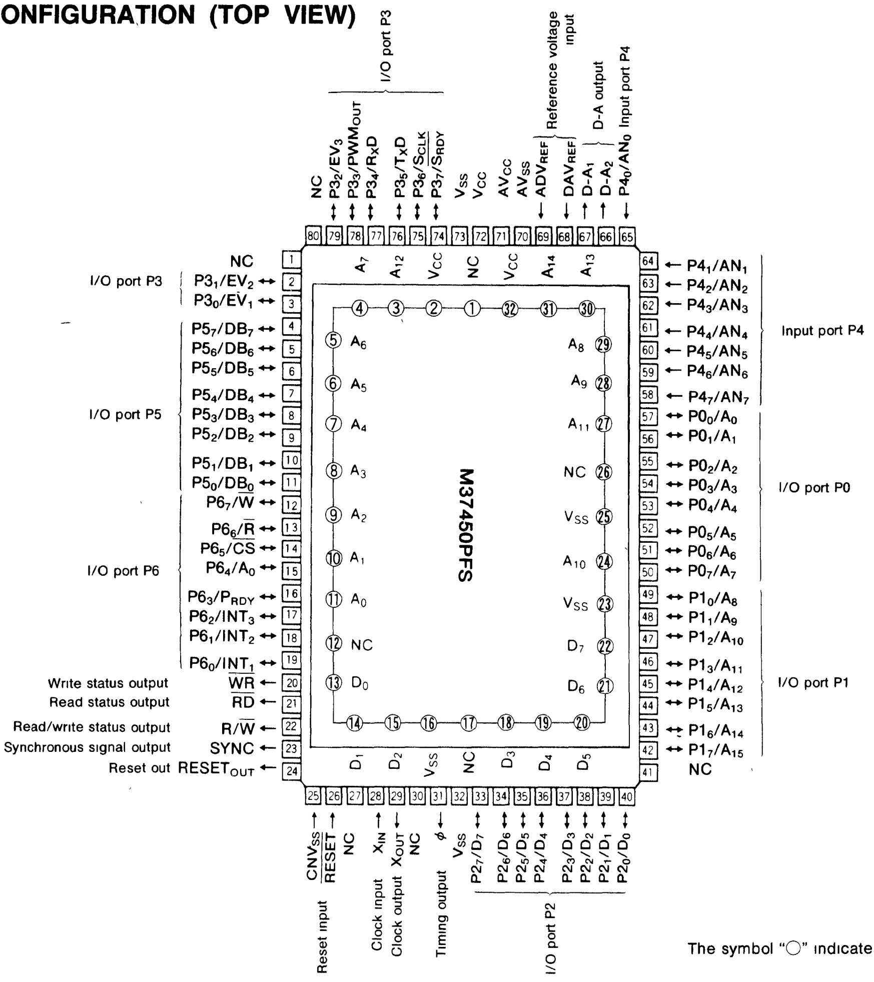
- Difference with the M37450M2-XXXFP, M37450M4-XXXFP and M37450M8-XXXFP is:
  (1) ROMless, EPROM is attached externally.
  (2) Suitable EPROM is that the outline is LCC-32C-A01 and 27C256

APPLICATION

Development of programs for the following systems:

- Slave controller for PPCs, facsimiles, and page printers
- HDD, optical disk, inverter, and industrial motor controllers
- Industrial robots and machines

PIN CONFIGURATION (TOP VIEW)



The symbol "○" indicates socket for EPROM

Outline 80S6M

NC : No Connection

PIN DESCRIPTION

Pin	Name	Input/ Output	Functions
V_{CC}, V_{SS}	Supply voltage		Power supply inputs 5V±10% to V_{CC} and 0V to V_{SS}
CNV_{SS}	CNV_{SS}		Controls the processor mode of the chip Normally connected to V_{SS} or V_{CC}
$\overline{RESET}$	Reset input	Input	To enter the reset state, the reset input pin must be kept at a "L" for more than 8 clock cycles (under normal V_{CC} conditions) If more time is needed for the crystal oscillator to stabilize, this "L" condition should be maintained for the required time
X_{IN}	Clock input	Input	These are I/O pins of internal clock generating circuit for main clock To control generating frequency, an external ceramic or a quartz crystal oscillator is connected between the X_{IN} and X_{OUT} pins If an external clock is used, the clock source should be connected to the X_{IN} pin and the X_{OUT} pin should be left open
X_{OUT}	Clock output	Output	
ϕ	Timing output	Output	Outputs signal consisting of oscillating frequency divided by four
SYNC	Synchronous signal output	Output	This signal is output "H" during operation code fetch and is used to control single stepping of programs
$R/\overline{W}$	Read/Write status output	Output	This signal determines the direction of the data bus It is "H" during read and "L" during write
$P0_0$-$P0_7$	I/O port P0	I/O	Port P0 is an 8-bit I/O port with directional registers allowing each I/O bit to be individually programed as input or output The output structure is CMOS output The low-order bits of the address are output except in single-chip mode
$P1_0$-$P1_7$	I/O port P1	I/O	Port P1 is an 8-bit I/O port and has basically the same function as port P0 The high-order bits of the address are output except in single-chip mode
$P2_0$-$P2_7$	I/O port P2	I/O	Port P2 is an 8-bit I/O port and has basically the same function as P0 Used as data bus except in single-chip mode
$P3_0$-$P3_7$	I/O port P3	I/O	Port P3 is an 8-bit I/O port and has basically the same function as P0 Serial I/O, PWM output, or even I/O function can be selected with a program
$P4_0$-$P4_7$	Input port P4	Input	Analog input pin for the A-D converter They may also be used as digital input pins
$P5_0$-$P5_7$	I/O port P5	I/O	Port P5 is an 8-bit I/O port and has basically the same function as P0 This port functions as an 8-bit data bus for the master CPU when slave mode is selected with a program
$P6_0$-$P6_7$	I/O port P6	I/O	Port P6 is an 8-bit I/O port and has basically the same function as P0 Pins $P6_3$ to $P6_7$ change to control bus for the master CPU when slave mode is selected with a program Pins $P6_0$ to $P6_2$ may be programed as external interrupt input pins
$D\text{-}A_1$, $D\text{-}A_2$	D-A output	Output	Analog signal from D-A converter is output
ADV_{REF}	A-D refference voltage input	Input	Reference voltage input pin for A-D converter
DAV_{REF}	D-A refference voltage input	Input	Reference voltage input pin for D-A converter
AV_{SS}	Analog power supply		Ground level input pin for A-D and D-A converter
AV_{CC}	Analog power supply		Power supply input pin for A-D converter
$\overline{RD}$	Read signal output	Output	Control signal output as active "L" when vailed data is read from data bus
$\overline{WR}$	Write signal output	Output	Control signal output as active "L" when writing data from data bus to external component
$RESET_{OUT}$	Reset output	Output	Control signal output as active "H" during reset It is used as a reset output signal for perpheral components
A_0-A_{14}	Output port A	Output	Port A outputs the adresses to the EPROM mounted on the top of the package
D_0-D_7	Input port D	Input	Port D takes the input data from the EPROM mounted on the top of the package

EXPLANATION OF FUNCTION BLOCK OPERATION

The differences between the M37450PFS and the M37450M2-XXXFP, M37450M4-XXXFP and M37450M8-XXXFP are explained below. As all other points are the same, only the differences are explained.

MEMORY

Instead of an internal ROM, an EPROM is mounted. The addresses of EPROM are 8000_{16} to $FFFF_{16}$, having 32K bytes. Internal RAMs are provided from 0000_{16} to $00BF_{16}$ (192 bytes) and from 0100_{16} to $01FF_{16}$ (256 bytes) for a total of 448 bytes. However, the 64-byte area from $01C0_{16}$ to $01FF_{16}$ cannot be used when creating masked ROM. The rest of the functions are equivalent to the M37450M2-XXXFP, M37450M4-XXXFP and M37450M8-XXXFP.

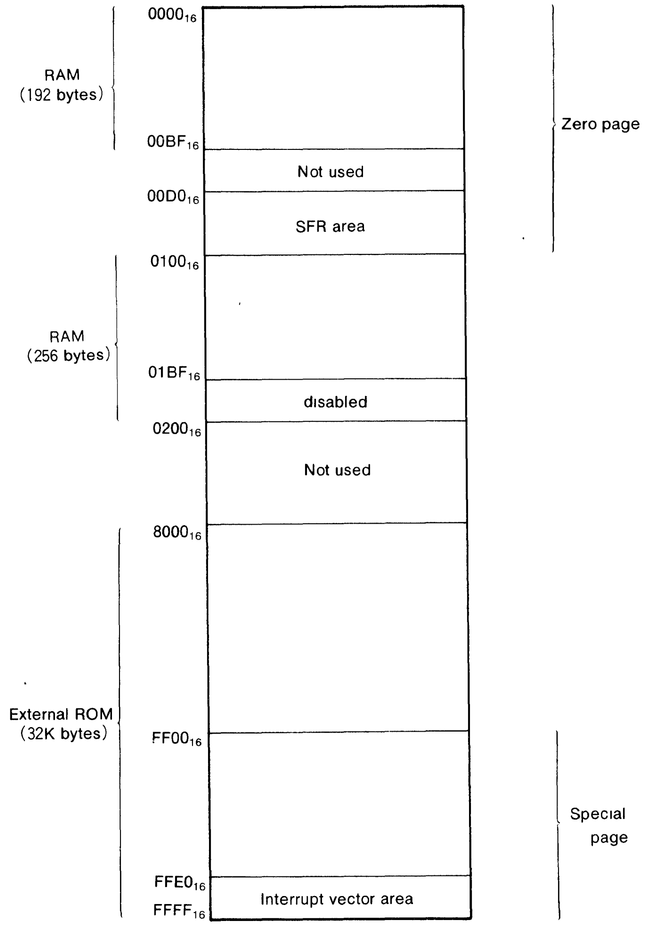


Fig. 1 Memory map

$00D0_{16}$	Port P0 register	$00E8_{16}$	Serial I/O control register
$00D1_{16}$	Port P0 directional register	$00E9_{16}$	UART control register
$00D2_{16}$	Port P1 register	$00EA_{16}$	Baud rate generator
$00D3_{16}$	Port P1 directional register	$00EB_{16}$	PWM register (lower-byte)
$00D4_{16}$	Port P2 register	$00EC_{16}$	PWM register (higher-byte)
$00D5_{16}$	Port P2 directional register	$00ED_{16}$	Timer 1 control register
$00D6_{16}$	Port P3 register	$00EE_{16}$	Timer 2 control register
$00D7_{16}$	Port P3 directional register	$00EF_{16}$	Timer 3 control register
$00D8_{16}$	Port P4 register	$00F0_{16}$	Timer 1 register (lower-byte)
$00D9_{16}$	Reserved	$00F1_{16}$	Timer 1 register (higher-byte)
$00DA_{16}$	Port P5 register	$00F2_{16}$	Timer 1 latch (lower-byte)
$00DB_{16}$	Port P5 directional register	$00F3_{16}$	Timer 1 latch (higher-byte)
$00DC_{16}$	Port P6 register	$00F4_{16}$	Timer 2 register (lower-byte)
$00DD_{16}$	Port P6 directional register	$00F5_{16}$	Timer 2 register (higher-byte)
$00DE_{16}$	MISRG1	$00F6_{16}$	Timer 2 latch (lower-byte)
$00DF_{16}$	MISRG2	$00F7_{16}$	Timer 2 latch (higher-byte)
$00E0_{16}$	D-A1 register	$00F8_{16}$	Timer 3 register (lower-byte)
$00E1_{16}$	D-A2 register	$00F9_{16}$	Timer 3 register (higher-byte)
$00E2_{16}$	A-D register	$00FA_{16}$	Timer 3 latch (lower-byte)
$00E3_{16}$	A-D control register	$00FB_{16}$	Timer 3 latch (higher-byte)
$00E4_{16}$	Data bus buffer register	$00FC_{16}$	Interrupt request register 1
$00E5_{16}$	Data bus buffer status register	$00FD_{16}$	Interrupt request register 2
$00E6_{16}$	Receive/transfer buffer register	$00FE_{16}$	Interrupt control register 1
$00E7_{16}$	Serial I/O status register	$00FF_{16}$	Interrupt control register 2

Fig. 2 SFR (Special Function Register) memory map

PROCESSOR MODE

External memory area differs from the M37450M2-XXXFP, M37450M4-XXXFP and M37450M8-XXXFP.

Figure 3 shows the external memory area when the M37450PFS is in the memory expanding mode and Figure 4 shows the external memory area when the M37450PFS is in the microprocessor mode.

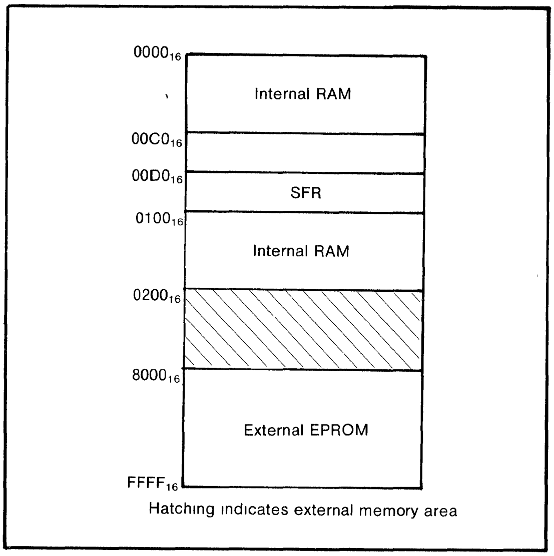


Fig. 3 Memory map in memory expanding area

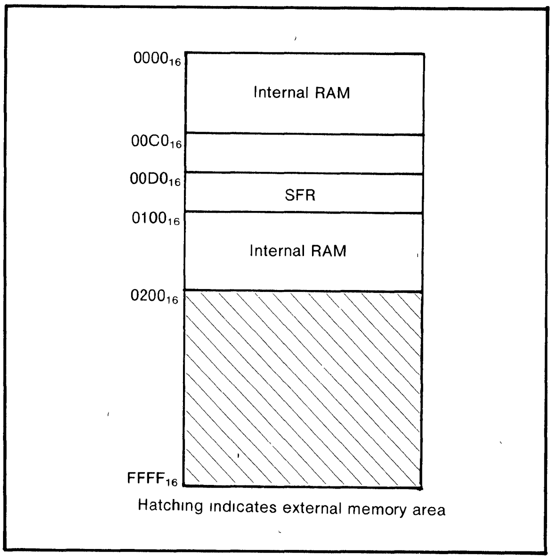


Fig. 4 Memory map in microprocessor mode

PRECAUTION FOR USE

(1) Program area

When developing programs on the M37450PFS, the ROM and sizes of the M37450M2-XXXFP, M37450M4-XXXFP, and M37450M8-XXXFP must be considered.

For the M37450M2-XXXFP, use the M37450PFS ROM program area from $F000_{16}$ to $FFFF_{16}$. (Write the program from 7000_{16} to $7FFF_{16}$ on the EPROM.)

Also, when creating masked ROMs, note that the RAM area for the M37450M2-XXXFP is 128 bytes from 0000_{16} to $0007F_{16}$.

For the M37450M4-XXXFP, use the M37450PFS ROM program area from $E000_{16}$ to $FFFF_{16}$. (Write the program from 6000_{16} to $7FFF_{16}$ on the EPROM.)

Also, when creating masked ROMs, note that the RAM area for the M37450M4-XXXFP is 192 bytes from 0000_{16} to $00BF_{16}$ and 64 bytes from 0100_{16} to $013F_{16}$ for a total of 256 bytes.

For the M37450M8-XXXFP, use the M37450PFS ROM program area from $C000_{16}$ to $FFFF_{16}$. (Write the program from 4000_{16} to $7FFF_{16}$ on the EPROM.)

Also, when creating masked ROMs, note that the RAM area for the M37450M8-XXXFP is 192 bytes from 0000_{16} to $00BF_{16}$ and 192 bytes from 0100_{16} to $01BF_{16}$ for a total of 384 bytes.

The 64 byte area from $01C0_{16}$ to $01FF_{16}$ can also be used as internal RAM. However, it cannot be used when creating masked ROMs because there is no corresponding device.

(2) External memory

When developing programs, note that the external memory area of the M37450PFS is as described in the previous section.

(3) EPROM orientation

Figure 5 shows the orientation when mountting the LCC type EPROM on the M37450PFS. Insert the EPROM firmily until it hits bottom.

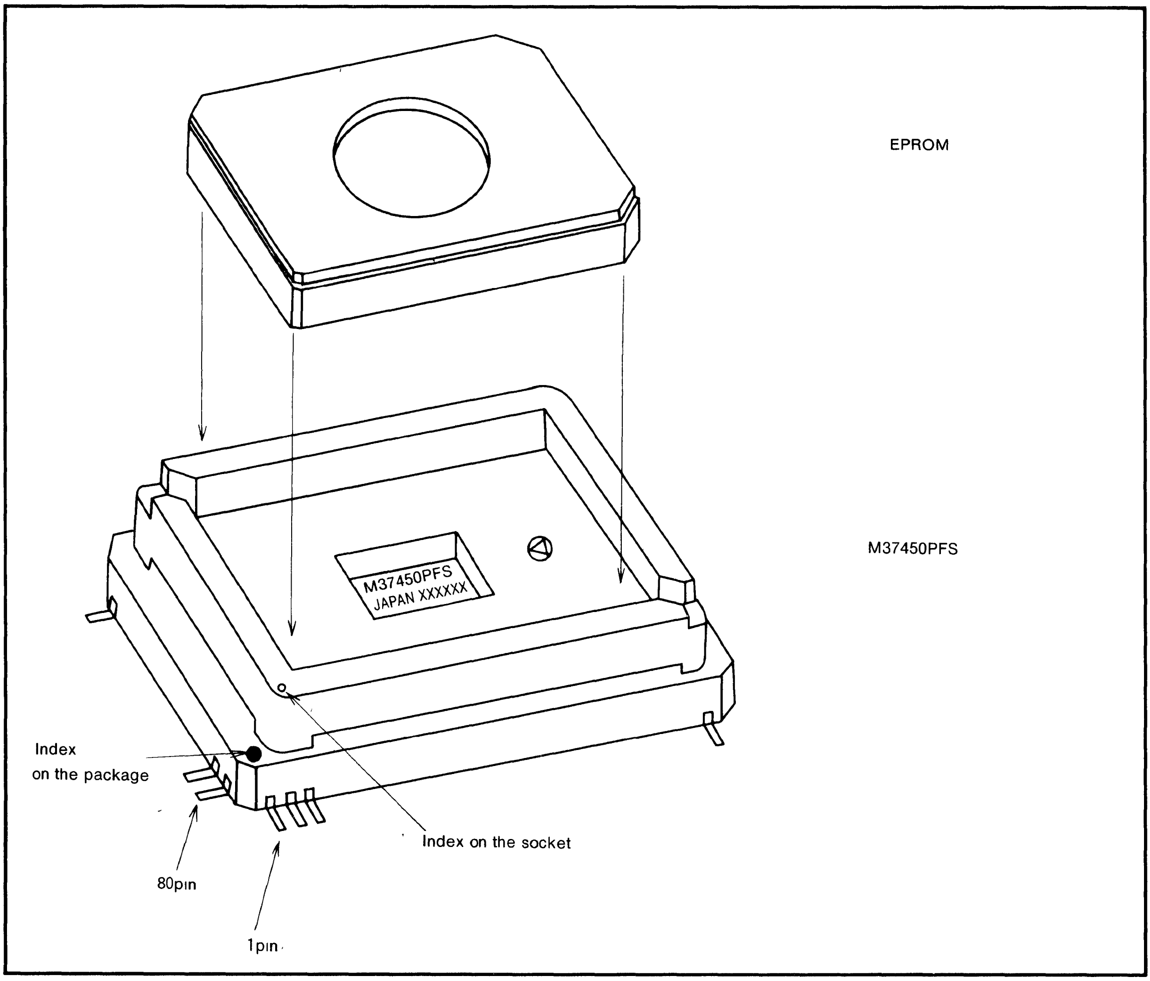


Fig. 5 EPROM orientation

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS} Output transistors are at "OFF" state	−0.3 to 7	V
V_I	Input voltage $\overline{RESET}$, X_{IN}		−0.3 to 7	V
V_I	Input voltage, $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, ADV_{RFF}, DAV_{RFF}, AV_{CC}		−0.3 to V_{CC}+0.3	V
V_I	Input voltage CNV_{SS}		−0.3 to 13	V
V_O	Output voltage, $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, X_{OUT}, ϕ, $\overline{RD}$, $\overline{WR}$, $RESET_{OUT}$, SYNC		−0.3 to V_{CC}+0.3	V
Pd	Power dissipation	T_a=25℃	500	mW
T_{opr}	Operating temperature		−10 to 70	℃
T_{stg}	Storage temperature		−40 to 125	℃

RECOMMENDED OPERATING CONDITIONS (V_{CC} = 5V±10%, T_a = −10 to 70℃, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage		0		V
V_{IH}	"H" input voltage $\overline{RESET}$, X_{IN}, CNV_{SS} (Note1)	0.8V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$ (except Note1)	2.0		V_{CC}	V
V_{IL}	"L" input voltage CNV_{SS} (Note1)	0		0.2V_{CC}	V
V_{IL}	"L" input voltage $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$ (except Note1)	0		0.8	V
V_{IL}	"L" input voltage $\overline{RESET}$	0		0.12V_{CC}	V
V_{IL}	"L" input voltage X_{IN}	0		0.16V_{CC}	V
$I_{OL(peak)}$	"L" peak output current $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$			10	mA
$I_{OL(avg)}$	"L" average output current $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$ (Note2)			5	mA
$I_{OH(peak)}$	"H" peak output current $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$			−10	mA
$I_{OH(avg)}$	"H" average output current $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$ (Note2)			−5	mA
$f(X_{IN})$	Clock oscillating frequency	1		10	MHz

Note 1 : Ports operate as INT_1-INT_3($P6_0$-$P6_2$), EV_1-EV_3($P3_0$-$P3_2$), R_XD($P3_4$)and S_{CLK}($P3_6$)

2 : The average output current $I_{OH(avg)}$ and $I_{OL(avg)}$ are the average value during a 100ms

3 : The total of "L" output $I_{OL(peak)}$ of port P0, P1 and P2 is 40mA max

The total of "H" output $I_{OH(peak)}$ of port P0, P1 and P2 is 40mA max.

The total of "L" output $I_{OL(peak)}$ of port P3, P5, P6, R/$\overline{W}$, SYNC, $RESET_{OUT}$, $\overline{RD}$, $\overline{WR}$ and ϕ is 40mA max.

The total of "H" output $I_{OH(peak)}$ of port P3, P5, P6, R/$\overline{W}$, SYNC, $RESET_{OUT}$, $\overline{RD}$, $\overline{WR}$ and ϕ is 40mA max

ELECTRICAL CHARACTERISTICS (V_{CC} = 5V±10%, V_{SS} = 0V, T_a = −10 to 70℃, f(X_{IN}) = 10MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{OH}	"H" output $\overline{RD}$, $\overline{WR}$, SYNC, $RESET_{OUT}$, ϕ	I_{OH}=−2mA	V_{CC}−1			V
V_{OH}	"H" output voltage $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$	I_{OH}=−5mA	V_{CC}−1			V
V_{OL}	"L" output voltage $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, R/$\overline{W}$, $\overline{RD}$, $\overline{WR}$, SYNC, $RESET_{OUT}$, ϕ	I_{OL}=2mA			0. 45	V
V_{OL}	"L" output voltage $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$	I_{OL}=5mA			1	V
$V_{T+}-V_{T-}$	Hysteresis INT_1-INT_3($P6_0$-$P6_2$), EV_1-EV_3($P3_0$-$P3_2$), R_XD($P3_4$), S_{CLK}($P3_6$)	Function input level	0. 3		1	V
$V_{T+}-V_{T-}$	Hysteresis $\overline{RESET}$				0. 7	V
$V_{T+}-V_{T-}$	Hysteresis X_{IN}		0. 1		0. 5	V
I_{IL}	"L" input current $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $\overline{RESET}$, X_{IN}	V_I=V_{SS}	−5		5	μA
I_{IH}	"H" input current $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $\overline{RESET}$, X_{IN}	V_I=V_{CC}	−5		5	μA
V_{RAM}	RAM retention voltage	At stop mode	2			V
I_{CC}	Supply current	At system operation f(X_{IN})=10MHz(Note 1)		6	10	mA

Note 1 : Only for M37450PFS (not contact in EPROM dissipation current)

A-D CONVERTER CHARACTERISTICS (V_{CC}=AV_{CC}=5V, V_{SS}=AV_{SS}=0V, T_a=25℃, f(X_{IN})=10MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
—	Resolution				8	Bits
—	Absolute accuracy	V_{CC}=AV_{CC}=ADV_{REF}=5. 12V		±1. 5	±3	LSB
t_{CONV}	Conversion time				49	t_C(ϕ)
V_{IA}	Analog input voltage		AV_{SS}		AV_{CC}	V
V_{ADVREF}	Reference analog input voltage		2		V_{CC}	V
R_{LADDER}	Ladder resistance value	ADV_{REF}=5V	2	7. 5	10	kΩ
$I_{IADVREF}$	Reference analog input current	ADV_{REF}=5V	0. 5	0. 7	2. 5	mA
V_{AVCC}	Analog power input			V_{CC}		V
V_{AVSS}	Analog power input			0		V

D-A CONVERTER CHARACTERISTICS (V_{CC} = 5V, V_{SS} = AV_{SS} = 0V, T_a = 25℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
—	Resolution				8	Bits
—	Absolute accuracy	V_{CC}=DAV_{REF}=5. 12V			1. 0	%
t_{SU}	Setup time				3	μs
R_O	Output resistance		1	2	4	kΩ
V_{AVSS}	Analog power input			0		V
V_{DAVREF}	Analog power input		4		V_{CC}	V
I_{DAVREF}	Reference power input current (Each pin)		0	2. 5	5	mA

M37450E4-XXXSP/FP
M37450E4SS/FS
PROM VERSION of M37450M4-XXXSP/FP

DESCRIPTION

The M37450E4-XXXSP is a single-chip microcomputer designed with CMOS silicon gate technology. It is housed in a 64-pin shrink plastic molded DIP. The features of this chip are similar to those of the M37450M4-XXXSP except that this chip has a 8192-byte PROM built-in. This single-chip microcomputer is useful for office automation appliances and consumer appliance controllers.

In addition to its simple instruction sets, the PROM, RAM and I/O addresses are placed on the same memory map to enable easy programming. Since general purpose PROM writes can be used for small quantity production runs. It also has a unique feature that enables it to be used as a slave microcomputer.

The M37450E4SS and the M37450E4FS are the window type. The differences between the M37450E4-XXXSP and the M37450E4-XXXFP, and between the M37450E4SS and the M37450E4FS are the package outline and the power dissipation ability (absolute maximum ratings).

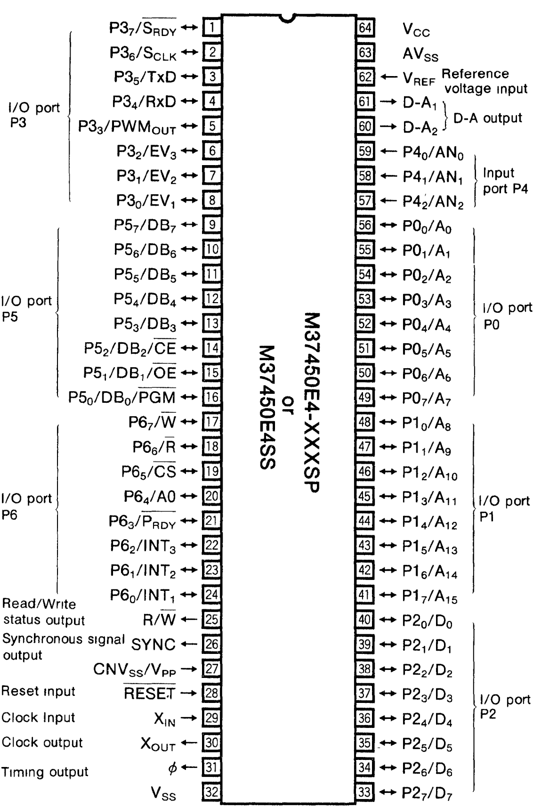
FEATURES

- Number of basic instructions ································ 71
  69 MELPS 740 basic instructions + 2 multiply/divide instructions
- Memory size PROM ································ 8192 bytes
  RAM ································ 256 bytes
- Instruction execution time
  (minimum instructions at 10 MHz frequency) ····· 0.8μs
- Single power supply ································ 5V±5%
- Power dissipation normal operation mode
  (at 10 MHz frequency) ································ 30mW
- Subroutine nesting ································ 96 levels max.
- Interrupt ································ 15 events
- Master CPU bus interface ································ 1 byte
- 16-bit timer ································ 3
- 8-bit timer (Serial I/O use) ································ 1
- Serial I/O (UART or clock synchronous) ································ 1
- A-D converter (8-bit resolution) ········· 3 channels (DIP)
  8 channels (QFP)
- D-A converter (8-bit resolution) ················· 2 channels
- PWM output (8-bit or 16-bit) ································ 1
- Programmable I/O ports
  (Ports P0, P1, P2, P3, P5, P6) ································ 48
- Input port (Port P4) ························ 3 (DIP), 8 (QFP)
- Output ports (Ports D-A$_1$, D-A$_2$) ································ 2
- PROM (equivalent to the M5L2764)
  program voltage ································ 21V

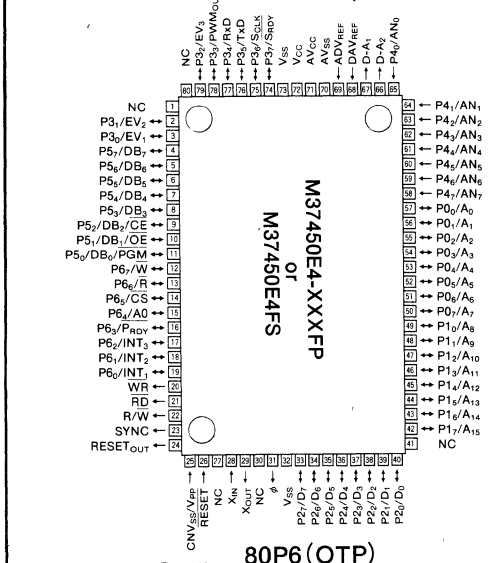
APPLICATION

Slave controller for PPCs, facsimiles, and page printers
HDD, optical disk, inverter, and industrial motor controllers
Industrial robots and machines

PIN CONFIGURATION (TOP VIEW)



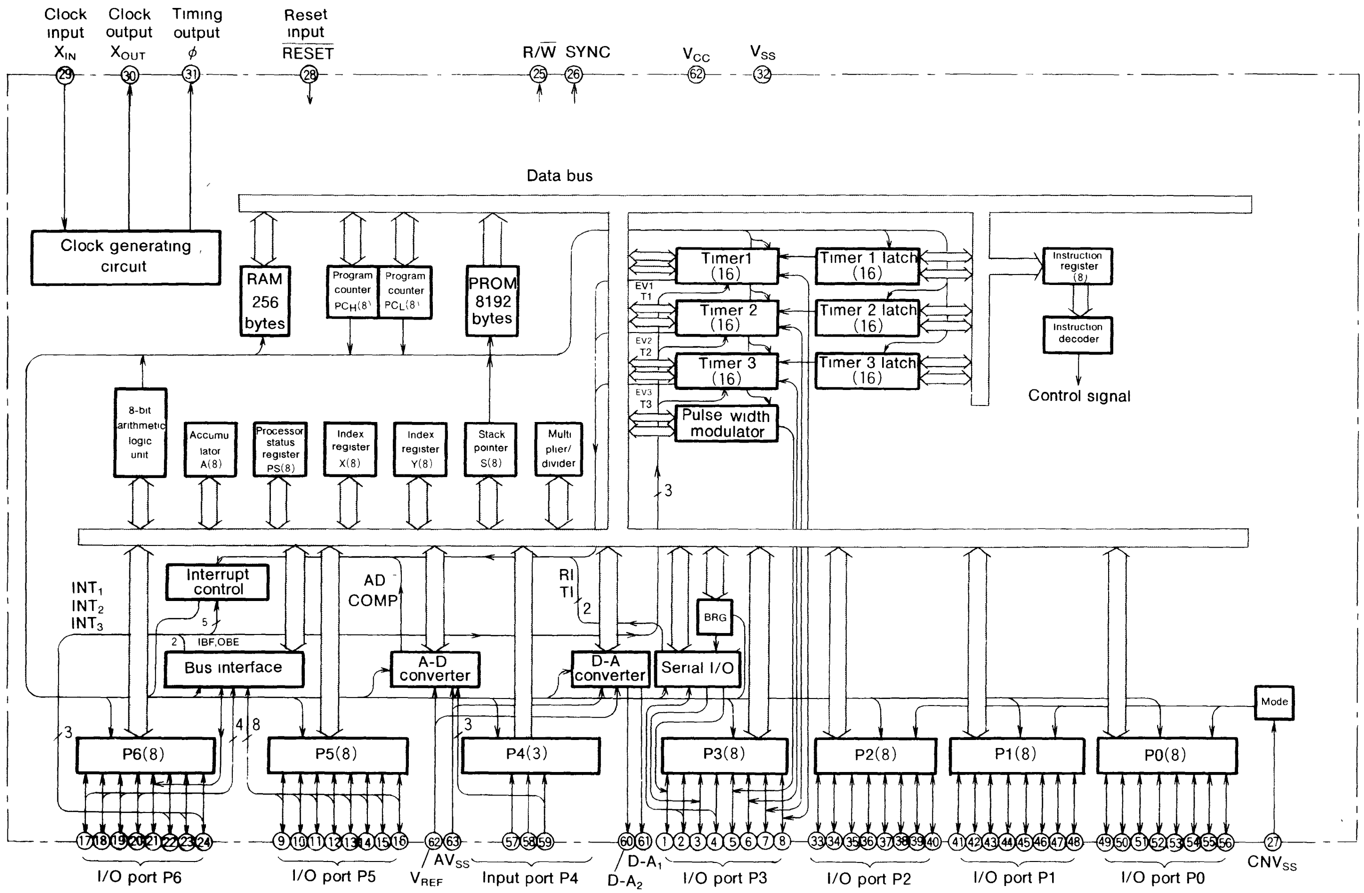
Outline 64P4B(OTP)
64S1B(Window)



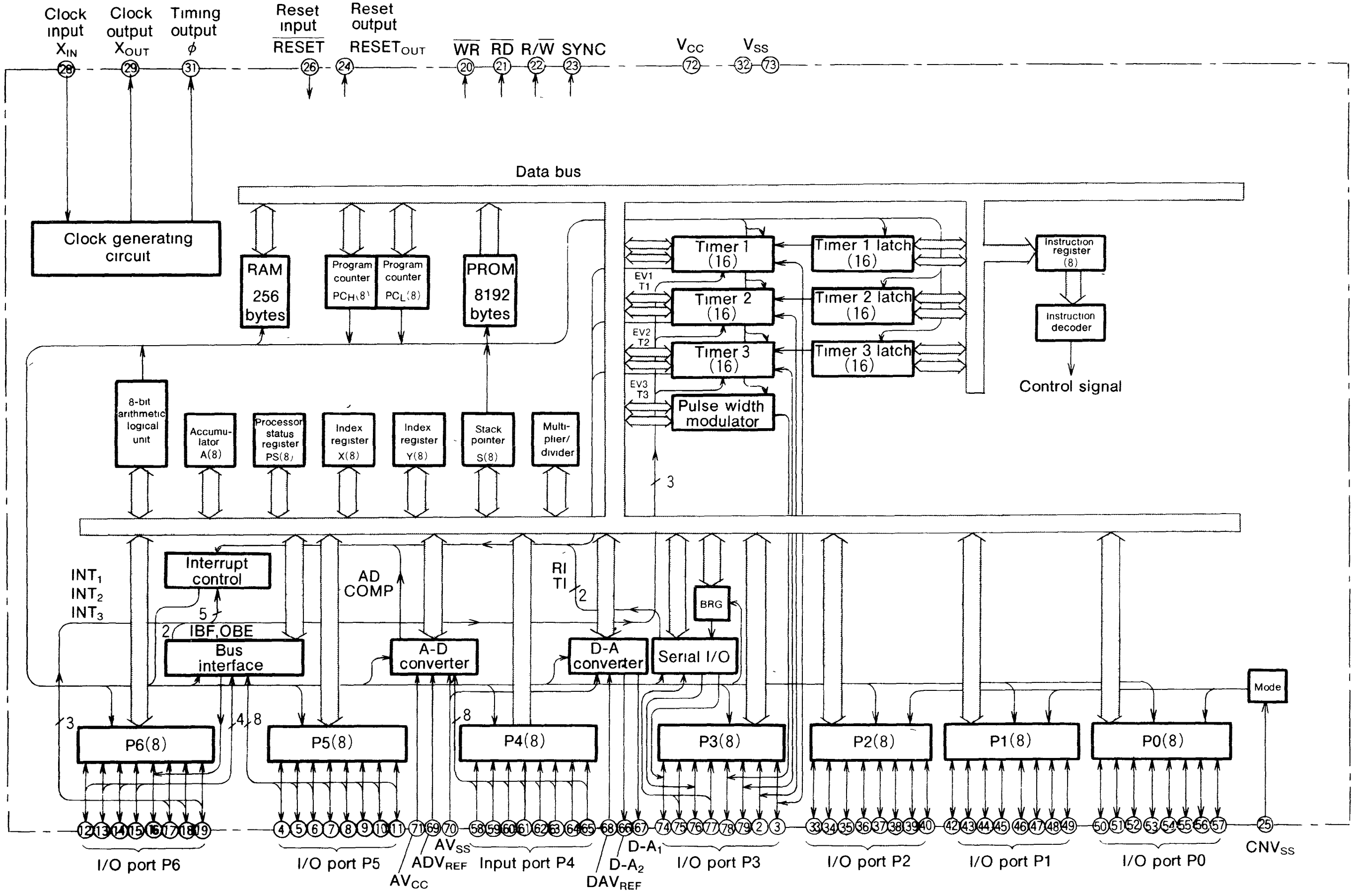
Outline 80P6(OTP)
80S6(Window)

NC : No connection

M37450E4-XXXSP, M37450E4SS BLOCK DIAGRAM



M37450E4-XXXFP, M37450E4FS BLOCK DIAGRAM



MITSUBISHI ELECTRIC

FUNCTIONS OF M37450E4-XXXSP/FP, M37450E4SS/FS

Parameter			Functions
Number of basic instructions			71(69 MELPS 740 basic instructions+2)
Instruction execution time			0. 8μs (minimum instructions, at 10MHz frequency)
Clock frequency			10MHz (max)
Memory size	PROM		8192 bytes
	RAM		256 bytes
Input/Output port	P0-P3, P5, P6	I/O	8-bit×6
	P4	Input	3-bit×1 (8-bit×1 for 80-pin model)
	D-A	Output	2-bit×1
Serial I/O			UART or clock synchronous
Timers			16-bit timer×3, 8-bit timer (Serial I/O baud rate generator)×1
A-D converter			8-bit×3 channels (8 channels for 80-pin model)
D-A converter			8-bit×2 channels
Pulse width modulator			8-bit or 16-bit×1
Data bus buffer			1-byte input and output each
Subroutine nesting			96-levels
Interrupt			6 external interrupts, 8 internal interrupts One software interrupt
Clock generating circuit			Built-in (ceramic or quarts crystal oscillator)
Supply voltage			5V±5%
Power dissipation			30mW (at 10MHz frequency)
Input/Output characters	Input/Output voltage		5V
	Output current		±5mA (max.)
Memory expansion			Possible
Operating temperature range			−10 to 70℃
Device structure			CMOS silicon gate
Package	M37450E4-XXXSP		64-pin shrink plastic molded DIP
	M37450E4-XXXFP		80-pin plastic molded QFP
	M37450E4SS		64-pin shrink ceramic DIP
	M37450E4FS		80-pin ceramic QFP

PIN DESCRIPTION (normal mode)

Pin	Name	Input/ Output	Functions
V_{CC}, V_{SS}	Supply voltage		Power supply inputs 5V±5% to V_{CC}, and 0V to V_{SS}
CNV_{SS}/V_{PP}	CNV_{SS}		Controls the processor mode of the chip Normally connected to V_{SS} or V_{CC}
$\overline{\text{RESET}}$	Reset input	Input	To enter the reset state, the reset input pin must be kept at a "L" for more than 8 clock cycles (under normal V_{CC} conditions) If more time is needed for the crystal oscillator to stabilize, this "L" condition should be maintained for the required time
X_{IN}	Clock input	Input	This chip has an internal clock generating circuit To control generating frequency, an external ceramic or a quartz crystal oscillator is connected between the X_{IN} and X_{OUT} pins If an external clock is used, the clock source should be connected to the X_{IN} pin and the X_{OUT} pin should be left open
X_{OUT}	Clock output	Output	
ϕ	Timing output	Output	Outputs signal consisting of oscillating frequency divided by four
SYNC	Synchronous signal output	Output	This signal is output "H" during operation code fetch and is used to control single stepping of programs
$R/\overline{W}$	Read/Write status output	Output	This signal determines the direction of the data bus It is "H" during read and "L" during write
$P0_0$-$P0_7$	I/O port P0	I/O	Port P0 is an 8-bit I/O port with directional registers allowing each I/O bit to be individually programmed as input or output The output structure is CMOS output The low-order bits of the address are output except in single-chip mode
$P1_0$-$P1_7$	I/O port P1	I/O	Port P1 is an 8-bit I/O port and has basically the same functions as port P0 The high-order bits of the address are output except in single-chip mode
$P2_0$-$P2_7$	I/O port P2	I/O	Port P2 is an 8-bit I/O port and has basically the same functions as port P0 Used as data bus except in single-chip mode
$P3_0$-$P3_7$	I/O port P3	I/O	Port P3 is an 8-bit I/O port and has basically the same functions as port P0 Serial I/O, PWM output, or event I/O function can be selected with a program
$P4_0$-$P4_2$ ($P4_0$-$P4_7$)	Input port P4	Input	Analog input pin for the A-D converter The 64-pin model has three pins and the 80-pin model has eight pins They may also be used as digital input pins
$P5_0$-$P5_7$	I/O port P5	I/O	Port P5 is an 8-bit I/O port and has basically the same functions as port P0 This port functions as an 8-bit data bus for the master CPU when slave mode is selected with a program
$P6_0$-$P6_7$	I/O port P6	I/O	Port P6 is an 8-bit I/O port and has basically the same function as port P0 Pins $P6_3$ to $P6_7$ change to a control bus for the master CPU when slave mode is selected with a program Pins $P6_0$ to $P6_2$ may be programmed as external interrupt input pins
D-A_1, D-A_2	D-A output	Output	Analog signal from D-A converter is output
V_{REF}	Reference voltage input	Input	Reference voltage input pin for A-D and D-A converter This pin is for 64-pin model only
ADV_{REF}	A-D reference voltage input	Input	Reference voltage input pin for A-D converter This pin is for 80-pin model only
DAV_{REF}	D-A reference voltage input	Input	Reference voltage input pin for D-A converter This pin is for 80-pin model only
AV_{SS}	Analog power supply		Ground level input pin for A-D and D-A converter Same voltage as V_{SS} is applied
AV_{CC}	Analog power supply		Power supply input pin for A-D converter This pin is for 80-pin model only Same voltage as V_{CC} is applied In the case of the 64-pin model, AV_{CC} is connected to V_{CC} internally
$\overline{\text{RD}}$	Read signal output	Output	Control signal output as active "L" when valid data is read from data bus This pin is for 80-pin model only
$\overline{\text{WR}}$	Write signal output	Output	Control signal output as active "L" when writing data from data bus to external component This pin is for 80-pin model only
$RESET_{OUT}$	Reset output	Output	Control signal output as active "H" during reset It is used as a reset output signal for peripheral components. This pin is for 80-pin model only

PIN DESCRIPTION (EPROM mode)

Pin	Name	Input/ Output	Functions
V_{CC}, V_{SS}	Supply voltage		Power supply inputs 5V±5% to V_{CC}, and 0V to V_{SS}
CNV_{SS}/V_{PP}	V_{PP}	Input	Connect to V_{PP} when programming or verifing.
$\overline{RESET}$	Reset input	Input	Connect to V_{SS}
X_{IN}	Clock input	Input	Connect a ceramic or a quartz crystal oscillator between X_{IN} and X_{OUT} for clock oscillation.
X_{OUT}	Clock output	Output	
ϕ	Timing output	Output	For timing output
SYNC	Synchronous signal output	Output	Kept to open ("L" signal is output)
$R/\overline{W}$	Read/Write status output	Output	Kept to open ("H" signal is output)
$P0_0$-$P0_7$	I/O port P0	Input	P0 works as the lower 8-bit address input
$P1_0$-$P1_7$	I/O port P1	Input	P1 works as the higher 8-bit address input
$P2_0$-$P2_7$	I/O port P2	I/O	P2 works as an 8-bit data bus
$P3_0$-$P3_7$	I/O port P3	Input	Connect to V_{SS}
$P4_0$-$P4_2$ ($P4_0$-$P4_7$)	Input port P4	Input	Connect to V_{SS} (The 80-pin model has eight pins $P4_0$ to $P4_7$)
$P5_0$-$P5_7$	I/O port P5	Input	$P5_0$, $P5_1$, $P5_2$ works as $\overline{PGM}$, $\overline{OE}$, and $\overline{CE}$ inputs respectively Connect $P5_3$ and $P5_4$ to V_{CC} and $P5_5$ to $P5_7$ to V_{SS}
$P6_0$-$P6_7$	I/O port P6	Input	Connect to V_{SS}
D-A_1, D-A_2	D-A output	Output	Kept to open
V_{REF}	Reference voltage input	Input	Connect to V_{SS}
ADV_{REF}	A-D reference voltage input	Input	Connect to V_{SS}.
DAV_{REF}	D-A reference voltage input	Input	Connect to V_{SS}.
AV_{SS}	Analog power	Input	Connect to V_{SS}
AV_{CC}	Analog power	Input	Connect to V_{CC} or V_{SS}.
$\overline{RD}$	Read signal output	Output	Kept to open ("H" signal is output)
$\overline{WR}$	Write signal output	Output	Kept to open ("H" signal is output).
$RESET_{OUT}$	Reset output	Output	Kept to open ("H" signal is output)

EPROM MODE

The M37450E4-XXXSP/FP, M37450E4SS/FS features an EPROM mode in addition to its normal modes. When the $\overline{RESET}$ signal level is low ("L") and CNV_{SS}/V_{PP} signal level is high ("H"), the chip automatically enters the EPROM mode. Table 1 list the correspondence between pins and Figure 1 and Figure 2 give the pin connections in the EPROM mode. When in the EPROM mode, ports P0, P1, P2, $P5_0$ to $P5_2$ and CNV_{SS} are used for the PROM (equivalent to the M5L2764). When in this mode, the built-in PROM can be written to or read from using these pins in the same way as with the M5L2764. The oscillator should be connected to the X_{IN} and X_{OUT} pins, or external clock should be connected to the X_{IN} pin.

Table 1. Pin function in EPROM mode

	M37450E4-XXXSP/FP, M37450E4SS/FS	M5L2764
V_{CC}	V_{CC}	V_{CC}
V_{PP}	CNV_{SS}/V_{PP}	V_{PP}
V_{SS}	V_{SS}	V_{SS}
Address input	Ports P0, $P1_0$-$P1_4$	A_0-A_{12}
Data I/O	Port P2	D_0-D_7
$\overline{CE}$	$P5_2/DB_2/\overline{CE}$	$\overline{CE}$
$\overline{OE}$	$P5_1/DB_1/\overline{OE}$	$\overline{OE}$
$\overline{PGM}$	$P5_0/DB_0/\overline{PGM}$	$\overline{PGM}$

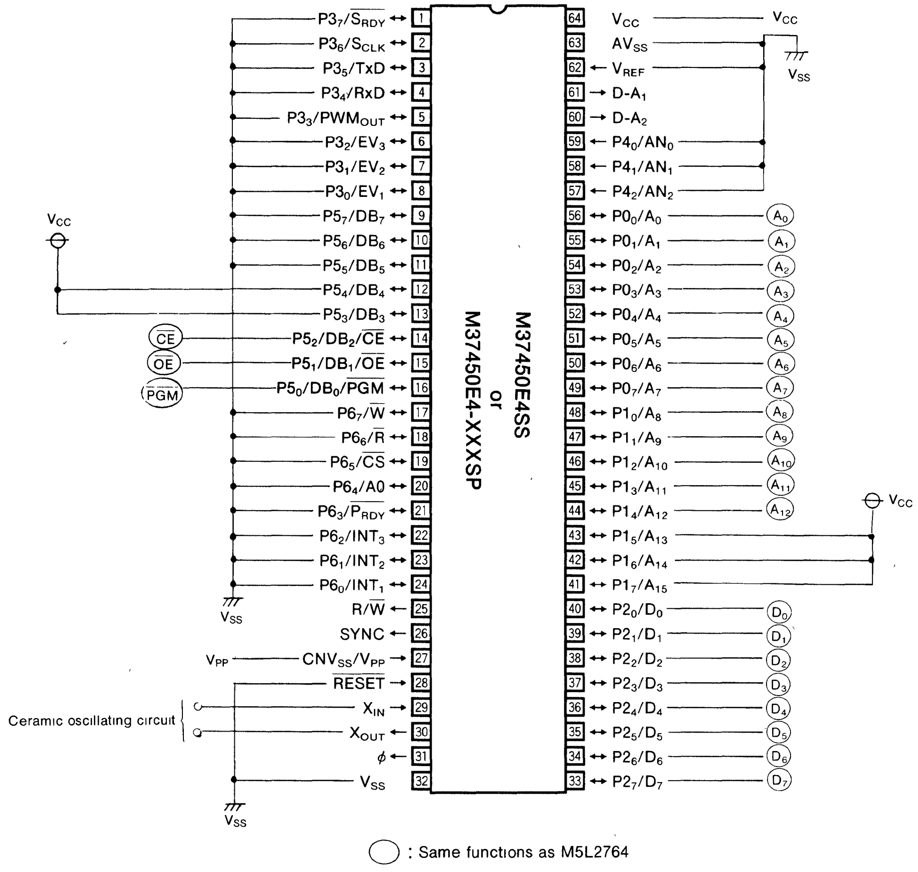


Fig. 1 Pin connection in EPROM mode (64-pin model)

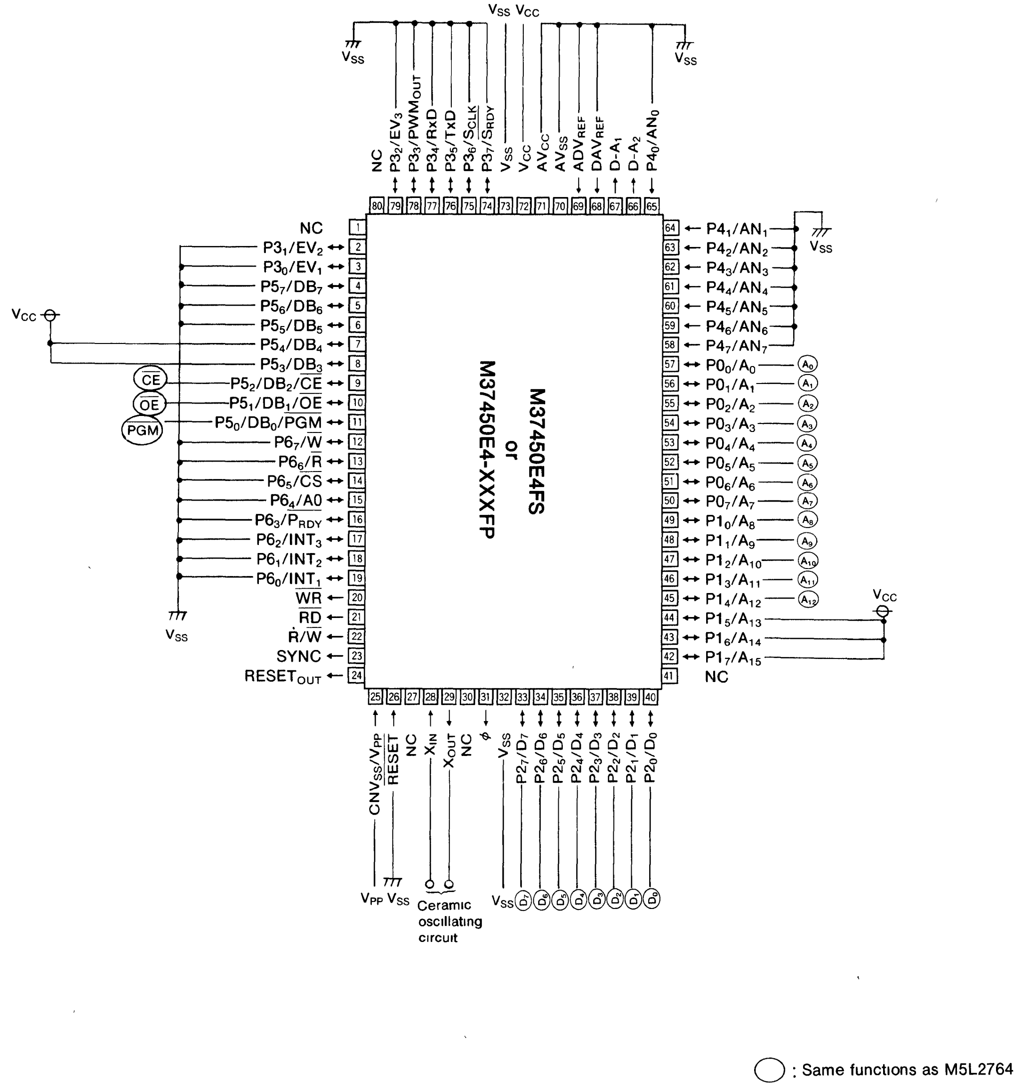


Fig. 2 Pin connection in EPROM mode (80-pin model)

PROM READING, WRITING AND ERASING

Reading

To read the PROM, set the $\overline{CE}$ and $\overline{OE}$ pins to a "L" level, and supply 0V to the $\overline{RESET}$ pin, and 5V to the V_{CC} and the CNV_{SS} (V_{PP}) pins. Input the address of the data (A_0 to A_{12}) to be read and the data will be output to the I/O pins D_0 to D_7. The data I/O pins will be floating when either the $\overline{CE}$ or $\overline{OE}$ pins are in the "H" state.

Writing

To write to the PROM, set the $\overline{CE}$ pin to a "L" level and the $\overline{OE}$ pin to a "H" level, and supply 0V to the $\overline{RESET}$ pin, 6V to the V_{CC} pin and 21V to the V_{PP} pin. The CPU will enter the program mode when V_{PP} is applied to the V_{PP} pin. The address to be written to is selected with pins A_0 to A_{12}, and the data to be written is input to pins D_0 to D_7. Set the $\overline{PGM}$ pin to a "L" level to begin writing.

Erasing

Data can only erased on the M37450E4SS/FS ceramic package, which includes a window. To erase data on this chip, use an ultraviolet light source with a 2537 Angstrom wave length. The minimum radiation power necessary for erasing is 15W•s/cm^2.

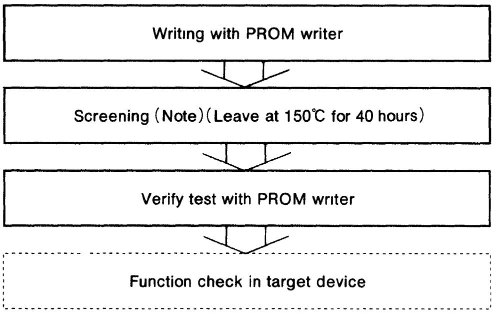
NOTES ON HANDLING

(1) Sunlight and fluorescent light contain wave lengths capable of erasing data. For ceramic package types, cover the transparent window with a seal (provided) when this chip is in use. However, this seal must not contact the lead pins.

(2) Before erasing, the glass should be cleaned and stains such as finger prints should be removed thoroughly. If these stains are not removed, complete erasure of the data could be prevented.

(3) Since a high voltage (21V) is used to write data, care should be taken when turning on the PROM writer's power.

(4) For the programmable microcomputer (shipped in blank or OTP type) , Mitsubishi does not perform PROM write test and screening in the assembly process and following process. To improve reliability after write, performing write and test according to the flow below before use is recommended.



Note : Since the screening temperature is higher than storage temperature, never expose to 150℃ exceeding 100 hours.

Table 2. I/O signal in each mode

Mode \ Pin	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	V_{PP}	V_{CC}	Port P2
• Read-out	V_{IL}	V_{IL}	V_{IH}	5V	5V	Output
Programming	V_{IL}	V_{IH}	V_{IL}	21V	6V	Input
Programming verify	V_{IL}	V_{IL}	V_{IH}	21V	6V	Output
Program disable	V_{IH}	X	X	21V	6V	Floating

Note 1 : V_{IL} and V_{IH} indicate a "L" and "H" input voltage, respectively
2 : An X indicates either V_{IL} or V_{IH}.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS} Output transistors are at "OFF" state	−0. 3 to 7	V
V_I	Input voltage $\overline{RESET}$, X_{IN}		−0. 3 to 7	V
V_I	Input voltage $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, ADV_{REF}, DAV_{REF}, V_{REF}, AV_{CC}		−0. 3 to V_{CC}+0. 3	V
V_I	Input voltage CNV_{SS}		−0. 3 to 13 (Note 1)	V
V_O	Output voltage $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, X_{OUT}, ϕ, $\overline{RD}$, $\overline{WR}$, R/$\overline{W}$, $RESET_{OUT}$, SYNC		−0. 3 to V_{CC}+0. 3	V
Pd	Power dissipation	T_a = 25℃	1000 (Note 2)	mW
Topr	Operating temperature		−10 to 70	℃
Tstg	Storage temperature		−40 to 125	℃

Note 1 : In PROM programming mode, CNV_{SS} is 22. 0V
2 : 500mW for QFP type

RECOMMENDED OPERATING CONDITIONS

(V_{CC}=5V±5%, Ta=−10 to 70℃ unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max.	
V_{CC}	Supply voltage	4. 75	5	5. 25	V
V_{SS}	Supply voltage		0		V
V_{IH}	"H" Input voltage $\overline{RESET}$, X_{IN}, CNV_{SS} (Note 1)	0. $8V_{CC}$		V_{CC}	V
V_{IH}	"H" Input voltage $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$ (except Note 1)	2. 0		V_{CC}	V
V_{IL}	"L" Input voltage CNV_{SS} (Note 1)	0		0. $2V_{CC}$	V
V_{IL}	"L" Input voltage $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$ (except Note 1)	0		0. 8	V
V_{IL}	"L" Input voltage $\overline{RESET}$	0		0. $12V_{CC}$	V
V_{IL}	"L" Input voltage X_{IN}	0		0. $16V_{CC}$	V
I_{OL}(peak)	"L" peak output current $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$			10	mA
I_{OL}(avg)	"L" average output current $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$ (Note 2)			5	mA
I_{OH}(peak)	"H" peak output current $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$			−10	mA
I_{OH}(avg)	"H" average output current $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$ (Note 2)			−5	mA
$f(X_{IN})$	Clock oscillating frequency	1		10	MHz

Note 1 : Ports operate as INT_1-INT_3($P6_0$-$P6_2$), EV_1-EV_3($P3_0$-$P3_2$), R_XD($P3_4$) and S_{CLK}($P3_6$)
2 : The average output current I_{OH}(avg) and I_{OL}(avg) are the average value during a 100ms
3 : The total of "L" output current I_{OL}(peak) of port P0, P1 and P2 is less than 40mA
The total of "H" output current I_{OH}(peak) of port P0, P1 and P2 is less than 40mA
The total of "L" output current I_{OL}(peak) of port P3, P5, P6, R/$\overline{W}$, SYNC, $RESET_{OUT}$, $\overline{RD}$, $\overline{WR}$ and ϕ is less than 40mA
The total of "H" output current I_{OH}(peak) of port P3, P5, P6, R/$\overline{W}$, SYNC, $RESET_{OUT}$, $\overline{RD}$, $\overline{WR}$ and ϕ is less than 40mA

ELECTRICAL CHARACTERISTICS (V_{CC} = 5V±5%, V_{SS} = 0V, T_a = −10 to 70℃, f(X_{IN}) = 10MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ	Max	
V_{OH}	"H" output voltage $\overline{RD}$, $\overline{WR}$, R/$\overline{W}$, SYNC, $RESET_{OUT}$, φ	I_{OH}=−2mA	V_{CC}−1			V
V_{OH}	"H" output voltage $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$	I_{OH}=−5mA	V_{CC}−1			V
V_{OL}	"L" output voltage $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $\overline{RD}$, $\overline{WR}$, R/$\overline{W}$, SYNC, $RESET_{OUT}$, φ	I_{OL}=2mA			0.45	V
V_{OL}	"L" output voltage $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$	I_{OL}=5mA			1	V
$V_{T+}-V_{T-}$	Hysterisis INT_1-INT_3($P6_0$-$P6_2$), EV_1-EV_3($P3_0$-$P3_2$), R_XD($P3_4$), S_{CLK}($P3_6$)	Function input level	0.3		1	V
$V_{T+}-V_{T-}$	Hysterisis $\overline{RESET}$				0.7	V
$V_{T+}-V_{T-}$	Hysterisis X_{IN}		0.1		0.5	V
I_{IL}	"L" input current $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $\overline{RESET}$, X_{IN}	V_I=V_{SS}	−5		5	μA
I_{IH}	"H" input current $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $\overline{RESET}$, X_{IN}	V_I=V_{CC}	−5		5	μA
V_{RAM}	RAM retention voltage	At stop mode	2			V
I_{CC}	Supply current	At system operation f(X_{IN})=10MHz		6	10	mA
		At stop mode (Note 1)		1	10	μA

Note 1 : The terminals $\overline{RD}$, $\overline{WR}$, R/$\overline{W}$, SYNC, $RESET_{OUT}$, φ, D-A_1 and D-A_2 are all open The other ports, which are in the input mode, are connected to V_{SS} A-D converter is in the A-D completion state The current through ADV_{REF} and DAV_{REF} is not included(Fig 6)

A-D CONVERTER CHARACTERISTICS

(V_{CC} = AV_{CC} = 5V, V_{SS} = AV_{SS} = 0V, T_a = 25℃, f(X_{IN})=10MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
—	Resolution				8	Bits
—	Absolute accuracy	V_{CC}=AV_{CC}=ADV_{REF}=5.12V		±1.5	±3	LSB
t_{CONV}	Conversion time				49	t_C(φ)
V_{IA}	Analog input voltage		AV_{SS}		AV_{CC}	V
V_{ADVREF}	Reference input voltage		2		V_{CC}	V
R_{LADDER}	Ladder resistance value	ADV_{REF}=5V	2	7.5	10	kΩ
$I_{IADVREF}$	Reference input current	ADV_{REF}=5V	0.5	0.7	2.5	mA
V_{AVCC}	Analog power supply input voltage			V_{CC}		V
V_{AVSS}	Analog power supply input voltage			0		V

D-A CONVERTER CHARACTERISTICS (V_{CC} = 5V, V_{SS} = AV_{SS} = 0V, T_a = 25℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
—	Resolution				8	Bits
—	Abusolute accuracy	V_{CC}=DAV_{REF}=5.12V			1.0	%
t_{SU}	Setup time				3	μs
R_O	Output resistance		1	2	4	kΩ
V_{AVSS}	Analog power supply input voltage			0		V
V_{DAVREF}	Reference input voltage		4		V_{CC}	V
I_{DAVREF}	Reference power input current (Each pin)		0	2.5	5	mA

TIMING REQUIREMENTS

Port/single-chip mode (V_{CC}=5V±5%, V_{SS}=0V, T_a=−10 to 70℃, unless otherwise noted)

Symbol	Parameter	Test condition	Limits			Unit
			Min	Typ.	Max	
$t_{su(P0D-\phi)}$	Port P0 input setup time	Fig 3	200			ns
$t_{su(P1D-\phi)}$	Port P1 input setup time		200			ns
$t_{su(P2D-\phi)}$	Port P2 input setup time		200			ns
$t_{su(P3D-\phi)}$	Port P3 input setup time		200			ns
$t_{su(P4D-\phi)}$	Port P4 input setup time		200			ns
$t_{su(P5D-\phi)}$	Port P5 input setup time		200			ns
$t_{su(P6D-\phi)}$	Port P6 input setup time		200			ns
$t_{h(\phi-P0D)}$	Port P0 input hold time		40			ns
$t_{h(\phi-P1D)}$	Port P1 input hold time		40			ns
$t_{h(\phi-P2D)}$	Port P2 input hold time		40			ns
$t_{h(\phi-P3D)}$	Port P3 input hold time		40			ns
$t_{h(\phi-P4D)}$	Port P4 input hold time		40			ns
$t_{h(\phi-P5D)}$	Port P5 input hold time		40			ns
$t_{h(\phi-P6D)}$	Port P6 input hold time		40			ns
$t_c(X_{IN})$	External clock input cycle time		100		1000	ns
$t_w(X_{IN}L)$	External clock input "L" pulse width		30			ns
$t_w(X_{IN}H)$	External clock input "H" pulse width		30			ns
$t_r(X_{IN})$	External clock rising edge time				20	ns
$t_f(X_{IN})$	External clock falling edge time				20	ns

Master CPU bus interface timing ($\overline{R}$ and $\overline{W}$ separation type mode)

(V_{CC}=5V±5%, V_{SS}=0V, T_a=−10 to 70℃, unless otherwise noted)

Symbol	Parameter	Test condition	Limits			Unit
			Min	Typ	Max	
$t_{su(CS-R)}$	$\overline{CS}$ setup time	Fig 3	0			ns
$t_{su(CS-W)}$	$\overline{CS}$ setup time		0			ns
$t_{h(R-CS)}$	$\overline{CS}$ hold time		0			ns
$t_{h(W-CS)}$	$\overline{CS}$ hold time		0			ns
$t_{su(A-R)}$	A0 setup time		40			ns
$t_{su(A-W)}$	A0 setup time		40			ns
$t_{h(R-A)}$	A0 hold time		10			ns
$t_{h(W-A)}$	A0 hold time		10			ns
$t_{w(R)}$	Read pulse width		160			ns
$t_{w(W)}$	Write pulse width		160			ns
$t_{su(D-W)}$	Date input setup time before write		100			ns
$t_{h(W-D)}$	Date input hold time after write		10			ns

Master CPU bus interface timing (R/$\overline{W}$ type mode)

(V_{CC}=5V±5%, V_{SS}=0V, T_a=−10 to 70℃, unless otherwise noted)

Symbol	Parameter	Test condition	Limits			Unit
			Min	Typ	Max	
$t_{su(CS-E)}$	$\overline{CS}$ setup time	Fig 4	0			ns
$t_{h(E-CS)}$	$\overline{CS}$ hold time		0			ns
$t_{su(A-E)}$	A0 setup time		40			ns
$t_{h(E-A)}$	A0 hold time		10			ns
$t_{su(RW-E)}$	R/$\overline{W}$ setup time		40			ns
$t_{h(E-RW)}$	R/$\overline{W}$ hold time		10			ns
$t_{w(EL)}$	Enable clock "L" pulse width		160			ns
$t_{w(EH)}$	Enable clock "H" pulse width		160			ns
$t_{r(E)}$	Enable clock rising edge time				25	ns
$t_{f(E)}$	Enable clock falling edge time				25	ns
$t_{su(D-E)}$	Data input setup time before write		100			ns
$t_{h(E-D)}$	Data input hold time after write		10			ns

Local bus/memory expansion mode, microprocessor mode

(V_{CC}=5V±5%, V_{SS}=0V, T_a=−10 to 70℃, unless otherwise noted)

Symbol	Parameter	Test condition	Limits			Unit
			Min	Typ	Max	
$t_{su(D-\phi)}$	Data input setup time	Fig 5	130			ns
$t_{h(\phi-D)}$	Data input hold time		0			ns
$t_{su(D-RD)}$	Data input setup time		130			ns
$t_{h(RD-D)}$	Data input hold time		0			ns

SWITCHING CHARACTERISTICS

Port/single-chip mode (V_{CC}=5V±5%, V_{SS}=0V, T_a=−10 to 70℃, unless otherwise noted)

Symbol	Parameter	Test condition	Limits			Unit
			Min	Typ	Max	
$t_{d(\phi-P0Q)}$	Port P0 data output delay time	Fig 3			200	ns
$t_{d(\phi-P1Q)}$	Port P1 data output delay time				200	ns
$t_{d(\phi-P2Q)}$	Port P2 data output delay time				200	ns
$t_{d(\phi-P3Q)}$	Port P3 data output delay time				200	ns
$t_{d(\phi-P5Q)}$	Port P5 data output delay time				200	ns
$t_{d(\phi-P6Q)}$	Port P6 data output delay time				200	ns
$t_{c(\phi)}$	Cycle time		400		4000	ns
$t_{w(\phi H)}$	ϕ clock pulse width ("H" level)		190			ns
$t_{w(\phi L)}$	ϕ clock pulse width ("L" level)		170			ns
$t_{r(\phi)}$	ϕ clock rising edge time				20	ns
$t_{f(\phi)}$	ϕ clock falling edge time				20	ns

Master CPU bus interface ($\overline{R}$ and $\overline{W}$ separation type mode)

(V_{CC}=5V±5%, V_{SS}=0V, T_a=−10 to 70℃, unless otherwise noted)

Symbol	Parameter	Test condition	Limits			Unit
			Min	Typ	Max	
$t_{a(R-D)}$	Data output enable time after read	Fig 4			120	ns
$t_{v(R-D)}$	Data output disable time after read		10		85	ns
$t_{PLH(R-PR)}$	$\overline{\mathrm{P}}_{\mathrm{RDY}}$ output transmission time after read				150	ns
$t_{PLH(W-PR)}$	$\overline{\mathrm{P}}_{\mathrm{RDY}}$ output transmission time after write				150	ns

Master CPU bus interface (R/$\overline{W}$ type mode) (V_{CC}=5V±5%, V_{SS}=0V, T_a=−10 to 70℃, unless otherwise noted)

Symbol	Parameter	Test condition	Limits			Unit
			Min	Typ	Max	
$t_{a(E-D)}$	Data output enable time after read	Fig 4			120	ns
$t_{v(E-D)}$	Data output disable time after read		10		85	ns
$t_{PLH(E-PR)}$	$\overline{\mathrm{P}}_{\mathrm{RDY}}$ output transmission time after E clock				150	ns

Local bus/memory expansion mode, microprocessor mode

(V_{CC}=5V±5%, V_{SS}=0V, T_a=−10 to 70℃, unless otherwise noted)

Symbol	Parameter	Test condition	Limits			Unit
			Min	Typ	Max	
$t_{d(\phi-A)}$	address delay time after ϕ	Fig 5			150	ns
$t_{v(\phi-A)}$	address effective time after ϕ		10			ns
$t_{v(RD-A)}$	address effective time after $\overline{RD}$		10			ns
$t_{v(WR-A)}$	address effective time after $\overline{WR}$		10			ns
$t_{d(\phi-D)}$	data output delay time after ϕ				160	ns
$t_{d(WR-D)}$	data output delay time after $\overline{WR}$				160	ns
$t_{v(\phi-D)}$	data output effective time after ϕ		20			ns
$t_{v(WR-D)}$	data output effective time after $\overline{WR}$		20			ns
$t_{d(\phi-RW)}$	R/$\overline{W}$ delay time after ϕ				150	ns
$t_{d(\phi-SYNC)}$	SYNC delay time after ϕ				150	ns
$t_{w(RD)}$	$\overline{RD}$ pulse width		170			ns
$t_{w(WR)}$	$\overline{WR}$ pulse width		170			ns

TEST CONDITION

Input voltage level : V_{IH} 2.4V
V_{IL} 0.45V
Output test level : V_{OH} 2.0V
V_{OL} 0.8V

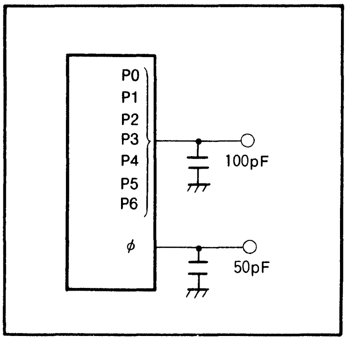


Fig. 3 Test circuit in single-chip mode

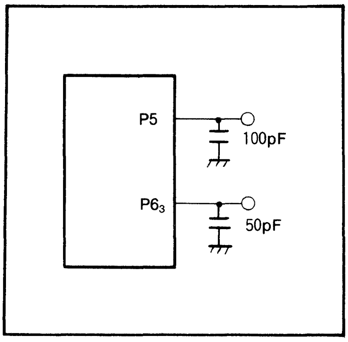


Fig. 4 Master CPU bus interface test circuit

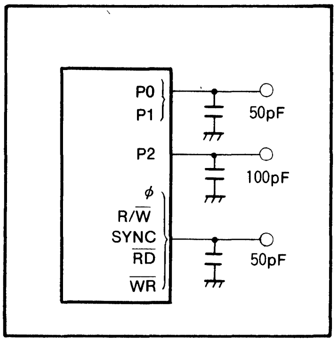


Fig. 5 Local bus test circuit

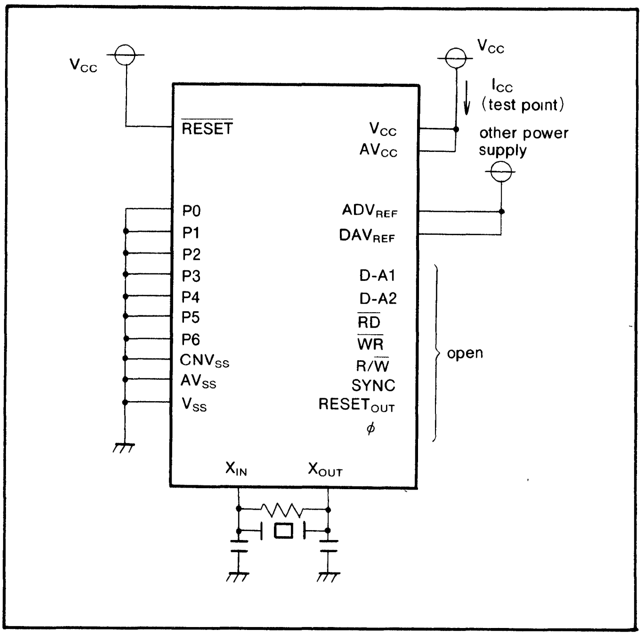
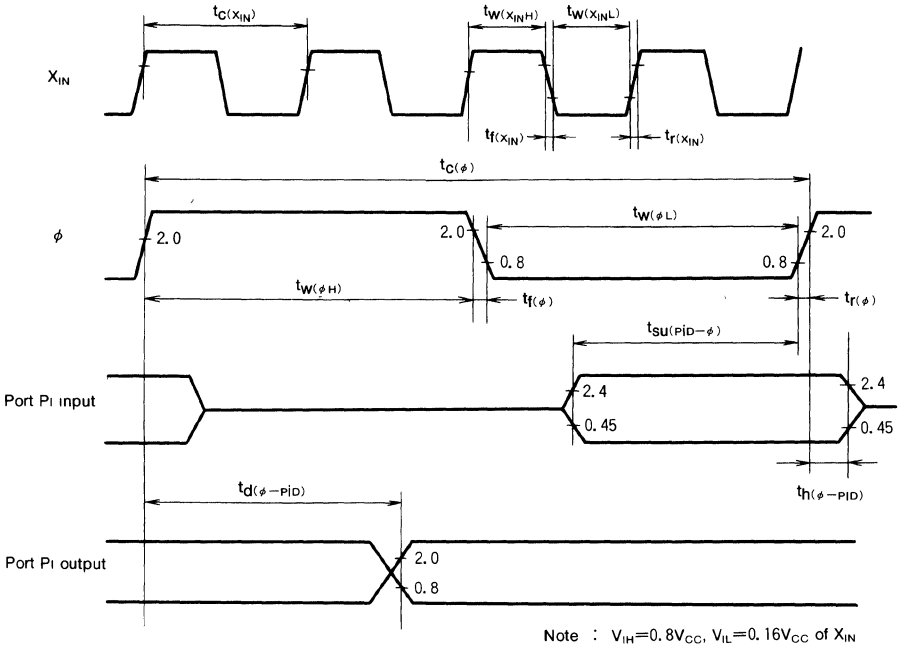


Fig. 6 I_{CC} (at STOP mode) test condition

TIMING DIAGRAM

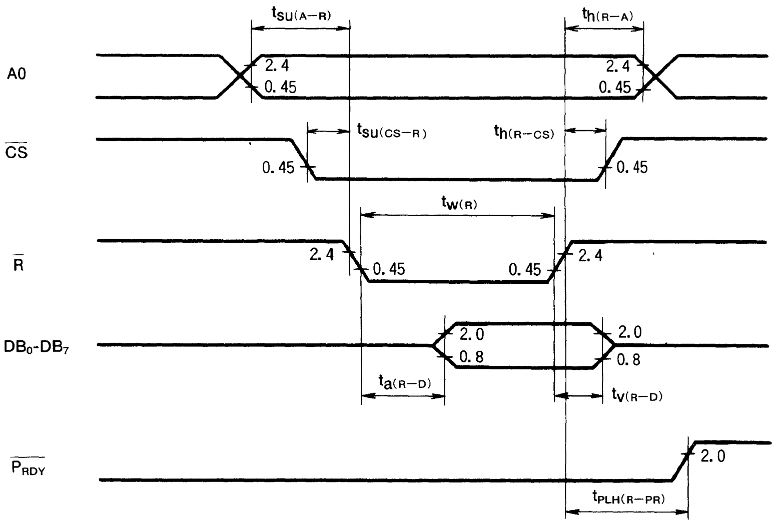
Port/single-chip mode timing diagram



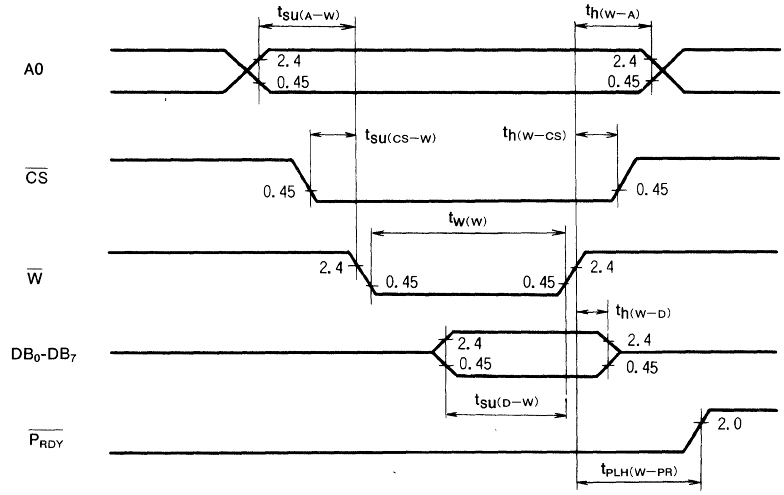
Note : V_{IH}=0.8V_{CC}, V_{IL}=0.16V_{CC} of X_{IN}

Master CPU bus interface/ $\overline{R}$ and $\overline{W}$ separation type timing diagram

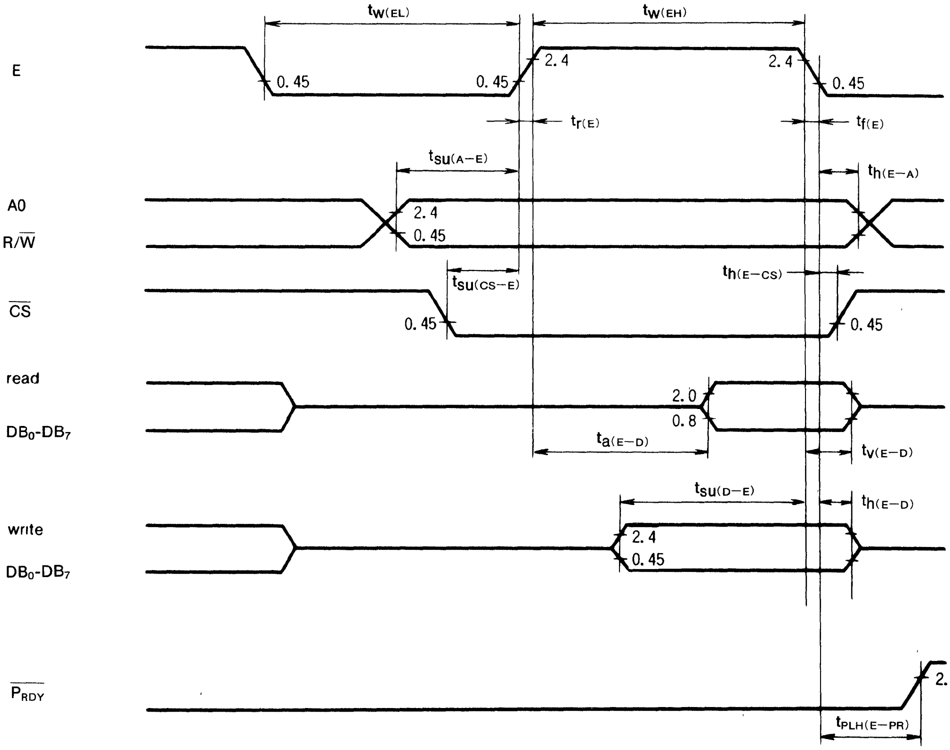
Read



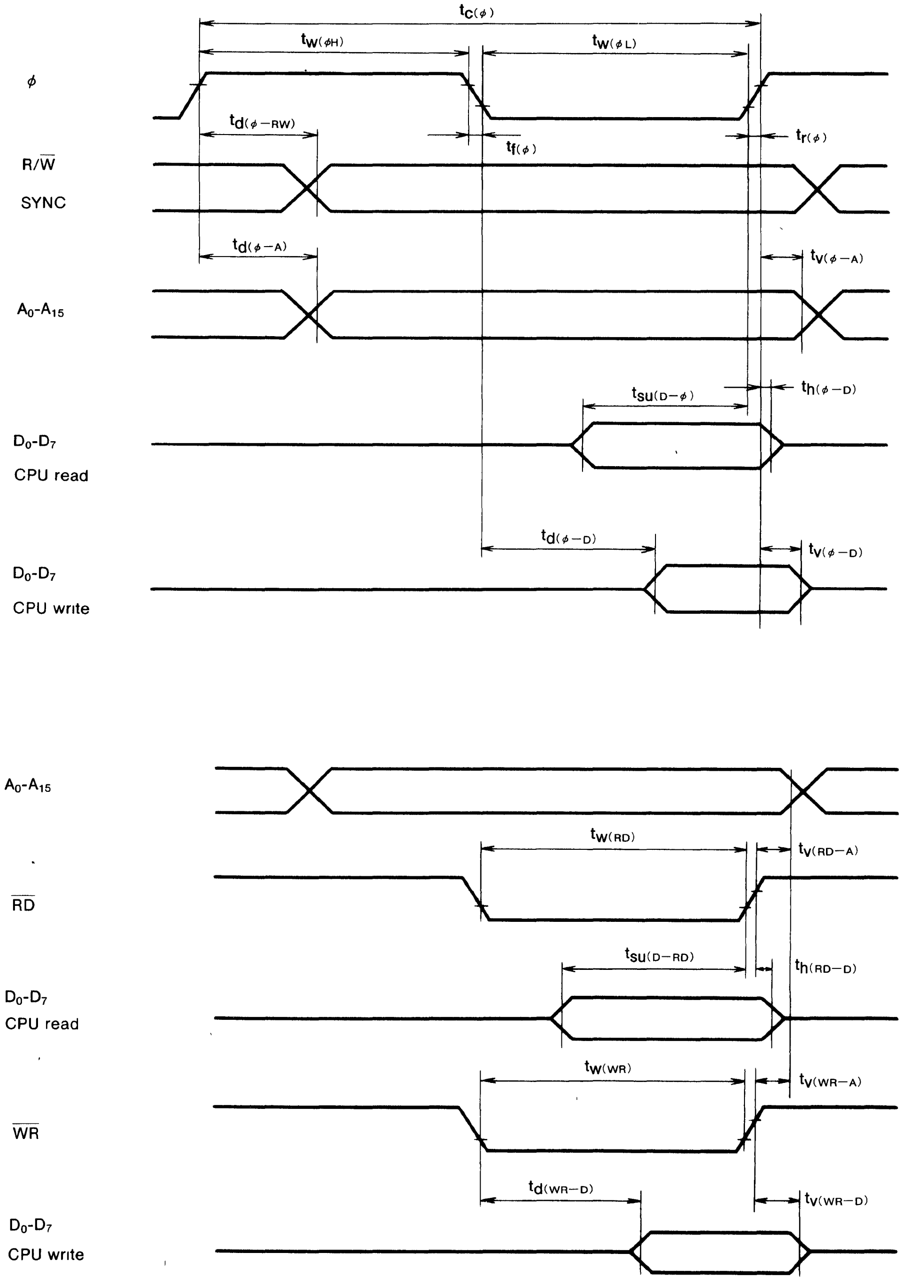
Write



Master CPU interface/ R/W type timing diagram



Local bus timing diagram



M37450E8-XXXSP/FP
M37450E8SS/FS
PROM VERSION of M37450M8-XXXSP/FP

DESCRIPITION

The M37450E8-XXXSP is a single-chip microcomputer designed with CMOS silicon gate technology. It is housed in a 64-pin shrink plastic molded DIP. The features of this chip are similar to those of the M37450M8-XXXSP except that this chip has a 16384-byte PROM built-in. This single-chip microcomputer is useful for office automation appliances and consumer appliance controllers.

In addition to its simple instruction sets, the PROM, RAM and I/O addresses are placed on the same memory map to enable easy programming. Since general purpose PROM writes can be used for small quantity production runs. It also has a unique feature that enables it to be used as a slave microcomputer.

The M37450E8SS and the M37450E8FS are the window type (M37450E8FS is housed in a 80-pin ceramic QFN package). The differences between the M37450E8-XXXSP and the M37450E8-XXXFP, and between the M37450E8SS and the M37450E8FS are the package outline and the power dissipation ability (absolute maximum ratings).

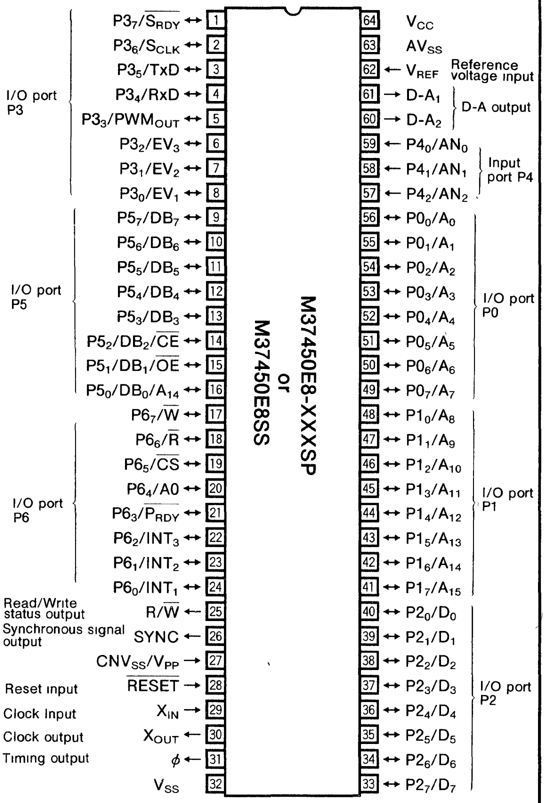
FEATURES

- Number of basic instructions ········· 71
  69 MELPS 740 basic instructions + 2 multiply/divide instructions
- Memory size EPROM ········· 16384 bytes
  RAM ········· 384 bytes
- Instruction execution time
  (minimum instructions at 10 MHz frequency) ····· 0.8μs
- Single power supply ········· 5V±5%
- Power dissipation normal operation mode
  (at 10 MHz frequency) ········· 30mW
- Subroutine nesting ········· 96 levels max.
- Interrupt ········· 15 events
- Master CPU bus interface ········· 1 byte
- 16-bit timer ········· 3
- 8-bit timer (Serial I/O use) ········· 1
- Serial I/O (UART or clock synchronous) ········· 1
- A-D converter (8-bit resolution) ········· 3 channels (DIP)
  8 channels (QFP)
- D-A converter (8-bit resolution) ········· 2 channels
- PWM output (8-bit or 16-bit) ········· 1
- Programmable I/O ports
  (Ports P0, P1, P2, P3, P5, P6) ········· 48
- Input port (Port P4) ········· 3 (DIP), 8 (QFP)
- Output ports (Ports D-A$_1$, D-A$_2$) ········· 2
- EPROM (equivalent to the M5L27256)
  program voltage ········· 12.5V

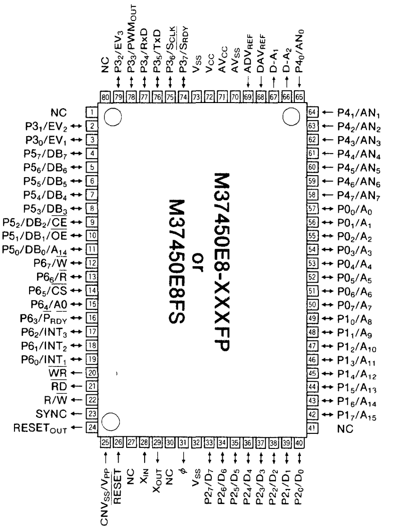
APPLICATION

Slave controller for PPCs, facsimiles, and page printers
HDD, optical disk, inverter, and industrial motor controllers
Industrial robots and machines

PIN CONFIGURATION (TOP VIEW)



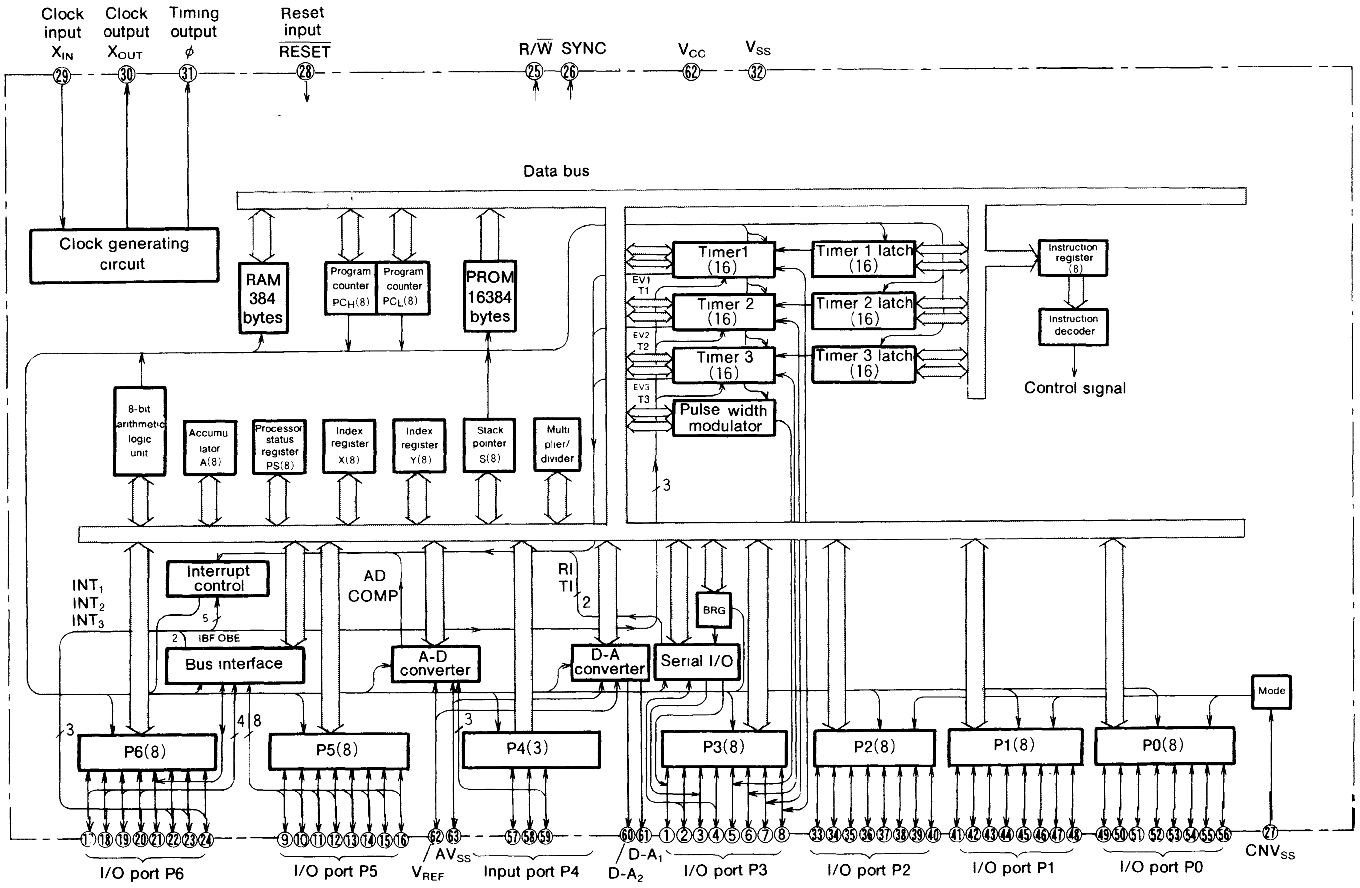
Outline 64P4B (OTP)
64S1B (Window)



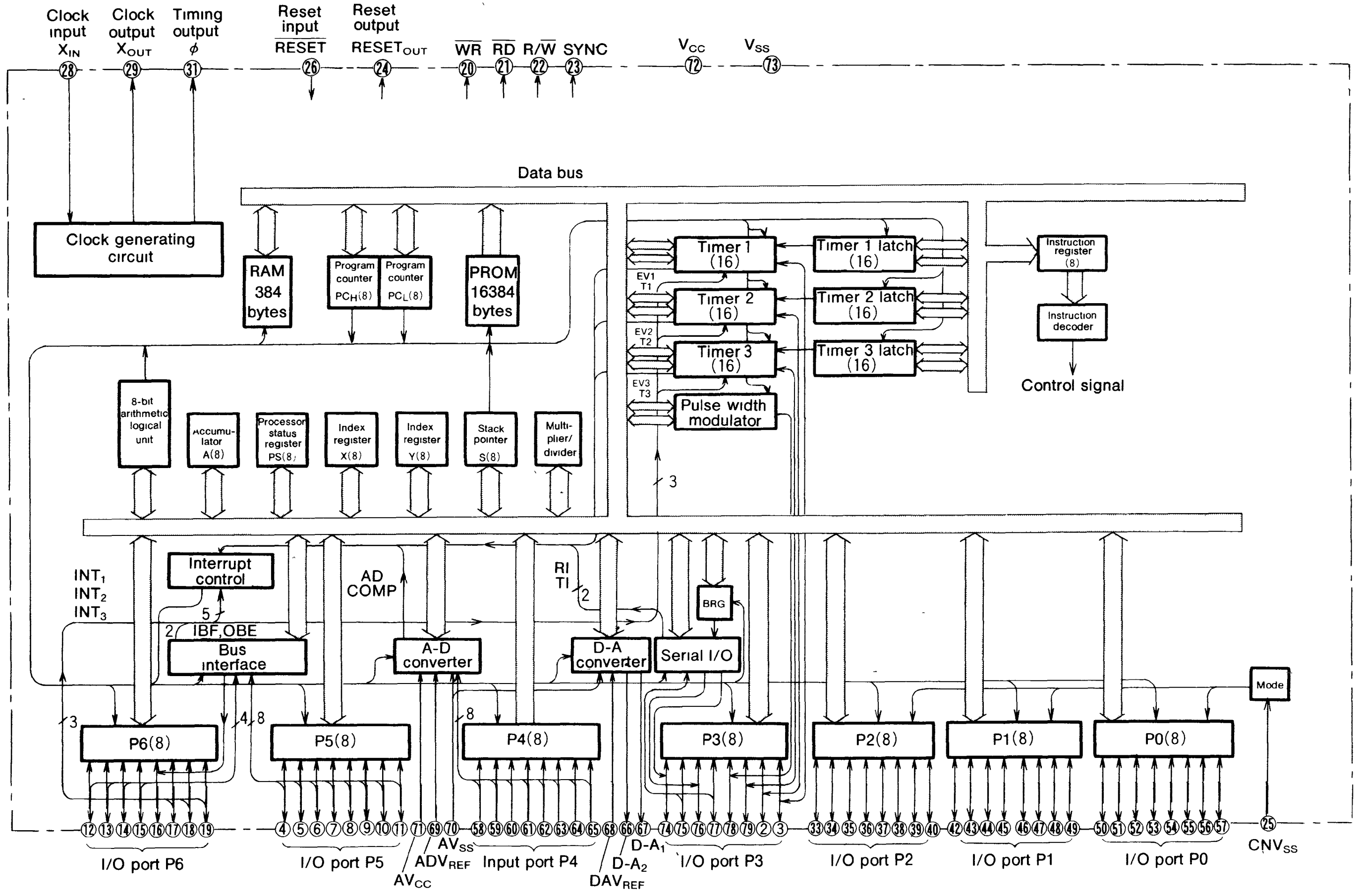
Outline 80P6 (OTP)
80D0 (Window)

NC : No connection

M37450E8-XXXSP, M37450E8SS BLOCK DIAGRAM



M37450E8-XXXFP, M37450E8FS BLOCK DIAGRAM



MITSUBISHI ELECTRIC

FUNCTIONS OF M37450E8-XXXSP/FP, M37450E8SS/FS

Parameter			Functions
Number of basic instructions			71 (69 MELPS 740 basic instructions+2)
Instruction execution time			0.8μs (minimum instructions, at 10MHz frequency)
Clock frequency			10MHz (max)
Memory size	PROM		16384 bytes
	RAM		384 bytes
Input/Output port	P0-P3, P5, P6	I/O	8-bit×6
	P4	Input	3-bit×1 (8-bit×1 for 80-pin model)
	D-A	Output	2-bit×1
Serial I/O			UART or clock synchronous
Timers			16-bit timer×3, 8-bit timer (Serial I/O baud rate generator)×1
A-D converter			8-bit×3 channels (8 channels for 80-pin model)
D-A converter			8-bit×2 channels
Pulse width modulator			8-bit or 16-bit×1
Data bus buffer			1-byte input and output each
Subroutine nesting			96-levels
Interrupt			6 external interrupts, 8 internal interrupts One software interrupt
Clock generating circuit			Built-in (ceramic or quarts crystal oscillator)
Supply voltage			5V±5%
Power dissipation			30mW (at 10MHz frequency)
Input/Output characters	Input/Output voltage		5V
	Output current		±5mA (max.)
Memory expansion			Possible
Operating temperature range			−10 to 70℃
Device structure			CMOS silicon gate
Package	M37450E8-XXXSP		64-pin shrink plastic molded DIP
	M37450E8-XXXFP		80-pin plastic molded QFP
	M37450E8SS		64-pin shrink ceramic DIP
	M37450E8FS		80-pin ceramic QFN

PIN DESCRIPTION (normal mode)

Pin	Name	Input/ Output	Functions
V_{CC}, V_{SS}	Supply voltage		Power supply inputs 5V±5% to V_{CC}, and 0V to V_{SS}
CNV_{SS}/V_{PP}	CNV_{SS}		Controls the processor mode of the chip Normally connected to V_{SS} or V_{CC}.
$\overline{RESET}$	Reset input	Input	To enter the reset state, the reset input pin must be kept at a "L" for more than 8 clock cycles (under normal V_{CC} conditions) If more time is needed for the crystal oscillator to stabilize, this "L" condition should be maintained for the required time
X_{IN}	Clock input	Input	This chip has an internal clock generating circuit To control generating frequency, an external ceramic or a quartz crystal oscillator is connected between the X_{IN} and X_{OUT} pins If an external clock is used, the clock source should be connected to the X_{IN} pin and the X_{OUT} pin should be left open.
X_{OUT}	Clock output	Output	
ϕ	Timing output	Output	Outputs signal consisting of oscillating frequency divided by four
SYNC	Synchronous signal output	Output	This signal is output "H" during operation code fetch and is used to control single stepping of programs.
$R/\overline{W}$	Read/Write status output	Output	This signal determines the direction of the data bus It is "H" during read and "L" during write
$P0_0$-$P0_7$	I/O port P0	I/O	Port P0 is an 8-bit I/O port with directional registers allowing each I/O bit to be individually programmed as input or output. The output structure is CMOS output. The low-order bits of the address are output except in single-chip mode.
$P1_0$-$P1_7$	I/O port P1	I/O	Port P1 is an 8-bit I/O port and has basically the same functions as port P0 The high-order bits of the address are output except in single-chip mode
$P2_0$-$P2_7$	I/O port P2	I/O	Port P2 is an 8-bit I/O port and has basically the same functions as port P0 Used as data bus except in single-chip mode.
$P3_0$-$P3_7$	I/O port P3	I/O	Port P3 is an 8-bit I/O port and has basically the same functions as port P0 Serial I/O, PWM output, or event I/O function can be selected with a program.
$P4_0$-$P4_2$ ($P4_0$-$P4_7$)	Input port P4	Input	Analog input pin for the A-D converter The 64-pin model has three pins and the 80-pin model has eight pins. They may also be used as digital input pins
$P5_0$-$P5_7$	I/O port P5	I/O	Port P5 is an 8-bit I/O port and has basically the same functions as port P0 This port functions as an 8-bit data bus for the master CPU when slave mode is selected with a program.
$P6_0$-$P6_7$	I/O port P6	I/O	Port P6 is an 8-bit I/O port and has basically the same function as port P0 Pins $P6_3$ to $P6_7$ change to a control bus for the master CPU when slave mode is selected with a program Pins $P6_0$ to $P6_2$ may be programmed as external interrupt input pins
D-A_1, D-A_2	D-A output	Output	Analog signal from D-A converter is output
V_{REF}	Reference voltage input	Input	Reference voltage input pin for A-D and D-A converter This pin is for 64-pin model only
ADV_{REF}	A-D reference voltage input	Input	Reference voltage input pin for A-D converter This pin is for 80-pin model only
DAV_{REF}	D-A reference voltage input	Input	Reference voltage input pin for D-A converter This pin is for 80-pin model only
AV_{SS}	Analog power supply		Ground level input pin for A-D and D-A converter Same voltage as V_{SS} is applied.
AV_{CC}	Analog power supply		Power supply input pin for A-D converter. This pin is for 80-pin model only Same voltage as V_{CC} is applied. In the case of the 64-pin model, AV_{CC} is connected to V_{CC} internally.
$\overline{RD}$	Read signal output	Output	Control signal output as active "L" when valid data is read from data bus This pin is for 80-pin model only.
$\overline{WR}$	Write signal output	Output	Control signal output as active "L" when writing data from data bus to external component This pin is for 80-pin model only
$RESET_{OUT}$	Reset output	Output	Control signal output as active "H" during reset It is used as a reset output signal for peripheral components This pin is for 80-pin model only

PIN DESCRIPTION (EPROM mode)

Pin	Name	Input/ Output	Functions
V_{CC}, V_{SS}	Supply voltage		Power supply inputs 5V or 6V to V_{CC}, and 0V to V_{SS}
CNV_{SS}/V_{PP}	V_{PP}	Input	Connect to V_{PP} when programming or verifing
$\overline{RESET}$	Reset input	Input	Connect to V_{SS}.
X_{IN}	Clock input	Input	Connect a ceramic or a quartz crystal oscillator between X_{IN} and X_{OUT} for clock oscillation
X_{OUT}	Clock output	Output	
ϕ	Timing output	Output	For timing output
SYNC	Synchronous signal output	Output	Kept to open ("L" signal is output)
$R/\overline{W}$	Read/Write status output	Output	Kept to open ("H" signal is output).
$P0_0$-$P0_7$	I/O port P0	Input	P0 works as the lower 8-bit address input
$P1_0$-$P1_7$	I/O port P1	Input	$P1_0$ to $P1_5$ works as the higher 6-bit address input. $P1_6$ and $P1_7$ connect to V_{CC} or V_{SS}
$P2_0$-$P2_7$	I/O port P2	I/O	P2 works as an 8-bit data bus.
$P3_0$-$P3_7$	I/O port P3	Input	Connect to V_{SS}.
$P4_0$-$P4_2$ ($P4_0$-$P4_7$)	Input port P4	Input	Connect to V_{SS} (The 80-pin model has eight pins $P4_0$ to $P4_7$).
$P5_0$-$P5_7$	I/O port P5	Input	$P5_0$, $P5_1$ and $P5_2$ work as A_{14}, $\overline{OE}$, and $\overline{CE}$ inputs respectively. Connect $P5_3$ and $P5_4$ to V_{CC} and $P5_5$ to $P5_7$ to V_{SS}.
$P6_0$-$P6_7$	I/O port P6	Input	Connect to V_{SS}
D-A_1, D-A_2	D-A output	Output	Kept to open.
V_{REF}	Reference voltage input	Input	Connect to V_{SS}
ADV_{REF}	A-D reference voltage input	Input	Connect to V_{SS}
DAV_{REF}	D-A reference voltage input	Input	Connect to V_{SS}.
AV_{SS}	Analog power	Input	Connect to V_{SS}.
AV_{CC}	Analog power	Input	Connect to V_{CC} or V_{SS}
$\overline{RD}$	Read signal output	Output	Kept to open ("H" signal is output)
$\overline{WR}$	Write signal output	Output	Kept to open ("H" signal is output)
$RESET_{OUT}$	Reset output	Output	Kept to open ("H" signal is output)

EPROM MODE

The M37450E8-XXXSP/FP, M37450E8SS/FS features an EPROM mode in addition to its normal modes. When the $\overline{\text{RESET}}$ signal level is low ("L") and CNV_{SS}/V_{PP} signal level is high ("H"), the chip automatically enters the EPROM mode. Table 1 list the correspondence between pins and Figure 1 and Figure 2 give the pin connections in the EPROM mode. When in the EPROM mode, ports P0, P1, P2, $P5_0$ to $P5_2$ and CNV_{SS} are used for the PROM (equivalent to the M5L27256). When in this mode, the built-in PROM can be written to or read from using these pins in the same way as with the M5L27256. The oscillator should be connected to the X_{IN} and X_{OUT} pins, or external clock should be connected to the X_{IN} pin.

Table 1. Pin function in EPROM mode

	M37450E8-XXXSP/FP, M37450E8SS/FS	M5L27256
V_{CC}	V_{CC}	V_{CC}
V_{PP}	CNV_{SS}/V_{PP}	V_{PP}
V_{SS}	V_{SS}	V_{SS}
Address input	Ports P0, $P1_0$-$P1_5$, $P5_0$	A_0-A_{14}
Data I/O	Port P2	D_0-D_7
$\overline{\text{CE}}$	$P5_2/DB_2/\overline{\text{CE}}$	$\overline{\text{CE}}$
$\overline{\text{OE}}$	$P5_1/DB_1/\overline{\text{OE}}$	$\overline{\text{OE}}$

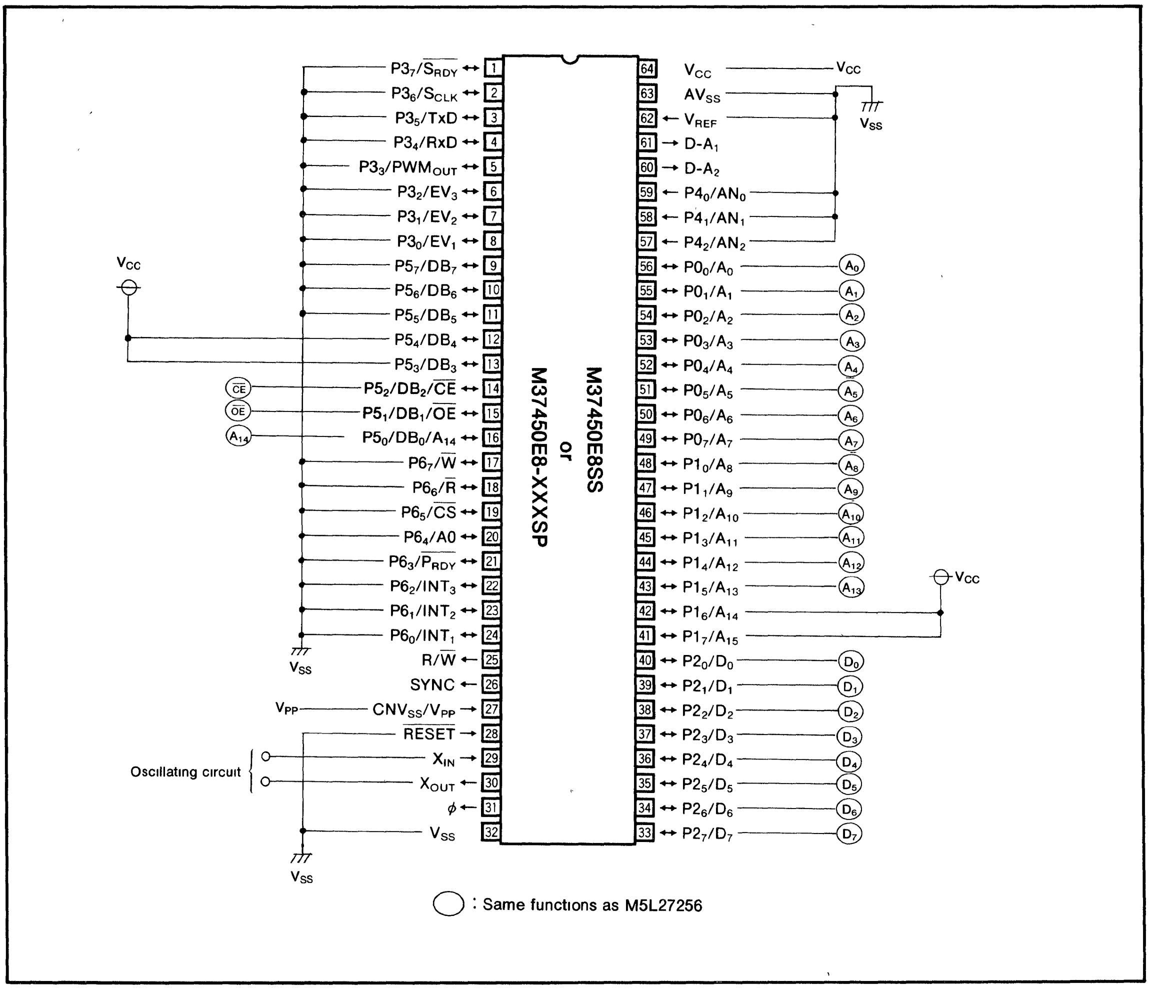
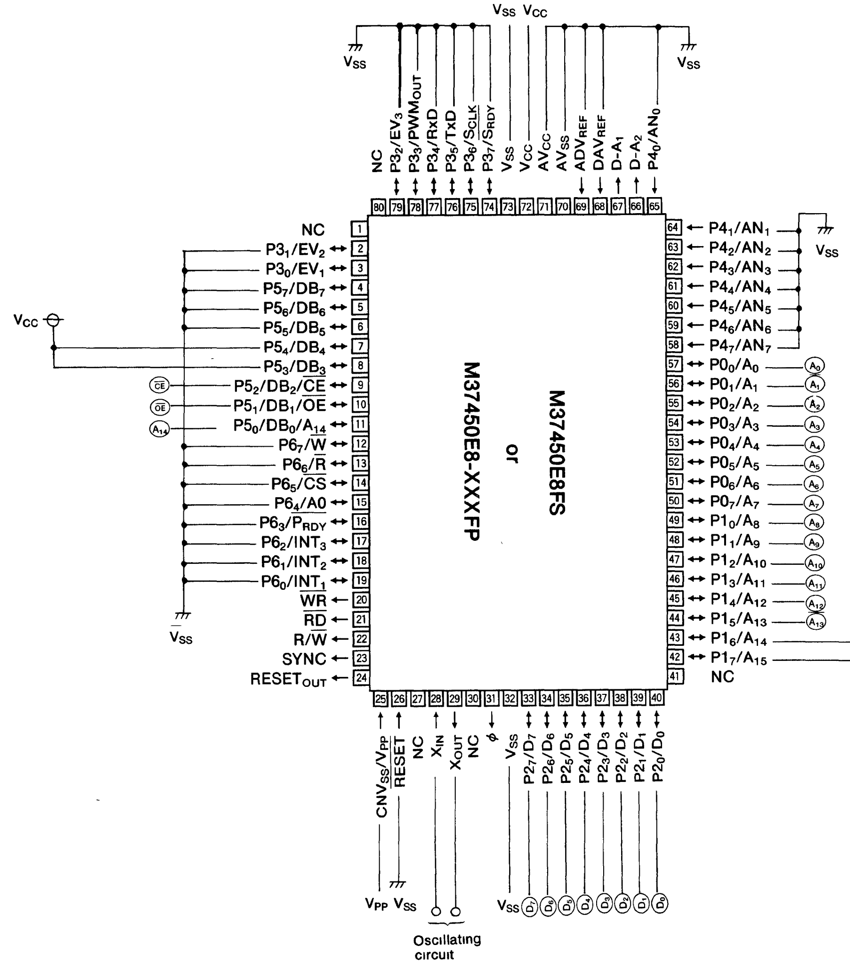


Fig. 1 Pin connection in EPROM mode (64-pin model)



○ : Same functions as M5L27256.

Fig. 2 Pin connection in EPROM mode (80-pin model)

PROM READING, WRITING AND ERASING

Reading

To read the PROM, set the $\overline{CE}$ and $\overline{OE}$ pins to a "L" level, and supply 0V to the $\overline{RESET}$ pin, 5V to the V_{CC} pin and the CNV_{SS} (V_{PP}) pin. Input the address of the data (A_0 to A_{14}) to be read and the data will be output to the I/O pins D_0 to D_7. The data I/O pins will be floating when the $\overline{OE}$ pin is in the "H" state.

Writing

To write to the PROM, set the $\overline{OE}$ pin to a "H" level, and supply 0V to the $\overline{RESET}$ pin, 6V to the V_{CC} pin and 12.5V to the V_{PP} pin. The CPU will enter the program mode when V_{PP} is applied to the V_{PP} pin. The address to be written to is selected with pins A_0 to A_{14}, and the data to be written is input to pins D_0 to D_7. Set the $\overline{CE}$ pin to a "L" level to begin writing.

Erasing

Data can only erased on the M37450E8SS/FS ceramic package, which includes a window. To erase data on this chip, use an ultraviolet light source with a 2537 Angstrom wave length. The minimum radiation power necessary for erasing is 15W•s/cm^2.

NOTES ON HANDLING

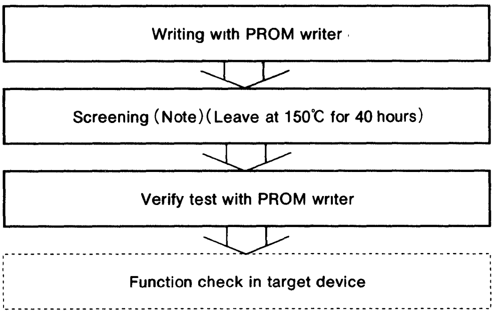
(1) Sunlight and fluorescent light contain wave lengths capable of erasing data. For ceramic package types, cover the transparent window with a seal (provided) when this chip is in use. However, this seal must not contact the lead pins.

(2) Before erasing, the glass should be cleaned and stains such as finger prints should be removed thoroughly. If these stains are not removed, complete erasure of the data could be prevented.

(3) Since a high voltage is used to write data, care should be taken when turning on the PROM writer's power.

(4) For the programmable microcomputer (shipped in blank or OTP type) , Mitsubishi does not perform PROM write test and screening in the assembly process and following process. To improve reliability after write, performing write and test according to the flow below before use is recommended.

(5) In EPROM mode, address A_{15} is set to "H" automatically.



Note : Since the screening temperature is higher than storage temperature, never expose to 150℃ exceeding 100 hours.

Table 2. I/O signal in each mode

Pin Mode	$\overline{CE}$	$\overline{OE}$	V_{PP}	V_{CC}	Port P2
Read-out	V_{IL}	V_{IL}	5V	5V	Output
Output disable	V_{IL}	V_{IH}	5V	5V	Floating
Programming	V_{IL}	V_{IH}	12. 5V	6V	Input
Programming verify	V_{IH}	V_{IL}	12. 5V	6V	Output
Program disable	V_{IH}	V_{IH}	12. 5V	6V	Floating

Note 1 : V_{IL} and V_{IH} indicate a "L" and "H" input voltage, respectively.
2 : An X indicates either V_{IL} or V_{IH}.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS} Output transistors are at "OFF" state	−0.3 to 7	V
V_I	Input voltage $\overline{RESET}$, X_{IN}		−0.3 to 7	V
V_I	Input voltage $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, ADV_{REF}, DAV_{REF}, V_{REF}, AV_{CC}		−0.3 to V_{CC}+0.3	V
V_I	Input voltage CNV_{SS}		−0.3 to 13 (Note 1)	V
V_O	Output voltage $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, X_{OUT}, ϕ, $\overline{RD}$, $\overline{WR}$, $R/\overline{W}$, $RESET_{OUT}$, SYNC		−0.3 to V_{CC}+0.3	V
Pd	Power dissipation	T_a = 25℃	1000 (Note 2)	mW
Topr	Operating temperature		−10 to 70	℃
Tstg	Storage temperature		−40 to 125	℃

Note 1 : In EPROM programming mode, CNV_{SS} is 13.5V.
2 : 500mW for QFP type

RECOMMENDED OPERATING CONDITIONS

(V_{CC}=5V±5%, Ta=−10 to 70℃ unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.75	5	5.25	V
V_{SS}	Supply voltage		0		V
V_{IH}	"H" Input voltage $\overline{RESET}$, X_{IN}, CNV_{SS} (Note 1)	0.8V_{CC}		V_{CC}	V
V_{IH}	"H" Input voltage $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$ (except Note 1)	2.0		V_{CC}	V
V_{IL}	"L" Input voltage CNV_{SS} (Note 1)	0		0.2V_{CC}	V
V_{IL}	"L" Input voltage $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$ (except Note 1)	0		0.8	V
V_{IL}	"L" Input voltage $\overline{RESET}$	0		0.12V_{CC}	V
V_{IL}	"L" Input voltage X_{IN}	0		0.16V_{CC}	V
I_{OL}(peak)	"L" peak output current $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$			10	mA
I_{OL}(avg)	"L" average output current $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$ (Note 2)			5	mA
I_{OH}(peak)	"H" peak output current $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$			−10	mA
I_{OH}(avg)	"H" average output current $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$ (Note 2)			−5	mA
$f(X_{IN})$	Clock oscillating frequency	1		10	MHz

Note 1 : Ports operate as INT_1-INT_3($P6_0$-$P6_2$), EV_1-EV_3($P3_0$-$P3_2$), R_XD($P3_4$) and S_{CLK}($P3_6$)
2 : The average output current I_{OH}(avg) and I_{OL}(avg) are the average value during a 100ms
3 : The total of "L" output current I_{OL}(peak) of port P0, P1 and P2 is less than 40mA
The total of "H" output current I_{OH}(peak) of port P0, P1 and P2 is less than 40mA.
The total of "L" output current I_{OL}(peak) of port P3, P5, P6, $R/\overline{W}$, SYNC, $RESET_{OUT}$, $\overline{RD}$, $\overline{WR}$ and ϕ is less than 40mA
The total of "H" output current I_{OH}(peak) of port P3, P5, P6, $R/\overline{W}$, SYNC, $RESET_{OUT}$, $\overline{RD}$, $\overline{WR}$ and ϕ is less than 40mA

ELECTRICAL CHARACTERISTICS ($V_{CC}=5V\pm5\%$, $V_{SS}=0V$, $T_a=-10$ to 70℃, $f(X_{IN})=10MHz$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{OH}	"H" output voltage $\overline{RD}$, $\overline{WR}$, $R/\overline{W}$, SYNC, $RESET_{OUT}$, ϕ	$I_{OH}=-2mA$	$V_{CC}-1$			V
V_{OH}	"H" output voltage $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$	$I_{OH}=-5mA$	$V_{CC}-1$			V
V_{OL}	"L" output voltage $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $\overline{RD}$, $\overline{WR}$, $R/\overline{W}$, SYNC, $RESET_{OUT}$, ϕ	$I_{OL}=2mA$			0.45	V
V_{OL}	"L" output voltage $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$	$I_{OL}=5mA$			1	V
$V_{T+}-V_{T-}$	Hysterisis INT_1-INT_3($P6_0$-$P6_2$), EV_1-EV_3($P3_0$-$P3_2$), R_XD($P3_4$), S_{CLK}($P3_6$)	Function input level	0.3		1	V
$V_{T+}-V_{T-}$	Hysterisis $\overline{RESET}$				0.7	V
$V_{T+}-V_{T-}$	Hysterisis X_{IN}		0.1		0.5	V
I_{IL}	"L" input current $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $\overline{RESET}$, X_{IN}	$V_I=V_{SS}$	−5		5	μA
I_{IH}	"H" input current $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $\overline{RESET}$, X_{IN}	$V_I=V_{CC}$	−5		5	μA
V_{RAM}	RAM retention voltage	At stop mode	2			V
I_{CC}	Supply current	At system operation $f(X_{IN})=10MHz$		6	10	mA
		At stop mode (Note 1)		1	10	μA

Note 1 : The terminals $\overline{RD}$, $\overline{WR}$, $R/\overline{W}$, SYNC, $RESET_{OUT}$, ϕ, D-A_1 and D-A_2 are all open The other ports, which are in the input mode, are connected to V_{SS} A-D converter is in the A-D completion state. The current through ADV_{REF} and DAV_{REF} is not included(Fig 6)

A-D CONVERTER CHARACTERISTICS

($V_{CC}=AV_{CC}=5V$, $V_{SS}=AV_{SS}=0V$, $T_a=25$℃, $f(X_{IN})=10MHz$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
—	Resolution				8	Bits
—	Absolute accuracy	$V_{CC}=AV_{CC}=ADV_{REF}=5.12V$		±1.5	±3	LSB
t_{CONV}	Conversion time				49	$t_C(\phi)$
V_{IA}	Analog input voltage		AV_{SS}		AV_{CC}	V
V_{ADVREF}	Reference input voltage		2		V_{CC}	V
R_{LADDER}	Ladder resistance value	$ADV_{REF}=5V$	20	35	50	kΩ
$I_{IADVREF}$	Reference input current	$ADV_{REF}=5V$	0.1	0.14	0.25	mA
V_{AVCC}	Analog power supply input voltage			V_{CC}		V
V_{AVSS}	Analog power supply input voltage			0		V

D-A CONVERTER CHARACTERISTICS ($V_{CC}=5V$, $V_{SS}=AV_{SS}=0V$, $T_a=25$℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
—	Resolution				8	Bits
—	Absolute accuracy	$V_{CC}=DAV_{REF}=5.12V$			1.0	%
t_{SU}	Setup time				3	μs
R_O	Output resistance		1	2	4	kΩ
V_{AVSS}	Analog power supply input voltage			0		V
V_{DAVREF}	Reference input voltage		4		V_{CC}	V
I_{DAVREF}	Reference power input current (Each pin)		0	2.5	5	mA

TIMING REQUIREMENTS

Port/single-chip mode (V_{CC}=5V±5%, V_{SS}=0V, T_a=−10 to 70℃, unless otherwise noted)

Symbol	Parameter	Test condition	Limits			Unit
			Min.	Typ	Max	
$t_{su(P0D-\phi)}$	Port P0 input setup time	Fig 3	200			ns
$t_{su(P1D-\phi)}$	Port P1 input setup time		200			ns
$t_{su(P2D-\phi)}$	Port P2 input setup time		200			ns
$t_{su(P3D-\phi)}$	Port P3 input setup time		200			ns
$t_{su(P4D-\phi)}$	Port P4 input setup time		200			ns
$t_{su(P5D-\phi)}$	Port P5 input setup time		200			ns
$t_{su(P6D-\phi)}$	Port P6 input setup time		200			ns
$t_{h(\phi-P0D)}$	Port P0 input hold time		40			ns
$t_{h(\phi-P1D)}$	Port P1 input hold time		40			ns
$t_{h(\phi-P2D)}$	Port P2 input hold time		40			ns
$t_{h(\phi-P3D)}$	Port P3 input hold time		40			ns
$t_{h(\phi-P4D)}$	Port P4 input hold time		40			ns
$t_{h(\phi-P5D)}$	Port P5 input hold time		40			ns
$t_{h(\phi-P6D)}$	Port P6 input hold time		40			ns
$t_c(X_{IN})$	External clock input cycle time		100		1000	ns
$t_w(X_{IN}L)$	External clock input "L" pulse width		30			ns
$t_w(X_{IN}H)$	External clock input "H" pulse width		30			ns
$t_r(X_{IN})$	External clock rising edge time				20	ns
$t_f(X_{IN})$	External clock falling edge time				20	ns

Master CPU bus interface timing ($\overline{R}$ and $\overline{W}$ separation type mode)

(V_{CC}=5V±5%, V_{SS}=0V, T_a=−10 to 70℃, unless otherwise noted)

Symbol	Parameter	Test condition	Limits			Unit
			Min.	Typ	Max	
$t_{su(CS-R)}$	$\overline{CS}$ setup time	Fig 3	0			ns
$t_{su(CS-W)}$	$\overline{CS}$ setup time		0			ns
$t_{h(R-CS)}$	$\overline{CS}$ hold time		0			ns
$t_{h(W-CS)}$	$\overline{CS}$ hold time		0			ns
$t_{su(A-R)}$	A0 setup time		40			ns
$t_{su(A-W)}$	A0 setup time		40			ns
$t_{h(R-A)}$	A0 hold time		10			ns
$t_{h(W-A)}$	A0 hold time		10			ns
$t_{w(R)}$	Read pulse width		160			ns
$t_{w(W)}$	Write pulse width		160			ns
$t_{su(D-W)}$	Date input setup time before write		100			ns
$t_{h(W-D)}$	Date input hold time after write		10			ns

Master CPU bus interface timing (R/$\overline{W}$ type mode)

(V_{CC}=5V±5%, V_{SS}=0V, T_a=−10 to 70℃, unless otherwise noted)

Symbol	Parameter	Test condition	Limits			Unit
			Min	Typ	Max	
$t_{su(CS-E)}$	$\overline{CS}$ setup time	Fig. 4	0			ns
$t_{h(E-CS)}$	$\overline{CS}$ hold time		0			ns
$t_{su(A-E)}$	A0 setup time		40			ns
$t_{h(E-A)}$	A0 hold time		10			ns
$t_{su(RW-E)}$	R/$\overline{W}$ setup time		40			ns
$t_{h(E-RW)}$	R/$\overline{W}$ hold time		10			ns
$t_{w(EL)}$	Enable clock "L" pulse width		160			ns
$t_{w(EH)}$	Enable clock "H" pulse width		160			ns
$t_{r(E)}$	Enable clock rising edge time				25	ns
$t_{f(E)}$	Enable clock falling edge time				25	ns
$t_{su(D-E)}$	Data input setup time before write		100			ns
$t_{h(E-D)}$	Data input hold time after write		10			ns

Local bus/memory expansion mode, microprocessor mode

(V_{CC}=5V±5%, V_{SS}=0V, T_a=−10 to 70℃, unless otherwise noted)

Symbol	Parameter	Test condition	Limits			Unit
			Min.	Typ.	Max.	
$t_{su(D-\phi)}$	Data input setup time	Fig. 5	130			ns
$t_{h(\phi-D)}$	Data input hold time		0			ns
$t_{su(D-RD)}$	Data input setup time		130			ns
$t_{h(RD-D)}$	Data input hold time		0			ns

SWITCHING CHARACTERISTICS

Port/single-chip mode (V_{CC}=5V±5%, V_{SS}=0V, T_a=−10 to 70℃, unless otherwise noted)

Symbol	Parameter	Test condition	Limits			Unit
			Min	Typ.	Max.	
$t_{d(\phi-P0Q)}$	Port P0 data output delay time	Fig 3			200	ns
$t_{d(\phi-P1Q)}$	Port P1 data output delay time				200	ns
$t_{d(\phi-P2Q)}$	Port P2 data output delay time				200	ns
$t_{d(\phi-P3Q)}$	Port P3 data output delay time				200	ns
$t_{d(\phi-P5Q)}$	Port P5 data output delay time				200	ns
$t_{d(\phi-P6Q)}$	Port P6 data output delay time				200	ns
$t_{c(\phi)}$	Cycle time		400		4000	ns
$t_{w(\phi H)}$	ϕ clock pulse width ("H" level)		190			ns
$t_{w(\phi L)}$	ϕ clock pulse width ("L" level)		170			ns
$t_{r(\phi)}$	ϕ clock rising edge time				20	ns
$t_{f(\phi)}$	ϕ clock falling edge time				20	ns

Master CPU bus interface ($\overline{R}$ and $\overline{W}$ separation type mode)

(V_{CC}=5V±5%, V_{SS}=0V, T_a=−10 to 70℃, unless otherwise noted)

Symbol	Parameter	Test condition	Limits			Unit
			Min	Typ	Max	
$t_{a(R-D)}$	Data output enable time after read	Fig 4			120	ns
$t_{v(R-D)}$	Data output disable time after read		10		85	ns
$t_{PLH(R-PR)}$	$\overline{P_{RDY}}$ output transmission time after read				150	ns
$t_{PLH(W-PR)}$	$\overline{P_{RDY}}$ output transmission time after write				150	ns

Master CPU bus interface (R/$\overline{W}$ type mode) (V_{CC}=5V±5%, V_{SS}=0V, T_a=−10 to 70℃, unless otherwise noted)

Symbol	Parameter	Test condition	Limits			Unit
			Min.	Typ.	Max.	
$t_{a(E-D)}$	Data output enable time after read	Fig 4			120	ns
$t_{v(E-D)}$	Data output disable time after read		10		85	ns
$t_{PLH(E-PR)}$	$\overline{P_{RDY}}$ output transmission time after E clock				150	ns

Local bus/memory expansion mode, microprocessor mode

(V_{CC}=5V±5%, V_{SS}=0V, T_a=−10 to 70℃, unless otherwise noted)

Symbol	Parameter	Test condition	Limits			Unit
			Min	Typ	Max	
$t_{d(\phi-A)}$	address delay time after ϕ	Fig 5			150	ns
$t_{v(\phi-A)}$	address effective time after ϕ		10			ns
$t_{v(RD-A)}$	address effective time after $\overline{RD}$		10			ns
$t_{v(WR-A)}$	address effective time after $\overline{WR}$		10			ns
$t_{d(\phi-D)}$	data output delay time after ϕ				160	ns
$t_{d(WR-D)}$	data output delay time after $\overline{WR}$				160	ns
$t_{v(\phi-D)}$	data output effective time after ϕ		20			ns
$t_{v(WR-D)}$	data output effective time after $\overline{WR}$		20			ns
$t_{d(\phi-RW)}$	R/$\overline{W}$ delay time after ϕ				150	ns
$t_{d(\phi-SYNC)}$	SYNC delay time after ϕ				150	ns
$t_{w(RD)}$	$\overline{RD}$ pulse width		170			ns
$t_{w(WR)}$	$\overline{WR}$ pulse width		170			ns

TEST CONDITION

Input voltage level : V_{IH} 2.4V

V_{IL} 0.45V

Output test level : V_{OH} 2.0V

V_{OL} 0.8V

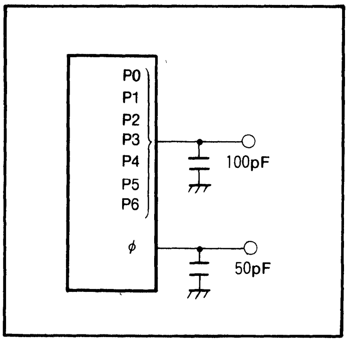


Fig. 3 Test circuit in single-chip mode

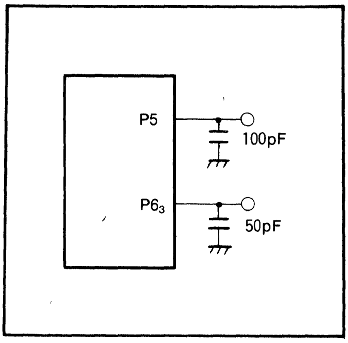


Fig. 4 Master CPU bus interface test circuit

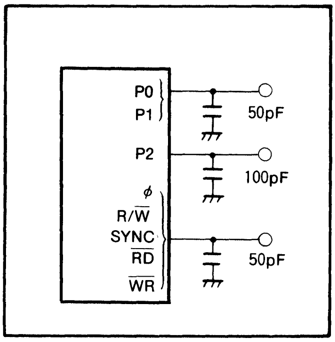


Fig. 5 Local bus test circuit

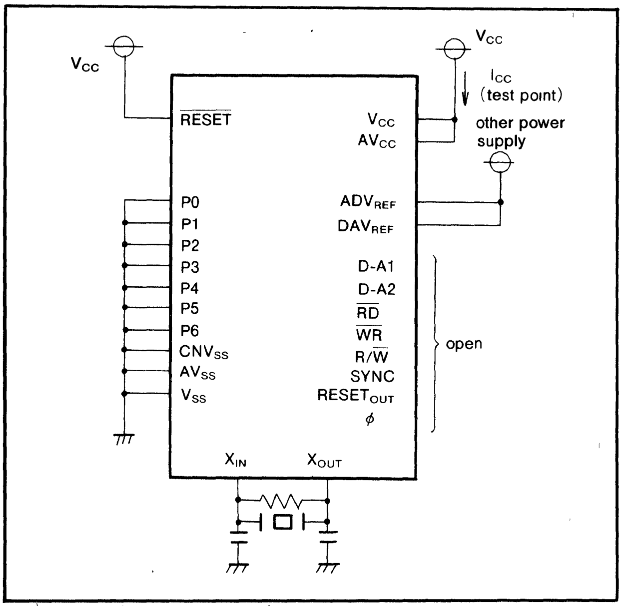
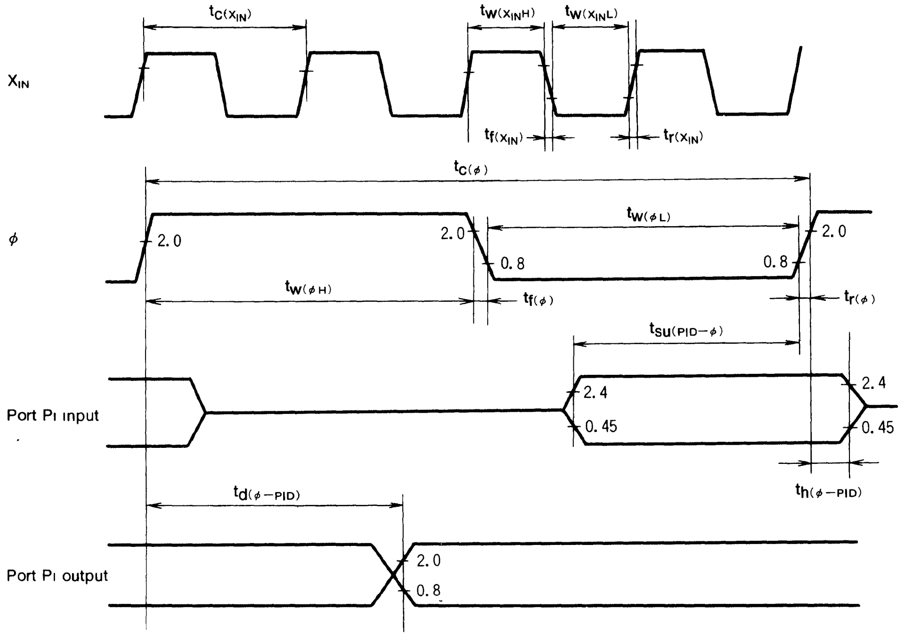


Fig. 6 I_{CC} (at STOP mode) test condition

TIMING DIAGRAM

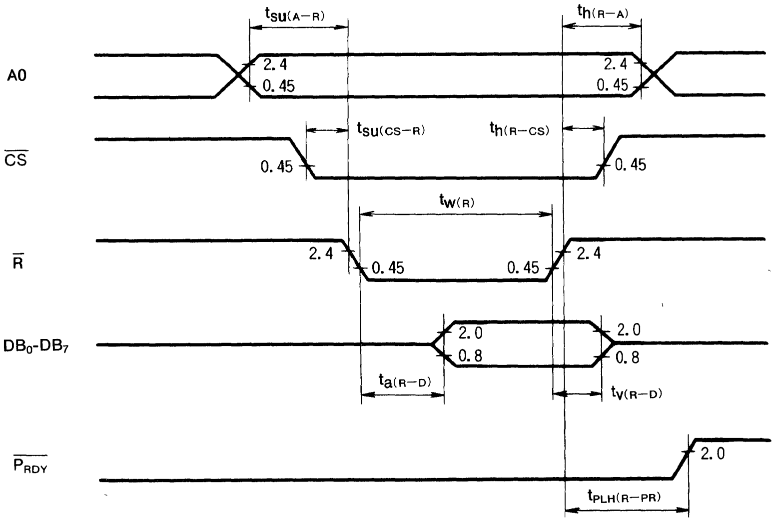
Port/single-chip mode timing diagram



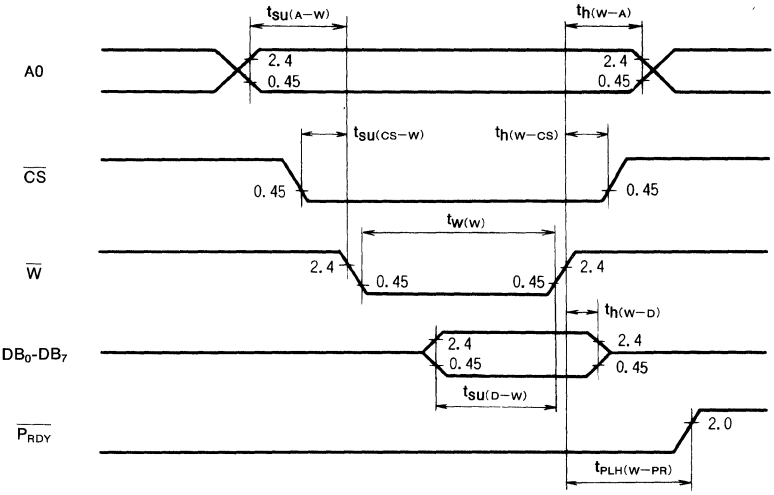
Note : $V_{IH}=0.8V_{CC}$, $V_{IL}=0.16V_{CC}$ of X_{IN}

Master CPU bus interface/ $\overline{R}$ and $\overline{W}$ separation type timing diagram

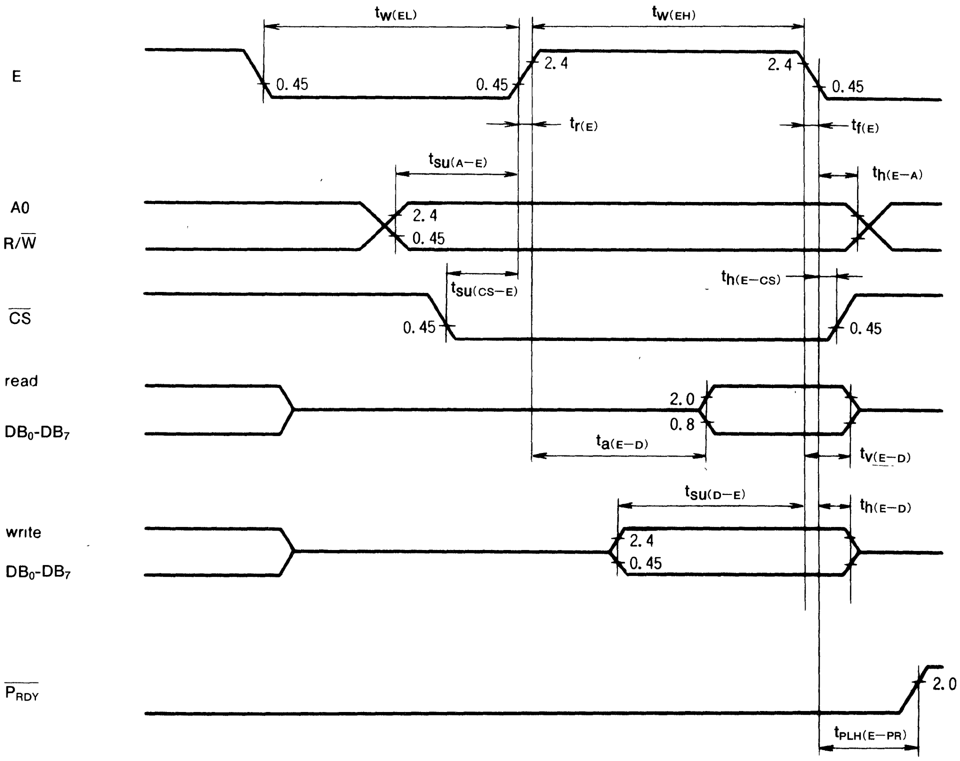
Read



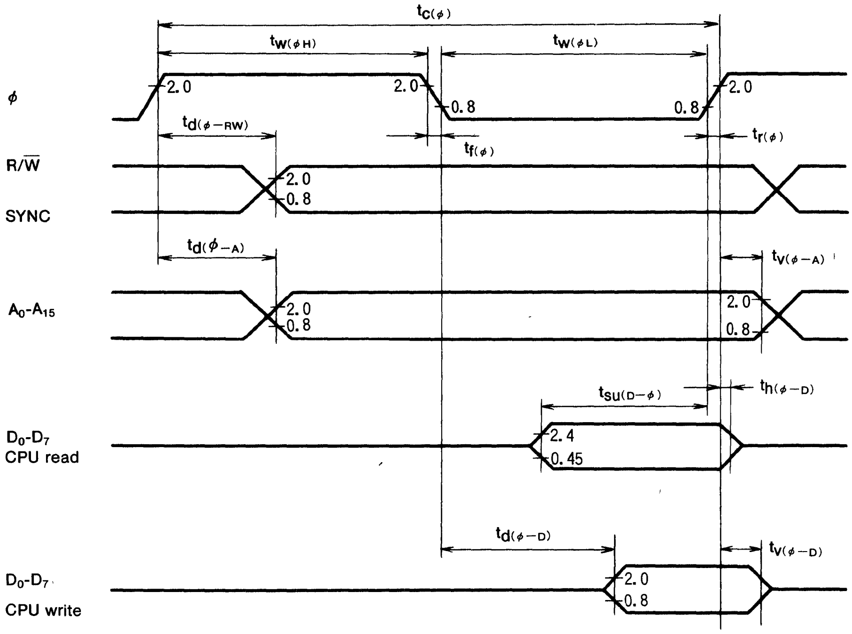
Write

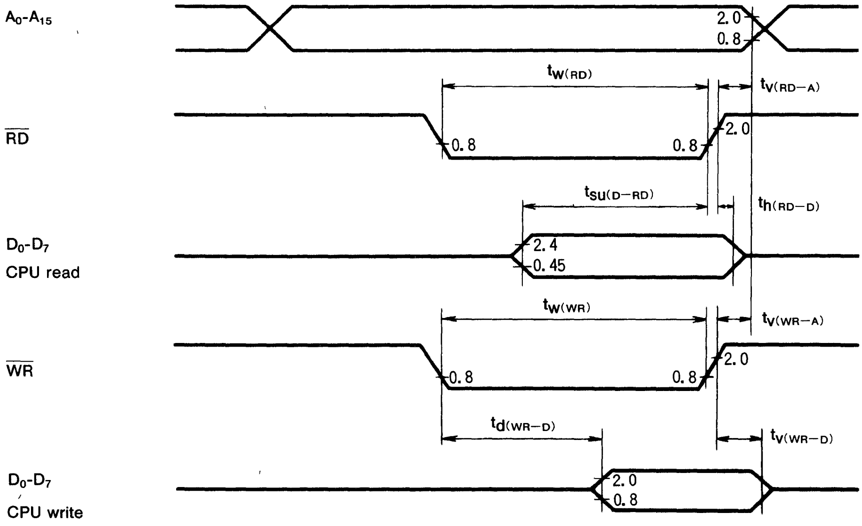


Master CPU interface/ R/W type timing diagram



Local bus timing diagram





MITSUBISHI MICROCOMPUTERS

M37450E4TXXXSP/J

PROM VERSION of M37450M4TXXXSP/J

DESCRIPTION

The M37450E4TXXXSP/J is a single-chip microcomputer designed with CMOS silicon gate technology. It is housed in a 64-pin shrink plastic molded DIP or 84-pin plastic molded QFJ (PLCC). The features of this chip are similar to those of the M37450M4-XXXSP except that this chip has a 8192 bytes PROM built-in. This single-chip microcomputer is useful for office automation appliances and consumer appliance controllers.

In addition to its simple instruction sets, the PROM, RAM and I/O addresses are placed on the same memory map to enable easy programming. It also has a unique feature that enables it to be used as a slave microcomputer.

The difference between the M37450E4TXXXSP and the M37450E4TXXXJ is the package outline.

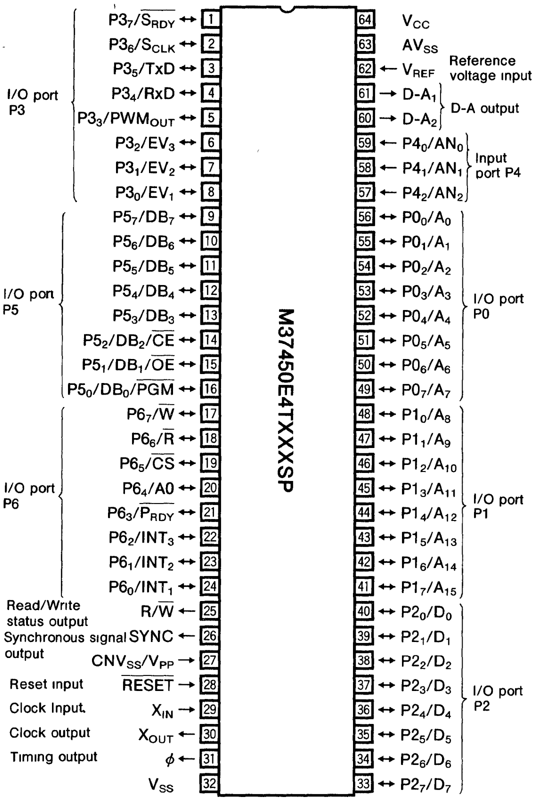
FEATURES

- Number of basic instructions………………………… 71
  69 MELPS 740 basic instructions + 2 multiply/divide instructions
- Memory size PROM ………………………… 8192 bytes
  RAM ………………………… 256 bytes
- Instruction execution time
  (minimum instructions at 10 MHz frequency) …… 0.8μs
- Single power supply ………………………… 5V±5%
- Power dissipation normal operation mode
  (at 10 MHz frequency) ………………………… 30mW
- Subroutine nesting ………………………… 96 levels max.
- Interrupt ………………………… 15 events
- Master CPU bus interface ………………………… 1 byte
- 16-bit timer ………………………… 3
- 8-bit timer (Serial I/O use) ………………………… 1
- Serial I/O (UART or clock synchronous) ………………………… 1
- A-D converter (8-bit resolution) ……… 3 channels (DIP)
  8 channels (QFJ)
- D-A converter (8-bit resolution) ………………………… 2 channels
- PWM output (8-bit or 16-bit) ………………………… 1
- Programmable I/O ports
  (Ports P0, P1, P2, P3, P5, P6) ………………………… 48
- Input port (Port P4) ………………………… 3 (DIP), 8 (QFJ)
- Output ports (Ports D-A_1, D-A_2) ………………………… 2
- PROM (equivalent to the M5L2764)
  program voltage ………………………… 21V

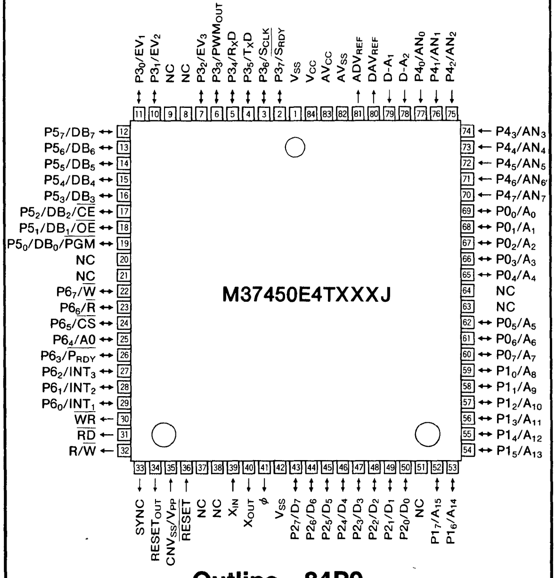
APPLICATION

Slave controller for PPCs, facsimiles, and page printers
HDD, optical disk, inverter, and industrial motor controllers
Industrial robots and machines

PIN CONFIGURATION (TOP VIEW)



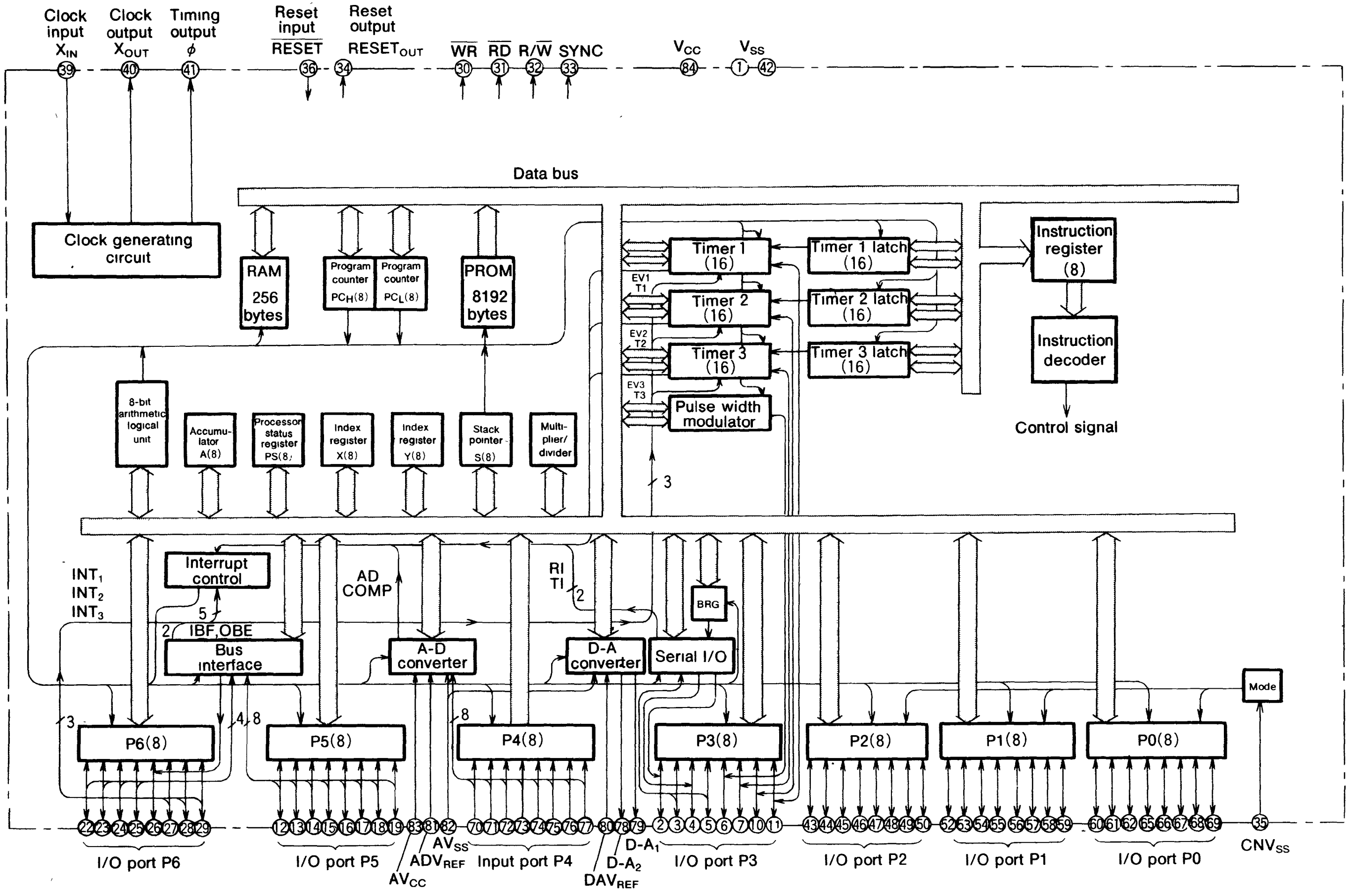
Outline 64P4B



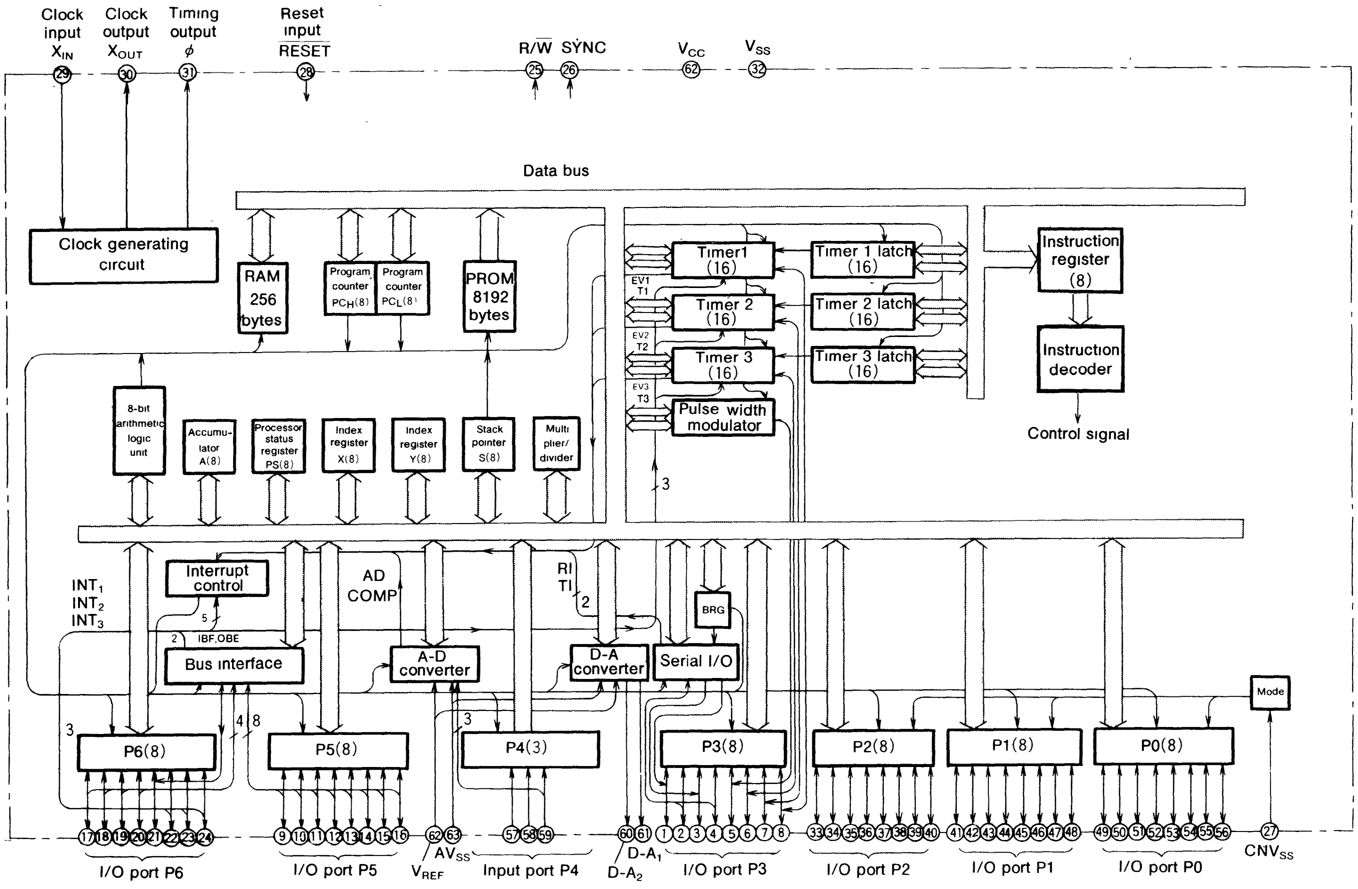
Outline 84P0

NC : No connection

M37450E4TXXXJ BLOCK DIAGRAM



M37450E4TXXXSP BLOCK DIAGRAM



FUNCTIONS OF M37450E4TXXXSP/J

Parameter			Functions
Number of basic instructions			71(69 MELPS 740 basic instructions+2)
Instruction execution time			0.8μs (minimum instructions, at 10MHz frequency)
Clock frequency			10MHz (max.)
Memory size	PROM		8192 bytes
	RAM		256 bytes
Input/Output port	P0-P3, P5, P6	I/O	8-bit×6
	P4	Input	3-bit×1 (8-bit×1 for 84-pin model)
	D-A	Output	2-bit×1
Serial I/O			UART or clock synchronous
Timers			16-bit timer×3, 8-bit timer (Serial I/O baud rate generator)×1
A-D converter			8-bit×3 channels (8 channels for 84-pin model)
D-A converter			8-bit×2 channels
Pulse width modulator			8-bit or 16-bit×1
Data bus buffer			1-byte input and output each
Subroutine nesting			96-levels
Interrupt			6 external interrupts, 8 internal interrupts One software interrupt
Clock generating circuit			Built-in (ceramic or quarts crystal oscillator)
Supply voltage			5V±5%
Power dissipation			30mW (at 10MHz frequency)
Input/Output characters	Input/Output voltage		5V
	Output current		±5mA (max.)
Memory expansion			Possible
Operating temperature range			−40 to 85℃
Device structure			CMOS silicon gate
Package	M37450E4TXXXSP		64-pin shrink plastic molded DIP
	M37450E4TXXXJ		84-pin plastic molded QFJ (PLCC)

PIN DESCRIPTION (normal mode)

Pin	Name	Input/ Output	Functions
V_{CC}, V_{SS}	Supply voltage		Power supply inputs 5V±5% to V_{CC}, and 0V to V_{SS}
CNV_{SS}/V_{PP}	CNV_{SS}		Controls the processor mode of the chip. Normally connected to V_{SS} or V_{CC}.
$\overline{RESET}$	Reset input	Input	To enter the reset state, the reset input pin must be kept at a "L" for more than 8 clock cycles (under normal V_{CC} conditions) If more time is needed for the crystal oscillator to stabilize, this "L" condition should be maintained for the required time
X_{IN}	Clock input	Input	This chip has an internal clock generating circuit. To control generating frequency, an external ceramic or a quartz crystal oscillator is connected between the X_{IN} and X_{OUT} pins. If an external clock is used, the clock source should be connected to the X_{IN} pin and the X_{OUT} pin should be left open.
X_{OUT}	Clock output	Output	
ϕ	Timing output	Output	Outputs signal consisting of oscillating frequency divided by four
SYNC	Synchronous signal output	Output	This signal is output "H" during operation code fetch and is used to control single stepping of programs.
$R/\overline{W}$	Read/Write status output	Output	This signal determines the direction of the data bus. It is "H" during read and "L" during write
$P0_0$-$P0_7$	I/O port P0	I/O	Port P0 is an 8-bit I/O port with directional registers allowing each I/O bit to be individually programmed as input or output The output structure is CMOS output. The low-order bits of the address are output except in single-chip mode.
$P1_0$-$P1_7$	I/O port P1	I/O	Port P1 is an 8-bit I/O port and has basically the same functions as port P0 The high-order bits of the address are output except in single-chip mode
$P2_0$-$P2_7$	I/O port P2	I/O	Port P2 is an 8-bit I/O port and has basically the same functions as port P0. Used as data bus except in single-chip mode.
$P3_0$-$P3_7$	I/O port P3	I/O	Port P3 is an 8-bit I/O port and has basically the same functions as port P0 Serial I/O, PWM output, or event I/O function can be selected with a program.
$P4_0$-$P4_2$ ($P4_0$-$P4_7$)	Input port P4	Input	Analog input pin for the A-D converter The 64-pin model has three pins and the 84-pin model has eight pins. They may also be used as digital input pins
$P5_0$-$P5_7$	I/O port P5	I/O	Port P5 is an 8-bit I/O port and has basically the same functions as port P0. This port functions as an 8-bit data bus for the master CPU when slave mode is selected with a program.
$P6_0$-$P6_7$	I/O port P6	I/O	Port P6 is an 8-bit I/O port and has basically the same function as port P0 Pins $P6_3$ to $P6_7$ change to a control bus for the master CPU when slave mode is selected with a program. Pins $P6_0$ to $P6_2$ may be programmed as external interrupt input pins
$D\text{-}A_1$, $D\text{-}A_2$	D-A output	Output	Analog signal from D-A converter is output.
V_{REF}	Reference voltage input	Input	Reference voltage input pin for A-D and D-A converter This pin is for 64-pin model only
ADV_{REF}	A-D reference voltage input	Input	Reference voltage input pin for A-D converter This pin is for 84-pin model only
DAV_{REF}	D-A reference voltage input	Input	Reference voltage input pin for D-A converter This pin is for 84-pin model only.
AV_{SS}	Analog power supply		Ground level input pin for A-D and D-A converter. Same voltage as V_{SS} is applied.
AV_{CC}	Analog power supply		Power supply input pin for A-D converter. This pin is for 84-pin model only. Same voltage as V_{CC} is applied. In the case of the 64-pin model, AV_{CC} is connected to V_{CC} internally
$\overline{RD}$	Read signal output	Output	Control signal output as active "L" when valid data is read from data bus This pin is for 84-pin model only.
$\overline{WR}$	Write signal output	Output	Control signal output as active "L" when writing data from data bus to external component This pin is for 84-pin model only.
$RESET_{OUT}$	Reset output	Output	Control signal output as active "H" during reset It is used as a reset output signal for peripheral components. This pin is for 84-pin model only.

PIN DESCRIPTION (EPROM mode)

Pin	Name	Input/ Output	Functions
V_{CC}, V_{SS}	Supply voltage		Power supply inputs 5V±5% to V_{CC}, and 0V to V_{SS}
CNV_{SS}/V_{PP}	V_{PP}	Input	Connect to V_{PP} when programming or verifing.
$\overline{RESET}$	Reset input	Input	Connect to V_{SS}
X_{IN}	Clock input	Input	Connect a ceramic or a quartz crystal oscillator between X_{IN} and X_{OUT} for clock oscillation
X_{OUT}	Clock output	Output	
ϕ	Timing output	Output	For timing output
SYNC	Synchronous signal output	Output	Kept to open ("L" signal is output)
$R/\overline{W}$	Read/Write status output	Output	Kept to open ("H" signal is output).
$P0_0$-$P0_7$	I/O port P0	Input	P0 works as the lower 8-bit address input
$P1_0$-$P1_7$	I/O port P1	Input	P1 works as the higher 8-bit address input.
$P2_0$-$P2_7$	I/O port P2	I/O	P2 works as an 8-bit data bus
$P3_0$-$P3_7$	I/O port P3	Input	Connect to V_{SS}
$P4_0$-$P4_2$ ($P4_0$-$P4_7$)	Input port P4	Input	Connect to V_{SS} (The 80-pin model has eight pins $P4_0$ to $P4_7$).
$P5_0$-$P5_7$	I/O port P5	Input	$P5_0$, $P5_1$, $P5_2$ works as $\overline{PGM}$, $\overline{OE}$, and $\overline{CE}$ inputs respectively Connect $P5_3$ and $P5_4$ to V_{CC} and $P5_5$ to $P5_7$ to V_{SS}
$P6_0$-$P6_7$	I/O port P6	Input	Connect to V_{SS}.
D-A_1, D-A_2	D-A output	Output	Kept to open
V_{REF}	Reference voltage input	Input	Connect to V_{SS}.
ADV_{REF}	A-D reference voltage input	Input	Connect to V_{SS}
DAV_{REF}	D-A reference voltage input	Input	Connect to V_{SS}.
AV_{SS}	Analog power	Input	Connect to V_{SS}
AV_{CC}	Analog power	Input	Connect to V_{SS}
$\overline{RD}$	Read signal output	Output	Kept to open ("H" signal is output)
$\overline{WR}$	Write signal output	Output	Kept to open ("H" signal is output).
$RESET_{OUT}$	Reset output	Output	Kept to open ("H" signal is output)

EPROM MODE

The M37450E4TXXXSP/J features an EPROM mode in addition to its normal modes. When the $\overline{\text{RESET}}$ signal level is low ("L") and CNV$_{SS}$/V$_{PP}$ signal level is high ("H"), the chip automatically enters the EPROM mode. Table 1 list the correspondence between pins and Figure 1 and Figure 2 give the pin connections in the EPROM mode. When in the EPROM mode, ports P0, P1, P2, P5$_0$ to P5$_2$ and CNV$_{SS}$ are used for the PROM (equivalent to the M5L2764). When in this mode, the built-in PROM can be written to or read from using these pins in the same way as with the M5L2764. The oscillator should be connected to the X$_{IN}$ and X$_{OUT}$ pins, or external clock should be connected to the X$_{IN}$ pin.

Table 1. Pin function in EPROM mode

	M37450E4TXXXSP/J	M5L2764
V_{CC}	V_{CC}	V_{CC}
V_{PP}	CNV$_{SS}$/V$_{PP}$	V_{PP}
V_{SS}	V_{SS}	V_{SS}
Address input	Ports P0, P1$_0$-P1$_4$	A_0-A_{12}
Data I/O	Port P2	D_0-D_7
$\overline{\text{CE}}$	P5$_2$/DB$_2$/$\overline{\text{CE}}$	$\overline{\text{CE}}$
$\overline{\text{OE}}$	P5$_1$/DB$_1$/$\overline{\text{OE}}$	$\overline{\text{OE}}$
$\overline{\text{PGM}}$	P5$_0$/DB$_0$/$\overline{\text{PGM}}$	$\overline{\text{PGM}}$

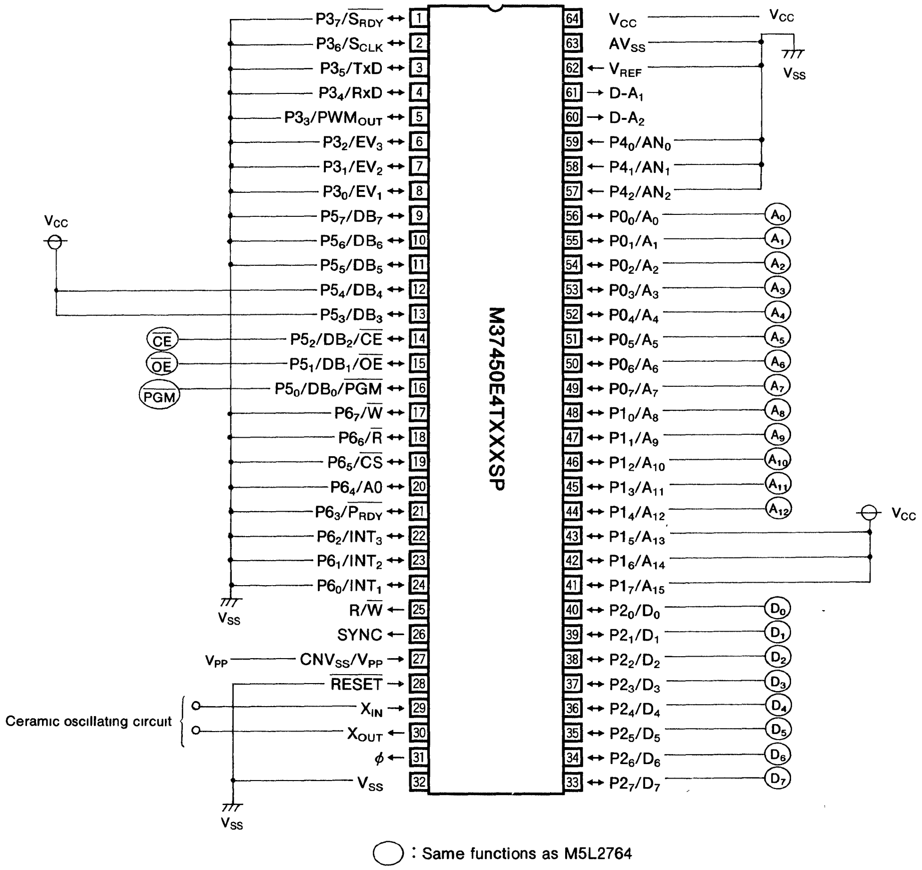


Fig. 1 Pin connection in EPROM mode (64-pin model)

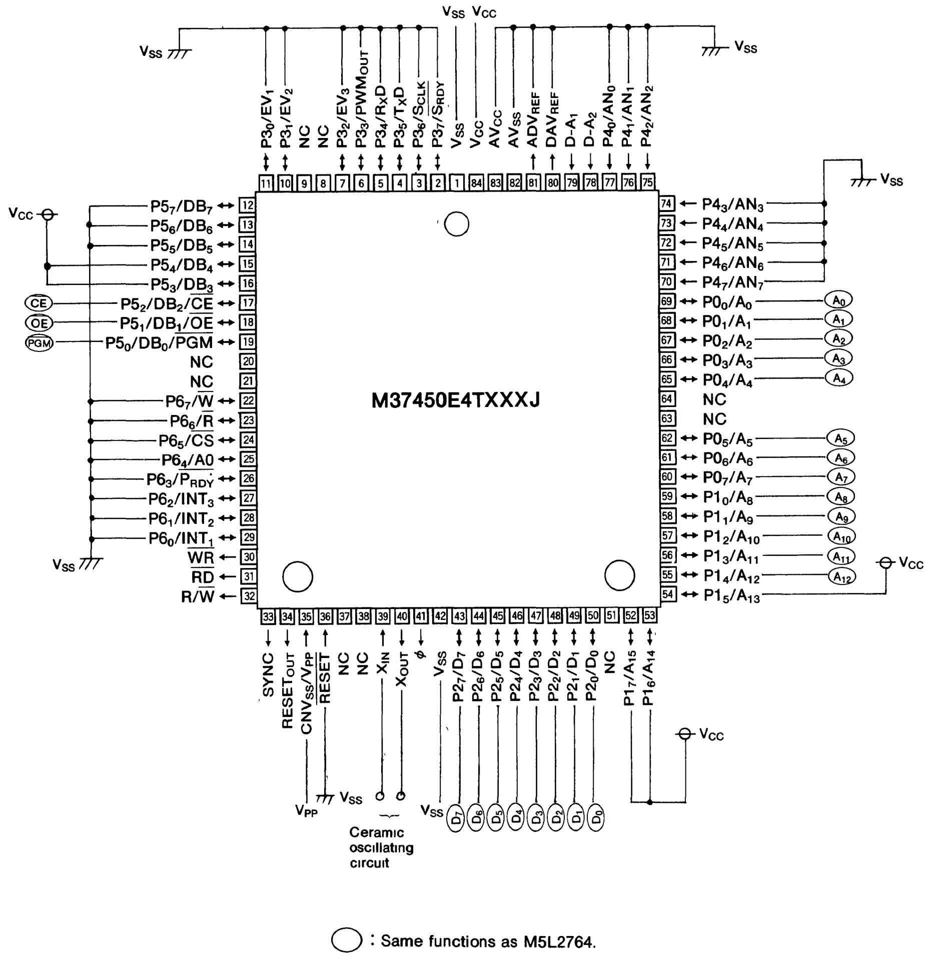


Fig. 2 Pin connection in EPROM mode (84-pin model)

PROM READING AND WRITING

Reading

To read the PROM, set the $\overline{CE}$ and $\overline{OE}$ pins to a "L" level, and the $\overline{PGM}$ pin to a "H" level. Input the address (A_0 to A_{12}) to be read and the data will be output to the I/O pins D_0 to D_7. The data I/O pins will be floating when either the $\overline{CE}$ or $\overline{OE}$ pins are in the "H" state.

Writing

The PROM is programmed at the factory already and do not use the writing mode.

NOTES ON HANDLING

(1) Since a high voltage (21V) is used to write data, care should be taken when turning on the PROM writer's power.

Table 2. I/O signal in each mode

Pin / Mode	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	V_{PP}	V_{CC}	Port P2
Read-out	V_{IL}	V_{IL}	V_{IH}	V_{CC}	V_{CC}	Output
Programming	V_{IL}	V_{IH}	Pulse($V_{IH} \rightarrow V_{IL}$)	V_{PP}	V_{CC}	Input
Programming verify	V_{IL}	V_{IL}	V_{IH}	V_{PP}	V_{CC}	Output
Program disable	V_{IH}	X	X	V_{PP}	V_{CC}	Floating

Note 1 : V_{IL} and V_{IH} indicate a "L" and "H" input voltage, respectively.
2 : An X indicates either V_{IL} or V_{IH}.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS} Output transistors are at "OFF" state.	−0. 3 to 7	V
V_I	Input voltage $\overline{RESET}$, X_{IN}		−0. 3 to 7	V
V_I	Input voltage $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, ADV_{REF}, DAV_{REF}, V_{REF}, AV_{CC}		−0. 3 to V_{CC}+0. 3	V
V_I	Input voltage CNV_{SS}		−0. 3 to 13(Note 1)	V
V_O	Output voltage $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, X_{OUT}, ϕ, $\overline{RD}$, $\overline{WR}$, R/$\overline{W}$, $RESET_{OUT}$, SYNC		−0. 3 to V_{CC}+0. 3	V
P_d	Power dissipation	T_a = 25℃	1000	mW
Topr	Operating temperature		−40 to 85	℃
Tstg	Storage temperature		−65 to 150	℃

Note 1 : In PROM programming mode, CNV_{SS} is 22. 0V.

RECOMMENDED OPERATING CONDITIONS

(V_{CC}=5V±5%, Ta=−40 to 85℃ unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max.	
V_{CC}	Supply voltage	4. 75	5	5. 25	V
V_{SS}	Supply voltage		0		V
V_{IH}	"H" input voltage $\overline{RESET}$, X_{IN}, CNV_{SS} (Note 1)	0. 8V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$ (except Note 1)	2. 0		V_{CC}	V
V_{IL}	"L" input voltage CNV_{SS} (Note 1)	0		0. 2V_{CC}	V
V_{IL}	"L" input voltage $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$ (except Note 1)	0		0. 8	V
V_{IL}	"L" input voltage $\overline{RESET}$	0		0. 12V_{CC}	V
V_{IL}	"L" input voltage X_{IN}	0		0. 16V_{CC}	V
I_{OL}(peak)	"L" peak output current $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$			10	mA
I_{OL}(avg)	"L" average output current $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$ (Note 2)			5	mA
I_{OH}(peak)	"H" peak output current $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$			−10	mA
I_{OH}(avg)	"H" average output current $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$ (Note 2)			−5	mA
f(X_{IN})	Clock oscillating frequency	1		10	MHz

Note 1 : Ports operate as INT_1-INT_3($P6_0$-$P6_2$), EV_1-EV_3($P3_0$-$P3_2$), R_xD($P3_4$) and S_{CLK}($P3_6$)

2 : The average output current I_{OH}(avg) and I_{OL}(avg) are the average value during a 100ms

3 : The total of "L" output current I_{OL}(peak) of port P0, P1 and P2 is less than 40mA.
The total of "H" output current I_{OH}(peak) of port P0, P1 and P2 is less than 40mA.
The total of "L" output current I_{OL}(peak) of port P3, P5, P6, R/$\overline{W}$, SYNC, $RESET_{OUT}$, $\overline{RD}$, $\overline{WR}$ and ϕ is less than 40mA
The total of "H" output current I_{OH}(peak) of port P3, P5, P6, R/$\overline{W}$, SYNC, $RESET_{OUT}$, $\overline{RD}$, $\overline{WR}$ and ϕ is less than 40mA.

ELECTRICAL CHARACTERISTICS ($V_{CC}=5V\pm5\%$, $V_{SS}=0V$, $T_a=-40$ to 85℃, $f(X_{IN})=10MHz$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ.	Max.	
V_{OH}	"H" output voltage $\overline{RD}$, $\overline{WR}$, R/$\overline{W}$, SYNC, $RESET_{OUT}$, ϕ	$I_{OH}=-2mA$	$V_{CC}-1$			V
V_{OH}	"H" output voltage $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$	$I_{OH}=-5mA$	$V_{CC}-1$			V
V_{OL}	"L" output voltage $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $\overline{RD}$, $\overline{WR}$, R/$\overline{W}$, SYNC, $RESET_{OUT}$, ϕ	$I_{OL}=2mA$			0.45	V
V_{OL}	"L" output voltage $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$	$I_{OL}=5mA$			1	V
$V_{T+}-V_{T-}$	Hysterisis INT_1-INT_3($P6_0$-$P6_2$), EV_1-EV_3($P3_0$-$P3_2$), R_XD($P3_4$), S_{CLK}($P3_6$)	Function input level	0.3		1	V
$V_{T+}-V_{T-}$	Hysterisis $\overline{RESET}$				0.7	V
$V_{T+}-V_{T-}$	Hysterisis X_{IN}		0.1		0.5	V
I_{IL}	"L" input current $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $\overline{RESET}$, X_{IN}	$V_I=V_{SS}$	−5		5	μA
I_{IH}	"H" input current $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $\overline{RESET}$, X_{IN}	$V_I=V_{CC}$	−5		5	μA
V_{RAM}	RAM retention voltage	At stop mode	2			V
I_{CC}	Supply current	At system operation $f(X_{IN})=10MHz$		6	15	mA
		At stop mode (Note 1)		1	10	μA

Note 1 : The terminals $\overline{RD}$, $\overline{WR}$, R/$\overline{W}$, SYNC, $RESET_{OUT}$, ϕ, $D\text{-}A_1$ and $D\text{-}A_2$ are all open. The other ports, which are in the input mode, are connected to V_{SS} A-D converter is in the A-D completion state. The current through ADV_{REF} and DAV_{REF} is not included(Fig.6)

A-D CONVERTER CHARACTERISTICS

($V_{CC}=AV_{CC}=5V\pm5\%$, $V_{SS}=AV_{SS}=0V$, $T_a=-40$ to 85℃, $f(X_{IN})=10MHz$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max	
—	Resolution				8	Bits
—	Absolute accuracy	$V_{CC}=AV_{CC}=ADV_{REF}=5V\pm5\%$		±1.5	±3	LSB
t_{CONV}	Conversion time				49	$t_C(\phi)$
V_{IA}	Analog input voltage		AV_{SS}		AV_{CC}	V
V_{ADVREF}	Reference input voltage		2		V_{CC}	V
R_{LADDER}	Ladder resistance value	$ADV_{REF}=5V$	2	7.5	10	kΩ
$I_{IADVREF}$	Reference input current	$ADV_{REF}=5V$	0.5	0.7	2.5	mA
V_{AVCC}	Analog power supply input voltage			V_{CC}		V
V_{AVSS}	Analog power supply input voltage			0		V

D-A CONVERTER CHARACTERISTICS ($V_{CC}=5V\pm5\%$, $V_{SS}=AV_{SS}=0V$, $T_a=-40$ to 85℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max	
—	Resolution				8	Bits
—	Absolute accuracy	$V_{CC}=DAV_{REF}=5.12V$			1.0	%
t_{SU}	Setup time				3	μs
R_O	Output resistance		1	2	4	kΩ
V_{AVSS}	Analog power supply input voltage			0		V
V_{DAVREF}	Reference input voltage		4		V_{CC}	V
I_{DAVREF}	Reference power input current (Each pin)		0	2.5	5	mA

TIMING REQUIREMENTS

Port/single-chip mode (V_{CC}=5V±5%, V_{SS}=0V, T_a=−40 to 85℃, unless otherwise noted)

Symbol	Parameter	Test condition	Limits			Unit
			Min	Typ	Max.	
$t_{su(P0D-\phi)}$	Port P0 input setup time	Fig 3	200			ns
$t_{su(P1D-\phi)}$	Port P1 input setup time		200			ns
$t_{su(P2D-\phi)}$	Port P2 input setup time		200			ns
$t_{su(P3D-\phi)}$	Port P3 input setup time		200			ns
$t_{su(P4D-\phi)}$	Port P4 input setup time		200			ns
$t_{su(P5D-\phi)}$	Port P5 input setup time		200			ns
$t_{su(P6D-\phi)}$	Port P6 input setup time		200			ns
$t_{h(\phi-P0D)}$	Port P0 input hold time		40			ns
$t_{h(\phi-P1D)}$	Port P1 input hold time		40			ns
$t_{h(\phi-P2D)}$	Port P2 input hold time		40			ns
$t_{h(\phi-P3D)}$	Port P3 input hold time		40			ns
$t_{h(\phi-P4D)}$	Port P4 input hold time		40			ns
$t_{h(\phi-P5D)}$	Port P5 input hold time		40			ns
$t_{h(\phi-P6D)}$	Port P6 input hold time		40			ns
$t_c(X_{IN})$	External clock input cycle time		100		1000	ns
$t_w(X_{IN}L)$	External clock input "L" pulse width		30			ns
$t_w(X_{IN}H)$	External clock input "H" pulse width		30			ns
$t_r(X_{IN})$	External clock rising edge time				20	ns
$t_f(X_{IN})$	External clock falling edge time				20	ns

Master CPU bus interface timing ($\overline{R}$ and $\overline{W}$ separation type mode)

(V_{CC}=5V±5%, V_{SS}=0V, T_a=−40 to 85℃, unless otherwise noted)

Symbol	Parameter	Test condition	Limits			Unit
			Min	Typ	Max	
$t_{su(CS-R)}$	$\overline{CS}$ setup time	Fig 3	0			ns
$t_{su(CS-W)}$	$\overline{CS}$ setup time		0			ns
$t_{h(R-CS)}$	$\overline{CS}$ hold time		0			ns
$t_{h(W-CS)}$	$\overline{CS}$ hold time		0			ns
$t_{su(A-R)}$	A0 setup time		40			ns
$t_{su(A-W)}$	A0 setup time		40			ns
$t_{h(R-A)}$	A0 hold time		10			ns
$t_{h(W-A)}$	A0 hold time		10			ns
$t_{w(R)}$	Read pulse width		160			ns
$t_{w(W)}$	Write pulse width		160			ns
$t_{su(D-W)}$	Date input setup time before write		100			ns
$t_{h(W-D)}$	Date input hold time after write		10			ns

Master CPU bus interface timing (R/$\overline{W}$ type mode)

(V_{CC}=5V±5%, V_{SS}=0V, T_a=−40 to 85℃, unless otherwise noted)

Symbol	Parameter	Test condition	Limits			Unit
			Min.	Typ.	Max	
$t_{su(CS-E)}$	$\overline{CS}$ setup time	Fig 4	0			ns
$t_{h(E-CS)}$	$\overline{CS}$ hold time		0			ns
$t_{su(A-E)}$	A0 setup time		40			ns
$t_{h(E-A)}$	A0 hold time		10			ns
$t_{su(RW-E)}$	R/$\overline{W}$ setup time		40			ns
$t_{h(E-RW)}$	R/$\overline{W}$ hold time		10			ns
$t_{w(EL)}$	Enable clock "L" pulse width		160			ns
$t_{w(EH)}$	Enable clock "H" pulse width		160			ns
$t_{r(E)}$	Enable clock rising edge time				25	ns
$t_{f(E)}$	Enable clock falling edge time				25	ns
$t_{su(D-E)}$	Data input setup time before write		100			ns
$t_{h(E-D)}$	Data input hold time after write		10			ns

Local bus/memory expansion mode, microprocessor mode

(V_{CC}=5V±5%, V_{SS}=0V, T_a=−40 to 85℃, unless otherwise noted)

Symbol	Parameter	Test condition	Limits			Unit
			Min.	Typ	Max	
$t_{su(D-\phi)}$	Data input setup time	Fig 5	130			ns
$t_{h(\phi-D)}$	Data input hold time		0			ns
$t_{su(D-RD)}$	Data input setup time		130			ns
$t_{h(RD-D)}$	Data input hold time		0			ns

SWITCHING CHARACTERISTICS

Port/single-chip mode (V_{CC}=5V±5%, V_{SS}=0V, T_a=−40 to 85℃, unless otherwise noted)

Symbol	Parameter	Test condition	Limits			Unit
			Min.	Typ	Max.	
$t_{d(\phi-P0Q)}$	Port P0 data output delay time	Fig 3			200	ns
$t_{d(\phi-P1Q)}$	Port P1 data output delay time				200	ns
$t_{d(\phi-P2Q)}$	Port P2 data output delay time				200	ns
$t_{d(\phi-P3Q)}$	Port P3 data output delay time				200	ns
$t_{d(\phi-P5Q)}$	Port P5 data output delay time				200	ns
$t_{d(\phi-P6Q)}$	Port P6 data output delay time				200	ns
$t_{c(\phi)}$	Cycle time		400		4000	ns
$t_{w(\phi H)}$	ϕ clock pulse width ("H" level)		190			ns
$t_{w(\phi L)}$	ϕ clock pulse width ("L" level)		170			ns
$t_{r(\phi)}$	ϕ clock rising edge time				20	ns
$t_{f(\phi)}$	ϕ clock falling edge time				20	ns

Master CPU bus interface ($\overline{R}$ and $\overline{W}$ separation type mode)

(V_{CC}=5V±5%, V_{SS}=0V, T_a=−40 to 85℃, unless otherwise noted)

Symbol	Parameter	Test condition	Limits			Unit
			Min	Typ	Max	
$t_{a(R-D)}$	Data output enable time after read	Fig 4			120	ns
$t_{v(R-D)}$	Data output disable time after read		10		85	ns
$t_{PLH(R-PR)}$	$\overline{P_{RDY}}$ output transmission time after read				150	ns
$t_{PLH(W-PR)}$	$\overline{P_{RDY}}$ output transmission time after write				150	ns

Master CPU bus interface (R/$\overline{W}$ type mode) (V_{CC}=5V±5%, V_{SS}=0V, T_a=−40 to 85℃, unless otherwise noted)

Symbol	Parameter	Test condition	Limits			Unit
			Min	Typ.	Max.	
$t_{a(E-D)}$	Data output enable time after read	Fig 4			120	ns
$t_{v(E-D)}$	Data output disable time after read		10		85	ns
$t_{PLH(E-PR)}$	$\overline{P_{RDY}}$ output transmission time after E clock				150	ns

Local bus/memory expansion mode, microprocessor mode

(V_{CC}=5V±5%, V_{SS}=0V, T_a=−40 to 85℃, unless otherwise noted)

Symbol	Parameter	Test condition	Limits			Unit
			Min	Typ	Max	
$t_{d(\phi-A)}$	address delay time after ϕ	Fig 5			150	ns
$t_{v(\phi-A)}$	address effective time after ϕ		10			ns
$t_{v(RD-A)}$	address effective time after $\overline{RD}$		10			ns
$t_{v(WR-A)}$	address effective time after $\overline{WR}$		10			ns
$t_{d(\phi-D)}$	data output delay time after ϕ				160	ns
$t_{d(WR-D)}$	data output delay time after $\overline{WR}$				160	ns
$t_{v(\phi-D)}$	data output effective time after ϕ		20			ns
$t_{v(WR-D)}$	data output effective time after $\overline{WR}$		20			ns
$t_{d(\phi-RW)}$	R/$\overline{W}$ delay time after ϕ				150	ns
$t_{d(\phi-SYNC)}$	SYNC delay time after ϕ				150	ns
$t_{w(RD)}$	$\overline{RD}$ pulse width		170			ns
$t_{w(WR)}$	$\overline{WR}$ pulse width		170			ns

TEST CONDITION

Input voltage level : V_{IH} 2.4V

V_{IL} 0.45V

Output test level : V_{OH} 2.0V

V_{OL} 0.8V

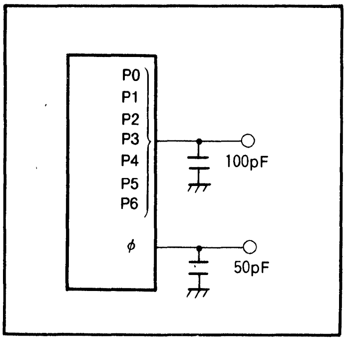


Fig. 3 Test circuit in single-chip mode

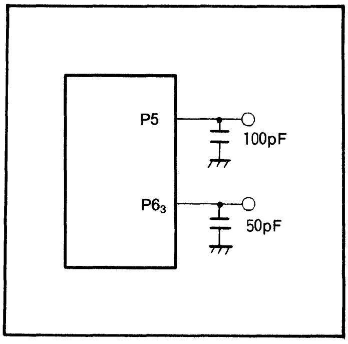


Fig. 4 Master CPU bus interface test circuit

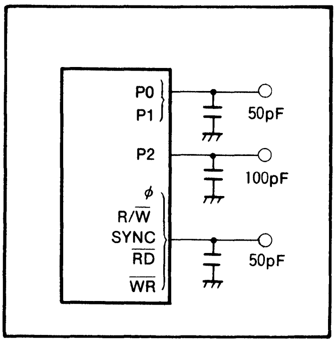


Fig. 5 Local bus test circuit

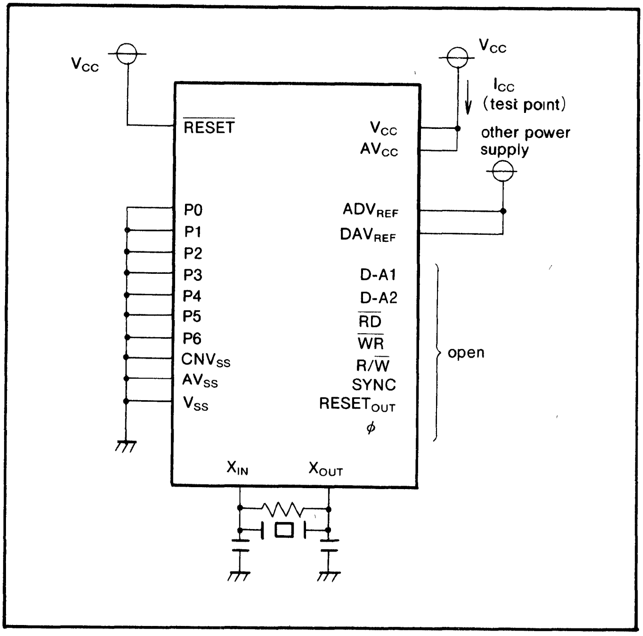


Fig. 6 I_{CC} (at STOP mode) test condition

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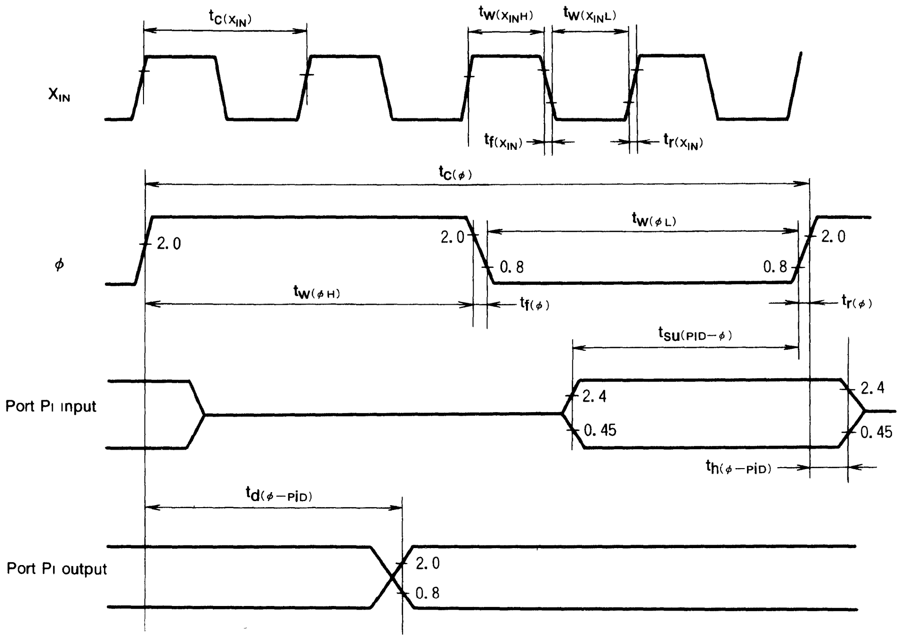
TIMING DIAGRAM

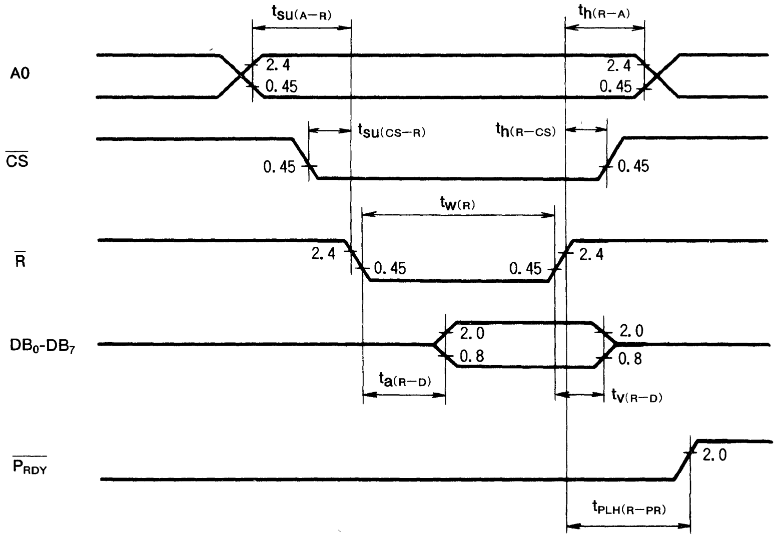
Port/single-chip mode timing diagram



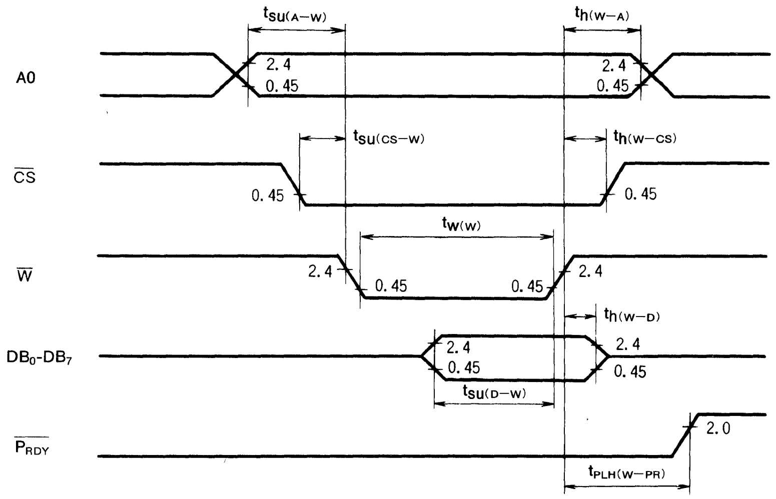
Note : $V_{IH}=0.8V_{CC}$, $V_{IL}=0.16V_{CC}$ of X_{IN}

Master CPU bus interface/ $\overline{R}$ and $\overline{W}$ separation type timing diagram

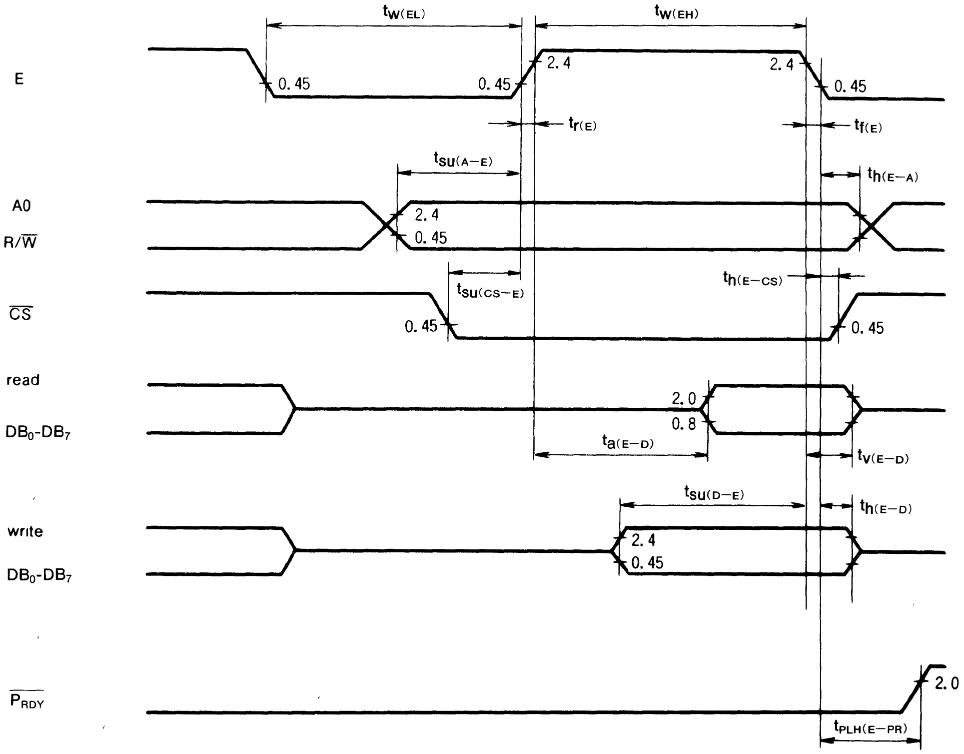
Read



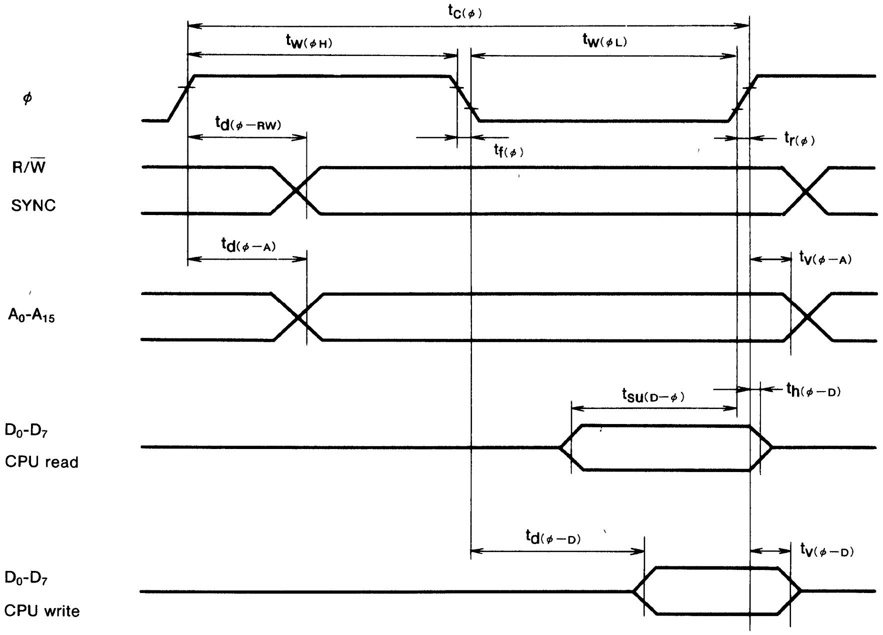
Write

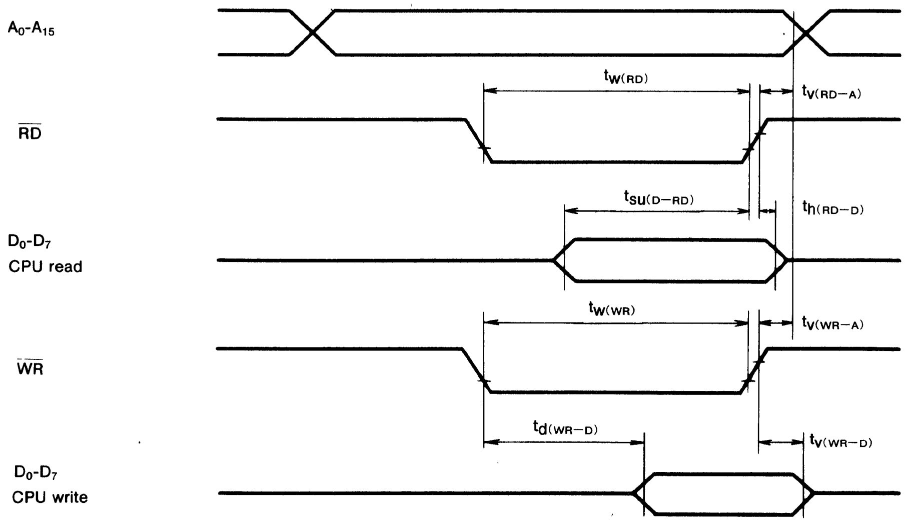


Master CPU interface/ R/W type timing diagram



Local bus timing diagram





PRELIMINARY
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M37451E4-XXXSP/FP/GP,M37451E4SS/FS
M37451E8-XXXSP/FP/GP,M37451E8SS/FS
M37451EC-XXXSP/FP/GP,M37451ECSS/FS
PROM Version of M37451 Group

DESCRIPTION

The M37451E4-XXXSP/FP/GP is a single-chip microcomputer designed with CMOS silicon gate technology. It is housed in a 64-pin shrink plastic molded DIP or a 0.8mm-pitch or 0.65mm-pitch 80-pin plastic molded QFP.

The features of this chip are similar to those of the M37451M4-XXXSP/FP/GP except that this chip has a 8192 bytes PROM built in.

In addition to its simple instruction sets, the PROM, RAM, and I/O addresses are placed on the same memory map to enable easy programming.

It is suited for office automation equipment and control devices. The low power consumption made by the use of a CMOS process makes it especially suitable for battery powered devices requiring low power consumption. It also has a unique feature that enables it to be used as a slave microcomputer.

Since general purpose PROM writers can be used for the built-in PROM, this chip is suitable for small quantity production runs.

The differences among M37451E4-XXXSP/FP/GP, M37451 E8-XXXSP/FP/GP and M37451EC-XXXSP/FP/GP are as shown below. The M37451E4SS/FS, M37451E8SS/FS and M37451ECSS/FS are the window type. The descriptions that follow describe the M37451E4-XXXSP/FP/GP unless otherwise noted.

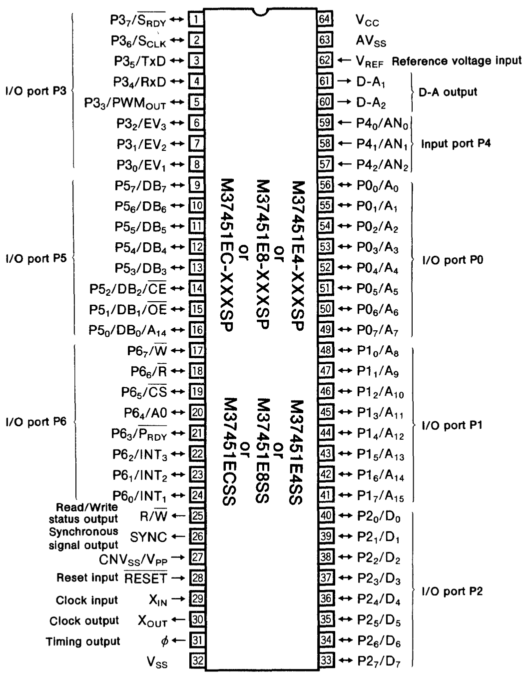
Type name	ROM size	RAM size	Built-in PROM
M37451E4SS/FS	8192 bytes	256 bytes	EPROM (Window type)
M37451E4-XXXSP/FP/GP			One-time programmable
M37451E8SS/FS	16384 bytes	384 bytes	EPROM (Window type)
M37451E8-XXXSP/FP/GP			One-time programmable
M37451ECSS/FS	24576 bytes	512 bytes	EPROM (Window type)
M37451EC-XXXSP/FP/GP			One-time programmable

The number of analog input pins for the 80-pin model (FP, GP version) is different from the 64-pin model (SP version). In addition, the 80-pin model has special pins for $\overline{RD}$, $\overline{WR}$, $RESET_{OUT}$, DAV_{REF}, ADV_{REF}, AV_{CC} and the 64-pin model has a special V_{REF} pin.

FEATURES

- Number of basic instructions ································ 71
  69 MELPS 740 basic instructions+2 multiply/divide instructions
- Instruction execution time
  (minimum instructions at 12.5MHz frequency) ···· 0.64μs
- Single power supply ································ 5V±10%
- Power dissipation normal operation mode
  (at 12.5MHz frequency) ································ 40mW
- Subroutine nesting ············· 96 levels max.(M37451E4)
  96 levels max.(M37451E8)
  128 levels max.(M37451EC)
- Interrupt ·· 15 events

PIN CONFIGURATION (TOP VIEW)



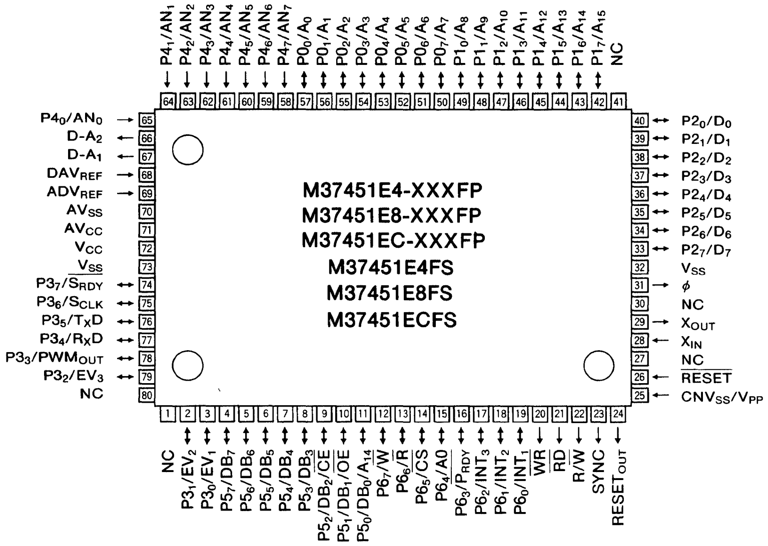
Outline 64P4B (OTP)
64S1B (Window)

- Master CPU bus interface ································ 1 byte
- 16-bit timer ·· 3
- 8-bit timer (Serial I/O use) ································ 1
- Serial I/O (UART or clock synchronous) ················ 1
- A-D converter (8-bit resolution) ········· 3 channels (DIP)
  8 channels (QFP, QFN)
- D-A converter (8-bit resolution) ················· 2 channels
- PWM output with 8-bit prescaler
  (Either resolution 8 bit or 16 bit is software selectable) ··· 1
- Programmable I/O ports
  (Ports P0, P1, P2, P3, P5, P6) ································ 48
- Input port (Port P4) ····················3(DIP), 8(QFP, QFN)
- Output ports (Ports $D\text{-}A_1$, $D\text{-}A_2$) ································ 2
- PROM (equivalent to the M5L27256)
  Program voltage ·· 12.5V

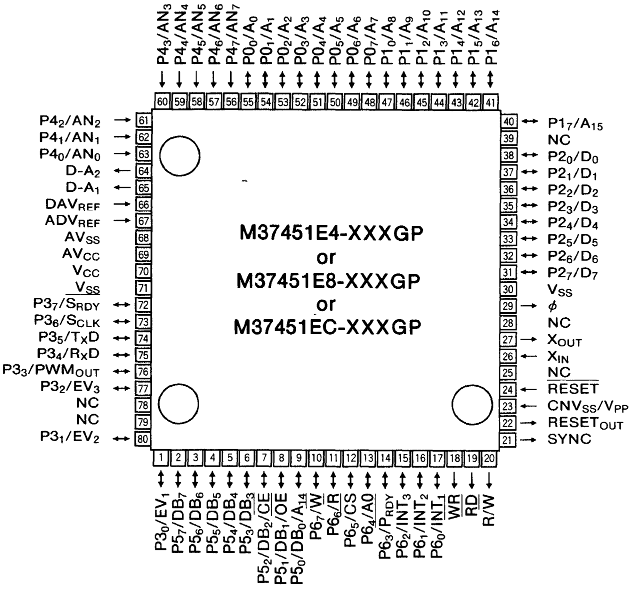
APPLICATION

Slave controller for PPCs, facsimiles, and page printers. HDD, optical disk, inverter, and industrial motor controllers. Industrial robots and machines.

PIN CONFIGURATION (TOP VIEW)



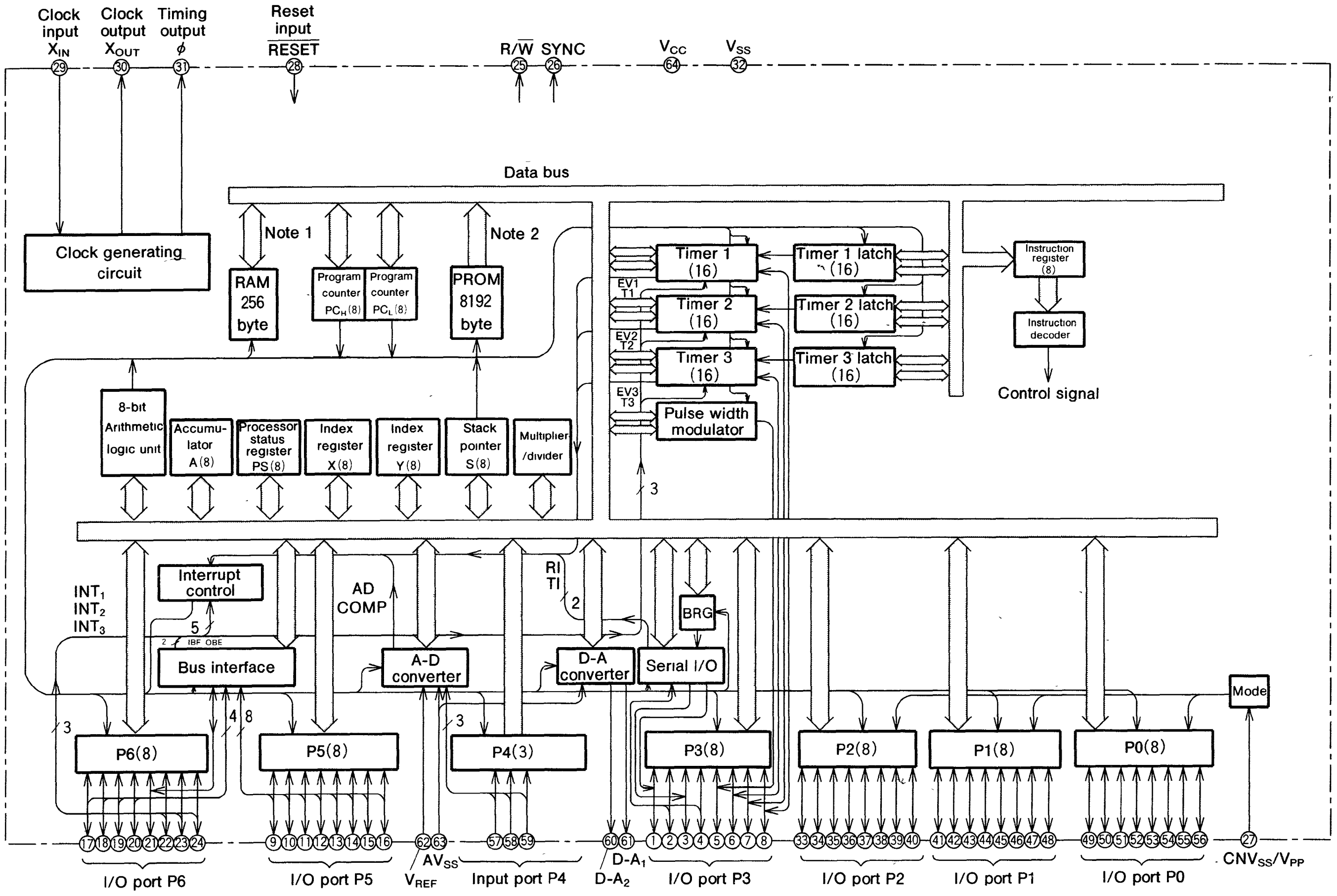
Outline 80P6N (OTP)
80D0 (Window)



Outline 80P6S

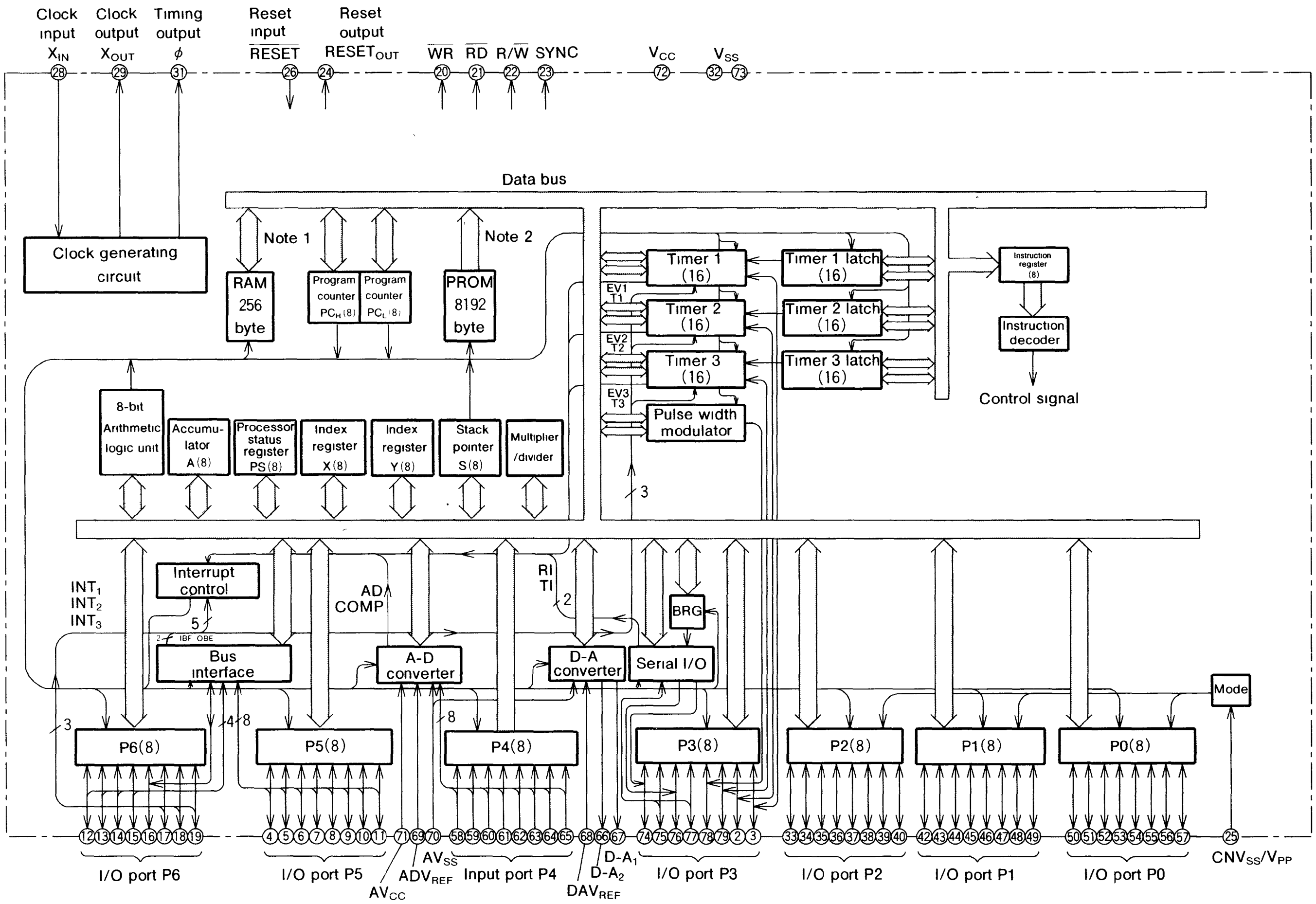
NC : No connection

M37451E4-XXXSP/M37451E4SS BLOCK DIAGRAM



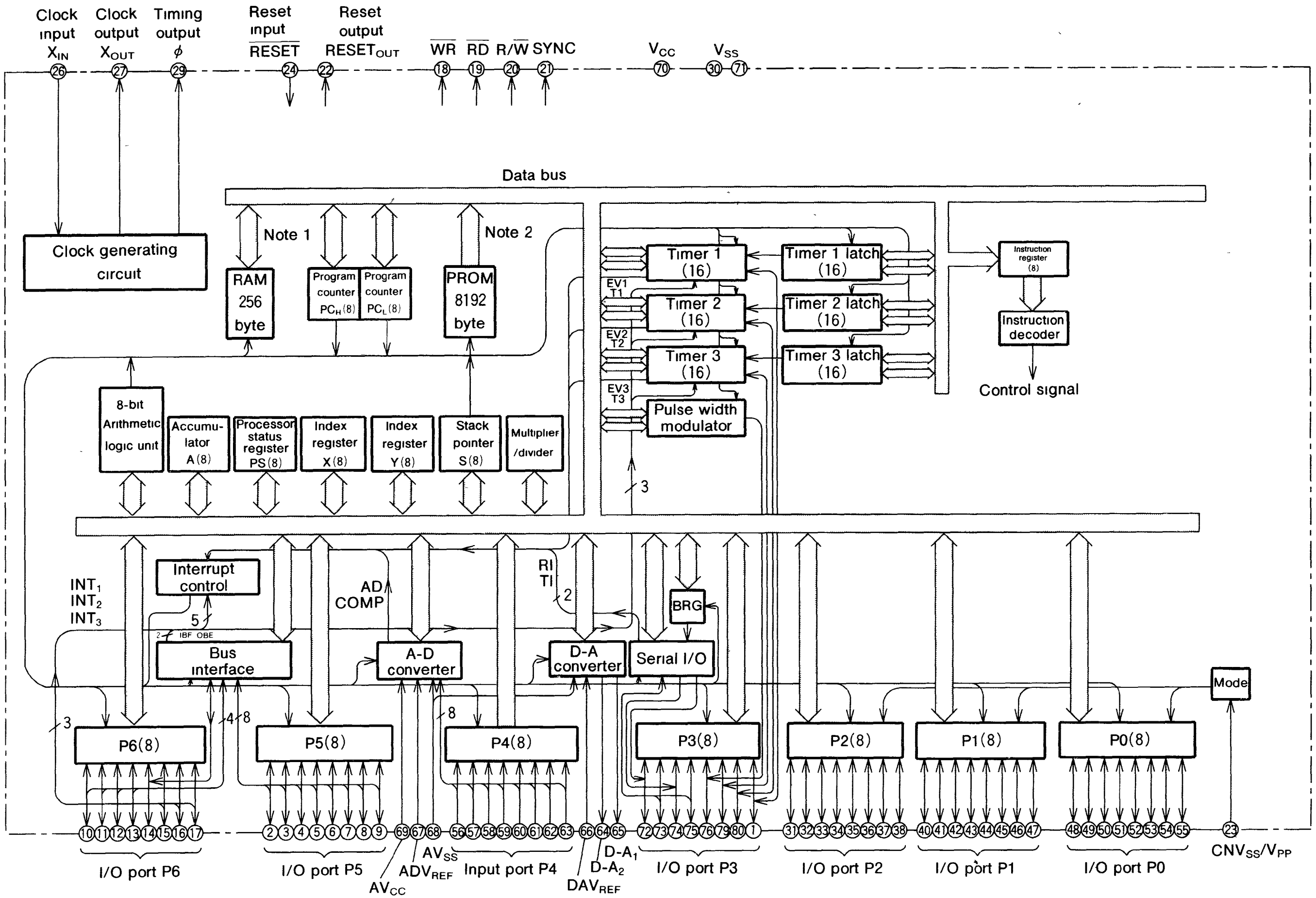
Note 1 : 384 bytes for M37451E8-XXXSP/M37451E8SS and 512 bytes for M37451EC-XXXSP/M37451ECSS.
2 : 16384 bytes for M37451E8-XXXSP/M37451E8SS and 24576 bytes for M37451EC-XXXSP/M37451ECSS

M37451E4-XXXFP/M37451E4FS BLOCK DIAGRAM



Note 1 : 384 bytes for M37451E8-XXXFP/M37451E8FS and 512 bytes for M37451EC-XXXFP/M37451ECFS
2 : 16384 bytes for M37451E8-XXXFP/M37451E8FS and 24576 bytes for M37451EC-XXXFP/M37451ECFS

M37451E4-XXXGP BLOCK DIAGRAM



Note 1 : 384 bytes for M37451E8-XXXGP and 512 bytes for M37451EC-XXXGP
2 : 16384 bytes for M37451E8-XXXGP and 24576 bytes for M37451EC-XXXGP.

FUNCTIONS OF M37451E4-XXXSP/FP/GP, M37451E8-XXXSP/FP/GP, M37451EC-XXXSP/FP/GP, M37451E4SS/FS, M37451E8SS/FS, M37451ECSS/FS

Parameter			Functions
Number of basic instructions			71(69 MELPS 740 basic instructions+2)
Instruction execution time			0. 64μs (minimum instructions, at 12.5MHz frequency)
Clock frequency			12.5MHz (max.)
Memory size	M37451E4-XXXSP/FP/GP M37451E4SS/FS	PROM	8192 bytes
		RAM	256 bytes
	M37451E8-XXXSP/FP/GP M37451E8SS/FS	PROM	16384 bytes
		RAM	384 bytes
	M37451EC-XXXSP/FP/GP M37451ECSS/FS	PROM	24576 bytes
		RAM	512 bytes
Input/Output port	P0 to P3, P5, P6	I/O	8-bit×6
	P4	Input	3-bit×1 (8-bit×1 for 80-pin model)
	D-A	Output	2-bit×1
Serial I/O			UART or clock synchronous
Timers			16-bit timer×3, 8-bit timer (Serial I/O baud rate generator)×1
A-D converter			8-bit×3 channels (8 channels for 80-pin model)
D-A converter			8-bit×2 channels
Pulse width modulator			8-bit or 16-bit×1
Data bus buffer			1-byte input and output each
Subroutine nesting			96-levels max (M37451E4, M37451E8)
			128-levels max (M37451EC)
Interrupt			6 external interrupts, 8 internal interrupts 1 software interrupt
Clock generating circuit			Built-in (ceramic or quarts crystal oscillator)
Supply voltage			5V±10%
Power dissipation			40mW (at 12.5MHz frequency)
Input/Output characters	Input/Output voltage		5V
	Output current		±5mA (max.)
Memory expansion			Possible (64K bytes max.)
Operating temperature range			−20 to 85℃
Device structure			CMOS silicon gate
Package	M37451E4-XXXSP		64-pin shrink plastic molded DIP
	M37451E8-XXXSP		
	M37451EC-XXXSP		
	M37451E4-XXXFP		80-pin plastic molded QFP (0.8mm-pitch)
	M37451E8-XXXFP		
	M37451EC-XXXFP		
	M37451E4-XXXGP		80-pin plastic molded QFP (0.65mm-pitch)
	M37451E8-XXXGP		
	M37451EC-XXXGP		
	M37451E4SS		64-pin shrink ceramic DIP
	M37451E8SS		
	M37451ECSS		
	M37451E4FS		80-pin ceramic QFN (LCC)
	M37451E8FS		
	M37451ECFS		

PIN DESCRIPTION (normal mode)

Pin	Name	Input/ Output	Functions
V_{CC}, V_{SS}	Supply voltage		Power supply inputs 5V±10% to V_{CC}, and 0V to V_{SS}
CNV_{SS}/V_{PP}	CNV_{SS}	Input	Controls the processor mode of the chip Normally connected to V_{SS} or V_{CC}.
$\overline{RESET}$	Reset input	Input	To enter the reset state, the reset input pin must be kept at a "L" for more than 8 clock cycles (under normal V_{CC} conditions) If more time is needed for the crystal oscillator to stabilize, this "L" condition should be maintained for the required time
X_{IN}	Clock input	Input	This chip has an internal clock generating circuit To control generating frequency, an external ceramic or a quartz crystal oscillator is connected between the X_{IN} and X_{OUT} pins If an external clock is used, the clock source should be connected to the X_{IN} pin and the X_{OUT} pin should be left open
X_{OUT}	Clock output	Output	
ϕ	Timing output	Output	Normally outputs signal consisting of oscillating frequency divided by four
SYNC	Synchronous signal output	Output	This signal is output "H" during operation code fetch and is used to control single stepping of programs
$R/\overline{W}$	Read/Write status output	Output	This signal determines the direction of the data bus It is "H" during read and "L" during write
$P0_0$—$P0_7$	I/O port P0	I/O	Port P0 is an 8-bit I/O port with directional registers allowing each I/O bit to be individually programmed as input or output The output structure is CMOS output The low-order bits of the address are output except in single-chip mode
$P1_0$—$P1_7$	I/O port P1	I/O	Port P1 is an 8-bit I/O port and has basically the same functions as port P0 The high-order bits of the address are output except in single-chip mode
$P2_0$—$P2_7$	I/O port P2	I/O	Port P2 is an 8-bit I/O port and has basically the same functions as port P0 Used as data bus except in single-chip mode
$P3_0$—$P3_7$	I/O port P3	I/O	Port P3 is an 8-bit I/O port and has basically the same functions as port P0. Serial I/O, PWM output, or event I/O function can be selected with a program
$P4_0$—$P4_2$ ($P4_0$—$P4_7$)	Input port P4	Input	Analog input pin for the A-D converter The 64-pin model has three pins and the 80-pin model has eight pins They may also be used as digital input pins
$P5_0$—$P5_7$	I/O port P5	I/O	Port P5 is an 8-bit I/O port and has basically the same functions as port P0. This port functions as an 8-bit data bus for the master CPU when slave mode is selected with a program.
$P6_0$—$P6_7$	I/O port P6	I/O	Port P6 is an 8-bit I/O port and has basically the same function as port P0 Pins $P6_3$—$P6_7$ change to a control bus for the master CPU when slave mode is selected with a program Pins $P6_0$—$P6_2$ may be programmed as external interrupt input pins
D-A_1, D-A_2	D-A output	Output	Analog signal from D-A converter is output
V_{REF}	Reference voltage input	Input	Reference voltage input pin for A-D and D-A converter This pin is for 64-pin model only
ADV_{REF}	A-D reference voltage input	Input	Reference voltage input pin for A-D converter This pin is for 80-pin model only
DAV_{REF}	D-A reference voltage input	Input	Reference voltage input pin for D-A converter This pin is for 80-pin model only
AV_{SS}	Analog power supply		Ground level input pin for A-D and D-A converter Same voltage as V_{SS} is applied
AV_{CC}	Analog power supply		Power supply input pin for A-D converter This pin is for 80-pin model only. Same voltage as V_{CC} is applied In the case of the 64-pin model, AV_{CC} is connected to V_{CC} internally
$\overline{RD}$	Read signal output	Output	Control signal output as active "L" when valid data is read from data bus This pin is for 80-pin model only
$\overline{WR}$	Write signal output	Output	Control signal output as active "L" when writing data from data bus to external component. This pin is for 80-pin model only
$RESET_{OUT}$	Reset output	Output	Control signal output as active "H" during reset It is used as a reset output signal for peripheral components. This pin is for 80-pin model only

PIN DESCRIPTION (EPROM mode)

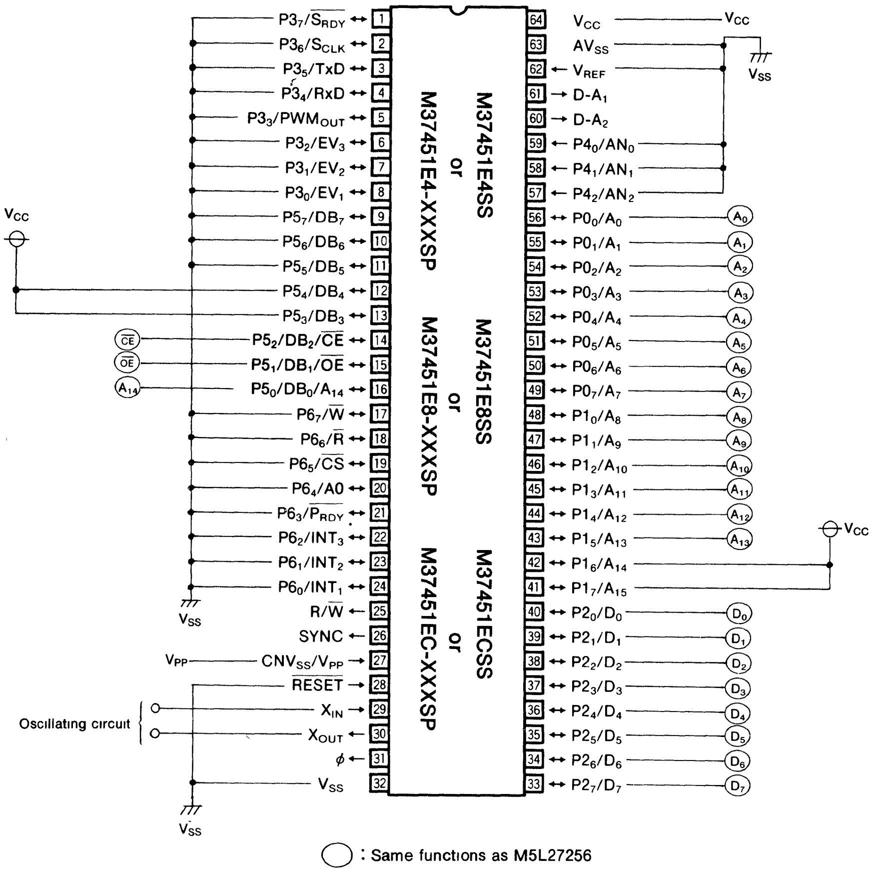
Pin	Name	Input/ Output	Functions
V_{CC}, V_{SS}	Supply voltage		Power supply inputs 5V±10% to V_{CC}, and 0V to V_{SS}
CNV_{SS}/V_{PP}	V_{PP}	Input	Connect to V_{PP} when programming or verifing
$\overline{RESET}$	Reset input	Input	Connect to V_{SS}
X_{IN}	Clock input	Input	Connect a ceramic or a quartz crystal oscillator between X_{IN} and X_{OUT} for clock oscillation
X_{OUT}	Clock output	Output	
ϕ	Timing output	Output	For timing output
SYNC	Synchronous signal output	Output	Kept to open ("L" signal is output)
$R/\overline{W}$	Read/Write status output	Output	Kept to open ("H" signal is output).
$P0_0$—$P0_7$	I/O port P0	Input	P0 works as the lower 8-bit address input
$P1_0$—$P1_7$	I/O port P1	Input	$P1_0$—$P1_5$ work as the higher 6-bit address input $P1_6$ and $P1_7$ connect to V_{CC}
$P2_0$—$P2_7$	I/O port P2	I/O	P2 works as an 8-bit data bus
$P3_0$—$P3_7$	I/O port P3	Input	Connect to V_{SS}
$P4_0$—$P4_7$ ($P4_0$—$P4_2$)	Input port P4	Input	Connect to V_{SS} The 64-pin model has only three pins $P4_0$—$P4_2$
$P5_0$—$P5_7$	I/O port P5	Input	$P5_0$, $P5_1$, $P5_2$ works as A_{14}, $\overline{OE}$, and $\overline{CE}$ inputs respectively Connect $P5_3$ and $P5_4$ to V_{CC} and $P5_5$—$P5_7$ to V_{SS}
$P6_0$—$P6_7$	I/O port P6	Input	Connect to V_{SS}
D-A_1, D-A_2	D-A output	Output	Kept to open
V_{REF}	Reference voltage input	Input	Connect to V_{SS}. This pin is for 64-pin model only
ADV_{REF}	A-D reference voltage input	Input	Connect to V_{SS} This pin is for 80-pin model only
DAV_{REF}	D-A reference voltage input	Input	Connect to V_{SS} This pin is for 80-pin model only
AV_{SS}	Analog power	Input	Connect to V_{SS}
AV_{CC}	Analog power	Input	Connect to V_{CC} or V_{SS} This pin is for 80-pin model only
$\overline{RD}$	Read signal output	Output	Kept to open ("H" signal is output) This pin is for 80-pin model only
$\overline{WR}$	Write signal output	Output	Kept to open ("H" signal is output) This pin is for 80-pin model only
$RESET_{OUT}$	Reset output	Output	Kept to open ("H" signal is output) This pin is for 80-pin model only

EPROM MODE

The M37451E4-XXXSP/FP/GP, M37451E4SS/FS features an EPROM mode in addition to its normal modes. When the $\overline{\text{RESET}}$ signal level is low ("L") and CNV_{SS}/V_{PP} signal level is high ("H"), the chip automatically enters the EPROM mode. Table 1 list the correspondence between pins and Figure 1, 2 and 3 give the pin connections in the EPROM mode. When in the EPROM mode, ports P0, $P1_0$—$P1_5$, P2, $P5_0$—$P5_2$ and CNV_{SS} are used for the PROM (equivalent to the M5L27256). When in this mode, the built-in PROM can be written to or read from using these pins in the same way as with the M5L27256. The oscillator should be connected to the X_{IN} and X_{OUT} pins, or external clock should be connected to the X_{IN} pin.

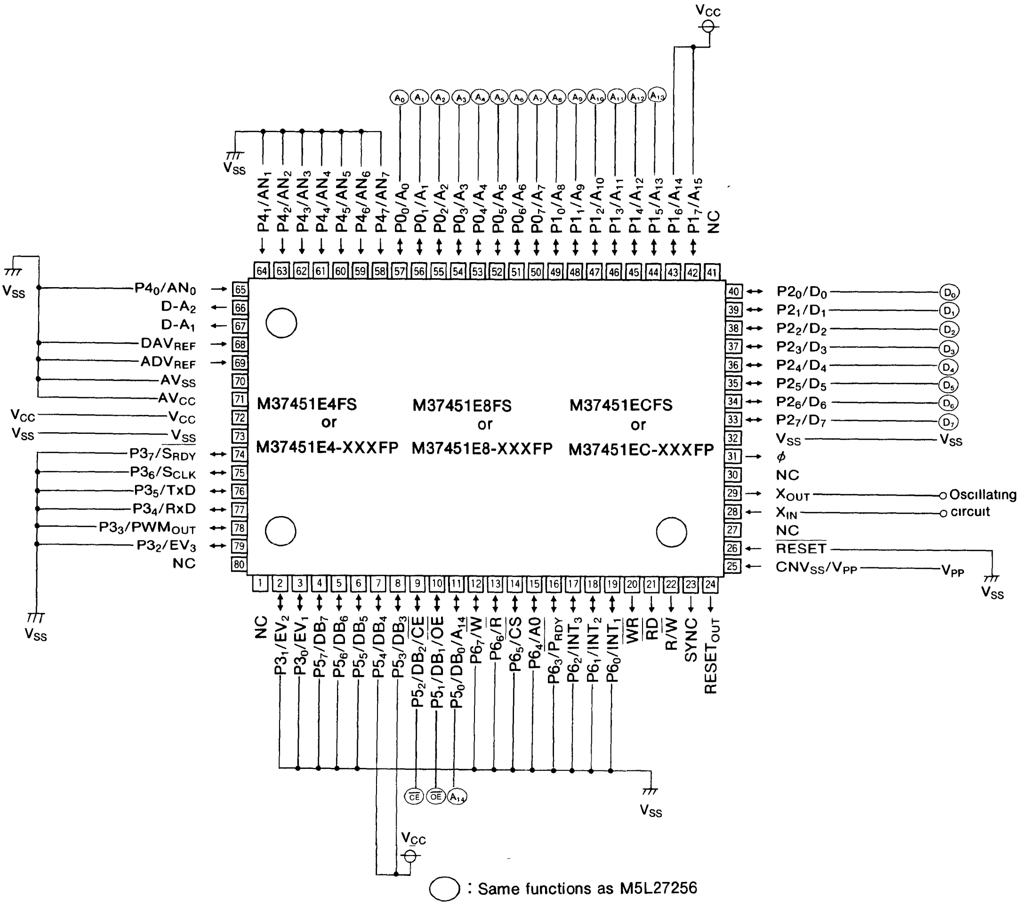
Table 1. Pin function in EPROM mode

	M37451E4-XXXSP/FP/GP, M37451E4SS/FS	M5L27256
V_{CC}	V_{CC}	V_{CC}
V_{PP}	CNV_{SS}/V_{PP}	V_{PP}
V_{SS}	V_{SS}	V_{SS}
Address input	Ports P0, $P1_0$—$P1_5$, $P5_0$	A_0—A_{14}
Data I/O	Port P2	D_0—D_7
$\overline{CE}$	$P5_2/DB_2/\overline{CE}$	$\overline{CE}$
$\overline{OE}$	$P5_1/DB_1/\overline{OE}$	$\overline{OE}$



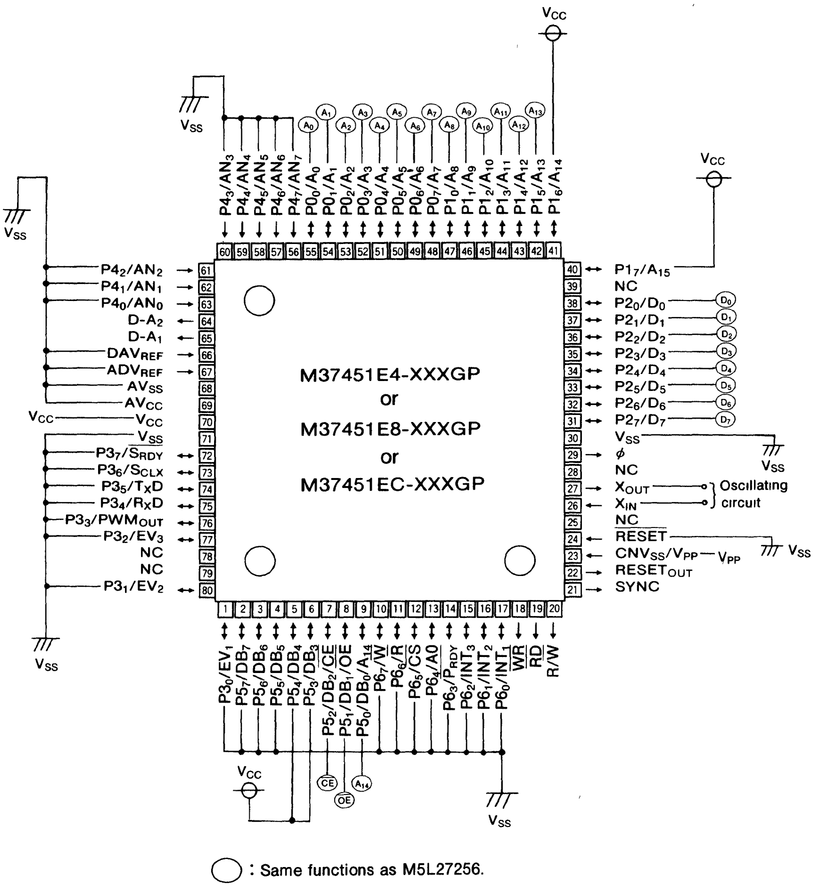
◯ : Same functions as M5L27256

Fig. 1 Pin connection in EPROM mode (64-pin model)



◯ : Same functions as M5L27256

Fig. 2 Pin connection in EPROM mode (0.8mm pitch 80-pin model)



○ : Same functions as M5L27256.

Fig. 3 Pin connection in EPROM mode (0.65mm pitch 80-pin model)

PROM READING, WRITING AND ERASING

Reading

To read the PROM, set the $\overline{CE}$ and $\overline{OE}$ pins to a "L" level, and supply 0V to the $\overline{RESET}$ pin, 5V to the V_{CC} pin and the CNV_{SS} (V_{PP}) pin. Input the address of the data (A_0—A_{14}) to be read and the data will be output to the I/O pins D_0—D_7. The data I/O pins will be floating when either the $\overline{CE}$ or $\overline{OE}$ pins are in the "H" state.

Writing

To write to the PROM, set the $\overline{OE}$ pin to an "H" level, and supply 0V to the $\overline{RESET}$ pin, 6V to the V_{CC} pin and 12.5V to the V_{PP} pin. The CPU will enter the program mode when V_{PP} is applied to the V_{PP} pin. The address to be written to is selected with pins A_0—A_{14}, and the data to be written is input to pins D_0—D_7. Set the $\overline{CE}$ pin to a "L" level to begin writing.

Erasing

Data can only erased on the M37451E4SS/FS, M37451E8SS/FS and M37451ECSS/FS ceramic package, which includes a window. To erase data on this chip, use an ultraviolet light source with a 2537 Angstrom wave length. The minimum radiation power necessary for erasing is 15W•s/cm^2.

NOTES ON HANDLING

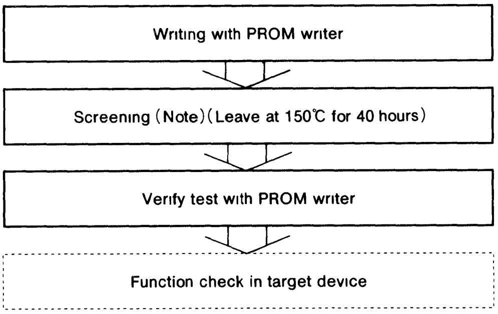
(1) Sunlight and fluorescent light contain wave lengths capable of erasing data. For ceramic package types, cover the transparent window with a seal (provided) when this chip is in use. However, this seal must not contact the lead pins.

(2) Before erasing, the glass should be cleaned and stains such as finger prints should be removed thoroughly. If these stains are not removed, complete erasure of the data could be prevented.

(3) Since a high voltage is used to write data, care should be taken when turning on the PROM writer's power.

(4) For the programmable microcomputer (shipped in blank or OTP type) , Mitsubishi does not perform PROM write test and screening in the assembly process and following process. To improve reliability after write, performing write and test according to the flow below before use is recommended.

(5) In EPROM mode, address A_{15} is set to "H" automatically.



Note : Since the screening temperature is higher than storage temperature, never expose to 150℃ exceeding 100 hours.

Table 2. I/O signal in each mode

Pin Mode	$\overline{CE}$	$\overline{OE}$	V_{PP}	V_{CC}	Port P2
Read-out	V_{IL}	V_{IL}	5V	5V	Output
Programming	V_{IL}	V_{IH}	12.5V	6V	Input
Programming verify	V_{IH}	V_{IL}	12.5V	6V	Output
Program disable	V_{IH}	V_{IH}	12.5V	6V	Floating

Note 1 : V_{IL} and V_{IH} indicate a "L" and "H" input voltage, respectively
2 : An X indicates either V_{IL} or V_{IH}

M37451E4DXXXSP/FP
M37451E8DXXXSP/FP
PROM VERSION of
M37451M4DXXXSP/FP, M37451M8DXXXSP/FP

DESCRIPITION

The M37451E4DXXXSP/FP is a single-chip microcomputer designed with CMOS silicon gate technology. It is housed in a 64-pin shrink plastic molded DIP or an 80-pin plastic molded QFP (0.8mm pitch). The features of this chip are similar to those of the M37451M4DXXXSP/FP except that this chip has a 8192 bytes PROM built-in. This single-chip microcomputer is useful for office automation appliances and consumer appliance controllers.

In addition to its simple instruction sets, the PROM, RAM and I/O addresses are placed on the same memory map to enable easy programming. It also has a unique feature that enables it to be used as a slave microcomputer.

Apart from the expansion in operating temperature range and consequent differences in electrical characteristics (Note), functions are the same as those of the M37451E4-XXXSP/FP.

The differences between the M37451E4DXXXSP/FP and M37451E8DXXXSP/FP are as shown below.

Type name	ROM size	RAM size
M37451E4DXXXSP/FP	8192 bytes	256 bytes
M37451E8DXXXSP/FP	16384 bytes	384 bytes

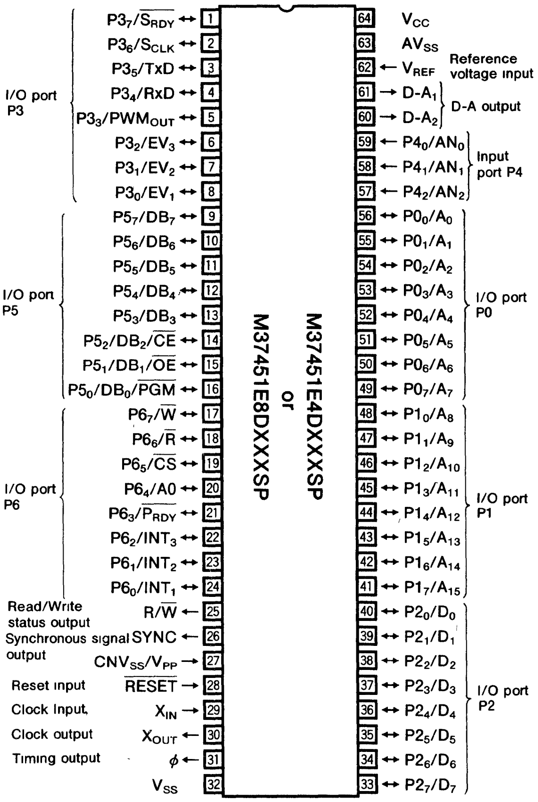
The number of analog input pins for the 80-pin model (FP version) is different from the 64-pin model (SP version). In addition, the 80-pin model has special pins for $\overline{RD}$, $\overline{WR}$, $RESET_{OUT}$, DAV_{REF}, ADV_{REF}, AV_{CC}, and the 64-pin model has a special V_{REF} pin.

Note : The maximum value of supply current is 20mA.
All other values are the same as that of M37451E4-XXXSP/FP.

FEATURES

- Number of basic instructions ································ 71
  69 MELPS 740 basic instructions + 2 multiply/divide instructions
- Instruction execution time
  (minimum instructions at 12.5 MHz frequency) ··· 0.64μs
- Single power supply ································ 5V±5%
- Power dissipation normal operation mode
  (at 12.5 MHz frequency) ································ 40mW
- Subroutine nesting ································ 96 levels max.
- Interrupt ································ 15 events
- Master CPU bus interface ································ 1 byte
- 16-bit timer ································ 3
- 8-bit timer (Serial I/O use) ································ 1
- Serial I/O (UART or clock synchronous) ································ 1
- A-D converter (8-bit resolution) ········· 3 channels (DIP)
  8 channels (QFP)
- D-A converter (8-bit resolution) ················· 2 channels
- PWM output with 8-bit prescaler
  (Either resolution 8-bit or 16-bit is software selectable) ··· 1
- Programmable I/O ports
  (Ports P0, P1, P2, P3, P5, P6) ································ 48
- Input port (Port P4) ································ 3 (DIP), 8 (QFP)
- Output ports (Ports D-A₁, D-A₂) ································ 2
- PROM (equivalent to the M5L27256)
  program voltage ································ 12.5V
- Operating temperature ································ −40 to 85℃

PIN CONFIGURATION (TOP VIEW)

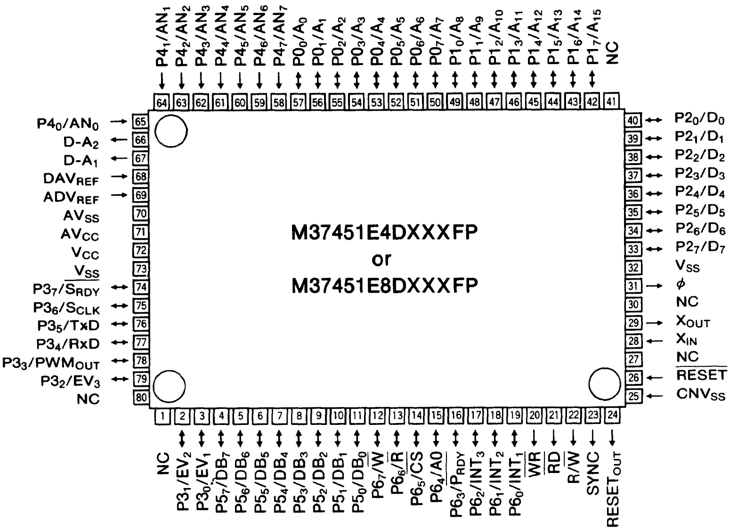


Outline 64P4B

APPLICATION

Industrial machinery

PIN CONFIGURATION (TOP VIEW)



Outline 80P6N

NC : No connection

SERIES 7470

MITSUBISHI MICROCOMPUTERS

M37470M2-XXXSP,M37470M4-XXXSP M37470M8-XXXSP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

DESCRIPTION

The M37470M2-XXXSP is a single-chip microcomputer designed with CMOS silicon gate technology. It is housed in a 32-pin shrink plastic molded DIP. This single-chip microcomputer is useful for business equipment and other consumer applications.

In addition to its simple instruction set, the ROM, RAM, and I/O addresses are placed on the same memory map to enable easy programming.

The differences among M37470M2-XXXSP, M37470M4-XXXSP and M37470M8-XXXSP are noted below. The following explanations apply to the M37470M2-XXXSP. Specificaiton variations for other chips are noted accordingly.

Type name	ROM size	RAM size
M37470M2-XXXSP	4096 bytes	128 bytes
M37470M4-XXXSP	8192 bytes	192 bytes
M37470M8-XXXSP	16384 bytes	384 bytes

FEATURES

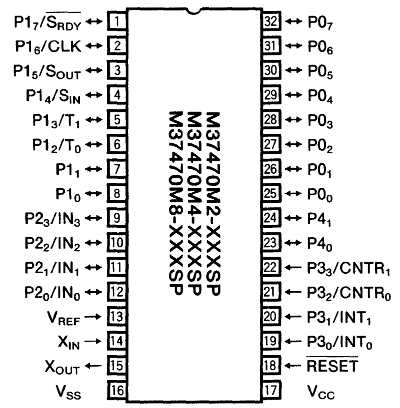
- Number of basic instructions ········· 69
- Memory size
  - ROM ········· 4096 bytes (M37470M2)
  - RAM ········· 128 bytes (M37470M2)
- Instruction execution time
  - ········· 1μs (minimum instructions at 4MHz frequency)
- Single power supply ········· 2 7∼5.5V
- Power dissipation normal operation mode
  - ········· 17.5mW (at 4MHz frequency)
- Subroutine nesting ········· 64 levels max. (M37470M2)
- Interrupt ········· 12types, 10vectors
- 8-bit timer ········· 4
- Programmable I/O ports
  - (Ports P0, P1, P2, P4) ········· 22
- Input port (Port P3) ········· 4
- Serial I/O (8-bit) ········· 1
- A-D converter ········· 8-bit, 4channel

APPLICATION

Audio-visual equipment, VCR, Tuner

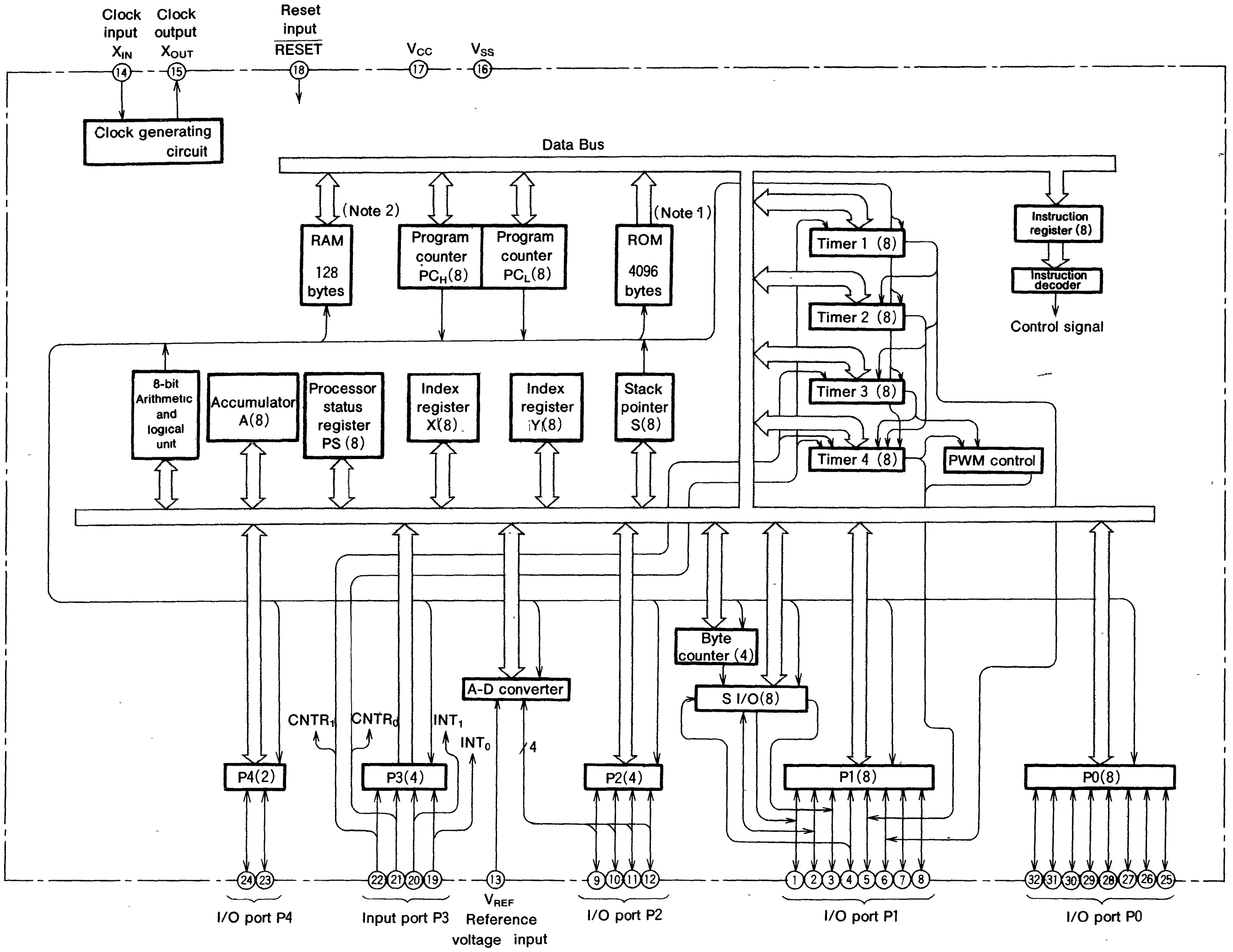
Office automation equipment

PIN CONFIGURATION (TOP VIEW)



Outline 32P4B

M37470M2-XXXSP BLOCK DIAGRAM



Note 1 : 8192 bytes for M37470M4-XXXSP and 16384 bytes for M37470M8-XXXSP
2 : 192 bytes for M37470M4-XXXSP and 384 bytes for M37470M8-XXXSP

FUNCTIONS OF M37470M2-XXXSP, M37470M4-XXXSP, M37470M8-XXXSP

Parameter			Functions
Number of basic instructions			69
Instruction execution time			1μs (minimum instructions, at 4MHz frequency)
Clock frequency			4MHz (max.)
Memory size	M37470M2-XXXSP	ROM	4096 bytes
		RAM	128 bytes
	M37470M4-XXXSP	ROM	8192 bytes
		RAM	192 bytes
	M37470M8-XXXSP	ROM	16384 bytes
		RAM	384 bytes
Input/Output port	P0, P1	I/O	8-bit×2
	P2	I/O	4-bit×1
	P3	Input	4-bit×1
	P4	I/O	2-bit×1
Serial I/O			8-bit×1
Timers			8-bit timer×4
A-D converter			8-bit×1 (4 channels)
Subroutine nesting	M37470M2-XXXSP		64 levels (max)
	M37470M4-XXXSP		96 levels (max)
	M37470M8-XXXSP		192 levels (max)
Interrupt			5 external interrupts, 6 internal interrupts 1 software interrupt
Clock generating circuit			Built-in with internal feedback resistor (ceramic or quarts crystal oscillator)
Supply voltage			2 7~5 5V
Power dissipation			17 5mW (at 4MHz frequency)
Input/Output characters	Input/Output voltage		5V
	Output current		−5~10mA(P0, P1, P2, P4 : CMOS tri-states)
Operating temperature range			−20~85℃
Device structure			CMOS silicon gate
Package			32-pin shrink plastic molded DIP

PIN DESCRIPTION

Pin	Name	Input/ Output	Functions
V_{CC}, V_{SS}	Supply voltage		Power supply inputs 2.7~5.5V to V_{CC}, and 0V to V_{SS}.
$\overline{\text{RESET}}$	Reset input	Input	To enter the reset state, the reset input pin must be kept at a "L" for more than 2μs (under normal V_{CC} conditions).
X_{IN}	Clock input	Input	These are I/O pins of internal clock generating circuit for main clock To control generating frequency, an external ceramic or a quartz crystal oscillator is connected between the X_{IN} and X_{OUT} pins. If an external clock is used, the clock source should be connected the X_{IN} pin and the X_{OUT} pin should be left open. Feedback resistor is connected between X_{IN} and X_{OUT}.
X_{OUT}	Clock output	Output	
V_{REF}	Reference voltage input	Input	This is reference voltage input pin for the A-D converters.
$P0_0$~$P0_7$	I/O port P0	I/O	Port P0 is an 8-bit I/O port The output structure is CMOS output When this port is selected for input, pull-up transistor can be connected in units of 1-bit and a key on wake up function is provided
$P1_0$~$P1_7$	I/O port P1	I/O	Port P1 is an 8-bit I/O port The output structure is CMOS output. When this port is selected for input, pull-up transistor can be connected in units of 4-bit. $P1_2$, $P1_3$ are in common with timer output pins T_0, T_1. $P1_4$, $P1_5$, $P1_6$, $P1_7$ are in common with serial I/O pins S_{IN}, S_{OUT}, CLK, $\overline{S_{RDY}}$, respectively. The output structure of S_{OUT} and $\overline{S_{RDY}}$ can be changed to N-channel open drain output
$P2_0$~$P2_3$	I/O port P2	I/O	Port P2 is an 4-bit I/O port The output structure is CMOS output When this port is selected for input, pull-up transistor can be connected in units of 4-bit. This port is in common with analog input pins IN_0~IN_3.
$P3_0$~$P3_3$	Input port P3	Input	Port P3 is an 4-bit input port. $P3_0$, $P3_1$ are in common with external interrupt input pins INT_0, INT_1 and $P3_2$, $P3_3$ are in common with timer input pins $CNTR_0$, $CNTR_1$.
$P4_0$, $P4_1$	I/O port P4	I/O	Port P4 is an 2-bit I/O port The output structure is CMOS output When this port is selected for input, pull-up transistor can be connected in units of 2-bit

FUNCTIONAL DESCRIPTION

Central Processing Unit (CPU)

The M37470 microcomputers use the standard MELPS 740 instruction set. For details of instructions, refer to the MELPS 740 CPU core basic functions, or the MELPS 740 Software Manual.

Machine-resident instructions are as follows:
The FST and SLW instructions are not provided.
The MUL and DIV instructions are not provided.
The WIT instruction can be used.
The STP instruction can be used.

CPU Mode Register

The CPU mode register is allocated to address $00FB_{16}$. This register has a stack page selection bit.

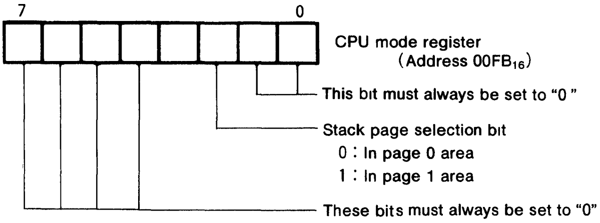


Fig. 1 Structure of CPU mode register

MEMORY

• Special Function Register (SFR) Area

The special function register (SFR) area contains the registers relating to functions such as I/O ports and timers.

• RAM

RAM is used for data storage as well as a stack area.

• ROM

ROM is used for storing user programs as well as the interrupt vector area.

• Interrupt Vector Area

The interrupt vector area is for storing jump destination addresses used at reset or when an interrupt is generated.

• Zero Page

Zero page addressing mode is useful because it enables access to this area with fewer instruction cycles.

• Special Page

Special page addressing mode is useful because it enables access to this area with fewer instruction cycles.

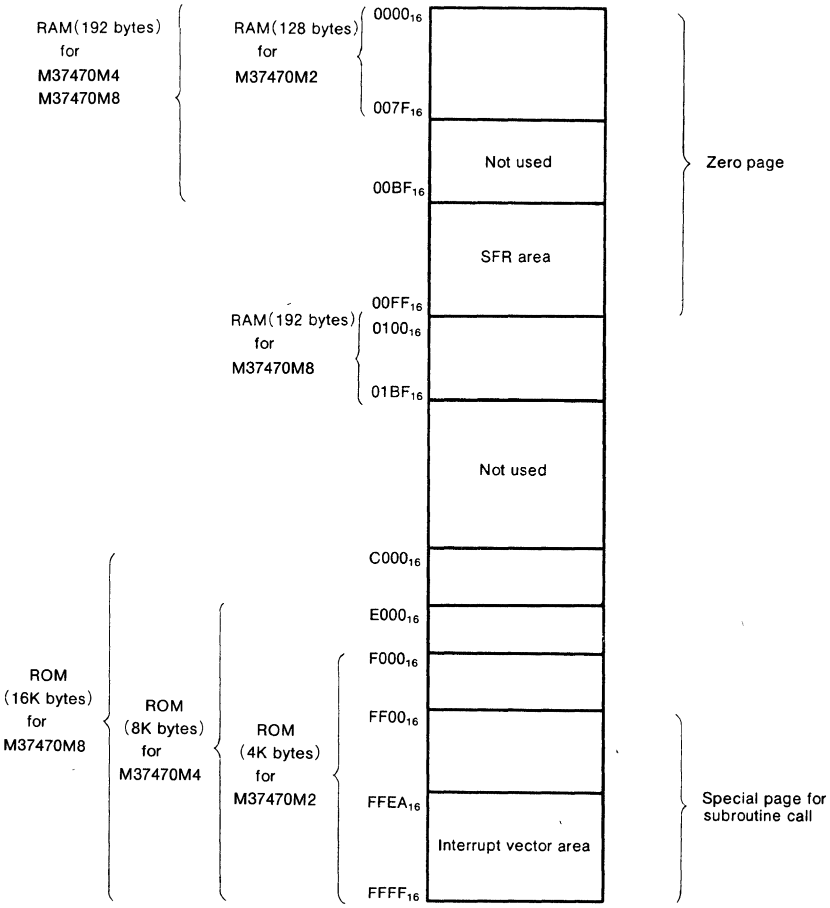


Fig. 2 Memory map

00C0$_{16}$	Port P0	
00C1$_{16}$	Port P0 directional register	
00C2$_{16}$	Port P1	
00C3$_{16}$	Port P1 directional register	
00C4$_{16}$	Port P2	
00C5$_{16}$	Port P2 directional register	
00C6$_{16}$	Port P3	
00C7$_{16}$		
00C8$_{16}$	Port P4	
00C9$_{16}$	Port P4 directional register	
00CA$_{16}$		
00CB$_{16}$		
00CC$_{16}$		
00CD$_{16}$		
00CE$_{16}$		
00CF$_{16}$		
00D0$_{16}$	P0 pull-up control register	
00D1$_{16}$	P1~P4 pull-up control register	
00D2$_{16}$		
00D3$_{16}$		
00D4$_{16}$	Edge polarity selection register	
00D5$_{16}$		
00D6$_{16}$	Input latch register	
00D7$_{16}$		
00D8$_{16}$		
00D9$_{16}$	A-D control register	
00DA$_{16}$	A-D conversion register	
00DB$_{16}$		
00DC$_{16}$	Serial I/O mode register	
00DD$_{16}$	Serial I/O register	
00DE$_{16}$	Serial I/O counter	Byte counter
00DF$_{16}$		

00E0$_{16}$	
00E1$_{16}$	
00E2$_{16}$	
00E3$_{16}$	
00E4$_{16}$	
00E5$_{16}$	
00E6$_{16}$	
00E7$_{16}$	
00E8$_{16}$	
00E9$_{16}$	
00EA$_{16}$	
00EB$_{16}$	
00EC$_{16}$	
00ED$_{16}$	
00EE$_{16}$	
00EF$_{16}$	
00F0$_{16}$	Timer 1
00F1$_{16}$	Timer 2
00F2$_{16}$	Timer 3
00F3$_{16}$	Timer 4
00F4$_{16}$	
00F5$_{16}$	
00F6$_{16}$	
00F7$_{16}$	Timer FF register
00F8$_{16}$	Timer 12 mode register
00F9$_{16}$	Timer 34 mode register
00FA$_{16}$	Timer mode register 2
00FB$_{16}$	CPU mode register
00FC$_{16}$	Interrupt request register 1
00FD$_{16}$	Interrupt request register 2
00FE$_{16}$	Interrupt control register 1
00FF$_{16}$	Interrupt control register 2

Fig. 3 SFR (Special Function Register) memory map

INTERRUPTS

Interrupts can be caused by 12 different events consisting of five external, six internal, and one software events.

Interrupts are vectored interrupts with priorities shown in Table 1. Reset is also included in the table because its operation is similar to an interrupt.

When an interrupt is accepted, the registers are pushed, interrupt disable flag I is set, and the program jumps to the address specified in the vector table. The interrupt request flag is cleared automatically. The reset and BRK instruction interrupt can never be inhibited. Other interrupts are disabled when the interrupt inhibit flag is set.

All interrupts except the BRK instruction interrupt have an interrupt request bit and an interrupt enable bit. The interrupt request bits are in interrupt request registers 1 and 2 and the interrupt enable bits are in interrupt control registers 1 and 2. External interrupts INT_0 and INT_1 can be asserted on either the falling or rising edge as set in the edge polarity selection register. When "0" is set to this register, the interrupt is activated on the falling edge; when "1" is set to the register, the interrupt is activated on the rising edge.

When the device is put into power-down state by the STP instruction or the WIT instruction, if bit 5 in the edge polarity selection register is "1", the INT_1 interrupt becomes a key on wake up interrupt. When a key on wake up interrupt is valid, an interrupt request is generated by applying the "L" level to any pin in port P0. In this case, the port used for interrupt must have been set for the input mode.

If bit 5 in the edge polarity selection register is "0" when the device is in power-down state, the INT_1 interrupt is selected. Also, if bit 5 in the edge polarity selection register is set to "1" when the device is not in a power-down state, neither key on wake up interrupt request nor INT_1 interrupt request are generated.

The $CNTR_0$/$CNTR_1$ interrupts function in the same as INT_0 and INT_1. The interrupt input pin can be specified for either $CNTR_0$ or $CNTR_1$ pin by setting bit 4 in the edge polarity selection register.

Figure 4 shows the structure of the edge polarity selection register, interrupt request registers 1 and 2, and interrupt control registers 1 and 2.

Interrupts other than the BRK instruction interrupt and reset are accepted when the interrupt enable bit is "1", interrupt request bit is "1", and the interrupt disable flag is "0". The interrupt request bit can be reset with a program, but not set. The interrupt enable bit can be set and reset with a program.

Reset is treated as a non-maskable interrupt with the highest priority. Figure 5 shows interrupts control.

Table 1. Interrupt vector address and priority

Event	Priority	Vector addresses	Remarks
$\overline{RESET}$	1	$FFFF_{16}$, $FFFE_{16}$	Non-maskable
INT_0 interrupt	2	$FFFD_{16}$, $FFFC_{16}$	External interrupt (phase programmable)
INT_1 interrupt or key on wake up interrupt	3	$FFFB_{16}$, $FFFA_{16}$	External interrupt (INT_1 is phase programmable)
$CNTR_0$ interrupt or $CNTR_1$ interrupt	4	$FFF9_{16}$, $FFF8_{16}$	External interrupt (phase programmable)
Timer 1 interrupt	5	$FFF7_{16}$, $FFF6_{16}$	
Timer 2 interrupt	6	$FFF5_{16}$, $FFF4_{16}$	
Timer 3 interrupt	7	$FFF3_{16}$, $FFF2_{16}$	
Timer 4 interrupt	8	$FFF1_{16}$, $FFF0_{16}$	
Serial I/O interrupt	9	$FFEF_{16}$, $FFEE_{16}$	
A-D conversion completion interrupt	10	$FFED_{16}$, $FFEC_{16}$	
BRK instruction interrupt	11	$FFEB_{16}$, $FFEA_{16}$	Non-maskable software interrupt

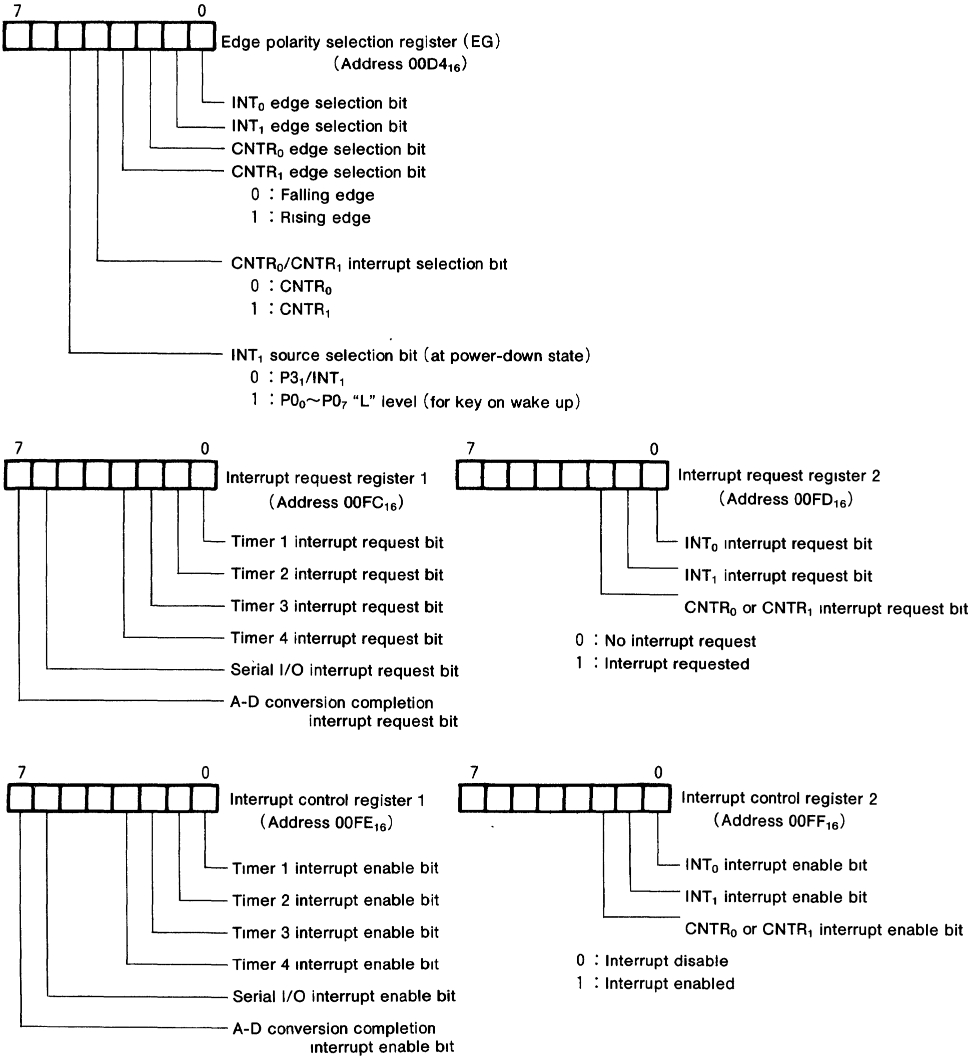


Fig. 4 Structure of registers related to interrupt

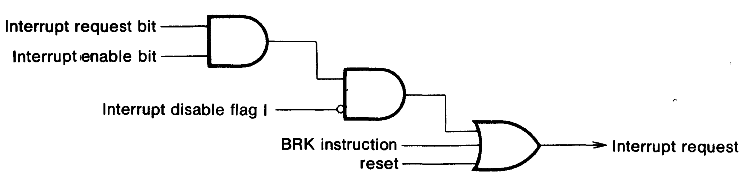


Fig. 5 Interrupt control

TIMER

The M37470M2-XXXSP has four timers; timer 1, timer 2, timer 3 and timer 4.

A block diagram of timer 1 through 4 is shown in Figure 6.

Timer 1 can be operated in the timer mode, event count mode, or pulse output mode. Timer 1 starts counting when bit 0 in the timer 12 mode register (address $00F8_{16}$) is set to "0".

The count source can be selected from the $f(X_{IN})$ divided by 16 or event input from $P3_2$/$CNTR_0$ pin. When bit 1 in the timer 12 mode register is "0", $f(X_{IN})$ divided by 16 is selected. When bit 1 in the timer 12 mode register is "1", an event input from the $CNTR_0$ pin is selected. Event inputs are selected depending on bit 2 in the edge polarity selection register (address $00D4_{16}$). When this bit is "0", the inverted value of $CNTR_0$ input is selected; when the bit is "1", $CNTR_0$ input is selected.

When bit 3 in the timer 12 mode register is set to "1", the $P1_2$ pin becomes timer output T_0. When the direction register of $P1_2$ is set for the output mode at this time, the timer 1 overflow divided by 2 is output from T_0. The initial output value can be set by writing the value to bit 0 in the timer FF register (address $00F7_{16}$) after setting "1" to bit 0 in timer mode register 2.

Timer 2 can only be operated in the timer mode. Timer 2 starts counting when bit 4 in the timer 12 mode register is set to "0".

The count source can be selected from the divide by 16, divide by 64, divide by 128, or divide by 256 frequency of $f(X_{IN})$, and timer 1 overflow. When bit 5 in the timer 12 mode register is "0", any of the divide by 16, divide by 64, divide by 128, or divide by 256 frequency of $f(X_{IN})$ is selected. The divide ratio is selected according to bit 6 and bit 7 in the timer 12 mode register. When bit 5 in the timer 12 mode register is "1", timer 1 overflow is selected as the count source.

Timer 3 can be operated in the timer mode, event count mode, or PWM mode. Timer 3 starts counting when bit 0 in the timer 34 mode register (address $00F9_{16}$) is set to "0".

The count source can be selected from the $f(X_{IN})$ divided by 16, timer 1 or timer 2 overflow, or an event input from $P3_3$/$CNTR_1$ pins according to the statuses of bit 1 and bit 2 in the timer 34 mode register, bit 6 in the timer mode register 2 (address $00FA_{16}$). Note, however, that if timer 1 overflow or timer 2 overflow is selected for the count source of timer 3 when timer 1 overflow is selected for the count source of timer 2, timer 1 overflow is always selected regardless of the status of bit 6 in the timer mode register 2. Event inputs are selected depending on bit 3 in the edge polarity selection register. When this bit is "0", the inverted value of $CNTR_1$ input is selected; when the bit is "1", $CNTR_1$ input is selected.

Timer 4 can be operated in the timer mode, event count mode, pulse output mode, pulse width measuring mode, or PWM mode. Timer 4 starts counting when bit 3 in the timer 34 mode register is set to "0" when bit 6 in this register is "0". When bit 6 is "1", the pulse width measuring mode is selected. The count source can be selected from timer 3 overflow, the $f(X_{IN})$ divided by 16, timer 1 or timer 2 overflow, or an event input from $P3_3$/$CNTR_1$ pins according to the statuses of bit 4 and bit 5 in the timer 34 mode register, bit 6 in the timer mode register 2. Note, however, that if timer 1 overflow or timer 2 overflow is selected for the count source of timer 4 when timer 1 overflow is selected for the count source of timer 2, timer 1 overflow is always selected regardless of the status of bit 6 in the timer mode register 2. Event inputs are selected depending on bit 3 in the edge polarity selection register. When this bit is "0", the inverted value of $CNTR_1$ input is selected; when the bit is "1", $CNTR_1$ input is selected.

When bit 7 in the timer 34 mode register is set to "1", the $P1_3$ pin becomes timer output T_1. When the direction register of $P1_3$ is set for the output mode at this time, the timer 4 overflow divided by 2 is output from T_1 when bit 7 in the timer mode register 2 is "0". The initial output value can be set by writing the value to bit 1 in the timer FF register after setting "1" to bit 1 in timer mode register 2.

(1) Timer mode

Timer perform down count operations with the dividing ratio being $1/(n+1)$. Writing a value to the timer latch sets a value to the timer. When the value to be set to the timer latch is nn_{16}, the value to be set to a timer is nn_{16}, which is down counted at the falling edge of the count source from nn_{16} to $(nn_{16}\text{-}1)$ to $(nn_{16}\text{-}2)$ to...01_{16} to 00_{16} to FF_{16}. At the falling edge of the count source immediately after timer value has reached FF_{16}, value $(nn_{16}\text{-}1)$ obtained by subtracting one from the timer latch value is set (reloaded) to the timer to continue counting. At the rising edge of the count source immediately after the timer value has reached FF_{16}, an overflow occurs, an interrupt request.

(2) Event count mode

Timer operates in the same way as in the timer mode except that it counts input from the $CNTR_0$ or $CNTR_1$ pin.

(3) Pulse output mode

In this mode, duty 50% pulses are output from the T_0 or T_1 pin. When the timer overflows, the polarity of the T_0 or T_1 pin output pin level is inverted.

(4) Pulse width measuring mode

The M37470 can measure the "H" or "L" width of the $CNTR_0$ or $CNTR_1$ input waveform by using the pulse width measuring mode of timer 4. The pulse width measuring mode is selected by writing "1" to bit 6 in the timer 34 mode register. In the pulse width measuring mode, the timer counts the count source while the $CNTR_0$ or $CNTR_1$ input is "H" or "L". Whether the $CNTR_0$ input or $CNTR_1$ input be measured can be specified by the status of bit 4 in the edge polarity selection register; whether the "H" width or "L" width be measured can be specified by the status of bit 2 ($CNTR_0$) and bit 3 ($CNTR_1$) in the edge polarity selection register.

(5) PWM mode

The PWM mode can be entered for timer 3 and timer 4 by setting bit 7 in the timer mode register 2 to "1". In the PWM mode, the $P1_3$ pin is set for timer output T_1 to output PWM waveforms by setting bit 7 in the timer 34 mode register to "1". The directional register of $P1_3$ must be set for the output mode before this can be done.

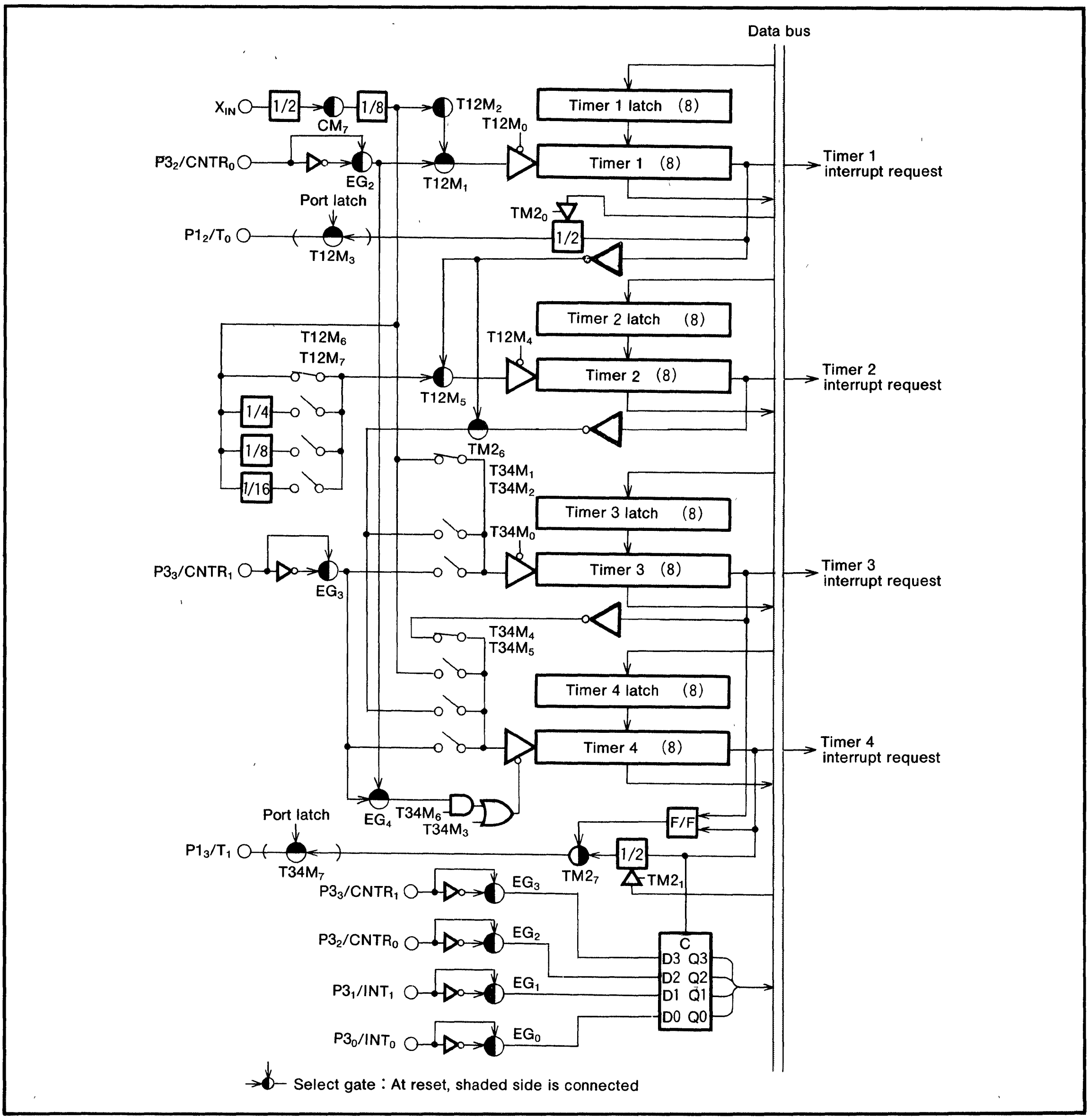
In the PWM mode, timer 3 is counting and timer 4 is idle while the PWM waveform is "L". When timer 3 overflows, the PWM waveform goes "H". At this time, timer 3 stops counting simultaneously and timer 4 starts counting. When timer 4 overflows, the PWM waveform goes "L", and timer 4 stops and timer 3 starts counting again. Consequently, the "L" duration of the PWM waveform is determined by the value of timer 3; the "H" duration of the PWM waveform is determined by the value of timer 4.

When a value is written to the timer in operation during the PWM mode, the value is only written to the timer latch, and not written to the timer. In this case, if the timer overflows, a value one less the value in the timer latch is written to the timer. When any value is written to an idle timer, the value is written to both the timer latch and the timer.

In this mode, do not select timer 3 overflow as the count source for timer 4.

INPUT LATCH FUNCTION

The M37470 can latch the $P3_0/INT_0$, $P3_1/INT_1$, $P3_2/CNTR_0$, and $P3_3/CNTR_1$ pin level into the input latch register (address $00D6_{16}$) when timer 4 overflows. The polarity of each pin latched to the input latch register can be selected by using the edge polarity selection register. When bit 0 in the edge polarity selection register is "0", the inverted value of the $P3_0/INT_0$ pin level is latched; when the bit is "1", the $P3_0/INT_0$ pin level is latched as is. When bit 1 in the edge polarity selection register is "0", the inverted value of the $P3_1/INT_1$ pin level is latched; when the bit is "1", the $P3_1/INT_1$ pin level is latched as is. When bit 2 in the edge polarity selection register is "0", the inverted value of the $P3_2/CNTR_0$ pin level is latched; when the bit is "1", the $P3_2/CNTR_0$ pin level is latched as is. When bit 3 in the edge polarity selection register is "0", the inverted value of the $P3_3/CNTR_1$ pin level is latched; when the bit is "1", the $P3_3/CNTR_1$ pin level is latched as is.



Select gate : At reset, shaded side is connected

Fig. 6 Block diagram of timer 1 through 4

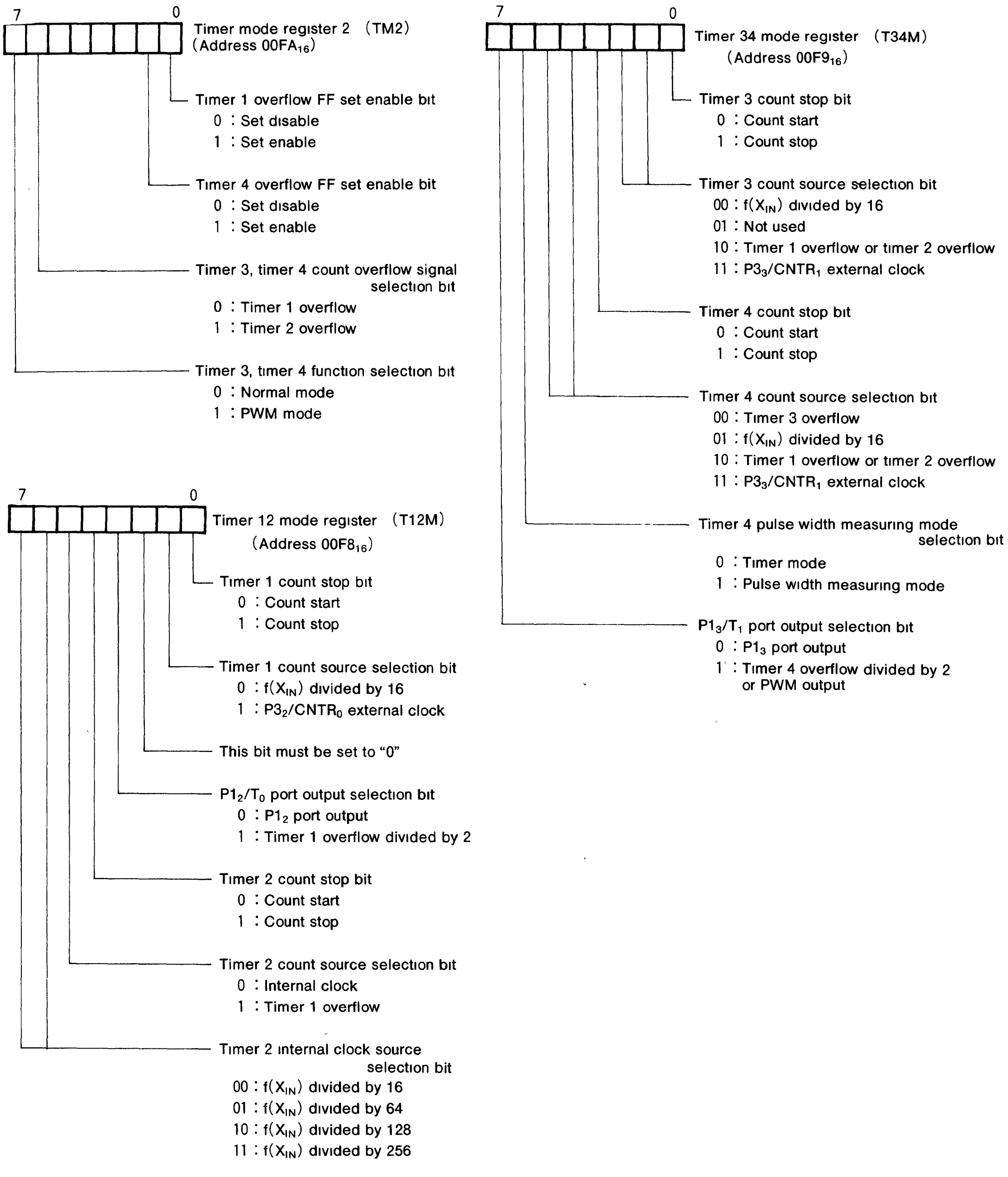


Fig. 7 Structure of timer mode registers

SERIAL I/O

The block diagram of serial I/O is shown in Figure 8. In the serial I/O mode, the receive ready signal ($\overline{S_{RDY}}$) synchronous input/output clock (CLK), and the serial I/O (S_{OUT}, S_{IN}) pins are used as $P1_7$, $P1_6$, $P1_5$, and $P1_4$, respectively. The serial I/O mode register (address $00DC_{16}$) is an 8-bit register. Bit 2 of this register is used to select a synchronous clock source. When this bit is "0", an external clock from $P1_6$ is selected. When this bit is "1" an internal clock is selected.

The internal clock can be selected from among the divide by 8, divide by 16, divide by 32, divide by 512 frequency of the oscillator frequency $f(X_{IN})$. The divide ratio is selected according to bit 0 and bit 1 in the serial I/O mode register. Bits 3 and 4 decide whether parts of P1 will be used as a serial I/O or not. When bit 3 is "1", $P1_6$ becomes an I/O pin of the synchronous clock. When an internal synchronous clock is selected, the clock is output from $P1_6$. If the external synchronous clock is selected, the clock is input to $P1_6$. And $P1_5$ will be a serial output. To use $P1_4$ as a serial input, set the directional register bit which corresponds to $P1_4$, to "0". For more information on the directional register, refer to the I/O pin section.

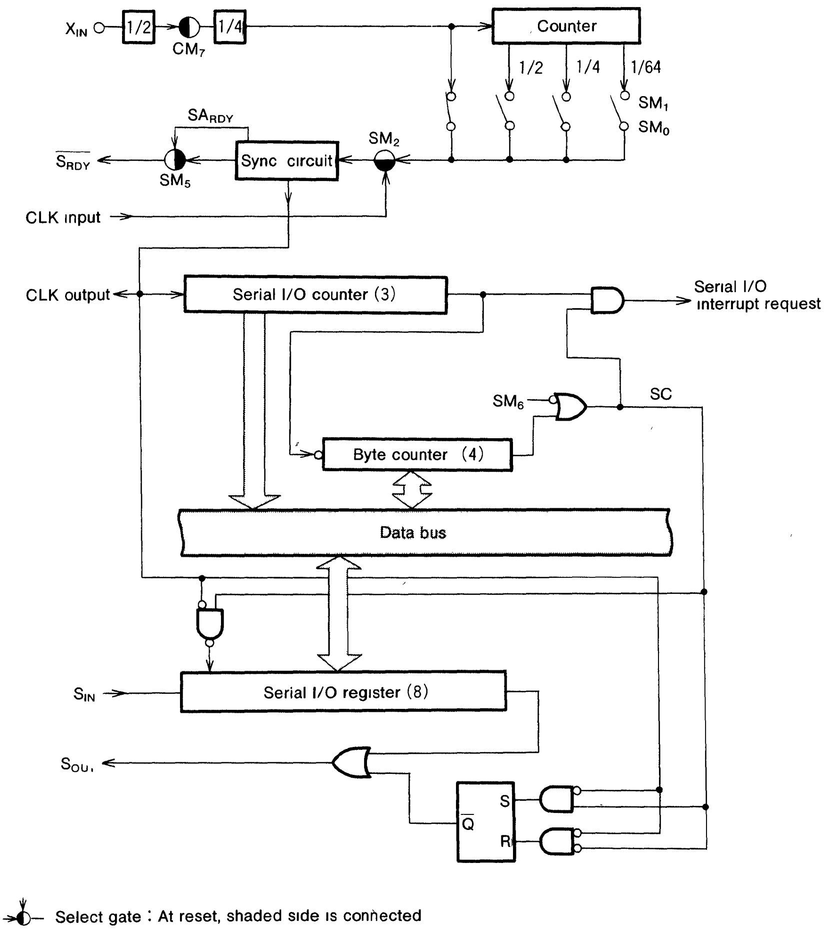


Fig. 8 Block diagram of serial I/O

Bit 4 determines if $P1_7$ is used as an output pin for the receive ready signal (bit 4="1", $\overline{S_{RDY}}$) or used as a normal I/O pin (bit 4="0").

When the $P1_7$ pin is used as the $\overline{S_{RDY}}$ output pin, output signal can be selected between $\overline{S_{RDY}}$ signal and SA_{RDY} signal by using bit 5 in the serial I/O mode register. The $\overline{S_{RDY}}$ signal is driven "L" by a signal written into the serial I/O register to inform that the device is ready to receive. Then, the $\overline{S_{RDY}}$ signal is driven "H" on the first falling edge of the transfer clock.

The SA_{RDY} signal is driven "H" by a signal written into the serial I/O register, and driven "L" on the last rising edge of the transfer clock.

The function of serial I/O differs depending on the clock source; external clock or internal clock.

Internal Clock—The serial I/O counter is set to 7 when data is stored in the serial I/O register. At each falling edge of the transfer clock, serial data is output to $P1_5$. During the rising edge of this clock, data can be input from $P1_4$ and the data in the serial I/O register will be shifted 1 bit. Data is output starting with the LSB. After the transfer clock has counted 8 times, the serial I/O register will be empty and the transfer clock will remain at a high level. At this time the interrupt request bit will be set.

External Clock—If an external clock is used, the interrupt request bit will be set after the transfer clock has counted 8 times but the transfer clock will not stop. Due to this reason, the external clock must be controlled from the outside.

Timing diagrams are shown in Figure 9.

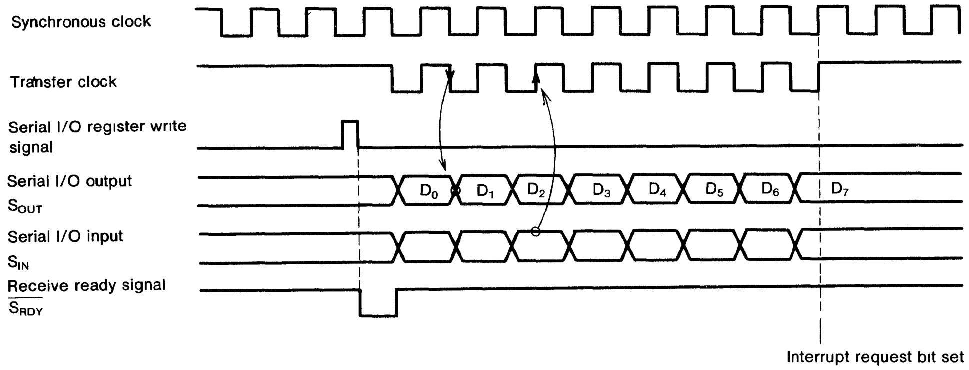


Fig. 9 Serial I/O timing

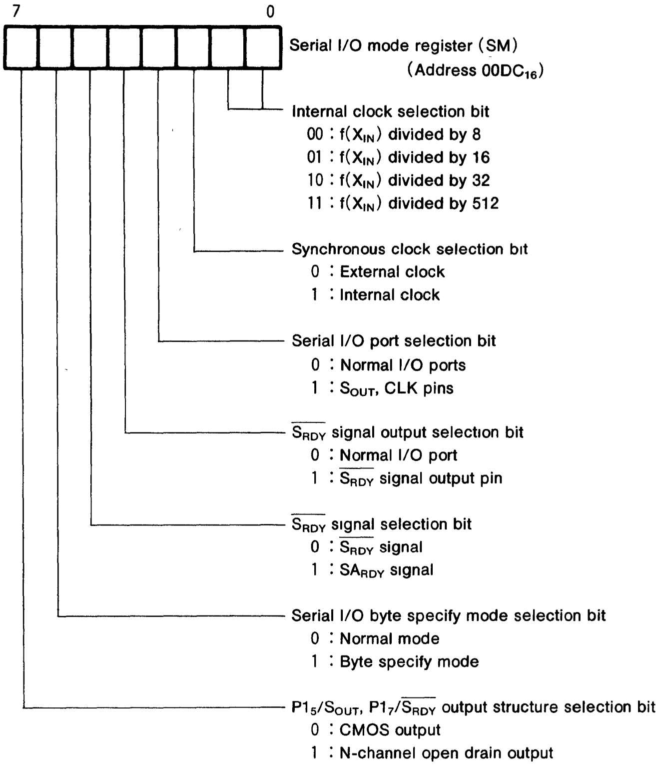


Fig. 10 Structure of serial I/O mode register

BYTE SPECIFY MODE

The serial I/O has a byte specify mode that allows one specific byte data to be selected tor transmission or reception when serial I/O circuits of two or more microcomputers are connected to send or receive data through one bus. The data to be sent or received can be specified by writing a value into the byte counter. The value written in the byte counter is decremented by one each time eight cycles of transfer clock are input. When the value in the byte counter becomes "0", serial transmission/reception is done by the next eight cycles of transfer clock. When the value in the byte counter is not "0", the output on the S_{OUT} pin is driven "H" by the falling edge of the first transfer clock pulse to inhibit transmission/reception.

Serial I/O interrupt requests are generated only when serial transmission/reception is done after the value in the byte counter is decremented to "0". When the SA_{RDY} signal output is selected, the SA_{RDY} signal is driven "L" by the last rising edge of the transfer clock after the value in the byte counter is decremented to "0".

Note that in the byte mode, an external clock must be used as the sync. clock for the purpose of the mode.

A-D CONVERTER

The A-D conversion uses an 8-bit successive comparison method. Figure 11 shows a block diagram of the A-D conversion circuit. Conversion is automatically carried out once started by the program.

There are four analog input pins which are shared with $P2_0$ to $P2_3$ of port P2. Which analog inputs are to be A-D converted is specified by using bit 2 to bit 0 in the A-D control register (address $00D9_{16}$). Pins for inputs to be A-D converted must be set for input by setting the directional register bit to "0". Bit 3 in the A-D control register is a A-D conversion end bit. This is "0" during A-D conversion; it is set to "1" when the conversion is terminated. Therefore, it is possible to know whether A-D conversion is terminated by checking this bit. Bit 4 in the A-D control register is a V_{REF} connection selection bit. During A-D conversion, this bit must be set "1" for the ladder resistor and V_{REF} pin to be connected; after the A-D conversion is terminated, this bit can be reset to "0" to separate the ladder resistor from the V_{REF} pin. In this way, power consumption in the ladder resistor can be suppressed while no A-D conversion is performed. Figure 13 shows the relationship between the contents of A-D control register and the selected input pins.

The A-D conversion register (address $00DA_{16}$) contains information on the results of conversion, so that it is possible to know the results of conversion by reading the contents of this register.

The following explains the procedure to execute A-D conversion. First, set values to bit 2 to bit 0 in the A-D control register to select the pins that you want to execute A-D conversion. Next, clear the A-D conversion terminate bit to "0". When the above is done, A-D conversion is initiated. The A-D conversion is completed after an elapse of 50 machine cycles (25μs when $f(X_{IN})=4MHz$), the A-D conversion end bit is set to "1", and the interrupt request bit is set to "1". The results of conversion are contained in the A-D conversion register.

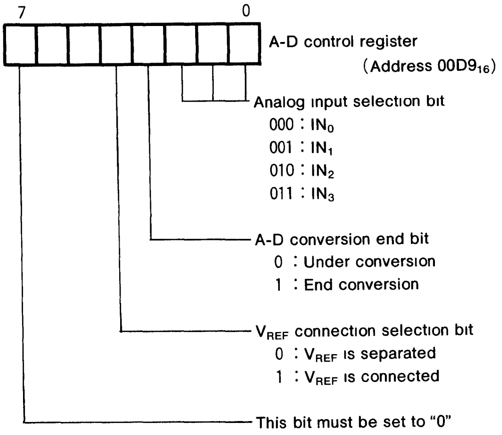


Fig. 12 Structure of A-D control register

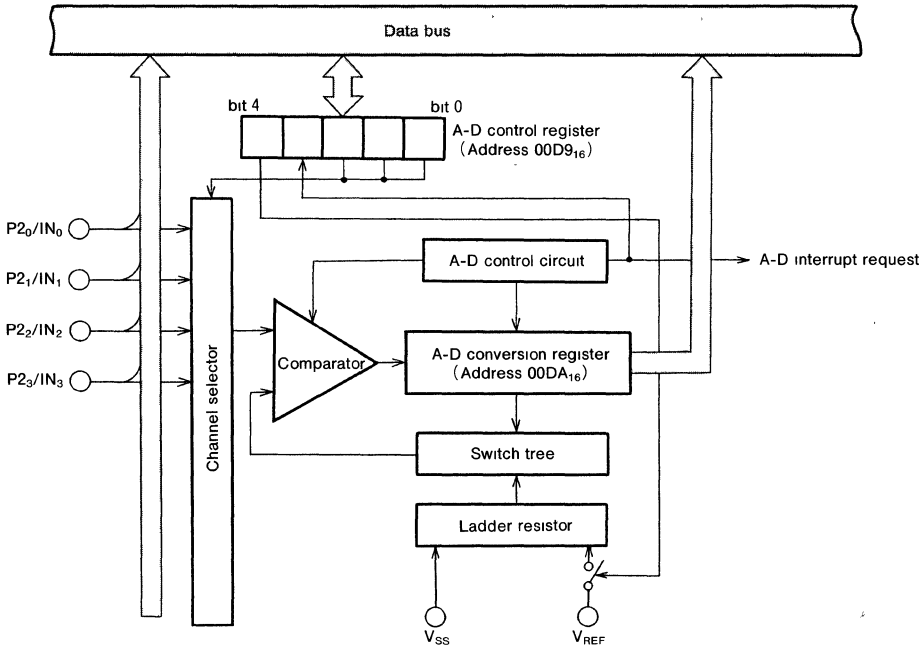


Fig. 11 A-D converter circuit

KEY ON WAKE UP

"Key on wake up" is one way of returning from a power down state caused by the STP or WIT instruction. If any terminal of port P0 has a "L" level applied, after bit 5 of the edge polarity selection register (EG_5) is set to "1", an interrupt is generated and the microcomputer is returned to the normal operating state. A key matrix can be connected to port P0 and the microcomputer can be returned to a normal state by pushing any key.

The key on wake up interrupt is common with the $\overline{INT_1}$ interrupt. When EG_5 is set to "1", the key on wake up function is selected. However, key on wake up cannot be used in the normal operating state. When the microcomputer is in the normal operating state, both key on wake up and $\overline{INT_1}$ are invalid.

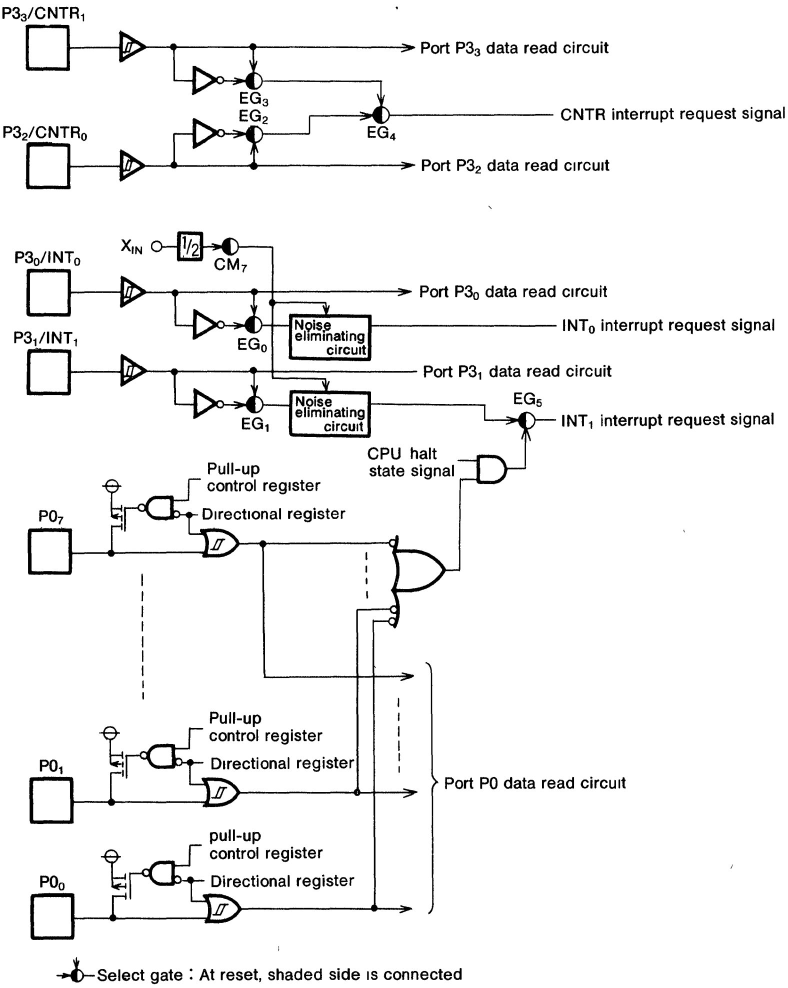


Fig. 13 Block diagram of interrupt input and key on wake up circuit

RESET CIRCUIT

The M37470M2-XXXSP is reset according to the sequence shown in Figure 15. It starts the program from the address formed by using the content of address $FFFF_{16}$ as the high order address and the content of the address $FFFE_{16}$ as the low order address, when the $\overline{RESET}$ pin is held at "L" level for no less than 2μs while the power voltage is in the recommended operating condition and then returned to "H" level.

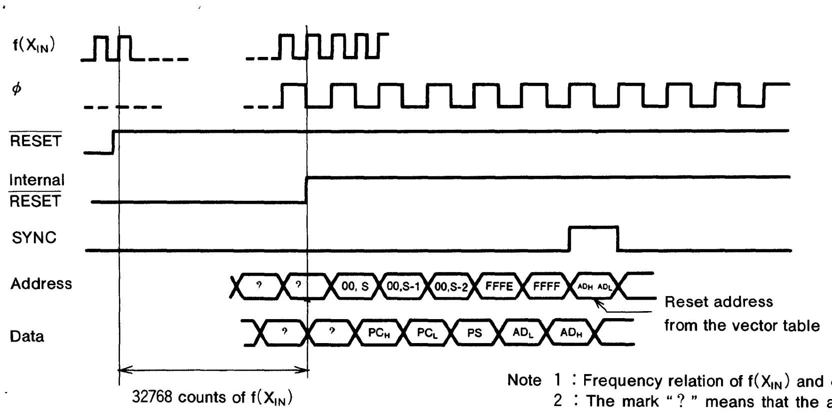
The internal initializations following reset are shown in Figure 14.

Immediately after reset, timer 3 and timer 4 are connected, and $f(X_{IN})$ divided by 16 are counted. At this time, FF_{16} is set to timer 3, and 07_{16} is set to timer 4. The reset is cleared when timer 4 overflows.

		Address								
(1)Port P0 directional register		($C1_{16}$)···	00_{16}							
(2)Port P1 directional register		($C3_{16}$)···	00_{16}							
(3)Port P2 directional register		($C5_{16}$)···					0	0	0	0
(4)Port P4 directional register		($C9_{16}$)···							0	0
(5)P0 pull-up control register		($D0_{16}$)···	00_{16}							
(6)P1~P4 pull-up control register		($D1_{16}$)···				0		0	0	0
(7)Edge selection register	(EG)	($D4_{16}$)···			0	0	0	0	0	0
(8)A-D control register		($D9_{16}$)···	0			0	1	0	0	0
(9)Serial I/O mode register	(SM)	(DC_{16})···	00_{16}							
(10)Timer 12 mode register	(T12M)	($F8_{16}$)···	00_{16}							
(11)Timer 34 mode register	(T34M)	($F9_{16}$)···	00_{16}							
(12)Timer mode register 2	(TM2)	(FA_{16})···	0	0					0	0
(13)CPU mode register	(CM)	(FB_{16})···	0	0	0	0		0	0	0
(14)Interrupt request register 1		(FC_{16})···	0	0			0	0	0	0
(15)Interrupt request register 2		(FD_{16})···						0	0	0
(16)Interrupt control register 1		(FE_{16})···	0	0			0	0	0	0
(17)Interrupt control register 2		(FF_{16})···						0	0	0
(18)Program counter		(PC_H)···	Contents of address $FFFF_{16}$							
		(PC_L)···	Contents of address $FFFE_{16}$							
(19)Processor status register		(PS)···						1		

Note : Since the contents of both registers other than those listed above (including timers and the serial I/O register) are undefined at reset, it is necessary to set initial values

Fig. 14 Internal state of microcomputer at reset



Note 1 : Frequency relation of $f(X_{IN})$ and ϕ is $f(X_{IN})=2 \cdot \phi$
2 : The mark " ? " means that the address is changeable depending upon the previous state

Fig. 15 Timing diagram at reset

I/O PORTS

(1) Port P0

Port P0 is an 8-bit I/O port with CMOS outputs. As shown in Figure 2, P0 can be accessed as memory through zero page address $00C0_{16}$. Port P0's directional register allows each bit to be programmed individually as input or output. The directional register (zero page address $00C1_{16}$) can be programmed as input with "0", or as output with "1". When in the output mode, the data to be output is latched to the port latch and output. When data is read from the output port, the output pin level is not read, only the latched data of the port latch is read. Therefore, a previously output value can be read correctly even though the output voltage level has been shifted up or down. Port pins set as input are in the high impedance state so the signal level can be read. When data is written into the input port, the data is latched only to the output latch and the pin still remains in the high impedance state. Following the execution of STP or WIT instruction, key matrix with port P0 can be used to generate the interrupt to bring the microcomputer back in its normal state. When this port is selected for input, pull-up transistor can be connected in units of 1-bit.

(2) Port P1

Port P1 has the same function as port P0. $P1_2 \sim P1_7$ serve dual functions, and the desired function can be selected by the program. When this port is selected for input, pull-up transistor can be connected in units of 4-bit.

(3) Port P2

Port P2 is an 4-bit I/O port and has basically the same functions as port P0. This port can also be used as an analog voltage input pin. When this port is selected for input, pull-up transistor can be connected in units of 4-bit.

(4) Port P3

Port P3 is an 4-bit input port.

(5) Port P4

Port P4 is an 2-bit I/O port and has basically the same functions as port P0. When this port is selected for input, pull-up transistor can be connected in units of 2-bit.

(6) INT_0 pin ($P3_0/INT_0$ pin)

This is an interrupt input pin, and is shared with port $P3_0$. When a "H" to "L" or a "L" to "H" transition input is applied to this pin, the INT_0 interrupt request bit (bit 0 of address $00FD_{16}$) is set to "1".

(7) INT_1 pin ($P3_1/INT_1$ pin)

This is an interrupt input pin, and is shared with port $P3_1$. When a "H" to "L" or a "L" to "H" transition input is applied to this pin, the INT_1 interrupt request bit (bit 1 of address $00FD_{16}$) is set to "1".

(8) Counter input $CNTR_0$ pin ($P3_2/CNTR_0$ pin)

This is a timer input pin, and is shared with port $P3_2$. When this pin is selected to $CNTR_0$ or $CNTR_1$ interrupt input pin and a "H" to "L" or a "L" to "H" transition input is applied to this pin, the $CNTR_0$ or $CNTR_1$ interrupt request bit (bit 2 of address $00FD_{16}$) is set to "1".

(9) Counter input $CNTR_1$ pin ($P3_3/CNTR_1$ pin)

This is a timer input pin, and is shared with port $P3_3$. When this pin is selected to $CNTR_0$ or $CNTR_1$ interrupt input pin and a "H" to "L" or a "L" to "H" transition input is applied to this pin, the $CNTR_0$ or $CNTR_1$ interrupt request bit (bit 2 of address $00FD_{16}$) is set to "1".

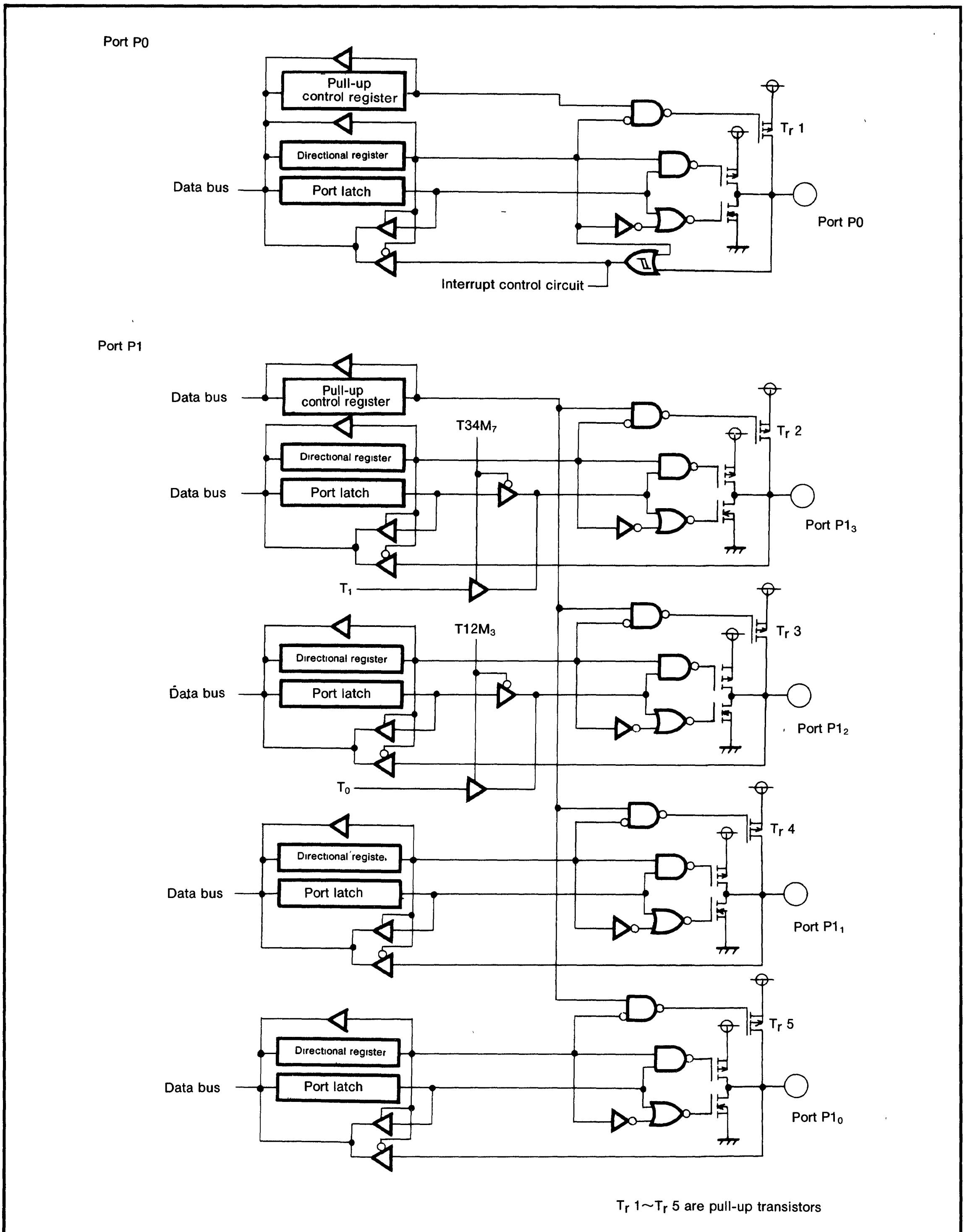


Fig. 16 Block diagram of ports P0~P1

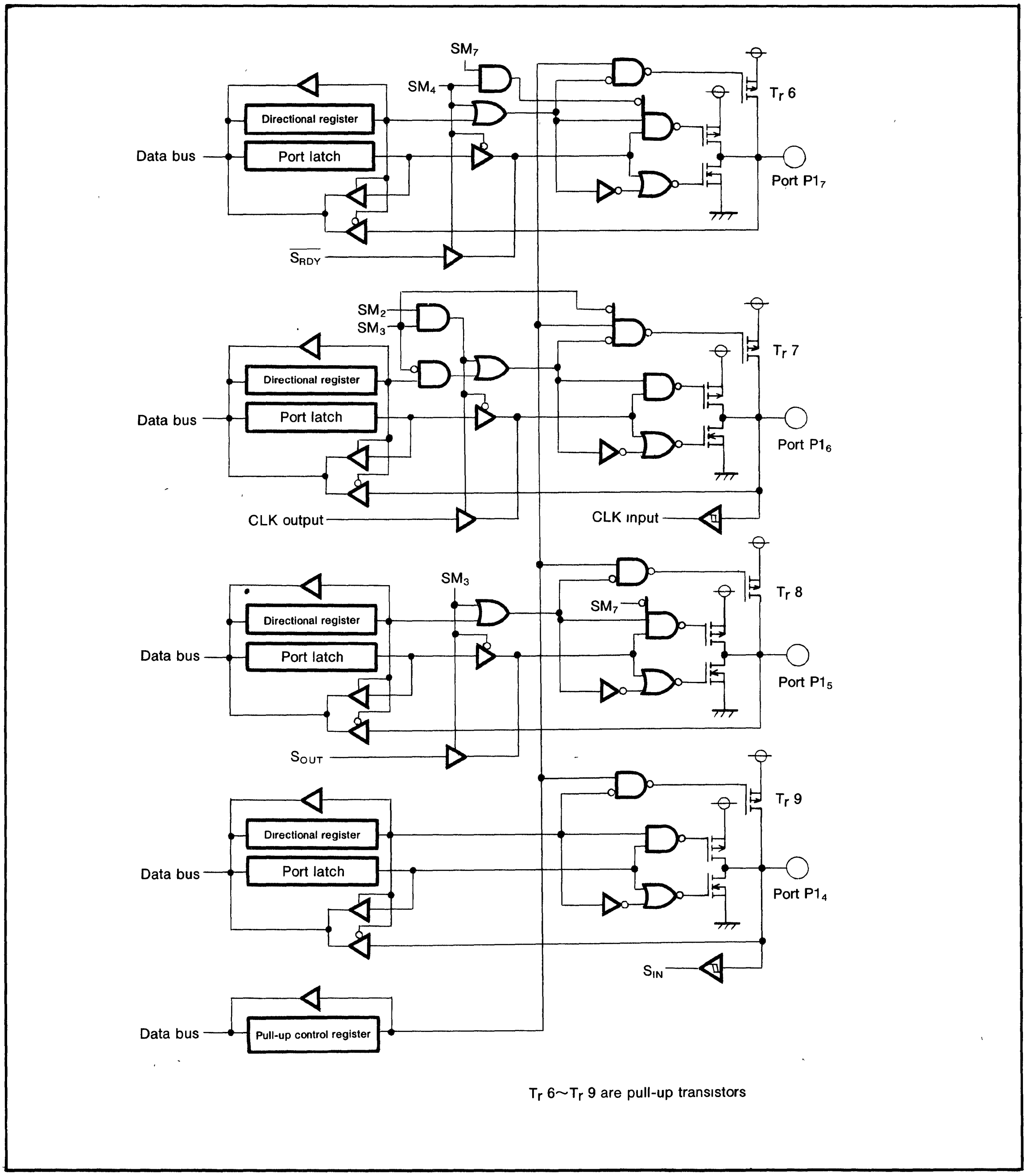


Fig. 17 Block diagram of port P1

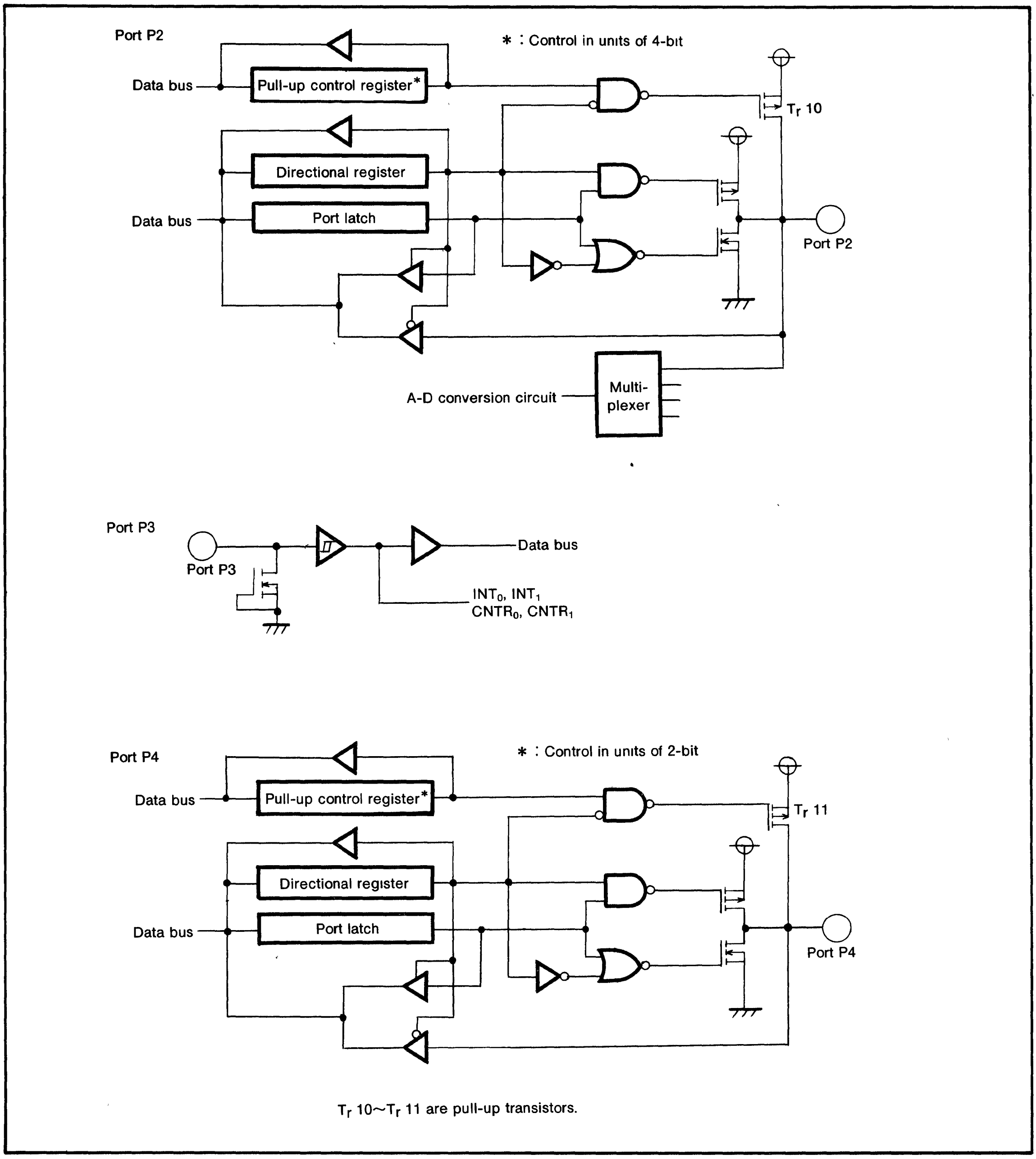


Fig. 18 Block diagram of ports P2~P4

CLOCK GENERATING CIRCUIT

The built-in clock generating circuits are shown in Figure 21.

When an STP instruction is executed, the internal clock ϕ stops oscillating at "H" level. At the same time, FF_{16} is set in the timer 3, 07_{16} is set in the timer 4.

The oscillator is restarted when an interrupt is accepted. However, the clock ϕ keeps its "H" level until timer 4 overflows.

This is because the oscillator needs a set-up period if a ceramic or a quartz crystal oscillator is used.

When the WIT instruction is executed, the clock ϕ stops in the "H" level but the oscillator continues running. This wait state is cleared when an interrupt is accepted. Since the oscillation does not stop, the next instructions are executed at once.

To return from the stop or the wait status, the interrupt enable bit must be set to "1" before executing STP or WIT instruction. Especially, to return from the stop status, the timer 3, timer 4 count stop bit must be set to "0" before executing STP instruction.

The circuit example using a ceramic oscillator (or a quartz crystal oscillator) is shown in Figure 19.

The constant capacitance will differ depending on which oscillator is used, and should be set to the manufactures suggested value.

The example of external clock usage is shown in Figure 20 X_{IN} is the input, and X_{OUT} is open.

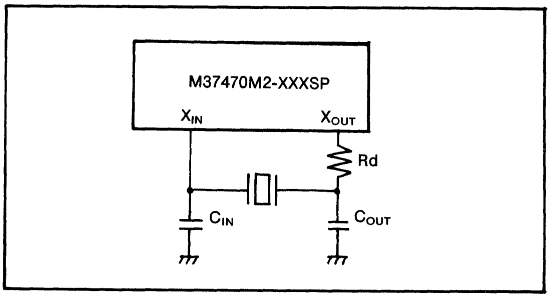


Fig. 19 Example of ceramic resonator circuit

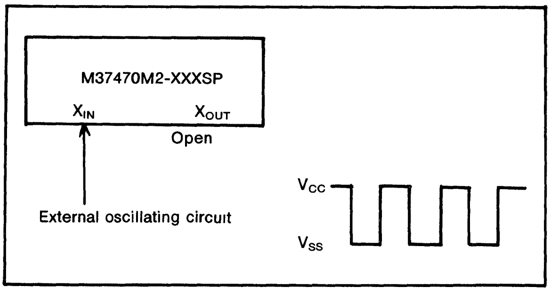


Fig. 20 External clock input circuit

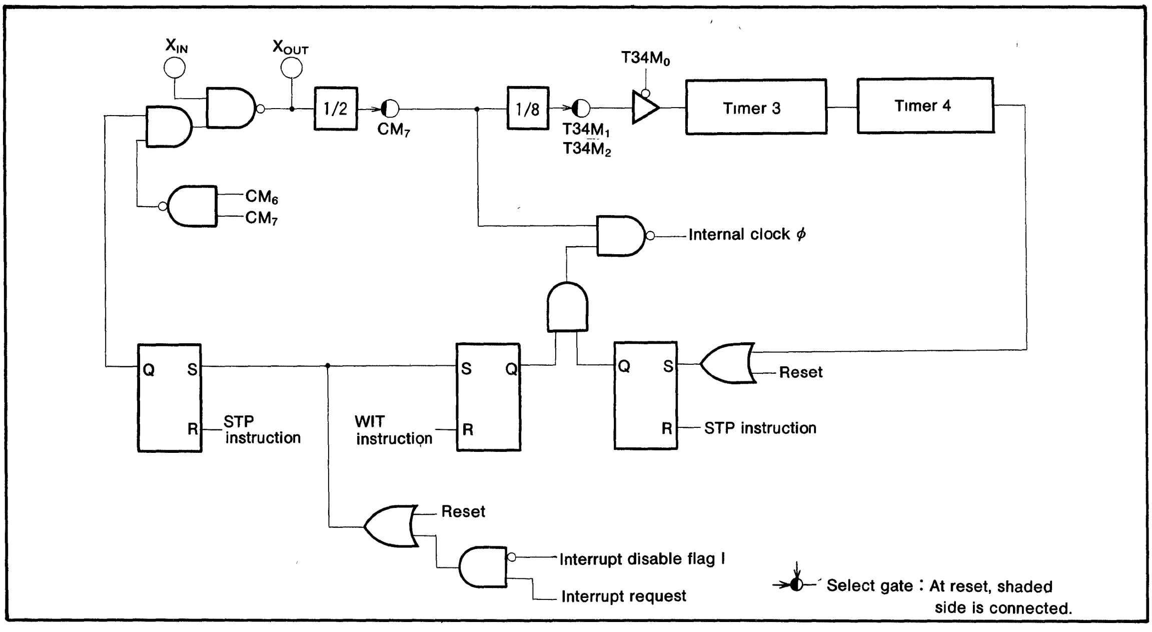


Fig. 21 Block diagram of clock generating circuit

PROGRAMMING NOTES

(1) The frequency ratio of the timer is 1/(n+1).
(2) Even though the BBC and BBS instructions are executed after the interrupt request bits are modified (by the program), those instructions are only valid for the contents before the modification. Also, at least one instruction cycle must be used (such as a NOP) between the modification of the interrupt request bits and the execution of the BBC and BBS instructions.
(3) After the ADC and SBC instructions are executed (in decimal mode), one instruction cycle (such as a NOP) is needed before the SEC, CLC, or CLD instructions are executed.
(4) A NOP instruction must be used after the execution of a PLP instruction.
(5) During A-D conversion, don't use STP instruction.

DATA REQUIRED FOR MASK ORDERING

Please send the following data for mask orders.
(1) mask ROM confirmation form
(2) mask specification form
(3) ROM data ·· EPROM 3 sets

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS} Output transistors are at "OFF" state	$-0.3 \sim 7$	V
V_I	Input voltage X_{IN}		$-0.3 \sim V_{CC}+0.3$	V
V_I	Input voltage $P0_0 \sim P0_7$, $P1_0 \sim P1_7$, $P2_0 \sim P2_3$, $P3_0 \sim P3_3$, $P4_0 \sim P4_1$, V_{REF}, $\overline{RESET}$		$-0.3 \sim V_{CC}+0.3$	V
V_O	Output voltage $P0_0 \sim P0_7$, $P1_0 \sim P1_7$, $P2_0 \sim P2_3$, $P4_0 \sim P4_1$, X_{OUT}		$-0.3 \sim V_{CC}+0.3$	V
P_d	Power dissipation	$T_a = 25$℃	1000	mW
Topr	Operating temperature		$-20 \sim 85$	℃
Tstg	Storage temperature		$-40 \sim 150$	℃

RECOMMENDED OPERATING CONDITIONS

($V_{CC}=2.7 \sim 5.5$V, $V_{SS}=0$V, $T_a=-20 \sim 85$℃ unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	2.7	5	5.5	V
V_{SS}	Supply voltage		0		V
V_{IH}	"H" Input voltage $P0_0 \sim P0_7$, $P1_0 \sim P1_7$, $P3_0 \sim P3_3$, $\overline{RESET}$, X_{IN}	$0.8V_{CC}$		V_{CC}	V
V_{IH}	"H" Input voltage $P2_0 \sim P2_3$, $P4_0 \sim P4_1$	$0.7V_{CC}$		V_{CC}	V
V_{IL}	"L" Input voltage $P0_0 \sim P0_7$, $P1_0 \sim P1_7$, $P3_0 \sim P3_3$	0		$0.2V_{CC}$	V
V_{IL}	"L" Input voltage $P2_0 \sim P2_3$, $P4_0 \sim P4_1$	0		$0.25V_{CC}$	V
V_{IL}	"L" Input voltage $\overline{RESET}$	0		$0.12V_{CC}$	V
V_{IL}	"L" Input voltage X_{IN}	0		$0.16V_{CC}$	V
I_{OH}(sum)	"H" sum output current $P0_0 \sim P0_7$, $P4_0 \sim P4_1$			−30	mA
I_{OH}(sum)	"H" sum output current $P1_0 \sim P1_7$, $P2_0 \sim P2_3$			−30	mA
I_{OL}(sum)	"L" sum output current $P0_0 \sim P0_7$, $P4_0 \sim P4_1$			60	mA
I_{OL}(sum)	"L" sum output current $P1_0 \sim P1_7$, $P2_0 \sim P2_3$			60	mA
I_{OL}(peak)	"L" peak output current $P0_0 \sim P0_7$, $P1_0 \sim P1_7$, $P2_0 \sim P2_3$, $P4_0 \sim P4_1$			20	mA
I_{OL}(avg)	"L" average output current $P0_0 \sim P0_7$, $P1_0 \sim P1_7$, $P2_0 \sim P2_3$, $P4_0 \sim P4_1$ (Note 2)			10	mA
I_{OH}(peak)	"H" peak output current $P0_0 \sim P0_7$, $P1_0 \sim P1_7$, $P2_0 \sim P2_3$, $P4_0 \sim P4_1$			−10	mA
I_{OH}(avg)	"H" average output current $P0_0 \sim P0_7$, $P1_0 \sim P1_7$, $P2_0 \sim P2_3$, $P4_0 \sim P4_1$ (Note 2)			−5	mA
f(CNTR)	Timer input frequency $CNTR_0$ ($P3_2$), $CNTR_1$ ($P3_3$) (Note 1)			1	MHz
f(CLK)	Serial I/O clock input frequency CLK ($P1_6$) (Note 1)			1	MHz
f(X_{IN})	Clock oscillating frequency (Note 1)			4	MHz

Note 1 : Oscillation frequency is at 50% duty cycle.
2 : The average output current I_{OH} (avg) and I_{OL} (avg) are the average value during a 100ms.

ELECTRICAL CHARACTERISTICS (V_{CC}=2.7~5.5V, V_{SS}=0V, T_a=−20~85℃, unless otherwise noted)

Symbol	Parameter	Test Conditions		Limits			Unit
				Min	Typ.	Max.	
V_{OH}	"H" output voltage $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_3$, $P4_0$, $P4_1$	V_{CC}=5V, I_{OH}=−5mA		3			V
		V_{CC}=3V, I_{OH}=−1.5mA		2			
V_{OL}	"L" output voltage $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_3$, $P4_0$, $P4_1$	V_{CC}=5V, I_{OL}=10mA				2	V
		V_{CC}=3V, I_{OL}=3mA				1	
$V_{T+}-V_{T-}$	Hysteresis $P0_0$~$P0_7$, $P3_0$~$P3_3$	V_{CC}=5V			0.5		V
		V_{CC}=3V			0.3		
$V_{T+}-V_{T-}$	Hysteresis $\overline{RESET}$	V_{CC}=5V			0.5		V
		V_{CC}=3V			0.3		
$V_{T+}-V_{T-}$	Hysteresis $P1_6$/CLK	use as CLK input	V_{CC}=5V		0.5		V
			V_{CC}=3V		0.3		
I_{IL}	"L" input current $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P3_0$~$P3_2$, $P4_0$, $P4_1$	V_I=0V,	V_{CC}=5V			−5	μA
		not use pull-up transistor	V_{CC}=3V			−3	
		V_I=0V,	V_{CC}=5V	−0.25	−0.5	−1.0	mA
		use pull-up transistor	V_{CC}=3V	−0.08	−0.18	−0.35	
I_{IL}	"L" input current $P3_3$	V_I=0V	V_{CC}=5V			−5	μA
			V_{CC}=3V			−3	
I_{IL}	"L" input current $P2_0$~$P2_3$	V_I=0V, not use as analog input,	V_{CC}=5V			−5	μA
		not use pull-up transistor	V_{CC}=3V			−3	
		V_I=0V, not use as analog input,	V_{CC}=5V	−0.25	−0.5	−1.0	mA
		use pull-up transistor	V_{CC}=3V	−0.08	−0.18	−0.35	
I_{IL}	"L" input current $\overline{RESET}$, X_{IN}	V_I=0V	V_{CC}=5V			−5	μA
		(X_{IN} is at stop mode)	V_{CC}=3V			−3	
I_{IH}	"H" input current $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P3_0$~$P3_2$, $P4_0$, $P4_1$	V_I=V_{CC},	V_{CC}=5V			5	μA
		not use pull-up transistor	V_{CC}=3V			3	
I_{IH}	"H" input current $P3_3$	V_I=V_{CC}	V_{CC}=5V			5	μA
			V_{CC}=3V			3	
I_{IH}	"H" input current $P2_0$~$P2_3$	V_I=V_{CC}, not use as analog input,	V_{CC}=5V			5	μA
		not use pull-up transistor	V_{CC}=3V			3	
I_{IH}	"H" input current $\overline{RESET}$, X_{IN}	V_I=V_{CC},	V_{CC}=5V			5	μA
		(X_{IN} is at stop mode)	V_{CC}=3V			3	
I_{CC}	Supply current	At normal operation, A-D conversion is not executed X_{IN}=4MHz	V_{CC}=5V		3.5	7	mA
			V_{CC}=3V		1.8	3.6	
		At normal operation, A-D conversion is executed X_{IN}=4MHz	V_{CC}=5V		4	8	
			V_{CC}=3V		2	4	
		At wait mode,	V_{CC}=5V		1	2	
		X_{IN}=4MHz	V_{CC}=3V		0.5	1	
		Stop all oscillation	T_a=25℃		0.1	1	μA
		V_{CC}=5V	T_a=85℃		1	10	
V_{RAM}	RAM retention voltage	Stop all oscillation		2			V

A-D CONVERTER CHARACTERISTICS (V_{CC}=2.7~5.5V, V_{SS}=0V, T_a=−20~85℃, f(X_{IN})=4MHz, unless otherwise noted)

Symbol	Parameter	Test Conditions	Limits			Unit
			Min.	Typ	Max.	
—	Resolution				8	bits
—	Non-linearity error				±2	LSB
—	Differential non-linearity error				±0.9	LSB
V_{OT}	Zero transition error	V_{CC}=V_{REF}=5.12V, $I_{OL(sum)}$=0mA			2	LSB
		V_{CC}=V_{REF}=3.072V, $I_{OL(sum)}$=0mA			3	
V_{FST}	Full-scale transition error	V_{CC}=V_{REF}=5.12V			4	LSB
		V_{CC}=V_{REF}=3.072V			7	
t_{CONV}	Conversion time				25	μs
V_{VREF}	Reference input voltage		0.5V_{CC}		V_{CC}	V
R_{LADDER}	Ladder resistance value		2	5	10	kΩ
V_{IA}	Analog input voltage		0		V_{REF}	V

MITSUBISHI MICROCOMPUTERS

M37471M2-XXXSP/FP,M37471M4-XXXSP/FP M37471M8-XXXSP/FP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

DESCRIPTION

The M37471M2-XXXSP/FP is a single-chip microcomputer designed with CMOS silicon gate technology. It is housed in a 42-pin shrink plastic molded DIP or a 56-pin plastic molded QFP. This single-chip microcomputer is useful for business equipment and other consumer applications.

In addition to its simple instruction set, the ROM, RAM, and I/O addresses are placed on the same memory map to enable easy programming.

The differences among M37471M2-XXXSP/FP, M37471M4-XXXSP/FP and M37471M8-XXXSP/FP are noted below. The following explanations apply to the M37471M2-XXXSP/FP. Specificaiton variations for other chips are noted accordingly.

Type name	ROM size	RAM size
M37471M2-XXXSP/FP	4096 bytes	128 bytes
M37471M4-XXXSP/FP	8192 bytes	192 bytes
M37471M8-XXXSP/FP	16384 bytes	384 bytes

The differences between the M37471M2-XXXSP and the M37471M2-XXXFP are the package outline and the power dissipation ability (absolute maximum ratings).

FEATURES

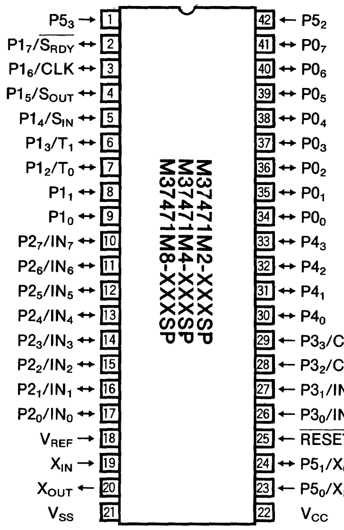
- Number of basic instructions ········ 69
- Memory size
  - ROM ········ 4096 bytes (M37471M2)
  - RAM ········ 128 bytes (M37471M2)
- Instruction execution time
  - ········ 1μs (minimum instructions at 4MHz frequency)
- Single power supply ········ 2.7~5.5V
- Power dissipation normal operation mode
  - ········ 17.5mW (at 4MHz frequency)
- Subroutine nesting ········ 64 levels max. (M37471M2)
- Interrupt ········ 12types, 10vectors
- 8-bit timer ········ 4
- Programmable I/O ports
  - (Ports P0, P1, P2, P4) ········ 28
- Input ports (Ports P3, P5) ········ 8
- Serial I/O (8-bit) ········ 1
- A-D converter ········ 8-bit, 8channel

APPLICATION

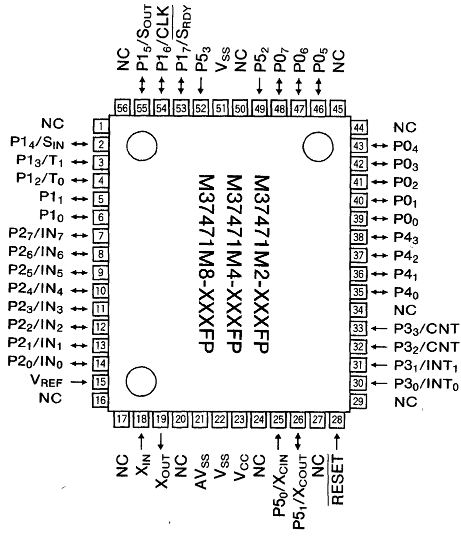
Audio-visual equipment, VCR, Tuner

Office automation equipment

PIN CONFIGURATION (TOP VIEW)



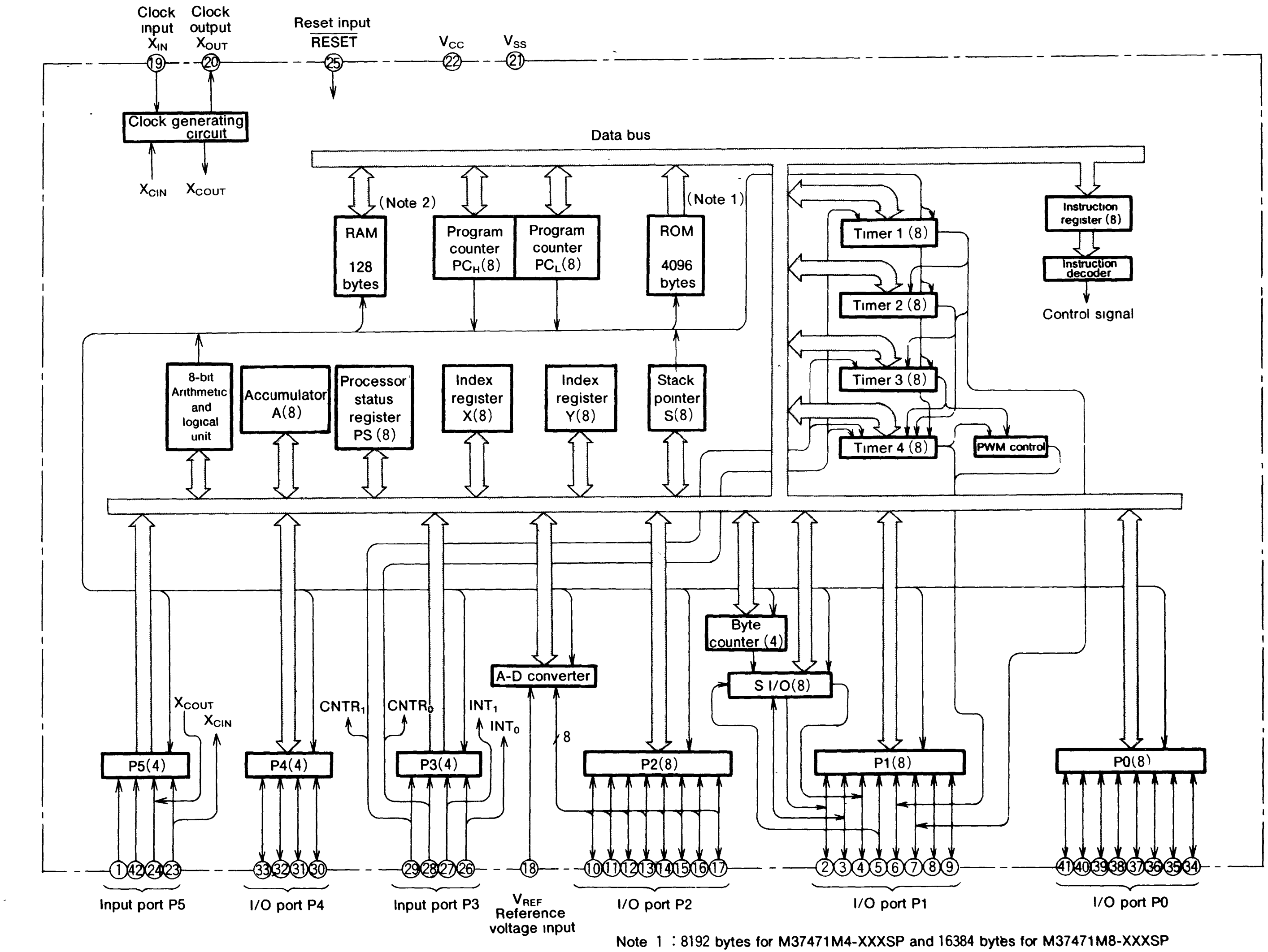
Outline 42P4B



Outline 56P6N

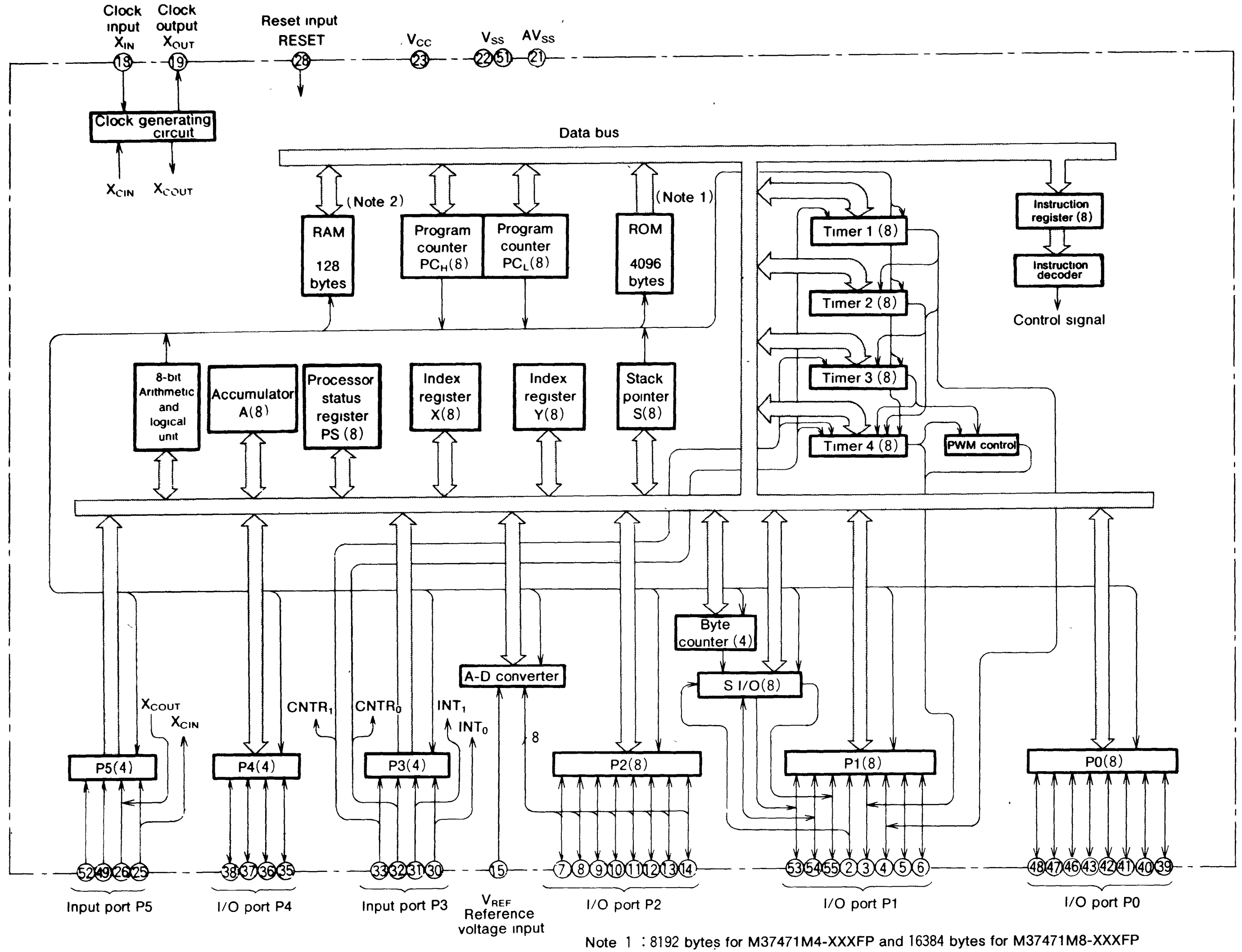
NC : No connection

M37471M2-XXXSP BLOCK DIAGRAM



Note 1 : 8192 bytes for M37471M4-XXXSP and 16384 bytes for M37471M8-XXXSP
2 : 192 bytes for M37471M4-XXXSP and 384 bytes for M37471M8-XXXSP

M37471M2-XXXFP BLOCK DIAGRAM



Note 1 : 8192 bytes for M37471M4-XXXFP and 16384 bytes for M37471M8-XXXFP
2 : 192 bytes for M37471M4-XXXFP and 384 bytes for M37471M8-XXXFP

FUNCTIONS OF M37471M2-XXXSP/FP, M37471M4-XXXSP/FP, M37471M8-XXXSP/FP

Parameter			Functions
Number of basic instructions			69
Instruction execution time			1μs (minimum instructions, at 4MHz frequency)
Clock frequency			4MHz (max)
Memory size	M37471M2-XXXSP/FP	ROM	4096 bytes
		RAM	128 bytes
	M37471M4-XXXSP/FP	ROM	8192 bytes
		RAM	192 bytes
	M37471M8-XXXSP/FP	ROM	16384 bytes
		RAM	384 bytes
Input/Output port	P0, P1, P2	I/O	8-bit×3
	P3, P5	Input	4-bit×2
	P4	I/O	4-bit×1
Serial I/O			8-bit×1
Timers			8-bit timer×4
A-D converter			8-bit×1 (8 channels)
Subroutine nesting	M37471M2-XXXSP/FP		64 (max)
	M37471M4-XXXSP/FP		96 (max)
	M37471M8-XXXSP/FP		192 (max)
Interrupt			5 external interrupts, 6 internal interrupts, 1 software interrupt
Clock generating circuit			Two built-in circuit with internal feedback resistor (ceramic or quartz crystal oscillator)
Supply voltage			2.7~5.5V
Power dissipation			17.5mW (at 4MHz frequency)
Input/Output characters	Input/Output voltage		5V
	Output current		−5~10mA (P0, P1, P2, P4 : CMOS tri-states)
Operating temperature range			−20~85℃
Device structure			CMOS silicon gate
Package	M37471M2/M4/M8-XXXSP		42-pin shrink plastic molded DIP
	M37471M2/M4/M8-XXXFP		56-pin plastic molded QFP

PIN DESCRIPTION

Pin	Name	Input/ Output	Functions
V_{CC}, V_{SS}	Supply voltage		Power supply inputs 2. 7~5. 5V to V_{CC}, and 0V to V_{SS}
AV_{SS}	Analog power supply		Ground level input pin for A-D converter Same voltage as V_{SS} is applied. This pin is for 56-pin type only.
$\overline{\text{RESET}}$	Reset input	Input	To enter the reset state, the reset input pin must be kept at a "L" for more than 2μs (under normal V_{CC} conditions).
X_{IN}	Clock input	Input	These are I/O pins of internal clock generating circuit for main clock. To control generating frequency, an external ceramic or a quartz crystal oscillator is connected between the X_{IN} and X_{OUT} pins. If an external clock is used, the clock source should be connected the X_{IN} pin and the X_{OUT} pin should be left open Feedback resistor is connected between X_{IN} and X_{OUT}
X_{OUT}	Clock output	Output	
V_{REF}	Reference voltage input	Input	This is reference voltage input pin for the A-D converters
$P0_0$~$P0_7$	I/O port P0	I/O	Port P0 is an 8-bit I/O port The output structure is CMOS output When this port is selected for input, pull-up transistor can be connected in units of 1-bit and a key on wake up function is provided
$P1_0$~$P1_7$	I/O port P1	I/O	Port P1 is an 8-bit I/O port The output structure is CMOS output When this port is selected for input, pull-up transistor can be connected in units of 4-bit $P1_2$, $P1_3$ are in common with timer output pins T_0, T_1 $P1_4$, $P1_5$, $P1_6$, $P1_7$ are in common with serial I/O pins S_{IN}, S_{OUT}, CLK, $\overline{S_{RDY}}$, respectively The output structure of S_{OUT} and $\overline{S_{RDY}}$ can be changed to N-channel open drain output
$P2_0$~$P2_7$	I/O port P2	I/O	Port P2 is an 8-bit I/O port The output structure is CMOS output When this port is selected for input, pull-up transistor can be connected in units of 4-bit This port is in common with analog input pins IN_0~IN_7
$P3_0$~$P3_3$	Input port P3	Input	Port P3 is an 4-bit input port $P3_0$, $P3_1$ are in common with external interrupt input pins INT_0, INT_1 and $P3_2$, $P3_3$ are in common with timer input pins $CNTR_0$, $CNTR_1$
$P4_0$~$P4_3$	I/O port P4	I/O	Port P4 is an 4-bit I/O port The output structure is CMOS output When this port is selected for input, pull-up transistor can be connected in units of 4-bit.
$P5_0$~$P5_3$	Input port P5	Input	Port P5 is an 4-bit input port and pull-up transistor can be connected in units of 4-bit $P5_0$, $P5_1$ are in common with input/output pins of clock for clock function X_{CIN}, X_{COUT}. When $P5_0$, $P5_1$ are used as X_{CIN}, X_{COUT}, connect a ceramic or a quartz crystal oscillator between X_{CIN} and X_{COUT} If an external clock input is used, connect the clock input to the X_{CIN} pin and open the X_{COUT} pin Feedback resistor is connected between X_{CIN} and X_{COUT} pins

FUNCTIONAL DESCRIPTION

Central Processing Unit (CPU)

The M37471 microcomputers use the standard MELPS 740 instruction set. For details of instruction operations, refer to the MELPS 740 CPU core basic functions, or the MELPS 740 Programming Manual.

Machine-resident instructions are as follows:
The FST and SLW instructions are not provided.
The MUL and DIV instructions are not provided.
The WIT instruction can be used.
The STP instruction can be used.

CPU Mode Register

The CPU mode register is allocated to address $00FB_{16}$. This register has a stack page selection bit.

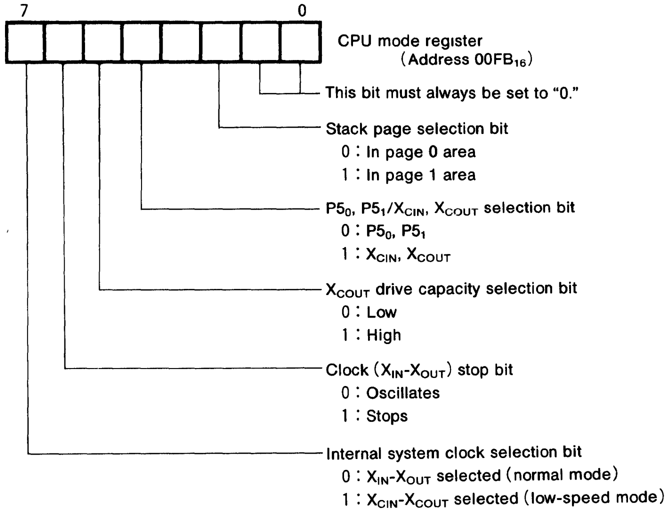


Fig. 1 Structure of CPU mode register

MEMORY

- **Special Function Register (SFR) Area**

The special function register (SFR) area contains the registers relating to functions such as I/O ports and timers.

- **RAM**

RAM is used for data storage as well as a stack area.

- **ROM**

ROM is used for storing user programs as well as the interrupt vector area.

- **Interrupt Vector Area**

The interrupt vector area is for storing jump destination addresses used at reset or when an interrupt is generated.

- **Zero Page**

Zero page addressing mode is useful because it enables access to this area with fewer instruction cycles.

- **Special Page**

Special page addressing mode is useful because it enables access to this area with fewer instruction cycles.

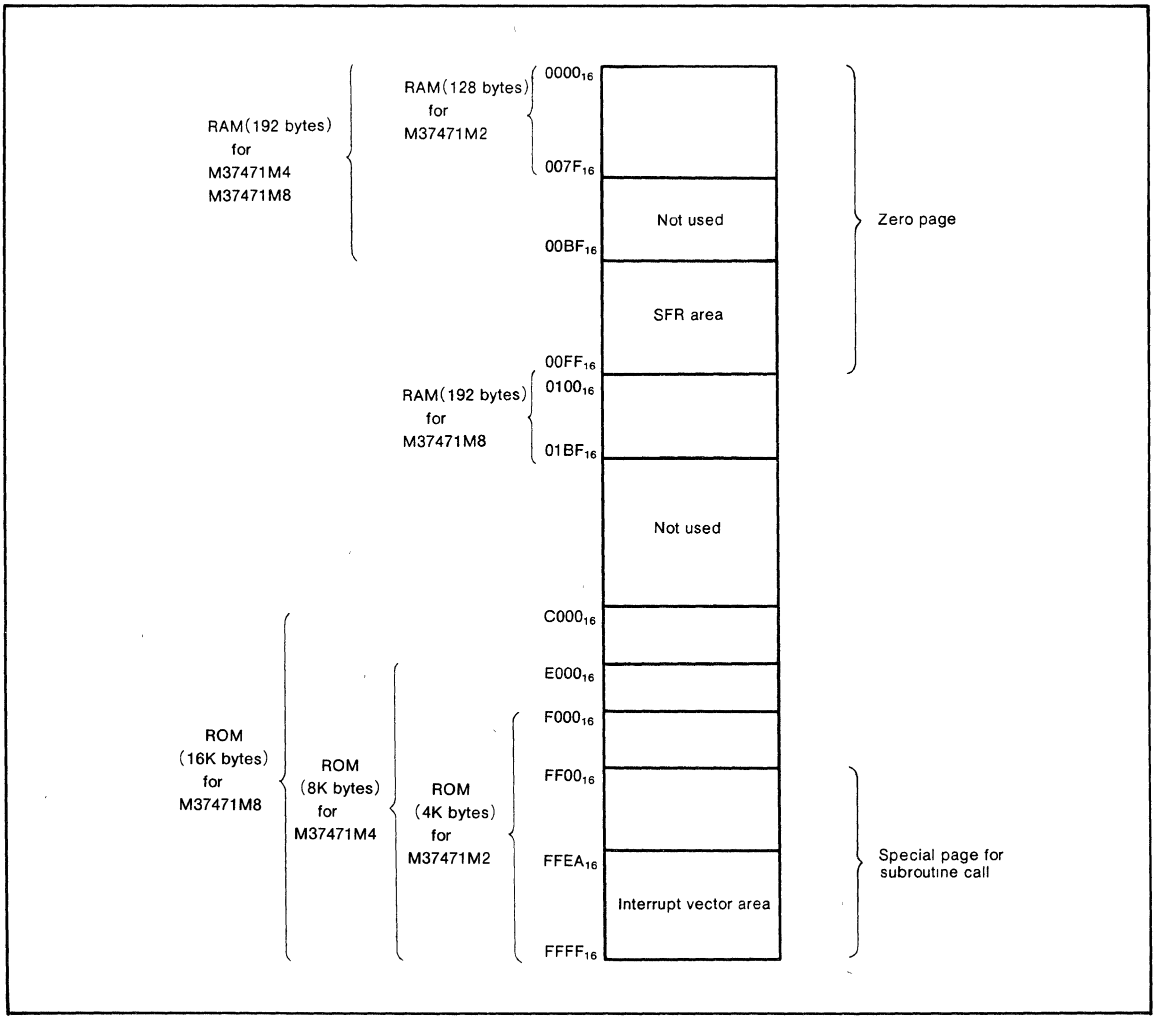


Fig. 2 Memory map

$00C0_{16}$	Port P0		$00E0_{16}$	
$00C1_{16}$	Port P0 directional register		$00E1_{16}$	
$00C2_{16}$	Port P1		$00E2_{16}$	
$00C3_{16}$	Port P1 directional register		$00E3_{16}$	
$00C4_{16}$	Port P2		$00E4_{16}$	
$00C5_{16}$	Port P2 directional register		$00E5_{16}$	
$00C6_{16}$	Port P3		$00E6_{16}$	
$00C7_{16}$			$00E7_{16}$	
$00C8_{16}$	Port P4		$00E8_{16}$	
$00C9_{16}$	Port P4 directional register		$00E9_{16}$	
$00CA_{16}$	Port P5		$00EA_{16}$	
$00CB_{16}$			$00EB_{16}$	
$00CC_{16}$			$00EC_{16}$	
$00CD_{16}$			$00ED_{16}$	
$00CE_{16}$			$00EE_{16}$	
$00CF_{16}$			$00EF_{16}$	
$00D0_{16}$	P0 pull-up control register		$00F0_{16}$	Timer 1
$00D1_{16}$	P1~P5 pull-up control register		$00F1_{16}$	Timer 2
$00D2_{16}$			$00F2_{16}$	Timer 3
$00D3_{16}$			$00F3_{16}$	Timer 4
$00D4_{16}$	Edge polarity selection register		$00F4_{16}$	
$00D5_{16}$			$00F5_{16}$	
$00D6_{16}$	Input latch register		$00F6_{16}$	
$00D7_{16}$			$00F7_{16}$	Timer FF register
$00D8_{16}$			$00F8_{16}$	Timer 12 mode register
$00D9_{16}$	A-D control register		$00F9_{16}$	Timer 34 mode register
$00DA_{16}$	A-D conversion register		$00FA_{16}$	Timer mode register 2
$00DB_{16}$			$00FB_{16}$	CPU mode register
$00DC_{16}$	Serial I/O mode register		$00FC_{16}$	Interrupt request register 1
$00DD_{16}$	Serial I/O register		$00FD_{16}$	Interrupt request register 2
$00DE_{16}$	Serial I/O counter	Byte counter	$00FE_{16}$	Interrupt control register 1
$00DF_{16}$			$00FF_{16}$	Interrupt control register 2

Fig. 3 SFR (Special Function Register) memory map

INTERRUPTS

Interrupts can be caused by 12 different events consisting of five external, six internal, and one software events.

Interrupts are vectored interrupts with priorities shown in Table 1. Reset is also included in the table because its operation is similar to an interrupt.

When an interrupt is accepted, the registers are pushed, interrupt disable flag I is set, and the program jumps to the address specified in the vector table. The interrupt request flag is cleared automatically. The reset and BRK instruction interrupt can never be inhibited. Other interrupts are disabled when the interrupt inhibit flag is set.

All interrupts except the BRK instruction interrupt have an interrupt request bit and an interrupt enable bit. The interrupt request bits are in interrupt request registers 1 and 2 and the interrupt enable bits are in interrupt control registers 1 and 2. External interrupts INT_0 and INT_1 can be asserted on either the falling or rising edge as set in the edge polarity selection register. When "0" is set to this register, the interrupt is activated on the falling edge; when "1" is set to the register, the interrupt is activated on the rising edge.

When the device is put into power-down state by the STP instruction or the WIT instruction, if bit 5 in the edge polarity selection register is "1", the INT_1 interrupt becomes a key on wake up interrupt. When a key on wake up interrupt is valide, an interrupt request is generated by applying the "L" level to any pin in port P0. In this case, the port used for interrupt must have been set for the input mode.

If bit 5 in the edge polarity selection register is "0" when the device is in power-down state, the INT_1 interrupt is selected. Also, if bit 5 in the edge polarity selection register is set to "1" when the device is not in a power-down state, neither key on wake up interrupt request nor INT_1 interrupt request are generated.

The $CNTR_0$/$CNTR_1$ interrupts function in the same as INT_0 and INT_1. The interrupt input pin can be specified for either $CNTR_0$ or $CNTR_1$ pin by setting bit 4 in the edge polarity selection register.

Figure 4 shows the structure of the edge polarity selection register, interrupt request registers 1 and 2, and interrupt control registers 1 and 2.

Interrupts other than the BRK instruction interrupt and reset are accepted when the interrupt enable bit is "1", interrupt request bit is "1", and the interrupt disable flag is "0". The interrupt request bit can be reset with a program, but not set. The interrupt enable bit can be set and reset with a program.

Reset is treated as a non-maskable interrupt with the highest priority. Figure 5 shows interrupts control.

Table 1. Interrupt vector address and priority.

Event	Priority	Vector addresses	Remarks
$\overline{\text{RESET}}$	1	$FFFF_{16}$, $FFFE_{16}$	Non-maskable
INT_0 interrupt	2	$FFFD_{16}$, $FFFC_{16}$	External interrupt (phase programmable)
INT_1 interrupt or key on wake up interrupt	3	$FFFB_{16}$, $FFFA_{16}$	External interrupt (INT_1 is phase programmable)
$CNTR_0$ interrupt or $CNTR_1$ interrupt	4	$FFF9_{16}$, $FFF8_{16}$	External interrupt (phase programmable)
Timer 1 interrupt	5	$FFF7_{16}$, $FFF6_{16}$	
Timer 2 interrupt	6	$FFF5_{16}$, $FFF4_{16}$	
Timer 3 interrupt	7	$FFF3_{16}$, $FFF2_{16}$	
Timer 4 interrupt	8	$FFF1_{16}$, $FFF0_{16}$	
Serial I/O interrupt	9	$FFEF_{16}$, $FFEE_{16}$	
A-D conversion completion interrupt	10	$FFED_{16}$, $FFEC_{16}$	
BRK instruction interrupt	11	$FFEB_{16}$, $FFEA_{16}$	Non-maskable software interrupt

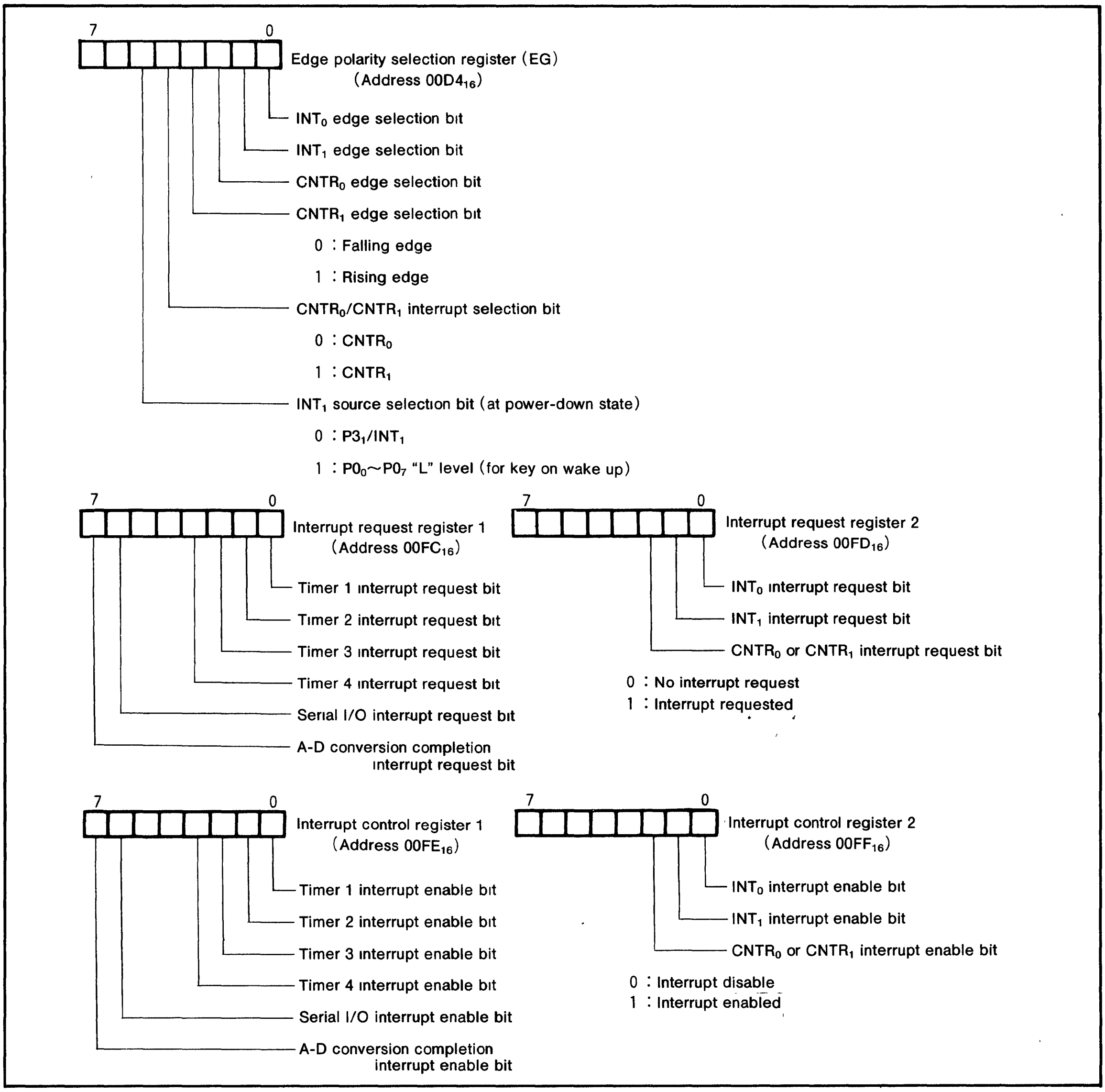


Fig. 4 Structure of registers related to interrupt

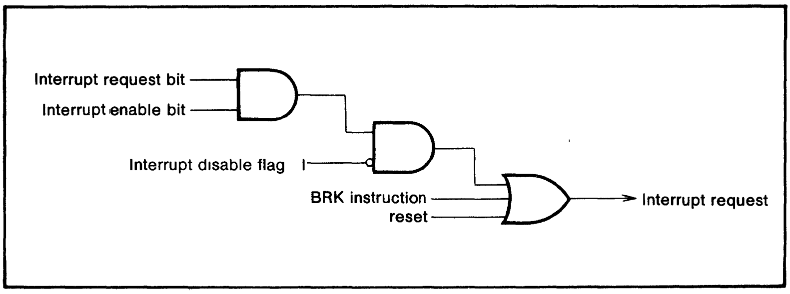


Fig. 5 Interrupt control

TIMER

The M37471M2-XXXSP/FP has four timers; timer 1, timer 2, timer 3 and timer 4.

A block diagram of timer 1 through 4 is shown in Figure 6.

Timer 1 can be operated in the timer mode, event count mode, or pulse output mode. Timer 1 starts counting when bit 0 in the timer 12 mode register (address $00F8_{16}$) is set to "0".

The count source can be selected from the $f(X_{IN})$ divided by 16, $f(X_{CIN})$ divided by 16, $f(X_{CIN})$, or event input from $P3_2/CNTR_0$ pin. When bit 1 and bit 2 in the timer 12 mode register are "0", $f(X_{IN})$ divided by 16 or $f(X_{CIN})$ divided by 16 is selected. Selection between $f(X_{IN})$ and $f(X_{CIN})$ is done by bit 7 in the CPU mode register (address $00FB_{16}$). When bit 1 in the timer 12 mode register is "0" and bit 2 is "1", $f(X_{CIN})$ is selected. And, when bit 1 in the timer 12 mode register is "1", an event input from the $CNTR_0$ pin is selected. Event inputs are selected depending on bit 2 in the edge polarity selection register (address $00D4_{16}$) . When this bit is "0", the inverted value of $CNTR_0$ input is selected; when the bit is "1", $CNTR_0$ input is selected.

When bit 3 in the timer 12 mode register is set to "1", the $P1_2$ pin becomes timer output T_0. When the direction register of $P1_2$ is set for the output mode at this time, the timer 1 overflow divided by 2 is output from T_0. The initial output value can be set by writing the value to bit 0 in the timer FF register (address $00F7_{16}$) after setting "1" to bit 0 in timer mode register 2.

Timer 2 can only be operated in the timer mode. Timer 2 starts counting when bit 4 in the timer 12 mode register is set to "0".

The count source can be selected from the divide by 16, divide by 64, divide by 128, or divide by 256 frequency of $f(X_{IN})$ or $f(X_{CIN})$, and timer 1 overflow. When bit 5 in the timer 12 mode register is "0", any of the divide by 16, divide by 64, divide by 128, or divide by 256 frequency of $f(X_{IN})$ or (X_{CIN}) is selected. The divide ratio is selected according to bit 6 and bit 7 in the timer 12 mode register, and selection between $f(X_{IN})$ and $f(X_{CIN})$ is made according to bit 7 in the CPU made register. When bit 5 in the timer 12 mode register is "1", timer 1 overflow is selected as the count source.

Timer 3 can be operated in the timer mode, event count mode, or PWM mode. Timer 3 starts counting when bit 0 in the timer 34 mode register (address $00F9_{16}$) is set to "0".

The count source can be selected from the $f(X_{IN})$ divided by 16, $f(X_{CIN})$ divided by 16, $f(X_{CIN})$, timer 1 or timer 2 overflow, or an event input from $P3_3/CNTR_1$ pins according to the statuses of bit 1 and bit 2 in the timer 34 mode register, bit 6 in the timer mode register 2 (address $00FA_{16}$) and bit 7 in the CPU mode register. Note, however, that if timer 1 overflow or timer 2 overflow is selected for the count source of timer 3 when timer 1 overflow is selected for the count source of timer 2, timer 1 overflow is always selected regardless of the status of bit 6 in the timer mode register 2. Event inputs are selected depending on bit 3 in the edge polarity selection register. When this bit is "0", the inverted value of $CNTR_1$ input is selected; when the bit is "1", $CNTR_1$ input is selected.

Timer 4 can be operated in the timer mode, event count mode, pulse output mode, pulse width measuring mode, or PWM mode. Timer 4 starts counting when bit 3 in the timer 34 mode register is set to "0" when bit 6 in this register is "0". When bit 6 is "1", the pulse width measuring mode is selected. The count source can be selected from timer 3 overflow, $f(X_{IN})$ divided by 16, $f(X_{CIN})$ divided by 16, $f(X_{CIN})$, timer 1 or timer 2 overflow, or an event input from $P3_3/CNTR_1$ pins according to the statuses of bit 4 and bit 5 in the timer 34 mode register, bit 6 in the timer mode register 2, and bit 7 in the CPU mode register. Note, however, that if timer 1 overflow or timer 2 overflow is selected for the count source of timer 4 when timer 1 overflow is selected for the count source of timer 2, timer 1 overflow is always selected regardless of the status of bit 6 in the timer mode register 2. Event inputs are selected depending on bit 3 in the edge polarity selection register. When this bit is "0", the inverted value of $CNTR_1$ input is selected; when the bit is "1", $CNTR_1$ input is selected.

When bit 7 in the timer 34 mode register is set to "1", the $P1_3$ pin becomes timer output T_1. When the direction register of $P1_3$ is set for the output mode at this time, the timer 4 overflow divided by 2 is output from T_1 when bit 7 in the timer mode register 2 is "0". The initial output value can be set by writing the value to bit 1 in the timer FF register after setting "1" to bit 1 in timer mode register 2.

(1) Timer mode

Timer perform down count operations with the dividing ratio being $1/(n+1)$. Writing a value to the timer latch sets a value to the timer. When the value to be set to the timer latch is nn_{16}, the value to be set to a timer is nn_{16}, which is down counted at the falling edge of the count source from nn_{16} to $(nn_{16}\text{-}1)$ to $(nn_{16}\text{-}2)$ to...01_{16} to 00_{16} to FF_{16}. At the falling edge of the count source immediately after timer value has reached FF_{16}, value $(nn_{16}\text{-}1)$ obtained by subtracting one from the timer latch value is set (reloaded) to the timer to continue counting. At the rising edge of the count source immediately after the timer value has reached FF_{16}, an overflow occurs, an interrupt request.

(2) Event count mode

Timer operates in the same way as in the timer mode except that it counts input from the $CNTR_0$ or $CNTR_1$ pin.

(3) Pulse output mode

In this mode, duty 50% pulses are output from the T_0 or T_1 pin. When the timer overflows, the polarity of the T_0 or T_1 pin output level is inverted.

(4) Pulse width measuring mode

The M37471 can measure the "H" or "L" width of the $CNTR_0$ or $CNTR_1$ input waveform by using the pulse width measuring mode of timer 4. The pulse width measuring mode is selected by writing "1" to bit 6 in the timer 34 mode register. In the pulse width measuring mode, the timer counts the count source while the $CNTR_0$ or $CNTR_1$ input is "H" or "L". Whether the $CNTR_0$ input or $CNTR_1$ input be measured can be specified by the status of bit 4 in the edge polarity selection register; whether the "H" width or "L" width be measured can be specified by the status of bit 2 ($CNTR_0$) and bit 3 ($CNTR_1$) in the edge polarity selection register.

(5) PWM mode

The PWM mode can be entered for timer 3 and timer 4 by setting bit 7 in the timer mode register 2 to "1". In the PWM mode, the $P1_3$ pin is set for timer output T_1 to output PWM waveforms by setting bit 7 in the timer 34 mode register to "1". The directional register of $P1_3$ must be set for the output mode before this can be done.

In the PWM mode, timer 3 is counting and timer 4 is idle while the PWM waveform is "L". When timer 3 overflows, the PWM waveform goes "H". At this time, timer 3 stops counting simultaneously and timer 4 starts counting. When timer 4 overflows, the PWM waveform goes "L", and timer 4 stops and timer 3 starts counting again. Consequently, the "L" duration of the PWM waveform is determined by the value of timer 3; the "H" duration of the PWM waveform is determined by the value of timer 4.

When a value is written to the timer in operation during the PWM mode, the value is only written to the timer latch, and not written to the timer. In this case, if the timer overflows, a value one less the value in the timer latch is written to the timer. When any value is written to an idle timer, the value is written to both the timer latch and the timer.

In this mode, do not select timer 3 overflow as the count source for timer 4.

INPUT LATCH FUNCTION

The M37471 can latch the $P3_0/INT_0$, $P3_1/INT_1$, $P3_2/CNTR_0$, and $P3_3/CNTR_1$ pin level into the input latch register (address $00D6_{16}$) when timer 4 overflows. The polarity of each pin latched to the input latch regiser can be selected by using the edge polarity selection register. When bit 0 in the edge polarity selection register is "0", the inverted value of the $P3_0/INT_0$ pin level is latched; when the bit is "1", the $P3_0/INT_0$ pin level is latched as is. When bit 1 in the edge polarity selection register is "0", the inverted value of the $P3_1/INT_1$ pin level is latched; when the bit is "1", the $P3_1/INT_1$ pin level is latched as is. When bit 2 in the edge polarity selection register is "0", the inverted value of the $P3_2/CNTR_0$ pin level is latched; when the bit is "1", the $P3_2/CNTR_0$ pin level is latched as is. When bit 3 in the edge polarity selection register is "0", the inverted value of the $P3_3/CNTR_1$ pin level is latched; when the bit is "1", the $P3_3/CNTR_1$ pin level is latched as is.

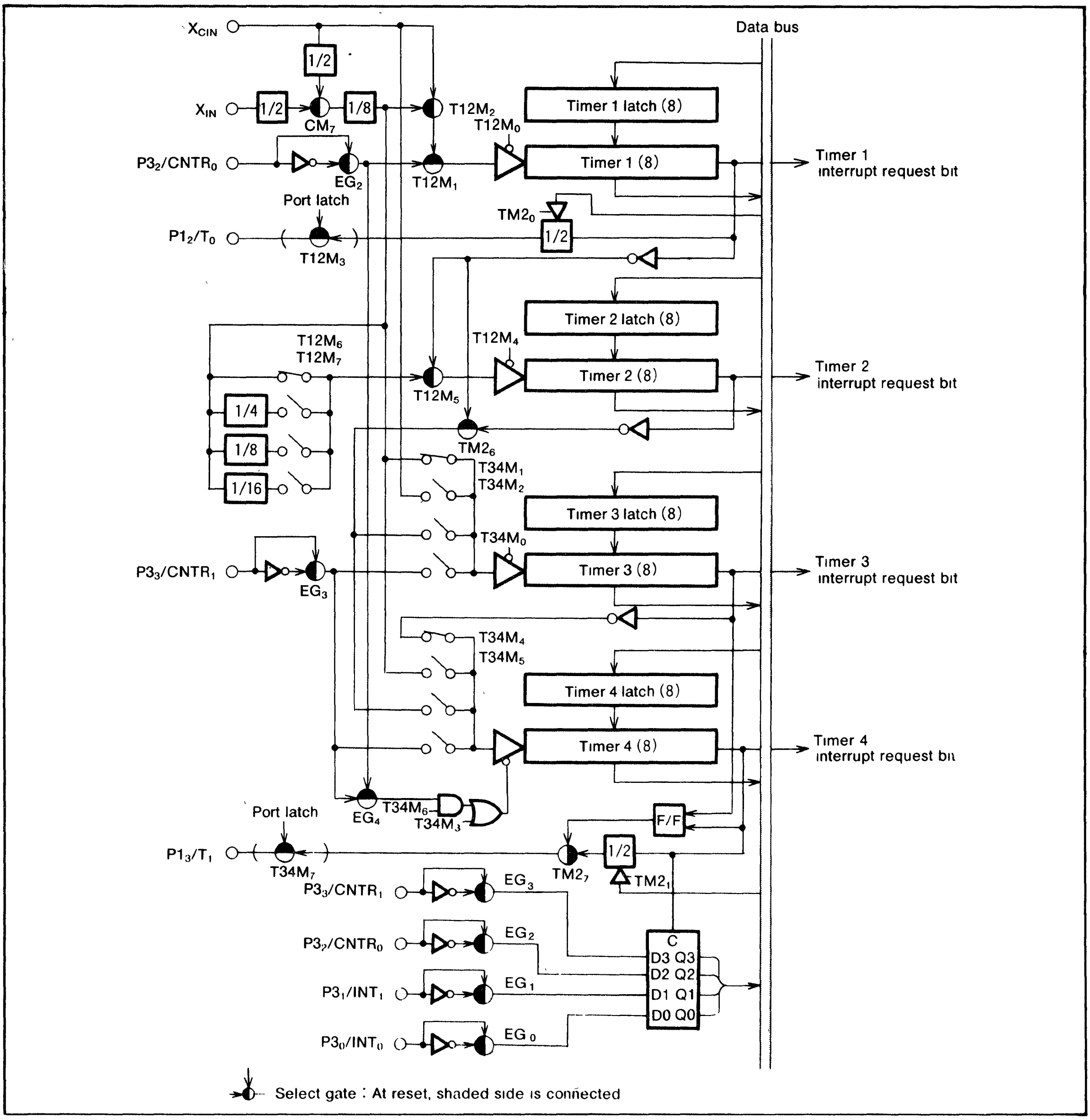


Fig. 6 Block diagram of timer 1 through 4

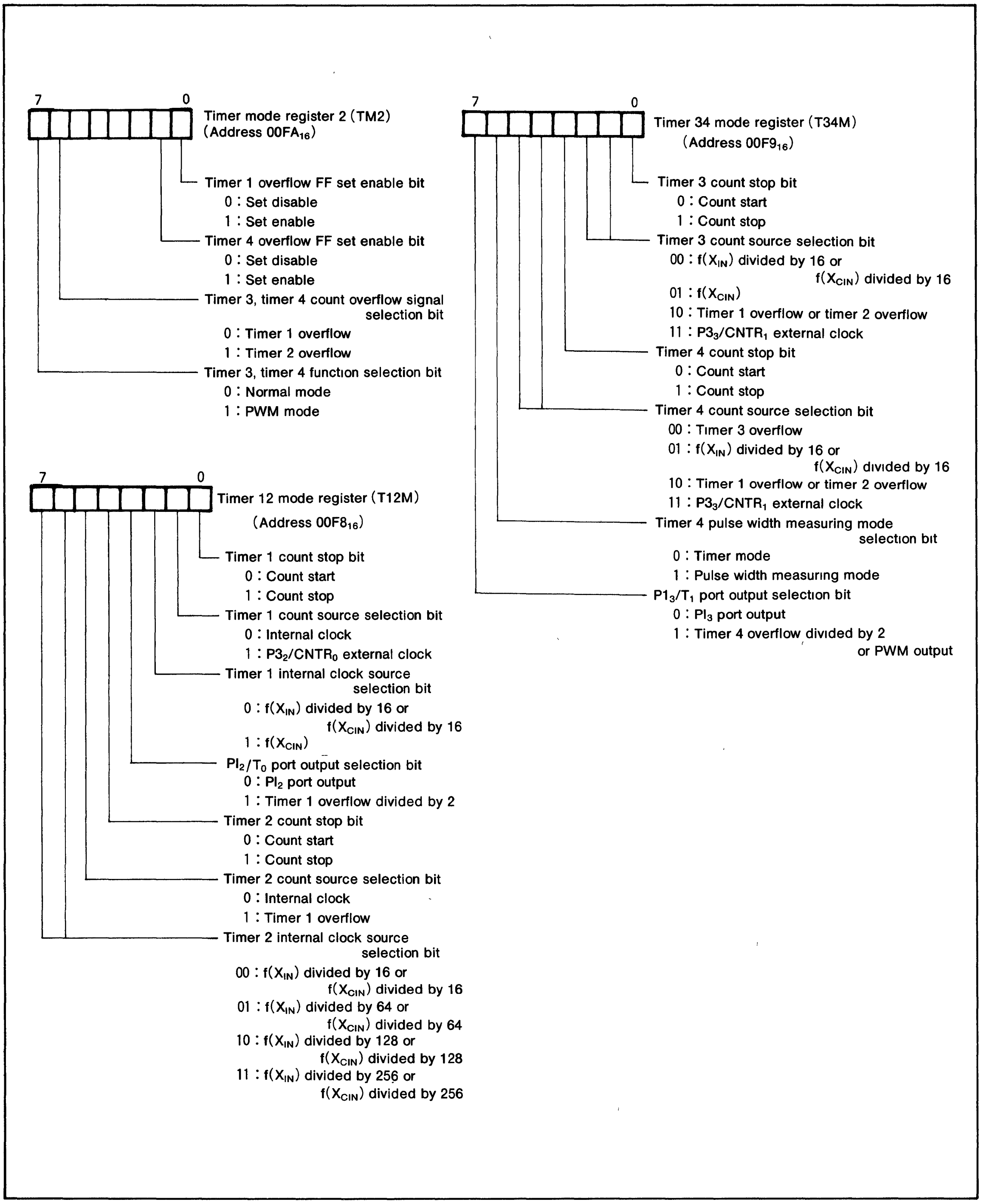


Fig. 7 Structure of timer mode registers

SERIAL I/O

The block diagram of serial I/O is shown in Figure 8. In the serial I/O mode, the receive ready signal ($\overline{S_{RDY}}$), synchronous input/output clock (CLK), and the serial I/O (S_{OUT}, S_{IN}) pins are used as $P1_7$, $P1_6$, $P1_5$, and $P1_4$, respectively. The serial I/O mode register (address $00DC_{16}$) is an 8-bit register. Bit 2 of this register is used to select a synchronous clock source. When this bit is "0", an external clock from $P1_6$ is selected. When this bit is "1", an internal clock is selected.

The internal clock can be selected from among the divide by 8, divide by 16, divide by 32, divide by 512 frequency of the oscillator frequency $f(X_{IN})$ or $f(X_{CIN})$. The divide ratio is selected according to bit 0 and bit 1 in the serial I/O mode register, and selection between $f(X_{IN})$ and $f(X_{CIN})$ is mode according to bit 7 in the CPU mode register.

Bits 3 and 4 decide whether parts of P1 will be used as a serial I/O or not. When bit 3 is "1", $P1_6$ becomes an I/O pin of the synchronous clock. When an internal synchronous clock is selected, the clock is output from $P1_6$. If the external synchronous clock is selected, the clock is input to $P1_6$. And $P1_5$ will be a serial output. To use $P1_4$ as a serial input, set the directional register bit which corresponds to $P1_4$, to "0". For more information on the directional register, refer to the I/O pin section.

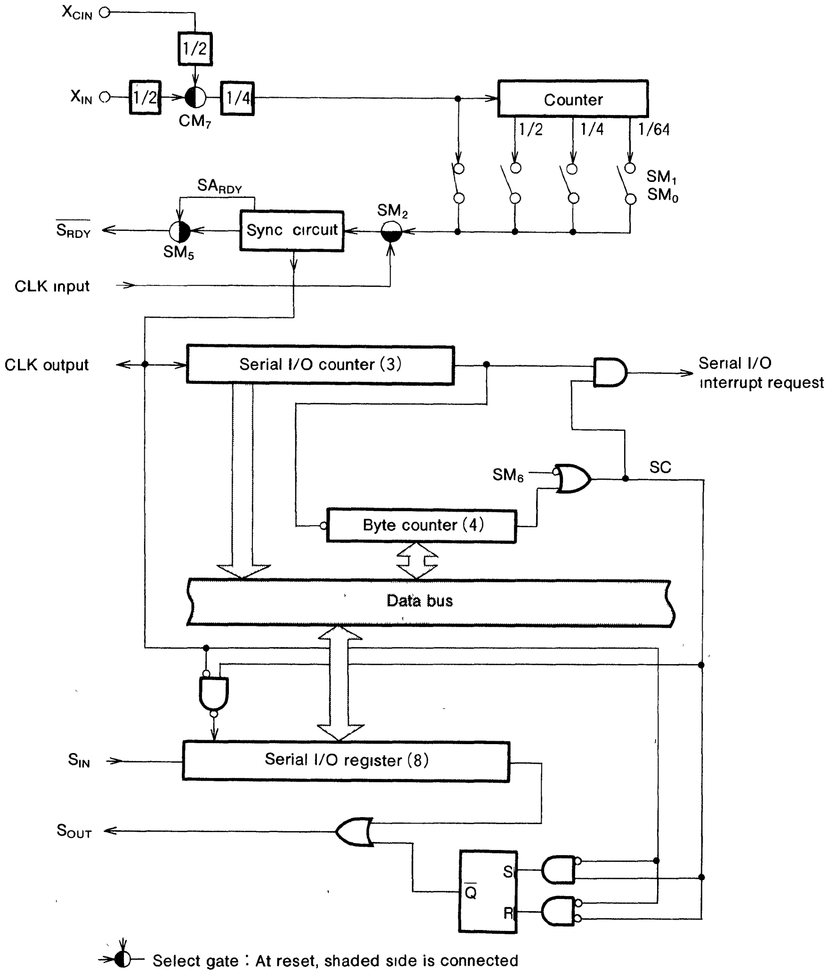


Fig. 8 Block diagram of serial I/O

Bit 4 determines if $P1_7$ is used as an output pin for the receive ready signal (bit 4="1", $\overline{S_{RDY}}$) or used as a normal I/O pin (bit 4="0").

When the $P1_7$ pin is used as the $\overline{S_{RDY}}$ output pin, output signal can be selected between $\overline{S_{RDY}}$ signal and SA_{RDY} signal by using bit 5 in the serial I/O mode register. The $\overline{S_{RDY}}$ signal is driven "L" by a signal written into the serial I/O register to inform that the device is ready to receive. Then, the $\overline{S_{RDY}}$ signal is driven "H" on the first falling edge of the transfer clock.

The SA_{RDY} signal is driven "H" by a signal written into the serial I/O register, and driven "L" on the last rising edge of the transfer clock.

The function of serial I/O differs depending on the clock source; external clock or internal clock.

Internal Clock— The serial I/O counter is set to 7 when data is stored in the serial I/O register. At each falling edge of the transfer clock, serial data is output to $P1_5$. During the rising edge of this clock, data can be input from $P1_4$ and the data in the serial I/O register will be shifted 1 bit. Data is output starting with the LSB. After the transfer clock has counted 8 times, the serial I/O register will be empty and the transfer clock will remain at a high level. At this time the interrupt request bit will be set.

External Clock— If an external clock is used, the interrupt request bit will be set after the transfer clock has counted 8 times but the transfer clock will not stop. Due to this reason, the external clock must be controlled from the outside.

Timing diagrams are shown in Figure 9.

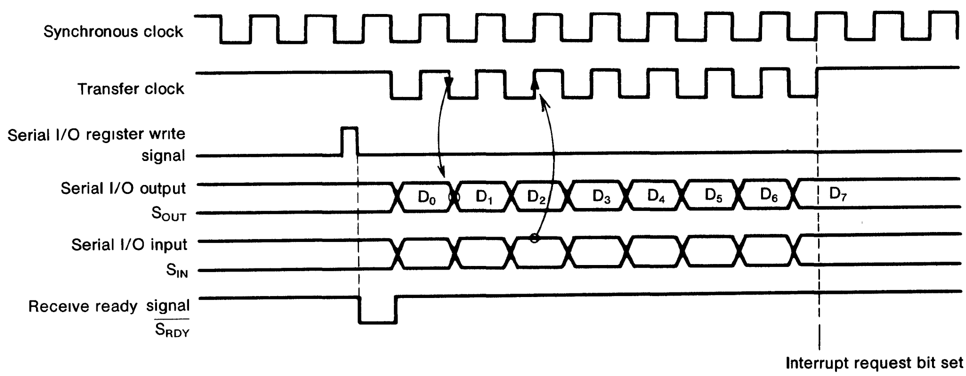


Fig. 9 Serial I/O timing

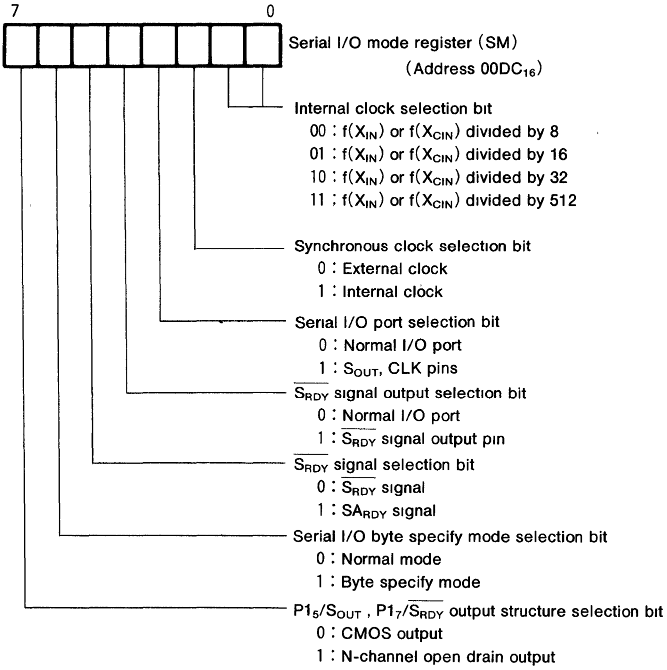


Fig. 10 Structure of serial I/O mode register

BYTE SPECIFY MODE

The serial I/O has a byte specify mode that allows one specific byte data to be selected for transmission or reception when serial I/O circuits of two or more microcomputers are connected to send or receive data through one bus. The data to be sent or received can be specified by writing a value into the byte counter. The value written in the byte counter is decremented by one each time eight cycles of transfer clock are input. When the value in the byte counter becomes "0", serial transmission/reception is done by the next eight cycles of transfer clock. When the value in the byte counter is not "0", the output on the S_{OUT} pin is driven "H" by the falling edge of the first transfer clock pulse to inhibit transmission/reception.

Serial I/O interrupt requests are generated only when serial transmission/reception is done after the value in the byte counter is decremented to "0". When the SA_{RDY} signal output is selected, the SA_{RDY} signal is driven "L" by the last rising edge of the transfer clock after the value in the byte counter is decremented to "0".

Note that in the byte mode, an external clock must be used as the sync. clock for the purpose of the mode.

A-D CONVERTER

The A-D conversion uses an 8-bit successive comparison method. Figure 11 shows a block diagram of the A-D conversion circuit. Conversion is automatically carried out once started by the program.

There are eight analog input pins which are shared with $P2_0$ to $P2_7$ of port P2. Which analog inputs are to be A-D converted is specified by using bit 2 to bit 0 in the A-D control register (address $00D9_{16}$). Pins for inputs to be A-D converted must be set for input by setting the directional register bit to "0". Bit 3 in the A-D control register is a A-D conversion end bit. This is "0" during A-D conversion; it is set to "1" when the conversion is terminated. Therefore, it is possible to know whether A-D conversion is terminated by checking this bit. Bit 4 in the A-D control register is a V_{REF} connection selection bit.

During A-D conversion, this bit must be set "1" for the ladder resistor and V_{REF} pin to be connected; after the A-D conversion is terminated, this bit can be reset to "0" to separate the ladder resistor from the V_{REF} pin. In this way, power consumption in the ladder resistor can be suppressed while no A-D conversion is performed. Figure 13 shows the relationship between the contents of A-D control register and the selected input pins.

The A-D conversion register (address $00DA_{16}$) contains information on the results of conversion, so that it is possible to know the results of conversion by reading the contents of this register.

The following explains the procedure to execute A-D conversion. First, set values to bit 2 to bit 0 in the A-D control register to select the pins that you want to execute A-D conversion. Next, clear the A-D conversion terminate bit to "0". When the above is done, A-D conversion is initiated. The A-D conversion is completed after an elapse of 50 machine cycles (25μs when $f(X_{IN})=4MHz$), the A-D conversion end bit is set to "1", and the interrupt request bit is set to "1". The results of conversion are contained in the A-D conversion register.

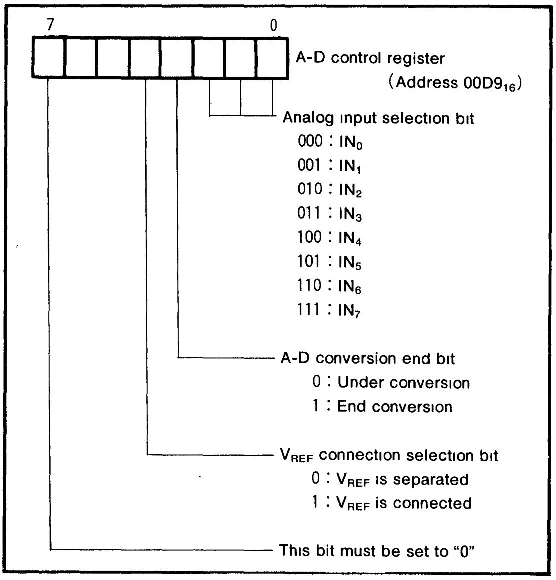


Fig. 12 Structure of A-D control register

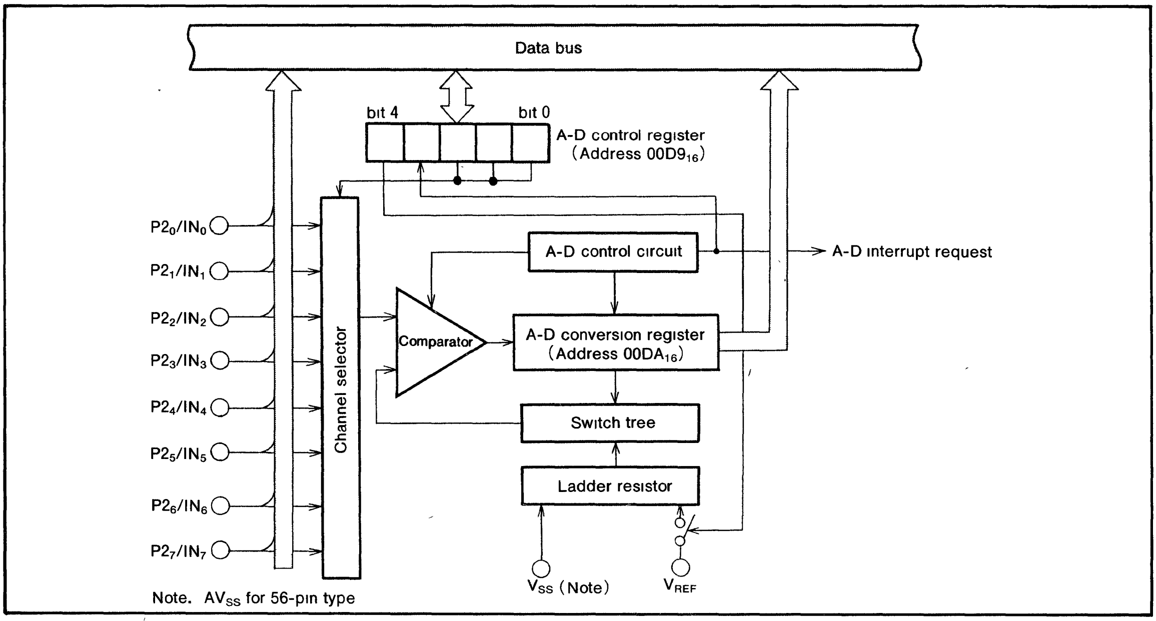


Fig. 11 A-D converter circuit

KEY ON WAKE UP

"Key on wake up" is one way of returning from a power down state caused by the STP or WIT instruction. If any terminal of port P0 has a "L" level applied, after bit 5 of the edge polarity selection register (EG_5) is set to "1", an interrupt is generated and the microcomputer is returned to the normal operating state. A key matrix can be connected to port P0 and the microcomputer can be returned to a normal state by pushing any key.

The key on wake up interrupt is common with the $\overline{INT_1}$ interrupt. When EG_5 is set to "1", the key on wake up function is selected. However, key on wake up cannot be used in the normal operating state. When the microcomputer is in the normal operating state, both key on wake up and $\overline{INT_1}$ are invalid.

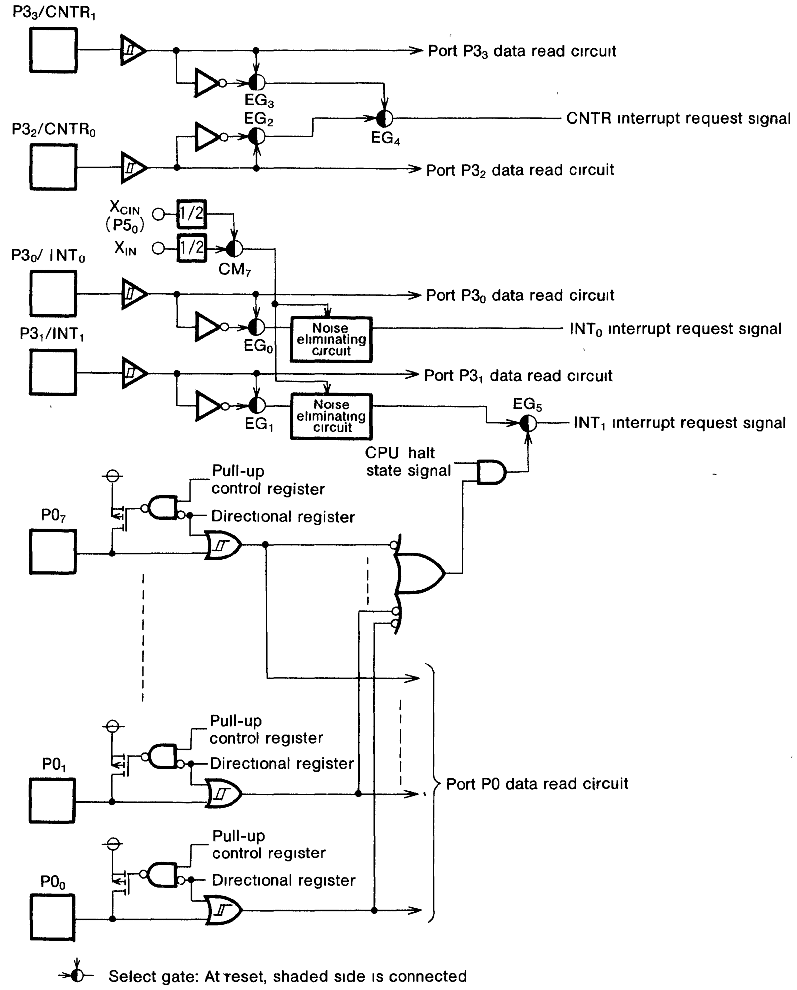


Fig. 13 Block diagram of interrupt input and key on wake up circuit

RESET CIRCUIT

The M37471M2-XXXSP/FP is reset according to the sequence shown in Figure 15. It starts the program from the address formed by using the content of address $FFFF_{16}$ as the high order address and the content of the address $FFFE_{16}$ as the low order address, when the $\overline{\text{RESET}}$ pin is held at "L" level for no less than 2μs while the power voltage is in the recommended operating condition and then returned to "H" level.

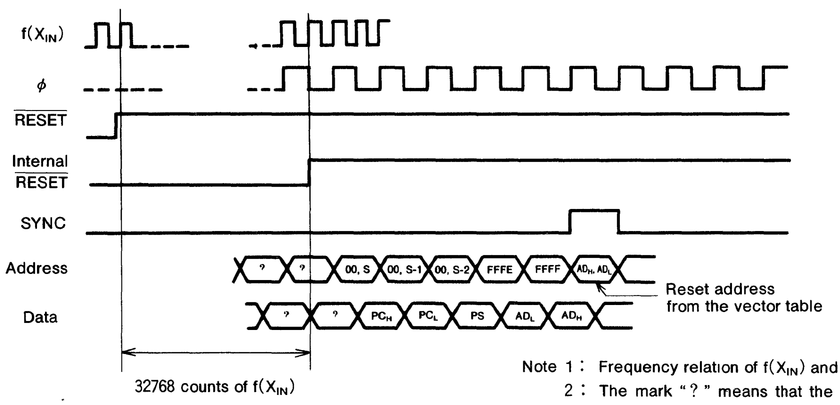
The internal initializations following reset are shown in Figure 14.

Immediately after reset, timer 3 and timer 4 are connected, and the $f(X_{IN})$ divided by 16 are counted. At this time, FF_{16} is set to timer 3, and 07_{16} is set to timer 4. The reset is cleared when timer 4 overflows.

		Address								
(1)	Port P0 directional register	$(C1_{16})$···	00_{16}							
(2)	Port P1 directional register	$(C3_{16})$···	00_{16}							
(3)	Port P2 directional register	$(C5_{16})$···	00_{16}							
(4)	Port P4 directional register	$(C9_{16})$···					0	0	0	0
(5)	P0 pull-up control register	$(D0_{16})$···	00_{16}							
(6)	P1~P5 pull-up control register	$(D1_{16})$···		0		0	0	0	0	0
(7)	Edge selection register	(EG) $(D4_{16})$···			0	0	0	0	0	0
(8)	A-D control register	$(D9_{16})$···	0			0	1	0	0	0
(9)	Serial I/O mode register	(SM) (DC_{16})···	00_{16}							
(10)	Timer 12 mode register	(T12M) $(F8_{16})$···	00_{16}							
(11)	Timer 34 mode register	(T34M) $(F9_{16})$···	00_{16}							
(12)	Timer mode register 2	(TM2) (FA_{16})···	0	0					0	0
(13)	CPU mode register	(CM) (FB_{16})···	0	0	0	0		0	0	0
(14)	Interrupt request register 1	(FC_{16})···	0	0			0	0	0	0
(15)	Interrupt request register 2	(FD_{16})···						0	0	0
(16)	Interrupt control register 1	(FE_{16})···	0	0			0	0	0	0
(17)	Interrupt control register 2	(FF_{16})···						0	0	0
(18)	Program counter	(PC_H)···	Contents of address $FFFF_{16}$							
		(PC_L)···	Contents of address $FFFE_{16}$							
(19)	Processor status register	(PS)···						1		

Note : Since the contents of both registers other than those listed above (including timers and the serial I/O register) are undefined at reset, it is necessary to set initial values

Fig. 14 Internal state of microcomputer at reset



Note 1 : Frequency relation of $f(X_{IN})$ and φ is $f(X_{IN}) = 2 \cdot φ$
2 : The mark "?" means that the address is changeable depending upon the previous state

Fig. 15 Timing diagram at reset

I/O PORTS

(1) Port P0

Port P0 is an 8-bit I/O port with CMOS outputs. As shown in Figure 2, P0 can be accessed as memory through zero page address $00C0_{16}$. Port P0's directional register allows each bit to be programmed individually as input or output. The directional register (zero page address $00C1_{16}$) can be programmed as input with "0", or as output with "1". When in the output mode, the data to be output is latched to the port latch and output. When data is read from the output port, the output pin level is not read, only the latched data of the port latch is read. Therefore, a previously output value can be read correctly even though the output voltage level has been shifted up or down. Port pins set as input are in the high impedance state so the signal level can be read. When data is written into the input port, the data is latched only to the output latch and the pin still remains in the high impedance state. Following the execution of STP or WIT instruction, key matrix with port P0 can be used to generate the interrupt to bring the microcomputer back in its normal state. When this port is selected for input, pull-up transistor can be connected in units of 1-bit.

(2) Port P1

Port P1 has the same function as port P0. $P1_2 \sim P1_7$ serve dual functions, and the desired function can be selected by the program. When this port is selected for input, pull-up transistor can be connected in units of 4-bit.

(3) Port P2

Port P2 has the same function as port P0. This port can also be used as an analog voltage input pin. When this port is selected for input, pull-up transistor can be connected in units of 4-bit.

(4) Port P3

Port P3 is an 4-bit input port.

(5) Port P4

Port P4 is an 4-bit I/O port and has basically the same functions as port P0. When this port is selected for input, pull-up transistor can be connected in units of 4-bit.

(6) Port P5

Port P5 is an 4-bit input port and pull-up transistor can be connected in units of 4-bit. $P5_0$ and $P5_1$ are shared with clock generating circuit input/output pins.

(7) INT_0 pin ($P3_0/INT_0$ pin)

This is an interrupt input pin, and is shared with port $P3_0$. When a "H" to "L" or a "L" to "H" transition input is applied to this pin, the INT_0 interrupt request bit (bit 0 of address $00FD_{16}$) is set to "1".

(8) INT_1 pin ($P3_1/INT_1$ pin)

This is an interrupt input pin, and is shared with port $P3_1$. When a "H" to "L" or a "L" to "H" transition input is applied to this pin, the INT_1 interrupt request bit (bit 1 of address $00FD_{16}$) is set to "1".

(9) Counter input $CNTR_0$ pin ($P3_2/CNTR_0$ pin)

This is a timer input pin, and is shared with port $P3_2$. When this pin is selected to $CNTR_0$ or $CNTR_1$ interrupt input pin and a "H" to "L" or a "L" to "H" transition input is applied to this pin, the $CNTR_0$ or $CNTR_1$ interrupt request bit (bit 2 of address $00FD_{16}$) is set to "1".

(10) Counter input $CNTR_1$ pin ($P3_3/CNTR_1$ pin)

This is a timer input pin, and is shared with port $P3_3$. When this pin is selected to $CNTR_0$ or $CNTR_1$ interrupt input pin and a "H" to "L" or a "L" to "H" transition input is applied to this pin, the $CNTR_0$ or $CNTR_1$ interrupt request bit (bit 2 of address $00FD_{16}$) is set to "1".

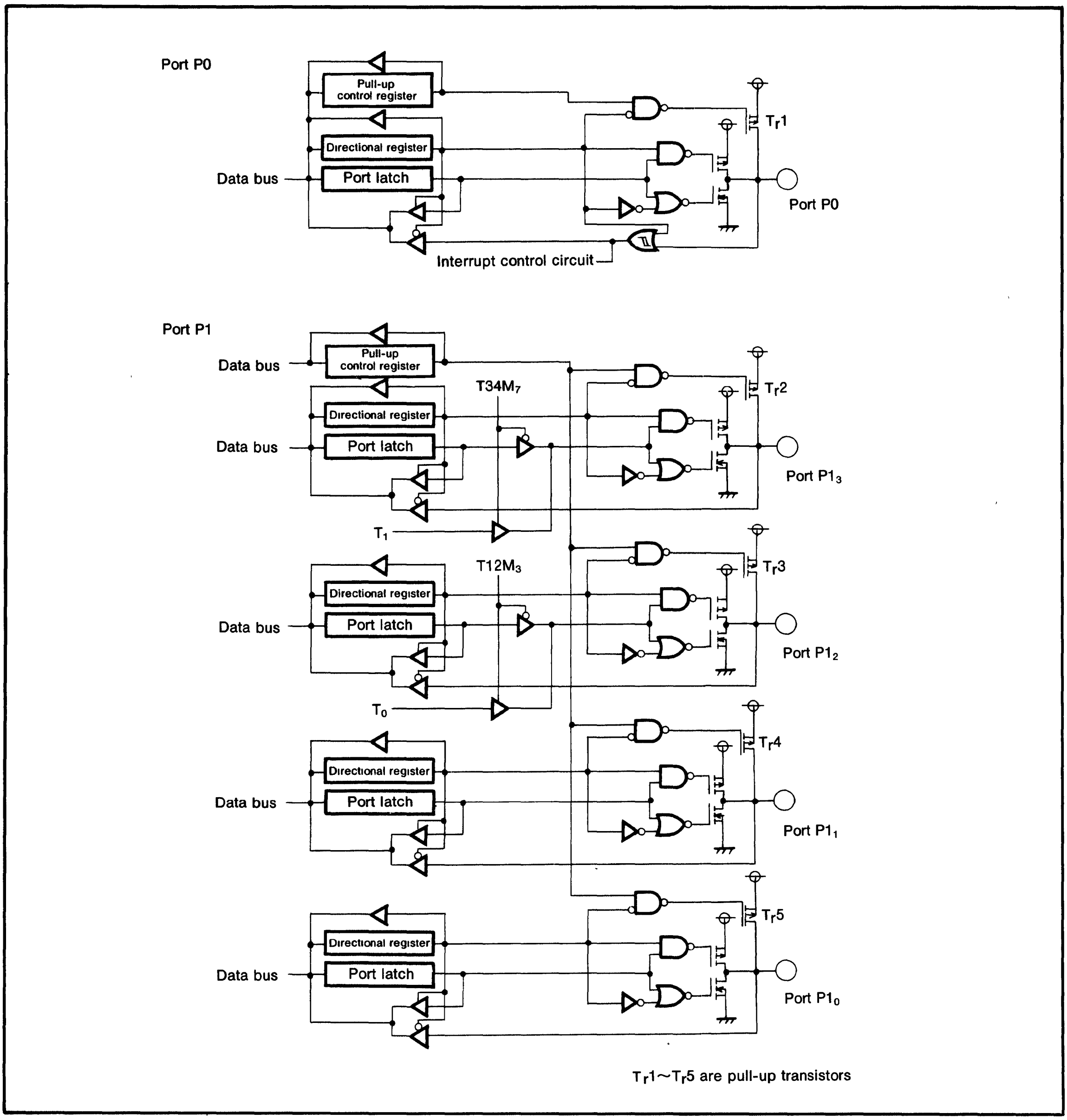


Fig. 16 Block diagram of ports P0～P1

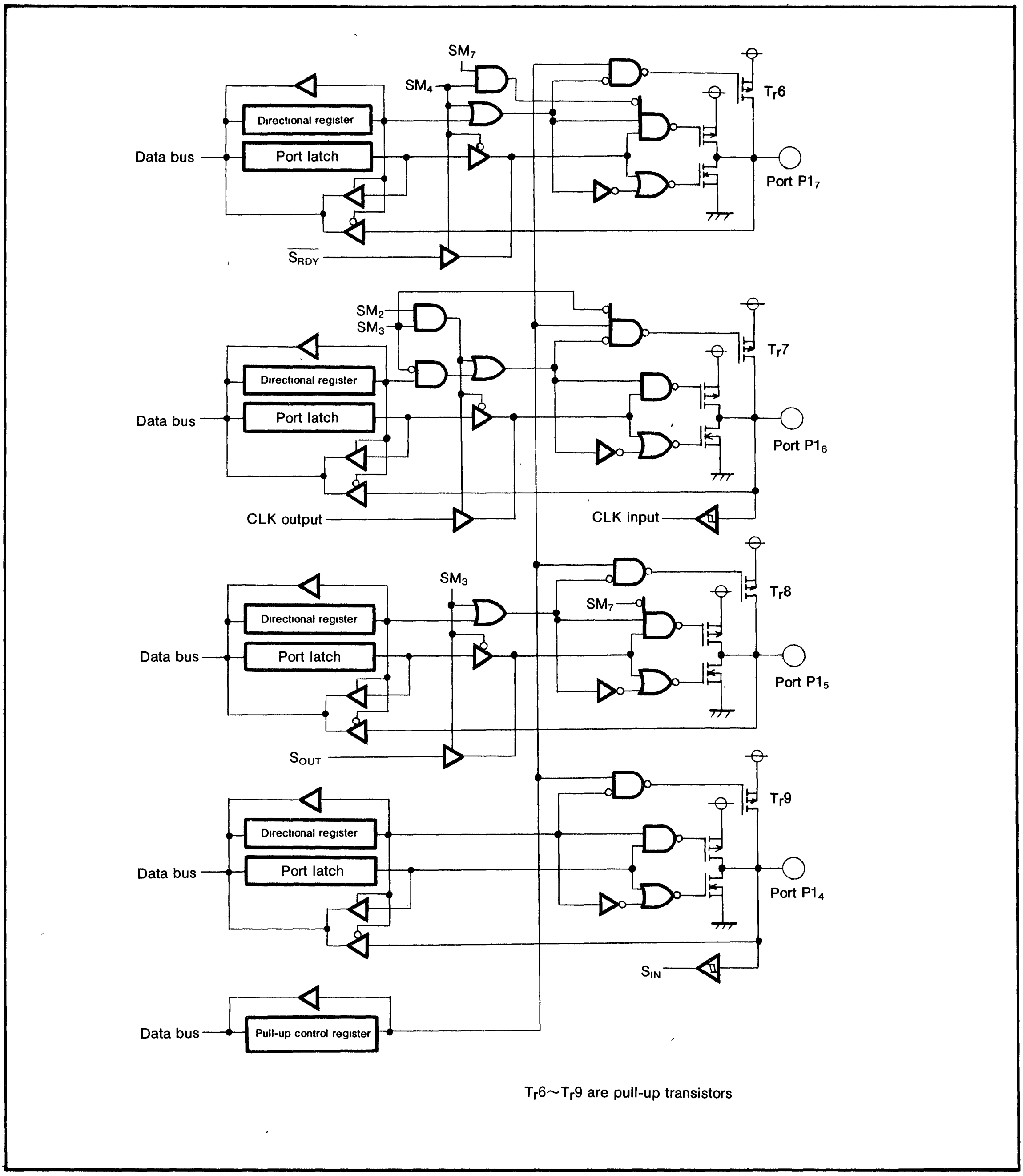
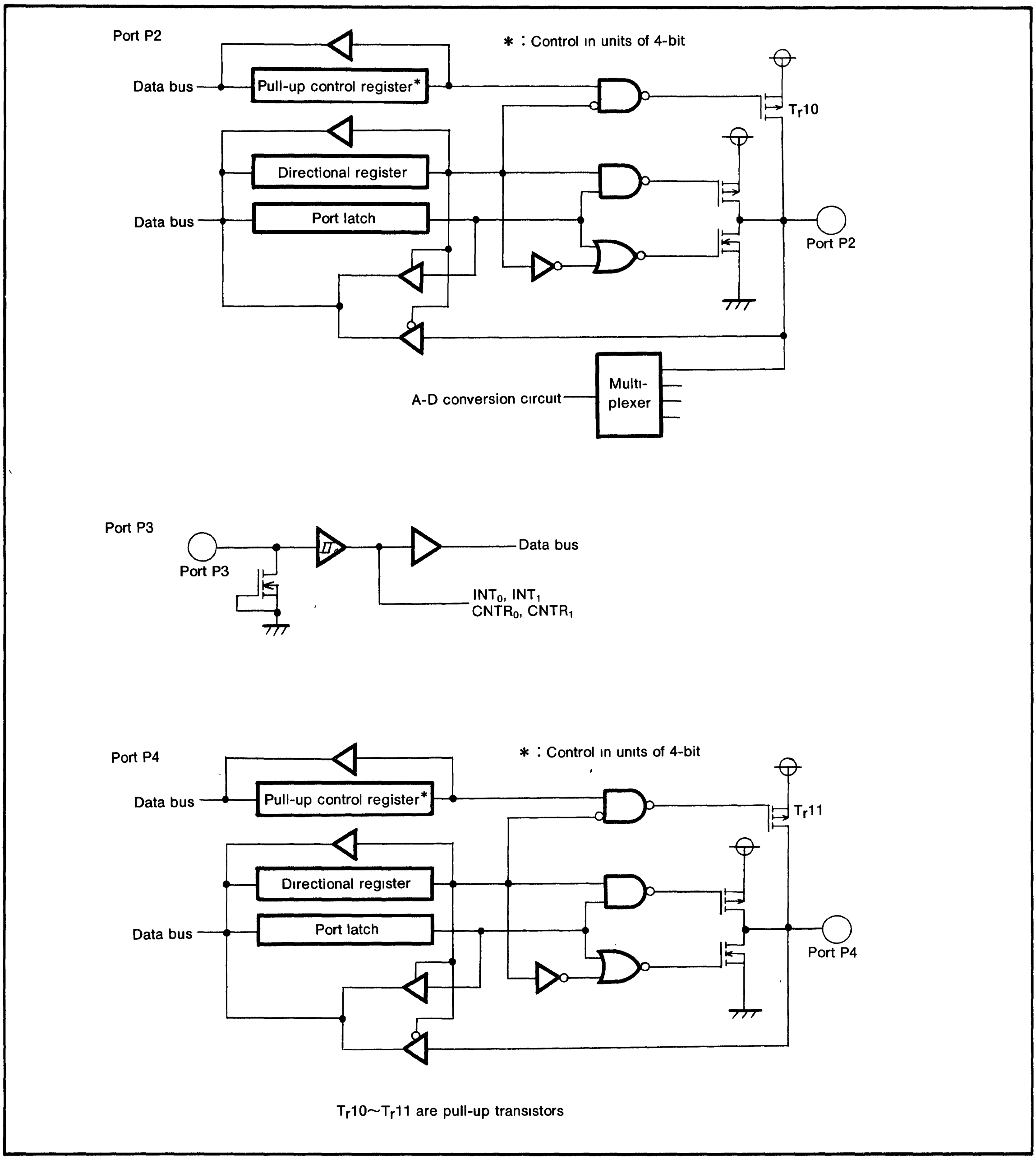


Fig. 17 Block diagram of port P1



$T_r10 \sim T_r11$ are pull-up transistors

Fig. 18 Block diagram of ports P2~P4

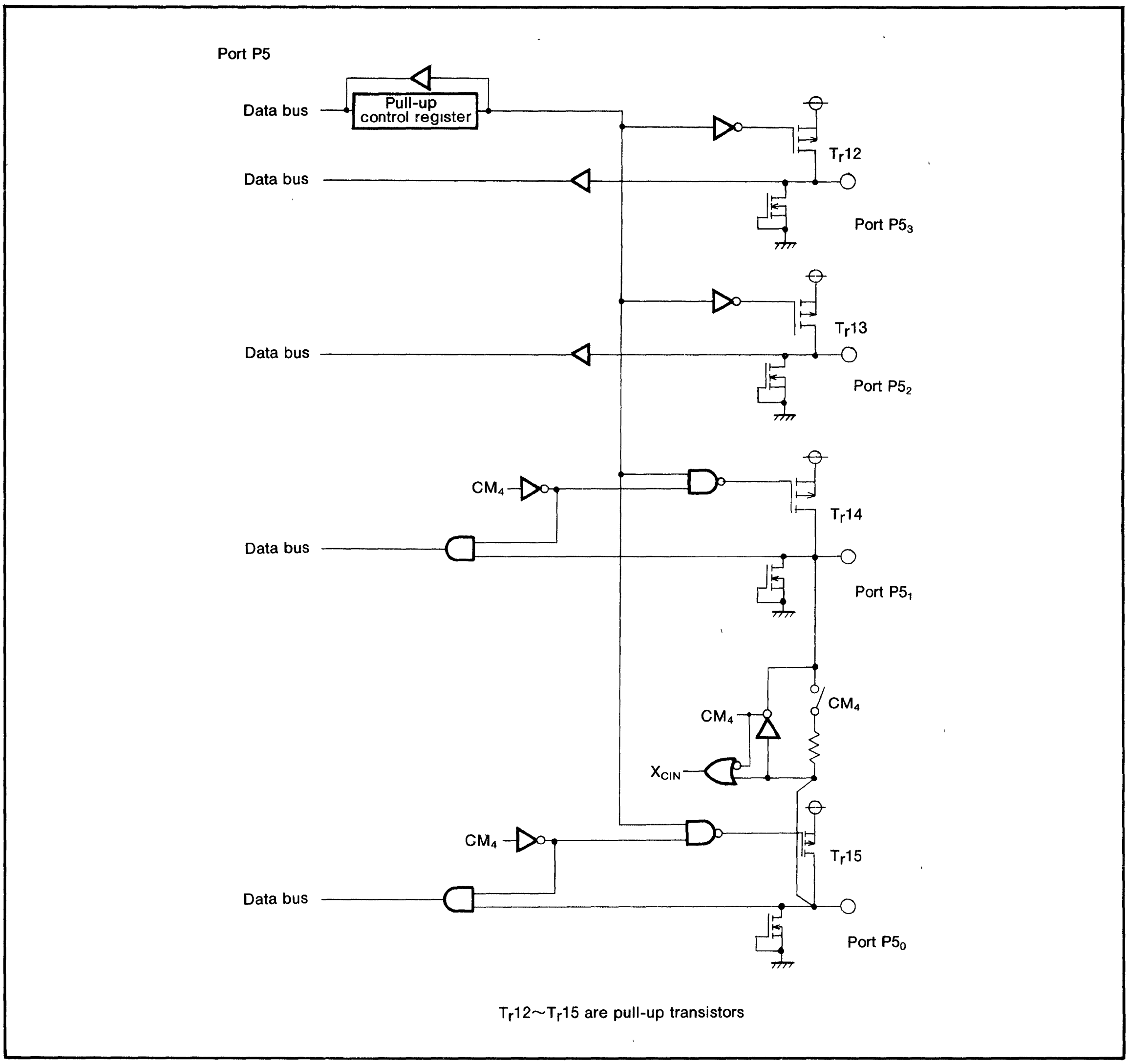


Fig. 19 Block diagram of port P5

CLOCK GENERATING CIRCUIT

The M37471M2-XXXSP/FP has two internal clock generating circuits. Figure 22 shows a block diagram of the clock generating circuits. Normally, the frequency applied to the clock input pin X_{IN} divided by two is used as the internal clock ϕ. Bit 7 of CPU mode register can be used to switch the internal clock ϕ to 1/2 the frequency applied to the clock input pin X_{CIN}.

Figure 20 shows a circuit example using a ceramic (or crystal) oscillator. Use the manufacturer's recommended values for constants such as capacitance which will differ depending on each oscillator. When using an external clock signal, input from the X_{IN} (X_{CIN}) pin and leave the X_{OUT} (X_{COUT}) pin open. A circuit example is shown in Figure 21.

The M37471M2-XXXSP/FP has two low power dissipation modes; stop and wait. The microcomputer enters a stop mode when the STP instruction is executed. The oscillator (both X_{IN} clock and X_{CIN} clock) stops with the internal clock ϕ held at "H" level. In this case timer 3 and timer 4 are forcibly connected and FF_{16} is automatically set in timer 3 and 07_{16} in timer 4.

Although oscillation is restarted when an external interrupt is accepted, the internal clock ϕ remains in the "H" state until timer 4 overflows. In other words, the internal clock ϕ is not supplied until timer 4 overflows. This is because when a ceramic or similar other oscillator is used, a finite time is required until stable oscillation is obtained after restart.

The microcomputer enters a wait mode when the WIT instruction is executed. The internal clock ϕ stops at "H" level, but the oscillator does not stop. ϕ is re-supplied (wait mode release) when the microcomputer recieves an interrupt.

Instructions can be executed immediately because the oscillator is not stopped. The interrupt enable bit of the interrupt used to reset the wait mode or the stop mode must be set to "1" before executing the WIT or the STP instruction.

Low power dissipation operation is also achieved when the X_{IN} clock is stopped and the internal clock ϕ is generated from the X_{CIN} clock (30μA typ. at f(X_{CIN}) = 32kHz). X_{IN} clock oscillation is stopped when the bit 6 of CPU mode register is set and restarted when it is cleared. However, the wait time until the oscillation stabilizes must be generated with a program when restarting. Figure 24 shows the transition of states for the system clock.

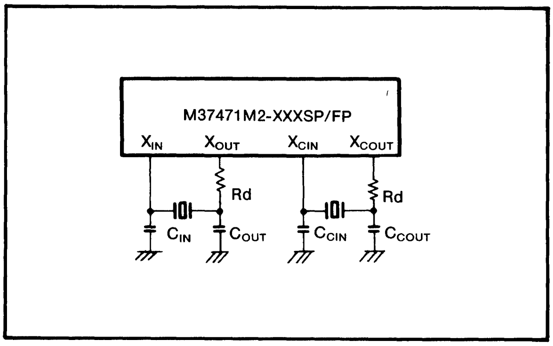


Fig. 20 Example of ceramic resonator circuit

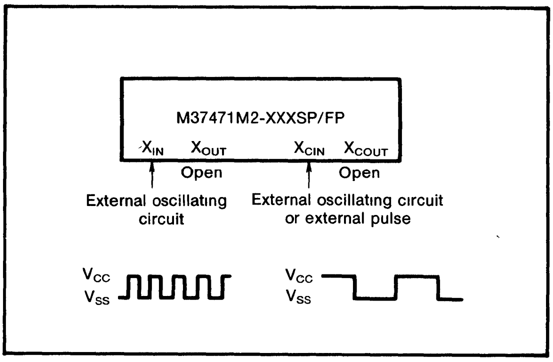


Fig. 21 External clock input circuit

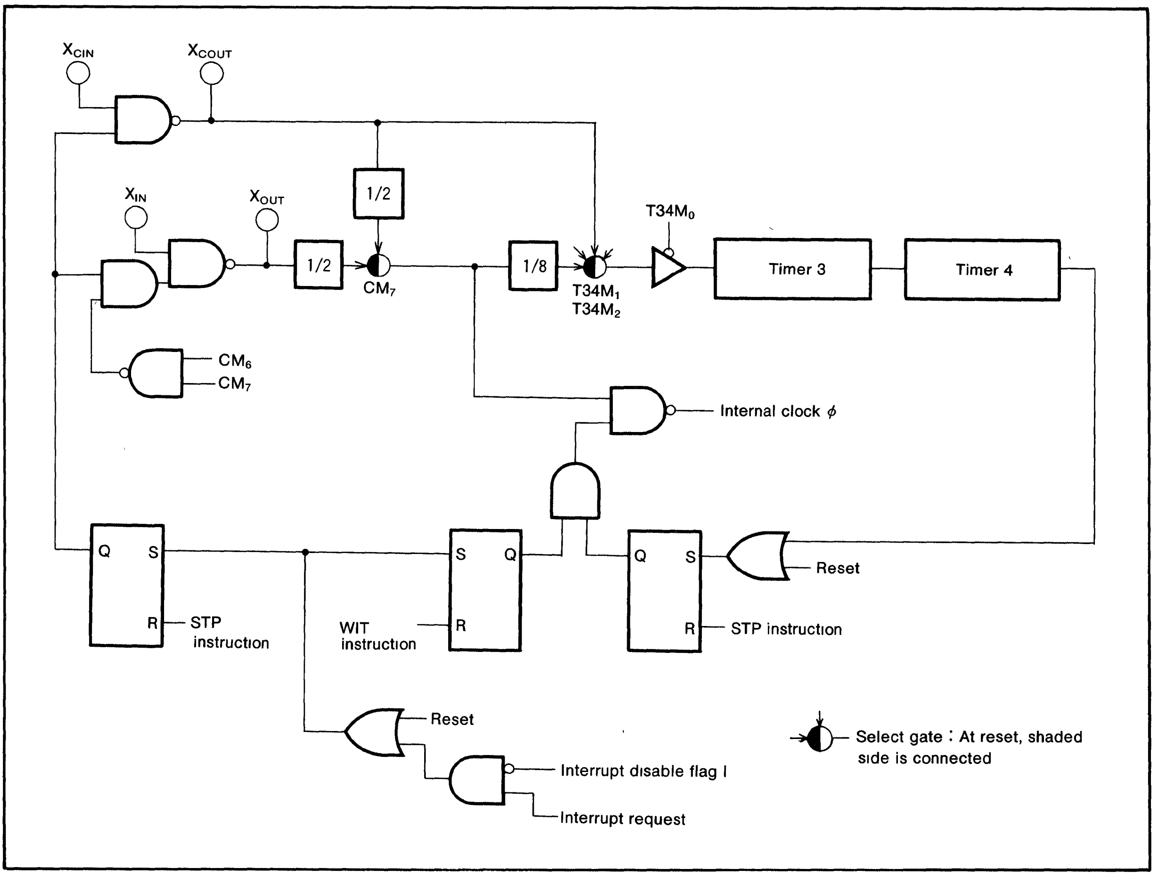


Fig. 22 Block diagram of clock generating circuit

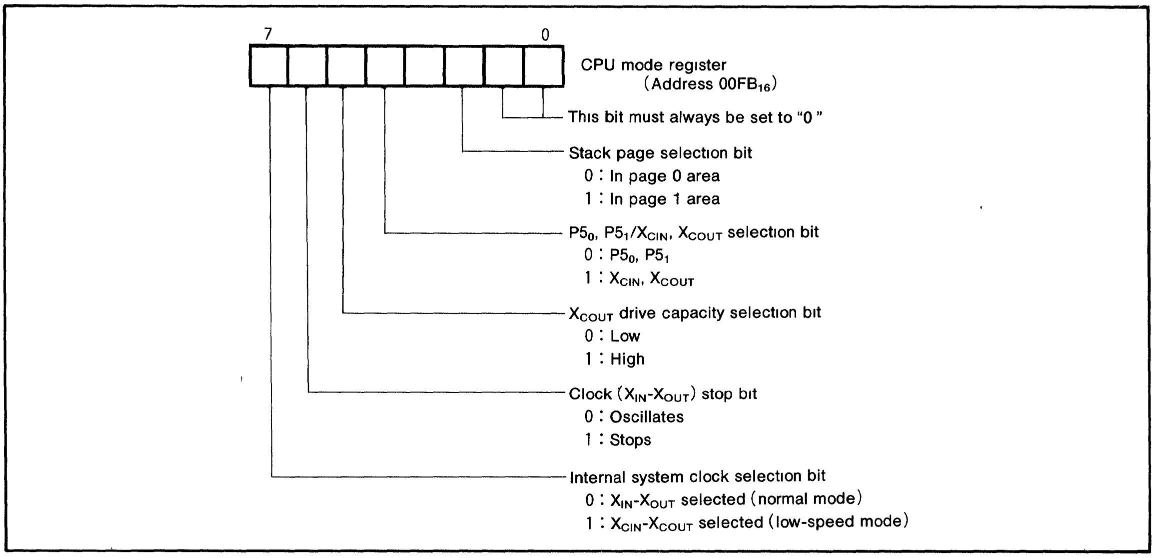
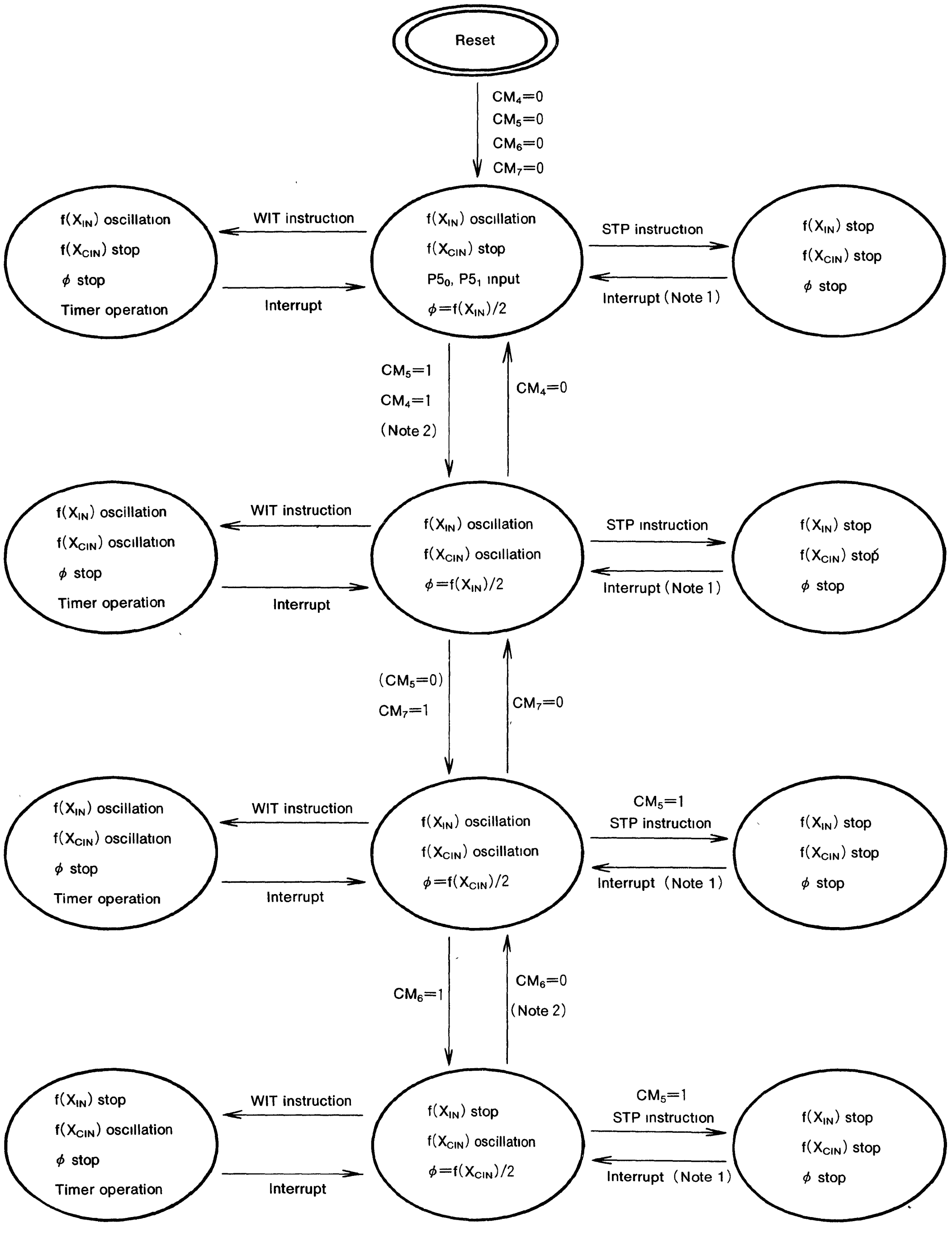


Fig. 23 Structure of CPU mode register

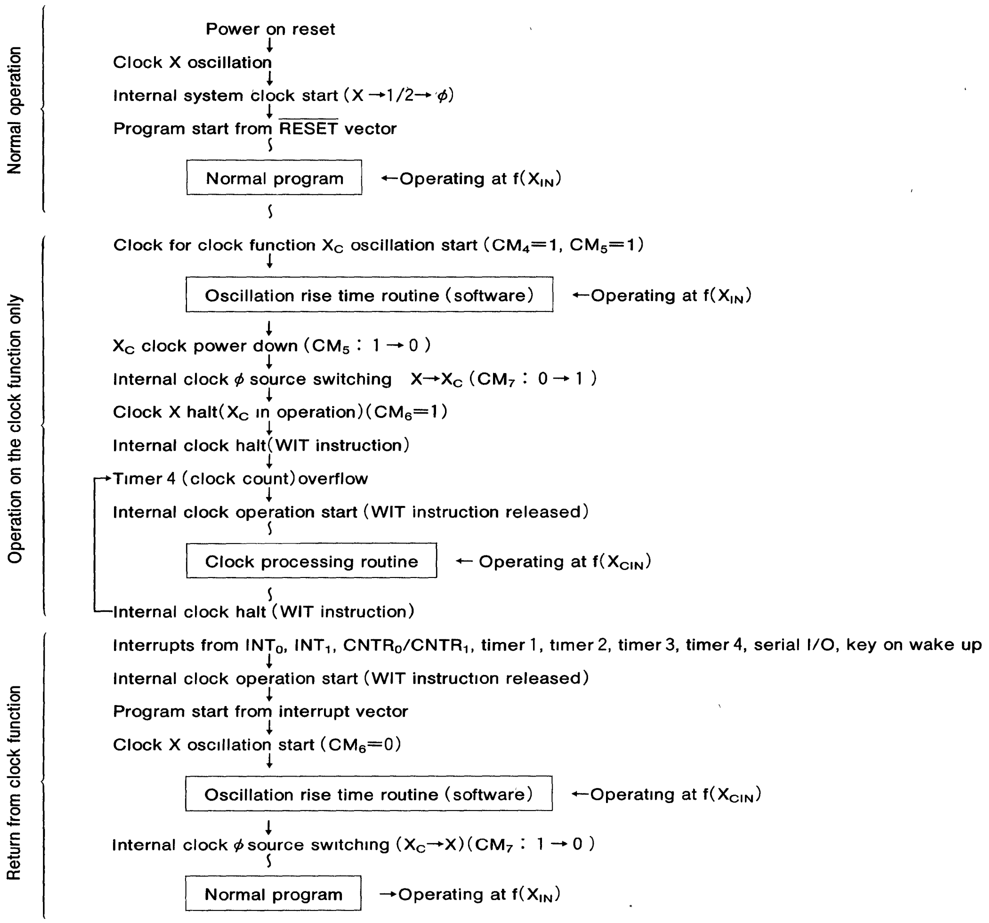


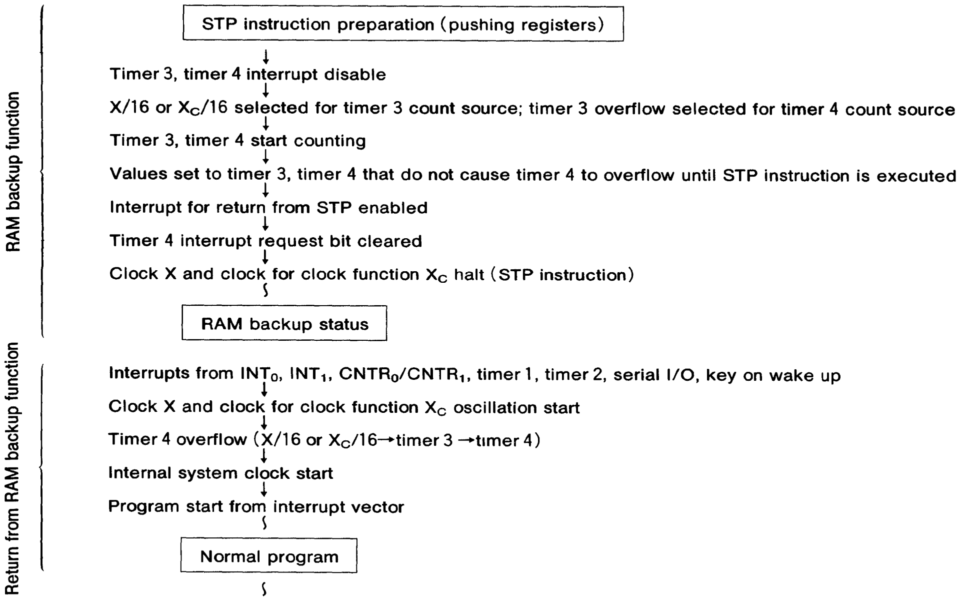
Note 1 : Latency time are automatically generated upon release from the STP instruction due to the connections of timer 3 and 4.

2 : When the system clock is switched over by restarting clock oscillation, a certain wait time required for oscillation to stabilize must be inserted by the program.

Fig. 24 Transition of states for the system clock.

≪An example of flow for system≫




RAM backup function
STP instruction preparation (pushing registers)
Timer 3, timer 4 interrupt disable
X/16 or X_C/16 selected for timer 3 count source; timer 3 overflow selected for timer 4 count source
Timer 3, timer 4 start counting
Values set to timer 3, timer 4 that do not cause timer 4 to overflow until STP instruction is executed
Interrupt for return from STP enabled
Timer 4 interrupt request bit cleared
Clock X and clock for clock function X_C halt (STP instruction)
RAM backup status
Return from RAM backup function
Interrupts from INT_0, INT_1, $CNTR_0$/$CNTR_1$, timer 1, timer 2, serial I/O, key on wake up
Clock X and clock for clock function X_C oscillation start
Timer 4 overflow (X/16 or X_C/16→timer 3 →timer 4)
Internal system clock start
Program start from interrupt vector
Normal program

PROGRAMMING NOTES

(1) The frequency ratio of the timer is 1/(n+1)

(2) Even though the BBC and BBS instructions are executed after the interrupt request bits are modified (by the program), those instructions are only valid for the contents before the modification. Also, at least one instruction cycle must be used (such as a NOP) between the modification of the interrupt request bits and the execution of the BBC and BBS instructions.

(3) After the ADC and SBC instructions are executed (in decimal mode), one instruction cycle (such as a NOP) is needed before the SEC, CLC, or CLD instructions are executed.

(4) A NOP instruction must be used after the execution of a PLP instruction.

(5) During A-D conversion, don't use STP instruction.

DATA REQUIRED FOR MASK ORDERING

Please send the following data for mask orders.

(1) mask ROM confirmation form

(2) mask specification form

(3) ROM data ·· EPROM 3 sets

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS} Output transistors are at "OFF" state	$-0.3\sim 7$	V
V_I	Input voltage X_{IN}		$-0.3\sim V_{CC}+0.3$	V
V_I	Input voltage $P0_0\sim P0_7$, $P1_0\sim P1_7$, $P2_0\sim P2_7$, $P3_0\sim P3_3$, $P4_0\sim P4_3$, $P5_0\sim P5_3$, V_{REF}, $\overline{RESET}$		$-0.3\sim V_{CC}+0.3$	V
V_O	Output voltage $P0_0\sim P0_7$, $P1_0\sim P1_7$, $P2_0\sim P2_7$, $P4_0\sim P4_3$, X_{OUT}		$-0.3\sim V_{CC}+0.3$	V
P_d	Power dissipation	$T_a=25$℃	1000(Note 1)	mW
Topr	Operating temperature		$-20\sim 85$	℃
Tstg	Storage temperature		$-40\sim 150$	℃

Note 1 : 500mW for QFP type

RECOMMENDED OPERATING CONDITIONS

($V_{CC}=2.7\sim 5.5$V, $V_{SS}=AV_{SS}=0$V, $Ta=-20\sim 85$℃ unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	2.7	5	5.5	V
V_{SS}	Supply voltage		0		V
AV_{SS}	Analog supply voltage		0		V
V_{IH}	"H" Input voltage $P0_0\sim P0_7$, $P1_0\sim P1_7$, $P3_0\sim P3_3$, $\overline{RESET}$, X_{IN}	$0.8V_{CC}$		V_{CC}	V
V_{IH}	"H" Input voltage $P2_0\sim P2_7$, $P4_0\sim P4_3$, $P5_0\sim P5_3$ (Note 1)	$0.7V_{CC}$		V_{CC}	V
V_{IL}	"L" Input voltage $P0_0\sim P0_7$, $P1_0\sim P1_7$, $P3_0\sim P3_3$	0		$0.2V_{CC}$	V
V_{IL}	"L" Input voltage $P2_0\sim P2_7$, $P4_0\sim P4_3$, $P5_0\sim P5_3$ (Note 1)	0		$0.25V_{CC}$	V
V_{IL}	"L" Input voltage $\overline{RESET}$	0		$0.12V_{CC}$	V
V_{IL}	"L" Input voltage X_{IN}	0		$0.16V_{CC}$	V
$I_{OH(sum)}$	"H" sum output current $P0_0\sim P0_7$, $P4_0\sim P4_3$			-30	mA
$I_{OH(sum)}$	"H" sum output current $P1_0\sim P1_7$, $P2_0\sim P2_7$			-30	mA
$I_{OL(sum)}$	"L" sum output current $P0_0\sim P0_7$, $P4_0\sim P4_3$			60	mA
$I_{OL(sum)}$	"L" sum output current $P1_0\sim P1_7$, $P2_0\sim P2_7$			60	mA
$I_{OL(peak)}$	"L" peak output current $P0_0\sim P0_7$, $P1_0\sim P1_7$, $P2_0\sim P2_7$, $P4_0\sim P4_3$			20	mA
$I_{OL(avg)}$	"L" average output current $P0_0\sim P0_7$, $P1_0\sim P1_7$, $P2_0\sim P2_7$, $P4_0\sim P4_3$ (Note 4)			10	mA
$I_{OH(peak)}$	"H" peak output current $P0_0\sim P0_7$, $P1_0\sim P1_7$, $P2_0\sim P2_7$, $P4_0\sim P4_3$			-10	mA
$I_{OH(avg)}$	"H" average output current $P0_0\sim P0_7$, $P1_0\sim P1_7$, $P2_0\sim P2_7$, $P4_0\sim P4_3$ (Note 4)			-5	mA
$f_{(CNTR)}$	Timer input frequency $CNTR_0$ ($P3_2$), $CNTR_1$ ($P3_3$) (Note 2)			1	MHz
$f_{(CLK)}$	Serial I/O clock input frequency CLK ($P1_6$) (Note 2)			1	MHz
$f(X_{IN})$	Clock oscillating frequency (Note 2)			4	MHz
$f(X_{CIN})$	Clock oscillating frequency for clock function (Note 2, 3)		32	50	kHz

Note 1 : It is except to use $P5_0$ as X_{CIN}

2 : Oscillation frequency is at 50% duty cycle

3 : When used in the low-speed mode, the clock oscillating frequency for clock function should be $f(X_{CIN})<f(X_{IN})/3$

4 : The average output current I_{OH} (avg) and I_{OL} (avg) are the average value during a 100ms

ELECTRICAL CHARACTERISTICS (V_{CC}=2.7~5.5V, V_{SS}=AV_{SS}=0V, T_a=−20~85℃, unless otherwise noted)

Symbol	Parameter	Test Conditions		Limits			Unit
				Min	Typ	Max	
V_{OH}	"H" output voltage $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P4_0$~$P4_3$	V_{CC}=5V, I_{OH}=−5mA		3			V
		V_{CC}=3V, I_{OH}=−1.5mA		2			
V_{OL}	"L" output voltage $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P4_0$~$P4_3$	V_{CC}=5V, I_{OL}=10mA				2	V
		V_{CC}=3V, I_{OL}=3mA				1	
$V_{T+}-V_{T-}$	Hysteresis $P0_0$~$P0_7$, $P3_0$~$P3_3$	V_{CC}=5V			0.5		V
		V_{CC}=3V			0.3		
$V_{T+}-V_{T-}$	Hysteresis $\overline{\text{RESET}}$	V_{CC}=5V			0.5		V
		V_{CC}=3V			0.3		
$V_{T+}-V_{T-}$	Hysteresis $P1_6$/CLK	use as CLK input	V_{CC}=5V		0.5		V
			V_{CC}=3V		0.3		
I_{IL}	"L" input current $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P3_0$~$P3_2$, $P4_0$~$P4_3$, $P5_0$~$P5_3$	V_I=0V, not use pull-up transistor	V_{CC}=5V			−5	µA
			V_{CC}=3V			−3	
		V_I=0V, use pull-up transistor	V_{CC}=5V	−0.25	−0.5	−1.0	mA
			V_{CC}=3V	−0.08	−0.18	−0.35	
I_{IL}	"L" input current $P3_3$	V_I=0V	V_{CC}=5V			−5	µA
			V_{CC}=3V			−3	
I_{IL}	"L" input current $P2_0$~$P2_7$	V_I=0V, not use as analog input, not use pull-up transistor	V_{CC}=5V			−5	µA
			V_{CC}=3V			−3	
		V_I=0V, not use as analog input, use pull-up transistor	V_{CC}=5V	−0.25	−0.5	−1.0	mA
			V_{CC}=3V	−0.08	−0.18	−0.35	
I_{IL}	"L" input current $\overline{\text{RESET}}$, X_{IN}	V_I=0V (X_{IN} is at stop mode)	V_{CC}=5V			−5	µA
			V_{CC}=3V			−3	
I_{IH}	"H" input current $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P3_0$~$P3_2$, $P4_0$~$P4_3$, $P5_0$~$P5_3$	V_I=V_{CC}, not use pull-up transistor	V_{CC}=5V			5	µA
			V_{CC}=3V			3	
I_{IH}	"H" input current $P3_3$	V_I=V_{CC}	V_{CC}=5V			5	µA
			V_{CC}=3V			3	
I_{IH}	"H" input current $P2_0$~$P2_7$	V_I=V_{CC}, not use as analog input, not use pull-up transistor	V_{CC}=5V			5	µA
			V_{CC}=3V			3	
I_{IH}	"H" input current $\overline{\text{RESET}}$, X_{IN}	V_I=V_{CC}, (X_{IN} is at stop mode)	V_{CC}=5V			5	µA
			V_{CC}=3V			3	
I_{CC}	Supply current	At normal operation, A-D conversion is not executed X_{IN}=4MHz	V_{CC}=5V		3.5	7	mA
			V_{CC}=3V		1.8	3.6	
		At normal operation, A-D conversion is executed X_{IN}=4MHz	V_{CC}=5V		4	8	
			V_{CC}=3V		2	4	
		At low-speed mode, X_{COUT} is low-power mode, A-D conversion is not executed X_{IN}=0Hz, X_{CIN}=32kHz, T_a=25℃	V_{CC}=5V		30	80	µA
			V_{CC}=3V		15	40	
		At wait mode, X_{IN}=4MHz	V_{CC}=5V		1	2	mA
			V_{CC}=3V		0.5	1	
		At wait mode, X_{IN}=0Hz, X_{CIN}=32kHz, X_{COUT} is low-power mode, T_a=25℃	V_{CC}=5V		3	12	µA
			V_{CC}=3V		2	8	
		Stop all oscillation V_{CC}=5V	T_a=25℃		0.1	1	
			T_a=85℃		1	10	
V_{RAM}	RAM retention voltage	Stop all oscillation		2			V

A-D CONVERTER CHARACTERISTICS (V_{CC}=2.7~5.5V, V_{SS}=AV_{SS}=0V, T_a=−20~85℃, f(X_{IN})=4MHz, unless otherwise noted)

Symbol	Parameter	Test Conditions	Limits			Unit
			Min.	Typ	Max	
—	Resolution				8	bits
—	Non-linearity error				±2	LSB
—	Differential non-linearity error				±0.9	LSB
V_{OT}	Zero transition error	V_{CC}=V_{REF}=5.12V, $I_{OL(sum)}$=0mA			2	LSB
		V_{CC}=V_{REF}=3.072V, $I_{OL(sum)}$=0mA			3	
V_{FST}	Full-scale transition error	V_{CC}=V_{REF}=5.12V			4	LSB
		V_{CC}=V_{REF}=3.072V			7	
t_{CONV}	Conversion time				25	μs
V_{VREF}	Reference input voltage		0.5V_{CC}		V_{CC}	V
R_{LADDER}	Ladder resistance value		2	5	10	kΩ
V_{IA}	Analog input voltage		0		V_{REF}	V

MITSUBISHI MICROCOMPUTERS

M37470E4-XXXSP
M37470E8-XXXSP

PROM VERSION of M37470M4-XXXSP,M37470M8-XXXSP

DESCRIPTION

The M37470E4-XXXSP is a single-chip microcomputer designed with CMOS silicon gate technology. It is housed in a 32-pin shrink plastic molded DIP. The features of this chip are similar to those of the M37470M4-XXXSP except that this chip has a 8192 bytes PROM built-in. This single-chip microcomputer is useful for home electrical appliances and consumer appliance controllers.

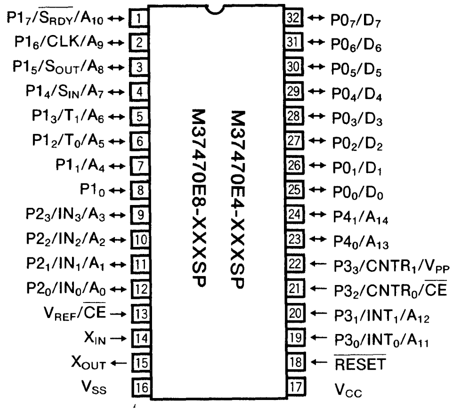
In addition to its simple instruction sets, the PROM, RAM, and I/O addresses are placed on the same memory map to enable easy programming. Since general purpose PROM writers can be used for the built-in PROM, this chip is suitable for small quantity production runs.

The differences between the M37470E4-XXXSP and the M37470E8-XXXSP are noted below. The following explanations apply to the M37470E4-XXXSP.

Specification variations for other chips are noted accordingly.

Type name	ROM size	RAM size
M37470E4-XXXSP	8192 bytes	192 bytes
M37470E8-XXXSP	16384 bytes	384 bytes

PIN CONFIGURATION (TOP VIEW)



Outline 32P4B

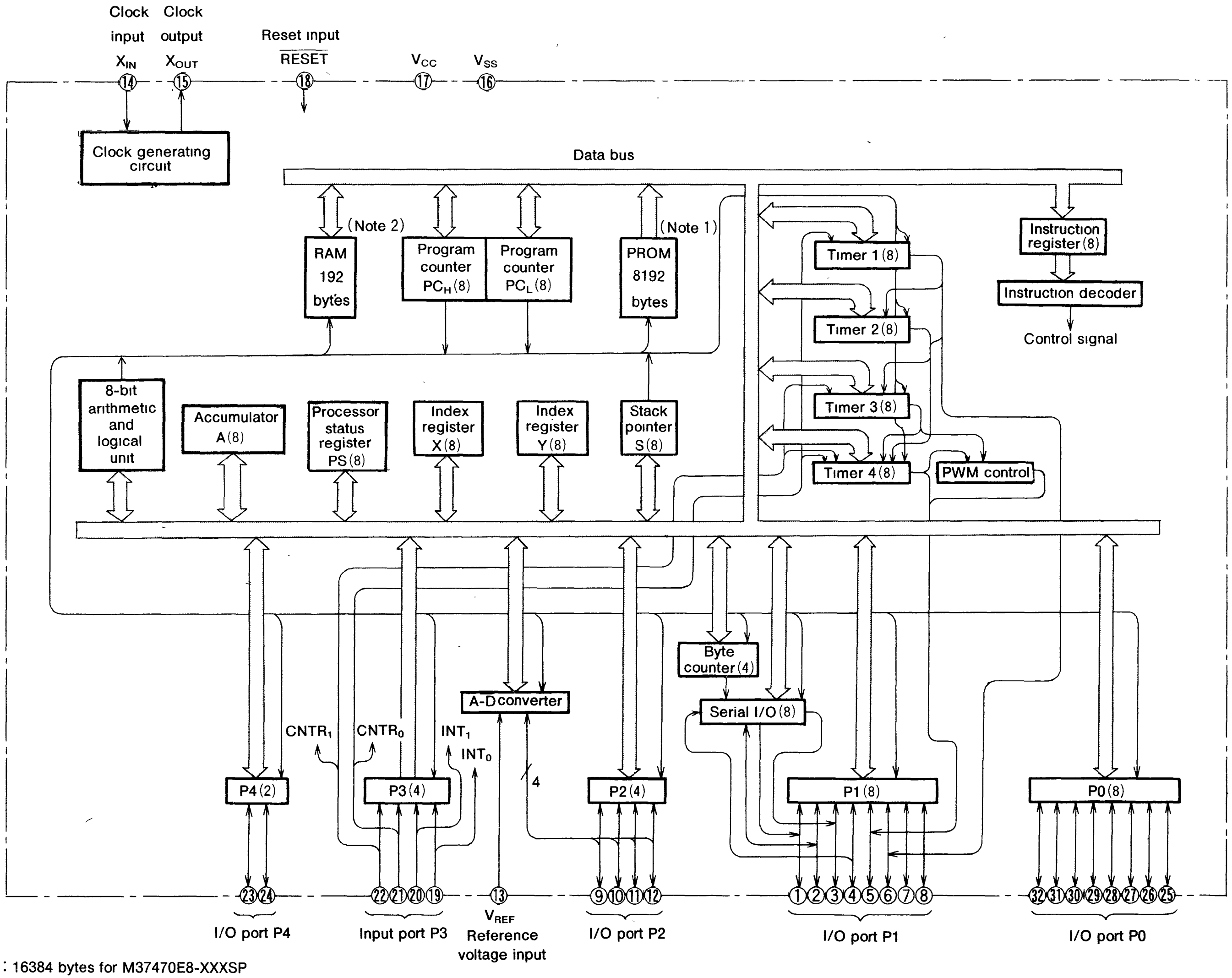
FEATURES

- Number of basic instructions ········· 69
- Memory size PROM ········· 8192 bytes (M37470E4)
  16384 bytes (M37470E8)
  RAM ········· 192 bytes (M37470E4)
  384 bytes (M37470E8)
- Instruction execution time
  ······· 1μs (minimum instructions at 4MHz frequency)
- Single power supply ········· 2.7~5.5V
- Power dissipation
  normal operation mode (at 4MHz frequency) 17.5mW
- Subroutine nesting ········· 96 levels max. (M37470E4)
- Interrupt ········· 12 types, 10 vectors
- 8-bit timer ········· 4
- Serial I/O ········· 8-bit×1
- Programmable I/O ports (Ports P0, P1, P2, P4) ········· 22
- Input port (Port P3) ········· 4
- A-D converter ········· 8-bit, 4-channel
- PROM (equivalent to the M5L27256)
  program voltage ········· 12.5V

APPLICATION

Office automation equipment, VCR, Tuner, Audio-visual equipment

M37470E4-XXXSP BLOCK DIAGRAM



Note 1 : 16384 bytes for M37470E8-XXXSP
2 : 384 bytes for M37470E8-XXXSP

FUNCTIONS OF M37470E4-XXXSP, M37470E8-XXXSP

Parameter			Functions
Number of basic instructions			69
Instruction execution time			1μs (minimum instructions, at 4MHz frequency)
Clock frequency			4MHz (max.)
Memory size	M37470E4-XXXSP	PROM	8192 bytes (Note 1)
		RAM	192 bytes
	M37470E8-XXXSP	PROM	16384 bytes (Note 1)
		RAM	384 bytes
Input/Output port	P0, P1	I/O	8-bit×2
	P2	I/O	4-bit×1
	P3	Input	4-bit×1
	P4	I/O	2-bit×1
Serial I/O			8-bit×1
Timers			8-bit timer×4
A-D converter			8-bit×1 (4channel)
Subroutine nesting	M37470E4-XXXSP		96 levels (max)
	M37470E8-XXXSP		192 levels (max)
Interrupt			Five external interrupts, six internal interrupts, one software interrupt
Clock generating circuit			Built-in with internal feedback resistor (ceramic or quartz crystal oscillator)
Supply voltage			2 7~5 5V
Power dissipation			17 5mW (at $f(X_{IN})$=4MHz)
Input/Output characteristics	Input/Output voltage		5V
	Output current		−5~10mA (ports P0, P1, P2, P4 CMOS tri-state output)
Operating temperature range			−20~85℃
Device structure			CMOS Silicon gate
Package			32-pin shrink plastic molded DIP

Note 1 : The PROM programming voltage is 12.5V (equivalent to the M5L27256).

PIN DESCRIPTION

Pin	Mode	Name	Input/ Output	Functions
V_{CC}, V_{SS}	Single-chip /EPROM	Supply voltage		Power supply inputs 2 7~5.5V to V_{CC} and 0V to V_{SS}
$\overline{\text{RESET}}$	Single-chip	RESET input	Input	To reset, keep this input terminal low for more than 2μs (min) under normal V_{CC} conditions.
	EPROM	RESET input		Connect to V_{SS}
X_{IN}	Single-chip /EPROM	Clock input	Input	Connect a ceramic or a quartz crystal oscillator between X_{IN} and X_{OUT} for clock oscillation If an external clock input is used, connect the clock input to the X_{IN} pin and open the X_{OUT} pin Feedback resistor is connected between the X_{IN} and X_{OUT} pins
X_{OUT}		Clock output	Output	
$P0_0$~$P0_7$	Single-chip	I/O port P0	I/O	Port P0 is an 8-bit I/O port The output structure is CMOS output When this port is selected for input, pull-up transistor can be connected in units of 1-bit and a key on wake up function is provided
	EPROM	Data input/output D_0~D_7	I/O	Port P0 works as an 8-bit data bus (D_0~D_7)
$P1_0$~$P1_7$	Single-chip	I/O port P1	I/O	Port P1 is an 8-bit I/O port The output structure is CMOS output When this port is selected for input, pull-up transistor can be connected in units of 4-bit $P1_2$, $P1_3$ are in common with timer output pins T_0, T_1 $P1_4$, $P1_5$, $P1_6$, $P1_7$ are in common with serial I/O pins S_{IN}, S_{OUT}, CLK, $\overline{S_{RDY}}$, respectively The output structure of S_{OUT} and $\overline{S_{RDY}}$ can be changed to N-channel open drain output
	EPROM	Address input A_4~A_{10}	Input	$P1_1$~$P1_7$ works as the 7-bit address input (A_4~A_{10}) $P1_0$ must be opened.
$P2_0$~$P2_3$	Single-chip	I/O port P2	I/O	Port P2 is an 4-bit I/O port. The output structure is CMOS output When this port is selected for input, pull-up transistor can be connected in units of 4-bit This port is in common with analog input pins IN_0~IN_3.
	EPROM	Address input A_0~A_3	Input	Port P2 works as the lower 4-bit address input (A_0~A_3)
$P3_0$~$P3_3$	Single-chip	Input port P3	Input	Port P3 is an 4-bit input port $P3_0$, $P3_1$ are in common with external interrupt input pins INT_0, INT_1 and $P3_2$, $P3_3$ are in common with timer input pins $CNTR_0$, $CNTR_1$
	EPROM	Address input A_{11}, A_{12} Select mode V_{PP} input	Input	$P3_0$, $P3_1$ works as the 2-bit address input (A_{11}, A_{12}) $P3_2$ works as $\overline{OE}$ input Connect to $P3_3$ to V_{PP} when programming or verifing
$P4_0$, $P4_1$	Single-chip	I/O port P4	I/O	Port P4 is an 2-bit I/O port The output structure is CMOS output When this port is selected for input, pull-up transistor can be connected in units of 2-bit
	EPROM	Address input A_{13}, A_{14}	Input	Port P4 works as the higher 2-bit address input (A_{13}, A_{14})
V_{REF}	Single-chip	Reference voltage input	Input	This is the reference voltage input pin for the A-D converter
	EPROM	Select mode	Input	V_{REF} works as $\overline{CE}$ input

EPROM MODE

The M37470E4-XXXSP, M37470E8-XXXSP feature an EPROM mode in addition to its normal modes. When the $\overline{\text{RESET}}$ signal level is low ("L"), the chip automatically enters the EPROM mode. Table 1 list the correspondence between pins and Figure 1 gives the pin connection in the EPROM mode. When in the EPROM mode, ports P0, $P1_1$~$P1_7$, P2, P3, P4, V_{REF} are used for the PROM (equivalent to the M5L27256). When in this mode, the built-in PROM can be written to or read from using these pins in the same way as with the M5L27256. The oscillator should be connected to the X_{IN} and X_{OUT} pins, or external clock should be connected to the X_{IN} pin.

Table 1. Pin function in EPROM mode

	M37470E4-XXXSP, M37470E8-XXXSP	M5L27256
V_{CC}	V_{CC}	V_{CC}
V_{PP}	$P3_3$	V_{PP}
V_{SS}	V_{SS}	V_{SS}
Address input	Ports $P1_1$~$P1_7$, $P2_0$~$P2_3$ $P3_0$, $P3_1$, $P4_0$, $P4_1$	A_0~A_{14}
Data I/O	Port P0	D_0~D_7
$\overline{\text{CE}}$	V_{REF}	$\overline{\text{CE}}$
$\overline{\text{OE}}$	$P3_2$	$\overline{\text{OE}}$

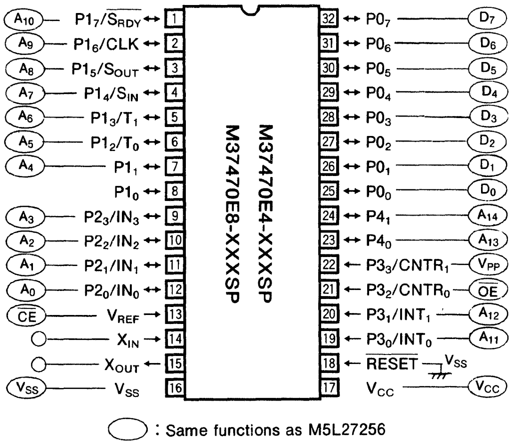


Fig.1 Pin connection in EPROM mode

PROM READING AND WRITING

Reading

To read the PROM, set the $\overline{CE}$ and $\overline{OE}$ pins to a "L" level. Input the address of the data ($A_0 \sim A_{14}$) to be read and the data will be output to the I/O pins $D_0 \sim D_7$. The data I/O pins will be floating when either the $\overline{CE}$ or $\overline{OE}$ pin is in the "H" state.

Writing

To write to the PROM, set the $\overline{OE}$ pin to a "H" level. The CPU will enter the program mode when V_{PP} is applied to the V_{PP} pin. The address to be written to is selected with pins $A_0 \sim A_{14}$, and the data to be written is input to pins $D_0 \sim D_7$. Set the $\overline{CE}$ pin to a "L" level to begin writing.

Notes on Writing

- ● M37470E4-XXXSP

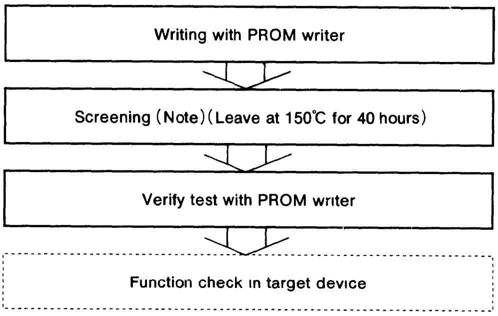
  When using a PROM writer, the address range should be between 6000_{16} and $7FFF_{16}$. Read/write operations on addresses 0000_{16} to $5FFF_{16}$ cannot be performed correctly.
- ● M37470E8-XXXSP

  When using a PROM writer, the address range should be between 4000_{16} and $7FFF_{16}$. When data is written between addresses 0000_{16} and $7FFF_{16}$, fill addresses 0000_{16} to $3FFF_{16}$ with FF_{16}.

NOTES ON HANDLING

(1) Since a high voltage (12.5V) is used to write data, care should be taken when turning on the PROM writer's power.

(2) For the programmable microcomputer (shipped in blank or OTP type), Mitsubishi does not perform PROM write test and screening in the assembly process and following processes. To improve reliability after write, performing write and test according to the flow below before use is recommended.



Note : Since the screening temperature is higher than storage temperature, never expose to 150℃ exceeding 100 hours.

Table 2. I/O signal in each mode

Pin / Mode	$\overline{CE}$(13)	$\overline{OE}$(21)	V_{PP}(22)	V_{CC}(17)	Data I/O (25~32)
Read-out	V_{IL}	V_{IL}	V_{CC}	V_{CC}	Output
Output disable	V_{IL}	V_{IH}	V_{CC}	V_{CC}	Floating
Programming	V_{IL}	V_{IH}	V_{PP}	V_{CC}	Input
Programming verify	V_{IH}	V_{IL}	V_{PP}	V_{CC}	Output
Program disable	V_{IH}	V_{IH}	V_{PP}	V_{CC}	Floating

Note 1 : V_{IL} and V_{IH} indicate a "L" and "H" input voltage, respectively

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS} Output transistors are at "OFF" state	$-0.3 \sim 7$	V
V_I	Input voltage X_{IN}		$-0.3 \sim V_{CC}+0.3$	V
V_I	Input voltage $P0_0 \sim P0_7$, $P1_0 \sim P1_7$, $P2_0 \sim P2_3$, $P3_0 \sim P3_3$, $P4_0$, $P4_1$, V_{REF}, $\overline{RESET}$		$-0.3 \sim V_{CC}+0.3$ (Note 1)	V
V_O	Output voltage $P0_0 \sim P0_7$, $P1_0 \sim P1_7$, $P2_0 \sim P2_3$, $P4_0$, $P4_1$, X_{OUT}		$-0.3 \sim V_{CC}+0.3$	V
Pd	Power dissipation	$T_a = 25°C$	1000	mW
Topr	Operating temperature		$-20 \sim 85$	℃
Tstg	Storage temperature		$-40 \sim 150$	℃

Note 1 : In EPROM programming mode, $P3_3$ is 13V

RECOMMENDED OPERATING CONDITIONS

($V_{CC}=2.7 \sim 5.5V$, $V_{SS}=0V$, $Ta=-20 \sim 85°C$ unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max.	
V_{CC}	Supply voltage	2.7	5	5.5	V
V_{SS}	Supply voltage		0		V
V_{IH}	"H" input voltage $P0_0 \sim P0_7$, $P1_0 \sim P1_7$, $P3_0 \sim P3_3$, $\overline{RESET}$, X_{IN}	$0.8V_{CC}$		V_{CC}	V
V_{IH}	"H" input voltage $P2_0 \sim P2_3$, $P4_0$, $P4_1$	$0.7V_{CC}$		V_{CC}	V
V_{IL}	"L" input voltage $P0_0 \sim P0_7$, $P1_0 \sim P1_7$, $P3_0 \sim P3_3$	0		$0.2V_{CC}$	V
V_{IL}	"L" input voltage $P2_0 \sim P2_3$, $P4_0$, $P4_1$	0		$0.25V_{CC}$	V
V_{IL}	"L" input voltage $\overline{RESET}$	0		$0.12V_{CC}$	V
V_{IL}	"L" input voltage X_{IN}	0		$0.16V_{CC}$	V
$I_{OH(sum)}$	"H" sum output current $P0_0 \sim P0_7$, $P4_0$, $P4_1$			-30	mA
$I_{OH(sum)}$	"H" sum output current $P1_0 \sim P1_7$, $P2_0 \sim P2_3$			-30	mA
$I_{OL(sum)}$	"L" sum output current $P0_0 \sim P0_7$, $P4_0$, $P4_1$			60	mA
$I_{OL(sum)}$	"L" sum output current $P1_0 \sim P1_7$, $P2_0 \sim P2_3$			60	mA
$I_{OL(peak)}$	"L" peak output current $P0_0 \sim P0_7$, $P1_0 \sim P1_7$, $P2_0 \sim P2_3$, $P4_0$, $P4_1$			20	mA
$I_{OL(avg)}$	"L" average output current $P0_0 \sim P0_7$, $P1_0 \sim P1_7$, $P2_0 \sim P2_3$, $P4_0$, $P4_1$ (Note 2)			10	mA
$I_{OH(peak)}$	"H" peak output current $P0_0 \sim P0_7$, $P1_0 \sim P1_7$, $P2_0 \sim P2_3$, $P4_0$, $P4_1$			-10	mA
$I_{OH(avg)}$	"H" average output current $P0_0 \sim P0_7$, $P1_0 \sim P1_7$, $P2_0 \sim P2_3$, $P4_0$, $P4_1$ (Note 2)			-5	mA
$f_{(CNTR)}$	Timer input frequency $CNTR_0$ ($P3_2$), $CNTR_1$ ($P3_3$) (Note 1)			1	MHz
$f_{(CLK)}$	Serial I/O clock input frequency CLK ($P1_6$) (Note 1)			1	MHz
$f(X_{IN})$	Clock oscillating frequency (Note 1)			4	MHz

Note 1 : Oscillation frequency is at 50% duty cycle.
2 : The average output current $I_{OH(avg)}$ and $I_{OL(avg)}$ are the average value during a 100ms

ELECTRICAL CHARACTERISTICS (V_{CC}=2.7~5.5V, V_{SS}=0V, T_a=−20~85℃, unless otherwise noted)

Symbol	Parameter	Test Conditions		Limits			Unit
				Min	Typ	Max	
V_{OH}	"H" output voltage $P0_0 \sim P0_7$, $P1_0 \sim P1_7$, $P2_0 \sim P2_3$, $P4_0$, $P4_1$	V_{CC}=5V, I_{OH}=−5mA		3			V
		V_{CC}=3V, I_{OH}=−1.5mA		2			
V_{OL}	"L" output voltage $P0_0 \sim P0_7$, $P1_0 \sim P1_7$, $P2_0 \sim P2_3$, $P4_0$, $P4_1$	V_{CC}=5V, I_{OL}=10mA				2	V
		V_{CC}=3V, I_{OL}=3mA				1	
$V_{T+}-V_{T-}$	Hysteresis $P0_0 \sim P0_7$, $P3_0 \sim P3_3$	V_{CC}=5V			0.5		V
		V_{CC}=3V			0.3		
$V_{T+}-V_{T-}$	Hysteresis $\overline{\text{RESET}}$	V_{CC}=5V			0.5		V
		V_{CC}=3V			0.3		
$V_{T+}-V_{T-}$	Hysteresis $P1_6$/CLK	use as CLK input	V_{CC}=5V		0.5		V
			V_{CC}=3V		0.3		
I_{IL}	"L" input current $P0_0 \sim P0_7$, $P1_0 \sim P1_7$, $P3_0 \sim P3_2$, $P4_0$, $P4_1$	V_I=0V, not use pull-up transistor	V_{CC}=5V			−5	µA
			V_{CC}=3V			−3	
		V_I=0V, use pull-up transistor	V_{CC}=5V	−0.25	−0.5	−1.0	mA
			V_{CC}=3V	−0.08	−0.18	−0.35	
I_{IL}	"L" input current $P3_3$	V_I=0V	V_{CC}=5V			−5	µA
			V_{CC}=3V			−3	
I_{IL}	"L" input current $P2_0 \sim P2_3$	V_I=0V, not use as analog input, not use pull-up transistor	V_{CC}=5V			−5	µA
			V_{CC}=3V			−3	
		V_I=0V, not use as analog input, use pull-up transistor	V_{CC}=5V	−0.25	−0.5	−1.0	mA
			V_{CC}=3V	−0.08	−0.18	−0.35	
I_{IL}	"L" input current $\overline{\text{RESET}}$, X_{IN}	V_I=0V (X_{IN} is at stop mode)	V_{CC}=5V			−5	µA
			V_{CC}=3V			−3	
I_{IH}	"H" input current $P0_0 \sim P0_7$, $P1_0 \sim P1_7$, $P3_0 \sim P3_2$, $P4_0$, $P4_1$	V_I=V_{CC}, not use pull-up transistor	V_{CC}=5V			5	µA
			V_{CC}=3V			3	
I_{IH}	"H" input current $P3_3$	V_I=V_{CC}	V_{CC}=5V			5	µA
			V_{CC}=3V			3	
I_{IH}	"H" input current $P2_0 \sim P2_3$	V_I=V_{CC}, not use as analog input, not use pull-up transistor	V_{CC}=5V			5	µA
			V_{CC}=3V			3	
I_{IH}	"H" input current $\overline{\text{RESET}}$, X_{IN}	V_I=V_{CC}, (X_{IN} is at stop mode)	V_{CC}=5V			5	µA
			V_{CC}=3V			3	
I_{CC}	Supply current	At normal operation, A-D conversion is not executed X_{IN}=4MHz	V_{CC}=5V		3.5	7	mA
			V_{CC}=3V		1.8	3.6	
		At normal operation, A-D conversion is executed X_{IN}=4MHz	V_{CC}=5V		4	8	
			V_{CC}=3V		2	4	
		At wait mode, X_{IN}=4MHz	V_{CC}=5V		1	2	
			V_{CC}=3V		0.5	1	
		Stop all oscillation V_{CC}=5V	T_a=25℃		0.1	1	µA
			T_a=85℃		1	10	
V_{RAM}	RAM retention voltage	Stop all oscillation		2			V

A-D CONVERTER CHARACTERISTICS (V_{CC}=2.7~5.5V, V_{SS}=0V, T_a=−20~85℃, f(X_{IN})=4MHz, unless otherwise noted)

Symbol	Parameter	Test Conditions	Limits			Unit
			Min	Typ	Max	
—	Resolution				8	bits
—	Non-linearity error				±2	LSB
—	Differential non-linearity error				±0.9	LSB
V_{OT}	Zero transition error	V_{CC}=V_{REF}=5.12V, $I_{OL(sum)}$=0mA			2	LSB
		V_{CC}=V_{REF}=3.072V, $I_{OL(sum)}$=0mA			3	
V_{FST}	Full-scale transition error	V_{CC}=V_{REF}=5.12V			4	LSB
		V_{CC}=V_{REF}=3.072V			7	
t_{CONV}	Conversion time				25	µs
V_{VREF}	Reference input voltage		0.5V_{CC}		V_{CC}	V
R_{LADDER}	Ladder resistance value		2	5	10	kΩ
V_{IA}	Analog input voltage		0		V_{REF}	V

M37471E4-XXXSP/FP
M37471E8-XXXSP/FP,M37471E8SS

PROM VERSION of M37471M4-XXXSP/FP,M37471M8-XXXSP/FP

DESCRIPTION

The M37471E4-XXXSP/FP is a single-chip microcomputer designed with CMOS silicon gate technology. It is housed in a 42-pin shrink plastic molded DIP or a 56-pin plastic molded QFP. The features of this chip are similar to those of the M37471M4-XXXSP/FP except that this chip has a 8192 bytes PROM built-in. This single-chip microcomputer is useful for home electrical appliances and consumer appliance controllers.

In addition to its simple instruction sets, the PROM, RAM, and I/O addresses are placed on the same memory map to enable easy programming. Since general purpose PROM writers can be used for the built-in PROM, this chip is suitable for small quantity production runs.

The differences between the M37471E4-XXXSP/FP and the M37471E8-XXXSP/FP are noted below. The M37471E8SS are the window type. The following explanations apply to the M37471E4-XXXSP/FP.

Specification variations for other chips are noted accordingly.

Type name	ROM size	RAM size
M37471E4-XXXSP/FP	8192 bytes	192 bytes
M37471E8-XXXSP/FP M37471E8SS	16384 bytes	384 bytes

The differences between the M37471E4-XXXSP and the M37471E4-XXXFP are the package outline and the power dissipation ability (absolute maximum ratings).

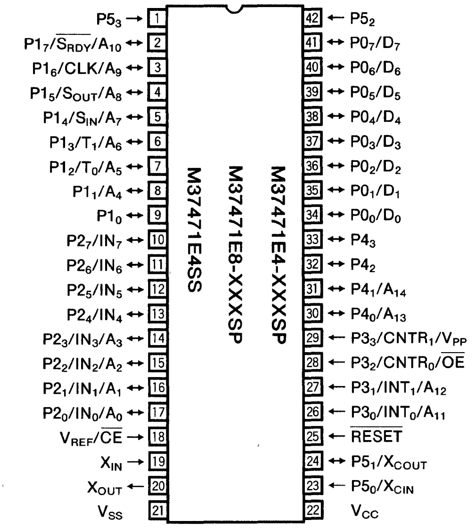
FEATURES

- Number of basic instructions ········· 69
- Memory size PROM ········· 8192 bytes (M37471E4)
  16384 bytes (M37471E8)
  RAM ········· 192 bytes (M37471E4)
  384 bytes (M37471E8)
- Instruction execution time
  ······· 1μs (minimum instructions at 4MHz frequency)
- Single power supply ········· 2.7~5.5V
- Power dissipation
  normal operation mode (at 4MHz frequency) 17.5mW
- Subroutine nesting ········· 96 levels max. (M37471E4)
- Interrupt ········· 12 types, 10 vectors
- 8-bit timer ········· 4
- Serial I/O ········· 8-bit×1
- Programmable I/O ports (Ports P0, P1, P2, P4) ········· 28
- Input ports (Port P3, P5) ········· 8
- A-D converter ········· 8-bit, 8-channel
- Two clock generator circuits
  (One is for main clock, the other is for clock function)
- PROM (equivalent to the M5L27256)
  program voltage ········· 12.5V

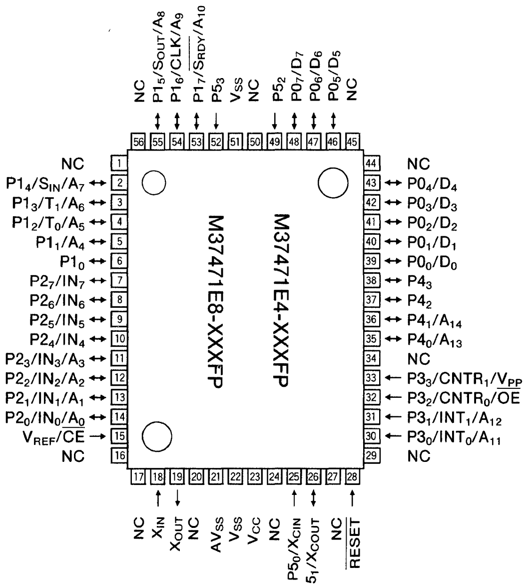
APPLICATION

Office automation equipment, VCR, Tuner, Audio-visual equipment

PIN CONFIGURATION (TOP VIEW)



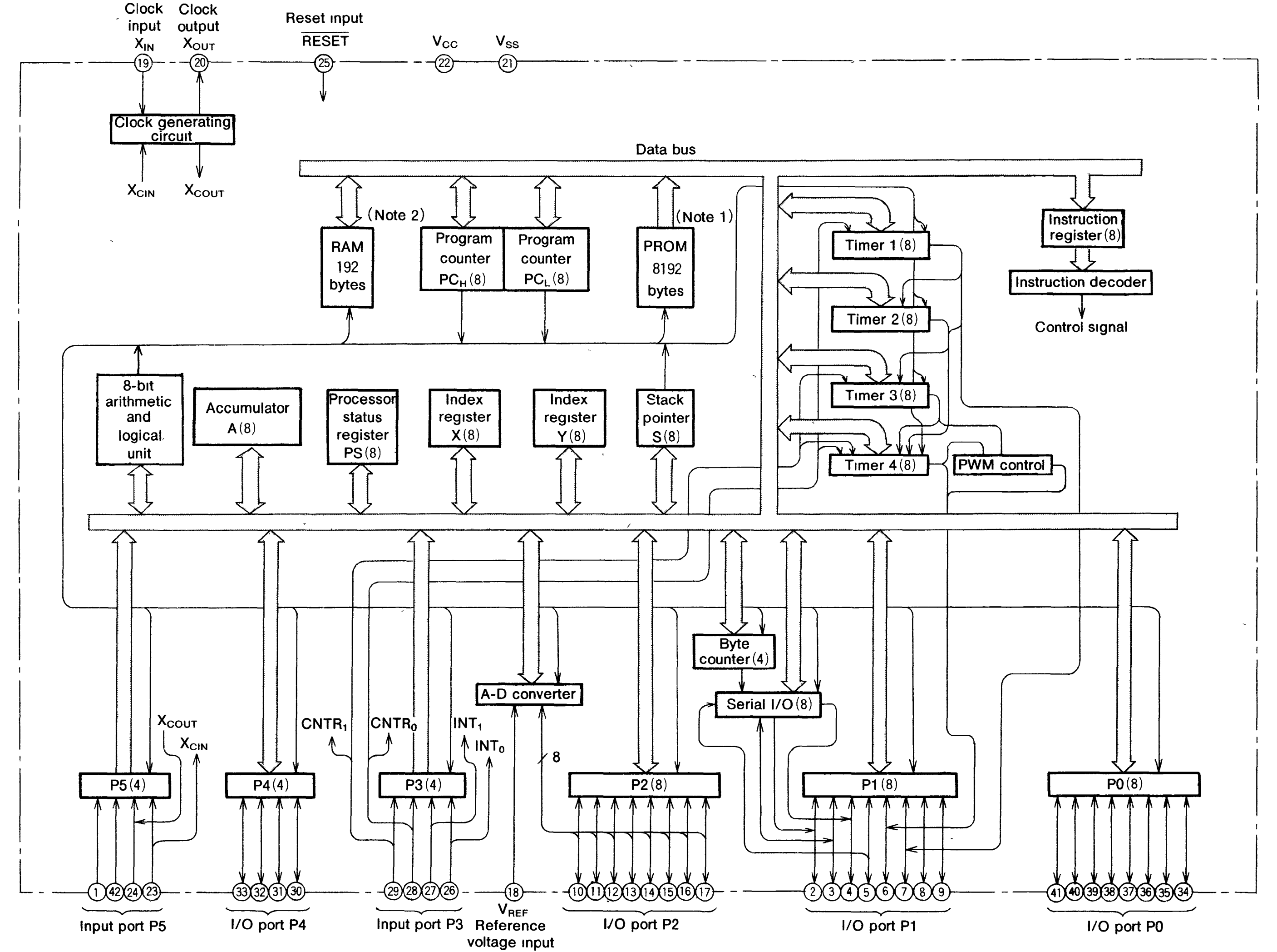
Outline 42P4B (OTP)
42S1B (Window)



Outline 56P6N

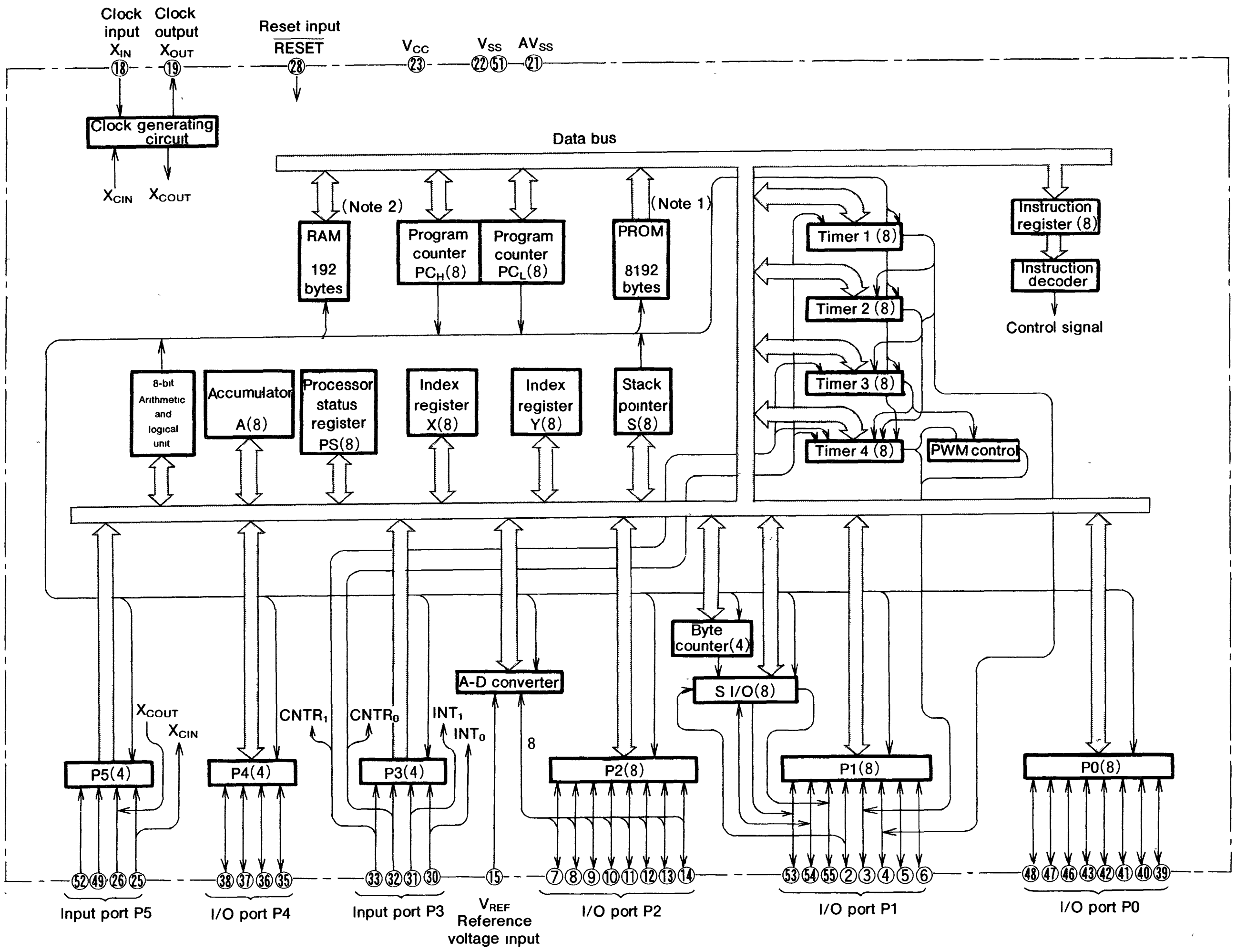
NC : No connection

M37471E4-XXXSP BLOCK DIAGRAM



Note 1 : 16384 bytes for M37471E8-XXXSP, M37471E8SS
2 : 384 bytes for M37471E8-XXXSP, M37471E8SS

M37471E4-XXXFP BLOCK DIAGRAM



Note 1 : 16384 bytes for M37471E8-XXXFP
2 : 384 bytes for M37471E8-XXXFP

FUNCTIONS OF M37471E4-XXXSP/FP, M37471E8-XXXSP/FP, M37471E8SS

Parameter			Functions
Number of basic instructions			69
Instruction execution time			1μs (minimum instructions, at 4MHz frequency)
Clock frequency			4MHz (main clock input), 32kHz (for clock function).
Memory size	M37471E4-XXXSP/FP	PROM	8192 bytes (Note 1)
		RAM	192 bytes
	M37471E8-XXXSP/FP	PROM	16384 bytes (Note 1)
	M37471E8SS	RAM	384 bytes
Input/Output port	P0, P1, P2	I/O	8-bit×3
	P3, P5	Input	4-bit×2
	P4	I/O	4-bit×1
Serial I/O			8-bit×1
Timers			8-bit timer×4
A-D converter			8-bit×1 (8channel)
Subroutine nesting	M37471E4-XXXSP/FP		96 levels (max)
	M37471E8-XXXSP/FP, M37471E8SS		192 levels (max)
Interrupt			Five external interrupts, six internal interrupts, one software interrupt
Clock generating circuit			Two built-in circuits with internal feedback resistor (ceramic or quartz crystal oscillator)
Supply voltage			2 7~5 5V
Power dissipation	At high-speed operation		17 5mW (at $f(X_{IN})=4MHz$)
	At low-speed operation		0 15mW (at $f(X_{CIN})=32kHz$)
	At stop mode		0 5μW (at clock stop)
Input/Output characteristics	Input/Output voltage		5V
	Output current		−5~10mA (ports P0, P1, P2, P4 CMOS tri-state output)
Operating temperature range			−20~85℃
Device structure			CMOS Silicon gate
Package	M37471E4-XXXSP		42-pin shrink plastic molded DIP
	M37471E8-XXXSP		
	M37471E4-XXXFP		56-pin plastic molded QFP
	M37471E8-XXXFP		
	M37471E8SS		42-pin shrink ceramic DIP

Note 1 : The PROM programming voltage is 12.5V (equivalent to the M5L27256)

PIN DESCRIPTION

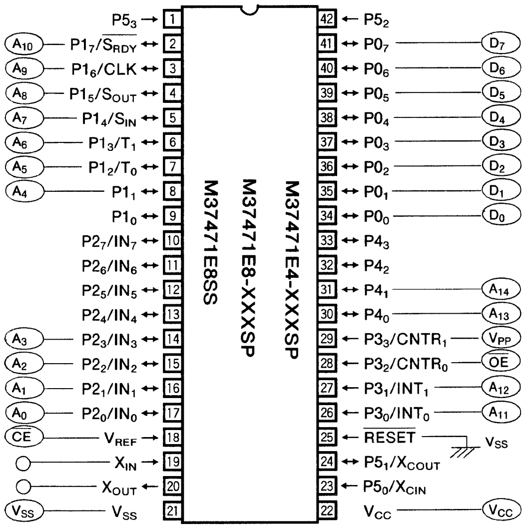
Pin	Mode	Name	Input/ Output	Functions
V_{CC}, V_{SS}	Single-chip /EPROM	Supply voltage		Power supply inputs 2 7~5 5V to V_{CC} and 0V to V_{SS}
AV_{SS}	Single-chip /EPROM	Analog power supply		Ground level input pin for A-D converter Same voltage as V_{SS} is applied This pin is for 56-pin model only
$\overline{RESET}$	Single-chip	RESET input	Input	To reset, keep this input terminal low for more than 2μs (min) under normal V_{CC} conditions
	EPROM	RESET input		Connect to V_{SS}
X_{IN}	Single-chip /EPROM	Clock input	Input	Connect a ceramic or a quartz crystal oscillator between X_{IN} and X_{OUT} for clock oscillation If an external clock input is used, connect the clock input to the X_{IN} pin and open the X_{OUT} pin Feedback resistor is connected between the X_{IN} and X_{OUT} pins
X_{OUT}		Clock output	Output	
$P0_0$~$P0_7$	Single-chip	I/O port P0	I/O	Port P0 is an 8-bit I/O port The output structure is CMOS output When this port is selected for input, pull-up transistor can be connected in units of 1-bit and a key on wake up function is provided
	EPROM	Data input/output D_0~D_7	I/O	Port P0 works as an 8-bit data bus (D_0~D_7)
$P1_0$~$P1_7$	Single-chip	I/O port P1	I/O	Port P1 is an 8-bit I/O port The output structure is CMOS output When this port is selected for input, pull-up transistor can be connected in units of 4-bit $P1_2$, $P1_3$ are in common with timer output pins T_0, T_1 $P1_4$, $P1_5$, $P1_6$, $P1_7$ are in common with serial I/O pins S_{IN}, S_{OUT}, CLK, $\overline{S_{RDY}}$, respectively The output structure of S_{OUT} and $\overline{S_{RDY}}$ can be changed to N-channel open drain output
	EPROM	Address input A_4~A_{10}	Input	$P1_1$~$P1_7$ works as the 7-bit address input (A_4~A_{10}) $P1_0$ must be opened
$P2_0$~$P2_7$	Single-chip	I/O port P2	I/O	Port P2 is an 8-bit I/O port The output structure is CMOS output When this port is selected for input, pull-up transistor can be connected in units of 4-bit This port is in common with analog input pins IN_0~IN_7.
	EPROM	Address input A_0~A_3	Input	$P2_0$~$P2_3$ works as the lower 4-bit address input (A_0~A_3) $P2_4$~$P2_7$ must be opened.
$P3_0$~$P3_3$	Single-chip	Input port P3	Input	Port P3 is an 4-bit input port $P3_0$, $P3_1$ are in common with external interrupt input pins INT_0, INT_1 and $P3_2$, $P3_3$ are in common with timer input pins $CNTR_0$, $CNTR_1$
	EPROM	Address input A_{11}, A_{12} Select mode V_{PP} input	Input	$P3_0$, $P3_1$ works as the 2-bit address input (A_{11}, A_{12}) $P3_2$ works as $\overline{OE}$ input Connect to $P3_3$ to V_{PP} when programming or verifing
$P4_0$~$P4_3$	Single-chip	I/O port P4	I/O	Port P4 is an 4-bit I/O port The output structure is CMOS output When this port is selected for input, pull-up transistor can be connected in units of 4-bit
	EPROM	Address input A_{13}, A_{14}	Input	$P4_0$, $P4_1$ works as the higher 2-bit address input (A_{13}, A_{14}) $P4_2$, $P4_3$ must be opened
$P5_0$~$P5_3$	Single-chip	Input port P5	Input	Port P5 is an 4-bit input port and pull-up transistor can be connected in units of 4-bit $P5_0$, $P5_1$ are in common with input/output pins of clock for clock function X_{CIN}, X_{COUT}. When $P5_0$, $P5_1$ are used as X_{CIN}, X_{COUT}, connect a ceramic or a quartz crystal oscillator between X_{CIN} and X_{COUT} If an external clock input is used, connect the clock input to the X_{CIN} pin and open the X_{COUT} pin Feedback resistor is connected between X_{CIN} and X_{COUT} pins
	EPROM			Open
V_{REF}	Single-chip	Reference voltage input	Input	This is the reference voltage input pin for the A-D converter
	EPROM	Select mode	Input	V_{REF} works as $\overline{CE}$ input

EPROM MODE

The M37471E4-XXXSP/FP, M37471E8-XXXSP/FP, M37471E8SS feature an EPROM mode in addition to its normal modes. When the $\overline{\text{RESET}}$ signal level is low ("L"), the chip automatically enters the EPROM mode. Table 1 list the correspondence between pins and Figure 1, 2 gives the pin connection in the EPROM mode. When in the EPROM mode, ports P0, $P1_1 \sim P1_7$, $P2_0 \sim P2_3$, P3, $P4_0$, $P4_1$, V_{REF} are used for the PROM (equivalent to the M5L27256). When in this mode, the built-in PROM can be written to or read from using these pins in the same way as with the M5L27256. The oscillator should be connected to the X_{IN} and X_{OUT} pins, or external clock should be connected to the X_{IN} pin.

Table 1. Pin function in EPROM mode

	M37471E4-XXXSP/FP, M37471E8-XXXSP/FP, M37471E8SS	M5L27256
V_{CC}	V_{CC}	V_{CC}
V_{PP}	$P3_3$	V_{PP}
V_{SS}	V_{SS}	V_{SS}
Address input	Ports $P1_1 \sim P1_7$, $P2_0 \sim P2_3$ $P3_0$, $P3_1$, $P4_0$, $P4_1$	$A_0 \sim A_{14}$
Data I/O	Port P0	$D_0 \sim D_7$
$\overline{\text{CE}}$	V_{REF}	$\overline{\text{CE}}$
$\overline{\text{OE}}$	$P3_2$	$\overline{\text{OE}}$



: Same functions as M5L27256

Fig.1 Pin connection in EPROM mode (42-pin model)

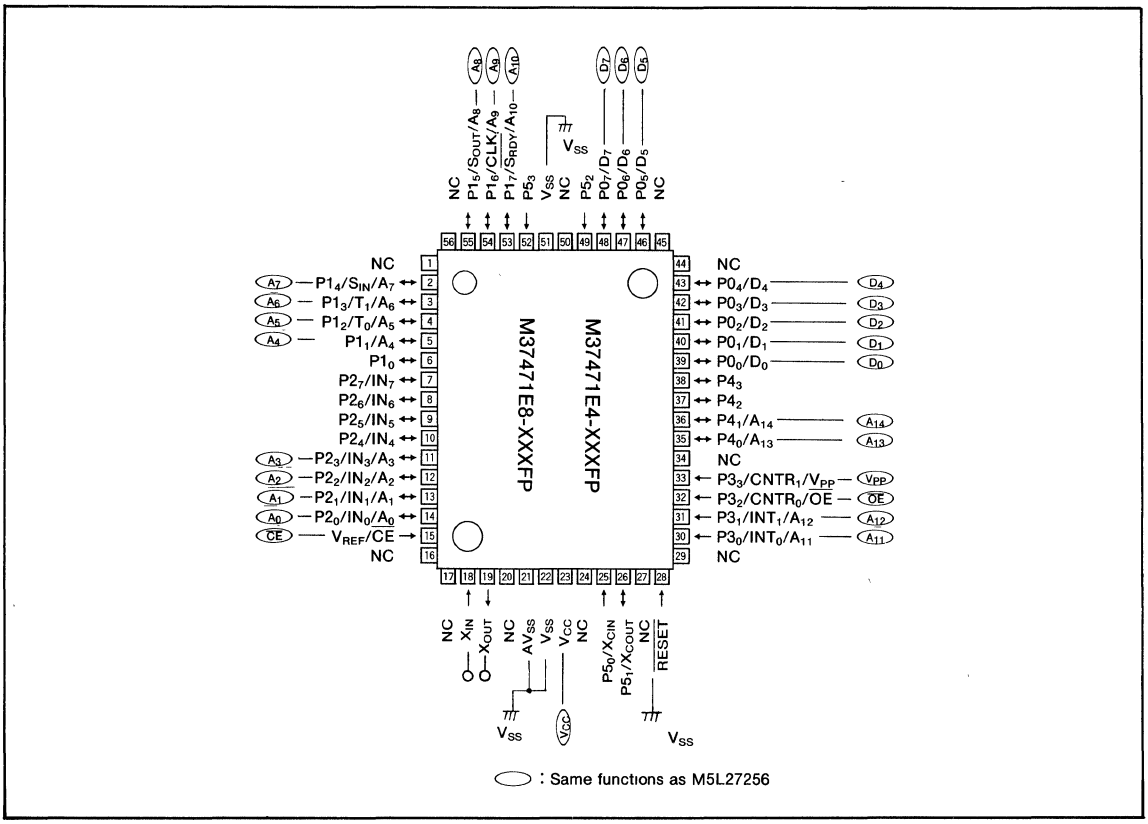


Fig. 2 Pin connection in EPROM mode (56-pin model)

PROM READING AND WRITING

Reading

To read the PROM, set the $\overline{CE}$ and $\overline{OE}$ pins to a "L" level. Input the address of the data ($A_0 \sim A_{14}$) to be read and the data will be output to the I/O pins $D_0 \sim D_7$. The data I/O pins will be floating when either the $\overline{CE}$ or $\overline{OE}$ pin is in the "H" state.

Writing

To write to the PROM, set the $\overline{OE}$ pin to a "H" level. The CPU will enter the program mode when V_{PP} is applied to the V_{PP} pin. The address to be written to is selected with pins $A_0 \sim A_{14}$, and the data to be written is input to pins $D_0 \sim D_7$. Set the $\overline{CE}$ pin to a "L" level to begin writing.

Notes on Writing

- M37471E4-XXXSP/FP

When using a PROM writer, the address range should be between 6000_{16} and $7FFF_{16}$. Read/write operations on addresses 0000_{16} to $5FFF_{16}$ cannot be performed correctly.

- M37471E8-XXXSP/FP, M37471E8SS

When using a PROM writer, the address range should be between 4000_{16} and $7FFF_{16}$. When data is written between addresses 0000_{16} and $7FFF_{16}$, fill addresses 0000_{16} to $3FFF_{16}$ with FF_{16}.

Erasing

Data can only erased on the M37471E8SS ceramic package, which includes a window. To erase data on this chip, use an ultraviolet light source with a 2537 Angstrom wave length. The minimum radiation power necessary for erasing is 15W・s/cm^2.

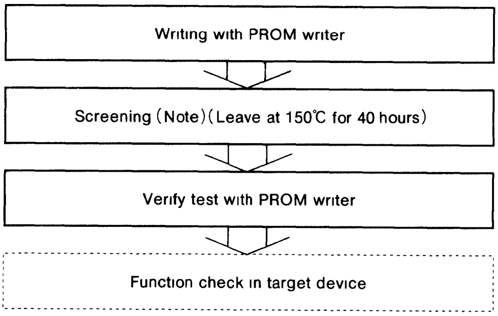
NOTES ON HANDLING

(1) Sunlight and fluorescent light contain wave lengths capable of erasing data. For ceramic package types, cover the transparent window with a seal (provided) when this chip is in use. However, this seal must not contact the lead pins.

(2) Before erasing, the glass should be cleaned and stains such as finger prints should be removed thoroughly. If these stains are not removed, complete erasure of the data could be prevented.

(3) Since a high voltage (12.5V) is used to write data, care should be taken when turning on the PROM writer's power.

(4) For the programmable microcomputer (shipped in blank or OTP type), Mitsubishi does not perform PROM write test and screening in the assembly process and following processes. To improve reliability after write, performing write and test according to the flow below before use is recommended.



Note : Since the screening temperature is higher than storage temperature, never expose to 150℃ exceeding 100 hours.

Table 2. I/O signal in each mode

Pin Mode	$\overline{CE}$	$\overline{OE}$	V_{PP}	V_{CC}	Data I/O
Read-out	V_{IL}	V_{IL}	V_{CC}	V_{CC}	Output
Output disable	V_{IL}	V_{IH}	V_{CC}	V_{CC}	Floating
Programming	V_{IL}	V_{IH}	V_{PP}	V_{CC}	Input
Programming verify	V_{IH}	V_{IL}	V_{PP}	V_{CC}	Output
Program disable	V_{IH}	V_{IH}	V_{PP}	V_{CC}	Floating

Note 1 : V_{IL} and V_{IH} indicate a "L" and "H" input voltage, respectively

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS} Output transistors are at "OFF" state	$-0.3 \sim 7$	V
V_I	Input voltage X_{IN}		$-0.3 \sim V_{CC}+0.3$	V
V_I	Input voltage $P0_0 \sim P0_7$, $P1_0 \sim P1_7$, $P2_0 \sim P2_7$, $P3_0 \sim P3_3$, $P4_0 \sim P4_3$, $P5_0 \sim P5_3$, V_{REF}, $\overline{RESET}$		$-0.3 \sim V_{CC}+0.3$ (Note 1)	V
V_O	Output voltage $P0_0 \sim P0_7$, $P1_0 \sim P1_7$, $P2_0 \sim P2_7$, $P4_0 \sim P4_3$, X_{OUT}		$-0.3 \sim V_{CC}+0.3$	V
P_d	Power dissipation	$T_a = 25$℃	1000 (Note 2)	mW
Topr	Operating temperature		$-20 \sim 85$	℃
Tstg	Storage temperature		$-40 \sim 150$	℃

Note 1 : In EPROM programming mode, $P3_3$ is 13V
2 : 500mW for QFP type

RECOMMENDED OPERATING CONDITIONS

($V_{CC}=2.7 \sim 5.5$V, $V_{SS}=AV_{SS}=0$V, $Ta=-20 \sim 85$℃ unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ'	Max	
V_{CC}	Supply voltage	2.7	5	5.5	V
V_{SS}	Supply voltage		0		V
AV_{SS}	Analog supply voltage		0		V
V_{IH}	"H" Input voltage $P0_0 \sim P0_7$, $P1_0 \sim P1_7$, $P3_0 \sim P3_3$, $\overline{RESET}$, X_{IN}	$0.8V_{CC}$		V_{CC}	V
V_{IH}	"H" Input voltage $P2_0 \sim P2_7$, $P4_0 \sim P4_3$, $P5_0 \sim P5_3$ (Note 1)	$0.7V_{CC}$		V_{CC}	V
V_{IL}	"L" Input voltage $P0_0 \sim P0_7$, $P1_0 \sim P1_7$, $P3_0 \sim P3_3$	0		$0.2V_{CC}$	V
V_{IL}	"L" Input voltage $P2_0 \sim P2_7$, $P4_0 \sim P4_3$, $P5_0 \sim P5_3$ (Note 1)	0		$0.25V_{CC}$	V
V_{IL}	"L" Input voltage $\overline{RESET}$	0		$0.12V_{CC}$	V
V_{IL}	"L" Input voltage X_{IN}	0		$0.16V_{CC}$	V
$I_{OH(sum)}$	"H" sum output current $P0_0 \sim P0_7$, $P4_0 \sim P4_3$			-30	mA
$I_{OH(sum)}$	"H" sum output current $P1_0 \sim P1_7$, $P2_0 \sim P2_7$			-30	mA
$I_{OL(sum)}$	"L" sum output current $P0_0 \sim P0_7$, $P4_0 \sim P4_3$			60	mA
$I_{OL(sum)}$	"L" sum output current $P1_0 \sim P1_7$, $P2_0 \sim P2_7$			60	mA
$I_{OL(peak)}$	"L" peak output current $P0_0 \sim P0_7$, $P1_0 \sim P1_7$, $P2_0 \sim P2_7$, $P4_0 \sim P4_3$			20	mA
$I_{OL(avg)}$	"L" average output current $P0_0 \sim P0_7$, $P1_0 \sim P1_7$, $P2_0 \sim P2_7$, $P4_0 \sim P4_3$ (Note 4)			10	mA
$I_{OH(peak)}$	"H" peak output current $P0_0 \sim P0_7$, $P1_0 \sim P1_7$, $P2_0 \sim P2_7$, $P4_0 \sim P4_3$			-10	mA
$I_{OH(avg)}$	"H" average output current $P0_0 \sim P0_7$, $P1_0 \sim P1_7$, $P2_0 \sim P2_7$, $P4_0 \sim P4_3$ (Note 4)			-5	mA
$f_{(CNTR)}$	Timer input frequency $CNTR_0$ ($P3_2$), $CNTR_1$ ($P3_3$) (Note 2)			1	MHz
$f_{(CLK)}$	Serial I/O clock input frequency CLK ($P1_6$) (Note 2)			1	MHz
$f(X_{IN})$	Clock oscillating frequency (Note 2)			4	MHz
$f(X_{CIN})$	Clock oscillating frequency for clock function (Note 2, 3)		32	50	kHz

Note 1 : It is except to use $P5_0$ as X_{CIN}
2 : Oscillation frequency is at 50% duty cycle
3 : When used in the low-speed mode, the clock oscillating frequency for clock function should be $f(X_{CIN}) < f(X_{IN})/3$
4 : The average output current $I_{OH(avg)}$ and $I_{OL(avg)}$ are the average value during a 100ms

ELECTRICAL CHARACTERISTICS (V_{CC}=2.7~5.5V, V_{SS}=0V, T_a=−20~85℃, unless otherwise noted)

Symbol	Parameter	Test Conditions		Limits			Unit
				Min	Typ	Max	
V_{OH}	"H" output voltage $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_3$, $P4_0$~$P4_3$	V_{CC}=5V, I_{OH}=−5mA		3			V
		V_{CC}=3V, I_{OH}=−1.5mA		2			
V_{OL}	"L" output voltage $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_3$, $P4_0$~$P4_3$	V_{CC}=5V, I_{OL}=10mA				2	V
		V_{CC}=3V, I_{OL}=3mA				1	
$V_{T+}-V_{T-}$	Hysteresis $P0_0$~$P0_7$, $P3_0$~$P3_3$	V_{CC}=5V			0.5		V
		V_{CC}=3V			0.3		
$V_{T+}-V_{T-}$	Hysteresis $\overline{RESET}$	V_{CC}=5V			0.5		V
		V_{CC}=3V			0.3		
$V_{T+}-V_{T-}$	Hysteresis $P1_6$/CLK	use as CLK input	V_{CC}=5V		0.5		V
			V_{CC}=3V		0.3		
I_{IL}	"L" input current $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P3_0$~$P3_2$, $P4_0$~$P4_3$, $P5_0$~$P5_3$	V_I=0V, not use pull-up transistor	V_{CC}=5V			−5	μA
			V_{CC}=3V			−3	
		V_I=0V, use pull-up transistor	V_{CC}=5V	−0.25	−0.5	−1.0	mA
			V_{CC}=3V	−0.08	−0.18	−0.35	
I_{IL}	"L" input current $P3_3$	V_I=0V	V_{CC}=5V			−5	μA
			V_{CC}=3V			−3	
I_{IL}	"L" input current $P2_0$~$P2_7$	V_I=0V, not use as analog input, not use pull-up transistor	V_{CC}=5V			−5	μA
			V_{CC}=3V			−3	
		V_I=0V, not use as analog input, use pull-up transistor	V_{CC}=5V	−0.25	−0.5	−1.0	mA
			V_{CC}=3V	−0.08	−0.18	−0.35	
I_{IL}	"L" input current $\overline{RESET}$, X_{IN}	V_I=0V (X_{IN} is at stop mode)	V_{CC}=5V			−5	μA
			V_{CC}=3V			−3	
I_{IH}	"H" input current $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P3_0$~$P3_2$, $P4_0$~$P4_3$, $P5_0$~$P5_3$	V_I=V_{CC}, not use pull-up transistor	V_{CC}=5V			5	μA
			V_{CC}=3V			3	
I_{IH}	"H" input current $P3_3$	V_I=V_{CC}	V_{CC}=5V			5	μA
			V_{CC}=3V			3	
I_{IH}	"H" input current $P2_0$~$P2_7$	V_I=V_{CC}, not use as analog input, not use pull-up transistor	V_{CC}=5V			5	μA
			V_{CC}=3V			3	
I_{IH}	"H" input current $\overline{RESET}$, X_{IN}	V_I=V_{CC}, (X_{IN} is at stop mode)	V_{CC}=5V			5	μA
			V_{CC}=3V			3	
I_{CC}	Supply current	At normal operation, A-D conversion is not executed X_{IN}=4MHz	V_{CC}=5V		3.5	7	mA
			V_{CC}=3V		1.8	3.6	
		At normal operation, A-D conversion is not executed X_{IN}=4MHz	V_{CC}=5V		4	8	
			V_{CC}=3V		2	4	
		At low-speed mode, X_{COUT} is low-power mode, A-D conversion is not executed X_{IN}=0Hz, X_{CIN}=32kHz, T_a=25℃	V_{CC}=5V		30	80	μA
			V_{CC}=3V		15	40	
		At wait mode, X_{IN}=4MHz	V_{CC}=5V		1	2	mA
			V_{CC}=3V		0.5	1	
		At wait mode, X_{IN}=0Hz, X_{CIN}=32kHz, X_{COUT} is low-power mode, T_a=25℃	V_{CC}=5V		3	12	μA
			V_{CC}=3V		2	8	
		Stop all oscillation V_{CC}=5V	T_a=25℃		0.1	1	
			T_a=85℃		1	10	
V_{RAM}	RAM retention voltage	Stop all oscillation		2			V

A-D CONVERTER CHARACTERISTICS (V_{CC}=2.7~5.5V, V_{SS}=0V, T_a=−20~85℃, f(X_{IN})=4MHz, unless otherwise noted)

Symbol	Parameter	Test Conditions	Limits			Unit
			Min	Typ.	Max	
—	Resolution				8	bits
—	Non-linearity error				±2	LSB
—	Differential non-linearity error				±0.9	LSB
V_{OT}	Zero transition error	V_{CC}=V_{REF}=5.12V, $I_{OL(sum)}$=0mA			2	LSB
		V_{CC}=V_{REF}=3.072V, $I_{OL(sum)}$=0mA			3	
V_{FST}	Full-scale transition error	V_{CC}=V_{REF}=5.12V			4	LSB
		V_{CC}=V_{REF}=3.072V			7	
t_{CONV}	Conversion time				25	μs
V_{VREF}	Reference input voltage		0.5V_{CC}		V_{CC}	V
R_{LADDER}	Ladder resistance value		2	5	10	kΩ
V_{IA}	Analog input voltage		0		V_{REF}	V

MELPS 740 CPU CORE BASIC FUNCTIONS

MELPS 740 CPU CORE BASIC FUNCTIONS

Each series of the MELPS 740 Family uses the standard MELPS 740 instruction set. The functions of the MELPS 740 CPU core are explained below. The multiply and divide instructions are not available in every microcomputer, and the clock control instructions differ in each microcomputer. For details, refer to the table of machine instruction or the functional explanation of each microcomputer.

CENTRAL PROCESSING UNIT (CPU) INTERNAL REGISTERS

The central processing unit (CPU) has the six registers.

Accumulator (A)

The accumulator is an 8-bit register. Data operations such as data transfer, etc., are executed mainly through the accumulator.

Index register X (X), Index register Y (Y)

Both index register X and index register Y are 8-bit registers. In the index addressing modes, the value of the OPERAND is added to the contents of register X or register Y and specifies the real address.

These index registers also have increment, decrement, comparison, and data transfer functions to allow these registers to take some of the functions of the accumulator.

When the T flag in the processor status register is set to "1", the value contained in index register X becomes the address for the second OPERAND.

Stack pointer (S)

The stack pointer is an 8-bit register used during subroutine calls and interrupts. The stack is used to store the current address data and processor status when branching to subroutines or interrupt routines.

The lower eight bits of the stack address are determined by the contents of the stack pointer. The upper eight bits of the stack address are determined by the Stack Page Selection Bit. If the Stack Page Selection Bit is "0", then the RAM in the zero page is used as the stack area. If the Stack Page Selection Bit is "1", then RAM in page 1 is used as the stack area.

The Stack Page Selection Bit is located in the SFR area in the zero page. Note that the initial value of the Stack Page Selection Bit varies with each microcomputer type. Also some microcomputer types have no Stack Page Selection Bit and the upper eight bits of the stack address are fixed.

The operations of pushing register contents onto the stack and popping them from the stack are shown in Fig. 2

Program counter (PC)

The program counter is a 16-bit counter consisting of two 8-bit .registers PC_H and PC_L. It is used to indicate the address of the next instruction to be executed.

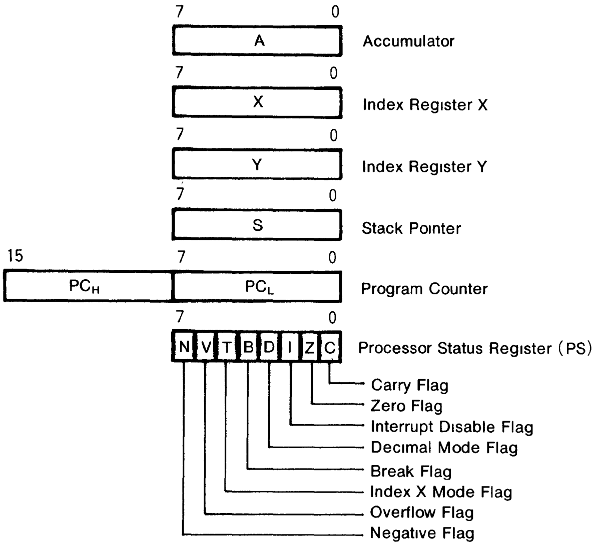
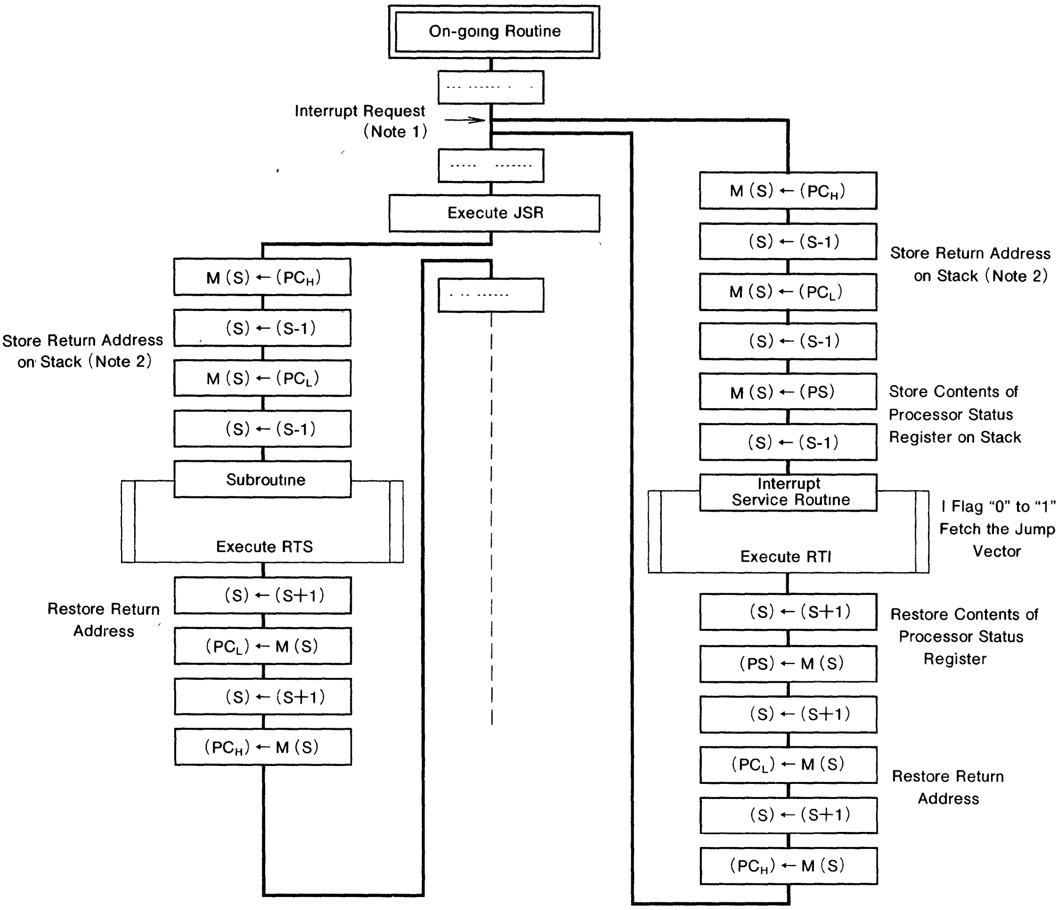


Fig. 1 MELPS 740 CPU register structure



Note 1 : The condition to enable the interrupt → Interrupt enable bit is "1"
Interrupt disable flag is "0"

2 : When an interrupt occurs, the address of the next instruction to be executed is stored in the stack area When a subroutine is called, the address one before the next instruction to be executed is stored in the stack area

Fig. 2 Register push and pop at interrupt generation and subroutine call

Table 1. Push and pop instructions of accumulator or processor status register

	Push instruction to stack	Pop instruction from stack
Accumulator	PHA	PLA
Processor status register	PHP	PLP

Processor status register (PS)

The processor status register is an 8-bit register consisting of flags which indicate the status of the processor after an arithmetic operation. Branch operations can be performed by testing the Carry (C) flag, Zero (Z) flag, Overflow (V) flag, or the Negative (N) flag. In decimal mode, the Z, V, N flags are not valid.

After reset, the Interrupt disable (I) flag is set to "1", but all other flags are undefined. Since the Index X mode (T) and Decimal mode (D) flags directly affect arithmetic operations, they should be initialized in the beginning of a program.

(1) Carry flag (C)
The C flag contains a carry or borrow generated by the arithmetic logic unit (ALU) immediately after an arithmetic operation. It can also be changed by a shift or rotate instruction.

(2) Zero flag (Z)
The Z flag is set if the result of an immediate arithmetic operation or a data transfer is "0", and cleared if the result is anything other than "0".

(3) Interrupt disable flag (I)
The I flag disables all interrupts except for the interrupt generated by the BRK instruction.
Interrupts are disabled when the I flag is "1".
When an interrupt occurs, this flag is automatically set to "1" to prevent other interrupts from interfering until the current interrupt is serviced.

(4) Decimal mode flag (D)
The D flag determines whether additions and subtractions are executed in binary or decimal. Binary arithmetic is executed when this flag is "0"; decimal arithmetic is executed when it is "1". Decimal correction is automatic in decimal mode. Only the ADC and SBC instructions can be used for decimal arithmetic.

(5) Break flag (B)
The B flag is used to indicate that the current interrupt was generated by the BRK instruction. The BRK flag in the processor status register is always "0". When the BRK instruction is used to generate an interrupt, the processor status register is pushed onto the stack with the break flag set to "1". The saved processor status is the only place where the break flag is ever set.

(6) Index X mode flag (T)
When the T flag is "0", arithmetic operations are performed between accumulator and memory, e.g. the results of an operation between two memory locations is stored in the accumulator. When the T flag is "1", direct arithmetic operations and direct data transfers are enabled between memory locations, i.e. between memory and memory, memory and I/O, and I/O and I/O. In this case, the result of an arithmetic operation performed on data in memory location 1 and memory location 2 is stored in memory location 1. The address of memory location 1 is specified by index register X, and the address of memory location 2 is specified by normal addressing modes.

(7) Overflow flag (V)
The V flag is used during the addition or subtraction of one byte of signed data. It is set if the result exceeds +127 to −128. When the BIT instruction is executed, bit 6 of the memory location operated on by the BIT instruction is stored in the overflow flag.

(8) Negative flag (N)
The N flag is set if the result of an arithmetic operation or data transfer is negative. When the BIT instruction is executed, bit 7 of the memory location operated on by the BIT instruction is stored in the negative flag

Table 2. Set and clear instructions of each bit of processor status register

	C flag	Z flag	I flag	D flag	B flag	T flag	V flag	N flag
Set instruction	SEC	—	SEI	SED	—	SET	—	—
Clear instruction	CLC	—	CLI	CLD	—	CLT	CLV	—

ADDRESSING MODE

The MELPS 740 Family has 17 addressing modes and a powerful memory access capability.

When extracting data required for arithmetic and logic operations from memory or when storing the results of such operations in memory, a memory address must be specified. The specification of the memory address is called addressing. The MELPS 740 Family instructions can be classified as 1-byte, 2-byte, and 3-byte instructions. In each case, the first byte is known as the OPCODE which forms the basis of the instruction. A second or third byte is called an OPERAND which affects the addressing. The contents of index registers X and Y can also effect the addressing.

Although there are many addressing modes, there is always a particular memory location specified. What differs is whether the operand, the index register contents, or a combination of both should be used to specify the memory or jump destination. Based on these 3 types of instructions, the range of variation is increased and operation is enhanced by combinations of the bit operation instructions, jump instruction, and arithmetic instructions.

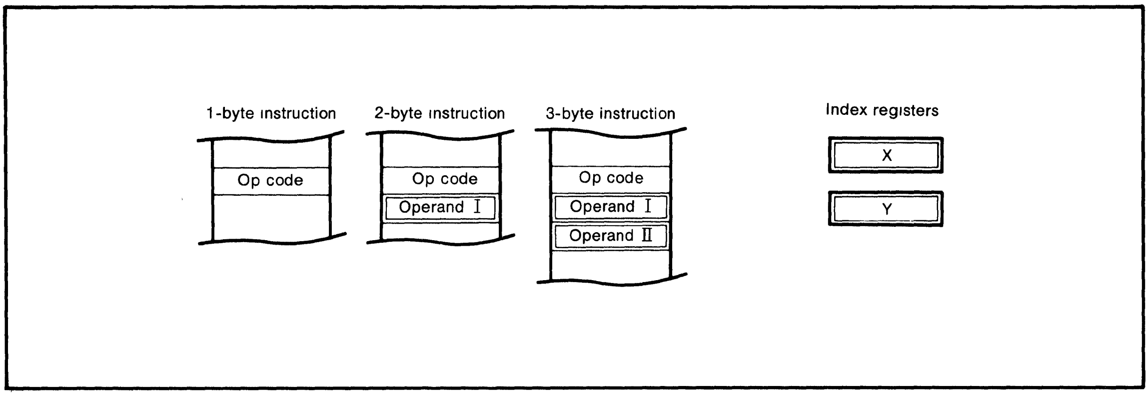
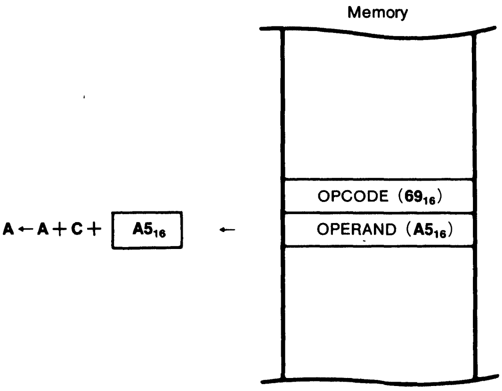
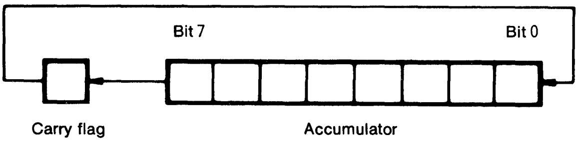


Fig. 3 Instruction byte configuration

Name : Immediate addressing mode
Function : The OPERAND follows immediately after the OPCODE.
Instructions : **ADC, AND, CMP, CPX, CPY, EOR, LDA, LDX, LDY, ORA, SBC**
Example : Mnemonic　　Machine code
ADC #$A5　　**$69_{16}$ $A5_{16}$**



Name : Accumulator addressing mode
Function : The operation is performed on the accumulator.
Instructions : **ASL, DEC, INC, LSR, ROL, ROR**
Example : Mnemonic　　Machine code
ROL A　　**$2A_{16}$**

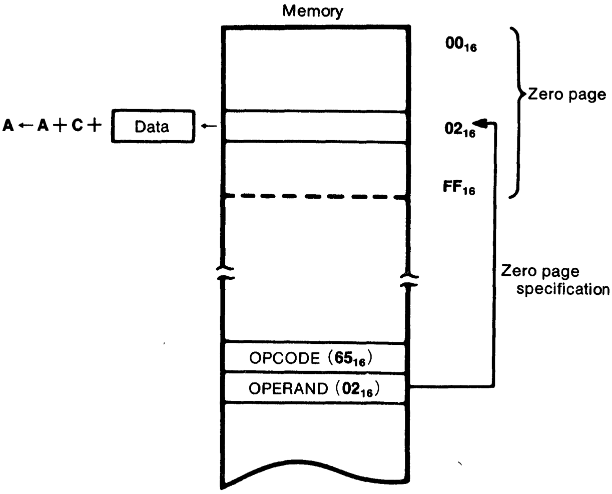


Name : Zero page addressing mode

Function : The operation is performed in zero page memory (00_{16} to FF_{16})

Instructions : **ADC, AND, ASL, BIT, CMP, COM, CPX, CPY, DEC, EOR, INC, LDA, LDM, LDX, LDY, LSR, ORA, ROL, ROR, RRF, SBC, STA, STX, STY, TST**

Example : Mnemonic Machine code
ADC \$02 **65_{16} 02_{16}**

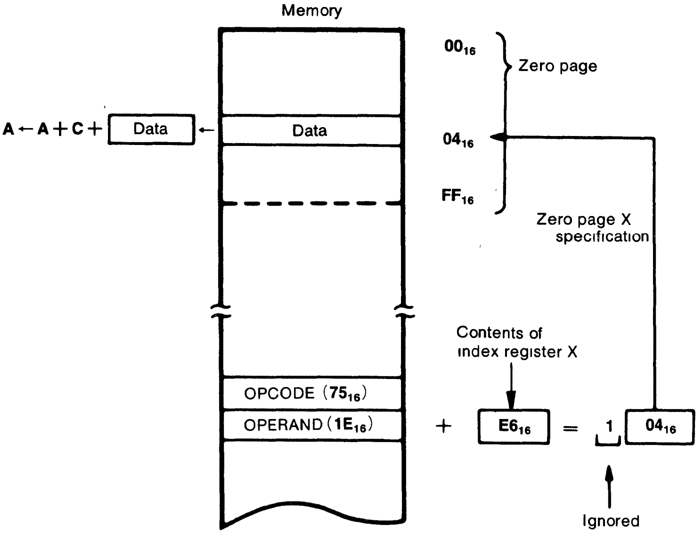


Name : Zero page X addressing mode

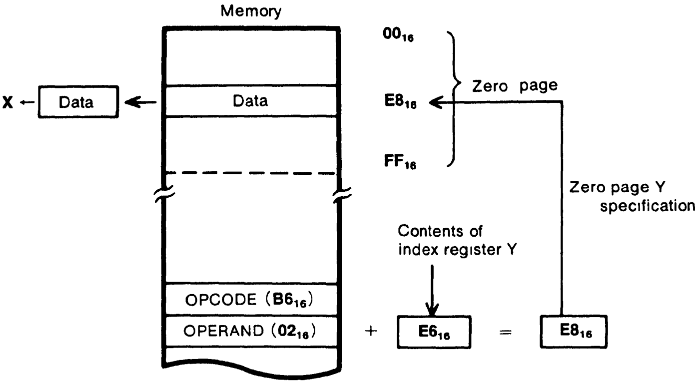
Function : The operation is performed on the zero page memory location whose address is specified by adding the OPERAND to the contents of index register X.

Instructions : **ADC, AND, ASL, CMP, DEC, DIV, EOR, INC, LDA, LDY, LSR, MUL, ORA, ROL, ROR, SBC, STA, STY**

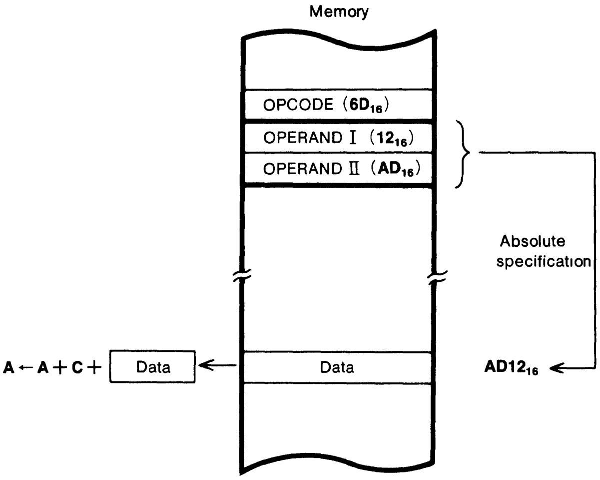
Example : Mnemonic Machine code
ADC \$1E,X **75_{16} $1E_{16}$**



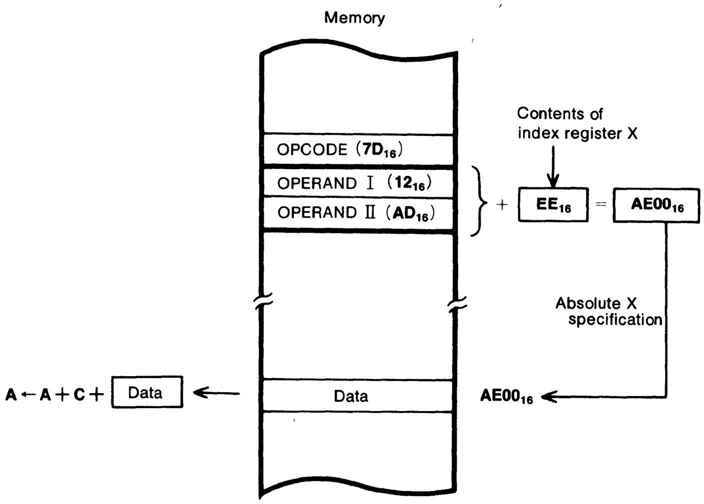
Name	: **Zero page Y addressing mode**
Function	: The operation is performed on the zero page memory location whose address is specified by adding the OPERAND to the contents of index register X.
Instructions	: **LDX, STX**
Example	: Mnemonic Machine code **LDX $02,Y** **B6$_{16}$ 02$_{16}$**



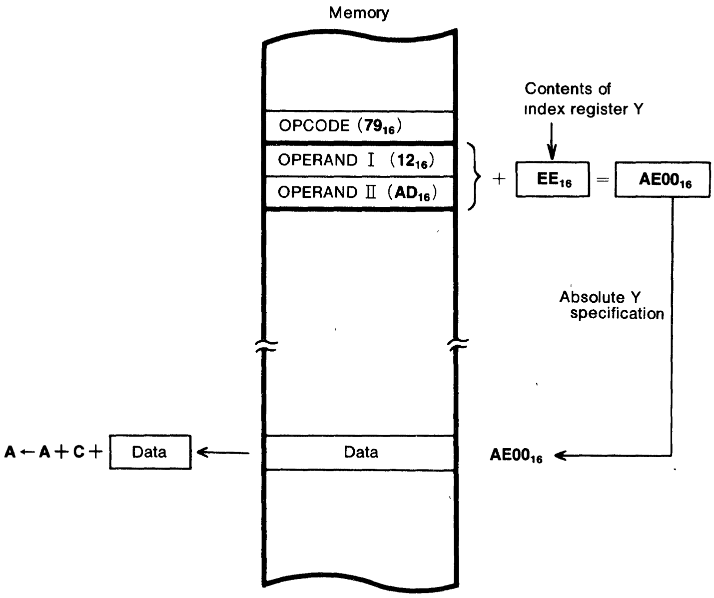
Name	: **Absolute addressing mode**
Function	: The operation is performed on the memory whose address is specified by first and second OPERAND.
Instructions	: **ADC, AND, ASL, BIT, CMP, CPX, CPY, DEC, EOR, INC, JMP, JSR, LDA, LDX, LDY, LSR, ORA, ROL, ROR, SBC, STA, STX, STY**
Example	: Mnemonic Machine code **ADC $AD12** **6D$_{16}$ 12$_{16}$ AD$_{16}$**



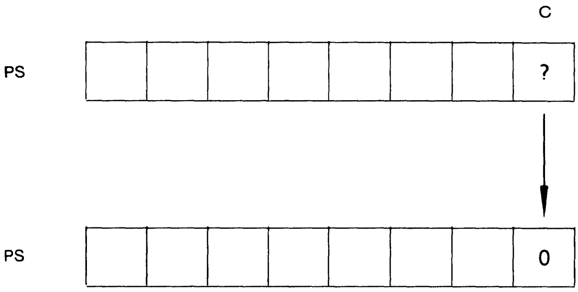
Name : **Absolute X addressing mode**
Function : The operation is performed on the memory location whose address is specified by adding the contents of index register X to the value indicated by the first and second OPERAND.
Instructions : **ADC, AND, ASL, CMP, DEC, EOR, INC, LDA, LDY, LSR, ORA, ROL, ROR, SBC, STA**
Example : Mnemonic Machine code
ADC $AD12,X **$7D_{16}$ 12_{16} AD_{16}**



Name : **Absolute Y addressing mode**
Function : The operation is performed on the memory location whose address is specified by adding the contents of index register Y to the value indicated by the first and second OPERAND.
Instructions : **ADC, AND, CMP, EOR, LDA, LDX, ORA, SBC, STA**
Example : Mnemonic Machine code
ADC $AD12,Y **$79_{16}$ 12_{16} AD_{16}**



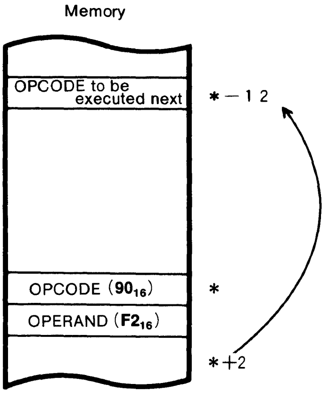
Name : Implied addressing mode
Function : Implied addressing mode operations need no OPERAND.
Instructions : **BRK, CLC, CLD, CLI, CLT, CLV, DEX, DEY, FST, INX, INY, NOP, PHA, PHP, PLA, PLP, RTI, RTS, SEC, SED, SEI, SET, SLW, STP, TAX, TAY, TSX, TXA, TXS, TYA, WIT**
Example : Mnemonic Machine code
CLC **18_{16}**



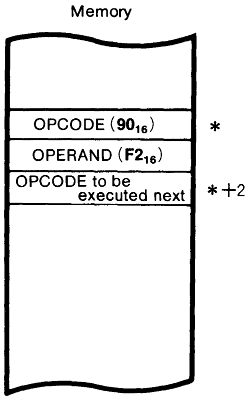
Carry flag reset

Name : Relative addressing mode
Function : Conditionally jumps to the address produced by adding the Program Counter to the OPERAND.
Instructions : **BCC, BCS, BEQ, BMI, BNE, BPL, BRA, BVC, BVS**
Example : Mnemonic Machine code
BCC *−12 **90_{16} $F2_{16}$**

Jumps to * −12 address when carry flag(C) is cleared.



Proceed to next address when carry flag(C) is set.

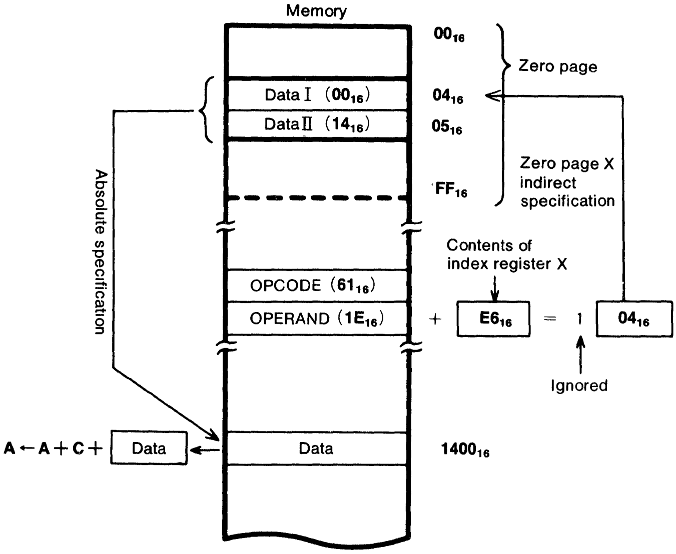


Name : Indirect X addressing mode

Function : The operation is performed on the memory location indicated by the contents of two consecutive bytes in zero page memory whose first address is specified by adding the OPERAND and the contents of index register X.

Instructions : **ADC, AND, CMP, EOR, LDA, ORA, SBC, STA**

Example : Mnemonic Machine code
ADC ($1E,X) **$61_{16}$ $1E_{16}$**



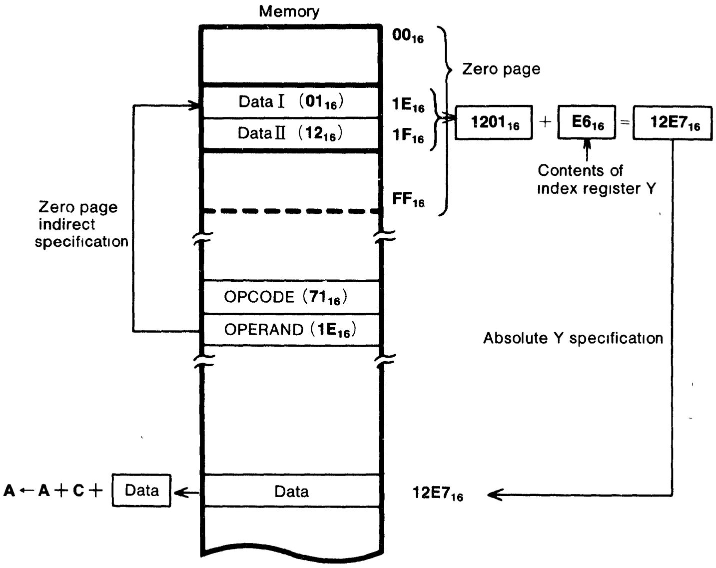
In this example, data I (00_{16}) and data II (14_{16}) have been stored beforehand.

Name : Indirect Y addressing mode

Function : The operation is performed on the memory location indicated by adding the contents of index register Y to the contents of two consecutive bytes in zero page memory whose first address is specified by the OPERAND.

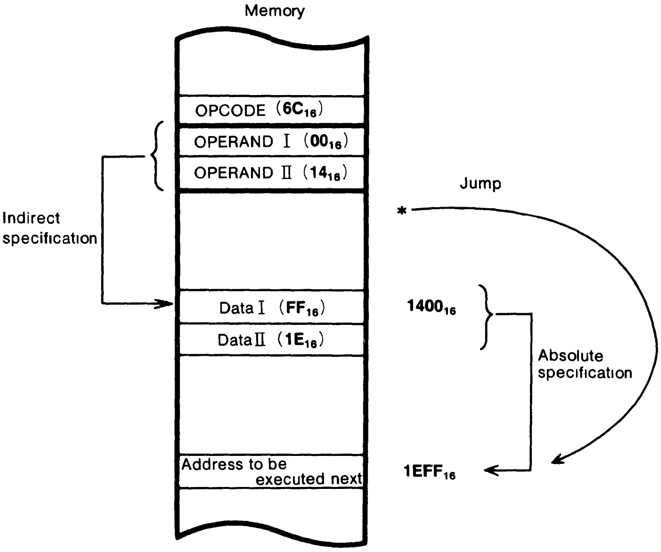
Instructions : **ADC, AND, CMP, EOR, LDA, ORA, SBC, STA**

Example : Mnemonic Machine code
ADC ($1E),Y **$71_{16}$ $1E_{16}$**



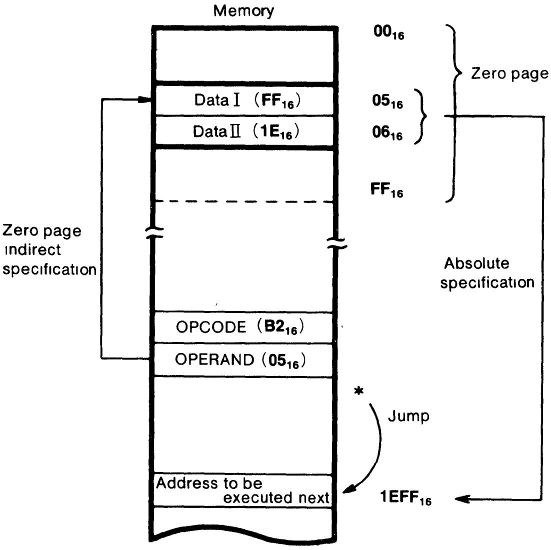
In this example, data I (01_{16}) and Data II (12_{16}) have been stored beforehand

Name	: Indirect absolute addressing mode
Function	: Jumps to the location specified by the contents of two consecutive bytes whose first address is specified by the first and second OPERAND.
Instructions	: **JMP**
Example	: Mnemonic Machine code **JMP ($1400)** **6C₁₆ 00₁₆ 14₁₆**



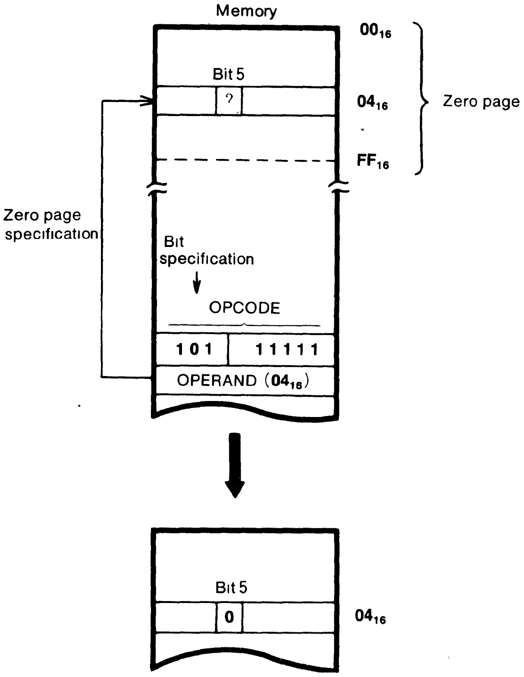
In this example, FF_{16} as data I and $1E_{16}$ as data II have been stored beforehand.

Name	: Zero page indirect absolute addressing mode
Function	: Jumps to the location specified by the contents of two consecutive bytes in zero page memory whose first address is specified by the OPERAND.
Instructions	: **JMP, JSR**
Example	: Mnemonic Machine code **JMP ($05)** **B2₁₆ 05₁₆**



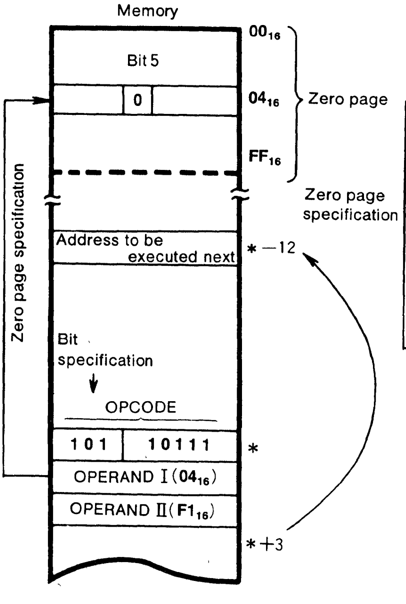
In this example, FF_{16} as data I and $1E_{16}$ as data II have been stored beforehand.

Name	: Zero page bit addressing mode
Function	: The operation is performed on the bit (specified by the three high order bits of the OPCODE), on the zero page memory location specified by the OPERAND.
Instructions	: **CLB, SEB**
Example	: Mnemonic Machine code **CLB 5,$04** **$BF_{16}$ 04_{16}**

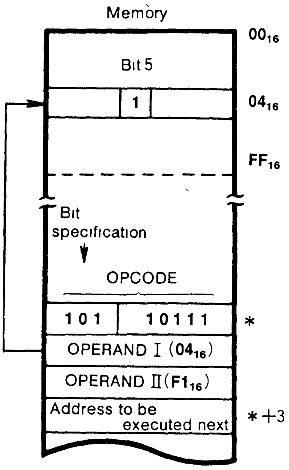


Name	: **Zero page bit relative addressing mode**
Function	: Conditionally jumps to the address specified by adding the second OPERAND to the program counter, depending on the bit (specified by the three higher order bits of the OPCODE) in the zero page memory location specified by the first OPERAND.
Instructions	: **BBC, BBS**
Example	: Mnemonic Machine code **BBC 5,$04,$*-12$** **$B7_{16}$ 04_{16} $F1_{16}$**

Jump to $* - 12$ address when 04_{16} address bit 5 is cleared.



Advance to $* + 3$ address when 04_{16} address bit 5 is set.



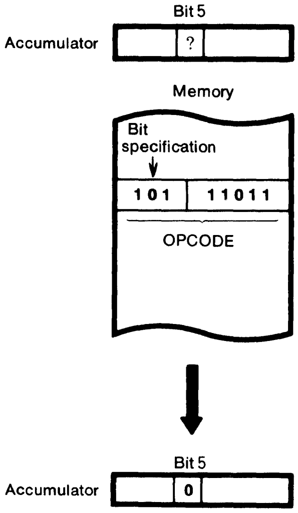
Name : Accumulator bit addressing mode

Function : The operation is performed on the bit in the accumulator which is specified by the three high order bits of the OPCODE. There is no OPERAND.

Instructions : **CLB, SEB**

Example :

Mnemonic	Machine code
CLB 5,A	**BB_{16}**



Name : Accumulator bit relative addressing mode

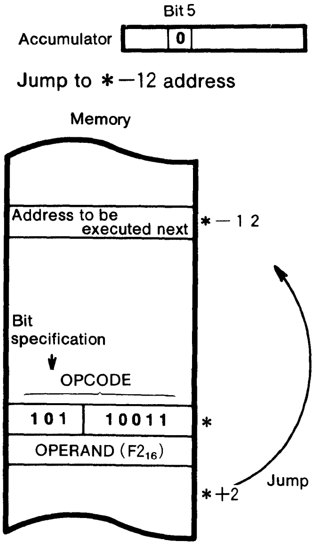
Function : Conditionally jumps to the address produced by adding the OPERAND to the program counter, depending on the bit in accumulator (specified by the high order three bits of the OPCODE).

Instructions : **BBC, BBS**

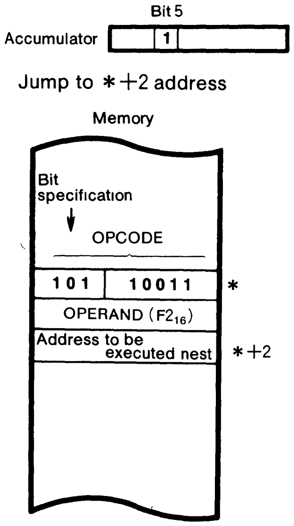
Example :

Mnemonic	Machine code
BBC 5,A,$*-12$	**$B3_{16}$ $F2_{16}$**

When accumulator bit 5 is cleared

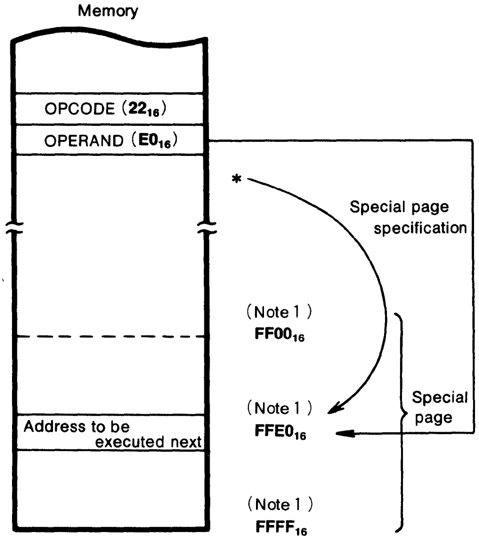


When accumulator bit 5 is set



Name	: Special page addressing mode
Function	: Jumps to the specified address in the special page area. The lower eight bits are specified by the OPERAND and the upper eight bits are defined by the special page (see Note 1).
Instructions	: **JSR**
Example	: Mnemonic Machine code
	JSR \$FFE0 22_{16} $E0_{16}$

Note 1 : Note that the special page is defined as the highest addressable 256 bytes of any given microcomputer and may be "FF_{16}", "$1F_{16}$", "$2F_{16}$", etc.



LIST OF INSTRUCTION CODES

	D_3~D_0	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
D_7~D_4	Hexadecimal notation	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0000	0	BRK	ORA IND, X	JSR ZP, IND	BBS 0, A	—	ORA ZP	ASL ZP	BBS 0, ZP	PHP	ORA IMM	ASL A	SEB 0, A	—	ORA ABS	ASL ABS	SEB 0, ZP
0001	1	BPL	ORA IND, Y	CLT	BBC 0, A	—	ORA ZP, X	ASL ZP, X	BBC 0, ZP	CLC	ORA ABS, Y	DEC A	CLB 0, A	—	ORA ABS, X	ASL ABS, X	CLB 0, ZP
0010	2	JSR ABS	AND IND, X	JSR SP	BBS 1, A	BIT ZP	AND ZP	ROL ZP	BBS 1, ZP	PLP	AND IMM	ROL A	SEB 1, A	BIT ABS	AND ABS	ROL ABS	SEB 1, ZP
0011	3	BMI	AND IND, Y	SET	BBC 1, A	—	AND ZP, X	ROL ZP, X	BBC 1, ZP	SEC	AND ABS, Y	INC A	CLB 1, A	LDM ZP	AND ABS, X	ROL ABS, X	CLB 1, ZP
0100	4	RTI	EOR IND, X	STP (Note)	BBS 2, A	COM ZP	EOR ZP	LSR ZP	BBS 2, ZP	PHA	EOR IMM	LSR A	SEB 2, A	JMP ABS	EOR ABS	LSR ABS	SEB 2, ZP
0101	5	BVC	EOR IND, Y	—	BBC 2, A	—	EOR ZP, X	LSR ZP, X	BBC 2, ZP	CLI	EOR ABS, Y	—	CLB 2, A	—	EOR ABS, X	LSR ABS, X	CLB 2, ZP
0110	6	RTS	ADC IND, X	MUL (Note)	BBS 3, A	TST ZP	ADC ZP	ROR ZP	BBS 3, ZP	PLA	ADC IMM	ROR A	SEB 3, A	JMP IND	ADC ABS	ROR ABS	SEB 3, ZP
0111	7	BVS	ADC IND, Y	—	BBC 3, A	—	ADC ZP, X	ROR ZP, X	BBC 3, ZP	SEI	ADC ABS, Y	—	CLB 3, A	—	ADC ABS, X	ROR ABS, X	CLB 3, ZP
1000	8	BRA	STA IND, X	RRF ZP	BBS 4, A	STY ZP	STA ZP	STX ZP	BBS 4, ZP	DEY	—	TXA	SEB 4, A	STY ABS	STA ABS	STX ABS	SEB 4, ZP
1001	9	BCC	STA IND, Y	—	BBC 4, A	STY ZP, X	STA ZP, X	STX ZP, Y	BBC 4, ZP	TYA	STA ABS, Y	TXS	CLB 4, A	—	STA ABS, X	—	CLB 4, ZP
1010	A	LDY IMM	LDA IND, X	LDX IMM	BBS 5, A	LDY ZP	LDA ZP	LDX ZP	BBS 5, ZP	TAY	LDA IMM	TAX	SEB 5, A	LDY ABS	LDA ABS	LDX ABS	SEB 5, ZP
1011	B	BCS	LDA IND, Y	JMP ZP, IND	BBC 5, A	LDY ZP, X	LDA ZP, X	LDX ZP, Y	BBC 5, ZP	CLV	LDA ABS, Y	TSX	CLB 5, A	LDY ABS, X	LDA ABS, X	LDX ABS, Y	CLB 5, ZP
1100	C	CPY IMM	CMP IND, X	SLW/ (Note) /WIT	BBS 6, A	CPY ZP	CMP ZP	DEC ZP	BBS 6, ZP	INY	CMP IMM	DEX	SEB 6, A	CPY ABS	CMP ABS	DEC ABS	SEB 6, ZP
1101	D	BNE	CMP IND, Y	—	BBC 6, A	—	CMP ZP, X	DEC ZP, X	BBC 6, ZP	CLD	CMP ABS, Y	—	CLB 6, A	—	CMP ABS, X	DEC ABS, X	CLB 6, ZP
1110	E	CPX IMM	SBC IND, X	FST/ (Note) /DIV	BBS 7, A	CPX ZP	SBC ZP	INC ZP	BBS 7, ZP	INX	SBC IMM	NOP	SEB 7, A	CPX ABS	SBC ABS	INC ABS	SEB 7, ZP
1111	F	BEQ	SBC IND, Y	—	BBC 7, A	—	SBC ZP, X	INC ZP, X	BBC 7, ZP	SED	SBC ABS, Y	—	CLB 7, A	—	SBC ABS, X	INC ABS, X	CLB 7, ZP

Note Support of these instructions depends on the microcomputer type

Instruction	Supported in the following microcomputer types
FST SLW	M50740A-XXXSP, M50740ASP, M50741-XXXSP, M50752-XXXSP, M50757-XXXSP, M50758-XXXSP
MUL DIV	Series 7450, Series 38000, M37424M8-XXXSP, M37524M4-XXXSP

Instruction	Not supported in the following microcomputer types
WIT	M50740A-XXXSP, M50740ASP, M50741-XXXSP, M50752-XXXSP, M50757-XXXSP, M50758-XXXSP
STP	M50752-XXXSP, M50757-XXXSP, M50758-XXXSP, M37424M8-XXXSP, M37524M4-XXXSP

▨ 3-byte instruction
☐ 2-byte instruction
☐ 1-byte instruction

MACHINE INSTRUCTIONS

Symbol	Function	Details	Addressing mode																	
			IMP			IMM			A			BIT,A			ZP			BIT,ZP		
			OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#
ADC (Note 1) (Note 6)	When T=0 A←A+M+C When T=1 M(X)←M(X)+M+C	Adds the carry, accumulator and memory contents The results are entered into the accumulator. Adds the contents of the memory in the address indicated by index register X, the contents of the memory specified by the addressing mode and the carry The results are entered into the memory at the address indicated by index register X				69	2	2							65	3	2			
AND (Note 1)	When T=0 A←A∧M When T=1 M(X)←M(X)∧M	"AND's" the accumulator and memory contents. The results are entered into the accumulator "AND's" the contents of the memory of the address indicated by index register X and the contents of the memory specified by the addressing mode. The results are entered into the memory at the address indicated by index register X				29	2	2							25	3	2			
ASL	7 0 C ← ▭ ←0	Shifts the contents of accumulator or contents of memory one bit to the left The low order bit of the accumulator or memory is cleared and the high order bit is shifted into the carry flag							0A	2	1				06	5	2			
BBC (Note 4)	A_b or M_b=0?	Branches when the contents of the bit specified in the accumulator or memory is "0"										13 + 2i	4	2				17 + 2i	5	3
BBS (Note 4)	A_b or M_b=1?	Branches when the contents of the bit specified in the accumulator or memory is "1"										03 + 2i	4	2				07 + 2i	5	3
BCC (Note 4)	C=0?	Branches when the contents of carry flag is "0"																		
BCS (Note 4)	C=1?	Branches when the contents of carry flag is "1"																		
BEQ (Note 4)	Z=1?	Branches when the contents of zero flag is "1"																		
BIT	A∧M	"AND's" the contents of accumulator and memory The results are not entered anywhere													24	3	2			
BMI (Note 4)	N=1?	Branches when the contents of negative flag is "1"																		
BNE (Note 4)	Z=0?	Branches when the contents of zero flag is "0"																		
BPL (Note 4)	N=0?	Branches when the contents of negative flag is "0"																		
BRA	PC←PC±offset	Jumps to address specified by adding offset to the program counter																		
BRK	B←1 M(S)←PC_H S←S−1 M(S)←PC_L S←S−1 M(S)←PS S←S−1 PC_L←AD_L PC_H←AD_H	Executes a software interrupt	00	7	1															

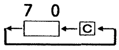
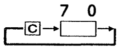
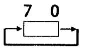
Addressing mode																																	Processor status register							
ZP,X			ZP,Y			ABS			ABS,X			ABS,Y			IND			ZP,IND			IND,X			IND,Y			REL			SP			7	6	5	4	3	2	1	0
OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	N	V	T	B	D	I	Z	C
75	4	2				6D	4	3	7D	5	3	79	5	3							61	6	2	71	6	2							N	V	•	•	•	•	Z	C
35	4	2				2D	4	3	3D	5	3	39	5	3							21	6	2	31	6	2							N	•	•	•	•	•	Z	•
16	6	2				0E	6	3	1E	7	3																						N	•	•	•	•	•	Z	C
																																	•	•	•	•	•	•	•	•
																																	•	•	•	•	•	•	•	•
																											90	2	2				•	•	•	•	•	•	•	•
																											B0	2	2				•	•	•	•	•	•	•	•
																											F0	2	2				•	•	•	•	•	•	•	•
						2C	4	3																									M_7	M_6	•	•	•	•	Z	•
																											30	2	2				•	•	•	•	•	•	•	•
																											D0	2	2				•	•	•	•	•	•	•	•
																											10	2	2				•	•	•	•	•	•	•	•
																											80	4	2				•	•	•	•	•	•	•	•
																																	•	•	•	1	•	1	•	•

Symbol	Function	Details	Addressing mode																	
			IMP			IMM			A			BIT,A			ZP			BIT,ZP		
			OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#
BVC (Note 4)	V=0?	Branches when the contents of overflow flag is "0"																		
BVS (Note 4)	V=1?	Branches when the contents of overflow flag is "1"																		
CLB	A_b or M_b←0	Clears the contents of the bit specified in the accumulator or memory to "0"										1B + 2i	2	1				1F + 2i	5	2
CLC	C←0	Clears the contents of the carry flag to "0"	18	2	1															
CLD	D←0	Clears the contents of decimal mode flag to "0"	D8	2	1															
CLI	I←0	Clears the contents of interrupt disable flag to "0"	58	2	1															
CLT	T←0	Clears the contents of index X mode flag to "0"	12	2	1															
CLV	V←0	Clears the contents overflow flag to "0"	B8	2	1															
CMP (Note 3)	When T=0 A−M When T=1 M(X)−M	Compares the contents of accumulator and memory Compares the contents of the memory specified by the addressing mode with the contents of the address indicated by index register X				C9	2	2							C5	3	2			
COM	M←$\overline{M}$	Forms a one's complement of the contents of memory, and stores it into memory													44	5	2			
CPX	X−M	Compares the contents of index register X and memory				E0	2	2							E4	3	2			
CPY	Y−M	Compares the contents of index register Y and memory				C0	2	2							C4	3	2			
DEC	A←A−1 or M←M−1	Decrements the contents of the accumulator or memory by 1							1A	2	1				C6	5	2			
DEX	X←X−1	Decrements the contents of index register X by 1	CA	2	1															
DEY	Y←Y−1	Decrements the contents of index register Y by 1	88	2	1															
DIV (Note 5)	A←(M(zz+X+1), M(zz+X))/A M(S) ← 1's complement of Remainder S←S− 1	Divides the 16-bit data that is the contents of M(zz+x+1) for high byte and the contents of M(zz + x) for low byte by the accumulator Stores the quotient in the accumulator and the 1's complement of the remainder on the stack																		
EOR (Note 1)	When T=0 A←A∀M When T=1 M(X)←M(X)∀M	"Exclusive-ORs" the contents of accumulator and memory The results are stored in the accumulator "Exclusive-ORs" the contents of the memory specified by the addressing mode and the contents of the memory at the address indicated by index register X The results are stored into the memory at the address indicated by index register X				49	2	2							45	3	2			
FST (Note 5)		Connects oscillator output to the X_{OUTF} pin	E2	2	1															
INC	A←A+1 or M←M+1	Increments the contents of accumulator or memory by 1							3A	2	1				E6	5	2			
INX	X←X+1	Increments the contents of index register X by 1	E8	2	1															
INY	Y←Y+1	Increments the contents of index register Y by 1	C8	2	1															

Addressing mode																																	Processor status register							
ZP,X			ZP,Y			ABS			ABS,X			ABS,Y			IND			ZP,IND			IND,X			IND,Y			REL			SP			7	6	5	4	3	2	1	0
OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	N	V	T	B	D	I	Z	C
																											50	2	2				•	•	•	•	•	•	•	•
																											70	2	2				•	•	•	•	•	•	•	•
																																	•	•	•	•	•	•	•	•
																																	•	•	•	•	•	•	•	0
																																	•	•	•	•	0	•	•	•
																																	•	•	•	•	•	0	•	•
																																	•	•	0	•	•	•	•	•
																																	•	0	•	•	•	•	•	•
D5	4	2				CD	4	3	DD	5	3	D9	5	3							C1	6	2	D1	6	2							N	•	•	•	•	•	Z	C
																																	N	•	•	•	•	•	Z	•
						EC	4	3																									N	•	•	•	•	•	Z	C
						CC	4	3																									N	•	•	•	•	•	Z	C
D6	6	2				CE	6	3	DE	7	3																						N	•	•	•	•	•	Z	•
																																	N	•	•	•	•	•	Z	•
																																	N	•	•	•	•	•	Z	•
E2	16	2																															•	•	•	•	•	•	•	•
55	4	2				4D	4	3	5D	5	3	59	5	3							41	6	2	51	6	2							N	•	•	•	•	•	Z	•
																																	•	•	•	•	•	•	•	•
F6	6	2				EE	6	3	FE	7	3																						N	•	•	•	•	•	Z	•
																																	N	•	•	•	•	•	Z	•
																																	N	•	•	•	•	•	Z	•

Symbol	Function	Details	Addressing mode																	
			IMP			IMM			A			BIT,A			ZP			BIT,ZP		
			OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#
JMP	If addressing mode is ABS $PC_L \leftarrow AD_L$ $PC_H \leftarrow AD_H$ If addressing mode is IND $PC_L \leftarrow M(AD_H, AD_L)$ $PC_H \leftarrow M(AD_H, AD_L+1)$ If addressing mode is ZP, IND $PC_L \leftarrow M(00, AD_L)$ $PC_H \leftarrow M(00, AD_L+1)$	Jumps to the specified address																			
JSR	$M(S) \leftarrow PC_H$ $S \leftarrow S-1$ $M(S) \leftarrow PC_L$ $S \leftarrow S-1$ After executing the above, if addressing mode is ABS, $PC_L \leftarrow AD_L$ $PC_H \leftarrow AD_H$ If addressing mode is SP, $PC_L \leftarrow AD_L$ $PC_H \leftarrow FF$ If addressing mode is ZP, IND, $PC_L \leftarrow M(00, AD_L)$ $PC_H \leftarrow M(00, AD_L+1)$	After storing contents of program counter in stack, and jumps to the specified address																			
LDA (Note 2)	When T=0 $A \leftarrow M$ When T=1 $M(X) \leftarrow M$	Load accumulator with contents of memory Load memory indicated by index register X with contents of memory specified by the addressing mode				A9	2	2							A5	3	2			
LDM	$M \leftarrow nn$	Load memory with immediate value													3C	4	3			
LDX	$X \leftarrow M$	Load index register X with contents of memory				A2	2	2							A6	3	2			
LDY	$Y \leftarrow M$	Load index register Y with contents of memory				A0	2	2							A4	3	2			
LSR	7 0 0 → ☐ → C	Shift the contents of accumulator or memory to the right by one bit The low order bit of accumulator or memory is stored in carry, 7th bit is cleared							4A	2	1				46	5	2			
MUL (Note 5)	$M(S) \cdot A \leftarrow A \times M(zz+X)$ $S \leftarrow S-1$	Multiplies the accumulator with the contents of memory specified by the zero page X addressing mode and stores the high byte of the result on the stack and the low byte in the accumulator																		
NOP	$PC \leftarrow PC+1$	No operation	EA	2	1															
ORA (Note 1)	When T=0 $A \leftarrow A \vee M$ When T=1 $M(X) \leftarrow M(X) \vee M$	"Logical OR's" the contents of memory and accumulator The result is stored in the accumulator "Logical OR's" the contents of memory indicated by index register X and contents of memory specified by the addressing mode The result is stored in the memory specified by index register X				09	2	2							05	3	2			

Addressing mode																																	Processor status register							
ZP,X			ZP,Y			ABS			ABS,X			ABS,Y			IND			ZP,IND			IND,X			IND,Y			REL			SP			7	6	5	4	3	2	1	0
OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	N	V	T	B	D	I	Z	C
						4C	3	3							6C	5	3	B2	4	2													•	•	•	•	•	•	•	•
						20	6	3										02	7	2										22	5	2	•	•	•	•	•	•	•	•
B5	4	2				AD	4	3	BD	5	3	B9	5	3							A1	6	2	B1	6	2							N	•	•	•	•	•	Z	•
																																	•	•	•	•	•	•	•	•
			B6	4	2	AE	4	3				BE	5	3																			N	•	•	•	•	•	Z	•
B4	4	2				AC	4	3	BC	5	3																						N	•	•	•	•	•	Z	•
56	6	2				4E	6	3	5E	7	3																						0	•	•	•	•	•	Z	C
62	15	2																															•	•	•	•	•	•	•	•
																																	•	•	•	•	•	•	•	•
15	4	2				0D	4	3	1D	5	3	19	5	3							01	6	2	11	6	2							N	•	•	•	•	•	Z	•

Symbol	Function	Details	Addressing mode																	
			IMP			IMM			A			BIT,A			ZP			BIT,ZP		
			OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#
PHA	M(S)←A S←S−1	Saves the contents of the accumulator in memory at the address indicated by the stack pointer and decrements the contents of stack pointer by 1	48	3	1															
PHP	M(S)←PS S←S−1	Saves the contents of the processor status register in memory at the address indicated by the stack pointer and decrements the contents of the stack pointer by 1	08	3	1															
PLA	S←S+1 A←M(S)	Increments the contents of the stack pointer by 1 and restores the accumulator from the memory at the address indicated by the stack pointer	68	4	1															
PLP	S←S+1 PS←M(S)	Increments the contents of stack pointer by 1 and restores the processor status register from the memory at the address indicated by the stack pointer	28	4	1															
ROL		Shifts the contents of the memory or accumulator to the left by one bit The high order bit is shifted into the carry flag and the carry flag is shifted into the low order bit							2A	2	1				26	5	2			
ROR		Shifts the contents of the memory or accumulator to the right by one bit The low order bit is shifted into the carry flag and the carry flag is shifted into the high order bit							6A	2	1				66	5	2			
RRF		Rotates the contents of memory to the right by 4 bits													82	8	2			
RTI	S←S+1 PS←M(S) S←S+1 PC_L←M(S) S←S+1 PC_H←M(S)	Returns from an interrupt routine to the main routine	40	6	1															
RTS	S←S+1 PC_L←M(S) S←S+1 PC_H←M(S)	Returns from a subroutine to the main routine	60	6	1															
SBC (Note 1) (Note 6)	When T=0 $A \leftarrow A - M - \overline{C}$ When T=1 $M(X) \leftarrow M(X) - M - \overline{C}$	Subtracts the contents of memory and complement of carry flag from the contents of accumulator The results are stored into the accumulator Subtracts contents of complement of carry flag and contents of the memory indicated by the addressing mode from the memory at the address indicated by index register X The results are stored into the memory of the address indicated by index register X				E9	2	2							E5	3	2			
SEB	A_b or M_b←1	Sets the specified bit in the accumulator or memory to "1 "										0B + 2i	2	1				0F + 2i	5	2
SEC	C←1	Sets the contents of the carry flag to "1 "	38	2	1															
SED	D←1	Sets the contents of the decimal mode flag to "1 "	F8	2	1															
SEI	I←1	Sets the contents of the interrupt disable flag to "1 "	78	2	1															
SET	T←1	Sets the contents of the index X mode flag to "1 "	32	2	1															
SLW (Note 5)		Disconnects the oscillator output from the X_{OUTF} pin	C2	2	1															

Addressing mode																																	Processor status register							
ZP,X			ZP,Y			ABS			ABS,X			ABS,Y			IND			ZP,IND			IND,X			IND,Y			REL			SP			7	6	5	4	3	2	1	0
OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	N	V	T	B	D	I	Z	C
																																	•	•	•	•	•	•	•	•
																																	•	•	•	•	•	•	•	•
																																	N	•	•	•	•	•	Z	•
																																	(Value saved in stack)							
36	6	2				2E	6	3	3E	7	3																						N	•	•	•	•	•	Z	C
76	6	2				6E	6	3	7E	7	3																						N	•	•	•	•	•	Z	C
																																	•	•	•	•	•	•	•	•
																																	(Value saved in stack)							
																																	•	•	•	•	•	•	•	•
F5	4	2				ED	4	3	FD	5	3	F9	5	3							E1	6	2	F1	6	2							N	V	•	•	•	•	Z	C
																																	•	•	•	•	•	•	•	•
																																	•	•	•	•	•	•	•	1
																																	•	•	•	•	1	•	•	•
																																	•	•	•	•	•	1	•	•
																																	•	•	1	•	•	•	•	•
																																	•	•	•	•	•	•	•	•

Symbol	Function	Details	Addressing mode																	
			IMP			IMM			A			BIT,A			ZP			BIT,ZP		
			OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#
STA	M←A	Stores the contents of accumulator in memory													85	4	2			
STP (Note 5)		Stops the oscillator	42	2	1															
STX	M←X	Stores the contents of index register X in memory													86	4	2			
STY	M←Y	Stores the contents of index register Y in memory													84	4	2			
TAX	X←A	Transfers the contents of the accumulator to index register X	AA	2	1															
TAY	Y←A	Transfers the contents of the accumulator to index register Y	A8	2	1															
TST	M=0?	Tests whether the contents of memory are "0" or not													64	3	2			
TSX	X←S	Transfers the contents of the stack pointer to index register X	BA	2	1															
TXA	A←X	Transfers the contents of index register X to the accumulator	8A	2	1															
TXS	S←X	Transfers the contents of index register X to the stack pointer	9A	2	1															
TYA	A←Y	Transfers the contents of index register Y to the accumulator	98	2	1															
WIT (Note 5)		Stops the internal clock	C2	2	1															

Note 1 : The number of cycles "n" is increased by 3 when T is 1
2 : The number of cycles "n" is increased by 2 when T is 1
3 : The number of cycles "n" is increased by 1 when T is 1
4 : The number of cycles "n" is increased by 2 when branching has occurred
5 : Support of these instructions depends on the microcomputer type

Instruction	Supported in the following microcomputer types
FST SLW	M50740A-XXXSP, M50740ASP, M50741-XXXSP, M50752-XXXSP, M50757-XXXSP, M50758-XXXSP
MUL DIV	Series 7450, Series 38000, M37424M8-XXXSP, M37524M4-XXXSP

Instruction	Not supported in the following microcomputer types
WIT	M50740A-XXXSP, M50740ASP, M50741-XXXSP, M50752-XXXSP, M50757-XXXSP, M50758-XXXSP
STP	M50752-XXXSP, M50757-XXXSP, M50758-XXXSP, M37424M8-XXXSP, M37524M4-XXXSP

6 : N, V, and Z flags are invalid in decimal operation mode

Addressing mode																																	Processor status register							
ZP,X			ZP,Y			ABS			ABS,X			ABS,Y			IND			ZP,IND			IND,X			IND,Y			REL			SP			7	6	5	4	3	2	1	0
OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	N	V	T	B	D	I	Z	C
95	5	2				8D	5	3	9D	6	3	99	6	3							81	7	2	91	7	2							•	•	•	•	•	•	•	•
																																	•	•	•	•	•	•	•	•
			96	5	2	8E	5	3																									•	•	•	•	•	•	•	•
94	5	2				8C	5	3																									•	•	•	•	•	•	•	•
																																	N	•	•	•	•	•	Z	•
																																	N	•	•	•	•	•	Z	•
																																	N	•	•	•	•	•	Z	•
																																	N	•	•	•	•	•	Z	•
																																	N	•	•	•	•	•	Z	•
																																	•	•	•	•	•	•	•	•
																																	N	•	•	•	•	•	Z	•
																																	•	•	•	•	•	•	•	•

Symbol	Contents	Symbol	Contents
IMP	Implied addressing mode	+	Addition
IMM	Immediate addressing mode	—	Subtraction
A	Accumulator or Accumulator addressing mode	Λ	Logical OR
		V	Logical AND
BIT, A	Accumulator bit relative addressing mode	⊻	Logical exclusive OR
		—	Negation
ZP	Zero page addressing mode	←	Shows direction of data flow
BIT, ZP	Zero page bit relative addressing mode	X	Index register X
		Y	Index register Y
ZP, X	Zero page X addressing mode	S	Stack pointer
ZP, Y	Zero page Y addressing mode	PC	Program counter
ABS	Absolute addressing mode	PS	Processor status register
ABS, X	Absolute X addressing mode	PC_H	8 high-order bits of program counter
ABS, Y	Absolute Y addressing mode	PC_L	8 low-order bits of program counter
IND	Indirect absolute addressing mode	AD_H	8 high-order bits of address
		AD_L	8 low-order bits of address
ZP, IND	Zero page indirect absolute addressing mode	FF	FF in Hexadecimal notation
		nn	Immediate value
IND, X	Indirect X addressing mode	M	Memory specified by address designation of any addressing mode
IND, Y	Indirect Y addressing mode		
REL	Relative addressing mode	M (X)	Memory of address indicated by contents of index register X
SP	Special page addressing mode		
C	Carry flag	M (S)	Memory of address indicated by contents of stack pointer
Z	Zero flag		
I	Interrupt disable flag	$M(AD_H, AD_L)$	Contents of memory at address indicated by AD_H and AD_L, in AD_H is 8 high-order bits and AD_L is 8 low-order bits
D	Decimal mode flag		
B	Break flag		
T	X-modified arithmetic mode flag	$M(00, AD_L)$	Contents of address indicated by zero page AD_L
V	Overflow flag	A_b	1 bit of accumulator
N	Negative flag	M_b	1 bit of memory
		OP	Opcode
		n	Number of cycles
		#	Number of bytes

NOTES on USE

Keep the following points in mind while programming.

Processor status register

(1) Initialization of processor status register

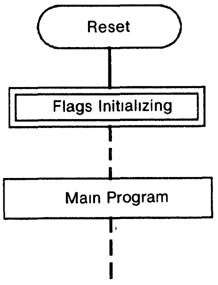
After a reset, the contents of the processor status register (PS) are undefined except for the I flag which is "1". Therefore, flags which affect program execution must be initialized after a reset.

In particular, it is essential to initialize the T and D flags because they have an important effect on calculations.

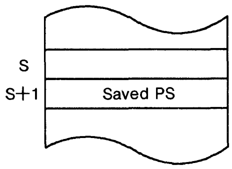
(2) How to reference the processor status register

To reference the contents of the processor status register (PS), execute the PHP instruction once then read the contents of (S+1). If necessary, execute the PLP instruction to return the PS to its original status.

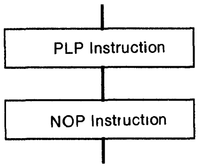
A NOP instruction should be executed after every PLP instruction. (The NOP in unnecessary when using a series 38000 microcomputer).



Initialization of Flags in PS



Stack Memory Contents after PHP Instruction Execution

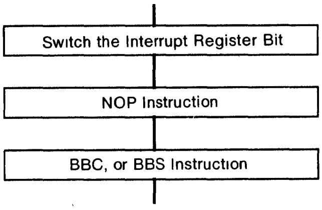


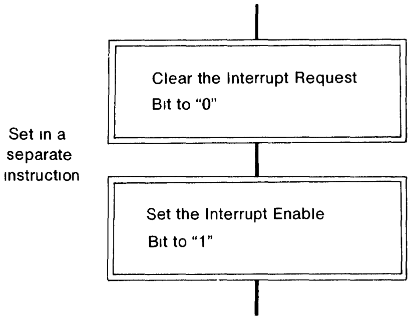
Interrupts

The contents of the interrupt request bits can be changed by software, but the values will not change immediately after being overwritten. Therefore, note the following points:

(1) After changing the value of the interrupt request bits, execute at least one instruction before executing a BBC, BBS, or any other read instruction.

(2) When clearing an interrupt request bit to "0" and setting an interrupt enable bit to "1" (=setting in an interrupt enable state), it needs to be cleared or set these bits in a separate instruction. The interrupt is accepted because it becomes in the interrupt enable state before clearing the interrupt request bit, if clearing the interrupt request bit and setting the interrupt enable bit are performed in an instruction.

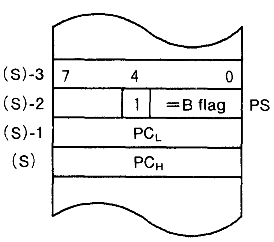




BRK instruction

(1) It can be detected that the BRK instruction interrupt event or the least priority interrupt event by referring the stored B flag state. Refer the stored B flag state in the interrupt routine, in this case.
However, the microcomputer that has an independent BRK instruction interrupt vector (cf. the 7450 series, the 7470 series, and the 38000 series) are not necessary this detection.

(2) The CPU of all 8-bit microcomputers except the 38000 series have the following bug about the BRK instruction execution.
At the following status,
① the interrupt request bit has set to "1".
② the interrupt enable bit has set to "1".
③ the interrupt disable flag (I) has set to "1".
if the BRK instruction is executed, the interrupt disable state is cancelled and it becomes in the interrupt enable state. So that the requested interrupts (the interrupts that corresponding to their request bits have set to "1") are accepted.



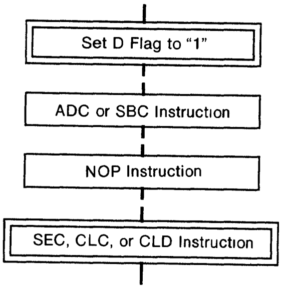
Decimal calculations

(1) Execution of decimal calculations

The ADC and SBC are the only instructions which will yield proper decimal results in decimal mode. To calculate in decimal notation, set the decimal mode flag (D) to "1" with the SED instruction. After executing the ADC or SBC instruction, execute another instruction before executing the SEC, CLC, or CLD instruction.

(2) Note on flags in decimal mode

When decimal mode is selected, the values of three of the flags in the status register (the N, V, and Z flags) are invalid after a ADC or SBC instruction is executed. The Carry flag (C) is set to "1" if a carry is generated as a result of the calculation, or is cleared to "0" if a borrow is generated. To determine whether a calculation has generated a carry, the C flag must be initialized to "0" before each calculation. To check for a borrow, the C flag must be initialized to "1" before each calculation.



JMP instruction

When using the JMP instruction in indirect addressing mode, do not specify the last address on a page as an indirect address.

APPENDICES

SERIES MELPS 740 MASK ROM ORDERING METHOD

SERIES MELPS 740 MASK ROM ORDERING METHOD

Mitsubishi Electric corp. accepts order to transfer EPROM supplied program data into the mask ROM in single-chip 8-bit microcomputers.

When placing such order, please submit the information described below.

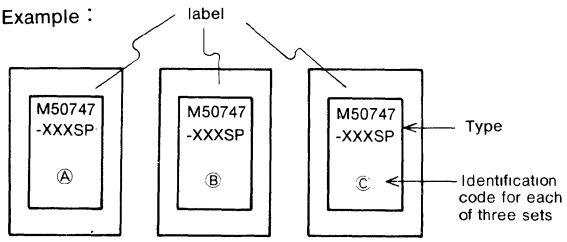
(1) Mask ROM confirmation form ·································· 1 set
(There is a specific form to be used for each model.)
(2) Data to be written into mask ROM ············· ··· EPROM
(Please provide three sets containing the identical data.)
(3) Mark specification form ·· 1 set

NOTES

(1) Acceptable EPROM type
Any EPROM made by Mitsubishi that is listed in the mask ROM confirmation form may be used.

(2) EPROM window labeling
Please write the model name and the identification code (A, B, C) on the label for each of the three sets of data EPROMs provided.

Example :



(3) Calculation and indication of checksum code
Please calculate the total number of data in words in the EPROM, and write the number in 4-digit hexadecimal form in the checksum code field of the mask ROM confirmation form.

(4) Options
Refer to the appropriate data book entry and write the desired options on the mask ROM confirmation form

(5) Mark specification method
The permissible mark specifications differ depending on the shape of package. Please fill out the mark specification form and attach it to the mask ROM confirmation form.

OUTLINE OF ORDER PROCESSING

Mitsubishi will produce the mask ROM if at least two of the three EPROM sets submitted contain identical data.

If we find error when the submitted EPROMs are compared, we will contact your representative

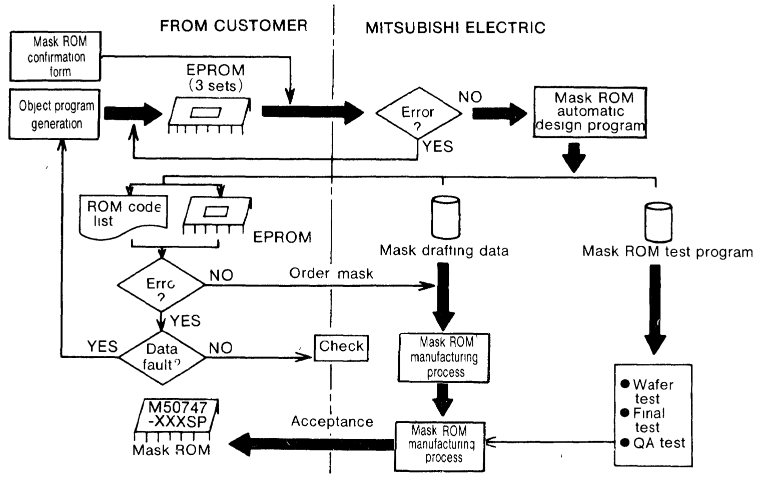
Thus, we assume responsibility only when we produce the mask ROM that contain data other than the data correctly provided by the customer.

Mitsubishi uses an automatic mask ROM design program to generated the following :

1. Drafting data for mask ROM production,
2. ROM code listing or EPROM for mask ROM production error check work,
3. Mask ROM test program.

The chart below shows the flow of mask ROM production

SERIES MELPS 740 MASK ROM DEVELOPMENT CAD SYSTEM



SERIES MELPS 740 MASK ROM ORDERING METHOD

GZZ–SH00–95A＜75B0＞

Mask ROM number	

SERIES MELPS 740 MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M37450M2-XXXSP/FP
MITSUBISHI ELECTRIC

Receipt	Date :	
	Section head signature	Supervisor signature

Note : Please fill in all items marked※.

※	Customer	Company name	TEL (　　　)	Issuance signature	Submitted by	Supervisor
		Date issued	Date :			

※ 1 . Confirmation

Specify the name of the product being ordered and the type of EPROMs submitted.

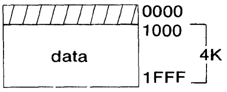
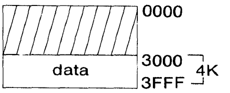
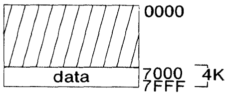
Three sets of EPROMs are required for each pattern (Check @ in the appropriate box).

If at least two of the three sets of EPROMs submitted contain identical data, we will produce masks based in this data. We shall assume the responsibility for errors only if the mask ROM data on the products we produce differ from this data. Thus, the customer must be especially careful in verifying the data contained in the EPROMs submitted.

Microcomputer name : ☐ M37450M2-XXXSP ☐ M37450M2-XXXFP

Checksum code for entire EPROM ☐☐☐☐ (hexadecimal notation)

EPROM type

☐ 2764	☐ 27128	☐ 27256
		

Set "FF$_{16}$" in the shaded area

※ 2 . Mark specification

Mark specification must be submitted using the correct form for the type package being ordered fill out the appropriate mark specification form (64P4B for M37450M2-XXXSP ; 80P6 for M37450M2-XXXFP) and attach to the mask ROM confirmation form.

※ 3 . Comments

GZZ–SH00–99A〈75B0〉

Mask ROM number	

Receipt	Date :	
	Section head signature	Supervisor signature

SERIES MELPS 740 MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M37450M4-XXXSP/FP
MITSUBISHI ELECTRIC

Note : Please fill in all items marked※.

※	Customer	Company name	TEL ( )	Issuance signature	Submitted by	Supervisor
		Date issued	Date :			

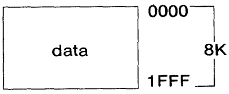
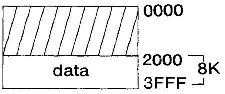
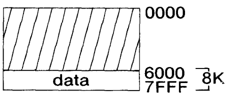
※1. Confirmation

Specify the name of the product being ordered and the type of EPROMs submitted.
Three sets of EPROMs are required for each pattern (Check @ in the appropriate box).
If at least two of the three sets of EPROMs submitted contain identical data, we will produce masks based in this data. We shall assume the responsibility for errors only if the mask ROM data on the products we produce differ from this data. Thus, the customer must be especially careful in verifying the data contained in the EPROMs submitted.

Microcomputer name : ☐ M37450M4-XXXSP ☐ M37450M4-XXXFP

Checksum code for entire EPROM ☐☐☐☐ (hexadecimal notation)

EPROM type

☐ 2764	☐ 27128	☐ 27256
		

Set "FF_{16}" in the shaded area.

※2. Mark specification

Mark specification must be submitted using the correct form for the type package being ordered fill out the appropriate mark specification form (64P4B for M37450M4-XXXSP ; 80P6 for M37450M4-XXXFP) and attach to the mask ROM confirmation form.

※3. Comments

GZZ—SH03—07A〈9YA0〉

Mask ROM number	

SERIES MELPS 740 MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M37450M4TXXXSP/J
MITSUBISHI ELECTRIC

Receipt	Date :	
	Section head signature	Supervisor signature

Note : Please fill in all items marked※.

<table>
<tr><td rowspan="2">※</td><td rowspan="2">Customer</td><td>Company name</td><td>TEL
(　　　)</td><td rowspan="2">Issuance signature</td><td>Submitted by</td><td>Supervisor</td></tr>
<tr><td>Date issued</td><td>Date :</td><td></td><td></td></tr>
</table>

※1. Confirmation

Specify the name of the product being ordered and the type of EPROMs submitted.

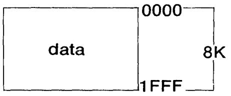
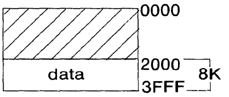
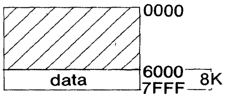
Three sets of EPROMs are required for each pattern (Check @ in the appropriate box).

If at least two of the three sets of EPROMs submitted contain identical data, we will produce masks based in this data. We shall assume the responsibility for errors only if the mask ROM data on the products we produce differ from this data. Thus, the customer must be especially careful in verifying the data contained in the EPROMs submitted.

Microcomputer name : ☐ M37450M4TXXXSP ☐ M37450M4TXXXJ

Checksum code for entire EPROM					(hexadecimal notation)

EPROM type

☐ 2764	☐ 27128	☐ 27256
		

Set "FF_{16}" in the shaded area.

※2. Mark specification

Mark specification must be submitted using the correct form for the type package being ordered fill out the appropriate mark specification form (64P4B for M37450M4TXXXSP ; 84P0 for M37450M4TXXXJ) and attach to the mask ROM confirmation form.

※3. Comments

GZZ–SH01–00A< 76B0 >

Mask ROM number	

SERIES MELPS 740 MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M37450M8-XXXSP/FP
MITSUBISHI ELECTRIC

Receipt	Date :	
	Section head signature	Supervisor signature

Note : Please fill in all items marked※

※	Customer	Company name	TEL ( )	Issuance signature	Submitted by	Supervisor
		Date issued	Date :			

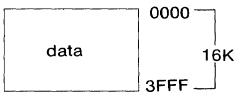
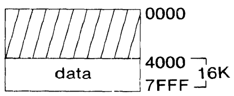
※ 1 . Confirmation

Specify the name of the product being ordered and the type of EPROMs submitted.
Three sets of EPROMs are required for each pattern (Check @ in the appropriate box).
If at least two of the three sets of EPROMs submitted contain identical data, we will produce masks based in this data. We shall assume the responsibility for errors only if the mask ROM data on the products we produce differ from this data. Thus, the customer must be especially careful in verifying the data contained in the EPROMs submitted.

Microcomputer name : ☐ M37450M8-XXXSP ☐ M37450M8-XXXFP

Checksum code for entire EPROM ☐☐☐☐ (hexadecimal notation)

EPROM type

☐ 27128	☐ 27256
	

Set "FF_{16}" in the shaded area

※ 2 . Mark specification

Mark specification must be submitted using the correct form for the type package being ordered fill out the appropriate mark specification form (64P4B for M37450M8-XXXSP ; 80P6 for M37450M8-XXXFP) and attach to the mask ROM confirmation form.

※ 3 . Comments

GZZ–SH03–89A〈0YA0〉

SERIES MELPS 740 MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M37451M4-XXXSP/FP/GP
MITSUBISHI ELECTRIC

Mask ROM number	

Receipt	Date :	
	Section head signature	Supervisor signature

Note : Please fill in all items marked※

※	Customer	Company name	TEL (　　　)	Issuance signature	Submitted by	Supervisor
		Date issued	Date :			

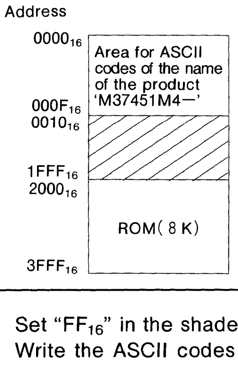
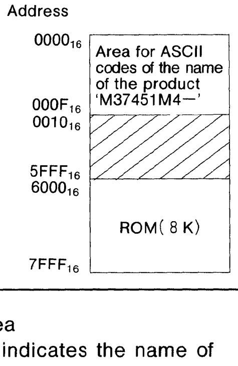
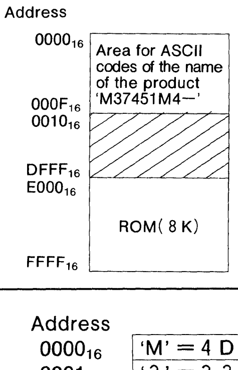
※1 . Confirmation

Specify the name of the product being ordered and the type of EPROMs submitted.
Three sets of EPROMs are required for each pattern (Check @ in the appropriate box).
If at least two of the three sets of EPROMs submitted contain identical data, we will produce masks based in this data. We shall assume the responsibility for errors only if the mask ROM data on the products we produce differ from this data. Thus, the customer must be especially careful in verifying the data contained in the EPROMs submitted.

Microcomputer name : ☐ M37451M4-XXXSP ☐ M37451M4-XXXFP ☐ M37451M4-XXXGP

Checksum code for entire EPROM ☐☐☐☐ (hexadecimal notation)

EPROM type

☐ 27128	☐ 27256	☐ 27512
		

(1) Set "FF_{16}" in the shaded area
(2) Write the ASCII codes that indicates the name of the product 'M37451M4—' to addresses 0000_{16} to $000F_{16}$. ASCII codes 'M37451M4—' are listed on the right. The addresses and data are in hexadecimal notation.

Address		Address	
0000_{16}	'M' = $4D_{16}$	0008_{16}	'—' = $2D_{16}$
0001_{16}	'3' = 33_{16}	0009_{16}	FF_{16}
0002_{16}	'7' = 37_{16}	$000A_{16}$	FF_{16}
0003_{16}	'4' = 34_{16}	$000B_{16}$	FF_{16}
0004_{16}	'5' = 35_{16}	$000C_{16}$	FF_{16}
0005_{16}	'1' = 31_{16}	$000D_{16}$	FF_{16}
0006_{16}	'M' = $4D_{16}$	$000E_{16}$	FF_{16}
0007_{16}	'4' = 34_{16}	$000F_{16}$	FF_{16}

GZZ–SH03–89A＜0YA0＞

Mask ROM number	

SERIES MELPS 740 MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M37451M4-XXXSP/FP/GP
MITSUBISHI ELECTRIC

Recommend to writing the following pseudo-command to the assembler source file :

EPROM type	27128	27256	27512
The pseudo-command	＊＝△$C000 △.BYTE△ 'M37451M4—'	＊＝△$8000 △.BYTE△ 'M37451M4—'	＊＝△$0000 △.BYTE△ 'M37451M4—'

Note : If the name of the product written to the EPROMs does not match the name of the mask confirmation, the ROM processing is disabled Write the data correctly.

※2. Mark specification

Mark specification must be submitted using the correct form for the type package being ordered fill out the appropriate mark specification form (64P4B for M37451M4-XXXSP ; 80P6N for M37451M4-XXXFP ; 80P6S for M37451M4-XXXGP) and attach to the mask ROM confirmation form.

※3. Comments

GZZ–SH03–95A〈0YA0〉

Mask ROM number	

Receipt	Date :	
	Section head signature	Supervisor signature

SERIES MELPS 740 MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M37451M4DXXXSP/FP
MITSUBISHI ELECTRIC

Note : Please fill in all items marked※.

※	Customer	Company name	TEL ( )	Issuance signature	Submitted by	Supervisor
		Date issued	Date :			

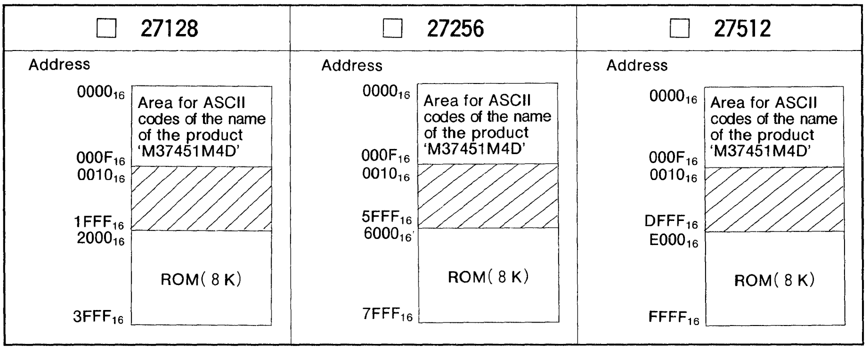
※1 . Confirmation

Specify the name of the product being ordered and the type of EPROMs submitted.
Three sets of EPROMs are required for each pattern (Check @ in the appropriate box).
If at least two of the three sets of EPROMs submitted contain identical data, we will produce masks based in this data. We shall assume the responsibility for errors only if the mask ROM data on the products we produce differ from this data. Thus, the customer must be especially careful in verifying the data contained in the EPROMs submitted.

Microcomputer name : ☐ M37451M4DXXXSP ☐ M37451M4DXXXFP

Checksum code for entire EPROM ☐☐☐☐ (hexadecimal notation)

EPROM type



(1) Set "FF$_{16}$" in the shaded area.
(2) Write the ASCII codes that indicates the name of the product 'M37451M4D' to addresses 0000$_{16}$ to 000F$_{16}$. ASCII codes 'M37451M4D' are listed on the right. The addresses and data are in hexadecimal notation.

Address		Address	
0000_{16}	'M' = 4 D$_{16}$	0008_{16}	'D' = 4 4$_{16}$
0001_{16}	'3' = 3 3$_{16}$	0009_{16}	F F$_{16}$
0002_{16}	'7' = 3 7$_{16}$	$000A_{16}$	F F$_{16}$
0003_{16}	'4' = 3 4$_{16}$	$000B_{16}$	F F$_{16}$
0004_{16}	'5' = 3 5$_{16}$	$000C_{16}$	F F$_{16}$
0005_{16}	'1' = 3 1$_{16}$	$000D_{16}$	F F$_{16}$
0006_{16}	'M' = 4 D$_{16}$	$000E_{16}$	F F$_{16}$
0007_{16}	'4' = 3 4$_{16}$	$000F_{16}$	F F$_{16}$

GZZ–SH03–95A＜0YA0＞

Mask ROM number	

SERIES MELPS 740 MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M37451M4DXXXSP/FP
MITSUBISHI ELECTRIC

Recommend to writing the following pseudo-command to the assembler source file :

EPROM type	27128	27256	27512
The pseudo-command	＊=△$C000 △.BYTE△ 'M37451M4D'	＊=△$8000 △.BYTE△ 'M37451M4D'	＊=△$0000 △.BYTE△ 'M37451M4D'

Note : If the name of the product written to the EPROMs does not match the name of the mask confirmation, the ROM processing is disabled. Write the data correctly.

※2. Mark specification

Mark specification must be submitted using the correct form for the type package being ordered fill out the appropriate mark specification form (64P4B for M37451M4DXXXSP ; 80P6N for M37451M4DXXXFP) and attach to the mask ROM confirmation form.

※3. Comments

GZZ–SH03–57A< 06A0 >

Mask ROM number	

SERIES MELPS 740 MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M37451M8-XXXSP/FP/GP
MITSUBISHI ELECTRIC

Receipt	Date :	
	Section head signature	Supervisor signature

Note : Please fill in all items marked※

※ Customer	Company name	TEL ( )	Issuance signature	Submitted by	Supervisor
	Date issued	Date :			

※ 1 . Confirmation

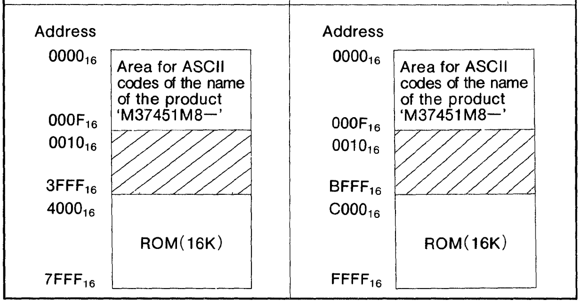
Specify the name of the product being ordered and the type of EPROMs submitted.
Three sets of EPROMs are required for each pattern (Check @ in the appropriate box).
If at least two of the three sets of EPROMs submitted contain identical data, we will produce masks based in this data. We shall assume the responsibility for errors only if the mask ROM data on the products we produce differ from this data. Thus, the customer must be especially careful in verifying the data contained in the EPROMs submitted.

Microcomputer name : ☐ M37451M8-XXXSP ☐ M37451M8-XXXFP ☐ M37451M8-XXXGP

Checksum code for entire EPROM ☐☐☐☐ (hexadecimal notation)

EPROM type

☐ 27256	☐ 27512



(1) Set "FF_{16}" in the shaded area.
(2) Write the ASCII codes that indicates the name of the product 'M37451M8—' to addresses 0000_{16} to $000F_{16}$. ASCII codes 'M37451M8—' are listed on the right. The addresses and data are in hexadecimal notation.

Address		Address	
0000_{16}	'M' = $4D_{16}$	0008_{16}	'—' = $2D_{16}$
0001_{16}	'3' = 33_{16}	0009_{16}	FF_{16}
0002_{16}	'7' = 37_{16}	$000A_{16}$	FF_{16}
0003_{16}	'4' = 34_{16}	$000B_{16}$	FF_{16}
0004_{16}	'5' = 35_{16}	$000C_{16}$	FF_{16}
0005_{16}	'1' = 31_{16}	$000D_{16}$	FF_{16}
0006_{16}	'M' = $4D_{16}$	$000E_{16}$	FF_{16}
0007_{16}	'8' = 38_{16}	$000F_{16}$	FF_{16}

GZZ—SH03—57A＜06A0＞

Mask ROM number	

SERIES MELPS 740 MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M37451M8-XXXSP/FP/GP
MITSUBISHI ELECTRIC

Recommend to writing the following pseudo-command to the assembler source file :

EPROM type	27256	27512
The pseudo-command	＊＝△$8000 △.BYTE△ 'M37451M8—'	＊＝△$0000 △.BYTE△ 'M37451M8—'

Note : If the name of the product written to the EPROMs does not match the name of the mask confirmation, the ROM processing is disabled. Write the data correctly.

※2. Mark specification

Mark specification must be submitted using the correct form for the type package being ordered fill out the appropriate mark specification form (64P4B for M37451M8-XXXSP ; 80P6N for M37451M8-XXXFP ; 80P6S for M37451M8-XXXGP) and attach to the mask ROM confirmation form.

※3. Comments

GZZ—SH03—96A＜0YA0＞

SERIES MELPS 740 MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M37451M8DXXXSP/FP
MITSUBISHI ELECTRIC

Mask ROM number	

Receipt	Date :	
	Section head signature	Supervisor signature

Note : Please fill in all items marked※

※ Customer	Company name	TEL (　　　)	Issuance signature	Submitted by	Supervisor
	Date issued	Date :			

※1. Confirmation

Specify the name of the product being ordered and the type of EPROMs submitted.

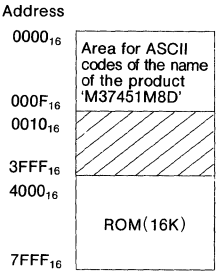
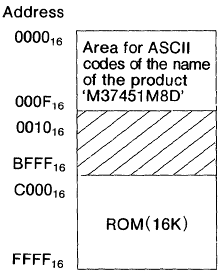
Three sets of EPROMs are required for each pattern (Check @ in the appropriate box).

If at least two of the three sets of EPROMs submitted contain identical data, we will produce masks based in this data. We shall assume the responsibility for errors only if the mask ROM data on the products we produce differ from this data. Thus, the customer must be especially careful in verifying the data contained in the EPROMs submitted.

Microcomputer name : ☐ M37451M8DXXXSP ☐ M37451M8DXXXFP

Checksum code for entire EPROM ☐☐☐☐ (hexadecimal notation)

EPROM type

☐ 27256	☐ 27512
	

(1) Set "FF_{15}" in the shaded area.

(2) Write the ASCII codes that indicates the name of the product 'M37451M8D' to addresses 0000_{16} to $000F_{16}$. ASCII codes 'M37451M8D' are listed on the right. The addresses and data are in hexadecimal notation.

Address		Address	
0000_{16}	'M' = 4 D$_{16}$	0008_{16}	'D' = 4 4$_{16}$
0001_{16}	'3' = 3 3$_{16}$	0009_{16}	F F$_{16}$
0002_{16}	'7' = 3 7$_{16}$	$000A_{16}$	F F$_{16}$
0003_{16}	'4' = 3 4$_{16}$	$000B_{16}$	F F$_{16}$
0004_{16}	'5' = 3 5$_{16}$	$000C_{16}$	F F$_{16}$
0005_{16}	'1' = 3 1$_{16}$	$000D_{16}$	F F$_{16}$
0006_{16}	'M' = 4 D$_{16}$	$000E_{16}$	F F$_{16}$
0007_{16}	'8' = 3 8$_{16}$	$000F_{16}$	F F$_{16}$

GZZ–SH03–96A〈0YA0〉

Mask ROM number	

SERIES MELPS 740 MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M37451M8DXXXSP/FP
MITSUBISHI ELECTRIC

Recommend to writing the following pseudo-command to the assembler source file :

EPROM type	27256	27512
The pseudo-command	∗=△$8000 △.BYTE△ 'M37451M8D'	∗=△$0000 △.BYTE△ 'M37451M8D'

Note : If the name of the product written to the EPROMs does not match the name of the mask confirmation, the ROM processing is disabled. Write the data correctly.

※2. Mark specification

Mark specification must be submitted using the correct form for the type package being ordered fill out the appropriate mark specification form (64P4B for M37451M8DXXXSP ; 80P6N for M37451M8DXXXFP) and attach to the mask ROM confirmation form.

※3. Comments

GZZ–SH03–91A＜0YA0＞

Mask ROM number	

Receipt	Date :	
	Section head signature	Supervisor signature

SERIES MELPS 740 MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M37451MC-XXXSP/FP/GP
MITSUBISHI ELECTRIC

Note : Please fill in all items marked※.

※ Customer	Company name	TEL ( )	Issuance signature	Submitted by	Supervisor
	Date issued	Date :			

※1 . Confirmation

Specify the name of the product being ordered and the type of EPROMs submitted.

Three sets of EPROMs are required for each pattern (Check @ in the appropriate box).

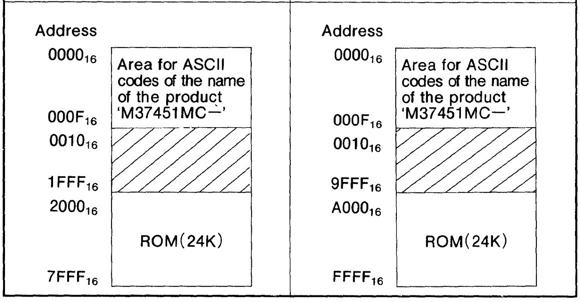
If at least two of the three sets of EPROMs submitted contain identical data, we will produce masks based in this data. We shall assume the responsibility for errors only if the mask ROM data on the products we produce differ from this data. Thus, the customer must be especially careful in verifying the data contained in the EPROMs submitted.

Microcomputer name : ☐ M37451MC-XXXSP ☐ M37451MC-XXXFP ☐ M37451MC-XXXGP

Checksum code for entire EPROM ☐☐☐☐ (hexadecimal notation)

EPROM type

☐ 27256	☐ 27512



(1) Set "FF_{16}" in the shaded area.

(2) Write the ASCII codes that indicates the name of the product 'M37451MC—' to addresses 0000_{16} to $000F_{16}$. ASCII codes 'M37451MC—' are listed on the right. The addresses and data are in hexadecimal notation.

Address		Address	
0000_{16}	'M' = 4 D_{16}	0008_{16}	'—' = 2 D_{16}
0001_{16}	'3' = 3 3_{16}	0009_{16}	F F_{16}
0002_{16}	'7' = 3 7_{16}	$000A_{16}$	F F_{16}
0003_{16}	'4' = 3 4_{16}	$000B_{16}$	F F_{16}
0004_{16}	'5' = 3 5_{16}	$000C_{16}$	F F_{16}
0005_{16}	'1' = 3 1_{16}	$000D_{16}$	F F_{16}
0006_{16}	'M' = 4 D_{16}	$000E_{16}$	F F_{16}
0007_{16}	'C' = 4 3_{16}	$000F_{16}$	F F_{16}

GZZ—SH03—91A〈0YA0〉

Mask ROM number	

SERIES MELPS 740 MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M37451MC-XXXSP/FP/GP
MITSUBISHI ELECTRIC

Recommend to writing the following pseudo-command to the assembler source file :

EPROM type	27256	27512
The pseudo-command	∗=△$8000 △.BYTE△ 'M37451MC—'	∗=△$0000 △.BYTE△ 'M37451MC—'

Note : If the name of the product written to the EPROMs does not match the name of the mask confirmation, the ROM processing is disabled. Write the data correctly.

※2. Mark specification

Mark specification must be submitted using the correct form for the type package being ordered fill out the appropriate mark specification form (64P4B for M37451MC-XXXSP ; 80P6N for M37451MC-XXXFP ; 80P6S for M37451MC-XXXGP) and attach to the mask ROM confirmation form.

※3. Comments

GZZ–SH02–91A＜9YA0＞

Mask ROM number	

Receipt	Date :	
	Section head signature	Supervisor signature

SERIES MELPS 740 MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M37470M2-XXXSP
MITSUBISHI ELECTRIC

Note : Please fill in all items marked※.

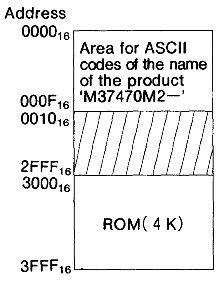
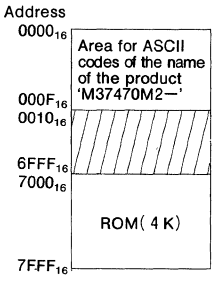
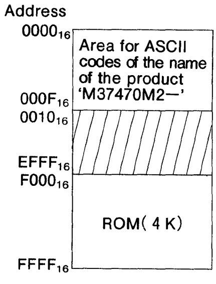
※ Customer	Company name	TEL ( )	Issuance signature	Submitted by	Supervisor
	Date issued	Date :			

※1 . Confirmation

Specify the name of the product being ordered and the type of EPROMs submitted.
Three sets of EPROMs are required for each pattern (Check @ in the appropriate box).
If at least two of the three sets of EPROMs submitted contain identical data, we will produce masks based in this data. We shall assume the responsibility for errors only if the mask ROM data on the products we produce differ from this data. Thus, the customer must be especially careful in verifying the data contained in the EPROMs submitted.

Checksum code for entire EPROM					(hexadecimal notation)

EPROM type

☐ 27128	☐ 27256	☐ 27512
		

(1) Set "FF_{16}" in the shaded area.
(2) Write the ASCII codes that indicates the name of the product 'M37470M2—' to addresses 0000_{16} to $000F_{16}$. ASCII codes 'M37470M2—' are listed on the right. The addresses and data are in hexadecimal notation.

Address		Address	
0000_{16}	'M' = 4 D_{16}	0008_{16}	'—' = 2 D_{16}
0001_{16}	'3' = 3 3_{16}	0009_{16}	F F_{16}
0002_{16}	'7' = 3 7_{16}	$000A_{16}$	F F_{16}
0003_{16}	'4' = 3 4_{16}	$000B_{16}$	F F_{16}
0004_{16}	'7' = 3 7_{16}	$000C_{16}$	F F_{16}
0005_{16}	'0' = 3 0_{16}	$000D_{16}$	F F_{16}
0006_{16}	'M' = 4 D_{16}	$000E_{16}$	F F_{16}
0007_{16}	'2' = 3 2_{16}	$000F_{16}$	F F_{16}

GZZ—SH02—91A<9YA0>

Mask ROM number	

SERIES MELPS 740 MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M37470M2-XXXSP
MITSUBISHI ELECTRIC

Recommend to writing the following pseudo-command to the start address of the assembler source program.

EPROM type	27128	27256	27512
The pseudo-command	∗=△$C000 △.BYTE△ 'M37470M2—'	∗=△$8000 △.BYTE△ 'M37470M2—'	∗=△$0000 △.BYTE△ 'M37470M2—'

Note : If the name of the product written to the EPROMs does not match the name of the mask confirmation, the ROM processing is disabled. Write the data correctly.

※2. Mark specification

Mark specification must be submitted using the correct form for the type package being ordered fill out the appropriate mark specification form (32P4B for M37470M2-XXXSP) and attach to the mask ROM confirmation form.

※3. Comments

GZZ–SH02–92A＜9YA0＞

Mask ROM number	

Receipt	Date :	
	Section head signature	Supervisor signature

SERIES MELPS 740 MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M37470M4-XXXSP
MITSUBISHI ELECTRIC

Note : Please fill in all items marked※

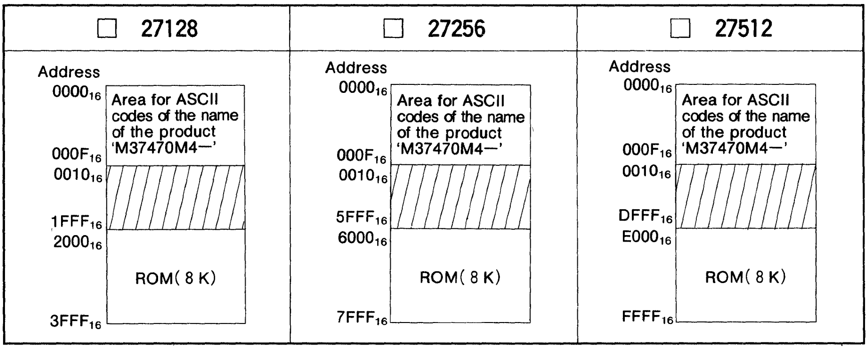
※	Customer	Company name	TEL (　　　)	Issuance signature	Submitted by	Supervisor
		Date issued	Date :			

※1 . Confirmation

Specify the name of the product being ordered and the type of EPROMs submitted.
Three sets of EPROMs are required for each pattern (Check @ in the appropriate box).
If at least two of the three sets of EPROMs submitted contain identical data, we will produce masks based in this data. We shall assume the responsibility for errors only if the mask ROM data on the products we produce differ from this data. Thus, the customer must be especially careful in verifying the data contained in the EPROMs submitted.

Checksum code for entire EPROM ☐☐☐☐ (hexadecimal notation)

EPROM type



(1) Set "FF_{16}" in the shaded area.

(2) Write the ASCII codes that indicates the name of the product 'M37470M4—' to addresses 0000_{16} to $000F_{16}$. ASCII codes 'M37470M4—' are listed on the right. The addresses and data are in hexadecimal notation.

Address		Address	
0000_{16}	'M' = $4D_{16}$	0008_{16}	'—' = $2D_{16}$
0001_{16}	'3' = 33_{16}	0009_{16}	FF_{16}
0002_{16}	'7' = 37_{16}	$000A_{16}$	FF_{16}
0003_{16}	'4' = 34_{16}	$000B_{16}$	FF_{16}
0004_{16}	'7' = 37_{16}	$000C_{16}$	FF_{16}
0005_{16}	'0' = 30_{16}	$000D_{16}$	FF_{16}
0006_{16}	'M' = $4D_{16}$	$000E_{16}$	FF_{16}
0007_{16}	'4' = 34_{16}	$000F_{16}$	FF_{16}

GZZ–SH02–92A＜9YA0＞

Mask ROM number	

SERIES MELPS 740 MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M37470M4-XXXSP
MITSUBISHI ELECTRIC

Recommend to writing the following pseudo-command to the start address of the assembler source program.

EPROM type	27128	27256	27512
The pseudo-command	＊=△$C000 △.BYTE△ 'M37470M4–'	＊=△$8000 △.BYTE△ 'M37470M4–'	＊=△$0000 △.BYTE△ 'M37470M4–'

Note : If the name of the product written to the EPROMs does not match the name of the mask confirmation, the ROM processing is disabled. Write the data correctly.

※2. Mark specification

Mark specification must be submitted using the correct form for the type package being ordered fill out the appropriate mark specification form (32P4B for M37470M4-XXXSP) and attach to the mask ROM confirmation form.

※3. Comments

GZZ—SH02—93A<9YA0>

SERIES MELPS 740 MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M37470M8-XXXSP
MITSUBISHI ELECTRIC

Mask ROM number	

Receipt	Date :	
	Section head signature	Supervisor signature

Note : Please fill in all items marked※.

※	Customer	Company name	TEL ( )	Issuance signature	Submitted by	Supervisor
		Date issued	Date :			

※1 . Confirmation

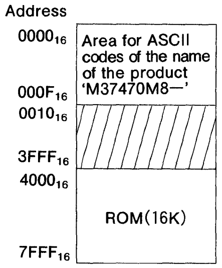
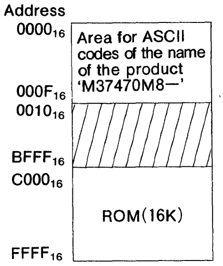
Specify the name of the product being ordered and the type of EPROMs submitted.

Three sets of EPROMs are required for each pattern (Check @ in the appropriate box).

If at least two of the three sets of EPROMs submitted contain identical data, we will produce masks based in this data. We shall assume the responsibility for errors only if the mask ROM data on the products we produce differ from this data. Thus, the customer must be especially careful in verifying the data contained in the EPROMs submitted.

Checksum code for entire EPROM ☐☐☐☐ (hexadecimal notation)

EPROM type

☐ 27256	☐ 27512
	

(1) Set "FF$_{16}$" in the shaded area.

(2) Write the ASCII codes that indicates the name of the product 'M37470M8—' to addresses 0000$_{16}$ to 000F$_{16}$. ASCII codes 'M37470M8—' are listed on the right. The addresses and data are in hexadecimal notation.

Address		Address	
0000$_{16}$	'M' = 4 D$_{16}$	0008$_{16}$	'—' = 2 D$_{16}$
0001$_{16}$	'3' = 3 3$_{16}$	0009$_{16}$	F F$_{16}$
0002$_{16}$	'7' = 3 7$_{16}$	000A$_{16}$	F F$_{16}$
0003$_{16}$	'4' = 3 4$_{16}$	000B$_{16}$	F F$_{16}$
0004$_{16}$	'7' = 3 7$_{16}$	000C$_{16}$	F F$_{16}$
0005$_{16}$	'0' = 3 0$_{16}$	000D$_{16}$	F F$_{16}$
0006$_{16}$	'M' = 4 D$_{16}$	000E$_{16}$	F F$_{16}$
0007$_{16}$	'8' = 3 8$_{16}$	000F$_{16}$	F F$_{16}$

GZZ—SH02—93A< 9YA0 >

Mask ROM number	

SERIES MELPS 740 MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M37470M8-XXXSP
MITSUBISHI ELECTRIC

Recommend to writing the following pseudo-command to the start address of the assembler source program.

EPROM type	27256	27512
The pseudo-command	＊=△$8000 △.BYTE△ 'M37470M8—'	＊=△$0000 △.BYTE△ 'M37470M8—'

Note : If the name of the product written to the EPROMs does not match the name of the mask confirmation, the ROM processing is disabled. Write the data correctly.

※2. Mark specification

Mark specification must be submitted using the correct form for the type package being ordered fill out the appropriate mark specification form (32P4B for M37470M8-XXXSP) and attach to the mask ROM confirmation form.

※3. Comments

GZZ–SH02–94A〈9YB0〉

Mask ROM number	

SERIES MELPS 740 MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M37471M2-XXXSP/FP
MITSUBISHI ELECTRIC

Receipt	Date :	
	Section head signature	Supervisor signature

Note : Please fill in all items marked※.

※	Customer	Company name	TEL ( )	Issuance signature	Submitted by	Supervisor
		Date issued	Date :			

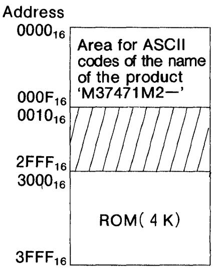
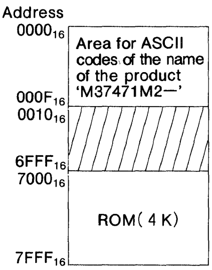
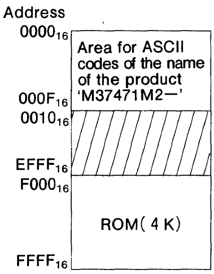
※1. Confirmation

Specify the name of the product being ordered and the type of EPROMs submitted.
Three sets of EPROMs are required for each pattern (Check @ in the appropriate box).
If at least two of the three sets of EPROMs submitted contain identical data, we will produce masks based in this data. We shall assume the responsibility for errors only if the mask ROM data on the products we produce differ from this data. Thus, the customer must be especially careful in verifying the data contained in the EPROMs submitted.

Microcomputer name : ☐ M37471M2-XXXSP ☐ M37471M2-XXXFP

Checksum code for entire EPROM ☐☐☐☐ (hexadecimal notation)

EPROM type

☐ 27128	☐ 27256	☐ 27512
		

(1) Set "FF_{16}" in the shaded area.
(2) Write the ASCII codes that indicates the name of the product 'M37471M2—' to addresses 0000_{16} to $000F_{16}$. ASCII codes 'M37471M2—' are listed on the right. The addresses and data are in hexadecimal notation.

Address		Address	
0000_{16}	'M' = $4D_{16}$	0008_{16}	'—' = $2D_{16}$
0001_{16}	'3' = 33_{16}	0009_{16}	FF_{16}
0002_{16}	'7' = 37_{16}	$000A_{16}$	FF_{16}
0003_{16}	'4' = 34_{16}	$000B_{16}$	FF_{16}
0004_{16}	'7' = 37_{16}	$000C_{16}$	FF_{16}
0005_{16}	'1' = 31_{16}	$000D_{16}$	FF_{16}
0006_{16}	'M' = $4D_{16}$	$000E_{16}$	FF_{16}
0007_{16}	'2' = 32_{16}	$000F_{16}$	FF_{16}

GZZ—SH02—94A< 9YB0 >

Mask ROM number	

SERIES MELPS 740 MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M37471M2-XXXSP/FP
MITSUBISHI ELECTRIC

Recommend to writing the following pseudo-command to the start address of the assembler source program.

EPROM type	27128	27256	27512
The pseudo-command	＊=△$C000 △.BYTE△ 'M37471M2—'	＊=△$8000 △.BYTE△ 'M37471M2—'	＊=△$0000 △.BYTE△ 'M37471M2—'

Note : If the name of the product written to the EPROMs does not match the name of the mask confirmation, the ROM processing is disabled. Write the data correctly.

※ 2. Mark specification

Mark specification must be submitted using the correct form for the type package being ordered fill out the appropriate mark specification form (42P4B for M37471M2-XXXSP ; 56P6N for M37471M2-XXXFP) and attach to the mask ROM confirmation form.

※ 3. Comments

GZZ—SH02—95A＜9YB0＞

Mask ROM number	

SERIES MELPS 740 MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M37471M4-XXXSP/FP
MITSUBISHI ELECTRIC

Receipt	Date :	
	Section head signature	Supervisor signature

Note : Please fill in all items marked※.

※ Customer	Company name	TEL ( )	Issuance signature	Submitted by	Supervisor
	Date issued	Date :			

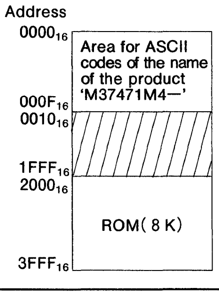
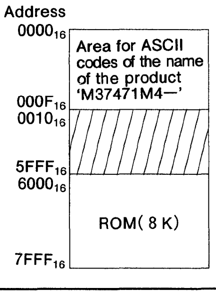
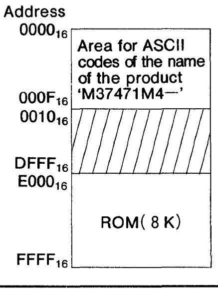
※ 1 . Confirmation

Specify the name of the product being ordered and the type of EPROMs submitted.
Three sets of EPROMs are required for each pattern (Check @ in the appropriate box).
If at least two of the three sets of EPROMs submitted contain identical data, we will produce masks based in this data. We shall assume the responsibility for errors only if the mask ROM data on the products we produce differ from this data. Thus, the customer must be especially careful in verifying the data contained in the EPROMs submitted.

Microcomputer name : ☐ M37471M4-XXXSP ☐ M37471M4-XXXFP

Checksum code for entire EPROM ☐☐☐☐ (hexadecimal notation)

EPROM type

☐ 27128	☐ 27256	☐ 27512
		

(1) Set "FF$_{16}$" in the shaded area.

(2) Write the ASCII codes that indicates the name of the product 'M37471M4—' to addresses 0000$_{16}$ to 000F$_{16}$. ASCII codes 'M37471M4—' are listed on the right. The addresses and data are in hexadecimal notation.

Address		Address	
0000$_{16}$	'M' = 4 D$_{16}$	0008$_{16}$	'—' = 2 D$_{16}$
0001$_{16}$	'3' = 3 3$_{16}$	0009$_{16}$	F F$_{16}$
0002$_{16}$	'7' = 3 7$_{16}$	000A$_{16}$	F F$_{16}$
0003$_{16}$	'4' = 3 4$_{16}$	000B$_{16}$	F F$_{16}$
0004$_{16}$	'7' = 3 7$_{16}$	000C$_{16}$	F F$_{16}$
0005$_{16}$	'1' = 3 1$_{16}$	000D$_{16}$	F F$_{16}$
0006$_{16}$	'M' = 4 D$_{16}$	000E$_{16}$	F F$_{16}$
0007$_{16}$	'4' = 3 4$_{16}$	000F$_{16}$	F F$_{16}$

GZZ—SH02—95A< 9YB0 >

Mask ROM number	

SERIES MELPS 740 MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M37471M4-XXXSP/FP
MITSUBISHI ELECTRIC

Recommend to writing the following pseudo-command to the start address of the assembler source program.

EPROM type	27128	27256	27512
The pseudo-command	*=△$C000 △.BYTE△ 'M37471M4—'	*=△$8000 △.BYTE△ 'M37471M4—'	*=△$0000 △.BYTE△ 'M37471M4—'

Note : If the name of the product written to the EPROMs does not match the name of the mask confirmation, the ROM processing is disabled. Write the data correctly.

※2. Mark specification

Mark specification must be submitted using the correct form for the type package being ordered fill out the appropriate mark specification form (42P4B for M37471M4-XXXSP ; 56P6N for M37471M4-XXXFP) and attach to the mask ROM confirmation form.

※3. Comments

GZZ—SH02—96A〈9YB0〉

Mask ROM number	

SERIES MELPS 740 MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M37471M8-XXXSP/FP
MITSUBISHI ELECTRIC

Receipt	Date :	
	Section head signature	Supervisor signature

Note : Please fill in all items marked※

※ Customer	Company name	TEL ( )	Issuance signature	Submitted by	Supervisor
	Date issued	Date :			

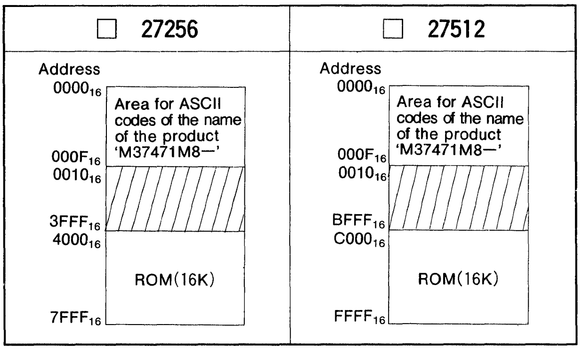
※1. Confirmation

Specify the name of the product being ordered and the type of EPROMs submitted.
Three sets of EPROMs are required for each pattern (Check @ in the appropriate box).
If at least two of the three sets of EPROMs submitted contain identical data, we will produce masks based in this data. We shall assume the responsibility for errors only if the mask ROM data on the products we produce differ from this data. Thus, the customer must be especially careful in verifying the data contained in the EPROMs submitted.

Microcomputer name : ☐ M37471M8-XXXSP ☐ M37471M8-XXXFP

Checksum code for entire EPROM ☐☐☐☐ (hexadecimal notation)

EPROM type



(1) Set "FF_{16}" in the shaded area.
(2) Write the ASCII codes that indicates the name of the product 'M37471M8—' to addresses 0000_{16} to $000F_{16}$. ASCII codes 'M37471M8—' are listed on the right. The addresses and data are in hexadecimal notation.

Address		Address	
0000_{16}	'M' = $4D_{16}$	0008_{16}	'—' = $2D_{16}$
0001_{16}	'3' = 33_{16}	0009_{16}	FF_{16}
0002_{16}	'7' = 37_{16}	$000A_{16}$	FF_{16}
0003_{16}	'4' = 34_{16}	$000B_{16}$	FF_{16}
0004_{16}	'7' = 37_{16}	$000C_{16}$	FF_{16}
0005_{16}	'1' = 31_{16}	$000D_{16}$	FF_{16}
0006_{16}	'M' = $4D_{16}$	$000E_{16}$	FF_{16}
0007_{16}	'8' = 38_{16}	$000F_{16}$	FF_{16}

GZZ–SH02–96A‹9YB0›

Mask ROM number	

SERIES MELPS 740 MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M37471M8-XXXSP/FP
MITSUBISHI ELECTRIC

Recommend to writing the following pseudo-command to the start address of the assembler source program.

EPROM type	27256	27512
The pseudo-command	＊=△$8000 △.BYTE△ 'M37471M8–'	＊=△$0000 △.BYTE△ 'M37471M8–'

Note : If the name of the product written to the EPROMs does not match the name of the mask confirmation, the ROM processing is disabled. Write the data correctly.

※2. Mark specification

Mark specification must be submitted using the correct form for the type package being ordered fill out the appropriate mark specification form (42P4B for M37471M8-XXXSP ; 56P6N for M37471M8-XXXFP) and attach to the mask ROM confirmation form.

※3. Comments

GZZ–SH04–34A＜13A0＞

Mask ROM number	

Receipt	Date :	
	Section head signature	Supervisor signature

SERIES MELPS 740 MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M38002M2-XXXSP/FP
MITSUBISHI ELECTRIC

Note : Please fill in all items marked※.

※	Customer	Company name	TEL (　　　)	Issuance signature	Submitted by	Supervisor
		Date issued	Date :			

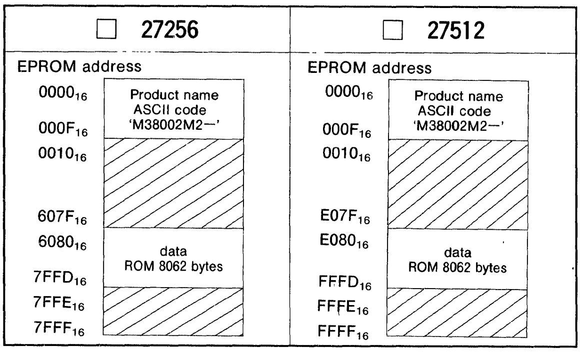
※ 1 . Confirmation

Specify the name of the product being ordered and the type of EPROMs submitted.
Three EPROMs are required for each pattern.
If at least two of the three sets of EPROMs submitted contain identical data, we will produce masks based on this data. We shall assume the responsibility for errors only if the mask ROM data on the products we produce differs from this data. Thus, extreme care must be taken to verify the data in the submitted EPROMs.

Microcomputer name : ☐ M38002M2-XXXSP ☐ M38002M2-XXXFP

Checksum code for entire EPROM ☐☐☐☐ (hexadecimal notation)

EPROM type (indicate the type used)



In the address space of the microcomputer, the internal ROM area is from address $E080_{16}$ to $FFFD_{16}$. The reset vector is stored in addresses $FFFC_{16}$ and $FFFD_{16}$.

(1) Set the data in the unused area (the shaded area of the diagram) to "FF_{16}".

(2) The ASCII codes of the product name "M38002M2–" must be entered in addresses 0000_{16} to 0008_{16}. The ASCII codes and addresses are listed to the right in hexadecimal notation.

Address		Address	
0000_{16}	'M' = $4D_{16}$	0008_{16}	'–' = $2D_{16}$
0001_{16}	'3' = 33_{16}	0009_{16}	FF_{16}
0002_{16}	'8' = 38_{16}	$000A_{16}$	FF_{16}
0003_{16}	'0' = 30_{16}	$000B_{16}$	FF_{16}
0004_{16}	'0' = 30_{16}	$000C_{16}$	FF_{16}
0005_{16}	'2' = 32_{16}	$000D_{16}$	FF_{16}
0006_{16}	'M' = $4D_{16}$	$000E_{16}$	FF_{16}
0007_{16}	'2' = 32_{16}	$000F_{16}$	FF_{16}

GZZ—SH04—34A〈13A0〉

Mask ROM number	

SERIES MELPS 740 MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M38002M2-XXXSP/FP
MITSUBISHI ELECTRIC

We recommend the use of the following pseudo-command to set the start address of the assembler source program.

EPROM type	27256	27512
The pseudo-command	*=△\$8000 .BYTE△ 'M38002M2—'	*=△\$0000 .BYTE△ 'M38002M2—'

Note : If the name of the product written to the EPROMs does not match the name of the mask confirmation form, the ROM will not be processed.

※2. Mark specification

Mark specification must be submitted using the correct form for the package being ordered. Fill out the appropriate mark specification form (64P4B for M38002M2-XXXSP, 64P6N for M38002M2-XXXFP) and attach it to the mask ROM confirmation form.

※3. Delivery standard

Choose the format of the specifications for the product to be delivered.

(1) Specifications for each ROM

☐ ROM code list unnecessary (standard).

☐ ROM code list necessary.

Note that each format has the same scope of guarantee. Therefore, the standard format is recommended.

※4. Usage conditions

Please answer the following questions about usage for use in our product inspection :

(1) How will you use the X_{IN}-X_{OUT} oscillator ?

☐ Ceramic resonator ☐ Quartz crystal

☐ External clock input ☐ Other (   )

At what frequency ? $f(X_{IN})=$ ☐ MHz

(2) In which operation mode will you use your microcomputer ?

☐ Single-chip mode ☐ Memory expansion mode

☐ Microprocessor mode

※5. Comments

GZZ—SH03—22A〈9YA0〉

Mask ROM number	

Receipt	Date :	
	Section head signature	Supervisor signature

SERIES MELPS 740 MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M38002M4-XXXSP/FP
MITSUBISHI ELECTRIC

Note : Please fill in all items marked※.

※ Customer	Company name	TEL ( )	Issuance signature		Submitted by	Supervisor
	Date issued	Date :				

※1 . Confirmation

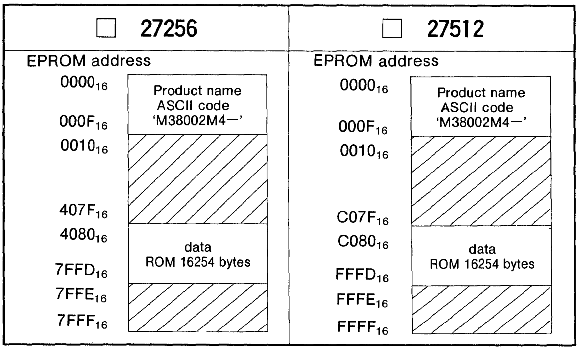
Specify the name of the product being ordered and the type of EPROMs submitted.

Three EPROMs are required for each pattern.

If at least two of the three sets of EPROMs submitted contain identical data, we will produce masks based on this data. We shall assume the responsibility for errors only if the mask ROM data on the products we produce differs from this data. Thus, extreme care must be taken to verify the data in the submitted EPROMs.

Microcomputer name : ☐ M38002M4-XXXSP ☐ M38002M4-XXXFP

Checksum code for entire EPROM ☐☐☐☐ (hexadecimal notation)



In the address space of the microcomputer, the internal ROM area is from address $C080_{16}$ to $FFFD_{16}$. The reset vector is stored in addresses $FFFC_{16}$ and $FFFD_{16}$.

(1) Set the data in the unused area (the shaded area of the diagram) to "FF_{16}".

(2) The ASCII codes of the product name "M38002M4—" must be entered in addresses 0000_{16} to 0008_{16}. The ASCII codes and addresses are listed to the right in hexadecimal notation.

Address		Address	
0000_{16}	'M' = 4 D_{16}	0008_{16}	'—' = 2 D_{16}
0001_{16}	'3' = 3 3_{16}	0009_{16}	F F_{16}
0002_{16}	'8' = 3 8_{16}	$000A_{16}$	F F_{16}
0003_{16}	'0' = 3 0_{16}	$000B_{16}$	F F_{16}
0004_{16}	'0' = 3 0_{16}	$000C_{16}$	F F_{16}
0005_{16}	'2' = 3 2_{16}	$000D_{16}$	F F_{16}
0006_{16}	'M' = 4 D_{16}	$000E_{16}$	F F_{16}
0007_{16}	'4' = 3 4_{16}	$000F_{16}$	F F_{16}

GZZ—SH03—22A＜9YA0＞

Mask ROM number	

SERIES MELPS 740 MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M38002M4-XXXSP/FP
MITSUBISHI ELECTRIC

We recommend the use of the following pseudo-command to set the start address of the assembler source program.

EPROM type	27256	27512
The pseudo-command	*=△\$8000 .BYTE△ 'M38002M4—'	*=△\$0000 .BYTE△ 'M38002M4—'

Note : If the name of the product written to the EPROMs does not match the name of the mask confirmation form, the ROM will not be processed.

※2. Mark specification

Mark specification must be submitted using the correct form for the package being ordered. Fill out the appropriate mark specification form (64P4B for M38002M4-XXXSP, 64P6N for M38002M4-XXXFP) and attach it to the mask ROM confirmation form.

※3. Delivery standard

Choose the format of the specifications for the product to be delivered.

(1) Specifications for each ROM

☐ ROM code list unnecessary (standard).

☐ ROM code list necessary.

Note that each format has the same scope of guarantee. Therefore, the standard format is recommended.

※4. Usage conditions

Please answer the following questions about usage for use in our product inspection :

(1) How will you use the X_{IN}-X_{OUT} oscillator ?

☐ Ceramic resonator ☐ Quartz crystal

☐ External clock input ☐ Other ( )

At what frequency ? $f(X_{IN})=$ ☐ MHz

(2) In which operation mode will you use your microcomputer ?

☐ Single-chip mode ☐ Memory expansion mode

☐ Microprocessor mode

※5. Comments

GZZ—SH04—30A〈13A0〉

SERIES MELPS 740 MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M38004M8-XXXSP/FP
MITSUBISHI ELECTRIC

Mask ROM number	

Receipt	Date :	
	Section head signature	Supervisor signature

Note : Please fill in all items marked※.

※	Customer	Company name	TEL ( )	Issuance signature	Submitted by	Supervisor
		Date issued	Date :			

※ 1 . Confirmation

Specify the name of the product being ordered and the type of EPROMs submitted.

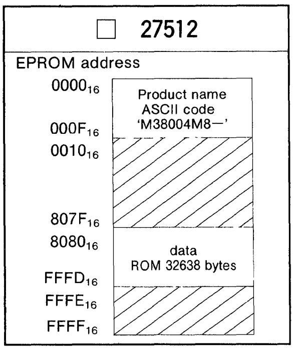
Three EPROMs are required for each pattern.

If at least two of the three sets of EPROMs submitted contain identical data, we will produce masks based on this data. We shall assume the responsibility for errors only if the mask ROM data on the products we produce differs from this data. Thus, extreme care must be taken to verify the data in the submitted EPROMs.

Microcomputer name : ☐ M38004M8-XXXSP ☐ M38004M8-XXXFP

Checksum code for entire EPROM ☐☐☐☐ (hexadecimal notation)

EPROM type (indicate the type used)



In the address space of the microcomputer, the internal ROM area is from address 8080_{16} to $FFFD_{16}$. The reset vector is stored in addresses $FFFC_{16}$ and $FFFD_{16}$.

(1) Set the data in the unused area (the shaded area of the diagram) to "FF_{16}".

(2) The ASCII codes of the product name "M38004M8—" must be entered in addresses 0000_{16} to 0008_{16}. The ASCII codes and addresses are listed to the right in hexadecimal notation.

Address		Address	
0000_{16}	'M' = 4 D_{16}	0008_{16}	'—' = 2 D_{16}
0001_{16}	'3' = 3 3_{16}	0009_{16}	F F_{16}
0002_{16}	'8' = 3 8_{16}	$000A_{16}$	F F_{16}
0003_{16}	'0' = 3 0_{16}	$000B_{16}$	F F_{16}
0004_{16}	'0' = 3 0_{16}	$000C_{16}$	F F_{16}
0005_{16}	'4' = 3 4_{16}	$000D_{16}$	F F_{16}
0006_{16}	'M' = 4 D_{16}	$000E_{16}$	F F_{16}
0007_{16}	'8' = 3 8_{16}	$000F_{16}$	F F_{16}

GZZ—SH04—30A<13A0>

Mask ROM number	

SERIES MELPS 740 MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M38004M8-XXXSP/FP
MITSUBISHI ELECTRIC

We recommend the use of the following pseudo-command to set the start address of the assembler source program.

EPROM type	27256	27512
The pseudo-command	*=△$8000 .BYTE△ 'M38004M8—'	*=△$0000 .BYTE△ 'M38004M8—'

Note : If the name of the product written to the EPROMs does not match the name of the mask confirmation form, the ROM will not be processed.

※ 2. Mark specification

Mark specification must be submitted using the correct form for the package being ordered. Fill out the appropriate mark specification form (64P4B for M38004M8-XXXSP, 64P6N for M38004M8-XXXFP) and attach it to the mask ROM confirmation form.

※ 3. Delivery standard

Choose the format of the specifications for the product to be delivered.

(1) Specifications for each ROM

☐ ROM code list unnecessary (standard).

☐ ROM code list necessary.

Note that each format has the same scope of guarantee. Therefore, the standard format is recommended.

※ 4. Usage conditions

Please answer the following questions about usage for use in our product inspection :

(1) How will you use the X_{IN}-X_{OUT} oscillator ?

☐ Ceramic resonator ☐ Quartz crystal

☐ External clock input ☐ Other ( )

At what frequency ? $f(X_{IN})=$ ☐ MHz

(2) In which operation mode will you use your microcomputer ?

☐ Single-chip mode ☐ Memory expansion mode

☐ Microprocessor mode

※ 5. Comments

GZZ—SH04—28A〈13A0〉

Mask ROM number	

SERIES MELPS 740 MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M38007M4-XXXSP/FP
MITSUBISHI ELECTRIC

Receipt	Date :	
	Section head signature	Supervisor signature

Note : Please fill in all items marked※.

※	Customer	Company name	TEL (　　　)	Issuance signature	Submitted by	Supervisor
		Date issued	Date :			

※ 1 . Confirmation

Specify the name of the product being ordered and the type of EPROMs submitted.

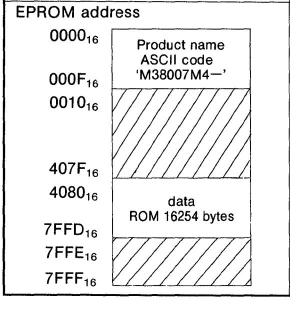
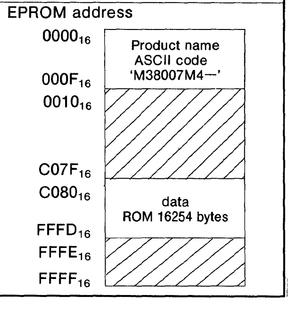
Three EPROMs are required for each pattern.

If at least two of the three sets of EPROMs submitted contain identical data, we will produce masks based on this data. We shall assume the responsibility for errors only if the mask ROM data on the products we produce differs from this data. Thus, extreme care must be taken to verify the data in the submitted EPROMs.

Microcomputer name :　☐ M38007M4-XXXSP　☐ M38007M4-XXXFP

Checksum code for entire EPROM ☐☐☐☐ (hexadecimal notation)

EPROM type (indicate the type used)

☐ 27256	☐ 27512
	

In the address space of the microcomputer, the internal ROM area is from address $C080_{16}$ to $FFFD_{16}$. The reset vector is stored in addresses $FFFC_{16}$ and $FFFD_{16}$.

(1) Set the data in the unused area (the shaded area of the diagram) to "FF_{16}".

(2) The ASCII codes of the product name "M38007M4—" must be entered in addresses 0000_{16} to 0008_{16}. The ASCII codes and addresses are listed to the right in hexadecimal notation.

Address		Address	
0000_{16}	'M' = $4D_{16}$	0008_{16}	'—' = $2D_{16}$
0001_{16}	'3' = 33_{16}	0009_{16}	FF_{16}
0002_{16}	'8' = 38_{16}	$000A_{16}$	FF_{16}
0003_{16}	'0' = 30_{16}	$000B_{16}$	FF_{16}
0004_{16}	'0' = 30_{16}	$000C_{16}$	FF_{16}
0005_{16}	'7' = 37_{16}	$000D_{16}$	FF_{16}
0006_{16}	'M' = $4D_{16}$	$000E_{16}$	FF_{16}
0007_{16}	'4' = 34_{16}	$000F_{16}$	FF_{16}

GZZ−SH04−28A〈13A0〉

Mask ROM number	

SERIES MELPS 740 MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M38007M4-XXXSP/FP
MITSUBISHI ELECTRIC

We recommend the use of the following pseudo-command to set the start address of the assembler source program.

EPROM type	27256	27512
The pseudo-command	*=△$8000 .BYTE△ 'M38007M4−'	*=△$0000 .BYTE△ 'M38007M4−'

Note : If the name of the product written to the EPROMs does not match the name of the mask confirmation form, the ROM will not be processed.

※ 2. Mark specification

Mark specification must be submitted using the correct form for the package being ordered. Fill out the appropriate mark specification form (64P4B for M38007M4-XXXSP, 64P6N for M38007M4-XXXFP) and attach it to the mask ROM confirmation form.

※ 3. Delivery standard

Choose the format of the specifications for the product to be delivered.

(1) Specifications for each ROM

☐ ROM code list unnecessary (standard).

☐ ROM code list necessary.

Note that each format has the same scope of guarantee. Therefore, the standard format is recommended.

※ 4. Usage conditions

Please answer the following questions about usage for use in our product inspection :

(1) How will you use the X_{IN}-X_{OUT} oscillator ?

☐ Ceramic resonator ☐ Quartz crystal

☐ External clock input ☐ Other (   )

At what frequency ? $f(X_{IN})=$ ☐ MHz

(2) In which operation mode will you use your microcomputer ?

☐ Single-chip mode ☐ Memory expansion mode

☐ Microprocessor mode

※ 5. Comments

GZZ—SH03—63A＜07A0＞

Mask ROM number	

Receipt	Date :	
	Section head signature	Supervisor signature

SERIES MELPS 740 MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M38062M3-XXXFP/GP
MITSUBISHI ELECTRIC

Note : Please fill in all items marked※.

※	Customer	Company name	TEL ( )	Issuance signature	Submitted by	Supervisor
		Date issued	Date :			

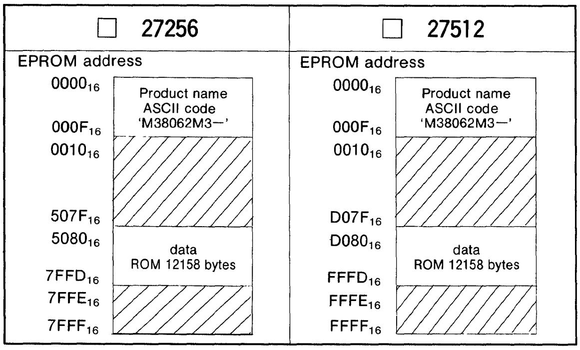
※1 . Confirmation

Specify the name of the product being ordered and the type of EPROMs submitted.
Three EPROMs are required for each pattern.
If at least two of the three sets of EPROMs submitted contain identical data, we will produce masks based on this data. We shall assume the responsibility for errors only if the mask ROM data on the products we produce differs from this data. Thus, extreme care must be taken to verify the data in the submitted EPROMs.

Microcomputer name : ☐ M38062M3-XXXFP ☐ M38062M3-XXXGP

Checksum code for entire EPROM ☐☐☐☐ (hexadecimal notation)

EPROM type (indicate the type used)



In the address space of the microcomputer, the internal ROM area is from address D080$_{16}$ to FFFD$_{16}$. The reset vector is stored in addresses FFFC$_{16}$ and FFFD$_{16}$.

(1) Set the data in the unused area (the shaded area of the diagram) to "FF$_{16}$".

(2) The ASCII codes of the product name "M38062M3—" must be entered in addresses 0000$_{16}$ to 0008$_{16}$. The ASCII codes and addresses are listed to the right in hexadecimal notation.

Address		Address	
0000$_{16}$	'M' = 4 D$_{16}$	0008$_{16}$	'—' = 2 D$_{16}$
0001$_{16}$	'3' = 3 3$_{16}$	0009$_{16}$	F F$_{16}$
0002$_{16}$	'8' = 3 8$_{16}$	000A$_{16}$	F F$_{16}$
0003$_{16}$	'0' = 3 0$_{16}$	000B$_{16}$	F F$_{16}$
0004$_{16}$	'6' = 3 6$_{16}$	000C$_{16}$	F F$_{16}$
0005$_{16}$	'2' = 3 2$_{16}$	000D$_{16}$	F F$_{16}$
0006$_{16}$	'M' = 4 D$_{16}$	000E$_{16}$	F F$_{16}$
0007$_{16}$	'3' = 3 3$_{16}$	000F$_{16}$	F F$_{16}$

GZZ–SH03–63A〈07A0〉

Mask ROM number	

SERIES MELPS 740 MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M38062M3-XXXFP/GP
MITSUBISHI ELECTRIC

We recommend the use of the following pseudo-command to set the start address of the assembler source program.

EPROM type	27256	27512
The pseudo-command	*=△$8000 .BYTE△ 'M38062M3–'	*=△$0000 .BYTE△ 'M38062M3–'

Note : If the name of the product written to the EPROMs does not match the name of the mask confirmation form, the ROM will not be processed.

※ 2. Mark specification

Mark specification must be submitted using the correct form for the package being ordered. Fill out the appropriate mark specification form (80P6N for M38062M3-XXXFP, 80P6S for M38062M3-XXXGP) and attach it to the mask ROM confirmation form.

※ 3. Delivery standard

Choose the format of the specifications for the product to be delivered.

(1) Specifications for each ROM

☐ ROM code list unnecessary (standard).

☐ ROM code list necessary.

Note that each format has the same scope of guarantee. Therefore, the standard format is recommended.

※ 4. Usage conditions

Please answer the following questions about usage for use in our product inspection :

(1) How will you use the X_{IN}-X_{OUT} oscillator ?

☐ Ceramic resonator ☐ Quartz crystal

☐ External clock input ☐ Other (   )

At what frequency ? $f(X_{IN})=$ ☐ MHz

(2) In which operation mode will you use your microcomputer ?

☐ Single-chip mode ☐ Memory expansion mode

☐ Microprocessor mode

※ 5. Comments

GZZ—SH03—26A〈 9YA0 〉

Mask ROM number	

SERIES MELPS 740 MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M38063M6-XXXFP/GP
MITSUBISHI ELECTRIC

Receipt	Date :	
	Section head signature	Supervisor signature

Note : Please fill in all items marked※.

※	Customer	Company name	TEL ( )	Issuance signature	Submitted by	Supervisor
		Date issued	Date :			

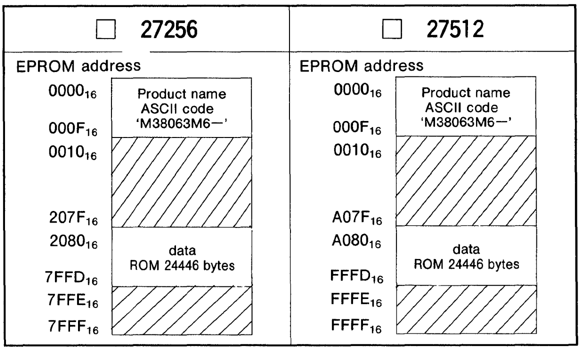
※ 1 . Confirmation

Specify the name of the product being ordered and the type of EPROMs submitted.
Three EPROMs are required for each pattern.
If at least two of the three sets of EPROMs submitted contain identical data, we will produce masks based on this data. We shall assume the responsibility for errors only if the mask ROM data on the products we produce differs from this data. Thus, extreme care must be taken to verify the data in the submitted EPROMs.

Microcomputer name : ☐ M38063M6-XXXFP ☐ M38063M6-XXXGP

Checksum code for entire EPROM ☐☐☐☐ (hexadecimal notation)

EPROM type (indicate the type used)



In the address space of the microcomputer, the internal ROM area is from address $A080_{16}$ to $FFFD_{16}$. The reset vector is stored in addresses $FFFC_{16}$ and $FFFD_{16}$.

(1) Set the data in the unused area (the shaded area of the diagram) to "FF_{16}".

(2) The ASCII codes of the product name "M38063M6—" must be entered in addresses 0000_{16} to 0008_{16}. The ASCII codes and addresses are listed to the right in hexadecimal notation.

Address		Address	
0000_{16}	'M' = $4D_{16}$	0008_{16}	'—' = $2D_{16}$
0001_{16}	'3' = 33_{16}	0009_{16}	FF_{16}
0002_{16}	'8' = 38_{16}	$000A_{16}$	FF_{16}
0003_{16}	'0' = 30_{16}	$000B_{16}$	FF_{16}
0004_{16}	'6' = 36_{16}	$000C_{16}$	FF_{16}
0005_{16}	'3' = 33_{16}	$000D_{16}$	FF_{16}
0006_{16}	'M' = $4D_{16}$	$000E_{16}$	FF_{16}
0007_{16}	'6' = 36_{16}	$000F_{16}$	FF_{16}

GZZ–SH03–26A<9YA0>

Mask ROM number	

SERIES MELPS 740 MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M38063M6-XXXFP/GP
MITSUBISHI ELECTRIC

We recommend the use of the following pseudo-command to set the start address of the assembler source program.

EPROM type	27256	27512
The pseudo-command	*=△$8000 .BYTE△ 'M38063M6–'	*=△$0000 .BYTE△ 'M38063M6–'

Note : If the name of the product written to the EPROMs does not match the name of the mask confirmation form, the ROM will not be processed.

※ 2. Mark specification

Mark specification must be submitted using the correct form for the package being ordered. Fill out the appropriate mark specification form (80P6N for M38063M6-XXXFP, 80P6S for M38063M6-XXXGP) and attach it to the mask ROM confirmation form.

※ 3. Delivery standard

Choose the format of the specifications for the product to be delivered.

(1) Specifications for each ROM

☐ ROM code list unnecessary (standard).

☐ ROM code list necessary.

Note that each format has the same scope of guarantee. Therefore, the standard format is recommended.

※ 4. Usage conditions

Please answer the following questions about usage for use in our product inspection :

(1) How will you use the X_{IN}-X_{OUT} oscillator ?

☐ Ceramic resonator ☐ Quartz crystal

☐ External clock input ☐ Other (   )

At what frequency ? $f(X_{IN})=$ ☐ MHz

(2) In which operation mode will you use your microcomputer ?

☐ Single-chip mode ☐ Memory expansion mode

☐ Microprocessor mode

※ 5. Comments

GZZ–SH03–27A＜9ZA1＞

SERIES MELPS 740 MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M38102M5-XXXSP/FP
MITSUBISHI ELECTRIC

Mask ROM number	

Receipt	Date :	
	Section head signature	Supervisor signature

Note : Please fill in all items marked※.

※ Customer	Company name	TEL ( )	Issuance signature	Submitted by	Supervisor
	Date issued	Date :			

※ 1 . Confirmation

Specify the name of the product being ordered and the type of EPROMs submitted.

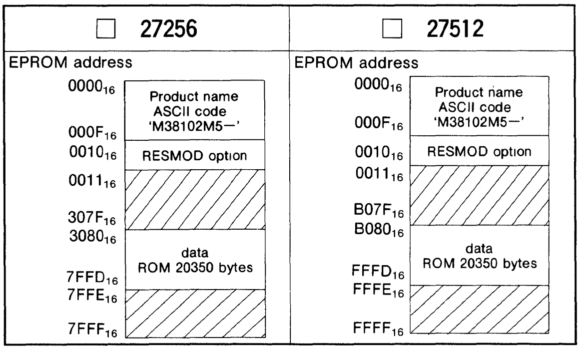
Three EPROMs are required for each pattern.

If at least two of the three sets of EPROMs submitted contain identical data, we will produce masks based on this data. We shall assume the responsibility for errors only if the mask ROM data on the products we produce differs from this data. Thus, extreme care must be taken to verify the data in the submitted EPROMs.

Microcomputer name : ☐ M38102M5-XXXSP ☐ M38102M5-XXXFP

Checksum code for entire EPROM ☐☐☐☐ (hexadecimal notation)

EPROM type (indicate the type used)



In the address space of the microcomputer, the internal ROM area is from address $B080_{16}$ to $FFFD_{16}$. The reset vector is stored in addresses $FFFC_{16}$ and $FFFD_{16}$

(1) Set the data in the unused area (the shaded area of the diagram) to "FF_{16}".

(2) The ASCII codes of the product name "M38102M5–" must be entered in addresses 0000_{16} to 0008_{16}. The ASCII codes and addresses are listed to the right in hexadecimal notation.

Address		Address	
0000_{16}	'M' = 4 D_{16}	0008_{16}	'–' = 2 D_{16}
0001_{16}	'3' = 3 3_{16}	0009_{16}	F F_{16}
0002_{16}	'8' = 3 8_{16}	$000A_{16}$	F F_{16}
0003_{16}	'1' = 3 1_{16}	$000B_{16}$	F F_{16}
0004_{16}	'0' = 3 0_{16}	$000C_{16}$	F F_{16}
0005_{16}	'2' = 3 2_{16}	$000D_{16}$	F F_{16}
0006_{16}	'M' = 4 D_{16}	$000E_{16}$	F F_{16}
0007_{16}	'5' = 3 5_{16}	$000F_{16}$	F F_{16}

GZZ–SH03–27A＜9ZA1＞

Mask ROM number	

SERIES MELPS 740 MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M38102M5-XXXSP/FP
MITSUBISHI ELECTRIC

We recommend the use of the following pseudo-command to set the start address of the assembler source program.

EPROM type	27256	27512
The pseudo-command	＊=△$8000 .BYTE△ 'M38102M5–'	＊=△$0000 .BYTE△ 'M38102M5–'

Note : If the name of the product written to the EPROMs does not match the name of the mask confirmation form, the ROM will not be processed.

※2. Option specification (write the option data also to the specified address of the EPROM)

Reset mode switching option

☐ Normal operation start mode ··············· 01_{16}

☐ Low-speed operation start mode ··············· 00_{16}

Address 0010_{16}

We recommend the use of the following pseudo-command to set the start address of the assembler source program.

EPROM type	27256	27512
Reset mode option	＊=△$8010 .BYTE△ $XX	＊=△$0010 .BYTE△ $XX

Note : If the name of the product written to the EPROMs does not match the name of the mask confirmation form, the ROM will not be processed. Write the data correctly. As for the option, if the contents of the confirmation and conflict with those of the EPROM, the contents of the EPROM are preferred.

※3. Mark specification

Mark specification must be submitted using the correct form for the package being ordered. Fill out the appropriate mark specification form (64P4B for M38102M5-XXXSP, 64P6N for M38102M5-XXXFP) and attach it to the mask ROM confirmation form.

※4. Delivery standard

Choose the format of the specifications for the product to be delivered.

(1) Specifications for each ROM

☐ ROM code list unnecessary (standard).

☐ ROM code list necessary.

Note that each format has the same scope of guarantee. Therefore, the standard format is recommended.

GZZ—SH03—27A‹9ZA1›

Mask ROM number	

SERIES MELPS 740 MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M38102M5-XXXSP/FP
MITSUBISHI ELECTRIC

※5. Usage conditions

Please answer the following questions about usage for use in our product inspection :

(1) How will you use the X_{IN}-X_{OUT} oscillator ?

☐ Ceramic resonator ☐ Quartz crystal
☐ External clock input ☐ Other (   )

At what frequency ? $f(X_{IN})=$ ☐ MHz

(2) How will you use the X_{CIN}-X_{COUT} oscillator ?

☐ Ceramic resonator ☐ Quartz crystal
☐ External clock input ☐ Other (   )

At what frequency ? $f(X_{CIN})=$ ☐ kHz

※6. Comments

GZZ–SH03–61A〈07A0〉

SERIES MELPS 740 MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M38103M6-XXXSP/FP
MITSUBISHI ELECTRIC

Mask ROM number	

Receipt	Date :	
	Section head signature	Supervisor signature

Note : Please fill in all items marked※.

※	Customer	Company name	TEL ( )	Issuance signature	Submitted by	Supervisor
		Date issued	Date :			

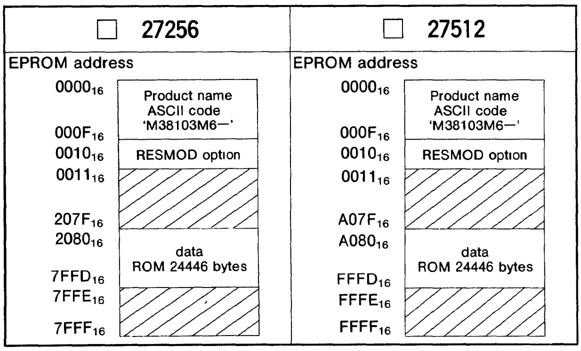
※1 . Confirmation

Specify the name of the product being ordered and the type of EPROMs submitted.
Three EPROMs are required for each pattern.
If at least two of the three sets of EPROMs submitted contain identical data, we will produce masks based on this data. We shall assume the responsibility for errors only if the mask ROM data on the products we produce differs from this data. Thus, extreme care must be taken to verify the data in the submitted EPROMs.

Microcomputer name : ☐ M38103M6-XXXSP ☐ M38103M6-XXXFP

Checksum code for entire EPROM ☐☐☐☐ (hexadecimal notation)

EPROM type (indicate the type used)



In the address space of the microcomputer, the internal ROM area is from address $A080_{16}$ to $FFFD_{16}$. The reset vector is stored in addresses $FFFC_{16}$ and $FFFD_{16}$.

(1) Set the data in the unused area (the shaded area of the diagram) to "FF_{16}".

(2) The ASCII codes of the product name "M38103M6–" must be entered in addresses 0000_{16} to 0008_{16}. The ASCII codes and addresses are listed to the right in hexadecimal notation.

Address		Address	
0000_{16}	'M' = 4 D_{16}	0008_{16}	'–' = 2 D_{16}
0001_{16}	'3' = 3 3_{16}	0009_{16}	F F_{16}
0002_{16}	'8' = 3 8_{16}	$000A_{16}$	F F_{16}
0003_{16}	'1' = 3 1_{16}	$000B_{16}$	F F_{16}
0004_{16}	'0' = 3 0_{16}	$000C_{16}$	F F_{16}
0005_{16}	'3' = 3 3_{16}	$000D_{16}$	F F_{16}
0006_{16}	'M' = 4 D_{16}	$000E_{16}$	F F_{16}
0007_{16}	'6' = 3 6_{16}	$000F_{16}$	F F_{16}

GZZ–SH03–61A<07A0>

Mask ROM number	

SERIES MELPS 740 MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M38103M6-XXXSP/FP
MITSUBISHI ELECTRIC

We recommend the use of the following pseudo-command to set the start address of the assembler source program.

EPROM type	27256	27512
The pseudo-command	∗=△$8000 .BYTE△ 'M38103M6–'	∗=△$0000 .BYTE△ 'M38103M6–'

Note : If the name of the product written to the EPROMs does not match the name of the mask confirmation form, the ROM will not be processed.

※2. Option specification (write the option data also to the specified address of the EPROM)

Reset mode switching option

☐ Normal operation start mode ···············	01_{16}	Address 0010_{16}
☐ Low-speed operation start mode ···············	00_{16}	

We recommend the use of the following pseudo-command to set the start address of the assembler source program.

EPROM type	27256	27512
Reset mode option	∗=△$8010 .BYTE△ $XX	∗=△$0010 .BYTE△ $XX

Note : If the name of the product written to the EPROMs does not match the name of the mask confirmation form, the ROM will not be processed. Write the data correctly. As for the option, if the contents of the confirmation and conflict with those of the EPROM, the contents of the EPROM are preferred.

※3. Mark specification

Mark specification must be submitted using the correct form for the package being ordered. Fill out the appropriate mark specification form (64P4B for M38103M6-XXXSP, 64P6N for M38103M6-XXXFP) and attach it to the mask ROM confirmation form.

※4. Delivery standard

Choose the format of the specifications for the product to be delivered.

(1) Specifications for each ROM

☐ ROM code list unnecessary (standard).

☐ ROM code list necessary.

Note that each format has the same scope of guarantee. Therefore, the standard format is recommended.

GZZ–SH03–61A<07A0>

Mask ROM number	

SERIES MELPS 740 MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M38103M6-XXXSP/FP
MITSUBISHI ELECTRIC

※5. Usage conditions

Please answer the following questions about usage for use in our product inspection :

(1) How will you use the X_{IN}-X_{OUT} oscillator ?

☐ Ceramic resonator ☐ Quartz crystal

☐ External clock input ☐ Other ( )

At what frequency ? $f(X_{IN})=$ ☐ MHz

(2) How will you use the X_{CIN}-X_{COUT} oscillator ?

☐ Ceramic resonator ☐ Quartz crystal

☐ External clock input ☐ Other ( )

At what frequency ? $f(X_{CIN})=$ ☐ kHz

※6. Comments

GZZ—SH03—49A＜03A0＞

SERIES MELPS 740 MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M38112M4-XXXSP/FP
MITSUBISHI ELECTRIC

Mask ROM number	

Receipt	Date :	
	Section head signature	Supervisor signature

Note : Please fill in all items marked※.

※	Customer	Company name	TEL ( )	Issuance signature	Submitted by	Supervisor
		Date issued	Date :			

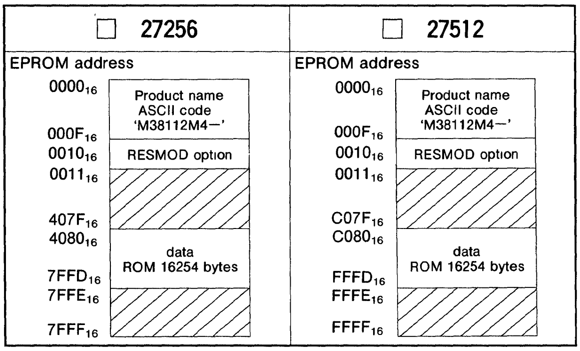
※ 1 . Confirmation

Specify the name of the product being ordered and the type of EPROMs submitted.
Three EPROMs are required for each pattern.
If at least two of the three sets of EPROMs submitted contain identical data, we will produce masks based on this data. We shall assume the responsibility for errors only if the mask ROM data on the products we produce differs from this data. Thus, extreme care must be taken to verify the data in the submitted EPROMs.

Microcomputer name : ☐ M38112M4-XXXSP ☐ M38112M4-XXXFP

Checksum code for entire EPROM ☐☐☐☐ (hexadecimal notation)

EPROM type (indicate the type used)



In the address space of the microcomputer, the internal ROM area is from address $C080_{16}$ to $FFFD_{16}$. The reset vector is stored in addresses $FFFC_{16}$ and $FFFD_{16}$.

(1) Set the data in the unused area (the shaded area of the diagram) to "FF_{16}".

(2) The ASCII codes of the product name "M38112M4—" must be entered in addresses 0000_{16} to 0008_{16}. The ASCII codes and addresses are listed to the right in hexadecimal notation.

Address		Address	
0000_{16}	'M' = 4 D_{16}	0008_{16}	'—' = 2 D_{16}
0001_{16}	'3' = 3 3_{16}	0009_{16}	F F_{16}
0002_{16}	'8' = 3 8_{16}	$000A_{16}$	F F_{16}
0003_{16}	'1' = 3 1_{16}	$000B_{16}$	F F_{16}
0004_{16}	'1' = 3 1_{16}	$000C_{16}$	F F_{16}
0005_{16}	'2' = 3 2_{16}	$000D_{16}$	F F_{16}
0006_{16}	'M' = 4 D_{16}	$000E_{16}$	F F_{16}
0007_{16}	'4' = 3 4_{16}	$000F_{16}$	F F_{16}

GZZ–SH03–49A＜03A0＞

Mask ROM number	

SERIES MELPS 740 MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M38112M4-XXXSP/FP
MITSUBISHI ELECTRIC

We recommend the use of the following pseudo-command to set the start address of the assembler source program.

EPROM type	27256	27512
The pseudo-command	＊=△$8000 .BYTE△ 'M38112M4–'	＊=△$0000 .BYTE△ 'M38112M4–'

Note : If the name of the product written to the EPROMs does not match the name of the mask confirmation form, the ROM will not be processed.

※2. Option specification (write the option data also to the specified address of the EPROM)

Reset mode switching option

☐ Normal operation start mode ··············· 01_{16}

☐ Low-speed operation start mode ··············· 00_{16}

Address 0010_{16}

We recommend the use of the following pseudo-command to set the start address of the assembler source program.

EPROM type	27256	27512
Reset mode option	＊=△$8010 .BYTE△ $XX	＊=△$0010 .BYTE△ $XX

Note : If the name of the product written to the EPROMs does not match the name of the mask confirmation form, the ROM will not be processed. Write the data correctly. As for the option, if the contents of the confirmation and conflict with those of the EPROM, the contents of the EPROM are preferred.

※3. Mark specification

Mark specification must be submitted using the correct form for the package being ordered. Fill out the appropriate mark specification form (64P4B for M38112M4-XXXSP, 64P6N for M38112M4-XXXFP) and attach it to the mask ROM confirmation form.

※4. Delivery standard

Choose the format of the specifications for the product to be delivered.

(1) Specifications for each ROM

☐ ROM code list unnecessary (standard).

☐ ROM code list necessary.

Note that each format has the same scope of guarantee. Therefore, the standard format is recommended.

GZZ—SH03—49A〈03A0〉

Mask ROM number	

SERIES MELPS 740 MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M38112M4-XXXSP/FP
MITSUBISHI ELECTRIC

※5. Usage conditions

Please answer the following questions about usage for use in our product inspection :

(1) How will you use the X_{IN}-X_{OUT} oscillator ?

☐ Ceramic resonator ☐ Quartz crystal

☐ External clock input ☐ Other (   )

At what frequency ? $f(X_{IN})=$ ☐ MHz

(2) How will you use the X_{CIN}-X_{COUT} oscillator ?

☐ Ceramic resonator ☐ Quartz crystal

☐ External clock input ☐ Other (   )

At what frequency ? $f(X_{CIN})=$ ☐ kHz

※6. Comments

GZZ–SH03–74A<09A1>

SERIES MELPS 740 MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M38173M6-XXXFP
MITSUBISHI ELECTRIC

Mask ROM number	

Receipt	Date :	
	Section head signature	Supervisor signature

Note : Please fill in all items marked※.

※	Customer	Company name	TEL ( )	Issuance signature	Submitted by	Supervisor
		Date issued	Date :			

※1. Confirmation

Specify the name of the product being ordered and the type of EPROMs submitted.

Three EPROMs are required for each pattern.

If at least two of the three sets of EPROMs submitted contain identical data, we will produce masks based on this data. We shall assume the responsibility for errors only if the mask ROM data on the products we produce differs from this data. Thus, extreme care must be taken to verify the data in the submitted EPROMs.

Checksum code for entire EPROM ☐☐☐☐ (hexadecimal notation)

EPROM type (indicate the type used)

☐ 27256		☐ 27512	
EPROM address		EPROM address	
0000_{16} $000F_{16}$	Product name ASCII code 'M38173M6–'	0000_{16}	Product name ASCII code 'M38173M6–'
0010_{16}	RESMOD option	0010_{16}	RESMOD option
0011_{16} $207F_{16}$	▨	0011_{16} $A07F_{16}$	▨
2080_{16} $7FFD_{16}$	data ROM 24446 bytes	$A080_{16}$ $FFFD_{16}$	data ROM 24446 bytes
$7FFE_{16}$ $7FFF_{16}$	▨	$FFFE_{16}$ $FFFF_{16}$	▨

In the address space of the microcomputer, the internal ROM area is from address $A080_{16}$ to $FFFD_{16}$. The reset vector is stored in addresses $FFFC_{16}$ and $FFFD_{16}$.

(1) Set the data in the unused area (the shaded area of the diagram) to "FF_{16}".

(2) The ASCII codes of the product name "M38173M6—" must be entered in addresses 0000_{16} to 0008_{16}. The ASCII codes and addresses are listed to the right in hexadecimal notation.

Address		Address	
0000_{16}	'M' = $4D_{16}$	0008_{16}	'—' = $2D_{16}$
0001_{16}	'3' = 33_{16}	0009_{16}	FF_{16}
0002_{16}	'8' = 38_{16}	$000A_{16}$	FF_{16}
0003_{16}	'1' = 31_{16}	$000B_{16}$	FF_{16}
0004_{16}	'7' = 37_{16}	$000C_{16}$	FF_{16}
0005_{16}	'3' = 33_{16}	$000D_{16}$	FF_{16}
0006_{16}	'M' = $4D_{16}$	$000E_{16}$	FF_{16}
0007_{16}	'6' = 36_{16}	$000F_{16}$	FF_{16}

GZZ–SH03–74A〈09A1〉

Mask ROM number	

SERIES MELPS 740 MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M38173M6-XXXFP
MITSUBISHI ELECTRIC

We recommend the use of the following pseudo-command to set the start address of the assembler source program.

EPROM type	27256	27512
The pseudo-command	＊=△$8000 .BYTE△ 'M38173M6−'	＊=△$0000 .BYTE△ 'M38173M6−'

Note : If the name of the product written to the EPROMs does not match the name of the mask confirmation form, the ROM will not be processed.

※2. Option specification (write the option data also to the specified address of the EPROM)

Reset mode switching option

☐ Normal operation start mode ··············· 01_{16}

☐ Low-speed operation start mode ··············· 00_{16}

Address 0010_{16}

We recommend the use of the following pseudo-command to set the start address of the assembler source program.

EPROM type	27256	27512
Reset mode option	＊=△$8010 .BYTE△ $XX	＊=△$0010 .BYTE△ $XX

Note : If the name of the product written to the EPROMs does not match the name of the mask confirmation form, the ROM will not be processed. Write the data correctly. As for the option, if the contents of the confirmation and conflict with those of the EPROM, the contents of the EPROM are preferred.

※3. Mark specification
Mark specification must be submitted using the correct form for the package being ordered. Fill out the appropriate mark specification form (80P6N for M38173M6-XXXFP) and attach it to the mask ROM confirmation form.

※4. Delivery standard
Choose the format of the specifications for the product to be delivered.
(1) Specifications for each ROM

☐ ROM code list unnecessary (standard)

☐ ROM code list necessary.

Note that each format has the same scope of guarantee. Therefore, the standard format is recommended.

GZZ–SH03–74A‹09A1›

Mask ROM number	

SERIES MELPS 740 MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M38173M6-XXXFP
MITSUBISHI ELECTRIC

※5. Usage conditions

Please answer the following questions about usage for use in our product inspection :

(1) How will you use the X_{IN}-X_{OUT} oscillator ?

☐ Ceramic resonator ☐ Quartz crystal

☐ External clock input ☐ Other (   )

At what frequency ? $f(X_{IN})=$ ☐ MHz

(2) How will you use the X_{CIN}-X_{COUT} oscillator ?

☐ Ceramic resonator ☐ Quartz crystal

☐ External clock input ☐ Other (   )

At what frequency ? $f(X_{CIN})=$ ☐ kHz

※6. Comments

GZZ—SH04—03A〈0YA0〉

SERIES MELPS 740 MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M38174M8-XXXFP
MITSUBISHI ELECTRIC

Mask ROM number	

Receipt	Date :	
	Section head signature	Supervisor signature

Note : Please fill in all items marked※.

※	Customer	Company name	TEL (　　　)	Issuance signature	Submitted by	Supervisor
		Date issued	Date :			

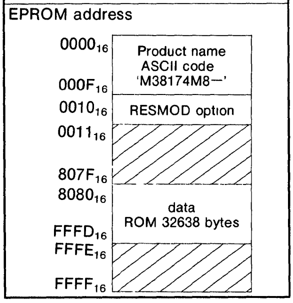
※ 1 . Confirmation

Specify the name of the product being ordered and the type of EPROMs submitted.
Three EPROMs are required for each pattern.
If at least two of the three sets of EPROMs submitted contain identical data, we will produce masks based on this data. We shall assume the responsibility for errors only if the mask ROM data on the products we produce differs from this data. Thus, extreme care must be taken to verify the data in the submitted EPROMs.

Checksum code for entire EPROM					(hexadecimal notation)

EPROM type (indicate the type used)

☐ 27512



In the address space of the microcomputer, the internal ROM area is from address 8080_{16} to $FFFD_{16}$. The reset vector is stored in addresses $FFFC_{16}$ and $FFFD_{16}$.

(1) Set the data in the unused area (the shaded area of the diagram) to "FF_{16}".

(2) The ASCII codes of the product name "M38174M8—" must be entered in addresses 0000_{16} to 0008_{16}. The ASCII codes and addresses are listed to the right in hexadecimal notation.

Address		Address	
0000_{16}	'M' = 4 D_{16}	0008_{16}	'—' = 2 D_{16}
0001_{16}	'3' = 3 3_{16}	0009_{16}	F F_{16}
0002_{16}	'8' = 3 8_{16}	$000A_{16}$	F F_{16}
0003_{16}	'1' = 3 1_{16}	$000B_{16}$	F F_{16}
0004_{16}	'7' = 3 7_{16}	$000C_{16}$	F F_{16}
0005_{16}	'4' = 3 4_{16}	$000D_{16}$	F F_{16}
0006_{16}	'M' = 4 D_{16}	$000E_{16}$	F F_{16}
0007_{16}	'8' = 3 8_{16}	$000F_{16}$	F F_{16}

GZZ–SH04–03A＜0YA0＞

Mask ROM number	

SERIES MELPS 740 MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M38174M8-XXXFP
MITSUBISHI ELECTRIC

We recommend the use of the following pseudo-command to set the start address of the assembler source program.

EPROM type	27256	27512
The pseudo-command	＊=△$8000 .BYTE△ 'M38174M8–'	＊=△$0000 .BYTE△ 'M38174M8–'

Note : If the name of the product written to the EPROMs does not match the name of the mask confirmation form, the ROM will not be processed.

※2. Option specification (write the option data also to the specified address of the EPROM)

Reset mode switching option

☐ Normal operation start mode ···············	01_{16}	Address 0010_{16}
☐ Low-speed operation start mode ···············	00_{16}	

We recommend the use of the following pseudo-command to set the start address of the assembler source program.

EPROM type	27256	27512
Reset mode option	＊=△$8010 .BYTE△ $XX	＊=△$0010 .BYTE△ $XX

Note : If the name of the product written to the EPROMs does not match the name of the mask confirmation form, the ROM will not be processed. Write the data correctly. As for the option, if the contents of the confirmation and conflict with those of the EPROM, the contents of the EPROM are preferred.

※3. Mark specification
Mark specification must be submitted using the correct form for the package being ordered. Fill out the appropriate mark specification form (80P6N for M38174M8-XXXFP) and attach it to the mask ROM confirmation form.

※4. Delivery standard
Choose the format of the specifications for the product to be delivered.
(1) Specifications for each ROM

☐ ROM code list unnecessary (standard).

☐ ROM code list necessary.

Note that each format has the same scope of guarantee. Therefore, the standard format is recommended.

GZZ–SH04–03A〈 0YA0 〉

Mask ROM number	

SERIES MELPS 740 MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M38174M8-XXXFP
MITSUBISHI ELECTRIC

※5. Usage conditions

Please answer the following questions about usage for use in our product inspection :

(1) How will you use the X_{IN}-X_{OUT} oscillator ?

☐ Ceramic resonator ☐ Quartz crystal

☐ External clock input ☐ Other (   )

At what frequency ? $f(X_{IN})=$ ☐ MHz

(2) How will you use the X_{CIN}-X_{COUT} oscillator ?

☐ Ceramic resonator ☐ Quartz crystal

☐ External clock input ☐ Other (   )

At what frequency ? $f(X_{CIN})=$ ☐ kHz

※6. Comments

MARK SPECIFICATION FORM

MARK SPECIFICATION FORM

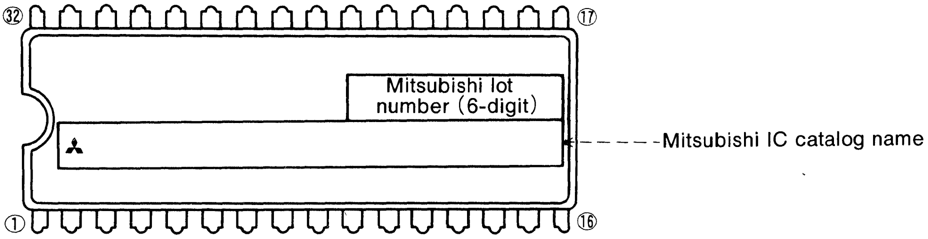
The mark specification form varies depending on the package type. Fill out the mark specification form for the package being ordered, and submit the form with the mask ROM confirmation form.

32P4B (32-PIN SHRINK DIP) MARK SPECIFICATION FORM

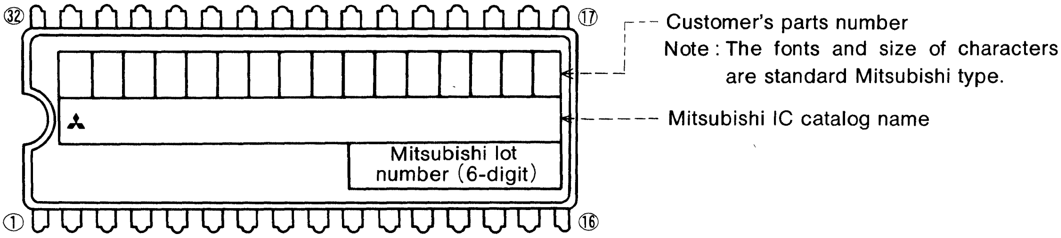
Mitsubishi IC catalog name

Please choose one of the marking types below (A, B, C), and enter the Mitsubishi IC catalog name and the special mark (if needed).

A. Standard Mitsubishi Mark



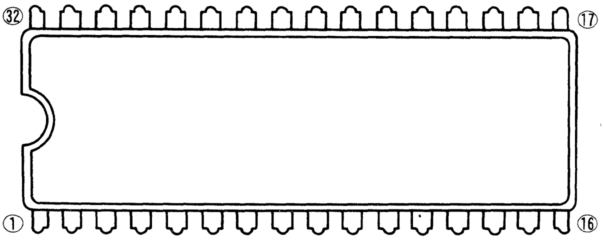
B. Customer's Parts Number + Mitsubishi Catalog Name



Note1 : The mark field should be written right aligned.
2 : The fonts and size of characters are standard Mitsubishi type.
3 : Customer's parts number can be up to 16 characters :
Only 0~9, A~Z, +, −, ⁄, (,), &, ©, . (period), and , (comma) are usable.
4 : If the Mitsubishi logo ⅄ is not required, check the box on the right.

⅄Mitsubishi logo is not required ☐

C. Special Mark Required



Note1 : If the special mark is to be printed, indicate the desired layout of the mark in the upper figure. The layout will be duplicated as close as possible. Mitsubishi lot number (6-digit) and mask ROM number (3-digit) are always marked.
2 : If the customer's trade mark logo must be used in the special mark, check the box below. Please submit a clean original of the logo.
For the new special character fonts a clean font original (ideally logo drawing) must be submitted.

Special logo required ☐

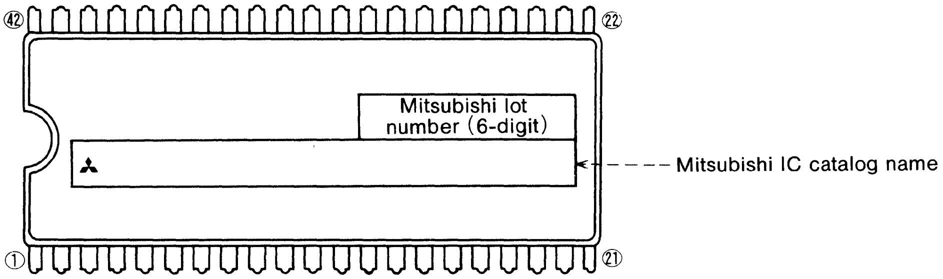
The standard Mitsubishi font is used for all characters except for a logo.

42P4B (42-PIN SHRINK DIP) MARK SPECIFICATION FORM

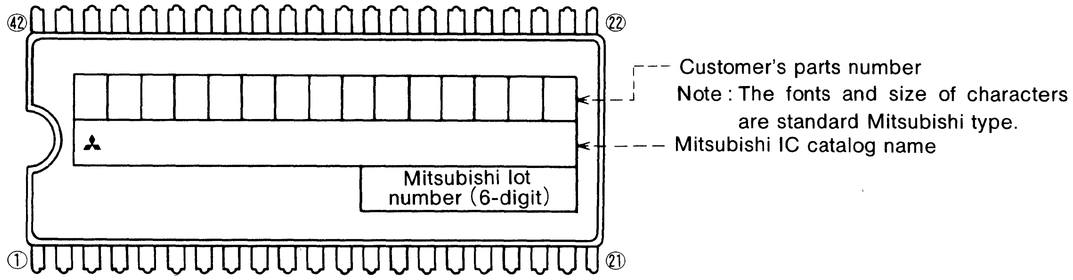
Mitsubishi IC catalog name

Please choose one of the marking types below (A, B, C), and enter the Mitsubishi IC catalog name and the special mark (if needed).

A. Standard Mitsubishi Mark



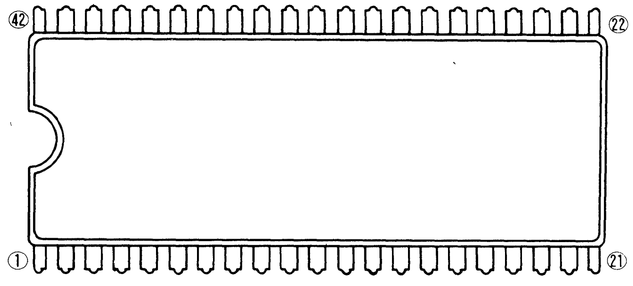
B. Customer's Parts Number + Mitsubishi Catalog Name



Note1 : The mark field should be written right aligned.
2 : The fonts and size of characters are standard Mitsubishi type.
3 : Customer's parts number can be up to 15 characters :
Only 0~9, A~Z, +, −, ／, (,), &, ©, . (period), and , (comma) are usable.
4 : If the Mitsubishi logo ⅄ is not required, check the box on the right.

⅄Mitsubishi logo is not required ☐

C. Special Mark Required



Note1 : If the special mark is to be printed, indicate the desired layout of the mark in the upper figure. The layout will be duplicated as close as possible. Mitsubishi lot number (6-digit) and mask ROM number (3-digit) are always marked.
2 : If the customer's trade mark logo must be used in the special mark, check the box below. Please submit a clean original of the logo.
For the new special character fonts a clean font original (ideally logo drawing) must be submitted.
The standard Mitsubishi font is used for all characters except for a logo.

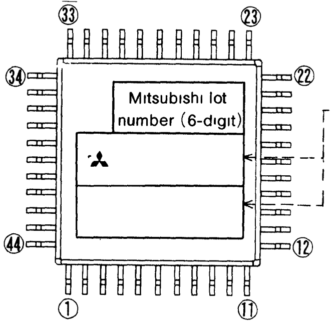
Special logo required ☐

44P6N (44-PIN QFP) MARK SPECIFICATION FORM

Mitsubishi IC catalog name ☐

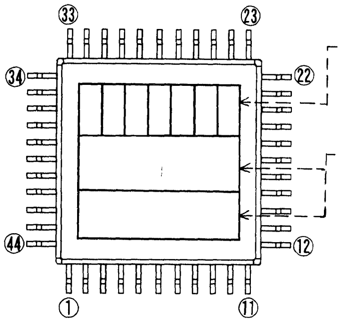
Please choose one of the marking types below (A, B, C), and enter the Mitsubishi IC catalog name and the special mark (if needed).

A. Standard Mitsubishi Mark



Mitsubishi IC catalog name

B. Customer's Parts Number + Mitsubishi Catalog Name



Customer's parts number
Note : The fonts and size of characters are standard Mitsubishi type.

Mitsubishi IC catalog name and Mitsubishi lot number

Note4 : If the Mitsubishi logo is not required, check the box below.

Mitsubishi logo is not required

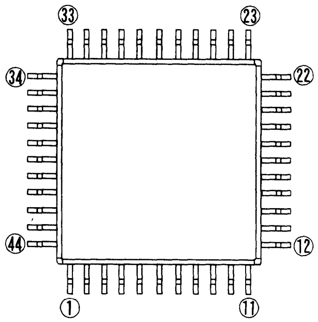
☐

Note1 : The mark field should be written right aligned.

2 : The fonts and size of characters are standard Mitsubishi type.

3 : Customer's parts number can be up to 7 characters :
Only 0~9, A~Z, +, −, ⁄, (,), &, ©, . (period), and , (comma) are usable.

C. Special Mark Required



Note1 : If the special mark is to be printed, indicate the desired layout of the mark in the left figure. The layout will be duplicated as close as possible. Mitsubishi lot number (6-digit) and mask ROM number (3-digit) are always marked.

2 : If the customer's trade mark logo must be used in the special mark, check the box below. Please submit a clean original of the logo.
For the new special character fonts a clean font original (ideally logo drawing) must be submitted.

Special logo required

☐

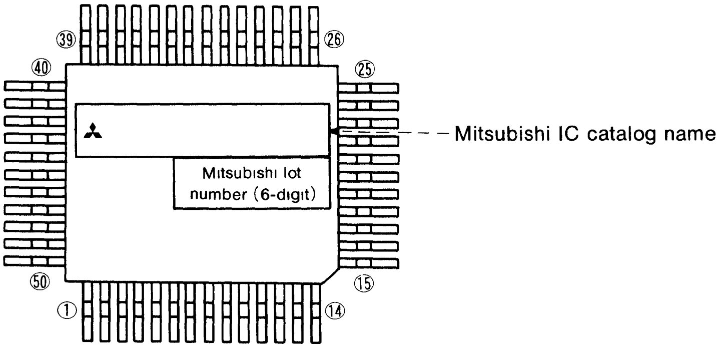
The standard Mitsubishi font is used for all characters except for a logo.

50P6 (50-PIN QFP) MARK SPECIFICATION FORM

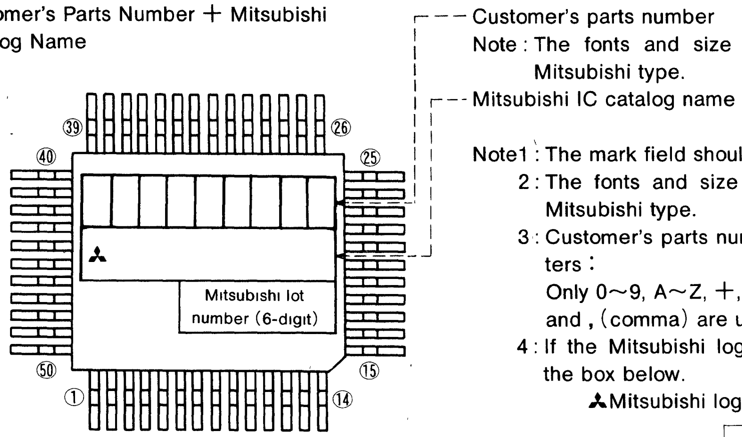
Mitsubishi IC catalog name ☐

Please choose one of the marking types below (A, B, C), and enter the Mitsubishi IC catalog name and the special mark (if needed).

A. Standard Mitsubishi Mark



B. Customer's Parts Number + Mitsubishi Catalog Name

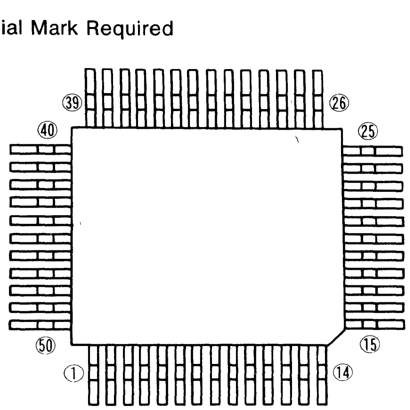


Note : The fonts and size of characters are standard Mitsubishi type.

Note1 : The mark field should be written right aligned.
2 : The fonts and size of characters are standard Mitsubishi type.
3 : Customer's parts number can be up to 9 characters :
Only 0~9, A~Z, +, −, /, (,), &, ©, . (period), and , (comma) are usable.
4 : If the Mitsubishi logo is not required, check the box below.
Mitsubishi logo is not required

☐

C. Special Mark Required



Note1 : If the special mark is to be printed, indicate the desired layout of the mark in the left figure. The layout will be duplicated as close as possible. Mitsubishi lot number (6-digit) and mask ROM number (3-digit) are always marked.
2 : If the customer's trade mark logo must be used in the special mark, check the box below. Please submit a clean original of the logo.
For the new special character fonts a clean font original (ideally logo drawing) must be submitted.
Special logo required

☐

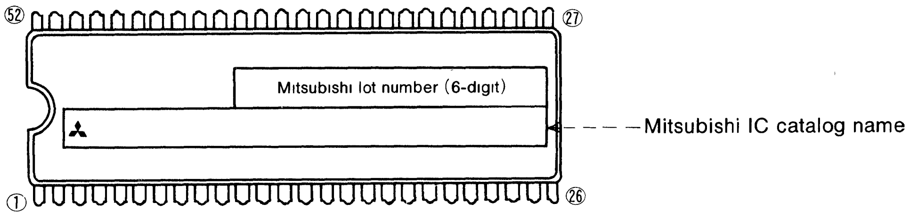
The standard Mitsubishi font is used for all characters except for a logo.

52P4B (52-PIN SHRINK DIP) MARK SPECIFICATION FORM

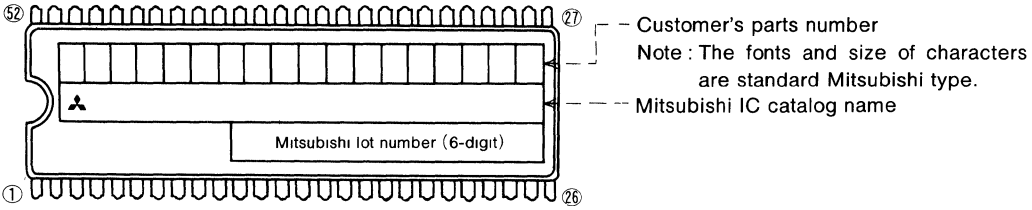
Mitsubishi IC catalog name ☐

Please choose one of the marking types below (A, B, C), and enter the Mitsubishi IC catalog name and the special mark (if needed).

A. Standard Mitsubishi Mark



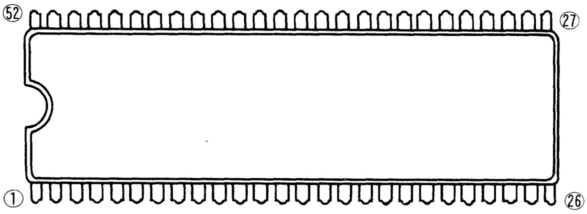
B. Customer's Parts Number + Mitsubishi Catalog Name



Note1 : The mark field should be written right aligned.
2 : The fonts and size of characters are standard Mitsubishi type.
3 : Customer's parts number can be up to 18 characters :
Only 0~9, A~Z, +, −, ⁄, (,), &, ©, . (period), and , (comma) are usable.
4 : If the Mitsubishi logo is not required, check the box on the right.

Mitsubishi logo is not required ☐

C. Special Mark Required



Note1 : If the special mark is to be printed, indicate the desired layout of the mark in the upper figure The layout will be duplicated as close as possible. Mitsubishi lot number (6-digit) and mask ROM number (3-digit) are always marked.
2 : If the customer's trade mark logo must be used in the special mark, check the box below. Please submit a clean original of the logo.
For the new special character fonts a clean font original (ideally logo drawing) must be submitted.

Special logo required ☐

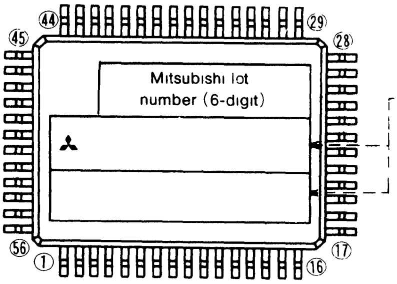
The standard Mitsubishi font is used for all characters except for a logo.

56P6N (56-PIN QFP) MARK SPECIFICATION FORM

Mitsubishi IC catalog name ☐

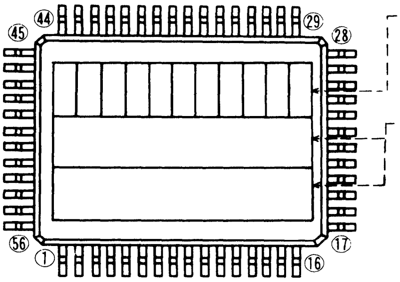
Please choose one of the marking types below (A, B, C), and enter the Mitsubishi IC catalog name and the special mark (if needed).

A. Standard Mitsubishi Mark



Mitsubishi IC catalog name

B. Customer's Parts Number + Mitsubishi Catalog Name



Customer's parts number
Note : The fonts and size of characters are standard Mitsubishi type.

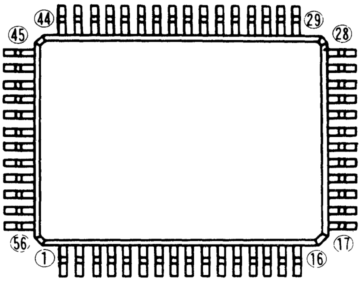
Mitsubishi IC catalog name and Mitsubishi lot number

Note1 : The mark field should be written right aligned.
2 : The fonts and size of characters are standard Mitsubishi type.
3 : Customer's parts number can be up to 11 characters :
Only 0~9, A~Z, +, $\dot{-}$, /, (,), &, ©, . (period), and , (comma) are usable.

Note4 . If the Mitsubishi logo ⅄ is not required, check the box below.
⅄ Mitsubishi logo is not required
☐

5 : Arrangement of Mitsubishi IC catalog name and Mitsubishi lot number is dependent on number of Mitsubishi IC catalog name and that Mitsubishi logo ⅄ is required or not.

C. Special Mark Required



Note1 : If the special mark is to be printed, indicate the desired layout of the mark in the left figure. The layout will be duplicated as close as possible. Mitsubishi lot number (6-digit) and mask ROM number (3-digit) are always marked.
2 : If the customer's trade mark logo must be used in the special mark, check the box below. Please submit a clean original of the logo.
For the new special character fonts a clean font original (ideally logo drawing) must be submitted.
Special logo required
☐

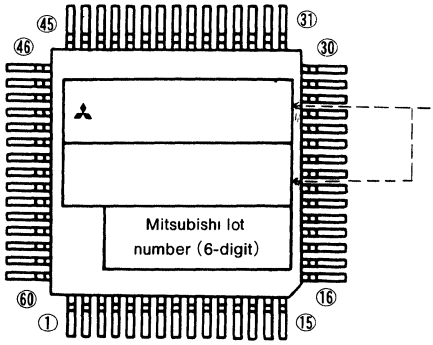
The standard Mitsubishi font is used for all characters except for a logo.

60P6 (60-PIN QFP) MARK SPECIFICATION FORM

Mitsubishi IC catalog name ☐

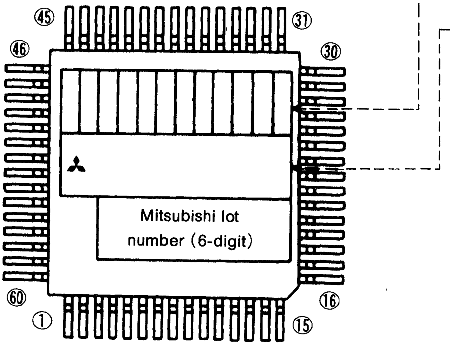
Please choose one of the marking types below (A, B, C), and enter the Mitsubishi IC catalog name and the special mark (if needed).

A. Standard Mitsubishi Mark



---Mitsubishi IC catalog name

B. Customer's Parts Number + Mitsubishi Catalog Name



---Customer's Parts Number

Note : The fonts and size of characters are standard Mitsubishi type.

--Mitsubishi IC catalog name

Note1 : The mark field should be written right aligned.

2 : The fonts and size of characters are standard Mitsubishi type.

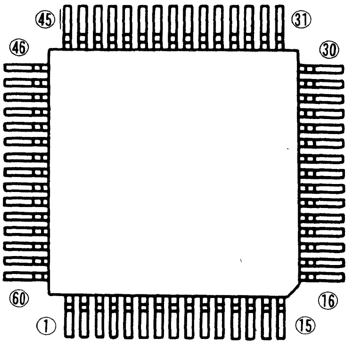
3 : Customer's parts number can be up to 12 characters :
Only 0~9, A~Z, +, −, ∕, (,), &, ©, . (period), and , (comma) are usable.

4 : If the Mitsubishi logo ⅄ is not required, check the box below.

⅄ Mitsubishi logo is not required

☐

C. Special Mark Required



Note1 : If the Special Mark is to be printed, indicate the desired layout of the mark in the left figure. The layout will be duplicated as close as possible. Mitsubishi lot number (6-digit) and mask ROM number (3-digit) are always marked.

2 : If the customer's trade mark logo must be used in the special mark, check the box below. Please submit a clean original of the logo.
For the new special character fonts a clean font original (ideally logo drawing) must be submitted.

Special logo required

☐

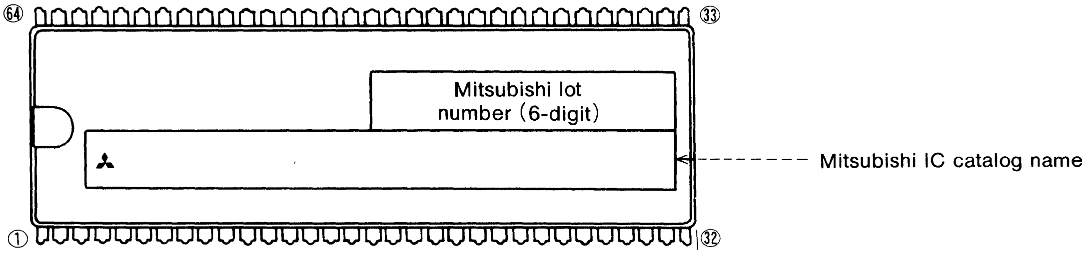
The standard Mitsubishi font is used for all characters except for a logo.

64P4B (64-PIN SHRINK DIP) MARK SPECIFICATION FORM

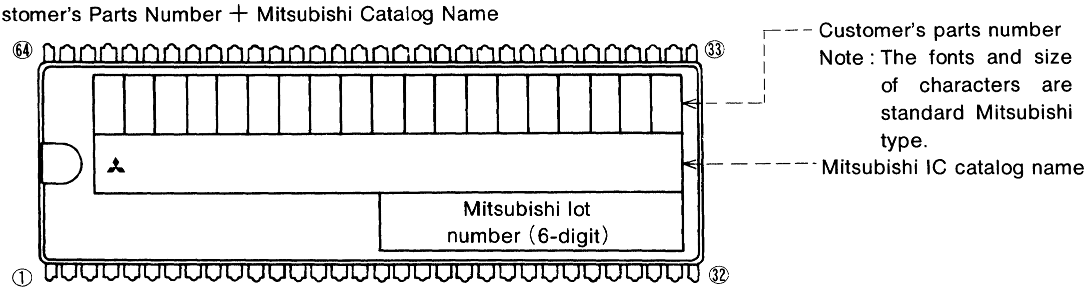
Mitsubishi IC catalog name ☐

Please choose one of the marking types below (A, B, C), and enter the Mitsubishi IC catalog name and the special mark (if needed).

A. Standard Mitsubishi Mark



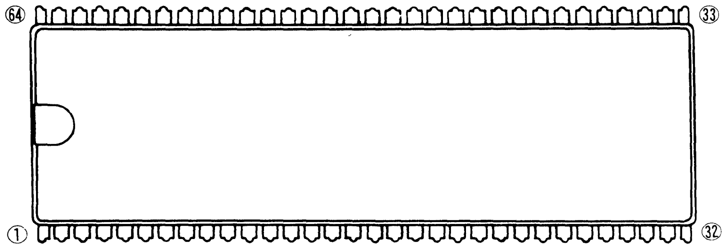
B. Customer's Parts Number + Mitsubishi Catalog Name



Note1 : The mark field should be written right aligned.
2 : The fonts and size of characters are standard Mitsubishi type.
3 : Customer's parts number can be up to 19 characters :
Only 0~9, A~Z, +, −, ⁄, (,), &, ©, . (period), and , (comma) are usable.
4 : If the Mitsubishi logo ⅄ is not required, check the box on the right.

⅄ Mitsubishi logo is not required
☐

C. Special Mark Required



Note1 : If the special mark is to be printed, indicate the desired layout of the mark in the upper figure The layout will be duplicated as close as possible. Mitsubishi lot number (6-digit) and mask ROM number (3-digit) are always marked.
2 : If the customer's trade mark logo must be used in the special mark, check the box below. Please submit a clean original of the logo.
For the new special character fonts a clean font original (ideally logo drawing) must be submitted.

Special logo required

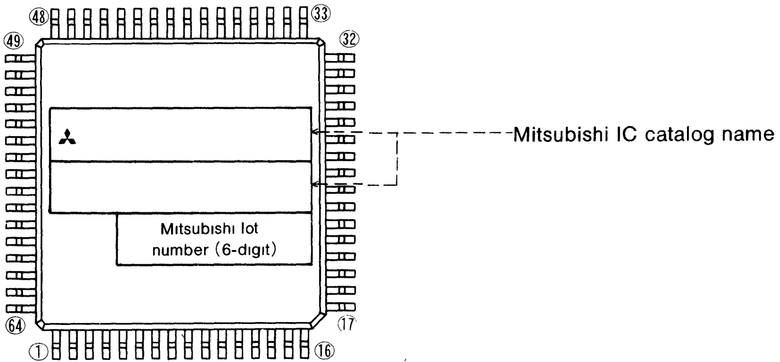
The standard Mitsubishi font is used for all characters except for a logo. ☐

64P6N (64-PIN QFP) MARK SPECIFICATION FORM

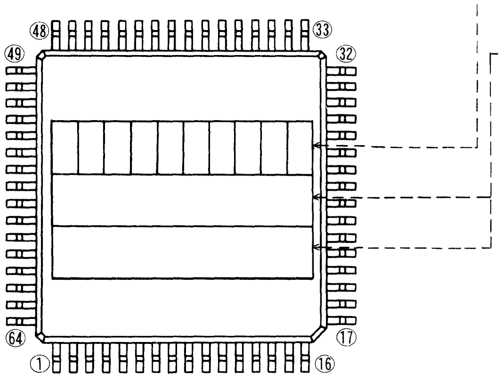
Mitsubishi IC catalog name ☐

Please choose one of the marking types below (A, B, C), and enter the Mitsubishi IC catalog name and the special mark (if needed).

A. Standard Mitsubishi Mark



B. Customer's Parts Number + Mitsubishi Catalog Name



Customer's parts number

Note · The fonts and size of characters are standard Mitsubishi type.

Mitsubishi IC catalog name

Note3 : Customer's parts number can be up to 10 characters :
Only 0~9, A~Z, +, −, ⁄, (,), &, ©, . (period), and , (comma) are usable.

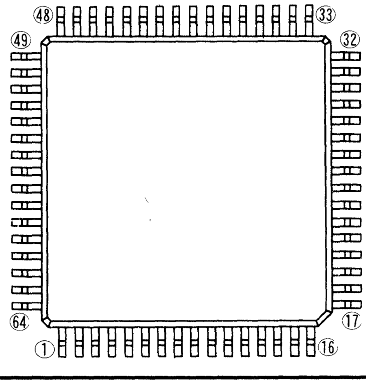
4 : If the Mitsubishi logo is not required, check the box below.
Mitsubishi logo is not required
☐

5 : Arrangement of Mitsubishi IC catalog name and Mitsubishi lot number is dependent on number of Mitsubishi IC catalog name and that Mitsubishi logo is required or not.

Note1 : The mark field should be written right aligned.

2 : The fonts and size of characters are standard Mitsubishi type. (The character size became smaller than A (standard Mitsubishi mark) type)

C. Special Mark Required



Note1 : If the special mark is to be printed, indicate the desired layout of the mark in the left figure. The layout will be duplicated as close as possible. Mitsubishi lot number (6-digit) and mask ROM number (3-digit) are always marked

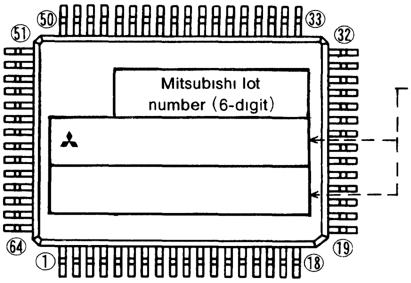
2 : If the customer's trade mark logo must be used in the special mark, check the box below. Please submit a clean original of the logo.
For the new special character fonts a clean font original (ideally logo drawing) must be submitted.
Special logo required
☐
The standard Mitsubishi font is used for all characters except for a logo.

64P6S (64-PIN QFP) MARK SPECIFICATION FORM

Mitsubishi IC catalog name ☐

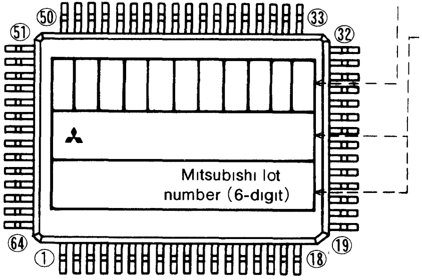
Please choose one of the marking types below (A, B, C), and enter the Mitsubishi IC catalog name and the special mark (if needed).

A. Standard Mitsubishi Mark



Mitsubishi IC catalog name

B. Customer's Parts Number + Mitsubishi Catalog Name



Customer's Parts Number

Note : The fonts and size of characters are standard Mitsubishi type.

Mitsubishi IC catalog name and Mitsubishi lot number

Note3 : Customer's parts number can be up to 11 characters :
Only 0~9, A~Z, +, −, ⁄, (,), &, ©, . (period), and , (comma) are usable.

4 : If the Mitsubishi logo is not required, check the box below.

Mitsubishi logo is not required

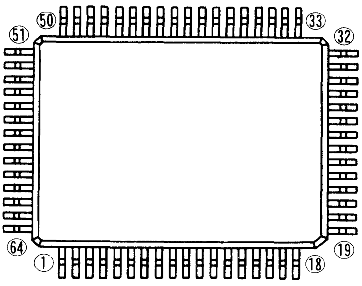
☐

5 : Arrangement of Mitsubishi IC catalog name and Mitsubishi lot number is dependent on number of Mitsubishi IC catalog name and that Mitsubishi logo is required or not.

Note1 : The mark field should be written right aligned.

2 : The fonts and size of characters are standard Mitsubishi type. (The character size become smaller than A (standard Mitsubishi mark) type)

C. Special Mark Required



Note1 : If the special mark is to be printed, indicate the desired layout of the mark in the left figure. The layout will be duplicated as close as possible. Mitsubishi lot number (6-digit) and mask ROM number (3-digit) are always marked.

2 : If the customer's trade mark logo must be used in the special mark, check the box below. Please submit a clean original of the logo.
For the new special character fonts a clean font original (ideally logo drawing) must be submitted.

Special logo required

☐

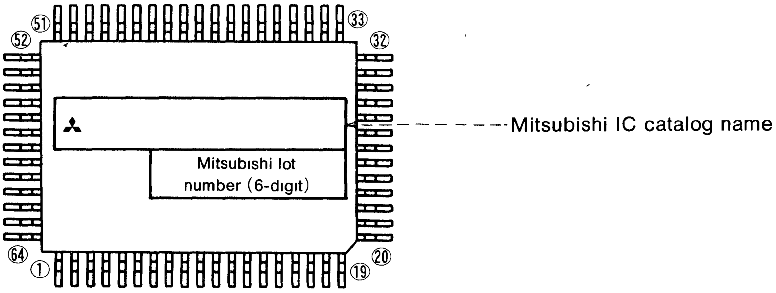
The standard Mitsubishi font is used for all characters except for a logo.

64P6W (64-PIN QFP) MARK SPECIFICATION FORM

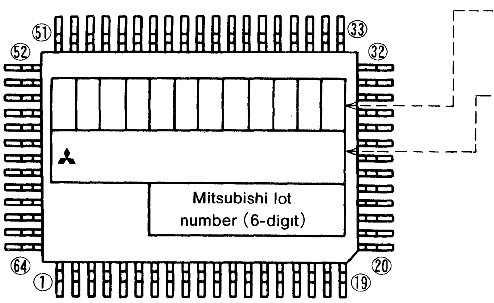
Mitsubishi IC catalog name ☐

Please choose one of the marking types below (A, B, C), and enter the Mitsubishi IC catalog name and the special mark (if needed).

A. Standard Mitsubishi Mark



B. Customer's Parts Number + Mitsubishi Catalog Name



Customer's parts number
Note : The fonts and size of characters are standard Mitsubishi type.

Mitsubishi IC catalog name

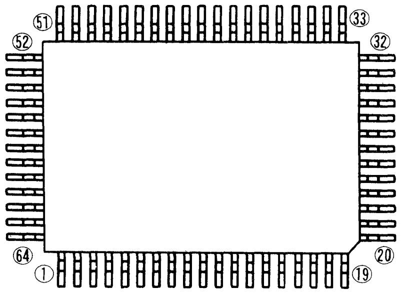
Note3 : Customer's parts number can be up to 12 characters :
Only 0~9, A~Z, +, −, ⁄, (,), &, ©, . (period), and , (comma) are usable.
4 : If the Mitsubishi logo is not required, check the box below.

Mitsubishi logo is not required

☐

Note1 : The mark field should be written right aligned.
2 : The fonts and size of characters are standard Mitsubishi type.

C. Special Mark Required



Note1 : If the special mark is to be printed, indicate the desired layout of the mark in the left figure. The layout will be duplicated as close as possible. Mitsubishi lot number (6-digit) and mask ROM number (3-digit) are always marked.
2 : If the customer's trade mark logo must be used in the special mark, check the box below. Please submit a clean original of the logo.
For the new special character fonts a clean font original (ideally logo drawing) must be submitted.

Special logo required

☐

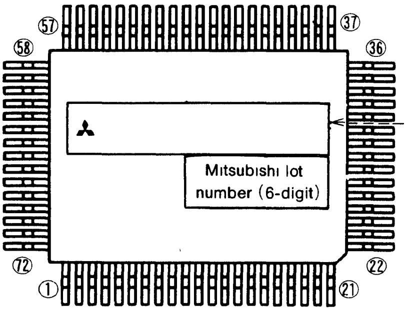
The standard Mitsubishi font is used for all characters except for a logo.

72P6 (72-PIN QFP) MARK SPECIFICATION FORM

Mitsubishi IC catalog name ☐

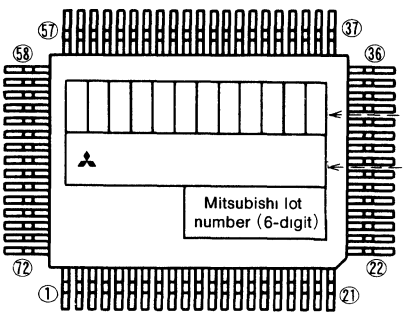
Please choose one of the marking types below (A, B, C), and enter the Mitsubishi IC catalog name and the special mark (if needed).

A. Standard Mitsubishi Mark



-----Mitsubishi IC catalog name

B. Customer's Parts Number + Mitsubishi Catalog Name

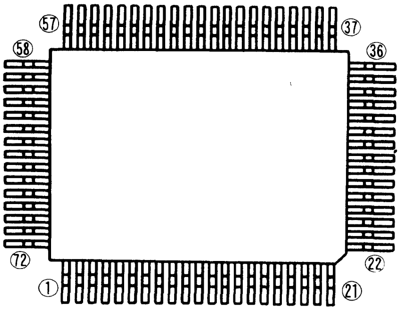


----- Customer's parts number
Note : The fonts and size of characters are standard Mitsubishi type.
---Mitsubishi IC catalog name

Note1 : The mark field should be written right aligned.
2 : The fonts and size of characters are standard Mitsubishi type.
3 : Customer's Parts Number can be up to 12 characters :
Only 0~9, A~Z, +, −, ／, (,), &, ©, . (period), and , (comma) are usable.
4 : If the Mitsubishi logo is not required, check the box below.
Mitsubishi logo is not required

☐

C. Special Mark Required



Note1 : If the special mark is to be printed, indicate the desired layout of the mark in the left figure. The layout will be duplicated as close as possible. Mitsubishi lot number (6-digit) and mask ROM number (3-digit) are always marked.
2 : If the customer's trade mark logo must be used in the special mark, check the box below. Please submit a clean original of the logo.
For the new special character fonts a clean font original (ideally logo drawing) must be submitted.
Special logo required

☐

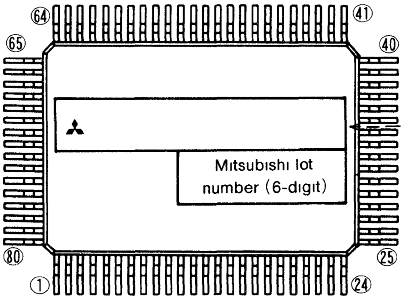
The standard Mitsubishi font is used for all characters except for a logo.

80P6 (80-PIN QFP) MARK SPECIFICATION FORM

Mitsubishi IC catalog name

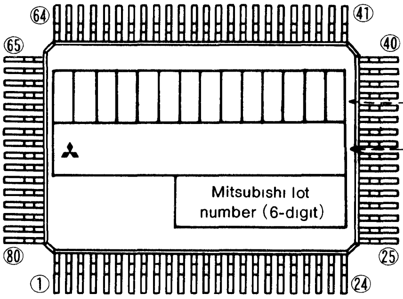
Please choose one of the marking types below (A, B, C), and enter the Mitsubishi IC catalog name and the special mark (if needed).

A. Standard Mitsubishi Mark



----Mitsubishi IC catalog name

B. Customer's Parts Number + Mitsubishi Catalog Name



---- Customer's parts number

Note : The fonts and size of characters are standard Mitsubishi type.

-- Mitsubishi IC catalog name

Note1 : The mark field should be written right aligned.

2 . The fonts and size of characters are standard Mitsubishi type.

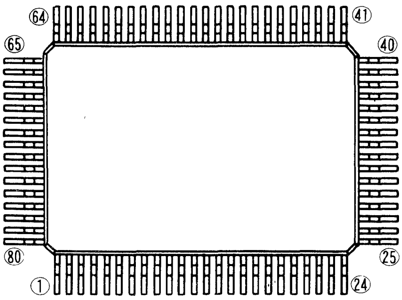
Note3 : Customer's parts number can be up to 14 characters :
Only 0~9, A~Z, +, −, ∕, (,), &, ©, . (period), and , (comma) are usable.

4 : If the Mitsubishi logo ⅄ is not required, check the box below.

⅄Mitsubishi logo is not required

☐

C. Special Mark Required



Note1 : If the special mark is to be printed, indicate the desired layout of the mark in the left figure. The layout will be duplicated as close as possible. Mitsubishi lot number (6-digit) and mask ROM number (3-digit) are always marked.

2 : If the customer's trade mark logo must be used in the special mark, check the box below. Please submit a clean original of the logo.
For the new special character fonts a clean font original (ideally logo drawing) must be submitted.

Special logo required

☐

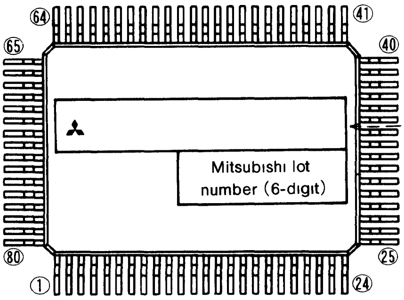
The standard Mitsubishi font is used for all characters except for a logo.

80P6N (80-PIN QFP) MARK SPECIFICATION FORM

Mitsubishi IC catalog name

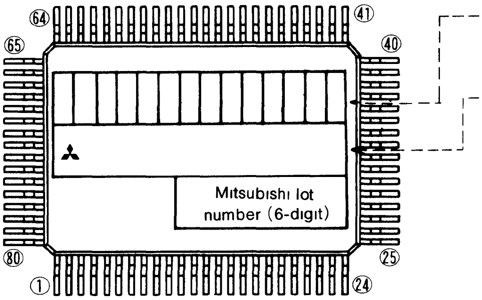
Please choose one of the marking types below (A, B, C), and enter the Mitsubishi IC catalog name and the special mark (if needed).

A. Standard Mitsubishi Mark



------Mitsubishi IC catalog name

B. Customer's Parts Number + Mitsubishi Catalog Name



----- Customer's parts number

Note : The fonts and size of characters are standard Mitsubishi type.

---Mitsubishi IC catalog name

Note1 : The mark field should be written right aligned

2 : The fonts and size of characters are standard Mitsubishi type.

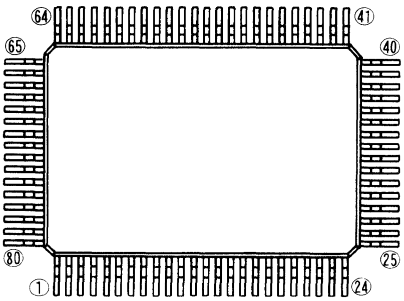
Note3 : Customer's parts number can be up to 14 characters :
Only 0~9, A~Z, +, −, ⁄, (,), &, ©, . (period), and , (comma) are usable.

4 : If the Mitsubishi logo ▲ is not required, check the box below.

▲Mitsubishi logo is not required

☐

C. Special Mark Required



Note1 : If the special mark is to be printed, indicate the desired layout of the mark in the left figure. The layout will be duplicated as close as possible. Mitsubishi lot number (6-digit) and mask ROM number (3-digit) are always marked.

2 : If the customer's trade mark logo must be used in the special mark, check the box below. Please submit a clean original of the logo.
For the new special character fonts a clean font original (ideally logo drawing) must be submitted.

Special logo required

☐

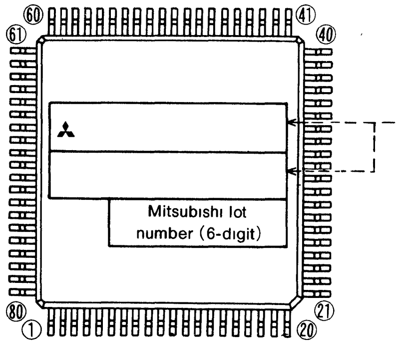
The standard Mitsubishi font is used for all characters except for a logo.

80P6S (80-PIN QFP) MARK SPECIFICATION FORM

Mitsubishi IC catalog name ☐

Please choose one of the marking types below (A, B, C), and enter the Mitsubishi IC catalog name and the special mark (if needed).

A. Standard Mitsubishi Mark



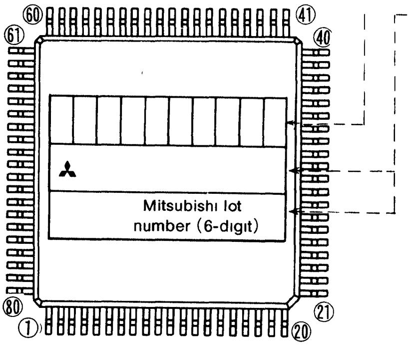
Mitsubishi IC catalog name

B. Customer's Parts Number + Mitsubishi Catalog Name

Customer's parts number

Note : The fonts and size of characters are standard Mitsubishi type.

Mitsubishi IC catalog name



Note1 : The mark field should be written right aligned.

2 : The fonts and size of characters are standard Mitsubishi type. (The character size become smaller than A (standard Mitsubishi mark) type)

Note3 : Customer's parts number can be up to 10 characters :
Only 0~9, A~Z, +, −, ／, (,), &, ©, . (period), and , (comma) are usable.

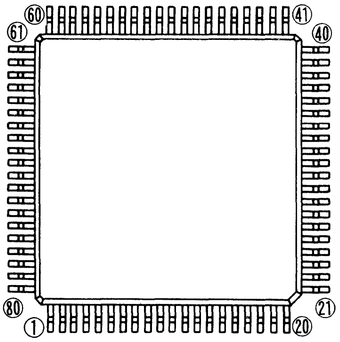
4 : If the Mitsubishi logo is not required, check the box below.

Mitsubishi logo is not required

☐

5 : Arrangement of Mitsubishi IC catalog name and Mitsubishi lot number is dependent on number of Mitsubishi IC catalog name and that Mitsubishi logo is required or not.

C. Special Mark Required



Note1 : If the special mark is to be printed, indicate the desired layout of the mark in the left figure. The layout will be duplicated as close as possible. Mitsubishi lot number (6-digit) and mask ROM number (3-digit) are always marked.

2 : If the customer's trade mark logo must be used in the special mark, check the box below. Please submit a clean original of the logo.
For the new special character fonts a clean font original (ideally logo drawing) must be submitted.

Special logo required ☐

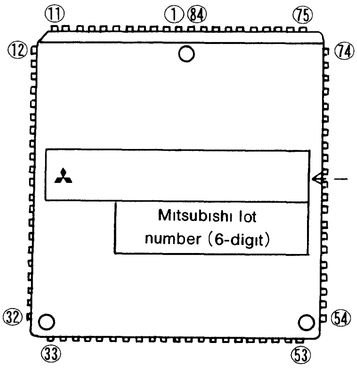
The standard Mitsubishi font is used for all characters except for a logo.

84P0 (84-PIN PLCC) MARK SPECIFICATION FORM

Mitsubishi IC catalog name ☐

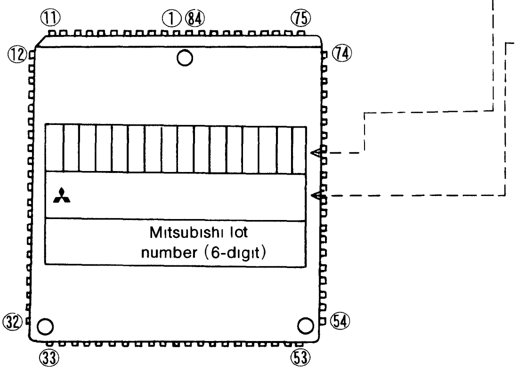
Please choose one of the marking types below (A, B, C), and enter the Mitsubishi IC catalog name and the special mark (if needed).

A. Standard Mitsubishi Mark



Mitsubishi IC catalog name

B. Customer's Parts Number + Mitsubishi Catalog Name



Customer's parts number

Note : The fonts and size of characters are standard Mitsubishi type.

Mitsubishi IC catalog name

Note1 : The mark field should be written right aligned.

2 : The fonts and size of characters are standard Mitsubishi type. (The character size become smaller than A (standard Mitsubishi mark) type)

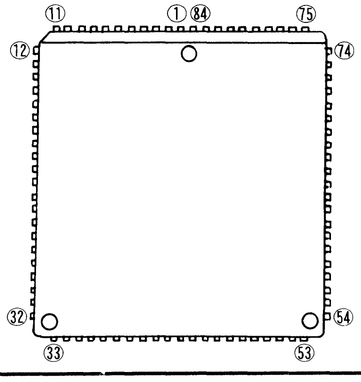
Note3 : Customer's parts number can be up to 16 characters :
Only 0~9, A~Z, +, −, ⁄, (,), &, ©, . (period), and , (comma) are usable.

4 : If the Mitsubishi logo ⅄ is not required, check the box below.
⅄ Mitsubishi logo is not required

☐

5 : Arrangement of Mitsubishi IC catalog name and Mitsubishi lot number is dependent on number of Mitsubishi IC catalog name and that Mitsubishi logo ⅄ is required or not.

C. Special Mark Required



Note1 : If the special mark is to be printed, indicate the desired layout of the mark in the left figure. The layout will be duplicated as close as possible. Mitsubishi lot number (6-digit) and mask ROM number (3-digit) are always marked.

2 : If the customer's trade mark logo must be used in the special mark, check the box below. Please submit a clean original of the logo.
For the new special character fonts a clean font original (ideally logo drawing) must be submitted.

Special logo required

☐

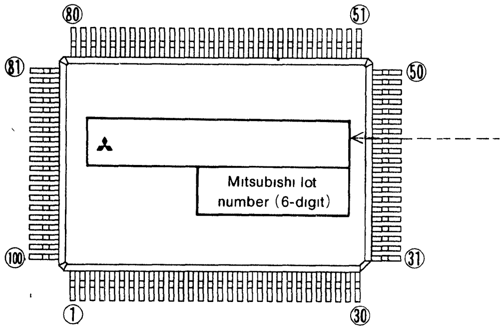
The standard Mitsubishi font is used for all characters except for a logo.

100P6S (100-PIN QFP) MARK SPECIFICATION FORM

Mitsubishi IC catalog name

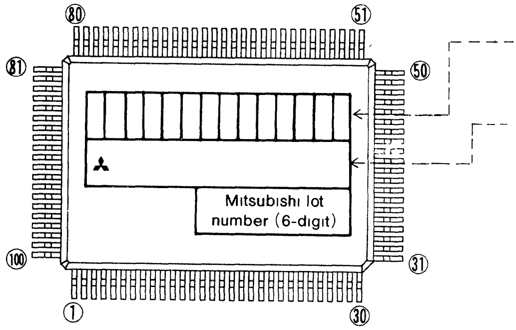
Please choose one of the marking types below (A, B, C), and enter the Mitsubishi IC catalog name and the special mark (if needed).

A. Standard Mitsubishi Mark



Mitsubishi IC catalog name

B. Customer's Parts Number + Mitsubishi Catalog Name



Customer's parts number
Note : The fonts and size of characters are standard Mitsubishi type.
Mitsubishi IC catalog name

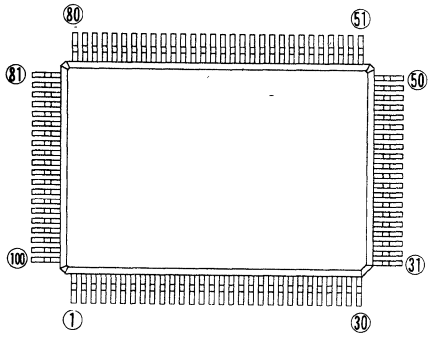
Note3 : Customer's parts number can be up to 14 characters :
Only 0~9, A~Z, +, −, ∕, (,), &, ©, . (period), and , (comma) are usable.
4 : If the Mitsubishi logo is not required, check the box below.

Mitsubishi logo is not required

☐

Note1 : The mark field should be written right aligned.
2 : The fonts and size of characters are standard Mitsubishi type.

C. Special Mark Required



Note1 : If the special mark is to be printed, indicate the desired layout of the mark in the left figure. The layout will be duplicated as close as possible. Mitsubishi lot number (6-digit) and mask ROM number (3-digit) are always marked.
2 : If the customer's trade mark logo must be used in the special mark, check the box below. Please submit a clean original of the logo.
For the new special character fonts a clean font original (ideally logo drawing) must be submitted.

Special logo required

☐

The standard Mitsubishi font is used for all characters except for a logo.

CONTACT ADDRESSES FOR FURTHER INFORMATION

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