MITSUBISHI SEMICONDUCTORS 1996

MEMORIES
SRAM

DATA BOOK

QCI / CEI

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Sunnyvale, CA 94086

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GUIDANCE 1

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■ LOW POWER DISSIPATION STATIC RAMs [5V Version]

Memory capacity	Configuration (Word × Bit)	Circuit function	Access time Max (ns)	Type name	Package outline	Page
256K	32K × 8	with ($\overline{S_1}$, S_2)	70	M5M5255BP-70	28P4	2-3
				M5M5255BFP-70	28P2W-C	
				M5M5255BKP-70	28P4Y	
			85	M5M5255BP-85	28P4	
				M5M5255BFP-85	28P2W-C	
				M5M5255BKP-85	28P4Y	
			100	M5M5255BP-10	28P4	
				M5M5255BFP-10	28P2W-C	
				M5M5255BKP-10	28P4Y	
			120	M5M5255BP-12	28P4	
				M5M5255BFP-12	28P2W-C	
				M5M5255BKP-12	28P4Y	
		with ($\overline{S_1}$, S_2) I_{CC}(Power down) = 50μA(max) = 0.3μA(typ)	70	M5M5255BP-70L	28P4	
				M5M5255BFP-70L	28P2W-C	
				M5M5255BKP-70L	28P4Y	
			85	M5M5255BP-85L	28P4	
				M5M5255BFP-85L	28P2W-C	
				M5M5255BKP-85L	28P4Y	
			100	M5M5255BP-10L	28P4	
				M5M5255BFP-10L	28P2W-C	
				M5M5255BKP-10L	28P4Y	
			120	M5M5255BP-12L	28P4	
				M5M5255BFP-12L	28P2W-C	
				M5M5255BKP-12L	28P4Y	
		with ($\overline{S_1}$, S_2) I_{CC}(Power down) = 10μA(max) = 0.3μA(typ)	70	M5M5255BP-70LL	28P4	
				M5M5255BFP-70LL	28P2W-C	
				M5M5255BKP-70LL	28P4Y	
			85	M5M5255BP-85LL	28P4	
				M5M5255BFP-85LL	28P2W-C	
				M5M5255BKP-85LL	28P4Y	
			100	M5M5255BP-10LL	28P4	
				M5M5255BFP-10LL	28P2W-C	
				M5M5255BKP-10LL	28P4Y	
			120	M5M5255BP-12LL	28P4	
				M5M5255BFP-12LL	28P2W-C	
				M5M5255BKP-12LL	28P4Y	
			70	M5M5256BP-70	28P4	2-9
				M5M5256BFP-70	28P2W-C	
				M5M5256BKP-70	28P4Y	
			85	M5M5256BP-85	28P4	
				M5M5256BFP-85	28P2W-C	
				M5M5256BKP-85	28P4Y	
			100	M5M5256BP-10	28P4	
				M5M5256BFP-10	28P2W-C	
				M5M5256BKP-10	28P4Y	
			120	M5M5256BP-12	28P4	
				M5M5256BFP-12	28P2W-C	
				M5M5256BKP-12	28P4Y	
			150	M5M5256BP-15	28P4	
				M5M5256BFP-15	28P2W-C	
				M5M5256BKP-15	28P4Y	

■ LOW POWER DISSIPATION STATIC RAMs 〔5V Version〕 (Cont.)

Memory capacity	Configuration (Word × Bit)	Circuit function	Access time Max (ns)	Type name	Package outline	Page
256K	32K × 8	Icc(Power down) = 50μA(max) = 0.3μA(typ)	70	M5M5256BP-70L	28P4	2-9
				M5M5256BFP-70L	28P2W-C	
				M5M5256BKP-70L	28P4Y	
				M5M5256BVP-70L	28P2C-A	2-14
				M5M5256BRV-70L	28P2C-B	
			85	M5M5256BP-85L	28P4	2-9
				M5M5256BFP-85L	28P2W-C	
				M5M5256BKP-85L	28P4Y	
				M5M5256BVP-85L	28P2C-A	2-14
				M5M5256BRV-85L	28P2C-B	
			100	M5M5256BP-10L	28P4	2-9
				M5M5256BFP-10L	28P2W-C	
				M5M5256BKP-10L	28P4Y	
				M5M5256BVP-10L	28P2C-A	2-14
				M5M5256BRV-10L	28P2C-B	
			120	M5M5256BP-12L	28P4	2-9
				M5M5256BFP-12L	28P2W-C	
				M5M5256BKP-12L	28P4Y	
				M5M5256BVP-12L	28P2C-A	2-14
				M5M5256BRV-12L	28P2C-B	
			150	M5M5256BP-15L	28P4	2-9
				M5M5256BFP-15L	28P2W-C	
				M5M5256BKP-15L	28P4Y	
				M5M5256BVP-15L	28P2C-A	2-14
				M5M5256BRV-15L	28P2C-B	
		Icc(Power down) = 10μA(max) = 0.3μA(typ)	70	M5M5256BP-70LL	28P4	2-9
				M5M5256BFP-70LL	28P2W-C	
				M5M5256BKP-70LL	28P4Y	
				M5M5256BVP-70LL	28P2C-A	2-14
				M5M5256BRV-70LL	28P2C-B	
			85	M5M5256BP-85LL	28P4	2-9
				M5M5256BFP-85LL	28P2W-C	
				M5M5256BKP-85LL	28P4Y	
				M5M5256BVP-85LL	28P2C-A	2-14
				M5M5256BRV-85LL	28P2C-B	
			100	M5M5256BP-10LL	28P4	2-9
				M5M5256BFP-10LL	28P2W-C	
				M5M5256BKP-10LL	28P4Y	
				M5M5256BVP-10LL	28P2C-A	2-14
				M5M5256BRV-10LL	28P2C-B	
			120	M5M5256BP-12LL	28P4	2-9
				M5M5256BFP-12LL	28P2W-C	
				M5M5256BKP-12LL	28P4Y	
				M5M5256BVP-12LL	28P2C-A	2-14
				M5M5256BRV-12LL	28P2C-B	
			150	M5M5256BP-15LL	28P4	2-9
				M5M5256BFP-15LL	28P2W-C	
				M5M5256BKP-15LL	28P4Y	
				M5M5256BVP-15LL	28P2C-A	2-14
				M5M5256BRV-15LL	28P2C-B	

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■ LOW POWER DISSIPATION STATIC RAMs [5V Version] (Cont.)

Memory capacity	Configuration (Word × Bit)	Circuit function	Access time Max (ns)	Type name		Package outline	Page
256K	32K × 8	with ($\overline{S_1}$, S_2) Icc(Power down) = 10μA(max) = 0.05μA(typ)	55	M5M5255CP-55LL	★	28P4	2-20
				M5M5255CFP-55LL	★	28P2W-C	
				M5M5255CKP-55LL	★	28P4Y	
			70	M5M5255CP-70LL	★	28P4	
				M5M5255CFP-70LL	★	28P2W-C	
				M5M5255CKP-70LL	★	28P4Y	
		with ($\overline{S_1}$, S_2) Icc(Power down) = 2μA(max) = 0.05μA(typ)	55	M5M5255CP-55XL	★	28P4	
				M5M5255CFP-55XL	★	28P2W-C	
				M5M5255CKP-55XL	★	28P4Y	
			70	M5M5255CP-70XL	★	28P4	
				M5M5255CFP-70XL	★	28P2W-C	
				M5M5255CKP-70XL	★	28P4Y	
		Icc(Power down) = 10μA(max) = 0.05μA(typ)	55	M5M5256CP-55LL		28P4	2-27
				M5M5256CFP-55LL		28P2W-C	
				M5M5256CKP-55LL		28P4Y	
				M5M5256CVP-55LL		28P2C-A	
				M5M5256CRV-55LL		28P2C-B	
			70	M5M5256CP-70LL		28P4	
				M5M5256CFP-70LL		28P2W-C	
				M5M5256CKP-70LL		28P4Y	
				M5M5256CVP-70LL		28P2C-A	
				M5M5256CRV-70LL		28P2C-B	
			85	M5M5256CP-85LL		28P4	2-34
				M5M5256CFP-85LL		28P2W-C	
				M5M5256CKP-85LL		28P4Y	
				M5M5256CVP-85LL		28P2C-A	
				M5M5256CRV-85LL		28P2C-B	
			100	M5M5256CP-10LL		28P4	
				M5M5256CFP-10LL		28P2W-C	
				M5M5256CKP-10LL		28P4Y	
				M5M5256CVP-10LL		28P2C-A	
				M5M5256CRV-10LL		28P2C-B	
		Icc(Power down) = 2μA(max) = 0.05μA(typ)	55	M5M5256CP-55XL		28P4	2-27
				M5M5256CFP-55XL		28P2W-C	
				M5M5256CKP-55XL		28P4Y	
				M5M5256CVP-55XL		28P2C-A	
				M5M5256CRV-55XL		28P2C-B	
			70	M5M5256CP-70XL		28P4	
				M5M5256CFP-70XL		28P2W-C	
				M5M5256CKP-70XL		28P4Y	
				M5M5256CVP-70XL		28P2C-A	
				M5M5256CRV-70XL		28P2C-B	
			85	M5M5256CP-85XL		28P4	2-34
				M5M5256CFP-85XL		28P2W-C	
				M5M5256CKP-85XL		28P4Y	
				M5M5256CVP-85XL		28P2C-A	
				M5M5256CRV-85XL		28P2C-B	
			100	M5M5256CP-10XL		28P4	
				M5M5256CFP-10XL		28P2W-C	
				M5M5256CKP-10XL		28P4Y	
				M5M5256CVP-10XL		28P2C-A	
				M5M5256CRV-10XL		28P2C-B	

★ : New product

■ LOW POWER DISSIPATION STATIC RAMs 〔5V Version〕 (Cont.)

Memory capacity	Configuration (Word × Bit)	Circuit function	Access time Max (ns)	Type name	Package outline	Page
1M	128K × 8	with ($\overline{S_1}$, S_2) Icc(Power down) = 50μA(max) = 0.3μA(typ)	55	M5M51008AP-55L	32P4	2-41
				M5M51008AFP-55L	32P2M-A	
				M5M51008AVP-55L	32P3H-E	
				M5M51008ARV-55L	32P3H-F	
			70	M5M51008AP-70L	32P4	2-48
				M5M51008AFP-70L	32P2M-A	
				M5M51008AVP-70L	32P3H-E	
				M5M51008ARV-70L	32P3H-F	
			85	M5M51008AP-85L	32P4	
				M5M51008AFP-85L	32P2M-A	
				M5M51008AVP-85L	32P3H-E	
				M5M51008ARV-85L	32P3H-F	
			100	M5M51008AP-10L	32P4	
				M5M51008AFP-10L	32P2M-A	
				M5M51008AVP-10L	32P3H-E	
				M5M51008ARV-10L	32P3H-F	
			120	M5M51008AP-12L	32P4	
				M5M51008AFP-12L	32P2M-A	
				M5M51008AVP-12L	32P3H-E	
				M5M51008ARV-12L	32P3H-F	
		with ($\overline{S_1}$, S_2) Icc(Power down) = 10μA(max) = 0.3μA(typ)	55	M5M51008AP-55LL	32P4	2-41
				M5M51008AFP-55LL	32P2M-A	
				M5M51008AVP-55LL	32P3H-E	
				M5M51008ARV-55LL	32P3H-F	
			70	M5M51008AP-70LL	32P4	2-48
				M5M51008AFP-70LL	32P2M-A	
				M5M51008AVP-70LL	32P3H-E	
				M5M51008ARV-70LL	32P3H-F	
			85	M5M51008AP-85LL	32P4	
				M5M51008AFP-85LL	32P2M-A	
				M5M51008AVP-85LL	32P3H-E	
				M5M51008ARV-85LL	32P3H-F	
			100	M5M51008AP-10LL	32P4	
				M5M51008AFP-10LL	32P2M-A	
				M5M51008AVP-10LL	32P3H-E	
				M5M51008ARV-10LL	32P3H-F	
			120	M5M51008AP-12LL	32P4	
				M5M51008AFP-12LL	32P2M-A	
				M5M51008AVP-12LL	32P3H-E	
				M5M51008ARV-12LL	32P3H-F	

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■ LOW POWER DISSIPATION STATIC RAMs 〔5V Version〕 (Cont.)

Memory capacity	Configuration (Word × Bit)	Circuit function	Access time Max (ns)	Type name		Package outline	Page
1M	128K × 8	with ($\overline{S_1}$, S_2) Icc(Power down) = 2μA(max) = 0.05μA(typ) TFT Load Type	55	M5M51T08AP-55SL		32P4	2-55
				M5M51T08AFP-55SL		32P2M-A	
				M5M51T08AVP-55SL		32P3H-E	
				M5M51T08ARV-55SL		32P3H-F	
			70	M5M51T08AP-70SL		32P4	2-62
				M5M51T08AFP-70SL		32P2M-A	
				M5M51T08AVP-70SL		32P3H-E	
				M5M51T08ARV-70SL		32P3H-F	
			85	M5M51T08AP-85SL		32P4	
				M5M51T08AFP-85SL		32P2M-A	
				M5M51T08AVP-85SL		32P3H-E	
				M5M51T08ARV-85SL		32P3H-F	
			100	M5M51T08AP-10SL		32P4	
				M5M51T08AFP-10SL		32P2M-A	
				M5M51T08AVP-10SL		32P3H-E	
				M5M51T08ARV-10SL		32P3H-F	
			120	M5M51T08AP-12SL		32P4	
				M5M51T08AFP-12SL		32P2M-A	
				M5M51T08AVP-12SL		32P3H-E	
				M5M51T08ARV-12SL		32P3H-F	
		with ($\overline{S_1}$, S_2) Icc(Power down) = 50μA(max) = 0.3μA(typ)	55	M5M51008BP-55L	★	32P4	2-69
				M5M51008BFP-55L	★	32P2M-A	
				M5M51008BVP-55L	★	32P3H-E	
				M5M51008BRV-55L	★	32P3H-F	
			70	M5M51008BP-70L	★	32P4	
				M5M51008BFP-70L	★	32P2M-A	
				M5M51008BVP-70L	★	32P3H-E	
				M5M51008BRV-70L	★	32P3H-F	
			100	M5M51008BP-10L	★	32P4	
				M5M51008BFP-10L	★	32P2M-A	
				M5M51008BVP-10L	★	32P3H-E	
				M5M51008BRV-10L	★	32P3H-F	
		with ($\overline{S_1}$, S_2) Icc(Power down) = 10μA(max) = 0.3μA(typ)	55	M5M51008BP-55LL	★	32P4	
				M5M51008BFP-55LL	★	32P2M-A	
				M5M51008BVP-55LL	★	32P3H-E	
				M5M51008BRV-55LL	★	32P3H-F	
			70	M5M51008BP-70LL	★	32P4	
				M5M51008BFP-70LL	★	32P2M-A	
				M5M51008BVP-70LL	★	32P3H-E	
				M5M51008BRV-70LL	★	32P3H-F	
			100	M5M51008BP-10LL	★	32P4	
				M5M51008BFP-10LL	★	32P2M-A	
				M5M51008BVP-10LL	★	32P3H-E	
				M5M51008BRV-10LL	★	32P3H-F	

★ : New product

■ LOW POWER DISSIPATION STATIC RAMs 〔5V Version〕 (Cont.)

Memory capacity	Configuration (Word × Bit)	Circuit function	Access time Max (ns)	Type name	Package outline	Page
1M	64K × 16	with (CS, $\overline{BC_1}$, $\overline{BC_2}$) Icc(Power down) = 50μA(max) = 0.3μA(typ)	70	M5M51016ATP-70L	44P3W-H	2-76
				M5M51016ART-70L	44P3W-J	
			85	M5M51016ATP-85L	44P3W-H	
				M5M51016ART-85L	44P3W-J	
			100	M5M51016ATP-10L	44P3W-H	
				M5M51016ART-10L	44P3W-J	
		with (CS, $\overline{BC_1}$, $\overline{BC_2}$) Icc(Power down) = 10μA(max) = 0.3μA(typ)	70	M5M51016ATP-70LL	44P3W-H	
				M5M51016ART-70LL	44P3W-J	
			85	M5M51016ATP-85LL	44P3W-H	
				M5M51016ART-85LL	44P3W-J	
			100	M5M51016ATP-10LL	44P3W-H	
				M5M51016ART-10LL	44P3W-J	
		with (CS, $\overline{BC_1}$, $\overline{BC_2}$) Icc(Power down) = 50μA(max) = 0.3μA(typ)	70	M5M51016BTP-70L ★★	44P3W-H	2-83
				M5M51016BRT-70L ★★	44P3W-J	
			100	M5M51016BTP-10L ★★	44P3W-H	
				M5M51016BRT-10L ★★	44P3W-J	
		with (CS, $\overline{BC_1}$, $\overline{BC_2}$) Icc(Power down) = 10μA(max) = 0.3μA(typ)	70	M5M51016BTP-70LL ★★	44P3W-H	
				M5M51016BRT-70LL ★★	44P3W-J	
			100	M5M51016BTP-10LL ★★	44P3W-H	
				M5M51016BRT-10LL ★★	44P3W-J	
4M	512K × 8	Icc(Power down) = 50μA(max) = 0.4μA(typ)	55	M5M5408FP-55L ★	32P2M-A	2-90
				M5M5408TP-55L ★	32P3Y-H	
				M5M5408RT-55L ★	32P3Y-J	
			70	M5M5408FP-70L	32P2M-A	
				M5M5408TP-70L	32P3Y-H	
				M5M5408RT-70L	32P3Y-J	
			100	M5M5408FP-10L	32P2M-A	
				M5M5408TP-10L	32P3Y-H	
				M5M5408RT-10L	32P3Y-J	
		Icc(Power down) = 10μA(max) = 0.4μA(typ)	55	M5M5408FP-55LL ★	32P2M-A	
				M5M5408TP-55LL ★	32P3Y-H	
				M5M5408RT-55LL ★	32P3Y-J	
			70	M5M5408FP-70LL	32P2M-A	
				M5M5408TP-70LL	32P3Y-H	
				M5M5408RT-70LL	32P3Y-J	
			100	M5M5408FP-10LL	32P2M-A	
				M5M5408TP-10LL	32P3Y-H	
				M5M5408RT-10LL	32P3Y-J	

★ : New product ★★ : Under development

■ LOW POWER DISSIPATION STATIC RAMs 〔5V Version〕 (Cont.)

Memory capacity	Configuration (Word × Bit)	Circuit function	Access time Max (ns)	Type name		Package outline	Page
4M	512K × 8	Icc(Power down) = 50μA(max) = 0.1μA(typ)	55	M5M5408AFP-55L	★★	32P2M-A	2-97
				M5M5408ATP-55L	★★	32P3Y-H	
				M5M5408ART-55L	★★	32P3Y-J	
			70	M5M5408AFP-70L	★★	32P2M-A	
				M5M5408ATP-70L	★★	32P3Y-H	
				M5M5408ART-70L	★★	32P3Y-J	
			100	M5M5408AFP-10L	★★	32P2M-A	
				M5M5408ATP-10L	★★	32P3Y-H	
				M5M5408ART-10L	★★	32P3Y-J	
		Icc(Power down) = 10μA(max) = 0.1μA(typ)	55	M5M5408AFP-55LL	★★	32P2M-A	
				M5M5408ATP-55LL	★★	32P3Y-H	
				M5M5408ART-55LL	★★	32P3Y-J	
			70	M5M5408AFP-70LL	★★	32P2M-A	
				M5M5408ATP-70LL	★★	32P3Y-H	
				M5M5408ART-70LL	★★	32P3Y-J	
			100	M5M5408AFP-10LL	★★	32P2M-A	
				M5M5408ATP-10LL	★★	32P3Y-H	
				M5M5408ART-10LL	★★	32P3Y-J	

★★ : Under development

■ LOW POWER DISSIPATION STATIC RAMs (Low voltage Version)

Memory capacity	Configuration (Word × Bit)	Circuit function	Access time Max (ns)	Type name		Package outline	Page
256K	32K × 8	Low Voltage Operation (3.0~3.6V) Icc(Power down) = 10μA(max) = 0.05μA(typ)	85	M5M5256CFP-85VLL	★	28P2W-C	3-3
				M5M5256CVP-85VLL	★	28P2C-A	
				M5M5256CRV-85VLL	★	28P2C-B	
			100	M5M5256CFP-10VLL	★	28P2W-C	
				M5M5256CVP-10VLL	★	28P2C-A	
				M5M5256CRV-10VLL	★	28P2C-B	
		Low Voltage Operation (3.0~3.6V) Icc(Power down) = 2μA(max) = 0.05μA(typ)	85	M5M5256CFP-85VXL	★	28P2W-C	
				M5M5256CVP-85VXL	★	28P2C-A	
				M5M5256CRV-85VXL	★	28P2C-B	
			100	M5M5256CFP-10VXL	★	28P2W-C	
				M5M5256CVP-10VXL	★	28P2C-A	
				M5M5256CRV-10VXL	★	28P2C-B	
		Low Voltage Operation (2.7~5.5V) Icc(Power down) = 10μA(max) = 0.05μA(typ)	120	M5M5256CFP-12VLL	★	28P2W-C	3-10
				M5M5256CVP-12VLL	★	28P2C-A	
				M5M5256CRV-12VLL	★	28P2C-B	
			150	M5M5256CFP-15VLL	★	28P2W-C	
				M5M5256CVP-15VLL	★	28P2C-A	
				M5M5256CRV-15VLL	★	28P2C-B	
		Low Voltage Operation (2.7~5.5V) Icc(Power down) = 2μA(max) = 0.05μA(typ)	120	M5M5256CFP-12VXL	★	28P2W-C	
				M5M5256CVP-12VXL	★	28P2C-A	
				M5M5256CRV-12VXL	★	28P2C-B	
			150	M5M5256CFP-15VXL	★	28P2W-C	
				M5M5256CVP-15VXL	★	28P2C-A	
				M5M5256CRV-15VXL	★	28P2C-B	
1M	128K × 8	Low Voltage Operation (3.0~3.6V) Icc(Power down) = 50μA(max) = 0.3μA(typ)	85	M5M51008AFP-85VL	★★	32P2M-A	3-17
				M5M51008AVP-85VL	★★	32P3H-E	
				M5M51008ARV-85VL	★★	32P3H-F	
			100	M5M51008AFP-10VL	★	32P2M-A	
				M5M51008AVP-10VL	★	32P3H-E	
				M5M51008ARV-10VL	★	32P3H-F	
		Low Voltage Operation (3.0~3.6V) Icc(Power down) = 10μA(max) = 0.3μA(typ)	85	M5M51008AFP-85VLL	★★	32P2M-A	
				M5M51008AVP-85VLL	★★	32P3H-E	
				M5M51008ARV-85VLL	★★	32P3H-F	
			100	M5M51008AFP-10VLL	★	32P2M-A	
				M5M51008AVP-10VLL	★	32P3H-E	
				M5M51008ARV-10VLL	★	32P3H-F	
		Low Voltage Operation (2.7~5.5V) Icc(Power down) = 50μA(max) = 0.3μA(typ)	120	M5M51008AFP-12VL	★	32P2M-A	3-24
				M5M51008AVP-12VL	★	32P3H-E	
				M5M51008ARV-12VL	★	32P3H-F	
			150	M5M51008AFP-15VL	★	32P2M-A	
				M5M51008AVP-15VL	★	32P3H-E	
				M5M51008ARV-15VL	★	32P3H-F	
		Low Voltage Operation (2.7~5.5V) Icc(Power down) = 10μA(max) = 0.3μA(typ)	120	M5M51008AFP-12VLL	★	32P2M-A	
				M5M51008AVP-12VLL	★	32P3H-E	
				M5M51008ARV-12VLL	★	32P3H-F	
			150	M5M51008AFP-15VLL	★	32P2M-A	
				M5M51008AVP-15VLL	★	32P3H-E	
				M5M51008ARV-15VLL	★	32P3H-F	

★ : New product ★★ : Under development

■ LOW POWER DISSIPATION STATIC RAMs 〔Low voltage Version〕 (Cont.)

Memory capacity	Configuration (Word × Bit)	Circuit function	Access time Max (ns)	Type name		Package outline	Page
1M	128K × 8	Low Voltage Operation (3.0~3.6V) Icc(Power down) = 2μA(max) = 0.05μA(typ) TFT Load Type	85	M5M51T08AFP-85VSL	★★	32P2M-A	3-31
				M5M51T08AVP-85VSL	★★	32P3H-E	
				M5M51T08ARV-85VSL	★★	32P3H-F	
			100	M5M51T08AFP-10VSL	★★	32P2M-A	
				M5M51T08AVP-10VSL	★★	32P3H-E	
				M5M51T08ARV-10VSL	★★	32P3H-F	
		Low Voltage Operation (2.7~5.5V) Icc(Power down) = 2μA(max) = 0.05μA(typ) TFT Load Type	120	M5M51T08AFP-12VSL	★★	32P2M-A	3-38
				M5M51T08AVP-12VSL	★★	32P3H-E	
				M5M51T08ARV-12VSL	★★	32P3H-F	
			150	M5M51T08AFP-15VSL	★★	32P2M-A	
				M5M51T08AVP-15VSL	★★	32P3H-E	
				M5M51T08ARV-15VSL	★★	32P3H-F	
		Low Voltage Operation (3.0~3.6V) Icc(Power down) = 50μA(max) = 0.3μA(typ)	70	M5M51008BFP-70VL	★★	32P2M-A	3-45
				M5M51008BVP-70VL	★★	32P3H-E	
				M5M51008BRV-70VL	★★	32P3H-F	
			100	M5M51008BFP-10VL	★★	32P2M-A	
				M5M51008BVP-10VL	★★	32P3H-E	
				M5M51008BRV-10VL	★★	32P3H-F	
		Low Voltage Operation (2.7~5.5V) Icc(Power down) = 50μA(max) = 0.3μA(typ)	120	M5M51008BFP-12VL	★★	32P2M-A	
				M5M51008BVP-12VL	★★	32P3H-E	
				M5M51008BRV-12VL	★★	32P3H-F	
			150	M5M51008BFP-15VL	★★	32P2M-A	
				M5M51008BVP-15VL	★★	32P3H-E	
				M5M51008BRV-15VL	★★	32P3H-F	
		Low Voltage Operation (3.0~3.6V) Icc(Power down) = 10μA(max) = 0.3μA(typ)	70	M5M51008BFP-70VLL	★★	32P2M-A	
				M5M51008BVP-70VLL	★★	32P3H-E	
				M5M51008BRV-70VLL	★★	32P3H-F	
			100	M5M51008BFP-10VLL	★★	32P2M-A	
				M5M51008BVP-10VLL	★★	32P3H-E	
				M5M51008BRV-10VLL	★★	32P3H-F	
		Low Voltage Operation (2.7~5.5V) Icc(Power down) = 10μA(max) = 0.3μA(typ)	120	M5M51008BFP-12VLL	★★	32P2M-A	
				M5M51008BVP-12VLL	★★	32P3H-E	
				M5M51008BRV-12VLL	★★	32P3H-F	
			150	M5M51008BFP-15VLL	★★	32P2M-A	
				M5M51008BVP-15VLL	★★	32P3H-E	
				M5M51008BRV-15VLL	★★	32P3H-F	
	64K × 16	Low Voltage Operation (3.0~3.6V) Icc(Power down)=50μA(max) =0.3μA(typ)	100	M5M51016ATP-10VL	★	44P3W-H	3-52
				M5M51016ART-10VL	★	44P3W-J	
		Low Voltage Operation (3.0~3.6V) Icc(Power down)=10μA(max) =0.3μA(typ)		M5M51016ATP-10VLL	★	44P3W-H	
				M5M51016ART-10VLL	★	44P3W-J	
		Low Voltage Operation (2.7~5.5V) Icc(Power down)=50μA(max) =0.3μA(typ)	150	M5M51016ATP-15VL	★	44P3W-H	3-59
				M5M51016ART-15VL	★	44P3W-J	
		Low Voltage Operation (2.7~5.5V) Icc(Power down)=10μA(max) =0.3μA(typ)		M5M51016ATP-15VLL	★	44P3W-H	
				M5M51016ART-15VLL	★	44P3W-J	
4M	512K × 8	Low Voltage Operation (3.0~3.6V) Icc(Power down) = 50μA(max) = 0.4μA(typ)	85	M5M5408FP-85VL	★★	32P2M-A	3-66
				M5M5408TP-85VL	★★	32P3Y-H	
				M5M5408RT-85VL	★★	32P3Y-J	
			100	M5M5408FP-10VL	★★	32P2M-A	
				M5M5408TP-10VL	★★	32P3Y-H	
				M5M5408RT-10VL	★★	32P3Y-J	
		Low Voltage Operation (3.0~3.6V) Icc(Power down) = 10μA(max) = 0.4μA(typ)	85	M5M5408FP-85VLL	★★	32P2M-A	
				M5M5408TP-85VLL	★★	32P3Y-H	
				M5M5408RT-85VLL	★★	32P3Y-J	
			100	M5M5408FP-10VLL	★★	32P2M-A	
				M5M5408TP-10VLL	★★	32P3Y-H	
				M5M5408RT-10VLL	★★	32P3Y-J	

★ : New product ★★ : Under development

INDEX BY FUNCTION

■ LOW POWER DISSIPATION STATIC RAMs WITH A WIDE OPERATINGS TEMPERATURE RANGE

Operating voltage range (Note 1)	Memory capacity (bit)	Memory configuration (word)	Stand-by current (model name in parentheses)	Operating voltage range	Type name	Access time (ns)			
						55	70	100	150
− 20~70℃	256K	32K × 8	10μA (LL) 2μA (XL)	5V ± 10%	M5M5256CP	○	○	○	
					M5M5256CFP	○	○	○	
					M5M5256CVP	○	○	○	
					M5M5256CRV	○	○	○	
					M5M5256CKP	○	○	○	
				3.0~3.6V/5.5V	M5M5256CFP			○	○
					M5M5256CVP			○	○
					M5M5256CRV			○	○
	1M	128K × 8	50μA (L) 10μA (LL)	5V ± 10%	M5M51008AP	○	○	○	
					M5M51008AFP	○	○	○	
					M5M51008AVP	○	○	○	
					M5M51008ARV	○	○	○	
			2μA (SL)		M5M51T08AP	○	○	○	
					M5M51T08AFP	○	○	○	
					M5M51T08AVP	○	○	○	
					M5M51T08ARV	○	○	○	
			50μA (L) 10μA (LL)	3.0~3.6V/5.5V	M5M51008AFP			○	○
					M5M51008AVP			○	○
					M5M51008ARV			○	○
			2μA (SL)		M5M51T08AFP			○	○
					M5M51T08AVP			○	○
					M5M51T08ARV			○	○
		64K × 16	50μA (L) 10μA (LL)	5V ± 10%	M5M51016ATP		○	○	
					M5M51016ART		○	○	
− 40~85℃	256K	32K × 8	20μA (LL) 4μA (XL)	5V ± 10%	M5M5256CP		○	○	
					M5M5256CFP		○	○	
					M5M5256CVP		○	○	
					M5M5256CRV		○	○	
					M5M5256CKP		○	○	
				3.0~3.6V/5.5V	M5M5256CFP			○	○
					M5M5256CVP			○	○
					M5M5256CRV			○	○
	1M	128K × 8	100μA (L) 20μA (LL)	5V ± 10%	M5M51008AP		○	○	
					M5M51008AFP		○	○	
					M5M51008AVP		○	○	
					M5M51008ARV		○	○	
			4μA (SL)		M5M51T08AP		○	○	
					M5M51T08AFP		○	○	
					M5M51T08AVP		○	○	
					M5M51T08ARV		○	○	
			100μA (L) 20μA (LL)	3.0~3.6V/5.5V	M5M51008AFP			○	○
					M5M51008AVP			○	○
					M5M51008ARV			○	○
			4μA (SL)		M5M51T08AFP			○	○
					M5M51T08AVP			○	○
					M5M51T08ARV			○	○
		64K × 16	100μA (L) 20μA (LL)	5V ± 10%	M5M51016ATP			○	
					M5M51016ART			○	

Note 1. Products with an operating temperature range from − 20℃ to 70℃ are called "W version."
Those with an operating temperature range from − 40℃ to 85℃ are called "I version."
Consult our distoributors or us for more derails. Refer to data sheets for standard characteristics of these products.

■ HIGH SPEED STATIC RAMs [5V Version]

Memory capacity	Configuration (Word × Bit)	Circuit function	Access time Max (ns)	Type name	Package outline	Page
256K	256K × 1		12	M5M5257DP-12	24P4Y	4-3
				M5M5257DJ-12	24P0J	
			15	M5M5257DP-15	24P4Y	
				M5M5257DJ-15	24P0J	
			20	M5M5257DP-20	24P4Y	
				M5M5257DJ-20	24P0J	
		Icc Stand by 50μA (max) (Vcc = 3.0V) Low Power Version	15	M5M5257DP-15L	24P4Y	
				M5M5257DJ-15L	24P0J	
			20	M5M5257DP-20L	24P4Y	
				M5M5257DJ-20L	24P0J	
	64K × 4		12	M5M5258DP-12	24P4Y	4-8
				M5M5258DJ-12	24P0J	
			15	M5M5258DP-15	24P4Y	
				M5M5258DJ-15	24P0J	
			20	M5M5258DP-20	24P4Y	
				M5M5258DJ-20	24P0J	
		Icc Stand by 50μA (max) (Vcc = 3.0V) Low Power Version	15	M5M5258DP-15L	24P4Y	
				M5M5258DJ-15L	24P0J	
			20	M5M5258DP-20L	24P4Y	
				M5M5258DJ-20L	24P0J	
	32K × 8	8-bit I/O	12	M5M5278DP-12	28P4Y	4-13
				M5M5278DJ-12	28P0J	
			15	M5M5278DP-15	28P4Y	
				M5M5278DJ-15	28P0J	
				M5M5278DFP-15	28P2W-C	
				M5M5278DVP-15	28P2C-A	
			20	M5M5278DP-20	28P4Y	
				M5M5278DJ-20	28P0J	
				M5M5278DFP-20	28P2W-C	
				M5M5278DVP-20	28P2C-A	
		Icc Stand by = 50μA (Vcc = 3.0V) Low Power Version	15	M5M5278DP-15L	28P4Y	
				M5M5278DJ-15L	28P0J	
				M5M5278DFP-15L	28P2W-C	
				M5M5278DVP-15L	28P2C-A	
			20	M5M5278DP-20L	28P4Y	
				M5M5278DJ-20L	28P0J	
				M5M5278DFP-20L	28P2W-C	
				M5M5278DVP-20L	28P2C-A	

■ HIGH SPEED STATIC RAMs 〔5V Version〕 (Cont.)

Memory capacity	Configuration (Word × Bit)	Circuit function	Access time Max (ns)	Type name	Package outline	Page
1M	1M × 1		15	M5M51001BP-15	28P4F	4-19
				M5M51001BJ-15	28P0K	
			20	M5M51001BP-20	28P4F	
				M5M51001BJ-20	28P0K	
			25	M5M51001BP-25	28P4F	
				M5M51001BJ-25	28P0K	
			20	M5M51001BP-20L	28P4F	
				M5M51001BJ-20L	28P0K	
			25	M5M51001BP-25L	28P4F	
				M5M51001BJ-25L	28P0K	
	256K × 4		15	M5M51004BP-15	28P4F	4-25
				M5M51004BJ-15	28P0K	
			20	M5M51004BP-20	28P4F	
				M5M51004BJ-20	28P0K	
			25	M5M51004BP-25	28P4F	
				M5M51004BJ-25	28P0K	
			20	M5M51004BP-20L	28P4F	
				M5M51004BJ-20L	28P0K	
			25	M5M51004BP-25L	28P4F	
				M5M51004BJ-25L	28P0K	

■ HIGH SPEED STATIC RAMs 〔5V Version〕 (300mil)

Memory capacity	Configuration (Word × Bit)	Circuit function	Access time Max (ns)	Type name	Package outline	Page
1M	128K × 8		15	M5M51288BKP-15	32P4Y	4-31
				M5M51288BKJ-15	32P0J	
			20	M5M51288BKP-20	32P4Y	
				M5M51288BKJ-20	32P0J	
				M5M51288BVP-20	32P3H-E	
			25	M5M51288BKP-25	32P4Y	
				M5M51288BKJ-25	32P0J	
				M5M51288BVP-25	32P3H-E	
		Icc Stand by = 50μA (Vcc = 3.0V) Low Power Version	20	M5M51288BKP-20L	32P4Y	
				M5M51288BKJ-20L	32P0J	
				M5M51288BVP-20L	32P3H-E	
			25	M5M51288BKP-25L	32P4Y	
				M5M51288BKJ-25L	32P0J	
				M5M51288BVP-25L	32P3H-E	

INDEX BY FUNCTION

■ HIGH SPEED STATIC RAMs 〔Low voltage Version〕

Memory capacity	Configuration (Word × Bit)	Circuit function	Access time Max (ns)	Type name		Package outline	Page
256K	32K × 8	Vcc = 3.3V $^{+10\%}_{-5\%}$	15	M5M5V278DP-15		28P4Y	5-3
				M5M5V278DJ-15		28P0J	
				M5M5V278DVP-15		28P2C-A	
			20	M5M5V278DP-20		28P4Y	
				M5M5V278DJ-20		28P0J	
				M5M5V278DVP-20		28P2C-A	
		Vcc = 3.3V $^{+10\%}_{-5\%}$	10	M5M5V278EJ-10	★★	28P0J	5-9
				M5M5V278EVP-10	★★	28P2C-A	
			12	M5M5V278EJ-12	★★	28P0J	
				M5M5V278EVP-12	★★	28P2C-A	
			15	M5M5V278EJ-15	★★	28P0J	
				M5M5V278EVP-15	★★	28P2C-A	

★★ : Under development

■ HIGH SPEED STATIC RAMs 〔Synchronous〕

Memory capacity	Configuration (Word × Bit)	Circuit function	Access/Cycle (ns)	Type name		Package outline	Page
1M	32K × 32	Vcc = 3.13~3.6V Sync. Burst Pipeline	5.5/10.0	M5M5V1132FP-6	★	100P6S-C	5-15
			7.0/13.3	M5M5V1132FP-7	★		
			8.0/15.0	M5M5V1132FP-8	★		
			10.0/16.7	M5M5V1132FP-10	★		
		Vcc = 3.13~3.6V Sync. Burst Pipeline Low Power Version Icc Stand by = max 200μA	7.0/13.3	M5M5V1132FP-7L	★		
			8.0/15.0	M5M5V1132FP-8L	★		
			10.0/16.7	M5M5V1132FP-10L	★		
		Vcc = 3.13~3.6V Sync. Burst Pipeline	3.0/6.7	M5M5V1132AFP-3	★★		5-28
				M5M5V1132AGP-3	★★	100P6A	
			4.0/8.0	M5M5V1132AFP-4	★★	100P6S-C	
				M5M5V1132AGP-4	★★	100P6A	
			5.5/10.0	M5M5V1132AFP-6	★★	100P6S-C	
				M5M5V1132AGP-6	★★	100P6A	
			7.0/13.3	M5M5V1132AFP-7	★★	100P6S-C	
				M5M5V1132AGP-7	★★	100P6A	
			8.0/15.0	M5M5V1132AFP-8	★★	100P6S-C	
				M5M5V1132AGP-8	★★	100P6A	

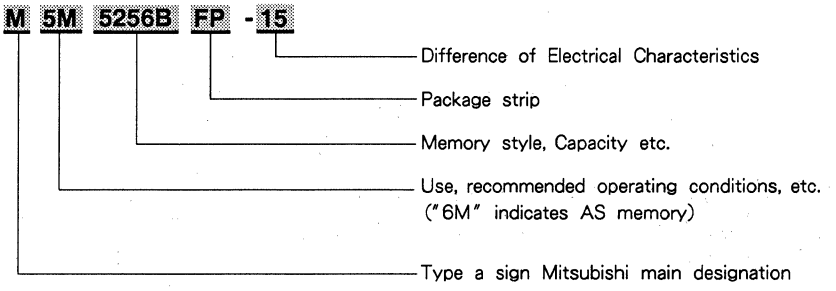
★ : New product ★★ : Under development

ORDERING INFORMATION

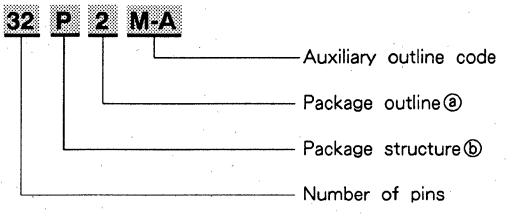
Understanding the Type-Designation Code

Type-designation examples are provided below to provide information about the products and their packages. These type designations are comprised of code elements. The blanks in some of the examples indicate that a code element is not necessary. When writing the type designation, the blank spaces are closed.

Example 1.



Example 2.(Package)



ⓐ **1** : DIP (Except for Plastic)
2 : SOP
3 : TSOP
4 : DIP (Plastic)
5 : SIP, ZIP
6 : QFP
8 : PGA
9 : Specialize, SIP
0 : Leadless, PLCC, SOJ

ⓑ **K** : Glass-sealed ceramic
N : PCB Module (Glass epoxy)
P : Molded plastic

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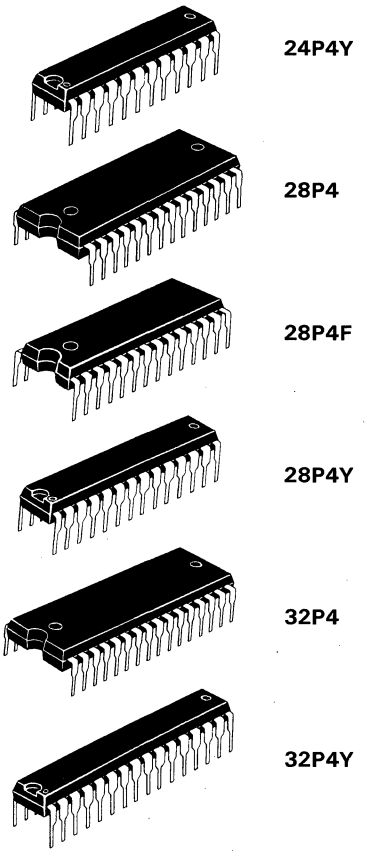
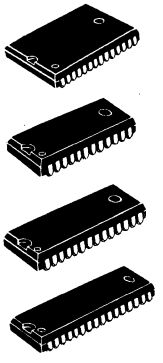
PACKAGE OUTWARD

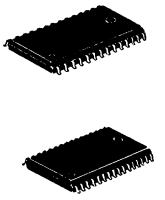
DIP



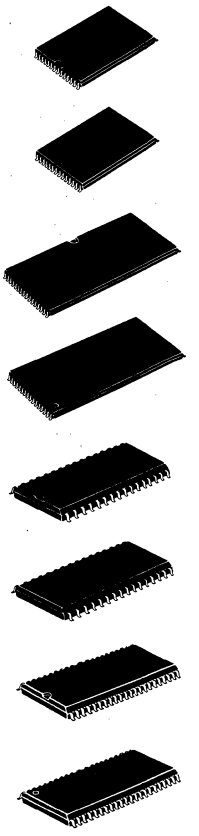
SOJ



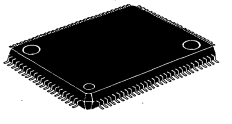
SOP



TSOP



QFP



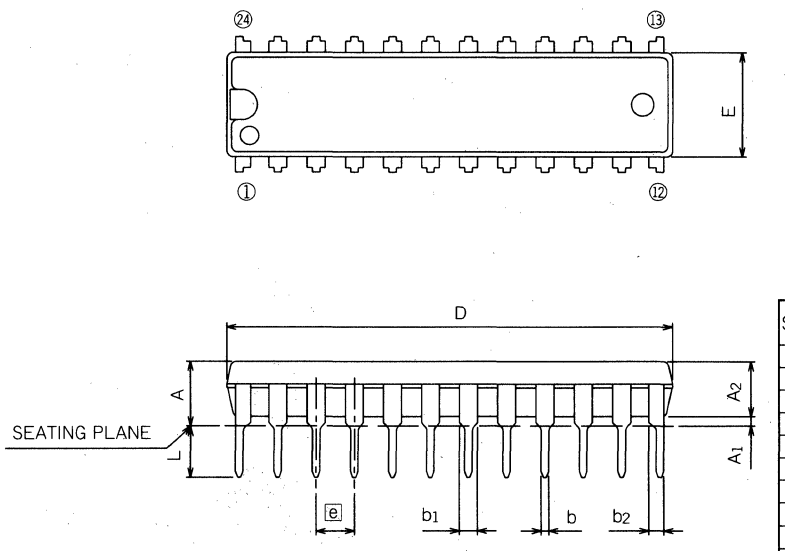
PACKAGE OUTLINES

24P4Y

Plastic 24pin 300mil DIP

EIAJ Package Code	JEDEC Code	Weight(g)
*DIP024-P-0300	—	1.61

Scale : 2/1



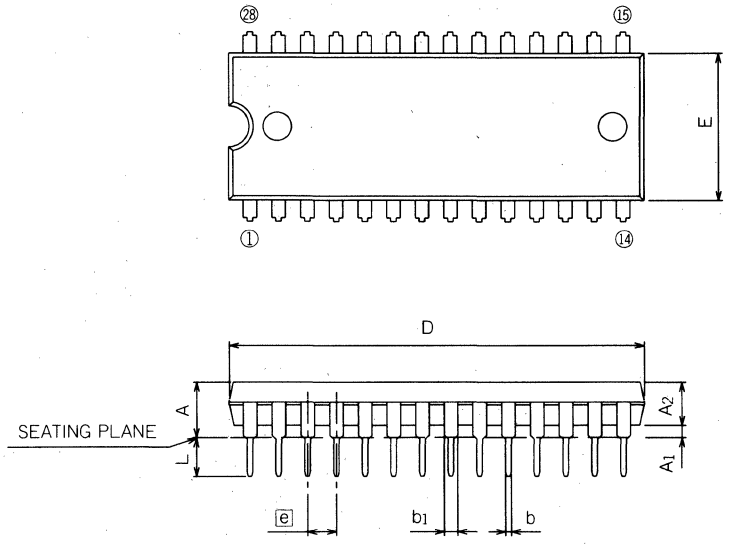
Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	—	—	4.75
A_1	0.51	—	—
A_2	—	3.65	—
b	0.4	0.5	0.6
b_1	1.1	1.2	1.5
b_2	0.9	1.0	1.3
c	0.2	0.25	0.32
D	29.4	29.6	29.8
E	6.75	6.9	7.05
e	—	2.54	—
e1	—	7.62	—
L	3.0	—	
θ	0°	—	15°

28P4

Plastic 28pin 600mil DIP

EIAJ Package Code	JEDEC Code	Weight(g)
*DIP028-P-0600	—	3.8

Scale : 1.5/1



Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	—	—	5.5
A_1	0.51	—	—
A_2	—	3.8	—
b	0.4	0.5	0.6
b_1	1.1	1.2	1.5
c	0.22	0.27	0.34
D	36.5	36.7	36.9
E	12.85	13.0	13.15
e	—	2.54	—
e1	—	15.24	—
L	3.0	—	—
θ	0°	—	15°

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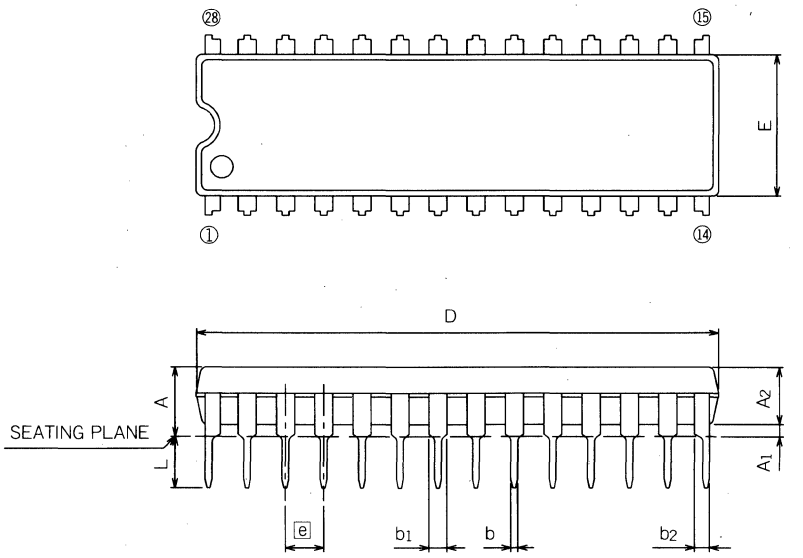
PACKAGE OUTLINES

28P4F

Plastic 28pin 400mil DIP

EIAJ Package Code	JEDEC Code	Weight(g)
* DIP028-P-0400	—	2.9

Scale : 2/1



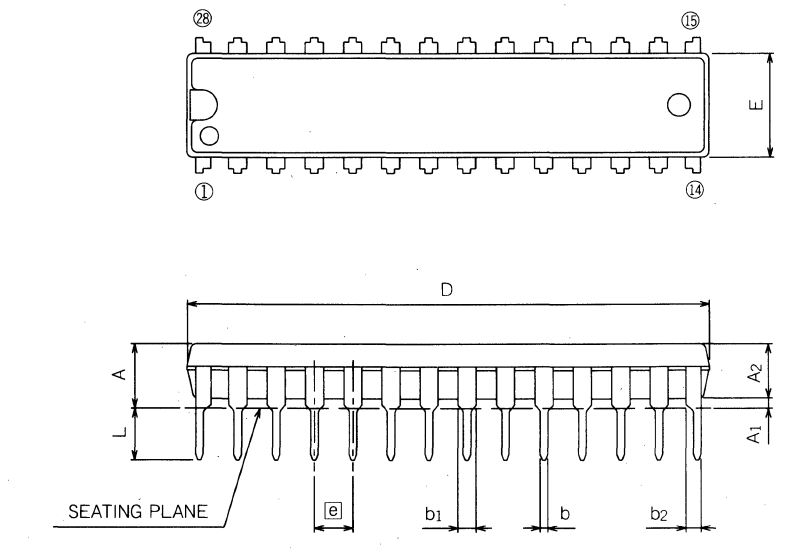
Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	—	—	5.08
A_1	0.51	—	—
A_2	—	3.8	—
b	0.4	0.5	0.6
b_1	1.1	1.2	1.5
b_2	0.9	1.0	1.3
c	0.2	0.25	0.32
D	34.48	34.68	34.88
E	9.25	9.4	9.55
e	—	2.54	—
e_1	—	10.16	—
L	3.0	—	—
θ	0°	—	15°

28P4Y

Plastic 28pin 300mil DIP

EIAJ Package Code	JEDEC Code	Weight(g)
* DIP028-P-0300	—	1.93

Scale : 2/1



Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	—	—	4.75
A_1	0.51	—	—
A_2	—	3.65	—
b	0.4	0.5	0.6
b_1	1.1	1.2	1.5
b_2	0.9	1.0	1.3
c	0.2	0.25	0.32
D	34.45	34.65	34.85
E	6.75	6.9	7.05
e	—	2.54	—
e_1	—	7.62	—
L	3.0	—	—
θ	0°	—	15°

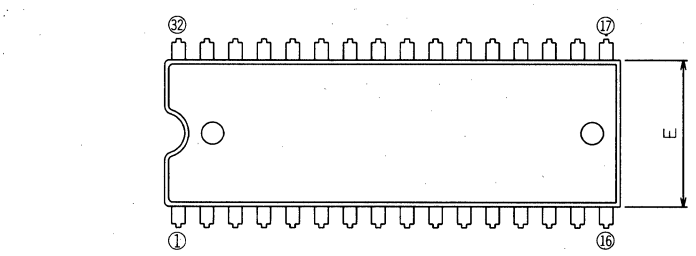
PACKAGE OUTLINES

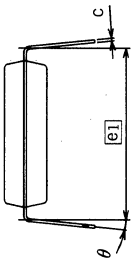
32P4

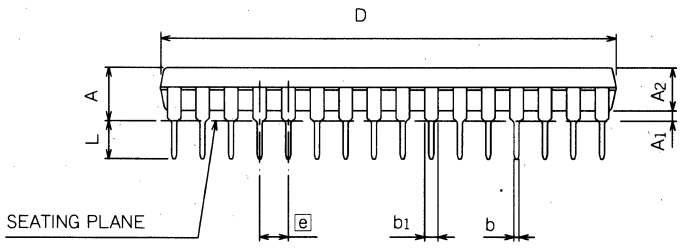
Plastic 32pin 600mil DIP

EIAJ Package Code	JEDEC Code	Weight(g)
* DIP032-P-0600	—	4.08

Scale : 1.5/1







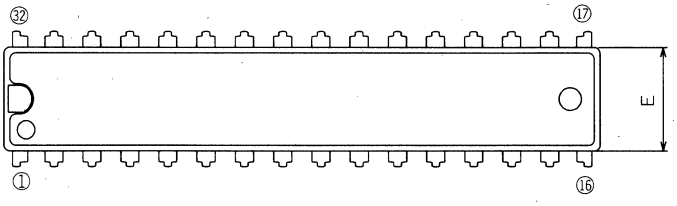
Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	—	—	5.1
A_1	0.51	—	—
A_2	—	3.8	—
b	0.35	0.45	0.55
b_1	1.1	1.2	1.5
c	0.2	0.25	0.32
D	40.4	40.6	40.8
E	12.85	13.0	13.15
e	—	2.54	—
e_1	—	15.24	—
L	3.0	—	—
θ	0°	—	15°

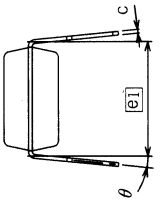
32P4Y

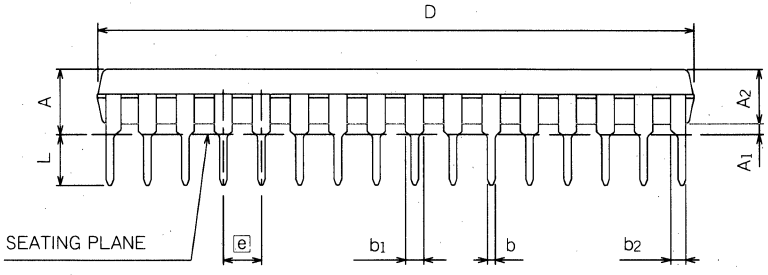
Plastic 32pin 300mil DIP

EIAJ Package Code	JEDEC Code	Weight(g)
* DIP032-P-0300	—	

Scale : 2/1







Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	—	—	4.75
A_1	0.51	—	—
A_2	—	3.65	—
b	0.4	0.5	0.6
b_1	1.1	1.2	1.5
b_2	0.9	1.0	1.3
c	0.2	0.25	0.32
D	39.56	39.76	39.96
E	6.75	6.9	7.05
e	—	2.54	—
e_1	—	7.62	—
L	3.0	—	—
θ	0°	—	15°

MITSUBISHI ELECTRIC

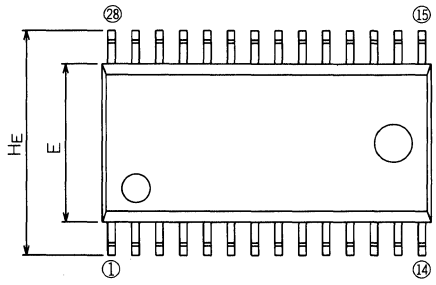
PACKAGE OUTLINES

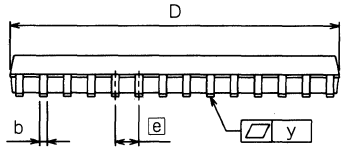
28P2W-C

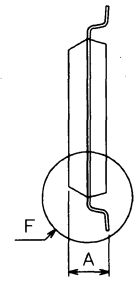
Plastic 28pin 450mil SOP

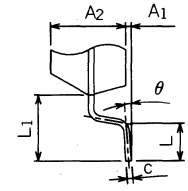
EIAJ Package Code	JEDEC Code	Weight(g)
*SOP028-P-0450	–	0.58

Scale : 2.5/1

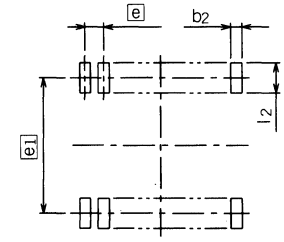








Detail F



Recommended Mount Pad

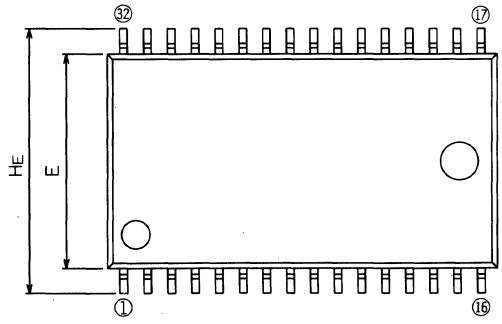
Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	2.4
A_1	0.05	–	–
A_2	–	2.0	–
b	0.35	0.4	0.5
c	0.13	0.15	0.2
D	17.3	17.5	17.7
E	8.2	8.4	8.6
e	–	1.27	–
H_E	11.63	11.93	12.23
L	0.8	1.0	1.2
L_1	–	1.765	–
y	–	–	0.15
θ	0°	–	10°
b_2	–	0.76	–
e1	–	10.58	–
l_2	1.75	–	–

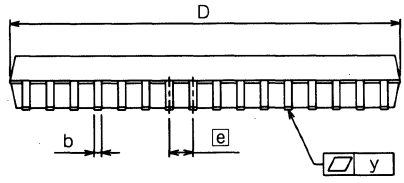
32P2M-A

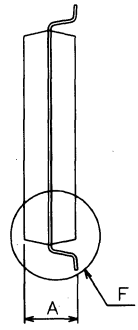
Plastic 32pin 525mil SOP

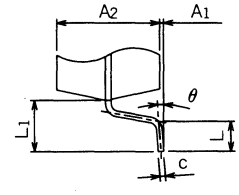
EIAJ Package Code	JEDEC Code	Weight(g)
*SOP032-P-0525	–	1.29

Scale : 2.5/1

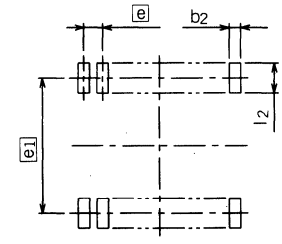








Detail F



Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	3.05
A_1	0	0.1	0.2
A_2	–	2.75	–
b	0.35	0.4	0.5
c	0.13	0.15	0.2
D	20.55	20.75	20.95
E	11.3	11.4	11.5
e	–	1.27	–
H_E	13.8	14.1	14.4
L	0.6	0.8	1.0
L_1	–	1.35	–
y	–	–	0.15
θ	0°	–	8°
b_2	–	0.76	–
e1	–	13.34	–
l_2	1.27	–	–

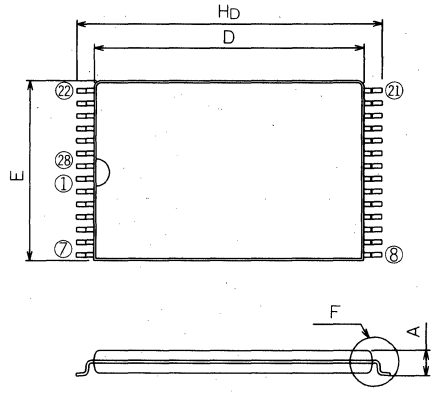
PACKAGE OUTLINES

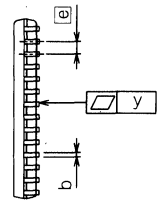
28P2C-A

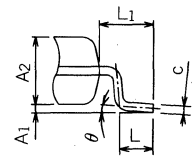
Plastic 28pin 8×13.4mm TSOP(I)

EIAJ Package Code	JEDEC Code	Weight(g)
—	—	0.23

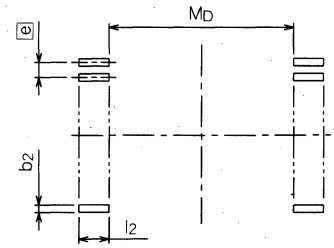
Scale : 3/1







Detail F



Recommended Mount Pad

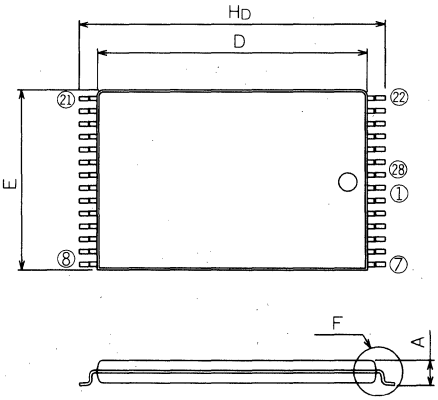
Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	—	—	1.2
A_1	0	0.05	0.15
A_2	—	1.0	—
b	0.15	0.2	0.3
c	0.13	0.15	0.2
D	11.7	11.8	11.9
E	7.9	8.0	8.1
e	—	0.55	—
H_D	13.1	13.4	13.7
L	0.4	0.5	0.6
L_1	—	0.8	—
y	—	—	0.1
θ	0°	—	10°
b_2	—	0.25	—
l_2	0.9	—	—
M_D	—	12.0	—

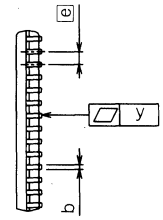
28P2C-B

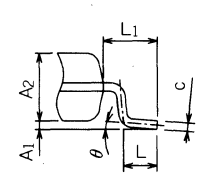
Plastic 28pin 8×13.4mm TSOP(I)

EIAJ Package Code	JEDEC Code	Weight(g)
—	—	0.23

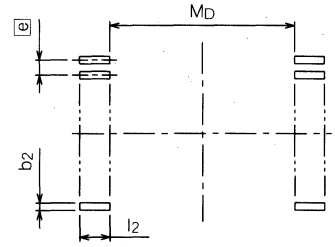
Scale : 3/1







Detail F



Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	—	—	1.2
A_1	0	0.05	0.15
A_2	—	1.0	—
b	0.15	0.2	0.3
c	0.13	0.15	0.2
D	11.7	11.8	11.9
E	7.9	8.0	8.1
e	—	0.55	—
H_D	13.1	13.4	13.7
L	0.4	0.5	0.6
L_1	—	0.8	—
y	—	—	0.1
θ	0°	—	10°
b_2	—	0.25	—
l_2	0.9	—	—
M_D	—	12.0	—

MITSUBISHI ELECTRIC

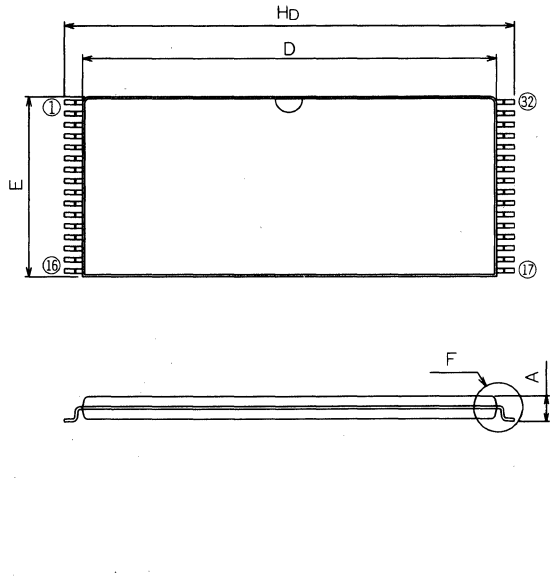
PACKAGE OUTLINES

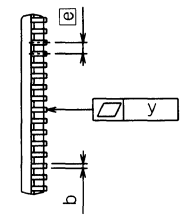
32P3H-E

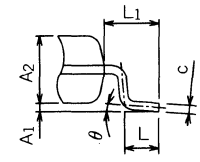
Plastic 32pin 8×20mm TSOP(I)

EIAJ Package Code	JEDEC Code	Weight(g)
TSOP32-P-0820	—	0.37

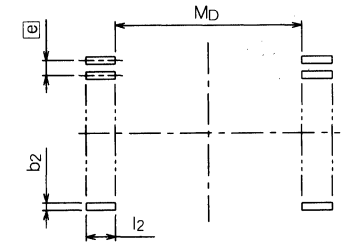
Scale : 3/1







Detail F



Recommended Mount Pad

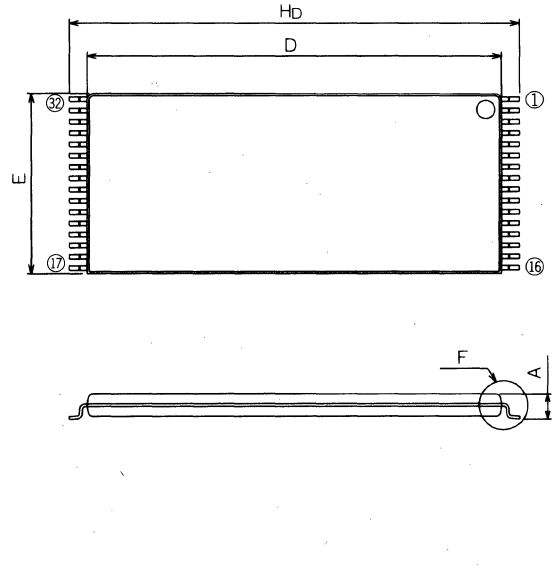
Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	—	—	1.2
A_1	0.05	0.125	0.2
A_2	—	1.0	—
b	0.15	0.2	0.3
c	0.105	0.125	0.175
D	18.3	18.4	18.5
E	7.9	8.0	8.1
e	—	0.5	—
H_D	19.8	20.0	20.2
L	0.4	0.5	0.6
L_1	—	0.8	—
y	—	—	0.1
θ	0°	—	10°
b_2	—	0.225	—
l_2	0.9	—	—
M_D	—	18.6	—

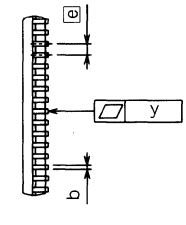
32P3H-F

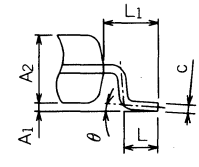
Plastic 32pin 8×20mm TSOP(I)

EIAJ Package Code	JEDEC Code	Weight(g)
TSOP32-P-0820	—	0.37

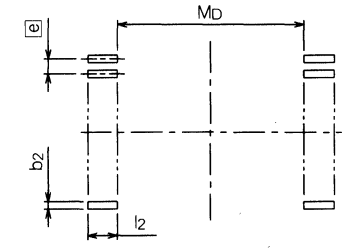
Scale : 3/1







Detail F



Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	—	—	1.2
A_1	0.05	0.125	0.2
A_2	—	1.0	—
b	0.15	0.2	0.3
c	0.105	0.125	0.175
D	18.3	18.4	18.5
E	7.9	8.0	8.1
e	—	0.5	—
H_D	19.8	20.0	20.2
L	0.4	0.5	0.6
L_1	—	0.8	—
y	—	—	0.1
θ	0°	—	10°
b_2	—	0.225	—
l_2	0.9	—	—
M_D	—	18.6	—

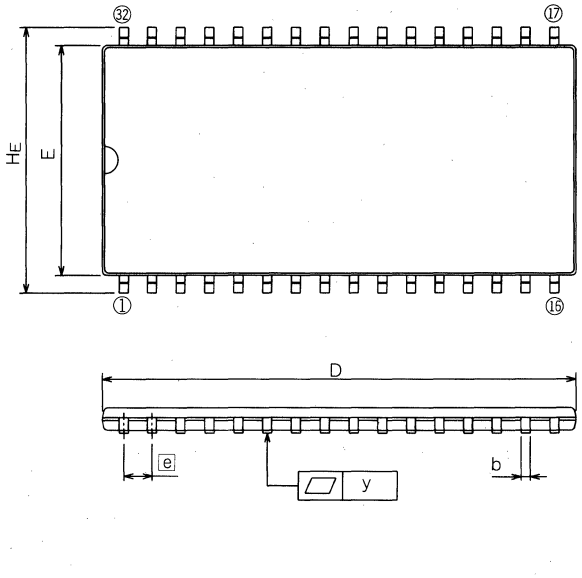
PACKAGE OUTLINES

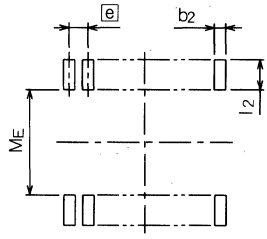
32P3Y-H

Plastic 32pin 400mil TSOP(II)

EIAJ Package Code	JEDEC Code	Weight(g)
TSOP032-P-0400	—	0.53

Scale : 3/1





Recommended Mount Pad

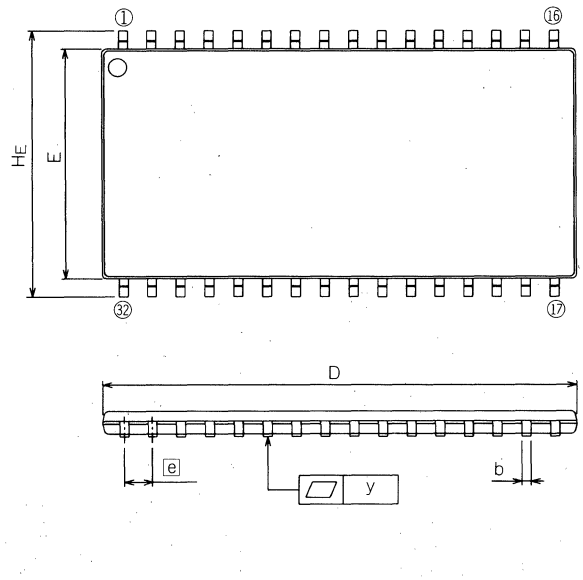
Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	—	—	1.2
A_1	0.05	0.125	0.2
A_2	—	1.0	—
b	0.35	0.4	0.5
c	0.105	0.125	0.175
D	20.85	20.95	21.05
E	10.06	10.16	10.26
e	—	1.27	—
H_E	11.56	11.76	11.96
L	0.4	0.5	0.6
L_1	—	0.8	—
y	—	—	0.1
θ	0°	—	10°
M_E	—	10.36	—
l_2	0.9	—	—
b_2	—	0.76	—

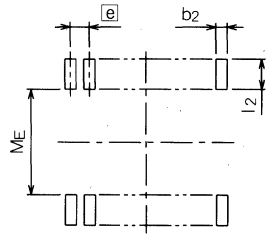
32P3Y-J

Plastic 32pin 400mil TSOP(II)

EIAJ Package Code	JEDEC Code	Weight(g)
TSOP032-P-0400	—	0.53

Scale : 3/1





Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	—	—	1.2
A_1	0.05	0.125	0.2
A_2	—	1.0	—
b	0.35	0.4	0.5
c	0.105	0.125	0.175
D	20.85	20.95	21.05
E	10.06	10.16	10.26
e	—	1.27	—
H_E	11.56	11.76	11.96
L	0.4	0.5	0.6
L_1	—	0.8	—
y	—	—	0.1
θ	0°	—	10°
M_E	—	10.36	—
l_2	0.9	—	—
b_2	—	0.76	—

MITSUBISHI ELECTRIC

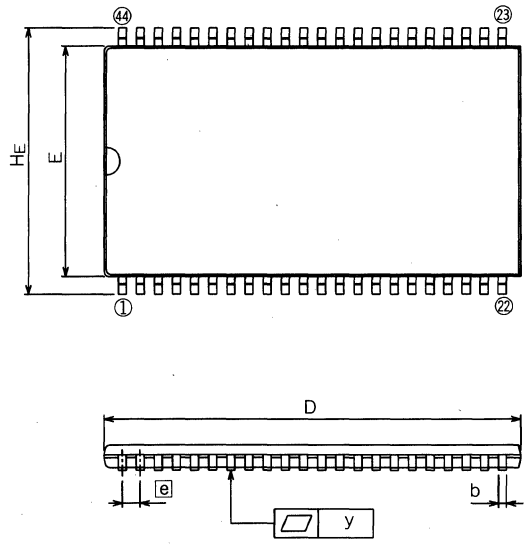
PACKAGE OUTLINES

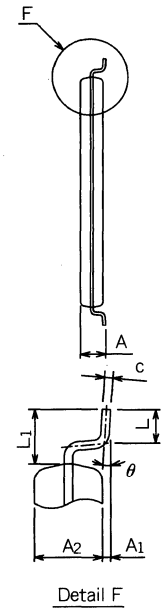
44P3W-H

Plastic 44pin 400mil TSOP(II)

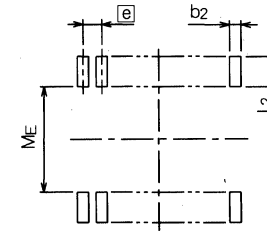
EIAJ Package Code	JEDEC Code	Weight(g)
TSOP044-P-0400	—	0.47

Scale : 3/1





Detail F



Recommended Mount Pad

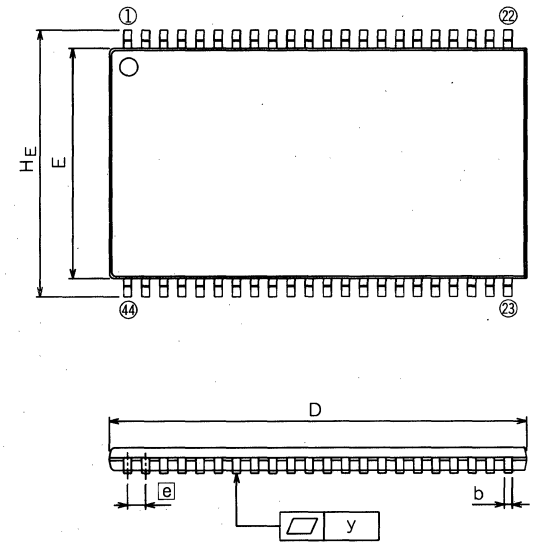
Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	—	—	1.2
A_1	0.05	0.125	0.2
A_2	—	1.0	—
b	0.3	0.35	0.45
c	0.105	0.125	0.175
D	18.31	18.41	18.51
E	10.06	10.16	10.26
e	—	0.8	—
H_E	11.56	11.76	11.96
L	0.4	0.5	0.6
L_1	—	0.8	—
y	—	—	0.1
θ	0°	—	10°
M_E	—	10.36	—
l_2	0.9	—	—
b_2	—	0.5	—

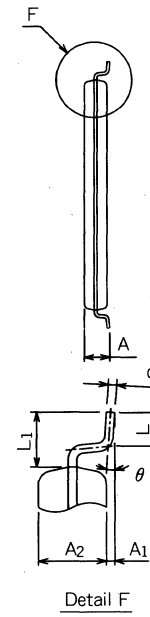
44P3W-J

Plastic 44pin 400mil TSOP(II)

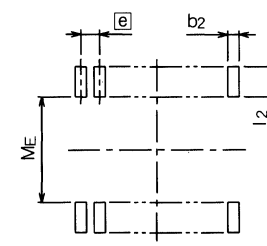
EIAJ Package Code	JEDEC Code	Weight(g)
TSOP044-P-0400	—	0.47

Scale : 3/1





Detail F



Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	—	—	1.2
A_1	0.05	0.125	0.2
A_2	—	1.0	—
b	0.3	0.35	0.45
c	0.105	0.125	0.175
D	18.31	18.41	18.51
E	10.06	10.16	10.26
e	—	0.8	—
H_E	11.56	11.76	11.96
L	0.4	0.5	0.6
L_1	—	0.8	—
y	—	—	0.1
θ	0°	—	10°
M_E	—	10.36	—
l_2	0.9	—	—
b_2	—	0.5	—

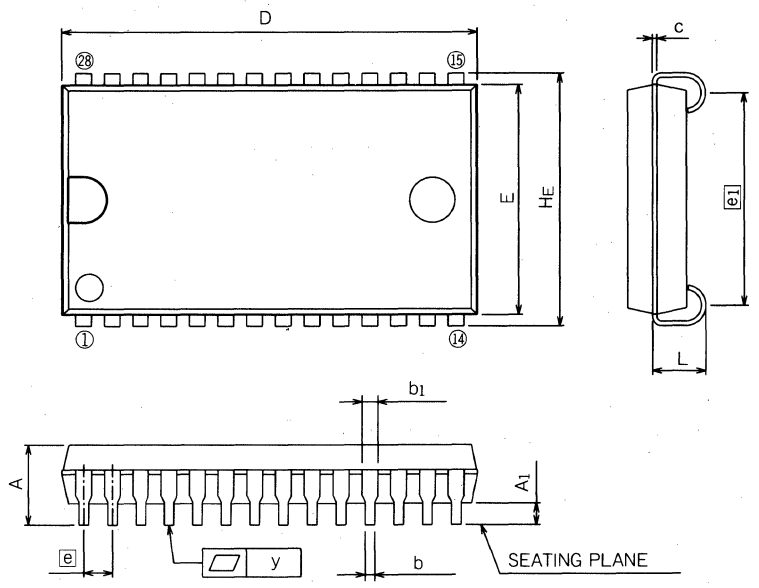
PACKAGE OUTLINES

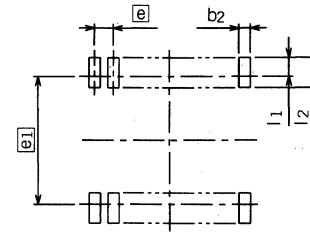
28P0K

Plastic 28pin 400mil SOJ

EIAJ Package Code	JEDEC Code	Weight(g)
*SOJ028-P-0400	MO-061AA	1.08

Scale : 3/1





Recommended Mount Pad

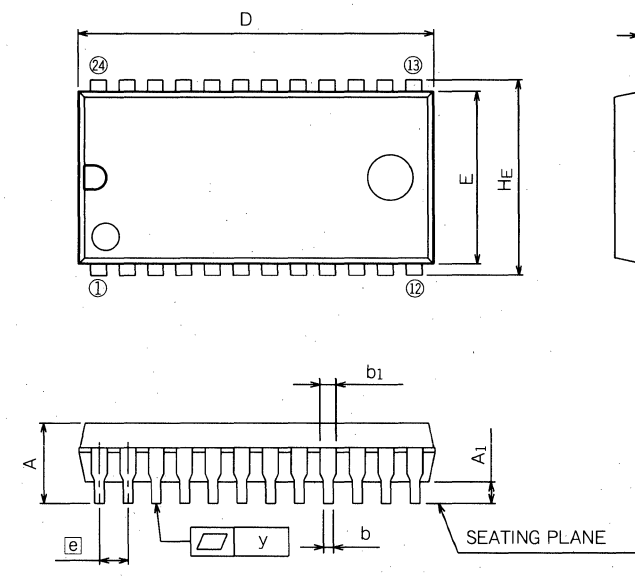
Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	3.35	3.45	3.55
A_1	0.8	—	—
b	0.38	0.43	0.5
b_1	0.66	0.7	0.81
c	0.18	0.2	0.25
D	18.28	18.41	18.54
E	10.03	10.16	10.29
e	—	1.27	—
e1	9.27	9.4	9.53
H_E	11.05	11.18	11.31
L	2.25	2.35	2.45
y	—	—	0.1
b_2	—	0.75	—
l_1	—	1.2	—
l_2	2.0	—	—

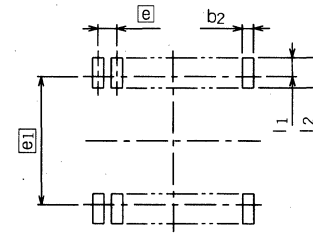
24P0J

Plastic 24pin 300mil SOJ

EIAJ Package Code	JEDEC Code	Weight(g)
*SOJ024-P-0300	—	0.68

Scale : 3/1





Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	3.35	3.45	3.55
A_1	0.8	—	—
b	0.38	0.43	0.5
b_1	0.66	0.7	0.81
c	0.18	0.2	0.25
D	15.74	15.87	16.0
E	7.52	7.62	7.72
e	—	1.27	—
e1	6.73	6.86	6.99
H_E	8.35	8.45	8.55
L	2.25	2.35	2.45
y	—	—	0.1
b_2	—	0.75	—
l_1	—	1.2	—
l_2	2.0	—	—

MITSUBISHI ELECTRIC

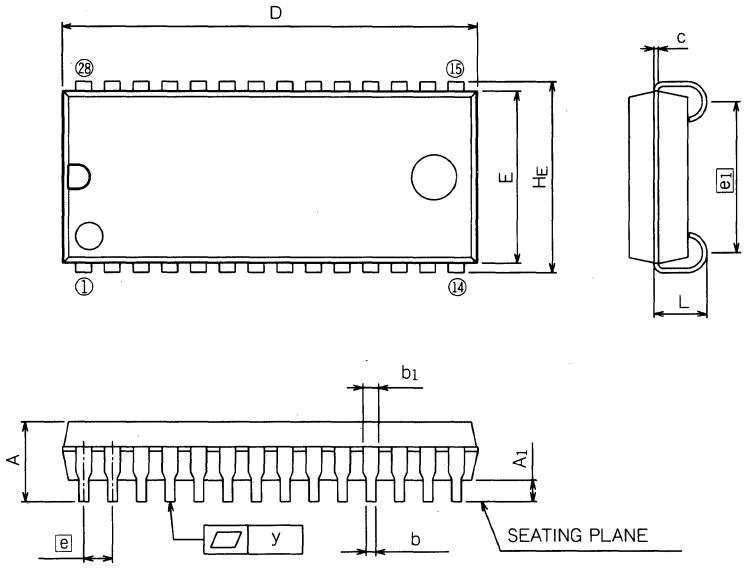
PACKAGE OUTLINES

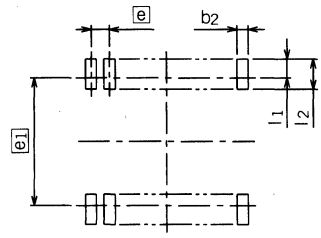
28P0J

Plastic 28pin 300mil SOJ

EIAJ Package Code	JEDEC Code	Weight(g)
*SOJ028-P-0300	—	0.81

Scale : 3/1





Recommended Mount Pad

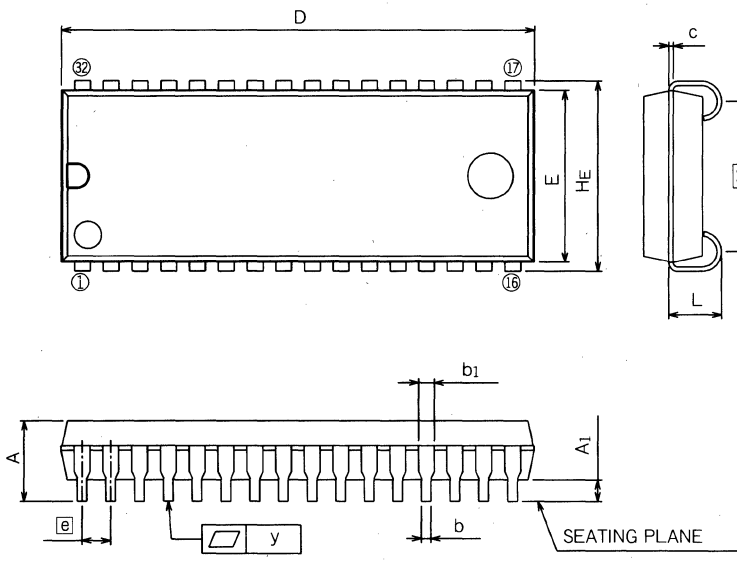
Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	3.35	3.45	3.55
A_1	0.8	—	—
b	0.38	0.43	0.5
b_1	0.66	0.7	0.81
c	0.18	0.2	0.25
D	18.28	18.41	18.54
E	7.52	7.62	7.72
e	—	1.27	—
e_1	6.73	6.86	6.99
H_E	8.35	8.45	8.55
L	2.25	2.35	2.45
y	—	—	0.1
b_2	—	0.75	—
l_1	—	1.2	—
l_2	2.0	—	—

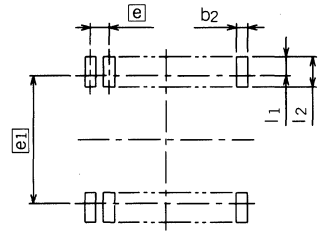
32P0J

Plastic 32pin 300mil SOJ

EIAJ Package Code	JEDEC Code	Weight(g)
*SOJ032-P-0300	—	1.03

Scale : 3/1





Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	3.35	3.45	3.55
A_1	0.8	—	—
b	0.38	0.43	0.5
b_1	0.66	0.7	0.81
c	0.18	0.2	0.25
D	20.82	20.95	21.08
E	7.52	7.62	7.72
e	—	1.27	—
e_1	6.73	6.86	6.99
H_E	8.35	8.45	8.55
L	2.25	2.35	2.45
y	—	—	0.1
b_2	—	0.75	—
l_1	—	1.2	—
l_2	2.0	—	—

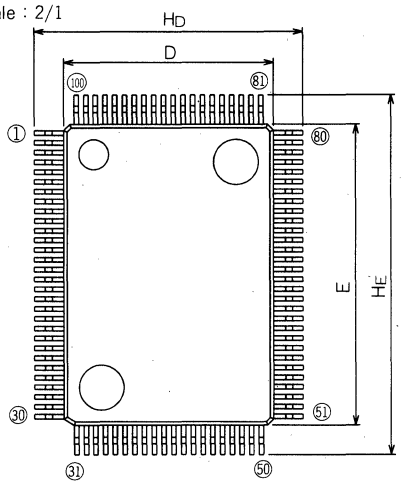
PACKAGE OUTLINES

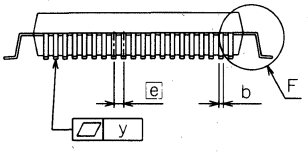
100P6S-C

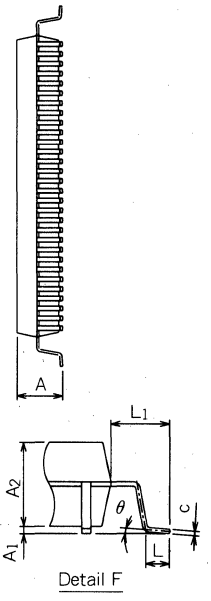
Plastic 100pin 14×20mm body QFP

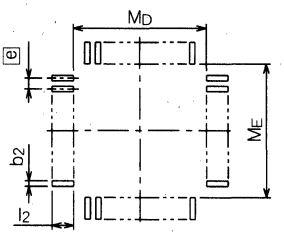
EIAJ Package Code	JEDEC Code	Weight(g)
*QFP100-P-1420	–	1.58

Scale : 2/1









Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	3.3
A_1	0.2	0.35	0.5
A_2	–	2.8	–
b	0.25	0.3	0.4
c	0.13	0.15	0.2
D	13.8	14.0	14.2
E	19.8	20.0	20.2
e	–	0.65	–
H_D	17.6	17.9	18.2
H_E	23.6	23.9	24.2
L	0.6	0.8	1.0
L_1	–	1.95	–
y	–	–	0.1
θ	0°	–	10°
b_2	–	0.35	–
l_2	1.5	–	–
M_D	–	15.3	–
M_E	–	21.3	–

MITSUBISHI ELECTRIC

SHIPMENT FORMS ACCORDING TO IC TYPES

Type name	Package outline	Shipment forms		
		Tube	Pallet	Tape & Reel
M5M5255BP M5M5256BP M5M5255CP M5M5256CP	28P4 (DIP) 28P4 (DIP) 28P4 (DIP) 28P4 (DIP)	○ ○ ○ ○		
M5M5255BKP M5M5256BKP M5M5255CKP M5M5256CKP	28P4Y (DIP) 28P4Y (DIP) 28P4Y (DIP) 28P4Y (DIP)	○ ○ ○ ○		
M5M5255BFP M5M5256BFP M5M5255CFP M5M5256CFP	28P2W-C (SOP) 28P2W-C (SOP) 28P2W-C (SOP) 28P2W-C (SOP)	○ ○ ○ ○		○ ○ ○ ○
M5M5256BVP, RV M5M5256CVP, RV	28P2C (TSOP) 28P2C (TSOP)		○ ○	○ ○
M5M51008AP M5M51T08AP M5M51008BP	32P4 (DIP) 32P4 (DIP) 32P4 (DIP)	○ ○ ○		
M5M51008AFP M5M51T08AFP M5M51008BFP	32P2M-A (SOP) 32P2M-A (SOP) 32P2M-A (SOP)	○ ○ ○		○ ○ ○
M5M51008AVP, RV M5M51T08AVP, RV M5M51008BVP, RV	32P3H (TSOP) 32P3H (TSOP) 32P3H (TSOP)		○ ○ ○	○ ○ ○
M5M51016ATP, RT M5M51016BTP, RT	44P3W (TSOP) 44P3W (TSOP)		○ ○	○ ○
M5M5408FP M5M5408AFP	32P2M-A (SOP) 32P2M-A (SOP)	○ ○		○ ○
M5M5408TP, RT M5M5408ATP, RT	32P3Y (TSOP) 32P3Y (TSOP)		○ ○	○ ○

※High-Speed SRAMs are shipped in tubes.

PRECAUTIONS IN HANDLING MOS ICs/LSIs

A MOS transistor has a very thin oxide insulator under the gate electrode on the silicon substrate. It is operated by altering the conductance (g_m) between source and drain to control mobile charges in the channel formed by the applied gate voltage.

If a high voltage were applied to a gate terminal, the insulator-film under the gate electrode could be destroyed, and all Mitsubishi MOS IC/LSIs contain internal protection circuits at each input terminal to prevent this. It is inherently necessary to apply reverse bias to the P-N junctions of a MOS IC/LSI.

Under certain conditions, however, it may be impossible to completely avoid destruction of the thin insulator-film due to the application of unexpectedly high voltage or thermal destruction due to excessive current from a forward biased P-N junction. The following recommendations should be followed in handling MOS devices.

1. KEEPING VOLTAGE AND CURRENT TO EACH TERMINAL BELOW MAXIMUM RATINGS

1. The recommended ranges of operating conditions provide adequate safety margins. Operating within these limits will assure maximum equipment performance and quality.
2. Forward bias should not be applied to any terminal since excessive current may cause thermal destruction.
3. Output terminals should not be connected directly to the power supply. Short-circuiting of a terminal to a power supply having low impedance may cause burn-out of the internal leads or thermal destruction due to excessive current.

2. KEEPING ALL TERMINALS AT THE SAME POTENTIAL DURING TRANSPORT AND STORAGE

When MOS IC/LSIs are not in use, both input and output terminals can be in a very high impedance state so that they are easily subjected to electrostatic induction from AC fields of the surrounding space or from charged objects in their vicinity. For this reason, MOS IC/LSIs should be protected from electrostatic charges while being transported and stored by conductive rubber foam, aluminum foil, shielded boxes or other protective precautions.

3. KEEPING ELECTRICAL EQUIPMENT, WORK TABLES AND OPERATING PERSONNEL AT THE SAME POTENTIAL

1. All electric equipment, work table surfaces and operating personnel should be grounded. Work tables should be covered with copper or aluminum plates of good conductivity, and grounded. One method of grounding personnel, after making sure that there is no potential difference with electrical equipment, is by the use of a wristwatch metallic ring, etc. attached around the wrist and grounded in series with a 1MΩ resistor. Be sure that the grounding meets national regulations on personnel safety.
2. Current leakage from electric equipment must be prevented not only for personnel safety, but also to avert the destruction of MOS IC/LSIs, as described above. Items such as testers, curve-tracers and synchro-scopes must be checked for current leakage before being grounded.

4. PRECAUTIONS FOR MOUNTING OF MOS IC/LSIs

1. The printed wiring lines to input and output terminals of MOS IC/LSIs should not be close to or parallel to high-voltage or high-power signal lines. Turning power on while the device is short-circuited, either by a solder bridge made during assembly or by a probe during adjusting and testing, may cause maximum ratings to be exceeded, which may result in the destruction of the device.
2. When input/output, or input and/or output, terminals of MOS IC/LSIs (now open-circuits) are connected, we must consider the possibility of current leakage and take precautions similar to § 2 above. To reduce such undesirable trouble, it is recommended that an interface circuit be inserted at the input or output terminal, or a resistor with a resistance that does not exceed the output driving capability of the MOS IC/LSI be inserted between the power supply and the ground.
3. A filter circuit should be inserted in the AC power supply line to absorb surges which can frequently be strong enough to destroy a MOS IC/LSI.
4. Terminal connections should be made as described in the catalog while being careful to meet specifications.
5. Ungrounded metal plates should not be placed near input or output terminals of any MOS IC/LSIs, since destruction of the insulation may result if they become electrostatically charged.
6. Equipment cases should provide shielding from electrostatic charges for more reliable operation. When a plastic case is used, it is desirable to coat the inside of the case with conductive paint and to ground it. This is considered necessary even for battery-operated equipment.

LOW POWER DISSIPATION SRAM

(5V Version)

2

M5M5255BP,FP,KP-70,-85,-10,-12,-70L,-85L, -10L,-12L,-70LL,-85LL,-10LL,-12LL

262144-BIT (32768-WORD BY 8-BIT) CMOS STATIC RAM

DESCRIPTION

The M5M5255BP, FP, KP is a 262144-bit CMOS static RAM organized as 32768-words by 8-bits which is fabricated using high-performance double polysilicon CMOS technology. The use of resistive load NMOS cells and CMOS periphery result in a high-density and low-power static RAM.

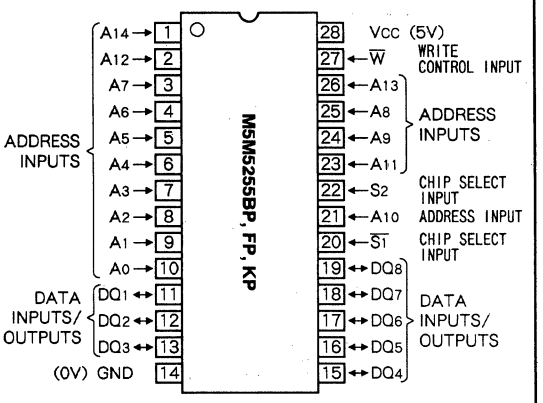
The M5M5255BP, FP, KP provides two chip select input ($\overline{S_1}$, S_2). It is ideal for battery back up application.

FEATURES

Type name	Access time (max)	Power supply current	
		Active (max)	Stand-by (max)
M5M5255BP, FP, KP-70 M5M5255BP, FP, KP-85 M5M5255BP, FP, KP-10 M5M5255BP, FP, KP-12	70ns 85ns 100ns 120ns	70mA	2mA
M5M5255BP, FP, KP-70L M5M5255BP, FP, KP-85L M5M5255BP, FP, KP-10L M5M5255BP, FP, KP-12L	70ns 85ns 100ns 120ns		100μA (Vcc = 5.5V) 50μA (Vcc = 3.0V)
M5M5255BP, FP, KP-70LL M5M5255BP, FP, KP-85LL M5M5255BP, FP, KP-10LL M5M5255BP, FP, KP-12LL	70ns 85ns 100ns 120ns		20μA (Vcc = 5.5V) 10μA (Vcc = 3.0V)

- Single +5V power supply
- No clocks, no refresh
- Data-hold on +2V power supply
- Directly TTL compatible : All inputs and outputs
- Three-state outputs : OR-tie capability
- Simple memory expansion by $\overline{S_1}$, S_2
- Common data I/O

PIN CONFIGURATION (TOP VIEW)



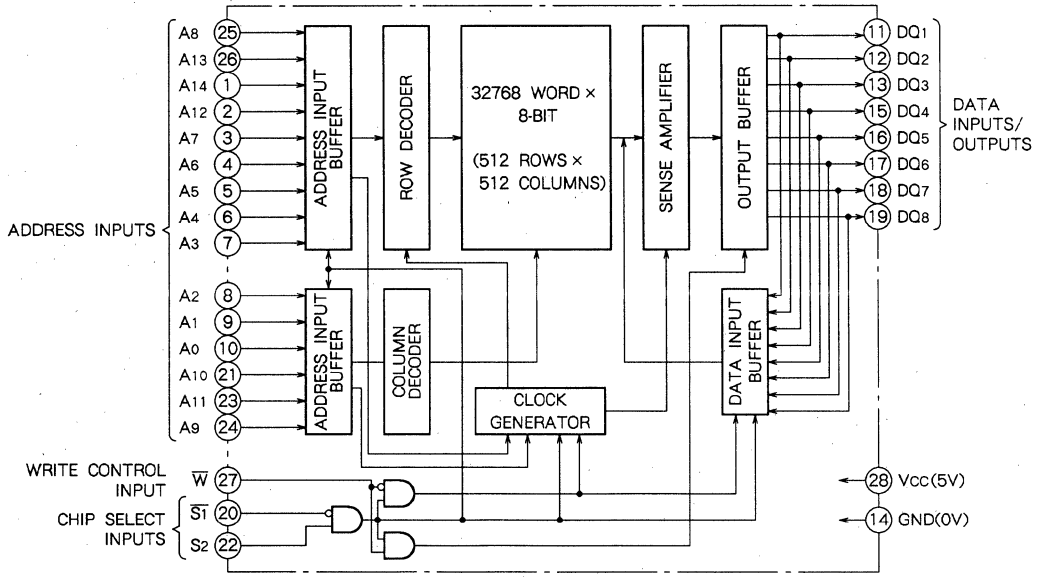
Outline 28P4(P)
28P2W-C(FP)
28P4Y(KP)

- Package
  - M5M5255BP ..... 28pin 600mil DIP
  - M5M5255BKP ..... 28pin 300mil DIP
  - M5M5255BFP ..... 28pin small outline package(SOP)

APPLICATION

Small capacity memory units

BLOCK DIAGRAM



M5M5255BP,FP,KP-70,-85,-10,-12,-70L,-85L, -10L,-12L,-70LL,-85LL,-10LL,-12LL

262144-BIT (32768-WORD BY 8-BIT) CMOS STATIC RAM

FUNCTION

The operation mode of the M5M5255BP, FP, KP is determined by a combination of the device control inputs $\overline{S_1}$, S_2, and $\overline{W}$. Each mode is summarized in the function table.

A write cycle is executed whenever the low level $\overline{W}$ overlaps with the low level $\overline{S_1}$ and the high level S_2. The address must be set up before the write cycle and must be stable during the entire cycle. The data is latched into a cell on the trailing edge of $\overline{W}$, $\overline{S_1}$ or S_2, whichever occurs first, requiring the set-up and hold time relative to these edge to be maintained.

A read cycle is executed by setting $\overline{W}$ at a high level while $\overline{S_1}$ and S_2 are in an active state($\overline{S_1}$ = L, S_2 = H)

When setting $\overline{S_1}$ at a high level or S_2 at a low level, the chip is in a non-selectable mode in which both reading and writing are disabled. In this mode, the output stage is in a high-impedance state, allowing OR-tie with other chips and memory expansion by $\overline{S_1}$ and S_2. The power supply current is reduced as low as the stand-by current which is specified as I_{CC3} or I_{CC4}, and the memory data can be held + 2V power supply, enabling battery back-up operation during power failure or power-down operation in the non-selected mode.

FUNCTION TABLE

$\overline{S_1}$	S_2	$\overline{W}$	Mode	DQ	Icc
H	X	X	Non selection	High-impedance	Stand-by
X	L	X	Non selection	High-impedance	Stand-by
L	H	L	Write	Din	Active
L	H	H	Read	Dout	Active

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to GND	− 0.3 ~7	V
V_I	Input voltage		− 0.3 ~V_{CC} + 0.3	V
V_O	Output voltage		0 ~V_{CC}	V
T_{opr}	Operating temperature	T_a = 25℃	0~70	℃
T_{stg}	Storage temperature		− 65~150	℃

ELECTRICAL CHARACTERISTICS (T_a = 0~70℃, V_{CC} = 5V ± 10%, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits Min	Limits Typ	Limits Max	Unit
V_{IH}	High input voltage			2.2		V_{CC}+0.3	V
V_{IL}	Low input voltage			− 0.3		0.8	V
V_{OH}	High output voltage	I_{OH} = − 1mA		2.4			V
V_{OL}	Low output voltage	I_{OL} = 2mA				0.4	V
I_I	Input leakage current	V_I = 0~V_{CC}				± 1	μA
I_O	Output leakage current	$\overline{S_1}$ = V_{IH} or S_2 = V_{IL}, $V_{I/O}$ = 0~V_{CC}				± 1	μA
I_{CC1}	Active supply current(AC MOS level)	$\overline{S_1}$ <0.2, S_2 >V_{CC} − 0.2 output open, Other inputs < 0.2 or > V_{CC} − 0.2, Min cycle			30	65	mA
I_{CC2}	Active supply current(AC TTL level)	$\overline{S_1}$ = V_{IL} or S_2 = V_{IH} output open, Other inputs = V_{IL} or V_{IH}, Min cycle			35	70	mA
I_{CC3}	Stand by supply current	1). S_2 ≦ 0.2V, Other inputs = 0~V_{CC}	BP,FP,KP			2	mA
		2). $\overline{S_1}$ ≧ V_{CC} − 0.2V, S_2 ≧ V_{CC} − 0.2V, Other inputs = 0~V_{CC}	BP,FP,KP-L			100	μA
			BP,FP,KP-LL			20	μA
I_{CC4}	Stand by supply current	1). S_2 = V_{IL} 2). $\overline{S_1}$ = V_{IH}, S_2 = V_{IH}, Other inputs = 0~V_{CC}				3	mA
C_I	Input capacitance (T_a = 25℃)	V_I = GND, V_I = 25mVrms, f = 1MHz				6	pF
C_O	Output capacitance (T_a = 25℃)	V_O = GND, V_O = 25mVrms, f = 1MHz				8	pF

Note 1. Direction for current flowing into IC is indicated as positive (no mark)
2. Typical value is V_{CC} = 5V, T_a = 25℃

SWITCHING CHARACTERISTICS (T_a = 0~70℃, V_{CC} = 5V ± 10%, unless otherwise noted)

Read cycle

Symbol	Parameter	Limits												Unit
		M5M5255-70 M5M5255-70L M5M5255-70LL			M5M5255-85 M5M5255-85L M5M5255-85LL			M5M5255-10 M5M5255-10L M5M5255-10LL			M5M5255-12 M5M5255-12L M5M5255-12LL			
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{CR}	Read cycle time	70			85			100			120			ns
$t_{a(A)}$	Address access time			70			85			100			120	ns
$t_{a(S1)}$	Chip select 1 access time			70			85			100			120	ns
$t_{a(S2)}$	Chip select 2 access time			70			85			100			120	ns
$t_{dis(S1)}$	Output disable time after $\overline{S_1}$ high			30			30			35			40	ns
$t_{dis(S2)}$	Output disable time after S_2 low			30			30			35			40	ns
$t_{en(S1)}$	Output enable time after $\overline{S_1}$ low	5			10			10			10			ns
$t_{en(S2)}$	Output enable time after S_2 high	5			10			10			10			ns
$t_{v(A)}$	Data valid time after address change	20			20			20			20			ns

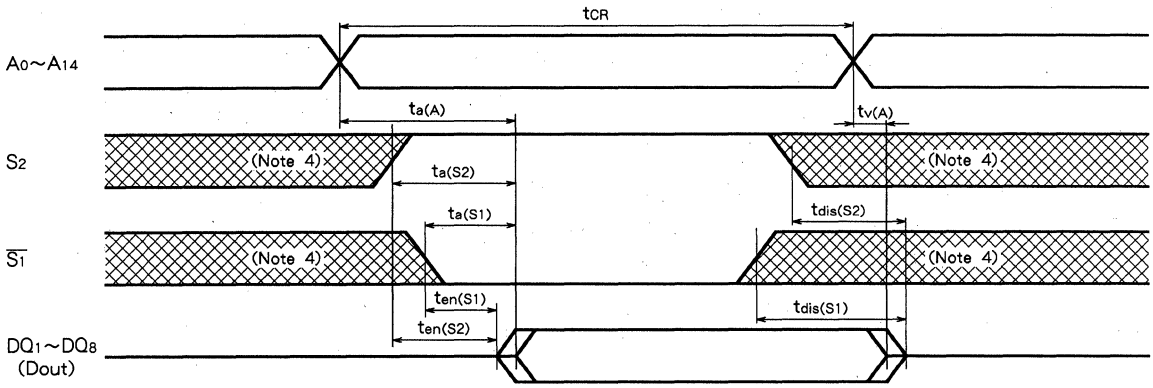
TIMING REQUIREMENTS (T_a = 0~70℃, V_{CC} = 5V ± 10%, unless otherwise noted)

Write cycle

Symbol	Parameter	Limits												Unit
		M5M5255-70 M5M5255-70L M5M5255-70LL			M5M5255-85 M5M5255-85L M5M5255-85LL			M5M5255-10 M5M5255-10L M5M5255-10LL			M5M5255-12 M5M5255-12L M5M5255-12LL			
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{CW}	Write cycle time	70			85			100			120			ns
$t_{w(W)}$	Write pulse width	55			60			60			70			ns
$t_{su(A)}$	Address set up time	0			0			0			0			ns
$t_{su(A-WH)}$	Address set up time with respect to $\overline{W}$ high	65			75			80			85			ns
$t_{su(S1)}$	Chip select set up time	65			75			80			85			ns
$t_{su(S2)}$	Chip select set up time	65			75			80			85			ns
$t_{su(D)}$	Data set up time	30			35			35			40			ns
$t_{h(D)}$	Data hold time	0			0			0			0			ns
$t_{rec(W)}$	Write recovery time	0			0			0			0			ns
$t_{dis(W)}$	Output disable time after $\overline{W}$ low			25			30			35			40	ns
$t_{en(W)}$	Output enable time after $\overline{W}$ high	5			5			10			10			ns

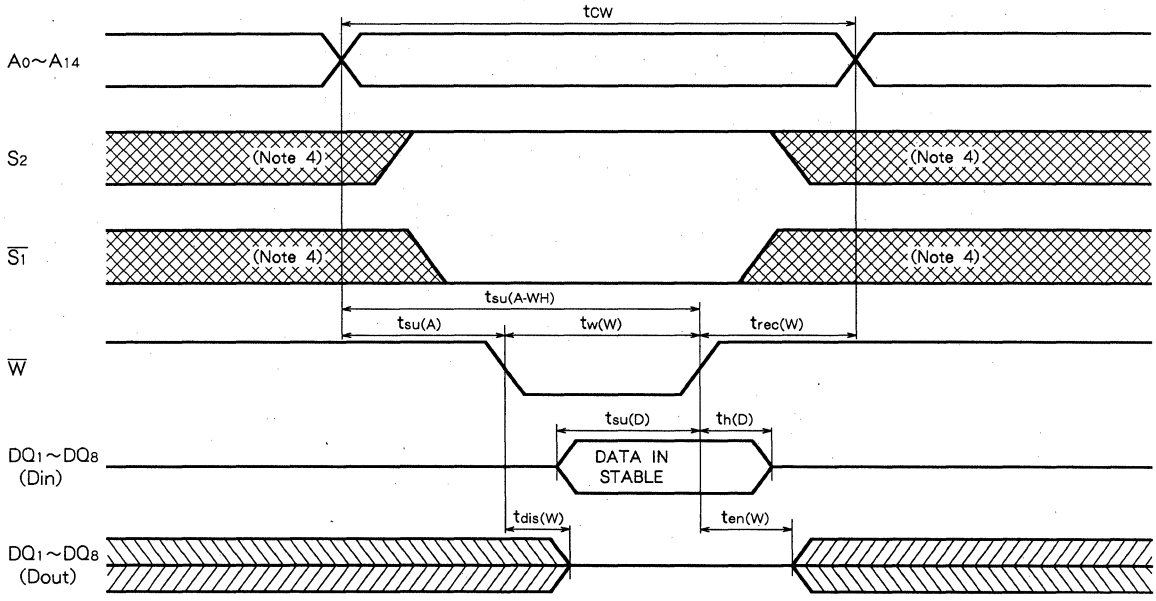
TIMING DIAGRAM

Read cycle

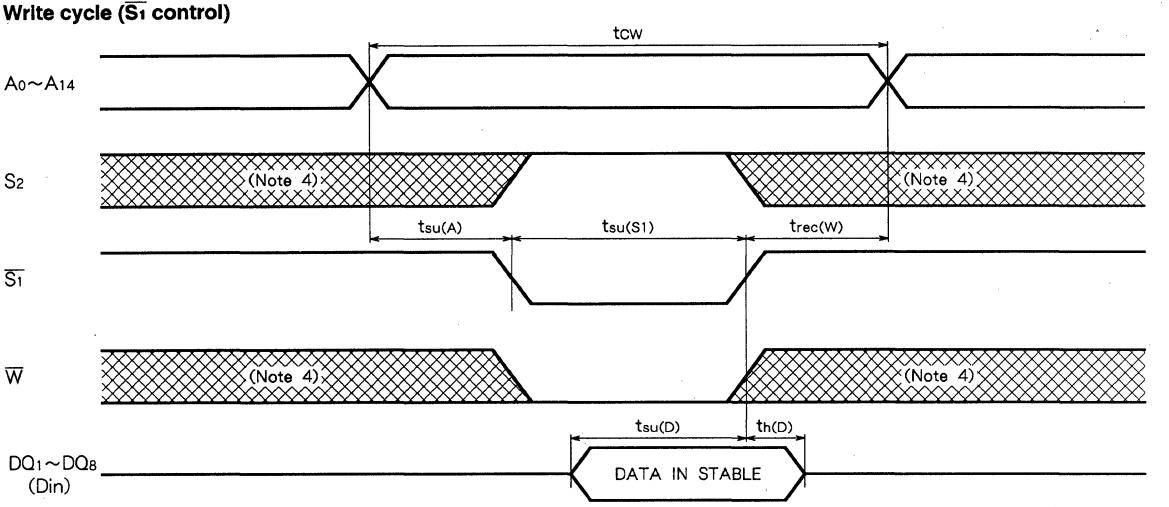


$\overline{W}$ = "H" level

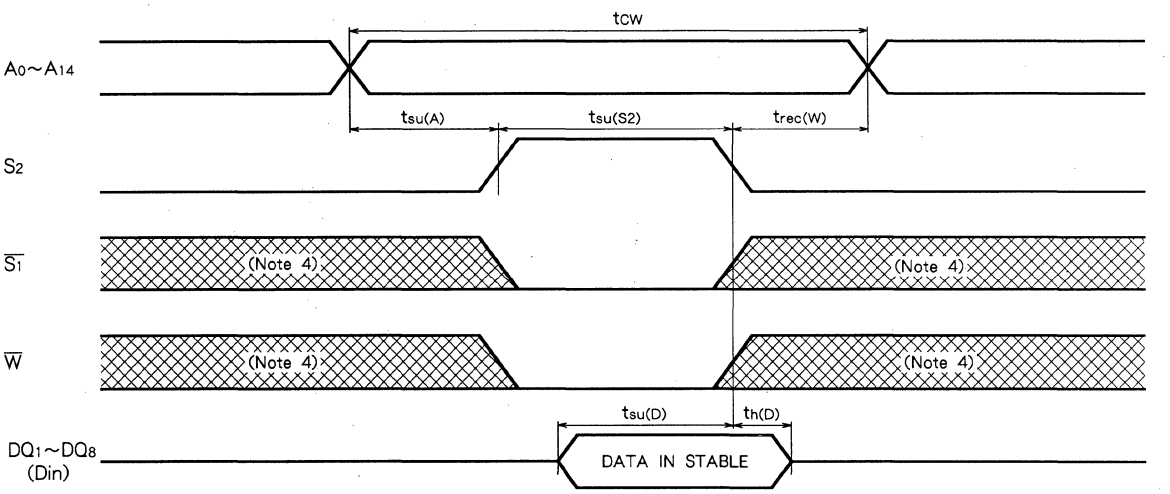
Write cycle ($\overline{W}$ control)



Write cycle ($\overline{S_1}$ control)



Write cycle (S_2 control)



Note 3 : Test condition

Input pulse levels ····· V_{IH} = 2.4V, V_{IL} = 0.6V

Input rise and fall time ····· 10ns

Reference levels ····· $V_{OH} = V_{OL}$ = 1.5V

Transition is measured ±500mV from steady state voltage.(for t_{en}, t_{dis})

Output loads ····· Fig. 1, C_L = 100pF (BP, FP, KP-85, -10, -12, -85L, -10L, -12L, -85LL, -10LL, -12LL)

C_L = 30pF (BP, FP, KP-70, -70L, -70LL)

C_L = 5pF (for t_{en}, t_{dis})

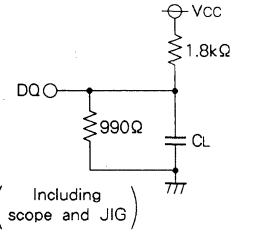


Fig. 1 Output load

Note 4. Hatching indicates the state is don't care.

5. Writing is executed while S2 high overlaps $\overline{S_1}$ and $\overline{W}$ low.
6. If $\overline{W}$ goes low simultaneously with or prior to $\overline{S_1}$ low or S2 high, the output remains in the high-impedance state.
7. Don't apply inverted phase signal externally when DQ pin is in output mode.

POWER DOWN CHARACTERISTICS

ELECTRICAL CHARACTERISTICS (T_a = 0~70℃, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ	Max	
$V_{CC(PD)}$	Power down supply voltage			2			V
$V_{I(\overline{S1})}$	Chip select input $\overline{S1}$	2.2V ≦ $V_{CC(PD)}$		2.2			V
		2V ≦ $V_{CC(PD)}$ ≦ 2.2V			$V_{CC(PD)}$		
$V_{I(S2)}$	Chip select input S_2	4.5V ≦ $V_{CC(PD)}$				0.8	V
		$V_{CC(PD)}$ < 4.5V				0.2	
$I_{CC(PD)}$	Power down supply current	V_{CC}=3V, Other inputs=0~3V 1). S_2≦0.2V 2). $\overline{S1}$ ≧ V_{CC}-0.2V, S_2 ≧ V_{CC}-0.2V	BP, FP, KP			2	mA
			BP, FP, KP-L			50	μA
			BP, FP, KP-LL			10*	μA

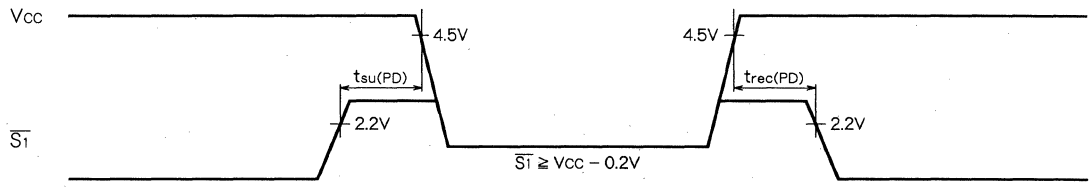
* T_a = 25℃, $I_{CC(PD)}$ = 1 μA

TIMING REQUIREMENTS (T_a = 0~70℃, unless otherwise noted)

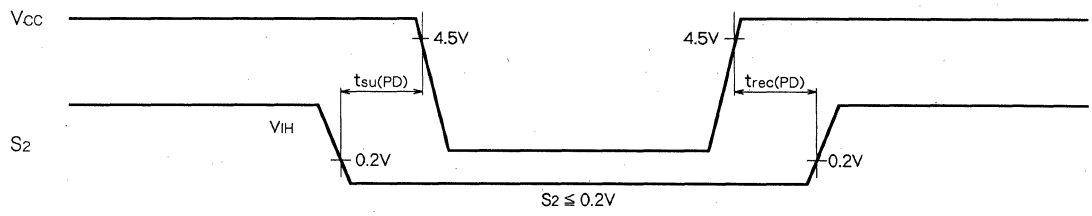
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{su(PD)}$	Power down setup time		0			ns
$t_{rec(PD)}$	Power down recovery time		t_{CR}			ns

POWER DOWN CHARACTERISTICS

$\overline{S1}$ control



S_2 control



M5M5256BP,FP,KP-70,-85,-10,-12,-15,-70L,-85L,-10L,-12L,-15L,-70LL,-85LL,-10LL,-12LL,-15LL

262144-BIT (32768-WORD BY 8-BIT) CMOS STATIC RAM

DESCRIPTION

This M5M5256BP, FP, KP is a 262144-bit CMOS static RAM organized as 32768-words by 8-bits which is fabricated using high-performance double polysilicon CMOS technology. The use of resistive load NMOS cells and CMOS periphery result in a high-density and low-power static RAM. It is ideal for the memory systems which require simple interface.

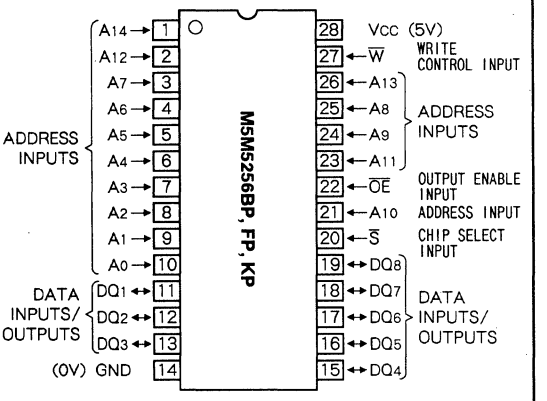
The stand-by current is low enough for a battery back-up application. It is mounted in a standard 28pin package and configured in an industrial standard 32K × 8-bit pinout.

FEATURES

Type name	Access time (max)	Power supply current	
		Active (max)	Stand-by (max)
M5M5256BP, FP, KP-70	70ns	70mA	2mA
M5M5256BP, FP, KP-85	85ns		
M5M5256BP, FP, KP-10	100ns		
M5M5256BP, FP, KP-12	120ns		
M5M5256BP, FP, KP-15	150ns		
M5M5256BP, FP, KP-70L	70ns		100μA (Vcc = 5.5V) 50μA (Vcc = 3.0V)
M5M5256BP, FP, KP-85L	85ns		
M5M5256BP, FP, KP-10L	100ns		
M5M5256BP, FP, KP-12L	120ns		
M5M5256BP, FP, KP-15L	150ns		
M5M5256BP, FP, KP-70LL	70ns		20μA (Vcc = 5.5V) 10μA (Vcc = 3.0V)
M5M5256BP, FP, KP-85LL	85ns		
M5M5256BP, FP, KP-10LL	100ns		
M5M5256BP, FP, KP-12LL	120ns		
M5M5256BP, FP, KP-15LL	150ns		

- Single + 5V power supply
- No clocks, no refresh
- Data-hold on + 2V power supply

PIN CONFIGURATION (TOP VIEW)



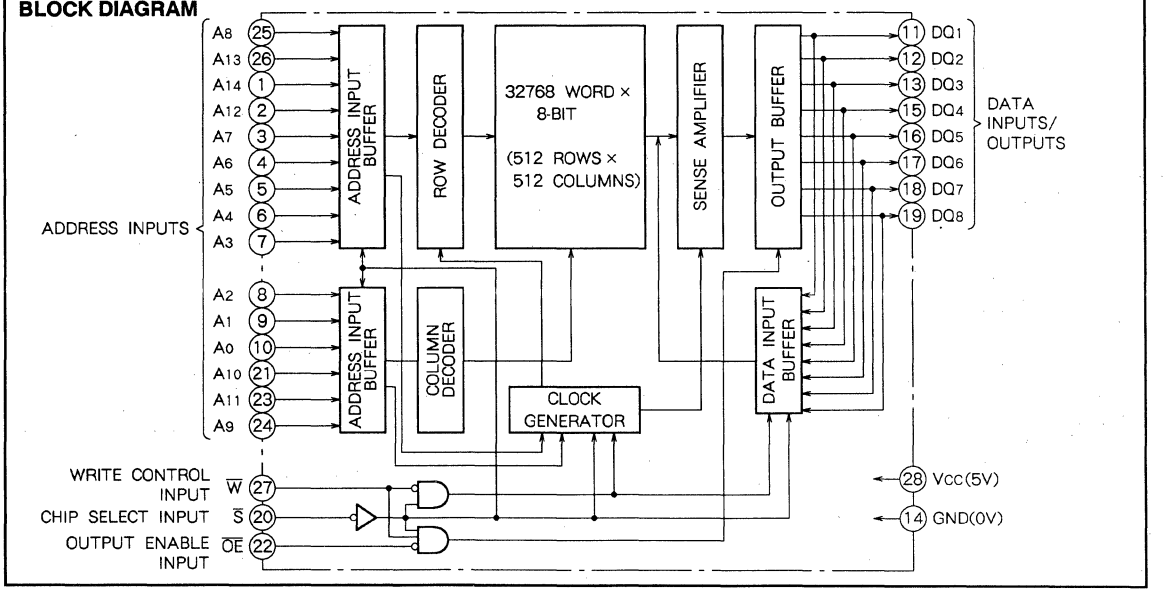
Outline 28P4(P)
28P2W-C(FP)
28P4Y(KP)

- Directly TTL compatible : All inputs and outputs
- Three-state outputs : OR-tie capability
- Simple memory expansion by $\overline{S}$
- $\overline{OE}$ prevents data contention in the I/O bus
- Common data I/O
- Package
  - M5M5256BP ..... 28pin 600mil DIP
  - M5M5256BKP ..... 28pin 300mil DIP
  - M5M5256BFP ..... 28pin small outline package(SOP)

APPLICATION

Small capacity memory units

BLOCK DIAGRAM



M5M5256BP,FP,KP-70,-85,-10,-12,-15,-70L,-85L, -10L,-12L,-15L,-70LL,-85LL,-10LL,-12LL,-15LL

262144-BIT (32768-WORD BY 8-BIT) CMOS STATIC RAM

FUNCTION

The operation mode of the M5M5256BP, FP, KP is determined by a combination of the device control inputs $\overline{S}$, $\overline{W}$ and $\overline{OE}$. Each mode is summarized in the function table.

A write cycle is executed whenever the low level $\overline{W}$ overlaps with the low level $\overline{S}$. The address must be set up before the write cycle and must be stable during the entire cycle. The data is latched into a cell on the trailing edge of $\overline{W}$, $\overline{S}$, whichever occurs first, requiring the set-up and hold time relative to these edge to be maintained. The output enable $\overline{OE}$ directly controls the output stage. Setting the $\overline{OE}$ at a high level, the output stage is in a high-impedance state, and the data bus contention problem in the write cycle is eliminated.

A read cycle is executed by setting $\overline{W}$ at a high level and $\overline{OE}$ at a low level while $\overline{S}$ are in an active state.

When setting $\overline{S}$ at a high level, the chip is in a non-selectable mode in which both reading and writing are disabled. In this mode, the output stage is in a high-impedance state, allowing OR-tie with other chips and memory expansion by $\overline{S}$. The power supply current is reduced as low as the stand-by current which is specified as I_{CC3} or I_{CC4}, and the memory data can be held + 2V power supply, enabling battery back-up operation during power failure or power-down operation in the non-selected mode.

FUNCTION TABLE

$\overline{S}$	$\overline{W}$	$\overline{OE}$	Mode	DQ	Icc
H	X	X	Non selection	High-impedance	Stand-by
L	L	X	Write	D_{in}	Active
L	H	L	Read	D_{out}	Active
L	H	H		High-impedance	Active

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to GND	− 0.3 ~7	V
V_I	Input voltage		− 0.3 ~V_{CC} + 0.3	V
V_O	Output voltage		0 ~V_{CC}	V
P_d	Power dissipation	T_a = 25℃	700	mW
T_{opr}	Operating temperature		0~70	℃
T_{stg}	Storage temperature		− 65~150	℃

ELECTRICAL CHARACTERISTICS (T_a = 0~70℃, V_{CC} = 5V ± 10%, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits Min	Limits Typ	Limits Max	Unit
V_{IH}	High input voltage			2.2		V_{CC}+0.3	V
V_{IL}	Low input voltage			− 0.3		0.8	V
V_{OH}	High output voltage	I_{OH} = − 1mA		2.4			V
V_{OL}	Low output voltage	I_{OL} = 2mA				0.4	V
I_I	Input leakage current	V_I = 0~V_{CC}				± 1	μA
I_O	Output leakage current	$\overline{S}$ = V_{IH} or $\overline{OE}$ = V_{IH}, $V_{I/O}$ = 0~V_{CC}				± 1	μA
I_{CC1}	Active supply current(AC MOS level)	$\overline{S}$ < 0.2, $\overline{W}$ > V_{CC}−0.2 output open Other inputs < 0.2 or > V_{CC} − 0.3 Min cycle			30	65	mA
I_{CC2}	Active supply current(AC TTL level)	$\overline{S}$ = V_{IL}, $\overline{W}$ = V_{IH} output open Other inputs = V_{IL} or V_{IH} Min cycle			35	70	mA
I_{CC3}	Stand by supply current	$\overline{S}$ ≧ V_{CC} − 0.2V Other inputs = 0~V_{CC}	BP, FP, KP			2	mA
			BP, FP, KP-L			100	μA
			BP, FP, KP-LL			20	μA
I_{CC4}	Stand by supply current	$\overline{S}$ = V_{IH}, other inputs = 0~V_{CC}				3	mA
C_I	Input capacitance (T_a = 25℃)	V_I = GND, V_I = 25mVrms, f = 1MHz				6	pF
C_O	Output capacitance (T_a = 25℃)	V_O = GND, V_O = 25mVrms, f = 1MHz				8	pF

Note 1. Direction for current flowing into IC is indicated as positive (no mark)
2. Typical value is V_{CC} = 5V, T_a = 25℃

SWITCHING CHARACTERISTICS (Ta = 0~70℃, Vcc = 5V ± 10%, unless otherwise noted)
Read cycle

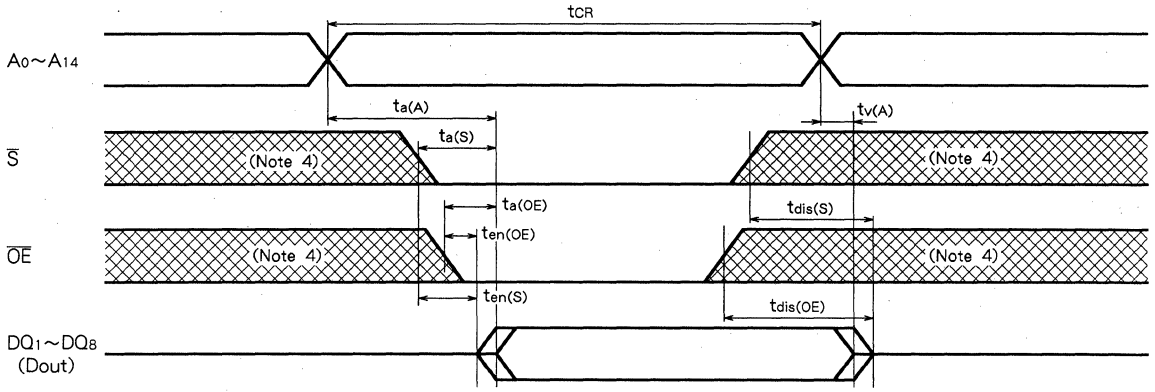
Symbol	Parameter	Limits										Unit
		M5M5256-70 M5M5256-70L M5M5256-70LL		M5M5256-85 M5M5256-85L M5M5256-85LL		M5M5256-10 M5M5256-10L M5M5256-10LL		M5M5256-12 M5M5256-12L M5M5256-12LL		M5M5256-15 M5M5256-15L M5M5256-15LL		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{CR}	Read cycle time	70		85		100		120		150		ns
$t_{a(A)}$	Address access time		70		85		100		120		150	ns
$t_{a(S)}$	Chip select access time		70		85		100		120		150	ns
$t_{a(OE)}$	Output enable access time		35		45		50		60		75	ns
$t_{dis(S)}$	Output disable time after $\overline{S}$ high		30		30		35		40		45	ns
$t_{dis(OE)}$	Output disable time after $\overline{OE}$ high		25		30		35		40		45	ns
$t_{en(S)}$	Output enable time after $\overline{S}$ low	5		5		10		10		10		ns
$t_{en(OE)}$	Output enable time after $\overline{OE}$ low	5		5		10		10		10		ns
$t_{v(A)}$	Data valid time after address change	20		20		20		20		20		ns

TIMING REQUIREMENTS (Ta = 0~70℃, Vcc = 5V ± 10%, unless otherwise noted)
Write cycle

Symbol	Parameter	Limits										Unit
		M5M5256-70 M5M5256-70L M5M5256-70LL		M5M5256-85 M5M5256-85L M5M5256-85LL		M5M5256-10 M5M5256-10L M5M5256-10LL		M5M5256-12 M5M5256-12L M5M5256-12LL		M5M5256-15 M5M5256-15L M5M5256-15LL		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{CW}	Write cycle time	70		85		100		120		150		ns
$t_{w(W)}$	Write pulse width	55		60		60		70		80		ns
$t_{su(A)}$	Address set up time	0		0		0		0		0		ns
$t_{su(A-WH)}$	Address set up time with respect to $\overline{W}$ high	65		75		80		85		90		ns
$t_{su(S)}$	Chip select set up time	65		75		80		85		90		ns
$t_{su(D)}$	Data set up time	30		35		35		40		50		ns
$t_{h(D)}$	Data hold time	0		0		0		0		0		ns
$t_{rec(W)}$	Write recovery time	0		0		0		0		0		ns
$t_{dis(W)}$	Output disable time after $\overline{W}$ low		25		30		35		40		45	ns
$t_{dis(OE)}$	Output disable time after $\overline{OE}$ high		25		30		35		40		45	ns
$t_{en(W)}$	Output enable time after $\overline{W}$ high	5		5		10		10		10		ns
$t_{en(OE)}$	Output enable time after $\overline{OE}$ low	5		5		10		10		10		ns

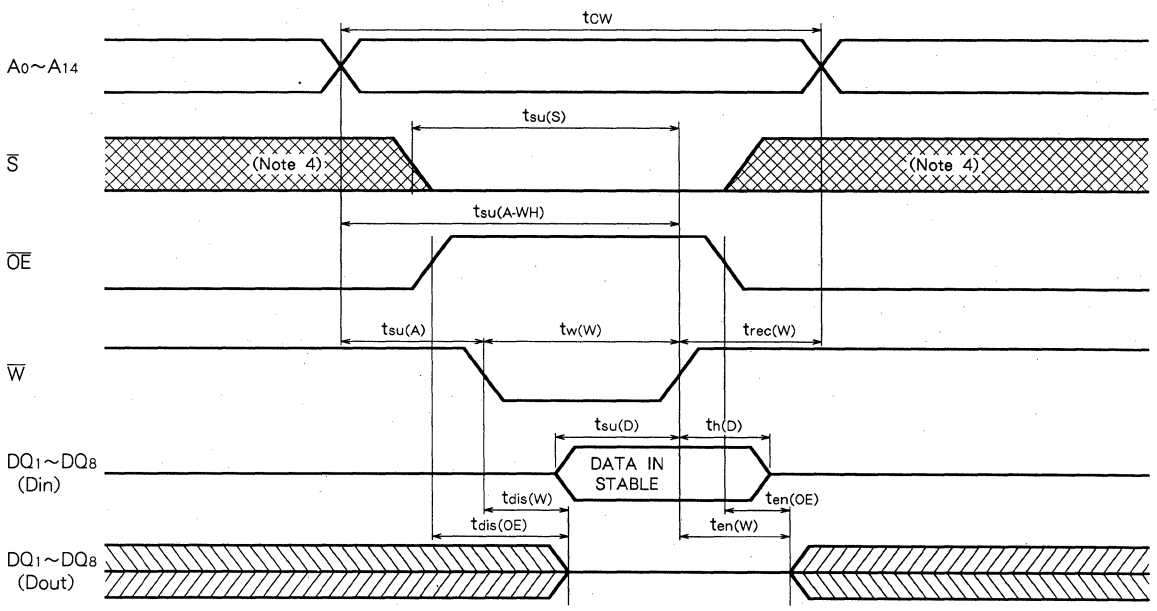
TIMING DIAGRAM

Read cycle

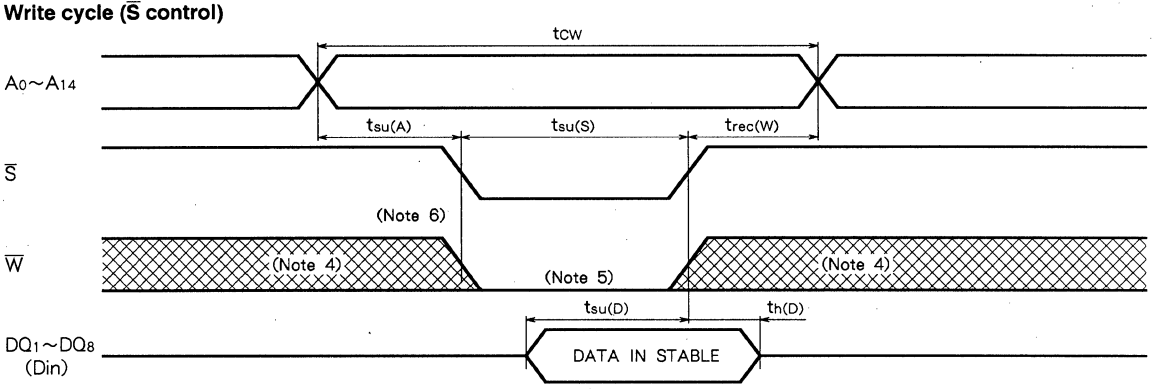


W = "H" level

Write cycle (W control)



Write cycle ($\overline{S}$ control)



Note 3 : Test condition

Input pulse levels ····· V_{IH} = 2.4V, V_{IL} = 0.6V

Input rise and fall time ····· 10ns

Reference levels ····· V_{OH} = V_{OL} = 1.5V

Transition is measured ±500mV from steady state voltage.(for t_{en}, t_{dis})

Output loads ····· Fig. 1, C_L = 100pF (BP, FP, KP-85, -10, -12, -15, -85L, -10L, -12L, -15L, -85LL, -10LL, -12LL, -15LL)

C_L = 30pF (BP, FP, KP-70, -70L, -70LL)

C_L = 5pF (for t_{en}, t_{dis})

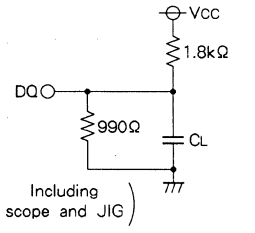


Fig. 1 Output load

Note 4. Hatching indicates the state is don't care.
5. Writing is executed in overlap of $\overline{S}$ and $\overline{W}$ low.
6. If $\overline{W}$ goes low simultaneously with or prior to $\overline{S}$, the output remains in the high-impedance state.
7. Don't apply inverted phase signal externally when DQ pin is in output mode.

POWER DOWN CHARACTERISTICS

ELECTRICAL CHARACTERISTICS (Ta = 0~70℃, unless otherwise noted)

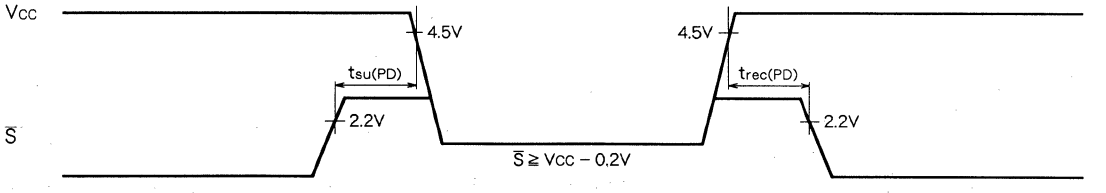
Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ	Max	
$V_{CC(PD)}$	Power down supply voltage			2			V
$V_{I(\overline{S})}$	Chip select input $\overline{S}$	2.2V ≦ $V_{CC(PD)}$		2.2			V
		2V ≦ $V_{CC(PD)}$ ≦ 2.2V			$V_{CC(PD)}$		
$I_{CC(PD)}$	Power down supply current	V_{CC} = 3V, Other inputs=3V	BP,FP,KP			2	mA
			BP,FP,KP-L			50	μA
			BP,FP,KP-LL			10*	μA

* Ta = 25℃, $I_{CC(PD)}$ = 1 μA

TIMING REQUIREMENTS (Ta = 0~70℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{su(PD)}$	Power down setup time		0			ns
$t_{rec(PD)}$	Power down recovery time		t_{CR}			ns

POWER DOWN CHARACTERISTICS



M5M5256BVP,RV-70L,-85L,-10L,-12L,-15L, -70LL,-85LL,-10LL,-12LL,-15LL

262144-BIT (32768-WORD BY 8-BIT) CMOS STATIC RAM

DESCRIPTION

The M5M5256BVP, RV are 262144-bit CMOS static RAMs organized as 32768-words by 8-bit. They are fabricated using high-performance double polysilicon CMOS technology. The use of resistive load NMOS cells and CMOS periphery result in a high-density and low-power static RAM. Stand-by current is small enough for battery backup application.

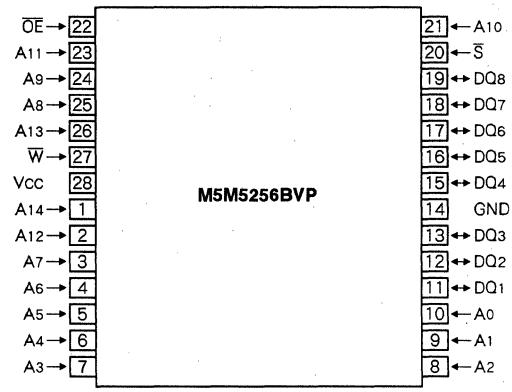
The M5M5256BVP, RV are packaged in a 28-pin very small outline package which is a high reliability and high density surface mount device (SMD). Two types of devices are available. M5M5256BVP (normal lead bend type package), M5M5256BRV (reverse lead bend type package). Using both type of devices, it becomes very easy to design a printed circuit board.

FEATURES

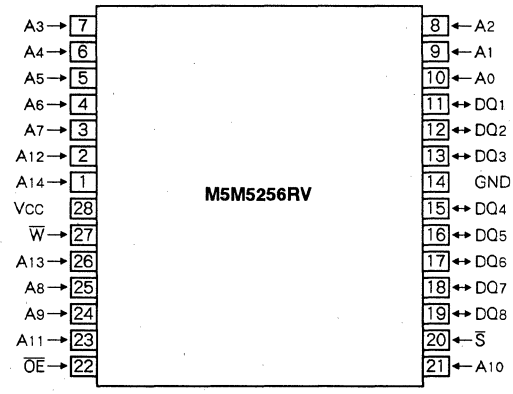
Type name	Access time (max)	Power supply current	
		Active (max)	Stand-by (max)
M5M5256BVP, RV-70L	70ns	70mA	100 μA (Vcc = 5.5V) 50 μA (Vcc = 3.0V)
M5M5256BVP, RV-85L	85ns		
M5M5256BVP, RV-10L	100ns		
M5M5256BVP, RV-12L	120ns		
M5M5256BVP, RV-15L	150ns		
M5M5256BVP, RV-70LL	70ns		20 μA (Vcc = 5.5V) 10 μA (Vcc = 3.0V)
M5M5256BVP, RV-85LL	85ns		
M5M5256BVP, RV-10LL	100ns		
M5M5256BVP, RV-12LL	120ns		
M5M5256BVP, RV-15LL	150ns		

- High density and high reliability surface mount device 28 -pin
  very small outline package : 8.0mm × 13.4mm (typ)
  very thin package : 1mm (typ)
- Single + 5V power supply
- Fully static operation
- Data-hold on + 2V power supply

PIN CONFIGURATION (TOP VIEW)

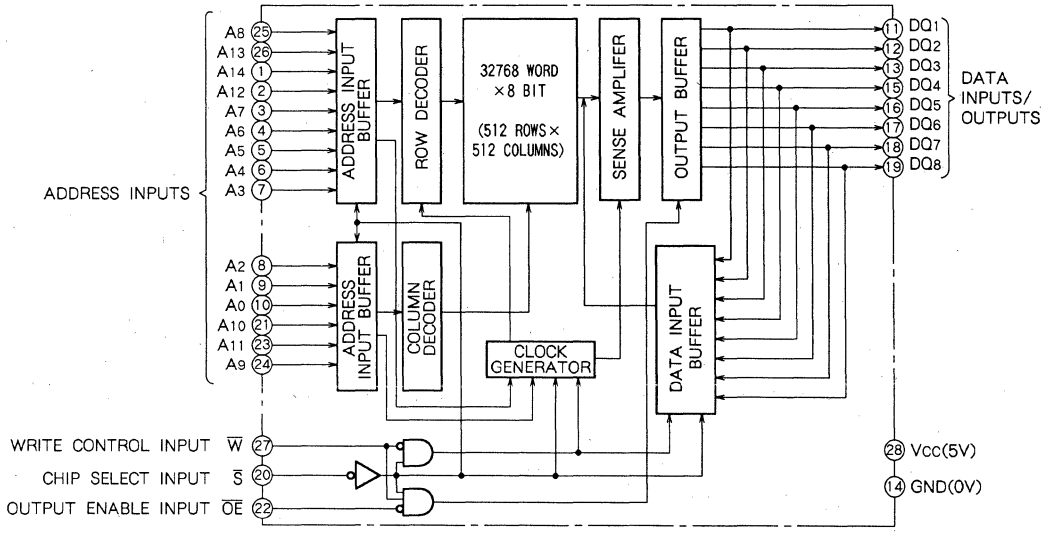


Outline 28P2C-A



Outline 28P2C-B

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

M5M5256BVP,RV-70L,-85L,-10L,-12L,-15L, -70LL,-85LL,-10LL,-12LL,-15LL

262144-BIT (32768-WORD BY 8-BIT) CMOS STATIC RAM

● Package

M5M5256BVP, RV

·····28 pin Thin Small Outline Package (TSOP)

APPLICATION

IC card, memory module

FUNCTION

The operation mode of the M5M5256BVP,RV is determined by a combination of the device control inputs $\overline{S}$, $\overline{W}$ and $\overline{OE}$. Each mode is summarized in the function table.

A write cycle is executed whenever the low level $\overline{W}$ overlaps with the low level $\overline{S}$. The address must be set up before the write cycle and must be stable during the entire cycle. The data is latched into a cell on the trailing edge of $\overline{W}$, $\overline{S}$, whichever occurs first, requiring the set-up and hold time relative to these edge to be maintained. The output enable $\overline{OE}$ directly controls the output state. Setting the $\overline{OE}$ at a high level, the output state is in a high-impedance state, and the data bus contention problem in the write cycle is eliminated.

A read cycle is executed by setting $\overline{W}$ at a high level and $\overline{OE}$ at a low level while $\overline{S}$ are in an active state.

When setting $\overline{S}$ at a high level, the chip is in a non-selectable mode in which both reading and writing are disabled. In this mode, the output state is in a high-impedance state, allowing OR-tie with other chips and memory expansion by $\overline{S}$. The power supply current is reduced as low as the stand-by current which is specified as I_{CC3} or I_{CC4}, and the memory data can be held + 2V power supply, enabling battery back-up operation during power failure or power-down operation in the non-selected mode.

FUNCTION TABLE

$\overline{S}$	$\overline{W}$	$\overline{OE}$	Mode	DQ	I_{CC}
H	X	X	Non selection	High-impedance	Stand-by
L	L	X	Write	D_{in}	Active
L	H	L	Read	D_{out}	Active
L	H	H		High-impedance	Active

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to GND	− 0.3~7	V
V_I	Input voltage		− 0.3~V_{CC} + 0.3	V
V_O	Output voltage		0~V_{CC}	V
P_d	Power dissipation	T_a = 25℃	700	mW
T_{opr}	Operating temperature		0~70	℃
T_{stg}	Storage temperature		− 65~150	℃

ELECTRICAL CHARACTERISTICS (T_a = 0~70℃, V_{CC} = 5V ± 10%, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ	Max	
V_{IH}	High-level input voltage			2.2		V_{CC}+0.3	V
V_{IL}	Low-level input voltage			−0.3		0.8	V
V_{OH}	High-level output voltage	I_{OH} = −1mA		2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 2mA				0.4	V
I_I	Input leakage current	V_I = 0~V_{CC}				±1	μA
I_O	Output leakage current	$\overline{S}$ = V_{IH} or $\overline{OE}$ = V_{IH}, $V_{I/O}$ = 0~V_{CC}				±1	μA
I_{CC1}	Active supply current (AC, MOS level)	$\overline{S}$<0.2V, $\overline{W}$>V_{CC}−0.2V, Output open Other inputs<0.2V or >V_{CC}−0.2V Min. cycle			30	65	mA
I_{CC2}	Active supply current (AC, TTL, level)	$\overline{S}$ = V_{IL}, $\overline{W}$ = V_{IH}, Output open Other inputs = V_{IH} or V_{IL} Min. cycle			35	70	mA
I_{CC3}	Stand by supply current	$\overline{S}$ > V_{CC} − 0.2V Other inputs = 0~V_{CC}	BVP, RV-L			100	μA
			BVP, RV-LL			20	μA
I_{CC4}	Stand by supply current	$\overline{S}$ = V_{IH}, Other inputs = 0~V_{CC}				3	mA
C_I	Input capacitance (T_a = 25℃)	V_I = GND, V_I = 25mVrms, f = 1MHz				6	pF
C_O	Output capacitance (T_a = 25℃)	V_O = GND, V_O = 25mVrms, f = 1MHz				8	pF

Note 1. Direction for current flowing into IC is indicated as positive (no mark).
2. Typical value is V_{CC} = 5V, T_a = 25℃.

SWITCHING CHARACTERISTICS (T_a = 0~70℃, V_{CC} = 5V ± 10%, unless otherwise noted)
Read Cycle

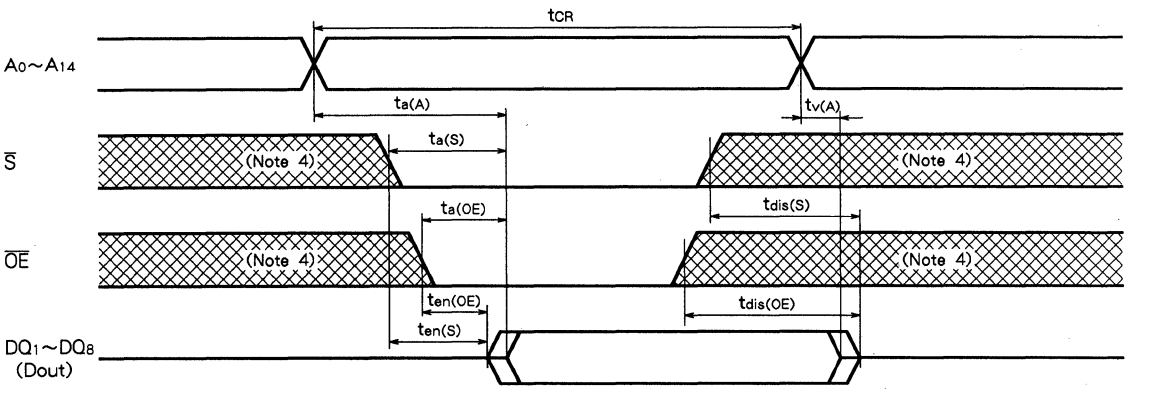
Symbol	Parameter	Limits										Unit
		M5M5256-70L M5M5256-70LL		M5M5256-85L M5M5256-85LL		M5M5256-10L M5M5256-10LL		M5M5256-12L M5M5256-12LL		M5M5256-15L M5M5256-15LL		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{CR}	Read cycle time	70		85		100		120		150		ns
$t_{a(A)}$	Address access time		70		85		100		120		150	ns
$t_{a(S)}$	Chip select access time		70		85		100		120		150	ns
$t_{a(OE)}$	Output enable access time		35		45		50		60		75	ns
$t_{dis(S)}$	Output disable time after $\overline{S}$ high		30		30		35		40		45	ns
$t_{dis(OE)}$	Output disable time after $\overline{OE}$ high		25		30		35		40		45	ns
$t_{en(S)}$	Output enable time after $\overline{S}$ low	5		5		10		10		10		ns
$t_{en(OE)}$	Output enable time after $\overline{OE}$ low	5		5		10		10		10		ns
$t_{v(A)}$	Data valid time after address	20		20		20		20		20		ns

TIMING REQUIREMENTS (T_a = 0~70℃, V_{CC} = 5V ± 10%, unless otherwise noted)
Write Cycle

Symbol	Parameter	Limits										Unit
		M5M5256-70L M5M5256-70LL		M5M5256-85L M5M5256-85LL		M5M5256-10L M5M5256-10LL		M5M5256-12L M5M5256-12LL		M5M5256-15L M5M5256-15LL		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{CW}	Write cycle time	70		85		100		120		150		ns
$t_{w(W)}$	Write pulse width	55		60		60		70		80		ns
$t_{su(A)}$	Address set up time	0		0		0		0		0		ns
$t_{su(A-WH)}$	Address set up time respect to $\overline{W}$ high	65		75		80		85		90		ns
$t_{su(S)}$	Chip select set up time	65		75		80		85		90		ns
$t_{su(D)}$	Data set up time	30		35		35		40		50		ns
$t_{h(D)}$	Data hold time	0		0		0		0		0		ns
$t_{rec(W)}$	Write recovery time	0		0		0		0		0		ns
$t_{dis(W)}$	Output disable time after $\overline{W}$ low		25		30		35		40		45	ns
$t_{dis(OE)}$	Output disable time after $\overline{OE}$ high		25		30		35		40		45	ns
$t_{en(W)}$	Output enable time after $\overline{W}$ high	5		5		10		10		10		ns
$t_{en(OE)}$	Output enable time after $\overline{OE}$ low	5		5		10		10		10		ns

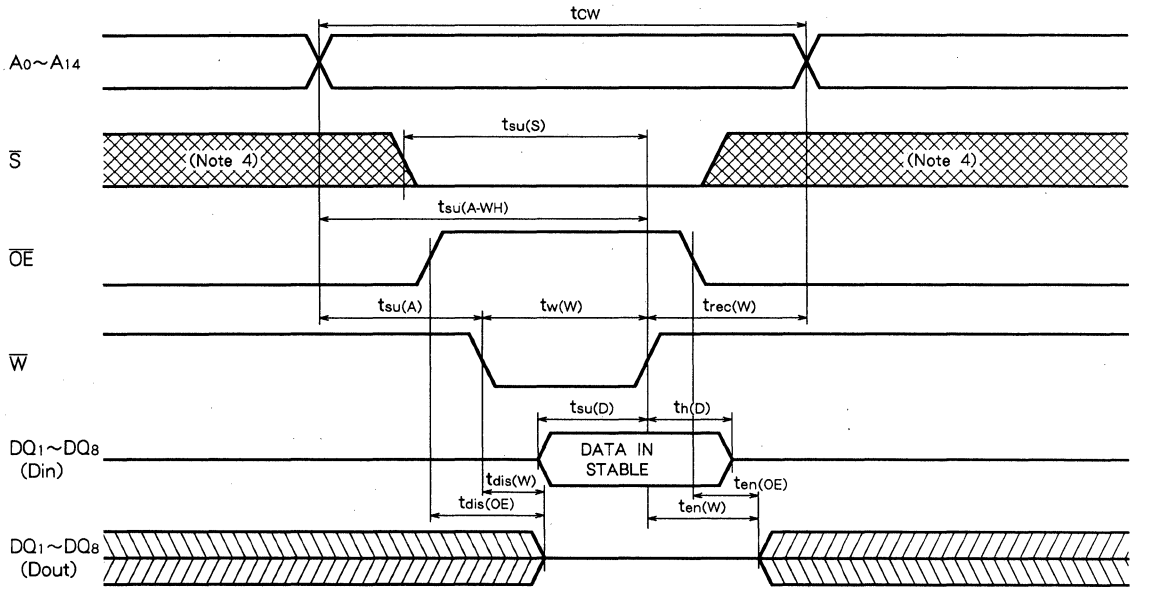
TIMING DIAGRAMS

Read cycle

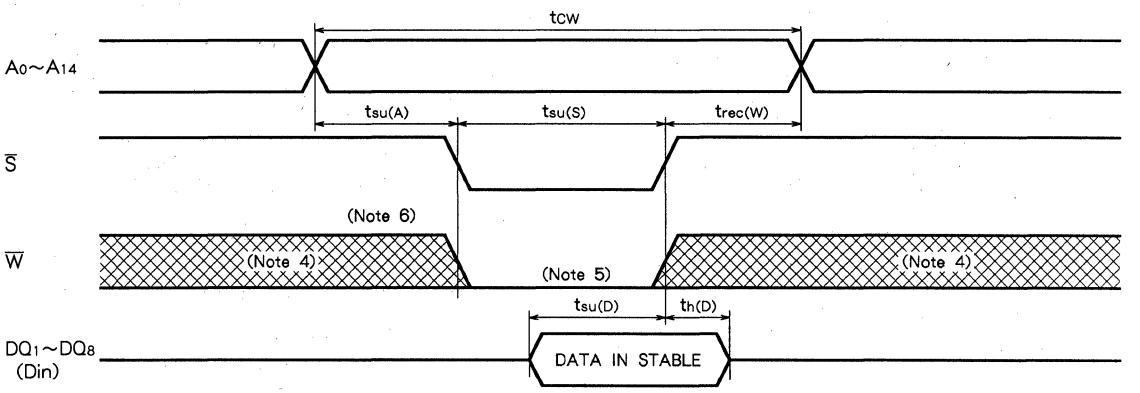


W = "H" level

Write cycle (W control mode)



Write cycle ($\overline{S}$ control mode)



Note 3 : Test condition

Input pulse levels ..... V_{IH} = 2.4V, V_{IL} = 0.6V

Input rise and fall time 10ns

Reference levels ..... V_{OH} = V_{OL} = 1.5V

Transition is measured ± 500mV from steady state voltage.(for t_{en}, t_{dis})

Output loads ..... Fig. 1, C_L = 100pF(85ns, 100ns, 120ns, 150ns)

C_L = 30pF (70ns)

C_L = 5pF (for t_{en}, t_{dis})

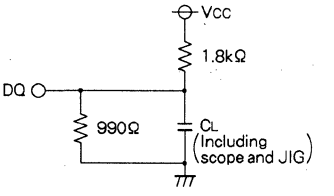


Fig. 1 Output load

Note 4. Hatching indicates the state is don't care.
5. Writing is executed in overlap of $\overline{S}$ and $\overline{W}$ low.
6. If $\overline{W}$ goes low simultaneously with or to S, the output remains in the high-impedance state.
7. Don't apply inverted phase signal externally when DQ pin is in output mode.

POWER DOWN CHARACTERISTICS

ELECTRICAL CHARACTERISTICS (T_a = 0~70℃, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ	Max	
$V_{CC(PD)}$	Power down supply voltage			2			V
$V_{I(\overline{S})}$	Chip select input $\overline{S}$	2.2V ≦ $V_{CC(PD)}$		2.2			V
		2V ≦ $V_{CC(PD)}$ ≦ 2.2V			$V_{CC(PD)}$		
$I_{CC(PD)}$	Power down supply current	V_{CC} = 3V, Other inputs = 3V	BVP, RV-L			50	μA
			BVP, RV-LL			10*	μA

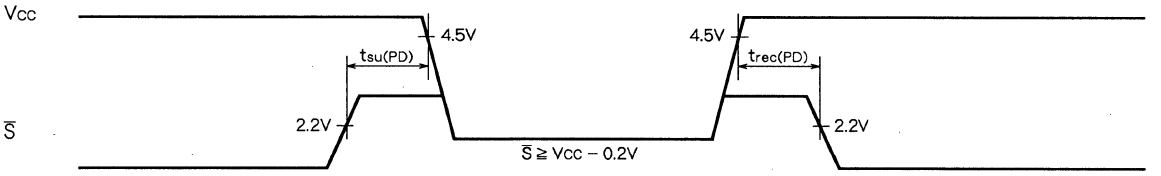
* T_a = 25℃, $I_{CC(PD)}$ = 1 μA

TIMING REQUIREMENTS

(T_a = 0~70℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{su(PD)}$	Power down set up time		0			ns
$t_{rec(PD)}$	Power down recovery time		t_{CR}			ns

POWER DOWN CHARACTERISTICS



M5M5255CP,FP,KP-55LL,-55XL, -70LL,-70XL

262144-BIT (32768-WORD BY 8-BIT) CMOS STATIC RAM

DESCRIPTION

This M5M5255CP,FP,KP is a 262144-bit CMOS static RAMs organized as 32768-words by 8-bits which is fabricated using high-performance 3 polysilicon CMOS technology. The use of resistive load NMOS cells and CMOS periphery result in a high-density and low-power static RAM. M5M5255CP,FP,KP provides two chip select input($\overline{S}_1$,S_2). Stand-by current is small enough for battery back-up application. It is ideal for the memory systems which require simple interface.

FEATURES

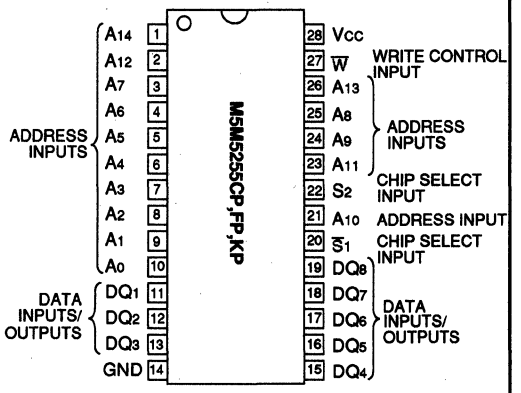
Type name	Access time (max)	Power supply current	
		Active (max)	Stand-by (max)
M5M5255CP,FP,KP-55LL M5M5255CP,FP,KP-70LL	55ns 70ns	60mA (Vcc=5.5V)	20 μA (Vcc=5.5V)
M5M5255CP,FP,KP-55XL M5M5255CP,FP,KP-70XL	55ns 70ns		5 μA (Vcc=5.5V) 0.05 μA (Vcc=3V,Typ)

- Single +5V power supply
- No clocks, no refresh
- Data-hold on +2V power supply
- Directly TTL compatible: All inputs and outputs
- Three-state outputs: OR-tie capability
- Simple memory expansion by $\overline{S}_1$, S_2
- Common data I/O
- Low stand-by current ····· 0.05 μA (Vcc=3V、typ)
- Package
  - M5M5255CP ····· 28 pin 600 mil DIP
  - M5M5255CFP ····· 28 pin 450 mil SOP
  - M5M5255CKP ····· 28 pin 300 mil DIP

APPLICATION

Small capacity memory units

PIN CONFIGURATION (TOP VIEW)



Outline 28P4(P)
28P2W-C(FP)
28P4Y(KP)

FUNCTION

The operation mode of the M5M5255CP,KP,FP is determined by a combination of the device control inputs $\overline{S}_1$,S_2 and $\overline{W}$. Each mode is summariezed in the function table.

A write cycle is executed whenever the low level $\overline{W}$ overlaps with the low level $\overline{S}_1$ and the high level S_2. The address must be set up before the write cycle and must be stable during the entire cycle.

The data is latched into a cell on the trailing edge of $\overline{W}$, $\overline{S}_1$ or S_2, whichever occurs first, requiring the set-up and hold time relative to these edge to be maintained.

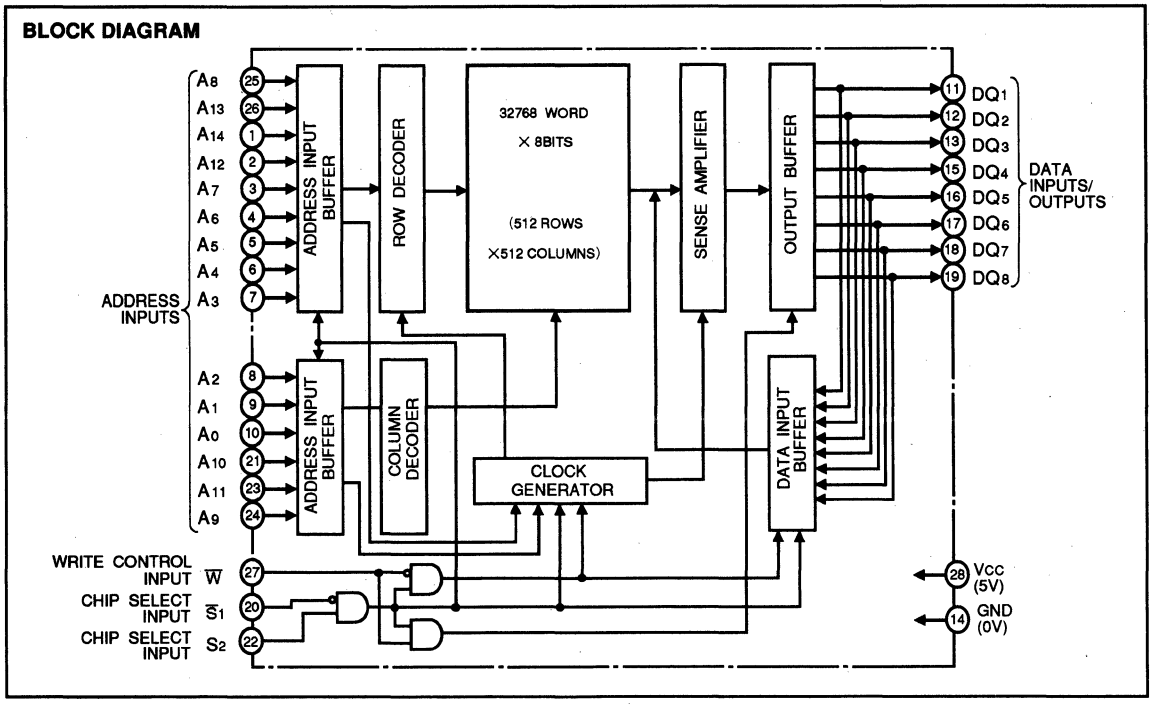
A read cycle is executed by setting $\overline{W}$ at a high level while $\overline{S}_1$ and S_2 are in an active state ($\overline{S}_1$="L", S_2="H").

When setting $\overline{S}_1$ at a high level or S_2 at a low level, the chip is in a non-selectable mode in which both reading and writing are disabled. In this mode, the output stage is in a high-impedance state, allowing OR-tie with other chips and memory expansion by $\overline{S}_1$ and S_2. The power supply current is reduced as low as the stand-by current which is specified as I_{CC3} or I_{CC4}, and the memory data can be held +2V power supply,enabling battery back-up operation during power failure or power-down operation in the non-selected mode.

FUNCTION TABLE

$\overline{S}_1$	S_2	$\overline{W}$	Mode	DQ	Icc
H	X	X	Non selection	High-impedance	Stand-by
L	L	X	Non selection	High-impedance	Stand-by
L	H	L	Write	DIN	Active
L	H	H	Read	DOUT	Active

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to GND	−0.3～7	V
V_I	Input voltage	With respect to GND	−0.3*～Vcc+0.3	V
V_O	Output voltage	With respect to GND	0～Vcc	V
P_d	Power dissipation	Ta=25℃	700	mW
T_{opr}	Operating temperature		0～70	℃
T_{stg}	Storage temperature		−65～150	℃

* −3.0V in case of AC (Pulse width≦30ns)

DC ELECTRICAL CHARACTERISTICS (Ta=0～70℃, Vcc=5V±10%, unless otherwise noted.)

Symbol	Parameter	Test conditions		Limits Min	Limits Typ	Limits Max	Unit
V_{IH}	High-level input voltage			2.2		Vcc+0.3V	V
V_{IL}	Low-level input voltage			−0.3*		0.8	V
V_{OH}	High-level output voltage	I_{OH}=−1mA		2.4			V
		I_{OH}=−0.1mA		Vcc−0.5V			
V_{OL}	Low-level output voltage	I_{OL}=2mA				0.4	V
I_I	Input leakage current	V_I=0～Vcc				±1	μA
I_O	Output leakage current	$\overline{S}_1$=V_{IH} or S_2=V_{IL}, $V_{I/O}$=0～Vcc				±1	μA
I_{CC1}	Active supply current (AC,MOS level)	$\overline{S}_1$≦0.2V, S_2≧Vcc−0.2 Other inputs≦0.2V or≧Vcc−0.2V Output open Min.cycle	55ns		35	55	mA
			70ns		30	50	
I_{CC2}	Active supply current (AC,TTL level)	$\overline{S}_1$=V_{IL} or S_2=V_{IH} Other inputs=V_{IH} or V_{IL} Output open Min.cycle	55ns		40	60	mA
			70ns		35	55	
I_{CC3}	Stand-by supply current	1) S_2≦0.2V, Other inputs=0～Vcc 2) $\overline{S}_1$≧Vcc−0.2V, S_2≧Vcc−0.2V, Other inputs=0～Vcc	-LL			20	μA
			-XL		0.1	5	μA
I_{CC4}	Stand-by supply current	1) S_2=V_{IL}, 2). $\overline{S}_1$=V_{IH}, S_2=V_{IH} Other inputs=0～Vcc				3	mA

* −3.0V in case of AC (Pulse width 30ns)

CAPACITANCE (Ta=0～70℃, Vcc=5V±10%, unless otherwise noted.)

Symbol	Parameter	Test conditions	Limits Min	Limits Typ	Limits Max	Unit
C_I	Input capacitance (Ta=25℃)	V_I=GND, V_I=25mVrms, f=1MHz			6	pF
C_O	Output capacitance (Ta=25℃)	V_O=GND, V_O=25mVrms, f=1MHz			8	pF

Note1: Direction for current flowing into IC is indicated as positive. (no mark)
2: Typical value is Vcc=5V, Ta=25℃.
3: C_I, C_O are periodically sampled and are not 100% tested.

AC ELECTRICAL CHARACTERISTICS (Ta=0～70℃, Vcc=5V±10%, unless otherwise noted.)

(1) MEASUREMENT CONDITIONS

Input pulse level ·····V_{IH} = 2.4V, V_{IL} = 0.6V
Input rise and fall time ·····5ns
Reference level ·····V_{OH} = V_{OL} = 1.5V
Transition is measured ±500mV from steady state voltage. (for t_{en}, t_{dis})
Output loads ·····Fig.1, C_L = 50pF
C_L = 5pF (for t_{en}, t_{dis})

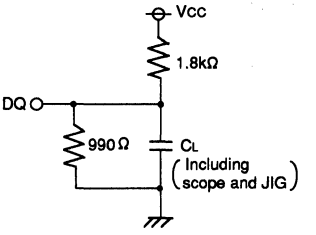


Fig.1 Output load

(2) READ CYCLE

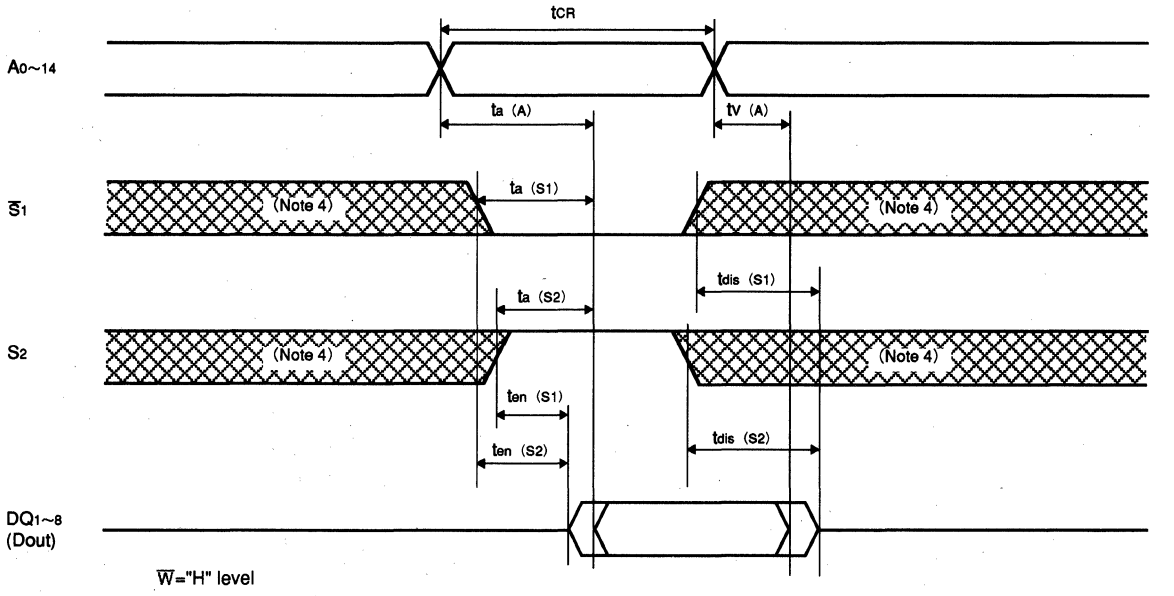
Symbol	Parameter	Limits				Unit
		M5M5255C-55LL, -55XL		M5M5255C-70LL, -70XL		
		Min	Max	Min	Max	
t_{CR}	Read cycle time	55		70		ns
$t_{a(A)}$	Address access time		55		70	ns
$t_{a(S1)}$	Chip serect 1 access time		55		70	ns
$t_{a(S2)}$	Chip serect 2 access time		55		70	ns
$t_{dis(S1)}$	Output disable time after $\overline{S}_1$ high		20		25	ns
$t_{dis(S2)}$	Output disable time after S_2 low		20		25	ns
$t_{en(S1)}$	Output enable time after $\overline{S}_1$ low	5		5		ns
$t_{en(S2)}$	Output enable time after S_2 high	5		5		ns
$t_{v(A)}$	Data valid time after address change	10		10		ns

(3) WRITE CYCLE

Symbol	Parameter	Limits				Unit
		M5M5255C-55LL, -55XL		M5M5255C-70LL, -70XL		
		Min	Max	Min	Max	
t_{CW}	Write cycle time	55		70		ns
$t_{w(W)}$	Write pulse width	45		55		ns
$t_{su(A)}$	Address set up time	0		0		ns
$t_{su(A-WH)}$	Address set up time with respect to $\overline{W}$ high	50		65		ns
$t_{su(S1)}$	Chip select 1 set up time	50		65		ns
$t_{su(S2)}$	Chip select 2 set up time	50		65		ns
$t_{su(D)}$	Data set up time	25		30		ns
$t_{h(D)}$	Data hold time	0		0		ns
$t_{rec(W)}$	Write recovery time	0		0		ns
$t_{dis(W)}$	Output disable time after $\overline{W}$ low		20		25	ns
$t_{en(W)}$	Output enable time after $\overline{W}$ high	5		5		ns

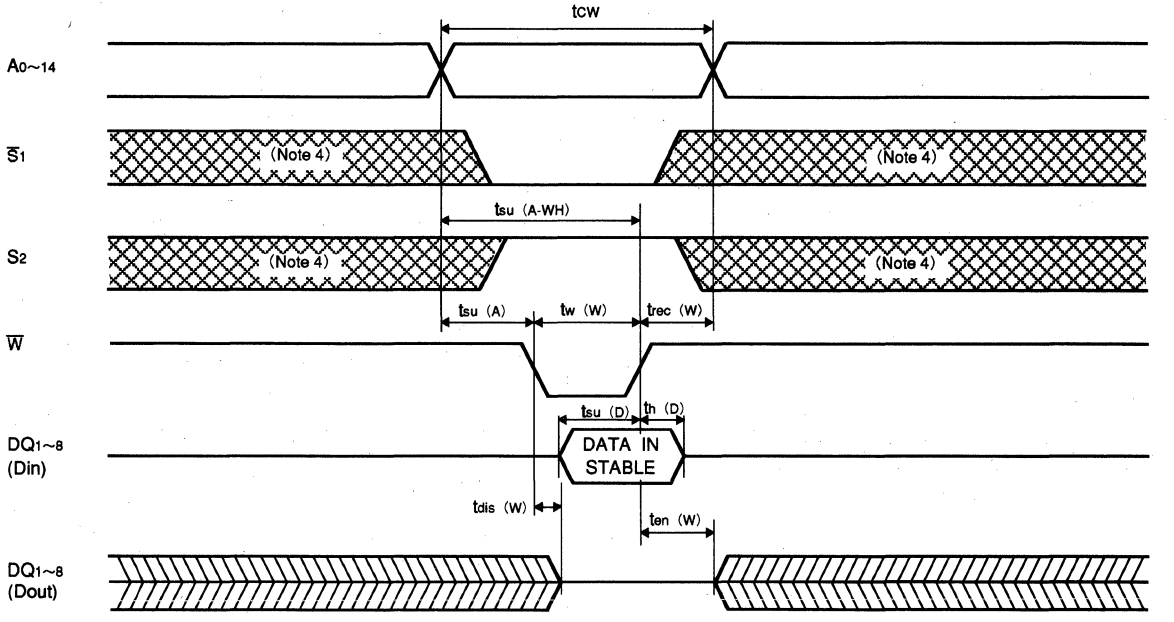
(4) TIMING DIAGRAMS

Read cycle

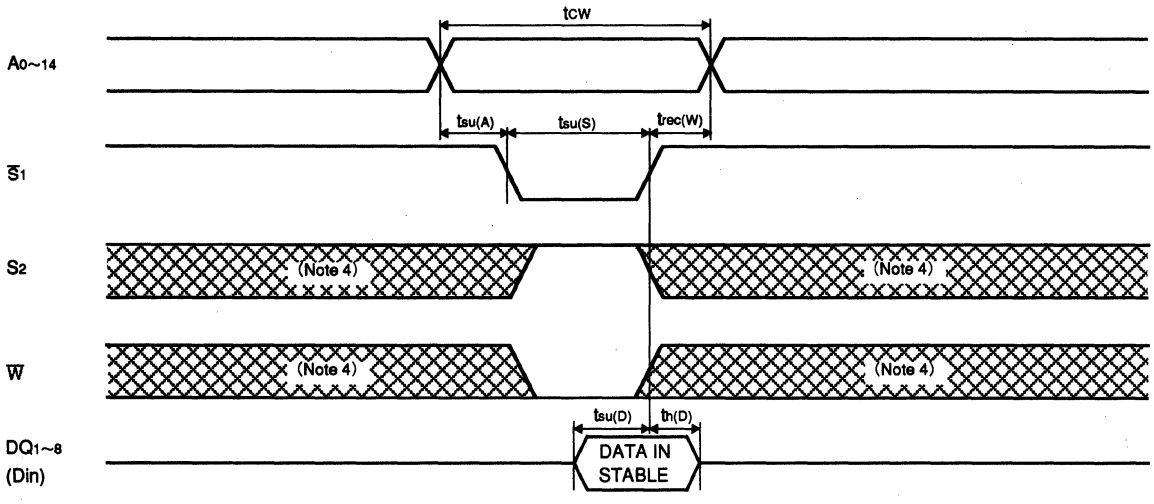


W="H" level

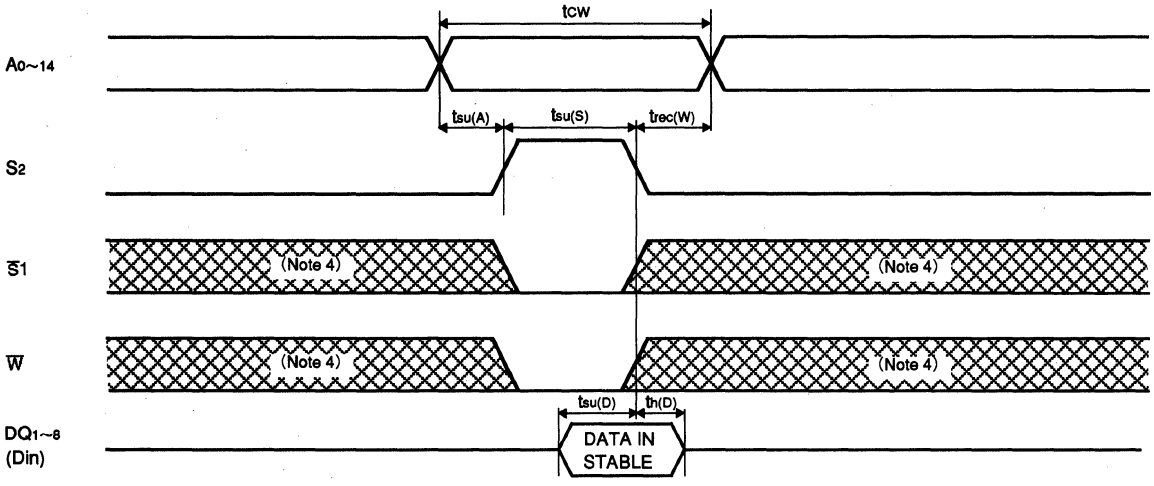
Write cycle (W control)



Write cycle ($\overline{S}_1$ control)



Write cycle (S_2 control)



Note 4: Hatching indicates the state is don't care.
5: Writing is executed while S_2 high overlaps $\overline{S}_1$ and $\overline{W}$ low.
6: If $\overline{W}$ goes low simultaneously with or prior to $\overline{S}_1$ low or S_2 high, the output remains in the high-impedance state.
7: Don't apply inverted phase signal externally when DQ pin is in output mode.
8: ten,tdis are periodically sampled and are not 100% tested.

POWER DOWN CHARACTERISTICS

(1) ELECTRICAL CHARACTERISTICS (Ta=0~70℃, Vcc=5V±10%, unless otherwise noted.)

Symbol	Parameter	Test conditions		Limits Min	Limits Typ	Limits Max	Unit
$V_{CC(PD)}$	Power down supply voltage			2			V
$V_{I(\overline{S1})}$	Chip select input $\overline{S_1}$	2.2V≦$V_{CC(PD)}$		2.2			V
		2V≦$V_{CC(PD)}$≦2.2V			$V_{CC(PD)}$		
$V_{I(S2)}$	Chip select input S_2	4.5V≦$V_{CC(PD)}$				0.8	V
		$V_{CC(PD)}$<4.5V				0.2	
$I_{CC(PD)}$	Power down supply current	Vcc=3V Other inputs=0~3V 1) S_2≦0.2V or 2) $\overline{S_1}$≧Vcc−0.2V, S_2≧Vcc−0.2V	-LL			10*	μA
			-XL		0.05	2**	μA

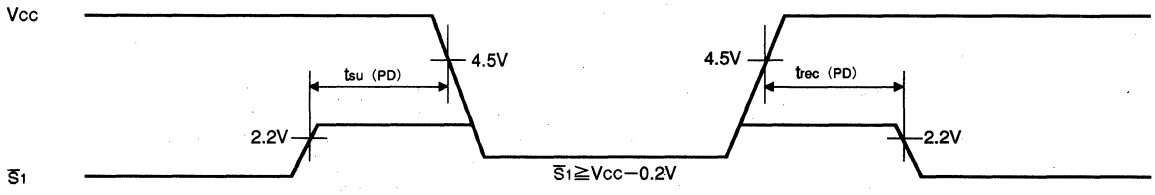
* Ta=25℃, $I_{CC(PD)}$=1 μA(max).
** Ta=25℃, $I_{CC(PD)}$=0.2 μA(max).

(2) TIMING REQUIREMENTS (Ta=0~70℃, VCC=5V±10%, unless otherwise noted.)

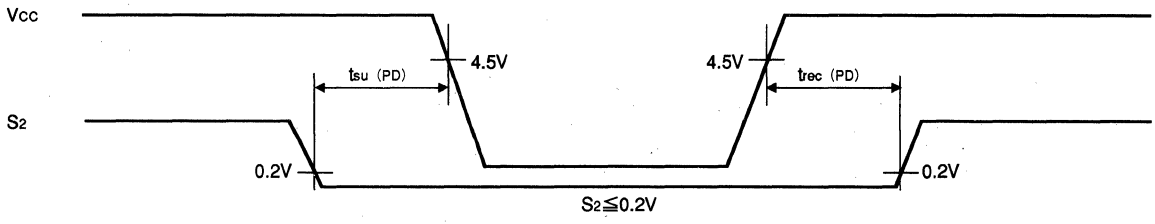
Symbol	Parameter	Test conditions	Limits Min	Limits Typ	Limits Max	Unit
$t_{su(PD)}$	Power down set up time		0			ns
$t_{rec(PD)}$	Power down recovery time		t_{CR}			ns

(3) POWER DOWN CHARACTERISTICS

$\overline{S_1}$ control mode



S_2 control



M5M5256CP,FP,KP,VP,RV-55LL,-55XL, -70LL,-70XL

262144-BIT(32768-WORD BY 8-BIT)CMOS STATIC RAM

DESCRIPTION

This M5M5256CP, FP, KP, VP, RV is a 262144-bit CMOS static RAMs organized as 32768-words by 8-bits which is fabricated using high-performance 3 polysilicon CMOS technology. The use of resistive load NMOS cells and CMOS periphery result in a high-density and low-power static RAM. Stand-by current is small enough for battery back-up applicaton. It is ideal for the memory systems which require simple interface.

Especially the M5M5256CVP, RV are packaged in a 28-pin thin small outline package. Two types of devices are available, M5M5256CVP (normal lead bend type package) and M5M5256CRV (reverse lead bend type package). Using both type of devices, it becomes very easy to design a printed circuit board.

FEATURES

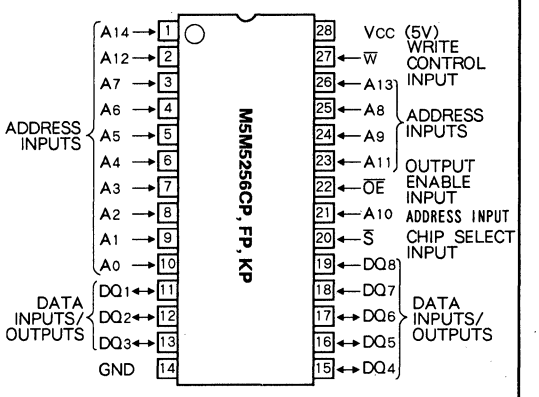
Type name	Access time (max)	Power supply current	
		Active (max)	Stand-by (max)
M5M5256CP, FP, KP, VP, RV-55LL	55ns	60mA (Vcc=5.5V)	20 μA (Vcc = 5.5V)
M5M5256CP, FP, KP, VP, RV-70LL	70ns		
M5M5256CP, FP, KP, VP, RV-55XL	55ns		5 μA (Vcc = 5.5V) 0.05 μA (Vcc = 3V, typ)
M5M5256CP, FP, KP, VP, RV-70XL	70ns		

- Single +5V power supply
- No clocks, no refresh
- Data-hold on +2V power supply
- Directly TTL compatible : All inputs and outputs
- Three-state outputs : OR-tie capability
- Simple memory expansion by $\overline{S}$
- $\overline{OE}$ prevents data contention in the I/O bus
- Common data I/O
- Low stand-by current ..... 0.05 μA (typ)
- Package
  - M5M5256CP ..... 28 pin 600 mil DIP
  - M5M5256CKP ..... 28 pin 300 mil DIP
  - M5M5256CFP ..... 28 pin 450 mil SOP
  - M5M5256CVP, RV ..... 28pin 8 × 13.4mm² TSOP

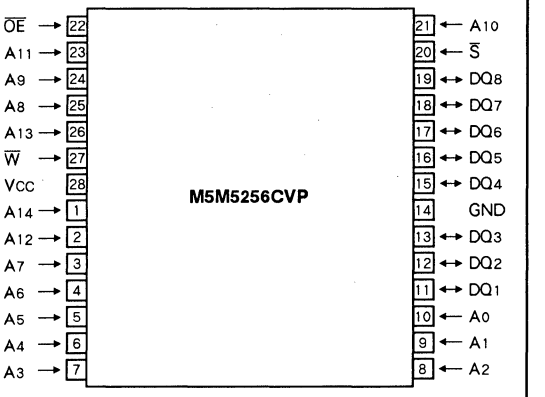
APPLICATION

Small capacity memory units

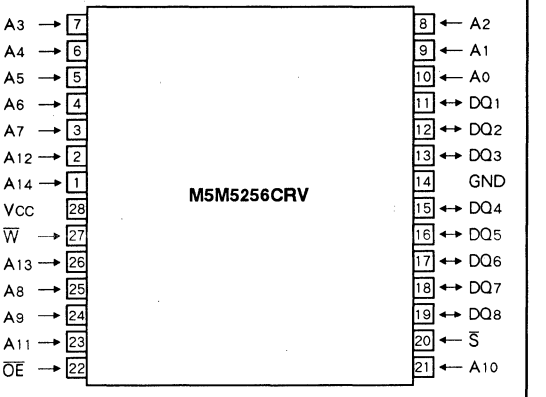
PIN CONFIGURATION (TOP VIEW)



Outline 28P4(P)
28P2W-C(FP)
28P4Y(KP)



Outline 28P2C-A



Outline 28P2C-B

262144-BIT(32768-WORD BY 8-BIT)CMOS STATIC RAM

FUNCTION

The operation mode of the M5M5256CP, FP, KP, VP, RV is determined by a combination of the device control inputs $\overline{S}$, $\overline{W}$ and $\overline{OE}$. Each mode is summariezed in the function table.

A write cycle is executed whenever the low level $\overline{W}$ overlaps with the low level $\overline{S}$. The address must be set-up before the write cycle and must be stable during the entire cycle. The data is latched into a cell on the trailing edge of $\overline{W}$, $\overline{S}$, whichever occurs first, requiring the set-up and hold time relative to these edge to be maintained. The output enable $\overline{OE}$ directly controls the output stage. Setting the $\overline{OE}$ at a high level, the output stage is in a high-impedance state, and the data bus contention problem in the write cycle is eliminated.

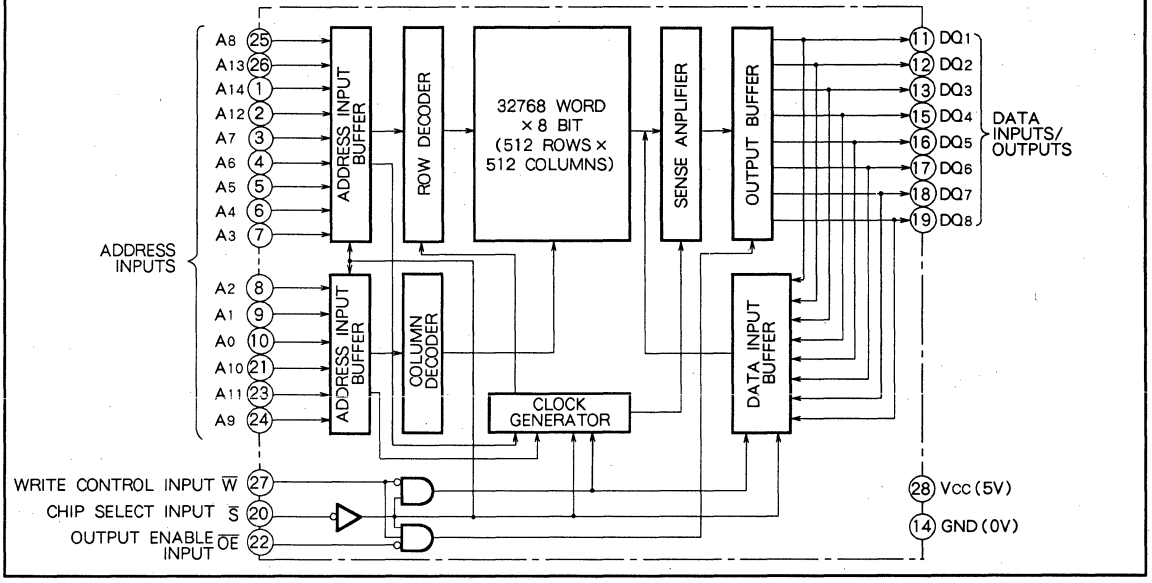
A read cycle is executed by setting $\overline{W}$ at a high level and $\overline{OE}$ at a low level while $\overline{S}$ are in an active state.

When setting $\overline{S}$ at a high level, the chip is in a non-selectable mode in which both reading and writing are disabled. In this mode, the output stage is in a high-impedance state, allowing OR-tie with other chips and memory expansion by $\overline{S}$. The power supply current is reduced as low as the stand-by current which is specified as I_{CC3} or I_{CC4}, and the memory data can be held +2V power supply, enabling battery back-up operation during power failure or power-down operation in the non-selected mode.

FUNCTION TABLE

$\overline{S}$	$\overline{W}$	$\overline{OE}$	Mode	DQ	Icc
H	X	X	Non selection	High-impedance	Stand-by
L	L	X	Write	Din	Active
L	H	L	Read	Dout	Active
L	H	H		High-impedance	Active

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to GND	− 0.3~7	V
V_I	Input voltage	With respect to GND	− 0.3*~V_{CC} + 0.3	V
V_O	Output voltage	With respect to GND	0~V_{CC}	V
P_d	Power dissipation	Ta = 25℃	700	mW
T_{opr}	Operating temperature		0~70	℃
T_{stg}	Storage temperature		− 65~150	℃

* − 3.0V in case of AC (Pulse width ≦ 30ns)

DC ELECTRICAL CHARACTERISTICS (Ta = 0~70℃, V_{CC} = 5V ± 10%, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits Min	Limits Typ	Limits Max	Unit
V_{IH}	High-level input voltage			2.2		V_{CC}+0.3	V
V_{IL}	Low-level input voltage			− 0.3*		0.8	V
V_{OH1}	High-level output voltage 1	I_{OH} = − 1mA		2.4			V
V_{OH2}	High-level output voltage 2	I_{OH} = − 0.1mA		V_{CC}−0.5			V
V_{OL}	Low-level output voltage	I_{OL} = 2mA				0.4	V
I_I	Input leakage current	V_I = 0~V_{CC}				± 1	μA
I_O	Output leakage current	$\overline{S}$ = V_{IH} or $\overline{OE}$ = V_{IH}, $V_{I/O}$ = 0~V_{CC}				± 1	μA
I_{CC1}	Active supply current (AC, MOS level)	$\overline{S}$ ≦ 0.2V Other inputs ≦ 0.2V or ≧ V_{CC} − 0.2V Output open Min.cycle	55ns		35	55	mA
			70ns		30	50	
I_{CC2}	Active supply current (AC, TTL level)	$\overline{S}$ = V_{IL} Other inputs = V_{IH} or V_{IL} Output open Min.cycle	55ns		40	60	mA
			70ns		35	55	
I_{CC3}	Stand-by supply current	$\overline{S}$ ≧ V_{CC} − 0.2V, Other inputs = 0~V_{CC}	-LL			20	μA
			-XL		0.1	5	μA
I_{CC4}	Stand-by supply current	$\overline{S}$ = V_{IH}, Other inputs = 0~V_{CC}				3	mA

* − 3.0V in case of AC (Pulse width 30ns)

CAPACITANCE (Ta = 0~70℃, V_{CC} = 5V ± 10%, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits Min	Limits Typ	Limits Max	Unit
C_I	Input capacitance (Ta = 25℃)	V_I = GND, V_I = 25mVrms, f = 1MHz			6	pF
C_O	Output capacitance (Ta = 25℃)	V_O = GND, V_O = 25mVrms, f = 1MHz			8	pF

Note 1. Direction for current flowing into IC is indicated as positive. (no mark)
2. Typical value is V_{CC} = 5V, Ta = 25℃.
3. C_I, C_O are periodically sampled and are not 100% tested.

AC ELECTRICAL CHARACTERISTICS (T_a = 0~70℃, V_{CC} = 5V ± 10%, unless otherwise noted)

(1) MEASUREMENT CONDITONS

Input pulse level·····V_{IH} = 2.4V, V_{IL} = 0.6V

Input rise and fall time ·····5ns

Reference level·····V_{OH} = V_{OL} = 1.5V

Transition is measured ± 500mV from steady state voltage.(for t_{en}, t_{dis})

Output loads·····Fig.1. C_L = 50pF

C_L = 5pF (for t_{en}, t_{dis})

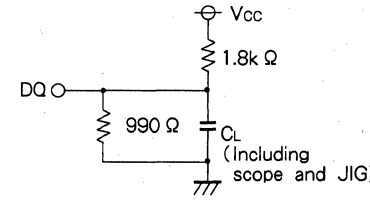


Fig.1 Output load

(2) READ CYCLE

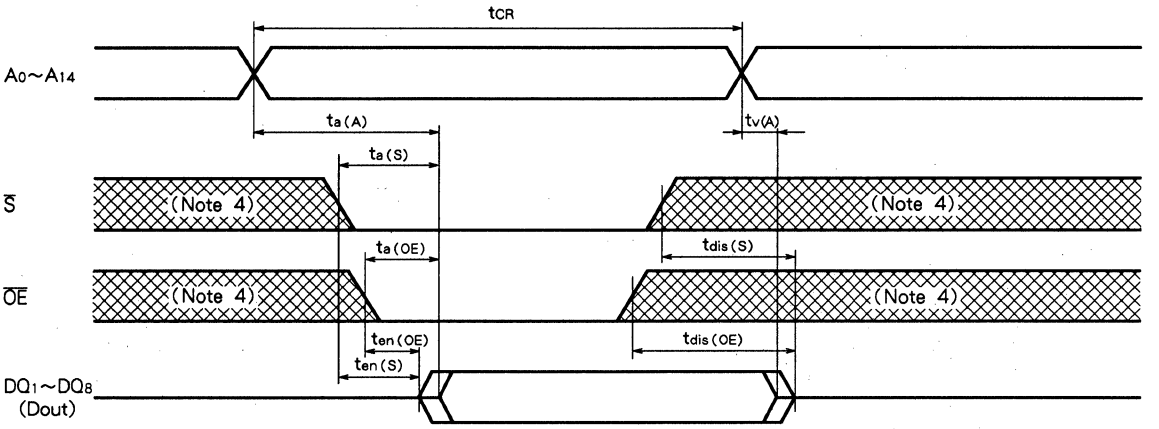
Symbol	Parameter	Limits						Unit
		M5M5256C-55LL M5M5256C-55XL			M5M5256C-70LL M5M5256C-70XL			
		Min	Typ	Max	Min	Typ	Max	
t_{CR}	Read cycle time	55			70			ns
$t_{a(A)}$	Address access time			55			70	ns
$t_{a(S)}$	Chip select access time			55			70	ns
$t_{a(OE)}$	Output enable access time			30			35	ns
$t_{dis(S)}$	Output disable time after $\overline{S}$ high			20			25	ns
$t_{dis(OE)}$	Output disable time after $\overline{OE}$ high			20			25	ns
$t_{en(S)}$	Output enable time after $\overline{S}$ low	5			5			ns
$t_{en(OE)}$	Output enable time after $\overline{OE}$ low	5			5			ns
$t_{v(A)}$	Data valid time after address	10			10			ns

(3) WRITE CYCLE

Symbol	Parameter	Limits						Unit
		M5M5256C-55LL M5M5256C-55XL			M5M5256C-70LL M5M5256C-70XL			
		Min	Typ	Max	Min	Typ	Max	
t_{CW}	Write cycle time	55			70			ns
$t_{w(W)}$	Write pulse width	45			55			ns
$t_{su(A)}$	Address set up time	0			0			ns
$t_{su(A-WH)}$	Address set up time with respect to $\overline{W}$ high	50			65			ns
$t_{su(S)}$	Chip select set up time	50			65			ns
$t_{su(D)}$	Data set up time	25			30			ns
$t_{h(D)}$	Data hold time	0			0			ns
$t_{rec(W)}$	Write recovery time	0			0			ns
$t_{dis(W)}$	Output disable time after $\overline{W}$ low			20			25	ns
$t_{dis(OE)}$	Output disable time after $\overline{OE}$ high			20			25	ns
$t_{en(W)}$	Output enable time after $\overline{W}$ high	5			5			ns
$t_{en(OE)}$	Output enable time after $\overline{OE}$ low	5			5			ns

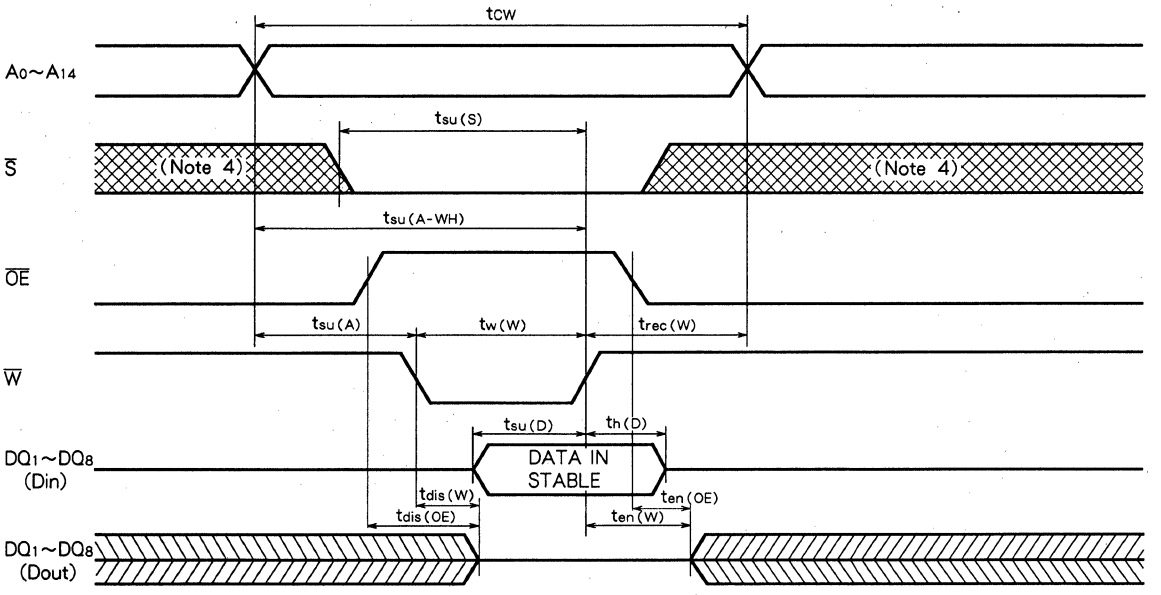
(4) TIMING DIAGRAMS

Read Cycle

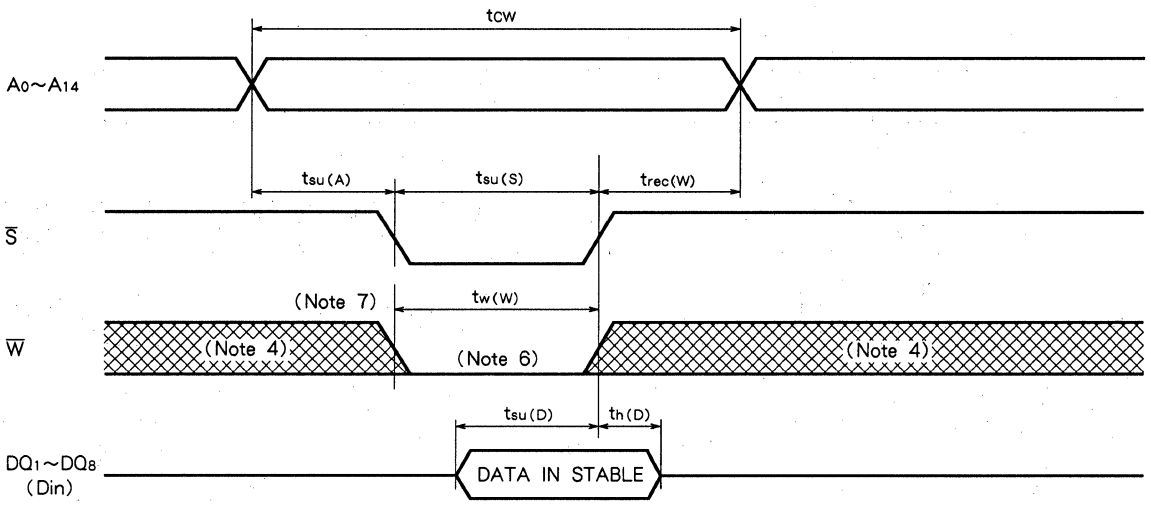


W = "H"level

Write cycle (W control mode)



Write cycle ($\overline{S}$ control mode)



Note 4. Hatching indicates the state is don't care.
5. Writing is executed in overlap of $\overline{S}$ and $\overline{W}$ low.
6. If $\overline{W}$ goes low simultaneously with or prior to $\overline{S}$, the output remains in the high-impedance state.
7. Don't apply inverted phase signal externally when DQ pin is in output mode.
8. t_{en}, t_{dis} are periodically sampled and are not 100% tested.

POWER DOWN CHARACTERISTICS

(1) ELECTRICAL CHARACTERISTICS (T_a = 0~70℃, V_{CC} = 5V ± 10%, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ	Max	
$V_{CC(PD)}$	Power down supply voltage			2			V
$V_{I(\overline{S})}$	Chip select input $\overline{S}$	2.2V ≦ $V_{CC(PD)}$		2.2			V
		2V ≦ $V_{CC(PD)}$ ≦ 2.2V			$V_{CC(PD)}$		
$I_{CC(PD)}$	Power down supply current	V_{CC} = 3V	-LL			10*	μA
		Other inputs = 3V	-XL		0.05	2**	μA

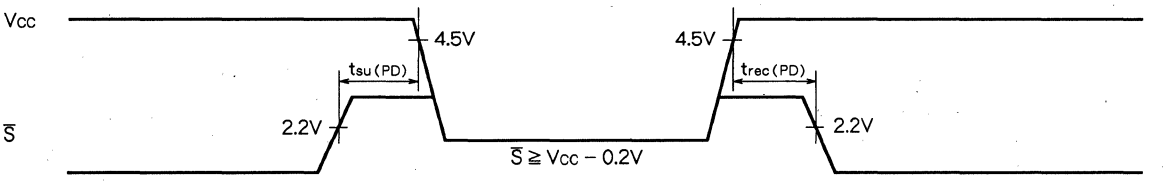
* T_a = 25℃, $I_{CC(PD)}$ = 1 μA
** T_a = 25℃, $I_{CC(PD)}$ = 0.2 μA

(2) TIMING REQUIREMENTS (T_a = 0~70℃, V_{CC} = 5V ± 10%, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{su(PD)}$	Power down set up time		0			ns
$t_{rec(PD)}$	Power down recovery time		t_{CR}			ns

(3) POWER COWN CHARACTERISTICS

$\overline{S}$ control mode



M5M5256CP,FP,KP,VP,RV-85LL,-85XL, -10LL,-10XL

262144-BIT(32768-WORD BY 8-BIT)CMOS STATIC RAM

DESCRIPTION

This M5M5256CP, FP, KP, VP, RV is a 262144-bit CMOS static RAMs organized as 32768-words by 8-bits which is fabricated using high-performance 3 polysilicon CMOS technology. The use of resistive load NMOS cells and CMOS periphery result in a high-density and low-power static RAM. Stand-by current is small enough for battery back-up applicaton. It is ideal for the memory systems which require simple interface.

Especially the M5M5256CVP, RV are packaged in a 28-pin thin small outline package. Two types of devices are available, M5M5256CVP (normal lead bend type package) and M5M5256CRV (reverse lead bend type package). Using both type of devices, it becomes very easy to design a printed circuit board.

FEATURES

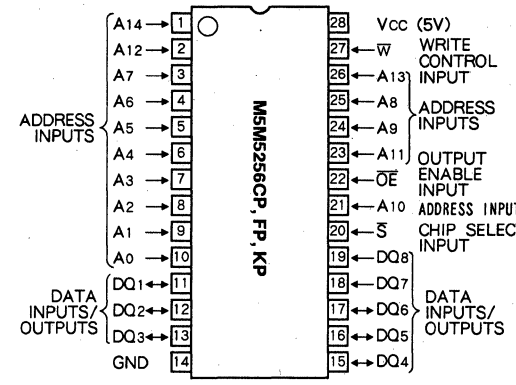
Type name	Access time (max)	Power supply current	
		Active (max)	Stand-by (max)
M5M5256CP, FP, KP, VP, RV-85LL	85ns	50mA (Vcc=5.5V)	20 μA (Vcc = 5.5V)
M5M5256CP, FP, KP, VP, RV-10LL	100ns		
M5M5256CP, FP, KP, VP, RV-85XL	85ns		5 μA (Vcc = 5.5V) 0.05 μA (Vcc = 3V, typ)
M5M5256CP, FP, KP, VP, RV-10XL	100ns		

- Single +5V power supply
- No clocks, no refresh
- Data-hold on +2V power supply
- Directly TTL compatible : All inputs and outputs
- Three-state outputs : OR-tie capability
- Simple memory expansion by $\overline{S}$
- $\overline{OE}$ prevents data contention in the I/O bus
- Common data I/O
- Low stand-by current ..... 0.05 μA (typ)
- Package
  - M5M5256CP ..... 28 pin 600 mil DIP
  - M5M5256CKP ..... 28 pin 300 mil DIP
  - M5M5256CFP ..... 28 pin 450 mil SOP
  - M5M5256CVP, RV ..... 28pin 8 × 13.4mm² TSOP

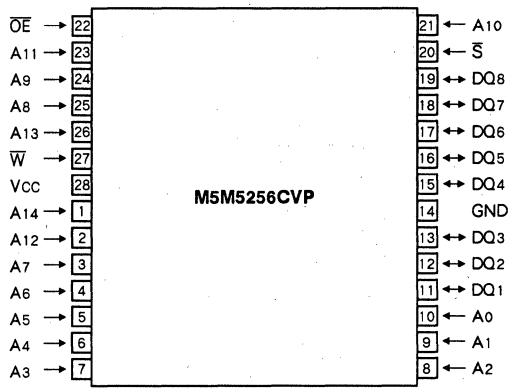
APPLICATION

Small capacity memory units

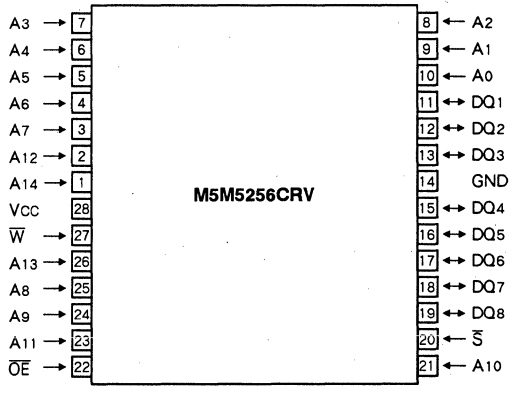
PIN CONFIGURATION (TOP VIEW)



Outline 28P4(P)
28P2W-C(FP)
28P4Y(KP)



Outline 28P2C-A



Outline 28P2C-B

262144-BIT(32768-WORD BY 8-BIT)CMOS STATIC RAM

FUNCTION

The operation mode of the M5M5256CP, FP, KP, VP, RV is determined by a combination of the device control inputs $\overline{S}$, $\overline{W}$ and $\overline{OE}$. Each mode is summariezed in the function table.

A write cycle is executed whenever the low level $\overline{W}$ overlaps with the low level $\overline{S}$. The address must be set-up before the write cycle and must be stable during the entire cycle. The data is latched into a cell on the trailing edge of $\overline{W}$, $\overline{S}$, whichever occurs first, requiring the set-up and hold time relative to these edge to be maintained. The output enable $\overline{OE}$ directly controls the output stage. Setting the $\overline{OE}$ at a high level, the output stage is in a high-impedance state, and the data bus contention problem in the write cycle is eliminated.

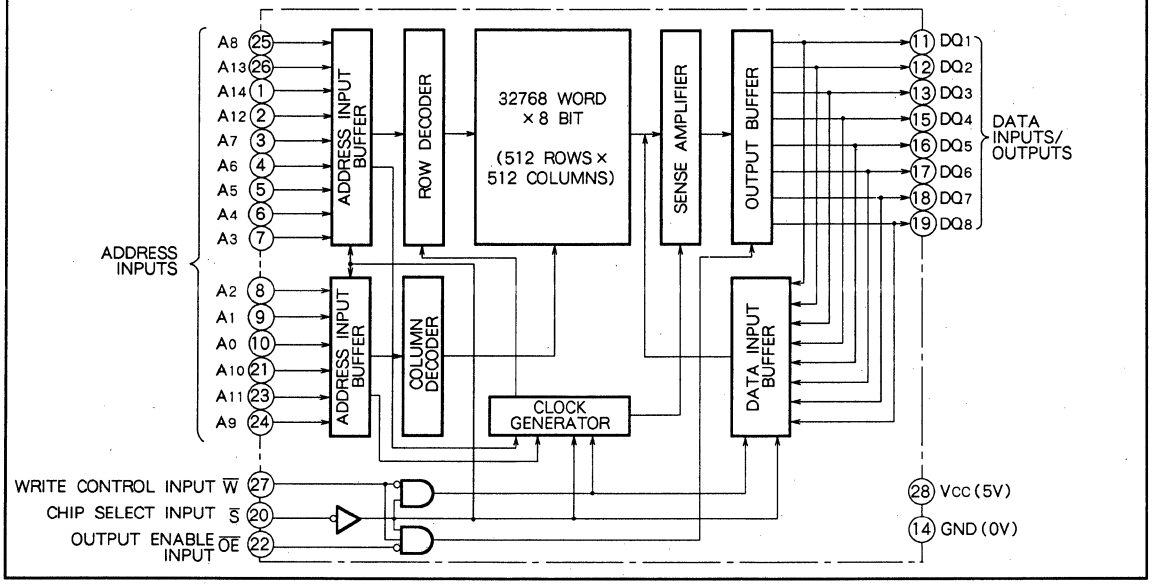
A read cycle is executed by setting $\overline{W}$ at a high level and $\overline{OE}$ at a low level while $\overline{S}$ are in an active state.

When setting $\overline{S}$ at a high level, the chip is in a non-selectable mode in which both reading and writing are disabled. In this mode, the output stage is in a high-impedance state, allowing OR-tie with other chips and memory expansion by $\overline{S}$. The power supply current is reduced as low as the stand-by current which is specified as I_{CC3} or I_{CC4}, and the memory data can be held +2V power supply, enabling battery back-up operation during power failure or power-down operation in the non-selected mode.

FUNCTION TABLE

$\overline{S}$	$\overline{W}$	$\overline{OE}$	Mode	DQ	Icc
H	X	X	Non selection	High-impedance	Stand-by
L	L	X	Write	Din	Active
L	H	L	Read	Dout	Active
L	H	H		High-impedance	Active

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to GND	− 0.3~7	V
V_I	Input voltage	With respect to GND	− 0.3*~V_{CC} + 0.3	V
V_O	Output voltage	With respect to GND	0~V_{CC}	V
P_d	Power dissipation	Ta = 25℃	700	mW
T_{opr}	Operating temperature		0~70	℃
T_{stg}	Storage temperature		− 65~150	℃

* − 3.0V in case of AC (Pulse width ≦ 30ns)

DC ELECTRICAL CHARACTERISTICS (Ta = 0~70℃, V_{CC} = 5V ± 10%, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits Min	Limits Typ	Limits Max	Unit
V_{IH}	High-level input voltage			2.2		V_{CC}+0.3	V
V_{IL}	Low-level input voltage			− 0.3*		0.8	V
V_{OH1}	High-level output voltage 1	I_{OH} = − 1mA		2.4			V
V_{OH2}	High-level output voltage 2	I_{OH} = − 0.1mA		V_{CC}-0.5			V
V_{OL}	Low-level output voltage	I_{OL} = 2mA				0.4	V
I_I	Input leakage current	V_I = 0~V_{CC}				± 1	μA
I_O	Output leakage current	$\overline{S}$ = V_{IH} or $\overline{OE}$ = V_{IH}, $V_{I/O}$ = 0~V_{CC}				± 1	μA
I_{CC1}	Active supply current (AC, MOS level)	$\overline{S}$ ≦ 0.2V Other inputs ≦ 0.2V or ≧ V_{CC} − 0.2V Output open	Min.cycle		30	45	mA
			1MHz		4	8	mA
I_{CC2}	Active supply current (AC, TTL level)	$\overline{S}$ = V_{IL} Other inputs = V_{IL} or V_{IH} Output open	Min.cycle		35	50	mA
			1MHz		5	10	mA
I_{CC3}	Stand-by supply current	$\overline{S}$ ≧ V_{CC} − 0.2V Other inputs = 0~V_{CC}	-LL			20	μA
			-XL		0.1	5	μA
I_{CC4}	Stand-by supply current	$\overline{S}$ = V_{IH}, Other inputs = 0~V_{CC}				3	mA

* − 3.0V in case of AC (Pulse width 30ns)

CAPACITANCE (Ta = 0~70℃, V_{CC} = 5V ± 10%, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits Min	Limits Typ	Limits Max	Unit
C_I	Input capacitance (Ta = 25℃)	V_I = GND, V_I = 25mVrms, f = 1MHz			6	pF
C_O	Output capacitance (Ta = 25℃)	V_O = GND, V_O = 25mVrms, f = 1MHz			8	pF

Note 1. Direction for current flowing into IC is indicated as positive. (no mark)
2. Typical value is V_{CC} = 5V, Ta = 25℃.
3. C_I, C_O are periodically sampled and are not 100% tested.

AC ELECTRICAL CHARACTERISTICS (T_a = 0~70℃, V_{CC} = 5V ± 10%, unless otherwise noted)

(1) MEASUREMENT CONDITIONS

Input pulse level ····· V_{IH} = 2.4V, V_{IL} = 0.6V

Input rise and fall time ····· 5ns

Reference level ····· V_{OH} = V_{OL} = 1.5V

Transition is measured ± 500mV from steady state voltage.(for t_{en}, t_{dis})

Output loads ····· Fig.1. C_L = 100pF

C_L = 5pF (for t_{en}, t_{dis})

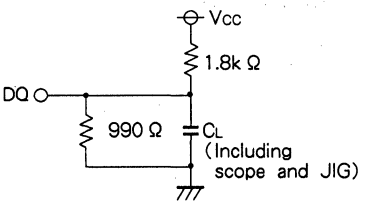


Fig.1 Output load

(2) READ CYCLE

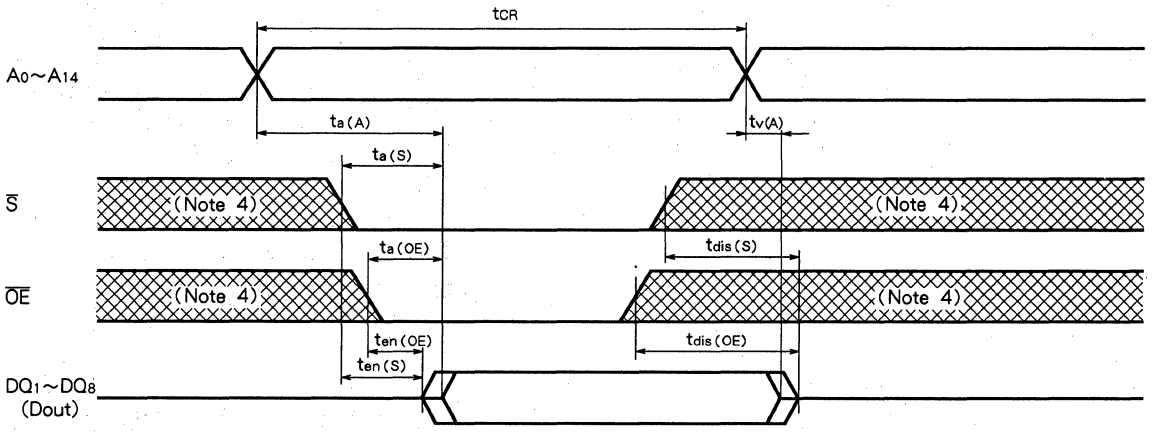
Symbol	Parameter	Limits						Unit
		M5M5256C-85LL M5M5256C-85XL			M5M5256C-10LL M5M5256C-10XL			
		Min	Typ	Max	Min	Typ	Max	
t_{CR}	Read cycle time	85			100			ns
$t_{a(A)}$	Address access time			85			100	ns
$t_{a(S)}$	Chip select access time			85			100	ns
$t_{a(OE)}$	Output enable access time			45			50	ns
$t_{dis(S)}$	Output disable time after $\overline{S}$ high			30			35	ns
$t_{dis(OE)}$	Output disable time after $\overline{OE}$ high			30			35	ns
$t_{en(S)}$	Output enable time after $\overline{S}$ low	10			10			ns
$t_{en(OE)}$	Output enable time after $\overline{OE}$ low	10			10			ns
$t_{v(A)}$	Data valid time after address	20			20			ns

(3) WRITE CYCLE

Symbol	Parameter	Limits						Unit
		M5M5256C-85LL M5M5256C-85XL			M5M5256C-10LL M5M5256C-10XL			
		Min	Typ	Max	Min	Typ	Max	
t_{CW}	Write cycle time	85			100			ns
$t_{w(W)}$	Write pulse width	60			70			ns
$t_{su(A)}$	Address set up time	0			0			ns
$t_{su(A-WH)}$	Address set up time with respect to $\overline{W}$ high	70			80			ns
$t_{su(S)}$	Chip select set up time	70			80			ns
$t_{su(D)}$	Data set up time	30			35			ns
$t_{h(D)}$	Data hold time	0			0			ns
$t_{rec(W)}$	Write recovery time	0			0			ns
$t_{dis(W)}$	Output disable time after $\overline{W}$ low			30			35	ns
$t_{dis(OE)}$	Output disable time after $\overline{OE}$ high			30			35	ns
$t_{en(W)}$	Output enable time after $\overline{W}$ high	10			10			ns
$t_{en(OE)}$	Output enable time after $\overline{OE}$ low	10			10			ns

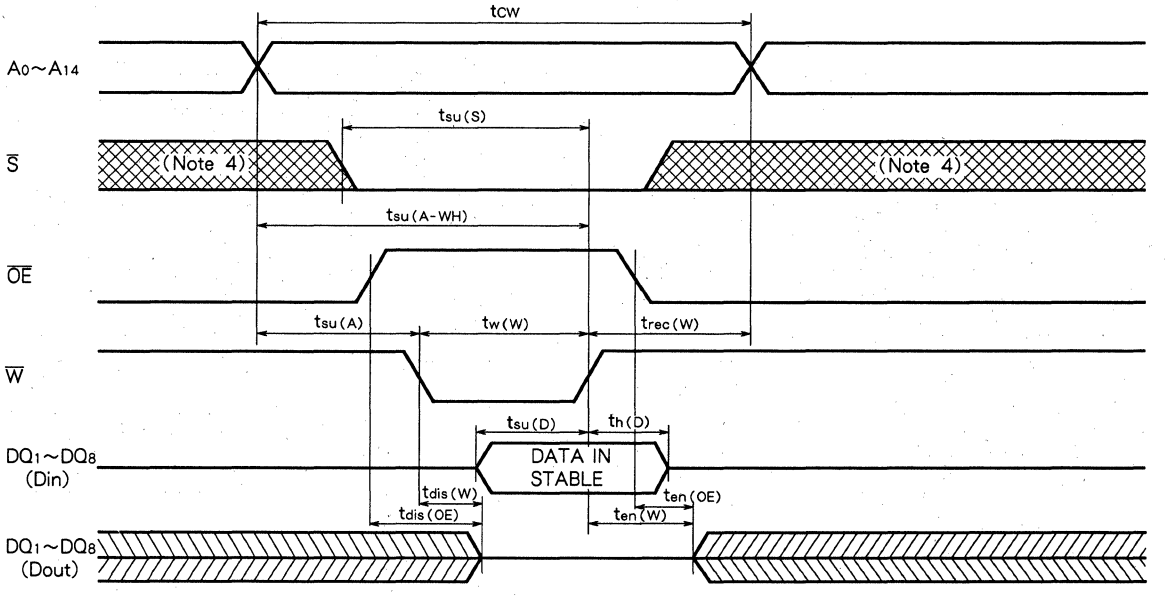
(4) TIMING DIAGRAMS

Read cycle

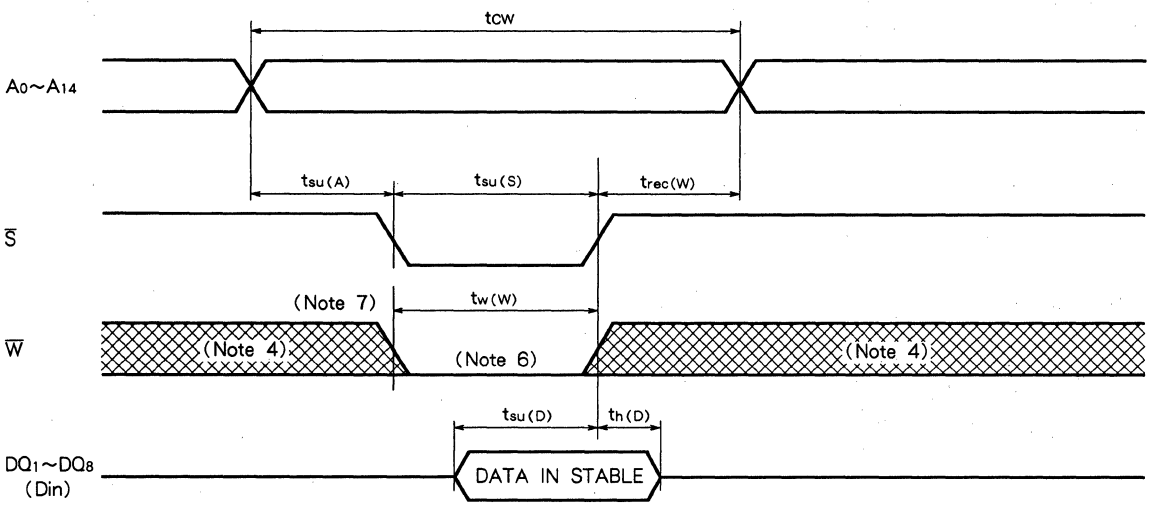


W = "H"level

Write cycle (W control mode)



Write cycle ($\overline{S}$ control mode)



Note 4. Hatching indicates the state is don't care.
5. Writing is executed in overlap of $\overline{S}$ and $\overline{W}$ low.
6. If $\overline{W}$ goes low simultaneously with or prior to $\overline{S}$, the output remains in the high-impedance state.
7. Don't apply inverted phase signal externally when DQ pin is in output mode.
8. ten, tdis are periodically sampled and are not 100% tested.

POWER DOWN CHARACTERISTICS

(1) ELECTRICAL CHARACTERISTICS (T_a = 0~70℃, V_{CC} = 5V ± 10%, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ	Max	
$V_{CC(PD)}$	Power down supply voltage			2			V
$V_{I(\overline{S})}$	Chip select input $\overline{S}$	2.2V ≦ $V_{CC(PD)}$		2.2			V
		2V ≦ $V_{CC(PD)}$ ≦ 2.2V			$V_{CC(PD)}$		
$I_{CC(PD)}$	Power down supply current	V_{CC} = 3V, Other inputs = 3V	-LL			10*	μA
			-XL		0.05	2**	μA

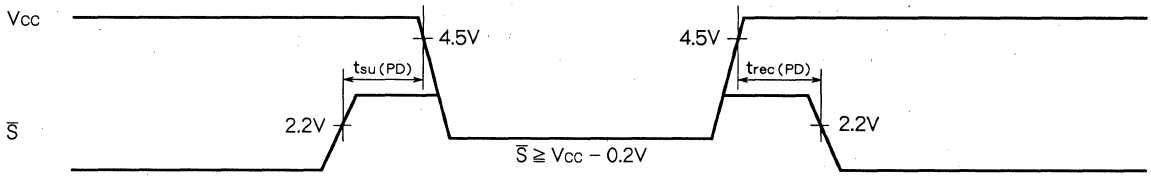
* T_a = 25℃, $I_{CC(PD)}$ = 1 μA
** T_a = 25℃, $I_{CC(PD)}$ = 0.2 μA

(2) TIMING REQUIREMENTS (T_a = 0~70℃, V_{CC} = 5V ± 10%, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{su(PD)}$	Power down set up time		0			ns
$t_{rec(PD)}$	Power down recovery time		t_{CR}			ns

(3) POWER DOWN CHARACTERISTICS

$\overline{S}$ control mode



M5M51008AP,FP,VP,RV-55L,-55LL

1048576-BIT(131072-WORD BY 8-BIT)CMOS STATIC RAM

DESCRIPTION

The M5M51008AP, FP, VP, RV are a 1048576-bit CMOS static RAM organized as 131072 word by 8-bit which are fabricated using high-performance triple polysilicon CMOS technology. The use of resistive load NMOS cells and CMOS periphery result in a high density and low power static RAM.

They are low stand-by current and low operation current and ideal for the battery back-up application.

The M5M51008AVP, RV are packaged in a 32-pin thin small outline package which is a high reliability and high density surface mount device (SMD). Two types of devices are available. M5M51008AVP (normal lead vend type package), M5M51008ARV (reverse lead vend type package). Using both types of devices, it becomes very easy to design a printed circuit board.

FEATURES

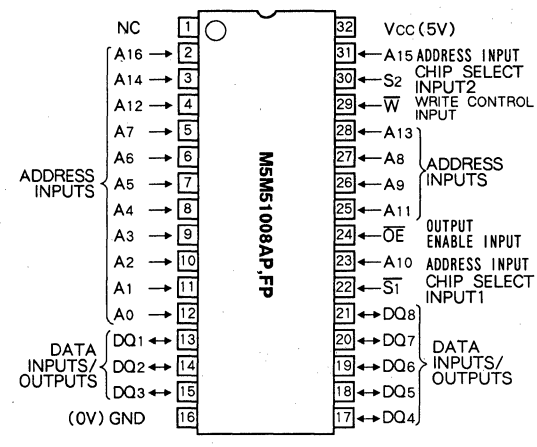
Type name	Access time (max)	Power supply current	
		Active (max)	Stand-by (max)
M5M51008AP, FP,VP,RV-55L	55ns	40mA (1MHz)	100 μA (Vcc = 5.5V)
M5M51008AP, FP,VP,RV-55LL	55ns		20 μA (Vcc = 5.5V) 0.3 μA (Vcc = 3.0V, typ)

- Single + 5V power supply
- Low stand-by current 0.3 μA (typ.)
- Directly TTL compatible : All inputs and outputs
- Easy memory expansion and power down by $\overline{S1}$,S2
- Data hold on + 2V power supply
- Three-state outputs : OR-tie capability
- $\overline{OE}$ prevents data contention in the I/O bus
- Common data I/O
- Package M5M51008AP ····· 32pin 600mil DIP
  M5M51008AFP ····· 32pin 525mil SOP
  M5M51008AVP, RV ···· 32pin 8 × 20mm² TSOP

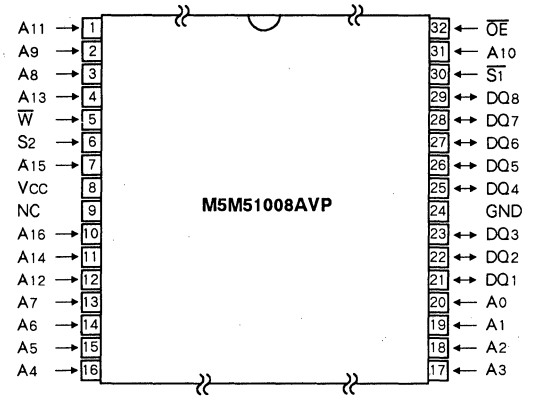
APPLICATION

Small capacity memory units

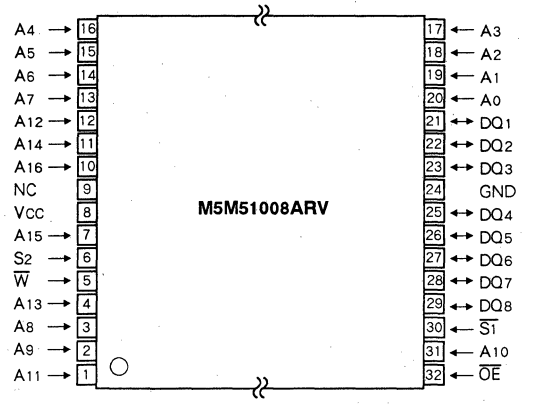
PIN CONFIGURATION (TOP VIEW)



Outline 32P4(P)
32P2M-A(FP)



Outline 32P3H-E



Outline 32P3H-F

NC : NO CONNECTION

FUNCTION

The operation mode of the M5M51008AP, FP, VP, RV are determined by a combination of the device control inputs $\overline{S_1}$, S_2, $\overline{W}$ and $\overline{OE}$. Each mode is summarized in the function table.

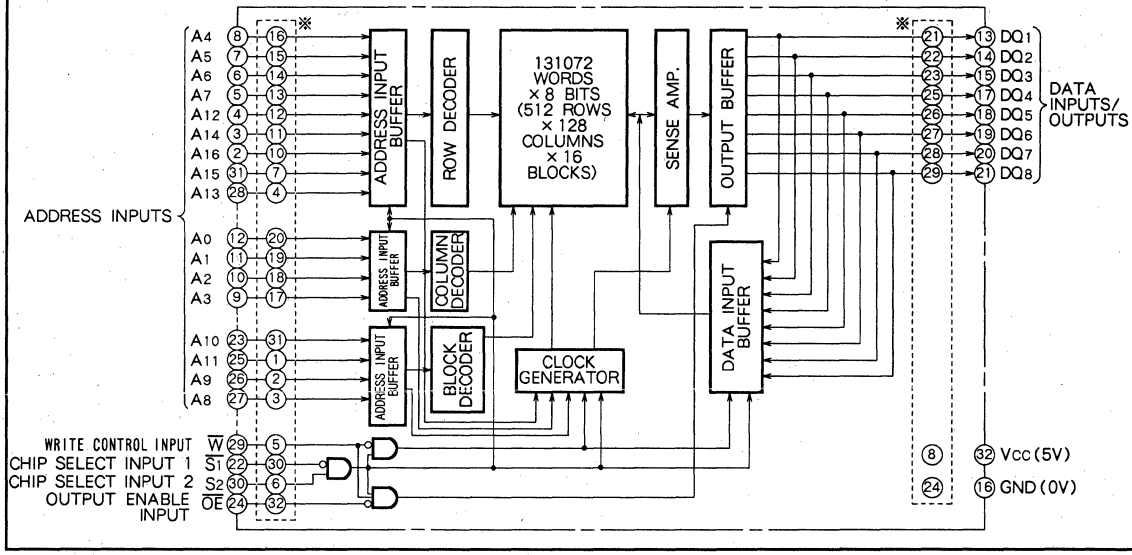
A write cycle is executed whenever the low level $\overline{W}$ overlaps with the low level $\overline{S_1}$ and the high level S_2. The address must be set up before the write cycle and must be stable during the entire cycle. The data is latched into a cell on the trailing edge of $\overline{W}$, $\overline{S_1}$ or S_2, whichever occurs first, requiring the set-up and hold time relative to these edge to be maintained. The output enable input $\overline{OE}$ directly controls the output stage. Setting the $\overline{OE}$ at a high level, the output stage is in a high-impedance state, and the data bus contention problem in the write cycle is eliminated.

A read cycle is executed by setting $\overline{W}$ at a high level and $\overline{OE}$ at a low level while $\overline{S_1}$ and S_2 are in an active state ($\overline{S_1}$ = L, S_2 = H)

When setting $\overline{S_1}$ at a high level or S_2 at a low level, the chip are in a non-selectable mode in which both reading and writing are disabled. In this mode, the output stage is in a high-impedance state, allowing OR-tie with other chips and memory expansion by $\overline{S_1}$ and S_2. The power supply current is reduced as low as the stand-by current which is specified as I_{CC3} or I_{CC4}, and the memory data can be held at +2V power supply, enabling battery back-up operation during power failure or power-down operation in the non-selected mode.

$\overline{S_1}$	S_2	$\overline{W}$	$\overline{OE}$	Mode	DQ	Icc
X	L	X	X	Non selection	High-impedance	Stand-by
H	X	X	X	Non selection	High-impedance	Stand-by
L	H	L	X	Write	D_{in}	Active
L	H	H	L	Read	D_{out}	Active
L	H	H	H		High-impedance	Active

BLOCK DIAGRAM



※ Pin numbers inside dotted line show those of TSOP.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to GND	− 0.3*~7	V
V_I	Input voltage		− 0.3*~V_{CC} + 0.3	V
V_O	Output voltage		0~V_{CC}	V
P_d	Power dissipation	Ta = 25℃	700	mW
T_{opr}	Operating temperature		0~70	℃
T_{stg}	Storage temperature		− 65~150	℃

* − 3.0V in case of AC (Pulse width ≦ 30ns)

DC ELECTRICAL CHARACTERISTICS (Ta = 0~70℃, V_{CC} = 5V ± 10%, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits Min	Limits Typ	Limits Max	Unit
V_{IH}	High-level input voltage			2.2		V_{CC}+0.3	V
V_{IL}	Low-level input voltage			− 0.3*		0.8	V
V_{OH}	High-level output voltage	I_{OH} = − 1mA		2.4			V
		I_{OH} = − 0.1mA		V_{CC}-0.5			
V_{OL}	Low-level output voltage	I_{OL} = 2mA				0.4	V
I_I	Input leakage current	V_I = 0~V_{CC}				± 1	μA
I_O	Output leakage current	$\overline{S_1}$ = V_{IH} or S_2 = V_{IL} or $\overline{OE}$ = V_{IH}, $V_{I/O}$ = 0~V_{CC}				± 1	μA
I_{CC1}	Active supply current (AC, MOS level)	$\overline{S_1}$ ≦ 0.2V, S_2 ≧ V_{CC} − 0.2V Other inputs ≦ 0.2V or ≧ V_{CC} − 0.2V Output-open (duty 100%)	Min cycle		47	85	mA
			1MHz		22	35	
I_{CC2}	Active supply current (AC, TTL level)	$\overline{S_1}$ = V_{IL}, S_2 = V_{IH}, Other inputs = V_{IH} or V_{IL} Output-open (duty 100%)	Min cycle		50	90	mA
			1MHz		25	40	
I_{CC3}	Stand-by current	1) S_2 ≦ 0.2V, other inputs = 0~V_{CC}	-55L			100	μA
		2) $\overline{S_1}$ ≧ V_{CC} − 0.2V, S_2 ≧ V_{CC} − 0.2V, other inputs = 0~V_{CC}	-55LL		1.0	20	
I_{CC4}	Stand-by current	$\overline{S_1}$=V_{IH} or S_2=V_{IL}, other inputs=0~V_{CC}				3	mA

* − 3.0V in case of AC (Pulse width ≦ 30ns)

CAPACITANCE (Ta = 0~70℃, V_{CC} = 5V ± 10%, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits Min	Limits Typ	Limits Max	Unit
C_I	Input capacitance	V_I = GND, V_I = 25mVrms, f = 1MHz			6	pF
C_O	Output capacitance	V_O = GND, V_O = 25mVrms, f = 1MHz			8	pF

Note 1 : Direction for current flowing into an IC is positive (no mark).
2 : Typical value is V_{CC} = 5V, Ta = 25℃.

AC ELECTRICAL CHARACTERISTICS (T_a = 0~70℃, V_{CC} = 5V ± 10%, unless otherwise noted)

(1) MEASUREMENT CONDITIONS

Input pulse level·····V_{IH} = 3.0V, V_{IL} = 0.0V
Input rise and fall time·····5ns
Reference level·····V_{OH} = V_{OL} = 1.5V
Output loads·····Fig.1, C_L = 30pF
C_L = 5pF (for t_{en}, t_{dis})
Transition is measured ± 500mV from steady state voltage.(for t_{en}, t_{dis})

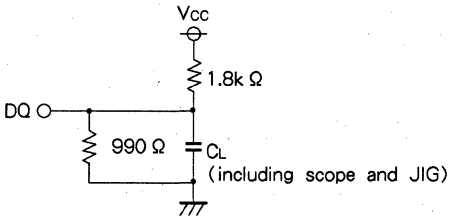


Fig.1 Output load

(2) READ CYCLE

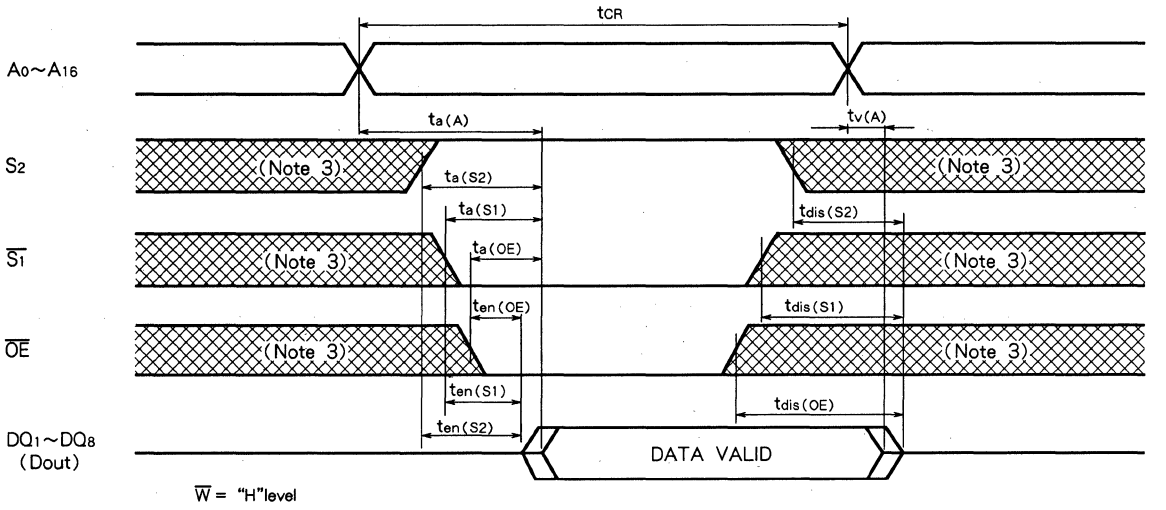
Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
t_{CR}	Read cycle time	55			ns
$t_{a(A)}$	Address access time			55	ns
$t_{a(S1)}$	Chip select 1 access time			55	ns
$t_{a(S2)}$	Chip select 2 access time			55	ns
$t_{a(OE)}$	Output enable access time			30	ns
$t_{dis(S1)}$	Output disable time after $\overline{S_1}$ high			20	ns
$t_{dis(S2)}$	Output disable time after S_2 low			20	ns
$t_{dis(OE)}$	Output disable time after $\overline{OE}$ high			20	ns
$t_{en(S1)}$	Output enable time after $\overline{S_1}$ low	5			ns
$t_{en(S2)}$	Output enable time after S_2 high	5			ns
$t_{en(OE)}$	Output enable time after $\overline{OE}$ low	5			ns
$t_{v(A)}$	Data valid time after address	5			ns

(3) WRITE CYCLE

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
t_{CW}	Write cycle time	55			ns
$t_{w(W)}$	Write pulse width	45			ns
$t_{su(A)}$	Address set up time	0			ns
$t_{su(A-WH)}$	Address set up time with respect to $\overline{W}$ high	50			ns
$t_{su(S1)}$	Chip select 1 set up time	50			ns
$t_{su(S2)}$	Chip select 2 set up time	50			ns
$t_{su(D)}$	Data set up time	25			ns
$t_{h(D)}$	Data hold time	0			ns
$t_{rec(W)}$	Write recovery time	0			ns
$t_{dis(W)}$	Output disable time from $\overline{W}$ low			20	ns
$t_{dis(OE)}$	Output disable time form $\overline{OE}$ high			20	ns
$t_{en(W)}$	Output enable time from $\overline{W}$ high	5			ns
$t_{en(OE)}$	Output enable time from $\overline{OE}$ low	5			ns

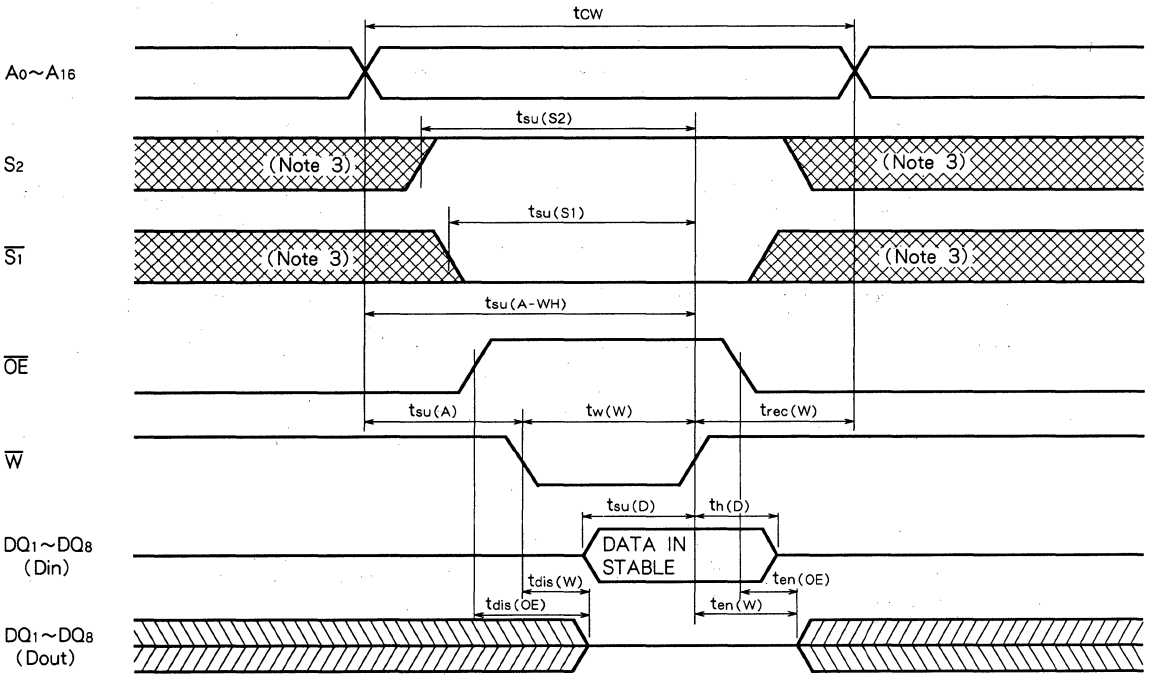
(4) TIMING DIAGRAMS

Read cycle

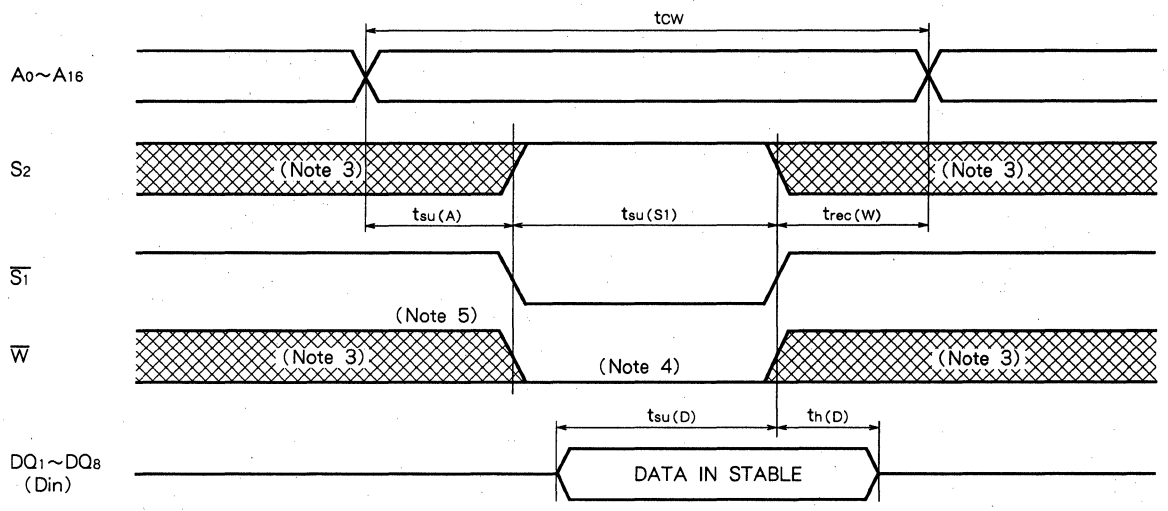


W = "H"level

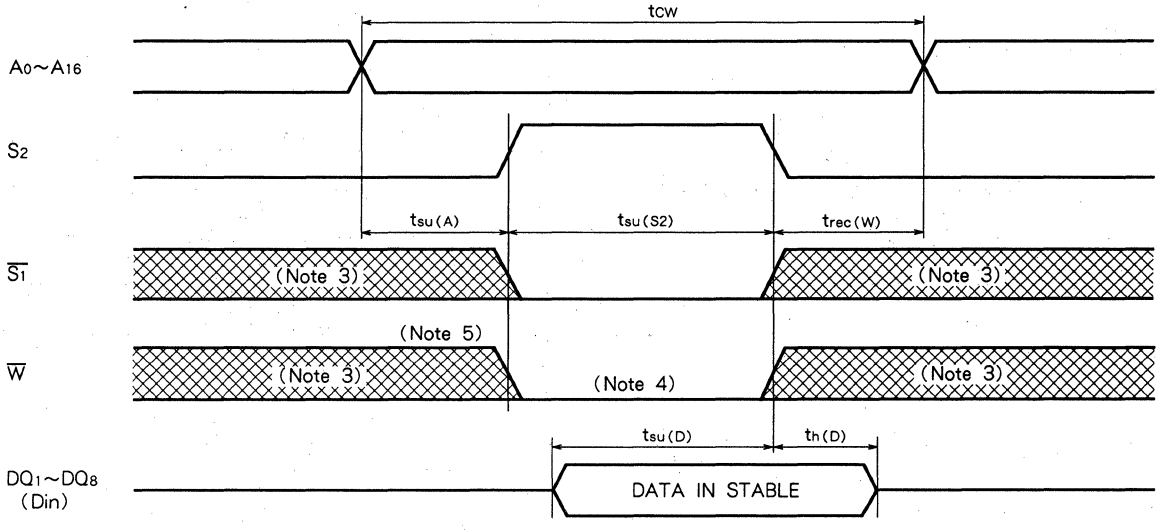
Write cycle
(W control mode)



Write cycle ($\overline{S_1}$ control mode)



Write cycle (S_2 control mode)



Note 3 : Hatching indicates the state is "don't care".
4 : Writing is executed while S2 high overlaps $\overline{S1}$ and $\overline{W}$ low.
5 : When the falling edge of $\overline{W}$ is simultaneously or prior to the falling edge of $\overline{S1}$ or rising edge of S2, the outputs are maintained in the high impedance state.
6 : Don't apply inverted phase signal externally when DQ pin is output mode.

POWER DOWN CHARACTERISTICS

(1) ELECTRICAL CHARACTERISTICS (T_a = 0~70℃, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ	Max	
$V_{CC(PD)}$	Power down supply voltage			2			V
$V_{I(\overline{ST})}$	Chip select input $\overline{S_1}$	2.2V ≦ $V_{CC(PD)}$		2.2			V
		2V ≦ $V_{CC(PD)}$ ≦ 2.2V			$V_{CC(PD)}$		
$V_{I(S2)}$	Chip select input S_2	4.5V ≦ $V_{CC(PD)}$				0.8	V
		$V_{CC(PD)}$ < 4.5				0.2	
$I_{CC(PD)}$	Power down supply current	V_{CC} = 3V 1) S_2 ≦ 0.2V, other inputs = 0~3V 2) $\overline{S_1}$ ≧ V_{CC} − 0.2V, S_2 ≧ V_{CC} − 0.2V, other inputs = 0~3V	-55L			50	μA
			-55LL		0.3	10 (Note 7)	

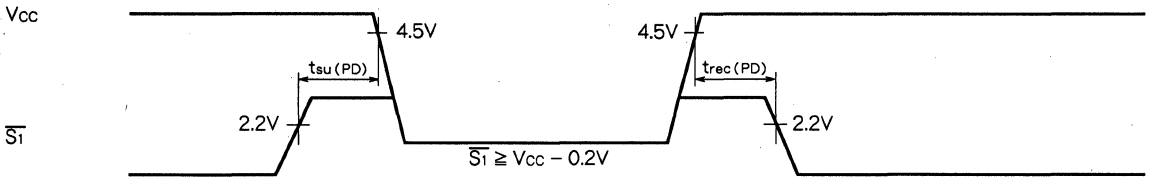
Note 7 : $I_{CC(PD)}$ = 1 μA in case of T_a = 25℃

(2) TIMING REQUIREMENTS (T_a = 0~70℃, unless otherwise noted)

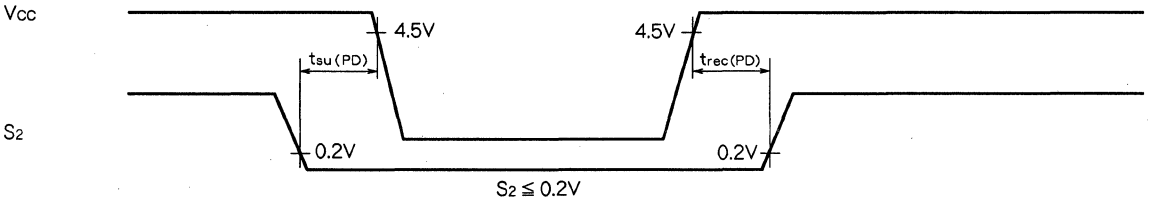
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{su(PD)}$	Power down set up time		0			ns
$t_{rec(PD)}$	Power down recovery time		5			ms

(3) POWER DOWN CHARACTERISTICS

$\overline{S_1}$ control mode



S_2 control mode



M5M51008AP,FP,VP,RV-70L,-85L,-10L, -12L,-70LL,-85LL,-10LL,-12LL

1048576-BIT(131072-WORD BY 8-BIT)CMOS STATIC RAM

DESCRIPTION

The M5M51008AP, FP, VP, RV are a 1048576-bit CMOS static RAM organized as 131072 word by 8-bit which are fabricated using high-performance triple polysilicon CMOS technology. The use of resistive load NMOS cells and CMOS periphery result in a high density and low power static RAM.

They are low stand-by current and low operation current and ideal for the battery back-up application.

The M5M51008AVP, RV are packaged in a 32-pin thin small outline package which is a high reliability and high density surface mount device (SMD). Two types of devices are available. M5M51008AVP (normal lead vend type package), M5M51008ARV (reverse lead vend type package). Using both types of devices, it becomes very easy to design a printed circut board.

FEATURES

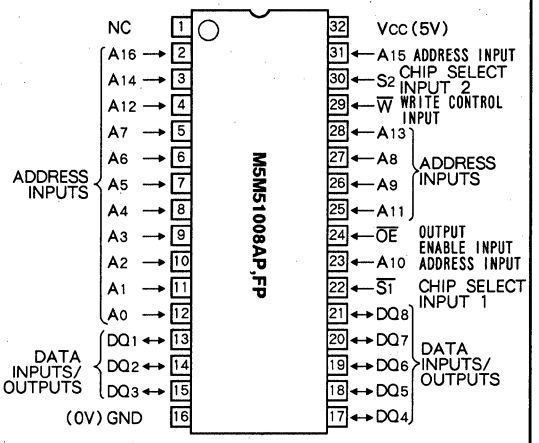
Type name	Access time (max)	Power supply current	
		Active (max)	Stand-by (max)
M5M51008AP, FP, VP, RV-70L M5M51008AP, FP, VP, RV-85L M5M51008AP, FP, VP, RV-10L M5M51008AP, FP, VP, RV-12L	70ns 85ns 100ns 120ns	15mA (1MHz)	100 μA (Vcc = 5.5V)
M5M51008AP, FP, VP, RV-70LL M5M51008AP, FP, VP, RV-85LL M5M51008AP, FP, VP, RV-10LL M5M51008AP, FP, VP, RV-12LL	70ns 85ns 100ns 120ns		20 μA (Vcc = 5.5V) 0.3 μA (Vcc = 3.0V, typ)

- Single + 5V power supply
- Low stand-by current 0.3 μA (typ.)
- Directly TTL compatible : All inputs and outputs
- Easy memory expansion and power down by $\overline{S1}$, S2
- Data hold on + 2v power supply
- Threee-state outputs : OR-tie capability
- $\overline{OE}$ prevents data contention in the I/O bus
- Common data I/O
- Package M5M51008AP ····· 32 pin 600mil DIP
  M5M51008AFP ····· 32 pin 525 mil SOP
  M5M51008AVP, RV ····· 32pin 8 × 20mm² TSOP

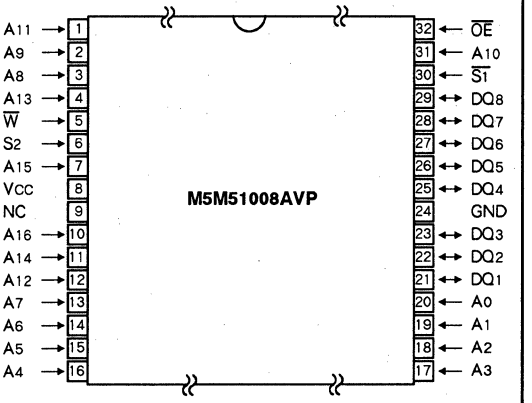
APPLICATION

Small capacity memory units

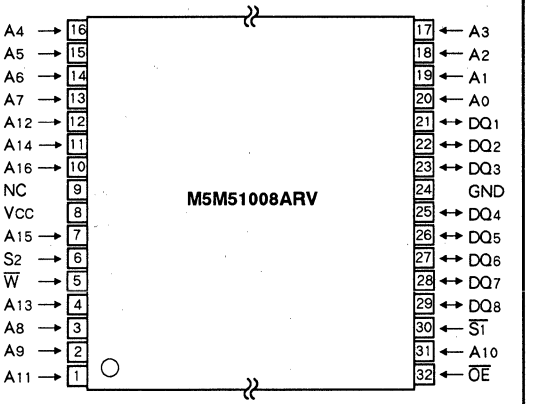
PIN CONFIGURATION (TOP VIEW)



Outline 32P4 (P)
32P2M-A (FP)



Outline 32P3H-E



Outline 32P3H-F

NC : NO CONNECTION

MITSUBISHI ELECTRIC

M5M51008AP,FP,VP,RV-70L,-85L,-10L, -12L,-70LL,-85LL,-10LL,-12LL

1048576-BIT(131072-WORD BY 8-BIT)CMOS STATIC RAM

FUNCTION

The operation mode of the M5M51008AP, FP, VP, RV are determined by a combination of the device control inputs $\overline{S1}$, S2, $\overline{W}$ and $\overline{OE}$. Each mode is summarized in the function table.

A write cycle is executed whenever the low level $\overline{W}$ overlaps with the low level $\overline{S1}$ and the high level S2. The address must be set up before the write cycle and must be stable during the entire cycle. The data is latched into a cell on the trailing edge of $\overline{W}$, $\overline{S1}$ or S2, whichever occurs first, requiring the set-up and hold time relative to these edge to be maintained. The output enable input $\overline{OE}$ directly controls the output stage. Setting the $\overline{OE}$ at a high level, the output stage is in a high-impedance state, and the data bus contention problem in the write cycle is eliminated.

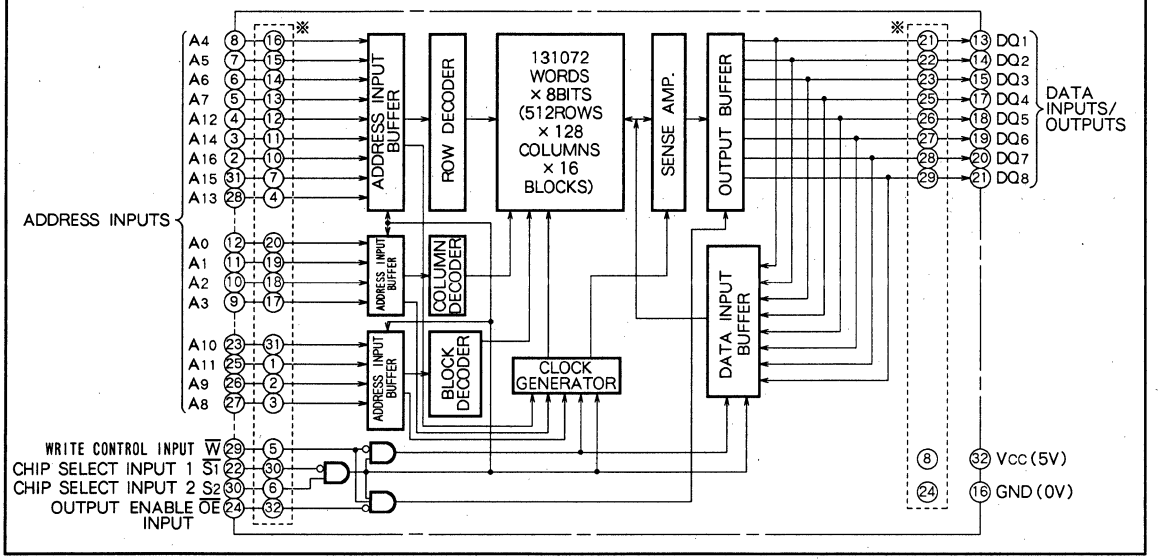
A read cycle is executed by setting $\overline{W}$ at a high level and $\overline{OE}$ at a low level while $\overline{S1}$ and S2 are in an active state ($\overline{S1}$ = L, S2 = H).

When setting $\overline{S1}$ at a high level or S2 at a low level, the chips are in a non-selectable mode in which both reading and writing are disabled. In this mode, the output state is in a high-impedance state, allowing OR-tie with other chips and memory expansion by $\overline{S1}$ and S2. The power supply current is reduced as low as the stand-by current which is specified as I_{CC3} or I_{CC4}, and the memory data can be held at + 2V power supply, enabling battery back-up operation during power failure or power-down operation in the non-selected mode.

FUNCTION TABLE

$\overline{S1}$	S2	$\overline{W}$	$\overline{OE}$	Mode	DQ	Icc
X	L	X	X	Non selection	High-impedance	Stand-by
H	X	X	X	Non selection	High-impedance	Stand-by
L	H	L	X	Write	Din	Active
L	H	H	L	Read	Dout	Active
L	H	H	H		High-impedance	Active

BLOCK DIAGRAM



※ Pin numbers inside dotted line show those of TSOP.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to GND	− 0.3~7	V
V_I	Input voltage		− 0.3*~V_{CC} + 0.3	V
V_O	Output voltage		0~V_{CC}	V
P_d	Power dissipation	Ta = 25℃	700	mW
T_{opr}	Operating temperature		0~70	℃
T_{stg}	Storage temperature		− 65~150	℃

* − 3.0V incase of AC (Pulse width ≦ 50ns)

DC ELECTRICAL CHARACTERISTICS (Ta = 0~70℃, V_{CC} = 5V ± 10%, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits Min	Limits Typ	Limits Max	Unit
V_{IH}	High-level input voltage			2.2		V_{CC}+0.3	V
V_{IL}	Low-level input voltage			− 0.3*		0.8	V
V_{OH}	High-level output voltage	I_{OH} = − 1mA		2.4			V
		I_{OH} = − 0.1mA		V_{CC}−0.5			
V_{OL}	Low-level output voltage	I_{OL} = 2mA				0.4	V
I_I	Intput leakage current	V_I = 0~V_{CC}				± 1	μA
I_O	Output leakage current	$\overline{S_1}$ = V_{IH} or S_2 = V_{IL} or $\overline{OE}$ = V_{IH}, $V_{I/O}$ = 0~V_{CC}				± 1	μA
I_{CC1}	Active supply current (AC, MOS level)	$\overline{S_1}$ ≦ 0.2V, S_2 ≧ V_{CC} − 0.2V Other inputs ≦ 0.2V or ≧ V_{CC} − 0.2V Output-open (duty 100%)	Min cycle		38	70	mA
			1MHz		5	15	
I_{CC2}	Active supply current (AC, TTL level)	$\overline{S_1}$ = V_{IL}, S_2 = V_{IH}, Other inputs = V_{IH} or V_{IL} Output-open (duty 100%)	Min cycle		40	70	mA
			1MHz		7	15	
I_{CC3}	Stand-by current	1) S_2 ≦ 0.2V, other inputs = 0~V_{CC} 2) $\overline{S_1}$ ≧ V_{CC} − 0.2V, S_2 ≧ V_{CC} − 0.2V, Other inputs = 0~V_{CC}	-L			100	μA
			-LL		1.0	20	
I_{CC4}	Stand-by current	$\overline{S_1}$ = V_{IH} or S_2 = V_{IL} Other inputs = 0~V_{CC}				3	mA

* − 3.0V incase of AC (Pulse width ≦ 50ns)

CAPACITANCE (Ta = 0~70℃, V_{CC} = 5V ± 10%, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits Min	Limits Typ	Limits Max	Unit
C_I	Input capacitance	V_I = GND, V_I = 25mV_{rms}, f = 1MHz			6	pF
C_O	Output capacitance	V_O = GND, V_O = 25mV_{rms}, f = 1MHz			8	pF

Note 1 : Direction for current flowing into an IC is positive (no mark)
2 : Typical value is V_{CC} = 5V, Ta = 25℃

AC ELECTRICAL CHARACTERISTICS (T_a = 0~70℃, V_{CC} = 5V ± 10%, unless otherwise noted)

(1) MEASUREMENT CONDITIONS

Input pulse level····· V_{IH} = 2.4V, V_{IL} = 0.6V
Input rise and fall time·····5ns
Reference level····· V_{OH} = V_{OL} = 1.5V
Transition is measured ± 500mV from steady state voltage.(for t_{en}, t_{dis})
Output loads·····Fig. 1, C_L = 100pF (P, FP, VP, RV-85L, -10L, -12L, -85LL, -10LL, -12LL)
C_L = 30pF (P, FP, VP, RV-70L, -70LL)
C_L = 5pF (for t_{en}, t_{dis})

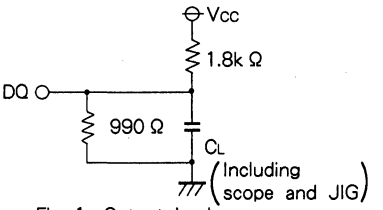


Fig. 1 Output load

(2) READ CYCLE

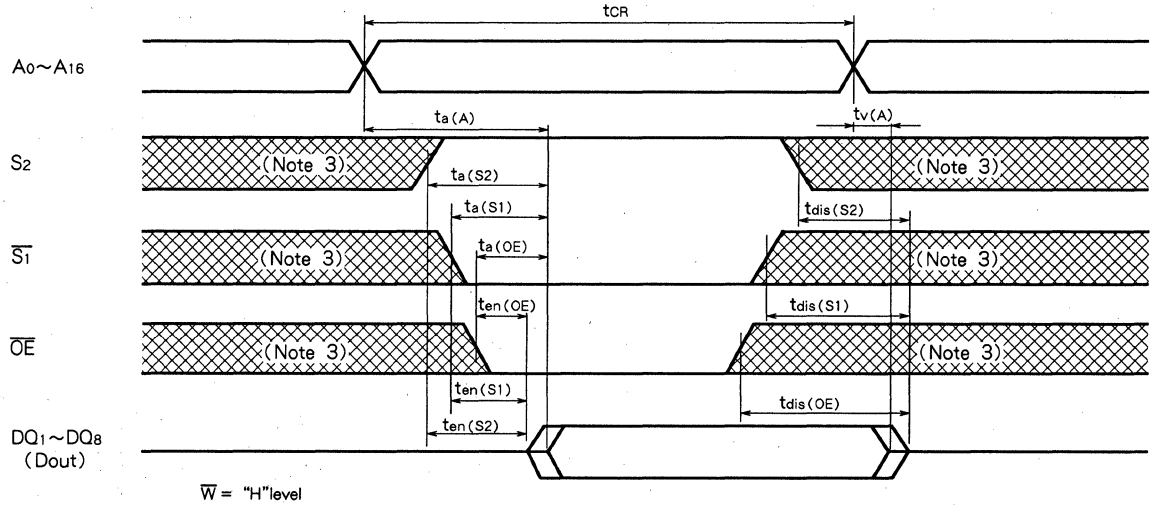
Symbol	Parameter	Limits								Unit
		M5M51008AP, FP, VP, RV-70L, -70LL		M5M51008AP, FP, VP, RV-85L, -85LL		M5M51008AP, FP, VP, RV-10L, -10LL		M5M51008AP, FP, VP, RV-12L, -12LL		
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{CR}	Read cycle time	70		85		100		120		ns
$t_{a(A)}$	Address access time		70		85		100		120	ns
$t_{a(S1)}$	Chip select 1 access time		70		85		100		120	ns
$t_{a(S2)}$	Chip select 2 access time		70		85		100		120	ns
$t_{a(OE)}$	Output enable access time		35		45		50		60	ns
$t_{dis(S1)}$	Output disable time after $\overline{S1}$ high		25		30		35		40	ns
$t_{dis(S2)}$	Output disable time after S_2 low		25		30		35		40	ns
$t_{dis(OE)}$	Output disable time after $\overline{OE}$ high		25		30		35		40	ns
$t_{en(S1)}$	Output enable time after $\overline{S1}$ low	10		10		10		10		ns
$t_{en(S2)}$	Output enable time after S_2 high	10		10		10		10		ns
$t_{en(OE)}$	Output enable time after $\overline{OE}$ low	5		5		5		5		ns
$t_{v(A)}$	Data valid time after address	10		10		10		10		ns

(3) WRITE CYCLE

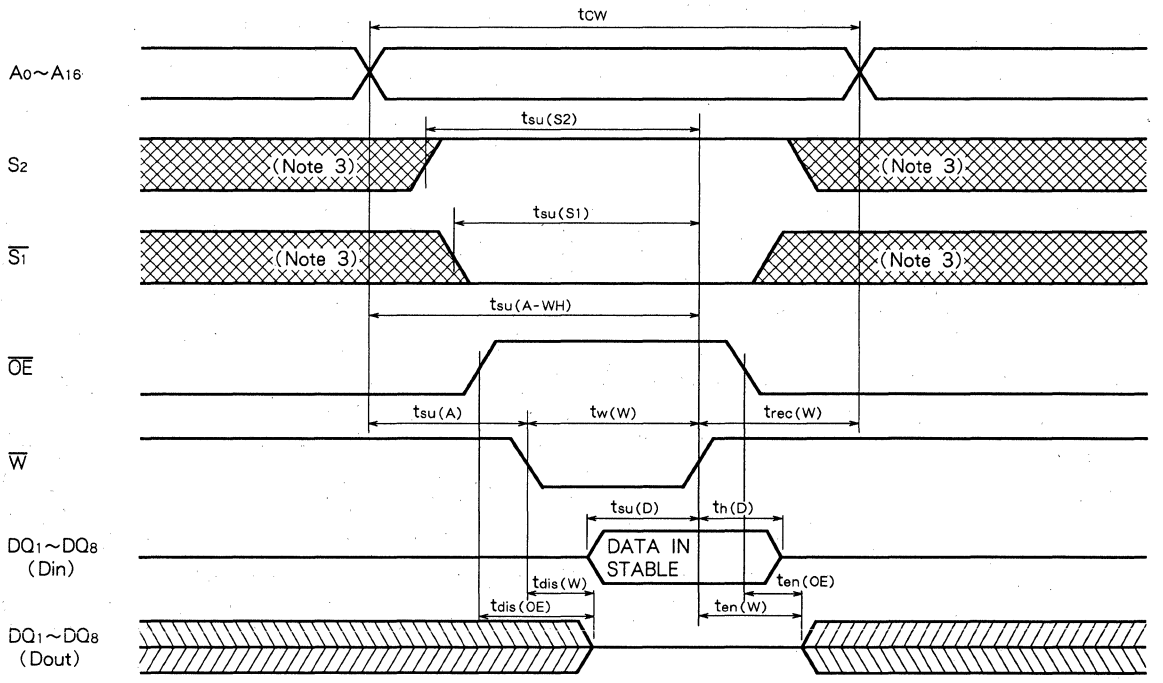
Symbol	Parameter	Limits								Unit
		M5M51008AP, FP, VP, RV-70L, -70LL		M5M51008AP, FP, VP, RV-85L, -85LL		M5M51008AP, FP, VP, RV-10L, -10LL		M5M51008AP, FP, VP, RV-12L, -12LL		
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{CW}	Write cycle time	70		85		100		120		ns
$t_{w(W)}$	Write pulse width	55		65		75		85		ns
$t_{su(A)}$	Address set up time	0		0		0		0		ns
$t_{su(A-WH)}$	Address set up time with respect to $\overline{W}$ high	65		75		85		100		ns
$t_{su(S1)}$	Chip select 1 set up time	65		75		85		100		ns
$t_{su(S2)}$	Chip select 2 set up time	65		75		85		100		ns
$t_{su(D)}$	Data set up time	30		35		40		45		ns
$t_{h(D)}$	Data hold time	0		0		0		0		ns
$t_{rec(W)}$	Write recovery time	0		0		0		0		ns
$t_{dis(W)}$	Output disable time from $\overline{W}$ low		25		30		35		40	ns
$t_{dis(OE)}$	Output disable time from $\overline{OE}$ high		25		30		35		40	ns
$t_{en(W)}$	Output enable time from $\overline{W}$ high	5		5		5		5		ns
$t_{en(OE)}$	Output enable time from $\overline{OE}$ low	5		5		5		5		ns

(4) TIMING DIAGRAMS

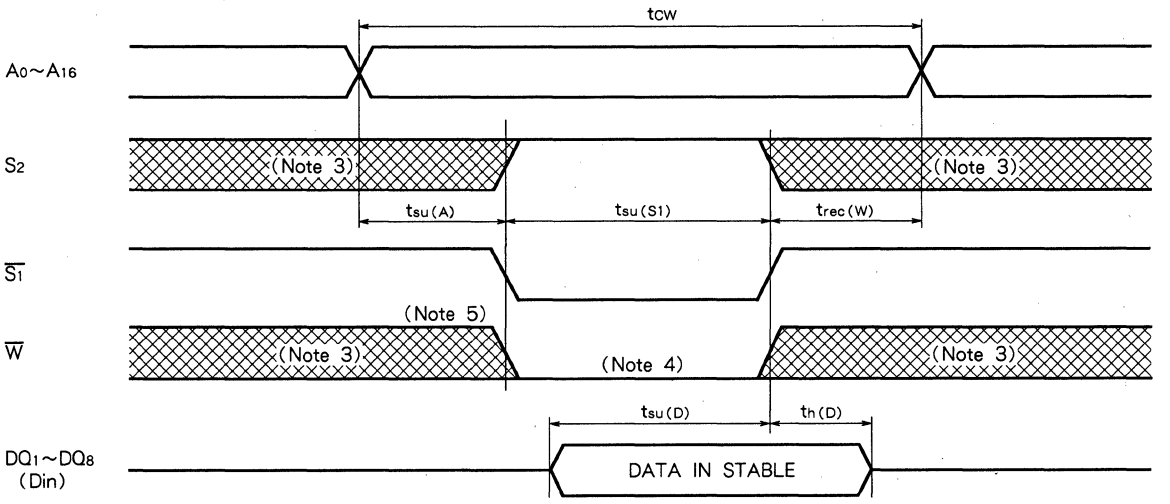
Read cycle



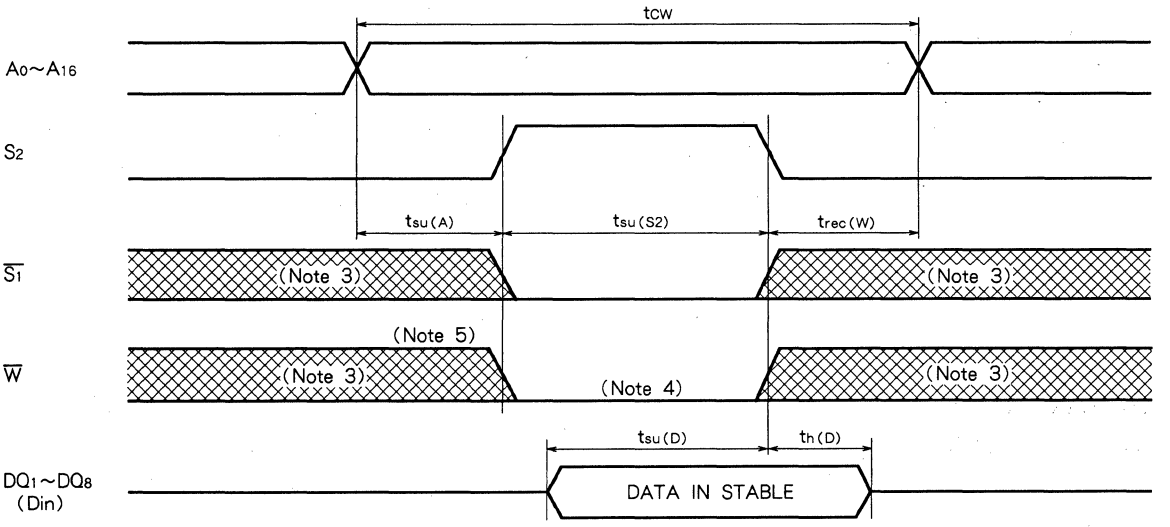
Write cycle (W control mode)



Write cycle ($\overline{S_1}$ control mode)



Write cycle (S_2 control mode)



Note 3 : Hatching indicates the state is "don't care".
4 : Writing is executed while S2 high overlaps $\overline{S1}$ and $\overline{W}$ low.
5 : When the falling edge of $\overline{W}$ is simultaneously or prior to the falling edge of $\overline{S1}$ or rising edge of S2, the outputs are maintained in the high impedance state.
6 : Don't apply inverted phase signal externally when DQ pin is output mode.

POWER DOWN CHARACTERISTICS

ELECTRICAL CHARACTERISTICS (T_a = 0~70℃, unless otherwise noted)

Symbol	Parameter	Test conditions		Limts Min	Limts Typ	Limts Max	Unit
$V_{CC(PD)}$	Power down supply voltage			2			V
$V_{I(\overline{S1})}$	Chip select input $\overline{S_1}$	2.2V ≦ $V_{CC(PD)}$		2.2			V
		2V ≦ $V_{CC(PD)}$ ≦ 2.2V			$V_{CC(PD)}$		
$V_{I(S2)}$	Chip select input S_2	4.5V ≦ $V_{CC(PD)}$				0.8	V
		$V_{CC(PD)}$ < 4.5V				0.2	
$I_{CC(PD)}$	Power down supply current	V_{CC} = 3V 1) S_2 ≦ 0.2V, other inputs = 0~3V 2) $\overline{S_1}$ ≧ V_{CC} − 0.2V, S_2 ≧ V_{CC} − 0.2V, other inputs = 0~3V	-L			50	μA
			-LL		0.3	10 (note 7)	

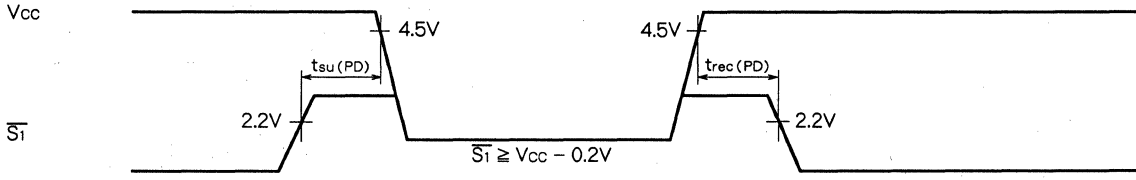
Note 7 : $I_{CC(PD)}$ = 1 μA in case of T_a = 25℃

TIMING REQUIREMENTS (T_a = 0~70℃, unless otherwise noted)

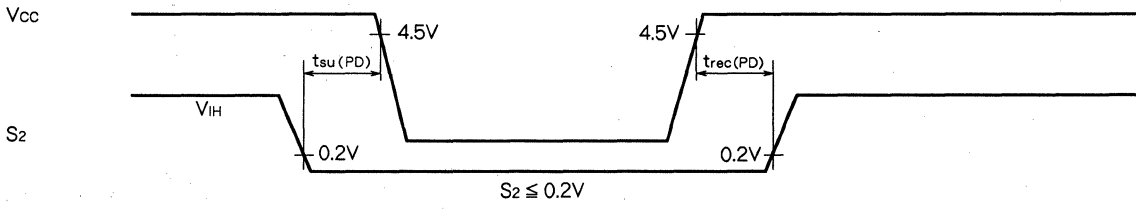
Symbol	Parameter	Test conditions	Limits Min	Limits Typ	Limits Max	Unit
$t_{su(PD)}$	Power down set up time		0			ns
$t_{rec(PD)}$	Power down recovery time		5			ms

POWER DOWN CHARACTERISTICS

$\overline{S_1}$ control mode



S_2 control mode



M5M51T08AP,FP,VP,RV-55SL

1048576-BIT(131072-WORD BY 8-BIT)CMOS STATIC RAM

DESCRIPTION

The M5M51T08AP, FP, VP, RV are a 1048576-bit CMOS static RAM organized as 131072 word by 8-bit which are fabricated using high-performance quadruple-polysilicon CMOS technology. The use of thin film transistor (TFT) load NMOS cells and CMOS periphery result in a high density, ultra low power and high reliability static RAM.

They are low stand-by current and low operation current and ideal for the battery back-up application.

The M5M51T08AP, FP, VP, RV are offered in a 32-pin plastic dual-in-line package (DIP), 32-pin plastic small outline package (SOP), as well as 32-pin thin small outline package (TSOP), providing high board level packing densities. Two types of TSOP packages are available, M5M51T08AVP (normal lead bend type package), M5M51T08ARV (reverse lead bend type package). Using both two types makes it easy to design a printed circuit board.

FEATURES

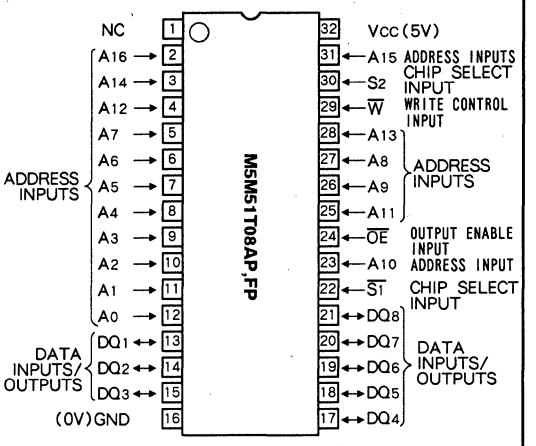
Type name	Access time (max)	Power supply current	
		Active (max)	Stand-by (max)
M5M51T08AP, FP,VP, RV-55SL	55ns	40mA (1MHz)	10 μA (V_{CC} = 5.5V) 0.05 μA (V_{CC} = 3.0V, typ)

- Single + 5V power supply
- Low stand-by current 0.05 μA (typ.)
- Directly TTL compatible : All inputs and outputs
- Easy memory expansion and power down by $\overline{S1}$, S2
- Data hold on + 2V power supply
- Three-state outputs : OR-tie capability
- $\overline{OE}$ prevents data contention in the I/O bus
- Common data I/O
- Package
  - M5M51T08AP ..... 32 pin 600 mil DIP
  - M5M51T08AFP ..... 32 pin 525 mil SOP
  - M5M51T08AVP, RV ..... 32 pin 8 × 20mm² TSOP

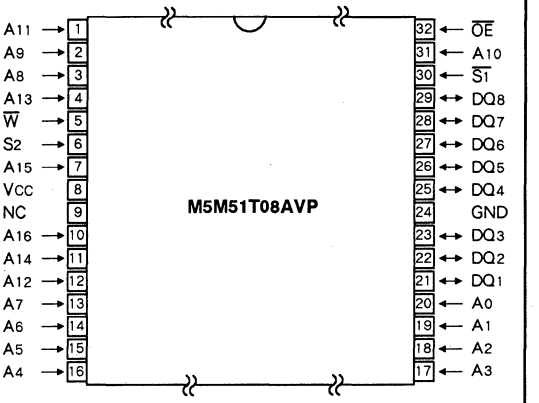
APPLICATION

Small capacity memory units

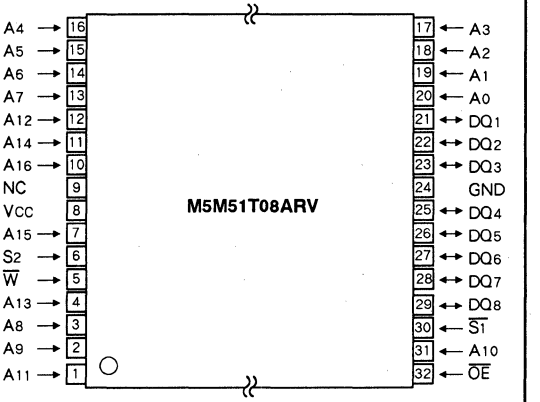
PIN CONFIGURATION (TOP VIEW)



Outline 32P4(P)
32P2M-A(FP)



Outline 32P3H-E



Outline 32P3H-F

NC : NO CONNECTION

1048576-BIT(131072-WORD BY 8-BIT)CMOS STATIC RAM

FUNCTION

The operation mode of the M5M51T08A serieas are determined by a combination of the device control inputs $\overline{S1}$, S2, $\overline{W}$ and $\overline{OE}$. Each mode is summarized in the function table.

A write cycle is executed whenever the low level $\overline{W}$ overlaps with the low level $\overline{S1}$ and the high level S2. The address must be set-up before the write cycle and must be stable during the entire cycle. The data is latched into a cell on the trailing edge of $\overline{W}$, $\overline{S1}$ or S2, whichever occurs first, requiring the set-up and hold time relative to these edge to be maintained. The output enable input $\overline{OE}$ directly controls the output stage. Setting the $\overline{OE}$ at a high level, the output stage is in a high-impedance state, and the data bus contention problem in the write cycle is eliminated.

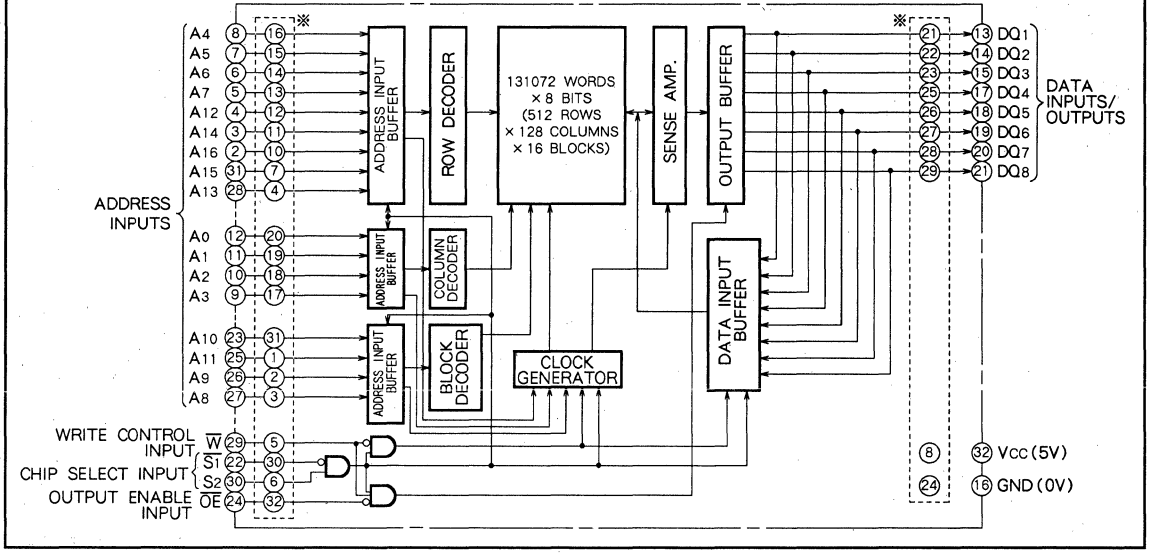
A read cycle is executed by setting $\overline{W}$ at a high level and $\overline{OE}$ at a low level while $\overline{S1}$ and S2 are in an active state ($\overline{S1}$ = L, S2 = H)

When setting $\overline{S1}$ at a high level or S2 at a low level, the chip are in a non-selectable mode in which both reading and writing are disabled. In this mode, the output stage is in a high-impedance state, allowing OR-tie with other chips and memory expansion by $\overline{S1}$ and S2. The power supply current is reduced as low as the standty current which is specified as I_{CC3} or I_{CC4}, and the memory data can be held at + 2V power supply, enabling battery back-up operation during power failure or power-down operation in the non-aelected mode.

FUNCTION TABLE

$\overline{S1}$	S2	$\overline{W}$	$\overline{OE}$	Mode	DQ	Icc
X	L	X	X	Non selection	High-impedance	Stand-by
H	X	X	X	Non selection	High-impedance	Stand-by
L	H	L	X	Write	Din	Active
L	H	H	L	Read	Dout	Active
L	H	H	H		High-impedance	Active

BLOCK DIAGRAM



※ Pin numbers inside dotted line show those of TSOP.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to GND	− 0.3*～7	V
V_I	Input voltage		− 0.3*～V_{CC} + 0.3	V
V_O	Output voltage		0～V_{CC}	V
P_d	Power dissipation	Ta = 25℃	700	mW
T_{opr}	Operating temperature		0～70	℃
T_{stg}	Storage temperature		− 65～150	℃

* − 3.0V in case of AC (Pulse width ≦ 30ns)

DC ELECTRICAL CHARACTERISTICS (Ta = 0～70℃, V_{CC} = 5V ± 10%, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits Min	Limits Typ	Limits Max	Unit
V_{IH}	High-level input voltage			2.2		V_{CC}+0.3	V
V_{IL}	Low-level input voltage			− 0.3*		0.8	V
V_{OH1}	High-level output voltage 1	I_{OH} = − 1mA		2.4			V
V_{OH2}	High-level output voltage 2	I_{OH} = − 0.1mA		V_{CC}-0.5			V
V_{OL}	Low-level output voltage	I_{OL} = 2mA				0.4	V
I_I	Input current	V_I = 0～V_{CC}				± 1	μA
I_O	Output current in off-state	$\overline{S_1}$ = V_{IH} or S_2 = V_{IL} or $\overline{OE}$ = V_{IH}, $V_{I/O}$ = 0～V_{CC}				± 1	μA
I_{CC1}	Active supply current (AC, MOS level)	$\overline{S_1}$ ≦ 0.2, S_2 ≧ V_{CC} − 0.2V other inputs ≦ 0.2V or ≧ V_{CC} − 0.2V Output-open (duty 100%)	Min cycle		47	85	mA
			1MHz		22	35	
I_{CC2}	Active supply current (AC, TTL level)	$\overline{S_1}$ = V_{IL}, S_2 = V_{IH}, other inputs = V_{IL} or V_{IH} Output-open (duty 100%)	Min cycle		50	90	mA
			1MHz		25	40	
I_{CC3}	Stand-by current	1) S_2 ≦ 0.2V, other inputs = 0～V_{CC} 2) $\overline{S_1}$ ≧ V_{CC} − 0.2V, S_2 ≧ V_{CC} − 0.2V, other inputs = 0～V_{CC}				10	μA
I_{CC4}	Stand-by current	$\overline{S_1}$ = V_{IH} or S_2 = V_{IL}, other inputs = 0～V_{CC}				3	mA

* − 3.0V in case of AC (Pulse width ≦ 30ns)

CAPACITANCE (Ta = 0～70℃, V_{CC} = 5V ± 10%, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits Min	Limits Typ	Limits Max	Unit
C_I	Input capacitance	V_I = GND, V_I = 25mVrms, f = 1MHz			6	pF
C_O	Output capacitance	V_O = GND, V_O = 25mVrms, f = 1MHz			8	pF

Note 1. Direction for current flowing into an IC is positive (no mark).
2. Typical value V_{CC} = 5V, Ta = 25℃.

AC ELECTRICAL CHARACTERISTICS (T_a = 0~70℃, V_{CC} = 5V ± 10%, unless otherwise noted)

(1) MEASUREMENT CONDITIONS

Input pulse level·····V_{IH} = 3.0V, V_{IL} = 0V
Input rise and fall time ·····5ns
Reference level·····V_{OH} = V_{OL} = 1.5V
Output loads·····Fig.1, C_L = 30pF
C_L = 5pF (for t_{en}, t_{dis})
Transition is measured ±500mV from steady state voltage.(for t_{en}, t_{dis})

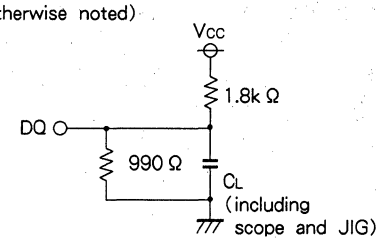


Fig.1 Output load

(2) READ CYCLE

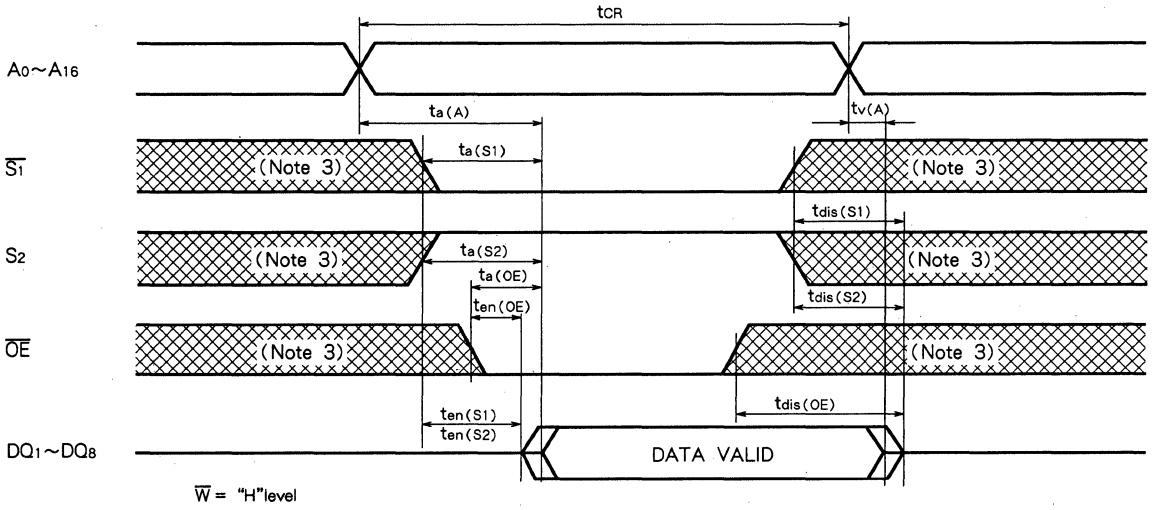
Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
t_{CR}	Read cycle time	55			ns
$t_{a(A)}$	Address access time			55	ns
$t_{a(S1)}$	Chip select 1 access time			55	ns
$t_{a(S2)}$	Chip select 2 access time			55	ns
$t_{a(OE)}$	Output enable access time			30	ns
$t_{dis(S1)}$	Output disable time after $\overline{S_1}$ high			20	ns
$t_{dis(S2)}$	Output disable time after S_2 low			20	ns
$t_{dis(OE)}$	Output disable time after $\overline{OE}$ high			20	ns
$t_{en(S1)}$	Output enable time after $\overline{S_1}$ low	5			ns
$t_{en(S2)}$	Output enable tiem after S_2 high	5			ns
$t_{en(OE)}$	Output enable time after $\overline{OE}$ low	5			ns
$t_{v(A)}$	Data valid time after address	5			ns

(3) WRITE CYCLE

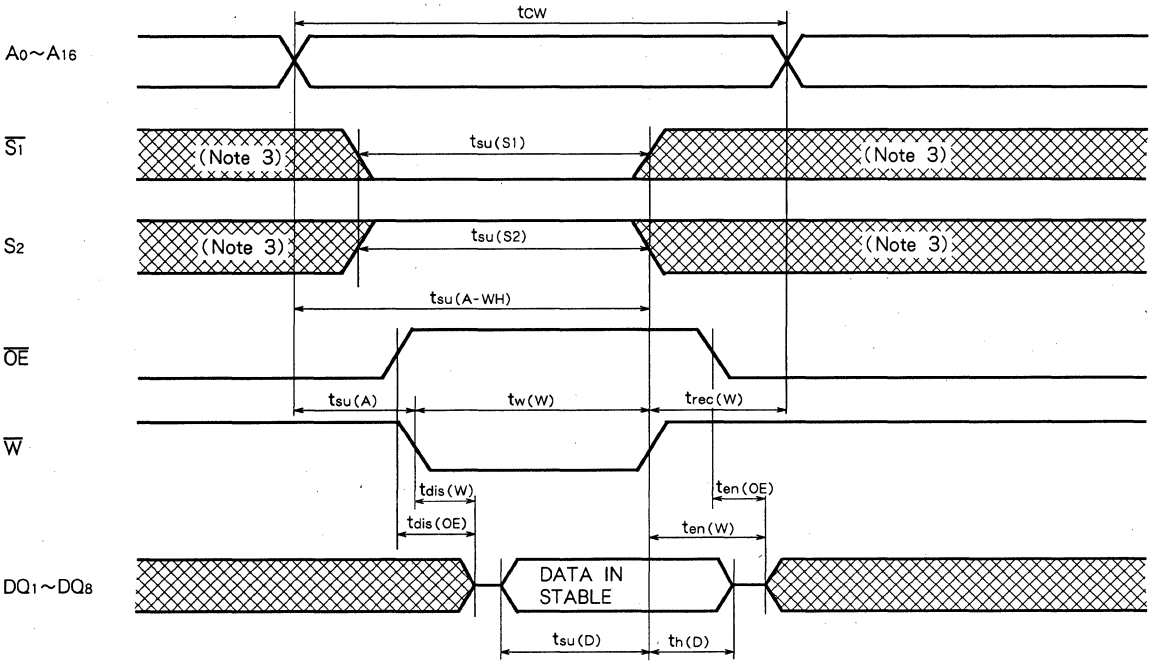
Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
t_{CW}	Write cycle time	55			ns
$t_{w(W)}$	Write pulse width	45			ns
$t_{su(A)}$	Address set up time	0			ns
$t_{su(A-WH)}$	Address set up time with respect to $\overline{W}$	50			ns
$t_{su(S1)}$	Chip select 1 set up time	50			ns
$t_{su(S2)}$	Chip select 2 set up time	50			ns
$t_{su(D)}$	Data set up time	25			ns
$t_{h(D)}$	Data hold time	0			ns
$t_{rec(W)}$	Write recovery time	0			ns
$t_{dis(W)}$	Output disable time from $\overline{W}$ low			20	ns
$t_{dis(OE)}$	Output disable time from $\overline{OE}$ high			20	ns
$t_{en(W)}$	Output enable time from $\overline{W}$ high	5			ns
$t_{en(OE)}$	Output enable time from $\overline{OE}$ low	5			ns

(4) TIMING DIAGRAMS

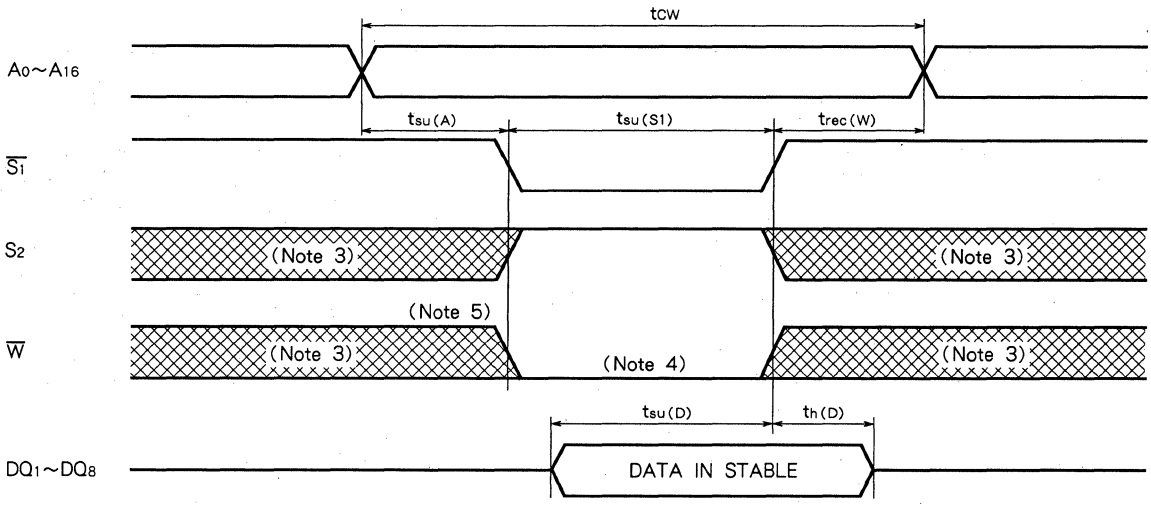
Read cycle



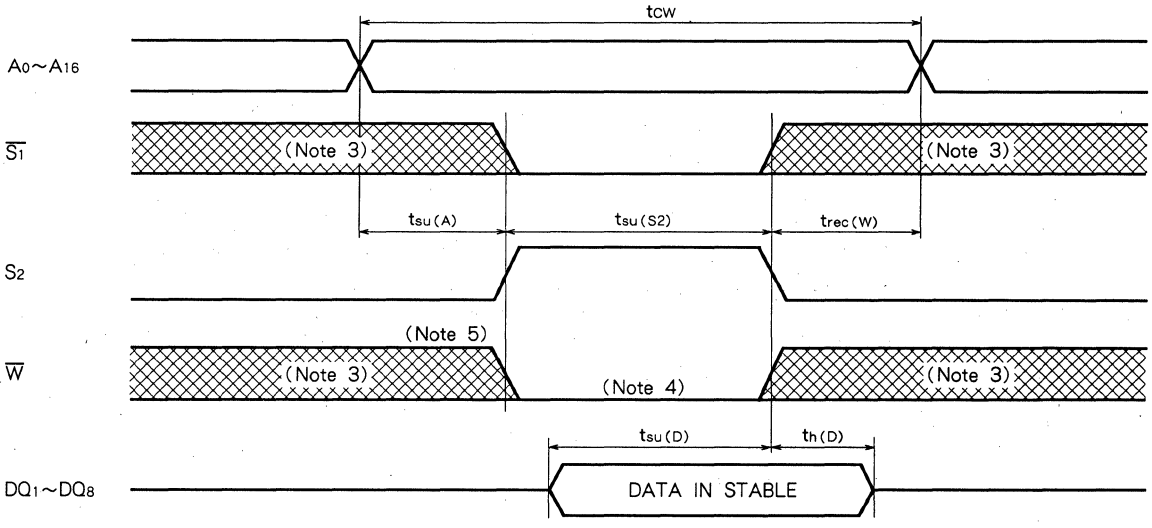
Write cycle ($\overline{W}$ control mode)



Write cycle ($\overline{S_1}$ control mode)



Write cycle (S_2 control mode)



Note 3. Hatching indicates the state is "don't care".
4. Writing is executed while S2 high overlaps $\overline{S_1}$ and $\overline{W}$ low.
5. When the falling edge of $\overline{W}$ is simultaneously or prior to the falling edge of $\overline{S_1}$ or rising edge of S2, the outputs are maintained in the high impedance state.
6. Don't apply inverted phase signal externally when DQ pin is output mode.

POWER DOWN CHARACTERISTICS

(1) ELECTRICAL CHARACTERISTICS (T_a = 0~70℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$V_{CC(PD)}$	Power down supply voltage		2			V
$V_{I(\overline{S1})}$	Chip select input $\overline{S1}$	2.2V ≦ $V_{CC(PD)}$	2.2			V
		2V ≦ $V_{CC(PD)}$ ≦ 2.2V		$V_{CC(PD)}$		
$V_{I(S2)}$	Chip select input S_2	4.5V ≦ $V_{CC(PD)}$			0.8	V
		$V_{CC(PD)}$ < 4.5V			0.2	
$I_{CC(PD)}$	Power down supply current	V_{CC} = 3V 1) S_2 ≦ 0.2V, other inputs = 0~3V 2) $\overline{S1}$ ≧ V_{CC} − 0.2V, S_2 ≧ V_{CC} − 0.2V, other inputs = 0~3V		0.05	2 (Note 7)	μA

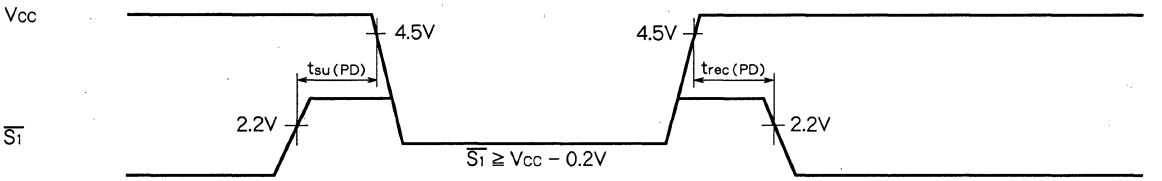
Note 7. $I_{CC(PD)}$ = 0.2 μA in case of T_a = 25℃

(2) TIMING REQUIREMENTS (T_a = 0~70℃, unless otherwise noted)

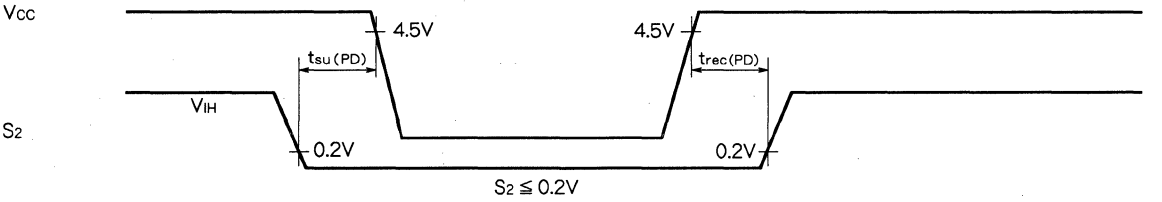
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{su(PD)}$	Power down set up time		0			ns
$t_{rec(PD)}$	Power down recovery time		5			ms

(3) POWER DOWN CHARACTERISTICS

$\overline{S1}$ control mode



S_2 control mode



M5M51T08AP,FP,VP,RV-70SL,-85SL,-10SL,-12SL

1048576-BIT(131072-WORD BY 8-BIT)CMOS STATIC RAM

DESCRIPTION

The M5M51T08AP, FP, VP, RV are a 1048576-bit CMOS static RAM organized as 131072 word by 8-bit which are fabricated using high-performance quadruple-polysilicon CMOS technology. The use of thin film transistor (TFT) load NMOS cells and CMOS periphery result in a high density, ultra low power and high reliability static RAM.

They are low standby current and low operation current and ideal for the battery back-up application.

The M5M51T08AVP, RV are offered in a 32-pin plastic dual-in-line package (DIP), 32-pin plastic small outline package (SOP), as well as 32-pin thin small outline package (TSOP), providing high board level packing densities. Two types of TSOP packages are available. M5M51T08AVP (normal lead bend type package), M5M51T08ARV (reverce lead bend type package). Using both two types makes it easy to design a printed circuit board.

FEATURES

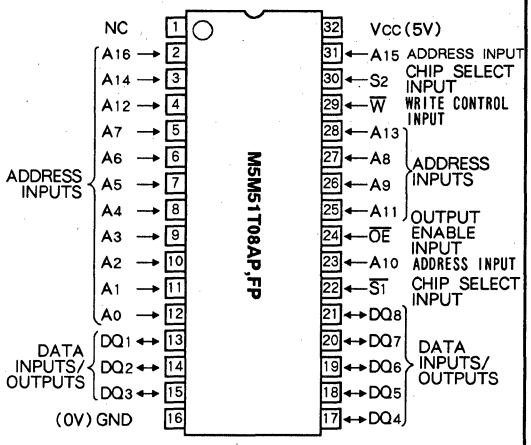
Type name	Access time (max)	Power supply current	
		Active (max)	Stand-by (max)
M5M51T08AP, FP, VP, RV-70SL M5M51T08AP, FP, VP, RV-85SL M5M51T08AP, FP, VP, RV-10SL M5M51T08AP, FP, VP, RV-12SL	70ns 85ns 100ns 120ns	15mA (1MHz)	10 μA (Vcc = 5.5V) 0.05 μA (Vcc = 3.0V, typ)

- Single +5V power supply
- Low stand-by current 0.05 μA (typ)
- Directly TTL compatible : All inputs and outputs
- Easy memory expansion and power down by $\overline{S}_1$, S_2
- Data hold on +2V power supply
- Three-state outputs : OR-tie capability
- $\overline{OE}$ prevents data contention in the I/O bus
- Common data I/O
- Package
  - M5M51T08AP ..... 32 pin 600 mil DIP
  - M5M51T08AFP ..... 32 pin 525 mil SOP
  - M5M51T08AVP, RV ..... 32 pin 8 × 20mm² TSOP

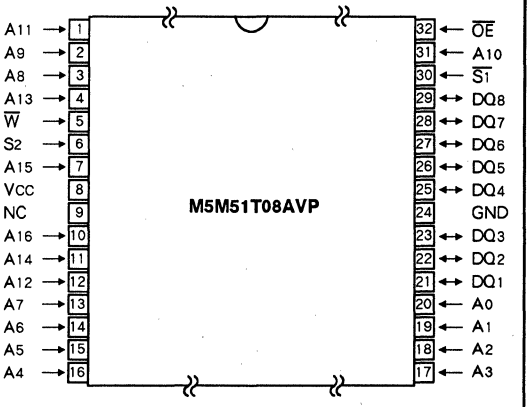
APPLICATION

Small capacity memory units

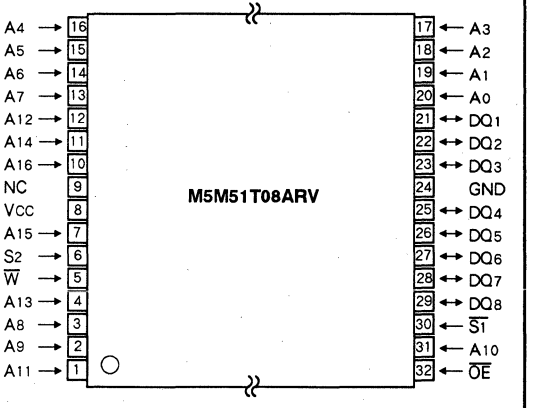
PIN CONFIGURATION (TOP VIEW)



Outline 32P4 (P)
32P2M-A (FP)



Outline 32P3H-E



Outline 32P3H-F

NC : NO CONNECTION

FUNCTION

The operation mode of the M5M51T08A serieas are determined by a combination of the device control inputs $\overline{S1}$, S2, $\overline{W}$ and $\overline{OE}$. Each mode is summarized in the function table.

A write cycle is executed whenever the low level $\overline{W}$ overlaps with the low level $\overline{S1}$ and the high level S2. The address must be set-up before the write cycle and must be stable during the entire cycle. The data is latched into a cell on the trailing edge of $\overline{W}$, $\overline{S1}$ or S2, whichever occurs first, requiring the set-up and hold time relative to these edge to be maintained. The output enable input $\overline{OE}$ directly controls the output stage. Setting the $\overline{OE}$ at a high level, the output stage is in a high-impedance state, and the data bus contention problm in the write cycle is eliminated.

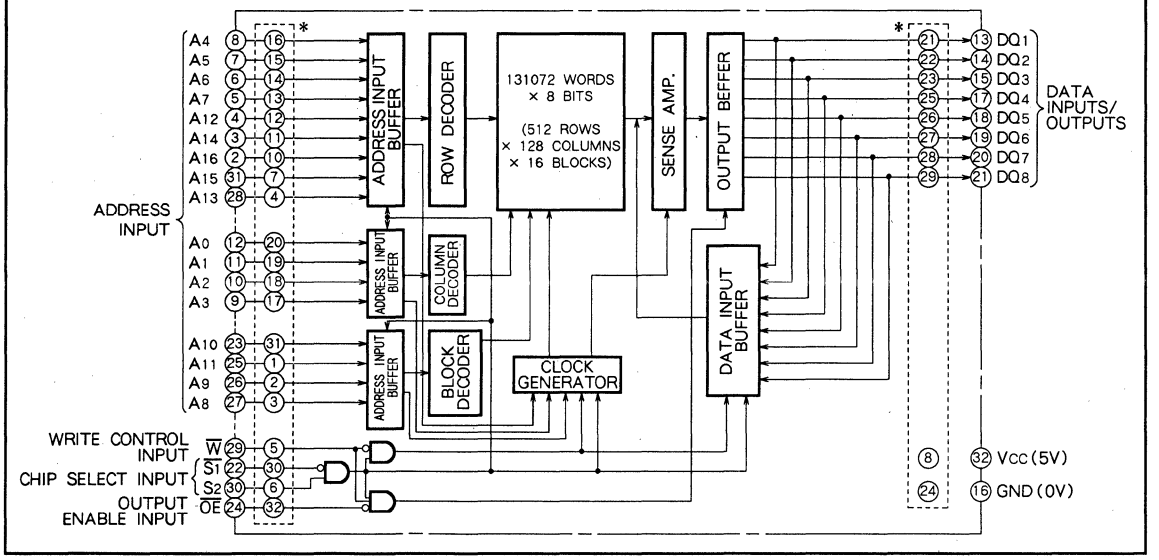
A read cycle is executed by setting $\overline{W}$ at a high level and $\overline{OE}$ at a low level while $\overline{S1}$ and S2 are in an active state ($\overline{S1}$ = L, S2 = H)

When setting $\overline{S1}$ at a high level or S2 at a low level, the chip are in a non-selectable mode in which both reading and writing are disabled. In this mode, the output stage is in a high-impedance state, allowing OR-tie with other chips and memory expansion by $\overline{S1}$ and S2. The power supply current is reduced as low as the stand-by current which is specified as I_{CC3} or I_{CC4}, and the memory data can be held at + 2V power supply, enabling battery back-up operation during power failure or power-down operation in the non-selected mode.

FUNCTION TABLE

$\overline{S1}$	S2	$\overline{W}$	$\overline{OE}$	Mode	DQ	Icc
X	L	X	X	Non selection	High-impedance	Stand-by
H	X	X	X	Non selection	High-impedance	Stand-by
L	H	L	X	Write	DIN	Active
L	H	H	L	Read	DOUT	Active
L	H	H	H		High-impedance	Active

BLOCK DIAGRAM



* Pin numbers inside dotted line show those of TSOP.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to GND	− 0.3*~7	V
V_I	Input voltage		− 0.3*~V_{CC} + 0.3	V
V_O	Output voltage		0~V_{CC}	V
P_d	Power dissipation	Ta = 25℃	700	mW
T_{opr}	Operating temperature		0~70	℃
T_{stg}	Storage temperature		− 65~150	℃

* − 3.0V in case of AC (Pulse width ≦ 30ns)

DC ELECTRICAL CHARACTERISTICS (Ta = 0~70℃, V_{CC} = 5V ± 10%, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits Min	Limits Typ	Limits Max	Unit
V_{IH}	High-level input voltage			2.2		V_{CC}+0.3	V
V_{IL}	Low-level input voltage			− 0.3*		0.8	V
V_{OH1}	High-level output voltage 1	I_{OH} = − 1mA		2.4			V
V_{OH2}	High-level output voltage 2	I_{OH} = − 0.1mA		V_{CC}-0.5			V
V_{OL}	Low-level output voltage	I_{OL} = 2mA				0.4	V
I_I	Input current	V_I = 0~V_{CC}				± 1	μA
I_O	Output current in off-state	$\overline{S_1}$ = V_{IH} or S_2 = V_{IL} or $\overline{OE}$ = V_{IH}, $V_{I/O}$ = 0~V_{CC}				± 1	μA
I_{CC1}	Active supply current (AC, MOS level)	$\overline{S_1}$ ≦ 0.2V, S_2 ≧ V_{CC} − 0.2V other inputs ≦ 0.2V or ≧ V_{CC} − 0.2V Output-open (duty 100%)	Min cycle		38	70	mA
			1MHz		5	15	
I_{CC2}	Active supply current (AC, TTL level)	$\overline{S_1}$ = V_{IL}, S_2 = V_{IH}, other inputs = V_{IL} or V_{IH} Output-open (duty 100%)	Min cycle		40	70	mA
			1MHz		7	15	
I_{CC3}	Stand-by current	1) S_2 ≦ 0.2V, other inputs = 0~V_{CC} 2) $\overline{S_1}$ ≧ V_{CC} − 0.2V, S_2 ≧ V_{CC} − 0.2V, other inputs = 0~V_{CC}				10	μA
I_{CC4}	Stand-by current	$\overline{S_1}$ = V_{IH}, S_2 = V_{IL}, other inputs = 0~V_{CC}				3	mA

* − 3.0V in case of AC (Pulse width ≦ 30ns)

CAPACITANCE (Ta = 0~70℃, V_{CC} = 5V ± 10%, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits Min	Limits Typ	Limits Max	Unit
C_I	Input capacitance	V_I = GND, V_I = 25mVrms, f = 1MHz			6	pF
C_O	Output capacitance	V_O = GND, V_O = 25mVrms, f = 1MHz			8	pF

Note 1. Direction for current flowing into an IC is positive (no mark).
2. Typical value is V_{CC} = 5V, Ta = 25℃.

AC ELECTRICAL CHARACTERISTICS (T_a = 0~70℃, V_{CC} = 5V ± 10%, unless otherwise noted)

(1) MEASUREMENT CONDITIONS

Input pulse level·····V_{IH} = 2.4V, V_{IL} = 0.6V
Input rise and fall time ·····5ns
Reference level·····V_{OH} = V_{OL} = 1.5V
Output loads·····Fig.1, C_L = 100pF (P,FP,VP,RV-85SL,-10SL,-12SL)
C_L = 30pF (P,FP,VP,RV-70SL)
C_L = 5pF (for t_{en}, t_{dis})
Transition is measured ±500mV from steady state voltage.(for t_{en}, t_{dis})

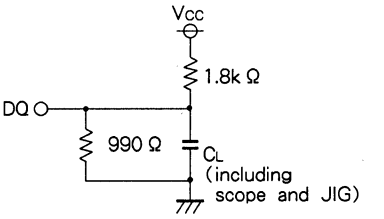


Fig.1 Output load

(2) READ CYCLE

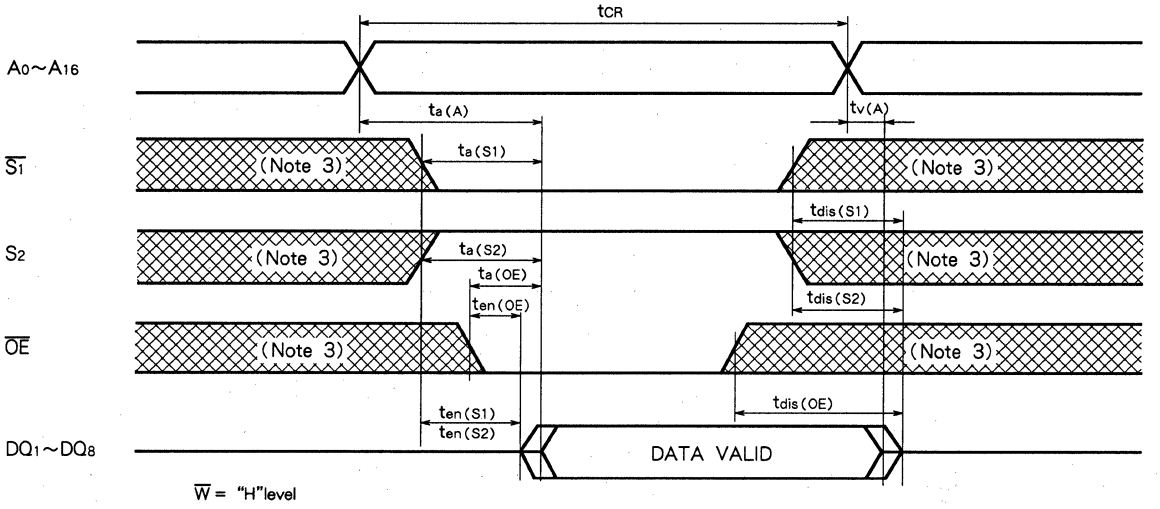
Symbol	Parameter	Limits								Unit
		M5M51T08AP, FP, VP, RV-70SL		M5M51T08AP, FP, VP, RV-85SL		M5M51T08AP, FP, VP, RV-10SL		M5M51T08AP, FP, VP, RV-12SL		
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{CR}	Read cycle time	70		85		100		120		ns
$t_{a(A)}$	Address access time		70		85		100		120	ns
$t_{a(S1)}$	Chip select 1 access time		70		85		100		120	ns
$t_{a(S2)}$	Chip select 2 access time		70		85		100		120	ns
$t_{a(OE)}$	Output enable access time		35		45		50		60	ns
$t_{dis(S1)}$	Output disable time after $\overline{S_1}$ high		25		30		35		40	ns
$t_{dis(S2)}$	Output disable time after S_2 low		25		30		35		40	ns
$t_{dis(OE)}$	Output disable time after $\overline{OE}$ high		25		30		35		40	ns
$t_{en(S1)}$	Output enable time after $\overline{S_1}$ low	10		10		10		10		ns
$t_{en(S2)}$	Output enable time after S_2 high	10		10		10		10		ns
$t_{en(OE)}$	Output enable time after $\overline{OE}$ low	5		5		5		5		ns
$t_{v(A)}$	Data valid time after address	10		10		10		10		ns

(3) WRITE CYCLE

Symbol	Parameter	Limits								Unit
		M5M51T08AP, FP, VP, RV-70SL		M5M51T08AP, FP, VP, RV-85SL		M5M51T08AP, FP, VP, RV-10SL		M5M51T08AP, FP, VP, RV-12SL		
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{CW}	Write cycle time	70		85		100		120		ns
$t_{w(W)}$	Write pulse width	55		65		75		85		ns
$t_{su(A)}$	Address setup time	0		0		0		0		ns
$t_{su(A-WH)}$	Address setup time with respect to $\overline{W}$	65		75		85		100		ns
$t_{su(S1)}$	Chip select 1 setup time	65		75		85		100		ns
$t_{su(S2)}$	Chip select 2 setup time	65		75		85		100		ns
$t_{su(D)}$	Data setup time	30		35		40		45		ns
$t_{h(D)}$	Data hold time	0		0		0		0		ns
$t_{rec(W)}$	Write recovery time	0		0		0		0		ns
$t_{dis(W)}$	Output disable time from $\overline{W}$ low		25		30		35		40	ns
$t_{dis(OE)}$	Output disable time from $\overline{OE}$ high		25		30		35		40	ns
$t_{en(W)}$	Output enable time from $\overline{W}$ high	5		5		5		5		ns
$t_{en(OE)}$	Output enable time from $\overline{OE}$ low	5		5		5		5		ns

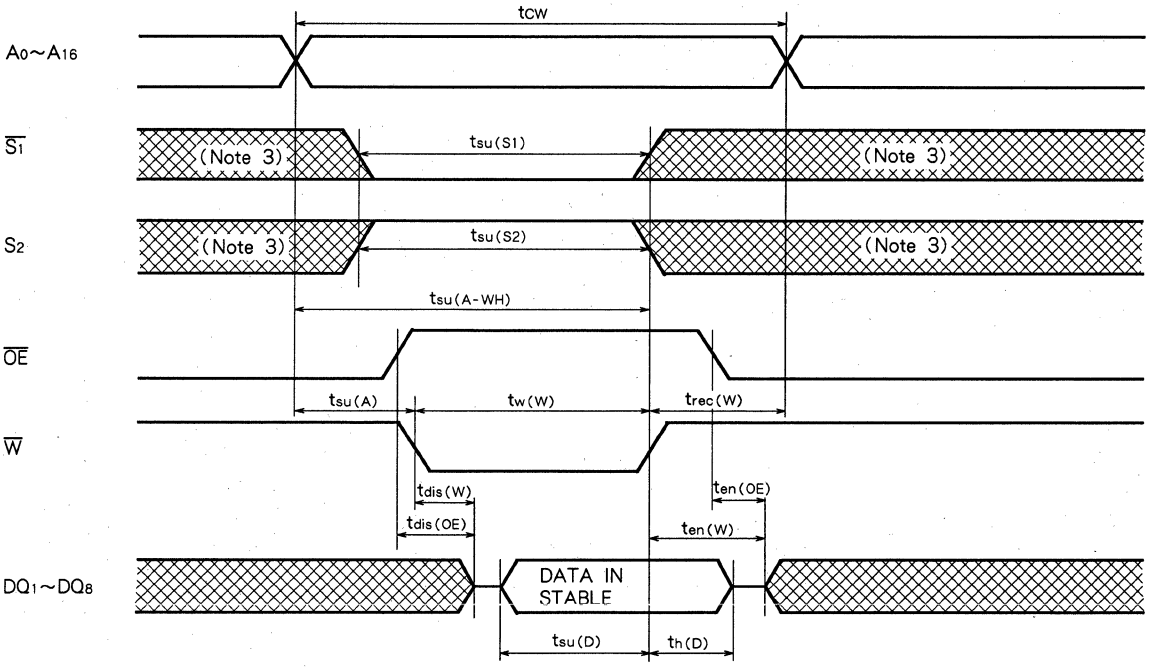
(4) TIMING DIAGRAMS

Read cycle

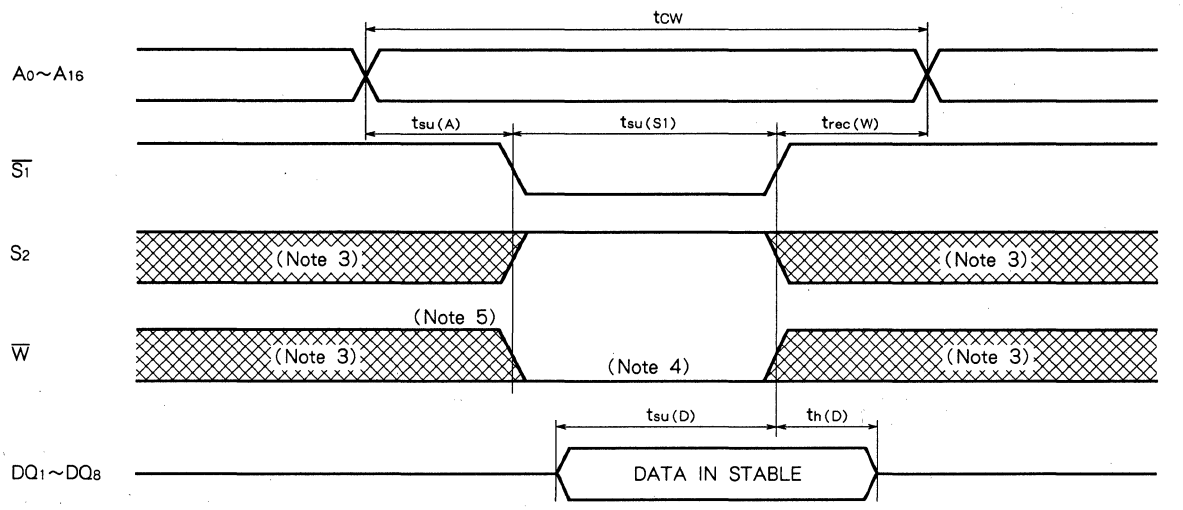


W = "H"level

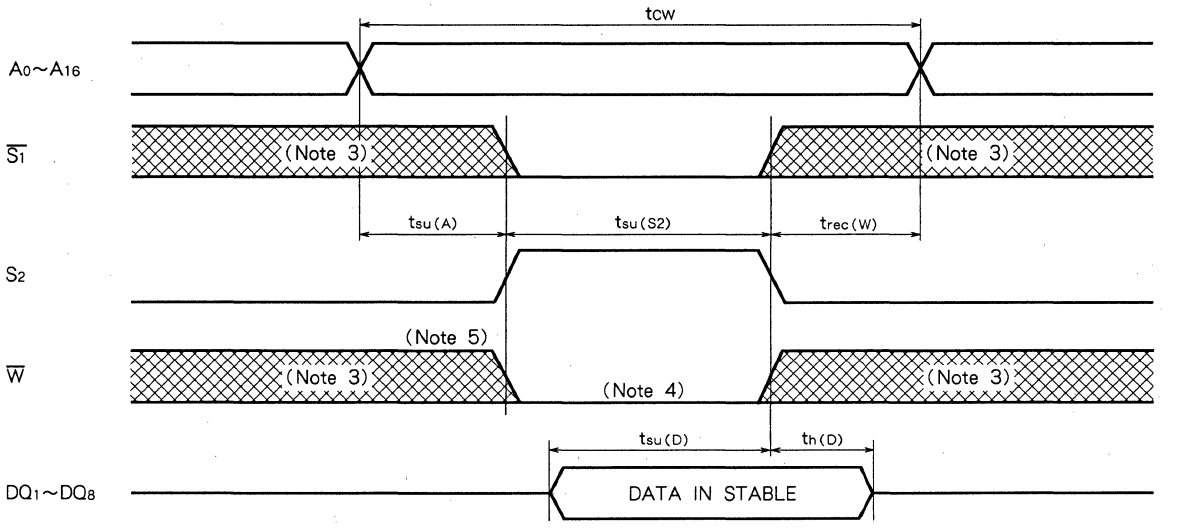
Write cycle (W control mode)



Write cycle ($\overline{S_1}$ control mode)



Write cycle (S_2 control mode)



Note 3. Hatching indicates the state is "don't care".
4. Writing is executed while S2 high overlaps $\overline{S_1}$ and $\overline{W}$ low.
5. When the falling edge of $\overline{W}$ is simultaneously or prior to the falling edge of $\overline{S_1}$ or rising edge of S2, the outputs are maintained in the high impedance state.
6. Don't apply inverted phase signal externally when DQ pin is output mode.

POWER DOWN CHARACTERISTICS

(1) ELECTRICAL CHARACTERISTICS (T_a = 0~70℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$V_{CC(PD)}$	Power down supply voltage		2			V
$V_{I(\overline{S1})}$	Chip select input $\overline{S_1}$	2.2V ≦ $V_{CC(PD)}$	2.2			V
		2V ≦ $V_{CC(PD)}$ ≦ 2.2V		$V_{CC(PD)}$		
$V_{I(S2)}$	Chip select input S_2	4.5V ≦ $V_{CC(PD)}$			0.8	V
		$V_{CC(PD)}$ < 4.5V			0.2	
$I_{CC(PD)}$	Power down supply current	V_{CC} = 3V 1) S_2 ≦ 0.2V, other inputs = 0~3V 2) $\overline{S_1}$ ≧ V_{CC} − 0.2V, S_2 ≧ V_{CC} − 0.2V, other inputs = 0~3V		0.05	2 (Note 7)	μA

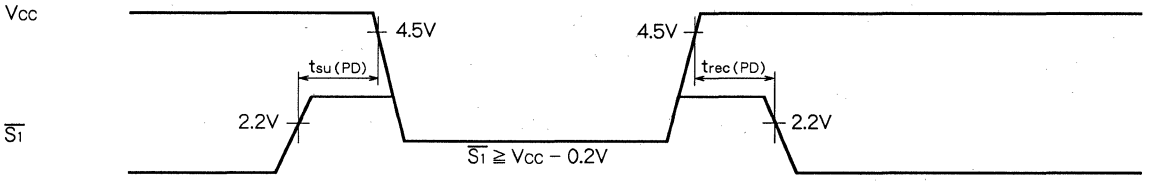
Note 7. $I_{CC(PD)}$ = 0.2 μA in case of T_a = 25℃

(2) TIMING REQUIREMENTS (T_a = 0~70℃, unless otherwise noted)

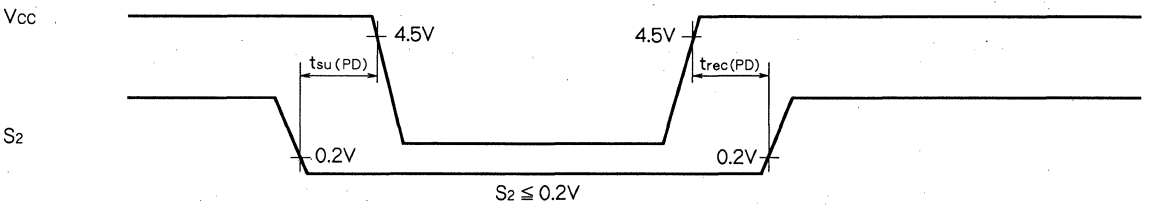
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{su(PD)}$	Power down setup time		0			ns
$t_{rec(PD)}$	Power down recovery time		5			ms

(3) POWER DOWN CHARACTERISTICS

$\overline{S_1}$ control mode



S_2 control mode



M5M51008BP,FP,VP,RV-55L, -70L, -10L, -55LL,-70LL,-10LL

1048576-BIT(131072-WORD BY 8-BIT)CMOS STATIC RAM

DESCRIPTION

The M5M51008BP,FP,VP,RV are a 1048576-bit CMOS static RAM organized as 131072-word by 8-bit which are fabricated using high-performance triple polysilicon CMOS technology. The use of resistive load NMOS cells and CMOS periphery result in a high density and low power static RAM.

They are low standby current and low operation current and ideal for the battery back-up application.

The M5M51008BVP,RV are packaged in a 32-pin thin small outline package which is a high reliability and high density surface mount device (SMD). Two types of devices are available. M5M51008BVP (normal lead vend type package), M5M51008BRV (reverce lead vend type package). Using both types of devices, it becames very easy to design a printed circuit board.

FEATURES

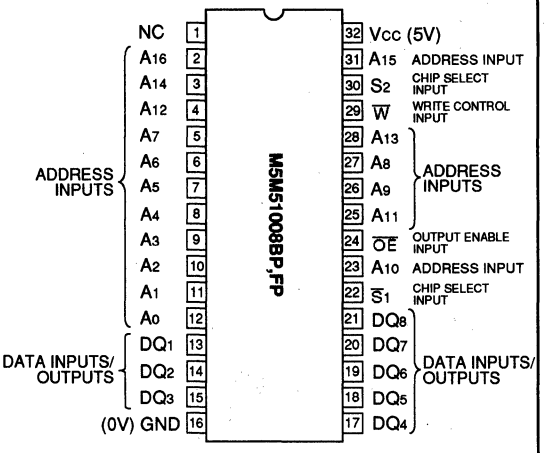
Type name	Access time (max)	Power supply current	
		Active (1MHz) (max)	stand-by (max)
M5M51008BP,FP,VP,RV-55L	55ns	15mA	100μA (Vcc=5.5V)
M5M51008BP,FP,VP,RV-70L	70ns		
M5M51008BP,FP,VP,RV-10L	100ns		
M5M51008BP,FP,VP,RV-55LL	55ns	15mA	20μA (Vcc=5.5V) 0.3μA (Vcc=3.0V,typ)
M5M51008BP,FP,VP,RV-70LL	70ns		
M5M51008BP,FP,VP,RV-10LL	100ns		

- Single +5V power supply
- Low stand-by current 0.3μA (typ.)
- Directly TTL compatible : All inputs and outputs
- Easy memory expansion and power down by $\overline{S}_1$, S_2
- Data hold on +2V power supply
- Three-state outputs : OR-tie capability
- $\overline{OE}$ prevents data contention in the I/O bus
- Common data I/O

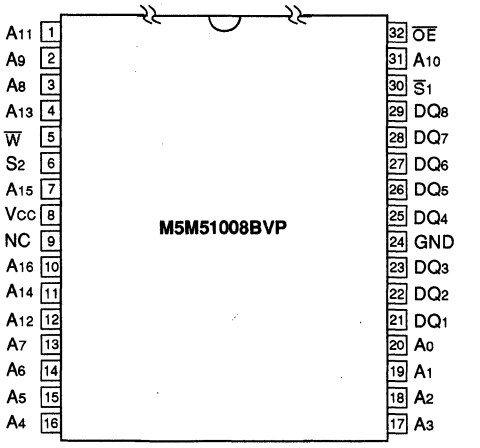
APPLICATION

Small capacity memory units

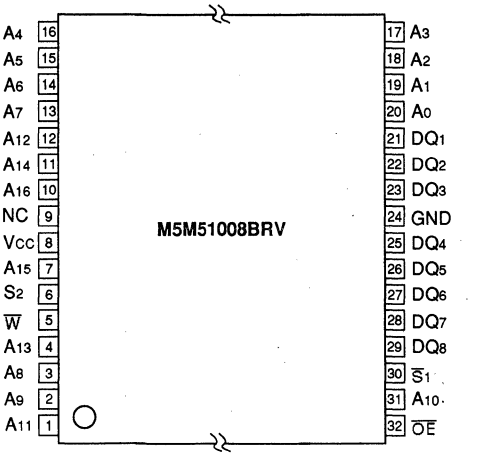
PIN CONFIGURATION (TOP VIEW)



Outline 32P4 (P)
32P2M-A (FP)



Outline 32P3H-E



Outline 32P3H-F

NC : NO CONNECTION

FUNCTION

The operation mode of the M5M51008B series are determined by a combination of the device control inputs $\overline{S}_1$, S_2, $\overline{W}$ and $\overline{OE}$. Each mode is summarized in the function table.

A write cycle is executed whenever the low level $\overline{W}$ overlaps with the low level $\overline{S}_1$ and the high level S_2. The address must be set up before the write cycle and must be stable during the entire cycle. The data is latched into a cell on the trailing edge of $\overline{W}$, $\overline{S}_1$ or S_2, whichever occurs first, requiring the set-up and hold time relative to these edge to be maintained. The output enable input $\overline{OE}$ directly controls the output stage. Setting the $\overline{OE}$ at a high level, the output stage is in a high-impedance state, and the data bus contention problem in the write cycle is eliminated.

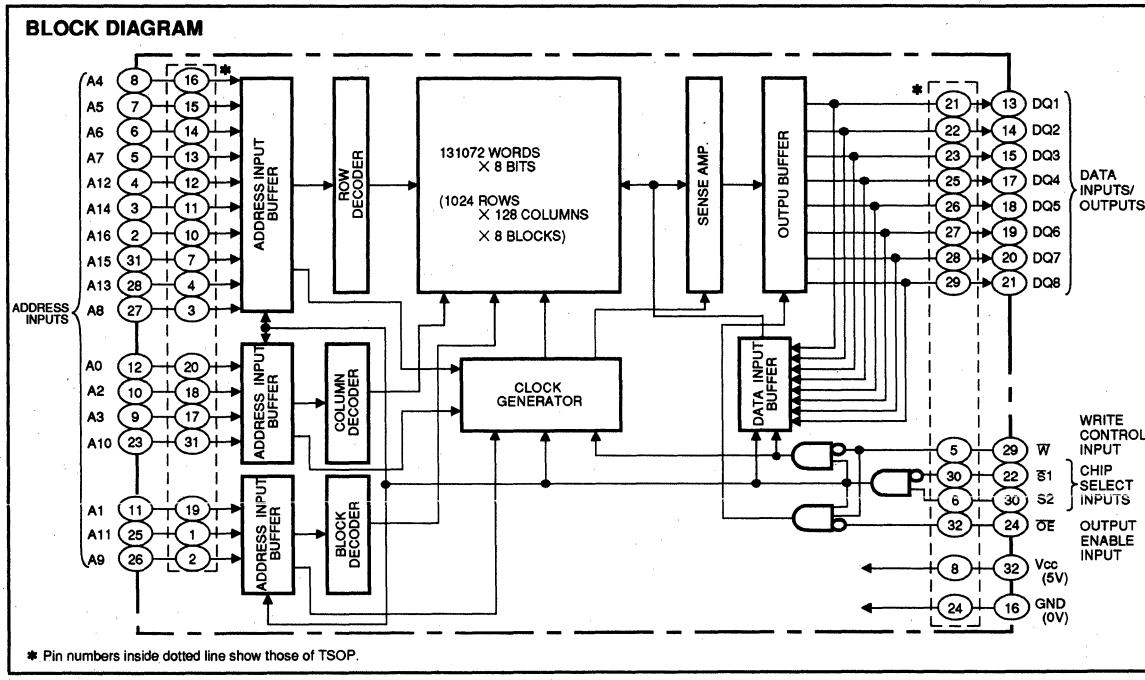
A read cycle is executed by setting $\overline{W}$ at a high level and $\overline{OE}$ at a low level while $\overline{S}_1$ and S_2 are in an active state ($\overline{S}_1$ = L, S_2 = H).

When setting $\overline{S}_1$ at a high level or S_2 at a low level, the chip are in a non-selectable mode in which both reading and writing are disabled. In this mode, the output stage is in a high-impedance state, allowing OR-tie with other chips and memory expansion by $\overline{S}_1$ and S_2. The power supply current is reduced as low as the stand-by current which is specified as I_{CC3} or I_{CC4}, and the memory data can be held at +2V power supply, enabling battery back-up operation during power failure or power-down operation in the non-selected mode.

FUNCTION TABLE

$\overline{S}_1$	S_2	$\overline{W}$	$\overline{OE}$	Mode	DQ	Icc
X	L	X	X	Non selection	High-impedance	Stand-by
H	X	X	X	Non selection	High-impedance	Stand-by
L	H	L	X	Write	Din	Active
L	H	H	L	Read	Dout	Active
L	H	H	H		High-impedance	Active

BLOCK DIAGRAM



* Pin numbers inside dotted line show those of TSOP.

MITSUBISHI ELECTRIC

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to GND	−0.3*～7	V
V_I	Input voltage		−0.3*～Vcc + 0.3	V
V_O	Output voltage		0～Vcc	V
P_d	Power dissipation	Ta = 25℃	700	mW
T_{opr}	Operating temperature		0～70	℃
T_{stg}	Storage temperature		−65～150	℃

* −3.0V in case of AC (Pulse width≦30ns)

DC ELECTRICAL CHARACTERISTICS (Ta = 0～70℃, Vcc = 5V±10%, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits Min	Limits Typ	Limits Max	Unit
V_{IH}	High-level input voltage			2.2		Vcc+0.3V	V
V_{IL}	Low-level input voltage			−0.3*		0.8	V
V_{OH1}	High-level output voltage 1	I_{OH} = −1mA		2.4			V
V_{OH2}	High-level output voltage 2	I_{OH} = −0.1mA		Vcc−0.5V			V
V_{OL}	Low-level output voltage	I_{OL} = 2mA				0.4	V
I_I	Input current	V_I = 0～Vcc				±1	μA
I_O	Output current in off-state	$\overline{S_1}$ = V_{IH} or S_2 = V_{IL} or $\overline{OE}$ = V_{IH} V_{IO} = 0～Vcc				±1	μA
I_{CC1}	Active supply current (AC, MOS level)	$\overline{S_1}$≦0.2V, S_2≧Vcc − 0.2V other inputs≦0.2V or ≧Vcc − 0.2V Output-open (duty 100%)	Min cycle		35 (40)**	70 (80)**	mA
			1MHz		4	15	
I_{CC2}	Active supply current (AC, TTL level)	$\overline{S_1}$ = V_{IL}, S_2 = V_{IH} other inputs = V_{IH} or V_{IL} Output-open (duty 100%)	Min cycle		38 (43)**	70 (85)**	mA
			1MHz		5	15	
I_{CC3}	Stand-by current	1) S_2≦0.2V, other inputs = 0～Vcc	-L			100	μA
		2) $\overline{S_1}$≧Vcc − 0.2V, S_2≧Vcc − 0.2V other inputs = 0～Vcc	-LL			20	
I_{CC4}	Stand-by current	$\overline{S_1}$ = V_{IH} or S_2 = V_{IL}, other inputs = 0～Vcc				3	mA

* −3.0V in case of AC (Pulse width≦30ns)
** inside ( ) is a value of -55L, -55LL

CAPACITANCE (Ta = 0～70℃, Vcc = 5V±10%, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits Min	Limits Typ	Limits Max	Unit
C_I	Input capacitance	V_I = GND, V_I = 25mVrms, f = 1MHz			6	pF
C_O	Output capacitance	V_O = GND, V_O = 25mVrms, f = 1MHz			8	pF

Note 1: Direction for current flowing into an IC is positive (no mark).
2: Typical value is Vcc = 5V, Ta = 25℃.

AC ELECTRICAL CHARACTERISTICS (T_a = 0～70℃, V_{CC}= 5V±10%, unless otherwise noted)

(1) MEASUREMENT CONDITIONS

Input pulse level ..... V_{IH} = 2.4V, V_{IL} = 0.6V(P,FP,VP,RV-70L,-10L,-70LL,-10LL)
V_{IH} = 3.0V, V_{IL} = 0.0V(P,FP,VP,RV-55L,-55LL)
Input rise and fall time 5ns
Reference level ..... V_{OH}=V_{OL}=1.5V
Output loads ..... Fig.1, C_L = 100pF (P,FP,VP,RV-10L,-10LL)
C_L = 30pF (P,FP,VP,RV-55L,-70L,-55LL,70LL)
C_L = 5pF (for t_{en},t_{dis})
Transition is measured ±500mV from steady state voltage. (for t_{en},t_{dis})

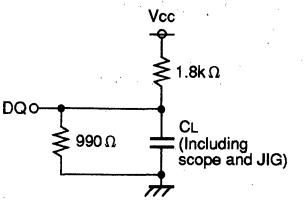


Fig.1 Output load

(2) READ CYCLE

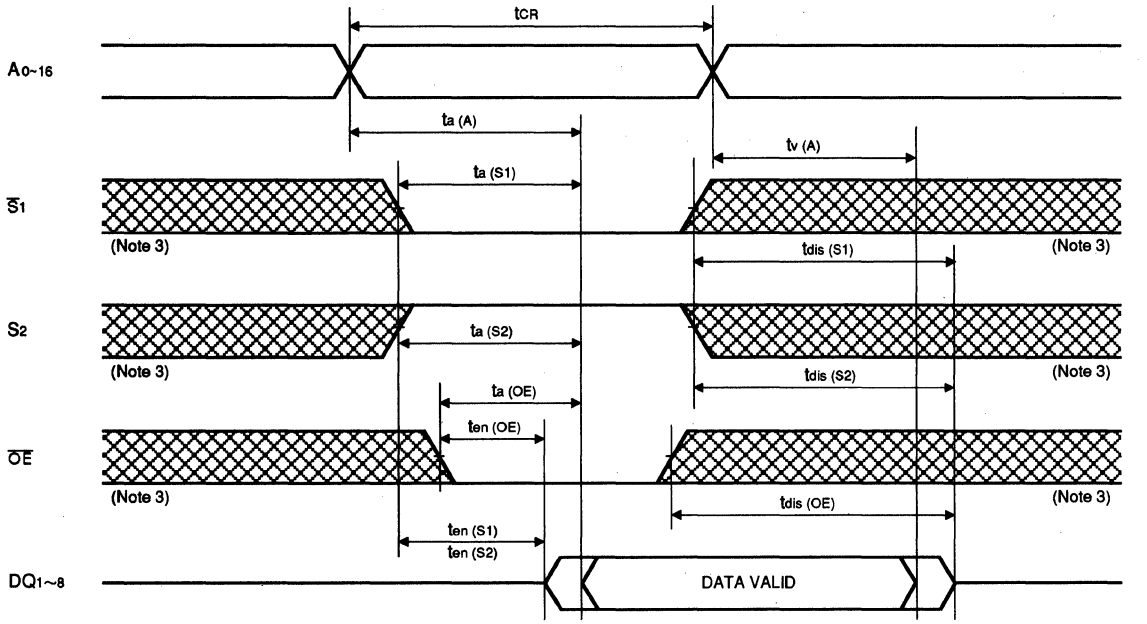
Symbol	Parameter	Limits						Unit
		M5M51008B-55L,55LL		M5M51008B-70L,70LL		M5M51008B-10L,10LL		
		Min	Max	Min	Max	Min	Max	
t_{CR}	Read cycle time	55		70		100		ns
$t_{a(A)}$	Address access time		55		70		100	ns
$t_{a(S1)}$	Chip select 1 access time		55		70		100	ns
$t_{a(S2)}$	Chip select 2 access time		55		70		100	ns
$t_{a(OE)}$	Output enable access time		30		35		50	ns
$t_{dis(S1)}$	Output disable time after $\overline{S_1}$ high		20		25		35	ns
$t_{dis(S2)}$	Output disable time after S_2 low		20		25		35	ns
$t_{dis(OE)}$	Output disable time after $\overline{OE}$ high		20		25		35	ns
$t_{en(S1)}$	Output enable time after $\overline{S_1}$ low	5		10		10		ns
$t_{en(S2)}$	Output enable time after S_2 high	5		10		10		ns
$t_{en(OE)}$	Output enable time after $\overline{OE}$ low	5		5		5		ns
$t_{v(A)}$	Data valid time after address	5		10		10		ns

(3) WRITE CYCLE

Symbol	Parameter	Limits						Unit
		M5M51008B-55L,55LL		M5M51008B-70L,70LL		M5M51008B-10L,10LL		
		Min	Max	Min	Max	Min	Max	
t_{CW}	Write cycle time	55		70		100		ns
$t_{w(W)}$	Write pulse width	45		55		75		ns
$t_{su(A)}$	Address setup time	0		0		0		ns
$t_{su(A-WH)}$	Address setup time with respect to $\overline{W}$	50		65		85		ns
$t_{su(S1)}$	Chip select 1 setup time	50		65		85		ns
$t_{su(S2)}$	Chip select 2 setup time	50		65		85		ns
$t_{su(D)}$	Data setup time	25		30		40		ns
$t_{h(D)}$	Data hold time	0		0		0		ns
$t_{rec(W)}$	Write recovery time	0		0		0		ns
$t_{dis(W)}$	Output disable time from $\overline{W}$ low		20		25		35	ns
$t_{dis(OE)}$	Output disable time from $\overline{OE}$ high		20		25		35	ns
$t_{en(W)}$	Output enable time from $\overline{W}$ high	5		5		5		ns
$t_{en(OE)}$	Output enable time from $\overline{OE}$ low	5		5		5		ns

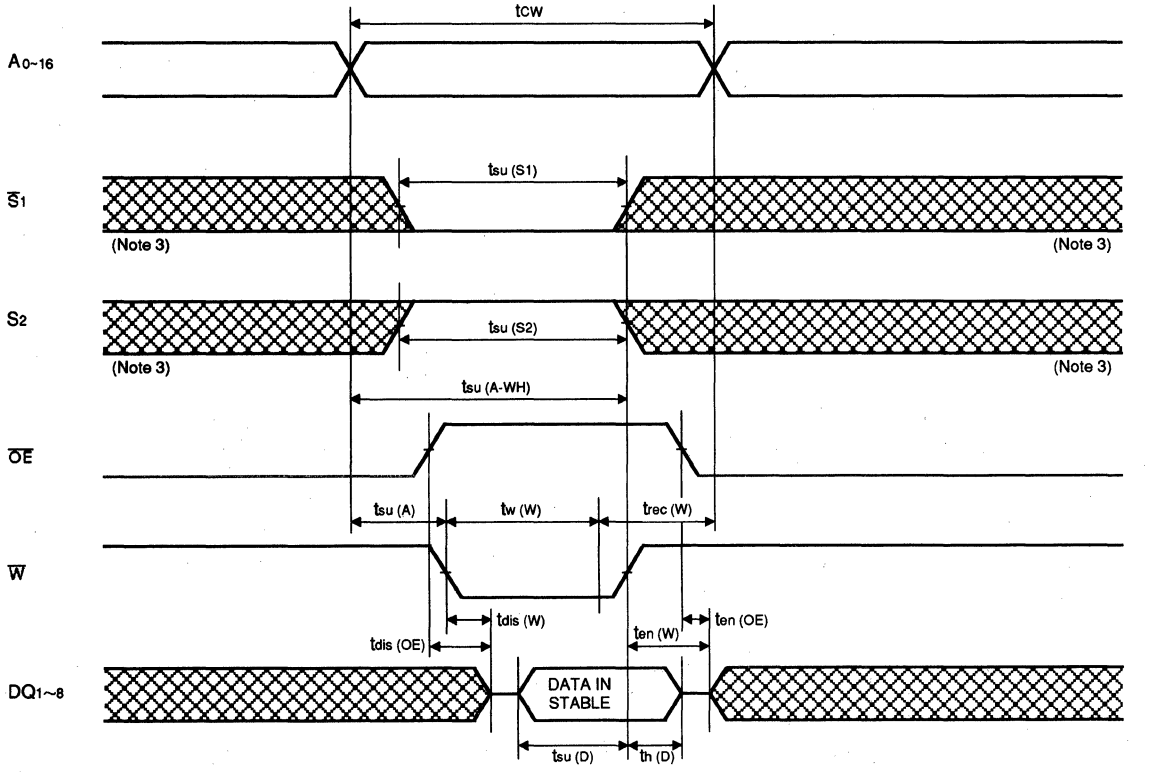
(4) TIMING DIAGRAMS

Read cycle

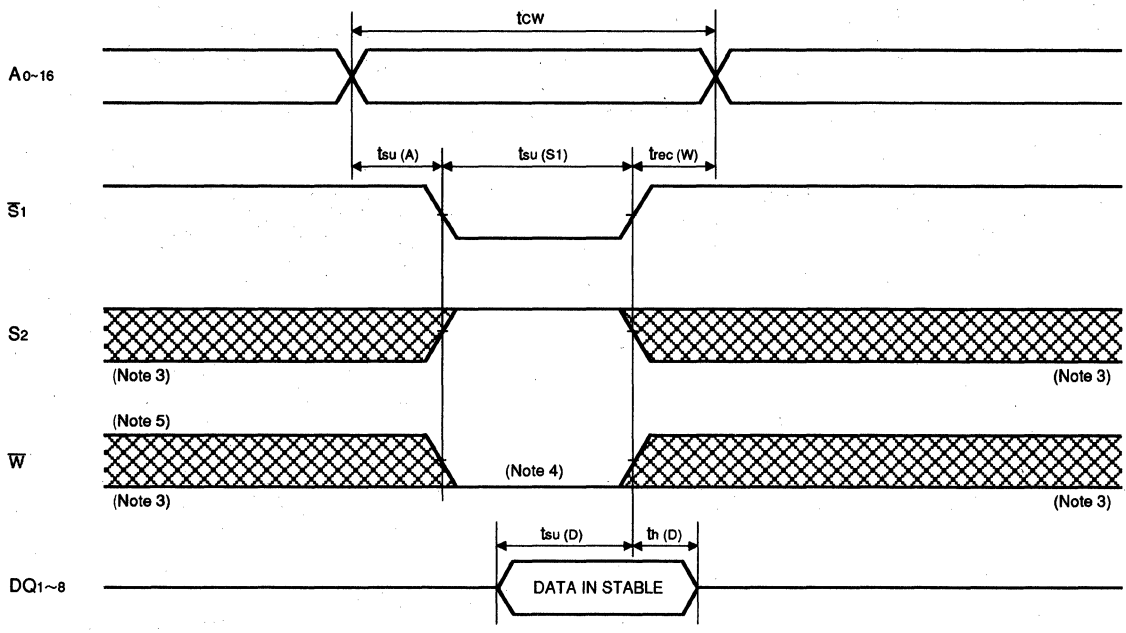


W = "H" level

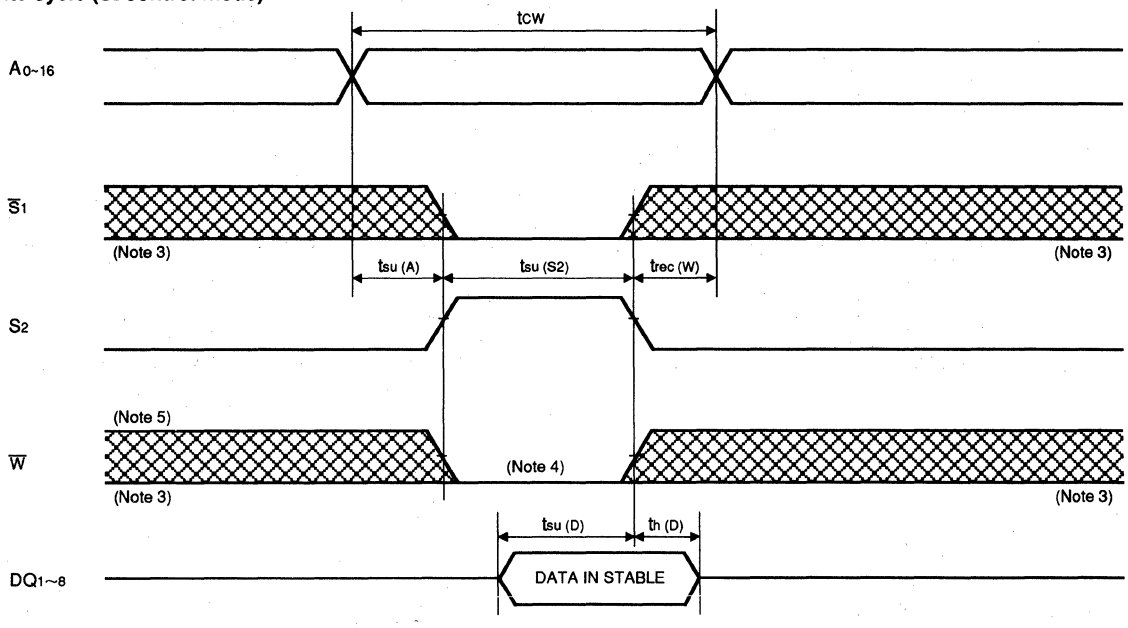
Write cycle (W control mode)



Write cycle ($\overline{S}_1$ control mode)



Write cycle (S_2 control mode)



Note 3 : Hatching indicates the state is "don't care".
4 : Writing is executed while S_2 high overlaps $\overline{S}_1$ and $\overline{W}$ low.
5 : When the falling edge of $\overline{W}$ is simultaneously or prior to the falling edge of $\overline{S}_1$ or rising edge of S_2 , the outputs are maintained in the high impedance state.
6 : Don't apply inverted phase signal externally when DQ pin is output mode.

POWER DOWN CHARACTERISTICS

(1) ELECTRICAL CHARACTERISTICS (T_a = 0~70℃, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ	Max	
$V_{CC\ (PD)}$	Power down supply voltage			2			V
$V_{I\ (\overline{S}1)}$	Chip select input $\overline{S}_1$	2.2V≦$V_{CC\ (PD)}$		2.2			V
		2V≦$V_{CC\ (PD)}$≦2.2V			$V_{CC\ (PD)}$		
$V_{I\ (S2)}$	Chip select input S_2	4.5V≦$V_{CC\ (PD)}$				0.8	V
		$V_{CC\ (PD)}$ < 4.5V				0.2	
$I_{CC\ (PD)}$	Power down supply current	V_{CC} = 3V 1) S_2≦0.2V, other inputs = 0~V_{CC}	-L			50	μA
		2) $\overline{S}_1$≧V_{CC}− 0.2V, S_2≧V_{CC}− 0.2V, other inputs = 0~V_{CC}	-LL		0.3	10 (Note 7)	

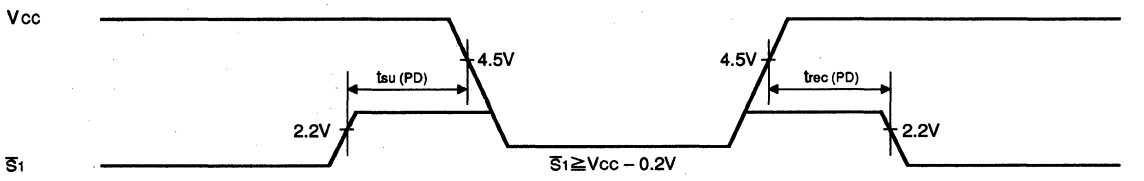
Note 7 : $I_{CC\ (PD)}$ = 1μA in case of T_a = 25℃

(2) TIMING REQUIREMENTS (T_a = 0~70℃, unless otherwise noted)

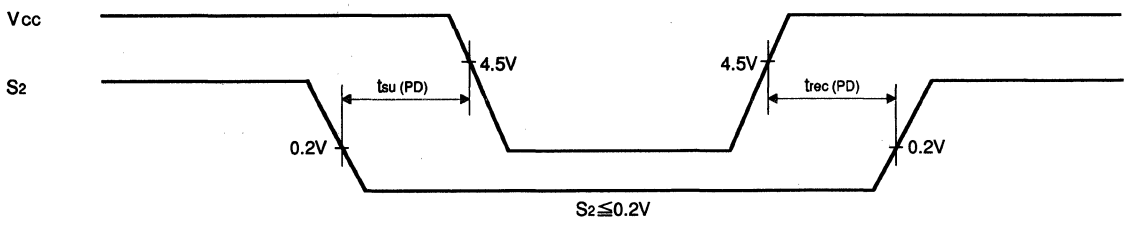
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{su\ (PD)}$	Power down set up time		0			ns
$t_{rec\ (PD)}$	Power down recovery time		5			ms

(3) POWER DOWN CHARACTERISTICS

$\overline{S}_1$ control mode



S_2 control mode



M5M51016ATP,RT-70L,-85L,-10L, -70LL,-85LL,-10LL

1048576-BIT(65536-WORD BY 16-BIT)CMOS STATIC RAM

DESCRIPTION

The M5M51016ATP, RT are a 1048576-bit CMOS static RAM organized as 65536 word by 16-bit which are fabricated using high-performance triple polysilicon CMOS technology. The use of resistive load NMOS cells and CMOS periphery result in a high density and low power static RAM.

They are low stand-by current and low operation current and ideal for the battery back-up application.

The M5M51016ATP, RT are packaged in a 44-pin thin small outline package which is a high reliability and high density surface mount device (SMD). Two types of devices are available. M5M51016ATP (normal lead bend type package), M5M51016ART (reverce lead bend type package). Using both types of devices, it becomes very easy to design a printed circuit board.

FEATURES

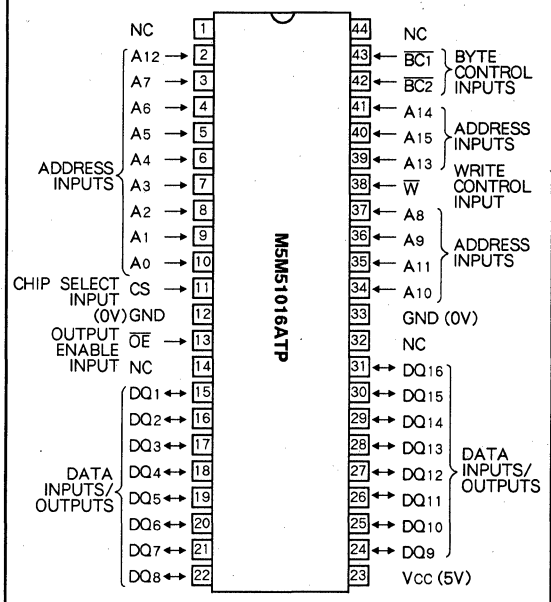
Type name	Access time (max)	Power supply current	
		Active (max)	Stand-by (max)
M5M51016ATP, RT-70L M5M51016ATP, RT-85L M5M51016ATP, RT-10L	70ns 85ns 100ns	30mA (1MHz)	100 μA (Vcc = 5.5V)
M5M51016ATP, RT-70LL M5M51016ATP, RT-85LL M5M51016ATP, RT-10LL	70ns 85ns 100ns		20 μA (Vcc = 5.5V) 0.3 μA (Vcc = 3.0V, typ)

- Single +5V power supply
- Low stand-by current 0.3 μA (typ)
- Directly TTL compatible : All inputs and outputs
- Easy memory expansion and power down by CS, $\overline{BC_1}$ & $\overline{BC_2}$
- Data hold on +2V power supply
- Three-state outputs : OR-tie capability
- $\overline{OE}$ prevents data contention in the I/O bus
- Common data I/O
- Package
  M5M51016ATP, RT ·····44pin 400 mil TSOP (II)

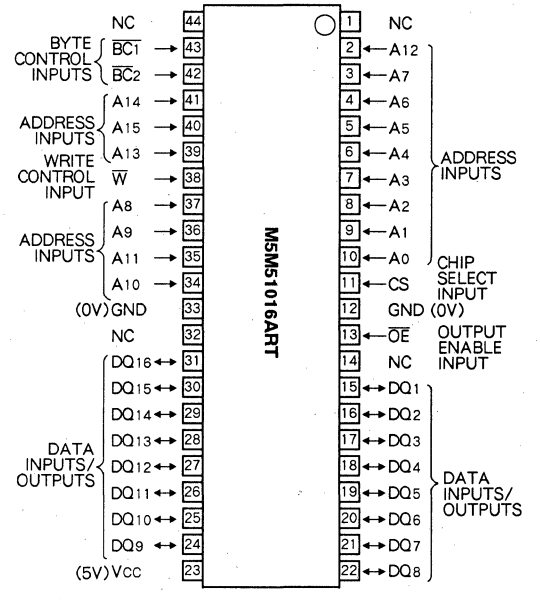
APPLICATION

Small capacity memory units

PIN CONFIGURATION (TOP VIEW)



Outline 44P3W-H (400mil TSOP Normal Bend)



Outline 44P3W-J (400mil TSOP Reverse Bend)

NC : NO CONNECTION

M5M51016ATP,RT-70L,-85L,-10L,-70LL,-85LL,-10LL

1048576-BIT(65536-WORD BY 16-BIT)CMOS STATIC RAM

FUNCTION

The operation mode of the M5M51016A series are determined by a combination of the device control inputs $\overline{BC1}$, $\overline{BC2}$, CS, $\overline{W}$ and $\overline{OE}$. Each mode is summarized in the function table.

A write cycle is executed whenever the low level $\overline{W}$ overlaps with the low level $\overline{BC1}$ and/or $\overline{BC2}$ and the high level CS. The address must be set up before the write cycle and must be stable during the entire cycle. The data is latched into a cell on the trailing edge of $\overline{W}$, $\overline{BC1}$, $\overline{BC2}$ or CS, whichever occurs first, requiring the set-up and hold time relative to these edge to be maintained. The output enable input $\overline{OE}$ directly controls the output state. Setting the $\overline{OE}$ at a high level, the output stage is in a high-impedance state, and the databus contention problem in the write cycle is eliminated.

A read cycle is executed by setting $\overline{W}$ at a high level and $\overline{OE}$ at a low level while $\overline{BC1}$ and/or $\overline{BC2}$ and CS are in an active state. ($\overline{BC1}$ and/or $\overline{BC2}$ = L, CS = H)

When setting $\overline{BC1}$ at a high level and the other pins are in an active state, upper-Byte are in a selectable mode in which both reading and writing are enabled, and lower-Byte are in a non-selectable mode. And when setting $\overline{BC2}$ at a high level and the other pins are in an active state, lower-Byte are in a selectable mode and upper-Byte are in a non-selectable mode.

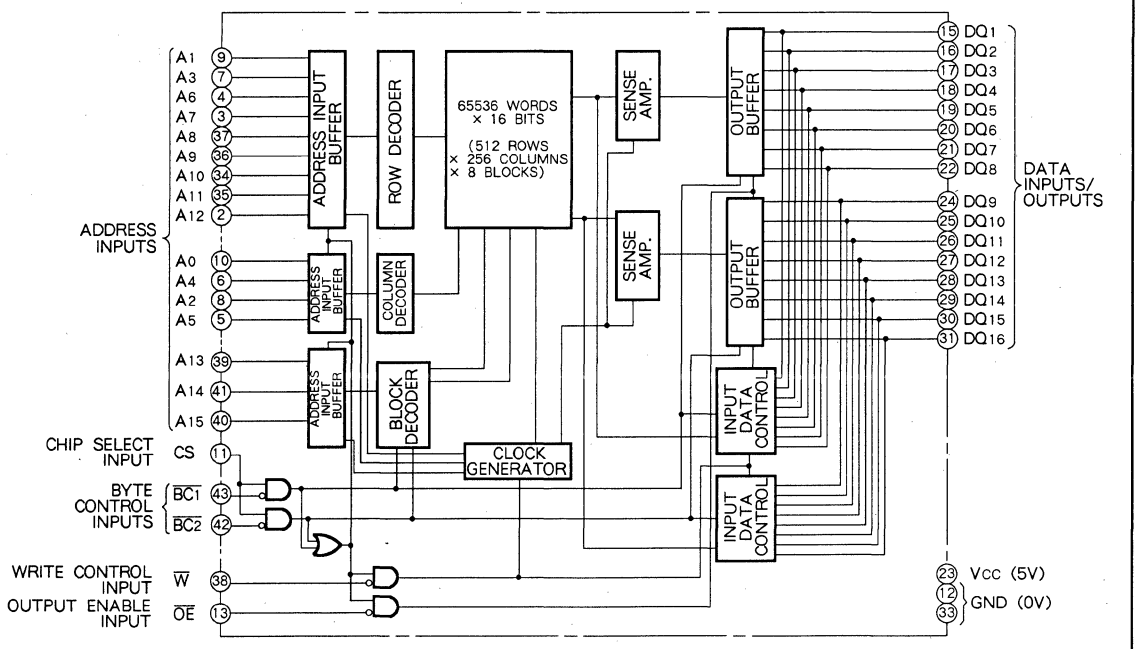
When setting $\overline{BC1}$ and $\overline{BC2}$ at a high level or CS at a low level, the chips are in a non-selectable mode in which both reading and writing are disabled. In this mode, the output stage is in a high-impedance state, allowing OR-tie with other chips and memory expansion by $\overline{BC1}$, $\overline{BC2}$ and CS. The power supply current is reduced as low as the stand-by current which is specified as I_{CC3} or I_{CC4}, and the memory data can be held at +2V power supply, enabling battery back-up operation during powerfailure or power-down operation in the non-selected mode.

FUNCTION TABLE

CS	$\overline{BC1}$	$\overline{BC2}$	$\overline{W}$	$\overline{OE}$	Mode	$DQ_{1\sim8}$	$DQ_{9\sim16}$	I_{CC}
L	X	X	X	X	Non selection	High-Z	High-Z	Stand-by
X	H	H	X	X	Non selection	High-Z	High-Z	Stand-by
H	H	L	L	X	upper-Byte Write	High-Z	Din	Active
H	H	L	H	L	upper-Byte Read	High-Z	Dout	Active
H	H	L	H	H	———	High-Z	High-Z	Active
H	L	H	L	X	Lower-Byte Write	Din	High-Z	Active
H	L	H	H	L	Lower-Byte Read	Dout	High-Z	Active
H	L	H	H	H	———	High-Z	High-Z	Active
H	L	L	L	X	Word Write	Din	Din	Active
H	L	L	H	L	Word Read	Dout	Dout	Active
H	L	L	H	H	———	High-Z	High-Z	Active

(High-Z = High-impedance)

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to GND	−0.3 ~7	V
V_I	Input voltage	With respect to GND	−0.3*~V_{CC} + 0.3	V
V_O	Output voltage	With respect to GND	0~V_{CC}	V
P_d	Power dissipation	Ta = 25℃	1	W
T_{opr}	Operating temperature		0~70	℃
T_{stg}	Storage temperature		−65~150	℃

* − 3.0V in case of AC (Pulse width ≦ 30ns)

DC ELECTRICAL CHARACTERISTICS (Ta = 0~70℃, V_{CC} = 5V ± 10%, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits Min	Limits Typ	Limits Max	Unit
V_{IH}	High-level input voltage			2.2		V_{CC}+0.3V	V
V_{IL}	Low-level input voltage			−0.3*		0.8	V
V_{OH1}	High-level output voltage 1	I_{OH} = −1mA		2.4			V
V_{OH2}	High-level output voltage 2	I_{OH} = −0.1mA		V_{CC}−0.5V			V
V_{OL}	Low-level output voltage	I_{OL} = 2mA				0.4	V
I_I	Input current	V_I = 0~V_{CC}				±1	μA
I_O	Output current in off-state	$\overline{BC_1}$ and $\overline{BC_2}$ = V_{IH} or CS = V_{IL} or $\overline{OE}$ = V_{IH}, $V_{I/O}$ = 0~V_{CC}				±1	μA
I_{CC1}	Active supply current (AC, MOS level)	$\overline{BC_1}$ and $\overline{BC_2}$ ≦ 0.2V, CS ≧ V_{CC} − 0.2V other inputs ≦ 0.2V or ≧ V_{CC} − 0.2V Output-open (duty 100%)	Min cycle		67	95	mA
			1MHz		12	30	
I_{CC2}	Active supply current (AC, TTL level)	$\overline{BC_1}$ and $\overline{BC_2}$ = V_{IL}, CS = V_{IH} other inputs = V_{IH} or V_{IL} Output-open (duty 100%)	Min cycle		70	100	mA
			1MHz		12	30	
I_{CC3}	Stand-by current	1) CS ≦ 0.2V, other inputs = 0~V_{CC} 2) $\overline{BC_1}$ and $\overline{BC_2}$ ≧ V_{CC} − 0.2V CS ≧ V_{CC} − 0.2V other inputs = 0~V_{CC}	-L			100	μA
			-LL			20	
I_{CC4}	Stand-by current	$\overline{BC_1}$ and $\overline{BC_2}$ = V_{IH} or CS = V_{IL}, other inputs = 0~V_{CC}				3	mA

* − 3.0V in case of AC (Pulse width ≦ 30ns)

CAPACITANCE (Ta = 0~70℃, V_{CC} = 5V ± 10%, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits Min	Limits Typ	Limits Max	Unit
C_I	Input capacitance	V_I = GND, V_I = 25mVrms, f = 1MHz			6	pF
C_O	Output capacitance	V_O = GND, V_O = 25mVrms, f = 1MHz			8	pF

Note 1. Direction for current flowing into an IC is positive (no mark).
2. Typical value is V_{CC} = 5V, Ta = 25℃.

AC ELECTRICAL CHARACTERISTICS (T_a = 0~70℃, V_{CC} = 5V ± 10%, unless otherwise noted)

(1) MEASUREMENT CONDITIONS

Input pulse level ·····V_{IH} = 2.4V, V_{IL} = 0.6V

Input rise and fall time·····5ns

Reference level ·····V_{OH} = 1.5V, V_{OL} = 1.5V

Output loads ·····Fig.1, C_L = 100pF (-85L, -85LL, -10L, -10LL)

C_L = 30pF (-70L, 70LL)

C_L = 5pF (for t_{en}, t_{dis})

Transition is measured ± 500mV from steady state voltage.(for t_{en}, t_{dis})

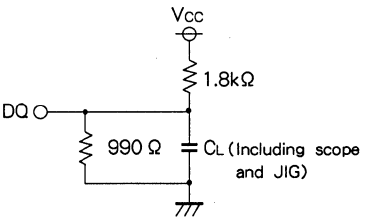


Fig. 1 Output load

(2) READ CYCLE

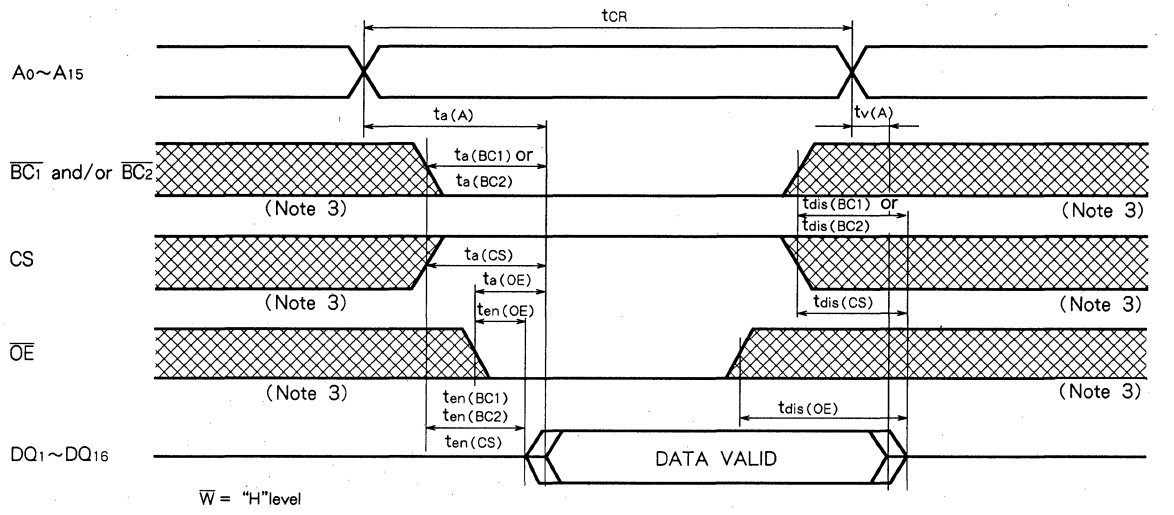
Symbol	Parameter	Limits						Unit
		-70L, -70LL		-85L, -85LL		-10L, -10LL		
		Min	Max	Min	Max	Min	Max	
t_{CR}	Read cycle time	70		85		100		ns
$t_{a(A)}$	Address access time		70		85		100	ns
$t_{a(BC1)}$	Byte control 1 access time		70		85		100	ns
$t_{a(BC2)}$	Byte control 2 access time		70		85		100	ns
$t_{a(CS)}$	Chip select access time		70		85		100	ns
$t_{a(OE)}$	Output enable access time		35		45		50	ns
$t_{dis(BC1)}$	Output disable time after $\overline{BC_1}$ high		25		30		35	ns
$t_{dis(BC2)}$	Output disable time after $\overline{BC_2}$ high		25		30		35	ns
$t_{dis(CS)}$	Output disable time after CS low		25		30		35	ns
$t_{dis(OE)}$	Output disable time after $\overline{OE}$ high		25		30		35	ns
$t_{en(BC1)}$	Output enable time after $\overline{BC_1}$ low	10		10		10		ns
$t_{en(BC2)}$	Output enable time after $\overline{BC_2}$ low	10		10		10		ns
$t_{en(CS)}$	Output enable time after CS high	10		10		10		ns
$t_{en(OE)}$	Output enable time after $\overline{OE}$ low	5		5		5		ns
$t_{v(A)}$	Data valid time after address	10		10		10		ns

(3) WRITE CYCLE

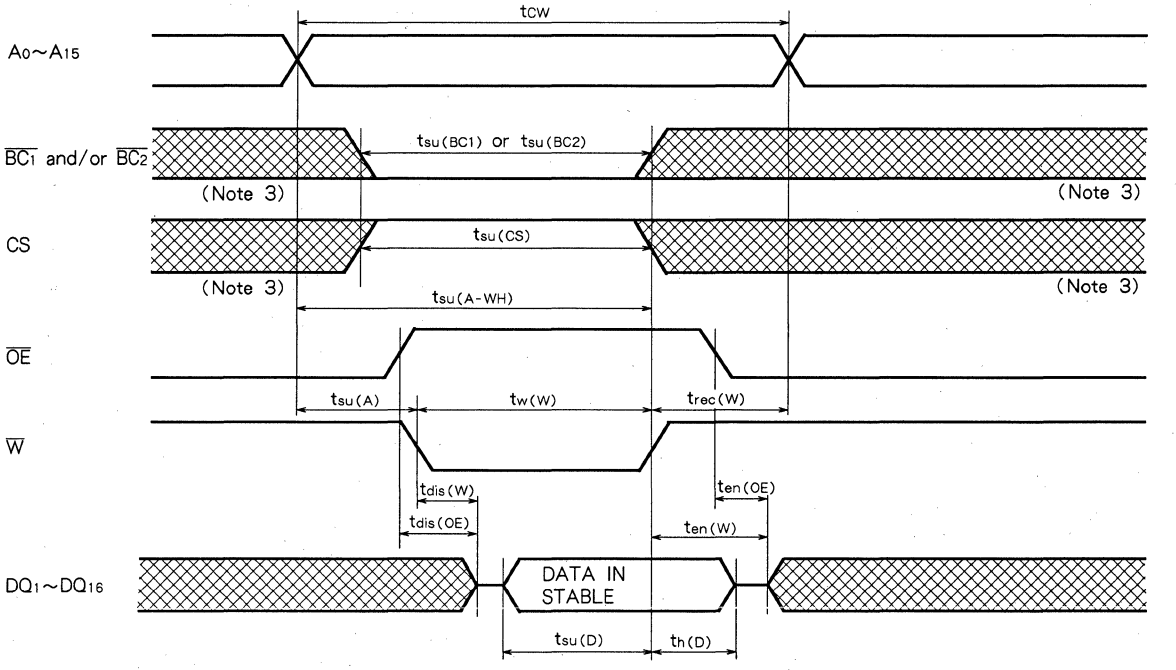
Symbol	Parameter	Limits						Unit
		-70L, -70LL		-85L, -85LL		-10L, -10LL		
		Min	Max	Min	Max	Min	Max	
t_{CW}	Write cycle time	70		85		100		ns
$t_{w(W)}$	Write pulse width	55		65		75		ns
$t_{su(A)}$	Address set up time	0		0		0		ns
$t_{su(A-WH)}$	Address set up time with respect to $\overline{W}$	65		75		85		ns
$t_{su(BC1)}$	Byte control 1 set up time	65		75		85		ns
$t_{su(BC2)}$	Byte control 2 set up time	65		75		85		ns
$t_{su(CS)}$	Chip select set up time	65		75		85		ns
$t_{su(D)}$	Data set up time	30		35		40		ns
$t_{h(D)}$	Data hold time	0		0		0		ns
$t_{rec(W)}$	Write recovery time	0		0		0		ns
$t_{dis(W)}$	Output disable time from $\overline{W}$ low		25		30		35	ns
$t_{dis(OE)}$	Output disable time from $\overline{OE}$ high		25		30		35	ns
$t_{en(W)}$	Output enable time from $\overline{W}$ high	5		5		5		ns
$t_{en(OE)}$	Output enable time from $\overline{OE}$ low	5		5		5		ns

(4) TIMING DIAGRAMS

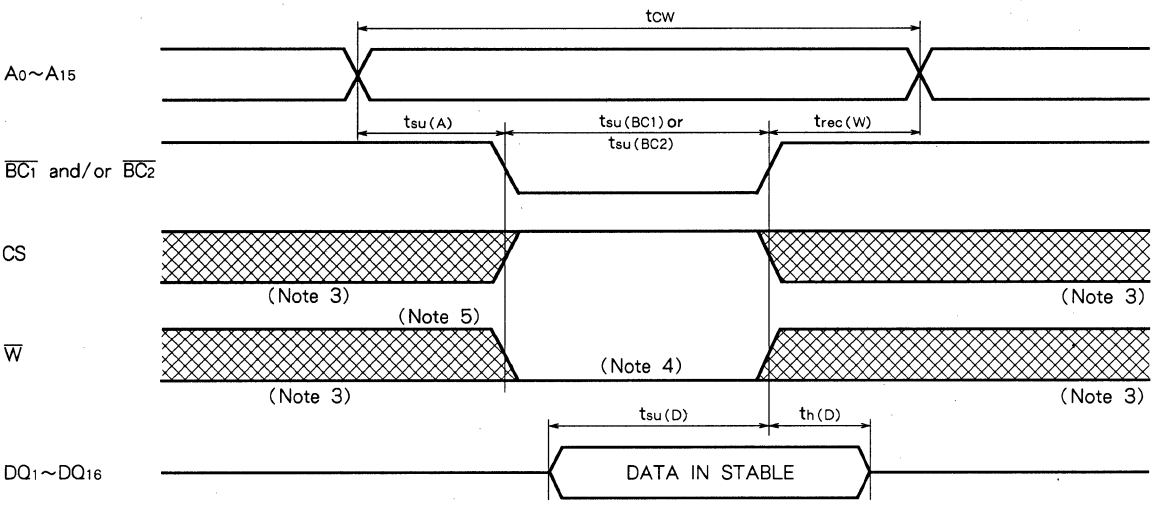
Read cycle



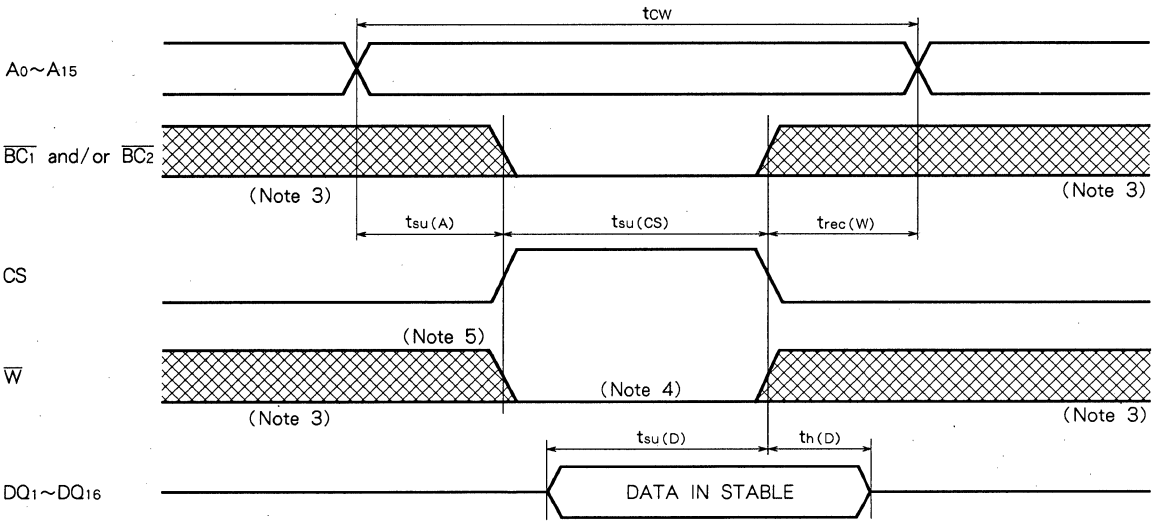
Write cycle ($\overline{W}$ control mode)



Write cycle ($\overline{BC}$ control mode)



Write cycle (CS control mode)



Note 3. Hatching indicates the state is "don't care".
4. Writing is executed while CS high overlaps $\overline{BC1}$ and/or $\overline{BC2}$ low and $\overline{W}$ low.
5. When the falling edge of $\overline{W}$ is simultaneously or prior to the falling edge of $\overline{BC1}$ and/or $\overline{BC2}$ or rising edge of CS, the outputs are maintained in the high impedance state.
6. Don't apply inverted phase signal externally when DQ pin is output mode.

POWER DOWN CHARACTERISTICS

(1) ELECTRICAL CHARACTERISTICS (T_a = 0~70℃, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ	Max	
$V_{CC(PD)}$	Power down supply voltage			2			V
$V_{I(BC)}$	Byte control input $\overline{BC_1}$ & $\overline{BC_2}$	2.2V ≦ $V_{CC(PD)}$		2.2			V
		2V ≦ $V_{CC(PD)}$ ≦ 2.2V			$V_{CC(PD)}$		
$V_{I(CS)}$	Chip select input CS	4.5V ≦ $V_{CC(PD)}$				0.8	V
		$V_{CC(PD)}$ < 4.5V				0.2	
$I_{CC(PD)}$	Power down supply current	V_{CC} = 3V 1) CS ≦ 0.2V, other inputs = 0~3V 2) $\overline{BC_1}$ and $\overline{BC_2}$ ≧ V_{CC} − 0.2V, CS ≧ V_{CC} − 0.2V, other inputs = 0~3V	-L			50	μA
			-LL		0.3	10 (Note 7)	

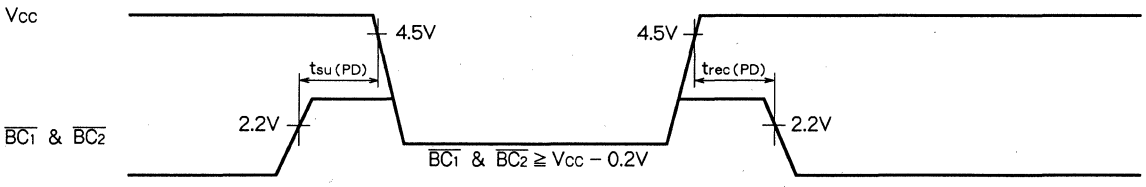
Note 7. $I_{CC(PD)}$ = 1 μA in case of T_a = 25℃.

(2) TIMING REQUIREMENTS (T_a = 0~70℃, unless otherwise noted)

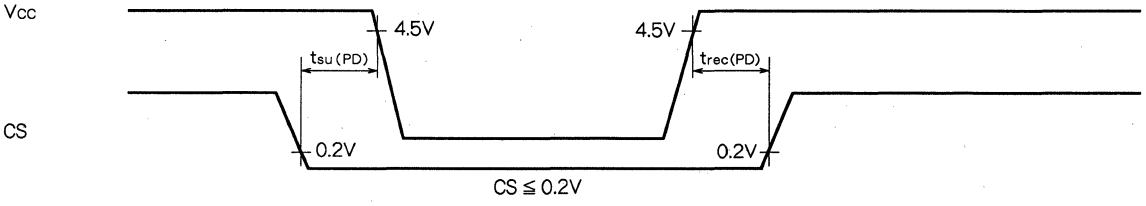
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{su(PD)}$	Power down set up time		0			ns
$t_{rec(PD)}$	Power down recovery time		5			ms

(3) POWER DOWN CHARACTERISTICS

$\overline{BC}$ control mode



CS control mode



M5M51016BTP,RT-70L,-10L, -70LL,-10LL

1048576-BIT(65536-WORD BY 16-BIT)CMOS STATIC RAM

DESCRIPTION

The M5M51016BTP, RT are a 1048576-bit CMOS static RAM organized as 65536 word by 16-bit which are fabricated using high-performance triple polysilicon CMOS technology. The use of resistive load NMOS cells and CMOS periphery result in a high density and low power static RAM.

They are low stand-by current and low operation current and ideal for the battery back-up application.

The M5M51016BTP,RT are packaged in a 44-pin thin small outline package which is a high reliability and high density surface mount device (SMD). Two types of devices are available. M5M51016BTP(normal lead bend type package), M5M51016BRT (reverce lead bend type package). Using both types of devices, it becomes very easy to design a printed circuit board.

FEATURES

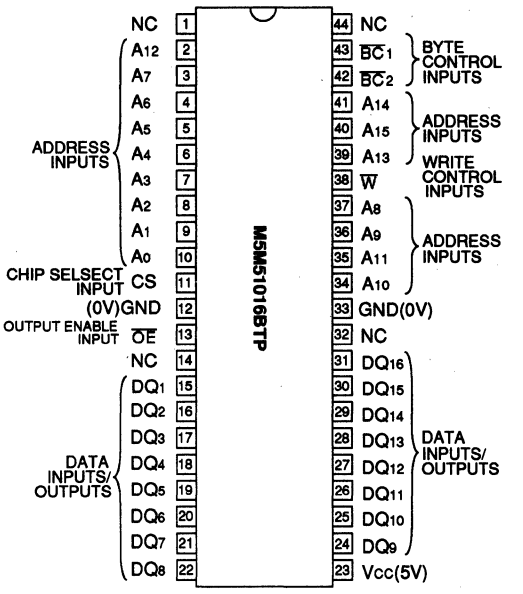
Type name	Access time (max)	Power supply current	
		Active (max)	stand-by (max)
M5M51016BTP,RT-70L M5M51016BTP,RT-10L	70ns 100ns	30mA (1MHz)	100 μA (Vcc = 5.5V)
M5M51016BTP,RT-70LL M5M51016BTP,RT-10LL	70ns 100ns		20 μA (Vcc = 5.5V) 0.3 μA (Vcc = 3.0V, typ)

- Single +5V power supply
- Low stand-by current 0.3 μA (typ.)
- Directly TTL compatible : All inputs and outputs
- Easy memory expansion and power down by CS, $\overline{BC}_1$ & $\overline{BC}_2$
- Data hold on +2V power supply
- Three-state outputs : OR-tie capability
- $\overline{OE}$ prevents data contention in the I/O bus
- Common data I/O
- Package
  M5M51016BTP,RT ..... 44pin 400mil TSOP(II)

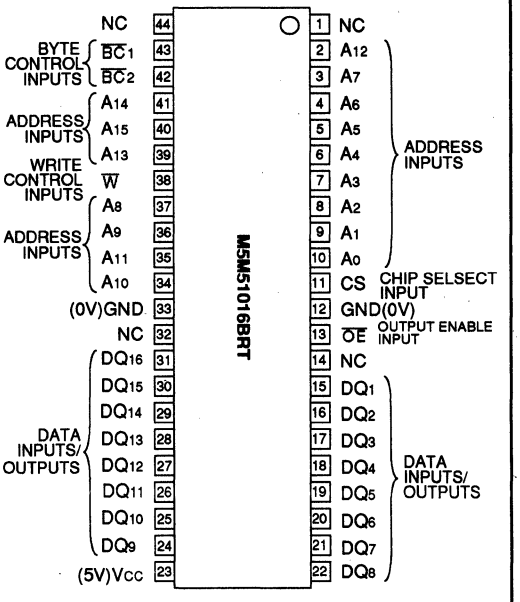
APPLICATION

Small capacity memory units

PIN CONFIGURATION (TOP VIEW)



Outline 44P3W - H (400mil TSOP Normal Bend)



Outline 44P3W - J (400mil TSOP Reverse Bend)

NC : NO CONNECTION

FUNCTION

The operation mode of the M5M51016B serieas are determined by a combination of the device control inputs $\overline{BC}_1$, $\overline{BC}_2$, CS, $\overline{W}$ and $\overline{OE}$. Each mode is summarized in the function table.

A write cycle is executed whenever the low level $\overline{W}$ overlaps with the low level $\overline{BC}_1$ and/or $\overline{BC}_2$ and the high level CS. The address must be set up before the write cycle and must be stable during the entire cycle.

The data is latched into a cell on the trailing edge of $\overline{W}$, $\overline{BC}_1$, $\overline{BC}_2$ or CS, whichever occurs first, requiring the set-up and hold time relative to these edge to be maintained. The output enable input $\overline{OE}$ directly controls the output stage. Setting the $\overline{OE}$ at a high level, the output stage is in a high-impedance state, and the databus contention problem in the write cycle is eliminated.

A read cycle is executed by setting $\overline{W}$ at a high level and $\overline{OE}$ at a low level while $\overline{BC}_1$ and/or $\overline{BC}_2$ and CS are in an active state. ($\overline{BC}_1$ and/or $\overline{BC}_2$=L,CS=H)

When setting $\overline{BC}_1$ at a high level and the other pins are in an active state, upper-Byte are in a selectable mode in which both reading and writing are enabled, and lower-Byte are in a non-selectable mode.And when setting $\overline{BC}_2$ at a high level and the other pins are in an active state, lower-Byte are in a selectable mode and upper -Byte are in a non-selectable mode.

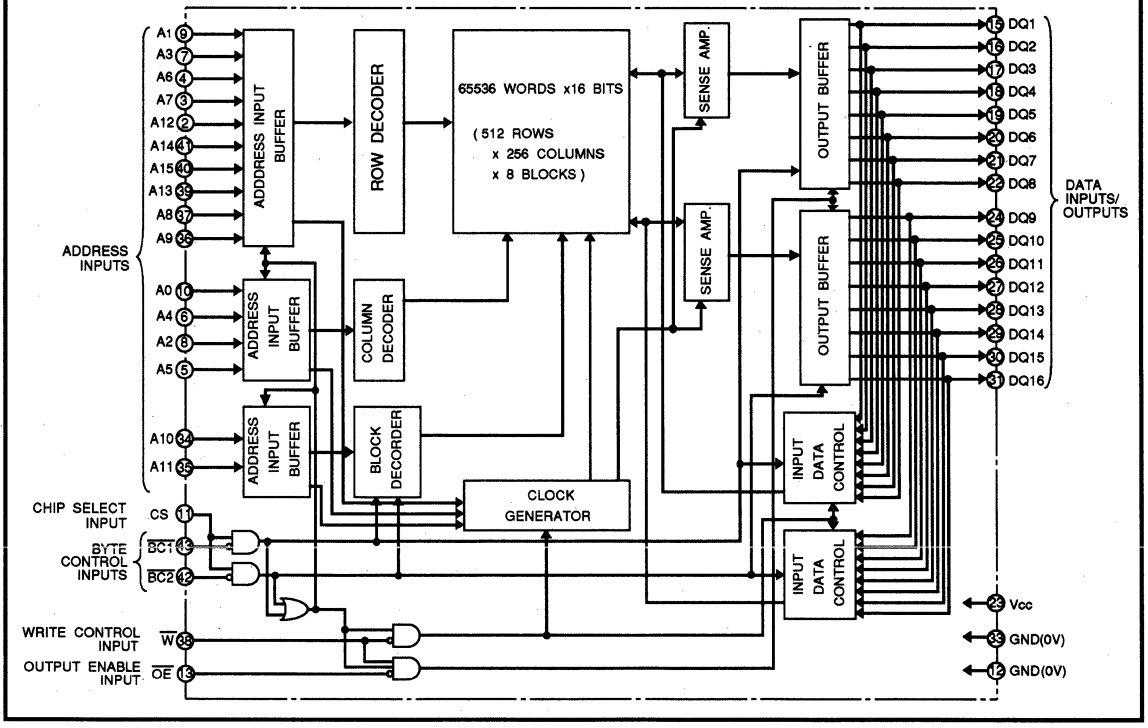
When setting $\overline{BC}_1$ and $\overline{BC}_2$ at a high level or CS at a low level, the chips are in a non-selectable mode in which both reading and writing are disabled.

In this mode, the output stage is in a high-impedance state, allowing OR-tie with other chips and memory expansion by $\overline{BC}_1$, $\overline{BC}_2$ and CS. The power supply current is reduced as low as the stand-by current which is specified as I_{CC3} or I_{CC4}, and the memory data can be held at +2V power supply, enabling battery back-up operation during powerfailure or power-down operation in the non-selected mode.

CS	$\overline{BC}_1$	$\overline{BC}_2$	$\overline{W}$	$\overline{OE}$	Mode	$DQ_{1\sim8}$	$DQ_{9\sim16}$	I_{CC}
L	X	X	X	X	Non selection	High-Z	High-Z	Stand-by
X	H	H	X	X	Non selection	High-Z	High-Z	Stand-by
H	H	L	L	X	Upper-Byte Write	High-Z	Din	Active
H	H	L	H	L	Upper-Byte Read	High-Z	Dout	Active
H	H	L	H	H	————	High-Z	High-Z	Active
H	L	H	L	X	Lower-Byte Write	Din	High-Z	Active
H	L	H	H	L	Lower-Byte Read	Dout	High-Z	Active
H	L	H	H	H	————	High-Z	High-Z	Active
H	L	L	L	X	Word Write	Din	Din	Active
H	L	L	H	L	Word Read	Dout	Dout	Active
H	L	L	H	H	————	High-Z	High-Z	Active

(High-Z=High-impedance)

BLOCK DIAGROM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to GND	−0.3～7	V
V_I	Input voltage		−0.3*～Vcc + 0.3	V
V_O	Output voltage		0～Vcc	V
P_d	Power dissipation	Ta=25℃	1	W
T_{opr}	Operating temperature		0～70	℃
T_{stg}	Storage temperature		−65～150	℃

* −3.0V in case of AC (Pulse width ≦ 30ns)

DC ELECTRICAL CHARACTERISTICS (Ta=0~70℃, Vcc=5V±10%, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits Min	Limits Typ	Limits Max	Unit
V_{IH}	High-level input voltage			2.2		Vcc+0.3V	V
V_{IL}	Low-level input voltage			−0.3*		0.8	V
V_{OH1}	High-level output voltage 1	I_{OH} = −1mA		2.4			V
V_{OH2}	High-level output voltage 2	I_{OH} = −0.1mA		Vcc−0.5V			V
V_{OL}	Low-level output voltage	I_{OL} = 2mA				0.4	V
I_I	Input current	V_I =0～Vcc				±1	μA
I_O	Output current in off-state	$\overline{BC}_1$ and $\overline{BC}_2$ = V_{IH} or CS = V_{IL} or $\overline{OE}$ = V_{IH}, $V_{I/O}$ = 0～Vcc				±1	μA
I_{CC1}	Active supply current (AC,MOS level)	$\overline{BC}_1$ and $\overline{BC}_2$ ≦0.2V, CS≧Vcc-0.2V other inputs ≦ 0.2V or Vcc-0.2V Output-open(duty 100%)	Min cycle		65	95	mA
			1MHz		8	30	mA
I_{CC2}	Active supply current (AC,TTL level)	$\overline{BC}_1$ and $\overline{BC}_2$ = V_{IL}, CS = V_{IH} other inputs = V_{IH} or V_{IL} Output-open(duty 100%)	Min cycle		70	100	mA
			1MHz		10	30	mA
I_{CC3}	Stand-by current	1) CS≦0.2V, other inputs = 0～Vcc	-L			100	μA
		2) $\overline{BC}_1$,$\overline{BC}_2$≧Vcc−0.2V, CS≧Vcc−0.2V other inputs = 0～Vcc	-LL			20	μA
I_{CC4}	Stand-by current	$\overline{BC}_1$ and $\overline{BC}_2$ = V_{IH} or CS = V_{IL}, other inputs = 0～Vcc				3	mA

* −3.0V in case of AC (Pulse width ≦ 30ns)

CAPACITANCE (Ta=0~70℃, Vcc=5V±10%, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits Min	Limits Typ	Limits Max	Unit
C_I	Input capacitance	V_I=GND, V_I=25mVrms, f=1MHz			6	pF
C_O	Output capacitance	V_O=GND,V_O=25mVrms, f=1MHz			8	pF

Note 1: Direction for current flowing into an IC is positive (no mark).
2: Typical value is Vcc = 5V, Ta = 25℃

AC ELECTRICAL CHARACTERISTICS (Ta = 0~70℃, Vcc = 5V±10%, unless otherwise noted)

(1) MEASUREMENT CONDITIONS

Input pulse level ..... V_{IH} = 2.4V, V_{IL} = 0.6V
Input rise and fall time 5ns
Reference level ..... V_{OH} = 1.5V, V_{OL} = 1.5V
Output loads ..... Fig.1, C_L = 100pF (-10L,-10LL)
C_L = 30pF (-70L,-70LL)
C_L = 5pF (for t_{en}, t_{dis})
Transition is measured ±500mV from steady state voltage. (for t_{en}, t_{dis})

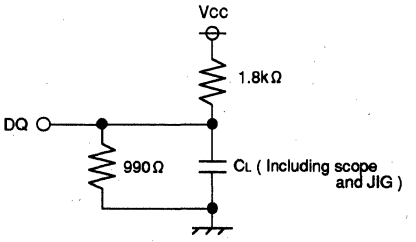


Fig.1 Output load

(2) READ CYCLE

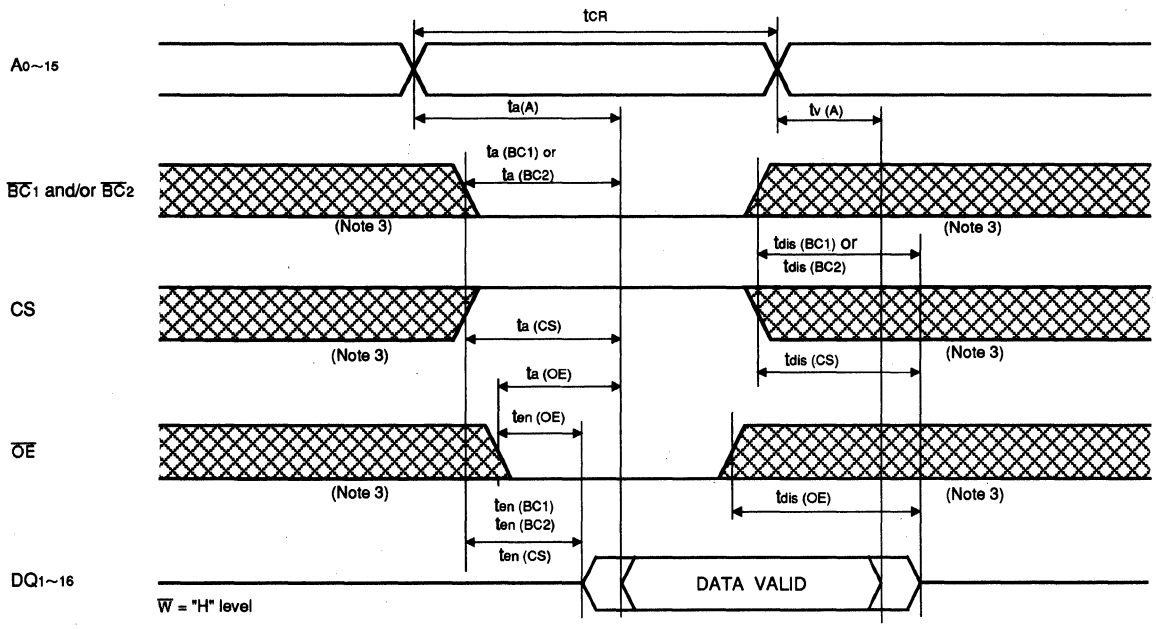
Symbol	Parameter	Limits				Unit
		M5M51016B -70L,-70LL		M5M51016B -10L,-10LL		
		Min	Max	Min	Max	
t_{CR}	Read cycle time	70		100		ns
$t_{a(A)}$	Address access time		70		100	ns
$t_{a(BC1)}$	Byte controle 1 access time		70		100	ns
$t_{a(BC2)}$	Byte controle 2 access time		70		100	ns
$t_{a(CS)}$	Chip select access time		70		100	ns
$t_{dis(OE)}$	Output enable access time		35		50	ns
$t_{dis(BC1)}$	Output disable time after $\overline{BC}_1$ high		25		35	ns
$t_{dis(BC2)}$	Output disable time after $\overline{BC}_2$ high		25		35	ns
$t_{dis(CS)}$	Output disable time after CS low		25		35	ns
$t_{dis(OE)}$	Output disable time after $\overline{OE}$ high		25		35	ns
$t_{en(BC1)}$	Output enable time after $\overline{BC}_1$ low	10		10		ns
$t_{en(BC2)}$	Output enable time after $\overline{BC}_2$ low	10		10		ns
$t_{en(CS)}$	Output enable time after CS high	10		10		ns
$t_{en(OE)}$	Output enable time after $\overline{OE}$ low	5		5		ns
$t_{v(A)}$	Data valid time after address	10		10		ns

(3) WRITE CYCLE

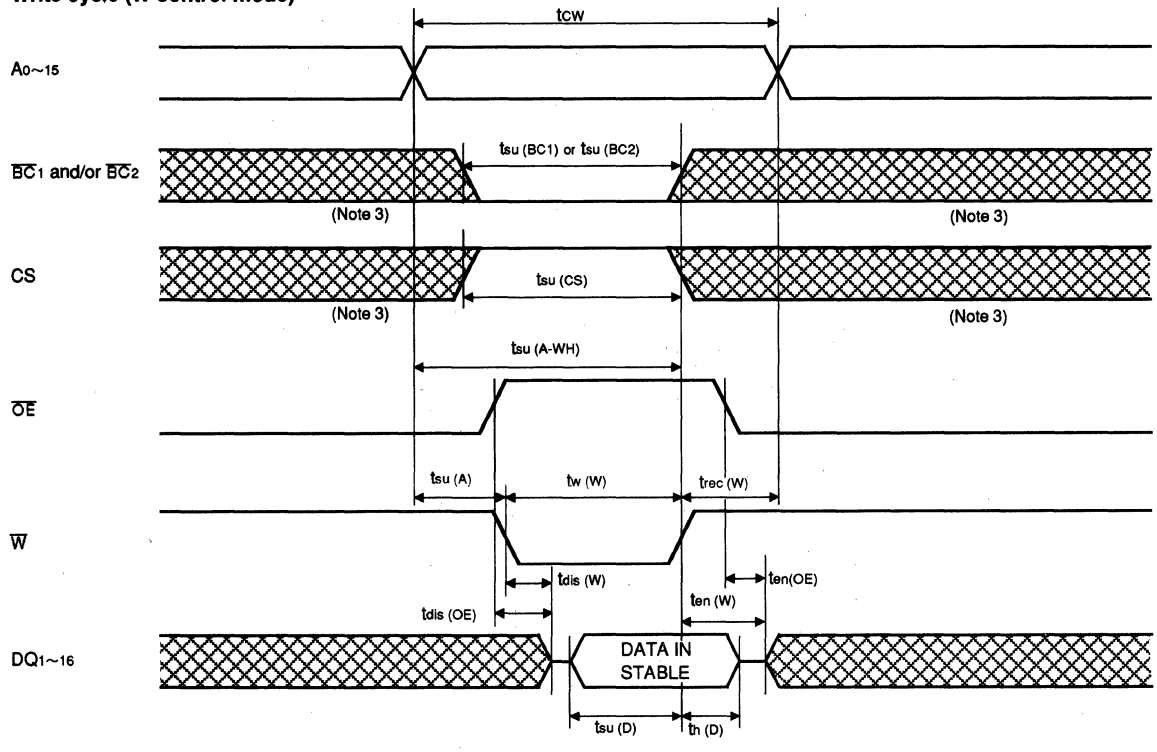
Symbol	Parameter	Limits				Unit
		M5M51016B -70L,-70LL		M5M51016B -10L,-10LL		
		Min	Max	Min	Max	
t_{CW}	Write cycle time	70		100		ns
$t_{w(W)}$	Write pulse width	55		75		ns
$t_{su(A)}$	Address set up time	0		0		ns
$t_{su(A-WH)}$	Address set up time with respect to $\overline{W}$	65		85		ns
$t_{su(BC1)}$	Byte controle 1 setup time	65		85		ns
$t_{su(BC2)}$	Byte controle 2 setup time	65		85		ns
$t_{su(CS)}$	Chip select set up time	65		85		ns
$t_{su(D)}$	Data set up time	30		40		ns
$t_{h(D)}$	Data hold time	0		0		ns
$t_{rec(W)}$	Write recovery time	0		0		ns
$t_{dis(W)}$	Output disable time from $\overline{W}$ low		25		35	ns
$t_{dis(OE)}$	Output disable time from $\overline{OE}$ high		25		35	ns
$t_{en(W)}$	Output enable time from $\overline{W}$ high	5		5		ns
$t_{en(OE)}$	Output enable time from $\overline{OE}$ low	5		5		ns

(4) TIMING DIAGRAMS

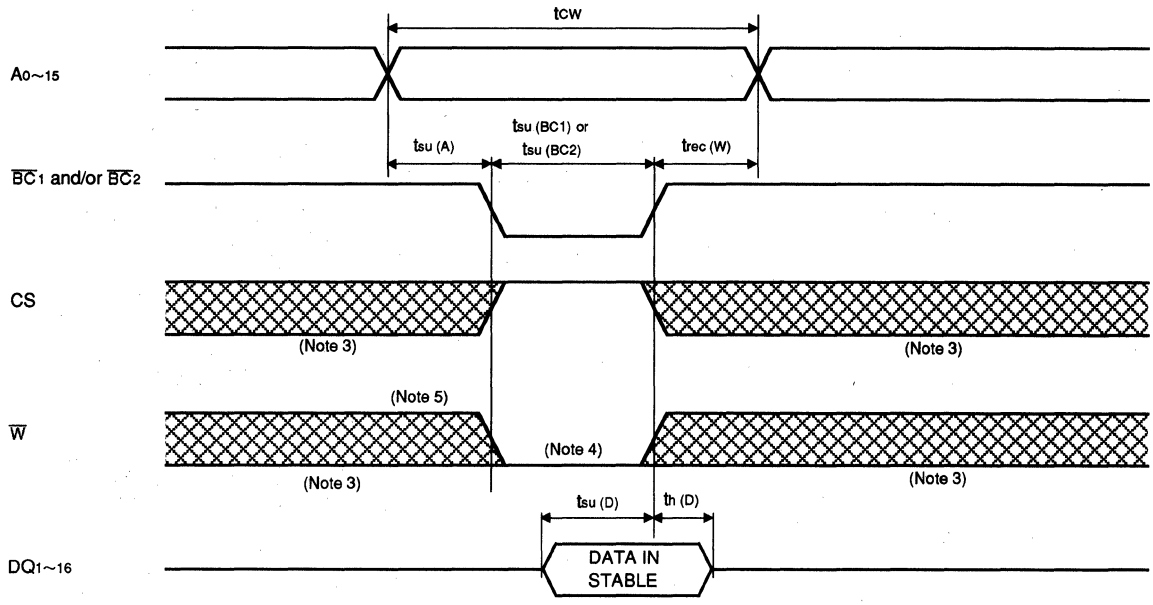
Read cycle



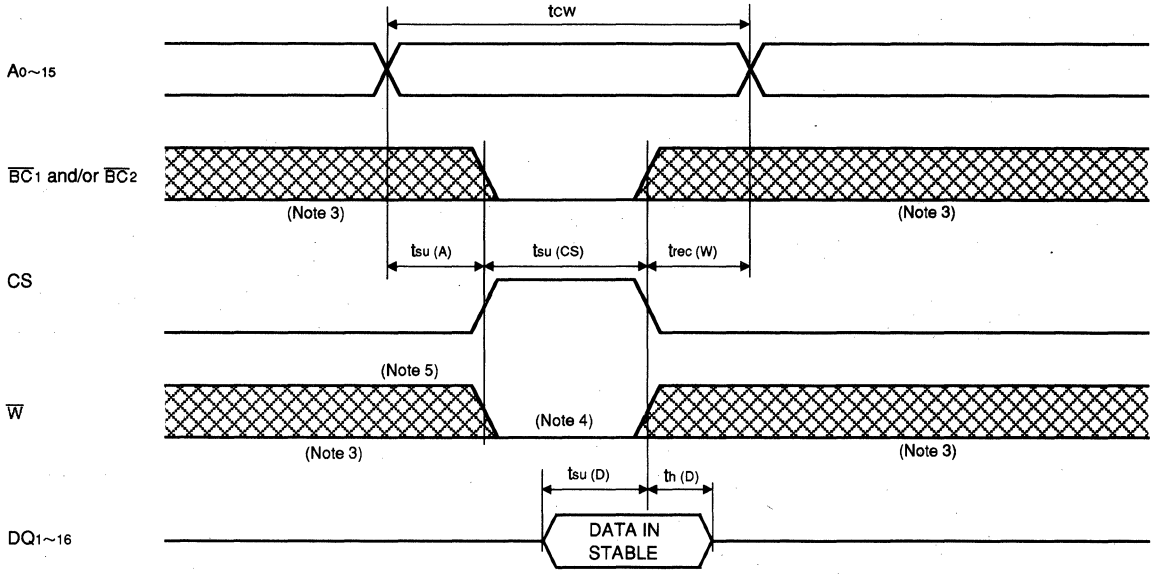
Write cycle (W control mode)



Write cycle ($\overline{BC}$ control mode)



Write cycle (CS control mode)



Note 3: Hatching indicates the state is "don't care".
4: Writing is executed while CS high overlaps $\overline{BC}_1$ and/or $\overline{BC}_2$ low and $\overline{W}$ low.
5: When the falling edge of $\overline{W}$ is simultaneously or prior to the falling edge of $\overline{BC}_1$ and/or $\overline{BC}_2$ or rising edge of CS, the outputs are maintained in the high impedance state.
6: Don't apply inverted phase signal externally when DQ pin is output mode.

POWER DOWN CHARACTERISTICS

(1) ELECTRICAL CHARACTERISTICS (Ta = 0~70℃, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits Min	Limits Typ	Limits Max	Unit
$V_{CC(PD)}$	Power down supply voltage			2			V
$V_{I(\overline{BC})}$	Byte control input $\overline{BC}_1$ & $\overline{BC}_2$	2.2V ≦ $V_{CC(PD)}$		2.2			V
		2V ≦ $V_{CC(PD)}$ ≦ 2.2V			$V_{CC(PD)}$		
$V_{I(CS)}$	Chip select input CS	4.5V ≦ $V_{CC(PD)}$				0.8	V
		$V_{CC(PD)}$ < 4.5V				0.2	
$I_{CC(PD)}$	Power down supply current	Vcc = 3V 1) CS ≦ 0.2V other inputs = 0~3V 2) $\overline{BC}_1$ & $\overline{BC}_2$ ≧ Vcc−0.2V, CS≧Vcc−0.2V,other inputs=0~3V	-L			50	μA
			-LL		0.3	10 (Note 7)	

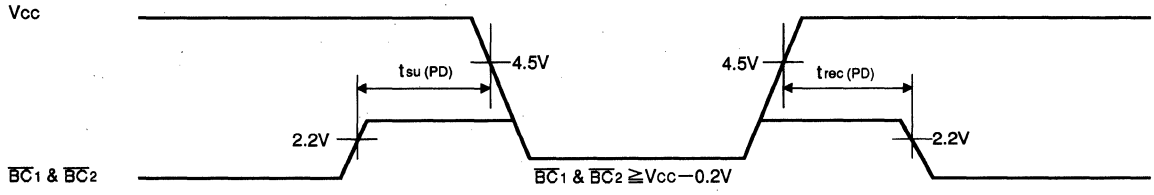
Note7. $I_{CC(PD)}$ = 1 μA in case of Ta = 25℃

(2) TIMING REQUIREMENTS (Ta = 0~70℃, unless otherwise noted)

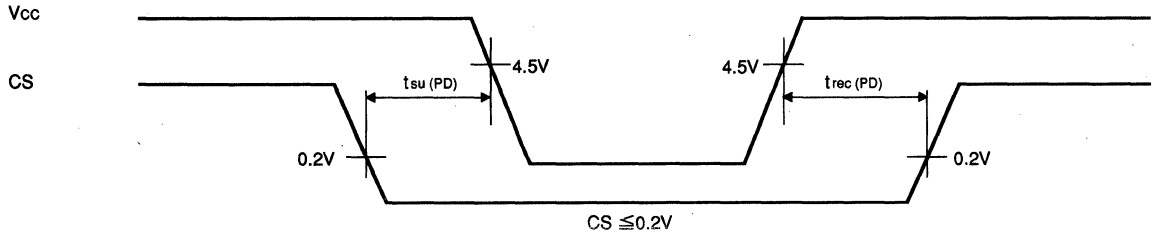
Symbol	Parameter	Test conditions	Limits Min	Limits Typ	Limits Max	Unit
$t_{su(PD)}$	Power down set up time		0			ns
$t_{rec(PD)}$	Power down recovery time		5			ms

(3) POWER DOWN CHARACTERISTICS

$\overline{BC}$ control mode



CS control mode



M5M5408FP,TP,RT-55L,-70L,-10L, -55LL,-70LL,-10LL

4194304-BIT (524288-WORD BY 8-BIT) CMOS STATIC RAM

DESCRIPTION

The M5M5408 is 4194304-bit CMOS static RAM organized as 524288-words by 8-bit, fabricated using high-performance quadruple-polysilicon and double metal CMOS technology.
The use of thin film transistor (TFT) load cells and CMOS periphery results in a high density and low power static RAM. The M5M5408 is designed for memory applications where the high performance, high reliability, large storage, simple interfacing and battery back-up are important design objectives.

The M5M5408 is offered in 32-pin plastic small outline package (SOP) and 32-pin thin small outline package (TSOP), providing high board level packing densities. Two types of TSOP packages are available, M5M5408TP (normal lead bend type package) and M5M5408RT (reverse lead bend type package). Using both two types makes it easy to design a printed circuit board.

FEATURES

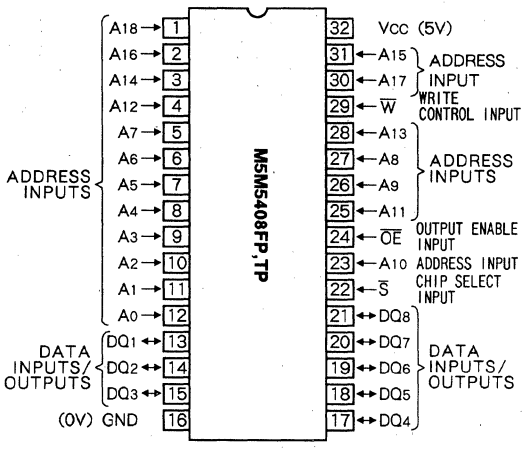
Type name	Access time (max)	Power supply current	
		Active (max)	Stand-by (max)
M5M5408FP, TP, RT-55L M5M5408FP, TP, RT-70L M5M5408FP, TP, RT-10L	55ns 70ns 100ns	30mA (1MHz)	100μA (Vcc = 5.5V)
M5M5408FP, TP, RT-55LL M5M5408FP, TP, RT-70LL M5M5408FP, TP, RT-10LL	55ns 70ns 100ns		20μA (Vcc = 5.5V) 0.4μA (Vcc = 3V, typ)

- Single + 5V power supply
- No clocks, no refresh
- All inputs and outputs are TTL compatible
- Easy memory expansion and power down by $\overline{S}$
- Data retention supply voltage = 2.0V to 5.5V
- Three-state outputs : OR-tie capability
- $\overline{OE}$ prevents data contention in the I/O bus
- Common data I/O
- Small stand-by current ·····0.4μA (typ)
- Battery back-up capability
- Package
  M5M5408FP : 32-pin 525mil SOP
  M5M5408TP : 32-pin 400mil TSOP (II)
  M5M5408RT : 32-pin 400mil TSOP (II)

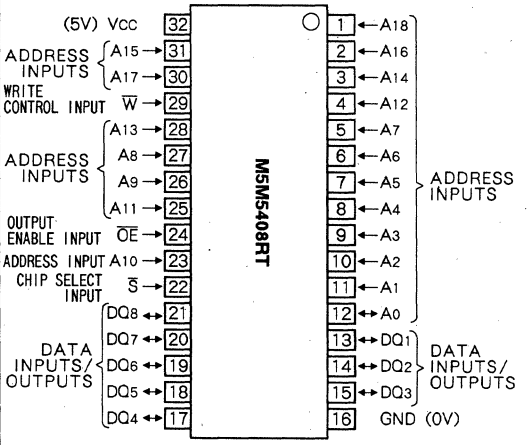
APPLICATION

Small capacity memory units, IC card, battery operating system

PIN CONFIGURATION (TOP VIEW)



Outline 32P2M-A(FP)
32P3Y-H(TP)

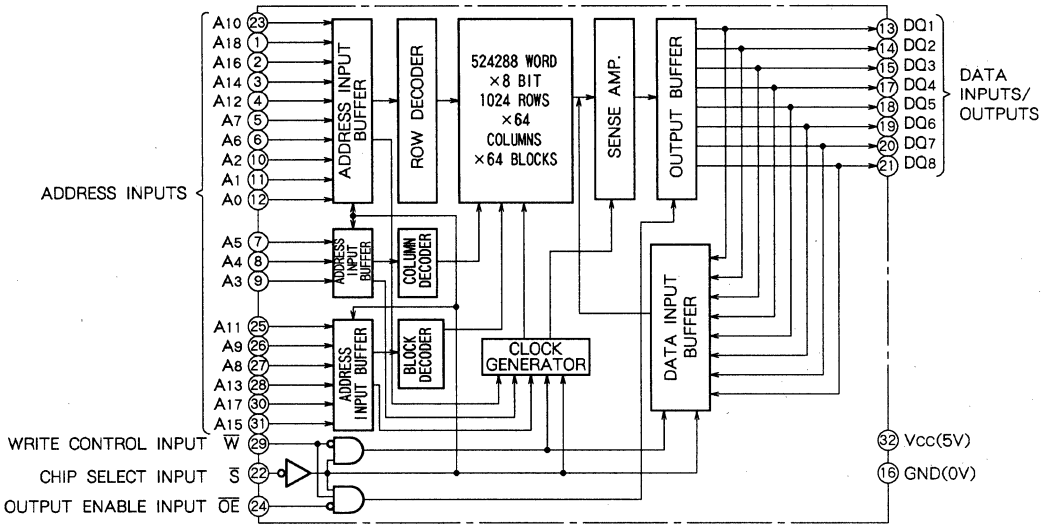


Outline 32P3Y-J

M5M5408FP,TP,RT-55L,-70L,-10L, -55LL,-70LL,-10LL

4194304-BIT (542488-WORD BY 8-BIT) CMOS STATIC RAM

BLOCK DIAGRAM



FUNCTION

The operation mode of the M5M5408 is determined by a combination of the device control inputs $\overline{S}$, $\overline{W}$ and $\overline{OE}$. Each mode is summarized in the function table.

A write cycle is executed whenever the low level $\overline{W}$ overlaps with the low level $\overline{S}$. The address must be set up before the write cycle and must be stable during the entire cycle. The data is latched into a cell on the trailing edge of $\overline{W}$, or $\overline{S}$ whichever occurs first, requiring the set-up and hold time relative to these edge to be maintained. The output enable input $\overline{OE}$ directly controls the output state. Setting the $\overline{OE}$ at a high level, the output state is in a highimpedance state, and the data bus contention problem in the write cycle is eliminated.

A read cycle is executed by setting $\overline{W}$ at a high level and $\overline{OE}$ at a low level while $\overline{S}$ is in an active state ($\overline{S}$ = L).

When setting $\overline{S}$ at a high level, the chips are in a non-selectable mode in which both reading and writing are disabled. In this mode, the output state is in a high-impedance state, allowing OR-tie with other chips and memory expansion by $\overline{S}$. The power supply current is reduced as low as the stand-by current which is specified as I_{CC3} or I_{CC4}, and the memory data can be held at +2V power supply, enabling battery back-up operation during power failure or power-down operation in the non-selected mode.

FUNCTION TABLE

$\overline{S}$	$\overline{W}$	$\overline{OE}$	Mode	DQ	Icc
H	X	X	Non selection	High-impedance	Stand-by
L	L	X	Write	Din	Active
L	H	L	Read	Dout	Active
L	H	H		High-impedance	Active

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to GND	− 0.3~7	V
V_I	Input voltage		− 0.3 * ~V_{CC} + 0.3	V
V_O	Output voltage		0~V_{CC}	V
P_d	Power dissipation	T_a = 25℃	700	mW
T_{opr}	Operating temperature		0~70	℃
T_{stg}	Storage temperature		− 65~150	℃

* − 3.0V in case of AC (Pulse width ≦ 50ns)

DC ELECTRICAL CHARACTERISTICS (T_a = 0~70℃, V_{CC} = 5V ± 10%, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits Min	Limits Typ	Limits Max	Unit
V_{IH}	High-level input voltage			2.2		V_{CC}+0.3	V
V_{IL}	Low-level input voltage			− 0.3 *		0.8	V
V_{OH}	High-level output voltage	I_{OH} = − 1mA		2.4			V
		I_{OH} = − 0.1mA		V_{CC}-0.5			
V_{OL}	Low-level output voltage	I_{OL} = 2.1mA				0.4	V
I_I	Input leakage current	V_I = 0~V_{CC}				± 1	μA
I_O	Output leakage current	$\overline{S}$ = V_{IH}, $\overline{OE}$ = V_{IH}, $V_{I/O}$ = 0~V_{CC}				± 1	μA
I_{CC1}	Active supply current (AC, MOS level)	$\overline{S}$ ≦ 0.2 other inputs ≦ 0.2V or ≧ V_{CC}-0.2V Output-open (duty 100%)	minimum cycle		50	80	mA
			1MHz		25	30	
I_{CC2}	Active supply current (AC, TTL level)	$\overline{S}$ = V_{IL} other inputs = V_{IH} or V_{IL} Output-open (duty 100%)	minimum cycle		60	90	mA
			1MHz		30	40	
I_{CC3}	Stand by current	$\overline{S}$ ≧ V_{CC} − 0.2V, other inputs = 0~V_{CC}	FP,TP, RT-L			100	μA
			FP,TP, RT-LL		1.0	20	
I_{CC4}	Stand by current	$\overline{S}$ = V_{IH}, other inputs = 0~V_{CC}				3	mA

* − 3.0V in case of AC (Pulse width ≦ 50ns)

CAPACITANCE (T_a = 0~70℃, V_{CC} = 5V ± 10%, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits Min	Limits Typ	Limits Max	Unit
C_I	Input capacitance	V_I = GND, V_I = 25mVrms, f = 1MHz			6	pF
C_O	Output capacitance	V_O = GND, V_O = 25mVrms, f = 1MHz			8	pF

Note 1. Direction for current flowing into an IC is positive (no mark).
2. Typical value is V_{CC} = 5V, T_a = 25℃.

AC ELECTRICAL CHARACTERISTICS (T_a = 0~70℃, V_{CC} = 5V ± 10%, unless otherwise noted)

(1) MEASUREMENT CONDITIONS

Input pulse levels ····· V_{IH} = 2.4V, V_{IL} = 0.6V

Input rise and fall time ····· 5ns

Reference levels ····· V_{OH} = V_{OL} = 1.5V

Transition in measured ± 500mV from steady state voltage.(for t_{en}, t_{dis})

Output loads ····· Fig.1, C_L = 100pF (FP, TP, RT-10L, -10LL)

C_L = 30pF (FP, TP, RT-55L, -70L, -55LL, -70LL)

C_L = 5pF (for t_{en}, t_{dis})

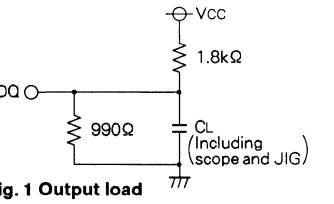


Fig. 1 Output load

(2) READ CYCLE

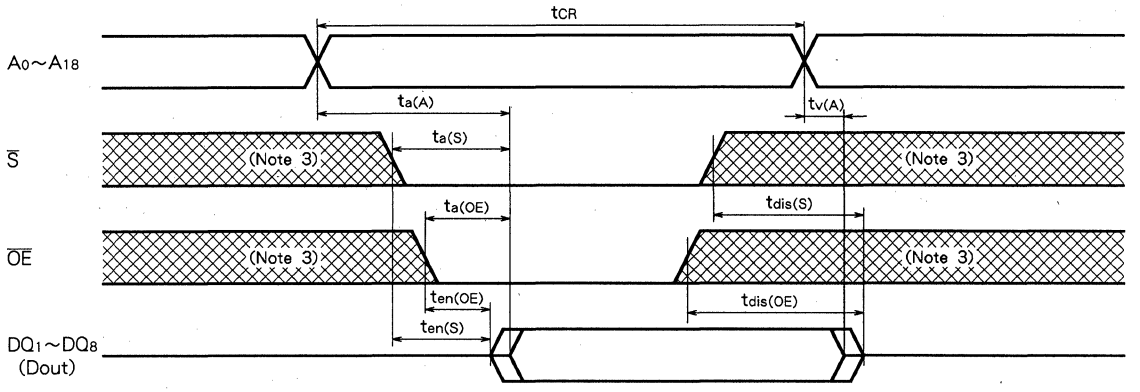
Symbol	Parameter	Limits						Unit
		M5M5408FP, TP, RT-55L, -55LL		M5M5408FP, TP, RT-70L, -70LL		M5M5408FP, TP, RT-10L, -10LL		
		Min	Max	Min	Max	Min	Max	
t_{CR}	Read cycle time	55		70		100		ns
$t_{a(A)}$	Address access time		55		70		100	ns
$t_{a(S)}$	Chip select access time		55		70		100	ns
$t_{a(OE)}$	Output enable access time		25		35		50	ns
$t_{dis(S)}$	Output disable time after $\overline{S}$ high		20		25		35	ns
$t_{dis(OE)}$	Output disable time after $\overline{OE}$ high		20		25		35	ns
$t_{en(S)}$	Output enable time after $\overline{S}$ low	10		10		10		ns
$t_{en(OE)}$	Output enable time after $\overline{OE}$ low	5		5		5		ns
$t_{v(A)}$	Data valid time after address	10		10		10		ns

(3) WRITE CYCLE

Symbol	Parameter	Limits						Unit
		M5M5408FP, TP, RT-55L, -55LL		M5M5408FP, TP, RT-70L, -70LL		M5M5408FP, TP, RT-10L, -10LL		
		Min	Max	Min	Max	Min	Max	
t_{CW}	Write cycle time	55		70		100		ns
$t_{w(W)}$	Write pulse width	40		50		60		ns
$t_{su(A)}$	Address set up time	0		0		0		ns
$t_{su(A-WH)}$	Address set up time with respect to $\overline{W}$ high	50		60		80		ns
$t_{su(S)}$	Chip select set up time	50		60		80		ns
$t_{su(D)}$	Data set up time	25		30		35		ns
$t_{h(D)}$	Data hold time	0		0		0		ns
$t_{rec(W)}$	Write recovery time	0		0		0		ns
$t_{dis(W)}$	Output disable time from $\overline{W}$ low		20		25		35	ns
$t_{dis(OE)}$	Output disable time from $\overline{OE}$ high		20		25		35	ns
$t_{en(W)}$	Output enable time from $\overline{W}$ high	5		5		5		ns
$t_{en(OE)}$	Output enable time from $\overline{OE}$ low	5		5		5		ns

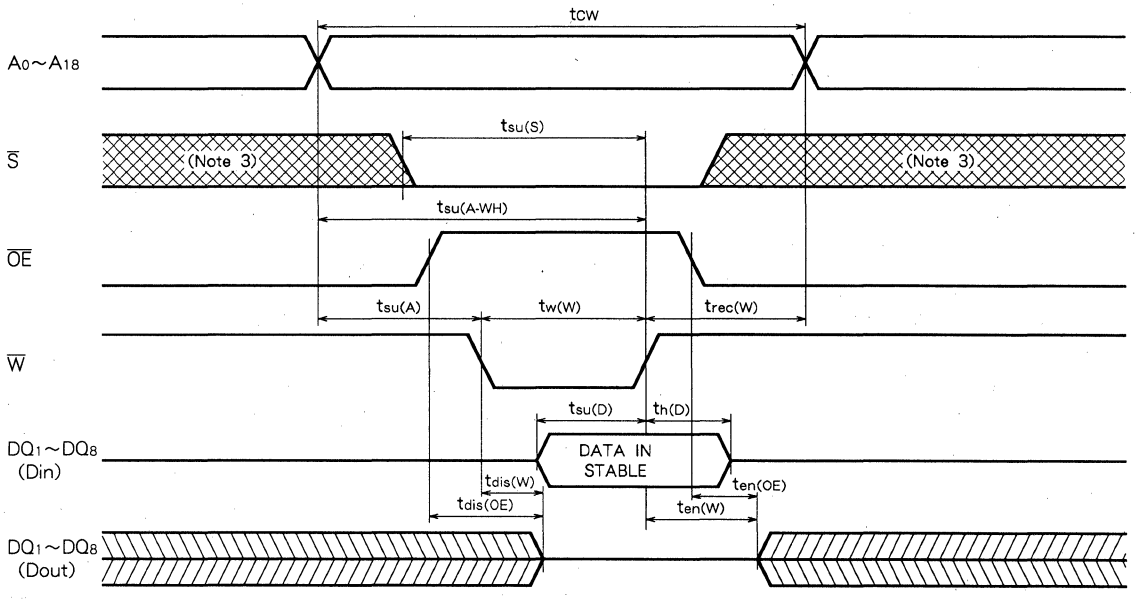
(4) TIMING DIAGRAMS

Read cycle

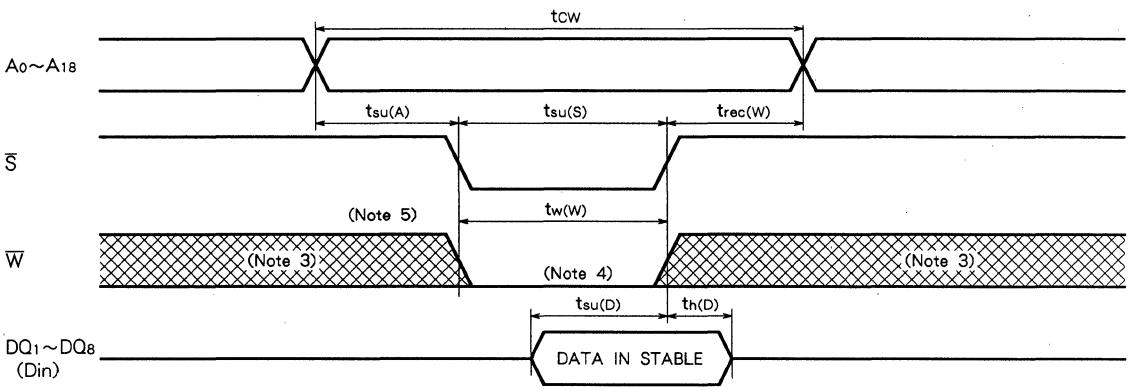


W = "H" level

Write cycle (W control mode)



Write cycle ($\overline{S}$ control mode)



Note 3. Hatching indicates the state is "don't care".
4. A write occurs during the overlap of a low $\overline{S}$ and low $\overline{W}$.
5. If $\overline{W}$ goes low simultaneously with or prior to $\overline{S}$, the output remains in the high impedance state.
6. Don't apply inverted phase signal externally when DQ pin is in output mode.

POWER DOWN CHARACTERISTICS

ELECTRICAL CHARACTERISTICS (T_a = 0~70℃, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ	Max	
$V_{CC(PD)}$	Power down supply voltage			2			V
$V_{I(S)}$	Chip select input $\overline{S}$	2.2 ≦ $V_{CC(PD)}$		2.2			V
		2V ≦ $V_{CC(PD)}$ ≦ 2.2V			$V_{CC(PD)}$		
$I_{CC(PD)}$	Power down supply current	V_{CC} = 3V, $\overline{S}$ ≧ V_{CC} − 0.2V, other inputs = 0~3V	FP,TP, RT-L			50	μA
			FP,TP, RT-LL		0.4	10 *	

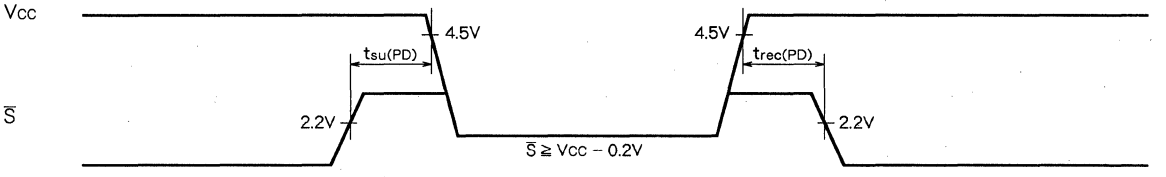
Note 7. When $\overline{S}$ is at 2.2V (V_{IH} min) and the supply voltage is at any level between 4.5V and 2.4V, supply current is defined as I_{CC4}.
* $I_{CC(PD)}$ = 1 μA at T_a = 25℃.

TIMING REQUIREMENTS (T_a = 0~70℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{su(PD)}$	Power down set up time		0			ns
$t_{rec(PD)}$	Power down recovery time		5			ms

POWER DOWN CHARACTERISTICS

$\overline{S}$ control mode



PRELIMINARY

Notice: This is not a final specification
Some parametric limits are subject to change.

M5M5408AFP,TP,RT-55L, -70L,-10L, -55LL,-70LL,-10LL

4194304-BIT (524288-WORD BY 8-BIT) CMOS STATIC RAM

DESCRIPTION

The M5M5408A is a 4194304-bit CMOS Static RAM organized as 524288-word by 8-bit. This device is fabricated using Mitsubishi's high-performance silicon-gate CMOS technology. This state-of-the-art process technology, combined with innovative circuit design techniques, yields high-density and low-power devices. The M5M5408A is suitable for memory applications where high reliability, large storage, simple interfacing and battery back-up are important design objectives.

The M5M5408A is available in 32-pin plastic SOP(M5M5408AFP), 32-pin plastic normal-lead-bend TSOP (M5M5408ATP) and 32-pin plastic reverse-lead-bend TSOP (M5M5408ART) packages. Two types of TSOP's are suitable for Surface Mounting on double-sided printed circuit boards.

FEATURES

Type name	Access time (max.)	Power supply current	
		Active (max.)	Stand-by (max.)
M5M5408AFP,TP,RT-55L M5M5408AFP,TP,RT-70L M5M5408AFP,TP,RT-10L	55ns 70ns 100ns	30mA (1MHz)	100 μA (Vcc=5.5V*)
M5M5408AFP,TP,RT-55LL M5M5408AFP,TP,RT-70LL M5M5408AFP,TP,RT-10LL	55ns 70ns 100ns	30mA (1MHz)	20 μA (Vcc=5.5V*) 0.1 μA (Vcc=3V**)

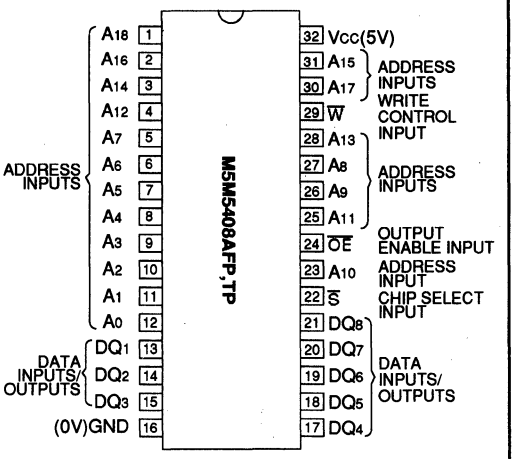
* at 70℃/ **at 25 ℃

- Single +5V power supply
- No clocks, No refresh
- All inputs and outputs are TTL compatible
- Easy memory expansion and power down by $\overline{S}$
- Data retention supply voltage=2.0V to 5.5V
- Three-state outputs: OR-tie capability
- $\overline{OE}$ prevents data contention in the I/O bus
- Common data I/O
- Battery backup capability
- Small stand-by current ..... 0.1 μA(typ)
- Package
  - M5M5408AFP : 32 pin 525 mil SOP
  - M5M5408ATP : 32 pin 400 mil TSOP(II)
  - M5M5408ART : 32 pin 400 mil TSOP(II)

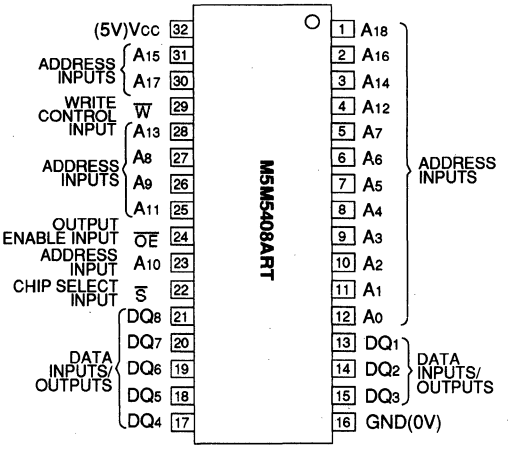
APPLICATION

Small capacity memory units, IC card, Battery operating system

PIN CONFIGURATION (TOP VIEW)



Outline 32P2M-A (FP)
32P3Y-H (TP)



Outline 32P3Y-J

PRELIMINARY

Notice: This is not a final specification.
Some parametric limits are subject to change.

M5M5408AFP,TP,RT-55L, -70L,-10L, -55LL,-70LL,-10LL

4194304-BIT (524288-WORD BY 8-BIT) CMOS STATIC RAM

FUNCTION

The operation mode of the M5M5408A is determined by a combination of the device control inputs $\overline{S}$, $\overline{W}$ and $\overline{OE}$. Each mode is summarized in the function table.

A write cycle is executed whenever the low level $\overline{W}$ overlaps with the low level $\overline{S}$. The address must be set up before the write cycle and must be stable during the entire cycle. The data is latched into a cell on the trailing edge of $\overline{W}$ or $\overline{S}$, whichever occurs first, requiring the set-up and hold time relative to these edge to be maintained. The output enable $\overline{OE}$ directly controls the output stage. Setting the $\overline{OE}$ at a high level, the output stage is in a high-impedance state, and the data bus contention problem in the write cycle is eliminated.

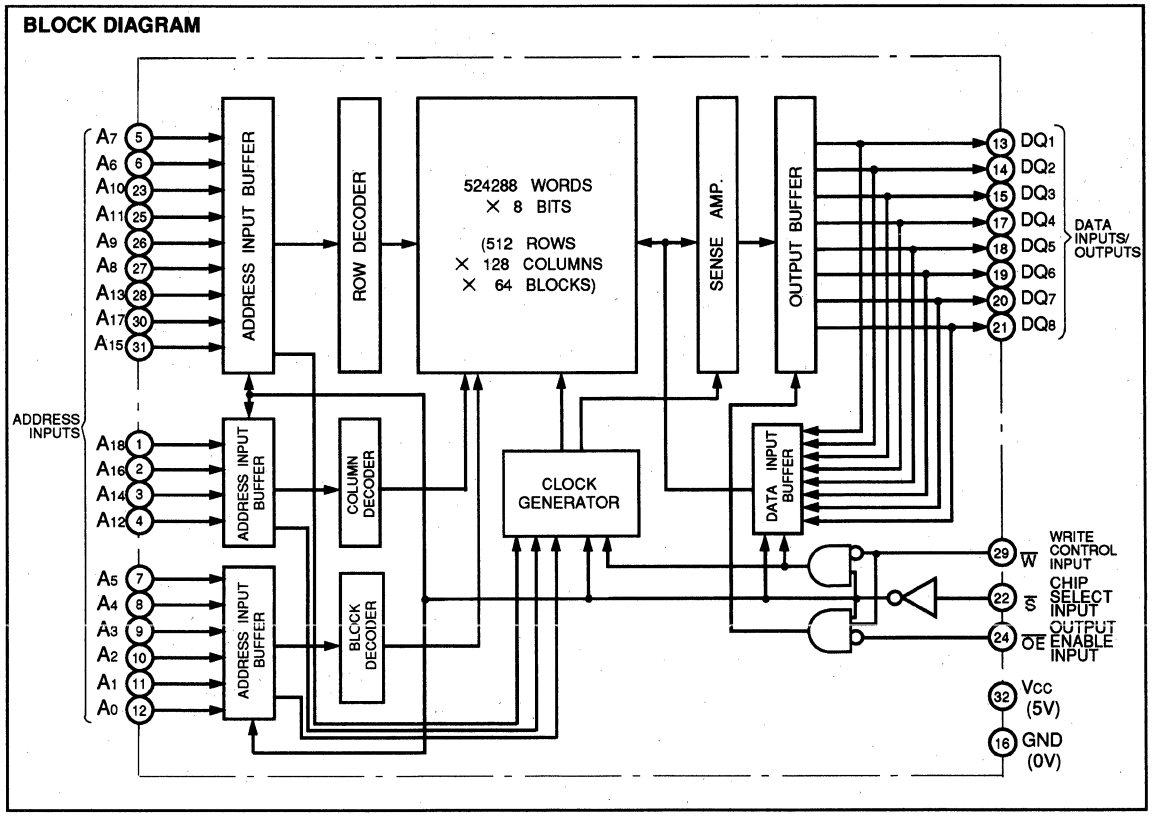
A read cycle is executed by setting $\overline{W}$ at a high level and $\overline{OE}$ at a low level while $\overline{S}$ are in an active state($\overline{S}$=L).

When setting $\overline{S}$ at a high level, the chips are in a non-selectable mode in which both reading and writing are disabled. In this mode, the output stage is in a high-impedance state, allowing OR-tie with other chips and memory expansion by $\overline{S}$. The power supply current is reduced as low as the stand-by current which is specified as I_{CC3} or I_{CC4}, and the memory data can be held at +2V power supply, enabling battery back-up operation during power failure or power-down operation in the non-selected mode.

FUNCTION TABLE

$\overline{S}$	$\overline{W}$	$\overline{OE}$	Mode	DQ	Icc
H	X	X	Non selection	High-impedance	Stand-by
L	L	X	Write	Data input	Active
L	H	L	Read	Data output	Active
L	H	H	Read	High-impedance	Active

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to GND	−0.3～7	V
V_I	Input voltage		−0.3*～V_{CC}+0.3	V
V_O	Output voltage		0～V_{CC}	V
P_d	Power dissipation	Ta = 25℃	700	mW
T_{opr}	Operating temperature		0～70	℃
T_{stg}	Storage temperature		−65～150	℃

* −3.0V in case of AC (Pulse width ≦ 50ns)

DC ELECTRICAL CHARACTERISTICS (Ta = 0～70℃, Vcc = 5V±10%, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits Min.	Limits Typ.	Limits Max.	Unit
V_{IH}	High-level input voltage			2.2		V_{CC}+0.3	V
V_{IL}	Low-level input voltage			−0.3*		0.8	V
V_{OH}	High-level output voltage	I_{OH} = −1mA		2.4			V
		I_{OH} = −0.1mA		V_{CC}−0.5			V
V_{OL}	Low-level output voltage	I_{OL} = 2mA				0.4	V
I_I	Input leakage current	Inputs = 0～V_{CC}				±1	μA
I_O	Output leakage current	$\overline{S}$ = V_{IH} $\overline{OE}$ = V_{IH}, DQ =0 ～V_{CC}				±1	μA
I_{CC1}	Active supply current (AC, MOS-level)	$\overline{S}$≦0.2V Other inputs≦0.2V or ≧V_{CC}−0.2V	Min cycle		50	80	mA
		DQ = open (duty 100%)	1MHz		25	30	
I_{CC2}	Active supply current (AC, TTL-level)	$\overline{S}$ = V_{IL} Other inputs = V_{IH} or V_{IL} DQ = open (duty 100%)	Min cycle		60	90	mA
			1MHz		30	40	
I_{CC3}	Stand-by current	$\overline{S}$ ≧ V_{CC}−0.2V, Other inputs = 0～V_{CC}	-L			100	μA
			-LL		1	20	μA
I_{CC4}	Stand-by current	$\overline{S}$ = V_{IH}, other inputs = 0～V_{CC}				3	mA

* −3.0V in case of AC (Pulse width ≦ 50ns)

CAPACITANCE (Ta = 0～70℃, Vcc=5V±10%, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits Min.	Limits Typ.	Limits Max.	Unit
C_I	Input capacitance	V_I = GND, V_I = 25mV rms, f = 1MHz			6	pF
C_O	Output capacitance	V_O = GND, V_O = 25mV rms, f = 1MHz			8	pF

Note 1. Direction for current flowing into IC is indicated as positive value.
2. Typical value is for Ta=25℃ and Vcc=5.0V
3. C_I and C_O are random samples ,not production tested.

AC ELECTRICAL CHARACTERISTICS (Ta=0~70℃, Vcc=5V±10%, unless otherwise noted)

(1) MEASUREMENT CONDITIONS

Input pulse ····· V_{IH}=2.4V, V_{IL}=0.6V(AFP,TP,RT-70L,-10L,-70LL,-10LL)
V_{IH}=3.0V, V_{IL}=0V(AFP,TP,RT-55L,-55LL)
Input rise and fall time ····· 5ns
Output reference level ····· V_{OH}=V_{OL}=1.5V
For t_{en} and t_{dis}, transition is measured ±500mV from steady state voltage
Output loads ····· Fig. 1; C_L=100pF(AFP,TP,RT-70L,-10L,-70LL,-10LL)
C_L=30pF(AFP,TP,RT-55L,-55LL)
C_L=5pF (for t_{en},t_{dis})

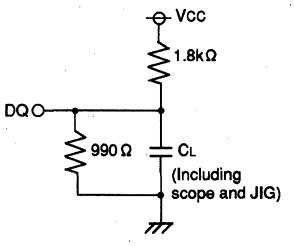


Fig.1 Output load

(2) READ CYCLE

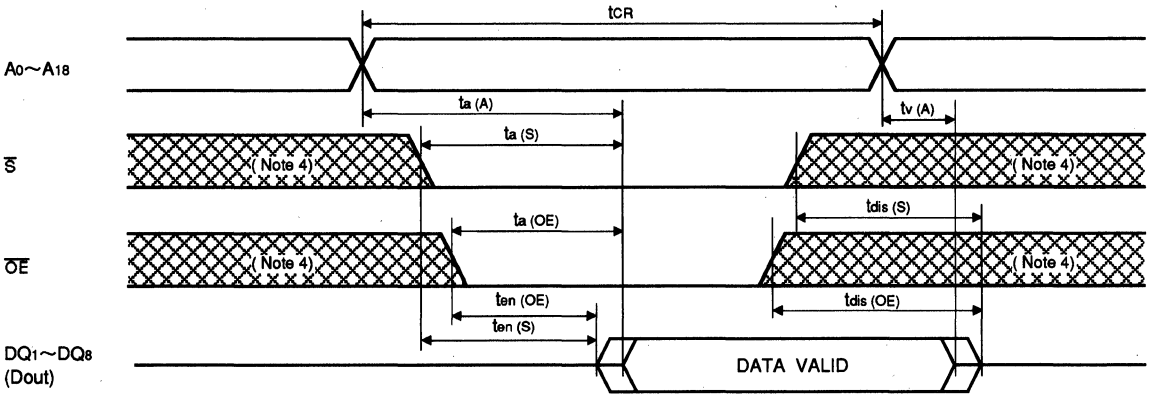
Symbol	Parameter	Limits						Unit
		M5M5408AFP,TP,RT -55L,55LL		M5M5408AFP,TP,RT -70L,70LL		M5M5408AFP,TP,RT -10L,10LL		
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{CR}	Read cycle time	55		70		100		ns
$t_{a(A)}$	Address access time		55		70		70	ns
$t_{a(S)}$	Chip select access time		55		70		70	ns
$t_{a(OE)}$	Output enable access time		25		35		50	ns
$t_{dis(S)}$	Output disable time after $\overline{S}$ high		20		25		35	ns
$t_{dis(OE)}$	Output disable time after $\overline{OE}$ high		20		25		35	ns
$t_{en(S)}$	Output enable time after $\overline{S}$ low	10		10		10		ns
$t_{en(OE)}$	Output enable time after $\overline{OE}$ low	5		5		5		ns
$t_{v(A)}$	Data valid time after address change	10		10		10		ns

(3) WRITE CYCLE

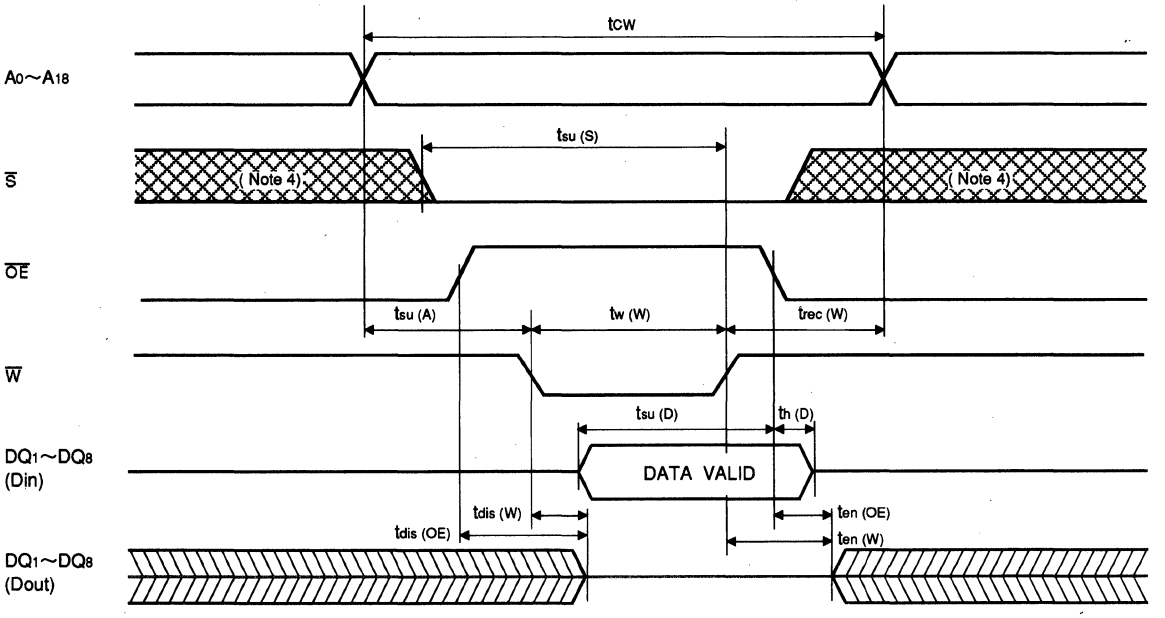
Symbol	Parameter	Limits						Unit
		M5M5408AFP,TP,RT -55L,55LL		M5M5408AFP,TP,RT -70L,70LL		M5M5408AFP,TP,RT -10L,10LL		
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{CW}	Write cycle time	55		70		100		ns
$t_{w(W)}$	Write pulse width	40		50		60		ns
$t_{su(A)}$	Address set up time	0		0		0		ns
$t_{su(A-WH)}$	Address set up time with respect to $\overline{W}$ high	50		60		80		ns
$t_{su(S)}$	Chip select set up time	50		60		80		ns
$t_{su(D)}$	Data set up time	25		30		35		ns
$t_{h(D)}$	Data hold time	0		0		0		ns
$t_{rec(W)}$	Write recovery time	0		0		0		ns
$t_{dis(W)}$	Output disable time after $\overline{W}$ low		20		25		35	ns
$t_{dis(OE)}$	Output disable time after $\overline{OE}$ high		20		25		35	ns
$t_{en(W)}$	Output enable time after $\overline{W}$ high	5		5		5		ns
$t_{en(OE)}$	Output enable time after $\overline{OE}$ low	5		5		5		ns

(4) TIMING DIAGRAMS

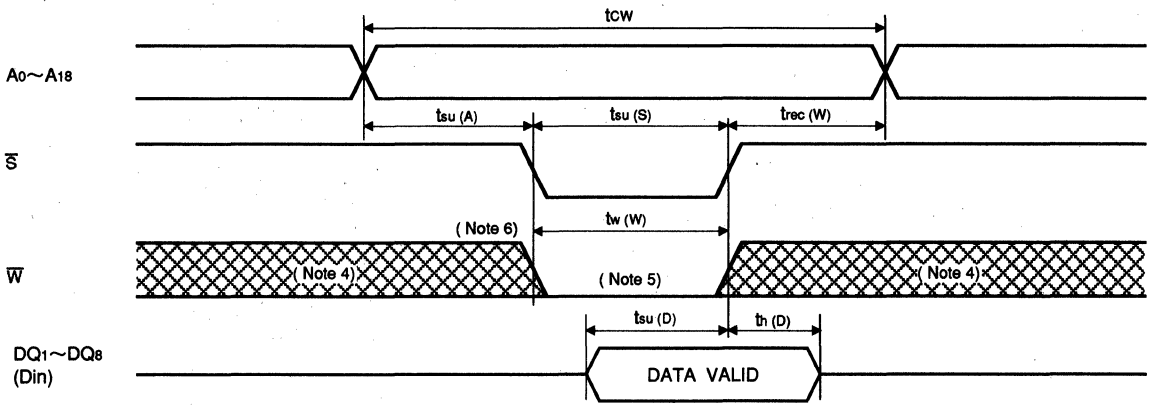
Read cycle



Write cycle ($\overline{WE}$ control mode)



Write cycle ($\overline{S}$ control mode)



Note 4: Hatching indicates the state is "don't care".
5: A Write occurs during the overlap of a low $\overline{S}$ and a low $\overline{W}$.
6: If $\overline{W}$ goes low simultaneously with or prior to $\overline{S}$, the output remains in the high-impedance state.
7: Don't apply inverted phase signal externally when DQ pin is in output mode.

POWER DOWN CHARACTERISTICS
(1) ELECTRICAL CHARACTERISTICS

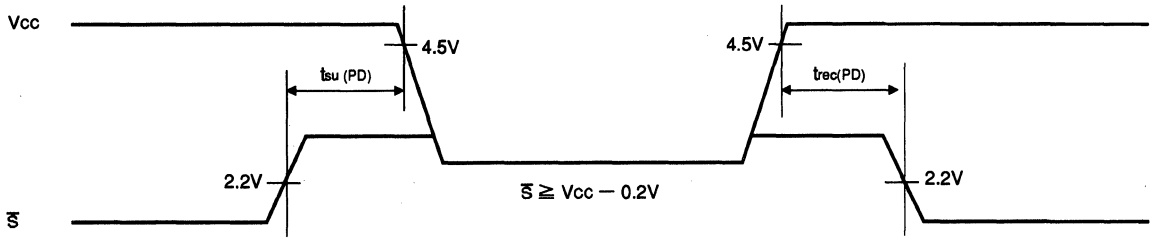
Symbol	Parameter	Test conditions		Limits			Unit
				Min.	Typ.	Max.	
$V_{CC\ (PD)}$	Power down supply voltage			2			V
$V_{I(\overline{S})}$	Chip select input $\overline{S}$	$V_{CC\ (PD)} \geqq 2.2V$		2.2			V
		$2.2V \geqq V_{CC\ (PD)} \geqq 2.0V$			$V_{CC(PD)}$		V
$I_{CC\ (PD)}$	Power down supply current	V_{CC} =3V, $\overline{S} \geqq V_{CC}-0.2V$, other inputs = 0~3V	-L			50	μA
			-LL		0.1	10*	μA

* $I_{CC\ (PD)}$ = 1 μA at Ta=25℃

(2) TIMING REQUIREMENTS (Ta=0~70℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{su(PD)}$	Power down set up time		0			ms
$t_{rec(PD)}$	Power down recovery time		5			ms

(3) TIMING DIAGRAM
$\overline{S}$ control mode



LOW POWER DISSIPATION SRAM

(Low voltage Version)

3

M5M5256CFP,VP,RV-85VLL,-10VLL, -85VXL,-10VXL

262144-BIT(32768-WORD BY 8-BIT)CMOS STATIC RAM

DESCRIPTION

This M5M5256CFP, VP, RV is a 262144-bit CMOS static RAMs organized as 32768-words by 8-bits which is fabricated using high-performance 3 polysilicon CMOS technology. The use of resistive load NMOS cells and CMOS periphery result in a high-density and low-power static RAM. They are low stand-by current and low voltage operation (3.3V) and ideal for the battery operation application.

Especially the M5M5256CVP, RV are packaged in a 28-pin thin small outline package. Two types of devices are available, M5M5256CVP (normal lead bend type package) and M5M5256CRV (reverse lead bend type package). Using both type of devices, it becomes very easy to design a printed circuit board.

FEATURES

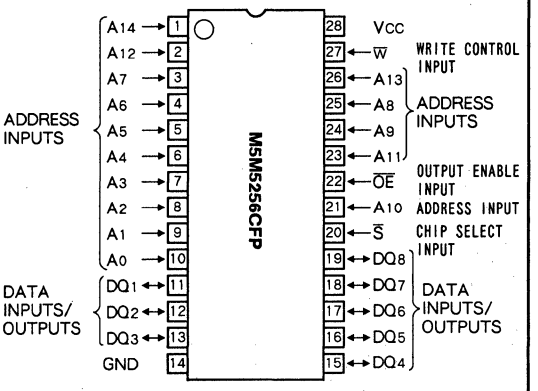
Type name	Access time (max)	Power supply current	
		Active (max)	Stand-by (max)
M5M5256CFP, VP, RV-85VLL	85ns	22mA (V_{CC}=3.6V)	12 μA (V_{CC} = 3.6V)
M5M5256CFP, VP, RV-10VLL	100ns		
M5M5256CFP, VP, RV-85VXL	85ns		2.4 μA (V_{CC} = 3.6V) 0.05 μA (V_{CC} = 3V, typ)
M5M5256CFP, VP, RV-10VXL	100ns		

- Single +3.3 ± 0.3V power supply
- No clocks, no refresh
- Data-hold on +2V power supply
- Directly TTL compatible : All inputs and outputs
- Three-state outputs : OR-tie capability
- Simple memory expansion by $\overline{S}$
- $\overline{OE}$ prevents data contention in the I/O bus
- Common data I/O
- Low stand-by current ····· 0.05 μA (typ)
- Package
  M5M5256CFP ····· 28 pin 450 mil SOP
  M5M5256CVP, RV ····· 28 pin 8 × 13.4mm² TSOP

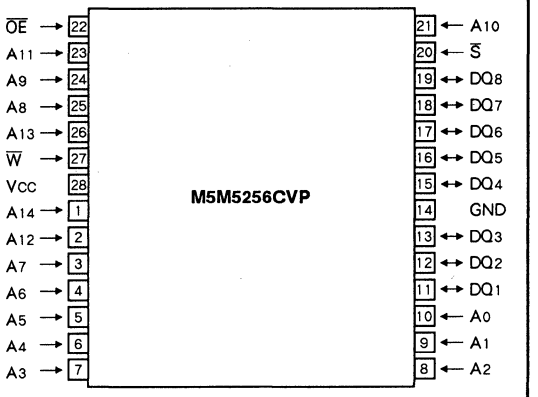
APPLICATION

Small capacity memory units

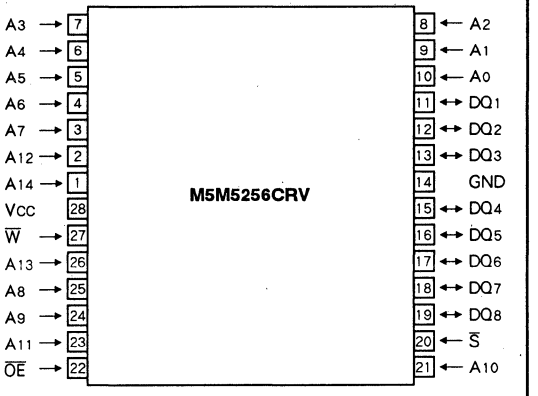
PIN CONFIGURATION (TOP VIEW)



Outline 28P2W-C



Outline 28P2C-A



Outline 28P2C-B

262144-BIT(32768-WORD BY 8-BIT)CMOS STATIC RAM

FUNCTION

The operation mode of the M5M5256CFP, VP, RV is determined by a combination of the device control inputs $\overline{S}$, $\overline{W}$ and $\overline{OE}$. Each mode is summariezed in the function table.

A write cycle is executed whenever the low level $\overline{W}$ overlaps with the low level $\overline{S}$. The address must be set up before the write cycle and must be stable during the entire cycle. The data is latched into a cell on the trailing edge of $\overline{W}$, $\overline{S}$, whichever occurs first, requiring the set-up and hold time relative to these edge to be maintained. The output enable $\overline{OE}$ directly controls the output stage. Setting the $\overline{OE}$ at a high level, the output stage is in a high-impedance state, and the data bus contention problem in the write cycle is eliminated.

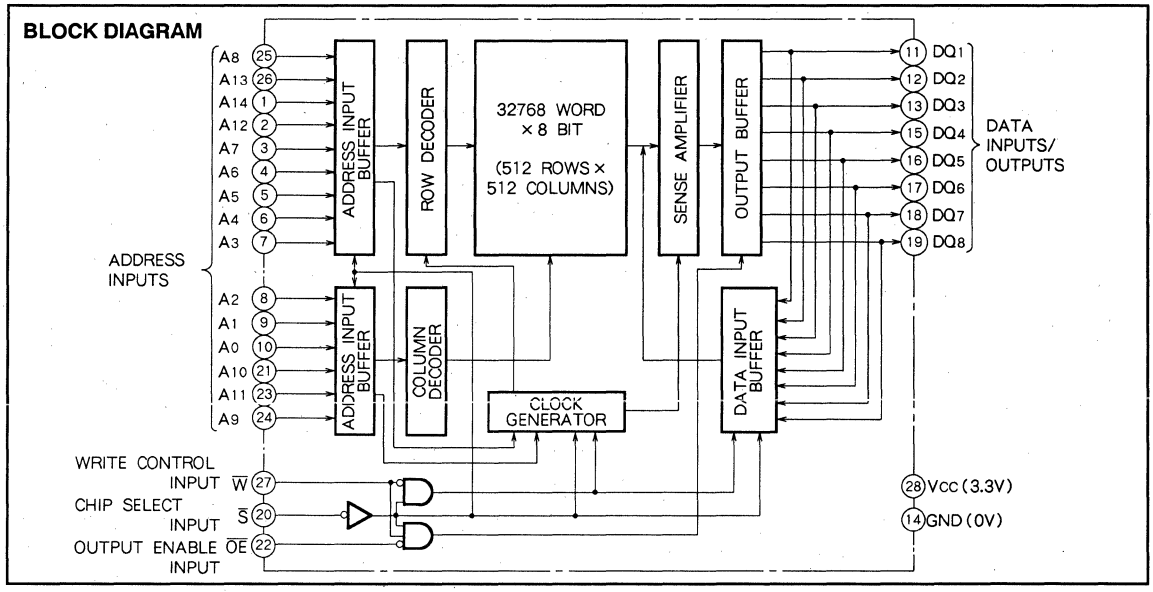
A read cycle is executed by setting $\overline{W}$ at a high level and $\overline{OE}$ at a low level while $\overline{S}$ are in an active state.

When setting $\overline{S}$ at a high level, the chip is in a non-selectable mode in which both reading and writing are disabled. In this mode, the output stage is in a high-impedance state , allowing OR-tie with other chips and memory expansion by $\overline{S}$. The power supply current is reduced as low as the stand-by current which is specified as I_{CC3} or I_{CC4}, and the memory data can be beld +2V power supply, enabling battery back-up operation during power failure or power-down operation in the non-selected mode.

FUNCTION TABLE

$\overline{S}$	$\overline{W}$	$\overline{OE}$	Mode	DQ	Icc
H	X	X	Non selection	High-impedance	Stand-by
L	L	X	Write	D_{in}	Active
L	H	L	Read	D_{out}	Active
L	H	H		High-impedance	Active

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to GND	− 0.3~7	V
V_I	Input voltage		− 0.3*~V_{CC} + 0.3	V
V_O	Output voltage		0~V_{CC}	V
P_d	Power dissipation	Ta = 25℃	700	mW
T_{opr}	Operating temperature		0~70	℃
T_{stg}	Storage temperature		− 65~150	℃

* − 3.0V in case of AC (Pulse width ≦ 30ns)

DC ELECTRICAL CHARACTERISTICS (Ta = 0~70℃, V_{CC} = 3.3 ± 0.3V, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits Min	Limits Typ	Limits Max	Unit
V_{IH}	High-level input voltage			2.0		V_{CC}+0.3	V
V_{IL}	Low-level input voltage			− 0.3*		0.6	V
V_{OH1}	High-level output voltage 1	I_{OH} = − 0.5mA		2.4			V
V_{OH2}	High-level output voltage 2	I_{OH} = − 0.05mA		V_{CC}-0.5			V
V_{OL}	Low-level output voltage	I_{OL} = 1mA				0.4	V
I_I	Input leakage current	V_I = 0~V_{CC}				± 1	μA
I_O	Output leakage current	$\overline{S}$ = V_{IH} or $\overline{OE}$ = V_{IH}, $V_{I/O}$ = 0~V_{CC}				± 1	μA
I_{CC1}	Active supply current (AC, MOS level)	$\overline{S}$ ≦ 0.2V, Other inputs ≦ 0.2V or ≧ V_{CC} − 0.2V Output open	Min.cycle		10	22	mA
			1MHz		1.5	3.3	
I_{CC2}	Active supply current (AC, TTL level)	$\overline{S}$ = V_{IL}, Other inputs = V_{IL} or V_{IH} Output open	Min.cycle		10	22	mA
			1MHz		1.5	3.3	
I_{CC3}	Stand-by supply current	$\overline{S}$ ≧ V_{CC} − 0.2V, Other inputs = 0~V_{CC}	-VLL			12	μA
			-VXL		0.05	2.4	
I_{CC4}	Stand-by supply current	$\overline{S}$ = V_{IH}, Other inputs = 0~V_{CC}				0.33	mA

* − 3.0V in case of AC (Pulse width ≦ 30ns)

CAPACITANCE (Ta = 0~70℃, V_{CC} = 3.3 ± 0.3V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits Min	Limits Typ	Limits Max	Unit
C_I	Input capacitance (Ta = 25℃)	V_I = GND, V_I = 25mVrms, f = 1MHz			6	pF
C_O	Output capacitance (Ta = 25℃)	V_O = GND, V_O = 25mVrms, f = 1MHz			8	pF

Note 1. Direction for current flowing into IC is indicated as positive. (no mark)
2. Typical value is V_{CC} = 3.3V, Ta = 25℃.
3. C_I, C_O are periodically sampled and are not 100% tested.

AC ELECTRICAL CHARACTERISTICS (T_a = 0~70℃, V_{CC} = 3.3 ± 0.3V, unless otherwise noted)

(1) MEASUREMENT CONDITIONS

Input pulse level ·····V_{IH} = 2.2V, V_{IL} = 0.4V
Input rise and fall time·····5ns
Reference level ·····V_{OH} = V_{OL} = 1.5V
Transition is measured ± 500mV from steady state voltage.(for t_{en}, t_{dis})
Output loads ·····Fig.1, C_L = 50pF
C_L = 5pF (for t_{en}, t_{dis})

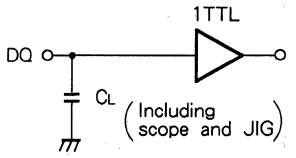


Fig.1 Output load

(2) READ CYCLE

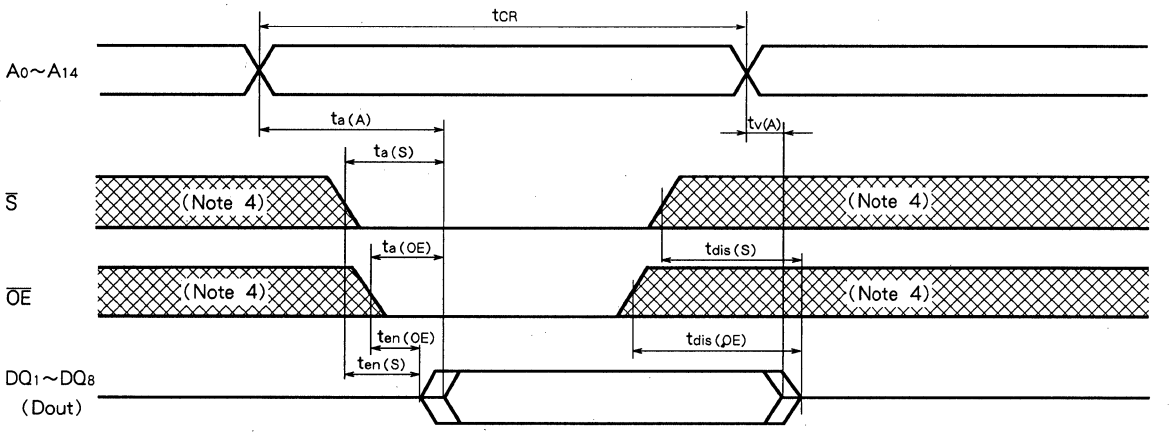
Symbol	Parameter	Limits						Unit
		M5M5256C-85VLL M5M5256C-85VXL			M5M5256C-10VLL M5M5256C-10VXL			
		Min	Typ	Max	Min	Typ	Max	
t_{CR}	Read cycle time	85			100			ns
$t_{a(A)}$	Address access time			85			100	ns
$t_{a(S)}$	Chip select access time			85			100	ns
$t_{a(OE)}$	Output enable access time			45			50	ns
$t_{dis(S)}$	Output disable time after $\overline{S}$ high			25			30	ns
$t_{dis(OE)}$	Output disable time after $\overline{OE}$ high			25			30	ns
$t_{en(S)}$	Output enable time after $\overline{S}$ low	10			10			ns
$t_{en(OE)}$	Output enable time after $\overline{OE}$ low	10			10			ns
$t_{v(A)}$	Data valid time after address	10			10			ns

(3) WRITE CYCLE

Symbol	Parameter	Limits						Unit
		M5M5256C-85VLL M5M5256C-85VXL			M5M5256C-10VLL M5M5256C-10VXL			
		Min	Typ	Max	Min	Typ	Max	
t_{CW}	Write cycle time	85			100			ns
$t_{w(W)}$	Write pulse width	60			70			ns
$t_{su(A)}$	Address set up time	0			0			ns
$t_{su(A-WH)}$	Address set up time with respect to $\overline{W}$ high	70			80			ns
$t_{su(S)}$	Chip select set up time	70			80			ns
$t_{su(D)}$	Data set up time	35			40			ns
$t_{h(D)}$	Data hold time	0			0			ns
$t_{rec(W)}$	Write recovery time	0			0			ns
$t_{dis(W)}$	Output disable time after $\overline{W}$ low			25			30	ns
$t_{dis(OE)}$	Output disable time after $\overline{OE}$ high			25			30	ns
$t_{en(W)}$	Output enable time after $\overline{W}$ high	10			10			ns
$t_{en(OE)}$	Output enable time after $\overline{OE}$ low	10			10			ns

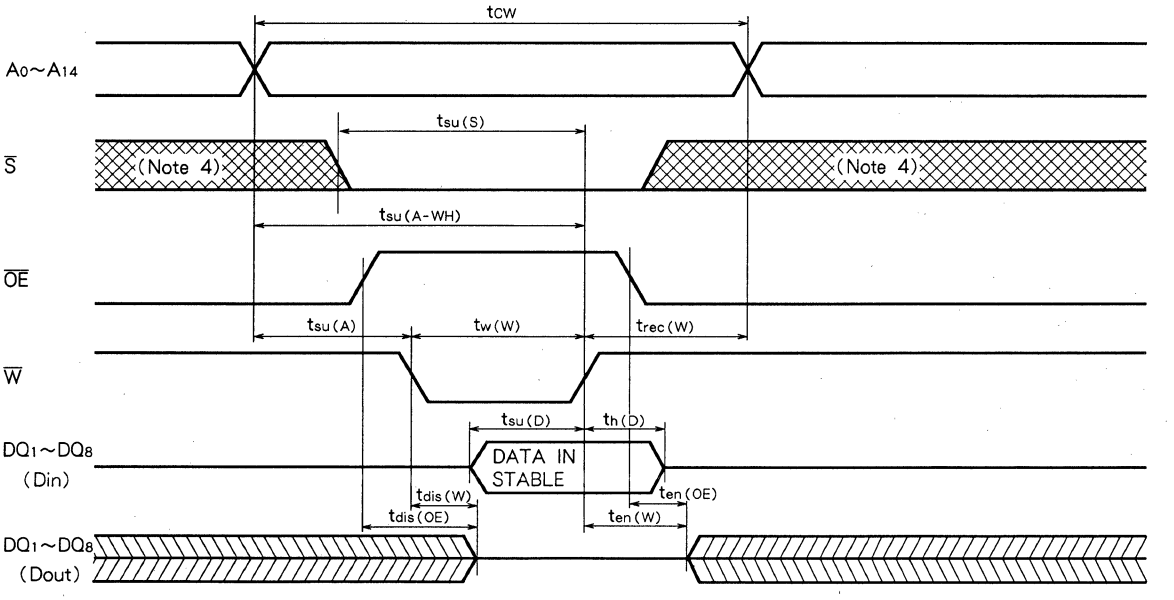
(4) TIMING DIAGRAMS

Read cycle

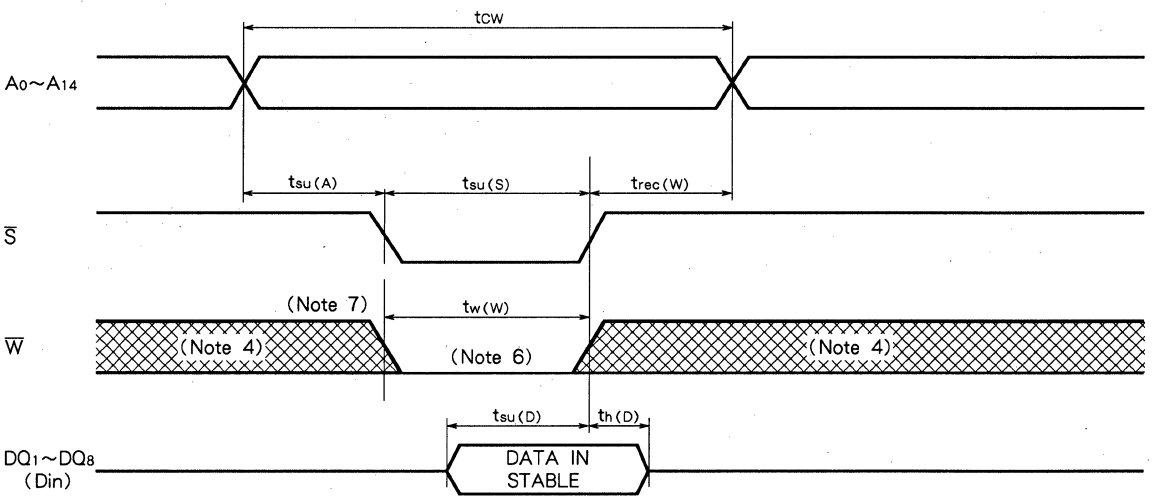


W = "H"level

Write cycle (W control mode)



Write cycle ($\overline{S}$ control mode)



Note 4. Hatching indicates the state is don't care.
5. Writing is executed in overlap of $\overline{S}$ and $\overline{W}$ low.
6. If $\overline{W}$ goes low simultaneously with or prior to $\overline{S}$, the output remains in the high-impedance state.
7. Don't apply inverted phase signal externally when DQ pin is in output mode.
8. t_{en}, t_{dis} are periodically sampled and are not 100% tested.

POWER DOWN CHARACTERISTICS

(1) ELECTRICAL CHARACTERISTICS (Ta = 0~70℃, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ	Max	
$V_{CC(PD)}$	Power down supply voltage			2			V
$V_{I(\overline{S})}$	Chip select input $\overline{S}$			2			V
$I_{CC(PD)}$	Power down supply current	V_{CC} = 3V, Other inputs = 3V	-VLL			10*	μA
			-VXL		0.05	2**	μA

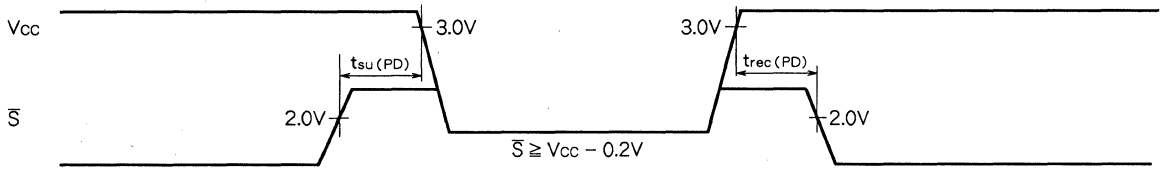
* Ta = 25℃, $I_{CC(PD)}$ = 1 μA
** Ta = 25℃, $I_{CC(PD)}$ = 0.2 μA

(2) TIMING REQUIREMENTS (Ta = 0~70℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{su(PD)}$	Power down set up time		0			ns
$t_{rec(PD)}$	Power down recovery time		t_{CR}			ns

(3) POWER DOWN CHARACTERISTICS

$\overline{S}$ control mode



M5M5256CFP,VP,RV-12VLL,-15VLL, -12VXL,-15VXL

262144-BIT(32768-WORD BY 8-BIT)CMOS STATIC RAM

DESCRIPTION

This M5M5256CFP, VP, RV is a 262144-bit CMOS static RAMs organized as 32768-words by 8-bits which is fabricated using high-performance 3 polysilicon CMOS technology. The use of resistive load NMOS cells and CMOS periphery result in a high-density and low-power static RAM. They are low stand-by current and low voltage operation (3V) and ideal for the battery operation application.

Especially the M5M5256CVP, RV are packaged in a 28-pin thin small outline package. Two types of devices are available, M5M5256CVP (normal lead bend type package) and M5M5256CRV (reverse lead bend type package). Using both type of devices, it becomes very easy to design a printed circuit board.

FEATURES

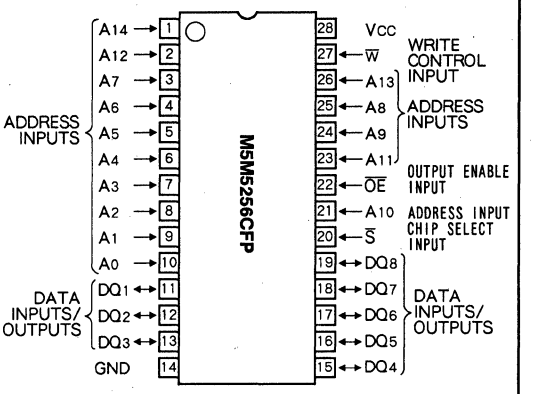
Type name	Access time (max)	Power supply current	
		Active (max)	Stand-by (max)
M5M5256CFP, VP, RV-12VLL M5M5256CFP, VP, RV-15VLL	120ns 150ns	50mA (Vcc=5.5V)	11 μA (Vcc = 3.3V)
M5M5256CFP, VP, RV-12VXL M5M5256CFP, VP, RV-15VXL	120ns 150ns	20mA (Vcc=3.3V)	2.2 μA (Vcc = 3.3V) 0.05 μA (Vcc = 3V, typ)

- Single +2.7~5.5V power supply
- No clocks, no refresh
- Data-hold on +2V power supply
- Directly TTL compatible : All inputs and outputs
- Three-state outputs : OR-tie capability
- Simple memory expansion by $\overline{S}$
- $\overline{OE}$ prevents data contention in the I/O bus
- Common data I/O
- Low stand-by current ..... 0.05 μA (typ)
- Package
  - M5M5256CFP ..... 28 pin 450 mil SOP
  - M5M5256CVP, RV ..... 28pin 8 × 13.4mm² TSOP

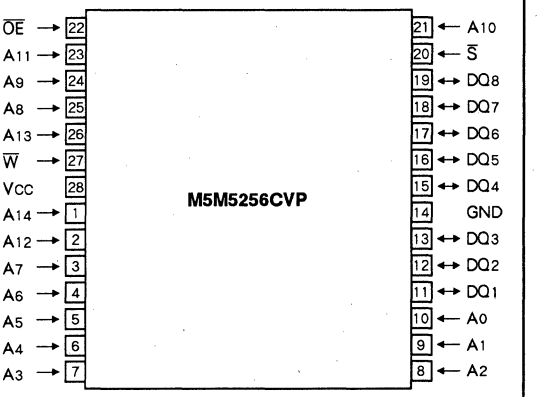
APPLICATION

Small capacity memory units

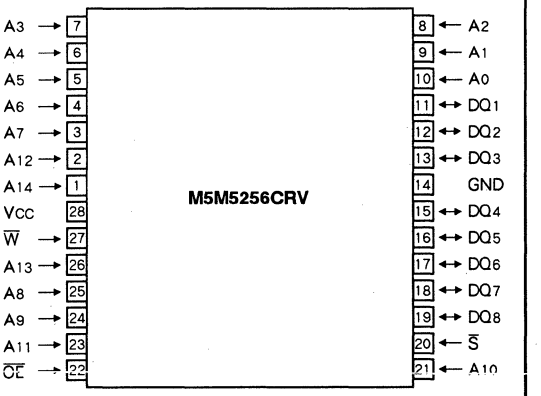
PIN CONFIGURATION (TOP VIEW)



Outline 28P2W-C



Outline 28P2C-A



Outline 28P2C-B

MITSUBISHI ELECTRIC

262144-BIT(32768-WORD BY 8-BIT)CMOS STATIC RAM

FUNCTION

The operation mode of the M5M5256CFP, VP, RV is determined by a combination of the device control inputs $\overline{S}$, $\overline{W}$ and $\overline{OE}$. Each mode is summariezed in the function table.

A write cycle is executed whenever the low level $\overline{W}$ overlaps with the low level $\overline{S}$. The address must be set-up before the write cycle and must be stable during the entire cycle. The data is latched into a cell on the trailing edge of $\overline{W}$, $\overline{S}$, whichever occurs first, requiring the set-up and hold time relative to these edge to be maintained. The output enable $\overline{OE}$ directly controls the output stage. Setting the $\overline{OE}$ at a high level, the output stage is in a high-impedance state, and the data bus contention problem in the write cycle is eliminated.

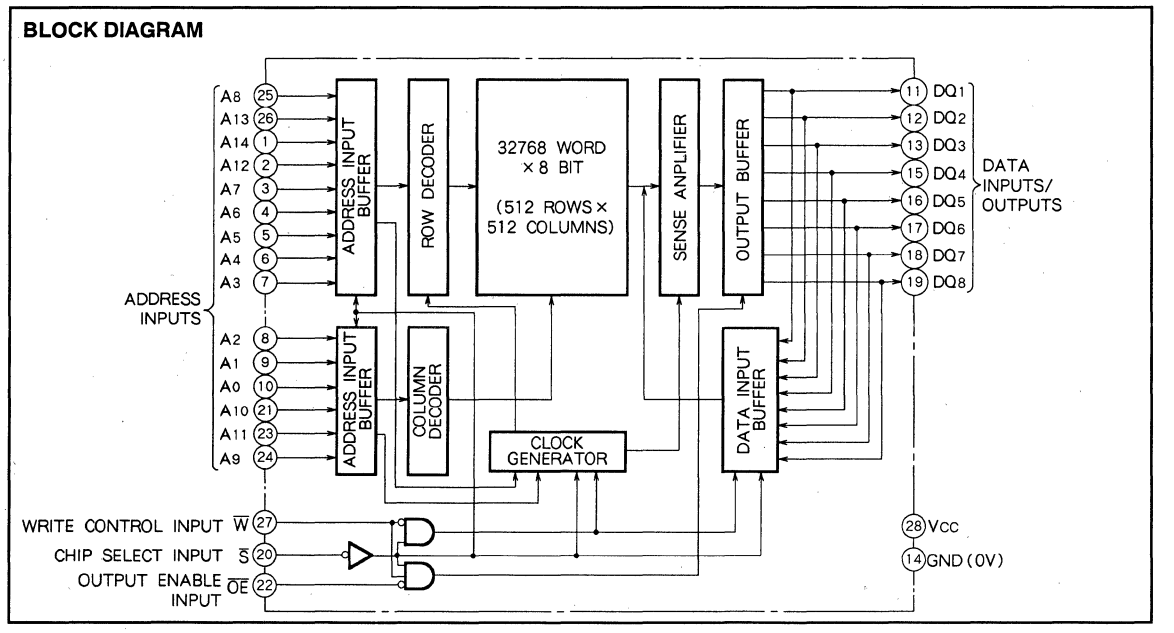
A read cycle is executed by setting $\overline{W}$ at a high level and $\overline{OE}$ at a low level while $\overline{S}$ are in an active state.

When setting $\overline{S}$ at a high level, the chip is in a non-selectable mode in which both reading and writing are disabled. In this mode, the output stage is in a high-impedance state, allowing OR-tie with other chips and memory expansion by $\overline{S}$. The power supply current is reduced as low as the stand-by current which is specified as I_{CC3} or I_{CC4}, and the memory data can be held +2V power supply, enabling battery back-up operation during power failure or power-down operation in the non-selected mode.

FUNCTION TABLE

$\overline{S}$	$\overline{W}$	$\overline{OE}$	Mode	DQ	Icc
H	X	X	Non selection	High-impedance	Stand-by
L	L	X	Write	D_{in}	Active
L	H	L	Read	D_{out}	Active
L	H	H		High-impedance	Active

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to GND	− 0.3~7	V
V_I	Input voltage		− 0.3*~V_{CC} + 0.3	V
V_O	Output voltage		0~V_{CC}	V
P_d	Power dissipation	Ta = 25℃	700	mW
T_{opr}	Operating temperature		0~70	℃
T_{stg}	Storage temperature		− 65~150	℃

* − 3.0V in case of AC (Pulse width ≧ 30ns)

DC ELECTRICAL CHARACTERISTICS (Ta = 0~70℃, V_{CC} = 2.7~5.5V, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits 1 (V_{CC} = 5V ± 10%) Min	Typ	Max	Limits 2 (V_{CC} = 3V ± 10%) Min	Typ	Max	Unit
V_{IH}	High-level input voltage			2.2		V_{CC}+0.3	2.0		V_{CC}+0.3	V
V_{IL}	Low-level input voltage			− 0.3*		0.8	− 0.3*		0.6	V
V_{OH1}	High-level output voltage 1	I_{OH} = − 1mA (V_{CC} = 5V ± 10%) I_{OH} = − 0.5mA (V_{CC} = 3V ± 10%)		2.4			2.4			V
V_{OH2}	High-level output voltage 2	I_{OH} = − 0.1mA (V_{CC} = 5V ± 10%) I_{OH} = − 0.05mA (V_{CC} = 3V ± 10%)		V_{CC}−0.5			V_{CC}−0.5			V
V_{OL}	Low-level output voltage	I_{OL} = 2mA (V_{CC} = 5V ± 10%) I_{OL} = 1mA (V_{CC} = 3V ± 10%)				0.4			0.4	V
I_I	Input leakage current	V_I = 0~V_{CC}				± 1			± 1	μA
I_O	Output leakage current	$\overline{S}$ = V_{IH} or $\overline{OE}$ = V_{IH}, $V_{I/O}$ = 0~V_{CC}				± 1			± 1	μA
I_{CC1}	Active supply current (AC, MOS level)	$\overline{S}$ ≦ 0.2V Other inputs ≦ 0.2V or ≧ V_{CC} − 0.2V Output open	Min. cycle		30	45		10	20	mA
			1MHz		4	8		1.5	3	
I_{CC2}	Active supply current (AC, TTL level)	$\overline{S}$ = V_{IL}, Other inputs = V_{IL} or V_{IH} Output open	Min. cycle		35	50		10	20	mA
			1MHz		5	10		1.5	3	
I_{CC3}	Stand-by supply current	$\overline{S}$ ≧ V_{CC} − 0.2V, Other inputs = 0~V_{CC}	-VLL			20			11	μA
			-VXL		0.1	5		0.05	2.2	
I_{CC4}	Stand-by supply current	$\overline{S}$ = V_{IH}, Other inputs = 0~V_{CC}				3			0.3	mA

* − 3.0V in case of AC (Pulse width ≦ 30ns)

CAPACITANCE (Ta = 0~70℃, V_{CC} = 2.7~5.5V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits Min	Typ	Max	Unit
C_I	Input capacitance	V_I = GND, V_I = 25mV_{rms}, f = 1MHz			6	pF
C_O	Output capacitance	V_O = GND, V_O = 25mV_{rms}, f = 1MHz			8	pF

Note 1. Direction for current flowing into IC is indicated as positive. (no mark)
2. Typical value is V_{CC} = 5V or 3V, Ta = 25℃.
3. C_I, C_O are periodically sampled and are not 100% tested.

AC ELECTRICAL CHARACTERISTICS (T_a = 0~70℃, V_{CC} = 2.7~5.5V, unless otherwise noted)

(1) MEASUREMENT CONDITIONS

Input pulse level ·····V_{IH} = 2.4V, V_{IL} = 0.6V (V_{CC} = 5V ± 10%)
V_{IH} = 2.2V, V_{IL} = 0.4V (V_{CC} = 3V ± 10%)
Input rise and fall time ·····5ns
Reference level ·····V_{OH} = V_{OL} = 1.5V
Transition is measured ±500mV from steady state voltage.(for t_{en}, t_{dis})
Output loads ·····Fig.1, C_L = 100pF (FP, VP, RV-15VLL, -15VXL)
C_L = 50pF (FP, VP, RV-12VLL, -12VXL)
C_L = 5pF (for t_{en}, t_{dis})

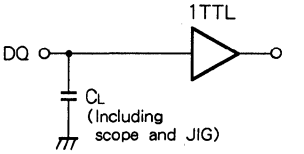


Fig.1 Output load

(2) READ CYCLE

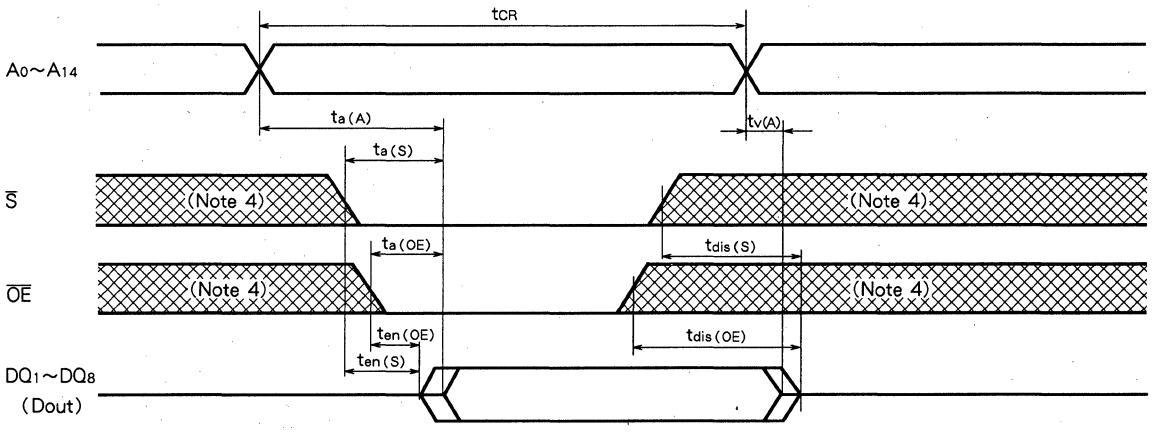
Symbol	Parameter	Limits						Unit
		M5M5256C-12VLL M5M5256C-12VXL			M5M5256C-15VLL M5M5256C-15VXL			
		Min	Typ	Max	Min	Typ	Max	
t_{CR}	Read cycle time	120			150			ns
$t_{a(A)}$	Address access time			120			150	ns
$t_{a(S)}$	Chip select access time			120			150	ns
$t_{a(OE)}$	Output enable access time			60			75	ns
$t_{dis(S)}$	Output disable time after $\overline{S}$ high			35			40	ns
$t_{dis(OE)}$	Output disable time after $\overline{OE}$ high			35			40	ns
$t_{en(S)}$	Output enable time after $\overline{S}$ low	10			10			ns
$t_{en(OE)}$	Output enable time after $\overline{OE}$ low	10			10			ns
$t_{v(A)}$	Data valid time after address	10			10			ns

(3) WRITE CYCLE

Symbol	Parameter	Limits						Unit
		M5M5256C-12VLL M5M5256C-12VXL			M5M5256C-15VLL M5M5256C-15VXL			
		Min	Typ	Max	Min	Typ	Max	
t_{CW}	Write cycle time	120			150			ns
$t_{w(W)}$	Write pulse width	80			90			ns
$t_{su(A)}$	Address set up time	0			0			ns
$t_{su(A-WH)}$	Address set up time with respect to $\overline{W}$ high	90			100			ns
$t_{su(S)}$	Chip select set up time	90			100			ns
$t_{su(D)}$	Data set up time	45			50			ns
$t_{h(D)}$	Data hold time	0			0			ns
$t_{rec(W)}$	Write recovery time	0			0			ns
$t_{dis(W)}$	Output disable time after $\overline{W}$ low			35			40	ns
$t_{dis(OE)}$	Output disable time after $\overline{OE}$ high			35			40	ns
$t_{en(W)}$	Output enable time after $\overline{W}$ high	10			10			ns
$t_{en(OE)}$	Output enable time after $\overline{OE}$ low	10			10			ns

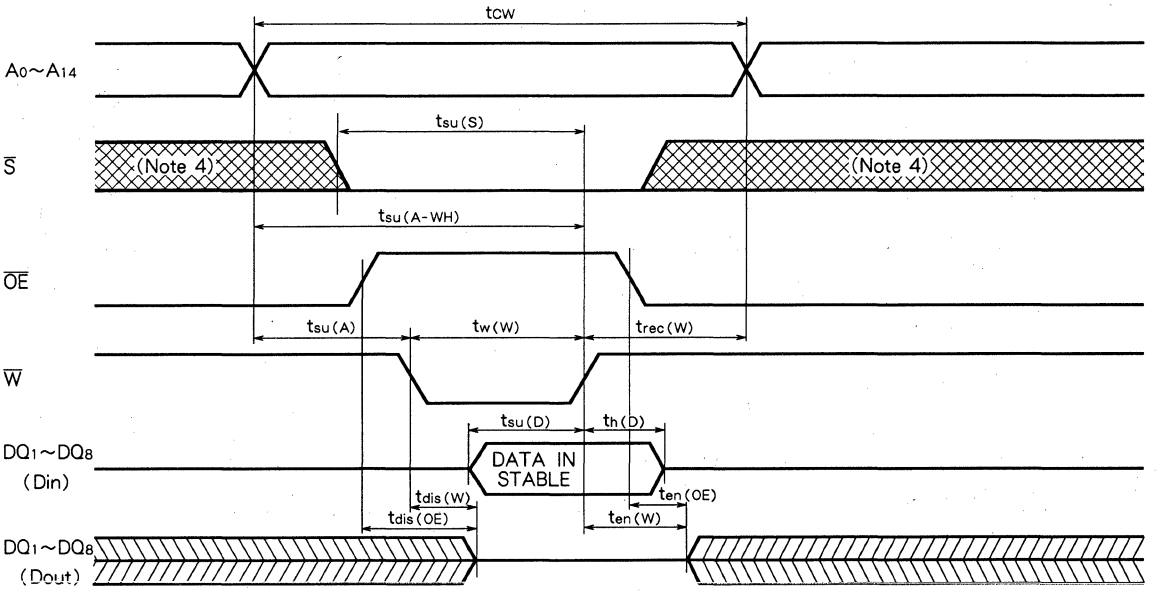
(4) TIMING DIAGRAMS

Read cycle

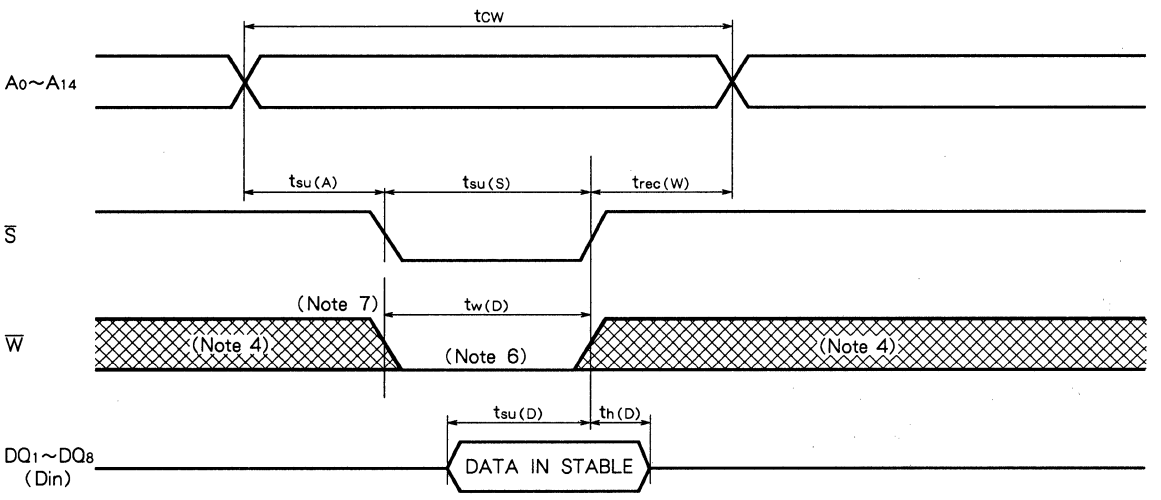


W = "H"level

Write cycle (W control mode)



Write cycle ($\overline{S}$ control mode)



Note 4. Hatching indicates the state is don't care.
5. Writing is executed in overlap of $\overline{S}$ and $\overline{W}$ low.
6. If $\overline{W}$ goes low simultaneously with or prior to $\overline{S}$, the output remains in the high-impedance state.
7. Don't apply inverted phase signal externally when DQ pin is in output mode.
8. t_{en}, t_{dis} are periodically sampled and are not 100% tested.

POWER DOWN CHARACTERISTICS

(1) ELECTRICAL CHARACTERISTICS (Ta = 0~70℃, unless otherwise noted)

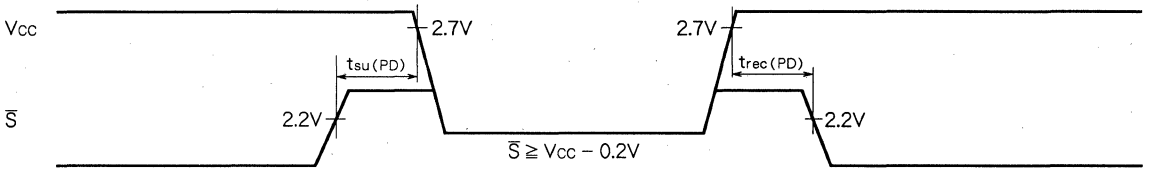
Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ	Max	
$V_{CC(PD)}$	Power down supply voltage			2			V
$V_{I(\overline{S})}$	Chip select input $\overline{S}$	2.2V ≦ $V_{CC(PD)}$		2.2			V
		2V ≦ $V_{CC(PD)}$ ≦ 2.2V			$V_{CC(PD)}$		
$I_{CC(PD)}$	Power down supply current	V_{CC} = 3V, Other inputs = 3V	-VLL			10*	μA
			-VXL		0.05	2**	

* Ta = 25℃, $I_{CC(PD)}$ = 1 μA
** Ta = 25℃, $I_{CC(PD)}$ = 0.2 μA

(2) TIMING REQUIREMENTS (Ta = 0~70℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{su(PD)}$	Power down set up time		0			ns
$t_{rec(PD)}$	Power down recovery time		t_{CR}			ns

(3) POWER DOWN CHARACTERISTICS
$\overline{S}$ control mode



M5M51008AFP,VP,RV-85VL,-10VL, -85VLL,-10VLL

1048576-BIT(131072-WORD BY 8-BIT)CMOS STATIC RAM

DESCRIPTION

The M5M51008AFP, VP, RV are a 1048576-bit CMOS static RAM organized as 131072 word by 8-bit which are fabricated using high-performance triple polysilicon CMOS technology. The use of resistive load NMOS cells and CMOS periphery result in a high density and low power static RAM.

They are low stand-by current and low operation current and ideal for the battery back-up application.

The M5M51008AVP, RV are packaged in a 32-pin thin small outline package which is a high reliability and high density surface mount device (SMD). Two types of devices are available. M5M51008AVP (normal lead bend type package), M5M51008ARV (reverse lead bend type package). Using both types of devices, it becames very easy to design a printed circuit board.

FEATURES

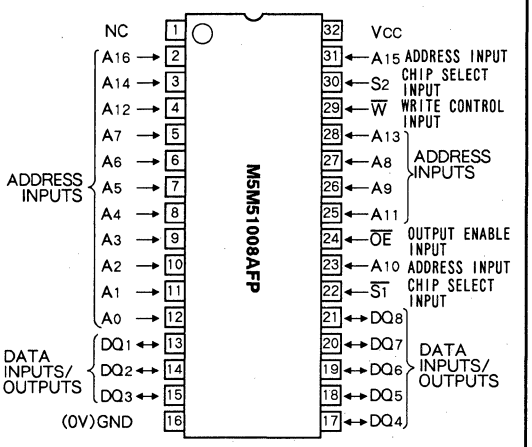
Type name	Access time (max)	Power supply current	
		Active (max)	Stand-by (max)
M5M51008AFP, VP, RV-85VL M5M51008AFP, VP, RV-10VL	85ns 100ns	20mA (1MHz)	60 μA (Vcc = 3.6V)
M5M51008AFP, VP, RV-85VLL M5M51008AFP, VP, RV-10VLL	85ns 100ns		12 μA (Vcc = 3.6V) 0.3 μA (Vcc=3.0V, typ)

- Single +3.3V power supply
- Low stand-by current 0.3 μA (typ.)
- Directly TTL compatible : All inputs and outputs
- Easy memory expansion and power down by $\overline{S1}$, S2
- Data hold on +2V power supply
- Three-state outputs : OR-tie capability
- $\overline{OE}$ prevents data contention in the I/O bus
- Common data I/O
- Package
  M5M51008AFP ····· 32pin 525 mil SOP
  M5M51008AVP, RV ····· 32pin 8 × 20mm² TSOP

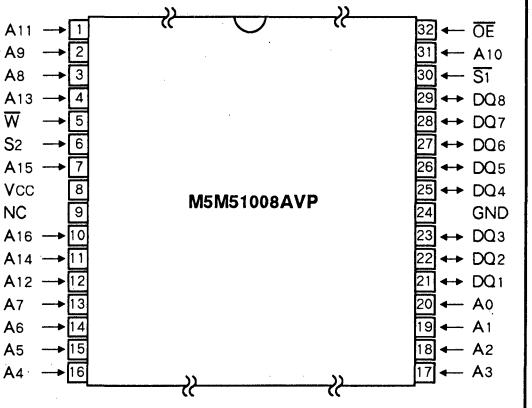
APPLICATION

Small capacity memory units

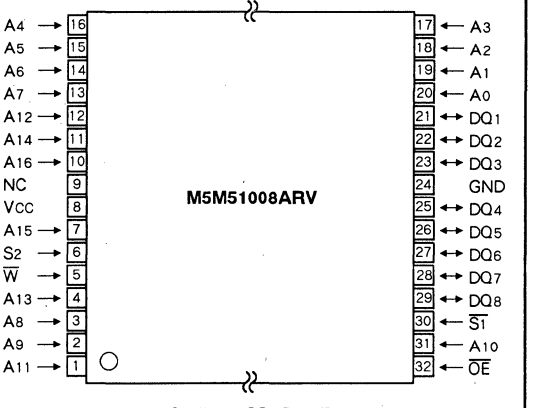
PIN CONFIGURATION (TOP VIEW)



Outline 32P2M-A



Outline 32P3H-E



Outline 32P3H-F

NC : NO CONNECTION

M5M51008AFP, VP, RV-85VL, -85VLL : Under development

1048576-BIT(131072-WORD BY 8-BIT)CMOS STATIC RAM

FUNCTION

The operation mode of the M5M51008A series are determined by a combination of the device control inputs $\overline{S_1}$, S_2, $\overline{W}$ and $\overline{OE}$. Each mode is summarized in the function table.

A write cycle is executed whenever the low level $\overline{W}$ overlaps with the low level $\overline{S_1}$ and the high level S_2. The address must be set-up before the write cycle and must be stable during the entire cycle. The data is latched into a cell on the trailing edge of $\overline{W}$, $\overline{S_1}$ or S_2, whichever occurs first, requiring the set-up and hold time relative to these edge to be maintained. The output enable input $\overline{OE}$ directly controls the output state. Setting the $\overline{OE}$ at a high level, the output stage is in a high-impedance state, and the data bus contention problem in the write cycle is eliminated.

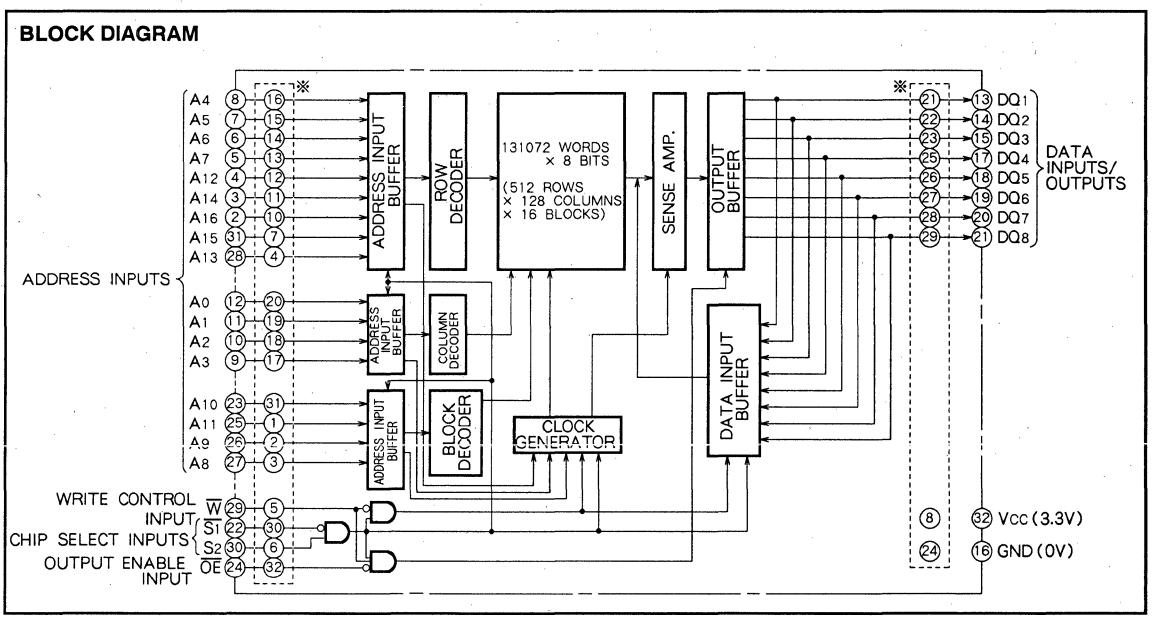
A read cycle is executed by setting $\overline{W}$ at a high level and $\overline{OE}$ at a low level while $\overline{S_1}$ and S_2 are in an active state ($\overline{S_1}$ = L, S_2 = H)

When setting $\overline{S_1}$ at a high level or S_2 at a low level, the chip are in a non-selectable mode in which both reading and writing are disabled. In this mode, the output stage is in a high-impedance state, allowing OR-tie with other chips and memory expansion by $\overline{S_1}$ and S_2. The power supply current is reduced as low as the stand-by current which is specified as I_{CC3} or I_{CC4}, and the memory data can be held at +2V power supply, enabling battery back-up operation during power failure or power-down operation in the non-selected mode.

FUNCTION TABLE

$\overline{S_1}$	S_2	$\overline{W}$	$\overline{OE}$	Mode	DQ	Icc
X	L	X	X	Non selection	High-impedance	Stand-by
H	X	X	X	Non selection	High-impedance	Stand-by
L	H	L	X	Write	D_{in}	Active
L	H	H	L	Read	D_{out}	Active
L	H	H	H		High-impedance	Active

BLOCK DIAGRAM



※ Pin numbers inside dotted line show those of TSOP.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to GND	− 0.3~7	V
V_I	Input voltage		− 0.3 ~V_{CC} + 0.3	V
V_O	Output voltage		0~V_{CC}	V
P_d	Power dissipation	Ta = 25℃	700	mW
T_{opr}	Operating temperature		0~70	℃
T_{stg}	Storage temperature		− 65~150	℃

DC ELECTRICAL CHARACTERISTICS (Ta = 0~70℃, V_{CC} = 3.3 ± 0.3V, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits Min	Limits Typ	Limits Max	Unit
V_{IH}	High-level input voltage			2.0		V_{CC}+0.3	V
V_{IL}	Low-level input voltage			− 0.3		0.6	V
V_{OH1}	High-level output voltage 1	I_{OH} = − 1mA		2.4			V
V_{OH2}	High-level output voltage 2	I_{OH} = − 0.1mA		V_{CC}-0.5			V
V_{OL}	Low-level outout voltage	I_{OL} = 2mA				0.4	V
I_I	Input current	V_I = 0~V_{CC}				± 1	μA
I_O	Output current in off-state	$\overline{S_1}$ = V_{IH} or S_2 = V_{IL} or $\overline{OE}$ = V_{IH} $V_{I/O}$ = 0~V_{CC}				± 1	μA
I_{CC1}	Active supply current (Min cycle)	Output-open (duty 100%) $\overline{S_1}$ = V_{IL}, S_2 = V_{IH}, other inputs = V_{IH} or V_{IL}			15	30	mA
I_{CC2}	Active supply current (1MHz)	Output-open (duty 100%)			8	20	mA
I_{CC3}	Stand-by current	1) S_2 ≦ 0.2V, other inputs = 0~V_{CC}	-VL			60	μA
		2) $\overline{S_1}$ ≧ V_{CC} − 0.2V, S_2 ≧ V_{CC} − 0.2V, other inputs = 0~V_{CC}	-VLL		0.3	12	μA
I_{CC4}	Stand-by current	$\overline{S_1}$ = V_{IH} or S_2 = V_{IL}, other inputs = 0~V_{CC}				0.33	mA

CAPACITANCE (Ta = 0~70℃, V_{CC} = 3.3 ± 0.3V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits Min	Limits Typ	Limits Max	Unit
C_I	Input capacitance	V_I = GND, V_I = 25mVrms, f = 1MHz			6	pF
C_O	Output capacitance	V_O = GND, V_O = 25mVrms, f = 1MHz			8	pF

Note 1. Direction for current flowing into an IC is positive (no mark).
2. Typical value is V_{CC} = 3.3V, Ta = 25℃.

AC ELECTRICAL CHARACTERISTICS (T_a = 0~70℃, V_{CC} = 3.3 ± 0.3V, unless otherwise noted)

(1) MEASUREMENT CONDITIONS

Input pulse level ·····V_{IH} = 2.2V, V_{IL} = 0.4V

Input rise and fall time·····5ns

Reference level ·····V_{OH} = V_{OL} = 1.5V

Output loads ·····Fig.1, C_L = 30pF (FP, VP, RV-85VL,-10VL, -85VLL,-10VLL)

C_L = 5pF (for t_{en}, t_{dis})

Transition is measured ± 500mV from steady state voltage.(for t_{en}, t_{dis})

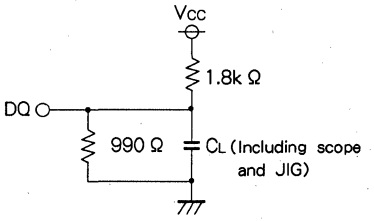


Fig. 1 Output load

(2) READ CYCLE

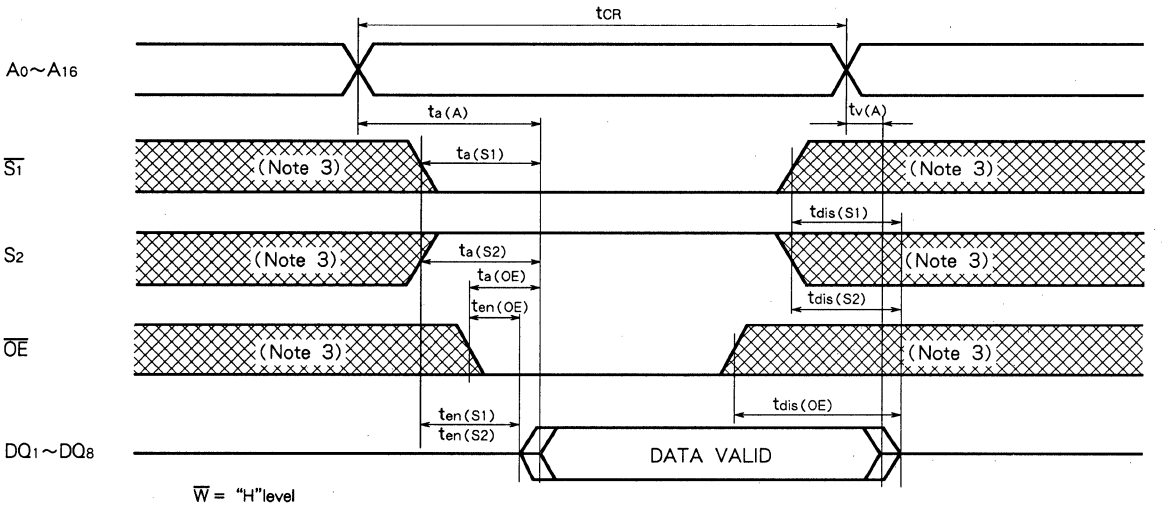
Symbol	Parameter	Limits						Unit
		M5M51008A -85VL,-85VLL			M5M51008A -10VL,-10VLL			
		Min	Typ	Max	Min	Typ	Max	
t_{CR}	Read cycle time	85			100			ns
$t_{a(A)}$	Address access time			85			100	ns
$t_{a(S1)}$	Chip select 1 access time			85			100	ns
$t_{a(S2)}$	Chip select 2 access time			85			100	ns
$t_{a(OE)}$	Output enable access time			45			50	ns
$t_{dis(S1)}$	Output disable time after $\overline{S_1}$ high			30			35	ns
$t_{dis(S2)}$	Output disable time after S_2 low			30			35	ns
$t_{dis(OE)}$	Output disable time after $\overline{OE}$ high			30			35	ns
$t_{en(S1)}$	Output enable time after $\overline{S_1}$ low	10			10			ns
$t_{en(S2)}$	Output enable time after S_2 high	10			10			ns
$t_{en(OE)}$	Output enable time after $\overline{OE}$ low	5			5			ns
$t_{v(A)}$	Data valid time after address	10			10			ns

(3) WRITE CYCLE

Symbol	Parameter	Limits						Unit
		M5M51008A -85VL,-85VLL			M5M51008A -10VL,-10VLL			
		Min	Typ	Max	Min	Typ	Max	
t_{CW}	Write cycle time	85			100			ns
$t_{w(W)}$	Write pulse width	65			75			ns
$t_{su(A)}$	Address set up time	0			0			ns
$t_{su(A-WH)}$	Address set up time with respect to $\overline{W}$	75			85			ns
$t_{su(S1)}$	Chip select 1 set up time	75			85			ns
$t_{su(S2)}$	Chip select 2 set up time	75			85			ns
$t_{su(D)}$	Data set up time	35			40			ns
$t_{h(D)}$	Data hold time	0			0			ns
$t_{rec(W)}$	Write recovery time	0			0			ns
$t_{dis(W)}$	Output disable time from $\overline{W}$ low			30			35	ns
$t_{dis(OE)}$	Output disable time from $\overline{OE}$ high			30			35	ns
$t_{en(W)}$	Output enable time from $\overline{W}$ high	5			5			ns
$t_{en(OE)}$	Output enable time from $\overline{OE}$ low	5			5			ns

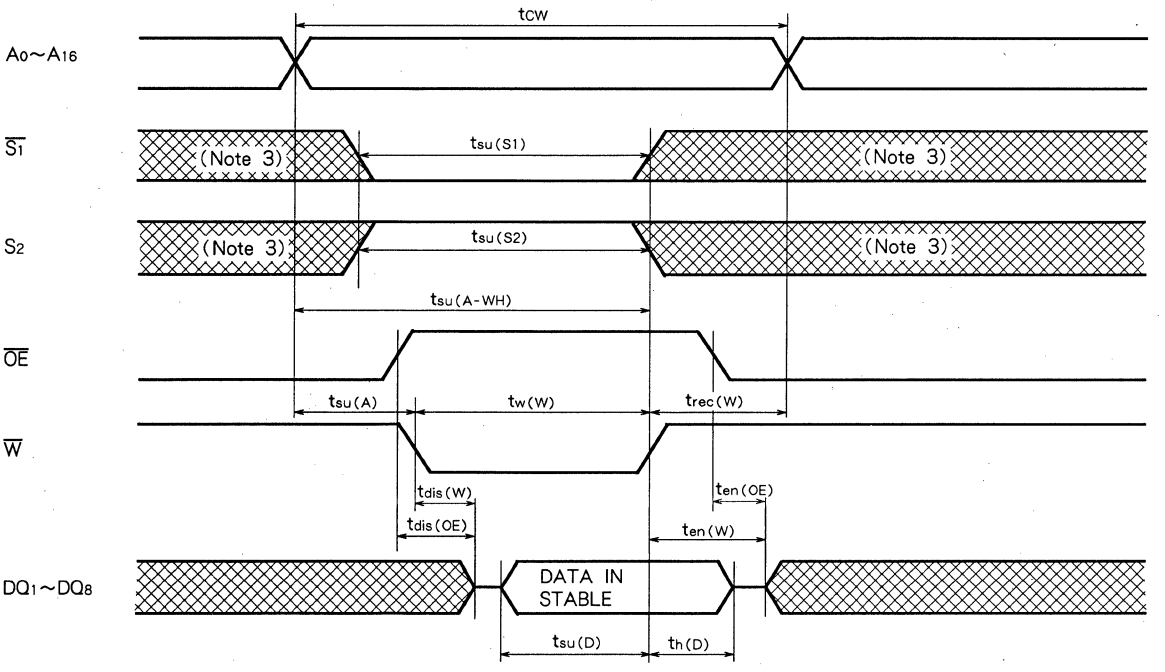
(4) TIMING DIAGRAMS

Read cycle

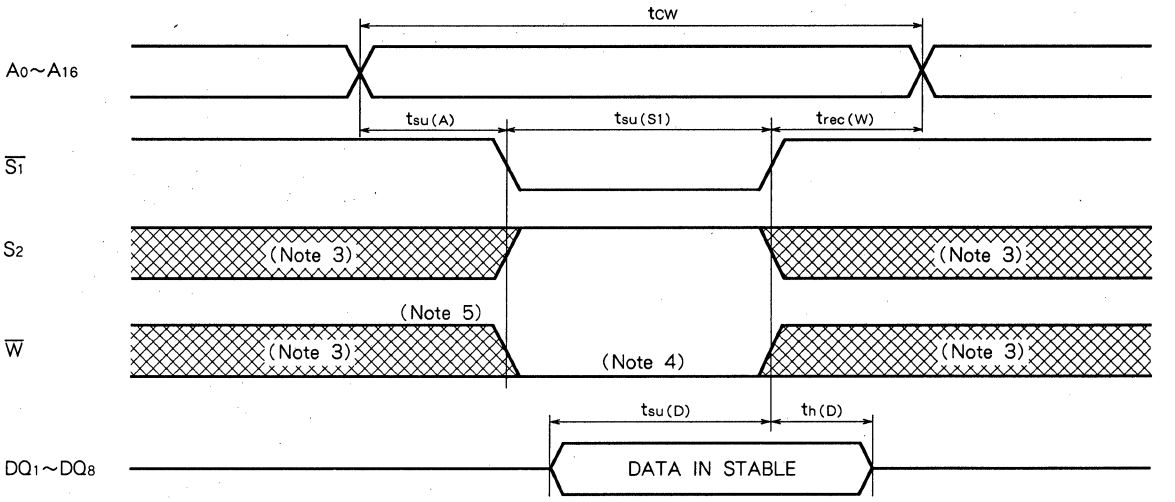


W = "H"level

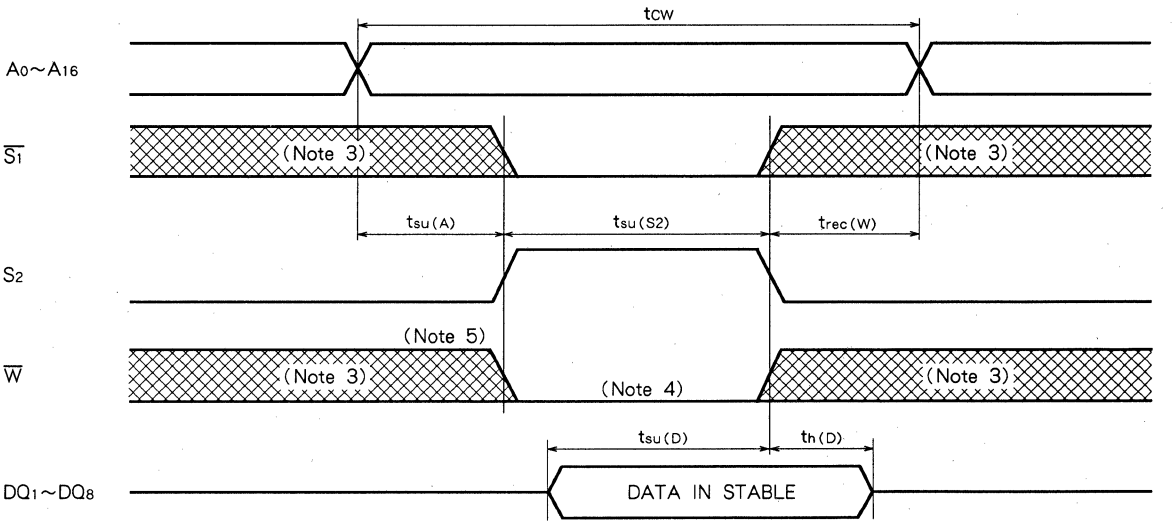
Write cycle (W control mode)



Write cycle ($\overline{S_1}$ control mode)



Write cycle (S_2 control mode)



Note 3. Hatching indicates the state is "don't care".
4. Writing is executed while S2 high overlaps $\overline{S_1}$ and $\overline{W}$ low.
5. When the falling edge of $\overline{W}$ is simultaneously or prior to the falling edge of $\overline{S_1}$ or rising edge of S2, the outputs are maintained in the high impedance state.
6. Don't apply inverted phase signal externally when DQ pin is output mode.

POWER DOWN CHARACTERISTICS

(1) ELECTRICAL CHARACTERISTICS (T_a = 0~70℃, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ	Max	
$V_{CC(PD)}$	Power down supply voltage			2			V
$V_{I(\overline{ST})}$	Chip select input $\overline{S_1}$			2.0			V
$V_{I(S2)}$	Chip select input S_2	3.0V ≦ $V_{CC(PD)}$				0.6	V
		$V_{CC(PD)}$ < 3.0V				0.2	
$I_{CC(PD)}$	Power down supply current	V_{CC} = 3V 1) S_2 ≦ 0.2V, other inputs = 0~3V 2) $\overline{S_1}$ ≧ V_{CC} − 0.2V, S_2 ≧ V_{CC} − 0.2V, other inputs = 0~3V	-VL			50	μA
			-VLL		0.3	10 (Note 7)	

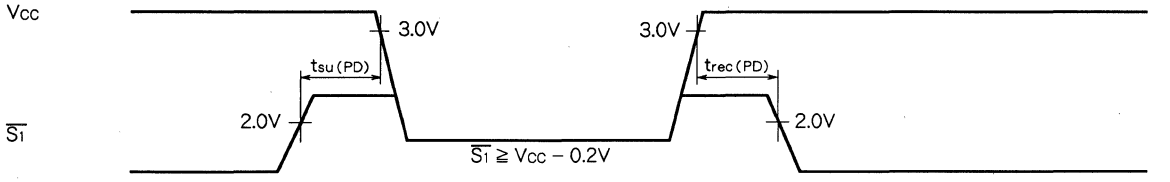
Note 7. $I_{CC(PD)}$ = 1 μA in case of T_a = 25℃.

(2) TIMING REQUIREMENTS (T_a = 0~70℃, unless otherwise noted)

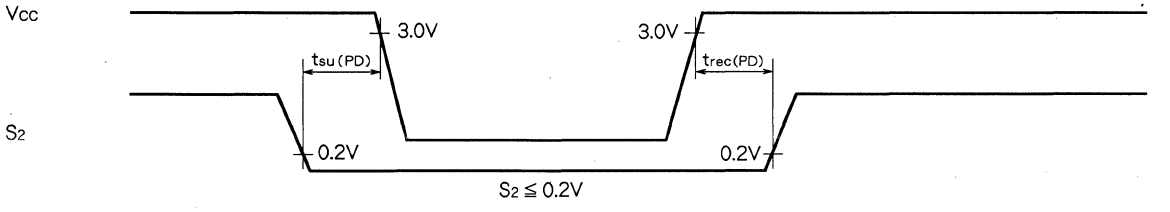
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{su(PD)}$	Power down set up time		0			ns
$t_{rec(PD)}$	Power down recovery time		5			ms

(3) POWER DOWN CHARACTERISTICS

$\overline{S_1}$ control mode



S_2 control mode



M5M51008AFP,VP,RV-12VL,-15VL, -12VLL,-15VLL

1048576-BIT(131072-WORD BY 8-BIT)CMOS STATIC RAM

DESCRIPTION

The M5M51008AFP, VP, RV are a 1048576-bit CMOS static RAM organized as 131072 word by 8-bit which are fabricated using high-performance triple polysilicon CMOS technology. The use of resistive load NMOS cells and CMOS periphery result in a high density and low power static RAM.

They are low stand-by current and low operation current and ideal for the battery back-up application.

The M5M51008AVP, RV are packaged in a 32-pin thin small outline package which is a high reliability and high density surface mount device (SMD). Two types of devices are available. M5M51008AVP (normal lead bend type package), M5M51008ARV (reverse lead bend type package). Using both types of devices, it became very easy to design a printed circuit board.

FEATURES

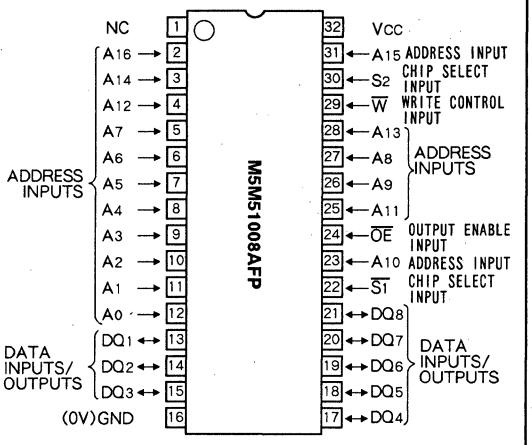
Type name	Access time (max)	Power supply current	
		Active (max)	Stand-by (max)
M5M51008AFP, VP, RV-12VL	120ns	15mA (1MHz)	55 μA (Vcc = 3.3V)
M5M51008AFP, VP, RV-15VL	150ns	5mA (1MHz)	
M5M51008AFP, VP, RV-12VLL	120ns	15mA (1MHz)	11 μA (Vcc = 3.3V) 0.3 μA (Vcc = 3.0V, typ)
M5M51008AFP, VP, RV-15VLL	150ns	5mA (1MHz)	

- Single + 2.7~5.5V power supply
- Low stand-by current 0.3 μA (typ.)
- Directly TTL compatible : All inputs and outputs
- Easy memory expansion and power down by $\overline{S1}$, S2
- Data hold on + 2V power supply
- Three-state outputs : OR-tie capability
- $\overline{OE}$ prevents data contention in the I/O bus
- Common data I/O
- Package
  M5M51008AFP ····· 32pin 525 mil SOP
  M5M51008AVP, RV ····· 32pin 8 × 20mm² TSOP

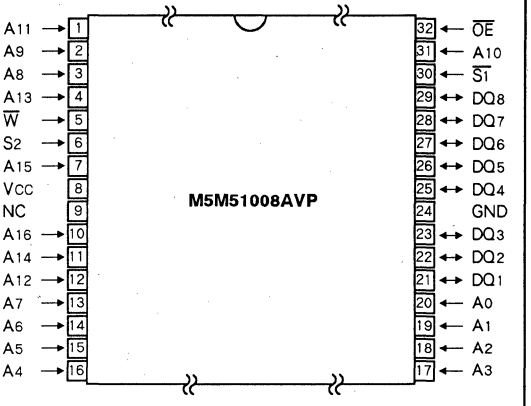
APPLICATION

Small capacity memory units

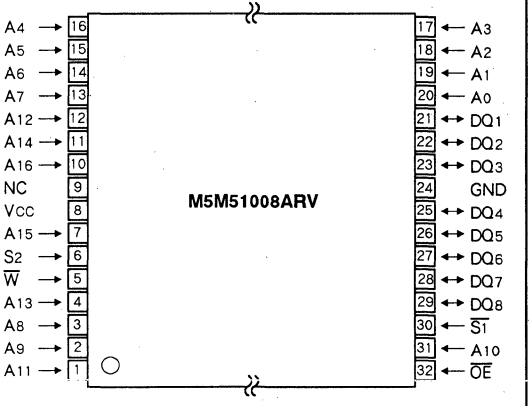
PIN CONFIGURATION (TOP VIEW)



Outline 32P2M-A



Outline 32P3H-E



Outline 32P3H-F

NC : NO CONNECTION

1048576-BIT(131072-WORD BY 8-BIT)CMOS STATIC RAM

FUNCTION

The operation mode of the M5M51008A series are determined by a combination of the device control inputs $\overline{S_1}$, S_2, $\overline{W}$ and $\overline{OE}$. Each mode is summarized in the function table.

A write cycle is executed whenever the low level $\overline{W}$ overlaps with the low level $\overline{S_1}$ and the high level S_2. The address must be set-up before the write cycle and must be stable during the entire cycle. The data is latched into a cell on the trailing edge of $\overline{W}$, $\overline{S_1}$ or S_2, whichever occurs first, requiring the set-up and hold time relative to these edge to be maintained. The output enable input $\overline{OE}$ directly controls the output stage. Setting the $\overline{OE}$ at a high level, the output stage is in a high-impedance state, and the data bus contention problem in the write cycle is eliminated.

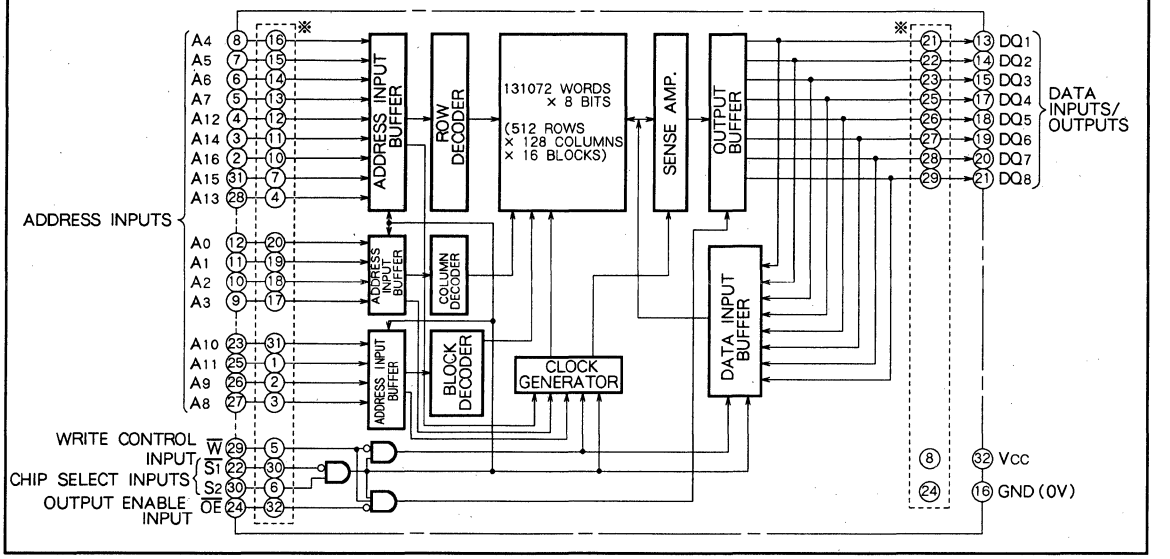
A read cycle is executed by setting $\overline{W}$ at a high level and $\overline{OE}$ at a low level while $\overline{S_1}$ and S_2 are in an active state ($\overline{S_1}$ = L, S_2 = H)

When setting $\overline{S_1}$ at a high level or S_2 at a low level, the chip are in a non-selectable mode in which both reading and writing are disabled. In this mode, the output stage is in a high-impedance state, allowing OR-tie with other chips and memory expansion by $\overline{S_1}$ and S_2. The power supply current is reduced as low as the stand-by current which is specified as I_{CC3} or I_{CC4}, and the memory data can be held at +2V power supply, enabling battery back-up operation during power failure or power-down operation in the non-selected mode.

FUNCTION TABLE

$\overline{S_1}$	S_2	$\overline{W}$	$\overline{OE}$	Mode	DQ	Icc
X	L	X	X	Non selection	High-impedance	Stand-by
H	X	X	X	Non selection	High-impedance	Stand-by
L	H	L	X	Write	Din	Active
L	H	H	L	Read	Dout	Active
L	H	H	H		High-impedance	Active

BLOCK DIAGRAM



※ Pin numbers inside dotted line show those of TSOP.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to GND	− 0.3~7	V
V_I	Input voltage		− 0.3 ~V_{CC} + 0.3	V
V_O	Output voltage		0~V_{CC}	V
P_d	Power dissipation	Ta = 25℃	700	mW
T_{opr}	Operating temperature		0~70	℃
T_{stg}	Storage temperature		− 65~150	℃

DC ELECTRICAL CHARACTERISTICS (Ta = 0~70℃, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits 1 (V_{CC} = 5V ± 10%) Min	Typ	Max	Limits 2 (V_{CC} = 3V ± 10%) Min	Typ	Max	Unit
V_{IH}	High-level input voltage			2.2		V_{CC}+0.3	2.0		V_{CC}+0.3	V
V_{IL}	Low-level input voltage			− 0.3		0.8	− 0.3		0.6	V
V_{OH1}	High-level output voltage 1	I_{OH} = − 1mA		2.4			2.4			V
V_{OH2}	High-level output voltage 2	I_{OH} = − 0.1mA		V_{CC}-0.5			V_{CC}-0.5			V
V_{OL}	Low-level outout voltage	I_{OL} = 2mA				0.4			0.4	V
I_I	Input current	V_I = 0~V_{CC}				± 1			± 1	μA
I_O	Output current in off-state	$\overline{S_1}$ = V_{IH} or S_2 = V_{IL} or $\overline{OE}$ = V_{IH} $V_{I/O}$ = 0~V_{CC}				± 1			± 1	μA
I_{CC1}	Active supply current (Min cycle)	$\overline{S_1}$ = V_{IL}, S_2 = V_{IH}, other inputs = V_{IH} or V_{IL} Output-open (duty 100%)	-12VL, -12VLL		30	60		10	20	mA
			-15VL, -15VLL		25	40		7	15	
I_{CC2}	Active supply current (1MHz)		-12VL, -12VLL		25	40		8	15	mA
			-15VL, -15VLL		7	15		2.5	5	
I_{CC3}	Stand-by current	1) S_2 ≦ 0.2V, other inputs = 0~V_{CC} 2) $\overline{S_1}$ ≧ V_{CC} − 0.2V, S_2 ≧ V_{CC} − 0.2V, other inputs = 0~V_{CC}	− VL			100			55	μA
			− VLL		0.5	20		0.3	11	μA
I_{CC4}	Stand-by current	$\overline{S_1}$ = V_{IH} or S_2 = V_{IL}, other inputs = 0~V_{CC}				3			0.33	mA

CAPACITANCE (Ta = 0~70℃, V_{CC} = 2.7~5.5V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits Min	Typ	Max	Unit
C_I	Input capacitance	V_I = GND, V_I = 25mV_{rms}, f = 1MHz			6	pF
C_O	Output capacitance	V_O = GND, V_O = 25mV_{rms}, f = 1MHz			8	pF

Note 1 : Direction for current flowing into an IC is positive (no mark).
2 : Typical value is V_{CC} = 5V, Ta = 25℃.

AC ELECTRICAL CHARACTERISTICS (T_a = 0~70℃, V_{CC} = 2.7~5.5V, unless otherwise noted)

(1) MEASUREMENT CONDITIONS

Input pulse level ····· V_{IH} = 2.4V, V_{IL} = 0.6V (V_{CC} = 5V ± 10%)
V_{IH} = 2.2V, V_{IL} = 0.4V (V_{CC} = 3V ± 10%)

Input rise and fall time ····· 5ns

Reference level ····· V_{OH} = V_{OL} = 1.5V

Output loads ····· Fig.1, C_L = 100pF (FP, VP, RV-15VL, -15VLL)
C_L = 30pF (FP, VP, RV-12VL, -12VLL)
C_L = 5pF (for t_{en}, t_{dis})

Transition is measured ± 500mV from steady state voltage.(for t_{en}, t_{dis})

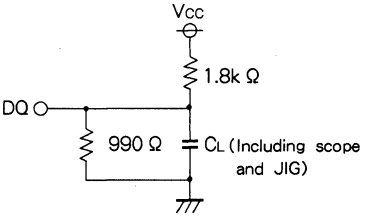


Fig. 1 Output load

(2) READ CYCLE

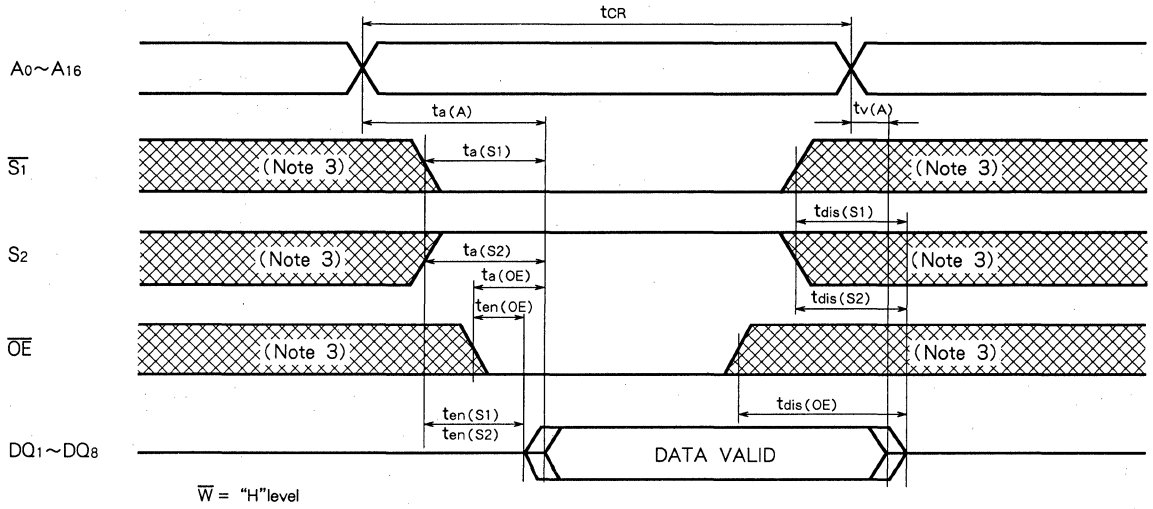
Symbol	Parameter	Limits						Unit
		M5M51008A -12VL,-12VLL			M5M51008A -15VL,-15VLL			
		Min	Typ	Max	Min	Typ	Max	
t_{CR}	Read cycle time	120			150			ns
$t_{a(A)}$	Address access time			120			150	ns
$t_{a(S1)}$	Chip select 1 access time			120			150	ns
$t_{a(S2)}$	Chip select 2 access time			120			150	ns
$t_{a(OE)}$	Output enable access time			60			75	ns
$t_{dis(S1)}$	Output disable time after $\overline{S_1}$ high			40			50	ns
$t_{dis(S2)}$	Output disable time after S_2 low			40			50	ns
$t_{dis(OE)}$	Output disable time after $\overline{OE}$ high			40			50	ns
$t_{en(S1)}$	Output enable time after $\overline{S_1}$ low	10			10			ns
$t_{en(S2)}$	Output enable time after S_2 high	10			10			ns
$t_{en(OE)}$	Output enable time after $\overline{OE}$ low	5			5			ns
$t_{v(A)}$	Data valid time after address	10			10			ns

(3) WRITE CYCLE

Symbol	Parameter	Limits						Unit
		M5M51008A -12VL,-12VLL			M5M51008A -15VL,-15VLL			
		Min	Typ	Max	Min	Typ	Max	
t_{CW}	Write cycle time	120			150			ns
$t_{w(W)}$	Write pulse width	85			100			ns
$t_{su(A)}$	Address set up time	0			0			ns
$t_{su(A-WH)}$	Address set up time with respect to $\overline{W}$	100			120			ns
$t_{su(S1)}$	Chip select 1 set up time	100			120			ns
$t_{su(S2)}$	Chip select 2 set up time	100			120			ns
$t_{su(D)}$	Data set up time	45			50			ns
$t_{h(D)}$	Data hold time	0			0			ns
$t_{rec(W)}$	Write recovery time	0			0			ns
$t_{dis(W)}$	Output disable time from $\overline{W}$ low			40			50	ns
$t_{dis(OE)}$	Output disable time from $\overline{OE}$ high			40			50	ns
$t_{en(W)}$	Output enable time from $\overline{W}$ high	5			5			ns
$t_{en(OE)}$	Output enable time from $\overline{OE}$ low	5			5			ns

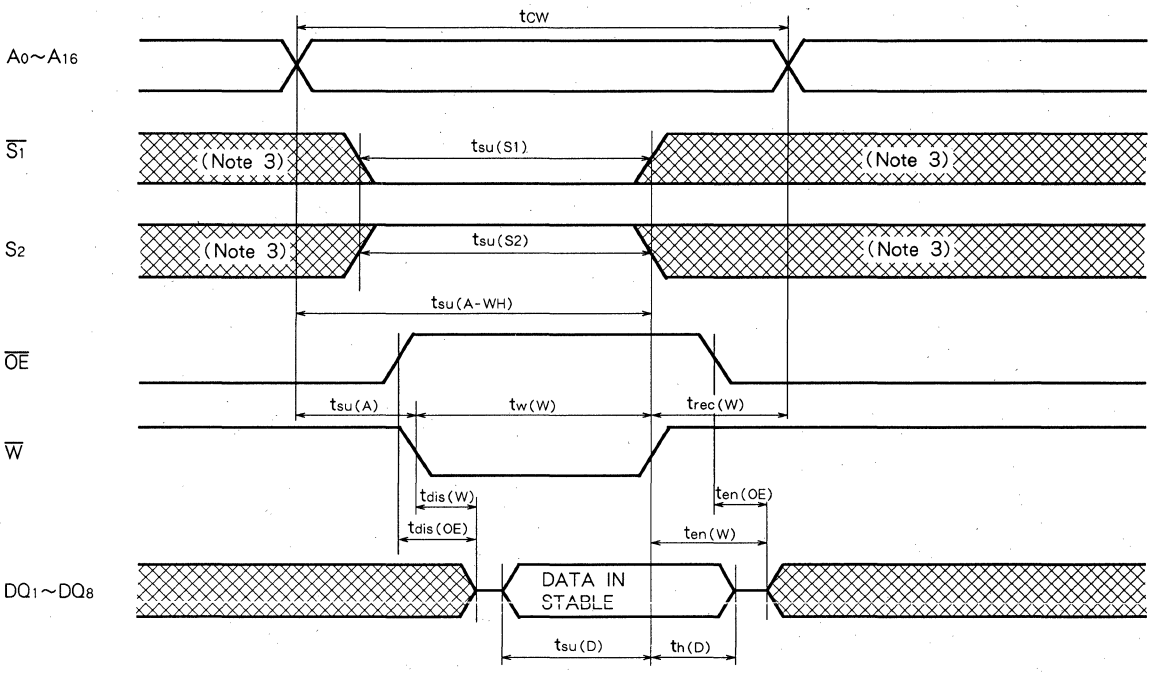
(4) TIMING DIAGRAMS

Read cycle

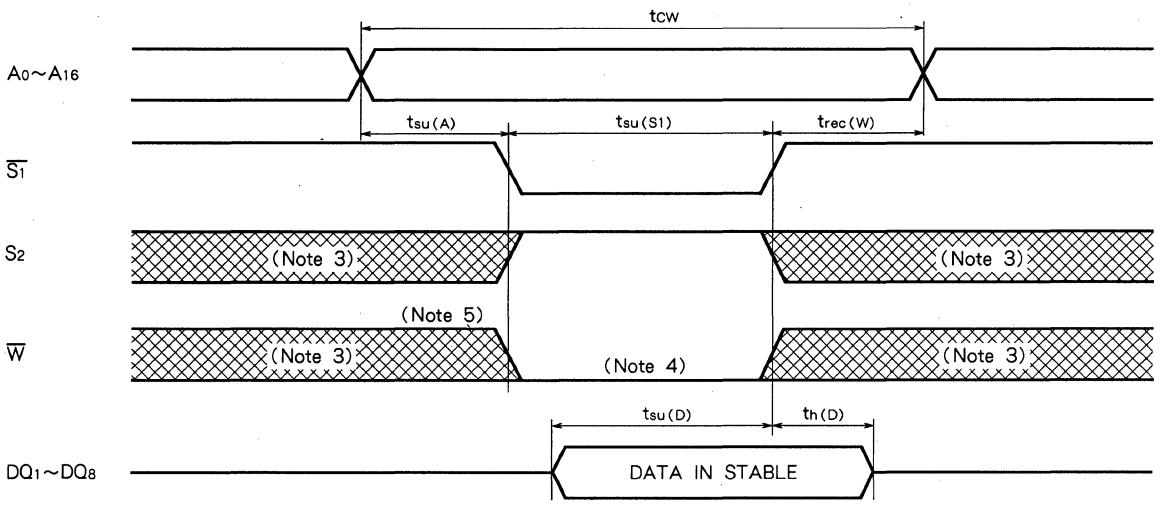


W = "H"level

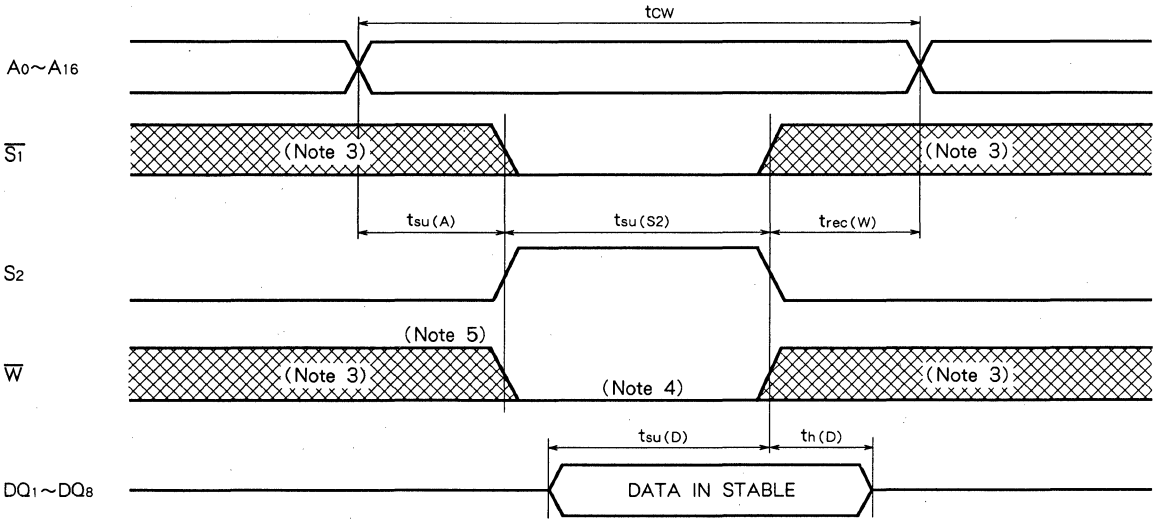
Write cycle (W control mode)



Write cycle ($\overline{S_1}$ control mode)



Write cycle (S_2 control mode)



Note 3 : Hatching indicates the state is "don't care".
4 : Writing is executed while S2 high overlaps $\overline{S1}$ and $\overline{W}$ low.
5 : When the falling edge of $\overline{W}$ is simultaneously or prior to the falling edge of $\overline{S1}$ or rising edge of S2, the outputs are maintained in the high impedance state.
6 : Don't apply inverted phase signal externally when DQ pin is output mode.

POWER DOWN CHARACTERISTICS

(1) ELECTRICAL CHARACTERISTICS (Ta = 0~70℃, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ	Max	
$V_{CC(PD)}$	Power down supply voltage			2			V
$V_{I(\overline{S1})}$	Chip select input $\overline{S1}$	$2.2V \leqq V_{CC(PD)}$		2.2			V
		$2V \leqq V_{CC(PD)} \leqq 2.2V$			$V_{CC(PD)}$		
$V_{I(S2)}$	Chip select input S_2	$4.5V \leqq V_{CC(PD)}$				0.8	V
		$V_{CC(PD)} < 4.5V$				0.2	
$I_{CC(PD)}$	Power down supply current	$V_{CC} = 3V$ 1) $S_2 \leqq 0.2V$, other inputs = 0~3V	-VL			50	μA
		2) $\overline{S1} \geqq V_{CC} - 0.2V$, $S_2 \geqq V_{CC} - 0.2V$, other inputs = 0~3V	-VLL		0.3	10 (Note 7)	

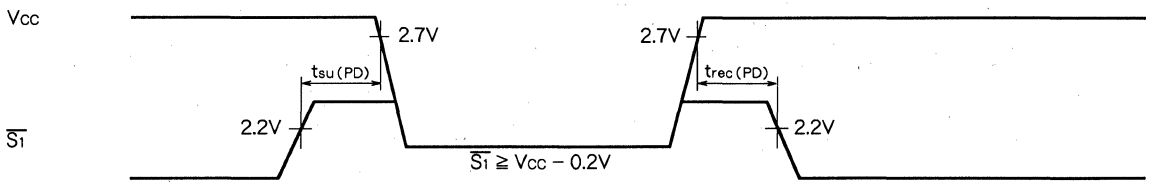
Note 7 : $I_{CC(PD)}$ = 1 μA in case of Ta = 25℃.

(2) TIMING REQUIREMENTS (Ta = 0~70℃, unless otherwise noted)

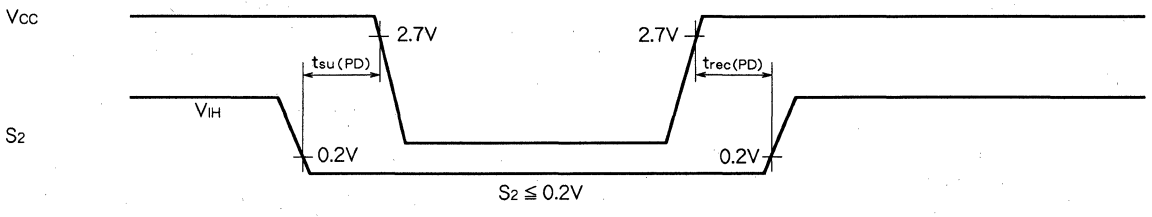
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{su(PD)}$	Power down set up time		0			ns
$t_{rec(PD)}$	Power down recovery time		5			ms

(3) POWER DOWN CHARACTERISTICS

$\overline{S1}$ control mode



S_2 control mode



M5M51T08AFP,VP,RV-85VSL,-10VSL

PRELIMINARY

Notice: This is not a final specification.
Some parametric limits are subject to change.

1048576-BIT(131072-WORD BY 8-BIT) CMOS STATIC RAM

DESCRIPTION

The M5M51T08AFP,VP,RV are a 1048576-bit CMOS static RAM organized as 131072-word by 8-bit which are fabricated using high-performance quadruple-polysilicon CMOS technology. The use of thin film transistor (TFT) load NMOS cells and CMOS periphery result in a high density, ultra low power and high reliability static RAM.

They are low standby current and low operation current and ideal for the battery back-up application.

The M5M51T08AVP,RV are packaged in a 32-pin thin small outline package which is a high reliability and high density surface mount device (SMD). Two types of devices are available. M5M51T08AVP (normal lead vend type package), M5M51T08ARV (reverce lead vend type package). Using both types of devices, it becames very easy to design a printed circuit board.

FEATURES

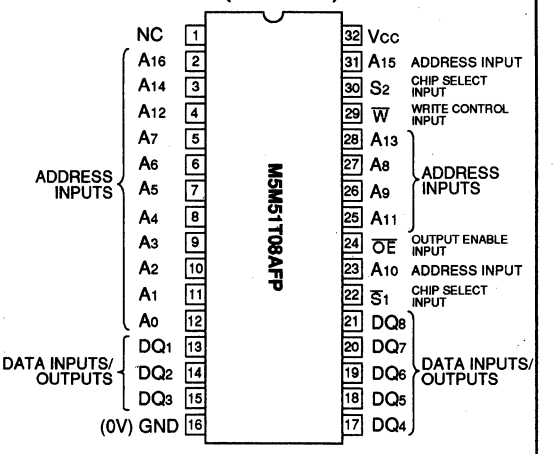
Type name	Access time (max)	Power supply current	
		Active (1MHz) (max)	Stand-by (max)
M5M51T08AFP,VP,RV-85VSL	85ns	20mA	2.4μA (V_{CC}=3.6V) 0.05μA (V_{CC}=3.0V typ.)
M5M51T08AFP,VP,RV-10VSL	100ns		

- Single +3.3V power supply
- Low stand-by current 0.05μA (typ.)
- Directly TTL compatible : All inputs and outputs
- Easy memory expansion and power down by $\overline{S}_1$, S_2
- Data hold on +2V power supply
- Three-state outputs : OR-tie capability
- $\overline{OE}$ prevents data contention in the I/O bus
- Common data I/O

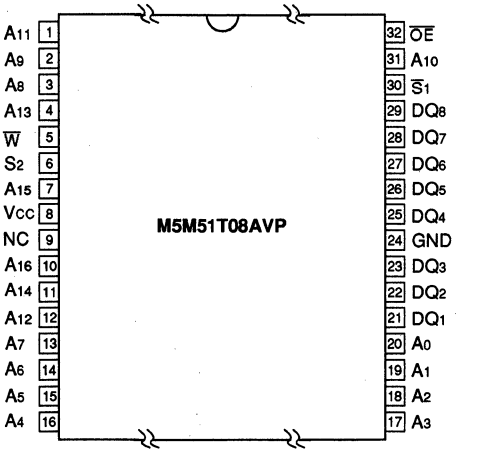
APPLICATION

Small capacity memory units

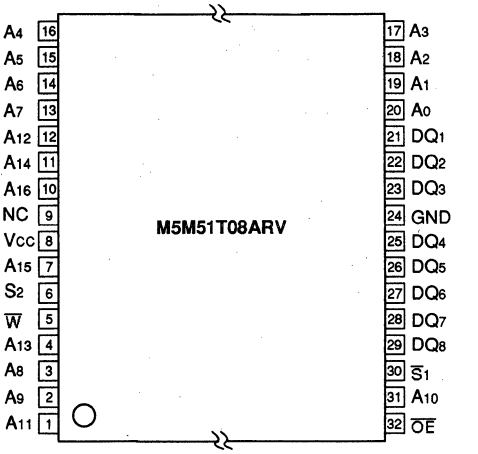
PIN CONFIGURATION (TOP VIEW)



Outline 32P2M-A



Outline 32P3H-E



Outline 32P3H-F

NC : NO CONNECTION

FUNCTION

The operation mode of the M5M51T08A series are determined by a combination of the device control inputs $\overline{S}_1$, S_2, $\overline{W}$ and $\overline{OE}$. Each mode is summarized in the function table.

A write cycle is executed whenever the low level $\overline{W}$ overlaps with the low level $\overline{S}_1$ and the high level S_2. The address must be set up before the write cycle and must be stable during the entire cycle. The data is latched into a cell on the trailing edge of $\overline{W}$, $\overline{S}_1$ or S_2, whichever occurs first, requiring the set-up and hold time relative to these edge to be maintained. The output enable input $\overline{OE}$ directly controls the output stage. Setting the $\overline{OE}$ at a high level, the output stage is in a high-impedance state, and the data bus contention problem in the write cycle is eliminated.

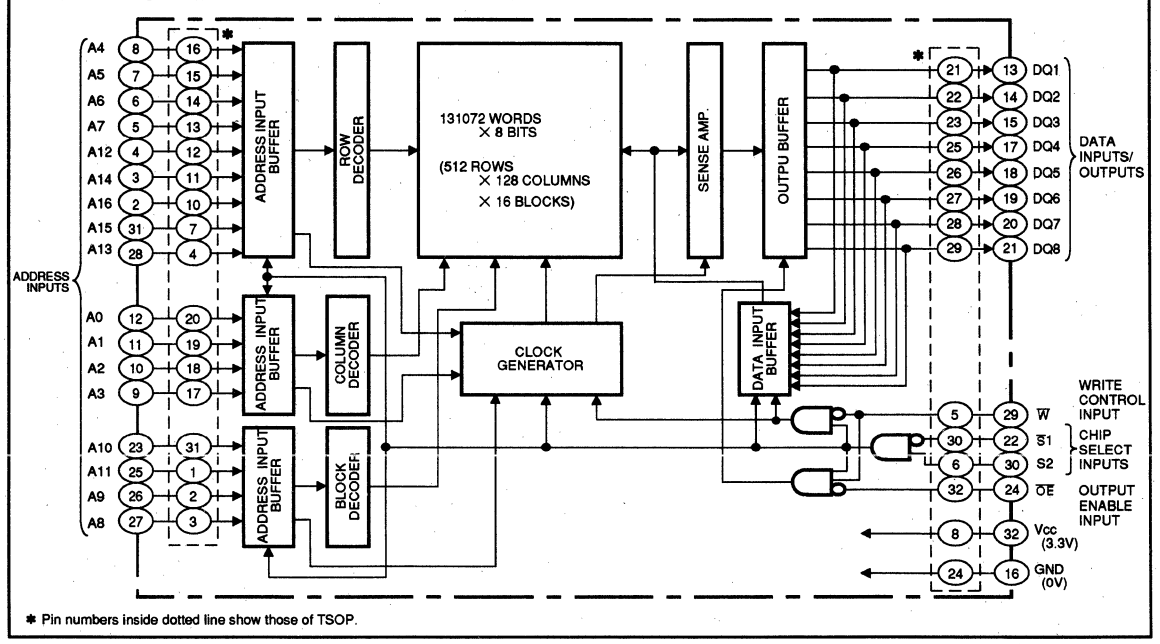
A read cycle is executed by setting $\overline{W}$ at a high level and $\overline{OE}$ at a low level while $\overline{S}_1$ and S_2 are in an active state ($\overline{S}_1$ = L, S_2 = H).

When setting $\overline{S}_1$ at a high level or S_2 at a low level, the chip are in a non-selectable mode in which both reading and writing are disabled. In this mode, the output stage is in a high-impedance state, allowing OR-tie with other chips and memory expansion by $\overline{S}_1$ and S_2. The power supply current is reduced as low as the stand-by current which is specified as I_{CC3} or I_{CC4}, and the memory data can be held at +2V power supply, enabling battery back-up operation during power failure or power-down operation in the non-selected mode.

FUNCTION TABLE

$\overline{S}_1$	S_2	$\overline{W}$	$\overline{OE}$	Mode	DQ	Icc
X	L	X	X	Non selection	High-impedance	Stand-by
H	X	X	X	Non selection	High-impedance	Stand-by
L	H	L	X	Write	Din	Active
L	H	H	L	Read	Dout	Active
L	H	H	H		High-impedance	Active

BLOCK DIAGRAM



* Pin numbers inside dotted line show those of TSOP.

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ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to GND	−0.3～7	V
V_I	Input voltage		−0.3～Vcc + 0.3	V
V_O	Output voltage		0～Vcc	V
P_d	Power dissipation	Ta = 25℃	700	mW
T_{opr}	Operating temperature		0～70	℃
T_{stg}	Storage temperature		−65～150	℃

DC ELECTRICAL CHARACTERISTICS (Ta = 0～70℃, Vcc = 3.3V±0.3V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{IH}	High-level input voltage		2.0		Vcc+0.3V	V
V_{IL}	Low-level input voltage		−0.3		0.6	V
V_{OH1}	High-level output voltage 1	I_{OH} = −1mA	2.4			V
V_{OH2}	High-level output voltage 2	I_{OH} = −0.1mA	Vcc−0.5V			V
V_{OL}	Low-level output voltage	I_{OL} = 2mA			0.4	V
I_I	Input current	V_I = 0～Vcc			±1	μA
I_O	Output current in off-state	$\overline{S_1}$ = V_{IH} or S_2 = V_{IL} or $\overline{OE}$ = V_{IH} $V_{I/O}$ = 0～Vcc			±1	μA
I_{CC1}	Active supply current (Min cycle)	$\overline{S_1}$ = V_{IL}, S_2 = V_{IH} other inputs = V_{IH} or V_{IL} Output-open (duty 100%)		15	30	mA
I_{CC2}	Active supply current (1MHz)			8	20	mA
I_{CC3}	Stand-by current	1) $S_2 \leqq 0.2V$, other inputs = 0～Vcc 2) $\overline{S_1} \geqq Vcc - 0.2V$, $S_2 \geqq Vcc - 0.2V$ other inputs = 0～Vcc			2.4	μA
I_{CC4}	Stand-by current	$\overline{S_1}$ = V_{IH} or S_2 = V_{IL}, other inputs = 0～Vcc			0.33	mA

CAPACITANCE (Ta = 0～70℃, Vcc = 3.3V±0.3V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
C_I	Input capacitance	V_I = GND, V_I = 25mVrms, f = 1MHz			6	pF
C_O	Output capacitance	V_O = GND, V_O = 25mVrms, f = 1MHz			8	pF

Note 1: Direction for current flowing into an IC is positive (no mark).
2: Typical value is Ta = 25℃.

AC ELECTRICAL CHARACTERISTICS (T_a = 0~70℃, V_{CC} = 3.3V±0.3V, unless otherwise noted)

(1) MEASUREMENT CONDITIONS

Input pulse level ····· V_{IH} = 2.2V, V_{IL} = 0.4V

Input rise and fall time ····· 5ns

Reference level ····· V_{OH} = V_{OL} = 1.5V

Output loads ····· Fig.1, C_L = 30pF

C_L = 5pF (for t_{en}, t_{dis})

Transition is measured ±500mV from steady state voltage. (for t_{en}, t_{dis})

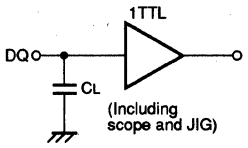


Fig.1 Output load

(2) READ CYCLE

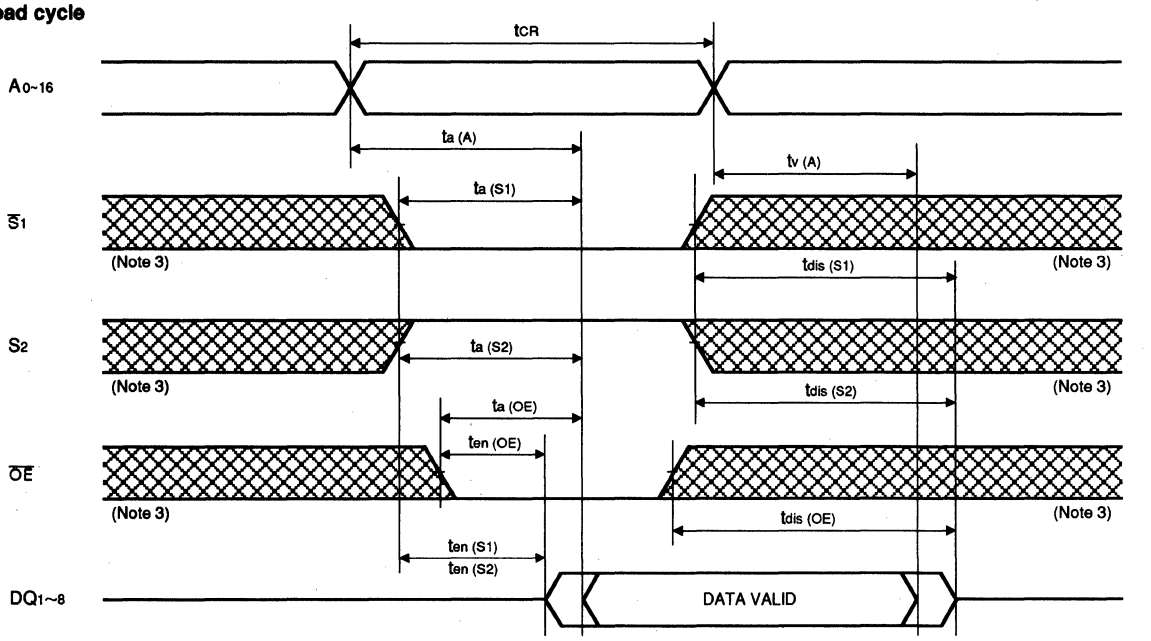
Symbol	Parameter	Limits				Unit
		M5M51T08A-85VSL		M5M51T08A-10VSL		
		Min	Max	Min	Max	
t_{CR}	Read cycle time	85		100		ns
$t_{a(A)}$	Address access time		85		100	ns
$t_{a(S1)}$	Chip select 1 access time		85		100	ns
$t_{a(S2)}$	Chip select 2 access time		85		100	ns
$t_{a(OE)}$	Output enable access time		45		50	ns
$t_{dis(S1)}$	Output disable time after $\overline{S_1}$ high		30		35	ns
$t_{dis(S2)}$	Output disable time after S_2 low		30		35	ns
$t_{dis(OE)}$	Output disable time after $\overline{OE}$ high		30		35	ns
$t_{en(S1)}$	Output enable time after $\overline{S_1}$ low	10		10		ns
$t_{en(S2)}$	Output enable time after S_2 high	10		10		ns
$t_{en(OE)}$	Output enable time after $\overline{OE}$ low	5		5		ns
$t_{v(A)}$	Data valid time after address	10		10		ns

(3) WRITE CYCLE

Symbol	Parameter	Limits				Unit
		M5M51T08A-85VSL		M5M51T08A-10VSL		
		Min	Max	Min	Max	
t_{CW}	Write cycle time	85		100		ns
$t_{w(W)}$	Write pulse width	65		75		ns
$t_{su(A)}$	Address setup time	0		0		ns
$t_{su(A-WH)}$	Address setup time with respect to W	75		85		ns
$t_{su(S1)}$	Chip select 1 setup time	75		85		ns
$t_{su(S2)}$	Chip select 2 setup time	75		85		ns
$t_{su(D)}$	Data setup time	35		40		ns
$t_{h(D)}$	Data hold time	0		0		ns
$t_{rec(W)}$	Write recovery time	0		0		ns
$t_{dis(W)}$	Output disable time from $\overline{W}$ low		30		35	ns
$t_{dis(OE)}$	Output disable time from $\overline{OE}$ high		30		35	ns
$t_{en(W)}$	Output enable time from $\overline{W}$ high	5		5		ns
$t_{en(OE)}$	Output enable time from $\overline{OE}$ low	5		5		ns

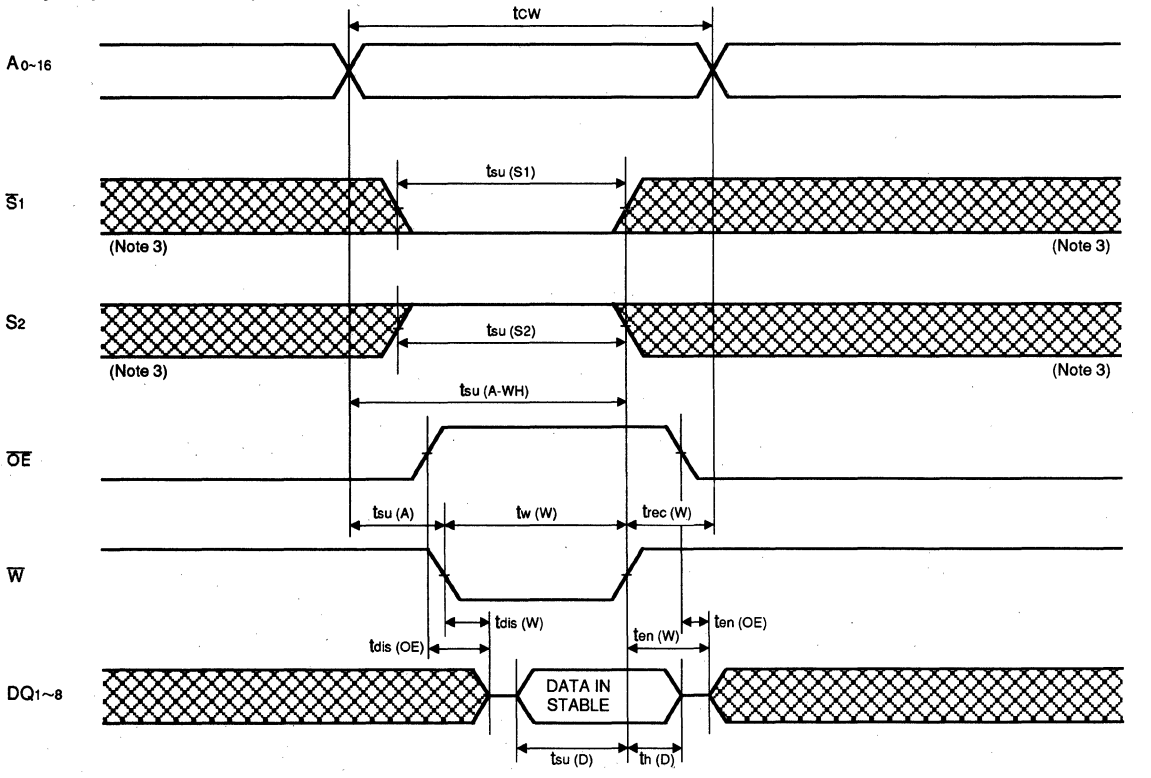
(4) TIMING DIAGRAMS

Read cycle

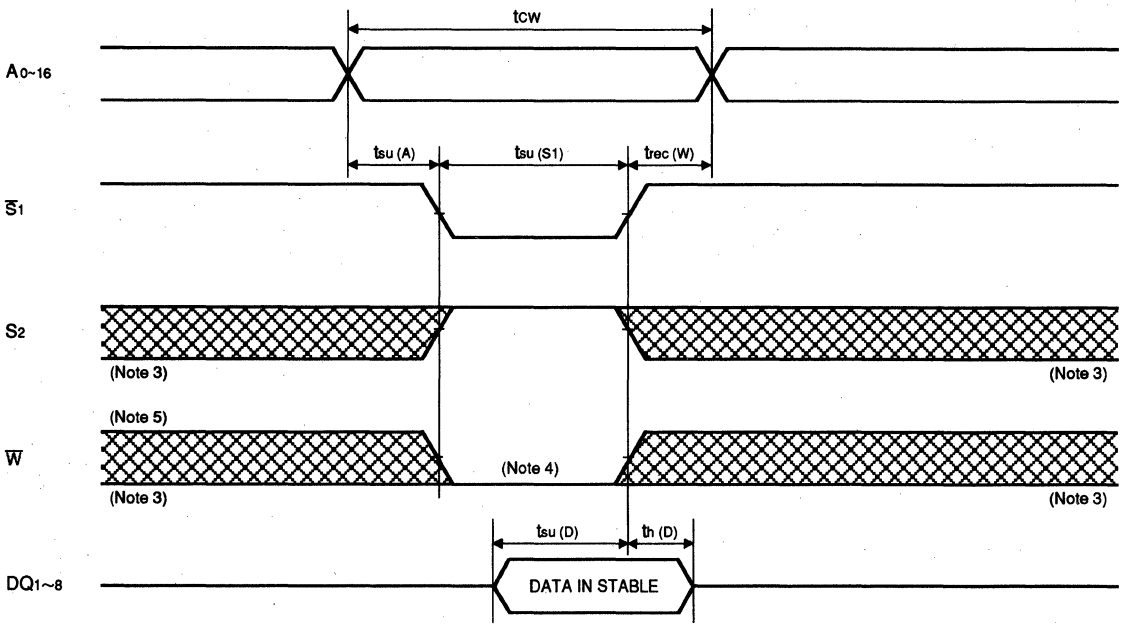


W = "H" level

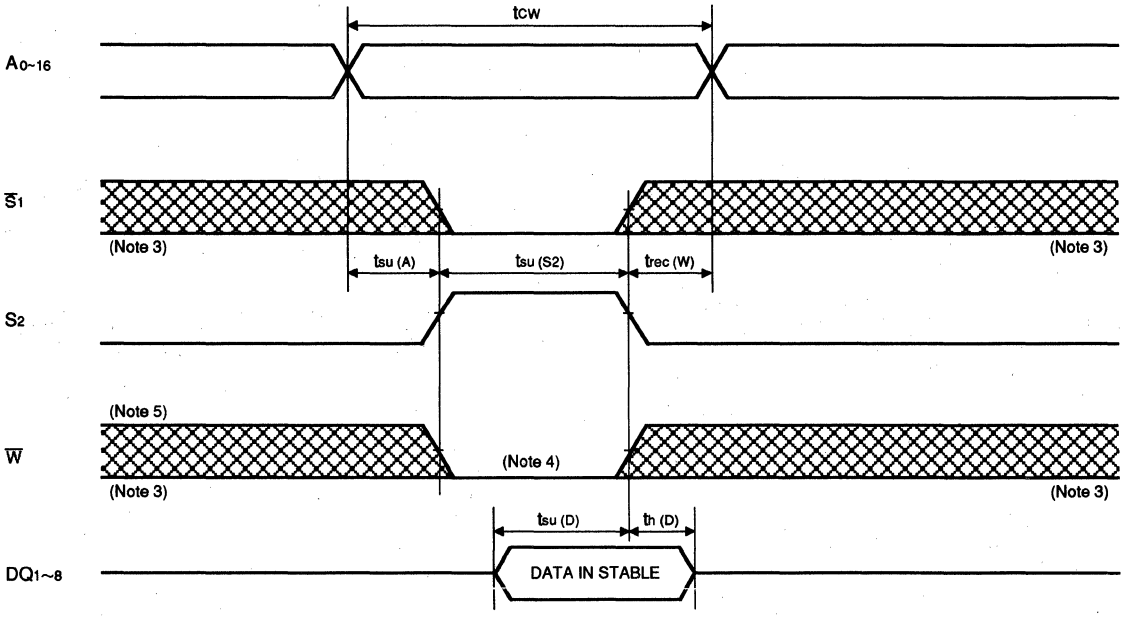
Write cycle (W control mode)



Write cycle ($\overline{S}_1$ control mode)



Write cycle (S_2 control mode)



Note 3 : Hatching indicates the state is "don't care".
4 : Writing is executed while S2 high overlaps $\overline{S}_1$ and $\overline{W}$ low.
5 : When the falling edge of $\overline{W}$ is simultaneously or prior to the falling edge of $\overline{S}_1$ or rising edge of S2 , the outputs are maintained in the high impedance state.
6 : Don't apply inverted phase signal externally when DQ pin is output mode.

POWER DOWN CHARACTERISTICS

(1) ELECTRICAL CHARACTERISTICS (T_a = 0～70℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$V_{CC\ (PD)}$	Power down supply voltage		2			V
$V_{I\ (\overline{S1})}$	Chip select input $\overline{S_1}$		2.0			V
$V_{I\ (S2)}$	Chip select input S_2	$3.0V \leqq V_{CC\ (PD)}$			0.6	V
		$V_{CC\ (PD)} < 3.0V$			0.2	
$I_{CC\ (PD)}$	Power down supply current	V_{CC} = 3V 1) $S_2 \leqq 0.2V$, other inputs=0～3V 2) $\overline{S_1} \geqq V_{CC} - 0.2V$, $S_2 \geqq V_{CC} - 0.2V$, other inputs=0～3V		0.05	2 (Note 7)	μA

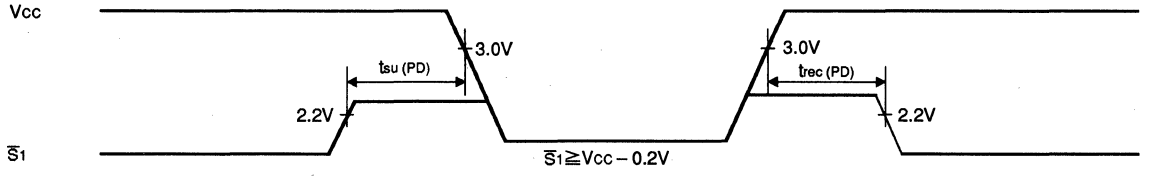
Note 7: $I_{CC\ (PD)}$ = 0.2 μA in case of T_a = 25℃

(2) TIMING REQUIREMENTS (T_a = 0～70℃, unless otherwise noted)

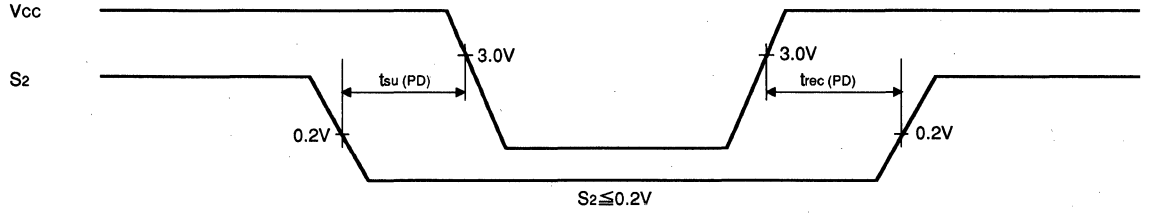
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{su\ (PD)}$	Power down set up time		0			ns
$t_{rec\ (PD)}$	Power down recovery time		5			ms

(3) POWER DOWN CHARACTERISTICS

$\overline{S_1}$ control mode



S_2 control mode



M5M51T08AFP,VP,RV-12VSL,-15VSL

PRELIMINARY

Notice: This is not a final specification.
Some parametric limits are subject to change.

1048576-BIT(131072-WORD BY 8-BIT) CMOS STATIC RAM

DESCRIPTION

The M5M51T08AFP,VP,RV are a 1048576-bit CMOS static RAM organized as 131072-word by 8-bit which are fabricated using high-performance quadruple-polysilicon CMOS technology. The use of thin film transistor (TFT) load NMOS cells and CMOS periphery result in a high density, ultra low power and high reliability static RAM.

They are low standby current and low operation current and ideal for the battery back-up application.

The M5M51T08AVP,RV are packaged in a 32-pin thin small outline package which is a high reliability and high density surface mount device (SMD). Two types of devices are available. M5M51T08AVP (normal lead vend type package), M5M51T08ARV (reverce lead vend type package). Using both types of devices, it becames very easy to design a printed circuit board.

FEATURES

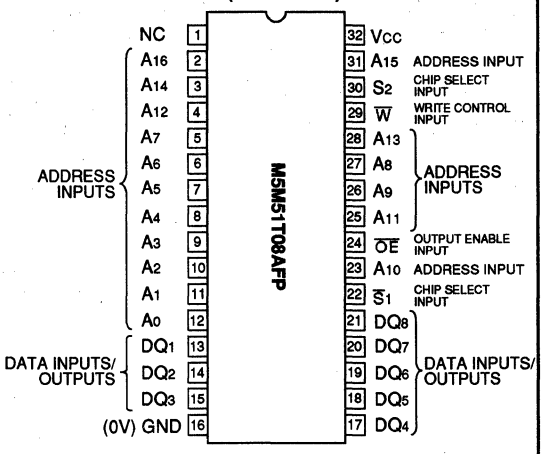
Type name	Access time (max)	Power supply current	
		Active (1MHz) (max)	Stand-by (max)
M5M51T08AFP,VP,RV-12VSL	120ns	15mA	2.2μA (Vcc=3.3V) 0.05μA (Vcc=3.0V,typ.)
M5M51T08AFP,VP,RV-15VSL	150ns	5mA	

- Single +2.7~5.5V power supply
- Low stand-by current 0.05μA (typ.)
- Directly TTL compatible : All inputs and outputs
- Easy memory expansion and power down by $\overline{S}_1$, S_2
- Data hold on +2V power supply
- Three-state outputs : OR-tie capability
- $\overline{OE}$ prevents data contention in the I/O bus
- Common data I/O

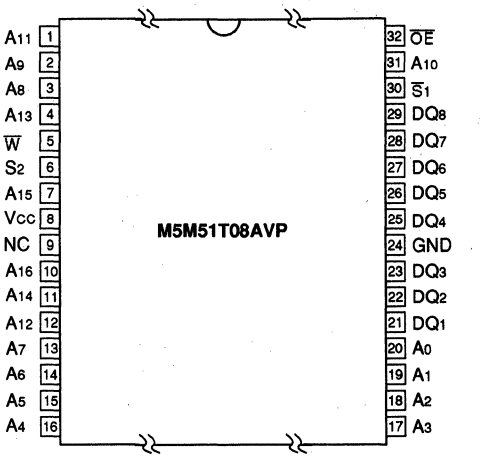
APPLICATION

Small capacity memory units

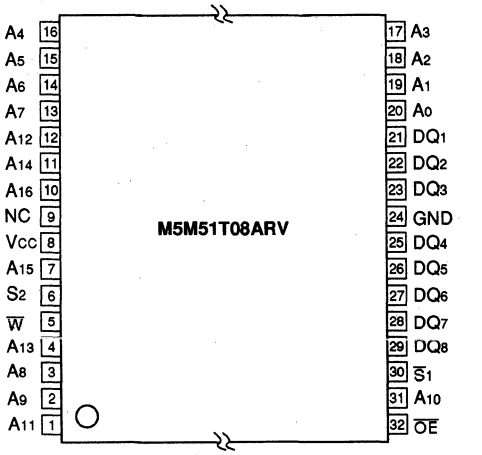
PIN CONFIGURATION (TOP VIEW)



Outline 32P2M-A



Outline 32P3H-E



Outline 32P3H-F

NC : NO CONNECTION

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FUNCTION

The operation mode of the M5M51T08A series are determined by a combination of the device control inputs $\overline{S}_1$, S_2, $\overline{W}$ and $\overline{OE}$. Each mode is summarized in the function table.

A write cycle is executed whenever the low level $\overline{W}$ overlaps with the low level $\overline{S}_1$ and the high level S_2. The address must be set up before the write cycle and must be stable during the entire cycle. The data is latched into a cell on the trailing edge of $\overline{W}$, $\overline{S}_1$ or S_2, whichever occurs first, requiring the set-up and hold time relative to these edge to be maintained. The output enable input $\overline{OE}$ directly controls the output stage. Setting the $\overline{OE}$ at a high level, the output stage is in a high-impedance state, and the data bus contention problem in the write cycle is eliminated.

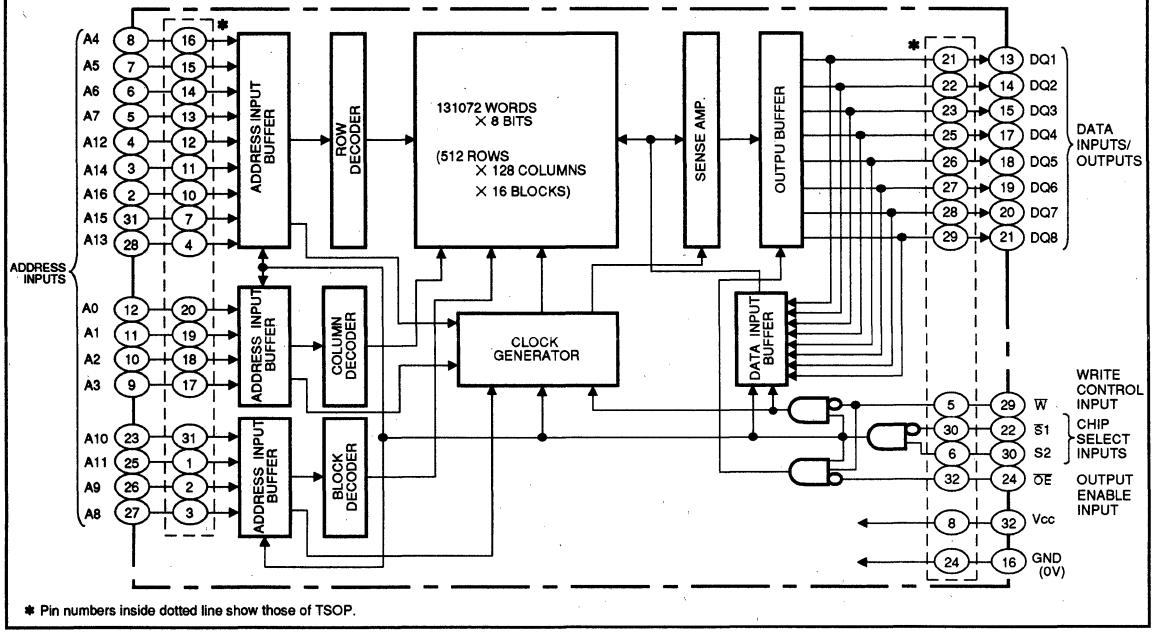
A read cycle is executed by setting $\overline{W}$ at a high level and $\overline{OE}$ at a low level while $\overline{S}_1$ and S_2 are in an active state ($\overline{S}_1$ = L, S_2 = H).

When setting $\overline{S}_1$ at a high level or S_2 at a low level, the chip are in a non-selectable mode in which both reading and writing are disabled. In this mode, the output stage is in a high-impedance state, allowing OR-tie with other chips and memory expansion by $\overline{S}_1$ and S_2. The power supply current is reduced as low as the stand-by current which is specified as I_{CC3} or I_{CC4}, and the memory data can be held at +2V power supply, enabling battery back-up operation during power failure or power-down operation in the non-selected mode.

FUNCTION TABLE

$\overline{S}_1$	S_2	$\overline{W}$	$\overline{OE}$	Mode	DQ	Icc
X	L	X	X	Non selection	High-impedance	Stand-by
H	X	X	X	Non selection	High-impedance	Stand-by
L	H	L	X	Write	Din	Active
L	H	H	L	Read	Dout	Active
L	H	H	H		High-impedance	Active

BLOCK DIAGRAM



* Pin numbers inside dotted line show those of TSOP.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to GND	−0.3～7	V
V_I	Input voltage		−0.3～Vcc + 0.3	V
V_O	Output voltage		0～Vcc	V
P_d	Power dissipation	Ta = 25℃	700	mW
T_{opr}	Operating temperature		0～70	℃
T_{stg}	Storage temperature		−65～150	℃

DC ELECTRICAL CHARACTERISTICS (Ta = 0～70℃, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits 1 (Vcc = 5V±10%) Min	Typ	Max	Limits 2 (Vcc = 3V±10%) Min	Typ	Max	Unit
V_{IH}	High-level input voltage			2.2		Vcc+0.3V	2.0		Vcc+0.3V	V
V_{IL}	Low-level input voltage			−0.3		0.8	−0.3		0.6	V
V_{OH1}	High-level output voltage 1	I_{OH} = −1mA		2.4			2.4			V
V_{OH2}	High-level output voltage 2	I_{OH} = −0.1mA		Vcc−0.5V			Vcc−0.5V			V
V_{OL}	Low-level output voltage	I_{OL} = 2mA				0.4			0.4	V
I_I	Input current	V_I = 0～Vcc				±1			±1	μA
I_O	Output current in off-state	$\overline{S_1}$ = V_{IH} or S_2 = V_{IL} or $\overline{OE}$ = V_{IH} V_{IO} = 0～Vcc				±1			±1	μA
I_{CC1}	Active supply current (Min cycle)	$\overline{S_1}$ = V_{IL}, S_2 = V_{IH} other inputs = V_{IH} or V_{IL} Output-open (duty 100%)	-12VSL		30	60		10	20	mA
			-15VSL		25	40		7	15	
I_{CC2}	Active supply current (1MHz)		-12VSL		25	40		8	15	mA
			-15VSL		7	15		2.5	5	
I_{CC3}	Stand-by current	1) S_2≦0.2V, other inputs = 0～Vcc 2) $\overline{S_1}$≧Vcc − 0.2V, S_2≧Vcc − 0.2V other inputs = 0～Vcc				10		0.05	2.2	μA
I_{CC4}	Stand-by current	$\overline{S_1}$ = V_{IH} or S_2 = V_{IL}, other inputs = 0～Vcc				3			0.33	mA

CAPACITANCE (Ta = 0～70℃, Vcc = 2.7V～5.5V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits Min	Typ	Max	Unit
C_I	Input capacitance	V_I = GND, V_I = 25mVrms, f = 1MHz			6	pF
C_O	Output capacitance	V_O = GND, V_O = 25mVrms, f = 1MHz			8	pF

Note 1: Direction for current flowing into an IC is positive (no mark).
2: Typical value is Ta = 25℃.

AC ELECTRICAL CHARACTERISTICS (Ta = 0~70℃, Vcc = 2.7~5.5V, unless otherwise noted)

(1) MEASUREMENT CONDITIONS

Input pulse level ···V_{IH} = 2.4V, V_{IL} = 0.6V (V_{CC} = 5V±10%)

V_{IH} = 2.2V, V_{IL} = 0.4V (V_{CC}= 3V±10%)

Input rise and fall time ····· 5ns

Reference level ····· V_{OH} = V_{OL} = 1.5V

Output loads ····· Fig.1, C_L = 100pF (FP, VP, RV-15VSL)

C_L = 30pF (FP, VP, RV-12VSL)

C_L = 5pF (for t_{en}, t_{dis})

Transition is measured ±500mV from steady state voltage. (for t_{en}, t_{dis})

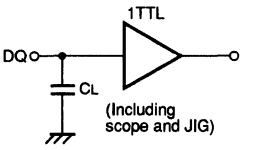


Fig.1 Output load

(2) READ CYCLE

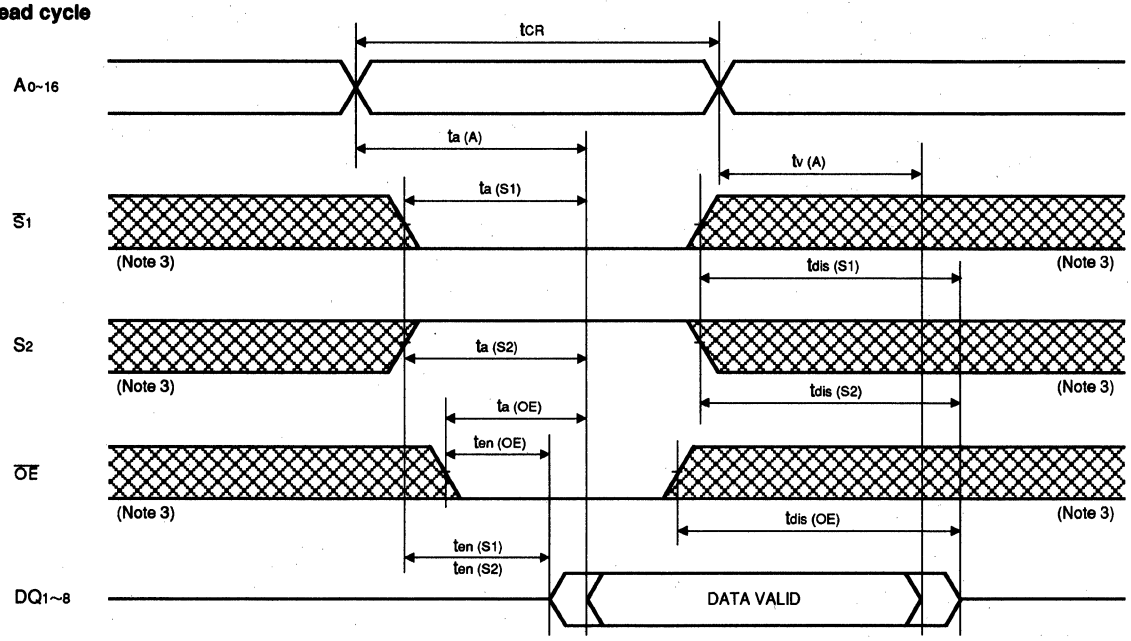
Symbol	Parameter	Limits				Unit
		M5M51T08A-12VSL		M5M51T08A-15VSL		
		Min	Max	Min	Max	
t_{CR}	Read cycle time	120		150		ns
$t_{a(A)}$	Address access time		120		150	ns
$t_{a(S1)}$	Chip select 1 access time		120		150	ns
$t_{a(S2)}$	Chip select 2 access time		120		150	ns
$t_{a(OE)}$	Output enable access time		60		75	ns
$t_{dis(S1)}$	Output disable time after $\overline{S_1}$ high		40		50	ns
$t_{dis(S2)}$	Output disable time after S_2 low		40		50	ns
$t_{dis(OE)}$	Output disable time after $\overline{OE}$ high		40		50	ns
$t_{en(S1)}$	Output enable time after $\overline{S_1}$ low	10		10		ns
$t_{en(S2)}$	Output enable time after S_2 high	10		10		ns
$t_{en(OE)}$	Output enable time after $\overline{OE}$ low	5		5		ns
$t_{v(A)}$	Data valid time after address	10		10		ns

(3) WRITE CYCLE

Symbol	Parameter	Limits				Unit
		M5M51T08A-12VSL		M5M51T08A-15VSL		
		Min	Max	Min	Max	
t_{CW}	Write cycle time	120		150		ns
$t_{w(W)}$	Write pulse width	85		100		ns
$t_{su(A)}$	Address setup time	0		0		ns
$t_{su(A-WH)}$	Address setup time with respect to W	100		120		ns
$t_{su(S1)}$	Chip select 1 setup time	100		120		ns
$t_{su(S2)}$	Chip select 2 setup time	100		120		ns
$t_{su(D)}$	Data setup time	45		50		ns
$t_{h(D)}$	Data hold time	0		0		ns
$t_{rec(W)}$	Write recovery time	0		0		ns
$t_{dis(W)}$	Output disable time from $\overline{W}$ low		40		50	ns
$t_{dis(OE)}$	Output disable time from $\overline{OE}$ high		40		50	ns
$t_{en(W)}$	Output enable time from $\overline{W}$ high	5		5		ns
$t_{en(OE)}$	Output enable time from $\overline{OE}$ low	5		5		ns

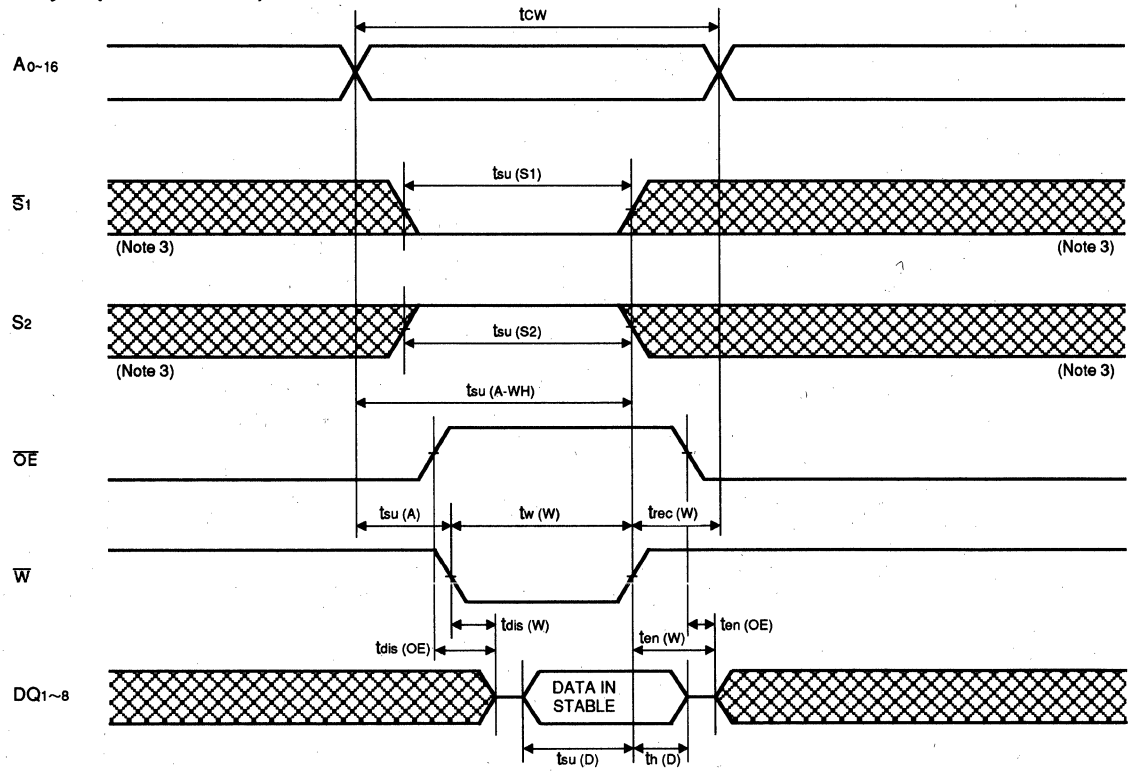
(4) TIMING DIAGRAMS

Read cycle

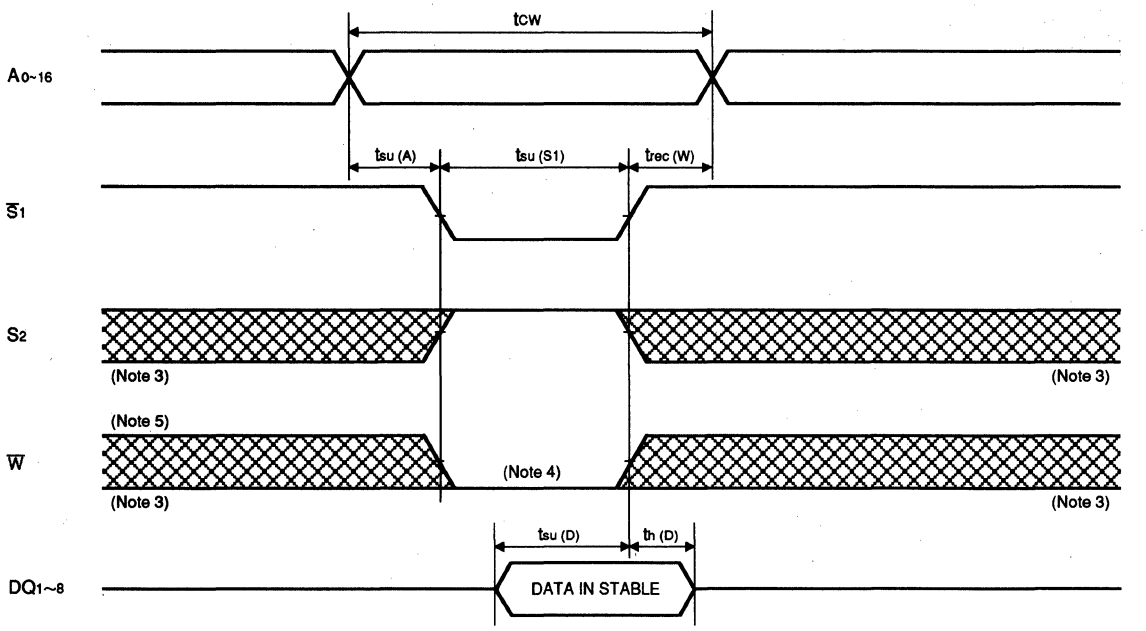


W = "H" level

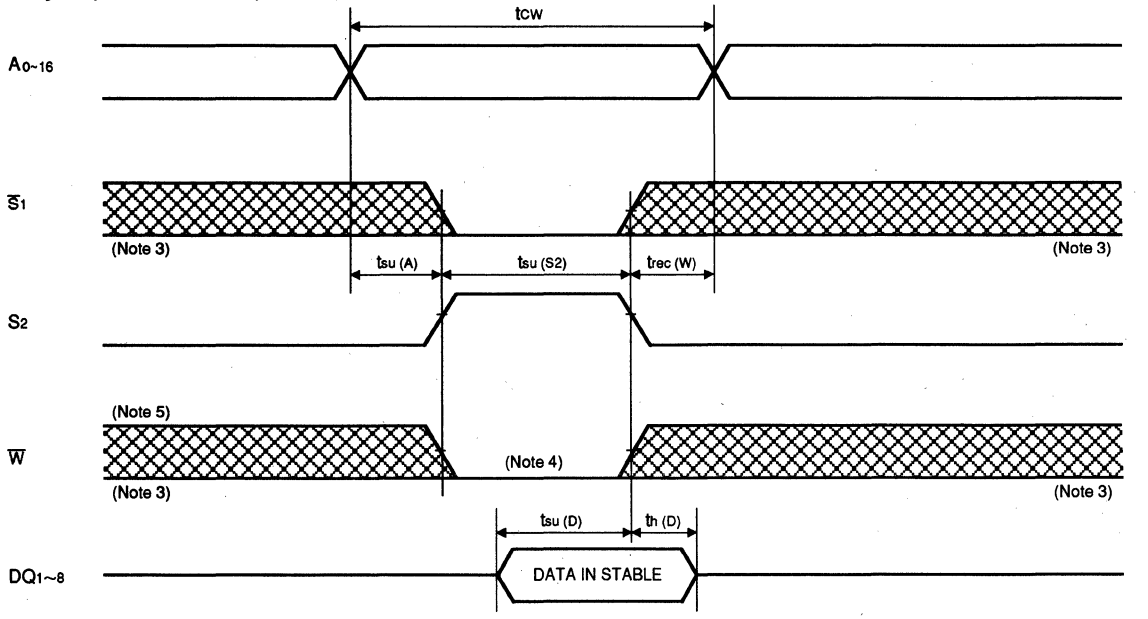
Write cycle (W control mode)



Write cycle ($\overline{S}_1$ control mode)



Write cycle (S_2 control mode)



Note 3 : Hatching indicates the state is "don't care".
4 : Writing is executed while S2 high overlaps $\overline{S}_1$ and $\overline{W}$ low.
5 : When the falling edge of $\overline{W}$ is simultaneously or prior to the falling edge of $\overline{S}_1$ or rising edge of S2 , the outputs are maintained in the high impedance state.
6 : Don't apply inverted phase signal externally when DQ pin is output mode.

POWER DOWN CHARACTERISTICS

(1) ELECTRICAL CHARACTERISTICS (Ta = 0~70℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$V_{CC\ (PD)}$	Power down supply voltage		2			V
$V_{I\ (\overline{S}1)}$	Chip select input $\overline{S}_1$	$2.2V \leqq V_{CC\ (PD)}$	2.2			V
		$2V \leqq V_{CC\ (PD)} \leqq 2.2V$		$V_{CC\ (PD)}$		
$V_{I\ (S2)}$	Chip select input S_2	$4.5V \leqq V_{CC\ (PD)}$			0.8	V
		$V_{CC\ (PD)} < 4.5V$			0.2	
$I_{CC\ (PD)}$	Power down supply current	V_{CC} = 3V 1) $S_2 \leqq 0.2V$, other inputs = 0~3V 2) $\overline{S}_1 \geqq V_{CC} - 0.2V$, $S_2 \geqq V_{CC} - 0.2V$, other inputs = 0~3V		0.05	2 (Note 7)	μA

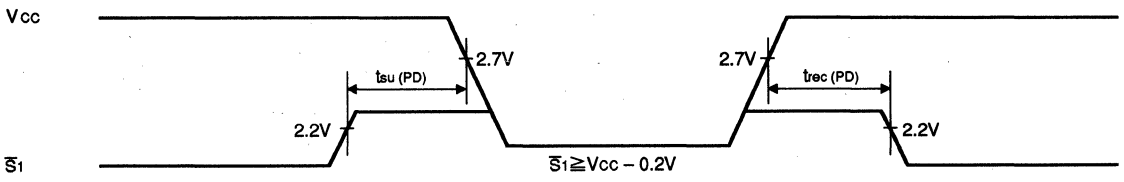
Note 7 : $I_{CC\ (PD)}$ = 0.2μA in case of Ta = 25℃

(2) TIMING REQUIREMENTS (Ta = 0~70℃, unless otherwise noted)

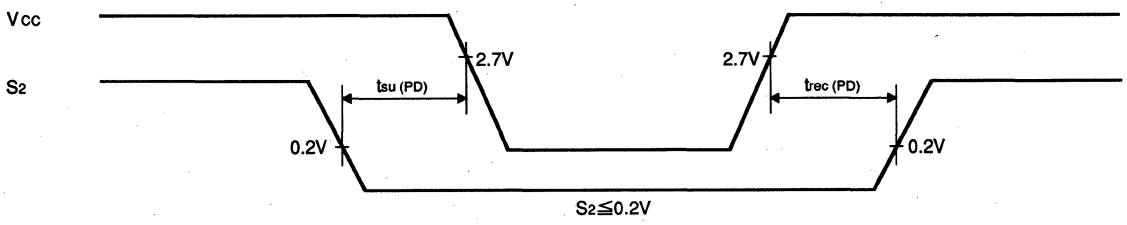
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{su\ (PD)}$	Power down set up time		0			ns
$t_{rec\ (PD)}$	Power down recovery time		5			ms

(3) POWER DOWN CHARACTERISTICS

$\overline{S}_1$ control mode



S_2 control mode



M5M51008BFP,VP,RV -70VL, -10VL, -12VL, -15VL, -70VLL,-10VLL,-12VLL,-15VLL

1048576-BIT(131072-WORD BY 8-BIT)CMOS STATIC RAM

PRELIMINARY

Notice: This is not a final specification.
Some parametric limits are subject to change.

DESCRIPTION

The M5M51008BFP,VP,RV are a 1048576-bit CMOS static RAM organized as 131072 word by 8-bit which are fabricated using high-performance triple polysilicon CMOS technology. The use of resistive load NMOS cells and CMOS periphery result in a high density and low power static RAM.

They are low standby current and low operation current and ideal for the battery back-up application.

The M5M51008BVP,RV are packaged in a 32-pin thin small outline package which is a high reliability and high density surface mount device(SMD).Two types of devices are available. M5M51008BVP (normal lead bend type package), M5M51008BRV (reverse lead bend type package). Using both types of devices, it becomes very easy to design a printed circuit board.

FEATURES

Type name	Access time (max)	Vcc	Power supply current	
			Active (1MHz) (max)	stand-by (max)
M5M51008BFP,VP,RV - 70VL	70ns	3.3±0.3V	25mA	60μA
M5M51008BFP,VP,RV - 10VL	100ns			
M5M51008BFP,VP,RV - 12VL	120ns	3.0±0.3V*	10mA	55μA
M5M51008BFP,VP,RV - 15VL	150ns			
M5M51008BFP,VP,RV - 70VLL	70ns	3.3±0.3V	25mA	12μA
M5M51008BFP,VP,RV - 10VLL	100ns			
M5M51008BFP,VP,RV - 12VLL	120ns	3.0±0.3V*	10mA	11μA
M5M51008BFP,VP,RV - 15VLL	150ns			

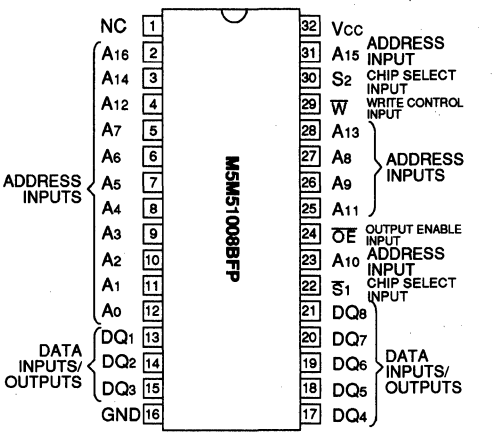
*Note Vcc=2.7~5.5V abailable

- Single power supply
- Low stand-by current 0.3 μA (typ.)
- Directly TTL compatible : All inputs and outputs
- Easy memory expansion and power down by $\overline{S}_1$,S_2
- Data hold on +2V power supply
- Three-state outputs : OR - tie capability
- $\overline{OE}$ prevents data contention in the I/O bus
- Common data I/O
- Package
  - M5M51008BFP ..... 32 pin 525 mil SOP
  - M5M51008BVP,RV ..... 32 pin 8 × 20 mm² TSOP

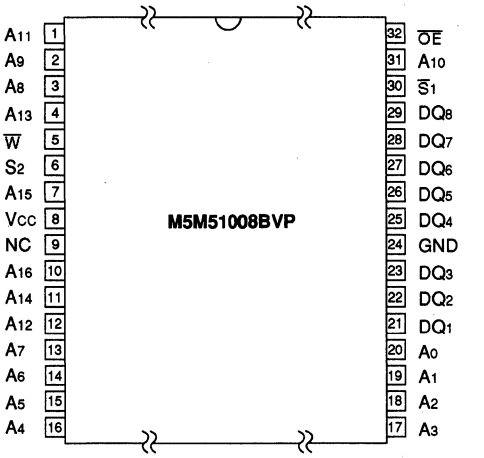
APPLICATION

Small capacity memory units

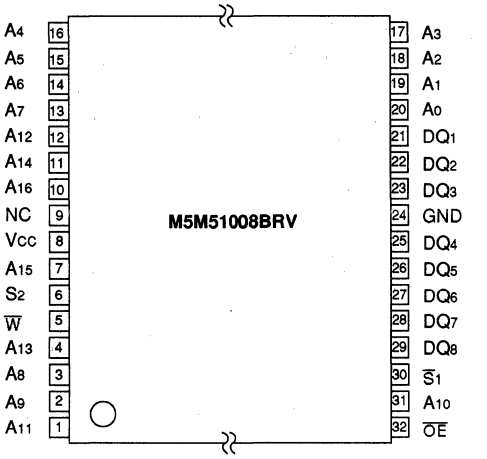
PIN CONFIGURATION (TOP VIEW)



Outline 32P2M-A



Outline 32P3H-E



Outline 32P3H-F

NC : NO CONNECTION

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

M5M51008BFP,VP,RV -70VL,-10VL,-12VL,-15VL, -70VLL,-10VLL,-12VLL,-15VLL

1048576-BIT(131072-WORD BY 8-BIT)CMOS STATIC RAM

FUNCTION

The operation mode of the M5M51008B series are determined by a combination of the device control inputs $\overline{S}_1$,S_2,$\overline{W}$ and $\overline{OE}$.

Each mode is summarized in the function table.

A write cycle is executed whenever the low level $\overline{W}$ overlaps with the low level $\overline{S}_1$ and the high level S_2. The address must be set up before the write cycle and must be stable during the entire cycle. The data is latched into a cell on the trailing edge of $\overline{W}$,$\overline{S}_1$ or S_2,whichever occurs first,requiring the set-up and hold time relative to these edge to be maintained. The output enable input $\overline{OE}$ directly controls the output stage. Setting the $\overline{OE}$ at a high level, the output stage is in a high-impedance state, and the data bus contention problem in the write cycle is eliminated.

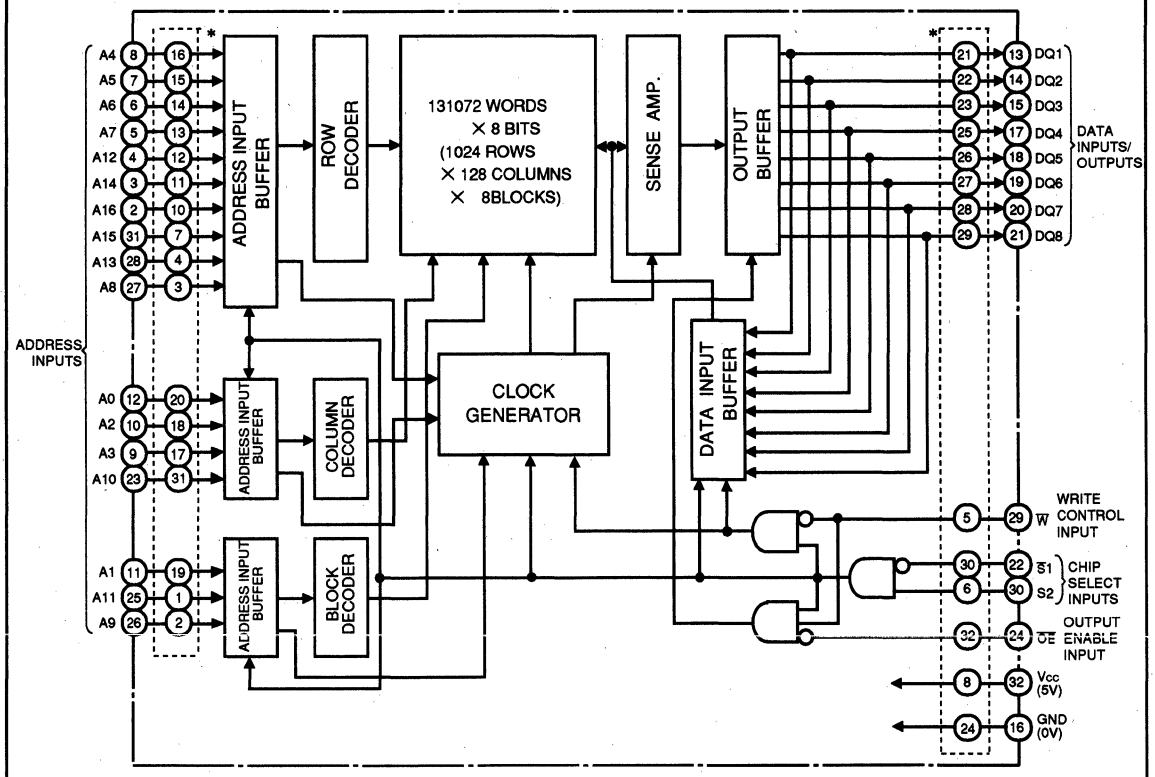
A read cycle is executed by setting $\overline{W}$ at a high level and $\overline{OE}$ at a low level while $\overline{S}_1$ and S_2 are in an active state($\overline{S}_1$=L,S_2=H).

When setting $\overline{S}_1$ at a high level or S_2 at a low level, the chip are in a non-selectable mode in which both reading and writing are disabled. In this mode, the output stage is in a high- impedance state, allowing OR-tie with other chips and memory expansion by $\overline{S}_1$ and S_2. The power supply current is reduced as low as the stand-by current which is specified as I_{CC3} or I_{CC4}, and the memory data can be held at +2V power supply, enabling battery back-up operation during power failure or power-down operation in the non-selected mode.

FUNCTION TABLE

$\overline{S}_1$	S_2	$\overline{W}$	$\overline{OE}$	Mode	DQ	Icc
X	L	X	X	Non selection	High-impedance	Stand-by
H	X	X	X	Non selection	High-impedance	Stand-by
L	H	L	X	Write	Din	Active
L	H	H	L	Read	Dout	Active
L	H	H	H		High-impedance	Active

BLOCK DIAGRAM



* Pin numbers inside dotted line show those of TSOP

MITSUBISHI ELECTRIC

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to GND	−0.3*~7	V
V_I	Input voltage		−0.3*~Vcc + 0.3	V
V_O	Output voltage		0~Vcc	V
P_d	Power dissipation	Ta=25℃	700	mW
T_{opr}	Operating temperature		0~70	℃
T_{stg}	Storage temperature		−65~150	℃

* −3.0V in case of AC (Pulse width ≦ 30ns)

DC ELECTRICAL CHARACTERISTICS (Ta=0~70℃, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits									Unit
				-70VL, -70VLL -10VL, -10VLL			-12VL, -12VLL -15VL, -15VLL						
				Vcc=3.3±0.3V			Vcc=5.0±0.5V			Vcc=3.0±0.3V			
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{IH}	High-level input voltage			2.0		Vcc +0.3V	2.2		Vcc +0.3V	2.0		Vcc +0.3V	V
V_{IL}	Low-level input voltage			−0.3		0.6	−0.3		0.8	−0.3		0.6	V
V_{OH1}	High-level output voltage 1	I_{OH}= −0.5mA		2.4			2.4			2.4			V
V_{OH2}	High-level output voltage 2	I_{OH}= −0.05mA		Vcc -0.5V			Vcc -0.5V			Vcc -0.5V			V
V_{OL}	Low-level output voltage	I_{OL}=2mA				0.4			0.4			0.4	V
I_I	Input current	V_I=0~Vcc				±1			±1			±1	μA
I_O	Output current in off-state	$\overline{S_1}$=V_{IH} or S_2=V_{IL} or $\overline{OE}$=V_{IH} $V_{I/O}$=0~Vcc				±1			±1			±1	μA
I_{CC1}	Active supply current (Min cycle)	$\overline{S_1}$=V_{IL}, S_2=V_{IH}, other inputs=V_{IH} or V_{IL} Output-open(duty 100%)			15	30		25	50		10	20	mA
I_{CC2}	Active supply current (1MHz)				2	10		5	15		2	10	mA
I_{CC3}	Stand-by current	S_2≦0.2V or $\overline{S_1}$≧Vcc-0.2V, S_2≧Vcc-0.2V other inputs=0~Vcc	-L			60			100			55	μA
			-LL			12			20			11	μA
I_{CC4}	Stand-by current	$\overline{S_1}$=V_{IH} or S_2=V_{IL}, other inputs=0~Vcc				0.33			3			0.33	mA

* −3.0V in case of AC (Pulse width ≦ 30ns)

CAPACITANCE (Ta=0~70℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
C_I	Input capacitance	V_I=GND, V_I=25mVrms, f=1MHz			6	pF
C_O	Output capacitance	V_O=GND, V_O=25mVrms, f=1MHz			8	pF

Note 1: Direction for current flowing into an IC is positive (no mark).
2: Typical value is Vcc = 5V, Ta = 25℃

AC ELECTRICAL CHARACTERISTICS (Ta = 0～70℃, unless otherwise noted)

(1) MEASUREMENT CONDITIONS

Vcc ····· 3.3±0.3V(FP,VP,RV-70VL,-70VLL,-10VL,-10VLL)
2.7～5.5V(FP,VP,RV-12VL,-12VLL,-15VL,-15VLL)
Input pulse level ····· V_{IH}=2.2V, V_{IL}=0.4V
Input rise and fall time ····· 5ns
Reference level ····· V_{OH}=V_{OL}=1.5V
Output loads ····· Fig.1, C_L=100pF (FP,VP,RV-15VL,-15VLL,)
C_L=30pF (FP,VP,RV-70VL,-10VL,12VL,-70VLL,-10VLL,12VLL)
C_L=5pF (for t_{en},t_{dis})
Transition is measured ±500mV from steady state voltage. (for t_{en},t_{dis})

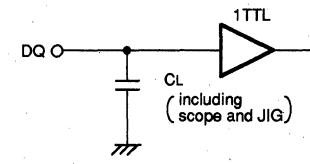


Fig.1 Output load

(2) READ CYCLE

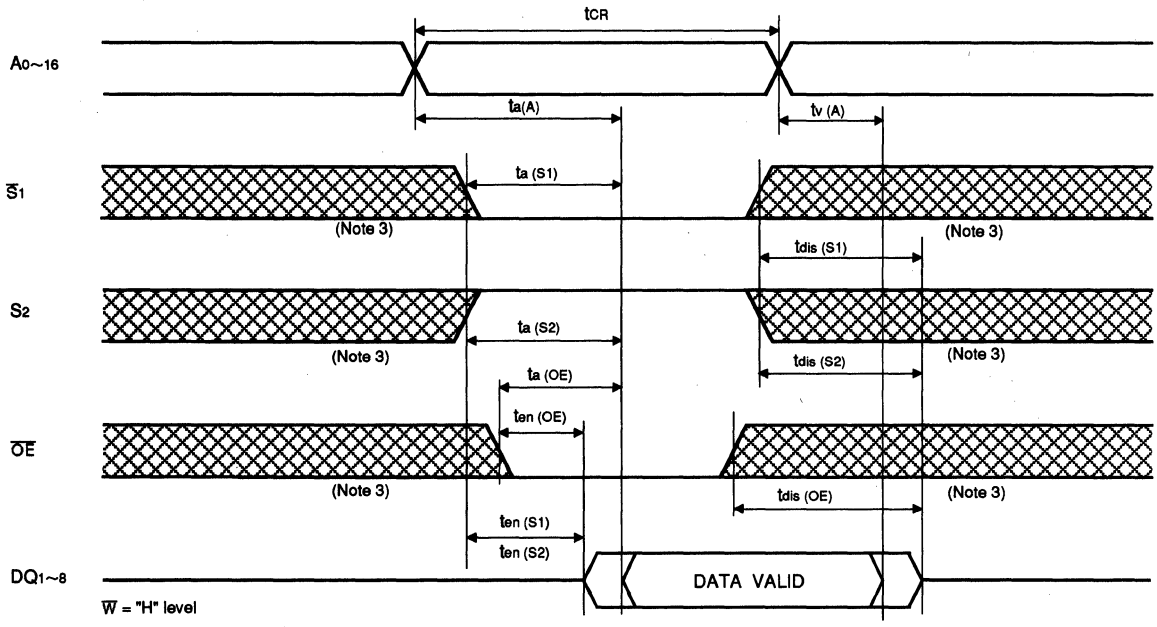
Symbol	Parameter	Limits								Unit
		-70VL,VLL		-10VL,VLL		-12VL,VLL		-15VL,VLL		
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{CR}	Read cycle time	70		100		120		150		ns
$t_{a(A)}$	Address access time		70		100		120		150	ns
$t_{a(S1)}$	Chip select 1 access time		70		100		120		150	ns
$t_{a(S2)}$	Chip select 2 access time		70		100		120		150	ns
$t_{a(OE)}$	Output enable access time		35		50		60		75	ns
$t_{dis(S1)}$	Output disable time after $\overline{S_1}$ high		25		35		40		50	ns
$t_{dis(S2)}$	Output disable time after S_2 low		25		35		40		50	ns
$t_{dis(OE)}$	Output disable time after $\overline{OE}$ high		25		35		40		50	ns
$t_{en(S1)}$	Output enable time after $\overline{S_1}$ low	10		10		10		10		ns
$t_{en(S2)}$	Output enable time after S_2 high	10		10		10		10		ns
$t_{en(OE)}$	Output enable time after $\overline{OE}$ low	5		5		5		5		ns
$t_{V(A)}$	Data valid time after address	10		10		10		10		ns

(3) WRITE CYCLE

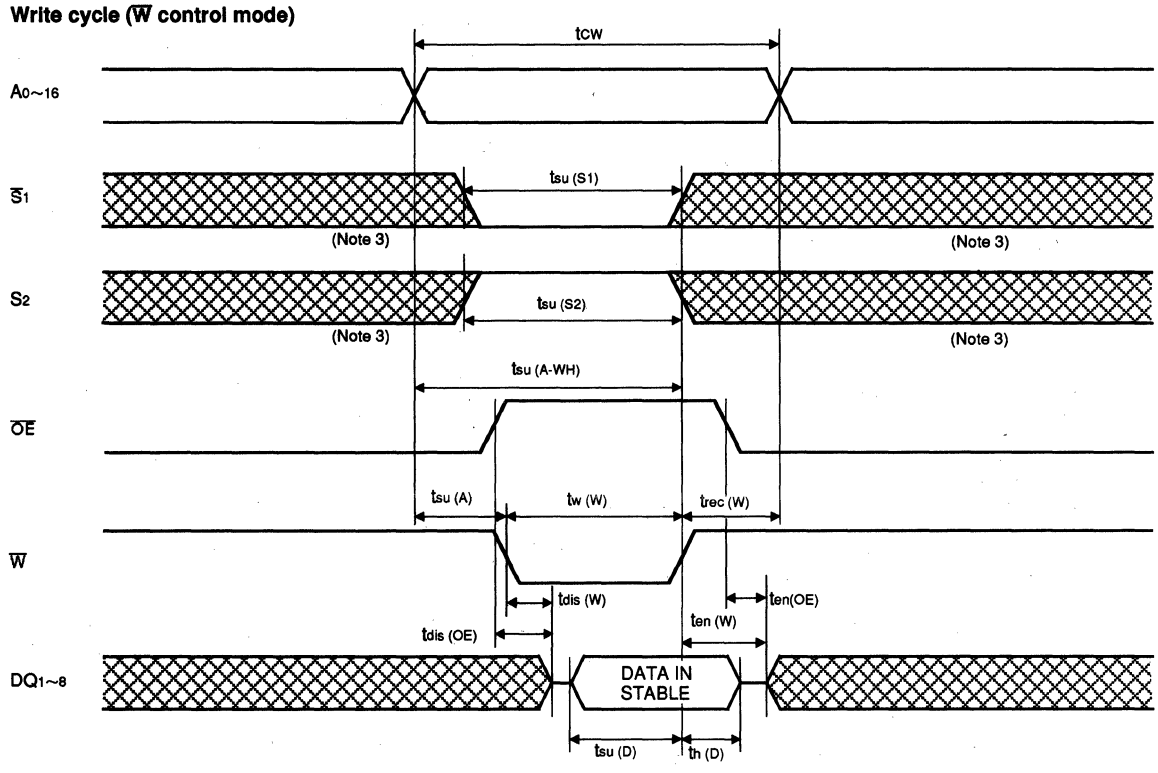
Symbol	Parameter	Limits								Unit
		-70VL,VLL		-10VL,VLL		-12VL,VLL		-15VL,VLL		
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{CW}	Write cycle time	70		100		120		150		ns
$t_{w(W)}$	Write pulse width	55		75		85		100		ns
$t_{su(A)}$	Address setup time	0		0		0		0		ns
$t_{su(A-WH)}$	Address setup time with respect to $\overline{W}$	65		85		100		120		ns
$t_{su(S1)}$	Chip select 1 setup time	65		85		100		120		ns
$t_{su(S2)}$	Chip select 2 setup time	65		85		100		120		ns
$t_{su(D)}$	Data setup time	30		40		45		50		ns
$t_{h(D)}$	Data hold time	0		0		0		0		ns
$t_{rec(W)}$	Write recovery time	0		0		0		0		ns
$t_{dis(W)}$	Output disable time from $\overline{W}$ low		25		35		40		50	ns
$t_{dis(OE)}$	Output disable time from $\overline{OE}$ high		25		35		40		50	ns
$t_{en(W)}$	Output enable time from $\overline{W}$ high	5		5		5		5		ns
$t_{en(OE)}$	Output enable time from $\overline{OE}$ low	5		5		5		5		ns

(4) TIMING DIAGRAMS

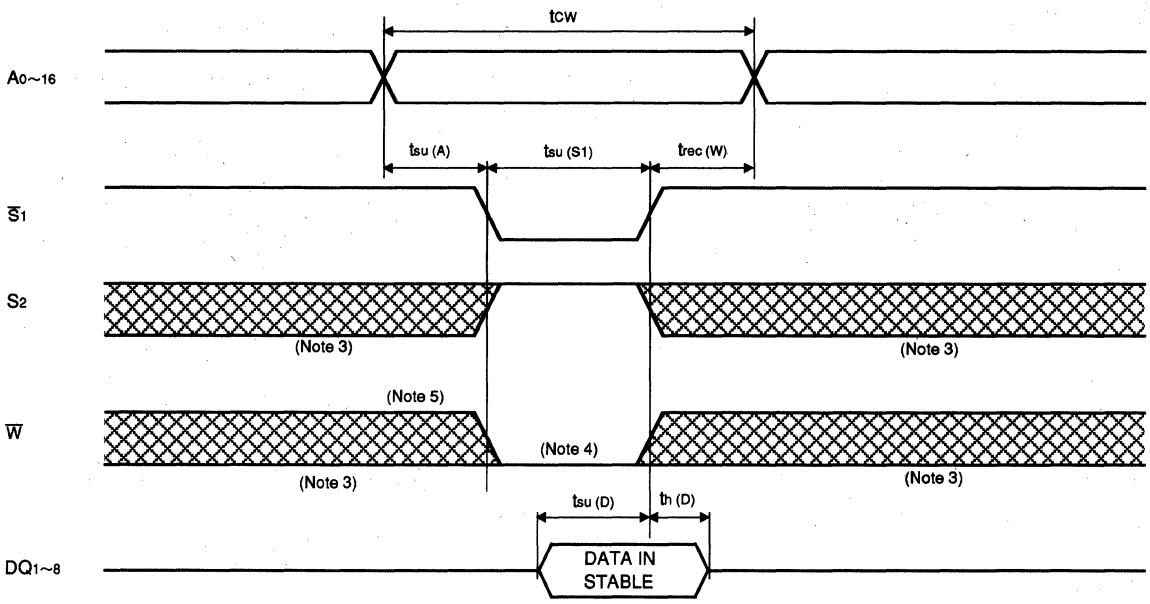
Read cycle



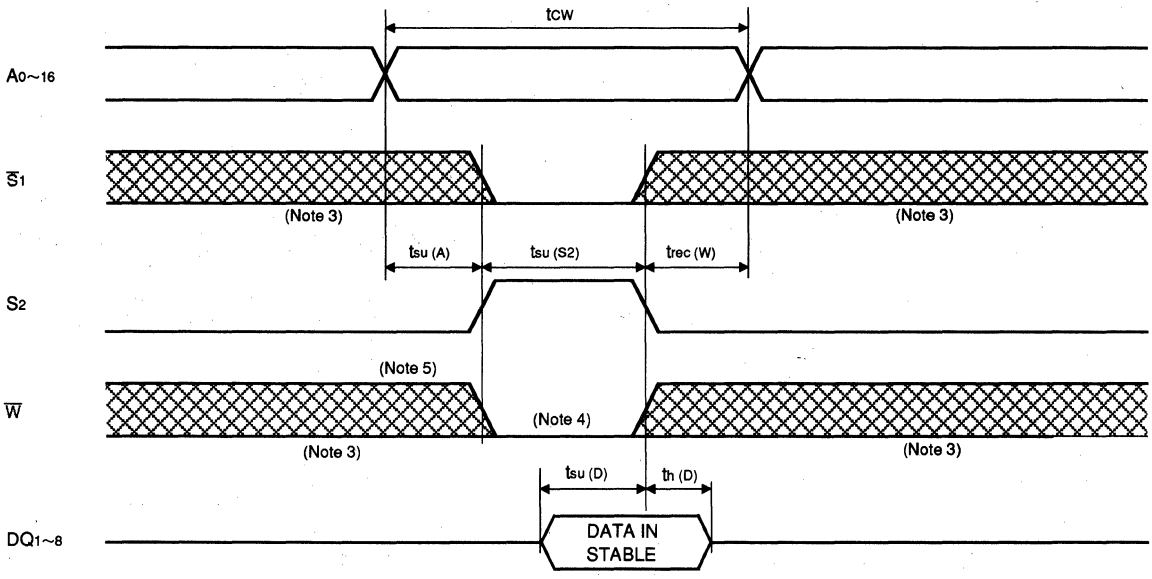
Write cycle (W control mode)



Write cycle ($\overline{S}_1$ control mode)



Write cycle (S_2 control mode)



Note 3: Hatching indicates the state is "don't care".
4: Writing is executed while S_2 high overlaps $\overline{S}_1$ and $\overline{W}$ low.
5: When the falling edge of $\overline{W}$ is simultaneously or prior to the falling edge of $\overline{S}_1$ or rising edge of S_2, the outputs are maintained in the high impedance state.
6: Don't apply inverted phase signal externally when DQ pin is output mode.

POWER DOWN CHARACTERISTICS

(1) ELECTRICAL CHARACTERISTICS (Ta = 0~70℃, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits Min	Limits Typ	Limits Max	Unit
$V_{CC\ (PD)}$	Power down supply voltage			2			V
$V_{I\ (\overline{S}1)}$	Chip select input $\overline{S}_1$	3.6V ≦ $V_{CC\ (PD)}$		2.2			V
		2.2V ≦ $V_{CC\ (PD)}$ ≦ 3.6V		2.0			
		2V ≦ $V_{CC\ (PD)}$ ≦ 2.2V			$V_{CC(PD)}$		
$V_{I\ (S2)}$	Chip select input S_2	4.5V≦$V_{CC\ (PD)}$				0.8	V
		$V_{CC\ (PD)}$ <4.5V				0.2	
$I_{CC\ (PD)}$	Power down supply current	V_{CC} = 3V, S_2≦0.2V or $\overline{S}_1$≧V_{CC} −0.2V, S_2≧V_{CC} −0.2V	-L			50	μA
			-LL		0.3	10 (Note 7)	

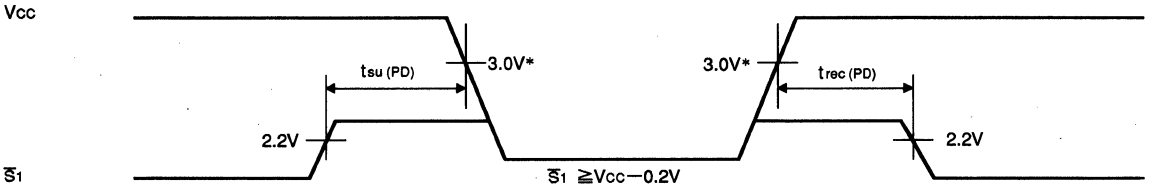
Note7: $I_{CC\ (PD)}$ = 1 μA in case of Ta = 25℃

(2) TIMING REQUIREMENTS (Ta = 0~70℃, unless otherwise noted)

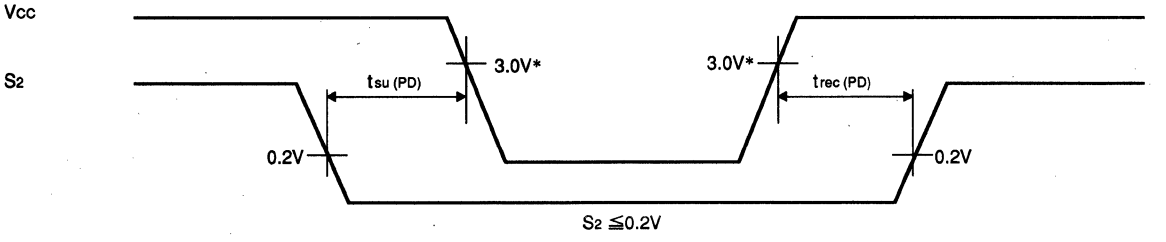
Symbol	Parameter	Test conditions	Limits Min	Limits Typ	Limits Max	Unit
$t_{su\ (PD)}$	Power down set up time		0			ns
$t_{rec\ (PD)}$	Power down recovery time		5			ms

(3) POWER DOWN CHARACTERISTICS

$\overline{S}_1$ control mode



S_2 control mode



*Note 2.7V(-12VL,-12VLL,-15VL,-15VLL)

M5M51016ATP,RT-10VL,-10VLL

1048576-BIT (65536-WORD BY 16-BIT) CMOS STATIC RAM

DESCRIPTION

The M5M51016ATP, RT are a 1048576-bit CMOS static RAM organized as 65536-word by 16-bit which are fabricated using high-performance triple polysilicon CMOS technology. The use of resistive load NMOS cells and CMOS periphery result in a high density and low power static RAM.

They are low stand-by current and low operation current and ideal for the battery back-up application.

The M5M51016ATP, RT are packaged in a 44-pin thin small outline package which is a high reliability and high density surface mount device (SMD). Two types of devices are available. M5M 51016ATP (normal lead bend type package), M5M51016ART (reverse lead bend type package). Using both types of devices, it becomes very easy to design a printed circuit board.

FEATURES

Type name	Access time (max)	Power supply current	
		Active (max)	Stand-by (max)
M5M51016ATP,RT-10VL	100ns	60mA	60μA (Vcc=3.6V)
M5M51016ATP,RT-10VLL	100ns		12μA (Vcc=3.6V) 0.3μA (Vcc=3.0V typ.)

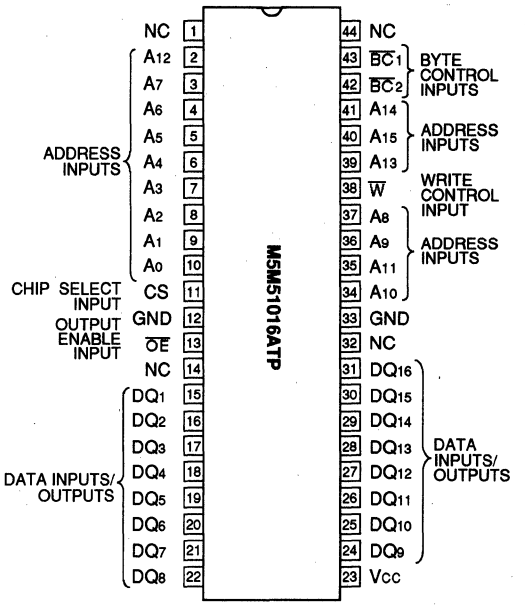
- Single +3.0~3.6V power supply
- Low stand-by current 0.3μA(typ.)
- Directly TTL compatible : All inputs and ouputs
- Easy memory expansion and power down by CS,$\overline{BC}_1$ & $\overline{BC}_2$
- Data hold on + 2V power supply
- Three-state outputs : OR-tie capability
- $\overline{OE}$ prevents data contention in the I/O bus
- Common data I/O
- Package

  M5M51016ATP,RT·····44pin 400mil TSOP(II)

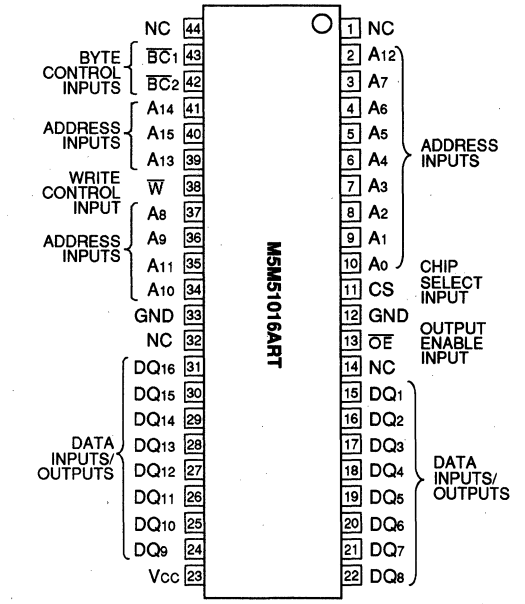
APPLICATION

Small capacity memory units

PIN CONFIGURATION (TOP VIEW)



Outline 44P3W-H (400mil TSOP Normal Bend)



Outline 44P3W-J (400mil TSOP Reverse Bend)

NC : NO CONNECTION

FUNCTION

The operation mode of the M5M51016A series are determined by a combination of the device control inputs $\overline{BC}_1$, $\overline{BC}_2$, CS, $\overline{W}$ and $\overline{OE}$. Each mode is summarized in the function table.

A write cycle is executed whenever the low level $\overline{W}$ overlaps with the low level $\overline{BC}_1$ and/or $\overline{BC}_2$ and the high level CS. The address must be set up before the write cycle and must be stable during the entire cycle. The data is latched into a cell on the trailing edge of $\overline{W}$, $\overline{BC}_1$, $\overline{BC}_2$ or CS, whichever occurs first, requiring the set-up and hold time relative to these edge to be maintained. The output enable input $\overline{OE}$ directly controls the output stage. Setting the $\overline{OE}$ at a high level, the output stage is in a high-impedance state, and the databus contention problem in the write cycle is eliminated.

A read cycle is executed by setting $\overline{W}$ at a high level and $\overline{OE}$ at a low level while $\overline{BC}_1$ and/or $\overline{BC}_2$ and CS are in an active state. ($\overline{BC}_1$ and/or $\overline{BC}_2$=L,CS=H)

When setting $\overline{BC}_1$ at a high level and the other pins are in an active state, upper-Byte are in a selectable mode in which both reading and writing are enabled, and lower-Byte are in a non-selectable mode. And when setting $\overline{BC}_2$ at a high level and the other pins are in an active state, lower-Byte are in a selectable mode and upper-Byte are in a non-selectable mode.

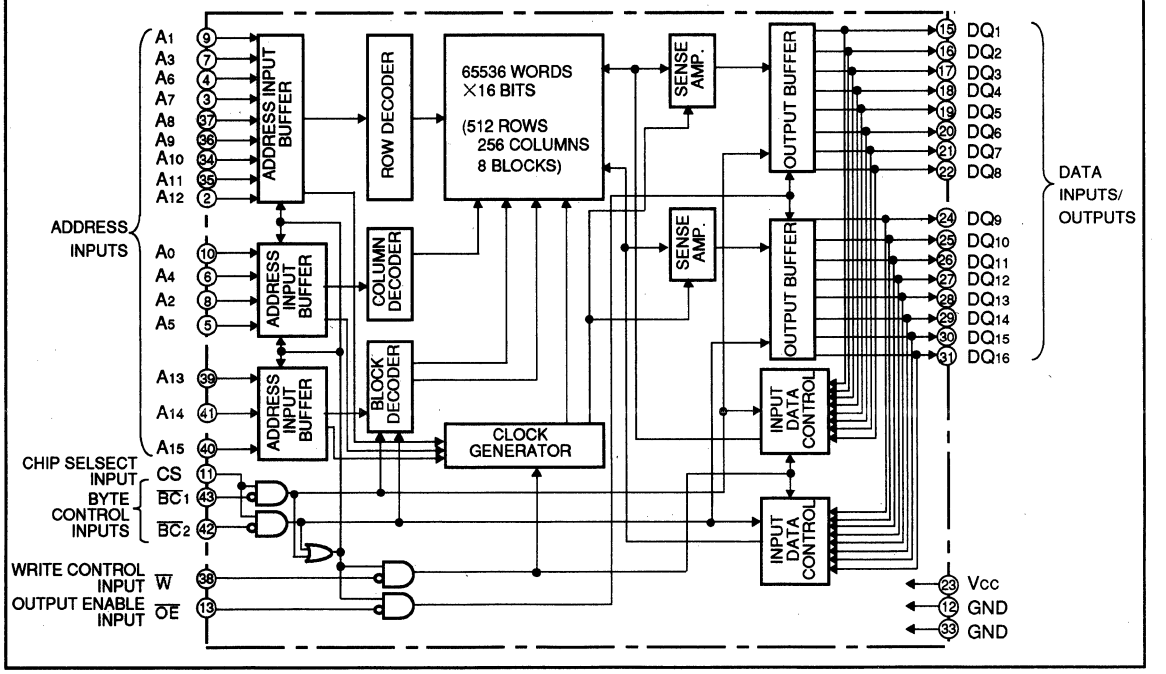
When setting $\overline{BC}_1$ and $\overline{BC}_2$ at a high level or CS at a low level, the chips are in a non-selectable mode in which both reading and writing are disabled. In this mode, the output stage is in a high-impedance state, allowing OR-tie with other chips and memory expansion by $\overline{BC}_1$, $\overline{BC}_2$ and CS. The power supply current is reduced as low as the stand-by current which is specified as I_{CC3} or I_{CC4}, and the memory data can be held at +2V power supply, enabling battery back-up operation during power failure or power-down operation in the non-selected mode.

FUNCTION TABLE

CS	$\overline{BC}_1$	$\overline{BC}_2$	$\overline{W}$	$\overline{OE}$	Mode	$DQ_{1\sim8}$	$DQ_{9\sim16}$	Icc
L	X	X	X	X	Non selection	High-Z	High-Z	Stand-by
X	H	H	X	X	Non selection	High-Z	High-Z	Stand-by
H	H	L	L	X	Upper-Byte Write	High-Z	Din	Active
H	H	L	H	L	Upper-Byte Read	High-Z	Dout	Active
H	H	L	H	H	———	High-Z	High-Z	Active
H	L	H	L	X	Lower-Byte Write	Din	High-Z	Active
H	L	H	H	L	Lower-Byte Read	Dout	High-Z	Active
H	L	H	H	H	———	High-Z	High-Z	Active
H	L	L	L	X	Word Write	Din	Din	Active
H	L	L	H	L	Word Read	Dout	Dout	Active
H	L	L	H	H	———	High-Z	High-Z	Active

(High-Z=High-impedance)

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to GND	−0.3～7	V
V_I	Input voltage		−0.3*～V_{CC} + 0.3	V
V_O	Output voltage		0～V_{CC}	V
P_d	Power dissipation	Ta = 25℃	1	W
T_{opr}	Operating temperature		0～70	℃
T_{stg}	Storage temperature		−65～150	℃

* −3.0V in case of AC(Pulse width≦50ns)

DC ELECTRICAL CHARACTERISTICS (Ta = 0～70℃, Vcc = 3.0V~3.6V, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits Min	Limits Typ	Limits Max	Unit
V_{IH}	High-level input voltage			2.0		V_{CC}+0.3V	V
V_{IL}	Low-level input voltage			−0.3*		0.6	V
V_{OH1}	High-level output voltage 1	I_{OH} = −1mA		2.4			V
V_{OH2}	High-level output voltage 2	I_{OH} = −0.1mA		V_{CC} − 0.5V			V
V_{OL}	Low-level output voltage	I_{OL} = 2mA				0.4	V
I_I	Input current	V_I = 0～V_{CC}				±1	μA
I_O	Output current in off-state	$\overline{BC}_1$ and $\overline{BC}_2$ =V_{IH} or CS=V_{IL} or $\overline{OE}$=V_{IH}, $V_{I/O}$=0～V_{CC}				±1	μA
I_{CC1}	Active supply current (Min cycle)	$\overline{BC}_1$ and $\overline{BC}_2$ = V_{IL}, CS=V_{IH} other inputs = V_{IH} or V_{IL} Output-open (duty 100%)			35	60	mA
I_{CC2}	Active supply current (1MHz)				8	12	mA
I_{CC3}	Stand-by current	1)CS≦0.2V, other inputs=0~V_{CC} 2)$\overline{BC}_1$ and $\overline{BC}_2$≧ V_{CC}− 0.2V CS≧V_{CC}− 0.2V other inputs = 0～V_{CC}	-VL			60	μA
			-VLL			12	μA
I_{CC4}	Stand-by current	$\overline{BC}_1$ and $\overline{BC}_2$ =V_{IH} or CS= V_{IL} other inputs = 0～V_{CC}				0.33	mA

* −3.0V in case of AC(Pulse width≦50ns)

CAPACITANCE (Ta = 0～70℃, Vcc = 3.0V～3.6 unless otherwise noted)

Symbol	Parameter	Test conditions	Limits Min	Limits Typ	Limits Max	Unit
C_I	Input capacitance	V_I = GND, V_I = 25mVrms, f = 1MHz			6	pF
C_O	Output capacitance	V_O = GND,V_O = 25mVrms, f = 1MHz			8	pF

Note 1: Direction for current flowing into an IC is positive (no mark).
2: Typical value is Vcc=5V, Ta = 25℃.

AC ELECTRICAL CHARACTERISTICS (Ta = 0～70℃, Vcc = 3.0V～3.6V, unless otherwise noted)

(1) MEASUREMENT CONDITIONS

Input pulse level ····· V_{IH} = 2.2V, V_{IL} = 0.4V
Input rise and fall time ····· 5ns
Reference level ····· V_{OH} = V_{OL} = 1.5V
Output loads ····· Fig.1, C_L = 30pF
C_L = 5pF (for t_{en}, t_{dis})
Transition is measured ±500mV
from steady state voltage. (for t_{en}, t_{dis})

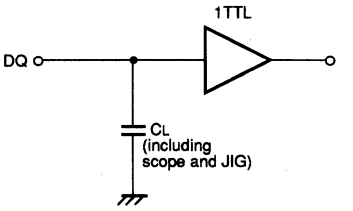


Fig.1 Output load

(2) READ CYCLE

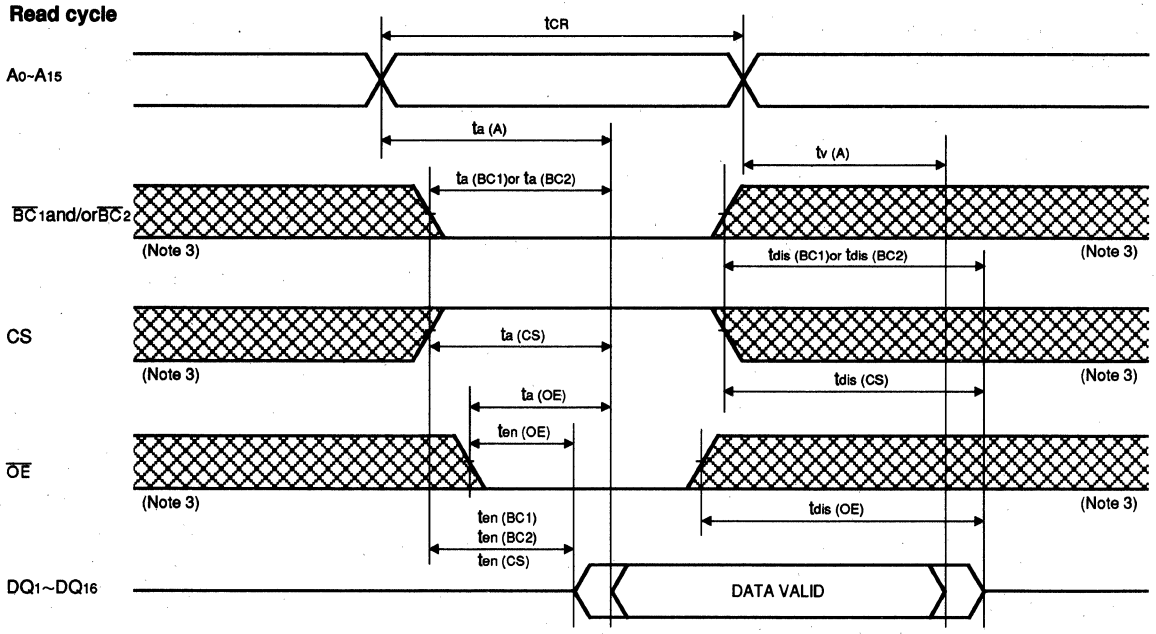
Symbol	Parameter	Limits M5M51016A-10VL,-10VLL Min	Limits M5M51016A-10VL,-10VLL Max	Unit
t_{CR}	Read cycle time	100		ns
$t_{a(A)}$	Address access time		100	ns
$t_{a(BC1)}$	Byte controle 1 access time		100	ns
$t_{a(BC2)}$	Byte controle 2 access time		100	ns
$t_{a(CS)}$	Chip select access time		100	ns
$t_{a(OE)}$	Output enable access time		50	ns
$t_{dis(BC1)}$	Output disable time after $\overline{BC}_1$ high		35	ns
$t_{dis(BC2)}$	Output disable time after $\overline{BC}_2$ high		35	ns
$t_{dis(CS)}$	Output disable time after CS low		35	ns
$t_{dis(OE)}$	Output disable time after $\overline{OE}$ high		35	ns
$t_{en(BC1)}$	Output enable time after $\overline{BC}_1$ low	10		ns
$t_{en(BC2)}$	Output enable time after $\overline{BC}_2$ low	10		ns
$t_{en(CS)}$	Output enable time after CS high	10		ns
$t_{en(OE)}$	Output enable time after $\overline{OE}$ low	5		ns
$t_{v(A)}$	Data valid time after address	10		ns

(3) WRITE CYCLE

Symbol	Parameter	Limits M5M51016A-10VL,-10VLL Min	Limits M5M51016A-10VL,-10VLL Max	Unit
t_{CW}	Write cycle time	100		ns
$t_{w(W)}$	Write pulse width	75		ns
$t_{su(A)}$	Address setup time	0		ns
$t_{su(A-WH)}$	Address setup time with respect to $\overline{W}$	85		ns
$t_{su(BC1)}$	Byte controle 1 setup time	85		ns
$t_{su(BC2)}$	Byte controle 2 setup time	85		ns
$t_{su(CS)}$	Chip select setup time	85		ns
$t_{su(D)}$	Data setup time	40		ns
$t_{h(D)}$	Data hold time	0		ns
$t_{rec(W)}$	Write recovery time	0		ns
$t_{dis(W)}$	Output disable time from $\overline{W}$ low		35	ns
$t_{dis(OE)}$	Output disable time from $\overline{OE}$ high		35	ns
$t_{en(W)}$	Output enable time from $\overline{W}$ high	5		ns
$t_{en(OE)}$	Output enable time from $\overline{OE}$ low	5		ns

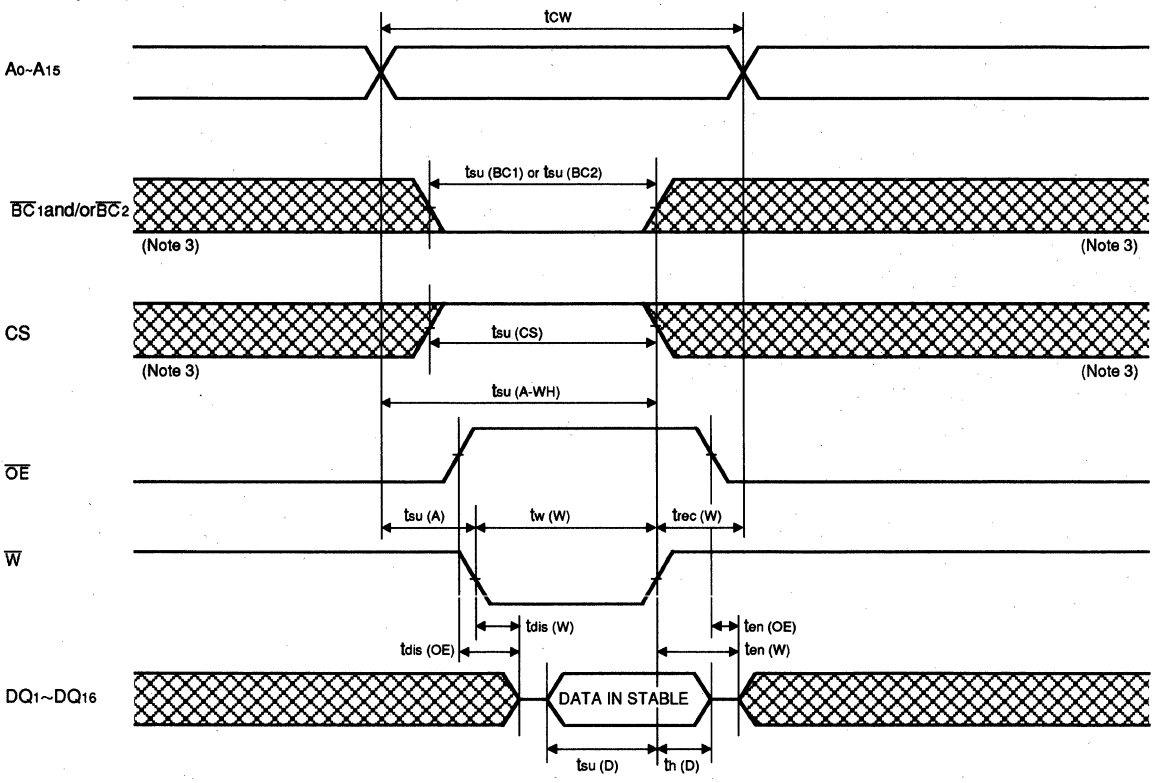
(4) TIMING DIAGRAMS

Read cycle

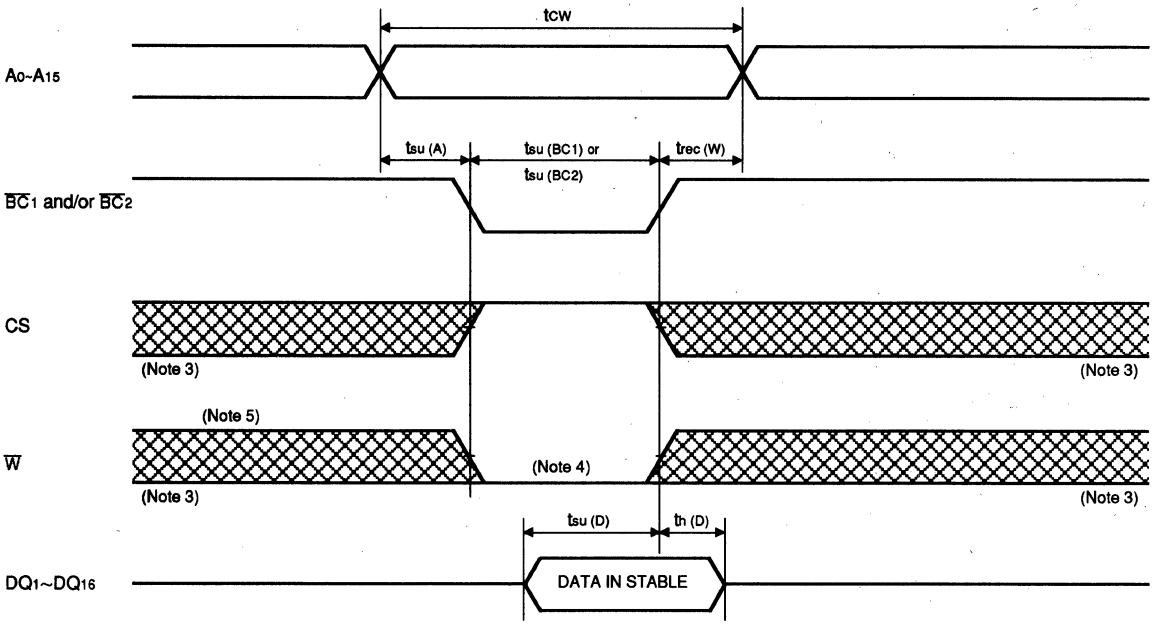


W = "H" level

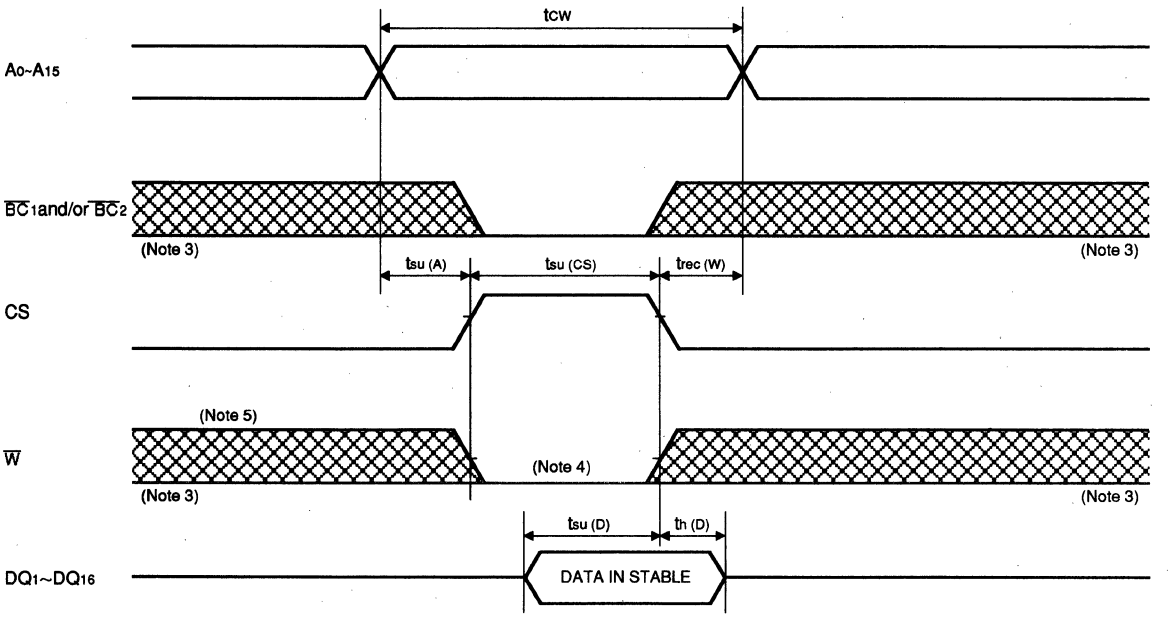
Write cycle (W control mode)



Write cycle ($\overline{BC}$ control mode)



Write cycle (CS control mode)



Note 3 : Hatching indicates the state is "don't care".
4 : Writing is executed while CS high overlaps $\overline{BC}1$ and/or $\overline{BC}2$ low and $\overline{W}$ low.
5 : When the falling edge of $\overline{W}$ is simultaneously or prior to the falling edge of $\overline{BC}1$ and/or $\overline{BC}2$ or rising edge of CS , the outputs are maintained in the high impedance state.
6 : Don't apply inverted phase signal externally when DQ pin is output mode.

POWER DOWN CHARACTERISTICS

(1) ELECTRICAL CHARACTERISTICS (Ta = 0~70℃, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ	Max	
$V_{CC\ (PD)}$	Power down supply voltage			2			V
$V_{I\ (BC)}$	Byte control input $\overline{BC}_1$ & $\overline{BC}_2$			2.0			V
$V_{I\ (CS)}$	Chip select input CS	$3.0V \leqq V_{CC\ (PD)}$				0.6	V
		$V_{CC\ (PD)} < 3.0V$				0.2	
$I_{CC\ (PD)}$	Power down supply current	V_{CC} = 3V 1)CS≦0.2V other inputs=0~3V	-VL			50	μA
		2)$\overline{BC}_1$ & $\overline{BC}_2 \geqq V_{CC} - 0.2V$ CS≧Vcc – 0.2V,other inputs=0~3V	-VLL		0.3	10 (Note 7)	

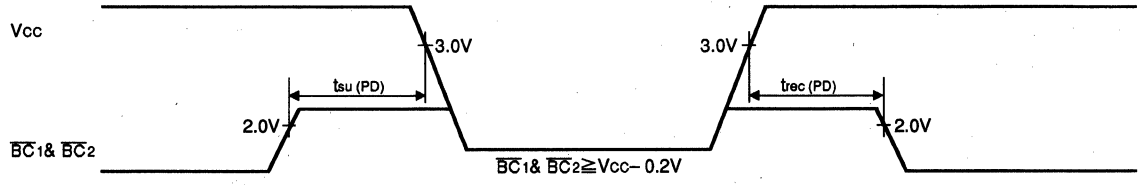
Note 7. $I_{CC\ (PD)}$ = 1 μA in case of Ta = 25℃

(2) TIMING REQUIREMENTS (Ta = 0~70℃, unless otherwise noted)

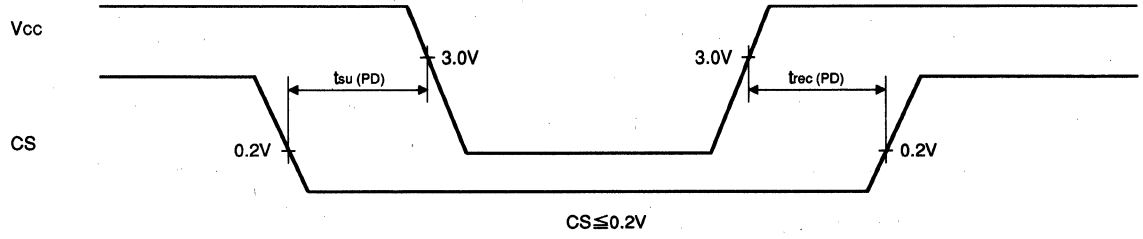
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{su\ (PD)}$	Power down set up time		0			ns
$t_{rec\ (PD)}$	Power down recovery time		5			ms

(3) POWER DOWN CHARACTERISTICS

$\overline{BC}$ control mode



CS control mode



M5M51016ATP,RT-15VL,-15VLL

1048576-BIT (65536-WORD BY 16-BIT) CMOS STATIC RAM

DESCRIPTION

The M5M51016ATP, RT are a 1048576-bit CMOS static RAM organized as 65536-word by 16-bit which are fabricated using high-performance triple polysilicon CMOS technology. The use of resistive load NMOS cells and CMOS periphery result in a high density and low power static RAM.

They are low stand-by current and low operation current and ideal for the battery back-up application.

The M5M51016ATP, RT are packaged in a 44-pin thin small outline package which is a high reliability and high density surface mount device (SMD). Two types of devices are available. M5M 51016ATP (normal lead bend type package), M5M51016ART (reverse lead bend type package). Using both types of devices, it becomes very easy to design a printed circuit board.

FEATURES

Type name	Access time (max)	Power supply current	
		Active (max)	Stand-by (max)
M5M51016ATP,RT-15VL	150ns	80mA (Vcc=5.5V)	55μA (Vcc=3.3V)
M5M51016ATP,RT-15VLL	150ns	30mA (Vcc=3.3V)	11μA (Vcc=3.3V) 0.3μA (Vcc=3.0V typ.)

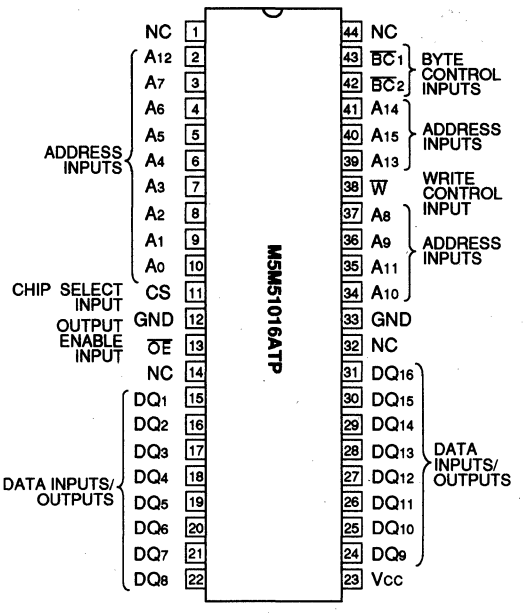
- Single +2.7~5.5V power supply
- Low stand-by current 0.3μA(typ.)
- Directly TTL compatible : All inputs and ouputs
- Easy memory expansion and power down by CS,$\overline{BC}_1$ & $\overline{BC}_2$
- Data hold on + 2V power supply
- Three-state outputs : OR-tie capability
- $\overline{OE}$ prevents data contention in the I/O bus
- Common data I/O
- Package

  M5M51016ATP,RT·····44pin 400mil TSOP(II)

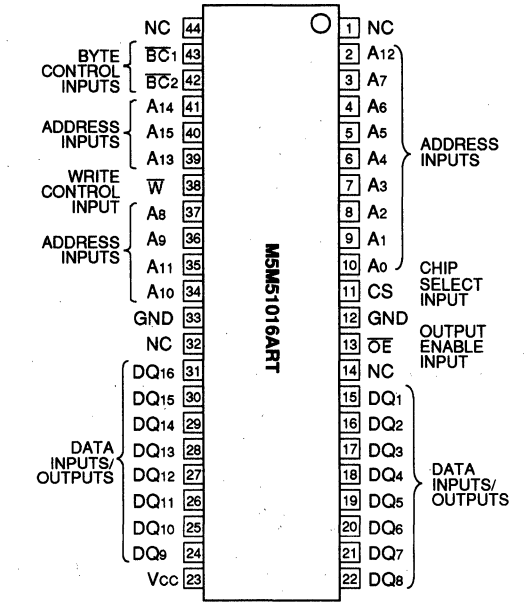
APPLICATION

Small capacity memory units

PIN CONFIGURATION (TOP VIEW)



Outline 44P3W-H (400mil TSOP Normal Bend)



Outline 44P3W-J (400mil TSOP Reverse Bend)

NC : NO CONNECTION

FUNCTION

The operation mode of the M5M51016A series are determined by a combination of the device control inputs $\overline{BC}_1$, $\overline{BC}_2$, CS, $\overline{W}$ and $\overline{OE}$. Each mode is summarized in the function table.

A write cycle is executed whenever the low level $\overline{W}$ overlaps with the low level $\overline{BC}_1$ and/or $\overline{BC}_2$ and the high level CS. The address must be set up before the write cycle and must be stable during the entire cycle. The data is latched into a cell on the trailing edge of $\overline{W}$, $\overline{BC}_1$, $\overline{BC}_2$ or CS, whichever occurs first, requiring the set-up and hold time relative to these edge to be maintained. The output enable input $\overline{OE}$ directly controls the output stage. Setting the $\overline{OE}$ at a high level, the output stage is in a high-impedance state, and the databus contention problem in the write cycle is eliminated.

A read cycle is executed by setting $\overline{W}$ at a high level and $\overline{OE}$ at a low level while $\overline{BC}_1$ and/or $\overline{BC}_2$ and CS are in an active state. ($\overline{BC}_1$ and/or $\overline{BC}_2$=L,CS=H)

When setting $\overline{BC}_1$ at a high level and the other pins are in an active state, upper-Byte are in a selectable mode in which both reading and writing are enabled, and lower-Byte are in a non-selectable mode. And when setting $\overline{BC}_2$ at a high level and the other pins are in an active state, lower-Byte are in a selectable mode and upper-Byte are in a non-selectable mode.

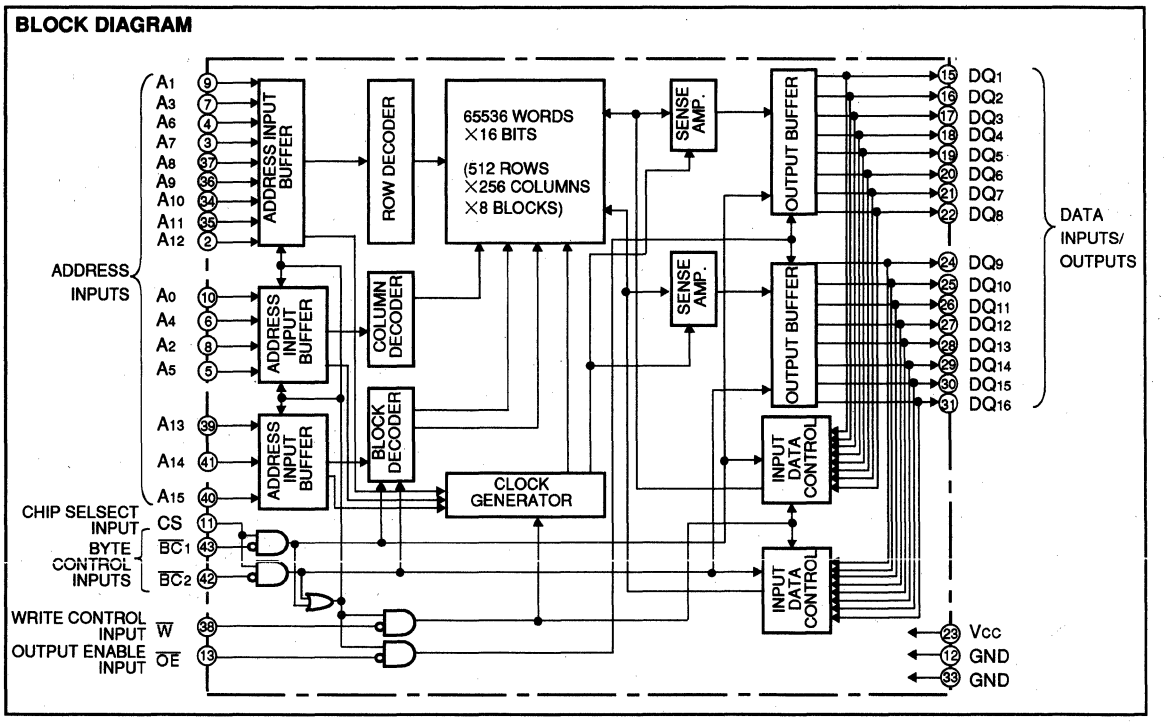
When setting $\overline{BC}_1$ and $\overline{BC}_2$ at a high level or CS at a low level, the chips are in a non-selectable mode in which both reading and writing are disabled. In this mode, the output stage is in a high-impedance state, allowing OR-tie with other chips and memory expansion by $\overline{BC}_1$, $\overline{BC}_2$ and CS. The power supply current is reduced as low as the stand-by current which is specified as I_{CC3} or I_{CC4}, and the memory data can be held at +2V power supply, enabling battery back-up operation during power failure or power-down operation in the non-selected mode.

FUNCTION TABLE

CS	$\overline{BC}_1$	$\overline{BC}_2$	$\overline{W}$	$\overline{OE}$	Mode	$DQ_{1\sim8}$	$DQ_{9\sim16}$	Icc
L	X	X	X	X	Non selection	High-Z	High-Z	Stand-by
X	H	H	X	X	Non selection	High-Z	High-Z	Stand-by
H	H	L	L	X	Upper-Byte Write	High-Z	Din	Active
H	H	L	H	L	Upper-Byte Read	High-Z	Dout	Active
H	H	L	H	H	———	High-Z	High-Z	Active
H	L	H	L	X	Lower-Byte Write	Din	High-Z	Active
H	L	H	H	L	Lower-Byte Read	Dout	High-Z	Active
H	L	H	H	H	———	High-Z	High-Z	Active
H	L	L	L	X	Word Write	Din	Din	Active
H	L	L	H	L	Word Read	Dout	Dout	Active
H	L	L	H	H	———	High-Z	High-Z	Active

(High-Z=High-impedance)

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to GND	−0.3～7	V
V_I	Input voltage		−0.3*～Vcc + 0.3	V
V_O	Output voltage		0～Vcc	V
P_d	Power dissipation	Ta = 25℃	1	W
T_{opr}	Operating temperature		0～70	℃
T_{stg}	Storage temperature		−65～150	℃

* −3.0V in case of AC(Pulse width≦50ns)

DC ELECTRICAL CHARACTERISTICS (Ta = 0～70℃, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits 1 (Vcc=5V±10%)			Limits 2 Vcc=3V±10%			Unit
				Min	Typ	Max	Min	Typ	Max	
V_{IH}	High-level input voltage			2.2		Vcc+0.3V	2.0		Vcc+0.3V	V
V_{IL}	Low-level input voltage			−0.3*		0.8	−0.3*		0.6	V
V_{OH1}	High-level output voltage 1	I_{OH} = −1mA		2.4			2.4			V
V_{OH2}	High-level output voltage 2	I_{OH} = −0.1mA		Vcc−0.5V			Vcc−0.5V			V
V_{OL}	Low-level output voltage	I_{OL} = 2mA				0.4			0.4	V
I_I	Input current	V_I = 0～Vcc				±1			±1	μA
I_O	Output current in off-state	$\overline{BC}_1$ and $\overline{BC}_2$ =V_{IH} or CS=V_{IL} or $\overline{OE}$=V_{IH}, $V_{I/O}$=0～Vcc				±1			±1	μA
I_{CC1}	Active supply current (Min cycle)	$\overline{BC}_1$ and $\overline{BC}_2$ = V_{IL}, CS=V_{IH} other inputs = V_{IH} or V_{IL} Output-open (duty 100%)			50	80		15	30	mA
I_{CC2}	Active supply current (1MHz)				12	25		5	10	mA
I_{CC3}	Stand-by current	1)CS≦0.2V, other inputs=0~Vcc 2)$\overline{BC}_1$ and $\overline{BC}_2$≧Vcc− 0.2V CS≧Vcc− 0.2V other inputs = 0～Vcc	-VL			100			55	μA
			-VLL			20			11	μA
I_{CC4}	Stand-by current	$\overline{BC}_1$ and $\overline{BC}_2$ =V_{IH} or CS= V_{IL} other inputs = 0～Vcc				3			0.3	mA

* −3.0V in case of AC(Pulse width≦50ns)

CAPACITANCE (Ta = 0～70℃, Vcc = 2.7V～5.5V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
C_I	Input capacitance	V_I = GND, V_I = 25mVrms, f = 1MHz			6	pF
C_O	Output capacitance	V_O = GND,V_O = 25mVrms, f = 1MHz			8	pF

Note 1: Direction for current flowing into an IC is positive (no mark).
2: Typical value is Vcc=5V, Ta = 25℃.

AC ELECTRICAL CHARACTERISTICS (Ta = 0~70℃, Vcc = 2.7V~5.5V, unless otherwise noted)

(1) MEASUREMENT CONDITIONS

Input pulse level ..... V_{IH} = 2.4V, V_{IL} = 0.6V(V_{CC}=5V±10%)

V_{IH} = 2.2V, V_{IL} = 0.4V(V_{CC}=3V±10%)

Input rise and fall time 5ns

Reference level ..... V_{OH} = V_{OL} = 1.5V

Output loads ..... Fig.1, C_L = 100pF

C_L = 5pF (for t_{en}, t_{dis})

Transition is measured ±500mV from steady state voltage. (for t_{en}, t_{dis})

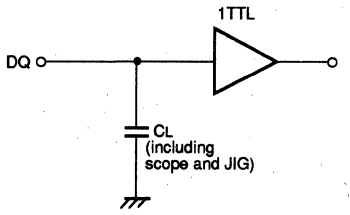


Fig.1 Output load

(2) READ CYCLE

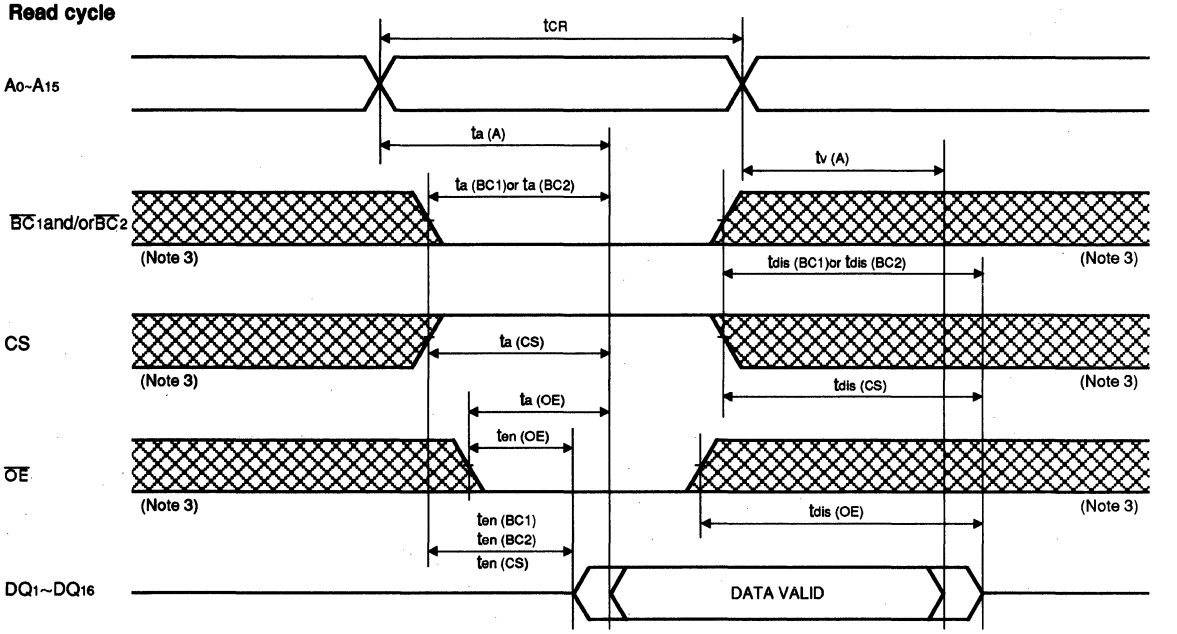
Symbol	Parameter	Limits M5M51016A-15VL,-15VLL		Unit
		Min	Max	
t_{CR}	Read cycle time	150		ns
$t_{a(A)}$	Address access time		150	ns
$t_{a(BC1)}$	Byte controle 1 access time		150	ns
$t_{a(BC2)}$	Byte controle 2 access time		150	ns
$t_{a(CS)}$	Chip select access time		150	ns
$t_{a(OE)}$	Output enable access time		75	ns
$t_{dis(BC1)}$	Output disable time after $\overline{BC}_1$ high		50	ns
$t_{dis(BC2)}$	Output disable time after $\overline{BC}_2$ high		50	ns
$t_{dis(CS)}$	Output disable time after CS low		50	ns
$t_{dis(OE)}$	Output disable time after $\overline{OE}$ high		50	ns
$t_{en(BC1)}$	Output enable time after $\overline{BC}_1$ low	10		ns
$t_{en(BC2)}$	Output enable time after $\overline{BC}_2$ low	10		ns
$t_{en(CS)}$	Output enable time after CS high	10		ns
$t_{en(OE)}$	Output enable time after $\overline{OE}$ low	5		ns
$t_{v(A)}$	Data valid time after address	10		ns

(3) WRITE CYCLE

Symbol	Parameter	Limits M5M51016A-15VL,-15VLL		Unit
		Min	Max	
t_{CW}	Write cycle time	150		ns
$t_{w(W)}$	Write pulse width	100		ns
$t_{su(A)}$	Address setup time	0		ns
$t_{su(A-WH)}$	Address setup time with respect to $\overline{W}$	120		ns
$t_{su(BC1)}$	Byte controle 1 setup time	120		ns
$t_{su(BC2)}$	Byte controle 2 setup time	120		ns
$t_{su(CS)}$	Chip select setup time	120		ns
$t_{su(D)}$	Data setup time	50		ns
$t_{h(D)}$	Data hold time	0		ns
$t_{rec(W)}$	Write recovery time	0		ns
$t_{dis(W)}$	Output disable time from $\overline{W}$ low		50	ns
$t_{dis(OE)}$	Output disable time from $\overline{OE}$ high		50	ns
$t_{en(W)}$	Output enable time from $\overline{W}$ high	5		ns
$t_{en(OE)}$	Output enable time from $\overline{OE}$ low	5		ns

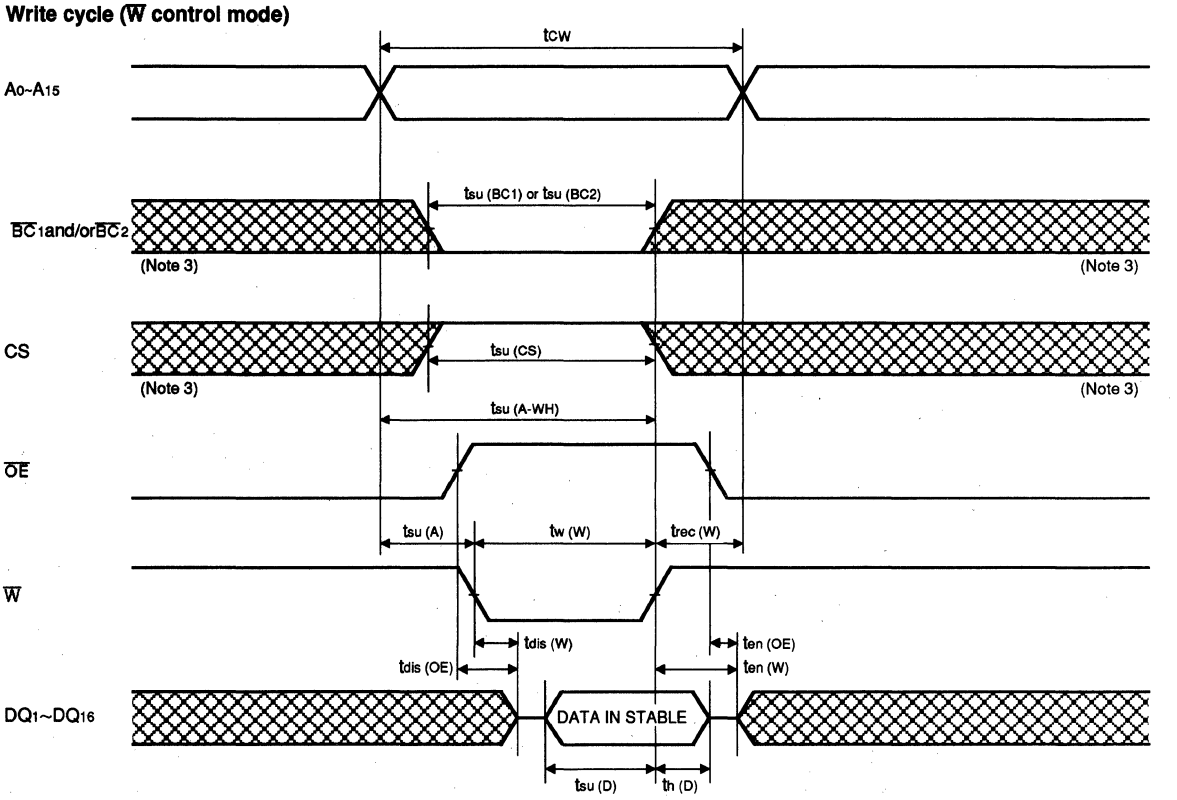
(4) TIMING DIAGRAMS

Read cycle

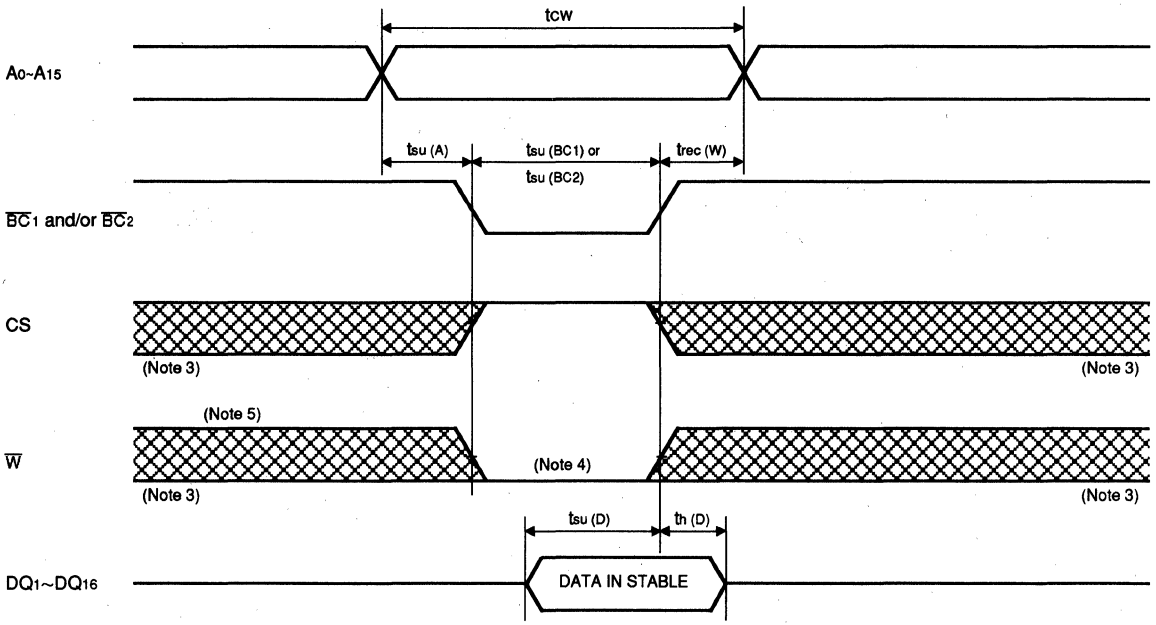


W = "H" level

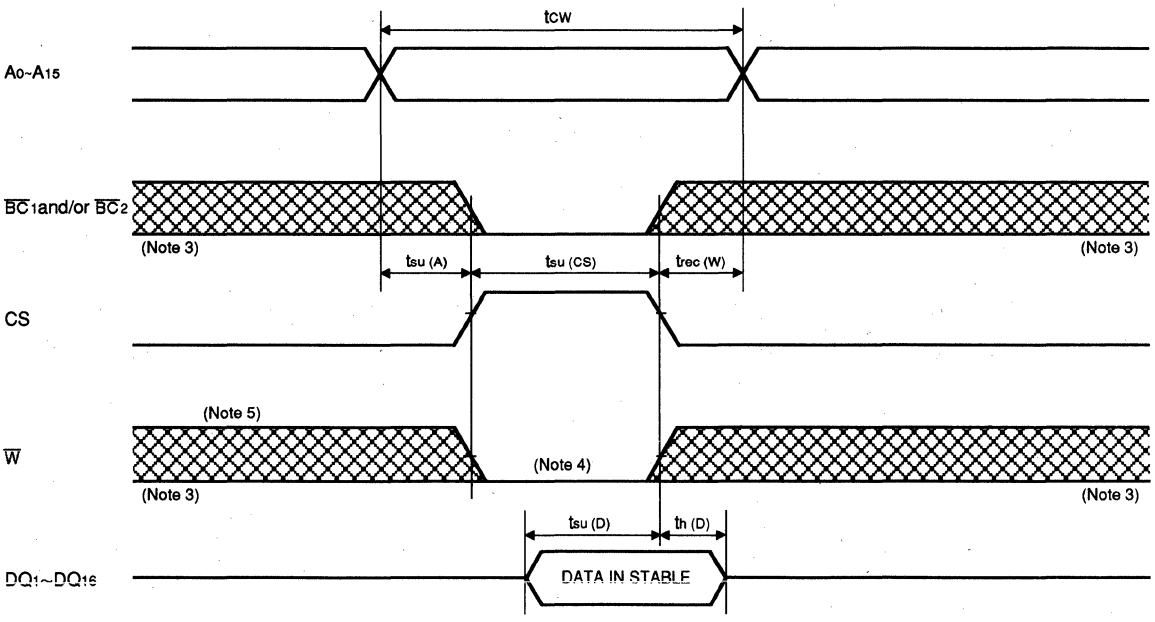
Write cycle (W control mode)



Write cycle ($\overline{BC}$ control mode)



Write cycle (CS control mode)



Note 3 : Hatching indicates the state is "don't care".
4 : Writing is executed while CS high overlaps $\overline{BC}$1 and/or $\overline{BC}$2 low and $\overline{W}$ low.
5 : When the falling edge of $\overline{W}$ is simultaneously or prior to the falling edge of $\overline{BC}$1 and/or $\overline{BC}$2 or rising edge of CS , the outputs are maintained in the high impedance state.
6 : Don't apply inverted phase signal externally when DQ pin is output mode.

POWER DOWN CHARACTERISTICS

(1) ELECTRICAL CHARACTERISTICS (Ta = 0~70℃, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ	Max	
$V_{CC\ (PD)}$	Power down supply voltage			2			V
$V_{I\ (BC)}$	Byte control input $\overline{BC}_1$ & $\overline{BC}_2$	$2.2V \leqq V_{CC\ (PD)}$		2.2			V
		$2V \leqq V_{CC\ (PD)} \leqq 2.2V$			$V_{CC\ (PD)}$		
$V_{I\ (CS)}$	Chip select input CS	$4.5V \leqq V_{CC\ (PD)}$				0.8	V
		$V_{CC\ (PD)} < 4.5V$				0.2	
$I_{CC\ (PD)}$	Power down supply current	V_{CC} = 3V 1)CS≦0.2V, other inputs=0~3V	-VL			50	μA
		2)$\overline{BC}_1$ and $\overline{BC}_2 \geqq V_{CC} - 0.2V$ $CS \geqq V_{CC} - 0.2V$, other inputs=0~3V	-VLL		0.3	10 (Note 7)	

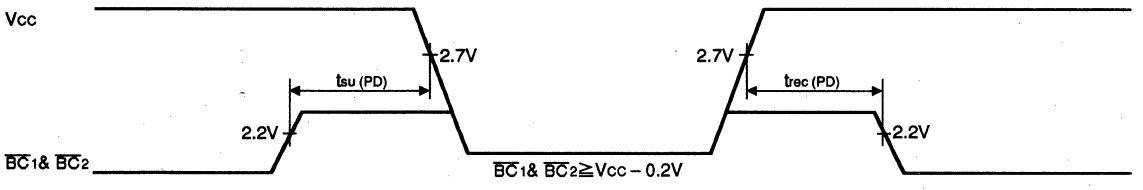
Note 7. $I_{CC\ (PD)}$ = 1 μA in case of Ta = 25℃

(2) TIMING REQUIREMENTS (Ta = 0~70℃, unless otherwise noted)

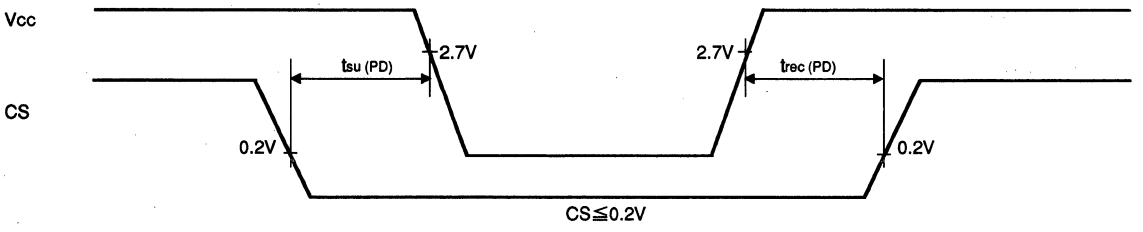
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{su\ (PD)}$	Power down set up time		0			ns
$t_{rec\ (PD)}$	Power down recovery time		5			ms

(3) POWER DOWN CHARACTERISTICS

$\overline{BC}$ control mode



CS control mode



M5M5408FP,TP,RT-85VL,-10VL, -85VLL,-10VLL

4194304-BIT (524288-WORD BY 8-BIT) CMOS STATIC RAM

DESCRIPTION

The M5M5408 is 4194304-bit CMOS static RAM organized as 524288-words by 8-bit, fabricated using high-performance quadruple-polysilicon and double metal CMOS technology.

The use of thin film transistor (TFT) load cells and CMOS periphery results in a high density and low power static RAM. The M5M5408 is designed for memory applications where the high performance, high reliability, large storage, simple interfacing and battery back-up are important design objectives.

The M5M5408 is offered in a 32-pin plastic small outline package (SOP) and a 32-pin thin small outline package (TSOP), providing high board level packing densities. Two types of TSOP packages are available, M5M5408TP(normal lead bend type package) and M5M5408RT(reverse lead bend type package). Using both two types makes it easy to design a printed circuit board.

FEATURES

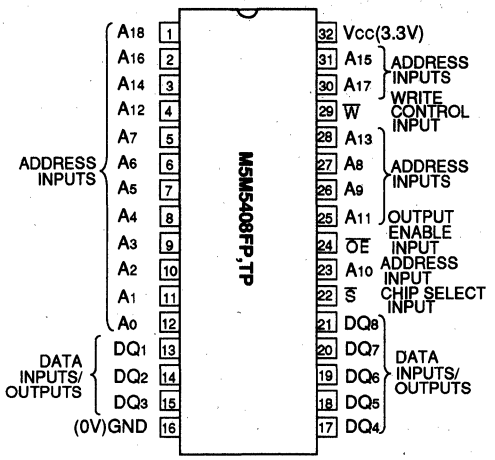
Type name	Access time (max)	Power supply current	
		Active (max)	Stand-by (max)
M5M5408FP,TP,RT- 85VL M5M5408FP,TP,RT- 10VL	85ns 100ns	3mA (1MHz)	60μA (Vcc=3.6V)
M5M5408FP,TP,RT- 85VLL M5M5408FP,TP,RT- 10VLL	85ns 100ns		12μA (Vcc=3.6V) 0.4μA (Vcc=3V,typ)

- Single +3.3V power supply
- No clocks, No refresh
- All inputs and outputs are TTL compatible
- Easy memory expansion and power down by $\overline{S}$
- Data retention supply voltage=2.0Vto 3.6V
- Three-state outputs : OR-tie capability
- $\overline{OE}$ prevents data contention in the I/O bus
- Common data I/O
- Small stand-by current·····0.4μA(typ.)
- Package
  - M5M5408FP : 32 pin 525 mil SOP
  - M5M5408TP : 32 pin 400 mil TSOP(Ⅱ)
  - M5M5408RT : 32 pin 400 mil TSOP(Ⅱ)

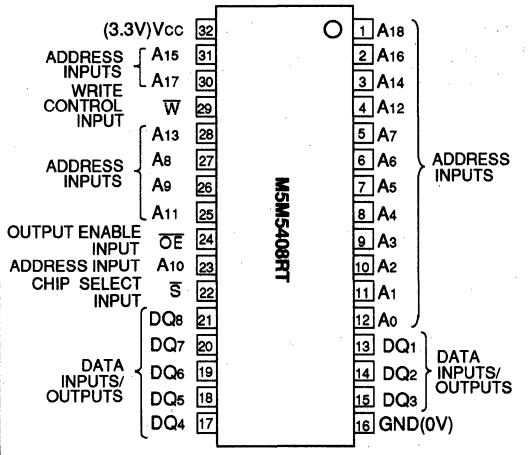
APPLICATION

Small capacity memory units, IC card, Battery operating system, Asynchronous server system

PIN CONFIGURATION (TOP VIEW)



Outline 32P2M-A(FP)
32P3Y-H(TP)



Outline 32P3Y-J

PRELIMINARY

Notice: This is not a final specification.
Some parametric limits are subject to change.

M5M5408FP,TP,RT-85VL,-10VL,-85VLL,-10VLL

4194304-BIT (524288-WORD BY 8-BIT) CMOS STATIC RAM

FUNCTION

The operation mode of the M5M5408 is determined by a combination of the device control inputs $\overline{S}$, $\overline{W}$ and $\overline{OE}$. Each mode is summarized in the function table.

A write cycle is executed whenever the low level $\overline{W}$ overlaps with the low level $\overline{S}$. The address must be set up before the write cycle and must be stable during the entire cycle. The data is latched into a cell on the trailing edge of $\overline{W}$ or $\overline{S}$, whichever occurs first, requiring the set-up and hold time relative to these edge to be maintained. The output enable $\overline{OE}$ directly controls the output stage. Setting the $\overline{OE}$ at a high level, the output stage is in a high-impedance state, and the data bus contention problem in the write cycle is eliminated.

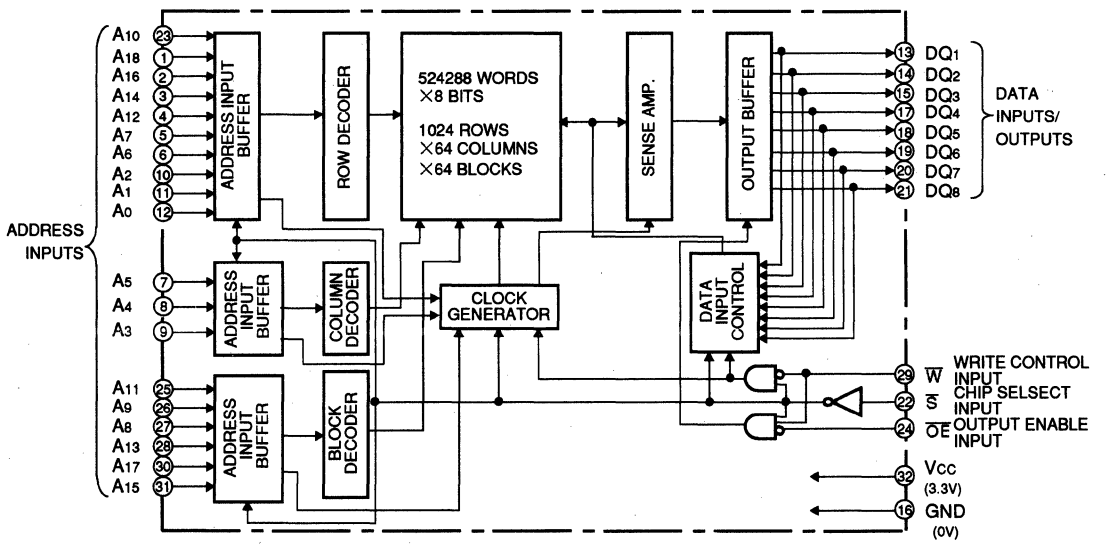
A read cycle is executed by setting $\overline{W}$ at a high level and $\overline{OE}$ at a low level while $\overline{S}$ are in an active state($\overline{S}$=L).

When setting $\overline{S}$ at a high level, the chips are in a non-selectable mode in which both reading and writing are disabled. In this mode,the output stage is in a high-impedance state, allowing OR-tie with other chips and memory expansion by $\overline{S}$. The power supply current is reduced as low as the stand-by current which is specified as Icc3 or Icc4, and the memory data can be held at +2V power supply, enabling battery back-up operation during power failure or power-down operation in the non-selected mode.

FUNCTION TABLE

$\overline{S}$	$\overline{W}$	$\overline{OE}$	Mode	DQ	Icc
H	X	X	Non selection	High-impedance	Stand-by
L	L	X	Write	D IN	Active
L	H	L	Read	D OUT	Active
L	H	H		High-impedance	Active

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to GND	−0.3～7	V
V_I	Input voltage		−0.3*～Vcc + 0.3	V
V_O	Output voltage		0～Vcc	V
P_d	Power dissipation	Ta = 25℃	700	mW
T_{opr}	Operating temperature		0～70	℃
T_{stg}	Storage temperature		−65～150	℃

* −3.0V in case of AC(Pulse width≦30ns)

ELECTRICAL CHARACTERISTICS (Ta = 0～70℃, Vcc = 3.3V±0.3V, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits Min	Limits Typ	Limits Max	Unit
V_{IH}	High-level input voltage			2.0		Vcc+0.3V	V
V_{IL}	Low-level input voltage			−0.3*		0.6	V
V_{OH}	High-level output voltage	I_{OH} = −1mA		2.4			V
		I_{OH} = −0.1mA		Vcc − 0.5V			
V_{OL}	Low-level output voltage	I_{OL} = 2mA				0.4	V
I_I	Input leakage current	V_I = 0～Vcc				±1	μA
I_O	Output leakage current	$\overline{S}$=V_{IH},$\overline{OE}$=V_{IH},$V_{I/O}$=0～Vcc				±1	μA
I_{CC1}	Active supply current (AC, MOS level)	$\overline{S}$≦0.2V Other inputs ≦0.2V or ≧Vcc − 0.2V Output-open (duty 100%)	Minimum cycle		20	30	mA
			1MHz		1.5	3	
I_{CC2}	Active supply current (AC, TTL level)	$\overline{S}$=V_{IL}, $\overline{W}$=V_{IH} Other inputs=V_{IH} or V_{IL} Output-open(duty 100%)	Minimum cycle		20	30	mA
			1MHz		1.5	3	
I_{CC3}	Stand-by supply current	$\overline{S}$≧Vcc − 0.2V other inputs = 0～Vcc	FP,TP,RT-VL			60	μA
			FP,TP,RT-VLL		0.4	12	
I_{CC4}	Stand-by supply current	$\overline{S}$=V_{IH}, other inputs=0～Vcc				0.33	mA

* −3.0V in case of AC(Pulse width≦30ns)

CAPACITANCE (Ta = 0～70℃, Vcc = 3.3V±0.3V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits Min	Limits Typ	Limits Max	Unit
C_I	Input capacitance (Ta=25℃)	V_I = GND, V_I = 25mVrms, f = 1MHz			6	pF
C_O	Output capacitance (Ta=25℃)	V_O = GND,V_O = 25mVrms, f = 1MHz			8	pF

Note 1: Direction for current flowing into IC is indicated as positive (no mark)
2: Typical value is Vcc=3.3V, Ta = 25℃

SWITCHING CHARACTERISTICS (Ta = 0～70℃, Vcc = 3.3V±0.3V, unless otherwise noted)

READ CYCLE

Symbol	Parameter	Limits				Unit
		M5M5408-85VL,-85VLL		M5M5408-10VL,-10VLL		
		Min	Max	Min	Max	
t_{CR}	Read cycle time	85		100		ns
$t_{a(A)}$	Address access time		85		100	ns
$t_{a(S)}$	Chip select access time		85		100	ns
$t_{a(OE)}$	Output enable access time		45		50	ns
$t_{dis(S)}$	Output disable time after $\overline{S}$ high		30		35	ns
$t_{dis(OE)}$	Output disable time after $\overline{OE}$ high		30		35	ns
$t_{en(S)}$	Output disable time after $\overline{S}$ low	10		10		ns
$t_{en(OE)}$	Output enable time after $\overline{OE}$ low	5		5		ns
$t_{v(A)}$	Data valid time after address	10		10		ns

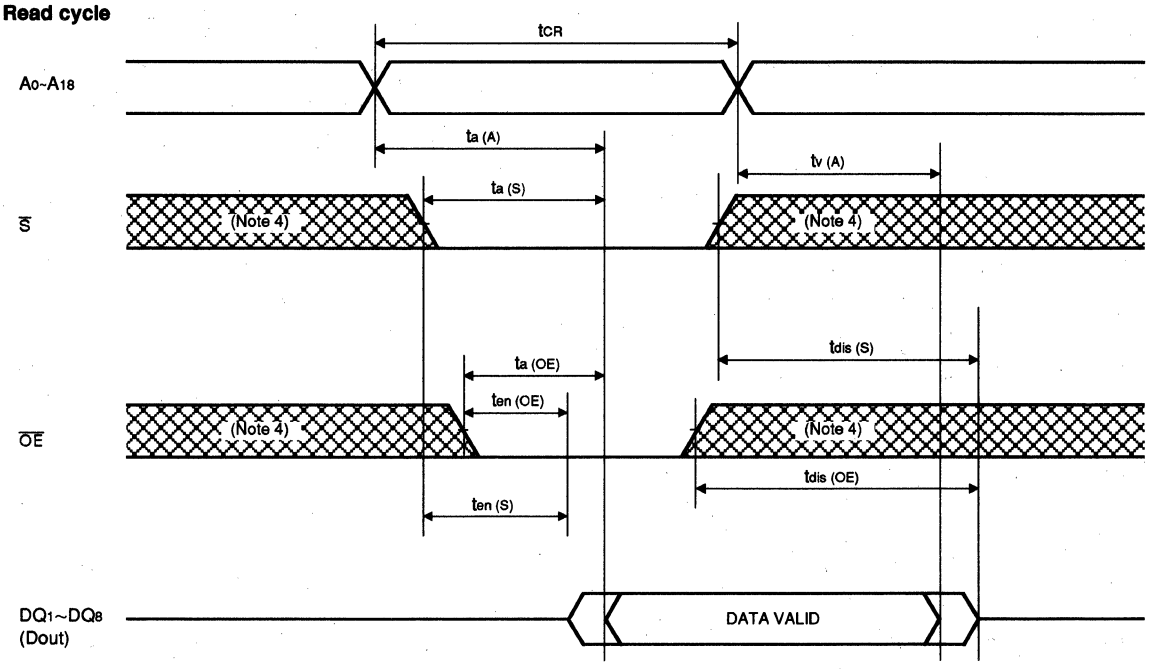
TIMING REQUIREMENTS (Ta = 0～70℃, Vcc = 3.3V±0.3V, unless otherwise noted)

WRITE CYCLE

Symbol	Parameter	Limits				Unit
		M5M5408-85VL,-85VLL		M5M5408-10VL,-10VLL		
		Min	Max	Min	Max	
t_{CW}	Write cycle time	85		100		ns
$t_{w(W)}$	Write pulse width	55		60		ns
$t_{su(A)}$	Address set up time	0		0		ns
$t_{su(A-\overline{W}H)}$	Address set up time with respect to $\overline{W}$ high	70		80		ns
$t_{su(S)}$	Chip select set up time	70		80		ns
$t_{su(D)}$	Data set up time	35		35		ns
$t_{h(D)}$	Data hold time	0		0		ns
$t_{rec(W)}$	Write recovery time	0		0		ns
$t_{dis(W)}$	Output disable time after $\overline{W}$ low		30		35	ns
$t_{dis(OE)}$	Output disable time after $\overline{OE}$ high		30		35	ns
$t_{en(W)}$	Output enable time after $\overline{W}$ high	5		5		ns
$t_{en(OE)}$	Output enable time after $\overline{OE}$ low	5		5		ns

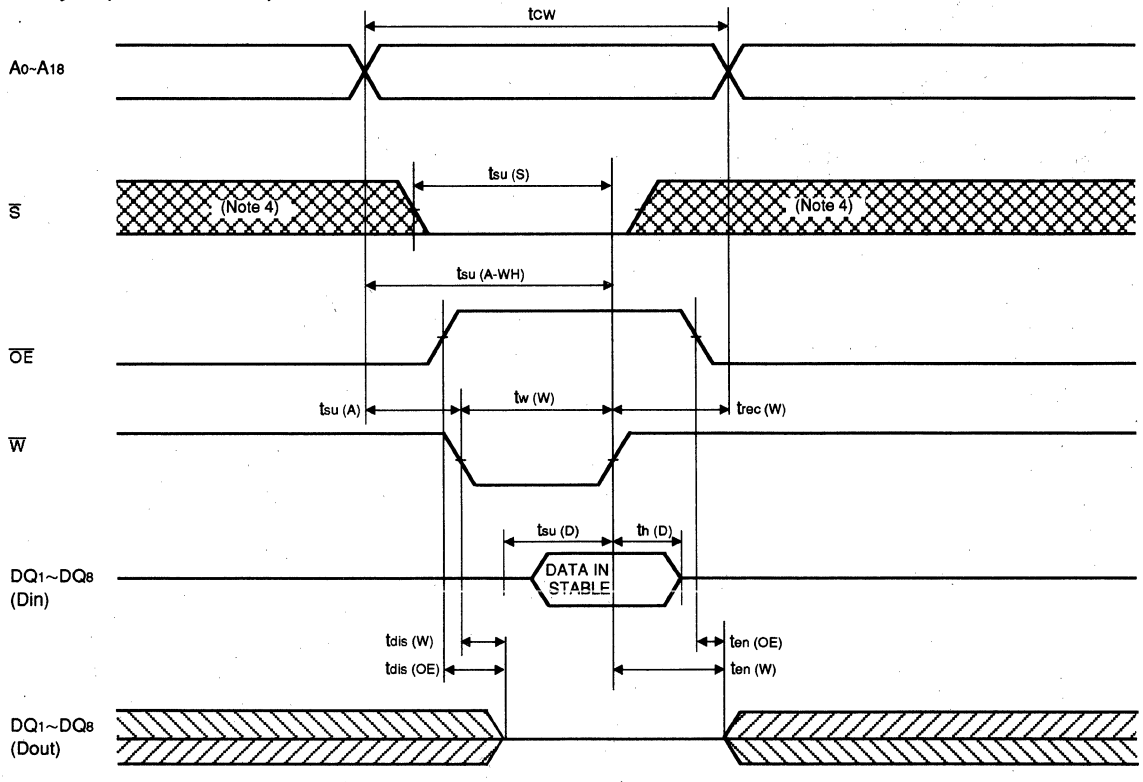
TIMING DIAGRAMS

Read cycle

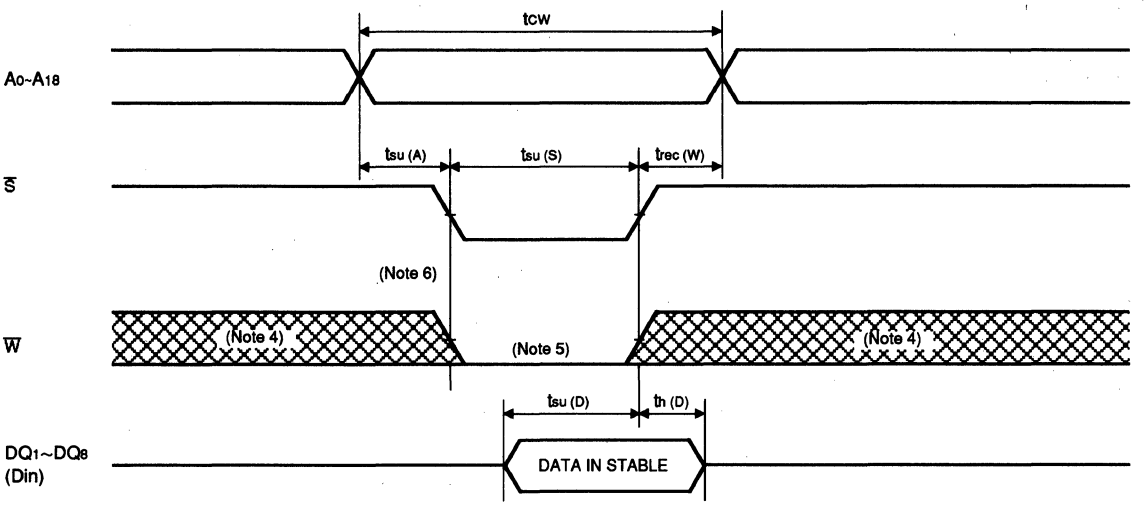


W = "H" level

Write cycle (W control mode)



Write cycle ($\overline{S}$ control mode)



Note 3 : Test condition
Input pulse ····· V_{IH}=2.2V, V_{IL}=0.4V
Input rise time and fall time ··· 5ns
Reference level ····· V_{OH}=V_{OL}=1.5V
Output loads ····· Fig. 1, C_L=30pF
C_L=5pF (for ten, tdis)
Transition is measured±500mV from steady state voltage. (for ten, tdis)

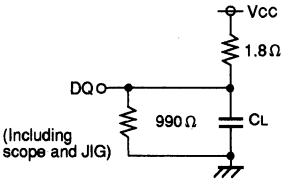


Fig.1 Output load

Note 4 : Hatching indicates the state is "don't care".
5 : A Write occurs during the overlap of a low $\overline{S}$ and a low $\overline{W}$.
6 : If $\overline{W}$ goes low simultaneously with or prior to $\overline{S}$, the output remains in the highimpedance state.
7 : Don't apply inverted phase signal externally when DQ pin is in output mode.

POWER DOWN CHARACTERISTICS

(1) ELECTRICAL CHARACTERISTICS (Ta = 0~70℃, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ	Max	
V_{CC} (PD)	Power down supply voltage			2			V
V_I ($\overline{S}$)	Chip select input $\overline{S}$			2.0			V
I_{CC} (PD)	Power down supply current	V_{CC}=3V, $\overline{S} \geqq V_{CC}$ - 0.2V, Other inputs=0~3V	FP, TP, RT-VL			50	μA
			FP, TP, RT-VLL		0.4	10*	

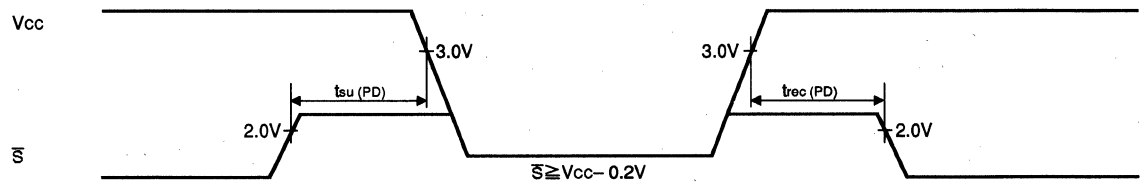
* I_{CC} (PD) = 1 μA at Ta = 25℃

(2) TIMING REQUIREMENTS (Ta = 0~70℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{su} (PD)	Power down set up time		0			ns
t_{rec} (PD)	Power down recovery time		5			ms

(3) POWER DOWN CHARACTERISTICS

$\overline{S}$ control mode



HIGH SPEED SRAM

(5V Version)

4

M5M5257DP,J-12,-15,-20, -15L,-20L

262144-BIT (262144-WORD BY 1-BIT) CMOS STATIC RAM

DESCRIPTION

The M5M5257D is a family of 262144-word by 1-bit static RAMs, fabricated with the high-performance CMOS silicon-gate MOS process and designed for high-speed application. These devices operate on a single 5V supply, and are directly TTL compatible. They include a power-down feature as well.

FEATURES

- Fast access time M5M5257DP,J-12 ..... 12ns(max)
  M5M5257DP,J-15,-15L ..... 15ns(max)
  M5M5257DP,J-20,-20L ..... 20ns(max)
- Low power dissipation Active ..... 300mW(typ)
  Stand-by (-12,-15,-20) ..... 5mW(typ)
  Stand-by(-15L,-20L) ..... 50 μW(typ)
- Power down by $\overline{S}$
- Single 5V power supply
- Fully static operation
- Requires neither external clock nor refreshing
- All inputs and outputs are directly TTL compatible
- Easy memory expansion by chip-select ($\overline{S}$) input
- All address inputs are changeable with each other

APPLICATION

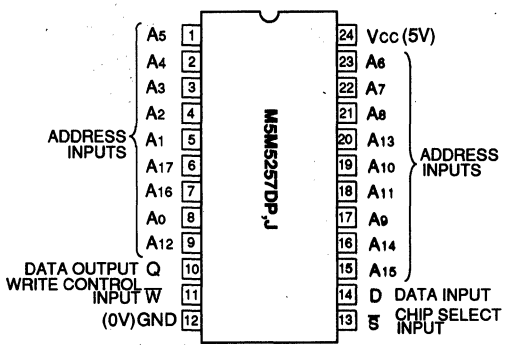
High-speed memory system

FUNCTION

A write operation is executed during the $\overline{S}$ low, and $\overline{W}$ low overlap time. In this period, address signals must be stable. When $\overline{W}$ is low, the Q terminal is maintained in the high impedance state, so it is possible to connect D and Q terminals directly.

In a read operation, after setting $\overline{W}$ to high, $\overline{S}$ to low, and if the address signals are stable, the data is available at the Q terminal.

PIN CONFIGURATION (TOP VIEW)

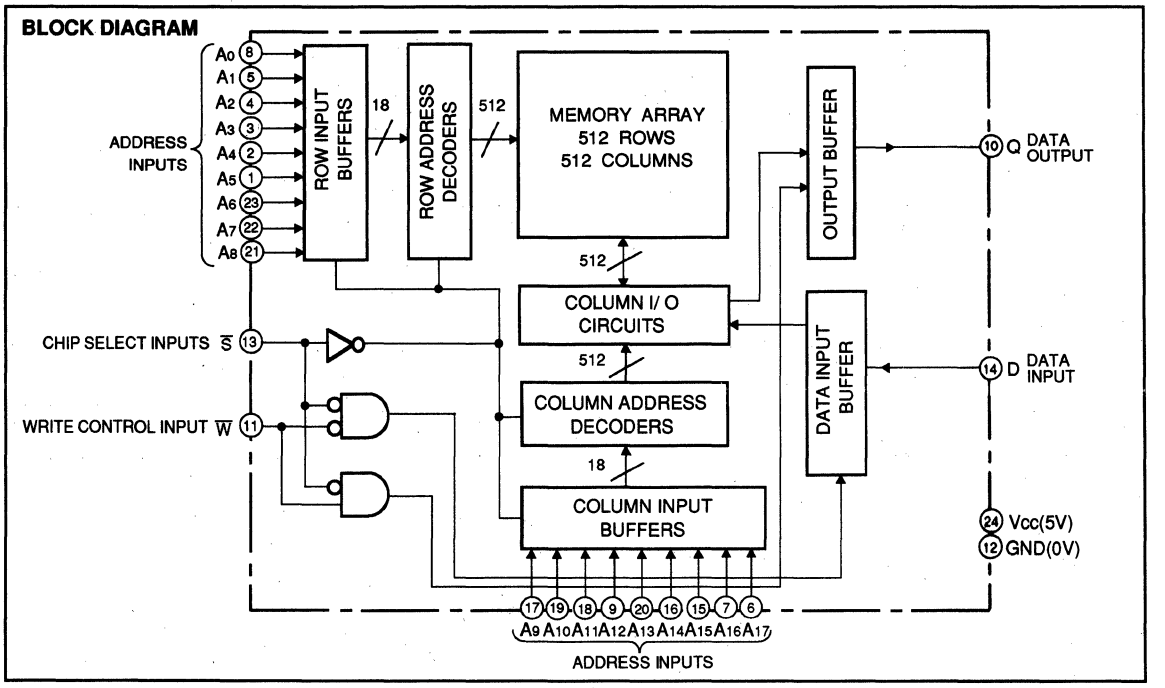


Outline 24P4Y(P)
24P0J(J)

When $\overline{S}$ is high, the chip is in the non-selectable state, disabling both reading and writing. In this case the output is in the floating (high-impedance) state, useful for OR- ties with other devices.

Signal $\overline{S}$ controls the power-down feature. When $\overline{S}$ goes high, power dissipation is reduced extremely. The access time from $\overline{S}$ is equivalent to the address access time.

BLOCK DIAGRAM



MODE SELECTION

$\overline{S}$	$\overline{W}$	Mode	Data input	Data output	Icc
H	X	Non selection	High-impedance	High-impedance	Stand-by
L	L	Write	Data input	High-impedance	Active
L	H	Read	High-impedance	Data output	Active

H:V_{IH} L:V_{IL} X:V_{IH} or V_{IL}

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to GND	−3.5*~7	V
V_I	Input voltage		−3.5*~7	V
V_O	Output voltage		−3.5*~7	V
P_d	Maximum power dissipation		1	W
T_{opr}	Operating temperature		0 ~ 70	℃
$T_{stg(bias)}$	Storage temperature (bias)		−10 ~ 85	℃
T_{stg}	Storage temperature		− 65 ~ 150	℃

* Pulse width ≦ 10ns, In case of DC: − 0.5V

ELECTRICAL CHARACTERISTICS (Ta = 0~70℃, Vcc=5V±10%, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits Min	Limits Typ	Limits Max	Unit
V_{IH}	High - level input voltage			2.2		Vcc+0.3	V
V_{IL}	Low - level input voltage			−0.5*		0.8	V
V_{OH}	High - level output voltage	I_{OH} = −4mA		2.4			V
V_{OL}	Low - level output voltage	I_{OL} = 8mA				0.4	V
I_I	Input current	V_I = 0~Vcc				2	μA
$\|I_{OZ}\|$	Off-state output current	$V_{I(\overline{S})} = V_{IH}$, V_O= 0~Vcc				10	μA
I_{CC1}	Supply current from Vcc	$V_{I(\overline{S})} = V_{IL}$ Output open	AC(12ns cycle)			140	mA
			AC(15ns cycle)			130	
			AC(20ns cycle)			120	
			DC		60	75	
I_{CC2}	Stand-by current	$V_{I(\overline{S})} = V_{IH}$	AC(12ns cycle)			60	mA
			AC(15ns cycle)			50	
			AC(20ns cycle)			40	
			Other $V_I \geqq V_{IH}$ or $\leqq V_{IL}$			30	
I_{CC3}	Stand-by current	$V_{I(\overline{S})}$ = Vcc − 0.2V Other $V_I \leqq$ 0.2V or $V_I \geqq$ Vcc − 0.2V	-12,-15,-20		1	10	mA
			-15L,-20L		10	100	μA

Note 1. Current flow into an IC is positive, out is negative.
* − 3.0V in case of AC (Pulse width≦10ns)

CAPACITANCE

Symbol	Parameter	Test conditions	Limits Min	Limits Typ	Limits Max	Unit
C_I	Input capacitance	V_I = GND, V_I =25mVrms, f=1MHz			5*	pF
C_O	Output capacitance	V_O = GND, V_O=25mVrms, f=1MHz			7*	pF

* C_I, C_O are periodically sampled and are not 100% tested.

AC ELECTRICAL CHARACTERISTICS (Ta = 0～70℃, Vcc=5V±10%, unless otherwise noted)

(1) MEASUREMENT CONDITIONS

Input pulse levels ····· V_{IH} = 3.0V, V_{IL} = 0V
Input rise and fall time ····· 3ns
Input timing reference levels ····· V_{IH} = 1.5V, V_{IL} = 1.5V
Output timing reference levels ····· V_{OH} = 1.5V, V_{OL} =1.5V
Output loads ····· Fig1,Fig2

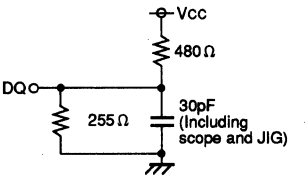


Fig.1 Output load

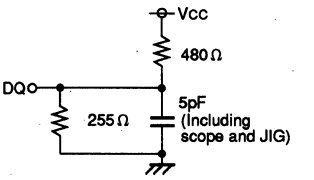


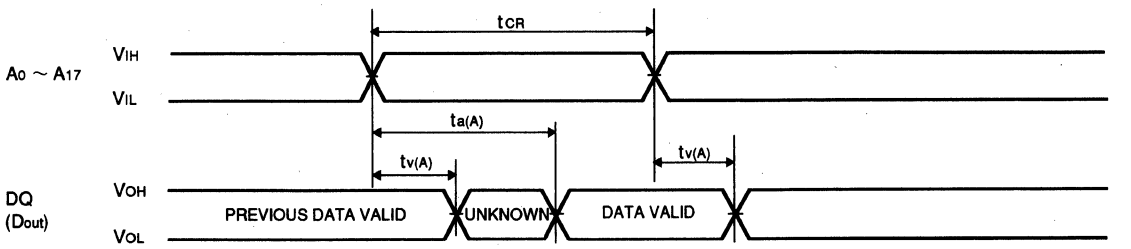
Fig.2 Output load for t_{en}, t_{dis}

(2) READ CYCLE

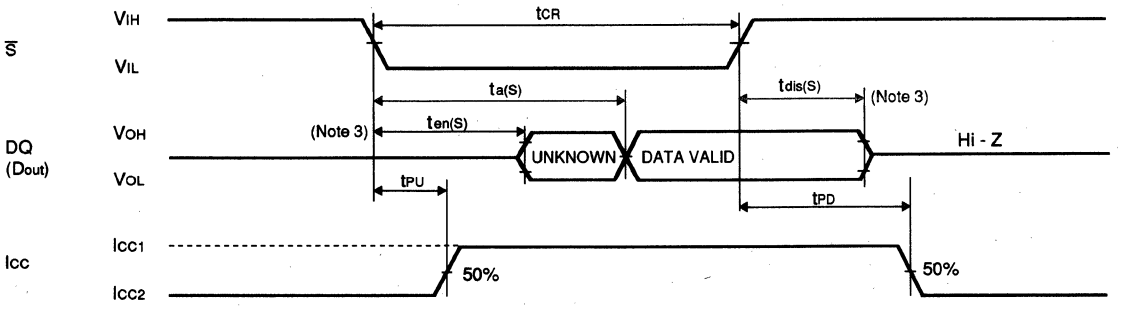
Symbol	Parameter	Limits						Unit
		M5M5257D-12		M5M5257D-15,-15L		M5M5257D-20,-20L		
		Min	Max	Min	Max	Min	Max	
t_{CR}	Read cycle time	12		15		20		ns
$t_{a(A)}$	Address access time		12		15		20	ns
$t_{a(S)}$	Chip select access time		12		15		20	ns
$t_{v(A)}$	Data valid time after address change	3		3		3		ns
$t_{en(S)}$	Output enable time after $\overline{S}$ low	3		3		3		ns
$t_{dis(S)}$	Output disable time after $\overline{S}$ high	0	6	0	7	0	8	ns
t_{PU}	Power-up time after chip selection	0		0		0		ns
t_{PD}	Power-down time after chip deselection		12		15		20	ns

(3) TIMING DIAGRAMS FOR READ CYCLE

Read cycle 1 <$\overline{W}$=H, $\overline{S}$=L>



Read cycle 2 <$\overline{W}$=H> (Note 2)



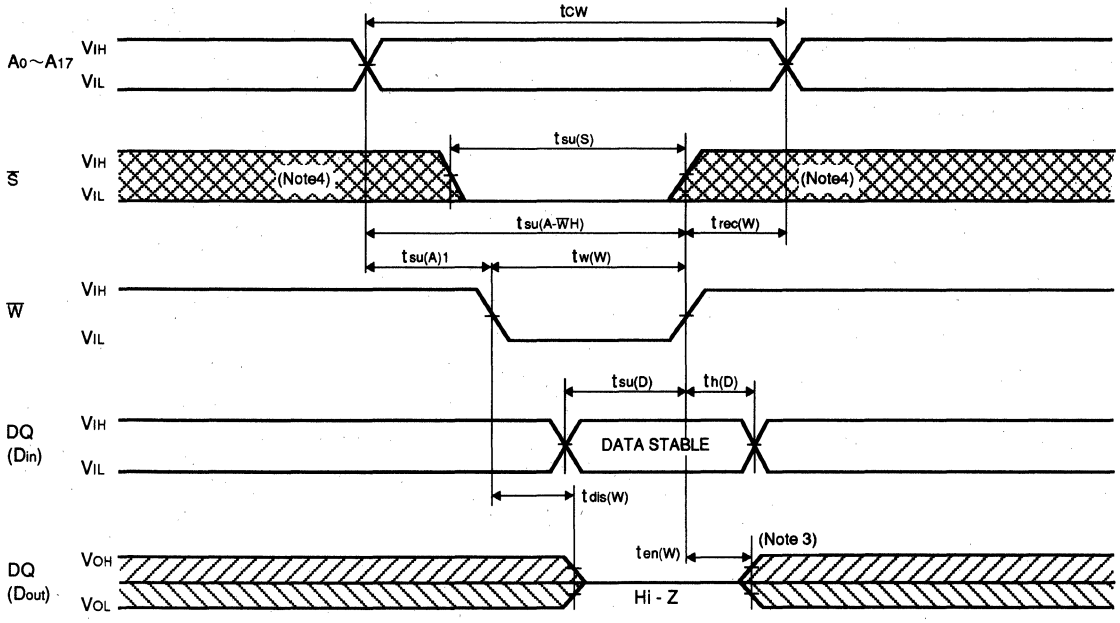
Note 2. Address valid prior to or coincident with $\overline{S}$ transition low.
3. Transition is measured ±500mV from steady state voltage with specified loading in Figure2.

(4) WRITE CYCLE

Symbol	Parameter	Limits						Unit
		M5M5257D-12		M5M5257D-15,-15L		M5M5257D-20,-20L		
		Min	Max	Min	Max	Min	Max	
t_{CW}	Write cycle time	12		15		20		ns
$t_{su(S)}$	Chip select setup time	10		12		15		ns
$t_{su(A)1}$	Address setup time 1 ($\overline{W}$ CONTROL)	0		0		0		ns
$t_{su(A)2}$	Address setup time 2 ($\overline{S}$ CONTROL)	0		0		0		ns
$t_{w(W)}$	Write pulse width	10		12		15		ns
$t_{rec(W)}$	Write recovery time	0		0		0		ns
$t_{su(D)}$	Data setup time	6		7		8		ns
$t_{h(D)}$	Data hold time	0		0		0		ns
$t_{dis(W)}$	Output disable time after $\overline{W}$ low	0	6	0	7	0	8	ns
$t_{en(W)}$	Output enable time after $\overline{W}$ high	0		0		0		ns
$t_{su(A-WH)}$	Address to $\overline{W}$ high	10		12		15		ns

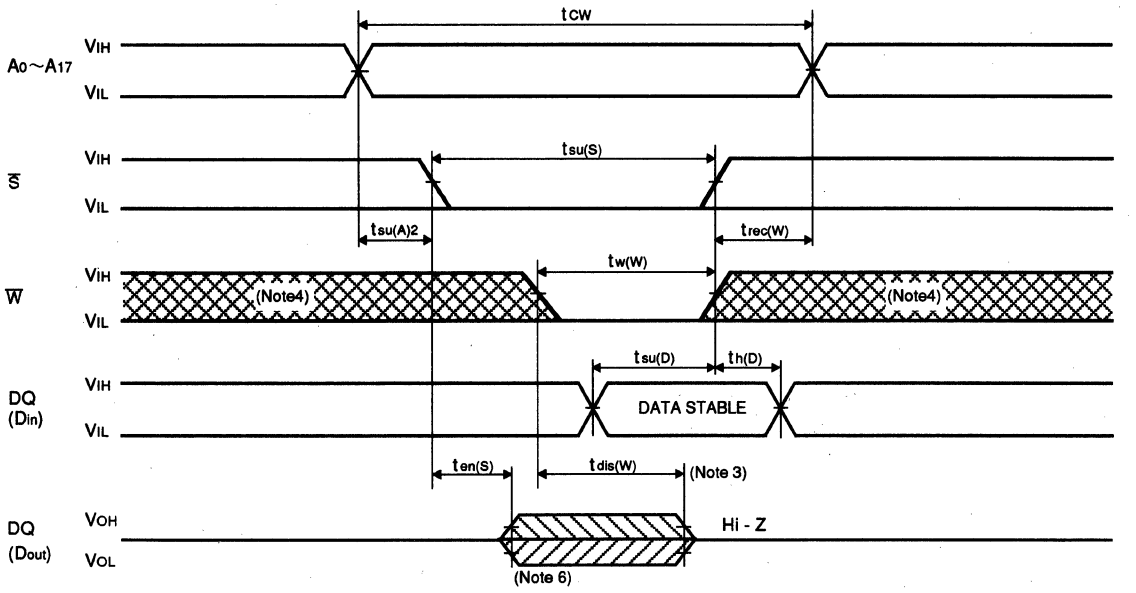
(5) TIMING DIAGRAMS FOR WRITE CYCLE

Write cycle 1 ($\overline{W}$ control mode)



Note 4. Hatching indicates the state is don't care.

Write cycle 2 ($\overline{S}$ control mode)



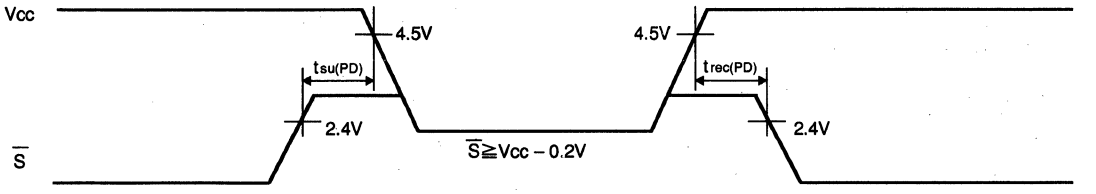
Note 5. When the falling edge of $\overline{W}$ is simultaneous or prior to the falling edge of $\overline{S}$, the output is maintained in the high impedance.
6. t_{en},t_{dis} are periodically sampled and are not 100% tested.

POWER DOWN CHARACTERISTICS (Ta = 0~70℃, Vcc=5V±10%, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ	Max	
$V_{CC(PD)}$	Power down supply voltage	$V_{I(\overline{S})} \geqq V_{CC}-0.2V$ $V_I \geqq V_{CC}-0.2V$ or $0V \leqq V_I \leqq 0.2V$		2			V
$V_{I(\overline{S})}$	Chip select input voltage			Vcc-0.2			V
$t_{su(PD)}$	Power down setup time			0			ns
$t_{rec(PD)}$	Power down recovery time		-15L	15			ns
			-20L	20			
$I_{CC(PD)}$	Power down supply current	Vcc = 3.0V				50	μA

Note 7. This is only M5M5257DP, J -15L,-20L

TIMING WAVEFORM FOR POWER DOWN



M5M5258DP,J-12,-15,-20, -15L,-20L

262144-BIT (65536-WORD BY 4-BIT) CMOS STATIC RAM

DESCRIPTION

The M5M5258D is a family of 65536-word by 4-bit static RAMs, fabricated with the high-performance CMOS silicon-gate MOS process and designed for high-speed application. These devices operate on a single 5V supply, and are directly TTL compatible. They include a power-down feature as well.

FEATURES

- Fast access time M5M5258DP,J-12 ..... 12ns(max)
  M5M5258DP,J-15,-15L ..... 15ns(max)
  M5M5258DP,J-20,-20L ..... 20ns(max)
- Low power dissipation Active ..... 300mW(typ)
  Stand-by (-12,-15,-20) ..... 5mW(typ)
  Stand-by(-15L,-20L) ..... 50 μW(typ)
- Power down by $\overline{S}$
- Single 5V power supply
- Fully static operation
- Requires neither external clock nor refreshing
- All inputs and outputs are directly TTL compatible
- Easy memory expansion by chip-select ($\overline{S}$) input
- All address inputs are changeable with each other

APPLICATION

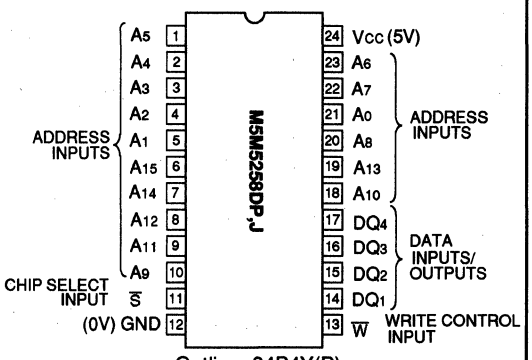
High-speed memory system

FUNCTION

A write operation is executed during the $\overline{S}$ low, and $\overline{W}$ low overlap time. In this period, address signals must be stable. When $\overline{W}$ is low, the DQ terminals are maintained in the high impedance state.

In a read operation, after setting $\overline{W}$ to high, $\overline{S}$ to low, and if the address signals are stable, the data is available at the DQ terminals.

PIN CONFIGURATION (TOP VIEW)

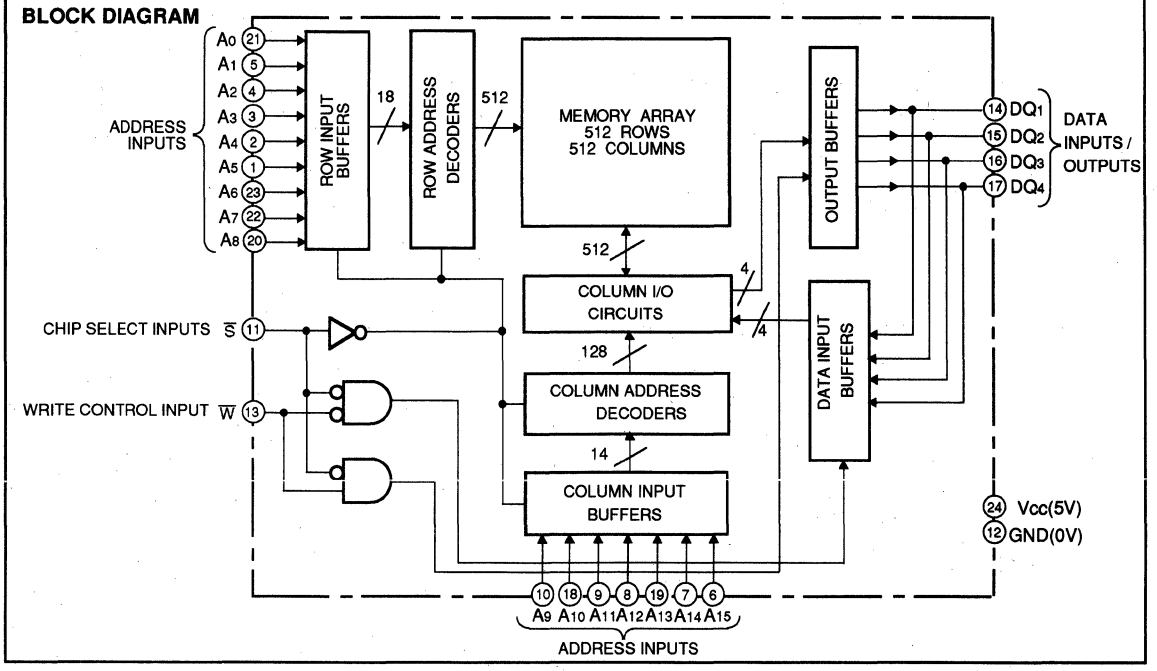


Outline 24P4Y(P)
24P0J(J)

When $\overline{S}$ is high, the chip is in the non-selectable state, disabling both reading and writing. In this case the output is in the floating (high-impedance) state,useful for OR- ties with other devices.

Signal $\overline{S}$ controls the power-down feature. When $\overline{S}$ goes high, power dissipation is reduced extremely. The access time from $\overline{S}$ is equivalent to the address access time.

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

MODE SELECTION

$\overline{S}$	$\overline{W}$	Mode	Data input /output	Icc
H	X	Non selection	High-impedance	Stand-by
L	L	Write	Din	Active
L	H	Read	Dout	Active

H:V_{IH} L:V_{IL} X:V_{IH} or V_{IL}

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to GND	−3.5*~7	V
V_I	Input voltage		−3.5*~7	V
V_O	Output voltage		−3.5*~7	V
P_d	Maximum power dissipation		1	W
T_{opr}	Operating temperature		0 ~ 70	℃
$T_{stg(bias)}$	Storage temperature (bias)		−10 ~ 85	℃
T_{stg}	Storage temperature		− 65 ~ 150	℃

* Pulse width ≦ 10ns, In case of DC: − 0.5V

ELECTRICAL CHARACTERISTICS (Ta = 0~70℃, Vcc=5V±10%, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits Min	Limits Typ	Limits Max	Unit
V_{IH}	High - level input voltage			2.2		Vcc+0.3	V
V_{IL}	Low - level input voltage			−0.5*		0.8	V
V_{OH}	High - level output voltage	I_{OH} = −4mA		2.4			V
V_{OL}	Low - level output voltage	I_{OL} = 8mA				0.4	V
I_I	Input current	V_I = 0~Vcc				2	μA
$\|I_{OZ}\|$	Off-state output current	$V_{I(\overline{S})} = V_{IH}$, V_O= 0~Vcc				10	μA
I_{CC1}	Supply current from Vcc	$V_{I(\overline{S})} = V_{IL}$ Output open	AC(12ns cycle)			140	mA
			AC(15ns cycle)			130	
			AC(20ns cycle)			120	
			DC		60	75	
I_{CC2}	Stand-by current	$V_{I(\overline{S})} = V_{IH}$	AC(12ns cycle)			60	mA
			AC(15ns cycle)			50	
			AC(20ns cycle)			40	
			Other V_I ≧V_{IH} or ≦ V_{IL}			30	
I_{CC3}	Stand-by current	$V_{I(\overline{S})}$ = Vcc − 0.2V Other V_I≦ 0.2V or V_I ≧Vcc − 0.2V	-12,-15,-20		1	10	mA
			-15L,-20L		10	100	μA

Note 1. Current flow into an IC is positive, out is negative.
* − 3.0V in case of AC (Pulse width≦10ns)

CAPACITANCE

Symbol	Parameter	Test conditions	Limits Min	Limits Typ	Limits Max	Unit
C_I	Input capacitance	V_I = GND,V_I =25mVrms, f=1MHz			5 *	pF
C_O	Output capacitance	V_O = GND,V_O=25mVrms, f=1MHz			7 *	pF

* C_I,C_O are periodically sampled and are not 100% tested.

AC ELECTRICAL CHARACTERISTICS (Ta = 0～70℃, Vcc=5V±10%, unless otherwise noted)

(1) MEASUREMENT CONDITIONS

Input pulse levels ····· V_{IH} = 3.0V, V_{IL} = 0V
Input rise and fall time ····· 3ns
Input timing reference levels ····· V_{IH} = 1.5V, V_{IL} = 1.5V
Output timing reference levels ····· V_{OH} = 1.5V, V_{OL} =1.5V
Output loads ····· Fig1,Fig2

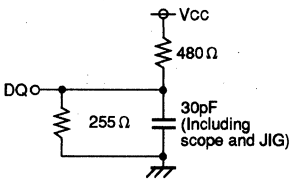


Fig.1 Output load

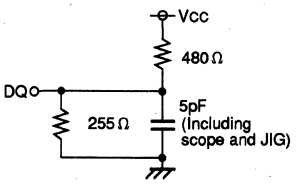


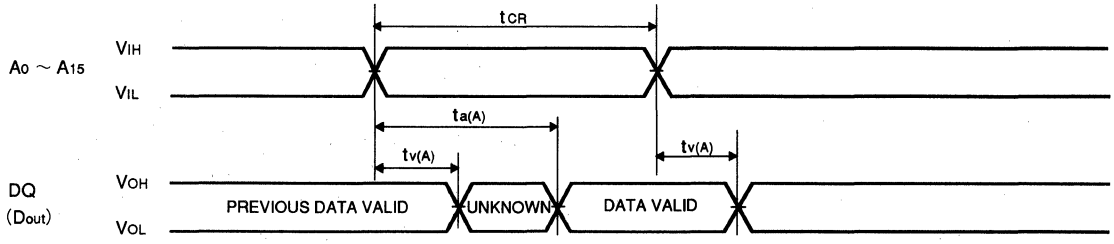
Fig.2 Output load for ten, tdis

(2) READ CYCLE

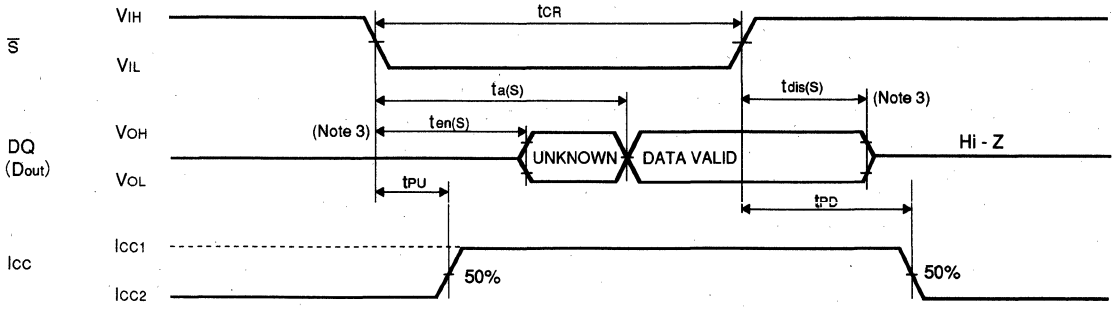
Symbol	Parameter	Limits						Unit
		M5M5258D-12		M5M5258D-15,-15L		M5M5258D-20,-20L		
		Min	Max	Min	Max	Min	Max	
t_{CR}	Read cycle time	12		15		20		ns
$t_{a(A)}$	Address access time		12		15		20	ns
$t_{a(S)}$	Chip select access time		12		15		20	ns
$t_{v(A)}$	Data valid time after address change	3		3		3		ns
$t_{en(S)}$	Output enable time after $\overline{S}$ low	3		3		3		ns
$t_{dis(S)}$	Output disable time after $\overline{S}$ high	0	6	0	7	0	8	ns
t_{PU}	Power-up time after chip selection	0		0		0		ns
t_{PD}	Power-down time after chip deselection		12		15		20	ns

(3) TIMING DIAGRAMS FOR READ CYCLE

Read cycle 1 <$\overline{W}$=H, $\overline{S}$=L>



Read cycle 2 <$\overline{W}$=H> (Note 2)



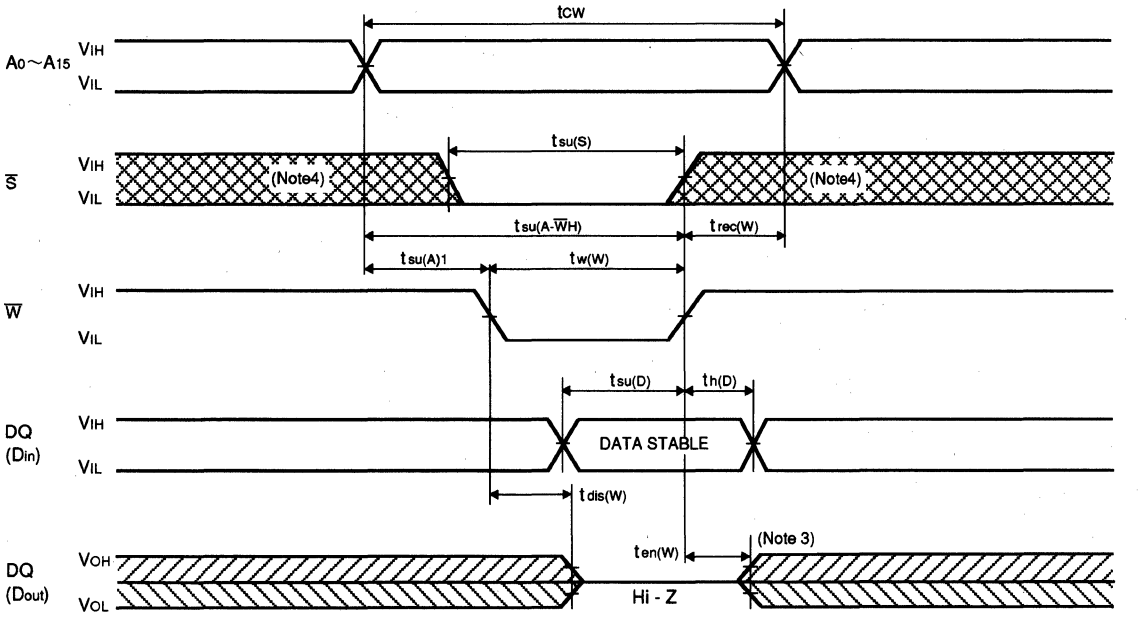
Note 2. Address valid prior to or coincident with $\overline{S}$ transition low.
3. Transition is measured ±500mV from steady state voltage with specified loading in Figure2.

(4) WRITE CYCLE

Symbol	Parameter	Limits						Unit
		M5M5258D-12		M5M5258D-15,-15L		M5M5258D-20,-20L		
		Min	Max	Min	Max	Min	Max	
t_{CW}	Write cycle time	12		15		20		ns
$t_{su(S)}$	Chip select setup time	10		12		15		ns
$t_{su(A)1}$	Address setup time 1 ($\overline{W}$ CONTROL)	0		0		0		ns
$t_{su(A)2}$	Address setup time 2 ($\overline{S}$ CONTROL)	0		0		0		ns
$t_{w(W)}$	Write pulse width	10		12		15		ns
$t_{rec(W)}$	Write recovery time	0		0		0		ns
$t_{su(D)}$	Data setup time	6		7		8		ns
$t_{h(D)}$	Data hold time	0		0		0		ns
$t_{dis(W)}$	Output disable time after $\overline{W}$ low	0	6	0	7	0	8	ns
$t_{en(W)}$	Output enable time after $\overline{W}$ high	0		0		0		ns
$t_{su(A\text{-}\overline{W}H)}$	Address to $\overline{W}$ high	10		12		15		ns

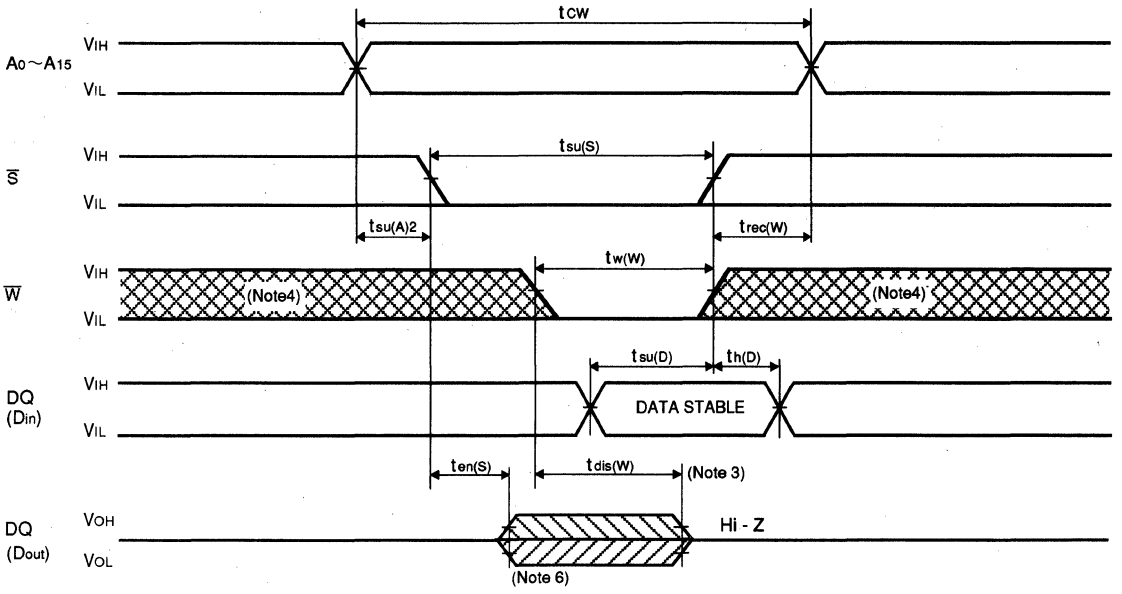
(5) TIMING DIAGRAMS FOR WRITE CYCLE

Write cycle 1 ($\overline{W}$ control mode)



Note 4. Hatching indicates the state is don't care.

Write cycle 2 ($\overline{S}$ control mode)



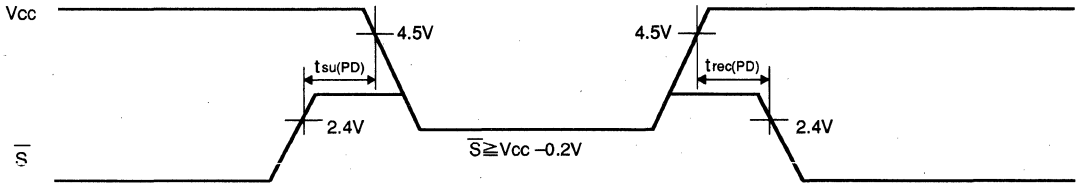
Note 5. When the falling edge of $\overline{W}$ is simultaneous or prior to the falling edge of $\overline{S}$, the output is maintained in the high impedance.
6. ten,tdis are periodically sampled and are not 100% tested.

POWER DOWN CHARACTERISTICS (Ta = 0～70℃, Vcc=5V±10%, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ	Max	
$V_{CC(PD)}$	Power down supply voltage			2			V
$V_{I(\overline{S})}$	Chip select input voltage	$V_{I(\overline{S})} \geqq V_{CC}-0.2V$		Vcc-0.2			V
$t_{su(PD)}$	Power down setup time	$V_I \geqq V_{CC}-0.2V$ or		0			ns
$t_{rec(PD)}$	Power down recovery time	$0V \leqq V_I \leqq 0.2V$	-15L	15			ns
			-20L	20			
$I_{CC(PD)}$	Power down supply current	Vcc = 3.0V				50	μA

Note 7. This is only M5M5258DP, J -15L,-20L

TIMING WAVEFORM FOR POWER DOWN



M5M5278DP,J-12,-15,-20,-15L,-20L
M5M5278DFP, VP-15,-20,-15L,-20L

262144-BIT (32768-WORD BY 8-BIT) CMOS STATIC RAM

DESCRIPTION

The M5M5278D is a family of 32768-word by 8-bit static RAMs, fabricated with the high-performance CMOS silicon-gate MOS process and designed for high-speed application.These devices operate on a single 5V supply, and are directly TTL compatible. They include a power-down feature as well.

FEATURES

- Fast access time M5M5278DP,J-12 ..... 12ns(max)
  M5M5278DP,J,FP,VP-15,-15L ..... 15ns(max)
  M5M5278DP,J,FP,VP-20,-20L ..... 20ns(max)
- Low power dissipation Active ..... 375mW(typ)
  Stand-by(-12,-15,-20) ..... 5 mW(typ)
  Stand-by(-15L,-20L) ..... 50μW(typ)
- Power down by $\overline{S}$
- Single 5V power supply
- Fully static operation
- Requires neither external clock nor refreshing
- All inputs and outputs are directly TTL compatible
- Easy memory expansion by chip-select ($\overline{S}$) input
- Output enable($\overline{OE}$) prevents data contention in the I/O bus
- All address inputs are changeable with each other

APPLICATION

High-speed memory system

FUNCTION

A write operation is executed during the $\overline{S}$ low, and $\overline{W}$ low overlap time. In this period, address signals must be stable. When $\overline{W}$ is low, the DQ terminals is maintained in the high impedance state.

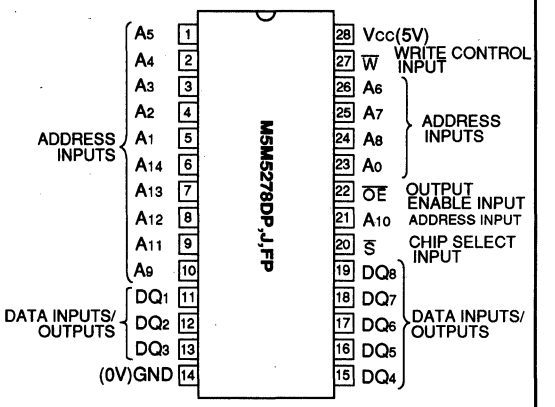
In a read operation, after setting $\overline{W}$ to high, $\overline{S}$ to low, and $\overline{OE}$ to low, if the address signals are stable, the data is available at the DQ terminals.

When $\overline{S}$ is high, the chip is in the non-selectable state, disabling both reading and writing. In this case the output is in the floating (high-impedance) state, useful for OR- ties with other devices.

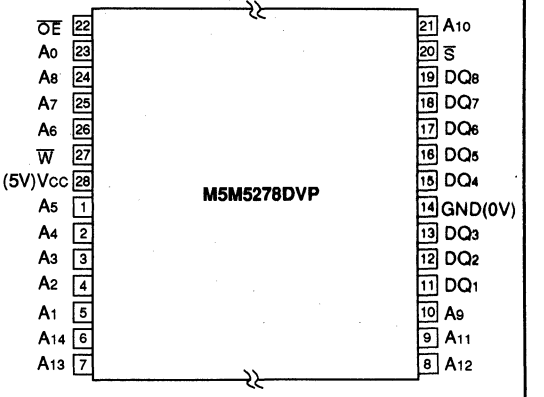
Setting $\overline{OE}$ at a high level,the output stage is in a high-impedance state, and the data bus contention problem in the write cycle is eliminated.

Signal $\overline{S}$ controls the power-down feature. When $\overline{S}$ goes high, power dissipation is reduced extremely. The access time from $\overline{S}$ is equivalent to the address access time.

PIN CONFIGURATION (TOP VIEW)



Outline 28P4Y(P)
28P0J(J)
28P2W-C(FP)



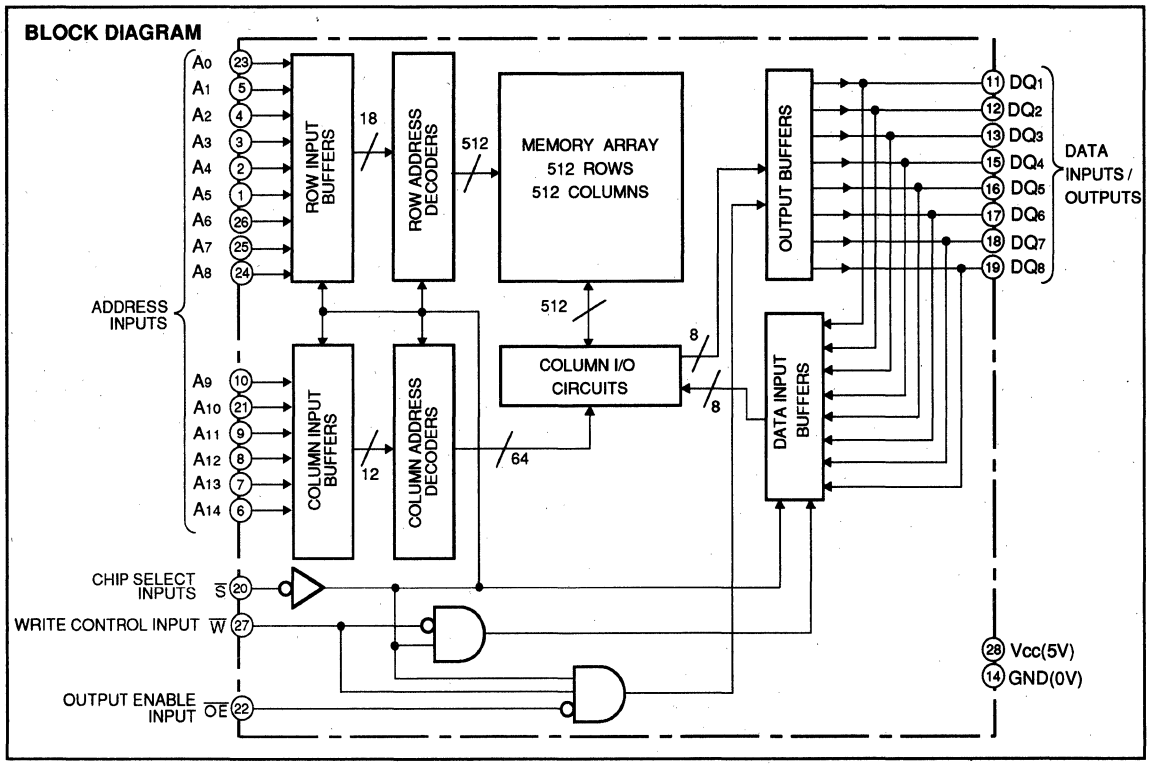
Outline 28P2C-A

MODE SELECTION

$\overline{S}$	$\overline{W}$	$\overline{OE}$	Mode	Data input /output	Icc
H	X	X	Non selection	High-impedance	Stand-by
L	L	X	Write	Din	Active
L	H	L	Read	Dout	Active
L	H	H		High-impedance	Active

H:VIH L:VIL X:VIH or VIL

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to GND	−3.5*~7	V
V_I	Input voltage		−3.5*~7	V
V_O	Output voltage		−3.5*~7	V
P_d	Maximum power dissipation		1	W
T_{opr}	Operating temperature		0 ~ 70	℃
$T_{stg(bias)}$	Storage temperature (bias)		−10 ~ 85	℃
T_{stg}	Storage temperature		− 65 ~ 150	℃

* Pulse width ≦ 10ns, In case of DC: − 0.5V

DC ELECTRICAL CHARACTERISTICS (Ta = 0~70℃, Vcc=5V±10%, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits Min	Limits Typ	Limits Max	Unit
V_{IH}	High - level input voltage			2.2		Vcc+0.3	V
V_{IL}	Low - level input voltage			−0.5*		0.8	V
V_{OH}	High - level output voltage	I_{OH} = − 4mA		2.4			V
V_{OL}	Low - level output voltage	I_{OL} = 8mA				0.4	V
I_I	Input current	V_I = 0~Vcc				2	μA
$\|I_{OZ}\|$	Off-state output current	$V_{I(S)}$ = V_{IH} , V_O= 0~Vcc				10	μA
I_{CC1}	Supply current from Vcc	$V_{I(S)}$ = V_{IL} Output open	AC(12ns cycle)			160	mA
			AC(15ns cycle)			150	
			AC(20ns cycle)			140	
			DC		75	85	
I_{CC2}	Stand-by current	$V_{I(S)}$ = V_{IH}	AC(12ns cycle)			60	mA
			AC(15ns cycle)			50	
			AC(20ns cycle)			40	
			Other V_I ≧V_{IH} or ≦ V_{IL}			30	
I_{CC3}	Stand-by current	$V_{I(S)}$ = Vcc − 0.2V Other V_I≦ 0.2V or V_I ≧Vcc−0.2V	-12,-15,-20		1	10	mA
			-15L,-20L		10	100	μA

Note 1. Current flow into an IC is positive, out is negative.
* − 3.0V in case of AC (Pulse width≦10ns)

CAPACITANCE

Symbol	Parameter	Test conditions	Limits Min	Limits Typ	Limits Max	Unit
C_I	Input capacitance	V_I = GND, V_I =25mVrms, f=1MHz			5*	pF
C_O	Output capacitance	V_O = GND, V_O=25mVrms, f=1MHz			7*	pF

* C_I, C_O are periodically sampled and are not 100% tested.

AC ELECTRICAL CHARACTERISTICS (Ta = 0~70℃, Vcc=5V±10%, unless otherwise noted)

(1) MEASUREMENT CONDITIONS

Input pulse levels ..... V_{IH} = 3.0V, V_{IL} = 0V
Input rise and fall time 3ns
Input timing reference levels ..... V_{IH} = 1.5V, V_{IL} = 1.5V
Output timing reference levels ..... V_{OH} = 1.5V, V_{OL} =1.5V
Output loads Fig1,Fig2

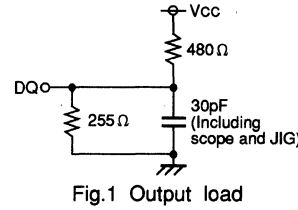


Fig.1 Output load

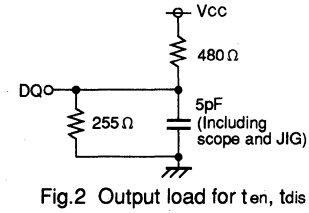


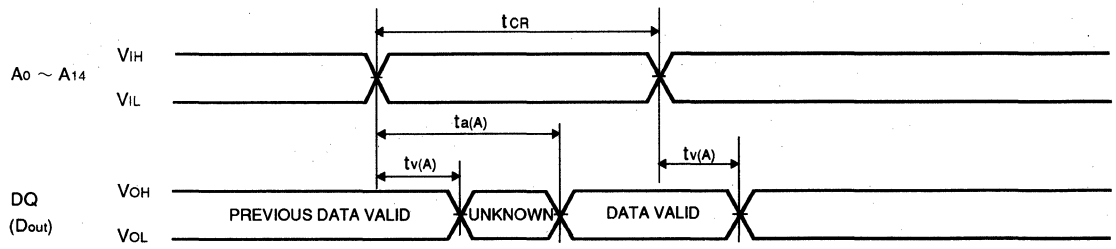
Fig.2 Output load for t_{en}, t_{dis}

(2) READ CYCLE

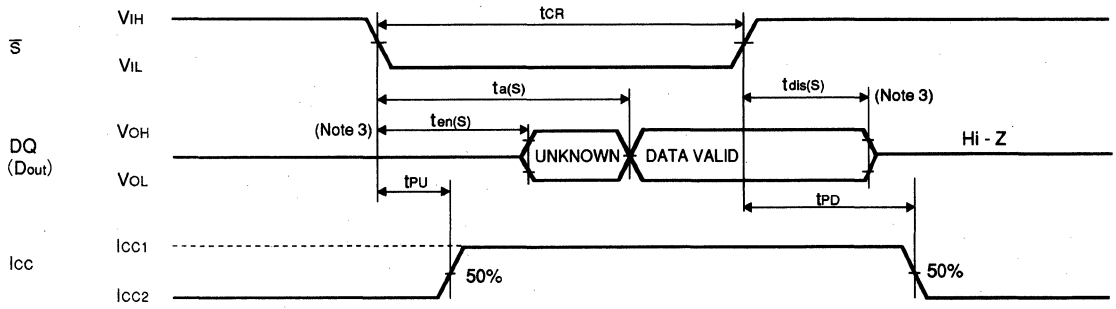
Symbol	Parameter	Limits						Unit
		M5M5278D-12		M5M5278D-15,-15L		M5M5278D-20,-20L		
		Min	Max	Min	Max	Min	Max	
t_{CR}	Read cycle time	12		15		20		ns
$t_{a(A)}$	Address access time		12		15		20	ns
$t_{a(S)}$	Chip select access time		12		15		20	ns
$t_{a(OE)}$	Output enable access time		6		8		10	ns
$t_{v(A)}$	Data valid time after address change	3		3		3		ns
$t_{en(S)}$	Output enable time after $\overline{S}$ low	3		3		3		ns
$t_{dis(S)}$	Output disable time after $\overline{S}$ high	0	6	0	7	0	8	ns
$t_{en(OE)}$	Output enable time after $\overline{OE}$ low	0		0		0		ns
$t_{dis(OE)}$	Output disable time after $\overline{OE}$ high	0	6	0	7	0	8	ns
t_{PU}	Power-up time after chip selection	0		0		0		ns
t_{PD}	Power-down time after chip deselection		12		15		20	ns

(3) TIMING DIAGRAMS FOR READ CYCLE

Read cycle 1 <$\overline{W}$=H, $\overline{S}$=L>

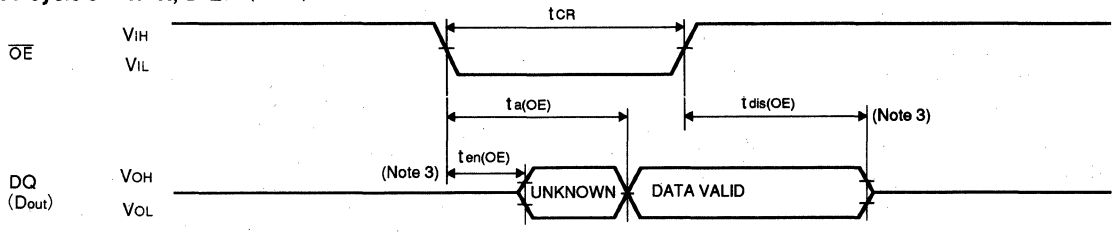


Read cycle 2 <$\overline{W}$=H> (Note 2)



Note 2. Address valid prior to or coincident with $\overline{S}$ transition low.
3. Transition is measured ±500mV from steady state voltage with specified loading in Figure2.

Read cycle 3 <$\overline{W}$=H, $\overline{S}$=L> (Note 4)



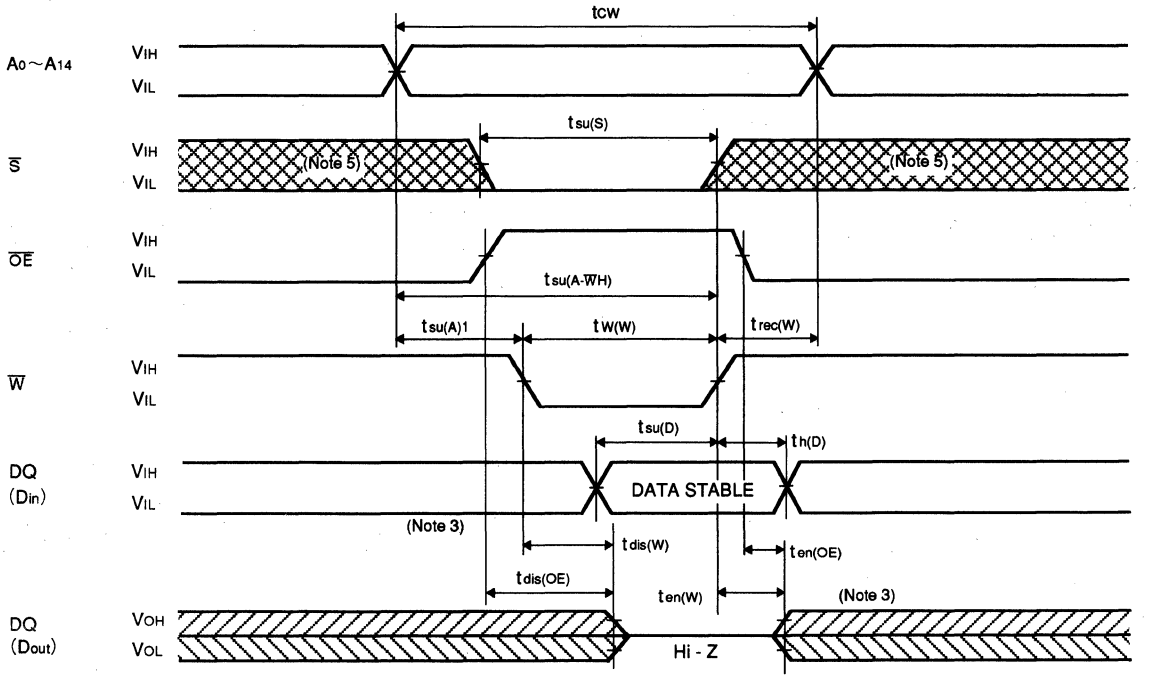
Note 4. Address and $\overline{S}$ valid prior to $\overline{OE}$ transition low by (ta(A) - ta(OE)), (ta(S)-ta(OE)).

(4) WRITE CYCLE

Symbol	Parameter	Limits						Unit
		M5M5278D-12		M5M5278D-15,-15L		M5M5278D-20,-20L		
		Min	Max	Min	Max	Min	Max	
t_{CW}	Write cycle time	12		15		20		ns
$t_{su(S)}$	Chip select setup time	10		12		15		ns
$t_{su(A)1}$	Address setup time 1 ($\overline{W}$ CONTROL)	0		0		0		ns
$t_{su(A)2}$	Address setup time 2 ($\overline{S}$ CONTROL)	0		0		0		ns
$t_{w(W)}$	Write pulse width	10		12		15		ns
$t_{rec(W)}$	Write recovery time	0		0		0		ns
$t_{su(D)}$	Data setup time	6		7		8		ns
$t_{h(D)}$	Data hold time	0		0		0		ns
$t_{dis(W)}$	Output disable time after $\overline{W}$ low	0	6	0	7	0	8	ns
$t_{en(W)}$	Output enable time after $\overline{W}$ high	0		0		0		ns
$t_{su(A-\overline{W}H)}$	Address to $\overline{W}$ high	10		12		15		ns
$t_{en(OE)}$	Output enable time after $\overline{OE}$ low	0		0		0		ns
$t_{dis(OE)}$	Output disable time after $\overline{OE}$ high	0	6	0	7	0	8	ns

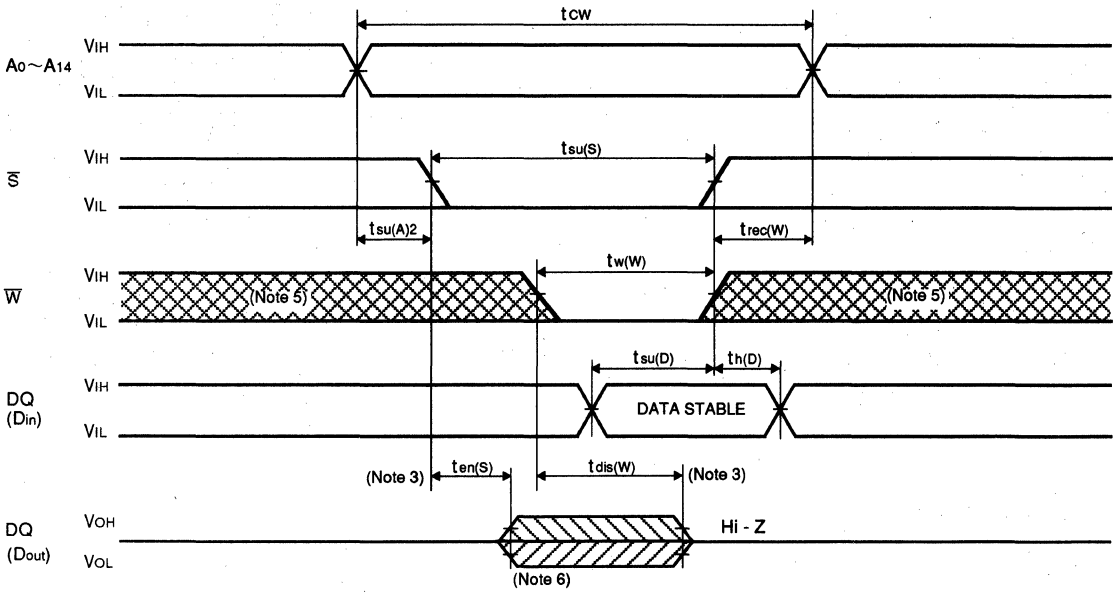
(5) TIMING DIAGRAMS FOR WRITE CYCLE

Write cycle 1 ($\overline{W}$ control mode)



Note 5. Hatching indicates the state is don't care.

Write cycle 2 ($\overline{S}$ control mode)



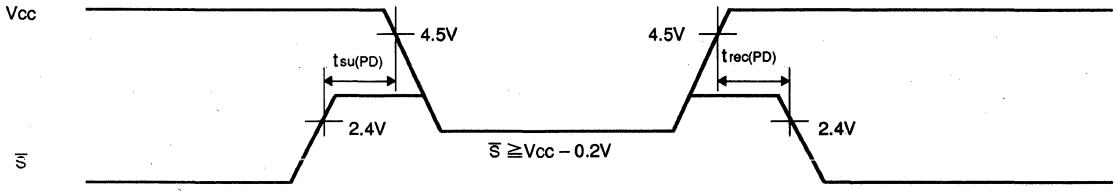
Note 6. When the falling edge of $\overline{W}$ is simultaneous or prior to the falling edge of $\overline{S}$, the output is maintained in the high impedance.
7. ten,tdis are periodically sampled and are not 100% tested.

POWER DOWN CHARACTERISTICS (Ta = 0~70℃, Vcc=5V±10%, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ	Max	
$V_{CC(PD)}$	Power down supply voltage	$V_{I(S)} \geqq V_{CC} - 0.2V$		2			V
$V_{I(S)}$	Chip select input voltage	$V_I \geqq V_{CC} - 0.2V$ or		Vcc-0.2			V
$t_{su(PD)}$	Power down setup time	$0V \leqq V_I \leqq 0.2V$		0			ns
$t_{rec(PD)}$	Power down recovery time		-15L	15			ns
			-20L	20			
$I_{CC(PD)}$	Power down supply current	Vcc = 3.0V				50	μA

Note 8. This is only M5M5278DP,J,FP,VP -15L,-20L.

TIMING WAVEFORM FOR POWER DOWN



M5M51001BP,J-15,-20,-25,-20L,-25L

1048576-BIT(1048576-WORD BY 1-BIT)CMOS STATIC RAM

DESCRIPTION

The M5M51001BP,J are a family of 1048576-word by 1-bit static RAMs, fabricated with the high performance CMOS silicon gate process and designed for high-speed application.

The M5M51001BP,J are offered in a 28-pin plastic dual-in-line package (DIP), 28-pin plastic small outline J-lead package (SOJ).

These devices operate on a single 5V supply, and are directly TTL compatible. They include power down feature as well.

FEATURES

Type name	Access time (max)	Power supply current	
		Active (max)	Stand-by (max)
M5M51001BP, J - 15	15ns	180mA	10mA
M5M51001BP, J - 20	20ns	160mA	10mA
M5M51001BP, J - 20L			100μA
M5M51001BP, J - 25	25ns	140mA	10mA
M5M51001BP, J - 25L			100μA

- Single +5V power supply
- Fully static operation : No clocks, No refresh
- Power down by $\overline{S}$
- Easy memory expansion by $\overline{S}$
- Three-state outputs : OR-tie capability
- Directly TTL compatible : All inputs and outputs
- TEST MODE is available

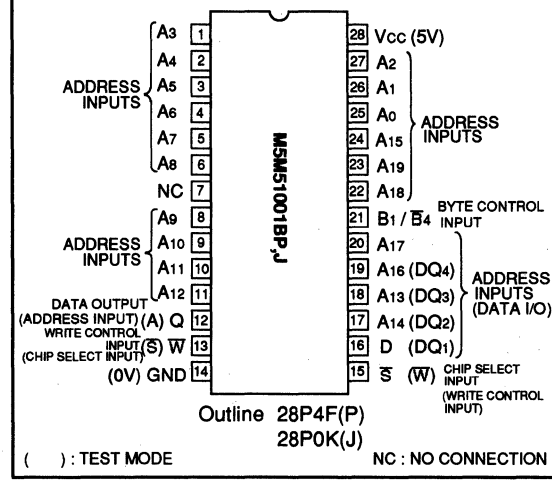
PACKAGE

M5M51001BP ..... 28pin 400mil DIP
M5M51001BJ ..... 28pin 400mil SOJ

APPLICATION

High speed memory units

PIN CONFIGURATION (TOP VIEW)



FUNCTION

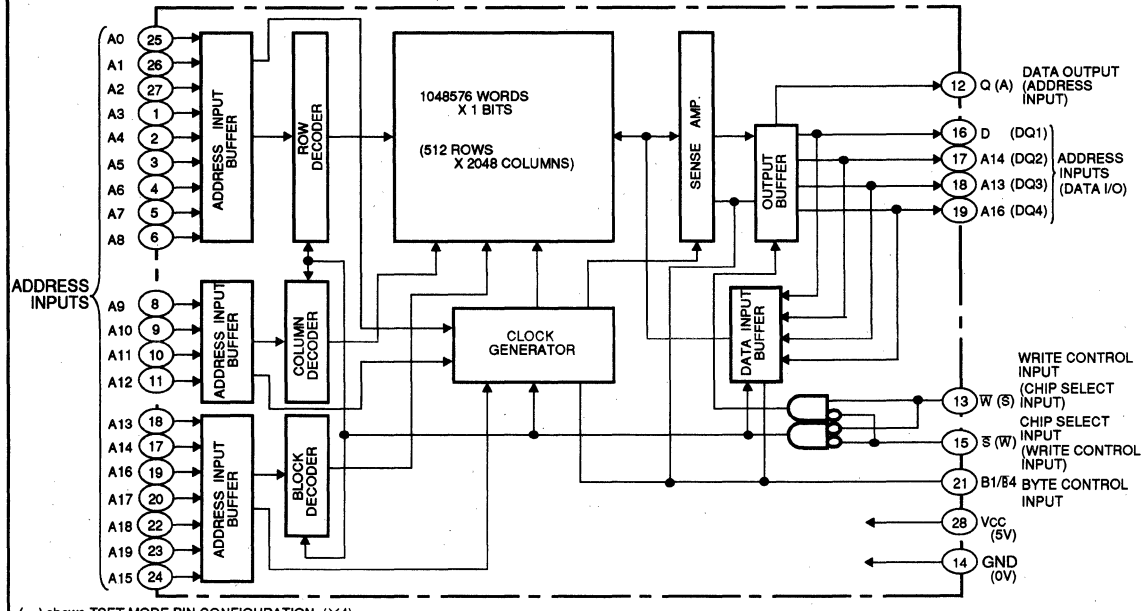
The operation mode of the M5M51001B series is determined by a combination of the device control inputs $\overline{S}$ and $\overline{W}$. Each mode is summarized in the function table shown in next page.

The RAM works with an organization of 1048576-word by 1-bit, when B1/$\overline{B4}$ is high of floating. And an organizaiton of 262144-word by 4-bit is also obtained for reducing the test time, when B1/$\overline{B4}$ is low.

A write cycle is executed whenever the low level $\overline{W}$ overlaps with the low level $\overline{S}$. The address must be set up before the write cycle and must be stable during the entire cycle.

The data is latched into a cell on the trailing edge of $\overline{W}$, $\overline{S}$

BLOCK DIAGRAM



whichever occurs first, requiring the set-up and hold time relative to these edge to be maintained. When $\overline{S}$ is high, the chip is non-selectable state, disabling both reading and writing. In the case, the output stage is in a high-impedance state.

A read cycle is executed by setting $\overline{W}$ at a high level while $\overline{S}$ are in an active state ($\overline{S}$ = L)

When setting $\overline{S}$ at a high level, the chip is in a non - selectable mode in which both reading and write are disabled.

In this mode, the output stage is in a high-impedance state, allowing OR-tie with other chips and memory expansion by $\overline{S}$.

Signal-$\overline{S}$ controls the power-down feature. When $\overline{S}$ goes high, power dissipation is reduced extremely. The access time from $\overline{S}$ is equivalent to the address access time.

FUNCTION TABLE

$\overline{S}$	$\overline{W}$	Mode	Q	D	Icc
H	X	Non selection	High-impedance	High-impedance	Stand-by
L	L	Write	Din	High-impedance	Active
L	H	Read	High-impedance	Dout	Active

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to GND	−3.5 *~7	V
V_I	Input voltage	With respect to GND	−3.5 *~ Vcc + 0.3	V
V_O	Output voltage	With respect to GND	−3.5 *~7	V
P_d	Power dissipation	Ta=25℃	1000	mW
T_{opr}	Operating temperature		0 ~70	℃
$T_{stg(bias)}$	Storage temperature (bias)		−10~85	℃
T_{stg}	Storage temperature		−65 ~ 150	℃

* Pulse width≦20ns, in case of DC : −0.5V

DC ELECTRICAL CHARACTERISTICS (Ta=0~70℃, Vcc=5V±10%, unless otherwise noted)

Symbol	Parameter	Test conditions			Limits Min	Limits Typ	Limits Max	Unit
V_{IH}	High-level input voltage				2.2		Vcc+0.3	V
V_{IL}	Low-level input voltage				−0.3*		0.8	V
V_{OH}	High-level output voltage	I_{OH}=−4mA			2.4			V
V_{OL}	Low-level output voltage	I_{OL}=8mA					0.4	V
I_I	Input current	V_I=0~Vcc					2	μA
I_{OZ}	Output current in off-state	$V_{I(\overline{S})}=V_{IH}$, V_{IO}=0 ~ Vcc					10	μA
I_{CC1}	Active supply current (TTL level)	$V_{I(\overline{S})}=V_{IL}$, other inputs=$V_{IH}$ or V_{IL}, Output-open(duty 100%)	AC	15ns cycle			180	mA
				20ns cycle			160	
				25ns cycle			140	
			DC			60	75	
I_{CC2}	Stand-by supply current (TTL level)	$V_{I(\overline{S})}=V_{IH}$	AC (min cycle)				40	mA
			DC				30	
I_{CC3}	Stand-by current (MOS level)	$V_{I(\overline{S})}\geqq V_{CC}-0.2V$, other inputs $V_I\leqq 0.2V$ or $V_I\geqq V_{CC}-0.2V$	-15,-20,-25			1	10	mA
			-20L,-25L			10	100	μA

* Pulse width≦20ns, in case of AC : −3.0V

CAPACITANCE (Ta = 0 ~ 70℃, Vcc = 5V±10%, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits Min	Limits Typ	Limits Max	Unit
C_I	Input capacitance	V_I=GND, V_I=25mVrms, f=1MHz			6	pF
C_O	Output capacitance	V_O=GND, V_O=25mVrms, f=1MHz			6	pF

Note 1: Direction for current flowing into an IC is positive (no mark).
2: Typical value is Vcc=5V, Ta=25℃
3: C_I, C_O are periodically sampled and are not 100% tested.

AC ELECTRICAL CHARACTERISTICS (Ta = 0～70℃, Vcc = 5V±10%, unless otherwise noted)

(1) MEASUREMENT CONDITIONS

Input pulse level ····· V_{IH} = 3.0V, V_{IL} = 0.0V
Input rise and fall time ····· 3ns
Input timing reference level ····· V_{IH} = 1.5V, V_{IL} = 1.5V
Output timing reference level ····· V_{OH} = 1.5V, V_{OL} =1.5V
Output loads ····· Fig1,Fig2

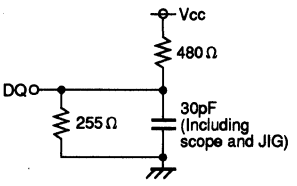


Fig.1 Output load

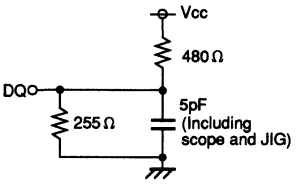


Fig.2 Output load for t_{en}, t_{dis}

(2) READ CYCLE

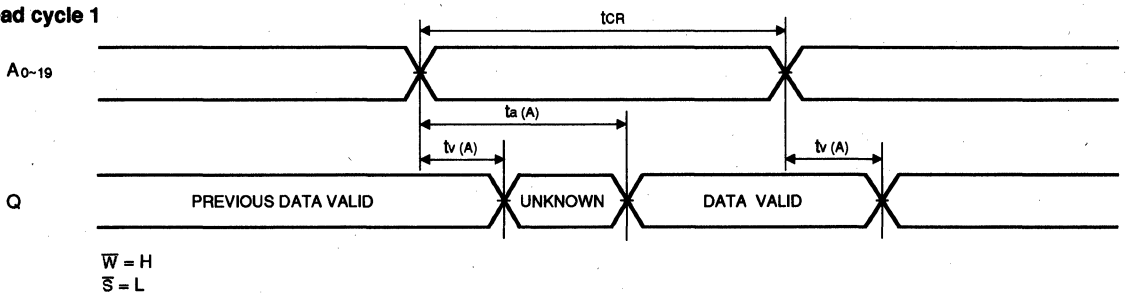
Symbol	Parameter	Limits						Unit
		M5M51001B-15		M5M51001B-20,-20L		M5M51001B-25,-25L		
		Min	Max	Min	Max	Min	Max	
t_{CR}	Read cycle time	15		20		25		ns
$t_{a(A)}$	Address access time		15		20		25	ns
$t_{a(S)}$	Chip select access time		15		20		25	ns
$t_{dis(S)}$	Output disable time after $\overline{S}$ high	0	7	0	7	0	8	ns
$t_{en(S)}$	Output enable time after $\overline{S}$ low	6		6		6		ns
$t_{v(A)}$	Data valid time after address change	7		7		7		ns
t_{PU}	Power-up time after $\overline{S}$ low	0		0		0		ns
t_{PD}	Power-down time after $\overline{S}$ high		15		20		25	ns

(3) WRITE CYCLE

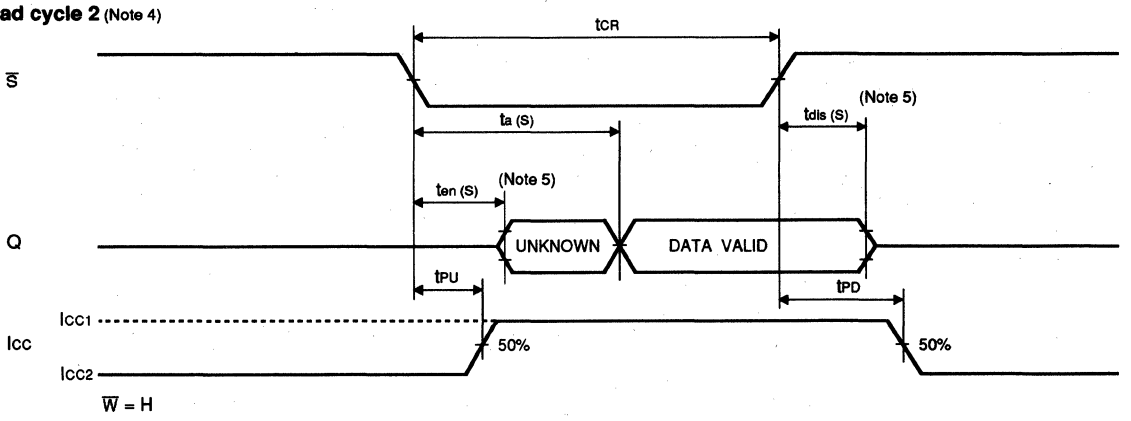
Symbol	Parameter	Limits						Unit
		M5M51001B-15		M5M51001B-20,-20L		M5M51001B-25,-25L		
		Min	Max	Min	Max	Min	Max	
t_{CW}	Write cycle time	15		20		25		ns
$t_{w(W)}$	Write pulse width	12		15		20		ns
$t_{su(A)}$	Address setup time	0		0		0		ns
$t_{su(A-\overline{W}H)}$	Address setup time with respect to $\overline{W}$	12		15		20		ns
$t_{su(S)}$	Chip select setup time	12		15		20		ns
$t_{su(D)}$	Data setup time	8		12		15		ns
$t_{h(D)}$	Data hold time	0		0		0		ns
$t_{rec(W)}$	Write recovery time	0		0		0		ns
$t_{dis(W)}$	Output disable time after $\overline{W}$ low	0	7	0	7	0	8	ns
$t_{en(W)}$	Output enable time after $\overline{W}$ high	0		0		0		ns

(4) TIMING DIAGRAMS

Read cycle 1

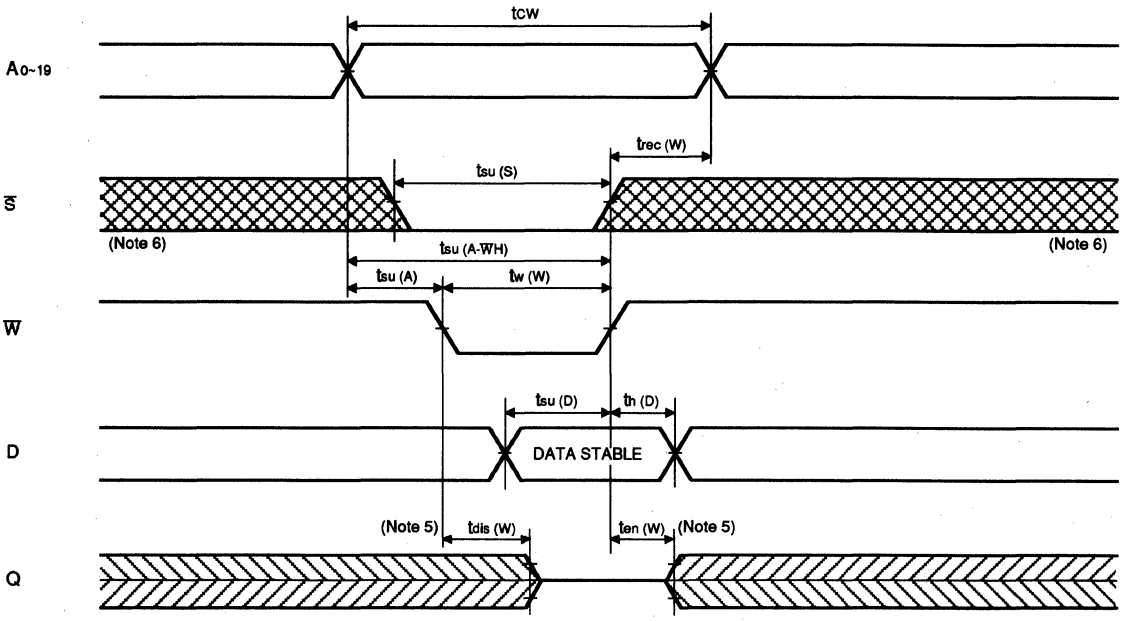


Read cycle 2 (Note 4)

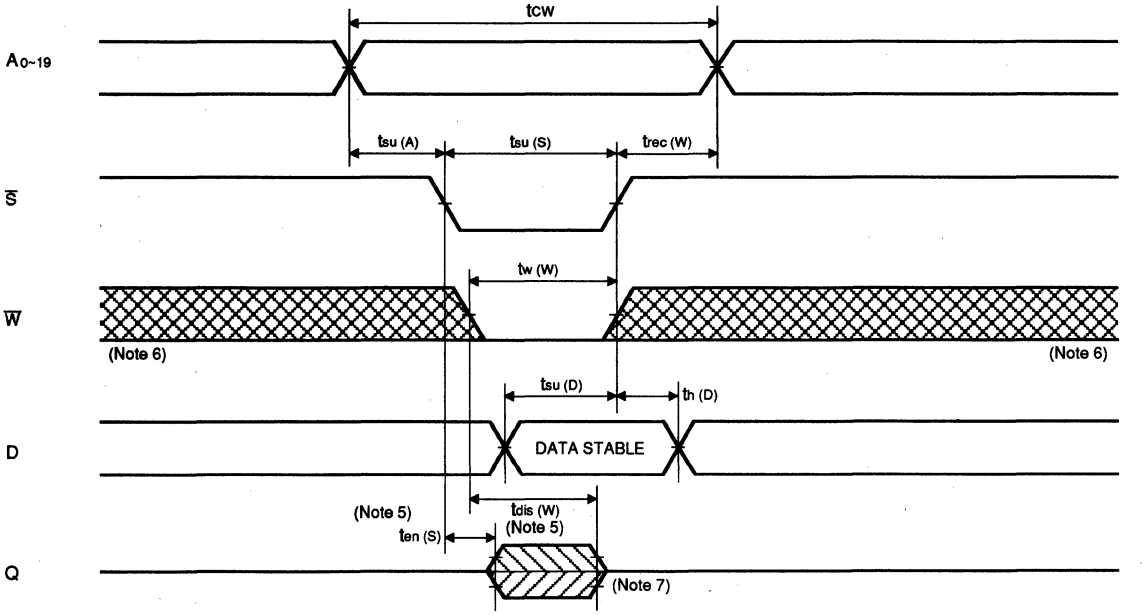


Note 4 : Addresses valid prior to or coincident with S transition low.
5 : Transition is measured ±500mV from steady state voltage with specified loading in Figure 2.

Write cycle ($\overline{W}$ control mode)



Write cycle ($\overline{S}$ control mode)



Note 5 : Hatching indicates the state is don't care.

6 : When the falling edge of $\overline{W}$ is simultaneous or prior to the falling edge of $\overline{S}$, the output is maintained in the high impedance.

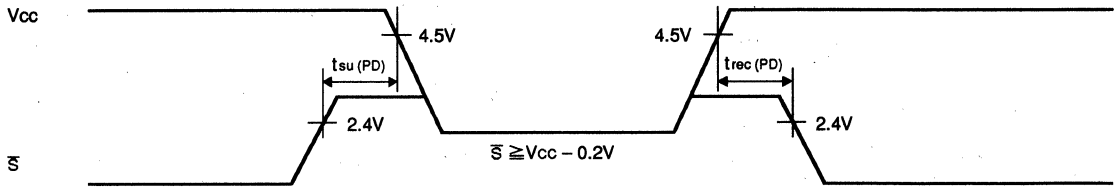
7 : t_{en}, t_{dis} are periodically sampled and are not 100% tested.

POWER DOWN CHARACTERISTICS (Ta = 0~70℃, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ	Max	
V_{CC} (PD)	Power down supply voltage			2			V
V_I ($\overline{S}$)	Chip select input voltage	V_I ($\overline{S}$) ≧ Vcc − 0.2V		Vcc − 0.2			V
t_{su} (PD)	Power down setup time	V_I ≧ Vcc − 0.2V or		0			ns
t_{rec} (PD)	Power down recovery time	0V ≦ V_I ≦ 0.2V	-20L	20			ns
			-25L	25			
I_{CC} (PD)	Power down supply current	Vcc = 3.0V				50	μA
		Vcc = 5.5V				100	

Note 8 : This is only M5M51001BP, J-20L, -25L.

TIMING WAVEFORM FOR POWER DOWN



M5M51004BP,J-15,-20,-25,-20L,-25L

1048576-BIT(262144-WORD BY 4-BIT)CMOS STATIC RAM

DESCRIPTION

The M5M51004BP,J are a family of 262144-word by 4-bit static RAMs, fabricated with the high performance CMOS silicon gate process and designed for high-speed application.

The M5M51004BP,J are offered in a 28-pin plastic dual-in-line package (DIP), 28-pin plastic small outline J-lead package (SOJ).

These devices operate on a single 5V supply, and are directly TTL compatible. They include power down feature as well.

FEATURES

Type name	Access time (max)	Power supply current	
		Active (max)	Stand-by (max)
M5M51004BP, J - 15	15ns	180mA	10mA
M5M51004BP, J - 20	20ns	160mA	
M5M51004BP, J - 20L			100µA
M5M51004BP, J - 25	25ns	140mA	10mA
M5M51004BP, J - 25L			100µA

- Single +5V power supply
- Fully static operation : No clocks, No refresh
- Common data I/O
- Easy memory expansion by $\overline{S}$
- Three-state outputs : OR-tie capability
- $\overline{OE}$ prevents data contention in the I/O bus
- Directly TTL compatible : All inputs and outputs

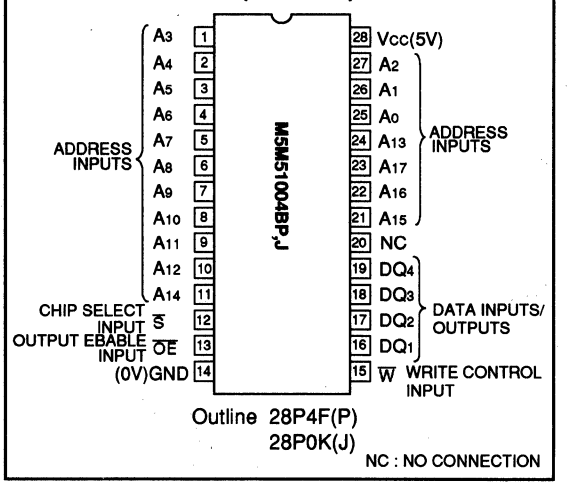
PACKAGE

M5M51004BP ..... 28pin 400mil DIP
M5M51004BJ ..... 28pin 400mil SOJ

APPLICATION

High speed memory units

PIN CONFIGURATION (TOP VIEW)



Outline 28P4F(P)
28P0K(J)

NC : NO CONNECTION

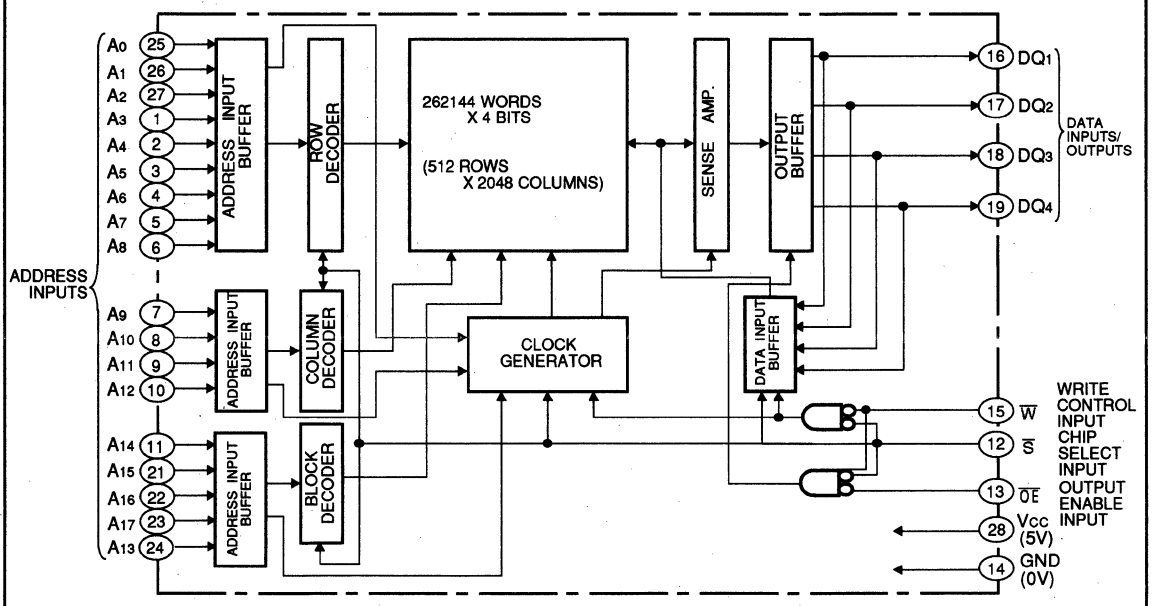
FUNCTION

The operation mode of the M5M51004B series is determined by a combination of the device control inputs $\overline{S}$, $\overline{W}$. Each mode is summarized in the function table shown in next page.

A write cycle is executed whenever the low level $\overline{W}$ overlaps with the low level $\overline{S}$. The address must be set-up before the write cycle and must be stable during the entire cycle.

The data is latched into a cell on the trailing edge of $\overline{W}$, $\overline{S}$, whichever occurs first, requiring the set-up and hold time relative to these edge to be maintained. The output enable input $\overline{OE}$ directly controls the output stage. Setting the $\overline{OE}$ at a high level, the output stage is in a high-impedance state, and the data bus contention problem in the write cycle is eliminated.

BLOCK DIAGRAM



A read cycle is executed by setting $\overline{W}$ at a high level and $\overline{OE}$ at a low level while $\overline{S}$ are in an active state ($\overline{S}$ = L)

When setting $\overline{S}$ at a high level, the chip is in a non-selectable mode in which both reading and write are disabled. In this mode, the output stage is in a high-impedance state, allowing OR-tie with other chips and memory expansion by $\overline{S}$.

Signal-S controls the power-down feature. When $\overline{S}$ goes high, power dissipation is reduced extremely. The access time from $\overline{S}$ is equivalent to the address access time.

FUNCTION TABLE

$\overline{S}$	$\overline{W}$	$\overline{OE}$	Mode	DQ	Icc
H	X	X	Non selection	High-impedance	Stand-by
L	L	X	Write	Din	Active
L	H	L	Read	Dout	Active
L	H	H		High-impedance	Active

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to GND	−3.5* ~7	V
V_I	Input voltage		−3.5* ~ Vcc + 0.3	V
V_O	Output voltage		−3.5* ~ 7	V
P_d	Power dissipation	Ta=25℃	1000	mW
T_{opr}	Operating temperature		0 ~70	℃
$T_{stg(bias)}$	Storage temperature (bias)		−10~85	℃
T_{stg}	Storage temperature		−65 ~ 150	℃

* Pulse width≦20ns, in case of DC : −0.5V

DC ELECTRICAL CHARACTERISTICS (Ta=0~70℃, Vcc=5V±10%, unless otherwise noted)

Symbol	Parameter	Test conditions			Limits Min	Limits Typ	Limits Max	Unit
V_{IH}	High-level input voltage				2.2		Vcc+0.3V	V
V_{IL}	Low-level input voltage				−0.3*		0.8	V
V_{OH}	High-level output voltage	I_{OH}=−4mA			2.4			V
V_{OL}	Low-level output voltage	I_{OL}=8mA					0.4	V
I_I	Input current	V_I=0~Vcc					2	μA
I_{OZ}	Output current in off-state	$V_{I(\overline{S})}=V_{IH}$ $V_{I/O}$= 0 ~ Vcc					10	μA
I_{CC1}	Active supply current (TTL level)	$V_{I(\overline{S})}=V_{IL}$ other inputs=V_{IH} or V_{IL} Output-open(duty 100%)	AC	15ns cycle			180	mA
				20ns cycle			160	
				25ns cycle			140	
			DC			60	75	
I_{CC2}	Stand-by supply current (TTL level)	$V_{I(\overline{S})}=V_{IH}$	AC (min cycle)				40	mA
			DC				30	
I_{CC3}	Stand-by current (MOS level)	$V_{I(\overline{S})}$ ≧Vcc − 0.2V other inputs V_I≦0.2V or V_I≧Vcc − 0.2V	-15,-20,-25			1	10	mA
			-20L,-25L			10	100	μA

* Pulse width≦20ns, in case of AC : −3.0V

CAPACITANCE (Ta = 0 ~ 70℃, Vcc = 5V±10%, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits Min	Limits Typ	Limits Max	Unit
C_I	Input capacitance	V_I=GND, V_I=25mVrms, f=1MHz			6	pF
C_O	Output capacitance	V_O=GND, V_O=25mVrms, f=1MHz			6	pF

Note 1: Direction for current flowing into an IC is positive (no mark).
2: Typical value is Vcc=5V, Ta=25℃
3: C_I, C_O are periodically sampled and are not 100% tested.

AC ELECTRICAL CHARACTERISTICS (Ta = 0~70℃, Vcc = 5V±10%, unless otherwise noted)

(1) MEASUREMENT CONDITIONS

Input pulse levels ····· V_{IH} = 3.0V, V_{IL} = 0.0V
Input rise and fall time ····· 3ns
Input timing reference levels ····· V_{IH} = 1.5V, V_{IL} = 1.5V
Reference levels ····· V_{OH} = 1.5V, V_{OL} = 1.5V
Output loads ····· Fig1,Fig2

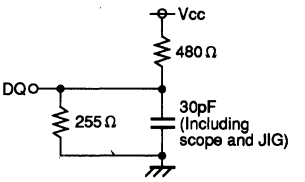


Fig.1 Output load

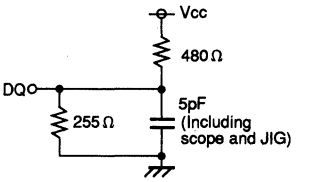


Fig.2 Output load for t_{en}, t_{dis}

(2) READ CYCLE

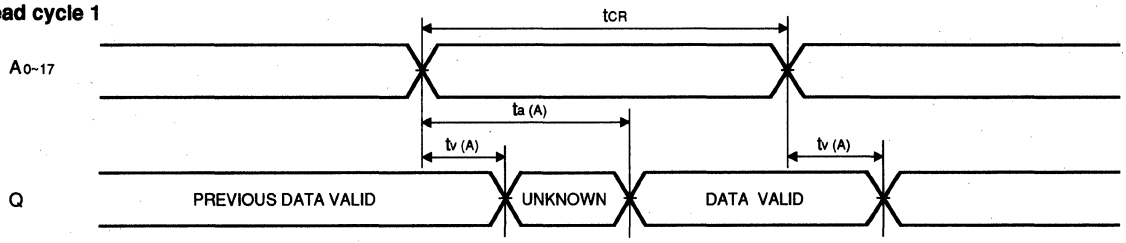
Symbol	Parameter	Limits						Unit
		M5M51004B-15		M5M51004B-20,-20L		M5M51004B-25,-25L		
		Min	Max	Min	Max	Min	Max	
t_{CR}	Read cycle time	15		20		25		ns
$t_{a(A)}$	Address access time		15		20		25	ns
$t_{a(S)}$	Chip select access time		15		20		25	ns
$t_{a(OE)}$	Output enable access time		8		10		13	ns
$t_{dis(S)}$	Output disable time after $\overline{S}_1$ high	0	7	0	7	0	8	ns
$t_{dis(OE)}$	Output disable time after $\overline{OE}$ high	0	7	0	7	0	8	ns
$t_{en(S)}$	Output enable time after $\overline{S}$ low	6		6		6		ns
$t_{en(OE)}$	Output enable time after $\overline{OE}$ low	0		0		0		ns
$t_{v(A)}$	Data valid time after address change	7		7		7		ns
t_{PU}	Power-up time after chip selection	0		0		0		ns
t_{PD}	Power-down time after chip selection		15		20		25	ns

(3) WRITE CYCLE

Symbol	Parameter	Limits						Unit
		M5M51004B-15		M5M51004B-20,-20L		M5M51004B-25,-25L		
		Min	Max	Min	Max	Min	Max	
t_{CW}	Write cycle time	15		20		25		ns
$t_{w(W)}$	Write pulse width	12		15		20		ns
$t_{su(A)}$	Address setup time	0		0		0		ns
$t_{su(A-\overline{W}H)}$	Address setup time with respect to $\overline{W}$	12		15		20		ns
$t_{su(S)}$	Chip select setup time	12		15		20		ns
$t_{su(D)}$	Data setup time	8		12		15		ns
$t_{h(D)}$	Data hold time	0		0		0		ns
$t_{rec(W)}$	Write recovery time	0		0		0		ns
$t_{dis(W)}$	Output disable time after $\overline{W}$ low	0	7	0	7	0	8	ns
$t_{dis(OE)}$	Output disable time after $\overline{OE}$ high	0	7	0	7	0	8	ns
$t_{en(W)}$	Output enable time after $\overline{W}$ high	0		0		0		ns
$t_{en(OE)}$	Output enable time after $\overline{OE}$ low	0		0		0		ns

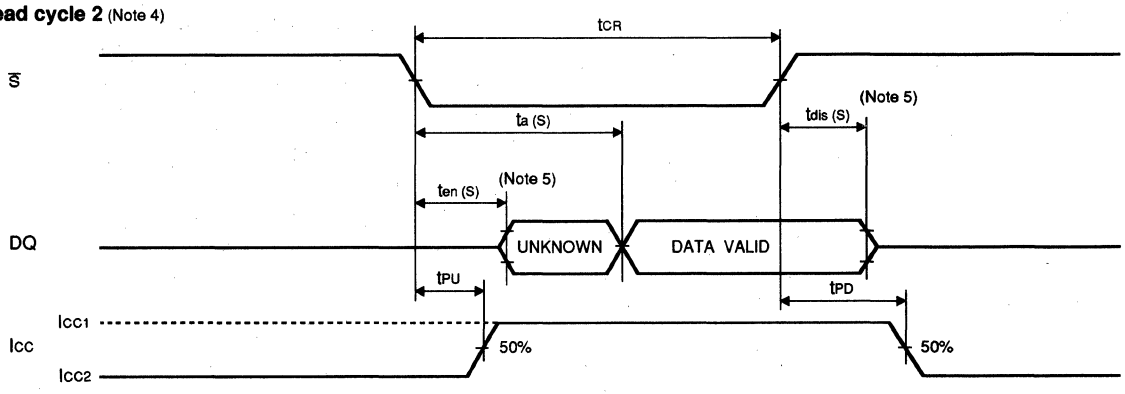
(4) TIMING DIAGRAMS

Read cycle 1



$\overline{W}$ = H
$\overline{S}$ = L
$\overline{OE}$ = L

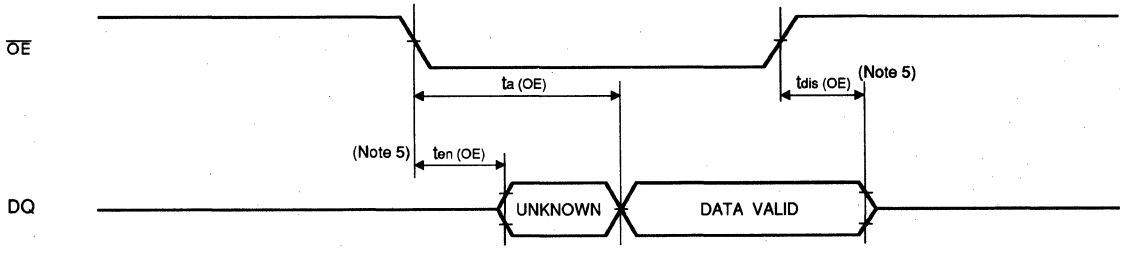
Read cycle 2 (Note 4)



$\overline{W}$ = H
$\overline{OE}$ = L

Note 4 : Addresses valid prior to or coincident with $\overline{S}$ transition low.
5 : Transition is measured ±500mV from steady state voltage with specified loading in Figure 2.

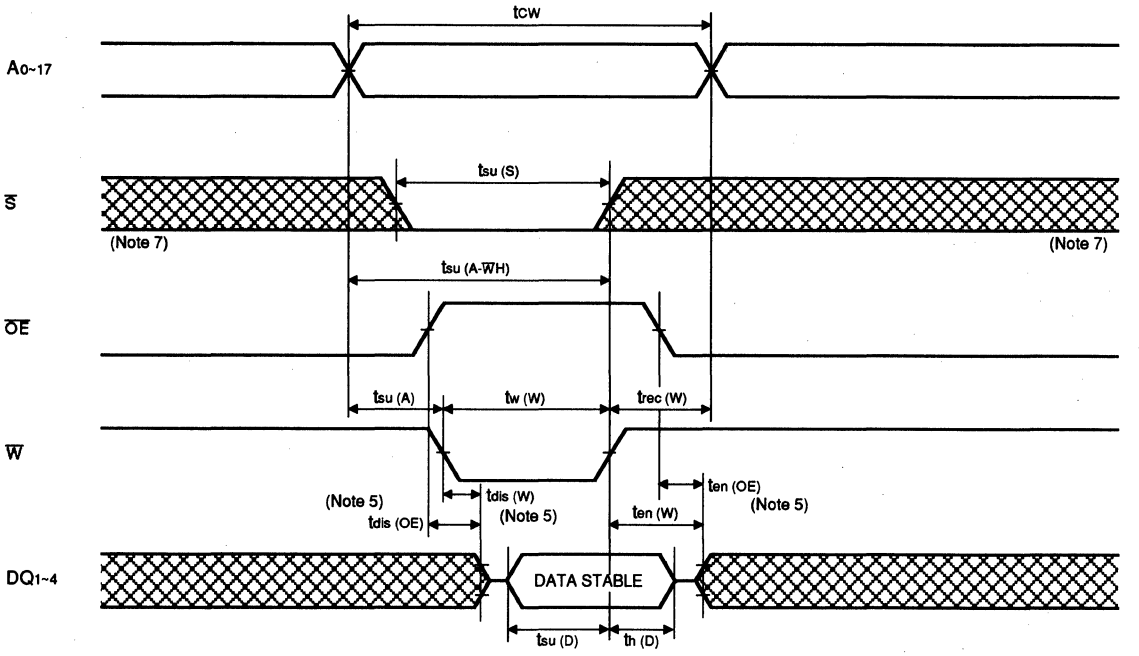
Read cycle 3 (Note 6)



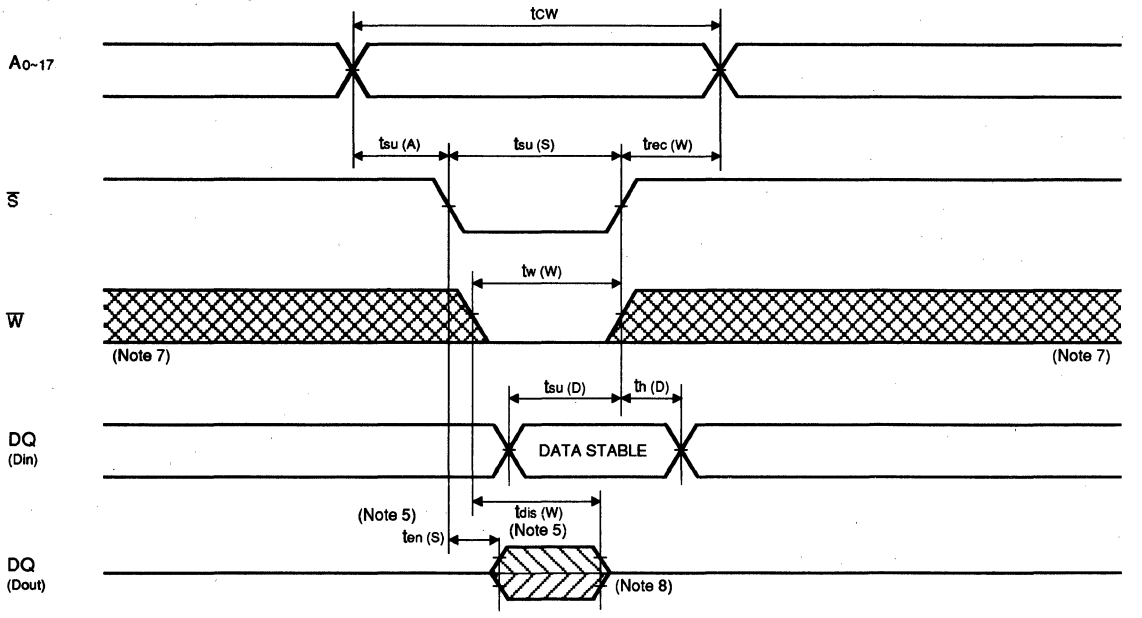
$\overline{W}$ = H
$\overline{S}$ = L

Note 6 : Addresses and $\overline{S}$ valid prior to $\overline{OE}$ transition low by (ta (A)-ta (OE)), (ta (S)-ta (OE))

Write cycle ($\overline{W}$ control mode)



Write cycle ($\overline{S}$ control mode)



Note 7 : Hatching indicates the state is don't care.

8 : When the falling edge of $\overline{W}$ is simultaneous or prior to the falling edge of $\overline{S}$, the output is maintained in the high impedance.

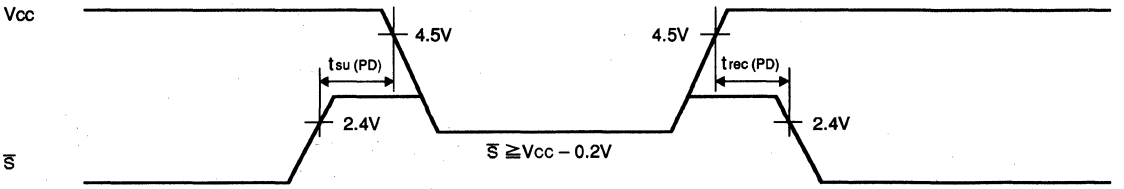
9 : t_{en}, t_{dis} are periodically sampled and are not 100% tested.

POWER DOWN CHARACTERISTICS (Ta = 0~70℃, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ	Max	
$V_{CC\ (PD)}$	Power down supply voltage	$V_{I(\overline{S})} \geqq V_{CC} - 0.2V$ $V_I \geqq V_{CC} - 0.2V$ or $0V \leqq V_I \leqq 0.2V$		2			V
$V_{I(\overline{S})}$	Chip select input voltage			$V_{CC} - 0.2$			V
$t_{su\ (PD)}$	Power down setup time			0			ns
$t_{rec\ (PD)}$	Power down recovery time		-20L	20			ns
			-25L	25			
$I_{CC\ (PD)}$	Power down supply current	$V_{CC} = 3.0V$				50	μA
		$V_{CC} = 5.5V$				100	

Note 10 : This is only M5M51004BP, J-20L, -25L.

TIMING WAVEFORM FOR POWER DOWN



M5M51288BKP,KJ-15,-20,-25,-20L,-25L
M5M51288BVP-20,-25,-20L,-25L

1048576-BIT(131072-WORD BY 8-BIT)CMOS STATIC RAM

DESCRIPTION

The M5M51288BKP,KJ,VP are a family of 131072-word by 8-bit static RAMs, fabricated with the high performance CMOS silicon gate process and designed for high-speed application.

The M5M51288BKP,KJ,VP are offered in a 32-pin plastic dual-in-line package(DIP), 32-pin plastic small outline J-lead package(SOJ), 32-pin thin small outline package (TSOP).

These devices operate on a single 5V supply, and are directly TTL compatible. They include power down feature as well.

FEATURES

Type name	Access time (max)	Power supply current	
		Active (max)	Stand-by (max)
M5M51288BKP,KJ - 15	15ns	190 mA	10mA
M5M51288BKP,KJ ,VP - 20	20ns	170 mA	
M5M51288BKP,KJ ,VP - 20L			100 μA
M5M51288BKP,KJ ,VP - 25	25ns	150 mA	10mA
M5M51288BKP,KJ ,VP - 25L			100 μA

- Single +5V power supply
- Fully static operation : No clocks, No refresh
- Common data I/O
- Easy memory expansion by $\overline{S}_1$,S_2
- Three-state outputs : OR-tie capability
- $\overline{OE}$ prevents data contention in the I/O bus
- Directly TTL compatible : All inputs and outputs

PACKAGE

M5M51288BKP ..... 32pin 300mil DIP
M5M51288BKJ ..... 32pin 300mil SOJ
M5M51288BVP ..... 32pin 8×20mm^2 TSOP(I)

APPLICATION

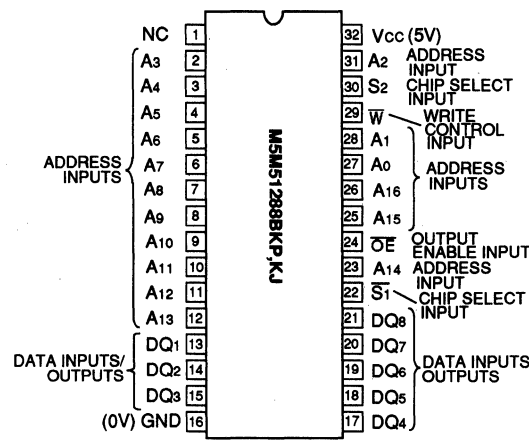
High speed memory units

FUNCTION

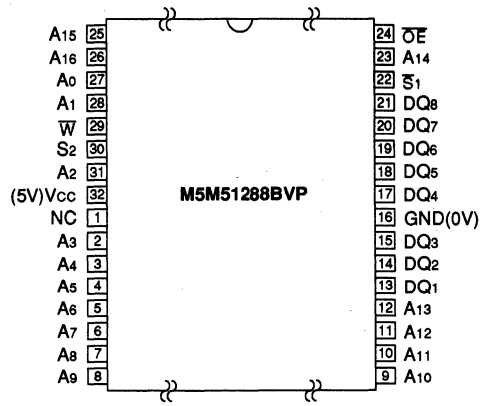
The operation mode of the M5M51288B series is determined by a combination of the device control inputs $\overline{S}_1$,S_2,$\overline{W}$ and $\overline{OE}$. Each mode is summarized in the function table shown in next page.

A write cycle is executed whenever the low level $\overline{W}$ overlaps with the low level $\overline{S}_1$ and the high level S_2. The address must be set up before the write cycle and must be stable during the entire cycle. The data is latched into a cell on the trailing edge of $\overline{W}$, $\overline{S}_1$ or S_2, whichever occurs first, requiring the set-up and hold time relative to these edge to be maintained. The output enable input $\overline{OE}$ directly controls the output stage. Setting the $\overline{OE}$ at a high level, the output stage is in a high-impedance state, and the data bus contention problem in the write cycle is eliminated.

PIN CONFIGURATION (TOP VIEW)



Outline 32P4Y(KP)
32P0J(KJ)



Outline 32P3H-E

NC : NO CONNECTION

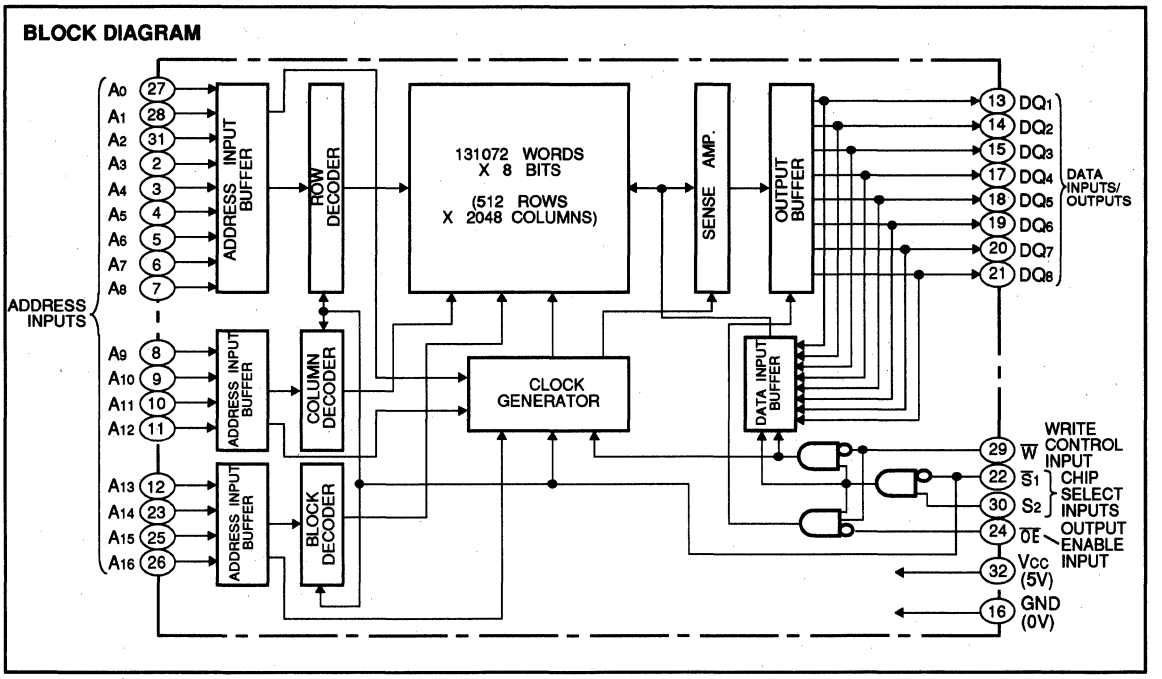
A read cycle is executed by setting $\overline{W}$ at a high level and $\overline{OE}$ at a low level while $\overline{S}_1$ and S_2 are in an active state ($\overline{S}_1$=L,S_2=H)

When setting $\overline{S}_1$ at a high level or S_2 at a low level,the chip is in a non-selectable mode in which both reading and writing are disabled.In this mode,the output stage is in a high-impedance state,allowing OR -tie with other chips and memory expansion by $\overline{S}_1$ and S_2.

FUNCTION TABLE

$\overline{S}_1$	S_2	$\overline{W}$	$\overline{OE}$	Mode	DQ	Icc
X	L	X	X	Non selection	High-impedance	Active
H	X	X	X	Non selection	High-impedance	Stand-by
L	H	L	X	Write	Din	Active
L	H	H	L	Read	Dout	Active
L	H	H	H		High-impedance	Active

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to GND	−3.5* ~7	V
V_I	Input voltage		−3.5* ~Vcc + 0.3	V
V_O	Output voltage		−3.5* ~Vcc + 0.3	V
P_d	Power dissipation	Ta=25℃	1000	mW
T_{opr}	Operating temperature		0~70	℃
$T_{stg(bias)}$	Storage temperature(bias)		−10~85	℃
T_{stg}	Storage temperature		−65~150	℃

*Pulse width≦20ns, in case of DC: −0.5V

DC ELECTRICAL CHARACTERISTICS (Ta=0~70℃, Vcc=5V±10%, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits Min	Limits Typ	Limits Max	Unit
V_{IH}	High-level input voltage			2.2		Vcc+0.3V	V
V_{IL}	Low-level input voltage			−0.3*		0.8	V
V_{OH}	High-level output voltage	I_{OH}=−4mA		2.4			V
V_{OL}	Low-level output voltage	I_{OL}=8mA				0.4	V
I_I	Input current	V_I=0~Vcc				2	μA
| I_{OZ} |	Output current in off-state	$V_{I(\overline{ST})}$=V_{IH}, $V_{I/O}$=0~Vcc				10	μA
I_{CC1}	Active supply current (TTL level)	$V_{I(\overline{ST})}$=V_{IL}, other inputs=V_{IH} or V_{IL}, Output-open(duty 100%)	AC (15ns cycle)			190	mA
			AC (20ns cycle)			170	
			AC (25ns cycle)			150	
			DC		70	85	
I_{CC2}	Stand-by supply current (TTL level)	$V_{I(\overline{ST})}$=V_{IH}	AC (15ns cycle)			60	mA
			AC (20/25ns cycle)			50	
			DC			35	
I_{CC3}	Stand-by current (MOS level)	$V_{I(\overline{ST})}$≧Vcc−0.2V, other inputs V_I≦0.2V or V_I≧Vcc−0.2V	-15,-20,-25		1	10	mA
			-20L,-25L		10	100	μA

*Pulse width≦20ns, in case of AC: −3.0V

CAPACITANCE (Ta=0~70℃, Vcc=5V±10%, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits Min	Limits Typ	Limits Max	Unit
C_I	Input capacitance	V_I=GND, V_I=25mVrms, f=1MHz			6	pF
C_O	Output capacitance	V_O=GND, V_O=25mVrms, f=1MHz			6	pF

Note 1: Direction for current flowing into an IC is positive (no mark).
2: Typical value is Vcc=5V, Ta=25℃
3: C_I, C_O are periodically sampled and are not 100% tested.

AC ELECTRICAL CHARACTERISTICS (Ta = 0～70℃, Vcc=5V±10%, unless otherwise noted)

(1) MEASUREMENT CONDITIONS

Input pulse levels ····· V_{IH} = 3.0V, V_{IL} = 0V
Input rise and fall time ····· 3ns
Input timing reference levels ····· V_{IH} = 1.5V, V_{IL} = 1.5V
Output timing reference levels ····· V_{OH} = 1.5V, V_{OL} =1.5V
Output loads ····· Fig1, Fig2

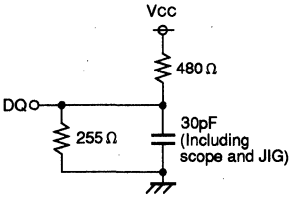


Fig.1 Output load

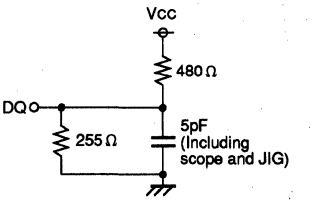


Fig.2 Output load for ten, tdis

(2) READ CYCLE

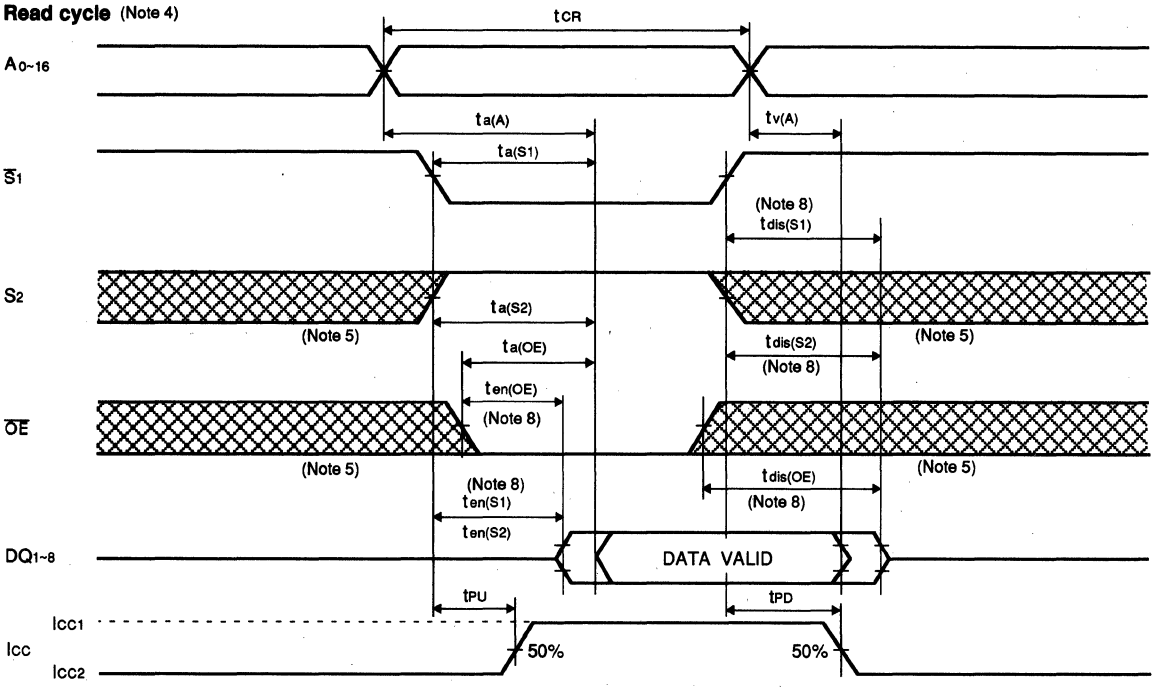
Symbol	Parameter	Limits						Unit
		M5M51288BKP,KJ-15		M5M51288BKP,KJ,VP -20, -20L		M5M51288BKP,KJ,VP -25, -25L		
		Min	Max	Min	Max	Min	Max	
t_{CR}	Read cycle time	15		20		25		ns
$t_{a(A)}$	Address access time		15		20		25	ns
$t_{a(S1)}$	Chip select 1 access time		15		20		25	ns
$t_{a(S2)}$	Chip select 2 access time		14		17		20	ns
$t_{a(OE)}$	Output enable access time		8		10		13	ns
$t_{dis(S1)}$	Output disable time after $\overline{S_1}$ high	0	7	0	7	0	8	ns
$t_{dis(S2)}$	Output disable time after S_2 low	0	7	0	7	0	8	ns
$t_{dis(OE)}$	Output disable time after $\overline{OE}$ high	0	7	0	7	0	8	ns
$t_{en(S1)}$	Output enable time after $\overline{S_1}$ low	6		6		6		ns
$t_{en(S2)}$	Output enable time after S_2 high	6		6		6		ns
$t_{en(OE)}$	Output enable time after $\overline{OE}$ low	0		0		0		ns
$t_{v(A)}$	Data valid time after address change	7		7		7		ns
t_{PU}	Power-up time after chip selection	0		0		0		ns
t_{PD}	Power-down time after chip selection		15		20		25	ns

(3) WRITE CYCLE

Symbol	Parameter	Limits						Unit
		M5M51288BKP,KJ-15		M5M51288BKP,KJ,VP -20, -20L		M5M51288BKP,KJ,VP -25, -25L		
		Min	Max	Min	Max	Min	Max	
t_{CW}	Write cycle time	15		20		25		ns
$t_{w(W)}$	Write pulse width	12		15		20		ns
$t_{su(A)1}$	Address setup time ($\overline{W}$)	0		0		0		ns
$t_{su(A)2}$	Address setup time ($\overline{S_1}$, S_2)	0		0		0		ns
$t_{su(S1)}$	Chip select 1 setup time	12		15		20		ns
$t_{su(S2)}$	Chip select 2 setup time	12		15		20		ns
$t_{su(D)}$	Data setup time	8		12		15		ns
$t_{h(D)}$	Data hold time	0		0		0		ns
$t_{rec(W)}$	Write recovery time	0		0		0		ns
$t_{dis(W)}$	Output disable time after $\overline{W}$ low	0	7	0	7	0	8	ns
$t_{dis(OE)}$	Output disable time after $\overline{OE}$ high	0	7	0	7	0	8	ns
$t_{en(W)}$	Output enable time after $\overline{W}$ high	0		0		0		ns
$t_{en(OE)}$	Output enable time after $\overline{OE}$ low	0		0		0		ns
$t_{su(A-WH)}$	Address to $\overline{W}$ high	12		15		20		ns

(4) TIMING DIAGRAMS

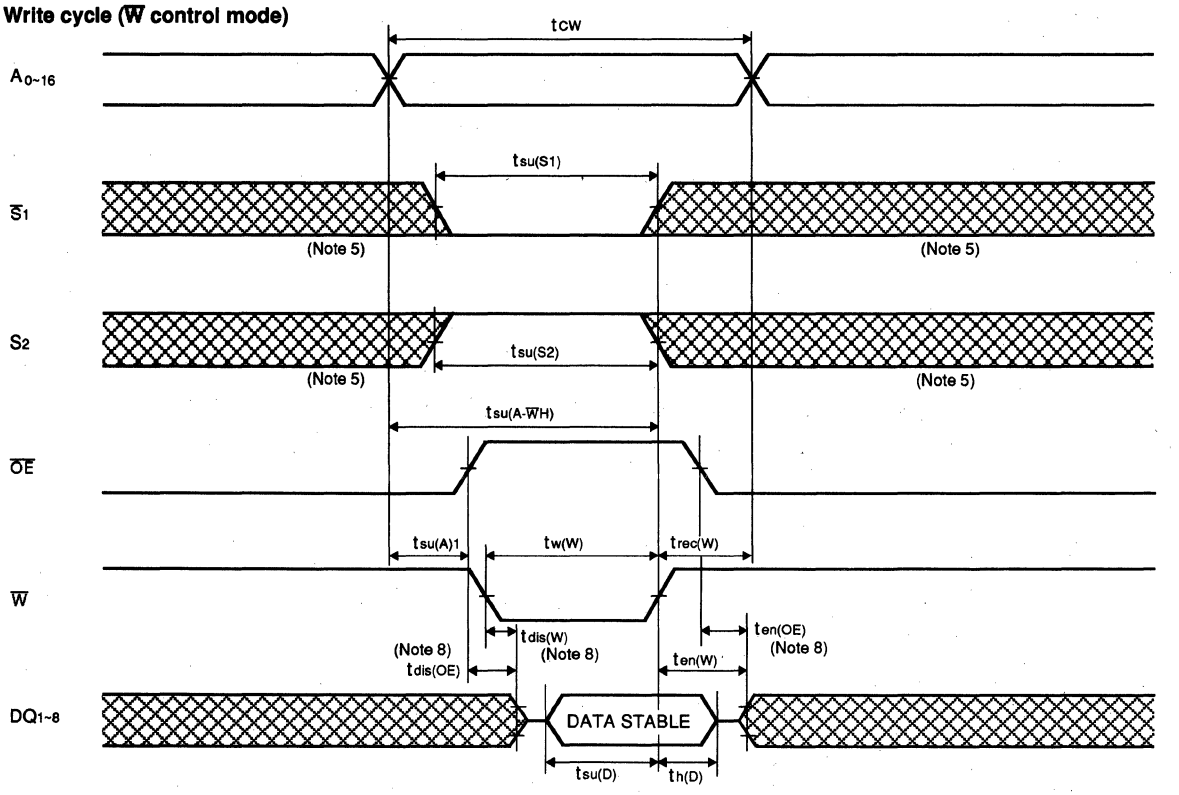
Read cycle (Note 4)



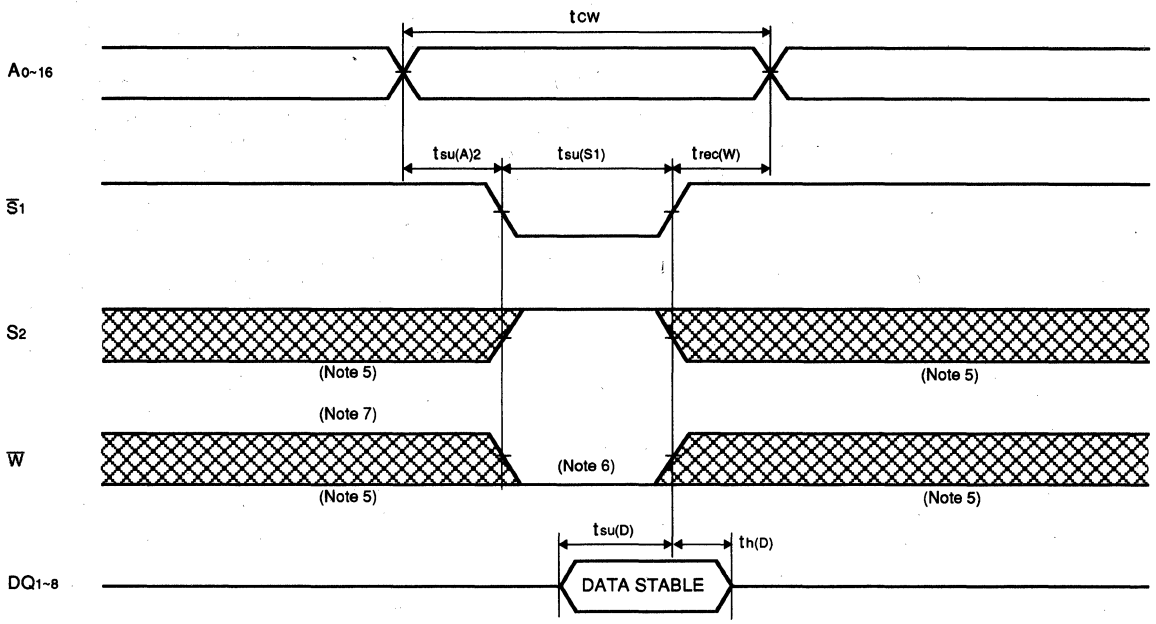
W = H

Note 4: Addresses and S1, S2 valid prior to OE transition low by (ta(A) - ta(OE)), (ta(S1) - ta(OE)), ta(S2) - ta(OE)).

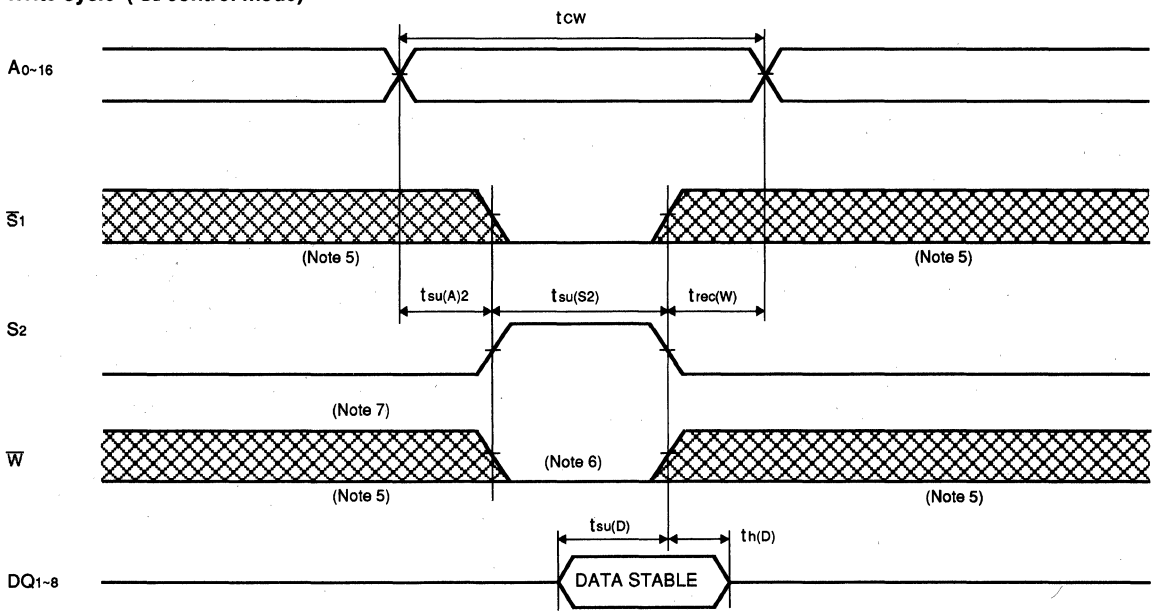
Write cycle (W control mode)



Write cycle ($\overline{S}_1$ control mode)



Write cycle (S_2 control mode)



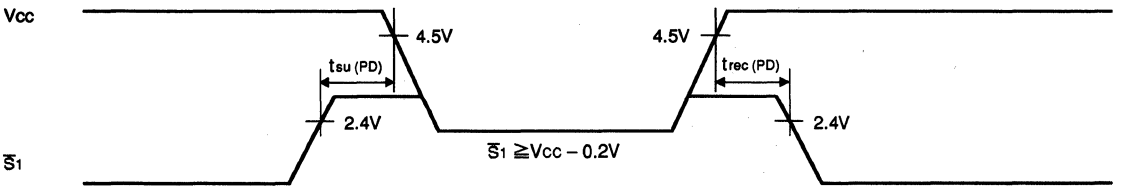
Note 5: Hatching indicates the state is "don't care".
6: Writing is executed while S2 high overlaps $\overline{S}_1$ and $\overline{W}$ low.
7: When the falling edge of $\overline{W}$ is simultaneously or prior to the falling edge of $\overline{S}_1$ or rising edge of S2, the outputs are maintained in the high impedance state.
8: Transition is measured ±500mV from steady state voltage with specified loading in Figure 2.
9: ten, tdis are periodically sampled and are not 100% tested.

POWER DOWN CHARACTERISTICS (Ta = 0~70°C, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ	Max	
$V_{CC\ (PD)}$	Power down supply voltage	$V_{I\ (\overline{S}1)} \geqq V_{CC} - 0.2V$ $V_I \geqq V_{CC} - 0.2V$ or $0V \leqq V_I \leqq 0.2V$		2			V
$V_{I\ (\overline{S}1)}$	Chip select input voltage			$V_{CC} - 0.2$			V
$t_{su\ (PD)}$	Power down setup time			0			ns
$t_{rec\ (PD)}$	Power down recovery time		-20L	20			ns
			-25L	25			
$I_{CC\ (PD)}$	Power down supply current	V_{CC} = 3.0V				50	μA
		V_{CC} = 5.5V				100	

Note 10 : This is only M5M51288BKP, KJ, VP-20L, -25L

TIMING WAVEFORM FOR POWER DOWN



HIGH SPEED SRAM

(Low voltage Version)

5

M5M5V278DP,J,VP-15,-20

262144-BIT (32768-WORD BY 8-BIT) CMOS STATIC RAM

DESCRIPTION

The M5M5V278D is a family of 32768-word by 8-bit static RAMs, fabricated with the high-performance CMOS silicon-gate MOS process and designed for high-speed application.These devices operate on a single 3.3V supply, and are directly TTL compatible. They include a power-down feature as well.

FEATURES

- Fast access time M5M5V278DP,J,VP-15 ..... 15ns(max)
  M5M5V278DP,J,VP-20 ..... 20ns(max)
- Low power dissipation Active ..... 165mW(typ)
  Stand-by ..... 330μW(typ)
- Power down by $\overline{S}$
- Single 3.3V power supply
- Fully static operation
- Requires neither external clock nor refreshing
- All inputs and outputs are directly TTL compatible
- Easy memory expansion by chip-select ($\overline{S}$) input
- Output enable($\overline{OE}$) prevents data contention in the I/O bus
- All address inputs are changeable with each other

APPLICATION

High-speed memory systems

FUNCTION

A write operation is executed during the $\overline{S}$ low, and $\overline{W}$ low overlap time. In this period, address signals must be stable. When $\overline{W}$ is low, the DQ terminals is maintained in the high impedance state.

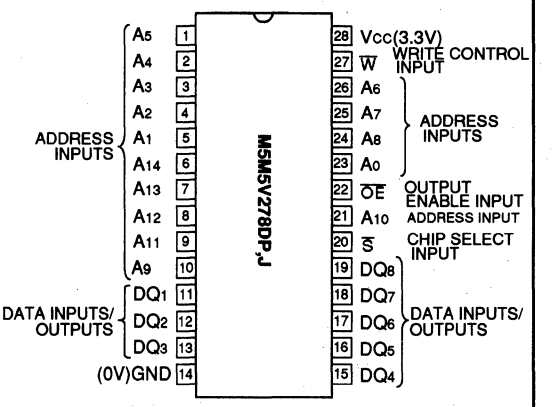
In a read operation, after setting $\overline{W}$ to high, $\overline{S}$ to low, and $\overline{OE}$ to low, if the address signals are stable, the data is available at the DQ terminals.

When $\overline{S}$ is high, the chip is in the non-selectable state, disabling both reading and writing. In this case the output is in the floating (high-impedance) state, useful for OR- ties with other devices.

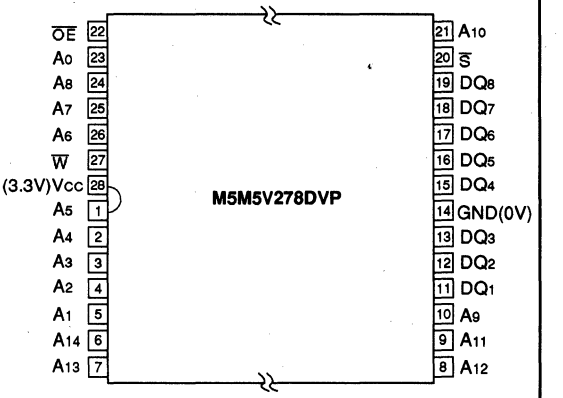
Setting $\overline{OE}$ at a high level,the output stage is in a high-impedance state, and the data bus contention problem in the write cycle is eliminated.

Signal $\overline{S}$ controls the power-down feature. When $\overline{S}$ goes high, power dissipation is reduced extremely. The access time from $\overline{S}$ is equivalent to the address access time.

PIN CONFIGURATION (TOP VIEW)



Outline 28P4Y(P)
28P0J(J)



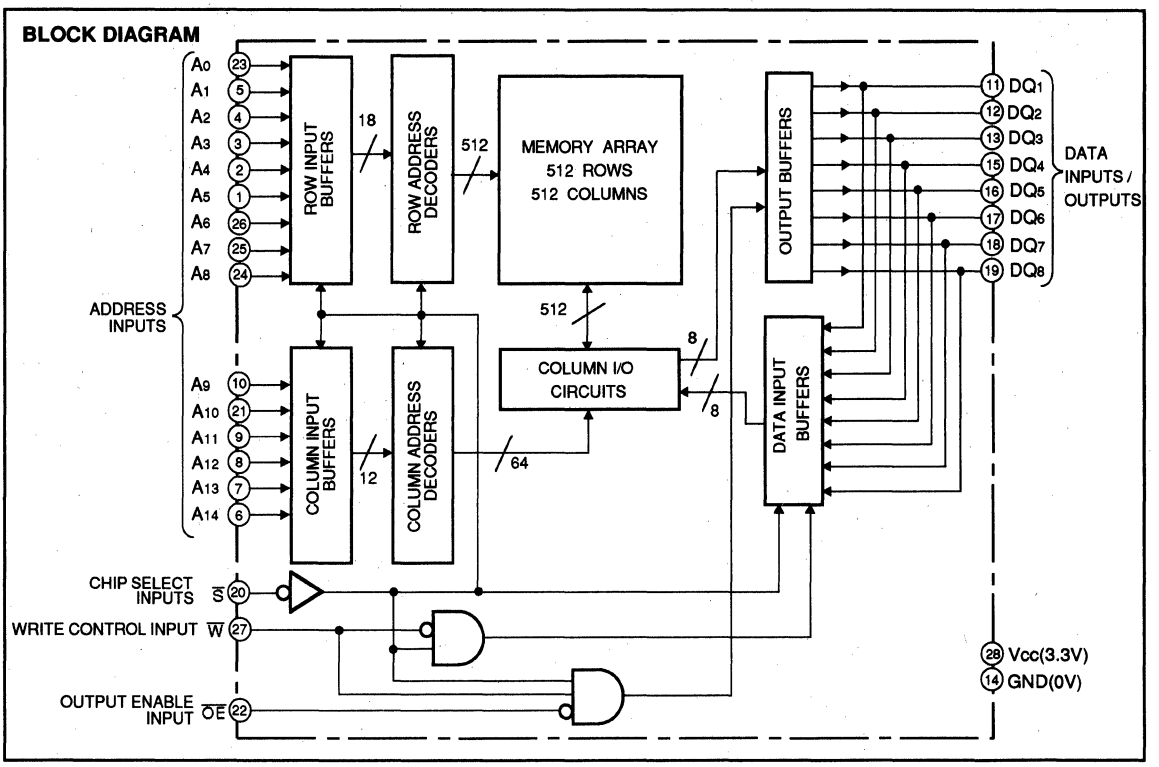
Outline 28P2C-A

MODE SELECTION

$\overline{S}$	$\overline{W}$	$\overline{OE}$	Mode	Data input /output	Icc
H	X	X	Non selection	High-impedance	Stand-by
L	L	X	Write	Din	Active
L	H	L	Read	Dout	Active
L	H	H		High-impedance	Active

H:VIH L:VIL X:VIH or VIL

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to GND	−2.0*～4.6	V
V_I	Input voltage		−2.0*～Vcc+0.5 (Max 4.6)	V
V_O	Output voltage		−2.0*～Vcc	V
P_d	Maximum power dissipation		1	W
T_{opr}	Operating temperature		0 ～ 70	℃
$T_{stg(bias)}$	Storage temperature (bias)		−10 ～ 85	℃
T_{stg}	Storage temperature		− 65 ～ 150	℃

* Pulse width ≦ 10ns, In case of DC: − 0.5V

DC ELECTRICAL CHARACTERISTICS (Ta = 0～70℃, Vcc=3.3V $^{+10\%}_{-5\%}$, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits Min	Limits Typ	Limits Max	Unit
V_{IH}	High - level input voltage			2.0		Vcc+0.3	V
V_{IL}	Low - level input voltage			−0.3*		0.8	V
V_{OH}	High - level output voltage	I_{OH} = − 4mA		2.4			V
V_{OL}	Low - level output voltage	I_{OL} = 8mA				0.4	V
I_I	Input current	V_I = 0～Vcc				2	μA
$\|I_{OZ}\|$	Off-state output current	$V_{I(\overline{S})}$ = V_{IH}, V_O= 0～Vcc				10	μA
I_{CC1}	Supply current from Vcc	$V_{I(\overline{S})}$ = V_{IL} Output open	AC(15ns cycle)			100	mA
			AC(20ns cycle)			90	
			DC		50	55	
I_{CC2}	Stand-by current	$V_{I(\overline{S})}$ = V_{IH}	AC(15ns cycle)			40	mA
			AC(20ns cycle)			35	
			Other V_I ≧V_{IH} or ≦ V_{IL}			20	
I_{CC3}	Stand-by current	$V_{I(\overline{S})}$ = Vcc − 0.2V Other V_I≦ 0.2V or V_I ≧Vcc − 0.2V			0.1	1	mA

Note 1. Current flow into an IC is positive, out is negative.
* − 3.0V in case of AC (Pulse width≦10ns)

CAPACITANCE

Symbol	Parameter	Test conditions	Limits Min	Limits Typ	Limits Max	Unit
C_I	Input capacitance	V_I = GND, V_I =25mVrms, f=1MHz			5*	pF
C_O	Output capacitance	V_O = GND, V_O=25mVrms, f=1MHz			7*	pF

* C_I, C_O are periodically sampled and are not 100% tested.

AC ELECTRICAL CHARACTERISTICS (Ta = 0～70℃, Vcc=3.3V $^{+10\%}_{-5\%}$, unless otherwise noted)

(1) MEASUREMENT CONDITIONS

Input pulse levels ····· V_{IH} = 3V, V_{IL} = 0V
Input rise and fall time ····· 3ns
Input timing reference levels ····· V_{IH} = 1.5V, V_{IL} = 1.5V
Output timing reference levels ····· V_{OH} = 1.5V, V_{OL} =1.5V
Output loads ····· Fig1, Fig2

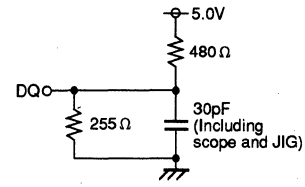


Fig.1 Output load

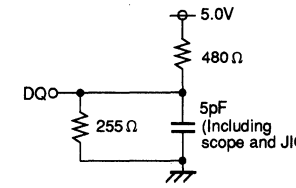


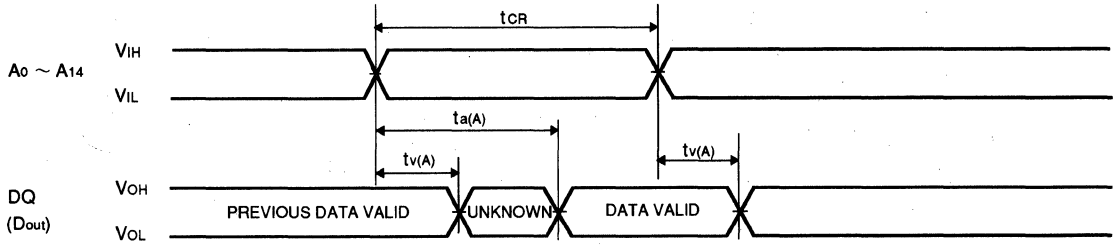
Fig.2 Output load for t_{en}, t_{dis}

(2) READ CYCLE

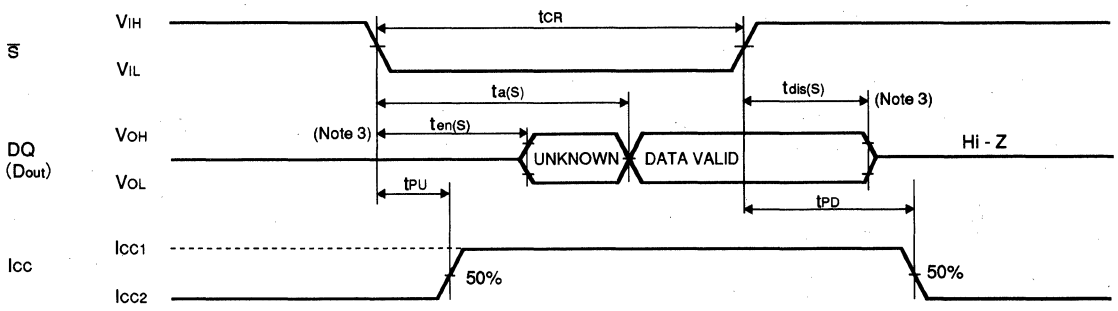
Symbol	Parameter	Limits				Unit
		M5M5V278D-15		M5M5V278D-20		
		Min	Max	Min	Max	
t_{CR}	Read cycle time	15		20		ns
$t_{a(A)}$	Address access time		15		20	ns
$t_{a(S)}$	Chip select access time		15		20	ns
$t_{a(OE)}$	Output enable access time		8		10	ns
$t_{v(A)}$	Data valid time after address change	3		3		ns
$t_{en(S)}$	Output enable time after $\overline{S}$ low	3		3		ns
$t_{dis(S)}$	Output disable time after $\overline{S}$ high	0	7	0	8	ns
$t_{en(OE)}$	Output enable time after $\overline{OE}$ low	0		0		ns
$t_{dis(OE)}$	Output disable time after $\overline{OE}$ high	0	7	0	8	ns
t_{PU}	Power-up time after chip selection	0		0		ns
t_{PD}	Power-down time after chip deselection		15		20	ns

(3) TIMING DIAGRAMS FOR READ CYCLE

Read cycle 1 <$\overline{W}$=H, $\overline{S}$=L>

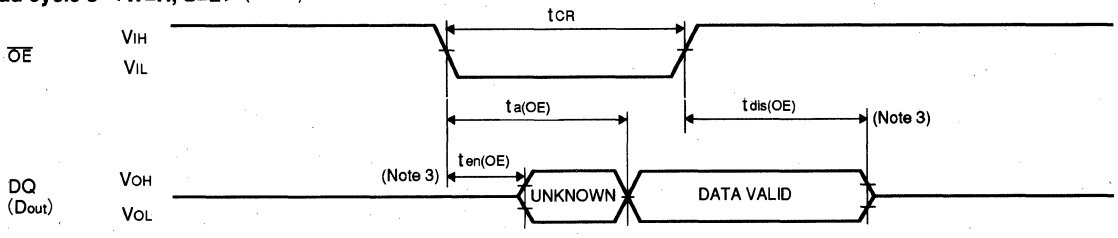


Read cycle 2 <$\overline{W}$=H> (Note 2)



Note 2. Address valid prior to or coincident with $\overline{S}$ transition low.
3. Transition is measured ±500mV from steady state voltage with specified loading in Figure2.

Read cycle 3 <$\overline{W}$=H, $\overline{S}$=L> (Note 4)



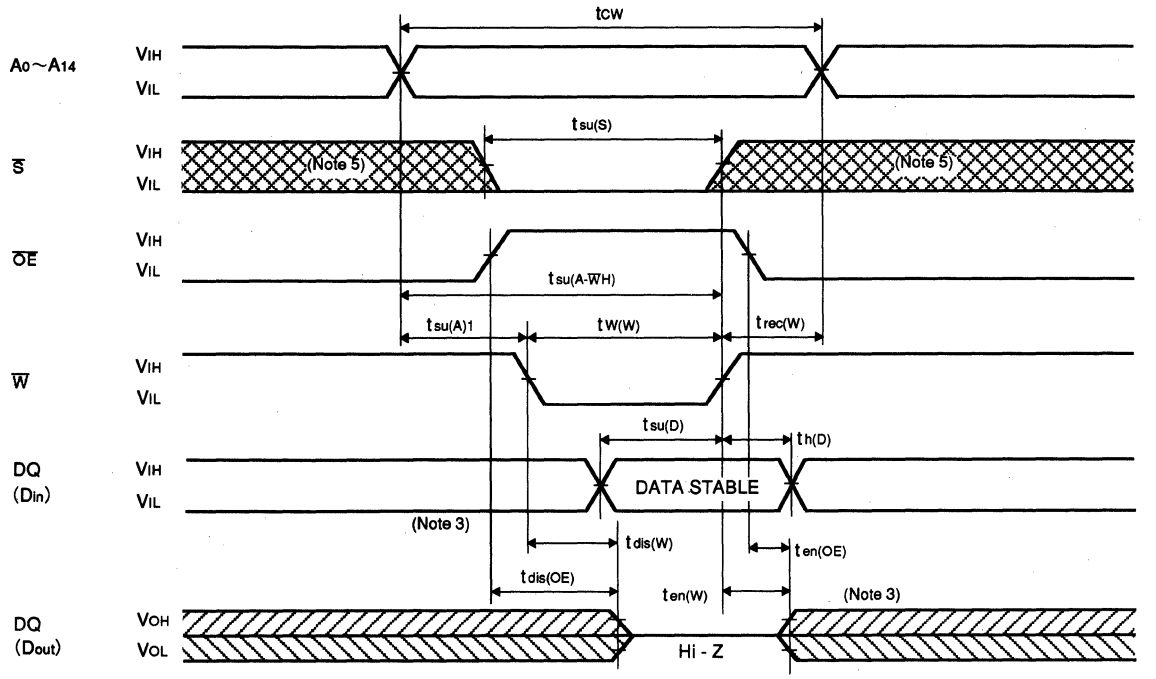
Note 4. Address and $\overline{S}$ valid prior to $\overline{OE}$ transition low by ($t_{a(A)}$ - $t_{a(OE)}$), ($t_{a(S)}$-$t_{a(OE)}$).

(4) WRITE CYCLE

Symbol	Parameter	Limits				Unit
		M5M5V278D-15		M5M5V278D-20		
		Min	Max	Min	Max	
t_{CW}	Write cycle time	15		20		ns
$t_{su(S)}$	Chip select setup time	12		15		ns
$t_{su(A)1}$	Address setup time 1 ($\overline{W}$ CONTROL)	0		0		ns
$t_{su(A)2}$	Address setup time 2 ($\overline{S}$ CONTROL)	0		0		ns
$t_{w(W)}$	Write pulse width	12		15		ns
$t_{rec(W)}$	Write recovery time	0		0		ns
$t_{su(D)}$	Data setup time	7		8		ns
$t_{h(D)}$	Data hold time	0		0		ns
$t_{dis(W)}$	Output disable time after $\overline{W}$ low	0	7	0	8	ns
$t_{en(W)}$	Output enable time after $\overline{W}$ high	0		0		ns
$t_{su(A-\overline{W}H)}$	Address to $\overline{W}$ high	12		15		ns
$t_{en(OE)}$	Output enable time after $\overline{OE}$ low	0		0		ns
$t_{dis(OE)}$	Output disable time after $\overline{OE}$ high	0	7	0	8	ns

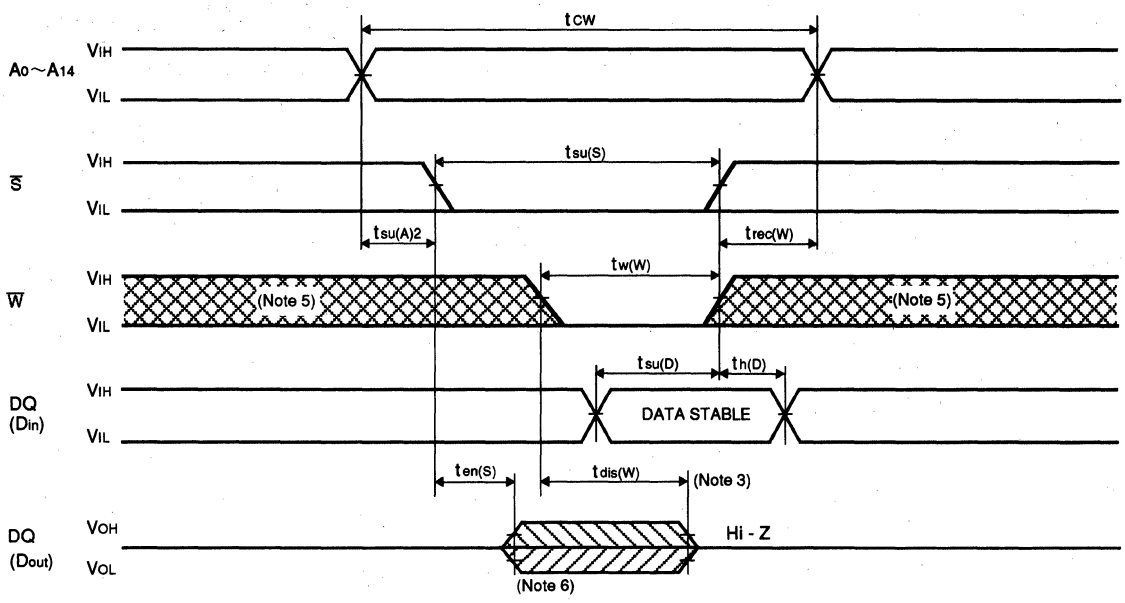
(5) TIMING DIAGRAMS FOR WRITE CYCLE

Write cycle 1 ($\overline{W}$ control mode)



Note 5. Hatching indicates the state is don't care.

Write cycle 2 ($\overline{S}$ control mode)



Note 6. When the falling edge of $\overline{W}$ is simultaneous or prior to the falling edge of $\overline{S}$, the output is maintained in the high impedance.
7. ten,tdis are periodically sampled and are not 100% tested.

M5M5V278EJ,VP-10,-12,-15

262144-BIT (32768-WORD BY 8-BIT) CMOS STATIC RAM

DESCRIPTION

The M5M5V278E is a family of 32768-word by 8-bit static RAMs, fabricated with the high-performance CMOS silicon-gate MOS process and designed for high-speed application. These devices operate on a single 3.3V supply, and are directly TTL compatible. They include a power-down feature as well.

FEATURES

- Fast acces stime M5M5V278EJ,VP-10 ..... 10ns(max)
  M5M5V278EJ,VP-12 ..... 12ns(max)
  M5M5V278EJ,VP-15 ..... 15ns(max)
- Low power dissipation Active ..... 264mW(typ)
  Stand by (-10,-12,-15) ..... 0.33mW(typ)
- Power down by $\overline{S}$
- Single 3.3V power supply
- Fully static operation
- Requires neither external clock nor refreshing
- All inputs and outputs are directly TTL compatible
- Easy memory expansion by chip-select ($\overline{S}$) input
- Output enable($\overline{OE}$) prevents data contention in the I/O bus
- All address inputs are changeable with each other

APPLICATION

High-speed memory systems

FUNCTION

A write operation is executed during the $\overline{S}$ low, and $\overline{W}$ low overlap time. In this period, address signals must be stable. When $\overline{W}$ is low, the DQ terminals is maintained in the high impedance state.

In a read operation, after setting $\overline{W}$ to high, $\overline{S}$ to low, and $\overline{OE}$ to low, if the address signals are stable, the data is available at the DQ terminals.

When $\overline{S}$ is high, the chip is in the non-selectable state, disabling both reading and writing. In this case the output is in the floating (high-impedance) state,useful for OR-ties with other devices.

Setting $\overline{OE}$ at a high level, the output stage is in a high-impedance state, and the data bus contention problem in the write cycle is eliminated.

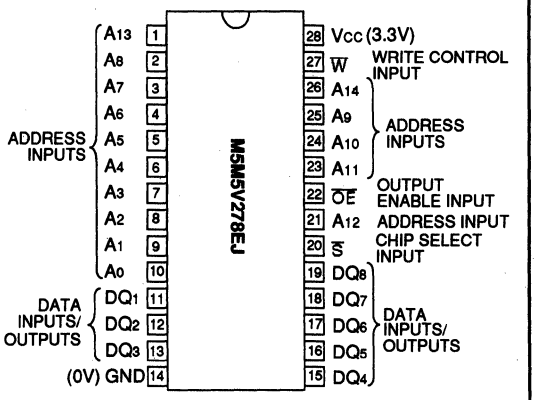
Signal $\overline{S}$ controls the power-down feature. When $\overline{S}$ goes high, power dissipation is reduced extremely. The access time from $\overline{S}$ is equivalent to the address access time.

MODE SELECTION

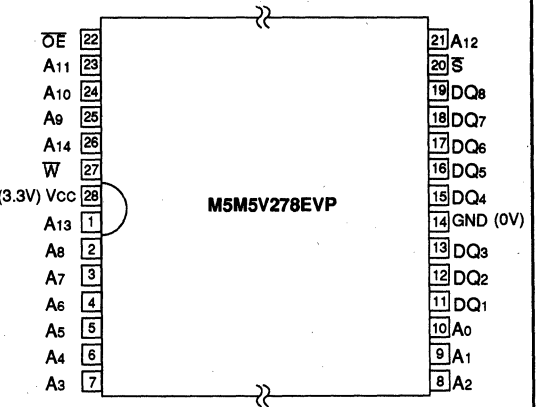
$\overline{S}$	$\overline{W}$	$\overline{OE}$	Mode	Data input /output	Icc
H	X	X	Non selection	High-impedance	Stand-by
L	L	X	Write	Din	Active
L	H	L	Read	Dout	Active
L	H	H		High-impedance	Active

H : VIH L : VIL X : VIH or VIL

PIN CONFIGURATION (TOP VIEW)

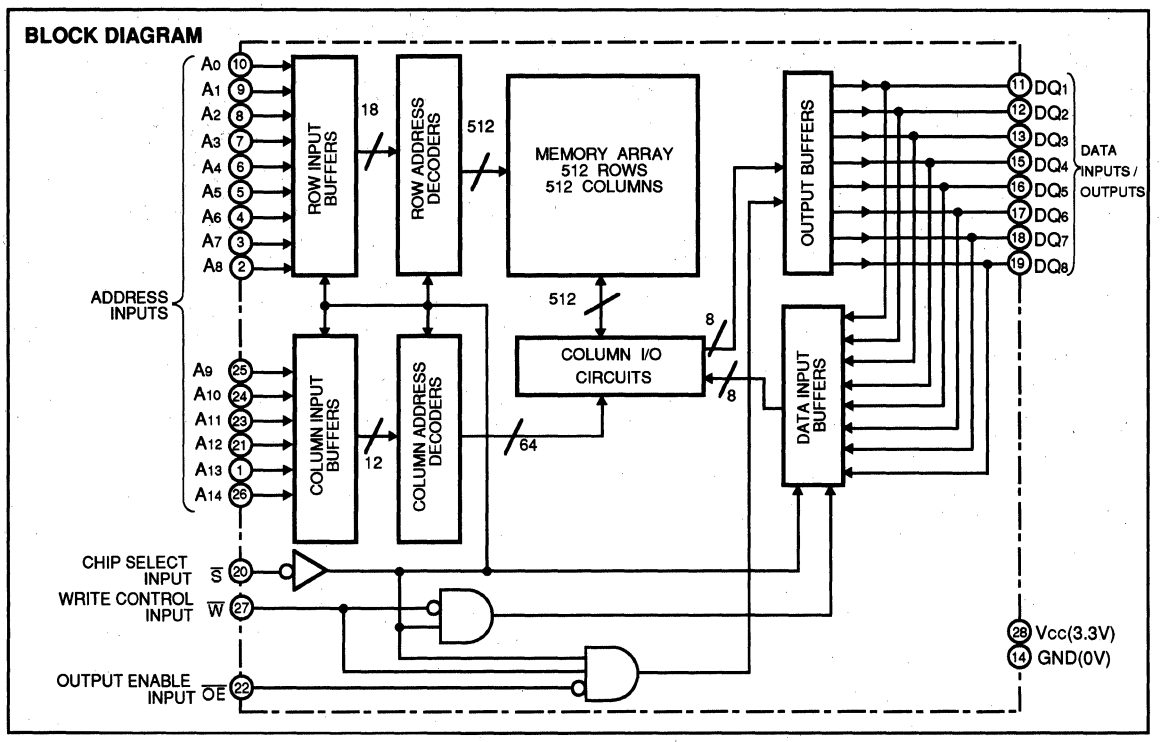


Outline 28P0J



Outline 28P2C-A

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to GND	−2.0*～4.6	V
V_I	Input voltage		−2.0*～Vcc+0.5 (Max 4.6)	V
V_O	Output voltage		−2.0*～Vcc	V
P_d	Maximum power dissipation		1	W
T_{opr}	Operating temperature		0～70	℃
$T_{stg(bias)}$	Storage temperature (bias)		−10～85	℃
T_{stg}	Storage temperature		−65～150	℃

*Pulse width ≦ 10ns,In case of DC: − 0.5V

DC ELECTRICAL CHARACTERISTICS (Ta=0～70℃, Vcc=3.3V $^{+10\%}_{-5\%}$ unless otherwise noted)

Symbol	Parameter	Test conditions		Limits Min	Limits Typ	Limits Max	Unit
V_{IH}	High-level input voltage			2.0		Vcc+0.3	V
V_{IL}	Low-level input voltage			−0.3*		0.8	V
V_{OH}	High-level output voltage	I_{OH} = −4mA		2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 8mA				0.4	V
I_I	Input current	V_I = 0～Vcc				2	μA
$\|I_{OZ}\|$	Off-state output current	$V_{I(\overline{S})} = V_{IH}$, V_O= 0～Vcc				10	μA
I_{CC1}	Supply current from Vcc	$V_{I(\overline{S})} = V_{IL}$ Output open	AC(10ns cycle)			140	mA
			AC(12ns cycle)			120	
			AC(15ns cycle)			100	
			DC		80	85	
I_{CC2}	Stand-by current	$V_{I(\overline{S})} = V_{IH}$	AC(10ns cycle)			60	mA
			AC(12ns cycle)			55	
			AC(15ns cycle)			50	
			Other $V_I \geqq V_{IH}$ or $\leqq V_{IL}$			30	
I_{CC3}	Stand-by current	$V_{I(\overline{S})}$ = Vcc−0.2V, or $V_I \geqq$ Vcc−0.2V Other $V_I \leqq$ 0.2V			0.1	10	mA

Note 1. Current flow into an IC is positive, out is negative.
* −3.0 V in case of AC (Pulse width≦10ns)

CAPACITANCE

Symbol	Parameter	Test conditions	Limits Min	Limits Typ	Limits Max	Unit
C_I	Input capacitance	V_I=GND, V_I=25mVrms, f=1MHz			5*	pF
C_O	Output capacitance	V_O=GND, V_O=25mVrms, f=1MHz			7*	pF

* C_I, C_O are predically sampled and are not 100% tested.

AC ELECTRICAL CHARACTERISTICS (Ta = 0～70℃, Vcc=3.3V $^{+10\%}_{-5\%}$, unless otherwise noted)

(1) MEASUREMENT CONDITIONS

Input pulse levels ..... V_{IH} = 3.0V, V_{IL} = 0.0V
Input rise and fall time 3ns
Input timing reference levels ..... V_{IH} = 1.5V, V_{IL} = 1.5V
Output timing reference levels ..... V_{OH} = 1.5V, V_{OL} = 1.5V
Output loads Fig1, Fig2

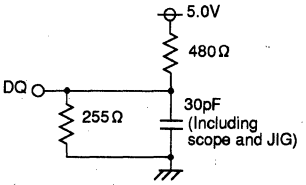


Fig.1 Output load

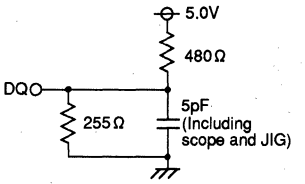


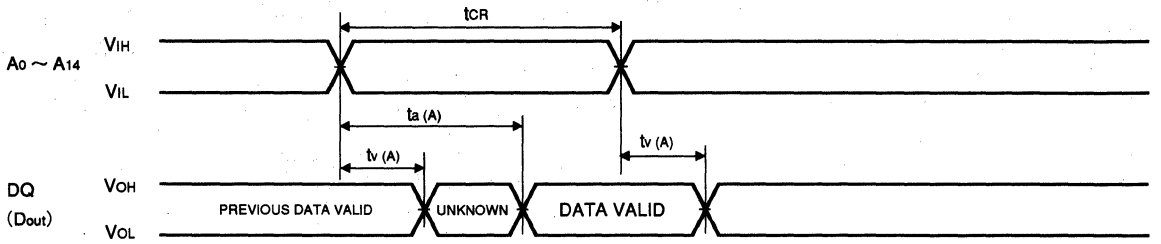
Fig.2 Output load for ten,tdis

(2) READ CYCLE

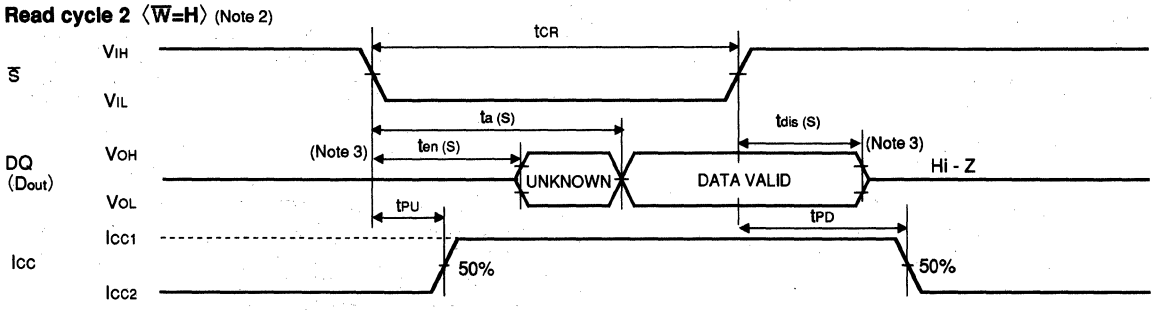
Symbol	Parameter	Limits						Unit
		M5M5V278E-10		M5M5V278E-12		M5M5V278E-15		
		Min	Max	Min	Max	Min	Max	
t_{CR}	Read cycle time	10		12		15		ns
$t_{a(A)}$	Address access time		10		12		15	ns
$t_{a(S)}$	Chip select access time		10		12		15	ns
$t_{a(OE)}$	Output enable access time		5		6		8	ns
$t_{v(A)}$	Data valid time after address change	3		3		3		ns
$t_{en(S)}$	Output enable time after chip selection	3		3		3		ns
$t_{dis(S)}$	Output disable time after chip deselection	0	5	0	6	0	7	ns
$t_{en(OE)}$	Output enable time after $\overline{OE}$ low	0		0		0		ns
$t_{dis(OE)}$	Output disable time after $\overline{OE}$ high	0	5	0	6	0	7	ns
t_{PU}	Power-up time after chip selection	0		0		0		ns
t_{PD}	Power-down time after chip deselection		10		12		15	ns

(3) TIMING DIAGRAMS FOR READ CYCLE

Read cycle 1 ⟨$\overline{W}$=H, $\overline{S}$=L⟩

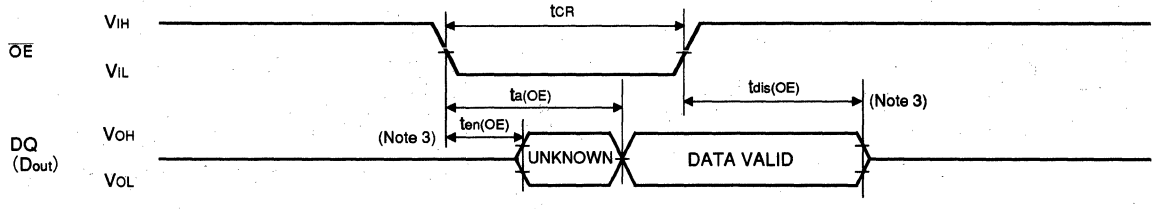


Read cycle 2 ⟨$\overline{W}$=H⟩ (Note 2)



Note2. Address valid prior to or coincident with $\overline{S}$ transition low.
3.Transition is measured ±500mV from steady state voltage with specified loading in Figure2.

Read cycle 3 ⟨$\overline{W}$=H, $\overline{S}$=L⟩ (Note 4)



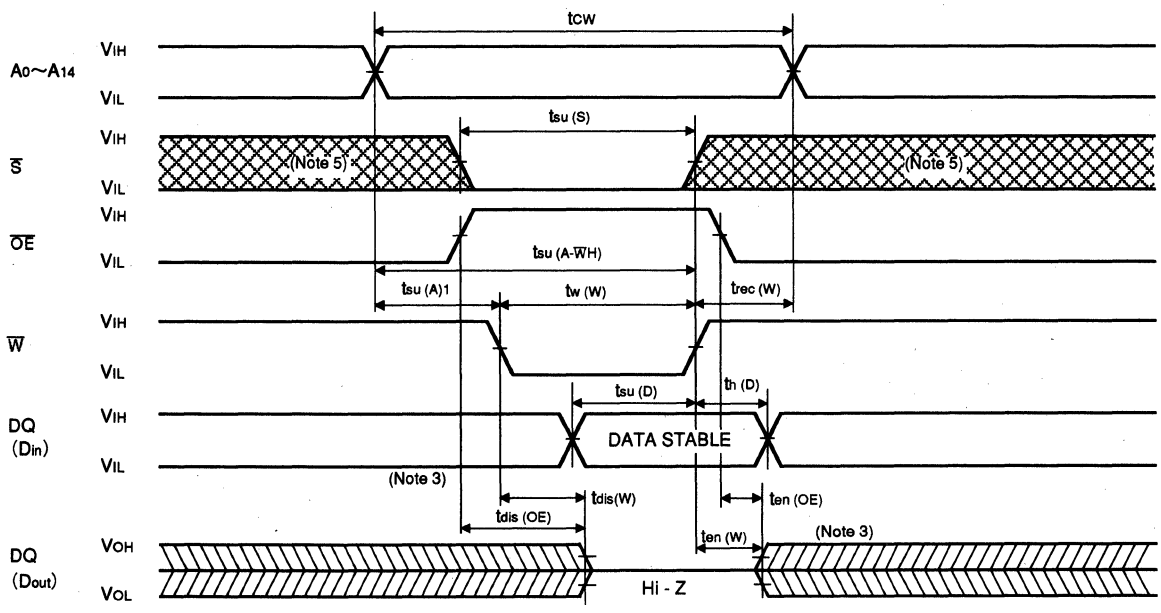
Note4. Address and $\overline{S}$ valid prior to $\overline{OE}$ transition low by ($t_{a(A)}$ - $t_{a(OE)}$), ($t_{a(S)}$-$t_{a(OE)}$).

(4) WRITE CYCLE

Symbol	Parameter	Limits						Unit
		M5M5V278E-10		M5M5V278E-12		M5M5V278E-15		
		Min	Max	Min	Max	Min	Max	
tcw	Write cycle time	10		12		15		ns
tsu(S)	Chip select setup time	8		10		12		ns
tsu(A)1	Address setup time 1 ($\overline{W}$ CONTROL)	0		0		0		ns
tsu(A)2	Address setup time 2 ($\overline{S}$ CONTROL)	0		0		0		ns
tw(W)	Write pulse width	8		10		12		ns
trec(W)	Write recovery time	0		0		0		ns
tsu(D)	Data setup time	5		6		7		ns
th(D)	Data hold time	0		0		0		ns
tdis(W)	Output disable time after $\overline{W}$ low	0	5	0	6	0	7	ns
ten(W)	Output enable time after $\overline{W}$ high	0		0		0		ns
tsu(A-WH)	Address to $\overline{W}$ high	8		10		12		ns
ten(OE)	Output enable time after $\overline{OE}$ low	0		0		0		ns
tdis(OE)	Output disable time after $\overline{OE}$ high	0	5	0	6	0	7	ns

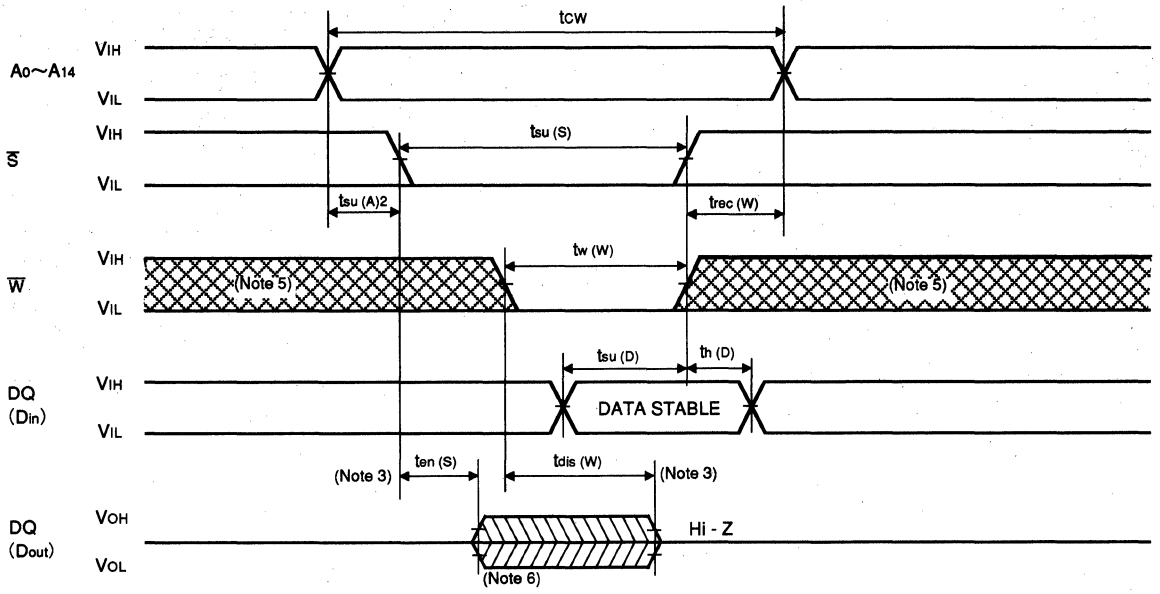
(5) TIMING DIAGRAMS FOR WRITE CYCLE

Write cycle 1 ($\overline{W}$ control mode)



Note5. Hatching indicates the state is don't care.

Write cycle 2 ($\overline{S}$ control mode)



Note6. When the falling edge of $\overline{W}$ is simultaneous or prior to the falling edge of $\overline{S}$, the output is maintained in the high impedance.

7. ten,tdis are periodically sampled and are not 100% tested.

DESCRIPTION

The M5M5V1132FP is a family of 1M bit synchronous SRAMs organized as 32768-words of 32-bit. The M5M5V1132FP provides a high speed secondary cache solution for microprocessors. The design integrates a 2-bit burst counter, input and output registers with the ultra fast 1M bit SRAM on a single monolithic circuit. This design reduces component count of cache data RAM solutions. Mitsubishi's SRAMs are fabricated with high-performance, low power CMOS technology, providing greater reliability. This device operates on a single 3.3V power supply and are directly LVTTL compatible.

FEATURES

- Access times /Cycle times
  - M5M5V1132FP-6 ..... 5.5ns/10.0ns (100MHz)
  - M5M5V1132FP-7, -7L 7.0ns/13.3ns (75MHz)
  - M5M5V1132FP-8, -8L 8.0ns/15.0ns (66MHz)
  - M5M5V1132FP-10, -10L 10.0ns/16.7ns (60MHz)
- Low power dissipation
  - Active (66MHz) ..... 415mW (typ)
  - Stand-by (-6, -7, -8, -10) ..... 0.7mW (typ)
  - Stand-by (-7L, -8L, -10L) ..... 20μW (typ)
- Package
  - 100pin QFP, Body Size (14.0×20.0 mm^2)
  - Pin Pitch (0.65 mm)
- Single 3.3V power supply (3.13 ~ 3.60V)
- Fully registered inputs and outputs (Pipeline operation)
- Global write control or individual byte write control
- MODE pin allows either liner or interleaved burst
- Snooze mode pin (ZZ) for power down
- CLK stopped stand by mode.
- 32-bit wide data I/O

APPLICATION

486/Pentium™/PowerPC™ processor second level caches

FUNCTION

Synchronous circuitry allows for precise cycle control triggered by a positive edge clock transition. Synchronous signals include : all addresses, all data inputs, all chip selects ($\overline{S}_1$, $\overline{S}_2$, S_2), burst control inputs ($\overline{ADSC}$, $\overline{ADSP}$, $\overline{ADV}$) and write enables ($\overline{MBW}$, $\overline{GW}$, $\overline{BW}_1$, $\overline{BW}_2$, $\overline{BW}_3$, $\overline{BW}_4$). $\overline{S}_2$ and S_2 provide easy depth expansion.

The write operation can be performed by two methods. The global write enable ($\overline{GW}$) will perform a write to all 32 bits. Byte wide writes are controlled by the master byte write enable ($\overline{MWB}$) and the 4 individual byte write enables ($\overline{BW}_1$~$\overline{BW}_4$). The byte write cycle will write from one to four bytes. The write cycle is internally self-timed, eliminating the complex signal generation of an off chip write.

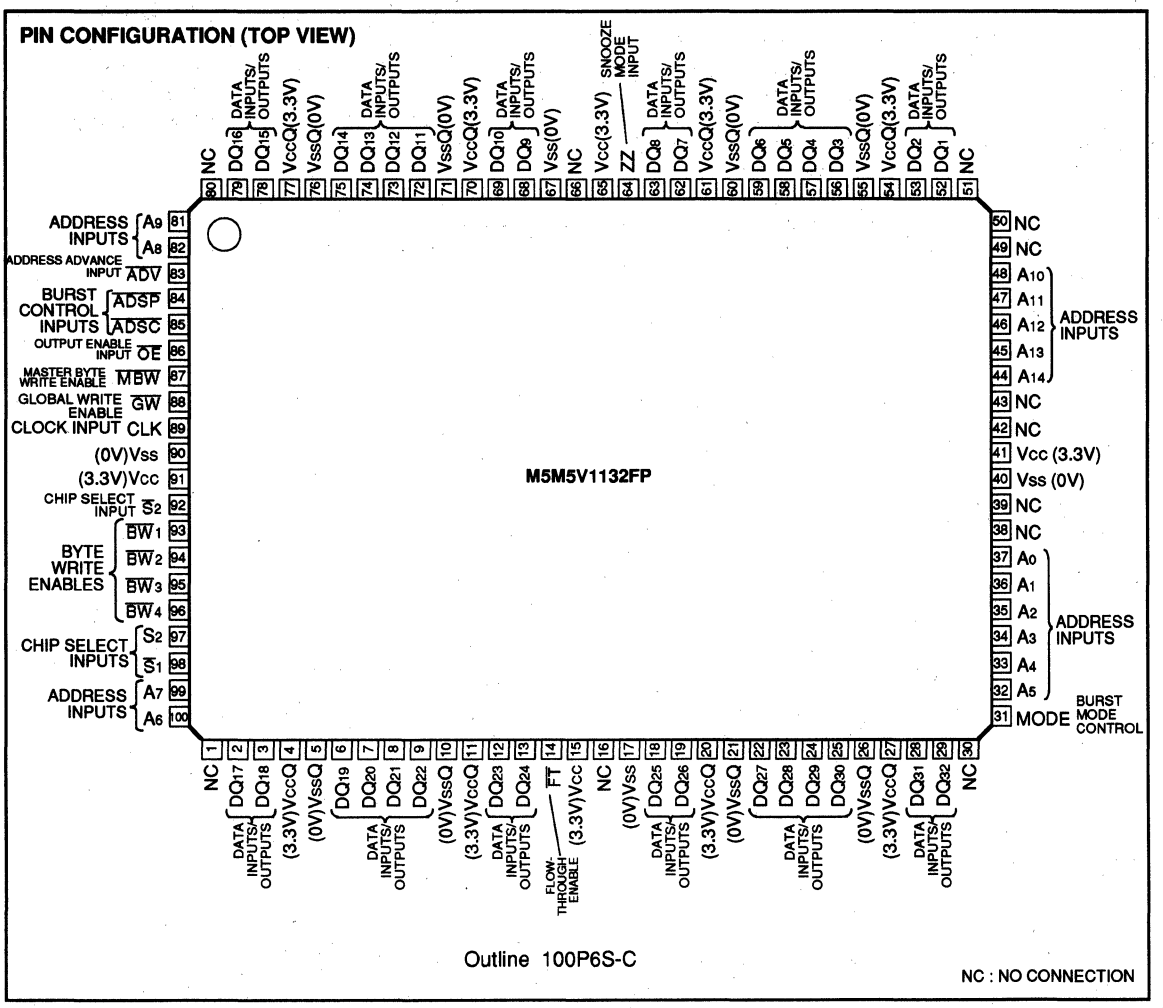
Asynchronous signals are output enable ($\overline{OE}$), snooze mode pin (ZZ) and clock (CLK). The HIGH input of ZZ pin puts the SRAM in the power-down state. When ZZ is pulled to LOW, the SRAM normally operates after 30ns of the wake up period.

When CLK is stopped and all inputs (Address, Burst control, CLK etc.) are fixed in CMOS level, the SRAM becomes in the power-down state that is called "CLK stopped stand-by mode". During CLK stopped stand-by mode, power supply current is almost same as snooze mode even if the SRAM is selected. When CLK is active again, the SRAM immediately recovers from CLK stopped stand-by mode to normal operation mode.

The burst mode control (MODE), and the flow-through enable ($\overline{FT}$) are DC operated pins. MODE pin will allow the choice of either an interleaved burst, or a linear burst. $\overline{FT}$ pin normally is pulled HIGH. When $\overline{FT}$ is pulled LOW, the SRAM changes non-pipelined type with flow-through output. $\overline{FT}$ LOW input is only used for a test mode.

The burst operation is initiated by either address status processor ($\overline{ADSP}$) or address status controller ($\overline{ADSC}$). The burst advance pin ($\overline{ADV}$) controls subsequent burst addresses.

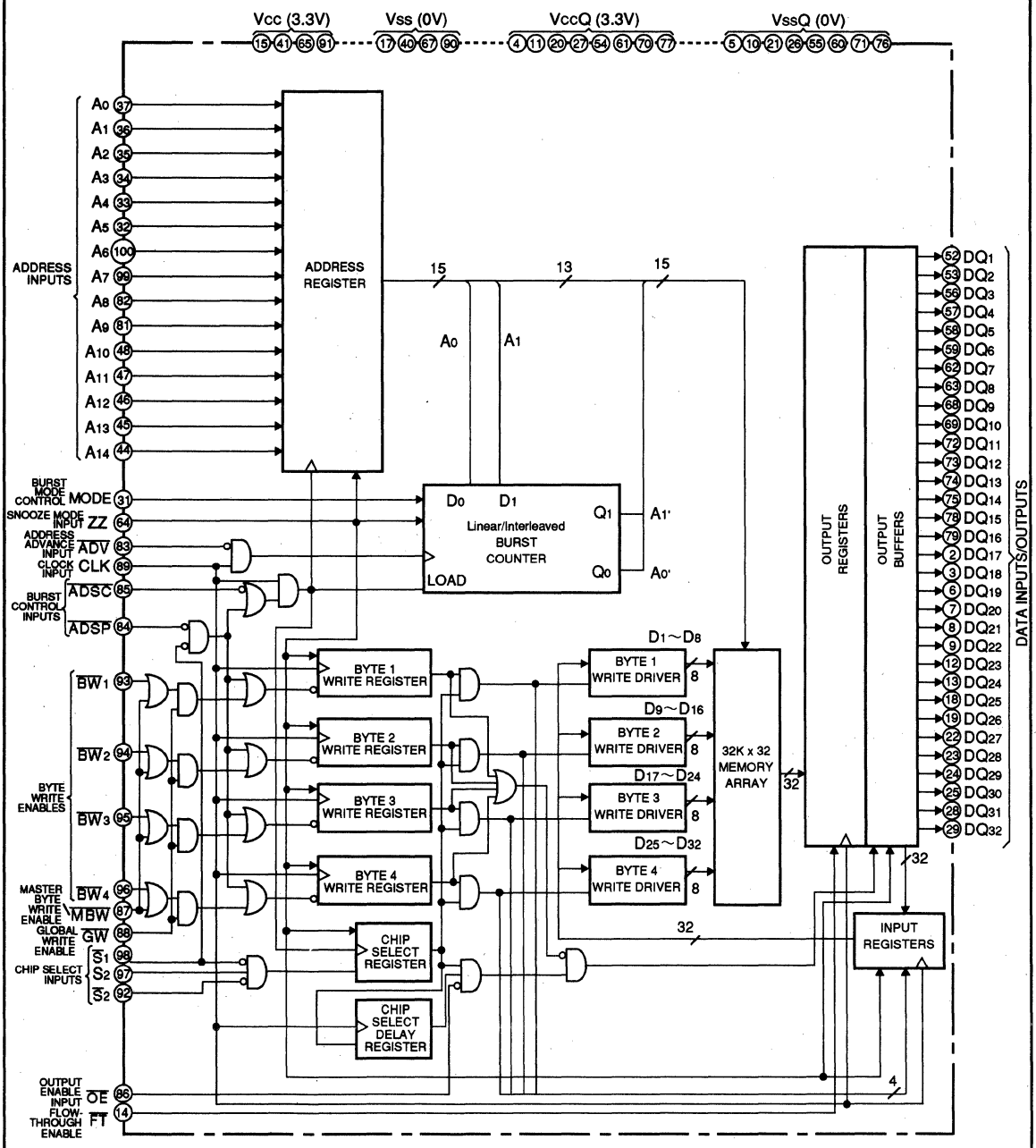
PIN CONFIGURATION (TOP VIEW)



Outline 100P6S-C

NC : NO CONNECTION

BLOCK DIAGRAM



Note: The Block Diagram illustrates simplified device operation. See Truth Table, pin descriptions and timing diagrams for detailed information.

PIN FUNCTIONS

Pin	Name	Function
A_0~A_{14}	Synchronous Address Inputs	These inputs are registered and must meet the setup and hold times around the rising edge of CLK.
$\overline{MBW}$	Synchronous Master Byte Write Enables	This active LOW input is used to enable the individual byte write operation. The individual byte write operation is performed when $\overline{MBW}$ is LOW and $\overline{GW}$ is HIGH. The global write operation (a write to all 32 bits) is performed when $\overline{GW}$ is LOW.
$\overline{GW}$	Synchronous Global Write Enables	This active LOW input is used to enable the global write operation (a write to all 32 bits) and must meet the setup and hold times around the rising edge of CLK.
$\overline{BW}_1$, $\overline{BW}_2$, $\overline{BW}_3$, $\overline{BW}_4$	Synchronous Byte Write Enables	These active LOW inputs allow individual bytes to be written and must meet the setup and hold times around the rising edge of CLK. A byte write enables is LOW for a WRITE cycle and HIGH for a READ cycle. $\overline{BW}_1$ controls DQ_1~DQ_8. $\overline{BW}_2$ controls DQ_9 ~DQ_{16}. $\overline{BW}_3$ controls DQ_{17}~DQ_{24}. $\overline{BW}_4$ controls DQ_{25}~DQ_{32}. Data I/O are tristated if any of these four inputs are LOW.
CLK	Clock Input	This signal latches the address, data, chip enables, byte write enables and burst control inputs on its rising edge. All synchronous inputs must meet setup and hold times around the clock's rising edge.
$\overline{S}_1$	Synchronous Chip Select Input	This active LOW input is used to enable the device and conditions internal use of $\overline{ADSP}$. This input is sampled only when a new external address is loaded.
$\overline{S}_2$	Synchronous Chip Select Input	This active LOW input is used to enable the device. This input is sampled only when a new external address is loaded. This input can be used for memory depth expansion.
S_2	Synchronous Chip Select Input	This active HIGH input is used to enable the device. This input is sampled only when a new external address is loaded. This input can be used for memory depth expansion.
$\overline{OE}$	Output Enable Input	This active LOW asynchronous input enables the data I/O output drivers.
DQ_1~DQ_{32}	Data I/O	Byte 1 is DQ_1~DQ_8; Byte 2 is DQ_9~DQ_{16}; Byte 3 is DQ_{17}~DQ_{24}; Byte 4 is DQ_{25}~DQ_{32}. Input data must meet setup and hold times around the rising edge of CLK.
ZZ	Snooze Mode Input	This asynchronous input allows the selection either normal operation mode or snooze mode that the SRAM is in the powerdown state even if CLK is operated. This active HIGH asynchronous input puts the SRAM in the snooze mode. When ZZ=HIGH, input leak current flows to this pin. When this pin is pulled to LOW or NC, the SRAM normally operates.
MODE	Burst Mode Control	This DC operated pin allows the choice of either a interleaved burst or a linear burst. If this pin is HIGH or NC, an interleaved burst occurs. When this pin is tied LOW, a linear burst occurs, and input leak current flows .
$\overline{FT}$	Flow-through Enable	This DC operated pin is used as a test mode pin. Normally, this pin is pulled HIGH or NC. When this pin is tied LOW, the SRAM changes non-pipelined type with flow-through output, and input leak current flows.
$\overline{ADSP}$	Synchronous Address Status Processor	This active LOW input interrupts any ongoing burst, causing a new external address to be latched. A READ is performed using the new address, independent of the byte write enables and $\overline{ADSC}$ but dependent upon S_2 and $\overline{S}_2$. $\overline{ADSP}$ is ignored if $\overline{S}_1$ is HIGH. Power-down state is entered if S_2 is LOW or $\overline{S}_2$ is HIGH.
$\overline{ADSC}$	Synchronous Address Status Controller	This active LOW input interrupts any ongoing burst and causes a new external address to be latched. A READ or WRITE is performed using the new address if all chip enables are active. Power-down state is entered if one or more chip enables are inactive.
$\overline{ADV}$	Synchronous Address Advance	This active LOW input is used to advance the internal burst counter, controlling burst access after the external address is loaded. A HIGH on this pin effectively causes wait states to be generated (no address advance). This pin must be HIGH at the rising edge of the first clock after an $\overline{ADSP}$ cycle is initiated if a WRITE cycle is desired (to ensure use of correct address)
V_{CC}	V_{CC}	Power Supply (3.3V)
V_{SS}	V_{SS}	Ground (0V)
V_{CCQ}	V_{CCQ}	I/O Buffer Supply (3.3V)
V_{SSQ}	V_{SSQ}	I/O Buffer Ground (0V)

DC OPERATED TRUTH TABLE

Name	Input status	Operation
MODE	H or NC	Interleaved Burst Sequence
	L	Linear Burst Sequence
$\overline{FT}$	H or NC	Pipelined SRAM
	L	Non-pipelined SRAM (Test mode)

Note 1. MODE and $\overline{FT}$ are DC operated pins.
2. H means logic HIGH or NC. L means logic LOW. NC meons No-Connection
3. Normally, $\overline{FT}$ is pulled to HIGH or NC. $\overline{FT}$ LOW input is only used for a test mode.
4. See BURST SEQUENCE TABLE about Interleaved and Linear Burst Sequence.

BURST SEQUENCE TABLE

Interleaved Burst Sequence (when MODE = HIGH or NC)

Operation	A_{14} -A_2	A_1	A_0
First access, latch external address	A_{14} -A_2	A_1	A_0
Second access (first burst address)	latched A_{14} -A_2	latched A_1	latched $\overline{A_0}$
Third access (second burst address)	latched A_{14} -A_2	latched $\overline{A_1}$	latched A_0
Fourth access (third burst address)	latched A_{14} -A_2	latched $\overline{A_1}$	latched $\overline{A_0}$

Linear Burst Sequence (when MODE = LOW)

Operation	A_{14} -A_2	A_1, A_0			
First access, latch external address	A_{14} -A_2	0, 0	0, 1	1, 0	1, 1
Second access (first burst address)	latched A_{14} -A_2	0, 1	1, 0	1, 1	0, 0
Third access (second burst address)	latched A_{14} -A_2	1, 0	1, 1	0, 0	0, 1
Fourth access (third burst address)	latched A_{14} -A_2	1, 1	0, 0	0, 1	1, 0

Note 5. The burst sequence wraps around to its initial state upon completion.

SYNCHRONOUS TRUTH TABLE

$\overline{S_1}$	$\overline{S_2}$	S_2	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{Write}$	CLK	Address used	Operation
H	X	X	X	L	X	X	L-H	None	Deselected Cycle, Power-down
L	X	L	L	X	X	X	L-H	None	Deselected Cycle, Power-down
L	H	X	L	X	X	X	L-H	None	Deselected Cycle, Power-down
L	X	L	X	L	X	X	L-H	None	Deselected Cycle, Power-down
L	H	X	X	L	X	X	L-H	None	Deselected Cycle, Power-down
L	L	H	L	X	X	X	L-H	External	READ Cycle, Begin Burst
L	L	H	H	L	X	L	L-H	External	WRITE Cycle, Begin Burst
L	L	H	H	L	X	H	L-H	External	READ Cycle, Begin Burst
X	X	X	H	H	L	H	L-H	Next	READ Cycle, Continue Burst
H	X	X	X	H	L	H	L-H	Next	READ Cycle, Continue Burst
X	X	X	H	H	L	L	L-H	Next	WRITE Cycle, Continue Burst
H	X	X	X	H	L	L	L-H	Next	WRITE Cycle, Continue Burst
X	X	X	H	H	H	H	L-H	Current	READ Cycle, Suspend Burst
H	X	X	X	H	H	H	L-H	Current	READ Cycle, Suspend Burst
X	X	X	H	H	H	L	L-H	Current	WRITE Cycle, Suspend Burst
H	X	X	X	H	H	L	L-H	Current	WRITE Cycle, Suspend Burst

Note 6. X means "don't care". H means logic HIGH. L means logic LOW.
7. $\overline{Write}$ =L means "WRITE" operation in WRITE TRUTH TABLE.
$\overline{Write}$ =H means "READ" operation in WRITE TRUTH TABLE.
8. All inputs in this table must meet setup and hold times around the rising edge (LOW to HIGH) of CLK.
9. $\overline{ADSP}$ LOW always initiates an internal READ at the L-H edge of CLK.
10. Operation finally depends on status of asynchronous input pins (ZZ and $\overline{OE}$).
See ASYNCHRONOUS TRUTH TABLE.

WRITE TRUTH TABLE

$\overline{GW}$	$\overline{MBW}$	$\overline{BW_1}$	$\overline{BW_2}$	$\overline{BW_3}$	$\overline{BW_4}$	Operation
H	H	X	X	X	X	READ
H	L	H	H	H	H	READ
H	L	L	H	H	H	WRITE BYTE 1
H	L	H	L	H	H	WRITE BYTE 2
H	L	H	H	L	H	WRITE BYTE 3
H	L	H	H	H	L	WRITE BYTE 4
H	L	L	L	H	H	WRITE BYTE1 and 2
H	L	H	H	L	L	WRITE BYTE3 and 4
H	L	L	L	L	L	WRITE ALL BYTE
L	X	X	X	X	X	WRITE ALL BYTE

Note 11. X means "don't care". H means logic HIGH. L means logic LOW.
12. All inputs in this table must meet setup and hold ties around the rising edge (LOW to HIGH) of CLK.

ASYNCHRONOUS TRUTH TABLE

ZZ	$\overline{OE}$	Operation of synchronous truth table	Operation	I/O Status
H	X	X	Snooze mode	High-Z
L or NC	L	READ	READ	Q
L or NC	H	READ	READ	High-Z
L or NC	X	WRITE	WRITE	High-Z - D
L or NC	X	Deselected	Deselected	High-Z

Note 13. For a write operation following a read operation, $\overline{OE}$ must be HIGH before the input data required setup time and held HIGH through the input data hold time.
14. In I/O STATUS, Q means output data during a read cycle, and D means input data during a write cycle.
15. "Snooze mode" means power down state of which stand-by current does not depend on cycle time.
16. "Deselected" means power down state of which stand-by current depends on cycle time.
17. When ZZ is pulled to LOW, the SRAM normally operates after 30ns of the wake up period.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Power supply voltage	With respect to GND	−2.0 * ~4.6	V
V_{CCQ}	I/O buffer supply voltage		−2.0 * ~Vcc+0.5 (max 4.6)	V
V_I	Input voltage		−2.0 * ~Vcc+0.5 (max 4.6)	V
V_O	Output voltage		−2.0 * ~4.6	V
P_d	Maximum power dissipation		1.2	W
T_{opr}	Operating temperature		0~70	℃
$T_{stg(bias)}$	Storage temperature (bias)		−10~85	℃
T_{stg}	Storage temperature		−65~150	℃

* This is −2.0V when pulse width ≦ 10ns, and −0.5V in case of DC.

DC ELECTRICAL CHARACTERISTICS (Ta = 0~70℃; Vcc = 3.13 ~ 3.60V, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits Min	Limits Typ	Limits Max	Unit
V_{CC}	Power supply voltage			3.13		3.60	V
V_{CCQ}	I/O buffer supply voltage			Vcc − 0.3		Vcc+0.3	V
V_{IH}	High-level input voltage			2.0		Vcc+0.3	V
V_{IL}	Low-level input voltage			−0.3 *		0.8	V
V_{OH}	High-level output voltage	I_{OH} = − 4mA		2.4			V
V_{OL}	Low-level output Voltage	I_{OL} = 8mA				0.4	V
I_I	Input current except ZZ, MODE and $\overline{FT}$	V_I = 0V~Vcc				2	μA
	Input current of MODE and $\overline{FT}$	V_I = Vcc				2	
		V_I = 0V				100	
	Input current of ZZ	V_I = Vcc				200	
		V_I = 0V				2	
I_{OZ}	Off - State output current	V_I ($\overline{OE}$) ≧V_{IH}, V_O = 0~Vcc				10	μA
I_{CC1}	Active power supply current	Output open Device selected V_I ≦V_{IL} or V_I ≧V_{IH} ZZ≦V_{IL}	AC (10.0ns cycle,100MHz)		250	300	mA
			AC (13.3ns cycle,75MHz)		140	200	
			AC (15.0ns cycle,66MHz)		125	170	
			AC (16.7ns cycle,60MHz)		110	160	
I_{CC2}	TTL Stand-by current	Device deselected V_I ≦V_{IL} or V_I ≧V_{IH} ZZ≦V_{IL}	AC (10.0ns cycle,100MHz)		75	95	mA
			AC (13.3ns cycle,75MHz)		55	70	
			AC (15.0ns cycle,66MHz)		50	65	
			AC (16.7ns cycle,60MHz)		45	60	
			CLK frequency= 0MHz All inputs statics		15	20	
I_{CC3}	CMOS Stand-by current (CLK stopped stand-by mode)	Output open VI ≦0.2V or VI ≧Vcc− 0.2V ZZ≦0.2V, $\overline{FT}$≧Vcc− 0.2V MODE≧Vcc− 0.2V CLK frequency=0MHz All inputs static	-6, -7, -8, -10		0.2	2	mA
			-7L, -8L, -10L		5	200	μA
I_{CC4}	Snooze mode Stand-by current	Snooze mode ZZ≧Vcc −0.2V $\overline{FT}$≧Vcc− 0.2V MODE≧Vcc− 0.2V	-6, -7, -8, -10		0.2	2	mA
			-7L, -8L, -10L		5	200	μA

Note 18. V_{IL}min * is −2.0V in case of AC (Pulse width ≦10ns).
19. "Device Deselected" means device is in POWER-DOWN mode as defined in the truth table.
20. Spec of I_{CC3} canbe supported by stopping CLK evenif device selected state.
21. I_{CC4} does not depend on CLK frequency and input level.

CAPACITANCE

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
CI	Input capacitance	VI = GND, VI = 25mVrms, f = 1MHz			6	pF
CO	Output capacitance	VO = GND, VO = 25mVrms, f = 1MHz			8	pF

This parameter is sampled.

THERMAL RESISTANCE

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
θ_{JA}	Thermal resistance - Junction to Ambient	Suspended in still air		89		℃/W
		Mounted on 70×70×1.6t Mitsubishi standard PC board, Air velocity = 0 m/s		72		
		Mounted on 70×70×1.6t Mitsubishi standard PC board, Air velocity = 1.0 m/s		57		
θ_{JC}	Thermal resistance - Junction to Case	Immersed in fluorinert		19		℃/W

This parameter is sampled.

AC ELECTRICAL CHARACTERISTICS (Ta = 0~70℃; Vcc = 3.13 ~ 3.60V, unless otherwise noted)

(1) MEASUREMENT CONDITIONS

Input pulse levels ..... VIH = 3.0V, VIL = 0V
Input rise and fall times 1.5ns
Input timing reference levels ..... VIH = 1.5V, VIL = 1.5V
Output reference levels ..... VOH = 1.5V, VOL = 1.5V
Output load ..... Fig. 1, 2

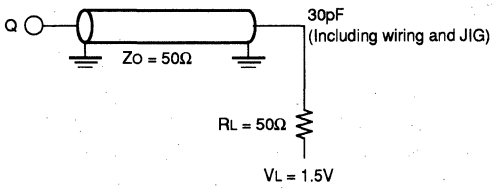


Fig. 1 Output load

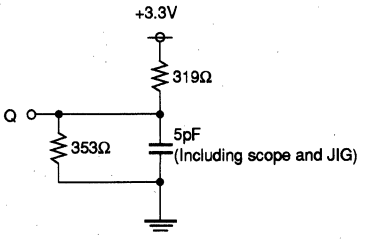


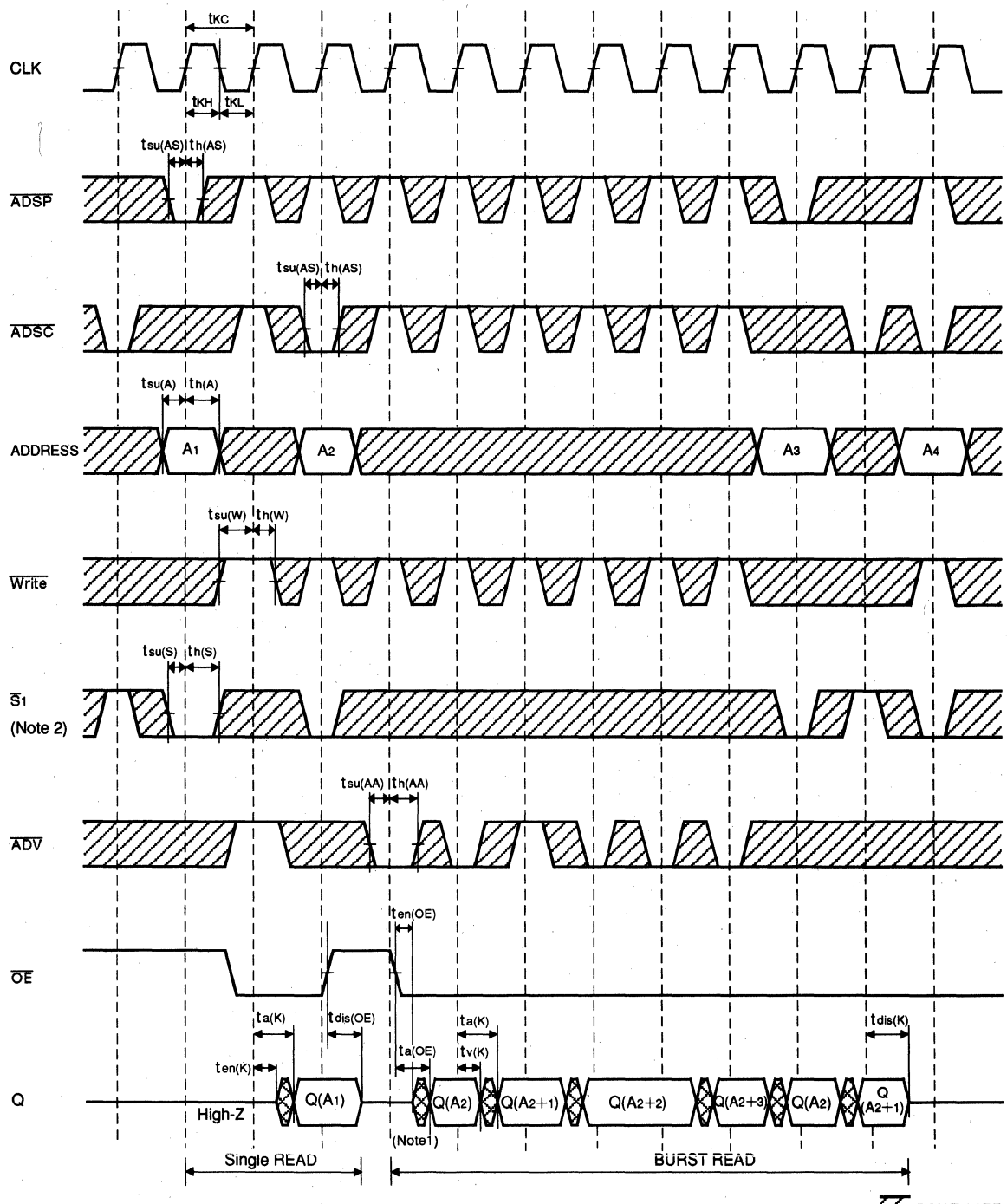
Fig. 2 Output load for ten, tdis

(2) TIMING CHARACTERISTICS

Symbol	Parameter	Limits								Unit
		100MHz		75MHz		66MHz		60MHz		
		-6		-7, -7L		-8, -8L		-10, -10L		
		Min	Max	Min	Max	Min	Max	Min	Max	
Clock										
t_{KC}	Clock cycle time	10		13.3		15		16.7		ns
t_{KH}	Clock HIGH time	3.5		5		6		6		ns
t_{KL}	Clock LOW time	3.5		5		6		6		ns
Output Times										
$t_{a(K)}$	Clock access time		5.5		7		8.0		10	ns
$t_{v(K)}$	Data valid time from Clock	2		2		3		3		ns
$t_{en(K)}$	Output enable time from Clock	0		0		0		0		ns
$t_{dis(K)}$	Output disable time from Clock	1	5.5	2	6	2	6	2	6	ns
$t_{a(OE)}$	OE access time		5.5		6		6		6	ns
$t_{en(OE)}$	Output enable time from OE	0		0		0		0		ns
$t_{dis(OE)}$	Output disable time from OE	1	5	2	6	2	6	2	6	ns
Setup Times										
$t_{su(A)}$	Address	2		2.5		2.5		2.5		ns
$t_{su(AS)}$	Address Status ($\overline{ADSC}$, $\overline{ADSP}$)	2		2.5		2.5		2.5		ns
$t_{su(AA)}$	Address Advance ($\overline{ADV}$)	2		2.5		2.5		2.5		ns
$t_{su(W)}$	Byte Write Enables ($\overline{MBW}$, $\overline{GW}$, $\overline{BWs}$)	2		2.5		2.5		2.5		ns
$t_{su(D)}$	Data-In	2		2.5		2.5		2.5		ns
$t_{su(S)}$	Chip Select enables ($\overline{S1}$, $\overline{S2}$, S2)	2		2.5		2.5		2.5		ns
Hold Times										
$t_{h(A)}$	Address	0.5		0.5		0.5		0.5		ns
$t_{h(AS)}$	Address Status ($\overline{ADSC}$, $\overline{ADSP}$)	0.5		0.5		0.5		0.5		ns
$t_{h(AA)}$	Address Advance ($\overline{ADV}$)	0.5		0.5		0.5		0.5		ns
$t_{h(W)}$	Byte Write Enables ($\overline{MBW}$, $\overline{GW}$, $\overline{BWs}$)	0.5		0.5		0.5		0.5		ns
$t_{h(D)}$	Data-In	0.5		0.5		0.5		0.5		ns
$t_{h(S)}$	Chip Select ($\overline{S1}$, $\overline{S2}$, S2)	0.5		0.5		0.5		0.5		ns
ZZ, MODE $\overline{FT}$										
t_{ZZS}	ZZ Stand-by		30		30		30		30	ns
t_{ZZREC}	ZZ Recovery	30		30		30		30		ns
t_{CFG}	Config setup (MODE, $\overline{FT}$)	40		53.3		60		66.7		ns

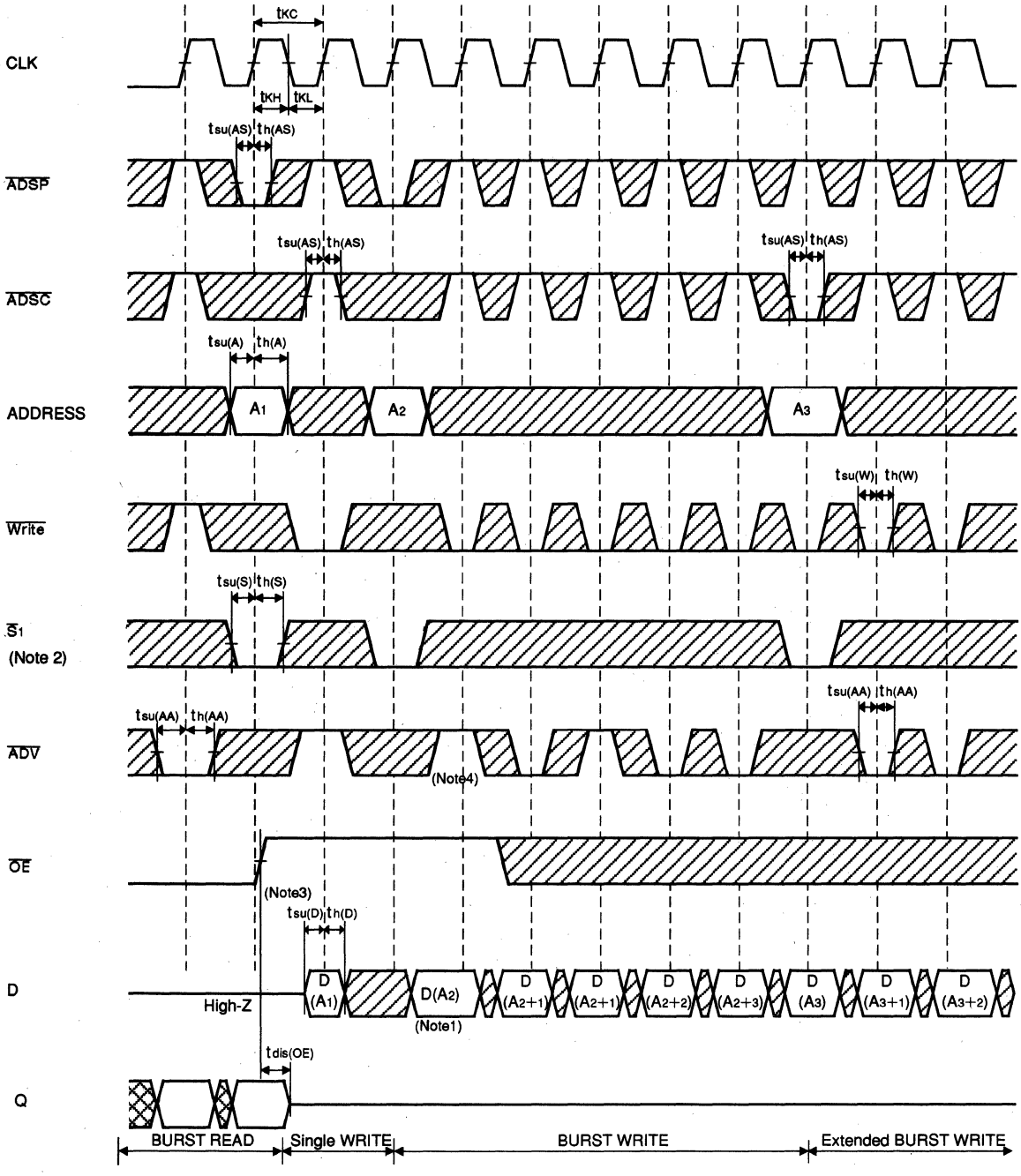
Note 22. All parameters except t_{ZZS}, t_{ZZREC} in this table are measured on condition that ZZ = LOW fix .
23. Test conditions is specified with the output loading shown in Fig. 1 unless otherwise noted.
24. When enable and disable time (t_{en}, t_{dis}) are measured, Output loading is specified with C_L = 5pF as in Fig. 2.
The transition is measured±500mV from steady state voltage.
25. The enable and disable time are sampled.
26. $\overline{ADSP}$ and $\overline{ADSC}$ must not be asserted during t_{ZZS} and t_{ZZREC}, due to a guarantee of data retention for snooze mode.
If synchronous inputs are made combinations of WRITE state during t_{ZZS}, memorized data may be destroyed.
27. Configuration signals (MODE and $\overline{FT}$)are static and must not change during normal operation.

(3) READ TIMING



Note 1. Q(A2) refers to output from address A2. Q(A2+1) refers to output from the next internal burst address following A2.
2. $\overline{S2}$ and S2 have timing identical to $\overline{S1}$. On this diagram, when $\overline{S1}$ is LOW, $\overline{S2}$ is LOW and S2 is HIGH.
When $\overline{S1}$ is HIGH, $\overline{S2}$ is HIGH and S2 is LOW.
3. ZZ = LOW fix.

(4) WRITE TIMING



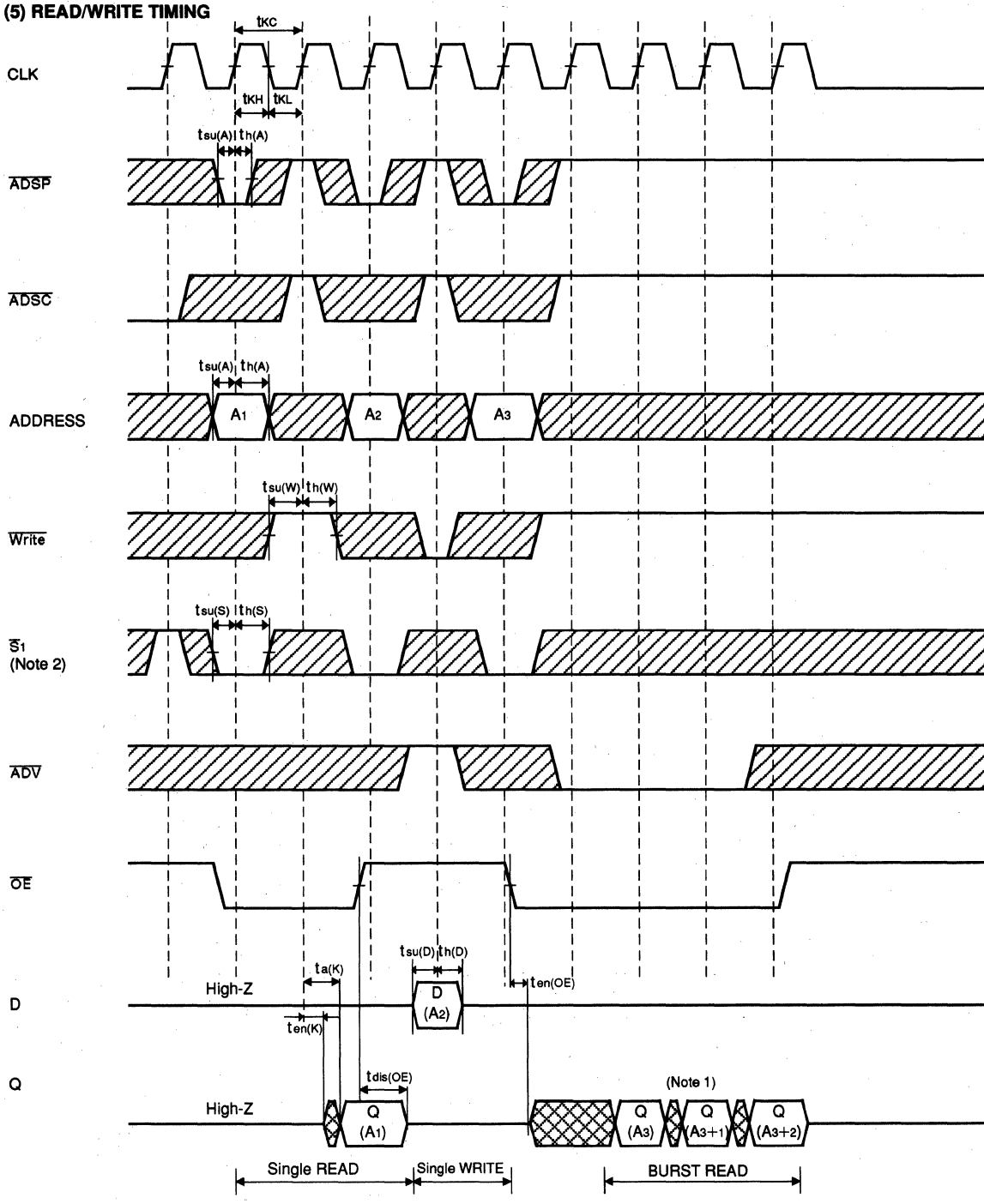
Note 1. Q(A2) refers to output from address A2. Q(A2+1) refers to output from the next internal burst address following A2.

2. $\overline{S2}$ and S2 have timing identical to $\overline{S1}$. On this diagram, when $\overline{S1}$ is LOW, $\overline{S2}$ is LOW and S2 is HIGH. When S1 is HIGH, S2 is HIGH and S2 is LOW.
3. $\overline{OE}$ must be HIGH before the input data setup and held HIGH throughout the data hold time. This prevents input/output data contention for the time period prior to the byte write enable inputs being sampled.
4. $\overline{ADV}$ must be high to permit a write to the loaded address.
5. ZZ = LOW fix.

DON'T CARE

UNDEFINED

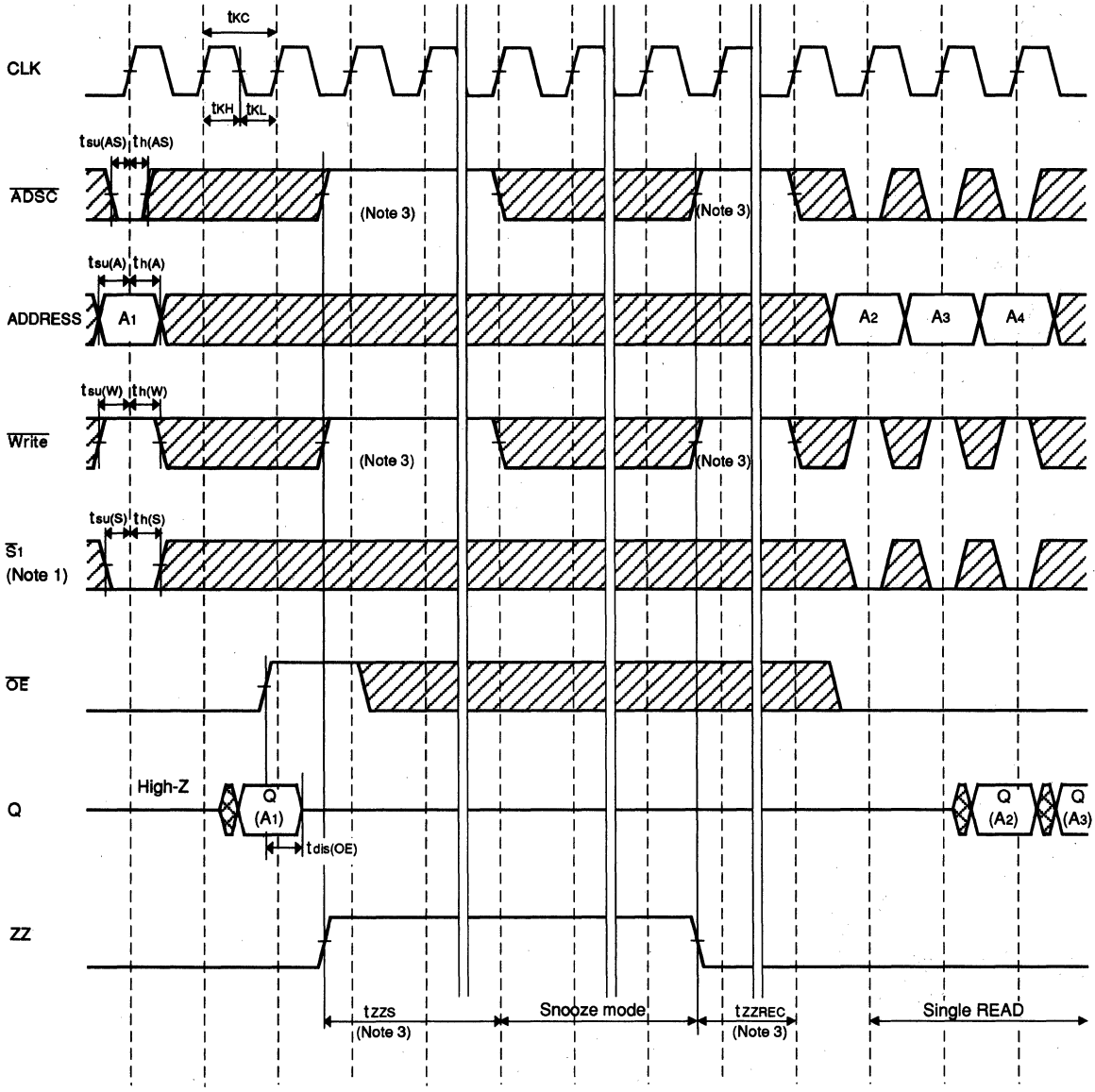
(5) READ/WRITE TIMING



Note 1. Q(A3) refers to output from address A3. Q(A3+1) refers to output from the next internal burst address following A3.
2. $\overline{S2}$ and S2 have timing identical to $\overline{S1}$. On this diagram, when $\overline{S1}$ is LOW, $\overline{S2}$ is LOW and S2 is HIGH. When $\overline{S1}$ is HIGH, $\overline{S2}$ is HIGH and S2 is LOW.
3. ZZ = LOW fix.

DON'T CARE
UNDEFINED

(6) SNOOZE MODE TIMING



Note 1. S2 and S2 have timing identical to S1. On this diagram, when S1 is LOW, S2 is LOW and S2 is HIGH.
When S1 is HIGH, S2 is HIGH and S2 is LOW.

2. On this timing chart, ADSP = HIGH fix, ADV = X.

3. ADSP and ADSC must not be asserted during tZZS and tZZREC, due to a guarantee of data retention for snooze mode.
If synchronous inputs are made combinations of WRITE state during tZZS and tZZREC, memorized data may be destroyed.

DON'T CARE

UNDEFINED

M5M5V1132AFP,GP-3,-4,-6,-7,-8

1048576-BIT(32768-WORD BY 32-BIT) SYNCHRONOUS BURST SRAM

DESCRIPTION

The M5M5V1132A is a family of 1M bit synchronous SRAMs organized as 32768-words of 32-bit. The M5M5V1132A provides a high speed secondary cache solution for microprocessors. The design integrates a 2-bit burst counter, input and output registers with the ultra fast 1M bit SRAM on a single monolithic circuit. This design reduces component count of cache data RAM solutions. Mitsubishi's SRAMs are fabricated with high-performance, low power Super (Advanced) CMOS technology, providing greater reliability. This device operates on a single 3.3V power supply and are directly LVTTL compatible.

FEATURES

- Access times /Cycle times
  - M5M5V1132AFP,GP-3 ..... 3.0ns/6.7ns (150MHz)
  - M5M5V1132AFP,GP-4 ..... 4.0ns/8.0ns (125MHz)
  - M5M5V1132AFP,GP-6 ..... 5.5ns/10.0ns (100MHz)
  - M5M5V1132AFP,GP-7 ..... 7.0ns/13.3ns (75MHz)
  - M5M5V1132AFP,GP-8 ..... 8.0ns/15.0ns (66MHz)
- Low power dissipation
  - Active (150 / 66MHz) ..... 726 / 413mW (typ)
  - Stand-by ..... 3.3mW (typ)
- Package
  100pin QFP, LQFP,Body Size (14.0×20.0 mm^2)
  Pin Pitch (0.65 mm)
- Single +3.3V power supply (3.13 ~ 3.60 V)
- Fully registered inputs and outputs (Pipeline operation)
- Global write control or individual byte write control
- MODE pin allows either liner or interleaved burst
- Snooze mode pin (ZZ) for power down
- CLK stopped stand-by mode
- 32-bit wide data I/O

APPLICATION

Pentium ™/PowerPC ™and High-end processor second level caches

FUNCTION

Synchronous circuitry allows for precise cycle control triggered by a positive edge clock transition. Synchronous signals include : all addresses, all data inputs, all chip selects ($\overline{S_1}$, $\overline{S_2}$, S_2), burst control inputs ($\overline{ADSC}$, $\overline{ADSP}$, $\overline{ADV}$) and write enables ($\overline{MBW}$, $\overline{GW}$, $\overline{BW_1}$, $\overline{BW_2}$, $\overline{BW_3}$, $\overline{BW_4}$). S_2 and $\overline{S_2}$ provide easy depth expansion.

The write operation can be performed by two methods. The global write enable ($\overline{GW}$) will perform a write to all 32 bits. Byte wide writes are controlled by the master byte write enable ($\overline{MWB}$) and the 4 individual byte write enables ($\overline{BW_1}$~$\overline{BW_4}$). The byte write cycle will write from one to four bytes. The write cycle is internally self-timed, eliminating the complex signal generation of an off chip write.

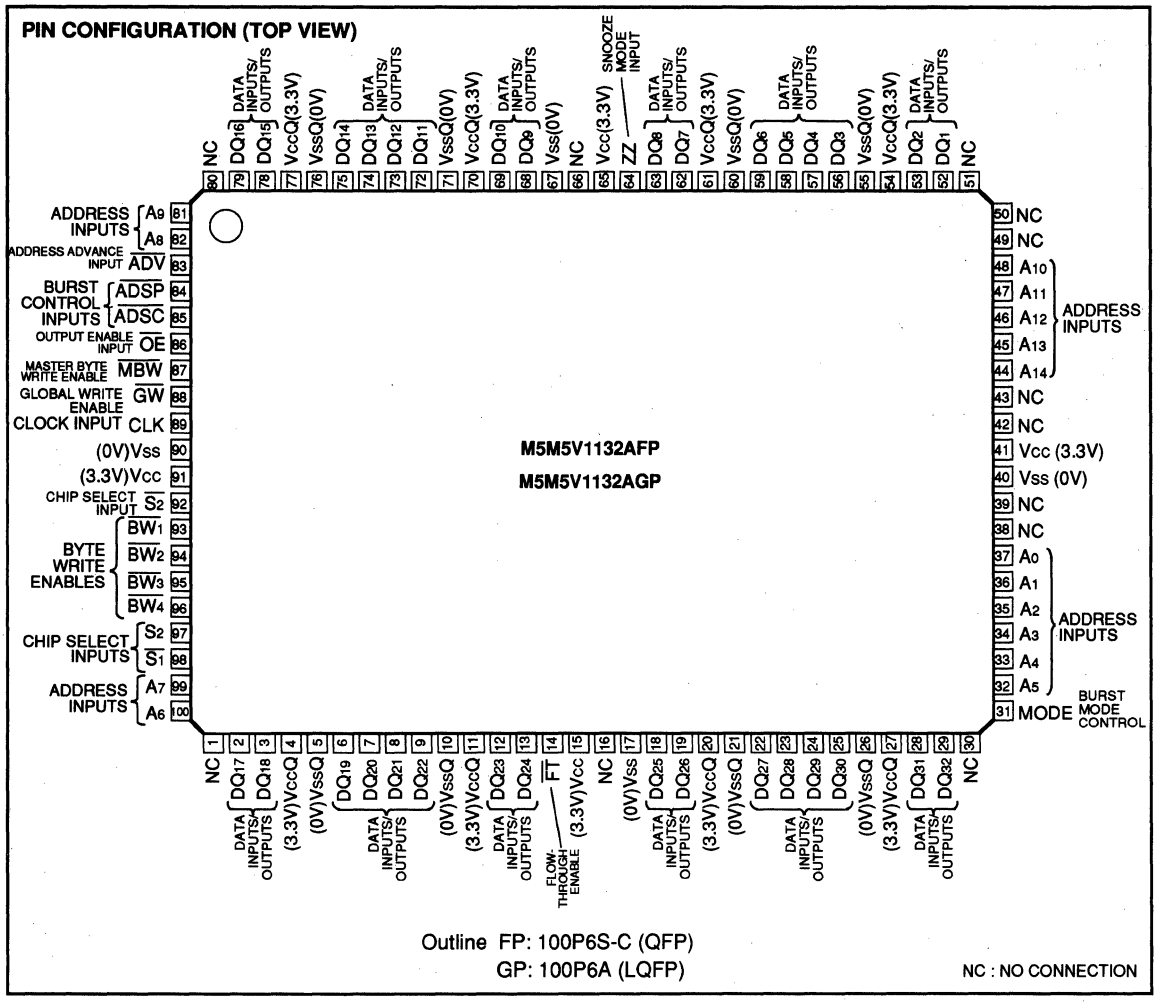
Asynchronous signals are output enable ($\overline{OE}$), snooze mode pin (ZZ) and clock (CLK). The HIGH input of ZZ pin puts the SRAM in the power-down state. When ZZ is pulled to LOW, the SRAM normally operates after 30ns of the wake up period.

When CLK is stopped and all inputs (Address, Burst control, CLK etc.) are fixed in CMOS level, the SRAM becomes in the power-down state that is called "CLK stopped stand-by mode". During CLK stopped stand-by mode, power supply current is almost same as snooze mode even if the SRAM is selected. When CLK is active again, the SRAM immediately recovers from CLK stopped stand-by mode to normal operation mode.

The burst mode control (MODE), and the flow-through enable ($\overline{FT}$) are DC operated pins. MODE pin will allow the choice of either an interleaved burst, or a linear burst. $\overline{FT}$ pin normally is pulled VccQ. When $\overline{FT}$ is Vss, the SRAM changes non-pipelined type with flow-through output. $\overline{FT}$ Vss input is only used for a test mode.

The burst operation is initiated by either address status processor ($\overline{ADSP}$) or address status controller ($\overline{ADSC}$). The burst advance pin ($\overline{ADV}$) controls subsequent burst addresses.

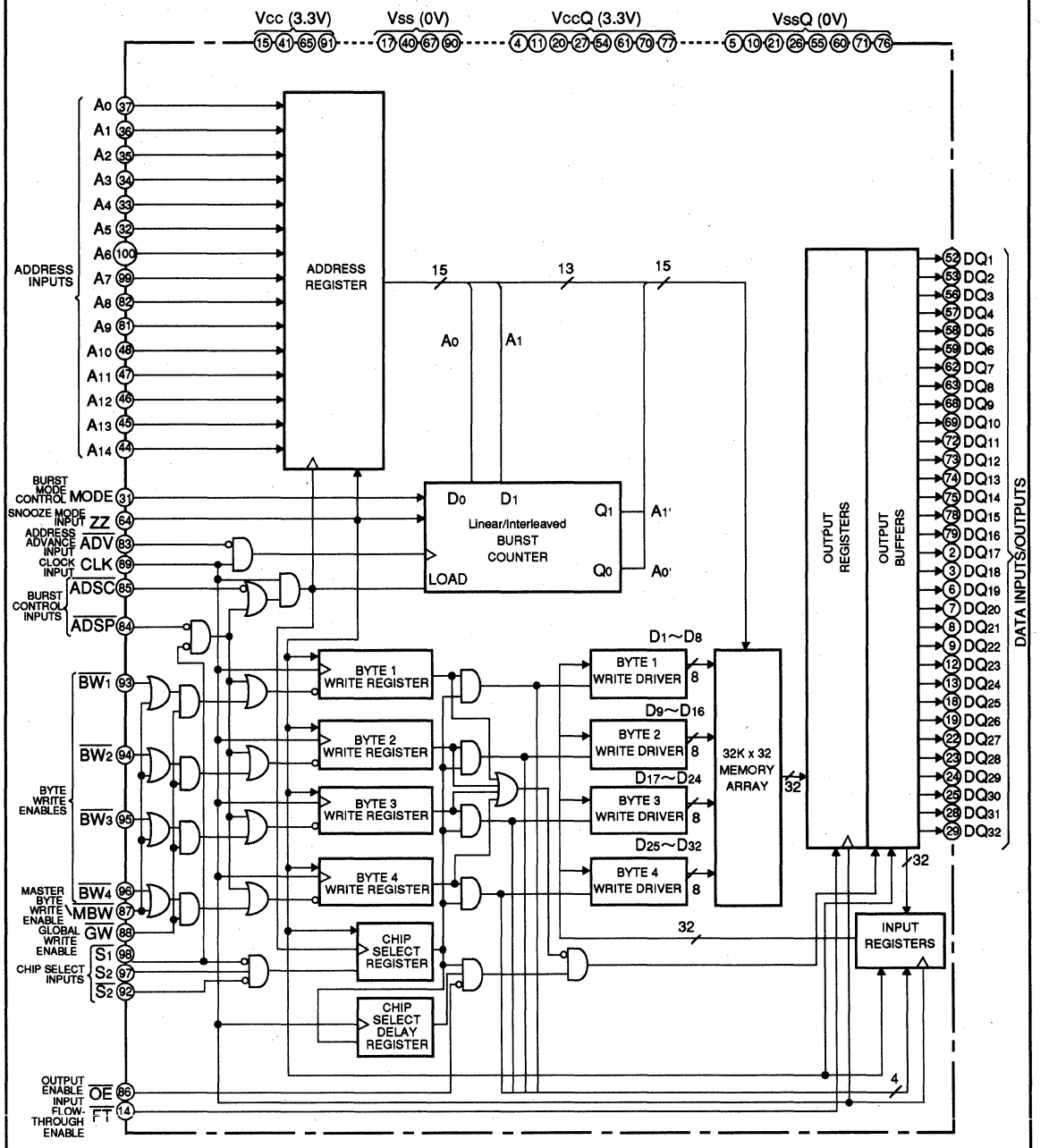
PIN CONFIGURATION (TOP VIEW)



Outline FP: 100P6S-C (QFP)
GP: 100P6A (LQFP)

NC : NO CONNECTION

BLOCK DIAGRAM



Note: The Block Diagram illustrates simplified device operation. See Truth Table, pin descriptions and timing diagrams for detailed information.

PIN FUNCTIONS

Pin	Name	Function
A_0~A_{14}	Synchronous Address Inputs	These inputs are registered and must meet the setup and hold times around the rising edge of CLK.
$\overline{MBW}$	Synchronous Master Byte Write Enables	This active LOW input is used to enable the individual byte write operation. The individual byte write operation is performed when $\overline{MBW}$ is LOW and $\overline{GW}$ is HIGH. The global write operation (a write to all 32 bits) is performed when $\overline{GW}$ is LOW.
$\overline{GW}$	Synchronous Global Write Enables	This active LOW input is used to enable the global write operation (a write to all 32 bits) and must meet the setup and hold times around the rising edge of CLK.
$\overline{BW_1}$, $\overline{BW_2}$, $\overline{BW_3}$, $\overline{BW_4}$	Synchronous Byte Write Enables	These active LOW inputs allow individual bytes to be written and must meet the setup and hold times around the rising edge of CLK. A byte write enables is LOW for a WRITE cycle and HIGH for a READ cycle. $\overline{BW_1}$ controls DQ_1~DQ_8. $\overline{BW_2}$ controls DQ_9~DQ_{16}. $\overline{BW_3}$ controls DQ_{17}~DQ_{24}. $\overline{BW_4}$ controls DQ_{25}~DQ_{32}. Data I/O are tristated if any of these four inputs are LOW.
CLK	Clock Input	This signal latches the address, data, chip enables, byte write enables and burst control inputs on its rising edge. All synchronous inputs must meet setup and hold times around the clock's rising edge.
$\overline{S_1}$	Synchronous Chip Select Input	This active LOW input is used to enable the device and conditions internal use of $\overline{ADSP}$. This input is sampled only when a new external address is loaded.
$\overline{S_2}$	Synchronous Chip Select Input	This active LOW input is used to enable the device. This input is sampled only when a new external address is loaded. This input can be used for memory depth expansion.
S_2	Synchronous Chip Select Input	This active HIGH input is used to enable the device. This input is sampled only when a new external address is loaded. This input can be used for memory depth expansion.
$\overline{OE}$	Output Enable Input	This active LOW asynchronous input enables the data I/O output drivers.
DQ_1~DQ_{32}	Data I/O	Byte 1 is DQ_1~DQ_8; Byte 2 is DQ_9~DQ_{16}; Byte 3 is DQ_{17}~DQ_{24}; Byte 4 is DQ_{25}~DQ_{32}. Input data must meet setup and hold times around the rising edge of CLK.
ZZ	Snooze Mode Input	This asynchronous input allows the selection either normal operation mode or snooze mode that the SRAM is in the power-down state even if CLK is operated. This active HIGH asynchronous input puts the SRAM in the snooze mode. At this time, the data I/O output drivers are disabled and input leak current flows to this pin. When this pin is LOW or NC, the SRAM normally operates.
MODE	Burst Mode Control	This DC operated pin allows the choice of either a interleaved burst or a linear burst. If this pin is VccQ or NC, an interleaved burst occurs. When this pin is Vss, a linear burst occurs, and input leak current flows to this pin.
$\overline{FT}$	Flow-through Enable	This DC operated pin is used as a test mode pin. Normally, this pin is pulled VccQ or NC. When this pin is Vss, the SRAM changes non-pipelined type with flow-through output, and input leak current flows to this pin.
$\overline{ADSP}$	Synchronous Address Status Processor	This active LOW input interrupts any ongoing burst, causing a new external address to be latched. A READ is performed using the new address, independent of the byte write enables and $\overline{ADSC}$ but dependent upon S_2 and $\overline{S_2}$. $\overline{ADSP}$ is ignored if $\overline{S_1}$ is HIGH. Power-down state is entered if S_2 is LOW or $\overline{S_2}$ is HIGH.
$\overline{ADSC}$	Synchronous Address Status Controller	This active LOW input interrupts any ongoing burst and causes a new external address to be latched. A READ or WRITE is performed using the new address if all chip enables are active. Power-down state is entered if one or more chip enables are inactive.
$\overline{ADV}$	Synchronous Address Advance	This active LOW input is used to advance the internal burst counter, controlling burst access after the external address is loaded. A HIGH on this pin effectively causes wait states to be generated (no address advance). This pin must be HIGH at the rising edge of the first clock after an $\overline{ADSP}$ cycle is initiated if a WRITE cycle is desired (to ensure use of correct address)
Vcc	Vcc	Power Supply (3.3V)
Vss	Vss	Ground (0V)
VccQ	VccQ	I/O Buffer Supply (3.3V)
VssQ	VssQ	I/O Buffer Ground (0V)

DC OPERATED TRUTH TABLE

Name	Input status	Operation
MODE	VccQ or NC	Interleaved Burst Sequence
	Vss	Linear Burst Sequence
$\overline{FT}$	VccQ or NC	Pipelined SRAM
	Vss	Non-pipelined SRAM (Test mode)

Note 1. MODE and $\overline{FT}$ are DC operated pins.
2. NC means No-Connection.
3. Normally, $\overline{FT}$ is pulled to VccQ or NC. $\overline{FT}$ input fixed to Vss is only used for a test mode.
4. See BURST SEQUENCE TABLE about Interleaved and Linear Burst Sequence.

BURST SEQUENCE TABLE

Interleaved Burst Sequence (when MODE = VccQ or NC)

Operation	A_{14} -A_2	A_1	A_0
First access, latch external address	A_{14} -A_2	A_1	A_0
Second access (first burst address)	latched A_{14} -A_2	latched A_1	latched $\overline{A_0}$
Third access (second burst address)	latched A_{14} -A_2	latched $\overline{A_1}$	latched A_0
Fourth access (third burst address)	latched A_{14} -A_2	latched $\overline{A_1}$	latched $\overline{A_0}$

Linear Burst Sequence (when MODE = Vss)

Operation	A_{14} -A_2	A_1, A_0			
First access, latch external address	A_{14} -A_2	0, 0	0, 1	1, 0	1, 1
Second access (first burst address)	latched A_{14} -A_2	0, 1	1, 0	1, 1	0, 0
Third access (second burst address)	latched A_{14} -A_2	1, 0	1, 1	0, 0	0, 1
Fourth access (third burst address)	latched A_{14} -A_2	1, 1	0, 0	0, 1	1, 0

Note 5. The burst sequence wraps around to its initial state upon completion.

SYNCHRONOUS TRUTH TABLE

$\overline{S_1}$	$\overline{S_2}$	S_2	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{Write}$	CLK	Address used	Operation
H	X	X	X	L	X	X	L-H	None	Deselected Cycle, Power-down
L	X	L	L	X	X	X	L-H	None	Deselected Cycle, Power-down
L	H	X	L	X	X	X	L-H	None	Deselected Cycle, Power-down
L	X	L	X	L	X	X	L-H	None	Deselected Cycle, Power-down
L	H	X	X	L	X	X	L-H	None	Deselected Cycle, Power-down
L	L	H	L	X	X	X	L-H	External	READ Cycle, Begin Burst
L	L	H	H	L	X	L	L-H	External	WRITE Cycle, Begin Burst
L	L	H	H	L	X	H	L-H	External	READ Cycle, Begin Burst
X	X	X	H	H	L	H	L-H	Next	READ Cycle, Continue Burst
H	X	X	X	H	L	H	L-H	Next	READ Cycle, Continue Burst
X	X	X	H	H	L	L	L-H	Next	WRITE Cycle, Continue Burst
H	X	X	X	H	L	L	L-H	Next	WRITE Cycle, Continue Burst
X	X	X	H	H	H	H	L-H	Current	READ Cycle, Suspend Burst
H	X	X	X	H	H	H	L-H	Current	READ Cycle, Suspend Burst
X	X	X	H	H	H	L	L-H	Current	WRITE Cycle, Suspend Burst
H	X	X	X	H	H	L	L-H	Current	WRITE Cycle, Suspend Burst

Note 6. X means "don't care". H means logic HIGH. L means logic LOW.
7. $\overline{Write}$ =L means "WRITE" operation in WRITE TRUTH TABLE.
$\overline{Write}$ =H means "READ" operation in WRITE TRUTH TABLE.
8. All inputs in this table must meet setup and hold times around the rising edge (LOW to HIGH) of CLK.
9. $\overline{ADSP}$ LOW always initiates an internal READ at the L-H edge of CLK.
10. Operation finally depends on status of asynchronous input pins (ZZ and $\overline{OE}$).
See ASYNCHRONOUS TRUTH TABLE.

WRITE TRUTH TABLE

$\overline{GW}$	$\overline{MBW}$	$\overline{BW_1}$	$\overline{BW_2}$	$\overline{BW_3}$	$\overline{BW_4}$	Operation
H	H	X	X	X	X	READ
H	L	H	H	H	H	READ
H	L	L	H	H	H	WRITE BYTE 1
H	L	H	L	H	H	WRITE BYTE 2
H	L	H	H	L	H	WRITE BYTE 3
H	L	H	H	H	L	WRITE BYTE 4
H	L	L	L	H	H	WRITE BYTE1 and 2
H	L	H	H	L	L	WRITE BYTE3 and 4
H	L	L	L	L	L	WRITE ALL BYTE
L	X	X	X	X	X	WRITE ALL BYTE

Note 11. X means "don't care". H means logic HIGH. L means logic LOW.
12. All inputs in this table must meet setup and hold ties around the rising edge (LOW to HIGH) of CLK.

ASYNCHRONOUS TRUTH TABLE

ZZ	$\overline{OE}$	Operation of synchronous truth table	Operation	I/O Status
H	X	X	Snooze mode	High-Z
L or NC	L	READ	READ	Q
L or NC	H	READ	READ	High-Z
L or NC	X	WRITE	WRITE	High-Z - D
L or NC	X	Deselected	Deselected	High-Z

Note 13. For a write operation following a read operation, $\overline{OE}$ must be HIGH before the input data required setup time and held HIGH through the input data hold time.
14. In I/O STATUS, Q means output data during a read cycle, and D means input data during a write cycle.
15. "Snooze mode" means power down state of which stand-by current does not depend on cycle time.
16. "Deselected" means power down state of which stand-by current depends on cycle time.
17. When ZZ is pulled to LOW, the SRAM normally operates after 30ns of the wake up period.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Power supply voltage	With respect to GND	−2.0 * ~4.6	V
V_{CCQ}	I/O buffer supply voltage		−2.0 * ~Vcc+0.5 (max 4.6)	V
V_I	Input voltage		−2.3 ~VccQ+2.3 ** (max 5.3)	V
V_O	Output voltage		−2.0 * ~4.6	V
P_d	Maximum power dissipation		1.2	W
T_{opr}	Operating temperature		0~70	℃
$T_{stg(bias)}$	Storage temperature (bias)		−10~85	℃
T_{stg}	Storage temperature		−65~150	℃

* This is −2.0V when pulse width ≦ 10ns, and −0.5V in case of DC.

**This is −2.3V~VccQ+2.3V(max5.3) when pulse width ≦ 3ns, and −0.5V~VccQ+0.5V (max4.6V) in case of DC.

DC ELECTRICAL CHARACTERISTICS (Ta = 0~70℃; Vcc = 3.13~3.60V, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits Min	Limits Typ	Limits Max	Unit
V_{CC}	Power Supply Voltage			3.13		3.60	V
V_{CCQ}	I/O Buffer Supply Voltage			Vcc-0.3		Vcc+0.3	V
V_{IH}	High-level input Voltage			2.0		VccQ+0.3*	V
V_{IL}	Low-level input Voltage			−0.3 *		0.8	V
V_{OH}	High-level output Voltage	I_{OH} = − 4mA		2.4			V
V_{OL}	Low-level output Voltage	I_{OL} = 8mA				0.4	V
I_I	Input current except ZZ, MODE and $\overline{FT}$	V_I = 0V~Vcc				2	μA
	Input current of MODE and $\overline{FT}$	V_I = Vcc				2	
		V_I = 0V				100	
	Input current of ZZ	V_I = Vcc				200	
		V_I = 0V				2	
I_{OZ}	Off - State output current	V_I ($\overline{OE}$) ≧V_{IH}, V_O = 0~Vcc				10	μA
I_{CC1}	Active power supply current	Output Open Device Selected V_I ≦V_{IL} or V_I ≧V_{IH} ZZ≦V_{IL}	AC (6.7ns cycle,150MHz)		220	260	mA
			AC (8.0ns cycle,125MHz)		200	240	
			AC (10.0ns cycle,100MHz)		170	220	
			AC (13.3ns cycle,75MHz)		140	200	
			AC (15.0ns cycle,66MHz)		125	170	
I_{CC2}	TTL Stand-by current	Device Deselected V_I ≦V_{IL} or V_I ≧V_{IH} ZZ≦V_{IL}	AC (6.7ns cycle,150MHz)		100	120	mA
			AC (8.0ns cycle,125MHz)		80	95	
			AC (10.0ns cycle,100MHz)		70	85	
			AC (13.3ns cycle,75MHz)		55	70	
			AC (15.0ns cycle,66MHz)		50	65	
			CLK frequency= 0MHz All inputs statics		15	20	
I_{CC3}	CMOS Stand-by current (CLK stopped stand-by mode)	Output Open V_I ≦0.2V or V_I ≧Vcc− 0.2V ZZ≦0.2V $\overline{FT}$≧Vcc− 0.2V MODE≧Vcc− 0.2V CLKfrequency=0MHz All inputs static			1	2	mA
I_{CC4}	Snooze mode Stand-by current	Snooze mode ZZ≧Vcc −0.2V $\overline{FT}$≧Vcc− 0.2V MODE≧Vcc− 0.2V			1	2	mA

Note 18. ** V_{IL}min is −2.3V and VIHmax is VccQ+2.3V in case of AC (Pulse width ≦3ns).
19. "Device Deselected" means device is in POWER-DOWN mode as defined in the truth table.
20. When CLK is stopped and all inputs are fixed in CMOS level, spec. of ICC3 can be achieved even if device selected state.
21. I_{CC4} does not depend on CLK frequency and input level.

CAPACITANCE

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
C_I	Input capacitance	V_I = GND, V_I = 25mVrms, f = 1MHz			6	pF
C_O	Output capacitance	V_O = GND, V_O = 25mVrms, f = 1MHz			8	pF

This parameter is sampled.

THERMAL RESISTANCE

Symbol	Parameter	Test conditions	Limits						Unit
			M5M5V1132AFP			M5M5V1132AGP			
			Min	Typ	Max	Min	Typ	Max	
θ_{JA}	Thermal resistance - Junction to Ambient	Mounted on 70×70×1.6t Mitsubishi standard PC board, Air velocity = 0 m/s		61			68		°C/W
		Mounted on 70×70×1.6t Mitsubishi standard PC board, Air velocity = 1.0 m/s		43			49		
θ_{JC}	Thermal resistance - Junction to Case	Immersed in fluorinert		21			12		°C/W

This parameter is sampled.

AC ELECTRICAL CHARACTERISTICS (Ta = 0~70°C; Vcc = 3.13~3.60V, unless otherwise noted)

(1) MEASUREMENT CONDITIONS

Input pulse levels ..... V_{IH} = 3.0V, V_{IL} = 0V
Input rise and fall times 1.5ns
Input timing reference levels ..... V_{IH} = 1.5V, V_{IL} = 1.5V
Output reference levels ..... V_{OH} = 1.5V, V_{OL} = 1.5V
Output load ..... Fig. 1, 2

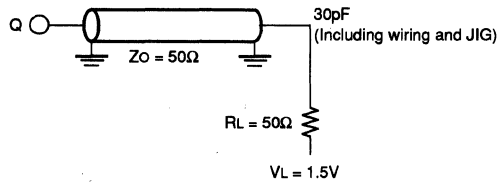


Fig. 1 Output load

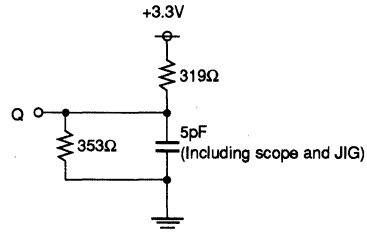


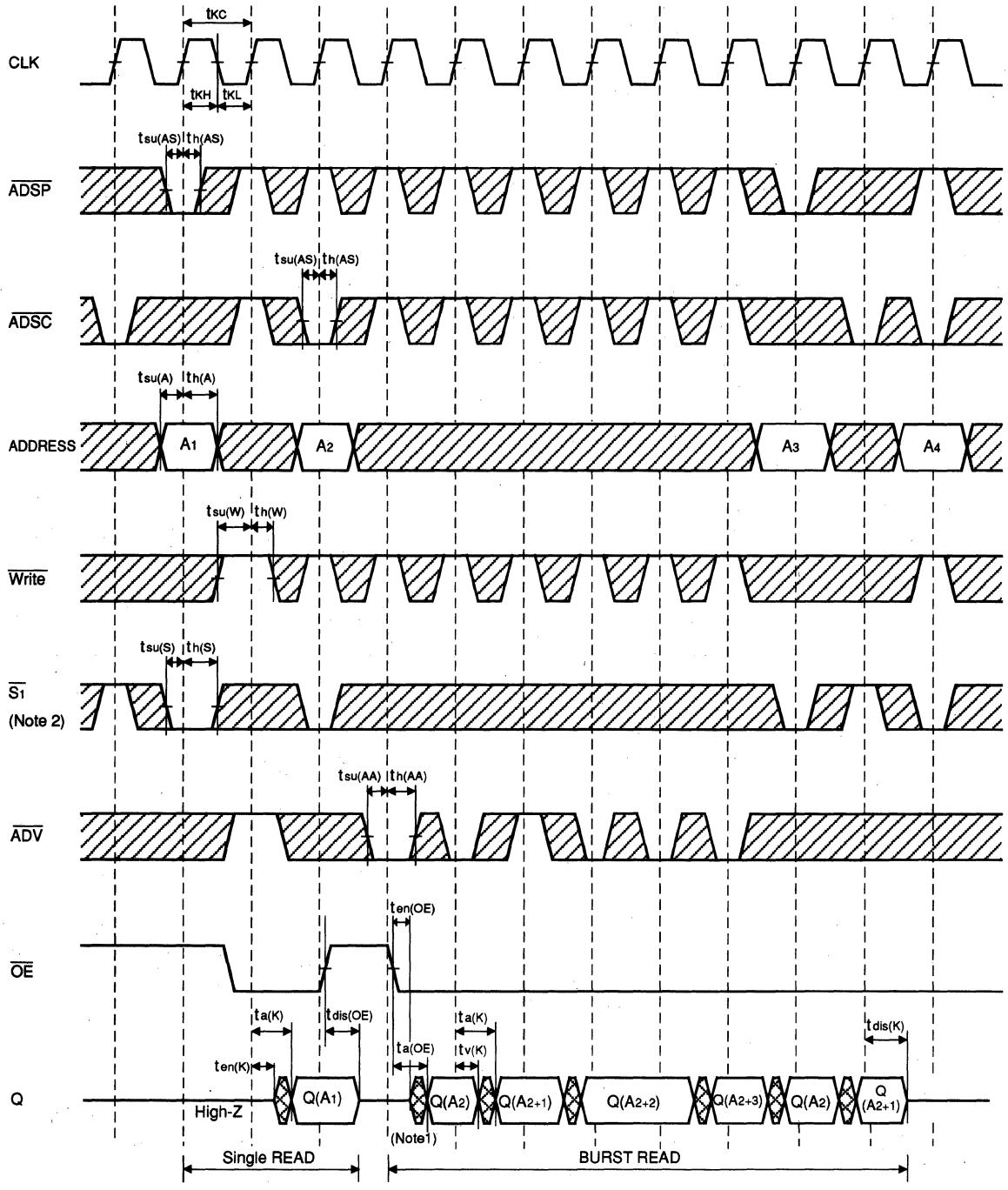
Fig. 2 Output load for ten, tdis

(2) TIMING CHARACTERISTICS

Symbol	Parameter	Limits										Unit
		150MHz		125MHz		100MHz		75MHz		66MHz		
		-3		-4		-6		-7		-8		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Clock												
t_{KC}	Clock cycle time	6.7		7.5		10		13.3		15		ns
t_{KH}	Clock HIGH time	2		3		3.5		5		6		ns
t_{KL}	Clock LOW time	2		3		3.5		5		6		ns
Output Times												
$t_{a(K)}$	Clock access time		3		4		5.5		7		8	ns
$t_{v(K)}$	Data valid time from Clock	1		2		2		2		3		ns
$t_{en(K)}$	Output enable time from Clock	0		0		0		0		0		ns
$t_{dis(K)}$	Output disable time from Clock	1	3	1	4	1	5.5	2	6	2	6	ns
$t_{a(OE)}$	$\overline{OE}$ access time		3		4		5.5		6		6	ns
$t_{en(OE)}$	Output enable time from $\overline{OE}$	0		0		0		0		0		ns
$t_{dis(OE)}$	Output disable time from $\overline{OE}$	1	3	1	4	1	5	2	6	2	6	ns
Setup Times												
$t_{su(A)}$	Address	2		2		2		2.5		2.5		ns
$t_{su(AS)}$	Address Status ($\overline{ADSC}$, $\overline{ADSP}$)	2		2		2		2.5		2.5		ns
$t_{su(AA)}$	Address Advance ($\overline{ADV}$)	2		2		2		2.5		2.5		ns
$t_{su(W)}$	Byte Write Enables ($\overline{MBW}$, $\overline{GW}$, $\overline{BWs}$)	2		2		2		2.5		2.5		ns
$t_{su(D)}$	Data-In	2		2		2		2.5		2.5		ns
$t_{su(S)}$	Chip Select enables ($\overline{S_1}$, $\overline{S_2}$, S_2)	2		2		2		2.5		2.5		ns
Hold Times												
$t_{h(A)}$	Address	0.5		0.5		0.5		0.5		0.5		ns
$t_{h(AS)}$	Address Status ($\overline{ADSC}$, $\overline{ADSP}$)	0.5		0.5		0.5		0.5		0.5		ns
$t_{h(AA)}$	Address Advance ($\overline{ADV}$)	0.5		0.5		0.5		0.5		0.5		ns
$t_{h(W)}$	Byte Write Enables ($\overline{MBW}$, $\overline{GW}$, $\overline{BWs}$)	0.5		0.5		0.5		0.5		0.5		ns
$t_{h(D)}$	Data-In	0.5		0.5		0.5		0.5		0.5		ns
$t_{h(S)}$	Chip Select ($\overline{S_1}$, $\overline{S_2}$, S_2)	0.5		0.5		0.5		0.5		0.5		ns
ZZ, MODE, $\overline{FT}$												
t_{ZZS}	ZZ Stand-by		30		30		30		30		30	ns
t_{ZZREC}	ZZ Recovery	30		30		30		30		30		ns
t_{CFG}	Config setup (MODE, $\overline{FT}$)	26.7		30		40		53.3		60		ns

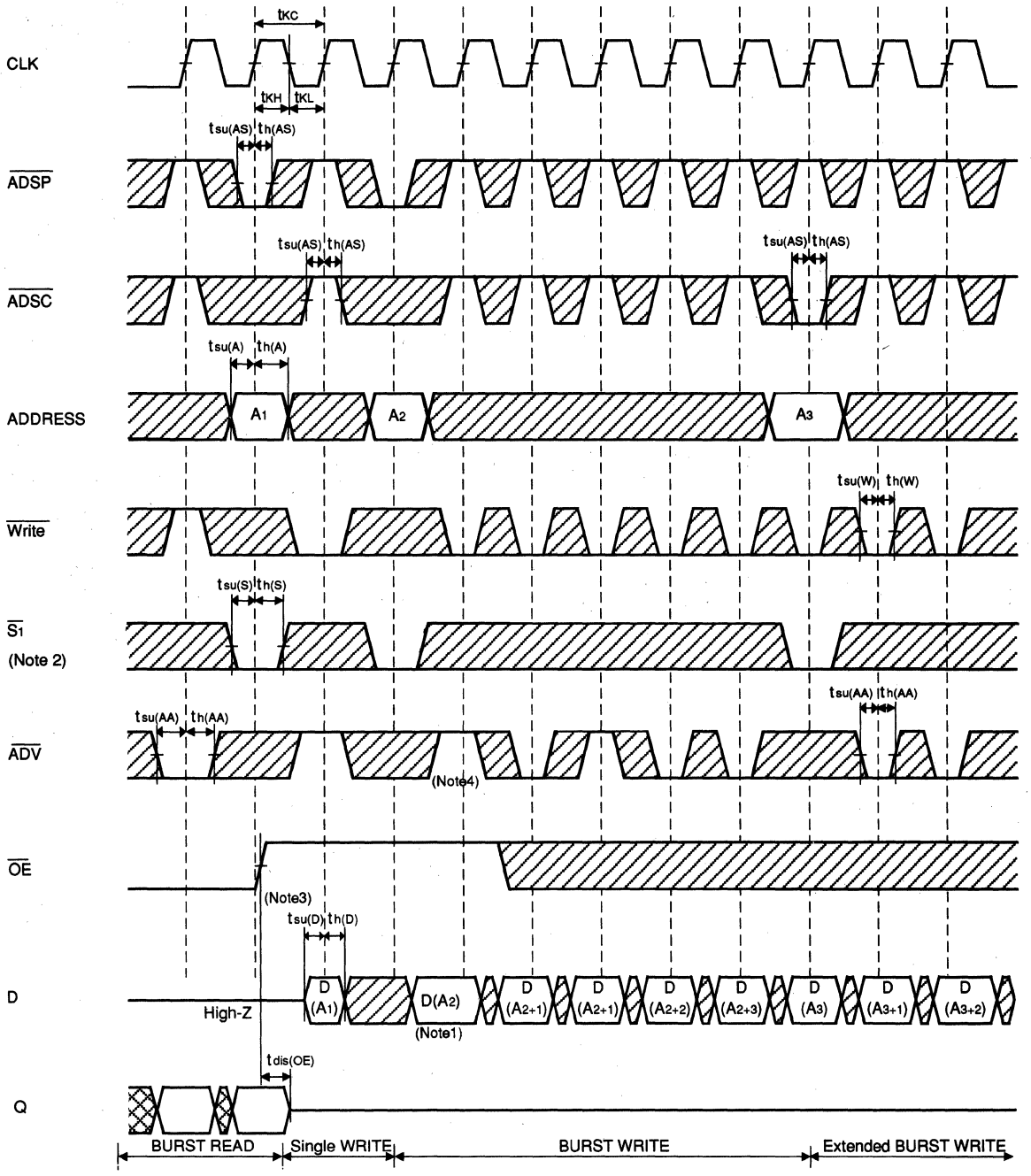
Note 22. All parameters except t_{ZZS}, t_{ZZREC} in this table are measured on condition that ZZ = LOW fix .
23. Test conditions is specified with the output loading shown in Fig. 1 unless otherwise noted.
24. When enable and disable time (t_{en}, t_{dis}) are measured, Output loading is specified with C_L = 5pF as in Fig. 2.
The transition is measured±500mV from steady state voltage.
25. The enable and disable time are sampled.
26. $\overline{ADSP}$ and $\overline{ADSC}$ must not be asserted during t_{ZZS} and t_{ZZREC}, due to a guarantee of data retention for snooze mode.
If synchronous inputs are made combinations of WRITE state during t_{ZZS}, memorized data may be destroyed.
27. Configuration signals (MODE and $\overline{FT}$)are static and must not change during normal operation.

(3) READ TIMING



Note 1. Q(A2) refers to output from address A2. Q(A2+1) refers to output from the next internal burst address following A2.
2. $\overline{S2}$ and S2 have timing identical to $\overline{S1}$. On this diagram, when $\overline{S1}$ is LOW, $\overline{S2}$ is LOW and S2 is HIGH.
When $\overline{S1}$ is HIGH, $\overline{S2}$ is HIGH and S2 is LOW.
3. ZZ = LOW fix.

(4) WRITE TIMING



Note 1. Q(A2) refers to output from address A2. Q(A2+1) refers to output from the next internal burst address following A2.
2. $\overline{S2}$ and S2 have timing identical to $\overline{S1}$. On this diagram, when $\overline{S1}$ is LOW, $\overline{S2}$ is LOW and S2 is HIGH. When $\overline{S1}$ is HIGH, $\overline{S2}$ is HIGH and S2 is LOW.
3. $\overline{OE}$ must be HIGH before the input data setup and held HIGH throughout the data hold time. This prevents input/output data contention for the time period prior to the byte write enable inputs being sampled.
4. $\overline{ADV}$ must be high to permit a write to the loaded address.
5. ZZ = LOW fix.

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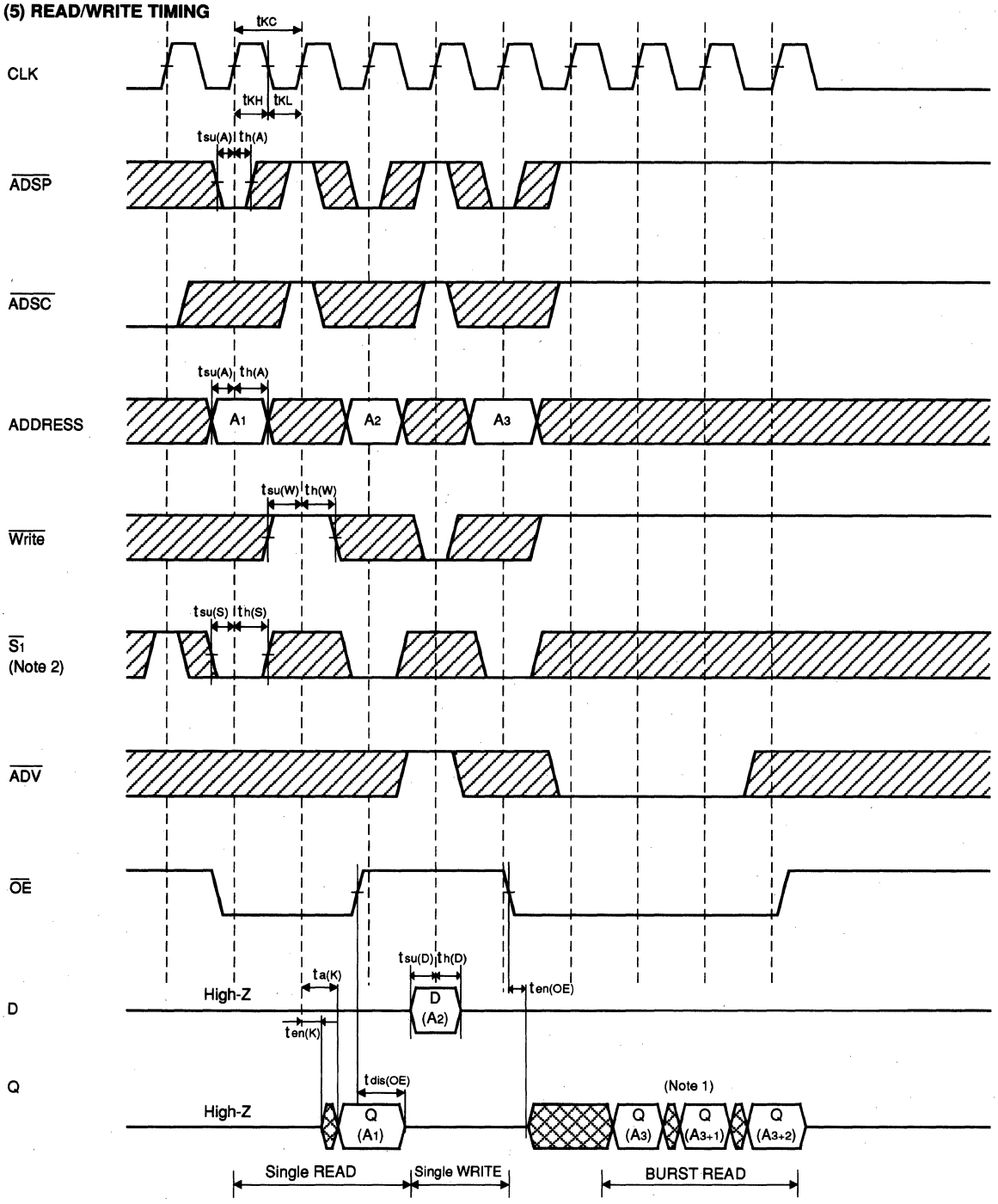
(5) READ/WRITE TIMING



Note 1. Q(A3) refers to output from address A3. Q(A3+1) refers to output from the next internal burst address following A3.

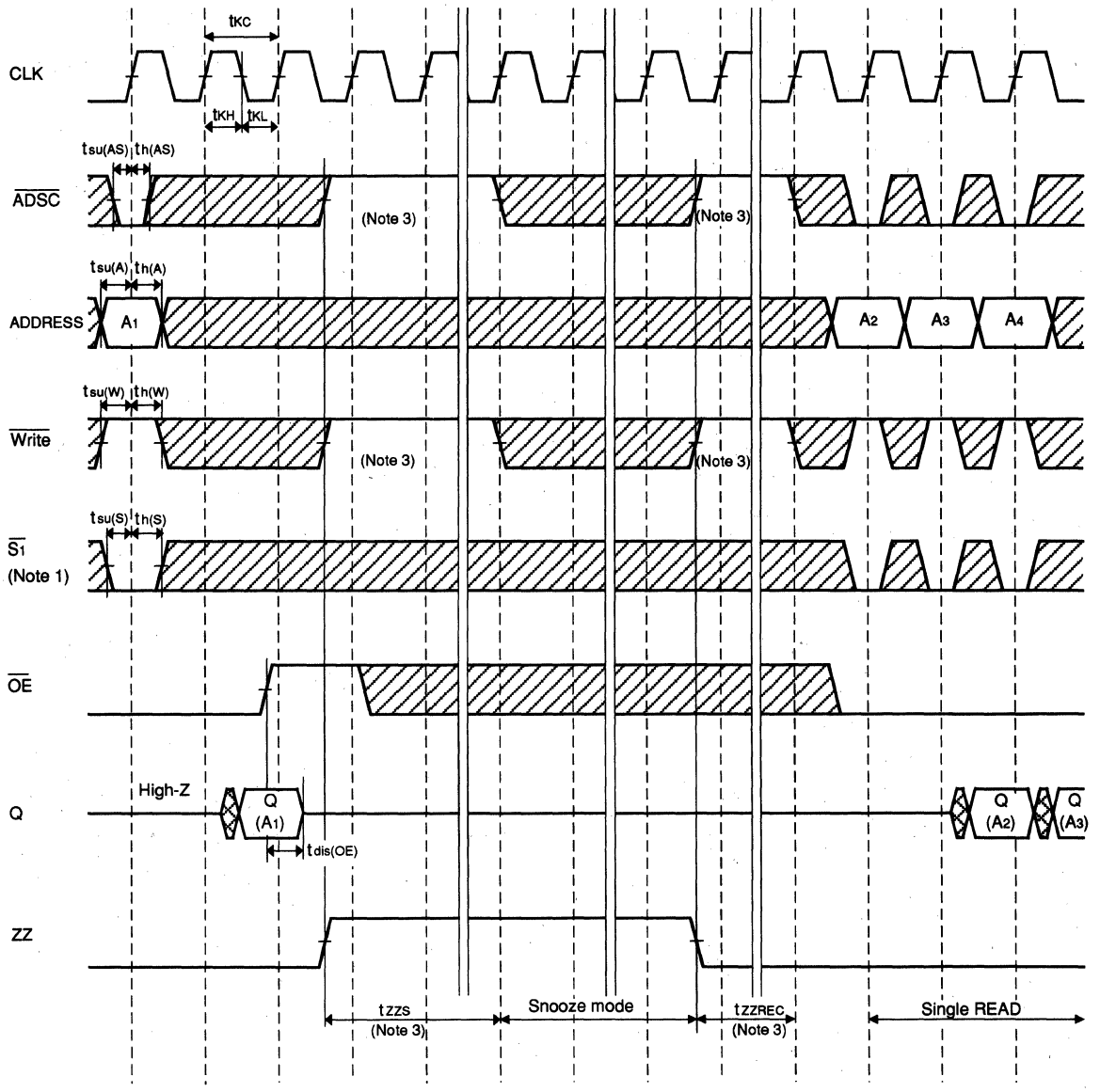
2. $\overline{S2}$ and $\overline{S2}$ have timing identical to $\overline{S1}$. On this diagram, when $\overline{S1}$ is LOW, $\overline{S2}$ is LOW and S2 is HIGH. When $\overline{S1}$ is HIGH, $\overline{S2}$ is HIGH and S2 is LOW.

3. ZZ = LOW fix.

DON'T CARE

UNDEFINED

(6) SNOOZE MODE TIMING



Note 1. $\overline{S2}$ and S2 have timing identical to $\overline{S1}$. On this diagram, when $\overline{S1}$ is LOW, $\overline{S2}$ is LOW and S2 is HIGH.
When $\overline{S1}$ is HIGH, $\overline{S2}$ is HIGH and S2 is LOW.

2. On this timing chart, $\overline{ADSP}$ = HIGH fix, $\overline{ADV}$ = X.

3. $\overline{ADSP}$ and $\overline{ADSC}$ must not be asserted during tZZS and tZZREC, due to a guarantee of data retention for snooze mode.
If synchronous inputs are made combinations of WRITE state during tZZS and tZZREC, memorized data may be destroyed.

DON'T CARE

UNDEFINED

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